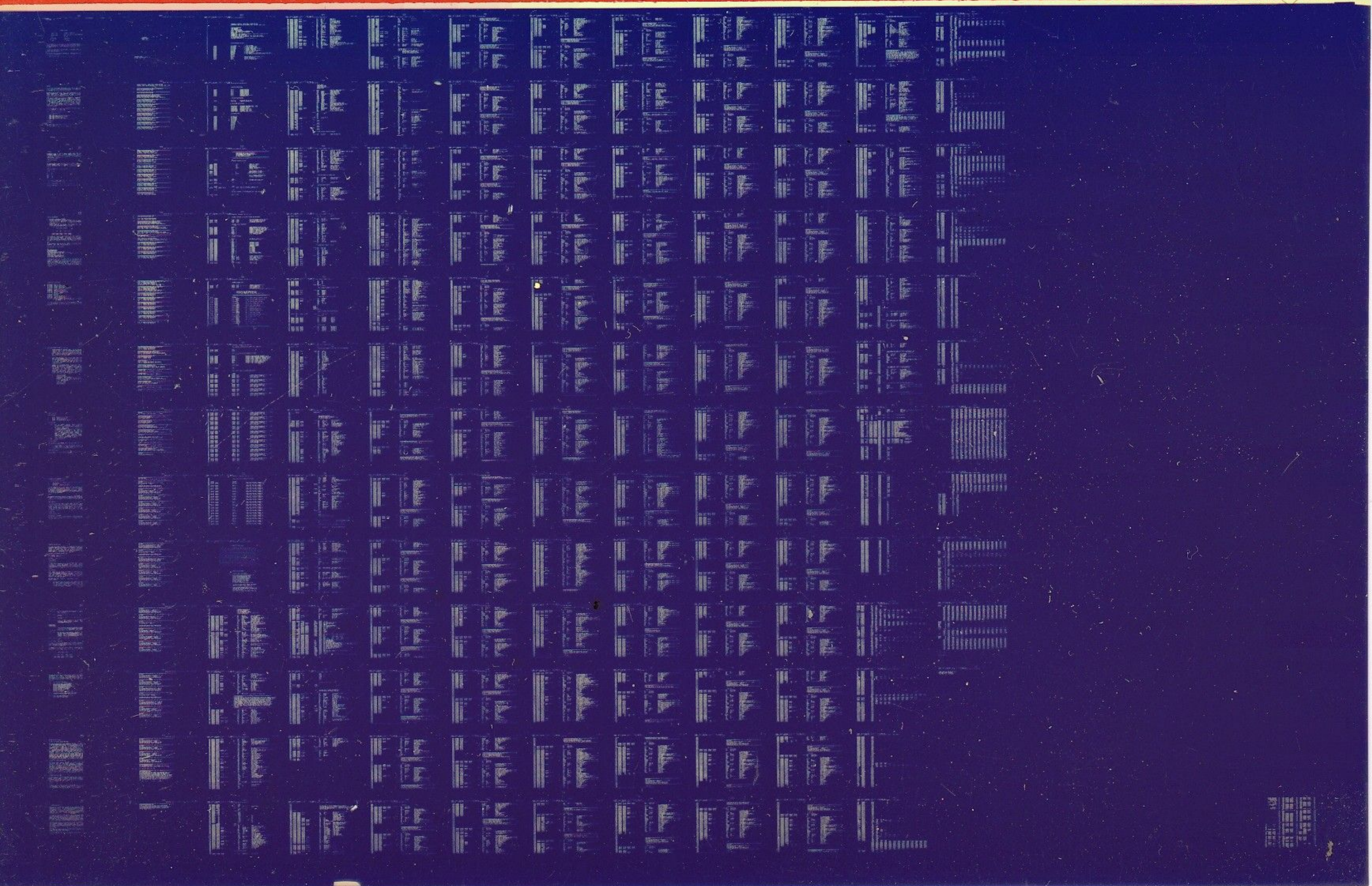


DMC11

BASIC W/R AND MICROPROC
MD-11-DZDMC-B

EP-DZDMC-B-DL-A
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PDP10 PAGE: 0001

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PDP10 411

KIHDR1DZDMCBSEQ

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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZDMC-B-D
PRODUCT NAME: BASIC W/R AND MICRO-PROCESSOR TESTS
DATE: MAY 1977
MAINTAINER: DIAGNOSTICS
AUTHOR: FAY BASHAW

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1. ABSTRACT

The function of the DMC11 diagnostics is to verify that the option operates according to specifications. The diagnostics verify that there are no malfunctions and that all operations of the DMC11 are correct in its environment.

Parameters must be set up to alert the diagnostics to the DMC11 configuration. These parameters are contained in the STATUS TABLE and are generated in two ways: 1) Manual Input - the operator answers questions. 2) Autosizing - the program determines the parameters automatically.

DZDMC tests the DMC11 micro-processor (MB200-YA or MB200-YB). It performs write/read tests on the DMC unibus registers, checks the micro-processor operation, checks out Main Memory, scratch pad memory, the ALU functions as well as interrupts and NPR operation. DZDMC performs no tests on the line unit or any CROM dependent tests. It does not require a line unit to run. NOTE: This diagnostic will run on a KMC11 (MB204), however it is not advised that this diagnostic be used to check a KMC11, rather you should check a KMC11 with the KMC11 diagnostic package.

Currently there are five off line diagnostics that are to be run in sequence to insure that if an error should occur it will be detected at an early stage.

NOTE: Additional diagnostics may be added in the future.

The five diagnostics are:

1. DZDMC [REV] Basic W/R and Micro-processor tests
2. DZDME [REV] DDCMP Line unit tests
3. DZDMF [REV] BITSTUFF Line unit tests
4. DZDMG [REV] Jump and CROM tests
5. DZDMH [REV] Free-running tests (Heat test tape)

2. REQUIREMENTS

2.1 EQUIPMENT

Any PDP11 family CPU (except an LSI-11) with minimum 8k memory
 ASP 33 (or equivalent)
 DMC11-AP (MB200-YA) or a DMC11-AL (MB200-YB)

2.2 STORAGE

Program will use all BK of memory except where ABL and BOOTSTRAP LOADER reside. Locations 1500 thru 1640; contain the "STATUS TABLE" information which is generated at start of diagnostics by manual input (questions) or automatically (auto-sizing). This area is an overlay area and should not be altered by the operator.

3. LOADING PROCEEDURE

3.1 METHOD

All programs are in absolute format and are loaded using the ABSOLUTE LOADER. NOTE: if the diagnostics are on a media such as DISK, MAGTAPE, DECTAPE, or CASSETTE; follow instructions for the monitor which has been provided on that specific media.

ABSOLUTE LOADER starting address *500

MEMORY * SIZE

4k	17
8k	37
12k	57
16k	77
20k	117
24k	137
28k	157

- 3.1.1 Place address of ABS loader into switch register.
(also place 'HALT' SW up)
- 3.1.2 Depress 'LOAD ADDRESS' key on console and release.
- 3.1.3 Depress 'START KEY' on console and release (program should now be loading into CPU)

4. STARTING PROCEDURE

- a. Set switch register to 000200
- b. Depress 'LOAD ADDRESS' key and release
- c. Set SWR to zero for 'AUTO SIZING' or SWR bit0=1 for manual input (questions) or SWR bit7=1 to use existing parameters set up by a previous start or a previously run DMC11 diagnostic.
- d. Depress 'START KEY' and release. The program will type Maindec Name and program name (if this was the first start up of the program) and also the following:

MAP OF DMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
001500	160010	145310	177777	000000
001510	160020	145320	177777	000000

The program will type 'R' and proceed to run the diagnostic. The above is only an example. This would indicate the status table starting at add. 1500 in the program. In this example the table contains the information and status of two DMC11'S. THE STATUS TABLE MUST BE VERIFIED BY THE USER IF AUTO SIZING IS DONE. For information of status table see section 8.4 for help.

If the diagnostic was started with SW00=1 indicating manual parameter input then the following shows an example of the questions asked and some example answers:

HOW MANY DMC11'S TO BE TESTED?1

0'

CSR ADDRESS?160010

VECTOR ADDRESS?310

BR PRIORITY LEVEL? (4,5,6,7)?5

DOES MICRO-PROCESSOR HAVE CRAM? (Y OR N)N

WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF M8202 TYPE "2"?1

IS THE LOOP BACK CONNECTOR ON?Y

SWITCH PAC#1 (DDCMP LINE#)?377

SWITCH PAC#2 (BMB73 BOOT ADD)?377

Following the questions the status map is printed out as described above. the information in the map reflects the answers to the questions. If the diagnostic was started with SW00=0 and SW07=0 (AUTO-SIZING) then no questions are asked and only the status-map is printed out. If AUTO-SIZING is used the status information must be verified to be correct (match the hardware). if it does not match the hardware the diagnostic must be restarted with SW00=1 and the questions answered.

4.1 CONTROL SWITCH SETTINGS

SW 15 Set: Halt on error
 SW 14 Set: Loop on current test
 SW 13 Set: Inhibit error print out
 SW 12 Set: Inhibit type out/abell on error.
 SW 11 Set: Inhibit iterations. (quick pass)
 SW 10 Set: Escape to next test on error
 SW 09 Set: Loop with current data
 SW 08 Set: Catch error and loop on it
 SW 07 Set: Use previous status table.
 SW 06 Set: Halt in ROMCLK routine before clocking
 micro-processor
 SW 05 Set: Reserved
 SW 04 Set: Reserved
 SW 03 Set: Reselect DMC11's desired active
 SW 02 Set: Lock on selected test
 SW 01 Set: Restart program at selected test
 SW 00 Set: Build new status table from questions. (If SW07=0
 and SW00=0 a new status table is built by
 auto-sizing)

Switch 06 and 08-15 are dynamic and can be changed as needed while the diagnostic is running. Switches 00-03 and switch 07 are static, and are used only on starting or restarting the diagnostic.

4.1.2 SWITCH REGISTER OPTIONS (at start up)

SW 01 RESTART PROGRAM AT SELECTED EST. It is strongly suggested that at least one pass has been made before trying to select a test, the reason being is that the program has to clear areas and set up parameters. When this switch is used the diagnostic will ask TEST NO.? Answer by typing the number of the test desired and carriage return to begin execution at the selected test.

SW 02 LOCK ON SELECTED TEST. This switch when used with SW01 will cause the program to constantly loop on the selected test. Hitting any key on the console will let it advance to the next test and loop until a key is hit again. If SW02=0 when SW01 is used. The program will begin at the selected test and continue normal operations.

SW 03 RESELECT DMC11'S DESIRED ACTIVE. Please note that a message is typed out for setting the switch register equal to DMC11's active. this means if the system has four DMC11s; bits 00,01,02,03 will be set in loc 'DMACTV' from the switch register. Using this switch(SW00) alters that location; therefore if four DMC11s are in the system ***DO NOT*** set switches greater than SW 03 in the up position. this would be a fatal error. do not select more active DMC11s than there is information on in the status table.

METHOC: A: Load address 200
 B: Start with SW 00=1
 C: Program will type message
 D: Set a switch for each DMC desired active.
 EXAMPLE: If you have 4 DMC's but only want to run the first and the last set SWR bits 0 and 3 = 1. PRESS CONTINUE
 E: Number (IF VALID) will be in data lights (excluding 11/05)
 F: Set with any other switch settings desired. PRESS CONTINUE.

4.1.3 DYNAMIC SWITCHES

ERROR SWITCHES

1. SW 12 Delete print out/bell on error.
2. SW 13 Delete error printout.
3. SW 15 Halt on the error.
4. SW 08 Goto beginning of the test(on error).
5. SW 10 Goto next test(on error).

SCOPE SWITCHES

1. SW06 Halt in ROMCLK routine before clocking micro-processor instruction. This allows the operator to scope a micro-processor instruction in the static state before it is clocked. Hit continue to resume running.
2. SW09 (if enabled by 'SCOPI') on an error; If an '*' is printed in front of the test no. (ex. *TEST NO. 10) SW09 is incorporated in that test and therefore SW09 is usually the best switch for the scope loop (SW14=0, SW10=0, SW09=1, SW08=0). If SW09 is not enabled; and there is a HARD error (constant); SW08 is best. (SW14=1,0, SW10=0, SW09=0, SW08=1). for intermittent errors; SW14=1 will loop on test regardless of error or not error. (SW14=1, SW10=0, SW09=0, SW08=1,0)
3. SW11 Inhibit interations.
4. SW14 Loop on current test.

4.2 STARTING ADDRESS

Starting address is at 000200 there are no other starting addresses for the DMC11 diagnostics. (See Section 4.0)

NOTE: If address 000042 is non-zero the program assumes it is under ACT11 or XXDP control and will act accordingly after all available DMC11's are tested the program will return to 'XXDP' or 'ACT-11'.

5. OPERATING PROCEDURE

When program is initially started messages as described in section 4.0 will be printed, and program will begin running the diagnostic

5.2 PROGRAM AND OR OPERATOR ACTION

The typical approach should be

1. Halt on error (via SW 15=1) when ever an error occurs.
2. Clear SW 15.
3. Set SW 14: (loop on this test)
4. Set SW 13: (inhibit error print out)

The TEST NUMBER and PC will be typed out and possibly an error message (this depends on the test) to give the operator an idea as to the source of the problem. If it is necessary to know more information concerning the error report; LOOK IN THE LISTING for that TEST NUMBER which was typed out and then NOTE THE PC of the ERROR REPORT this way the EXACT FUNCTION of the test CAN BE DETERMINED.

5. ERRORS

As described previously there will always be a TEST NUMBER and PC typed out at the time of an error (providing SW 13=0 and SW 12=0). in most cases additional information will be supplied in the the error message to give the operator an indication of the error.

5.2 ERROR RECOVERY

If for some reason the DMC11 should 'HANG THE BUS' (gain control of bus so that console manual functions are inhibited) an init or power down/up is necessary for operator to regain control of cpu. If this should happen; look in location 'TSTNO' (address 1226) for the number of the test that was running at the time of the catastrophic error. In this way the operator will have an idea as to what the DMC11 was doing at the time of the error.

7. RESTRICTIONS

7.1 STARTING RESTRICTIONS

See section 4. (PLEASE)
Status table should be verified regardless of how program was started. Also it is important to use this listing along with the information printed on the TTY to completely isolate problems.

7.2 OPERATING RESTRICTIONS

The first time a DMC11 diagnostic is loaded into core and run the STATUS TABLE must be set up. This is done by manual input (SW00=1) or by autosizing (SW00=0 and SW07=0). Thereafter however the status table need not be setup by subsequent restarts or even loading the next DMC diagnostic because the STATUS TABLE is overlaid. The current parameters in the STATUS TABLE are used when SW07=1 on start up.

7.3 HARDWARE CONFIGURATION RESTRICTIONS

DMC11(MB200)- Jumper W1 must be in, and switch 7 of E76 must be in the OFF position.

KMC(MB204)- Jumper W1 must be in.

8. MISCELLANEOUS

8.1 EXECUTION TIME

All DMC11 device diagnostics will give an 'END PASS' message (providing no errors and sw12=0) within 4 mins. This is assuming SW11=1 (DELETE ITERATIONS) is set to give the fastest possible execution. The actual execution time depends greatly on the PDF11 CPU configuration and the amount of memory in the system.

8.2 PASS COMPLETE

NOTE: EVERY time the program is started; the tests will run as if SW11 (delete iterations) was up (=1). This is to 'VERIFY NO HARD ERRORS' as soon as possible. Therefore the first pass -EACH TIME PROGRAM IS STARTED- will be a 'QUICK PASS' until all DMC11's in system are tested. When the diagnostic has completed a pass the following is an example of the print out to be expected.

```
END PASS DZDMC CSR: 175000 VEC: 0300 PASSES: 000001
ERRORS: 000000
```

NOTE: The pass count and error counts are cumulative for each DMC11 that is running, and are set to zero only when the diagnostic is started. Therefore after an overnight run for example, the total passes and errors for each DMC11 since the diagnostic was started are reflected in PASSES: and ERRORS:.

B.4 KEY LOCATIONS

RETURN (1214) Contains the address where program will return when iteration count is reached or if loop on test is asserted.

NEXT (1216) Contains the address of the next test to be performed.

TSTNO (1226) Contains the number of the test now being performed.

RUN (1316) The bit in 'RUN' always points to the DMC11 currently being tested. EXAMPLE: (RUN) 1302/0000000001000000 Means that DMC11 no.06 is the DMC11 now running.

DMC00-DMC17
DMST00-DMST17
(1500)-(1640)

These locations contain the information needed to test up to 16 (decimal) DMC11s sequentially. they contain the CSR, VECTOR and STATUS concerning the configuration of each DMC11.

DMACTV (1306) Each bit set in this location indicates that the associated DMC11 will be tested in turn. EXAMPLE: (DMACTV) 1276/0000000000011111 means that DMC11 no. 00,01,02,03,04 will be tested. EXAMPLE: (DMACTV) 1276/0000000000010001 Means that DMC11 no. 00,04 will be tested.

DMCSR (1404) Contains the CSR of the current DMC11 under test.

B.4A 'STATUS TABLE' (1500-1640)

The table is filled by AUTO SIZING or by the manual parameter input (questions) as described previously. Also if desired by user; the locations may be altered by hand (toggled in) to suit the specific configuration.

The example status map shown below contains information for two DMC11'S. the table can contain up to 16 DMC11'S. Following the map is a description of the bits for each map entry

MAP OF DMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
001500	160010	145310	177777	000000
001510	160020	016320	000000	000000

Each map entry contains 4 words which contain the status information for 1 DMC11. The PC shows where in core memory the first of the 4 words is. In the example above the first DMC'S status is in locations, 1500, 1502, 1504, and 1506. The second DMC status is located at 1510, 1512, 1514, and 1516. The information contained in each 4 word entry is defined as follows:

CSR: Contains DMC11 CSR address

STAT1: BITS 00-08 IS DMC11 VECTOR ADDRESS
 BIT15=1 MICRO-PROCESSOR HAS CRAM
 BIT15=0 MICRO-PROCESSOR HAS CROM
 BIT14=1 TURNAROUND CONNECTOR IS ON
 BIT14=0 NO TURNAROUND CONNECTOR
 BIT13=0 LINE UNIT IS AN M8201
 BIT13=1 LINE UNIT IS AN M8202
 BIT12=1 NO LINE UNIT
 BITS 09-11 IS DMC11 BR PRIORITY LEVEL

STAT2: LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)
 HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)

STAT3: BIT0=1 RUN FREE RUNNING TESTS ON KMC11
 BIT1=0 DMC11-AR (LOW SPEED)
 BIT1=1 DMC11-AL (HIGH SPEED)

8.5 METHOD OF AUTO SIZING

8.5.1 FINDING THE CONTROL STATUS REGISTER.

The auto-sizing routine finds a DMC11 as follows: It starts at address 160000 and tests all address in increments of 10 up to and including address 167760. If the address does not time out, the following is done, the first CROM address is written to a 125252 then it is read back. If it contains a -1 or 125252 or 626 or 16520 a DMC11 or KMC11 has been found, if not, the address is updated by 10 and the search continues. A -1 indicates a DMC11 with no CROM, a 125252 indicates a KMC11 with CROM, a 626 indicates a DMC11-AL and a 16520 indicates a DMC11-AR. Further tests are performed at this point to determine which line unit, if any, is installed, if a loop-back connector is installed and various switch settings on the line unit. THIS IS WHY THE STATUS TABLE MUST BE VERIFIED BY THE USER AND IF ANY OF THE INFORMATION DOES NOT AGREE WITH THE HARDWARE THE DIAGNOSTIC MUST BE RESTARTED AND THE QUESTIONS MUST BE ANSWERED. All DMC11's in the system will be found by the auto-sizer. If it does not find a DMC11 the diagnostic must be restarted and the questions answered.

8.5.2 FINDING THE VECTOR AND BR LEVEL

The vector area (address 300-776) is filled with the instruction IOT and '+2' (next address). The processor status is started at 7 and the DMC is programmed to interrupt. The PS is lowered by 1 until the DMC interrupts, a delay is made and if no interrupt occurs at PS level 3 (because of a bad DMC11) the program assumes vector address 300 at BR level 5 and the problem should be fixed in the diagnostic. Once the problem is fixed; the program should be re-setup again to get correct vector. If an interrupt occurred; the address to which the DMC11 interrupted to is picked up and reported as the vector. NOTE: if the vector reported is not the vector set up by you; there is a problem and AUTO SIZING should not be done.

8.5 SOFTWARE SWITCH REGISTER

If the diagnostic is run on an 11/04 or other CPU without a switch register then a software switch register is used to allow user the same switch options as described previously. If the hardware switch register does not exist or if one does and it contains all ones (177777) this software switch register is used.

Control:

To obtain control at any allowable time during execution of the diagnostic the operator types a CTRL G on the console terminal keyboard. As soon as the CTRL G is recognized, by the diagnostic, the following message will be displayed:

SWR=XXXXXX NEW?

Where XXXXXX is the current contents of the software switch register in octal. The software control routine will then await operator action. At which time the operator is required to type one or more of the legal characters: 1) 0 - 7, 2) line feed(<LF>), 3) carriage return(<CR>), or 4) control-U (CTRL U). No check is made for legality. If the input character is not a <LF>, <CR>, or CTRL U it is assumed to be an octal digit.

To change the contents of the SSR the operator simply types the new desired value in octal - leading zeros need not be typed. And terminates the input string with a <CR> or <LF> depending on the program action desired as described below. The input value will be truncated to the last 6 digits typed. At least one digit must be typed on any given input string prior to the terminator before a change to the SSR will occur.

When the input string is terminated with a <CR> the diagnostic will continue execution from the point at which it was interrupted. If a <CR> is the only thing typed the program will continue without changing the SSR. The <LF> differs from the <CR> by restarting the program as if it were restarted at address 200.

If a CTRL U is typed at any point in the input string prior to the terminator the input value will be disregarded and the prompt displayed (SWR = XXXXXX NEW?).

To set the SSR for the starting switches, first load the diagnostic, then hit CTRL G, then start the diagnostic.

DZDMC LST

B02

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DOCUMENT

DZDMC LST

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6 MAINDEC-11-DZDMC-B BASIC DMC11 CONTROLLER TEST
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1668 ***** TEST 1 *****
VERIFY THAT REFERENCING UNIBUS DEVICE REGISTERS
DOES NOT CAUSE A TIME OUT TRAP

1697 ***** TEST 2 *****
VERIFY THAT RUN CAN BE CLEARED

1714 ***** TEST 3 *****
UNIBUS REGISTER WORD DUAL ADDRESSING TEST
LOAD ALL REGISTERS WITH INCREMENTING PATTERN
READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING

1756 ***** TEST 4 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT0, VERIFY BIT0 WAS SET
CLEAR BIT0, VERIFY BIT0 WAS CLEARED

1786 ***** TEST 5 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT1, VERIFY BIT1 WAS SET
CLEAR BIT1, VERIFY BIT1 WAS CLEARED

1816 ***** TEST 6 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT2, VERIFY BIT2 WAS SET
CLEAR BIT2, VERIFY BIT2 WAS CLEARED

1846 ***** TEST 7 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BITS, VERIFY BITS WAS SET
CLEAR BITS, VERIFY BITS WAS CLEARED

1876 ***** TEST 10 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT6, VERIFY BIT6 WAS SET
CLEAR BIT6, VERIFY BIT6 WAS CLEARED

1906 ***** TEST 11 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT7, VERIFY BIT7 WAS SET
CLEAR BIT7, VERIFY BIT7 WAS CLEARED

1936 ***** TEST 12 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT9, VERIFY BIT9 WAS SET
CLEAR BIT9, VERIFY BIT9 WAS CLEARED

1966 ***** TEST 13 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT11, VERIFY BIT11 WAS SET
CLEAR BIT11, VERIFY BIT11 WAS CLEARED

1996 ***** TEST 14 *****
CONTROL STATUS REGISTER WRITE/READ TEST
SET BIT12, VERIFY BIT12 WAS SET
CLEAR BIT12, VERIFY BIT12 WAS CLEARED

2026 ***** TEST 15 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT0, VERIFY BIT0 WAS SET
CLEAR BIT0, VERIFY BIT0 WAS CLEARED

2056 ***** TEST 16 *****
2057 CONTROL OUT REGISTER WRITE/READ TEST
SET BIT1, VERIFY BIT1 WAS SET
CLEAR BIT1, VERIFY BIT1 WAS CLEARED

2086 ***** TEST 17 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT2, VERIFY BIT2 WAS SET
CLEAR BIT2, VERIFY BIT2 WAS CLEARED

2116 ***** TEST 20 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT6, VERIFY BIT6 WAS SET
CLEAR BIT6, VERIFY BIT6 WAS CLEARED

2146 ***** TEST 21 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT7, VERIFY BIT7 WAS SET
CLEAR BIT7, VERIFY BIT7 WAS CLEARED

2176 ***** TEST 22 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT12, VERIFY BIT12 WAS SET
CLEAR BIT12, VERIFY BIT12 WAS CLEARED

2206 ***** TEST 23 *****
CONTROL OUT REGISTER WRITE/READ TEST
SET BIT13, VERIFY BIT13 WAS SET
CLEAR BIT13, VERIFY BIT13 WAS CLEARED

2236 ***** TEST 24 *****
PORT4 REGISTER WRITE/READ TEST
FLOAT A ONE THROUGH PORT4 REGISTER
FLOAT A ZERO THROUGH PORT4 REGISTER

2279 ***** TEST 25 *****
PORT6 REGISTER WRITE/READ TEST

2281 FLOAT A ONE THROUGH PORT6 REGISTER
FLOAT A ZERO THROUGH PORT6 REGISTER

2322 ***** TEST 26 *****
UNIBUS REGISTER BYTE DUAL ADDRESSING TEST
LOAD ALL REGISTERS WITH INCREMENTING PATTERN
READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING

2364 ***** TEST 27 *****
MAINTENANCE INSTRUCTION REGISTER TEST
VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS'
AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A BUS RESET.

2425 ***** TEST 30 *****
MAINTENANCE INSTRUCTION REGISTER TEST
VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS'
AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A MASTER RESET.

2446 ***** TEST 31 *****
MICRO PROCESSOR TEST
LOAD DMPO6 WITH A MICRO-PROCESSOR INSTRUCTION, CLOCK IT

2449 VERIFY INSTRUCTION EXECUTED PROPERLY
INSTRUCTION SHOULD MOVE IBUS*4 TO IBUS*5, IBUS*4 IS ALL 1'S
AND IBUS*5 IS ALL 0'S. RESULT SHOULD BE ALL 1'S IN SEL4

2473 ***** TEST 32 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS* REGISTER 0
FLOAT A 0 THROUGH IBUS* REGISTER 0

2529 ***** TEST 33 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS* REGISTER 2
FLOAT A 0 THROUGH IBUS* REGISTER 2

2585 ***** TEST 34 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS* REGISTER 4
FLOAT A 0 THROUGH IBUS* REGISTER 4

2637 ***** TEST 35 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
FLOAT A 1 THROUGH IBUS* REGISTER 5
FLOAT A 0 THROUGH IBUS* REGISTER 5

2689 ***** TEST 36 *****
 MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
 FLOAT A 1 THROUGH IBUS* REGISTER 10
 FLOAT A 0 THROUGH IBUS* REGISTER 10
 THE NPR RQ BIT (BIT 0) IS MASKED DURING THIS TEST

2746 ***** TEST 37 *****
 MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
 FLOAT A 1 THROUGH IBUS* REGISTER 11
 FLOAT A 0 THROUGH IBUS* REGISTER 11
 THE BR RQ BIT, PGM CLOCK BIT, FORCE POWER FAIL BIT
 (BITS 7,4,1) ARE ALL MASKED DURING THIS TEST

2808 ***** TEST 40 *****
 MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
 FLOAT A 1 THROUGH IBUS REGISTER 0
 FLOAT A 0 THROUGH IBUS REGISTER 0

2860 ***** TEST 41 *****
 MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
 FLOAT A 1 THROUGH IBUS REGISTER 1
 FLOAT A 0 THROUGH IBUS REGISTER 1

2912 ***** TEST 42 *****
 MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
 FLOAT A 1 THROUGH IBUS REGISTER 2
 FLOAT A 0 THROUGH IBUS REGISTER 2

2964 ***** TEST 43 *****
 MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
 FLOAT A 1 THROUGH IBUS REGISTER 3
 FLOAT A 0 THROUGH IBUS REGISTER 3

3016 ***** TEST 44 *****
 MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
 FLOAT A 1 THROUGH IBUS REGISTER 4
 FLOAT A 0 THROUGH IBUS REGISTER 4

3068 ***** TEST 45 *****
 MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
 FLOAT A 1 THROUGH IBUS REGISTER 5
 FLOAT A 0 THROUGH IBUS REGISTER 5

3120 ***** TEST 46 *****
 3121 MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
 FLOAT A 1 THROUGH IBUS REGISTER 6
 FLOAT A 0 THROUGH IBUS REGISTER 6

- 3172 ***** TEST 47 *****
 MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
 FLOAT A 1 THROUGH IBUS REGISTER 7
 FLOAT A 0 THROUGH IBUS REGISTER 7

- 3224 ***** TEST 50 *****
 MICRO PROCESSOR IBUS DUAL ADDRESS TEST
 WRITE ALL IBUS REGISTERS WITH INCREMENTING PATTERN
 READ ALL IBUS REGISTERS TO VERIFY CORRECT ADDRESSING

- 3285 ***** TEST 51 *****
 MICRO PROCESSOR BR REGISTER TEST
 FLOAT A 1 THROUGH THE BR
 FLOAT A 0 THROUGH THE BR

- 3336 ***** TEST 52 *****
 SCRATCH PAD TEST
 FLOAT A 1 THROUGH EACH SCRATCH PAD LOCATION
 FLOAT A 0 THROUGH EACH SCRATCH PAD LOCATION

- 3432 ***** TEST 53 *****
 SCRATCH PAD DUAL ADDRESSING TEST
 WRITE AN INCREMENTING PATTERN IN ALL SP LOCATIONS
 READ ALL SP LOCATIONS TO VERIFY CORRECT ADDRESSING

- 3462 ***** TEST 54 *****
 INTERRUPT TEST
 TEST THAT DEVICE CAN INTERRUPT TO VECTOR A

- 3491 ***** TEST 55 *****
 INTERRUPT TEST
 TEST THAT DEVICE CAN INTERRUPT TO VECTOR B

- 3519 ***** TEST 56 *****
 PRIORITY INTERRUPT TESTS
 SET PS TO ALL BR LEVELS EQUAL OR GREATER THAN
 THE DMC11 LEVEL, VERIFY THAT DMC11 DOES NOT INTERRUPT

- 3557 ***** TEST 57 *****
 PRIORITY INTERRUPT TESTS
 SET PS TO ALL BR LEVELS LESS THAN THE DMC11 LEVEL
 VERIFY THAT THE DMC11 WILL INTERRUPT

- 3601 ***** TEST 60 *****
 NPR TEST
 TEST OF DAT0, 1 WORD FROM UPROC TO 11 MEMORY

- 3634 ***** TEST 61 *****
 NPR TEST
 TEST OF DAT1, 1 WORD FROM 11 MEMORY TO UPROC

- 3670 ***** TEST 62 *****
NPR TEST
TEST OF DATOB, 1 BYTE FROM UPROC TO 11 MEMORY
- 3702 ***** TEST 63 *****
TEST OF EA BITS 16 AND 17
DO A DATO TO AN ADDRESS USING OUT BA BITS 16 AND 17
VERIFY CORRECT RESULTS
- 3741 ***** TEST 64 *****
TEST OF EA BITS 16 AND 17
DO A DATI USING IN BA BITS 16 AND 17
VERIFY CORRECT RESULTS
- 3777 ***** TEST 65 *****
NPR NON-EXISTENT MEMORY TEST
DO A DATO TO A NON-EXISTENT ADDRESS
VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11
- 3812 ***** TEST 66 *****
NPR NON-EXISTENT MEMORY TEST
DO A DATI FROM A NON-EXISTENT ADDRESS
VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11
- 3847 ***** TEST 67 *****
NPR TEST
- 3849 USING DATO, NPR A BINARY COUNT (0-377)
FROM MICRO-PROCESSOR TO ALL AVAILABLE MEMORY
- 3903 ***** TEST 70 *****
MAIN MEMORY TEST
- 3905 FLOAT A 1 THROUGH ALL MAIN MEMORY LOCATIONS
- 3943 ***** TEST 71 *****
MAIN MEMORY TEST
FLOAT A 0 THROUGH ALL MAIN MEMORY LOCATIONS
- 3985 ***** TEST 72 *****
MAIN MEMORY DUAL ADDRESSING TEST
LOAD EACH MEMORY LOCATION WITH ITS OWN ADDRESS
READ BACK EACH LOCATION TO VERIFY CORRECT ADDRESSING
- 4041 ***** TEST 73 *****
MAR TEST
PERFORM DUAL ADDRESSING TEST
USING MAR AUTO-INC FEATURE

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4087 ***** TEST 74 *****
ALU C BIT TEST
TEST THAT AN ADD OF 377 AND 377 WILL SET THE C BIT

4125 ***** TEST 75 *****
ALU TEST
TEST OF ALU FUNCTION SEL B WITH C BIT CLEARED
ALU FUNCTION (B) CODE=11

4129 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4174 ***** TEST 76 *****
ALU TEST
TEST OF ALU FUNCTION SEL A WITH C BIT CLEARED
ALU FUNCTION (A) CODE=10
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4223 ***** TEST 77 *****
ALU TEST
TEST OF ALU FUNCTION A OR NOTB WITH C BIT CLEARED
ALU FUNCTION (A OR NOTB) CODE=12
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4272 ***** TEST 100 *****
ALU TEST
TEST OF ALU FUNCTION A AND B WITH C BIT CLEARED
ALU FUNCTION (A AND B) CODE=13
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4321 ***** TEST 101 *****
ALU TEST
TEST OF ALU FUNCTION A OR B WITH C BIT CLEARED
ALU FUNCTION (A OR B) CODE=14
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4370 ***** TEST 102 *****
ALU TEST
TEST OF ALU FUNCTION A XOR B WITH C BIT CLEARED
ALU FUNCTION (A XOR B) CODE=15
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4419 ***** TEST 103 *****
ALU TEST
TEST OF ALU FUNCTION ADD WITH C BIT CLEARED
ALU FUNCTION (A PLUS B) CODE=00
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS
    
```


4468 ***** TEST 104 *****
ALU TEST
TEST OF ALU FUNCTION 2A W/C WITH C BIT CLEARED
ALU FUNCTION (A PLUS A PLUS C) CODE=6
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4517 ***** TEST 105 *****
ALU TEST
TEST OF ALU FUNCTION SUB WITH C BIT CLEARED
ALU FUNCTION (A-B) CODE=16

4521 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4566 ***** TEST 106 *****
ALU TEST
TEST OF ALU FUNCTION ADD W/C WITH C BIT CLEARED
ALU FUNCTION (A PLUS B PLUS C) CODE=01
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4615 ***** TEST 107 *****
ALU TEST
TEST OF ALU FUNCTION SUB W/C WITH C BIT CLEARED
ALU FUNCTION (A-B-C) CODE=2
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4664 ***** TEST 110 *****
ALU TEST
TEST OF ALU FUNCTION INC A WITH C BIT CLEARED
ALU FUNCTION (A PLUS 1) CODE=3
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4713 ***** TEST 111 *****
ALU TEST
TEST OF ALU FUNCTION 2A WITH C BIT CLEARED
ALU FUNCTION (A PLUS A) CODE=5
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4762 ***** TEST 112 *****
ALU TEST
TEST OF ALU FUNCTION A PLUS C WITH C BIT CLEARED
ALU FUNCTION (A PLUS C) CODE=4
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4811 ***** TEST 113 *****
ALU TEST
TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT CLEARED
ALU FUNCTION (A-B-1) CODE=17
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

486C ***** TEST 114 *****
ALU TEST
TEST OF ALU FUNCTION DEC A WITH C BIT CLEARED
ALU FUNCTION (A-1) CODE=7
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4909 ***** TEST 115 *****
ALU TEST
TEST OF ALU FUNCTION SEL B WITH C BIT SET
ALU FUNCTION (B) CODE=1!

4913 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4958 ***** TEST 116 *****
ALU TEST
TEST OF ALU FUNCTION SEL A WITH C BIT SET
ALU FUNCTION (A) CODE=10
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5007 ***** TEST 117 *****
ALU TEST
TEST OF ALU FUNCTION A OR NOTB WITH C BIT SET
ALU FUNCTION (A OR NOTB) CODE=12
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5056 ***** TEST 120 *****
ALU TEST
TEST OF ALU FUNCTION A AND B WITH C BIT SET
ALU FUNCTION (A AND B) CODE=13
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5105 ***** TEST 121 *****
ALU TEST
TEST OF ALU FUNCTION A OR B WITH C BIT SET
ALU FUNCTION (A OR B) CODE=14
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5154 ***** TEST 122 *****
ALU TEST
TEST OF ALU FUNCTION A XOR B WITH C BIT SET
ALU FUNCTION (A XOR B) CODE=15
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5203 ***** TEST 123 *****
ALU TEST
TEST OF ALU FUNCTION ADD WITH C BIT SET
ALU FUNCTION (A PLUS B) CODE=00
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5252 ***** TEST 124 *****
ALU TEST
TEST OF ALU FUNCTION 2A W/C WITH C BIT SET
ALU FUNCTION (A PLUS A PLUS C) CODE=6
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5301 ***** TEST 125 *****
ALU TEST
TEST OF ALU FUNCTION SUB WITH C BIT SET
ALU FUNCTION (A-B) CODE=16

5305 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5350 ***** TEST 126 *****
ALU TEST
TEST OF ALU FUNCTION ADD W/C WITH C BIT SET
ALU FUNCTION (A PLUS B PLUS C) CODE=01
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5399 ***** TEST 127 *****
ALU TEST
TEST OF ALU FUNCTION SUB W/C WITH C BIT SET
ALU FUNCTION (A-B-C) CODE=2
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5448 ***** TEST 130 *****
ALU TEST
TEST OF ALU FUNCTION INC A WITH C BIT SET
ALU FUNCTION (A PLUS 1) CODE=3
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5497 ***** TEST 131 *****
ALU TEST
TEST OF ALU FUNCTION 2A WITH C BIT SET
ALU FUNCTION (A PLUS A) CODE=5
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5546 ***** TEST 132 *****
ALU TEST
TEST OF ALU FUNCTION A PLUS C WITH C BIT SET
ALU FUNCTION (A PLUS C) CODE=4
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5595 ***** TEST 133 *****
ALU TEST
TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT SET
ALU FUNCTION (A-B-1) CODE=17
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5644 ***** TEST 134 *****
ALU TEST
TEST OF ALU FUNCTION DEC A WITH C BIT SET
ALU FUNCTION (A-1) CODE=7
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5693 ***** TEST 135 *****
TEST OF PROGRAM CLOCK BIT
DO A MASTER CLEAR, VERIFY THAT PROGRAM CLOCK IS SET
WRITE PROGRAM CLOCK BIT TO A ONE, VERIFY THAT IT CLEARS.

5697 AND THEN SETS SOME TIME LATER

5734 ***** TEST 136 *****
FORCE POWER FAIL TEST
SET FORCE POWER FAIL BIT VERIFY THAT PROCESSOR TRAPS TO 24
GOING DOWN AND COMING UP. VERIFY ALSO THAT BUS INIT WAS
BLOCKED FROM GETTING TO THE DMC DURING THE POWER FAIL
THIS TEST MAY HANG ON SOME PROCESSORS IF AN M9301 IS PRESENT.
TO AVOID HANGING SW02 (POWER ON REBOOT ENABLE) ON THE M9301
MUST BE IN THE OFF POSITION. THIS TEST WILL ALSO FAIL IF THE
CPU POWER FAIL VECTOR IS SET TO ANY LOCATION OTHER THAN 24.
IF THIS TEST HANGS OR FAILS DUE TO EITHER REASON ABOVE THE
FOLLOWING PATCH MAY BE INSTALLED TO SKIP THIS TEST:

LOC 33362

WAS 33532

SB 33724

N02

DZDMC LST

5789

***** TEST 137 *****
MICRO-PROCESSOR NOISE TEST
WRITE ALL ZERO'S THEN ALL ONE'S THEN A DATA PATTERN
TO THE IBUS* AND IBUS REGISTERS AND TO THE SP AND MAIN MEM
THEN GO BACK AND READ THE DATA PATERNS TO VERIFY THAT
READING AND WRITING OF OTHER LOCATIONS AND REGISTERS
DID NOT CHANGE THE DATA.

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;*MAINDEC-11-DZDMC-B BASIC DMC11 CONTROLLER TEST
;*COPYRIGHT 1976, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754
*-----

: STARTING PROCEDURE
: LOAD PROGRAM
: LOAD ADDRESS 000200
: SWR=0 AUTOSIZE DMC11
: SW07=1 USE CURRENT DMC11 PARAMETERS
: SW00=1 INPUT NEW DMC11 PARAMETERS
: PRESS START
: PROGRAM WILL TYPE "MAINDEC-11-DZDMC-B BASIC DMC11 CONTROLLER TEST"
: PROGRAM WILL TYPE STATUS MAP
: PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
: AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE
: AND THEN RESUME TESTING
: SUBSEQUENT RESTARTS WILL NOT TYPE PROGRAM TITLE

: SWITCH REGISTER OPTIONS
:-----

100000
040000
020000
010000
004000
002000
001000
000400
000200
000100
000040
000020
000010
000004
000002
000001

SW15=100000 :=1, HALT ON ERROR
SW14=40000 :=1, LOOP ON CURRENT TEST
SW13=20000 :=1, INHIBIT ERROR TYPEOUT
SW12=10000 :=1, DELETE TYPEOUT/BELL ON ERROR.
SW11=4000 :=1, INHIBIT ITERATIONS
SW10=2000 :=1, ESCAPE TO NEXT TEST ON ERROR
SW09=1000 :=1, LOOP WITH CURRENT DATA
SW08=400 :=1, LOOP ON ERROR
SW07=200 :=1, USE CURRENT DMC11 PARAMETERS, =0, AUTOSIZE DMC11
SW06=100 :=1, HALT BEFORE CLOCKING MICRO-PROCESSOR INSTRUCTION

SW05=40
SW04=20
SW03=10 := RESELECT DMC11'S TO BE TESTED (ACTIVE)
SW02=4 := LOCK ON TEST SELECT
SW01=2 := RESTART PROGRAM AT SELECTED TEST
SW00=1 := INPUT DMC11 PARAMETERS

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:REGISTER DEFINITIONS

000000	R0=%0	:GENERAL REGISTER
000001	R1=%1	:GENERAL REGISTER
000002	R2=%2	:GENERAL REGISTER
000003	R3=%3	:GENERAL REGISTER
000004	R4=%4	:GENERAL REGISTER
000005	R5=%5	:GENERAL REGISTER
000006	SP=%6	:PROCESSOR STACK POINTER
000007	PC=%7	:PROGRAM COUNTER

:LOCATION EQUIVALENCIES

177776	PS=177776	:PROCESSOR STATUS WORD
001200	STACK=1200	:START OF PROCESSOR STACK

:INSTRUCTION DEFINITIONS

005746	PUSH1SP=5746	:DECREMENT PROCESSOR STACK 1 WORD
005726	POP1SP=5726	:INCREMENT PROCESSOR STACK 1 WORD
010046	PUSHR0=10046	:SAVE R0 ON STACK
012600	POPPO=12600	:RESTORE R0 FROM STACK
024646	PUSH2SP=24646	:DECREMENT STACK TWICE
022626	POP2SP=22626	:INCREMENT STACK TWICE
	.EQUIV EMT,HLT	:BASIC DEFINITION OF ERROR CALL

:BIT DEFINITIONS

100000	BIT15=100000
040000	BIT14=40000
020000	BIT13=20000
010000	BIT12=10000
004000	BIT11=4000
002000	BIT10=2000
001000	BIT9=1000
000400	BIT8=400
000200	BIT7=200
000100	BIT6=100
000040	BIT5=40
000020	BIT4=20
000010	BIT3=10
000004	BIT2=4
000002	BIT1=2
000001	BIT0=1

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DZDMC.P11 23-MAY-77 11:16

TRAPCATCHER FOR UNEXPECTED INTERRUPTS

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000024 005336
000026 000340
000030 004750
000032 000340
000034 004716
000036 000340

000040 000000
000042 000000
000044 000000
000046 003522
000052 040000

000174 000000
000176 000000

000200 000137 002002

001000 005377 040515 047111
001025 102 051501 041511

001200 177570
001202 177570

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*****
-----
; TRAPCATCHER FOR ILLEGAL INTERRUPTS
; THE STANDARD "TRAP CATCHER" IS PLACED
; BETWEEN ADDRESS 0 TO ADDRESS 776.
; IT LOOKS LIKE "PC+2 HALT".
-----
*****

.=0
; STANDARD INTERRUPT VECTORS
-----

.=24
.PFAIL          ; POWER FAIL HANDLER
340             ; SERVICE AT LEVEL 7
.HLT            ; ERROR HANDLER
340             ; SERVICE AT LEVEL 7
.TRPSRV        ; GENERAL HANDLER DISPATCH SERVICE
340             ; SERVICE AT LEVEL 7

.=40
0              ; SAVE FOR ACT-11 OR XXDP
0              ; RETURN ADDRESS IF UNDER ACT-11 OR XXDP
0              ; SAVE FOR ACT-11 OR XXDP
$ENDAD        ; FOR USE WITH ACT-11 OR XXDP

.=52
BIT14         ; ACT-11 PROGRAM CHARACTERISTICS
              ; BIT14=1 PROGRAM EXECUTION TIME
              ; IS MEMORY SIZE DEPENDENT

.=174
DISPREG: 0    ; SOFTWARE DISPLAY REGISTER
SWREG: 0     ; SOFTWARE SWITCH REGISTER

.=200
JMP .START   ; GO TO START OF PROGRAM

.=1000
MTITLE: .ASCII <377><12>/MAINDEC-11-DZDMC-B <377>
        .ASCII /BASIC DMC11 CONTROLLER TEST/<377>

.=1200
; INDIRECT POINTERS TO SWITCH REGISTER AND LIGHT DISPLAY
-----

DISPLAY: 177570
SWP: 177570
```

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150 001204 177560
151 001206 177562
152 001210 177564
153 001212 177566
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158 001214 000000
159 001216 000000
160 001220 000000
161 001222 000003
162 001224 000000
163 001226 000000
164 001230 000000
165 001232 000000
166 001234 000000
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171 001236 000000
172 001240 000000
173 001242 000000
174 001244 000000
175 001246 000000
176 001250 000000
177 001252 000000
178 001254 000000
179 001256 000000
180 001260 000000
181 001262 000000
182 001264 000000
183 001266 000000
184 001270 000000
185 001272 000000
186 001274 000000
187 001276 000000
188 001300 000000
189 001302 000001
190 001304 000000
191 001306 000001
192 001310 000001
193 001312 000001
194 001314 000001
195 001316 000000
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197 001320 001472
198 001322 001676

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:INDIRECT POINTERS TO TELETYPE VECTORS AND REGISTERS
:-----
TKCSR: 177560      :TELETYPE KEYBOARD CONTROL REGISTER
TKDBR: 177562      :TELETYPE KEYBOARD DATA BUFFER
TPCSR: 177564      :TELEPRINTER CONTROL REGISTER
TPDBR: 177566      :TELEPRINTER DATA BUFFER

:PROGRAM CONTROL PARAMETERS
:-----
RETURN: 0          :SCOPE ADDRESS FOR LOOP ON TEST
NEXT: 0            :ADDRESS OF NEXT TEST TO BE EXECUTED
LOCK: 0           :ADDRESS FOR LOCK ON CURRENT DATA
ICOUNT: 3         :NUMBER OF ITERATIONS THAT CURRENT TEST WILL BE
LPCNT: 0          :NUMBER OF ITERATIONS COMPLETED
TSTNO: 0          :NUMBER OF TEST IN PROGRESS
PASCNT: 0         :NUMBER OF PASSES COMPLETED
ERRCNT: 0         :TOTAL NUMBER OF ERRORS
LSTERR: 0         :PC OF LAST ERROR CALL

:PROGRAM VARIABLES
:-----
STRTSW: 0         :SWITCHES AT START OF PROGRAM
STAT: 0          :DM STATUS WORD STORAGE
CLKX: 0
MASKX: 0
TEMP1: 0         :TEMPORARY STORAGE
TEMP2: 0         :TEMPORARY STORAGE
TEMP3: 0         :TEMPORARY STORAGE
TEMP4: 0         :TEMPORARY STORAGE
TEMP5: 0         :TEMPORARY STORAGE
SAVR0: 0         :R0 STORAGE
SAVR1: 0         :R1 STORAGE
SAVR2: 0         :R2 STORAGE
SAVR3: 0         :R3 STORAGE
SAVR4: 0         :R4 STORAGE
SAVR5: 0         :R5 STORAGE
SAVSP: 0         :STACK POINTER STORAGE
SAVPC: 0         :PROGRAM COUNTER STORAGE
ZERO: 0
ONE: 1
MEMLIM: 0       :HIGHEST LOCATION FOR NPR'S
DMACTV: .BLKW 1 :DMC11'S SELECTED ACTIVE.
DMNUM: .BLKW 1  :OCTAL NUMBER OF DMC11'S.
SAVACT: .BLKW 1 :ORIGINAL ACTV DEVICES
SAVNUM: .BLKW 1 :WORKABLE NUMBER
RUN: 0          :POINTER TO RUNNING DEVICE.
.EVEN
CREAM: DM.MAP-6 :TABLE POINTER.
MILK: CNT.MAP-4 :TABLE POINTER

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001330 104400
001330 003576
001332 104401
001332 003736
001334 104402
001334 003766
001336 104403
001336 004050
001340 104404
001340 004154
001342 104405
001342 004174
001344 104406
001344 004374
001346 104407
001346 004434
001350 104410
001350 004466
001352 104411
001352 004472
001354 104412
001354 005466
001356 104413
001356 005436
001360 104414
001360 005504
001362 104415
001362 005552
001364 104416
001364 005616

:PROGRAM CONTROL FLAGS
:-----

INIFLG: .BYTE 0 ;PROGRAM INITIALIZATION FLAG
ERRFLG: .BYTE 0 ;ERROR OCCURED FLAG
LOKFLG: .BYTE 0 ;LOCK ON CURRENT TEST FLAG
QV.FLG: .BYTE 0 ;QUICK VERIFY FLAG.
;ON FIRST PASS OF EACH DMC11 ITERATIONS WILL BE
.EVEN

:DEFINITIONS FOR TRAP SUBROUTINE CALLS
:POINTERS TO SUBROUTINES CAN BE FOUND
:IN THE TABLE IMMEDIATLY FOLLOWING THE DEFINITIONS

:*****

:-----
:TRPTAB:
SCOPE=TRAP+0 ;CALL TO SCOPE LOOP AND ITERATION HANDLER
.SCOPE
SCOPI=TRAP+1 ;CALL TO LOOP ON CURRENT DATA HANDLER
.SCOPI
TYPE=TRAP+2 ;CALL TO TELETYPE OUTPUT ROUTINE
.TYPE
INSTR=TRAP+3 ;CALL TO ASCII STRING INPUT ROUTINE
.INSTR
INSTER=TRAP+4 ;CALL TO INPUT ERROR HANDLER
.INSTER
PARAM=TRAP+5 ;CALL TO NUMERICAL DATA INPUT ROUTINE
.PARAM
SAVOS=TRAP+6 ;CALL TO REGISTER SAVE ROUTINE
.SAVOS
RESOS=TRAP+7 ;CALL TO REGISTER RESTORE ROUTINE
.RESOS
CONVRT=TRAP+10 ;CALL TO DATA OUTPUT ROUTINE
.CONVRT
CNVRT=TRAP+11 ;CALL TO DATA OUTPUT ROUTINE WITHOUT CR/LF.
.CNVRT
MSTCLR=TRAP+12 ;CALL TO ISUE A MASTER CLEAR
.MSTCLR
DELAY=TRAP+13 ;CALL TO DELAY
.DELAY
ROMCLK=TRAP+14 ;CALL TO CLOCK ROM ONCE
.ROMCLK
DATACLK=TRAP+15 ;CALL TO CLK DATA
.DATACLK
TIMER=TRAP+16 ;CALL TO DELAY A CLOCK TICK
.TIMER
:-----

:*****

PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

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250          :DMC11 CONTROL INDICATORS FOR CURRENT DMC11 UNDER TEST
          :-----
251          STAT1: 0
252          STAT2: 0
253          STAT3: 0
254          001366 000000
255          001370 000000
256          001372 000000
257
258          :DMC11 VECTOR AND REGISTER INDIRECT POINTERS
          :-----
259          DMRVEC: 0          : POINTER TO DMC11 RECEIVER INTERRUPT VECTOR
260          DMRLVL: 0         : POINTER TO DMC11 RECEIVER INTERRUPT SERVICE PS
261          DMTVEC: 0         : POINTER TO DMC11 TRANSMITTER INTERRUPT VECTOR
262          DMTLVL: 0         : POINTER TO DMC11 TRANSMITTER INTERRUPT SERVICE PS
263          DMCSR: 0          : POINTER TO DMC11 CONTROL STATUS REGISTER
264          DMCSRH: 0         : POINTER TO DMC11 CONTROL STATUS REGISTER HIGH BYTE.
265          DMCTL: 0          : POINTER TO DMC11 CONTROL OUT REGISTER
266          DMFO4: 0          : POINTER TO DMC11 PORT REGISTER (SEL 4)
267          DMFO6: 0          : POINTER TO DMC11 PORT REGISTER (SEL 6)
268          001374 000000
269          001376 000000
270          001400 000000
271          001402 000000
272          001404 000000
273          001406 000000
274          001410 000000
275          001412 000000
276          001414 000000
277
278          :TEMP STORAGE
          :-----
279          TEMP: 0
280          . = +40
281          001416 000000
282          0014E0
283
284          :DMC11 STATUS TABLE AND ADDRESS ASSIGNMENTS
          :-----
285          . = 1500
286          DM.MAP:
287          DMCRO0: .BLKW 1          : CONTROL STATUS REGISTER FOR DMC11 NUMBER 00
288          DMS100: .BLKW 1          : VECTOR FOR DMC11 NUMBER 00
289          DMS200: .BLKW 1          : DDCMP LINE# FOR DMC11 NUMBER 00
290          DMS300: .BLKW 1          : 3RD STATUS WORD
291
292          DMCRO1: .BLKW 1          : CONTROL STATUS REGISTER FOR DMC11 NUMBER 01
293          DMS101: .BLKW 1          : VECTOR FOR DMC11 NUMBER 01
294          DMS201: .BLKW 1          : DDCMP LINE# FOR DMC11 NUMBER 01
295          DMS301: .BLKW 1          : 3RD STATUS WORD
296
297          DMCRO2: .BLKW 1          : CONTROL STATUS REGISTER FOR DMC11 NUMBER 02
298          DMS102: .BLKW 1          : VECTOR FOR DMC11 NUMBER 02
299          DMS202: .BLKW 1          : DDCMP LINE# FOR DMC11 NUMBER 02
300          DMS302: .BLKW 1          : 3RD STATUS WORD
301
302          DMCRO3: .BLKW 1          : CONTROL STATUS REGISTER FOR DMC11 NUMBER 03
303          DMS103: .BLKW 1          : VECTOR FOR DMC11 NUMBER 03
304          DMS203: .BLKW 1          : DDCMP LINE# FOR DMC11 NUMBER 03
305          DMS303: .BLKW 1          : 3RD STATUS WORD
306
307          DMCRO4: .BLKW 1          : CONTROL STATUS REGISTER FOR DMC11 NUMBER 04
308          DMS104: .BLKW 1          : VECTOR FOR DMC11 NUMBER 04
309          DMS204: .BLKW 1          : DDCMP LINE# FOR DMC11 NUMBER 04
310          DMS304: .BLKW 1          : 3RD STATUS WORD
311
312          001500 001500
313          001500 000001
314          001502 000001
315          001504 000001
316          001506 000001
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318          001510 000001
319          001512 000001
320          001514 000001
321          001516 000001
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323          001520 000001
324          001522 000001
325          001524 000001
326          001526 000001
327
328          001530 000001
329          001532 000001
330          001534 000001
331          001536 000001
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333          001540 000001
334          001542 000001
335          001544 000001
336          001546 000001

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PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

306	001550	000001	DMCR05: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 05
307	001552	000001	DMS105: .BLKW	1	:VECTOR FOR DMC11 NUMBER 05
308	001554	000001	DMS205: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 05
309	001556	000001	DMS305: .BLKW	1	:3RD STATUS WORD
310					
311	001560	000001	DMCR06: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 06
312	001562	000001	DMS106: .BLKW	1	:VECTOR FOR DMC11 NUMBER 06
313	001564	000001	DMS206: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 06
314	001566	000001	DMS306: .BLKW	1	:3RD STATUS WORD
315					
316	001570	000001	DMCR07: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 07
317	001572	000001	DMS107: .BLKW	1	:VECTOR FOR DMC11 NUMBER 07
318	001574	000001	DMS207: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 07
319	001576	000001	DMS307: .BLKW	1	:3RD STATUS WORD
320					
321	001600	000001	DMCR10: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 10
322	001602	000001	DMS110: .BLKW	1	:VECTOR FOR DMC11 NUMBER 10
323	001604	000001	DMS210: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 10
324	001606	000001	DMS310: .BLKW	1	:3RD STATUS WORD
325					
326	001610	000001	DMCR11: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 11
327	001612	000001	DMS111: .BLKW	1	:VECTOR FOR DMC11 NUMBER 11
328	001614	000001	DMS211: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 11
329	001616	000001	DMS311: .BLKW	1	:3RD STATUS WORD
330					
331	001620	000001	DMCR12: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 12
332	001622	000001	DMS112: .BLKW	1	:VECTOR FOR DMC11 NUMBER 12
333	001624	000001	DMS212: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 12
334	001626	000001	DMS312: .BLKW	1	:3RD STATUS WORD
335					
336	001630	000001	DMCR13: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 13
337	001632	000001	DMS113: .BLKW	1	:VECTOR FOR DMC11 NUMBER 13
338	001634	000001	DMS213: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 13
339	001636	000001	DMS313: .BLKW	1	:3RD STATUS WORD
340					
341	001640	000001	DMCR14: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 14
342	001642	000001	DMS114: .BLKW	1	:VECTOR FOR DMC11 NUMBER 14
343	001644	000001	DMS214: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 14
344	001646	000001	DMS314: .BLKW	1	:3RD STATUS WORD
345					
346	001650	000001	DMCR15: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 15
347	001652	000001	DMS115: .BLKW	1	:VECTOR FOR DMC11 NUMBER 15
348	001654	000001	DMS215: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 15
349	001656	000001	DMS315: .BLKW	1	:3RD STATUS WORD
350					
351	001660	000001	DMCR16: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 16
352	001662	000001	DMS116: .BLKW	1	:VECTOR FOR DMC11 NUMBER 16
353	001664	000001	DMS216: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 16
354	001666	000001	DMS316: .BLKW	1	:3RD STATUS WORD
355					
356	001670	000001	DMCR17: .BLKW	1	:CONTROL STATUS REGISTER FOR DMC11 NUMBER 17
357	001672	000001	DMS117: .BLKW	1	:VECTOR FOR DMC11 NUMBER 17
358	001674	000001	DMS217: .BLKW	1	:DDCMP LINE# FOR DMC11 NUMBER 17
359	001676	000001	DMS317: .BLKW	1	:3RD STATUS WORD
360					
361	001700	000000	DM.END: 000000		

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001702
001702 000000
001704 000000

001706 000000
001710 000000

001712 000000
001714 000000

001716 000000
001720 000000

001722 000000
001724 000000

001726 000000
001730 000000

001732 000000
001734 000000

001736 000000
001740 000000

001742 000000
001744 000000

001746 000000
001750 000000

001752 000000
001754 000000

001756 000000
001760 000000

001762 000000
001764 000000

001766 000000
001770 000000

001772 000000
001774 000000

001776 000000
002000 000000

:DMC11 PASS COUNT AND ERROR COUNT TABLE
:-----

CNT.MAP:
PACT00: 0 :PASS COUNT FOR DMC11 NUMBER 00
ERCT00: 0 :ERROR COUNT FOR DMC11 NUMBER 00

PACT01: 0 :PASS COUNT FOR DMC11 NUMBER 01
ERCT01: 0 :ERROR COUNT FOR DMC11 NUMBER 01

PACT02: 0 :PASS COUNT FOR DMC11 NUMBER 02
ERCT02: 0 :ERROR COUNT FOR DMC11 NUMBER 02

PACT03: 0 :PASS COUNT FOR DMC11 NUMBER 03
ERCT03: 0 :ERROR COUNT FOR DMC11 NUMBER 03

PACT04: 0 :PASS COUNT FOR DMC11 NUMBER 04
ERCT04: 0 :ERROR COUNT FOR DMC11 NUMBER 04

PACT05: 0 :PASS COUNT FOR DMC11 NUMBER 05
ERCT05: 0 :ERROR COUNT FOR DMC11 NUMBER 05

PACT06: 0 :PASS COUNT FOR DMC11 NUMBER 06
ERCT06: 0 :ERROR COUNT FOR DMC11 NUMBER 06

PACT07: 0 :PASS COUNT FOR DMC11 NUMBER 07
ERCT07: 0 :ERROR COUNT FOR DMC11 NUMBER 07

PACT10: 0 :PASS COUNT FOR DMC11 NUMBER 10
ERCT10: 0 :ERROR COUNT FOR DMC11 NUMBER 10

PACT11: 0 :PASS COUNT FOR DMC11 NUMBER 11
ERCT11: 0 :ERROR COUNT FOR DMC11 NUMBER 11

PACT12: 0 :PASS COUNT FOR DMC11 NUMBER 12
ERCT12: 0 :ERROR COUNT FOR DMC11 NUMBER 12

PACT13: 0 :PASS COUNT FOR DMC11 NUMBER 13
ERCT13: 0 :ERROR COUNT FOR DMC11 NUMBER 13

PACT14: 0 :PASS COUNT FOR DMC11 NUMBER 14
ERCT14: 0 :ERROR COUNT FOR DMC11 NUMBER 14

PACT15: 0 :PASS COUNT FOR DMC11 NUMBER 15
ERCT15: 0 :ERROR COUNT FOR DMC11 NUMBER 15

PACT16: 0 :PASS COUNT FOR DMC11 NUMBER 16
ERCT16: 0 :ERROR COUNT FOR DMC11 NUMBER 16

PACT17: 0 :PASS COUNT FOR DMC11 NUMBER 17
ERCT17: 0 :ERROR COUNT FOR DMC11 NUMBER 17

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FORMAT OF STATUS TABLE

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00															
I	C	I	O	I	N	I	T	I	R	O	L	I	R	E	I	G	I	S	T	E	R	I								
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	CSR							
I	*	I	*	I	*	I	*	I	*	I	*	I	*	I	*	I	V	I	E	I	C	I	T	O	I	R	I	*	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	STAT1
I	*	I	B	I	M	I	I	A	I	D	I	D	*	I	*	I	L	I	I	N	I	E	I	I	*	I	*	I		
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	STAT2
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	STAT3

DEFINITION OF FORMAT

- CSR: CONTAINS DMC11 CSR ADDRESS
- STAT1: BITS 00-08 IS DMC11 VECTOR ADDRESS
 BIT15=1 MICRO-PROCESSOR HAS CROM
 BIT15=0 MICRO-PROCESSOR HAS CROM
 BIT14=1 ??? TURNAROUND CONNECTOR IS ON
 BIT14=0 NO TURNAROUND CONNECTOR
 BIT13=0 LINE UNIT IS AN M8201
 BIT13=1 LINE UNIT IS AN M8202
 BIT12=1 NO LINE UNIT
 BITS 09-11 IS DMC11 BR PRIORITY LEVEL
- STAT2: LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)
 HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)
- STAT3: BIT0=1 DO FREE RUNNING TESTS ON KMC
 (MUST BE SET TO A ONE MANUALLY (PROGRAM DZDMI ONLY))
 KMC MUST HAVE MICRO-CODE WRITTEN FROM RUNNING
 DZDMG TEST 2 FIRST
 BIT1=1 DMC11-AL LOCAL HIGH SPEED MICRO-CODE
 BIT1=0 DMC11-AP REMOTE LOW SPEED MICRO-CODE


```

470                                     :PROGRAM INITIALIZATION
471                                     :LOCK OUT INTERRUPTS
472                                     :SET UP PROCFSSOR STACK
473                                     :SET UP POWER FAIL VECTOR
474                                     :CLEAR PROGRAM CONTROL FLAGS AND COUNTS
475                                     :TYPE TITLE MESSAGE
476
477
478 002002 012737 000340 177776      .START: MOV      #340,PS      :LOCK OUT INTERRUPTS
479 002010 012706 001200              MOV      #STACK,SP      :SET UP STACK
480 002014 012737 005336 000024      MOV      #.PFAIL,2#24   :SET UP POWER FAIL VECTOR
481 002022 013737 001310 001314      MOV      QMNUM,SAVNUM   :SAVE NUMBER OF DEVICES IN SYSTEM.
482 002030 005037 010016              CLR      SWFLG          :CLEAR SOFT TIMEOUT FLAG
483 002034 105037 001325              CLR      ERRFLG        :CLEAR ERROR FLAG
484 002040 105037 001327              CLR      QV.FLG        :ZERO QUICK VERIFY FLAG
485 002044 012737 001470 001320      MOV      #DM.MAP-10,CREAM:GET MAP POINTER.
486 002052 012737 001676 001322      MOV      #CNT.MAP-4,MILK:GET PASS COUNT MAP POINTER
487 002060 012737 100000 001316      MOV      #BIT15,RUN     :POINT POINTER TO FIRST DEVICE.
488 002066 012700 001702              MOV      #CNT.MAP,RO    :PASS COUNT POINTER TO RC
489 002072 005020                    23$: CLR      (RO)+         :CLEAR TABLE
490 002074 022700 002002              CMP      #CNT.MAP+100,RO:DONE YET?
491 002100 001374                    BNE     23$            :KEEP GOING
492 002102 005037 001234              CLR      LSTERR        :CLEAR LAST ERROR POINTER
493 002106 012737 000001 001226      MOV      #1,TSTNO      :SET UP FOR TEST 1
494 002114 012737 002002 001214      MOV      #.START,RETURN:SET UP FOR POWER FAIL BEFORE
495                                     :TESTING STARTS
496 002122 013746 000006              MOV      2#6,-(SP)     :SAVE CURRENT VECTORS
497 002126 013746 000004              MOV      2#4,-(SP)
498 002132 012737 002166 000004      MOV      #6$,2#4       :SET UP FOR TIMEOUT
499 002140 012737 177570 001202      MOV      #177570,SWR   :SET SWR TO HARD SWR ADDRESS
500 002146 012737 177570 001200      MOV      #177570,DISPLAY:SET DISPLAY TO HARD SWR ADDRESS
501 002154 022777 177777 177020      CMP      #-1,2$SWR     :REFERENCE HARDWARE SWITCH REGISTER
502 002162 001402                    BEQ     6$+2          :IF = -1 USE SOFT SWR ANYWAY
503 002164 000407                    BR      7$           :IF IT EXISTS AND NOT = -1 USE HARD SWR
504 002166 022626                    6$: CMP      (SP)+,(SP)+  :ADJUST STACK
505 002170 012737 000176 001202      MOV      #SWREG,SWR    :POINTER TO SOFT SWR
506 002176 012737 000174 001200      MOV      #DISPREG,DISPLAY:POINTER TO SOFT DISPLAY REG
507 002204 012637 000004                    7$: MOV      (SP)+,2#4    :RESTORE VECTORS
508 002210 012637 000006              MOV      (SP)+,2#6
509 002214 105737 001324              TSTB    INIFLG        :HAS INITIALIZATION BEEN PERFORMED
510 002220 001006                    BNE     20$          :BR IF YES
511 002222 022737 003522 000042      CMP      #SENDAD,2#42  :IF ACT-11 AUTOMATIC MODE, DON'T TYPE ID
512 002230 001402                    BEQ     20$
513 002232 104402 001000                    TYPE    #MTITLE       :TYPE TITLE MESSAGE
514 002236 004737 007606                    JSR    #PC,CKSWR     :CHECK FOR SOFT SWR
515 002242 017737 176734 001236      MOV      2$SWR,STRTSW  :STORE STARTING SWITCHES
516 002250 005737 000042              TST     2#42          :IS IT RUNNING IN AUTO MODE?
517 002254 001402                    BEQ     .+6          :BR IF NO
518 002256 005037 001236              CLR     STRTSW        :IF YES, CLEAR SWITCHES
519 002262 032737 000001 001236      BIT     #SW00,STRTSW   :IF SW00=1, QUESTIONS ARE ASKED.
520 002270 001012                    BNE     17$          :BR IF SW00=1
521 002272 105737 001236              TSTB    STRTSW        :BIT7=1??
522 002276 100007                    BPL     17$          :BR IF SW07=0
523 002300 005737 001306              TST     DMACTV        :ARE ANY DEVICES SELECTED?
524 002304 001006                    BNE     16$          :BR IF YES
525 002306 104402 007154              TYPE    #NOACT       :NO DEVICES SELECTED.

```

LOC

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526 002312 000000          HALT          ;STOP THE SHOW
527 002314 000776          BR          ;DISQUALIFY CONTINUE SWITCH
528 002316 004737 010512 17$: JSR      PC,AUTO.SIZE ;GO DO THE AUTO SIZE
529 002322 105737 001324 16$: TSTB   INIFLG    ;FIRST TIME?
530 002326 001410          BEQ      21$      ;BR IF YES
531 002330 105737 001236  TSTB   STRTSW    ;IF USING SAME PARAMETERS DONT TYPE MAP
532 002334 100431          BMI      1$
533 002336 032737 000006 001236 BIT     #BIT1!BIT2,STRTSW ;IS TEST NO. OR LOCK SELECTED
534 002344 001403          BEQ      24$      ;IF NO THEN TYPE STATUS
535 002346 000424          BR          ;IF YES DO NOT TYPE STATUS
536 002350 005137 001324 21$: COM    INIFLG    ;SET FLAG
537 002354 104402 006224 24$: TYPE   ,XHEAD    ;TYPE HEADER
538 002360 012704 001500  MOV     #DM.MAP,R4    ;SET POINTER
539 002364 010437 001246 5$:  MOV     R4,TEMP1    ;SET ADDRESS
540 002370 012437 001250  MOV     (R4)+,TEMP2   ;SET CSR
541 002374 001411          BEQ      1$
542 002376 012437 001252  MOV     (R4)+,TEMP3   ;SET STAT1
543 002402 012437 001254  MOV     (R4)+,TEMP4   ;SET STAT2
544 002406 012437 001256  MOV     (R4)+,TEMP5   ;SET STAT3
545 002412 104410          CONVRT   ;TYPE OUT STATUS MAP
546 002414 007454          XSTATO
547 002416 000762          BR          ;
548 002420 012700 001500 1$:  MOV     #DM.MAP,R0    ;R0 POINTS TO STATUS TABLE

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549
550 ;*****
551 ;*AUTO SIZE TEST
552 ;*THIS TEST VERIFYS THAT THE DMC11S AND/OR KMC11S ARE AT THE CORRECT FLOATING
553 ;*ADDRESSES FOR YOUR SYSTEM. IF THIS TEST FAILS, IT IS NOT A HARDWARE ERROR.
554 ;*CHECK THE ADDRESSES OF ALL FLOATING DEVICES (DJ,DM,DO,DU,DUP,LK,DMC,DZ,KMC.
555 ;*IF THERE ARE NO OTHER FLOATING DEVICES BEFORE THE DMC11, THE FIRST
556 ;*DMC11 ADDRESS IS 760070, KMC11 IS 760110. NO DEVICE SHOULD EVER BE AT
557 ;*ADDRESS 760000. THIS TEST MAY REQUIRE 2 OR MORE ATTEMPTS TO GET THE
558 ;*RIGHT ADDRESSES. AFTER YOU HAVE CHANGED THE ADDRESS TO WHAT IT TOLD
559 ;*YOU THE FIRST TIME, IT MAY COME BACK AND TELL YOU A DIFFERENT ADDRESS
560 ;*THE NEXT TIME YOU RUN IT. PLEASE HAVE PATIENCE, THE FINAL ADDRESS
561 ;*WILL BE CORRECT (AS LONG AS ALL DEVICES IN FRONT OF THE DMC'S ARE
562 ;*CORRECT).
563 ;*****

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564
565 002424 013746 000004          MOV     @#4,-(SP)    ;SAVE LOC 4
566 002430 013746 000006          MOV     @#6,-(SP)    ;SAVE LOC 6
567 002434 005037 000006          CLR     @#6          ;CLEAR VEC+2
568 002440 005037 001252          CLR     TEMP3       ;CLEAR FLAG
569 002444 005005          CLR     R5          ;R5=0=DMC, R5=-1=KMC
570 002446 011037 001404  AUSTRT: MOV    (R0),DMCSR    ;GET NEXT DMC CSR
571 002452 001564          BEQ     AUDONE      ;BR IF DONE
572 002454 005705          TST    R5          ;DMC OR KMC?
573 002456 001005          BNE    1$          ;BR IF KMC
574 002460 032760 100000 000002 BIT     #BIT15,2(R0) ;CHECK FOR DMC CSR
575 002466 001061          BNE    SKIP        ;SKIP IF NOT DMC
576 002470 000404          BR     2$          ;ITS A DMC SO CONTINUE
577 002472 032760 100000 000002 1$: BIT     #BIT15,2(R0) ;CHECK FOR KMC CSR
578 002500 001454          BEQ     SKIP        ;SKIP IF NOT KMC
579 002502 012737 002674 000004 2$: MOV     #NODEV,@#4  ;SET UP FOR TIMEOUT
580 002510 005705          TST    R5          ;DMC OR KMC?
581 002512 001003          BNE    3$          ;BR IF KMC

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582	002514	012703	000006		MOV	#6,R3	;R3 IS COUNT OF DEVICES BEFORE DMC
583	002520	000402			BR	4\$;GO ON
584	002522	012703	000010	3\$:	MOV	#10,R3	;R3 IS COUNT OF DEVICES BEFORE KMC
585	002526	012702	003010	4\$:	MOV	#DEVTAB,R2	;R2 IS DEVICE TABLE POINTER
586	002532	012701	160010		MOV	#160010,R1	;START WITH ADDRESS 160010
587	002536	005711		FLOAT:	TST	(R1)	;CHECK ADDRESS IN R1
588	002540	111204			MOV	(R2),R4	;IF NO TIMEOUT, GET NEXT ADDRESS
589	002542	060401			ADD	R4,R1	;IN R1
590	002544	005201			INC	R1	
591	002546	040401			BIC	R4,R1	
592	002550	005703			TST	R3	;ANY MORE DEVICES TO CHECK FOR?
593	002552	001371			BNE	FLOAT	;BR IF YES
594	002554	012737	002700	000004	MOV	#ERR,2#4	;OK ONLY DMC'S ARE LEFT, SET UP FOR TIMEOUT
595	002562	010137	003022		MOV	R1,XLOC	;SAVE FIRST DMC/KMC ADDRESS
596	002566	005705		FY:	TST	R5	;DMC OR KMC?
597	002570	001005			BNE	1\$;BR IF KMC
598	002572	032760	100000	000002	BIT	#BIT15,2(R0)	;CHECK FOR DMC CSR
599	002600	001014			BNE	SKIP	;SKIP IF NOT DMC
600	002602	000404			BR	2\$;ITS A DMC SO CONTINUE
601	002604	032760	100000	000002	1\$:	BIT	#BIT15,2(R0)
602	002612	001407			BEQ	SKIP	;CHECK FOR KMC CSR
603	002614	005711			2\$:	TST	(R1)
604	002616	020137	001404		CMP	R1,DMCSR	;CHECK DMC ADDRESS
605	002622	001411			BEQ	OK	;DOES IT MATCH
606	002624	062701	000010		ADD	#10,R1	;BR IF YES
607	002630	000756			BR	FY	;GET NEXT DMC ADDRESS
608	002632	062700	000010		SKIP:	ADD	#10,R0
609	002636	011037	001404		MOV	(R0),DMCSR	;DO IT AGAIN
610	002642	001470			BEQ	AUDONE	;SKIP TO NEXT CSR IN TABLE
611	002644	000750			BR	FY	;GET NEXT CSR
612	002646	062700	000010		OK:	ADD	#10,R0
613	002652	062737	000010	003022	ADD	#10,XLOC	;BR IF DONE
614	002660	011037	001404		MOV	(R0),DMCSR	;ELSE CONTINUE
615	002664	001457			BEQ	AUDONE	;SKIP TO NEXT DMC CSR
616	002666	013701	003022		MOV	XLOC,R1	;UPDATE EXPECTED DMC/KMC ADDRESS
617	002672	000735			BR	FY	;GET NEXT DMC/KMC CSR
618	002674	122243			NODEV:	CMPB	(R2)+,-(R3)
619	002676	000002			RTI		;BR IF DONE
620	002700	005737	001252		ERR:	TST	TEMP3
621	002704	001014			BNE	1\$;ON TIMEOUT, INC R2, DEC R3
622	002706	104402			TYPE		;RETURN
623	002710	007223			CONERR		;CHECK FLAG IF = 0 TYPE HEADER
624	002712	012737	002700	001276	MOV	#ERR,SAVPC	;SKIP HEADER
625	002720	104411			CONVRT		;TYPEOUT HEADER MESSAGE
626	002722	002770			ERRPC		;CONFIGURATION ERROR!!!!
627	002724	104402			TYPE		;SAVE PC FOR TYPEOUT
628	002726	007277			CNERR		;TYPE OUT ERROR PC
629	002730	012737	177777	001252	1\$:	MOV	#-1,TEMP3
630	002736	010137	001262		MOV	R1,SAVR1	;TYPE REST OF HEADER
631	002742	104410			CONVRT		;SET FLAG SO IT ONLY GETS TYPED ONCE
632	002744	002776			CONTAB		;SAVE R1 FOR TYPEOUT
633	002746	005705			TST	R5	;TYPE CSR VALUES
634	002750	001003			BNE	3\$;DMC OR KMC ?
635	002752	104402			TYPE		;BR IF KMC
636	002754	007320			DMCM		
637	002756	000402			BR	4\$;CONTINUE

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 DZDMC.P11 23-MAY-77 11:16 PROGRAM INITIALIZATION AND START UP.

638	002760	104402		3\$:	TYPE			
639	002762	007330			KMCM			
640	002764	022626		4\$:	CMP	(SP)+, (SP)+		:ADJUST STACK
641	002766	000727			BR	OK		:BR TO GET OUT
642	002770	00000!		ERRPC:	1			
643	002772	006	002		.BYTE	6,2		
644	002774	001276			SAVPC			
645	002776	000002		CONTAB:	2			
646	003000	006	004		.BYTE	6,4		
647	003002	003022			XLOC			
648	003004	006	002		.BYTE	6,2		
649	003006	001404			DMCSR			
650	003010	007		DEVTAB:	.BYTE	7		:DJ
651	003011	017			.BYTE	17		:DH
652	003012	007			.BYTE	7		:DQ
653	003013	007			.BYTE	7		:DU
654	003014	007			.BYTE	7		:DUP
655	003015	007			.BYTE	7		:LK
656	003016	007			.BYTE	7		:DMC
657	003017	007			.BYTE	7		:DZ
658	003020	007			.BYTE	7		:KMC
659		003022		.EVEN				
660	003022	000000		YLOC:	0			
661	003024	005705		AUDONE:	TST	R5		:DMC?
662	003026	001005			BNE	1\$:BR IF KMC AND ALL DONE
663	003030	012705	177777		MOV	#-1, R5		:SET R5 TO -1 (KMC)
664	003034	012700	001500		MOV	#DM.MAP, RO		:RESET RO TO START OF TABLE
665	003040	000602			BR	AUSTR		:GO DO KMC'S
666	003042	012637	000006	1\$:	MOV	(SP)+, @#6		:RESTORE LOC 6
667	003046	012637	000004		MOV	(SP)+, @#4		:RESTORE LOC 4
668	003052	032737	000010	001236	BIT	#SW03, STRTSW		:SELECT SPECIFIC DEVICES??
669	003060	001422			BEQ	3\$:BR IF NO.
670	003062	104402	006144		TYPE	MNEW		:TYPE THE MESSAGE.
671	003066	005000			CLR	RO		:ZERO DATA LIGHTS
672	003070	000000			HALT			:WAIT FOR USER TO TELL WHAT DEVICES TO RUN
673	003072	027737	176104	001312	CMP	@SWR, SAVACT		:IS THE NUMBER VALID?
674	003100	101404			BLOS	2\$:BR IF NUMBER IS OK.
675	003102	104402	006005		TYPE	, MERR3		:TELL USER OF INVALID NUMBER.
676	003106	000000			HALT			:STOP EVERY THING.
677	003110	000776			BR	-2		:RESTART THE PROGRAM AGAIN.
678	003112	017737	176064	001306	2\$:	MOV	@SWR, DMACTV	:GET NEW DEVICE PATTERN
679	003120	013700	001306		MOV	DMACTV, RO		:SHOW THE USER WHAT HE SELECTED.
680	003124	000000			HALT			:CONTINUE DYNAMIC SWITCHES.
681	003126	012700	000300	3\$:	MOV	#300, RO		:PREPARE TO CLEAR THE FLOATING
682	003132	012701	000302		MOV	#302, R1		:VECTOR AREA. 300-776
683	003136	010120		4\$:	MOV	R1 (RO)+		:START PUTTING "PC+2 - HALT"
684	003140	005021			CLR	(R1)+		:IN VECTOR AREA.
685	003142	022021			CMP	(RO)+, (R1)+		:POP POINTERS
686	003144	022700	001000		CMP	#1000, RO		:ALL DONE??
687	003150	00.372			BNE	4\$:BR IF NO.
688								
689								
690								
691								
692	003152	012706	001200		.BEGIN:	MOV	#STACK, SP	:SET UP STACK
693	003156	013746	000006		MOV	@#6, -(SP)		:SAVE LOC 6

:TEST START AND RESTART
 :-----

694	003162	013746	000004		MOV	204, -(SP)	:SAVE LOC 4
695	003166	005000			CLR	RO	:START AT 0
696	003170	012737	003234	000004	MOV	225, 204	:SET UP FOR TIME OUT
697	003176	005037	000006		CLR	206	:TO AUTOSIZE MEMORY
698	003202	005720			65: TST	(RO)+	:CHECK ADDRESS IN RO
699	003204	022700	157776		CMP	157776, RO	:IS IT AT LEAST 28K
700	003210	001374			BNE	65	:BR IF NO
701	003212	162700	007776		SUB	7776, RO	:SAVE 2K FOR MONITORS
702	003216	010037	001304		75: MOV	RO, MEM LIM	:STORE MEMORY LIMIT
703	003222	012637	000004		MOV	(SP)+, 204	:RESTORE LOC 4
704	003226	012637	000006		MOV	(SP)+, 206	:RESTORE LOC 6
705	003232	000413			BR	105	:CONTINUE
706	003234	022626			25: CMP	(SP)+, (SP)+	:ADJUST STACK
707	003236	162700	000004		SUB	4, RO	:GET LAST GOOD ADDRESS
708	003242	162700	007776		SUB	7776, RO	:SAVE 2K FOR MONITORS
709	003246	022700	030000		CMP	30000, RO	:IS IT 8K?
710	003252	001361			BNE	75	:BR IF NO
711	003254	012700	037400		MOV	37400, RO	:IF 8K DON'T SAVE 2K
712	003260	000756			BR	75	:
713	003262	012737	000340	177776	105: MOV	340, PS	:LOCK OUT INTERRUPTS
714	003270	032737	000004	001236	BIT	BIT2, STRTSW	:CHECK FOR LOCK ON TEST
715	003276	001411			BEQ	15	:BR IF NO LOCK DESIRED.
716	003300	104402	006043		TYPE	MLOCK	:TYPE LOCK SELECTED.
717	003304	012737	000240	003612	MOV	NOP, TTST	:ADJUST SCOPE ROUTINE.
718	003312	012737	000240	003614	MOV	NOP, TTST+2	:SET UP TO LOCK
719	003320	000406			BR	35	:CONTINUE ALONG.
720	003322	013737	003730	003612	15: MOV	BRW, TTST	:PREPARE NORMAL SCOPE ROUTINE
721	003330	013737	003732	003614	MOV	BRX, TTST+2	:LOCK NOT SELECTED, SET UP FOR NORMAL SCOPE LOOP
722	003336	012737	010060	001214	35: MOV	CYCLE, RETURN	:START AT "CYCLE" FIND WHICH DE.ICE TO TEST
723	003344	032737	000002	001236	45: BIT	SW01, STRTSW	:IS TEST NO. SELECTED?
724	003352	001002			BNE	55	:BR IF YES
725	003354	104402	005755		TYPE	MR	:TYPE R
726	003360	000177	175630		55: JMP	RETURN	:START TESTING

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DZDMC.P11 23-MAY-77 11:16 END OF PASS ROUTINE

```

727 ;END OF PASS
728 ;TYPE NAME OF TEST
729 ;UPDATE PASS COUNT
730 ;CHECK FOR EXIT TO ACT-11
731 ;RESTART TEST
732
733 003364 000005 .EOP: RESET ;MAKE THE WORLD CLEAN AGAIN.
734 003366 005037 001234 CLR LSTERR ;CLEAR LAST ERROR PC
735 003372 105037 001325 CLRB ERRFLG ;CLEAR ERROR FLAG
736 003376 005237 001230 INC PASCNT ;UPDATE PASS COUNT
737 003402 013777 001230 175570 MOV PASCNT, @DISPLAY ;DISPLAY PASS COUNT
738 003410 104402 005733 TYPE ,MEPASS ;TYPE END PASS
739 003414 104402 006072 TYPE ,MCSRX ;TYPE CSR
740 003420 104411 003546 CNVRT ,XCSR ;SHOW IT
741 003424 104402 006100 TYPE ,MVECX ;TYPE VECTOR
742 003430 104411 003554 CNVRT ,XVEC ;SHOW IT
743 003434 104402 006106 TYPE ,MPASSX ;TYPE PASSES
744 003440 104411 003562 CNVRT ,XPASS ;SHOW IT
745 003444 104402 006117 TYPE ,MERRX ;TYPE ERRORS
746 003450 104411 003570 CNVRT ,XERR ;SHOW IT
747 003454 013700 001322 MOV MILK, RO ;GET POINTER TO PASS COUNT
748 003460 013720 001230 MOV PASCNT, (RO)+ ;STORE PASS COUNT FOR THIS DMC11
749 003464 013720 001232 MOV ERRCNT, (RO)+ ;STORE ERROR COUNT FOR THIS DMC11
750 003470 005337 001314 DEC SAVNUM ;ARE ALL DEVICES TESTED?
751 003474 001017 BNE RESTR ;BR IF NO.
752 003476 112737 000377 001327 MOVVB #377, QV.FLG ;SET THE QUICK VERIFY FLAG.
753 003504 013737 001310 001314 MOV DMNUM, SAVNUM ;RESTORE THE COUNT
754 003512 013701 000042 MOV #42, R1 ;CHECK FOR ACT-11 OR DDP
755 003516 001406 BEQ RESTR ;IF NOT, CONTINUE TESTING
756 003520 000005 RESTR ;STOP THE SHOW--CLEAR THE WORLD
757 003522 SENDAD:
758 003522 004711 JSR PC, (R1)
759 003524 000240 NOP
760 003526 000240 NOP
761 003530 000240 NOP
762 003532 000240 NOP
763 003534 012737 010060 001214 RESTR: MOV #CYCLE, RETURN
764 003542 000137 010060 JMP CYCLE
765 003546 000001 XCSR: 1
766 003550 006 002 .BYTE 6,2
767 003552 001404 DMCSR
768 003554 000001 XVEC: 1
769 003556 004 002 .BYTE 4,2
770 003560 001374 DMRVEC
771 003562 000001 XPASS: 1
772 003564 006 002 .BYTE 6,2
773 003566 001230 XERR: 1
774 003570 000001 .BYTE 6,2
775 003572 006 002 ERRCNT
776 003574 001232
777
778 ;SCOPE LOOP AND ITERATION HANDLER
779 -----
780
781 003576 004737 007606 .SCOPE: JSR PC, CKSWR ;CHECK FOR SOFT SWR
782 003602 010016 MOV RO, (SP) ;SAVE RO ON THE STACK

```

GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

```

783 003604 032777 040000 175370
784 003612 001407
785 003614 000437
786 003616 005737 003734
787 003622 001434
788 003624 005037 003734
789 003630 000415
790 003632 032777 004000 175342
791 003640 001011
792 003642 105737 001327
793 003646 001406
794 003650 005237 001224
795 003654 023737 001224 001222
796 003662 101414
797 003664 105037 001325
798 003670 005037 001224
799 003674 005037 001220
800 003700 012737 000020 001222
801 003706 013737 001216 001214
802 003714 011600
803 003716 022626
804 003720 013701 001404
805 003724 000177 175264
806 003730 001407
807 003732 000437
808 003734 000000
809
810
811
812
813 003736 004737 007606
814 003742 032777 001000 175232
815 003750 001405
816 003752 005737 001220
817 003756 001402
818 003760 013716 001220
819 003764 000002
820
821
822
823
824 003766 010546
825 003770 017605 000002
826 003774 062766 000002 000002
827 004002 005737 010016
828 004006 001004
829 004010 032777 010000 175164
830 004016 001012
831 004020 105715
832 004022 100002
833 004024 104402 005672
834 004030 105777 175154
835 004034 100375
836 004036 112577 175150
837 004042 001357
838 004044 012605

```

```

TTST: BIT #BIT14,ASWR ;"LOOP ON THIS TEST"?
      BEQ 1$ ;BR IF NO. (IF LOCK SW01=1; THIS LOC =240)
      BR 3$ ;GOTO 3$ (IF LOCK SW01=1; THIS LOC =240)
      TST DONE ;WAS TKCSR DONE SET?
      BEQ 3$ ;BR IF NO (LOCKED ON TEST)
      CLR DONE ;YES, CLEAR FLAG
      BR 2$ ;GO TO NEXT TEST
1$: BIT #SW11,ASWR ;DELETE ITERATION? (QUICK PASS)
      BNE 2$ ;BR IF YES
      TSTB QV.FLG ;HAVE PASSES BEECOMPLETED?
      BEQ 2$ ;BR IF QUICK PASS.
      INC LPCNT ;UPDATE ITERATION COUNTER
      CMP LPCNT,ICOUNT ;ARE ALL ITERATIONS DONE??
      BLOS 3$ ;BR IF NOT YET
2$: CLRB ERRFLG ;PREPARE FOR NEW TEST
      CLR LPCNT ;START ICOUNTER AT 0
      CLR LOCK
      MOV #20,ICOUNT ;RESET ITERATIONS
      MOV NEXT,RETURN ;GET NEXT TEST
3$: MOV (SP),RO ;POP RO OFF OF THE STACK
      POP2SP ;FAKE AN "RTI"
      MOV DMCSR,R1 ;R1 CONTAINS BASE DMC ADDRESS
      JMP @RETURN ;GO DO THE TEST
BRW: 1407
BRX: 437
DONE: 0

```

:CHECK FOR FREEZE ON CURRENT DATA

```

813 003736 004737 007606
814 003742 032777 001000 175232
815 003750 001405
816 003752 005737 001220
817 003756 001402
818 003760 013716 001220
819 003764 000002
820
821
822
823
824 003766 010546
825 003770 017605 000002
826 003774 062766 000002 000002
827 004002 005737 010016
828 004006 001004
829 004010 032777 010000 175164
830 004016 001012
831 004020 105715
832 004022 100002
833 004024 104402 005672
834 004030 105777 175154
835 004034 100375
836 004036 112577 175150
837 004042 001357
838 004044 012605

```

```

.SCOPI: JSR PC,CKSWR ;CHECK FOR SOFT SWR
        BIT #SW09,ASWR ;IS SW09=1(SET)?
        BEQ 1$ ;BR IF NOT SET.
        TST LOCK
        BEQ 1$
1$: MOV LOCK,(SP) ;GOTO THE ADDRESS IN LOCK.
      RTI ;GO BACK.

```

:TELETYPE OUTPUT ROUTINE

```

824 003766 010546
825 003770 017605 000002
826 003774 062766 000002 000002
827 004002 005737 010016
828 004006 001004
829 004010 032777 010000 175164
830 004016 001012
831 004020 105715
832 004022 100002
833 004024 104402 005672
834 004030 105777 175154
835 004034 100375
836 004036 112577 175150
837 004042 001357
838 004044 012605

```

```

.TYPE: MOV R5, -(SP) ;SAVE R5 ON THE STACK.
        MOV @2(SP),R5 ;GET ADDRESS OF MESSAGE.
        ADD #2,2(SP) ;POP OVER ADDRESS.
4$: TST SWFLG ;SOFT SWR MESSAGE?
      BNE 1$ ;IF YES TYPE IT OUT REGARDLESS OF SW12
      BIT #SW12,ASWR ;INHIBIT ALL PRINT OUT??
      BNE 3$ ;BR IF NO PRINT OUT WANTED (SW12=1)
1$: TSTB (R5) ;IS NUMBER MINUS? (MSB=1(BIT?))
      BPL 2$ ;BR IF NUMBER IS PLUS
      TYPE MCRLF ;TYPE A CR/LF!
2$: TSTB @TPCSR ;TTY READY?
      BPL 2$ ;BR IF NO.
      MOVB (R5)+,@TPDBR ;PRINT CURRENT CHAR.
      BNE 4$ ;IF NOT ZERO KEEP PRINTING!
3$: MOV (SP)+,R5 ;END OF OUTPUT. RESTORE R5

```



```

839 004046 000002          RTI          ;GO HOME
840                               ;-----
841                               .INSTR: MOV    R3,-(SP)      ;SAVE R3 ON STACK
842 004050 010346          MOV    R4,-(SP)      ;SAVE R4 ON STACK
843 004052 010446          MOV    #4(SP),MSG
844 004054 017637 000004 004072  ADD    #2,4(SP)
845 004062 062766 000002 000004  .INST1: TYPE
846 004070 104402          .MSG: 0
847 004072 000000          MOV    #INBUF,R4
848 004074 012704 007502          MOV    #7,R3
849 004100 012703 000007 1S:  TSTB  @TKCSR
850 004104 105777 175074          BPL   1S
851 004110 100375          MOVB  @TKDBR,(R4)
852 004112 117714 175070          BICB  #200,(R4)
853 004116 142714 000200          CMPB  (R4),#15
854 004122 122427 000015          BEQ   INSTR2
855 004126 001417          2S:  TSTB  @TPCSR
856 004130 105777 175054          BPL   2S
857 004134 100375          MOV   @TKDBR,@TPDBR
858 004136 017777 175044 175046          DEC   R3
859 004144 005303          BNE   1S
860 004146 001356          MOV   (SP)+,R4
861 004150 012604          MOV   (SP)+,R3
862 004152 012603          .INSTE: TYPE  MQM
863 004154 104402 005666          MOV   R3,-(SP)
864 004160 010346          MOV   R4,-(SP)
865 004162 010446          BR    .INST1
866 004164 000741          INSTR2: MOV  (SP)+,R4      ;RESTORE R4
867 004166 012604          MOV  (SP)+,R3      ;RESTORE R3
868 004170 012603          RTI
869 004172 000002
870
871                               ;CONVERT ASCII STRING TO OCTAL
872                               ;-----
873
874 004174 010546          .PARAM: MOV  R5,-(SP)
875 004176 010446          MOV  R4,-(SP)
876 004200 016605 000004          MOV  4(SP),R5
877 004204 012537 004364          MOV  (R5)+,LOLIM
878 004210 012537 004366          MOV  (R5)+,HILIM
879 004214 012537 004370          MOV  (R5)+,DEVADR
880 004220 112537 004372          MOVB (R5)+,LOBITS
881 004224 112537 004374          MOVB (R5)+,ADRCNT
882 004230 010566 000004          MOV  R5,4(SP)
883 004234 005005          PARAM1: CLR  R5
884 004236 012704 007502          MOV  #INBUF,R4
885 004242 122714 000015          CMPB #15,(R4)
886 004246 001420          BEQ  PAREAR
887 004250 121427 000060 1S:  CMPB (R4),#60
888 004254 002415          BLT  PAREAR
889 004256 121427 000067          CMPB (R4),#67
890 004262 003012          BGT  PAREAR
891 004264 142714 000060          BICB #60,(R4)
892 004270 152405          BICB (R4)+,R5
893 004272 122714 000015          CMPB #15,(R4)
894 004276 001406          BEQ  LIMITS

```

```

895 004300 006305
896 004302 006305
897 004304 006305
898 004306 000760
899 004310 104404
900 004312 000750
901
902
903
904
905 004314 020537 004366
906 004320 101373
907 004322 020537 004364
908 004326 103770
909 004330 133705 004372
910 004334 001365
911
912
913
914 004336 013704 004370
915 004342 010524
916 004344 062705 000002
917 004350 105337 004373
918 004354 001372
919 004356 012604
920 004360 012605
921 004362 000002
922 004364 000000
923 004366 000000
924 004370 000000
925 004372 000000
926 004373
927
928
929
930
931 004374 016637 000004 001276
932
933
934
935 004402 010537 001272
936 004406 010437 001270
937 004412 010337 001266
938 004416 010237 001264
939 004422 010137 001262
940 004426 010037 001260
941 004432 000002
942
943
944
945 004434 013700 001260
946 004440 013701 001262
947 004444 013702 001264
948 004450 013703 001266
949 004454 013704 001270
950 004460 013705 001272

```

```

ASL R5
ASL R5
ASL R5
BR 1$
PARERR: INSTER
BR PARAM1

;TEST TO SEE IF NUMBER IS WITHIN LIMITS
;-----
LIMITS: CMP R5,HILIM
BHI PARERR
CMP R5,LOLIM
BLO PARERR
BITB LOBITS,R5
BNE PARERR

;STORE NUMBER AT SPECIFIED ADDRESS

1$: MOV DEVADR,R4
MOV R5,(R4)+
ADD #2,R5
DECB ADCNT
BNE 1$
MOV (SP)+,R4
MOV (SP)+,R5
RTI

LOLIM: 0
HILIM: 0
DEVADR: 0
LOBITS: 0
ADCNT=LOBITS+1

;SAVE PC OF TEST THAT FAILED AND R0-R5
;-----
.SAVOS: MOV 4(SP),SAVPC ;SAVE R7 (PC)

;SAVE R0-R5

SVOS: MOV R5,SAVR5 ;SAVE R5
MOV R4,SAVR4 ;SAVE R4
MOV R3,SAVR3 ;SAVE R3
MOV R2,SAVR2 ;SAVE R2
MOV R1,SAVR1 ;SAVE R1
MOV R0,SAVR0 ;SAVE R0
RTI ;LEAVE.

;RESTORE R0-R5

.RESOS: MOV SAVR0,R0 ;RESTORE R0
MOV SAVR1,R1 ;RESTORE R1
MOV SAVR2,R2 ;RESTORE R2
MOV SAVR3,R3 ;RESTORE R3
MOV SAVR4,R4 ;RESTORE R4
MOV SAVR5,R5 ;RESTORE R5

```

```

951 004464 000002 RTI ;LEAVE
952
953 ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
954 -----
55
956 004466 104402 005672 .CONVR: TYPE MCRLF
957 004472 010046 .CHVRT: MOV R0,-(SP)
958 004474 010146 MOV R1,-(SP)
959 004476 010346 MOV R3,-(SF)
960 004500 010446 MOV R4,-(SP)
961 004502 010546 MOV R5,-(SP)
962 004504 017601 000012 MOV @12(SP),R1
963 004510 062766 000002 000012 ADD #2,12(SP)
964 004516 012137 004710 MOV (R1)+,WRDCNT
965 004522 112137 004712 1$: MOVB (R1)+,CHRCNT
966 004526 112137 004713 MOVB (R1)+,SPACNT
967 004532 013137 004714 MOV @2(R1)+,BINWRD
968 004536 122737 000003 004712 CMPB #3,CHRCNT
969 004544 001003 BNE 2$
970 004546 042737 177400 004714 BIC #177400,BINWRD
971 004554 013704 004714 2$: MOV BINWRD,R4
972 004560 113705 004712 MOVB CHRCNT,R5
973 004564 012700 001416 MOV #TEMP,R0
974 004570 010403 3$: MOV R4,R3
975 004572 042703 177770 BIC #177770,R3
976 004576 062703 000060 ADD #060,R3
977 004602 110320 MOVB R3,(R0)+
978 004604 000241 CLC
979 004606 006004 ROR R4
980 004610 000241 CLC
981 004612 006004 ROR R4
982 004614 000241 CLC
983 004616 006004 ROR R4
984 004620 005305 DEC R5
985 004622 001362 BNE 3$
986 004624 012703 007544 MOV #MDATA,R3
987 004630 114023 4$: MOVB -(R0),(R3)+
988 004632 105337 004712 DECB CHRCNT
989 004636 001374 BNE 4$
990 004640 105737 004713 TSTB SPACNT
991 004644 001405 BEQ 5$
992 004646 112723 000040 5$: MOVB #040,(R3)+
993 004652 105337 004713 DECB SPACNT
994 004656 001373 BNE 5$
995 004660 105013 6$: CLRB (R3)
996 004662 104402 007544 TYPE .MDATA
997 004666 005337 004710 DEC WRDCNT
998 004672 001313 BNE 1$
999 004674 012605 MOV (SP)+,R5
1000 004676 012604 MOV (SP)+,R4
1001 004700 012603 MOV (SP)+,R3
1002 004702 012601 MOV (SP)+,R1
1003 004704 012600 MOV (SP)+,R0
1004 004706 000002 RTI
1005 004710 000000 WRDCNT: 0
1006 004712 000000 CHRCNT: 0

```

SPACNT=CHRCNT+1
BINWRD: 0

1007 004713
1008 004714 000000
1009
1010
1011
1012
1013
1014
1015
1016 004716 011646
1017 004720 162716 000002
1018 004724 017616 000000
1019 004730 006316
1020 004732 042716 177001
1021 004736 062716 001330
1022 004742 017616 000000
1023 004746 000136
1024
1025
1026
1027
1028 004750 004737 007606
1029 004754 032777 010000 174220
1030 004762 001406
1031 004764 105777 174220
1032 004770 100003
1033 004772 112777 000207 174212
1034 005000 032777 020000 174174
1035 005006 001105
1036 005010 021637 001234
1037 005014 001404
1038 005016 011637 001234
1039 005022 105037 001325
1040 005026 104406
1041 005030 011605
1042 005032 162705 000002
1043 005036 011504
1044 005040 006304
1045 005042 061504
1046 005044 006304
1047 005046 042704 177001
1048 005052 062704 036316
1049 005056 012437 005172
1050 005062 012437 005204
1051 005066 011437 005216
1052 005072 105737 001325
1053 005076 001403
1054 005100 005737 005216
1055 005104 001040
1056 005106 104402 005672
1057 005112 104402 005672
1058 005116 005737 001220
1059 005122 001402
1060 005124 104402 006142
1061 005130 104402 006130
1062 005134 104411 005330

: TRAP DISPATCH SERVICE
: ARGUMENT OF TRAP IS EXTRACTED
: AND USED AS OFFSET TO OBTAIN POINTER
: TO SELECTED SUBROUTINE
: TRAPSR: MOV (SP), -(SP) : GET PC OF RETURN
: SUB #2, (SP) : =PC OF TRAP
: MOV #2(SP), (SP) : GET TRP
TRPOK: ASL (SP) : MULTIPLY TRAP ARG BY 2
: BIC #177001, (SP) : CLEAR UNWANTED BITS
: ADD #.TRPTAB, (SP) : POINTER TO SUBROUTINE ADDRESS
: MOV #2(SP), (SP) : SUBROUTINE ADDRESS
: JMP #2(SP) : GO TO SUBROUTINE
: ERROR HANDLER
: -----
: HLT: JSR PC, CKSWR : CHECK FOR SOFT SWR
: BIT #SW12, @SWR : BELL ON ERROR?
: BEQ XBX : BR IF NO BELL
: TSTB @TPCSR : TTY READY.
: BPL XBX : DON'T WAIT IF TTY NOT READY.
: MOVB #207, @TPDDBR : PUSH A BELL AT THE TTY.
: BIT #SW13, @SWR : DELETE ERROR PRINT OUT?
: BNE HALTS : BR IF NO PRINT OUT WANTED.
: CMP (SP), LSTERR : WAS THIS ERROR FOUND LAST TIME?
: BEQ IS : BR IF YES
: MOV (SP), LSTERR : RECORD BEING HERE
: CLRB ERRFLG : PREPARE HEADER
: SAVOS : SAVE ALL PROC REGISTERS
: MOV (SP), R5 : GET THE PC OF ERROR
: SUB #2, R5 : GET ADDRESS OF TRAP CALL
: MOV (R5), R4 : GET HLT INSTRUCTION
: ASL R4 : MULT BY TWO
: ADD (R5), R4 : DOUBLE IT
: ASL R4 : MULT AGAIN
: BIC #177001, R4 : CLEAR JUNK
: ADD #.ERRTAB, R4 : GET POINTER
: MOV (R4)+, ERRMSG : GET ERROR MESSAGE
: MOV (R4)+, DATAHD : GET DATA HEADER
: MOV (R4), DATABP : GET DATA TABLE
: TSTB ERRFLG : TYPE HEADREER
: BEQ TYPMSG : BR IF YES
: TST DATABP : DOES DATA TABLE EXIST?
: BNE TYPDAT : BR IF YES.
TYPMSG: TYPE ,MCR LF
: TYPE ,MCR LF
: TST LOCK
: BEQ IS
: TYPE ,MASTEK
IS: TYPE ,MSTN
: CNVRT ,XTSTN : SHOW IT

GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

1063	005140	104402	006217			TYPE	,MERRPC	;TYPE PC.
1064	005144	104411	005322			CNVRT	,ERTABO	;SHOW IT
1065	005150	104402	005672			TYPE	,MCRFL	;GIVE A CR/LF
1066	005154	112737	177777	001325		MOVB	#-1,ERRFLG	;NO MORE HEADER UNLESS NO DATA TABLE.
1067	005162	005737	005172			TST	ERRMSG	;IS THERE AN ERROR MESSAGE?
1068	005166	001402				BEQ	WRKO.FM	;BR IF NO.
1069	005170	104402				TYPE		;TYPE
1070	005172	000000			ERRMSG: 0			ERROR MESSAGE
1071	005174				WRKO.FM:			
1072	005174	005737	005204			TST	DATAHD	;DATA HEADER?
1073	005200	001402				BEQ	TYPDAT	;BR IF NO
1074	005202	104402				TYPE		;TYPE
1075	005204	000000			DATAHD: 0			DATA HEADER
1076	005206	005737	005216		TYPDAT: TST	DATABP		DATA TABLE?
1077	005212	001402				BEQ	RESREG	;BR IF NO.
1078	005214	104410				CONVRT		;SHOW
1079	005216	000000			DATABP: 0			DATA TABLE
1080	005220	104407			RESREG: RESOS			RESTORE PROC REGISTERS
1081	005222	022737	003522	000042	HALTS: CMP	#SENDAD,2#42		;IF ACT-11 AUTOMATIC MODE. HALT!!
1082	005230	001403				BEQ	1\$	
1083	005232	005777	173744			TST	2\$WR	;HALT ON ERROR?
1084	005236	100005				BPL	EXITER	;BR IF NO HALT ON ERROR
1085	005240	010046			1\$: PUSHRO			;SAVE RO
1086	005242	016600	000002			MOV	2(SP),RO	;SHOW ERROR PC IN DATA LIGHTS
1087	005246	000000				HALT		;HALT
1088	005250	012600				POPPO		;GET RO
1089	005252	005237	001232		EXITER: INC	ERRCNT		UPDATE ERROR CCUNT
1090	005256	032777	000400	173716		BIT	#SW08,2\$WR	;GOTO TOP OF TEST?
1091	005264	001007				BNE	1\$;BR IF YES
1092	005266	032777	002000	173706		BIT	#SW10,2\$WR	;GOTO NEXT TEST?
1093	005274	001411				BEQ	2\$;BR IF NO
1094	005276	013737	001216	001214		MOV	NEXT,RETURN	;SET FOR NEXT TEST
1095	005304	012706	001200		1\$: MOV	#STACK,SP		;RESET SP
1096	005310	013701	001404			MOV	DMCSR,R1	;SET UP R1
1097	005314	000177	173674			JMP	2\$RETURN	;GOTO SPECIFIED TEST
1098	005320	000002			2\$: RTI			;RETURN
1099	005322	000001			ERTABO: 1			
1100	005324	006	002			.BYTE	6,2	
1101	005326	001276				SAVPC		
1102	005330	000001			XTSTN: 1			
1103	005332	003	002			.BYTE	3,2	
1104	005334	001226				TSTNO		
1105								;ENTER HERE ON POWER FAILURE
1106								-----
1107								
1108								
1109	005336				.PFAIL:			
1110	005336	012737	005350	000024		MOV	#RESTART,24	;SET JP FOR POWER UP TRAP
1111	005344	000000				HALT		;HALT ON POWER DOWN NORMAL
1112	005346	000777				BR	.	
1113								
1114								;PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED
1115								
1116	005350				RESTAR:			
1117	005350	012737	005336	000024		MOV	#.PFAIL,24	;SET UP FOR POWER FAILURE
1118	005356	012706	001200			MOV	#STACK,5P	;RESET THE STACK POINTER

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1119 005362 013701 001404      MOV      DMCSR,R1      ;RESTORE R1
1120 005366 005037 001416      CLR      TEMP         ;READY FOR TIMER
1121 005372 005237 001416      INC      TEMP         ;PLUS ONE TO THE TIMER!
1122 005376 001375          BNE     -4            ;BR IF MORE TO GO
1123 005400 104402 005675      TYPE    ,MPFAIL      ;TYPE THE MESSAGE
1124 005404 104411 005430      CNVRT   ,PFTAB       ;TELL WHAT TEST TO RETURN TO.
1125 005410 105037 001325      CLRB   ERFLG        ;START CLEAN
1126 005414 005037 001234      CLR     LSTERR      ;.....
1127 005420 005011          CLR     (R1)        ;CLEAR MAINT BITS
1128 005422 104412          MSTCLR ;START CLEAN UP OF DEVICE
1129 005424 000177 173564      JMP     @RETURN     ;START DOING THAT TEST AGAIN.
1130 005430 000001          PFTAB: 1
1131 005432          .BYTE 3,2
1132 005434 001226          .TSTNO
1133
1134 005436          .DELAY:
1135 005436 012777 000020 173746      MOV     #20,@DMP04
1136 005444 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1137 005446 121111          121111 ;POKE CLOCK DELAY BIT
1138 005450          1$:
1139 005450 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1140 005452 121224          121224 ;PORT4<IBUS*11
1141 005454 032777 000020 173730      BIT     #BIT4,@DMP04 ;IS CLOCK BIT SET?
1142 005462 001772          BEQ    1$          ;BR IF NO
1143 005464 000002          RTI
1144
1145 005466          .MSTCLR:
1146 005466 152777 000100 173712      BISB   #BIT6,@DMCSRH ;SET MASTER CLEAR
1147 005474 142777 000300 173704      BICB   #BIT6!BIT7,@DMCSRH ;CLEAR MASTER CLEAR AND RUN
1148 005502 000002          RTI              ;RETURN
1149
1150 005504          .ROMCLK:
1151 005504 152777 000002 173674      BISB   #BIT1,@DMCSRH ;SET ROMI
1152 005512 013677 173676      MOV    @($P)+,@DMP06 ;LOAD INSTRUCTION IN SEL6
1153 005516 062746 000002          ADD    #2,-($P)      ;ADJUST STACK
1154 005522 032777 000100 173452      BIT    #SW06,@SWR    ;HALT IF SW06 =1
1155 005530 001401          BEQ    1$          ;BR IF SW06 =0
1156 005532 000000          HALT   ;HALT BEFORE CLOCKING INSTRUCTION
1157 005534 152777 000003 173644      BISB   #BIT1!BIT0,@DMCSRH ;CLOCK INSTRUCTION
1158 005542 142777 000007 173636      BICB   #BIT2!BIT1!BIT0,@DMCSRH ;CLEAR ROMO, ROMI, STEP
1159 005550 000002          RTI
1160
1161 005552          .DATACLK:
1162 005552 013637 001416      MOV    @($P)+,TEMP   ;PUT TICK COUNT IN TEMP
1163 005556 062746 000002          ADD    #2,-($P)      ;ADJUST STACK
1164 005562 152777 000020 173616      BISB   #BIT4,@DMCSRH ;SET STEP LU
1165 005570 027777 173610 173606      CMP    @DMCSR,@DMCSR ;WASTE TIME
1166 005576 142777 000020 173602      BICB   #BIT4,@DMCSRH ;CLEAR STEP LU
1167 005604 005337 001416      DEC    TEMP         ;DEC TICK COUNT
1168 005610 001364          BNE    1$          ;BR IF NOT DONE
1169 005612 000002          RTI              ;RETURN
1170 005614 000001          3$: .BLKW 1
1171
1172 005616          .TIMER:
1173 005616 013637 001416      MOV    @($P)+,TEMP   ;MOVE COUNT TO TEMP
1174 005622 062746 000002          ADD    #2,-($P)      ;ADJUST STACK

```

GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

```

1175 005626 104414
1176 005626 021364
1177 005630 021364
1178 005632 032777 000002 173552
1179 005640 001772
1180 005642
1181 005642 104414
1182 005644 021364
1183 005646 032777 000002 173536
1184 005654 001372
1185 005656 005337 001416
1186 005662 001361
1187 005664 000002
1188
1189 005666 020040 000077
(2) 005672 005015 000
(2) 005675 377 053520 020122
(2) 005733 377 047105 020104
(2) 005755 377 000122
(2) 005760 047377 020117 042504
(2) 006005 377 047111 052523
(2) 006031 377 042524 052123
(2) 006043 377 047514 045503
(2) 006072 051503 035122 000040
(2) 006100 042526 035103 000040
(2) 006106 040520 051523 051505
(2) 006117 105 051122 051117
(2) 006130 042524 052123 047040
(2) 006142 000052
(2) 006144 051777 052105 051440
(2) 006217 120 035103 000040
(2) 006224 020212 020040 020040
(2) 006263 377 020040 020040
(2) 006322 020212 050040 020103
(2) 006374 026777 026455 026455
(2) 006450 044377 053517 046440
(2) 006510 041777 051123 040440
(2) 006526 053377 041505 047524
(2) 006547 377 051102 050040
(2) 006606 044777 020106 046504
(2) 006704 053777 044510 044103
(2) 007016 051777 044527 041524
(2) 007054 051777 044527 041524
(2) 007114 044777 020123 044124
(2) 007154 047377 020117 042504
(2) 007205 377 051412 051127
(2) 007215 116 053505 020077
(2) 007223 377 042377 041515
(2) 007277 377 054105 042520
(2) 007320 024040 046504 024503
(2) 007330 024040 046513 024503
(2) 007340 042377 041515 030461
(2)
(2) 007454 000005
1190 007456 006 003
1191 007460 001246

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1S: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
021364 ;PORT4+IBUS* REG11
BIT #2,ADMP04 ;IS PGM CLOCK BIT CLEAR?
BEQ 1S ;BR IF YES

2S: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
021364 ;PORT4+IBUS* REG11
BIT #2,ADMP04 ;IS PGM CLOCK BIT SET?
BNE 2S ;BR IF YES
DEC TEMP ;DEC COUNT
BNE 1S ;BR IF NOT DONE
RTI ;RETURN

MQM: .ASCIZ / ?/
MCRLF: .ASCIZ <15><12>
MPFAIL: .ASCIZ <377>/PWR FAILED. RESTART AT TEST /
MEPASS: .ASCIZ <377>/END PASS DZDMC /
MR: .ASCIZ <377>/R/
MERR2: .ASCIZ <377>/NO DEVICES PRESENT./
MERR3: .ASCIZ <377>/INSUFFICIENT DATA!/
MTSTPC: .ASCIZ <377>/TEST PC-/
MLOCK: .ASCIZ <377>/LOCK ON SELECTED TEST/
MCSRX: .ASCIZ /CSR: /
MVECX: .ASCIZ /VEC: /
MPASSX: .ASCIZ /PASSES: /
MERRX: .ASCIZ /ERRORS: /
MTSTN: .ASCIZ /TEST NO: /
MASTEK: .ASCIZ /*/
MNEW: .ASCIZ <377>/SET SWITCH REG TO DMC11'S DESIRED ACTIVE./
MERRPC: .ASCIZ /PC: /
XHEAD: .ASCII <212>/ MAP OF DMC11 STATUS/
.ASCII <377>/ -----/
.ASCII <212>/ PC CSR STAT1 STAT2 STAT3/
.ASCII <377>/-----/
NUM: .ASCIZ <377>/HOW MANY DMC11'S TO BE TESTED?/
CSR: .ASCIZ <377>/CSR ADDRESS?/
VEC: .ASCIZ <377>/VECTOR ADDRESS?/
PRIO: .ASCIZ <377>/BR PRIORITY LEVEL? (4,5,6,7)?/
CRAM: .ASCIZ <377>/IF DMC HAS CRAM (M8204) TYPE "Y", IF CROM (M8200) TYPE "N"
MODU: .ASCIZ <377>/WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF M
LINE: .ASCIZ <377>/SWITCH PAC#1 (DDCMP LINE #)?/
BM: .ASCIZ <377>/SWITCH PAC#2 (BM873 BOOT ACC)?/
CONN: .ASCIZ <377>/IS THE LOOP BACK CONNECTOR ON?/
NOACT: .ASCIZ <377>/NO DEVICES ARE SELECTED/
SWMES: .ASCIZ <377><12>/SWR= /
SWMES1: .ASCIZ /NEW? /
CONERR: .ASCIZ <377><377>/DMC11 FOUND AT NON-STANDARD ADDRESS PC: /
CNERR: .ASCIZ <377>/EXPECTED FOUND/
DMCM: .ASCIZ / (DMC) /
KMCM: .ASCIZ / (KMC) /
SPEED: .ASCIZ <377>/DMC11-AR(REMOTE,LOW SPEED) OR DMC11-AL(LOCAL,HIGH SPEED) T
.EVEN
XSTATG: 5
.BYTE 6.3
TEMP1

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1192 007462 006 003 .BYTE 6,3
1193 007464 001250 TEMP2
1194 007466 006 003 .BYTE 6,3
1195 007470 001252 TEMP3
1196 007472 006 003 .BYTE 6,3
1197 007474 001254 TEMP4
1198 007476 006 002 .BYTE 6,2
1199 007500 001256 TEMPS
1200 .EVEN
1201 ;BUFFERS FOR INPUT-OUTPUT
1202
1203
1204 007502 000000 INBUF: 0
1205 007544 007544 .=. +40
1206 007544 000000 MDATA: 0
1207 007606 007606 .=. +40
1208
1209
1210 ;ROUTINE USED TO CHANGE SOFTWARE SWITCH
1211 ;REGISTER USING THE CONSOLE TERMINAL
1212 -----
1213
1214 007606 022737 000176 001202 CKSWR: CMP #SWREG,SWR ;IS THE SOFT SWR BEING USED?
1215 007614 001077 BNE CKSWR5 ;BR IF NO
1216 007616 105777 171362 TSTB JTKCSR ;IS DONE SET?
1217 007622 100003 BPL 2$ ;GO ON IF NOT SET
1218 007624 012737 177777 003734 MOV #-1,DONE ;IF DONE SET, SET FLAG
1219 007632 022777 000007 171346 2$: CMP #7,JTKDBR ;WAS CTRL G TYPED? (7 BIT ASCII)
1220 007640 001404 BEQ 1$ ;BR IF YES
1221 007642 022777 000207 171336 CMP #207,JTKDBR ;WAS CTRL G TYPED? (8 BIT ASCII)
1222 007650 001061 BNE CKSWR5 ;BR IF NO
1223 007652 010246 1$: MOV R2,-(SP) ;STORE R2
1224 007654 010346 MOV R3,-(SP) ;STORE R3
1225 007656 010446 MOV R4,-(SP) ;STORE R4
1226 007660 012737 177777 010016 MOV #-1,SWFLG ;SET SOFT TYPE OUT FLAG
1227 007666 005002 CKSWR1: CLR R2 ;CLEAR NEW SWR CONTENTS
1228 007670 012704 177777 MOV #-1,R4 ;SET FLAG TO ALL ONES
1229 007674 104402 007205 TYPE ,SWMES ;TYPE "SWR="
1230 007700 104411 CKSWR2: CNVRT ;TYPE OUT PRESENT CONTENTS
1231 007702 010052 SOFTSW ;OF SOFT SWITCH REGISTER
1232 007704 104402 007215 CKSWR3: TYPE SWMES1 ;TYPE "NEW"
1233 007710 004737 010020 CKSWR4: JSR PC,INCHAR ;GET RESPONSE
1234 007714 022703 000015 CMP #15,R3 ;WAS IT A CR?
1235 007720 001424 BEQ 5$ ;BR IF YES
1236 007722 022703 000012 CMP #12,R3 ;WAS IT A LF?
1237 007726 001416 BEQ 4$ ;BR IF YES
1238 007730 022703 000025 CMP #25,R3 ;WAS IT CTRL U?
1239 007734 001754 BEQ CKSWR1 ;BR IF YES(START OVER)
1240 007736 022703 000007 CMP #7,R3 ;IF CNTL G GET NEXT CHAR
1241 007742 001762 BEQ CKSWR4
1242 007744 005004 CLR R4 ;IT MUST BE A DIGIT SO CLR FLAG
1243 007746 042703 177770 BIC #177770,R3 ;ONLY 0-7 ARE LEGAL SO MASK OFF BITS
1244 007752 006302 ASL R2 ;SHIFT R2 3 TIMES
1245 007754 006302 ASL R2
1246 007756 006302 ASL R2
1247 007760 050302 BIS R3,R2 ;ADD LAST DIGIT

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GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

1248	007762	000752			BR	CKSWR4	;GET NEXT CHARACTER
1249	007764	012766	002002	000006	4S: MOV	#.START,6(SP)	;LF WAS TYPED SO GO TO START
1250	007772	005704			5S: TST	R4	;IS FLAG CLEAR?
1251	007774	001002			BNE	6S	;IF NOT DON'T CHANGE SOFT SWR
1252	007776	010277	171200		MOV	R2,@SWR	;IF YES THEN WRITE NEW CONTENTS TO SCF* SWR
1253	010002	005037	010016		6S: CLR	SWFLG	;CLEAR TYPEOUT FLAG
1254	010006	012604			MOV	(SP)+,R4	;RESTORE R4
1255	010010	012603			MOV	(SP)+,R3	;RESTORE R3
1256	010012	012602			MOV	(SP)+,R2	;RESTORE R2
1257	010014	000207			CKSWR5: RTS	PC	;RETURN
1258							
1259	010016	000000			SWFLG: 0		
1260							
1261	010020	105777	171160		INCHAR: TSTB	@TKCSR	
1262	010024	100375			BPL	.-4	
1263	010026	017703	171154		MOV	@TKDBR,R3	
1264	010032	105777	171152		TSTB	@TPCSR	
1265	010036	100375			BPL	.-4	
1266	010040	010377	171146		MOV	R3,@TPDBR	
1267	010044	042703	000200		BIC	#BIT7,R3	
1268	010050	000207			RTS	PC	
1269							
1270	010052	000001			SOFTSW: 1		
1271	010054	006	002		.BYTE	6.2	
1272	010056	000176			SWREG		

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010060 005737 001306
010064 001004
010066 104402 007154
010072 000000
010074 000776
010076 000241
010100 006137 001316
010104 005537 001316
010110 062737 000004 001322
010116 062737 000010 001320
010124 022737 001700 001320
010132 001006
010134 012737 001500 001320
010142 012737 001702 001322
010150 033737 001316 001306
010156 001747
010160 013700 001320
010164 013702 001322
010170 012037 001404
010174 011037 001374
010200 042737 177000 001374
010206 012037 001366
010212 012037 001370
010216 012037 001372
010222 012237 001230
010226 012237 001232
010232 012700 000002
010236 013737 001404 001406
010244 005237 001406
010250 013737 001406 001410
010256 005237 001410
010262 013737 001410 001412
010270 060037 001412
010274 013737 001412 001414
010302 060037 001414
010306 013737 001374 001376
010314 060037 001376
010320 013737 001376 001400
010326 060037 001400
010332 013737 001400 001402
010340 060037 001402
010344 032737 000002 001236
010352 001450
010354
010354 005737 000042

```
ROUTINE USED TO "CYCLE" THROUGH UP TO 16 DMC11'S
THIS ROUTINE SETS UP THE CONTROL ADDRESS FOR THE DIAGNOSTIC
AND RUNS THE SPECIFIED DMC11'S. THIS ROUTINE *MUST*
BE RUN FIRST BEFORE ENTERING THE DIAGNOSTIC FOR THE
SETUP NECESSARY.

CYCLE: TST DMACTV ;ARE ANY DMC11'S TO BE TESTED?
      BNE 1$ ;BR IF OK.
      TYPE ,NOACT ;NO DMC11'S SELECTED!!
      HALT ;STOP THE SHOW.
      BR -.2 ;DISQUALIFY CONT. SW.
1$: CLC ;CLEAR PROC. CARRY BIT.
   ROL RUN ;UPDATE POINTER
   ADC RUN ;CATCH CARRY FROM RUN
   ADD #4,MILK ;UPDATE POINTER
   ADD #10,CREAM ;UPDATE ADDRESS POINTER.
   CMP #DM.MAP+200,CREAM
   BNE 2$ ;KEEP GOING; NOT ALL TESTED FOR.
   MOV #DM.MAP,CREAM ;RESET ADDRESS POINTER.
   MOV #CNT.MAP,MILK ;RESET PASS COUNT POINTER
2$: BIT RUN,DMACTV ;IS THIS ONE ACTIVE?
   BEQ 1$ ;BR IF NO
   MOV CREAM,R0 ;GET ADDRESS POINTER
   MOV MILK,R2 ;GET PASS COUNT POINTER
   MOV (R0)+,DMCSR ;LOAD SYSTEM CTRL. REG
   MOV (R0),DMRVEC ;LOAD VECTOR
   BIC #177000,DMRVEC ;CLEAR UNWANTED BITS
   MOV (R0)+,STAT1 ;LOAD STAT1
   MOV (R0)+,STAT2 ;LOAD STAT2
   MOV (R0)+,STAT3 ;LOAD STAT3
   MOV (R2)+,PASCNT ;LOAD PASS COUNT
   MOV (R2)+,ERRCNT ;LOAD ERROR COUNT
   MOV #2,R0 ;SAVE CORE THIS WAY!
   MOV DMCSR,DMCSRH
   INC DMCSRH
   MOV DMCSRH,DMCTL
   INC DMCTL
   MOV DMCTL,DMP04
   ADD R0,DMP04
   MOV DMP04,DMP06
   ADD R0,DMP06

   MOV DMRVEC,DMRLVL ;PTY LVL
   ADD R0,DMRLVL
   MOV DMRLVL,DMTVEC ;TX VEC
   ADD R0,DMTVEC
   MOV DMTVEC,DMTLVL ;TX LVL
   ADD R0,DMTLVL

4$: BIT #SW01,STATSW ;IS TEST NO. SELECTED
   BEQ 7$ ;BR IF NO
   TST #42 ;RUNNING IN AUTO MODE?
```



GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

1329	010360	001045			BNE	7\$;BR IF YFS
1330	010362	104402	005672		TYPE	.MCRLF		
1331	010366	104403			INSTR			;GET TEST NO.
1332	010370	006130			MTSTN			
1333	010372	104405			PARAM			
1334	010374	000001			1			
1335	010376	001000			1000			
1336	010400	001226			TSTNO			
1337	010402	000			0			
1338	010403	001			.BYTE			
1339	010404	012700	012320		MOV	#TST1,RO		
1340	010410	022710			5\$: CMP	(PC)+,(RO)		;CMP FIRST WORD TO 12737
1341	010412	012737			MOV	(PC)+,2(PC)+		
1342	010414	001020			BNE	6\$;BR IF NOT SAME
1343	010416	023760	001226	000002	CMP	TSTNO,2(RO)		;DOES TSTNO MATCH?
1344	010424	001014			BNE	6\$;BR IF NO
1345	010426	022760	001226	000004	CMP	#TSTNO,4(RO)		;IS LAST WORD OK?
1346	010434	001010			BNE	6\$;BR IF NO
1347	010436	010037	001214		MOV	RO,RETURN		;IT IS A LEGAL TEST SO DO IT
1348	010442	104402	005755		TYPE	MR		
1349	010446	042737	000002	001236	BIC	#SW01,STRTSW		
1350	010454	000412			BR	8\$		
1351	010456	005720			6\$: TST	(RO)+		;POP RO
1352	010460	020027	033734		CMP	RO,#TLAST+10		;AT END YET?
1353	010464	001351			BNE	5\$;BR IF NO
1354	010466	104402	005666		TYPE	MQM		;YES ILLEGAL TEST NO.
1355	010472	000730			BR	4\$;TRY AGAIN
1356								
1357	010474	012737	012320	001214	7\$: MOV	#TST1,RETURN		;PREPARE RETURN ADDRESS
1358	010502	013701	001404		8\$: MOV	DMCSR,R1		;R1 = BASE DMC11 ADDRESS
1359	010506	000177	170502		JMP	2RETURN		;GO START TESTING.
1360								
1361								
1362								
1363								
1364								
1365								
1366								
1367								
1368								
1369								
1370	010512							
1371	010512	000005			AUTO.SIZE:	RESET		;INSURE A BUS INIT.
1372	010514	012702	001500		CSRMAP: MOV	#DM.MAP,R2		;LOAD MAP POINTER.
1373	010520	005022			1\$: CLR	(R2)+		;ZERO ENTIRE MAP
1374	010522	022702	001700		CMP	#DM.END,R2		;ALL DONE?
1375	010526	001374			BNE	1\$;BR IF NO
1376	010530	005037	001310		CLR	DMNUM		;SET OCTAL NUMBER OF DMC11'S TO 0
1377	010534	012702	001500		MOV	#DM.MAP,R2		;R2 POINTS TO DMC MAP
1378	010540	005037	001306		CLR	DMACTV		;CLEAR ACTIVE
1379	010544	032737	000001	001236	BIT	#SW00,STRTSW		;QUESTIONS?
1380	010552	001002			BNE	+6		;BR IF YES
1381	010554	000137	011252		JMP	7\$;IF NO SKIP QUESTIONS
1382	010560	012737	000001	001256	MOV	#1,TEMPS		;START WITH 1
1383	010566	104403			INSTR			
1384	010570	006450			NUM			

:ROUTINE USED TO "AUTO SIZE" THE DMC11
 :CSR AND VECTOR.
 :NOTE: THE CSR MAY BE ANY WHERE IN THE FLOATING
 ADDRESS RANGE (160000:164000)
 AND THE VECTOR MAY BE ANY WHERE IN THE
 FLOATING VECTOR RANGE (300:770)

1385	010572	104405			PARAM		
1386	010574	000001			1		
1387	010576	000020			16.		
1388	010600	001252			TEMP3		
1389	010602	000			.BYTE	0	
1390	010603	001			.BYTE	1	
1391	010604	013737	001252	001310	MOV	TEMP3,DMNUM	;DMNUM = HOW MANY
1392	010612	104402	005672		TYPE	,MCRLF	
1393	010616	104410		12\$:	CONVRT		;TYPE WHICH DMC IS BEING DONE
1394	010620	012002			WHICH		;TEMPS IS WHICH DMC
1395	010622	005237	001256		INC	TEMPS	
1396	010626	104403			INSTR		
1397	010630	006510			CSR		
1398	010632	104405			PARAM		
1399	010634	160000			160000		
1400	010636	164000			164000		
1401	010640	001254			TEMP4		
1402	010642	000			.BYTE	0	
1403	010643	001			.BYTE	1	
1404	010644	013722	001254		MOV	TEMP4,(R2,+)	;STORE CSR IN MAP
1405	010650	104403			INSTR		
1406	010652	006526			VEC		
1407	010654	104405			PARAM		
1408	010656	000000			0		
1409	010660	000776			776		
1410	010662	001254			TEMP4		
1411	010664	000			.BYTE	0	
1412	010665	001			.BYTE	1	
1413	010666	013712	001254		MOV	TEMP4,(R2)	;STORE VECTOR IN MAP
1414	010672	104402		10\$:	TYPE		
1415	010674	006547			PRI0		;ASK WHAT BR LEVEL
1416	010676	004737	012266		JSR	PC,INTTY	;GET RESPONSE
1417	010702	022703	000024		CMP	#24,R3	
1418	010706	101014			BHI	50\$;BR IF LESS THAN 4
1419	010710	022703	000027		CMP	#27,R3	
1420	010714	103411			BLO	50\$;BR IF GREATER THAN 7
1421	010716	012704	000011		MOV	#11,R4	;R4 = NUMBER OF SHIFTS
1422	010722	006303			ASL	R3	;SHIFT R3 LEFT
1423	010724	005304			DEC	R4	;DEC SHIFT COUNT
1424	010726	001375			BNE	-4	;BR IF NOT DONE
1425	010730	042703	170777		BIC	#170777,R3	;BIC UNWANTED BITS
1426	010734	050312			BIS	R3,(R2)	;PUT BR LEVEL IN STATUS MAP
1427	010736	000403			BR	8\$;CONTINUE
1428	010740	104402		50\$:	TYPE		
1429	010742	005666			MQM		;RESPONSE IS OUT OF LIMITS
1430	010744	000752			BR	10\$;TRY AGAIN
1431	010746	104402		8\$:	TYPE		
1432	010750	006606			CRAM		;DOES DMC HAVE CRAM?
1433	010752	004737	012266		JSR	PC,INTTY	;GET REPLY
1434	010756	022703	000131		CMP	#131,R3	
1435	010762	001427			BEQ	9\$;YES
1436	010764	022703	000116		CMP	#116,R3	;NO
1437	010770	001403			BEQ	40\$;NOT A Y OR N
1438	010772	104402			TYPE		
1439	010774	005666			MQM		;TYPE ""
1440	010776	000763			BR	8\$;ASK AGAIN

GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

1441	011000	104402		40S:	TYPE		
1442	011002	007340			SPEED		:DMC11-AR OR DMC11-AL?
1443	011004	004737	012266		JSR	PC,INTTY	:GET RESPONSE
1444	011010	022703	000122		CMP	#122,R3	:IS IT R
1445	011014	001414			BEQ	16S	:BR IF REMOTE
1446	011016	022703	000114		CMP	#114,R3	:IS IT L
1447	011022	001403			BEQ	41S	:BR IF LOCAL
1448	011024	104402			TYPE		
1449	011026	005666			MQM		
1450	011030	000763			BR	40S	:TRY AGAIN
1451	011032	052762	000002 000004	41S:	BIS	#BIT1,4(R2)	:SET BIT1 IN STAT3
1452	011040	000402			BR	16S	:CONTINUE
1453	011042	052712	100000	9S:	BIS	#BIT15,(R2)	:SET BIT 15 IF CRAM
1454	011046	104402		16S:	TYPE		
1455	011050	006704			MODU		:ASK WHICH LINE UNIT
1456	011052	004737	012266		JSR	PC,INTTY	:GET REPLY
1457	011056	022703	000021		CMP	#21,R3	: "1"
1458	011062	001417			BEQ	30S	
1459	011064	022703	000022		CMP	#22,R3	: "2"
1460	011070	001412			BEQ	31S	
1461	011072	022703	000116		CMP	#116,R3	: "N"
1462	011076	001403			BEQ	32S	
1463	011100	104402			TYPE		
1464	011102	005666			MQM		: IF NOT A 1,2 OR N TYPE ""
1465	011104	000760			BR	16S	:TRY AGAIN
1466	011106	052722	010000	32S:	BIS	#BIT12,(R2)+	:SET BIT 12 IN STAT2 IF NO LU
1467	011112	022222			CMP	(R2)+,(R2)+	:POP OVER STAT2 AND STAT3
1468	011114	000447			BR	33S	
1469	011116	052712	020000	31S:	BIS	#BIT13,(R2)	:SET BIT 13 IN STAT2 IF M8202
1470	011122	104402		30S:	TYPE		
1471	011124	007114			CONN		:ASK IF LOOP-BACK IS ON
1472	011126	004737	012266		JSR	PC,INTTY	:GET REPLY
1473	011132	022703	000131		CMP	#131,R3	:Y
1474	011136	001406			BEQ	17S	
1475	011140	022703	000116		CMP	#116,R3	:N
1476	011144	001406			BEQ	18S	
1477	011146	104402			TYPE		
1478	011150	005666			MQM		: IF NOT Y OR N TYPE ""
1479	011152	000763			BR	30S	:TRY AGAIN
1480	011154	052722	040000	17S:	BIS	#BIT14,(R2)+	:TURNAROUND IS CONNECTED
1481	011160	000402			BR	19S	
1482	011162	042722	040000	18S:	BIC	#BIT14,(R2)+	:NO TURNAROUND
1483	011166			19S:			
1484	011166	104403			INSTR		
1485	011170	007016			LINE		
1486	011172	104405			PARAM		
1487	011174	000000			0		
1488	011176	000377			377		
1489	011200	001254			TEMP4		
1490	011202	000			.BYTE	0	
1491	011203	001			.BYTE	1	
1492	011204	113722	001254		MOVE	TEMP4,(R2)+	:STORE SWITCH PAC IN MAP
1493	011210	104403			INSTR		
1494	011212	007054			BM		
1495	011214	104405			PARAM		
1496	011216	000000			0		

1497	011220	000377			377			
1498	011222	001254			TEMP4			
1499	011224	000			.BYTE	0		
1500	011225	001			.BYTE	1		
1501	011226	113722	001254		MOVB	TEMP4,(R2)+	:STORE SWITCH PAC IN MAP	
1502	011232	005722			TST	(R2)+	:POP OVER STAT3	
1503	011234	005337	001252	33\$:	DEC	TEMP3	:DEC DMC COUNT	
1504	011240	001402			BEQ	34\$:BR IF DONE	
1505	011242	000137	010612		JMP	12\$:JUMP IF NOT	
1506	011246	000137	011702	34\$:	JMP	13\$:CONTINUE	
1507	011252	012701	160000	7\$:	MOV	#160000,R1	:SET FOR FIRST ADDRESS TO BE TESTED	
1508	011256	012737	011774	000004	MOV	#65,2#4	:SET FOR NON-EXISTANT DEVICE TIME OUT	
1509	011264	005011		2\$:	CLR	(R1)	:CLEAR SEL0	
1510	011266	005711			TST	(R1)	:IF DMC11 DMC5R S/B 0	
1511	011270	001172			BNE	3\$:IF NO DEV ; TRAP TO 4. IF NO BIT 8 THEN NO DMC1	
1512	011272	005061	070006		CLR	6(R1)	:CLEAR SEL6	
1513	011276	005761	000006		TST	6(R1)	:IF DMC11 THEN DMRIC S/B =0!	
1514	011302	001165			BNE	3\$:BR IF NOT DMC11	
1515	011304	012711	002000		MOV	#BIT10,(R1)	:SET ROM0	
1516	011310	005061	000004		CLR	4(R1)	:CLEAR SEL4	
1517	011314	012761	125252	000006	MOV	#125252,6(R1)	:WRITE THIS TO SEL6	
1518	011322	052711	020000		BIS	#BIT13,(R1)	:WRITE IT!	
1519	011326	022761	125252	000004	CMP	#125252,4(R1)	:WAS IT WRITTEN?	
1520	011334	001004			BNE	21\$:IF NO IT IS NOT CRAM	
1521	011336	052762	100000	000002	BIS	#BIT15,2(R2)	:SET BIT15 IF CRAM	
1522	011344	000431			BR	22\$		
1523	011346	012711	001000	21\$:	MOV	#BIT9,(R1)	:SET ROM1	
1524	011352	012761	100417	000006	MOV	#100417,6(R1)	:PUT INSTRUCTION IN SEL6	
1525	011360	012711	001400		MOV	#BIT9:BIT8,(R1)	:CLOCK INSTRUCTION (MICRO PROC PC TO 3)	
1526	011364	012711	002000		MOV	#BIT10,(R1)	:SET ROM0	
1527	011370	022761	000626	000006	CMP	#626,6(R1)	:IS IT LOCAL CROM	
1528	011376	001411			BEQ	23\$:BR IF YES	
1529	011400	022761	016520	000006	CMP	#16520,6(R1)	:IS IT REMOTE CROM?	
1530	011406	001410			BEQ	22\$:BR IF YES	
1531	011410	022761	177777	000006	CMP	#-1,6(R1)	:NO CROM?	
1532	011416	001404			BEQ	22\$:BR IF YES	
1533	011420	000516			BR	3\$:NOT A DMC	
1534	011422	052762	000002	000006	23\$:	BIS	#BIT1,6(R2)	:SET BIT 1 IN STAT3
1535					22\$:	MOV	R1,(R2)+	:AT THIS POINT IT IS ASSUMED THAT R1 HOLDS A DMC11 CSR ADDRESS.
1536	011430	010122			15\$:	MOV	#BIT9,(R1)	:STORE CSR IN CORE TABLE.
1537	011432	012711	001000		MOV	#BIT9,(R1)	:CLEAR LINE UNIT LOOP	
1538	011436	005061	000004		CLR	4(R1)	:CLEAR PORT4	
1539	011442	012761	122113	000006	MOV	#122113,6(R1)	:LOAD INSTRUCTION (CLR DTR)	
1540	011450	052711	000400		BIS	#BIT8,(R1)	:CLOCK INSTRUCTION	
1541	011454	012761	021264	000006	MOV	#021264,6(R1)	:LOAD INSTRUCTION	
1542	011462	052711	000400		BIS	#BIT8,(R1)	:CLOCK INSTRUCTION	
1543	011466	122761	000377	000004	CMPB	#377,4(R1)	:IS IT ALL ONES?	
1544	011474	001003			BNE	+.10	:BR IF NO	
1545	011476	052712	010000		BIS	#BIT12,(R2)	:IF YES, NO LINE UNIT, SET STATUS BIT	
1546	011502	000436			BR	20\$		
1547	011504	032761	000002	000004	BIT	#BIT1,4(R1)	:IS SWITCH A ONE?	
1548	011512	001403			BEQ	+.10	:BR IF M8201	
1549	011514	052712	060003		BIS	#BIT13:BIT14,(R2)	:M8202 ASSUME CONNECTOR	
1550	011520	000427			BR	20\$:CONNECTOR ON)	
1551	011522	032761	000010	000004	BIT	#BIT3,4(R1)	:IS M8201 SET	
1552	011530	001023			BNE	20\$:BR IF M8201 NO CONNECTOR (ON LINE)	

1553	011532	012761	000100	000004		MOV	#BIT6,4(R1)	;LOAD PORT4
1554	011540	012761	122113	000006		MOV	#122113,6(R1)	;LOAD INSTRUCTION
1555	011546	052711	000400			BIS	#BIT8,(R1)	;CLOCK INSTRUCTION(SET DTR)
1556	011552	012761	021264	000006		MOV	#021264,6(R1)	;LOAD INSTRUCTION
1557	011560	052711	000400			BIS	#BIT8,(R1)	;CLOCK INSTRUCTION(READ MODEM REG)
1558	011564	032761	000010	000004		BIT	#BIT3,4(R1)	;IS MRDY SET NOW?
1559	011572	001402				BEQ	20\$;BR IF NO CONNECTOR
1560	011574	052712	040000			BIS	#BIT14,(R2)	;SET STATUS BIT FOR CONNECTOR
1561	011600	005722			20\$:	TST	(R2)+	;POP POINTER
1562	011602	012761	021324	000006		MOV	#021324,6(R1)	;PUT INSTRUCTION IN PORT6
1563	011610	012711	001400			MOV	#BIT9!BIT8,(R1)	;PORT4+LU IS
1564	011614	156122	000004			BISB	4(R1),(R2)+	;STORE ODCMP LINE # IN TABLE
1565	011620	012761	021344	000006		MOV	#021344,6(R1)	;PORT6+INSTRUCTION
1566	011626	012711	001400			MOV	#BIT8!BIT9,(R1)	;CLOCK INSTR.
1567	011632	156122	000004			BISB	4(R1),(R2)+	;STORE BM873 ADD IN TABLE
1568	011636	005722				TST	(R2)+	;POP OVER STAT3
1569	011640	005011				CLR	(R1)	;CLEAR ROMI
1570	011642	005237	001310			INC	DMNUM	;UPDATE DEVICE COUNTER
1571	011646	022737	000020	001310		CMP	#20,DMNUM	;ARE MAX. NO. OF DEV FOUND?
1572	011654	001412				BEQ	13\$;YES DON'T LOOK FOR ANY MORE.
1573	011656	005011			3\$:	CLR	(R1)	;CLEAR BIT 10
1574	011660	005061	000006			CLR	6(R1)	;CLEAR SEL 6
1575	011664	062701	000010		14\$:	ADD	#10,R1	;UPDATE CSR POINTER ADDRESS
1576	011670	022701	164000			CMP	#164000,R1	
1577	011674	001402				BEQ	13\$;BR IF DONE
1578	011676	000137	011264			JMP	2\$;JUMP IF NOT
1579	011702	005037	001306		13\$:	CLR	DMACTV	
1580	011706	005737	001310			TST	DMNUM	;WERE ANY DMC11'S FOUND AT ALL?
1581	011712	001423				BEQ	5\$;ERROR AUTO SIZER FOUND NO DMC11'S IN THIS SYS.
1582	011714	013701	001310			MOV	DMNUM,R1	
1583	011720	010137	001314			MOV	R1,SAVNUM	;SAVE NUMBER OF DEVICES
1584	011724	000241			4\$:	CLC		
1585	011726	006137	001306			ROL	DMACTV	;GENERATE ACTIVE REGISTER OF DEVICES.
1586	011732	005237	001306			INC	DMACTV	;SET THE BIT
1587	011736	005301				DEC	R1	
1588	011740	001371				BNE	4\$;BR IF MORE TO GENERATE
1589	011742	012737	000006	000004		MOV	#6,2#4	;RESTORE TRAP VECTOR
1590	011750	013737	001306	001312		MOV	DMACTV,SAVACT	;SAVE ACTIVE REGISTER
1591	011756	000137	012010			JMP	VECMAP	;GO FIND THE VECTOR NOW.
1592	011762	104402	005760		5\$:	TYPE	MERR2	;NOTIFY OPR THAT NO DMC11'S FOUND.
1593	011766	005000				CLR	R0	;MAKE DATA LIGHTS ZERO
1594	011770	000000				HALT		;STOP THE SHOW
1595	011772	000776				BR	.-2	;DISABLE CONT. SW.
1596	011774	012716	011664		6\$:	MOV	#14\$, (SP)	;ENTERED BY NON-EXISTANT TIME-OUT.
1597	012000	000002				RTI		;RETURN TO MAINSTREAM
1598								
1599	012002	000001			WHICH:	1		
1600	012004	002	002			.BYTE	2.2	
1601	012006	001256				TEMP5		
1602								
1603	012010	032737	000001	001236	VECMAP:	BIT	#5W00,STRTSW	
1604	012016	001114				BNE	5\$	
1605	012020	012737	000340	000022		MOV	#340,2#22	;SET IOT TRAP PRIO TO 7
1606	012026	012737	012202	000020		MOV	#4\$,2#20	;SET IOT TRAP VECTOR
1607	012034	012702	001500			MOV	#DM.MAP,R2	;SET SOFTWARE POINTER
1608	012040	012700	000300			MOV	#300,R0	;FLOATING VECTORS START HERE.


```

1609 012044 012701 000302      MOV      #302,R1      ;PC OF IOT INSTR.
1610 012050 010120      1$: MOV      R1,(R0)+  ;START FILLING VECTOR AREA
1611 012052 012721 000004      MOV      #4,(R1)+   ;WITH +2; IOT
1612 012056 022021      CMP      (R0)+,(R1)+ ;ADD 2 TO R0 +R1
1613 012060 020127 001000      CMP      R1,#1000
1614 012064 101771      BLOS    1$          ;BR IF MORE TO FILL
1615 012066 013737 001306 001246      MOV      DMACTV,TEMP1 ;STORE TEMPORALLY
1616 012074 006037 001246      2$: ROR      TEMP1    ;BRING OUT A BIT
1617 012100 103063      BCC     5$          ;BR IF ALL DONE
1618 012102 012704 000012      MOV      #12,R4     ;R4 IS INDEX REGISTER
1619 012106 016437 012252 177776      MOV      BRVL(R4),PS ;SET PS TO 7
1620 012114 011201      MOV      (R2),R1
1621 012116 012761 000200 000004      MOV      #200,4(R1)
1622 012124 012711 001000      MOV      #BIT9,(R1)
1623 012130 012761 121111 000006      MOV      #121111,6(R1) ;SET ROMI
1624 012136 012711 001400      MOV      #BIT9:BIT8,(R1) ;PUT INSTRUCTION IN PORT6
1625 012142 105200      7$: INCB    RO        ;FORCE AN INTERRUPT
1626 012144 001376      BNE     .-2         ;STALL
1627 012146 162704 000002      SUB     #2,R4       ;FOR TIME TO INTERUPT
1628 012152 001404      BEQ     6$          ;GET NEXT LOWEST PS LEVEL
1629 012154 016437 012252 177776      MOV      BRVL(R4),PS ;BR IF R4 = 0
1630 012162 000767      BR      7$          ;MOVE NEXT LOWER LEVEL IN PS
1631 012164 052762 005300 000002      6$: BIS     #5300,2(R2) ;BR TO DELAY
1632 012172 005011      3$: CLR     (R1)      ;NO INTERUPT ASSUME 300 AT LEVEL 5 AND FIX DMC11
1633 012174 062702 000010      ADD     #10,R2      ;CLEAR ROMI
1634 012200 000735      BR      2$          ;POP SOFTWARE POINTER
1635 012202 051662 000002      4$: BIS     (SP),2(R2) ;KEEP GOING
1636 012206 042762 000007 000002      BIC     #7,2(R2)    ;GET VECTOR ADDRESS
1637 012214 016405 012254      MOV     BRVL+2(R4),R5 ;CLEAR JUNK
1638 012220 006305      ASL    R5           ;GET BR LEVEL OF DMC11
1639 012222 006305      ASL    R5           ;SHIFT LEVEL 4 PLACES
1640 012224 006305      ASL    R5           ;TO THE LEFT FOR THE
1641 012226 006305      ASL    R5           ;STATUS TABLE
1642 012230 042705 170777      BIC     #170777,R5  ;CLEAR UNWANTED BITS
1643 012234 050562 000002      BIS     R5,2(R2)    ;PUT BR LEVEL IN STATUS TABLE
1644 012240 022626      CMP     (SP)+,(SP)+ ;POP IOT JUNK OFF STACK
1645 012242 012716 012172      MOV     #3$, (SP)   ;SET FOR RETURN
1646 012246 000002      RTI
1647 012250 000207      5$: RTS     PC        ;ALL DONE WITH "AUTO SIZING"
1648
1649 012252 000000      BRVL:  0           ;LEVEL 0
1650 012254 000000      0           ;LEVEL 0
1651 012256 000200      200          ;LEVEL 4
1652 012260 000240      240          ;LEVEL 5
1653 012262 000300      300          ;LEVEL 6
1654 012264 000340      340          ;LEVEL 7
1655
1656
1657 012266 105777 166712      INTTY: TSTB   @TKCSR  ;WAIT FOR DONE
1658 012272 100375      BPL    .-4
1659 012274 017703 166706      MOV    @TKDBR,R3   ;PUT CHAR IN R3
1660 012300 105777 166704      TSTB  @TPCSR
1661 012304 100375      BPL    .-4         ;WAIT UNTIL PRINTER IS READY
1662 012306 010377 166700      MOV    R3,@TPDBR  ;ECHO CHAR
1663 012312 042703 000240      BIC    #BIT7:BITS,R3 ;MASK OFF LOWER CASE
1664 012316 000207      RTS     PC        ;RETURN

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012320	012737	000001	001226
012326	012737	012426	001216
012334	012737	012366	001220
012342	013701	001404	
012346	012700	000004	
012352	012737	012420	000004
012360	012737	000340	000006
012366	005711		
012370	000240		
012372	104401		
012374	062701	000002	
012400	005300		
012402	001371		
012404	012737	000006	000004
012412	005037	000006	
012416	104400		
012420	011602		
012422	104001		
012424	000002		
012426	012737	000002	001226
012434	012737	012456	001216
012442	005011		
012444	005005		
012446	011104		
012450	001401		
012452	104002		
012454	104400		

```
***** TEST 1 *****  
*VERIFY THAT REFERENCING UNIBUS DEVICE REGISTERS  
*DOES NOT CAUSE A TIME OUT TRAP  
*****  
: TEST 1  
-----  
TST1: MOV #1,TSTNO  
MOV #TST2,NEXT  
MOV #1$,LOCK  
  
MOV DMCSR,R1 ;R1 CONTAINS BASE DMC11 ADDRESS  
MOV #4,R0 ;R1 CONTAINS BASE DMC11 ADDRESS  
MOV #2$,4 ;4 REGISTERS TO BE TESTED  
MOV #340,6 ;SET UP TIMEOUT TRAP  
1$: TST (R1) ;LEVEL 7  
NOP ;REFERENCE DEVICE REGISTER  
SCOPE1 ;SW09=1?  
ADD #2,R1 ;NEXT REGISTER  
DEC R0 ;DEC REGISTER COUNT  
BNE 1$ ;BR IF NOT LAST REGISTER  
MOV #6,4 ;RESTORE LOC 4  
CLR 6 ;RESTORE LOC 6  
2$: SCOPE ;SCOPE THIS TEST  
MOV (SP),R2 ;GET PC OF TRAP  
HLT 1 ;TIME-OUT ERROR  
RTI
```

***** TEST 2 *****
*VERIFY THAT RUN CAN BE CLEARED

```
: TEST 2  
-----  
TST2: MOV #2,TSTNO  
MOV #TST3,NEXT  
  
CLR (R1) ;R1 CONTAINS BASE DMC11 ADDRESS  
CLR R5 ;CLEAR DMCSR  
MOV (R1),R4 ;CLEAR "EXPECTED"  
BEQ 1$ ;PUT DMCSR IN "FOUND"  
HLT 2 ;BR IF CLEARED  
1$: SCOPE ;ERROR DMCSR NOT CLEARED  
;SCOPE THIS TEST
```

***** TEST 3 *****
*UNIBUS REGISTER WORD DUAL ADDRESSING TEST
*LOAD ALL REGISTERS WITH INCREMENTING PATTERN
*READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING

: TEST 3

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1721
1722 012456 012737 000003 001226      TST3:  MOV      #3,TSTNO
1723 012464 012737 012606 001216      MOV      #TST4,NEXT
1724 012472 012737 012506 001220      MOV      #1$,LOCK
1725
1726 012500 104412                MSTCLR                ;R1 CONTAINS BASE DMC11 ADDRESS
1727 012502 012700 000001      MOV      #1,R0        ;MASTER CLEAR DMC11
1728 012506 005011      1$:  CLR      (R1)        ;START PATTERN AT 1
1729 012510 010005      MOV      R0,R5        ;CLEAR REGISTER
1730 012512 010011      MOV      R0,(R1)      ;PUT DATA IN "EXPECTED"
1731 012514 011104      MOV      (R1),R4      ;WRITE DMC REGISTER WITH PATTERN
1732 012516 020504      CMP      R5,R4        ;READ DMC REGISTER INTO "FOUND"
1733 012520 001401      BEQ      2$          ;IS DATA CORRECT
1734 012522 104002      HLT      2           ;BR IF YES
1735 012524 104401      2$:  SCOPE1          ;DATA ERROR
1736 012526 005721      TST      (R1)+        ;SW09=1?
1737 012530 005200      INC      R0          ;NEXT REGISTER
1738 012532 022700 000005      CMP      #5,R0       ;INCREMENT DATA PATTERN
1739 012536 001363      BNE      1$          ;LAST REGISTER?
1740 012540 013701 001404      MOV      DMCSR,R1    ;BR IF NO
1741 012544 012700 000001      MOV      #1,R0       ;BASE DMC11 ADDRESS TO R1
1742 012550 012737 012556 001220      MOV      #3$,LOCK   ;RESTART PATTERN AT 1
1743 012556 010005      3$:  MOV      R0,R5        ;NEW SCOPE1
1744 012560 011104      MOV      (R1),R4      ;PUT DATA IN "EXPECTED"
1745 012562 020504      CMP      R5,R4        ;READ DMC REGISTER INTO "FOUND"
1746 012564 001401      BEQ      4$          ;IS DATA CORRECT
1747 012566 104002      HLT      2           ;BR IF YES
1748 012570 104401      4$:  SCOPE1          ;DUAL ADDRESSING ERROR
1749 012572 005721      TST      (R1)+        ;SW09=1?
1750 012574 005200      INC      R0          ;NEXT REGISTER
1751 012576 022700 000005      CMP      #5,R0       ;INCREMENT PATTERN
1752 012602 001365      BNE      3$          ;LAST REGISTER?
1753 012604 104400      SCOPE                ;BR IF NO
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1764 012606 012737 000004 001226      TST4:  MOV      #4,TSTNO
1765 012614 012737 012704 001216      MOV      #TST5,NEXT
1766 012622 012737 012632 001220      MOV      #1$,LOCK
1767 012630 104412                MSTCLR                ;MASTER CLEAR DMC11
1768 012632 013701 001404      MOV      DMCSR,R1    ;PLT REGISTER ADDRESS IN R1
1769 012636 012705 000001      MOV      #BIT0,R5    ;PUT DATA IN "EXPECTED"
1770 012642 010511      MOV      R5,(R1)     ;WRITE BIT 0
1771 012644 011104      MOV      (R1),R4     ;READ CONTROL STATUS REGISTER
1772 012646 020504      CMP      R5,R4        ;IS DATA CORRECT
1773 012650 001401      BEQ      2$          ;BR IF YES
1774 012652 104002      HLT      2           ;DATA ERROR
1775 012654 104401      2$:  SCOPE1          ;SW09 JP?
1776 012656 012737 012664 001220      MOV      #3$,LOCK   ;NEW SCOPE1

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:***** TEST 4 *****
:*CONTROL STATUS REGISTER WRITE/READ TEST*
:*SET BIT0, VERIFY BIT0 WAS SET
:*CLEAR BIT0, VERIFY BIT0 WAS CLEARED
:*****

```

: TEST 4

```

1764 012606 012737 000004 001226      TST4:  MOV      #4,TSTNO
1765 012614 012737 012704 001216      MOV      #TST5,NEXT
1766 012622 012737 012632 001220      MOV      #1$,LOCK
1767 012630 104412                MSTCLR                ;MASTER CLEAR DMC11
1768 012632 013701 001404      MOV      DMCSR,R1    ;PLT REGISTER ADDRESS IN R1
1769 012636 012705 000001      MOV      #BIT0,R5    ;PUT DATA IN "EXPECTED"
1770 012642 010511      MOV      R5,(R1)     ;WRITE BIT 0
1771 012644 011104      MOV      (R1),R4     ;READ CONTROL STATUS REGISTER
1772 012646 020504      CMP      R5,R4        ;IS DATA CORRECT
1773 012650 001401      BEQ      2$          ;BR IF YES
1774 012652 104002      HLT      2           ;DATA ERROR
1775 012654 104401      2$:  SCOPE1          ;SW09 JP?
1776 012656 012737 012664 001220      MOV      #3$,LOCK   ;NEW SCOPE1

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1777 012664 042711 000001      3$: BIC    #BIT0,(R1)      ;CLEAR BIT 0
1778 012670 005005              CLR    R5              ;CLEAR "EXPECTED"
1779 012672 011104              MOV    (R1),R4        ;READ CONTROL STATUS REGISTER
1780 012674 001402              BEQ    4$             ;BR IF ZERO
1781 012676 104002              HLT    2              ;DATA ERROR BIT0 NOT CLEARED
1782 012700 104401              SCOPI                      ;SW09 UP?
1783 012702 104400              4$: SCOPE                ;SCOPE THIS TEST

```

```

1784
1785
1786                                     ;***** TEST 5 *****
1787                                     ;*CONTROL STATUS REGISTER WRITE/READ TEST
1788                                     ;*SET BIT1, VERIFY BIT1 WAS SET
1789                                     ;*CLEAR BIT1, VERIFY BIT1 WAS CLEARED
1790                                     ;*****
1791

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1792                                     ; TEST 5
1793                                     ;-----

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1794 012704 012737 000005 001226  TST5: MOV    #5,TSTNO
1795 012712 012737 013002 001216      MOV    #TST6,NEXT
1796 012720 012737 012730 001220      MOV    #1$,LOCK
1797 012726 104412              MSTCLR                      ;MASTER CLEAR DMC11
1798 012730 013701 001404              1$: MOV    DMCSR,R1        ;PUT REGISTER ADDRESS IN R1
1799 012734 012705 000002              MOV    #BIT1,R5          ;PUT DATA IN "EXPECTED"
1800 012740 010511              MOV    R5,(R1)          ;WRITE BIT 1
1801 012742 011104              MOV    (R1),R4          ;READ CONTROL STATUS REGISTER
1802 012744 020504              CMP    R5,R4            ;IS DATA CORRECT
1803 012746 001401              BEQ    2$             ;BR IF YES
1804 012750 104002              HLT    2              ;DATA ERROR
1805 012752 104401              2$: SCOPI                ;SW09 UP?
1806 012754 012737 012762 001220      MOV    #3$,LOCK          ;NEW SCOPI
1807 012762 042711 000002              3$: BIC    #BIT1,(R1)    ;CLEAR BIT 1
1808 012766 005005              CLR    R5              ;CLEAR "EXPECTED"
1809 012770 011104              MOV    (R1),R4          ;READ CONTROL STATUS REGISTER
1810 012772 001402              BEQ    4$             ;BR IF ZERO
1811 012774 104002              HLT    2              ;DATA ERROR BIT1 NOT CLEARED
1812 012776 104401              SCOPI                      ;SW09 UP?
1813 013000 104400              4$: SCOPE                ;SCOPE THIS TEST

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1816                                     ;***** TEST 6 *****
1817                                     ;*CONTROL STATUS REGISTER WRITE/READ TEST
1818                                     ;*SET BIT2, VERIFY BIT2 WAS SET
1819                                     ;*CLEAR BIT2, VERIFY BIT2 WAS CLEARED
1820                                     ;*****
1821

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1822                                     ; TEST 6
1823                                     ;-----

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1824 013002 012737 000006 001226  TST6: MOV    #6,TSTNO
1825 013010 012737 013100 001216      MOV    #TST7,NEXT
1826 013016 012737 013026 001220      MOV    #1$,LOCK
1827 013024 104412              MSTCLR                      ;MASTER CLEAR DMC11
1828 013026 013701 001404              1$: MOV    DMCSR,R1        ;PUT REGISTER ADDRESS IN R1
1829 013032 012705 000004              MOV    #BIT2,R5          ;PUT DATA IN "EXPECTED"
1830 013036 010511              MOV    R5,(R1)          ;WRITE BIT 2
1831 013040 011104              MOV    (R1),R4          ;READ CONTROL STATUS REGISTER
1832 013042 020504              CMP    R5,R4            ;IS DATA CORRECT

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1833 013044 001401          BEQ      2$          ;BR IF YES
1834 013046 104002          HLT      2          ;DATA ERROR
1835 013050 104401          2$:     SCOPI       ;SW09 UP?
1836 013052 012737 013060 001220  MOV     #3$,LOCK   ;NEW SCOPI
1837 013060 042711 000004          3$:     BIC     #BIT2,(R1) ;CLEAR BIT 2
1838 013064 005005          CLR      R5        ;CLEAR "EXPECTED"
1839 013066 011104          MOV     (R1),R4    ;READ CONTROL STATUS REGISTER
1840 013070 001402          BEQ     4$          ;BR IF ZERO
1841 013072 104002          HLT     2          ;DATA ERROR BIT2 NOT CLEARED
1842 013074 104401          SCOPI              ;SW09 UP?
1843 013076 104400          4$:     SCOPE              ;SCOPE THIS TEST
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1854 013100 012737 000007 001226  TST7:  MOV     #7,TSTNO
1855 013106 012737 013176 001216  MOV     #TST10,NEXT
1856 013114 012737 013124 001220  MOV     #1$,LOCK
1857 013122 104412          MSTCLR
1858 013124 013701 001404          1$:     MOV     DMCSR,R1 ;MASTER CLEAR DMC11
1859 013130 012705 000040          MOV     #BIT5,R5   ;PUT REGISTER ADDRESS IN R1
1860 013134 010511          MOV     R5,(R1)    ;PUT DATA IN "EXPECTED"
1861 013136 011104          MOV     (R1),R4    ;WRITE BIT 5
1862 013140 020504          CMP     R5,R4      ;READ CONTROL STATUS REGISTER
1863 013142 001401          BEQ     2$          ;IS DATA CORRECT
1864 013144 104002          HLT     2          ;BR IF YES
1865 013146 104401          2$:     SCOPI       ;DATA ERROR
1866 013150 012737 013156 001220  MOV     #3$,LOCK   ;SW09 UP?
1867 013156 042711 000040          3$:     BIC     #BIT5,(R1) ;NEW SCOPI
1868 013162 005005          CLR     R5        ;CLEAR BIT 5
1869 013164 011104          MOV     (R1),R4    ;CLEAR "EXPECTED"
1870 013166 001402          BEQ     4$          ;READ CONTROL STATUS REGISTER
1871 013170 104002          HLT     2          ;BR IF ZERO
1872 013172 104401          SCOPI              ;DATA ERROR BITS NOT CLEARED
1873 013174 104400          4$:     SCOPE              ;SW09 UP?
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1884 013176 012737 000010 001226  TST10: MOV     #10,TSTNO
1885 013204 012737 013274 001216  MOV     #TST11,NEXT
1886 013212 012737 013222 001220  MOV     #1$,LOCK
1887 013220 104412          MSTCLR
1888 013222 013701 001404          1$:     MOV     DMCSR,R1 ;MASTER CLEAR DMC11

```

```

;***** TEST *****
;CONTROL STATUS REGISTER WRITE/READ TEST
;SET BITS, VERIFY BITS WAS SET
;CLEAR BITS, VERIFY BITS WAS CLEARED
;*****

```

```

; TEST 7
-----

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;***** TEST 10 *****
;CONTROL STATUS REGISTER WRITE/READ TEST
;SET BIT6, VERIFY BIT6 WAS SET
;CLEAR BIT6, VERIFY BIT6 WAS CLEARED
;*****

```

```

; TEST 10
-----

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DMC11 UNIBUS REGISTER TESTS

```

1889 013226 012705 000100      MOV      #BIT6,R5      ;PUT DATA IN "EXPECTED"
1890 013232 010511      MOV      R5,(R1)      ;WRITE BIT 6
1891 013234 011104      MOV      (R1),R4      ;READ CONTROL STATUS REGISTER
1892 013236 020504      CMP      R5,R4        ;IS DATA CORPECT
1893 013240 001401      BEQ      2$           ;BR IF YES
1894 013242 104002      HLT      2           ;DATA ERROR
1895 013244 104401      HLT      2           ;SW09 UP?
1896 013246 012737 013254 001220 2$: SCOPI      ;NEW SCOPI
1897 013254 042711 000100 3$: BIC      #BIT6,(R1)  ;CLEAR BIT 6
1898 013260 005005      CLR      R5          ;CLEAR "EXPECTED"
1899 013262 011104      MOV      (R1),R4      ;READ CONTROL STATUS REGISTER
1900 013264 000002      BEQ      4$           ;BR IF ZERO
1901 013266 104002      HLT      2           ;DATA ERROR BIT6 NOT CLEARED
1902 013270 104401      SCOPI      ;SW09 UP?
1903 013272 104400 4$: SCOPE      ;SCOPE THIS TEST
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1914 013274 012737 000011 001226 TST11: MOV      #11,TSTNO
1915 013302 012737 013372 001216      MOV      #TST12,NEXT
1916 013310 012737 013320 001220      MOV      #15,LOCK
1917 013316 104412      MSTCLR      ;MASTER CLEAR DMC11
1918 013320 013701 001404 1$: MOV      DMCSR,R1  ;PUT REGISTER ADDRESS IN R1
1919 013324 012705 000200      MOV      #BIT7,R5    ;PUT DATA IN "EXPECTED"
1920 013330 010511      MOV      R5,(R1)    ;WRITE BIT 7
1921 013332 011104      MOV      (R1),R4    ;READ CONTROL STATUS REGISTER
1922 013334 020504      CMP      R5,R4      ;IS DATA CORRECT
1923 013336 001401      BEQ      2$         ;BR IF YES
1924 013340 104002      HLT      2         ;DATA ERROR
1925 013342 104401      HLT      2         ;SW09 UP?
1926 013344 012737 013352 001220 2$: SCOPI      ;NEW SCOPI
1927 013352 042711 000200 3$: BIC      #BIT7,(R1)  ;CLEAR BIT 7
1928 013356 005005      CLR      R5          ;CLEAR "EXPECTED"
1929 013360 011104      MOV      (R1),R4    ;READ CONTROL STATUS REGISTER
1930 013362 001402      BEQ      4$         ;BR IF ZERO
1931 013364 104002      HLT      2         ;DATA ERROR BIT7 NOT CLEARED
1932 013366 104401      SCOPI      ;SW09 UP?
1933 013370 104400 4$: SCOPE      ;SCOPE THIS TEST
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1944 013372 012737 000012 001226 TST12: MOV      #12,TSTNO

```

;***** TEST 11 *****
;*CONTROL STATUS REGISTER WRITE/READ TEST
;*SET BIT7, VERIFY BIT7 WAS SET
;*CLEAR BIT7, VERIFY BIT7 WAS CLEARED
;*****
: TEST 11

;***** TEST 12 *****
;*CONTROL STATUS REGISTER WRITE/READ TEST
;*SET BIT9, VERIFY BIT9 WAS SET
;*CLEAR BIT9, VERIFY BIT9 WAS CLEARED
;*****
: TEST 12

DMC11 UNIBUS REGISTER TESTS

1945	013400	012737	013470	001216
1946	013406	012737	013416	001220
1947	013414	104412		
1948	013416	013701	001404	
1949	013422	012705	001000	
1950	013426	010511		
1951	013430	011104		
1952	013432	020504		
1953	013434	001401		
1954	013436	104002		
1955	013440	104401		
1956	013442	012737	013450	001220
1957	013450	042711	001000	
1958	013454	005005		
1959	013456	011104		
1960	013460	001402		
1961	013462	104002		
1962	013464	104401		
1963	013466	104400		

```

MOV      #TST13,NEXT
MOV      #15,LOCK
MSTCLR
1$:      MOV      DMCSR,R1
         MOV      #BIT9,R5
         MOV      R5,(R1)
         MOV      (R1),R4
         CMP      R5,R4
         BEQ      2$
         HLT      2
2$:      SCOPE1
         MOV      #3$,LOCK
3$:      BIC      #BIT9,(R1)
         CLR      R5
         MOV      (R1),R4
         BEQ      4$
         HLT      2
4$:      SCOPE1
         SCOPE

```

```

;MASTER CLEAR DMC11
;PUT REGISTER ADDRESS IN R1
;PUT DATA IN "EXPECTED"
;WRITE BIT 9
;READ CONTROL STATUS REGISTER
;IS DATA CORRECT
;BR IF YES
;DATA ERROR
;SW09 UP?
;NEW SCOPE1
;CLEAR BIT 9
;CLEAR "EXPECTED"
;READ CONTROL STATUS REGISTER
;BR IF ZERO
;DATA ERROR BIT9 NOT CLEARED
;SW09 UP?
;SCOPE THIS TEST

```

```

;***** TEST 13 *****
;CONTROL STATUS REGISTER WRITE/READ TEST
;SET BIT11, VERIFY BIT11 WAS SET
;CLEAR BIT11, VERIFY BIT11 WAS CLEARED
;*****

```

TEST 13

1974	013470	012737	006013	001226
1975	013476	012737	013566	001216
1976	013504	012737	013514	001220
1977	013512	104412		
1978	013514	013701	001404	
1979	013520	012705	004000	
1980	013524	010511		
1981	013526	011104		
1982	013530	020504		
1983	013532	001401		
1984	013534	104002		
1985	013536	104401		
1986	013540	012737	013546	001220
1987	013546	042711	004000	
1988	013552	005005		
1989	013554	011104		
1990	013556	001402		
1991	013560	104002		
1992	013562	104401		
1993	013564	104400		

```

TST13:  MOV      #13,TSTNO
         MOV      #TST14,NEXT
         MOV      #15,LOCK
MSTCLR
1$:      MOV      DMCSR,R1
         MOV      #BIT11,R5
         MOV      R5,(R1)
         MOV      (R1),R4
         CMP      R5,R4
         BEQ      2$
         HLT      2
2$:      SCOPE1
         MOV      #3$,LOCK
3$:      BIC      #BIT11,(R1)
         CLR      R5
         MOV      (R1),R4
         BEQ      4$
         HLT      2
4$:      SCOPE1
         SCOPE

```

```

;MASTER CLEAR DMC11
;PUT REGISTER ADDRESS IN R1
;PUT DATA IN "EXPECTED"
;WRITE BIT 11
;READ CONTROL STATUS REGISTER
;IS DATA CORRECT
;BR IF YES
;DATA ERROR
;SW09 UP?
;NEW SCOPE1
;CLEAR BIT 11
;CLEAR "EXPECTED"
;READ CONTROL STATUS REGISTER
;BR IF ZERO
;DATA ERROR BIT11 NOT CLEARED
;SW09 UP?
;SCOPE THIS TEST

```

```

;***** TEST 14 *****
;CONTROL STATUS REGISTER WRITE/READ TEST
;SET BIT12, VERIFY BIT12 WAS SET
;CLEAR BIT12, VERIFY BIT12 WAS CLEARED
;*****

```

1994
1995
1996
1997
1998
1999
2000

```

2001
2002
2003
2004 013566 012737 000014 001226
2005 013574 012737 013664 001216
2006 013602 012737 013612 001220
2007 013610 104412
2008 013612 013701 001404
2009 013616 012705 010000
2010 013622 010511
2011 013624 011104
2012 013626 020504
2013 013630 001401
2014 013632 104002
2015 013634 104401
2016 013636 012737 013644 001220
2017 013644 042711 010000
2018 013650 005005
2019 013652 011104
2020 013654 001402
2021 013656 104002
2022 013660 104401
2023 013662 104400

```

```

; TEST 14
-----
TST14: MOV #14,TSTNO
MOV #TST15,NEXT
MOV #15,LOCK
MSTCLR
1$: MOV DMCSR,R1 ; MASTER CLEAR DMC11
MOV #BIT12,R5 ; PUT REGISTER ADDRESS IN R1
MOV R5,(R1) ; PUT DATA IN "EXPECTED"
MOV (R1),R4 ; WRITE BIT 12
CMP R5,R4 ; READ CONTROL STATUS REGISTER
BEQ 2$ ; IS DATA CORRECT
HLT 2 ; BR IF YES
; DATA ERROR
; SW09 UP?
2$: SCOPE1
MOV #3$,LOCK ; NEW SCOPE1
3$: BIC #BIT12,(R1) ; CLEAR BIT 12
CLR R5 ; CLEAR "EXPECTED"
MOV (R1),R4 ; READ CONTROL STATUS REGISTER
BEQ 4$ ; BR IF ZERO
HLT 2 ; DATA ERROR BIT12 NOT CLEARED
; SW09 UP?
4$: SCOPE ; SCOPE THIS TEST

```

```

;***** TEST 15 *****
; *CONTROL OUT REGISTER WRITE/READ TEST
; *SET BIT0, VERIFY BIT0 WAS SET
; *CLEAR BIT0, VERIFY BIT0 WAS CLEARED
;*****

```

```

2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034 013664 012737 000015 001226
2035 013672 012737 013762 001216
2036 013700 012737 013710 001220
2037 013706 104412
2038 013710 013701 001410
2039 013714 012705 000001
2040 013720 010511
2041 013722 011104
2042 013724 020504
2043 013726 001401
2044 013730 104002
2045 013732 104401
2046 013734 012737 013742 001220
2047 013742 042711 000001
2048 013746 005005
2049 013750 011104
2050 013752 001402
2051 013754 104002
2052 013756 104401
2053 013760 104400

```

```

; TEST 15
-----
TST15: MOV #15,TSTNO
MOV #TST16,NEXT
MOV #15,LOCK
MSTCLR
1$: MOV DMCTL,R1 ; MASTER CLEAR DMC11
MOV #BIT0,R5 ; PUT REGISTER ADDRESS IN R1
MOV R5,(R1) ; PUT DATA IN "EXPECTED"
MOV (R1),R4 ; WRITE BIT 0
CMP R5,R4 ; READ CONTROL OUT REGISTER
BEQ 2$ ; IS DATA CORRECT
HLT 2 ; BR IF YES
; DATA ERROR
; SW09 UP?
2$: SCOPE1
MOV #0$,LOCK ; NEW SCOPE1
3$: BIC #BIT0,(R1) ; CLEAR BIT 0
CLR R5 ; CLEAR "EXPECTED"
MOV (R1),R4 ; READ CONTROL OUT REGISTER
BEQ 4$ ; BR IF ZERO
HLT 2 ; DATA ERROR BIT0 NOT CLEARED
; SW09 UP?
4$: SCOPE ; SCOPE THIS TEST

```

```

;***** TEST 16 *****

```

```

2054
2055
2056

```



```

2057 : *CONTROL OUT REGISTER WRITE/READ TEST
2058 : *SET BIT1, VERIFY BIT1 WAS SET
2059 : *CLEAR BIT1, VERIFY BIT1 WAS CLEARED
2060 : *****

```

```

2061 :
2062 : TEST 16
2063 : -----
2064 013762 012737 000016 001226 TST16: MOV #16,TSTNO
2065 013770 012737 014060 001216 MOV #TST17,NEXT
2066 013776 012737 014006 001220 MOV #15,LOCK
2067 014004 104412 MSTCLR ; MASTER CLEAR DMC11
2068 014006 013701 001410 1S: MOV DMCTL,R1 ; PUT REGISTER ADDRESS IN R1
2069 014012 012705 000002 MOV #BIT1,R5 ; PUT DATA IN "EXPECTED"
2070 014016 010511 MOV R5,(R1) ; WRITE BIT 1
2071 014020 011104 MOV (R1),R4 ; READ CONTROL OUT REGISTER
2072 014022 020504 CMP R5,R4 ; IS DATA CORRECT
2073 014024 001401 BEQ 2S ; BR IF YES
2074 014026 104002 HLT 2 ; DATA ERROR
2075 014030 104401 2S: SCOPI ; SW09 UP?
2076 014032 012737 014040 001220 MOV #3S,LOCK ; NEW SCOPI
2077 014040 042711 000002 3S: BIC #BIT1,(R1) ; CLEAR BIT 1
2078 014044 005005 CLR R5 ; CLEAR "EXPECTED"
2079 014046 011104 MOV (R1),R4 ; READ CONTROL OUT REGISTER
2080 014050 001402 BEQ 4S ; BR IF ZERO
2081 014052 104002 HLT 2 ; DATA ERROR BIT1 NOT CLEARED
2082 014054 104401 4S: SCOPI ; SW09 UP?
2083 014056 104400 SCOPE ; SCOPE THIS TEST
2084
2085
2086 : ***** TEST 17 *****
2087 : *CONTROL OUT REGISTER WRITE/READ TEST
2088 : *SET BIT2, VERIFY BIT2 WAS SET
2089 : *CLEAR BIT2, VERIFY BIT2 WAS CLEARED
2090 : *****

```

```

2091 :
2092 : TEST 17
2093 : -----
2094 014060 012737 000017 001226 TST17: MOV #17,TSTNO
2095 014066 012737 014156 001216 MOV #TST20,NEXT
2096 014074 012737 014104 001220 MOV #15,LOCK
2097 014102 104412 MSTCLR ; MASTER CLEAR DMC11
2098 014104 013701 001410 1S: MOV DMCTL,R1 ; PUT REGISTER ADDRESS IN R1
2099 014110 012705 000004 MOV #BIT2,R5 ; PUT DATA IN "EXPECTED"
2100 014114 010511 MOV R5,(R1) ; WRITE BIT 2
2101 014116 011104 MOV (R1),R4 ; READ CONTROL OUT REGISTER
2102 014120 020504 CMP R5,R4 ; IS DATA CORRECT
2103 014122 001401 BEQ 2S ; BR IF YES
2104 014124 104002 HLT 2 ; DATA ERROR
2105 014126 104401 2S: SCOPI ; SW09 UP?
2106 014130 012737 014136 001220 MOV #3S,LOCK ; NEW SCOPI
2107 014136 042711 000004 3S: BIC #BIT2,(R1) ; CLEAR BIT 2
2108 014142 005005 CLR R5 ; CLEAR "EXPECTED"
2109 014144 011104 MOV (R1),R4 ; READ CONTROL OUT REGISTER
2110 014146 001402 BEQ 4S ; BR IF ZERO
2111 014150 104002 HLT 2 ; DATA ERROR BIT2 NOT CLEARED
2112 014152 104401 SCOPI ; SW09 UP?

```

```

2113 014154 104400          4$: SCOPE ;SCOPE THIS TEST
2114
2115
2116 ;***** TEST 20 *****
2117 ;*CONTROL OUT REGISTER WRITE/READ TEST
2118 ;*SET BIT6, VERIFY BIT6 WAS SET
2119 ;*CLEAR BIT6, VERIFY BIT6 WAS CLEARED
2120 ;*****
2121
2122 ; TEST 20
2123 ;-----
2124 014156 012737 000020 001226 TST20: MOV #20,TSTNO
2125 014164 012737 014254 001216 MOV #TST21,NEXT
2126 014172 012737 014202 001220 MOV #1$,LOCK
2127 014200 104412 MSTCLR ;MASTER CLEAR DMC11
2128 014202 013701 001410 1$: MOV DMCTL,R1 ;PUT REGISTER ADDRESS IN R1
2129 014206 012705 000100 MOV #BIT6,R5 ;PUT DATA IN "EXPECTED"
2130 014212 010511 MOV R5,(R1) ;WRITE BIT 6
2131 014214 011104 MOV (R1),R4 ;READ CONTROL OUT REGISTER
2132 014216 020504 CMP R5,R4 ;IS DATA CORRECT
2133 014220 001401 BEQ 2$ ;BR IF YES
2134 014222 104002 HLT 2 ;DATA ERROR
2135 014224 104401 2$: SCOPI ;SW09 UP?
2136 014226 012737 014234 001220 MOV #3$,LOCK ;NEW SCOPI
2137 014234 042711 000100 3$: BIC #BIT6,(R1) ;CLEAR BIT 6
2138 014240 005005 CLR R5 ;CLEAR "EXPECTED"
2139 014242 011104 MOV (R1),R4 ;READ CONTROL OUT REGISTER
2140 014244 001402 BEQ 4$ ;BR IF ZERO
2141 014246 104002 HLT 2 ;DATA ERROR BIT6 NOT CLEARED
2142 014250 104401 4$: SCOPI ;SW09 UP?
2143 014252 104400 SCOPE ;SCOPE THIS TEST
2144
2145
2146 ;***** TEST 21 *****
2147 ;*CONTROL OUT REGISTER WRITE/READ TEST
2148 ;*SET BIT7, VERIFY BIT7 WAS SET
2149 ;*CLEAR BIT7, VERIFY BIT7 WAS CLEARED
2150 ;*****
2151
2152 ; TEST 21
2153 ;-----
2154 014254 012737 000021 001226 TST21: MOV #21,TSTNO
2155 014262 012737 014352 001216 MOV #TST22,NEXT
2156 014270 012737 014300 001220 MOV #1$,LOCK
2157 014276 104412 MSTCLR ;MASTER CLEAR DMC11
2158 014300 013701 001410 1$: MOV DMCTL,R1 ;PUT REGISTER ADDRESS IN R1
2159 014304 012705 000200 MOV #BIT7,R5 ;PUT DATA IN "EXPECTED"
2160 014310 010511 MOV R5,(R1) ;WRITE BIT 7
2161 014312 011104 MOV (R1),R4 ;READ CONTROL OUT REGISTER
2162 014314 020504 CMP R5,R4 ;IS DATA CORRECT
2163 014316 001401 BEQ 2$ ;BR IF YES
2164 014320 104002 HLT 2 ;DATA ERROR
2165 014322 104401 2$: SCOPI ;SW09 UP?
2166 014324 012737 014332 001220 MOV #3$,LOCK ;NEW SCOPI
2167 014332 042711 000200 3$: BIC #BIT7,(R1) ;CLEAR BIT 7
2168 014336 005005 CLR R5 ;CLEAR "EXPECTED"

```

```

2169 014340 011104      MOV      (R1),R4      ;READ CONTROL OUT REGISTER
2170 014342 001402      BEQ      4$          ;BR IF ZERO
2171 014344 104002      HLT      2          ;DATA ERROR BIT7 NOT CLEARED
2172 014346 104401      SCOPI    ;SW09 UP?
2173 014350 104400      4$:      SCOPE      ;SCOPE THIS TEST
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184 014352 012737 000022 001226      TST22:  MOV      #22,TSTNO
2185 014360 012737 014450 001216      MOV      #TST23,NEXT
2186 014366 012737 014376 001220      MOV      #1$,LOCK
2187 014374 104412      MSTCLR   ;MASTER CLEAR DMC11
2188 014376 013701 001410      1$:      MOV      DMCTL,R1  ;PUT REGISTER ADDRESS IN R1
2189 014402 012705 010000      MOV      #BIT12,R5  ;PUT DATA IN "EXPECTED"
2190 014406 010511      MOV      R5,(R1)    ;WRITE BIT 12
2191 014410 011104      MOV      (R1),R4    ;READ CONTROL OUT REGISTER
2192 014412 020504      CMP      R5,R4      ;IS DATA CORRECT
2193 014414 001401      BEQ      2$          ;BR IF YES
2194 014416 104002      HLT      2          ;DATA ERROR
2195 014420 104401      2$:      SCOPI    ;SW09 UP?
2196 014422 012737 014430 001220      MOV      #3$,LOCK  ;NEW SCOPI
2197 014430 042711 010000      3$:      BIC      #BIT12,(R1);CLEAR BIT 12
2198 014434 005005      CLR      R5         ;CLEAR "EXPECTED"
2199 014436 011104      MOV      (R1),R4    ;READ CONTROL OUT REGISTER
2200 014440 001402      BEQ      4$          ;BR IF ZERO
2201 014442 104002      HLT      2          ;DATA ERROR BIT12 NOT CLEARED
2202 014444 104401      SCOPI    ;SW09 UP?
2203 014446 104400      4$:      SCOPE      ;SCOPE THIS TEST
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214 014450 012737 000023 001226      TST23:  MOV      #23,TSTNO
2215 014456 012737 014546 001216      MOV      #TST24,NEXT
2216 014464 012737 014474 001220      MOV      #1$,LOCK
2217 014472 104412      MSTCLR   ;MASTER CLEAR DMC11
2218 014474 013701 001410      1$:      MOV      DMCTL,R1  ;PUT REGISTER ADDRESS IN R1
2219 014500 012705 020000      MOV      #BIT13,R5  ;PUT DATA IN "EXPECTED"
2220 014504 010511      MOV      R5,(R1)    ;WRITE BIT 13
2221 014506 011104      MOV      (R1),R4    ;READ CONTROL OUT REGISTER
2222 014510 020504      CMP      R5,R4      ;IS DATA CORRECT
2223 014512 001401      BEQ      2$          ;BR IF YES
2224 014514 104002      HLT      2          ;DATA ERROR

```



```

2225 014516 104401          2$: SCOP1          ;SW09 UP?
2226 014520 012737 014526 001220  MOV          #3$,LOCK ;NEW SCOP1
2227 014526 042711 020000 3$: BIC          #BIT13,(R1) ;CLEAR BIT 13
2228 014532 005005          CLR          R5          ;CLEAR "EXPECTED"
2229 014534 011104          MOV          (R1),R4      ;READ CONTROL OUT REGISTER
2230 014536 001402          BEQ          4$          ;BR IF ZERO
2231 014540 104002          HLT          2          ;DATA ERROR BIT13 NOT CLEARED
2232 014542 104401          SCOP1          ;SW09 UP?
2233 014544 104400          4$: SCOPE          ;SCOPE THIS TEST
2234
2235
2236
2237
2238
2239
2240
2241
2242
2243
2244 014546 012737 000024 001226  TST24: MOV          #24,TSTNO
2245 014554 012737 014672 001216  MOV          #TST25,NEXT
2246 014562 012737 014602 001220  MOV          #64$,LOCK
2247 014570 104412          MSTCLR          ;MASTER CLEAR DMC11
2248 014572 013701 001412          MOV          DMP04,R1      ;PUT REGISTER ADDRESS IN R1
2249 014576 012700 000001          MOV          #1,R0          ;START WITH BIT0
2250 014602
2251 014602 010005          64$: MOV          R0,R5          ;PUT "EXPECTED" IN R5
2252 014604 010511          MOV          R5,(R1)      ;WRITE PORT4 REGISTER
2253 014606 011104          MOV          (R1),R4      ;READ PORT4 REGISTER
2254 014610 020504          CMP          R5,R4          ;COMPARE EXPECTED AND FOUND
2255 014612 001401          BEQ          65$          ;BR IF OK
2256 014614 104002          HLT          2          ;WRITE/READ ERROR
2257 014616 104401          65$: SCOP1          ;LOOP TO 64$ IF SW09=1
2258 014620 000241          CLC          ;CLEAR CARRY
2259 014622 006100          ROL          R0          ;SHIFT TO NEXT BIT
2260 014624 001366          BNE          64$          ;BR IF NOT DONE YET
2261 014626 012737 014640 001220  MOV          #66$,LOCK      ;NEW SCOP1
2262 014634 012700 000001          MOV          #1,R0          ;START WITH BIT0
2263 014640
2264 014640 005100          66$: COM          R0          ;CHANGE TO A FLOATING ZERO
2265 014642 010005          MOV          R0,R5          ;PUT "EXPECTED" IN R5
2266 014644 010511          MOV          R5,(R1)      ;WRITE PORT4 REGISTER
2267 014646 011104          MOV          (R1),R4      ;READ PORT4 REGISTER
2268 014650 020504          CMP          R5,R4          ;COMPARE EXPECTED AND FOUND
2269 014652 001401          BEQ          67$          ;BR IF OK
2270 014654 104002          HLT          2          ;WRITE/READ ERROR
2271 014656 104401          67$: SCOP1          ;LOOP TO 66$ IF SW09=1
2272 014660 005100          COM          R0          ;CHANGE BACK TO A FLOATING ONE
2273 014662 000241          CLC          ;CLEAR CARRY
2274 014664 006100          ROL          R0          ;SHIFT TO NEXT BIT
2275 014666 001364          BNE          66$          ;BR IF NOT DONE YET
2276 014670 104400          SCOPE          ;SCOPE THIS TEST
2277
2278
2279
2280
;***** TEST 25 *****
;*PORT6 REGISTER WRITE/READ TEST

```

DMC11 UNIBUS REGISTER TESTS

```

2281 ;*FLOAT A ONE THROUGH PORT6 REGISTER
2282 ;*FLOAT A ZERO THROUGH PORT6 REGISTER
2283 ;:*****
2284
2285 ; TEST 25
2286 -----
2287 014672 012737 000025 001226 TST25: MOV #25,TSTNO
2288 014700 012737 015016 001216 MOV #TST26,NEXT
2289 014706 012737 014726 001220 MOV #64$,LOCK
2290 014714 104412 MSTCLR ;MASTER CLEAR DMC11
2291 014716 013701 001414 MOV DMP06,R1 ;PUT REGISTER ADDRESS IN R1
2292 014722 012700 000001 MOV #1,R0 ;START WITH BIT0
2293 014726 64$:
2294 014726 010005 MOV R0,R5 ;PUT "EXPECTED" IN R5
2295 014730 010511 MOV R5,(R1) ;WRITE PORT6 REGISTER
2296 014732 011104 MOV (R1),R4 ;READ PORT6 REGISTER
2297 014734 020504 CMP R5,R4 ;COMPARE EXPECTED AND FOUND
2298 014736 001401 BEQ 65$ ;BR IF OK
2299 014740 104002 HLT 2 ;WRITE/READ ERROR
2300 014742 104401 65$: SCOPI ;LOOP TO 64$ IF SW09=1
2301 014744 000241 CLC ;CLEAR CARRY
2302 014746 006100 ROL R0 ;SHIFT TO NEXT BIT
2303 014750 001366 BNE 64$ ;BR IF NOT DONE YET
2304 014752 012737 014764 001220 MOV #66$,LOCK ;NEW SCOPI
2305 014760 012700 000001 MOV #1,R0 ;START WITH BIT0
2306 014764 66$:
2307 014764 005100 COM R0 ;CHANGE TO A FLOATING ZERO
2308 014766 010005 MOV R0,R5 ;PUT "EXPECTED" IN R5
2309 014770 010511 MOV R5,(R1) ;WRITE PORT6 REGISTER
2310 014772 011104 MOV (R1),R4 ;READ PORT6 REGISTER
2311 014774 020504 CMP R5,R4 ;COMPARE EXPECTED AND FOUND
2312 014776 001401 BEQ 67$ ;BR IF OK
2313 015000 104002 HLT 2 ;WRITE/READ ERROR
2314 015002 104401 67$: SCOPI ;LOOP TO 66$ IF SW09=1
2315 015004 005100 COM R0 ;CHANGE BACK TO A FLOATING ONE
2316 015006 000241 CLC ;CLEAR CARRY
2317 015010 006100 ROL R0 ;SHIFT TO NEXT BIT
2318 015012 001364 BNE 66$ ;BR IF NOT DONE YET
2319 015014 104400 SCOPE ;SCOPE THIS TEST
2320
2321 ;***** TEST 26 *****
2322 ;*UNIBUS REGISTER BYTE DUAL ADDRESSING TEST
2323 ;*LOAD ALL REGISTERS WITH INCREMENTING PATTERN
2324 ;*READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING
2325 ;:*****
2326
2327 ; TEST 26
2328 -----
2329
2330 015016 012737 000026 001226 TST26: MOV #26,TSTNO
2331 015024 012737 015146 001216 MOV #TST27,NEXT
2332 015032 012737 015046 001220 MOV #1$,LOCK
2333
2334 015040 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
2335 015042 012700 000001 MOV #1,R0 ;MASTER CLEAR DMC11
2336 015046 105011 1$: CLR R1 ;START PATTERN AT 1
;CLEAR REGISTER

```

DMC11 UNIBUS REGISTER TESTS

2337	015050	110005				MOV B	R0,R5		;PUT DATA IN "EXPECTED"
2338	015052	110011				MOV B	R0,(R1)		;WRITE DMC REGISTER WITH PATTERN
2339	015054	111104				MOV B	(R1),R4		;READ DMC REGISTER INTO "FOUND"
2340	015056	020504				CMP	R5,R4		;IS DATA CORRECT
2341	015060	001401				BEQ	2\$;BR IF YES
2342	015062	104002				HLT	2		;DATA ERROR
2343	015064	104401			2\$:	SCOPI			;SW09=1?
2344	015066	105721				TST B	(R1)+		;NEXT REGISTER
2345	015070	005200				INC	R0		;INCREMENT DATA PATTERN
2346	015072	022700	000011			CMP	#11,R0		;LAST REGISTER?
2347	015076	001363				BNE	1\$;BR IF NO
2348	015100	013701	001404			MOV	DMCSR,R1		;BASE DMC11 ADDRESS TO R1
2349	015104	012700	000001			MOV	#1,R0		;RESTART PATTERN AT 1
2350	015110	012737	015116	001220		MOV	#3\$,LOCK		;NEW SCOPI
2351	015116	110005			3\$:	MOV B	R0,R5		;PUT DATA IN "EXPECTED"
2352	015120	111104				MOV B	(R1),R4		;READ DMC REGISTER INTO "FOUND"
2353	015122	020504				CMP	R5,R4		;IS DATA CORRECT
2354	015124	001401				BEQ	4\$;BR IF YES
2355	015126	104002				HLT	2		;DUAL ADDRESSING ERROR
2356	015130	104401			4\$:	SCOPI			;SW09=1?
2357	015132	105721				TST B	(R1)+		;NEXT REGISTER
2358	015134	005200				INC	R0		;INCREMENT PATTERN
2359	015136	022700	000011			CMP	#11,R0		;LAST REGISTER?
2360	015142	001365				BNE	3\$;BR IF NO
2361	015144	104400				SCOPE			;SCOPE THIS TEST

```

:***** TEST 27 *****
: *MAINTENANCE INSTRUCTION REGISTER TEST
: *VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS
: *AND ALL ONES. VERIFY THAT IT IS CLEARED ON A BUS RESET.
:*****

```

; TEST 27

2372	015146	012737	000027	001226		TST27:	MOV	#27,TSTNO		
2373	015154	012737	015306	001216			MOV	#TST30,NEXT		
2374	015162	012737	015200	001220			MOV	#1\$,LOCK		
2375										
2376	015170	104412				MSTCLR				;R1 CONTAINS BASE DMC11 ADDRESS
2377	015172	012711	003000			MOV	#BIT9:BIT10,(R1)			;MASTER CLEAR DMC11
2378	015176	005005				CLR	R5			;SEL6 IS NOW THE IR
2379	015200	010561	000006		1\$:	MOV	R5,6(R1)			;PUT "EXPECTED" IN R5
2380	015204	016104	000006			MOV	6(R1),R4			;CLEAR THE IR
2381	015210	020504				CMP	R5,R4			;READ THE IR
2382	015212	001401				BEQ	2\$;IS IT CLEARED?
2383	015214	104023				HLT	23			;BR IF YES
2384	015216	104401			2\$:	SCOPI				;ERROR IR IS NOT CLEAR
2385	015220	012737	015232	001220		MOV	#3\$,LOCK			;LOOP TO 1\$ IF SW09=1
2386	015226	012705	177777			MOV	#-1,R5			;NEW SCOPI
2387	015232	010561	000006		3\$:	MOV	R5,6(R1)			;PUT "EXPECTED" IN R5
2388	015236	016104	000006			MOV	6(R1),R4			;WRITE ALL ONES TO THE IR
2389	015242	020504				CMP	R5,R4			;READ THE IR
2390	015244	001401				BEQ	4\$;IS IT ALL ONES?
2391	015246	104023				HLT	23			;BR IF YES
2392	015250	104401			4\$:	SCOPI				;ERROR IR IS NOT = ALL ONES

;LOOP TO 3\$ IF SW09=1

DMC11 UNIBUS REGISTER TESTS

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2393 015252 012737 015262 001220
2394 015260 005005
2395 015262 000005
2396 015264 012711 003000
2397 015270 016104 000006
2398 015274 020504
2399 015276 001401
2400 015300 104023
2401 015302 104401
2402 015304 104400
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2413 015306 012737 000030 001226
2414 015314 012737 015450 001216
2415 015322 012737 015340 001220
2416
2417 015330 104412
2418 015332 012711 003000
2419 015336 005005
2420 015340 010561 000006
2421 015344 016104 000006
2422 015350 020504
2423 015352 001401
2424 015354 104023
2425 015356 104401
2426 015360 012737 015372 001220
2427 015366 012705 177777
2428 015372 010561 000006
2429 015376 016104 000006
2430 015402 020504
2431 015404 001401
2432 015406 104023
2433 015410 104401
2434 015412 012737 015422 001220
2435 015420 005005
2436 015422 052711 040000
2437 015426 012711 003000
2438 015432 016104 000006
2439 015436 020504
2440 015440 001401
2441 015442 104023
2442 015444 104401
2443 015446 104400
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MOV #5$,LOCK ;NEW SCOPE
CLR R5 ;PUT "EXPECTED" IN R5
5$: RESET ;BUS RESET
MOV #BIT9:BIT10,(R1) ;SEL6 IS IR
MOV 6(R1),R4 ;READ THE IR
CMP R5,R4 ;IS IT CLEARED?
BEQ 6$ ;BR IF YES
HLT 23 ;ERROR, IR IS NOT CLEARED
6$: SCOPE ;LOOP TO 5$ IF SW09=1
SCOPE ;SCOPE THIS TEST

:***** TEST 30 *****
:*MAINTENANCE INSTRUCTION REGISTER TEST
:*VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS'
:*AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A MASTER RESET.
:*****

: TEST 30
:-----
TST30: MOV #30,TSTNO
MOV #TST31,NEXT
MOV #1$,LOCK ;R1 CONTAINS BASE DMC11 ADDRESS
MSTCLR ;MASTER CLEAR DMC11
MOV #BIT9:BIT10,(R1) ;SEL6 IS NOW THE IR
CLR R5 ;PUT "EXPECTED" IN R5
1$: MOV R5,6(R1) ;CLEAR THE IR
MOV 6(R1),R4 ;READ THE IR
CMP R5,R4 ;IS IT CLEARED?
BEQ 2$ ;BR IF YES
HLT 23 ;ERROR IR IS NOT CLEAR
2$: SCOPE ;LOOP TO 1$ IF SW09=1
MOV #3$,LOCK ;NEW SCOPE
MOV #-1,R5 ;PUT "EXPECTED" IN R5
3$: MOV R5,6(R1) ;WRITE ALL ONES TO THE IR
MOV 6(R1),R4 ;READ THE IR
CMP R5,R4 ;IS IT ALL ONES?
BEQ 4$ ;BR IF YES
HLT 23 ;ERROR IR IS NOT = ALL ONES
4$: SCOPE ;LOOP TO 3$ IF SW09=1
MOV #5$,LOCK ;NEW SCOPE
CLR R5 ;PUT "EXPECTED" IN R5
5$: BIS #BIT14,(R1) ;MASTER CLEAR
MOV #BIT9:BIT10,(R1) ;SEL6 IS IR
MOV 6(R1),R4 ;READ THE IR
CMP R5,R4 ;IS IT CLEARED?
BEQ 6$ ;BR IF YES
HLT 23 ;ERROR, IR IS NOT CLEARED
6$: SCOPE ;LOOP TO 5$ IF SW09=1
SCOPE ;SCOPE THIS TEST

:***** TEST 31 *****
:*MICRO PROCESSOR TEST
:*LOAD DMPO6 WITH A MICRO-PROCESSOR INSTRUCTION, CLOCK IT

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015450 012737 000031 001226
015456 012737 015534 001216
015464 104412
015466 012761 000377 000004
015474 012711 001000
015500 012761 121105 000006
015506 052711 001400
015512 000240
015514 012705 177777
015520 016104 000004
015524 020504
015526 001401
015530 104003
015532 104400

015534 012737 000032 001226
015542 012737 015734 001216
015550 012737 015570 001220
015556 104412
015560 012702 000000
015564 012700 000001
015570
015574 010061 000004
015574 042761 000030 000004
015602 104414
015604 121100
015606 104414
015610 121005
015612 010005
015614 042705 000030
015620 116104 000005
015624 120504
015626 001401
015630 104004
015632 104401
015634 000241
015636 106100
015640 001353

```

: *VERIFY INSTRUCTION EXECUTED PROPERLY
: *INSTRUCTION SHOULD MOVE IBUS*4 TO IBUS*5. IBUS*4 IS ALL 1'S
: *AND IBUS*5 IS ALL 0'S. RESULT SHOULD BE ALL 1'S IN SEL4
: *****
:
: TEST 31
: -----
TST31: MOV #31,TSTNO
MOV #TST32,NEXT
MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
MOV #377,4(R1) ;PORT4 HI-BYTE=0'S LO-BYTE=1'S
MOV #BIT9,(R1) ;SET ROM1
MOV #121105,6(R1) ;INSTRUCTION TO PORT6
BIS #BIT8!BIT9,(R1) ;CLK INSTRUCTION, MOVE IBUS*4 TO IBUS*5
NOP
MOV #-1,R5 ;PUT "EXPECTED" IN R5
MOV 4(R1),R4 ;PUT "FOUND" INTO R4
CMP R5,R4 ;IS DATA CORRECT
BEQ 1$ ;BR IF YES
HLT 3 ;ERROR
;SCOPE THIS TEST
1$: SCOPE

: ***** TEST 32 *****
: *MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST*
: *FLOAT A 1 THROUGH IBUS* REGISTER 0
: *FLOAT A 0 THROUGH IBUS* REGISTER 0
: *****
:
: TEST 32
: -----
TST32: MOV #32,TSTNO
MOV #TST33,NEXT
MOV #64$,LOCK
MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
MOV #0,R2 ;SAVE REGISTER ADDRESS FOR TYPEOUT
MOV #1,PO ;START WITH BIT 0
64$: MOV R0,4(R1) ;PUT PATTERN INTO PORT4
BIC #30,4(R1) ;CLEAR UNWANTED BITS
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121100!0 ;MOV DATA TO IBUS* REGISTER 0
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121005!<0*20> ;READ FROM IBUS* REGISTER 0
MOV R0,R5 ;PUT EXPECTED IN R5
BIC #30,R5 ;CLEAR UNWANTED BITS
MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 65$ ;BR IF YES
HLT 4 ;ERROR
;SW09=1?
65$: CLC ;CLEAR CARRY
ROLB R0 ;SHIFT BIT IN R0
BNE 64$ ;IF R0=0 THEN DONE

```


2505	015642	012737	015656	001220		MOV	#67\$, LOCK	: NEW SCOPE
2506	015650	012700	000001			MOV	#1, R0	: START WITH BIT 0
2507	015654	005100			69\$:	COM	R0	: CHANGE TO FLOATING ZERO
2508	015656				67\$:			
2509	015656	010061	000004			MOV	R0, 4(R1)	: PUT PATTERN INTO PORT4
2510	015662	042761	000030	000004		BIC	#30, 4(R1)	: CLEAR UNWANTED BITS
2511	015670	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2512	015672	121100				121100!0		: MOV DATA TO IBUS* REGISTER 0
2513	015674	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2514	015676	121005				121005! <0*20>		: READ FROM IBUS* REGISTER 0
2515	015700	010005				MOV	R0, R5	: PUT EXPECTED IN R5
2516	015702	042705	000030			BIC	#30, R5	: CLEAR UNWANTED BITS
2517	015706	116104	000005			MOVB	5(R1), R4	: PUT "FOUND" INTO R4
2518	015712	120504				CMPB	R5, R4	: DATA CORRECT?
2519	015714	001401				BEQ	68\$: BR IF YES
2520	015716	104004				HLT	4	: ERROR
2521	015720	104401			68\$:	SCOPE		: SW09=1?
2522	015722	005100				COM	R0	: CHANGE TO FLOATING 1
2523	015724	000241				CLC		: CLEAR CARRY
2524	015726	106100				ROLB	R0	: SHIFT BIT IN R0
2525	015730	001351				BNE	69\$: IF R0=0 THEN DONE
2526	015732	104400				SCOPE		: SCOPE THIS TEST
2527								
2528								
2529								
2530								: ***** TEST 33 *****
2531								: *MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
2532								: *FLOAT A 1 THROUGH IBUS* REGISTER 2
2533								: *FLOAT A 0 THROUGH IBUS* REGISTER 2
2534								: *****
2535								: TEST 33
2536								: -----
2537	015734	012737	000033	001226	TST33:	MOV	#33, TSTNO	
2538	015742	012737	016134	001216		MOV	#TST34, NEXT	
2539	015750	012737	015770	001220		MOV	#64\$, LOCK	
2540								: R1 CONTAINS BASE DMC11 ADDRESS
2541	015756	104412				MSTCLR		: MASTER CLEAR DMC11
2542	015760	012702	000002			MOV	#2, R2	: SAVE REGISTER ADDRESS FOR TYPEOUT
2543	015764	012700	000001			MOV	#1, R0	: START WITH BIT 0
2544	015770				64\$:			
2545	015770	010061	000004			MOV	R0, 4(R1)	: PUT PATTERN INTO PORT4
2546	015774	042761	000070	000004		BIC	#70, 4(R1)	: CLEAR UNWANTED BITS
2547	016002	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2548	016004	121102				121100!2		: MOV DATA TO IBUS* REGISTER 2
2549	016006	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2550	016010	121045				121005! <2*20>		: READ FROM IBUS* REGISTER 2
2551	016012	010005				MOV	R0, R5	: PUT EXPECTED IN R5
2552	016014	042705	000070			BIC	#70, R5	: CLEAR UNWANTED BITS
2553	016020	116104	000005			MOVB	5(R1), R4	: PUT "FOUND" INTO R4
2554	016024	120504				CMPB	R5, R4	: DATA CORRECT?
2555	016026	001401				BEQ	65\$: BR IF YES
2556	016030	104004				HLT	4	: ERROR
2557	016032	104401			65\$:	SCOPE		: SW09=1?
2558	016034	000241				CLC		: CLEAR CARRY
2559	016036	106100				ROLB	R0	: SHIFT BIT IN R0
2560	016040	001353				BNE	64\$: IF R0=0 THEN DONE

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2561 016042 012737 016056 001220      MOV      #67$,LOCK      ;NEW SCOPE1
2562 016050 012700 000001              MOV      #1,R0          ;START WITH BIT 0
2563 016054 005100      69$:    COM      R0          ;CHANGE TO FLOATING ZERO
2564 016056              67$:
2565 016056 010061 000004              MOV      R0,4(R1)      ;PUT PATTERN INTO PORT4
2566 016062 042761 000070 000004      BIC      #70,4(R1)     ;CLEAR UNWANTED BITS
2567 016070 104414      ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2568 016072 121102      121100!2 ;MOV DATA TO IBUS* REGISTER 2
2569 016074 104414      ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2570 016076 121045      121005!<2*20> ;READ FROM IBUS* REGISTER 2
2571 016100 010005              MOV      R0,R5         ;PUT EXPECTED IN R5
2572 016102 042705 000070      BIC      #70,R5        ;CLEAR UNWANTED BITS
2573 016104 116104 000005      MOV      5(R1),R4      ;PUT "FOUND" INTO R4
2574 016112 20504              CMPB    R5,R4         ;DATA CORRECT?
2575 016114 001401      BEQ     68$           ;BR IF YES
2576 016116 104004              HLT     4              ;ERROR
2577 016120 104401      68$:    SCOPE1         ;SW09=1?
2578 016122 005100      COM      R0           ;CHANGE TO FLOATING 1
2579 016124 000241      CLC
2580 016126 106100      ROLB    R0           ;SHIFT BIT IN R0
2581 016130 001351      BNE     69$           ;IF R0=0 THEN DONE
2582 016132 104400      SCOPE   ;SCOPE THIS TEST
2583
2584
2585      ;***** TEST 34 *****
2586      ;*MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
2587      ;*FLOAT A 1 THROUGH IBUS* REGISTER 4
2588      ;*FLOAT A 0 THROUGH IBUS* REGISTER 4
2589      ;*****
2590
2591      ; TEST 34
2592      ;-----
2593 016134 012737 000034 001226      TST34:  MOV      #34,TSTNO
2594 016142 012737 016310 001216      MOV      #TST35,NEXT
2595 016150 012737 016170 001220      MOV      #64$,LOCK
2596
2597 016156 104412              MSTCLR   ;R1 CONTAINS BASE DMC11 ADDRESS
2598 016160 012702 000004              MOV      #4,R2         ;MASTER CLEAR DMC11
2599 016164 012700 000001              MOV      #1,R0         ;SAVE REGISTER ADDRESS FOR TYPEOUT
2600 016170      64$:    ;START WITH BIT 0
2601 016170 010061 000004              MOV      R0,4(R1)     ;PUT PATTERN INTO PORT4
2602 016174 104414      ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2603 016176 121104      121100!4 ;MOV DATA TO IBUS* REGISTER 4
2604 016200 104414      ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2605 016202 121105      121005!<4*20> ;READ FROM IBUS* REGISTER 4
2606 016204 010005              MOV      R0,R5         ;PUT EXPECTED IN R5
2607 016206 116104 000005      MOV      5(R1),R4      ;PUT "FOUND" INTO R4
2608 016212 120504              CMPB    R5,R4         ;DATA CORRECT?
2609 016214 001401      BEQ     65$           ;BR IF YES
2610 016216 104004              HLT     4              ;ERROR
2611 016220 104401      65$:    SCOPE1         ;SW09=1?
2612 016222 000241      CLC           ;CLEAR CARRY
2613 016224 106100      ROLB    R0           ;SHIFT BIT IN R0
2614 016226 001360      BNE     64$           ;IF R0=0 THEN DONE
2615 016230 012737 016244 001220      MOV      #67$,LOCK   ;NEW SCOPE1
2616 016236 012700 000001              MOV      #1,R0         ;START WITH BIT 0

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2617 016242 005100          69$: COM      RO          ;CHANGE TO FLOATING ZERO
2618 016244          67$:          ;
2619 016244 010061 000004          MOV      RO,4(R1)      ;PUT PATTERN INTO PORT4
2620 016250 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2621 016252 121104          121100!4          ;MOV DATA TO IBUS* REGISTER 4
2622 016254 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2623 016256 121105          121005!<4*20>      ;READ FROM IBUS* REGISTER 4
2624 016260 010005          MOV      RO,R5          ;PUT EXPECTED IN R5
2625 016262 116104 000005          MOVB    5(R1),R4      ;PUT "FOUND" INTO R4
2626 016266 120504          CMPB    R5,R4          ;DATA CORRECT?
2627 016270 001401          BEQ     68$            ;BR IF YES
2628 016272 104004          HLT     4              ;ERROR
2629 016274 104401          68$: SCOPI          ;SW09=1?
2630 016276 005100          COM      RO          ;CHANGE TO FLOATING 1
2631 016300 000241          CLC          ;CLEAR CARRY
2632 016302 106100          ROLB    RO            ;SHIFT BIT IN RO
2633 016304 001356          BNE     69$            ;IF RO=0 THEN DONE
2634 016306 104400          SCOPE          ;SCOPE THIS TEST
2635
2636
2637
2638          ;***** TEST 35 *****
2639          ;*MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
2640          ;*FLOAT A 1 THROUGH IBUS* REGISTER 5
2641          ;*FLOAT A 0 THROUGH IBUS* REGISTER 5
2642          ;*****
2643          ; TEST 35
2644          ;-----
2645 016310 012737 000035 001226 TST35: MOV      #35,TSTNO
2646 016316 012737 016464 001216      MOV      #TST36,NEXT
2647 016324 012737 016344 001220      MOV      #64$,LOCK
2648          ;R1 CONTAINS BASE DMC11 ADDRESS
2649 016332 104412          MSTCLR          ;MASTER CLEAR DMC11
2650 016334 012702 000005          MOV      #5,R2          ;SAVE REGISTER ADDRESS FOR TYPEOUT
2651 016340 012700 000001          MOV      #1,RO          ;START WITH BIT 0
2652 016344          64$:          ;
2653 016344 010061 000004          MOV      RO,4(R1)      ;PUT PATTERN INTO PORT4
2654 016350 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2655 016352 121105          121100!5          ;MOV DATA TO IBUS* REGISTER 5
2656 016354 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2657 016356 121125          121005!<5*20>      ;READ FROM IBUS* REGISTER 5
2658 016360 010005          MOV      RO,R5          ;PUT EXPECTED IN R5
2659 016362 116104 000005          MOVB    5(R1),R4      ;PUT "FOUND" INTO R4
2660 016366 120504          CMPB    R5,R4          ;DATA CORRECT?
2661 016370 001401          BEQ     65$            ;BR IF YES
2662 016372 104004          HLT     4              ;ERROR
2663 016374 104401          65$: SCOPI          ;SW09=1?
2664 016376 000241          CLC          ;CLEAR CARRY
2665 016400 106100          ROLB    RO            ;SHIFT BIT IN RO
2666 016402 001360          BNE     64$            ;IF RO=0 THEN DONE
2667 016404 012737 016420 001220      MOV      #67$,LOCK
2668 016412 012700 000001          MOV      #1,RO          ;NEW SCOPI
2669 016416 005100          69$: COM      RO          ;START WITH BIT 0
2670 016420          67$:          ;CHANGE TO FLOATING ZERO
2671 016420 010061 000004          MOV      RO,4(R1)      ;PUT PATTERN INTO PORT4
2672 016424 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

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2673	016426	121105				121100!5	; MOV DATA TO IBUS* REGISTER 5
2674	016430	104414				ROMCLK	; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2675	016432	121125				121005!<5*20>	; READ FROM IBUS* REGISTER 5
2676	016434	010005				MOV RO,R5	; PUT EXPECTED IN R5
2677	016436	116104	000005			MOV B 5(R1),R4	; PUT "FOUND" INTO R4
2678	016442	120504				CMPB R5,R4	; DATA CORRECT?
2679	016444	001401				BEQ 68\$; BR IF YES
2680	016446	104004				HLT 4	; ERROR
2681	016450	104401			68\$:	SCOPI	; SW09=1?
2682	016452	005100				COM RO	; CHANGE TO FLOATING 1
2683	016454	000241				CLC	; CLEAR CARRY
2684	016456	106100				ROLB RO	; SHIFT BIT IN RO
2685	016460	001356				BNE 69\$; IF RO=0 THEN DONE
2686	016462	104400				SCOPE	; SCOPE THIS TEST
2687							
2688							
2689							
2690							
2691							
2692							
2693							
2694							
2695							
2696							
2697							
2698	016464	012737	000036	001226		TST36: MOV #36,TSTNO	
2699	016472	012737	016664	001216		MOV #TST37,NEXT	
2700	016500	012737	016520	001220		MOV #64\$,LOCK	
2701							
2702	016506	104412				MSTCLR	; R1 CONTAINS BASE DMC11 ADDRESS
2703	016510	012702	000010			MOV #10,R2	; MASTER CLEAR DMC11
2704	016514	012700	000001			MOV #1,R0	; SAVE REGISTER ADDRESS FOR TYPEOUT
2705	016520				64\$:		; START WITH BIT 0
2706	016520	010061	000004			MOV RO,4(R1)	; PUT PATTERN INTO PORT4
2707	016524	042761	000141	000004		BIC #141,4(R1)	; CLEAR UNWANTED BITS
2708	016532	104414				ROMCLK	; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2709	016534	121110				121100!10	; MOV DATA TO IBUS* REGISTER 10
2710	016536	104414				ROMCLK	; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2711	016540	121205				121005!<10*20>	; READ FROM IBUS* REGISTER 10
2712	016542	010005				MOV RO,R5	; PUT EXPECTED IN R5
2713	016544	042705	000141			BIC #141,R5	; CLEAR UNWANTED BITS
2714	016550	116104	000005			MOV B 5(R1),R4	; PUT "FOUND" INTO R4
2715	016554	120504				CMPB R5,R4	; DATA CORRECT?
2716	016556	001401				BEQ 65\$; BR IF YES
2717	016560	104004				HLT 4	; ERROR
2718	016562	104401			65\$:	SCOPI	; SW09=1?
2719	016564	000241				CLC	; CLEAR CARRY
2720	016566	106100				ROLB RO	; SHIFT BIT IN RO
2721	016570	001353				BNE 64\$; IF RO=0 THEN DONE
2722	016572	012737	016606	001220		MOV #67\$,LOCK	; NEW SCOPI
2723	016600	012700	000001			MOV #1,R0	; START WITH BIT 0
2724	016604	005100			69\$:	COM RO	; CHANGE TO FLOATING ZERO
2725	016606				67\$:		
2726	016606	010061	000004			MOV RO,4(R1)	; PUT PATTERN INTO PORT4
2727	016612	042761	000141	000004		BIC #141,4(R1)	; CLEAR UNWANTED BITS
2728	016620	104414				ROMCLK	; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

2729 016622 121110
2730 016624 104414
2731 016626 121205
2732 016630 010005
2733 016632 042705 000141
2734 016636 116104 000005
2735 016642 120504
2736 016644 001401
2737 016646 104004
2738 016650 104401
2739 016652 005100
2740 016654 000241
2741 016656 106100
2742 016660 001351
2743 016662 104400

68\$:

121100!10
ROMCLK
121005!<10*20>
MOV RO,R5
BIC #141,R5
MOVB 5(R1),R4
CMPB R5,R4
BEQ 68\$
HLT 4
SCOPI
COM RO
CLC
ROLB RO
BNE 69\$
SCOPE

;MOV DATA TO IBUS* REGISTER 10
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;READ FROM IBUS* REGISTER 10
;PUT EXPECTED IN R5
;CLEAR UNWANTED BITS
;PUT "FOUND" INTO R4
;DATA CORRECT?
;BR IF YES
;ERROR
;SW09=1?
;CHANGE TO FLOATING 1
;CLEAR CARRY
;SHIFT BIT IN RO
;IF RO=0 THEN DONE
;SCOPE THIS TEST

2744
2745
2746
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2755

***** TEST 37 *****
;MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS* REGISTER 11
;FLOAT A 0 THROUGH IBUS* REGISTER 11
;THE BR RQ BIT, PGM CLOCK BIT, FORCE POWER FAIL BIT
;(BITS 7,4,1) ARE ALL MASKED DURING THIS TEST

; TEST 37

2756 016664 012737 000037 001226
2757 016672 012737 017104 001216
2758 016700 012737 016720 001220
2759
2760 016706 104412
2761 016710 012702 000011
2762 016714 012700 000001
2763 016720
2764 016720 010061 000004
2765 016724 042761 000262 000004
2766 016732 104414
2767 016734 121111
2768 016736 104414
2769 016740 121225
2770 016742 010005
2771 016744 042705 000262
2772 016750 052705 000020
2773 016754 116104 000005
2774 016760 052704 000020
2775 016764 120504
2776 016766 001401
2777 016770 104004
2778 016772 104401
2779 016774 000241
2780 016776 106100
2781 017000 001347
2782 017002 012737 017016 001220
2783 017010 012700 000001
2784 017014 005100

TST37:

64\$:

65\$:

69\$:

MOV #37,TSTNO
MOV #TST40,NEXT
MOV #64\$,LOCK
MSTCLR
MOV #11,R2
MOV #1,RO
MOV RO,4(R1)
BIC #262,4(R1)
ROMCLK
121100!11
ROMCLK
121005!<11*20>
MOV RO,R5
BIC #262,R5
BIS #20,R5
MOVB 5(R1),R4
BIS #20,R4
CMPB R5,R4
BEQ 65\$
HLT 4
SCOPI
CLC
ROLB RO
BNE 64\$
MOV #67\$,LOCK
MOV #1,RO
COM RO

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;SAVE REGISTER ADDRESS FOR TYPEOUT
;START WITH BIT 0
;PUT PATTERN INTO PORT4
;CLEAR UNWANTED BITS
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOV DATA TO IBUS* REGISTER 11
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;READ FROM IBUS* REGISTER 11
;PUT EXPECTED IN R5
;CLEAR UNWANTED BITS
;ADD THESE BITS
;PUT "FOUND" INTO R4
;ADD THIS BIT
;DATA CORRECT?
;BR IF YES
;ERROR
;SW09=1?
;CLEAR CARRY
;SHIFT BIT IN RO
;IF RO=0 THEN DONE
;NEW SCOPI
;START WITH BIT C
;CHANGE TO FLOATING ZERO

```

2785 017016
2786 017016 010061 000004
2787 017022 042761 000262 000004
2788 017030 104414
2789 017032 121111
2790 017034 104414
2791 017036 121225
2792 017040 010005
2793 017042 042705 000262
2794 017046 052705 000020
2795 017052 116104 000005
2796 017056 052704 000020
2797 017062 120504
2798 017064 001401
2799 017066 104004
2800 017070 104401
2801 017072 005100
2802 017074 000241
2803 017076 106100
2804 017100 001345
2805 017102 104400
2806
2807
2808
2809
2810
2811
2812
2813
2814
2815
2816 017104 012737 000040 001226
2817 017112 012737 017260 001216
2818 017120 012737 017140 001220
2819
2820 017126 104412
2821 017130 012702 000000
2822 017134 012700 000001
2823 017140
2824 017140 010061 000004
2825 017144 104414
2826 017146 122100
2827 017150 104414
2828 017152 021005
2829 017154 010005
2830 017156 116104 000005
2831 017162 120504
2832 017164 001401
2833 017166 104005
2834 017170 104401
2835 017172 000241
2836 017174 106100
2837 017176 001360
2838 017200 012737 017214 001220
2839 017206 012700 000001
2840 017212 005100

```

67\$:

```

MOV RO,4(R1) ;PUT PATTERN INTO PORT4
BIC #262,4(R1) ;CLEAR UNWANTED BITS
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121100!11 ;MOV DATA TO IBUS* REGISTER 11
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121005!<11*20> ;READ FROM IBUS* REGISTER 11
MOV RO,R5 ;PUT EXPECTED IN R5
BIC #262,R5 ;CLEAR UNWANTED BITS
BIS #20,R5 ;ADD THESE BITS
MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
BIS #20,R4 ;ADD THIS BIT
CMPB R5,R4 ;DATA CORRECT?
BEQ 68$ ;BR IF YES
HLT 4 ;ERROR
;SW09=1?
;CHANGE TO FLOATING 1
COM RO ;CLEAR CARRY
CLC ;SHIFT BIT IN RO
ROLB RO ;SHIFT BIT IN RO
BNE 69$ ;IF RO=0 THEN DONE
SCOPE ;SCOPE THIS TEST

```

68\$:

```

;***** TEST 40 *****
;MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS REGISTER 0
;FLOAT A 0 THROUGH IBUS REGISTER C
;*****

```

TEST 40

TST40:

```

MOV #40,TSTNO
MOV #TST41,NEXT
MOV #64$,LOCK
;R1 CONTAINS BASE DMC11 ADDRESS
MSTCLR ;MASTER CLEAR DMC11
MOV #0,R2 ;SAVE REGISTER ADDRESS FOR TYPEOUT
MOV #1,R0 ;START WITH BIT 0

```

64\$:

```

MOV RO,4(R1) ;PUT PATTERN INTO PORT4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!0 ;MOV DATA TO IBUS REGISTER 0
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!<0*20> ;READ FROM IBUS REGISTER 0
MOV RO,R5 ;PUT EXPECTED IN R5
MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 65$ ;BR IF YES
HLT 5 ;ERROR
;SW09=1?
;CLEAR CARRY
COM RO ;SHIFT BIT IN RO
ROLB RO ;SHIFT BIT IN RO
BNE 64$ ;IF RO=0 THEN DONE
MOV #67$,LOCK ;NEW SCOPE
MOV #1,R0 ;START WITH BIT 0

```

65\$:

```

SCOPE ;CHANGE TO FLOATING ZERO
CLC
ROLB RO
BNE 64$
MOV #67$,LOCK
MOV #1,R0
COM RO

```

69\$:

2841	017214				67\$:	MOV	RO,4(R1)	:	PUT PATTERN INTO PORT4
2842	017214	010061	000004			ROMCLK		:	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2843	017220	104414				122100!0		:	MOV DATA TO IBUS REGISTER 0
2844	017222	122100				ROMCLK		:	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2845	017224	104414				21005!<0*20>		:	READ FROM IBUS REGISTER 0
2846	017226	021005				MOV	RO,R5	:	PUT EXPECTED IN R5
2847	017230	010005				MOV	5(R1),R4	:	PUT "FOUND" INTO R4
2848	017232	116104	000005			CMPB	R5,R4	:	DATA CORRECT?
2849	017236	120504				BEQ	68\$:	BR IF YES
2850	017240	001401				HLT	5	:	ERROR
2851	017242	104005			68\$:	SCOPI		:	SW09=1?
2852	017244	104401				COM	RO	:	CHANGE TO FLOATING 1
2853	017246	005100				CLC		:	CLEAR CARRY
2854	017250	000241				ROLB	RO	:	SHIFT BIT IN RO
2855	017252	106100				BNE	69\$:	IF RO=0 THEN DONE
2856	017254	001356				SCOPE		:	SCOPE THIS TEST
2857	017256	104400							
2858									
2859									
2860									
2861									
2862									
2863									
2864									
2865									
2866									
2867									
2868	017260	012737	000041	001226	TST41:	MOV	#41,TSTNO		
2869	017266	012737	017434	001216		MOV	#TST42,NEXT		
2870	017274	012737	017314	001220		MOV	#64\$,LOCK		
2871									
2872	017302	104412				MSTCLR		:	R1 CONTAINS BASE DMC11 ADDRESS
2873	017304	012702	000001			MOV	#1,R2	:	MASTER CLEAR DMC11
2874	017310	012700	000001			MOV	#1,RO	:	SAVE REGISTER ADDRESS FOR TYPEOUT
2875	017314							:	START WITH BIT 0
2876	017314	010061	000004		64\$:	MOV	RO,4(R1)	:	PUT PATTERN INTO PORT4
2877	017320	104414				ROMCLK		:	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2878	017322	122101				122100!1		:	MOV DATA TO IBUS REGISTER 1
2879	017324	104414				ROMCLK		:	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2880	017326	021025				21005!<1*20>		:	READ FROM IBUS REGISTER 1
2881	017330	010005				MOV	RO,R5	:	PUT EXPECTED IN R5
2882	017332	116104	000005			MOV	5(R1),R4	:	PUT "FOUND" INTO R4
2883	017336	120504				CMPB	R5,R4	:	DATA CORRECT?
2884	017340	001401				BEQ	65\$:	BR IF YES
2885	017342	104005				HLT	5	:	ERROR
2886	017344	104401			65\$:	SCOPI		:	SW09=1?
2887	017346	000241				CLC		:	CLEAR CARRY
2888	017350	106100				ROLB	RO	:	SHIFT BIT IN RO
2889	017352	001360				BNE	64\$:	IF RO=0 THEN DONE
2890	017354	012737	017370	001220		MOV	#67\$,LOCK	:	NEW SCOPI
2891	017362	012700	000001			MOV	#1,RO	:	START WITH BIT 0
2892	017366	005100			69\$:	COM	RO	:	CHANGE TO FLOATING ZERO
2893	017370				67\$:				
2894	017370	010061	000004			MOV	RO,4(R1)	:	PUT PATTERN INTO PORT4
2895	017374	104414				ROMCLK		:	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2896	017376	122101				122100!1		:	MOV DATA TO IBUS REGISTER 1

```

;***** TEST 41 *****
;MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS REGISTER 1
;FLOAT A 0 THROUGH IBUS REGISTER 1
;*****

```

TEST 41

```

-----
TST41: MOV #41,TSTNO
MOV #TST42,NEXT
MOV #64$,LOCK

```

```

MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
MOV #1,R2 ;MASTER CLEAR DMC11
MOV #1,RO ;SAVE REGISTER ADDRESS FOR TYPEOUT
;START WITH BIT 0

```

```

64$: MOV RO,4(R1) ;PUT PATTERN INTO PORT4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!1 ;MOV DATA TO IBUS REGISTER 1
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!<1*20> ;READ FROM IBUS REGISTER 1
MOV RO,R5 ;PUT EXPECTED IN R5
MOV 5(R1),R4 ;PUT "FOUND" INTO R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 65$ ;BR IF YES
HLT 5 ;ERROR

```

```

65$: SCOPI ;SW09=1?
CLC ;CLEAR CARRY
ROLB RO ;SHIFT BIT IN RO
BNE 64$ ;IF RO=0 THEN DONE
MOV #67$,LOCK ;NEW SCOPI
MOV #1,RO ;START WITH BIT 0
COM RO ;CHANGE TO FLOATING ZERO

```

```

67$: MOV RO,4(R1) ;PUT PATTERN INTO PORT4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!1 ;MOV DATA TO IBUS REGISTER 1

```

2897	017400	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2898	017402	021025				21005!<1*20>		;READ FROM IBUS REGISTER 1
2899	017404	010005				MOV RO,R5		;PUT EXPECTED IN R5
2900	017406	116104	000005			MOVB 5(R1),R4		;PUT "FOUND" INTO R4
2901	017412	120504				CMPB R5,R4		;DATA CORRECT?
2902	017414	001401				BEQ 68\$;BR IF YES
2903	017416	104005				HLT 5		;ERROR
2904	017420	104401			68\$:	SCOPI		;SW09=1?
2905	017422	005100				COM RO		;CHANGE TO FLOATING 1
2906	017424	000241				CLC		;CLEAR CARRY
2907	017426	106100				ROLB RO		;SHIFT BIT IN RO
2908	017430	001356				BNE 69\$;IF RO=0 THEN DONE
2909	017432	104400				SCOPE		;SCOPE THIS TEST
2910								
2911								
2912								
2913								
2914								
2915								
2916								
2917								
2918								
2919								
2920	017434	012737	000042	001226		TST42: MOV #42,TSTNO		
2921	017442	012737	017610	001216		MOV #TST43,NEXT		
2922	017450	012737	017470	001220		MOV #64\$,LOCK		
2923								
2924	017456	104412				MSTCLR		;R1 CONTAINS BASE DMC11 ADDRESS
2925	017460	012702	000002			MOV #2,R2		;MASTER CLEAR DMC11
2926	017464	012700	000001			MOV #1,R0		;SAVE REGISTER ADDRESS FOR TYPEOUT
2927	017470				64\$:			;START WITH BIT 0
2928	017470	010061	000004			MOV RO,4(R1)		;PUT PATTERN INTO PORT4
2929	017474	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2930	017476	122102				122100!2		;MOV DATA TO IBUS REGISTER 2
2931	017500	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2932	017502	021045				21005!<2*20>		;READ FROM IBUS REGISTER 2
2933	017504	010005				MOV RO,R5		;PUT EXPECTED IN R5
2934	017506	116104	000005			MOVB 5(R1),R4		;PUT "FOUND" INTO R4
2935	017512	120504				CMPB R5,R4		;DATA CORRECT?
2936	017514	001401				BEQ 65\$;BR IF YES
2937	017516	104005				HLT 5		;ERROR
2938	017520	104401			65\$:	SCOPI		;SW09=1?
2939	017522	000241				CLC		;CLEAR CARRY
2940	017524	106100				ROLB RO		;SHIFT BIT IN RO
2941	017526	001360				BNE 64\$;IF RO=0 THEN DONE
2942	017530	012737	017544	001220		MOV #67\$,LOCK		;NEW SCOPI
2943	017536	012700	000001			MOV #1,R0		;START WITH BIT 0
2944	017542	005100			69\$:	COM RO		;CHANGE TO FLOATING ZERO
2945	017544				67\$:			
2946	017544	010061	000004			MOV RO,4(R1)		;PUT PATTERN INTO PORT4
2947	017550	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2948	017552	122102				122100!2		;MOV DATA TO IBUS REGISTER 2
2949	017554	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2950	017556	021045				21005!<2*20>		;READ FROM IBUS REGISTER 2
2951	017560	010005				MOV RO,R5		;PUT EXPECTED IN R5
2952	017562	116104	000005			MOVB 5(R1),R4		;PUT "FOUND" INTO R4

2953 017566 120504
 2954 017570 001401
 2955 017572 104005
 2956 017574 104401
 2957 017576 005100
 2958 017600 000241
 2959 017602 106100
 2960 017604 001356
 2961 017606 104400
 2962
 2963
 2964
 2965
 2966
 2967
 2968
 2969
 2970
 2971
 2972 017610 012737 000043 001226
 2973 017616 012737 017764 001216
 2974 017624 012737 017644 001220
 2975
 2976 017632 104412
 2977 017634 012702 000003
 2978 017640 012700 000001
 2979 017644
 2980 017644 010061 000004
 2981 017650 104414
 2982 017652 122103
 2983 017654 104414
 2984 017656 021065
 2985 017660 010005
 2986 017662 116104 000005
 2987 017666 120504
 2988 017670 001401
 2989 017672 104005
 2990 017674 104401
 2991 017676 000241
 2992 017700 106100
 2993 017702 001360
 2994 017704 012737 017720 001220
 2995 017712 012700 000001
 2996 017716 005100
 2997 017720
 2998 017720 010061 000004
 2999 017724 104414
 3000 017726 122103
 3001 017730 104414
 3002 017732 021065
 3003 017734 010005
 3004 017736 116104 000005
 3005 017742 120504
 3006 017744 001401
 3007 017746 104005
 3008 017750 104401

68\$:

CMPB R5,R4
 BEQ 68\$
 HLT 5
 SCOP1
 COM RO
 CLC
 ROLB RO
 BNE 69\$
 SCOPE

:DATA CORRECT?
 :BR IF YES
 :ERROR
 :SW09=1?
 :CHANGE TO FLOATING 1
 :CLEAR CARRY
 :SHIFT BIT IN RO
 :IF RO=0 THEN DONE
 :SCOPE THIS TEST

:***** TEST 43 *****
 :*MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
 :*FLOAT A 1 THROUGH IBUS REGISTER 3
 :*FLOAT A 0 THROUGH IBUS REGISTER 3
 :*****

: TEST 43

TST43:

MOV #43,TSTNO
 MOV #TST44,NEXT
 MOV #64\$,LOCK

:R1 CONTAINS BASE DMC11 ADDRESS
 :MASTER CLEAR DMC11
 :SAVE REGISTER ADDRESS FOR TYPEOUT
 :START WITH BIT 0

64\$:

MOV RO,4(R1)
 ROMCLK
 122100!3
 ROMCLK
 21005!<3*20>
 MOV RO,R5
 MOVB 5(R1),R4

:PUT PATTERN INTO PORT4
 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 :MOV DATA TO IBUS REGISTER 3
 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 :READ FROM IBUS REGISTER 3

65\$:

CMPB R5,R4
 BEQ 65\$
 HLT 5
 SCOP1
 CLC
 ROLB RO
 BNE 64\$
 MOV #67\$,LOCK
 MOV #1,RO

:PUT EXPECTED IN R5
 :PUT "FOUND" INTO R4
 :DATA CORRECT?
 :BR IF YES
 :ERROR
 :SW09=1?
 :CLEAR CARRY
 :SHIFT BIT IN RO
 :IF RO=0 THEN DONE

69\$:

COM RO

:NEW SCOPE
 :START WITH BIT 0
 :CHANGE TO FLOATING ZERO

67\$:

MOV RO,4(R1)
 ROMCLK
 122100!3
 ROMCLK
 21005!<3*20>
 MOV RO,R5
 MOVB 5(R1),R4

:PUT PATTERN INTO PORT4
 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 :MOV DATA TO IBUS REGISTER 3
 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 :READ FROM IBUS REGISTER 3

68\$:

CMPB R5,R4
 BEQ 68\$
 HLT 5
 SCOP1

:PUT EXPECTED IN R5
 :PUT "FOUND" INTO R4
 :DATA CORRECT?
 :BR IF YES
 :ERROR
 :SW09=1?

3009 017752 005100
 3010 017754 000241
 3011 017756 106100
 3012 017760 001356
 3013 017762 104400
 3014
 3015
 3016
 3017
 3018
 3019
 3020
 3021
 3022
 3023
 3024 017764 012737 000044 001226
 3025 017772 012737 020140 001216
 3026 020000 012737 020020 001220
 3027
 3028 020006 104412
 3029 020010 012702 000004
 3030 020014 012700 000001
 3031 020020
 3032 020020 010061 000004
 3033 020024 104414
 3034 020026 122104
 3035 020030 104414
 3036 020032 021105
 3037 020034 010005
 3038 020036 116104 000005
 3039 020042 120504
 3040 020044 001401
 3041 020046 104005
 3042 020050 104401
 3043 020052 000241
 3044 020054 106100
 3045 020056 001360
 3046 020060 012737 020074 001220
 3047 020066 012700 000001
 3048 020072 005100
 3049 020074
 3050 020074 010061 000004
 3051 020100 104414
 3052 020102 122104
 3053 020104 104414
 3054 020106 021105
 3055 020110 010005
 3056 020112 116104 000005
 3057 020116 120504
 3058 020120 001401
 3059 020122 104005
 3060 020124 104401
 3061 020126 005100
 3062 020130 000241
 3063 020132 106100
 3064 020134 001356

```

COM      RO      ;CHANGE TO FLOATING 1
CLC      ;CLEAR CARRY
ROLB     RO      ;SHIFT BIT IN RO
BNE      69$     ;IF RO=0 THEN DONE
SCOPE    ;SCOPE THIS TEST

;***** TEST 44 *****
;MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
;FLOAT A 1 THROUGH IBUS REGISTER 4
;FLOAT A 0 THROUGH IBUS REGISTER 4
;*****

; TEST 44
-----
TST44:  MOV      #44,TSTNO
        MOV      #TST45,NEXT
        MOV      #64$,LOCK
        ;R1 CONTAINS BASE DMC11 ADDRESS
        MSTCLR   ;MASTER CLEAR DMC11
        MOV      #4,R2
        MOV      #1,R0
        ;SAVE REGISTER ADDRESS FOR TYPE3JT
        ;START WITH BIT 0
        64$:    MOV      RO,4(R1)
        ;PUT PATTERN INTO PORT4
        ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
        122100!4 ;MOV DATA TO IBUS REGISTER 4
        ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
        21005!<4*20> ;READ FROM IBUS REGISTER 4
        MOV      RO,R5
        MOVB     S(R1),R4
        ;PUT EXPECTED IN R5
        ;PUT "FOUND" INTO R4
        CMPB     R5,R4
        ;DATA CORRECT?
        BEQ      65$
        ;BR IF YES
        HLT      5
        ;ERROR
        65$:    SCOP1
        ;SW09=1?
        CLC      ;CLEAR CARRY
        ROLB     RO
        ;SHIFT BIT IN RO
        BNE      64$
        ;IF RO=0 THEN DONE
        MOV      #67$,LOCK
        ;NEW SCOP1
        MOV      #1,R0
        ;START WITH BIT 0
        69$:    COM      RO
        ;CHANGE TO FLOATING ZERO
        67$:    MOV      RO,4(R1)
        ;PUT PATTERN INTO PORT4
        ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
        122100!4 ;MOV DATA TO IBUS REGISTER 4
        ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
        21005!<4*20> ;READ FROM IBUS REGISTER 4
        MOV      RO,R5
        MOVB     S(R1),R4
        ;PUT EXPECTED IN R5
        ;PUT "FOUND" INTO R4
        CMPB     R5,R4
        ;DATA CORRECT?
        BEQ      68$
        ;BR IF YES
        HLT      5
        ;ERROR
        68$:    SCOP1
        ;SW09=1?
        COM      RO
        ;CHANGE TO FLOATING !
        CLC      ;CLEAR CARRY
        ROLB     RO
        ;SHIFT BIT IN RO
        BNE      69$
        ;IF RO=0 THEN DONE
  
```

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3065 020136 104400          SCOPE          ;SCOPE THIS TEST
3066
3067
3068          ;***** TEST 45 *****
3069          ;*MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
3070          ;*FLOAT A 1 THROUGH IBUS REGISTER 5
3071          ;*FLOAT A 0 THROUGH IBUS REGISTER 5
3072          ;*****
3073
3074          ; TEST 45
3075          ;-----
3076 020140 012737 000045 001226      TST45:  MOV     #45,TSTNO
3077 020146 012737 020314 001216      MOV     #TST46,NEXT
3078 020154 012737 020174 001220      MOV     #64$,LOCK
3079
3080 020162 104412          MSTCLR          ;R1 CONTAINS BASE DMC11 ADDRESS
3081 020164 012702 000005          MOV     #5,R2    ;MASTER CLEAR DMC11
3082 020170 012700 000001          MOV     #1,R0    ;SAVE REGISTER ADDRESS FOR TYPEOUT
3083 020174          64$:          ;START WITH BIT 0
3084 020174 010061 000004          MOV     R0,4(R1) ;PUT PATTERN INTO PORT4
3085 020200 104414          ROMCLK         ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3086 020202 122105          122100!5      ;MOV DATA TO IBUS REGISTER 5
3087 020204 104414          ROMCLK         ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3088 020206 021125          21005!<5*20> ;READ FROM IBUS REGISTER 5
3089 020210 010005          MOV     R0,R5    ;PUT EXPECTED IN R5
3090 020212 116104 000005          MOV     5(R1),R4 ;PUT "FOUND" INTO R4
3091 020216 120504          CMP     R5,R4    ;DATA CORRECT?
3092 020220 001401          BEQ     65$      ;BR IF YES
3093 020222 104005          HLT     5        ;ERROR
3094 020224 104401          65$:          SCOP1          ;SW09=1?
3095 020226 000241          CLC          ;CLEAR CARRY
3096 020230 106100          ROL     R0       ;SHIFT BIT IN R0
3097 020232 001360          BNE     64$      ;IF R0=0 THEN DONE
3098 020234 012737 020250 001220      MOV     #67$,LOCK ;NEW SCOP1
3099 020242 012700 000001          MOV     #1,R0    ;START WITH BIT 0
3100 020246 005100          69$:          COM     R0       ;CHANGE TO FLOATING ZERO
3101 020250          67$:
3102 020250 010061 000004          MOV     R0,4(R1) ;PUT PATTERN INTO PORT4
3103 020254 104414          ROMCLK         ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3104 020256 122105          122100!5      ;MOV DATA TO IBUS REGISTER 5
3105 020260 104414          ROMCLK         ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3106 020262 021125          21005!<5*20> ;READ FROM IBUS REGISTER 5
3107 020264 010005          MOV     R0,R5    ;PUT EXPECTED IN R5
3108 020266 116104 000005          MOV     5(R1),R4 ;PUT "FOUND" INTO R4
3109 020272 120504          CMP     R5,R4    ;DATA CORRECT?
3110 020274 001401          BEQ     68$      ;BR IF YES
3111 020276 104005          HLT     5        ;ERROR
3112 020300 104401          68$:          SCOP1          ;SW09=1?
3113 020302 005100          COM     R0       ;CHANGE TO FLOATING 1
3114 020304 000241          CLC          ;CLEAR CARRY
3115 020306 106100          ROL     R0       ;SHIFT BIT IN R0
3116 020310 001356          BNE     69$      ;IF R0=0 THEN DONE
3117 020312 104400          SCOPE          ;SCOPE THIS TEST
3118
3119
3120          ;***** TEST 46 *****

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3121                                     ;*MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
3122                                     ;*FLOAT A 1 THROUGH IBUS REGISTER 6
3123                                     ;*FLOAT A 0 THROUGH IBUS REGISTER 6
3124                                     ;:*****
3125
3126                                     ; TEST 46
3127                                     -----
3128 020314 012737 000046 001226      TST46: MOV #46,TSTNO
3129 020322 012737 020470 001216      MOV #TST47,NEXT
3130 020330 012737 020350 001220      MOV #64$,LOCK
3131
3132 020336 104412                                     ;R1 CONTAINS BASE DMC11 ADDRESS
3133 020340 012702 000006      MSTCLR      ;MASTER CLEAR DMC11
3134 020344 012700 000001      MOV #6,R2   ;SAVE REGISTER ADDRESS FOR TYPEOUT
3135 020350                                     MOV #1,R0   ;START WITH BIT 0
3136 020350 010061 000004      64$: MOV R0,4(R1) ;PUT PATTERN INTO PORT4
3137 020354 104414      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3138 020356 122106      122100!6    ;MOV DATA TO IBUS REGISTER 6
3139 020360 104414      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3140 020362 021145      21005!<6*20> ;READ FROM IBUS REGISTER 6
3141 020364 010005      MOV R0,R5   ;PUT EXPECTED IN R5
3142 020366 116104 000005      MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
3143 020372 120504      CMPB R5,R4 ;DATA CORRECT?
3144 020374 001401      BEQ 65$   ;BR IF YES
3145 020376 104005      HLT 5    ;ERROR
3146 020400 104401      65$: SCOP1  ;SW09=1?
3147 020402 000241      CLC      ;CLEAR CARRY
3148 020404 106100      ROLB R0  ;SHIFT BIT IN R0
3149 020406 001360      BNE 64$  ;IF R0=0 THEN DONE
3150 020410 012737 020424 001220      MOV #67$,LOCK ;NEW SCOP1
3151 020416 012700 000001      MOV #1,R0   ;START WITH BIT 0
3152 020422 005100      69$: COM R0 ;CHANGE TO FLOATING ZERO
3153 020424      67$:
3154 020424 010061 000004      MOV R0,4(R1) ;PUT PATTERN INTO PORT4
3155 020430 104414      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3156 020432 122106      122100!6    ;MOV DATA TO IBUS REGISTER 6
3157 020434 104414      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3158 020436 021145      21005!<6*20> ;READ FROM IBUS REGISTER 6
3159 020440 010005      MOV R0,R5   ;PUT EXPECTED IN R5
3160 020442 116104 000005      MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
3161 020446 120504      CMPB R5,R4 ;DATA CORRECT?
3162 020450 001401      BEQ 68$   ;BR IF YES
3163 020452 104005      HLT 5    ;ERROR
3164 020454 104401      68$: SCOP1  ;SW09=1?
3165 020456 005100      COM R0   ;CHANGE TO FLOATING ;
3166 020460 000241      CLC      ;CLEAR CARRY
3167 020462 106100      ROLB R0  ;SHIFT BIT IN R0
3168 020464 001356      BNE 69$  ;IF R0=0 THEN DONE
3169 020466 104400      SCOPE   ;SCOPE THIS TEST
3170
3171
3172                                     ;***** TEST 47 *****
3173                                     ;*MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
3174                                     ;*FLOAT A 1 THROUGH IBUS REGISTER 7
3175                                     ;*FLOAT A 0 THROUGH IBUS REGISTER 7
3176                                     ;:*****

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3179
3180 020470 012737 000047 001226
3181 020476 012737 020644 001216
3182 020504 012737 020524 001220
3183
3184 020512 104412
3185 020514 012702 000007
3186 020520 012700 000001
3187 020524
3188 020524 010061 000004
3189 020530 104414
3190 020532 122107
3191 020534 104414
3192 020536 021165
3193 020540 010005
3194 020542 116104 000005
3195 020546 120504
3196 020550 001401
3197 020552 104005
3198 020554 104401
3199 020556 000241
3200 020560 106100
3201 020562 001360
3202 020564 012737 020600 001220
3203 020572 012700 000001
3204 020576 005100
3205 020600
3206 020600 010061 000004
3207 020604 104414
3208 020606 122107
3209 020610 104414
3210 020612 021165
3211 020614 010005
3212 020616 116104 000005
3213 020622 120504
3214 020624 001401
3215 020626 104005
3216 020630 104401
3217 020632 005100
3218 020634 000241
3219 020636 106100
3220 020640 001356
3221 020642 104400
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3232 020644 012737 000050 001226

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; TEST 47
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TST47: MOV #47,TSTNO
MOV #TST50,NEXT
MOV #64$,LOCK
;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;SAVE REGISTER ADDRESS FOR TYPEOUT
;START WITH BIT 0
MSTCLR
MOV #7,R2
MOV #1,R0
64$: MOV R0,4(R1) ;PUT PATTERN INTO PORT4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!7 ;MOV DATA TO IBUS REGISTER 7
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!(<7*20) ;READ FROM IBUS REGISTER 7
MOV R0,R5 ;PUT EXPECTED IN R5
MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 65$ ;BR IF YES
HLT 5 ;ERROR
65$: SCOP1 ;SW09=1?
CLC ;CLEAR CARRY
ROLB R0 ;SHIFT BIT IN R0
BNE 64$ ;IF R0=0 THEN DONE
MOV #67$,LOCK ;NEW SCOP1
MOV #1,R0 ;START WITH BIT 0
COM R0 ;CHANGE TO FLOATING ZERO
67$: MOV R0,4(R1) ;PUT PATTERN INTO PORT4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
122100!7 ;MOV DATA TO IBUS REGISTER 7
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
21005!(<7*20) ;READ FROM IBUS REGISTER 7
MOV R0,R5 ;PUT EXPECTED IN R5
MOVB 5(R1),R4 ;PUT "FOUND" INTO R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 68$ ;BR IF YES
HLT 5 ;ERROR
68$: SCOP1 ;SW09=1?
COM R0 ;CHANGE TO FLOATING 1
CLC ;CLEAR CARRY
ROLB R0 ;SHIFT BIT IN R0
BNE 69$ ;IF R0=0 THEN DONE
SCOPE ;SCOPE THIS TEST

;***** TEST 50 *****
;*MICRO PROCESSOR IBUS DUAL ADDRESS TEST
;*WRITE ALL IBUS REGISTERS WITH INCREMENTING PATTERN
;*READ ALL IBUS REGISTERS TO VERIFY CORRECT ADDRESSING
;*****

; TEST 50
-----
TST50: MOV #50,TSTNO

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DMC11 MICRO PROCESSOR IBUS TESTS

3233	020652	012737	021072	001216	MOV	#TST51,NEXT	
3234	020660	012737	020676	001220	MOV	#1\$,LOCK	
3235							:R1 CONTAINS BASE DMC11 ADDRESS
3236	020666	104412			MSTCLR		:MASTER CLEAR DMC11
3237	020670	012700	000001		MOV	#1,R0	:START WITH A ONE
3238	020674	005002			CLR	R2	:R2 CONTAINS ADDRESS OF REGISTER
3239	020676	010203			MOV	R2,R3	:R3=REGISTER ADDRESS
3240	020700	010061	000004		MOV	R0,4(R1)	:WRITE DATA TO PORT4
3241	020704	042737	000017	020720	BIC	#17,5\$:CLEAR ADDRESS FIELD OF INSTRUCTION
3242	020712	050337	020720		BIS	R3,5\$:ADD ADDRESS TO INSTRUCTION
3243	020716	104414			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3244	020720	122100			122100		:MOVE DATA TO IBUS REGISTER
3245	020722	006303			ASL	R3	:SHIFT ADDRESS
3246	020724	006303			ASL	R3	:4 TIMES TO GET
3247	020726	006303			ASL	R3	:IT TO BITS 4-7
3248	020730	006303			ASL	R3	:OF NEXT INSTRUCTION
3249	020732	042737	000360	020746	BIC	#360,6\$:CLEAR ADDRESS FIELD
3250	020740	050337	020746		BIS	R3,6\$:ADD ADDRESS TO INSTRUCTION
3251	020744	104414			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3252	020746	021005			21005		:READ FROM IBUS REGISTER
3253	020750	010005			MOV	R0,R5	:PUT "EXPECTED" IN R5
3254	020752	116104	000005		MOV#B	5(R1),R4	:PUT "FOUND" IN R4
3255	020756	120504			CMP#B	R5,R4	:IS DATA CORRECT?
3256	020760	001401			BEQ	2\$:BR IF YES
3257	020762	104005			HLT	5	:DATA ERROR
3258	020764	104401			2\$:	SCOPE1	:SW09=1?
3259	020766	005200			INC	R0	:INCREMENT PATTERN
3260	020770	005202			INC	R2	:INCREMENT REGISTER ADDRESS
3261	020772	022702	000010		CMP	#7+1,R2 ;LAST ADDRESS DONE?	
3262	020776	001337			BNE	1\$:BR IF NO
3263	021000	012737	021016	001220	MOV	#3\$,LOCK	:NEW SCOPE1
3264	021006	012700	000001		MOV	#1,R0	:RESTART PATTERN TO 1
3265	021012	005002			CLR	R2	:RESTART AT ADDRESS 0
3266	021014	005003			CLR	R3	:RESTART AT ADDRESS 0
3267	021016	042737	000360	021032	BIC	#360,7\$:CLEAR ADDRESS FIELD OF INSTRUCTION
3268	021024	050337	021032		BIS	R3,7\$:ADD ADDRESS TO INSTRUCTION
3269	021030	104414			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3270	021032	021005			21005		:READ FROM IBUS REGISTER
3271	021034	010005			MOV	R0,R5	:PUT "EXPECTED" IN R5
3272	021036	116104	000005		MOV#B	5(R1),R4	:PUT "FOUND" IN R4
3273	021042	120504			CMP#B	R5,R4	:DATA CORRECT?
3274	021044	001401			BEQ	4\$:BR IF YES
3275	021046	104005			HLT	5	:DUAL ADDRESSING ERROR
3276	021050	104401			4\$:	SCOPE1	:SW09=1?
3277	021052	005200			INC	R0	:INCREMENT PATTERN
3278	021054	005202			INC	R2	:NEXT ADDRESS
3279	021056	062703	000020		ADD	#20,R3	:ADD 1 TO ADDRESS IN R3 (SHIFTED 4 TIMES)
3280	021062	022702	000010		CMP	#7+1,R2 ;LAST ADDRESS DONE?	
3281	021066	001353			BNE	3\$:BR IF NO
3282	021070	104400			SCOPE		:SCOPE THIS TEST
3283							
3284							
3285							:***** TEST 51 *****
3286							:*MICRO PROCESSOR BR REGISTER TEST
3287							:*FLOAT A 1 THROUGH THE BR
3288							:*FLOAT A 0 THROUGH THE BR

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3289 ;:*****
3290 ;
3291 ; TEST 51
3292 ;-----
3293 021072 012737 000051 001226 TST51: MOV #51,TSTNO
3294 021100 012737 021242 001216 MOV #TST52,NEXT
3295 021106 012737 021122 001220 MOV #64$,LOCK
3296 ;
3297 021114 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
3298 021116 012700 000001 MOV #1,R0 ;MASTER CLEAR DMC11
3299 021122 64$: ;START PATTERN WITH BIT0
3300 021122 010061 000004 MOV RO,4(R1) ;WRITE PATTERN IN PORT4
3301 021126 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3302 021130 120500 120500 ;MOVE DATA TO THE BR REGISTER
3303 021132 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3304 021134 061225 061225 ;MOVE BR TO PORT 5
3305 021136 010005 MOV RO,R5 ;PUT "EXPECTED" IN R5
3306 021140 116104 000005 MOVB 5(R1),R4 ;PUT "FOUND" IN R4
3307 021144 120504 CMPB R5,R4 ;DATA CORRECT?
3308 021146 001401 BEQ 65$ ;BR IF YES
3309 021150 104006 HLT 6 ;DATA ERROR
3310 021152 104401 65$: SCOP1
3311 021154 000241 CLC ;CLEAR CARRY
3312 021156 106100 ROLB RO ;SHIFT BIT IN RO
3313 021160 001360 BNE 64$ ;DONE IF RO=0
3314 021162 012737 021176 001220 MOV #67$,LOCK ;NEW SCOP1
3315 021170 012700 000001 MOV #1,R0 ;START PATTERN WITH BIT0
3316 021174 005100 69$: COM RO ;CHANGE TO FLOATING ZERO
3317 021176 67$:
3318 021176 010061 000004 MOV RO,4(R1) ;WRITE PATTERN IN PORT4
3319 021202 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3320 021204 120500 120500 ;MOVE DATA TO THE BR REGISTER
3321 021206 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3322 021210 061225 061225 ;MOVE BR TO PORT 5
3323 021212 010005 MOV RO,R5 ;PUT "EXPECTED" IN R5
3324 021214 116104 000005 MOVB 5(R1),R4 ;PUT "FOUND" IN R4
3325 021220 120504 CMPB R5,R4 ;DATA CORRECT?
3326 021222 001401 BEQ 68$ ;BR IF YES
3327 021224 104006 HLT 6 ;DATA ERROR
3328 021226 104401 68$: SCOP1
3329 021230 005100 COM RO ;CHANGE BACK TO ONE
3330 021232 000241 CLC ;CLEAR CARRY
3331 021234 106100 ROLB RO ;SHIFT BIT IN RO
3332 021236 001356 BNE 69$ ;DONE IF RO=0
3333 021240 104400 SCOPE ;SCOPE THIS TEST
3334
3335
3336 ;:***** TEST 52 *****
3337 ;*SCRATCH PAD TEST
3338 ;*FLOAT A 1 THROUGH EACH SCRATCH PAD LOCATION
3339 ;*FLOAT A 0 THROUGH EACH SCRATCH PAD LOCATION
3340 ;:*****
3341 ;
3342 ; TEST 52
3343 ;-----
3344 021242 012737 000052 001226 TST52: MOV #52,TSTNO

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3345 021250 012737 021510 001216 MOV #TST53,NEXT
3346 021256 012737 021274 001220 MOV #64$,LOCK
3347
3348 021264 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
3349 021266 005002 CLR R2 ;MASTER CLEAR DMC11
3350 021270 012700 000001 MOV #1,R0 ;START AT ADDRESS ZERO
3351 021274 042737 000017 021314 64$: BIC #17,65$ ;START WITH BIT0
3352 021302 050237 021314 BIC #17,65$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
3353 021306 010061 000004 MOV R2,65$ ;ADD ADDRESS TO INSTRUCTION
3354 021312 104414 ROMCLK R0,4(R1) ;WRITE PATTERN TO PORT4
3355 021314 123100 65$: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3356 021316 042737 000017 021332 BIC #17,66$ ;WRITE SCRATCH PAD(ADDRESS IN R2)
3357 021324 050237 021332 BIS R2,66$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
3358 021330 104414 ROMCLK ;ADD ADDRESS TO INSTRUCTION
3359 021332 040600 66$: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3360 021334 104414 ROMCLK ;MOV SP TO BR
3361 021336 061225 061225 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3362 021340 010005 MOV R0,R5 ;MOVE BR TO PORT5
3363 021342 116104 000005 MOV #5(R1),R4 ;PUT "EXPECTED" IN R5
3364 021346 120504 CMPB R5,R4 ;PUT "FOUND" IN R4
3365 021350 001401 BEQ 67$ ;DATA CORRECT
3366 021352 104007 HLT 7 ;BR IF YES
3367 021354 104401 67$: SCOPI ;DATA ERROR
3368 021356 000241 CLC ;SW09=1?
3369 021360 106100 ROLB R0 ;CLEAR CARRY
3370 021362 001344 BNE 64$ ;SHIFT BIT IN R0
3371 021364 012737 021400 001220 MOV #69$,LOCK ;DONE IF R0=0
3372 021372 012700 000001 MOV #1,R0 ;NEW SCOPI
3373 021376 005100 73$: COM R0 ;START WITH BIT0
3374 021400 042737 000017 021420 69$: BIC #17,70$ ;CHANGE TO FLOATING ZERO
3375 021406 050237 021420 BIS R2,70$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
3376 021412 010061 000004 MOV R0,4(R1) ;ADD ADDRESS TO INSTRUCTION
3377 021416 104414 ROMCLK ;WRITE PATTERN TO PORT4
3378 021420 123100 70$: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3379 021422 042737 000017 021436 BIC #17,71$ ;WRITE SCRATCH PAD(ADDRESS IN R2)
3380 021430 050237 021436 BIS R2,71$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
3381 021434 104414 ROMCLK ;ADD ADDRESS TO INSTRUCTION
3382 021436 040600 71$: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3383 021440 104414 ROMCLK ;MOV SP TO BR
3384 021442 061225 061225 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3385 021444 010005 MOV R0,R5 ;MOVE BR TO PORT5
3386 021446 116104 000005 MOV #5(R1),R4 ;PUT "EXPECTED" IN R5
3387 021452 120504 CMPB R5,R4 ;PUT "FOUND" IN R4
3388 021454 001401 BEQ 72$ ;DATA CORRECT
3389 021456 104007 HLT 7 ;BR IF YES
3390 021460 104401 72$: SCOPI ;DATA ERROR
3391 021462 005100 COM R0 ;SW09=1?
3392 021464 000241 CLC ;CHANGE BACK TO A ONE
3393 021466 106100 ROLB R0 ;CLEAR CARRY
3394 021470 001342 BNE 73$ ;SHIFT BIT IN R0
3395 021472 012700 000001 MOV #1,R0 ;DONE IF R0=0
3396 021476 005202 INC R2 ;RESTART AT BIT 0
3397 021500 022702 000020 CMP #20,R2 ;NEXT SP ADDRESS
3398 021504 001273 BNE 64$ ;LAST ADDRESS?
3399 021506 104400 SCOPE ;BR IF NO
3400 ;SCOPE THIS TEST
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021510 012737 000053 001226
021516 012737 021732 001216
021524 012737 021542 001220

021532 104412
021534 012700 000001
021540 005003
021542 010302
021544 042737 000017 021564
021552 050237 021564
021556 010061 000004
021562 104414
021564 123100
021566 042737 000017 021602
021574 050237 021602
021600 104414
021602 060600
021604 104414
021606 061225
021610 010005
021612 116104 000005
021616 120504
021620 001401
021622 104007
021624 104401
021626 005200
021630 005203
021632 022703 000020
021636 001341
021640 012737 021654 001220
021646 012700 000001
021652 005003
021654 010302
021656 042737 000017 021672
021664 050237 021672
021670 104414
021672 060600
021674 104414
021676 061225
021700 010005
021702 116104 000005
021706 120504
021710 001401
021712 104007
021714 104401
021716 005200
021720 005203

TST53:

1\$:

2\$:

3\$:

4\$:

5\$:

6\$:

7\$:

```
***** TEST 53 *****  
;SCRATCH PAD DUAL ADDRESSING TEST  
;WRITE AN INCREMENTING PATTERN IN ALL SP LOCATIONS  
;READ ALL SP LOCATIONS TO VERIFY CORRECT ADDRESSING  
*****  
  
; TEST 53  
-----  
MOV #53,TSTNO  
MOV #TST54,NEXT  
MOV #1$,LOCK  
  
MSTCLR  
MOV #1,R0  
CLR R3  
1$: MOV R3,R2  
BIC #17,2$  
BIS R2,2$  
MOV R0,4(R1)  
ROMCLK  
2$: 123100  
BIC #17,3$  
BIS R2,3$  
ROMCLK  
3$: 60600  
ROMCLK  
61225  
MOV R0,R5  
MOV 5(R1),R4  
CMPB R5,R4  
BEQ 4$  
HLT 7  
4$: SCOP1  
INC R0  
INC R3  
CMP #20,R3  
BNE 1$  
MOV #5$,LOCK  
MOV #1,R0  
CLR R3  
5$: MOV R3,R2  
BIC #17,6$  
BIS R2,6$  
ROMCLK  
6$: 60600  
ROMCLK  
61225  
MOV R0,R5  
MOV 5(R1),R4  
CMPB R5,R4  
BEQ 7$  
HLT 7  
7$: SCOP1  
INC R0  
INC R3
```

```
;R1 CONTAINS BASE DMC11 ADDRESS  
;MASTER CLEAR DMC11  
;START WITH A 1  
;ADDRESS 0  
;MOVE ADDRESS TO R2  
;CLEAR ADDRESS FIELD  
;ADD ADDRESS TO INSTRUCTION  
;WRITE PATTERN TO PORT4  
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
;WRITE SP(ADDRESS IN R2)  
;CLEAR ADDRESS FIELD OF INSTRUCTION  
;ADD ADDRESS TO INSTRUCTION  
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
;MOV SP TO BR  
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
;MOV BR TO PORT5  
;PUT "EXPECTED" IN R5  
;PUT "FOUND" IN R4  
;DATA CORRECT?  
;BR IF YES  
;DATA ERROR  
;SW09=0  
;INCREMENT PATTERN  
;NEXT ADDRESS  
;LAST ADDRESS DONE?  
;BR IF NO  
;NEW SCOP1  
;RESTART PATTERN AT 1  
;RESTART AT ADDRESS ZERO  
;PUT ADDRESS IN R2  
;CLEAR ADDRESS FIELD OF INSTRUCTION  
;ADD ADDRESS TO INSTRUCTION  
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
;MOV SP TO BR  
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
;MOV BR TO PORT5  
;PUT "EXPECTED" IN R5  
;PUT "FOUND" IN R4  
;DATA CORRECT?  
;BR IF YES  
;SP ADDRESSING ERROR  
;SW09=1?  
;INCREMENT PATTERN  
;NEXT ADDRESS
```

```

3457 021722 022703 000020
3458 021726 001352
3459 021730 104400
3460
3461
3462
3463
3464
3465
3466
3467
3468
3469 021732 012737 000054 001226
3470 021740 012737 022026 001216
3471
3472 021746 000005
3473 021750 005011
3474 021752 004537 034600
3475 021756 022020
3476 021760 022016
3477 021762 340 340
3478 021764 012737 000340 177776
3479 021772 012761 000200 000004
3480 022000 104414
3481 022002 121111
3482 022004 005037 177776
3483 022010 000240
3484 022012 104010
3485 022014 000403
3486 022016 104011
3487 022020 012706 001200
3488 022024 104400
3489
3490
3491
3492
3493
3494
3495
3496
3497
3498 022026 012737 000055 001226
3499 022034 012737 022120 001216
3500
3501 022042 104412
3502 022044 004537 034600
3503 022050 022110
3504 022052 022112
3505 022054 340 340
3506 022056 012737 000340 177776
3507 022064 012761 000300 000004
3508 022072 104414
3509 022074 121111
3510 022076 005037 177776
3511 022102 000240
3512 022104 104010

```

```

CMP #20,R3 ;LAST ADDRESS DONE?
BNE 55 ;BR IF NO
SCOPE ;SCOPE THIS TEST

```

```

;***** TEST 54 *****
;*INTERRUPT TEST
;*TEST THAT DEVICE CAN INTERRUPT TO VECTOR A
;*****

```

; TEST 54

```

-----
TST54: MOV #54,TSTNO
MOV #TST55,NEXT
;R1 CONTAINS BASE DMC11 ADDRESS
;BUS RESET
;CLEAR RUN
;SET UP VECTORS
;XX0
;XX4
;LEVEL 7
;PS = LEVEL 7
;WRITE PORT4
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;SET BR RQ IN IBUS* REG 11
;ALLOW INTERRUPT

1S: .BYTE 340,340
MOV #340,PS
MOV #200,4(R1)
ROMCLK
121111
CLR PS
NOP
HLT 10 ;NO INTERRUPT
BR 4S
2S: HLT 11 ;WRONG VECTOR
3S: MOV #STACK,SP ;RESET STACK
4S: SCOPE ;SCOPE THIS TEST

```

```

;***** TEST 55 *****
;*INTERRUPT TEST
;*TEST THAT DEVICE CAN INTERRUPT TO VECTOR B
;*****

```

; TEST 55

```

-----
TST55: MOV #55,TSTNO
MOV #TST56,NEXT
;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;SET UP VECTORS
;XX0
;XX4
;LEVEL 7
;PS = LEVEL 7
;WRITE PORT4
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;SET BR RQ IN IBUS* REG 11
;ALLOW INTERRUPT

1S: .BYTE 340,340
MOV #340,PS
MOV #300,4(R1)
ROMCLK
121111
CLR PS
NOP
HLT 10 ;NO INTERRUPT

```

```

3513 022106 000403
3514 022110 104011
3515 022112 012706 001200
3516 022116 104400
3517
3518
3519
3520
3521
3522
3523
3524
3525
3526
3527 022120 012737 000056 001226
3528 022126 012737 022240 001216
3529
3530 022134 104412
3531 022136 012702 000340
3532 022142 010237 177776
3533 022146 013700 001366
3534 022152 006200
3535 022154 006200
3536 022156 006200
3537 022160 006200
3538 022162 042700 177437
3539 022166 004537 034600
3540 022172 022234
3541 022174 022234
3542 022176 340 340
3543 022200 012761 000200 000004
3544 022206 104414
3545 022210 121111
3546 022212 010237 177776
3547 022216 000240
3548 022220 020002
3549 022222 001403
3550 022224 162702 000040
3551 022230 000770
3552 022232 104400
3553 022234 104020
3554 022236 000002
3555
3556
3557
3558
3559
3560
3561
3562
3563
3564
3565 022240 012737 000057 001226
3566 022246 012737 022404 001216
3567
3568 022254 104412

```

```

BR 45
25: HLT 11 ;WRONG VECTOR
35: MOV #STACK,SP ;RESET STACK
45: SCOPE ;SCOPE THIS TEST

```

```

***** TEST 56 *****
*PRIORITY INTERRUPT TESTS
*SET PS TO ALL BR LEVELS EQUAL OR GREATER THAN
*THE DMC11 LEVEL, VERIFY THAT DMC11 DOES NOT INTERRUPT
*****
; TEST 56
-----
TST56: MOV #56,TSTNO
MOV #TST57,NEXT
MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
MOV #340,R2 ;PUT LEVEL 7 IN R2
MOV R2,PS ;SET PRIORITY TO 7
MOV STAT1,R0 ;GET BR LEVEL OF DMC11
ASR R0 ;SHIFT R0 4 TIMES
ASK R0 ;TO GET PROPER LEVEL
ASR R0
ASR R0
BIC #177437,R0 ;CLEAR UNWANTED BITS
JSR R5,SETVEC ;SET UP VECTORS
25 ;A VECTOR
25 ;B VECTOR
;BYTE 340,340 ;PRIORITY 7
MOV #200,4(R1) ;LOAD PORT4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121111 ;SET BR REQUEST
55: MOV R2,PS ;PUT LEVEL IN R2 IN PS
NOP
CMP R0,R2 ;IS PRESENT PS LEVEL = TO DMC LEVEL
BEQ 15 ;BR IF YES
SUB #40,R2 ;NO GET NEXT LOWER LEVEL IN R2
BR 55 ;AND CONTINUE WITH TEST
15: SCOPE ;SCOPE THIS TEST
25: HLT 20 ;ERROR UNEXPECTED INTERRUPT
RTI

```

```

***** TEST 57 *****
*PRIORITY INTERRUPT TESTS
*SET PS TO ALL BR LEVELS LESS THAN THE DMC11 LEVEL
*VERIFY THAT THE DMC11 WILL INTERRUPT
*****
; TEST 57
-----
TST57: MOV #57,TSTNO
MOV #TST60,NEXT
MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11

```

```

3569 022256 012702 000340      MOV      #340,R2      ;PUT LEVEL 7 IN R2
3570 022262 010237 177776      MOV      R2,PS       ;SET PRIORITY TO 7
3571 022266 013700 001366      MOV      STAT1,R0    ;GET BR LEVEL OF DMC11
3572 022272 006200             ASR      R0          ;SHIFT R0 4 TIMES
3573 022274 006200             ASR      R0          ;TO GET PROPER LEVEL
3574 022276 006200             ASR      R0
3575 022300 006200             ASR      R0
3576 022302 042700 177437      BIC      #177437,R0  ;CLEAR UNWANTED BITS
3577 022306 010002             MOV      R0,R2       ;PUT DMC LEVEL IN R2
3578 022310 162702 000040      SUB      #40,R2      ;GET NEXT LOWER LEVEL IN R2
3579 022314 004537 034600      JSR      R5,SETVEC   ;SET UP VECTORS
3580 022320 022366             2$        ;A VECTOR
3581 022322 022374             3$        ;B VECTOR
3582 022324             340      340      .BYTE     340,340    ;PRIORITY 7
3583 022326 012761 000200 000004 4$:      MOV      #200,4(R1)  ;LOAD PORT4
3584 022334 104414             ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3585 022336 121111             121111    ;SET BR REQUEST
3586 022340 010237 177776      5$:      MOV      R2,PS       ;PUT LEVEL IN R2 IN PS
3587 022344 000240             NOP
3588 022346 104010             HLT      10          ;ERROR, NO INTERRUPT
3589 022350 622702 000140      6$:      CMP      #140,R2    ;IS IT DOWN TO LEVEL 3 YET?
3590 022354 001403             BEQ      1$          ;YES,DMC DID NOT INTERRUPT, ERROR
3591 022356 162702 000040      SUB      #40,R2      ;PUT NEXT LOWER LEVEL IN R2
3592 022362 000761             BR       4$          ;CONTINUE TEST
3593 022364 104400             1$:      SCOPE
3594 022366 012716 022350      2$:      MOV      #6$, (SP)  ;SCOPE THIS TEST
3595 022372 000002             RTI
3596 022374 104011             3$:      HLT      11          ;ERROR, WRONG VECTOR
3597 022376 012716 022350      MOV      #6$, (SP)  ;SET UP FOR RTI
3598 022402 000002             RTI

```

```

;***** TEST 60 *****
;NPR TEST
;TEST OF DATO, 1 WORD FROM UPROC TO 11 MEMORY
;*****

```

TEST 60

```

3607
3608 022404 012737 000060 001226  TST60:  MOV      #60,TSTNO
3609 022412 012737 022510 001216      MOV      #TST61,NEXT
3610
3611 022420 000005             RESET
3612 022422 005011             CLR      (R1)        ;R1 CONTAINS BASE DMC11 ADDRESS
3613 022424 005061 000004      CLR      4(R1)       ;BUS RESET
3614 022430 004537 034622      JSR      R5,NPRSET   ;CLEAR RUN
3615 022434 000000             0          ;CLR PORT4
3616 022436 177777             -1        ;SET UP IBUS REG 0-7
3617 022440 022506             3$        ;IN DATA
3618 022442 022504             2$        ;OUT DATA
3619 022444 005037 022504      CLR      2$          ;IN BA
3620 022450 012761 000021 000004  MOV      #21,4(R1)   ;OUT BA
3621 022456 104414             ROMCLK    ;CLEAR 2$
3622 022460 121110             121110    ;WRITE PORT4
3623 022462 000240             NOP        ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3624 022464 012705 177777      MOV      #-1,R5     ;SET NPR BITS IN IBUS* REG 11
                       ;PUT "EXPECTED" IN R5

```

```

3625 022470 013704 022504      MOV      2$,R4      ;PUT "FOUND" IN R4
3626 022474 020504              CMP      R5,R4      ;DATA CORRECT?
3627 022476 001401              BEQ      4$          ;BR IF YES
3628 022500 104012              HLT      12          ;ERROR NPR FAILED
3629 022502 104400              4$:      SCOPE      ;SCOPE THIS TEST
3630 022504 000000              2$:      0           ;OUT BA
3631 022506 000000              3$:      0           ;IN BA
3632
3633
3634 ;***** TEST 61 *****
3635 ;*NPR TEST
3636 ;*TEST OF DAT1, 1 WORD FROM 11 MEMORY TO UPROC
3637 ;*****
3638
3639 ; TEST 61
3640 ;-----
3641 022510 012737 000061 001226      TST61:  MOV      #61,TSTNO
3642 022516 012737 022624 001216      MOV      #TST62,NEXT
3643
3644 022524 104412              MSTCLR              ;R1 CONTAINS BASE DMC11 ADDRESS
3645 022526 005061 000004              CLR      4(R1)      ;MASTER CLEAR DMC11
3646 022532 004537 034622              JSR      R5,NPRSET  ;CLR PORT4
3647 022536 000000              0                ;SET UP IBUS REG 0-7
3648 022540 177777              -1              ;IN DATA
3649 022542 022622              3$              ;OUT DATA
3650 022544 022620              2$              ;IN BA
3651 022546 012737 177777 022622      MOV      #-1,3$    ;OUT BA
3652 022554 012761 000001 000004      MOV      #1,4(R1)  ;PUT DATA IN 3$
3653 022562 104414              ROMCLK          ;WRITE PORT4
3654 022564 121110              121110          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3655 022566 000240              NOP              ;SET NPR BITS IN IBUS* REG 11
3656 022570 012705 177777      MOV      #-1,R5    ;PUT "EXPECTED" IN R5
3657 022574 104414              ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3658 022576 021004              021004          ;MOVE IN DATA LOW BYTE TO PORT4
3659 022600 104414              ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3660 022602 021025              021025          ;MOVE IN DATA HIGH BYTE TO PORT5
3661 022604 016104 000004      MOV      4(R1),R4  ;PUT "FOUND" IN R4
3662 022610 020504              CMP      R5,R4      ;DATA CORRECT?
3663 022612 001401              BEQ      4$          ;BR IF YES
3664 022614 104012              HLT      12          ;ERROR NPR FAILED
3665 022616 104400              4$:      SCOPE      ;SCOPE THIS TEST
3666 022620 000000              2$:      0           ;OUT BA
3667 022622 000000              3$:      0           ;IN BA
3668
3669
3670 ;***** TEST 62 *****
3671 ;*NPR TEST
3672 ;*TEST OF DAT08, 1 BYTE FROM UPROC TO 11 MEMORY
3673 ;*****
3674
3675 ; TEST 62
3676 ;-----
3677 022624 012737 000062 001226      TST62:  MOV      #62,TSTNO
3678 022632 012737 022726 001216      MOV      #TST63,NEXT
3679
3680 022640 104412              MSTCLR              ;R1 CONTAINS BASE DMC11 ADDRESS

```

3681	022642	005061	000004		CLR	4(R1)	: CLR PORT4
3682	022646	004537	034622		JSR	R5,NPRSET	: SET UP IBUS REG 0-7
3683	022652	000000			0		: IN DATA
3684	022654	177777			-1		: OUT DATA
3685	022656	022724			3\$: IN BA
3686	022660	022723			2\$+1	: OUT BA	
3687	022662	005037	022722		CLR	2\$: CLEAR 2\$
3688	022666	012761	000221	000004	MOV	#221,4(R1)	: WRITE PORT4
3689	022674	104414			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3690	022676	121110			121110		: SET NPR BITS IN IBUS* REG 11
3691	022700	000240			NOP		
3692	022702	012705	177400		MOV	#177400,R5	: PUT "EXPECTED" IN R5
3693	022706	013704	022722		MOV	2\$,R4	: PUT "FOUND" IN R4
3694	022712	020504			CMP	R5,R4	: DATA CORRECT?
3695	022714	001401			BEQ	4\$: BR IF YES
3696	022716	104012			HLT	12	: ERROR NPR FAILED
3697	022720	104400		4\$:	SCOPE		: SCOPE THIS TEST
3698	022722	000000		2\$:	0		: OUT BA
3699	022724	000000		3\$:	0		: IN BA
3700							
3701							
3702							: ***** TEST 63 *****
3703							: *TEST OF EA BITS 16 AND 17
3704							: *DO A DATO TO AN ADDRESS USING OUT BA BITS 16 AND 17
3705							: *VERIFY CORRECT RESULTS
3706							: *****
3707							
3708							: TEST 63
3709							
3710	022726	012737	000063	001226	TST63:	MOV	#63,TSTNO
3711	022734	012737	023064	001216		MOV	#TST64,NEXT
3712							: R1 CONTAINS BASE DMC11 ADDRESS
3713	022742	104412			MSTCLR		: MASTER CLEAR DMC11
3714	022744	013737	001412	022772	MOV	DMP04,1\$: USE SEL4 FOR ADDRESS
3715	022752	013737	001412	022770	MOV	DMP04,2\$: USE SEL4 FOR ADDRESS
3716	022760	004537	034622		JSR	R5,NPRSET	: LOAD BA AND DATA
3717	022764	000000			0		: IN DATA
3718	022766	125252			125252		: OUT DATA
3719	022770	000000			0		: IN BA
3720	022772	000000			0		: OUT BA
3721	022774	012761	000014	000004	MOV	#14,4(R1)	: LOAD SEL 4 WITH OUT BA16 AND 17
3722	023002	104414			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3723	023004	121111			121111		: SET OUTBA 16 AND 17
3724	023006	012761	000021	000004	MOV	#21,4(R1)	: LOAD SEL4
3725	023014	012761	121110	000006	MOV	#121110,6(R1)	: PUT INSTRUCTION IN SEL6
3726	023022	012711	003000		MOV	#BIT9!BIT10,(R1)	: SET CROMI AND CROMO!!
3727	023026	052711	000400		BIS	#BIT8,(R1)	: CLOCK IT!
3728	023032	000240			NOP		: WAIT FOR NPR
3729	023034	012705	121110		MOV	#121110,R5	: PUT "EXPECTED" IN R5
3730	023040	104414			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3731	023042	021044			021044		: MOVE OUT DATA LB TO SEL4
3732	023044	104414			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3733	023046	021065			021065		: MOVE OUT DATA HB TO SEL5
3734	023050	016104	000004		MOV	4(R1),R4	: PUT "FOUND" IN R4
3735	023054	020504			CMP	R5,R4	: CORRECT RESULTS ?
3736	023056	001401			BEQ	3\$: BR IF YES

```

3737 023060 104012
3738 023062 104400
3739
3740
3741
3742
3743
3744
3745
3746
3747
3748
3749 023064 012737 000064 001226
3750 023072 012737 023210 001216
3751
3752 023100 104412
3753 023102 013737 001412 023130
3754 023110 013737 001412 023126
3755 023116 004537 034622
3756 023122 000000
3757 023124 125252
3758 023126 000000
3759 023130 000000
3760 023132 012761 000015 000004
3761 023140 012761 121110 000006
3762 023146 012711 003000
3763 023152 052711 000400
3764 023156 000240
3765 023160 012705 121110
3766 023164 104414
3767 023166 021004
3768 023170 104414
3769 023172 021025
3770 023174 016104 000004
3771 023200 020504
3772 023202 001401
3773 023204 104012
3774 023206 104400
3775
3776
3777
3778
3779
3780
3781
3782
3783
3784
3785 023210 012737 000065 001226
3786 023216 012737 023320 001216
3787
3788 023224 104412
3789 023226 004537 034622
3790 023232 000000
3791 023234 000000
3792 023236 177320

```

```

3$:
TST64:
2$:
1$:
3$:
TST65:

```

```

HLT 12 ;ERROR BA 16 AND 17 FAILED
SCOPE ;SCOPE THIS TEST

:***** TEST 64 *****
:*TEST OF EA BITS 16 AND 17
:*DO A DATI USING IN BA BITS 16 AND 17
:*VERIFY CORRECT RESULTS
:*****

: TEST 64
-----
MOV #64,TSTNO
MOV #TST65,NEXT
MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
MOV DMP04,1$ ;MASTER CLEAR DMC11
MOV DMP04,2$ ;USE SEL4 FOR ADDRESS
JSR R5,NPRSET ;LOAD BA AND DATA
0 ;IN DATA
125252 ;OUT DATA
0 ;IN BA
0 ;OUT BA
MOV #15,4(R1) ;LOAD SEL4
MOV #121110,6(R1) ;PUT INSTRUCTION IN SEL6
MOV #BIT9:BIT10,(R1) ;SET CROMI AND CROMO!!
BIS #BIT8,(R1) ;CLOCK IT!
NOP ;WAIT FOR NPR
MOV #121110,R5 ;PUT "EXPECTED" IN R5
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
021004 ;MOVE IN DATA LB TO SEL4
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
021025 ;MOVE IN DATA HB TO SEL5
MOV 4(R1),R4 ;PUT "FOUND" IN R4
CMP R5,R4 ;CORRECT RESULTS ?
BEQ 3$ ;BA IF YES
HLT 12 ;ERROR BA 16 AND 17 FAILED
SCOPE ;SCOPE THIS TEST

:***** TEST 65 *****
:*NPR NON-EXISTENT MEMORY TEST
:*DO A DATO TO A NON-EXISTENT ADDRESS
:*VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11
:*****

: TEST 65
-----
MOV #65,TSTNO
MOV #TST66,NEXT
MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
JSR R5,NPRSET ;MASTER CLEAR DMC11
0 ;LOAD IBUS REGISTERS 0-7
0 ;IN DATA
0 ;OUT DATA
177320 ;IN BA

```

3793	023240	177320			177320	:OUT BA
3794	023242	012761	000014	000004	MOV #14,4(R1)	:SET OUT BA BITS 16+17 IN PORT4
3795	023250	104414			ROMCLK	:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3796	023252	121111			121111	:SET OUTBA 16 AND 17
3797	023254	012761	000021	000004	MOV #21,4(R1)	:SET NPR REQUEST BITS IN PORT4
3798	023262	104414			ROMCLK	:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3799	023264	121110			121110	:MOV IBUS* 4 TO IBUS* 10
3800	023266	000240			NOP	
3801	023270	104414			ROMCLK	:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3802	023272	121225			121225	:MOV IBUS*11 TO IBUS*5
3803	023274	012705	000001		MOV #1,R5	:PUT "EXPECTED" IN R5
3804	023300	116104	000005		MOVB 5(R1),R4	:PUT "FOUND" IN R4
3805	023304	042704	177776		BIC #177776,R4	:CLEAR UNWANTED BITS
3806	023310	020504			CMP R5,R4	:DATA CORRECT?
3807	023312	001401			BEQ 1\$:BR IF YES
3808	023314	104012			HLT 12	:ERROR NON-EXISTENT MEM BIT FAILED TO SET
3809	023316	104400		1\$:	SCOPE	:SCOPE THIS TEST

3810
3811
3812
3813
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3815
3816
3817
3818
3819

```

:***** TEST 66 *****
:*NPR NON-EXISTENT MEMORY TEST
:*DO A DATA FROM A NON-EXISTENT ADDRESS
:*VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11
:*****

```

```

: TEST 66
:-----
TST66: MOV #66,TSTNO
MOV #TST67,NEXT
MSTCLR
JSR R5,NPRSET
0
0
177320
177320
CLR 4(R1)
ROMCLK
121111
MOV #15,4(R1)
ROMCLK
121110
NOP
ROMCLK
121225
MOV #1,R5
MOVB 5(R1),R4
BIC #177776,R4
CMP R5,R4
BEQ 1$
HLT 12
SCOPE

```

3820 023320 012737 000066 001226
3821 023326 012737 023426 001216

3822
3823 023334 104412
3824 023336 004537 034622
3825 023342 000000
3826 023344 000000
3827 023346 177320
3828 023350 177320
3829 023352 005061 000004
3830 023356 104414
3831 023360 121111
3832 023362 012761 000015 000004
3833 023370 104414
3834 023372 121110
3835 023374 000240
3836 023376 104414
3837 023400 121225
3838 023402 012705 000001
3839 023406 116104 000005
3840 023412 042704 177776
3841 023416 020504
3842 023420 001401
3843 023422 104012
3844 023424 104400

1\$:
1\$:

```

:***** TEST 67 *****
:*NPR TEST

```

3845
3846
3847
3848


```

3849
3850
3851
3852
3853
3854
3855 023426 012737 000067 001226
3856 023434 012737 000003 001222
3857 023442 012737 023624 001216
3858
3859 023450 104412
3860 023452 005037 023622
3861 023456 005000
3862 023460 012702 036522
3863 023464
3864 023464 010037 023514
3865 023470 010237 023520
3866 023474 032702 000001
3867 023500 001402
3868 023502 000337 023514
3869 023506 004537 034622
3870 023512 000000
3871 023514 000000
3872 023516 000000
3873 023520 000000
3874 023522 105012
3875 023524 012761 000221 000004
3876 023532 104414
3877 023534 121110
3878 023536 000240
3879 023540 010005
3880 023542 111204
3881 023544 120504
3882 023546 001401
3883 023550 104021
3884 023552 104401
3885 023554 005200
3886 023556 042700 177400
3887 023562 005737 023622
3888 023566 001402
3889 023570 005700
3890 023572 001412
3891 023574 005202
3892 023576 023702 001304
3893 023602 001330
3894 023604 012702 036522
3895 023610 012737 177777 023622
3896 023616 000722
3897 023620 104400
3898 023622 000000
3899
3900
3901
3902
3903
3904

```

```

:*USING DATO, NPR A BINARY COUNT (0-377 )
:*FROM MICRO-PROCESSOR TO ALL AVAILABLE MEMORY
:*****
: TEST 67
-----
TST67: MOV #67,TSTNO
MOV #3,ICOUNT
MOV #TST70,NEXT

MSTCLR
CLR 5$
CLR R0
MOV #CORMAX,R2
1$: MOV R0,2$
MOV R2,4$
BIT #BIT0,R2
BEQ .+6
SWAB 2$
JSR R5,NPASET
0
2$: 0
0
4$: 0
CLRB (R2)
MOV #221,4(R1)
ROMCLK 121110
NOP
MOV R0,R5
MOVB (R2),R4
CMPB R5,R4
BEQ 3$
HLT 2!
3$: SCOP1
INC R0
BIC #177400,R0
TST 5$
BEQ 6$
TST R0
BEQ 7$
6$: INC R2
CMP MEMLIM,R2
BNE 1$
MOV #CORMAX,R2
MOV #-1,5$
BR 1$
7$: SCOPE
5$: 0

:R1 CONTAINS BASE DMC11 ADDRESS
:MASTER CLEAR DMC11
:START FLAG AT 0
:DATA
:ADDRESS
:LOAD DATA
:LOAD BA
:IS BA ODD?
:BR IF NO
:IF ODD PUT DATA IN HI-BYTE
:LOAD NPR REGISTERS
:IN DATA
:OUT DATA
:IN BA
:OUT BA
:CLEAR MEMORY LOCATION
:LOAD PORT4
:NEXT WORD IS INSTRUCTION. ROMCLK PC=5304
:DO THE NPR
:PUT "EXPECTED" IN R5
:PUT "FOUND" IN R4
:IS DATA CORRECT?
:BR IF YES
:ERROR. DATA INCORRECT
:NEXT CHARACTER
:USE ONLY LOW BYTE
:HAS MAX MEMORY BEEN REACHED YET?
:BR IF NO
:DONE PATTERN?
:BR IF YES
:INC BA
:REACHED MEMORY LIMIT YET?
:BR IF NOT
:RESTART BA AT FIRST ADDRESS
:SET FLAG TO END TEST AT END OF DATA PATTERN
:CONTINUE
:SCOPE THIS TEST
:THIS LOCATION IS A FLAG. IT STARTS AT 0
:AND IS SET TO -1 WHEN LAST MEMORY ADDRESS
:IS USED. TEST IS THEN ENDED WHEN PATTERN IS FIN

:***** TEST 70 *****
:*MAIN MEMORY TEST

```

```

3905                                     : *FLOAT A 1 THROUGH ALL MAIN MEMORY LOCATIONS
3906                                     : :*****
3907                                     :
3908                                     : TEST 70
3909                                     : -----
3910 023624 012737 000070 001226      TST70: MOV      #70,TSTNO
3911 023632 012737 023752 001216      MOV      #TST71,NEXT
3912 023640 012737 023656 001220      MOV      #65$,LOCK
3913                                     :
3914 023646 104412                                     MSTCLR
3915 023650 005002                                     CLR      R2
3916 023652 012700 000001      1$: MOV      #1,R0
3917 023656 042737 000377 023672      65$: BIC      #377,66$
3918 023664 050237 023672      BIS      R2,66$
3919 023670 104414                                     ROMCLK
3920 023672 010000      66$: 010000
3921 023674 010061 000004      MOV      R0,4(R1)
3922 023700 104414      ROMCLK
3923 023702 122500      122500
3924 023704 104414      ROMCLK
3925 023706 040620      040620
3926 023710 104414      ROMCLK
3927 023712 061225      61225
3928 023714 010005      MOV      R0,R5
3929 023716 116104 000005      MOVB    5(R1),R4
3930 023722 120504      CMPB    R5,R4
3931 023724 001401      BEQ     67$
3932 023726 104013      HLT
3933 023730 104401      67$: SCOP1
3934 023732 000241      CLC
3935 023734 106100      ROLB    R0
3936 023736 001347      BNE     65$
3937 023740 005202      INC     R2
3938 023742 022702 000400      CMP     #400,R2
3939 023746 001341      BNE     1$
3940 023750 104400      SCOPE
3941
3942                                     : ***** TEST 71 *****
3943                                     : *MAIN MEMORY TEST
3944                                     : *FLOAT A 0 THROUGH ALL MAIN MEMORY LOCATIONS
3945                                     : :*****
3946                                     :
3947                                     :
3948                                     : TEST 71
3949                                     : -----
3950 023752 012737 000071 001226      TST71: MOV      #71,TSTNO
3951 023760 012737 024104 001216      MOV      #TST72,NEXT
3952 023766 012737 024006 001220      MOV      #65$,LOCK
3953                                     :
3954 023774 104412                                     MSTCLR
3955 023776 005002                                     CLR      R2
3956 024000 012700 000001      1$: MOV      #1,R0
3957 024004 005100      64$: COM     R0
3958 024006 042737 000377 024022      65$: BIC      #377,66$
3959 024014 050237 024022      BIS      R2,66$
3960 024020 104414      ROMCLK

```

```

:R1 CONTAINS BASE DMC11 ADDRESS
:MASTER CLEAR DMC11
:START WITH ADDRESS 0
:START WITH BIT 0
: CLEAR ADDRESS FIELD OF INSTRUCTION
:ADD ADDRESS TO INSTRUCTION
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:LOAD MAR WITH ADDRESS IN R2
:WRITE PATTERN IN PORT4
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:MOVE PORT4 TO MEMORY
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:MOVE MEMORY TO BR
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:MOVE BR TO PORT5
:PUT "EXPECTED" IN R5
:PUT "FOUND" IN R4
:DATA CORRECT?
:BR IF YES
:DATA ERROR
:SW09=1?
:CLEAR CARRY
:SHIFT BIT IN RC
:DONE IF R0=0
:NEXT ADDRESS
:LAST ADDRESS
:BR IF NO
:SCOPE THIS TEST

```

```

:R1 CONTAINS BASE DMC11 ADDRESS
:MASTER CLEAR DMC11
:START WITH ADDRESS 0
:START WITH BIT 0
:CHANGE TO FLOATING 0
: CLEAR ADDRESS FIELD OF INSTRUCTION
:ADD ADDRESS TO INSTRUCTION
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

```

3961 024022 010000          66$: 010000          ;LOAD MAR WITH ADDRESS IN R2
3962 024024 010061 000004    MOV      R0,R1)          ;WRITE PATTERN IN PORT4
3963 024030 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3964 024032 122500          122500          ;MOVE PORT4 TO MEMORY
3965 024034 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3966 024036 040620          040620          ;MOVE MEMORY TO BR
3967 024040 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3968 024042 061225          61225           ;MOVE BR TO PORTS
3969 024044 010005          MOV      R0,R5          ;PUT "EXPECTED" IN R5
3970 024046 116104 000005    MOVB    5(R1),R4        ;PUT "FOUND" IN R4
3971 024052 120504          CMPB    R5,R4           ;DATA CORRECT?
3972 024054 001401          BEQ     67$            ;BR IF YES
3973 024056 104013          HLT     13             ;DATA ERROR
3974 024060 104401          67$: SCOP1           ;SW09=1?
3975 024062 005100          COM     R0             ;CHANGE TO FLOATING 1
3976 024064 000241          CLC                    ;CLEAR CARRY
3977 024066 106100          ROLB   R0             ;SHIFT BIT IN R0
3978 024070 001345          BNE    64$            ;DONE IF R0=0
3979 024072 005202          INC    R2             ;NEXT ADDRESS
3980 024074 022702 000400    CMP    #400,R2        ;LAST ADDRESS
3981 024100 001337          BNE    1$             ;BR IF NO
3982 024102 104400          SCOPE                    ;SCOPE THIS TEST
3983
3984
3985
3986
3987
3988
3989
3990
3991
3992
3993 024104 012737 000072 001226    TST72: MOV    #72,TSTNO
3994 024112 012737 024304 001216    MOV    #TST73,NEXT
3995 024120 012737 024132 001220    MOV    #1$,LOCK
3996
3997 024126 104412          MSTCLR          ;R1 CONTAINS BASE DMC11 ADDRESS
3998 024130 005002          CLR    R2           ;MASTER CLEAR DMC11
3999 024132 042737 000377 024146    1$: BIC    #377,2$      ;START AT ADDRESS 0
4000 024140 050237 024146          BIS    R2,2$        ;CLEAR ADDRESS FIELD OF INSTRUCTION
4001 024144 104414          ROMCLK          ;ADD ADDRESS TO INSTRUCTION
4002 024146 010000          2$: 010000          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4003 024150 010261 000004    MOV    R2,R1)        ;LOAD MAR
4004 024154 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4005 024156 122500          122500          ;MOVE PORT4 TO MEMORY
4006 024160 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4007 024162 040620          040620          ;MOVE MEMORY TO THE BR
4008 024164 104414          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4009 024166 061225          61225           ;MOVE BR TO PORTS
4010 024170 010205          MOV    R2,R5          ;PUT "EXPECTED" IN R5
4011 024172 116104 000005    MOVB    5(R1),R4        ;PUT "FOUND" IN R4
4012 024176 120504          CMPB    R5,R4           ;DATA CORRECT?
4013 024200 001401          BEQ     3$            ;BR IF YES
4014 024202 104013          HLT     13             ;DATA ERROR
4015 024204 104401          3$: SCOP1           ;SW09=1?
4016 024206 005202          INC    R2             ;NEXT ADDRESS

```

```

:***** TEST 72 *****
:MAIN MEMORY DUAL ADDRESSING TEST
:LOAD EACH MEMORY LOCATION WITH ITS OWN ADDRESS
:READ BACK EACH LOCATION TO VERIFY CORRECT ADDRESSING
:*****

```

```

: TEST 72
:-----

```

```

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;START AT ADDRESS 0
;CLEAR ADDRESS FIELD OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;LOAD MAR
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE PORT4 TO MEMORY
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE MEMORY TO THE BR
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE BR TO PORTS
;PUT "EXPECTED" IN R5
;PUT "FOUND" IN R4
;DATA CORRECT?
;BR IF YES
;DATA ERROR
;SW09=1?
;NEXT ADDRESS

```

4017	024210	022702	000400		CMP	#400,R2	;LAST ADDRESS
4018	024214	001346			BNE	1\$;BR IF NO
4019	024216	012737	024226	001220	MOV	#4\$,LOCK	;NEW SCOPE 1
4020	024224	005002			CLR	R2	;RESTART AT ADDRESS 0
4021	024226	042737	000377	024242	4\$: BIC	#377,5\$;CLEAR ADDRESS FIELD OF INSTRUCTION
4022	024234	050237	024242		BIS	R2,5\$;ADD ADDRESS TO INSTRUCTION
4023	024240	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4024	024242	010000		5\$:	010000		;LOAD THE MAR
4025	024244	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4026	024246	040620			040620		;MOVE MEMORY TO THE BR
4027	024250	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4028	024252	061225			61225		;MOV BR TO PORT5
4029	024254	010205			MOV	R2,R5	;PUT "EXPECTED" IN R5
4030	024256	116104	000005		MOVB	5(R1),R4	;PUT "FOUND" IN R4
4031	024262	120504			CMPB	R5,R4	;DATA CORRECT?
4032	024264	001401			BEQ	6\$;BR IF YES
4033	024266	104013			HLT	13	;ADDRESSING ERROR
4034	024270	104401		5\$:	SCOPE		;SWD9=1?
4035	024272	005202			INC	R2	;NEXT ADDRESS
4036	024274	022702	000400		CMP	#400,R2	;IS IT THE LAST
4037	024300	001352			BNE	4\$;BR IF NO
4038	024302	104400			SCOPE		;SCOPE THIS TEST

```

;***** TEST 73 *****
;*MAR TEST
;*PERFORM DUAL ADDRESSING TEST
;*USING MAR AUTO-INC FEATURE
;*****

```

: TEST 73

4049	024304	012737	000073	001226	TST73:	MOV	#73,TSTNO	
4050	024312	012737	024440	001216		MOV	#TST74,NEXT	
4051								;R1 CONTAINS BASE DMC11 ADDRESS
4052	024320	104412			MSTCLR			;MASTER CLEAR DMC11
4053	024322	005002			CLR	R2		;START WITH A ZERO
4054	024324	104414			ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4055	024326	010000			010000			;LOAD MAR
4056	024330	032737	100000	001366	BIT	#BIT15,STAT1		;DMC?
4057	024336	001402			BEQ	+.6		;BR IF YES
4058	024340	104414			ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4059	024342	004000			4000			;MAR HI ← 0 (KMC ONLY)
4060	024344	010261	000004		1\$: MOV	R2,4(R1)		;WRITE DATA TO PORT4
4061	024350	104414			ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4062	024352	136500			136500			;LOAD MEM AUTO-INC MAR
4063	024354	005202			INC	R2		;INCREMENT DATA
4064	024356	022702	000400		CMP	#400,R2		;DONE YET?
4065	024362	001370			BNE	1\$;BR IF NO
4066	024364	005002			CLR	R2		;RESTART WITH A ZERO
4067	024366	104414			ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4068	024370	010000			010000			;LOAD MAR
4069	024372	032737	100000	001366	BIT	#BIT15,STAT1		;DMC?
4070	024400	001402			BEQ	+.6		;BR IF YES
4071	024402	104414			ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4072	024404	004000			4000			;MAR HI ← 0 (KMC ONLY)

4073	024406				25:	ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4074	024406	104414				055224		;MOVE MEM TO PORT4
4075	024410	055224				MOV	R2,R5	;PUT "EXPECTED" IN R5
4076	024412	010205				MOV	4(R1),R4	;PUT "FOUND" IN R4
4077	024414	016104	000004			CMPB	R5,R4	;DATA CORRECT?
4078	024420	120504				BEQ	35	;BR IF YES
4079	024422	001401				HLT	14	;MAR ERROR
4080	024424	104014			35:	INC	R2	;NEXT ADDRESS
4081	024426	005202				CMP	#400.R2	;DONE YET?
4082	024430	022702	000400			BNE	25	;BR IF NO
4083	024434	001364				SCOPE		;SCOPE THIS TEST
4084	024436	104400						
4085								
4086								
4087								
4088								
4089								
4090								
4091								
4092								
4093								
4094	024440	012737	000074	001226	TST74:	MOV	#74,TSTNO	
4095	024446	012737	024552	001216		MOV	#TST75,NEXT	
4096	024454	012737	024500	001220		MOV	#15,LOCK	
4097								
4098	024462	104412				MSTCLR		;R1 CONTAINS BASE DMC11 ADDRESS
4099	024464	004737	034664			JSR	PC,MEMLD	;MASTER CLEAR DMC11
4100	024470	024542				TDATA		;LOAD MAINMEM DATA
4101	024472	004737	034720			JSR	PC,SPLD	;POINTER TO DATA
4102	024476	024542				TDATA		;LOAD SP DATA
4103	024500				15:			;POINTER TO DATA
4104	024500	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4105	024502	010000				010000		;MAR←0
4106	024504	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4107	024506	054400				054400!<0*20>		;ADD 377 AND 377 TO SET C BIT
4108	024510	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4109	024512	040421				040401!<1*20>		;ADD 0 AND 0 AND THE C BIT
4110	024514	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4111	024516	061224				61224		;PUT RESULTS IN PORT4
4112	024520	012705	000001			MOV	#1,R5	;PUT "EXPECTED" IN R5
4113	024524	016104	000004			MOV	4(R1),R4	;PUT "FOUND" IN R4
4114	024530	120504				CMPB	R5,R4	;DATA CORRECT?
4115	024532	001401				BEQ	25	;BR IF YES
4116	024534	104015			25:	HLT	15	;ERROR C BIT NOT SET
4117	024536	104401				SCOPE		;SW09=1?
4118	024540	104400				SCOPE		;SCOPE THIS TEST
4119	024542	377	000	000	TDATA:	.BYTE	-1,0,0,0,0,0,0,0	
4120	024545	000	000	000				
4121	024550	000	000					
4122								
4123								
4124								
4125								
4126								
4127								
4128								

```

;***** TEST 74 *****
;*ALU C BIT TEST
;*TEST THAT AN ADD OF 377 AND 377 WILL SET THE C BIT
;*****

```

```

; TEST 74
;-----

```

```

;***** TEST 75 *****
;*ALU TEST
;*TEST OF ALU FUNCTION SEL B WITH C BIT CLEARED
;*ALU FUNCTION (B) CODE=11

```

```

4129
4130
4131
4132
4133
4134
4135 024552 012737 000075 001226
4136 024560 012737 024726 001216
4137 024566 012737 024620 001220
4138
4139 024574 104412
4140 024576 005000
4141 024600 012702 024716
4142 024604 004737 034664
4143 024610 035010
4144 024612 004737 034720
4145 024616 035020
4146 024620 004737 034764
4147 024624 042737 000017 024640
4148 024632 050037 024640
4149 024636 104414
4150 024640 010000
4151 024642 042737 000017 024656
4152 024650 050037 024656
4153 024654 104414
4154 024656 040620
4155 024660 104414
4156 024662 061224
4157 024664 111205
4158 024666 116104 000004
4159 024672 120504
4160 024674 001401
4161 024676 104015
4162 024700 001401
4163 024702 005202
4164 024704 005200
4165 024706 022700 000010
4166 024712 001342
4167 024714 104400
4168 024716 000 377 000
4169 024721 377 125 252
4170 024724 125 252

```

```

: TEST 75
:-----
TST75: MOV #75,TSTNO
MOV #TST76,NEXT
MOV #1$,LOCK

MSTCLR
CLR RO
MOV #5$,R2
JSR PC,MEMLD
MEMDAT
JSR PC,SPLD
SPDAT
1$: JSR PC,CLRC
BIC #17,2$
BIS RO,2$
ROMCLK
2$: 010000
BIC #17,3$
BIS RO,3$
ROMCLK
3$: 040400! <11*20>
ROMCLK
61224
MOVB (R2),R5
MOVB 4(R1),R4
CMPB R5,R4
BEQ 4$
HLT 1$
4$: SCOP1
INC R2
INC RO
CMP #10,RO
BNE 1$
SCOPE
5$: .BYTE 0,-1,0,-1,125,252,125,252

```

```

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;MEM + SP ADDRESS
;POINTER TO CORRECT DATA
;LOAD 8 WORDS OF MAIN MEMORY
;POINTER TO DATA
;LOAD 8 WORDS OF SP
;POINTER TO DATA
;CLEAR C BIT!
;CLEAR ADDRESS FIELD OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;LOAD MAR
;CLEAR ADDRESS OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;BR + SEL B
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE BR TO PORT4
;PUT "EXPECTED" IN R5
;PUT "FOUND" IN R4
;DATA CORRECT?
;BR IF YES
;ALU ERROR
;SW09=1?
;NEXT DATA
;NEXT ADDRESS
;DONE YET?
;BR IF NO
;SCOPE THIS TEST

```

.EVEN

```

***** TEST 76 *****
;ALU TEST
;TEST OF ALU FUNCTION SEL A WITH C BIT CLEARED
;ALU FUNCTION (A) CODE=10
;LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

```

4181
4182
4183
4184 024726 012737 000076 001226

```

```

: TEST 76
:-----
TST76: MOV #76,TSTNO

```

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4185	024734	012737	025102	001216
4186	024742	012737	024774	001220
4187				
4188	024750	104412		
4189	024752	005000		
4190	024754	012702	025072	
4191	024760	004737	034664	
4192	024764	035010		
4193	024766	004737	034720	
4194	024772	035020		
4195	024774	004737	034764	
4196	025000	042737	000017	025014
4197	025006	050037	025014	
4198	025012	104414		
4199	025014	010000		
4200	025016	042737	000017	025032
4201	025024	050037	025032	
4202	025030	104414		
4203	025032	040600		
4204	025034	104414		
4205	025036	061224		
4206	025040	111205		
4207	025042	116104	000004	
4208	025046	120504		
4209	025050	001401		
4210	025052	104015		
4211	025054	104401		
4212	025056	005202		
4213	025060	005200		
4214	025062	022700	000010	
4215	025066	001342		
4216	025070	104400		
4217	025072	000	000	377
4218	025075	377	125	125
4219	025100	252	252	

```

MOV      #TST77,NEXT
MOV      #1$,LOCK
;R1 CONTAINS BASE DMC11 ADDRESS
MSTCLR  ;MASTER CLEAR DMC11
CLR      R0 ;MEM + SP ADDRESS
MOV      #5$,R2 ;POINTER TO CORRECT DATA
JSR      PC,MEMLD ;LOAD 8 WORDS OF MAIN MEMORY
MEMDAT  ;POINTER TO DATA
JSR      PC,SPLD ;LOAD 8 WORDS OF SP
SPDAT   ;POINTER TO DATA
1$:     JSR      PC,CLRC ;CLEAR C BIT!
        BIC      #17,2$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
        BIS      R0,2$ ;ADD ADDRESS TO INSTRUCTION
        ROMCLK  ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2$:     ROMCLK  010000 ;LOAD MAR
        BIC      #17,3$ ;CLEAR ADDRESS OF INSTRUCTION
        BIS      R0,3$ ;ADD ADDRESS TO INSTRUCTION
        ROMCLK  ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3$:     ROMCLK  040400! <10*20> ;BR + SEL A
        ROMCLK  61224 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
        MOV      (R2),R5 ;MOVE BR TO PORT4
        MOV      4(R1),R4 ;PUT "EXPECTED" IN R5
        CMP      R5,R4 ;PUT "FOUND" IN R4
        BEQ      4$ ;DATA CORRECT?
        HLT      1$ ;BR IF YES
        SCOPI  ;ALU ERROR
4$:     INC      R2 ;SW09=1?
        INC      R0 ;NEXT DATA
        CMP      #10,R0 ;NEXT ADDRESS
        BNE     1$ ;DONE YET?
        SCOPE  ;BR IF NO
5$:     .BYTE  0,0,-1,-1,125,125,252,252 ;SCOPE THIS TEST
        .EVEN

```

```

***** TEST 77 *****
*ALU TEST
*TEST OF ALU FUNCTION A OR NOTB WITH C BIT CLEARED
*ALU FUNCTION (A OR NOTB) CODE=12
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

4233	025102	012737	000077	001226
4234	025110	012737	025256	001216
4235	025116	012737	025150	001220
4236				
4237	025124	104412		
4238	025126	005000		
4239	025130	012702	025246	
4240	025134	004737	034664	

```

; TEST 77
-----
TST77:  MOV      #77,TSTNO
        MOV      #TST100,NEXT
        MOV      #1$,LOCK
;R1 CONTAINS BASE DMC11 ADDRESS
MSTCLR  ;MASTER CLEAR DMC11
CLR      R0 ;MEM + SP ADDRESS
MOV      #5$,R2 ;POINTER TO CORRECT DATA
JSR      PC,MEMLD ;LOAD 8 WORDS OF MAIN MEMORY

```

4241	025140	035010				MEMDAT	: POINTER TO DATA
4242	025142	004737	034720			JSR PC,SPLD	: LOAD 8 WORDS OF SP
4243	025146	035020				SPDAT	: POINTER TO DATA
4244	025150	004737	034764	1\$:		JSR PC,CLRC	: CLEAR C BIT!
4245	025154	042737	000017	025170		BIC #17,2\$: CLEAR ADDRESS FIELD OF INSTRUCTION
4246	025162	050037	025170			BIS RO,2\$: ADD ADDRESS TO INSTRUCTION
4247	025166	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4248	025170	010000		2\$:		010000	: LOAD MAR
4249	025172	042737	000017	025206		BIC #17,3\$: CLEAR ADDRESS OF INSTRUCTION
4250	025200	050037	025206			BIS RO,3\$: ADD ADDRESS TO INSTRUCTION
4251	025204	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4252	025206	040640		3\$:		040400! <12*20>	: BR + A OR NOTB
4253	025210	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4254	025212	061224				61224	: MOVE BR TO PORT4
4255	025214	111205				MOVB (R2),R5	: PUT "EXPECTED" IN R5
4256	025216	116104	000004			MOVB 4(R1),R4	: PUT "FOUND" IN R4
4257	025222	120504				CMPB R5,R4	: DATA CORRECT?
4258	025224	001401				BEQ 4\$: BR IF YES
4259	025226	104015				HLT 1\$: ALU ERROR
4260	025230	104401		4\$:		SCOPI	: SW09=1?
4261	025232	005202				INC R2	: NEXT DATA
4262	025234	005200				INC RO	: NEXT ADDRESS
4263	025236	022700	000010			CMP #10,RO	: DONE YET?
4264	025242	0J1342				BNE 1\$: BR IF NO
4265	025244	104400				SCOPE	: SCOPE THIS TEST
4266	025246	377	000	377	5\$:	.BYTE -1,0,-1,-1,-1,125,252,-1	
4267	025251	377		125			
4268	025254	252	377				

.EVEN

```

***** TEST 100 *****
*ALU TEST
*TEST OF ALU FUNCTION A AND B WITH C BIT CLEARED
*ALU FUNCTION (A AND B) CODE=13
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

: TEST 100

4281							
4282	025256	012737	000100	001226	TST100:	MOV #100,TSTNO	
4283	025264	012737	025432	001216		MOV #TST101,NEXT	
4284	025272	012737	025324	001220		MOV #1\$,LOCK	
4285							: R1 CONTAINS BASE DMC11 ADDRESS
4286	025300	104412			MSTCLR		: MASTER CLEAR DMC11
4287	025302	005000			CLR RO		: MEM + SP ADDRESS
4288	025304	012702	025422		MOV #5\$,R2		: POINTER TO CORRECT DATA
4289	025310	004737	034664		JSR PC,MEMLD		: LOAD 8 WORDS OF MAIN MEMORY
4290	025314	035010			MEMDAT		: POINTER TO DATA
4291	025316	004737	034720		JSR PC,SPLD		: LOAD 8 WORDS OF SP
4292	025322	035020			SPDAT		: POINTER TO DATA
4293	025324	004737	034764	1\$:	JSR PC,CLRC		: CLEAR C BIT!
4294	025330	042737	000017	025344	BIC #17,2\$: CLEAR ADDRESS FIELD OF INSTRUCTION
4295	025336	050037	025344		BIS RO,2\$: ADD ADDRESS TO INSTRUCTION
4296	025342	104414			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

4297	025344	010000			25:	010000	: LOAD MAR
4298	025346	042737	000017	025362		BIC #17,35	: CLEAR ADDRESS OF INSTRUCTION
4299	025354	050037	025362			BIS RO,35	: ADD ADDRESS TO INSTRUCTION
4300	025360	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4301	025362	040660			35:	040400! <13*20>	: BR + A AND B
4302	025364	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4303	025366	061224				61224	: MOVE BR TO PORT4
4304	025370	111205				MOV8 (R2),R5	: PUT "EXPECTED" IN R5
4305	025372	116104	000004			MOV8 4(R1),R4	: PUT "FOUND" IN R4
4306	025376	120504				CMP8 R5,R4	: DATA CORRECT?
4307	025400	001401				BEQ 45	: BR IF YES
4308	025402	104015				HLT 15	: ALU ERROR
4309	025404	104401			45:	SCC=1	: SW09=1?
4310	025406	005202				INC R2	: NEXT DATA
4311	025410	005200				INC R0	: NEXT ADDRESS
4312	025412	022700	000010			CMP #10,R0	: DONE YET?
4313	025416	001342				BNE 15	: BR IF NC
4314	025420	104400				SCOPE	: SCOPE THIS TEST
4315	025422	000	000	000	55:	.BYTE 0,0,0,-1,125,0,0,252	
4316	025425	377	125	000			
4317	025430	000	252				
4318						.EVEN	
4319							
4320							
4321							: ***** TEST 101 *****
4322							: *ALU TEST
4323							: *TEST OF ALU FUNCTION A OR B WITH C BIT CLEARED
4324							: *ALU FUNCTION (A OR B) CODE=14
4325							: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
4326							: *PERFORM THE FUNCTION, VERIFY THE RESULTS
4327							: *****
4328							
4329							: TEST 101
4330							: -----
4331	025432	012737	000101	001226	TST101:	MOV #101,TSTNO	
4332	025440	012737	025606	001216		MOV #TST102,NEXT	
4333	025446	012737	025500	001220		MOV #15,LOCK	
4334							: R1 CONTAINS BASE DMC11 ADDRESS
4335	025454	104412				MSTCLR	: MASTER CLEAR DMC11
4336	025456	005000				CLR R0	: MEM + SP ADDRESS
4337	025460	012702	025576			MOV #55,R2	: POINTER TO CORRECT DATA
4338	025464	004737	034664			JSR PC,MEMLD	: LOAD 8 WORDS OF MAIN MEMORY
4339	025470	035010				MEMDAT	: POINTER TO DATA
4340	025472	004737	034720			JSR PC,SPLD	: LOAD 8 WORDS OF SP
4341	025476	035020				SPDAT	: POINTER TO DATA
4342	025500	004737	034764		15:	JSR PC,CLRC	: CLEAR C BIT!
4343	025504	042737	000017	025520		BIC #17,25	: CLEAR ADDRESS FIELD OF INSTRUCTION
4344	025512	050037	025520			BIS RO,25	: ADD ADDRESS TO INSTRUCTION
4345	025516	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4346	025520	010000			25:	010000	: LOAD MAR
4347	025522	042737	000017	025536		BIC #17,35	: CLEAR ADDRESS OF INSTRUCTION
4348	025530	050037	025536			BIS RO,35	: ADD ADDRESS TO INSTRUCTION
4349	025534	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4350	025536	040700			35:	040400! <14*20>	: BR + A OR B
4351	025540	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4352	025542	061224				61224	: MOVE BR TO PCRT4

```

4353 025544 111205
4354 025546 116104 000004
4355 025552 120504
4356 025554 001401
4357 025556 104015
4358 025560 104401 45:
4359 025562 005202
4360 025564 005200
4361 025566 022700 000010
4362 025572 001342
4363 025574 104400
4364 025576 000 377 377
4365 025601 377 125 377
4366 025604 377 252
4367
4368
4369
4370
4371
4372
4373
4374
4375
4376
4377
4378
4379
4380 025606 012737 000102 001226
4381 025614 012737 025762 001216
4382 025622 012737 025654 001220
4383
4384 025630 104412
4385 025632 005000
4386 025634 012702 025752
4387 025640 004737 034664
4388 025644 035010
4389 025646 004737 034720
4390 025652 035020
4391 025654 004737 034764
4392 025660 042737 000017 025674
4393 025666 050037 025674
4394 025672 104414
4395 025674 010000 25:
4396 025676 042737 000017 025712
4397 025704 050037 025712
4398 025710 104414
4399 025712 040720 33:
4400 025714 104414
4401 025716 061224
4402 025720 111205
4403 025722 116104 000004
4404 025726 120504
4405 025730 001401
4406 025732 104015
4407 025734 104401 45:
4408 025736 005202

```

```

MOV B (R2),R5 ;PUT "EXPECTED" IN R5
MOV B 4(R1),R4 ;PUT "FOUND" IN R4
CMP B R5,R4 ;DATA CORRECT?
BEQ 45 ;BR IF YES
HLT 15 ;ALU ERROR
SCOPI ;SW09=1?
INC R2 ;NEXT DATA
INC R0 ;NEXT ADDRESS
CMP #10,R0 ;DONE YET?
BNE 15 ;BR IF NO
SCOPE ;SCOPE THIS TEST
.BYTE 0,-1,-1,-1,125,-1,-1,252

.EVEN

;***** TEST 102 *****
;ALU TEST
;TEST OF ALU FUNCTION A XOR B WITH C BIT CLEARED
;ALU FUNCTION (A XOR B) CODE=15
;LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;PERFORM THE FUNCTION, VERIFY THE RESULTS
;*****

; TEST 102
-----
TST102: MOV #102,TSTNO
MOV #TST103,NEXT
MOV #15,LOCK

MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
CLR R0 ;MASTER CLEAR DMC11
MEM + SP ADDRESS
MOV #55,R2 ;MEM + SP ADDRESS
JSR PC,MEMLD ;LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ;POINTER TO DATA
JSR PC,SPLD ;LOAD 8 WORDS OF SP
SPDAT ;POINTER TO DATA
JSR PC,CLRC ;CLEAR C BIT!
BIC #17,25 ;CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0,25 ;ADD ADDRESS TO INSTRUCTION
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ;LOAD MAR
BIC #17,35 ;CLEAR ADDRESS OF INSTRUCTION
BIS R0,35 ;ADD ADDRESS TO INSTRUCTION
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! (15*20) ;BR ← A XOR B
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ;MOVE BR TO PORT4
MOV B (R2),R5 ;PUT "EXPECTED" IN R5
MOV B 4(R1),R4 ;PUT "FOUND" IN R4
CMP B R5,R4 ;DATA CORRECT?
BEQ 45 ;BR IF YES
HLT 15 ;ALU ERROR
SCOPI ;SW09=1?
INC R2 ;NEXT DATA

```

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4409	025740	005200			
4410	025742	022700	000010		
4411	025746	001342			
4412	025750	104400			
4413	025752	000	377	377	
4414	025755	000	000	377	
4415	025760	377	000		
4416					.EVEN
4417					
4418					
4419					
4420					
4421					
4422					
4423					
4424					
4425					
4426					
4427					
4428					
4429	025762	012737	000103	001226	
4430	025770	012737	026136	001216	
4431	025776	012737	026030	001220	
4432					
4433	026004	04412			
4434	026006	005000			
4435	026010	012702	026126		
4436	026014	004737	034664		
4437	026020	035010			
4438	026022	004737	034720		
4439	026026	035020			
4440	026030	004737	034764		
4441	026034	042737	000017	026050	
4442	026042	050037	026050		
4443	026046	104414			
4444	026050	010000			
4445	026052	042737	000017	026066	
4446	026060	050037	026066		
4447	026064	104414			
4448	026066	040400			
4449	026070	104414			
4450	026072	061224			
4451	026074	111205			
4452	026076	116104	000004		
4453	026102	120504			
4454	026104	001401			
4455	026106	104015			
4456	026110	104401			
4457	026112	005202			
4458	026114	005200			
4459	026116	022700	000010		
4460	026122	001342			
4461	026124	104400			
4462	026126	000	377	377	
4463	026131	376	252	377	
4464	026134	377	124		

```

INC      RO      ;NEXT ADDRESS
CMP      #10,RO  ;DONE YET?
BNE      1$     ;BR IF NO
SCOPE   1$     ;SCOPE THIS TEST
SCOPE   .BYTE   0,-1,-1,0,0,-1,-1,0

```

```

***** TEST 103 *****
:ALU TEST
:TEST OF ALU FUNCTION ADD WITH C BIT CLEARED
:ALU FUNCTION (A PLUS B) CODE=0C
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

```

: TEST 103
-----
TST103: MOV      #103,TSTNO
MOV      #TST104,NEXT
MOV      #1$,LOCK

MSTCLR
CLR      RO
MOV      #$$,R2
JSR      PC,MEMLD
MEMDAT
JSR      PC,SPLD
SPDAT
JSR      PC,CLRC
1$: BIC      #17,2$
BIS      RO,2$
ROMCLK
2$: 010000
BIC      #17,3$
BIS      RO,3$
ROMCLK
3$: 040400!<00*20>
ROMCLK
61224
MOVB    (R2),R5
MOVB    4(R1),R4
CMPB    R5,R4
BEQ     4$
HLT     1$
4$: SCOP1
INC     R2
INC     RO
CMP     #10,RO
BNE     1$
SCOPE   1$
SCOPE   .BYTE   0,-1,-1,376,252,-1,-1,124

```

```

:R1 CONTAINS BASE DMC11 ADDRESS
:MASTER CLEAR DMC11
:MEM + SP ADDRESS
:POINTER TO CORRECT DATA
:LOAD 8 WORDS OF MAIN MEMCRY
:POINTER TO DATA
:LOAD 8 WORDS OF SP
:POINTER TO DATA
:CLEAR C BIT!
:CLEAR ADDRESS FIELD OF INSTRUCTION
:ADD ADDRESS TO INSTRUCTION
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:LOAD MAR
:CLEAR ADDRESS OF INSTRUCTION
:ADD ADDRESS TO INSTRUCTION
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:BR - ADD
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:MOVE BR TO PORT4
:PUT "EXPECTED" IN R5
:PUT "FOUND" IN R4
:DATA CORRECT?
:BR IF YES
:ALU ERROR
:SW09=1?
:NEXT DATA
:NEXT ADDRESS
:DONE YET?
:BR IF NO
:SCOPE THIS TEST

```

4465
4466
4467
4468
4469
4470
4471
4472
4473
4474
4475
4476
4477
4478
4479
4480
4481
4482
4483
4484
4485
4486
4487
4488
4489
4490
4491
4492
4493
4494
4495
4496
4497
4498
4499
4500
4501
4502
4503
4504
4505
4506
4507
4508
4509
4510
4511
4512
4513
4514
4515
4516
4517
4518
4519
4520

.EVEN

***** TEST 104 *****
: *ALU TEST
: *TEST OF ALU FUNCTION 2A W/C WITH C BIT CLEARED
: *ALU FUNCTION (A PLUS A PLUS C) CODE=6
: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: *PERFORM THE FUNCTION, VERIFY THE RESULTS
: *****

: TEST 104

TST104: MOV #104,TSTNO
MOV #TST105,NEXT
MOV #1\$,LOCK

MSTCLR
CLR R0
MOV #5\$,R2
JSR PC,MEMLO
MEMDAT
JSR PC,SPLD
SPDAT

: R1 CONTAINS BASE DMC11 ADDRESS
: MASTER CLEAR DMC11
: MEM + SP ADDRESS
: POINTER TO CORRECT DATA
: LOAD 8 WORDS OF MAIN MEMORY
: POINTER TO DATA
: LOAD 8 WORDS OF SP
: POINTER TO DATA

1\$: JSR PC,CLRC
BIC #17,2\$
BIS R0,2\$

: CLEAR C BIT!
: CLEAR ADDRESS FIELD OF INSTRUCTION
: ADD ADDRESS TO INSTRUCTION
: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

2\$: BIC #17,3\$
BIS R0,3\$
ROMCLK

: LOAD MAR
: CLEAR ADDRESS OF INSTRUCTION
: ADD ADDRESS TO INSTRUCTION
: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

3\$: ROMCLK 040400! <6*20>
ROMCLK 61224

: BR + 2A W/C
: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: MOVE BR TO PORT4
: PUT "EXPECTED" IN R5

MOV #R2,R5
MOV #4(R1),R4
CMPB R5,R4
BEQ 4\$
HLT 1\$

: PUT "FOUND" IN R4
: DATA CORRECT?
: BR IF YES
: ALU ERROR

4\$: SCOP1
INC R2
INC R0
CMP #10,R0
BNE 1\$

: SW09=1"
: NEXT DATA
: NEXT ADDRESS
: DONE YET?
: BR IF NO

5\$: SCOPE
.BYTE 0,0,376,376,252,252,124,124

: SCOPE THIS TEST

.EVEN

***** TEST 105 *****
: *ALU TEST
: *TEST OF ALU FUNCTION 5JB WITH C BIT CLEARED
: *ALU FUNCTION (A-B) CODE=16

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026312 012737 000105 001226
026320 012737 026466 001216
026326 012737 026360 001220

026334 104412
026336 005000
026340 012702 026456
026344 004737 034664
026350 035010
026352 004737 034720
026356 035020
026360 004737 034764
026364 042737 000017 026400
026372 050037 026400
026376 104414
026400 010000
026402 042737 000017 026416
026410 050037 026416
026414 104414
026416 040740
026420 104414
026422 061224
026424 111205
026426 116104 000004
026432 120504
026434 001401
026436 104015
026440 104401
026442 005202
026444 005200
026446 022700 000010
026452 001342
026454 104400
026456 000 001 377
026461 000 000 253
026464 125 000

: TEST 105

TST105: MOV #105,TSTNO
MOV #TST106,NEXT
MOV #1\$,LOCK

MSTCLR
CLR R0
MOV #5\$,R2
JSR PC,MEMLD
MEMDAT
JSR PC,SPLD
SPDAT
JSR PC,CLRC
1\$: BIC #17,2\$
BIS R0,2\$
ROMCLY
010000
2\$: BIC #17,3\$
BIS R0,3\$
ROMCLK
040400! (16*20)
3\$: ROMCLK
61224
MOV8 (R2),R5
MOV8 4(R1),R4
CMPB R5,R4
BEQ 4\$
HLT 1\$
4\$: SCOPE
INC R2
INC R0
CMP #10,R0
BNE 1\$
SCOPE
5\$: .BYTE 0,1,-1,0,0.253,125,0

:R1 CONTAINS BASE DMC11 ADDRESS
:MASTER CLEAR DMC11
:MEM + SP ADDRESS
: POINTER TO CORRECT DATA
: LOAD 8 WORDS OF MAIN MEMORY
: POINTER TO DATA
: LOAD 8 WORDS OF SP
: POINTER TO DATA
: CLEAR C BIT!
: CLEAR ADDRESS FIELD OF INSTRUCTION
: ADD ADDRESS TO INSTRUCTION
: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: LOAD MAR
: CLEAR ADDRESS OF INSTRUCTION
: ADD ADDRESS TO INSTRUCTION
: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: BR + SUB
: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: MOVE BR TO PORT4
: PUT "EXPECTED" IN R5
: PUT "FOUND" IN R4
: DATA CORRECT?
: BR IF YES
: ALU ERROR
: SW09=1?
: NEXT DATA
: NEXT ADDRESS
: DONE YET?
: BR IF NO
: SCOPE THIS TEST

.EVEN

:***** TEST 106 *****
:ALU TEST
:TEST OF ALU FUNCTION ADD W/C WITH C BIT CLEARED
:ALU FUNCTION (A PLUS B PLUS C) CODE=01
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

: TEST 106

TST106: MOV #106,TSTNO

4577	026474	012737	026642	001216	MOV	#TST107,NEXT	
4578	026502	012737	026534	001220	MOV	#1\$,LOCK	
4579							:R1 CONTAINS BASE DMC11 ADDRESS
4580	026510	104412			MSTCLR		:MASTER CLEAR DMC11
4581	026512	005000			CLR	R0	:MEM + SP ADDRESS
4582	026514	012702	026632		MOV	#5\$,R2	:POINTER TO CORRECT DATA
4583	026520	004737	034664		JSR	PC,MEMLD	:LOAD 8 WORDS OF MAIN MEMORY
4584	026524	035010			MEMDAT		:POINTER TO DATA
4585	026526	004737	034720		JSR	PC,SPLD	:LOAD 8 WORDS OF SP
4586	026532	035020			SPDAT		:POINTER TO DATA
4587	026534	004737	034764		JSR	PC,CLRC	:CLEAR C BIT!
4588	026540	042737	000017	026554	BIC	#17,2\$:CLEAR ADDRESS FIELD OF INSTRUCTION
4589	026546	050037	026554		BIS	R0,2\$:ADD ADDRESS TO INSTRUCTION
4590	026552	104414			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4591	026554	010000			010000		:LOAD MAR
4592	026556	042737	000017	026572	BIC	#17,3\$:CLEAR ADDRESS OF INSTRUCTION
4593	026564	050037	026572		BIS	R0,3\$:ADD ADDRESS TO INSTRUCTION
4594	026570	104414			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4595	026572	040420			040400! <01*20>		:BR + ADD W/C
4596	026574	104414			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4597	026576	061224			61224		:MOVE BR TO PORT4
4598	026600	111205			MOVB	(R2),R5	:PUT "EXPECTED" IN R5
4599	026602	116104	000004		MOVB	4(R1),R4	:PUT "FOUND" IN R4
4600	026606	120504			CMPB	R5,R4	:DATA CORRECT?
4601	026610	001401			BEQ	4\$:BR IF YES
4602	026612	104015			HLT	1\$:ALU ERROR
4603	026614	104401			SCOPI		:SW09=1?
4604	026616	005202			INC	R2	:NEXT DATA
4605	026620	005200			INC	R0	:NEXT ADDRESS
4606	026622	022700	000010		CMP	#10,R0	:DONE YET?
4607	026626	001342			BNE	1\$:BR IF NO
4608	026630	104400			SCOPE		:SCOPE THIS TEST
4609	026632	000	377	377	.BYTE	0,-1,-1,376,252,-1,-1,124	
4610	026635	376	252	377			
4611	026640	377	124				
4612					.EVEN		
4613							
4614							
4615							:***** TEST 107 *****
4616							:*ALU TEST
4617							:*TEST OF ALU FUNCTION SUB W/C WITH C BIT CLEARED
4618							:*ALU FUNCTION (A-B-C) CODE=2
4619							:*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
4620							:*PERFORM THE FUNCTION, VERIFY THE RESULTS
4621							:*****
4622							
4623							: TEST 107
4624							
4625	026642	012737	000107	001226	TST107: MOV	#107,TSTNO	
4626	026650	012737	027016	001216	MOV	#TST110,NEXT	
4627	026656	012737	026710	001220	MOV	#1\$,LOCK	
4628							:R1 CONTAINS BASE DMC11 ADDRESS
4629	026664	104412			MSTCLR		:MASTER CLEAR DMC11
4630	026666	005000			CLR	R0	:MEM + SP ADDRESS
4631	026670	012702	027006		MOV	#5\$,R2	:POINTER TO CORRECT DATA
4632	026674	004737	034664		JSR	PC,MEMLD	:LOAD 8 WORDS OF MAIN MEMORY

4633	026700	035010				MEMDAT	: POINTER TO DATA
4634	026702	004737	034720			JSR PC,SPLD	: LOAD 8 WORDS OF SP
4635	026706	035020				SPDAT	: POINTER TO DATA
4636	026710	004737	034764		1\$:	JSR PC,CLRC	: CLEAR C BIT!
4637	026714	042737	000017	026730		BIC #17,2\$: CLEAR ADDRESS FIELD OF INSTRUCTION
4638	026722	050037	026730			BIS RO,2\$: ADD ADDRESS TO INSTRUCTION
4639	026726	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4640	026730	010000			2\$:	010000	: LOAD MAR
4641	026732	042737	000017	026746		BIC #17,3\$: CLEAR ADDRESS OF INSTRUCTION
4642	026740	050037	026746			BIS RO,3\$: ADD ADDRESS TO INSTRUCTION
4643	026744	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4644	026746	040440			3\$:	040400!<2*20>	: BR + SUB W/C
4645	026750	104414				ROMCLK	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4646	026752	061224				61224	: MOVE BR TO PORT4
4647	026754	111205				MOVE (R2),R5	: PUT "EXPECTED" IN R5
4648	026756	116104	000004			MOVE 4(R1),R4	: PUT "FOUND" IN R4
4649	026762	120504				CMPB R5,R4	: DATA CORRECT?
4650	026764	001401				BEQ 4\$: BR IF YES
4651	026766	104015				HLT 1\$: ALU ERROR
4652	026770	104401			4\$:	SCOPE1	: SW09=1?
4653	026772	005202				INC R2	: NEXT DATA
4654	026774	005200				INC RO	: NEXT ADDRESS
4655	026776	022700	000010			CMP #10,RO	: DONE YET?
4656	027002	001342				BNE 1\$: BR IF NO
4657	027004	104400				SCOPE	: SCOPE THIS TEST
4658	027006	377	000	376	5\$:	.BYTE -1,0,376,-1,-1,252,124,-1	
4659	027011	377	377	252			
4660	027014	124	377				
4661						.EVEN	

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:***** TEST 110 *****
: *ALU TEST
: *TEST OF ALU FUNCTION INC A WITH C BIT CLEARED
: *ALU FUNCTION (A PLUS 1) CODE=3
: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: *PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

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: TEST 110

4674	027016	012737	000110	001226	TST110:	MOV #110,TSTNO	
4675	027024	012737	027172	001216		MOV #TST111,NEXT	
4676	027032	012737	027064	001220		MOV #1\$,LOCK	
4677							
4678	027040	104412				MSTCLR	: R1 CONTAINS BASE DMC11 ADDRESS
4679	027042	005000				CLR RO	: MASTER CLEAR DMC11
4680	027044	012702	027162			MOV #5\$,R2	: MEM + SP ADDRESS
4681	027050	004737	034664			JSR PC,MEMLD	: POINTER TO CORRECT DATA
4682	027054	035010				MEMDAT	: LOAD 8 WORDS OF MAIN MEMORY
4683	027056	004737	034720			JSR PC,SPLD	: POINTER TO DATA
4684	027062	035020				SPDAT	: LOAD 8 WORDS OF SP
4685	027064	004737	034764		1\$:	JSR PC,CLRC	: POINTER TO DATA
4686	027070	042737	000017	027104		BIC #17,2\$: CLEAR C BIT!
4687	027076	050037	027104			BIS RO,2\$: CLEAR ADDRESS FIELD OF INSTRUCTION
4688	027102	104414				ROMCLK	: ADD ADDRESS TO INSTRUCTION
							: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

4689	027104	010000			2\$:	010000		:LOAD MAR
4690	027106	042737	000017	027122		BIC	#17,3\$:CLEAR ADDRESS OF INSTRUCTION
4691	027114	050037	027122			BIS	RO,3\$:ADD ADDRESS TO INSTRUCTION
4692	027120	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4693	027122	040400			3\$:	040400!	<3*20>	:BR + INC A
4694	027124	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4695	027126	061224				61224		:MOVE BR TO PORT4
4696	027130	111205				MOV8	(R2),R5	:PUT "EXPECTED" IN R5
4697	027132	116104	000004			MOV8	4(R1),R4	:PUT "FOUND" IN R4
4698	027136	120504				CMP8	R5,R4	:DATA CORRECT?
4699	027140	001401				BEQ	4\$:BR IF YES
4700	027142	104015				HLT	15	:ALU ERROR
4701	027144	104401			4\$:	SCOPI		:SW09=1?
4702	027146	005202				INC	R2	:NEXT DATA
4703	027150	005200				INC	RO	:NEXT ADDRESS
4704	027152	022700	000010			CMP	#10,RO	:DONE YET?
4705	027156	001342				BNE	1\$:BR IF NO
4706	027160	104400				SCOPE		:SCOPE THIS TEST
4707	027162	001	001	000	5\$:	.BYTE	1,1,0,0,126,126,253,253	
4708	027165	000	126	126				
4709	027170	253	253					
4710						.EVEN		
4711								
4712								
4713								
4714								
4715								
4716								
4717								
4718								
4719								
4720								
4721								
4722								
4723	027172	012737	000111	001226	TST111:	MOV	#111,TSTNO	
4724	027200	012737	027346	001216		MOV	#TST112,NEXT	
4725	027206	012737	027240	001220		MOV	#1\$,LOCK	
4726								
4727	027214	104412				MSTCLR		:R1 CONTAINS BASE DMC11 ADDRESS
4728	027216	005000				CLR	RO	:MASTER CLEAR DMC11
4729	027220	012702	027336			MOV	#5\$,R2	:MEM + SP ADDRESS
4730	027224	004737	034664			JSR	PC,MEMLD	:POINTER TO CORRECT DATA
4731	027230	035010				MEMDAT		:LOAD 8 WORDS OF MAIN MEMORY
4732	027232	004737	034720			JSR	PC,SPLD	:POINTER TO DATA
4733	027236	035020				SPDAT		:LOAD 8 WORDS OF SP
4734	027240	004737	034764		1\$:	JSR	PC,CLRC	:POINTER TO DATA
4735	027244	042737	000017	027260		BIC	#17,2\$:CLEAR C BIT!
4736	027252	050037	027260			BIS	RO,2\$:CLEAR ADDRESS FIELD OF INSTRUCTION
4737	027256	104414				ROMCLK		:ADD ADDRESS TO INSTRUCTION
4738	027260	010000			2\$:	010000		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4739	027262	042737	000017	027276		BIC	#17,3\$:LOAD MAR
4740	027270	050037	027276			BIS	RO,3\$:CLEAR ADDRESS OF INSTRUCTION
4741	027274	104414				ROMCLK		:ADD ADDRESS TO INSTRUCTION
4742	027276	040520			3\$:	040400!	<5*20>	:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4743	027300	104414				ROMCLK		:BR + 2A
4744	027302	061224				61224		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
								:MOVE BR TO PORT4

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;***** TEST 111 *****
;*ALU TEST
;*TEST OF ALU FUNCTION 2A WITH C BIT CLEARED
;*ALU FUNCTION (A PLUS A) CODE=5
;*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;*PERFORM THE FUNCTION, VERIFY THE RESULTS
;*****

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; TEST 111
;-----
TST111: MOV #111,TSTNO
MOV #TST112,NEXT
MOV #1$,LOCK

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;MEM + SP ADDRESS
;POINTER TO CORRECT DATA
;LOAD 8 WORDS OF MAIN MEMORY
;POINTER TO DATA
;LOAD 8 WORDS OF SP
;POINTER TO DATA
;CLEAR C BIT!
;CLEAR ADDRESS FIELD OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;LOAD MAR
;CLEAR ADDRESS OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;BR + 2A
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE BR TO PORT4

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4745	027304	111205			
4746	027306	116104	000004		
4747	027312	120504			
4748	027314	001401			
4749	027316	104015			
4750	027320	104401		45:	
4751	027322	005202			
4752	027324	005200			
4753	027326	022700	000010		
4754	027332	001342			
4755	027334	104400			
4756	027336	000	000	376	55:
4757	027341	376	252	252	
4758	027344	124	124		
4759					.EVEN
4760					
4761					
4762					
4763					
4764					
4765					
4766					
4767					
4768					
4769					
4770					
4771					
4772	027346	012737	000112	001226	
4773	027354	012737	027522	001216	
4774	027362	012737	027414	001220	
4775					
4776	027370	104412			
4777	027372	005000			
4778	027374	012702	027512		
4779	027400	004737	034664		
4780	027404	035010			
4781	027406	004737	034720		
4782	027412	035020			
4783	027414	004737	034764		
4784	027420	042737	000017	027434	
4785	027426	050037	027434		
4786	027432	104414			
4787	027434	010000			
4788	027436	042737	000017	027452	
4789	027444	050037	027452		
4790	027450	104414			
4791	027452	040500			
4792	027454	104414			
4793	027456	061224			
4794	027460	111205			
4795	027462	116104	000004		
4796	027466	120504			
4797	027470	001401			
4798	027472	104015			
4799	027474	104401			
4800	027476	005202			

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MOV8 (R2),R5 ;PUT "EXPECTED" IN R5
MOV8 4(R1),R4 ;PUT "FOUND" IN R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 4$ ;BR IF YES
HLT 15 ;ALU ERROR
45: SCOP1 ;SW09=1?
INC R2 ;NEXT DATA
INC R0 ;NEXT ADDRESS
CMP #10,R0 ;DONE YET?
BNE 1$ ;BR IF NO
SCOPE ;SCOPE THIS TEST
55: .BYTE 0,0,376,376,252,252,124,124

.EVEN

:***** TEST 112 *****
:ALU TEST
:TEST OF ALU FUNCTION A PLUS C WITH C BIT CLEARED
:ALU FUNCTION (A PLUS C) CODE=4
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

: TEST 112
:-----
TST112: MOV #112,TSTNO
MOV #TST113,NEXT
MOV #15,LOCK

MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
CLR R0 ;MASTER CLEAR DMC11
MOV #5$,R2 ;MEM + SP ADDRESS
JSR PC,MEMLD ;LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ;POINTER TO DATA
JSR PC,SPLD ;LOAD 8 WORDS OF SP
SPDAT ;POINTER TO DATA
15: JSR PC,CLRC ;CLEAR C BIT!
BIC #17,2$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0,2$ ;ADD ADDRESS TO INSTRUCTION
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
25: 010000 ;LOAD MAR
BIC #17,3$ ;CLEAR ADDRESS OF INSTRUCTION
BIS R0,3$ ;ADD ADDRESS TO INSTRUCTION
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
35: 040400! <4*20> ;BR + A PLUS C
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ;MOVE BR TO PORT4
MOV8 (R2),R5 ;PUT "EXPECTED" IN R5
MOV8 4(R1),R4 ;PUT "FOUND" IN R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 4$ ;BR IF YES
HLT 15 ;ALU ERROR
45: SCOP1 ;SW09=1?
INC R2 ;NEXT DATA

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4801	027500	005200				INC	RO		:NEXT ADDRESS
4802	027502	022700	000010			CMP	#10,RO		:DONE YET?
4803	027506	001342				BNE	1\$:BR IF NO
4804	027510	104400				SCOPE			:SCOPE THIS TEST
4805	027512	000	000	377	5\$:	.BYTE	0,0,-1,-1,125,125,252,252		
4806	027515	377	125	125					
4807	027520	252	252						
4808									.EVEN
4809									
4810									
4811									:***** TEST 113 *****
4812									:*ALU TEST
4813									:*TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT CLEARED
4814									:*ALU FUNCTION (A-B-1) CODE=17
4815									:*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
4816									:*PERFORM THE FUNCTION, VERIFY THE RESULTS
4817									:*****
4818									
4819									: TEST 113
4820									
4821	027522	012737	000113	001226		TST113:	MOV	#113,TSTNO	
4822	027530	012737	027676	001216			MOV	#TST114,NEXT	
4823	027536	012737	027570	001220			MOV	#1\$,LOCK	
4824									
4825	027544	104412					MSTCLR		:P1 CONTAINS BASE DMC11 ADDRESS
4826	027546	005000					CLR	RO	:MASTER CLEAR DMC11
4827	027550	012702	027666				MOV	#5\$,R2	:MEM + SP ADDRESS
4828	027554	004737	034664				JSR	PC,MEMLD	:POINTER TO CORRECT DATA
4829	027560	035010					MEMDAT		:LOAD 8 WORDS OF MAIN MEMCRY
4830	027562	004737	034720				JSR	PC,SPLD	:POINTER TO DATA
4831	027566	035020					SPDAT		:LOAD 8 WORDS OF SP
4832	027570	004737	034764		1\$:		JSR	PC,CLRC	:POINTER TO DATA
4833	027574	042737	000017	027610			BIC	#17,2\$:CLEAR C BIT!
4834	027602	050037	027610				BIS	RO,2\$:CLEAR ADDRESS FIELD OF INSTRUCTION
4835	027606	104414					ROMCLK		:ADD ADDRESS TO INSTRUCTION
4836	027610	010000			2\$:		010000		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4837	027612	042737	000017	027626			BIC	#17,3\$:LOAD MAR
4838	027620	050037	027626				BIS	RO,3\$:CLEAR ADDRESS OF INSTRUCTION
4839	027624	104414					ROMCLK		:ADD ADDRESS TO INSTRUCTION
4840	027626	040760			3\$:		040400!(17*20)		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4841	027630	104414					ROMCLK		:BR + 2'S COMP SUB
4842	027632	061224					61224		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4843	027634	111205					MOVB	(R2),R5	:MOVE BR TO PORT4
4844	027636	116104	000004				MOVB	4(R1),R4	:PUT "EXPECTED" IN R5
4845	027642	120504					CMPB	R5,R4	:PUT "FOUND" IN R4
4846	027644	001401					BEQ	4\$:DATA CORRECT?
4847	027646	104015					HLT	1\$:BR IF YES
4848	027650	104401			4\$:		SCOPE		:ALU ERROR
4849	027652	005202					INC	R2	:SW09=1?
4850	027654	005200					INC	RO	:NEXT DATA
4851	027656	022700	000010				CMP	#10,RO	:NEXT ADDRESS
4852	027662	001342					BNE	1\$:DONE YET?
4853	027664	104400					SCOPE		:BR IF NO
4854	027666	377	000	376	5\$:		.BYTE	-1,0,376,-1,-1,252,124,-1	:SCOPE THIS TEST
4855	027671	377	377	252					
4856	027674	124	377						

4857 .EVEN

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4907
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4909
4910
4911
4912

027676 012737 000114 001226
027704 012737 030052 001216
027712 012737 027744 001220

027720 104412
027722 005000
027724 012702 030042
027730 004737 034664
027734 035010
027736 004737 034720
027742 035020
027744 004737 034764
027750 042737 000017 027764
027756 050037 027764
027762 104414
027764 010000
027766 042737 000017 030002
027774 050037 030002
030000 104414
030002 040560
030004 104414
030006 061224
030010 111205
030012 116104 000004
030016 120504
030020 001401
030022 104015
030024 104401
030026 005202
030030 005200
030032 022700 000010
030036 001342
030040 104400
030042 377 377 376
030045 376 124 124
030050 251 251

***** TEST 114 *****
*ALU TEST
*TEST OF ALU FUNCTION DEC A WITH C BIT CLEARED
*ALU FUNCTION (A-1) CODE=7
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS

TEST 114

TST114: MOV #114,TSTNO
MOV #TST115,NEXT
MOV #15,LOCK

MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
CLR RO ;MASTER CLEAR DMC11
MOV #55,R2 ;MEM + SP ADDRESS
JSR PC,MEMLD ;POINTER TO CORRECT DATA
MEMDAT ;LOAD 8 WORDS OF MAIN MEMORY
JSR PC,SPLD ;POINTER TO DATA
SPDAT ;LOAD 8 WORDS OF SP
JSR PC,CLRC ;POINTER TO DATA
BIC #17,25 ;CLEAR C BIT!
BIS RO,25 ;CLEAR ADDRESS FIELD OF INSTRUCTION
ROMCLK ;ADD ADDRESS TO INSTRUCTION
010000 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
BIC #17,35 ;LOAD MAR
BIS RO,35 ;CLEAR ADDRESS OF INSTRUCTION
ROMCLK ;ADD ADDRESS TO INSTRUCTION
040400! <7*20> ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ;BR + DEC A
MOV8 (R2),R5 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
MOV8 4(R1),R4 ;MOVE BR TO PORT4
CMPB R5,R4 ;PUT "EXPECTED" IN R5
BEQ 45 ;PUT "FOUND" IN R4
HLT 15 ;DATA CORRECT?
SCOP1 ;BR IF YES
INC R2 ;ALU ERROR
INC RO ;SW09=1?
CMP #10,RO ;NEXT DATA
BNE 15 ;NEXT ADDRESS
SCOPE ;DONE YET?
BYTE -1,-1,376,376,124,124,251,251 ;BR IF NO
 ;SCOPE THIS TEST

.EVEN

***** TEST 115 *****
*ALU TEST
*TEST OF ALU FUNCTION SEL B WITH C BIT SET
*ALU FUNCTION (B) CODE=11

```

4913
4914
4915
4916
4917
4918
4919 030052 012737 000115 001226
4920 030060 012737 030226 001216
4921 030066 012737 030120 001220
4922
4923 030074 104412
4924 030076 005000
4925 030100 012702 030216
4926 030104 004737 034664
4927 030110 035010
4928 030112 004737 034720
4929 030116 035020
4930 030120 004737 034776
4931 030124 042737 000017 030140
4932 030132 050037 030140
4933 030136 104414
4934 030140 010000
4935 030142 042737 000017 030156
4936 030150 050037 030156
4937 030154 104414
4938 030156 040620
4939 030160 104414
4940 030162 061224
4941 030164 111205
4942 030166 116104 000004
4943 030172 120504
4944 030174 001401
4945 030176 104015
4946 030200 104401
4947 030202 005202
4948 030204 005200
4949 030206 022700 000010
4950 030212 001342
4951 030214 104400
4952 030216 000 377 000
4953 030221 377 125 252
4954 030224 125 252
4955
4956
4957
4958
4959
4960
4961
4962
4963
4964
4965
4966
4967
4968 030226 012737 000116 001226

```

```

; *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; *****
. TEST 115
-----
TST115: MOV #115,TSTNO
MOV #TST116,NEXT
MOV #1$,LOCK
MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
CLR RO ;MASTER CLEAR DMC11
MOV #5$,R2 ;MEM + SP ADDRESS
JSR PC,MEMLD ;LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ;POINTER TO CORRECT DATA
JSR PC,SPLD ;LOAD 8 WORDS OF SP
SPDAT ;POINTER TO DATA
1$: JSR PC,SETC ;SET C BIT!
BIC #17,2$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
BIS RO,2$ ;ADD ADDRESS TO INSTRUCTION
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ;LOAD MAR
2$: BIC #17,3$ ;CLEAR ADDRESS OF INSTRUCTION
BIS RO,3$ ;ADD ADDRESS TO INSTRUCTION
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! <11*20> ;BR + SEL B
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ;MOVE BR TO PORT4
MOV8 (R2),R5 ;PUT "EXPECTED" IN R5
MOV8 4(R1),R4 ;PUT "FOUND" IN R4
CMP8 R5,R4 ;DATA CORRECT?
BEQ 4$ ;BR IF YES
HLT 15 ;ALU ERROR
4$: SCOPI ;SW09=1?
INC R2 ;NEXT DATA
INC RO ;NEXT ADDRESS
CMP #10,RO ;DONE YET?
BNE 1$ ;BR IF NO
SCOPE ;SCOPE THIS TEST
5$: .BYTE 0,-1,0,-1,125,252,125,252
.EVEN
; ***** TEST 116 *****
; *ALU TEST
; *TEST OF ALU FUNCTION SEL A WITH C BIT SET
; *ALU FUNCTION (A) CODE=10
; *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; *****
. TEST 116
-----
TST116: MOV #116,TSTNO

```

```

4969 030234 012737 030402 001216
4970 030242 012737 030274 001220
4971
4972 030250 104412
4973 030252 005000
4974 030254 012702 030372
4975 030260 004737 034664
4976 030264 035010
4977 030266 004737 034720
4978 030272 035020
4979 030274 004737 034776
4980 030300 042737 000017 030314
4981 030306 050037 030314
4982 030312 104414
4983 030314 010000
4984 030316 042737 000017 030332
4985 030324 050037 030332
4986 030330 104414
4987 030332 040600
4988 030334 104414
4989 030336 061224
4990 030340 111205
4991 030342 116104 000004
4992 030346 120504
4993 030350 001401
4994 030352 104015
4995 030354 104401
4996 030356 005202
4997 030360 005200
4998 030362 022700 000010
4999 030366 001342
5000 030370 104400
5001 030372 000 000 377
5002 030375 377 125 125
5003 030400 252 252
5004
5005
5006
5007
5008
5009
5010
5011
5012
5013
5014
5015
5016
5017 030402 012737 000117 001226
5018 030410 012737 030556 001216
5019 030416 012737 030450 001220
5020
5021 030424 104412
5022 030426 005000
5023 030430 012702 030546
5024 030434 004737 034664

```

```

MOV #TST117,NEXT
MOV #15,LOCK
MSTCLR
CLR R0
MOV #55,R2
JSR PC,MEMLD
MEMDAT
JSR PC,SPLD
SPDAT
JSR PC,SETC
15: BIC #17,25
BIS R0,25
ROMCLK
010000
25: BIC #17,35
BIS R0,35
ROMCLK
35: 040400! <10*20>
ROMCLK
61224
MOV# (R2),R5
MOV# 4(R1),R4
CMPB R5,R4
BEQ 45
HLT 15
45: SCOPE
INC R2
INC R0
CMP #10,R0
BNE 15
SCOPE
55: .BYTE 0,0,-1,-1,125,125,252,252

```

```

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;MEM + SP ADDRESS
;POINTER TO CORRECT DATA
;LOAD 8 WORDS OF MAIN MEMORY
;POINTER TO DATA
;LOAD 8 WORDS OF SP
;POINTER TO DATA
;SET C BIT!
;CLEAR ADDRESS FIELD OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;LOAD MAR
;CLEAR ADDRESS OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;BR + SEL A
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE BR TO PORT4
;PUT "EXPECTED" IN P5
;PUT "FOUND" IN R4
;DATA CORRECT?
;BR IF YES
;ALU ERROR
;SW09=1?
;NEXT DATA
;NEXT ADDRESS
;DONE YET?
;BR IF NO
;SCOPE THIS TEST

```

.EVEN

```

:***** TEST 117 *****
:ALU TEST
:TEST OF ALU FUNCTION A OR NOTB WITH C BIT SET
:ALU FUNCTION (A OR NOTB) CODE=12
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

: TEST 117

```

TST117: MOV #117,TSTNO
MOV #TST120,NEXT
MOV #15,LOCK
MSTCLR
CLR R0
MOV #55,R2
JSR PC,MEMLD

```

```

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;MEM + SP ADDRESS
;POINTER TO CORRECT DATA
;LOAD 8 WORDS OF MAIN MEMORY

```

5025	030440	035010				MEMDAT		: POINTER TO DATA
5026	030442	004737	034720			JSR	PC, SPLD	: LOAD 8 WORDS OF SP
5027	030446	035020				SPDAT		: POINTER TO DATA
5028	030450	004737	034776		1\$:	JSR	PC, SETC	: SET C BIT!
5029	030454	042737	000017	030470		BIC	#17, 2\$: CLEAR ADDRESS FIELD OF INSTRUCTION
5030	030462	050037	030470			BIS	RO, 2\$: ADD ADDRESS TO INSTRUCTION
5031	030466	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5032	030470	010000			2\$:	010000		: LOAD MAR
5033	030472	042737	000017	030506		BIC	#17, 3\$: CLEAR ADDRESS OF INSTRUCTION
5034	030500	050037	030506			BIS	RO, 3\$: ADD ADDRESS TO INSTRUCTION
5035	030504	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5036	030506	040640			3\$:	040400! (12*20)		: BR + A OR NOTB
5037	030510	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5038	030512	061224				61224		: MOVE BR TO PORT4
5039	030514	111205				MOVB	(R2), R5	: PUT "EXPECTED" IN R5
5040	030516	116104	000004			MOVB	4(R1), R4	: PUT "FOUND" IN R4
5041	030522	120504				CMPB	R5, R4	: DATA CORRECT?
5042	030524	001401				BEQ	4\$: BR IF YES
5043	030526	104015				HLT	1\$: ALU ERROR
5044	030530	104401			4\$:	SCOPI		: SW09=1?
5045	030532	005202				INC	R2	: NEXT DATA
5046	030534	005200				INC	PC	: NEXT ADDRESS
5047	030536	022700	000010			CMP	#10, RO	: DONE YET?
5048	030542	001342				BNE	1\$: BR IF NO
5049	030544	104400				SCOPE		: SCOPE THIS TEST
5050	030546	377	000	377	5\$:	.BYTE	-1, 0, -1, -1, -1, 125, 252, -1	
5051	030551	377	377	125				
5052	030554	252	377					
5053						.EVEN		
5054								
5055								
5056								: ***** TEST 120 *****
5057								: *ALU TEST
5058								: *TEST OF ALU FUNCTION A AND B WITH C BIT SET
5059								: *ALU FUNCTION (A AND B) CODE=13
5060								: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
5061								: *PERFORM THE FUNCTION, VERIFY THE RESULTS
5062								: *****
5063								
5064								
5065								: TEST 120
5066	030556	012737	000120	001226		TST120:	MOV	#120, TSTNO
5067	030564	012737	030732	001216			MOV	#TST121, NEXT
5068	030572	012737	030624	001220			MOV	#1\$, LOCK
5069								: R1 CONTAINS BASE DMC11 ADDRESS
5070	030600	104412				MSTCLR		: MASTER CLEAR DMC11
5071	030602	005000				CLR	RO	: MEM + SP ADDRESS
5072	030604	012702	030722			MOV	#5\$, R2	: POINTER TO CORRECT DATA
5073	030610	004737	034664			JSR	PC, MEMLD	: LOAD 8 WORDS OF MAIN MEMORY
5074	030614	035010				MEMDAT		: POINTER TO DATA
5075	030616	004737	034720			JSR	PC, SPLD	: LOAD 8 WORDS OF SP
5076	030622	035020				SPDAT		: POINTER TO DATA
5077	030624	004737	034776		1\$:	JSR	PC, SETC	: SET C BIT!
5078	030630	042737	000017	030644		BIC	#17, 2\$: CLEAR ADDRESS FIELD OF INSTRUCTION
5079	030636	050037	030644			BIS	RO, 2\$: ADD ADDRESS TO INSTRUCTION
5080	030642	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

5137	031044	111205				MOV B	(R2),R5	:PUT "EXPECTED" IN R5
5138	031046	116104	000004			MOV B	4(R1),R4	:PUT "FOUND" IN R4
5139	031052	120504				CMP B	R5,R4	:DATA CORRECT?
5140	031054	001401				BEQ	4\$:BR IF YES
5141	031056	104015				HLT	1\$:ALU ERROR
5142	031060	104401			4\$:	SCOPI		:SW09=1?
5143	031062	005202				INC	R2	:NEXT DATA
5144	031064	005200				INC	R0	:NEXT ADDRESS
5145	031066	022700	000010			CMP	#10,R0	:DONE YET?
5146	031072	001342				BNE	1\$:BR IF NO
5147	031074	104400				SCOPE		:SCOPE THIS TEST
5148	031076	000	377	377	5\$:	.BYTE	0,-1,-1,-1,125,-1,-1,252	
5149	031101	377	125	377				
5150	031104	377	252					
5151								.EVEN
5152								
5153								
5154								:***** TEST 122 *****
5155								:*ALU TEST
5156								:*TEST OF ALU FUNCTION A XOR B WITH C BIT SET
5157								:*ALU FUNCTION (A XOR B) CODE=15
5158								:*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
5159								:*PERFORM THE FUNCTION, VERIFY THE RESULTS
5160								:*****
5161								
5162								: TEST 122
5163								
5164	031106	012737	000122	001226	TST122:	MOV	#122,TSTNC	
5165	031114	012737	031262	001216		MOV	#TST123,NEXT	
5166	031122	012737	031154	001220		MOV	#1\$,LOCK	
5167								:R1 CONTAINS BASE DMC11 ADDRESS
5168	031130	104412				MSTCLR		:MASTER CLEAR DMC11
5169	031132	005000				CLR	R0	:MEM + SP ADDRESS
5170	031134	012702	031252			MOV	#5\$,R2	:POINTER TO CORRECT DATA
5171	031140	004737	034664			JSR	PC,MEMLD	:LOAD 8 WORDS OF MAIN MEMORY
5172	031144	035010				MEMDAT		:POINTER TO DATA
5173	031146	004737	034720			JSR	PC,SPLD	:LOAD 8 WORDS OF SP
5174	031152	035020				SPDAT		:POINTER TO DATA
5175	031154	004737	034776		1\$:	JSR	PC,SETC	:SET C BIT!
5176	031160	042737	000017	031174		BIC	#17,2\$:CLEAR ADDRESS FIELD OF INSTRUCTION
5177	031166	050037	031174			BIS	R0,2\$:ADD ADDRESS TO INSTRUCTION
5178	031172	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5179	031174	010000			2\$:	010000		:LOAD MAR
5180	031176	042737	000017	031212		BIC	#17,3\$:CLEAR ADDRESS OF INSTRUCTION
5181	031204	050037	031212			BIS	R0,3\$:ADD ADDRESS TO INSTRUCTION
5182	031210	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5183	031212	040720			3\$:	040400!(15*20)		:BR + A XOR B
5184	031214	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5185	031216	061224				61224		:MOVE BR TO PORT4
5186	031220	111205				MOV B	(R2),R5	:PUT "EXPECTED" IN R5
5187	031222	116104	000004			MOV B	4(R1),R4	:PUT "FOUND" IN R4
5188	031226	120504				CMP B	R5,R4	:DATA CORRECT?
5189	031230	001401				BEQ	4\$:BR IF YES
5190	031232	104015				HLT	1\$:ALU ERROR
5191	031234	104401			4\$:	SCOPI		:SW09=1?
5192	031236	005202				INC	R2	:NEXT DATA


```

5193 031240 005200
5194 031242 022700 000010
5195 031246 001342
5196 031250 104400
5197 031252 000 377 377
5198 031255 000 000 377
5199 031260 377 000
5200
5201
5202
5203
5204
5205
5206
5207
5208
5209
5210
5211
5212
5213 031262 012737 000123 001226
5214 031270 012737 031436 001216
5215 031276 012737 031330 001220
5216
5217 031304 104412
5218 031306 005000
5219 031310 012702 031426
5220 031314 004737 034664
5221 031320 035010
5222 031322 004737 034720
5223 031326 035020
5224 031330 004737 034776
5225 031334 042737 000017 031350
5226 031342 050037 031350
5227 031346 104414
5228 031350 010000
5229 031352 042737 000017 031366
5230 031360 050037 031366
5231 031364 104414
5232 031366 040400
5233 031370 104414
5234 031372 061224
5235 031374 111205
5236 031376 116104 000004
5237 031402 120504
5238 031404 001401
5239 031406 104015
5240 031410 104401
5241 031412 005202
5242 031414 005200
5243 031416 022700 000010
5244 031422 001342
5245 031424 104400
5246 031426 000 377 377
5247 031431 376 252 377
5248 031434 377 124

```

```

INC RO :NEXT ADDRESS
CMP #10,RO :DONE YET?
BNE 1$ :BR IF NO
SCOPE :SCOPE THIS TEST
.BYTE 0,-1,-1,0,0,-1,-1,0

```

5\$:

.EVEN

```

:***** TEST 123 *****
:ALU TEST
:TEST OF ALU FUNCTION ADD WITH C BIT SET
:ALU FUNCTION (A PLUS B) CODE=00
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

TEST 123

```

TST123: MOV #123,TSTNO
MOV #TST124,NEXT
MOV #1$,LOCK

```

```

MSTCLR :R1 CONTAINS BASE DMC11 ADDRESS
CLR RO :MASTER CLEAR DMC11
MOV #5$,R2 :MEM + SP ADDRESS
JSR PC,MEMLD :POINTER TO CORRECT DATA
MEMDAT :LOAD 8 WORDS OF MAIN MEMORY
JSR PC,SPLD :POINTER TO DATA
SPDAT :LOAD 8 WORDS OF SP
1$: JSR PC,SETC :POINTER TO DATA
BIC #17,2$ :SET C BIT!
BIS RO,2$ :CLEAR ADDRESS FIELD OF INSTRUCTION
ROMCLK :ADD ADDRESS TO INSTRUCTION
010000 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2$: BIC #17,3$ :LOAD MAR
BIS RO,3$ :CLEAR ADDRESS OF INSTRUCTION
ROMCLK :ADD ADDRESS TO INSTRUCTION
040400!<00*20> :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3$: MOVB (R2),R5 :BR + ADD
ROMCLK :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 :MOVE BR TO PORT4
MOVB 4(R1),R4 :PUT "EXPECTED" IN R5
CMPB R5,R4 :PUT "FOUND" IN R4
BEQ 4$ :DATA CORRECT?
HLT 1$ :BR IF YES
4$: SCOPE :ALU ERROR
INC R2 :SW09=1?
INC RO :NEXT DATA
CMP #10,RO :NEXT ADDRESS
BNE 1$ :DONE YET?
SCOPE :BR IF NO
.BYTE 0,-1,-1,376,252,-1,-1,124 :SCOPE THIS TEST

```

5249
5250
5251
5252
5253
5254
5255
5256
5257
5258
5259
5260
5261
5262
5263
5264
5265
5266
5267
5268
5269
5270
5271
5272
5273
5274
5275
5276
5277
5278
5279
5280
5281
5282
5283
5284
5285
5286
5287
5288
5289
5290
5291
5292
5293
5294
5295
5296
5297
5298
5299
5300
5301
5302
5303
5304

.EVEN

***** TEST 124 *****
:ALU TEST
:TEST OF ALU FUNCTION 2A W/C WITH C BIT SET
:ALU FUNCTION (A PLUS A PLUS C) CODE=6
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

: TEST 124

TST124: MOV #124,TSTNO
MOV #TST125,NEXT
MOV #1\$,LOCK

MSTCLR
CLR R0
MOV #5\$,R2
JSR PC,MEMLD
MEMDAT
JSR PC,SPLD
SPDAT
1\$: JSR PC,SETC
BIC #17,2\$
BIS R0,2\$
ROMCLK
010000
2\$: BIC #17,3\$
BIS R0,3\$
ROMCLK
040400! (6*20)
3\$: ROMCLK
61224
MOV# (R2),R5
MOV# 4(R1),R4
CMPB R5,R4
BEQ 4\$
HLT 1\$
4\$: SCOPE
INC R2
INC R0
CMP #10,R0
BNE 1\$
SCOPE
5\$: .BYTE 1,1,-1,-1,253,253,125,125

:R1 CONTAINS BASE DMC11 ADDRESS
:MASTER CLEAR DMC11
:MEM + SP ADDRESS
: POINTER TO CORRECT DATA
:LOAD 8 WORDS OF MAIN MEMORY
: POINTER TO DATA
:LOAD 8 WORDS OF SP
: POINTER TO DATA
:SET C BIT!
:CLEAR ADDRESS FIELD OF INSTRUCTION
:ADD ADDRESS TO INSTRUCTION
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:LOAD MAR
:CLEAR ADDRESS OF INSTRUCTION
:ADD ADDRESS TO INSTRUCTION
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:BR + 2A W/C
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:MOVE BR TO PORT4
:PUT "EXPECTED" IN R5
:PUT "FOUND" IN R4
:DATA CORRECT?
:BR IF YES
:ALU ERROR
:SW09=1?
:NEXT DATA
:NEXT ADDRESS
:DONE YET?
:BR IF NO
:SCOPE THIS TEST

.EVEN

***** TEST 125 *****
:ALU TEST
:TEST OF ALU FUNCTION SJB WITH C BIT SET
:ALU FUNCTION (A-B) CODE=16

```

5305
5306
5307
5308
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5310
5311 031612 012737 000125 001226
5312 031620 012737 031766 001216
5313 031626 012737 031660 001220
5314
5315 031634 104412
5316 031636 005000
5317 031640 012702 031756
5318 031644 004737 034664
5319 031650 035010
5320 031652 004737 034720
5321 031656 035020
5322 031660 004737 034776
5323 031664 042737 000017 031700
5324 031672 050037 031700
5325 031676 104414
5326 031700 010000
5327 031702 042737 000017 031716
5328 031710 050037 031716
5329 031714 104414
5330 031716 040740
5331 031720 104414
5332 031722 061224
5333 031724 111205
5334 031726 116104 000004
5335 031732 120504
5336 031734 001401
5337 031736 104015
5338 031740 104401
5339 031742 005202
5340 031744 005200
5341 031746 022700 000010
5342 031752 001342
5343 031754 104400
5344 031756 000 001 377
5345 031761 000 000 253
5346 031764 125 000
5347
5348
5349
5350
5351
5352
5353
5354
5355
5356
5357
5358
5359
5360 031766 012737 000126 001226

```

```

; *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; :*****
: TEST 125
-----
TST125: MOV #125,TSTNO
MOV #TST126,NEXT
MOV #1$,LOCK

MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
CLR RO ;MASTER CLEAR DMC11
MOV #5$,R2 ;MEM + SP ADDRESS
JSR PC,MEMLD ; POINTER TO CORRECT DATA
MEMDAT ;LOAD 8 WORDS OF MAIN MEMORY
JSR PC,SPLD ; POINTER TO DATA
SPDAT ;LOAD 8 WORDS OF SP
1$: JSR PC,SETC ; POINTER TO DATA
BIC #17,2$ ;SET C BIT!
BIS RO,2$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ;LOAD MAR
2$: BIC #17,3$ ;CLEAR ADDRESS OF INSTRUCTION
BIS RO,3$ ;ADD ADDRESS TO INSTRUCTION
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400! <16*20> ;BR + SUB
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ;MOVE BR TO PORT4
MOV8 (R2),R5 ;PUT "EXPECTED" IN R5
MOV8 4(R1),R4 ;PUT "FOUND" IN R4
CMPB R5,R4 ;DATA CORRECT?
BEQ 4$ ;BR IF YES
HLT 15 ;ALU ERROR
4$: SCOP1 ;SW09=1?
INC R2 ;NEXT DATA
INC RO ;NEXT ADDRESS
CMP #10,RO ;DONE YET?
BNE 1$ ;BR IF NO
SCOPE ;SCOPE THIS TEST
5$: .BYTE 0,1,-1,0,0,253,125,0

.EVEN

;***** TEST 126 *****
; *ALU TEST
; *TEST OF ALU FUNCTION ADD W/C WITH C BIT SET
; *ALU FUNCTION (A PLUS B PLUS C) CODE=01
; *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; :*****
: TEST 126
-----
TST126: MOV #126,TSTNO

```

```

5361 031774 012737 032142 001216
5362 032002 012737 032034 001220
5363
5364 032010 104412
5365 032012 005000
5366 032014 012702 032132
5367 032020 004737 034664
5368 032024 035010
5369 032026 004737 034720
5370 032032 035020
5371 032034 004737 034776
5372 032040 042737 000017 032054
5373 032046 050037 032054
5374 032052 104414
5375 032054 010000
5376 032056 042737 000017 032072
5377 032064 050037 032072
5378 032070 104414
5379 032072 040420
5380 032074 104414
5381 032076 061224
5382 032100 111205
5383 032102 116104 000004
5384 032106 120504
5385 032110 001401
5386 032112 104015
5387 032114 104401
5388 032116 005202
5389 032120 005200
5390 032122 022700 000010
5391 032126 001342
5392 032130 104400
5393 032132 001 000 000
5394 032135 377 253 000
5395 032140 000 125
5396
5397
5398
5399
5400
5401
5402
5403
5404
5405
5406
5407
5408
5409 032142 012737 000127 001226
5410 032150 012737 032316 001216
5411 032156 012737 032210 001220
5412
5413 032164 104412
5414 032166 005000
5415 032170 012702 032306
5416 032174 004737 034664

```

```

MOV #TST127,NEXT
MOV #15,LOCK
MSTCLR
CLR R0
MOV #55,R2
JSR PC,MEMLD
MEMDAT
JSR PC,SPLD
SPDAT
JSR PC,SETC
BIC #17,25
BIS R0,25
ROMCLK
010000
BIC #17,35
BIS R0,35
ROMCLK
040400! <01*20>
ROMCLK
61224
MOVB (R2),R5
MOVB 4(R1),R4
CMPB R5,R4
BEQ 45
HLT 15
SCOPI
INC R2
INC R0
CMP #10,R0
BNE 15
SCOPE
.BYTE 1,0,0,-1,253,0,0,125

```

```

:R1 CONTAINS BASE DMC11 ADDRESS
:MASTER CLEAR DMC11
:MEM + SP ADDRESS
:POINTER TO CORRECT DATA
:LOAD 8 WORDS OF MAIN MEMORY
:POINTER TO DATA
:LOAD 8 WORDS OF SP
:POINTER TO DATA
:SET C BIT!
:CLEAR ADDRESS FIELD OF INSTRUCTION
:ADD ADDRESS TO INSTRUCTION
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:LOAD MAR
:CLEAR ADDRESS OF INSTRUCTION
:ADD ADDRESS TO INSTRUCTION
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:BR + ADD W/C
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:MOVE BR TO PORT4
:PUT "EXPECTED" IN R5
:PUT "FOUND" IN R4
:DATA CORRECT?
:BR IF YES
:ALU ERROR
:SW09=1?
:NEXT DATA
:NEXT ADDRESS
:DONE YET?
:BR IF NO
:SCOPE THIS TEST

```

```

:***** TEST 127 *****
:*ALU TEST
:*TEST OF ALU FUNCTION SUB W/C WITH C BIT SET
:*ALU FUNCTION (A-B-C) CODE=2
:*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:*PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

```

: TEST 127
:-----
TST127: MOV #127,TSTNO
MOV #TST130,NEXT
MOV #15,LOCK

```

```

MSTCLR
CLR R0
MOV #55,R2
JSR PC,MEMLD
:R1 CONTAINS BASE DMC11 ADDRESS
:MASTER CLEAR DMC11
:MEM + SP ADDRESS
:POINTER TO CORRECT DATA
:LOAD 8 WORDS OF MAIN MEMORY

```

.EVEN

5417	032200	035010				MEMDAT		: POINTER TO DATA
5418	032202	004737	034720			JSR	PC, SPLD	: LOAD 8 WORDS OF SP
5419	032206	035020				SPDAT		: POINTER TO DATA
5420	032210	004737	034776		1\$:	JSR	PC, SETC	: SET C BIT!
5421	032214	042737	000017	032230		BIC	#17, 2\$: CLEAR ADDRESS FIELD OF INSTRUCTION
5422	032222	050037	032230			BIS	RO, 2\$: ADD ADDRESS TO INSTRUCTION
5423	032226	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5424	032230	010000			2\$:	010000		: LOAD MAR
5425	032232	042737	000017	032246		BIC	#17, 3\$: CLEAR ADDRESS OF INSTRUCTION
5426	032240	050037	032246			BIS	RO, 3\$: ADD ADDRESS TO INSTRUCTION
5427	032244	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5428	032246	040440			3\$:	040400! (2*20)		: BR + SUB W/C
5429	032250	104414				ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5430	032252	061224				61224		: MOVE BR TO PORT4
5431	032254	111205				MOVB	(R2), R5	: PUT "EXPECTED" IN R5
5432	032256	116104	000004			MOVB	4(R1), R4	: PUT "FOUND" IN R4
5433	032262	120504				CMPB	R5, R4	: DATA CORRECT?
5434	032264	001401				BEQ	4\$: BR IF YES
5435	032266	104015				HLT	1\$: ALU ERROR
5436	032270	104401			4\$:	SCOPI		: SW09=1?
5437	032272	005202				INC	R2	: NEXT DATA
5438	032274	005200				INC	RO	: NEXT ADDRESS
5439	032276	022700	000010			CMP	#10, RO	: DONE YET?
5440	032302	001342				BNE	1\$: BR IF NO
5441	032304	104400				SCOPE		: SCOPE THIS TEST
5442	032306	000	001	377	5\$:	.BYTE	0, 1, -1, 0, 0.253, 125, 0	
5443	032311	000	000	253				
5444	032314	125	000					

.EVEN

```

:***** TEST 130 *****
:*ALU TEST
:*TEST OF ALU FUNCTION INC A WITH C BIT SET
:*ALU FUNCTION (A PLUS 1) CODE=3
:*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:*PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****
    
```

; TEST 130

5458	032316	012737	000130	001226		TST130:	MOV	#130, TSTNO	
5459	032324	012737	032472	001216			MOV	#TST131, NEXT	
5460	032332	012737	032364	001220			MOV	#1\$, LOCK	
5461									: R1 CONTAINS BASE DMC11 ADDRESS
5462	032340	104412				MSTCLR			: MASTER CLEAR DMC11
5463	032342	005000				CLR	RO		: MEM + SP ADDRESS
5464	032344	012702	032462			MOV	#5\$, R2		: POINTER TO CORRECT DATA
5465	032350	004737	034664			JSR	PC, MEMLD		: LOAD 8 WORDS OF MAIN MEMORY
5466	032354	035010				MEMDAT			: POINTER TO DATA
5467	032356	004737	034720			JSR	PC, SPLD		: LOAD 8 WORDS OF SP
5468	032362	035020				SPDAT			: POINTER TO DATA
5469	032364	004737	034776		1\$:	JSR	PC, SETC		: SET C BIT!
5470	032370	042737	000017	032404		BIC	#17, 2\$: CLEAR ADDRESS FIELD OF INSTRUCTION
5471	032376	050037	032404			BIS	RO, 2\$: ADD ADDRESS TO INSTRUCTION
5472	032402	104414				ROMCLK			: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

5473	032404	010000			2\$:	010000	:LOAD MAR
5474	032406	042737	000017	032422		BIC #17,3\$:CLEAR ADDRESS OF INSTRUCTION
5475	032414	050037	032422			BIS RO,3\$:ADD ADDRESS TO INSTRUCTION
5476	032420	104414				ROMCLK	:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5477	032422	040460			3\$:	040400! <3*20>	:BR + INC A
5478	032424	104414				ROMCLK	:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5479	032426	061224				61224	:MOVE BR TO PORT4
5480	032430	111205				MOVB (R2),R5	:PUT "EXPECTED" IN R5
5481	032432	116104	000004			MOVB 4(R1),R4	:PUT "FOUND" IN R4
5482	032436	120504				CMPB R5,R4	:DATA CORRECT?
5483	032440	001401				BEQ 4\$:BR IF YES
5484	032442	104015				HLT 1\$:ALU ERROR
5485	032444	104401			4\$:	SCOPI	:SW09=1?
5486	032446	005202				INC R2	:NEXT DATA
5487	032450	005200				INC RO	:NEXT ADDRESS
5488	032452	022700	000010			CMP #10,RO	:DONE YET?
5489	032456	001342				BNE 1\$:BR IF NO
5490	032460	104400				SCOPE	:SCOPE THIS TEST
5491	032462	001	001	000	5\$:	.BYTE 1,1,0,0,126,126,253,253	
5492	032465	000	126	126			
5493	032470	253	253				
5494						.EVEN	
5495							
5496							
5497							
5498							
5499							
5500							
5501							
5502							
5503							
5504							
5505							
5506							
5507	032472	012737	000131	001226	TST131:	MOV #131,TSTNO	
5508	032500	012737	032646	001216		MOV #TST132,NEXT	
5509	032506	012737	032540	001220		MOV #1\$,LOCK	
5510							
5511	032514	104412				MSTCLR	:R1 CONTAINS BASE DMC11 ADDRESS
5512	032516	005000				CLR RO	:MASTER CLEAR DMC11
5513	032520	012702	032636			MOV #5\$,R2	:MEM + SP ADDRESS
5514	032524	004737	034664			JSR PC,MEMLD	:POINTER TO CORRECT DATA
5515	032530	035010				MEMDAT	:LOAD 8 WORDS OF MAIN MEMORY
5516	032532	004737	034720			JSR PC,SPLD	:POINTER TO DATA
5517	032536	035020				SPDAT	:LOAD 8 WORDS OF SP
5518	032540	004737	034776		1\$:	JSR PC,SETC	:POINTER TO DATA
5519	032544	042737	000017	032560		BIC #17,2\$:SET C BIT!
5520	032552	050037	032560			BIS RO,2\$:CLEAR ADDRESS FIELD OF INSTRUCTION
5521	032556	104414				ROMCLK	:ADD ADDRESS TO INSTRUCTION
5522	032560	010000			2\$:	010000	:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5523	032562	042737	000017	032576		BIC #17,3\$:LOAD MAR
5524	032570	050037	032576			BIS RO,3\$:CLEAR ADDRESS OF INSTRUCTION
5525	032574	104414				ROMCLK	:ADD ADDRESS TO INSTRUCTION
5526	032576	040520			3\$:	040400! <5*20>	:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5527	032600	104414				ROMCLK	:BR + 2A
5528	032602	061224				61224	:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
							:MOVE BR TO PCRT4

```

:***** TEST 131 *****
:ALU TEST
:TEST OF ALU FUNCTION 2A WITH C BIT SET
:ALU FUNCTION (A PLUS A) CODE=5
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

```

: TEST 131
:-----
TST131: MOV #131,TSTNO
MOV #TST132,NEXT
MOV #1$,LOCK

:R1 CONTAINS BASE DMC11 ADDRESS
:MASTER CLEAR DMC11
:MEM + SP ADDRESS
:POINTER TO CORRECT DATA
:LOAD 8 WORDS OF MAIN MEMORY
:POINTER TO DATA
:LOAD 8 WORDS OF SP
:POINTER TO DATA
:SET C BIT!
:CLEAR ADDRESS FIELD OF INSTRUCTION
:ADD ADDRESS TO INSTRUCTION
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:LOAD MAR
:CLEAR ADDRESS OF INSTRUCTION
:ADD ADDRESS TO INSTRUCTION
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:BR + 2A
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:MOVE BR TO PCRT4

```

```

5529 032604 111205
5530 032606 116104 000004
5531 032612 120504
5532 032614 001401
5533 032616 104015
5534 032620 104401 4$:
5535 032622 005202
5536 032624 005200
5537 032626 022700 000010
5538 032632 001342
5539 032634 104400
5540 032636 000 000 376 5$:
5541 032641 376 252 252
5542 032644 124 124
5543
5544 .EVEN
5545
5546
5547
5548
5549
5550
5551
5552
5553
5554
5555
5556 032646 012737 000132 001226
5557 032654 012737 033022 001216
5558 032662 012737 032714 001220
5559
5560 032670 104412
5561 032672 005000
5562 032674 012702 033012
5563 032700 004737 034664
5564 032704 035010
5565 032706 004737 034720
5566 032712 035020
5567 032714 004737 034776 1$:
5568 032720 042737 000017 032734
5569 032726 050037 032734
5570 032732 104414
5571 032734 010000 2$:
5572 032736 042737 000017 032752
5573 032744 050037 032752
5574 032750 104414
5575 032752 040500 3$:
5576 032754 104414
5577 032756 061224
5578 032760 111205
5579 032762 116104 000004
5580 032766 120504
5581 032770 001401
5582 032772 104015
5583 032774 104401 4$:
5584 032776 005202

```

```

MOV# (R2),R5 ;PUT "EXPECTED" IN R5
MOV# 4(R1),R4 ;PUT "FOUND" IN R4
CMP# R5,R4 ;DATA CORRECT?
BEQ 4$ ;BR IF YES
HLT 15 ;ALU ERROR
SCOPI ;SW09=1?
INC R2 ;NEXT DATA
INC R0 ;NEXT ADDRESS
CMP #10,R0 ;DONE YET?
BNE 1$ ;BR IF NO
SCOPE ;SCOPE THIS TEST
.BYTE 0,0,376,376,252,252,124,124

***** TEST 132 *****
*ALU TEST
*TEST OF ALU FUNCTION A PLUS C WITH C BIT SET
*ALU FUNCTION (A PLUS C) CODE=4
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

: TEST 132
-----
TST132: MOV #132,TSTNO
MOV #TST133,NEXT
MOV #1$,LOCK

MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
CLR R0 ;MASTER CLEAR DMC11
MOV #5$,R2 ;MEM + SP ADDRESS
JSR PC,MEMLD ;POINTER TO CORRECT DATA
MEMDAT ;LOAD 8 WORDS OF MAIN MEMORY
JSR PC,SPLD ;POINTER TO DATA
SPDAT ;LOAD 8 WORDS OF SP
JSR PC,SETC ;POINTER TO DATA
BIC #17,2$ ;SET C BIT!
BIS R0,2$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
ROMCLK ;ADD ADDRESS TO INSTRUCTION
010000 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
BIC #17,3$ ;LOAD MAR
BIS R0,3$ ;CLEAR ADDRESS OF INSTRUCTION
ROMCLK ;ADD ADDRESS TO INSTRUCTION
040400! <4*20> ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
ROMCLK ;BR + A PLUS C
61224 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
MOV# (R2),R5 ;MOVE BR TO PORT4
MOV# 4(R1),R4 ;PUT "EXPECTED" IN R5
CMP# R5,R4 ;PUT "FOUND" IN R4
BEQ 4$ ;DATA CORRECT?
HLT 15 ;BR IF YES
SCOPI ;ALU ERROR
INC R2 ;SW09=1?
;NEXT DATA

```

```

5585 033000 005200
5586 033002 022700 000010
5587 033006 001342
5588 033010 104400
5589 033012 001 001 000 5$:
5590 033015 000 126 126
5591 033020 253 253
5592
5593
5594
5595
5596
5597
5598
5599
5600
5601
5602
5603
5604
5605 033022 012737 000133 001226
5606 033030 012737 033176 001216
5607 033036 012737 033070 001220
5608
5609 033044 104412
5610 033047 005000
5611 033050 012702 033166
5612 033054 004737 034664
5613 033060 035010
5614 033062 004737 034720
5615 033066 035020
5616 033070 004737 034776 1$:
5617 033074 042737 000017 033110
5618 033102 057037 033110
5619 033106 1.414
5620 033110 010000 2$:
5621 033112 042737 000017 033126
5622 033120 050037 033126
5623 033124 104414
5624 033126 040760 3$:
5625 033130 104414
5626 033132 061224
5627 033134 111205
5628 033136 116104 000004
5629 033142 120504
5630 033144 001401
5631 033146 104015
5632 033150 104401 4$:
5633 033152 005202
5634 033154 005200
5635 033156 022700 000010
5636 033162 001342
5637 033164 104400
5638 033166 377 000 376 5$:
5639 033171 377 377 252
5640 033174 124 377

```

```

INC RO ;NEXT ADDRESS
CMP #10,RO ;DONE YET?
BNE 1$ ;BR IF NO
SCOPE ;SCOPE THIS TEST
.BYTE 1,1,0,0,126,126,253,253

.EVEN

:***** TEST 133 *****
:ALU TEST
:TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT SET
:ALU FUNCTION (A-B-1) CODE=17
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

; TEST 133
-----
TST133: MOV #133,TSTNO
MOV #TST134,NEXT
MOV #1$,LOCK

MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
CLR RO ;MASTER CLEAR DMC11
MOV #5$,R2 ;MEM + SP ADDRESS
JSR PC,MEMLD ;POINTER TO CORRECT DATA
MEMDAT ;LOAD 8 WORDS OF MAIN MEMORY
JSR PC,SPLD ;POINTER TO DATA
SPDAT ;LOAD 8 WORDS OF SP
JSR PC,SETC ;POINTER TO DATA
BIC #17,2$ ;SET C BIT!
BIS RO,2$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
ROMCLK ;ADD ADDRESS TO INSTRUCTION
010000 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
BIC #17,3$ ;LOAD MAR
BIS RO,3$ ;CLEAR ADDRESS OF INSTRUCTION
ROMCLK ;ADD ADDRESS TO INSTRUCTION
040400! <17*20> ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ;BR + 2'S COMP SUB
MOV# (R2),R5 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
MOV# 4(R1),R4 ;MOVE BR TO PORT4
CMPB R5,R4 ;PUT "EXPECTED" IN R5
BEQ 4$ ;PUT "FOUND" IN R4
HLT 1$ ;DATA CORRECT?
SCOPE ;BR IF YES
INC R2 ;ALU ERROR
INC RO ;SW09=1?
CMP #10,RO ;NEXT DATA
BNE 1$ ;NEXT ADDRESS
SCOPE ;DONE YET?
.BYTE -1,0,376,-1,-1,252,124,-1 ;BR IF NO
;SCOPE THIS TEST

```


.EVEN

5641
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5682
5683
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5685
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5695
5696

033176 012737 000134 001226
033204 012737 033352 001216
033212 012737 033244 001220

033220 104412
033222 005000
033224 012702 033342
033230 004737 034664
033234 035010
033236 004737 034720
033242 035020
033244 004737 034776
033250 042737 000017 033264
033256 050037 033264
033262 104414
033264 010000
033266 042737 000017 033302
033274 050037 033302
033300 104414
033302 040560
033304 104414
033306 061224
033310 111205
033312 116104 000004
033316 120504
033320 001401
033322 104015
033324 104401
033326 005202
033330 005200
033332 022700 000010
033336 001342
033340 104400
033342 377 377 376
033345 376 124 124
033350 251 251

TST134:

***** TEST 134 *****
*ALU TEST
*TEST OF ALU FUNCTION DEC A WITH C BIT SET
*ALU FUNCTION (A-1) CODE=7
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS

; TEST 134

MOV #134,TSTNO
MOV #TST135,NEXT
MOV #1\$,LOCK

;R1 CONTAINS BASE DMC11 ADDRESS

MSTCLR
CLR R0
MOV #5\$,R2
JSR PC,MEMLD
MEMDAT
JSR PC,SPLD
SPDAT

;MASTER CLEAR DMC11
;MEM + SP ADDRESS
;POINTER TO CORRECT DATA
;LOAD 8 WORDS OF MAIN MEMORY
;POINTER TO DATA
;LOAD 8 WORDS OF SP
;POINTER TO DATA

1\$:

JSR PC,SETC
BIC #17,2\$
BIS R0,2\$

;SET C BIT!
;CLEAR ADDRESS FIELD OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

2\$:

ROMCLK 010000
BIC #17,3\$
BIS R0,3\$

;LOAD MAR
;CLEAR ADDRESS OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

3\$:

ROMCLK 040400! <7*20>
61224

;BR + DEC A
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE BR TO PORT4

MOV (R2),R5
MOV 4(R1),R4
CMPB R5,R4
BEQ 4\$

;PUT "EXPECTED" IN R5
;PUT "FOUND" IN R4
;DATA CORRECT?
;BR IF YES

4\$:

HLT 15
SCOPE1
INC R2
INC R0
CMP #10,R0
BNE 1\$

;ALU ERROR
;SW09=1?
;NEXT DATA
;NEXT ADDRESS
;DONE YET?
;BR IF NO

5\$:

SCOPE
.BYTE -1,-1,376,376,124,124,251,251

;SCOPE THIS TEST

.EVEN

***** TEST 135 *****
*TEST OF PROGRAM CLOCK BIT
*DO A MASTER CLEAR, VERIFY THAT PROGRAM CLOCK IS SET
*WRITE PROGRAM CLOCK BIT TO A ONE, VERIFY THAT IT CLEARS.

```

5697
5698
5699
5700
5701
5702 033352 012737 000135 001226
5703 033360 012737 033532 001216
5704
5705 033366 104412
5706 033370 005037 001416
5707 033374 005037 001246
5708 033400 012702 000011
5709 033404 012761 000020 000004
5710 033412 152761 000002 000001
5711 033420 012761 121111 000006
5712 033426 152761 000003 000001
5713 033434 012761 121224 000006
5714 033442 152761 000003 000001
5715 033450 142761 000003 000001
5716 033456 016104 000004
5717 033462 005005
5718 033464 120504
5719 033466 001401
5720 033470 104016
5721 033472
5722 033472 104414
5723 033474 121224
5724 033476 122761 000020 000004
5725 033504 001411
5726 033506 005237 001416
5727 033512 005537 001246
5728 033516 022737 000006 001246
5729 033524 001362
5730 033526 104016
5731 033530 104400
5732
5733
5734
5735
5736
5737
5738
5739
5740
5741
5742
5743
5744
5745
5746
5747
5748
5749
5750
5751 033532 012737 000136 001226
5752 033540 012737 033724 001216

```

```

: *AND THEN SETS SOME TIME LATER
: *****
: TEST 135
-----
TST135: MOV #135,TSTNO
MOV #TST136,NEXT
MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
CLR TEMP ;MASTER CLEAR DMC11
CLR TEMP1 ;PREPARE FOR
MOV #11,R2 ;DELAY
MOV #20,4(R1) ;SAVE FOR TYPEOUT
BISB #BIT1,1(R1) ;LOAD PORT 4
MOV #121111,6(R1) ;SET ROMI
BISB #BIT1:BIT0,1(R1) ;SET CLOCK BIT
MOV #121224,6(R1) ;LOAD NEXT INSTRUCTION
BISB #BIT1:BIT0,1(R1) ;SET CLOCK BIT
BICB #BIT1:BIT0,1(R1) ;LOAD NEXT INSTRUCTION
MOV 4(R1),R4 ;READ CLOCK BIT
CLR R5 ;CLEAR MAINT BITS
CMPB R5,R4 ;PUT "FOUND" IN R4
BEQ 2$ ;PUT "EXPECTED" IN R5
HLT 16 ;IS PGM CLOCK CLEAR?
2$: ;ERROR, PGM CLOCK IS NOT CLEAR
3$: ROMCLK ;NEXT WORD IS INSTRUCTION. ROMCLK PC=5304
121224 ;PORT4+LUI1
CMPB #20,4(R1) ;IS PGM CLOCK SET?
BEQ 3$ ;BR IF YES
INC TEMP ;INCREMENT DELAY
ADC TEMP1 ;INCREMENT DELAY
CMP #6,TEMP1 ;IS DELAY DONE
BNE 2$ ;BR IF NO
HLT 16 ;ERROR PGM CLOCK NOT SET
3$: SCOPE ;SCOPE THIS TEST

```

```

***** TEST 136 *****
*FORCE POWER FAIL TEST
*SET FORCE POWER FAIL BIT VERIFY THAT PROCESSOR TRAPS TO 24
*GOING DOWN AND COMING UP. VERIFY ALSO THAT BUS INIT WAS
*BLOCKED FROM GETTING TO THE DMC DURING THE POWER FAIL
*THIS TEST MAY HANG ON SOME PROCESSORS IF AN M9301 IS PRESENT.
*TO AVOID HANGING SW02 (POWER ON REBOOT ENABLE) ON THE M9301
*MUST BE IN THE OFF POSITION. THIS TEST WILL ALSO FAIL IF THE
*CPU POWER FAIL VECTOR IS SET TO ANY LOCATION OTHER THAN 24.
*IF THIS TEST HANGS OR FAILS DUE TO EITHER REASON ABOVE THE
*FOLLOWING PATCH MAY BE INSTALLED TO SKIP THIS TEST:
*
* LOC 33362 WAS 33532 SB 33724
*****

```

```

: TEST 136
-----
TST136: MOV #136,TSTNO
MOV #TST137,NEXT

```

```

5753                                     ;R1 CONTAINS BASE DMC11 ADDRESS
5754 033546 104412 MSTCLR                ;MASTER CLEAR DMC11
5755 033550 005037 001416 CLR          TEMP ;PREPARE FOR DELAY
5756 033554 013746 000024 MOV          #0#24, -(SP) ;STORE POWER FAIL ADDRESS
5757 033560 012737 033624 000024 MOV          #1$, #0#24 ;SET UP FOR FORCE POWER FAIL
5758 033566 012761 000002 000004 MOV          #2, 4(R1) ;LOAD PORT4
5759 033574 012711 001000 MOV          #BIT9, (R1) ;SET ROMI
5760 033600 012761 121111 000006 MOV          #121111, 6(R1) ;LOAD INSTRUCTION
5761 033606 012711 001400 MOV          #BIT9!BIT8, (R1) ;CLOCK INSTRUCTION
5762 033612 005237 001416 5$: INC          TEMP ;WAIT FOR POWER FAIL
5763 033616 001375 BNE          5$ ;BR IF DELAY NOT DONE
5764 033620 104017 HLT          17 ;ERROR, NO POWER FAIL
5765 033622 000426 BR          4$
5766 033624 012737 033642 000024 1$: MOV          #3$, #0#24 ;POWER UP ADDRESS
5767 033632 010637 033640 MOV          SP, 2$ ;STORE STACK
5768 033636 000000 HALT ;WAIT FOR POWER UP SEQUENCE
5769 033640 000000 2$: 0
5770 033642 013706 033640 3$: MOV          2$, SP ;RESTORE STACK
5771 033646 022626 POP2SP ;POP STACK TWICE
5772 033650 012637 000024 MOV          (SP)+, #0#24 ;RESTORE TRUE POWER FAIL ADDRESS
5773 033654 022737 005336 000024 CMP          #.PFAIL, #0#24 ;IS IT CORRECT?
5774 033662 001406 BEQ          4$ ;BR IF YES
5775 033664 104017 HLT          17 ;ERROR, STACK IS INCORRECT
5776 033666 012737 005336 000024 MOV          #.PFAIL, #0#24 ;RESTORE TRUE POWER FAIL ADDRESS
5777 033674 012706 001200 MOV          #STACK, SP ;RESTORE STACK
5778 033700 012711 003000 4$: MOV          #BIT9!BIT10, (R1) ;SEL6 = MAINT IR
5779 033704 012705 121111 MOV          #121111, R5 ;R5 = EXPECTED
5780 033710 016104 000004 MOV          4(R1), R4 ;R4 = FOUND
5781 033714 020504 CMP          R5, R4 ;MAINT IR SHOULD = 12111
5782 033716 001401 BEQ          +4 ;BR IF OK
5783 033720 104025 HLT          25 ;IF = 0 THEN BUS INIT WAS
5784                                     ;NOT BLOCKED FROM CLEARING
5785                                     ;THE DMC-11
5786 033722 104400 SCOPE ;SCOPE THIS TEST
5787
5788
5789 ;***** TEST 137 *****
5790 ;*MICRO-PROCESSOR NOISE TEST
5791 ;*WRITE ALL ZERO'S THEN ALL ONE'S THEN A DATA PATTERN
5792 ;*TO THE IBUS* AND IBUS REGISTERS AND TO THE SP AND MAIN MEM
5793 ;*THEN GO BACK AND READ THE DATA PATERNS TO VERIFY THAT
5794 ;*READING AND WRITING OF OTHER LOCATIONS AND REGISTERS
5795 ;*DID NOT CHANGE THE DATA.
5796 ;*****
5797
5798 ; TEST 137
5799 ;-----
5800 033724 012737 000137 001226 TST137: MOV          #137, TSTNO
5801 033732 012737 003364 001216 MOV          #.EOP, NEXT
5802
5803 033740 104412 MSTCLR                ;R1 CONTAINS BASE DMC11 ADDRESS
5804 033742 005002 CLR          R2 ;MASTER CLEAR DMC11
5805 033744 042737 000017 033770 1$: BIC          #17, 2$ ;R2 IS INDEX REGISTER
5806 033752 156237 034564 033770 B1SB         30$(R2), 2$ ;CLEAR ADDRESS FIELD
5807 033760 116261 034572 000004 MOV          31$(R2), 4(R1) ;ADD IBUS* REG ADDRESS TO INSTRUCTION
5808 033766 104414 ROMCLK ;LOAD PORT4
                                     ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

5809	033770	121100			25:	121100		:WRITE IBUS* REGISTER
5810	033772	005202				INC	R2	:INC INDEX REGISTER
5811	033774	022702	000005			CMP	#5,R2	:DONE YET?
5812	034000	001361				BNE	1\$:BR IF NO
5813	034002	005002				CLR	R2	:R2 IS IBUS REGISTER ADDRESS
5814	034004	042737	000017	034050	35:	BIC	#17,4\$:CLEAR ADDRESS FIELD OF INSTRUCTIONS
5815	034012	042737	000017	034062		BIC	#17,5\$	
5816	034020	042737	000017	034072		BIC	#17,6\$	
5817	034026	050237	034050			BIS	R2,4\$:ADD IBUS REG ADDRESS TO INSTRUCTION
5818	034032	050237	034062			BIS	R2,5\$	
5819	034036	050237	034072			BIS	R2,6\$	
5820	034042	105061	000004			CLRB	4(R1)	:CLEAR PORT4
5821	034046	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5822	034050	122100			45:	122100		:WRITE 0 TO IBUS REG
5823	034052	112761	000377	000004		MOVW	#377,4(R1)	:LOAD PORT4
5824	034060	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5825	034062	122100			55:	122100		:WRITE ALL ONES TO IBUS REG
5826	034064	110261	000004			MOVW	R2,4(R1)	:LOAD PORT4
5827	034070	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5828	034072	122100			65:	122100		:WRITE ITS OWN ADDRESS TO IBUS REG
5829	034074	005202				INC	R2	:NEXT ADDRESS
5830	034076	022702	000010			CMP	#10,R2	:DONE YET?
5831	034102	001340				BNE	3\$:BR IF NO
5832	034104	005002				CLR	R2	:START AT SP ADDRESS C
5833	034106	042737	000017	034152	75:	BIC	#17,8\$:CLEAR ADDRESS FIELD
5834	034114	042737	000017	034164		BIC	#17,9\$	
5835	034122	042737	000017	034174		BIC	#17,10\$	
5836	034130	050237	034152			BIS	R2,8\$:ADD ADDRESS TO INSTRUCTION
5837	034134	050237	034164			BIS	R2,9\$	
5838	034140	050237	034174			BIS	R2,10\$	
5839	034144	105061	000004			CLRB	4(R1)	:CLEAR PORT4
5840	034150	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5841	034152	123100			85:	123100		:WRITE ZERO TO SP
5842	034154	112761	000377	000004		MOVW	#377,4(R1)	:LOAD PORT4
5843	034162	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5844	034164	123100			95:	123100		:WRITE ALL ONES TO SP
5845	034166	110261	000004			MOVW	R2,4(R1)	:LOAD PORT4
5846	034172	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5847	034174	123100			105:	123100		:WRITE SP ADDRESS TO ITSELF
5848	034176	005202				INC	R2	:NEXT SP ADDRESS
5849	034200	022702	000020			CMP	#20,R2	:DONE YET?
5850	034204	001340				BNE	7\$:BR IF NO
5851	034206	005002				CLR	R2	:R2 = MAIN MEM ADDRESS
5852	034210	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5853	034212	010000				010000		:MAR ← 0
5854	034214	105061	000004		115:	CLRB	4(R1)	:CLEAR PORT4
5855	034220	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5856	034222	122500				122500		:WRITE ZEROS TO MEM
5857	034224	112761	000377	000004		MOVW	#377,4(R1)	:LOAD PORT4
5858	034232	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5859	034234	122500				122500		:WRITE ONES TO MEM
5860	034236	110261	000004			MOVW	R2,4(R1)	:LOAD PORT4
5861	034242	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5862	034244	136500				136500		:WRITE TO MEM IT OWN ADDRESS
5863	034246	005202				INC	R2	:NEXT MEM ADDRESS
5864	034250	022702	000400			CMP	#400,R2	:DONE YET?

5865	034254	001357		BNE	11\$;BR IF NO
5866							
5867							;NOW GO BACK AND READ EVERYTHING
5868							
5869	034256	104414		ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5870	034260	010000		010000			;MAR←0
5871	034262	032737	100000	001366	BIT	#BIT15,STAT1	;DMC?
5872	034270	001402			BEQ	.+6	;BR IF YES
5873	034272	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5874	034274	004000			4000		;MAR HI ← 0 (KMC ONLY)
5875	034276	005000			CLR	R0	;R0 IS INDEX REGISTER
5876	034300	042737	000360	034336	12\$:	BIC	#360,13\$
5877	034306	116002	034564			MOV	30\$(R0),R2
5878	034312	010203				MOV	R2,R3
5879	034314	006303				ASL	R3
5880	034316	006303				ASL	R3
5881	034320	006303				ASL	R3
5882	034322	006303				ASL	R3
5883	034324	050337	034336			BIS	R3,13\$
5884	034330	116005	034572			MOV	31\$(R0),R5
5885	034334	104414				ROMCLK	
5886	034336	121004		13\$:	121004		;ADD ADDRESS TO INSTRUCTION
5887	034340	016104	000004			MOV	4(R1),R4
5888	034344	120504				CMP	R5,R4
5889	034346	001401				BEQ	.+4
5890	034350	104004				HLT	4
5891	034352	005200				INC	R0
5892	034354	022700	000005			CMP	#5,R0
5893	034360	001347				BNE	12\$
5894	034362	005002				CLR	R2
5895	034364	042737	000360	034414	14\$:	BIC	#360,15\$
5896	034372	010203				MOV	R2,R3
5897	034374	006303				ASL	R3
5898	034376	006303				ASL	R3
5899	034400	006303				ASL	R3
5900	034402	006303				ASL	R3
5901	034404	050337	034414			BIS	R3,15\$
5902	034410	010205				MOV	R2,R5
5903	034412	104414				ROMCLK	
5904	034414	021004		15\$:	021004		;ADD ADDRESS TO INSTRUCTION
5905	034416	016104	000004			MOV	4(R1),R4
5906	034422	120504				CMP	R5,R4
5907	034424	001401				BEQ	.+4
5908	034426	104005				HLT	5
5909	034430	005202				INC	R2
5910	034432	022702	000010			CMP	#10,R2
5911	034436	001352				BNE	14\$
5912	034440	005002				CLR	R2
5913	034442	042737	000017	034456	16\$:	BIC	#17,17\$;CLEAR ADDRESS FIELD OF INSTRUCTION
5914	034450	050237	034456			BIS	R2,17\$
5915	034454	104414				ROMCLK	
5916	034456	040600		17\$:	040600		;ADD ADDRESS TO INSTRUCTION
5917	034460	010205				MOV	R2,R5
5918	034462	104414				ROMCLK	
5919	034464	061224				061224	;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5920	034466	016104	000004			MOV	4(R1),R4

```

5921 034472 120504      CMPB   R5,R4      ;SP CONTENTS OK?
5922 034474 001401      BEQ    .+4        ;BR IF YES
5923 034476 104007      HLT    ?         ;SP DATA ERROR
5924 034500 005202      INC    R2        ;NEXT SP LOCATION
5925 034502 022702 000020      CMP    #20,R2    ;DONE YET?
5926 034506 001355      BNE   16$       ;BR IF NO
5927 034510 005002      CLR   R2        ;R2 = MEMORY ADDRESS
5928 034512 104414      ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5929 034514 010000      010000 ;MAR ← 0
5930 034516 032737 100000 001366      BIT   #BIT15,STAT1 ;DMC?
5931 034524 001402      BEQ    .+6       ;BR IF YES
5932 034526 104414      ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5933 034530 004000      4000 ;MAR HI ← 0 (KMC ONLY)
5934 034532 010205      19$: MOV    R2,R5   ;R5 = "EXPECTED"
5935 034534 104414      ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5936 034536 055224      055224 ;PORT4 ← MAIN MEM
5937 034540 016104 000304      MOV    4(R1),R4  ;R4 = "FOUND"
5938 034544 120504      CMPB  R5,R4     ;MAIN MEM CONTENTS OK?
5939 034546 001401      BEQ    .+4       ;BR IF YES
5940 034550 104013      HLT   13        ;MAIN MEM DATA ERROR
5941 034552 005202      INC   R2        ;NEXT MEM ADDRESS
5942 034554 022702 000400      CMP    #400,R2  ;DONE YET?
5943 034560 001364      BNE   18$       ;BR IF NO
5944 034562 104400      SCOPE ;SCOPE THIS TEST
5945 034564      000      002      003      30$: .BYTE 0,2,3,5,10
5946 034567      005      010
5947      034572
5948 034572      001      003      304      31$: .BYTE 1,3,4,6,10
5949 034575      006      010
5950      034600
5951
5952      00200
5953      00300
5954      00400 ;SUBROUTINES
5955      00500 ;-----
5956      034600      00600
5957      00700 SETVEC:
5958      00800 ;THIS SUBROUTINE LOADS THE VECTORS AND VECTOR LEVELS
5959      00900
5959 034600 012577 144570      01000 MOV    (R5)+,DMRVEC ;LOAD BASE VECTOR
5960 034604 012577 144570      01100 MOV    (R5)+,DMTVEC ;LOAD VECTOR + 2
5961 034610 112577 144562      01200 MOVB  (R5)+,DMRLVL ;LOAD VECTOR + 4
5962 034614 112577 144562      01300 MOVB  (R5)+,DMTLVL ;LOAD VECTOR + 6
5963 034620 000205      01400 RTS    R5        ;RETURN
5964      01500
5965      01600
5966 034622      01700 NPRSET:
5967      01800 ;THIS SUBROUTINE LOADS IBUS REGISTERS 0-7
5968      01900 ;WITH NPR INFORMATION (INBA, OUTBA, OUT DATA)
5969      02000
5970 034622 010246      02100 MOV    R2,-(SP)  ;SAVE R2
5971 034624 005002      02200 CLR   R2        ;START AT IBUS REG 0
5972 034626 112561 000004      02300 1$: MOVB  (R5)+,4(R1) ;LOAD PORT4
5973 034632 042737 000017 034646      02400 BIC   #17,2$   ;CLEAR ADDRESS FIELD OF INSTRUCTION
5974 034640 050237 034646      02500 BIS   R2,2$    ;ADD ADDRESS TO INSTRUCTION
5975 034644 104414      ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5976 034646 122100      2$: 122100 ;MOVE PORT4 TO IBUS REG

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5977	034650	005202		02800		INC	R2	:NEXT ADDRESS
5978	034652	022702	000010	02900		CMP	#10,R2	:ALL DONE?
5979	034656	001363		03000		BNE	1\$:BR IF NO
5980	034660	012602		03100		MOV	(SP)+,R2	:RESTORE R2
5981	034662	000205		03200		RTS	R5	:RETURN
5982				03300				
5983				03400				
5984	034664			03500	MEMLD:			
5985				03600				:THIS SUBROUTINE LOADS THE FIRST 8 LOCATIONS OF MAIN
5986				03700				:MEMORY WITH THIS DATA: 0,-1,0,-1,125,252,125,252
5987				03800				
5988	034664	013605		03900		MOV	2(SP)+,R5	:PUT POINTER TO DATA IN R5
5989	034666	062746	000002	04000		ADD	#2,-(SP)	:ADJUST STACK
5990	034672	012704	000010	04100		MOV	#10,R4	:DO 8 LOADS
5991	034676	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5992	034700	010000		04300		010000		:MAR < 0
5993	034702	112577	144504	04400	1\$:	MOVB	(R5)+,2DMP04	:LOAD PORT4
5994	034706	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5995	034710	136500		04600		136500		:MOV DATA TO MEM, AUTO INC MAR
5996	034712	005304		04700		DEC	R4	:DECREMENT COUNT
5997	034714	001372		04800		BNE	1\$:BR IF NOT DONE
5998	034716	000207		04900		RTS	PC	:RETURN
5999				05000				
6000				05100				
6001	034720			00200	SPLD:			
6002				00300				:THIS SUBROUTINE LOADS THE FIRST 8 SCRATCH PAD
6003				00400				:LOCATIONS WITH: 0,0,-1,-1,125,125,252,252
6004				00500				
6005	034720	013605		00600		MOV	2(SP)+,R5	:PUT POINTER TO DATA IN R5
6006	034722	062746	000002	00700		ADD	#2,-(SP)	:ADJUST STACK
6007	034726	005004		00800		CLR	R4	:START AT SP ADDRESS 0
6008	034730	112577	144456	00900	1\$:	MOVB	(R5)+,2DMP04	:LOAD PORT4 WITH DATA
6009	034734	042737	000017	01000		BIC	#17,2\$:CLEAR ADDRESS FIELD OF INSTRUCTION
6010	034742	050437	034750	01100		BIS	R4,2\$:ADD ADDRESS TO INSTRUCTION
6011	034746	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6012	034750	123100		01300	2\$:	123100		:MOVE DATA TO SP
6013	034752	005204		01400		INC	R4	:INCREMENT COUNT
6014	034754	022704	000010	01500		CMP	#10,R4	:DONE YET?
6015	034760	001363		01600		BNE	1\$:BR IF NO
6016	034762	000207		01700		RTS	PC	:RETURN
6017				01800				
6018				01900				
6019	034764			02000	CLRC:			
6020				02100				:THIS SUBROUTINE CLEARS THE MICRO PROCESSOR C BIT
6021				02200				
6022	034764	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6023	034766	010000		02400		010000		:MAR=0
6024	034770	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6025	034772	040400		02600		040400! (0*20)		:CLEAR C BIT
6026	034774	000207		02700		RTS	PC	:RETURN
6027				02800				
6028				02900				
6029	034776			03000	SETC:			
6030				03100				:THIS SUBROUTINE SETS THE MICRO PROCESSOR C BIT
6031				03200				
6032	034776	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

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6033 035000 010003 03400 010003 :MAR+3
6034 035002 104414 ROMCLK :NEXT WORD IS INSTRUCTION, ROMCLK PC=53C4
6035 035004 040403 03600 040403! <0*20> :SET C BIT
6036 035006 000207 03700 RTS PC :RETURN
6037 03800
6038 03900
6039 035010 000 377 000 04000 MEMDAT: .BYTE 0,-1,0,-1,125,252,125,252
6040 035013 377 125 252
6041 035016 125 252
6042 035020 000 000 377 04100 SPDAT: .BYTE 0,0,-1,-1,125,125,252,252
6043 035023 377 125 125
6044 035026 252 252
6045
6046 035030 052777 044516 052502 04200 .EVEN
035075 377 047125 041111 00400 EM1: .ASCIZ <377>/UNIBUS REGISTER ADDRESSING TIME-OUT/
035136 046777 041511 047522 00500 EM2: .ASCIZ <377>/UNIBUS REGISTER WRITE/READ TEST/
035164 046777 041511 047522 00600 EM3: .ASCIZ <377>/MICRO PROCESSOR TEST/
035225 377 051102 051040 00700 EM4: .ASCIZ <377>/MICRO PROCESSOR WRITE/READ TEST/
035247 377 041523 040522 00800 EM5: .ASCIZ <377>/BR REGISTER TEST/
035271 377 042504 044526 00900 EM6: .ASCIZ <377>/SCRATCH PAD TEST/
035325 377 042504 044526 01000 EM7: .ASCIZ <377>/DEVICE FAILED TO INTERRUPT/
035371 377 050116 020122 01100 EM10: .ASCIZ <377>/DEVICE INTERRUPTED TO WRONG VECTOR/
035403 377 040515 047111 01200 EM11: .ASCIZ <377>/NPR TEST/
035425 377 040515 020122 01300 EM12: .ASCIZ <377>/MAIN MEMORY TEST/
035437 377 046101 020125 01400 EM13: .ASCIZ <377>/MAR TEST/
035451 377 051120 043517 01500 EM14: .ASCIZ <377>/ALU TEST/
035475 377 047506 041522 01600 EM15: .ASCIZ <377>/PROGRAM CLOCK TEST/
035525 377 047125 054105 01700 EM16: .ASCIZ <377>/FORCE POWER FAIL ERROR/
035553 377 046504 030503 01800 EM17: .ASCIZ <377>/UNEXPECTED INTERRUPT/
035606 046777 044501 052116 01900 EM20: .ASCIZ <377>/DMC11 CONFIGURATION ERROR/
035655 377 047520 042527 02000 EM21: .ASCIZ <377>/MAINTENANCE INSTRUCTION REGISTER TEST/
02100 EM22: .ASCIZ <377>/POWER FAIL INITIALIZE FAILURE/
035714 051377 043505 051511 02200 DH1: .ASCIZ <377>/REGISTER TRAPPED FROM
035755 377 054105 042520 02300 DH2: .ASCIZ <377>/EXPECTED FOUND REGISTER/
036013 377 054105 042520 02400 DH3: .ASCIZ <377>/EXPECTED FOUND
036034 042777 050130 041505 02500 DH4: .ASCIZ <377>/EXPECTED FOUND IBUS* REGISTER
036076 042777 050130 041505 02600 DH5: .ASCIZ <377>/EXPECTED FOUND IBUS REGISTER
036137 377 054105 042520 02700 DH6: .ASCIZ <377>/EXPECTED FOUND ADDRESS
02800 .EVEN
02900
036174 000002 03000 DT1: 2
036176 006 015 03100 .BYTE 6,15
036200 001262 03200 SAVR1
036202 006 002 03300 .BYTE 6,2
036204 001264 03400 SAVR2
036206 000003 03500 DT2: 3
036210 006 004 03600 .BYTE 6,4
036212 001272 03700 SAVR5
036214 006 004 03800 .BYTE 6,4
036216 001270 03900 SAVR4
036220 006 002 04000 .BYTE 6,2
036222 001262 04100 SAVR1
036224 000002 04200 DT3: 2
036226 006 004 04300 .BYTE 6,4
036230 001272 04400 SAVR5
036232 006 002 04500 .BYTE 6,2

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036234	001270		04600		SAVR4		
036236	000003		04700	DT4:	3		
036240	003	007	04800		.BYTE	3.7	
036242	001272		04900		SAVR5		
036244	003	011	05000		.BYTE	3.11	
036246	001270		05100		SAVR4		
036250	002	002	05200		.BYTE	2.2	
036252	001264		05300		SAVR2		
036254	000003		05400	DT5:	3		
036256	003	007	05500		.BYTE	3.7	
036260	001272		05600		SAVR5		
036262	003	007	05700		.BYTE	3.7	
036264	001270		05800		SAVR4		
036266	006	002	05900		.BYTE	6.2	
036270	001264		06000		SAVR2		
036272	000002		06100	DT6:	2		
036274	003	007	06200		.BYTE	3.7	
036276	001272		06300		SAVR5		
036300	003	002	06400		.BYTE	3.2	
036302	001270		06500		SAVR4		
036304	000002		06600	DT7:	2		
036306	006	004	06700		.BYTE	5.4	
036310	001262		06800		SAVR1		
036312	006	002	06900		.BYTE	6.2	
036314	001404		07000		DMCSR		
036316			07100	.ERRTAB:			
036316	000000		07200		0		
036320	000000		07300		0		
036322	000000		07400		0		
036324	035030		07500		EM1		
036326	035714		07600		DM1	:HLT	1
036330	036174		07700		DT1		
036332	035075		07800		EM2		
036334	035755		07900		DM2	:HLT	2
036336	036206		08000		DT2		
036340	035136		08100		EM3		
036342	036013		08200		DM3	:HLT	3
036344	036224		08300		DT3		
036346	035164		08400		EM4		
036350	036034		08500		DM4	:HLT	4
036352	036236		08600		DT4		
036354	035164		08700		EM4		
036356	036076		08800		DM5	:HLT	5
036360	036236		08900		DT4		
036362	035225		09000		EM5		
036364	036013		09100		DM3	:HLT	6
036366	036272		09200		DT6		
036370	035247		09300		EM6		
036372	036137		09400		DM6	:HLT	7
036374	036254		09500		DT5		
036376	035271		09600		EM7		
036400	000000		09700		0	:HLT	10
036402	000000		09800		0		
036404	035325		09900		EM10		
036406	000000		10000		0	:HLT	11
036410	000000		10100		0		

036412	035371	10200	EM11		
036414	036013	10300	DH3	:HLT	12
036416	036224	10400	DT3		
036420	035403	10500	EM12		
036422	036137	10600	DH6	:HLT	13
036424	036254	10700	DT5		
036426	035425	10800	EM13		
036430	036137	10900	DH6	:HLT	14
036432	036254	11000	DT5		
036434	035437	11100	EM14		
036436	036013	11200	DH3	:HLT	15
036440	036272	11300	DT6		
036442	035451	11400	EM15		
036444	036034	11500	DH4	:HLT	16
036446	036236	11600	DT4		
036450	035475	11700	EM16		
036452	000000	11800	0	:HLT	17
036454	000000	11900	0		
036456	035525	12000	EM17		
036460	000000	12100	0	:HLT	20
036462	000000	12200	0		
036464	035371	12300	EM11		
036466	036137	12400	DH6	:HLT	21
036470	036254	12500	DT5		
036472	035553	12600	EM20		
036474	036013	12700	DH3	:HLT	22
036476	036304	12800	DT7		
036500	035606	12900	EM21		
036502	036013	13000	DH3	:HLT	23
036504	036224	13100	DT3		
036506	035553	13200	EM20		
036510	000000	13300	0	:HLT	24
036512	000000	13400	0		
036514	035655	13500	EM22		
036516	036013	13600	DH3	:HLT	25
036520	036224	13700	DT3		
		13800			
036522		13900			
	000001	14400			

CORMAX:
.END

*ST12	013372	1915	1944#
*ST120	030556	5018	5066#
TST121	030732	5067	5115#
TST122	031106	5116	5164#
TST123	031262	5165	5213#
TST124	031436	5214	5262#
*ST125	031612	5263	5311#
TST126	031766	5312	5360#
TST127	032142	5361	5409#
TST13	013470	1945	1974#
*ST130	032316	5410	5458#
TST131	032472	5459	5507#
TST132	032646	5508	5556#
*ST133	033022	5557	5605#
TST134	033176	5606	5654#
TST135	033352	5655	5702#
TST136	033532	5703	5751#
TST137	033724	5752	5800#
TST14	013566	1975	2004#
TST140=	***** U	5801	
TST15	013664	2005	2034#
*ST16	013762	2035	2064#
TST17	014060	2065	2094#
TST18	012426	1676	1703#
*ST20	014156	2095	2124#
TST21	014254	2125	2154#
TST22	014352	2155	2184#
TST23	014450	2185	2214#
TST24	014546	2215	2244#
TST25	014672	2245	2287#
TST26	015016	2288	2330#
*ST27	015146	2331	2372#
TST3	012456	1704	1722#
TST30	015306	2373	2413#
TST31	015450	2414	2456#
TST32	015534	2457	2481#
*ST33	015734	2482	2537#
*ST34	016134	2538	2593#
TST35	016310	2594	2645#
TST36	016464	2646	2698#
*ST37	016664	2699	2756#
*ST4	012606	1723	1764#
TST40	017104	2757	2816#
TST41	017260	2817	2868#
TST42	017434	2869	2920#
TST43	017610	2921	2972#
*ST44	017764	2973	3024#
*ST45	020140	3025	3076#
*ST46	020314	3077	3128#
TST47	020470	3129	3180#
*ST5	012704	1765	1794#
*ST50	020644	3181	3232#
TST51	021072	3233	3293#
*ST52	021242	3294	3344#
*ST53	021510	3345	3410#
*ST54	021732	3411	3469#

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02DMC MACY11 30(1046) 11-JUL-77 10:53 PAGE 125
02DMC.P11 23-MAY-77 11:16 CROSS REFERENCE TABLE -- USER SYMBOLS

TST55	022026	3470	3498#											
*ST56	022120	3499	3527#											
*ST57	022240	3528	3565#											
TST6	013002	1795	1924#											
*ST60	022404	3566	3608#											
TST61	022510	3609	3641#											
*ST62	022624	3642	3677#											
*ST63	022726	3678	3710#											
*ST64	023064	3711	3749#											
TST65	023210	3750	3785#											
*ST66	023320	3786	3820#											
TST67	023426	3821	3855#											
TST7	013100	1825	1854#											
*ST70	023624	3857	3910#											
TST71	023752	3911	3950#											
TST72	024104	3951	3993#											
TST73	024304	3994	4049#											
TST74	024440	4050	4094#											
TST75	024552	4095	4135#											
*ST76	024726	4136	4184#											
TST77	025102	4185	4233#											
TST	003612	717	718*	720*	721*	784#								
TWCSYN=	010000	96#												
*YPSAT	005206	1055	1073	1076#										
*YPE =	104402	221#	513	525	537	622	627	635	639	670	675	716	725	739
		739	741	743	745	833	846	863	956	996	1056	1057	1060	1061
		1063	1065	1069	1074	1123	1229	1232	1284	1330	1348	1354	1392	1414
		1428	1431	1438	1441	1448	1454	1463	1470	1477	1592			
*YPM5G	005106	1053	1056#											
VEC	006526	1189#	1406											
VECMAP	012010	1591	1603#											
WHICH	012002	1394	1599#											
WPCNT	004710	964*	997*	1005#										
WPKO.F	005174	1068	1071#											
XBX	005000	1030	1032	1034#										
XCSR	003546	740	765#											
YERR	003570	746	774#											
XHEAD	006224	537	1189#											
XLOC	003022	595*	613*	616	647	660#								
XPASS	003562	744	771#											
XSTATQ	007454	546	1189#											
XTSTN	005330	1062	1102#											
XVEC	003554	742	768#											
ZERC	001300	188#												
\$COD =	*****	1												
\$CRAP =	:77777	1#	1666#	1669	1671#	1695#	1698	1699#	1712#	1715	1718#	1754#	1757	1760#
		1784#	1787	1790#	1814#	1817	1820#	1844#	1847	1850#	1874#	1877	1880#	1904#
		1907	1910#	1934#	1937	1940#	1964#	1967	1970#	1994#	1997	2000#	2024#	2027
		2030#	2054#	2057	2060#	2084#	2087	2090#	2114#	2117	2120#	2144#	2147	2150#
		2174#	2177	2180#	2204#	2207	2210#	2234#	2237	2240#	2277#	2280	2283#	2320#
		2323	2326#	2362#	2355	2368#	2403#	2406	2409#	2444#	2447	2452#	2471#	2474
		2477#	2527#	2530	2533#	2583#	2586	2589#	2635#	2638	2641#	2687#	2690	2694#
		2744#	2747	2752#	2806#	2809	2812#	2858#	2861	2864#	2910#	2913	2916#	2962#
		2965	2968#	3014#	3017	3020#	3066#	3069	3072#	3118#	3121	3124#	3170#	3173
		3176#	3222#	3225	3228#	3283#	3286	3289#	3334#	3337	3340#	3400#	3403	3406#
		3460#	3463	3465#	3489#	3492	3494#	3517#	3520	3523#	3555#	3558	3561#	3595#

CROSS REFERENCE TABLE -- USER SYMBOLS

3602	3604	3632	3635	3637	3668	3671	3673	3700	3703	3706	3739	3742
3745	3775	3778	3781	3810	3813	3816	3845	3848	3851	3901	3904	3906
3941	3944	3946	3983	3986	3989	4039	4042	4045	4085	4088	4090	4123
4126	4131	4172	4175	4180	4221	4224	4229	4270	4273	4278	4319	4322
4327	4368	4371	4376	4417	4420	4425	4466	4469	4474	4515	4518	4523
4564	4567	4572	4613	4616	4621	4662	4665	4670	4711	4714	4719	4760
4763	4768	4809	4812	4817	4858	4861	4866	4907	4910	4915	4956	4959
4964	5005	5008	5013	5054	5057	5062	5103	5106	5111	5152	5155	5160
5201	5204	5209	5250	5253	5258	5299	5302	5307	5348	5351	5356	5397
5400	5405	5446	5449	5454	5495	5498	5503	5544	5547	5552	5593	5596
5601	5642	5645	5650	5691	5694	5698	5732	5735	5747	5787	5790	5796
123	511	757	1081									
1	1666	1671	1673	1679	1695	1699	1701	1706	1712	1719	1720	1726
1727	1754	1760	1762	1767	1768	1784	1790	1792	1797	1798	1814	1820
1822	1827	1828	1844	1850	1852	1857	1858	1874	1880	1882	1887	1888
1904	1910	1912	1917	1918	1934	1940	1942	1947	1948	1964	1970	1972
1977	1978	1994	2000	2002	2007	2008	2024	2030	2032	2037	2038	2054
2060	2062	2067	2068	2084	2090	2092	2097	2098	2114	2120	2122	2127
2128	2144	2150	2152	2157	2158	2174	2180	2182	2197	2188	2204	2210
2212	2217	2218	2234	2240	2242	2247	2248	2277	2283	2285	2290	2291
2320	2326	2328	2334	2335	2362	2368	2370	2376	2377	2403	2409	2411
2417	2418	2444	2452	2454	2459	2460	2471	2477	2479	2485	2486	2521
2533	2535	2541	2542	2583	2589	2591	2597	2598	2635	2641	2643	2649
2650	2687	2694	2696	2702	2703	2744	2752	2754	2760	2761	2806	2812
2814	2820	2821	2858	2864	2866	2872	2873	2910	2916	2918	2924	2925
2962	2968	2970	2976	2977	3014	3020	3022	3028	3029	3066	3072	3074
3080	3081	3118	3124	3126	3132	3133	3170	3176	3178	3184	3185	3222
3228	3230	3236	3237	3283	3289	3291	3297	3298	3334	3340	3342	3348
3349	3400	3406	3408	3414	3415	3460	3465	3467	3472	3474	3489	3494
3496	3501	3502	3517	3523	3525	3530	3531	3555	3561	3563	3568	3569
3599	3604	3606	3611	3613	3632	3637	3639	3644	3645	3668	3673	3675
3680	3681	3700	3706	3708	3713	3714	3739	3745	3747	3752	3753	3775
3781	3783	3788	3789	3810	3816	3818	3823	3824	3845	3851	3853	3859
3860	3901	3906	3908	3914	3915	3941	3946	3948	3954	3955	3983	3989
3991	3997	3998	4039	4045	4047	4052	4053	4095	4090	4092	4098	4099
4123	4131	4133	4139	4140	4172	4180	4182	4188	4189	4221	4229	4231
4237	4237	4270	4278	4279	4280	4286	4287	4319	4327	4329	4329	4335
4336	4368	4376	4377	4378	4384	4385	4417	4425	4426	4427	4433	4434
4466	4474	4475	4476	4482	4483	4515	4523	4524	4525	4531	4532	4564
4572	4573	4574	4580	4581	4613	4621	4622	4623	4629	4630	4662	4670
4671	4672	4678	4679	4711	4719	4720	4721	4727	4729	4750	4768	4769
4770	4776	4777	4809	4817	4818	4819	4825	4826	4858	4866	4867	4868
4874	4875	4907	4915	4916	4917	4923	4924	4956	4964	4965	4966	4972
4973	5005	5013	5014	5015	5021	5022	5054	5062	5063	5064	5070	5071
5103	5111	5112	5113	5119	5120	5152	5160	5161	5162	5168	5169	5201
5209	5210	5211	5217	5218	5250	5258	5259	5260	5266	5267	5299	5307
5308	5309	5315	5316	5348	5356	5357	5358	5364	5365	5397	5405	5406
5407	5413	5414	5446	5454	5455	5456	5462	5463	5495	5503	5504	5505
5511	5512	5544	5552	5553	5554	5560	5561	5593	5601	5602	5603	5609
5610	5642	5650	5651	5652	5658	5659	5691	5698	5699	5700	5705	5706
5732	5747	5748	5749	5754	5755	5787	5796	5797	5798	5803	5804	6046
1	1676	1679	1704	1706	1723	1727	1765	1768	1795	1798	1825	1828
1855	1858	1885	1888	1915	1918	1945	1948	1975	1978	2005	2008	2035
2038	2065	2068	2095	2098	2125	2129	2155	2158	2185	2199	2215	2219
2245	2248	2288	2291	2331	2335	2373	2377	2414	2419	2457	2462	2482
2486	2528	2542	2594	2598	2646	2650	2699	2703	2757	2761	2817	2821

SENCAD = 003522
SN = 000137

SE = 000141

\$RAMCL	1#	1133													
\$RCLK	1#	1136	1139	1176	1181	2491	2493	2511	2513	2547	2549	2567	2569	2602	2604
	2620	2622	2654	2656	2672	2674	2708	2710	2728	2730	2766	2768	2788	2790	2825
	2827	2843	2845	2877	2879	2895	2897	2929	2931	2947	2949	2981	2983	2999	3001
	3033	3035	3051	3053	3085	3087	3103	3105	3137	3139	3155	3157	3189	3191	3207
	3209	3243	3251	3269	3301	3303	3319	3321	3354	3358	3360	3377	3381	3383	3421
	3425	3427	3445	3447	3480	3508	3544	3584	3621	3653	3657	3659	3689	3722	3730
	3732	3766	3768	3795	3798	3801	3830	3833	3836	3876	3919	3922	3924	3925	3960
	3963	3965	3967	4001	4004	4006	4008	4023	4025	4027	4054	4058	4061	4067	4071
	4074	4104	4106	4108	4110	4149	4153	4155	4198	4202	4204	4247	4251	4253	4296
	4300	4302	4345	4349	4351	4394	4398	4400	4443	4447	4449	4492	4496	4498	4541
	4545	4547	4590	4594	4596	4639	4643	4645	4688	4692	4694	4737	4741	4743	4786
	4790	4792	4835	4839	4841	4884	4888	4890	4933	4937	4939	4982	4986	4988	5031
	5035	5037	5080	5084	5086	5129	5133	5135	5178	5182	5184	5227	5231	5233	5276
	5280	5282	5325	5329	5331	5374	5378	5380	5423	5427	5429	5472	5476	5478	5521
	5525	5527	5570	5574	5576	5619	5623	5625	5668	5672	5674	5722	5808	5821	5824
	5827	5840	5843	5846	5852	5855	5858	5861	5869	5873	5885	5903	5915	5918	5928
	5932	5935	5975	5991	5994	6011	6022	6024	6032	6034					
\$SCOPE	1#	777													
\$SIMBC	1#														
\$SOFTC	1#	1209													
\$SPF	1#	3350	3372												
\$SP1	1#	3334													
\$SP2	1#	3400													
\$TIMER	1#	5691													
\$TRPDE	1#	217	219	221	223	225	227	229	231	233	235	237	239	241	243
\$TS^N	245														
	1#	1673	1701	1720	1762	1792	1822	1852	1882	1912	1942	1972	2002	2032	2062
	2092	2122	2152	2182	2212	2242	2295	2328	2370	2411	2454	2479	2535	2591	2643
	2696	2754	2814	2866	2919	2970	3022	3074	3126	3178	3230	3291	3342	3408	3467
	3496	3525	3563	3606	3639	3675	3708	3747	3783	3818	3853	3908	3948	3991	4047
	4092	4133	4182	4231	4280	4329	4378	4427	4476	4525	4574	4623	4672	4721	4770
	4819	4868	4917	4966	5015	5064	5113	5162	5211	5260	5309	5358	5407	5456	5505
	5554	5603	5652	5700	5749	5798									
\$VARIA	1#	136													
\$WRFLT	1#	2249	2262	2292	2305										
\$WR46	1#	2234	2277												
\$XZ	1#	1666	1671	1695	1699	1712	1718	1754	1760	1784	1790	1814	1820	1844	1850
	1874	1880	1904	1910	1934	1940	1964	1970	1994	2000	2024	2030	2054	2060	2084
	2090	2114	2120	2144	2150	2174	2180	2204	2210	2234	2240	2277	2283	2320	2326
	2362	2368	2403	2409	2444	2452	2471	2477	2527	2533	2583	2589	2635	2641	2687
	2694	2744	2752	2806	2812	2858	2864	2910	2916	2962	2968	3014	3020	3066	3072
	3118	3124	3170	3176	3222	3228	3283	3289	3334	3340	3400	3406	3460	3465	3489
	3494	3517	3523	3555	3561	3599	3604	3632	3637	3668	3673	3700	3706	3739	3745
	3775	3781	3810	3816	3845	3851	3901	3906	3941	3946	3983	3989	4039	4045	4085
	4090	4123	4131	4172	4180	4221	4229	4270	4278	4319	4327	4368	4376	4417	4425
	4466	4474	4515	4523	4564	4572	4613	4621	4662	4670	4711	4719	4760	4768	4809
	4817	4858	4866	4907	4915	4956	4964	5005	5013	5054	5062	5103	5111	5153	5160
	5201	5209	5250	5258	5299	5307	5348	5356	5397	5405	5446	5454	5495	5503	5544
	5552	5593	5601	5642	5650	5691	5698	5732	5747	5787	5796				

. ABS. 036522 COC

ERRORS DETECTED: 0

DZDMC DZDMC/SOL/CRF+IPLUTL,DZDMC
RUN-TIME: 18 25 1 SECONDS
RUN-TIME RATIO: 1675/46=35.8
CORE USED: 27K (53 PAGES)