

# DH11

DIAGNOSTIC  
MD-11-DZDHM-B

EP-DZDHM-B-DL-A NOV 1976  
COPYRIGHT © 1976  
FICHE 1 OF 2 MADE IN U.S.

The image displays a grid of 100 small diagnostic charts or tables, arranged in 10 rows and 10 columns. Each chart contains various data points, possibly representing engine performance metrics or diagnostic test results. The charts are too small to read individually but appear to follow a consistent layout. The overall appearance is that of a technical manual or diagnostic aid for the MD-11 aircraft engine.



# DH11

DIAGNOSTIC  
MD-11-DZDHM-B

EP-DZDHM-B-DL-A  
COPYRIGHT © 1976

NOV 1976  
**digital**  
MADE IN USA

FICHE 2 OF 2



PRODUCT CODE: MAINDEX-11-DZDM-2  
 PRODUCT NAME: DHI1 DIAGNOSTIC  
 DATE: 21 SEPTEMBER-1976  
 AUTHOR: E. CRAWLEY  
 MAINTAINED BY: DIAGNOSTIC ENGINEERING

COPYRIGHT (C) 1976

DIGITAL EQUIPMENT CORPORATION, MAYNARD, MASS.

THIS SOFTWARE IS FURNISHED UNDER A LICENSE FOR USE ONLY ON A  
 SINGLE COMPUTER SYSTEM AND MAY BE COPIED ONLY WITH THE  
 INCLUSION OF THE ABOVE COPYRIGHT NOTICE. THIS SOFTWARE, OR  
 ANY OTHER COPIES THEREOF, MAY NOT BE PROVIDED OR OTHERWISE  
 MADE AVAILABLE TO ANY OTHER PERSON EXCEPT FOR USE ON SUCH  
 SYSTEM AND TO ONE WHO AGREES TO THESE LICENSE TERMS. TITLE  
 AND OWNERSHIP OF THE SOFTWARE SHALL AT ALL TIMES REMAIN  
 IN DEC.

THE INFORMATION IN THIS DOCUMENT IS SUBJECT TO CHANGE  
 WITHOUT NOTICE AND SHOULD NOT BE CONSTRUED AS A COMMITMENT  
 BY DIGITAL EQUIPMENT CORPORATION.

DEC ASSUMES NO RESPONSIBILITY FOR THE USE OR RELIABILITY OF  
 THE SOFTWARE IN EQUIPMENT WHICH IS NOT SUPPLIED BY DEC.

TABLE OF CONTENTS

: SEQ 0002

1.0	GENERAL PROGRAM DESCRIPTION
1.01	PROGRAM PURPOSE
1.1.1	LOGIC TEST SUMMARY
1.1.2	MD-11-DZCHM CORE MEMORY MAP
1.2	SYSTEM REQUIREMENTS
1.2.1	HARDWARE REQUIREMENTS
1.2.2	SOFTWARE REQUIREMENTS
1.3	RELATED DOCUMENTS AND STANDARDS
1.4	DIAGNOSTIC HIERARCHY PREREQUISITES
1.5	FAILURE ASSUMPTIONS
2.0	OPERATING INSTRUCTIONS
2.1	LOADING AND STARTING PROCEDURES
2.1.1	LOADING PROCEDURES
2.1.2	STARTING PROCEDURES
2.2	SPECIAL ENVIRONMENTS
2.2.1	ACT11/APT11
2.2.2	"XXDP" SYSTEMS
2.2.3	SWITCHLESS FEATURE
2.3	PROGRAM OPTIONS
2.3.1	CONSOLE SWITCH REGISTER
2.3.2	CORE MEMORY LOCATIONS
2.3.3	REGISTER USAGE
2.4	EXECUTION TIMES
3.0	ERROR INFORMATION
3.1	ERROR REPORTING PROCEDURES
3.1.1	STANDARD SYSMAC SML ERROR REPORTING CONVENTIONS
3.1.2	ERROR MESSAGE TABLE
3.1.3	DATA HEADER MNEUMONIC DEFINITIONS
3.2	POWER FAIL PRINTOUT
3.3	ERROR HALTS
4.0	PERFORMANCE AND PROGRESS REPORTS
4.1	PERFORMANCE REPORTS
4.2	PROGRESS REPORTS



5.0	DH11 DEVICE INFORMATION
5.1	ADDRESS AND VECTOR ASSIGNMENTS
5.2	REGISTER DEFINITIONS
5.2.1	SYSTEM CONTROL REGISTER
5.2.2	NEXT RECEIVED CHARACTER REGISTER
5.2.3	LINE PARAMETER REGISTER
5.2.4	CURRENT ADDRESS REGISTER
5.2.5	BYTE COUNT REGISTER
5.2.6	BUFFER ACTIVE REGISTER
5.2.7	BREAK CONTROL REGISTER
5.2.8	SILO STATUS REGISTER
5.3	DH11 FUNCTIONAL LOGIC PARTITIONING
5.4	DH11 MODULE ALLOCATION CHART
6.0	MAINTENANCE PROCEDURES
6.1	INTRODUCTION
6.2	PRELIMINARY CHECKS
6.3	MAINTENANCE CONNECTORS
6.4	COMPLETE DH11 SUB-SYSTEM CHECKOUT
6.5	MAINTENANCE HEADER DESCRIPTION



1.0 GENERAL PROGRAM DESCRIPTION  
-----

SEQ 0004

1.1 PROGRAM PURPOSE  
-----

"MD-11-DZCHM" IS A COMPREHENSIVE DIAGNOSTIC TEST PROGRAM DESIGNED TO AID IN THE ACCEPTANCE TESTING, INSTALLATION CHECKOUT, AND CORRECTIVE MAINTENANCE OF THE DM11 16. LINE ASYNCHRONOUS SERIAL LINE MULTIPLEXOR. IT CONSISTS OF 44 LOGICALLY SEQUENCED DIAGNOSTIC TESTS DESIGNED TO TEST AND VERIFY THAT THE DM11 IS OPERATING IN ACCORDANCE WITH ITS DESIGN SPECIFICATIONS.

THE PROGRAM IS CONFIGURABLE BY THE AUTOSIZER OR BY CONSOLE DIALOGUE TO ENABLE IT TO AUTOMATICALLY TEST AND VERIFY ALL 16. LINES ON UP TO 16. CONTIGUOUS DM11'S (WITH NON-CONTIGUOUS/CONTIGUOUS VECTOR ASSIGNMENTS). INDIVIDUAL UNITS AND INDIVIDUAL LINES WITHIN A UNIT MAY BE SELECTED OR DESELECTED TO FACILITATE FAULT ISOLATION TO A PARTICULAR DM11 OR A FUNCTIONAL AREA OF LOGIC AFFECTING A PARTICULAR LINE WITHIN A UNIT. WHENEVER AN ERROR IS DETECTED A COMPREHENSIVE ERROR REPORT IS TYPED THAT ALLOWS THE USER TO ISOLATE THE FAULT TO A FUNCTIONAL AREA OF LOGIC. EXTENSIVE DOCUMENTATION IS PROVIDED TO PERMIT THE USER TO PROCEED FROM THE ERROR REPORT TO ADDITIONAL LOGIC CHECKS TO MAKE IN ORDER TO ISOLATE THE PROBLEM TO A REPLACEABLE UNIT.

IN ORDER TO FACILITATE INSTALLATION CHECKOUT, TESTS 101, AND 105 THROUGH 107 (TEST GROUP 1) OF THE DM11-BB MODEM CONTROL DIAGNOSTIC, DZDHK, HAVE BEEN INCLUDED IN THIS PROGRAM. IN THIS WAY ALL THE LEVEL CONVERTERS AND CABLES CAN BE CHECKED WITH JUST ONE PROGRAM USING THE H315 TURNAROUND CONNECTOR. HOWEVER, RUNNING THESE TESTS REQUIRE OPERATOR INTERVENTION (SRIO=1) OTHERWISE, THE TESTS ARE BYPASSED. (REFER TO SECTION 6.3)



T1 CHECK SSYN RESPONSE FROM ALL DM11 REGISTERS  
 T2 TEST THAT "MASTER CLR" CAN CLEAR THE "SCR", "LPR", "BKR", AND "SSR" REGS  
 T3 TEST "SCR" REG R/W BITS CAN SET/CLR (NORMAL MODE)  
 T4 TEST "SCR" REG. READ ONLY BITS (NORMAL MODE)  
 T5 TEST "SCR" REG. BITS THAT CAN BE SET/CLR IN MAINT. MODE  
 T6 TEST THAT ALL R/W BITS IN "LPR" CAN BE SET/CLR  
 T7 TEST THAT ALL R/W BITS IN "BKR" CAN BE SET/CLR  
 T10 TEST THAT ALL R/W BITS IN "SSR" CAN BE SET/CLR  
 T11 TEST THAT CLR SET OF BIT "N" IN "LPR" DOES NOT CLEAR ANY OTHER BITS  
 T12 TEST THAT CLR SET OF BIT "N" IN "BKR" DOES NOT CLEAR ANY OTHER BITS  
 T13 TEST THAT CLR SET OF BIT "N" IN "SSR" DOES NOT CLEAR ANY OTHER BITS  
 T14 "CAR" MEMORY ADDRESSING TEST  
 T15 "BCR" MEMORY ADDRESSING TEST  
 T16 "CAR" REGISTER TEST - ALL 1'S / ALL 0'S - ALL LINES  
 T17 "BCR" REGISTER TEST - ALL 1'S / ALL 0'S - ALL LINES  
 T20 "CAR" MEMORY PATTERNS TEST / 0'S DISTURB  
 T21 "BCR" MEMORY PATTERNS TEST / 0'S DISTURB  
 T22 "CAR" MEMORY PATTERNS TEST / 1'S DISTURB  
 T23 "BCR" MEMORY PATTERNS TEST / 1'S DISTURB  
 T24 TEST THAT "CAR" MEMORY EXT BITS SET/CLR PROPERLY  
 T25 TEST INTR. ENAB. BITS - INTR. CONDITION DISABLED  
 T26 TEST CHAR. AVAIL. I.E. WITH INTR. CONDITION ACTIVE  
 T27 TEST SILO OVFLW. I.E. WITH INTR. CONDITION ACTIVE  
 T28 TEST NON EX MEM I.E. WITH INTR. CONDITION ACTIVE  
 T29 TEST XMITTR DONE I.E. WITH INTR. CONDITION ACTIVE  
 T32 BASIC TRANSMITTER "NPR" LOGIC TEST 1  
 T33 TRANSMITTR NPR LOGIC TEST 2  
 T34 TEST THAT CHARACTER AVAILABLE CAN CAUSE RCVR INTERRUPT  
 T35 TEST THAT THE SILO STATUS REG COUNTS UP CORRECTLY  
 T36 TEST THAT SILO STATUS REGISTER DOWN COUNTS CORRECTLY  
 T37 TEST SILO ALARM LEVEL FOR COUNTS 0, 1, 2, 4, 8, 16, AND 32  
 T40 TRANSMITTER TIMING TEST - ALL SELECTED LINES - ALL SPEEDS  
 T41 RECEIVER TIMING TEST - ALL SELECTED LINES - ALL SPEEDS  
 T42 VERIFY STORAGE OVERFLOW - NON MAINT MODE - ALL SELECTED LINES  
 T43 BASIC DATA TEST - ALL SELECTED LINES/ALL CHAR LENGTHS  
 T44 SINGLE LINE DATA TEST - ALL SELECTED LINES  
 T45 BASIC PARITY LOGIC TEST - ALL SELECTED LINES - ODD PARITY  
 T46 MULTI-LINE PARITY DATA TEST - ALL SELECTED LINES  
 T47 AUTO ECHO TEST 1 - ALL SELECTED LINES  
 T50 AUTO ECHO TEST 2 - ALL SELECTED LINES  
 T51 AUTO ECHO TEST 3 - ALL SELECTED LINES  
 T52 BREAK BIT TEST - ALL SELECTED LINES  
 T53 HALF DUPLEX TEST - ALL SELECTED LINES  
 T54 VERIFY THAT OVERRUN CAN SET PROPERLY - ALL SELECTED LINES  
 T55 ABBREVIATED DM11-BB DIAGNOSTIC. (DZDHK T101)  
 T56 DM11-BB DIAGNOSTIC CONTINUED (DZDHK T105)  
 T57 DM11-BB DIAGNOSTIC CONTINUED (DZDHK T106)  
 T60 DM11-BB DIAGNOSTIC CONTINUED (DZDHK T107)



```

*****
000000: *
*      VECTOR AREA      *
*      *                  *
*****
*      STACK AREA      *
*      *                  *
001100: *
*      SYSMAC CONSTANTS *
*      AND VARIABLES    *
*      *                  *
*****
BEGIN: *
*      START-UP CODE    *
*      *                  *
*****
START1: *
*      START-UP CODE    *
*      *                  *
*****
TST1: *
*      DH11 LOGIC TESTS *
*      TST1(8)-TST54(8) *
*      *                  *
*****
SEOP: *
*      STANDARD SYSMAC  *
*      UTILITY ROUTINES *
*      *                  *
*****
CKRST1: *
*      COMMON DH11 UTILITIES *
*      *                  *
*****
DHADR: *
*      DH11 PROGRAM CONSTANTS *
*      AND VARIABLES      *
*      *                  *
*****
*
*****
* CONT. *
*****
*****
* CONT. *
*****

```

*Handwritten mark*

*Handwritten mark*

# H01

SEQ 0007

\*\*\*\*\*  
\* CONT. \*  
\*\*\*\*\*

\*\*\*\*\*  
\* CONT. \*  
\*\*\*\*\*

EMI:

```
*
*****
*
*   SYSMAC ERROR MESSAGE
*   BUFFERS
*
*
```

TITLE:

```
*
*****
*
*   DH11 MISCELLANEOUS
*   MESSAGE BUFFERS
*
*
```

RBUF:

```
*
*****
*
*   TRANSMIT AND RECEIVE
*   DATA BUFFERS
*
*
*****
```



## 1.2 SYSTEM REQUIREMENTS

---

### 1.2.1 HARDWARE REQUIREMENTS

---

- A. ANY PDP11 COMPUTER SYSTEM WITH 12K OF CORE MEMORY AND A CONSOLE TERMINAL DEVICE (VT50, LA36 ETC)

NOTE: FOR PAPER TAPE SYSTEMS USING THE PDP11 ABSOLUTE LOADER, THE PROGRAM CAN LOAD AND RUN IN 8K OF CORE

- B. A DH11 16. LINE ASYNCHRONOUS SERIAL LINE MULTIPLEXOR

- C. TEST CONNECTORS AND MODULE (THE NO. OF EACH REQUIRED IS DETERMINED BY THE PARTICULAR TEST APPLICATION. REFER TO SECTION 6.3 FOR A COMPLETE DISCUSSION OF THE MAINTENANCE CONNECTORS)

1. H315 TEST CONNECTOR
2. H8611 TEST CONNECTOR
3. M974 TEST MODULE

### 1.2.2 SOFTWARE REQUIREMENTS

---

- A. ACT11/ APT11 THE PROGRAM CONTAINS THE REQUIRED ACT11/APT11 SOFTWARE HOOKS TO PROPERLY INTERFACE WITH THE ACT/APT SYSTEMS. THE PROGRAM CONTAINS AN AUTOSIZER AND CAN BE RUN IN QUICK VERIFY MODE USING "CHAINS".
- B. XXDP THE PROGRAM MAY BE LOADED AND RUN FROM ANY "XXDP" MEDIUM PROVIDED THE SYSTEM HAS AT LEAST 12K OF CORE STORAGE.

## 1.3 RELATED DOCUMENTS AND STANDARDS

---

- A. DH11-0 ENGINEERING DRAWINGS
- B. DH11 MANUAL EK-DH11-MM-002
- C. PDP11 PERIPHERALS HANDBOOK
- D. PDP11 PROCESSOR HANDBOOK
- E. MD-11-DZQAC-C1 SYSMAC.SML
- F. MD-11-DZQXA "XXDP" USER'S GUIDE
- G. DIAGNOSTIC ENGINEERING STANDARDS AND CONVENTIONS PROGRAMMING PRACTICES DOC NO. 175-003-009-00

## 1.4 DIAGNOSTIC HIERARCHY PREREQUISITES

---

MD-11-DZDHM ASSUMES THAT THE FOLLOWING DIAGNOSTICS HAVE BEEN RUN PRIOR TO ITS EXECUTION AND THAT NO ERRORS WERE DETECTED:

- A. CPU/CORE MEMORY DIAGNOSTICS

1.5 FAILURE ASSUMPTIONS  
-----

SEQ 0009

MD-11-DZDHM ASSUMES THAT THE PROGRAM CAN BE LOADED INTO CORE AND STARTED. IT ALSO ASSUMES THE CPU/MEMORY HARDWARE IS FUNCTIONING ERROR FREE.

2.0 OPERATING INSTRUCTIONS  
-----2.1 LOADING AND STARTING PROCEDURES  
-----2.1.1 LOADING PROCEDURES  
-----

## A. PAPER TAPE SYSTEMS

USE THE STANDARD PDP11 ABSOLUTE LOADER PROCEDURE FOR LOADING PAPER TAPES. AFTER LOADING THE PROGRAM MUST BE MANUALLY STARTED AS DESCRIBED IN SECTION 2.1.2.

## B. "XXDP" SYSTEMS (REFER TO "XXDP" USER'S GUIDE MD-11-DZQXA)

1. MOUNT THE APPROPRIATE MEDIUM (DECTAPE, DISK ETC) CONTAINING THE "XXDP" MONITOR AND MD-11-DZDHM.
2. BOOT THE SYSTEM TO LOAD THE MONITOR
3. ONCE LOADED THE "XXDP" MONITOR PRINTS AN INTRODUCTORY MESSAGE AND RESPONDS WITH A "."
4. TYPE: "DZDHMB" FOLLOWED BY EITHER A <CR> CARRIAGE RETURN OR AN "ALTMODE" TO LOAD THE PROGRAM.

IF A <CR> WAS TYPED THE USER MUST MANUALLY START THE PROGRAM AFTER LOADING.

IF THE "ALTMODE" TERMINATOR WAS USED THE PROGRAM WILL SELF START AFTER LOADING.

NOTE: WHENEVER THE DHI1 CONFIGURATION IS CHANGED THE DIAGNOSTIC SHOULD BE RELOADED.



A. TO AUTOMATICALLY START THE PROGRAM USING THE AUTOSIZER  
(START AT LOC 000200(8))

1. INSTALL THE REQUIRED TEST CONNECTORS FOR THE PARTICULAR TEST APPLICATION (REFER TO SECTION 6.3)
2. SET THE HALT/ENABLE SWITCH TO HALT
3. SET THE SR=000200(8)
4. DEPRESS LOAD ADDRESS
5. SET THE SR=000000 (WORST CASE TESTING)

SET THE SR=000002 (TO TYPE THE DEVICE MAP)

SET THE SR=004000 (QUICK PASS)

SET THE SR=002000 (TO PERFORM AN ABBREVIATED DM11-BB TEST.  
REFER TO SECTIONS 1.1 AND 6.3)

SET THE SR=000400 (HALT AFTER PARAMETER SET-UP)

6. SET THE HALT/ENABLE SWITCH TO ENABLE
7. DEPRESS START - THE PROGRAM WILL TEST ALL LINES ON ALL DH'S FOUND.

NOTE: THE CSR REGISTER ADDRESS OF THE DM11-BB('S) IS LOADED ONLY FROM THE AUTOSIZER. HOWEVER, AFTER INITIAL LOAD, THE PROGRAM CAN BE STARTED AT 210(8) TO CHANGE SELECTION PARAMETERS AS DESCRIBED IN SECTION 2.1.2 D.

B. TO TYPE IN ALL REQUIRED PARAMETERS (START AT LOC 000200(8))

1. INSTALL THE REQUIRED TEST CONNECTORS FOR THE PARTICULAR TEST APPLICATION (REFER TO SECTION 6.3)
2. SET THE HALT/ENABLE SWITCH TO HALT
3. SET THE SR=000200(8)
4. DEPRESS LOAD ADDRESS
5. SET THE SR=000001 (FOR INPUT DIALOGUE)

AFTER INPUT DIALOGUE BEGINS BUT PRIOR TO ACTUAL TESTING:  
SET T = SR=000000 (WORST CASE TESTING)

SET THE SR=004000 (QUICK PASS)

SET SR=000400 (HALT AFTER PARAMETER SET-UP)

6. SET THE HALT/ENABLE SWITCH TO ENABLE
7. DEPRESS START - THE PROGRAM TYPES THE TITLE AND THEN ASKS FOR THE NUMBER OF ADDRESSES BETWEEN VECTORS. TYPE EITHER 10(8) OR 20(8) DEPENDING UPON THE PARTICULAR CONFIGURATION TO BE TESTED:

NOTES: IF THE DM11-BB VECTORS ARE INTERLEAVED WITH THE DH11 VECTORS (2040 FRONT END) THE DISPLACEMENT IS 20(8) ADDRESSES.

FOR STANDARD DH11'S WITH CONTIGUOUS VECTORS THE DISPLACEMENT IS 10(8) ADDRESSES.

IF <CR> ONLY WAS TYPED, THE DEFAULT  
WILL BE 20(8) ADDRESSES.

8. THE PROGRAM WILL ASK FOR THE DEVICE ADDRESS.  
TYPE IN THE ADDRESS (OCTAL) OF THE FIRST DH11  
IN THE SYSTEM FOLLOWED BY A <CR>.

IF AN INVALID ADDRESS IS TYPED THE PPROGRAM  
WILL TYPE AN ERROR MESSAGE AND ASK YOU TO  
TRY AGAIN.

9. THE PROGRAM WILL ASK FOR THE VECTOR ADDRESS.  
TYPE IN RECEIVER VECTOR ADDRESS (OCTAL) OF  
THE FIRST DH11 FOLLOWED BY A <CR>.

IF AN INVALID VECTOR ADDRESS IS TYPED THE  
PROGRAM WILL TYPE AN ERROR MESSAGE AND ASK  
YOU TO TRY AGAIN.

10. NEXT THE PROGRAM WILL ASK FOR THE DEVICE SELECTION  
PARAMETER. TYPE IN AN OCTAL NO. ENCODED AS FOLLOWS:

BIT00=1 TEST DH11 #00  
BIT01=1 TEST DH11 #01  
BIT02=0 DO NOT TEST DH11 #02

..

BIT15=1 TEST DH11 #15

EXAMPLES:

177777<CR> TEST ALL 16. DH11'S  
100000<CR> TEST ONLY DH11 #17(9)  
000005<CR> TEST DH11 #00 AND 02

IF A <CR> ONLY IS TYPED THE PROGRAM WILL DEFAULT  
TO THE LAST TYPED IN DEVICE SELECT PARAMETER. IF  
THIS IS THE INITIAL LOAD IT WILL DEFAULT TO  
000003 (DH11 #00 AND 01)

11. NEXT THE PROGRAM WILL ASK FOR THE LINE SELECTION  
PARAMETERS. TYPE AN ENCODED OCTAL NO. AS  
FOLLOWS:

BIT00=1 TEST LINE #00  
BIT01=1 TEST LINE #01  
BIT02=0 DO NOT TEST LINE #02

..

BIT15=1 TEST LINE #15

EXAMPLES:

177777<CR> TEST ALL 16. LINES  
100000<CR> TEST LINE 17(8) ONLY  
000005<CR> TEST LINES 00 AND 02

IF A <CR> RETURN ONLY IS TYPED THE PROGRAM WILL  
DEFAULT TO 16. LINES.



\*\*\*\*\*  
NOTE  
\*\*\*\*\*

IF MORE THAN ONE DH11 IS TESTED THE SAME COMBINATION  
OF LINES WILL BE TESTED ON ALL DH11'S SELECTED.

12. IF SR8=1, THE PROGRAM WILL HALT AND PRINT THE  
FOLLOWING MESSAGE:

"DEPRESS CONTINUE TO START TESTING"

AT THIS POINT SET UP THE DESIRED SWITCH REG-  
ISTER OPTIONS (REFER TO PARA 2.3.1) AND DEPRESS  
"CONTINUE" TO START THE TESTING.

THE PURPOSE OF THIS HALT IS TO ALLOW THE USER TO  
DUMP THE PROGRAM AFTER SETTING UP THE CONFIGURATION  
PARAMETERS FOR HIS SYSTEM.

13. PROGRAM WILL BEGIN EXECUTION. REFER TO SECTIONS  
2.4, 3.0, AND 4.0 FOR ERROR AND STATUS REPORTS.

C. DEFAULT PARAMETER START \*\* (START AT LOC 000204(8))

1. INSTALL THE REQUIRED TEST CONNECTORS FOR THE  
PARTICULAR TEST APPLICATION (REFER TO SECTION 6.3)
2. SET THE HALT/ENABLE SWITCH TO HALT
3. SET THE SR=000204(8)
4. DEPRESS LOAD ADDRESS
5. SET THE SR=000000 (WORST CASE TESTING)
6. SET THE HALT/ENABLE SWITCH TO ENABLE
7. DEPRESS START

\*\* IF THIS IS THE INITIAL LOAD,  
THE DEFAULT PARAMETERS ASSUME TWO DH11'S  
WITH THE FOLLOWING ADDRESS ASSIGNMENTS

DH11 #0 DEVADR=760020, VECTOR=330, BR5  
DH11 #1 DEVADR=760040, VECTOR=350, BR5

OTHERWISE, THE PROGRAM WILL DEFAULT TO  
THE PARAMETERS USED IN THE PREVIOUS EXECUTION.

8. PROGRAM EXECUTION BEGINS. REFER TO SECTIONS 2.4, 3.0,  
AND 4.0 FOR EXECUTION TIMES, ERROR REPORTS, AND  
PROGRESS REPORTS.

D. TO CHANGE DEVICE AND LINE SELECT PARAMETERS ONLY (START AT LOC 000210(8))

1. INSTALL THE REQUIRED TEST CONNECTORS FOR THE  
PARTICULAR TEST APPLICATION (REFER TO SECTION 6.3)
2. SET THE HALT/ENABLE SWITCH TO HALT
3. SET THE SR=000210(8)
4. DEPRESS LOAD ADDRESS
5. SET THE SR=000000 (WORST CASE TESTING)

# NO1

SEQ 0013

SET THE SR=004000 (QUICK PASS)

SET THE SR=002000 (TO PERFORM AN ABBREVIATED DM11-BB TEST.  
THIS ASSUMES THE AUTOSIZER WAS PREVIOUSLY  
USED TO LOAD THE DM11-BB CSR ADDRESSES.)

SET THE SR=000400 (HALT AFTER PARAMETER SET-UP)

6. SET THE HALT/ENABLE SWITCH TO ENABLE
7. DEPRESS START - THE PROGRAM TYPES THE TITLE  
AND THEN ASKS FOR DEVICE SELECTION PARAMETER.  
PROCEED AS IN (B-10) ABOVE.
9. PROGRAM WILL ASK FOR LINE SELECTION PARAMETERS.  
PROCEED AS IN (B-11) ABOVE.  
NOTE: THE DEVICE SELECTION AND LINE SELECTION  
PARAMETERS APPLY TO BOTH THE DM11 AND THE DM11-BB.  
THAT IS, IF DM #7, LINE #3 IS CHOSEN THEN DM11-BB  
#7 LINE #3 WILL ALSO BE TESTED.
10. IF SRB=1, THE PROGRAM WILL HALT AND PRINT THE  
FOLLOWING MESSAGE:

"DEPRESS CONTINUE TO START TESTING"

AT THIS POINT SET UP THE DESIRED SWITCH REG-  
ISTER OPTIONS (REFER TO PARA 2.3.1) AND DEPRESS  
"CONTINUE" TO START THE TESTING.

THE PURPOSE OF THIS HALT IS TO ALLOW THE USER TO  
DUMP THE PROGRAM AFTER SETTING UP THE CONFIGURATION  
PARAMETERS FOR HIS SYSTEM.

11. PROGRAM WILL BEGIN EXECUTION. REFER TO SECTIONS  
2.4, 3.0, AND 4.0 FOR EXECUTION TIMES ERROR AND  
STATUS REPORTS.

## 2.2 SPECIAL ENVIRONMENTS

SEQ 0014

2.2.1 ACT11 WHEN UNDER CONTROL OF THE ACT11 APT11  
 APT11 SYSTEMS THE PROGRAM MAY BE LOADED IN DUMP  
 MODE AND CAN BE RUN AS PART OF A QUICK  
 VERIFY CHAIN SINCE AN AUTOSIZER IS USED.

2.2.2 XXDP THE PROGRAM MAY BE LOADED AND RUN FROM  
 ANY "XXDP" MEDIUM PROVIDED THERE IS AT LEAST  
 12K OF CORE. IT MAY BE RUN AS PART OF  
 AN "XXDP" CHAIN.

## 2.2.3 SWITCHLESS FEATURE

IF THE DIAGNOSTIC IS RUN ON A CPU WITHOUT A SWITCH  
 REGISTER THEN A SOFTWARE SWITCH REGISTER IS USED WHICH ALLOWS  
 THE USER THE SAME SWITCH OPTIONS AS THE HARDWARE SWITCH REGISTER.  
 IF THE HARDWARE SWITCH REGISTER DOES NOT EXIST OR IF ONE DOES  
 AND IT CONTAINS ALL ONES (177777) THEN THE SOFTWARE SWITCH  
 REGISTER (LOC. 176) IS USED.

## CONTROL:

THIS PROGRAM ALSO SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH  
 REGISTER (LOC. 176) FROM THE TTY. THIS CAN BE ACCOMPLISHED BY  
 DOING THE FOLLOWING:

- 1) TYPE CONTROL G (16): THIS WILL ALLOW THE TTY TO ENTER DATA INTO  
 LOC. 176 AT SELECTED POINTS WITHIN THE PROGRAM.
- 2) THE MACHINE WILL THEN TYPE: SWR=XXXXXXNEW= (XXXXXX IS THE OCTAL CONTENTS  
 OF THE SOFTWARE SWITCH REGISTER.)
- 3) AFTER THE "NEW=" HAS BEEN TYPED THEN THE OPERATOR CAN DO ONE  
 OF THE FOLLOWING AT THE TTY:
  - A) TYPE A NUMBER TO BE LOADED INTO LOC. 176 FOLLOWED BY A (CR).  
 (ONLY OCTAL NUMBERS WILL BE ACCEPTED AND ONLY 6 NUMBERS  
 WILL BE ALLOWED)  
 IF A (CR) IS THE FIRST KEY DEPRESSED THE SOFTWARE SWITCH  
 REGISTER CONTENTS WILL NOT BE CHANGED.
  - B) IF A CONTROL U (15) IS DEPRESSED THEN THE PROGRAM WILL DO A (CR).  
 RETYPE THE DESIRED NUMBER.



## 2.3 PROGRAM OPTIONS

## 2.3.1 CONSOLE SWITCH REGISTER

THE FOLLOWING TABLE ILLUSTRATES THE FUNCTIONS OF THE CONSOLE SWITCH REGISTER DURING PROGRAM START AND DURING DM TESTING:

SWITCH REGISTER	START	TESTING
15 = 1	-----	HALT ON ERROR (AFTER TYPING ERROR MESSAGE)
14 = 1	-----	LOOP CONTINUOUSLY ON CURRENT TEST.
13 = 1	-----	INHIBIT ERROR TYPEDS.
11 = 1	-----	INHIBIT SUB-TEST ITERATIONS (QUICK PASS)
10 = 1	-----	PERFORM DMI:-BB ABBREVIATED TESTS.
9 = 1	-----	LOCK ON HARD ERRORS
8 = 1	HALTS AFTER CONFIGURATION TO PERMIT DUMPING PRE- CONFIGURED COPIES OF THE PROGRAM.	SEARCH FOR AND LOCK ON TEST SELECTED BY CONTENTS OF SR <07:00>
<07:00>		CONTAINS TEST NUMBER TO SEARCH FOR WHEN SR 08 = 1
1 = 1	TYPES DEVICE MAP GENERATED BY THE AUTOSIZER.	-----
0 = 1	ALLOWS THE USER TO INPUT DM PARAMETERS MANUALLY. (INHIBITS THE AUTOSIZER)	-----

## A. DM11 CONFIGURATION TABLES AND VARIABLES

WHEN THE AUTOSIZER OPTION IS USED, THIS PROGRAM CAN RUN NON-STANDARD DM11 CONFIGURATIONS (NON-CONTIGUOUS ADDRESSES). THE USER CAN ALSO PATCH IN HIS OWN ADDRESSES TO MATCH HIS CONFIGURATION AND THEN USE THE DEFAULT START TO RUN THE UPDATED PROGRAM. THE TABLES AND LOCATIONS TO MODIFY ARE DESCRIBED BELOW:

## 1. DMADTB: 16. WORD DEVICE ADDRESS TABLE

THE USER CAN DEPOSIT THE ADDRESSES FOR HIS NON-STANDARD CONFIGURATION IN THIS TABLE. THE POSITION OF THE ENTRY IN THE TABLE CORRESPONDS DIRECTLY TO THE DEVICE NO. (IE DM11 #00 - WORD 00, DM11 #01 - WORD 01 ETC.)

## 2. DMVCTB: 16. WORD DEVICE VECTOR ADDRESS TABLE

THE USER CAN DEPOSIT THE VECTOR ADDRESSES FOR HIS NON-STANDARD CONFIGURATION IN THIS TABLE. AGAIN THE POSITION IN THE TABLE CORRESPONDS DIRECTLY TO DEVICE NUMBER.

## 3. BRlvl: 16. WORD BR LEVEL TABLE

THIS TABLE STORES THE BR LEVELS ASSUMED BY THE INTERRUPT SERVICE ROUTINES FOR EACH DM11. THE RCVR BR LEVEL IS STORED IN THE LOW BYTE AND THE XMITTER BR LEVEL IN THE HIGH BYTE. AGAIN THE POSITION IN THE TABLE CORRESPONDS DIRECTLY TO THE DM11 DEVICE NO.

## 4. DHSSEL: DEVICE SELECTION PARAMETER

THIS WORD MUST BE SET UP TO CORRESPOND TO THE DEFAULT CONFIGURATION DEFINED BY THE TABLE SET-UPS. REFER TO SECTION 2.1.2.(B10) FOR A DESCRIPTION OF ITS ENCODING.

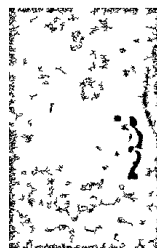
## 5. LINSSEL: LINE SELECTION PARAMETER

THIS WORD IS PROGRAM LOADED AS A 177777(9) TO SPECIFY THAT ALL LINES (16.) ARE TO BE TESTED. IT MAY BE MODIFIED AT CONFIGURATION TIME TO SPECIFY ANY COMBINATION OF LINES TO TEST. REFER TO SECTION 2.1.3.(B11) FOR A DESCRIPTION OF ITS ENCODING.

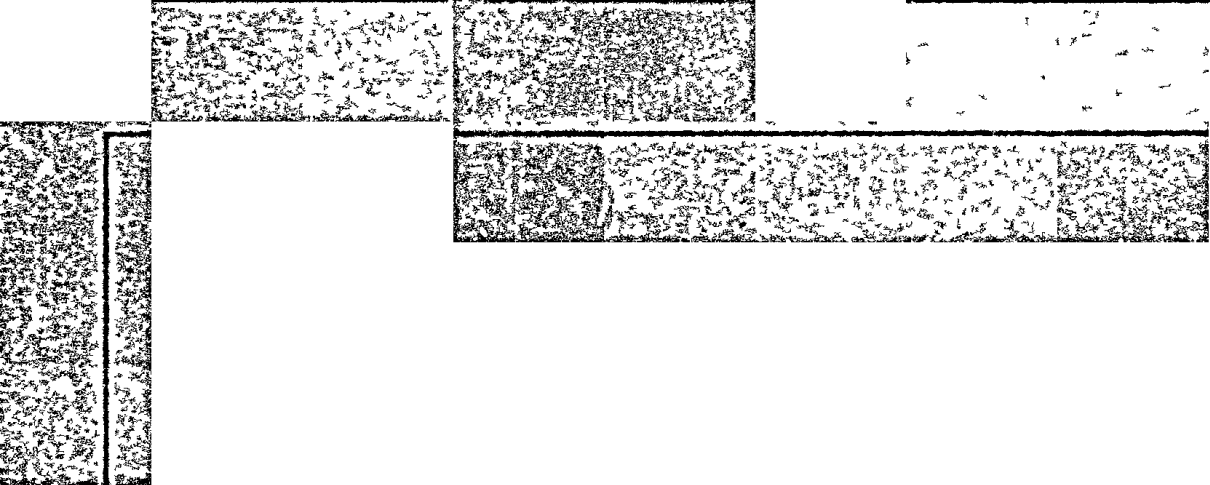
NOTE: ONCE THE PROGRAM IS STARTED IT IS TABLE DRIVEN AND USES "DHSSEL" "LINSSEL" AND THE CONTENTS OF THE THREE TABLES ABOVE TO DEFINE THE CONFIGURATION TO TEST.

NOTE: IT IS RECOMMENDED THAT WHEN NON-STANDARD CONFIGURATIONS ARE ENCOUNTERED, THE DM11-BB MODEM CONTROL DIAGNOSTIC, DZDHK, SHOULD BE RJN. RATHER THAN ALTERING THE DM11-BB TABLES IN THIS PROGRAM.

E02



Vertical text or markings along the right edge of the page, appearing as a dense column of small characters or noise.





## B. SUB-TEST ITERATION COUNT

SEQ 0018

THERE IS A LOCATION TAGGED "SMXCNT:" THAT DETERMINES HOW MANY TIMES EACH SUB-TEST IS REPEATED (SR11=0) IT IS PROGRAM LOADED TO 000010(8) BUT CAN BE CHANGED TO MODIFY THE ITERATION COUNT.

NOTE THAT MODIFYING THIS LOCATION WILL CHANGE THE PROGRAM EXECUTION TIME DEFINED IN PARA 2.4(B).

## 2.3.3 REGISTER USAGE

IN MOST OF THE TESTS THE GENERAL REGISTERS CONTAIN STANDARD INFORMATION AS SHOWN BELOW. ON PROGRAM HALTS THE REGISTERS CAN BE EXAMINED DIRECTLY TO DISPLAY THIS INFORMATION.

R0	TEST NUMBER IN OCTAL
R1	ADDRESS OF THE "SCR" REG (DEVICE ADDRESS)
R2	ADDRESS OF THE DH11 REGISTER BEING TESTED
R3	ACTUAL CONTENTS OF THE DH11 REG BEING TESTED
R4	WHAT THE CONTENTS OF THE DH11 REG BEING TESTED SHOULD HAVE BEEN
R5	GENERAL USE - REFER TO THE LISTING FOR ITS USE
R6	CONTENTS OF THE STACK POINTER
R7	CONTENTS OF THE PROGRAM COUNTER

## 2.4 EXECUTION TIMES

## A. SR11 = 0 SUB-TEST ITERATIONS

WITH ONE DH11 SELECTED FOR TESTING 16. LINES ONE COMPLETE ERROR FREE PASS TAKES APPROXIMATELY 8 MINUTES.

## B. SR11 = 1 INHIBIT ITERATIONS

WITH ONE DH11 SELECTED FOR TESTING 16. LINES ONE COMPLETE ERROR FREE PASS TAKES APPROXIMATELY ONE MINUTE

NOTE: THE ABOVE TIMES WERE DETERMINED WHEN THE PROGRAM WAS RUN ON A PDP-11/45 AND A PDP-11/40 CPU.

3.C ERROR INFORMATION  
-----3.1 ERROR REPORTING PROCEDURES  
-----3.1.1 STANDARD SYSMAC.SML ERROR REPORTING CONVENTIONS  
-----

THE PROGRAM UTILIZES THE STANDARD PDP11 DIAGNOSTICS ERROR UTILITIES. THE TEST ROUTINE CALLS THESE UTILITIES USING AN "ERROR N" INSTRUCTION (CODED EMT) WHERE "N" IS THE NUMBER OF THE ERROR MESSAGE. THE UTILITY ROUTINE USES "N" TO ACCESS THE PROPER ERROR INFORMATION VIA THE ERROR TABLE DESCRIBED IN SECTION 3.1.2 BELOW. EACH MESSAGE RESULTS IN THREE LINES OF TYPEOUT AS FOLLOWS:

LINE 1 A BRIEF DESCRIPTION OF THE FAILING FUNCTION  
 LINE 2 LABELS TO IDENTIFY THE DATA TYPED ON LINE 3  
 LINE 3 THE ACTUAL ERROR DATA (UP TO 8 OCTAL OR DECIMAL NOS.)

## EXAMPLE:

```
SYSTEM CONTROL REGISTER ERROR
  (FC)   (PS)   (SP)   TEST   DEVADR  REGADR   WAS   S/B
002720  000002  001074  000003  160020  160020  000000  000001
```

THE ERROR TABLE ITEMS SHOWN IN THE NEXT SECTION DESCRIBE ALL THE DH ERROR MESSAGES WITHIN MD-11-DZDHM AND ARE INTERPRETED AS FOLLOWS:

EM ADDRESS OF THE MESSAGE FOR LINE 1  
 DH ADDRESS OF THE DATA HEADER MESSAGE FOR LINE 2  
 DT ADDRESS OF THE TABLE OF ADDRESSES THAT POINT  
 TO THE DATA WORDS TO BE PRINTED  
 DF ADDRESS THAT POINTS TO THE DATA DESCRIPTOR  
 TABLE THAT DEFINES WHETHER AN ITEM IS OCTAL OR DECIMAL.  
 IF THIS ENTRY IS "O" ALL DATA WORDS ARE IN OCTAL.

SECTION 3.1.3 DEFINES THE MEANING OF THE MNEUMONICS USED IN THE VARIOUS DATA HEADERS.

THERE ARE ONLY TWO MESSAGES IN THE DM11-BB PORTION OF THIS PROGRAM:

ONE INFORMS THE USER THAT NO DM11-BB'S WERE FOUND BY THE AUTOSIZER AND THE PROGRAM THEN CONTINUES TESTING THE DM11'S. THE OTHER INSTRUCTS THE USER TO RUN THE DM11-BB MODEM CONTROL DIAGNOSTIC, DZDHK, DUE TO AN ERROR. THE PROGRAM THEN HALTS.

## :ERROR TABLE ITEM FOR ERROR MESSAGE 1

```

EM1      : "DH11 REGISTER REFERENCE CAUSED TIMEOUT"
DH1      : " (PC) (PS) (SP) TEST DEVADR REGADR "
DT1      : $ERRPC,$TMPD,$REG6,$REGD,$REG1,$REG2
C        : PRINT ALL OCTAL

```

## :ERROR TABLE ITEM FOR ERROR MESSAGE 2

```

EM2      : "SYSTEM CONTROL REGISTER ERROR"
DH2      : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2      : $ERRPC,$TMPD,$REG6,$REGD,$REG1,$REG2,$REG3,$REG4
0        : PRINT ALL OCTAL

```

## :ERROR TABLE ITEM FOR ERROR MESSAGE 3

```

EM3      : "DH11 MASTER CLEAR FAILED TO CLR SPECIFIED REG"
DH2      : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2      : $ERRPC,$TMPD,$REG6,$REGD,$REG1,$REG2,$REG3,$REG4
0        : PRINT ALL OCTAL

```

## :ERROR TABLE ITEM FOR ERROR MESSAGE 4

```

EM4      : "LINE PARAMETER REGISTER ERROR"
DH2      : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2      : $ERRPC,$TMPD,$REG6,$REGD,$REG1,$REG2,$REG3,$REG4
0        : PRINT ALL OCTAL

```

## :ERROR TABLE ITEM FOR ERROR MESSAGE 5

```

EM5      : "BREAK CONTROL REGISTER ERROR"
DH2      : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2      : $ERRPC,$TMPD,$REG6,$REGD,$REG1,$REG2,$REG3,$REG4
0        : PRINT ALL OCTAL

```

## :ERROR TABLE ITEM FOR ERROR MESSAGE 6

```

EM6      : "SILO STATUS REGISTER ERROR"
DH2      : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2      : $ERRPC,$TMPD,$REG6,$REGD,$REG1,$REG2,$REG3,$REG4
0        : PRINT ALL OCTAL

```

## :ERROR TABLE ITEM FOR ERROR MESSAGE 7

```

EM7      : "CURRENT ADDRESS REGISTER ERROR - LINE #XX"
DH2      : " (PC) (FS) (SP) TEST DEVADR REGADR WAS S/B "
DT2      : $ERRPC,$TMPD,$REG6,$REGD,$REG1,$REG2,$REG3,$REG4
0        : PRINT ALL OCTAL

```



;ERROR TABLE ITEM FOR ERROR MESSAGE 10

```
EM10      : "BYTE COUNTER REGISTER ERROR - LINE #XX"
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 11

```
EM11      : "UNEXPECTED DH11 RCVR INTERRUPT"
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 12

```
EM12      : "UNEXPECTED DH11 XMITTR INTERRUPT"
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 13

```
EM13      : "CHAR AVAILABLE FAILED TO GENERATE RCVR INTERRUPT"
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 14

```
EM14      : "TRANSMITTER NPR LOGIC ERROR - LINE # "
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 15

```
EM15      : "XMITTR FAILED TO INTERRUPT - LINE # "
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 16

```
EM16      : "RCVR FAILED TO INTERRUPT"
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 17

```

EM17      : "TRANSMITTER TIMING ERROR - LINE # "
DH6       : " (PC) (PS) (SP) TEST DEVADR SPEED TIMEB TIMEC"
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL

```

:ERROR TABLE ITEM FOR ERROR MESSAGE 20

```

EM20      : "RECEIVER TIMING ERROR - LINE # "
DH6       : " (PC) (PS) (SP) TEST DEVADR SPEED TIMEB TIMEC"
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL

```

:ERROR TABLE ITEM FOR ERROR MESSAGE 21

```

EM21      : "RCVR FAILED TO INTERRUPT - LINE # "
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL

```

:ERROR TABLE ITEM FOR ERROR MESSAGE 22

```

EM22      : "CHAR AVAIL FAILED TO SET ON TIME - LINE # "
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL

```

:ERROR TABLE ITEM FOR ERROR MESSAGE 23

```

EM23      : "BASIC DATA TEST ERROR - LINE # "
DH7       : " (PC) (PS) (SP) TEST DEVADR CHRLNG WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL

```

:ERROR TABLE ITEM FOR ERROR MESSAGE 24

```

EM24      : "AUTO ECHO TEST ERROR - LINE # "
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL

```

:ERROR TABLE ITEM FOR ERROR MESSAGE 25

```

EM25      : "BREAK BIT TEST ERROR - LINE # "
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL

```

;ERROR TABLE ITEM FOR ERROR MESSAGE 26

```
EM26      : "HALF-DUPLEX TEST ERROR - LINE # "
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 27

```
EM27      : "UNEXPECTED BUS ERROR TRAP"
DH3       : (PC) (PS) (SP) TEST TRPPC TRPPS
DT3       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 30

```
EM30      : "UNEXPECTED RSVD INSTR TRAP"
DH3       : (PC) (PS) (SP) TEST TRPPC TRPPS
DT3       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 31

```
EM31      : "AU. J ECHO DATA COMPARE ERROR - LINE # "
DH4       : (PC) (PS) (SP) TEST WASADR SBADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 32

```
EM32      : "AUTO ECHO TEST TIMEOUT - LINE # "
DH5       : " (PC) (LPRG) TEST"
DT4       : $ERRPC,$TMPD,$TMP2
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 33

```
EM33      : "PARITY LOGIC TEST ERROR - LINE # "
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B"
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 34

```
EM34      : "MULTI-LINE PARITY DATA TEST ERROR - LINE # - SUBTEST # "
DH4       : " (PC) (PS) (SP) TEST WASADR SBADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```



;ERROR TABLE ITEM FOR ERROR MESSAGE 35

```
EM35      : "MULTI-LINE PARITY DATA TEST TIMEOUT"
DH14     : " (PC) (LPRG) LINACT "
DT6      : "$ERRPC,$TMP0,$TMP3"
0        : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 36

```
EM36      : "CHAR AVAILABLE TIMEOUT"
DH5      : " (PC) (LPRG) TEST"
DT4      : "$ERRPC,$TMP0,$TMP2"
0        : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 37

```
EM37      : "DATA COMPARE ERROR - LINE # "
DH4      : " (PC) (PS) (SP) TEST WASADR SBADR WAS S/B "
DT2      : "$ERRPC,$TMP0,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4"
0        : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 40

```
EM40      : "BUFFER ACTIVE REG ERROR - LINE # "
DH2      : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2      : "$ERRPC,$TMP0,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4"
0        : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 41

```
EM41      : "RCVR FALSE INTERRUPT"
DH5      : " (PC) (LPRG) TEST"
DT4      : "$ERRPC,$TMP0,$TMP2"
0        : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 42

```
EM42      : "SILO OVERFLOW ERROR"
DH5      : " (PC) (LPRG) TEST"
DT4      : "$ERRPC,$TMP0,$TMP2"
0        : PRINT ALL OCTAL
```

;ERROR TABLE ITEM FOR ERROR MESSAGE 43

```
EM43      : "SILO OVERFLOW FAILED TO GENERATE RCVR INTERRUPT"
DH2      : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2      : "$ERRPC,$TMP0,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4"
0        : PRINT ALL OCTAL
```

29

## M02

SEQ 0025

:ERROR TABLE ITEM FOR ERROR MESSAGE 44

```
EM44      : "NON EX MEMORY FAILED TO GENERATE XMITTR INTERRUPT"
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 45

```
EM45      : "XMIT DONE FAILED TO GENERATE XMITTR INTERRUPT"
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 46

```
EM46      : "CURRENT ADDRESS MEMORY PATTERNS TEST ERROR - LINE # "
DH10      : " (PC) LINEWR PATTRN TEST DEVADR REGADR WAS S/B"
DTS       : $ERRPC,$TMPD,$TMP1,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 47

```
EM47      : "BYTE COUNT MEMORY PATTERNS TEST ERROR - LINE # "
DH10      : " (PC) LINEWR PATTRN TEST DEVADR REGADR WAS S/B"
DTS       : $ERRPC,$TMPD,$TMP1,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 50

```
EM50      : "TEST TIMEOUT WAITING FOR XMIT DONE - LINE # '
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B"
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4"
0         : PRINT ALL OCTAL
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 51

```
EM51      : "NPR LOGIC TEST 2 ERROR"
DH11      : " (PC) LINACT LINCHK TEST DEVADR REGADR WAS S/B"
DTS       : $ERRPC,$TMPD,$TMP1,$REG0,$REG1,$REG2,$REG3,$REG4"
0         : PRINT ALL OCTAL
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 52

```
EM52      : "BASIC DATA COMPARE ERROR"
DH2       : " (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B"
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4"
0         : PRINT ALL OCTAL
```

# N02

SEQ 0026

:ERROR TABLE ITEM FOR ERROR MESSAGE 53

```

EM50      : "TEST TIMEOUT WAITING FOR XMIT DONE - LINE # "
DH12      : " (PC)  SPEED  (SP)  TEST  DEVADR  REGADR  WAS  S/B"
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
    
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 54

```

EM22      : "CHAR AVAIL FAILED TO SET ON TIME - LINE # "
DH12      : " (PC)  SPEED  (SP)  TEST  DEVADR  REGADR  WAS  S/B"
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
    
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 55

```

EM22      : "CHAR AVAIL FAILED TO SET ON TIME - LINE # "
DH13      : " (PC)  (PS)  (SP)  TEST  DEVADR  CHRLNG  SCRWAS  SCRS/B"
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
    
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 56

```

EM56      : "OVERRUN BIT FAILED TO SET - LINE # "
DH2       : " (PC)  (PS)  (SP)  TEST  DEVADR  REGADR  WAS  S/B"
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
    
```

:ERROR TABLE ITEM FOR ERROR MESSAGE 57

```

EM57      : "STORAGE OVERFLOW BIT FAILED - LINE # "
DH2       : " (PC)  (PS)  (SP)  TEST  DEVADR  REGADR  WAS  S/B"
DT2       : $ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
0         : PRINT ALL OCTAL
    
```

## 3.1.3 DATA HEADER MNEUMONIC DEFINITIONS

SEQ 0027

ALL NUMBERS PRINTED AS ERROR DATA ARE IN OCTAL

(PC) ADDRESS OF THE ERROR CALL (ERROR PC)

(PS) CONTENTS OF THE PSW AT THE TIME OF THE ERROR

(SP) CONTENTS OF THE STACK POINTER AT THE TIME OF THE ERROR

TEST TEST NUMBER

DEVADR DEVICE ADDRESS - 1ST ADDRESS IN THE SELECTED DH11

REGADR ADDRESS OF THE DH11 REGISTER BEING TESTED

WAS WHAT THE ACTUAL DATA READ WAS (DH11 REG OR CORE LOC.)

S/B WHAT THE DATA READ SHOULD HAVE BEEN

SPEED SPEED CODE IN THE "LPR" REG AT THE TIME OF THE ERROR  
REFER TO SECTION 5.2.3 FOR SPEED CODE TABLES

TIMEB CONTENTS OF SOFTWARE COUNTER USED IN TIMING TESTS

TIMEC CONTENTS OF SOFTWARE COUNTER USED IN TIMING TESTS  
NOTE: "TIMEB" SHOULD ALWAYS BE LESS THAN "TIMEC"

CHARNG CHARACTER LENGTH CODE IN THE "LPR" AT THE TIME OF THE ERROR  
00=5 BITS, 01=6 BITS, 02=7 BITS, 03= 8 BITS

TRPFC CONTENTS OF THE PC (R7) AT THE TIME OF A BUS ERROR  
OR RSVD INSTR TRAP.

TRPPS CONTENTS OF THE PSW AT THE TIME OF A BUS ERROR  
OR RSVD INSTR TRAP.

(LPRG) CONTENTS OF THE "LPR" REGISTER AT THE TIME OF THE ERROR

LINACT FLAGS USED BY MULTI-LINE TESTS TO INDICATE LINES STILL ACTIVE

WASADR CORE MEMORY ADDRESS OF THE "WAS" DATA (ACTUAL DATA READ)

SBADR CORE MEMORY ADDRESS OF THE S/B DATA (GOOD DATA)

SCRWAS CONTENTS OF THE "SCR" REGISTER

SCR/S/B WHAT THE CONTENTS OF THE "SCR" REGISTER SHOULD HAVE BEEN

LINCHK LINE NO. BEING CHECKED DURING "CAR" AND "BCR" MEMORY TESTS

LINWR LINE NO. BEING WRITTEN INTO DURING "CAR" AND "BCR" MEMORY TESTS

PATRN TEST PATTERN BEING WRITTEN INTO EITHER THE "CAR" OR "BCR" MEMORIES

## 3.2 POWER FAIL PRINTOUT

SEP 0028

IF A POWER FAILURE OCCURS WHILE THE PROGRAM IS RUNNING,  
THE FOLLOWING PRINTOUT OCCURS:

"POWER"

AFTER THE PRINTOUT THE PROGRAM WILL BE RESTARTED AUTOMATICALLY  
FROM THE BEGINNING. NO ATTEMPT IS MADE TO CONTINUE THE PROGRAM  
FROM THE POINT OF THE POWER FAIL INTERRUPTION.

## 3.3 ERROR HALTS

## A. SYSMAC ERROR SERVICE ROUTINE HALT

WHEN SR15=1 A "HALT" IS EXECUTED IN THE SYSMAC ERROR  
UTILITY AFTER THE ERROR TYPEOUT. TO RESUME TESTING  
FROM THE POINT OF THE "HALT" SIMPLY DEPRESS CONTINUE.

## B. POWER FAIL HALT

WHEN A POWER DOWN IS DETECTED, THE PROGRAM HALTS IN  
THE POWER FAIL UTILITY ROUTINE. IF FOR SOME REASON  
THE AUTO-START FEATURE FAILS TO RESTART THE PROGRAM,  
THE PROGRAM WILL "LOCK" ON THIS HALT IF CONTINUE IS  
DEPRESSED. IN THIS CASE THE PROGRAM MUST BE RESTARTED.

## C. TRAP CATCHER HALTS

ALL INACTIVE VECTORS ARE SET UP WITH THE STANDARD  
PDF11 TRAP CATCHER AS DESCRIBED BELOW:

VN / VN+2  
VN+2 / HALT

IF A TRAP OR INTERRUPT OCCURS TO A VECTOR THAT HAS  
NOT BEEN SET UP BY THE TEST ROUTINE, A "HALT" OCCURS  
IN THE VECTOR AREA. THE ADDRESS DISPLAY INDICATES  
WHICH VECTOR THE PROGRAM TRAPPED TO AND THE LAST ENTRY  
PUSHED ON TO THE STACK INDICATES WHERE THE PROGRAM WAS  
WHEN THE TRAP OR INTERRUPT OCCURRED.



4.0 PERFORMANCE AND PROGRESS REPORTS4.1 PERFORMANCE REPORTS

(NONE PROVIDED)

4.2 PROGRESS REPORTS

- A. WHEN THE PROGRAM IS STARTED OR RESTARTED IT PRINTS THE TITLE MESSAGE:

"MAINDEC-11-DZDHM-"X" DH11 DIAGNOSTIC"

WHERE "X" IS THE REVISION LEVEL LETTER DESIGNATION.

- B. WHEN THE PROGRAM BEGINS TESTING ON EACH DH11 IT TYPES THE FOLLOWING MESSAGE:

"TESTING DH11 #NN"

WHERE "NN" IS THE DEVICE NO. IN OCTAL (00-17)

- C. WHEN THE PROGRAM COMPLETES A PASS (TESTED ALL SELECTED LINES ON ALL SELECTED DH11'S) IT TYPES:

"END PASS       #XXXXX"

WHERE "X" IS THE PASS COUNT IN DECIMAL.

- D. WHEN THE PROGRAM IS IN THE CONFIGURATION DIALOGUE (START AT 200, OR 210) AND SR8 AND SRC=1, THE PROGRAM WILL HALT AFTER ACCEPTING THE INPUT PARAMETERS AND TYPE THE FOLLOWING MESSAGE:

"DEPRESS CONTINUE TO START TESTING"

THE PURPOSE OF THIS HALT IS TO ALLOW THE USER TO DUMP THE UPDATED PROGRAM ON THE LOAD MEDIUM FOR NON-STANDARD CONFIGURATIONS. (SEE SECTION 2.2.2 AND 2.3.2)

5.0 DH11 DEVICE INFORMATION

SEQ 0030

5.1 ADDRESS AND VECTOR ASSIGNMENTS

THE DH11 USES FLOATING ADDRESSES AND IS LOCATED AFTER DJ11'S IN THE FLOATING ADDRESS SPACE THAT BEGINS AT LOCATION 760010. BECAUSE THE DH11 HAS EIGHT REGISTERS, IT MUST BE ASSIGNED AN ADDRESS THAT IS A MULTIPLE OF 20 (OCTAL). ALL DH11'S IN A SYSTEM SHOULD HAVE CONSECUTIVE ADDRESSES.

EXAMPLE #1: A SYSTEM WITH NO DJ11'S BUT TWO DH11'S.

760 010 CANNOT USE FOR DH11'S BECAUSE NOT MULTIPLE OF 20.  
 760 020 FIRST DH11  
 760 040 SECOND DH11  
 760 060 DH11 GAP (INDICATES THAT THERE ARE NO MORE DH11'S).

EXAMPLE #2: A SYSTEM WITH ONE DJ11, TWO DH11'S:

760 010 FIRST DJ11  
 760 020 DJ11 GAP (INDICATES THAT THERE ARE NO MORE DJ11'S).  
 760 030 CANNOT USE FOR DH11'S BECAUSE NOT MULTIPLE OF 20.  
 760 040 FIRST DH11  
 760 060 SECOND DH11  
 760 100 DH11 GAP (INDICATES THAT THERE ARE NO MORE DH11'S).

THE DH11 VECTORS (2) FOLLOW THOSE OF THE DJ11 IN THE FLOATING VECTOR SPACE THAT STARTS AT ADDRESS 300. THE VECTORS STARTING AT 300 ARE USED IN THE FOLLOWING ORDER: DC11; KL11/DL11-A, B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 READERS; PA611 PUNCHES; DT11; DX11; DL11-C, D, E; DH11.

THE RECEIVER VECTOR IS THE LOWER NUMBERED VECTOR. THE PRIORITY OF THE RECEIVER AND TRANSMITTER INTERRUPTS ARE INDIVIDUALLY SELECTABLE BY MEANS OF TWO STANDARD PDP11 PRIORITY JUMPER PLUGS. BR LEVEL 5 IS STANDARD.

5.2 REGISTER DEFINITION

THE FOLLOWING SECTION DESCRIBES THE BIT ASSIGNMENTS WITHIN EACH REGISTER: BITS MARKED UNUSED AND WRITE ONLY ARE ALWAYS READ AS ZERO. ATTEMPTING TO WRITE INTO UNUSED OR READ ONLY BITS HAS NO EFFECT ON THOSE BITS. INIT REFERS TO THE INITIALIZE SIGNAL GENERATED BY THE PROCESSOR (E.G. UPON EXECUTION OF A RESET INSTRUCTION). TRANSMIT AND RECEIVE ARE WITH RESPECT TO THE DH11.

# F03

## 5.2.1 THE SYSTEM CONTROL REGISTER - ADDRESS X00

SEQ 0031

THE SYSTEM CONTROL REGISTER IS A BYTE-ADDRESSABLE REGISTER. THE BIT ASSIGNMENT IS AS FOLLOWS:

BITS      DESCRIPTION  
-----

00-03    LINE SELECTION

EACH OF THE 16 LINES SERVED BY THE DH11 HAS ITS OWN STORAGE FOR LINE PARAMETER INFORMATION, CURRENT ADDRESS, AND BYTE COUNT. THESE STORAGE LOCATIONS ARE LOADED BY THE PROGRAM VIA THE LINE PARAMETER REGISTER, CURRENT ADDRESS REGISTER, AND BYTE COUNT REGISTER, BUT THE HARDWARE MUST FIRST BE TOLD WHICH LINE IS TO HAVE ITS LINE PARAMETERS, CURRENT ADDRESS, OR BYTE COUNT CHANGED. THIS ROUTING IS ACCOMPLISHED BY SETTING THE LINE SELECTION BITS TO THE BINARY ADDRESS (0000-1111) OF THE DESIRED LINE. THESE BITS ARE READ/WRITE.

04, 05    MEMORY EXTENSION

THE INFORMATION STORED IN THESE BITS BECOMES BITS 16 AND 17 RESPECTIVELY OF ANY CURRENT ADDRESS LOADED BY THE PROGRAM INTO THE CURRENT ADDRESS REGISTER. THESE BITS ARE READ/WRITE BUT, WHEN READ, REPRESENT ONLY THE STATUS OF BITS 4 AND 5 OF THE SYSTEM CONTROL REGISTER, NOT THE STATUS OF ADDRESS BITS 16 AND 17 OF THE SELECTED LINE. SEE THE SILO STATUS REGISTER FOR FURTHER INFORMATION. THIS ARRANGEMENT PERMITS INTERRUPT SERVICE ROUTINES TO SAVE THE CONTENTS OF THE SYSTEM CONTROL REGISTER ACCURATELY.

06        RECEIVER INTERRUPT ENABLE

THIS BIT, WHEN SET, ENABLES RECEIVER INTERRUPTS (BIT 7)

07        RECEIVER INTERRUPT

THIS BIT, WHEN SET, INDICATES THAT THE NUMBER OF CHARACTERS STORED IN THE SILO EXCEEDS THE "ALARM LEVEL" SPECIFIED BY THE LOW BYTE OF THE SILO STATUS REGISTER. THIS BIT IS READ ONLY, EXCEPT IN MAINTENANCE MODE, WHERE IT IS READ/WRITE. SETTING OF THIS BIT WILL GENERATE AN INTERRUPT REQUEST IF BIT 6 (ABOVE) IS ALSO SET.

08        CLEAR NON-EXISTENT MEMORY INTERRUPT

THIS BIT, WHEN SET, CLEARS THE NON-EXISTENT MEMORY INTERRUPT FLIP-FLOP (BIT 10) AND CLEARS ITSELF. THIS BIT IS READ/WRITE.

09        MAINTENANCE

THIS BIT, WHEN SET, PLACES THE DH11 IN MAINTENANCE MODE.

10        NON-EXISTENT MEMORY

THIS BIT IS SET WHENEVER THE NPR HARDWARE PLACES THE ADDRESSES OF A MEMORY LOCATION ON THE UNIBUS AND NO SLAVE SYNC IS RECEIVED IN 20 S. THIS INDICATES THAT THE ADDRESSED LOCATION OR DEVICE DOES NOT EXIST. THIS BIT CAUSES AN INTERRUPT REQUEST IF SET WHILE TRANSMITTER AND NON-EXISTENT MEMORY INTERRUPT ENABLE IS SET. THIS BIT IS READ ONLY, EXCEPT IN MAINTENANCE MODE, WHERE IT IS READ/WRITE.

11        MASTER CLEAR

THIS BIT, WHEN SET, GENERATES "INITIALIZE" WITHIN THE DH11, CLEARING THE SILO, THE UARTS, AND THE REGISTERS. THE EXACT BITS CLEARED ARE DISCUSSED IN THE SECTION ON INITIALIZATION. READ/WRITE.

12        STORAGE INTERRUPT ENABLE

THIS BIT, WHEN SET, PERMITS THE SETTING OF BIT 14 TO GENERATE AN INTERRUPT REQUEST. THIS BIT IS READ/WRITE.

# G03

13 TRANSMITTER AND NON-EX-MEM INTERRUPT ENABLE

SEQ 0032

THIS BIT, WHEN SET, PERMITS THE SETTING OF BIT 10 OR 15 TO GENERATE AN INTERRUPT REQUEST. THIS BIT IS READ/WRITE.

14 STORAGE INTERRUPT

THIS BIT IS SET WHEN THE RECEIVER SCANNER FINDS A RECEIVER HOLDING BUFFER WITH A CHARACTER IN IT, TRIES TO STORE THAT CHARACTER IN THE SILO, AND CANNOT DO SO BECAUSE OF A LACK OF SPACE. WHEN SET THIS BIT WILL CAUSE AN INTERRUPT REQUEST IF BIT 12 IS SET. THIS BIT IS READ ONLY, EXCEPT IN MAINTENANCE MODE, WHERE IT IS READ/WRITE.

15 TRANSMITTER INTERRUPT

THIS BIT IS SET WHEN THE DH11 CONCLUDES AN NPR CYCLE THAT INCREMENTED A BYTE COUNT TO ZERO, INDICATING THE LAST CHARACTER IN A MESSAGE BUFFER WAS LOADED INTO A UART TRANSMITTER HOLDING REGISTER. THIS BIT WILL CAUSE AN INTERRUPT REQUEST IF BIT 13 IS SET. THIS BIT IS READ/WRITE. (IT IS SET DURING AN NPR CYCLE.)

BITS    DESCRIPTION

00-07    NEXT RECEIVED CHARACTER

THESE BITS CONTAIN THE NEXT RECEIVED CHARACTER, RIGHT JUSTIFIED. THE LEAST SIGNIFICANT BIT IS BIT 00.

08-11    LINE NUMBER

THESE BITS INDICATE THE LINE NUMBER ON WHICH THE NEXT RECEIVED CHARACTER WAS RECEIVED. BIT 8 IS THE LEAST SIGNIFICANT BIT.

12        PARITY ERROR

THIS BIT IS SET IF THE PARITY OF THE RECEIVED CHARACTER DOES NOT AGREE WITH THAT DESIGNATED FOR THAT LINE.

13        FRAMING ERROR

THIS BIT IS SET IF THE RECEIVER SAMPLES A LINE FOR THE FIRST STOP BIT, AND FINDS THE LINE IN A SPACING CONDITION (LOGICAL 0). THIS CONDITION USUALLY INDICATES THE RECEPTION OF A BREAK.

14        DATA OVERRUN

THIS BIT IS SET WHEN THE RECEIVED CHARACTER WAS PRECEDED BY A CHARACTER THAT WAS LOST DUE TO THE INABILITY OF THE RECEIVER SCANNER TO SERVICE THE UART RECEIVER HOLDING BUFFER. REFER TO THE SECTION ON PROGRAMMING FOR FURTHER DETAILS ON DOUBLE-BUFFERED RECEPTION.

15        VALID DATA PRESENT

THIS BIT INDICATES THAT THE DATA PRESENTED IN BITS 14-00 IS VALID. IT PERMITS A CHARACTER HANDLING PROGRAM TO TAKE CHARACTERS FROM THE SILO UNTIL IT IS EMPTY. THIS IS DONE BY READING THIS REGISTER AND CHECKING BIT 15 UNTIL A WORD IS OBTAINED FOR WHICH BIT 15 IS A ZERO. THE ENTIRE NEXT RECEIVED CHARACTER REGISTER IS READ-ONLY AND IS ADDRESSABLE ONLY ON A WORD BASIS.



5.2.3 LINE PARAMETER REGISTER ADDRESS X04

SEQ 0034

THIS REGISTER SHOULD BE LOADED ONLY AFTER THE LINE SELECTION BITS OF THE SYSTEM CONTROL REGISTER HAVE BEEN SET TO SELECT THE LINE TO WHICH THESE PARAMETERS APPLY. THIS REGISTER IS WRITE ONLY.

BITS    DESCRIPTION

00-01 CHARACTER LENGTH

THESE BITS SHOULD BE SET AS SHOWN TO RECEIVE AND TRANSMIT CHARACTERS OF THE LENGTH (EXCLUDING PARITY) SHOWN:

BIT 01 00

0	0	5 BIT
0	1	6 BIT
1	0	7 BIT
1	1	8 BIT

02 TWO STOP BITS

THIS BIT, WHEN SET, CONDITIONS A LINE TRANSMITTING WITH 6, 7, OR 8-BIT CODE TO TRANSMIT CHARACTERS HAVING TWO STOP MARKS. IF THE LINE IS TRANSMITTING 5-BIT CODE, ASSERTION OF THIS BIT CAUSES THE CHARACTERS TO BE TRANSMITTED WITH 1.5 STOP MARKS. IF THIS BIT IS NOT ASSERTED, 1 STOP MARK IS SENT.

03 NOT USED

04 PARITY ENABLED

IF THIS BIT IS SET, CHARACTERS TRANSMITTED ON THIS LINE WILL HAVE AN APPROPRIATE PARITY BIT AFFIXED, AND CHARACTERS RECEIVED ON THIS LINE WILL HAVE THEIR PARITY CHECKED.

05 ODD PARITY

IF THIS BIT AND BIT 4 ARE SET, CHARACTERS OF ODD PARITY WILL BE GENERATED ON THIS LINE AND INCOMING CHARACTERS WILL BE EXPECTED TO HAVE ODD PARITY. IF THIS BIT IS NOT SET, BUT BIT 4 IS SET, CHARACTERS OF EVEN PARITY WILL BE GENERATED ON THIS LINE AND INCOMING CHARACTERS WILL BE EXPECTED TO HAVE EVEN PARITY. IF BIT 4 IS NOT SET, THE SETTING OF THIS BIT IS IMMATERIAL.

06-09 RECEIVER SPEED

THE STATE OF THESE BITS DETERMINES THE OPERATING SPEED FOR THIS LINE'S RECEIVER. THE SPEED TABLE BELOW IS APPLICABLE.

10-13 TRANSMITTER SPEED

THE STATE OF THESE BITS DETERMINES THE OPERATING SPEED FOR THIS LINE'S TRANSMITTER. THE SPEED TABLE ON THE NEXT PAGE IS APPLICABLE.



SPEED TABLE FOR RECEIVER AND TRANSMITTER SPEEDS:

	BIT				
TRANSMITTER	13	12	11	10	
RECEIVER	9	8	7	6	
	--	--	--	--	
	0	0	0	0	ZERO BAUD
	0	0	0	1	50 BAUDS
	0	0	1	0	75 BAUDS
	0	0	1	1	110 BAUDS
	0	1	0	0	134.5 BAUDS
	0	1	0	1	150 BAUDS
	0	1	1	0	200 BAUDS
	0	1	1	1	300 BAUDS
	1	0	0	0	600 BAUDS
	1	0	0	1	1200 BAUDS
	1	0	1	0	1800 BAUDS
	1	0	1	1	2400 BAUDS
	1	1	0	0	4800 BAUDS
	1	1	0	1	9600 BAUDS
				0	EXTERNAL INPUT A
				1	EXTERNAL INPUT B

14 HALF DUPLEX/FULL DUPLEX

IF THIS BIT IS SET, THIS LINE WILL OPERATE IN HALF-DUPLEX MODE. IF NOT SET, THIS LINE WILL OPERATE IN FULL-DUPLEX MODE.

IN THIS APPLICATION HALF-DUPLEX MEANS THAT THE DHI1 RECEIVER IS BLINDED DURING TRANSMISSION OF A CHARACTER.

15 AUTO-ECHO ENABLE

WHEN THIS BIT IS SET, CHARACTERS RECEIVED ON THIS LINE WILL BE HARDWARE ECHOED. SEE THE DISCUSSION OF AUTO-ECHO FOR FURTHER DETAILS.

5.2.4 CURRENT ADDRESS REGISTER ADDRESS X06  
-----

SEQ 0036

THIS REGISTER SHOULD BE LOADED ONLY AFTER THE SYSTEM CONTROL REGISTER (SCR) HAS HAD THE APPROPRIATE BITS SET TO SELECT THE DESIRED LINE NUMBER. WHEN THIS REGISTER IS LOADED, ADDRESS BITS 00-15 ARE TRANSFERRED INTO SEMICONDUCTOR MEMORIES IN THE DH11 FROM BITS 00-15 OF THIS REGISTER. ADDRESS BITS 16-17 ARE TRANSFERRED INTO SEMICONDUCTOR MEMORIES IN THE DH11 FROM BITS 4-5 OF THE SYSTEM CONTROL REGISTER.

INTERRUPTS MUST BE INHIBITED OR THE SCR SAVED BETWEEN THE SETTING OF THE SCR BITS 0-3 AND THE READ OR WRITE OF THE CURRENT ADDRESS REGISTER.

WHEN THIS REGISTER IS READ, IT WILL INDICATE THE CURRENT ADDRESS OF THE LINE SELECTED BY THE SYSTEM CONTROL REGISTER. BITS 16 AND 17 WILL APPEAR IN THE SILO STATUS REGISTER, BITS 6 AND 7.

5.2.5 BYTE COUNT REGISTER ADDRESS X10  
-----

IN THE SAME FASHION AS THE LINE PARAMETER AND CURRENT ADDRESS REGISTERS, THIS REGISTER SHOULD NOT BE LOADED OR READ WITHOUT FIRST SELECTING A LINE NUMBER BY MEANS OF THE LOWER-ORDER FOUR BITS OF THE SYSTEM CONTROL REGISTER. THIS REGISTER SHOULD BE LOADED WITH THE TWO'S COMPLEMENT OF THE NUMBER OF CHARACTERS (BYTES) TO BE TRANSMITTED ON THAT LINE. THE BYTE COUNT REGISTER IS READ/WRITE.

INTERRUPTS MUST BE INHIBITED OR THE SCR SAVED BETWEEN THE SETTING OF THE SCR BITS 0-3 AND THE READ OR WRITE OF THE BYTE COUNT REGISTER

5.2.6 BUFFER ACTIVE REGISTER (BAR) ADDRESS X12  
-----

THIS REGISTER CONTAINS ONE BIT FOR EACH LINE. THE BITS ARE INDIVIDUALLY SET USING BIS INSTRUCTIONS. SETTING A BIT INITIATES TRANSMISSION ON THE ASSOCIATED LINE. THE BIT IS CLEARED BY THE HARDWARE WHEN THE LAST CHARACTER TO BE TRANSMITTED IS LOADED INTO THE TRANSMITTER DATA HOLDING REGISTER OF THE UART FOR THAT LINE. IT SHOULD BE NOTED THAT WHILE THE CLEARING OF A BAR DOES INDICATE THAT A MESSAGE MAY BE SENT, IT DOES NOT INDICATE THAT THE LAST CHARACTERS FROM THE PRECEDING MESSAGE HAVE BEEN COMPLETELY SENT. SPECIFICALLY, TWO MORE CHARACTERS WILL BE SENT AFTER THE BAR BIT CLEARS. THESE ARE THE LAST TWO CHARACTERS OF THE MESSAGE; ONE OF THEM WAS JUST STARTING WHEN THE BAR WAS CLEARED AND ONE WAS THAT FINAL CHARACTER THAT WAS LOADED INTO THE HOLDING REGISTER, THUS CLEARING THE BAR BIT. THIS EFFECT IS A NORMAL CONSEQUENCE OF DOUBLE-BUFFERED TRANSMISSION AND IS MENTIONED HERE FOR THE BENEFIT OF PROGRAMMERS WHO WANT TO WRITE PROGRAMS THAT CONTROL SUCH MODEM LEADS ARE REQUEST TO SEND. REQUEST TO SEND (RTS) SHOULD NOT BE DROPPED UNTIL AT LEAST TWO CHARACTER TIMES AFTER THE BAR BIT FOR A GIVEN LINE CLEARS.

THIS TIMING MAY BE EFFECTED BY SENDING TWO EXTRA (NULL) CHARACTERS IN A MESSAGE AND DROPPING RTS WHEN BAR CLEARS.

CLEARING A BAR BIT SHOULD NOT BE USED TO ABORT TRANSMISSION ON A LINE. RATHER, THE BYTE COUNT FOR THAT LINE SHOULD BE SET TO ZERO. THE BUFFER ACTIVE REGISTER BITS ARE READ/WRITE.

5.2.7 BREAK CONTROL REGISTER ADDRESS X14  
-----

THIS REGISTER CONTAINS ONE BIT FOR EACH LINE. SETTING A BIT IN THIS REGISTER WILL IMMEDIATELY GENERATE A BREAK CONDITION ON THE LINE CORRESPONDING TO THAT BIT NUMBER. CLEARING THE BIT WILL TERMINATE THE BREAK CONDITION. THE BREAK CONDITION MAY BE TIMED BY SENDING CHARACTERS DURING THE BREAK INTERVAL, SINCE THESE CHARACTERS WILL NEVER ACTUALLY REACH THE LINE. FURTHER COMMENTS CONCERNING THE TRANSMISSION OF BREAK SIGNALS MAY BE FOUND IN THE BREAK SIGNALS SECTION.

## 5.2.8 SILO STATUS REGISTER ADDRESS X16

SEQ 0037

THIS REGISTER IS ACTUALLY TWO BYTE-SIZED REGISTERS. THE BIT ASSIGNMENTS ARE:

BIT      DESCRIPTION  
---      -----

00-05    SILO ALARM LEVEL

THE PROGRAM MAY LOAD AN INTEGRAL POWER OF 2 BETWEEN 0 AND 63 INTO THIS LOCATION (E.G., 0, 1, 2, 4, 8, 16, OR 32). WHEN THE NUMBER OF CHARACTERS STORED IN THE SILO EXCEEDS THAT NUMBER, AN INTERRUPT REQUEST (SYSTEM CONTROL REGISTER BIT 7) IS GENERATED, IF SYSTEM CONTROL REGISTER BIT 6 IS SET. THESE BITS ARE READ/WRITE.

06-07    READ EXTENDED MEMORY

THESE BITS ARE READ ONLY AND CONTAIN THE A16 AND A17 BITS OF THE CURRENT LINE ADDRESS WHICH THE LINE SELECTION BITS OF THE SYSTEM CONTROL REGISTER ARE POINTING.

08-13    SILO FILL LEVEL

THESE BITS ARE AN UP-DOWN COUNTER THAT INDICATES THE ACTUAL NUMBER OF CHARACTERS IN THE SILO. IT SHOULD BE NOTED THAT THERE ARE SIX BITS, HENCE NUMBERS BETWEEN 0 AND 63 CAN BE REPRESENTED. A FULL SILO HAS 64 ENTRIES AND THE FILL LEVEL APPEARS AS 00000, BUT ONE MAY EASILY TELL THE DIFFERENCE BETWEEN AN EMPTY SILO (00000) AND A FULL SILO (00000) BY CHECKING THE STORAGE OVERFLOW BIT (BIT 14 OF SYSTEM CONTROL). THESE BITS ARE READ ONLY.

THIS SECTION LISTS ALL OF THE PRINTS FOR ALL OF THE MODULES IN THE DH11 SUBSYSTEM. IT BRIEFLY SUMMARIZES THE FUNCTIONAL LOGIC DESCRIBED ON EACH PRINT. THIS INFORMATION MAY PROVE USEFUL FOR A MODULE OR CHIP REPLACEMENT GUIDE WHEN THE FUNCTIONAL AREA OF LOGIC THAT IS FAULTY IS KNOWN TO BE INTERMITTENTLY FAILING.

M7277 CURRENT ADDR REG MEMORY AND ADDR SELECT  
\*\*\*\*\*

- SH3 CONTROL STROBE MUX FOR THE "LPR" REGISTER  
TRANSMITTER DATA MUX WITH AUTO-ECHO CONTROL LOGIC SELECTION  
MSYN / SSYN TIMING CHAIN  
DH11 MASTER CLEAR LOGIC
- SH4: UNIBUS ADDRESS SELECTION LOGIC WITH JUMPERS  
TRANSMITTER SCAN COUNTER WITH XMITTER STATUS MULTIPLEXOR (BAR N \* TBMT N)
- SH5: BYTE COUNT AND CURRENT ADDRESS MEMORY WRITE TIMING LOGIC  
CURRENT ADDRESS MEMORY LOGIC BITS<17:08>  
UNIBUS ADDRESS DRIVERS BITS <17:08>
- SH6: BYTE COUNT AND CURRENT ADDRESS MEMORY ADDRESS SELECT MULTIPLEXOR  
CURRENT ADDRESS MEMORY LOGIC FOR BITS <07:00>  
UNIBUS ADDRESS DRIVERS FOR BITS <07:00>  
TRANSMITTER EVEN/ODD BYTE DATA MULTIPLEXOR

M7279 FIFO BUFFER  
\*\*\*\*\*

- SH1: INPUT DATA MULTIPLEXOR FOR SILO MEMORY
- SH2: SILO MEMORY CHIPS (FOUR 64 X 4 CHIPS)  
SILO MEMORY READ/WRITE TIMING LOGIC  
"SSR" REGISTER BITS <13:08>  
SILO ALARM LEVEL COMPARATOR  
RECEIVED "DATA READY" STATUS FLAG



M7288 LINE PARAMETER CONTROL  
 \*\*\*\*\*

SEQ 0039

- SH3: CLOCK TIMING SIGNAL BUFFERS
- SH4: TRANSMITTER CLOCK SELECTION MULTIPLEXORS LINES<03:00>
- SH5: RECEIVER CLOCK SELECTION MULTIPLEXORS LINES <03:00>  
 AUTO ECHO AND HALF DUPLEX CONTROL LINES<03:00>
- SH6: TRANSMITTER CLOCK SELECTION MULTIPLEXORS LINES<07:04>
- SH7: RECEIVER CLOCK SELECTION MULTIPLEXORS LINES <07:04>  
 AUTO ECHO AND HALF DUPLEX CONTROL LINES <07:04>
- SH8: TRANSMITTER CLOCK SELECTION MULTIPLEXORS LINES<11:08>
- SH9: RECEIVER CLOCK SELECTION MULTIPLEXORS LINES <11:08>  
 AUTO ECHO AND HALF DUPLEX CONTROL LINES <11:08>
- SH10: TRANSMITTER CLOCK SELECTION MULTIPLEXORS LINES<15:12>
- SH11: RECEIVER CLOCK SELECTION MULTIPLEXORS LINES <15:12>  
 AUTO ECHO AND HALF DUPLEX CONTROL LINES <15:12>

M7280 #1 MULTIPLE UART CARD FOR LINES <0-7>  
 \*\*\*\*\*

- SH2: UART CHIPS BIT<1:0>  
 RECEIVER SCAN MULTIPLEXORS (CLR R DONE, STB RD, MASTER DA, AND MASTER OR)
- SH3: UART CHIPS BIT<3:2>
- SH4: UART CHIPS BIT<5:4>  
 RECEIVER SCAN MULTIPLEEXORS (MASTER FE AND MASTER PE)
- SH5: UART CHIPS BIT<7:6>  
 TRANSMITTER SCAN MULTIPLEXOR  
 -12 VOLT DC REGULATOR

M7280 #2 MULTIPLE UART CARD FOR LINES 8-15  
\*\*\*\*\*

SEQ 0040

- SH2: UART CHIPS BIT<9:8>  
RECEIVER SCAN MULTIPLEXORS (CLR R DONE, STB RD, MASTER DA, AND MASTER OR)
- SH3: UART CHIPS BIT<11:10>
- SH4: UART CHIPS BIT<13:12>  
RECEIVER SCAN MULTIPLEXORS (MASTER FE AND MASTER PE)
- SH5: UART CHIPS BIT<15:14>  
TRANSMITTER SCAN MULTIPLEXOR  
-12 VOLT DC REGULATOR

M7289 SYSTEM CONTROL AND RCVR SCAN  
\*\*\*\*\*

- SH3: TRANSMITTER AND RECEIVER SCAN LOGIC
- SH4: TRANSMITTER AND RECEIVER SCAN TIMING
- SH5: HALF-DUPLEX CONTROL LOGIC  
UART DATA MULTIPLEXORS
- SH6: SYSTEM CONTROL REGISTER

M4540 DC11 - CH11 CLOCK  
\*\*\*\*\*

- SH1: CRYSTAL OSCILLATOR AND FREQUENCY DIVIDERS

M796 UNIBUS MASTER CONTROL  
\*\*\*\*\*

- SH1: NPR CONTROL LOGIC

M7281 #1 INTERRUPT CONTROL  
\*\*\*\*\*

- "A" SECTION: RECEIVER INTERRUPT CONTROL LOGIC
- "B" SECTION: TRANSMITTER INTERRUPT CONTROL LOGIC

M7281 #2 NPR CONTROL  
\*\*\*\*\*

- "A" SECTION: USED TO GAIN CONTROL OF THE BUS FOR NPR XFERS
- "B" SECTION: (NOT USED)

M727S REGISTER AND BYTE CONTROL  
\*\*\*\*\*

SH3: CLEAR "BAR" REG MULTIPLEXOR  
BYTE COUNT MEMORY AND CONTROL - BITS<15:08>  
UNIBUS RECEIVERS BIT<15:08>

SH4: BYTE COUNT MEMORY AND CONTROL LOGIC BIT<07:00>  
UNIBUS DATA RECEIVERS BIT<07:00>

SH5 - SH8: "BAR", "BCR", "LPR", AND "SSR" REGISTERS PLUS THE  
DATA OUTPUT MUX AND UNIBUS DRIVERS FOR DATA LINES.

SH5: BIT<15:12> SH7: BIT<07:04>  
SH6: BIT<11:09> SH8: BIT<03:00>

*Chis*

5.4 DH11 MODULE ALLOCATION CHART

SEQ 0042

VIEW FROM WIRING SIDE

SLOT

	1	2	3	4	5	6	7	8	9
	M920	M7821	M7277	M7287	M7289	M7821	M7360	M7288	M920
	CABLE								CABLE
ROW A	UNIBUS CONNECTOR (NOTE #3)	NPR CNTL	REG 8 BYTE CNT	CURRENT ADDRS 8 ADDRS	SYSTEM CNTL 8 RCV SCAN	INTR CNTL	PRIORITY SELECTOR (NOTE #9)	LINE PARAMETER CNTL	UNIBUS CONNECTOR (NOTES #1, #2)
		M796				M405	M971		
		UNIBUS MASTER CNTL				EXTERNAL B CLOCK (NOTE #5)	DATA CABLE (NOTES #6, #9)		
B	M7247	M7247				M7280	M7280		M7279
	* CONTROL MUX LINES 8-15 (NOTE #7)	* CONTROL MUX LINES 0-7 (NOTE #8)				MULTIPLE UART LINES 0-7	MULTIPLE UART LINES 8-15		FIFO BUFFER
C									
	M105	M7246							M405
	* ADDRESS SELECTOR (NOTE #7)	* CONTROL SCAN (NOTES #4, #8)							EXTERNAL A CLOCK (NOTE #5)
E	M7821								M4540
F	* INTR CNTL (NOTE #7)								DH11 DC11 CLOCK

FIGURE 2-4 DH11 MODULE UTILIZATION DIAGRAM  
PAGE 2

## NOTES:

1. IF END OF BUS. REPLACE M920 WITH M930.
2. IF LAST UNIT IN BASIC BOX, REPLACE M920 WITH BC11A CABLE WHEN EXPANDING TO PERIPHERAL BOX.
3. IF FIRST UNIT IN EXPANDER BOX, REPLACE M920 WITH BC11A CABLE.
4. EQ2 MUST BE G727 GRANT CONTINUITY IF MODEM CONTROL MODULE SET IS NOT INSTALLED. \* DENOTES DM11-BB MODEM CONTROL OPTION, WITH DH11-AA OR AC.
5. MODULE SLOTS PROVIDE FOR ADDITIONAL CLOCK RATES.
6. FOR DIAGNOSTIC CHECKOUT OF DH11-AA, AB, OR AC, REPLACES M971 WITH M974.
7. THIS SLOT CONTAINS MODEM CONTROL MODULE M7807 WITH DH11-AD.
8. THIS SLOT CONTAINS MODEM CONTROL MODULE M7808 WITH DH11-AD.
9. THIS SLOT CONTAINS EIA CONVERTER AND PRIORITY MODULE M5906 FOR DH11-AD OR AE.



5.0 MAINTENANCE PROCEDURES  
-----6.1 INTRODUCTION  
-----

THIS SECTION DESCRIBES HOW TO USE MD-DZDHM AS A TROUBLESHOOTING TOOL. IT OUTLINES SOME PRELIMINARY CHECKS TO MAKE BEFORE STARTING DETAILED DEBUG PROCEDURES. IT ATTEMPTS TO PROVIDE THE USER WITH SUGGESTIONS FOR PROCEEDING FROM THE ERROR PRINTOUT TO DETAILED ISOLATION OF THE FAULT.

6.2 PRELIMINARY CHECKS  
-----

## A. VISUAL INSPECTION

PERFORM A VISUAL INSPECTION OF THE DH11 SUBSYSTEM TO INSURE THAT:

- 1) ALL MODULES ARE INSTALLED IN THEIR PROPER SLOTS (REFER TO PARA 5.3) AND ARE PROPERLY SEATED.
- 2) THE CABLING IS CORRECT AND ALL CABLE CONNECTORS ARE FIRMLY SEATED.
- 3) THE REQUIRED MAINTENANCE CONNECTORS ARE PROPERLY INSTALLED. (REFER TO SECTION 6.3)

## B. POWER CHECKS

USE A SCOPE TO CHECK THE FOLLOWING POWER SUPPLY AND CONTROL SIGNALS ON THE DH11 BACKPLANE:

+15 VDC	GRAY WIRE
-15 VDC	BLUE WIRE
+5 VDC	RED WIRE
AC LO	YELLOW WIRE
DC LO	PURPLE WIRE

NOTES: USE THE BLACK WIRE FOR GROUND REFERENCE

"AC LO" AND "DC LO" SHOULD BOTH BE "HIGH" - "LOW" GOING GLITCHES ON THESE LINES CAN CAUSE UNUSUAL AND SUBTLE SYMPTOMS.

6.3 MAINTENANCE CONNECTORS  
-----

MOST OF THE TESTS IN MD-DZDHM USE HARDWARE DIAGNOSTIC AIDS TO TURN THE DATA AROUND. THESE AIDS REQUIRE THAT THE USER INSTALL SPECIFIC JUMPERS OR MODULES BEFORE RUNNING THE PROGRAM. DEPENDENT UPON THE SPECIFIC DH11 CONFIGURATION AND THE TYPE OF TESTING DESIRED, CERTAIN MAINTENANCE AIDS MUST BE INSTALLED AS OUTLINED BELOW:

## A. DH11-AA, AB, OR AC CONFIGURATIONS

- 1) TESTING LOGIC FOR ALL LINES WITHOUT DATA CABLES OR LEVEL CONVERTERS.

- A. REMOVE THE DATA CABLE FROM SLOT B7 IN EACH DH11 TO BE TESTED.
  - B. INSTALL AN M974 MAINT JUMPER MODULE INTO SLOT B7 OF EACH DH11 TO BE TESTED.
- 2) TESTING ALL 16. LINES INCLUDING DATA CABLES WHICH CONNECT TO DISTRIBUTION PANEL. DOES NOT TEST LEVEL CONVERTER CIRCUITS LOCATED IN DISTRIBUTION PANEL.
    - A. INSTALL THE M974 MAINT JUMPER MODULE INTO SLOT B3 OF THE MULTIPLEXOR DISTRIBUTION PANEL FOR EACH DH11 TO BE TESTED. ALL LEVEL CONVERTERS IN THE DISTRIBUTION PANEL MUST BE REMOVED FOR THIS TEST.
  - 3) TESTING ONE OR MORE SINGLE LINES INCLUDING EIA LEVEL CONVERTERS AND DEVICE CABLES WHICH ARE NOT TESTED IN 1 AND 2 ABOVE.
    - A. INSTALL AN H315 TEST CONNECTOR AT THE END OF THE DEVICE CABLE FOR EACH LINE TO BE TESTED.

#### B. DH11-AD CONFIGURATION

1. TESTING ALL 16. LINES WITHOUT DATA CABLES
  - A. DISCONNECT THE DATA CABLES (2) FROM THE TWO CONNECTORS ON THE M5906 MODULE (SLOT AB7 OF THE DH11 BACKPLANE).
  - B. INSTALL TWO H8611 TEST CONNECTORS ON THE M5906 IN PLACE OF THE CABLES.
2. TESTING ONE OR MORE SINGLE LINES INCLUDING DATA CABLES
  - A. DISCONNECT THE DEVICE CABLE FROM THE DH11-AD DISTRIBUTION PANEL FOR EACH LINE TO BE TESTED.
  - B. INSTALL AN H315 TEST CONNECTOR IN ITS PLACE ON THE DH11-AD DISTRIBUTION PANEL.

NOTE: TO TEST THE DEVICE CABLE AS WELL, INSTALL THE H315 TEST CONNECTOR AT THE END OF THE DEVICE CABLE AND LEAVE THE DEVICE CABLE CONNECTED TO THE DISTRIBUTION PANEL. WHEN RUN IN THIS CONFIGURATION THE OPERATOR CAN SET THE SR=002000, THEREBY ENABLING THE PROGRAM TO PERFORM AN ABBREVIATED DM11-BB TEST. IN THIS WAY ALL THE LEVEL CONVERTERS AND CABLES CAN BE CHECKED WITH JUST ONE PROGRAM.

6.4 COMPLETE DH11 SUBSYSTEM CHECKOUT

SEQ 0046

COMPLETE DH11 SUB-SYSTEM VERIFICATION INVOLVES RUNNING THE FOLLOWING PROGRAMS IN THE SEQUENCE SUGGESTED:

## A. MD-11-DZDHM DH11 DIAGNOSTIC

LOAD AND RUN THE BASIC DIAGNOSTIC CONFIGURED TO TEST ALL 16 LINES ON ALL DH11'S INSTALLED IN THE SYSTEM AND ALLOW IT TO COMPLETE AT LEAST TWO COMPLETE PASSES. (THE FIRST PASS IS A QUICK VERIFY WITHOUT SUB-TEST ITERATIONS AND THE SECOND PASS INCLUDES SUB-TEST ITERATIONS). IF ANY ERRORS ARE REPORTED, STOP HERE, AND REFER TO PARA 6.5 FOR SUBSEQUENT PROCEDURES.

## B. MD-11-DZDHN DATA RELIABILITY TEST

LOAD AND RUN THE DATA RELIABILITY SUB-PROGRAM OF MD-11-DZDHN CONFIGURED TO TEST ALL 16 LINES ON ALL DH11'S INSTALLED IN THE SYSTEM AND ALLOW IT TO COMPLETE AT LEAST ONE PASS WITH SRO7=0 (QUICK TEST MODE). IN THIS MODE ONE PASS TAKES APPROXIMATELY 5 MINUTES. IF ANY ERRORS ARE REPORTED, REFER TO THE DOCUMENTATION FOR MD-11-DZDHN FOR SUBSEQUENT PROCEDURES.

FOR MORE COMPLETE DATA RELIABILITY TESTING THE PROGRAM MAY BE RUN WITH SRO7=1 (COMPLETE TEST) BUT THIS WILL REQUIRE A RUN TIME OF APPROX 15 MINUTES FOR EACH SELECTED LINE, SO IN MOST CASES IT IS ONLY USED FOR OVER-NIGHT RUNS.

## C. SYSTEMS EXERCISER "DHAX" EXERCISER MODULE

WHERE "X" DESIGNATES THE REVISION LEVEL IN USE.

ASSUMING THAT BOTH THE DIAGNOSTIC AND THE DATA RELIABILITY INDICATE ERROR FREE PERFORMANCE, THE FINAL STEP IS TO RUN THE SYSTEM'S EXERCISER PROGRAM THAT INCLUDES A DH11 EXERCISER MODULE. THIS IS NECESSARY TO DETECT CERTAIN CLASSES OF BUS PROBLEMS THAT ONLY MANIFEST THEMSELVES WHEN THE DH11 IS RUN CONCURRENTLY WITH ALL THE OTHER DEVICES IN THE SYSTEM

IF ALL TESTS UP TO THIS POINT INDICATE ERROR FREE PERFORMANCE OF THE DH11, THE SUB-SYSTEM SHOULD BE CAPABLE OF RUNNING SYSTEM SOFTWARE. THERE ARE, HOWEVER, CERTAIN SUBTLE OR INTERMITTENT PROBLEMS THAT COULD STILL CAUSE THE DH11 SUB-SYSTEM TO FAIL IN THE OPERATING SYSTEM ENVIRONMENT. IN THESE RARE CASES, THE USER WILL HAVE TO USE THE SYMPTOMS GATHERED FROM THE FAILING MODE TO ISOLATE THE PROBLEM. ONCE A SYMPTOM IS RECOGNIZED, THE TWO OTHER PROGRAMS IN MD-DZDHN, THE ECHO TEST AND THE DATA PATTERNS/CABLE TESTS MAY PROVE USEFUL AS A TROUBLESHOOTING AID TO DUPLICATE THE PROBLEM FOR FAULT ISOLATION.

EACH TEST IN THE LISTING IS PREFACED BY A STANDARD MAINTENANCE HEADER TO PROVIDE INFORMATION THAT WILL FACILITATE RAPID ISOLATION OF THE FAULT THAT CAUSED A PARTICULAR TEST TO FAIL. EACH HEADER HAS THE SAME FORMAT (SEE EXAMPLE BELOW) AS FOLLOWS:

TEST ABSTRACT: THIS IS A CAPSULE SUMMARY OF WHAT THE TEST IS DESIGNED TO TEST AND HOW IT OPERATES.

ERRORS: LISTS THE PARTICULAR ERROR CALLS INVOKED BY THE TEST WHEN A FAULT IS DETECTED.  
(REFER TO PARA 3.1.2 AND 3.1.3 FOR A DETAILED DESCRIPTION OF THE ERROR CALL INFORMATION)

SYNC: LISTS ONE OR MORE SIGNALS THAT MAY BE USED TO SYNCHRONIZE THE OSCILLOSCOPE WHEN AN ERROR LOOP IS ESTABLISHED (SR09=1). FOR (H) SIGNALS USE (-) SLOPE TO TRIGGER ON THE TRAILING EDGE OF THE SIGNAL AND FOR (L) SIGNALS USE (+) SLOPE TO TRIGGER ON THE TRAILING EDGE.

DEBUG: CONTAINS SUGGESTIONS OF THINGS TO CHECK AND WHERE POSSIBLE THE MOST PROBABLE MODULE IS GIVEN.

KEY LOGIC: CONTAINS A LIST OF LOGIC SIGNALS AND/OR LOGIC COMPONENTS WITH MODULE NAMES AND PRINT NUMBERS TO RELATE THE TEST ROUTINE FUNCTION TO THE FUNCTIONAL AREAS OF LOGIC WITHIN THE PRINTS. WHERE POSSIBLE SIGNAL PIN NOS. ARE LISTED.



EXAMPLE: MAINTENANCE HEADER FOR TEST 1  
\*\*\*\*\*

TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST ATTEMPTS TO REFERENCE EACH OF THE EIGHT REGISTERS IN THE DM11 SELECTED FOR TEST USING ITS ASSIGNED UNIBUS ADDRESS. IF ANY ADDRESS FAILS TO RESPOND A BUS ERROR TRAP VECTORS THE TEST TO THE ERROR SET-UP AND CALL ROUTINE. AFTER THE ERROR IS TYPED THE TEST WILL TEST THE NEXT DM11 ADDRESS IN SEQUENCE UNTIL ALL EIGHT ARE TESTED.

ERRORS:  
\*\*\*\*\*

- 1.) ERROR 11 REPORTS THAT THE REGISTER WHOSE ADDRESS IS IN R2 FAILED TO RESPOND WITH "SSYN" WHEN REFERENCED.

SYNC: (NONE)  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

- 1.) PROBLEM IS MOST LIKELY THE M7277 MODULE.
- 2.) IF ALL EIGHT REGISTERS FAIL TO RESPOND, MAKE SURE THAT YOU CONFIGURED THE PROGRAM PROPERLY BEFORE STARTING. IF YOU DID, CHECK THE SETTINGS OF THE ADDRESS SELECT JUMPERS ON THE M7277 MODULE.
- 3.) IF ONE OR MORE RESPONDED PROPERLY, SET UP AN ERROR SCOPE LOOP AND BACKTRACK THROUGH THE LOGIC STARTING WITH THE KEY LOGIC SIGNALS LISTED BELOW.

KEY LOGIC:  
\*\*\*\*\*

M7277	SH3	SSYN H	CE2
		DEVICE RESPONDING L	E72-6
	SH4	DEVICE SELECTED H	E09-11

?

FLOW CHART

\*\*\*\*\*

MD-11-DZDHM-B DH11 DIAGNOSTIC

\*\*\*\*\*

COPYRIGHT 1976  
DIGITAL EQUIPMENT CORPORATION

TABLE OF CONTENTS  
\*\*\*\*\*

PAGE 01	PROGRAM START-UP 1
PAGE 02	PROGRAM START-UP 2
PAGE 03	TEST 01 CHECK SSYN RESPONSE FROM ALL DH11 REGISTERS
PAGE 04	TEST 02 TEST THAT "MSTCLR" CAN CLEAR "SCR","LPR","BKR", AND "SSR" REGS
PAGE 05	TEST 03 TEST "SCR" REG R/W BITS CAN SET/CLR (NORMAL MODE)
PAGE 06	TEST 04 TEST "SCR" REG READ ONLY BITS (NORMAL MODE)
PAGE 07	TEST 05 TEST "SCR" REG BITS THAT CAN BE SET/CLR IN MAINT MODE
PAGE 08	TEST 06 TEST THAT ALL R/W BITS IN "LPR" CAN BE SET/CLR
PAGE 09	TEST 07 TEST THAT ALL R/W BITS IN "BKR" CAN BE SET/CLR
PAGE 10	TEST 10 TEST THAT ALL R/W BITS IN "SSR" CAN BE SET/CLR
PAGE 11	TEST 11 TEST THAT CLR/SET OF BIT "N" IN "LPR" DOES NOT CLEAR ANY OTHER BITS
PAGE 12	TEST 12 TEST THAT CLR/SET OF BIT "N" IN "BKR" DOES NOT CLEAR ANY OTHER BITS
PAGE 13	TEST 13 TEST THAT CLR/SET OF BIT "N" IN "SSR" DOES NOT CLEAR ANY OTHER BITS
PAGE 14	TEST 14 "CAR" MEMORY ADDRESSING TEST
PAGE 15	TEST 15 "BCR" MEMORY ADDRESSING TESTS
PAGE 16	TEST 16 "CAR" REGISTER TEST - ALL 1'S/ALL 0'S/ALL LINES
PAGE 17	TEST 17 "BCR" REGISTER TEST - ALL 1'S/ALL 0'S/ALL LINES
PAGE 18	TEST 20 "CAR" MEMORY PATTERNS TEST - 0'S DISTURB
PAGE 19	TEST 21 "BCR" MEMORY PATTERNS TEST - 0'S DISTURB
PAGE 20	TEST 22 "CAR" MEMORY PATTERNS TEST - 1'S DISTURB
PAGE 21	TEST 23 "BCR" MEMORY PATTERNS TEST - 1'S DISTURB
PAGE 22	TEST 24 "CAR" EXT MEMORY BITS TEST
PAGE 23	TEST 25 TEST INTR. ENAB. BITS - INTR. CONDITION DISABLED
PAGE 24	TEST 26 TEST CHAR. AVAIL. I.E. WITH INTR. CONDITION ACTIVE



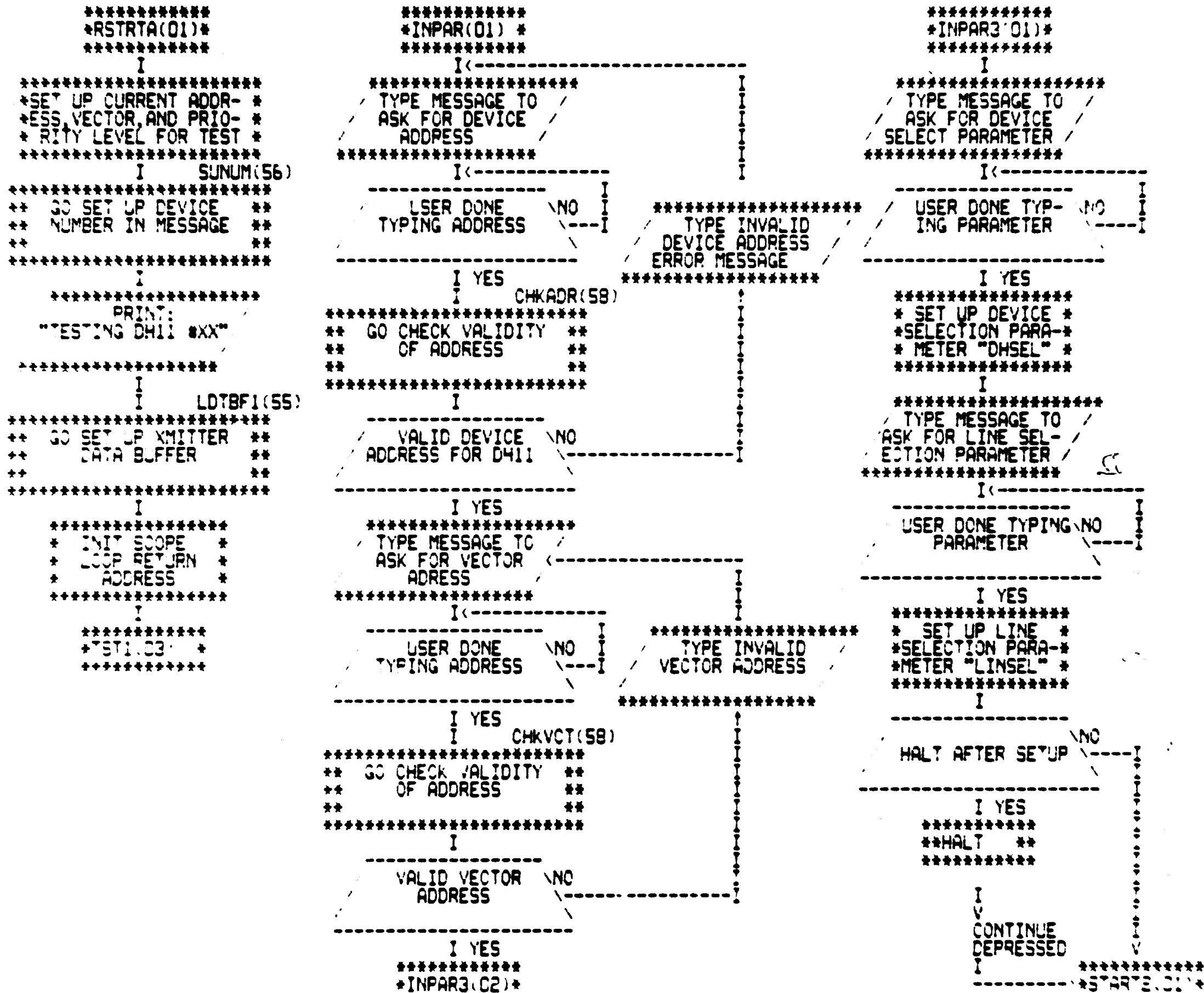
TABLE OF CONTENTS  
\*\*\*\*\*

PAGE 26	TEST 30 TEST NON-EX MEM I.E. WITH INTR. CONDITION ACTIVE
PAGE 27	TEST 31 TEST TRANSMIT DONE I.E. WITH INTR. CONDITION ACTIVE
PAGE 28	TEST 32 BASIC "NPR" LOGIC TEST 1
PAGE 29	TEST 32 BASIC "NPR" LOGIC TEST 1 (CONT.)
PAGE 30	TEST 33 BASIC "NPR" LOGIC TEST 2
PAGE 31	TEST 34 TEST THAT CHAR. AVAIL. CAN GENERATE RCVR. INTR.
PAGE 32	TEST 35 TEST THAT SILO STATUS REGISTER COUNTS UP CORRECTLY
PAGE 33	TEST 36 TEST THAT SILO STATUS REG DOWN COUNTS CORRECTLY
PAGE 34	TEST 37 TEST SILO ALARM LEVEL
PAGE 35	TEST 40 VERIFY STORAGE OVERFLOW - NON MAINT MODE - ALL LINES
PAGE 36	TEST 41 TRANSMITTER TIMING TEST - ALL LINES - ALL SPEEDS
PAGE 37	TEST 42 RECEIVER TIMING TEST - ALL LINES - ALL SPEEDS
PAGE 38	TEST 43 BASIC DATA TEST - ALL LINES - ALL CHAR. LENGTHS
PAGE 39	TEST 44 SINGLE LINE DATA TEST-ALL LINES (PAGE 1)
PAGE 40	TEST 44 SINGLE LINE DATA TEST-ALL LINES (PAGE 2)
PAGE 41	TEST 45 BASIC PARITY LOGIC TEST - ALL LINES - ODD PARITY
PAGE 42	TEST 46 MULTI-LINE PARITY-DATA TEST - PAGE 1
PAGE 43	TEST 46 MULTI-LINE PARITY TEST - PAGE 2
PAGE 44	TEST 47 AUTO-ECHO TEST 1-ALL LINES
PAGE 45	TEST 50 AUTO-ECHO TEST 2-ALL LINES (PAGE 1)
PAGE 46	TEST 50 AUTO ECHO TEST 2-ALL LINES (PAGE 2)
PAGE 47	TEST 51 AUTO-ECHO TEST-3
PAGE 48	TEST 52 BREAK BIT TEST-ALL LINES (PAGE 1)
PAGE 49	TEST 52 BREAK BIT TEST-ALL LINES (PAGE 2)

TABLE OF CONTENTS  
\*\*\*\*\*

PAGE 51	TEST 54 VERIFY THAT OVERRUN CAN SET PROPERLY-ALL LINES.
PAGE 52	SCOPE LOOP ROUTINE
PAGE 53	ERROR SERVICE ROUTINE
PAGE 54	COMMON DH11 SUB-ROUTINES - PAGE 1
PAGE 55	COMMON DH11 SUB-ROUTINES - PAGE 2
PAGE 56	COMMON DH11 SUB-ROUTINES - PAGE 3
PAGE 57	COMMON DH11 SUB-ROUTINES - PAGE 4
PAGE 58	COMMON DH11 SUB-ROUTINES - PAGE 5
PAGE 59	COMMON DH11 SUBROUTINES - PAGE 6





MC-11-DZDMM-B DH11 DIAGNOSTIC  
TEST 01 CHECK S5YN RESPONSE FROM ALL DH11 REGISTERS

\*\*\*\*\*  
\*TST1(02) \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\*LOAD R2 AND R5 \*  
\*WITH DMADR AND \*  
\*ADD 16(9) TO R5\*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SAVE TIMEOUT \*  
\* VECTOR ON THE \*  
\* STACK \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\*SET UP TIMEOUT \*  
\*VECTOR TO GO TO\*  
\* 3\$: ON TRAP \*  
\*\*\*\*\*

1\$ I  
\*\*\*\*\*  
\* SELECT NEXT \*  
\* DH11 REGISTER \*  
\* ADDRESS \*  
\*\*\*\*\*

2\$ I  
\*\*\*\*\*  
\* ATTEMPT TO \*  
\*ACCESS SELECTED\*  
\* ADDRESS \*  
\*\*\*\*\*

-----  
/ DID SELECTED \ YES \*\*\*  
/ DH11 ADDRESS CAUSE \ \*\*\*  
/ TIMEOUT TRAP ? \ \*\*\*  
-----

3\$ I SUER1(55)  
\*\*\*\*\*  
\*\* GO SET UP ERROR \*\*  
\*\* INFORMATION TO BE \*\*  
\*\* PRINTED \*\*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* RESET SP TO \*  
\* CORRECT FOR \*  
\* TRAP \*  
\*\*\*\*\*

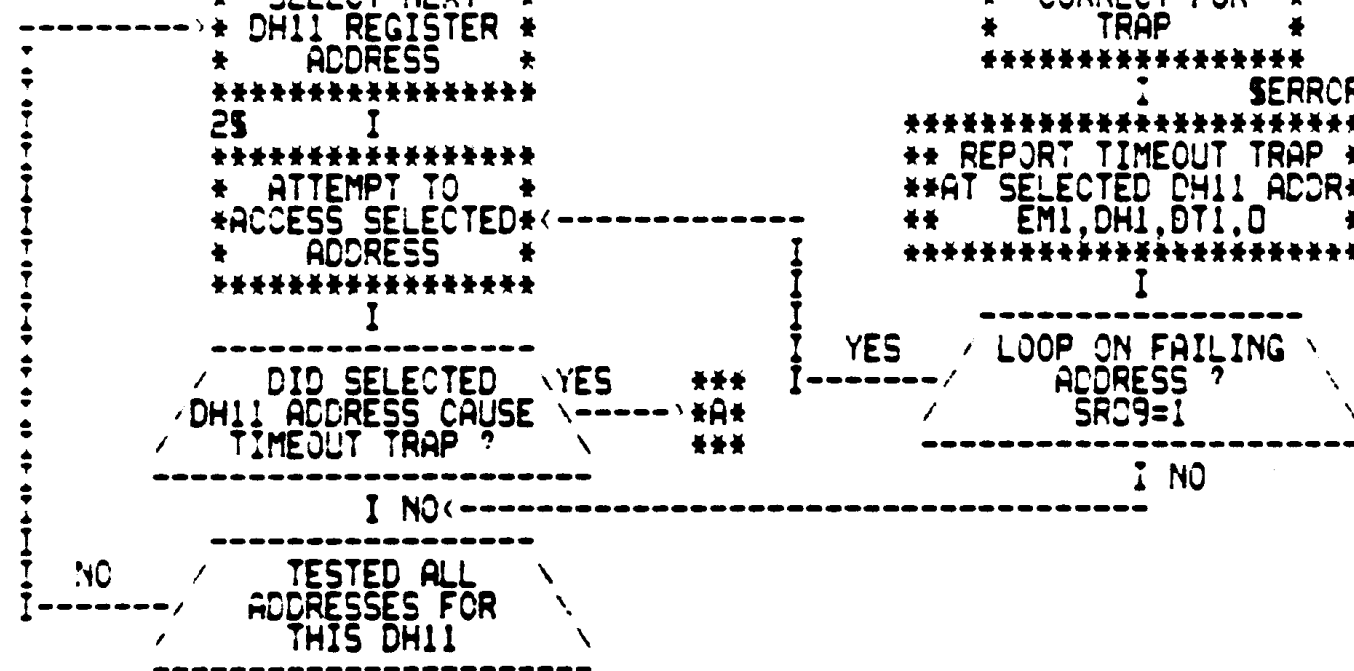
4\$ SERROR(53)  
\*\*\*\*\*  
\*\* REPORT TIMEOUT TRAP \*\*  
\*\* AT SELECTED DH11 ADDR \*\*  
\*\* EMI,DH1,DT1,0 \*\*  
\*\*\*\*\*

-----  
/ LOOP ON FAILING \  
/ ADDRESS ? \  
/ SRC9=1 \  
-----

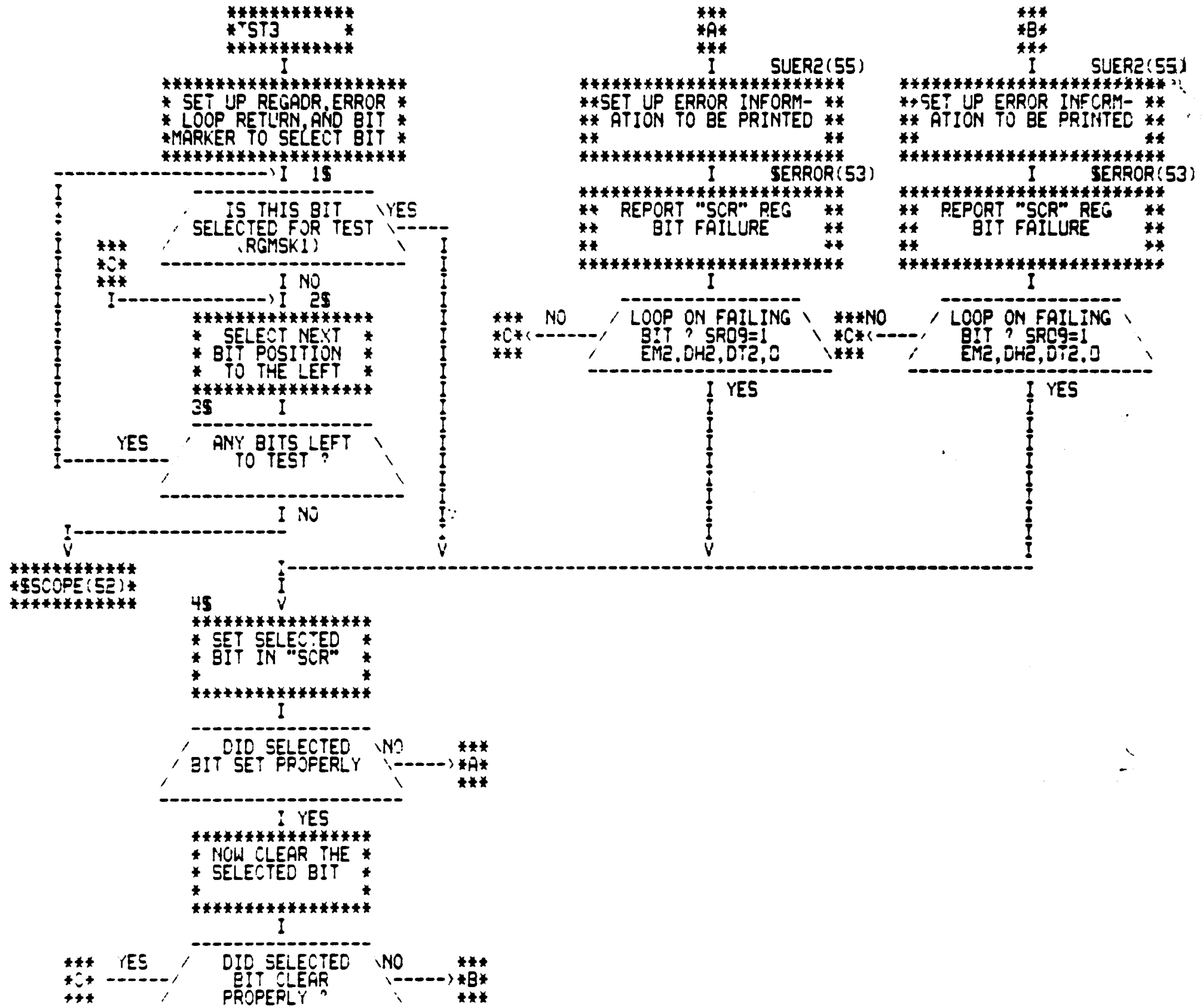
I NO  
-----  
/ TESTED ALL \  
/ ADDRESSES FOR \  
/ THIS DH11 \  
-----

I YES  
\*\*\*\*\*  
\* RESTORE PLUS \*  
\* TIMEOUT VECTOR \*  
\* FROM STACK \*  
\*\*\*\*\*

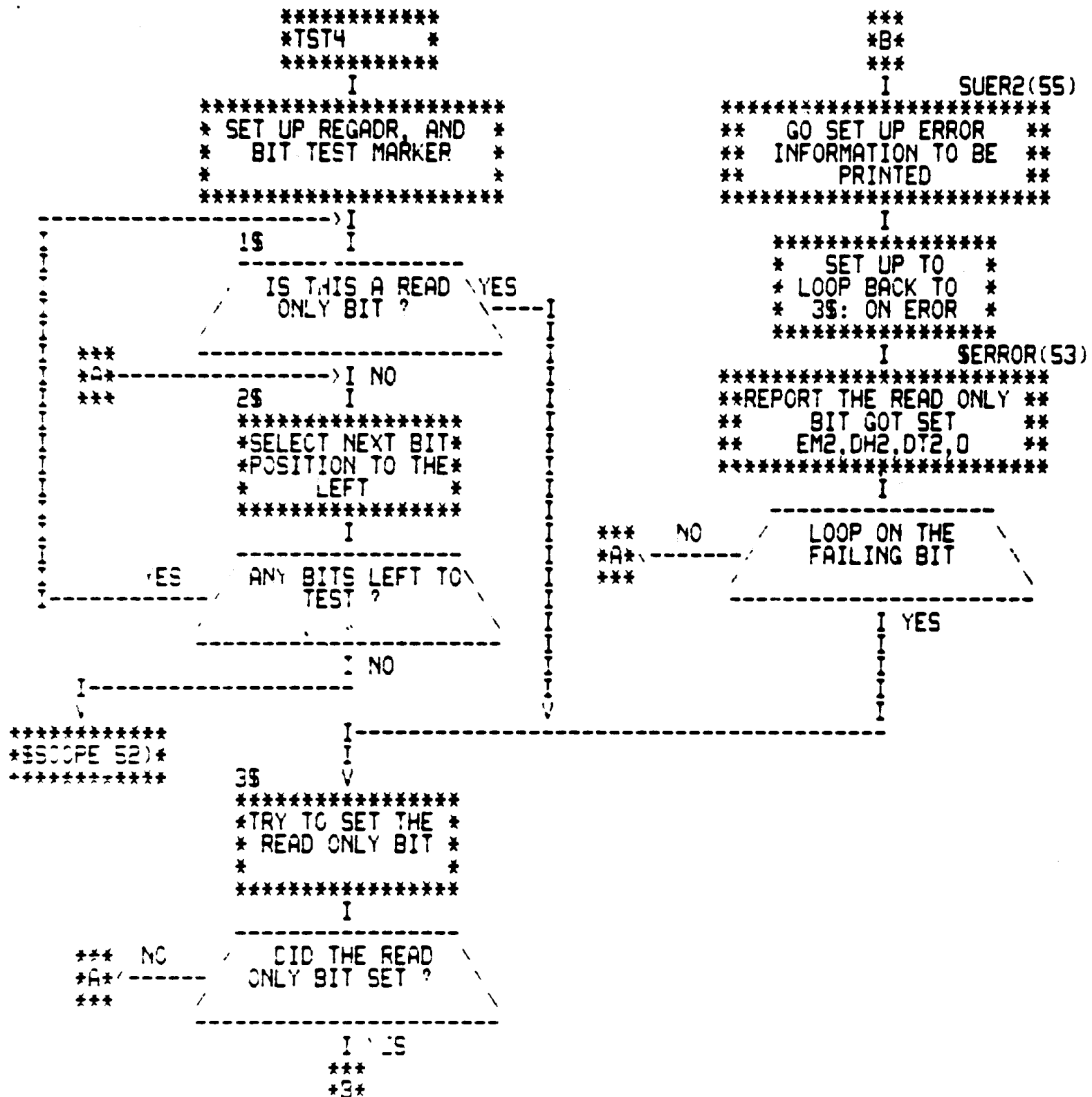
I  
\*\*\*\*\*  
\*SCOPE(52)\*  
\*\*\*\*\*

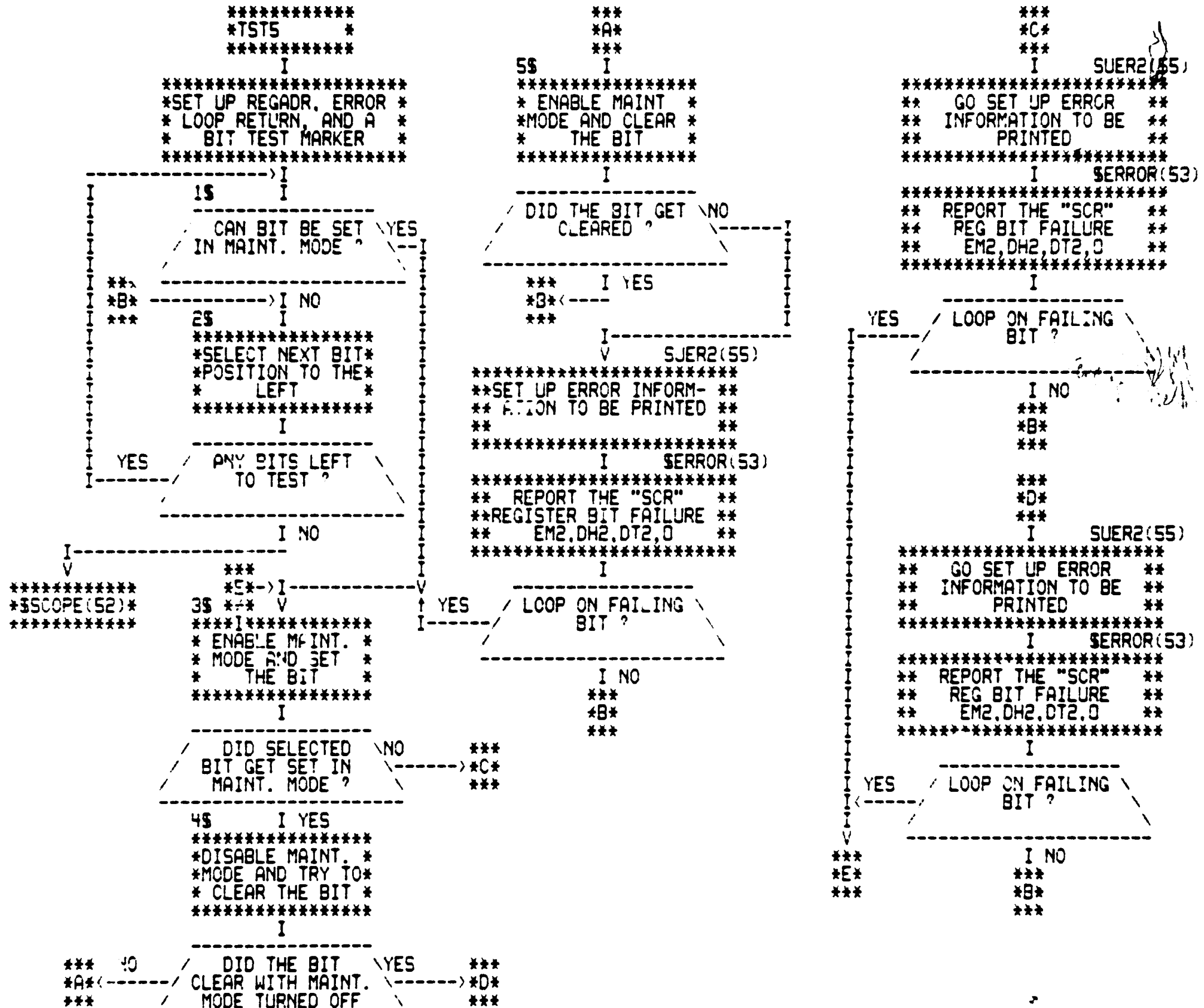


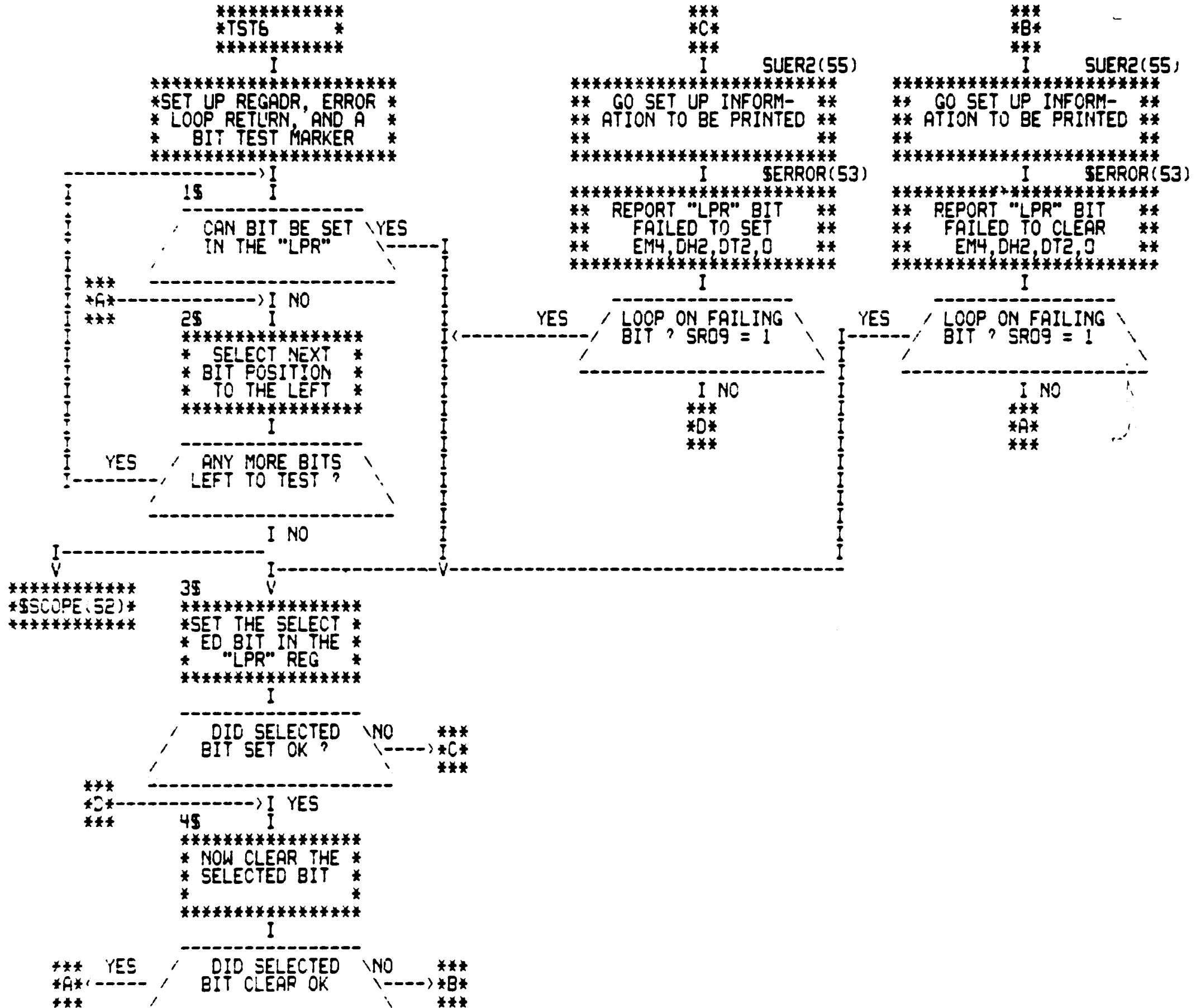


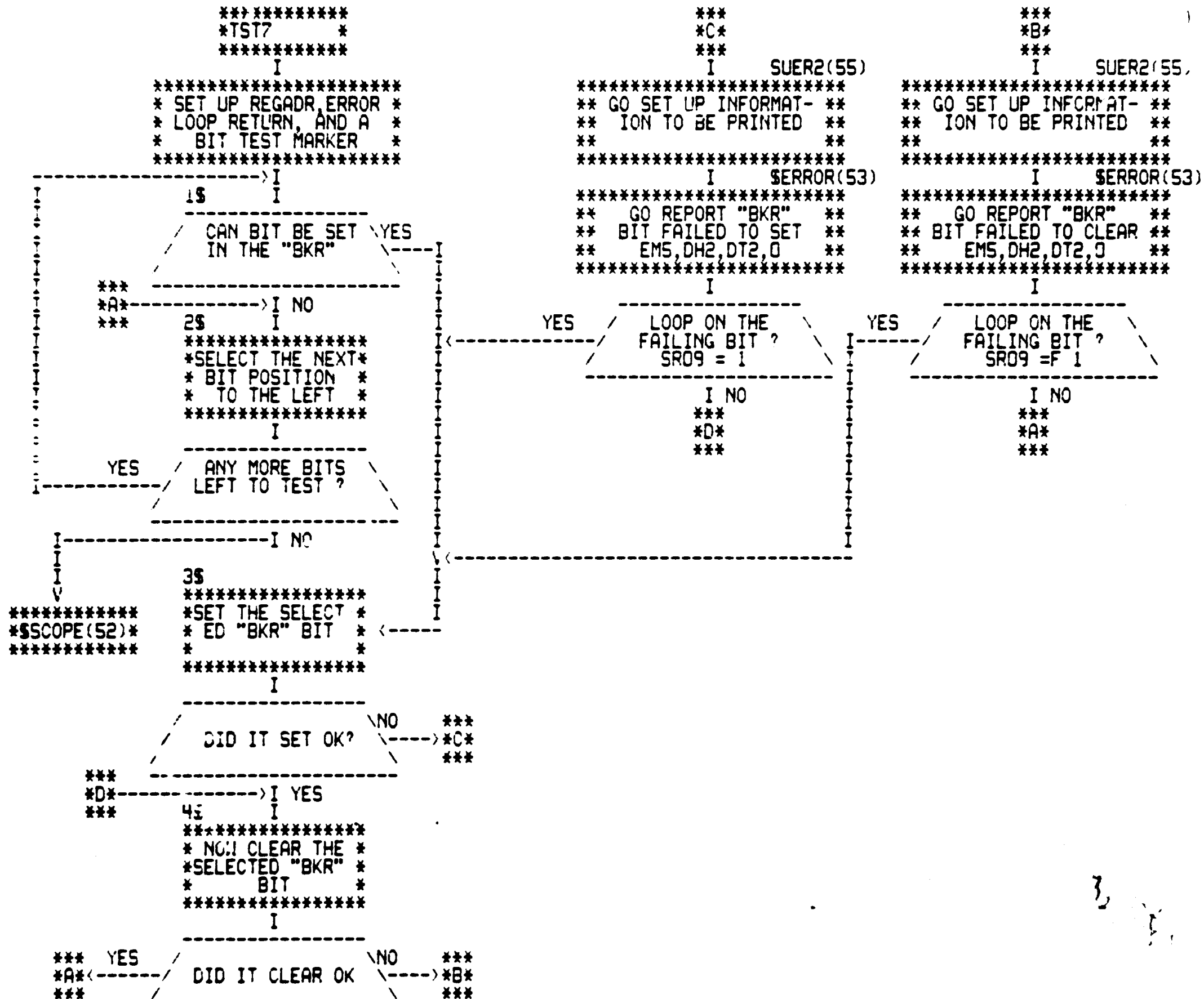


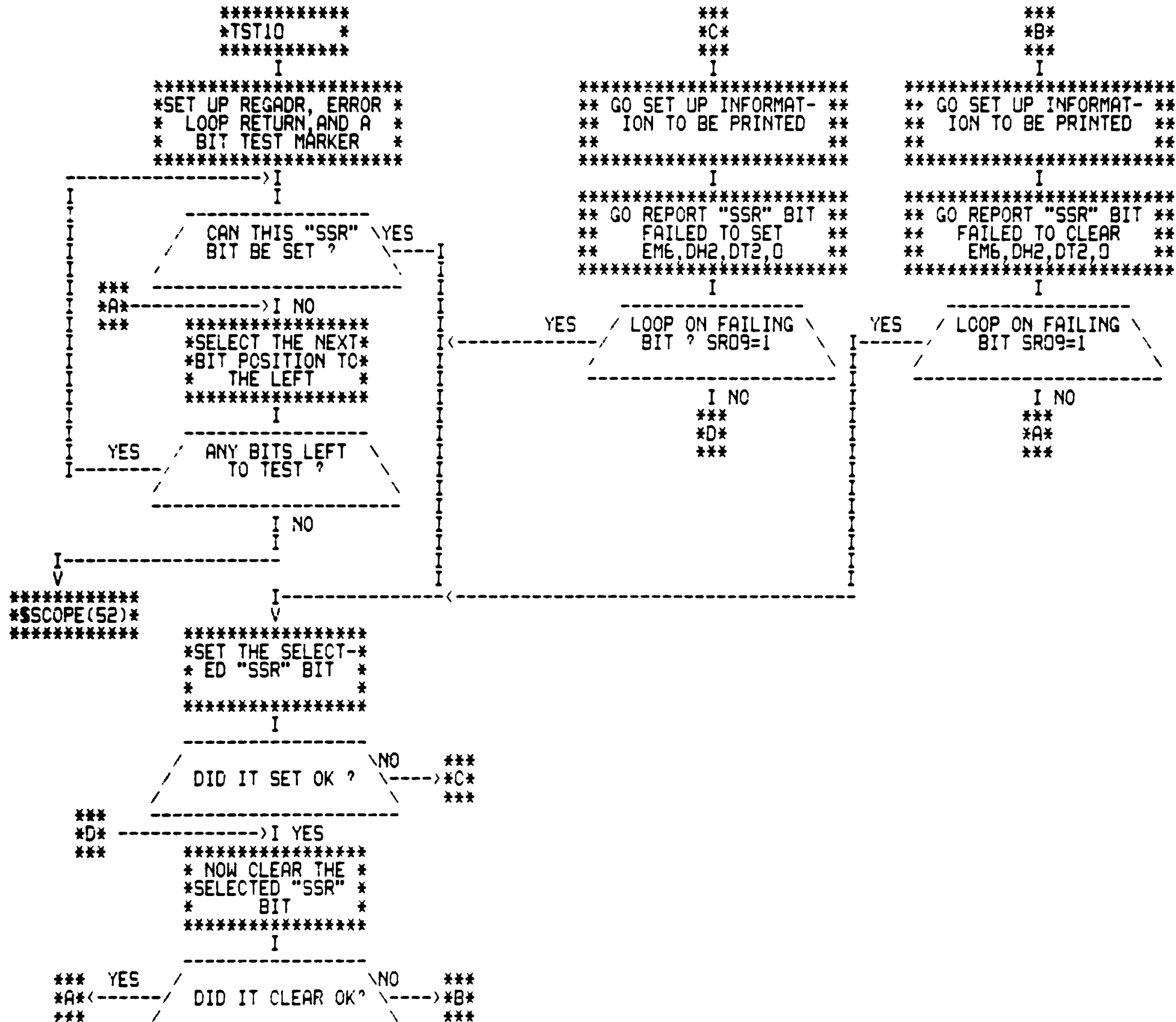




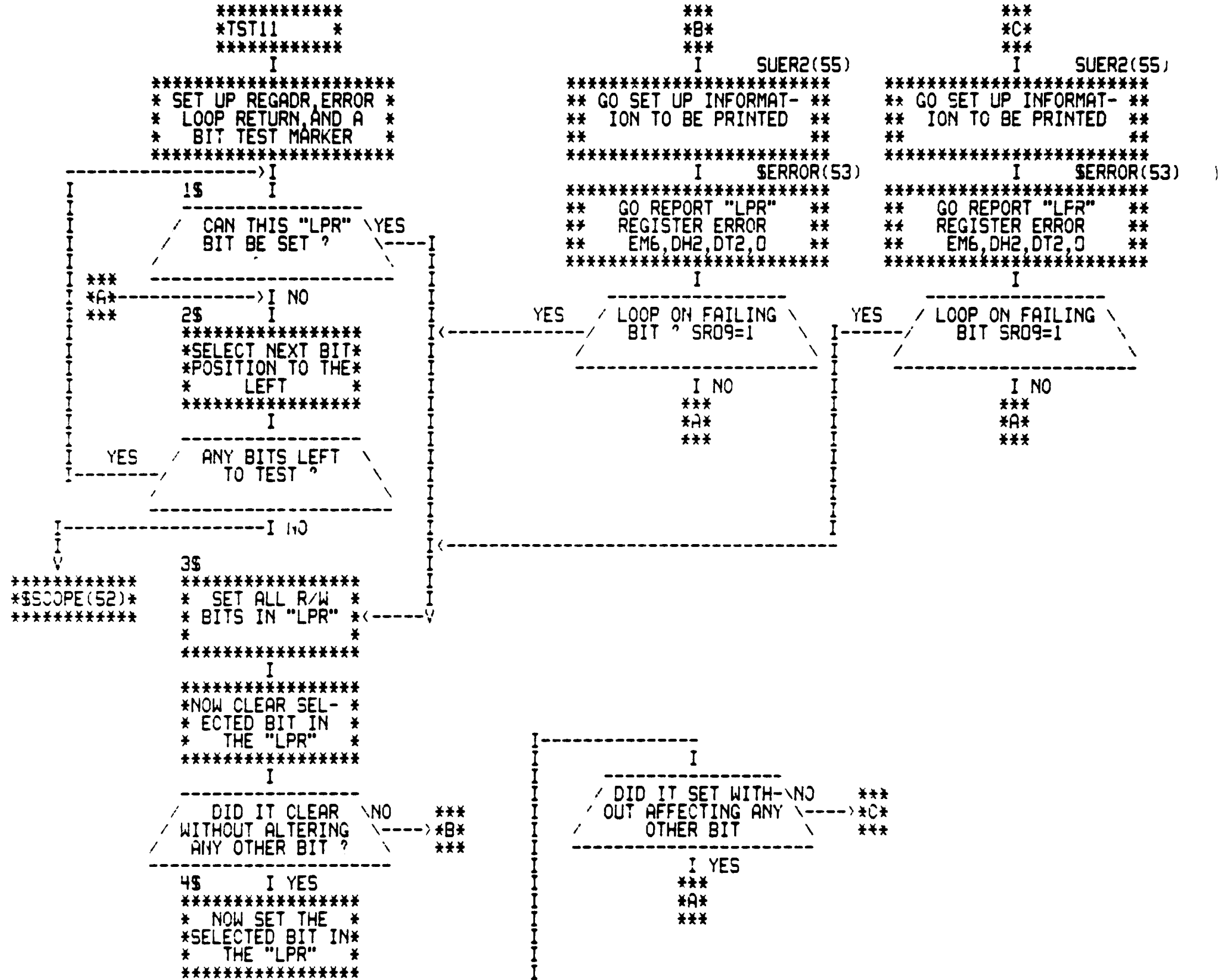








L05

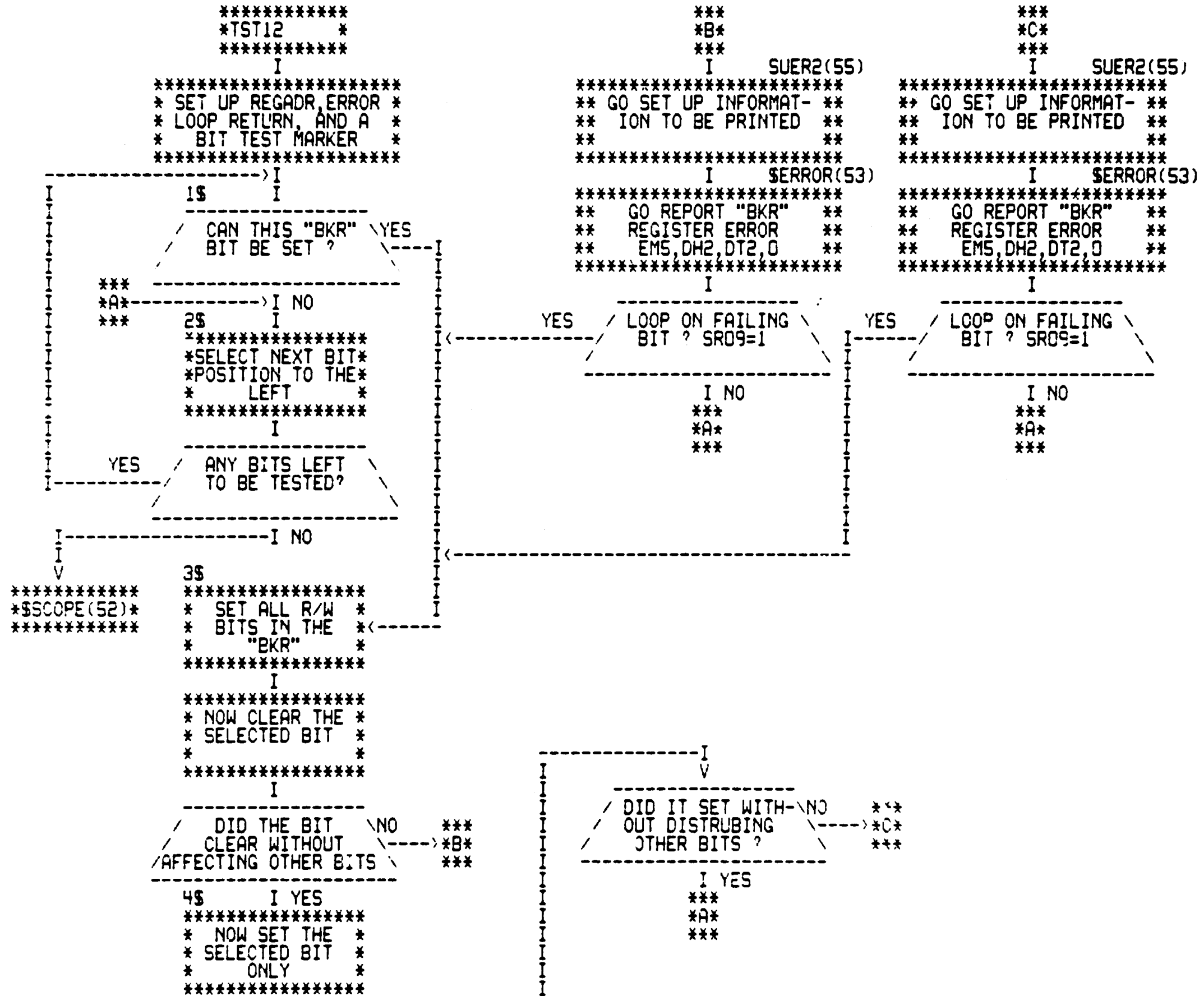


M05

MD-11-DZDMM-B DH11 DIAGNOSTIC  
TEST 12 TEST THAT CLR/SET OF BIT "N" IN "BKR" DOES NOT CLEAR ANY OTHER BITS

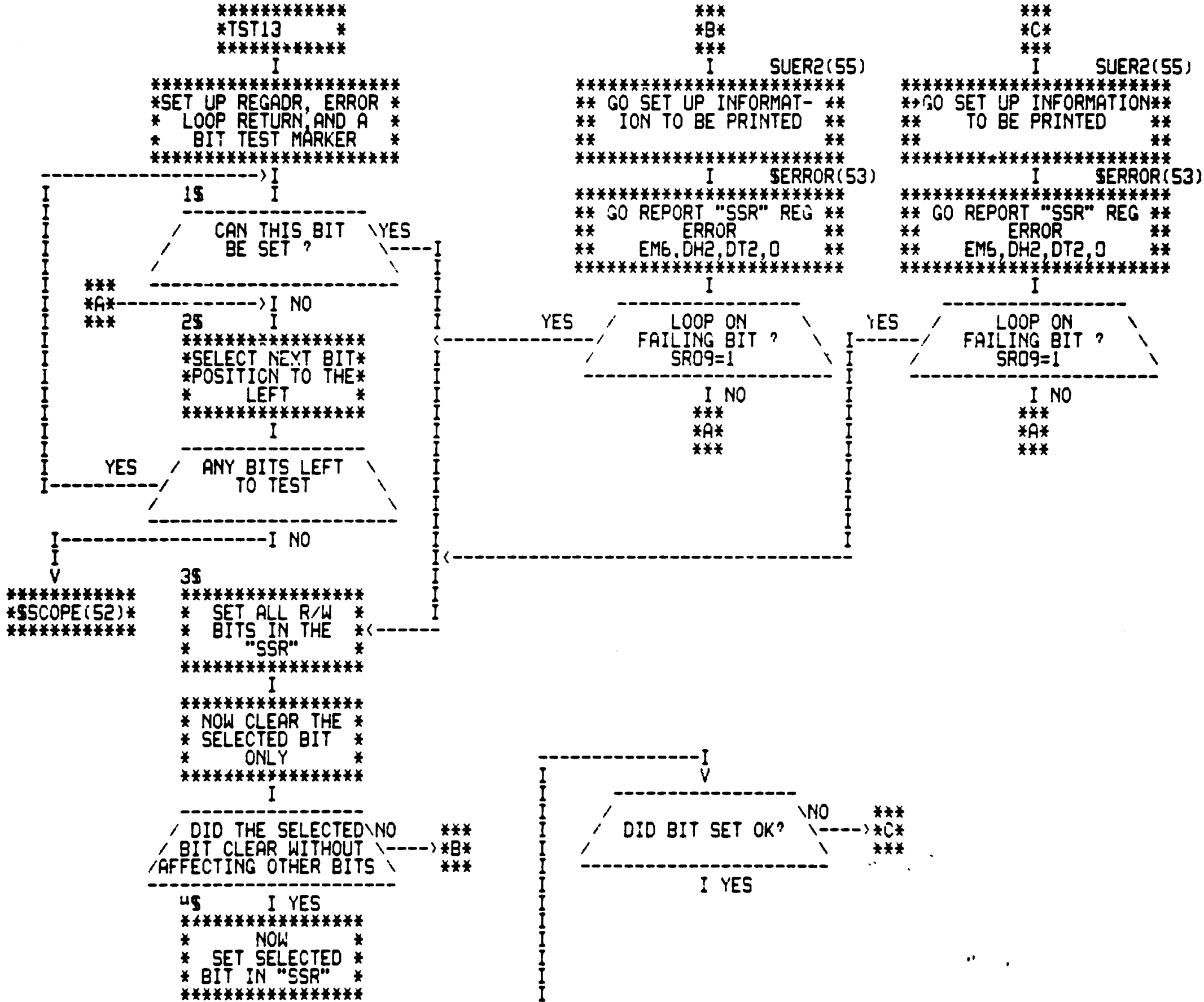
DECFL0 VER 00.12 23-SEP-76.14:43 PAGE 12

SEQ 0064





N05



```

*****
*TST14
*****
I
*****
* SET UP REGADR, AND *
* SAVE LINE SELECT *
* PARAMETER IN STMP7 *
*****
I
*****
*SET UP TO CHECK*
* ALL 16. LINES *
*
*****

```

```

***
*A*
***
I SUEP2(55)
*****
** GO SET UP INFORMAT- **
** ION TO BE PRINTED **
**
*****
I SUNUM(56)
*****
**GO SET LINE NO. INTO **
** ERROR MESSAGE **
**
*****

```

```

15
I
*****
* LOAD "CAR" MEMORY *
* WITH ADDRESS TEST *
* PATTERN *
*****

```

```

65
I
*****
*INIT TO RESTART*
* AT LINE 00 *
* FOR SETUP *
*****

```

```

I
*****
* SET UP ERROR *
* LOOP RETURN *
*
*****
I SERROR(53)
*****
** GO REPORT "CAR" **
** ADDRESSING ERROR **
** EM7,DH2,DT2,0 **
*****

```

```

35
I SELINE(60)
*****
**GO SELECT A LINE NO. **
** TO CHECK **
**
*****

```

```

YES / LOOP ON ERROR /
SRC9=1

```

```

YES
DONE CHECKING
ALL 16. LINES

```

```

45
I NO
*****
*READ "CAR" FOR *
* SELECTED LINE *
*
*****

```

```

*****
* READ "CAR" LINE *
* SELECTED LINE *
* PARAMETER IN STMP7 *
*****

```

```

*****
*SCOPE(52)*
*****

```

```

CORRECT PATTERN NO
READ FROM SELECTED LINE ?
***
*A*
***

```

```

55
I YES
*****
*UPDATE EXPECTED*
* TEST PATTERN *
* FOR NEXT LINE *
*****

```

NO

```

*****
*TST15 *
*****
I
*****
* SET UP REGADR AND *
* SAVE THE LINE SELECT *
* PARAMETER IN STMP7 *
*****

```

```

I
*****
*SET UP TO TEST *
* ALL 16.LINES *
*
*****

```

```

18 I
*****
* LOAD "BCR" WITH *
* ADDRESS TEST *
* PATTERN *
*****

```

```

I SELINE(60)
*****
** GO SELECT A LINE **
** NO. TO CHECK **
**
*****

```

```

YES / DONE CHECKING /
      / ALL 16. LINES ? /

```

```

*****
* RESTORE LINE *
* SECTION PARAM- *
* OVER FM STMP7 *
*****

```

```

I
*****
*SCOPE(S2)*
*****

```

```

I NO
48 I
*****
*READ "BCR" FOR *
* SELECTED LINE *
*
*****

```

```

CORRECT PATTERN / NO ***
      / READ ? / --- *A*

```

```

I YES
58 I
*****
*UPDATE EXPECT- *
*ED TEST PATTERN*
* FOR NXT LINE *
*****

```

```

***
*A*
***
I SUER2(55)

```

```

*****
**GO SET UP INFORMATION**
** TO BE PRINTED **
**
*****

```

```

I SUNUM(56)
*****
** GO SET UP LINE NO **
** IN ERROR MESSAGE **
**
*****

```

```

I
*****
* SET UP ERROR *
* LOOP RETURN *
*
*****

```

```

65 I
*****
*INIT TO RESTR *
* AT LINE 00 *
*
*****

```

```

I
*****
**GO REPORT "BCR" ADDR-**
** ESSING ERROR **
** EM10,DM2,DT2,0 **
*****

```

```

YES / LOOP ON ERROR /
      / SRO9=1 /

```

```

I NO

```

MD-11-DZDMM-B DH11 DIAGNOSTIC  
TEST 16 "CAR" REGISTER TEST - ALL 1'S ALL 0'S ALL LINES

\*\*\*\*\*  
\*TST16 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SET UP REGADR \*  
\*\*\*\*\*

\*\*\*  
\*A\*  
\*\*\*

I SUER2(55)  
\*\*\*\*\*  
\*\*GO SET UP INFORMATION\*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*\*  
\*\*\*\*\*

\*\*\*  
\*B\*  
\*\*\*

I SUER2(55)  
\*\*\*\*\*  
\*\*GO SET UP INFORMATION\*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*\*  
\*\*\*\*\*

I  
15 I SELINE(60)  
\*\*\*\*\*  
\*\*GO SELECT A LINE NO. \*\*  
\*\* TO TEST \*\*  
\*\* \*\*  
\*\*\*\*\*

I SERROR(53)  
\*\*\*\*\*  
\*\* GO REPORT "CAR" \*\*  
\*\* DATA ERROR \*\*  
\*\* \*\*  
\*\*\*\*\*

I SERROR(53)  
\*\*\*\*\*  
\*\* GO REPORT "CAR" \*\*  
\*\* DATA ERROR \*\*  
\*\* \*\*  
\*\*\*\*\*

YES  
I  
TESTED ALL  
SELECTED LINES

\*\*\*YES  
\*C\*  
\*\*\*  
LOOP ON FAILING  
LINE ? SRO9=1

\*\*\*YES  
\*C\*  
\*\*\*  
LOOP ON FAILING  
LINE ? SRO9=1

\*\*\*\*\*:\*\*\*\*\*  
\*SCOPE.SR\*  
\*\*\*\*\*

I NO  
\*\*\*\*\*  
\*WRITE ALL ONES \*  
\* INTO SELECTED \*  
\* "CAR" \*  
\*\*\*\*\*

I NO  
\*\*\*  
\*C\*  
\*\*\*

I NO  
\*\*\*  
\*C\*  
\*\*\*

I  
\*\*\*\*\*  
\*READ BACK SE- \*  
\* LECTED "CAR" \*  
\* \*  
\*\*\*\*\*

NO  
WAS IT ALL ONES? -----> \*A\*  
\*\*\*

I YES  
\*\*\*\*\*  
\* NOW CLEAR THE \*  
\* SELECTED "CAR" \*  
\* \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* READ BACK THE \*  
\* SELECTED "CAR" \*  
\* \*  
\*\*\*\*\*

YES  
WAS IT ALL ZEROS ? -----> \*B\*  
\*\*\*

MC-11-DZDMM-B DH11 DIAGNOSTIC  
TEST 17 "BCR" REGISTER TEST - ALL 1'S ALL 0'S ALL LINES

\*\*\*\*\*  
\*TST17 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SET LP REGADR \*  
\*\*\*\*\*

1\$ I SELINE(60)  
\*\*\*\*\*  
\*\*GO SELECT A LINE NO. \*\*  
\*\* TO TEST \*\*  
\*\*\*\*\*

YES / TESTED ALL  
SELECTED LINES? \

\*\*\*\*\* 2\$ I NO  
\*\*SCOPE(52)\*\*  
\*\*\*\*\*  
\*WRITE ALL ONES \*  
\* INTO SELECTED \*  
\*C\*-->\* "SCR" \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* READ BACK \*  
\*SELECTED "SCR" \*  
\*\*\*\*\*

-----  
/ WAS IT ALL ONES \ NO \*\*\*  
? ----- \*A\*  
----- \*\*\*

3\$ I YES  
\*\*\*\*\*  
\*WRITE ALL ZEROS\*  
\* INTO SELECTED \*  
\*D\*-->\* "BCR" \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* READ BACK \*  
\*SELECTED "BCR" \*  
\*\*\*\*\*

YES / WAS IT ALL ZEROS \ NO \*\*\*  
? ----- \*B\*  
----- \*\*\*

\*\*\*  
\*A\*  
\*\*\*

I SUER2(55)  
\*\*\*\*\*  
\*\*GO SET UP INFORMATION\*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*\*\*\*\*

I \$ERROR(53)  
\*\*\*\*\*  
\*\* GO REPORT "BCR" \*\*  
\*\* DATA ERROR \*\*  
\*\* EM10,DH2,DT2,0 \*\*  
\*\*\*\*\*

\*\*\* YES / LOOP ON FAILING \  
\*C\*--> LINE ' SRO9=1 \*C\*  
\*\*\*

I NO  
\*\*\*  
\*D\*  
\*\*\*

\*\*\*  
\*B\*  
\*\*\*

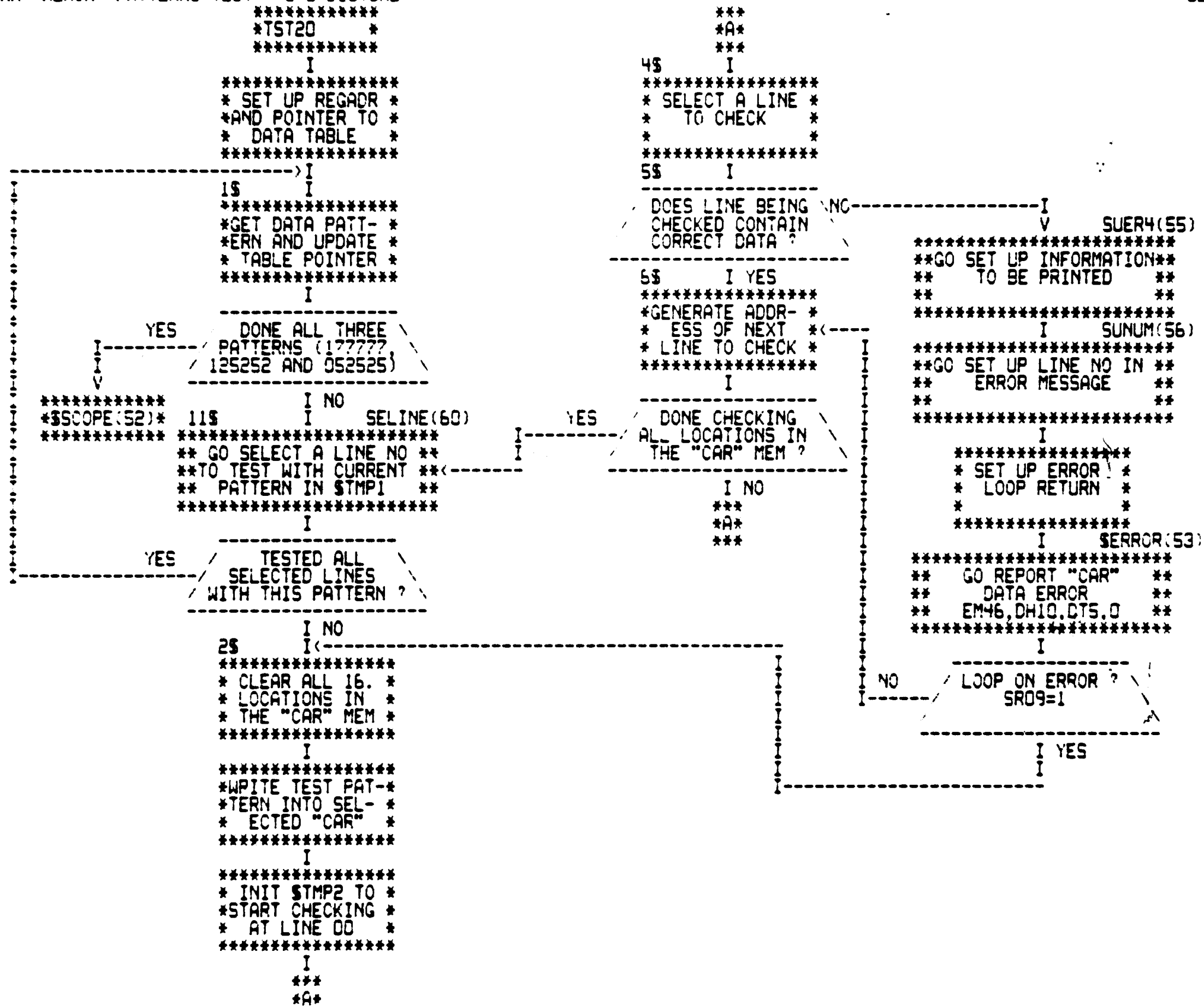
I SUER2(55)  
\*\*\*\*\*  
\*\*GC SET UP INFORMATION\*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*\*\*\*\*

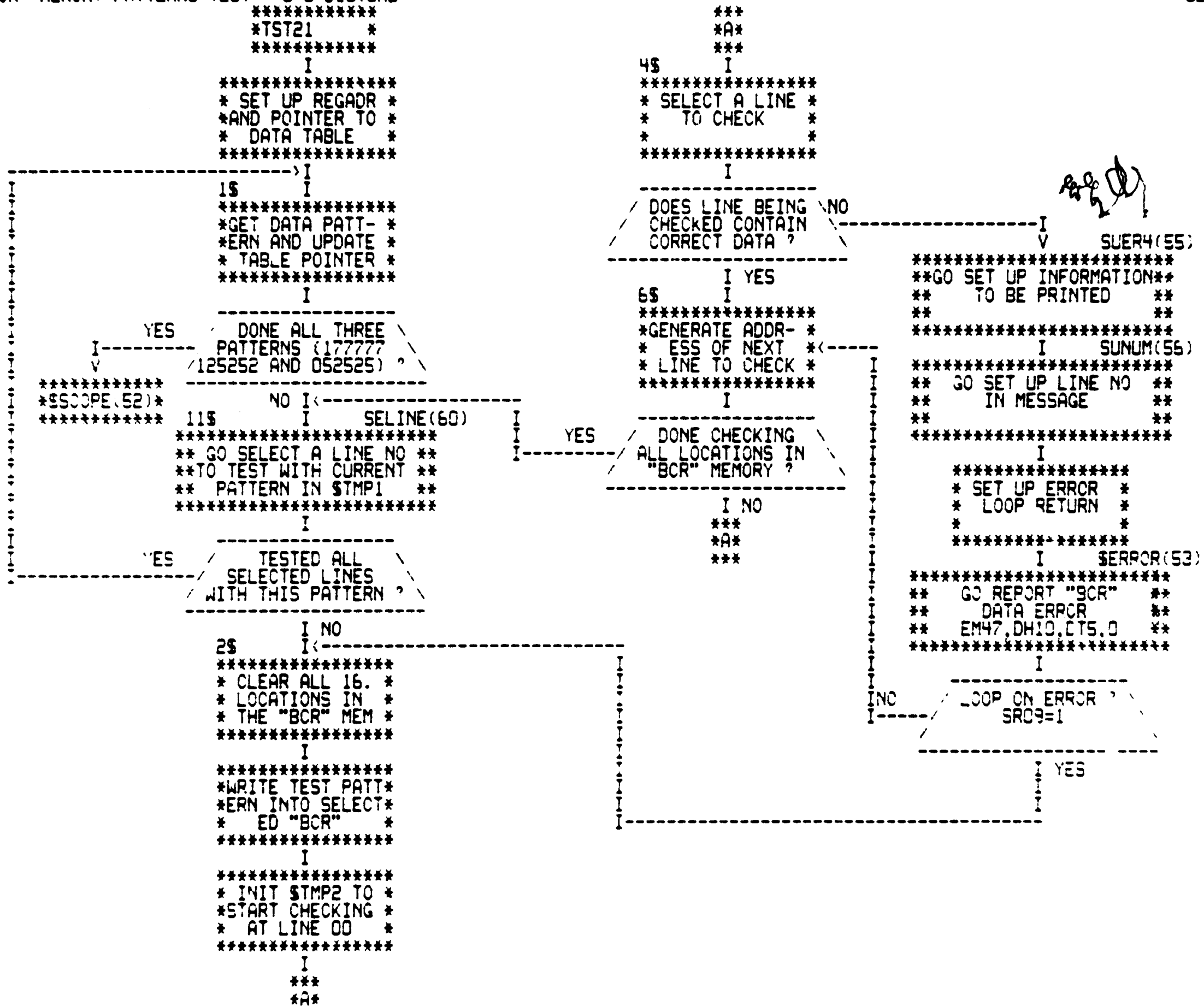
I \$ERROR(53)  
\*\*\*\*\*  
\*\* GO REPORT "BCR" \*\*  
\*\* DATA ERROR \*\*  
\*\* EM10,DH2,DT2,0 \*\*  
\*\*\*\*\*

\*\*\* YES / LOOP ON FAILING \  
\*C\*--> LINE ' SRO9=1 \*C\*  
\*\*\*

I NO  
|  
|  
|

MD-11-DZDMM-B DH11 DIAGNOSTIC  
TEST 20 "CAR" MEMORY PATTERNS TEST - 0'S DISTURB



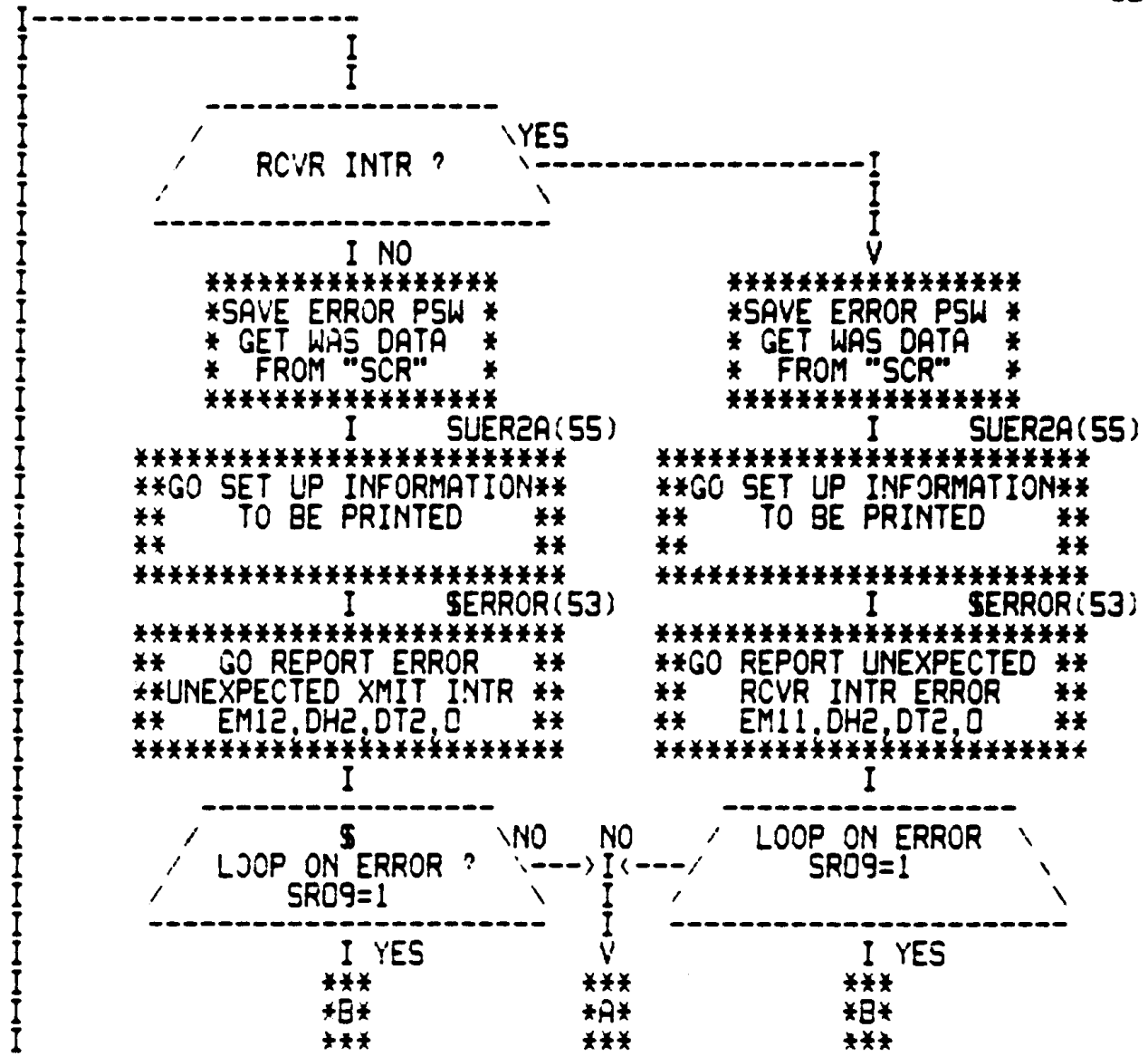
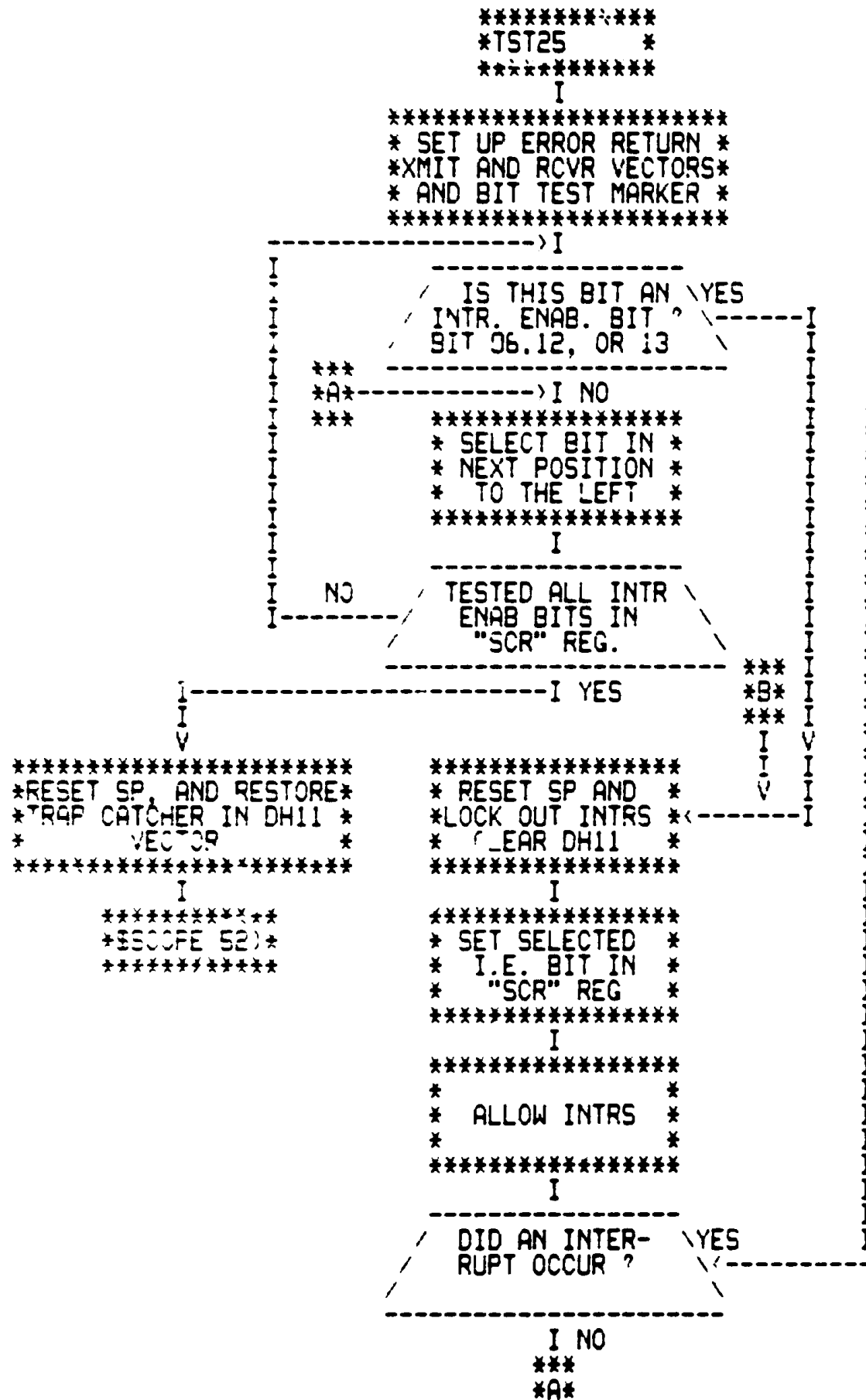


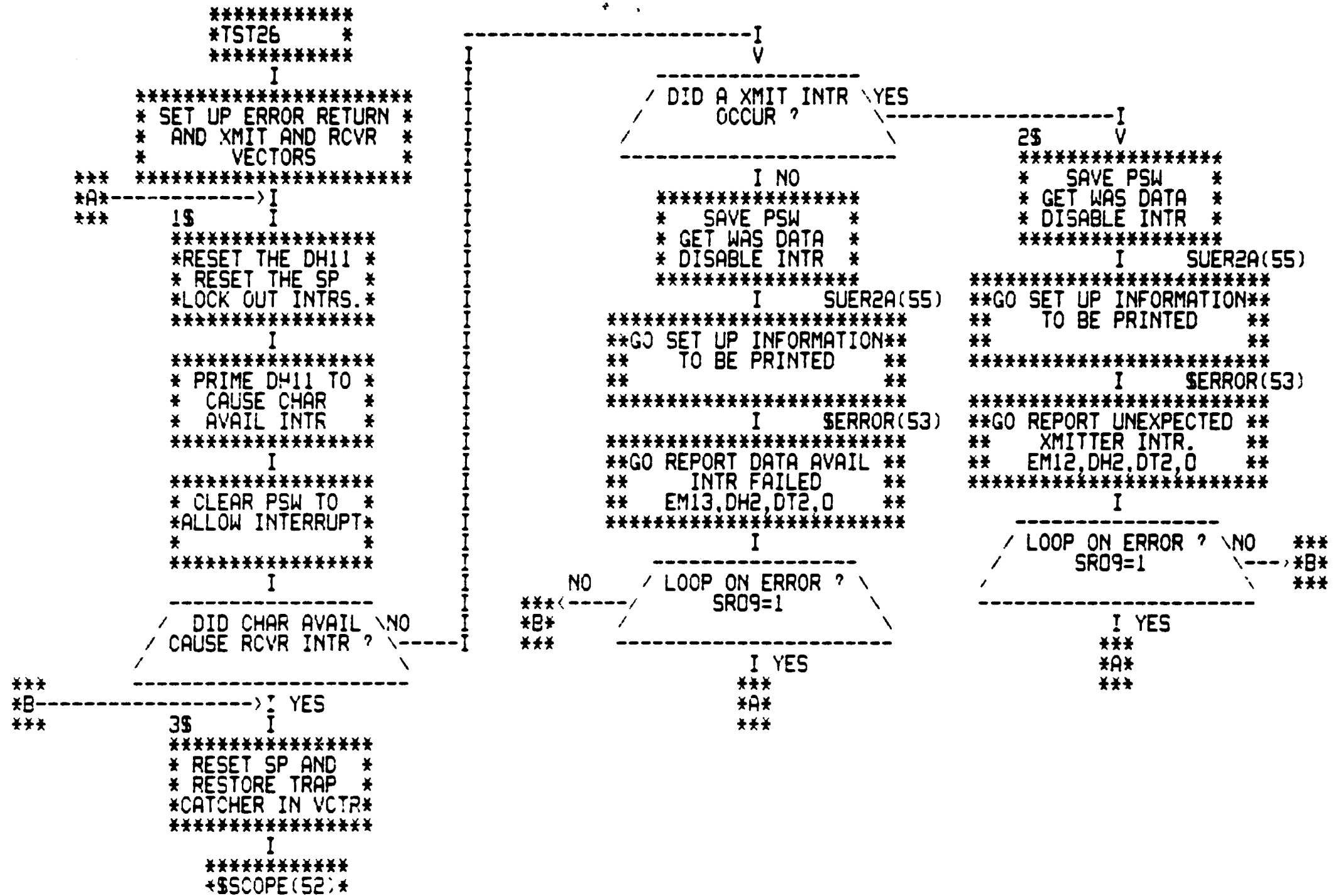


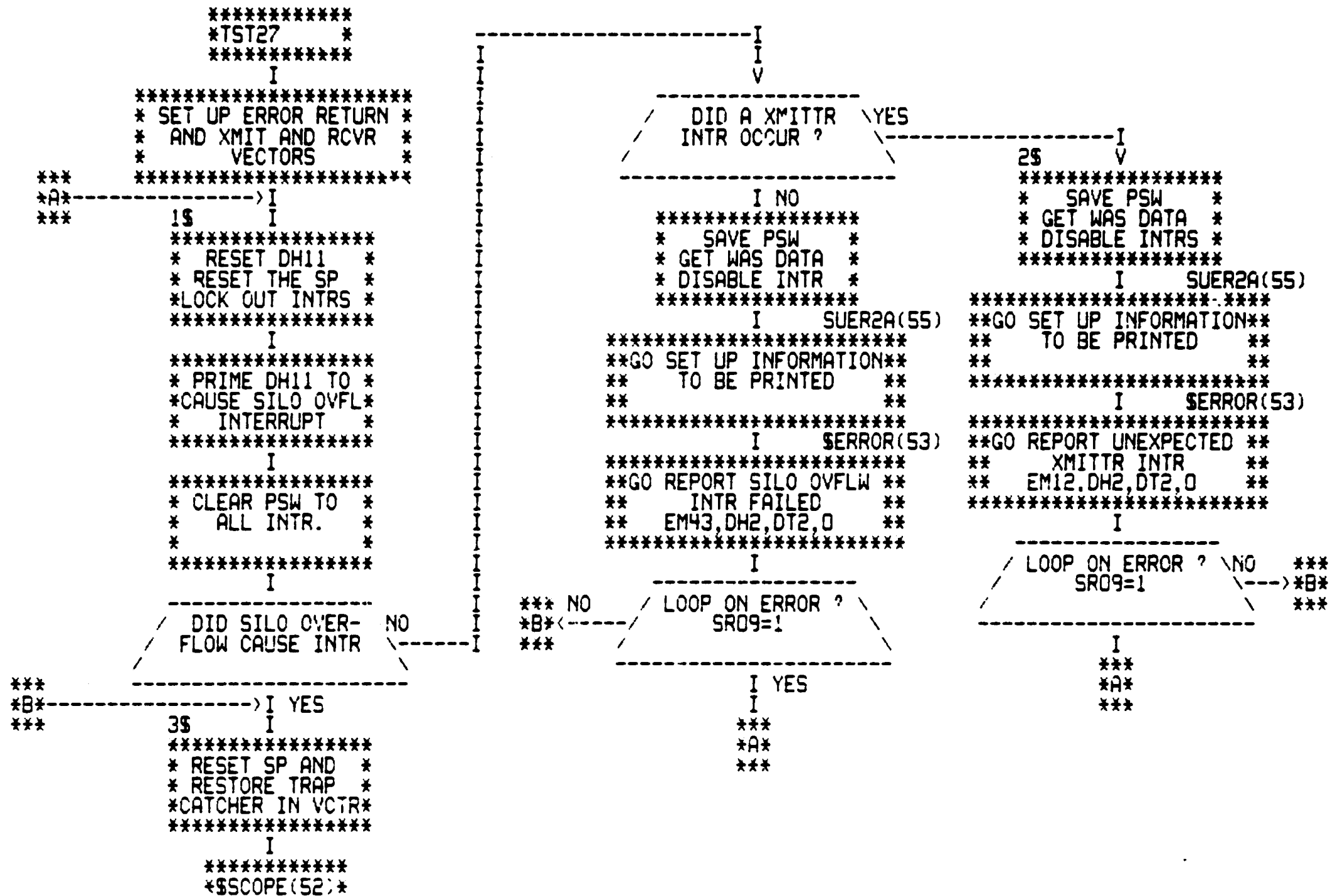
















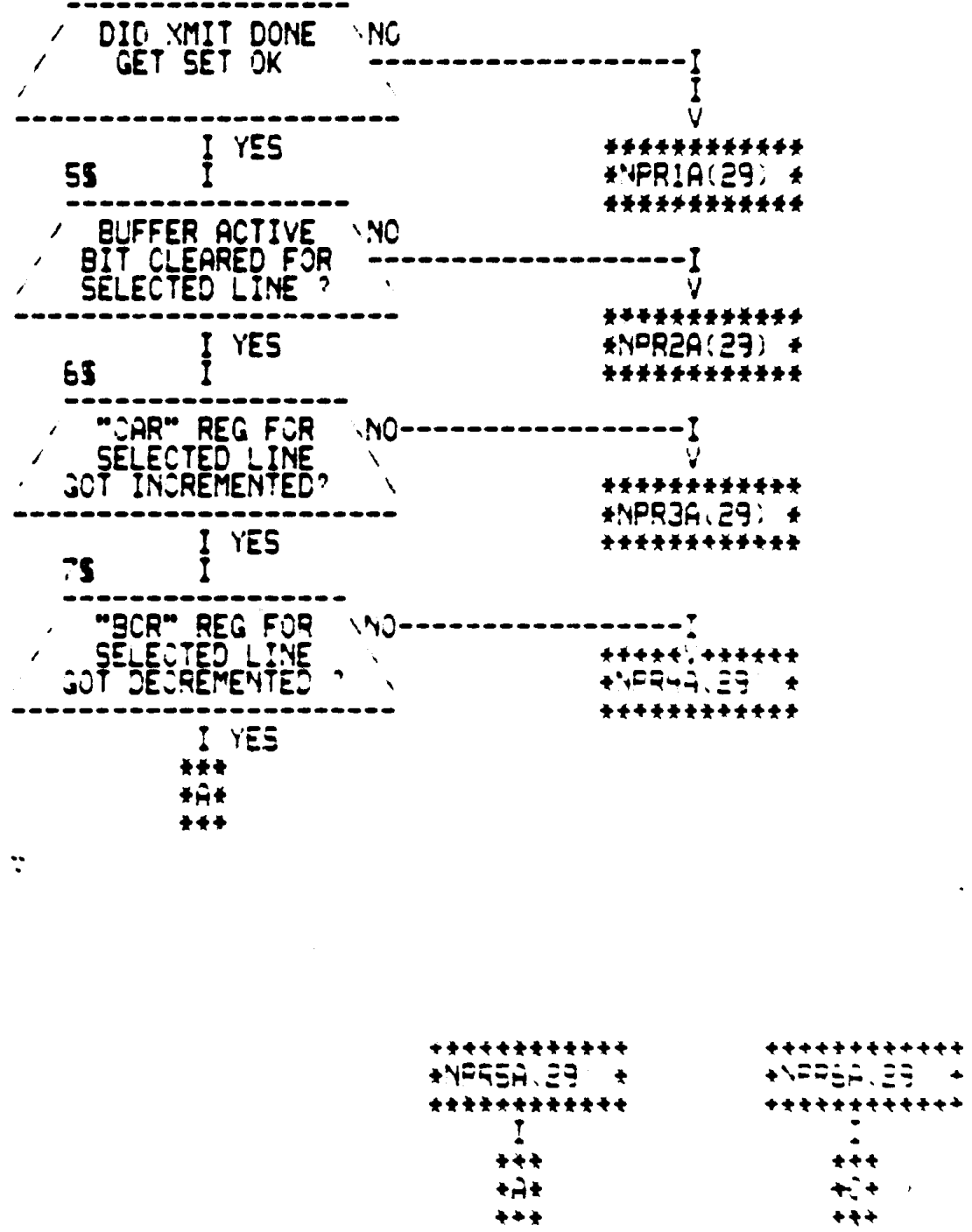


NOTE: \*\*\*  
COME HERE \*D\*  
ON XMIT \*\*\*  
INTERRUPT I

```

*****
*YST32 *
*****
I
*****
* SET UP ERROR RETURN *
* AND XMIT VECTOR *
*****
***
*****
I
3S I TIMEIT(59)
*****
** CALL TIMER **
*****
I
*****
DID TIMEOUT
OCCUR BEFORE INTR
ON SELECTED LINE
*****
I YES
*****
* SAVE ERROR PSW *
* GET WAS DATA *
*****
I SUER2A(55)
*****
**GO SET UP INFORMATION**
** TO BE PRINTED **
*****
I SUNUM(56)
*****
** GO SET UP LINE NO. **
** IN ERROR MESSAGE **
*****
I SERROR(53)
*****
** GO REPORT TIMEOUT **
** WAITING FOR XMIT DONE **
** EM15,DH2,DT2,0 **
*****
I
*****
LOOP ON ERROR ? YES ***
SRC9=1 ***
*****
I NO
*****
I 8S
*****
** CLEAR DH11 RESTORE *
** TRAP CATCHER IN VEC *
** TOR AND CLR PSW *
*****
I
*****
**SCOPE 52**

```



\*\*\*\*\*  
\*NPR1A(28) \*  
\*\*\*\*\*

\*\*\*\*\*  
\*NPR2A(28) \*  
\*\*\*\*\*

\*\*\*\*\*  
\*NPR3A(29) \*  
\*\*\*\*\*

\*\*\*\*\*  
\*NPR4A(28) \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\*SAVE ERROR PSW \*  
\* GET WAS DATA \*  
\* \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\*SAVE ERROR PSW \*  
\* GET WAS DATA \*  
\* \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\*SAVE ERROR PSW \*  
\* GET WAS DATA \*  
\* \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\*SAVE ERROR PSW \*  
\* GET WAS DATA \*  
\* \*  
\*\*\*\*\*

I SUER2A(55)

I SUER2A(55)

I SUER2A(55)

I SUER2A(55)

\*\*\*\*\*  
\*\*GO SET UP INFORMATION\*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\*GO SET UP INFORMATION\*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\*GO SET UP INFORMATION\*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\*GO SET UP INFORMATION\*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*\*  
\*\*\*\*\*

I 9\$

I 9\$

I 9\$

I 9\$

\*\*\*\*\*  
\*\* CALL SUBR TO SET UP \*\*  
\*\* LINE NO. \*\*  
\*\* \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\* CALL SUBR TO SET UP \*\*  
\*\* LINE NO. \*\*  
\*\* \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\* CALL SUBR TO SET UP \*\*  
\*\* LINE NO. \*\*  
\*\* \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\* CALL SUBR TO SET UP \*\*  
\*\* LINE NO. \*\*  
\*\* \*\*  
\*\*\*\*\*

I SERROR(53)

I SERROR(53)

I SERROR(53)

I SERROR(53)

\*\*\*\*\*  
\*\* GO REPORT XMIT DONE \*\*  
\*\* FAILED TO SET \*\*  
\*\* EM14,DH2,DT2,0 \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\* GO REPORT "BAR" \*\*  
\*\* REG ERROR \*\*  
\*\* EM14,DH2,DT2,0 \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\* GO REPORT "CAR" \*\*  
\*\* REG ERROR \*\*  
\*\* EM14,DH2,DT2,0 \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*\* GO REPORT "BCR" \*\*  
\*\* REG ERROR \*\*  
\*\* EM14,DH2,DT2,0 \*\*  
\*\*\*\*\*

-----  
LOOP ON ERROR ? \YES \*\*\*  
                  \---> \*E\*  
                  /---> \*\*\*  
SR09=1

-----  
LOOP ON ERROR ? \YES \*\*\*  
                  \---> \*E\*  
                  /---> \*\*\*  
SRC9=1

-----  
LOOP ON ERROR ? \YES \*\*\*  
                  \---> \*E\*  
                  /---> \*\*\*  
SR09=1

-----  
LOOP ON ERROR ? \YES \*\*\*  
                  \---> \*E\*  
                  /---> \*\*\*  
SR09=1

I NO

I NO

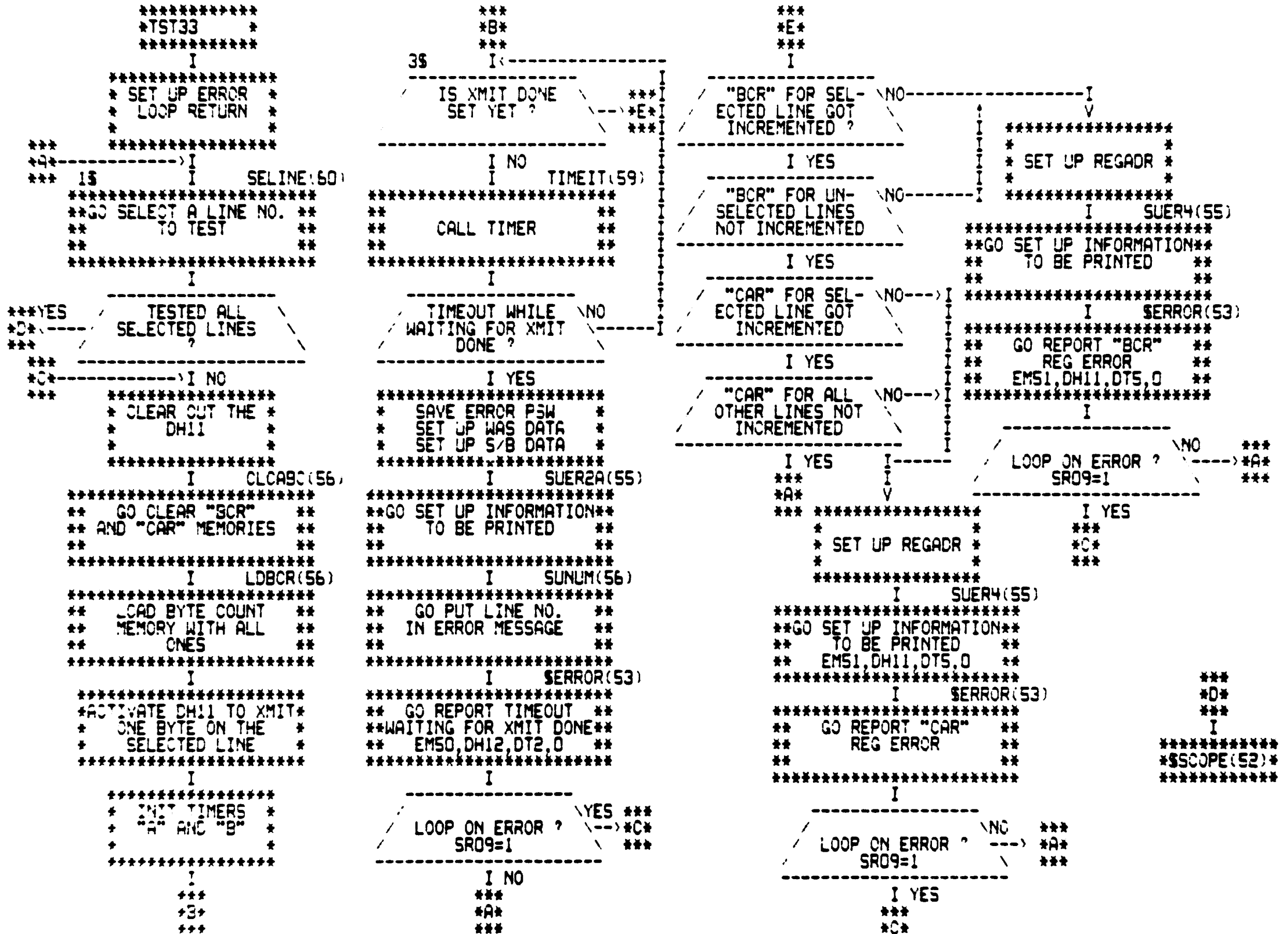
I NO

I NO

\*\*\*\*\*  
\*NPR5A(28) \*  
\*\*\*\*\*

\*\*\*  
\*E\*  
\*\*\*  
I  
\*\*\*\*\*  
\*NPR6A(28) \*

9\$                   SUNUM(56)  
\*\*\*\*\*  
\*\* GO SET UP LINE NO. \*\*  
\*\* IN ERROR MESSAGE \*\*  
\*\*



\*\*\*\*\*  
\*TST34 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SET UP ERROR \*  
\* RETURN AND RCVR \*  
\* VECTOR \*  
\*\*\*\*\*

\*\*\*  
\*B-----I  
\*\*\* I\$ I

\*\*\*\*\*  
\* LOCK OUT INTRs \*  
\* RESET SP AND \*  
\* CLEAR DH11 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SET SILO MAINT TO \*  
\* LOAD SILO AND ENAB \*  
\* CHAR AVAIL INTRs \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* CLEAR THE PSW \*  
\* TO ALLOW INTR \*  
\* \*  
\*\*\*\*\*  
2\$ I

-----I  
/ DID TIMEOUT \ YES  
/ OCCUR WHILE WAIT- \  
/ ING FOR INTR. \  
-----I

3\$ I NO

-----I  
/ DID SILO CONTAIN \ NO  
/ TEST PATTERN \  
/ 125252 ? \  
-----I

4\$ I YES

-----I  
/ DID SILO FILL \ NO  
/ COUNT = 1? \  
-----I

5\$ I YES  
\*\*\*\*\*  
\* RESET SP RESTORE \*  
\* TRAP CATCHER IN VECT \*  
\* OR, CLR PSW \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* \$SCOPE(52) \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SAVE ERROR PSW \*  
\* SET UP WAS DATA \*  
\* \*  
\*\*\*\*\*

I SUER2A(55)

\*\*\*\*\*  
\*\* GO SET UP INFORMATION \*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*  
\*\*\*\*\*

I \$ERROR(53)

\*\*\*\*\*  
\*\* GO REPORT CHAR AVAIL \*\*  
\*\* TIMEOUT \*\*  
\*\* EM13, DH2, DT2, 0 \*\*  
\*\*\*\*\*

-----I  
/ LOOP ON ERROR \ NO \*\*\*  
/ SR09=1 \ --> \*A\*  
-----I

I YES  
\*\*\*  
\*B\*  
\*\*\*

I  
\*\*\*\*\*  
\* SAVE ERROR PSW \*  
\* SET UP REGADR \*  
\* \*  
\*\*\*\*\*

I SUER2A(55)

\*\*\*\*\*  
\*\* GO SET JP INFORMATION \*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*  
\*\*\*\*\*

I \$ERROR(53)

\*\*\*\*\*  
\*\* GO REPORT SILO \*\*  
\*\* DATA ERROR \*\*  
\*\* EM52, DH2, DT2, 0 \*\*  
\*\*\*\*\*

-----I  
/ LOOP ON ERROR \ NO \*\*\*  
/ SR09=1 \ --> \*A\*  
-----I

I YES  
\*\*\*  
\*B\*  
\*\*\*

I  
\*\*\*\*\*  
\* SAVE ERROR PSW \*  
\* SET UP REGADR \*  
\* \*  
\*\*\*\*\*

I SUER2A(55)

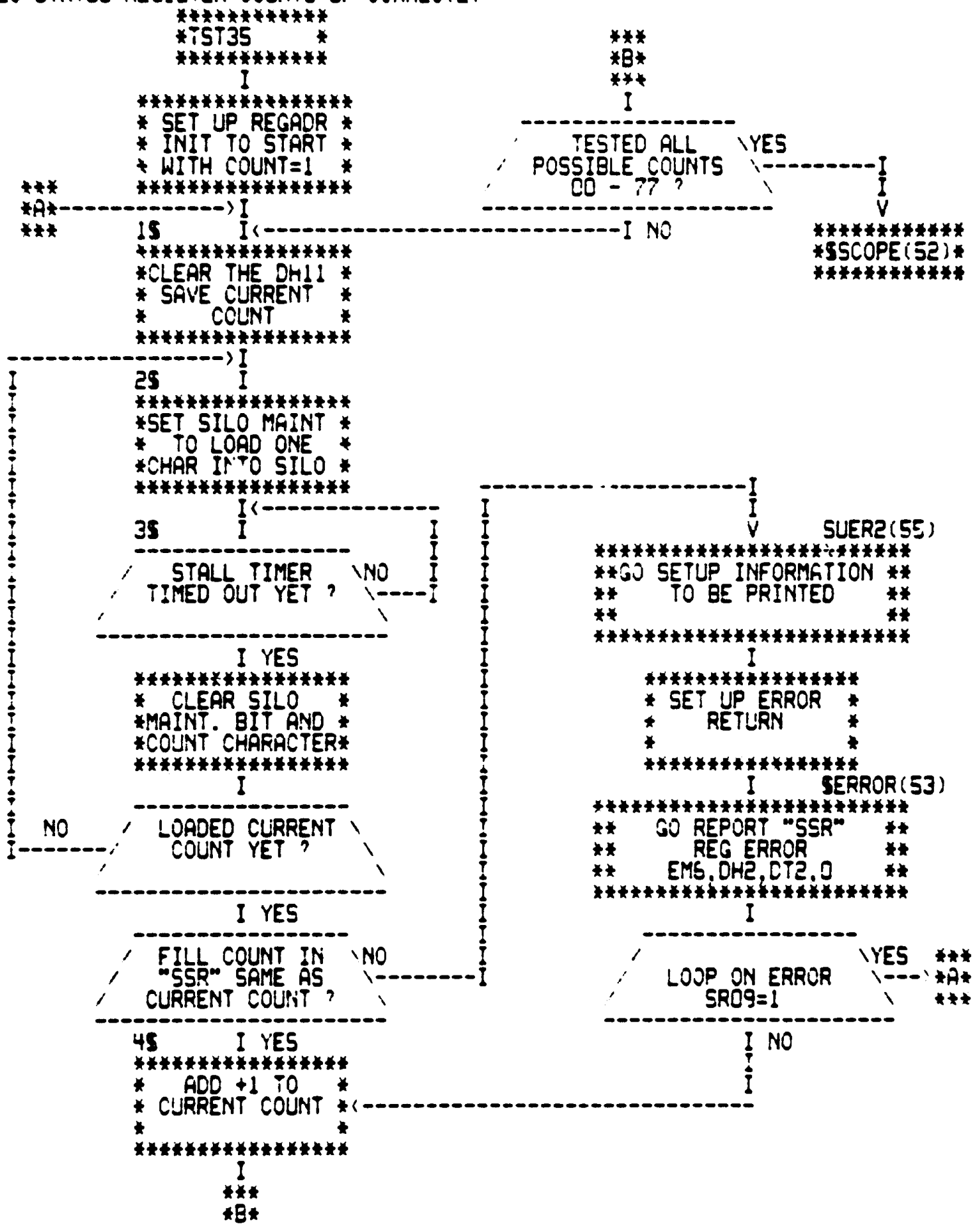
\*\*\*\*\*  
\*\* GO SET UP INFORMATION \*\*  
\*\* TO BE PRINTED \*\*  
\*\* \*  
\*\*\*\*\*

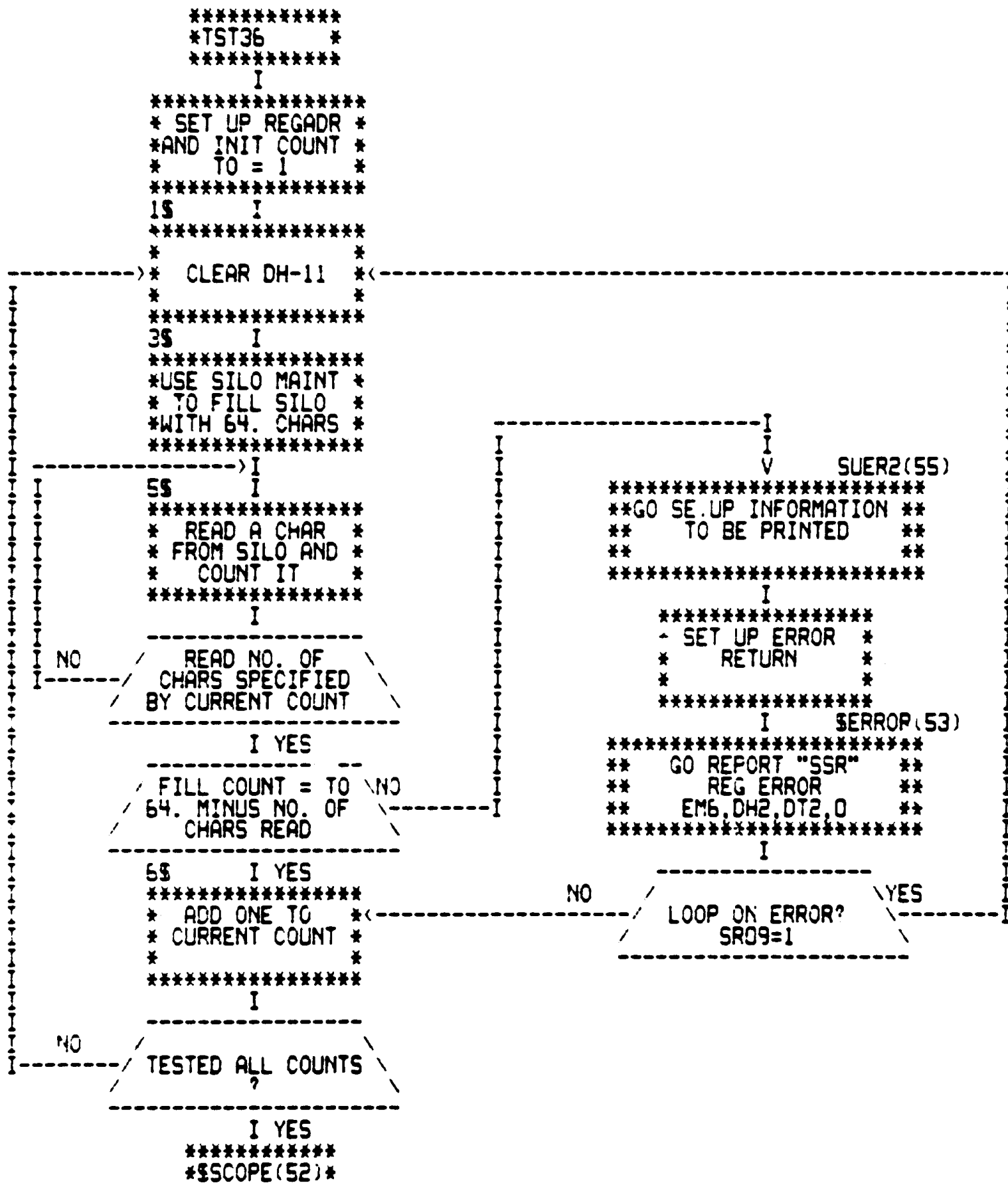
I \$ERROR(53)

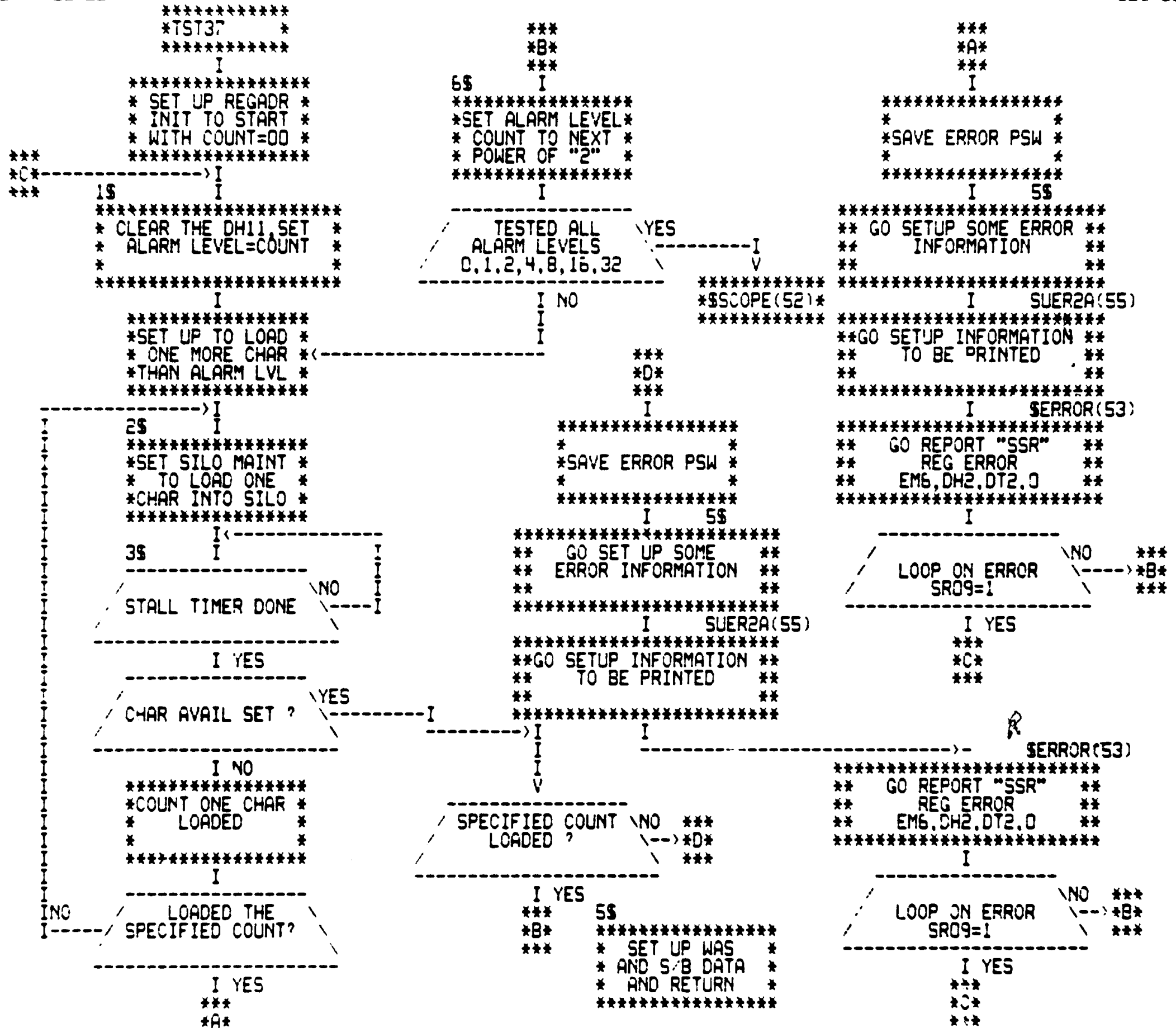
\*\*\*\*\*  
\*\* GO REPORT SILO \*\*  
\*\* FILL COUNT ERROR \*\*  
\*\* EM6, DH2, DT2, 0 \*\*  
\*\*\*\*\*

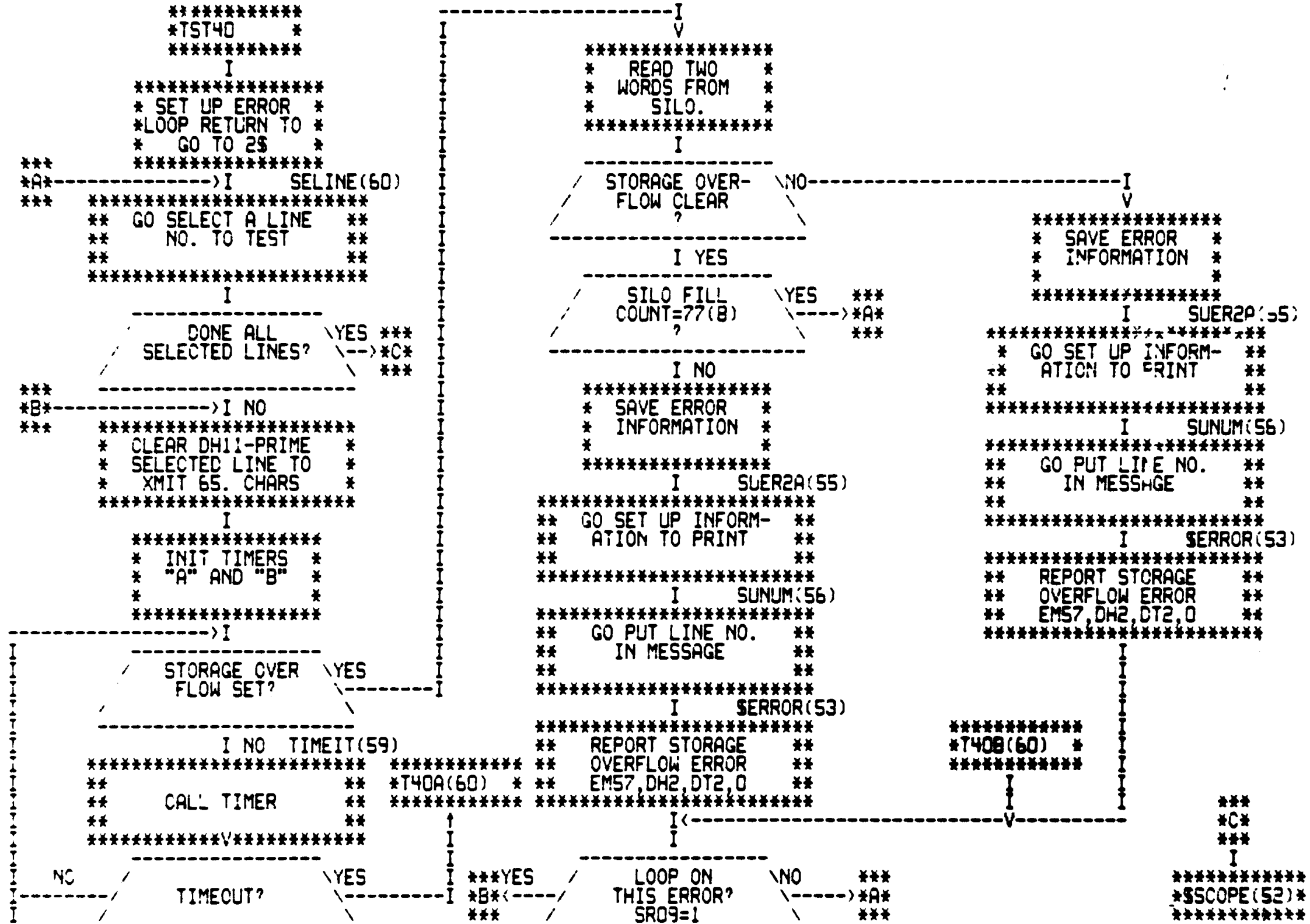
-----I  
/ LOOP ON ERROR \ NO \*\*\*  
/ SR09=1 \ --> \*A\*  
-----I

I YES  
\*\*\*  
\*B\*  
\*\*\*

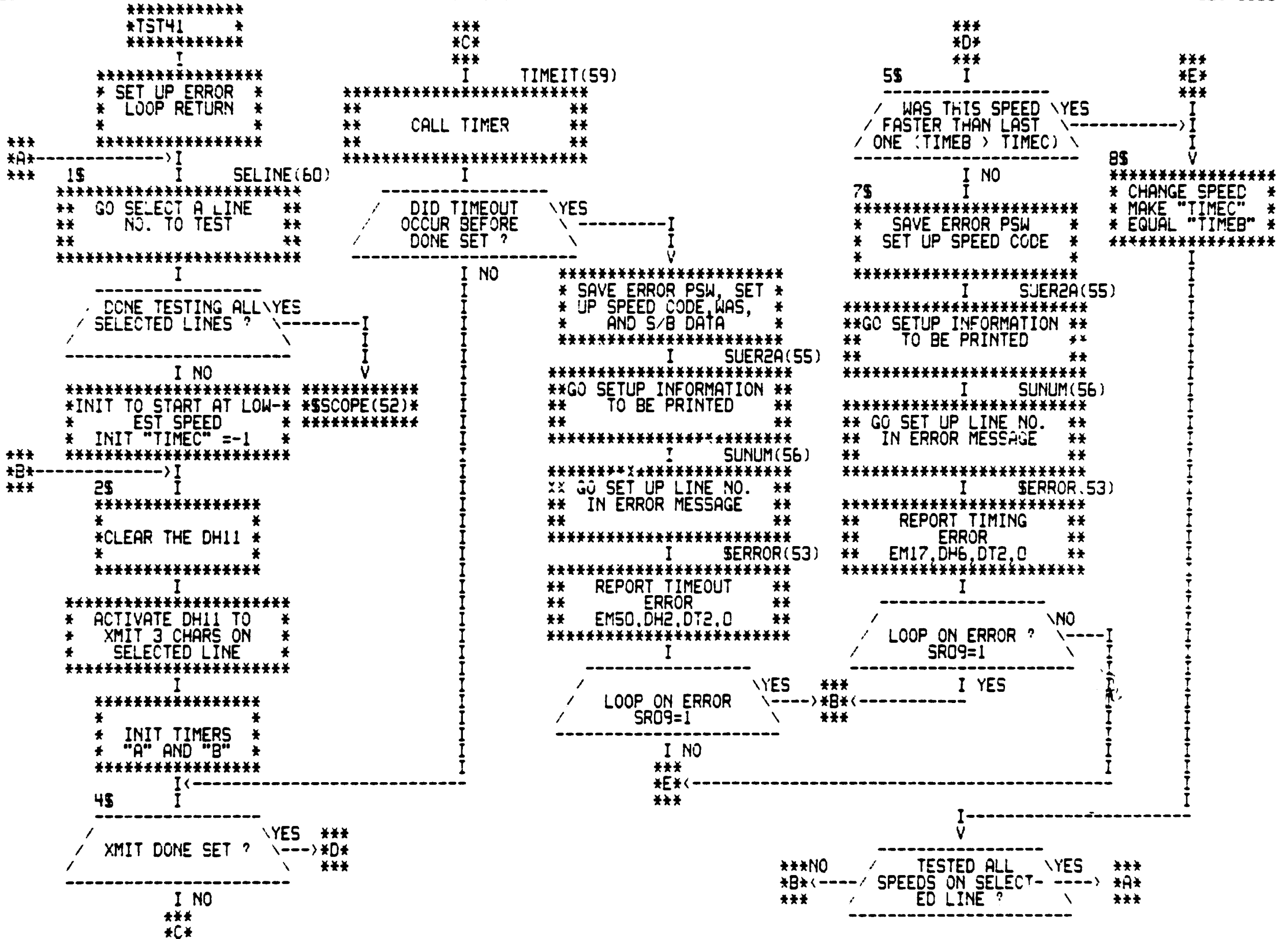


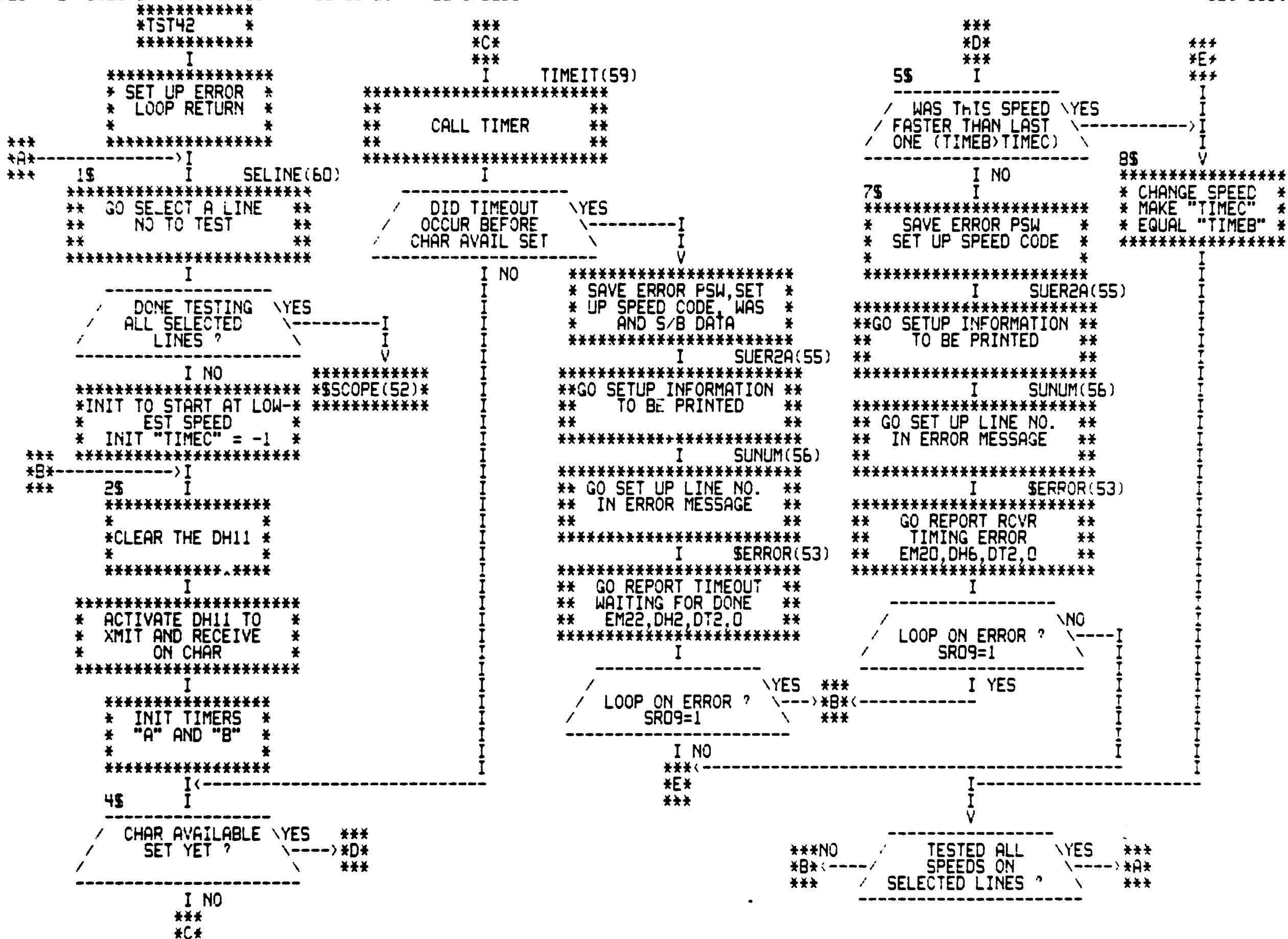




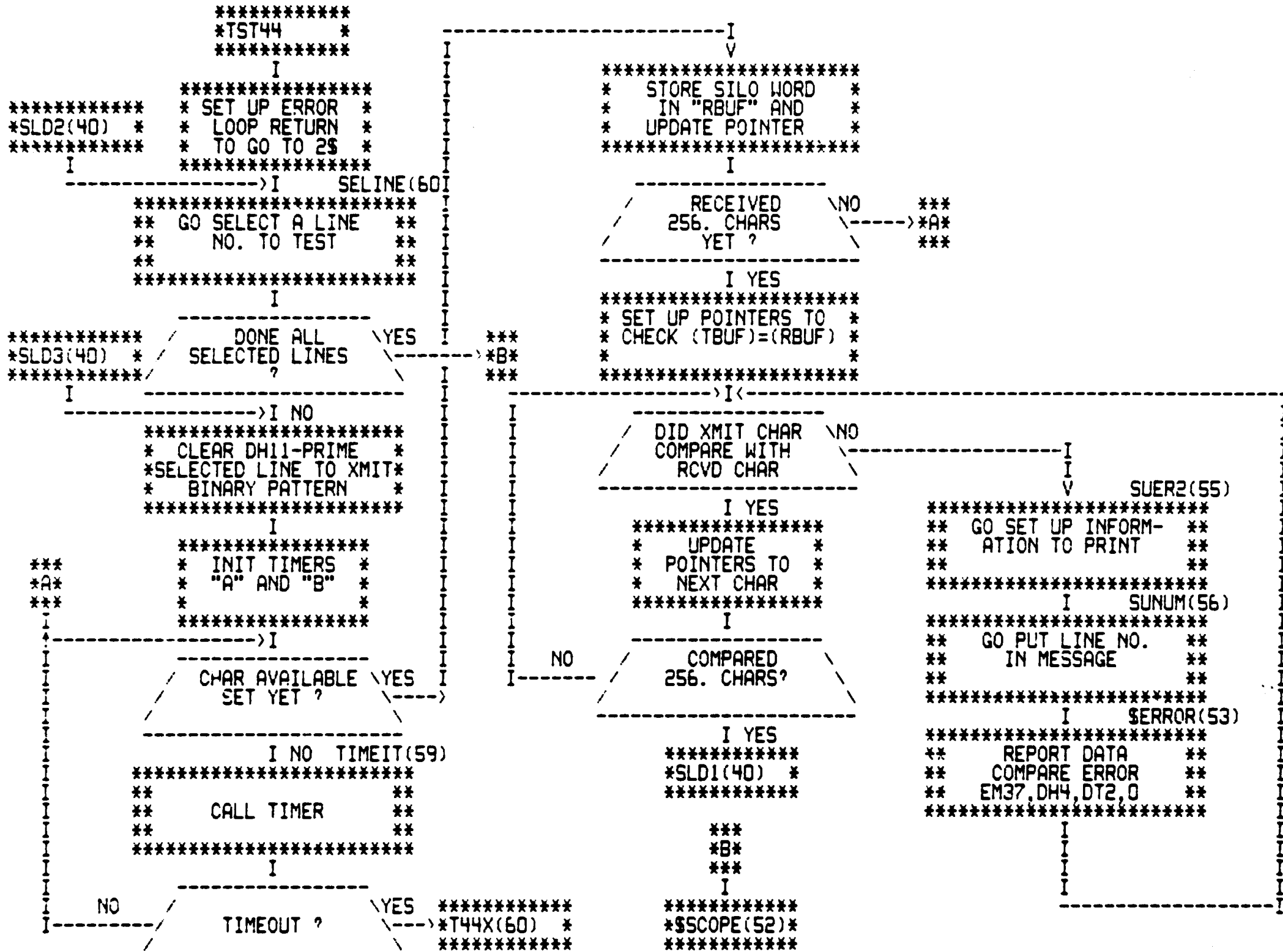


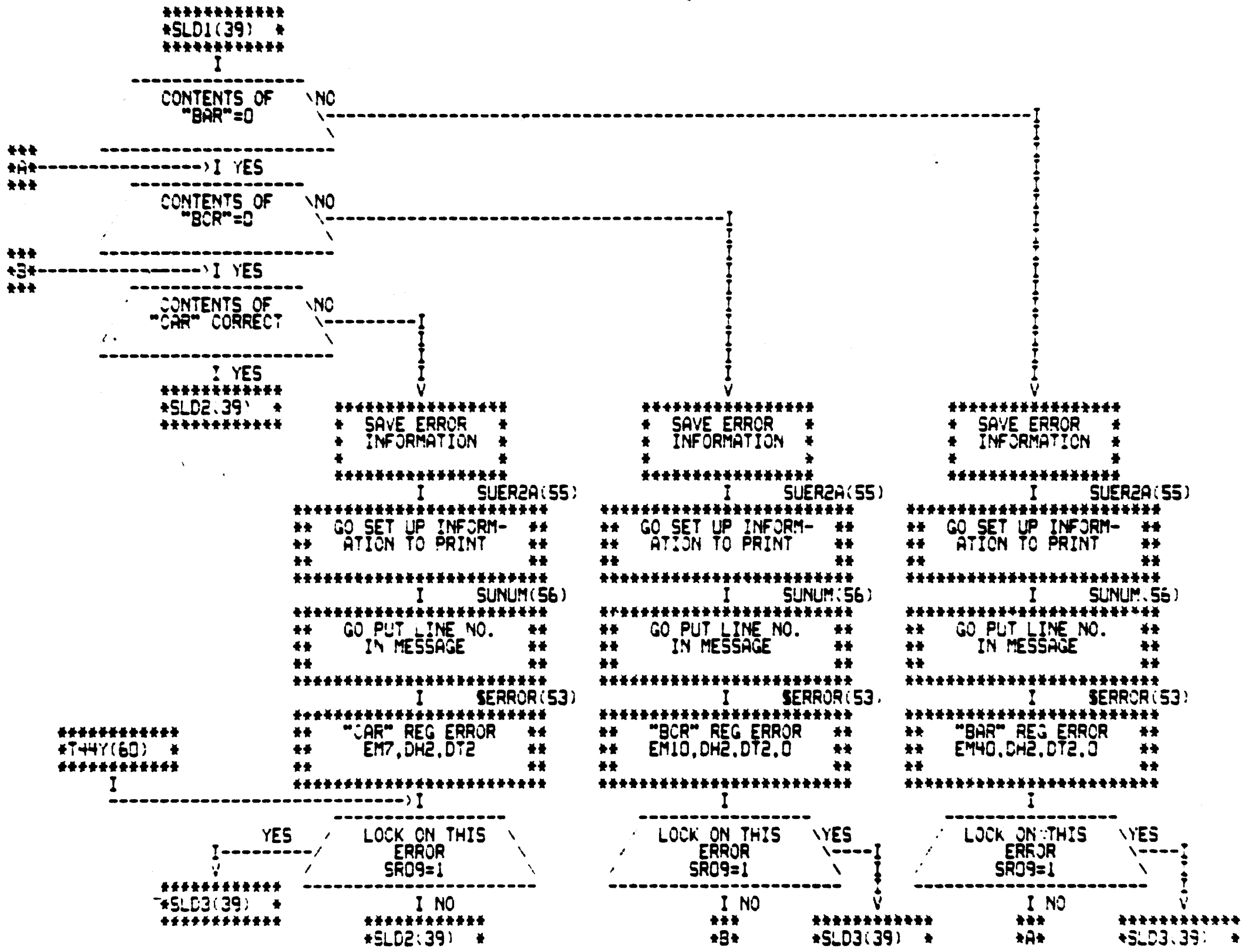












```

*****
* TST45 *
*****
I
*****
* SET UP ERROR *
* LOOP RETURN *
*****

```

```

***
*B*
***
I
*****
* SAVE ERROR PSW SET *
* UP WAS, S B DATA AND *
* REGADR *
*****

```

```

***
*C*
***
45 I
-----
CORRECT DATA YES ***
RECEIVED ? ----- **A**

```

```

***
15 I SELINE(60)
*****
**GO SELECT A LINE NO. **
** TO TEST **
*****

```

```

I SUER2A(55)
*****
**GO SETUP INFORMATION **
** TO BE PRINTED **
*****

```

```

I NO
*****
* SAVE ERROR PSW *
* SET UP REGADR *
*****

```

```

I
-----
TESTED ALL SEL- YES
ECTED LINES ? -----

```

```

I SUNUM(56)
*****
** GO SET UP LINE NO. **
** IN ERROR MESSAGE **
*****

```

```

I SUER2A(55)
*****
**GO SETUP INFORMATION **
** TO BE PRINTED **
*****

```

```

***
25 I
*****
**SCOPE(52)**
**ACTIVATE DM11 TO XFER**
** ONE CHAR WITH "ODD" *
** PARITY SELECTED *
*****

```

```

I SERROR(53)
*****
** GO REPORT DATA **
** AVAILABLE TIMEOUT **
** EM22,DM2,DT2,0 **
*****

```

```

I SUNUM(56)
*****
** GO SET UP LINE NO. **
** IN ERROR MESSAGE **
** EM33,DM2,DT2,0 **
*****

```

```

I
*****
* INIT TIMERS *
* "A" AND "B" *
*****

```

```

*** YES
**D*----- LOOP ON ERROR ?
*** SRO9=1
-----

```

```

I SERROR(53)
*****
** GO REPORT PARITY **
** DATA ERROR **
*****

```

```

35 I
-----
CHAR AVAIL SET YES ***
YE? ----- **C**

```

```

*** YES
**D*----- LOOP ON ERROR ?
*** SRO9=1
-----
I NO
***
**A**
***

```

```

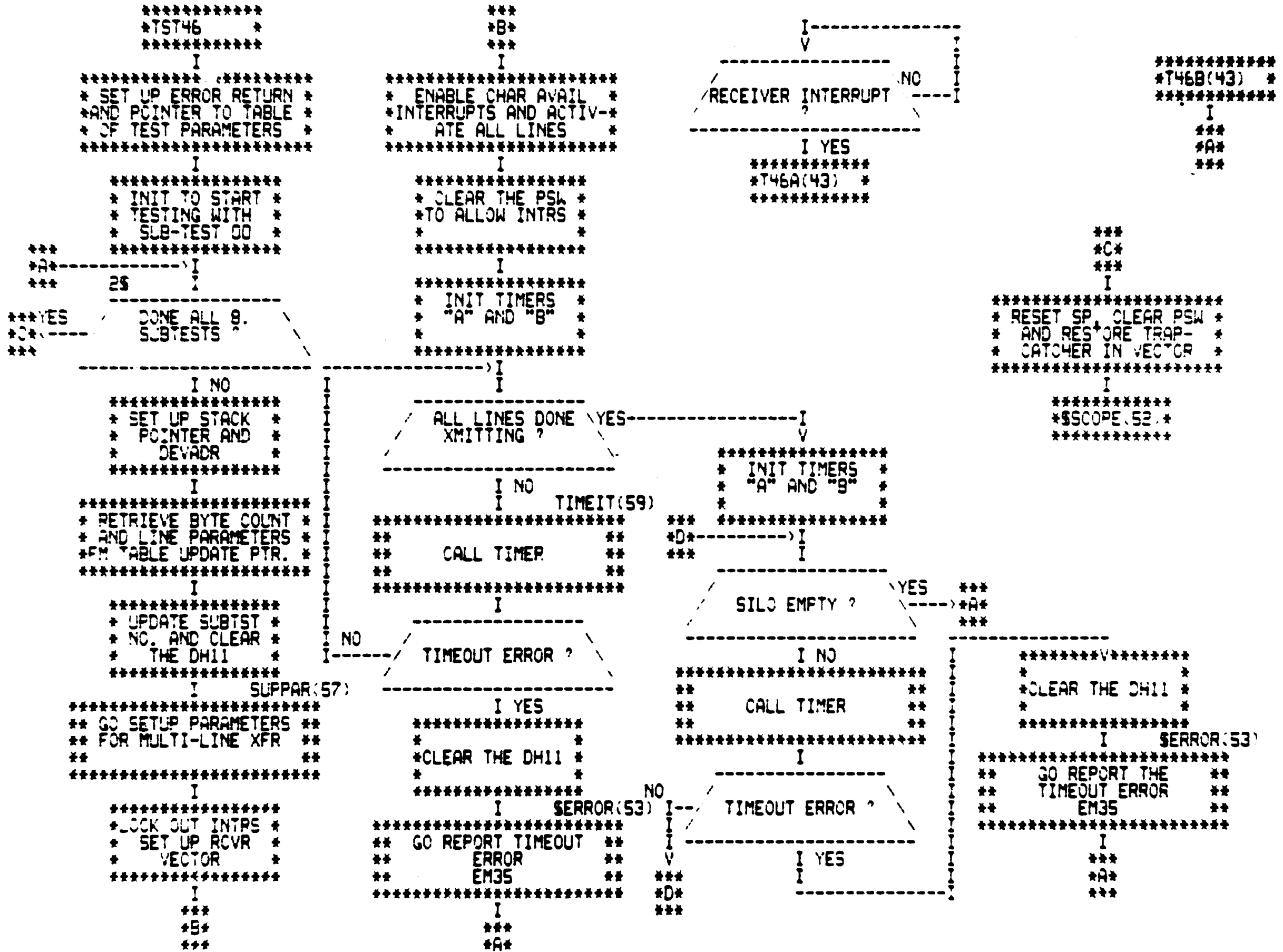
I NO TIMEIT(59)
*****
** CALL TIMER **
*****

```

```

I
-----
CHAR AVAILABLE
TIMEOUT ?
-----
I YES
***
**B*

```



```

*****
*T46A(42) *
*****
I
-----
/ WAS CHAR AVAIL- \ NO
/ ABLE SET ? \
-----
I YES
-----
***YES
*B* \----- SILO OVERFLOW
***
-----
I NO
*****
* GET THE DATA *
* FROM THE SILO *
* *
*****
I
*****
*INDEX PARITY TABLE TO*
* GET DATA FOR THIS *
* LINE *
*****
I
-----
/ WAS RECEIVED \ NO
/ DATA SAME AS THE \
/ TABLE DATA ? \
-----
I YES
*****
* UPDATE TABLE DATA *
* FOR THIS LINE *
* CHECK FOR LINE DONE *
*****
I
-----
/ RECEIVED ALL \ YES
/ CHARACTERS FOR \
/ THIS LINE ? \
-----
I NO
-----
I
-----
*****
**RTI **

```

```

-----
I
*****
* CLEAR OUT *
* THE DH11 *
* *
*****
I SERROR(53)
*****
** REPORT RCVR FALSE **
** INTERRUPT ERROR **
** EM41,DH5,DT4,0 **
*****
I
*****
*T46B(42) *
*****
-----
I
*****
* SAVE PSW *
* CLEAR DH11 *
* *
*****
I
*****
* SAVE ERROR *
* INFORMATION *
* *
*****
I SUER2A(55)
*****
** SET UP INFORMATION **
** TO BE PRINTED **
*****
I SUNUM(56)
*****
** PUT LINE NO. **
** IN ERROR MSG **
*****
I
-----
I NO
*****
* CLEAR LINE *
* ACTIVE BIT FOR *
* THIS LINE *
*****
I
-----

```

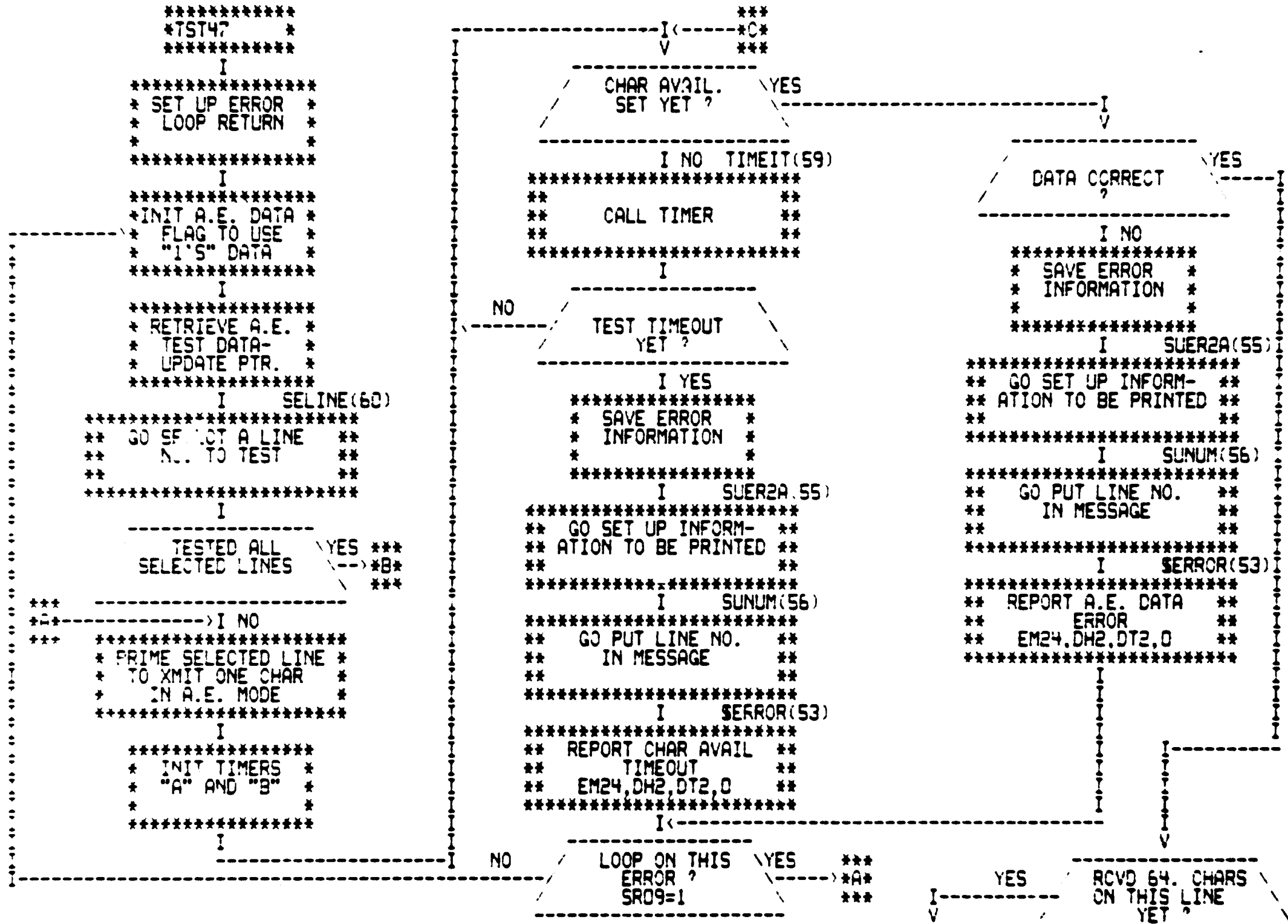
```

***
*B*
***
I
*****
* CLEAR OUT *
* THE DH11 *
* *
*****
I SERROR(53)
*****
** REPORT THE SILO **
** OVERFLOW ERROR **
** EM42,DH5,DT4,0 **
*****
I
*****
*T46B(42) *
*****
-----
I
*****
I SUNUM(56)
*****
** PUT SUB-TEST NO. **
** IN ERROR MSG **
** *
*****
I SERROR(53)
*****
** REPORT PARITY DATA **
** ERROR **
** EM34,DH4,DT2,0 **
*****
I
*****
*T46B(42) *
*****
-----

```

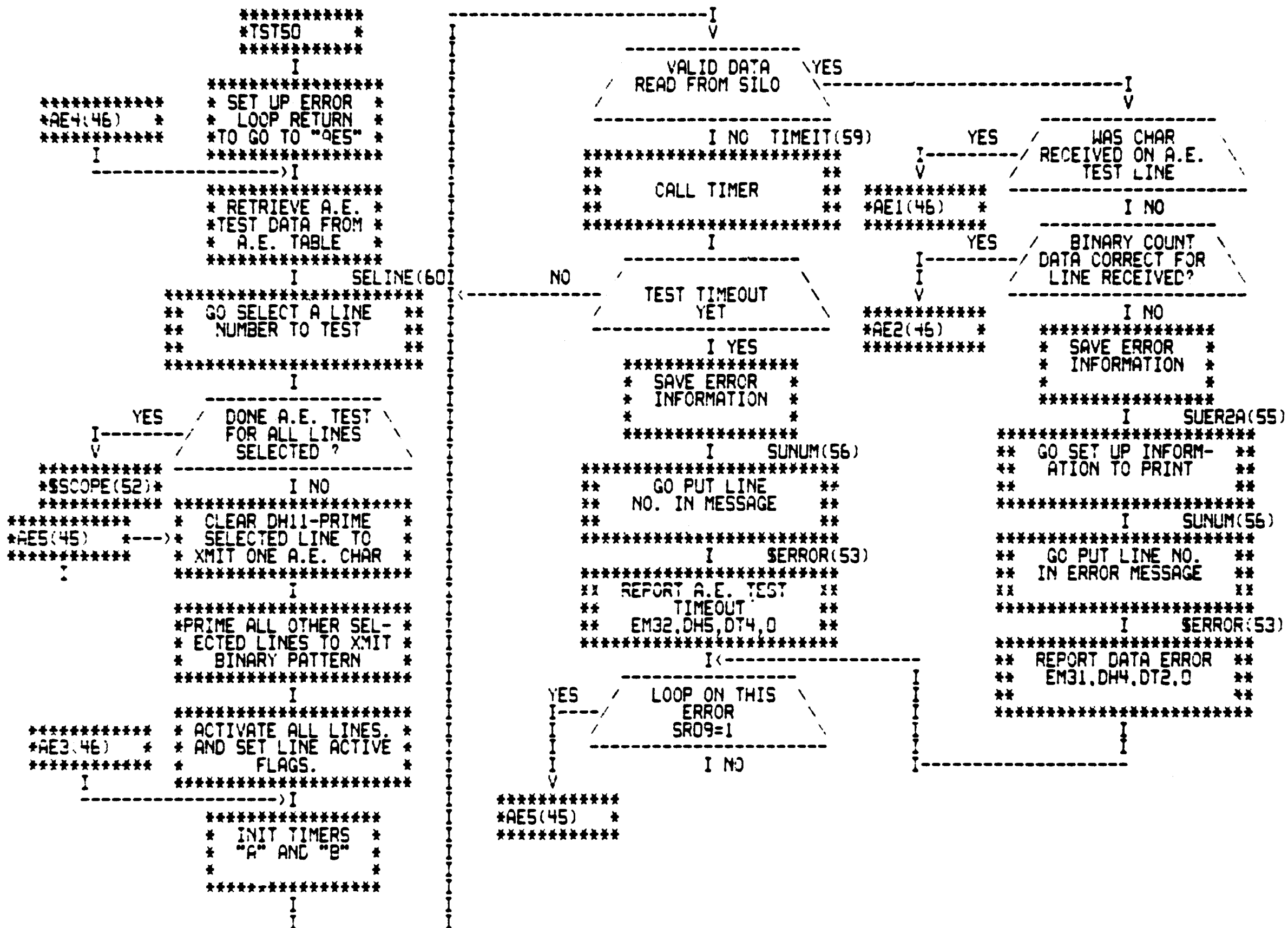
NOTE WHEN THE "RTI" IS EXECUTED ROUTINE RETURNS TO XMIT DONE

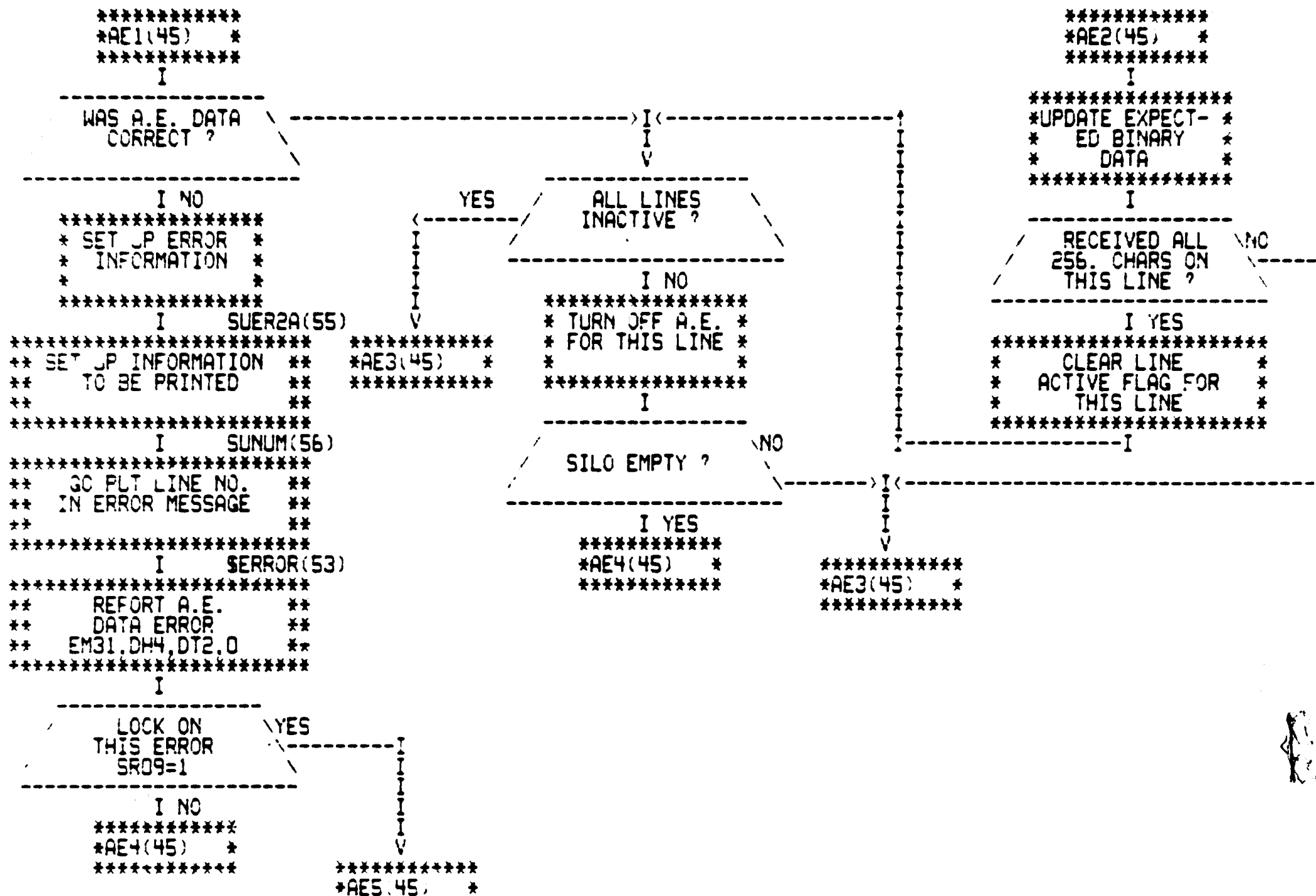


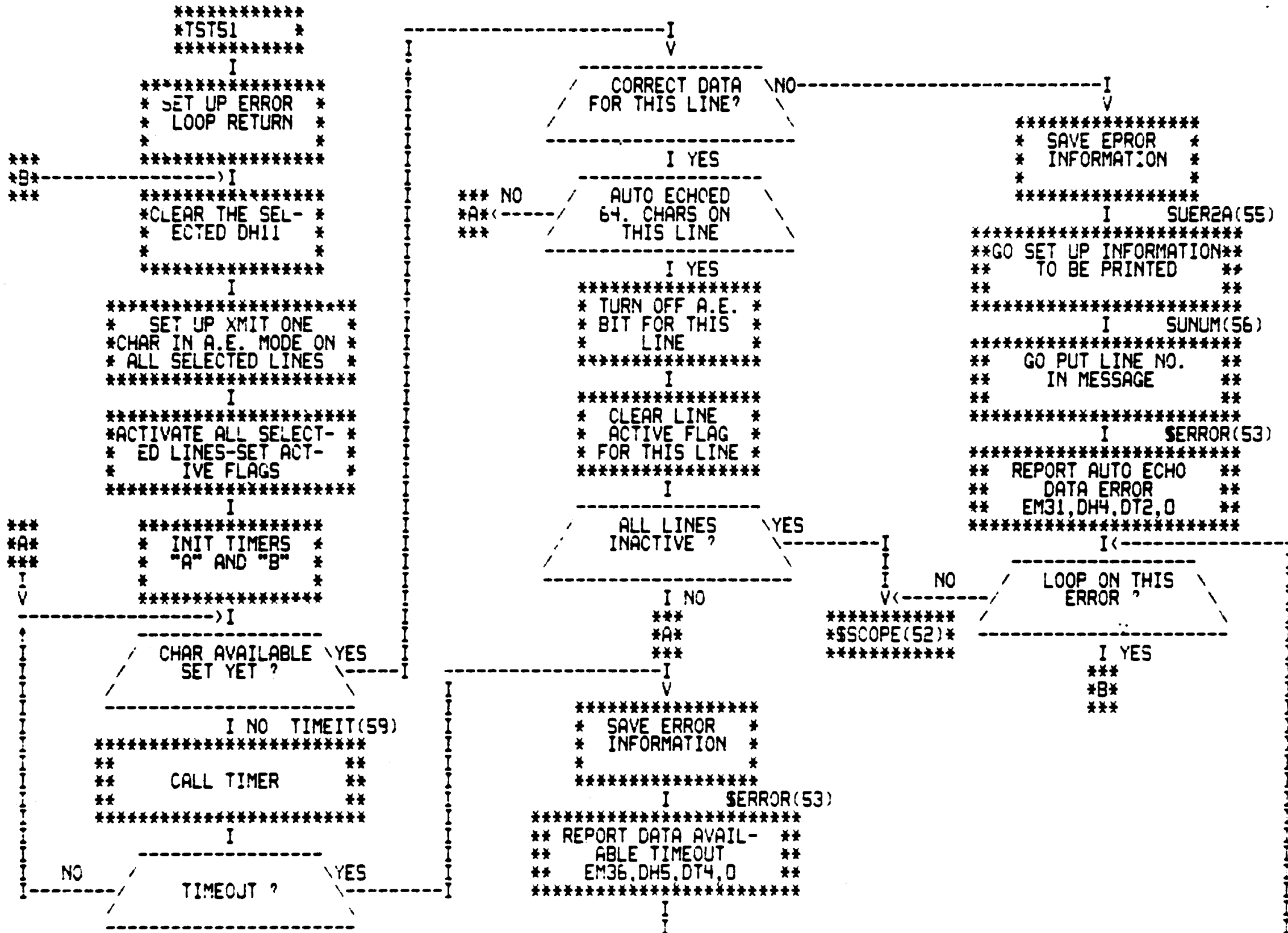


\*\*\*  
 \*B\*  
 \*\*\* NOTE: THIS TEST REPEATED FOR  
 I BOTH ALL (1'S) AND ALL (0'S) TEST  
 \*\*\*\*\* DATA - THEN EXITS TO NEXT TEST  
 \*\$SCOPE(52)\* VIA "SCOPE"

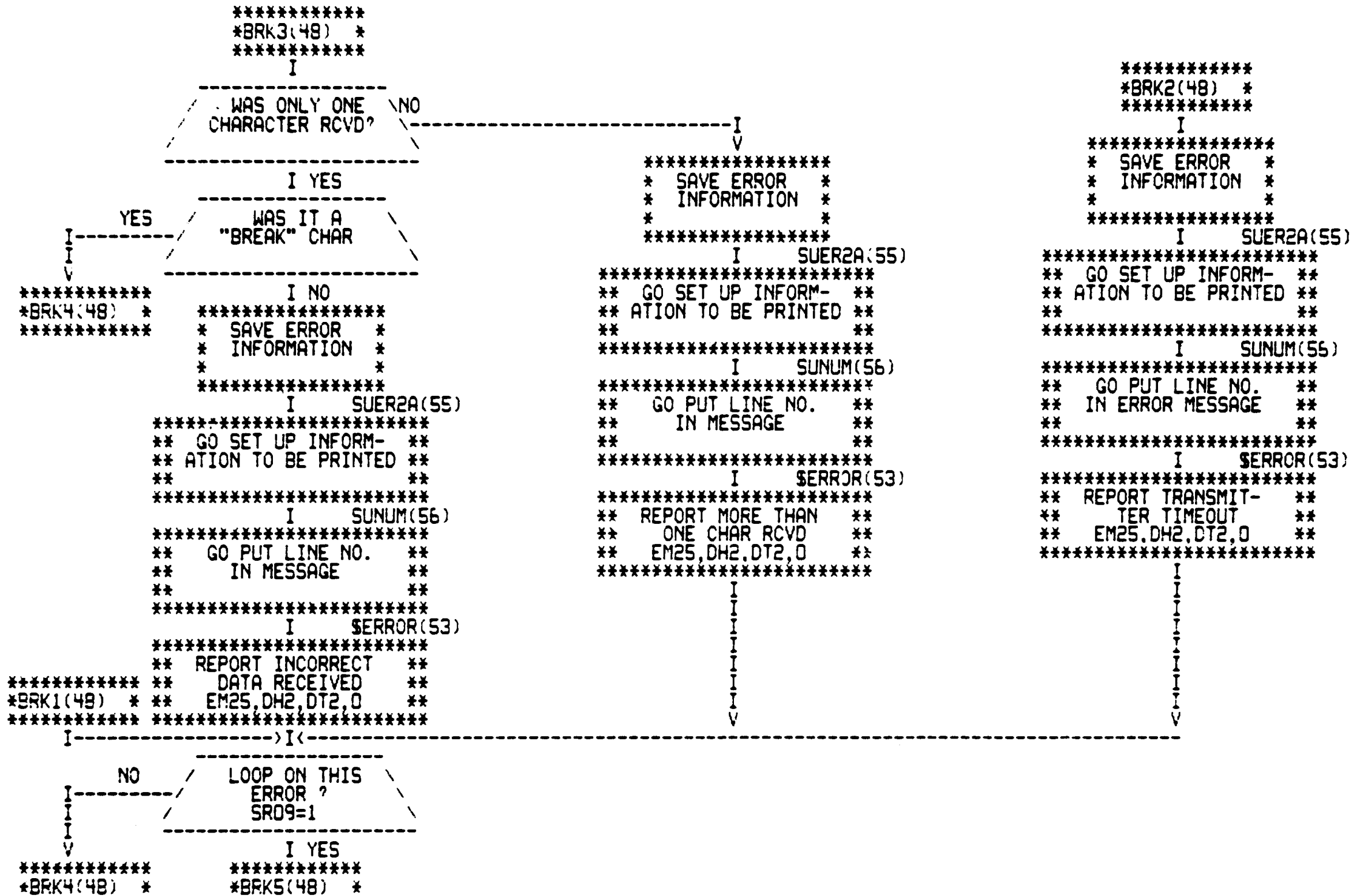
\*\*\*\*\*  
 \* DISABLE AUTO \* I NO  
 \* ECHO MODE \* \*\*\*  
 \* \*-----\* \*C\*  
 \*\*\*\*\* \*\*\*







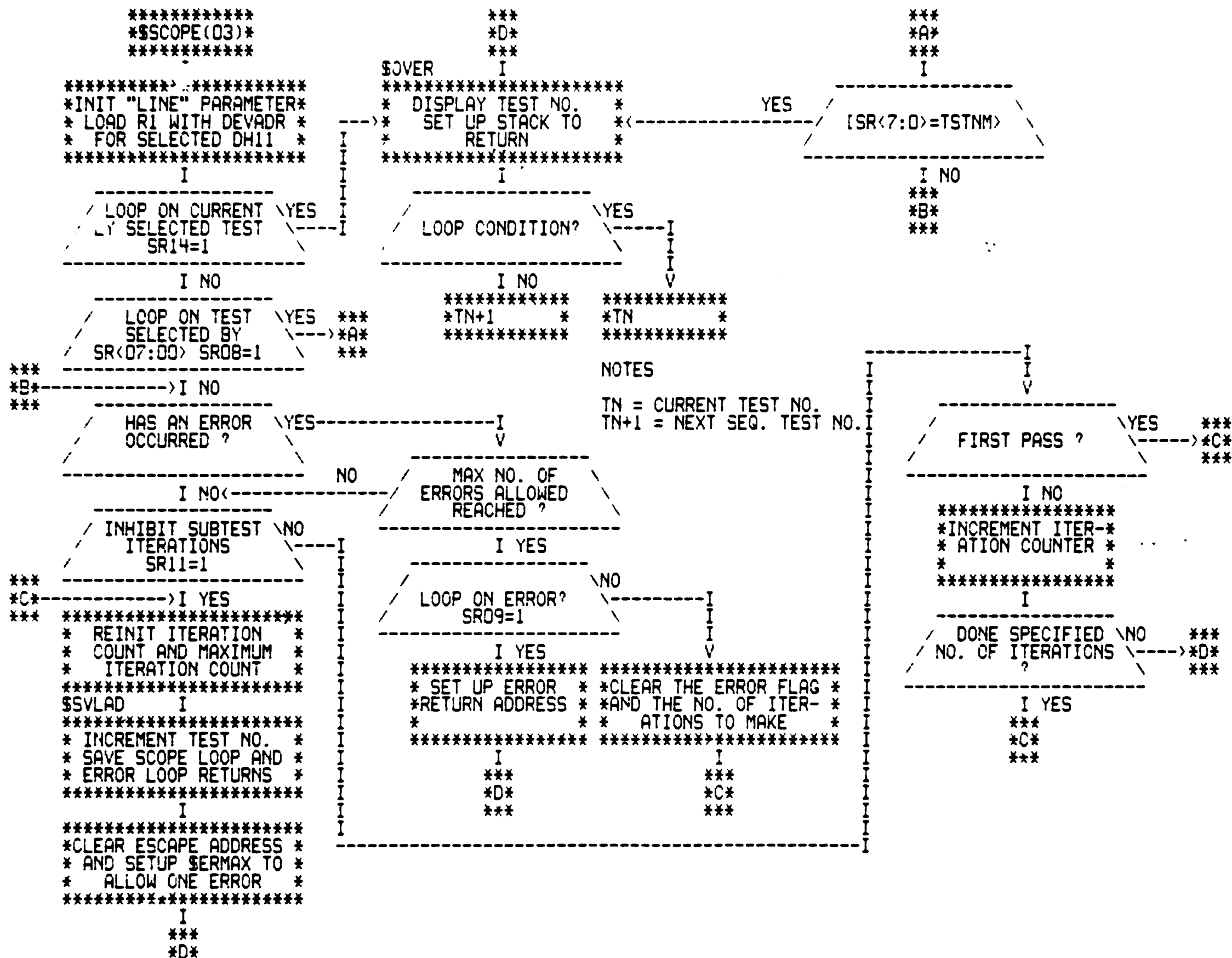










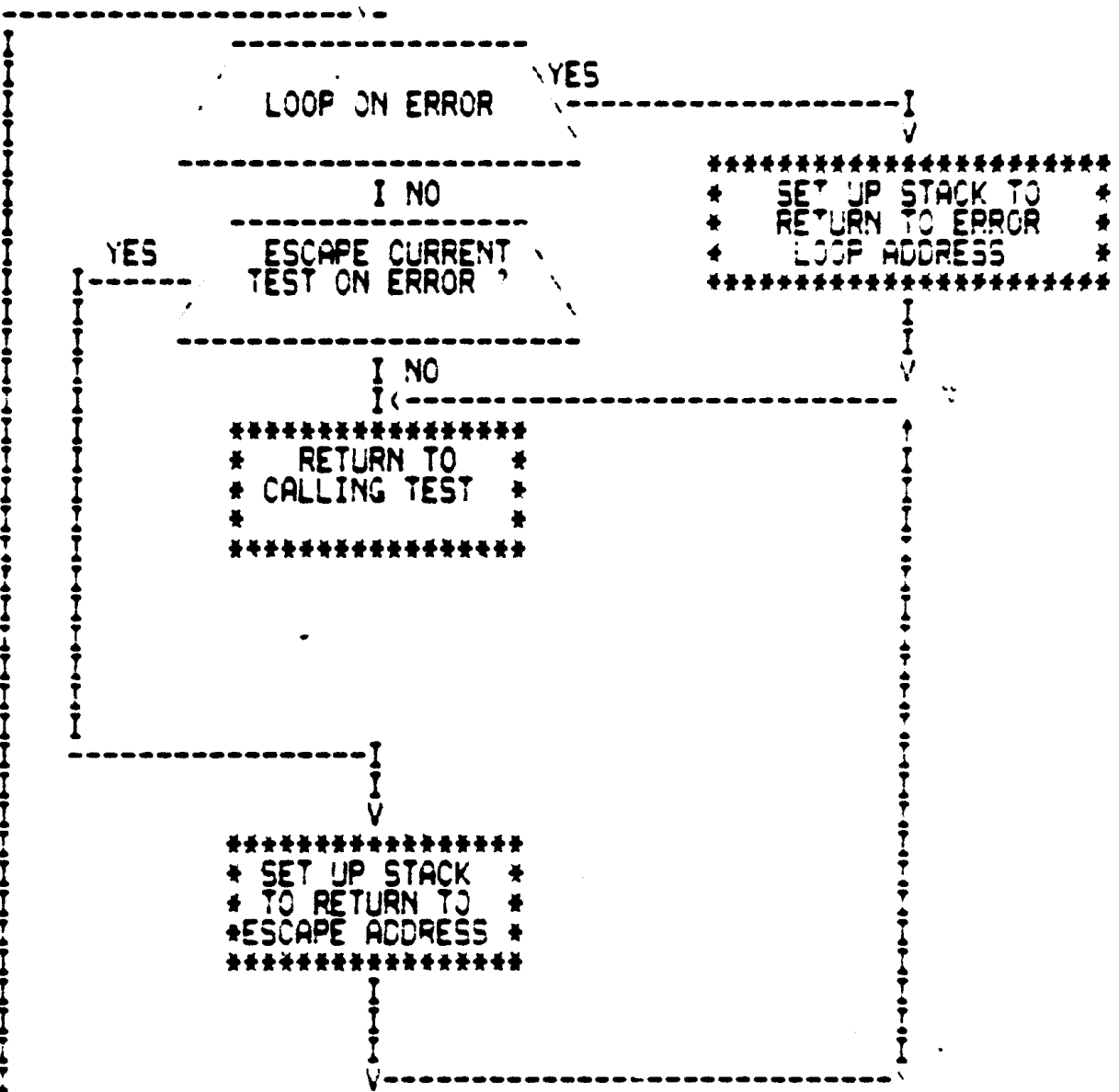


NOTES  
 TN = CURRENT TEST NO.  
 TN+1 = NEXT SEQ. TEST NO.

```

*****
*ERROR*
*****
I
*****
* INCREMENT THE *
* ERROR FLAG *
*****
DID ERROR FLAG YES
GO TO ZERO
I
I NO
*****
* DISPLAY TEST NO. *
* INCREMENT ERROR COUNT *
* GET ERROR PC *
*****
I
*****
* CORRECT ERROR PC. GET *
* ERROR TRAP INSTR. *
* SAVE ERROR ITEM CODE *
*****
I
YES INHIBIT ERROR
TYPEOUTS ?
SR13=1
I NO
SERTYP
*****
** GO TYPE THE ERROR **
** MESSAGE (SERTYP) **
**
*****
I
*****
** GO TYPE A CARRIAGE **
** RETURN LINE FEED **
**
*****
I
HALT ON ERROR ? NO
SR15=1
I YES
*****
**HALT**

```



```

*****
*SET L *
*****
I
*****
* SET UP $TMP6 *
* TO A 20(8) TO *
* COUNT 16. LINES*
*****
I
*****
* INIT R2 TO INDEX *
* READ BUFFER TEST *
* DATA TABLE *
*****
I
*****
* INIT R3 TO SET UP *
* VALID DATA BIT + *
* LINE NO. IN TABLE *
*****
I
*****
* INIT R4 TO SET UP *
* FOR INDEXING HIGH *
* BYTE IN TABLE *
*****
I
*****
* INIT "SCR" TO *
* START WITH *
* LINE 00 *
*****
I<-----
*****
* LOAD "CAR" "BCR" *
* AND "LPR" REGS *
* FOR SELECTED LINE *
*****
I
*****
* CLEAR LC BYTE TABLE *
* ENTRY AND LOAD [R3] *
* INTO HI BYTE *
*****
I
***
**A*
***

```

```

***
**A*
***
I
*****
* INCREMENT (SCR) *
* UPDATE R3,R2, AND *
* R4 FOR NEXT ENTRY *
*****
I
*****
* COUNT $TMP6 *
* TO INDICATE THE *
* NEXT LINE TO DO *
*****
I
-----
NO / HAVE WE SET /
I / UP ALL 16. LINES /
I /
I YES
*****
**RTS **
*****
I
*****
*CHPS1 *
*****
I
*****
* PUSH NEW PSW=000 *
* AND NEW PC=1$ *
* ON TO STACK *
*****
I
*****
* DO AN RTI TO *
* LOAD NEW PSW *
* GO TO 1$ *
*****
I
*****
* DO RTS TO *
* RETURN TO *
* CALLER *
*****
I
*****
**RTS **

```

```

*****
*CHPS2 *
*****
I
*****
* PUSH PSW=340 *
* AND PC=1$ *
* ON THE STACK *
*****
I
*****
* DO AN RTI TO *
* LOAD NEW PSW *
* GO TO 1$ *
*****
I
*****
* DO AN RTS *
* TO RETURN TO *
* CALLER *
*****
I
*****
**RTS **
*****

```

```

*****
*SAPS *
*****
I
*****
* PUSH STACK TO *
* SAVE SPACE *
* FOR SAVPSW *
*****
I
*****
* PUSH THE CURRENT *
* CONTENTS OF THE *
* TRAP VECTOR *
*****
I
*****
* SET UP TRAP VECT- *
* OR TO GO TO 1$ *
*****
I
*****
* DO A "TRAP" *
* INSTRUCTION *
*****
I
*****
* SAVE PSW, PUSH *
* 2$ ON STACK *
* DO RTI *
*****
I
*****
* RESTORE TRAP VECTOR *
* POP STACK (SAVPS) *
* INTO $TMP0 *
*****
I
*****
**RTS **
*****

```

NOTE: I"CHPS1", "CHPS2", AND "SAPS" ARE CALLED WHENEVER  
THE MAINLINE CODE HAS TO CLEAR THE PSW, LOCK OUT INTRs,  
AND SAVE THE PSW RESPECTIVELY

THESE ROUTINES ARE REQUIRED FOR LS111 COMPATIBILITY

\*\*\*\*\*  
\*LDTBF1 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SET R1 TO \*  
\* PCINT TO XMIT \*  
\* BUFFER \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* INIT R2=0 \*  
\* AS A CHAR \*  
\* GENERATOR \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* LOAD [R2] INTO \*  
\* XMIT BUFFER \*  
\* UPDATE R1 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* GENERATE \*  
\* NEXT CHAR \*  
\*\*\*\*\*

-----  
LOADED ALL  
256.. COMBINATIONS  
-----

I YES  
\*\*\*\*\*  
\*\*RTS \*\*

\*\*\*\*\*  
\*SUER1 \*  
\*\*\*\*\*

I SAPS(54)  
\*\*\*\*\*  
\*\* GO SAVE PSW \*\*  
\*\* IN \$TMPD \*\*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SAVE TEST NO. \*  
\* IN R0 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SAVE R0,R1,R2,R6 \*  
\* IN \$REG<0,1,2,6> \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* CORRECT \$REG6 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\*\*RTS \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*SUER2 \*  
\*\*\*\*\*

I SAPS(54)  
\*\*\*\*\*  
\*\* GO SAVE PSW \*\*  
\*\* IN \$TMPD \*\*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SAVE TEST NO. \*  
\* IN R0 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SAVE R0,R1,R2,R3,R4, \*  
\* AND R6 IN \*  
\* \$REG<0,1,2,3,4,6> \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* CORRECT \$REG6 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\*\*RTS \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*SUER2A \*  
\*\*\*\*\*

I  
I  
I  
I  
I

\*\*\*\*\*  
\*SUER4 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SAVE LINE NO. \*  
\* IN \$TMPD \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SAVE R0,R1,R2,R3,R4 \*  
\* IN \$REG<0,1,2,3,4> \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\*\*RTS \*\*  
\*\*\*\*\*

\*\*\*\*\*  
\*SLER3 \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\* SAVE R0,R1,R2 \*  
\* IN \$REG<0,1,2> \*  
\*\*\*\*\*

I  
\*\*\*\*\*  
\*\*RTS \*\*  
\*\*\*\*\*

```

*****
*SUNUM *
*****
I
*****
* SAVE REGS RETRIEVE *
* ADDRESSES OF NUM *
* AND MSG BUFFER *
*****
I
*****
* GET NUMBER *
* TO CONVERT *
*****
I
*****
* CONVERT AND *
* STORE MSD *
*****
I
*****
* CONVERT AND *
* STORE LSD *
*****
I
*****
* RESTORE REGS *
*****
I
*****
**RTS **
*****

```

```

*****
*CLCABC *
*****
I
*****
* INIT A LINE *
* COUNTER TO *
* START AT 00 *
*****
I
*****
* SELECT A *
* LINE IN THE *
* "SCR" *
*****
I
*****
* CLEAR "CAR" *
* AND "BCR" *
* FOR SEL LINE *
*****
I
*****
* UPDATE LINE *
* COUNTER *
*****
I
-----
CLEARED ALL \NO
16. LINES YET -----
I
I YES
*****
* INIT "SCR" *
* TO SELECT *
* LINE 00 *
*****
I
*****
**RTS **

```

```

*****
*LDBCR *
*****
I
*****
* INIT A LINE *
* COUNTER TO *
* STRT AT 00 *
*****
I
*****
* SELECT A *
* LINE IN THE *
* "SCR" *
*****
I
*****
* LOAD THAT *
* LINE'S "BCR" *
* WITH A 177777 *
*****
I
*****
* GENERATE NEXT *
* LINE NO. *
*****
I
-----
DONE 16. LINES ? \NO
-----
I
I YES
*****
**RTS **
*****

```

```

*****
*SUPPAR *
*****
I
*****
* INIT LINE COUNTER *
* AND "SCR" TO *
* START AT LINE 00 *
*****
I
*****
* INIT R3 AND R4 *
* TO LOAD TEST DATA *
* TABLE *
*****
I
*****
* LOAD "CAR", "BCR", *
* AND "LPR" FOR *
* SELECTED LINE *
*****
I
*****
* GENERATE NEW *
* LINE NO. *
*****
I
*****
* DONE SET UP \NO *
* FOR 16. LINES *
*****
I YES
*****
* SET UP MULTI-LINE *
* PARITY TEST DATA *
* TABLE *
*****
I
*****
**RTS **
*****

```

```

*****
*INPARA *
*****
I
*****
* ASK USER TO *
* TYPE IN VECTOR *
* DISPLACEMENT *
*****
I
*****
* DID HE TYPE \YES *
* A <CR> ONLY ? *
*****
I NO
*****
* DID HE TYPE \YES *
* A "4" ? *
*****
I NO
*****
* DID HE TYPE \YES *
* A "10(8)" ? *
*****
I YES
*****
* LOAD RO WITH *
* A 20(8) *
*****
I
*****
* LOAD RO *
* WITH A 10(8) *
*****
I
*****
**RTS **
*****

```

```

*****
*ENDA(S:) *
*****
I
*****
*SCOPE(S2)*
*****
* "NOP" SCOPE *
* CALL IN SEOP *
* ROUTINE *
*****
I
*****
* GENERATE NEXT *
* DEVICE NO. *
*****
I
*****
* UPDATE DEVICE PARA- *
* METER TABLE POINTERS *
* SHIFT SELECT MASK *
*****
I
*****
* TESTED ALL \YES *
* POSSIBLE DH11'S *
*****
I NO
*****
* IS THIS DH11 *
* SELECTED FOR TEST *
*****
I YES
*****
* CLEAR $STNM *
* TO START AT *
* TST I AGAIN *
*****
I
*****
* RSTRTA(02)*
*****
I
*****
* CALL "SEOP" TO *
* REPORT END OF *
* PASS *
*****

```

```
*****  
*CHKADR *  
*****  
I  
-----  
/ WAS DEVICE ADDR \ NO  
/ TYPED GREATER \  
/ THAN 160020(8) ? \  
-----  
15 I YES  
I  
-----  
/ WAS IT LESS \ NO  
/ THAN 160420(8) ? \  
-----  
25 I YES  
I  
-----  
/ WAS IT A MULT- \ NO  
/ IPLE OF 20(8) ? \  
-----  
45 I YES  
*****  
/ PRINT INVALID  
/ ADDRESS MESSAGE  
-----  
*****  
I  
35 I  
*****  
*GENERATE AND LOAD 16.*  
* ENTRY DH11 DEVICE *  
* ADDRESS TABLE *  
*****  
I  
*****  
**RTS **  
*****
```

```
*****  
*CHKVCT *  
*****  
I  
-----  
/ WAS VECTOR ADDR \ NO  
/ TYPED GREATER \  
/ THAN 300(8) ? \  
-----  
15 I YES  
I  
-----  
/ WAS IT LESS \ NO  
/ THAN 1000(8) ? \  
-----  
25 I YES  
I  
-----  
/ WAS IT A MULT- \ NO  
/ IPLE OF 10(8) ? \  
-----  
45 I YES  
*****  
/ PRINT INVALID  
/ VECTOR MESSAGE  
-----  
*****  
I  
35 I  
*****  
* GENERATE AND LOAD *  
* 16. ENTRY DH11 VECT. *  
* ADDRESS TABLE *  
*****  
I  
*****  
**RTS **  
*****
```





```
*****  
*T40A(35) *  
*****  
      I      SAPS(54)  
*****  
**          **  
** GO SAVE ERROR PSW **  
**          **  
*****  
      I  
*****  
* SAVE ERROR *  
* INFORMATION *  
*          *  
*****  
      I      SUER2A(55)  
*****  
** GO SET UP INFORM- **  
** ATION TO BE PRINTED **  
**          **  
*****  
      I      SUNUM(56)  
*****  
** GO PUT LINE NO. **  
** IN ERROR MSG **  
**          **  
*****  
      I      SERROR(53)  
*****  
** REPORT STORAGE **  
** OVERFLOW TIMEOUT **  
** EM57,DH2,DT2,0 **  
*****  
      I  
*****  
*T40B(35) *  
*****
```

```
*****  
*T44X(39) *  
*****  
      I      SAPS(54)  
*****  
**          **  
** GO SAVE ERROR PSW **  
**          **  
*****  
      I  
*****  
* SAVE ERROR *  
* INFORMATION *  
*          *  
*****  
      I      SUER2A(55)  
*****  
** GO SET UP INFORM- **  
** ATION TO BE PRINTED **  
**          **  
*****  
      I      SUNUM(56)  
*****  
** GO PUT LINE NO. **  
** IN ERROR MSG **  
**          **  
*****  
      I      SERROR(53)  
*****  
** REPORT CHAR AVAIL **  
** TIMEOUT ERROR **  
** EM22,DH2,DT2,0 **  
*****  
      I  
*****  
*T44Y(40) *  
*****
```

```
*****  
*SELINE *  
*****  
      I  
-----  
NO / 1ST TIME THRU  
I-----FOR CURRENT TEST ?  
-----  
      I YES  
*****  
* SET ENTRY FLAG,INIT *  
* MASK AND "LINE" TO *  
* BEGIN WITH LINE 00 *  
*****  
      I  
*****  
* GENERATE LINE *  
----->* NO. IN "LINE" *  
*          *  
*****  
      I  
*****  
* SHIFT SELECT *  
* TEST MASK *  
*          *  
*****  
      I  
-----  
YES / TESTED FOR ALL  
I-----16. LINES?  
-----  
      I NO  
-----  
IS THIS LINE / NO  
SELECTED FOR /  
TESTING ?  
-----  
      I YES  
*****  
* CLEAR LINE * *  
* AND ENTRY * *  
* FLAG * *  
*****  
      I  
*****  
* MOVE RETURN *  
* PC AROUND *  
* EXIT BRANCH *  
*****  
      I  
*****  
* INIT LINE SEL. *  
----->* BITS IN "SCR" *  
*          *  
*****  
      I  
*****  
**RTS **
```

MD-11-DZDMM-B DH11 DIAGNOSTIC  
FLOW CHART CROSS REFERENCE LIST

AF1	F	55																
AF2	F	55																
AF3	F	55	45															
AF4	F	55	46															
AF5	F	55	46															
BEGINA	F	01																
BRK1	F	59																
BRK2	F	59																
BRK3	F	59																
BRK4	F	59	49															
BRK5	F	59																
BUSER	F	59																
CHKADR	F	58																
CHKVCT	F	58																
CHPS1	F	58																
CHPS2	F	58																
CLCABC	F	50	50	56														
ENDR	F	57																
HALT	F	57																
INPAR	F	57																
INPAR3	F	02																
INPARA	F	57																
LOBCR	F	56																
LOTBF1	F	55																
NPR1A	F	59																
NPR2A	F	59																
NPR3A	F	59																
NPR4A	F	59																
NPR5A	F	59																
NPR6A	F	59																
RESERR	F	59																
REST1	F	59																
RESTRP	F	59																
RESTRT	F	01																
RSTRTA	F	02	57															
RTI	F	54	54	54	55	55	55	55	55	56	56	56	57	57	58	58	59	59
RTS	F	54	54	54	55	55	55	55	55	56	56	56	57	57	58	58	59	59
SAFE	F	55	55	60	60													
SELIN	F	15	16	17	18	19	20	21	22	28	30	35	36	37	38	39	41	44
SELIN	F	48	50	51	60													
SETALL	F	55																
SLO1	F	40																
SLO2	F	40	40															
SLO3	F	40	40	40														
START	F	01																
START1	F	01	01	02														
START2	F	01	01	02														
SUER1	F	05	05	06	07	07	07	08	08	09	09	11	11	12	12	13	13	14
SUER2	F	05	05	06	07	07	07	08	08	09	09	11	11	12	12	13	13	14
15	F	16	16	17	17	22	32	33	38	39	55							





THIS IS A HISTORY FILE OF THE DEVELOPMENT OF MD-11-DZDHM

SEQ 0116

PRODUCT CODE: MD-11-DZDHM                   VERSION 000.000

PRODUCT NAME: DH11 DIAGNOSTIC

RELEASE DATE: JANUARY 1976

AUTHOR: ED CROWLEY

\*\*\*\*\*

PRODUCT CODE: MD-11-DZDHM-B               (REV B)

PRODUCT NAME: DH11 DIAGNOSTIC

RELEASE DATE: SEPTEMBER 1976

SUBMITTED BY: PAUL F. CANTIN

\*\*\*\*\*

PROGRAM CHANGES:

1. A DH11/DM11-BB AUTOSIZER HAS BEEN BUILT AND INSERTED INTO THE PROGRAM TO MAKE IT CHAINABLE UNDER ACT AND APT. CODE WAS ALSO INSERTED TO LOAD AND RUN NON-CONTIGUOUS DH11 ADDRESSES WITHOUT OPERATOR INTERVENTION.
2. WHEN A DH11 REGISTER FAILS TO RESPOND DURING TEST 1, THE PROGRAM ENTERS AN ENDLESS LOOP CAUSING ERROR MESSAGE 1 TO BE PRINTED CONTINUOUSLY. CODE HAS BEEN CORRECTED.
3. PROGRAM UPDATED TO USE SWITCHLESS FEATURE IN SYSMAC REV.C1.
4. IN ORDER TO FACILITATE INSTALLATION CHECKOUT WHERE MODEM CONTROL IS INVOLVED, TESTS 101, 105, 106, AND 107 OF DZDHK HAVE BEEN INSERTED. THIS ALLOWS ALL THE LEVEL CONVERTERS AND CABLES TO BE CHECKED WITH JUST ONE PROGRAM USING THE H315 TURNAROUND CONNECTORS.
5. CODE HAS BEEN INSERTED TO INHIBIT FALSE ERROR REPORTING WHICH SOMETIMES OCCURS WHEN H315 TURNAROUND CONNECTORS ARE USED ON SOME LINES WHILE OTHER LINES REMAIN OPEN.
6. TEST 40 HAS BEEN RELOCATED BETWEEN TEST 42 AND TEST 43.
7. THE "HALT AFTER PARAMETER SETUP" OPTION SHOULD BE CONTROLLED BY A SWITCH OTHER THAN SR15. CODING HAS BEEN CHANGED TO SENSE SRO8 FOR THIS OPTION.

DOCUMENT CHANGES:

1. FLOW CHARTS HAVE BEEN DELETED ALONG WITH SECTIONS 6.2D AND 6.5.

2. CHANGE "WORDS BETWEEN VECTORS (4(8) OR 10(8))" REFERENCES TO "ADDRESSES BETWEEN VECTORS (10(8) OR 20(8))", WITH APPROPRIATE CODING CHANGES.

3. PARAGRAPH ON SWITCHLESS FEATURE INSERTED.

4. AUTOSIZER STARTING PROCEDURE DESCRIBED.

5. CONSOLE SWITCH REGISTER OPRIONS TABLE INSERTED.

6. SEVERAL ADDITIONS TO SECTION 6.3 WERE MADE FOR CLARITY.

\*\*\*\*\*



5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26  
27  
28  
29  
30  
31  
32  
33  
34  
35  
36  
37  
38  
39  
40  
41  
42  
43  
44  
45  
46  
47  
48  
49  
50  
51  
52  
53  
54  
55  
56  
57  
58  
59  
60  
61  
62  
63  
64  
65  
66  
67  
68  
69  
70  
71  
72  
73  
74  
75  
76  
77  
78  
79  
80  
81  
82  
83  
84  
85  
86  
87  
88  
89  
90  
91  
92  
93  
94  
95  
96  
97  
98  
99  
100

156 DM11-BB DIAGNOSTIC CONTINUED  
 157 DM11-BB DIAGNOSTIC CONTINUED  
 160 DM11-BB DIAGNOSTIC CONTINUED  
 END OF PASS ROUTINE  
 SCOPE HANDLER ROUTINE  
 ERROR HANDLER ROUTINE  
 ERROR MESSAGE TIMEOUT ROUTINE  
 BINARY TO OCTAL (ASCII) AND TYPE  
 CONVERT BINARY TO DECIMAL AND TYPE ROUTINE  
 TYPE ROUTINE  
 APT COMMUNICATIONS ROUTINE  
 TTY INPUT ROUTINE  
 READ AN OCTAL NUMBER FROM THE TTY  
 TRAP DECODER  
 TRAP TABLE  
 POWER DOWN AND UP ROUTINES



MAINDEC-11-DZDMM-B  
DMMAC.P11

MAY11 27(732) 23-SEP-76 14:33 PAGE 1

D10

SEQ 0120

ih.ewru-



117  
116  
115  
114  
113  
112  
111  
110  
109  
108  
107  
106  
105  
104  
103  
102  
101  
100  
99  
98  
97  
96  
95  
94  
93  
92  
91  
90  
89  
88  
87  
86  
85  
84  
83  
82  
81  
80  
79  
78  
77  
76  
75  
74  
73  
72  
71  
70  
69  
68  
67  
66  
65  
64  
63  
62  
61  
60  
59  
58  
57  
56  
55  
54  
53  
52  
51  
50  
49  
48  
47  
46  
45  
44  
43  
42  
41  
40  
39  
38  
37  
36  
35  
34  
33  
32  
31  
30  
29  
28  
27  
26  
25  
24  
23  
22  
21  
20  
19  
18  
17  
16  
15  
14  
13  
12  
11  
10  
9  
8  
7  
6  
5  
4  
3  
2  
1

000214  
000024  
000200  
000044  
000214  
000214  
000214  
000216  
000220  
000222  
000224  
000226  
000011  
000012  
000015  
000207  
177776  
177774  
177772  
177570  
177570  
000000  
000001  
000002  
000003  
000004  
000005  
000006  
000007  
000006  
000007  
000000  
000040

```
*****  
:SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT  
*****  
.$X=      :SAVE CURRENT LOCATION  
.=24     :SET POWER FAIL TO POINT TO START OF PROGRAM  
200      :FOR APT START UP  
.=44     :POINT TO APT INDIRECT ADDRESS PNTR.  
$APTHDR  :POINT TO APT HEADER BLOCK  
.=.$X    :RESET LOCATION COUNTER  
*****  
:SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC  
:INTERFACE SPEC.
```

```
$APTHD:      :  
$SHIBTS: .WORD 0      :TWO HIGH BITS OF 18 BIT MAILBOX ADDR.  
$MBADR: .WORD $MAIL   :ADDRESS OF APT MAILBOX (BITS 0-15)  
$STIM: .WORD 30.     :RUN TIM OF LONGEST TEST  
$PASTM: .WORD 120.   :RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)  
$UNITM: .WORD 120.   :ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT  
          .WORD $ETEND-$MAIL/2 ;;LENGTH MAILBOX-ETABLE(WORDS)
```

.SBTTL BASIC DEFINITIONS

```
;*INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***  
STACK= 1100  
.EQUIV EMT.ERROR      ;;BASIC DEFINITION OF ERROR CALL  
.EQUIV IOT.SCOPE     ;;BASIC DEFINITION OF SCOPE CALL
```

:+MISCELLANEOUS DEFINITIONS

```
HT= 11      ;;CODE FOR HORIZONTAL TAB  
LF= 12      ;;CODE FOR LINE FEED  
CR= 15      ;;CODE FOR CARRIAGE RETURN  
CRLF= 200   ;;CODE FOR CARRIAGE RETURN-LINE FEED  
PS= 177776  ;;PROCESSOR STATUS WORD  
.EQUIV PS,PSW  
STKLMT= 177774 ;;STACK LIMIT REGISTER  
PIRQ= 177772  ;;PROGRAM INTERRUPT REQUEST REGISTER  
DSWR= 177570  ;;HARDWARE SWITCH REGISTER  
DDISP= 177570 ;;HARDWARE DISPLAY REGISTER
```

:\*GENERAL PURPOSE REGISTER DEFINITIONS

```
R0= %0      ;;GENERAL REGISTER  
R1= %1      ;;GENERAL REGISTER  
R2= %2      ;;GENERAL REGISTER  
R3= %3      ;;GENERAL REGISTER  
R4= %4      ;;GENERAL REGISTER  
R5= %5      ;;GENERAL REGISTER  
R6= %6      ;;GENERAL REGISTER  
R7= %7      ;;GENERAL REGISTER  
SP= %6      ;;STACK POINTER  
PC= %7      ;;PROGRAM COUNTER
```

:+PRIORITY LEVEL DEFINITIONS

```
PRI0= 0      ;;PRIORITY LEVEL 0  
PRI1= 40     ;;PRIORITY LEVEL 1
```

118  
119  
120  
121  
122  
123  
124  
125  
126  
127  
128  
129  
130  
131  
132  
133  
134  
135  
136  
137  
138  
139  
140  
141  
142  
143  
144  
145  
146  
147  
148  
149  
150  
151  
152  
153  
154  
155  
156  
157  
158  
159  
160  
161  
162  
163  
164  
165  
166  
167  
168  
169  
170  
171  
172  
173

000100  
000140  
000200  
000240  
000300  
000340  
  
100000  
040000  
020000  
010000  
004000  
002000  
001000  
000400  
000200  
000100  
000040  
000020  
000010  
000004  
000002  
000001  
  
100000  
040000  
020000  
010000  
004000  
002000  
001000  
000400  
000200  
000100  
000040  
000020  
000010  
000004  
000002  
000001

PR2= 100  
PR3= 140  
PR4= 200  
PR5= 240  
PR6= 300  
PR7= 340  
::PRIORITY LEVEL 2  
::PRIORITY LEVEL 4  
::PRIORITY LEVEL 5  
::PRIORITY LEVEL 6  
::PRIORITY LEVEL 7

:"SWITCH REGISTER" SWITCH DEFINITIONS

SW15= 100000  
SW14= 40000  
SW13= 20000  
SW12= 10000  
SW11= 4000  
SW10= 2000  
SW09= 1000  
SW08= 400  
SW07= 200  
SW06= 100  
SW05= 40  
SW04= 20  
SW03= 10  
SW02= 4  
SW01= 2  
SW00= 1  
.EQUIV SW09,SW9  
.EQUIV SW08,SW8  
.EQUIV SW07,SW7  
.EQUIV SW06,SW6  
.EQUIV SW05,SW5  
.EQUIV SW04,SW4  
.EQUIV SW03,SW3  
.EQUIV SW02,SW2  
.EQUIV SW01,SW1  
.EQUIV SW00,SW0

:"DATA BIT DEFINITIONS (BIT0 TO BIT15)

BIT15= 100000  
BIT14= 40000  
BIT13= 20000  
BIT12= 10000  
BIT11= 4000  
BIT10= 2000  
BIT09= 1000  
BIT08= 400  
BIT07= 200  
BIT06= 100  
BIT05= 40  
BIT04= 20  
BIT03= 10  
BIT02= 4  
BIT01= 2  
BIT00= 1  
.EQUIV BIT09,BIT9  
.EQUIV BIT08,BIT8  
.EQUIV BIT07,BIT7  
.EQUIV BIT06,BIT6

174  
175  
176  
177  
178  
179  
180  
181  
182  
183  
184  
185  
186  
187  
188  
189  
190  
191  
192  
193

.EQUIV BIT05,BIT5  
.EQUIV BIT04,BIT4  
.EQUIV BIT03,BIT3  
.EQUIV BIT02,BIT2  
.EQUIV BIT01,BIT1  
.EQUIV BIT00,BIT0

000004  
000010  
000014  
000014  
000014  
000014  
000020  
000024  
000030  
000034  
000060  
000064  
000240

.\*BASIC "CPU" TRAP VECTOR ADDRESSES  
ERRVEC= 4 ;: TIME OUT AND OTHER ERRORS  
RESVEC= 10 ;: RESERVED AND ILLEGAL INSTRUCTIONS  
TBITVEC= 14 ;: "T" BIT  
TRTVEC= 14 ;: TRACE TRAP  
BPTVEC= 14 ;: BREAKPOINT TRAP (3PT)  
IOTVEC= 20 ;: INPUT/OUTPUT TRAP (IOT) \*\*SCOPE\*\*  
PWRVEC= 24 ;: POWER FAIL  
EMTVEC= 30 ;: EMULATOR TRAP (EMT) \*\*ERROR\*\*  
TRAPVEC= 34 ;: "TRAP" TRAP  
TKVEC= 60 ;: TTY KEYBOARD VECTOR  
TPVEC= 64 ;: TTY PRINTER VECTOR  
PIRQVEC= 240 ;: PROGRAM INTERRUPT REQUEST VECTOR



250 001224 000000  
 251 001226 077  
 252 001227 015  
 253 001230 000012  
 254  
 255  
 256  
 257  
 258  
 259  
 260 001232 000000  
 261 001234 000000  
 262 001236 000000  
 263 001240 000000  
 264 001242 000000  
 265 001244 000000  
 266 001246 000000  
 267 001250 000000  
 268 001252  
 269 001252 000  
 270 001253 000  
 271 001254 000000  
 272 001256 000000  
 273 001260 000000  
 274  
 275  
 276  
 277  
 278  
 279  
 280 001262 000  
 281 001263 000  
 282  
 283  
 284  
 285  
 286 001264 000000  
 287  
 288 001266 000  
 289 001267 000  
 290 001270 000000  
 291 001272 000  
 292 001273 000  
 293 001274 000000  
 294 001276 000  
 295 001277 000  
 296 001300 000000  
 297 001302 000000  
 298 001304 000000  
 299 001306 000000  
 300 001310 000000  
 301 001312 000000  
 302 001314 000000  
 303 001316 000000  
 304 001320 000000  
 305 001322 000000

```

$ESCAPE:0                ;; ESCAPE CN ERROR ADDRESS
$QUES: .ASCII  /?/      ;; QUESTION MARK
$CRLF: .ASCII  <15>    ;; CARRIAGE RETURN
$LF: .ASCII  <12>     ;; LINE FEED
:*****
.SBTTL  APT MAILBOX-ETABLE

:*****
.EVEN
$MAIL:                   ;; APT MAILBOX
$MSGTY: .WORD  AMSGTY    ;; MESSAGE TYPE CODE
$FATAL: .WORD  AFATAL    ;; FATAL ERROR NUMBER
$TESTN: .WORD  ATESTN    ;; TEST NUMBER
$PASS: .WORD  APASS      ;; PASS COUNT
$DEVCT: .WORD  ADEVCT    ;; DEVICE COUNT
$UNIT: .WORD  AUNIT      ;; I/O UNIT NUMBER
$MSGAD: .WORD  AMSGAD    ;; MESSAGE ADDRESS
$MSGLG: .WORD  AMSGLG    ;; MESSAGE LENGTH
$ETABLE:                 ;; APT ENVIRONMENT TABLE
$ENV: .BYTE  AENV        ;; ENVIRONMENT BYTE
$ENVM: .BYTE  AENVM      ;; ENVIRONMENT MODE BITS
$SWREG: .WORD  ASWREG    ;; APT SWITCH REGISTER
$USWR: .WORD  AUSWR      ;; USER SWITCHES
$CPUOP: .WORD  ACPUOP    ;; CPU TYPE, OPTIONS
: *
: *                      BIT 15-11=CPU TYPE
: *                      11/04=01, 11/05=02, 11/20=03, 11/40=04, 11/45=05
: *                      11/70=06, PDQ=07, Q=10
: *
: *                      BIT 10=REAL TIME CLOCK
: *                      BIT 9=FLOATING POINT PROCESSOR
: *                      BIT 8=MEMORY MANAGEMENT
$MAMS1: .BYTE  AMAMS1    ;; HIGH ADDRESS, M.S. BYTE
$MTYP1: .BYTE  AMTYP1    ;; MEM. TYPE, BLK#1
: *
: *                      MEM. TYPE BYTE -- (HIGH BYTE)
: *                      900 NSEC CORE=001
: *                      300 NSEC BIPOLAR=002
: *                      500 NSEC MOS=003
$MADR1: .WORD  AMADR1    ;; HIGH ADDRESS, BLK#1
: *
: *                      MEM. LAST ADDR.=3 BYTES, THIS WORD AND LOW OF "TYPE" ABOVE
$MAMS2: .BYTE  AMAMS2    ;; HIGH ADDRESS, M.S. BYTE
$MTYP2: .BYTE  AMTYP2    ;; MEM. TYPE, BLK#2
$MADR2: .WORD  AMADR2    ;; MEM. LAST ADDRESS, BLK#2
$MAMS3: .BYTE  AMAMS3    ;; HIGH ADDRESS, M.S. BYTE
$MTYP3: .BYTE  AMTYP3    ;; MEM. TYPE, BLK#3
$MADR3: .WORD  AMADR3    ;; MEM. LAST ADDRESS, BLK#3
$MAMS4: .BYTE  AMAMS4    ;; HIGH ADDRESS, M.S. BYTE
$MTYP4: .BYTE  AMTYP4    ;; MEM. TYPE, BLK#4
$MADR4: .WORD  AMADR4    ;; MEM. LAST ADDRESS, BLK#4
$VECT1: .WORD  AVECT1    ;; INTERRUPT VECTOR#1 BUS PRIORITY#1
$VECT2: .WORD  AVECT2    ;; INTERRUPT VECTOR#2 BUS PRIORITY#2
$BASE: .WORD  ABASE      ;; BASE ADDRESS OF EQUIPMENT UNDER TEST
$DEVM: .WORD  ADEV      ;; DEVICE MAP
$CDW1: .WORD  ACDW1     ;; CONTROLLER DESCRIPTION WORD#1
$CDW2: .WORD  ACDW2     ;; CONTROLLER DESCRIPTION WORD#2
$DDW0: .WORD  ADDW0     ;; DEVICE DESCRIPTOR WORD#0
$DDW1: .WORD  ADDW1     ;; DEVICE DESCRIPTOR WORD#1
$DDW2: .WORD  ADDW2     ;; DEVICE DESCRIPTOR WORD#2

```

306	001324	000000	\$DDW3:	.WORD	ADDW3	:::DEVICE	DESCRIPTOR	WORD#3
307	001326	000000	\$DDW4:	.WORD	ADDW4	:::DEVICE	DESCRIPTOR	WORD#4
308	001330	000000	\$DDW5:	.WORD	ADDW5	:::DEVICE	DESCRIPTOR	WORD#5
309	001332	000000	\$DDW6:	.WORD	ADDW6	:::DEVICE	DESCRIPTOR	WORD#6
310	001334	000000	\$DDW7:	.WORD	ADDW7	:::DEVICE	DESCRIPTOR	WORD#7
311	001336	000000	\$DDW8:	.WORD	ADDW8	:::DEVICE	DESCRIPTOR	WORD#8
312	001340	000000	\$DDW9:	.WORD	ADDW9	:::DEVICE	DESCRIPTOR	WORD#9
313	001342	000000	\$DDW10:	.WORD	ADDW10	:::DEVICE	DESCRIPTOR	WORD#10
314	001344	000000	\$DDW11:	.WORD	ADDW11	:::DEVICE	DESCRIPTOR	WORD#11
315	001346	000000	\$DDW12:	.WORD	ADDW12	:::DEVICE	DESCRIPTOR	WORD#12
316	001350	000000	\$DDW13:	.WORD	ADDW13	:::DEVICE	DESCRIPTOR	WORD#13
317	001352	000000	\$DDW14:	.WORD	ADDW14	:::DEVICE	DESCRIPTOR	WORD#14
318	001354	000000	\$DDW15:	.WORD	ADDW15	:::DEVICE	DESCRIPTOR	WORD#15
319								
320								
321	001356		\$ETEND:					
322								



323  
324  
325  
326  
327  
328  
329  
330  
331  
332  
333  
334  
335  
336  
337  
338  
339  
340  
341  
342  
343  
344  
345  
346  
347  
348  
349  
350  
351  
352  
353  
354  
355  
356  
357  
358  
359  
360  
361  
362  
363  
364  
365  
366  
367  
368  
369  
370  
371  
372  
373  
374  
375  
376  
377  
378

.SBTTL ERROR POINTER TABLE

;\*THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.  
;\*THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN  
;\*LOCATION \$ITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.  
;\*NOTE1: IF \$ITEMB IS 0 THE ONLY PERTINENT DATA IS (\$ERRPC).  
;\*NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:

;\* EM ;;POINTS TO THE ERROR MESSAGE  
;\* DH ;;POINTS TO THE DATA HEADER  
;\* DT ;;POINTS TO THE DATA  
;\* DF ;;POINTS TO THE DATA FORMAT

\$ERRTB:  
;ERROR TABLE ITEM FOR ERROR MESSAGE 1

EM1 ;"DH11 REGISTER REFERENCE CAUSED TIMEOUT"  
DH1 ;" (PC) (PS) (SP) TEST DEVADR REGADR "  
DT1 ;\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2  
0 ;PRINT ALL OCTAL

;ERROR TABLE ITEM FOR ERROR MESSAGE 2

EM2 ;"SYSTEM CONTROL REGISTER ERROR"  
DH2 ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "  
DT2 ;\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4  
0 ;PRINT ALL OCTAL

;ERROR TABLE ITEM FOR ERROR MESSAGE 3

EM3 ;"DH11 MASTER CLEAR FAILED TO CLR SPECIFIED REG"  
DH2 ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "  
DT2 ;\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4  
0 ;PRINT ALL OCTAL

;ERROR TABLE ITEM FOR ERROR MESSAGE 4

EM4 ;"LINE PARAMETER REGISTER ERROR"  
DH2 ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "  
DT2 ;\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4  
0 ;PRINT ALL OCTAL

;ERROR TABLE ITEM FOR ERROR MESSAGE 5

EM5 ;"BREAK CONTROL REGISTER ERROR"  
DH2 ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "  
DT2 ;\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4  
0 ;PRINT ALL OCTAL

;ERROR TABLE ITEM FOR ERROR MESSAGE 6

EM6 ;"SILO STATUS REGISTER ERROR"  
DH2 ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "  
DT2 ;\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4  
0 ;PRINT ALL OCTAL

# M10

```

379
380      ;ERROR TABLE ITEM FOR ERROR MESSAGE 7
381
382      001436 030776      EM7      ;"CURRENT ADDRESS REGISTER ERROR - LINE #XX"
383      001440 030452      DH2      ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
384      001442 030550      DT2      ;$ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
385      001444 000000      0        ;PRINT ALL OCTAL
386
387      ;ERROR TABLE ITEM FOR ERROR MESSAGE 10
388
389      001446 031050      EM10     ;"BYTE COUNTER REGISTER ERROR - LINE #XX"
390      001450 030452      DH2      ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
391      001452 030550      DT2      ;$ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
392      001454 000000      0        ;PRINT ALL OCTAL
393
394      ;ERROR TABLE ITEM FOR ERROR MESSAGE 11
395
396      001456 031117      EM11     ;"UNEXPECTED DH11 RCVR INTERRUPT"
397      001460 030452      DH2      ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
398      001462 030550      DT2      ;$ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
399      001464 000000      0        ;PRINT ALL OCTAL
400
401      ;ERROR TABLE ITEM FOR ERROR MESSAGE 12
402
403      001466 031156      EM12     ;"UNEXPECTED DH11 XMITTR INTERRUPT"
404      001470 030452      DH2      ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
405      001472 030550      DT2      ;$ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
406      001474 000000      0        ;PRINT ALL OCTAL
407
408      ;ERROR TABLE ITEM FOR ERROR MESSAGE 13
409
410      001476 031217      EM13     ;"CHAR AVAILABLE FAILED TO GENERATE RCVR INTERRUPT"
411      001500 030452      DH2      ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
412      001502 030550      DT2      ;$ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
413      001504 000000      0        ;PRINT ALL OCTAL
414
415      ;ERROR TABLE ITEM FOR ERROR MESSAGE 14
416
417      001506 031300      EM14     ;"TRANSMITTER NPR LOGIC ERROR - LINE # "
418      001510 030452      DH2      ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
419      001512 030550      DT2      ;$ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
420      001514 000000      0        ;PRINT ALL OCTAL
421
422      ;ERROR TABLE ITEM FOR ERROR MESSAGE 15
423
424      001516 031347      EM15     ;"XMITTR FAILED TO INTERRUPT - LINE # "
425      001520 030452      DH2      ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
426      001522 030550      DT2      ;$ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
427      001524 000000      0        ;PRINT ALL OCTAL
428
429      ;ERROR TABLE ITEM FOR ERROR MESSAGE 16
430
431      001526 031415      EM16     ;"RCVR FAILED TO INTERRUPT"
432      001530 030452      DH2      ;" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
433      001532 030550      DT2      ;$ERRPC,$TMPD,$REG6,$REG0,$REG1,$REG2,$REG3,$REG4
434      001534 000000      0        ;PRINT ALL OCTAL
  
```

435					
436					
437					
438	001536	031446	EM17	;	"TRANSMITTER TIMING ERROR - LINE # "
439	001540	031512	DH6	;	" (PC) (PS) (SP) TEST DEVADR SPEED TIMEB TIMEC"
440	001542	030550	DT2	;	\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4
441	001544	000000	0	;	PRINT ALL OCTAL
442					
443					
444					
445	001546	031610	EM20	;	RECEIVER TIMING ERROR - LINE # "
446	001550	031512	DH6	;	" (PC) (PS) (SP) TEST DEVADR SPEED TIMEB TIMEC"
447	001552	030550	DT2	;	\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4
448	001554	000000	0	;	PRINT ALL OCTAL
449					
450					
451					
452	001556	031651	EM21	;	RCVR FAILED TO INTERRUPT - LINE # "
453	001560	030452	DH2	;	" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
454	001562	030550	DT2	;	\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4
455	001564	000000	0	;	PRINT ALL OCTAL
456					
457					
458					
459	001566	031715	EM22	;	CHAR AVAIL FAILED TO SET ON TIME - LINE # "
460	001570	030452	DH2	;	" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
461	001572	030550	DT2	;	\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4
462	001574	000000	0	;	PRINT ALL OCTAL
463					
464					
465					
466	001576	031771	EM23	;	BASIC DATA TEST ERROR - LINE # "
467	001600	032032	DH7	;	" (PC) (PS) (SP) TEST DEVADR CHRLNG WAS S/B "
468	001602	030550	DT2	;	\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4
469	001604	000000	0	;	PRINT ALL OCTAL
470					
471					
472					
473					
474	001606	032127	EM24	;	AUTO ECHO TEST ERROR - LINE # "
475	001610	030452	DH2	;	" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
476	001612	030550	DT2	;	\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4
477	001614	000000	0	;	PRINT ALL OCTAL
478					
479					
480					
481	001616	032167	EM25	;	BREAK BIT TEST ERROR - LINE # "
482	001620	030452	DH2	;	" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
483	001622	030550	DT2	;	\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4
484	001624	000000	0	;	PRINT ALL OCTAL
485					
486					
487					
488	001626	032227	EM26	;	HALF-DUPLEX TEST ERROR - LINE # "
489	001630	030452	DH2	;	" (PC) (PS) (SP) TEST DEVADR REGADR WAS S/B "
490	001632	030550	DT2	;	\$ERRPC,\$TMPO,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4

ERROR POINTER TABLE

001634	000000	0	:PRINT ALL OCTAL
:ERROR TABLE ITEM FOR ERROR MESSAGE 27			
001636	032271	EM27	: "UNEXPECTED BUS ERROR TRAP"
001640	032323	DH3	: (PC) (PS) (SP) TEST TRPPC TRPPS
001642	032402	DT3	: SERRPC, STMP0, \$REG6, \$REG0, \$REG1, \$REG2
001644	000000	0	:PRINT ALL OCTAL
:ERROR TABLE ITEM FOR ERROR MESSAGE 30			
001646	032420	EM30	: "UNEXPECTED R5VD INSTR TRAP"
001650	032323	DH3	: (PC) (PS) (SP) TEST TRPPC TRPPS
001652	032402	DT3	: SERRPC, STMP0, \$REG6, \$REG0, \$REG1, \$REG2
001654	000000	0	:PRINT ALL OCTAL
:ERROR TABLE ITEM FOR ERROR MESSAGE 31			
001656	032453	EM31	: "AUTO ECHO DATA COMPARE ERROR - LINE # "
001660	032523	DH4	: (PC) (PS) (SP) TEST WASADR SBADR WAS
001662	030550	DT2	: SERRPC, STMP0, \$REG6, \$REG0, \$REG1, \$REG2, \$REG3, \$REG4
001664	000000	0	:PRINT ALL OCTAL
:ERROR TABLE ITEM FOR ERROR MESSAGE 32			
001666	032620	EM32	: "AUTO ECHO TEST TIMEOUT - LINE # "
001670	032662	DH5	: (PC) (LPRG) TEST
001672	032710	DT4	: SERRPC, STMP0, STMP2
001674	000000	0	:PRINT ALL OCTAL
:ERROR TABLE ITEM FOR ERROR MESSAGE 33			
001676	032720	EM33	: "PARITY LOGIC TEST ERROR - LINE # "
001700	030452	DH2	: (PC) (PS) (SP) TEST DEVADR REGADR WAS
001702	030550	DT2	: SERRPC, STMP0, \$REG6, \$REG0, \$REG1, \$REG2, \$REG3, \$REG4
001704	000000	0	:PRINT ALL OCTAL
:ERROR TABLE ITEM FOR ERROR MESSAGE 34			
001706	032763	EM34	: "MULTI-LINE PARITY DATA TEST ERROR - LINE # "
001710	032523	DH4	: (PC) (PS) (SP) TEST WASADR SBADR WAS
001712	030550	DT2	: SERRPC, STMP0, \$REG6, \$REG0, \$REG1, \$REG2, \$REG3, \$REG4
001714	000000	0	:PRINT ALL OCTAL
:ERROR TABLE ITEM FOR ERROR MESSAGE 35			
001716	033056	EM35	: "MULTI-LINE PARITY DATA TEST TIMEOUT"
001720	033122	DH14	: (PC) (LPRG) LINACT
001722	033152	DT6	: SERRPC, STMP0, STMP3
001724	000000	0	:PRINT ALL OCTAL
:ERROR TABLE ITEM FOR ERROR MESSAGE 36			
001726	033162	EM36	: "CHAR AVAILABLE TIMEOUT"
001730	032662	DH5	: (PC) (LPRG) TEST



603	002032	033766	D15	:SERRPC \$TMP0 \$TMP1 \$REG0 \$REG1 \$REG2 \$REG3 \$REG4	
604	002034	000000	0	:PRINT ALL OCTAL	
;ERROR TABLE ITEM FOR ERROR MESSAGE 47					
609	002036	034010	EM47	: "BYTE COUNT MEMORY PATTERNS TEST ERROR - LINE # "	
610	002040	033671	DH10	: (PC) LINEWR PATRN TEST DEVADR REGADR WAS	S/B"
611	002042	033766	DT5	:SERRPC \$TMP0 \$TMP1 \$REG0 \$REG1 \$REG2 \$REG3 \$REG4	
612	002044	000000	0	:PRINT ALL OCTAL	
;ERROR TABLE ITEM FOR ERROR MESSAGE 50					
615	002046	034071	EM50	: "TEST TIMEOUT WAITING FOR XMIT DONE - LINE # "	
616	002050	030452	DH2	: (PC) (PS) (SP) TEST DEVADR REGADR WAS	S/B"
617	002052	030550	DT2	:SERRPC \$TMP0 \$REG6 \$REG0 \$REG1 \$REG2 \$REG3 \$REG4"	
618	002054	000000	0	:PRINT ALL OCTAL	
;ERROR TABLE ITEM FOR ERROR MESSAGE 51					
622	002056	034147	EM51	: "NPR LOGIC TEST 2 ERROR"	
623	002060	034176	DH11	: (PC) LINACT LINCHK TEST DEVADR REGADR WAS	S B"
624	002062	033766	DT5	:SERRPC \$TMP0 \$TMP1 \$REG0 \$REG1 \$REG2 \$REG3 \$REG4"	
625	002064	000000	0	:PRINT ALL OCTAL	
;ERROR TABLE ITEM FOR ERROR MESSAGE 52					
630	002066	034273	EM52	: "BASIC DATA COMPARE ERROR"	
631	002070	030452	DH2	: (PC) (PS) (SP) TEST DEVADR REGADR WAS	S B"
632	002072	030550	DT2	:SERRPC \$TMP0 \$REG6 \$REG0 \$REG1 \$REG2 \$REG3 \$REG4"	
633	002074	000000	0	:PRINT ALL OCTAL	
;ERROR TABLE ITEM FOR ERROR MESSAGE 53					
636	002076	034071	EM50	: "TEST TIMEOUT WAITING FOR XMIT DONE - LINE # "	
637	002100	034324	DH12	: (PC) SPEED (SP) TEST DEVADR REGADR WAS	S B"
638	002102	030550	DT2	:SERRPC \$TMP0 \$REG6 \$REG0 \$REG1 \$REG2 \$REG3 \$REG4	
639	002104	000000	0	:PRINT ALL OCTAL	
;ERROR TABLE ITEM FOR ERROR MESSAGE 54					
643	002106	031715	EM22	: "CHAR AVAIL FAILED TO SET ON TIME - LINE # "	
644	002110	034324	DH12	: (PC) SPEED (SP) TEST DEVADR REGADR WAS	S/B"
645	002112	030550	DT2	:SERRPC \$TMP0 \$REG6 \$REG0 \$REG1 \$REG2 \$REG3 \$REG4	
646	002114	000000	0	:PRINT ALL OCTAL	
;ERROR TABLE ITEM FOR ERROR MESSAGE 55					
650	002116	031715	EM22	: "CHAR AVAIL FAILED TO SET ON TIME - LINE # "	
651	002120	034421	DH13	: (PC) (PS) (SP) TEST DEVADR CHRLNG SCR WAS SCRS B	
652	002122	030550	DT2	:SERRPC \$TMP0 \$REG6 \$REG0 \$REG1 \$REG2 \$REG3 \$REG4	
653	002124	000000	0	:PRINT ALL OCTAL	
;ERROR TABLE ITEM FOR ERROR MESSAGE 56					
657	002126	034520	EM56	: "OVERRUN BIT FAILED TO SET - LINE # "	
658	002130	030452	DH2	: (PC) (PS) (SP) TEST DEVADR REGADR WAS	S B"

# E11

659	002132	030550	DT2	:SERRPC,STMPD,SREG6,SREG0,SREG1,SREG2,SREG3,SREG4"
660	002134	000000	0	:PRINT ALL OCTAL
661				
662				
663				
664	002136	034565	EM57	:"STORAGE OVERFLOW BIT FAILED) - LINE # "
665	002140	030452	OH2	:" (PC) (PS) (SP) TEST DEJADR REGADR WAS
666	002142	030550	DT2	:SERRPC,STMPD,SREG6,SREG0,SREG1,SREG2,SREG3,SREG4"
667	002144	000000	0	:PRINT ALL OCTAL

:ERROR TABLE ITEM FOR ERROR MESSAGE 57

S/B"





```

725 002464 012767 026566 175312 START1: MOV #BUSER,ERRVEC ;SET UP THE BUS ERROR VECTOR
726 002472 012767 000340 175306 MOV #340,ERRVEC+2
727 002500 012767 026642 175302 MOV #RESERR,RESVEC ;SET UP THE RSVD INSTR VECTOR
728 002506 012767 000340 175275 MOV #340,RESVEC+2
729 002514 005767 025516 TST TITFLG ;HAVE WE TYPED TITLE ONCE ^
730 002520 001012 BNE 1$ ;BR IF YES
731 002522 104401 TYPE ;GO TYPE PROGRAM TITLE
732 002524 034634 TITLE
733 002526 005167 025504 COM TITFLG ;SET FLAG - TYPE TITLE ONLY ONCE PER LOAD
734 002532 032777 000001 176400 BIT #BIT0,DSWR ;DO WE WANT TO AUTOSIZE?
735 002540 001002 BNE 1$ ;BRANCH IF NOT.
736 002542 004767 022330 JSR PC,AUTOSZ ;GO AUTOSIZE.
737 002546 005767 025116 1$: TST VCFLG ;START AT 200 ??
738 002552 001413 BEQ 11$ ;BR IF NOT
739 002554 032777 000001 176356 BIT #BIT0,DSWR ;ARE PARAMETERS TO BE INPUT MANUALLY?
740 002562 001003 BNE 9$ ;BRANCH IF YES.
741 002564 016700 025406 MOV ADRVEC,RO ;OTHERWISE, GET ADDRESSES BETWEEN VECTORS FROM AUTOSIZER
742 002570 000402 BR 10$
743 002572 004767 023250 9$: JSR PC,INPARA ;GO ASK FOR PARAMETERS
744 002576 005067 025066 10$: CLR VCFLG ;RE INIT VECTOR FLAG
745 002602 005700 11$: TST RO ;USE DEFAULT PARAMETERS ?
746 002604 001407 BEQ START2 ;BR IF YES
747 002606 022700 177777 CMP #-1,RO ;CHANGE DH SELECT PARAM ONLY ^
748 002612 001002 BNE 2$ ;BR IF NOT
749 002614 000167 023375 JMP INPAR3 ;GO ASK FOR SELECT PARAM.
750 002620 000167 023302 2$: JMP INPAR ;GO ASK FOR ALL PARAMETERS
751
752 002624 012767 027566 025364 START2: MOV #DHADTB-2,ADPTR ;GET POINTER TO ADDRESS TABLE
753 002632 012767 027626 025360 MOV #DHSVCTB-2,VCPTR ;GET POINTER TO VECTOR TABLE
754 002640 012767 027670 025354 MOV #BRLVL-2,BRPTR ;GET POINTER TO BR LEVEL TABLE
755 002646 012767 177777 025334 MOV #-1,DHNUM ;START WITH DH #00
756 002654 012767 000001 024314 MOV #1,SELMSK ;SET UP DH11 BIT TEST MARKER
757
758 002662 005267 025322 RESTAT: INC DHNUM ;GENERATE DH11 DEV NUMBER
759 002666 062767 000002 025322 ADD #2,ADPTR ;UPDATE TABLE POINTERS
760 002674 062767 000002 025316 ADD #2,VCPTR
761 002702 062767 000002 025312 ADD #2,BRPTR
762 002710 036767 024262 024262 BIT SELMSK,DHSEL ;TEST FOR SELECTED DH11
763 002716 001004 BNE RSTRTA ;BR IF SELECTED FOR TEST
764 002720 006367 024252 REST1: ASL SELMSK ;SHIFT MARKER TO TEST NEXT DH11
765 002724 001737 BEQ START2 ;BR IF 16 TESTED - START OVER
766 002726 000755 BR RESTAT ;GO TEST IF THIS ONE SELECTED
767 002730 017767 025262 024234 RSTRTA: MOV @ADPTR,DHADR ;SET UP DH11 ADDRESS
768 002736 017767 025256 024230 MOV @VCPTR,DHVCT ;SET UP THE DH11 VECTOR ENTRY
769 002744 017767 025252 025234 MOV @BRPTR,DHRLVL ;GET BR LEVEL VALUES
770 002752 004567 021616 JSR R5,SUNUM ;GO SET DH NUMBER IN THE MESSAGE BUFFER
771 002756 030210 DHNUM
772 002760 034724 TITLE2+20
773 002762 104401 TYPE ;GO PRINT "TESTING DH11 #XX"
774 002764 034704 TITLE2
775 002766 004767 021274 JSR PC,LDTBF1 ;GO LOAD XMITTR OUTPUT BUFFER WITH
776 ;BINARY COUNT PATTERN
777 002772 012767 002772 176106 MOV #.,$LPADR ;INIT SCOPE LOOP RETURN

```

# H11

MAINDE?-11-DZDMM-B  
DZDMMB.P11 TI

MACY11 27(732) 23-SEP-76 14:33 PAGE 19  
CHECK SSYN RESPONSE FROM ALL DH11 REGISTERS

SEQ 0137

```

778
779
780
781 003000 000004
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819 003002 010102
820 003004 010205
821 003006 062705 000020
822 003012 015746 174766
823 003016 012767 003044 174760
824 003024 162702 000002
825
826 003030 062702 000002
827 003034 020205
828 003036 001412
829 003040 005712
830 003042 000772
831
832 003044 004767 021240
833 003050 022626

```

```

*****
:*TEST 1 CHECK SSYN RESPONSE FROM ALL DH11 REGISTERS
*****
TST1: SCOPE
REM %
TEST ABSTRACT:
*****

```

THIS TEST ATTEMPTS TO REFERENCE EACH OF THE EIGHT REGISTERS IN THE DH11 SELECTED FOR TEST USING ITS ASSIGNED UNIBUS ADDRESS. IF ANY ADDRESS FAILS TO RESPOND A BUS ERROR TRAP VECTORS THE TEST TO THE ERROR SET-UP AND CALL ROUTINE. AFTER THE ERROR IS TYPED THE TEST WILL TEST THE NEXT DH11 ADDRESS IN SEQUENCE UNTIL ALL EIGHT ARE TESTED.

```

ERRORS:
*****
1.) [ERROR 1] REPORTS THAT THE REGISTER WHOSE ADDRESS IS IN R2 FAILED TO RESPOND WITH "SSYN" WHEN REFERENCED.

```

```

SYNC: (NONE)
*****

```

```

DEBUG:
*****
1.) PROBLEM IS MOST LIKELY THE M7277 MODULE.
2.) IF ALL EIGHT REGISTERS FAIL TO RESPOND, MAKE SURE THAT YOU CONFIGURED THE PROGRAM PROPERLY BEFORE STARTING. IF YOU DID, CHECK THE SETTINGS OF THE ADDRESS SELECT JUMPERS ON THE M7277 MODULE.
3.) IF ONE OR MORE RESPONDED PROPERLY, SET UP AN ERROR SCOPE LOOP AND BACKTRACK THROUGH THE LOGIC STARTING WITH THE KEY LOGIC SIGNALS LISTED BELOW.

```

```

KEY LOGIC:
*****

```

	M7277	SH3	SSYN H	CE2
		SH4	DEVICE RESPONDING L	E72-6
			DEVICE SELECTED H	E09-11
%				
	MOV	R1,R2		:COPY IT INTO R2
	MOV	R2,R5		:ALSO R5
	ADD	#20,R5		:R5 WILL TELL US WHEN WE'VE TESTED ALL 8
	MOV	ERRVEC, -(SP)		:SAVE BUS ERROR VECTOR
	MOV	#3\$,ERRVEC		:GO TO 3\$ IF REG FAILS TO RESPOND
	SUB	#2,R2		:SO WE START WITH FIRST REG
1\$:	ADD	#2,R2		:POINT TO A DH11 REGISTER
	CMP	R2,R5		:TESTED ALL EIGHT ?
	BEG	4\$		:BR IF YES
2\$:	TST	(R2)		:ACCESS DH11 REG ADDR
	BR	1\$		:BR WHEN ALL 8 ARE DONE
3\$:	JSR	PC,SUER1		:GO SET UP ERROR INFO
	CMP	(SP)+,(SP)+		:FIX SP BECAUSE OF TRAP

MAINDEC-11-DZDMM-8  
DZDHMB.P11 T1

MACY11 27(732) 23-SEP-76 14:33 PAGE 20  
CHECK SSYN RESPONSE FROM ALL DH11 REGISTERS

SEQ 0138

834	003052	012767	003040	176030		MOV	#2\$.SLPERR		;SET UP ERROR LOOP RETURN
835	003060	104001				ERROR	1		;DH11 REGISTER FAILED TO RESPOND TO MSYN
836									
837	003062	000762				BR	1\$		;GO TEST NEXT ONE
838	003064	012667	174714		4\$:	MOV	(SP)+.ERRVEC		;RESTORE BUS ERROR VECTOR

839  
840  
841  
842 003070 000004  
843  
844  
845  
846  
847  
848  
849  
850  
851  
852  
853  
854  
855  
856  
857  
858  
859  
860  
861  
862  
863  
864  
865  
866  
867  
868  
869  
870  
871  
872  
873  
874  
875  
876  
877  
878  
879  
880  
881  
882  
883  
884  
885  
886  
887  
888  
889  
890  
891  
892  
893  
894

::\*\*\*\*\*  
:\*TEST 2 TEST THAT "MASTER CLR" CAN CLEAR THE "SCR", "LPR", "BKR", AND "SSR" REGS  
:\*\*\*\*\*

TST2: SCOPE  
.REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST SETS ALL WRITEABLE BITS IN THE TARGET REGISTER (SCR, LPR, BKR, AND SSR) THEN SETS BIT11 IN THE "SCR" (MASTER CLEAR) AND CHECKS THAT IT INDEED CLEARED ALL BITS IN THE TARGET REGISTER. IT PERFORMS THIS SEQUENCE FOR ALL TARGET REGISTERS. IF A REGISTER FAILS TO CLEAR PROPERLY, THE ERROR IS REPORTED, AND THEN THE ROUTINE TESTS THE NEXT REGISTER IN SEQUENCE.

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 3] REPORTS THAT THE REGISTER WHOSE ADDRESS IS IN R2 FAILED TO CLEAR WHEN MASTER CLEAR WAS ACTIVATED.

SYNC:  
\*\*\*\*\*

M7289 SH6 SCR 11 H (MASTER CLEAR) FK2

DEBUG:  
\*\*\*\*\*

- 1.) IF THE ERROR REPORTS INDICATE THAT ALL REGISTERS ARE FAILING, ESTABLISH AN ERROR SCOPE LOOP AND PROCEED TO BACKTRACK THROUGH THE KEY LOGIC SIGNALS LISTED BELOW.
- 2.) IF ONLY ONE REGISTER FAILS WITH ALL SET BITS -- THEN LET TESTS 03-10 RUN -- THEY WILL PROBABLY GIVE BETTER ISOLATION. USE ONE OF THESE TESTS TO DEBUG THE FAULT.

KEY LOGIC:  
\*\*\*\*\*

M7277 SH3 INIT A L FR2  
INIT B L FM2  
INIT A H EF2  
INIT B H FV2  
SH4 LOAD SCR HIGH BYTE H CP1  
M7289 SH6 SCR 11 H (MASTER CLEAR) FK2  
M7278 SH3 BUFF DATA 11 H AA1

%  
MOV #MSTCLR, R5 ;GET POINTER TO ADDRESS TABLE  
MOV R1, (R5)+ ;SET UP THE TEST ADDRESS TABLE SO THAT  
MOV R1, (R5)+ ;IT CONTAINS THE ADDRESSES OF THE  
MOV R1, (R5)+ ;SCR, LPR, BKR, AND SSR REGISTERS  
MOV R1, (R5)+  
ADD #SSR, -(R5) ;GENERATE SSR ADDRESS  
ADD #BKR, -(R5) ;GENERATE BKR ADDRESS



# K11

MAINDEC-11-DZDHM-B  
DZDHMB.P11 T2

MACY11 27(732) 23-SEP-76 14:33 PAGE 22  
TEST THAT "MASTER CLR" CAN CLEAR THE "SCR", "LPR", "BKR", AND "SSR" REGS

SEQ 0140

895	003116	062745	000004		ADD	#LPR, -(R5)	; GENERATE LPR ADDRESS
896	003122	005745			TST	-(R5)	; POINT R5 TO FIRST ADDR ENTRY (SCR)
897	003124	005004			CLR	R4	; RESULT S/B 000000 AFTER MASTER CLEAR
898							
899	003126	012502		1\$:	MOV	(R5)+, R2	; GET REG ADDRESS
900	003130	022705	027220		CMP	#MSTCLR+10, R5	; DONE ALL FOUR REGS ??
901	003134	001415			SEQ	TST3	; BR IF YES
902	003136	012712	177777	2\$:	MOV	#-1, (R2)	; SET 1'S IN REGISTER
903	003142	052711	004000		BIS	#BIT11, (R1)	; ISSUE MASTER CLEAR
904	003146	011203			MOV	(R2), R3	; GET CONTENT OF REGISTER
905	003150	001766			BEQ	1\$	; BR IF IT'S ALL ZEROES
906							
907	003152	004767	021172		JSR	PC, SUER2	; GO SET UP ERROR INFO
908	003156	012767	003136	175724	MOV	#2\$, \$LPERR	; SET UP ERROR LOOP RETURN
909	003164	104003			ERROR	3	; MASTER CLR FAILED TO CLR SEL. REG.
910	003166	000757			BR	1\$	; GO TEST NEXT REGISTER

911  
912  
913  
914 003170 000004  
915  
916  
917  
918  
919  
920  
921  
922  
923  
924  
925  
926  
927  
928  
929  
930  
931  
932  
933  
934  
935  
936  
937  
938  
939  
940  
941  
942  
943  
944  
945  
946  
947  
948  
949  
950  
951  
952  
953  
954  
955  
956  
957  
958  
959  
960  
961  
962  
963  
964  
965  
966

\*\*\*\*\*  
\*TEST 3 TEST "SCR" REG R/W BITS CAN SET/CLR (NORMAL MODE)  
\*\*\*\*\*

TST3: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT EACH R/W BIT IN THE "SCR" REGISTER CAN BE INDIVIDUALLY SET AND CLEARED IN NORMAL MODE (MAINT BIT = 0) A BIT MASK (RGMSK1: 131177) IS USED TO DEFINE THE R/W BITS ( ALL BUT BITS 14, 11, 10, 8, AND 7). THE TEST IS REPEATED ELEVEN TIMES WITH A DIFFERENT BIT SELECTED FOR EACH TEST. RS CONTAINS THE BIT CURRENTLY BEING TESTED. IF AN ERROR IS DETECTED, IT IS REPORTED AND THEN THE TEST RESUMES WITH THE NEXT BIT IN SEQUENCE UNTIL ALL HAVE BEEN TESTED.

ERRORS:  
\*\*\*\*\*

1.) [ERROR 2] IS CALLED TO REPORT A FAILURE TO SET PROPERLY AND AGAIN TO REPORT A FAILURE TO CLEAR PROPERLY.

SYNC:  
\*\*\*\*\*

- 1.) SET FAILURE M7277 SH4 LOAD SSR LOW BYTE H CR1
- 2.) CLR FAILURE M7277 SH4 LOAD SSR HIGH BYTE H CP2

DEBUG:  
\*\*\*\*\*

- 1.) IF ALL BITS FAIL - SUSPECT THE "LOAD SCR" SIGNALS ON THE M7277 SH4.
- 2.) IF ONLY ONE OR TWO BITS FAIL - SUSPECT EITHER THE "SCR" REGISTER FLOPS ON THE M7289 SH6, THE BUS RECEIVERS ON THE M7278 SH3 AND SH4, OR THE MULTIPLEXORS AND BUS DRIVERS ON THE M7289 SH5-8.

KEY LOGIC:  
\*\*\*\*\*

M7278	SH3	BUF DATA <15:08> H	
	SH4	BUF DATA <07:00> H	
M7277	SH4	LOAD SCR LOW BYTE H	CT2
		LOAD SCR HIGH BYTE H	CP1
		DATA TO BUS H	EN2
		DATA SOURCE <A,B,C> H	DUI.DJ2.DT2
M7289	SH5	BUF DATA TO BUS B H	E05-12
	SH6	BUS DATA <15:12> L	
		BUS DATA <11:08> L	
	SH7	SCR <15:00> H	
		BUF DATA TO BUS A H	E05-8
		BUS DATA <07:04> L	
	SH8	BUS DATA <03:00> L	

%

## M11

MAINDEC-11-DZDHM-B  
DZDHMB.P11 T3

MACY11 27(732) 23-SEP-76 14:33 PAGE 24  
TEST "SCR" REG R/W BITS CAN SET/CLR (NORMAL MODE)

SEQ 0142

967	003172	012767	003222	175710		MOV	#4\$, \$LPERR	;SET UP ERROR LOOP RETURN
968	003200	010102				MOV	R1, R2	;GET REGISTER ADDRESS
969	003202	012705	000001			MOV	#1, R5	;SET UP TO START WITH BIT00
970								
971	003206	030567	024340		1\$:	BIT	R5, RGMSK1	;SHALL WE TEST THIS BIT ?
972	003212	001003				BNE	4\$	;BR IF YES
973	003214	006305			2\$:	ASL	R5	;SHIFT TO TST NEXT BIT
974	003216				3\$:			
975	003216	001430				BEQ	TST4	; <BR IF DONE ALL R/W BITS>
976	003220	000772				BR	1\$	;GO TEST NEXT BIT
977								
978	003222	010504			4\$:	MOV	R5, R4	;RESULT S/B IN R4
979	003224	005012				CLR	(R2)	;INIT REG BEING TESTED
980	003226	112761	000000	000016		MOVB	#0, SSR(R1)	;SCOPE SYNC
981	003234	010512				MOV	R5, (R2)	;SET THE BIT
982	003236	011203				MOV	(R2), R3	;GET THE WAS DATA
983	003240	020403				CMP	R4, R3	;RESULT = S/B DATA ??
984	003242	001403				BEQ	5\$	;BR IF YES
985								
986	003244	004767	021100			JSR	PC, SUER2	;GO SET UP ERROR INFO
987	003250	104002				ERROR	2	;SELECTED BIT FAILED TO SET IN SCR
988								
989	003252	005004			5\$:	CLR	R4	;SET UP TO CLEAR THE BIT S/B=000000
990	003254	112761	000000	000017		MOVB	#0, SSR+1(R1)	;SCOPE SYNC
991	003262	040512				BIC	R5, (R2)	;CLR THE SELECTED BIT
992	003264	011203				MOV	(R2), R3	;GET THE WAS DATA
993	003266	001403				BEQ	6\$	;BR IF IT CLEARED
994								
995	003270	004767	021054			JSR	PC, SUER2	;GO SET UP THE ERROR INFO
996	003274	104002				ERROR	2	;SELECTED BIT FAILED TO CLEAR IN SCR
997	003276	000746			6\$:	BR	2\$	;GO SELECT NEXT BIT

998  
999  
1000  
1001 003300 000004  
1002  
1003  
1004  
1005  
1006  
1007  
1008  
1009  
1010  
1011  
1012  
1013  
1014  
1015  
1016  
1017  
1018  
1019  
1020  
1021  
1022  
1023  
1024  
1025  
1026  
1027  
1028  
1029  
1030  
1031  
1032  
1033  
1034  
1035 003302 010102  
1036 003304 012705 000001  
1037 003310 030567 024240  
1038 003314 001003  
1039 003316 006305  
1040 003320 001420  
1041 003322 000772  
1042  
1043 003324 005004  
1044 003326 005012  
1045 003330 112761 000000 000016  
1046 003336 010512  
1047 003340 011203  
1048 003342 001765  
1049  
1050 003344 004767 021000  
1051 003350 012767 003324 175532  
1052 003356 104002  
1053 003360 000756

\*\*\*\*\*  
:TEST 4 TEST "SCR" REG. READ ONLY BITS (NORMAL MODE)  
\*\*\*\*\*  
TST4: SCOPE  
.REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT THE "SCR" REGISTER READ ONLY BITS CAN NOT BE SET OR CLEARED IN NORMAL MODE. A BIT MASK (RGMSK2: 046600) IS USED TO DEFINE THE READ ONLY BITSS (14,11,10,8, AND 7). THE TEST IS REPEATED FIVE TIMES, ONCE FOR EACH BIT TO BE TESTED, AND ANY ERRORS DETECTED ARE REPORTED. AFTER THE ERROR REPORT THE TEST RESUMES WITH THE NEXT BIT IN SEQUENCE UNTIL ALL BITS HAVE BEEN TESTED.

ERRORS:  
\*\*\*\*\*

1.) [ERROR 2] IS CALLED TO REPORT ANY READ ONLY BIT THAT FAILED TO RESPOND PROPERLY.

SYNC:  
\*\*\*\*\*

M7277 SH4 LOAD SSR LOW BYTE H CR1

DEBUG:  
\*\*\*\*\*

SAME AS FOR TEST 03

KEY LOGIC:  
\*\*\*\*\*

SAME AS FOR TEST 03

%  
MOV R1,R2 ;MAKE IT THE REG. ADDR ALSO  
MOV #1,R5 ;INIT BIT TEST MARKER  
1\$: BIT R5, RGMSK2 ;IS IT A READ ONLY BIT ?  
BNE 3\$ ;BR IF IT IS - GO TEST IT  
2\$: ASL R5 ;SHIFT BIT MARKER  
BEQ TST5 ;BR IF DONE ALL BITS  
BR 1\$ ;GO TEST THIS BIT  
3\$: CLR R4 ;RESULT S/B = 000000  
CLR (R2) ;INIT REG BEING TESTED  
MOV #0, SSR(R1) ;SCOPE SYNC  
MOV R5, (R2) ;ATTEMPT TO SET A READ ONLY BIT  
MOV (R2), R3 ;GET THE WAS DATA  
BEQ 2\$ ;BR IF THE BIT DIDN'T SET  
JSR PC, SUER2 ;GO SET UP ERROR INFO  
MOV #3\$, \$LPERR ;SET UP ERROR LOOP RETURN ADDR  
ERROR 2 ;READ ONLY BIT SET IN "SCR"  
BR 2\$ ;CONTINUE WITH NEXT BIT





```

1110
1111
1112
1113
1114
1115 003364 012767 003414 175516
1116 003372 010102
1117 003374 012705 000001
1118 003400 030567 024160 1S:
1119 003404 001003
1120 003406 006305 2S:
1121 003410 001457
1122 003412 000772
1123
1124
1125 003414 010504 3S:
1126 003416 052704 001003
1127 003422 005012
1128 003424 052712 001000
1129 003430 112761 000000 000016
1130 003436 050512
1131 003440 011203
1132 003442 020304
1133 003444 001404
1134
1135 003446 004767 020676
1136 003452 104002
1137 003454 000754
1138
1139 003456 042712 001000 4S:
1140 003462 042704 001000
1141 003466 112761 000500 000017
1142 003474 040512
1143 003476 011203
1144 003500 020304
1145 003502 001404
1146
1147 003504 004767 020640
1148 003510 104002
1149 003512 000735
1150
1151 003514 012704 001000 5S:
1152 003520 050412
1153 003522 012761 000000 000004
1154 003530 040512
1155 003532 011203
1156 003534 020304
1157 003536 001723
1158
1159 003540 004767 020604
1160 003544 104002
1161 003546 000717

```

SAME AS TEST 03 WITH THE FOLLOWING ADDITION

M7289 SH4 74121 ONE-SHOTS E35-6, E23-6

```

MOV #35, $LPERR ;SET UP THE ERROR LOOP RETURN
MOV R1, R2 ;MAKE IT REG ADDR TOC
MOV #1, R5 ;INIT BIT TEST MARKER
BIT R5, RGMSK6 ;IS IT A READ ONLY BIT ??
BNE 3S ;BR IF YES - TEST IT
ASL R5 ;SHIFT THE BIT MARKER
BEQ TST6 ;BR IF DONE ALL SELECTED BITS
SR 1S ;GO TEST FOR THIS BIT

MOV R5, R4 ;SET UP S/B DATA
BIS #BIT09, R4 ;PUT IN THE MAINT. BIT
CLR (R2) ;INIT REG BEING TESTED
BIS #BIT09, (R2) ;TURN ON MAINT. MODE
MOVB #0, SSR(R1) ;SCOPE SYNC
BIS R5, (R2) ;SET THE SELECTED BIT
MOV (R2), R3 ;GET THE WAS DATA
CMP R3, R4 ;DID SELECTED BIT GET SET ??
BEQ 4S ;BR IF IT DID

JSR PC, SUER2 ;GO SET UP ERROR INFO
ERROR 2 ;SELECTED BIT FAILED TO SET IN MAINT MODE
BR 2S ;GO TEST NEXT BIT

BIC #BIT09, (R2) ;TURN OFF MAINT. MODE
BIC #BIT09, R4 ;CLR MAINT BIT IN S/B DATA
MOVB #0, SSR+1(R1) ;SCOPE SYNC
BIC R5, (R2) ;ATTEMPT TO CLR SELECTED BIT
MOV (R2), R3 ;GET THE WAS DATA
CMP R3, R4 ;DID BIT GET CLEARED ??
BEQ 5S ;BR IF IT DIDN'T

JSR PC, SUER2 ;GO SET UP ERROR INFO
ERROR 2 ;SELECTED BIT GOT CLEARED WITH MAINT MODE OFF
BR 2S ;GO TEST NEXT BIT

MOV #BIT09, R4 ;SET UP S/B DATA
BIS R4, (R2) ;SET MAINT. MODE
MOV #0, LPR(R1) ;SCOPE SYNC
BIC R5, (R2) ;NOW CLR SELECTED BIT
MOV (R2), R3 ;GET THE WAS DATA
CMP R3, R4 ;DID BIT GET CLEARED OK ??
BEQ 2S ;BR IF YES

JSR PC, SUER2 ;GO SET UP ERROR INFO
ERROR 2 ;FAILED TO CLR SELECTED BIT IN MAINT MODE
BR 2S ;GO SELECT NEXT BIT FOR TEST

```

1161  
1162  
1163  
1164  
1165  
1166  
1167  
1168  
1169  
1170  
1171  
1172  
1173  
1174  
1175  
1176  
1177  
1178  
1179  
1180  
1181  
1182  
1183  
1184  
1185  
1186  
1187  
1188  
1189  
1190  
1191  
1192  
1193  
1194  
1195  
1196  
1197  
1198  
1199  
1200

003550 000004

::\*\*\*\*\*  
:TEST 6 TEST THAT ALL R/W BITS IN "LPR" CAN BE SET/CLR  
:\*\*\*\*\*  
TST6: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT ALL R/W BITS IN THE "LPR" REGISTER CAN BE SET AND CLEARED INDIVIDUALLY. A BIT MASK (RGMSK3: 177767) IS USED TO DEFINE THE BITS TO BE TESTED (ALL BUT BIT03). THE TEST SEQUENCE IS AS FOLLOWS:

1. SELECT A BIT TO TEST
2. SET THE BIT AND VERIFY IT SET
3. CLEAR THE BIT AND VERIFY IT CLEARED
4. REPEAT 1 THRU 3 UNTIL ALL BITS TESTED

ANY ERRORS DETECTED ARE REPORTED AND AFTER THE ERROR, THE TEST RESUMES WITH THE NEXT BIT IN SEQUENCE.

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 4] IS CALLED TO REPORT BOTH FAIL TO SET AND FAIL TO CLEAR FAULTS.

SYNC:  
\*\*\*\*\*

- 1.) FAIL TO SET: M7277 SH4 LOAD SSR LOW BYTE H CR1
- 2.) FAIL TO CLEAR: M7277 SH4 LOAD SSR HIGH BYTE H CP2

DEBUG:  
\*\*\*\*\*

- 1.) IF ALL BITS FAIL THE PROBLEM IS MOST LIKELY THE M7277 MODULE (LPR LOAD SIGNALS)
- 2.) IF NOT THEN IT IS PROBABLY AN "LPR" REGISTER CHIP OR BAD OUTPUT DATA MUX CHIP, BOTH ON THE M7278 MODULE.

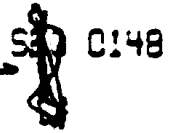
KEY LOGIC:  
\*\*\*\*\*

M7277	SH4	LOAD LPR H	EP2
M7278	SH5	LPR <15:12> L	(E52)
	SH6	LPR <11:08> L	(E37)
	SH7	LPR <07:04> L	(E59)
	SH8	LPR <03:00> L	(E61)
	SH5.6.7.9	OUTPUT MUX CHIPS	(74151'S PIN 2)

003552 012767 003606 175330  
003560 010102  
003562 062702 000004

MOV #35,\$LPERR ;SET UP THE ERROR LOOP RETURN  
MOV R1,R2 ;COPY IT IN R2  
ADD #LPR,R2 ;GENERATE REGADR IN R2

12291	003566	012705	000001		MOV	#1,R5	:INIT BIT TEST MARKER
12292	003576	030567	023760	1\$:	BIT	R5,RGMSK3	:TEST THIS BIT ??
12293	003576	001003			BNE	2\$	:BR IF YES
12294	003600	006305		2\$:	ASL	R5	:SHIFT THE MARKER
12295	003602	001430			BEQ	1\$	:BR IF DONE ALL BITS
12296	003604	000772			BR	1\$	:GO TEST NXT BIT
12297	003606	010504		3\$:	MOV	R5,R4	:SET UP S/B DATA
12298	003610	005012			CLR	(R2)	:INIT REG BEING TESTED
12299	003612	112767	000000	000016	MOV	#0,SSR,R1	:SCOPE SYNC
12300	003620	010512			MOV	R5,(R2)	:SET LPR BIT
12301	003622	011133			MOV	(R2),R3	:GET THE WAS DATA
12302	003624	020304			CMP	R3,R4	:DID IT SET
12303	003626	001403			BEQ	4\$	:BR IF IT SET PROPERLY
12304	003630	004767	020514		JSR	PC,SUER2	:GO SET UP ERROR INFO
12305	003634	104004			ERROR	4	:LPR BIT FAILED TO SET PROPERLY
12306	003636	005004		4\$:	CLR	R4	:GET READY TO CLEAR SELECTED BIT
12307	003640	112767	000000	000017	MOV	#0,SSR+1(R1)	:SCOPE SYNC
12308	003646	040512			BIC	R5,(R2)	:CLEAR THE BIT
12309	003650	011203			MOV	(R2),R3	:GET THE WAS DATA
12310	003652	001752			BEQ	2\$	:BR IF BIT CLEARED PROPERLY
12311	003654	004767	020470		JSR	PC,SUER2	:GO SET UP ERROR INFO
12312	003660	104004			ERROR	4	:LPR BIT FAILED TO CLEAR PROPERLY
12313	003662	000746			BR	2\$	:GO SELECT NEXT BIT



1244  
1245  
1246  
1247 003664 000004  
1248  
1249  
1250  
1251  
1252  
1253  
1254  
1255  
1256  
1257  
1258  
1259  
1260  
1261  
1262  
1263  
1264  
1265  
1266  
1267  
1268  
1269  
1270  
1271  
1272  
1273  
1274  
1275  
1276  
1277  
1278  
1279  
1280  
1281  
1282  
1283  
1284  
1285  
1286  
1287  
1288  
1289  
1290  
1291  
1292  
1293  
1294  
1295  
1296  
1297  
1298 003666 012767 003722 175214  
1299 003674 010102

```
::*****  
:*TEST 7 TEST THAT ALL R/W BITS IN "BKR" CAN BE SET/CLR  
:*****  
TST7: SCOPE  
REM %  
TEST ABSTRACT:  
*****
```

THIS TEST VERIFIES THAT ALL BITS IN THE BREAK CONTROL REGISTER CAN BE SET AND CLEARED INDIVIDUALLY. IT USES A BIT MASK (RGMSK4: 177777) TO DEFINE THE R/W BITS (ALL 16.). R5 ALWAYS CONTAINS THE BIT CURRENTLY SELECTED FOR TEST. THE TEST SEQUENCE IS AS FOLLOWS:

1. SELECT A BIT TO TEST
2. SET THE BIT AND VERIFY THAT IT SET PROPERLY
3. CLEAR THE BIT AND VERIFY THAT IT CLEARED PROPERLY
4. REPEAT 1 THRU 4 UNTIL ALL BITS HAVE BEEN TESTED.

ANY ERROR DETECTED IS REPORTED AND THE TEST RESUMES WITH THE NEXT BIT IN SEQUENCE.

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 5] IS CALLED TO REPORT BOTH FAIL TO SET PROPERLY AND FAIL TO CLEAR PROPERLY FAULTS.

SYNC:  
\*\*\*\*\*

- 1.) FAIL TO SET: M7277 SH4 LOAD SSR LOW BYTE H CR1
- 2.) FAIL TO CLR: M7277 SH4 LOAD SSR HIGH BYTE H CP2

DEBUG:  
\*\*\*\*\*

- 1.) THE ONLY DIFFERENCES IN THE DATA PATH HERE AND THAT FOR THE PREVIOUS TESTS ARE THE ACTUAL REGISTER CHIPS AND THE INPUT SELECTED ON THE OUTPUT DATA MULTIPLEXORS.
- 2.) IF ALL BITS FAIL THE PROBLEM IS MOST LIKELY THE M7277.
- 3.) IF ONLY ONE OR TWO FAIL THE PROBLEM IS MOST LIKELY THE M7279.

KEY LOGIC:  
\*\*\*\*\*

```
M7277 SH4 LOAD BCR H FU1  
DATA TO BUS H EN2  
DATA SOURCE (A,B,C) H DU1,DU2,DT2
```

```
M7278 SH5 - SH8 74175 REGISTER CHIPS (E51,E38,E67,E60)  
SH5 - SH8 74151'S MUX CHIPS INPUT PIN 13
```

```
%  
MOV #3$, $LPERR :SET UP THE ERROR LOOP RETURN  
MOV R1,R2 :GENERATE "BKR" ADDRESS IN R2
```

MAINDEC-11-DZDMM-B  
DZDMMB.P11 17

MAY11 27(732) 23-SEP-76 14:33 PAGE 31  
TEST THAT ALL R/W BITS IN "BKR" CAN BE SET/CLR

SEQ 0149

1300	003576	052702	000014		ADD	#BKR,R2		
1301	003702	012705	000001		MOV	#1,R5		:INIT BIT TEST MARKER
1302	003706	030567	023646		BIT	R5,RGMSK4	1\$:	:TEST THIS BIT ??
1303	003712	001003			BNE	3\$		:BR IF YES
1304	003714	006305			ASL	R5	2\$:	:SHIFT BIT MARKER
1305	003716	001430			BEQ	TST10		:BR IF ALL BITS TESTED
1306	003720	000772			BR	1\$		:GO TEST THE BIT
1307								
1308	003722	010504			MOV	R5,R4	3\$:	:SET UP S/B DATA
1309	003724	005012			CLR	(R2)		:INIT REG BEING TESTED
1310	003726	112761	000000	000016	MOVB	#0,SSR(R1)		:SCOPE SYNC
1311	003734	050512			BIS	R5,(R2)		:SET THE SELECTED BIT IN "BKR"
1312	003736	011203			MOV	(R2),R3		:GET THE WAS DATA
1313	003740	020304			CMP	R3,R4		:DID BIT SET OK
1314	003742	001403			BEQ	4\$		:BR IF YES
1315								
1316	003744	004767	020400		JSR	PC,SUER2		:GO SET UP ERROR INFO
1317	003750	104005			ERROR	5		:BKR BIT FAILED TO SET PROPERLY
1318								
1319	003752	005004			CLR	R4	4\$:	:SET UP S/B DATA
1320	003754	112761	000000	000017	MOVB	#0,SSR+1(R1)		:SCOPE SYNC
1321	003752	040512			BIC	R5,(R2)		:CLEAR BKR BIT
1322	003764	011203			MOV	(R2),R3		:GET THE BKR WAS DATA
1323	003766	001752			BEQ	2\$		:BR IF BKR BIT CLEARED OK
1324								
1325	003770	004767	020354		JSR	PC,SUER2		:GO SET UP ERROR INFO
1326	003774	104005			ERROR	5		:BKR BIT FAILED TO CLR PROPERLY
1327	003776	000746			BR	2\$		:GO SELECT NEXT BIT

1328  
1329  
1330  
1331 004000 000004  
1332  
1333  
1334  
1335  
1336  
1337  
1338  
1339  
1340  
1341  
1342  
1343  
1344  
1345  
1346  
1347  
1348  
1349  
1350  
1351  
1352  
1353  
1354  
1355  
1356  
1357  
1358  
1359  
1360  
1361  
1362  
1363  
1364  
1365  
1366  
1367  
1368  
1369  
1370  
1371  
1372  
1373  
1374  
1375  
1376  
1377  
1378  
1379  
1380  
1381  
1382  
1383

\*\*\*\*\*  
\*TEST 10 TEST THAT ALL P/W BITS IN "SSR" CAN BE SET/CLR  
\*\*\*\*\*  
\*TST10: SCOPE  
\*REM %  
\*TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT ALL R/W BITS IN THE SILO STATUS REGISTER (SSR) CAN BE SET AND CLEARED INDIVIDUALLY. IT USES A BIT MASK (RGMSK5: 100077) TO DEFINE THE R/W BITS (15,5,4,3,2,1 AND 0). R5 ALWAYS CONTAINS THE BIT CURRENTLY SELECTED FOR TEST. THE TEST SEQUENCE IS AS FOLLOWS:

- 1. SELECT A BIT TO TEST
- 2. SET THE BIT AND VERIFY THAT IT SET PROPERLY
- 3. CLEAR THE BIT AND VERIFY THAT IT CLEARED PROPERLY
- 4. REPEAT 1 THRU 3 UNTIL ALL BITS ARE TESTED

ANY ERRORS DETECTED ARE REPORTED AND THEN THE TEST RESUMES WITH THE NEXT BIT IN SEQUENCE.

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 6] IS CALLED TO REPORT BOTH FAIL TO SET PROPERLY AND FAIL TO CLEAR PROPERLY FAULTS.

SYNC:  
\*\*\*\*\*

- 1.) FAIL TO SET: M7277 SH4 LOAD LPR H EP2
- 2.) FAIL TO CLR: M7277 SH4 LOAD BCR H FU1

DEBUG:  
\*\*\*\*\*

- 1.) THE ONLY DIFFERENCES BETWEEN THEE DATA PATHS USED BY THIS TEST AND THAT USED BY THE PREVIOUS TESTS ARE THE ACTUAL "SSR" REGISTER CHIPS AND THE INPUT PIN SELECTED ON THE OUTPUT DATA MULTIPLEXORS.
- 2.) IF ALL BITS FAIL IT IS MOST LIKELY THE M7277
- 3.) IF BITS <13:08> FAIL IT IS MOST LIKELY THE M7279
- 4.) IF JUST ONE OR TWO BITS FAIL IT IS MOST LIKELY THE M7278

KEY LOGIC:  
\*\*\*\*\*

M7277	SH4	LOAD SSR LOW BYTE H	CR1
		LOAD SSR HIGH BYTE H	CP2
		DATA TO BUS H	EN2
		DATA SOURCE (A,B,C) H	DUI,DU2,DT2
M7279	SH2	SSR <13:08> H	(E20 AND E24)
M7278	SH5 - SH8	REGISTER CHIPS E53,E68, OR E69 (74175'S)	OUTPUT MUX CHIPS - (74151'S PIN 12)

%

MAINDEC-11-DZDMM-B  
DZDMMB.P11 T10

MACY11 27(732) 23-SEP-76 14:33 PAGE 33  
TEST THAT ALL R/W BITS IN "SSR" CAN BE SET/CLR

SEQ 0151

1384	004002	012767	004036	175100		MOV	#3\$, \$LPERR	;SET UP THE ERROR LOOP RETURN
1385	004010	010102				MOV	R1, R2	;GENERATE "SSR" ADDRESS IN R2
1386	004012	062702	000016			ADD	#SSR, R2	
1387	004016	012705	000001			MOV	#1, R5	;INIT BIT TEST MARKER
1388	004022	030567	023534		1\$:	BIT	R5, RGMSKS	;TEST THIS BIT ??
1389	004026	001003				BNE	3\$	;BR IF YES
1390	004030	006305			2\$:	ASL	R5	;SHIFT BIT MARKER
1391	004032	001435				BEQ	TST11	;BR IF ALL BITS TESTED
1392	004034	000772				BR	1\$	;GO TEST THE BIT
1393								
1394	004036	010504			3\$:	MOV	R5, R4	;SET UP S/B DATA
1395	004040	005012				CLR	(R2)	;INIT REG BEING TESTED
1396	004042	012761	000000	000004		MOV	#0, LPR(R1)	;SCOPE SYNC
1397	004050	050512				BIS	R5, (R2)	;SET THE SELECTED BIT IN "SSR"
1398	004052	011203				MOV	(R2), R3	;GET THE WAS DATA
1399	004054	042703	077700			BIC	#77700, R3	;CLEAR OUT DON'T CARE BITS
1400	004060	020304				CMP	R3, R4	;DID BIT SET OK
1401	004062	001403				BEQ	4\$	;BR IF YES
1402								
1403	004064	004767	020260			JSR	PC, \$UER2	;GO SET UP ERROR INFO
1404	004070	104006				ERROR	E	;SSR BIT FAILED TO SET PROPERLY
1405								
1406	004072	005004			4\$:	CLR	R4	;SET UP S/B DATA
1407	004074	012761	000000	000014		MOV	#0, BKR(R1)	;SCOPE SYNC
1408	004102	040512				BIC	R5, (R2)	;CLEAR SSR BIT
1409	004104	011203				MOV	(R2), R3	;GET THE SSR WAS DATA
1410	004106	042703	077700			BIC	#77700, R3	;CLEAR JUNK BITS
1411	004112	020304				CMP	R3, R4	;DID THE SSR BIT GET CLEARED ??
1412	004114	001745				BEQ	2\$	;BR IF SSR BIT CLEARED OK
1413								
1414	004116	004767	020226			JSR	PC, \$UER2	;GO SET UP ERROR INFO
1415	004122	104006				ERROR	6	;SSR BIT FAILED TO CLR PROPERLY
1416	004124	000741				BR	2\$	;GO SELECT NEXT BIT



1417  
1418  
1419  
1420 004126 000004  
1421  
1422  
1423  
1424  
1425  
1426  
1427  
1428  
1429  
1430  
1431  
1432  
1433  
1434  
1435  
1436  
1437  
1438  
1439  
1440  
1441  
1442  
1443  
1444  
1445  
1446  
1447  
1448  
1449  
1450  
1451  
1452  
1453  
1454  
1455  
1456  
1457  
1458  
1459  
1460  
1461 004130 012767 004164 174752  
1462 004136 010102  
1463 004140 062702 000004  
1464 004144 012705 000001  
1465 004150 030567 023402  
1466 004154 001003  
1467 004156 006305  
1468 004160 001436  
1469 004162 000772  
1470  
1471 004164 016704 023366  
1472 004170 005012

\*\*\*\*\*  
:TEST 11 TEST THAT CLR/SET OF BIT "N" IN "LPR" DOES NOT CLEAR ANY OTHER BITS  
\*\*\*\*\*

TST11: SCOPE  
.REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT SETTING AND CLEARING EACH R/W BIT IN THE "LPR" REGISTER DOES NOT DISTURB (CLEAR) ANY OTHER BIT IN THE REGISTER. A BIT MASK (RGMSK3: 177767) IS USED TO DEFINE THE R/W BITS (ALL BUT BIT 03). R5 ALWAYS CONTAINS THE BIT CURRENTLY SELECTED FOR TEST. THE TEST SEQUENCE IS AS FOLLOWS:

- 1. SELECT A BIT TO TEST
- 2. SET ALL THE WRITABLE BITS
- 3. CLEAR THE SELECTED BIT - VERIFY IT CLEARED PROPERLY
- 4. SET THE SELECTED BIT - VERIFY IT SET PROPERLY
- 5. REPEAT 1 THRU 4 UNTIL ALL BITS ARE TESTED

ANY ERRORS DETECTED ARE REPORTED AND THEN THE TEST RESUMES WITH THE NEXT BIT IN SEQUENCE .

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 4] IS CALLED TO REPORT BOTH FAIL TO CLEAR PROPERLY AND FAIL TO SET PROPERLY FAULTS.

SYNC:  
\*\*\*\*\*

- 1.) FAIL TO CLR: M7277 LOAD SSR LOW BYTE H CR1
- 2.) FAIL TO SET: M7277 LOAD SSR HIGH BYTE H CP2

DEBUG:  
\*\*\*\*\*

- 1.) PROBLEMS DETECTED BY THIS TEST INDICATE ADJACENT BIT INTERFERENCE CAUSED BY CROSS TALK OR NOISE. PROBLEM IS MOST LIKELY THE M7279.

KEY LOGIC: (SAME AS FOR TEST 6)  
\*\*\*\*\*

```
%  
MOV #3$, $LPERR ;SET UP THE ERROR LOOP RETURN  
MOV R1, R2 ;SET UP THE REG ADDR  
ADD #LPR, R2  
MOV #1, R5 ;INIT BIT TEST MASK  
1$: BIT R5, RGMSK3 ;TEST THIS BIT ??  
BNE 3$ ;BR IF YES  
2$: ASL R5 ;SHIFT THE BIT TEST MASK  
BEQ TST12 ;BR IF TESTED ALL BITS  
BR 1$ ;GO TEST THIS BIT  
3$: MOV RGMSK3, R4 ;SET UP S/B DATA  
CLR (R2) ;INIT REG BEING TESTED
```

# K12

MAINDEC-11-DZDHM-B  
DZDHMB.P11 T11

MACY11 27(732) 23-SEP-76 14:33 PAGE 35  
TEST THAT CLR/SET OF BIT "N" IN "LPR" DOES NOT CLEAR ANY OTHER BITS

SEQ 0153

1473	004172	112761	000000	000016		MOVB	#0,SSR(R1)	;SCOPE SYNC
1474	004200	040504				BIC	R5,R4	;CLR BIT "N"
1475	004202	016712	023350			MOV	RGMSK3,(R2)	;SET ALL R/W BITS IN LPR
1476	004206	040512				BIC	R5,(R2)	;CLEAR BIT "N" IN LPR
1477	004210	011203				MOV	(R2),R3	;GET THE WAS DATA
1478	004212	020304				CMP	R3,R4	;DID IT CLEAR OK ?
1479	004214	001404				SEQ	4\$	;BR IF YES
1480								
1481	004216	004767	020126			JSR	PC,SUER2	;GO SET UP ERROR INFO
1482	004222	104004				ERROR	4	;BIT "N" FAILED TO CLR PROPERLY
1483	004224	000754				BR	2\$	;GO TEST NEXT BIT
1484								
1485	004226	050504			4\$:	BIS	R5,R4	;SET BIT "N" IN S/B DATA
1486	004230	112761	000000	000017		MOVB	#0,SSR+1(R1)	;SCOPE SYNC
1487	004236	050512				BIS	R5,(R2)	;SET BIT "N" IN LPR
1488	004240	011203				MOV	(R2),R3	;GET THE WAS DATA
1489	004242	020304				CMP	R3,R4	;DID BIT "N" SET PROPERLY ?
1490	004244	001744				SEQ	2\$	;BR IF YES
1491								
1492	004246	004767	020076			JSR	PC,SUER2	;GO SET UP ERROR INFO
1493	004252	104004				ERROR	4	;BIT "N" FAILED TO SET PROPERLY
1494	004254	000740				BR	2\$	;GO SELECT NEXT BIT

1495  
1496  
1497  
1498 004256 000004  
1499  
1500  
1501  
1502  
1503  
1504  
1505  
1506  
1507  
1508  
1509  
1510  
1511  
1512  
1513  
1514  
1515  
1516  
1517  
1518  
1519  
1520  
1521  
1522  
1523  
1524  
1525  
1526  
1527  
1528  
1529  
1530  
1531  
1532  
1533  
1534  
1535  
1536  
1537  
1538  
1539 004260 012767 004314 174622  
1540 004266 010102  
1541 004270 062702 000014  
1542 004274 012705 000001  
1543 004300 030567 023254  
1544 004304 001003  
1545 004306 006305  
1546 004310 001436  
1547 004312 000772  
1548  
1549 004314 016704 023240  
1550 004320 040504

\*\*\*\*\*  
:TEST 12 TEST THAT CLR/SET OF BIT "N" IN "BKR" DOES NOT CLEAR ANY OTHER BITS  
\*\*\*\*\*

TST12: SCOPE  
.REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT CLEARING AND SETTING EACH R/W BIT IN THE BREAK CONTROL REGISTER INDIVIDUALLY DOES NOT DISTURB ANY OF THE OTHER BITS. A BIT MASK (RGMSK4: 177777) IS USED TO DEFINE THE R/W BITS (ALL 16.). R5 ALWAYS CONTAINS THE BIT CURRENTLY SELECTED FOR TEST. THE TEST SEQUENCE IS AS FOLLOWS:

- 1. SELECT A BIT TO TEST
- 2. SET ALL WRITABLE BITS IN THE "BKR"
- 3. CLEAR THE SELECTED BIT AND VERIFY THAT IT CLEARED PROPERLY
- 4. SET THE SELECTED BIT AND VERIFY THAT IT SET PROPERLY
- 5. REPEAT 1 THRU 4 UNTIL ALL BITS HAVE BEEN TESTED

ANY ERROR DETECTED IS REORTRD AND THEN THE TEST RESUMES WITH THE NEXT BIT IN SEQUENCE.

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 5] IS CALLED TO REPORT BOTH CLEAR AND SET FAULTS.

SYNC:  
\*\*\*\*\*

- 1.) FAIL TO CLR: M7277 SH4 LOAD SSR LOW BYTE H CR1
- 2.) FAIL TO SET: M7277 SH4 LOAD SSR HIGH BYTE H CP2

DEBUG:  
\*\*\*\*\*

- 1.) LIKE THE PREVIOUS TEST, FAILURES HERE INDICATE ADJACENT BIT INTERFERENCE CAUSED BY CROSS TALK OR NOISE. THE FAULT IS MOST LIKELY THE M7278 MODULE.

KEY LOGIC: (SAME AS FOR TEST 7)  
\*\*\*\*\*

%  
MOV #3\$, \$LPERR ;SET UP THE ERROR LOOP RETURN  
MOV R1, R2 ;SET UP THE REG ADDR  
ADD #BKR, R2  
MOV #1, R5 ;INIT BIT TEST MASK  
1\$: BIT R5, RGMSK4 ;TEST THIS BIT ?  
BNE 3\$ ;BR IF YES  
2\$: ASL R5 ;SHIFT THE BIT TEST MASK  
BEQ TST13 ;BR IF TESTED ALL BITS  
BR 1\$ ;GO TEST THIS BIT  
3\$: MOV RGMSK4, R4 ;SET UP S/B DATA  
BIC R5, R4 ;CLR BIT "N"

## M12

MAINDEC-11-DZDHM-8  
DZDHMB.P11 T12

MACY11 27(732) 23-SEP-76 14:33 PAGE 37  
TEST THAT CLR SET OF BIT "N" IN "BKR" DOES NOT CLEAR ANY OTHER BITS

SEQ 0155

1551	004322	005012			CLR	(R2)		; INIT REG BEING TESTED
1552	004324	016712	023230		MOV	RGMSK4,(R2)		; SET ALL R/W BITS IN PKR
1553	004330	112761	000000	000016	MOVB	#0,SSR(R1)		; SCOPE SYNC
1554	004336	040512			BIC	R5,(R2)		; CLEAR BIT "N" IN BKR
1555	004340	011203			MOV	(R2),R3		; GET THE WAS DATA
1556	004342	020304			CMP	R3,R4		; DID IT CLEAR OK ?
1557	004344	001404			BEQ	4\$		; BR IF YES
1558								
1559	004346	004767	017776		JSR	PC,SUER2		; GO SET UP ERROR INFO
1560	004352	104005			ERROR	5		; BIT "N" FAILED TO CLR PROPERLY
1561	004354	000754			BR	2\$		; GO TEST NEXT BIT
1562								
1563	004356	050504			BIS	R5,R4	4\$:	; SET BIT "N" IN S/B DATA
1564	004360	112761	000000	000017	MOVB	#0,SSR+1(R1)		; SCOPE SYNC
1565	004366	050512			BIS	R5,(R2)		; SET BIT "N" IN BKR
1566	004370	011203			MOV	(R2),R3		; GET THE WAS DATA
1567	004372	020304			CMP	R3,R4		; DID BIT "N" SET PROPERLY ?
1568	004374	001744			BEQ	2\$		; BR IF YES
1569								
1570	004376	004767	017746		JSR	PC,SUER2		; GO SET UP ERROR INFO
1571	004402	104005			ERROR	5		; BIT "N" FAILED TO SET PROPERLY
1572	004404	000740			BR	2\$		; GO SELECT NEXT BIT

1573  
1574  
1575  
1576 004406 000004  
1577  
1578  
1579  
1580  
1581  
1582  
1583  
1584  
1585  
1586  
1587  
1588  
1589  
1590  
1591  
1592  
1593  
1594  
1595  
1596  
1597  
1598  
1599  
1600  
1601  
1602  
1603  
1604  
1605  
1606  
1607  
1608  
1609  
1610  
1611  
1612  
1613  
1614  
1615  
1616  
1617 004410 012767 004444 174472  
1618 004416 010102  
1619 004420 062702 000016  
1620 004424 012705 000001  
1621 004430 030567 023126  
1622 004434 001003  
1623 004436 006305  
1624 004440 001442  
1625 004442 000772  
1626  
1627 004444 016704 023112  
1628 004450 040504

```
;;*****  
;*TEST 13 TEST THAT CLR/SET OF BIT "N" IN "SSR" DOES NOT CLEAR ANY OTHER BITS  
;;*****  
TST13: SCOPE  
.REM %  
TEST ABSTRACT:  
*****
```

THIS TEST VERIFIES THAT CLEARING AND SETTING EACH R/W BIT IN THE SILO STATUS REGISTER INDIVIDUALLY DOES NOT DISTURB ANY OF THE OTHER BITS. A BIT MASK (RGMSK5: 100077) IS USED TO DEFINE THE R/W BITS (15,5,4,3,2,1, AND 0). R5 ALWAYS CONTAINS THE BIT CURRENTLY SELECTED FOR TEST. THE TEST SEQUENCE IS AS FOLLOWS:

1. SELECT A BIT TO TEST
2. SET ALL WRITABLE BITS IN THE "SSR"
3. CLEAR THE SELECTED BIT AND VERIFY THAT IT CLEARED PROPERLY
4. SET THE SELECTED BIT AND VERIFY THAT IT SET PROPERLY
5. REPEAT 1 THRU 4 UNTIL ALL BITS HAVE BEEN TESTED

ANY ERROR DETECTED IS REORTRD AND THEN THE TEST RESUMES WITH THE NEXT BIT IN SEQUENCE.

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 6] IS CALLED TO REPORT BOTH CLEAR AND SET FAULTS.

SYNC:  
\*\*\*\*\*

- 1.) FAIL TO CLR: M7277 SH4 LOAD LPR H EP2
- 2.) FAIL TO SET: M7277 SH4 LOAD BCR H FUI

DEBUG:  
\*\*\*\*\*

- 1.) LIKE THE PREVIOUS TEST, FAILURES HERE INDICATE ADJACENT BIT INTERFERENCE CAUSED BY CROSS TALK OR NOISE. THE FAULT IS MOST LIKELY THE M7278 MODULE.

KEY LOGIC: (SAME AS FOR TEST 10)  
\*\*\*\*\*

```
%  
MOV #3$, $LPERR ;SET UP THE ERROR LOOP RETURN  
MOV R1, R2 ;SET UP THE PEG ADDR  
ADD #SSR, R2  
MOV #1, R5 ;INIT BIT TEST MASK  
1$: BIT R5, RGMSK5 ;TEST THIS BIT ??  
BNE 3$ ;BR IF YES  
2$: ASL R5 ;SHIFT THE BIT TEST MASK  
BEQ TST14 ;BR IF TESTED ALL BITS  
BR 1$ ;GO TEST THIS BIT  
3$: MOV RGMSK5, R4 ;SET UP S/B DATA  
BIC R5, R4 ;CLR BIT "N"
```

B13

MACY11-11-DZDM-B  
DZDM.P11 T13

MACY11 27(732) 23-SEP-76 14:33 PAGE 39  
TEST THAT CLR SET OF BIT "N" IN "SSR" DOES NOT CLEAR ANY OTHER BITS

323 0157

004453	005013		CLR	(R2)	: INIT REG BEING TESTED
004454	016713	023102	MOV	R0,MSYS (R2)	: SET ALL R/W BITS IN SSR
004460	012761	000000 000004	MOV	R0,LPR(R1)	: SCOPE SYNC
004466	040510		BIC	R5 (R2)	: CLEAR BIT "N" IN SSR
004470	011203		MOV	(R2),R3	: GET THE WAS DATA
004476	042703	077700	BIC	#7700,R3	: CLEAR JUNK BITS
004478	020304		COMP	R3,R4	: DID IT CLEAR OK ?
004500	001404		BEG	45	: BR IF YES
004502	004767	017642	JSR	PC,SJER2	: GO SET UP ERROR INFO
004506	004306		ERROR	6	: BIT "N" FAILED TO CLR PROPERLY
004510	000752		BR	25	: GO TEST NEXT BIT
004512	050504		BIS	R5,R4	: SET BIT "N" IN S/B DATA
004514	000206	000000 000014 45:	MOV	R0,BKR(R1)	: SCOPE SYNC
004516	000506		BIS	R5 (R2)	: SET BIT "N" IN SSR
004518	000106		MOV	(R2),R3	: GET THE WAS DATA
004520	000206	077700	BIC	#7700,R3	: CLEAR JUNK BITS
004522	000306		COMP	R3,R4	: DID BIT "N" SET PROPERLY ?
004524	001750		BEG	25	: BR IF YES
004526	004767	017606	JSR	PC,SUEF2	: GO SET UP ERROR INFO
004528	004306		ERROR	5	: BIT "N" FAILED TO SET PROPERLY
004530	000752		BR	25	: GO SELECT NEXT BIT

1697  
1698  
1699  
1700  
1701  
1702  
1703  
1704  
1705  
1706  
1707  
1708

004546 000004

\*\*\*\*\*  
\*TEST 14 "CAR" MEMORY ADDRESSING TEST  
\*\*\*\*\*  
\*ST14: SCOPE  
\*REM :  
\*TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT EACH LOCATION IN THE CURRENT ADDRESS MEMORY CAN BE UNIQUELY ADDRESSED. IT WRITES THE PATTERN SHOWN BELOW INTO THE MEMORY AND THEN READS BACK EACH LOCATION TO VERIFY THAT IT WAS WRITTEN CORRECTLY. SINCE THE MEMORY LOGIC IS PARTITIONED INTO FOUR 16 X 4 READ/WRITE MEMORY CHIPS, THE PATTERN RESULTS IN THE LINE NUMBER (00 - 17(8)) BEING WRITTEN AS DATA INTO TO EACH LOCATION (00 - 17(8)) IN EACH CHIP. THAT IS: LOC00 = 00, LOC 01 = 01, .....LOC 17 = 17.

MEMORY PATTERN:	LOCATION	CONTENTS	(BOTH OCTAL)
	00	000000	
	01	010421	
	02	021042	
	03	031463	
	04	042104	
	05	052525	
	06	063146	
	07	073567	
	10	104210	
			11 114631
	12	125252	
	13	135673	
	14	146314	
	15	156735	
	16	167356	
	17	177777	

ANY ERRORS DETECTED ARE REPORTED AND THEN THE TEST RESUMES CHECKING THE NEXT LOCATION IN SEQUENCE UNTIL ALL 16. HAVE BEEN CHECKED.

NOTE: THIS TEST ALWAYS CHECKS ALL 16. LINES REGARDLESS OF HOW THE LINE SELECTION PARAMETER WAS INITIALLY SET UP.

ERRORS:  
\*\*\*\*\*

1.) (ERROR 7) IS CALLED TO REPORT ANY LINES (LOCATIONS) THAT FAIL. THE FAILING LINE # IS INCLUDED AS PART OF THE ERROR HEADER MESSAGE.

SYNC:  
\*\*\*\*\*

- 1.) WRITE SYNC: M7277 SH4 LOAD SSR LOW BYTE H CR1
- 2.) READ SYNC: M7277 SH4 LOAD SSR HIGH BYTE H CR2

1709  
1710  
1711  
1712  
1713  
1714  
1715  
1716  
1717  
1718  
1719  
1720  
1721  
1722  
1723  
1724  
1725  
1726  
1727  
1728  
1729  
1730  
1731  
1732  
1733  
1734  
1735  
1736  
1737  
1738  
1739  
1740  
1741  
1742  
1743  
1744  
1745  
1746  
1747  
1748  
1749  
1750  
1751  
1752  
1753  
1754

DEBUG:  
\*\*\*\*\*

1.) ANALYZE THE ERROR REPORTS CAREFULLY ASKING THE FOLLOWING QUESTIONS:

- A. DOES THE FAULT AFFECT ONLY ONE LINE ?
- B. DOES THE FAULT AFFECT ONLY ONE 4-BIT DATA GROUP ?  
IE <15:12>, <11:08>, <07:04> OR <03:00>
- C. DOES ANY DATA AT ALL APPEAR TO BE WRITTEN ?

2.) IF "A" IS TRUE THEN SUSPECT AN ADDRESSING PROBLEM IN THE MEMORY ADDRESS MUX.

3.) IF "B" IS TRUE THEN SUSPECT A DATA MUX, UP-COUNTER, MEMORY, OR INTER CHIP PROBLEM.

4.) IF "C" IS TRUE SUSPECT A MEMORY WRITE TIMING PROBLEM.

5.) IN MOST CASES THE FAULT IS MOST LIKELY THE M7277 OR M7279.

KEY LOGIC:  
\*\*\*\*\*

```

M7277 SH4 LOAD CA H E58-13
          DATA TO BUS H EN2
          DATA SOURCE (A,B,C) DU1,DU2,DT2

SH5 MEMADD SOURCE SEL H E55-8
    CA MEM WRITE ENAB L E50-1
    BUF ADDRS TO BUS H E33-1 (SHD BE LOW)
    74157 MUX CHIPS E33,E27,E20 BITS<17:08>
    74193 COUNTER CHIPS E19,E26,E32 BITS<17:08>
    7489 MEMORY CHIPS E18,E25,E31 BITS<17:08>
    7404 INVERTER CHIPS E30,E24,E17 BITS<17:08>

SH5 74157 MUX CHIP E48
    74157 DATA MUX CHIPS E13,E05 BITS<07:00>
    74193 COUNTER CHIPS E12,E05 BITS<07:00>
    7489 MEMORY CHIPS E11,E04 BITS<07:00>

```

M7278 SH5 THRU SH8 74151 DATA MUX OUTPUT CHIPS (PIN 1 INPUT)

```

%
MOV R1,R2 ;COPY IT IN R2
ADD #CAR,R2 ;SET UP REGADR IN R2
MOV LINSSEL,$TMP7 ;SAVE LINE SELECT PARAMETER
MOV #-1,LINSSEL ;DO ALL LINES FOR THIS TEST
1$: JSR PC,$ELINE ;GO SELECT A LINE NO.
    BR 3$ ;BR IF DONE ALL SELECTED LINES
    TSTB LINE ;DOING LINE 00 ?
    BNE 2$ ;BR IF NOT
    CLR R4 ;INIT TEST DATA

2$: BISB LINE,(R1) ;SELECT A LINE
    MOVB #0,SSR(R1) ;SCOPE SYNC
    MOV R4,(R2) ;LOAD THE CAR REG.

```

```

004550 010102 000006
004552 062702 000006
004556 016767 022420 174434
004564 012767 177777 022410
004572 004767 017704
004576 000415
004600 105767 023406
004604 001001
004606 005004
004610 156711 023376
004614 112761 000000 000016
004622 C10412

```



1765	004624	062704	010421		ADD	#10421,R4	:GENERATE NEW DATA	
1766	004630	000760			BR	1\$	:GO DO NEXT LINE	
1768	004632	004767	017644	3\$:	JSR	PC,SELINE	:GO SELECT A LINE NO.	
1769	004636	000434			BR	7\$	:BR IF CHECKED ALL LINES	
1770	004640	105767	023346		TSTB	LINE	:DOING LINE 00 ?	
1771	004644	001001			SNE	4\$	:BR IF NOT	
1772	004646	005004			CLR	R4	:INIT S/B DATA	
1774	004650	156711	023336	4\$:	BISB	LINE,(R1)	:SELECT A LINE	
1775	004654	112761	000000	000017	MOVB	#0,SSR+1(R1)	:SCOPE SYNC	
1776	004652	011203			MOV	(R2),R3	:GET CONTENTS OF CAR	
1777	004654	020304			CMP	R3,R4	:WAS DATA OK ?	
1778	004666	001412			BEQ	5\$	:BR IF YES	
1779								
1780	004670	004767	017454		JSR	PC,SUER2	:GO SET UP ERROR INFO	
1781	004674	004567	017674		JSR	RS,SUNUM	:SET UP LINE NO. IN MSG BUFFER	
1782	004700	030212			LINE			
1783	004702	031045			EM7+47			
1784	004704	012767	004722	174176	MOV	#6\$,SLPERR	:SET UP ERROR LOOP RETURN	
1785	004712	104007			ERROR	7	:CAR ADDRESSING ERROR	
1786								
1787	004714	062704	010421	5\$:	ADD	#10421,R4	:GENERATE NEW S/B DATA	
1788	004720	000744			BR	3\$	:GO CHECK NEXT LINE	
1789								
1790	004722	005067	023264	6\$:	CLR	LINE	:RESTART AT LINE 00 IF LOOPING	
1791	004726	000721			BR	1\$	:GO RESTART	
1792								
1793	004730	016767	174264	022244	7\$:	MOV	\$TMP7,LINSEL	:RESTORE LINE SELECT PARAMETER

1794  
1795  
1796  
1797 004736 000004  
1798  
1799  
1800  
1801  
1802  
1803  
1804  
1805  
1806  
1807  
1808  
1809  
1810  
1811  
1812  
1813  
1814  
1815  
1816  
1817  
1818  
1819  
1820  
1821  
1822  
1823  
1824  
1825  
1826  
1827  
1828  
1829  
1830  
1831  
1832  
1833  
1834  
1835  
1836  
1837  
1838  
1839  
1840  
1841  
1842  
1843  
1844  
1845  
1846  
1847  
1848  
1849

::\*\*\*\*\*  
; \*TEST 15 "BCR" MEMORY ADDRESSING TEST  
::\*\*\*\*\*  
†ST15: SCOPE  
.REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT EACH LOCATION IN THE BYTE COUNT MEMORY CAN BE UNIQUELY ADDRESSED. IT WRITES THE PATTERN SHOWN BELOW INTO THE MEMORY AND THEN READS BACK EACH LOCATION TO VERIFY THAT IT WAS WRITTEN CORRECTLY. SINCE THE MEMORY LOGIC IS PARTITIONED INTO FOUR 16 X 4 READ/WRITE MEMORY CHIPS, THE PATTERN RESULTS IN THE LINE NUMBER (00 - 17(8)) BEING WRITTEN AS DATA INTO TO EACH LOCATION (00 - 17(8)) IN EACH CHIP. THAT IS: LOC00 = 00, LOC 01 = 01, .....LOC 17 = 17.

MEMORY PATTERN:	LOCATION	CONTENTS	(BCTH OCTAL)
	00	000000	
	01	010421	
	02	021042	
	03	031463	
	04	042104	
	05	052525	
	06	063146	
	07	073567	
	10	104210	
	11	114631	
	12	125252	
	13	135673	
	14	146314	
	15	156735	
	16	167356	
	17	177777	

ANY ERRORS DETECTED ARE REPORTED AND THEN THE TEST RESUMES CHECKING THEE NEXT LOCATION IN SEQUENCE UNTIL ALL 16. HAVE BEEN CHECKED.

NOTE: THIS TEST ALWAYS CHECKS ALL 16. LINES REGARDLESS OF HOW THE LINE SELECTION PARAMETER WAS INITIALLY SET UP.

ERRORS:  
\*\*\*\*\*

1.) [ERROR 10] IS CALLED TO REPORT ANY LINES (LOCATIONS) THAT FAIL. THE FAILING LINE # IS INCLUDED AS PART OF THE ERROR HEADER MESSAGE.

SYNC:  
\*\*\*\*\*

1.) WRITE SYNC: M7277 SH4 LOAD SSR LOW BYTE H CR1  
2.) READ SYNC: M7277 SH4 LOAD SSR HIGH BYTE H CP2

1850  
1851  
1852  
1853  
1854  
1855  
1856  
1857  
1858  
1859  
1860  
1861  
1862  
1863  
1864  
1865  
1866  
1867  
1868  
1869  
1870  
1871  
1872  
1873  
1874  
1875  
1876  
1877  
1878  
1879  
1880  
1881  
1882  
1883  
1884  
1885  
1886  
1887  
1888  
1889  
1890  
1891  
1892  
1893  
1894  
1895  
1896  
1897  
1898  
1899  
1900  
1901  
1902  
1903  
1904  
1905

DEBUG:  
\*\*\*\*\*

1.) ANALYZE THE ERROR REPORTS CAREFULLY ASKING THE FOLLOWING QUESTIONS:

- A. DOES THE FAULT AFFECT ONLY ONE LINE ?
- B. DOES THE FAULT AFFECT ONLY ONE 4-BIT DATA GROUP ?  
IE <15:12>, <11:08>, <07:04>, OR <03:00>
- C. DOES ANY DATA AT ALL APPEAR TO BE WRITTEN ?

2.) IF "A" IS TRUE THEN SUSPECT AN ADDRESSING PROBLEM IN THE MEMORY ADDRESS MUX.

3.) IF "B" IS TRUE THEN SUSPECT A DATA MUX, UP-COUNTER, MEMORY, OR INVERTER CHIP PROBLEM.

4.) IF "C" IS TRUE SUSPECT A MEMORY WRITE TIMING PROBLEM.

5.) IN MOST CASES THE FAULT IS MOST LIKELY THE M7277 OR M7279.

KEY LOGIC:  
\*\*\*\*\*

```

M7277 SH4 LOAD BC H          FU2
          DATA TO BUS H      EN2
          DATA SOURCE (A,B,C) DU1,DU2,DT2

SH5 MEMADD SOURCE SEL H      E55-8
BC MEM WRITE ENAB L         E57-4
BUF ADDRS TO BUS H          E33-1 (SHD BE LOW)

M7278 SH3 BITS<15:08>
74157 INPUT MUX CHIPS E18,E19
74193 UP COUNTER CHIPS E27,E28
7489 MEMORY CHIPS E33,E34
7404 INVERTER CHIPS E41,E42

SH4 BITS<07:00>
74157 INPUT MUX CHIPS E16,E17
74193 UP COUNTER CHIPS E24,E25
7489 MEMORY CHIPS E31,E32
7404 INVERTER CHIPS E39,E40

SH5 THRU SH8 74151 DATA MUX OUTPUT CHIPS (PIN 1 INPUT)

%
MOV R1,R2 ;COPY IT IN R2
ADD #BCR,R2 ;SET UP REGADR IN R2
MOV LINSSEL,$TMP7 ;SAVE LINE SELECT PARAMETER
MOV #-1,LINSSEL ;DO ALL LINES FOR THIS TEST
JSR PC,SELINE ;GO SELECT A LINE NO.
BR 3$ ;:BR IF DONE ALL SELECTED LINES
TSTB LINE ;DOING LINE 00 ?
BNE 2$ ;BR IF NOT
CLR R4 ;INIT TEST DATA

2$: BISB LINE,(R1) ;SELECT A LINE
MOV #0,$SR(R1) ;SCOPE SYNC

```

```

1894 004740 010102
1895 004742 062702 000010
1896 004746 016767 022230 174244
1897 004754 012767 177777 022220
1898 004762 004767 017514
1899 004766 000415
1900 004770 105767 023216
1901 004774 001001
1902 004776 005004
1903
1904 005000 156711 023206
1905 005004 112761 000000 000016

```

1906	005012	010412			MOV	R4,(R2)		:LOAD THE BCR REG.
1907	005014	062704	010421		ADD	#10421,R4		:GENERATE NEW DATA
1908	005020	000760			BR	1\$		:GO DO NEXT LINE
1909								
1910	005022	004767	017454	3\$:	JSR	PC,SELINE		:GO SELECT A LINE NO.
1911	005026	000434			BR	7\$		:BR IF CHECKED ALL LINES
1912	005030	105767	023156		TSTB	LINE		:DOING LINE 00 ?
1913	005034	001001			BNE	4\$		:BR IF NOT
1914	005036	005004			CLR	R4		:INIT S/B DATA
1915								
1916	005040	156711	023146	4\$:	BISB	LINE,(R1)		:SELECT A LINE
1917	005044	112761	000000	000017	MOVB	#0,SSR+1(R1)		:SCOPE SYNC
1918	005052	011203			MOV	(R2),R3		:GET CONTENTS OF BCR
1919	005054	020304			CMP	R3,R4		:WAS DATA OK ?
1920	005056	001412			BEQ	5\$		:BR IF YES
1921								
1922	005060	004767	017264		JSR	PC,SUER2		:GO SET UP ERROR INFO
1923	005064	004567	017504		JSR	R5,SUNUM		:GO SET UP LINE NO. IN MSG BUFFER
1924	005070	030212			LINE			
1925	005072	031114			EM10+44			
1926	005074	012767	005112	174006	MOV	#6\$, \$LPERR		:SET UP ERROR LOOP RETURN
1927	005102	104010			ERROR	10		:BCR ADDRESSING ERROR
1928								
1929	005104	062704	010421	5\$:	ADD	#10421,R4		:GENERATE NEW S/B DATA
1930	005110	000744			BR	3\$		:GO CHECK NEXT LINE
1931								
1932	005112	005067	023074	6\$:	CLR	LINE		:RESTART AT LINE 00 IF LOOPING
1933	005116	000721			BR	1\$		:GO RESTART
1934								
1935	005120	016767	174074	022054	7\$:	MOV	\$TMP7,LINSEL	:RESTORE THE LINE SELECT PARAMETER

1936  
1937  
1938  
1939 005126 000004  
1940  
1941  
1942  
1943  
1944  
1945  
1946  
1947  
1948  
1949  
1950  
1951  
1952  
1953  
1954  
1955  
1956  
1957  
1958  
1959  
1960  
1961  
1962  
1963  
1964  
1965  
1966  
1967  
1968  
1969  
1970  
1971  
1972  
1973  
1974  
1975  
1976  
1977  
1978 005130 010102  
1979 005132 062702 000006  
1980 005136 004767 017340  
1981 005142 000443  
1982 005144 C:2704 177777  
1983 005150 156711 023036  
1984 005154 004567 017414  
1985 005160 030212  
1986 005162 031045  
1987  
1988 005164 112761 000000 000016 2\$:  
1989 005172 010412  
1990 005174 011203  
1991 005176 020403

```
::*****  
: *TEST 16 "CAR" REGISTER TEST - ALL 1'S / ALL 0'S - ALL LINES  
:*****  
TST16: SCOPE  
.REM %  
TEST ABSTRACT:  
*****
```

THIS TEST VERIFIES THE ABILITY TO SET AND CLEAR ALL BITS IN ALL THE SELECTED LOCATIONS (LINES) OF THE CURRENT ADDRESS MEMORY. IT USES THE CONFIGURATION PARAMETER (LINSEL:) TO DEFINE WHICH LINES TO TEST. THE TEST SEQUENCE IS AS FOLLOWS:

1. SELECT A LINE # TO TEST
2. LOAD THE SELECTED LOCATION WITH 177777
3. READ IT BACK TO VERIFY ALL BITS SET
4. LOAD THE SELECTED LOCATION WITH 000000
5. READ IT BACK TO VERIFY ALL BITS CLEARED
6. REPEAT STEPS 1 THRU 5 UNTIL ALL SELECTED LINES ARE TESTED.

ALL ERRORS ARE REPORTED AND THEN THE TEST RESUMES WITH THE NEXT LINE # IN SEQUENCE AS DEFINED BY "LINSEL".

ERRORS:  
\*\*\*\*\*

1.) [ERROR 7] IS CALLED TO REPORT ALL DATA COMPARE ERRORS

SYNC:  
\*\*\*\*\*

- 1.) WRITE 1'S: M7277 SH4 LOAD SSR LOW BYTE H CR1
- 2.) WRITE 0'S: M7277 SH4 LOAD SSR HIGH BYTE H CP2

DEBUG: (REFER TO TEST 14)  
\*\*\*\*\*

KEY LOGIC: (REFER TO TEST 14)  
\*\*\*\*\*

```
%  
MOV R1,R2 ;COPY IT INTO R2  
ADD #CAR,R2 ;R2 GETS CAR ADDRESS  
1$: JSR PC,SELINE ;GO SELECT A LINE NO.  
BR TST17 ;BR IF DONE ALL SELECTED LINES  
MOV #-1,R4 ;RESULT IN CAR S/B = 177777  
BISB LINE,(R1) ;SELECT A LINE NO.  
JSR R5,SUNUM ;GO SET UP LINE NO. IN MSG BUFFER  
LINE  
EM7+47  
%  
MOV #0,SSR(R1) ;SCOPE SYNC  
MOV R4,(R2) ;LOAD A CAR WITH ALL ONES  
MOV (R2),R3 ;GET THE WAS DATA FROM THE CAR  
CMP R4,R3 ;DID IT CONTAIN ALL ONES ??
```

MAINDEC-11-DZDMM-8  
DZDMMB.P11 T16

MACY11 27(732) 23-SEP-76 14:33 PAGE 47  
"CAR" REGISTER TEST - ALL 1'S / ALL 0'S - ALL LINES

SEQ 0165

1992	005200	001406			BEQ	3\$		::BR IF ALL 1'S
1993								
1994	005202	004767	017142		JSR	PC,SUER2		;GO SET UP ERROR INFO
1995	005206	012767	005164	173674	MOV	#2\$, \$LPERR		;SET UP ERROR LOOP RETURN
1996	005214	104007			ERROR	7		;FAILED TO SET ALL 1'S IN SELECTED CAR
1997								
1998	005216	005004			CLR	R4		;RESULT IN CAR S/B = 000000
1999	005220	112761	000000	000017	MOVB	#0,SSR+1(R1)		;SCOPE SYNC
2000	005226	010412			MOV	R4,(R2)		;CLEAR SELECTED CAR
2001	005230	011203			MOV	(R2),R3		;GET THE WAS DATA
2002	005232	001741			BEQ	1\$		;BR IF CAR GOT CLEARED
2003								
2004	005234	004767	017110		JSR	PC,SUER2		;GO SET UP FOR ERROR CALL
2005	005240	012767	005216	173642	MOV	#3\$, \$LPERR		;SET UP ERROR LOOP RETURN
2006	005246	104007			ERROR	7		;FAILED TO CLR ALL BITS IN SELECTED CAR
2007	005250	000732			BR	1\$		;GO TEST NEXT LINE

# K13

MAINDEC-11-DZDHM-B  
DZDHMB.P11 T17

MACY11 27(732) 23-SEP-76 14:33 PAGE 48  
"BCR" REGISTER TEST - ALL 1'S / ALL 0'S - ALL LINES

SEQ 0166

2008  
2009  
2010  
2011 005252 000004  
2012  
2013  
2014  
2015  
2016  
2017  
2018  
2019  
2020  
2021  
2022  
2023  
2024  
2025  
2026  
2027  
2028  
2029  
2030  
2031  
2032  
2033  
2034  
2035  
2036  
2037  
2038  
2039  
2040  
2041  
2042  
2043  
2044  
2045  
2046  
2047  
2048  
2049  
2050 005254 010102  
2051 005256 062702 000010  
2052 005262 004767 017214  
2053 005266 000443  
2054 005270 012704 177777  
2055 005274 156711 022712  
2056 005300 004567 017270  
2057 005304 030212  
2058 005306 031114  
2059  
2060 005310 112761 000000 000016 25:  
2061 005316 010412  
2062 005320 011203  
2063 005322 020403

```

:*****
;*TEST 17 "BCR" REGISTER TEST - ALL 1'S / ALL 0'S - ALL LINES
:*****

```

```

TST17: SCOPE
.REM %
TEST ABSTRACT:
*****

```

THIS TEST VERIFIES THE ABILITY TO SET AND CLEAR ALL BITS IN ALL THE SELECTED LOCATIONS (LINES) OF THE BYTE COUNT MEMORY. IT USES THE CONFIGURATION PARAMETER (LINSEL:) TO DEFINE WHICH LINES TO TEST. THE TEST SEQUENCE IS AS FOLLOWS:

1. SELECT A LINE # TO TEST
2. LOAD THE SELECTED LOCATION WITH 177777
3. READ IT BACK TO VERIFY ALL BITS SET
4. LOAD THE SELECTED LOCATION WITH 000000
5. READ IT BACK TO VERIFY ALL BITS CLEARED
6. REPEAT STEPS 1 THRU 5 UNTIL ALL SELECTED LINES ARE TESTED.

ALL ERRORS ARE REPORTED AND THEN THE TEST RESUMES WITH THE NEXT LINE # IN SEQUENCE AS DEFINED BY "LINSEL".

ERRORS:  
\*\*\*\*\*

1.) [ERROR 10] IS CALLED TO REPORT ALL DATA COMPARE ERRORS

SYNC:  
\*\*\*\*\*

1.) WRITE 1'S: M7277 SH4 LOAD SSR LOW BYTE H CR1

2.) WRITE 0'S: M7277 SH4 LOAD SSR HIGH BYTE H CP2

DEBUG: (REFER TO TEST 15)  
\*\*\*\*\*

KEY LOGIC: (REFER TO TEST 15)  
\*\*\*\*\*

```

%
MOV R1,R2 ;COPY IT INTO R2
ADD #BCR,R2 ;R2 GETS BCR ADDRESS
1$: JSR PC,SELIN ;GO SELECT A LINE NO.
BR TST20 ;:BR IF DONE ALL SELECTED LINES
MOV #-1,R4 ;:RESULT IN BCR S/B = 177777
BISB LINE,(R1) ;:SELECT A LINE NO.
JSR R5,SUNUM ;:GO SET UP LINE NO. IN MSG BUFFER
LINE
EM10+44

2$: MOVB #0,SSR(R1) ;SCOPE SYNC
MOV R4,(R2) ;LOAD A BCR WITH ALL ONES
MOV (R2),R3 ;GET THE WAS DATA FROM THE BCR
CMP R4,R3 ;DID IT CONTAIN ALL ONES ??

```

# L13

MAINDEC-11-DZDMM-B  
DZDMMB.P11 T17

MACY11 27(732) 23-SEP-76 14:33 PAGE 49  
"BCR" REGISTER TEST - ALL 1'S / ALL 0'S - ALL LINES

SEQ 0167

2064	005324	001406		BEQ	3\$		::BR IF ALL 1'S
2065							
2066	005326	004767	017016	JSR	PC,SUER2		:GO SET UP ERROR INFO
2067	005332	012767	005310 173550	MOV	#2\$, \$LPERR		:SET UP ERROR LOOP RETURN
2068	005340	104010		ERROR	10		:FAILED TO SET ALL 1'S IN SELECTED BCR
2069							
2070	005342	005004		CLR	R4		:RESULT IN BCR S/B = 000000
2071	005344	112761	000000 000017	MOV	#0, SSR+1(R1)		:SCOPE SYNC
2072	005352	010412		MOV	R4, (R2)		:CLEAR SELECTED BCR
2073	005354	011203		MOV	(R2), R3		:GET THE WAS DATA
2074	005356	001741		BEQ	1\$		:BR IF BCR GOT CLEARED
2075							
2076	005360	004767	016764	JSR	PC,SUER2		:GO SET UP FOR ERROR CALL
2077	005364	012767	005342 173516	MOV	#3\$, \$LPERR		:SET UP ERROR LOOP RETURN
2078	005372	104010		ERROR	10		:FAILED TO CLR ALL BITS IN SELECTED BCR
2079	005374	000732		BR	1\$		:GO TEST NEXT LINE



2080  
2081  
2082  
2083 005376 000004  
2084  
2085  
2086  
2087  
2088  
2089  
2090  
2091  
2092  
2093  
2094  
2095  
2096  
2097  
2098  
2099  
2100  
2101  
2102  
2103  
2104  
2105  
2106  
2107  
2108  
2109  
2110  
2111  
2112  
2113  
2114  
2115  
2116  
2117  
2118  
2119  
2120  
2121  
2122  
2123  
2124  
2125  
2126  
2127  
2128  
2129  
2130  
2131  
2132  
2133  
2134  
2135

```
::*****  
;*TEST 20 "CAR" MEMORY PATTERNS TEST / O'S DISTURB  
:*****  
TST20: SCOPE  
.REM %  
TEST ABSTRACT:  
*****
```

THIS TEST VERIFIES THAT WHEN A TEST PATTERN IS WRITTEN INTO LOCATION "N" OF THE "CAR" MEMORY, IT DOES NOT DISTURB ANY BITS IN ANY OTHER LOCATIONS. THERE ARE THREE TEST PATTERNS USED\* (177777, 125252, 052525) FOR EACH LOCATION SELECTED BY THE CONFIGURATION PARAMETER "LINSEL". THE TEST SEQUENCE IS AS FOLLOWS:

1. SELECT A TEST PATTERN
2. SELECT A LINE # TO TEST
3. CLEAR ALL 16. LOCATIONS IN THE MEMORY
4. WRITE THE TEST PATTERN INTO THE SELECTED LOCATION
5. VERIFY THAT THE PATTERN WAS WRITTEN CORRECTLY AND THAT NO OTHER LOCATIONS WERE DISTURBED.
6. REPEAT 2 THRU 5 UNTIL ALL SELECTED LINES TESTED
7. REPEAT 1 THRU 6 UNTIL ALL THREE PATTERNS TESTED

ALL ERRORS ARE REPORTED AND THEN THE TEST RESUMES WITH CHECKING THE NEXT LINE IN SEQUENCE.

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 46] IS CALLED TO REPORT ANY ERROR DETECTED. THE INFORMATION PRINTED INCLUDES THE LINE # WRITTEN, THE LINE # BEING CHECKED, AND THE PATTERN USED.

SYNC\*  
\*\*\*\*\*

- 1.) WRITE LINE: M7277 SH4 LOAD SSR LOW BYTE H CR1
- 2.) READ CHECK: M7277 SH4 LOAD SSR HIGH BYTE H CP2

DEBUG: (REFER TO TEST 14)  
\*\*\*\*\*

KEY LOGIC: (REFER TO TEST 14)  
\*\*\*\*\*  
%

```
MOV R1,R2 ;SET UP REGADR  
ADD #CAR,R2  
MOV #PATR1,R5 ;SET UP POINTER TO DATA PATTERNS  
1$: MOV (R5)+,$TMP1 ;GET A DATA TEST PATTERN  
BEQ TST21 ;BR IF DONE THREE PATTERNS  
11$: JSR PC,SELINEL ;GO SELECT A LINE TO TEST  
BR 1$ ;BR IF DONE ALL SELECTED LINES  
MOV LINE,LINEL ;SAVE THE LINE NO. FOR ERROR LOOPING  
2$: CLRB $TMP3 ;INIT LINE COUNTER
```

005400 010102  
005402 062702 000006  
005406 012705 027220  
005412 012567 173566  
005416 001472  
005420 004767 017056  
005424 000772  
005426 116767 022560 022560  
005434 105067 173550

2136	005440	116711	173544	3\$:	MOVB	\$TMP3, (R1)	; SELECT A LINE TO CLEAR
2137	005444	005012			CLR	(R2)	; CLR CAR FOR THAT LINE
2138	005446	105267	173536		INCB	\$TMP3	; GENERATE NEW LINE NO.
2139	005452	126727	173532	000020	CMPB	\$TMP3, #20	; DONE CLEARING ALL LINES ?
2140	005460	001367			BNE	3\$	; BR IF NOT
2141							
2142	005462	116711	022526		MOVB	LINEA, (R1)	; SET LINE SELECT BITS
2143	005466	112761	000000	000016	MOVB	#0, SSR(R1)	; SCOPE SYNC
2144	005474	016712	173504		MOV	\$TMP1, (R2)	; LOAD CAR WITH TEST PATTERN
2145							
2146	005500	105067	173502		CLRB	\$TMP2	; INIT A LINE COUNTER
2147	005504	016704	173474	4\$:	MOV	\$TMP1, R4	; SET UP S/B DATA
2148	005510	116711	173472		MOVB	\$TMP2, (R1)	; SET LINE SELECT IN SCR
2149	005514	112761	000000	000017	MOVB	#0, SSR+1(R1)	; SCOPE SYNC
2150	005522	011203			MOV	(R2), R3	; GET WAS DATA
2151	005524	126767	173456	022460	CMPB	\$TMP2, LINE	; IS THIS THE LINE WITH THE TEST PATTERN
2152	005532	001401			BEQ	5\$	; BR IF IT IS
2153	005534	005004			CLR	R4	; MAKE S/B DATA = 000000
2154	005536	020304		5\$:	CMP	R3, R4	; CORRECT DATA IN CAR ?
2155	005540	001412			BEQ	6\$	; BR IF YES
2156							
2157	005542	004767	016670		JSR	PC, SJER4	; GO SET UP ERROR IN FO
2158	005546	004567	017022		JSR	FS, SUNUM	; GO SET UP LINE NO. IN MSG BUFFER
2159	005552	001206			\$TMP2		
2160	005554	033566			EM46+63		
2161	005556	012767	005434	173324	MOV	#2\$, \$LPERR	; SET UP ERROR LOOP RETURN
2162	005564	104046			EKROP	4\$	; INCORRECT DATA READ FROM CAR
2163							
2164	005566	105267	173414	6\$:	INCB	\$TMP2	; GENERATE NEXT LINE NO.
2165	005572	122767	000020	173406	CMPB	#20, \$TMP2	; DONE ALL LINES ?
2166	005600	001707			BEQ	11\$	; BR IF YES
2167	005602	000740			BR	4\$	; GO CHECK NEXT LINE

005606  
005610  
005614  
005620  
005624  
005626  
005632  
005634  
005642

005604 000004

\*\*\*\*\*  
:TEST 21 "BCR" MEMORY PATTERNS TEST / O'S DISTURB  
\*\*\*\*\*

TST21: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT WHEN A TEST PATTERN IS WRITTEN INTO LOCATION "N" OF THE "BCR" MEMORY, IT DOES NOT DISTURB ANY BITS IN ANY OTHER LOCATIONS. THERE ARE THREE TEST PATTERNS USED\* (17777, 125252, 052525) FOR EACH LOCATION SELECTED BY THE CONFIGURATION PARAMETER "LINSEL". THE TEST SEQUENCE IS AS FOLLOWS:

1. SELECT A TEST PATTERN
2. SELECT A LINE # TO TEST
3. CLEAR ALL 16 LOCATIONS IN THE MEMORY
4. WRITE THE TEST PATTERN INTO THE SELECTED LOCATION
5. VERIFY THAT THE PATTERN WAS WRITTEN CORRECTLY AND THAT NO OTHER LOCATIONS WERE DISTURBED.
6. REPEAT 2 THRU 5 UNTIL ALL SELECTED LINES TESTED
7. REPEAT 1 THRU 6 UNTIL ALL THREE PATTERNS TESTED

ALL ERRORS ARE REPORTED AND THEN THE TEST RESUMES WITH CHECKING THE NEXT LINE IN SEQUENCE.

ERRORS:  
\*\*\*\*\*

1.) !ERROR 471 IS CALLED TO REPORT ANY ERROR DETECTED. THE INFORMATION PRINTED INCLUDES THE LINE # WRITTEN, THE LINE # BEING CHECKED, AND THE PATTERN USED.

SYNC\*  
\*\*\*\*\*

- 1.) WRITE LINE: M7277 SH4 LOAD SSR LOW BYTE H CR1
- 2.) READ CHECK: M7277 SH4 LOAD SSR HIGH BYTE H CP2

DEBUG: (REFER TO TEST 15)  
\*\*\*\*\*

KEY LOGIC: (REFER TO TEST 15)  
\*\*\*\*\*

```

%
005606 010102          MOV    R1,R2          ;SET UP REGADR
005610 062702 000010  ADD    #BCR,R2
005614 012705 027220  MOV    #PATRMA,R5    ;SET UP POINTER TO DATA PATTERNS
005620 012567 173360 15:  MOV    (R5)+,$TMP1   ;GET A DATA TEST PATTERN
005624 001472          BEQ    TST22          ;BR IF DONE THREE PATTERNS
005626 004767 016650 115: JSR    PC,SELIN    ;GO SELECT A LINE TO TEST
005632 000772          BR     15            ;BR IF SELECTED ALL LINES
005634 116767 022352 022352  MOVB  LINE,LINER     ;SAVE THE LINE NO. FOR ERROR LOOP

005642 105067 173342 25:  CLRB  $TMP3         ;INIT LINE COUNTER

```

005646	116711	173336		35:	MOVB	STMP3, (R1)	: SELECT A LINE TO CLEAR
005652	005012				CLR	(R2)	: CLR BCR FOR THAT LINE
005654	105267	173330			INCB	STMP3	: GENERATE NEW LINE NO.
005660	126727	173324	000020		CMPB	STMP3, #20	: DONE CLEARING ALL LINES ?
005666	001357				BNE	35	: BR IF NOT
005670	116711	022320			MOVB	LINEA, (R1)	: SET LINE SELECT BITS
005674	112761	000000	000016		MOVB	#0, SSR(R1)	: SCOPE SYNC
005702	016712	173276			MOV	STMP1, (R2)	: LOAD BCR WITH TEST PATTERN
005706	105067	173274			CLRB	STMP2	: INIT A LINE COUNTER
005712	016704	173266		45:	MOV	STMP1, R4	: SET UP S/B DATA
005716	116711	173264			MOVB	STMP2, (R1)	: SELECT A LINE TO CHECK
005722	112761	000000	000017		MOVB	#0, SSR+1(R1)	: SCOPE SYNC
005730	011203				MOV	(R2), R3	: GET WAS DATA
005732	126767	173250	022252		CMPB	STMP2, LINE	: IS THIS THE LINE WITH THE TEST PATTERN
005740	001401				BEQ	55	: BR IF IT IS
005742	005004				CLR	R4	: MAKE S/B DATA = 000000
005744	020304			55:	CMP	R3, R4	: CORRECT DATA IN BCR ?
005746	001412				BEQ	65	: BR IF YES
005750	004767	016462			JSR	PC, SUER4	: GO SET UP ERROR IN FO
005754	004567	016614			JSR	R5, SUNUM	: GO SET UP LINE NO. IN MSG BUFFER
005760	001206				STMP2		
005762	034066				EM47+56		
005764	012767	005642	173116		MOV	#25, \$LPERP	: SET UP ERROR LOOP RETURN
005772	104047				ERROR	47	: INCORRECT DATA READ FROM BCR
005774	105267	173206		65:	INCB	STMP2	: GENERATE NEXT LINE NO.
006000	122767	000020	173200		CMPB	#20, STMP2	: DONE ALL LINES ?
006006	001707				BEQ	115	: BR IF YES
006010	000740				BR	45	: GO CHECK NEXT LINE

15



2313	006072	001367			BNE	3\$		:BR IF NOT
2314	006074	116711	022114		MOVW	LINEA, (R1)		:SET LINE SELECT IN SCR
2315	006100	112761	000000	000016	MOVW	#0, SSR(R1)		:SCOPE SYNC
2316	006106	005012			CLR	(R2)		:CLEAR THE CAR UNDER TEST
2317	006110	105067	173072		CLRB	\$TMP2		:INIT A LINE COUNTER
2318	006114	005004			CLR	R4	4\$:	:MAKE S/B DATA = 000000
2319	006116	116711	173064		MOVW	\$TMP2, (R1)		:SELECT A LINE TO CHECK
2320	006122	112761	000000	000017	MOVW	#0, SSR+1(R1)		:SCOPE SYNC
2321	006130	011203			MOV	(R2), F3		:GET WAS DATA
2322	006132	126767	173050	022052	CMPB	\$TMP2, LINE		:IS THIS THE LINE WITH THE TEST PATTERN
2323	006140	001401			SEQ	5\$		:BR IF IT IS
2324	006142	010504			MOV	R5, R4	5\$:	:MAKE S/B DATA = 177777
2325	006144	020304			CMP	R3, R4		:CORRECT DATA IN CAR ?
2326	006146	001412			BEQ	6\$		:BR IF YES
2327	006150	004767	016262		JSR	PC, SJER4		:GO SET UP ERROR IN FO
2328	006154	004567	016414		JSR	R5, SUNUM		:GO SET UP LINE NO. IN MSG BUFFER
2329	006160	001206			\$TMP2			
2330	006162	033666			EM46+63			
2331	006164	012767	006046	172716	MOV	#2\$, \$LPERR		:SET UP ERROR LOOP RETURN
2332	006172	104046			ERROR	46		:INCORRECT DATA READ FROM CAR
2333	006174	105267	173006		INCB	\$TMP2	6\$:	:GENERATE NEXT LINE NO.
2334	006200	122767	000020	173000	CMPB	#20, \$TMP2		:DONE ALL LINES ?
2335	006206	001711			BEQ	1\$		:BR IF YES
2336	006210	020741			BR	4\$		:GO CHECK NEXT LINE

2340  
2341  
2342  
2343  
2344  
2345  
2346  
2347  
2348  
2349  
2350  
2351  
2352  
2353  
2354  
2355  
2356  
2357  
2358  
2359  
2360  
2361  
2362  
2363  
2364  
2365  
2366  
2367  
2368  
2369  
2370  
2371  
2372  
2373  
2374  
2375  
2376  
2377  
2378  
2379  
2380  
2381  
2382  
2383  
2384  
2385  
2386  
2387  
2388  
2389  
2390  
2391  
2392  
2393  
2394  
2395

006212 000004

```
::*****  
:*TEST 23 "BCR" MEMORY PATTERNS TEST / 1'S DISTURB  
:*****  
TST23: SCOPE  
.REM %  
TEST ABSTRACT:  
*****
```

THIS TEST VERIFIES THAT WHEN ALL ZEROS ARE WRITTEN INTO LINE "N"  
IN THE "BCR" MEMORY, IT DOES NOT CLEAR ANY BITS IN ANY OTHER LOCATIONS.  
ONLY THE LINES SELECTED BY "LINSEL" ARE TESTED. THE TEST SEQUENCE IS  
AS FOLLOWS:

1. SELECT A LINE TO TEST
2. SET ALL ONES (177777) INTO ALL MEMORY LOCATIONS
3. CLEAR THE SELECTED LINE
4. VERIFY THAT ONLY THE SELECTED LINE WAS CLEARED  
AND ALL OTHER LINES STILL CONTAIN 177777
5. REPEAT STEPS 1 THRU 4 UNTIL ALL SELECTED LINES ARE TESTED

ALL ERRORS ARE REPORTED AND THEN THE TEST RESUMES CHECKING THE NEXT  
LINE IN SEQUENCE.

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 47] IS CALLED TO REPORT ALL ERRORS. THE INFORMATION PRINTED  
INCLUDES THE LINE # WRITTEN, THE LINE # BEING CHECKED, AND THE  
PATTERN USED.

SYNC:  
\*\*\*\*\*

- 1.) WRITE LINE: M7277 SH4 LOAD SSR LOW BYTE H CR1
- 2.) CHECK LINE: M7277 SH4 LOAD SSR HIGH BYTE H CP2

DEBUG: (REFER TO TEST 15)  
\*\*\*\*\*

KEY LOGIC: (REFER TO TEST 15)  
\*\*\*\*\*

006214 010102  
006216 062702 000010  
006222 012705 177777  
006226 010567 172752  
006232 004767 016244  
006236 000465  
006240 116767 021746 021746  
006246 105067 172736  
006252 116711 172732  
006256 010512  
006260 105267 172724  
006264 126727 172720 000020

```
%  
MOV R1,R2 ;SET UP REGADR  
ADD #BCR,R2  
MOV #-1,R5 ;TEST PATERN IN R5 = 177777  
MOV R5,$TMP1 ;SAVE IT FOR ERROR REPORTING  
1$: JSR PC,SELIN ;GO SELECT A LINE TO TEST  
BR TST24 ;BR IF DONE ALL LINES  
MOV# LINE,LINEA ;SAVE THE LINE NO.  
2$: CLRB $TMP3 ;INIT LINE COUNTER  
3$: MOV# $TMP3,(R1) ;SELECT A LINE TO INIT  
MOV R5,(R2) ;LOAD BCR WITH 177777  
INCB $TMP3 ;GENERATE NEW LINE NO.  
CMPB $TMP3,#20 ;DONE SETTING ALL LINES TO 177777 ?
```

MAINDEC-11-DZDHM-8  
DZDHMB.P11 T23

MACY11 27(722) 23-SEP-76 14:33 PAGE 57  
"BCR" MEMORY PATTERNS TEST / 1'S DISTURB

SEQ 0175

```

2396 006272 001367          BNE      3$          ;BR IF NOT
2397
2398 006274 116711 021714    MOVB     LINEA,(R1)   ;SET LINE SELECT BITS
2399 006300 112761 000000 000016  MOVB     #0,SSR(R1)  ;SCOPE SYNC
2400 006306 005012          CLR      (R2)        ;CLEAR THE BCR UNDER TEST
2401
2402 006310 105067 172672          CLRB     $TMP2       ;INIT A LINE COUNTER
2403 006314 005004          CLR      R4         ;MAKE S/B DATA = 000000
2404 006316 116711 172664          MOVB     $TMP2,(R1)  ;SELECT A LINE TO CHECK
2405 006322 112761 000000 000017  MOVB     #0,SSR+1(R1);SCOPE SYNC
2406 006330 011203          MOV      (R2),R3    ;GET WAS DATA
2407 006332 126767 172650 021652  CMPB     $TMP2,LINE  ;IS THIS THE LINE WITH THE TEST PATTERN
2408 006340 001401          BEQ      5$         ;BR IF IT IS
2409 006342 010504          MOV      R5,R4      ;MAKE S/B DATA = 177777
2410 006344 020304          CMP      R3,R4      ;CORRECT DATA IN BCR ?
2411 006346 001412          BEQ      6$         ;BR IF YES
2412
2413 006350 004767 016062          JSR      PC,SUER4    ;GO SET UP ERROR IN FO
2414 006354 004567 016214          JSR      R5,SUNUM    ;GO SET UP LINE NO. IN MSG BUFFER
2415 006360 001206          $TMP2
2416 006362 034066          EM47+56
2417 006364 012767 006246 172516  MOV      #2$,SLPERR  ;SET UP ERROR LOOP RETURN
2418 006372 104047          ERROR     47        ;INCORRECT DATA READ FROM BCR
2419
2420 006374 105267 172606          INCB     $TMP2       ;GENERATE NEXT LINE NO.
2421 006400 122767 000020 172600  CMPB     #20,$TMP2   ;DONE ALL LINES ?
2422 006406 001711          BEQ      1$         ;BR IF YES
2423 006410 000741          BR       4$         ;GO CHECK NEXT LINE

```



474  
475  
476  
477  
478  
479  
480  
481  
482  
483  
484  
485  
486  
487  
488  
489  
490  
491  
492  
493  
494  
495  
496  
497  
498  
499  
500  
501  
502  
503  
504  
505  
506  
507  
508  
509  
510  
511  
512  
513  
514  
515  
516  
517  
518  
519  
520  
521  
522  
523  
524  
525  
526  
527  
528  
529  
530  
531  
532  
533  
534  
535  
536  
537  
538  
539  
540  
541  
542  
543  
544  
545  
546  
547  
548  
549  
550  
551  
552  
553  
554  
555  
556  
557  
558  
559  
560  
561  
562  
563  
564  
565  
566  
567  
568  
569  
570  
571  
572  
573  
574  
575  
576  
577  
578  
579

006412 000004

```
::*****  
: *TEST 24 TEST THAT "CAR" MEMORY EXT BITS SET/CLR PROPERLY  
:*****  
†ST24: SCOPE  
-REM %  
TEST ABSTRACT:  
*****
```

THIS TEST VERIFIES THAT THE "EXT MEM" BITS (CAR<17:16> CAN BE SET AND CLEARED IN ALL "CAR" MEMORY LOCATIONS. IT WRITES THE BINARY TEST PATTERNS (11, 01, AND 10) INTO BITS<17:16> TO CHECK EVERY MEMORY LOCATION. THE TEST SEQUENCE IS AS FOLLOWS:

1. SELECT A TEST PATTERN TO USE
2. CLEAR ALL 18 BITS IN ALL 16 LOCATIONS
3. SELECT A LINE TO TEST
4. WRITE THE TEST PATTERN INTO <17:16> OF THE SELECTED LOCATION
5. READ CHECK ALL LOCATIONS TO VERIFY THAT ONLY THE SELECTED LOCATION CONTAINS THE PATTERN
6. REPEAT STEPS 3 THRU 5 UNTIL ALL SELECTED LINES TESTED
7. REPEAT STEPS 1 THRU 6 UNTIL ALL PATTERNS USED

ALL ERRORS ARE REPORTED AND THEN THE TEST RESUMES CHECKING THE NEXT LINE IN SEQUENCE.

- NOTES: 1.) BITS<05:04> IN THE "SCR" ARE USED TO WRITE THE EXT MEM BITS  
2.) BITS<07:06> IN THE "SSR" ARE USED TO CHECK BITS<17:16>

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 7] IS CALLED TO REPORT ALL ERRORS

SYNC:  
\*\*\*\*\*

- 1.) WRITE CAR: M7277 SH4 LOAD LPR H EP2
- 2.) READ CAR: M7277 SH4 LOAD BCR H FU2

DEBUG:  
\*\*\*\*\*

- 1.) ASSUMING THAT THE PREVIOUS "CAR" MEMORY TESTS RAN ERROR FREE. THE PROBLEM IS EITHER THE M7277 OR THE M7278
- 2.) SET UP SCOPE ERROR LOOP AND START BACKTRACKING THROUGH THE LOGIC STARTING WITH THE KEY SIGNALS BELOW.

KEY LOGIC:  
\*\*\*\*\*

M7277	SH5	SCR05 H	CD2
		SCR04 H	CE1
		SSR07 H	CF1



SSR06 H CH1

M7278 SH7 74151 MUX CHIPS E66 AND E59 (INPUT PIN 12)

NOTE: THER MAY BE A PRINT ERROR ON SH7 OF THE M7278. THE SIGNALS INTO THE MUX CHIPS E66 AND E59 CCOME FROM THE M7277 SH5 RATHER FROM M7279 SH3.

```

2480
2481
2482
2483
2484
2485
2486
2487
2488
2489
2490 006414 010102          MOV R1,R2          ;SET UP REGADR
2491 006416 062702 000016  ADD #SSR,R2
2492 006422 012705 027230  MOV #PATRNB,R5    ;SET UP POINTER TO DATA PATTERNS
2493 006426 012567 172552 1$: MOV (R5)+,$+MP1  ;GET THE PATTERNS
2494 006432 012567 172550  MOV (R5)+,$+MP2
2495 006436 001505          BEQ TST25         ;;BR IF DONE ALL PATTERNS
2496 006440 105067 172544 2$: CLRB $TMP3      ;INIT A LINE COUNTER
2497 006444 142711 000017 3$: BICB #17,(R1)   ;INIT LINE SELECT BITS IN "SCR"
2498 006450 156711 172534  BISB $TMP3,(R1)  ;SELECT A LINE IN SCR
2499 006454 142711 000060  BICB #50,(R1)   ;SO WE CLEAR ALL THE MEM EXT BITS
2500 006460 005061 000006  CLR CAR(R1) ;CLEAR A CAR
2501 006464 105267 172520  INCB $TMP3      ;GENERATE NXT LINE NO.
2502 006470 122767 000020 172512  CMPB #20,$TMP3  ;CLEARED THE WHOLE THING ?
2503 006476 001362          BNE 3$          ;BR IF NOT
2504
2505 006500 004767 015776 4$: JSR PC,SELINE   ;GO SELECT A LINE NO.
2506 006504 000750          BR 1$          ;BR IF DONE ALL LINES
2507 006506 156711 021500  BISB LINE,(R1)  ;SET UP LINE SELECT BITS
2508 006512 156711 172466  BISB $TMP1,(R1) ;SET UP MEM EXT BIT PATTERN
2509 006516 012761 000000 000004  MOV #0,LPR(R1)  ;SCOPE SYNC
2510 006524 012761 000000 000006  MOV #0,CAR(R1) ;WRITE EXT BITS IN THIS LOCATION
2511
2512 006532 105067 172454          CLRB $TMP4      ;INIT A LINE COUNTER
2513 006536 016704 172444 5$: MOV $TMP2,R4   ;SET UP S/B DATA
2514 006542 142711 000017  BICB #17,(R1)   ;INIT SELECT BITS IN "SCR"
2515 006546 156711 172440  BICB $TMP4,(R1) ;SET SELECT BITS IN SCR
2516 006552 012761 000000 000014  MOV #0,BKR(R1) ;SCOPE SYNC
2517 006560 016103 000006  MOV CAR(R1),R3 ;READ THE SELECTED "CAR"
2518 006564 011203          MOV (R2),R3    ;GET THE WAS DATA
2519 006566 042703 177477  BIC #177477,R3  ;CLEAR JUNK BITS
2520 006572 126767 021414 172412  CMPB LINE,$TMP4 ;LINE UNDER TEST ??
2521 006600 001401          BEQ 6$         ;BR IF YES
2522 006602 005004          CLR R4        ;MAKE S/B DATA = 000000
2523 006604 020304 6$: CMP R3,R4     ;WERE MEM EXT BITS CORRECT ?
2524 006606 001412          BEQ 7$         ;BR IF YES
2525
2526 006610 004767 015534          JSR PC,SUER2   ;GO SET UP ERROR INFO
2527 006614 004567 015754          JSR R5,SUINJM ;GO SET LINE NO. IN MSG BUFFER
2528 006620 001212          $TMP4
2529 006622 031045          EM7+47
2530 006624 012767 006440 172256  MOV #2$, $LPERR ;SET UP ERROR LOOP RETURN
2531 006632 104007          ERROR 7       ;MEM EXT BITS READ INCORRECTLY
2532
2533 006634 105267 172352 7$: INCB $TMP4    ;GENERATE NXT LINE NO.
2534 006640 122767 000020 172344  CMPB #20,$TMP4 ;DONE ALL LINES
2535 006646 001674          BEQ 2$        ;BR IF YES

```



J14

MAINDEC-11-DZDMM-B  
DZDHMB.P11 T24

MACY11 27(732) 23-SEP-76 14:33 PAGE 60  
TEST THAT "CAR" MEMORY EXT BITS SET/CLR PROPERLY

SEQ 0178

2536 006650 000732

BR SS

;GO CHECK NEXT LINE

2537  
2538  
2539  
2540 006652 000004  
2541  
2542  
2543  
2544  
2545  
2546  
2547  
2548  
2549  
2550  
2551  
2552  
2553  
2554  
2555  
2556  
2557  
2558  
2559  
2560  
2561  
2562  
2563  
2564  
2565  
2566  
2567  
2568  
2569  
2570  
2571  
2572  
2573  
2574  
2575  
2576  
2577  
2578  
2579  
2580  
2581  
2582  
2583  
2584  
2585  
2586 006654 012767 006732 172226  
2587 006662 010102  
2588 006664 016703 020304  
2589 006670 012723 006762  
2590 006674 116723 021306  
2591 006700 105723  
2592 006702 012723 007004

::\*\*\*\*\*  
: \*TEST 25 TEST INTR. ENAB. BITS - INTR. CONDITION DISABLED  
: \*\*\*\*\*  
†ST25: SCOPE  
.REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT NO TRANSMITTER OR RECEIVER INTERRUPT OCCURS WHEN THE ENABLE BIT IS SET WITH OUT THE INTERRUPTING CONDITION ACTIVE. A BIT MASK (INTMSK: 030100) IS USED TO DEFINE THE I.E. BITS. IN THE "SCR" (BITS 13, 12, AND 06). THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP THE XMIT AND RCVR VECTORS
2. SELECT AN I.E. BIT TO TEST
3. INIT THE SP AND LOCK OUT INTERRUPTS
4. SET THE SELECTED BIT IN THE "SCR"
5. CLEAR THE PSW TO ALLOW INTR
6. IF NO INTR: REPEAT 2 THRU 5 UNTIL ALL BITS TESTED
7. IF INTR: REPORT ERROR AND CONTINUE WITH NEXT BIT TO TEST

ALL ERRORS ARE REPORTED AND THEN THE TEST RESUMES WITH THE NEXT BIT IN SEQUENCE .

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 11] IS CALLED TO REPORT RCVR INTR FAULTS
- 2.) [ERROR 12] IS CALLED TO REPORT XMITTR INTR FAULTS

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

- 1.) PROBLEM IS MOST LIKELY THE M7289 MODULE IF THIS IS THE FIRST TEST TO FAIL.
- 2.) SET UP SCOPE ERROR LOOP AND BACKTRACK THROUGH THE LOGIC STARTING WITH THE KEY LOGIC BELOW.

KEY LOGIC:  
\*\*\*\*\*

```

M7289 SH6 XMIT INT REQ H FM1
RCV INT REQ H DP1

%
MOV #3$, $LPERR ;SET UP THE ERROR LOOP RETURN
MOV R1, R2 ;MAKE IT REGADR TOO
MOV DHVCT, R3 ;GET FIRST VECTOR ADDRESS
MOV #4$, (R3)+ ;GO TO 3$ IF RCVR INTR
MOVB DHRVLV, (R3)+
TSTB (R3)+ ;UPDATE POINTER
MOV #5$, (R3)+ ;GO TO 5$ IF XMITTR INTR
```

2593	005706	116713	021275		MOV	DHTLVL,(R3)	
2594	006712	012705	000001		MOV	#1,R5	:INIT BIT TEST MARKER
2595	006716	030567	020644	1\$:	BIT	R5,INTMSK	:TEST THIS BIT ??
2596	006722	001003			BNE	3\$	:BR IF YES
2597	006724	006305		2\$:	ASL	R5	:SHIFT THE MARKER
2598	006726	001437			BEQ	6\$	:BR IF TESTED ALL REQUIRED BITS
2599	006730	000772			BR	1\$	:GO TEST FOR THIS ONE
2600							
2601	006732	012706	001100	3\$:	MOV	#STACK,SP	:RESET SP FOR ERROR LOOPING
2602	006736	004767	020150		JSR	PC,CHPS2	:GO LOCK OUT INTR
2603	006742	012711	004000		MOV	#BIT11,(R1)	:CLEAR THE DH11 INTERFACE
2604	006746	010504			MOV	R5,R4	:SET UP S/B DATA
2605	006750	050511			BIS	R5,(R1)	:SET THE TEST I.E. BIT
2606	006752	004767	020120		JSR	PC,CHPS1	:GO CLEAR PSW
2607	006756	000240			NOP		:WAIT A BIT TO ALLOW INTR
2608	006760	000761			BR	2\$	:OK - GO DO NEXT I.E. BIT
2609							
2610	006762	004767	020140	4\$:	JSR	PC,SAPS	:SAVE THE ERROR PSW
2611	006766	011103			MOV	(R1),R3	:GET THE WAS DATA
2612	006770	004767	015360		JSR	PC,SUER2A	:GO SET UP ERROR INFO
2613	006774	104011			ERROR	11	:DH11 RCVR SHOULD NOT HAVE INTERRUPTED
2614	006776	012716	006724		MOV	#2\$,(SP)	:SET UP TO RETURN
2615	007002	000002			RTI		:RETURN TO TEST NEXT BIT
2616							
2617	007004	004767	020116	5\$:	JSR	PC,SAPS	:SAVE THE ERROR PSW
2618	007010	011103			MOV	(R1),R3	:GET THE WAS DATA
2619	007012	004767	015336		JSR	PC,SUER2A	:GO SET UP ERROR INFO
2620	007016	104012			ERROR	12	:XMITTER SHOULD NOT HAVE INTERRUPTED
2621	007020	012716	006724		MOV	#2\$,(SP)	:SET UP TO RETURN
2622	007024	000002			RTI		:RETURN TO TEST NEXT BIT
2623							
2624	007026	012706	001100	6\$:	MOV	#STACK,SP	:RESET THE SP JUST IN CASE
2625	007032	004767	017660		JSR	PC,RES+RP	:GO RESTORE TRAP CATCHER IN VECTOR

2626  
2627  
2628  
2629  
2630  
2631  
2632  
2633  
2634  
2635  
2636  
2637  
2638  
2639  
2640  
2641  
2642  
2643  
2644  
2645  
2646  
2647  
2648  
2649  
2650  
2651  
2652  
2653  
2654  
2655  
2656  
2657  
2658  
2659  
2660  
2661  
2662  
2663  
2664  
2665  
2666  
2667  
2668  
2669  
2670  
2671  
2672  
2673  
2674  
2675  
2676  
2677  
2678  
2679  
2680  
2681

007036 000004

```
*****
*TEST 26 TEST CHAR. AVAIL. I.E. WITH INTR. CONDITION ACTIVE
*****
TST26: SCOPE
.REM %
TEST ABSTRACT:
*****
```

THIS TEST USES MAIN1. MODE (SCRO9=1) TO SET THE CHAR AVAIL BIT (SCR7) TO GENERATE A RCVR INTERRUPT THROUGH THE PROPER VECTOR. THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP THE VECTORS
2. ISSUE DH11 "MASTER CLR", RESET THE SP, AND LOCK OUT INTR
3. PRINT THE DH11 TO GENERATE A RCVR INTR
4. CLEAR THE PSW TO ALLOW INTR
5. REPORT NO RCVR INTR OR FALSE XMITTR INTR.

ALL ERRORS ARE REPORTED AND THEN THE TEST RESETS THE VECTOR AND SP AND CONTINUES TO THE NEXT TEST IN THE PROGRAM.

ERRORS:  
\*\*\*\*\*

- 1.) [ERROR 13] IS CALLED TO REPORT RCVR INTR FAULTS
- 2.) [ERROR 12] IS CALLED TO REPORT XMITTR INTR FAULTS

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

- 1.) IF NO RCVR INTR OCCURRED THE PROBLEM IS EITHER SECTION "A" OF THE M7821 OR THE M7289 - SH6.
- 2.) IF A FALSE XMIT INTR OCCURRED THE PROBLEM IS MOST LIKELY THE M7821 GENERATING AN INCORRECT VECTOR ADDRESS.

KEY LOGIC:  
\*\*\*\*\*

M7289	SH6	E31-12	
M7821	SEC "A"	BUS A BR L	U2
		BUS SACK L	T2
		BUS BG IN H	B1
		"A" MASTER L	N1
		VECTOR BIT 02 H 02	

NOTE: REMEMBER THAT PROBLEMS IN THIS AREA COULD BE CAUSED BY ANY DEVICE IN THE SYSTEM INCLUDING THE "CPU". SYSTEM RE-CONFIGURATION TO ISOLATE THE FAULTY SUB-SYSTEM MAY BE REQUIRED.

007040 012767 007076 172042 %  
007046 010102

```
MOV #1$, $LPERR ;SET UP THE ERROR LOOP RETURN
MOV R1,R2 ;MAKE IT REGADR TOO
```

# N14

MAINDEC-11-DZDMM-B  
DZDMMB.P11 T26

MACY11 27(732) 23-SEP-76 14:33 PAGE 64  
TEST CHAR. AVAIL. I.E. WITH INTR. CONDITION ACTIVE

SEQ 0182

2682	007050	016703	020120		MOV	DHVCT,R3	:GET FIRST VECTOR ADDR
2683	007054	012723	007206		MOV	#3\$, (R3)+	:GO TO 3\$ IF RCVR INTRS
2684	007060	116723	021122		MOVB	DHRLVL, (R3)+	
2685	007064	105723			TSTB	(R3)+	:UPDATE POINTER
2686	007066	012723	007162		MOV	#2\$, (R3)+	:GO TO 3\$ ON XMITTR INTRS
2687	007072	116713	021111		MOVB	DHTLVL, (R3)	
2688	007076	012711	004000	1\$:	MOV	#BIT11, (R1)	:CLR THE DH11
2689	007102	012706	001100		MOV	#STACK, SP	:RESET THE SP FOR ERROR LOOPS
2690	007106	004767	020000		JSR	PC, CHPS2	:GO LOCK OUT INTRS
2691	007112	012711	001000		MOV	#BIT09, (R1)	:SET MAINT MODE BIT
2692	007116	052711	000100		BIS	#BIT06, (R1)	:SET CHAR AVAILABLE I.E. BIT
2693	007122	052711	000200		BIS	#BIT07, (R1)	:SET THE CHAR AVAIL BIT TO FORCE INTR
2694	007126	004767	017744		JSR	PC, CHPS1	:GO CLEAR PSW
2695	007132	000240			NOP		:GIVE IT A LITTLE TIME
2696							
2697	007134	004767	017766		JSR	PC, SAPS	:SAVE THE ERROR PSW
2698	007140	011103			MOV	(R1), R3	:GET THE WAS DATA
2699	007142	005011			CLR	(R1)	:CLEAR OUT THE SCR
2700	007144	005011			CLR	(R1)	
2701	007146	012704	001300		MOV	#1300, R4	:SET UP S/B DATA
2702	007152	004767	015176		JSR	PC, SUER2A	:GO SET UP ERROR INFO
2703	007156	104013			ERROR	13	:TIMED OUT AWAITING CHAR AVAIL INTR
2704	007160	000412			BR	3\$	:GO EXIT TEST
2705							
2706	007162	004767	017740	2\$:	JSR	PC, SAPS	:SAVE THE ERROR PSW
2707	007166	011103			MOV	(R1), R3	:GET WAS DATA
2708	007170	012704	001300		MOV	#1300, R4	:SET UP S/B DATA
2709	007174	005011			CLR	(R1)	:CLR OUT SCR REG
2710	007176	005011			CLR	(R1)	
2711	007200	004767	015150		JSR	PC, SUER2A	:GO SET UP ERROR INFO
2712	007204	104012			ERROR	12	:UNEXPECTED XMITTR INTR
2713							
2714	007206	012706	001100	3\$:	MOV	#STACK, SP	:RESET THE SP
2715	007212	004767	017500		JSR	PC, RESTRP	:GO RESTORE TRAP CATCHER

007216 000004  
007217 000004  
007218 000004  
007219 000004  
007220 000004  
007221 000004  
007222 000004  
007223 000004  
007224 000004  
007225 000004  
007226 000004  
007227 000004  
007228 000004  
007229 000004  
007230 000004  
007231 000004  
007232 000004  
007233 000004  
007234 000004  
007235 000004  
007236 000004  
007237 000004  
007238 000004  
007239 000004  
007240 000004  
007241 000004  
007242 000004  
007243 000004  
007244 000004  
007245 000004  
007246 000004  
007247 000004  
007248 000004  
007249 000004  
007250 000004  
007251 000004  
007252 000004  
007253 000004  
007254 000004  
007255 000004  
007256 000004  
007257 000004  
007258 000004  
007259 000004  
007260 000004  
007261 000004  
007262 000004  
007263 000004  
007264 000004  
007265 000004  
007266 000004  
007267 000004  
007268 000004  
007269 000004  
007270 000004  
007271 000004  
007272 000004  
007273 000004  
007274 000004  
007275 000004  
007276 000004  
007277 000004  
007278 000004  
007279 000004  
007280 000004  
007281 000004  
007282 000004  
007283 000004  
007284 000004  
007285 000004  
007286 000004  
007287 000004  
007288 000004  
007289 000004  
007290 000004  
007291 000004  
007292 000004  
007293 000004  
007294 000004  
007295 000004  
007296 000004  
007297 000004  
007298 000004  
007299 000004  
007300 000004

\*\*\*\*\*  
\*TEST 27 TEST SILO OVFLW. I.E. WITH INTR. CONDITION ACTIVE  
\*\*\*\*\*  
TEST27: SCOPE  
REM %  
TEST ABSTRACT  
\*\*\*\*\*

THIS TEST USES MAINT. MODE (SCR09=1) TO ENABLE SILO FULL INTERRUPT. THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP XMIT AND RCVR VECTORS
2. RESET THE DH11 AND S.P. - THE LOCK OUT INTR.
3. PRIME DH11 TO GENERATE SILO FULL INTR. - ALLOW INTR.
4. REPORT ERROR IF NO RCVR. INTR OCCURS OR A FALSE XMIT INTR. DOES OCCUR
5. AFTER REPORTING ANY ERRORS DETECTED RESET THE SP AND VECTORS THEN GO TO TEST 30

ERRORS:  
\*\*\*\*\*

1. [ERROR 43] IS CALLED TO REPORT NO RCVR INTR OCCURRED
2. [ERROR 12] IS CALLED TO REPORT FALSE TRANSMITTER INTF.

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. IF THE RECEIVER INTR FAILED TO INTERRUPT PROBLEM IS MOST LIKELY THE M7289 MODULE
2. IF A FALSE XMITTR INTR OCCURRED PROBLEM IS MOST LIKELY THE M7291 MODULE

KEY LOGIC:  
\*\*\*\*\*

M7289 SHG E35, E50, OR E31  
SCR 14 H (STORAGE) DS1

M7821 "B" SECTION

%  
MOV #15, SLPERR ;SET UP THE ERROR LOOP RETURN  
MOV R1, R2 ;MAKE IT REGADR TOO  
MOV DHVCT, R3 ;GET FIRST VECTOR ADDR  
MOV #35, (R3)+ ;GO TO 35 IF RCVR INTR  
MOVB DHRLVL, (R3 +  
TSTB (R3)+ ;UPDATE POINTER  
MOV #25, (R3)+ ;GO TO 25 ON XMITTR INTR  
MOVB DHTLVL, (R3)  
15: MOV #BIT11, (R1) ;CLR THE DH11  
MOV #STACK, SP ;RESET THE SP FOR ERROR LOOPS  
JSR PC, CHPS2 ;GO LOCK OUT INTR  
MOV #BIT09, (R1) ;SET MAINT MODE BIT



C15

MAINDEC-11-DZDMM-B  
DZDMMB.P11 T27

MAY11 27.732) 23-SEP-76 14:33 PAGE 66  
TEST SILO OVFLW. I.E. WITH INTR. CONDITION ACTIVE

SEQ 0184

007326	052711	040000		BIS	#BIT14,(R1)	:SET SILO OVFLW I.E. BIT
007328	052711	010000		BIS	#BIT12,(R1)	:SET THE SILO FULL BIT TO FORCE INTR
007306	004767	017564		JSR	PC,CHPS1	:GO CLEAR PSW
007312	000240			NOP		:GIVE IT A LITTLE TIME
007314	004767	017606		JSR	PC,SAPS	:SAVE THE ERROR PSW
007320	011103			MOV	(R1),R3	:GET THE WAS DATA
007322	005011			CLR	(R1)	:CLEAR OUT THE SCR
007324	005011			CLR	(R1)	
007326	012704	051000		MOV	#51000,R4	:SET UP S/B DATA
007332	004767	015016		JSR	PC,SUER2A	:GO SET UP ERROR INFO
007336	104043			ERROR	43	:TIMED OUT AWAITING SILO OVFLW INTR
007340	000412			BR	25	:GO EXIT TEST
007342	004767	017560	25:	JSR	PC,SAPS	:SAVE THE ERROR PSW
007346	011103			MOV	(R1),R3	:GET WAS DATA
007350	012704	051000		MOV	#51000,R4	:SET UP S/B DATA
007354	005011			CLR	(R1)	:CLR OUT SCR REG
007356	005011			CLR	(R1)	
007360	004767	014770		JSR	PC,SUER2A	:GO SET UP ERROR INFO
007364	104012			ERROR	12	:UNEXPECTED XMITTR INTR
007366	012706	001100	35:	MOV	#STACK,SP	:RESET THE SP
007372	004767	017320		JSR	PC,RESTRP	:GO RESTORE TRAP CATCHER

0

007376 000004

```

*****
: TEST 30 TEST NON EX MEM I.E. WITH INTR. CONDITION ACTIVE
*****
TST30: SCOPE
REM %
TEST ABSTRACT:
*****

```

THIS TEST VERIFIES THAT THE NON-EX-MEM BIT (SCR10) CAN CAUSE A TRANSMITTER INTERRUPT VIA THE PROPER VECTOR. THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP XMIT AND RCVR VECTORS
2. CLEAR THE DH11, RESET SP, AND LOCK OUT INTR
3. PRIME DH11 TO GENERATE XMIT INTR IN MAINT. MODE
4. ALLOW INTR.
5. REPORT ERROR IF NO XMIT INTR OCCURS OR IF A FALSE RCVR INTR OCCURS
6. REST SP AND VECTORS THEN GO TO TEST 31

ERRORS:  
\*\*\*\*\*

1. [ERROR 44] IS CALLED IF NON-EX-MEM FAILS TO GENERATE XMIT INTR
2. [ERROR 11] IS CALLED IF FALSE RCVR INTR OCCURS

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. IF THE NON-EX-MEM INTERRUPT FAILS TO OCCUR PROBLEM IS MOST LIKELY THE M7289 MODULE
2. IF A FALSE RCVR INTR OCCURS PROBLEM IS MOST LIKELY THE M7289 OR THE M7281 MODULES.

KEY LOGIC:  
\*\*\*\*\*

M7289 SH6 SCR 10 H (NO EX MEM) FL1  
E35, E41, OR E48

```

%
007400 012767 007436 171502 MOV #15, $LPERR ;SET UP THE ERROR LOOP RETURN
007406 010102 MOV R1, R2 ;MAKE IT REGADR TOO
007410 016733 017560 MOV DHVCT, R3 ;GET FIRST VECTOR ADDR
007414 012723 007522 MOV #2$, (R3)+ ;GO TO 2$ IF RCVR INTR
007420 116723 020562 MOVB DHR(LVL, (R3)+
007424 105723 TSTB (R3)+ ;UPDATE POINTER
007426 012723 007546 MOV #3$, (R3)+ ;GO TO 3$ ON XMITTR INTR
007432 116713 020551 MOVB DHT(LVL, (R3)
15: 007436 012711 004000 MOV #BIT11, (R1) ;CLR THE DH11
007442 012706 001100 MOV #STACK, SP ;RESET THE SP FOR ERROR LOOPS
007446 004767 017440 JSR PC, CHPS2 ;GO LOCK OUT INTR
007452 012711 001000 MOV #BIT09, (R1) ;SET MAINT MODE BIT

```

# E15

MAINDEC-11-DZDMM-6  
DZDMMB.P11 T30

MACY11 27(732) 23-SEP-76 14:33 PAGE 69  
TEST NON EX MEM I.E. WITH INTR. CONDITION ACTIVE

SEQ 0196

007456	052711	020000		BIS	#BIT13,(R1)	:SET XMITTR I.E. BIT
007462	052711	002000		BIS	#BIT10,(R1)	:SET THE NON EX MEM BIT TO FORCE INTR
007466	004767	017404		JSR	PC,CHPS1	:GO CLEAR PSW
007472	000240			NOP		:GIVE IT A LITTLE TIME
007474	004767	017426		JSR	PC,SAPS	:SAVE THE ERROR PSW
007500	011103			MOV	(R1),R3	:GET THE WAS DATA
007502	005011			CLR	(R1)	:CLEAR OUT THE SCR
007504	005011			CLR	(R1)	
007506	012704	023000		MOV	#23000,R4	:SET UP S/B DATA
007512	004767	014636		JSR	PC,SUER2A	:GO SET UP ERROR INFO
007516	104044			ERROR	44	:TIMED OUT AWAITING NON EX MEM INTR
007520	000412			BR	3\$	:GO EXIT TEST
007522	004767	017400	2\$:	JSR	PC,SAPS	:SAVE THE ERROR PSW
007526	011103			MOV	(R1),R3	:GET WAS DATA
007530	012704	023000		MOV	#23000,R4	:SET UP S/B DATA
007534	005011			CLR	(R1)	:CLR OUT SCR REG
007536	005011			CLR	(R1)	
007540	004767	014610		JSR	PC,SUER2A	:GO SET UP ERROR INFO
007544	104011			ERROR	11	:UNEXPECTED RCVR INTR
007546	012706	001100	3\$:	MOV	#STACK,SP	:RESET THE SP
007552	004767	017140		JSR	PC,RESTRP	:GO RESTORE TRAP CATCHER

F15

MAINDEC-11-DZDMM-8  
DZDMMB.P11 T31

MACY11 27(732) 23-SEP-76 14:33 PAGE 69  
TEST XMITTR DONE I.E. WITH INTR. CONDITION ACTIVE

SEQ 0197

2915  
2916  
2917  
2918  
2919  
2920  
2921  
2922  
2923  
2924  
2925  
2926  
2927  
2928  
2929  
2930  
2931

007556 000004

\*\*\*\*\*  
:TEST 31 TEST XMITTR DONE I.E. WITH INTR. CONDITION ACTIVE  
\*\*\*\*\*  
†ST31: SCOPE  
.REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT XMIT DONE (SCR15) CAN BE SET IN MAINT.  
MODE TO CAUSE A XMITTR INTR VIA THE PROPER VECTOR. THE TEST SEQUENCE  
IS AS FOLLOWS:

1. SET UP XMIT AND RCVR VECTORS
2. CLEAR THE DH11, RESET SP, AND LOCK OUT INTRs
3. PRIME DH11 TO GENERATE "XMIT DONE" INTR
4. CLEAR PSW TO ALLOW INTRs
5. REPOT ERROR IF XMITTR FAILS TO INTR OR A FALSE RCVR INTR OCCURS

ERRORS:  
\*\*\*\*\*

1. [ERROR 45] IS CALLED TO REPORT "XMIT DONE" INTR FAILED TO OCCUR
2. [ERROR 11] IS CALLED TO REPORT FALSE RCVR INTRs

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. IF NO XMIT INTR OCCURS PROBLEM IS MOST LIKELY THE M7289 MODULE
2. IF A FALSE RCVR INTR. OCCURS PROBLEM IS MOST LIKELY THE M7821 MODULE.

KEY LOGIC:  
\*\*\*\*\*

M7289 SH6 SCR 15 H (XMIT) FR2  
E48. E50

```

%
MOV #15, $LPERR ;SET UP THE ERROR LOOP RETURN
MOV R1, R2 ;MAKE IT REGADR TOO
MOV DHVCT, R3 ;GET FIRST VECTOR ADDR
MOV #2$, (R3)+ ;GO TO 2$ IF RCVR INTRs
MOVVB DHRLVL, (R3)+
TSTB (R3)+ ;UPDATE POINTER
MOV #3$, (R3)+ ;GO TO 3$ ON XMITTR INTRs
MOVVB DHTLVL, (R3)
1$: MOV #BIT11, (R1) ;CLR THE DH11
MOV #STACK, SP ;RESET THE SP FOR ERROR LOOPS
JSR PC, CHPS2 ;GO LOCK OUT INTRs
MOV #BIT09, (R1) ;SET MAINT MODE BIT
BIS #BIT13, (R1) ;SET XMIT DONE I.E. BIT
BIS #BIT15, (R1) ;SET THE XMITTR DONE BIT TO FORCE INTR

```

0  
x

# G15

MAINDEC-11-DZDMM-8  
DZDMMB.P11 T31

MACY11 27(732) 23-SEP-76 14:33 PAGE 70  
TEST XMITTR DONE I.E. WITH INTR. CONDITION ACTIVE

SEQ 0198

2932	007646	004767	017224		JSR	PC,CHPS1		;GO CLEAR PSW
2933	007652	000240			NOP			;GIVE IT A LITTLE TIME
2934								
2935	007654	004767	017246		JSR	PC,SAPS		;SAVE THE ERROR PSW
2936	007660	011103			MOV	(R1),R3		;GET THE WAS DATA
2937	007662	005011			CLR	(R1)		;CLEAR OUT THE SCR
2938	007664	005011			CLR	(R1)		
2939	007666	012704	121000		MOV	#121000,R4		;SET UP S/B DATA
2940	007672	004767	014456		JSR	PC,SUER2A		;GO SET UP ERROR INFO
2941	007676	104045			ERROR	45		;TIMED OUT AWAITING XMIT DONE INTR
2942	007700	000412			BR	33		;GO EXIT TEST
2943								
2944	007702	004767	017220	2\$:	JSR	PC,SAPS		;SAVE THE ERROR PSW
2945	007706	011103			MOV	(R1),R3		;GET WAS DATA
2946	007710	012704	121000		MOV	#121000,R4		;SET UP S/B DATA.
2947	007714	005011			CLR	(R1)		;CLR OUT SCR REG
2948	007716	005011			CLR	(R1)		
2949	007720	004767	014430		JSR	PC,SUER2A		;GO SET UP ERROR INFO
2950	007724	104011			ERROR	11		;UNEXPECTED RCVR INTR
2951								
2952	007726	012706	001100	3\$:	MOV	#STACK,SP		;RESET THE SP
2953	007732	004767	016760		JSR	PC,RESTAP		;GO RESTORE TRAP CATCHER

2954  
2955  
2956  
2957  
2958  
2959  
2960  
2961  
2962  
2963  
2964  
2965  
2966  
2967  
2968  
2969  
2970  
2971  
2972  
2973  
2974  
2975  
2976  
2977  
2978  
2979  
2980  
2981  
2982  
2983  
2984  
2985  
2986  
2987  
2988  
2989  
2990  
2991  
2992  
2993  
2994  
2995  
2996  
2997  
2998  
2999  
3000  
3001  
3002  
3003  
3004  
3005  
3006  
3007  
3008  
3009

007736 000004

```
::*****  
:*TEST 32 BASIC TRANSMITTER "NPR" LOGIC TEST 1  
:*****  
†ST32: SCOPE  
REM %  
TEST ABSTRACT:  
*****
```

THIS TEST TRANSMITS A SINGLE BYTE FROM LOCATION 0 ON ALL SELECTED LINES (AS SELECTED BY THE CONFIGURATION PARAMETER "LINSEL:") ONE AT A TIME. THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP THE XMITTR VECTOR
2. SELECT A LINE # TO TEST
3. RESET THE SP
4. CLEAR ALL LOCATIONS IN "CAR" AND "BCR" MEMORIES
5. LOCK OUT INTRs AND CLEAR THE DH11
6. PRIME DH11 TO XMIT ONE CHAR FROM LOCATION 0  
[9600 BAUD, 5-BITS, 1 STOP BIT]
7. ACTIVATE SELECTED XMITTR AND ENABLE XMIT DONE INTR
8. CLEAR PSW TO ALLOW INTR.
9. ACTIVATE TIMER TO WAIT FOR XMIT DONE INTR
10. IF TIMEOUT OCCURS REPORT ERROR AND RESTART AT STEP 2
11. IF XMIT INTERRUPT OCCURS CHECK THE FOLLOWING CONDITIONS AND REPORT ANY ERRORS:
  - A. XMIT DONE (SCR15=1) SET
  - B. "BAR" BIT GOT CLEARED
  - C. "CAR" REGISTER GOT INCREMENTED TO +1
  - D. "BCR" REGISTER GO INCREMENTED TO 0
12. REPEAT STEP 2 THRU 11 UNTIL ALL SELECTED LINES TESTED
13. AFTER TESTING ALL LINES CLEAR THE DH11, RESET THE VECTOR CLEAR PSW, RESET SP, AND GO TO TEST 33.

ERRORS:  
\*\*\*\*\*

1. [ERROR 15] IS CALLED IF XMIT DONE FAILS TO INTR ON TIME
2. [ERROR 14] IS CALLED IF XMIT DONE NOT SET
3. [ERROR 14] IS CALLED IF "BAR" BIT FAILED TO CLEAR
4. [ERROR 14] IS CALLED IF "CAR" NOT INCREMENTED PROPERLY
5. [ERROR 14] IS CALLED IF "BCR" NOT INCREMENTED PROPERLY

ALL ERROR MESSAGE HEADERS INCLUDE THE LINE NO. OF THE FAILING LINE.

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

(NOTE: USE SR09=1 TO LOCK ON FAILING LINE AND SR13=1 TO INHIBIT ERROR PRINTOUT TO MINIMIZE SCOPE LOOP.)

DEBUG:  
\*\*\*\*\*

1. IF ALL LINES FAIL TO INTERRUPT ON TIME, SUSPECT LOSS OF 9600 BAUD

3010  
3011  
3012  
3013  
3014  
3015  
3016  
3017  
3018  
3019  
3020  
3021  
3022  
3023  
3024  
3025  
3026  
3027  
3028  
3029  
3030  
3031  
3032  
3033  
3034  
3035  
3036  
3037  
3038  
3039  
3040  
3041  
3042  
3043  
3044  
3045  
3046  
3047  
3048  
3049  
3050  
3051  
3052  
3053  
3054  
3055  
3056  
3057  
3058  
3059  
3060  
3061  
3062  
3063  
3064  
3065

- 2. CLOCK SIGNAL OR BYTE COUNT DECODER ON M7278 SH3 (XMIT FINISHED PULSE L)  
IF GROUP OF 8 LINES <15:08> OR <07:00> FAIL TO INTERRUPT ON TIME, SUSPECT  
THE BUFFERED CLOCK SIGNALS (TOP AND BOT) ON THE M7288 SH3
- 3. IF ONLY ONE LINE FAILS TO INTERRUPT ON TIME, SUSPECT LOSS OF CLOCK IN  
LINE MULTIPLEXORS M7288 SH4-SH11.
- 4. IF LINE INTERRUPTED OK BUT "SCR", "BAR", "CAR", OR "BCR" WAS INCORRECT  
REFER TO KEY LOGIC SIGNALS BELOW.

KEY LOGIC:  
\*\*\*\*\*

XMIT DONE FAILED TO SET:

```

M7289 SH6 SCR15 H FR2
M7278 SH3 XMIT FINISHED PULSE L ARI

```

"BAR" BIT FAILED TO CLEAR:

```

M7278 SH3 CLR BAR <15:00> L
SH5 BAR <15:12> H E54, E55 (7474)
SH6 BAR <11:08> H E62, E63 (7474)
SH7 BAR <07:04> H E70, E71 (7474)
SH8 BAR <03:00> H E78, E79 (7474)

```

"CAR" REG NOT INCREMENTED:

```

M7277 SH6 END CYCLE PULSE DLY H FL2
SH5 AND SH6 "CAR" MEMORY LOGIC
M796 END CYCLE H P2

```

"BCR" REG NOT INCREMENTED:

```

M796 END CYCLE L N2
M7278 SH3 AND SH4 "BCR" MEMORY LOGIC

```

```

007740 012767 007774 171142
007746 016703 017222
007752 062703 000004
007756 012723 010140
007762 116713 020221
007766 004767 014510
007772 000552

007774 012706 001100
010000 010102
010002 012704 120000
010006 156704 020200
010012 004767 014636
010016 004767 017070
010022 012711 004000
010026 156711 020160
010032 012761 177777 000010
010040 012751 033500 000004
010046 056751 017132 000012

```

```

%
MOV #2$, $LPERR ;SET UP ERROR LOOP RETURN
MOV DHVCT, R3 ;GET THE FIRST VECTOR ADDRESS
ADD #4, R3 ;POINT TO XMITTR ENTRY
MOV #4$, (R3)+ ;GO TO 4$ ON XMITTR INTR
MOVVB DHTLVL, (R3)
1$: JSR PC, SELINE ;GO SELECT A LINE NO. TO TEST
BR B$ ;BR IF TESTED ALL SELECTED LINES

2$: MOV #STACK, SP ;RESET SP FOR ERROR LOOPS
MOV R1, R2 ;SET UP REGADR
MOV #120000, R4 ;SET UP S/B DATA
BISB LINE, R4
JSR PC, CLCABC ;GO CLEAR CAR AND BCR MEMORIES
JSR PC, CHPS2 ;GO LOCK OUT INTR
MOV #BIT11, (R1) ;CLEAR THE DH11 INTERFACE
BISB LINE, (R1) ;SELECT A LINE NO.
MOV #-1, BCR(R1) ;SET BYTE COUNT TO -1
MOV #33500, LPR(R1) ;SET UP LINE PARAMETERS
BIS LINMSK, BAR(R1) ;ACTIVATE SELECTED LINE

```

```

3066 010054 052711 020000      B1S      #BIT13,(R1)      ;ENABLE INTERRUPT ON XMIT DONE
3067 010060 004767 017012      JSR      PC,CHPS1  ;GO CLEAR PSW
3068
3069 010064 012767 000001 020146      MOV      #1,TIMEA  ;INIT TIMER A
3070 010072 005067 020144      CLR      TIMEB    ;INIT TIMER B
3071 010076 000240      NOP      ;DO NOTHING WAIT
3072 010100 004767 016640      JSR      PC,TIMEIT ;CALL TIMER
3073 010104 000774      BR       3$       ;TIMER ROUTINE WILL MOVE RETURN PC AROUND
3074                                     ;THIS BRANCH IF TIMEOUT OCCURS
3075
3076 010106 004767 017014      JSR      PC,SAPS   ;SAVE THE ERROR PSW
3077 010112 011103      MOV      (R1),R3  ;GET THE WAS DATA
3078 010114 042703 000200      BIC      #BIT07,R3 ;WE'RE NOT INTERESTED IN THIS BIT
3079 010120 004767 014230      JSR      PC,SUER2A ;GO SET UP ERROR INFO
3080 010124 004567 014444      JSR      RS,SUNUM  ;GO SET LINE NO. IN ERROR MSG
3081 010130 030212      LINE
3082 010132 031412      EM15+43
3083 010134 104015      ERROR    15      ;TIMEOUT WHILE AWAITING XMIT INTR
3084 010136 000713      BR       1$      ;GO TEST NEXT LINE
3085
3086 010140 005711      4$:      TST      (R1)    ;DID XMIT DONE SET ??
3087 010142 100411      BMI     5$      ;BR IF YES
3088
3089 010144 004767 016756      JSR      PC,SAPS   ;SAVE THE ERROR PSW
3090 010150 011103      MOV      (R1),R3  ;GET THE WAS DATA
3091 010152 004767 014176      JSR      PC,SUER2A ;GO SET UP ERROR INFO
3092 010156 004767 000174      JSR      PC,9$    ;GO SET UP SOME ERROR STUFF
3093 010162 104014      ERROR    14      ;XMIT DONE FAILED TO SET
3094 010164 000700      BR       1$      ;GO TEST NEXT LINE
3095
3096 010166 016103 000012      5$:      MOV      BAR(R1),R3 ;GET WAS DATA FROM "BAR"
3097 010172 001413      BEQ     6$      ;BR IF BAR BIT GOT CLEARED
3098
3099 010174 004767 016726      JSR      PC,SAPS   ;SAVE THE ERROR PSW
3100 010200 062702 000012      ADD      #BAR,R2  ;SET UP REGADR
3101 010204 005004      CLR      R4      ;SET UP S/B DATA
3102 010206 004767 014142      JSR      PC,SUER2A ;GO SET UP ERROR INFO
3103 010212 004767 000140      JSR      PC,9$    ;GO SET UP SOME ERROR STUFF
3104 010216 104014      ERROR    14      ;BAR BIT FAILED TO CLEAR
3105 010220 000662      BR       1$      ;GO TEST NEXT LINE
3106
3107 010222 016103 000006      6$:      MOV      CAR(R1),R3 ;GET THE WAS DATA FROM CAR
3108 010226 022703 000001      CMP      #1,R3   ;DID IT GET INCREMENTED ?
3109 010232 001414      BEQ     7$      ;BR IF YES
3110
3111 010234 004767 016666      JSR      PC,SAPS   ;SAVE THE ERROR PSW
3112 010240 012704 000001      MOV      #1,R4   ;SET UP S/B DATA
3113 010244 062702 000006      ADD      #CAR,R2  ;SET UP REGADR
3114 010250 004767 014100      JSR      PC,SUER2A ;GO SET UP ERROR INFO
3115 010254 004767 000076      JSR      PC,9$    ;GO SET UP SOME ERROR STUFF
3116 010260 104014      ERROR    14      ;CAR REG NOT INCREMENTED PROPERLY
3117 010262 000641      BR       1$      ;GO TEST NEXT LINE.
3118
3119 010264 016103 000010      7$:      MOV      BCR(R1),R3 ;GET WAS DATA FROM BCR
3120 010270 001636      BEQ     1$      ;BR IF BCR GOT INCREMENTED TO 000000
3121

```



3122	010272	004767	016630		JSR	PC,SAPS	;SAVE THE ERROR PSW
3123	010276	005004			CLR	R4	;SET UP S/B DATA
3124	010300	062702	000010		ADD	#BCR,R2	;SET UP REGADR
3125	010304	004767	014344		JSR	PC,SUER2A	;GO SET UP ERROR INFO
3126	010310	004767	000042		JSR	PC,9\$	;GO SET UP SOME ERROR STUFF
3127	010314	104014			ERROR	14	;BCR REG NOT INCREMENTED PROPERLY
3128	010316	000623			BR	1\$	;GO TEST NEXT LINE
3129							
3130	010320	012711	004000	9\$:	MOV	#BIT11,(R1)	;CLEAR THE DH11
3131	010324	016703	016644		MOV	DHVCT,R3	;GET THE VECTOR ADDR
3132	010330	062703	000004		ADD	#4,R3	;POINT TO XMIT VECTOR
3133	010334	010313			MOV	R3,(R3)	;RESTORE TRAP CATCHER
3134	010336	062723	000002		ADD	#2,(R3)+	
3135	010342	005013			CLR	(R3)	
3136	010344	004767	016526		JSR	PC,CHPS1	;GO CLEAR PSW
3137	010350	012706	001100		MOV	#STACK,SP	;RESET THE STACK POINTER
3138	010354	000405			BR	TST33	;GO TO NEXT TEST
3139							
3140	010356	004567	014212	9\$:	JSR	R5,SUNUM	;GO SET UP LINE NO. IN MSG.
3141	010362	030212			LINE		
3142	010364	031344			EM14+44		
3143	010366	000207			RTS	PC	;RETURN TO REPORT ERROR

3144  
3145  
3146  
3147 010370 000004  
3148  
3149  
3150  
3151  
3152  
3153  
3154  
3155  
3156  
3157  
3158  
3159  
3160  
3161  
3162  
3163  
3164  
3165  
3166  
3167  
3168  
3169  
3170  
3171  
3172  
3173  
3174  
3175  
3176  
3177  
3178  
3179  
3180  
3181  
3182  
3183  
3184  
3185  
3186  
3187  
3188  
3189  
3190  
3191  
3192  
3193  
3194 010372 012767 010406 170510  
3195 010400 004767 014076  
3196 010404 000544  
3197 010406 052711 004000  
3198 010412 004767 014236  
3199 010416 004767 014274

```

:*****
:*TEST 33 TRANSMITTR NPR LOGIC TEST 2
:*****
TST33: SCOPE
.REM %
TEST ABSTRACT:
*****

```

THIS TEST IS SIMILAR TO TEST 32 EXCEPT THAT ALL LOCATIONS IN THE "BCR" AND "CAR" MEMORIES ARE TESTED TO VERIFY THAT TRANSMISSION ON THE SELECTED LINE DID NOT DISTURB ANY UNSELECTED LOCATIONS IN THE MEMORIES. IF ALSO OPERATES IN "FLAG" MODE RATHER THAN USING INTERRUPTS. THE TEST SEQUENCE IS AS FOLLOWS:

1. SELECT A LINE # TO TEST (AS DEFINED BY "LINSEL:")
2. CLEAR BOTH THE "CAR" AND "BCR" MEMORIES
3. LOAD THE "BCR" MEMORY WITH ALL ONES (BYTE COUNT = -1)
4. ACTIVATE THE XMITTER ON THE SELECTED LINE
5. ACTIVATE TIMER TO WAIT FOR "XMIT DONE"
6. IF "XMIT DONE" FAILS TO SET ON TIME - REPORT ERROR AND REPEAT 1 THRU 5 UNTIL ALL SELECTED LINES TESTED
7. IF "XMIT DONE" SETS CHECK ALL LOCATIONS IN THE "BCR" MEMORY REPORT ANY UNSELECTED LINES NOT CONTAINING -1 AND THE SELECTED LINE IF IT DOES NOT CONTAIN 0
8. CHECK ALL LOCATIONS IN THE "CAR" MEMORY AND REPORT ANY UNSELECTED LOCATIONS NOT CONTAINING 0 AND THE SELECTED LINE IF IT DOES NOT CONTAIN +1.
9. REPEAT STEPS 1 THRU 8 UNTIL ALL SELECTED LINES TESTED.

ERRORS:  
\*\*\*\*\*

1. [ERROR 50] CALLED IF XMIT DONE TIMEOUT ERROR DETECTED.
2. [ERROR 51] CALLED IF "BCR" MEMORY ERROR DETECTED
3. [ERROR 51] CALLED IF "CAR" MEMORY ERROR DETECTED

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. ASSUMING TEST 32 RAN ERROR FREE THE PROBLEM IS MOST LIKELY THE:  
M7278 MODULE IF "BCR" ERRORS  
M7277 MODULE IF "CAR" ERRORS

KEY LOGIC: (SAME AS TEST 32)  
\*\*\*\*\*

```

%
1$: MOV #25,$LPERR ;SET UP ERROR LOOP RETURN
JSR PC,SELINE ;GO SELECT A LINE TO TEST
BR TST34 ;BR IF DONE ALL SELECTED LINES
2$: BIS #BIT11,(R1) ;CLEAR THE DH11
JSR PC,CLCABC ;GO CLEAR "CAR" AND "BCR" MEMORIES
JSR PC,LDBCR ;GO LOAD "BCR" MEMORY WITH ALL ONES

```

# M15

MAINDEC-11-DZDHM-B  
DZDHMB.P11 T33

MACY11 27(732) 23-SEP-76 14:33 PAGE 76  
TRANSMITTR NPR LOGIC TEST 2

SEQ 0194

3200	010422	156711	017564		BISB	LINE, (R1)	;SELECT THE LINE
3201	010426	012761	033500	000004	MOV	#33500, LPR(R1)	;SET UP PARAMETERS
3202	010434	016761	016544	000012	MOV	LINMSK, BAR(R1)	;ACTIVATE XMIT ON SELECTED LINE
3203							
3204	010442	012767	000001	017570	MOV	#1, TIMEA	;INIT TIMER A
3205	010450	005067	017566		CLR	TIMEB	;INIT TIMER B
3206	010454	005711			TST	(R1)	;XMITTR DONE YET
3207	010456	100423			BMI	4\$	;BR IF YES
3208	010460	004767	016260		JSR	PC, TIMEIT	;CALL THE TIMER
3209	010464	000773			BR	3\$	;TIMER ROUTINE WILL MOVE RETURN PC ;AROUND THIS BRANCH IF TIME OUT OCCURS
3210							
3211							
3212	010466	004767	016434		JSR	PC, SAPS	;SAVE THE ERROR PSW
3213	010472	011103			MOV	(R1), R3	;GET THE WAS DATA
3214	010474	012704	100000		MOV	#BIT15, R4	;SET UP S/B DATA
3215	010500	156704	017506		BISB	LINE, R4	
3216	010504	010102			MOV	R1, R2	;MAKE REGADR = DEVADR
3217	010506	004767	013642		JSR	PC, SUER2A	;GO SET UP ERROR INFO
3218	010512	004567	014056		JSR	R5, SUNUM	;SET LINE NO. IN MSG
3219	010516	030212			LINE		
3220	010520	034144			EM50+53		
3221	010522	104050			ERROR	50	;TIMED OUT AWAITING XMIT DONE ON SEL LINE
3222	010524	000725			BR	1\$	;GO TRY THE NEXT LINE
3223							
3224	010526	005067	170466		4\$: CLR	\$TMP7	;INIT A LINE COUNTER
3225	010532	116711	170462		5\$: MOV	\$TMP7, (R1)	;SELECT LINE NO. IN "SCR"
3226	010536	012704	177777		MOV	#-1, R4	;SET UP S/B DATA
3227	010542	016103	000010		MOV	BCR(R1), R3	;GET THE WAS BYTE COUNT
3228	010546	126767	017440	170444	CMPB	LINE, \$TMP7	;WAS THIS THE ACTIVE LINE ??
3229	010554	001001			BNE	6\$	;BR IF NOT
3230	010556	005004			CLR	R4	;CHANGE S/B DATA TO 000000
3231	010560	020304			6\$: CMP	R3, R4	;WAS BYTE COUNT CORRECT ??
3232	010562	001416			BEQ	7\$	;BR IF YES
3233							
3234	010564	005067	170412		CLR	\$TMP0	;SAVE THE ACTIVE LINE NO.
3235	010570	116767	017416	170404	MOV	LINE, \$TMP0	
3236	010576	016767	170416	170400	MOV	\$TMP7, \$TMP1	;SAVE THE LINE NO. BEING CHECKED
3237	010604	010102			MOV	R1, R2	;SET UP REGADR = BCR REG ADDR
3238	010606	062702	000010		ADD	#BCR, R2	
3239	010612	004767	013620		JSR	PC, SUER4	;GO SET UP ERROR INFO
3240	010616	104051			ERROR	51	;BYTE COUNT INCORRECT
3241							
3242	010620	005004			7\$: CLR	R4	;SET UP S/B DATA
3243	010622	016103	000006		MOV	CAR(R1), R3	;GET THE WAS DATA
3244	010626	126767	017360	170364	CMPB	LINE, \$TMP7	;IS THIS THE ACTIVE LINE
3245	010634	001001			BNE	8\$	;BR IF NOT
3246	010636	005204			INC	R4	;BUMP THE CAR ADDRESS FOR ACTIVE LINE
3247	010640	020304			8\$: CMP	R3, R4	;CAR CONTENTS CORRECT ??
3248	010642	001416			BEQ	9\$	;BR IF YES
3249							
3250	010644	005067	170332		CLR	\$TMP0	;SET UP ACT LINE NO.
3251	010650	116767	017336	170324	MOV	LINE, \$TMP0	
3252	010656	016767	170336	170320	MOV	\$TMP7, \$TMP1	;SAVE THE LINE NO. BEING CHECKED
3253	010664	010102			MOV	R1, R2	;SET UP REGADR
3254	010666	062702	000006		ADD	#CAR, R2	
3255	010672	004767	013540		JSR	PC, SUER4	;SET UP THE ERROR INFO

N15

MAINDEC-11-DZDMM-B  
DZDMMB.P11 T33

MACY11 27(732) 23-SEP-76 14:33 PAGE 77  
TRANSMITTR NPR LOGIC TEST 2

SEQ 0195

3256	010676	104051			ERROR	51		:CAR REG INCORRECT
3257								
3259	010700	005267	170314	9\$:	INC	\$TMP7		:GENERATE NEW LINE NO.
3259	010704	022767	000020 170306		CMP	#20,\$*MP7		:TESTED ALL LINES
3260	010712	001307			BNE	5\$		:BR IF NOT
3261	010714	000631			BR	1\$		:GO SELECT NEXT ACTIVE LINE

010716 000004

010716 000004

\*\*\*\*\*  
\*TEST 34 TEST THAT CHARACTER AVAILABLE CAN CAUSE RCVR INTERRUPT  
\*\*\*\*\*

TEST 34: S0CFE

REM %  
TEST ABSTRACT:

\*\*\*\*\*

THIS TEST VERIFIES THAT WHEN "CHAR AVAIL" (BIT07 IN "SCR") SETS AS A RESULT OF XMITTING AND RECEIVING ONE CHARACTER (USING SILO MAINT MODE). IT CAUSES A RCVR INTR VIA THE PROPER VECTOR. THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP THE RCVR VECTOR
2. LOCK OUT INTRs, RESET SP, AND CLEAR DM11
3. USE MAINT MODE TO LOAD A CHAR INTO THE SILO (DATA=125252)
4. CLEAR PSW TO ALLOW INTERRUPTS
5. ACTIVATE TIMER TO WAIT FOR INTR TO OCCUR
6. IF NO RCVR INTR OCCURS REPORT ERROR AND GO TO STEP 9
7. WHEN RCVR INTRs - CHECK SILO DATA FOR 125252 - IF NOT CORRECT REPORT ERROR AND GO TO STEP 9
8. CHECK THAT SILO FILL LEVEL=1 - IF NOT REPORT ERROR
9. RESET SP, CLEAR PSW, RESET VECTOR, AND GO TO TEST 35

ERRORS:  
\*\*\*\*\*

1. [ERROR 13] IS CALLED TO REPORT RCVR TIMEOUT ERROR
2. [ERROR 52] IS CALLED TO REPORT SILO DATA INCORRECT
3. [ERROR 61] IS CALLED TO REPORT INCORRECT SILO FILL COUNT

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. IF NOT RCVR INTR OCCURS SUSPECT THE M7277, M7281, OR M7279 MODULES
2. IF SILO DATA OR FILL-ERRORS SUSPECT THE M7279 MODULE

KEY LOGIC:  
\*\*\*\*\*

M7279	SH1	SILO DATA MUY'S (74157'S) SSR15 H CR1	
	SH2	DATA READY L MFC 15 H SILO MEMORY LOAD SILO L 5.068 MHZ (CLOCK) SSR (13:00) H	DV1 DL1 (E13,E17,E9,E3) (3341'S) DJ2 DN1 (E20,E24)
M7289	SH6	RCV INT REQ H	DP1
M7278	SH8	SSR (03:00) H	

# C16

MAINDEC-11-DZHM-8  
DZHM8.P11 134

MAY11 27(732) 23-SEP-76 14:33 PAGE 79  
TEST THAT CHARACTER AVAILABLE CAN CAUSE RCVR INTERRUPT

SEQ 0197

SH7 SSR (07:00) 4

00100	010720	012767	010742	170162	MOV	#15,SLPERR	:SET UP THE ERROR LOOP RETURN
00101	010720	015703	015242		MOV	DHVC7,R3	:GET FIRST VECTOR ADDR
00102	010720	012723	011026		MOV	#35,(R3)+	:GO TO 35 ON RCVR INTERRUPT
00103	010720	116713	017244		MOV	CHRLVL,(R3)	
00104	010742	004767	016144		JSR	PC,CHPS2	:GO LOCK OUT INTR
00105	010742	012706	001100	15:	MOV	#STACK,SP	:RESET SP FOR ERROR LOOPS
00106	010752	012711	004000		MOV	#BIT11,(R1)	:CLEAR THE DH11
00107	010756	052761	100000	000016	BIS	#BIT15,SSR(R1)	:SET SILO MAINT. BIT TO LOAD SILO
00108	010764	012711	000100		MOV	#BIT06,(R1)	:ENABLE CHAR. AVAIL INTERRUPT
00109	010770	004767	016102		JSR	PC,CHPS1	:GO CLEAR PSW
00110	010774	012703	001000		MOV	#1000,R3	:INIT TIMER
00111	011000	005303		25:	DEC	R3	:DEC TIMER
00112	011002	001376			BNE	25	:BR IF NO TIMEOUT
00113	011004	004767	016116		JSR	PC,SAPS	:SAVE THE ERROR PSW
00114	011010	011103			MOV	(R1),R3	:GET THE WAS DATA
00115	011012	012704	020300		MOV	#300,R4	:SET UP S/B DATA
00116	011016	004767	013332		JSR	PC,SUER2A	:GO SET UP ERROR INFO
00117	011022	104013			ERROR	13	:CHAR AVAIL FAILED TO SET ON TIME
00118	011024	000436			BR	55	:ESCAPE FROM THIS TEST - CATASTROPHIC ERROR
00119	011026	016105	000016	35:	MOV	SSR(R1),R5	:SAVE THE SILO STATUS REG.
00120	011032	016103	000002		MOV	NRC(R1),R3	:GET THE WAS DATA
00121	011036	012704	125252		MOV	#125252,R4	:SET UP S/B DATA
00122	011042	020334			CMP	R3,R4	:WAS = S/B = 125252 ??
00123	011044	001410			BEG	45	:BR IF IT IS
00124	011046	004767	016054		JSR	PC,SAPS	:SAVE THE ERROR PSW
00125	011052	062702	000002		ADD	#NRC,R2	:SET UP REGADR
00126	011056	004767	013272		JSR	PC,SUER2A	:GO SET UP ERROR INFO
00127	011062	104052			ERROR	52	:DATA COMPARE ERROR
00128	011064	000416			BR	55	:GET OLT
00129	011066	010503		45:	MOV	R5,R3	:NOW GET THW SILO STATUS REG AGAIN
00130	011070	042703	140377		BIC	#140377,R5	:CLR OUT JUNK
00131	011074	012704	000400		MOV	#400,R4	:SET UP S/B DATA
00132	011100	020304			CMP	R3,R4	:SSR CHAR COUNT = 1 ??
00133	011102	001407			BEG	55	:BR IF IT IS
00134	011104	004767	016016		JSR	PC,SAPS	:SAVE THE ERROR PSW
00135	011110	062702	000016		ADD	#SSR,R2	:SET UP REGADR
00136	011114	004767	013234		JSR	PC,SUER2A	:SET UP ERROR INFO
00137	011120	104006			ERROR	6	:SSR COUNT NOT CORRECT
00138	011122	012706	001100	55:	MOV	#STACK,SP	:RESET THE STACK POINTER
00139	011126	004767	015744		JSR	PC,CHPS1	:GO CLEAR PSW
00140	011132	005011			CLR	(R1)	:RESET I.E. BIT
00141	011134	016703	016034		MOV	DHVC7,R3	:GET FIRST VECTOR ADDR
00142	011140	010313			MOV	R3,(R3)	:RESTORE TRAP CATCHER
00143	011142	062723	000002		ADD	#2,(R3)+	
00144	011146	005013			CLR	(R3)	

011152 010102  
011154 062702  
011160 012767  
011166 012711  
011172 016705  
011176 005004  
011200 052712  
011204 012703  
011210 005303  
011212 001376  
011214 042712  
011220 005204  
011222 005305

01:152 000004

\*\*\*\*\*  
:TEST 35 TEST THAT THE SILO STATUS REG COUNTS UP CORRECTLY  
\*\*\*\*\*  
TEST35: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT THE SILO FILL LEVEL COUNTS UP CORRECTLY  
WHEN ALL COUNTS (0-77) ARE TESTED BY LOADING THE SILO USING  
MAINT MODE. THE TEST SEQUENCE IS AS FOLLOWS:

1. INIT "STMP7" TO START WITH A COUNT=01
2. CLEAR THE DH11
3. LOAD THE SILO WITH 125252'S IN MAINT MODE  
UNTIL # OF WORDS INDICATED BY THE COUNT ARE LOADED
4. AFTER LOADING REQUIRED COUNT CHECK THAT FILL LEVEL  
BITS (SSR<13:08>) EQUAL COUNT - IF NOT REPORT ERROR
5. INCREMENT COUNT IN "STMP7" AND REPEAT 1 THRU 4  
UNTIL ALL COUNTS (01-77) HAVE BEEN TESTED

ERRORS:  
\*\*\*\*\*

1. [ERROR 6] IS CALLED TO REPORT SILO FILL LEVEL ERRORS

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. FAILURES IN THIS TEST MOST LIKELY INDICATE A BAC M7279 MODULE

KEY LOGIC:  
\*\*\*\*\*

M7279 SH2 SSR <13:08>  
LOAD SILO L DJ2  
5.068 MHZ (CLOCK) DN1  
DATA READY L DVI

```

%      MOV      R1,R2      :MAKE REGADR = SSR
      ADD      #SSR,R2
      MOV      #1,STMP7    :START WITH COUNT OF 1
1$:    MOV      #BIT11,(R1) :CLEAR THE DH11
      MOV      STMP7,R5    :SAVE CHARACTER COUNT BEING TESTED
      CLR      R4          :INIT A CHAR COUNTER
2$:    BVS     #BIT15,(R2) :SET THE SILO MAINT BIT
      MOV      #1000,R3    :INIT A TIMER
3$:    DEC     R3          :STALL TO ALLOW TIME TO LOAD SILO
      BNE     3$
      BIC     #BIT15,(R2) :CLEAR SILO MAINT. BIT
      INC     R4          :COUNT A CHAR LOADED
      DEC     R5          :DECREMENT TEST COUNT

```

# E16

MAINDEC-11-DZDMM-B  
DZDMMB.P11 T35

MACY11 27(732) 23-SEP-76 14:33 PAGE 91  
TEST THAT THE SILO STATUS REG COUNTS UP CORRECTLY

SEQ 0199

3430	011224	J01365				BNE	25		:BR UNTIL WE'VE LOADED THE TEST COUNT
3431						MOV	(R2),R3		:SET THE WAS COUNT
3432	011226	011203				BIC	#140377,R3		:CLR JUNK BITS
3433	011230	042703	140377			SWAB	R4		:SET UP S/B DATA
3434	011234	000304				CMP	R3,R4		:TEST COUNT = SILO COUNTER ?
3435	011236	020304				SEQ	45		:BR IF YES
3436	011240	001406							
3437						FC, SUER2			:GO SET UP ERROR INFO
3438	011242	004767	013102		JSR	MOV	#15,SLPERR		:SET UP ERROR LOOP RETURN
3439	011246	012767	011166	167634		ERROR	6		:SSR FAILED TO UP-COUNT CORRECTLY
3440	011254	104006							
3441						INC	\$TMP7		:INCREMENT TO NEXT COUNT TO TEST
3442	011256	005267	167736		45:	CMP	#100,\$TMP7		:MAXIMUM COUNT ??
3443	011260	022767	000100	167730		BNE	15		:BR IF NOT
3444	011270	001336							



3446  
3447  
3448  
3449 011272 000034  
3450  
3451  
3452  
3453  
3454  
3455  
3456  
3457  
3458  
3459  
3460  
3461  
3462  
3463  
3464  
3465  
3466  
3467  
3468  
3469  
3470  
3471  
3472  
3473  
3474  
3475  
3476  
3477  
3478  
3479  
3480 011274 010102  
3481 011276 062702 000016  
3482 011302 012767 000001 167710  
3483 011310 012711 004000  
3484 011314 012705 000100  
3485 011320 166705 167674  
3486 011324 012703 000100  
3487 011330 012704 001000  
3488 011334 052712 100000  
3489 011340 005304  
3490 011342 001376  
3491 011344 042712 100000  
3492 011350 005303  
3493 011352 001366  
3494  
3495 011354 016703 167640  
3496 011360 012704 001000  
3497 011364 005761 000002  
3498 011370 005304  
3499 011372 001376  
3500 011374 005303  
3501 011376 001370

\*\*\*\*\*  
:TEST 36 TEST THAT SILO STATUS REGISTER DOWN COUNTS CORRECTLY  
\*\*\*\*\*  
†ST36: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT THE SILO FILL LEVEL COUNTS DOWN PROPERLY  
WHEN WORDS ARE READ FROM THE SILO. ALL COUNTS FROM 77-00 ARE  
TESTED. THE TEST SEQUENCE IS AS FOLLOWS:

- 1. INIT "\$TMP7" TO START WITH A COUNT OF 1
- 2. CLEAR THE DH11 AND FILL SILO WITH 64. WORDS
- 3. READ THE NO. OF WORDS SPECIFIED BY COUNT
- 4. CHECK THAT FILL LEVEL=64. MINUS [COUNT] - REPORT ERRORS
- 5. INCREMENT "\$TMP7" AND REPEAT 2 THRU 4 UNTIL ALL COUNTS TESTED.

ERRORS:  
\*\*\*\*\*

1. [ERROR 6] IS CALLED TO REPORT SILO FILL LEVEL ERRORS

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG: (REFER TO TEST 35)  
\*\*\*\*\*

KEY LOGIC: (REFER TO TEST 35)  
\*\*\*\*\*

%  
MOV R1,R2 ;SET UP REGADR  
ADD #SSR,R2  
MOV #1,\$TMP7 ;START WITH COUNT = 1  
1\$: MOV #BIT11,(R1) ;CLR THE DH11  
MOV #100,R5 ;TEST COUNT SHOULD BE 64(10) MINUS  
SUB \$TMP7,R5 ;THE NO. OF CHARS READ  
MOV #100,R3 ;COUNTER USED TO FILL SILO  
2\$: MOV #1000,R4 ;INIT TIMER  
BIS #BIT15,(R2) ;SET SILO MAINT. BIT  
3\$: DEC R4 ;STALL TO ALLOW SILO TO LOAD  
BNE 3\$  
BIC #BIT15,(R2) ;CLEAR THE SILO MAINT BIT  
DEC R3 ;COUNT ONE CHAR LOADED  
BNE 2\$ ;BR UNTIL ALL LOADED  
MOV \$TMP7,R3 ;INIT COUNTER FOR READING SILO  
4\$: MOV #1000,R4 ;INIT TIMER  
TST NRC(R1) ;READ THE SILO  
5\$: DEC R4 ;GIVE IT TIME TO SETTLE  
BNE 5\$  
DEC R3 ;COUNT ONE READ  
BNE 4\$ ;BR UNTIL WE'VE READ TEST COUNT



# H16

MAINDEC-11-DZDHM-B  
DZDHMB.F11 T37

MACY11 27(732) 23-SEP-76 14:33 PAGE 84  
TEST SILO ALARM LEVEL FOR COUNTS 0,1,2,4,8,16, AND 32

SEQ 0202

011446 000004  
011447  
011448  
011449  
011450  
011451  
011452  
011453  
011454  
011455  
011456  
011457  
011458  
011459  
011460  
011461  
011462  
011463  
011464  
011465  
011466  
011467  
011468  
011469  
011470  
011471  
011472  
011473  
011474  
011500

```
*****  
: TEST 37 TEST SILO ALARM LEVEL FOR COUNTS 0,1,2,4,8,16, AND 32  
*****  
†ST37: SCOPE  
REM %  
TEST ABSTRACT:  
*****
```

THIS TEST VERIFIES THAT THE SILO ALARM LEVEL WORKS PROPERLY FOR INTEGRAL POWER OF 2 COUNTS (0, 1, 2, 4, 8, 16, AND 32). THE TEST SEQUENCE IS AS FOLLOWS:

1. INIT "\$TMP7" TO START WITH ALARM LEVEL OF 000
2. CLEAR THE DH11 AND LOAD THEN SILO WITH THAT NO. OF WORDS THAT IS ONE GREATER THAN THE ALARM LEVEL.
3. VERIFY THAT "DATA READY" DOES NOT SET UNTIL THE FILL LEVEL EXCEEDS THE ALARM LEVEL.
4. REPORT ERRORS IF:
  - A. "READY" SETS TOO SOON
  - B. "READY" SETS TOO LATE
5. SHIFT "\$TMP7" LEFT TO GENERATE NEXT POWER OF 2 LEVEL
6. REPEAT 2 THRU 5 UNTIL ALL 7 TEST LEVELS CHECKED

NOTE: FOR (A) ABOVE IF "READY" SETS JUST ONE WORK TOO SOON IT IS ALLOWED BY ANYTHING GREATER RESULTS IN AN ERROR MESSAGE.

ERRORS:  
\*\*\*\*\*

1. [ERROR 6] IS CALLED TO REPORT BOTH TYPES OF ERRORS OUTLINED IN 4(A,B) ABOVE

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. ERRORS IN THIS TEST ONLY INDICATE BAD COMPARATOR CHIP (E23 OR E19) ON THE M7279 - SH2

KEY LOGIC:  
\*\*\*\*\*

M7279 SH2 E19 - PIN 5 (COMPARATOR)  
ALSO SAME LOGIC AS TEST 35

```
%
MOV #15,$LPERR ;SET UP THE ERROR LOOP RETURN
MOV R1,R2 ;SET UP REGADR
ADD #SSR,R2
CLR $TMP7 ;START WITH LEVEL 00
1$: MOV #BIT11,(R1) ;CLEAR THE DH11
MOV $TMP7,R5 ;SAVE IT IN R5
MOV R5,(R2) ;SET ALARM LEVEL IN SSR
```

```
011450 012767 011470 167432
011456 010102
011460 062702 000016
011464 005067 167530
011470 012711 004000
011474 016705 167520
011500 010512
```

3575	011502	005205			INC	R5		:LOAD ONE MORE THAN FILL LEVEL
3576	011504	052712	100000	2\$:	BIS	#BIT15,(R2)		:SET SILO MAINT. TO LOAD A CHAR
3577	011510	012703	001000		MOV	#1000,R3		:INIT STALL TIMER
3578	011514	005303		3\$:	DEC	R3		:WAIT FOR SILO TO SETTLE
3579	011516	001376			BNE	3\$		:BR TIL R3 GOES TO 000000
3580	011520	042712	100000		BIC	#BIT15,(R2)		:CLR THE SILO MAINT BIT
3581	011524	005305			DEC	R5		:COUNT ONE LOADED
3582	011526	105711			TSTB	(R1)		:CHAR AVAIL SET YET
3583	011530	100412			BMI	4\$		:BR IF IT IS
3584	011532	005705			TST	R5		:SHOULD IT BE ??
3585	011534	001363			BNE	2\$		:BR IF NOT
3586								
3587	011536	004767	015364		JSR	PC,SAPS		:SAVE THE ERROR PSW
3588	011542	004767	000042		JSR	PC,5\$		:GO SET UP S/B DATA
3589	011546	004767	012602		JSR	PC,SUER2A		:GO SET UP ERROR INFO
3590	011552	104006			ERROR	6		:SILO ALARM LEVEL FAILED AT SELECTED COUNT
3591	011554	000426			BR	6\$		:GO CHECK NEXT COUNT
3592								
3593	011556	005705		4\$:	TST	R5		:SHOULD IT HAVE BEEN SET (CHAR AVAIL)
3594	011560	001424			BEQ	6\$		:BR IF YES
3595								
3596	011562	004767	015340		JSR	PC,SAPS		:SAVE THE ERROR PSW
3597	011566	022705	000001		CMP	#1,R5		:IS IT OFF BY ONLY ONE ??
3598	011572	001417			BEQ	6\$		:BR IF YES - WE'LL ALLOW HIM THIS
3599	011574	004767	000010		JSR	PC,5\$		:GO SET UP S/B DATA
3600	011600	004767	012550		JSR	PC,SUER2A		:GO SET UP ERROR INFO
3601	011604	104006			ERROR	6		:SILO ALARM LEVEL FAILED
3602	011606	000411			BR	6\$		:GO CHECK NEXT COUNT
3603								
3604	011610	011203		5\$:	MOV	(R2),R3		:GET WAS DATA
3605	011612	016704	167402		MOV	\$TMP7,R4		:SET UP THE S/B DATA
3606	011616	005204			INC	R4		
3607	011620	000304			SWAB	R4		
3608	011622	105004			CLRB	R4		
3609	011624	156704	167370		BISB	\$TMP7,R4		
3610	011630	000207			RTS	PC		:RETRN TO SET UP AND REPORT ERROR
3611								
3612	011632	005767	167362	6\$:	TST	\$TMP7		:COUNT AT ZERO
3613	011636	001002			BNE	7\$		:BR IF NOT
3614	011640	000261			SEC			:SET THE "C" BIT
3615	011642	000401			BR	8\$		:GO SET UP COUNT
3616	011644	000241		7\$:	CLC			:CLEAR THE "C" BIT
3617	011646	006167	167346	8\$:	ROL	\$TMP7		:SHIFT-POWER OF TWO BIT
3618	011652	032767	000100 167340		BIT	#BIT6,\$TMP7		:DONE ALL POWERS ??
3619	011650	001703			BEQ	1\$		:BR IF NOT

3620  
3621  
3622  
3623 011662 000004  
3624  
3625  
3626  
3627  
3628  
3629  
3630  
3631  
3632  
3633  
3634  
3635  
3636  
3637  
3638  
3639  
3640  
3641  
3642  
3643  
3644  
3645  
3646  
3647  
3648  
3649  
3650  
3651  
3652  
3653  
3654  
3655  
3656  
3657  
3658  
3659  
3660  
3661  
3662  
3663  
3664  
3665  
3666  
3667  
3668  
3669  
3670  
3671  
3672  
3673  
3674  
3675

```
::*****  
:*TEST 40 TRANSMITTER TIMING TEST - ALL SELECTED LINES - ALL SPEEDS  
:*****  
TST40: SCOPE  
.REM %  
TEST ABSTRACT:  
*****
```

THIS TEST PERFORMA A "RELATIVE" TIMING TEST FOR ALL BAUD RATES ON ALL SELECTED LINES. IT DOES NOT MEASURE ABSOLUTE TIMES BUT SIMPLY VERIFIES THAT EACH SUCCESSIVE SPEED FROM 50 TO 9600 BAUD IS FASTER THAN THE PREVIOUS SPEED. THE TEST SEQUENCE IS AS FOLLOWS:

1. SELECT A LINE # TO TEST (AS DEFINED BY "LINSEL:");
2. INIT "\$TMP7" TO START WITH 50 BAUD AND A RELATIVE TIMER "TIMEC" TO -1 (177777)
3. CLEAR THE DH11 AND ACTIVATE SELECTED LINE TO TRANSMIT THREE CHARS.
4. ACTIVATE TIMER TO UPDATE "TIMEB" THE LINE SPEED TIMER
5. IF "XMIT DONE" FAILS TO SET ON TIME - REPORT ERROR AND REPEAT 3 THRU 4 UNTIL ALL SPEEDS CHECKED - THEN REPEAT 1 THRU 5 UNTIL ALL LINES CHECKED
6. IF "XMIT DONE" SETS VERIFY [TIMEB] LESS THAN [TIMEC] IF NOT REPORT ERROR - MAKE [TIMEC]=[TIMEB] AND REPEAT 3 THRU 5 UNTIL ALL SPEEDS CHECKED
7. REPEAT 1 THRU 6 FOR ALL SELECTED LINES.

ERRORS:  
\*\*\*\*\*

1. [ERROR 53] IS CALLED TO REPORT XMIT TIMEOUT ERRORS
2. [ERROR 17] IS CALLED TO REPORT TIMING ERRORS

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. IF ALL LINES FAIL ON ALL SPEEDS SUSPECT THE CLOCK MODULE M4540
2. IF ALL LINES FAIL ON JUST ONE SPEED (THE SAME ONE) SUPECT EITHER THE CLOCK MODULE OR THE M7288 MODULE (TIMING SELECT MUXES)
3. IF JUST ONE LINE FAILS SUSPECT EITHER THE UART MODULE (M7280) EITHER FOR LINES <15:08> OR <07:00> OR THE M7298 MODULE

KEY LOGIC:  
\*\*\*\*\*

M4540 SH2 <9600:50> BAUD SIGNALS  
M7288 SH3 BOT AND TOP BUF CLOCK SIGNALS  
SH4,6,8,OR 10 TX CLOCK NN L SIGNALS  
M7280 TBM LINE "N" SIGNALS ON UART PIN 22  
TX CLOCK LINE "N" SIGNALS ON UART PIN 40

# K16

MAINDEC-11-DZDHM-8  
DZDHMB.P11 T40

MACY11 27(732) 23-SEP-76 14:33 PAGE 87  
TRANSMITTER TIMING TEST - ALL SELECTED LINES - ALL SPEEDS

SEQ 0205

3676	011664	012767	011714	167216		MOV	#2\$, \$LPERR	:SET UP ERROR LOOP RETURN
3677	011672	004767	012604		1\$:	JSR	PC, SELINE	:GO SELECT A LINE TO TEST
3678	011676	000534				BR	TST41	:BR IF TESTED ALL SELECTED LINES
3679	011700	012767	002100	167312		MOV	#2100, \$TMP7	:INIT TI START WITH LO. EST SPEED
3680	011706	012767	177777	016330		MOV	#-1, TIMEC	:INIT RELATIVE TIME CHECKER
3681	011714	012711	004000		2\$:	MOV	#BIT11, (R1)	:CLEAR THE DH11
3682	011720	156711	016266		3\$:	BISB	LINE, (R1)	:SELECT IT IN THE SCR
3683	011724	012761	177775	000010		MOV	#-3, BCR(R1)	:SET BYTE COUNT TO XFER 3 CHARS
3684	011732	005061	000006			CLR	CAR(R1)	:GET TEST DATA STARTING AT LOC. 0
3685	011736	016761	167256	000004		MOV	\$TMP7, LPR(R1)	:SELECT A XMIT SPEED
3686	011744	016761	015234	000012		MOV	LINMSK, BAR(R1)	:ACTIVATE THE TRANSMITTER
3687								
3688	011752	012767	000001	016260		MOV	#1, TIMEA	:INIT TIMER A
3689	011760	005067	016256			CLR	TIMEB	:INIT TIMER B
3690	011764	005711			4\$:	TST	(R1)	:XMITR DONE SET YET ?
3691	011766	100437				BMI	\$S	:BR IF YES
3692	011770	004767	014750			JSR	PC, TIMEIT	:CALL THE TIMER
3693	011774	000773				BR	4\$	:TIMER ROUTINE WILL MOVE RETURN PC
3694								:AROUND THIS BRANCH IF TIME OUT OCCURS
3695								
3696	011776	016767	167216	167176		MOV	\$TMP7, \$TMP0	:SAVE AND SET UP THE SPEED CODE
3697	012004	000367	167172			SWAB	\$TMP0	
3698	012010	006267	167166			ASR	\$TMP0	
3699	012014	006267	167162			ASR	\$TMP0	
3700	012020	042767	177760	167154		BIC	#177760, \$TMP0	
3701	012026	011103				MOV	(R1), R3	:GET THE WAS DATA
3702	012030	042703	000200			BIC	#BIT07, R3	:CLEAR UNINTERESTING BITS
3703	012034	010102				MOV	R1, R2	:MAKE REGADR = DEVADR
3704	012036	012704	100000			MOV	#BIT15, R4	:SET UP S/B DATA
3705	012042	156704	016144			BISB	LINE, R4	
3706	012046	004767	012302			JSR	PC, SUER2A	:GO SET UP ERROR INFO
3707	012052	004567	012516			JSR	R5, SUNUM	:GO SET LINE NO. IN MSG
3708	012056	030212				LINE		
3709	012060	034144				EM50+53		
3710	012062	104053				ERROR	53	:TIMED OUT WAITING FOR XMIT DONE
3711	012064	000426				BR	8\$	:GO TEST NEXT SPEED
3712								
3713	012066	016703	016150		5\$:	MOV	TIMEB, R3	:GET THE WAS COUNT
3714	012072	016704	016146			MOV	TIMEC, R4	:GET LASTR CHECK COUNT
3715	012076	020304				CMP	R3, R4	:COMPARE RELATIVE TIMES
3716	012100	103420				BLO	8\$	:BR IF THIS SPEED FASTER THAN LAST
3717								:SPEED TESTED
3718								
3719	012102	004767	015020		7\$:	JSR	PC, SAPS	:SAVE THE ERROR PSW
3720	012106	016702	167106			MOV	\$TMP7, R2	:GET SPEED CODE AND RIGHT JUSTIFY
3721	012112	000302				SWAB	F.2	
3722	012114	006202				ASR	R2	
3723	012116	006202				ASR	R2	
3724	012120	042702	177760			BIC	#177760, R2	:STRIP AWAY ALL JUNK
3725	012124	004767	012224			JSR	PC, SUER2A	:GO SET UP ERROR INFO
3726	012130	004567	012440			JSR	R5, SUNUM	:GO PUT LINE NO. IN MSG
3727	012134	030212				LINE		
3728	012136	031507				EM17+41		
3729	012140	104017				ERROR	17	:TRANSMITTER SPEED INCORRECT
3730								
3731	012142	016767	016074	016074	8\$:	MOV	TIMEB, TIMEC	:SET UP NEW CHECK TIMER COUNT

L16

MAINDEC-11-DZDMM-B  
DZDMMB.P11 T40

MACY11 27(732) 23-SEP-76 14:33 PAGE 89  
TRANSMITTER TIMING TEST - ALL SELECTED LINES - ALL SPEEDS

SEQ 0206

3732	012150	062767	002100	167042	ADD	#2100.\$TMP7	:GENERATE NEXT SPEED
3733	012156	022767	035600	167034	CMP	#35600.\$TMP7	:DONE ALL SPEEDS ?
3734	012164	001253			BNE	2\$	:BR IF NOT
3735	012166	000641			BR	1\$	:GO TEST NEXT LINE
3736							

M16

MAINDEC-11-DZDHM-B  
DZDHMB.P11 T41

MACY11 27(732) 23-SEP-76 14:33 PAGE 89  
RECEIVER TIMING TEST - ALL SELECTED LINES - ALL SPEEDS

SEQ 0207

3737  
3738  
3739  
3740 012170 000004  
3741  
3742  
3743  
3744  
3745  
3746  
3747  
3748  
3749  
3750  
3751  
3752  
3753  
3754  
3755  
3756  
3757  
3758  
3759  
3760  
3761  
3762  
3763  
3764  
3765  
3766  
3767  
3768  
3769 012172 012767 012222 166710  
3770 012200 004767 012276  
3771 012204 000532  
3772 012206 012767 002100 167004  
3773 012214 012767 177777 016022  
3774 012222 012711 004000  
3775 012226 156711 015750  
3776 012232 012761 177777 000010  
3777 012240 005061 000036  
3778 012244 016761 166750 000004  
3779 012252 016761 014726 000012  
3780  
3781 012260 012767 000001 015752  
3782 012266 005067 015750  
3783 012272 105711  
3784 012274 100435  
3785 012276 004767 014442  
3786 012302 000773  
3787  
3788  
3789 012304 016767 166710 166670  
3790 012312 006367 166664  
3791 012316 006367 166660  
3792 012322 000367 166654

::\*\*\*\*\*  
;\*TEST 41 RECEIVER TIMING TEST - ALL SELECTED LINES - ALL SPEEDS  
:\*\*\*\*\*  
TST41: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST ID IDENTICAL TO TEST 42 EXCEPT IT WAITS FOR "DATA READ"  
TO CHECK RECEIVER TIMING. THE SEQUENCE IS SIMILAR AND THE SAME TIMERS  
ARE USED FOR ERROR CHECKING.

ERRORS:  
\*\*\*\*\*

- 1. [ERROR 54] IS CALLED TO REPORT RCVR TIMEOUT ERRORS
- 2. [ERROR 20] IS CALLED TO REPORT RCVR TIMING ERRORS

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBJG: (SAME AS TEST 42)  
\*\*\*\*\*

KEY LOGIC: (SAME AS TEST 42 PLUS)  
\*\*\*\*\*

M7288 SH5,7,9,11 RX CLOCK NN L SIGNALS  
M7280 BUF DA LINE "N" UART PIN 19  
RX CLOCK LINE "N" UART PIN 17

%  
1\$: MOV #25,\$LPERR ;SET UP ERROR LOOP RETURN  
JSR PC,SELIN ;GO SELECT A LINE TO TEST  
BR TST42 ;BR IF TESTED ALL SELECTED LINES  
MOV #2100,\$TMP7 ;INIT TO START WITH LOWEST SPEED  
MOV #-1,\$TIMEC ;INIT RELATIVE TIME CHECKER  
2\$: MOV #BIT11,(R1) ;CLEAR THE DH11  
3\$: ETSB LINE,(R1) ;SELECT IT IN THE SCR  
MOV #-1,\$BCR(R1) ;SET BYTE COUNT TO XFER 1 CHAR  
CLR CAR(R1) ;GET TEST DATA STARTING AT LOC. 0  
MOV \$TMP7,\$LPR(R1) ;SELECT A XMIT SPEED  
MOV LINMSK,\$BAR(R1) ;ACTIVATE THE TRANSMITTER  
4\$: MOV #1,\$TIMEA ;INIT TIMER A  
CLR \$TIMEB ;INIT TIMER B  
TSTB (R1) ;RCVR DONE YET ??  
BMI \$5 ;BR IF YES  
JSR PC,\$TIMEIT ;CALL THE TIMER  
BR \$4 ;TIMER ROUTINE WILL MOVE RETURN PC  
;AROUND THIS BRANCH IF TIME OUT OCCURS  
MOV \$TMP7,\$TMP0 ;SAVE AND SET UP THE SPEED CODE  
ASL \$TMP0  
ASL \$TMP0  
SWAB \$TMP0





CO1

MAINCOC-11-DZDMM-B  
DZDMMB.F11 T41

MACY11 27(732) 23-SEP-76 14:33 PAGE 91  
RECEIVER TIMING TEST - ALL SELECTED LINES - ALL SPEEDS

SEP 22 09

3829

AS

012472 000004  
012473 000005  
012474 000006  
012475 000007  
012476 000008  
012477 000009  
012478 000010  
012479 000011  
012480 000012  
012481 000013  
012482 000014  
012483 000015  
012484 000016  
012485 000017  
012486 000018  
012487 000019  
012488 000020  
012489 000021  
012490 000022  
012491 000023  
012492 000024  
012493 000025  
012494 000026  
012495 000027  
012496 000028  
012497 000029  
012498 000030  
012499 000031  
012500 000032  
012501 000033  
012502 000034  
012503 000035  
012504 000036  
012505 000037  
012506 000038  
012507 000039  
012508 000040  
012509 000041  
012510 000042  
012511 000043  
012512 000044  
012513 000045  
012514 000046  
012515 000047  
012516 000048  
012517 000049  
012518 000050  
012519 000051  
012520 000052  
012521 000053  
012522 000054  
012523 000055  
012524 000056  
012525 000057  
012526 000058  
012527 000059  
012528 000060  
012529 000061  
012530 000062  
012531 000063  
012532 000064  
012533 000065  
012534 000066  
012535 000067  
012536 000068  
012537 000069  
012538 000070  
012539 000071  
012540 000072  
012541 000073  
012542 000074  
012543 000075  
012544 000076  
012545 000077  
012546 000078  
012547 000079  
012548 000080  
012549 000081  
012550 000082  
012551 000083  
012552 000084  
012553 000085  
012554 000086  
012555 000087  
012556 000088  
012557 000089  
012558 000090  
012559 000091  
012560 000092  
012561 000093  
012562 000094  
012563 000095  
012564 000096  
012565 000097  
012566 000098  
012567 000099  
012568 000100  
012569 000101  
012570 000102  
012571 000103  
012572 000104  
012573 000105  
012574 000106  
012575 000107  
012576 000108  
012577 000109  
012578 000110  
012579 000111  
012580 000112  
012581 000113  
012582 000114  
012583 000115  
012584 000116  
012585 000117  
012586 000118  
012587 000119  
012588 000120  
012589 000121  
012590 000122  
012591 000123  
012592 000124  
012593 000125  
012594 000126  
012595 000127  
012596 000128  
012597 000129  
012598 000130  
012599 000131  
012600 000132  
012601 000133  
012602 000134  
012603 000135  
012604 000136  
012605 000137  
012606 000138  
012607 000139  
012608 000140  
012609 000141  
012610 000142  
012611 000143  
012612 000144  
012613 000145  
012614 000146  
012615 000147  
012616 000148  
012617 000149  
012618 000150  
012619 000151  
012620 000152  
012621 000153  
012622 000154  
012623 000155  
012624 000156  
012625 000157  
012626 000158  
012627 000159  
012628 000160  
012629 000161  
012630 000162  
012631 000163  
012632 000164  
012633 000165  
012634 000166  
012635 000167  
012636 000168  
012637 000169  
012638 000170  
012639 000171  
012640 000172  
012641 000173  
012642 000174  
012643 000175  
012644 000176  
012645 000177  
012646 000178  
012647 000179  
012648 000180  
012649 000181  
012650 000182  
012651 000183  
012652 000184  
012653 000185  
012654 000186  
012655 000187  
012656 000188  
012657 000189  
012658 000190  
012659 000191  
012660 000192  
012661 000193  
012662 000194  
012663 000195  
012664 000196  
012665 000197  
012666 000198  
012667 000199  
012668 000200  
012669 000201  
012670 000202  
012671 000203  
012672 000204  
012673 000205  
012674 000206  
012675 000207  
012676 000208  
012677 000209  
012678 000210  
012679 000211  
012680 000212  
012681 000213  
012682 000214  
012683 000215  
012684 000216  
012685 000217  
012686 000218  
012687 000219  
012688 000220  
012689 000221  
012690 000222  
012691 000223  
012692 000224  
012693 000225  
012694 000226  
012695 000227  
012696 000228  
012697 000229  
012698 000230  
012699 000231  
012700 000232  
012701 000233  
012702 000234  
012703 000235  
012704 000236  
012705 000237  
012706 000238  
012707 000239  
012708 000240  
012709 000241  
012710 000242  
012711 000243  
012712 000244  
012713 000245  
012714 000246  
012715 000247  
012716 000248  
012717 000249  
012718 000250  
012719 000251  
012720 000252  
012721 000253  
012722 000254  
012723 000255  
012724 000256  
012725 000257  
012726 000258  
012727 000259  
012728 000260  
012729 000261  
012730 000262  
012731 000263  
012732 000264  
012733 000265  
012734 000266  
012735 000267  
012736 000268  
012737 000269  
012738 000270  
012739 000271  
012740 000272  
012741 000273  
012742 000274  
012743 000275  
012744 000276  
012745 000277  
012746 000278  
012747 000279  
012748 000280  
012749 000281  
012750 000282  
012751 000283  
012752 000284  
012753 000285  
012754 000286  
012755 000287  
012756 000288  
012757 000289  
012758 000290  
012759 000291  
012760 000292  
012761 000293  
012762 000294  
012763 000295  
012764 000296  
012765 000297  
012766 000298  
012767 000299  
012768 000300  
012769 000301  
012770 000302  
012771 000303  
012772 000304  
012773 000305  
012774 000306  
012775 000307  
012776 000308  
012777 000309  
012778 000310  
012779 000311  
012780 000312  
012781 000313  
012782 000314  
012783 000315  
012784 000316  
012785 000317  
012786 000318  
012787 000319  
012788 000320  
012789 000321  
012790 000322  
012791 000323  
012792 000324  
012793 000325  
012794 000326  
012795 000327  
012796 000328  
012797 000329  
012798 000330  
012799 000331  
012800 000332  
012801 000333  
012802 000334  
012803 000335  
012804 000336  
012805 000337  
012806 000338  
012807 000339  
012808 000340  
012809 000341  
012810 000342  
012811 000343  
012812 000344  
012813 000345  
012814 000346  
012815 000347  
012816 000348  
012817 000349  
012818 000350  
012819 000351  
012820 000352  
012821 000353  
012822 000354  
012823 000355  
012824 000356  
012825 000357  
012826 000358  
012827 000359  
012828 000360  
012829 000361  
012830 000362  
012831 000363  
012832 000364  
012833 000365  
012834 000366  
012835 000367  
012836 000368  
012837 000369  
012838 000370  
012839 000371  
012840 000372  
012841 000373  
012842 000374  
012843 000375  
012844 000376  
012845 000377  
012846 000378  
012847 000379  
012848 000380  
012849 000381  
012850 000382  
012851 000383  
012852 000384  
012853 000385  
012854 000386  
012855 000387  
012856 000388  
012857 000389  
012858 000390  
012859 000391  
012860 000392  
012861 000393  
012862 000394  
012863 000395  
012864 000396  
012865 000397  
012866 000398  
012867 000399  
012868 000400  
012869 000401  
012870 000402  
012871 000403  
012872 000404  
012873 000405  
012874 000406  
012875 000407  
012876 000408  
012877 000409  
012878 000410  
012879 000411  
012880 000412  
012881 000413  
012882 000414  
012883 000415  
012884 000416  
012885 000417  
012886 000418  
012887 000419  
012888 000420  
012889 000421  
012890 000422  
012891 000423  
012892 000424  
012893 000425  
012894 000426  
012895 000427  
012896 000428  
012897 000429  
012898 000430  
012899 000431  
012900 000432  
012901 000433  
012902 000434  
012903 000435  
012904 000436  
012905 000437  
012906 000438  
012907 000439  
012908 000440  
012909 000441  
012910 000442  
012911 000443  
012912 000444  
012913 000445  
012914 000446  
012915 000447  
012916 000448  
012917 000449  
012918 000450  
012919 000451  
012920 000452  
012921 000453  
012922 000454  
012923 000455  
012924 000456  
012925 000457  
012926 000458  
012927 000459  
012928 000460  
012929 000461  
012930 000462  
012931 000463  
012932 000464  
012933 000465  
012934 000466  
012935 000467  
012936 000468  
012937 000469  
012938 000470  
012939 000471  
012940 000472  
012941 000473  
012942 000474  
012943 000475  
012944 000476  
012945 000477  
012946 000478  
012947 000479  
012948 000480  
012949 000481  
012950 000482  
012951 000483  
012952 000484  
012953 000485  
012954 000486  
012955 000487  
012956 000488  
012957 000489  
012958 000490  
012959 000491  
012960 000492  
012961 000493  
012962 000494  
012963 000495  
012964 000496  
012965 000497  
012966 000498  
012967 000499  
012968 000500  
012969 000501  
012970 000502  
012971 000503  
012972 000504  
012973 000505  
012974 000506  
012975 000507  
012976 000508  
012977 000509  
012978 000510  
012979 000511  
012980 000512  
012981 000513  
012982 000514  
012983 000515  
012984 000516  
012985 000517  
012986 000518  
012987 000519  
012988 000520  
012989 000521  
012990 000522  
012991 000523  
012992 000524  
012993 000525  
012994 000526  
012995 000527  
012996 000528  
012997 000529  
012998 000530  
012999 000531  
013000 000532

012472 000004

\*\*\*\*\*  
: \*TEST 42 VERIFY STORAGE OVERFLOW - NON MAINT. MODE - ALL SELECTED LINES  
: \*\*\*\*\*  
TST42: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT THE STORAGE OVERFLOW BIT (SCR14) SETS AND CLEARS PROPERLY FOR ALL SELECTED LINES. THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP THE ERROR RETURN
2. SELECT A LINE NUMBER TO TEST - GO TO NEXT TEST IF ALL SELECTED LINES HAVE BEEN TESTED.
3. PRIME THE SELECTED LINE TO XMIT 65(10) CHARS.
4. ACTIVATE THE SELECTED LINE AND WAIT FOR STORAGE OVERFLOW TO SET (SCR14=1)
5. IF SCR14 FAILS TO SET ON TIME - REPORT ERROR AND THEN CONTINUE WITH THE NEXT LINE (STEP 2).
6. IF IT SETS OK - READ THE "NRC" REG TWICE TO EMPTY TWO WORDS FROM THE SILO.
7. AFTER A BRIEF STALL, VERIFY THAT SCR14 HAS CLEARED - IF NOT REPORT ERROR AND CONTINUE WITH NEXT LINE (STEP 2)
8. IF IT CLEARS OK, VERIFY THAT THE FILL COUNT (SSR:15:08) CONTAINS A 77(8) - IF NOT REPORT ERROR AND CONTINUE WITH NEXT LINE (STEP 2).
9. REPEAT STEPS 2 THRU 8 UNTIL ALL SELECTED LINES HAVE BEEN TESTED.

ERRORS:  
\*\*\*\*\*

1. (ERROR 57) IS CALLED TO REPORT ALL ERRORS DETECTED.

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. PROBLEM IS MOST LIKELY ON THE M7289 MODULE (SH4) OR SOME SIGNAL FEEDING THIS LOGIC.

KEY LOGIC:  
\*\*\*\*\*

M7289	SH4	STORAGE OVERFLOW L	E43-12
		READY IN PULSE H	E40-11
		UC1 MASTER DA H	BH2
		UC2 MASTER DA H	BD2

012474 012767 012510 166406  
012502 004767 011774

IS: MOV #25,SLPERR ;SET UP ERROR RETURN  
JSR PC,SELIN E ;GO SELECT A LINE NO. TO TEST



# F01

MAINDEC-11-DZDMM-B  
DZDMMB.P11 T42

MACY11 271732) 23-SEP-76 14:33 PAGE 94  
VERIFY STORAGE OVERFLOW - NON MAINT. MODE - ALL SELECTED LINES

SEQ 0212

3942 012766 004567  
3943 012772 030212  
3944 012774 034631  
3945 012776 104057  
3946  
3947 013000 000640

211602

JSR RS,SUNUM  
LINE  
EMS7+44  
ERROR 57  
BR 1\$

;PUT LINE NO. IN MSG

:READING SILO F \*LED TO DEC SSP OR  
:STORAGE OVFL SE \*AT WRONG COUNT  
:GO TRY NEXT LINE

GO1

MAINDEC-11-DZDMM-8  
DZDMMB.P11 T43

MACY11 27(732) 23-SEP-76 14:33 PAGE 95  
BASIC DATA TEST - ALL SELECTED LINES ALL CHAR LENGTHS

SEG 0213

3948  
3949  
3950  
3951 013002 000004  
3952  
3953  
3954  
3955  
3956  
3957  
3958  
3959  
3960  
3961  
3962  
3963  
3964  
3965  
3966  
3967  
3968  
3969  
3970  
3971  
3972  
3973  
3974  
3975  
3976  
3977  
3978  
3979  
3980  
3981  
3982  
3983  
3984  
3985  
3986  
3987  
3988  
3989  
4000  
4001  
4002  
4003 013004 012767 013032 166076

\*\*\*\*\*  
:TEST 43 BASIC DATA TEST - ALL SELECTED LINES ALL CHAR LENGTHS  
\*\*\*\*\*  
↑ST43: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT A SINGLE ALL ONES CHAR. CAN BE TRANS-  
MITTED AND RECEIVED ON ALL SELECTED LINES AT ALL FOUR CHAR LENGTHS  
(5, 6, 7, AND 8 BITS). THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP THE ERROR LOOP RETURN
2. SELECT A LINE NO. TO TEST - GO TO TEST 43 IF DONE ALL  
SELECTED LINES.
3. GET A TEST CHARACTER FROM THE DATA TABLE AND UPDATE THE  
TABLE POINTER.
4. CLEAR THE DH11
5. PRIME THE SELECTED LINE TO XMIT ONE CHAR AT 9600 BAUD
6. WAIT FOR "CHAR AVAIL" TO SET - IF TIMEOUT REPORT ERROR AND  
RESTART AT STEP 3.
7. IF NO TIMEOUT - CHECK DATA AND REPORT ANY ERRORS
8. INCREMENT "SCR" REG TO CHANGE CHAR LENGTH - IF DONE  
ALL FOUR GO TO STEP 2 - IF NOT THEN STEP 4.

ERRORS:  
\*\*\*\*\*

1. [ERROR 55] IS CALLED TO REPORT RCVR TIMEOUT.
2. [ERROR 23] IS CALLED TO REPORT DATA COMPARE ERRORS

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. IF FAULT AFFECTS ONLY ONE LINE AT ALL CHAR LENGTHS, SUSPECT A  
BAD UART MODULE M7280.
2. IF FAULT AFFECTS ONLY ONE BIT ON ALL LINES, SUSPECT THE  
THE M7279 MODULE.
3. IF FAULT AFFECTS ONLY CERTAIN CHAR LENGTHS, SUSPECT EITHER THE M7279  
OR THE UART MODULE M7280.

KEY LOGIC:  
\*\*\*\*\*

M7280'S UART CHIPS PINS <12:05>

M7279 SH1 E1,E2,E6, OR E7

M7278 SH8 NB2 LPR 01 H FH1  
NB1 LPR 00 H FH2

MOV \*3\$, \$LPERR ;SET UP ERROR LOOP RETURN

# H01

MAINDEC-11-02DHM-B  
02DAMB.P11 T43

MACY11 27(732) 23-SEP-76 14:33 PAGE 96  
BASIC DATA TEST - ALL SELECTED LINES/ALL CHAR LENGTHS

SEQ 0214

4004	013012	004767	011464		1\$: JSR	PC, SELINE	;GO SELECT A LINE TO TEST
4005	013016	000511			BR	TST44	;BR IF DONE ALL SELECTED LINES
4006	013020	012705	030226		MOV	#TDATA2, R5	;GET POINTER TO DATA TABLE
4007	013024	005002			CLR	R2	;INIT R2 TO START AT CHAR LENGTH OF 5 BITS
4008	013026	012557	166156		2\$: MOV	(R5)+, \$TMP7	;PUT TEST CHAR IN XMIT BUFFER
4009	013032	012711	004000		3\$: MOV	#BIT11, (R1)	;CLEAR THE DH11
4010	013036	156711	015150		SISB	LINE, (R1)	;SELECT THE LINE
4011	013042	012761	177777	000010	MOV	#-1, BCR(R1)	;SET BYTE COUNT TO -1
4012	013050	012761	001220	000006	MOV	#\$TMP7, CAR(R1)	;SET CURRENT ADDRESS REG
4013	013056	012761	033500	000004	MOV	#33500, LPR(R1)	;SET BAUD RATE TO 9600
4014	013064	050261	000004		BIS	R2, LPR(R1)	;SELECT CHAR LENGTH
4015	013070	156761	014110	000012	BISB	LINMSK, BAR(R1)	;ACTIVATE THE SELECTED LINE
4016							
4017	013076	012767	000001	015134	MOV	#1, TIMEA	;INIT TIMER A
4018	013104	005067	015132		CLR	TIMEB	;INIT TIMER B
4019	013110	105711			4\$: TSTB	(R1)	;RCVR DONE YET ??
4020	013112	100424			BMI	5\$	;BR IF YES
4021	013114	004767	013624		JSR	PC, TIMEIT	;CALL THE TIMER
4022	013120	000773			BR	4\$	;TIMER ROUTINE WILL MOVE RETURN PC
4023							;AROUND THIS BRANCH IF TIME OUT OCCURS
4024							
4025	013122	004767	014000		JSR	PC, SAPS	;SAVE THE ERROR PSW
4026	013126	011103			MOV	(R1), R3	;GET THE SCR
4027	013130	042703	177560		BIC	#177560, R3	;CLEAR UNINTERESTING BITS
4028	013134	012704	000200		MOV	#200, R4	;SET UP S/B DATA
4029	013140	156704	015046		BISB	LINE, R4	
4030	013144	004767	011204		JSR	PC, SUER2A	;GO SET UP ERROR INFO
4031	013150	004567	011420		JSR	R5, SUNUM	;GO SET LINE NO. IN MSG
4032	013154	030212			LINE		
4033	013156	031766			EM22+51		
4034	013160	104055			ERROR	5\$	;CHAR AVAIL FAILED TO SET ON TIME
4035	013162	000422			BR	6\$	;GO TEST NEXT CHAR LENGTH
4036							
4037	013164	016103	000002		5\$: MOV	NRC(R1), R3	;GET THE WAS DATA
4038	013170	012704	000200		MOV	#200, R4	;SET UP THE S/B DATA IN R4
4039	013174	156704	015012		BISB	LINE, R4	
4040	013200	000304			SWAB	R4	
4041	013202	156704	166012		BISB	\$TMP7, R4	
4042	013206	020304			CMP	R3, R4	;WAS THE RCVD DATA CORRECT ??
4043	013210	001407			BEQ	6\$	;BR IF YES
4044							
4045	013212	004767	011132		JSR	PC, SUER2	;GO SET UP THE ERROR INFO
4046	013216	004567	011352		JSR	R5, SUNUM	;GO PUT LINE NO. IN MSG
4047	013222	030212			LINE		
4048	013224	032027			EM23+36		
4049	013226	104023			ERROR	23	;DATA COMPARE ERROR
4050							
4051	013230	005202			6\$: INC	R2	;DO NEXT CHAR LENGTH ON SELECTED LINE
4052	013232	022702	000004		CMP	#4, R2	;HAVE WE DONE ALL FOUR CHAR LENGTHS ??
4053	013236	001273			BNE	2\$	;BR IF NOT
4054	013240	000664			BR	1\$	;GO DO NEXT LINE

4055  
4056  
4057  
4058  
4059  
4060  
4061  
4062  
4063  
4064  
4065  
4066  
4067  
4068  
4069  
4070  
4071  
4072  
4073  
4074  
4075  
4076  
4077  
4078  
4079  
4080  
4081  
4082  
4083  
4084  
4085  
4086  
4087  
4088  
4089  
4090  
4091  
4092  
4093  
4094  
4095  
4096  
4097  
4098  
4099  
4100  
4101  
4102  
4103  
4104  
4105  
4106  
4107  
4108  
4109  
4110

013242 003004

::\*\*\*\*\*  
: \*TEST 44 SINGLE LINE DATA TEST - ALL SELECTED LINES  
: \*\*\*\*\*  
†ST44: SCOPE  
.REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST TRANSMITS AND RECEIVES A BINARY COUNT PATTERN  
(000 - 377) ON ALL SELECTED LINES. THE TEST SEQUENCE IS AS  
FOLLOWS:

1. SET UP THE ERROR LOOP RETURN
2. GO SELECT A LINE NO. TO TEST - IF DONE ALL SELECTED LINES THEN GO TO TEST 44.
3. CLEAR THE DH11 AND PRIME THE SELECTED LINE TO XMIT TO XMIT 256. CHARS AT 9600. BAUD - 8 BIT CHARS.
4. SET UP R5 TO POINT TO RCVR CORE BUFFER.
5. ACTIVATE THE SELECTED XMITTER.
6. WAIT FOR "CHAR AVAIL" TO SET BEFORE READING THE SILO. IF RCVR TIMEOUT REPORT ERROR AND RESTART AT STEP 2.
7. IF NO TIMEOUT READ THE SILO AND STORE THE WORD IN THE RCVR CORE BUFFER - WHEN THE BUFFER IS FULL GO TO STEP 8 IF NOT THEN GO TO STEP 6.
8. COMPARE THE XMIT AND RCVR CORE IMAGE BUFFERS AND REPORT ALL DATA COMPARE ERRORS.
9. CHECK THE "BAR" "BCR" AND "CAR" REGISTERS FOR CORRECT CONTENTS - REPORT ALL ERRORS.
10. GO TO STEP 2

NOTE: THIS TEST USES THE MAINT. BIT (SCRD9=1) TO TURN THE DATA AROUND INSTEAD OF THE MAINT CONNECTORS OR MODULE.

ERRORS:  
\*\*\*\*\*

1. [ERROR 22] IS CALLED TO REPORT "DATA AVAIL" TIMEOUT
2. [ERROR 37] " " " DATA COMPARE ERRORS
3. [ERROR 40] " " " "BAR" REG NOT CLEARED
4. [ERROR 10] " " " "BCR" REG NOT ALL ZEROES
5. [ERROR 7] " " " "CAR" REG NOT UPDATED CORRECTLY

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. IF THE FAULT AFFECTS ONE OR MORE LINES IN AN 8 LINE GROUP <15:08> OR <07:00>, SWAP THE M7280 MODULES. IF THE FAULT SHIFTS SO THAT THE ERROR INDICATES DIFFERENT LINES THE PROBLEM IS MOST LIKELY THE M7280 THE SYMPTOM SHIFTED TO.
2. IF THE FAULT GIVES DATA ERRORS BUT AFFECTS ONLY CERTAIN PATTERNS ON ONE LINE THE FAULT IS MOST LIKELY A "UART" CHIP.



- 3. IF THE FAULT GIVES DATA ERRORS BUT AFFECTS ONLY CERTAIN PATTERNS ON ALL LINES SUSPECT THE DATA PATHS EXTERNAL TO, THE M7280 MODULES.
- 4. IF THE FAULT CAUSES NO DATA ERRORS BUT GIVES "BAR", "BCR", OR "CAR" ERRORS SUSPECT THE M7278 OR M7277 MODULES RESPECTFULLY.

KEY LOGIC (REFER TO TEST 43)  
\*\*\*\*\*

4111									
4112									
4113									
4114									
4115									
4116									
4117									
4118									
4119									
4120									
4121									
4122	013244	012767	013266	165636	%	MOV	#25, \$LPERR	;SET UP ERROR LOOP RETURN	
4123	013252	004767	011224		1\$:	JSR	PC, SELINE	;GO SELECT A LINE TO TEST	
4124	013256	000401				BR	11\$	;BR IF ALL SELECTED LINES DONE	
4125	013260	000402				BR	2\$	;GO TEST IT	
4126	013262	000167	000424		11\$:	JMP	2\$	;EXIT TEST	
4127	013266	016701	013700		2\$:	MOV	DHADR, R1	;RESET DEVADR	
4128	013272	012711	004000			MOV	#BIT11, (R1)	;CLEAR THE DH11	
4129	013276	156711	014710			BISB	LINE, (R1)	;SET SELECT BITS IN SCR	
4130	013302	012761	037112	000006		MOV	#TBUF, CAR(R1)	;SET UP BUS ADDRESS REG	
4131	013310	012761	177400	000010		MOV	#-400, BCR(R1)	;SET UP BYTE COUNT	
4132	013316	012761	033503	000004		MOV	#33503, LPR(R1)	;SET LINE PARAMETERS	
4133	013324	012705	036112			MOV	#RBUF, R5	;SET UP POINTER TO INPUT DATA BUFFER	
4134	013330	052711	001000			BIS	#BIT09, (R1)	;SET MAINT MODE BIT	
4135	013334	016761	013644	000012		MOV	LINMSK, BAR(R1)	;ACTIVATE THE SELECTED LINE	
4136									
4137	013342	012767	000002	014670		MOV	#2, TIMEA	;INIT TIMER A	
4138	013350	005067	014666			CLR	TIMES	;INIT TIMER B	
4139	013354	105711			3\$:	TSTB	(R1)	;RCVR DONE YET ??	
4140	013356	100425				BMI	4\$	;BR IF YES	
4141	013360	004767	013360			JSR	PC, TIMEIT	;CALL THE TIMER	
4142	013364	000773				BR	3\$	;TIMER ROUTINE WILL MOVE RETURN PC AROUND THIS BRANCH IF TIME OUT OCCURS	
4143									
4144									
4145	013366	004767	013534			JSR	PC, SAPS	;SAVE THE ERROR PSW	
4146	013372	010102				MOV	R1, R2	;SET UP REGADR	
4147	013374	011203				MOV	(R2), R3	;GET THE WAS DATA	
4148	013376	042703	176400			BIC	#176400, R3	;CLEAR JUNK BITS	
4149	013402	012704	001200			MOV	#1200, R4	;SET UP S/B DATA	
4150	013406	156704	014600			BISB	LINE, R4		
4151	013412	004767	010736			JSR	PC, SUER2A	;GO SET UP ERROR INFO	
4152	013416	004567	011152			JSR	R5, SUNUM	;PUT LINE NO. IN MESSAGE	
4153	013422	030212				LINE			
4154	013424	031765				EM22+51			
4155	013426	104022				ERROR	22	;CHAR AVAIL TIMEOUT	
4156	013430	000710				BR	1\$	;GO TRY NEXT LINE	
4157									
4158	013432	016125	000002		4\$:	MOV	NRC(R1), (R5)+	;SAVE THE RECEIVED DATA	
4159	013436	022705	037112			CMP	#RBUF+1000, R5	;INPUT BUFFER FULL ??	
4160	013442	001344				BNE	3\$	;BR IF NOT	
4161									
4162	013444	012702	037112			MOV	#TBUF, R2	;SET UP POINTER TO OUTPUT BUFFER	
4163	013450	012701	036112			MOV	#RBUF, R1	;SET UP POINTER TO INPUT BUFFER	
4164	013454	111204			5\$:	MOVSB	(R2), R4	;SET UP S/B DATA IN R4	
4165	013456	042704	177400			BIC	#177400, R4		
4166	013452	000304				SWAB	R4		

K01

MAINDEC-11-DZDHM-B  
DZDHMB.P11 T44

MACY11 27(732) 23-SEP-76 14:33 PAGE 99  
SINGLE LINE DATA TEST - ALL SELECTED LINES

SEQ 0217

4167	013464	156704	014522	BISB	LINE,R4	
4168	013470	152704	000200	BISB	#200,R4	
4169	013474	000304		SWAB	R4	
4170	013476	011103		MOV	(R1),R3	;GET THE WAS DATA
4171	013500	020304		CMP	R3,R4	;DATA CORRECT ??
4172	013502	001407		BEQ	6\$	;BR IF YES
4173						
4174	013504	004767	010640	JSR	PC,SUER2	;GO SET UP ERROR INFO
4175	013510	004567	011060	JSR	R5,SUNUM	;PUT LINE NO. IN MESSAGE
4176	013514	030212		LINE		
4177	013516	033244		EM37+33		
4178	013520	104037		ERROR	37	;DATA COMPARE ERROR
4179						
4180						
4181	013522	005202		6\$: INC	R2	;UPDATE DATA BUFFER POINTERS
4182	013524	062701	000002	ADD	#2,R1	
4183	013530	022701	037112	CMP	#RBUF+1000,R1	;COMPARED ALL 256. CHARS ??
4184	013534	001347		BNE	5\$	;BR IF NOT
4185						
4186	013536	016701	013430	MOV	DHADR,R1	;RESET DEVADR
4187	013542	010102		MOV	R1,R2	;SET UP REGADR
4188	013544	062702	000012	ADD	#BAR,R2	
4189	013550	005712		TST	(R2)	;WAS THE "BAR" ALL ZEROES ??
4190	013552	001413		BEQ	7\$	;BR IF YES
4191						
4192	013554	004767	013346	JSR	PC,SAPS	;SAVE THE ERROR PSW
4193	013560	011203		MOV	(R2),R3	;GET THE WAS DATA
4194	013562	005004		CLR	R4	;SET UP S/B DATA
4195	013564	004767	010564	JSR	PC,SUER2A	;GO SET UP ERROR INFO
4196	013570	004567	011000	JSR	R5,SUNUM	;PUT LINE NO. IN MESSAGE
4197	013574	030212		LINE		
4198	013576	033307		EM40+40		
4199	013600	104040		ERROR	40	; "BAR" REG NOT ALL ZEROES
4200						
4201	013602	010102		7\$: MOV	R1,R2	;SET UP REGADR
4202	013604	062702	000010	ADD	#BCR,R2	
4203	013610	005712		TST	(R2)	;BYTE COUNT REG ALL ZEROES ?
4204	013612	001413		BEQ	71\$	;BR IF BYTE COUNT ZERO
4205						
4206	013614	004767	013306	JSR	PC,SAPS	;SAVE THE ERROR PSW
4207	013620	011203		MOV	(R2),R3	;GET THE WAS DATA
4208	013622	005004		CLR	R4	;SET UP THE S/B DATA
4209	013624	004767	010524	JSR	PC,SUER2A	;GO SET UP ERROR INFO
4210	013630	004567	010740	JSR	R5,SUNUM	;PUT LINE NO. IN MESSAGE
4211	013634	030212		LINE		
4212	013636	031114		EM10+44		
4213	013640	104010		ERROR	10	;BYTE COUNT NOT ALL ZEROES
4214						
4215	013642	010102		71\$: MOV	R1,R2	;SET UP REGADR
4216	013644	062702	000006	ADD	#CAR,R2	
4217	013650	022712	037512	CMP	#TBUF+400,(R2)	;DID "CAR" INCREMENT PROPERLY ?
4218	013654	001414		BEQ	72\$	;BR IF YES
4219						
4220	013656	004767	013244	JSR	PC,SAPS	;SAVE THE ERROR PSW
4221	013662	011203		MOV	(R2),R3	;GET THE WAS DATA
4222	013664	012704	037512	MOV	#TBUF+400,R4	;SET UP S B DATA

L01

MAINDEC-11-DZDHM-8  
DZDHMB.P11 T44

MACY11 27(732) 23-SEP-76 14:33 PAGE 100  
SINGLE LINE DATA TEST - ALL SELECTED LINES

SEQ 0218

4223	013670	004767	010460	JSR	PC,SUER2A	:GO SET UP ERROR INFO
4224	013674	004567	010674	JSR	R5,SUNUM	:GO PUT LINE NO IN MESSAGE
4225	013700	030212		LINE		
4226	013702	031045		EM7+47		
4227	013704	104007		ERROR	7	;"CAR" NOT UPDATED CORRECTLY
4228						
4229	013706	000167	177340	72\$: JMP	1\$	:GO DO NEXT LINE
4230						
4231	013712	000240		8\$: NOP		:EXIT POINT



# NO1

MACY11-11-DZDMM-B  
 014111.P11 T45

MACY11 27(732) 23-SEP-76 14:33 PAGE 102  
 BASIC PARITY LOGIC TEST - ALL SELECTED LINES - ODD PARITY

SEQ 0220

014044	004767	013056		JSR	PC,SAPS	;AROUND THIS BRANCH IF TIME OUT OCCURS
014050	011103			MOV	(R1),R3	;SAVE THE ERROR PSW
014052	012704	100200		MOV	#100200,R4	;GET THE WAS DATA
014056	156704	014130		BISB	LINE,R4	;SET UP THE S/B DATA
014062	010102			MOV	R1,R2	;SET UP REGADR
014064	004767	010264		JSR	PC,SUER2A	;GO SET UP ERROR INFO
014070	004567	010500		JSR	R5,SUNUM	;PUT LINE NO. IN MESSAGE
014074	030212			LINE		
014076	031766			EM22+51		
014100	104022			ERROR	22	;TIMED OUT WAITING FOR DATA AVAIL
014102	000710			BR	1\$	;GO TEST NEXT LINE
014104	016103	000002	4\$:	MOV	NRC(R1),R3	;GET THE WAS DATA
014110	020304			CMP	R3,R4	;CORRECT DATA RECEIVED ??
014112	001704			BEG	1\$	;BR IF YES
014114	004767	013006		JSR	PC,SAPS	;SAVE THE ERROR PSW
014120	010102			MOV	R1,R2	;SET UP THE REGADR
014122	062702	000002		ADD	#NRC,R2	
014126	004767	010222		JSR	PC,SUER2A	;GO SET UP ERROR INFO
014132	004567	010436		JSR	R5,SUNUM	;PUT LINE NO. IN MESSAGE
014136	030212			LINE		
014140	032760			EM33+40		
014142	104033			ERROR	33	;INCORRECT DATA OR PARITY ERROR
014144	000667			BR	1\$	;GO TEST NEXT LINE

014146 000004

\*\*\*\*\*  
\*TEST 46 MULTI-LINE PARITY DATA TEST - ALL SELECTED LINES  
\*\*\*\*\*  
†ST46: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES ALL SELECTED LINES CAN TRANSMIT AND RECEIVE  
A BINARY COUNT PATTERN WHEN RUN CONCURRENTLY. ALL CHAR LENGTHS (5, 6, 7,  
AND 8 BITS) ARE TESTED WITH BOTH EVEN AND ODD PARITY CHECKING SPECIFIED.  
THE TEST ACTUALLY INCLUDES EIGHT SUB-TESTS - THE PARAMETERS FOR EACH  
SUB-TEST RETRIEVED FROM A TABLE TAGGED "PRTYTB:". REFER TO THIS TABLE  
TO DETERMINE THE TEST SEQUENCE.

ERRORS:  
\*\*\*\*\*

- 1. [ERROR 41] IS CALLED TO REPORT FALSE RECEIVER INTRs.
- 2. [ERROR 42] IS CALLED TO REPORT SILO OVERFLOW ERRORS
- 3. [ERROR 34] IS CALLED TO REPORT PARITY/DATA ERRORS
- 4. [ERROR 35] IS CALLED TO REPORT TEST TIMEOUTS

SYNC: (NONE)  
\*\*\*\*\*

DEBUG: (REFER TO TEST 45)  
\*\*\*\*\*

KEY LOGIC: (REFER TO TEST 45)  
\*\*\*\*\*

01276 014:66 164732  
000000 027310  
000000 001100  
000000 012756  
000000 164776  
000000 164770  
000000 164770  
000000 004000  
000000 010516  
000000 164734  
000000 164734  
000000 012632  
000000 012710  
000000 014256  
000000 000000  
000000 013:42

%  
15:  
25:  
MOV #15, \$LPERR ;SET UP THE ERROR LOOP RETURN  
MOV #PRTYTB+4, R5 ;SET UP POINTER TO TEST PARAMETERS  
CLR \$TMP7 ;START WITH SUB TEST #00  
SUB #4, R5 ;RESET POINTER FOR ERROR LOOPS  
DEC \$TMP7 ;RESET SUB TEST # FOR ERROR LOOP  
CMP #PRTYTB+40, R5 ;DONE ALL 9. SUB TESTS ??  
BEQ 21\$ ;BR IF YES  
MOV \$STACK, SP ;RESET STACK POINTER FOR ERROR LOOPS  
CHADR, R1 ;RESET DEVADR FOR ERROR LOOPS  
MOV (R5)+, \$TMP6 ;GET THE BYTE COUNT PARAMETER  
MOV (R5)+, \$TMP5 ;GET THE LINE PARAMETERS  
INC \$TMP7 ;GENERATE NEW SUB-TEST NO.  
MOV #BIT11, (R1) ;CLEAR THE DH11  
JSR PC, SUPPAR ;GO SET UP PARAMETERS  
MOV LPA(R1), \$TMP0 ;SAVE CURRENT LINE PARAMETERS  
MOV LINSSEL, \$TMP3 ;SAVE SELECTED LINES PARAMETER  
JSR PC, CHPS2 ;GO LOCK OUT INTRs  
MOV DHVCT, R2 ;SET UP THE VECTOR  
MOV #35, (R2)+ ;GO TO 35 ON RCVR INTERRUPT  
MOV #100, (R1) ;ENABLE CHAR AVAIL INTERRUPTS  
MOV LINSSEL, LINACT ;FLAG ALL SELECTED LINES ACTIVE

```

014336 016761 012670 000012      MOV      LINSEL, BAR(R1)  :ACTIVATE ALL SELECTED LINES
014337 016762 164562 164664      MOVB     STSTNM, STMP2   :SAVE THE TEST NO.
014338 016763 164563 164665      BIC      #177400, STMP2
014339 004767 012542      JSR      PC, CHPS1      :GO CLEAR PSW
014340 000167 000232      JMP      *              :GO WAIT FOR INTERRUPTS

014340 012706 001100      218:    MOV      #STACK, SP      :RESTORE THE SP
014341 004767 012526      JSR      PC, CHPS1      :GO CLEAR PSW
014342 004767 012342      JSR      PC, RESTRP     :RESTORE TRAP CATCHER
014343 000554      BR       TS147          :GO TO NEXT TEST

:RECEIVER INTERRUPT SERVICE ROUTINE

014366 005067 164630      35:    CLR      STMP4          :CHAR AVAIL SET
014367 005068 005068      TSTB    (R1)           :BR IF YES
014368 005069 005069      BMI     45

014366 012711 004000      MOV      #BIT11, (R1)   :CLEAR OUT THE DH11
014367 005068 005068      ERROR   41            :RCVR FALSE INTERRUPT - CHAR AVAIL NOT SET
014368 005069 005069      BR      25            :GO TRY NEXT SUB TEST

014366 005067 040000      45:    BIT      #BIT14, (R1)  :SILO OVERFLOW ??
014367 005068 005068      BEQ     55            :BR IF NOT

014366 005067 004000      MOV      #BIT11, (R1)   :CLEAR OUT THE DH11
014367 005068 005068      ERROR   42            :SILO OVERFLOW ERROR
014368 005069 005069      BR      25            :GO TRY NEXT SUB TEST

014366 000002 000002      55:    MOV      NRC(R1), R3    :GET THE WAS DATA
014367 000003 000003      MOV     R3, R2          :EXTRACT AND SAVE LINE NO.
014368 000004 177760      SWAB    R2
014369 000005 164554      BIC     #177760, R2     :GENERATE TABLE OFFSETR
014370 000006 000006      ASL    R2
014371 000007 164554      INC     STMP4
014372 000008 000008      CMP     #101, STMP4
014373 000009 000009      BEQ     65
014374 000010 030136 012526      BIT     $LINSEL(R2), LINSEL :IS THIS ONE OF THE SELECTED LINES?
014375 000011 000011      BEQ     55            :IF NOT, THIS IS GARBAGE, SO CHECK NEXT SILCO ENTRY.
014376 000012 164530      MOV     R2, STMP4
014377 000013 164524      ASR    STMP4
014378 000014 036112      CMP     RBUF(R2), R3    :CORRECT DATA RECEIVED ??
014379 000015 000015      BEQ     65            :BR IF YES

014376 004767 012426      JSR     PC, SAPS        :SAVE THE ERROR PSW
014377 000016 012711 004000      MOV     #BIT11, (R1)   :CLEAR OUT THE DH11
014378 000017 016204 036112      MOV     RBUF(R2), R4    :SET UP S B DATA
014379 000018 062701 000002      ADD     #NRC, R1        :SET UP WAS ADDRESS
014380 000019 062702 036112      ADD     #RBUF, R2       :SET UP S B ADDRESS
014381 000020 004767 007630      JSR     PC, SUER2A     :GO SET UP ERROR INFO
014382 000021 004567 010044      JSR     R5, SUNUM      :PUT LINE NO. IN MESSAGE
014383 000022 001212      STMP4
014384 000023 003034      EM34+51
014385 000024 004567 010034      JSR     R5, SUNUM      :PUT SUBTEST NO. IN MESSAGE
014386 000025 003035      STMP7
014387 000026 003036      EM34+67
014388 000027 003037      ERROR   34            :PARITY DATA COMPARE ERROR

```

```

014546 000613 BR 25 ;GO TRY NEXT SUBTEST
014550 105262 036112 65: INCB RBUF(R2) ;GENERATE NEW RCVD DATA
014554 005067 027452 INC MULPTB(R2) ;COUNT ONE BYTES RECEIVED
014558 001003 BNE 615 ;BR IF NOT DONE
014562 046267 027410 012660 BIC LINBIT(R2),LINACT ;FLAG THIS LINE DONE
014570 000002 615: RTI ;RETURN TO WAIT ROUTINE
;WAIT ROUTINE
014572 012767 000002 013440 75: MOV #2,TIMEA ;INIT TIMER A
014576 005067 013436 CLR TIMEB ;INIT TIMER B
014580 005761 000012 85: TST BAR(R1) ;ALL LINES DONE XMITTING ??
014584 001412 BEQ 95 ;BR IF YES
014588 004767 012126 JSR PC,TIMEIT ;CALL THE TIMER
014596 000772 BR 95 ;TIMER ROUTINE WILL MOVE RETURN PC
;AROUND THIS BRANCH IF TIME OUT OCCURS
014600 016167 000012 164362 MOV BAR(R1),STMP3 ;SAVE THE ACTIVE LINES FLAG
014604 012711 004000 MOV #BIT11,(R1) ;CLEAR OUT THE DH11
014608 104035 ERROR 35 ;TIMED OUT WAITING FOR TRANSMITTERS TO FINISH
014612 000167 177336 JMP 25 ;GO TRY NEXT SUBTEST
014616 012767 000001 013372 95: MOV #1,TIMEA ;INIT TIMER A
014620 005067 013370 CLR TIMEB ;INIT TIMER B
014624 005767 012572 105: TST LINACT ;ALL CHARS RECEIVED ?
014628 001411 BEQ 115 ;BR IF YES
014632 004767 012060 JSR PC,TIMEIT ;CALL THE TIMER
014636 000772 BR 105 ;TIMER ROUTINE WILL MOVE RETURN PC
;AROUND THIS BRANCH IF TIME OUT OCCURS
014640 016767 012556 164314 MOV LINACT,STMP3 ;SET UP ACTIVE LINE PARAMETER
014644 012711 004000 MOV #BIT11,(R1) ;CLEAR OUT THE DH11
014648 104035 ERROR 35 ;SILE EMPTY TIMEOUT
014652 000167 177270 115: JMP 25 ;GO TRY NEXT SUB TEST

```







45	015142	000677			BR	15		;GO TRY NEXT LINE
	015144	005267	164046		45:	INC	\$TMP6	;COUNT ONE CHAR RECVD
	015150	016103	000002			MOV	NRC(R1),R3	;GET THE WAS DATA
	015154	020394				CMP	R3,R4	;WAS CHAR AUTO ECHOED CORRECTLY ?
	015156	001417				BEG	55	;BR IF YES
	015160	004767	011742			JSR	PC,SAPS	;SAVE THE ERROR PSW
	015164	005061	000004			CLR	LPR(R1)	;DISABLE AUTO ECHO
	015170	010102				MOV	R1,R2	;SET UP REGADR
	015172	062702	000002			ADD	#NRC,R2	
	015176	004767	007152			JSR	PC,SUER2A	;GO SET UP ERROR INFO
	015202	004567	007366			JSR	R5,SUNUM	;PUT LINE NO. IN ERROR MSG
	015206	030212				LINE		
	015210	032164				EM24+35		
	015212	104024				ERROR	24	;CHAR AUTO ECHOED INCORRECTLY
	015214	000652				BR	15	;GO TRY NEXT LINE
	015216	005367	163776		55:	DEC	\$TMP7	;COUNT ONE CHAR READ OUT OF 54
	015222	003317				BGT	35	;BR IF NOT LAST ONE
	015224	100646				BMI	15	;BR IF LAST ONE READ
	015226	042761	100000	000004		BIC	#BIT15,LPR(R1)	;DISABLE AUTO ECHO
	015234	000712				BR	35	;GO READ LAST CHAR
	015236	005167	163746		65:	COM	\$TMP3	;TOGGLE I/O FLAG
	015242	001406				BEG	TST50	;BR IF DONE BOTH I/O DATA
	015244	005067	012742			CLR	LINE	;INIT LINE NO TO CO
	015250	012705	027350			MOV	#AETAB0,R5	;SET POINTER TO O'S TABLE
	015254	000167	177452			JMP	75	;REPEAT TEST FOR ZERO PATTERNS

4600  
4601  
4602  
4603  
4604  
4605  
4606  
4607  
4608  
4609  
4610  
4611  
4612  
4613  
4614  
4615  
4616  
4617  
4618  
4619  
4620  
4621  
4622  
4623  
4624  
4625  
4626  
4627  
4628  
4629  
4630  
4631  
4632  
4633  
4634  
4635  
4636  
4637  
4638  
4639  
4640  
4641  
4642  
4643  
4644  
4645  
4646  
4647  
4648  
4649  
4650  
4651  
4652  
4653  
4654  
4655  
4656  
4657  
4658  
4659  
4660

015260 000004

::\*\*\*\*\*  
: \*TEST 50 AUTO ECHO TEST 2 - ALL SELECTED LINES  
:\*\*\*\*\*  
†T50: SCOPE  
.REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST IS SIMILAR TO TEST 47 EXCEPT ALL SELECTED LINES OTHER THAN THE A.E. TEST LINE ARE ACTIVELY TURNING AROUND A BINARY COUNT TEST PATTERN IN NON-AUTO ECHO MODE AND THE A.E. TEST LINE IS TESTED FOR ALL 1'S DATA ONLY.

ERRORS:  
\*\*\*\*\*

- 1. [ERROR 32] IS CALLED TO REPORT A.E. TEST TIMEOUTS
- 2. [ERROR 31] IS CALLED TO REPORT ALL DATA COMPARE ERRORS

SYNC: M7277 SH4 LOAD BAR LB+HB L CN2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

REFER TO TEST 47

KEY LOGIC:  
\*\*\*\*\*

REFER TO TEST 47

015262 012767 015336 163620  
015270 012705 027310  
015274 005067 011706  
015300 000261  
015302 000401  
015304 000241  
015306 006167 011674  
015312 001410  
015314 012567 163700  
015320 036767 011662 011654  
015326 001766  
015330 004767 007146  
015334  
015334 000575  
015336 016701 011630  
015342 012711 004000  
015346 004767 011414  
015352 156711 012634  
015356 010561 000006  
015362 162761 000002 000006  
015370 012761 177777 000010

%  
MOV #25,\$LPERR ;SET UP ERROR LOOP RETURN  
MOV #AETAB,R5 ;SET POINTER TO A.E. TEST DATA TABLE  
CLR LMSK1 ;INIT BIT TEST MASK  
SEC ;GENERATER MARKER BIT IN "0"  
BR 12\$ ;GO SHIFT MASK  
1\$: CLC ;INIT THE "C" BIT  
12\$: ROL LMSK1 ;SHIFT TEST BIT  
BEQ 11\$ ;BR IF TESTED ALL LINES  
MOV (R5)+,\$TMP7 ;GET THE A.E. TEST DATA FOR THIS LINE  
BIT LMSK1,LINSEL ;TEST THIS LINE ?  
BEQ 11\$ ;BR IF NOT  
JSR PC,SELIN ;GO SELECT A LINE  
11\$: BR TST51 ;;BR IF DONE ALL SELECTED LINES  
2\$: MOV DHADR,R1 ;RESET DEVADR IN CASE OF ERROR LOOP  
MOV #BIT11,(R1) ;CLEAR OUT THE DH11  
JSR PC,SETALL ;GO SET UP FOR BINARY COUNT XFER ON  
;ALL LINES OTHER THAN THE SELECTED ONE  
BISB LINE,(R1) ;SELECT THE LINE FOR A.E. TEST  
MOV R5,CAR(R1) ;SET BUS ADDR TO XMIT TEST CHAR  
SUB #2,CAR(R1) ;CORRECT THE ADDRESS  
MOV #-1,BCR(R1) ;XMIT ONE CHAR ON THIS LINE

*Handwritten mark*

```

4661 015376 012761 133503 000004      MOV      #133503,LPR(R1) ;DO IT AT 9600 BAUD/8 BITS
4662 015411 116767 163472 163574      MOVVB   $STNM,$TMP2    ;SAVE THE TEST NO.
4663 015412 042767 177400 163566      BIC     #177400,$TMP2
4664 015420 046767 011560 012022      BIC     LINMSK,LINACT  ;MAKE THIS LINE APPEAR INACTIVE
4665 015426 016761 011550 000012      MOV     LINSEL,BAR(R1) ;ACTIVATE ALL SELECTED TRANSMITTERS
4666
4667 015434 012767 000002 012576 21$:  MOV     #2,TIMEA      ;INIT TIMER A
4668 015442 005067 012574          CLR     TIMEB        ;INIT TIMER B
4669 015446 016103 000002          MOV     NRC(R1),R3   ;GET THE WAS DATA
4670 015452 100414          BMI    4$           ;BR IF YES
4671 015454 004767 011264          JSR    PC,TIMEIT     ;CALL THE TIMER
4672 015460 000772          BR     3$           ;TIMER ROUTINE WILL MOVE RETURN PC
4673                                     ;AROUND THIS BRANCH IF TIME OUT OCCURS
4674
4675 015462 016167 000004 163512      MOV     LPR(R1),$TMP0 ;SAVE THE CURRENT "LPR"
4676 015470 004567 007100          JSR    R5,SUNUM     ;PUT LINE NO. IN MESSAGE
4677 015474 030212          LINE
4678 015476 032655          EM32+35
4679 015500 104032          ERROR  32          ;AUTO ECHO TIMEOUT
4680 015502 000700          BR     1$           ;GO TRY NEXT LINE
4681
4682 015504 010304          4$:  MOV     R3,R4        ;EXTRACT LINE NUMBER OF RCVD CHAR
4683 015506 000304          SWAB   R4
4684 015510 042704 177760          BIC    #177760,R4
4685 015514 010402          MOV    R4,R2        ;SAVE IT IN R2
4686 015516 006302          ASL   R2            ;GENERATE TABLE INDEX IN R2
4687 015520 126704 012466          CMPB  LINE,R4      ;IS THIS THE A.E. TEST LINE ??
4688 015524 001432          BEQ   5$           ;BRANCH IF YES.
4689 015526 036267 030136 011446          BIT   $LNSEL(R2),LINSEL
4690 015534 001737          BEQ   21$
4691
4692 015536 026203 036112          CMP   RBUF(R2),R3  ;RECVD DATA CORRECT ??
4693 015542 001447          BEQ   6$           ;BR IF IT WAS
4694
4695 015544 004767 011356          JSR   PC,SAPS      ;SAVE THE ERROR PSW
4696 015550 010467 163440          MOV   R4,$TMP5    ;SAVE THE LINE NUMBER
4697 015554 016204 036112          MOV   RBUF(R2),R4 ;SET UP S/B DATA
4698 015560 062702 036112          ADD  #RBUF,R2     ;SET UP S/B ADDRESS
4699 015564 012701 177703          MOV  #177703,R1  ;SET UP THE WAS ADDRESS
4700 015570 004767 006560          JSR  PC,SUER2A    ;GO SET UP ERROR INFO
4701 015574 004567 006774          JSR  R5,SUNUM    ;PUT LINE NO. IN MESSAGE
4702 015600 001214          $TMP5
4703 015602 032520          EM31+45
4704 015604 104031          ERROR  31          ;NON-ECHO DATA COMPARE ERROR
4705 015606 000167 177472          JMP   1$          ;GO TRY NEXT LINE
4706
4707
4708 015612 020367 163402          5$:  CMP   R3,$TMP7    ;CHAR ECHOED OK ??
4709 015616 001427          BEQ   7$          ;BR IF YES
4710
4711 015620 004767 011302          JSR  PC,SAPS      ;SAVE THE ERROR PSW
4712 015624 012702 001220          MOV  # $TMP7,R2  ;SAVE THE S/B ADDRESS
4713 015630 016704 163364          MOV  $TMP7,R4    ;SAVE THE S/B DATA
4714 015634 012701 177703          MOV  #177703,R1 ;SAVE THE WAS ADDRESS
4715 015640 004767 006510          JSR  PC,SUER2A    ;GO SET UP ERROR INFO
4716 015644 004567 006724          JSR  R5,SUNUM    ;GO SET UP LINE NO. IN MESSAGE

```

4717	015650	030212			LINE		
4718	015652	032520			EM31+45		
4719	015654	104031			ERROR	31	:AUTO ECHO LINE DATA ERROR
4720	015656	000167	177422		JMP	1\$	:GO TRY NEXT LINE
4721							
4722	015662	105262	036112	6\$:	INCB	RBUF(R2)	:GENERATE NEXT EXPECTED DATA ON THIS LINE -
4723	015666	001262			SNE	21\$	:BR IF ITS NOT BACK TO 000
4724	015670	046267	027410	011552	BIC	LINBIT(R2),LINACT	:INDICATE THIOS LINE DONE 256 BYTES
4725	015676	005767	011546	7\$:	TST	LINACT	:ALL LINES INACTIVE
4726	015702	001254			BNE	21\$	:BR IF NOT
4727	015704	042761	100000	000004	BIC	#BIT15,LPR(R1)	:TURN OFF THE A.E. BIT
4728	015712	105761	000017		TSTB	SSR+1(R1)	:SILO EMPTY ??
4729	015716	001002			SNE	8\$	:BR IF NOT
4730	015720	000167	177360		JMP	1\$	:GO TEST NEXT LINE
4731	015724	000167	177504	8\$:	JMP	21\$	:GO EMPTY IT

4732  
4733  
4734  
4735 015730 000004  
4736  
4737  
4738  
4739  
4740  
4741  
4742  
4743  
4744  
4745  
4746  
4747  
4748  
4749  
4750  
4751  
4752  
4753  
4754  
4755  
4756  
4757  
4758  
4759  
4760  
4761  
4762  
4763  
4764 015732 012767 015740 163150  
4765 015740 012711 004000  
4766 015744 012705 000020  
4767 015750 012702 027310  
4768 015754 012703 036052  
4769 015760 010261 000006  
4770 015764 012761 177777 000010  
4771 015772 012761 131403 000004  
4772 016000 005023  
4773 016002 062702 000002  
4774 016006 005211  
4775 016010 005305  
4776 016012 001362  
4777 016014 116767 163062 163164  
4778 016022 042767 177400 163156  
4779 016030 016767 011146 011412  
4780 016036 016761 011140 000012  
4781  
4782 016044 012767 000002 012166  
4783 016052 005067 012164  
4784 016056 005067 163130  
4785 016062 105711  
4786 016064 100410  
4787 016066 004767 010652

\*\*\*\*\*  
:TEST 51 AUTO ECHO TEST 3 - ALL SELECTED LINES  
\*\*\*\*\*  
TST51: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST IS IDENTICAL TO TEST 47 EXCEPT ALL SELECTED LINES  
ARE ACTIVATED CONCURRENTLY RATHER THAN ONE AT A TIME AND ONLY  
THE ALL 1'S DATA IS USED.

ERRORS:  
\*\*\*\*\*

- 1. [ERROR 36] IS CALLED TO REPORT "DATA AVAIL" TIMEOUTS
- 2. [ERROR 31] IS CALLED TO REPORT A.E. DATA ERRORS

SYNC: M7277 SH4 LOAD BAR LB+HB L CN2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

REFER TO TEST 47

KEY LOGIC:  
\*\*\*\*\*

REFER TO TEST 47

%  
15: MOV #15,SLPERR ;SET UP THE ERROR LOOP RETURN  
MOV #BIT11,(R1) ;CLEAR OUT THE DH11  
MOV #20,R5 ;INIT COUNTER TO SET UP 16. LINES  
MOV #AETAB,R2 ;SET UP POINTER TO AUTO ECHO TEST DATA  
MOV #RCNT,R3 ;R3 POINTS TO TABLE OF CHAR COUNTERS  
25: MOV R2,CAR(R1) ;SET UP BUS ADDRESS REG  
MOV #-1,BCR(R1) ;SET UP BYTE COUNT REG  
MOV #131403,LPR(R1) ;SET UP LINE PARAMETERS  
CLR (R3)+ ;CLEAR A COUNTER  
ADD #2,R2 ;UPDATE POINTERS  
INC (R1) ;SELECT NEXT LINE  
DEC R5 ;COUNT ONE DONE  
BNE 25 ;BR TILL 16. DONE  
MOVB \$TSTNM,\$TMP2 ;SAVE THE TEST NO.  
BIC #177400,\$TMP2  
MOV LINSSEL,LINACT ;SET FLAG TO INDICATE ALL 16. ACTIVE  
MOV LINSSEL,BAR(R1) ;ACTIVATE ALL XMITTERS  
35: MOV #2,TIMEA ;INIT TIMER A  
CLR TIMEB ;INIT TIMERB  
CLR \$TMP4  
TSTB (R1) ;CHAR AVAIL SET YET ?  
BMI 45 ;BR IF YES  
JSR PC,TIMEIT ;CALL THE TIMER

```

4798 016072 000771          BR      3$          :TIMER ROUTINE WILL MOVE RETURN PC
4799                                     :AROUND THIS BRANCH IF TIME OUT OCCURS
4791 016074 016167 000004 162100  MOV    LPR,R1), $TMP0  :SAVE THE "LPR" REG
4792 016102 104036          ERROR   36          :DATA AVAILABLE TIMEOUT
4793 016104 000465          BR      TST52        :;EXIT TEST ON ERROR
4795 016106 016103 000002          4$:  MOV    NRC(R1),R3      :GET THE WAS DATA
4796 016112 010302          MOV    R3,R2        :BUILD AND SAVE LINE NO.
4797 016114 000302          SWAB   R2
4798 016116 042702 177760          BIC    #177760,R2
4799 016122 010267 163070          MOV    R2,$TMP6     :SAVE THE LINE NO.
4800 016126 006302          ASL    R2           :GENERATE TABLE OFFSET
4801 016130 005267 163056          INC    $TMP4
4802 016134 022767 000101 163050  CMP    #101,$TMP4
4803 016142 001745          BEQ    3$
4804 016144 036267 03013E 011030  BIT    $LNSEL(R2),LNSEL ;IS THIS ONE C THE SELECTED LINES?
4805 016152 001755          BEQ    4$          :IF NOT, THIS IS GARBAGE, SO CHECK NEXT SILO ENTRY.
4806 016154 005262 036052          INC    RCNT(R2)     :COUNT THE CHARACTER
4807 016160 020362 027310          CMP    R3,AETAB(R2) :IS THE DATA CORRECT ??
4808 016164 001420          BEQ    5$          :BR IF YES
4809
4810 016166 004767 010734          JSR    PC,SAPS      :SAVE THE ERROR PSW
4811 016172 016204 027310          MOV    AETAB(R2),R4 :GET THE S/B DATA
4812 016176 062702 027310          ADD    #AETAB,R2    :GENERATE S/B ADDRESS
4813 016202 062701 000002          ADD    #NRC,R1     :GENERATE THE WAS ADDRESS
4814 016206 004767 006142          JSR    PC,SUER2A   :GO SET UP ERROR INFO
4815 016212 004567 006356          JSR    R5,SUNUM    :PUT LINE NO. IN MESSAGE
4816 016216 001216          $TMP6  EM31+45
4817 016220 032520          ERROR   31
4818 016222 104031          BR      TST52        :DATA COMPARE ERROR
4819 016224 000415          BR      TST52        :;EXIT TEST ON ERROR
4820
4821 016226 022762 000100 036052 5$:  CMP    #100,RCNT(R2) :DONE 64. CHARS ON THIS LINE ?
4822 016234 001310          BNE    3$          :BR IF NOT
4823 016236 016711 162754          MOV    $TMP6,(R1)   :SELECT LINE IN SCR REG
4824 016242 042761 100000 000004  BIC    #BIT15,LPR,R1 :TURN OFF A.E. BIT
4825 016250 046267 027410 011172  BIC    LINBIT(R2),LINACT :ALL LINES INACTIVE ??
4826 016256 001277          BNE    3$          :BR IF NOT

```



4827  
4828  
4829  
4830 016260 000004  
4831  
4832  
4833  
4834  
4835  
4836  
4837  
4838  
4839  
4840  
4841  
4842  
4843  
4844  
4845  
4846  
4847  
4848  
4849  
4850  
4851  
4852  
4853  
4854  
4855  
4856  
4857  
4858  
4859  
4860  
4861  
4862  
4863  
4864  
4865  
4866  
4867  
4868  
4869  
4870  
4871  
4872  
4873  
4874  
4875  
4876  
4877  
4878  
4879  
4880  
4881  
4882

::\*\*\*\*\*  
: TEST 52 BREAK BIT TEST - ALL SELECTED LINES  
:\*\*\*\*\*  
TST52: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT THE "BREAK" FEATURE WORKS PROPERLY FOR ALL SELECTED LINES. THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP THE ERROR LOOP RETURN
2. RETRIEVE THE CORRECT S/B DATA FROM THE "BREAK" DATA TABLE AND UPDATE THE POINTER.
3. GO SELECT A LINE TO TEST - GO TO TEST 52 IF DONE ALL SELECTED LINES
4. RESET THE DH11 AND CLEAR THE "CAR" AND "BCR" MEMORIES.
5. PRIME SELECTED LINE TO OUTPUT TWO "NULL" CHARS TO CLEAR UART
6. ACTIVATE THE SELECTED LINE
7. WAIT FOR SILO TO RECEIVE TWO NULLS - IF TIMEOUT REPORT ERROR AND RESTART AT STEP 2
8. IF NO TIMEOUT CLEAR THE SELECTED DH11 AND RESELECT LINE NO.
9. PRIME SELECTED LINE TO OUT PUT 256. CHARS.
10. SET THE SELECTED LINE'S BREAK BIT
11. ACTIVATE THE SELECTED LINE
12. WAIT FOR "BAR" REG TO CLEAR -F TIMEOUT REPORT ERROR AND RESTART AT STEP 2
13. IF NO TIMEOUT VERIFY THAT THE SILO RECEIVED ONLY ONE CHAR- IF NOT REPORT ERROR AND RESTART AT STEP 2
14. IF SILO RECEIVED ONLY ONE CHAR VERIFY THAT IT WAS A "BREAK" CHAR - IF NOT REPORT ERROR - AND RESTART AT STEP 2

ERRORS:  
\*\*\*\*\*

1. [ERROR 25] IS CALLED TO REPORT ALL ERRORS

SYNC: M7277 SH4 LOAD BCR H FU1  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. IF ALL LINES FAILED SUSPECT THAT THE M7277 IS NOT GENERATING THE BREAK CONTROL REG LOAD SIGNAL.
2. IF ONLY ONE LINE FAILS SL ECT THE BREAK CONTROL LOGIC ON THE M7278

KEY SIGNALS:  
\*\*\*\*\*

M7277 SH4 LOAD BCR H FU1

M7278 SH5 THRU SH8

74175 REGISTER CHIPS E51, E38, E67, E60

7400 DRIVERS E45, E46, E75, E76

4883										
4884										
4885										
4886	016262	012767	016342	162620		MOV	#2\$, \$LPERR		:SET UP ERROR LOOP RETURN	
4887	016270	012705	027512			MOV	#BRKTAB, R5		:SET UP POINTER TO BREAK DATA TABLE	
4888	016274	005067	010706			CLR	LMSK1		:INIT BIT TEST MASK	
4889	016300	000261				SEC			:SET BIT MARKER IN "C"	
4890	016302	000401				BR	12\$		:GO SHIFT MASK	
4891	016304	000241			1\$:	CLC			:INIT THE "C" BIT	
4892	016306	006167	010674		12\$:	ROL	LMSK1		:SHIFT TEST MARKER	
4893	016312	001411				BEQ	11\$		:BR IF ALL LINES DONE	
4894	016314	012504				MOV	(R5)+, R4		:GET TEST DATA FOR THIS LINE	
4895	016316	036767	010664	010656		BIT	LMSK1, LINSEL		:LINE SELECTED ?	
4896	016324	001767				BEQ	1\$		:BR IF NOT	
4897	016326	004767	006150			JSR	PC, SELINE		:GO SELECT A LINE TO TEST	
4898	016332	000401				BR	11\$		:BR IF DONE ALL SELECTED LINES	
4899	016334	000402				BR	2\$		:GO TEST THE SELECTED LINE	
4900	016336	000167	000454		11\$:	JMP	9\$		:GO EXIT TEST	
4901	016342	012711	004000		2\$:	MOV	#BIT11, (R1)		:CLEAR THE DH11	
4902	016346	004767	006302			JSR	PC, CLCABC		:GO CLR THE "CAR" AND "BCR" MEMORIES	
4903	016352	116711	011634			MOVB	LINE, (R1)		:SELECT THE LINE	
4904										
4905	016356	012761	030246	000006		MOV	#NULL, CAR(R1)		:SET UP TO OUTPUT TWO NULL CHARS	
4906	016364	012761	177776	000010		MOV	#-2, BCR(R1)		:SET BYTE COUNT TO 2	
4907	016372	012761	033503	000004		MOV	#33503, LPR(R1)		:SET UP LINE PARAMETERS	
4908	016400	016761	010600	000012		MOV	LINMSK, BAR(R1)		:ACTIVATE SELECTED LINE	
4909										
4910	016406	012767	000001	011624		MOV	#1, TIMEA		:INIT TIMER A	
4911	016414	005067	011622			CLR	TIMEB		:INIT TIMER B	
4912	016420	122761	000002	000017	3\$:	CMPE	#2, SSR+1(R1)		:TWO CHARS RECEIVED ??	
4913	016426	001432				BEQ	4\$		:BR IF YES	
4914	016430	004767	010310			JSR	PC, TIMEIT		:CALL THE TIMER	
4915	016434	000771				BR	3\$		:TIMER ROUTINE WILL MOVE RETURN PC	
4916									:AROUND THIS BRANCH IF TIME OUT OCCURS	
4917										
4918	016436	004767	010464			JSR	PC, SAPS		:SAVE THE ERROR PSW	
4919	016442	010467	162536			MOV	R4, \$TMP1		:SAVE S/B DATA	
4920	016446	010102				MOV	R1, R2		:SET UP REGADR	
4921	016450	062702	000016			ADD	#SSR, R2			
4922	016454	011203				MOV	(R2), R3		:GET THE WAS DATA	
4923	016456	042703	100377			BIC	#100377, R3		:CLEAR JUNK	
4924	016462	012704	000002			MOV	#2, R4		:SET UP S/B DATA	
4925	016466	000304				SWAB	R4			
4926	016470	004767	005660			JSR	PC, SUER2A		:GO SET UP ERROR INFO	
4927	016474	004567	006074			JSR	RS, SUNUM		:GO PUT LINE NO. IN MESSAGE	
4928	016500	030212				LINE				
4929	016502	032223				EM25+34				
4930	016504	016704	162474			MOV	\$TMP1, R4		:RESTORE S/B DATA	
4931	016510	104025				ERROR	2\$		:TIMED OUT WAITING FOR TWO NULLS	
4932	016512	000674				BR	1\$		:GO TRY NEXT LINE	
4933										
4934	016514	012711	004000		4\$:	MOV	#BIT11, (R1)		:CLEAR THE INTERFACE	
4935	016520	116711	011466			MOVB	LINE, (R1)		:SELECT THE LINE	
4936	016524	012761	037112	000006		MOV	#TBUF, CAR(R1)		:SET UP BUS ADDRESS REG FOR XMITTR	
4937	016532	012761	177400	000010		MOV	#-400, BCR(R1)		:SET BYTE COUNT TO XMIT 256(10) CHARS	
4938	016540	012761	033503	000004		MOV	#33503, LPR(R1)		:SET UP LINE PARAMETERS	

016546	016761	010432	000014		MOV	LINMSK, BAR(R1)	:SET BREAK BIT FOR ACTIVE LINE
016554	016761	010424	000012		MOV	LINMSK, BAR(R1)	:ACTIVATE - SELECTED LINE
016562	012767	010005	011450		MOV	R5, TIMEA	:INIT TIMER A
016570	012767	011446			MOV	R5, TIMEB	:INIT TIMER B
016578	012767	000012		58:	MOV	R1, R1	:BAR BIT CLEARED ?
016586	012767	010136			MOV	R1, R1	:BAR IFD YES
016594	012767				MOV	R1, R1	:CALL THE TIMER
016602	012767				MOV	R1, R1	:TIMER ROUTINE WILL MOVE RETURN PC
016610	012767				MOV	R1, R1	:ROUND THIS BRANCH IF TIME OUT OCCURS
016618	012767	010312			MOV	R1, R1	:SAVE THE ERROR PSW
016626	012767	162264			MOV	R1, R1	:SAVE THE S/B DATA
016634	012767	000012			MOV	R1, R1	:SET UP REGADR
016642	012767				MOV	R1, R1	:GET THE WAS DATA
016650	012767	005516			CLR	R4	:SET UP S/B DATA
016658	012767	005732			JSR	PC, SUER2A	:GO SET UP ERROR INFO
016666	012767				JSR	R5, SUNUM	:PUT LINE NO IN MESSAGE
016674	012767				LINE		
016682	012767				EM25+34		
016690	012767	162332			MOV	\$TMP1, R4	:RESTORE THE S/B DATA
016698	012767				ERROR	R5	:BAR BIT FAILED TO CLEAR
016706	012767				BR	15	:GO TRY NEXT LINE
016714	012767						
016722	012767			65:	CMPS	#1, SSR+1(R1)	:ONE CHAR RECEIVED ?
016730	012767				BEO	75	:BR IF YES
016738	012767						
016746	012767				JSR	PC, SAPS	:SAVE THE ERROR PSW
016754	012767	010234			MOV	R4, \$TMP1	:SAVE THE S/B DATA
016762	012767	162306			MOV	R1, R2	:SET UP REGADR
016770	012767				ADD	#SSR, R2	
016778	012767	000016			MOV	(R2), R3	:GET THE WAS DATA
016786	012767				BIC	#100377, R3	:CLEAR JUNK
016794	012767	100377			MOV	#1, R4	:SET UP S/B DATA
016802	012767	000001			SWAB	R4	
016810	012767				JSR	PC, SUER2A	:GO SET UP ERROR INFO
016818	012767	005430			JSR	R5, SUNUM	:GO PUT LINE NO. IN MESSAGE
016826	012767	005644			LINE		
016834	012767				EM25+34		
016842	012767				MOV	\$TMP1, R4	:RESTORE THE S/B DATA
016850	012767	162244			ERROR	R5	:FAILED TO RECEIVE THE ONE CHAR
016858	012767				JMP	15	:GO TRY NEXT LINE
016866	012767						
016874	012767			75:	MOV	NAC(R1), R3	:GET THE WAS DATA
016882	012767				MOV	R3, R4	:WAS IT A BREAK CHAR ?
016890	012767				BNE	95	:BR IF NOT CORRECT
016898	012767	177322			JMP	15	:GO TEST NEXT LINE
016906	012767						
016914	012767			85:	JSR	PC, SAPS	:SAVE THE ERROR PSW
016922	012767	010140			MOV	R1, R2	:SET UP REGADR
016930	012767				ADD	#NAC, R2	
016938	012767	000002			JSR	PC, SUER2A	:GO SET UP ERROR INFO
016946	012767	005354			JSR	R5, SUNUM	:PUT LINE NO IN MESSAGE
016954	012767	005570			LINE		



017020 000004

```

*****
:TEST 53 HALF DUPLEX TEST - ALL SELECTED LINES
*****
TST53: SCOPE
REM %
TEST ABSTRACT:
*****

```

THIS TEST VERIFIES THAT THE RECEIVERS ON ALL SELECTED LINES ARE "BLINDED" WHEN THE HALF-DUPLEX MODE IS ENABLED. THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP THE ERROR LOOP RETURN
2. GO SELECT A LINE NO. TO TEST
3. IF DONE ALL SELECTED LINES - GO TO TEST 53
4. RESET THE DH11 AND CLEAR THE "CAR" AND "BCR" MEMORIES
5. PRIME THE SELECTED DH11 TO XMIT 256. CHARS IN HALF-DUPLEX MODE.
6. ACTIVATE THE SELECTED LINE AND WAIT FOR THE "BAR" REG TO CLEAR
7. IF TIMEOUT - REPORT ERROR AND GO TO STEP 2
8. IF NO TIMEOUT VERIFY THE "CHAR AVAIL" DID NOT SET (RECEIVER BLINDED) - IF ERROR REPORT IT AND GO TO STEP 2 - IF NO ERROR GO TO STEP 2

ERRORS:  
\*\*\*\*\*

1. [ERROR 26] IS CALLED TO REPORT ALL ERRORS

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. SUSPECT EITHER THE M7289 OR THE M7288 MODULES

KEY LOGIC:  
\*\*\*\*\*

```

M7289 SH5 HALF DUPLEX <15:00> H SIGNALS
      SH5 END OF CHAR <15:00> SIGNALS

M7288 SH5 HALF DUPLEX <03:00> H SIGNALS
      SH7 " " <07:00> H SIGNALS
      SH9 " " <11:08> H SIGNALS
      SH11 " " <15:12> H SIGNALS

```

```

017022 012767 017036 162060
017030 004767 005446
017034 000477
017036 012711 004000
017042 004767 005606
017046 156711 011140
017052 012761 037112 000006

```

```

: MOV #25,SLPERR ;SET UP ERROR LOOP RETURN
15: JSR PC,SELIN
BR TST54 ;:BR IF ALL LINES TESTED
25: MOV #BIT11,(R1) ;:CLEAR THE INTERFACE
JSR PC,CLCABC ;:GO CLR THE "CAR" AND "BCR" MEMORIES
BISB LINE,(R1) ;:SELECT THE LINE
MOV #TBUF,CAR(R1) ;:POINT TO XMIT BUFFER

```

```

017160 012761 177400 000010 MOV #400,BCR(R1) :XMIT 256(10) CHARS
017161 012761 073503 000004 MOV #73503,LPR(R1) :SET UP THE LINE PARAMETERS
017164 012104 000012 MOV LINMSK,BAR(R1) :ACTIVATE THE SELECTED LINE

017165 012767 000001 01:130 MOV #1,TIMEA :INIT TIME A
017166 012767 000002 CLR TIMEB :INIT TIME B
35: 017167 012767 000003 TST BAR,R1 :WAIT FOR XMITTR TO FINISH
017168 012767 000004 BNE TIMEIT :BR IF XMITTR FINISHED
017169 012767 000005 BR 35 :CALL TIMER
:TIMER WILL MOVE RETURN PC AROUND
:THIS BRANCH IF TIMEOUT OCCURS

017170 012767 000006 JSR PC,SAPS :SAVE THE ERROR PSW
017171 012767 000007 MOV BAR(R1),R3 :GET THE WAS DATA
017172 012767 000008 MOV R1,R2 :SET UP REGADR
017173 012767 000009 ADD #BAR,R2
017174 012767 000010 CLR R4 :SET UP NEW S/B DATA
017175 012767 005200 JSR PC,SUER2A :GO SET UP THE ERROR INFO
017176 012767 005414 JSR RS,SUNUM :PUT LINE NO. IN MESSAGE
017177 012767 000011 LINE
017178 012767 000012 EM26+37
017179 012767 104026 ERROR 26 :BAR BIT FAILED TO CLEAR ON TIME
017180 012767 000013 BR 15 :GO TRY NEXT LINE

45: 017170 105711 TSTB (R1) :CHAR AVAIL SET ??
017172 100316 BPL 15 :BR IF NOT IT SHOULDN'T BE

017174 004767 007726 JSR PC,SAPS :SAVE THE ERROR PSW
017200 010102 MOV R1,R2 :SET UP REGADR
017202 011103 MOV (R1),R3 :GET WAS DATA
017204 042703 100000 BIC #BIT15,R3 :CLEAR JUNK BIT
017210 116704 010776 MOV# LINE,R4 :SET UP S/B DATA
017214 004767 005134 JSR PC,SUER2A :GO SETUP ERROR INFO
017220 004767 005350 JSR RS,SUNUM :PUT LINE NO. IN MSG
017226 030212 LINE
017232 032266 EM26+37
017238 104026 ERROR 26 :HALF DUPLEX FAILED TO BLIND RECVR
017244 000013 BR 15 :GO SELECT NEXT LINE

```

017234 000004  
017235 000004  
017236 000004  
017237 000004  
017238 000004  
017239 000004  
017240 000004  
017241 000004  
017242 000004  
017243 000004  
017244 000004  
017245 000004  
017246 000004  
017247 000004  
017248 000004  
017249 000004  
017250 000004  
017251 000004  
017252 000004  
017253 000004  
017254 000004  
017255 000004  
017256 000004  
017257 000004  
017258 000004  
017259 000004  
017260 000004  
017261 000004  
017262 000004  
017263 000004  
017264 000004  
017265 000004  
017266 000004  
017267 000004  
017268 000004  
017269 000004  
017270 000004  
017271 000004  
017272 000004  
017273 000004  
017274 000004  
017275 000004  
017276 000004  
017277 000004  
017278 000004  
017279 000004  
017280 000004  
017281 000004  
017282 000004  
017283 000004  
017284 000004  
017285 000004  
017286 000004  
017287 000004  
017288 000004  
017289 000004  
017290 000004  
017291 000004  
017292 000004  
017293 000004  
017294 000004  
017295 000004  
017296 000004  
017297 000004  
017298 000004  
017299 000004  
017300 000004

\*\*\*\*\*  
:TEST 54 VERIFY THAT OVERRUN CAN SET PROPERLY - ALL SELECTED LINES  
\*\*\*\*\*

TEST54: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT "OVERRUN" SETS PROPERLY FOR ALL LINES  
THAT ARE SELECTED FOR TEST WHEN THE OVERRUN CONDITION IS FORCED BY THE  
PROGRAM. THE TEST SEQUENCE IS AS FOLLOWS:

1. SET UP THE ERROR LOOP RETURN
2. SELECT A LINE NO. TO TEST - IF DONE ALL LINES GO TO  
END OF PASS HANDLER.
3. PRIME THE SELECTED LINE TO XMIT 68. CHARS
4. ACTIVATE THE SELECTED LINE
5. WAIT FOR "XMIT DONE" TO SET - IF TIMEOUT REPORT ERROR  
AND RESTART AT STEP 2
6. IF NO TIMEOUT READ 65. CHARS FROM THE SILO AND VERIFY THAT  
"OVERRUN" IS SET ON THE LAST WORD READ
7. IF NOT REPORT ERROR AND RESTART AT STEP 2

ERRORS:  
\*\*\*\*\*

1. [ERROR 50] IS CALLED TO REPORT "XMIT DONE " TIMEOUTS
2. [ERROR 56] IS CALLED TO REPORT "OVERRUN" ERROR

SYNC: M7277 SH3 INIT A H EF2  
\*\*\*\*\*

DEBUG:  
\*\*\*\*\*

1. IF FAULT APPEARS ON ONLY ONE LINE SUSPECT UART MODULE  
FOR THE APPROPRIATE LINE IN QUESTION.
2. IF FAULT APPEARS ON ALL LINES SUSPECT THE M7279 MODULE

KEY LOGIC:  
\*\*\*\*\*

M7279	SH1	MASTER OR H	E12-9
	SH2	MEMORY CHIP (3341)	E13-11
M7280	SH2	UC1 OR 2 MASTER OR	EN2
	SH2-5	UART PIN 15 (BLF OR LINE NN)	

%

017236	012767	017252	161644	MOV	#25, \$LPERR	:SET UP ERROR LOOP RETURN
017244	004767	005232		15: JSR	PC SELINE	:GO SELECT A LINE # TO TEST
017250	000512			BR	TEST5	:BR IF DONE ALL SELECTED LINES
017252	012711	004000		25: MOV	#BIT11, (R1)	:CLEAR OUT THE DH11
017256	116711	010730		MOV8	LINE, (R1)	:SELECT THE LINE TO TEST

# G03

MAXNDEC-11-02DMM-8  
02DMMB.P11 T54

MACY11 27(732) 23-SEP-76 14:33 PAGE 121  
VERIFY THAT OVERRUN CAN SET PROPERLY - ALL SELECTED LINES

SEQ 0239

150	0173262	012761	037112	000006		MOV	#TBUF,CAR(R1)	;SET UP CURRENT ADDRESS
151	0173270	012761	177674	000010		MOV	#-68,BCR(R1)	;SET UP BYTE COUNT REG
152	0173276	012761	033503	000004		MOV	#33503,LPR(R1)	;DO IT AT 9600 BAUD - 8 BITS
153	0173274	016761	007674	000012		MOV	LINMSK,BAR(R1)	;ACTIVATE THE SELECTED LINE
154								
155	017312	012767	000001	010720		MOV	#1,TIMEA	;INIT TIMERS A AND B
156	0173270	005067	010716			CLR	TIMEB	
157	0173274	005711			3\$:	TST	(R1)	;TRANSMITTER DONE ??
158	0173266	100425				BMI	4\$	;BR IF YES
159	0173300	004767	007410			JSR	PC,TIMEIT	;CALL TIMER
160	017334	000773				BR	3\$	;BR IF NO TIMEOUT
161								
162	017336	004767	007564			JSR	PC,SAPS	;GO SAVE PSW
163	017342	011103				MOV	(R1),R3	;GET THE WAS DATA
164	017344	042703	077760			BIC	#77760,R3	;CLEAR UNINTERESTING BITS
165	017350	116704	010636			MOV	LINE,R4	;SET UP S/B DATA
166	017354	052704	100000			BIS	#BIT15,R4	
167	017360	010102				MOV	R1,R2	;SET UP REGADR
168	017362	004767	004766			JSR	PC,SUER2A	;GO SET UP ERROR INFO
169	017366	004567	005202			JSR	R5,SUNUM	;PUT LINE NO. IN MESSAGE HEADER
170	017372	030212				LINE		
171	017374	034144				EM50+53		
172	017376	104050				ERROR	50	;REPORT XMIT DONE TIME OUT
173	017400	000721				BR	1\$	;GO TRY NEXT LINE
174								
175	017402	012767	000101	161574	4\$:	MOV	#65,\$TMP1	;SET UP TO READ 65. WORDS FROM SILO
176	017410	116704	010576			MOV	LINE,R4	;SET UP S/B DATA
177	017414	000304				SWAB	R4	
178	017416	152704	000101			BISB	#65,R4	
179	017422	052704	140000			BIS	#BIT15+BIT14,R4	;PUT IN OVERRUN AND VALID DATA BITS
180	017426	016103	000002		5\$:	MOV	NRC(R1),R3	;GET WAS DATA FROM SILO
181	017432	005367	161546			DEC	\$TMP1	;COUNT ONE WORD READ
182	017436	001373				BNE	5\$	;BR TIL 65. READ
183	017440	020304				CMP	R3,R4	;WAS DATA AND OVERRUN CORRECT ??
184	017442	001700				BEQ	1\$	;BR IF YES TRY NEXT SELECTED LINE
185								
186	017444	004767	007456			JSR	PC,SAPS	;GO SAVE PSW
187	017450	010102				MOV	R1,R2	;SET UP REGADR
188	017452	062702	000002			ADD	#NRC,R2	
189	017456	004767	004672			JSR	PC,SUER2A	;GO SET UP ERROR INFO
190	017462	004567	005106			JSR	R5,SUNUM	;GO PUT LINE NO. IN MSG HDR
191	017466	030212				LINE		
192	017470	034562				EM56+42		
193	017472	104056				ERROR	56	;OVERRUN OR DATA INCORRECT
194	017474	000663				BR	1\$	;GO TEST NEXT SELECTED LINE
195								





017566	020103		CMP	R1,R3	:IF LINE NUMBER=SELECTED LINE NUMBER,
017570	001002		BNE	MUX11C	:EXCEPT LINE ENABLE FUNCTION FLIP FLOP
017672	012705	000001	MOV	#LINENA,R5	
017676	020504		MUX11C: CMP	R5,R4	:TO BE SET
017700	001403		BEQ	MUX11D	:COMPARE EXPECTED AND RECEIVED
017702	104401		TYPE		:RESULTS
017704	035755		MSG4		:ERROR
017706	000000		HALT		
017710	052777	000400 010262	MUX11D: BIS	#STEP,JDHMCSR	:EXAMINE NEXT LINE
017716	005302		DEC	R2	
017720	001353		BNE	MUX11B	
017722	005005		CLR	R5	
017724	010177	010250	MUX11E: MOV	R1,JDHMCSR	
017730	010103		MOV	R1,R3	:SET LINE COUNTER TO SELECTED LINE
017732	005077	010244	CLR	JDHMLSR	:CLEAR LINE ENABLE FLIP FLOP
017736	105227	000000	INCB	#0	:DELAY FOR CABLE
017742	001375		BNE	.-4	:DITTO
017744	017704	010232	MOV	JDHMLSR,R4	:READ LINE STATUS REGISTER
017750	005704		TST	R4	:WAS LINE ENABLE FUNCTION FLIP FLOP
017752	001710		BEQ	DOIT11	:CLEARED
017754	104401		TYPE		
017756	035755		MSG4		:ERROR
017760	000000		HALT		

5278  
5279  
5280  
5281  
5282  
5283  
5284  
5285  
5286  
5287  
5288  
5289  
5290  
5291  
5292  
5293  
5294  
5295  
5296  
5297  
5298  
5299  
5300  
5301  
5302  
5303  
5304  
5305  
5306  
5307  
5308  
5309  
5310  
5311  
5312  
5313  
5314  
5315  
5316  
5317  
5318  
5319  
5320  
5321  
5322  
5323  
5324  
5325  
5326  
5327  
5328  
5329  
5330  
5331  
5332

017762 000004

\*\*\*\*\*  
\*TEST 56 DM11-BB DIAGNOSTIC CONTINUED  
\*\*\*\*\*  
\*ST56: SCOPE  
.REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT CLEAR TO SEND AND CARRIER ARE SET  
IF "LINE ENABLE" AND TERMINAL ARE SET FOR THE SELECTED LINE.

ERRORS:  
\*\*\*\*\*

IF ANY ERRORS OCCUR, RUN THE DM11-BB MODEM CONTROL DIAGNOSTIC.  
DZDHK.

017764 005077 010212  
017770 004767 004506  
017774 000467  
017776 005077 010176  
020002 042767 000340 157766  
020010 116701 010176  
020014 012702 000020  
020020 010177 010154  
020024 012777 000003 C10150  
020032 005077 010142  
020036 005005  
020040 017704 010136  
020044 117703 010130  
020050 042703 177760  
020054 020103  
020056 001002  
020060 012705 000143  
020064 020405  
020066 001403  
020070 104401  
020072 035755  
020074 000000  
020076 052777 000400 010074  
020104 005302  
020106 001353  
020110 012705 000001  
020114 010103  
020116 010177 010056  
020122 042777 000002 010052  
020130 105227 000000  
020134 001375  
020136 017704 010040  
020142 020504  
020144 001707  
020146 104401  
020150 035755  
020152 000000

%  
DOIT15: CLR @DHMLSR ; CLEAR LINE STATUS REGISTER  
JSR PC, SELINE ; GO SELECT A LINE.  
BR TS157 ; BR IF DONE ALL SELECTED LINES  
MUX15: CLR @DHMCSR ; CLEAR CONTROL REGISTER  
BIC #340, PS ; ENABLE INTERRUPTS  
MOV LINE, R1  
MUX15A: MOV #16, R2 ; 16 LINES  
MOV R1, @DHMCSR ; SELECT A LINE  
MOV #LINENA+TRMRDY, @DHMLSR ; SET LINE ENABLE +TRMRDY  
CLR @DHMCSR ; CLEAR CONTROL REGISTER  
MUX15B: CLR R5 ; CLEAR EXPECTED RESULT  
MOV @DHMLSR, R4 ; READ LINE STATUS  
MOVB @DHMCSR, R3 ; READ LINE NUMBER  
BIC #177760, R3 ; CLEAR UNWANTED BITS  
CMP R1, R3 ; IF RECEIVED LINE=SELECTED LINE  
BNE MUX15C ; EXPECT LINE ENABLE AND  
MOV #LINENA+TRMRDY+CC+CS, R5  
MUX15C: CMP R4, R5 ; CLEAR TO SEND AND CARRIER ARE SET  
BEQ MUX15D ; COMPARE EXPECTED AND  
TYPE MSG4 ; RECEIVED RESULTS  
MSG4  
HALT ; ERROR.  
MUX15D: BIS #STEP, @DHMCSR ; UPDATE LINE COUNTER  
DEC R2 ; CONTINUE IF ALL CHECKS  
BNE MUX15E ; ARE NOT DONE FOR THIS LINE  
MOV #LINENA, R5 ; EXPECT LINE ENABLE  
MUX15E: MOV R1, R3 ; ON SELECTED LINE  
MOV R1, @DHMCSR ; SELECT LINE  
BIC #TRMRDY, @DHMLSR ; CLEAR TERMINAL  
INCB #0 ; DELAY FOR CABLE  
BNE -4 ; DITTO  
MOV @DHMLSR, R4 ; READ LINE STATUS REGISTER  
CMP R5, R4 ; ONLY LINE ENABLE SHOULD BE  
BEQ DOIT15 ; SET ON THIS LINE  
TYPE MSG4  
MSG4  
HALT ; ERROR.

K03

MAINDEC-11-DZDM-B  
DZDMB.P11 T56

MACY11 27(732) 23-SEP-76 14:33 PAGE 125  
DM11-98 DIAGNOSTIC CONTINUED

SEC 0243

5334  
5335

5336  
5337  
5338  
5339  
5340  
5341  
5342  
5343  
5344  
5345  
5346  
5347  
5348  
5349  
5350  
5351  
5352  
5353  
5354  
5355  
5356  
5357  
5358  
5359  
5360  
5361  
5362  
5363  
5364  
5365  
5366  
5367  
5368  
5369  
5370  
5371  
5372  
5373  
5374  
5375  
5376  
5377  
5378  
5379  
5380  
5381  
5382  
5383  
5384  
5385  
5386  
5387  
5388  
5389  
5390  
5391

02C154 000004

\*\*\*\*\*  
\*TEST 57 DM11-BB DIAGNOSTIC CONTINUED  
\*\*\*\*\*  
TST57: SCOPE  
REM %  
TEST ABSTRACT:  
\*\*\*\*\*

THIS TEST VERIFIES THAT RING IS SET IF "LINE ENABLE" AND  
REQUEST TO SEND ARE SET FOR THE SELECTED LINE.

ERRORS:  
\*\*\*\*\*

IF ANY ERRORS OCCUR, RUN THE DM11-BB MODEM CONTROL DIAGNOSTIC,  
DZDMM.

%  
DOIT16: CLR @DHMLSR ;CLEAR LINE STATUS REGISTER  
JSR PC, SELINE ;GO SELECT A LINE.  
BR TST60 ;;BR IF DONE ALL SELECTED LINES  
MUX16: CLR @DHMCSR ;CLEAR CONTROL REGISTER  
BIC #340, PS ;ENABLE INTERRUPTS  
MOVB LINE, R1  
MUX16A: MOV #16, R2 ;16 LINES  
MOV R1, @DHMCSR ;SELECT A LINE  
MOV #LINENA+RS, @DHMLSR ;SET LINE ENABLE +RS  
CLR @DHMCSR ;CLEAR CONTROL REGISTER  
MUX16B: CLR R5 ;CLEAR EXPECTED RESULT  
MOV @DHMLSR, R4 ;READ LINE STATUS  
MOVB @DHMCSR, R3 ;READ LINE NUMBER  
BIC #177760, R3 ;CLEAR UNWANTED BITS  
CMP R1, R3 ;IF RECEIVED LINE=SELECTED LINE  
BNE MUX16C ;EXPECT LINE ENABLE AND  
MOV #LINENA+RS+RING, R5 ;RING IS SET  
MUX16C: CMP R4, R5 ;COMPARE EXPECTED AND  
BEQ MUX16D ;RECEIVED RESULTS  
TYPE MSG4 ;ERROR  
MUX16D: BIS #STEP, @DHMCSR ;UPDATE LINE COUNTER  
DEC R2 ;CONTINUE IF ALL CHECKS  
BNE MUX16E ;ARE NOT DONE FOR THIS LINE  
MOV #LINENA, R5 ;EXPECT LINE ENABLE  
MUX16E: MOV R1, R3 ;ON SELECTED LINE  
MOV R1, @DHMCSR ;SELECT LINE  
BIC #RS, @DHMLSR ;CLEAR REQUEST TO SEND  
INCB #0 ;DELAY FOR CABLE  
BNE .-4 ;DITTO  
MOV @DHMLSR, R4 ;READ LINE STATUS REGISTER  
CMP R5, R4 ;ONLY LINE ENABLE SHOULD BE  
BEQ DOIT16 ;SET ON THIS LINE  
TYPE MSG4 ;ERROR  
HALT

157574

007756

000400 007702

007660

007646

MAINDEC-11-DZDMM-B  
DZDMMB.P11 T57

MACY11 27(732) 23-SEP-76 14:33 PAGE 127  
DM11-BB DIAGNOSTIC CONTINUED

M03

SEQ 0245

5392  
5393

```

5394
5395
5396
5397 020346 000004
5398
5399
5400
5401
5402
5403
5404
5405
5406
5407
5408
5409
5410
5411
5412 020350 005077 007626
5413 020354 004767 004122
5414 020360 000467
5415 020362 005077 007612
5416 020366 042767 000340 157402
5417 020374 116701 007612
5418 020400 012702 000020
5419 020404 010177 007570
5420 020410 012777 000011 007564
5421 020416 005077 007556
5422 020422 005005
5423 020424 017704 007552
5424 020430 117703 007544
5425 020434 042703 177760
5426 020440 020103
5427 020442 001002
5428 020444 012705 000031
5429
5430 020450 020405
5431 020452 001403
5432 020454 104401
5433 020456 035755
5434 020460 000000
5435 020462 052777 000430 007510
5436 020470 005302
5437 020472 001353
5438 020474 012705 000001
5439 020500 010103
5440 020502 010177 007472
5441 020506 042777 000010 007466
5442 020514 105227 000000
5443 020520 001375
5444 020522 017704 007454
5445 020526 020504
5446 020530 001707
5447 020532 104401
5448 020534 035755
5449 020536 000000

```

```

:*****
:*TEST 60 DM11-BB DIAGNOSTIC CONTINUED
:*****
†ST60: SCOPE
.REM %
TEST ABSTRACT:
*****

```

THIS TEST VERIFIES THAT SECONDARY RECEIVE IS SET IF "LINE ENABLE" AND SECONDARY TRANSMIT ARE SET FOR THE SELECTED LINE.

ERRORS:  
\*\*\*\*\*

IF ANY ERRORS OCCUR, RUN THE DM11-BB MODEM CONTROL DIAGNOSTIC.  
DZDHK.

```

%
DOIT17: CLR @DHMLSR ;CLEAR LINE STATUS REGISTER.
JSR PC,SELINE ;GO SELECT A LINE.
BR ENDA
MUX17: CLR @DHMCSR ;CLEAR CONTROL REGISTER
BIC #340,PS ;ENABLE INTERRUPTS
MOVB LINE,R1
MUX17A: MOV #16,R2 ;16 LINES
MOV R1,@DHMCSR ;SELECT A LINE
MOV #LINENA+SECTX,@DHMLSR ;SET LINE ENABLE +SECTX
CLR @DHMCSR ;CLEAR CONTROL REGISTER
MUX17B: CLR R5 ;CLEAR EXPECTED RESULT
MOV @DHMLSR,R4 ;READ LINE STATUS
MOVB @DHMCSR,R3 ;READ LINE NUMBER
BIC #177760,R3 ;CLEAR UNWANTED BITS
CMP R1,R3 ;IF RECEIVED LINE=SELECTED LINE
BNE MUX17C ;EXPECT LINE ENABLE AND
MOV #LINENA+SECTX+SECRX,R5 ;SECONDARY RECEIVE IS SET
MUX17C: CMP R4,R5 ;COMPARE EXPECTED AND
BEQ MUX17D ;RECEIVED RESULTS
TYPE MSG4
HALT
MUX17D: BIS #STEP,@DHMCSR ;UPDATE LINE COUNTER
DEC R2 ;CONTINUE IF ALL CHECKS
BNE MUX17B ;ARE NOT DONE FOR THIS LINE
MOV #LINENA,R5 ;EXPECT LINE ENABLE
MUX17E: MOV R1,R3 ;ON SELECTED LINE
MOV R1,@DHMCSR ;SELECT LINE
BIC #SECTX,@DHMLSR ;CLEAR SECONDARY TRANSMIT
INCB #0 ;DELAY FOR CABLE
BNE #-4 ;DITTO
MOV @DHMLSR,R4 ;READ LINE STATUS REGISTER
CMP R5,R4 ;ONLY LINE ENABLE SHOULD BE
BEQ DOIT17 ;SET ON THIS LINE
TYPE MSG4
HALT

```







0211202	011667	157702
0211203	005067	160012
0211204	112767	000001 157575
0211205	016777	157656 157714
0211206	016776	157654
0211207	000002	
0211208	000010	

```

MOV (SP), $LPERR      ;; SAVE ERROR LOOP ADDRESS
CLR $ESCAPE           ;; CLEAR THE ESCAPE FROM ERROR ADDRESS
MOV B, #1, $SERMAX    ;; ONLY ALLOW ONE(1) ERROR ON NEXT TEST
$OVER: MOV $STNM, $DISPLAY ;; DISPLAY TEST NUMBER
MOV $LPADR, (SP)      ;; FUDGE RETURN ADDRESS
RTI                   ;; FIXES PS
SMXCNT: 10            ;; MAX. NUMBER OF ITERATIONS
.SBTTL ERROR HANDLER ROUTINE

```

```

*****
*THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT,
*SAVE THE ERROR ITEM NUMBER AND THE ADDRESS OF THE ERROR CALL
*AND GO TO $ERRTYP ON ERROR
*THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
*SW15=1      HALT ON ERROR
*SW13=1      INHIBIT ERROR TYPEOUTS
*SW09=1      LOOP ON ERROR
*CALL
*          ERROR      N      ;; ERROR=EMT AND N=ERROR ITEM NUMBER

```

0211236	104407	
0211238	105267	157637
0211240	001777	
0211242	016777	157630 157666
0211244	005267	157632
0211246	011667	157632
0211248	000002	157624
0211250	117767	157620 157614
0211252	032777	020000 157632
0211254	001004	
0211256	004767	000106
0211258	104401	001227
0211320	122767	000001 157724
0211322	001007	
0211324	116767	157560 000004
0211326	004767	001166
0211328	000	
0211330	000	
0211332	000777	
0211334	005777	157566
0211336	100002	
0211338	000000	
0211340	104407	
0211342	032777	001000 157552
0211344	001402	
0211346	016716	157514
0211348	005767	157624
0211350	001402	
0211352	016716	157616
0211406	022737	020712 000042
0211408	001001	
0211410	000000	

```

$ERRCR:
7$: CKSWR           ;; TEST FOR CHANGE IN SOFT-SWR
INCB $ERFLG        ;; SET THE ERROR FLAG
BEQ 7$             ;; DON'T LET THE FLAG GO TO ZERO
MOV $STNM, $DISPLAY ;; DISPLAY TEST NUMBER AND ERROR FLAG
INC $ERTTL         ;; INC THE ERROR COUNT
MOV (SP), $ERRPC   ;; GET ADDRESS OF ERROR INSTRUCTION
SUB #2, $ERRPC
MOV B, $SERAPC
MOV B, $SERAPC, $ITEMB ;; STRIP AND SAVE THE ERROR ITEM CODE
BIT #BIT13, $SWR    ;; SKIP TYPEOUT IF SET
BNE 20$            ;; SKIP TYPEOUTS
JSR PC, $ERRTYP    ;; GO TO USER ERROR ROUTINE
TYPE $SRLF

20$: CMPB #APTENV, $ENV ;; RUNNING IN APT MODE
BNE 2$            ;; NO SKIP APT ERROR REPORT
MOV B, $ITEMB, 21$ ;; SET ITEM NUMBER AS ERROR NUMBER
JSR PC, $SATY4    ;; REPORT FATAL ERROR TO APT

21$: .BYTE 0
.BYTE 0

22$: BR 22$        ;; APT ERROR LOOP
2$: TST $SWR      ;; HALT ON ERROR
BPL 3$           ;; SKIP IF CONTINUE
HALT             ;; HALT ON ERROR!
CKSWR           ;; TEST FOR CHANGE IN SOFT-SWR
BIT #BIT09, $SWR ;; LOOP ON ERROR SWITCH SET?
BEQ 4$          ;; BR IF NO
MOV $LPERR, (SP) ;; FUDGE RETURN FOR LOOPING
TST $ESCAPE     ;; CHECK FOR AN ESCAPE ADDRESS
BEQ 5$          ;; BR IF NONE
MOV $ESCAPE, (SP) ;; FUDGE RETURN ADDRESS FOR ESCAPE

5$: CMP #SENDAC, 2#42 ;; ACT-11 AUTO-ACCEPT?
BNE 6$          ;; BRANCH IF NO
HALT            ;; YES

6$:

```

```

021420 000002
021420 010046
021420 005000
021420 153700
021420 001004
021440 016746 157452
021444 104402
021446 000426
021450 005300
021452 006300
021454 006300
021456 006300
021460 062700 001356
021464 012067 000004
021470 001404
021472 004401
021474 000000
021476 104401 001227
021478 012067 000004
021480 001404
021482 004401
021484 000000
021486 104401 001227
021488 011000
021490 001004
021492 012600
021494 104401 001227
021496 000207
021500 013046
021502 104402
021504 005710
021506 001770
021508 104401 021552
021510 000771
021512 020040 000
021514 021556

```

```

R11 ;:RETURN
.SBTTL ERROR MESSAGE TYPEOUT ROUTINE

;*****
;THIS ROUTINE USES THE "ITEM CONTROL BYTE" ($ITEMB) TO DETERMINE WHICH
;ERROR IS TO BE REPORTED. IT THEN OBTAINS FROM THE "ERROR TABLE" $ERRTB.
;AND REPORTS THE APPROPRIATE INFORMATION CONCERNING THE ERROR.
;*****

$ERRTYP:
TYPE .SCLF ;:"CARRIAGE RETURN" & "LINE FEED"
MOV RO,-(SP) ;:SAVE RO
CLR RO ;:PICKUP THE ITEM INDEX
BISB $ITEMB,RO
BNE IS ;:IF ITEM NUMBER IS ZERO, JUST
;:TYPE THE PC OF THE ERROR
MOV $ERRPC,-(SP) ;:SAVE $ERRPC FOR TYPEOUT
;:ERROR ADDRESS
TYPOC ;:GO TYPE--OCTAL ASCII(ALL DIGITS)
BR 6$ ;:GET OUT
IS: DEC RO ;:ADJUST THE INDEX SO THAT IT WILL
ASL RO ;:WORK FOR THE ERROR TABLE
ASL RO
ASL RO
ADD $ERRTB,RO ;:FORM TABLE POINTER
MOV (RO)+,2$ ;:PICKUP "ERROR MESSAGE" POINTER
BEQ 3$ ;:SKIP TYPEOUT IF NO POINTER
TYPE "ERROR MESSAGE" ;:TYPE THE "ERROR MESSAGE"
;:"ERROR MESSAGE" POINTER GOES HERE
.SCLF ;:"CARRIAGE RETURN" & "LINE FEED"
MOV (RO)+,4$ ;:PICKUP "DATA HEADER" POINTER
BEQ 5$ ;:SKIP TYPEOUT IF 0
TYPE "DATA HEADER" ;:TYPE THE "DATA HEADER"
;:"DATA HEADER" POINTER GOES HERE
.SCLF ;:"CARRIAGE RETURN" & "LINE FEED"
MOV (RO),RO ;:PICKUP "DATA TABLE" POINTER
BNE 7$ ;:GO TYPE THE DATA
MOV (SP)+,RO ;:RESTORE RO
TYPE .SCLF ;:"CARRIAGE RETURN" & "LINE FEED"
RTS PC ;:RETURN
7$: MOV 2(RO)+,-(SP) ;:SAVE 2(RO)+ FOR TYPEOUT
TYPOC ;:GO TYPE--OCTAL ASCII(ALL DIGITS)
TST (RO) ;:IS THERE ANOTHER NUMBER?
BEQ 6$ ;:BR IF NO
TYPE 2$ ;:TYPE TWO(2) SPACES
BR 7$ ;:LOOP
8$: .ASCIZ / / ;:TWO(2) SPACES
.EVEN
.SBTTL BINARY TO OCTAL (ASCII) AND TYPE

;*****
;THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 6-DIGIT
;OCTAL (ASCII) NUMBER AND TYPE IT.
;$TYPOS---ENTER HERE TO SETUP SUPPRESS ZEROS AND NUMBER OF DIGITS TO TYPE
;CALL:
;* MOV NUM,-(SP) ;:NUMBER TO BE TYPED

```

```

*          TYPOS          ::CALL FOR TYPEOUT
*          .BYTE N        ::N=1 TO 6 FOR NUMBER OF DIGITS TO TYPE
*          .BYTE M        ::M=1 OR 0
*                               ::1=TYPE LEADING ZEROS
*                               ::0=SUPPRESS LEADING ZEROS
*STYPCN----ENTER HERE TO TYPE OUT WITH THE SAME PARAMETERS AS THE LAST
*STYPOS OR STYPC
*CALL:
*      MOV      NUM,-(SP)    ::NUMBER TO BE TYPED
*      TYPON    ::CALL FOR TYPEOUT
*STYPC----ENTER HERE FOR TYPEOUT OF A 16 BIT NUMBER
*CALL:
*      MOV      NUM,-(SP)    ::NUMBER TO BE TYPED
*      TYPC    ::CALL FOR TYPEOUT
*
*STYPOS: MOV      2(SP),-(SP)  ::PICKUP THE MODE
*        MOVB   1(SP),%ZFILL  ::LOAD ZERO FILL SWITCH
*        MOVB   (SP)+,%MODE+1  ::NUMBER OF DIGITS TO TYPE
*        ADD    #2,(SP)       ::ADJUST RETURN ADDRESS
*        BR     STYPCN
*STYPC:  MOVB   #1,%ZFILL     ::SET THE ZERO FILL SWITCH
*        MOVB   #6,%MODE+1    ::SET FOR SIX(6) DIGITS
*        MOVB   #5,%CNT       ::SET THE ITERATION COUNT
*        MOV    R3,-(SP)      ::SAVE R3
*        MOV    R4,-(SP)      ::SAVE R4
*        MOV    R5,-(SP)      ::SAVE R5
*        MOVB   %MODE+1,R4    ::GET THE NUMBER OF DIGITS TO TYPE
*        NEG    R4
*        ADD    #6,R4         ::SUBTRACT IT FOR MAX. ALLOWED
*        MOVB   R4,%MODE      ::SAVE IT FOR USE
*        MOVB   %ZFILL,R4     ::GET THE ZERO FILL SWITCH
*        MOV    12(SP),R5     ::PICKUP THE INPUT NUMBER
*        CLR    R3           ::CLEAR THE OUTPUT WORD
*1$:     ROL    R5           ::ROTATE MSB INTO "C"
*        BR    3$           ::GO DO MSB
*2$:     ROL    R5           ::FORM THIS DIGIT
*        BR    3$
*3$:     ROL    R3           ::GET LSB OF THIS DIGIT
*        DECB  %MODE         ::TYPE THIS DIGIT?
*        BPL   7$           ::BR IF NO
*        BIC   #177770,R3    ::GET RID OF JUNK
*        BNE   4$           ::TEST FOR 0
*        TST   R4           ::SUPPRESS THIS 0?
*        BEQ   5$           ::BR IF YES
*4$:     INC    R4           ::DON'T SUPPRESS ANYMORE 0'S
*        BIS   #'0,R3       ::MAKE THIS DIGIT ASCII
*5$:     BIS   #' ,R3       ::MAKE ASCII IF NOT ALREADY
*        MOVB  R3,%R5       ::SAVE FOR TYPING
*        TYPE  %R5         ::GO TYPE THIS DIGIT
*7$:     DECB  %CNT         ::COUNT BY 1
*        BGT   2$         ::BR IF MORE TO DO
*        BLT   6$         ::BR IF DONE

```

```

021556 017646 000000
021558 116667 000001 000211
021560 112667 000207
021562 062716 000002
021600 000406
021602 112767 000001 000171
021610 112767 000006 000165
021616 112767 000005 000154
021624 010346
021626 010446
021630 010546
021632 116704 000145
021636 005404
021640 062704 000006
021644 110467 000132
021650 116704 000125
021654 016605 000012
021660 005003
021662 006105 1$:
021664 000404 2$:
021666 006105 2$:
021670 006105
021672 006105
021674 010503 3$:
021676 006103 3$:
021700 105367 000076
021704 100016
021706 042703 177770
021712 001002
021714 005704
021716 001403
021720 005204 4$:
021722 052703 000060
021726 052703 000040 5$:
021732 110367 000040
021736 104401 021776
021742 105367 000032 7$:
021746 003347
021750 002402

```



```

000000 0222126 005720          TST      R0,4          ;; JUST INCREMENTING
000001 0222130 020027 000010  CMP      R0,#10       ;; CHECK THE TABLE INDEX
000002 0222134 002746          BLT     R0,R1         ;; GO DO THE NEXT DIGIT
000003 0222136 003002          BGT     R0,R1         ;; GO TO EXIT
000004 0222140 010502          MOV     R0,R2         ;; GET THE LSD
000005 0222142 000764          BR     R0             ;; GO CHANGE TO ASCII
000006 0222144 105726          85:    TSTB   (SP)+       ;; WAS THE LSD THE FIRST NON-ZERO?
000007 0222146 100003          BPL     R0            ;; BR IF NO
000008 0222150 116663 177777 177776 95:    MOVB   -1(SP),-2(R3)  ;; YES--SET THE SIGN FOR TYPING
000009 0222152 105013          95:    CLRB   (R3)         ;; SET THE TERMINATOR
000010 0222160 012605          MOV     (SP)+,R5      ;; POP STACK INTO R5
000011 0222162 012603          MOV     (SP)+,R3      ;; POP STACK INTO R3
000012 0222164 012602          MOV     (SP)+,R2      ;; POP STACK INTO R2
000013 0222166 012601          MOV     (SP)+,R1      ;; POP STACK INTO R1
000014 0222170 012600          MOV     (SP)+,R0      ;; POP STACK INTO R0
000015 0222172 104401 022220          TYPE   $DBLK         ;; NOW TYPE THE NUMBER
000016 0222176 016666 000002 000004  MOV     2(SP),4(SP)   ;; ADJUST THE STACK
000017 0222204 012616          MOV     (SP)+,SP     ;;
000018 0222206 000002          RTI                    ;; RETURN TO USER
000019 0222210 023420          $DTBL: 10000.
000020 0222212 001750          1000.
000021 0222214 000144          100.
000022 0222216 000012          10.
000023 0222220 000004          $DBLK: .BLKW 4
000024 0222220 000004          .SBTTL TYPE ROUTINE

*****
*ROUTINE TO TYPE ASCIZ MESSAGE. MESSAGE MUST TERMINATE WITH A 0 BYTE.
*THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.
*NOTE1: $NULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.
*NOTE2: $FILLS CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.
*NOTE3: $FILLC CONTAINS THE CHARACTER TO FILL AFTER.
*
*CALL:
*1) USING A TRAP INSTRUCTION
*   TYPE .MESADR          ;; MESADR IS FIRST ADDRESS OF AN ASCIZ STRING
*OR
*   TYPE MESADR
*
000027 0222230 105767 156723 $TYPE: TSTB   $TPFLG    ;; IS THERE A TERMINAL?
000028 0222234 100002          BPL     IS           ;; BR IF YES
000029 0222236 000000          HALT                    ;; HALT HERE IF NO TERMINAL
000030 0222240 000430          BR     35            ;; LEAVE
000031 0222242 010046          15:    MOV     R0,-(SP)      ;; SAVE R0
000032 0222244 017600 000002  MOV     02(SP),R0     ;; GET ADDRESS OF ASCIZ STRING
000033 0222250 122767 000001 156774  CMPB   #APTENV,$ENV   ;; RUNNING IN APT MODE
000034 0222256 001011          BNE     62$          ;; NO, GO CHECK FOR APT CONSOLE
000035 0222260 132767 000100 156765  BITB   #APTPOOL,$ENVM ;; SPOOL MESSAGE TO APT
000036 0222266 001405          BEQ     62$          ;; NO, GO CHECK FOR CONSOLE
000037 0222270 010067 000004  MOV     R0,61$        ;; SETUP MESSAGE ADDRESS FOR APT
000038 0222274 004767 000220  JSR     PC,$ATY3     ;; SPOOL MESSAGE TO APT
000039 0222300 000000          61$:   .WORD 0           ;; MESSAGE ADDRESS
000040 0222302 132767 000040 156743 62$:   BITB   #APTCJIP,$ENVM ;; APT CONSOLE SUPPRESSED
000041 0222310 001003          BNE     60$          ;; YES, SKIP TYPE OUT

```



```

5842 022312 112046 2$: MOVB (RO)+, -(SP) ;; PUSH CHARACTER TO BE TYPED ONTC STACK
5843 022314 001005 BNE 4$ ;; BR IF IT ISN'T THE TERMINATOR
5844 022316 005726 TST (SP)+ ;; IF TERMINATOR POP IT OFF THE STACK
5845 022320 012600 60$: MOV (SP)+, RO ;; RESTORE RO
5846 022322 062716 3$: ADD #2, (SP) ;; ADJUST RETURN PC
5847 022326 000002 RTI ;; RETURN
5848 022330 122716 000011 4$: CMPB #HT, (SP) ;; BRANCH IF <HT>
5849 022334 001430 BEQ 8$
5850 022336 122716 000200 CMPB #CRLF, (SP) ;; BRANCH IF NOT <CRLF>
5851 022342 001006 BNE 5$
5852 022344 005726 TST (SP)+ ;; POP <CR><LF> EQUIV
5853 022346 104401 TYPE ;; TYPE A CR AND LF
5854 022350 001227 $CRLF
5855 022352 105067 000130 CLRB $CHARCNT ;; CLEAR CHARACTER COUNT
5856 022356 000755 BR 2$ ;; GET NEXT CHARACTER
5857 022360 004767 000056 5$: JSR PC, $TYPEC ;; GO TYPE THIS CHARACTER
5858 022364 126726 156566 5$: CMPB $FILLC, (SP)+ ;; IS IT TIME FOR FILLER CHARS.?
5859 022370 001350 BNE 2$ ;; IF NO GO GET NEXT CHAR.
5860 022372 016746 156556 MOV $NULL, -(SP) ;; GET # OF FILLER CHARS. NEEDED
5861 AND THE NULL CHAR.
5862 022376 105366 000001 7$: DECB 1(SP) ;; DOES A NULL NEED TO BE TYPED?
5863 022402 002770 BLT 6$ ;; BR IF NO--GO POP THE NULL OFF OF STACK
5864 022404 004767 000032 JSR PC, $TYPEC ;; GO TYPE A NULL
5865 022410 105367 000072 DECB $CHARCNT ;; DO NOT COUNT AS A COUNT
5866 022414 000770 BR 7$ ;; LOOP

```

;HORIZONTAL TAB PROCESSOR

```

5870 022416 112716 000040 8$: MOVB #' (SP) ;; REPLACE TAB WITH SPACE
5871 022422 004767 000014 9$: JSR PC, $TYPEC ;; TYPE A SPACE
5872 022426 132767 000007 000052 BITB #7, $CHARCNT ;; BRANCH IF NOT AT
5873 022434 001372 BNE 9$ ;; TAB STOP
5874 022436 005726 TST (SP)+ ;; POP SPACE OFF STACK
5875 022440 000724 BR 2$ ;; GET NEXT CHARACTER
5876 022442 105777 156502 $TYPEC: TSTB $STPS ;; WAIT UNTIL PRINTER IS READY
5877 022446 100375 BPL $TYPEC
5878 022450 116677 000002 156474 MOVB 2(SP), $STPB ;; LOAD CHAR TO BE TYPED INTO DATA REG.
5879 022456 122766 000015 000002 CMPB #CR, 2(SP) ;; IS CHARACTER A CARRIAGE RETURN?
5880 022464 001003 BNE 1$ ;; BRANCH IF NO
5881 022466 105067 000014 CLRB $CHARCNT ;; YES--CLEAR CHARACTER COUNT
5882 022472 000406 BR $TYPEX ;; EXIT
5883 022474 122766 000012 000002 1$: CMPB #LF, 2(SP) ;; IS CHARACTER A LINE FEED?
5884 022502 001402 BEQ $TYPEX ;; BRANCH IF YES
5885 022504 105227 INCB (PC)+ ;; COUNT THE CHARACTER
5886 022506 000000 $CHARCNT: .WORD 0 ;; CHARACTER COUNT STORAGE
5887 022510 000207 $TYPEX: RTS PC

```

.SBTTL APT COMMUNICATIONS ROUTINE

```

5892 022512 112767 000001 000236 $ATY1: MOVB #1, $FFLG ;; TO REPORT FATAL ERROR
5893 022520 112767 000001 000226 $ATY3: MOVB #1, $MFLG ;; TO TYPE A MESSAGE
5894 022526 000403 BR $ATYC
5895 022530 112767 000001 000220 $ATY4: MOVB #1, $FFLG ;; TO ONLY REPORT FATAL ERROR
5896 022536 $ATYC:
5897 022538 010046 MOV RO, -(SP) ;; PUSH RO ON STACK

```

```

5898 022540 010146      MOV      R1,-(SP)      ;;PUSH R1 ON STACK
5899 022542 105767 000206  TSTB    $MFLG        ;;SHOULD TYPE A MESSAGE?
5900 022546 001450      BEQ     5$           ;;IF NOT: BR
5901 022550 122767 000001 156474  CMPB    #APTENV,$ENV  ;;OPERATING UNDER APT?
5902 022556 001031      BNE     3$           ;;IF NOT: BR
5903 022560 132767 000100 156465  BITB    #APTPOOL,$ENVM ;;SHOULD SPOOL MESSAGES?
5904 022566 001425      SEQ     3$           ;;IF NOT: BR
5905 022570 017600 000004      MOV     @4(SP),R0     ;;GET MESSAGE ADDR.
5906 022574 062766 000002 000004  ADD     #2,4(SP)      ;;BUMP RETURN ADDR.
5907 022602 005767 156424      TST     $MSGTYPE     ;;SEE IF DONE W/ LAST XMISSION?
5908 022606 001375      BNE     1$           ;;IF NOT: WAIT
5909 022610 010067 156432      MOV     R0,$MSGAD    ;;PUT ADDR IN MAILBOX
5910 022614 105720      TSTB   (R0)+         ;;FIND END OF MESSAGE
5911 022616 001376      BNE     2$           ;;
5912 022620 166700 156422      SUB     $MSGAD,R0    ;;SUB START OF MESSAGE
5913 022624 006200      ASR    R0           ;;GET MESSAGE LNTH IN WORDS
5914 022626 010067 156416      MOV     R0,$MSGGLT   ;;PUT LENGTH IN MAILBOX
5915 022632 012767 000004 156372  MOV     #4,$MSGTYPE  ;;TELL APT TO TAKE MSG.
5916 022640 000413      BR      5$           ;;
5917 022642 017667 000004 000016 3$:     MOV     @4(SP),4$    ;;PUT MSG ADDR IN JSR LINKAGE
5918 022650 062766 000002 000004  ADD     #2,4(SP)     ;;BUMP RETURN ADDRESS
5919 022656 016746 155114      MOV     177776,-(SP) ;;PUSH 177776 ON STACK
5920 022662 004767 177342      JSR    PC,$TYPE     ;;CALL TYPE MACRO
5921 022666 000000      .WORD  0
5922 022670      5$:
5923 022670 105767 000062 10$:   TSTB   $FFLG        ;;SHOULD REPORT FATAL ERROR?
5924 022674 001416      BEQ     12$         ;;IF NOT: BR
5925 022676 005767 156350      TST     $ENV        ;;RUNNING UNDER APT?
5926 022702 001413      BEQ     12$         ;;IF NOT: BR
5927 022704 005767 156322 11$:   TST     $MSGTYPE    ;;FINISHED LAST MESSAGE?
5928 022710 001375      BNE     11$        ;;IF NOT: WAIT
5929 022712 017667 000004 156314  MOV     @4(SP),$FATAL ;;GET ERROR #
5930 022720 062766 000002 000004  ADD     #2,4(SP)     ;;BUMP RETURN ADDR.
5931 022726 005267 156300      INC     $MSGTYPE    ;;TELL APT TO TAKE ERROR
5932 022732 105067 000020 12$:   CLRB   $FFLG        ;;CLEAR FATAL FLAG
5933 022736 105067 000013      CLRB   $LFLG        ;;CLEAR LOG FLAG
5934 022742 105067 000006      CLRB   $MFLG        ;;CLEAR MESSAGE FLAG
5935 022746 012601      MOV     (SP)+,R1    ;;POP STACK INTO R1
5936 022750 012600      MOV     (SP)+,R0    ;;POP STACK INTO R0
5937 022752 000207      RTS     PC          ;;RETURN
5938 022754 000      $MFLG: .BYTE 0     ;;MESSG. FLAG
5939 022755 000      $LFLG: .BYTE 0     ;;LOG FLAG
5940 022756 000      $FFLG: .BYTE 0     ;;FATAL FLAG
5941 022760      .EVEN
5942 000200  APTSIZE=200
5943 000001  APTENV=001
5944 000100  APTPOOL=100
5945 000040  APTCSUP=040
5946      .SBTTL TTY INPUT ROUTINE
5947
5948 *****
5949 .ENABL .LSB
5950
5951 *****
5952 ;*SOFTWARE SWITCH REGISTER CHANGE ROUTINE.
5953 ;*ROUTINE IS ENTERED FROM THE TRAP HANDLER, AND WILL

```



```

5954      : *SERVICE THE TEST FOR CHANGE IN SOFTWARE SWITCH REGISTER TRAP CALL
5955      : *WHEN OPERATING IN TTY FLAG MODE.
5956 022760 022767 000176 156152 $OKSWR: CMP      #5,REG,SWR      ;; IS THE SOFT-SWR SELECTED?
5957 022766 001074          BNE      15$          ;; BRANCH IF NO
5958 022770 105777 156150          TSTB     2$TKS          ;; CHAR THERE?
5959 022774 100071          BPL      15$          ;; IF NO, DON'T WAIT AROUND
5960 022776 117746 156144          MOVB    2$TKB,-(SP)    ;; SAVE THE CHAR
5961 023002 042716 177600          BIC     #1C177,(SP)    ;; STRIP-OFF THE ASCII
5962 023006 022726 000007          CMP     #7,(SP)+      ;; IS IT A CONTROL G?
5963 023012 001062          BNE      15$          ;; NO, RETURN TO USER
5964 023014 126727 156114 000001  CMPB    $AUTOB,#1     ;; ARE WE RUNNING IN AUTO-MODE?
5965 023022 001456          BEQ     15$          ;; BRANCH IF YES
5966
5967 023024 104401 023633          TYPE    , $CNTLG     ;; ECHO THE CONTROL-G (↑G)
5968 023030 104401 023640 $GTSWR: TYPE    $MSWR     ;; TYPE CURRENT CONTENTS
5969 023034 016746 155136          MOV     SWREG,-(SP)   ;; SAVE SWREG FOR TYPEOUT
5970 023040 104402          TYPOC          ;; GO TYPE--OCTAL ASCII(ALL DIGITS)
5971 023042 104401 023651          TYPE    , $MNEW     ;; PROMPT FOR NEW SWR
5972 023046 005046 19$: CLR     -(SP)      ;; CLEAR COUNTER
5973 023050 005046          CLR     -(SP)      ;; THE NEW SWR
5974 023052 105777 156066 7$: TSTB    2$TKS      ;; CHAR THERE?
5975 023056 100375          BPL     7$          ;; IF NOT TRY AGAIN
5976
5977 023060 117746 156062          MOVB    2$TKB,-(SP)  ;; PICK UP CHAR
5978 023064 042716 177600          BIC     #1C177,(SP)  ;; MAKE IT 7-BIT ASCII
5979
5980
5981
5982 023070 021627 000025 9$: CMP     (SP),#25     ;; IS IT A CONTROL-U?
5983 023074 001005          BNE     10$          ;; BRANCH IF NOT
5984 023076 104401 023626          TYPE    , $CNTLU    ;; YES, ECHO CONTROL-U (↑U)
5985 023102 062706 000006 20$: ADD     #6,SP      ;; IGNORE PREVIOUS INPUT
5986 023106 000757          BR     19$          ;; LET'S TRY IT AGAIN
5987
5988
5989 023110 021627 000015 10$: CMP     (SP),#15    ;; IS IT A <CR>?
5990 023114 001022          BNE     16$          ;; BRANCH IF NO
5991 023116 005766 000004          TST     4(SP)        ;; YES, IS IT THE FIRST CHAR?
5992 023122 001403          BEQ     11$          ;; BRANCH IF YES
5993 023124 016677 000002 156006  MOV     2(SP),2$SWR   ;; SAVE NEW SWR
5994 023132 062706 000006 11$: ADD     #6,SP      ;; CLEAR UP STACK
5995 023136 104401 001227 14$: TYPE    , $CRLF     ;; ECHO <CR> AND <LF>
5996 023142 126727 155767 000001  CMPB    $INTAG,#1    ;; RE-ENABLE TTY KBD INTERRUPTS?
5997 023150 001003          BNE     15$          ;; BRANCH IF NOT
5998 023152 012777 000100 155764  MOV     #100,2$TKS   ;; RE-ENABLE TTY KBD INTERRUPTS
5999 023160 000002          RTI                    ;; RETURN
6000 023162 004767 177254 15$: JSR     PC,$TYPEC    ;; ECHO CHAR
6001 023166 021627 000060          CMP     (SP),#60     ;; CHAR < 0?
6002 023172 002420          BLT     18$          ;; BRANCH IF YES
6003 023174 021627 000067          CMP     (SP),#67     ;; CHAR > 7?
6004 023200 003015          BGT     18$          ;; BRANCH IF YES
6005 023202 042726 000060          BIC     #60,(SP)+    ;; STRIP-OFF ASCII
6006 023206 005766 000002          TST     2(SP)        ;; IS THIS THE FIRST CHAR
6007 023212 001403          BEQ     17$          ;; BRANCH IF YES
6008 023214 006316          ASL     (SP)         ;; NO, SHIFT PRESENT
6009 023216 006316          ASL     (SP)         ;; CHAR OVER TO MAKE

```

```

6010 023220 006316          ASL      (SP)          ;; ROOM FOR NEW ONE.
6011 023222 005266 000002 17$: INC      2(SP)          ;; KEEP COUNT OF CHAR
6012 023226 056616 177776  BIS      -2(SP), (SP)  ;; SET IN NEW CHAR
6013 023232 000707          BR       7$           ;; GET THE NEXT ONE
6014 023234 104431 001226 18$: TYPE   $QUES       ;; TYPE ?<CR><LF>
6015 023240 000720          BR       20$          ;; SIMULATE CONTROL-U
6016 .DSABL  LSB
6017
6018
6019
6020
6021
6022
6023
6024
6025
6026
6027 023242 011646          $RDCHR: MOV      (SP), -(SP)  ;; PUSH DOWN THE PC
6028 023244 016666 000004 000002 MOV      4(SP), 2(SP)  ;; SAVE THE PS
6029 023252 105777 155666 1$: TSTB   2$TKS       ;; WAIT FOR
6030 023256 100375          BPL      1$           ;; A CHARACTER
6031 023260 117766 155662 000004 MOVB     2$TKB, 4(SP)  ;; READ THE TTY
6032 023266 042766 177600 000004 BIC      #1C<17>, 4(SP) ;; GET RID OF JUNK IF ANY
6033 023274 026627 000004 000023 CMP      4(SP), #23   ;; IS IT A CONTROL-S?
6034 023302 001013          BNE      3$           ;; BRANCH IF NO
6035 023304 105777 155634 2$: TSTB   2$TKS       ;; WAIT FOR A CHARACTER
6036 023310 100375          BPL      2$           ;; LOOP UNTIL ITS THERE
6037 023312 117746 155630 MOVB     2$TKB, -(SP)  ;; GET CHARACTER
6038 023316 042716 177600 BIC      #1C17, (SP)  ;; MAKE IT 7-BIT ASCII
6039 023322 022627 000021 CMP      (SP)+, #21   ;; IS IT A CONTROL-Q?
6040 023326 001366          BNE      2$           ;; IF NOT DISCARD IT
6041 023330 000750          BR       1$           ;; YES, RESUME
6042 023332 026627 000004 000140 3$: CMP      4(SP), #140  ;; IS IT UPPER CASE?
6043 023340 002407          BLT      4$           ;; BRANCH IF YES
6044 023342 026627 000004 000175 CMP      4(SP), #175  ;; IS IT A SPECIAL CHAR?
6045 023350 003003          BGT      4$           ;; BRANCH IF YES
6046 023352 042766 000040 000004 BIC      #40, 4(SP)   ;; MAKE IT UPPER CASE
6047 023360 000002          4$: RTI             ;; GO BACK TO USER
6048
6049
6050
6051
6052
6053
6054
6055 023362 010346          $RDLIN: MOV      R3, -(SP)  ;; SAVE R3
6056 023364 005046          CLR      -(SP)       ;; CLEAR THE RUBOUT KEY
6057 023366 012703 023616 1$: MOV      #$TTYIN, R3  ;; GET ADDRESS
6058 023372 022703 023626 2$: CMP      #$TTYIN+8., R3  ;; BUFFER FULL?
6059 023376 101456          BLOS    4$           ;; BR IF YES
6060 023400 104410          RDCHR    ;; GO READ ONE CHARACTER FROM THE TTY
6061 023402 112613          MOVB     (SP)+, (R3)  ;; GET CHARACTER
6062 023404 122713 000177 10$: CMPB    #177, (R3)  ;; IS IT A RUBOUT
6063 023410 001022          BNE     5$           ;; BR IF NO
6064 023412 005716          TST     (SP)         ;; IS THIS THE FIRST RUBOUT?
6065 023414 001007          BNE     6$           ;; BR IF NO

```

```

6066 023416 112767 000134 000170      MOVB    #' \,9$      ;;TYPE A BACK SLASH
6067 023424 104401 023614      TYPE    .9$
6068 023430 012716 177777      MOV     #-1,(SP)    ;;SET THE RUBOUT KEY
6069 023434 005303      DEC     R3          ;;BACKUP BY ONE
6070 023436 020327 023616 65:    CMP     R3,#$TTYIN ;;STACK EMPTY?
6071 023442 103434      BLO    4$          ;;BR IF YES
6072 023444 111367 000144      MOVB   (R3),9$     ;;SETUP TO TYPEOUT THE DELETED CHAR.
6073 023450 104401 023614      TYPE   .9$        ;;GO TYPE
6074 023454 000746      BR     2$          ;;GO READ ANOTHER CHAR.
6075 023456 005716 55:    TST    (SP)        ;;RUBOUT KEY SET?
6076 023460 001406      BEQ    7$          ;;BR IF NO
6077 023462 112767 000134 000124      MOVB   #' \,9$     ;;TYPE A BACK SLASH
6078 023470 104401 023614      TYPE   .9$
6079 023474 005016      CLR    (SP)        ;;CLEAR THE RUBOUT KEY
6080 023476 122713 000025 75:    CMPB   #25,(R3)   ;;IS CHARACTER A CTRL U?
6081 023502 001003      BNE    8$          ;;BR IF NO
6082 023504 104401 023626      TYPE   $CNTLU     ;;TYPE A CONTROL "U"
6083 023510 000726      BR     1$          ;;GO START OVER
6084 023512 122713 000022 85:    CMPB   #22,(R3)   ;;IS CHARACTER A "↑R"?
6085 023516 001011      BNE    3$          ;;BRANCH IF NO
6086 023520 105013      CLRB   (R3)        ;;CLEAR THE CHARACTER
6087 023522 104401 001227      TYPE   $CRLF      ;;TYPE A "CR" & "LF"
6088 023526 104401 023616      TYPE   $TTYIN     ;;TYPE THE INPUT STRING
6089 023532 000717      BR     2$          ;;GO PICKUP ANOTHER CHARACTER
6090 023534 104401 001226 45:    TYPE   $QUES      ;;TYPE A "?"
6091 023540 000712      BR     1$          ;;CLEAR THE BUFFER AND LOOP
6092 023542 111367 000046 35:    MOVB   (R3),9$    ;;ECHO THE CHARACTER
6093 023546 104401 023614      TYPE   .9$
6094 023552 122723 000015      CMPB   #15,(R3)+  ;;CHECK FOR RETURN
6095 023556 001305      BNE    2$          ;;LOOP IF NOT RETURN
6096 023560 105063 177777      CLRB   -1(R3)     ;;CLEAR RETURN (THE .15)
6097 023564 104401 001230      TYPE   $LF        ;;TYPE A LINE FEED
6098 023570 005726      TST    (SP)+      ;;CLEAN RUBOUT KEY FROM THE STACK
6099 023572 012603      MOV    (SP)+,R3   ;;RESTORE R3
6100 023574 011646      MOV    (SP)-,(SP) ;;ADJUST THE STACK AND PUT ADDRESS OF THE
6101 023576 016666 000004 000002      MOV    4(SP),2(SP) ;;FIRST ASCII CHARACTER ON IT
6102 023604 012766 023616 000004      MC     #$TTYIN,4(SP)
6103 023612 000002      RTI
6104 023614      000      95:    .BYTE  0          ;;RETURN
6105 023615      000      .BYTE  0          ;;STORAGE FOR ASCII CHAR. TO TYPE
6106 023616 000010      $TTYIN: .BLKB  8.    ;;TERMINATOR
6107 023626 052536 005015 000      $CNTLU: .ASCIZ  /↑U/<15><12> ;;RESERVE 8 BYTES FOR TTY INPUT
6108 023633      136 006507 000012      $CNTLG: .ASCIZ  /↑G/<15><12> ;;CONTROL "U"
6109 023640 005015 053523 020122      $MSWR:  .ASCIZ  <15><12>/SWR = / ;;CONTROL "G"
6110 023646 020075      000
6111 023651      040 047040 053505      $MNEW:  .ASCIZ  / NEW = /
6112 023656 036440 000040
6113
6114
6115
6116
6117
6118
6119
6120
6121

```

```

;*****
;*THIS ROUTINE WILL READ AN OCTAL (ASCII) NUMBER FROM THE TTY AND
;*CHANGE IT TO BINARY.
;*THE INPUT CHARACTERS WILL BE CHECKED TO INSURED THEY ARE LEGAL
;*OCTAL DIGITS. IF AN ILLEGAL CHARACTER IS READ A "?" WILL BE TYPED
;*FOLLOWED BY A CARRIAGE RETURN-LINE FEED. THE COMPLETE NUMBER MUST
;*THEN BE RETYPED. THE INPUT IS TERMINATED BY TYPING A CARRIAGE RETURN.

```

```

6122          ;*CALL:
6123          ;*      RDOCT          ;; READ AN OCTAL NUMBER
6124          ;*      PFTJRN HERE  ;; LOW ORDER BITS ARE ON TOP OF THE STACK
6125          ;*                                     ;; HIGH ORDER BITS ARE IN $HIOCT
6126
6127 023662 011646 $RDOCT: MOV      (SP), -(SP)  ;; PROVIDE SPACE FOR THE
6128 023664 016566 000004 000002 MOV      4(SP), 2(SP)  ;; INPUT NUMBER
6129 023672 010046 MOV      RD, -(SP)  ;; PUSH RD ON STACK
6130 023674 010146 MOV      R1, -(SP)  ;; PUSH R1 ON STACK
6131 023676 010246 MOV      R2, -(SP)  ;; PUSH R2 ON STACK
6132 023700 104411 1$:      RDLIN  ;; READ AN ASCII LINE
6133 023702 012600 MOV      (SP)+, RD  ;; GET ADDRESS OF 1ST CHARACTER
6134 023704 010067 000100 MOV      RD, 5$  ;; AND SAVE IT.
6135 023710 005001 CLR      R1  ;; CLEAR DATA WORD
6136 023712 005002 CLR      R2
6137 023714 112046 2$:      MOVVB  (RD)+, -(SP)  ;; PICKUP THIS CHARACTER
6138 023716 001420 BEQ      3$  ;; IF ZERO GET OUT
6139 023720 122716 000060 CMPB    #'0, (SP)  ;; MAKE SURE THIS CHARACTER
6140 023724 003026 BGT      4$  ;; IS AN OCTAL DIGIT
6141 023726 122716 000067 CMPB    #'7, (SP)
6142 023732 002423 BLT      4$
6143 023734 006301 ASL      R1  ;; *2
6144 023736 006102 ROL      R2
6145 023740 006301 ASL      R1  ;; *4
6146 023742 006102 ROL      R2
6147 023744 006301 ASL      R1  ;; *8
6148 023746 006102 ROL      R2
6149 023750 042716 177770 BIC      #'07, (SP)  ;; STRIP THE ASCII JUNK
6150 023754 062601 ADD      (SP)+, R1  ;; ADD IN THIS DIGIT
6151 023756 000756 BR       2$  ;; LOOP
6152 023760 005726 3$:      TST      (SP)+  ;; CLEAN TERMINATOR FROM STACK
6153 023762 010166 000012 MOV      R1, 12(SP)  ;; SAVE THE RESULT
6154 023766 010267 000026 MOV      R2, $HIOCT
6155 023772 012602 MOV      (SP)+, R2  ;; POP STACK INTO R2
6156 023774 012601 MOV      (SP)+, R1  ;; POP STACK INTO R1
6157 023776 012600 MOV      (SP)+, RD  ;; POP STACK INTO RD
6158 024000 000002 RTI  ;; RETURN
6159 024002 005726 4$:      TST      (SP)+  ;; CLEAN PARTIAL FROM STACK
6160 024004 105010 CLRB    (RD)  ;; SET A TERMINATOR
6161 024006 104401 TYPE  ;; TYPE UP THRU THE BAD CHAR.
6162 024010 000000 5$:      .WORD    0
6163 024012 104401 001226 TYPE    $QUES  ;; "?" "CR" & "LF"
6164 024016 000730 BR       1$  ;; TRY AGAIN
6165 024020 000000 $HIOCT: .WORD    0  ;; HIGH ORDER BITS GO HERE
6166          .SBTTL  TRAP DECODER
6167
6168          ;:*****
6169          ;*THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION
6170          ;*AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS
6171          ;*OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
6172          ;*GO TO THAT ROUTINE.
6173
6174 024022 010046 $STRAP: MOV      RD, -(SP)  ;; SAVE RD
6175 024024 016600 000002 MOV      2(SP), RD  ;; GET TRAP ADDRESS
6176 024030 005740 TST      -(RD)  ;; BACKUP BY 2
6177 024032 111000 MOVVB    (RD), RD  ;; GET RIGHT BYTE OF TRAP

```





\*\*\*\*\*  
:COMMON DM11 SERVICE ROUTINES  
\*\*\*\*\*

:THIS ROUTINE IS CALLED DURING START UP TO LOAD THE XMITTER  
:OUTPUT BUFFER WITH A BINARY COUNT TEST PATTERN

024266 012701 037112  
024267 005002  
024268 110327  
024269 005202  
024300 022702 000400  
024301 001373  
024306 000207

LDTBF1: MOV ,TBUF,R1 ;POINT TO START OF BUFFER  
CLR R2 ;INIT DATA BYTE GENERATOR  
IS: MOVB R2,(R1)+ ;LOAD ONE CHAR  
INC R2 ;GENERATE NEXT CHAR  
CMP #400,R2 ;LOADED 256(10) BYTES  
SNE IS ;BR IF NOT  
RTS PC ;RETURN TO START TESTING

:THIS ROUTINE SETS UP THE ERROR INFORMATION REQUIRED BY ANY TEST  
:USING A "DH1" HEADER

024310 004767 002612  
024311 116700 154532  
024312 010067 154536  
024313 010167 154534  
024314 010267 154532  
024315 010367 154536  
024316 062767 000002 154630  
024317 000207

SUER1: JSR PC,SAPS ;SAVE THE ERROR PSW  
MOVB \$STNM,R0 ;SAVE THE TEST NO.  
MOV R0,\$REG0 ;SAVE THE TEST NO. FOR ERROR PRINT  
MOV R1,\$REG1 ;SAVE THE DH1 ADDR  
MOV R2,\$REG2 ;SAVE THE REG ADDRESS  
MOV R6,\$REG6 ;SAVE THE SP  
ADD #2,\$REG6 ;CORRECT FOR CALLING JSR  
RTS PC ;RETURN TO CALLING ROUTINE

:THIS ROUTINE IS CALLED BY THOSE TESTS USING A "DH2" HEADER TO  
:SAVE THE ERROR INFORMATION IN "DT2"

024335 004767 002552  
024336 116700 154532  
024337 010067 154576  
024338 010167 154574  
024339 010267 154572  
024340 010367 154570  
024341 010467 154566  
024342 010567 154566  
024343 062767 000002 154560  
024344 000207

SUER2: JSR PC,SAPS ;SAVE THE ERROR PSW  
SUER2A: MOVB \$STNM,R0 ;GET THE TEST NO.  
MOV R0,\$REG0 ;SAVE THE REGISTERS-TEST#  
MOV R1,\$REG1 ;SAVE THE DH ADDRESS  
MOV R2,\$REG2 ;SAVE THE REGISTER ADDRESS  
MOV R3,\$REG3 ;SAVE THE WAS DATA  
MOV R4,\$REG4 ;SAVE THE S B DATA  
MOV R6,\$REG6 ;SAVE THE STACK POINTER  
ADD #2,\$REG6 ;CORRECT FOR CALLING JSR  
RTS PC ;RETURN TO REPORT ERROR

:THIS ROUTINE IS CALLED TO SET UP ERROR INFORMATION FOR THE  
:BUS ERROR AND RSVD INSTR ERROR ROUTINES

024400 010067 154536  
024401 010167 154534  
024402 010267 154532  
024403 000207

SUER3: MOV R0,\$REG0 ;SAVE THE REGS  
MOV R1,\$REG1  
MOV R2,\$REG2  
RTS PC ;RETURN TO REPORT ERROR

:THIS ROUTINE IS CALLED TO SET UP ERROR INFORMATION FOR THE  
:CAR/BCR MEMORY PATTERNS TESTS

024436 005067 154540  
024437 116767 003546 154532  
024438 116700 154426  
024439 010067 154502

SUER4: CLR \$TMP0 ;SAVE THE LINE NO. WRITTEN  
MOVB LINEA,\$TMP0  
MOVB \$STNM,R0 ;SAVE THE TEST NUMBER  
MOV R0,\$REG0 ;SAVE THE REGISTER INFORMATION



024460 010167 154500  
024464 010267 154476  
024470 010367 154454  
024474 010467 154432  
024500 000207

MOV R1,\$REG1  
MOV R2,\$REG2  
MOV R3,\$REG3  
MOV R4,\$REG4  
RTS PC

;RETURN TO PATTERNS TEST

;THIS ROUTINE IS CALLED TO SELECT A NEW LINE NO. BASED ON THE  
;VALUE OF THE LINE SELECTION PARAMETER

;CALLING SEQUENCE:

;JSR PC,SELINE  
;BR 1\$

;CALL THE ROUTINE  
;EXIT BRANCH-ROUTINE MOVES THE RETURN  
;PC AROUND THIS BR IF MORE LINES APE  
;YET TO BE TESTED

024502 105767 003505  
024506 001010  
024510 105167 003477  
024514 012767 003001 002462  
024518 105067 003464  
024522 000405  
024526 105267 003456  
024530 006367 002444  
024534 001407  
024538 006767 002436 002432  
024542 001767  
024546 002716 000302  
024550 000405  
024554 005067 003426  
024558 142767 000017 002400  
024600 000207

SELINE: TSTB LINE+1  
BNE 1\$  
COMB LINE+1  
MOV #1,LINMSK  
CLRB LINE  
BR 2\$  
1\$: INCB LINE  
ASL LINMSK  
BEQ 3\$  
2\$: BIT LINMSK,LINSEL  
BEQ 1\$  
ADD #2,(SP)  
BR 4\$  
3\$: CLR LINE  
4\$: BICB #17,DHADR  
RTS PC

;FIRST TIME THROUGH FOR ANY TEST ?  
;BR IF NOT  
;SET ENTRY FLAG  
;INIT SELECT TEST MASK TO TEST LINE 00  
;START WITH LINE #00  
;GO TEST FOR LINE #00  
;GENERATE NEW LINE NO.  
;SHIFT SELECT MASK TO TEST NXT LINE  
;RETURN TO EXIT BRANCH - ALL LINES DONE  
;IS THE LINE SELECTED FOR TEST ??  
;BR IF NOT  
;MOVE RETURN PC AROUND EXIT BRANCH  
;RETURN TO TEST SELECTED LINE  
;INIT ENTRY FLAG AND LINE NO. TO 000  
;INIT LINE SELECT BITS IN "SCR"  
;RETURN TO CALLING TEST

;THIS ROUTINE IS CALLED TO CONVERT EITHER THE "DH" NUMBER OR THE  
;"LINE" NUMBER TO TWO ASCII CHARACTERS AND MOVE THEM INTO A  
;PARTICULAR MESSAGE BUFFER FOR ERROR REPORTING

;CALLING SEQUENCE

;JSR R5,SUNUM  
;ADDR1  
;ADDR2

;CALL TO THIS ROUTINE  
;ADDRESS OF THE NUMBER TO BE CONVERTED  
;ADDRESS OF THE MSG BUFFER SLOT

024574  
024574 010046  
024576 010146  
024600 010246  
024602 012500  
024604 012301  
024606 111000  
024610 010002  
024612 006202  
024614 006202  
024616 006202  
024620 042702 177770  
024624 062702 000060

SUNUM: MOV R0,-(SP)  
MOV R1,-(SP)  
MOV R2,-(SP)  
MOV (R5)+,R0  
MOV (R5)+,R1  
MOV#B (R0),R0  
MOV R0,R2  
ASR R2  
ASR R2  
ASR R2  
BIC #177770,R2  
ADD #60,R2

:: PUSH R0 ON STACK  
:: PUSH R1 ON STACK  
:: PUSH R2 ON STACK  
;GET ADDRESS OF NUMBER  
;GET MSG BUFFER ADDR  
;GET NO. TO BE CONVERTED  
;SAVE IT IN R2  
;SHIFT MSD TO LSD POSITION  
  
;CLR JUNK BITS  
;MAKE IT ASCII



6366 024630 110221  
6367 024632 042700 177770  
6368 024636 062700 000060  
6369 024642 110011  
6370 024644 012602  
6371 024646 012601  
6372 024650 012600  
6373 024652 000205

MOVB R2,(R1)+ ;PUT IT IN MSG BUFFER  
BIC #177770,R0 ;CLR JUNK FROM LSD  
ADD #60,R0 ;MAKE IT ASCII  
MOVB R0,(R1) ;PUT LSD IN THE BUFFER  
MOV (SP)+,R2 ;POP STACK INTO R2  
MOV (SP)+,R1 ;POP STACK INTO R1  
MOV (SP)+,R0 ;POP STACK INTO R0  
RTS R5 ;RETURN TO CALLER

:THIS ROUTINE IS CALLED TO CLEAR THE "CAR" AND "BCR" MEMORIES  
:IT ASSUMES THAT THE ADDRESS OF THE "SCR" IS IN R1

6374 024654 005067 154340  
6375 024660 116711 154334  
6376 024664 005061 000006  
6377 024670 005061 000010  
6378 024674 005267 154320  
6379 024700 022767 000020 154312  
6380 024706 001364  
6381 024710 142711 000017  
6382 024714 000207

CLCABC: CLR STMP7 ;INIT A COUNTER  
1\$: MOVB STMP7,(R1) ;SELECT A LINE  
CLR CAR(R1) ;CLEAR A CAR LOCATION  
CLR BCR(R1) ;CLEAR A BCR LOCATION  
INC STMP7 ;GENERATE NEW LINE NO.  
CMP #20,STMP7 ;DONE ALL LINES ?  
BNE 1\$ ;BR IF NOT  
BICB #17,(R1) ;SET "SCR" TO SELECT LINE 00  
RTS PC ;RETURN TO CALLER

:THIS ROUTINE IS CALLED TO LOAD THE "BCR" MEMORY WITH ALL ONES  
:IT ASSUMES THAT THE ADDRESS OF THE SCR IS IN R1

6383 024716 005067 154276  
6384 024722 116711 154272  
6385 024726 012761 177777 000010  
6386 024734 005267 154260  
6387 024740 022767 000020 154252  
6388 024746 001365  
6389 024750 142711 000017  
6390 024754 000207

LDBCR: CLR STMP7 ;INIT A COUNTER  
1\$: MOVB STMP7,(R1) ;SELECT A LINE  
MOV #-1,BCR(R1) ;LOAD BCR LOC. WITH 177777  
INC STMP7 ;GENERATE NEXT LINE NO.  
CMP #20,STMP7 ;DONE ALL LINES ?  
BNE 1\$ ;BR IF NOT  
BICB #17,(R1) ;SET "SCR" TO SELECT LINE 00  
RTS PC ;RETURN TO CALLER

:THIS ROUTINE CALLED TO SET UP FOR PARITY TESTS

6400 024756 012767 000020 154226  
6401 024764 105011  
6402 024766 005002  
6403 024770 012703 000200  
6404 024774 012704 000001  
6405 025000 012761 037112 000006  
6406 025006 016761 154204 000010  
6407 025014 016761 154174 000004  
6408 025022 105062 036112  
6409 025026 110364 036112  
6410 025032 005211  
6411 025034 005203  
6412 025036 062702 000002  
6413 025042 062704 000002  
6414 025046 005367 154140  
6415 025052 001362  
6416 025054 012704 027452  
6417 025060 016724 154132  
6418 025064 022704 027512  
6419 025070 001372

SUPPAR: MOV #20,STMP4 ;SET UP FOR 16. LINES  
CLRB (R1) ;INIT SCR TO START AT LINE 00  
CLR R2 ;INIT INDEX REGISTER FOR RBUF (EVEN)  
MOV #200,R3 ;SET UP CONSTANT  
MOV #1,R4 ;INIT INDEX REG FOR RBUF (ODD)  
1\$: MOV #TABUF,CAR(R1) ;LOAD BUS ADDRESS REWG  
MOV STMP6,BCR(R1) ;LOAD BYTE COUNT REG  
MOV STMP5,LPR(R1) ;LOAD LINE PARAMETERS  
CLRB RBUF(R2) ;INIT DATA BYTE IN RBUF TO START AT 000  
MOVB R3,RBUF(R4) ;SET CONSTANT IN HIGH BYTE  
INC (R1) ;SELECT NEXT LINE  
INC R3 ;GENERATE NEW CONSTANT  
ADD #2,R2 ;UPDATE POINTERS TO RBUF (EVEN/ODD)  
ADD #2,R4  
DEC STMP4 ;COUNT ONE LINE SETUP  
BNE 1\$ ;BR TILL ALL 16. SET UP  
MOV #MULPTB,R4 ;SET UP TABLE POINTER  
2\$: MOV STMP6,(R4)+ ;SET UP BYTE COUNT ENTRY  
CMP #MULPTB+40,R4 ;SET UP ALL COUNTS  
BNE 2\$ ;BR IF NOT

```

6422 025072 105011          CLRB (R1)          ;INIT SCR TO SELECT LINE 00
6423 025074 000207          RTS PC           ;RETURN TO PARITY TEST
6424
6425          ;THIS ROUTINE AUTOSIZES THE SYSTEM TO DETERMINE THE ADDRESSES AND
6426          ;VECTORS OF THE DH11'S AND DM11-BB'S.
6427
6428 025076 010046          AUTOSZ: MOV      R0,-(SP)
6429 025100 005003          CLR      R3
6430 025102 012702 027732          MOV      #DHADRS,R2          ;POINT TO BEGINNING OF TABLE
6431 025106 005022          25$: CLR      (R2)+          ;CLEAR AUTOSIZER TABLES.
6432 025110 005263          INC      R3
6433 025112 020327 000102          CMP      R3,#102          ;HAVE WE CLEARED ALL ENTRIES?
6434 025116 001373          BNE      25$          ;BRANCH IF NOT.
6435 025120 013746 000004          MOV      @#4,-(SP)          ;SAVE TRAP VECTOR.
6436 025124 012737 025232 000004          MOV      #4$,@#4          ;SETUP FOR NON-EXISTENT MEMORY TRAP.
6437 025132 012703 030034          MOV      #DMADRS,R3          ;SETUP DM ADDRESS TABLE POINTER.
6438 025136 012702 027732          MOV      #DHADRS,R2          ;SET UP DH ADDRESS TABLE POINTER.
6439
6440 025142 012701 160020          MOV      #160020,R1          ;R1=FIRST ADDRESS TO BE TESTED.
6441
6442 025146 005711          1$: TST      (R1)          ;SEE IF ADDRESS IN R1 RESPONDS.
6443 025150 005761 000016          TST      16(R1)          ;CHECK TO SEE IF DEVICE IS MODULO 20.
6444 025154 052711 004000          BIS      #4000,(R1)          ;IF IT IS, CONTINUE
6445          ;AND CHECK TO SEE
6446 025160 052711 001000          BIS      #1000,(R1)          ;IF THIS ADDRESS CONTAINS
6447 025164 052711 002000          BIS      #2000,(R1)          ;A DH-11.
6448 025170 032711 003000          BIT      #3000,(R1)          ;CHECK TO INSURE THESE BITS SET.
6449 025174 001410          BEQ      3$          ;IF NOT, BRANCH.
6450          ;SET THE MAINTENANCE BIT, THE NON-
6451 025176 052711 000400          BIS      #400,(R1)          ;EXISTENT MEMORY BIT AND THE CLEAR
6452          ;NON-EXISTENT MEMORY INTERRUPT BIT.
6453 025202 032711 002400          BIT      #2400,(R1)          ;IS THIS A DH-11? (BITS 8 AND 10 SHOULD
6454          ;CLEAR IF THIS IS A DH11.)
6455
6456 025206 001003          BNE      3$          ;IF NOT, CHECK TO SEE IF THIS IS A DM11-BB.
6457 025210 042711 001000          BIC      #1000,(R1)          ;CLEAR MAINTENANCE BIT.
6458 025214 010122          MOV      R1,(R2)+          ;SAVE THE ADDRESS IN THE DH ACR TABLE.
6459
6460 025216 020127 163760          3$: CMP      R1,#163760          ;HAVE WE REACHED THE TOP OF THE FLOATING ADDRESSES.
6461 025222 001406          BEQ      5$          ;IF YES, GET OUT.
6462 025224 062701 000020          ADD      #20,R1          ;IF NOT, UPDATE ADDRESS AND
6463 025230 000746          BR       1$          ;GO CHECK IT.
6464
6465 025232 012716 025216          4$: MOV      #3$,(SP)          ;IF DH ADDRESS DOES NOT RESPOND, GO TO 3$.
6466 025236 000002          RTI
6467
6468          ;TEST FOR DM11 BB ADDRESS
6469
6470 025240 012737 025272 000004          5$: MOV      #6$,@#4          ;SETUP FOR NON-EXISTENT MEMORY TRAP.
6471 025246 012701 170500          MOV      #170500,R1          ;R1=FIRST ADDRESS TO BE TESTED.
6472 025252 005711          21$: TST      (R1)          ;SEE IF ADDRESS RESPONDS.
6473 025254 010123          MOV      R1,(R3)+          ;IF IT DOES, THIS IS A DM11-BB.
6474          ;SO SAVE THE ADDRESS.
6475 025256 020127 170670          23$: CMP      R1,#170670          ;HAVE WE REACHED THE TOP OF THE DM11 ADDRESSES?
6476 025262 001406          BEQ      22$          ;IF YES, GET OUT.

```

```

6478 025264 062701 000010          ADD    #10,R1      ;IF NOT, UPDATE ADDRESS AND
6479 025270 000770          BR     21$        ;GO CHECK IT.
6480
6481 025272 012716 025256 -      6$:    MOV    #23$, (SP) ;IF DM ADDRESS DOES NOT RESPOND, GO TO 23$.
6482 025276 000002          RTI
6483
6484 025300 012637 000004          22$:   MOV    (SP)+, 2#4 ;RESTORE TRAP VECTOR.
6485 025304 162702 027732          SUB    #DHADRS,R2 ;HAVE WE FOUND ANY DH11'S AT ALL?
6486 025310 001003          BNE   7$         ;IF YES, BRANCH
6487 025312 104401 035451          TYPE  ,MSG1      ;NO DH11'S WERE FOUND.
6488 025316 000000          HALT
6489
6490 025320 006202          7$:    ASR    R2       ;R2 NOW CONTAINS THE NUMBER
6491 025322 005000          CLR    R0        ;OF DH'S FOUND.
6492 025324 006100          8$:    ROL    R0        ;FILL R0 WITH 1'S
6493 025326 005200          INC    R0        ;CORRESPONDING TO
6494 025330 005302          DEC    R2        ;THE NUMBER OF DH'S
6495 025332 005702          TST   R2        ;FOUND.
6496 025334 001373          BNE   8$
6497 025336 010067 002642          MOV    R0, $DHSEL ;$DHSEL CONTAINS THE DH SELECTION PARAMETER.
6498                          ;IE. ALL DH'S FOUND WILL BE TESTED.
6499
6500                          ;FIND DH VECTOR:
6501 025342 012702 027732          MOV    #DHADRS,R2 ;SETUP POINTER TO BEGINNING OF DH
6502 025346 012705 027774          MOV    #DHVEC,R5  ;ADDRESS TABLE AND VECTOR TABLE.
6503 025352 012737 000340 000022          MOV    #340, 2#IOTVEC+2 ;SET IOT TRAP PRIORITY TO 7.
6504 025360 012737 025470 000020          MOV    #12$, 2#IOTVEC ;SETUP IOT TRAP VECTOR.
6505 025366 012703 000300          MOV    #300,R3   ;START OF FLOATING VECTORS
6506 025372 012704 000302          MOV    #302,R4   ;PC OF IOT INSTR.
6507
6508 025376 010423          9$:    MOV    R4, (R3)+ ;FILL VECTOR AREA WITH ADDRESS
6509                          ;OF NEXT INSTR (.+2)
6510 025400 012724 000004          MOV    #4, (R4)+ ;NEXT INSTRUCTION IS AN IOT TRAP.
6511 025404 022324          CMP    (R3)+, (R4)+ ;UPDATE R3+R4.
6512 025406 020427 001000          CMP    R4, #1000 ;HAVE WE REACHED TO TOP OF THE
6513                          ;VECTOR SPACE?
6514 025412 101771          BLOS  9$        ;IF NOT, REPEAT PROCESS.
6515
6516 025414 005712          10$:   TST   (R2)     ;HAVE WE CHECK ALL DH'S?
6517 025416 001441          BEQ   13$      ;IF YES, GET OUT + CHECK FOR DM11 BB'S VECTORS.
6518
6519 025420 005067 152352          CLR    PS       ;ZERO CPU PRIORITY.
6520 025424 052772 001000 000000          BIS    #1000, 2(R2) ;SET MAINTENANCE BIT
6521 025432 052772 000300 000000          BIS    #300, 2(R2) ;ATTEMPT TO CAUSE RECEIVER
6522                          ;INTERRUPT.
6523 025440 005000          CLR    R0
6524
6525 025442 005200          11$:   INC    R0        ;WAIT...
6526 025444 001376          BNE   11$
6527 025446 104401 035501          TYPE  ,MSG2      ;ERROR MSG-NO DH RECEIVER INTERRUPT OCCURRED.
6528 025452 052772 004000 000000          BIS    #4000, 2(R2) ;DO A MASTER CLEAR
6529 025460 042772 001000 000000          BIC    #1000, 2(R2) ;CLEAR MAINTENANCE BIT
6530 025466 000752          BR     10$
6531
6532 025470 011601          12$:   MOV    (SP), R1
6533 025472 042701 000007          BIC    #7, R1    ;CLEAR GARBAGE.

```

```

6534 025476 010125      MOV      R1,(R5)+      ;SAVE VECTOR ADDRESS.
6535 025500 022626      CMP      (SP)+,(SP)+  ;POP STACK
6536 025502 012716 025414    MOV      #105,(SP)    ;SETUP FOR RETURN.
6537 025506 052772 004000 000000    BIS      #4000,@(R2)  ;DO A MASTER CLEAR
6538 025514 042732 001000    BIC      #1000,@(R2)+ ;CLEAR MAINTENANCE BIT.
6539 025520 000002      RTI
6540
6541                ;FIND DM11 BB VECTORS:
6542
6543 025522 012702 030034    13$:    MOV      #DMADRS,R2   ;SET POINTERS TO BEGINNING OF
6544 025526 012705 030076      MOV      #DMVEC,R5    ;ADR TABLE & VECTOR TABLE.
6545 025532 012737 025614 000020    MOV      #165,@#IOTVEC ;SET IOT TRAP VECTOR.
6546
6547 025540 005712    14$:    TST      (R2)         ;HAVE WE CHECKED ALL DM'S?
6548 025542 001441      BEQ      17$         ;IF YES, GET OUT.
6549 025544 005067 152226    CLR      PS          ;ZERO CPU PRIORITY
6550 025550 052772 001000 000000    BIS      #1000,@(R2)  ;SET MAINTENANCE BIT.
6551 025556 052772 000300 000000    BIS      #300,@(R2)  ;ATTEMPT TO CAUSE INTERRUPT.
6552 025564 005000      CLR      R0
6553
6554 025566 005200    15$:    INC      R0          ;WAIT....
6555 025570 001376      BNE      15$
6556 025572 104401 035546    TYPE    ,MSG3        ;ERROR MSG - NO DM11-BB INTERRUPT OCCURRED.
6557 025576 052772 004000 000000    BIS      #4000,@(R2)  ;CLEAR BITS PREVIOUSLY SET.
6558 025604 042772 001000 000000    BIC      #1000,@(R2)  ;CLEAR MAINTENANCE BIT.
6559 025612 000752      BR      14$
6560
6561 025614 011601    16$:    MOV      (SP),R1      ;CALCULATE VECTOR ADDRESS.
6562 025616 162701 000004    SUB      #4,R1        ;SAVE VECTOR ADDRESS.
6563 025622 010125      MOV      R1,(R5)+    ;POP STACK.
6564 025624 022626      CMP      (SP)+,(SP)+ ;SETUP FOR RETURN.
6565 025626 012716 025540    MOV      #145,(SP)   ;CLEAR BITS PREVIOUSLY SET.
6566 025632 052772 004000 000000    BIS      #4000,@(R2)  ;CLEAR MAINTENANCE BIT AND
6567 025640 042732 001000    BIC      #1000,@(R2)+ ;POINT TO NEXT DM11-BB ADDRESS.
6568
6569 025644 000002      RTI
6570
6571 025646 012737 020746 000020    17$:    MOV      #SCOPE,@#IOTVEC ;RESTORE IOT VECTOR FOR SCOPE ROUTINE.
6572 025654 012600      MOV      (SP)+,R0    ;RESTORE R0.
6573 025656 012703 000300      MOV      #300,R3     ;START OF FLOATING VECTORS.
6574 025662 012704 000302      MOV      #302,R4
6575
6576 025666 010423    18$:    MOV      R4,(R3)+    ;FILL VECTOR AREA WITH ADDRESS OF NEXT
6577                ;INSTRUCTION (.+2).
6578 025670 012724 000000    MOV      #0,(R4)+    ;NEXT INSTRUCTION IS A HALT.
6579 025674 022324      CMP      (R3)+,(R4)+ ;UPDATE R3 & R4.
6580 025676 020427 001000    CMP      R4,#1000    ;ARE WE DONE?
6581 025702 101771      BLOS    18$         ;IF NOT, REPEAT UNTIL ADDRESSES
6582                ;377 TO 777 ARE DONE.
6583 025704 013701 027774      MOV      @#DHVEC,R1  ;LET R1 POINT TO 1ST DH VECTOR ADDRESS.
6584 025710 005737 027776      TST      @#DHVEC+2   ;IS THERE MORE THAN ONE VECTOR?
6585 025714 001403      BEQ      26$         ;BRANCH IF NOT.
6586 025716 163701 027776      SUB      @#DHVEC+2,R1 ;DETERMINE NUMBER OF ADDRESSES
6587                ;BETWEEN DH VECTORS (10(8) OR 20(8)).
6588 025722 005401      NEG      R1          ;MAKE R1 POSITIVE.
6589 025724 010167 002246    26$:    MOV      R1,ADRVEC   ;SAVE THAT NUMBER.

```

```

6590 025730 032777 000002 153202 BIT #BIT1,DSWR ;SHOULD DEVICE MAP BE TYPED OUT?
6591 025736 001442 BEQ 20$ ;IF NOT, RETURN.
6592 025740 104401 TYPE ;TYPEOUT MAP OF DH & DM11-BB'S
6593 025742 035613 DEVMAP ;FOUND.
6594 025744 012701 027732 MOV #DHADRS,R1 ;R1-BEGINNING OF DH ADDRESS TABLE.
6595 025750 012702 027774 MOV #DHVEC,R2 ;R2-BEGINNING OF DH VECTOR TABLE.
6596 025754 012703 030034 MOV #DMADRS,R3 ;R3-BEGINNING OF DM11-BB ADDRESS TABLE.
6597 025760 012704 030076 MOV #DMVEC,R4 ;R4-BEGINNING OF DM11-BB VECTOR TABLE.
6598
6599 025764 012146 19$: MOV (R1)+,-(SP) ;MOVE DATA TO BE TYPED
6600 025766 104403 TYPOS ;TYPE DATA
6601 025770 006 .BYTE 6
6602 025771 001 .BYTE 1
6603 025772 012246 MOV (R2)+,-(SP) ;MOVE DATA TO BE TYPED
6604 025774 104403 TYPOS ;TYPE DATA
6605 025776 005 .BYTE 5
6606 025777 000 .BYTE 0
6607 026000 104401 035607 TYPE SPACE
6608 026004 012346 MOV (R3)+,-(SP) ;MOVE DATA TO BE TYPED.
6609 026006 104403 TYPOS ;TYPE DATA.
6610 026010 006 .BYTE 6
6611 026011 001 .BYTE 1
6612 026012 104401 035607 TYPE SPACE
6613 026016 012446 MOV (R4)+,-(SP) ;MOVE DATA TO BE TYPED.
6614 026020 104403 TYPOS ;TYPE DATA.
6615 026022 005 .BYTE 5
6616 026023 000 .BYTE 0
6617 026024 104401 TYPE ;TYPE A CARRIAGE RETURN & LINE FEED.
6618 026026 001227 $CRLF
6619 026030 005711 TST (R1) ;HAVE WE TYPED ALL CH ENTRIES?
6620 026032 001354 BNE 19$ ;IF NOT, DO IT AGAIN.
6621 026034 005713 TST (R3) ;HAVE WE TYPED ALL DM ENTRIES?
6622 026036 001352 BNE 19$ ;IF NOT - ONE MORE TIME.
6623 026040 104401 001227 TYPE $CRLF
6624 026044 000207 20$: RTS PC ;IF YES, GO BACK TO MAIN PROGRAM.
6625
6626 ;THIS ROUTINE IS USED TO ACCEPT INPUT PARAMETERS FROM THE CONSOLE
6627 ;TELETYPE
6628
6629 026046 104401 INPARA: TYPE
6630 026050 035354 VCWC ;"ASK FOR NO. ADDRESSES BETWEEN VECTORS"
6631 026052 104412 RDOCT ;READ OCTAL NO. FM TTY
6632 026054 012600 MOV (SP)+,RO ;GET THE NO. HE TYPED
6633 026056 001407 BEQ 3$ ;BR IF HE TYPED <CR>
6634 026060 022700 000010 CMP #10,RO ;10(8) ADDRESSES BETWEEN VECTORS ?
6635 026064 001406 BEQ 4$ ;BR IF YES
6636 026066 022700 000020 CMP #20,RO ;20(8) ADDRESSES BETWEEN VECTORS ??
6637 026072 001403 BEQ 4$ ;BR IF YES
6638 026074 000764 BR INPARA ;ASK ALL OVER AGAIN
6639 026076 012700 000020 3$: MOV #20,RO ;SET UP CONSTANT FOR 20(8) ADDRESSES
6640 026102 000207 4$: RTS PC ;RETURN TO CALLER
6641
6642
6643
6644 026104 012700 177777 INPARC: MOV #-1,RO ;SET FLAG IN RO
6645 026110 000167 154034 JMP BEGINA ;GO ASK FOR SELECT PARAMETER

```

6646										
6647	026114	012767	177777	001546	INPARX:	MOV	#-1, VCFLG			:SET SETUP FLAG
6648	026122	000167	154022			JMP	BEGINA			:GO START UP
6649										
6650	026126	013701	027732		INPAR:	MOV	3#DHADR, R1			:MOVE ADDRESS OF FIRST DH INTO R1.
6651	026132	032777	000001	153000		BIT	#BIT0, 3SWR			:ARE PARAMETERS TO BE INPUT MANUALLY?
6652	026140	001405				BEQ	2\$			:BRANCH IF NOT.
6653	026142	104401			1\$:	TYPE				:ASK FOR DEVICE ADDRESS
6654	026144	034731				INMSG1				
6655	026146	104412				RDOCT				:READ IN WHAT IS TYPED
6656	026150	012601				MOV	(SP)+, R1			:GET THE NO. HE TYPED
6657	026152	001403				BEQ	INPAR1			:BR IF DEFAULT
6658	026154	004767	000160		2\$:	JSR	PC, CHKADR			:GO CHECK VALIDITY OF THE ADDR
6659	026160	000770				BR	1\$			:ERROR BRANCH
6660										
6661	026162	013701	027774		INPAR1:	MOV	2#DHVEC, R1			:MOVE FIRST DH VECTOR INTO R1.
6662	026166	032777	000001	152744		BIT	#BIT0, 3SWR			:ARE PARAMETERS TO BE INPUT MANUALLY?
6663	026174	001405				BEQ	2\$			:BRANCH IF NOT.
6664	026176	104401			1\$:	TYPE				:ASK FOR VECTOR ADDRESS
6665	026200	034775				INMSG2				
6666	026202	104412				RDOCT				:READ IN WHAT HE TYPES
6667	026204	012601				MOV	(SP)+, R1			:GET THE ADDRESS
6668	026206	001403				BEQ	INPAR3			:BR IF DEFAULT
6669	026210	004767	000240		2\$:	JSR	PC, CHKVCT			:GO CHECK VALIDITY OF VECTOR
6670	026214	000770				BR	1\$			:ERROR BRANCH
6671										
6672	026216	013701	030204		INPAR3:	MOV	2#DHSEL, R1			:MOVE DEVICE SELECTION PARAMETER INTO R1.
6673	026222	005700				TST	R0			:DID WE START AT 210?
6674	026224	100404				BMI	2\$			:BRANCH IF YES.
6675	026226	032777	000001	152704		BIT	#BIT0, 3SWR			:IS PARAMETER TO BE INPUT MANUALLY?
6676	026234	001405				BEQ	1\$			:BRANCH IF NOT.
6677	026236	104401			2\$:	TYPE				:ASK FOR DEVICE SELECTION PARAMETER
6678	026240	035044				INMSG3				
6679	026242	104412				RDOCT				:READ IN WHAT HE TYPES
6680	026244	012601				MOV	(SP)+, R1			:GET THE SELECT PARAMETER
6681	026246	001402				BEQ	INPAR4			:BR IF DEFAULT
6682	026250	010167	000724		1\$:	MOV	R1, DHSEL			:SET UP DH11 SELECTION PARAMETER
6683										
6684	026254	005700			INPAR4:	TST	R0			:DID WE START AT 210?
6685	026256	100404				BMI	3\$			:BRANCH IF YES.
6686	026260	032777	000001	152652		BIT	#BIT0, 3SWR			:IS LINE SELECT PARAMETER TO BE INPUT MANUALLY?
6687	026266	001410				BEQ	1\$			:BRANCH IF NO.
6688	026270	104401			3\$:	TYPE				:ASK FOR LINE SELECT PARAMETER
6689	026272	035242				INMSG6				
6690	026274	104412				RDOCT				:GET WHAT HE TYPES
6691	026276	012601				MOV	(SP)+, R1			:GET PARAMETER
6692	026300	001403				BEQ	1\$			:BR IF DEFAULT
6693	026302	010167	000674			MOV	R1, LINSEL			:SET UP LINE SELECT PARAMETER
6694	026306	000403				BR	2\$			:CONTINUE
6695	026310	012767	177777	000664	1\$:	MOV	#-1, LINSEL			:SET UP DEFAULT (ALL LINES)
6696	026316	032777	000400	152614	2\$:	BIT	#BIT0, 3SWR			:HALT AFTER SET UP ??
6697	026324	001403				BEQ	EXPAR			:BR IF NOT
6698	026326	104401				TYPE				:TYPE CONTINUE MESSAGE PRIOR TO HALTING
6699	026330	035304				INMSG7				
6700	026332	000000				HALT				:DEPRESS CONTINUE TO RESUME TESTING
6701	026334	000167	154264		EXPAR:	JMP	START2			:GO START UP THE PROGRAM

6702									
6703									
6704	026340	020127	160020	CHKADR:	CMP	R1, #160020		: IS ADDRESS ABOVE OR EQUAL TO LOW LIMIT	
6705	026344	002001			BGE	1\$		: BR IF YES	
6706	026346	000437			BR	4\$		: BR IF NOT	
6707	026350	020127	160420	1\$:	CMP	R1, #160420		: IS IT BELOW THE HIGH LIMIT?	
6708	026354	002401			BLT	2\$		: BR IF YES	
6709	026356	000433			BR	4\$		: BR IF NOT	
6710	026360	032701	000017	2\$:	BIT	#17, R1		: CORRECT BOUNDARY ?	
6711	026364	001030			BNE	4\$		: BR IF NOT	
6712	026366	062716	000002		ADD	#2, (SP)		: MOVE RETURN PC AROUND ERROR BRANCH	
6713	026372	012702	027570		MOV	#DHADTB, R2		: POINT TO BEGIN OF ADDR TABLE	
6714	026376	032777	000001	152534	BIT	#BIT0, @SWR		: ARE WE AUTOSIZING?	
6715	026404	001011			BNE	3\$		: BRANCH IF NOT.	
6716	026406	012703	027732		MOV	#DHADRS, R3		: POINT TO BEGINNING OF AUTOSIZER	
6717								: DH ADDRESS TABLE.	
6718	026412	016704	001566		MOV	\$DHSEL, R4			
6719	026416	012322		6\$:	MOV	(R3)+, (R2)+		: MOVE CONTENTS OF AUTOSIZER DH TABLE	
6720								: TO THE TABLE USED BY PROGRAM.	
6721	026420	006204			ASR	R4			
6722	026422	005704			TST	R4		: HAVE WE MOVED ALL TABLE ENTRIES?	
6723	026424	001374			BNE	6\$		: BRANCH IF NOT--ONE MORE TIME.	
6724	026426	000411			BR	5\$		: RETURN TO INPUT ROUTINES.	
6725	026430	010122		3\$:	MOV	R1, (R2)+		: SET UP A TABLE ENTRY	
6726	026432	062701	000020		ADD	#20, R1		: GENERATE NEXT DH11 ADDR	
6727	026436	022702	027630		CMP	#DHADTB+40, R2		: END OF TABLE ?	
6728	026442	001372			BNE	3\$		: BR IF NOT	
6729	026444	000402			BR	5\$		: RETURN TO INPUT ROUTINES	
6730	026446	004401		4\$:	TYPE			: TELL HIM HE GOOFED	
6731	026450	035.15			INMSG4				
6732	026452	000207		5\$:	RTS	PC		: RETURN TO INPUT ROUTINES	
6733									
6734	026454	020127	000300	CHKVCT:	CMP	R1, #300		: IS ADDRESS ABOVE OR EQUAL TO LOW LIMIT	
6735	026460	002001			BGE	1\$		: BR IF YES	
6736	026462	000436			BR	4\$		: BR IF NOT	
6737	026464	020127	001000	1\$:	CMP	R1, #1000		: IS IT BELOW THE HIGH LIMIT?	
6738	026470	002401			BLT	2\$		: BR IF YES	
6739	026472	000432			BR	4\$		: BR IF NOT	
6740	026474	032701	000007	2\$:	BIT	#7, R1		: CORRECT BOUNDARY ?	
6741	026500	001027			BNE	4\$		: BR IF NOT	
6742	026502	062716	000002		ADD	#2, (SP)		: MOVE RETURN PC AROUND ERROR BRANCH	
6743	026506	012702	027630		MOV	#DHVCTB, R2		: POINT TO BEGIN OF VECTOR TABLE	
6744	026512	032777	000001	152420	BIT	#BIT0, @SWR		: ARE WE AUTOSIZING?	
6745	026520	001011			BNE	3\$		: BRANCH IF NOT.	
6746	026522	012703	027774		MOV	#DHVEC, R3		: POINT TO BEGINING OF AUTOSIZER	
6747								: DH VECTOR TABLE.	
6748	026526	016704	001452		MOV	\$DHSEL, R4			
6749	026532	012322		6\$:	MOV	(R3)+, (R2)+		: MOVE CONTENTS OF AUTOSIZER VECTOR	
6750								: TABLE TO TABLE USED BY PROGRAM.	
6751	026534	006204			ASR	R4			
6752	026536	005704			TST	R4		: HAVE WE MOVED ALL TABLE ENTRIES?	
6753	026540	001374			BNE	6\$		: BRANCH IF NOT--ONE MORE TIME.	
6754	026542	000410			BR	5\$		: RETURN TO INPUT ROUTINES.	
6755	026544	010122		3\$:	MOV	R1, (R2)+		: SET UP A TABLE ENTRY	
6756	026546	060001			ADD	R0, R1		: GENERATE NEXT DH11 ADDR	
6757	026550	022702	027670		CMP	#DHVCTB+40, R2		: END OF TABLE ?	



```

6758 026554 001373          BNE      3$          ;BR IF NOT
6759 026556 000402          BR       5$          ;RETURN TO INPUT ROUTINES
6760 026560 104401          4$:     TYPE          ;TELL HIM HE GOOFED
6761 026562 035166          INMSG5
6762 026564 000207          5$:     RTS         PC      ;RETURN TO INPUT ROUTINES
6763
6764          ;THESE TWO ROUTINES SERVICE UNEXPECTED BUS ERROR AND RSVD INSTP TRAPS
6765
6766 026566 012767 000340 152406 BUSER:  MOV     #340,$TMPD    ;SAVE THE PSW
6767 026574 010667 152376          MOV     SP,$REG6     ;SAVE THE SP
6768 026600 012601          MOV     (SP)+,R1     ;GET THE TRAP PC
6769 026602 012602          MOV     (SP)+,R2     ;GET THE TRAP PSW
6770 026604 116700 152272          MOVB   $STNM,R0     ;GET TEST NO.
6771 026610 012706 001100          MOV     #STACK,SP   ;RESET THE STACK POINTER
6772 026614 004767 175600          JSR    PC,SUER3     ;GO SET UP ERROR INFO
6773 026620 012767 026630 152262          MOV     #1$,$LPERR  ;ALWAYS COME BACK TO 1$
6774 026626 104027          ERROR  27          ;UNEXPECTED BUS ERROR TRAP
6775 026630 000005          1$:    RESET        ;PREPARE TO RESTART.
6776 026632 004767 000240          JSR    PC,CHPS1     ;GO CLEAR PSW
6777 026636 000167 154056          JMP    REST1        ;GO RESTART THE PROGRAM
6778
6779 026642 012767 000340 152332 RESERR: MOV     #340,$TMPD    ;SAVE THE PSW
6780 026650 010667 152322          MOV     SP,$REG6     ;SAVE THE SP
6781 026654 012601          MOV     (SP)+,R1     ;GET THE TRAP PC
6782 026656 012602          MOV     (SP)+,R2     ;GET THE TRAP PSW
6783 026660 116700 152216          MOVB   $STNM,R0     ;GET TEST NO.
6784 026664 012706 001100          MOV     #STACK,SP   ;RESET THE STACK POINTER
6785 026670 004767 175524          JSR    PC,SUER3     ;GO SET UP ERROR INFO
6786 026674 012767 026704 152206          MOV     #1$,$LPERR  ;ALWAYS COME BACK TO 1$
6787 026702 104030          ERROR  30          ;UNEXPECTED RSVD INSTR ERROR TRAP
6788 026704 000005          1$:    RESET        ;PREPARE TO RESTART
6789 026706 004767 000164          JSR    PC,CHPS1     ;GO CLEAR PSW
6790 026712 000167 154002          JMP    REST1        ;GO RESTART THE PROGRAM
6791
6792          ;THIS ROUTINE IS CALLED WHEN A TEST NEEDS TO RESTORE THE TRAP
6793          ;CATCHER IN THE DH11 VECTOR
6794
6795 026716 016703 000252          RESTRP: MOV     DHVCT,R3    ;GET VECTOR ADDRESS
6796 026722 010313          MOV     R3,(R3)     ;RESTORE THE TRAP CATCHER
6797 026724 062723 000002          ADD     #2,(R3)+
6798 026730 005023          CLR    (R3)+
6799 026732 010313          MOV     R3,(R3)
6800 026734 062723 000002          ADD     #2,(R3)+
6801 026740 005023          CLR    (R3)+
6802 026742 000207          RTS         PC      ;RETURN TO CALLING TEST
6803
6804          ;THIS ROUTINE CALLED BY ANY TEST THAT NEEDS A TIMING WAIT LOOP
6805          ;"TIMEA" IS INITIALIZED BY THE CALLING ROUTINE TO THE MINIMUM REQUIRED
6806          ;VALUE AND "TIMEB" IS CLEARED TO 000000. IF A TIME OUT OCCURS THIS
6807          ;ROUTINE WILL MOVE THE RETURN PC AROUND THE "LOOP" BRANCH BACK IN
6808          ;THE ROUTINE THAT CALLED IT TO ALLOW REPORTING AN ERROR MESSAGE
6809
6810 026744 005267 001272          TIMEIT: INC     TIMEB     ;COUNT B
6811 026750 001005          BNE    1$          ;BR IF NOT ZERO
6812 026752 005367 001262          DEC     TIMEA     ;COUNT TIME A
6813 026756 001002          BNE    1$          ;BR IF NO TIMEOUT

```



```

6814 026760 062716 000002          ADD    #2,(SP)      ;MOVE RETURN PC TO ALLOW ERROR REPORT
6815 026764 000207          1$:   RTS    PC      ;RETURN TO THE CALLING TEST
6816
6817          ;THIS ROUTINE CALLED BY THE AUTO ECHO TEST TO SET UP FOR TRANSFERRING
6818          ;A BINARY COUNT TEST PATTERN ON ALL LINES
6819
6820 026766 012767 000020 152222 SETALL: MOV    #20,$TMP6    ;SET UP SIXTEEN LINES
6821 026774 005002          CLR    R2          ;INIT A TABLE INDEX REG
6822 026776 012703 000200          MOV    #200,R3    ;SET UP TO GENERATE HI BYTE OF EXPECTED DATA
6823 027002 012704 000001          MOV    #1,R4      ;SET UP INDEX REG TO ODD BYTES
6824 027006 005011          CLR    (R1)       ;START WITH LINE 00
6825 027010 012761 037112 000006 1$:   MOV    #TBUF,CAR(R1) ;SET UP BUS ADDR REG
6826 027016 012761 177400 000010          MOV    #-400,BCR(R1) ;SET UP BYTE COUNT REG
6827 027024 012761 031403 000004          MOV    #31403,LPR(R1) ;SET UP FOR 4800 BAUD/8 BIT CHARS
6828 027032 105062 036112          CLR   RBUF(R2)    ;START WITH DATA CHAR OF 000
6829 027036 110364 036112          MOV   R3,RBUF(R4) ;SET UP HIGH BYTE OF EXPECTED DATA
6830 027042 005211          INC   (R1)        ;GEN NEW LINE NO. IN SCR
6831 027044 005203          INC   R3          ;UPDATE THE POINTERS AND DATA
6832 027046 062702 000002          ADD   #2,R2
6833 027052 062704 000002          ADD   #2,R4
6834 027056 005367 152134          DEC   $TMP6      ;COUNT ONE LINE DONE
6835 027062 001352          BNE   1$         ;BR TIL ALL 16 SET UP
6836 027064 016767 000112 000356          MOV   LINSEL,LINACT ;SET SOFTWARE FLAG FOR ALL LINES ACTIVE
6837 027072 005011          CLR   (R1)       ;PUT SCR REG BACK TO LINE 00
6838 027074 000207          RTS    PC        ;RETURN TO AUTO ECHO TEST
6839
6840
6841          ;THIS ROUTINE IS CALLED TO SET PSW PRIORITY TO 000 IN ORDER
6842          ;TO BE LSI11 COMPATIBLE
6843
6844 027076 012746 000000          CHPS1: MOV    #0,-(SP) ;NEW PSW
6845 027102 012746 027110          MOV    #1$,-(SP)    ;NEW PC
6846 027106 000002          RTI                    ;CHANGE PSW
6847 027110 000207          1$:   RTS    PC      ;RETURN TO CALLING TEST
6848
6849          ;THIS ROUTINE DOES THE SAME THING EXCEPT IT SET THE PSW
6850          ;PRIORITY TO 340 (LEVEL 7 ) TO LOCK OUT INTRs
6851
6852 027112 012746 000340          CHPS2: MOV    #340,-(SP) ;NEW PSW
6853 027116 012746 027124          MOV    #1$,-(SP)    ;NEW PC
6854 027122 000002          RTI                    ;CHANGE THE PSW
6855 027124 000207          1$:   RTS    PC      ;RETURN TO CALLING TEST
6856
6857          ;THIS ROUTINE IS ALSO FOR LSI11 COMPATIBILITY AND IT IS CALLED
6858          ;TO SAVE THE PSW IN "$TMP0"
6859
6860 027126 005046          SAPS: CLR    -(SP)    ;TEMP STORAGE TO SAVE PSW
6861 027130 016746 150700          MOV    34,-(SP)    ;SAVE TRAP VECTOR POINTER
6862 027134 012767 027144 150672          MOV    #1$,34     ;GO TO 1$ ON TRAP
6863 027142 104400          TRAP                    ;GO TO IT
6864 027144 016666 000002 000006 1$:   MOV    2(SP),6(SP)  ;GET PSW SAVED
6865 027152 012716 027160          MOV    #2$,(SP)    ;GO TO 2$ ON RTI
6866 027156 000002          RTI
6867 027160 012667 150650          2$:   MOV    (SP)+,34  ;RESTORE VECTOR
6868 027164 012667 152012          MOV    (SP)+,$TMP0 ;FINALLY SAVE PSW IN $TMP0
6869 027170 000207          RTS    PC
    
```

806

MACY11 27 (732) 23-SEP-76 14:33 PAGE 155  
POWER DOWN AND UP ROUTINES

SEC 0273

0000



: THIS 16 WORD TABLE CONTAINS THE TEST DATA USED BY THE AUTO ECHO  
: TEST (ALL 1'S DATA TABLE)

RETAB:	100377	: TEST DATA FOR LINE 00
	100777	: TEST DATA FOR LINE 01
	101377	
	101777	
	102377	
	102777	
	103377	
	103777	
	104377	
	104777	
	105377	
	105777	
	106377	
	106777	
	107377	
	107777	: TEST DATA FOR LINE 17

: THIS 16 WORD TABLE CONTAINS THE TEST DATA USED BY THE AUTO ECHO  
: TEST (ALL 0'S DATA TABLE)

RETAB0:	100000	: TEST DATA FOR LINE 00
	100400	: TEST DATA FOR LINE 01
	101000	
	101400	
	102000	
	102400	
	103000	
	103400	
	104000	
	104400	
	105000	
	105400	
	106000	
	106400	
	107000	
	107400	: TEST DATA FOR LINE 17

: THIS TABLE USED BY THE AUTO ECHO TEST 2 TO RESET ACTIVE BIT WHEN A  
: LINE IS DONE

LINBIT:	BIT00	: DEACTIVATE LINE 00
	BIT01	: DEACTIVATE LINE 01
	BIT02	
	BIT03	
	BIT04	
	BIT05	
	BIT06	
	BIT07	
	BIT08	
	BIT09	
	BIT10	
	BIT11	

```

: THIS 16 WORD TABLE CONTAINS THE TEST DATA USED BY THE AUTO ECHO
: TEST (ALL 1'S DATA TABLE)
RETAB: 100377      : TEST DATA FOR LINE 00
        100777      : TEST DATA FOR LINE 01
        101377
        101777
        102377
        102777
        103377
        103777
        104377
        104777
        105377
        105777
        106377
        106777
        107377
        107777      : TEST DATA FOR LINE 17

: THIS 16 WORD TABLE CONTAINS THE TEST DATA USED BY THE AUTO ECHO
: TEST (ALL 0'S DATA TABLE)
RETAB0: 100000     : TEST DATA FOR LINE 00
         100400     : TEST DATA FOR LINE 01
         101000
         101400
         102000
         102400
         103000
         103400
         104000
         104400
         105000
         105400
         106000
         106400
         107000
         107400     : TEST DATA FOR LINE 17

: THIS TABLE USED BY THE AUTO ECHO TEST 2 TO RESET ACTIVE BIT WHEN A
: LINE IS DONE
LINBIT: BIT00      : DEACTIVATE LINE 00
        BIT01      : DEACTIVATE LINE 01
        BIT02
        BIT03
        BIT04
        BIT05
        BIT06
        BIT07
        BIT08
        BIT09
        BIT10
        BIT11

```



7033 027616 160300  
7034 027620 160320  
7035 027622 160340  
7036 027624 160360  
7037 027626 160400

160300  
160320  
160340  
160360  
160400

; ADDRESS OF THE LAST DH11

; DH11 VECTOR TABLE - THIS TABLE CONTAINS THE VECTOR ADDRESSES FOR UP  
; TO SIXTEEN DH11'S

7038 027630 000330  
7039 027632 000350  
7040 027634 000370  
7041 027636 000410  
7042 027640 000430  
7043 027642 000450  
7044 027644 000470  
7045 027646 000510  
7046 027650 000530  
7047 027652 000550  
7048 027654 000570  
7049 027656 000610  
7050 027660 000630  
7051 027662 000650  
7052 027664 000670  
7053 027666 000710

DHVCTB: 330  
350  
370  
410  
430  
450  
470  
510  
530  
550  
570  
610  
630  
650  
670  
710

; ADDRESS OF VECTOR FOR FIRST DH11  
; ADDRESS OF VECTOR FOR SECOND DH11

; ADDRESS OF VECTOR FOR LAST DH11

7054 027670 000000

VCFLG: 0

; VECTOR SET UP FLAGG

; BR PRIORITY LEVEL TABLE - THIS TABLE CONTAINS THE PRIORITY LEVELS  
; FOR UP TO SIXTEEN DH11'S - THE RCVR LEVEL IS STORED IN THE LOW BYTE  
; AND THE XMYTR LEVEL IN THE HIGH BYTE

7055 027672 120240  
7056 027674 120240  
7057 027676 120240  
7058 027700 120240  
7059 027702 120240  
7060 027704 120240  
7061 027706 120240  
7062 027710 120240  
7063 027712 120240  
7064 027714 120240  
7065 027716 120240  
7066 027720 120240  
7067 027722 120240  
7068 027724 120240  
7069 027726 120240  
7070 027730 120240

BRLVL: 120240  
120240  
120240  
120240  
120240  
120240  
120240  
120240  
120240  
120240  
120240  
120240  
120240  
120240  
120240  
120240

; BR LEVELS FOR FIRST DH11  
; BR LEVELS FOR SECOND DH11

; BR LEVELS FOR LAST DH11

; THIS DH ADDRESS TABLE IS FILLED BY THE AUTOSIZER.

7091 027732 000000  
7092 027732 000000  
7093 027734 000000  
7094 027736 000000

DHADDRS:  
.WORD 0  
.WORD 0  
.WORD 0

7095	027740	000000	.WORD	0
7096	027742	000000	.WORD	0
7097	027744	000000	.WORD	0
7098	027746	000000	.WORD	0
7099	027750	000000	.WORD	0
7100	027752	000000	.WORD	0
7101	027754	000000	.WORD	0
7102	027756	000000	.WORD	0
7103	027760	000000	.WORD	0
7104	027762	000000	.WORD	0
7105	027764	000000	.WORD	0
7106	027766	000000	.WORD	0
7107	027770	000000	.WORD	0
7108	027772	000000	.WORD	0

; THIS DH VECTOR TABLE IS FILLED BY THE AUTOSIZER.

7112	027774		DHVEC:	
7113	027774	000000	.WORD	0
7114	027776	000000	.WORD	0
7115	030000	000000	.WORD	0
7116	030002	000000	.WORD	0
7117	030004	000000	.WORD	0
7118	030006	000000	.WORD	0
7119	030010	000000	.WORD	0
7120	030012	000000	.WORD	0
7121	030014	000000	.WORD	0
7122	030016	000000	.WORD	0
7123	030020	000000	.WORD	0
7124	030022	000000	.WORD	0
7125	030024	000000	.WORD	0
7126	030026	000000	.WORD	0
7127	030030	000000	.WORD	0
7128	030032	000000	.WORD	0

; THIS DM ADDRESS TABLE IS FILLED BY THE AUTOSIZER.

7132	030034		DMADRS:	
7133	030034	000000	.WORD	0
7134	030036	000000	.WORD	0
7135	030040	000000	.WORD	0
7136	030042	000000	.WORD	0
7137	030044	000000	.WORD	0
7138	030046	000000	.WORD	0
7139	030050	000000	.WORD	0
7140	030052	000000	.WORD	0
7141	030054	000000	.WORD	0
7142	030056	000000	.WORD	0
7143	030060	000000	.WORD	0
7144	030062	000000	.WORD	0
7145	030064	000000	.WORD	0
7146	030066	000000	.WORD	0
7147	030070	000000	.WORD	0
7148	030072	000000	.WORD	0
7149	030074	000000	.WORD	0
7150				

: THIS DM VECTOR TABLE IS FILLED BY THE AUTOSIZER.

7151		
7152		
7153		
7154	030076	000000
7155	030076	000000
7156	030100	000000
7157	030102	000000
7158	030104	000000
7159	030106	000000
7160	030110	000000
7161	030112	000000
7162	030114	000000
7163	030116	000000
7164	030120	000000
7165	030122	000000
7166	030124	000000
7167	030126	000000
7168	030130	000000
7169	030132	000000
7170	030134	000000

DMVEC:

.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00
.WORD	00

7171	030136	000001
7172	030136	000002
7173	030140	000004
7174	030142	000004
7175	030144	000010
7176	030146	000020
7177	030150	000040
7178	030152	000100
7179	030154	000200
7180	030156	000400
7181	030160	001000
7182	030162	002000
7183	030164	004000
7184	030166	010000
7185	030170	020000
7186	030172	040000
7187	030174	100000

\$LNSEL:

.WORD	1
.WORD	2
.WORD	4
.WORD	10
.WORD	20
.WORD	40
.WORD	100
.WORD	200
.WORD	400
.WORD	1000
.WORD	2000
.WORD	4000
.WORD	10000
.WORD	20000
.WORD	40000
.WORD	100000

7189	030176	000000
7190	030200	000000
7191	030202	000000
7192	030204	000000
7193	030206	000
7194	030207	000
7195	030210	000000
7196	030212	000000
7197	030214	000000
7198		
7199		
7200		
7201	030216	000000
7202	030220	000000
7203	030222	000000
7204		
7205		
7206		

ADRVEC: 0 ; ADDRESSES BETWEEN VECTORS - FILLED BY THE AUTOSIZER  
 DMCSR: 0 ; DM11-BB CONTROL AND STATUS REGISTER.  
 DMLSR: 0 ; DM11-BB LINE STATUS REGISTER.  
 \$DHSEL: 0 ; DEVICE SELECT PARAMETER - FILLED BY THE AUTOSIZER.  
 CHRLVL: .BYTE 0 ; BR LEVEL FOR RCVR  
 CHTLVL: .BYTE 0 ; BR LEVEL FOR XMITTER  
 DHNUM: 0 ; CONTAINS NUMBER OF THE DM11 UNDER TEST  
 LINE: 0 ; CONTAINS NUMBER OF THE LINE UNDER TEST  
 LINEA: 0 ; LOCATION TO SAVE LINE NUMBER  
 ; ADDRESS POINTERS TO SET UP TABLES WHEN INPUTTING PARAMETERS

ADPTR: 0 ; POINTS TO ADDRESS TABLE  
 VCPTR: 0 ; POINTS TO VECTOR TABLE  
 BRPTR: 0 ; POINTS TO BR LEVEL TABLE

: THE FOLLOWING TEN CONSTANTS ARE USED BY THE DM11-BB PORTION OF THIS PROGRAM.



000007	000400	STEP=400
000008	000001	LINENA=1
000009	000002	TRMRDY=2
000010	000004	RS=4
000011	000010	SECTX=10
000012	000020	SECRX=20
000013	000040	CS=40
000014	000100	CO=100
000015	000200	RING=200
000016	002000	CLRMUX=2000
000017		
000018	030224	TDATA1: 0
000019	030226	TDATA2: 37
000020	030230	
000021	030232	
000022	030234	
000023	030236	
000024	030240	TITLEG: 0
000025	030242	TIMEA: 0
000026	030244	TIMEB: 0
000027	030246	TIMEC: 0
000028		TINCL: 0
000029		
000030		
000031		
000032		
000033		
000034		
000035		
000036		
000037		
000038		
000039		
000040		
000041		
000042		
000043		
000044		
000045		
000046		
000047		
000048		
000049		
000050		
000051		
000052		
000053		
000054		
000055		
000056		
000057		
000058		
000059		
000060		
000061		
000062		
000063		
000064		
000065		
000066		
000067		
000068		
000069		
000070		
000071		
000072		
000073		
000074		
000075		
000076		
000077		
000078		
000079		
000080		
000081		
000082		
000083		
000084		
000085		
000086		
000087		
000088		
000089		
000090		
000091		
000092		
000093		
000094		
000095		
000096		
000097		
000098		
000099		
000100		

```

:DATA BUFFER FOR BASIC DATA TEST
:TEST DATA FOR FIVE BIT CHAR
:TEST DATA FOR SIX BIT CHAR
:TEST DATA FOR SEVEN BIT CHAR
:TEST DATA FOR EIGHT BIT CHAR
:FLAG TO ALLOW PRINTING TITLE ONLY ONCE
:GENERAL PURPOSE TIMERS

:TIMER FOR TIMING TESTS
:CONTAINS TWO NULL CHARS USED BY BREAK TEST

```

7231  
7232  
7233  
7234  
7235  
7236  
7237  
7238  
7239  
7240  
7241  
7242  
7243  
7244  
7245  
7246  
7247  
7248  
7249  
7250  
7251  
7252  
7253  
7254  
7255  
7256  
7257  
7258  
7259  
7260  
7261  
7262  
7263  
7264  
7265  
7266  
7267  
7268  
7269  
7270  
7271  
7272  
7273  
7274  
7275  
7276  
7277  
7278  
7279  
7280  
7281  
7282  
7283  
7284  
7285  
7286

030250 044104 030461 051040  
030256 043505 051511 042524  
030264 020122 042522 042506  
030272 042522 041516 020105  
030300 040503 051525 042105  
030396 052040 046511 047505  
030314 052125 000  
030317 040 050050 024503  
030324 020040 020040 050050  
030332 024523 020040 020040  
030340 051450 024520 020040  
030346 020040 042524 052123  
030354 020040 042040 053105  
030362 042101 020122 051040  
030370 043505 042101 000122  
  
030376 001116 001202 001176  
030404 001162 001164 001166  
030412 000000  
  
030414 054523 052123 046505  
030422 041440 047117 051124  
030430 046117 051040 043505  
030436 051511 042524 020122  
030444 051105 047522 000122  
030452 024040 041520 020051  
030460 020040 024040 051520  
030466 020051 020040 024040  
030474 050123 020051 020040  
030502 052040 051505 020124  
030510 020040 042504 040526  
030516 051104 020040 042522  
030524 040507 051104 020040  
030532 053440 051501 020040  
030540 020040 051440 041057  
030546 000  
030550  
030550 001116 001202 001176  
030556 001162 001164 001166  
030564 001170 001172 000000  
  
030572 044104 030461 046440  
030600 051501 042524 020122  
030606 046103 040505 020122  
030614 040506 046111 042105  
030622 052040 020117 046103

\*\*\*\*\*  
:ERROR MESSAGE INFORMATION - MESSAGE BUFFERS AND POINTERS  
:\*\*\*\*\*

:INFORMATION FOR MESSAGE 1

EM1: .ASCIZ 'DH11 REGISTER REFERENCE CAUSED TIMEOUT'

DH1: .ASCIZ ' (PC) (PS) (SP) TEST DEVADR REGADR'

.EVEN  
DT1: .WORD \$ERRPC,\$TMP0,\$REG6,\$REG0,\$REG1,\$REG2,0

:INFORMATION FOR MESSAGE 2

EM2: .ASCIZ 'SYSTEM CONTROL REGISTER ERROR'

DH2: .ASCIZ ' (PC) (PS) (SP) TEST DEVADR REGADR WAS S B'

.EVEN  
DT2: .WORD \$ERRPC,\$TMP0,\$REG6,\$REG0,\$REG1,\$REG2,\$REG3,\$REG4,0

:INFORMATION FOR MESSAGE 3

EM3: .ASCIZ 'DH11 MASTER CLEAR FAILED TO CLR SPECIFIED REG'

7287	030630	020122	050123	041505
7288	030636	043111	042511	020104
7289	030644	042522	000107	

; INFORMATION FOR MESSAGE 4

7293	030650	044514	042516	050040
7294	030656	051101	046501	052105
7295	030664	051105	051040	043505
7296	030672	051511	042524	020122
7297	030700	051105	047522	000122

EM4: .ASCIZ 'LINE PARAMETER REGISTER ERROR'

; INFORMATION FOR MESSAGE 5

7301	030706	051102	040505	020113
7302	030714	047503	052116	047522
7303	030722	020114	042522	044507
7304	030730	052123	051105	042440
7305	030736	051122	051117	000

EM5: .ASCIZ 'BREAK CONTROL REGISTER ERROR'

; INFORMATION FOR MESSAGE 6

7309	030743	123	046111	020117
7310	030750	052123	052101	051525
7311	030756	051040	043505	051511
7312	030764	042524	020122	051105
7313	030772	047522	000122	

EM6: .ASCIZ 'SILO STATUS REGISTER ERROR'

; INFORMATION FOR MESSAGE 7

7317	030776	052503	051122	047105
7318	031004	020124	042101	051104
7319	031012	051505	020123	042522
7320	031020	044507	052123	051105
7321	031026	042440	051122	051117
7322	031034	026440	046040	047111
7323	031042	020105	054043	000130

EM7: .ASCIZ 'CURRENT ADDRESS REGISTER ERROR - LINE #XX'

; INFORMATION FOR MESSAGE 10

7327	031050	054502	042524	041440
7328	031056	052517	052116	051105
7329	031064	051040	043505	051511
7330	031072	042524	020122	051105
7331	031100	047522	020122	020055
7332	031106	044514	042516	021440
7333	031114	054130	000	

EM10: .ASCIZ 'BYTE COUNTER REGISTER ERROR - LINE #XX'

; INFORMATION FOR MESSAGE 11

7337	031117	125	042516	050130
7338	031124	041505	042524	020104
7339	031132	044104	030461	051040
7340	031140	053103	020122	047111
7341	031146	042524	051122	050125
7342	031154	000124		

EM11: .ASCIZ 'UNEXPECTED DM11 RCVR INTERRUPT'

7343  
7344  
7345  
7346  
7347  
7348  
7349  
7350  
7351  
7352  
7353  
7354  
7355  
7356  
7357  
7358  
7359  
7360  
7361  
7362  
7363  
7364  
7365  
7366  
7367  
7368  
7369  
7370  
7371  
7372  
7373  
7374  
7375  
7376  
7377  
7378  
7379  
7380  
7381  
7382  
7383  
7384  
7385  
7386  
7387  
7388  
7389  
7390  
7391  
7392  
7393  
7394  
7395  
7396  
7397  
7398

; INFORMATION FOR MESSAGE 12

031156 047125 054105 042520  
031164 052103 042105 042040  
031172 030510 020061 046530  
031200 052111 051124 044440  
031206 052116 051105 052522  
031214 052120 000

EM12: .ASCIZ 'UNEXPECTED DH11 XMITTR INTERRUPT'

; INFORMATION FOR MESSAGE 13

031217 103 040510 020122  
031224 053101 044501 040514  
031232 046102 020105 040506  
031240 046111 042105 052040  
031246 020117 042507 042516  
031254 040522 042524 051040  
031262 053103 020122 047111  
031270 042524 051122 050125  
031276 000124

EM13: .ASCIZ 'CHAR AVAILABLE FAILED TO GENERATE RCVR INTERRUPT'

; INFORMATION FOR MESSAGE 14

031300 051124 047101 046523  
031306 052111 042524 020122  
031314 050116 020122 047514  
031322 044507 020103 051105  
031330 047522 020122 020055  
031336 044514 042516 021440  
031344 020040 000

EM14: .ASCIZ 'TRANSMITTER NPR LOGIC ERROR - LINE # '

; INFORMATION FOR MESSAGE 15

031347 130 044515 052124  
031354 020122 040506 046111  
031362 042105 052040 020117  
031370 047111 042524 051122  
031376 050125 020124 020055  
031404 044514 042516 021440  
031412 020040 000

EM15: .ASCIZ 'XMITTR FAILED TO INTERRUPT - LINE # '

; INFORMATION FOR MESSAGE 16

031415 122 053103 020122  
031422 040506 046111 042105  
031430 052040 020117 047111  
031436 042524 051122 050125  
031444 000124

EM16: .ASCIZ 'RCVR FAILED TO INTERRUPT'

; INFORMATION FOR MESSAGE 17

031446 051124 047101 046523  
031454 052111 042524 020122  
031462 044524 044515 043516  
031470 042440 051122 051117

EM17: .ASCIZ 'TRANSMITTER TIMING ERROR - LINE # '



7455	032062	052040	051505	020124
7456	032070	020040	042504	040526
7457	032076	051104	020040	044103
7458	032104	046122	043516	020040
7459	032112	053440	051501	020040
7460	032120	020040	051440	041057
7461	032126	000		

; INFORMATION FOR MESSAGE 24

7465	032127	101	052125	020117
7466	032134	041505	047510	052040
7467	032142	051505	020124	051105
7468	032150	047522	020122	020055
7469	032156	044514	042516	021440
7470	032164	020040	000	

EM24: .ASCIZ 'AUTO ECHO TEST ERROR - LINE # '

7471				
7472				
7473				

; INFORMATION FOR MESSAGE 25

7474	032167	102	042522	045501
7475	032174	041040	052111	052040
7476	032202	051505	020124	051105
7477	032210	047522	020122	020055
7478	032216	044514	042516	021440
7479	032224	020040	000	

EM25: .ASCIZ 'BREAK BIT TEST ERROR - LINE # '

7480				
7481				
7482				

; INFORMATION FOR MESSAGE 26

7483	032227	110	046101	026506
7484	032234	052504	046120	054105
7485	032242	052040	051505	020124
7486	032250	051105	047522	020122
7487	032256	020055	044514	042516
7488	032264	021440	020040	000

EM26: .ASCIZ 'HALF-DUPLEX TEST ERROR - LINE # '

7489				
7490				
7491				

; INFORMATION FOR MESSAGE 27

7492	032271	125	042516	050130
7493	032276	041505	042524	020104
7494	032304	052502	020123	051105
7495	032312	047522	020122	051124
7496	032320	050101	000	
7497	032323	040	050050	024503
7498	032330	020040	020040	050050
7499	032336	024523	020040	020040
7500	032344	051450	024520	020040
7501	032352	020040	042524	052123
7502	032360	020040	052040	050122
7503	032366	041520	020040	052040
7504	032374	050122	051520	000040

EM27: .ASCIZ 'UNEXPECTED BUS ERROR TRAP'

7505				
7506	032402	001116	001202	001176
7507	032410	001162	001164	001166
7508	032416	000000		
7509				
7510				

DH3: .ASCIZ ' (PC) (PS) (SP) TEST TRPPC TRPPS '

.EVEN  
 DT3: .WORD \$ERRPC, \$TMFC, \$REG6, \$REG0, \$REG1, \$REG2, 0

; INFORMATION FOR MESSAGE 30



0332770	047111	0520105
0332778	047111	0520105
0332786	047111	0520105
0332794	047111	0520105
0332802	047111	0520105
0332810	047111	0520105
0332818	047111	0520105
0332826	047111	0520105
0332834	047111	0520105
0332842	047111	0520105
0332850	047111	0520105

: INFORMATION FOR MESSAGE 35

0333056	052114	026511
0333064	042516	050340
0333072	052111	020131
0333080	040524	052040
0333088	020124	044524
0333096	052517	000124
0333104	041520	020051
0333112	046050	051120
0333120	020040	041501
0333128	047111	000
0333136	033152	
0333144	001116	001202
0333152	000000	001210

EM35: .ASCIZ 'MULTI-LINE PARITY DATA TEST TIMEOUT'

DM14: .ASCIZ '(PC) (LPRG) ACTLIN'

DY6: .EVEN .WORD SERRPC, STMPC, STMP3, 0

: INFORMATION FOR MESSAGE 36

0333162	051101	040440
0333170	046111	041101
0333178	052040	046511
0333186	052125	000

EM36: .ASCIZ 'CHAR AVAILABLE TIMEOUT'

: INFORMATION FOR MESSAGE 37

0333211	052101	020101
0333219	050115	051101
0333227	051105	047522
0333235	020055	044514
0333243	021440	020040
0333251	000	

EM37: .ASCIZ 'DATA COMPARE ERROR - LINE # '

: INFORMATION FOR MESSAGE 40

0333247	043125	042506
0333255	041501	044524
0333263	051040	043505
0333271	051122	051117
0333279	046040	047111
0333287	020043	000040

EM40: .ASCIZ 'BUFFER ACTIVE REG ERROR - LINE # '

: INFORMATION FOR MESSAGE 41

0333313	051126	043040
0333321	042523	044440
0333329	051105	052522

EM41: .ASCIZ 'RCVR FALSE INTERRUPT'







; INFORMATION FOR MESSAGE 52

EM52: .ASCIZ 'BASIC DATA COMPARE ERROR'

034323	0423102	051501	041511
034324	0423102	051501	020101
034325	0423102	050115	051101
034326	020105	051105	047522
034327	000122		

; INFORMATION FOR MESSAGE 53

DH12: .ASCIZ ' (PC) SPEED (SP) TEST DEVAOR REGADR WAS S/B'

034334	024040	041520	020051
034335	020040	050123	042505
034336	020104	020040	024040
034337	050123	020051	020040
034338	020040	051505	020124
034339	020040	042504	040526
034340	051104	020040	042522
034341	040507	051104	020040
034342	052340	051501	020040
034343	000	051440	041057

; INFORMATION FOR MESSAGE 55

DH13: .ASCIZ ' (PC) (PS) (SP) TEST DEVAOR CHALNG SCRWAS SCRS/B'

034350	020040	050050	024503
034351	020040	020040	050050
034352	020040	020040	020040
034353	020040	024520	020040
034354	042524	042524	052123
034355	042040	042040	053105
034356	020122	020122	041440
034357	051110	047114	020107
034358	051440	051103	040527
034359	020123	051440	051103
034360	000102	000102	

; INFORMATION FOR MESSAGE 56

EM56: .ASCIZ 'OVERRUN BIT FAILED TO SET - LINE #'

034520	053117	051105	052522
034521	020116	044502	020124
034522	040506	046111	042105
034523	052040	020117	042523
034524	020124	020055	044514
034525	042516	021440	020040
034526	000		

; INFORMATION FOR MESSAGE 57

EM57: .ASCIZ 'STORAGE OVERFLOW BIT FAILED - LINE #'

034565	042507	047524	040522
034566	043122	047440	042526
034567	044502	047514	020127
034568	044502	020124	040506
034569	046111	042105	026440
034570	046040	047111	020105
034571	020043	000040	

.EVEN

:MISCELLANEOUS MESSAGES

7799						
7798						
7797						
7796	034634	005015	040515	047111	TITLE: .ASCIZ	<15><12>'MAINDEC-11-DZDMM-B DH11 DIAGNOSTIC'<15><12>
7795	034642	042504	026503	030461		
7794	034650	042055	042132	046510		
7793	034656	041055	020040	044104		
7792	034664	030461	042040	040511		
7791	034700	047111	051517	044524		
7790	034706	006503	000012			
7789	034712	005015	042524	052123	TITLE2: .ASCIZ	<15><12>'TESTING DH11 # ' <15><12>
7788	034720	047111	020107	044104		
7787	034726	030461	021440	020040		
7786	034731	005015	000			
7785	034736	015	052012	050131	INMSG1: .ASCIZ	<15><12>'TYPE SCR ADDRESS FOR FIRST DH11'<15><12>
7784	034744	020105	041523	020122		
7783	034752	042101	051104	051505		
7782	034760	020123	047506	020122		
7781	034766	044506	051522	020124		
7780	034774	044104	030461	005015		
7779	034775	000				
7778	035002	015	052012	050131	INMSG2: .ASCIZ	<15><12>'TYPE VECTOR ADDRESS FOR FIRST DH11'<15><12>
7777	035010	020105	042526	052103		
7776	035016	051117	040440	042104		
7775	035024	042522	051523	042040		
7774	035032	051117	043040	051111		
7773	035040	052123	042040	030510		
7772	035044	030461	000012			
7771	035052	005015	054524	042520	INMSG3: .ASCIZ	<15><12>'TYPE DH11 DEVICE SELECTION PARAMETER'<15><12>
7770	035058	042040	030510	020061		
7769	035060	042504	044526	042503		
7768	035066	051440	046105	041505		
7767	035074	044524	047117	050040		
7766	035102	051101	046501	052105		
7765	035110	051105	005015	000		
7764	035118	015	044412	053116	INMSG4: .ASCIZ	<15><12>'INVALID DH11 SCR ADDRESS - TRY AGAIN'<15><12>
7763	035126	046101	042111	042040		
7762	035134	030510	020061	041523		
7761	035142	020122	042101	051104		
7760	035150	020123	020123	020055		
7759	035158	051124	020131	043501		
7758	035166	044501	006516	000012	INMSG5: .ASCIZ	<15><12>'INVALID DH11 VECTOR ADDRESS - TRY AGAIN'<15><12>
7757	035174	005015	047111	040526		
7756	035202	044514	020104	044104		
7755	035210	030461	053040	041505		
7754	035216	047524	020122	042101		
7753	035224	051104	051505	020123		
7752	035232	020055	051124	020131		
7751	035240	043501	044501	006516		
7750	035242	000012				
7749	035250	005015	054524	042520	INMSG6: .ASCIZ	<15><12>'TYPE LINE SELECTION PARAMETER'<15><12>
7748	035256	046040	047111	020105		
7747	035264	042523	042514	052103		
7746	035272	047511	020116	040520		
7745	035300	040522	042515	042524		
7744	035304	006522	000012			
7743	035304	005015	042504	051120	INMSG7: .ASCIZ	<15><12>'DEPRESS "CONTINUE" TO START TESTING'<15><12>

78047	035312	051505	020123	041442
78048	035320	047117	044524	052516
78049	035326	021105	052040	020117
78050	035334	052123	051101	020124
78051	035342	042524	052123	047111
78052	035350	006507	000012	
78054	035354	005015	054524	042520
78055	035362	047040	027117	047440
78056	035370	020106	042101	051104
78057	035376	051505	042523	020123
78058	035404	047450	052103	046101
78059	035412	020051	042502	053524
78060	035420	042505	020116	042526
78061	035426	052103	051117	020123
78062	035434	030450	020060	051117
78063	035442	031040	024460	005015
78064	035450	000		
78065	035451	116	020117	044104
78066	035456	030461	051447	053440
78067	035464	051105	020105	047506
78068	035472	047125	027104	005015
78069	035500	000		
78070	035501	116	020117	044104
78071	035506	051040	041505	044505
78072	035514	042526	020122	047111
78073	035522	042524	051122	050125
78074	035530	020124	041517	052503
78075	035536	051122	042105	006456
78076	035544	000012		
78077	035546	047516	042040	030515
78078	035554	025461	041102	044440
78079	035562	052116	051105	052522
78080	035570	052120	047440	041503
78081	035576	051125	042522	027104
78082	035604	005015	000	
78083	035607	040	020040	000
78084	035613	0015	042012	030510
78085	035620	026061	042040	030515
78086	035626	026461	041102	042040
78087	035634	053105	041511	020105
78088	035642	040515	035120	005015
78089	035650	005015	044104	030461
78090	035656	020040	042040	030510
78091	035664	020061	020040	046504
78092	035672	030461	041055	020102
78093	035700	020040	046504	030461
78094	035706	041055	102	
78095	035711	015	040412	051104
78096	035716	020122	020040	042526
78097	035724	052103	020040	020040
78098	035732	042101	051522	020040
78099	035740	020040	020040	042526
79000	035746	052103	005015	005015
79001	035754	000		
79002	035755	015	042012	030515

VCWC: .ASCIZ <15><12>'TYPE NO. OF ADDRESSES (OCTAL) BETWEEN VECTORS (10 OR 20)'<<15><1

MSG1: .ASCIZ /NO DM11'S WERE FOUND./<15><12>

MSG2: .ASCIZ 'NO DM RECEIVER INTERRUPT OCCURRED.'<<15><12>

MSG3: .ASCIZ 'NO DM11-BB INTERRUPT OCCURRED.'<<15><12>

SPACE: .ASCIZ ' '  
DEVMAP: .ASCII <15><12>'DM11, DM11-BB DEVICE MAP:'<15><12>

.ASCII <15><12>'DM11 DM11 DM11-BB DM11-BB'

.ASCIZ <15><12>'ADRS VECT ADRS VECT'<<15><12><15><12>

MSG4: .ASCIZ <15><12>'DM11-BB ERROR, RUN DZDMM DIAGNOSTIC'<<15><12>

7903	035762	026461	041102	042440
7904	035770	051122	051117	020054
7905	035776	052522	020116	055104
7906	036004	044104	020113	044504
7907	036012	043501	047516	052123
7908	036020	041511	005015	000
7909	036025	015	047012	020117
7910	036032	046504	030461	041055
7911	036040	020102	047506	047125
7912	036046	006504	000012	
7913				
7914				
7915				
7916				
7917				
7918				
7919				
7920				
7921				
7922				
7923				
7924				
7925				
7926				
7927				
7928				

MSG5: .ASCIZ <15><12>/NO DM11-BB FOUND/<15><12>

.EVEN  
;SIXTEEN CHAR COUNTERS USED BY THE AUTO ECHO TEST #3

RCNT: .BLKW 16.

;256. WORD RECEIVER INPUT BUFFER

RBUF: .BLKW 256.

;256(10) BYTE TRANSMITTER OUTPUT DATA BUFFER

.EVEN  
TBUF: .BLKB 256.

.ENC





























































LINE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
LINE	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
LINE	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45
LINE	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
LINE	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75
LINE	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
LINE	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105
LINE	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120
LINE	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135
LINE	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150
LINE	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165
LINE	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180
LINE	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195
LINE	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210
LINE	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225
LINE	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240
LINE	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
LINE	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270
LINE	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285
LINE	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300
LINE	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315
LINE	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330
LINE	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345
LINE	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360
LINE	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375
LINE	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390
LINE	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405
LINE	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420
LINE	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435
LINE	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450
LINE	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465
LINE	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480
LINE	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495
LINE	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510
LINE	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525
LINE	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540
LINE	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555
LINE	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570
LINE	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585
LINE	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600
LINE	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615
LINE	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630
LINE	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645
LINE	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660
LINE	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675
LINE	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690
LINE	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705
LINE	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720
LINE	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
LINE	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750
LINE	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765
LINE	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780
LINE	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795
LINE	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810
LINE	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825
LINE	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840
LINE	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855
LINE	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870
LINE	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885
LINE	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900
LINE	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915
LINE	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930
LINE	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945
LINE	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960
LINE	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975
LINE	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990
LINE	991	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005

ERRORS DETECTED: 0  
DEFAULT GLOBALS GENERATED: 0

\* DZDHMB=DHMMAC, DZDHMB  
RUN-TIME: 92 74 12 SECONDS  
RUN-TIME RATIO: 349/179=1.9  
CORE USED: 42K (83 PAGES)



