

DH11

LOGIC TEST
MD-11-DZDHC-B

EP-DZDHC-B-DL-A
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FICHE 1 OF 1

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MADE IN U.S.A.

The microfiche card displays a grid of 10 columns and 20 rows of small frames. Each frame contains a logic test diagram or data table. The diagrams include various symbols, lines, and text, typical of a logic test procedure. The right side of the card is mostly blank with some faint markings.

UNCLASSIFIED

1. ABSTRACT

THE D411 TRANSMITTER AND RECEIVER LOGIC TEST CHECKS
THE BASIC TRANSMITTER AND RECEIVER FUNCTIONS.
FUNCTIONS TESTED INCLUDE INTERRUPTS, OPERATION OF
TRANSMITTER NPR LOGIC, AND OPERATION OF RECEIVER SILO LOGIC.

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4.3 (CONT'D)

4.3.1.6 TYPE IN THE ADDRESS OF THE RECEIVER INTERRUPT VECTOR
FOR THE DH11 TO BE TESTED FOLLOWED BY <CARRIAGE RETURN>

NOTE: WORDS IN ANGLE BRACKETS, I.E. <CARRIAGE RETURN> MEAN THAT
THE TELETYPE KEY WITH THE NAMED FUNCTION SHOULD BE STRUCK

IF AN INCORRECT ADDRESS IS ENTERED, THE PROGRAM
WILL TYPE "?" AND WILL REPEAT THE SECOND MESSAGE OF 4.3.1.5
4.3.1.7 THE PROGRAM WILL TYPE "CONTROL REGISTER ADDRESS-"
AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.1.8 TYPE IN THE ADDRESS OF THE SYSTEM CONTROL REGISTER OF THE
DH11 TO BE TESTED FOLLOWED BY <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED, THE PROGRAM WILL TYPE
"?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.1.7
4.3.1.9 THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT IS
ABOUT TO START TESTING, AND THEN TESTING WILL BEGIN

4.3.2 PROGRAM RESTART WITH ALL SWITCHES DOWN

4.3.2.1 PERFORM 4.3.1.2 TO 4.3.1.5
4.3.2.2 THE PROGRAM WILL TYPE "DH11 XXXX"
AND WILL THEN CONTINUE AS DESCRIBED IN 4.3.1.9

4.3.3 PROGRAM RESTART WITH SW00=1

4.3.3.1 LOAD ADDRESS 000200
4.3.3.2 SET SW01=1
4.3.3.3 PRESS START
4.3.3.4 THE PROGRAM WILL PERFORM AS DESCRIBED IN 4.3.1.5 TO 4.3.1.9

4.3.4 PROGRAM RESTART WITH SW01=1

4.3.4.1 LOAD ADDRESS 000200
4.3.4.2 SET SW01=1
4.3.4.3 PRESS START
4.3.4.4 THE PROGRAM WILL TYPE "DH11 XXXX"
AND WILL THEN TYPE "TEST PC-" AND WILL WAIT FOR AN INPUT
FROM THE TELETYPE KEYBOARD
4.3.4.5 TYPE IN THE ADDRESS OF THE TEST AT WHICH THE PROGRAM IS TO
BE STARTED FOLLOWED BY <CARRIAGE RETURN>
4.3.4.6 THE PROGRAM WILL TYPE R TO INDICATE THAT IT HAS STARTED
AND WILL START TESTING AT THE SELECTED TEST.

NOTE: CARE MUST BE TAKEN WHEN THIS FEATURE IS USED, SINCE
THERE IS NO PROTECTION AGAINST SELECTING AN ADDRESS THAT
IS IN THE MIDDLE OF A TEST

NOTE: IF IT IS DESIRED TO LOOP ON THE TEST THAT IS SELECTED
SET SW14=1 BEFORE ENTERING THE TEST ADDRESS

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5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

SW15=1, HALT ON ERROR
SW14=1, LOOP ON CURRENT TEST
SW13=1, SUPPRESS ERROR TYPEOUT
SW11=1, INHIBIT ITERATIONS
SW10=1, ESCAPE TO NEXT TEST ON ERROR
SW09=1, FREEZE VARIABLE PARAMETER IN CURRENT TEST
SW01=1, START PROGRAM AT SELECTED TEST
SW00=1, CHANGE PARAMETERS AT PROGRAM RESTART

5.2 SUBROUTINE ABSTRACTS

5.2.1 TRAPCATCHER (LOCATIONS 000000-000776)

THIS ROUTINE IS USED TO INTERCEPT UNEXPECTED INTERRUPTS AND TRAPS. THE AREA FROM 000000-000776 IS LOADED WITH THE FOLLOWING SEQUENCE

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IF AN UNEXPECTED INTERRUPT OR TRAP OCCURS, THE PROGRAM WILL HALT WITH THE PC 2 GREATER THAN THE ADDRESS TO WHICH THE PROGRAM TRAPPED. THE PROCESSOR STACK MAY BE EXAMINED TO DETERMINE WHERE THE PROGRAM WAS WHEN THE TRAP OR INTERRUPT OCCURED.

5.2.2 START (PROGRAM INITIALIZATION)

THIS ROUTINE INITIALIZES ALL PROGRAM FLAGS AND COUNTERS, TYPES THE PROGRAM TITLE MESSAGE, AND INPUTS THE VECTOR AND CONTROL REGISTER ADDRESSES OF THE DH11 TO BE TESTED.

5.2.3 BEGIN (PROGRAM START AND RESTART)

THIS ROUTINE IS ENTERED IMMEDIATLY AFTER "START" AND EACH TIME A PROGRAM PASS HAS BEEN COMPLETED. THE ROUTINE SETS UP THE PROCESSOR STACK AND STATUS WORD AND THEN TRANSFERS CONTROL TO THE TEST AT WHICH TESTING WILL BEGIN. IF SW01=0 WHEN THIS ROUTINE IS ENTERED TESTING WILL START AT T1 (TEST 1). IF SW01=1 WHEN THIS ROUTINE IS ENTERED, TESTING WILL START AT THE PC ENTERED FROM THE TELETYPE KEYBOARD.

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5.2.4 EOP (END OF PASS)

THIS ROUTINE IS ENTERED ONCE PER PASS AFTER ALL TESTS HAVE BEEN COMPLETED. THIS ROUTINE TYPES THE MAINDEC IDENTIFICATION CODE OF THE PROGRAM, CLEARS ERROR FLAGS AND UPDATES THE PASS COUNT. IF THE PROGRAM WAS LOADED UNDER ACT11 OR DDP, THE ROUTINE CHECKS FOR RETURN TO THE ACT11 OR DDP MONITOR. IF THE PROGRAM IS NOT UNDER MONITOR CONTROL, THE ROUTINE TRANSFERS TO BEGIN.

5.2.5 SCOPER (SCOPE LOOP AND ITERATION HANDLER)

THIS ROUTINE IS ENTERED EACH TIME A TEST IS COMPLETED. THE ROUTINE CHECKS FOR THE FOLLOWING UPON ENTRY
A) IF SW10=1, THE ROUTINE WILL TRANSFER TO THE NEXT TEST IN SEQUENCE, AFTER CLEARING ERROR FLAGS.
B) IF SW11=1, THE ROUTINE WILL TRANSFER TO THE NEXT TEST SEQUENCE, AFTER CLEARING ERROR FLAGS.
C) IF SW14=1, THE ROUTINE WILL LOOP ON THE CURRENT TEST REGARDLESS OF THE ITERATION COUNT.

IF NONE OF THE ABOVE IS TRUE, THE ROUTINE WILL ADD 1 TO THE COUNT OF TEST ITERATIONS, AND COMPARE THIS VALUE TO THE NUMBER OF ITERATIONS THAT SHOULD BE PERFORMED. IF THESE NUMBERS ARE EQUAL, THE ROUTINE WILL TRANSFER TO THE NEXT TEST IN SEQUENCE. IF THE NUMBERS ARE NOT EQUAL, THE TEST CURRENTLY IN PROGRESS WILL BE REPEATED.

5.2.6 SCOP1R (FREEZE ON CURRENT DATA)

THE CALL TO THIS ROUTINE FOLLOWS IMMEDIATELY AFTER THE CALL TO THE ERROR HANDLER IN THOSE TESTS THAT HAVE VARIABLE PARAMETERS. THIS ROUTINE IS ALWAYS ENTERED IN THOSE TESTS, WHETHER OR NOT AN ERROR OCCURS. IF SW09=1, THE ROUTINE WILL TRANSFER CONTROL BACK TO THE TEST AT A POINT WHICH WILL ALLOW REPEATING THE FUNCTION UNDER TEST CONTINUOUSLY WITH THE SAME DATA. IF THIS OPTION IS SELECTED, THE ROUTINE "SCOPER" IS NEVER ENTERED AND ITERATION COUNTS WILL NOT BE UPDATED.

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5.2.7 ERRORS (ERROR HANDLER)

THIS ROUTINE IS ENTERED UPON ERROR DETECTION ONLY. WITH ALL CONSOLE SWITCHES DOWN, THE ROUTINE PROCEEDS AS FOLLOWS:

- A) THE PC OF THE INSTRUCTION THAT CALLED THE ERROR HANDLER IS ACCESSED THRU THE STACK, AND THEN THE EMT INSTRUCTION ITSELF IS FETCHED. THE 8 LSB OF THE EMT INSTRUCTION ARE THE ERROR CODE. THIS CODE IS USED TO ACCESS A TABLE OF ERROR MESSAGES AND ERROR DATA STORAGE LOCATIONS.
- B) IF THE TEST THAT FAILED DID NOT FAIL PREVIOUSLY DURING THIS PASS, A COMPLETE ERROR REPORT IS MADE IF THE TEST THAT FAILED FAILED MOR THAT ONCE DURING THE CURRENT PASS, ONLY THE DATA RELATING TO THE FAILUER IS TYPED. IF SW13=1, NO ERROR TYPEOUT IS MADE.
- C) THE ROUTINE NOW CHECKS FOR HALT ON ERROR. IF SW15=1 THE PROGRAM WILL HALT WITH THE PC OF THE CALL TO THE ERROR ROUTINE IN RO. IF SW15=0, THE PROGRAM WILL NOT HALT, BUT WILL CHECK FOR ESCAPE TO NEXT TEST.
- D) IF SW10=0, THE ROUTINE WILL RETURN TO THE TEST IN PROGRESS. IF SW10=1, THE ROUTINE WILL ABORT THE CURRENT TEST, AND TRANSFER TO THE NEXT TEST IN SEQUENCE, THRU THE ROUTINE "SCOPER".

5.2.8 TRPSRV (TRAP DECODE AND DISPATCH)

THIS ROUTINE DECODES THE 8 LSB OF THE TRAP INSTRUCTION THAT CAUSED TH PROGRAM INTERRUPT, AND TRANSFERS CONTROL TO THE ROUTINE THRU THE TABLE "TRPTAB" USING THE 8 LSB OF THE TRAP INSTRUCTION AS AN OFFSET TO THE POINTER TO THE ROUTINE TO BE ENTERED.

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- 5.3 PROGRAM AND OR OPERATOR ACTION
- 5.3.1 PROGRAM START WITH ALL SWITCHES DOWN
- 5.3.1.1 REFER TO SECTIONS 4.3.1 AND 4.3.2 FOR INITIAL PROGRAM BEHAVIOR.
- 5.3.1.2 AFTER "R" HAS BEEN TYPED BY THE PROGRAM, TEST EXECUTION WILL BEGIN. EACH TEST WILL BE REPEATED A SELECTED NUMBER OF ITERATIONS (SEE LISTING FOR EXACT NUMBER FOR EACH TEST) AND THEN THE PROGRAM WILL PROCEED TO THE NEXT TEST.
- 5.3.1.3 WHEN ALL ITERATIONS HAVE BEEN COMPLETED, THE PROGRAM WILL TYPE "DZDHX" AND THEN RESTART TESTING AT TEST 1 (LOCATION T1 IN THE PROGRAM).
- 5.3.1.4 IF AN ERROR OCCURS, THE PROGRAM WILL TYPE AN APPROPRIATE ERROR MESSAGE, AND THEN CONTINUE THE TEST IN PROGRESS.
- 5.3.2 PROGRAM START WITH SW00=1
THE PROGRAM WILL PERFORM AS DESCRIBED IN 4.3.1 AND 5.3.1
- 5.3.3 PROGRAM START WITH SW01=1
- 5.3.3.1 REFER TO SECTION 4.3.4 FOR INITIAL PROGRAM BEHAVIOR
- 5.3.3.2 TEST EXECUTION WILL START AT THE ADDRESS SPECIFIED AND WILL CONTINUE AS DESCRIBED IN 5.3.1.2
- 5.3.3.3 AFTER "DZDHX" HAS BEEN TYPED, THE PROGRAM WILL RESUME TESTING AT TEST 1
- 5.3.4 PROGRAM OPERATION WITH SW15=1
SAME AS 5.3.1, EXCEPT THAT IN THE CASE OF AN ERROR, THE PROGRAM WILL HALT AFTER THE ERROR TYPEOUT, AND THE PC+2 OF THE CALL TO THE ERROR ROUTINE WILL BE DISPLAYED IN RO.
- 5.3.5 PROGRAM OPERATION WITH SW13=1
SAME AS 5.3.1 EXCEPT THAT NO ERROR TYPEOUTS WILL OCCUR
- 5.3.6 PROGRAM OPERATION WITH SW11=1
SAME AS 5.3.1 EXCEPT THAT EACH TEST WILL BE REPEATED ONCE ONLY
- 5.3.7 PROGRAM OPERATION WITH SW10=1
SAME AS 5.3.1, EXCEPT THAT IN THE CASE OF AN ERROR THE CURRENT TEST WILL BE ABORTED, AND THE PROGRAM WILL PROCEED TO THE NEXT TEST IN SEQUENCE.

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5. (CONT'D)

5.3.8 PROGRAM OPERATION WITH SW14=1, OR SW09=1

THESE FUNCTIONS ARE NORMALLY USED FOR TROUBLE SHOOTING.
 SEE SECTION 6.3 FOR THEIR USE.

6. ERRORS

6.1 ERROR HALTS

THE ERROR MESSAGE FORMAT FOR ALL ERROR TYPEOUTS
 IS AS FOLLOWS

PC+2 MESSAGE
 HEADER (IF APPLICABLE)
 DATA (IF APPLICABLE)

WHERE

PC+2 IS THE ADDRESS OF THE CALL TO THE ERROR HANDLER + 2
 MESSAGE IS AN ASCII MESSAGE DESCRIBING (BRIEFLY) THE FAILURE
 HEADER IS A DESCRIPTION OF THE DATA TO FOLLOW
 DATA IS OCTAL INFORMATION RELATING TO THE CAUSE OF THE FAILURE
 IF THE SAME ERROR OCCURS IN A GIVEN TEST ON THE SAME
 PASS, AND IF DATA IS ASSOCIATED WITH THAT ERROR, ONLY
 DATA IS TYPE ON SUCCEEDING ERROR TYPEOUTS

IF NO DATA IS ASSOCIATED WITH THE ERROR
 THE COMPLETE ERROR MESSAGE IS TYPED.

6.1.1 ERROR DESCRIPTIONS

SEE LISTING FOR DETAILS OF ERRORS

6.2 ERROR RECOVERY

6.2.1 SW15=0

IF THE PROGRAM IS RUN WITH SW15=0, NO OPERATOR ACTION IS
 REQUIRED TO CONTINUE TESTING

6.2.2 SW15=1

IF THE PROGRAM IS RUN WITH SW15=1, TO CONTINUE TESTING
 AFTER THE PROGRAM HAS HALTED, PRESS THE PROCESSOR
 CONSOLE CONTINUE SWITCH

6.2.3 ILLEGAL INTERRUPTS

IF AN INTERRUPT OCCURS TO A VECTOR ADDRESS NOT
 SELECTED DURING PROGRAM INITIALIZATION, THE PROGRAM WILL
 HALT IN THE TRAPCATCHER. THE ADDRESS AT WHICH
 THE PROGRAM HALTS IS 2 GREATER THAN THE ADDRESS
 TO WHICH THE INTERRUPT OCCURED. THE PROGRAM MUST BE
 RESTARTED AT 200 TO RECOVER FROM THIS ERROR.

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6.3 SCOPE LOOPING

6.3.1 TO SCOPE ON A SPECIFIC TEST, SET SW14=1 AND SW13=1
THIS WILL CAUSE THE PROGRAM TO CONTINUOUSLY LOOP ON THE
SAME TEST, AND WILL CAUSE ALL ERROR TYPEOUTS TO BE INHIBITED

6.3.2 TO SCOPE ON A SPECIFIC VALUE OF A PARAMETER WITHIN
A TEST, SET SW09=1 TO FREEZE THE DATA
(SEE LISTING FOR THOSE TESTS THAT INCORPORATE THIS FEATURE)

6. (CONT'D)

6.3.3 PROGRAM START TO SCOPE LOOP ON SELECTED TEST

PERFORM SECTION 4.3.4 WITH SW14=1

7. RESTRICTIONS

7.1 STARTING

THE DH11 TEST CARD MUST BE INSTALLED

7.2 RUNNING

NONE

8. MISCELLANEOUS

8.1 EXECUTION TIME

THE TIME FOR ONE PASS OF THE PROGRAM (END OF
TYPEOUT OF DZDHX TO END OF TYPEOUT OF DZDHX)
IS GIVEN FOR VARIOUS PROCESSORS IN THE TABLE BELOW

PROCESSOR	TIME
PDP-11/05,10	
PDP-11/20	
PDP-11/40	
PDP-11/45	

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9. PROGRAM DESCRIPTION

THE FIRST GROUP OF TESTS VERIFIES THAT NO INTERRUPTS OCCUR WITH INTERRUPT ENABLES SET FOR EACH INTERRUPTING FUNCTION AND THE ASSOCIATED DONE BIT OR FLAG FOR THAT FUNCTION CLEARED.

THE NEXT GROUP OF TESTS VERIFIES THAT AN INTERRUPT DOES OCCUR IF A SPECIFIC DONE BIT OR FLAG IS SET, ALONG WITH ITS CORRESPONDING INTERRUPT ENABLE. AT THIS TIME, INTERRUPTS TO THE CORRECT VECTOR ARE TESTED. IF AN INTERRUPT OCCURS TO ANY VECTOR OTHER THAN THOSE SELECTED AT PROGRAM START, THE PROGRAM WILL HALT IN THE TRAPCATCHER IN A LOCATION 2 GREATER THAN THE ADDRESS OF THE VECTOR TO WHICH THE INTERRUPT OCCURED.

THE NEXT GROUP OF TESTS CHECKS TRANSMITTER NPR AND INTERRUPT LOGIC OPERATION FOR EACH LINE, IN AN INDIVIDUAL TEST FOR EACH LINE. THE BYTE COUNT FOR THE SELECTED LINE IS SET TO -1 (FOR 1 CHARACTER TRANSMISSION) AND THE BUS ADDRESS MEMORY LOCATION FOR THAT LIN IS SET TO 0. THE BAR BIT FOR THE SELECTED LINE IS SET, TRANSMITTER INTERRUPT ENABLE IS SET, AND THE PROCESSOR STATUS WORD IS CLEARED TO ALLOW INTERRUPTS TO OCCUR. A DELAY LOOP IS THEN ENTERED, AND IF THE DELAY TIMES OUT BEFORE AN INTERRUPT OCCURS, AN ERROR MESSAGE IS TYPED. IF AN INTERRUPT DOES OCCUR, THE CONTROL REGISTER IS TESTED TO SEE IF THE TRANSMITTER DONE BIT HAS BEEN SET, THE BAR REGISTER IS CHECKED TO SEE THAT THE BAR BIT FOR THE SELECTED LIN HAS CLEARED, BYTE COUNT IS CHECKED TO SEE THAT IT WENT TO 0 AND THE BUS ADDRESS REGISTER FOR THE SELECTED LINE IS CHECKED TO SEE THAT IT INCREMENTED TO 1.

THE NEXT GROUP OF TESTS VERIFIES THAT A SINGLE SELECTED LINE WILL PERFORM TRANSMIT FUNCTIONS WITHOUT AFFECTING ANY OTHER LINE. THIS IS DONE BY SETTING ALL BYTE COUNTS TO -1, AND VERIFYING THAT ONLY THE LINE SELECTED FOR TRANSMISSION HAD CHANGES MADE IN BYTE COUNT AND BUS ADDRESS WHEN TRANSMISSION HAS BEEN COMPLETED.

THE NEXT TEST VERIFIES THAT A SINGLE CHARACTER CAN BE LOADED INTO THE SILO (IN MAINTENANCE MODE). THE TEST IS MADE WITH INTERRUPTS ENABLED AND CHECKS ARE MADE TO DETERMINE IF RECEIVER DONE WAS SET, IF THE SILO FILL LEVEL REGISTER WAS INCREMENTED, AND IF THE DATA RECEIVED IN MAINTENANCE MODE WAS CORRECT.

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9. (CONT'D)

THE NEXT TEST VERIFIES THAT FROM 1 TO 63 CHARACTERS CAN BE LOADED INTO THE SILO, AND THAT THE SILO FILL LEVEL REGISTER INDICATES THE CORRECT NUMBER OF CHARACTERS IN THE SILO.

THE NEXT TEST VERIFIES THAT 64 CHARACTERS CAN BE LOADED INTO THE SILO, FROM 1 TO 64 CHARACTERS CAN BE READ OUT OF THE SILO, AND THAT THE SILO FILL REGISTER INDICATES THE NUMBER OF CHARACTERS REMAINING IN THE SILO.

THE FINAL TEST VERIFIES THAT THE CHARACTER AVAILABLE FLAG WILL NOT BE SET UNTIL THE SILO FILL LEVEL EXCEEDS THE SILO ALARM LEVEL, FOR ALL ALARM LEVELS 0-63.

10. LISTING

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;DH11 TRANSMITTER AND RECEIVER BASIC LOGIC TEST
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```
;STARTING PROCEDURE
;LOAD PROGRAM
;LOAD ADDRESS 000200
;PRESS START
;PROGRAM WILL TYPE DH11 TRANSMITTER AND RECEIVER BASIC LOGIC TEST
;PROGRAM WILL TYPE "VECTOR ADDRESS-"
;TYPE IN THE ADDRESS OF THE RECEIVER INTERRUPT VECTOR
;FOR THE DH11 TO BE TESTED, FOLLOWED BY <CARRIAGE RETURN>
;PROGRAM WILL TYPE "CONTROL REGISTER ADDRESS-"
;TYPE IN THE ADDRESS OF THE SYSTEM CONTROL REGISTER
;FOR THE DH11 TO BE TESTED, FOLLOWED BY <CARRIAGE RETURN>
;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
;AT THE END OF A PASS, PROGRAM WILL TYPE " DZDHC "
;AND THEN RESUM TESTING
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;SWITCH REGISTER OPTIONS

100000
 040000
 020000
 010000
 004000
 002000
 001000
 000400
 000100
 000040
 000020

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SW15=100000      ;=1,HALT ON ERROR
SW14=40000       ;=1,LOOP ON CURRENT TEST
SW13=20000       ;=1,INHIBIT ERROR TYPEOUT
SW12=10000
SW11=4000        ;=1,INHIBIT ITERATIONS
SW10=2000        ;=1,ESCAPE TO NEXT TEST ON ERROR
SW09=1000        ;=1,LOOP WITH CURRENT DATA
SW08=400
SW06=100
SW05=40
SW04=20
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NO1.

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 14
DZDHCB.PFC

553 000010
554 000004
555 000002
556 000001
557

SW03=10
SW02=4
SW01=2
SW00=1

;RESTART PROGRAM AT SELECTED TEST
;RESELECT VECTOR AND CONTROL REGISTER
;ADDRESS AFTER PROGRAM RESTART

661	000154	000156	.+2	: UNEXPECTED TRAP TO THIS LOCATION
662	000156	000000	HALT	: EXAMINE STACK TO FIND CAUSE
663	000160	000162	.+2	: UNEXPECTED TRAP TO THIS LOCATION
664	000162	000000	HALT	: EXAMINE STACK TO FIND CAUSE
665	000164	000166	.+2	: UNEXPECTED TRAP TO THIS LOCATION
666	000166	000000	HALT	: EXAMINE STACK TO FIND CAUSE
667	000170	000172	.+2	: UNEXPECTED TRAP TO THIS LOCATION
668	000172	000000	HALT	: EXAMINE STACK TO FIND CAUSE
669	000174	000176	.+2	: UNEXPECTED TRAP TO THIS LOCATION
670	000176	000000	HALT	: EXAMINE STACK TO FIND CAUSE
671	000200	000202	.+2	: UNEXPECTED TRAP TO THIS LOCATION
672	000202	000000	HALT	: EXAMINE STACK TO FIND CAUSE
673	000204	000206	.+2	: UNEXPECTED TRAP TO THIS LOCATION
674	000206	000000	HALT	: EXAMINE STACK TO FIND CAUSE
675	000210	000212	.+2	: UNEXPECTED TRAP TO THIS LOCATION
676	000212	000000	HALT	: EXAMINE STACK TO FIND CAUSE
677	000214	000216	.+2	: UNEXPECTED TRAP TO THIS LOCATION
678	000216	000000	HALT	: EXAMINE STACK TO FIND CAUSE
679	000220	000222	.+2	: UNEXPECTED TRAP TO THIS LOCATION
680	000222	000000	HALT	: EXAMINE STACK TO FIND CAUSE
681	000224	000226	.+2	: UNEXPECTED TRAP TO THIS LOCATION
682	000226	000000	HALT	: EXAMINE STACK TO FIND CAUSE
683	000230	000232	.+2	: UNEXPECTED TRAP TO THIS LOCATION
684	000232	000000	HALT	: EXAMINE STACK TO FIND CAUSE
685	000234	000236	.+2	: UNEXPECTED TRAP TO THIS LOCATION
686	000236	000000	HALT	: EXAMINE STACK TO FIND CAUSE
687	000240	000242	.+2	: UNEXPECTED TRAP TO THIS LOCATION
688	000242	000000	HALT	: EXAMINE STACK TO FIND CAUSE
689	000244	000246	.+2	: UNEXPECTED TRAP TO THIS LOCATION
690	000246	000000	HALT	: EXAMINE STACK TO FIND CAUSE
691	000250	000252	.+2	: UNEXPECTED TRAP TO THIS LOCATION
692	000252	000000	HALT	: EXAMINE STACK TO FIND CAUSE
693	000254	000256	.+2	: UNEXPECTED TRAP TO THIS LOCATION
694	000256	000000	HALT	: EXAMINE STACK TO FIND CAUSE
695	000260	000262	.+2	: UNEXPECTED TRAP TO THIS LOCATION
696	000262	000000	HALT	: EXAMINE STACK TO FIND CAUSE
697	000264	000266	.+2	: UNEXPECTED TRAP TO THIS LOCATION
698	000266	000000	HALT	: EXAMINE STACK TO FIND CAUSE
699	000270	000272	.+2	: UNEXPECTED TRAP TO THIS LOCATION
700	000272	000000	HALT	: EXAMINE STACK TO FIND CAUSE
701	000274	000276	.+2	: UNEXPECTED TRAP TO THIS LOCATION
702	000276	000000	HALT	: EXAMINE STACK TO FIND CAUSE
703	000300	000302	.+2	: UNEXPECTED TRAP TO THIS LOCATION
704	000302	000000	HALT	: EXAMINE STACK TO FIND CAUSE
705	000304	000306	.+2	: UNEXPECTED TRAP TO THIS LOCATION
706	000306	000000	HALT	: EXAMINE STACK TO FIND CAUSE
707	000310	000312	.+2	: UNEXPECTED TRAP TO THIS LOCATION
708	000312	000000	HALT	: EXAMINE STACK TO FIND CAUSE
709	000314	000316	.+2	: UNEXPECTED TRAP TO THIS LOCATION
710	000316	000000	HALT	: EXAMINE STACK TO FIND CAUSE
711	000320	000322	.+2	: UNEXPECTED TRAP TO THIS LOCATION
712	000322	000000	HALT	: EXAMINE STACK TO FIND CAUSE
713	000324	000326	.+2	: UNEXPECTED TRAP TO THIS LOCATION
714	000326	000000	HALT	: EXAMINE STACK TO FIND CAUSE
715	000330	000332	.+2	: UNEXPECTED TRAP TO THIS LOCATION
716	000332	000000	HALT	: EXAMINE STACK TO FIND CAUSE

717	000334	000336	.+2	:UNEXPECTED TRAP TO THIS LOCATION
718	000336	000000	HALT	:EXAMINE STACK TO FIND CAUSE
719	000340	000342	.+2	:UNEXPECTED TRAP TO THIS LOCATION
720	000342	000000	HALT	:EXAMINE STACK TO FIND CAUSE
721	000344	000346	.+2	:UNEXPECTED TRAP TO THIS LOCATION
722	000346	000000	HALT	:EXAMINE STACK TO FIND CAUSE
723	000350	000352	.+2	:UNEXPECTED TRAP TO THIS LOCATION
724	000352	000000	HALT	:EXAMINE STACK TO FIND CAUSE
725	000354	000356	.+2	:UNEXPECTED TRAP TO THIS LOCATION
726	000356	000000	HALT	:EXAMINE STACK TO FIND CAUSE
727	000360	000362	.+2	:UNEXPECTED TRAP TO THIS LOCATION
728	000362	000000	HALT	:EXAMINE STACK TO FIND CAUSE
729	000364	000366	.+2	:UNEXPECTED TRAP TO THIS LOCATION
730	000366	000000	HALT	:EXAMINE STACK TO FIND CAUSE
731	000370	000372	.+2	:UNEXPECTED TRAP TO THIS LOCATION
732	000372	000000	HALT	:EXAMINE STACK TO FIND CAUSE
733	000374	000376	.+2	:UNEXPECTED TRAP TO THIS LOCATION
734	000376	000000	HALT	:EXAMINE STACK TO FIND CAUSE
735	000400	000402	.+2	:UNEXPECTED TRAP TO THIS LOCATION
736	000402	000000	HALT	:EXAMINE STACK TO FIND CAUSE
737	000404	000406	.+2	:UNEXPECTED TRAP TO THIS LOCATION
738	000406	000000	HALT	:EXAMINE STACK TO FIND CAUSE
739	000410	000412	.+2	:UNEXPECTED TRAP TO THIS LOCATION
740	000412	000000	HALT	:EXAMINE STACK TO FIND CAUSE
741	000414	000416	.+2	:UNEXPECTED TRAP TO THIS LOCATION
742	000416	000000	HALT	:EXAMINE STACK TO FIND CAUSE
743	000420	000422	.+2	:UNEXPECTED TRAP TO THIS LOCATION
744	000422	000000	HALT	:EXAMINE STACK TO FIND CAUSE
745	000424	000426	.+2	:UNEXPECTED TRAP TO THIS LOCATION
746	000426	000000	HALT	:EXAMINE STACK TO FIND CAUSE
747	000430	000432	.+2	:UNEXPECTED TRAP TO THIS LOCATION
748	000432	000000	HALT	:EXAMINE STACK TO FIND CAUSE
749	000434	000436	.+2	:UNEXPECTED TRAP TO THIS LOCATION
750	000436	000000	HALT	:EXAMINE STACK TO FIND CAUSE
751	000440	000442	.+2	:UNEXPECTED TRAP TO THIS LOCATION
752	000442	000000	HALT	:EXAMINE STACK TO FIND CAUSE
753	000444	000446	.+2	:UNEXPECTED TRAP TO THIS LOCATION
754	000446	000000	HALT	:EXAMINE STACK TO FIND CAUSE
755	000450	000452	.+2	:UNEXPECTED TRAP TO THIS LOCATION
756	000452	000000	HALT	:EXAMINE STACK TO FIND CAUSE
757	000454	000456	.+2	:UNEXPECTED TRAP TO THIS LOCATION
758	000456	000000	HALT	:EXAMINE STACK TO FIND CAUSE
759	000460	000462	.+2	:UNEXPECTED TRAP TO THIS LOCATION
760	000462	000000	HALT	:EXAMINE STACK TO FIND CAUSE
761	000464	000466	.+2	:UNEXPECTED TRAP TO THIS LOCATION
762	000466	000000	HALT	:EXAMINE STACK TO FIND CAUSE
763	000470	000472	.+2	:UNEXPECTED TRAP TO THIS LOCATION
764	000472	000000	HALT	:EXAMINE STACK TO FIND CAUSE
765	000474	000476	.+2	:UNEXPECTED TRAP TO THIS LOCATION
766	000476	000000	HALT	:EXAMINE STACK TO FIND CAUSE
767	000500	000502	.+2	:UNEXPECTED TRAP TO THIS LOCATION
768	000502	000000	HALT	:EXAMINE STACK TO FIND CAUSE
769	000504	000506	.+2	:UNEXPECTED TRAP TO THIS LOCATION
770	000506	000000	HALT	:EXAMINE STACK TO FIND CAUSE
771	000510	000512	.+2	:UNEXPECTED TRAP TO THIS LOCATION
772	000512	000000	HALT	:EXAMINE STACK TO FIND CAUSE

773	000514	000516	.+2	:UNEXPECTED TRAP TO THIS LOCATION
774	000516	000000	HALT	:EXAMINE STACK TO FIND CAUSE
775	000520	000522	.+2	:UNEXPECTED TRAP TO THIS LOCATION
776	000522	000000	HALT	:EXAMINE STACK TO FIND CAUSE
777	000524	000526	.+2	:UNEXPECTED TRAP TO THIS LOCATION
778	000526	000000	HALT	:EXAMINE STACK TO FIND CAUSE
779	000530	000532	.+2	:UNEXPECTED TRAP TO THIS LOCATION
780	000532	000000	HALT	:EXAMINE STACK TO FIND CAUSE
781	000534	000536	.+2	:UNEXPECTED TRAP TO THIS LOCATION
782	000536	000000	HALT	:EXAMINE STACK TO FIND CAUSE
783	000540	000542	.+2	:UNEXPECTED TRAP TO THIS LOCATION
784	000542	000000	HALT	:EXAMINE STACK TO FIND CAUSE
785	000544	000546	.+2	:UNEXPECTED TRAP TO THIS LOCATION
786	000546	000000	HALT	:EXAMINE STACK TO FIND CAUSE
787	000550	000552	.+2	:UNEXPECTED TRAP TO THIS LOCATION
788	000552	000000	HALT	:EXAMINE STACK TO FIND CAUSE
789	000554	000556	.+2	:UNEXPECTED TRAP TO THIS LOCATION
790	000556	000000	HALT	:EXAMINE STACK TO FIND CAUSE
791	000560	000562	.+2	:UNEXPECTED TRAP TO THIS LOCATION
792	000562	000000	HALT	:EXAMINE STACK TO FIND CAUSE
793	000564	000566	.+2	:UNEXPECTED TRAP TO THIS LOCATION
794	000566	000000	HALT	:EXAMINE STACK TO FIND CAUSE
795	000570	000572	.+2	:UNEXPECTED TRAP TO THIS LOCATION
796	000572	000000	HALT	:EXAMINE STACK TO FIND CAUSE
797	000574	000576	.+2	:UNEXPECTED TRAP TO THIS LOCATION
798	000576	000000	HALT	:EXAMINE STACK TO FIND CAUSE
799	000600	000602	.+2	:UNEXPECTED TRAP TO THIS LOCATION
800	000602	000000	HALT	:EXAMINE STACK TO FIND CAUSE
801	000604	000606	.+2	:UNEXPECTED TRAP TO THIS LOCATION
802	000606	000000	HALT	:EXAMINE STACK TO FIND CAUSE
803	000610	000612	.+2	:UNEXPECTED TRAP TO THIS LOCATION
804	000612	000000	HALT	:EXAMINE STACK TO FIND CAUSE
805	000614	000616	.+2	:UNEXPECTED TRAP TO THIS LOCATION
806	000616	000000	HALT	:EXAMINE STACK TO FIND CAUSE
807	000620	000622	.+2	:UNEXPECTED TRAP TO THIS LOCATION
808	000622	000000	HALT	:EXAMINE STACK TO FIND CAUSE
809	000624	000626	.+2	:UNEXPECTED TRAP TO THIS LOCATION
810	000626	000000	HALT	:EXAMINE STACK TO FIND CAUSE
811	000630	000632	.+2	:UNEXPECTED TRAP TO THIS LOCATION
812	000632	000000	HALT	:EXAMINE STACK TO FIND CAUSE
813	000634	000536	.+2	:UNEXPECTED TRAP TO THIS LOCATION
814	000636	000000	HALT	:EXAMINE STACK TO FIND CAUSE
815	000640	000642	.+2	:UNEXPECTED TRAP TO THIS LOCATION
816	000642	000000	HALT	:EXAMINE STACK TO FIND CAUSE
817	000644	000646	.+2	:UNEXPECTED TRAP TO THIS LOCATION
818	000646	000000	HALT	:EXAMINE STACK TO FIND CAUSE
819	000650	000652	.+2	:UNEXPECTED TRAP TO THIS LOCATION
820	000652	000000	HALT	:EXAMINE STACK TO FIND CAUSE
821	000654	000656	.+2	:UNEXPECTED TRAP TO THIS LOCATION
822	000656	000000	HALT	:EXAMINE STACK TO FIND CAUSE
823	000660	000662	.+2	:UNEXPECTED TRAP TO THIS LOCATION
824	000662	000000	HALT	:EXAMINE STACK TO FIND CAUSE
825	000664	000666	.+2	:UNEXPECTED TRAP TO THIS LOCATION
826	000666	000000	HALT	:EXAMINE STACK TO FIND CAUSE
827	000670	000672	.+2	:UNEXPECTED TRAP TO THIS LOCATION
828	000672	000000	HALT	:EXAMINE STACK TO FIND CAUSE

829	000674	000676	.+2	:UNEXPECTED TRAP TO THIS LOCATION
830	000676	000000	HALT	:EXAMINE STACK TO FIND CAUSE
831	000700	000702	.+2	:UNEXPECTED TRAP TO THIS LOCATION
832	000702	000000	HALT	:EXAMINE STACK TO FIND CAUSE
833	000704	000706	.+2	:UNEXPECTED TRAP TO THIS LOCATION
834	000706	000000	HALT	:EXAMINE STACK TO FIND CAUSE
835	000710	000712	.+2	:UNEXPECTED TRAP TO THIS LOCATION
836	000712	000000	HALT	:EXAMINE STACK TO FIND CAUSE
837	000714	000716	.+2	:UNEXPECTED TRAP TO THIS LOCATION
838	000716	000000	HALT	:EXAMINE STACK TO FIND CAUSE
839	000720	000722	.+2	:UNEXPECTED TRAP TO THIS LOCATION
840	000722	000000	HALT	:EXAMINE STACK TO FIND CAUSE
841	000724	000726	.+2	:UNEXPECTED TRAP TO THIS LOCATION
842	000726	000000	HALT	:EXAMINE STACK TO FIND CAUSE
843	000730	000732	.+2	:UNEXPECTED TRAP TO THIS LOCATION
844	000732	000000	HALT	:EXAMINE STACK TO FIND CAUSE
845	000734	000736	.+2	:UNEXPECTED TRAP TO THIS LOCATION
846	000736	000000	HALT	:EXAMINE STACK TO FIND CAUSE
847	000740	000742	.+2	:UNEXPECTED TRAP TO THIS LOCATION
848	000742	000000	HALT	:EXAMINE STACK TO FIND CAUSE
849	000744	000746	.+2	:UNEXPECTED TRAP TO THIS LOCATION
850	000746	000000	HALT	:EXAMINE STACK TO FIND CAUSE
851	000750	000752	.+2	:UNEXPECTED TRAP TO THIS LOCATION
852	000752	000000	HALT	:EXAMINE STACK TO FIND CAUSE
853	000754	000756	.+2	:UNEXPECTED TRAP TO THIS LOCATION
854	000756	000000	HALT	:EXAMINE STACK TO FIND CAUSE
855	000760	000762	.+2	:UNEXPECTED TRAP TO THIS LOCATION
856	000762	000000	HALT	:EXAMINE STACK TO FIND CAUSE
857	000764	000766	.+2	:UNEXPECTED TRAP TO THIS LOCATION
858	000766	000000	HALT	:EXAMINE STACK TO FIND CAUSE
859	000770	000772	.+2	:UNEXPECTED TRAP TO THIS LOCATION
860	000772	000000	HALT	:EXAMINE STACK TO FIND CAUSE
861	000774	000776	.+2	:UNEXPECTED TRAP TO THIS LOCATION
862	000776	000000	HALT	:EXAMINE STACK TO FIND CAUSE

```

863                                     ;STANDARD INTERRUPT VECTORS
864
865
866                                     . =24
867 000024 015460 PFAIL ;POWER FAIL HANDLER
868 000026 000340 340 ;SERVICE AT LEVEL 7
869 000030 014240 ERRORS ;ERROR HANDLER
870 000032 000340 340 ;SERVICE AT LEVEL 7
871 000034 014442 TRPSRV ;GENERAL HANDLER DISPATCH SERVICE
872 000036 000340 340 ;SERVICE AT LEVEL 7
873                                     . =200
874 000200 000167 000574 JMP START ;GO TO START OF PROGRAM
875
876
877
878 ;DEFINITIONS FOR TRAP SUBROUTINE CALLS
879 ;POINTERS TO SUBROUTINES CAN BE FOUND STARTING
880 ;AT LOCATION "TRPTAB"
881
882 104400 SCOPE=TRAP+Y ;SCOPE LOOP AND ITERATION HANDLER
883 104401 TYPE=TRAP+Y ;TELETYPE OUTPUT ROUTINE
884 104402 OCTASC=TRAP+Y ;OCTAL TO ASCII CONVERSION
885 104403 INSTR=TRAP+Y ;INPUT ASCII STRING
886 104404 INSTER=TRAP+Y ;STRING INPUT ERROR
887 104405 PARAM=TRAP+Y ;CONVERT STRING TO OCTAL, CHECK LIMITS
888 104406 SAVOSP=TRAP+Y ;SAVE R0-R5, PC
889 104407 RESO5=TRAP+Y ;RESTORE R0-R5
890 104410 SCOPE1=TRAP+Y ;CHECK FOR FREEZE ON CURRENT DATA
891
892 000046 LOGICAL . =46
893 000052 . =52
894 040000 40000
  
```

```

001000      . =1000
:PROGRAM INITIALIZATION
:LOCK OUT INTERRUPTS
:SET UP PROCESSOR STACK
:SET UP POWER FAIL VECTOR
:CLEAR PROGRAM FLAGS AND COUNTS
:TYPE TITLE MESSAGE
:DETERMINE MEMORY SIZE

905 001000 012767 000340 176770 START: MOV #340,PS ;LOCK OUT INTERRUPTS
906 001006 012706 017102 MOV #STACK,SP ;SET UP PROCESSOR STACK
907 001012 012737 015460 000024 MOV #PFAIL,#24 ;SET UP POWER FAIL TRAP
908 001020 005067 014426 CLR STFLG ;CLEAR TEST START FLAG
909 001024 005067 014362 CLR PASCNT ;CLEAR PASS COUNT
910 001030 005067 014360 CLR ERRCNT ;CLEAR ERROR COUNT
911 001034 005067 014350 CLR ERRFLG ;CLEAR ERROR FLAG
912 001040 005067 014344 CLR ERRFLG ;CLEAR LAST ERROR PC
913 001044 104401 015624 TYPE MTITLE ;TYPE TITLE MESSAGE
914 001050 005767 014374 TST INIFLG ;CHECK INITIALIZATION FLAG
915 001054 001021 BNE VEC1 ;IF NOT 0, CHECK SWITCHES
;FOR REINITIALIZATION

917 001056 005000 SIZE: CLR R0
918 001060 012737 001072 000004 MOV #25,#4 ;SET UP TIME OUT RETURN
919 001066 005720 1$: TST (R0)+ ;WILL TRAP WHEN NO MEMORY
920 001070 000776 BR 1$ ;LOCATION RESPONDED, CONTINUE
921 001072 010067 014360 2$: MOV R0,HCORE ;R0 CONTAINS ADDRESS OF
922 001076 162767 000002 014352 SUB #2,HCORE ;NON EXISTATN MEMORY
923 001104 012737 000006 000004 MOV #6,#4 ;RESTORE TRAPCATCHER

925 001112 005767 014332 TST INIFLG ;IF INITIALIZE FLAG=0
926 001116 001404 BEQ VEC2 ;GET VECTOR AND CSR ADDRESS
927 001120 032767 000001 176442 VEC1: BIT #SW00,SWR ;IF SW00=1, GET NEW VECTOR
928 001126 001445 BEG BEGIN ;AND CSR
929 001130 012701 000300 VEC2: MOV #300,R1
930 001134 012702 000302 MOV #302,R2
931 001140 012703 000004 MOV #4,R3
932 001144 010211 1$: MOV R2,(R1) ;RESTORE TRAPCATCHER
933 001146 005012 CLR (R2) ;IN FLOATING VECTOR AREA
934 001150 060301 ADD R3,R1
935 001152 060302 ADD R3,R2
936 001154 020127 001000 CMP R1,#1000
937 001160 001371 BNE 1$
938 001162 104403 INSTR ;INPUT ADDRESS OF DEVICE VECTOR
939 001164 015703 MVECTOR ;MESSAGE "VECTOR ADDRESS-"
940 001166 104405 ;CONVERT STRING TO OCTAL
941 001170 000300 300 ;LOW LIMIT
942 001172 000770 770 ;HIGH LIMIT
943 001174 015400 DHRVEC ;LOCATIONS TO BE FILLED
944 001176 003 .BYTE 3 ;NUMBER OF LOCATIONS
945 001177 004 .BYTE 4 ;LSB MASK
946 001200 104403 INSTR ;INPUT ADDRESS OF DEVICE CSR
947 001202 015725 MREGAD ;MESSAGE "CONTROL REGISTER ADDRESS-"
948 001204 104405 PARAM ;CONVERT STRING TO OCTAL
949 001206 000000 0 ;LOW LIMIT
950 001210 177776 177776 ;HIGH LIMIT

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951	001212	015356				DHSCR			:LOCATIONS TO BE FILLED
952	001214	007				7			:NUMBER OF LOCATIONS
953	001215	010			.BYTE	10			:LSB MASK
954	001216	016767	014152	014152	.BYTE	MOV	DHSSR,DHSLR		:SET UP ADDRESS OF SILO
955	001224	005267	014146			INC	DHSLR		:STATUS REGISTER HIGH BYTE
956	001230	005767	014214			TST	INIFLG		:IF INITIALIZATION FLAG
957	001234	001002				BNE	BEGIN		:IS CLEARED
958	001236	005167	014206			COM	INIFLG		:SET IT
959									
960								:PROGRAM START	
961								:CHECK FOR PROGRAM START AT SELECTED ADDRESS	
962									
963	001242	012767	000340	176526	BEGIN:	MOV	#340,PS		:LOCK OUT INTERRUPTS
964	001250	012706	017102			MOV	#STACK,SP		:SET UP PROCESSOR STACK
965	001254	032767	000002	176306		BIT	#SW01,SWR		:IF SW01=1
966	001262	001410				BEQ	1\$:GET PC FOR PROGRAM START
967	001264	104403				INSTR			:GET PC
968	001266	016071				MTSTPC			:MESSAGE "TEST PC"
969	001270	104405				PARAM			:CONVERT STRING TO OCTAL
970	001272	000000				0			
971	001274	017500				17500			
972	001276	000207				RETURN			
973	001300	001			.BYTE	1			
974	001301	001			.BYTE	1			
975	001302	000410				BR	2\$		
976	001304	012767	001334	014104	1\$:	MOV	#T1,RETURN		:NORMAL START, TEST 1
977	001312	005767	014134			TST	STFLG		:IF LOOPING, BYPASS TIMEOUT
978	001316	001004				BNE	3\$		
979	001320	005167	014126			COM	STFLG		
980	001324	104401	016065		2\$:	TYPE	MR		:TYPE "R" TO INDICATE START
981	001330	000177	014062		3\$:	JMP	RETURN		:START TESTING

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982
983
984           ; INTERRUPT LOGIC TEST
985           ; SET CHARACTER AVAILABLE INTERRUPT ENABLE
986           ; VERIFY THAT NO INTERRUPTS OCCUR
987 001334 012767 000340 176434 T1:  MOV    #340,PS           ; DISABLE ALL INTERRUPTS
988 001342 012767 004000 014054      MOV    #4000,ICOUNT      ; SET UP FOR 4000 ITERATIONS
989 001350 012767 001470 014042      MOV    #3$,ESCAPE      ; SET UP TO ESCAPE TO NEXT TEST
990 001356 012777 004000 013772      MOV    #BIT11,JDHSCR   ; MASTER CLEAR INTERFACE
991 001364 012777 001440 014006      MOV    #1$,JDHRVEC    ; SET UP FOR POSSIBLE
992                                     ; RECEIVER INTERRUPT
993 001372 012777 000340 014002      MOV    #340,JDHRLVL   ;
994 001400 012777 001454 013776      MOV    #2$,JDHTVEC    ; SET UP FOR POSSIBLE
995                                     ; TRANSMITTER INTERRUPT
996 001406 012777 000340 013772      MOV    #340,JDHTLVL   ;
997 001414 012777 000100 013734      MOV    #BIT06,JDHSCR  ; SET CHARACTER AVAILABLE
998                                     ; INTERRUPT ENABLE
999 001422 005067 176350              CLR    PS              ; ALLOW INTERRUPTS
1000 001426 000240                    NOP                    ; WINDOW FOR INTERRUPTS
1001 001430 012767 000340 176340      MOV    #340,PS        ; NO INTERRUPT OCCURED
1002 001436 000414                    BR    3$              ; CONTINUE
1003 001440 017705 013712           1$:  MOV    JDHSCR,R5      ; GET CONTENTS OF SYSTEM CONTROL REGISTER
1004 001444 104000                    HLT    0              ; UNEXPECTED INTERRUPT
1005 001446 012716 001470              MOV    #3$, (SP)      ; SET UP TO
1006 001452 000002                    RTI                    ; RETURN FROM INTERRUPT
1007 001454 017705 013676           2$:  MOV    JDHSCR,R5      ; GET CONTENTS OF SYSTEM CONTROL REGISTER
1008 001460 104000                    HLT    0              ; UNEXPECTED INTERRUPT
1009 001462 012716 001470              MOV    #3$, (SP)      ; SET UPT TO
1010 001466 000002                    RTI                    ; RETURN FROM INTERRUPT
1011 001470 016777 013706 013702  3$:  MOV    DHRLVL,JDHRVEC  ; RESTORE TRAPCATCHER
1012 001476 005077 013700              CLR    JDHRLVL
1013 001502 016777 013700 013674      MOV    DHTLVL,JDHTVEC
1014 001510 005077 013672              CLR    JDHTLVL
1015 001514 104400                    SCOPE                 ; CHECK FOR ITERATIONS, LOOP
1016
1017           ; INTERRUPT LOGIC TEST
1018           ; SET SILO OVERFLOW INTERRUPT ENABLE
1019           ; VERIFY THAT NO INTERRUPTS OCCUR
1020
1021 001516 012767 000340 176252 T2:  MOV    #340,PS           ; DISABLE ALL INTERRUPTS
1022 001524 012767 004000 013672      MOV    #4000,ICOUNT   ; SET UP FOR 4000 ITERATIONS
1023 001532 012767 001652 013660      MOV    #3$,ESCAPE    ; SET UP TO ESCAPE TO NEXT TEST
1024 001540 012777 004000 013610      MOV    #BIT11,JDHSCR ; MASTER CLEAR INTERFACE
1025 001546 012777 001622 013624      MOV    #1$,JDHRVEC   ; SET UP FOR POSSIBLE
1026                                     ; RECEIVER INTERRUPT
1027 001554 012777 000340 013620      MOV    #340,JDHRLVL  ;
1028 001562 012777 001636 013614      MOV    #2$,JDHTVEC   ; SET UP FOR POSSIBLE
1029                                     ; TRANSMITTER INTERRUPT
1030 001570 012777 000340 013610      MOV    #340,JDHTLVL  ;
1031 001576 012777 010000 013552      MOV    #BIT12,JDHSCR ; SET SILO OVERFLOW
1032                                     ; INTERRUPT ENABLE
1033 001604 005067 176166              CLR    PS              ; ALLOW INTERRUPTS
1034 001610 000240                    NOP                    ; WINDOW FOR INTERRUPTS
1035 001612 012767 000340 176156      MOV    #340,PS        ; NO INTERRUPT OCCURED
1036 001620 000414                    BR    3$              ; CONTINUE
1037 001622 017705 013530           1$:  MOV    JDHSCR,R5      ; GET CONTENTS OF SYSTEM CONTROL REGISTER

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1038 001626 104000          HLT      0          ;UNEXPECTED INTERRUPT
1039 001632 012716 001652    MOV      #3$, (SP) ;SET UP TO
1040 001634 000002          RTI          ;RETURN FROM INTERRUPT
1041 001636 017705 013514    2$:     MOV      @DHSCR, R5 ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1042 001642 104000          HLT      0          ;UNEXPECTED INTERRUPT
1043 001644 012716 001652    MOV      #3$, (SP) ;SET UP TO
1044 001650 000002          RTI          ;RETURN FROM INTERRUPT
1045 001652 016777 013524 013520 3$:     MOV      DHRLVL, @DHRVEC ;RESTORE TRAPCATCHER
1046 001660 005077 013516    CLR      @DHRLVL
1047 001664 016777 013516 013512    MOV      DHTLVL, @DHTVEC
1048 001672 005077 013510    CLR      @DHTLVL
1049 001676 104400          SCOPE          ;CHECK FOR ITERATIONS, LOOP
1050
1051          ;INTERRUPT LOGIC TEST
1052          ;SET TRANSMITTER DONE INTERRUPT ENABLE
1053          ;VERIFY THAT NO INTERRUPTS OCCUR
1054
1055 001700 012767 000340 176070 T3:     MOV      #340, PS ;DISABLE ALL INTERRUPTS
1056 001706 012767 004000 013510    MOV      #4000, ICOUNT ;SET UP FOR 4000 ITERATIONS
1057 001714 012767 002034 013476    MOV      #3$, ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1058 001722 012777 004000 013426    MOV      #BIT11, @DHSCR ;MASTER CLEAR INTERFACE
1059 001730 012777 002004 013442    MOV      #1$, @DHRVEC ;SET UP FOR POSSIBLE
1060          ;RECEIVER INTERRUPT
1061 001736 012777 000340 013436    MOV      #340, @DHRLVL
1062 001744 012777 002020 013432    MOV      #2$, @DHTVEC ;SET UP FOR POSSIBLE
1063          ;TRANSMITTER INTERRUPT
1064 001752 012777 000340 013426    MOV      #340, @DHTLVL
1065 001760 012777 020000 013370    MOV      #BIT13, @DHSCR ;SET TRANSMITTER DONE
1066          ;INTERRUPT ENABLE
1067 001766 005067 176004          CLR      PS ;ALLOW INTERRUPTS
1068 001772 000240          NOP          ;WINDOW FOR INTERRUPTS
1069 001774 012767 000340 175774    MOV      #340, PS ;NO INTERRUPT OCCURED
1070 002002 000414          BR       3$ ;CONTINUE
1071 002004 017705 013346    1$:     MOV      @DHSCR, R5 ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1072 002010 104000          HLT      0          ;UNEXPECTED INTERRUPT
1073 002012 012716 002034    MOV      #3$, (SP) ;SET UP TO
1074 002016 000002          RTI          ;RETURN FROM INTERRUPT
1075 002020 017705 013332    2$:     MOV      @DHSCR, R5 ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1076 002024 104000          HLT      0          ;UNEXPECTED INTERRUPT
1077 002026 012716 002034    MOV      #3$, (SP) ;SET UP TO
1078 002032 000002          RTI          ;RETURN FROM INTERRUPT
1079 002034 016777 013342 013336 3$:     MOV      DHRLVL, @DHRVEC ;RESTORE TRAPCATCHER
1080 002042 005077 013334    CLR      @DHRLVL
1081 002046 016777 013334 013330    MOV      DHTLVL, @DHTVEC
1082 002054 005077 013326    CLR      @DHTLVL
1083 002060 104400          SCOPE          ;CHECK FOR ITERATIONS, LOOP
1084
1085          ;INTERRUPT LOGIC TEST
1086          ;SET CHARACTER AVAILABLE INTERRUPT ENABLE
1087          ;SET CHARACTER AVAILABLE (MAINTENANCE MODE IS ENABLED
1088          ;VERIFY THAT AN INTERRUPT OCCURS
1089
1090 002062 012767 000340 175706 T4:     MOV      #340, PS ;DISABLE ALL INTERRUPTS
1091 002070 012767 004000 013326    MOV      #4000, ICOUNT ;SET UP FOR 4000 ITERATIONS
1092 002076 012767 002226 013314    MOV      #3$, ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1093 002104 012777 004000 013244    MOV      #BIT11, @DHSCR ;MASTER CLEAR INTERFACE

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1094 002112 012777 002204 013260      MOV      #1$, @DHRVEC      ;SET UP FOR RECEIVER INTERRUPT
1095 002120 012777 000340 013254      MOV      #340, @DHRLVL
1096 002126 012777 002212 013250      MOV      #2$, @DHTVEC      ;SET UP FOR TRANSMITTER INTERRUPT
1097 002134 012777 000340 013244      MOV      #340, @DHTLVL
1098 002142 012777 001000 013206      MOV      #BIT09, @DHSCR      ;SET MAINTENANCE MODE
1099 002150 052777 000100 013200      BIS      #BIT06, @DHSCR      ;SET CHARACTER AVAILABLE
1100                                     ;INTERRUPT ENABLE
1101 002156 052777 000200 013172      BIS      #BIT07, @DHSCR      ;FORCE INTERRUPT BY
1102                                     ;SETTING CHARACTER AVAILABLE
1103 002164 005067 175606                                     CLR      PS      ;ALLOW INTERRUPTS
1104 002170 000240                                     NOP
1105 002172 012767 000340 175576      MOV      #340, PS      ;WINDOW FOR INTERRUPTS
1106 002200 104001                                     HLT      1      ;NO INTERRUPT OCCURED
1107                                     ;WITH CHARACTER AVAILABLE INTERRUPT
1108                                     ;ENABLE AND CHARACTER AVAILABLE SET
1109                                     ;ERROR
1109 002202 000411                                     BR      3$
1110 002204 012716 002226      1$:      MOV      #3$, (SP)      ;SET UP TO RETURN
1111 002210 000002                                     RTI
1112 002212 017705 013140      2$:      MOV      @DHSCR, R5      ;FROM VALID INTERRUPT
1113 002216 104000                                     HLT      0      ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1114 002220 012716 002226      MOV      #3$, (SP)      ;UNEXPECTED INTERRUPT
1115 002224 000002                                     RTI      ;SET UP TO RETURN
1116 002226 016777 013150 013144 3$:      MOV      DHRLVL, @DHRVEC      ;FROM UNEXPECTED INTERRUPT
1117 002234 005077 013142      CLR      @DHRLVL      ;RESTORE TRAPCATCHER
1118 002240 016777 013142 013136      MOV      DHTLVL, @DHTVEC
1119 002246 005077 013134      CLR      @DHTLVL
1120 002252 104400      SCOPE
1121
1122                                     ; INTERRUPT LOGIC TEST
1123                                     ; SET SILO OVERFLOW INTERRUPT ENABLE
1124                                     ; SET SILO OVERFLOW (MAINTENANCE MODE IS ENABLED)
1125                                     ; VERIFY THAT AN INTERRUPT OCCURS
1126
1127 002254 012767 000340 175514  T5:      MOV      #340, PS      ;DISABLE ALL INTERRUPTS
1128 002262 012767 004000 013134      MOV      #4000, ICOUNT      ;SET UP FOR 4000 ITERATIONS
1129 002270 012767 002420 013122      MOV      #3$, ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1130 002276 012777 004000 013052      MOV      #BIT11, @DHSCR      ;MASTER CLEAR INTERFACE
1131 002304 012777 002376 013066      MOV      #1$, @DHRVEC      ;SET UP FOR RECEIVER INTERRUPT
1132 002312 012777 000340 013062      MOV      #340, @DHRLVL
1133 002320 012777 002404 013056      MOV      #2$, @DHTVEC      ;SET UP FOR TRANSMITTER INTERRUPT
1134 002326 012777 000340 013052      MOV      #340, @DHTLVL
1135 002334 012777 001000 013014      MOV      #BIT09, @DHSCR      ;SET MAINTENANCE MODE
1136 002342 052777 040000 013006      BIS      #BIT14, @DHSCR      ;SET SILO OVERFLOW
1137                                     ;INTERRUPT ENABLE
1138 002350 052777 010000 013000      BIS      #BIT12, @DHSCR      ;FORCE INTERRUPT BY
1139                                     ;SETTING SILO OVERFLOW
1140                                     ;ALLOW INTERRUPTS
1141 002356 005067 175414                                     CLR      PS      ;WINDOW FOR INTERRUPTS
1142 002362 000240                                     NOP
1143 002364 012767 000340 175404      MOV      #340, PS      ;NO INTERRUPT OCCURED
1144 002372 104001                                     HLT      1      ;WITH SILO OVERFLOW INTERRUPT
1145                                     ;ENABLE AND SILO OVERFLOW SET
1146                                     ;ERROR
1146 002374 000411                                     BR      3$
1147 002376 012716 002420      1$:      MOV      #3$, (SP)      ;SET UP TO RETURN
1148 002402 000002                                     RTI
1149 002404 017705 012746      2$:      MOV      @DHSCR, R5      ;FROM VALID INTERRUPT
                                     ;GET CONTENTS OF SYSTEM CONTROL REGISTER

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1150 002410 104000          HLT      0          ;UNEXPECTED INTERRUPT
1151 002412 012716 002420  MOV      #3$, (SP) ;SET UP TO RETURN
1152 002416 000002          RTI          ;FROM UNEXPECTED INTERRUPT
1153 002420 016777 012756 012752 3$:  MOV      DHRLVL, @DHRVEC ;RESTORE TRAPCATCHER
1154 002426 005077 012750          CLR      @DHRLVL
1155 002432 016777 012750 012744  MOV      DHTLVL, @DHTVEC
1156 002440 005077 012742          CLR      @DHTLVL
1157 002444 104400          SCOPE
1158
1159          ; INTERRUPT LOGIC TEST
1160          ; SET TRANSMITTER INTERRUPT ENABLE
1161          ; SET NON EXISTATN MEMORY (MAINTENANCE MODE IS ENABLED)
1162          ; VERIFY THAT AN INTERRUPT OCCURS
1163
1164 002446 012767 000340 175322 T6:  MOV      #340, PS ;DISABLE ALL INTERRUPTS
1165 002454 012767 004000 012742  MOV      #4000, ICOUNT ;SET UP FOR 4000 ITERATIONS
1166 002462 012767 002612 012730  MOV      #3$, ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1167 002470 012777 004000 012660  MOV      #BIT11, @DHSCR ;MASTER CLEAR INTERFACE
1168 002476 012777 002576 012674  MOV      #2$, @DHRVEC ;SET UP FOR RECEIVER INTERRUPT
1169 002504 012777 000340 012670  MOV      #340, @DHRLVL
1170 002512 012777 002570 012664  MOV      #1$, @DHTVEC ;SET UP FOR TRANSMITTER INTERRUPT
1171 002520 012777 000340 012660  MOV      #340, @DHTLVL
1172 002526 012777 001000 012622  MOV      #BIT09, @DHSCR ;SET MAINTENANCE MODE
1173 002534 052777 020000 012614  BIS      #BIT13, @DHSCR ;SET TRANSMITTER
1174          ; INTERRUPT ENABLE
1175 002542 052777 002000 012606  BIS      #BIT10, @DHSCR ;FORCE INTERRUPT BY
1176          ; SETTING NON EXISTATN MEMORY
1177 002550 005067 175222          CLR      PS ;ALLOW INTERRUPTS
1178 002554 000240          NOP ;WINDOW FOR INTERRUPTS
1179 002556 012767 000340 175212  MOV      #340, PS ;NO INTERRUPT OCCURED
1180 002564 104001          HLT      1 ;WITH TRANSMITTER INTERRUPT
1181          ; ENABLE AND NON EXISTATN MEMORY SET
1182          ; ERROR
1183 002566 000411          BR      3$
1184 002570 012716 002612          1$:  MOV      #3$, (SP) ;SET UP TO RETURN
1185 002574 000002          RTI          ;FROM VALID INTERRUPT
1186 002576 017705 012554          2$:  MOV      @DHSCR, R5 ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1187 002602 104000          HLT      0 ;UNEXPECTED INTERRUPT
1188 002604 012716 002612  MOV      #3$, (SP) ;SET UP TO RETURN
1189 002610 000002          RTI          ;FROM UNEXPECTED INTERRUPT
1190 002612 016777 012564 012560 3$:  MOV      DHRLVL, @DHRVEC ;RESTORE TRAPCATCHER
1191 002620 005077 012556          CLR      @DHRLVL
1192 002624 016777 012556 012552  MOV      DHTLVL, @DHTVEC
1193 002632 005077 012550          CLR      @DHTLVL
1194 002636 104400          SCOPE
1195
1196          ; INTERRUPT LOGIC TEST
1197          ; SET TRANSMITTER DONE INTERRUPT ENABLE
1198          ; SET TRANSMITTER DONE (MAINTENANCE MODE IS ENABLED)
1199          ; VERIFY THAT AN INTERRUPT OCCURS
1200
1201 002640 012767 000340 175130 T7:  MOV      #340, PS ;DISABLE ALL INTERRUPTS
1202 002646 012767 004000 012550  MOV      #4000, ICOUNT ;SET UP FOR 4000 ITERATIONS
1203 002654 012767 003004 012536  MOV      #3$, ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1204 002662 012777 004000 012466  MOV      #BIT11, @DHSCR ;MASTER CLEAR INTERFACE
1205 002670 012777 002770 012502  MOV      #2$, @DHRVEC ;SET UP FOR RECEIVER INTERRUPT

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1230	002766	012777	000340	012476	MOV	#340,JDHRLVL	
1231	002767	012777	002762	012472	MOV	#1\$,JDHTVEC	:SET UP FOR TRANSMITTER INTERRUPT
1232	002771	012777	000340	012466	MOV	#340,JDHTLVL	
1233	002720	012777	001000	012430	MOV	#BIT09,JDHSCR	:SET MAINTENANCE MODE
1234	002726	052777	020000	012422	BIS	#BIT13,JDHSCR	:SET TRANSMITTER DONE
1235							:INTERRUPT ENABLE
1236	002734	052777	100000	012414	BIS	#BIT15,JDHSCR	:FORCE INTERRUPT BY
1237							:SETTING TRANSMITTER DONE
1238	002742	005067	175030		CLR	PS	:ALLOW INTERRUPTS
1239	002746	000240			NOP		:WINDOW FOR INTERRUPTS
1240	002750	012767	000340	175020	MOV	#340,PS	:NO INTERRUPT OCCURED
1241	002756	104001			HLT	1	:WITH TRANSMITTER DONE INTERRUPT
1242							:ENABLE AND TRANSMITTER DONE SET
1243							:ERROR
1244	002760	000411			BR	3\$	
1245	002762	012716	003004		1\$:	MOV #3\$, (SP)	:SET UP TO RETURN
1246	002766	000002			RTI		:FROM VALID INTERRUPT
1247	002770	017705	012362		2\$:	MOV JDHSCR,RS	:GET CONTENTS OF SYSTEM CONTROL REGISTER
1248	002774	104000			HLT	0	:UNEXPECTED INTERRUPT
1249	002776	012716	003004		MOV	#3\$, (SP)	:SET UP TO RETURN
1250	003002	000002			RTI		:FROM UNEXPECTED INTERRUPT
1251	003004	016777	012372	012366	3\$:	MOV DHRLVL,JDHRVEC	:RESTORE TRAPCATCHER
1252	003012	005077	012364		CLR	JDHRLVL	
1253	003016	016777	012364	012360	MOV	DHTLVL,JDHTVEC	
1254	003024	005077	012356		CLR	JDHTLVL	
1255	003030	104400			SCOPE		
1256							:NPR LOGIC TEST
1257							:SET BYTE COUNT TO 1 FOR LINE 0
1258							:SET BAR BIT FOR LINE 0
1259							:DELAY FOR NPR
1260							:VERIFY THAT BAR BIT FOR LINE 0 CLEARS
1261							:VERIFY THAT TRANSMITTER DONE IS SET
1262	003032	012767	000340	174736	T10:	MOV #340,PS	:DISABLE ALL INTERRUPTS
1263	003040	012767	000020	012356	MOV	#20,COUNT	:SET UP FOR 20 ITERATIONS
1264	003046	012767	003262	012344	MOV	#6\$,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
1265	003054	012777	004000	012274	MOV	#BIT11,JDHSCR	:ISSUE MASTER CLEAR
1266	003062	004767	012176		JSR	PC,CLEAR	:CLEAR ALL BUS ADDRESS
1267							:AND BYTE COUNT MEMORY LOCATIONS
1268	003066	012777	003150	012310	MOV	#2\$,JDHTVEC	:SET UP TRANSMITTER
1269	003074	012777	000340	012304	MOV	#340,JDHTLVL	:INTERRUPT VECTOR
1270	003102	012777	000000	012246	MOV	#0,JDHSCR	:SELECT LINE 0
1271	003110	012777	177777	012250	MOV	#-1,JDHBC	:SET BYTE COUNT TO 1
1272	003116	012700	001000		MOV	#1000,RO	
1273	003122	012777	000001	012240	MOV	#1,JDHBAR	:SET BAR BIT FOR
1274							:LINE 0
1275	003130	052777	020000	012220	BIS	#BIT13,JDHSCR	:SET TRANSMITTER INTERRUPT ENABLE
1276	003136	005067	174634		CLR	PS	:ALLOW INTERRUPTS
1277	003142	005300			1\$:	DEC RO	:DELAY FOR NPR
1278	003144	001376			BNE	1\$	
1279	003146	104001			HLT	1	:NO INTERRUPT OCCURED, ERROR
1280	003150	005777	012202		2\$:	TST JDHSCR	:VERIFY THAT TRANSMITTER
1281							:DONE IS SET
1282	003154	100401			BMI	3\$	
1283	003156	104002			HLT	2	:TRANSMITTER DONE NOT SET, ERROR

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13000 003160 005777 012204 3$: TST 3DHBAR ;WAS BAR BIT CLEARED FOR LINE 0
13001 003164 001404 BEQ 4$
13002 003166 005005 CLR R5 ;(R5)=EXPECTED DATA IN
;BUFFER ACTIVE REGISTER, 0
13003 003170 017704 012174 MOV 3DHBAR,R4 ;(R4)=ACTUAL CONTENTS OF
;BUFFER ACTIVE REGISTER
13004 003174 104000 HLT 0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
13005 003176 022777 000001 012160 4$: CMP #1,3DHBA ;WAS BUS ADDRESS INCREMENTED
13006 003204 001405 BEQ 5$
13007 003206 017704 012152 MOV 3DHBA,R4 ;(R4)=ACTUAL CONTENTS
;OF BUS ADDRESS MEMORY FOR
;LINE 0
13008 003212 012705 000001 MOV #1,R5 ;(R5)=EXPECTED VALUE OF
;BUS ADDRESS MEMORY FOR
;LINE 0, 1
13009 003216 104003 HLT 3 ;BUS ADDRESS NOT UPDATED
;CORRECTLY, ERROR
13010 003220 005777 012142 5$: TST 3DHBC ;DID BYTE COUNT DECREMENT TO 0
13011 003224 001416 BEQ 6$
13012 003226 017704 012134 MOV 3DHBC,R4 ;(R4)=ACTUAL VALUE OF BYTE
;COUNT FOR LINE 0
13013 003232 005005 CLR R5 ;(R5)=EXPECTED VALUE OF BYTE
;COUNT FOR LINE 0, 0
13014 003234 104004 HLT 4 ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
13015 003236 016777 012140 012134 MOV DHRVLV,3DHVEC ;RESTORE TRAPCATCHER
13016 003244 005077 012132 CLR 3DHRVLV
13017 003250 016777 012132 012126 MOV DHTLVL,3DHTVEC
13018 003256 005077 012124 CLR 3DHTLVL
13019 003262 012706 017102 6$: MOV #STACK,SP ;RESTORE STACK
13020 003266 104000 SCOPE ;CHECK FOR ITERATIONS, LOOP

;NPR LOGIC TEST
;SET BYTE COUNT TO 1 FOR LINE 1
;SET BAR BIT FOR LINE 1
;DELAY FOR NPR
;VERIFY THAT BAR BIT FOR LINE 1 CLEARS
;VERIFY THAT TRANSMITTER DONE IS SET

13021 003270 012767 000340 174500 T11: MOV #340,PS ;DISABLE ALL INTERRUPTS
13022 003276 012767 000020 012120 MOV #20,COUNT ;SET UP FOR 20 ITERATIONS
13023 003304 012767 003520 012106 MOV #6$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
13024 003312 012777 004000 012036 MOV #BIT11,3DHSCR ;ISSUE MASTER CLEAR
13025 003320 004767 011740 JSR PC,CLEAR ;CLEAR ALL BUS ADDRESS
;AND BYTE COUNT MEMORY LOCATIONS
13026 003324 012777 003406 012052 MOV #2$,3DHTVEC ;SET UP TRANSMITTER
13027 003332 012777 000340 012046 MOV #340,3DHTLVL ;INTERRUPT VECTOR
13028 003340 012777 000001 012010 MOV #1,3DHSCR ;SELECT LINE 1
13029 003346 012777 177777 012012 MOV #-1,3DHBC ;SET BYTE COUNT TO 1
13030 003354 012700 001000 MOV #1000,R0
13031 003360 012777 000002 012002 MOV #2,3DHBAR ;SET BAR BIT FOR
;LINE 1
13032 003366 052777 020000 011762 BIS #BIT13,3DHSCR ;SET TRANSMITTER INTERRUPT ENABLE
13033 003374 005067 174376 CLR PS ;ALLOW INTERRUPTS
13034 003400 005300 1$: DEC R0 ;DELAY FOR NPR
13035 003402 001376 BNE 1$
13036 003404 104001 HLT 1 ;NO INTERRUPT OCCURED, ERROR

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1318 003406 005777 011744 2$: TST 3DHSCR ;VERIFY THAT TRANSMITTER
1319 ;DONE IS SET
1320 003412 100401 BMI 3$
1321 003414 104002 HLT 2 ;TRANSMITTER DONE NOT SET, ERROR
1322 003416 005777 011746 3$: TST 3DHBAR ;WAS BAR BIT CLEARED FOR LINE 1
1323 003422 001404 BEQ 4$
1324 003424 005005 CLR R5 ;(R5)=EXPECTED DATA IN
1325 ;BUFFER ACTIVE REGISTER, 0
1326 003426 017704 011736 MOV 3DHBAR,R4 ;(R4)=ACTUAL CONTENTS OF
1327 ;BUFFER ACTIVE REGISTER
1328 003432 104000 HLT 0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
1329 003434 022777 000001 011722 4$: CMP #1,3DHBA ;WAS BUS ADDRESS INCREMENTED
1330 003442 001405 BEQ 5$
1331 003444 017704 011714 MOV 3DHBA,R4 ;(R4)=ACTUAL CONTENTS
1332 ;OF BUS ADDRESS MEMORY FOR
1333 ;LINE 1
1334 003450 012705 000001 MOV #1,R5 ;(R5)=EXPECTED VALUE OF
1335 ;BUS ADDRESS MEMORY FOR
1336 ;LINE 1, 1
1337 003454 104003 HLT 3 ;BUS ADDRESS NOT UPDATED
1338 ;CORRECTLY, ERROR
1339 003456 005777 011704 5$: TST 3DHBC ;DID BYTE COUNT DECREMENT TO 0
1340 003462 001416 BEQ 6$
1341 003464 017704 011676 MOV 3DHBC,R4 ;(R4)=ACTUAL VALUE OF BYTE
1342 ;COUNT FOR LINE 1
1343 003470 005005 CLR R5 ;(R5)=EXPECTED VALUE OF BYTE
1344 ;COUNT FOR LINE 1, 0
1345 003472 104004 HLT 4 ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1346 003474 016777 011702 011676 MOV DHRLVL,3DHAVEC ;RESTORE TRAPCATCHER
1347 003502 005077 011674 CLR 3DHRLVL
1348 003506 016777 011674 011670 MOV DHRTLVL,3DHTEVC
1349 003514 005077 011666 CLR 3DHRTLVL
1350 003520 012706 017102 6$: MOV #STACK,SP ;RESTORE STACK
1351 003524 104400 SCOPE ;CHECK FOR ITERATIONS, LOOP
1352 ;NPR LOGIC TEST
1353 ;SET BYTE COUNT TO 1 FOR LINE 2
1354 ;SET BAR BIT FOR LINE 2
1355 ;DELAY FOR NPR
1356 ;VERIFY THAT BAR BIT FOR LINE 2 CLEARS
1357 ;VERIFY THAT TRANSMITTER DONE IS SET
1358
1359
1360 003526 012767 000340 174242 T12: MOV #340,FS ;DISABLE ALL INTERRUPTS
1361 003534 012767 000020 011662 MOV #20,ICOUNT ;SET UP FOR 20 ITERATIONS
1362 003542 012767 003756 011650 MOV #6$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1363 003550 012777 004000 011600 MOV #BIT11,3DHSCR ;ISSUE MASTER CLEAR
1364 003556 004767 011502 JSR PC,CLEAR ;CLEAR ALL BUS ADDRESS
1365 ;AND BYTE COUNT MEMORY LOCATIONS
1366 003562 012777 003644 011614 MOV #2$,3DHTEVC ;SET UP TRANSMITTER
1367 003570 012777 000340 011610 MOV #340,3DHRTLVL ;INTERRUPT VECTOR
1368 003576 012777 000002 011552 MOV #2,3DHSCR ;SELECT LINE 2
1369 003604 012777 177777 011554 MOV #-1,3DHBC ;SET BYTE COUNT TO 1
1370 003612 012700 001000 MOV #1000,R0
1371 003616 012777 000004 011544 MOV #4,3DHBAR ;SET BAR BIT FOR
1372 ;LINE 2
1373 003624 052777 020000 011524 BIS #BIT13,3DHSCR ;SET TRANSMITTER INTERRUPT ENABLE

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1374	003632	005067	174140			CLR	PS	;ALLOW INTERRUPTS
1375	003636	005300		1\$:		DEC	RO	;DELAY FOR NPR
1376	003640	001376				BNE	1\$	
1377	003642	104001				HLT	1	;NO INTERRUPT OCCURED, ERROR
1378	003644	005777	011506	2\$:		TST	2DHSCR	;VERIFY THAT TRANSMITTER ;DONE IS SET
1379								
1380	003650	100401				BMI	3\$	
1381	003652	104002				HLT	2	;TRANSMITTER DONE NOT SET, ERROR
1382	003654	005777	011510	3\$:		TST	2DHBAR	;WAS BAR BIT CLEARED FOR LINE 2
1383	003660	001404				BEQ	4\$	
1384	003662	005005				CLR	R5	; (R5)=EXPECTED DATA IN ;BUFFER ACTIVE REGISTER, 0
1385								; (R4)=ACTUAL CONTENTS OF ;BUFFER ACTIVE REGISTER
1386	003664	017704	011500			MOV	2DHBAR,R4	;BUS ACTIVE BIT NOT CLEARED, ERROR
1387								;WAS BUS ADDRESS INCREMENTED
1388	003670	104000				HLT	0	
1389	003672	022777	000001	011464	4\$:	CMP	#1,2DHBA	
1390	003700	001405				BEQ	5\$	
1391	003702	017704	011456			MOV	2DHBA,R4	; (R4)=ACTUAL CONTENTS ;OF BUS ADDRESS MEMORY FOR ;LINE 2
1392								; (R5)=EXPECTED VALUE OF ;BUS ADDRESS MEMORY FOR ;LINE 2, 1
1393								;BUS ADDRESS NOT UPDATED ;CORRECTLY, ERROR
1394	003706	012705	000001			MOV	#1,R5	;DID BYTE COUNT DECREMENT TO 0
1395								
1396								
1397	003712	104003				HLT	3	
1398								
1399	003714	005777	011446	5\$:		TST	2DHBC	
1400	003720	001416				BEQ	6\$	
1401	003722	017704	011440			MOV	2DHBC,R4	; (R4)=ACTUAL VALUE OF BYTE ;COUNT FOR LINE 2
1402								; (R5)=EXPECTED VALUE OF BYTE ;COUNT FOR LINE 2, 0
1403	003726	005005				CLR	R5	;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1404								
1405	003730	104004				HLT	4	
1406	003732	016777	011444	011440		MOV	DHRLVL,2DHVEC	;RESTORE TRAPCATCHER
1407	003740	005077	011436			CLR	2DHRLVL	
1408	003744	016777	011436	011432		MOV	DHTLVL,2DHTVEC	
1409	003752	005077	011430			CLR	2DHTLVL	
1410	003756	012706	017102	6\$:		MOV	#STACK,SP	;RESTORE STACK
1411	003762	104400				SCOPE		;CHECK FOR ITERATIONS, LOOP
1412								
1413								
1414								
1415								
1416								
1417								
1418								
1419								
1420	003764	012767	000340	174004	T13:	MOV	#340,PS	;DISABLE ALL INTERRUPTS
1421	003772	012767	000020	011424		MOV	#20,ICOUNT	;SET UP FOR 20 ITERATIONS
1422	004000	012767	004214	011412		MOV	#6\$,ESCAPE	;SET UP TO ESCAPE TO NEXT TEST
1423	004006	012777	004000	011342		MOV	#BIT11,2DHSCR	;ISSUE MASTER CLEAR
1424	004014	004767	011244			JSR	PC,CLEAR	;CLEAR ALL BUS ADDRESS ;AND BYTE COUNT MEMORY LOCATIONS
1425								
1426	004020	012777	004102	011356		MOV	#2\$,2DHTVEC	;SET UP TRANSMITTER
1427	004026	012777	000340	011352		MOV	#340,2DHTLVL	;INTERRUPT VECTOR
1428	004034	012777	000003	011314		MOV	#3,2DHSCR	;SELECT LINE 3
1429	004042	012777	177777	011316		MOV	#-1,2DHBC	;SET BYTE COUNT TO 1


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1486 004256 012777 004340 011120      MOV      #2$, @DHTVEC      ;SET UP TRANSMITTER
1487 004264 012777 000340 011114      MOV      #340, @DHTLVL    ;INTERRUPT VECTOR
1488 004272 012777 000004 011056      MOV      #4, @DHSCR       ;SELECT LINE 4
1489 004300 012777 177777 011060      MOV      #-1, @DHBC       ;SET BYTE COUNT TO 1
1490 004306 012700 001000      MOV      #1000, R0
1491 004312 012777 000020 011050      MOV      #20, @DHBAR      ;SET BAR BIT FOR
1492                                     ;LINE 4
1493 004320 052777 020000 011030      BIS      #BIT13, @DHSCR    ;SET TRANSMITTER INTERRUPT ENABLE
1494 004326 005067 173444      CLR      PS               ;ALLOW INTERRUPTS
1495 004332 005300      1$: DEC      R0            ;DELAY FOR NPR
1496 004334 001376      BNE     1$
1497 004336 104001      HLT     1
1498 004340 005777 011012      2$: TST     @DHSCR        ;NO INTERRUPT OCCURED, ERROR
1499                                     ;VERIFY THAT TRANSMITTER
1500                                     ;DONE IS SET
1501 004346 104002      HLT     2
1502 004350 005777 011014      3$: TST     @DHBAR        ;TRANSMITTER DONE NOT SET, ERROR
1503 004354 001404      BEQ     4$               ;WAS BAR BIT CLEARED FOR LINE 4
1504 004356 005005      CLR     R5
1505                                     ;(R5)=EXPECTED DATA IN
1506 004360 017704 011004      MOV     @DHBAR, R4       ;BUFFER ACTIVE REGISTER, 0
1507                                     ;(R4)=ACTUAL CONTENTS OF
1508 004364 104000      HLT     0               ;BUFFER ACTIVE REGISTER
1509 004366 022777 000001 010770 4$: CMP     #1, @DHBA       ;BUS ACTIVE BIT NOT CLEARED, ERROR
1510 004374 001405      BEQ     5$               ;WAS BUS ADDRESS INCREMENTED
1511 004376 017704 010762      MOV     @DHBA, R4
1512                                     ;(R4)=ACTUAL CONTENTS
1513                                     ;OF BUS ADDRESS MEMORY FOR
1514 004402 012705 000001      MOV     #1, R5          ;LINE 4
1515                                     ;(R5)=EXPECTED VALUE OF
1516                                     ;BUS ADDRESS MEMORY FOR
1517 004406 104003      HLT     3               ;LINE 4, 1
1518                                     ;BUS ADDRESS NOT UPDATED
1519 004410 005777 010752      5$: TST     @DHBC        ;CORRECTLY, ERROR
1520 004414 001416      BEQ     6$               ;DID BYTE COUNT DECREMENT TO 0
1521 004416 017704 010744      MOV     @DHBC, R4
1522                                     ;(R4)=ACTUAL VALUE OF BYTE
1523 004422 005005      CLR     R5              ;COUNT FOR LINE 4
1524                                     ;(R5)=EXPECTED VALUE OF BYTE
1525 004424 104004      HLT     4               ;COUNT FOR LINE 4, 0
1526 004426 016777 010750 010744      MOV     @DTRLVL, @DTRVEC ;RESTORE TRAPCATCHER
1527 004434 005077 010742      CLR     @DTRLVL
1528 004440 016777 010742 010736      MOV     @DTRLVL, @DTRVEC
1529 004446 005077 010734      CLR     @DTRLVL
1530 004452 012706 017102      6$: MOV     #STACK, SP     ;RESTORE STACK
1531 004456 104400      SCOPE    ;CHECK FOR ITERATIONS, LOOP
1532
1533      ;NPR LOGIC TEST
1534      ;SET BYTE COUNT TO 1 FOR LINE 5
1535      ;SET BAR BIT FOR LINE 5
1536      ;DELAY FOR NPR
1537      ;VERIFY THAT BAR BIT FOR LINE 5 CLEARS
1538      ;VERIFY THAT TRANSMITTER DONE IS SET
1539
1540 004460 012767 000340 173310 715: MOV     #340, PS         ;DISABLE ALL INTERRUPTS
1541 004466 012767 000020 010730      MOV     #20, ICOUNT     ;SET UP FOR 20 ITERATIONS

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1542 004474 012767 004710 010716      MOV      #6$, ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1543 004502 012777 004000 010646      MOV      #BIT11, @DHSCR  ;ISSUE MASTER CLEAR
1544 004510 004767 010550                JSR      PC, CLEAR      ;CLEAR ALL BUS ADDRESS
1545                                ;AND BYTE COUNT MEMORY LOCATIONS
1546 004514 012777 004576 010662      MOV      #2$, @DHTVEC    ;SET UP TRANSMITTER
1547 004522 012777 000340 010656      MOV      #340, @DHTLVL   ;INTERRUPT VECTOR
1548 004530 012777 000005 010620      MOV      #5, @DHSCR      ;SELECT LINE 5
1549 004536 012777 177777 010622      MOV      #-1, @DHBC      ;SET BYTE COUNT TO 1
1550 004544 012700 001000                MOV      #1000, R0
1551 004550 012777 000040 010612      MOV      #40, @DHBAR     ;SET BAR BIT FOR
1552                                ;LINE 5
1553 004556 052777 020000 010572      BIS      #BIT13, @DHSCR  ;SET TRANSMITTER INTERRUPT ENABLE
1554 004564 005067 173206                CLR      PS              ;ALLOW INTERRUPTS
1555 004570 005300                1$:    DEC      R0              ;DELAY FOR NPR
1556 004572 001376                BNE     1$
1557 004574 104001                HLT     1
1558 004576 005777 010554                2$:    TST     @DHSCR      ;NO INTERRUPT OCCURED, ERROR
1559                                ;VERIFY THAT TRANSMITTER
1560                                ;DONE IS SET
1561 004604 104002                HLT     2
1562 004606 005777 010556                3$:    TST     @DHBAR     ;TRANSMITTER DONE NOT SET, ERROR
1563 004612 001404                BEQ     4$              ;WAS BAR BIT CLEARED FOR LINE 5
1564 004614 005005                CLR     R5
1565                                ;(R5)=EXPECTED DATA IN
1566 004616 017704 010546      MOV      @DHBAR, R4     ;BUFFER ACTIVE REGISTER, 0
1567                                ;(R4)=ACTUAL CONTENTS OF
1568 004622 104000                HLT     0              ;BUFFER ACTIVE REGISTER
1569 004624 022777 000001 010532  4$:    CMP     #1, @DHBA     ;BUS ACTIVE BIT NOT CLEARED, ERROR
1570 004632 001405                BEQ     5$              ;WAS BUS ADDRESS INCREMENTED
1571 004634 017704 010524      MOV      @DHBA, R4
1572                                ;(R4)=ACTUAL CONTENTS
1573                                ;OF BUS ADDRESS MEMORY FOR
1574 004640 012705 000001      MOV      #1, R5        ;LINE 5
1575                                ;(R5)=EXPECTED VALUE OF
1576                                ;BUS ADDRESS MEMORY FOR
1577 004644 104003                HLT     3              ;LINE 5, 1
1578                                ;BUS ADDRESS NOT UPDATED
1579 004646 005777 010514                5$:    TST     @DHBC      ;CORRECTLY, ERROR
1580 004652 001416                BEQ     6$              ;DID BYTE COUNT DECREMENT TO 0
1581 004654 017704 010506      MOV      @DHBC, R4
1582                                ;(R4)=ACTUAL VALUE OF BYTE
1583                                ;COUNT FOR LINE 5
1584 004660 005005                CLR     R5              ;(R5)=EXPECTED VALUE OF BYTE
1585                                ;COUNT FOR LINE 5, 0
1586 004662 104004                HLT     4              ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1587 004664 016777 010512 010506      MOV      @DHLVL, @DHVEC ;RESTORE TRAPCATCHER
1588 004672 005077 010504                CLR     @DHLVL
1589 004676 016777 010504 010500      MOV      @DHTLVL, @DHTVEC
1590 004704 005077 010476                CLR     @DHTLVL
1591 004710 012706 017102                6$:    MOV      #STACK, SP ;RESTORE STACK
1592                                ;CHECK FOR ITERATIONS, LOOP
1593                                ;NPR LOGIC TEST
1594                                ;SET BYTE COUNT TO 1 FOR LINE 6
1595                                ;SET BAR BIT FOR LINE 6
1596                                ;DELAY FOR NPR
1597                                ;VERIFY THAT BAR BIT FOR LINE 6 CLEARS

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1654                                     ;SET BYTE COUNT TO 1 FOR LINE 7
1655                                     ;SET BAR BIT FOR LINE 7
1656                                     ;DELAY FOR NPR
1657                                     ;VERIFY THAT BAR BIT FOR LINE 7 CLEARS
1658                                     ;VERIFY THAT TRANSMITTER DONE IS SET
1659
1660 005154 012767 000340 172614 T17: MOV #340,PS ;DISABLE ALL INTERRUPTS
1661 005162 012767 000020 010234 MOV #20,ICOUNT ;SET UP FOR 20 ITERATIONS
1662 005170 012767 005404 010222 MOV #6$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1663 005176 012777 004000 010152 MOV #BIT11,JDHSCR ;ISSUE MASTER CLEAR
1664 005204 004767 010054 JSR PC,CLEAR ;CLEAR ALL BUS ADDRESS
1665                                     ;AND BYTE COUNT MEMORY LOCATIONS
1666 005210 012777 005272 010166 MOV #2$,JDHTVEC ;SET UP TRANSMITTER
1667 005216 012777 000340 010162 MOV #340,JDHTLVL ;INTERRUPT VECTOR
1668 005224 012777 000007 010124 MOV #7,JDHSCR ;SELECT LINE 7
1669 005232 012777 177777 010126 MOV #-1,JDHBC ;SET BYTE COUNT TO 1
1670 005240 012700 001000 MOV #1000,RO
1671 005244 012777 000200 010116 MOV #200,JDHBAR ;SET BAR BIT FOR
1672                                     ;LINE 7
1673 005252 052777 020000 010076 BIS #BIT13,JDHSCR ;SET TRANSMITTER INTERRUPT ENABLE
1674 005260 005067 172512 CLR PS ;ALLOW INTERRUPTS
1675 005264 005300 1$: DEC RO ;DELAY FOR NPR
1676 005266 001376 BNE 1$
1677 005270 104001 HLT 1 ;NO INTERRUPT OCCURED, ERROR
1678 005272 005777 010060 2$: TST JDHSCR ;VERIFY THAT TRANSMITTER
1679                                     ;DONE IS SET
1680 005276 100401 BMI 3$
1681 005300 104002 HLT 2 ;TRANSMITTER DONE NOT SET, ERROR
1682 005302 005777 010062 3$: TST JDHBAR ;WAS BAR BIT CLEARED FOR LINE 7
1683 005306 001404 BEQ 4$
1684 005310 005005 CLR R5 ;(R5)=EXPECTED DATA IN
1685                                     ;BUFFER ACTIVE REGISTER, 0
1686 005312 017704 010052 MOV JDHBAR,R4 ;(R4)=ACTUAL CONTENTS OF
1687                                     ;BUFFER ACTIVE REGISTER
1688 005316 104000 HLT 0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
1689 005320 022777 000001 010036 4$: CMP #1,JDHBA ;WAS BUS ADDRESS INCREMENTED
1690 005326 001405 BEQ 5$
1691 005330 017704 010030 MOV JDHBA,R4 ;(R4)=ACTUAL CONTENTS
1692                                     ;OF BUS ADDRESS MEMORY FOR
1693                                     ;LINE 7
1694 005334 012705 000001 MOV #1,R5 ;(R5)=EXPECTED VALUE OF
1695                                     ;BUS ADDRESS MEMORY FOR
1696                                     ;LINE 7, 1
1697 005340 104003 HLT 3 ;BUS ADDRESS NOT UPDATED
1698                                     ;CORRECTLY, ERROR
1699 005342 005777 010020 5$: TST JDHBC ;DID BYTE COUNT DECREMENT TO 0
1700 005346 001416 BEQ 6$
1701 005350 017704 010012 MOV JDHBC,R4 ;(R4)=ACTUAL VALUE OF BYTE
1702                                     ;COUNT FOR LINE 7
1703 005354 005005 CLR R5 ;(R5)=EXPECTED VALUE OF BYTE
1704                                     ;COUNT FOR LINE 7, 0
1705 005356 104004 HLT 4 ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1706 005360 016777 010016 010012 MOV DHRLVL,JDHRVEC ;RESTORE TRAPCATCHER
1707 005366 005077 010010 CLR JDHRLVL
1708 005372 016777 010010 010004 MOV DHTLVL,JDHTVEC
1709 005400 005077 010002 CLR JDHTLVL
    
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1710 005404 012706 017102      6$:  MOV      #STACK,SP      ;RESTORE STACK
1711 005410 104400                SCOPE                    ;CHECK FOR ITERATIONS, LOOP
1712
1713                ;NPR LOGIC TEST
1714                ;SET BYTE COUNT TO 1 FOR LINE 10
1715                ;SET BAR BIT FOR LINE 10
1716                ;DELAY FOR NPR
1717                ;VERIFY THAT BAR BIT FOR LINE 10 CLEARS
1718                ;VERIFY THAT TRANSMITTER DONE IS SET
1719
1720 005412 012767 000340 172356 T20:  MOV      #340,PS        ;DISABLE ALL INTERRUPTS
1721 005420 012767 000020 007776      MOV      #20,ICOUNT     ;SET UP FOR 20 ITERATIONS
1722 005426 012767 005642 007764      MOV      #6$,ESCAPE     ;SET UP TO ESCAPE TO NEXT TEST
1723 005434 012777 004000 007714      MOV      #BIT11,ADHSCR  ;ISSUE MASTER CLEAR
1724 005442 004767 007616      JSR      PC,CLEAR      ;CLEAR ALL BUS ADDRESS
1725                                ;AND BYTE COUNT MEMORY LOCATIONS
1726 005446 012777 005530 007730      MOV      #2$,ADHTVEC    ;SET UP TRANSMITTER
1727 005454 012777 000340 007724      MOV      #340,ADHTLVL  ;INTERRUPT VECTOR
1728 005462 012777 000010 007666      MOV      #10,ADHSCR    ;SELECT LINE 10
1729 005470 012777 177777 007670      MOV      #-1,ADHBC     ;SET BYTE COUNT TO 1
1730 005476 012700 001000      MOV      #1000,R0
1731 005502 012777 000400 007660      MOV      #400,ADHBAR   ;SET BAR BIT FOR
1732                                ;LINE 10
1733 005510 052777 020000 007640      BIS      #BIT13,ADHSCR ;SET TRANSMITTER INTERRUPT ENABLE
1734 005516 005067 172254      CLR      PS            ;ALLOW INTERRUPTS
1735 005522 005300                1$:  DEC      R0            ;DELAY FOR NPR
1736 005524 001376                BNE      1$
1737 005526 104001                HLT      1
1738 005530 005777 007622                2$:  TST      ADHSCR      ;NO INTERRUPT OCCURED, ERROR
1739                                ;VERIFY THAT TRANSMITTER
1740                                ;DONE IS SET
1741 005534 100401                BMI      3$
1742 005536 104002                HLT      2
1743 005540 005777 007624                3$:  TST      ADHBAR      ;TRANSMITTER DONE NOT SET, ERROR
1744 005544 001404                BEQ      4$            ;WAS BAR BIT CLEARED FOR LINE 10
1745 005546 005005                CLR      R5
1746                                ;(R5)=EXPECTED DATA IN
1747                                ;BUFFER ACTIVE REGISTER, 0
1748 005550 017704 007614                MOV      ADHBAR,R4    ;(R4)=ACTUAL CONTENTS OF
1749                                ;BUFFER ACTIVE REGISTER
1750 005554 104000                HLT      0            ;BUS ACTIVE BIT NOT CLEARED, ERROR
1751 005556 022777 000001 007600 4$:  CMP      #1,ADHBA     ;WAS BUS ADDRESS INCREMENTED
1752 005564 001405                BEQ      5$
1753 005566 017704 007572                MOV      ADHBA,R4    ;(R4)=ACTUAL CONTENTS
1754                                ;OF BUS ADDRESS MEMORY FOR
1755                                ;LINE 10
1756 005572 012705 000001                MOV      #1,R5        ;(R5)=EXPECTED VALUE OF
1757                                ;BUS ADDRESS MEMORY FOR
1758                                ;LINE 10, 1
1759 005576 104003                HLT      3            ;BUS ADDRESS NOT UPDATED
1760                                ;CORRECTLY, ERROR
1761 005600 005777 007562                5$:  TST      ADHBC      ;DID BYTE COUNT DECREMENT TO 0
1762 005604 001416                BEQ      6$
1763 005606 017704 007554                MOV      ADHBC,R4    ;(R4)=ACTUAL VALUE OF BYTE
1764                                ;COUNT FOR LINE 10
1765 005612 005005                CLR      R5          ;(R5)=EXPECTED VALUE OF BYTE
1766                                ;COUNT FOR LINE 10, 0
1767 005614 104004                HLT      4            ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR

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1766 005616 016777 007560 007554      MOV    DHRLVL,ADHRVEC ;RESTORE TRAPCATCHER
1767 005624 005077 007552                CLR    ADHRLVL
1768 005630 016777 007552 007546      MOV    DHTLVL,ADHTVEC
1769 005636 005077 007544                CLR    ADHTLVL
1770 005642 012706 017102      6$:   MOV    #STACK,SP ;RESTORE STACK
1771 005646 104400                SCOPE ;CHECK FOR ITERATIONS, LOOP
1772
1773                ;NPR LOGIC TEST
1774                ;SET BYTE COUNT TO 1 FOR LINE 11
1775                ;SET BAR BIT FOR LINE 11
1776                ;DELAY FOR NPR
1777                ;VERIFY THAT BAR BIT FOR LINE 11 CLEARS
1778                ;VERIFY THAT TRANSMITTER DONE IS SET
1779
1780 005650 012767 000340 172120 T21:  MOV    #340,PS ;DISABLE ALL INTERRUPTS
1781 005656 012767 000020 007540      MOV    #20,COUNT ;SET UP FOR 20 ITERATIONS
1782 005664 012767 006100 007526      MOV    #6$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1783 005672 012777 004000 007456      MOV    #BIT11,ADHSCR ;ISSUE MASTER CLEAR
1784 005700 004767 007360      JSR    PC,CLEAR ;CLEAR ALL BUS ADDRESS
1785                ;AND BYTE COUNT MEMORY LOCATIONS
1786 005704 012777 005766 007472      MOV    #2$,ADHTVEC ;SET UP TRANSMITTER
1787 005712 012777 000340 007466      MOV    #340,ADHTLVL ;INTERRUPT VECTOR
1788 005720 012777 000011 007430      MOV    #11,ADHSCR ;SELECT LINE 11
1789 005726 012777 177777 007432      MOV    #-1,ADHBC ;SET BYTE COUNT TO 1
1790 005734 012700 001000      MOV    #1000,R0
1791 005740 012777 001000 007422      MOV    #1000,ADHBAR ;SET BAR BIT FOR
1792                ;LINE 11
1793 005746 052777 020000 007402      BIS    #BIT13,ADHSCR ;SET TRANSMITTER INTERRUPT ENABLE
1794 005754 005067 172016      CLR    PS ;ALLOW INTERRUPTS
1795 005760 005300      1$:   DEC    R0 ;DELAY FOR NPR
1796 005762 001376      BNE   1$
1797 005764 104001      HLT   1 ;NO INTERRUPT OCCURED, ERROR
1798 005766 005777 007364      2$:   TST   ADHSCR ;VERIFY THAT TRANSMITTER
1799                ;DONE IS SET
1800 005772 100401      BMI   3$
1801 005774 104002      HLT   2 ;TRANSMITTER DONE NOT SET, ERROR
1802 005776 005777 007366      3$:   TST   ADHBAR ;WAS BAR BIT CLEARED FOR LINE 11
1803 006002 001404      BEQ   4$
1804 006004 005005      CLR   R5 ;(R5)=EXPECTED DATA IN
1805                ;BUFFER ACTIVE REGISTER, 0
1806 006006 017704 007356      MOV    ADHBAR,R4 ;(R4)=ACTUAL CONTENTS OF
1807                ;BUFFER ACTIVE REGISTER
1808 006012 104000      HLT   0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
1809 006014 022777 000001 007342 4$:   CMP    #1,ADHBA ;WAS BUS ADDRESS INCREMENTED
1810 006022 001405      BEQ   5$
1811 006024 017704 007334      MOV    ADHBA,R4 ;(R4)=ACTUAL CONTENTS
1812                ;OF BUS ADDRESS MEMORY FOR
1813                ;LINE 11
1814 006030 012705 000001      MOV    #1,R5 ;(R5)=EXPECTED VALUE OF
1815                ;BUS ADDRESS MEMORY FOR
1816                ;LINE 11, 1
1817 006034 104003      HLT   3 ;BUS ADDRESS NOT UPDATED
1818                ;CORRECTLY, ERROR
1819 006036 005777 007324      5$:   TST   ADHBC ;DID BYTE COUNT DECREMENT TO 0
1820 006042 001416      BEQ   6$
1821 006044 017704 007316      MOV    ADHBC,R4 ;(R4)=ACTUAL VALUE OF BYTE

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1822                                     ;COUNT FOR LINE 11
1823 006050 005005          CLR      R5          ;(R5)=EXPECTED VALUE OF BYTE
1824                                     ;COUNT FOR LINE 11, 0
1825 006052 104004          HLT      4          ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1826 006054 016777 007322 007316      MOV     DHRLVL, @DHRVEC ;RESTORE TRAPCATCHER
1827 006062 005077 007314          CLR     @DHRLVL
1828 006066 016777 007314 007310      MOV     DHTLVL, @DHTVEC
1829 006074 005077 007306          CLR     @DHTLVL
1830 006100 012706 017102 6$:      MOV     #STACK, SP      ;RESTORE STACK
1831 006104 104400          SCOPE      ;CHECK FOR ITERATIONS, LOOP
1832
1833                                     ;NPR LOGIC TEST
1834                                     ;SET BYTE COUNT TO 1 FOR LINE 12
1835                                     ;SET BAR BIT FOR LINE 12
1836                                     ;DELAY FOR NPR
1837                                     ;VERIFY THAT BAR BIT FOR LINE 12 CLEARS
1838                                     ;VERIFY THAT TRANSMITTER DONE IS SET
1839
1840 006106 012767 000340 171662 T22:  MOV     #340, PS      ;DISABLE ALL INTERRUPTS
1841 006114 012767 000020 007302      MOV     #20, COUNT      ;SET UP FOR 20 ITERATIONS
1842 006122 012767 006336 007270      MOV     #6$, ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1843 006130 012777 004000 007220      MOV     #BIT11, @DHSCR   ;ISSUE MASTER CLEAR
1844 006136 004767 007122          JSR     PC, CLEAR        ;CLEAR ALL BUS ADDRESS
1845                                     ;AND BYTE COUNT MEMORY LOCATIONS
1846 006142 012777 006224 007234      MOV     #2$, @DHTVEC      ;SET UP TRANSMITTER
1847 006150 012777 000340 007230      MOV     #340, @DHTLVL    ;INTERRUPT VECTOR
1848 006156 012777 000012 007172      MOV     #12, @DHSCR      ;SELECT LINE 12
1849 006164 012777 177777 007174      MOV     #-1, @DHBC       ;SET BYTE COUNT TO 1
1850 006172 012700 001000          MOV     #1000, RO
1851 006176 012777 002000 007164      MOV     #2000, @DHBAR    ;SET BAR BIT FOR
1852                                     ;LINE 12
1853 006204 052777 020000 007144      BIS     #BIT13, @DHSCR   ;SET TRANSMITTER INTERRUPT ENABLE
1854 006212 005067 171560          CLR     PS              ;ALLOW INTERRUPTS
1855 006216 005300 1$:      DEC     RO              ;DELAY FOR NPR
1856 006220 001376          BNE     1$
1857 006222 104001          HLT     1              ;NO INTERRUPT OCCURED, ERROR
1858 006224 005777 007126 2$:      TST     @DHSCR          ;VERIFY THAT TRANSMITTER
1859                                     ;DONE IS SET
1860 006230 100401          BMI     3$
1861 006232 104002          HLT     2              ;TRANSMITTER DONE NOT SET, ERROR
1862 006234 005777 007130 3$:      TST     @DHBAR          ;WAS BAR BIT CLEARED FOR LINE 12
1863 006240 001404          BEQ     4$
1864 006242 005005          CLR     R5
1865                                     ;(R5)=EXPECTED DATA IN
1866 006244 017704 007120      MOV     @DHBAR, R4      ;BUFFER ACTIVE REGISTER, 0
1867                                     ;(R4)=ACTUAL CONTENTS OF
1868                                     ;BUFFER ACTIVE REGISTER
1868 006250 104000          HLT     0              ;BUS ACTIVE BIT NOT CLEARED, ERROR
1869 006252 022777 000001 007104 4$:  CMP     #1, @DHBA       ;WAS BUS ADDRESS INCREMENTED
1870 006260 001405          BEQ     5$
1871 006262 017704 007076      MOV     @DHBA, R4
1872                                     ;(R4)=ACTUAL CONTENTS
1873                                     ;OF BUS ADDRESS MEMORY FOR
1874 006266 012705 000001      MOV     #1, R5          ;LINE 12
1875                                     ;(R5)=EXPECTED VALUE OF
1876                                     ;BUS ADDRESS MEMORY FOR
1876                                     ;LINE 12, 1
1877 006272 104003          HLT     3              ;BUS ADDRESS NOT UPDATED

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1878                                     ;CORRECTLY, ERROR
1879 006274 005777 007066          5$:  TST   3DHBC          ;DID BYTE COUNT DECREMENT TO 0
1880 006300 001416                    BEQ   6$
1881 006302 017704 007060          MOV   3DHBC,R4          ;(R4)=ACTUAL VALUE OF BYTE
1882                                     ;COUNT FOR LINE 12
1883 006306 005005                    CLR   R5              ;(R5)=EXPECTED VALUE OF BYTE
1884                                     ;COUNT FOR LINE 12, 0
1885 006310 104004                    HLT   4              ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1886 006312 016777 007064 007060    MOV   DHRLVL,3DHRVEC ;RESTORE TRAPCATCHER
1887 006320 005077 007056                    CLR   3DHRLVL
1888 006324 016777 007056 007052    MOV   DHTLVL,3DHTVEC
1889 006332 005077 007050                    CLR   3DHTLVL
1890 006336 012706 017102          6$:  MOV   #STACK,SP      ;RESTORE STACK
1891 006342 104400                    SCOPE                ;CHECK FOR ITERATIONS, LOOP
1892
1893                                     ;NPR LOGIC TEST
1894                                     ;SET BYTE COUNT TO 1 FOR LINE 13
1895                                     ;SET BAR BIT FOR LINE 13
1896                                     ;DELAY FOR NPR
1897                                     ;VERIFY THAT BAR BIT FOR LINE 13 CLEARS
1898                                     ;VERIFY THAT TRANSMITTER DONE IS SET
1899
1900 006344 012767 000340 171424    T23: MOV   #340,PS        ;DISABLE ALL INTERRUPTS
1901 006352 012767 000020 007044    MOV   #20,ICOUNT     ;SET UP FOR 20 ITERATIONS
1902 006360 012767 006574 007032    MOV   #6$,ESCAPE     ;SET UP TO ESCAPE TO NEXT TEST
1903 006366 012777 004000 006762    MOV   #BIT11,3DHSCR  ;ISSUE MASTER CLEAR
1904 006374 004767 006664                    JSR   PC,CLEAR        ;CLEAR ALL BUS ADDRESS
1905                                     ;AND BYTE COUNT MEMORY LOCATIONS
1906 006400 012777 006462 006776    MOV   #2$,3DHTVEC    ;SET UP TRANSMITTER
1907 006406 012777 000340 006772    MOV   #340,3DHTLVL   ;INTERRUPT VECTOR
1908 006414 012777 000013 006734    MOV   #13,3DHSCR     ;SELECT LINE 13
1909 006422 012777 177777 006736    MOV   #-1,3DHBC      ;SET BYTE COUNT TO 1
1910 006430 012700 001000                    MOV   #1000,R0
1911 006434 012777 004000 006726    MOV   #4000,3DHBAR   ;SET BAR BIT FOR
1912                                     ;LINE 13
1913 006442 052777 020000 006706    BIS   #BIT13,3DHSCR  ;SET TRANSMITTER INTERRUPT ENABLE
1914 006450 005067 171322                    CLR   PS              ;ALLOW INTERRUPTS
1915 006454 005300          1$:  DEC   R0              ;DELAY FOR NPR
1916 006456 001376                    BNE   1$
1917 006460 104001                    HLT   1              ;NO INTERRUPT OCCURED, ERROR
1918 006462 005777 006670          2$:  TST   3DHSCR        ;VERIFY THAT TRANSMITTER
1919                                     ;DONE IS SET
1920 006466 100401                    BMI   3$
1921 006470 104002                    HLT   2              ;TRANSMITTER DONE NOT SET, ERROR
1922 006472 005777 006672          3$:  TST   3DHBAR        ;WAS BAR BIT CLEARED FOR LINE 13
1923 006476 001404                    BEQ   4$
1924 006500 005005                    CLR   R5              ;(R5)=EXPECTED DATA IN
1925                                     ;BUFFER ACTIVE REGISTER, 0
1926 006502 017704 006662                    MOV   3DHBAR,R4      ;(R4)=ACTUAL CONTENTS OF
1927                                     ;BUFFER ACTIVE REGISTER
1928 006506 104000                    HLT   0              ;BUS ACTIVE BIT NOT CLEARED, ERROR
1929 006510 022777 000001 006646    4$:  CMP   #1,3DHBA     ;WAS BUS ADDRESS INCREMENTED
1930 006516 001405                    BEQ   5$
1931 006520 017704 006640                    MOV   3DHBA,R4      ;(R4)=ACTUAL CONTENTS
1932                                     ;OF BUS ADDRESS MEMORY FOR
1933                                     ;LINE 13

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1990 006754 001405      BEQ      5$
1991 006756 017704 006402      MOV      3DHBA,R4      ;(R4)=ACTUAL CONTENTS
1992 006762 012705 000001      MOV      #1,R5        ;OF BUS ADDRESS MEMORY FOR
1993 006766 104003      HLT      3            ;LINE 14
1994 006770 005777 006372      5$: TST      3DHBC      ;(R5)=EXPECTED VALUE OF
1995 006774 001416      BEQ      6$          ;BUS ADDRESS MEMORY FOR
1996 006776 017704 006364      MOV      3DHBC,R4      ;LINE 14
1997 007002 005005      CLR      R5          ;BUS ADDRESS NOT UPDATED
1998 007004 104004      HLT      4            ;CORRECTLY, ERROR
1999 007006 016777 006370 006364      MOV      DHRVLV,3DHVEC ;DID BYTE COUNT DECREMENT TO 0
2000 007014 005077 006362      CLR      3DHRVLV      ;(R4)=ACTUAL VALUE OF BYTE
2001 007020 016777 006362 006356      MOV      DHTLVL,3DHTVEC ;COUNT FOR LINE 14
2002 007026 005077 006354      CLR      3DHTLVL      ;(R5)=EXPECTED VALUE OF BYTE
2003 007032 012706 017102      6$: MOV      #STACK,SP ;COUNT FOR LINE 14, 0
2004 007036 104400      SCOPE                ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
2005 007040 012767 000340 170730      T25: MOV      #340,PS   ;RESTORE TRAPCATCHER
2006 007046 012767 000020 006350      MOV      #20,COUNT    ;
2007 007054 012767 007270 006336      MOV      #6$,ESCAPE   ;
2008 007062 012777 004000 006266      MOV      #BIT11,3DHSCR ;DISABLE ALL INTERRUPTS
2009 007070 004767 006170      JSR      PC,CLEAR     ;SET UP FOR 20 ITERATIONS
2010 007074 012777 007156 006302      MOV      #2$,3DHTVEC  ;SET UP TO ESCAPE TO NEXT TEST
2011 007102 012777 000340 006276      MOV      #340,3DHTLVL ;ISSUE MASTER CLEAR
2012 007110 012777 000015 006240      MOV      #1$,3DHSCR   ;CLEAR ALL BUS ADDRESS
2013 007116 012777 177777 006242      MOV      #-1,3DHBC    ;AND BYTE COUNT MEMORY LOCATIONS
2014 007124 012700 001000      MOV      #1000,R0     ;SET UP TRANSMITTER
2015 007130 012777 020000 006232      MOV      #20000,3DHBAR ;INTERRUPT VECTOR
2016 007136 052777 020000 006212      BIS      #BIT13,3DHSCR ;SELECT LINE 15
2017 007144 005067 170626      CLR      PS           ;SET TRANSMITTER INTERRUPT ENABLE
2018 007150 005300      1$: DEC      R0        ;ALLOW INTERRUPTS
2019 007152 001376      BNE     1$           ;DELAY FOR NPR
2020 007154 104001      HLT     1            ;NO INTERRUPT OCCURED, ERROR
2021 007156 005777 006174      2$: TST      3DHSCR    ;VERIFY THAT TRANSMITTER
2022 007162 100401      BMI     3$          ;DONE IS SET
2023 007164 104002      HLT     2            ;TRANSMITTER DONE NOT SET, ERROR
2024 007166 005777 006176      3$: TST      3DHBAR    ;WAS BAR BIT CLEARED FOR LINE 15
2025 007172 001404      BEQ     4$          ;
2026 007174 005005      CLR     R5          ;(R5)=EXPECTED DATA IN
2027 007174 005005      CLR     R5          ;BUFFER ACTIVE REGISTER, 0

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0046 007176 017704 006166      MOV      3DHBAR,R4      ;(R4)=ACTUAL CONTENTS OF
0047 007202 104000      HLT      0              ;BUFFER ACTIVE REGISTER
0048 007204 022777 000001 006152 4$:    CMP      #1,3DHBA      ;BUS ACTIVE BIT NOT CLEARED, ERROR
0049 007212 001405      BEQ      5$              ;WAS BUS ADDRESS INCREMENTED
0050 007214 017704 006144      MOV      3DHBA,R4      ;(R4)=ACTUAL CONTENTS
0051 007220 012705 000001      MOV      #1,R5          ;OF BUS ADDRESS MEMORY FOR
0052 007224 104003      HLT      3              ;LINE 15
0053 007226 005777 006134      TST      3DHBC          ;(R5)=EXPECTED VALUE OF
0054 007232 001416      BEQ      6$              ;BUS ADDRESS MEMORY FOR
0055 007234 017704 006126      MOV      3DHBC,R4      ;LINE 15, 1
0056 007240 005005      CLR      R5             ;BUS ADDRESS NOT UPDATED
0057 007242 104004      HLT      4              ;CORRECTLY, ERROR
0058 007244 016777 006132 006126    MOV      DHRVLV,3DHVEC ;DID BYTE COUNT DECREMENT TO 0
0059 007252 005077 006124      CLR      3DHRVLV        ;RESTORE TRAPCATCHER
0060 007256 016777 006124 006120    MOV      DHTLVL,3DHTVEC
0061 007264 005077 006116      CLR      3DHTLVL
0062 007270 012706 017102 6$:    MOV      #STACK,SP     ;RESTORE STACK
0063 007274 104400      SCOPE                   ;CHECK FOR ITERATIONS, LOOP
0064 007300 012706 017102 6$:    ;NPR LOGIC TEST
0065 007304 012706 017102 6$:    ;SET BYTE COUNT TO 1 FOR LINE 16
0066 007308 012706 017102 6$:    ;SET BAR BIT FOR LINE 16
0067 007312 012706 017102 6$:    ;DELAY FOR NPR
0068 007316 012706 017102 6$:    ;VERIFY THAT BAR BIT FOR LINE 16 CLEARS
0069 007320 012706 017102 6$:    ;VERIFY THAT TRANSMITTER DONE IS SET
0070 007324 012706 017102 6$:
0071 007328 012706 017102 6$:
0072 007332 012706 017102 6$:
0073 007336 012706 017102 6$:
0074 007340 012706 017102 6$:
0075 007344 012706 017102 6$:
0076 007348 012706 017102 6$:
0077 007352 012706 017102 6$:
0078 007356 012706 017102 6$:
0079 007360 012706 017102 6$:
0080 007276 012767 000340 170472 T26:  MOV      #340,PS        ;DISABLE ALL INTERRUPTS
0081 007304 012767 000020 006112    MOV      #20,ICOUNT     ;SET UP FOR 20 ITERATIONS
0082 007312 012767 007526 006100    MOV      #6$,ESCAPE     ;SET UP TO ESCAPE TO NEXT TEST
0083 007320 012777 004000 006030    MOV      #BIT11,3DHSCR  ;ISSUE MASTER CLEAR
0084 007326 004767 005732      JSR      PC,CLEAR       ;CLEAR ALL BUS ADDRESS
0085 007332 012777 007414 006044      MOV      #2$,3DHTVEC    ;AND BYTE COUNT MEMORY LOCATIONS
0086 007340 012777 000340 006040      MOV      #340,3DHTLVL  ;SET UP TRANSMITTER
0087 007346 012777 000016 006002      MOV      #16,3DHSCR    ;INTERRUPT VECTOR
0088 007354 012777 177777 006004      MOV      #-1,3DHBC     ;SELECT LINE 16
0089 007362 012700 001000      MOV      #1000,R0       ;SET BYTE COUNT TO 1
0090 007366 012777 040000 005774      MOV      #40000,3DHBAR ;SET BAR BIT FOR
0091 007374 052777 020000 005754      BIS      #BIT13,3DHSCR ;LINE 16
0092 007402 005067 170370      CLR      PS             ;SET TRANSMITTER INTERRUPT ENABLE
0093 007406 005300      DEC      R0             ;ALLOW INTERRUPTS
0094 007410 001376      BNE     1$              ;DELAY FOR NPR
0095 007412 104001      HLT     1$              ;NO INTERRUPT OCCURED, ERROR
0096 007414 005777 005736 2$:    TST     3DHSCR          ;VERIFY THAT TRANSMITTER
0097 007420 100401      BMI     3$              ;DONE IS SET
0098 007422 104002      HLT     2$              ;TRANSMITTER DONE NOT SET, ERROR

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2102 007424 005777 005740 3$: TST 3DHBAR ;WAS BAR BIT CLEARED FOR LINE 16
2103 007430 001404 BEQ 4$
2104 007432 005005 CLR R5 ;(R5)=EXPECTED DATA IN
;BUFFER ACTIVE REGISTER, 0
2105 007434 017704 005730 MOV 3DHBAR,R4 ;(R4)=ACTUAL CONTENTS OF
;BUFFER ACTIVE REGISTER
2106 007440 104000 HLT 0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
2107 007442 022777 000001 005714 4$: CMP #1,3DHBA ;WAS BUS ADDRESS INCREMENTED
2108 007450 001405 BEQ 5$
2109 007452 017704 005706 MOV 3DHBA,R4 ;(R4)=ACTUAL CONTENTS
;OF BUS ADDRESS MEMORY FOR
;LINE 16
2110 007456 012705 000001 MOV #1,R5 ;(R5)=EXPECTED VALUE OF
;BUS ADDRESS MEMORY FOR
;LINE 16, 1
2111 007462 104003 HLT 3 ;BUS ADDRESS NOT UPDATED
;CORRECTLY, ERROR
2112 007464 005777 005676 5$: TST 3DHBC ;DID BYTE COUNT DECREMENT TO 0
2113 007470 001416 BEQ 6$
2114 007472 017704 005670 MOV 3DHBC,R4 ;(R4)=ACTUAL VALUE OF BYTE
;COUNT FOR LINE 16
2115 007476 005005 CLR R5 ;(R5)=EXPECTED VALUE OF BYTE
;COUNT FOR LINE 16, 0
2116 007500 104004 HLT 4 ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
2117 007502 016777 005674 005670 MOV DHRLVL,3DHRVEC ;RESTORE TRAPCATCHER
2118 007510 005077 005666 CLR 3DHRLVL
2119 007514 016777 005666 005662 MOV DHTLVL,3DHTVEC
2120 007522 005077 005660 CLR 3DHTLVL
2121 007526 012706 017102 6$: MOV #STACK,SP ;RESTORE STACK
2122 007532 104400 SCOPE ;CHECK FOR ITERATIONS, LOOP
;NPR LOGIC TEST
;SET BYTE COUNT TO 1 FOR LINE 17
;SET BAR BIT FOR LINE 17
;DELAY FOR NPR
;VERIFY THAT BAR BIT FOR LINE 17 CLEARS
;VERIFY THAT TRANSMITTER DONE IS SET
2140 007534 012767 000340 170234 T27: MOV #340,PS ;DISABLE ALL INTERRUPTS
2141 007542 012767 000020 005654 MOV #20,COUNT ;SET UP FOR 20 ITERATIONS
2142 007550 012767 007764 005642 MOV #6$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2143 007556 012777 004000 005572 MOV #BIT11,3DHSCR ;ISSUE MASTER CLEAR
2144 007564 004767 005474 JSR PC,CLEAR ;CLEAR ALL BUS ADDRESS
;AND BYTE COUNT MEMORY LOCATIONS
2145 007570 012777 007652 005606 MOV #2$,3DHTVEC ;SET UP TRANSMITTER
2146 007576 012777 000340 005602 MOV #340,3DHTLVL ;INTERRUPT VECTOR
2147 007604 012777 000017 005544 MOV #17,3DHSCR ;SELECT LINE 17
2148 007612 012777 177777 005546 MOV #-1,3DHBC ;SET BYTE COUNT TO 1
2149 007620 012700 001000 MOV #1000,R0
2150 007624 012777 100000 005536 MOV #100000,3DHBAR ;SET BAR BIT FOR
;LINE 17
2151 007632 052777 020000 005516 BIS #BIT13,3DHSCR ;SET TRANSMITTER INTERRUPT ENABLE
2152 007640 005067 170132 CLR PS ;ALLOW INTERRUPTS
2153 007644 005300 1$: DEC R0 ;DELAY FOR NPR
2154 007646 001376 BNE 1$
2155 007650 104001 HLT 1 ;NO INTERRUPT OCCURED, ERROR

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2158 007652 005777 005500      2$:  TST      QDHSCR      ;VERIFY THAT TRANSMITTER
2159                                     ;DONE IS SET
2160 007656 100401              BMI      3$
2161 007660 104002              HLT
2162 007662 005777 005502      3$:  TST      QDHBAR      ;TRANSMITTER DONE NOT SET, ERROR
2163 007666 001404              BEQ      4$           ;WAS BAR BIT CLEARED FOR LINE 17
2164 007670 005005              CLR      R5
2165                                     ;(R5)=EXPECTED DATA IN
2166 007672 017704 005472      MOV      QDHBAR,R4    ;BUFFER ACTIVE REGISTER, 0
2167                                     ;(R4)=ACTUAL CONTENTS OF
2168 007676 104000              HLT
2169 007700 022777 000001 005456 4$:  CMP      #1,QDHBA    ;BUFFER ACTIVE REGISTER
2170 007706 001405              BEQ      5$           ;BUS ACTIVE BIT NOT CLEARED, ERROR
2171 007710 017704 005450      MOV      QDHBA,R4    ;WAS BUS ADDRESS INCREMENTED
2172                                     ;(R4)=ACTUAL CONTENTS
2173                                     ;OF BUS ADDRESS MEMORY FOR
2174 007714 012705 000001      MOV      #1,R5       ;LINE 17
2175                                     ;(R5)=EXPECTED VALUE OF
2176                                     ;BUS ADDRESS MEMORY FOR
2177 007720 104003              HLT      3           ;LINE 17, 1
2178                                     ;BUS ADDRESS NOT UPDATED
2179 007722 005777 005440      5$:  TST      QDHBC      ;CORRECTLY, ERROR
2180 007726 001416              BEQ      6$           ;DID BYTE COUNT DECREMENT TO 0
2181 007730 017704 005432      MOV      QDHBC,R4
2182                                     ;(R4)=ACTUAL VALUE OF BYTE
2183 007734 005005              CLR      R5          ;COUNT FOR LINE 17
2184                                     ;(R5)=EXPECTED VALUE OF BYTE
2185 007736 104004              HLT      4           ;COUNT FOR LINE 17, 0
2186 007740 016777 005436 005432  MOV      DHRVLV,QDHVEC ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
2187 007746 005077 005430      CLR      QDHRVLV    ;RESTORE TRAPCATCHER
2188 007752 016777 005430 005424  MOV      DHTLVL,QDHTVEC
2189 007760 005077 005422      CLR      QDHTLVL
2190 007764 012706 017102      6$:  MOV      #STACK,SP  ;RESTORE STACK
2191 007770 104400              SCOPE              ;CHECK FOR ITERATIONS, LOOP
2192
2193                                     ;NPR LOGIC TEST
2194                                     ;SET BYTE COUNT ON ALL LINES TO 1
2195                                     ;SET BAR BIT FOR LINE 0
2196                                     ;VERIFY THAT BYTE COUNT FOR LINE 0 GOES TO 0
2197                                     ;VERIFY THAT BUS ADDRESS FOR LINE 0 IS INCREMENTED
2198                                     ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2199                                     ;ARE UNCHANGED
2200
2201 007772 012767 000340 167776 T30:  MOV      #340,PS     ;DISABLE ALL INTERRUPTS
2202 010000 012767 000010 005416      MOV      #10,ICOUNT  ;SET UP FOR 10 ITERATIONS
2203 010006 012767 010140 005404      MOV      #8$,ESCAPE  ;SET UP TO ESCAPE TO NEXT TEST
2204 010014 012777 004000 005334      MOV      #BIT11,QDHSCR ;MASTER CLEAR INTERFACE
2205                                     ;TO SET ALL TBMT BITS
2206 010022 004767 005236      JSR      PC,CLEAR    ;CLEAR ALL BYTE COUNT AND
2207                                     ;BUS ADDRESS MEMORY LOCATIONS
2208 010026 004767 005264      JSR      PC,LOAD     ;SET ALL BYTE COUNT LOCATIONS TO -1
2209 010032 012777 000001 005330      MOV      #1,QDHBAR   ;SET BAR BIT FOR LINE 0
2210 010040 005777 005312      3$:  TST      QDHSCR      ;WAIT FOR TRANSMITTER DONE
2211 010044 100375              BPL      3$
2212 010046 012700 000020      MOV      #20,R0     ;SET UP TO CHECK ALL 16 LINES
2213 010052 005077 005300      CLR      QDHSCR      ;START AT LINE 0
  
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2214	010056	005001				CLR	R1		:KEEP TRACK OF LINE NUMBER
2215	010060	012705	177777		4\$:	MOV	#-1,R5		:(R5)=EXPECTED BYTE COUNT,
2216									:IF LINE NUMBER NOT = 0
2217	010064	005003				CLR	R3		:(R3)=EXPECTED BUS ADDRESS,
2218									:IF LINE NUMBER NOT = 0
2219	010066	017704	005274			MOV	JDHBC,R4		:(R4)=ACTUAL BYTE ACCOUNT
2220	010072	017702	005266			MOV	JDHBA,R2		:(R5)=ACTUAL BUS ADDRESS
2221	010076	027727	005254	000000		CMP	JDHSCR,#0		:IF LINE BEING COMPARED IS LINE 0
2222	010104	001002				BNE	5\$		
2223	010106	005005				CLR	R5		:EXPECTED BYTE COUNT=0
2224	010110	005203				INC	R3		:EXPECTED BUS ADDRESS = 1
2225	010112	020504			5\$:	CMP	R5,R4		:IS BYTE COUNT CORRECT
2226	010114	001401				BEQ	6\$		
2227	010116	104004				HLT	4		:BYTE COUNT ERROR
2228	010120	020302			6\$:	CMP	R3,R2		:IS BUS ADDRESS CORRECT
2229	010122	001401				BEQ	7\$		
2230	010124	104003				HLT	3		:BUS ADDRESS ERROR
2231	010126	005277	005224		7\$:	INC	JDHSCR		:PREPARE TO CHECK NEXT LINE
2232	010132	005201				INC	R1		
2233	010134	005300				DEC	R0		:CONTINUE IF ALL NOT DONE
2234	010136	001350				BNE	4\$		
2235	010140	104400			8\$:	SCOPE			:CHECK FOR ITERATIONS, LOOP
2236									
2237									
2238									
2239									
2240									
2241									
2242									
2243									
2244									
2245	010142	012767	000340	167626	T31:	MOV	#340,PS		:DISABLE ALL INTERRUPTS
2246	010150	012767	000010	005246		MOV	#10,ICOUNT		:SET UP FOR 10 ITERATIONS
2247	010156	012767	010310	005234		MOV	#8\$,ESCAPE		:SET UP TO ESCAPE TO NEXT TEST
2248	010164	012777	004000	005164		MOV	#BIT11,JDHSCR		:MASTER CLEAR INTERFACE
2249									:TO SET ALL TBMT BITS
2250	010172	004767	005066			JSR	PC,CLEAR		:CLEAR ALL BYTE COUNT AND
2251									:BUS ADDRESS MEMORY LOCATIONS
2252	010176	004767	005114			JSR	PC,LOAD		:SET ALL BYTE COUNT LOCATIONS TO -1
2253	010202	012777	000002	005160		MOV	#2,JDHBAR		:SET BAR BIT FOR LINE 1
2254	010210	005777	005142		3\$:	TST	JDHSCR		:WAIT FOR TRANSMITTER DONE
2255	010214	100375				BPL	3\$		
2256	010216	012700	000020			MOV	#20,R0		:SET UP TO CHECK ALL 16 LINES
2257	010222	005077	005130			CLR	JDHSCR		:START AT LINE 0
2258	010226	005001				CLR	R1		:KEEP TRACK OF LINE NUMBER
2259	010230	012705	177777		4\$:	MOV	#-1,R5		:(R5)=EXPECTED BYTE COUNT,
2260									:IF LINE NUMBER NOT = 1
2261	010234	005003				CLR	R3		:(R3)=EXPECTED BUS ADDRESS,
2262									:IF LINE NUMBER NOT = 1
2263	010236	017704	005124			MOV	JDHBC,R4		:(R4)=ACTUAL BYTE ACCOUNT
2264	010242	017702	005116			MOV	JDHBA,R2		:(R5)=ACTUAL BUS ADDRESS
2265	010246	027727	005104	000001		CMP	JDHSCR,#1		:IF LINE BEING COMPARED IS LINE 1
2266	010254	001002				BNE	5\$		
2267	010256	005005				CLR	R5		:EXPECTED BYTE COUNT=0
2268	010260	005203				INC	R3		:EXPECTED BUS ADDRESS = 1
2269	010262	020504			5\$:	CMP	R5,R4		:IS BYTE COUNT CORRECT

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: NPR LOGIC TEST
: SET BYTE COUNT ON ALL LINES TO 1
: SET BAR BIT FOR LINE 1
: VERIFY THAT BYTE COUNT FOR LINE 1 GOES TO 0
: VERIFY THAT BUS ADDRESS FOR LINE 1 IS INCREMENTED
: VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
: ARE UNCHANGED
    
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2326      ;SET BYTE COUNT ON ALL LINES TO 1
2327      ;SET BAR BIT FOR LINE 3
2328      ;VERIFY THAT BYTE COUNT FOR LINE 3 GOES TO 0
2329      ;VERIFY THAT BUS ADDRESS FOR LINE 3 IS INCREMENTED
2330      ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2331      ;ARE UNCHANGED
2332
2333 010462 012767 000340 167306 T33: MOV #340,PS ;DISABLE ALL INTERRUPTS
2334 010470 012767 000010 004726 MOV #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2335 010476 012767 010630 004714 MOV #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2336 010504 012777 004000 004644 MOV #BIT11,JDHSCR ;MASTER CLEAR INTERFACE
2337 ;TO SET ALL TBMT BITS
2338 010512 004767 004546 JSR PC,CLEAR ;CLEAR ALL BYTE COUNT AND
2339 ;BUS ADDRESS MEMORY LOCATIONS
2340 010516 004767 004574 JSR PC,LOAD ;SET ALL BYTE COUNT LOCATIONS TO -1
2341 010522 012777 000010 004640 MOV #10,JDHBAR ;SET BAR BIT FOR LINE 3
2342 010530 005777 004622 3$: TST JDHSCR ;WAIT FOR TRANSMITTER DONE
2343 010534 100375 BPL 3$
2344 010536 012700 000020 MOV #20,R0 ;SET UP TO CHECK ALL 16 LINES
2345 010542 005077 004610 CLR JDHSCR ;START AT LINE 0
2346 010546 005001 CLR R1 ;KEEP TRACK OF LINE NUMBER
2347 010550 012705 177777 4$: MOV #-1,R5 ;(R5)=EXPECTED BYTE COUNT,
2348 ;IF LINE NUMBER NOT = 3
2349 010554 005003 CLR R3 ;(R3)=EXPECTED BUS ADDRESS,
2350 ;IF LINE NUMBER NOT = 3
2351 010556 017704 004604 MOV JDHBC,R4 ;(R4)=ACTUAL BYTE ACOUNT
2352 010562 017702 004576 MOV JDHBA,R2 ;(R5)=ACTUAL BUS ADDRESS
2353 010566 027727 004564 000003 CMP JDHSCR,#3 ;IF LINE BEING COMPARED IS LINE 3
2354 010574 001002 BNE 5$
2355 010576 005005 CLR R5 ;EXPECTED BYTE COUNT=0
2356 010600 005203 INC R3 ;EXPECTED BUS ADDRESS = 1
2357 010602 020504 5$: CMP R5,R4 ;IS BYTE COUNT CORRECT
2358 010604 001401 BEQ 6$
2359 010606 104004 HLT 4 ;BYTE COUNT ERROR
2360 010610 020302 6$: CMP R3,R2 ;IS BUS ADDRESS CORRECT
2361 010612 001401 BEQ 7$
2362 010614 104003 HLT 3 ;BUS ADDRESS ERROR
2363 010616 005277 004534 7$: INC JDHSCR ;PREPARE TO CHECK NEXT LINE
2364 010622 005201 INC R1
2365 010624 005300 DEC R0 ;CONTINUE IF ALL NOT DONE
2366 010626 001350 BNE 4$
2367 010630 104400 8$: SCOPE ;CHECK FOR ITERATIONS, LOOP
2368
2369 ;NPR LOGIC TEST
2370 ;SET BYTE COUNT ON ALL LINES TO 1
2371 ;SET BAR BIT FOR LINE 4
2372 ;VERIFY THAT BYTE COUNT FOR LINE 4 GOES TO 0
2373 ;VERIFY THAT BUS ADDRESS FOR LINE 4 IS INCREMENTED
2374 ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2375 ;ARE UNCHANGED
2376
2377 010632 012767 000340 167136 T34: MOV #340,PS ;DISABLE ALL INTERRUPTS
2378 010640 012767 000010 004556 MOV #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2379 010646 012767 011000 004544 MOV #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2380 010654 012777 004000 004474 MOV #BIT11,JDHSCR ;MASTER CLEAR INTERFACE
2381 ;TO SET ALL TBMT BITS

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2438                                     ; IF LINE NUMBER NOT = 5
2439 011076 017704 004264                MOV    @DHBC,R4                ; (R4)=ACTUAL BYTE ACOUNT
2440 011102 017702 004256                MOV    @DHBA,R2                ; (R5)=ACTUAL BUS ADDRESS
2441 011106 027727 004244 000005        CMP    @DHSCR,#5                ; IF LINE BEING COMPARED IS LINE 5
2442 011114 001002                        BNE    5$
2443 011116 005005                        CLR    R5                        ; EXPECTED BYTE COUNT=0
2444 011120 005203                        INC    R3                        ; EXPECTED BUS ADDRESS = 1
2445 011122 020504 5$:                   CMP    R5,R4                    ; IS BYTE COUNT CORRECT
2446 011124 001401                        BEQ    6$
2447 011126 104004                        HLT    4                        ; BYTE COUNT ERROR
2448 011130 020302 6$:                   CMP    R3,R2                    ; IS BUS ADDRESS CORRECT
2449 011132 001401                        BEQ    7$
2450 011134 104003                        HLT    3                        ; BUS ADDRESS ERROR
2451 011136 005277 004214 7$:           INC    @DHSCR                    ; PREPARE TO CHECK NEXT LINE
2452 011142 005201                        INC    R1
2453 011144 005300                        DEC    R0                        ; CONTINUE IF ALL NOT DONE
2454 011146 001350                        BNE    4$
2455 011150 104400 8$:                   SCOPE                            ; CHECK FOR ITERATIONS, LOOP
2456
2457                                     ; NPR LOGIC TEST
2458                                     ; SET BYTE COUNT ON ALL LINES TO 1
2459                                     ; SET BAR BIT FOR LINE 6
2460                                     ; VERIFY THAT BYTE COUNT FOR LINE 6 GOES TO 0
2461                                     ; VERIFY THAT BUS ADDRESS FOR LINE 6 IS INCREMENTED
2462                                     ; VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2463                                     ; ARE UNCHANGED
2464
2465 011152 012767 000340 166616 T36:    MOV    #340,PS                    ; DISABLE ALL INTERRUPTS
2466 011160 012767 000010 004236        MOV    #10,ICOUNT                ; SET UP FOR 10 ITERATIONS
2467 011166 012767 011320 004224        MOV    #8$,ESCAPE                ; SET UP TO ESCAPE TO NEXT TEST
2468 011174 012777 004000 004154        MOV    #BIT11,@DHSCR            ; MASTER CLEAR INTERFACE
2469                                     ; TO SET ALL TBMT BITS
2470 011202 004767 004056                JSR    PC,CLEAR                    ; CLEAR ALL BYTE COUNT AND
2471                                     ; BUS ADDRESS MEMORY LOCATIONS
2472 011206 004767 004104                JSR    PC,LOAD                    ; SET ALL BYTE COUNT LOCATIONS TO -1
2473 011212 012777 000100 004150        MOV    #100,@DHBAR              ; SET BAR BIT FOR LINE 6
2474 011220 005777 004132 3$:           TST    @DHSCR                    ; WAIT FOR TRANSMITTER DONE
2475 011224 100375                        BPL    3$
2476 011226 012700 000020                MOV    #20,R0                    ; SET UP TO CHECK ALL 16 LINES
2477 011232 005077 004120                CLR    @DHSCR                    ; START AT LINE 0
2478 011236 005001                        CLR    R1                        ; KEEP TRACK OF LINE NUMBER
2479 011240 012705 177777 4$:           MOV    #-1,R5                    ; (R5)=EXPECTED BYTE COUNT,
2480                                     ; IF LINE NUMBER NOT = 6
2481 011244 005003                        CLR    R3                        ; (R3)=EXPECTED BUS ADDRESS,
2482                                     ; IF LINE NUMBER NOT = 6
2483 011246 017704 004114                MOV    @DHBC,R4                    ; (R4)=ACTUAL BYTE ACOUNT
2484 011252 017702 004106                MOV    @DHBA,R2                    ; (R5)=ACTUAL BUS ADDRESS
2485 011256 027727 004074 000006        CMP    @DHSCR,#6                ; IF LINE BEING COMPARED IS LINE 6
2486 011264 001002                        BNE    5$
2487 011266 005005                        CLR    R5                        ; EXPECTED BYTE COUNT=0
2488 011270 005203                        INC    R3                        ; EXPECTED BUS ADDRESS = 1
2489 011272 020504 5$:                   CMP    R5,R4                    ; IS BYTE COUNT CORRECT
2490 011274 001401                        BEQ    6$
2491 011276 104004                        HLT    4                        ; BYTE COUNT ERROR
2492 011300 020302 6$:                   CMP    R3,R2                    ; IS BUS ADDRESS CORRECT
2493 011302 001401                        BEQ    7$

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2494 011304 104003          HLT      3          ;BUS ADDRESS ERROR
2495 011306 005277 004044 7$:      INC      3DHSCR    ;PREPARE TO CHECK NEXT LINE
2496 011312 005201          INC      R1
2497 011314 005300          DEC      R0          ;CONTINUE IF ALL NOT DONE
2498 011316 001350          BNE     4$
2499 011320 104400          8$:      SCOPE      ;CHECK FOR ITERATIONS, LOOP
2500
2501          ;NPR LOGIC TEST
2502          ;SET BYTE COUNT ON ALL LINES TO 1
2503          ;SET BAR BIT FOR LINE 7
2504          ;VERIFY THAT BYTE COUNT FOR LINE 7 GOES TO 0
2505          ;VERIFY THAT BUS ADDRESS FOR LINE 7 IS INCREMENTED
2506          ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2507          ;ARE UNCHANGED
2508
2509 011322 012767 000340 166446 T37:   MOV     #340,PS    ;DISABLE ALL INTERRUPTS
2510 011330 012767 000010 004066   MOV     #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2511 011336 012767 011470 004054   MOV     #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2512 011344 012777 004000 004004   MOV     #BIT11,3DHSCR ;MASTER CLEAR INTERFACE
2513          ;TO SET ALL TBMT BITS
2514 011352 004767 003706          JSR     PC,CLEAR   ;CLEAR ALL BYTE COUNT AND
2515          ;BUS ADDRESS MEMORY LOCATIONS
2516 011356 004767 003734          JSR     PC,LOAD    ;SET ALL BYTE COUNT LOCATIONS TO -1
2517 011362 012777 000200 004000   MOV     #200,3DHBAR ;SET BAR BIT FOR LINE 7
2518 011370 005777 003762          3$:     TST     3DHSCR   ;WAIT FOR TRANSMITTER DONE
2519 011374 100375          BPL     3$
2520 011376 012700 000020          MOV     #20,R0     ;SET UP TO CHECK ALL 16 LINES
2521 011402 005077 003750          CLR     3DHSCR    ;START AT LINE 0
2522 011406 005001          CLR     R1         ;KEEP TRACK OF LINE NUMBER
2523 011410 012705 177777          4$:     MOV     #-1,R5   ;(R5)=EXPECTED BYTE COUNT,
2524          ;IF LINE NUMBER NOT = 7
2525 011414 005003          CLR     R3         ;(R3)=EXPECTED BUS ADDRESS,
2526          ;IF LINE NUMBER NOT = 7
2527 011416 017704 003744          MOV     3DHBC,R4   ;(R4)=ACTUAL BYTE ACOUNT
2528 011422 017702 003736          MOV     3DHBA,R2   ;(R5)=ACTUAL BUS ADDRESS
2529 011426 027727 003724 000007   CMP     3DHSCR,#7  ;IF LINE BEING COMPARED IS LINE 7
2530 011434 001002          BNE     5$
2531 011436 005005          CLR     R5         ;EXPECTED BYTE COUNT=0
2532 011440 005203          INC     R3         ;EXPECTED BUS ADDRESS = 1
2533 011442 020504          5$:     CMP     R5,R4     ;IS BYTE COUNT CORRECT
2534 011444 001401          BEQ     6$
2535 011446 104004          HLT     4          ;BYTE COUNT ERROR
2536 011450 020302          6$:     CMP     R3,R2   ;IS BUS ADDRESS CORRECT
2537 011452 001401          BEQ     7$
2538 011454 104003          HLT     3          ;BUS ADDRESS ERROR
2539 011456 005277 003674 7$:     INC     3DHSCR    ;PREPARE TO CHECK NEXT LINE
2540 011462 005201          INC     R1
2541 011464 005300          DEC     R0          ;CONTINUE IF ALL NOT DONE
2542 011466 001350          BNE     4$
2543 011470 104400          8$:     SCOPE      ;CHECK FOR ITERATIONS, LOOP
2544
2545          ;NPR LOGIC TEST
2546          ;SET BYTE COUNT ON ALL LINES TO 1
2547          ;SET BAR BIT FOR LINE 10
2548          ;VERIFY THAT BYTE COUNT FOR LINE 10 GOES TO 0
2549          ;VERIFY THAT BUS ADDRESS FOR LINE 10 IS INCREMENTED

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2550                                     ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2551                                     ;ARE UNCHANGED
2552
2553 011472 012767 000340 166276 T40: MOV #340,PS ;DISABLE ALL INTERRUPTS
2554 011500 012767 000010 003716 MOV #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2555 011506 012767 011640 003704 MOV #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2556 011514 012777 004000 003634 MOV #BIT11,ADHSCR ;MASTER CLEAR INTERFACE
2557 ;TO SET ALL TBMT BITS
2558 011522 004767 003536 JSR PC,CLEAR ;CLEAR ALL BYTE COUNT AND
2559 ;BUS ADDRESS MEMORY LOCATIONS
2560 011526 004767 003564 JSR PC,LOAD ;SET ALL BYTE COUNT LOCATIONS TO -1
2561 011532 012777 000400 003630 MOV #400,ADHBAR ;SET BAR BIT FOR LINE 10
2562 011540 005777 003612 3$: TST ADHSCR ;WAIT FOR TRANSMITTER DONE
2563 011544 100375 BPL 3$
2564 011546 012700 000020 MOV #20,R0 ;SET UP TO CHECK ALL 16 LINES
2565 011552 005077 003600 CLR ADHSCR ;START AT LINE 0
2566 011556 005001 CLR R1 ;KEEP TRACK OF LINE NUMBER
2567 011560 012705 177777 4$: MOV #-1,R5 ;(R5)=EXPECTED BYTE COUNT,
2568 ;IF LINE NUMBER NOT = 10
2569 011564 005003 CLR R3 ;(R3)=EXPECTED BUS ADDRESS,
2570 ;IF LINE NUMBER NOT = 10
2571 011566 017704 003574 MOV ADHBC,R4 ;(R4)=ACTUAL BYTE ACOUNT
2572 011572 017702 003566 MOV ADHBA,R2 ;(R5)=ACTUAL BUS ADDRESS
2573 011576 027727 003554 000010 CMP ADHSCR,#10 ;IF LINE BEING COMPARED IS LINE 10
2574 011604 001002 BNE 5$
2575 011606 005005 CLR R5 ;EXPECTED BYTE COUNT=0
2576 011610 005203 INC R3 ;EXPECTED BUS ADDRESS = 1
2577 011612 020504 5$: CMP R5,R4 ;IS BYTE COUNT CORRECT
2578 011614 001401 BEQ 6$
2579 011616 104004 HLT 4 ;BYTE COUNT ERROR
2580 011620 020302 6$: CMP R3,R2 ;IS BUS ADDRESS CORRECT
2581 011622 001401 BEQ 7$
2582 011624 104003 HLT 3 ;BUS ADDRESS ERROR
2583 011626 005277 003524 7$: INC ADHSCR ;PREPARE TO CHECK NEXT LINE
2584 011632 005201 INC R1
2585 011634 005300 DEC R0 ;CONTINUE IF ALL NOT DONE
2586 011636 001350 BNE 4$
2587 011640 104400 8$: SCOPE ;CHECK FOR ITERATIONS, LOOP
2588
2589 ;NPR LOGIC TEST
2590 ;SET BYTE COUNT ON ALL LINES TO 1
2591 ;SET BAR BIT FOR LINE 11
2592 ;VERIFY THAT BYTE COUNT FOR LINE 11 GOES TO 0
2593 ;VERIFY THAT BUS ADDRESS FOR LINE 11 IS INCREMENTED
2594 ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2595 ;ARE UNCHANGED
2596
2597 011642 012767 000340 166126 T41: MOV #340,PS ;DISABLE ALL INTERRUPTS
2598 011650 012767 000010 003546 MOV #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2599 011656 012767 012010 003534 MOV #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2600 011664 012777 004000 003464 MOV #BIT11,ADHSCR ;MASTER CLEAR INTERFACE
2601 ;TO SET ALL TBMT BITS
2602 011672 004767 003366 JSR PC,CLEAR ;CLEAR ALL BYTE COUNT AND
2603 ;BUS ADDRESS MEMORY LOCATIONS
2604 011676 004767 003414 JSR PC,LOAD ;SET ALL BYTE COUNT LOCATIONS TO -1
2605 011702 012777 001000 003460 MOV #1000,ADHBAR ;SET BAR BIT FOR LINE 11

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2606	011710	005777	003442		3\$:	TST	ADHSCR		;WAIT FOR TRANSMITTER DONE
2607	011714	100375				BPL	3\$		
2608	011716	012700	000020			MOV	#20,R0		;SET UP TO CHECK ALL 16 LINES
2609	011722	005077	003430			CLR	ADHSCR		;START AT LINE 0
2610	011726	005001				CLR	R1		;KEEP TRACK OF LINE NUMBER
2611	011730	012705	177777		4\$:	MOV	#-1,R5		; (R5)=EXPECTED BYTE COUNT,
2612									; IF LINE NUMBER NOT = 11
2613	011734	005003				CLR	R3		; (R3)=EXPECTED BUS ADDRESS,
2614									; IF LINE NUMBER NOT = 11
2615	011736	017704	003424			MOV	ADHBC,R4		; (R4)=ACTUAL BYTE ACOUNT
2616	011742	017702	003416			MOV	ADHBA,R2		; (R5)=ACTUAL BUS ADDRESS
2617	011746	027727	003404	000011		CMP	ADHSCR,#11		; IF LINE BEING COMPARED IS LINE 11
2618	011754	001002				BNE	5\$		
2619	011756	005005				CLR	R5		; EXPECTED BYTE COUNT=0
2620	011760	005203				INC	R3		; EXPECTED BUS ADDRESS = 1
2621	011762	020504			5\$:	CMP	R5,R4		; IS BYTE COUNT CORRECT
2622	011764	001401				BEQ	6\$		
2623	011766	104004				HLT	4		; BYTE COUNT ERROR
2624	011770	020302			6\$:	CMP	R3,R2		; IS BUS ADDRESS CORRECT
2625	011772	001401				BEQ	7\$		
2626	011774	104003				HLT	3		; BUS ADDRESS ERROR
2627	011776	005277	003354		7\$:	INC	ADHSCR		; PREPARE TO CHECK NEXT LINE
2628	012002	005201				INC	R1		
2629	012004	005300				DEC	R0		; CONTINUE IF ALL NOT DONE
2630	012006	001350				BNE	4\$		
2631	012010	104400			8\$:	SCOPE			; CHECK FOR ITERATIONS, LOOP
2632									
2633									; NPR LOGIC TEST
2634									; SET BYTE COUNT ON ALL LINES TO 1
2635									; SET BAR BIT FOR LINE 12
2636									; VERIFY THAT BYTE COUNT FOR LINE 12 GOES TO 0
2637									; VERIFY THAT BUS ADDRESS FOR LINE 12 IS INCREMENTED
2638									; VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2639									; ARE UNCHANGED
2640									
2641	012012	012767	000340	165756	T42:	MOV	#340,PS		; DISABLE ALL INTERRUPTS
2642	012020	012767	000010	003376		MOV	#10,ICOUNT		; SET UP FOR 10 ITERATIONS
2643	012026	012767	012160	003364		MOV	#8\$,ESCAPE		; SET UP TO ESCAPE TO NEXT TEST
2644	012034	012777	004000	003314		MOV	#BIT11,ADHSCR		; MASTER CLEAR INTERFACE
2645									; TO SET ALL TBMT BITS
2646	012042	004767	003216			JSR	PC,CLEAR		; CLEAR ALL BYTE COUNT AND
2647									; BUS ADDRESS MEMORY LOCATIONS
2648	012046	004767	003244			JSR	PC,LOAD		; SET ALL BYTE COUNT LOCATIONS TO -1
2649	012052	012777	002000	003310		MOV	#2000,ADHBAR		; SET BAR BIT FOR LINE 12
2650	012060	005777	003272		3\$:	TST	ADHSCR		; WAIT FOR TRANSMITTER DONE
2651	012064	100375				BPL	3\$		
2652	012066	012700	000020			MOV	#20,R0		; SET UP TO CHECK ALL 16 LINES
2653	012072	005077	003260			CLR	ADHSCR		; START AT LINE 0
2654	012076	005001				CLR	R1		; KEEP TRACK OF LINE NUMBER
2655	012100	012705	177777		4\$:	MOV	#-1,R5		; (R5)=EXPECTED BYTE COUNT,
2656									; IF LINE NUMBER NOT = 12
2657	012104	005003				CLR	R3		; (R3)=EXPECTED BUS ADDRESS,
2658									; IF LINE NUMBER NOT = 12
2659	012106	017704	003254			MOV	ADHBC,R4		; (R4)=ACTUAL BYTE ACOUNT
2660	012112	017702	003246			MOV	ADHBA,R2		; (R5)=ACTUAL BUS ADDRESS
2661	012116	027727	003234	000012		CMP	ADHSCR,#12		; IF LINE BEING COMPARED IS LINE 12


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718 012326 001350
719 012330 104400
720
721
722
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724
725
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728
729
730 012332 012767 000340 165436 T44: MOV #340,PS ;DISABLE ALL INTERRUPTS
731 012340 012767 000010 003056 MOV #10,COUNT ;SET UP FOR 10 ITERATIONS
732 012346 012767 012500 003044 MOV #88,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
733 012354 012777 004000 002774 MOV #BIT11,JDHSCR ;MASTER CLEAR INTERFACE
734
735 012362 004767 002676 JSR PC,CLEAR ;TO SET ALL TBM BITS
736
737 012366 004767 002724 JSR PC,LOAD ;CLEAR ALL BYTE COUNT AND
738 012372 012777 010000 002770 MOV #10000,JDHBAR ;BUS ADDRESS MEMORY LOCATIONS
739 012400 005777 002752 3$: TST JDHSCR ;SET ALL BYTE COUNT LOCATIONS TO -1
740 012404 100375 BPL 3$ ;SET BAR BIT FOR LINE 14
741 012406 012700 000020 MOV #20,R0 ;WAIT FOR TRANSMITTER DONE
742 012412 005077 002740 CLR JDHSCR ;SET UP TO CHECK ALL 16 LINES
743 012416 005001 CLR R1 ;START AT LINE 0
744 012420 012705 177777 4$: MOV #-1,R5 ;KEEP TRACK OF LINE NUMBER
745
746 012424 005003 CLR R3 ;(R5)=EXPECTED BYTE COUNT,
747
748 012426 017704 002734 MOV JDHBC,R4 ;IF LINE NUMBER NOT = 14
749 012432 017702 002726 MOV JDHBA,R2 ;(R3)=EXPECTED BUS ADDRESS,
750 012436 027727 002714 000014 CMP JDHSCR,#14 ;IF LINE BEING COMPARED IS LINE 14
751
752 012444 001002 BNE 5$ ;(R4)=ACTUAL BYTE ACCOUNT
753 012446 005005 CLR R5 ;(R5)=ACTUAL BUS ADDRESS
754 012450 005203 INC R3 ;EXPECTED BYTE COUNT=0
755 012452 020504 5$: CMP R5,R4 ;EXPECTED BUS ADDRESS = 1
756 012454 001401 BEQ 6$ ;IS BYTE COUNT CORRECT
757 012456 104004 HLT 4 ;BYTE COUNT ERROR
758 012460 020302 6$: CMP R3,R2 ;IS BUS ADDRESS CORRECT
759 012462 001401 BEQ 7$
760 012464 104003 HLT 3 ;BUS ADDRESS ERROR
761 012466 005277 002664 7$: INC JDHSCR ;PREPARE TO CHECK NEXT LINE
762 012472 005201 INC R1
763 012474 005300 DEC R0 ;CONTINUE IF ALL NOT DONE
764 012476 001350 BNE 4$
765 012500 104400 8$: SCOPE ;CHECK FOR ITERATIONS, LOOP
766
767
768
769
770
771
772
773 012502 012767 000340 165266 T45: MOV #340,PS ;DISABLE ALL INTERRUPTS

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:NPR LOGIC TEST
:SET BYTE COUNT ON ALL LINES TO 1
:SET BAR BIT FOR LINE 14
:VERIFY THAT BYTE COUNT FOR LINE 14 GOES TO 0
:VERIFY THAT BUS ADDRESS FOR LINE 14 IS INCREMENTED
:VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
:ARE UNCHANGED

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:DISABLE ALL INTERRUPTS
:SET UP FOR 10 ITERATIONS
:SET UP TO ESCAPE TO NEXT TEST
:MASTER CLEAR INTERFACE
:TO SET ALL TBM BITS
:CLEAR ALL BYTE COUNT AND
:BUS ADDRESS MEMORY LOCATIONS
:SET ALL BYTE COUNT LOCATIONS TO -1
:SET BAR BIT FOR LINE 14
:WAIT FOR TRANSMITTER DONE
:SET UP TO CHECK ALL 16 LINES
:START AT LINE 0
:KEEP TRACK OF LINE NUMBER
:(R5)=EXPECTED BYTE COUNT,
:IF LINE NUMBER NOT = 14
:(R3)=EXPECTED BUS ADDRESS,
:IF LINE NUMBER NOT = 14
:(R4)=ACTUAL BYTE ACCOUNT
:(R5)=ACTUAL BUS ADDRESS
:IF LINE BEING COMPARED IS LINE 14

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:EXPECTED BYTE COUNT=0
:EXPECTED BUS ADDRESS = 1
:IS BYTE COUNT CORRECT
:BYTE COUNT ERROR
:IS BUS ADDRESS CORRECT
:BUS ADDRESS ERROR
:PREPARE TO CHECK NEXT LINE
:CONTINUE IF ALL NOT DONE
:CHECK FOR ITERATIONS, LOOP

```

```

:NPR LOGIC TEST
:SET BYTE COUNT ON ALL LINES TO 1
:SET BAR BIT FOR LINE 15
:VERIFY THAT BYTE COUNT FOR LINE 15 GOES TO 0
:VERIFY THAT BUS ADDRESS FOR LINE 15 IS INCREMENTED
:VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
:ARE UNCHANGED

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2774	012510	012767	000010	002706		MOV	#10,ICOUNT	:SET UP FOR 10 ITERATIONS
2775	012516	012767	012650	002674		MOV	#8\$,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
2776	012524	012777	004000	002624		MOV	#BIT11,JDHSCR	:MASTER CLEAR INTERFACE
2777								:TO SET ALL TBMT BITS
2778	012532	004767	002526			JSR	PC,CLEAR	:CLEAR ALL BYTE COUNT AND
2779								:BUS ADDRESS MEMORY LOCATIONS
2780	012536	004767	002554			JSR	PC,LOAD	:SET ALL BYTE COUNT LOCATIONS TO -1
2781	012542	012777	020000	002620		MOV	#20000,JDHBAR	:SET BAR BIT FOR LINE 15
2782	012550	005777	002602		3\$:	TST	JDHSCR	:WAIT FOR TRANSMITTER DONE
2783	012554	100375				BPL	3\$	
2784	012556	012700	000020			MOV	#20,R0	:SET UP TO CHECK ALL 16 LINES
2785	012562	005077	002570			CLR	JDHSCR	:START AT LINE 0
2786	012566	005001				CLR	R1	:KEEP TRACK OF LINE NUMBER
2787	012570	012705	177777		4\$:	MOV	#-1,R5	:R5=EXPECTED BYTE COUNT,
2788								:IF LINE NUMBER NOT = 15
2789	012574	005003				CLR	R3	:R3=EXPECTED BUS ADDRESS,
2790								:IF LINE NUMBER NOT = 15
2791	012576	017704	002564			MOV	JDHBC,R4	:R4=ACTUAL BYTE ACOUNT
2792	012602	017702	002556			MOV	JDHBA,R2	:R5=ACTUAL BUS ADDRESS
2793	012606	027727	002544	000015		CMP	JDHSCR,#15	:IF LINE BEING COMPARED IS LINE 15
2794	012614	001002				BNE	5\$	
2795	012616	005005				CLR	R5	:EXPECTED BYTE COUNT=0
2796	012620	005203				INC	R3	:EXPECTED BUS ADDRESS = 1
2797	012622	020504			5\$:	CMP	R5,R4	:IS BYTE COUNT CORRECT
2798	012624	001401				BEQ	6\$	
2799	012626	104004				HLT	4	:BYTE COUNT ERROR
2800	012630	020302			6\$:	CMP	R3,R2	:IS BUS ADDRESS CORRECT
2801	012632	001401				BEQ	7\$	
2802	012634	104003				HLT	3	:BUS ADDRESS ERROR
2803	012636	005277	002514		7\$:	INC	JDHSCR	:PREPARE TO CHECK NEXT LINE
2804	012642	005201				INC	R1	
2805	012644	005300				DEC	R0	:CONTINUE IF ALL NOT DONE
2806	012646	001350				BNE	4\$	
2807	012650	104400			8\$:	SCOPE		:CHECK FOR ITERATIONS, LOOP
2808								
2809								
2810								:NPR LOGIC TEST
2811								:SET BYTE COUNT ON ALL LINES TO 1
2812								:SET BAR BIT FOR LINE 16
2813								:VERIFY THAT BYTE COUNT FOR LINE 16 GOES TO 0
2814								:VERIFY THAT BUS ADDRESS FOR LINE 16 IS INCREMENTED
2815								:VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2816								:ARE UNCHANGED
2817	012652	012767	000340	165116	T46:	MOV	#340,PS	:DISABLE ALL INTERRUPTS
2818	012660	012767	000010	002536		MOV	#10,ICOUNT	:SET UP FOR 10 ITERATIONS
2819	012666	012767	013020	002524		MOV	#8\$,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
2820	012674	012777	004000	002454		MOV	#BIT11,JDHSCR	:MASTER CLEAR INTERFACE
2821								:TO SET ALL TBMT BITS
2822	012702	004767	002356			JSR	PC,CLEAR	:CLEAR ALL BYTE COUNT AND
2823								:BUS ADDRESS MEMORY LOCATIONS
2824	012706	004767	002404			JSR	PC,LOAD	:SET ALL BYTE COUNT LOCATIONS TO -1
2825	012712	012777	040000	002450		MOV	#40000,JDHBAR	:SET BAR BIT FOR LINE 16
2826	012720	005777	002432		3\$:	TST	JDHSCR	:WAIT FOR TRANSMITTER DONE
2827	012724	100375				BPL	3\$	
2828	012726	012700	000020			MOV	#20,R0	:SET UP TO CHECK ALL 16 LINES
2829	012732	005077	002420			CLR	JDHSCR	:START AT LINE 0


```

2830 012736 005001          CLR      R1          ;KEEP TRACK OF LINE NUMBER
2831 012740 012705 177777 4$:      MOV      #-1,R5     ;(R5)=EXPECTED BYTE COUNT,
2832                                ;IF LINE NUMBER NOT = 16
2833 012744 005003          CLR      R3          ;(R3)=EXPECTED BUS ADDRESS,
2834                                ;IF LINE NUMBER NOT = 16
2835 012746 017704 002414  MOV      3DHBC,R4     ;(R4)=ACTUAL BYTE ACCOUNT
2836 012752 017702 002406  MOV      3DHBA,R2     ;(R5)=ACTUAL BUS ADDRESS
2837 012756 027727 002374 000016  CMP      3DHSCR,#16   ;IF LINE BEING COMPARED IS LINE 16
2838 012764 001002          BNE      5$
2839 012766 005005          CLR      R5          ;EXPECTED BYTE COUNT=0
2840 012770 005203          INC      R3          ;EXPECTED BUS ADDRESS = 1
2841 012772 020504          CMP      R5,R4       ;IS BYTE COUNT CORRECT
2842 012774 001401          BEQ      6$
2843 012776 104004          HLT      4           ;BYTE COUNT ERROR
2844 013000 020302          CMP      R3,R2       ;IS BUS ADDRESS CORRECT
2845 013002 001401          BEQ      7$
2846 013004 104003          HLT      3           ;BUS ADDRESS ERROR
2847 013006 005277 002344 7$:      INC      3DHSCR      ;PREPARE TO CHECK NEXT LINE
2848 013012 005201          INC      R1
2849 013014 005300          DEC      R0          ;CONTINUE IF ALL NOT DONE
2850 013016 001350          BNE      4$
2851 013020 104400          8$:      SCOPE          ;CHECK FOR ITERATIONS, LOOP

;NPR LOGIC TEST
;SET BYTE COUNT ON ALL LINES TO 1
;SET BAR BIT FOR LINE 17
;VERIFY THAT BYTE COUNT FOR LINE 17 GOES TO 0
;VERIFY THAT BUS ADDRESS FOR LINE 17 IS INCREMENTED
;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
;ARE UNCHANGED

2861 013022 012767 000340 164746 T47:  MOV      #340,PS     ;DISABLE ALL INTERRUPTS
2862 013030 012767 000010 002366  MOV      #10,COUNT   ;SET UP FOR 10 ITERATIONS
2863 013036 012767 013170 002354  MOV      #8$,ESCAPE  ;SET UP TO ESCAPE TO NEXT TEST
2864 013044 012777 004000 002304  MOV      #BIT11,3DHSCR ;MASTER CLEAR INTERFACE
2865                                ;TO SET ALL TBMT BITS
2866 013052 004767 002206          JSR      PC,CLEAR    ;CLEAR ALL BYTE COUNT AND
2867                                ;BUS ADDRESS MEMORY LOCATIONS
2868 013056 004767 002234          JSR      PC,LOAD     ;SET ALL BYTE COUNT LOCATIONS TO -1
2869 013062 012777 100000 002300  MOV      #100000,3DHBAR ;SET BAR BIT FOR LINE 17
2870 013070 005777 002262 3$:      TST      3DHSCR     ;WAIT FOR TRANSMITTER DONE
2871 013074 100375          BPL      3$
2872 013076 012700 000020          MOV      #20,R0     ;SET UP TO CHECK ALL 16 LINES
2873 013102 005077 002250          CLR      3DHSCR     ;START AT LINE 0
2874 013106 005001          CLR      R1          ;KEEP TRACK OF LINE NUMBER
2875 013110 012705 177777 4$:      MOV      #-1,R5     ;(R5)=EXPECTED BYTE COUNT,
2876                                ;IF LINE NUMBER NOT = 17
2877 013114 005003          CLR      R3          ;(R3)=EXPECTED BUS ADDRESS,
2878                                ;IF LINE NUMBER NOT = 17
2879 013116 017704 002244  MOV      3DHBC,R4     ;(R4)=ACTUAL BYTE ACCOUNT
2880 013122 017702 002236  MOV      3DHBA,R2     ;(R5)=ACTUAL BUS ADDRESS
2881 013126 027727 002224 000017  CMP      3DHSCR,#17   ;IF LINE BEING COMPARED IS LINE 17
2882 013134 001002          BNE      5$
2883 013136 005005          CLR      R5          ;EXPECTED BYTE COUNT=0
2884 013140 005203          INC      R3          ;EXPECTED BUS ADDRESS = 1
2885 013142 020504          5$:      CMP      R5,R4       ;IS BYTE COUNT CORRECT

```

00000000	013144	001401
00000000	013146	104004
00000000	013150	020302
00000000	013152	001401
00000000	013154	104003
00000000	013156	005277
00000000	013162	005201
00000000	013164	005300
00000000	013166	001350
00000000	013170	104400

002174

65:	BEQ	65
	HLT	4
	CMP	R3,R2
75:	BEQ	75
	HLT	3
	INC	0DHSCR
	INC	R1
	DEC	R0
	BNE	48
85:	SCOPE	

:BYTE COUNT ERROR
 :IS BUS ADDRESS CORRECT
 :BUS ADDRESS ERROR
 :PREPARE TO CHECK NEXT LINE
 :CONTINUE IF ALL NOT DONE
 :CHECK FOR ITERATIONS, LOOP

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013172	012767	000340	164576	T50:	MOV	#340,PS	:DISABLE ALL INTERRUPTS
013200	012767	000010	002216		MOV	#10,ICOUNT	:SET UP FOR 10 ITERATIONS
013206	012767	013350	002204		MOV	#5\$,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
013214	012777	004000	002134		MOV	#BIT11,JDHSCR	:MASTER CLEAR INTERFACE
013222	012777	013270	002150		MOV	#2\$,JDHARVEC	:SET UP RECEIVER INTERRUPT
013230	012777	000340	002144		MOV	#340,JDHRLVL	:VECTOR AND STATUS
013236	052777	100000	002130		BIS	#BIT15,JDHSSR	:SET SILO MAINTENANCE
013244	012777	000100	002104		MOV	#BIT06,JDHSCR	:SET RECEIVER INTERRUPT ENABLE
013252	005067	164520			CLR	PS	:ALLOW INTERRUPTS
013256	012700	001000			MOV	#1000,R0	:SET UP DELAY FOR SILO LOAD
013262	005300			1\$:	DEC	R0	:DELAY FOR SILO LOAD
013264	001376				BNE	1\$	
013266	104001				HLT	1	:NO CHARACTER AVAILABLE INTERRUPT OCCURED
013270	042777	100000	002076	2\$:	BIC	#BIT15,JDHSSR	:CLEAR SILO MAINTENANCE BIT
013276	105777	002054			TSTB	JDHSCR	:IS CHARACTER AVAILABLE BIT SET
013302	100401				BMI	3\$	
013304	104005				HLT	5	:CHARACTER AVAILABLE NOT, ERROR
013306	017703	002062		3\$:	MOV	JDHSSR,R3	:READ SILO STATUS REGISTER
013312	017704	002042			MOV	JDHNR,R4	:(R4)=ACTUAL DATA IN NEXT
							:RECEIVED CHARACTER REGISTER
013316	012705	125252			MOV	#125252,R5	:(R5)=EXPECTED DATA IN
							:NEXT RECEIVED CHARACTER REGISTER
013322	020504				CMP	R5,R4	:IS DATA IN SILO CORRECT
013324	001401				BEQ	4\$	
013326	104006				HLT	6	:SILO DATA ERROR
013330	010304			4\$:	MOV	R3,R4	:GET SILO STATUS REGISTER
013332	042704	000300			BIC	#300,R4	:CLEAR UNWANTED BITS
013336	012705	000400			MOV	#400,R5	:(R5)=EXPECTED DATA
							:IN SILO STATUS REGISTER
013342	020504				CMP	R5,R4	:CHECK RESULTS
013344	001401				BEQ	5\$	
013346	104007				HLT	7	:SILO STATUS ERROR
013350	012706	017102		5\$:	MOV	#STACK,SP	:RESTORE STACK
013354	104400				SCOPE		:CHECK FOR ITERATIONS, LOOP
							:SILO LOGIC TEST (MAINTENANCE MODE)
							:LOAD 63(DECIMAL) CHARACTERS INTO SILO
							:VERIFY THAT SILO STATUS REGISTER COUNTS UP CORRECTLY
013356	012767	000340	164412	T51:	MOV	#340,PS	:DISABLE ALL INTERRUPTS
013364	012767	000001	002032		MOV	#1,ICOUNT	:SET UP FOR 1 ITERATIONS
013372	012767	013510	002020		MOV	#5\$,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
013400	012767	013412	002014		MOV	#1\$,FREEZ1	:SET UP TO LOOP WITH DATA
013406	012701	000001			MOV	#1,R1	:SET UP TO LOAD SILO WITH 1 CHARACTER

```

2952 013412 012777 004000 001736 1$:  MOV      #BIT11,JDHSCR      ;MASTER CLEAR INTERFACE
2953 013420 010100          MOV      R1,R0             ;SAVE COUNT
2954 013422 005005          CLR      R5                ;WILL BE COUNT OF CHARACTERS LOADED
2955 013424 052777 100000 001742 2$:  BIS      #BIT15,JDHSSR     ;LOAD A CHARACTER
2956 013432 012702 001000          MOV      #1000,R2         ;STALL FOR SILO
2957 013436 005302          DEC      R2                ;
2958 013440 001376          BNE     3$                 ;
2959 013442 042777 100000 001724          BIC      #BIT15,JDHSSR     ;CLEAR LOAD BIT
2960 013450 005205          INC      R5                ;UPDATE COUNT OF CHARACTERS LOADED
2961 013452 005300          DEC      R0                ;IF ALL CHARACTERS NOT LOADED
2962 013454 001363          BNE     2$                 ;LOAD ANOTHER
2963 013456 017704 001712          MOV      JDHSSR,R4         ;READ SILO STATUS REGISTER
2964 013462 042704 000300          BIC      #300,R4           ;CLEAR UNWANTED BITS
2965 013466 000304          SWAB    R4                 ;GET DATA INTO LOW BYTE
2966 013470 020504          CMP     R5,R4              ;COMPARE
2967 013472 001401          BEQ     4$                 ;
2968 013474 104007          HLT     7                   ;SILO STATUS ERROR
2969 013476 104410          SCOPE1 4$:                ;CHECK FOR LOOP WITH CURRENT
2970          ;LOAD COUNT (R5)
2971 013500 005201          INC     R1                  ;ADD 1 TO NUMBER OF CHARACTERS
2972          ;TO BE LOADED INTO SILO
2973 013502 022701 000100          CMP     #100,R1            ;CONTINUE UNTIL SILO IS FULL
2974 013506 001341          BNE     1$                 ;
2975 013510 104400          SCOPE 5$:                 ;
2976          ;SILO LOGIC TEST (MAINTENANCE MODE)
2977          ;LOAD 64 (DECIMAL CHARACTERS INTO SILO)
2978          ;READ CHARACTERS OUT OF SILO
2979          ;VERIFY THAT SILO STATUS REGISTER COUNTS DOWN CORRECTLY
2980
2981
2982 013512 012767 000340 164256 T52:  MOV      #340,PS            ;DISABLE ALL INTERRUPTS
2983 013520 012767 000001 001676          MOV      #1,ICOUNT         ;SET UP FOR 1 ITERATIONS
2984 013526 012767 013670 001664          MOV      #7$,ESCAPE        ;SET UP TO ESCAPE TO NEXT TEST
2985 013534 012767 013546 001660          MOV      #1$,FREEZ1        ;SET UP TO LOOP WITH DATA
2986 013542 012701 000001          MOV      #1,R1             ;SET UP TO READ 1 CHARACTER
2987 013546 012777 004000 001602 1$:  MOV      #BIT11,JDHSCR     ;MASTER CLEAR INTERFACE
2988 013554 012705 000100          MOV      #100,R5           ;SILO STATUS COUNT SHOULD BE
2989 013560 160105          SUB     R1,R5              ;100(OCTAL)-NUMBER
2990          ;OF CHARACTERS READ
2991 013562 012700 000100          MOV      #100,R0           ;SET UP TO LOAD SILO
2992 013566 012702 001000          MOV      #1000,R2          ;SET UP DELAY
2993 013572 052777 100000 001574          BIS      #BIT15,JDHSSR     ;LOAD 1 CHARACTER
2994 013600 005302          DEC     R2                  ;DELAY
2995 013602 001376          BNE     3$                 ;
2996 013604 042777 100000 001562          BIC      #BIT15,JDHSSR     ;CLEAR SILO LOAD BIT
2997 013612 005300          DEC     R0                  ;CONTINUE IF SILO NOT FULL
2998 013614 001364          BNE     2$                 ;
2999 013616 010100          MOV     R1,R0              ;SET UP TO READ SILO
3000 013620 012702 001000          MOV     #1000,R2           ;SET UP DELAY FOR SILO
3001 013624 005777 001530          TST     JDHNR0             ;READ SILO
3002 013630 005302          DEC     R2                  ;DELAY FOR SILO
3003 013632 001376          BNE     5$                 ;
3004 013634 005300          DEC     R0                  ;UPDATE NUMBER OF CHARACTER S TO BE READ
3005 013636 001370          BNE     4$                 ;CONTINUE READING
3006 013640 117704 001532          MOVB   JDHSLR,R4          ;READ SILO STATUS REGISTER
3007 013644 042704 000300          BIC     #300,R4            ;CLEAR UNWANTED BITS

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3008
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3010
3011
3012 013650 020504      CMP      R5,R4
3013 013652 001401      BEQ      6$
3014 013654 104007      HLT      7
3015 013656 104410      6$:     SCOPE1
3016 013660 005201      INC      R1
3017 013662 020127 000101  CMP      R1,#101
3018 013666 001327      BNE      1$
3019 013670 104400      7$:     SCOPE

```

```

:(R5)=EXPECTED SILO STATUS
:(IN UPPER BYTE)
:(R4)=ACTUAL SILO STATUS
:(IN UPPER BYTE)
:COMPARE EXPECTED AND RECEIVED DATA

:SILO STATUS ERROR
:CHECK FOR LOOP WITH SAME READ COUNT
:UPDATE COUNT OF CHARACTERS TO BE READ
;CONTINUE IF NOT DONE

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3020
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3027 013672 012767 000340 164076 T53: MOV #340,PS ;DISABLE ALL INTERRUPTS
3028 013700 012767 000040 001516 MOV #40,ICOUNT ;SET UP FOR 40 ITERATIONS
3029 013706 012767 014046 001504 MOV #5$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
3030 013714 012767 013724 001500 MOV #1$,FREEZ1 ;SET UP TO LOOP WITH DATA
3031 013722 005005 CLR R5 ;START AT ALARM LEVEL 0
3032 013724 012777 004000 001424 1$: MOV #BIT11,ADHSCR ;MASTERCLEAR INTERFACE
3033 013732 010577 001436 MOV R5,ADHSSR ;SET ALARM LEVEL
3034 013736 010501 MOV R5,R1 ;SET FILL COUNT
3035 013740 005201 INC R1 ;ONE MORE THAN ALARM LEVEL
3036 013742 052777 100000 001424 2$: BIS #BIT15,ADHSSR ;LOAD A CHARACTER
3037 013750 012700 001000 MOV #1000,R0 ;WAIT FOR SILO TO SETTLE
3038 013754 005300 DEC R0
3039 013756 001376 BNE .-2
3040 013760 042777 100000 001406 BIC #BIT15,ADHSSR ;CLEAR MAINTENANCE BIT
3041 013766 005301 DEC R1 ;UPDATE FILL COUNT
3042 013770 105777 001362 TSTB ADHSCR ;IS CHARACTER AVAILABLE FLAG SET
3043 013774 100406 BMI 3$ ;YES
3044 013776 005701 TST R1 ;CHARACTER AVAILALBE FLAG NOT SET
3045 014000 001360 BNE 2$ ;SHOULD IT BE
3046 014002 117703 001370 MOVB ADHSLR,R3 ;READ SILO FILL LEVEL
3047 014006 104010 HLT 10 ;SILO ALARM ERROR
3048 ;NO CHARACTER AVAILABLE WHEN EXPECTED
3049 014010 000406 BR 4$
3050 014012 020127 000001 3$: CMP R1,#1
3051 014016 003403 BLE 4$
3052 014020 117703 001352 MOVB ADHSLR,R3 ;READ SILO FILL LEVEL
3053 014024 104010 HLT 10 ;SILO ALARM ERROR
3054 014026 104410 4$: SCOPE1 ;CHECK FOR FREEZE AT CURRENT ALARM LEVEL
3055 014030 005705 TST R5
3056 014032 001001 BNE 10$
3057 014034 000261 SEC
3058 014036 006105 10$: ROL R5 ;GO TO NEXT ALARM LEVEL
3059 014040 022705 000100 CMP #100,R5 ;CONTINUE IF NOT DONE
3060 014044 001327 BNE 1$
3061 014046 104400 5$: SCOPE ;CHECK FOR ITERATIONS, LOOP
  
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3062
3063
3064 ;END OF PASS
3065 ;TYPE NAME OF TEST
3066 ;UPDATE PASS COUNT
3067 ;CHECK FOR EXIT TO ACT-11
3068 ;RESTART TEST
3069
3070 014050 104401 EOP: TYPE ;TYPE NAME OF TEST
3071 014052 016055 MEPASS
3072 014054 005067 001374 CLR LAST ;CLEAR LAST ERROR PC
3073 014060 005067 001324 CLR ERRFLG ;CLEAR ERROR FLAG
3074 014064 005267 001322 INC PASCNT ;UPDATE PASS COUNT
3075 014070 016767 001316 163472 MOV PASCNT,LIGHTS ;DISPLAY PASS COUNT
3076 014076 013701 000042 MOV #42,R1 ;CHECK FOR ACT-11 OR DDP
3077 014102 001405 BEQ RESTRT ;IF NOT, CONTINUE TESTING
3078 014104 000005 RESET
3079 014106 004711 LOGICAL: JSR PC,(R1)
3080 014110 000240 NOP
3081 014112 000240 NOP
3082 014114 000240 NOP
3083 014116 000167 165120 RESTRT: JMP BEGIN
3084
3085 ;CHECK FOR LOOP ON CURRENT TEST
3086 ;CHECK FOR ITERATION SUPPRESSION
3087
3088 014122 032767 002000 163440 SCOPER: BIT #SW10,SWR
3089 014130 001030 BNE 4$
3090 014132 032767 040000 163430 1$: BIT #SW14,SWR
3091 014140 001021 BNE 3$
3092 014142 032767 004000 163420 BIT #SW11,SWR
3093 014150 001006 BNE 2$
3094 014152 005267 001250 INC LPCNT
3095 014156 026767 001244 001240 CMP LPCNT,ICOUNT
3096 014164 001007 BNE 3$
3097 014166 005067 001234 2$: CLR LPCNT
3098 014172 005067 001212 CLR ERRFLG
3099 014176 011667 001214 MOV (SP),RETURN
3100 014202 000002 RTI
3101 014204 016716 001206 3$: MOV RETURN,(SP)
3102 014210 000002 RTI
3103 014212 005767 001172 4$: TST ERRFLG
3104 014216 001745 BEQ 1$
3105 014220 000762 BR 2$
3106
3107 ;CHECK FOR FREEZE ON CURRENT DATA
3108
3109 014222 032767 001000 163340 SCOP1R: BIT #SW09,SWR
3110 014230 001402 BEQ 1$
3111 014232 016716 001164 MOV FREEZ1,(SP)
3112 014236 000002 1$: RTI
3113
3114 ;ERROR HANDLER
3115
3116 014240 032767 020000 163322 ERRORS: BIT #SW13,SWR
3117 014246 001051 BNE HALTS

```

3118	014250	021667	001200		CMP	(SP),LAST	
3119	014254	001404			BEQ	1\$	
3120	014256	011667	001172		MOV	(SP),LAST	
3121	014262	005067	001122		CLR	ERRFLG	
3122	014266	104406		1\$:	SAVOSP		
3123	014270	011605			MOV	(SP),R5	
3124	014272	162705	000002		SUB	#2,R5	
3125	014276	011504			MOV	(R5),R4	
3126	014300	006304			ASL	R4	
3127	014302	006304			ASL	R4	
3128	014304	042704	177001		BIC	#177001,R4	
3129	014310	062704	016164		ADD	#ERRTAB,R4	
3130	014314	012467	000034		MOV	(R4)+,ERRMSG	
3131	014320	011467	000042		MOV	(R4),DATABP	
3132	014324	005767	001060		TST	ERRFLG	
3133	014330	001403			BEQ	TYPMSG	
3134	014332	005767	000030		TST	DATABP	
3135	014336	001007			BNE	TYPDAT	
3136	014340	104402		TYPMSG:	OCTASC		
3137	014342	014434			ERTABO		
3138	014344	012767	000001	001036	MOV	#1,ERRFLG	
3139	014352	104401			TYPE		
3140	014354	000000		ERRMSG:	0		
3141	014356	005767	000004		TYPDAT:	TST	DATABP
3142	014362	001402			BEQ	RESREG	
3143	014364	104402			OCTASC		
3144	014366	000000		DATABP:	0		
3145	014370	104407		RESREG:	RES05		
3146	014372	005767	163172	HALTS:	TST	SWR	
3147	014376	100005			BPL	EXITER	
3148	014400	010046			PUSHRO		
3149	014402	016600	000002		MOV	2(SP),RO	
3150	014406	000000			HALT		
3151	014410	012600			POPPO		
3152	014412	005267	000776	EXITER:	INC	ERPCNT	
3153	014416	032767	002000	163144	BIT	#SW10,SWR	
3154	014424	001402			BEQ	1\$	
3155	014426	016716	000766		MOV	ESCAPE,(SP)	
3156	014432	000002		1\$:	RTI		
3157	014434	000001		ERTABO:	1		
3158	014436	006	002		.BYTE	6,2	
3159	014440	015446			SAVPC		
3160					;TRAP DISPATCH SERVICE		
3161					;ARGUMENT OF TRAP IS EXTRACTED		
3162					;AND USED AS OFFSET TO OBTAIN POINTER		
3163					;TO SELECTED SUBROUTINE		
3164							
3165	014442	011646		TRPSRV:	MOV	(SP),-(SP)	;GET PC OF RETURN
3166	014444	162716	000002		SUB	#2,(SP)	;=PC OF TRAP
3167	014450	017616	000000		MOV	2(SP),(SP)	;GET TRP
3168	014454	006316		TRPOK:	ASL	(SP)	;MULTIPLY TRAP ARG BY 2
3169	014456	042716	177001		BIC	#177001,(SP)	;CLEAR UNWANTED BITS
3170	014462	062716	016104		ADD	#TRPTAB,(SP)	;POINTER TO SUBROUTINE ADDRESS
3171	014466	017616	000000		MOV	2(SP),(SP)	;SUBROUTINE ADDRESS
3172	014472	000136			JMP	2(SP)+	;GO TO SUBROUTINE
3173							


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3174                                     ; TELETYPE OUTPUT ROUTINE
3175
3176 014474 017605 000000          TYPBR:  MOV    @ (SP), R5
3177 014500 062716 000002          ADD    #2, (SP)
3178 014504 105777 000642          1$:    TSTB  @TPCSR
3179 014510 100375                   BPL    1$
3180 014512 105715                   TSTB  (R5)
3181 014514 001001                   BNE   2$
3182 014516 000002                   RTI
3183 014520 112577 000630          2$:    MOVB  (R5)+, @TPDBR
3184 014524 000767                   BR    1$
    
```

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3186                                     ; ASCII STRING INPUT ROUTINE
3187
3188 014526 017667 000000 000006  INSTRG: MOV    @ (SP), MSG
3189 014534 062716 000002          ADD    #2, (SP)
3190 014540 104401          INSTR1: TYPE
3191 014542 000000          MSG:    0
3192 014544 012704 016126          MOV    #INBUF, R4
3193 014550 012703 000007          MOV    #7, R3
3194 014554 105777 000566          1$:    TSTB  @TKCSR
3195 014560 100375                   BPL    1$
3196 014562 117714 000562          MOVB  @TKDBR, (R4)
3197 014566 142714 000200          BICB  #200, (R4)
3198 014572 122427 000015          CMPB  (R4)+, #15
3199 014576 001413          BEQ   INSTR2
3200 014600 117777 000544 000546  MOVB  @TKDBR, @TPDBR
3201 014606 105777 000540          2$:    TSTB  @TPCSR
3202 014612 100375                   BPL    2$
3203 014614 005303                   DEC    R3
3204 014616 001356                   BNE   1$
3205 014620 104401          INSTRE: TYPE
3206 014622 015761          MQM
3207 014624 000745          BR    INSTR1
3208 014626 000002          INSTR2: RTI
    
```

```

3209                                     ; CONVERT ASCII STRING TO OCTAL
3210
3211
3212 014630 011605          PARAMS: MOV    (SP), R5
3213 014632 012567 000146          MOV    (R5)+, LOLIM
3214 014636 012567 000144          MOV    (R5)+, HILIM
3215 014642 012567 000142          MOV    (R5)+, DEVADR
3216 014646 112567 000140          MOVB  (R5)+, LOBITS
3217 014652 112567 000135          MOVB  (R5)+, ADRCNT
3218 014656 010516          MOV    R5, (SP)
3219 014660 005005          PARAM1: CLR    R5
3220 014662 012704 016126          MOV    #INBUF, R4
3221 014666 122714 000015          CMPB  #15, (R4)
3222 014672 001420          BEQ   PARERR
3223 014674 121427 000060          1$:    CMPB  (R4), #60
3224 014700 002415          BLT   PARERR
3225 014702 121427 000067          CMPB  (R4), #67
3226 014706 003012          BGT   PARERR
3227 014710 142714 000060          BICB  #60, (R4)
3228 014714 152405          BISB  (R4)+, R5
3229 014716 122714 000015          CMPB  #15, (R4)
    
```

3230	014722	001406		BEQ	LIMITS
3231	014724	006305		ASL	R5
3232	014726	006305		ASL	R5
3233	014730	006305		ASL	R5
3234	014732	000760		BR	1\$
3235	014734	104404		PARERR: INSTER	
3236	014736	000750		BR	PARAM1
3237					
3238				;TEST TO SEE IF NUMBER IS WITHIN LIMITS	
3239					
3240	014740	020567	000042	LIMITS: CMP	R5, HILIM
3241	014744	101373		BHI	PARERR
3242	014746	020567	000032	CMP	R5, LOLIM
3243	014752	103770		BLO	PARERR
3244	014754	136705	000032	BITB	LOBITS, R5
3245	014760	001365		BNE	PARERR
3246					
3247				;STORE NUMBER AT SPECIFIED ADDRESS	
3248					
3249	014762	016704	000022	1\$: MOV	DEVADR, R4
3250	014766	010524		MOV	R5, (R4)+
3251	014770	062705	000002	ADD	#2, R5
3252	014774	105367	000013	DECB	ADRCNT
3253	015000	001372		BNE	1\$
3254	015002	000002		RTI	
3255	015004	000000		LOLIM: 0	
3256	015006	000000		HILIM: 0	
3257	015010	000000		DEVADR: 0	
3258	015012	000000		LOBITS: 0	
3259		015013		ADRCNT=LOBITS+1	
3260					
3261				;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER	
3262					
3263	015014	104401		OCTASN: TYPE	
3264	015016	015765		MCRLF	
3265	015020	017601	000000	MOV	@(SP), R1
3266	015024	062716	000002	ADD	#2, (SP)
3267	015030	012167	000130	MOV	(R1)+, WRDCNT
3268	015034	112167	000126	1\$: MOV	(R1)+, CHRCNT
3269	015040	112167	000123	MOV	(R1)+, SPACNT
3270	015044	013167	000120	MOV	@(R1)+, BINWRD
3271	015050	016704	000114	2\$: MOV	BINWRD, R4
3272	015054	116705	000106	MOV	CHRCNT, R5
3273	015060	012700	016140	MOV	#TEMP, R0
3274	015064	010403		3\$: MOV	R4, R3
3275	015066	042703	177770	BIC	#177770, R3
3276	015072	062703	000260	ADD	#260, R3
3277	015076	110320		MOV	R3, (R0)+
3278	015100	006204		ASR	R4
3279	015102	006204		ASR	R4
3280	015104	006204		ASR	R4
3281	015106	005305		DEC	R5
3282	015110	001365		BNE	3\$
3283	015112	012703	016152	4\$: MOV	#MDATA, R3
3284	015116	114023		MOV	-(R0), (R3)+
3285	015120	105367	000042	DECB	CHRCNT

015334 005277 000016
015340 005300
015342 001371
015344 000207

INC 3DHSCR
DEC RO
BNE R3
RTS PC
: INDIRECT POINTERS

: ADVANCE LINE NUMBER
: CONTINUE IF NOT DONE
: RETURN TO CALLING ROUTINE

015346 177560
015350 177562
015352 177564
015354 177566
015356 000000
015358 000000
015360 000000
015362 000000
015364 000000
015366 000000
015368 000000
015370 000000
015372 000000
015374 000000
015376 000000
015378 000000
015380 000000
015382 000000
015384 000000
015386 000000
015388 000000
015390 000000
015392 000000
015394 000000
015396 000000
015398 000000
015400 000000
015402 000000
015404 000000
015406 000000

TKCSR: 177560
TKOBR: 177562
TPCSR: 177564
TPOBR: 177566
DHSCR: 0
DHNRC: 0
DHLPR: 0
DHBA: 0
DHBC: 0
DHBAR: 0
DHBCR: 0
DHSSR: 0
DHSLR: 0
DHAVEC: 0
DHLVL: 0
DHTVEC: 0
DHTLVL: 0

: PROGRAM VARIABLES

015410 000000
015412 000000
015414 000000
015416 000000
015420 000000
015422 000000
015424 000000
015426 000000
015430 000000
015432 000000
015434 000000
015436 000000
015438 000000
015440 000000
015442 000000
015444 000000
015446 000000
015448 000000
015450 000000
015452 000000
015454 000000
015456 000000
015458 000000
015460 000000

ERRFLG: 0 : ERROR FLAG
PASCNT: 0 : PASS COUNT
ERRCNT: 0 : ERROR COUNT
RETURN: 0 : SCOPE RETURN ADDRESS FOR TEST LOOPING
ESCAPE: 0 : ADDRESS FOR ERROR ESCAPE
FREEZ1: 0 : DATA LOOPING RETURN ADDRESS
ICOUNT: 0 : ITERATION COUNT FOR TEST IN PROGRESS
LPCNT: 0 : NUMBER OF ITERATIONS THIS TEST
SAVR0: 0 : R0 SAVE AREA
SAVR1: 0 : R1 SAVE AREA
SAVR2: 0 : R2 SAVE AREA
SAVR3: 0 : R3 SAVE AREA
SAVR4: 0 : R4 SAVE AREA
SAVR5: 0 : R5 SAVE AREA
SAVSP: 0 : STACK POINTER SAVE AREA
SAVPC: 0 : CALLING ROUTINE SAVE AREA
INIFLG: 0 : PROGRAM INITIALIZATION FLAG
STFLG: 0 : PROGRAM START FLAG
LAST: 0 : LAST ERROR PC
HCORE: 0

: ENTER HERE ON POWER FAILURE

015462 010046
015464 010146
015466 010246
015468 010346
015470 010446
015472 010546
015474 016746
015476 162324
015478 177740
015480 010667

PFAIL: MOV R0, -(SP) : SAVE R0-R5 ON PROCESSOR STACK
MOV R1, -(SP)
MOV R2, -(SP)
MOV R3, -(SP)
MOV R4, -(SP)
MOV R5, -(SP)
MOV R6, -(SP)
MOV R7, -(SP)
MOV R8, -(SP)
MOV R9, -(SP)
MOV R10, -(SP)
MOV R11, -(SP)
MOV R12, -(SP)
MOV R13, -(SP)
MOV R14, -(SP)
MOV R15, -(SP)
MOV SP, SAVSP : SAVE STACK POINTER

```

0398 015504 012767 015516 162312      MOV      #RESTART,24      ;SET UP FOR POWER UP TRAP
0399 015512 000000      HALT                               ;HALT ON POWER DOWN NORMAL
0400 015514 000777      BR                               .
                                ;PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED.
0401 015516 016706 177722      RESTAR: MOV      SAVSP,SP      ;RESTORE STACK POINTER
0402 015522 012605      MOV      (SP)+,R5          ;RESTORE R0-R5
0403 015524 012604      MOV      (SP)+,R4
0404 015526 012603      MOV      (SP)+,R3
0405 015530 012602      MOV      (SP)+,R2
0406 015532 012601      MOV      (SP)+,R1
0407 015534 012600      MOV      (SP)+,R0
0408 015536 012767 015460 162260      MOV      #PFAIL,24      ;SET UP FOR POWER FAILURE
0409 015544 012767 000340 162224      MOV      #340,PS
0410 015552 012706 017102      MOV      #STACK,SP
0411 015556 005067 000356      CLR      TEMP
0412 015562 005267 000352      INC      TEMP
0413 015566 001375      BNE      .-4
0414 015570 104402      OCTASC
0415 015572 015614      PFTAB
0416 015574 104401      TYPE
0417 015576 015770      MPFAIL
0418 015600 005067 177604      CLR      ERRFLG
0419 015604 005067 177644      CLR      LAST
0420 015610 000177 177602      JMP      @RETURN
0421 015614 000001      PFTAB: 1
0422 015616 000006 000002      6,2
0423 015622 000207      RETURN
0424 015624 005015 042012 030510      MTITLE: .ASCIZ  <15><12><12>/DH11 TRANSMITTER AND RECEIVER LOGIC TEST <15><12>
0425 015632 020061 051124 047101
0426 015640 046523 052111 042524
0427 015646 020122 047101 020104
0428 015654 042522 042503 053111
0429 015662 051105 046040 043517
0430 015670 041511 052040 051505
0431 015676 020124 005015 000
0432 015703 015 053012 041505      MVECT0: .ASCIZ  <15><12>/VECTOR ADDRESS-/
0433 015710 047524 020122 042101
0434 015716 051104 051505 026523
0435 015724 000
0436 015725 015 041412 047117      MREGAD: .ASCIZ  <15><12>/CONTROL REGISTER ADDRESS-/
0437 015732 051124 046117 051040
0438 015740 043505 051511 042524
0439 015746 020122 042101 051104
0440 015754 051505 026523 000
0441 015761 040 037440 000
0442 015765 015 000012
0443 015770 020040 047520 042527      MQM: .ASCIZ  / ?/
0444 015776 020122 040506 046111      MCRLF: .ASCIZ  <15><12>
0445 016004 051125 026105 050040      MPFAIL: .ASCIZ  / POWER FAILURE, PROGRAM RESTART AT TEST IN PROGRESS/
0446 016012 047522 051107 046501
0447 016020 051040 051505 040524
0448 016026 052122 040440 020124
0449 016034 042524 052123 044440
0450 016042 020116 051120 043517

```

016050	042522	051523	000
016055	015	042012	042132
016062	041510	000	
016071	015	051012	000
016076	020124	052012	051505
		041520	000055

```

MEPASS: .ASCIZ <15><12>/DZDHC/
MR: .ASCIZ <15><12>/R/
MTSTPC: .ASCIZ <15><12>/TEST PC-/

```

;TABLE OF POINTERS FOR TRAP DECODING

016104	014122
016106	014474
016110	015014
016112	014526
016114	014620
016116	014630
016120	015172
016122	015232
016124	014222

```

TRPTAB: SCOPER
        TYPER
        OCTASN
        INSTRG
        INSTRE
        PARAMS
        SVOSP
        RSOS
        SCOP1R

```

;BUFFERS FOR INPUT-OUTPUT

016126	000000
	016140
016140	000000
	016152
016152	000000
	016164

```

INBUF: 0
        =.+10
TEMP: 0
        =.+10
MDATA: 0
        =.+10

```

;TABLE OF POINTERS TO ERROR MESSAGES AND DATA

016164			
016164	016230		
016166	016656		
016170	016310		
016172	000000		
016174	016325		
016176	000000		
016200	016356		
016202	016656		
016204	016415		
016206	016656		
016210	016453		
016212	000000		
016214	016507		
016216	016656		
016220	016544		
016222	016656		
016224	016603		
016226	016670		
016230	047125	054105	042520
016236	052103	042105	044440
016244	052116	051105	052522
016252	052120		
016254	005015	047503	052116
016262	047522	020114	042522
016270	044507	052123	051105

```

ERRTAB: EMO
        DT1
        EM1
        0
        EM2
        0
        EM3
        DT1
        EM4
        DT1
        EM5
        0
        EM6
        DT1
        EM7
        DT1
        EM10
        DT2
EMO: .ASCII /UNEXPECTED INTERRUPT/

.ASCIZ <15><12>/CONTROL REGISTER CONTENTS/

```

3510	016276	041440	047117	042524		
3511	016304	052116	000123			
3512	016310	047516	044440	052116	EM1:	.ASCIZ /NO INTERRUPT/
3513	016316	051105	052522	052120		
3514	016324	000				
3515	016325	124	040522	051516	EM2:	.ASCIZ /TRANSMITTER DONE NOT SET/
3516	016332	044515	052124	051105		
3517	016340	042040	047117	020105		
3518	016346	047516	020124	042523		
3519	016354	000124				
3520	016356	052502	020123	042101	EM3:	.ASCII /BUS ADDRESS ERROR/
3521	016364	051104	051505	020123		
3522	016372	051105	047522	122		
3523	016377	015	042412	050130		.ASCIZ <15><12>/EXP REC/
3524	016404	020040	020040	051040		
3525	016412	041505	000			
3526	016415	102	052131	020105	EM4:	.ASCII /BYTE COUNT ERROR/
3527	016422	047503	047125	020124		
3528	016430	051105	047522	122		
3529	016435	015	042412	050130		.ASCIZ <15><12>/EXP REC/
3530	016442	020040	020040	051040		
3531	016450	041505	000			
3532	016453	103	040510	040522	EM5:	.ASCIZ /CHARACTER AVAILABLE NOT SET/
3533	016460	052103	051105	040440		
3534	016466	040526	046111	041101		
3535	016474	042514	047040	052117		
3536	016502	051440	052105	000		
3537	016507	123	046111	020117	EM6:	.ASCII /SILO DATA ERROR/
3538	016514	040504	040524	042440		
3539	016522	051122	051117			
3540	016526	005015	054105	020120		.ASCIZ <15><12>/EXP REC/
3541	016534	020040	020040	042522		
3542	016542	000103				
3543	016544	044523	047514	051440	EM7:	.ASCII /SILO STATUS ERROR/
3544	016552	040524	052524	020123		
3545	016560	051105	047522	122		
3546	016565	015	042412	050130		.ASCIZ <15><12>/EXP REC/
3547	016572	020040	020040	051040		
3548	016600	041505	000			
3549	016603	123	046111	020117	EM10:	.ASCII /SILO ALARM ERROR/
3550	016610	046101	051101	020115		
3551	016616	051105	047522	122		
3552	016623	015	040412	040514		.ASCIZ <15><12>/ALARM LEVEL FILL LEVEL/
3553	016630	046522	046040	053105		
3554	016636	046105	020040	044506		
3555	016644	046114	046040	053105		
3556	016652	046105	000			
3557		016656				.EVEN
3558						
3559						;DATA TABLES FOR ERROR OUTPUT
3560						
3561	016656	000002			DT1:	2
3562	016660	006	002		.BYTE	6,2
3563	016662	015442				SAVR5
3564	016664	006	000		.BYTE	6,0
3565	016666	015440				SAVR4

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DZDHC.B.PFC

3566	016670	000002		DT2:	2
3567	016672	002	014	.BYTE	14
3568	016674	015442			SAVR5
3569	016676	002	000	.BYTE	0
3570	016700	015436			SAVR3
3571	016702	000000		ENDCOD: 0	
3572		000001		.END	

ADRCNT = 015013	3217*	3252*	3259#											
BEGIN 001242	528	957	963#	3083										
SINWRD 015170	3270*	3271	3301#											
BITX = 000001	1232#	1292#	1352#	1412#	1472#	1532#	1592#	1652#	1712#	1772#	1832#	1892#	1952#	
	2012#	2072#	2132#	2192#	2236#	2280#	2324#	2368#	2412#	2456#	2500#	2544#	2588#	
	2632#	2676#	2720#	2764#	2808#	2852#	2896#							
BIT00 = 000001	604#													
BIT01 = 000002	603#													
BIT02 = 000004	602#													
BIT03 = 000010	601#													
BIT04 = 000020	600#													
BIT05 = 000040	599#													
BIT06 = 000100	598#	997	1099	2915										
BIT07 = 000200	597#	1101												
BIT08 = 000400	596#													
BIT09 = 001000	595#	1098	1135	1172	1209									
BIT10 = 002000	594#	1175												
BIT11 = 004000	593#	990	1024	1058	1093	1130	1167	1204	1243	1303	1363	1423	1483	
	1543	1603	1663	1723	1783	1843	1903	1963	2023	2093	2143	2204	2248	
	2292	2336	2380	2424	2468	2512	2556	2600	2644	2688	2732	2776	2820	
	2864	2911	2952	2987	3032									
BIT12 = 010000	592#	1031	1138											
BIT13 = 020000	591#	1065	1173	1210	1253	1313	1373	1433	1493	1553	1613	1673	1733	
	1793	1853	1913	1973	2033	2093	2153							
BIT14 = 040000	590#	1136												
BIT15 = 100000	589#	1212	2914	2921	2955	2959	2993	2996	3036	3040				
CHRCNT 015166	3268*	3272	3285*	3299#	3300									
CLEAR 015264	1244	1304	1364	1424	1484	1544	1604	1664	1724	1784	1844	1904	1964	
	2024	2084	2144	2206	2250	2294	2338	2382	2426	2470	2514	2558	2602	
	2646	2690	2734	2778	2822	2866	3328#							
DATABP 014366	3131*	3134	3141	3144#										
DEVADR 015010	3215*	3249	3257#											
DHBA 015364	1269	1271	1329	1331	1389	1391	1449	1451	1509	1511	1569	1571	1629	
	1631	1689	1691	1749	1751	1809	1811	1869	1871	1929	1931	1989	1991	
	2049	2051	2109	2111	2169	2171	2220	2264	2308	2352	2396	2440	2484	
	2528	2572	2616	2660	2704	2748	2792	2836	2880	3331*	3355#			
DHBA 015370	1251*	1262	1266	1311*	1322	1326	1371*	1382	1396	1431*	1442	1446	1491*	
	1502	1506	1551*	1562	1566	1611*	1622	1626	1671*	1682	1686	1731*	1742	
	1746	1791*	1802	1806	1851*	1862	1866	1911*	1922	1926	1971*	1982	1986	
	2031*	2042	2046	2091*	2102	2106	2151*	2162	2166	2209*	2253*	2297*	2341*	
	2385*	2429*	2473*	2517*	2561*	2605*	2649*	2693*	2737*	2781*	2825*	2869*	3357#	
DHBC 015366	1249*	1279	1281	1309*	1339	1341	1369*	1399	1401	1429*	1459	1461	1489*	
	1519	1521	1549*	1579	1581	1609*	1639	1641	1669*	1699	1701	1729*	1759	
	1761	1789*	1819	1821	1849*	1879	1881	1909*	1939	1941	1969*	1999	2001	
	2029*	2059	2061	2089*	2119	2121	2149*	2179	2181	2219	2263	2307	2351	
	2395	2439	2483	2527	2571	2615	2659	2703	2747	2791	2835	2879	3330*	
	3341*	3356#												
DHBCR 015372	3358#													
DHLPR 015362	3354#													
DHNRC 015360	2926	3001	3353#											
DHRLVL 015402	993*	1011	1012*	1027*	1045	1046*	1061*	1079	1080*	1095*	1116	1117*	1132*	
	1153	1154*	1169*	1190	1191*	1206*	1227	1228*	1286	1287*	1346	1347*	1406	
	1407*	1466	1467*	1526	1527*	1586	1587*	1646	1647*	1706	1707*	1766	1767*	
	1826	1827*	1886	1887*	1946	1947*	2006	2007*	2066	2067*	2126	2127*	2186	
	2187*	2913*	3362#											
DHRVEC 015400	943	991*	1011*	1025*	1045*	1059*	1079*	1094*	1116*	1131*	1153*	1169*	1190*	

HILIM	015006	3214*	3240	3256#										
ICOUNT	015424	988*	1022*	1056*	1091*	1128*	1165*	1202*	1241*	1301*	1361*	1421*	1481*	1541*
		1601*	1661*	1721*	1781*	1841*	1901*	1961*	2021*	2081*	2141*	2202*	2246*	2290*
		2334*	2378*	2422*	2466*	2510*	2554*	2598*	2642*	2686*	2730*	2774*	2818*	2862*
		2909*	2948*	2993*	3028*	3095	3373#							
INBUF	016126	3192	3220	3475#										
INIFLG	015450	914	925	956	958*	3383#								
INSTER=	104404	886#	3235											
INSTR =	104403	885#	938	946	967									
INSTRE	014620	3205#	3467											
INSTRG	014526	3188#	3466											
INSTR1	014540	3190#	3207											
INSTR2	014626	3199	3208#											
LAST	015454	3072*	3118	3120*	3385#	3422*								
LIGHTS=	177570	574#	3075*											
LIMITS	014740	3230	3240#											
LINE =	000000	1232#	1292#	1352#	1412#	1472#	1532#	1592#	1652#	1712#	1772#	1832#	1892#	1952#
		2012#	2072#	2132#	2192#	2236#	2280#	2324#	2368#	2412#	2456#	2500#	2544#	2588#
		2632#	2676#	2720#	2764#	2808#	2852#	2896#						
LOAD	015316	2208	2252	2296	2340	2384	2428	2472	2516	2560	2604	2648	2692	2736
		2780	2824	2868	3339#									
LOBITS	015012	3216*	3244	3258#	3259									
LOGICA	014106	892	3079#											
LOLIM	015004	3213*	3242	3255#										
LPCNT	015426	3094*	3095	3097*	3374#									
MCRLF	015765	3264	3445#											
MDATA	016152	3283	3294	3479#										
MEPASS	016055	3071	3455#											
MPFAIL	015770	3420	3446#											
MQM	015761	3206	3444#											
MR	016065	980	3457#											
MREGAD	015725	947	3439#											
MSG	014542	3188*	3191#											
MTITLE	015624	913	3427#											
MTSTPC	016071	968	3458#											
MVECTO	015703	939	3435#											
N =	000001	1#												
OCTASC=	104402	884#	3136	3143	3417									
OCTASN	015014	3263#	3465											
PARAM =	104405	887#	940	948	969									
PARAMS	014630	3212#	3468											
PARAM1	014660	3219#	3236											
PAPERR	014734	3222	3224	3226	3235#	3241	3243	3245						
PASCNT	015412	909*	3074*	3075	3368#									
PC =	%000007	569#	1244*	1304*	1364*	1424*	1484*	1544*	1604*	1664*	1724*	1784*	1844*	1904*
		1964*	2024*	2084*	2144*	2206*	2208*	2250*	2252*	2294*	2296*	2338*	2340*	2382*
		2384*	2426*	2428*	2470*	2472*	2514*	2516*	2558*	2560*	2602*	2604*	2646*	2648*
		2690*	2692*	2734*	2736*	2778*	2780*	2822*	2824*	2866*	2868*	3079*	3335*	3345*
PFail	015460	867	907	3390#	3411									
PFTAB	015614	3418	3424#											
POPPO =	012600	583#	3151											
POP1SP=	005726	581#												
POP2SP=	022626	585#												
PS =	177776	575#	905*	963*	987*	999*	1001*	1021*	1033*	1035*	1055*	1067*	1069*	1090*
		1103*	1105*	1127*	1140*	1142*	1164*	1177*	1179*	1201*	1214*	1216*	1240*	1254*
		1300*	1314*	1360*	1374*	1420*	1434*	1480*	1494*	1540*	1554*	1600*	1614*	1660*

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 DZDHC.B.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

		1674*	1720*	1734*	1780*	1794*	1840*	1854*	1900*	1914*	1960*	1974*	2020*	2034*
		2080*	2094*	2140*	2154*	2201*	2245*	2289*	2333*	2377*	2421*	2465*	2509*	2553*
		2597*	2641*	2685*	2729*	2773*	2817*	2861*	2908*	2916*	2947*	2982*	3027*	3412*
PUSHRO=	010046	582#	3148											
PUSH1S=	005746	580#												
PUSH2S=	024646	584#												
RESREG	014370	3142	3145#											
RESTAR	015516	3398	3404#											
RESTRY	014116	3077	3083#											
RESOS =	104407	889#	3145											
RETURN	015416	976*	981	3099*	3101	3370#	3423							
RSCS	015232	3318#	3470											
RO	=%000000	562#	917*	919	921	1250*	1255*	1310*	1315*	1370*	1375*	1430*	1435*	1490*
		1495*	1550*	1555*	1610*	1615*	1670*	1675*	1730*	1735*	1790*	1795*	1850*	1855*
		1910*	1915*	1970*	1975*	2030*	2035*	2090*	2095*	2150*	2155*	2212*	2233*	2256*
		2277*	2300*	2321*	2344*	2365*	2388*	2409*	2432*	2453*	2476*	2497*	2520*	2541*
		2564*	2585*	2608*	2629*	2652*	2673*	2696*	2717*	2740*	2761*	2784*	2805*	2828*
		2849*	2872*	2893*	2917*	2918*	2953*	2961*	2991*	2997*	2999*	3004*	3037*	3038*
R1	=%000001	3149*	3273*	3277*	3284	3314	3318*	3328*	3333*	3339*	3343*	3390	3410*	3038*
		563#	929*	932*	934*	936	2214*	2232*	2258*	2276*	2302*	2320*	2346*	2364*
		2390*	2408*	2434*	2452*	2478*	2496*	2522*	2540*	2566*	2584*	2610*	2628*	2654*
		2672*	2698*	2716*	2742*	2760*	2786*	2804*	2830*	2848*	2874*	2892*	2951*	2953
		2971*	2973	2986*	2989	2999	3016*	3017	3034*	3035*	3041*	3044	3050	3076*
R2	=%000002	3079	3265*	3267	3268	3269	3270	3313	3319*	3391	3409*			
		564#	930*	932	933*	935*	2220*	2228	2264*	2272	2308*	2316	2352*	2360
		2396*	2404	2440*	2448	2484*	2492	2528*	2536	2572*	2580	2616*	2624	2660*
		2668	2704*	2712	2748*	2756	2792*	2800	2836*	2844	2880*	2888	2956*	2957*
		2992*	2994*	3000*	3002*	3312	3320*	3392	3408*					
R3	=%000003	565#	931*	934	935	2217*	2224*	2228	2261*	2268*	2272	2305*	2312*	2316
		2349*	2356*	2360	2393*	2400*	2404	2437*	2444*	2448	2481*	2488*	2492	2525*
		2532*	2536	2569*	2576*	2580	2613*	2620*	2624	2657*	2664*	2668	2701*	2708*
		2712	2745*	2752*	2756	2789*	2796*	2800	2833*	2840*	2844	2877*	2884*	2888
		2925*	2933	3046*	3052*	3193*	3203*	3274*	3275*	3276*	3277	3283*	3284*	3289*
		3292*	3311	3321*	3393	3407*								
R4	=%000004	566#	1266*	1271*	1281*	1326*	1331*	1341*	1386*	1391*	1401*	1446*	1451*	1461*
		1506*	1511*	1521*	1566*	1571*	1581*	1626*	1631*	1641*	1686*	1691*	1701*	1746*
		1751*	1761*	1806*	1811*	1821*	1866*	1871*	1881*	1926*	1931*	1941*	1986*	1991*
		2001*	2046*	2051*	2061*	2106*	2111*	2121*	2166*	2171*	2181*	2219*	2225	2263*
		2269	2307*	2313	2351*	2357	2395*	2401	2439*	2445	2483*	2489	2527*	2533
		2571*	2577	2615*	2621	2659*	2665	2703*	2709	2747*	2753	2791*	2797	2835*
		2841	2879*	2885	2926*	2930	2933*	2934*	2937	2963*	2964*	2965*	2966	3006*
		3007*	3012	3125*	3126*	3127*	3128*	3129*	3130	3131	3192*	3196*	3197*	3199
		3220*	3221	3223	3225	3227*	3228	3229	3249*	3250*	3271*	3274	3278*	3279*
		3280*	3310	3322*	3394	3406*								
R5	=%000005	567#	1003*	1007*	1037*	1041*	1071*	1075*	1112*	1149*	1186*	1223*	1264*	1274*
		1283*	1324*	1334*	1343*	1384*	1394*	1402*	1444*	1454*	1463*	1504*	1514*	1523*
		1564*	1574*	1583*	1624*	1634*	1643*	1684*	1694*	1703*	1744*	1754*	1763*	1804*
		1814*	1823*	1864*	1874*	1883*	1924*	1934*	1943*	1984*	1994*	2003*	2044*	2054*
		2063*	2104*	2114*	2123*	2164*	2174*	2183*	2215*	2223*	2225	2259*	2267*	2269
		2303*	2311*	2313	2347*	2355*	2357	2391*	2399*	2401	2435*	2443*	2445	2479*
		2487*	2489	2523*	2531*	2533	2567*	2575*	2577	2611*	2619*	2621	2655*	2663*
		2665	2699*	2707*	2709	2743*	2751*	2753	2787*	2795*	2797	2831*	2839*	2841
		2875*	2883*	2885	2928*	2930	2935*	2937	2954*	2960*	2966	2998*	2989*	3012
		3031*	3033	3034	3055	3058*	3059	3123*	3124*	3125	3176*	3180	3183	3212*
		3213	3214	3215	3216	3217	3218	3219*	3228*	3231*	3232*	3233*	3240	3242
		3244	3250	3251*	3272*	3281*	3309	3323*	3395	3405*				

TYPER	014474	3176#	3464											
TYPMSG	014340	3133	3136#											
T1	001334	976	987#											
T10	003032	1240#												
T11	003270	1300#												
T12	003526	1360#												
T13	003764	1420#												
T14	004222	1480#												
T15	004460	1540#												
T16	004716	1600#												
T17	005154	1660#												
T2	001516	1021#												
T20	005412	1720#												
T21	005650	1780#												
T22	006106	1840#												
T23	006344	1900#												
T24	006602	1960#												
T25	007040	2020#												
T26	007276	2080#												
T27	007534	2140#												
T3	001700	1055#												
T30	007772	2201#												
T31	010142	2245#												
T32	010312	2289#												
T33	010462	2333#												
T34	010632	2377#												
T35	011002	2421#												
T36	011152	2465#												
T37	011322	2509#												
T4	002062	1090#												
T40	011472	2553#												
T41	011642	2597#												
T42	012012	2641#												
T43	012162	2685#												
T44	012332	2729#												
T45	012502	2773#												
T46	012652	2817#												
T47	013022	2861#												
T5	002254	1127#												
T50	013172	2908#												
T51	013356	2947#												
T52	013512	2982#												
T53	013672	3027#												
T6	002446	1164#												
T7	002640	1201#												
VEC1	001120	915	927#											
VEC2	001130	926	929#											
WRDCNT	015164	3267*	3295*	3298#										
X =	000000	1#												
XBIT =	000001	1232#	2192#	2896#										
XLIN =	000000	1232#	2192#	2896#										
XN =	000054	1#	987	990#	1021	1024#	1055	1058#	1090	1093#	1127	1130#	1164	1167#
		1201	1204#	1240	1243#	1300	1303#	1360	1363#	1420	1423#	1480	1483#	1540
		1543#	1600	1603#	1660	1663#	1720	1723#	1780	1783#	1840	1843#	1900	1903#
		1960	1963#	2020	2023#	2080	2083#	2140	2143#	2201	2204#	2245	2248#	2299
		2292#	2333	2336#	2377	2380#	2421	2424#	2465	2468#	2509	2512#	2553	2556#

		2597	2600#	2641	2644#	2685	2688#	2729	2732#	2773	2776#	2817	2820#	2861
Y	= 000011	2864#	2908	2911#	2947	2951#	2982	2986#	3027	3031#				
.	= 016704	1#	882	883#	884#	885#	886#	887#	888#	889#	890#	891#		
		606#	607	609	611	613	615	617	619	621	623	625	627	629
		631	633	635	637	639	641	643	645	647	649	651	653	655
		657	659	661	663	665	667	669	671	673	675	677	679	681
		683	685	687	689	691	693	695	697	699	701	703	705	707
		709	711	713	715	717	719	721	723	725	727	729	731	733
		735	737	739	741	743	745	747	749	751	753	755	757	759
		761	763	765	767	769	771	773	775	777	779	781	783	785
		787	789	791	793	795	797	799	801	803	805	807	809	811
		813	815	817	819	821	823	825	827	829	831	833	835	837
		839	841	843	845	847	849	851	853	855	857	859	861	863
		873#	891#	893#	895#	3039	3400	3416	3476#	3478#	3480#	3557#		866#

	2640	2641	2642	2643	2644	2649	2652	2655	2659	2660	2685	2686
MOV8	3046	3052	3183	3196	3200	3217	3269	3269	3272	3284	3289	3408
NOP	1034	1068	1104	1141	1178	1215	3080	3081	3082			
RETURN	3426											
ROL												
RTI	1010	1040	1044	1074	1078	1111	1115	1148	1152	1185	1189	3100
RTS	3312	3156	3182	3208	3254	3297	3315	3324				
LIB	3345											
LIB	2989	3124	3166									
ST	882	884	885	886	887	888	889	890				
TEST	1491	1492	1502	1519	1558	1562	1579	1618	1322	1339	1378	1438
TEST	1798	1798	1802	1819	1858	1862	1879	1918	1622	1639	1678	1738
TEST	2098	2098	2102	2119	2158	2162	2179	2218	1922	1939	1978	2038
TEST	2606	2606	2650	2694	2738	2782	2826	2870	2254	2299	2343	2403
TEST	3014	3178	3180	3194	3201	3287			3001	3044	3055	3103
TEST	3436	3526	3537	3543	3549				3044	3044	3055	3103
TEST	3446	3439	3444	3445	3446	3455	3457	3458	3507	3512	3515	3523
TEST	945	952	953	973	974	3158	3562	3564	3567	3569		
TEST												
TEST	924	927	954	956	990	1024	1058	1093	1130	1167	1204	1243
TEST	1483	1543	1603	1663	1723	1783	1843	1903	1963	2023	2083	2143
TEST	2336	2380	2424	2468	2512	2556	2600	2644	2688	2732	2776	2820
TEST	2986	3031										
TEST												
TEST	915	917	924	954	990	1024	1058	1093	1130	1167	1204	1243
TEST	1483	1543	1603	1663	1723	1783	1843	1903	1963	2023	2083	2143
TEST	2336	2380	2424	2468	2512	2556	2600	2644	2688	2732	2776	2820
TEST	2986	3031										
TEST												
TEST	917	924										
TEST	903	904										
TEST	3386											
TEST												
TEST	520	539	883	884	885	886	887	888	889	890	891	982
TEST	1093	1130	1167	1204	1232	1243	1292	1303	1352	1363	1412	1472
TEST	1592	1592	1603	1652	1663	1712	1723	1772	1783	1832	1843	1892
TEST	2012	2023	2072	2083	2132	2143	2192	2204	2236	2248	2290	2340
TEST	2380	2412	2424	2456	2468	2500	2512	2544	2556	2588	2600	2640
TEST	2720	2732	2764	2776	2808	2820	2852	2864	2896	2911	2951	3031

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 DZDHC.B.PFC CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

MACRO	1	895	982											
.NLIST	105	1093	1130	1167	1204	1232	1243	1292	1303	1352	1363	1412	1423	1472
	153	1543	1592	1603	1652	1663	1712	1723	1772	1783	1832	1843	1892	1903
	195	2012	2023	2072	2083	2132	2143	2192	2204	2236	2248	2280	2292	2324
	236	2380	2412	2424	2456	2468	2500	2512	2544	2556	2588	2600	2632	2644
	268	2720	2732	2764	2776	2808	2820	2852	2864	2896	2911	2951	2986	3031
.PAGE	558	605	863	895										
.REFM														
.REPT	607	1232	2192											
.TITLE	539													

ERRORS DETECTED: 0
 DEFAULT GLOBALS GENERATED: 0

*DZDHC.B.DZDHC.B.SEQ/CRF/SOL/PAGNUM=DSKZ:UTIL2.P11,DZDHC.B.PFC
 RUN-TIME: 14 26 4 SECONDS
 RUN-TIME RATIO: 107/45=2.3
 CORE USED: 12K (23 PAGES)

