

KW11-P

REAL TIME CLOCK TEST
CZKWBIO

AH-8878I-MC

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FICHE 1 OF 1

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MADE IN USA

This microfiche card contains a grid of frames, likely representing a real-time clock test. The frames are arranged in approximately 15 rows and 4 columns. Each frame contains a small table or data set. The data is too small to read clearly but appears to be organized in a structured format, possibly showing time intervals and test results. The frames are separated by dark lines, and the overall layout is typical of a microfiche card used for data storage and retrieval.

1.0 ABSTRACT

THIS PROGRAM TESTS THE KW11-P REAL TIME CLOCK. IT CONTAINS A SERIES OF INCREMENTAL ROUTINES THAT TEST THE CONTROL AND STATUS REGISTER, COUNT SET BUFFER, COUNTER, AND INTERRUPT VECTOR ADDRESS USING 100KHZ, 10KHZ, LINE AND EXTERNAL FREQUENCIES.

2.0 REQUIREMENTS
2.1 EQUIPMENT

PDP-11 WITH KW11-P

2.2 STORAGE

THIS PROGRAM OCCUPIES MEMORY FROM 0 TO 11636.

3.0 LOADING PROCEDURE

3.1 METHOD

PROCEDURE FOR NORMAL BINARY TAPES SHOULD BE FOLLOWED

1. ABSOLUTE LOADER MUST BE IN MEMORY.
2. PLACE BINARY TAPE IN READER.
3. LOAD ADDRESS *7500 (* DETERMINED BY LOCATION OF LOADER).
4. PRESS "START" (PROGRAM WILL LOAD).

4.0 STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

SET SW0=1 TO SUPPRESS TESTS USING EXTERNAL FREQUENCY.
SET SW2=1 TO INCLUDE REPEATABILITY TEST T25 & T26 IF COW IS PRESENT

4.2 STARTING ADDRESSES

200 BASIC TEST
204 RESTART ADDRESS-PRIMARYLY USED BY XOR TESTER
210 TIMING TEST
214 DOUBLE OR SINGLE REAL TIME CLOCK TEST. 100KHZ.
220 DOUBLE OR SINGLE REAL TIME CLOCK TEST. 10KHZ.
224 DOUBLE OR SINGLE REAL TIME CLOCK TEST. 60HZ.
230 DOUBLE OR SINGLE REAL TIME CLOCK TEST 50HZ

4.3 PROGRAM AND/OR OPERATOR ACTION

**NOTE: IF NO HARDWARE SWITCH REGISTER IS AVAILABLE THE PROGRAM WILL AUTOMATICALLY USE THE CONTENTS OF LOC. 176 AS THE SOFTWARE SWITCH REGISTER. THE USER SHOULD SET UP THIS LOC. BEFORE STARTING THE PROGRAM.

LOAD PROGRAM INTO MEMORY
SET SWITCH REGISTER TO STARTING ADDRESS
LOAD ADDRESS.
IF DESIRED TO SUPPRESS EXTERNAL FREQUENCY TESTS SET SW0=1.
PRESS START
PROGRAM WILL BEGIN TESTING

5. OPERATING PROCEDURE

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5.1 OPERATIONAL SWITCH SETTINGS
5.1.1 BASIC TEST

WITH SWITCHES 12 THRU 15=0 (DOWN) THE PROGRAM WILL PRINT OUT ON ERRORS AND CONTINUE IN TEST. BELL WILL RING AT COMPLETION OF A PASS.

SWITCH SETTINGS ARE:

SW15=1 OR UP...HALT ON ERROR
SW14=1 OR UP...SCOPE LOOP
SW13=1 OR UP...INHIBIT PRINTOUT
SW11=1 OR UP...SINGLE ITERATIONS ONLY
SW4 =1 OR UP...ENABLE SYNCHRONIZATION TESTS
SW3 =1 OR UP...ADJUSTS DELAYS FOR 11/60, 11/70 OR 11/45 WITH MOS OR BIPOLAR MEMO
SW2 =1 OR UP...CLK2 PRESENT-EXECUTE REPEATABILITY TESTS

5.2 SUBROUTINE ABSTRACTS

5.2.1 SCOPE

THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUB-TEST IN THE BASIC TEST SECTION. IT RECORDS THE STARTING ADDRESS OF EACH SUB-TEST AS IT IS BEING ENTERED. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUB-TEST INDICATED BY "SCOPE".

5.2.2 HLT

THIS SUBROUTINE CALL PRINTS THE ADDRESS THAT TAGS THE FAILING SUB-TEST AND THE CONTENTS OF THE CONTROL AND STATUS REGISTER, COUNTER, AND "TEMP".

6. ERRORS

6.1 ERROR PRINTOUT FORMAT

WITH SW13=0 (OR DOWN) THE FOLLOWING PRINTOUT WILL APPEAR ON AN ERROR:

| PC | STATUS | COUNTER | TEMP |
|--------|--------|---------|--------|
| XXXXXX | XXXXXX | XXXXXX | XXXXXX |

PC = ADDRESS OF TEST WHERE ERROR OCCURRED
STATUS = CONTENTS OF COMMAND AND STATUS REGISTER AT TIME OF ERROR
COUNTER = CONTENTS OF COUNTER AT TIME OF ERROR
TEMP = CONTENTS OF ADDRESS "TEMP" USED BY SOME TESTS.

NOTE: NOT ALL OF THE INFORMATION PRINTED IS INTENDED TO BE USEFUL FOR EVERY TYPE OF ERROR. THIS IS SIMPLY A STANDARD ERROR REPORT FOR ALL ERRORS. THE OPERATOR MUST REFER TO THE PROGRAM LISTING AT THE ADDRESS OR THE ERROR FOR A DESCRIPTION OF THE CAUSE OF THE ERROR.

6.2 ERROR RECOVERY

WITH SWITCH 15=1 (OR UP) THE PROGRAM WILL HALT ON AN ERROR. DEPRESS "CONTINUE" TO RESUME TESTING.

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7. RESTRICTIONS

7.1 OPERATIONAL RESTRICTIONS

FOR PURPOSES OF TESTING THE EXTERNAL FREQUENCY SELECTION IT IS NECESSARY TO SUPPLY A KNOWN FREQUENCY TO THE EXTERNAL FREQUENCY INPUT. THIS PROGRAM USES THE INTERNAL 60HZ FOR ITS SOURCE. TO DO THIS IT IS REQUIRED THAT A JUMPER WIRE BE CONNECTED BETWEEN PINS CF1 AND DA1 OF THE SLOT IN WHICH THE CLOCK MODULE IS INSERTED. IF THIS IS NOT DONE, THEN THE PROGRAM MUST ALWAYS BE RUN WITH SWO=1 TO SUPPRESS THE EXTERNAL TESTS.
* IF A SECOND P CLOCK IS BEING USED FOR TEST PURPOSES, SET THE SWITCH REG = 000004 TO ENABLE TESTS T25 AND T26, DURING THE BASE TEST

8. MISCELLANEOUS

8.1 EXECUTION TIME

BASIC TEST REQUIRES 11 SECONDS PER PASS W/O ITERATIONS 66 WITH. TIMING TEST REQUIRES 4 MINUTES PER PASS.
DOUBLE OR SINGLE REAL TIME CLOCK TEST-DETERMINED BY OPERATOR SUGGESTED EXECUTION TIMES ARE:

1. IF THE SINGLE CLOCK TEST IS RUN WITHOUT BEING FOLLOWED BY THE DUAL CLOCK TEST: 17 MINUTES FOR EACH FREQUENCY (100KHZ, 10KHZ, 60KHZ)
2. IF THE SINGLE CLOCK TEST IS FOLLOWED BY THE DUAL TEST
RUN SINGLE CLOCK TEST FOR ONE MINUTE (FOR EACH FREQUENCY)
RUN DUAL CLOCK TEST FOR FIFTY SECONDS (10 PRINTOUTS) (FOR EACH FREQUENCY)

NOTE: THIS TIME NOMINAL TIME FOR PDP-11/05
OTHER C.P.U.'S THE TIME WILL VARY

9. PROGRAM DESCRIPTION

THE PROGRAM CONSISTS OF THREE SECTIONS: THE BASIC TEST THE TIMING TEST AND THE REAL TIME CLOCK TEST. THE BASIC TEST CHECKS EACH OF THE INDIVIDUAL BITS IN THE CONTROL AND STATUS REGISTER, COUNT SET BUFFER, AND COUNTER ALONG WITH PROPER OPERATION UNDER INTERRUPT CONTROL (SINGLE OR REPEATED INTERRUPTS) COUNT UP OR COUNT DOWN, AND REPEATABILITY. THE TIMING TEST USES ALL CLOCK FREQUENCIES TO RING THE TELETYPE BELL AT 10 SECOND INTERVALS. THE CLOCK TEST PROVIDES A REAL TIME CLOCK WHOSE ACCURACY CAN BE MEASURED AGAINST AN ACCURATE EXTERNAL SOURCE.

9.1 BASIC TEST

| TEST | DESCRIPTION |
|------------|--|
| TO THRU T9 | TEST THAT CSR, COUNT SET BUFFER AND COUNTER BITS MAY BE SET AND CLEARED. |

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- T10 THRU T11 TEST FIX(BITS) TO SINGLE CLOCK COUNTER.
- T12 THRU T15 TEST CLOCK TO COUNT UP.
- T16 THRU T19 TEST CLOCK TO COUNT DOWN.
- T20 THRU T24 TEST INTERRUPT MODES.
- T25 THRU T26 TEST REPEATABILITY BY CHECKING THAT THE COUNTER CONTAINS THE SAME NUMBER OF COUNTS OVER TWO EQUAL PERIODS OF TIME.

9.2 TIMING TEST

THIS TEST USES THE REPEATED INTERRUPT MODE TO RING THE TELETYPE BELL AT 10 SECOND INTERVALS. FIRST THE BELL IS RUNG AT 10 SECOND INTERVALS FOR 1 MINUTE USING 100HZ, FOLLOWED BY 1 MINUTE AT 10KHZ FOLLOWED BY 1 MINUTE AT LINE FREQ. (60HZ OR 50HZ) AND (IF SWD=0) 1 MINUTE AT LINE FREQ. USING EXTERNAL FREQUENCY INPUT.

9.3 DOUBLE OR SINGLE REAL TIME CLOCK TEST

9.3.1 SINGLE CLOCK REAL TIME TEST

THE 24 HOUR CYCLE:
THIS TEST TRANSFORMS YOUR COMPUTER INTO AN ACCURATE DIGITAL "WALL CLOCK." A NORMAL CLOCK'S 12 HOUR CYCLE HAS BEEN REPLACED BY A 24 HOUR CYCLE.

EXAMPLES OF THE 24 HOUR CYCLE FOLLOW:

| ACTUAL TIME | PRINTOUT | | | | | | |
|-------------|----------|------|------|---------------------------|----|---|----|
| ----- | HRS | MINS | SECS | TENTHS+HUNDRETHS OF SECS. | | | |
| MIDNIGHT | 00 | : | 00 | : | 00 | : | 00 |
| 8:32 AM | 08 | : | 32 | : | 00 | : | 00 |
| 12 NOON | 12 | : | 00 | : | 00 | : | 00 |
| 2:15 PM | 14 | : | 15 | : | 00 | : | 00 |
| 11:30 PM | 23 | : | 30 | : | 00 | : | 00 |

9.3.1.1 ENTERING THE TIME

THE CLOCK CAN BE UPDATED BY HOLDING THE CTRL KEY DOWN AND TAPPING THE I KEY. THE CTRL KEY IS THEN RELEASED, AND THE STARTING TIME IS ENTERED.

THE MOST SIGNIFICANT HOUR DIGIT IS ENTERED FIRST. THIS DIGIT MUST BE A ZERO, A ONE OR A TWO. THE LEAST SIGNIFICANT HOURS DIGIT IS ENTERED NEXT FOLLOWED BY THE TWO MINUTES DIGIT, FOLLOWED BY THE TWO SECONDS DIGIT. THE FRACTION OF A SECOND DIGITS ARE NOT ENTERED. THE USER WILL ENTER A TOTAL OF SIX DIGITS WITH NO SPACES, COLONS, OR ANY OTHER CHARACTERS BETWEEN DIGITS. THE USER MUST

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ENTER A TIME THAT WILL OCCUR A HALF MINUTE OR MORE IN THE FUTURE, TO ALLOW ENOUGH TIME TO ENTER THE REQUIRED INFORMATION. AFTER THE INFORMATION HAS BEEN ENTERED, THE USER MONITORS THE TIME STANDARD. WHEN THAT STANDARD REACHES THE TIME ENTERED VIA THE KEYBOARD, THE USER HITS THE CARRAGE RETURN (CR) KEY TO START THE CLOCK. NOTE THAT THE CHARACTERS WILL NOT BE PRINTED OUT AS THE TIME IS BEING ENTERED.

9.3.1.2 READING THE TIME

TO PRINT THE TIME, DEPRESS THE CTRL KEY. WHILE HOLDING THE CTRL KEY DOWN, SMARTLY TAP THE T KEY. THE TIME WHICH CORRESPONDS TO THE INSTANT THAT THE T KEY WAS DOWN, WILL BE PRINTED OUT. THE FORMAT OF THE PRINTOUT WILL BE SIMILAR TO THAT SHOWN IN THE 24 HOUR TIME EXAMPLE. THE ONLY DIFFERENCE WILL BE THE ABSENCE OF SPACES.

9.3.1.3 TIME REFERENCES

SINCE THE SYSTEM CLOCK IS MORE ACCURATE THAN MANY WRIST WATCHES, IT IS A GOOD IDEA TO USE AN ACCURATE TIME STANDARD. MANY TELEPHONE COMPANIES PROVIDE A NUMBER WHERE THE TIME, SYNCHRONIZED TO THE NATIONAL BUREAU OF STANDARDS RADIO STATION (WWV), IS AVAILABLE. CONSULT WITH YOUR LOCAL TELEPHONE COMPANY TO SEE IF THIS SERVICE IS AVAILABLE IN YOUR AREA.

9.3.1.4 PROCEDURE FOR SINGLE CLOCK REAL TIME TEST.

1. PERFORM THE BASIC TEST, PRIOR TO THE PERFORMANCE OF THIS TEST. PROCEED ONLY IF THE BASIC TEST HAS PASSED.
2. LOAD ADDRESS 214 VIA THE SWITCH REGISTER, (100KHZ TEST)
3. PLACE ALL ZEROS IN SWITCH REG., DEPRESS START
4. EXAMINE YOUR TIME REFERENCE, AND SELECT A TIME THAT WILL ALLOW YOU ENOUGH TIME TO ENTER THE TIME VIA THE KEYBOARD.
5. ENTER THE TIME, AS DESCRIBED PREVIOUSLY.
6. START THE CLOCK (HIT THE CR KEY) AT THE INSTANT THE TIME REFERENCE CORRELATES WITH THE TIME ENTERED.
7. MONITOR YOUR TIME REFERENCE, EXACTLY 1 MINUTE FROM THE TIME YOU STARTED THE CLOCK, READ THE PROGRAM CLOCK AS DESCRIBED PREVIOUSLY.
8. THE ONE MINUTE TIME ERROR SHOULD BE WITHIN ONE SECOND OF THE ACTUAL TIME.
9. IF THE RESULT OF STEP 8 IS NOT WITHIN ONE SECOND, ALLOW EXACTLY ONE MORE MINUTE TO PASS (FROM THE ORIGINAL START TIME). READ THE TIME AGAIN. IF THE TOTAL ERROR DOUBLED, THE BOARD IS DEFECTIVE. IF THE ERROR IS CONSTANT,

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RESTART THE TEST.

- 10.* IF THE ONE MINUTE TEST WAS PASSED, ALLOW THE TEST TO RUN FOR EXACTLY 16 MINUTES MORE. AT THE EXACT END OF THE 16TH MINUTE INTERVAL, READ THE CLOCK. IT SHOULD BE WITHIN THREE SECONDS OF THE CORRECT TIME. IF IT IS NOT, THE BOARD IS DEFECTIVE. IN THE EVENT THAT THE DUAL CLOCK REAL TIME TEST IS GOING TO BE PERFORMED, THIS STEP CAN BE OMITTED.
11. LOAD ADDRESS 220 VIA SWITCH REGISTER, DEPRESS START (10KHZ TEST) REPEAT STEPS 3-10
12. LOAD ADDRESS 224 VIA SWITCH REGISTER, DEPRESS START (224 IF 60HZ, OR 230 IF 50HZ LINE TEST) REPEAT STEPS 3-10

* THE DURATION OF THIS TEST IS ARBITRARY. IT IS NOMINALLY A THOUSAND SECOND TEST. LONGER TESTS ARE PERMISSIBLE. THE RESULTS OF LONG TERM TESTS SHOULD BE WITHIN (PLUS OR MINUS) 1 MINUTE FOR A 24 HR TEST.

NOTE THAT THE TIME CAN BE READ AT ANY POINT WITHIN THE TEST WITHOUT AFFECTING THE TEST.

9.3.2 DUAL CLOCK REAL TIME CLOCK TEST

THE USE OF A TEMPORARY CLOCK (REFERED AS COW) REDUCES THE TIME REQUIRED FOR THE REAL TIME TEST. THE SECOND CLOCK INTERRUPTS THE FIRST CLOCK EVERY FIVE SECONDS. THE DURATION OF THE COMBINED REAL TIMES TESTS, WHEN THE DUAL CLOCK TEST IS USED IS 1 MIN : 50 SEC/FREQ VERSUS 17 MIN/FREQ FOR THE SINGLE CLOCK REAL TIME TEST ALONE.

THE DUAL CLOCK TEST REQUIRES THAT THE CLOCK BE STARTED AS IN THE SINGLE MODE. RAISING SWITCHES #0 AND #2 CAUSE THE PRINTOUT TO OCCUR AUTOMATICALLY.

THE COW MODULE SHOULD ONLY BE INSTALLED IN THE SYSTEM WHILE THIS DIAGNOSTIC IS BEING USED.

TO CONVERT A STANDARD F CLOCK TO A "COW" MODULE:

1. REMOVE JUMPER A4
CSR=772560
CSB=772562
CTR=772564
2. ADD JUMPER V8
VECTOR LOCATION IS 504
PSW " " 506

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NOTE: THIS VECTOR IS IN FLOATING VECTOR SPACE, CAUTION IS ADVISED WITH RESPECT TO ALLOWING VECTOR CONFLICTS.

9.3.2.1 PROCEDURE FOR DUAL CLOCK REAL TIME CLOCK TEST

1. LOAD ADDRESS 214, DEPRESS START (100KHZ TEST)
2. ENTER THE TIME VIA THE TTY KEYBOARD AS DESCRIBED PREVIOUSLY
3. SET THE SWITCHES IN THE SWITCH REGISTER TO 000005. THE TTY WILL PRINT THE TIME AT 5 SECOND INTERVALS
4. CONSECUTIVE PRINTOUTS WILL BE WITHIN 5.00 PLUS OR MINUS .01 SECONDS OF EACH OTHER. ALLOW THE TEST TO RUN FOR AT LEAST TEN PRINTOUTS. IF THE TOLERANCE IS EXCEEDED, THE CLOCK IS DEFECTIVE.
5. LOAD ADDRESS 220, DEPRESS START (10KHZ TEST)
6. REPEAT STEPS 2-4
7. LOAD ADDRESS 224, IF 60HZ, OR 230 IF 50HZ DEPRESS START (LINE TEST)
8. REPEAT STEPS 2 & 3
9. CONSECUTIVE PRINTOUTS WILL BE WITHIN 5.00 PLUS OR MINUS .04 SECONDS OF EACH OTHER. TYPICALLY, AND 5.00 PLUS OR MINUS .2 SECONDS WORST CASE, DUE TO POSSIBLE AC LINE FREQUENCY VARIATIONS. ALLOW THE TEST TO RUN FOR AT LEAST TEN PRINTOUTS. IF THE TOLERANCE IS EXCEEDED, THE CLOCK IS DEFECTIVE.

10.

THIS KW11-P DIAGNOSTIC WILL GO OUT & FIND IF THIS SHOULD RUN WITH CPU THAT HAS A SWITCH REG. OR WILL RUN WITH A PDP-11/04 THAT HAS NO SWITCH REGISTER. IF CPU HAS NO SWITCH REG. LOCATION 176 EQUALS SOFTWARE SWITCH REGISTER. IN THE ABOVE TEST TYPING ↑G(CONTROL-G) WILL ALLOW YOU TO ENTER/ALTER THE SOFTWARE SWITCH SETTINGS .ENDR

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429 .TITLE CZKWBHO KW11-P RT CLK TST
430
431 .SBTTL BASIC TEST
432 :COPYRIGHT 1971, 1978 DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754
433 ;JOHN RODENHISER/JIM LACEY
434 .ENABL AMA,ABS
435 =0
436 ;TRAP CATCHER 0-200
437 =30
438 000030 005650 PRINT
439 000032 000340 340
440 000034 006150 SCOPEC
441 000036 000340 340
442 000046 LOGICAL
443 000046 005174 HLT=EMT
444 104000 CC=177776
445 177776 NOP=240
446 000240 SCOPE=TRAP
447 104400 SOFTSR=176
448 000176 ;SOFTWARE SWITCH REGISTER
449 000776 BUFF=776
450 000200 =200
451 000200 000137 001046 JMP @#BEGIN2 ;START BASIC TEST
452 000204 000137 001150 JMP @#BEGIN ;RESTART BASIC TEST
453 000210 000137 005210 JMP @#BEGIN1 ;START TIMING TEST
454 000214 000137 006714 JMP @#K100HZ ;DOUBLE OR SINGAL CLK TEST. 100KHZ.
455 000220 000137 007000 JMP @#K10HZ ;DOUBLE OR SINGLE CLK TEST. 10KHZ.
456 000224 000137 007064 JMP @#H60Z ;DOUBLE OR SINGLE CLK TEST. 60HZ.
457 000230 000137 007150 JMP @#H50Z ;DOUBLE OR SINGLE CLK TEST. 50HZ
458
459 001000 =1000
460 001000 172540 CSR: 172540 ;CONTROL AND STATUS REGISTER
461 001002 172542 CSB: 172542 ;COUNT SET BUFFER
462 001004 172544 CTR: 172544 ;COUNTER
463 001006 000104 CKV: 104 ;CLOCK VECTOR ADDRESS
464 001010 000106 CKVS: 106
465 001012 177566 TDBR: 177566
466 001014 177564 TCSR: 177564
467 001016 000000 TEMP1: 0
468 001020 000000 TEMP: 0
469 001022 000001 ICOUNT: 1
470 001024 177740 DEL1: -40
471 001026 177730 DEL2: -50
472 001030 160000 DEL3: -20000
473 001032 160000 DEL4: -20000
474 001034 177700 ADJ: -100 ;DELAY ADJUSTMENT FOR 11/70
475 ; & 11/45 WITH MOS MEM.
476 001036 177660 -120
477 001040 140000 -40000
478 001042 140000 -40000
479 001044 177570 SR: 177570
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484 001046 012706 000776 BEGIN2: MOV #BUFF,%6

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K01

CZKWBHO KW11-P RT CLK TST
CZKWB1.P11 30-JAN-78 09:34

MACY11 30A(1052) 30-JAN-78 09:35 PAGE 10
BASIC TEST

SEQ 0010

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485 001052 023737 000042 000046      CMP      @#42, @#46      ;UNDER ACT ?
486 001060 001404          BEQ      1$            ;YES-SKIP TITLE PRINT OUT
487 001062 012702 006436          MOV      #MSG3, %2
488 001066 004737 006266          JSR      %7, TOP      ;PRINT TITLE
489 001072 004737 011652          JSR      %7, SWADJ    ;HAS THIS CPU HAVE A SWITCH REG.?
490 001076 004737 011610          JSR      %7, DELADJ   ;IS ADJUSTMENT IN DELAY REQUIRED
491 001102 013746 000004          MOV      @#4, -(%6)
492 001106 012737 001230 000004      MOV      #XOR, @#4
493 001114 005737 177060          TST      @#177060
494 001120 012637 000004          MOV      (%6)+, @#4
495 001124 012737 177777 006252      MOV      #-1, @XORFLG
496 001132 012737 000001 001022      MOV      #1, @ICOUNT
497 001140 012702 006540          MOV      #XORM, %2
498 001144 004737 006266          JSR      %7, TOP
499
500 001150 012706 000776          BEGIN:  MOV      #BUFF, %6      ;SET UP STACK FOR SCOPE LOOPS
501 001154 004737 011652          JSR      %7, SWADJ    ;HAS THIS CPU HAVE A SWITCH REG.?
502 001160 004737 011610          JSR      %7, DELADJ   ;IS ADJUSTMENT IN DELAY REQUIRED
503 001164 012737 005572 000024      MOV      #PWF1, 24    ;INIT POWER FAIL POINTER
504 001172 005077 005442          CLR      @PSW        ;CLEAR PROC. STATUS REG.
505 001176 005037 001020          CLR      TEMP
506 001202 005037 006250          CLR      SCOPEF      ;INIT. SCOPEF TAG
507 001206 005037 001016          CLR      TEMP1
508 001212 012737 001254 006264      MOV      #TO, RETURN  ;SET UP RESTART OF PROGRAM
509 001220 005037 005764          CLR      PRINT1     ;INITIALIZE ERROR PRINTOUT READING
510 001224 000137 001254          JMP      TO
511
512 001230 022626          XOR:    CMP      (%6)+, (%6)+
513 001232 012637 000004 001022      MOV      (%6)+, @#4
514 001236 012737 000005          MOV      #5, @ICOUNT
515 001244 005037 006252          CLR      @XORFLG
516 001250 000137 001150          JMP      @BEGIN
517
518          ;TEST INIT TO CLEAR CONTROL AND STATUS REGISTER
519
520 001254 013746 000004          TO:    MOV      @#4, -(%6)
521 001260 012737 001312 000004      MOV      #CSRT, @#4
522 001266 012777 100377 177504      MOV      #100377, @CSR
523 001274 000005          RESET
524 001276 032777 100377 177474      BIT      #100377, @CSR
525 001304 001413          BEQ      T1
526 001306 104000          HLT
527 001310 000411          BR      T1          ;ERROR, INIT FAILED TO CLEAR ALL BITS OF CSR.
528 001312 022626          CSRT:  CMP      (%6)+, (%6)+
529 001314 012637 000004          MOV      (%6)+, @#4
530 001320 032777 040000 177516      BIT      #40000, @SR
531 001326 001352          BNE     TO
532 001330 000000          HALT
533 001332 000750          BR      TO          ;NO SSYN FROM DEVICE
534
535          ;TEST COUNT SET BUFFER
536 001334 012637 000004          †1:   MOV      (%6)+, @#4
537 001340 104400          SCOPE
538 001342 012777 177777 177432      MOV      #-1, @CSB
539 001350 005777 177426          TST      @CSB
540 001354 001401          BEQ     .+4
541 001356 104000          HLT
542 001360 012737 177777 001020      MOV      #-1, @TEMP

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541 001366 012777 000000 177410      MOV      #0, @CTR
542 001374 023777 001020 177402      CMP      @#TEMP, @CTR
543 001402 001401                BEQ      .+4
544 001404 104000                HLT
                    ;CTR CHANGED WHEN WRITTEN TO
545                ;TEST COUNT SET BUFFER TO ACCEPT A COUNT PATTERN
546                ;TEST COUNTER TO CONTAIN COUNT SET BUFFER VALUE
547 001406 005037 001020      CLR      TEMP
548 001412 104400                SCOPE
549 001414 013777 001020 177360 T3:      MOV      TEMP, @CSB
550 001422 023777 001020 177354      CMP      TEMP, @CTR
551 001430 001401                BEQ      .+4
552 001432 104000                HLT
                    ;ERROR, CTR NOT=TEMP
553 001434 005237 001020      INC      TEMP                ;+1 TO COUNT PATTERN
554 001440 001365                BNE      T3                ;REPEAT UNTIL COUNT OVERFLOWS
555                ;TEST THAT CTR REMAINS CONSTANT IF RUN CLEAR
556 001442 104400      †3A:      SCOPE
557 001444 005077 177330      CLR      @CSR
558 001450 012777 177777 177324      MOV      #-1, @CSB
559 001456 013737 001030 001020      MOV      @#DEL3, @#TEMP
560 001464 005237 001020      1S:      INC      @#TEMP
561 001470 001375                BNE      1S
562 001472 022777 177777 177304      CMP      #-1, @CTR
563 001500 001401                BEQ      .+4
564 001502 104000                HLT
                    ;CTR CHANGED ALTHOUGH RUN 0
565                ;TEST THAT CTR REMAINS CONSTANT WHEN CSR IS REF'D
566 001504 104400      †3B:      SCOPE
567 001506 005077 177266      CLR      @CSR
568 001512 012777 177777 177262      MOV      #-1, @CSB
569 001520 013737 001030 001020      MOV      @#DEL3, @#TEMP
570
571 001526 012777 177736 177244      1S:      MOV      #177736, @CSR
572 001534 017700 177240      MOV      @CSR, %0
573 001540 012777 000000 177232      MOV      #0, @CSR
574 001546 017700 177226      MOV      @CSR, %0
575 001552 005237 001020      INC      @#TEMP
576 001556 001363                BNE      1S
577 001560 022777 177777 177216      CMP      #-1, @CTR
578 001566 001401                BEQ      .+4
579 001570 104000                HLT
                    ;CTR CHANGED BY CSR REF
580                ;TEST INIT TO CLEAR COUNT SET BUFFER WHEN IT IS =-1
581 001572 104400      †4:      SCOPE
582 001574 012777 177777 177200      MOV      #-1, @CSB
583 001602 000005                RESET
584 001604 005777 177174                TST      @CTR
585 001610 001401                BEQ      .+4
586 001612 104000                HLT
                    ;ERROR, INIT FAILED TO CLEAR CSB
587                ;TEST RATE SELECT (BIT,2) MAY BE SET AND CLEARED
588 001614 104400      †5:      SCOPE
589 001616 012777 000002 177154      MOV      #2, @CSR
590 001624 022777 000002 177146      CMP      #2, @CSR
591 001632 001401                BEQ      .+4
592 001634 104000                HLT
                    ;ERROR, CSR NOT = 2
593 001636 012777 000004 177134      MOV      #4, @CSR
594 001644 022777 000004 177126      CMP      #4, @CSR
595 001652 001401                BEQ      .+4
596 001654 104000                HLT
                    ;ERROR, CSR NOT = 4

```

BASIC TEST

| | | | | | | | |
|-----|--------|--------|--------|--------|---|-----------|--|
| 597 | 001656 | 012777 | 000006 | 177114 | MOV | #6,@CSR | |
| 598 | 001664 | 022777 | 000006 | 177106 | CMP | #6,@CSR | |
| 599 | 001672 | 001401 | | | BEQ | +.4 | |
| 600 | 001674 | 104000 | | | HLT | | ;ERROR, CSR NOT = 6 |
| 601 | 001676 | 005077 | 177076 | | CLR | @CSR | |
| 602 | 001702 | 005777 | 177072 | | TST | @CSR | |
| 603 | 001706 | 001401 | | | BEQ | +.4 | |
| 604 | 001710 | 104000 | | | HLT | | ;ERROR, CSR NOT = 0 |
| 605 | | | | | ;TEST MODE (BIT 3) CAN BE SET AND CLEARED | | |
| 606 | 001712 | 104400 | | | T6: | SCOPE | |
| 607 | 001714 | 012777 | 000010 | 177056 | MOV | #10,@CSR | |
| 608 | 001722 | 022777 | 000010 | 177050 | CMP | #10,@CSR | |
| 609 | 001730 | 001401 | | | BEQ | +.4 | |
| 610 | 001732 | 104000 | | | HLT | | ;ERROR, CSR NOT = 10 |
| 611 | 001734 | 005077 | 177040 | | CLR | @CSR | |
| 612 | 001740 | 005777 | 177034 | | TST | @CSR | |
| 613 | 001744 | 001401 | | | BEQ | +.4 | |
| 614 | 001746 | 104000 | | | HLT | | ;ERROR, CSR NOT = 0 |
| 615 | | | | | ;TEST LIP/DN (BIT 4) CAN BE SET AND CLEARED | | |
| 616 | 001750 | 104400 | | | T7: | SCOPE | |
| 617 | 001752 | 012777 | 000020 | 177020 | MOV | #20,@CSR | |
| 618 | 001760 | 022777 | 000020 | 177012 | CMP | #20,@CSR | |
| 619 | 001766 | 001401 | | | BEQ | +.4 | |
| 620 | 001770 | 104000 | | | HLT | | ;ERROR, CSR NOT = 20 |
| 621 | 001772 | 005077 | 177002 | | CLR | @CSR | |
| 622 | 001776 | 005777 | 176776 | | TST | @CSR | |
| 623 | 002002 | 001401 | | | BEQ | +.4 | |
| 624 | 002004 | 104000 | | | HLT | | ;ERROR, CSR NOT = 0 |
| 625 | | | | | | | |
| 626 | | | | | | | |
| 627 | | | | | ;TEST INTERRUPT ENABLE (BIT 6) CAN BE SET AND CLEARED | | |
| 628 | 002006 | 104400 | | | T9: | SCOPE | |
| 629 | 002010 | 012737 | 000340 | 177776 | MOV | #340,CC | ;SET PROCESSOR PRIORITY LEVEL 7 |
| 630 | 002016 | 012777 | 000100 | 176754 | MOV | #100,@CSR | |
| 631 | 002024 | 022777 | 000100 | 176746 | CMP | #100,@CSR | |
| 632 | 002032 | 001401 | | | BEQ | +.4 | |
| 633 | 002034 | 104000 | | | HLT | | ;ERROR, CSR NOT = 100 |
| 634 | 002036 | 005077 | 176736 | | CLR | @CSR | |
| 635 | 002042 | 005777 | 176732 | | TST | @CSR | |
| 636 | 002046 | 001401 | | | BEQ | +.4 | |
| 637 | 002050 | 104000 | | | HLT | | ;ERROR, CSR NOT = 0 |
| 638 | | | | | ;TEST RUN (BIT 0) CAN BE SET AND CLEARED | | |
| 639 | | | | | T9A: | SCOPE | |
| 640 | 002052 | 104400 | | | CLR | @CSR | |
| 641 | 002054 | 005077 | 176720 | | CLR | TEMP | |
| 642 | 002060 | 005037 | 001020 | | CLR | TEMP | |
| 643 | 002064 | 013777 | 001020 | 176710 | MOV | TEMP,@CSB | ;START AT ZERO |
| 644 | 002072 | 012777 | 000021 | 176700 | MOV | #21,@CSR | ;DISABLE INTERRUPT, COUNT UP, SET RUN |
| 645 | 002100 | 032777 | 000001 | 176672 | BIT | #1,@CSR | ;CHECK IF ZERO IS STILL SET |
| 646 | 002106 | 001001 | | | BNE | +.4 | |
| 647 | 002110 | 104000 | | | HLT | | ;CSR LOST BIT 0 AFTER BIT INSTRUCTION |
| 648 | 002112 | 104400 | | | SCOPE | | |
| 649 | 002114 | 005077 | 176660 | | CLR | @CSR | |
| 650 | 002120 | 005037 | 001020 | | CLR | TEMP | |
| 651 | 002124 | 013777 | 001020 | 176650 | MOV | TEMP,@CSB | ;START AT ZERO |
| 652 | 002132 | 012777 | 000020 | 176640 | MOV | #20,@CSR | ;DISABLE INTERRUPT, COUNT UP, DO NOT SET RUN |

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653 002140 052777 000001 176632      BIS      #1, @CSR      ;SET RUN
654 002146 032777 000001 176624      BIT      #1, @CSR      ;CHECK IF BIT 0 IS SET
655 002154 001001                BNE      .+4
656 002156 104000                HLT
657 002160 104400                SCOPE
658 002162 005077      176612      CLR      @CSR
659 002166 005037      001020      CLR      TEMP
660 002172 013777      001020      176602      MOV      TEMP, @CSB      ;START AT ZERO
661 002200 012777      000021      176572      MOV      #21, @CSR      ;DISABLE INTERRUPT, COUNT UP, SET RUN
662 002206 012777      000020      176564      MOV      #20, @CSR      ;LEAVE ALL SAME RESET RUN
663 002214 032777      000001      176556      BIT      #1, @CSR      ;CHECK BIT 0
664 002222 001401                BEQ      .+4      ;BRANCH IF NOT SET
665 002224 104000                HLT      ;CSR PICKED BIT 0 ON A MOV.
666
667
668
669      ; TEST FIX (BIT 5) TO SINGLE CLOCK COUNTER
670 002226 104400                ; SET UP/DN (BIT 4) =0 TO ENABLE COUNT DOWN
671 002230 005077      176544      T10:     SCOPE
672 002234 012777      177777      176540      CLR      @CSR
673 002242 012737      177776      001020      MOV      #-1, @CSB
674 002250 012777      000040      176522      T10A:    MOV      #-2, TEMP
675 002256 023777      001020      176520      MOV      #40, @CSR
676 002264 001401                CMP      TEMP, @CTR
677 002266 104000                BEQ      .+4
678 002270 005337      001020                HLT      ;ERROR, COUNTER NOT = TEMP, DIDN'T COUNT DOWN
679 002274 023727      001020      000000      DEC      TEMP      ; -1 TO PATTERN COUNT
680 002302 001362                CMP      TEMP, #0      ; DONE ALL COUNTS?
681                BNE      T10A      ; NO
682      ;TEST FIX (BIT 5) TO SINGLE CLOCK COUNTER
683 002304 104400                ;SET UP/DN (BIT 4)=1 TO ENABLE COUNT UP
684 002306 005077      176466      T11:     SCOPE
685 002312 005077      176464      CLR      @CSR
686 002316 012737      000001      001020      CLR      @CSB
687 002324 012777      000060      176446      T11A:    MOV      #1, TEMP
688 002332 023777      001020      176444      MOV      #60, @CSR
689 002340 001401                CMP      TEMP, @CTR
690 002342 104000                BEQ      .+4
691 002344 005237      001020                HLT      ;ERROR, COUNTER NOT = TEMP, FAILED TO COUNT UP.
692 002350 023727      001020      000000      INC      TEMP      ; +1 TO PATTERN COUNT
693 002356 001362                CMP      TEMP, #0      ; DONE ALL COUNTS ?
694                BNE      T11A      ; NO
695      ;TEST CLOCK TO COUNT DOWN AT ALL FREQUENCIES
696      ;100KHZ
697 002360 104400                T12:     SCOPE
698 002362 005077      176412      CLR      @CSR
699 002366 012777      000002      176406      MOV      #2, @CSB      ;COUNT SET BUFFER TO 2
700 002374 012777      000001      176376      MOV      #1, @CSR      ;DOWN COUNT , 100KHZ, GO
701 002402 013737      001024      001020      MOV      @DEL1, @TEMP
702 002410 105777      176364      T12A:    TSTB   @CSR
703 002414 100410                BMI     T12B
704 002416 062737      000001      001020      ADD      #1, @TEMP
705 002424 001371                BNE     T12A
706 002426 042777      000001      176344      BIC     #1, @CSR
707 002434 104000                HLT
708 002436 005777      176342      T12B:    TST   @CTR
709 002442 001401                BEQ   .+4

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709 002444 104000 HLT ;ERROR, COUNTER DID NOT COUNT DOWN TO 0
710
711 ;10KHZ
712 002446 104400 T13: SCOPE
713 002450 005077 176324 CLR @CSR
714 002454 012777 000002 176320 MOV @2,@CSB ;DOWN COUNT, 10KHZ, GO
715 002462 012777 000003 176310 MOV @3,@CSR
716 002470 013737 001026 001020 MOV @DEL2,@TEMP
717 002476 105777 176276 T13A: TSTB @CSR
718 002502 100410 BMI T13B
719 002504 062737 000001 001020 ADD @1,@TEMP
720 002512 001371 BNE T13A
721 002514 042777 000001 176256 BIC @1,@CSR
722 002522 104000 HLT ;ERROR, P INTR (BIT 7) NOT = 1.
723 002524 005777 176254 T13B: TST @CTR
724 002530 001401 BEQ .+4 ;ERROR, COUNTER DID NOT COUNTDOWN TO 0
725 002532 104000 HLT
726 ;LINE FREQ.
727 002534 104400 T14: SCOPE
728 002536 005737 006252 TST @XORFLG
729 002542 100432 BMI T15
730 002544 005077 176230 CLR @CSR
731 002550 012777 000002 176224 MOV @2,@CSB ;DOWN COUNT, LINE FREQ., GO
732 002556 012777 000005 176214 MOV @5,@CSR
733 002564 013737 001030 001020 MOV @DEL3,@TEMP
734 002572 105777 176202 T14A: TSTB @CSR
735 002576 100410 BMI T14B
736 002600 062737 000001 001020 ADD @1,@TEMP
737 002606 001371 BNE T14A
738 002610 042777 000001 176162 BIC @1,@CSR
739 002616 104000 HLT ;ERROR, P INTR (BIT 7) NOT=1
740 002620 005777 176160 T14B: TST @CTR
741 002624 001401 BEQ .+4 ;ERROR, COUNTER DID NOT COUNT DOWN TO 0
742 002626 104000 HLT
743 ;EXT FREQ.
744 002630 104400 T15: SCOPE
745 002632 032777 000001 176204 BIT @1,@SR ;
746 002640 001032 BNE T16 ;
747 002642 005077 176132 CLR @CSR
748 002646 012777 000002 176126 MOV @2,@CSB ;DOWN COUNT, EXT., GO
749 002654 012777 000007 176116 MOV @7,@CSR
750 002662 013737 001032 001020 MOV @DEL4,@TEMP
751 002670 105777 176104 T15A: TSTB @CSR
752 002674 100410 BMI T15B
753 002676 062737 000001 001020 ADD @1,@TEMP
754 002704 001371 BNE T15A
755 002706 042777 000001 176064 BIC @1,@CSR
756 002714 104000 HLT ;ERROR, P INTR (BIT 7) NOT=1
757 002716 005777 176062 T15B: TST @CTR
758 002722 001401 BEQ .+4 ;ERROR, COUNTER DID NOT COUNT DOWN TO 0
759 002724 104000 HLT
760 ;TEST CLOCK TO COUNT UP AT ALL FREQUENCIES
761 ;100 KHZ
762 T16: SCOPE
763 002726 104400 CLR @CSR
764 002730 005077 176044

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765 002734 012777 177776 176040      MOV      #-2,@CSB
766 002742 012777 000021 176030      MOV      #21,@CSR      ;UP COUNT, 100 KHZ, GO
767 002750 013737 001024 001020      MOV      @DEL1,@TEMP
768 002756 105777 176016      T16A:    TSTB     @CSR
769 002762 100410      BMI      T16B
770 002764 062737 000001 001020      ADD      #1,@TEMP
771 002772 001371      BNE      T16H
772 002774 042777 000001 175776      BIC      #1,@CSR
773 003002 104000      HLT
774 003004 005777 175774      T16B:    TST      @CTR      ;ERROR
775 003010 001401      BEQ      .+4
776 003012 104000      HLT      ;ERROR
777
778 003014 104400      ;10 KHZ
779 003016 005077 175756      †17:    SCOPE
780 003022 012777 177776 175752      CLR      @CSR
781 003030 012777 000023 175742      MOV      #-2,@CSB      ;UP COUNT, 10 KHZ, GO
782 003036 013737 001026 001020      MOV      #23,@CSR
783 003044 105777 175730      T17A:    MOV      @DEL2,@TEMP
784 003050 100410      BMI      @CSR
785 003052 062737 000001 001020      TSTB     T17B
786 003060 001371      ADD      #1,@TEMP
787 003062 042777 000001 175710      BNE      T17A
788 003070 104000      BIC      #1,@CSR      ;ERROR
789 003072 005777 175706      HLT
790 003076 001401      T17B:    TST      @CTR
791 003100 104000      BEQ      .+4      ;ERROR
792 003102 104400      HLT
793 003104 005737 006252      ;LINE FREQ.
794 003110 100432      †18:    SCOPE
795 003112 005077 175662      TST      @XORFLG
796 003116 012777 177776 175656      BMI      T19
797 003124 012777 000025 175646      CLR      @CSR
798 003132 013737 001030 001020      MOV      #-2,@CSB      ;UP COUNT, LINE, GO
799 003140 105777 175634      T18A:    MOV      #25,@CSR
800 003144 100410      BMI      @DEL3,@TEMP
801 003146 062737 000001 001020      TSTB     @CSR
802 003154 001371      ADD      #1,@TEMP
803 003156 042777 000001 175614      BNE      T18B
804 003164 104000      BIC      #1,@CSR      ;ERROR
805 003166 005777 175612      HLT
806 003172 001401      T18B:    TST      @CTR
807 003174 104000      BEQ      .+4      ;ERROR
808 003176 104400      HLT
809
810 003176 104400      ;EXT FREQ.
811 003200 032777 000001 175636      †19:    SCOPE
812 003206 001033      BIT      #1,@SR
813 003210 005077 175564      BNE      T20
814 003214 012777 177776 175560      CLR      @CSR
815 003222 012777 000027 175550      MOV      #-2,@CSB      ;UP COUNT, EXT FREQ, GO
816 003230 013737 001032 001020      MOV      #27,@CSR
817 003236 105777 175536      T19A:    MOV      @DEL4,@TEMP
818 003242 100411      BMI      @CSR
819 003244 062737 000001 001020      TSTB     T19B
820 003244 062737 000001 001020      ADD      #1,@TEMP

```



```

821 003252 001371      BNE      T19A
822 003254 042777 000001 175516      BIC      #1, @CSR
823 003262 104000      HLT
;ERROR.
824 003264 000005      RESET
825 003266 005777 175512      T19B:   TST      @CTR
826 003272 001401      BEQ      .+4
827 003274 104000      HLT
;ERROR
828
829 003276 104400      ;TEST THAT INTERRUPT OCCURS TO PROPER VECTOR WITH PROCESSOR PRIORITY 4
↑20:   SCOPE
830 003300 012737 000200 177776      MOV      #200, CC      ;SET PROCESSOR PRIORITY 4
831 003306 005077 175476      CLR      @CKV5        ;CLEAR INTERRUPT RETURN STATUS
832 003312 005077 175462      CLR      @CSR
833 003316 012777 000002 175456      MOV      #2, @CSB
834 003324 012777 003366 175454      MOV      #T20A, @CKV   ;SET UP INTERRUPT RETURN VECTOR
835 003332 012777 000101 175440      MOV      #101, @CSR    ;ENABLE INTERRUPT
836 003340 013737 001024 001020      MOV      @DEL1, @TEMP
837 003346 005237 001020      IS:     INC      @TEMP
838 003352 001375      BNE      IS
839 003354 042777 000001 175416      BIC      #1, @CSR
;ERROR, INTERRUPT FAILED TO OCCUR.
840 003362 104000      HLT
841 003364 000420      BR
842 003366 017737 175406 001020      T20A:   MOV      @CSR, @TEMP
843 003374 105737 001020      TSTB    @TEMP
844 003400 100401      BMI     .+4
845 003402 104000      HLT
;DONE NOT SET ON INT.
846 003404 032737 000001 001020      BIT     #1, @TEMP
847 003412 001401      BEQ     .+4
848 003414 104000      HLT
;RUN NOT CLEARED
849 003416 005077 175356      CLR     @CSR
850 003422 012706 000776      MOV     @BUFF, %6
851
852 003426 104400      ;TEST THAT INTERRUPT OCCURS WITH PROCESSOR PRIORITY 5
↑21:   SCOPE
853 003430 012737 000240 177776      MOV     #240, CC      ;SET PROCESSOR PRIORITY 5
854 003436 012777 003512 175342      MOV     #T21A, @CKV   ;SET UP INTERRUPT RETURN STATUS
855 003444 005077 175330      CLR     @CSR
856 003450 012777 000002 175324      MOV     #2, @CSB
857 003456 012777 000101 175314      MOV     #101, @CSR    ;ENABLE INTERRUPT
858 003464 013737 001024 001020      MOV     @DEL1, @TEMP
859 003472 005237 001020      IS:     INC     @TEMP
860 003476 001375      BNE     IS
861 003500 042777 000001 175272      BIC     #1, @CSR
;ERROR, INTERRUPT FAILED TO OCCUR
862 003506 104000      HLT
863 003510 000404      BR
864 003512 005077 175262      T21A:   CLR     @CSR
865 003516 012706 000776      MOV     @BUFF, %6
;RETURN HERE AFTER INTERRUPT
866
867 003522 104400      ;TEST THAT INTERRUPT IS INHIBITED WITH PROCESSOR PRIORITY 6
↑22:   SCOPE
868 003524 012737 000300 177776      MOV     #300, CC      ;SET PROCESSOR PRIORITY 6
869 003532 012777 003602 175246      MOV     #T22A, @CKV   ;SET UP INTERRUPT RETURN
870 003540 005077 175234      CLR     @CSR
871 003544 012777 000002 175230      MOV     #2, @CSB
872 003552 012777 000101 175220      MOV     #101, @CSR    ;INTERRUPT ENABLE
873 003560 013737 001024 001020      MOV     @DEL1, @TEMP
874 003566 005237 001020      IS:     INC     @TEMP
875 003572 001375      BNE     IS
876 003574 005077 175200      CLR     @CSR

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```

877 003600 000406
878 003602 042777 000001 175170 T22A: BR T23
879 003610 104000 HLT #1, @CSR ;ERROR, INT SHOULDN'T HAVE OCCURRED
880 003612 012706 000776 MOV #BUFF, %6
881
882 ;TEST SINGLE INTERRUPT (MODE 0) ON OVERFLOW
883 003616 104400 T23: SCOPE
884 003620 012737 000200 177776 MOV #200, CC ;SET PROCESSOR PRIORITY 4
885 003626 005077 175146 CLR @CSR
886 003632 012777 177776 175142 MOV #-2, @CSB
887 003640 012777 003702 175140 MOV #T23A, @CKV ;SET INTERRUPT RETURN
888 003646 012777 000121 175124 MOV #121, @CSR ;INTERRUPT ENABLE, UP COUNT, 100 KHZ, GO
889 003654 013737 001024 001020 MOV @DEL1, @TEMP
890 003662 062737 000001 001020 T23AA: ADD #1, @TEMP ;WASTE TIME
891 003670 001374 BNE T23AA
892 003672 042777 000001 175100 BIC #1, @CSR
893 003700 104000 HLT ;ERROR, INTERRUPT FAILED TO OCCUR.
894 003702 005077 175072 T23A: CLR @CSR ;RETURN HERE AFTER INTERRUPT.
895 003706 012706 000776 MOV #BUFF, %6 ;RESET STACK
896
897 ;TEST REPEATED INTERRUPT (MODE 1).
898 003712 104400 T24: SCOPE
899 003714 012737 177700 001016 MOV #-100, TEMP1 ;SET UP COUNTER FOR INTER
900 003722 012777 003774 175056 MOV #T24B, @CKV ;SET INTERRUPT RETURN
901 003730 012777 000010 175044 MOV #10, @CSB ;SET UP COUNT SET BUFFER
902 003736 012777 000111 175034 MOV #111, @CSR ;INTERRUPT ENABLE, REPEATED INTERRUPTS, 100 KHZ.
903 003744 013737 001024 001020 T24A: MOV @DEL1, @TEMP
904 003752 062737 000001 001020 ADD #1, @TEMP
905 003760 001374 BNE .-6
906 003762 042777 000001 175010 BIC #1, @CSR
907 003770 104000 HLT ;ERROR, INTERRUPT FAILED TO OCCUR
908 003772 000406 BR T24C
909 003774 022626 T24B: CMP (6)+, (6)+ ;POP STACK
910 003776 005237 001016 INC TEMP1 ;DONE 100 INTERRUPTS?
911 004002 001360 BNE T24A ;NO
912 004004 005077 174770 CLR @CSR ;CLEAR CLOCK
913
914
915
916 ;SYNCHRONIZATION TEST
917 ;NO. 1 FOR
918 ;KW11-P BOARDS THAT
919 ;ARE REV F OR GREATER
920
921
922 004010 104400 T24C: SCOPE
923 004012 005003 CLR %3
924 004014 032777 000020 175022 BIT #20, @SR ;
925 004022 001002 BNE 1$ ;
926 004024 000137 004264 JMP T25 ;
927 004030 012777 010000 174744 1$: MOV #10000, @CSB ;LOAD COUNTER
928 004036 012777 000001 174734 MOV #1, @CSR ;GO COUNT DOWN, 100 KHZ
929 004044 017700 174734 MOV @CTR, %0 ;SAVE CTR
930 004050 020027 010000 CMP %0, #10000 ;DID COUNT INCREASE?
931 004054 101404 BLOS 2$ ;BRANCH IF OK TO 1$
932 004056 010037 001020 MOV %0, @TEMP ;

```

```

933 004062 104000          HLT          : SYNC ERROR
934 004064 000404          BR          T24D       : END TEST
935 004066 005077 174706 2$: CLR          @CSR     : CLR CSR
936 004072 005203          INC          %3       : NO OF TIMES THROUGH PROGRAM DETECTS 2(16)
937 004074 001355          BNE         1$       : 2(16) YET, IF NOT GO BACK TO LOOP 1
938
939
940
941          : SYNCHRONIZATION TEST
942          : NO. 2 FOR KW11-P
943          : BOARDS THAT ARE
944          : REV F OR GREATER
945
946
947 004076 104400          T24D: SCOPE
948 004100 017746 174702    MOV          @CKV, -(%6) : SAVE CLOCK VECTOR
949 004104 012777 000340 002526 MOV          #340, @PSW  : PS=7 STOPS ALL INTRs
950 004112 005037 004246    CLR          TIKTIK    : CLEAR CLOCK COUNTER
951 004116 005037 006632    CLR          CNT       : CLEAR ITERATION COUNT
952 004122 012777 004240 174656 MOV          @CLKSER, @CKV : SETUP INTR SERVICE RTN
953 004130 012777 000300 174652 MOV          #300, @CKVS : SETUP INTR PSW
954 004136 012777 000010 174636 MOV          #10, @CSB  : KW11 COUNT = 10
955 004144 012777 000111 174626 MOV          #111, @CSR : SET TO RUN @100KH
956          : INTR ENABLE & COUNT DOWN
957          : AND REPEAT INTR MODE
958 004152
959 004152 012777 000340 002460 LOOP: MOV          #340, @PSW  : PS=7 STOPS ALL INTRs
960 004160 004737 004250    JSR         PC, TYPE   : 100MS DELAY @PR7
961 004164 005077 002450    CLR          @PSW     : PS=0 ALLOWS INTRs
962 004170 013701 004246    MOV          TIKTIK, R1 : GET CURRENT CLK COUNT
963 004174 004737 004250    JSR         PC, TYPE   : 100MS DELAY @PRO
964 004200 023701 004246    CMP          TIKTIK, R1 : ANY INTRs DURING DELAY?
965 004204 001001          BNE         1$       : IF YES, GO TO 1$
966 004206 104000          HLT
967          : ELSE THERE WAS AN ERROR
968          : CHECK FOR JUMPERS ON THE
969          : KW11-P BOARD NEAR I.C.
970          : LOCATIONS E41 & E51 ON REV F
971          : BOARD & GREATER ONLY
971 004210
972 004210 005237 006632          1$: INC          CNT       :
973 004214 022737 000170 006632 CMP          #120., CNT : ; 120 ITERATIONS?
974 004222 001353          BNE         LOOP     : ; IF NOT, GO BACK TO LOOP
975 004224 012677 174556    MOV          (%6)+, @CKV : ; ELSE RESTORE THE VECTOR
976 004230 005077 174544    CLR          @CSR     : ; CLEAR CONTROL REG
977 004234 000137 004264    JMP          T25      : ; AND GO TO NEXT TEST
978
979 004240          CLKSER:
980 004240 005237 004246    CLKXIT: INC          TIKTIK : ; INC CLK COUNTER
981 004244          CLKXIT: RTI       : ; ELSE EXIT RTN
982 004244 000002
983
984 004246 000000          TIKTIK: 0
985
986 004250 105777 174540          TYPE: TSTB         @TCSR : ; READY TO SEND
987 004254 100375          BPL         TYPE     : ; BR IF NOT
988 004256 110077 174530          MOVB        RO, @TDBR : ; SEND THEM A MESSAGE

```

```

989 004262 000207          RTS    PC
990
991
992
993
994
995
996 004264 104400          :TEST 100 KHZ REPEATABILITY
997 004266 032777 000004 174550  †25:  SCOPE
998 004274 001002          BIT    #4, @SR          :ARE TWO CLK'S PRESENT
999 004276 000137 004740          BNE   3$              :BRANCH IF SW#2 IS UP
1000 004302 005077 174472          JMP   T27             :EXIT IF ONLY ONE CLK
1001 004306 012777 000000 174466  3$:  CLR    @CSR          :SET CTR
1002 004314 012777 000021 174456  MOV   #0, @CSB        :COUNT UP 100KHZ GO
1003 004322 004537 004416          JSR   RS, DELY        :GO TO DELAY SUBROUTINE
1004 004326 105777 174446          TSTB @CSR            :TEST DONE BIT SET
1005 004332 100001          BPL   1$              :
1006 004334 104000          HLT
1007 004336 017737 174442 001020  1$:  MOV   @CTR, @TEMP    :DONE BIT SET TOO SOON
1008 004344 005077 174430          CLR   @CSR            :DONE NOT SET SO SAVE CTR
1009 004350 012777 000000 174424  MOV   #0, @CSB
1010 004356 012777 000021 174414  MOV   #21, @CSR
1011 004364 004537 004416          JSR   RS, DELY
1012 004370 105777 174404          TSTB @CSR
1013 004374 100001          BPL   2$              :
1014 004376 104000          HLT
1015 004400 017737 174400 001016  2$:  MOV   @CTR, @TEMP1   :HERE WE ARE SAVING SEC CNT
1016 004406 004537 004446          JSR   RS, CACL        :GO DETERMINE ACCURACY OF CNT'S
1017 004412 104000          HLT
1018 004414 000432          BR    T25A
1019
1020 004416 005077 002154          DELY: CLR    @CSR1     :DELAY SUBROUTINE
1021 004422 012777 001130 002144  MOV   #1130, @CSB1
1022 004430 012777 000021 002140  MOV   #21, @CSR1
1023 004436 105777 002134          1$:  TSTB @CSR1        :WAIT 600 MIL.
1024 004442 100375          BPL   1$
1025 004444 000205          RTS    RS
1026
1027 004446 013700 001020          CACL: MOV   @TEMP, R0   :COMPARE CTR1 WITH CTR2
1028 004452 013701 001016          MOV   @TEMP1, R1
1029 004456 160001          SUB   R0, R1
1030 004460 100001          BPL   1$
1031 004462 005401          NEG   R1
1032 004464 022701 000005          1$:  CMP   #5, R1         :DIFFERENCE MUST BE LESS THAN 5
1033 004470 002401          BLT   2$
1034 004472 005725          TST   (RS)+
1035 004474 010137 001020          2$:  MOV   R1, TEMP      :UPDATE RETURN
1036 004500 000205          RTS    RS             :DEFRENCE FOR PRINT OUT
1037
1038          :TEST 10 KHZ REPEATABILITY
1039          :THIS TEST IS THE SAME AS T25 EXCEPT IT IS
1040          :FOR 10KHZ.
1041 004502 104400          †25A: SCOPE
1042 004504 005077 174270          CLR   @CSR
1043 004510 012777 000000 174264  MOV   #0, @CSB
1044 004516 012777 000023 174254  MOV   #23, @CSR

```

```

1045 004524 004537 004416
1046 004530 105777 174244
1047 004534 100001
1048 004536 104000
1049 004540 017737 174240 001020 1$:
1050 004546 005077 174226
1051 004552 012777 000000 174222
1052 004560 012777 000023 174212
1053 004566 004537 004416
1054 004572 105777 174202
1055 004576 100001
1056 004600 104000
1057 004602 017737 174176 001016 2$:
1058 004610 004537 004446
1059 004614 104000
1060
1061
1062
1063
1064 004616 104400
1065 004620 005737 006252
1066 004624 100445
1067 004626 005077 174146
1068 004632 012777 000000 174142
1069 004640 012777 000025 174132
1070 004646 004537 004416
1071 004652 105777 174122
1072 004656 100001
1073 004660 104000
1074 004662 017737 174116 001020 1$:
1075 004670 005077 174104
1076 004674 012777 000000 174100
1077 004702 012777 000025 174070
1078 004710 004537 004416
1079 004714 105777 174060
1080 004720 100001
1081 004722 104000
1082 004724 017737 174054 001016 2$:
1083 004732 004537 004446
1084 004736 104000
1085
1086 004740 104400
1087 004742 005077 174032
1088 004746 012737 000340 177776
1089 004754 012777 000002 174020
1090 004762 012777 000111 174010
1091 004770 013737 001024 001020
1092 004776 062737 000001 001020
1093 005004 001374
1094 005006 005777 173766
1095 005012 100404
1096 005014 042777 000001 173756
1097 005022 104000
1098 005024 005077 173750 1$:
1099 005030 005777 173744
1100 005034 100001

```

```

: TEST LINE REPEATABILITY
: THIS TEST IS THE SAME AS T25 EXCEPT IT IS
: FOR LINE FREQ.

```

T26:

```

SCOPE
TST @XORFLG
BMI T27
CLR @CSR
MOV #0,@CSB
MOV #25,@CSR
JSR R5,DELY
TSTB @CSR
BPL 1$
HLT
MOV @CTR,@TEMP
CLR @CSR
MOV #0,@CSB
MOV #25,@CSR
JSR R5,DELY
TSTB @CSR
BPL 2$
HLT
MOV @CTR,@TEMP1
JSR R5,CACL
HLT

```

```

: TEST ERROR (BIT 15) TO SET WHEN INTERRUPT IS NOT SERVICED IN REPEAT MODE

```

T27:

```

SCOPE
CLR @CSR
MOV #340,CC
MOV #2,@CSB
MOV #111,@CSR
MOV @DEL1,@TEMP
ADD #1,@TEMP
BNE -6
TST @CSR
BMI 1$
BIC #1,@CSR
HLT
CLR @CSR
TST @CSR
BPL +4

```

```

: SET PROCESSOR PRIORITY 7
: SET COUNTER FOR FAST INTERRUPTS
: INT EN, REPEATED INT, DOWN COUNT, 100 KHZ. GO

```

```

: ERROR, ERROR (BIT 15) NOT SET

```

| | | | | | | | | | | | |
|------|--------|--------|--------|--------|---------------------------------|-------------|--|--|--|--|---------------------------------|
| 1101 | 005036 | 104000 | | | HLT | | | | | | |
| 1102 | | | | | :TEST BIT 15 IS CLEARED BY INIT | | | | | | :ERR, FAILED TO CLEAR WHEN REF. |
| 1103 | 005040 | 104400 | | | ↑27A: SCOPE | | | | | | |
| 1104 | 005042 | 012737 | 000340 | 177776 | MOV | #340,CC | | | | | |
| 1105 | 005050 | 012777 | 000002 | 173724 | MOV | #2,@CSR | | | | | |
| 1106 | 005056 | 012777 | 000111 | 173714 | MOV | #111,@CSR | | | | | |
| 1107 | 005064 | 013737 | 001024 | 001020 | MOV | @DEL1,@TEMP | | | | | |
| 1108 | 005072 | 062737 | 000001 | 001020 | ADD | #1,@TEMP | | | | | |
| 1109 | 005100 | 001374 | | | BNE | .-6 | | | | | |
| 1110 | 005102 | 005777 | 173672 | | TST | @CSR | | | | | |
| 1111 | 005106 | 100404 | | | BMI | 1\$ | | | | | |
| 1112 | 005110 | 042777 | 000001 | 173662 | BIC | #1,@CSR | | | | | |
| 1113 | 005116 | 104000 | | | HLT | | | | | | :BIT 15 NOT SET |
| 1114 | 005120 | 000005 | | | 1\$: RESET | | | | | | |
| 1115 | 005122 | 005777 | 173652 | | TST | @CSR | | | | | |
| 1116 | 005126 | 100001 | | | BPL | .+4 | | | | | :BIT 15 NOT CLEARED BY RESET |
| 1117 | 005130 | 104000 | | | HLT | | | | | | |
| 1118 | 005132 | 104400 | | | SCOPE | | | | | | |
| 1119 | | | | | | | | | | | |
| 1120 | | | | | :BELL ON PASS COMPLETE | | | | | | |
| 1121 | 005134 | 012777 | 000207 | 173650 | ↑STEND: MOV | #207,@DDBR | | | | | |
| 1122 | 005142 | 105777 | 173646 | | TSTB | @TCSR | | | | | |
| 1123 | 005146 | 100375 | | | BPL | .-4 | | | | | |
| 1124 | 005150 | 012777 | 000000 | 173634 | MOV | #0,@DDBR | | | | | :SEND A NULL CHAR. |
| 1125 | 005156 | 105777 | 173632 | | TSTB | @TCSR | | | | | |
| 1126 | 005162 | 100375 | | | BPL | .-4 | | | | | |
| 1127 | 005164 | 013702 | 000042 | | MOV | @#42,%2 | | | | | |
| 1128 | 005170 | 001405 | | | BEQ | TRPA | | | | | |
| 1129 | 005172 | 000005 | | | RESET | | | | | | |
| 1130 | 005174 | 004712 | | | LOGICAL: JSR | %7,(2) | | | | | |
| 1131 | 005176 | 000240 | | | NOP | | | | | | |
| 1132 | 005200 | 000240 | | | NOP | | | | | | |
| 1133 | 005202 | 000240 | | | NOP | | | | | | |
| 1134 | 005204 | 000137 | 001150 | | TRPA: JMP | BEGIN | | | | | |

```

1135
1136
1137
1138
1139
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1141
1142
1143 005210 012706 000776
1144 005214 004737 011652
1145 005220 013777 001010 173560
1146 005226 012777 000002 173554
1147 005234 012737 005602 000024
1148 005242 000005
1149
1150 005244 012777 141520 173530
1151 005252 012700 177772
1152 005256 012701 177754
1153 005262 012777 000111 173510
1154 005270 000001
1155 005272 005201
1156 005274 001375
1157 005276 105777 173512
1158 005302 100375
1159 005304 012777 000207 173500
1160 005312 005200
1161 005314 001360
1162 005316 042777 000101 173454
1163
1164 005324 012777 011610 173450
1165 005332 012700 177772
1166 005336 012701 177754
1167 005342 012777 000113 173430
1168 005350 000001
1169 005352 005201
1170 005354 001375
1171 005356 105777 173432
1172 005362 100375
1173 005364 012777 000207 173420
1174 005372 005200
1175 005374 001360
1176 005376 042777 000101 173374
1177
1178 005404 005737 006252
1179 005410 100677
1180 005412 012737 001130 005570
1181 005420 032777 000002 173416
1182 005426 001403
1183 005430 012737 000764 005570
1184
1185 005436 013777 005570 173336
1186 005444 012700 177772
1187 005450 012777 000115 173322
1188 005456 000001
1189 005460 105777 173330
1190 005464 100375

.SBTTL          TIMING TEST
:RING TELETYPE BELL AT 10 SECOND INTERVALS USING REPEATED INTERRUPT MODE
:1ST MINUTE = 100 KHZ
:2ND MINUTE = 10 KHZ
:3RD MINUTE = LINE
:4TH MINUTE = EXTERNAL

BEGIN1: MOV      #BUFF,%6
        JSR      %7,SWADJ      ;HAS THIS CPU HAVE A SWITCH REG.?
        MOV      CKVS,@CKV
        MOV      @RTI,@CKVS
        MOV      #PWR2,24      ;INIT POWER FAIL POINTER
        RESET

;100 KHZ
        MOV      #50000.,@CSB  ;INIT COUNT SET BUFFER FOR .5 SECONDS
        MOV      #-6,%0        ;COUNT 6(10 SECOND) INTERVALS
T28:    MOV      #-20,%1        ;COUNT 20(.5 SECOND) INTERVALS
        MOV      #111,@CSR     ;100 KHZ, REPEATED INTERRUPTS, INTERRUPT ENABLE, GO
T28A:   WAIT
        INC      %1            ;DONE 10 SECONDS?
        BNE     T28A          ;NO
        TSTB    @TCSR
        BPL     -4
        MOV      #207,@TDBR
        INC     %0            ;DONE 6 TIMES?
        BNE     T28          ;NO
        BIC     #101,@CSR     ;YES DISABLE INTERRUPTS

;10 KHZ
        MOV      #5000.,@CSB  ;INIT COUNT SET BUFFER FOR .5 SECONDS
        MOV      #-6,%0        ;COUNT 6(10SECOND) INTERVALS
T29:    MOV      #-20,%1        ;COUNT 20(.5 SECOND) INTERVALS
        MOV      #113,@CSR     ;10 KHZ, REPEATED INTERRUPTS, INTERRUPT ENABLE, GO
T29A:   WAIT
        INC      %1            ;DONE 10 SECONDS?
        BNE     T29A          ;NO
        TSTB    @TCSR        ;YES, RING BELL
        BPL     -4
        MOV      #207,@TDBR
        INC     %0            ;DONE 6 TIMES?
        BNE     T29          ;NO
        BIC     #101,@CSR     ;YES, DISABLE INTERRUPTS

;SET UP FOR 10 SECONDS AT LINE FREQ.
        TST     @#XORFLG
        BMI     BEGIN1
        MOV      #600.,LINE
        BIT     #2,@SR
        BEQ     +10
        MOV      #500.,LINE

;LINE
        MOV      LINE,@CSB    ;INITIALZE COUNT SET BUFFER FOR 10 SECONDS
        MOV      #-6,%0        ;COUNT 6 (10 SECOND) INTERVALS
        MOV      #115,@CSR     ;LINE, REPEATED INTERRUPTS, INTERRUPT ENABLE, GO
T30:    WAIT
        TSTB    @TCSR
        BPL     -4

```

| | | | | | | | |
|------|--------|--------|--------|--------|----------------------------------|-------------|---|
| 1191 | 005466 | 012777 | 000207 | 173316 | MOV | #207, @TDBR | :RING BELL |
| 1192 | 005474 | 005200 | | | INC | %0 | :DONE 6 TIMES |
| 1193 | 005476 | 001367 | | | BNE | T30 | :NO |
| 1194 | 005500 | 042777 | 000101 | 173272 | BIC | #101, @CSR | :YES--DISABLE INTERRUPTS |
| 1195 | 005506 | 032777 | 000001 | 173330 | BIT | #1, @SR | : |
| 1196 | 005514 | 001235 | | | BNE | BEGIN1 | : |
| 1197 | | | | | | | : |
| 1198 | 005516 | 013777 | 005570 | 173256 | ;EXTERNAL (LINE FOR MAINTENANCE) | | |
| 1199 | 005524 | 012700 | 177772 | | MOV | LINE, @CSB | :INITIALZE COUNT SET BUFFER FOR 10 SECONDS |
| 1200 | 005530 | 012777 | 000117 | 173242 | MOV | #-6, %0 | :COUNT 6 (10 SECOND) INTERVALS |
| 1201 | 005536 | 000001 | | | MOV | #117, @CSR | :EXT FREQ, REPEATED INTERRUPTS, INTERRUPT ENABLE . GO |
| 1202 | 005540 | 105777 | 173250 | | T31: | WAIT | |
| 1203 | 005544 | 100375 | | | TSTB | @TCSR | |
| 1204 | 005546 | 012777 | 000207 | 173236 | BPL | .-4 | |
| 1205 | 005554 | 005200 | | | MOV | #207, @TDBR | :RING BELL |
| 1206 | 005556 | 001367 | | | INC | %0 | :DONE 6 TIMES |
| 1207 | 005560 | 042777 | 000100 | 173212 | BNE | T31 | :NO |
| 1208 | 005566 | 000610 | | | BIC | #100, @CSR | :YES, DISABLE INTERRUPTS |
| 1209 | 005570 | 001130 | | | BR | BEGIN1 | :REPEAT |
| | | | | | LINE: | 600. | |


```

1210 .SBTTL SUBROUTINES
1211 :POWER FAIL HANDLERS
1212 005572 012737 001150 005646 PWRF1: MOV #BEGIN,PWRRTN
1213 005600 000403 BR PWRDWN
1214 005602 012737 005210 005646 PWRF2: MOV #BEGIN1,PWRRTN
1215 005610 012737 005620 000024 PWRDWN: MOV #PWRUP,24
1216 005616 000000 HALT
1217 005620 012706 000776 PWRUP: MOV #BUFF,%6
1218 005624 005000 CLR %0
1219 005626 005200 INC %0
1220 005630 001376 BNE -2
1221 005632 012702 006472 MOV #MSGPWR,%2
1222 005636 004737 006266 JSR %7, TOP
1223 005642 000177 000000 JMP @PWRRTN
1224 005646 001150 PWRRTN: BEGIN
1225
1226 ;ENTERED WITH SYSTEM TRAP CALL (HLT)
1227 :PRINT PC STATUS REGISTER, COMAND REGISTER, BYTE COUNT, CURRENT ADDRESS, DATA
1228 005650 037727 173170 020000 PRINT: BIT JSR, #20000 ;TEST FOR INHIBIT PRINT OUT
1229 005656 001401 BEQ .+4 ;BRANCH TO PRINT
1230 005660 000002 RTI ;INHIBIT, RETURN TO MAIN STREAM
1231 005662 012702 006370 MOV #MSG1,%2
1232 005666 005737 005764 TST PRINT1
1233 005672 001402 BEQ .+6
1234 005674 012702 006432 MOV #MSG2,%2
1235 005700 004737 006266 JSR %7, TOP ;PRINT ERROR HEADING
1236 005704 005237 005764 INC PRINT1
1237 005710 011602 MOV (6),%2
1238 005712 162702 000002 SUB #2,%2
1239 005716 004737 005766 JSR %7, OCTPRT ;PRINT PC
1240 005722 017702 173052 MOV @CSR,%2
1241 005726 004737 005766 JSR %7, OCTPRT ;PRINT STATUS REGISTER
1242 005732 017702 173046 MOV @CTR,%2
1243 005736 004737 005766 JSR %7, OCTPRT ;PRINT COUNTER
1244 005742 013702 001020 MOV TEMP,%2
1245 005746 004737 005766 JSR %7, OCTPRT ;PRINT TEMP
1246 005752 005777 173066 TST @SR ;CHECK SR FOR HALT SWITCH
1247 005756 100001 BPL .+4
1248 005760 000000 HALT ;HALT ON ERROR UP
1249 005762 000002 RTI ;RETURN TO MAINLINE
1250 005764 000000
1251 PRINT1: 0
1252 005766 012737 000060 006100 :PRINT OCTAL VALUE IN REGISTER2
1253 005774 005702 OCTPRT: MOV #'0,CHAR ;INITIALIZE 1ST NUMBER AS 0
1254 005776 100003 TST %2 ;IS VALUE POSITIVE
1255 006000 012737 000061 006100 BPL OCT1 ;YES PRINT 0
1256 006006 004737 006102 MOV #'1,CHAR ;NO PRINT 1
1257 006012 006102 OCT1: JSR %7, OCTP
1258 006014 006102 ROL %2
1259 006016 012737 177773 006076 MOV #-5, OCT ;COUNT 5 DIGITS
1260 006024 006102 OCT2: ROL %2
1261 006026 006102 ROL %2
1262 006030 006102 ROL %2
1263 006032 010237 006100 MOV %2, CHAR ;SAVE DIGIT
1264 006036 042737 177770 006100 BIC #177770, CHAR ;CLEAR OTHER BITS
1265 006044 052737 000060 006100 BIS #60, CHAR ;MAKE ASCII DIGIT

```

SUBROUTINES

| | | | | | | | |
|------|--------|--------|--------|--------|---------------------------------------|------------------------------|------------------------------------|
| 1266 | 006052 | 006002 | | | ROR | %2 | |
| 1267 | 006054 | 004737 | 006102 | | JSR | %7, OCTP | ;PRINT |
| 1268 | 006060 | 006102 | | | ROL | %2 | |
| 1269 | 006062 | 005237 | 006076 | | INC | OCT | ;+1 TO DIGIT COUNT |
| 1270 | 006066 | 001356 | | | BNE | OCT2 | ;NOT DONE |
| 1271 | 006070 | 004737 | 006120 | | JSR | %7, SP3 | |
| 1272 | 006074 | 000207 | | | RTS | %7 | ;EXIT |
| 1273 | 006076 | 000000 | | | OCT: | 0 | |
| 1274 | 006100 | 000000 | | | CHAR: | 0 | |
| 1275 | 006102 | 105777 | 172706 | | OCTP: | TSTB | @TCSR |
| 1276 | 006106 | 100375 | | | BPL | -4 | ;WAIT FOR READY |
| 1277 | 006110 | 013777 | 006100 | 172674 | MOV | CHAR, @TDBR | ;PRINT |
| 1278 | 006116 | 000207 | | | RTS | %7 | |
| 1279 | | | | | :TYPE 3 | SPACES | |
| 1280 | 006120 | 012702 | 006132 | | SP3: | MOV | #SP3A, %2 |
| 1281 | 006124 | 004737 | 006266 | | JSR | %7, TOP | |
| 1282 | 006130 | 000207 | | | RTS | %7 | |
| 1283 | 006132 | 020057 | 027440 | | SP3A: | .ASCII | ;/ /; |
| 1284 | | | | | | .EVEN | |
| 1285 | | | | | | | |
| 1286 | 006136 | 022606 | | | SCOPEB: | CMP | (%)+, %6 |
| 1287 | 006140 | 012637 | 177776 | | MOV | (%)+, CC | ;REPOSITION THE STACK |
| 1288 | 006144 | 000177 | 000114 | | JMP | @RETURN | ;SCOPE RETURN |
| 1289 | | | | | | | |
| 1290 | | | | | :SCOPE OR/AND | ITERATION LOOP FOR EACH TEST | |
| 1291 | 006150 | 032777 | 040000 | 172666 | SCOPEC: | BIT | #40000, @SR |
| 1292 | 006156 | 001367 | | | BNE | SCOPEB | ;TEST SR FOR SCOPE |
| 1293 | 006160 | 005737 | 006252 | | TST | @XORFLG | ;YES SCOPE |
| 1294 | 006164 | 100011 | | | BPL | 1\$ | |
| 1295 | 006166 | 013746 | 000004 | | MOV | @#4, -(%6) | |
| 1296 | 006172 | 012737 | 006254 | 000004 | MOV | @XORA, @#4 | |
| 1297 | 006200 | 005737 | 177060 | | TST | @#177060 | |
| 1298 | 006204 | 012637 | 000004 | | MOV | (%6)+, @#4 | ;RESTORE STACK |
| 1299 | 006210 | 032777 | 004000 | 172626 | 1\$: | BIT | #4000, @SR |
| 1300 | 006216 | 001007 | | | BNE | SCOPEB | ;NO - TEST FOR ITERATION |
| 1301 | 006220 | 023737 | 006250 | 001022 | CMP | SCOPEF, ICOUNT | ;INHIBIT ITERATION |
| 1302 | 006226 | 001403 | | | BEQ | SCOPEF | ;EXIT - DONE |
| 1303 | 006230 | 005237 | 006250 | | INC | SCOPEF | ;INCREMENT COUNT |
| 1304 | 006234 | 000740 | | | BR | SCOPEB | ;LOOP SOME MORE |
| 1305 | 006236 | 005037 | 006250 | | SCOPEG: | CLR | SCOPEF |
| 1306 | 006242 | 011637 | 006264 | | MOV | @%6, RETURN | ;CLEAR COUNT |
| 1307 | 006246 | 000002 | | | RTI | | ;SAVE SCOPE RETURN POINTER |
| 1308 | 006250 | 000000 | | | SCOPEF: | 0 | ;RETURN INLINE-NEXT TEST |
| 1309 | 006252 | 000000 | | | XORFLG: | 0 | ;COUNT LOCATION FOR ITERATION LOOP |
| 1310 | 006254 | 022626 | | | XORA: | CMP | (%6)+, (%6)+ |
| 1311 | 006256 | 012637 | 000004 | | MOV | (%6)+, @#4 | |
| 1312 | 006262 | 000725 | | | BR | SCOPEB | |
| 1313 | 006264 | 001150 | | | RETURN: | BEGIN | ;ADDRESS OF LAST TEST |
| 1314 | | | | | :MOV ADDRESS OF MESSAGE TO REGISTER 2 | | |
| 1315 | | | | | :THEN JSR %7, TOP | | |
| 1316 | 006266 | 142777 | 000177 | 172520 | TOP: | BICB | #177, @TCSR |
| 1317 | 006274 | 112237 | 006366 | | MOVB | (2)+, EOMK | ;CLR INT FLAG |
| 1318 | 006300 | 121237 | 006366 | | CMPB | @%2, EOMK | ;MOVE IN EOM MARKER |
| 1319 | 006304 | 001001 | | | BNE | .+4 | ;COMPARE FOR EOM |
| 1320 | 006306 | 000207 | | | RTS | %7 | ;NO |
| 1321 | 006310 | 121227 | 000100 | | CMPB | @%2, #'@ | ;YES, EXIT |

| | | | | | | | | |
|------|--------|--------|--------|--------|---------|-------------------------|---|------------------------|
| 1322 | 006314 | 001406 | | | BEQ | TOP2 | | |
| 1323 | 006316 | 105777 | 172472 | | TSTB | @TCSR | | :CK TTY |
| 1324 | 006322 | 100375 | | | BPL | .-4 | | :WAIT FOR DONE |
| 1325 | 006324 | 112277 | 172462 | | MOVB | (2)+,@TDBR | | :MOVE CHARACTER |
| 1326 | 006330 | 000763 | | | BR | TOP1 | | :BRANCH BACK |
| 1327 | 006332 | 105777 | 172456 | | TOP2: | TSTB | @TCSR | |
| 1328 | 006336 | 100375 | | | BPL | .-4 | | |
| 1329 | 006340 | 112777 | 000215 | 172444 | MOVB | #215,@TDBR | | :SEND CARRIAGE RETURN |
| 1330 | 006346 | 105777 | 172442 | | TSTB | @TCSR | | |
| 1331 | 006352 | 100375 | | | BPL | .-4 | | |
| 1332 | 006354 | 112777 | 000212 | 172430 | MOVB | #212,@TDBR | | :SEND LINE FEED |
| 1333 | 006362 | 005202 | | | INC | %2 | | :INCRMTN R2 |
| 1334 | 006364 | 000745 | | | BR | TOP1 | | :NO EOM, SO LOOP |
| 1335 | 006366 | 000 | | | EOMK: | .BYTE | 0 | |
| 1336 | | 006370 | | | | .EVEN | | |
| 1337 | 006370 | 040057 | 020040 | 041520 | MSG1: | .ASCII | ;/@ PC | STATUS COUNTER TEMP@/; |
| 1338 | 006376 | 020040 | 020040 | 052123 | | | | |
| 1339 | 006404 | 052101 | 051525 | 020040 | | | | |
| 1340 | 006412 | 047503 | 047125 | 042524 | | | | |
| 1341 | 006420 | 020122 | 052040 | 046505 | | | | |
| 1342 | 006426 | 040120 | 057 | | | | | |
| 1343 | | 006432 | | | | .EVEN | | |
| 1344 | 006432 | 040057 | 057 | | MSG2: | .ASCII | ;/@/; | |
| 1345 | | 006436 | | | | .EVEN | | |
| 1346 | 006436 | 040057 | 055103 | 053513 | MSG3: | .ASCII | ;/@CZKWB1 KW11-P RT CLK TST@/; | |
| 1347 | 006444 | 044502 | 045440 | 030527 | | | | |
| 1348 | 006452 | 026461 | 020120 | 052122 | | | | |
| 1349 | 006460 | 041440 | 045514 | 052040 | | | | |
| 1350 | 006466 | 052123 | 027500 | | | | | |
| 1351 | | | | | | .EVEN | | |
| 1352 | 006472 | 040057 | 042522 | 052123 | MSGPWR: | .ASCII | ;/@RESTARTING AFTER A POWER FAILURE@@/; | |
| 1353 | 006500 | 051101 | 044524 | 043516 | | | | |
| 1354 | 006506 | 040440 | 052106 | 051105 | | | | |
| 1355 | 006514 | 040440 | 050040 | 053517 | | | | |
| 1356 | 006522 | 051105 | 043040 | 044501 | | | | |
| 1357 | 006530 | 052514 | 042522 | 040100 | | | | |
| 1358 | 006536 | 057 | | | | | | |
| 1359 | | 006540 | | | | .EVEN | | |
| 1360 | 006540 | 040057 | 047531 | 020125 | XORM: | .ASCII | ;/@YOU ARE ON AN XOR TESTER@/; | |
| 1361 | 006546 | 051101 | 020105 | 047117 | | | | |
| 1362 | 006554 | 040440 | 020116 | 047530 | | | | |
| 1363 | 006562 | 020122 | 042524 | 052123 | | | | |
| 1364 | 006570 | 051105 | 027500 | | | | | |
| 1365 | | | | | | .EVEN | | |
| 1366 | | | | | | :TIMER FOR KW11-P CLOCK | | |
| 1367 | | | | | | | | |
| 1368 | 006574 | 172562 | | | CSB1: | 172562 | | |
| 1369 | 006576 | 172560 | | | CSR1: | 172560 | | |
| 1370 | 006600 | 172564 | | | CTR1: | 172564 | | |
| 1371 | 006602 | 000504 | | | CKV1: | 504 | | |
| 1372 | 006604 | 000506 | | | CKV51: | 506 | | |
| 1373 | 006606 | 000000 | | | CLKFLG: | 0 | | |
| 1374 | 006610 | 000000 | | | INTFLG: | 0 | | |
| 1375 | 006612 | 177566 | | | PDBR: | 177566 | | |
| 1376 | 006614 | 177564 | | | PCSR: | 177564 | | |
| 1377 | 006616 | 000064 | | | PVEC: | 64 | | |

```

1378 006620 000066
1379 006622 177562
1380 006624 177560
1381 006626 000060
1382 006630 000062
1383 006632 000000
1384 006634 000000
1385 006636 000000
1386      000211
1387      000224
1388 006640 177776
1389 006642 000000
1390 006644 000000
1391 006646 000000
1392 006650 000000
1393 006652 000000
1394 006654 000000
1395 006656 000000
1396 006660 000000
1397 006662 000000
1398 006664 000000
1399 006666 000000
1400 006670 000000
1401 006672 000000
1402 006674 000000
1403 006676 000000
1404 006700 000000
1405 006702 000000
1406 006704      000
1407 006705      000
1408 006706      000
1409 006707      000
1410 006710      000
1411 006711      000
1412 006712      000
1413      006714
1414
1415
1416
1417

```

```

PVECS: 66
KDBR: 177562
KCSR: 177560
KVEC: 60
KVECS: 62
CNT: 0
CNT1: 0
CNTB: 0
CTRLI=211
CTRLT=224
PSW: 177776
HRS1: 0
HRS2: 0
MIN1: 0
MIN2: 0
SEC1: 0
SEC2: 0
LST: 0
MST: 0
HRS1A: 0
HRS2A: 0
MIN1A: 0
MIN2A: 0
SEC1A: 0
SEC2A: 0
LSTA: 0
MSTA: 0
TMPSWR: 0
BYT1: .BYTE 0
BYT2: .BYTE 0
BYT3: .BYTE 0
BYT4: .BYTE 0
BYT5: .BYTE 0
BYT6: .BYTE 0
BYT7: .BYTE 0
.EVEN

```

```

;TEMP LOC FOR SOFT-SWR CONTENTS
;LOC FOR 1ST # INPUT VIA TTY
; " " 2ND " " " "
; " " 3RD " " " "
; " " 4TH " " " "
; " " 5TH " " " "
; " " 6TH " " " "
; " " 7TH " " " "

```

```

1418 006714 012706 000776
1419 006720 004737 011652
1420 006724 005077 177710
1421 006730 012737 000000 007674
1422 006736 012737 000131 007702
1423 006744 012700 010356
1424 006750 012701 010376
1425 006754 004537 007234
1426 006760 012737 000043 010506
1427 006766 012737 001217 010536
1428 006774 000137 007250
1429
1430 007000 012706 000776
1431 007004 004737 011652
1432 007010 005077 177624
1433 007014 012737 164217 007674

```

```

;K100HZ: MOV #BUFF,%6
;JSR %7,SWADJ ;HAS THIS CPU HAVE A SWITCH REG.?
;CLR @PSW
;MOV #0,CLK+2 ;:100KHZ
;MOV #131,CLK1+2
;MOV #TABL,%0
;MOV #TABL1,%1
;JSR %5,@#MOVE
;MOV #35,CLK3+2 ;:LEAST VALUE
;MOV #655,CLK4+2 ;:MOST VALUE
;JMP @#INIT

;K10HZ: MOV #BUFF,%6
;JSR %7,SWADJ ;HAS THIS CPU HAVE A SWITCH REG.?
;CLR @PSW
;MOV #-13561,CLK+2 ;:10KHZ

```

| | | | | | | |
|------|--------|--------|--------|--------|-----|-------------|
| 1434 | 007022 | 012737 | 000133 | 007702 | MOV | #133,CLK1+2 |
| 1435 | 007030 | 012700 | 010356 | | MOV | #TABL,%0 |
| 1436 | 007034 | 012701 | 010416 | | MOV | #TABL,%1 |
| 1437 | 007040 | 004537 | 007234 | | JSR | %5,%#MOVE |
| 1438 | 007044 | 012737 | 000000 | 010506 | MOV | #0,CLK3+2 |

CZKWBHD KW11-P RT CLK TST
CZKWB1.P11 30-JAN-78 09:34

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SUBROUTINES

SEQ 0029

1439 007052 012737 001130 010536
1440 007060 000137 007250

MOV #600, CLK4+2
JMP @INIT

| | | | |
|------|--------|--------|--------|
| 1441 | | | |
| 1442 | 007064 | 012706 | 000776 |
| 1443 | 007070 | 004737 | 011652 |
| 1444 | 007074 | 005077 | 177540 |

H602: MOV #BUFF,%6
JSR %7,SWADJ
CLR @PSW

:HAS THIS CPU HAVE A SWITCH REG.?
:

F03

CZKWBHD KW11-P RT CLK TST
CZKWB1.F11 30-JAN-78 09:34

MACY11 30A(1052) 30-JAN-78 09:35 PAGE 31
SUBROUTINES

SEQ 0031

1445 007100 012737 177733 007674

MOV # -45, CLK+2

:60HZ

G03

CZKWBMO KW11-P RT CLK TST
CZKWB1.P11 30-JAN-78 09:34

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SUBROUTINES

SEQ 0032

1446 007106 012737 000135 007702

MOV #135,CLK1+2

```

1447 007114 012700 010356      MOV      #TABL,%0
1448 007120 012701 010436      MOV      #TABL3,%1
1449 007124 004537 007234      JSR      %5,@#MOVE
1450 007130 012737 000000 010506      MOV      #00,CLK3+2
1451 007136 012737 001130 010536      MOV      #600,CLK4+2
1452 007144 000137 007250      JMP      @#INIT
1453
1454 007150 012706 000776      H50Z:    MOV      #BUFF,%6
1455 007154 004737 011652      JSR      %7,SWADJ      ;HAS THIS CPU HAVE A SWITCH REG.?
1456 007160 005077 177454      CLR      @PSW          ;50HZ
1457 007164 012737 177742 007674      MOV      #-36,CLK+2
1458 007172 012737 000135 007702      MOV      #135,CLK1+2
1459 007200 012700 010356      MOV      #TABL,%0
1460 007204 012701 010456      MOV      #TABL4,%1
1461 007210 004537 007234      JSR      %5,@#MOVE
1462 007214 012737 000000 010506      MOV      #0,CLK3+2
1463 007222 012737 001104 010536      MOV      #580,CLK4+2
1464 007230 000137 007250      JMP      @#INIT
1465
1466 007234 012702 177771      MOVE:    MOV      #-7,%2
1467 007240 012120 1$:          MOV      (%1)+,(%0)+
1468 007242 005202      INC      %2
1469 007244 001375      BNE      1$
1470 007246 000205      RTS      %5
1471
1472 007250 013737 005572 000024  INIT:    MOV      PWRFL,24
1473 007256 012706 000776      MOV      #BUFF,%6      ;INITIALIZE
1474 007262 005037 006656      CLR      @#LST
1475 007266 005037 006660      CLR      @#MST
1476 007272 012737 000060 006642      MOV      #60,@#HRS1
1477 007300 012737 000060 006644      MOV      #60,@#HRS2
1478 007306 012737 000060 006646      MOV      #60,@#MIN1
1479 007314 012737 000060 006650      MOV      #60,@#MIN2
1480 007322 012737 000060 006652      MOV      #60,@#SEC1
1481 007330 012737 000060 006654      MOV      #60,@#SEC2
1482 007336 012777 010476 171442      MOV      #CLKI,@CKV
1483 007344 012777 000340 171436      MOV      #340,@CKVS
1484 007352 012777 007560 177246      MOV      #KINTR,@KVEC
1485 007360 012777 000200 177242      MOV      #200,@KVECS
1486 007366 012777 000200 177224      MOV      #200,@PVECS
1487 007374 012777 000100 177222      MOV      #100,@KCSR
1488 007402 005037 006606      CLR      @#CLKFLG
1489 007406 005037 006610      CLR      @#INTFLG
1490 007412 005077 171362      START:  CLR      @CSR
1491 007416 005077 171360      CLR      @CSB
1492 007422 032777 000002 171414  WAITA:  BIT      #2,@SR
1493 007430 001401      BEQ      CLKON      ;WAIT LOOP, SW 1 CAUSE WAIT
1494 007432 000001      WAITB:  WAIT
1495 007434 032777 000001 171402  CLKON:  BIT      #1,@SR
1496 007442 001432      BEQ      3$          ;SW 0 TURNS ON CLK2
1497 007444 032777 000004 171372  BIT      #4,@SR
1498 007452 001426      BEQ      3$          ;SW 2 DETERMINES PRESENCE OF CLOCK 2
1499 007454 005737 006606      TST      @#CLKFLG
1500 007460 001360      BNE      WAITA      ;CLKFLG ALLOW CLK 2 TO BE TURNED ON
1501 007462 005077 177106      CLR      @CSB1
1502 007466 012777 007762 177106      MOV      #KOUT,@CKV1

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1503 007474 012777 000200 177102      MOV      #200,@CKVS1
1504 007502 012737 177777 006606      MOV      #-1,@CLKFLG
1505 007510 012777 141521 177056      MOV      #141521,@CSB1
1506 007516 012777 000113 177052      MOV      #113,@CSR1      ;TURN ON CLK 2
1507 007524 000137 007432      JMP      WAITB
1508 007530 005037 006606      3$:     CLR      @CLKFLG      ;CLEAR CLK 2 IF PRESENT
1509 007534 032777 000004 171302      BIT      #4,@SR
1510 007542 001404      BEQ     4$
1511 007544 005077 177026      CLR      @CSR1
1512 007550 005077 177020      CLR      @CSB1
1513 007554 000137 007422      4$:     JMP      WAITA
1514
1515 007560 017701 177036      KINTR:  MOV      @KDBR,%1      ;KEYBOARD INTERRUPT HANDLER
1516 007564 042701 177600      BIC     #177600,%1      ;STRIP JUNK
1517 007570 022701 000007      CMP     #7,%1      ;IS CHAR A ↑G(CONTROL-G)?
1518 007574 001557      BEQ     CNCSWR      ;IF YES,GO TO CNCSWR
1519 007576 022701 000011      CMP     #11,%1      ;IS IT A CNTRL I ?
1520 007602 001404      BEQ     KIN
1521 007604 022701 000024      CMP     #24,%1      ;IS IT A CNTRL T ?
1522 007610 001464      BEQ     KOUT
1523 007612 000002      RTI
1524
1525
1526 007614 005077 171160      KIN:    CLR      @CSR      ;HANDLER FOR CTRL I
1527 007620 005077 171156      CLR      @CSB      ;SETUP TIME OF DAY
1528 007624 012737 177772 006632      MOV      #-6,@CNT
1529 007632 012737 006642 006634      MOV      #HRS1,@CNT1      ;INPUT
1530 007640 005037 006656      CLR      LST
1531 007644 005037 006660      CLR      MST
1532 007650 012777 007710 176750      MOV      #KINI,@KVEC
1533 007656 000002      RTI
1534
1535 007660 012777 007560 176740      KINI2:  MOV      #KINTR,@KVEC      ;AWAIT A CHAR TO START
1536 007666 017701 176730      MOV      @KDBR,%1
1537 007672 012777 000000 171102      CLK:    MOV      #0,@CSB      ;CLK 1
1538 007700 012777 000131 171072      CLK1:   MOV      #131,@CSR
1539 007706 000002      RTI
1540
1541 007710 013704 006634      KINI:   MOV      @CNT1,%4      ;STORE TIME OF DAY
1542 007714 017701 176702      MOV      @KDBR,%1
1543 007720 042701 000300      BIC     #300,%1
1544 007724 010124      MOV     %1,(%4)+
1545 007726 010437 006634      MOV     %4,@CNT1
1546 007732 005237 006632      INC     @CNT
1547 007736 001003      BNE     1$
1548 007740 012777 007660 176660      MOV     #KINI2,@KVEC
1549 007746 000002      1$:    RTI
1550
1551 007750 017737 176646 007760      HOLDIT:MOV      @KDBR,@HOLD      ;DUMMY INTERRUPT SERVICE ROUTINE
1552 007756 000002      RTI
1553
1554 007760 000000      HOLD:   0
1555
1556 007762 005037 006610      KOUT:   CLR      @INTFLG      ;INPUT HANDLER FOR CTRL T
1557 007766 012777 007750 176632      MOV     #HOLDIT,@KVEC      ;SET DUMMY VECTOR
1558 007774 012700 006642      MOV     #HRS1,%0      ;GET TIME OF DAY INTO

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1559 010000 012703 006662      MOV      #HRS1A,%3      ;WORK AREA
1560 010004 012704 177770      MOV      #-10,%4
1561 010010 012023      1$:     MOV      (%0)+,(%3)+
1562 010012 005204      INC      %4
1563 010014 001375      BNE     1$
1564 010016 017701 170762      MOV      @CTR,%1
1565 010022 005737 006610      TST     @INTFLG      ;SEE IF CLK HAS INTERRUPTED IN THIS TIME
1566 010026 001355      BNE     KOUT         ;CALC VALUE OF CTR
1567 010030 005737 007674      TST     @CLK+2      ;IS CLOCK RUNNING AT 100KHZ ?
1568 010034 001416      BEQ     2$
1569 010036 163701 007674      SUB     @CLK+2,%1    ;SUB INIT VALUE
1570 010042 006301      ASL     %1
1571 010044 006301      ASL     %1
1572 010046 023727 007674 164217      CMP     @CLK+2,#-13561 ;IS CLOCK RUNNING AT 10KHZ ?
1573 010054 001405      BEQ     3$
1574 010056 000301      10$:    SWAB     %1
1575 010060 023727 007674 177742      CMP     @CLK+2,#-36   ;IS CLOCK RUNNING AT 50HZ ?
1576 010066 001001      BNE     2$
1577 010070 006301      3$:     ASL     %1
1578 010072 005000      2$:     CLR     %0
1579 010074 005003      CLR     %3
1580 010076 012704 010356      5$:     MOV     #TABL,%4
1581 010102 005701      6$:     TST     %1
1582 010104 100001      BPL     4$
1583 010106 061403      ADD     @%4,%3
1584 010110 006301      4$:     ASL     %1
1585 010112 005724      TST     (%4)+
1586 010114 005200      INC     %0
1587 010116 022700 000007      CMP     #7,%0
1588 010122 001367      BNE     6$
1589 010124 060337 006700      ADD     %3,@MSTA     ;ADD VALUE OF CTR TO MST
1590 010130 000137 010772      JMP     @CLK2
1591 010134      CNGSWR:
1592 010134 010246      MOV     %2,-(6)      ;SAVE R2
1593 010136 010346      MOV     %3,-(6)      ;SAVE R3
1594 010140      SETBYT:
1595 010140 005037 006702      CLR     TMPSWR      ;CLEAR TEMP SWR
1596 010144 005003      CLR     %3          ;CLEAR R3
1597 010146 004737 010324      JSR     PC,CRLF     ;PRINT <CR><LF>
1598 010152 012702 006704      MOV     #BYT1,%2    ;INIT R2 TO 1ST BYTE LOC
1599 010156      CKCSR:
1600 010156 105777 176442      TSTB   @KCSR        ;IS CHAR TYPED?
1601 010162 100375      BPL     CKCSR        ;IF NOT WAIT
1602 010164 017701 176432      MOV     @KDBR,%1    ;ELSE MOVE THE CHAR TO R1
1603 010170 042701 177600      BIC     #177600,%1  ;STRIP JUNK
1604 010174      5$:
1605 010174 105777 176414      TSTB   @PCSR
1606 010200 100375      BPL     5$
1607 010202 010177 176404      MOV     %1,@PDBR
1608 010206 122701 000025      CMPB   #25,%1      ;IS CHAR ↑U (CONTROL-U)?
1609 010212 001752      BEQ     SETBYT      ;IF YES START OVER
1610 010214 122701 000015      CMPB   #15,%1      ;ELSE IS IT <CR>?
1611 010220 001412      BEQ     SWDONE      ;IF EQUAL,GO TO SWDONE
1612 010222 122701 000012      CMPB   #12,%1      ;IS IT <LF>?
1613 010226 001407      BEQ     SWDONE      ;IF EQUAL,GO TO SWDONE
1614 010230 005203      INC     %3          ;INDICATE A CHAR INPUTTED

```

| | | | | | | | |
|------|--------|--------|--------|---------|------|--------------|------------------------------------|
| 1615 | 010232 | 042701 | 177770 | | BIC | #177770,%1 | : LEAVE ONLY BINARY # IN R1 |
| 1616 | 010236 | 110122 | | | MOVB | %1,(2)+ | : MOVE # TO PROPER BYTE LOC |
| 1617 | 010240 | 022702 | 006712 | | CMP | #BYT7,%2 | : IS R2 PAST BYT6 ADDR? |
| 1618 | 010244 | 001344 | | | BNE | CKCSR | : IF NOT, GO BACK FOR ANOTHER CHAR |
| 1619 | 010246 | | | SWDONE: | | | |
| 1620 | 010246 | 005703 | | | TST | %3 | : WAS A CHAR TYPED? |
| 1621 | 010250 | 001420 | | | BEQ | 30\$ | : IF NOT, EXIT |
| 1622 | 010252 | 012703 | 006704 | | MOV | #BYT1,%3 | : INIT R3 TO 1ST BYTE ADDR |
| 1623 | 010256 | | | 10\$: | | | |
| 1624 | 010256 | 152337 | 006702 | | BISB | (3)+,TMP\$WR | : SET LOW 3 BITS OF TMP\$WR |
| 1625 | 010262 | 020302 | | | CMP | %3,%2 | : IS R3 EQUAL BYTE ADDR IN R2? |
| 1626 | 010264 | 001407 | | | BEQ | 20\$ | : IF YES, EXIT |
| 1627 | 010266 | 006137 | 006702 | | ROL | TMP\$WR | : ELSE |
| 1628 | 010272 | 006137 | 006702 | | ROL | TMP\$WR | : SHIFT |
| 1629 | 010276 | 006137 | 006702 | | ROL | TMP\$WR | : NEXT 3 BITS UP |
| 1630 | 010302 | 000765 | | | BR | 10\$ | : AND GO GET ANOTHER # |
| 1631 | 010304 | | | 20\$: | | | |
| 1632 | 010304 | 013777 | 006702 | 170532 | MOV | TMP\$WR,%SR | : SET UP NEW \$WR |
| 1633 | 010312 | | | 30\$: | | | |
| 1634 | 010312 | 012603 | | | MOV | (6)+,%3 | : RESTORE R3 |
| 1635 | 010314 | 012602 | | | MOV | (6)+,%2 | : RESTORE R2 |
| 1636 | 010316 | 004737 | 010324 | | JSR | PC,CRLF | : PRINT <CR><LF> |
| 1637 | 010322 | 000002 | | | RTI | | |
| 1638 | | | | | | | |
| 1639 | 010324 | | | CRLF: | | | |
| 1640 | 010324 | 105777 | 176264 | | TSTB | %PCSR | : IS TTY READY? |
| 1641 | 010330 | 100375 | | | BPL | CRLF | : IF NOT, WAIT |
| 1642 | 010332 | 012777 | 000215 | 176252 | MOV | #215,%PDBR | : ELSE TYPE <CR> |
| 1643 | 010340 | | | 10\$: | | | |
| 1644 | 010340 | 105777 | 176250 | | TSTB | %PCSR | : IS TTY READY? |
| 1645 | 010344 | 100375 | | | BPL | 10\$ | : IF NOT, WAIT |
| 1646 | 010346 | 012777 | 000212 | 176236 | MOV | #212,%PDBR | : ELSE TYPE <LF> |
| 1647 | 010354 | 000207 | | | RTS | PC | |
| 1648 | | | | | | | |
| 1649 | 010356 | 000510 | | TABL: | 328. | | : TABLE FOR WORK AREA |
| 1650 | 010360 | 000244 | | | 164. | | |
| 1651 | 010362 | 000122 | | | 82. | | |
| 1652 | 010364 | 000051 | | | 41. | | |
| 1653 | 010366 | 000024 | | | 20. | | |
| 1654 | 010370 | 000012 | | | 10. | | |
| 1655 | 010372 | 000005 | | | 5. | | |
| 1656 | 010374 | 000003 | | | 3. | | |
| 1657 | | | | | | | |
| 1658 | 010376 | 000510 | | TABL1: | 328. | | : 100KHZ TIME TABLE |
| 1659 | 010400 | 000244 | | | 164. | | |
| 1660 | 010402 | 000122 | | | 82. | | |
| 1661 | 010404 | 000051 | | | 41. | | |
| 1662 | 010406 | 000024 | | | 20. | | |
| 1663 | 010410 | 000012 | | | 10. | | |
| 1664 | 010412 | 000005 | | | 5. | | |
| 1665 | 010414 | 000003 | | | 3. | | |
| 1666 | | | | | | | |
| 1667 | 010416 | 000632 | | TABL2: | 410. | | : 10KHZ TIME TABLE |
| 1668 | 010420 | 000315 | | | 205. | | |
| 1669 | 010422 | 000146 | | | 102. | | |
| 1670 | 010424 | 000063 | | | 51. | | |

| | | | |
|------|--------|--------|-------------|
| 1671 | 010426 | 000032 | 26. |
| 1672 | 010430 | 000015 | 13. |
| 1673 | 010432 | 000006 | 6. |
| 1674 | 010434 | 000003 | 3. |
| 1675 | | | |
| 1676 | 010436 | 001025 | TABL3: 533. |
| 1677 | 010440 | 000413 | 267. |
| 1678 | 010442 | 000205 | 133. |
| 1679 | 010444 | 000103 | 67. |
| 1680 | 010446 | 000041 | 33. |
| 1681 | 010450 | 000021 | 17. |
| 1682 | 010452 | 000000 | 0. |
| 1683 | 010454 | 000000 | 0. |
| 1684 | | | |
| 1685 | 010456 | 000500 | TABL4: 320. |
| 1686 | 010460 | 000240 | 160. |
| 1687 | 010462 | 000120 | 80. |
| 1688 | 010464 | 000050 | 40. |
| 1689 | 010466 | 000024 | 20. |
| 1690 | 010470 | 000000 | 0. |
| 1691 | 010472 | 000000 | 0. |
| 1692 | 010474 | 000000 | 0. |

;60HZ TIME TABLE

;50HZ TIME TABLE

; THIS ROUTINE KEEPS THE 24 HOUR
; TIME OF DAY

| | | | | |
|------|--------|--------|--------|--------|
| 1697 | 010476 | 012737 | 177777 | 006610 |
| 1698 | 010504 | 062737 | 000044 | 006656 |
| 1699 | 010512 | 022737 | 000144 | 006656 |
| 1700 | 010520 | 003005 | | |
| 1701 | 010522 | 162737 | 000144 | 006656 |
| 1702 | 010530 | 005237 | 006660 | |
| 1703 | 010534 | 062737 | 001217 | 006660 |
| 1704 | 010542 | 022737 | 001750 | 006660 |
| 1705 | 010550 | 003011 | | |
| 1706 | 010552 | 162737 | 001750 | 006660 |
| 1707 | 010560 | 005237 | 006654 | |
| 1708 | 010564 | 022737 | 000072 | 006654 |
| 1709 | 010572 | 001401 | | |
| 1710 | 010574 | 000002 | | |
| 1711 | 010576 | 012737 | 000060 | 006654 |
| 1712 | 010604 | 005237 | 006652 | |
| 1713 | 010610 | 022737 | 000066 | 006652 |
| 1714 | 010616 | 001401 | | |
| 1715 | 010620 | 000002 | | |
| 1716 | 010622 | 012737 | 000060 | 006652 |
| 1717 | 010630 | 005237 | 006650 | |
| 1718 | 010634 | 022737 | 000072 | 006650 |
| 1719 | 010642 | 001401 | | |
| 1720 | 010644 | 000002 | | |
| 1721 | 010646 | 012737 | 000060 | 006650 |
| 1722 | 010654 | 005237 | 006646 | |
| 1723 | 010660 | 022737 | 000066 | 006646 |
| 1724 | 010666 | 001401 | | |
| 1725 | 010670 | 000002 | | |
| 1726 | 010672 | 012737 | 000060 | 006646 |

2\$:

```

CLK1:  MOV    #-1, @INTFLG      ; CLOCK INTERRUPT SERVICE ROUTINE
CLK3:  ADD    #36, @LST          ; ADD LSB TO LST
      CMP    #100, @LST         ; DID IT OVER FLOW
      BGT   CLK4
      SUB   #100, @LST          ; YES
      INC   @MST                ; INC MST
CLK4:  ADD    #655, @MST         ; ADD MSB TO MST
      CMP    #1000, @MST        ; DID IT OVER FLOW
      BGT   2$
      SUB   #1000, @MST         ; YES
      INC   @SEC2               ; INC SECOND
      CMP    #72, @SEC2         ; HAS 10 SECONDS ELAPSED
      BEQ   .+4
      RTI
      MOV    #60, @SEC2         ; YES
      INC   @SEC1               ; INC MSB OF SECOND
      CMP    #66, @SEC1         ; HAS 60 MIN ELAPSED
      BEQ   .+4
      RTI
      MOV    #60, @SEC1         ; YES
      INC   @MIN2               ; INC LSB OF MIN
      CMP    #72, @MIN2        ; HAS 10 MIN ELAPSED
      BEQ   .+4
      RTI
      MOV    #60, @MIN2
      INC   @MIN1               ; INC MSB OF MIN
      CMP    #66, @MIN1        ; HAS 60 MIN ELAPSED
      BEQ   .+4
      RTI
      MOV    #60, @MIN1

```

```

1727 010700 005237 006644      INC      2#HRS2      ; INC LSB OF HOURS
1728 010704 022737 000064 006644      CMP      #64,2#HRS2 ; IS LSB A 4
1729 010712 001014      BNE      NEWTM
1730 010714 022737 000062 006642      CMP      #62,2#HRS1 ; IF YES, IS MSB A 2
1731 010722 001401      BEQ      .+4
1732 010724 000002      RTI
1733 010726 012737 000060 006642      MOV      #60,2#HRS1 ; IF 24 HOURS RESET
1734 010734 012737 000060 006644      MOV      #60,2#HRS2 ; LSB AND MSB OF HOURS
1735 010742 000002      RTI
1736 010744 022737 000072 006644 NEWTM:  CMP      #72,2#HRS2 ; IF NOT 4 IS IT 10 HOURS
1737 010752 001401      BEQ      .+4
1738 010754 000002      RTI
1739 010756 005237 006642      INC      2#HRS1      ; YES INC MSB OF HOURS
1740 010762 012737 000060 006644      MOV      #60,2#HRS2
1741 010770 000002      RTI
1742
1743
1744
1745
1746 010772 022737 001750 006700 CLK2:  CMP      #1000.,2#MSTA ; THIS ROUTINE IS THE WORK
1747 011000 003011      BGT      2$
1748 011002 162737 001750 006700      SUB      #1000.,2#MSTA ; AREA ROUTINE AND IS THE
1749 011010 005237 006674      INC      2#SEC2A      ; SAME AS INTERRUPT HANDLER
1750 011014 022737 000072 006674      CMP      #72,2#SEC2A ; SERVICE ROUTINE
1751 011022 001401      BEQ      .+4
1752 011024 000475      BR       2$:
1753 011026 012737 000060 006674      MOV      #60,2#SEC2A
1754 011034 005237 006672      INC      2#SEC1A
1755 011040 022737 000066 006672      CMP      #66,2#SEC1A
1756 011046 001401      BEQ      .+4
1757 011050 000463      BR       2$:
1758 011052 012737 000060 006672      MOV      #60,2#SEC1A
1759 011060 005237 006670      INC      2#MIN2A
1760 011064 022737 000072 006670      CMP      #72,2#MIN2A
1761 011072 001401      BEQ      .+4
1762 011074 000451      BR       2$:
1763 011076 012737 000060 006670      MOV      #60,2#MIN2A
1764 011104 005237 006666      INC      2#MIN1A
1765 011110 022737 000066 006666      CMP      #66,2#MIN1A
1766 011116 001401      BEQ      .+4
1767 011120 000437      BR       2$:
1768 011122 012737 000060 006666      MOV      #60,2#MIN1A
1769 011130 005237 006664      INC      HRS2A
1770 011134 022737 000064 006664      CMP      #64,2#HRS2A
1771 011142 001014      BNE      NEWT
1772 011144 022737 000062 006662      CMP      #62,2#HRS1A
1773 011152 001401      BEQ      .+4
1774 011154 000421      BR       2$:
1775 011156 012737 000060 006662      MOV      #60,2#HRS1A
1776 011164 012737 000060 006664      MOV      #60,2#HRS2A
1777 011172 000412      BR       2$:
1778 011174 022737 000072 006664 NEWT:  CMP      #72,2#HRS2A
1779 011202 001401      BEQ      .+4
1780 011204 000405      BR       2$:
1781 011206 005237 006662      INC      2#HRS1A
1782 011212 012737 000060 006664      MOV      #60,2#HRS2A

```

```

1783 011220 012777 011266 175370 END1A: MOV      #CR, @PVEC      ;SET UP FOR PRINTER OUTPUT
1784 011226 012737 177776 006636 MOV      #-2, @CNTB
1785 011234 012737 006662 006634 MOV      #HRS1A, @CNT1
1786 011242 012737 177767 006632 MOV      #-11, @CNT
1787 011250 012777 000000 175334 MOV      #0, @PDBR
1788 011256 012777 000100 175330 MOV      #100, @PCSR
1789 011264 000002 RTI
1790
1791
1792 011266 012777 011304 175322 CR:      MOV      #LF, @PVEC      ;OUTPUT CR
1793 011274 012777 000215 175310 MOV      #215, @PDBR
1794 011302 000002 RTI
1795
1796 011304 012777 011322 175304 LF:      MOV      #PINTR, @PVEC ;OUTPUT LF
1797 011312 012777 000212 175272 MOV      #212, @PDBR
1798 011320 000002 RTI
1799 011322 005237 006632 PINTR:  INC      @CNT      ;PRINT TWO DIGITS FOLLOWED
1800 011326 001414 BEQ      DONE      ;BY COLON UNTIL TIME OF
1801 011330 005737 006636 TST      CNTB      ;DAY IS PRINTED
1802 011334 001420 BEQ      COLON
1803 011336 013704 006634 MOV      @CNT1, %4
1804 011342 012477 175244 MOV      (%4)+, @PDBR
1805 011346 010437 006634 MOV      %4, @CNT1
1806 011352 005237 006636 INC      @CNTB
1807 011356 000002 RTI
1808 011360 012777 011414 175230 DONE:  MOV      #PER, @PVEC ;WHEN DONE PRINT "."
1809 011366 012777 000056 175216 MOV      #56, @PDBR
1810 011374 000002 RTI
1811
1812 011376 012737 177776 006636 COLON: MOV      #-2, @CNTB
1813 011404 012777 000072 175200 MOV      #72, @PDBR
1814 011412 000002 RTI
1815
1816 011414 005037 006636 PER:    CLR      @CNTB      ;PRINT MSB OF MILLISEC
1817 011420 000250 CLN
1818 011422 013737 006700 006634 MOV      @MSTA, @CNT1
1819 011430 012737 177767 006632 MOV      #-9, @CNT
1820 011436 162737 000144 006634 1$:    SUB      #100., @CNT1
1821 011444 100406 BMI
1822 011446 005237 006636 INC      @CNTB
1823 011452 005237 006632 INC      @CNT
1824 011456 001367 BNE     1$
1825 011460 000404 BR      3$
1826 011462 062737 000144 006634 2$:    ADD      #100., @CNT1
1827 011470 000250 CLN
1828 011472 062737 000060 006636 3$:    ADD      #60, @CNTB
1829 011500 012777 011516 175110 MOV      #NUM1, @PVEC
1830 011506 013777 006636 175076 MOV      @CNTB, @PDBR
1831 011514 000002 RTI
1832
1833 011516 012777 011600 175072 NUM1:  MOV      #NUM2, @PVEC ;PRINT LSB OF MILLISEC
1834 011524 005037 006636 CLR      @CNTB
1835 011530 000250 CLN
1836 011532 012737 177767 006632 MOV      #-9, @CNT
1837 011540 162737 000012 006634 1$:    SUB      #10., @CNT1
1838 011546 100405 BMI

```



```

1839 011550 005237 006636      INC      @CNTB
1840 011554 005237 006632      INC      @CNT
1841 011560 001367              BNE      1$
1842 011562 062737 000060 006636 3$:    ADD      @60,@CNTB
1843 011570 013777 006636 175014    MOV      @CNTB,@PDBR
1844 011576 000002              RTI
1845
1846 011600 012777 007560 175020 NUM2:  MOV      @KINTR,@KVEC      ;RESTORE KEYBOARD VECTOR
1847 011606 000002              RTI
1848
1849
1850
1851
1852
1853
1854 011610 032777 000010 167226 DELADJ: BIT      @10,@SR      ;TEST FOR SR3=1 WHICH INCL.CATES
1855                                ;11/60, 11/70 & 11/45 WITH MOS
1856 011616 001001              BNE      1$      ;ADJUST DELAY TIMES
1857 011620 000207              RTS      %7      ;NO ADJUSTMENTS REQUIRED
1858 011622 012701 001034      1$:    MOV      @ADJ,R1      ;GET START OF REG. FOR ADJUST
1859 011626 012700 001024      MOV      @DEL1,R0      ;GET START OF REG. TO ADJUST
1860 011632 012702 001032      MOV      @DEL4,R2      ;GET END TAG OF ADJUSTMENT
1861 011636 062702 000002      ADD      @2,R2      ;UPDATE END CHECK
1862 011642 012120      2$:    MOV      (R1)+,(R0)+      ;UPDATE DELAY COUNTS
1863 011644 020200      CMP      R2,R0      ;ARE WE DONE
1864 011646 001375      BNE      2$      ;NO CONTINUE UPDATE
1865 011650 000207      RTS      %7      ;ADJUSTMENT MADE
1866
1867 011652 013746 000004      SWADJ: MOV      @#4,-(%6)      ;SAVE CONTENT OF TRAP
1868                                ;VECTOR
1869 011656 012737 011676 000004      MOV      @SWADJ1,@#4      ;SET UP NEW TRAP VECTOR
1870 011664 005777 167154      TST      @SR      ;TEST FOR SWITCH REG.
1871 011670 012637 000004      MOV      (%6)+,@#4      ;RESTORE STACK NO
1872                                ;TIME OUT ACCONED.
1873 011674 000207              RTS      %7
1874
1875 011676 022626      SWADJ1: CMP      (%6)+,(%6)+      ;UPDATE STACK
1876 011700 012637 000004      MOV      (%6)+,@#4      ;RESTORE TRAP VECTOR
1877 011704 012737 000176 001044      MOV      @SOFTSR,SR      ;SET SWITCH REG.(SR) TO
1878                                ;EQUAL SOFTSR
1879 011712 000207              RTS      %7      ;RETURN TO CALLER
1880
1881
1882
1883      000001      .END

```

| | | | | | | | | | | | | | | |
|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| ADJ | 001034 | 474# | 1858 | | | | | | | | | | | |
| BEGIN | 001150 | 452 | 500# | 516 | 1134 | 1212 | 1224 | 1313 | | | | | | |
| BEGIN1 | 005210 | 453 | 1143# | 1179 | 1196 | 1208 | 1214 | | | | | | | |
| BEGIN2 | 001046 | 451 | 484# | | | | | | | | | | | |
| BUFF = | 000776 | 449# | 484 | 500 | 850 | 865 | 880 | 895 | 1143 | 1217 | 1418 | 1430 | 1442 | 1454 |
| | | 1473 | | | | | | | | | | | | |
| BYT1 | 006704 | 1406# | 1598 | 1622 | | | | | | | | | | |
| BYT2 | 006705 | 1407# | | | | | | | | | | | | |
| BYT3 | 006706 | 1408# | | | | | | | | | | | | |
| BYT4 | 006707 | 1409# | | | | | | | | | | | | |
| BYT5 | 006710 | 1410# | | | | | | | | | | | | |
| BYT6 | 006711 | 1411# | | | | | | | | | | | | |
| BYT7 | 006712 | 1412# | 1617 | | | | | | | | | | | |
| CACL | 004446 | 1016 | 1027# | 1058 | 1083 | | | | | | | | | |
| CC = | 177776 | 445# | 629* | 830* | 853* | 868* | 884* | 1088* | 1104* | 1287* | | | | |
| CHAR | 006100 | 1252* | 1255* | 1263* | 1264* | 1265* | 1274* | 1277 | | | | | | |
| CKCSR | 010156 | 1599# | 1601 | 1618 | | | | | | | | | | |
| CKV | 001006 | 463# | 834* | 854* | 869* | 887* | 899* | 948 | 952* | 975* | 1145* | 1482* | | |
| CKVS | 001010 | 464# | 831* | 953* | 1145 | 1146* | 1483* | | | | | | | |
| CKVS1 | 006604 | 1372# | 1503* | | | | | | | | | | | |
| CKV1 | 006602 | 1371# | 1502* | | | | | | | | | | | |
| CLK | 007672 | 1421* | 1433* | 1445* | 1457* | 1537# | 1567 | 1569 | 1572 | 1575 | | | | |
| CLKFLG | 006606 | 1373# | 1488* | 1499 | 1504* | 1508* | | | | | | | | |
| CLKI | 010476 | 1482 | 1697# | | | | | | | | | | | |
| CLKON | 007434 | 1493 | 1495# | | | | | | | | | | | |
| CLKSER | 004240 | 952 | 979# | | | | | | | | | | | |
| CLKXIT | 004244 | 981# | | | | | | | | | | | | |
| CLK1 | 007700 | 1422* | 1434* | 1446* | 1458* | 1538# | | | | | | | | |
| CLK2 | 010772 | 1590 | 1746# | | | | | | | | | | | |
| CLK3 | 010504 | 1426* | 1438* | 1450* | 1462* | 1698# | | | | | | | | |
| CLK4 | 010534 | 1427* | 1439* | 1451* | 1463* | 1700 | 1703# | | | | | | | |
| CNGSWR | 010134 | 1518 | 1591# | | | | | | | | | | | |
| CNT | 006632 | 951# | 972* | 973 | 1383# | 1528* | 1546* | 1786* | 1799* | 1819* | 1823* | 1836* | 1840* | |
| CNTB | 006636 | 1385# | 1784* | 1801 | 1806* | 1812* | 1816* | 1822* | 1828* | 1830 | 1834* | 1839* | 1842* | 1843 |
| CNT1 | 006634 | 1384# | 1529* | 1541 | 1545* | 1785* | 1803 | 1805* | 1818* | 1820* | 1826* | 1837* | | |
| COLON | 011376 | 1802 | 1812# | | | | | | | | | | | |
| CR | 011266 | 1783 | 1792# | | | | | | | | | | | |
| CRLF | 010324 | 1597 | 1636 | 1639# | 1641 | | | | | | | | | |
| CSB | 001002 | 461# | 536* | 537 | 549* | 558* | 568* | 582* | 643* | 651* | 660* | 672* | 685* | 698* |
| | | 714* | 731* | 748* | 765* | 780* | 797* | 815* | 833* | 856* | 871* | 886* | 900* | 927* |
| | | 954* | 1001* | 1009* | 1043* | 1051* | 1068* | 1076* | 1089* | 1105* | 1150* | 1164* | 1185* | 1198* |
| | | 1491* | 1527* | 1537* | | | | | | | | | | |
| CSB1 | 006574 | 1021* | 1368# | 1501* | 1505* | 1512* | | | | | | | | |
| CSR | 001000 | 460# | 521* | 523 | 557* | 567* | 571* | 572 | 573* | 574 | 589* | 590 | 593* | 594 |
| | | 597* | 598 | 601* | 602 | 607* | 608 | 611* | 612 | 617* | 618 | 621* | 622 | 630* |
| | | 631 | 634* | 635 | 641* | 644* | 645 | 649* | 652* | 653* | 654 | 658* | 661* | 662* |
| | | 663 | 671* | 674* | 684* | 687* | 697* | 699* | 701 | 705* | 713* | 715* | 717 | 721* |
| | | 730* | 732* | 734 | 738* | 747* | 749* | 751 | 755* | 764* | 766* | 768 | 772* | 779* |
| | | 781* | 783 | 787* | 796* | 798* | 800 | 804* | 814* | 816* | 818 | 822* | 832* | 835* |
| | | 839* | 842 | 849* | 855* | 857* | 861* | 864* | 870* | 872* | 876* | 878* | 885* | 888* |
| | | 892* | 894* | 901* | 905* | 911* | 928* | 935* | 955* | 976* | 1000* | 1002* | 1004 | 1008* |
| | | 1010* | 1012 | 1042* | 1044* | 1046 | 1050* | 1052* | 1054 | 1067* | 1069* | 1071 | 1075* | 1077* |
| | | 1079 | 1087* | 1090* | 1094 | 1096* | 1098* | 1099 | 1106* | 1110 | 1112* | 1115 | 1153* | 1162* |
| | | 1167* | 1176* | 1187* | 1194* | 1200* | 1207* | 1240 | 1490* | 1526* | 1538* | | | |
| CSRT | 001312 | 520 | 527# | | | | | | | | | | | |
| CSR1 | 006576 | 1020* | 1022* | 1023 | 1369# | 1506* | 1511* | | | | | | | |

| | | | | | | | | | | | | | | | | | | | |
|--------|----------|-------|-------|-------|------|------|-------|-------|-------|-------|-------|------|------|------|--|--|--|--|--|
| T24C | 004010 | 907 | 922# | | | | | | | | | | | | | | | | |
| T24D | 004076 | 934 | 947# | | | | | | | | | | | | | | | | |
| T25 | 004264 | 926 | 977 | 996# | | | | | | | | | | | | | | | |
| T25A | 004502 | 1018 | 1041# | | | | | | | | | | | | | | | | |
| T26 | 004616 | 1064# | | | | | | | | | | | | | | | | | |
| T27 | 004740 | 999 | 1066 | 1086# | | | | | | | | | | | | | | | |
| T27A | 005040 | 1103# | | | | | | | | | | | | | | | | | |
| T28 | 005256 | 1152# | 1161 | | | | | | | | | | | | | | | | |
| T28A | 005270 | 1154# | 1156 | | | | | | | | | | | | | | | | |
| T29 | 005336 | 1166# | 1175 | | | | | | | | | | | | | | | | |
| T29A | 005350 | 1168# | 1170 | | | | | | | | | | | | | | | | |
| T3 | 001414 | 549# | 554 | | | | | | | | | | | | | | | | |
| T3A | 001442 | 556# | | | | | | | | | | | | | | | | | |
| T38 | 001504 | 566# | | | | | | | | | | | | | | | | | |
| T30 | 005456 | 1188# | 1193 | | | | | | | | | | | | | | | | |
| T31 | 005536 | 1201# | 1206 | | | | | | | | | | | | | | | | |
| T4 | 001572 | 581# | | | | | | | | | | | | | | | | | |
| T5 | 001614 | 588# | | | | | | | | | | | | | | | | | |
| T6 | 001712 | 606# | | | | | | | | | | | | | | | | | |
| T7 | 001750 | 616# | | | | | | | | | | | | | | | | | |
| T9 | 002006 | 628# | | | | | | | | | | | | | | | | | |
| T9A | 002052 | 640# | | | | | | | | | | | | | | | | | |
| WAITA | 007422 | 1492# | 1500 | 1513 | | | | | | | | | | | | | | | |
| WAITB | 007432 | 1494# | 1507 | | | | | | | | | | | | | | | | |
| XOR | 001230 | 492 | 512# | | | | | | | | | | | | | | | | |
| XORA | 006254 | 1296 | 1310# | | | | | | | | | | | | | | | | |
| XORFLG | 006252 | 495* | 515* | 728 | 794 | 1065 | 1178 | 1293 | 1309# | | | | | | | | | | |
| XORM | 006540 | 497 | 1360# | | | | | | | | | | | | | | | | |
| . | = 011714 | 435# | 437# | 442# | 450# | 459# | 538 | 543 | 551 | 563 | 578 | 585 | 591 | 595 | | | | | |
| | | 599 | 603 | 609 | 613 | 619 | 623 | 632 | 636 | 646 | 655 | 664 | 676 | 683 | | | | | |
| | | 708 | 724 | 741 | 758 | 775 | 790 | 807 | 826 | 844 | 847 | 904 | 1093 | 1100 | | | | | |
| | | 1109 | 1116 | 1123 | 1126 | 1158 | 1172 | 1182 | 1190 | 1203 | 1220 | 1229 | 1233 | 1247 | | | | | |
| | | 1276 | 1319 | 1324 | 1328 | 1331 | 1336# | 1343# | 1345# | 1359# | 1413# | 1709 | 1714 | 1719 | | | | | |
| | | 1724 | 1731 | 1737 | 1751 | 1756 | 1761 | 1766 | 1773 | 1779 | | | | | | | | | |

. ABS. 011714 000

ERRORS DETECTED: 0

CZKWBI.BIN,CZKWBI.LST/CRF/SOL/NL:TOC=CZKWBI.P11
RUN-TIME: 24.6 SECONDS
RUN-TIME RATIO: 210/7=27.6
CORE USED: 9K (17 PAGES)

H04