

DL11-W

DIAGNOSTIC
CZDLDC0

AH-8529C-MC

JUL 1978

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FICHE 1 OF 1

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This microfiche card contains a grid of frames, each displaying diagnostic data. The data is organized into columns and rows, with some frames containing headers such as 'CPU', 'I/O', and 'MEMORY'. The frames are arranged in a regular grid pattern, with the first column containing the most legible text. The data appears to be a series of test results or system status reports.

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IDENTIFICATION

PRODUCT CODE: AC-8528C-MC
PRODUCT NAME: CZDLDC0 DL11-W DIAG
DATE CREATED: MARCH 1978
MAINTAINER: DIAGNOSTIC ENGINEERING
AUTHOR: DAN CASALETTO

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1.0 GENERAL INFORMATION

1.1 ABSTRACT

THIS DIAGNOSTIC IS A LOGIC TEST TO VERIFY THE OPERATION OF THE DL11-W SERIAL LINE/ REAL TIME CLOCK INTERFACE. THE PROGRAM WILL RUN WITHOUT ANY SPECIAL TEST FIXTURES BY DEFAULT. HOWEVER, A WRAP CABLE CAN BE USED AND TESTED BY OPTION (BIT7 OF SWR).

THIS TEST OPERATES ON THE CONSOLE DL11-W SERIAL LINE AND CLOCK INTERFACES AS WELL AS UP TO FIFTEEN(15) ADDITIONAL IDENTICALLY CONFIGURED DL11-W SERIAL LINE INTERFACES. THE DEFAULT ADDRESSES ARE:

A. CONSOLE - 177560 SERIAL LINE
177546 CLOCK

B. OTHER SERIAL LINE - 776500 FIRST SERIAL LINE ADDRESS
OF 15 CONSECUTIVE SERIAL
LINE ADDRESSES

THE PROGRAM IS DESIGNED TO RUN ON ANY PDP-11 WITH 8K OF MEMORY AND A DL11-W MODULE. IT CAN BE RUN UNDER XXDP, APT, AND ACT MONITORS, AND ON PROCESSORS WITH NO HARDWARE SWITCH REGISTER, SOFTWARE SWITCH REGISTER = LOCATION 176

POWER FAILURE IS SUPPORTED FOR SYSTEMS WITH CORE MEMORY.

NOTE: THIS DIAGNOSTIC WITH THE SWR = 000020 (CLOCK TESTS ONLY) SHOULD BE USED ON SWITCHLESS CPU'S TO TEST KW-11L LINE CLOCK MODULES.

1.2 SYSTEM REQUIREMENTS

1.2.1 EQUIPMENT

STANDARD 11 FAMILY COMPUTER WITH A CONSOLE OUTPUT DEVICE AND 8K OF MEMORY.

1.2.2 STORAGE

THE PROGRAM USES MEMORY FROM 00000 TO 22372

1.3 ASSUMPTIONS

- A. IF THE UNIT UNDER TEST (UUT) IS THE CONSOLE , THE PROGRAM WILL ASSUME THE REAL TIME CLOCK (RTC) IS ENABLED AND WILL TEST IT UNLESS THE TESTS ARE DISABLED BY BIT6 OF THE SWR.
- B. IF THE UUT IS NOT THE CONSOLE, THE RTC IS NOT TESTED FOR THAT DEVICE.
- C. THE PROGRAM WILL ASSUME THE ERROR FLAG BITS AND THE BREAK FUNCTION OF THE DL11-W ARE DISABLED AND WILL NOT TEST THESE FUNCTIONS UNLESS ENABLED BY BIT10 (FOR ERROR FLAGS) AND BIT8 (FOR BREAK) OF THE SWR. THE DEFAULT CHARACTER SIZE IS 8 BITS (SEE PARA 2.3.2).

2.0 OPERATING INSTRUCTIONS

2.1 LOADING PROCEDURE

USE STANDARD PROCEDURE FOR PDP-11 ABSOLUTE BINARY FORMATTED TAPES.

2.2 STARTING PROCEDURE

LOAD THE SWITCH REGISTER WITH SETTING
(SOFTWARE SWITCH REGISTER LOCATION = 176)

- A. START AT 200.
AFTER CHECKING THE TRANSMITTER, THE PROGRAM WILL PRINT ITS IDENTIFICATION AND REPORT THE NUMBER OF DEVICES UNDER TEST (NUMBER IS OCTAL).
"END PASS" IS PRINTED AFTER A FULL PASS HAS BEEN MADE ON ALL DEVICES UNDER TEST.
- B. START AT 204. ****NOTE****
THE "ECHO" TEST WILL BE EXECUTED. AN "*" IS PRINTED AT THE BEGINNING OF THE TEST. THE ECHO TEST READS A CHARACTER FROM THE TERMINAL, WRITES THAT CHARACTER TO THE TERMINAL AND REPORTS ANY ERROR FLAGS SET IN THE RECEIVER BUFFER.
A CONTROL-C HALTS THE TEST AND PRINTS "STOP" AT THE TERMINAL CONTINUING RESTARTS THE ECHO TEST.
- C. START AT 210. ****NOTE****
THE TERMINAL OUTPUT TEST WILL BE EXECUTED. DEPRESSING ANY CHARACTER AT THE TERMINAL, HALTS THE TEST. CONTINUING RESTARTS THE TEST.
THE TEST OUTPUTS 32 CHARACTERS ON A LINE AND REPEATS THE PATTERN EVERY THREE LINES. THE PATTERN IS AS FOLLOWS
(OCTAL CODE 040 --> 377):

!'"\$%&'()*+,-./0123456789:;<=>?	(OCTAL CODE) (040 --> 077)
@ABCDEFGHIJKLMN OPQRSTUVWXYZ	(100 --> 137)
'ABCDEFGHIJKLMN OPQRSTUVWXYZ	(140 --> 177) LOWER CASE ALPHA

THIS BOTTOM LINE COULD BE THE FOLLOWING IF THE TERMINAL
DOES NOT HAVE LOWER CASE:

@ABCDEFGHIJKLMNOPQRSTUVWXYZ

UPPER CASE ALPHA

*****NOTE*****

IF THE TESTING ON TERMINIALS OTHER THAN THE CONSOLE IS DESIRED
FOR TESTS B OR C,SEE SECTION 2.3.4. AND 2.3.5. OF THIS DOCUMENT.

::++C
::++C

2.3 OPERATING PROCEDURE

2.3.1 OPERATIONAL SWITCH SETTINGS

NOTE: IF NO HARDWARE SWITCH REGISTER IS AVAILABLE THE PROGRAM WILL AUTOMATICALLY USE THE CONTENTS OF LOCATION 176 AS THE SOFTWARE SWITCH REGISTER. THE USER SHOULD SET THIS LOCATION BEFORE STARTING THE PROGRAM. IF A HARDWARE SWITCH IS AVAILABLE AND A SOFTWARE SWR IS DESIRED, PUT ALL SWITCHES UP.

BIT15	- HALT ON ERROR
BIT14	- SCOPE LOOP
BIT13	- INHIBIT ERROR TIMEOUT
BIT12	- UNUSED
BIT11	- UNUSED
BIT10	- ENABLE ERROR FLAGS TESTS
BIT09	- LOOP ON ERROR
BIT08	- ENABLE BREAK FUNCTION TESTS
BIT07	- ENABLE DATA TEST WITH WRAP CABLE
BIT06	- INHIBIT RTC TESTS (ALLOW ONLY SLU TESTS)
BIT05	- ALLOW MANUAL SETTING OF '\$DEVN' (DEVICE MAP)
BIT04	- INHIBIT SLU TESTS (ALLOW ONLY LINE CLOCK TESTS)

BUILT INTO THE PROGRAM IS THE ABILITY TO DYNAMICALLY CHANGE THE CONTENTS OF SWREG DURING PROGRAM EXECUTION. BY STRIKING G (CNTRL G) ON CONSOLE TTY THE OPERATOR SETS A REQUEST FLAG TO CHANGE THE CONTENTS OF SWREG, WHICH IS PROCESSED IN KEY AREAS OF THE PROGRAM CODE (IE) ERROR ROUTINES, AFTER HALTS END OF PASS, AND OTHER APPLICABLE AREAS. BECAUSE THIS DIAGNOSTIC USES THE MAINTENANCE BIT OF THE SERIAL LINE, THE CONTROL-G SHOULD BE ISSUED DURING PROGRAM TIMEOUTS AT THAT TIME THE MAINTENANCE BIT IS SURE TO BE CLEAR.

IF A CONTROL-G IS DETECTED, UPON EXECUTION THE CONTENTS OF THE SWREG ARE DUMPED IN OCTAL ON THE CONSOLE TTY AND ANY CHANGES ARE REQUESTED

(IE) SWR=XXXXXX NEW=

POSSIBLE RESPONSES ARE:

1. <CR> IF NO CHANGES ARE TO BE MADE
2. 6 DIGITS 0-7 TO REPRESENT IN OCTAL THE NEW SWITCH REGISTER VALUE ;LAST DIGIT FOLLOWED BY <CR>.
3. U TO ALLOW REENTERING VALUE IF ERROR IS COMMITTED KEYING IN SWREG VALUE.

2.3.2 SETTING BITS PER CHARACTER

THIS PROGRAM DEFAULTS TO TESTING 8 BITS PER CHARACTER. IF THE SERIAL LINE IS SET FOR 5-->7 BITS PER CHARACTER, SET THE MEMORY LOCATION "\$USWR" AS FOLLOWS:

CHAR. SIZE (# OF BITS)	"\$USWR" CONTENTS (BINARY)	(OCTAL)
8	100000000	400
7	010000000	200
6	001000000	100
5	000100000	40

"\$USWR" IS USED IN THE DATA PATH TESTS TO LIMIT THE BINARY COUNT TEST PATTERN TO THE NUMBER OF BITS SELECTED ON THE SERIAL LINE.

2.3.3 RUNNING UNDER APT

THE APT MAILBOX IS LOCATED AT LOCATION 500, TO ALLOW ADDITIONAL SERIAL LINE VECTOR ASSIGNMENTS TO THE 400 AREA OF MEMORY.

THE EXECUTION TIMES PROVIDED ARE FOR EXECUTION WITH AN 11/34 PROCESSOR, CORE MEMORY, AND 110 BAUD.

2.3.4 RUN WITH ALTERNATE CONSOLE ADDRESS

TO USE A CONSOLE ADDRESS OTHER THAN 177560, OR VECTOR OTHER THAN 60, THE OPERATOR MUST SUPPLY THE PROGRAM WITH THE CORRECT ADDRESSES BY INSERTING THEM AT THE TAG LABELED "CRCSR":

CRCSR: ADDRESS OF RECEIVER RCSR
CRBUF: ADDRESS OF RECEIVER BUFFER
CTCSR: ADDRESS OF TRANSMITTER CSR
CTBUF: ADDRESS OF TRANSMITTER BUFFER
CRVECT: ADDRESS OF RECEIVER VECTOR
CRPSW: ADDRESS OF ASSOCIATED PSW
CTVECT: ADDRESS OF TRANSMITTER VECTOR
CTPSW: ADDRESS OF ASSOCIATED PSW

2.3.5 TESTING ADDITIONAL SERIAL LINES

THIS PROGRAM WILL SUPPORT TESTING OF MULTIPLE SLU'S. IT REQUIRES THE ADDRESS OF THE FIRST ADDITIONAL RCSR (STORED AT "\$BASE") AND ITS INTERRUPT VECTOR (STORED AT "\$VECT1"); AND WILL BE ABLE TO ADDRESS ANY SLU STARTING AT THE SPECIFIED BASE ADDRESS UP TO 15 CONSECUTIVE DEVICES.

EXAMPLE: \$BASE: 776500
 \$VECT1: 300

THE PROGRAM WILL BE ABLE TO TEST THE CONSOLE PLUS ANY ADDITIONAL DL11-W SLU'S WITHIN THE RANGE 776500 --> 776660

\$BASE AND \$VECT1 DEFAULT TO 776500 AND 300 RESPECTIVELY.

THE PROGRAM ASSOCIATES UNIT NUMBERS TO DEVICES AS FOLLOWS:
(NUMBERS IN PARENTHESIS ARE OCTAL)

UNIT# 0 --> CONSOLE ADDRESS STORED AT "CRCSR"
UNIT# 1 --> BASE ADDRESS STORED AT "\$BASE"
 ASSOCIATED BASE VECTOR STORED AT "\$VECT1"
UNIT# 2 --> BASE ADDRESS + (10)
 BASE VECTOR + (10)
UNIT# 3 --> BASE ADDRESS + (20)
 BASE VECTOR + (20)
UNIT# 4 --> BASE ADDRESS + (30)
 BASE VECTOR + (30)

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 V
UNIT#15 --> BASE ADDRESS + (160)
 BASE VECTOR + (160)

STARTING AT LOCATION 200 AND HAVING BITS OF SWR CLEAR, THE PROGRAM WILL SELF
SIZE THE NUMBER OF DEVICES (STARTING AT THE BAS ADDRESS) AND
STORE A BIT MAP AT "\$DEV" (DEVICE MAP) TO INDICATE WHICH UNIT NUMBERS
ARE PRESENT AND WILL BE TESTED:

```
-----  
! UNIT ! UNIT ! ..... ! UNIT ! UNIT ! CONSOLE!  
! 15 ! 14 ! ..... ! 2 ! 1 !  
-----
```

A BIT MAP CAN BE ENTERED AT "\$DEV" PRIOR TO STARTING THE PROGRAM
SETTING BITS OF THE SWR INHIBITS THE SELF-SIZING AND DEVICE MAP
GENERATION, AND USES THE VALUE STORED BY THE OPERATOR.

EXAMPLE:

SWR = 000040 BINARY 0 000 000 000 100 000
\$BASE: 776500
\$VECT1: 300

\$DEV: 13 BINARY - 0 000 000 000 001 011

THE PROGRAM WILL TEST -
UNIT# 0 = CONSOLE
UNIT# 1 = 776500 ; 300
UNIT# 3 = 776520 ; 320

2.4 EXECUTION TIMES - (110 BAUD)

LONGEST SUBTEST TIME = 50 SECONDS
PASS TIME = 60 SECONDS
ADDITIONAL DEVICES = 55 SECONDS/DEVICE

3.0 ERROR REPORTING

IF A ROUTINE FAILS AND THE INHIBIT ERROR TYPEOUT (BIT13) OF THE SWR IS NOT SET, A PRINTOUT RESULTS IN THE FORM:

“(SOME ASCII MESSAGE)”
TEST# ERR PC RCSR ANY APPLICABLE DAT HEADINGS
XXXXXX XXXXXX XXXXXX ANY APPLICABLE DATA

NOTE: "RCSR" IS DEPENDENT ON THE FAILURE
& THEREFORE COULD BE TCSR,RBUF,TBUF,OR LKS

WHERE "XXXXXX" IS AN OCTAL NUMBER.
THIS ERROR PRINTOUT OCCURS PROVIDED THE ERROR THAT EXISTS
WOULD NOT HINDER THE TYPEOUT. IN CASES WHERE IT IS NOT POSSIBLE
TO PRINT AN ERROR MESSAGE (I.E. FATAL CONSOLE TRANSMITTER
FAILURES), A HALT OCCURS AND THE PC CAN BE EXAMINED BY THE OPERATOR
TO FIND THE ERROR INFORMATION IN THE PROGRAM LISTING.

NOTE: FOR SOFTWARE SWITCH OPERATION, THE SWITCH REGISTER CAN
BE CHANGED BY TYPING A CONTROL-G AT THE CONSOLE DURING ERROR PRINTOUTS.
AFTER CONTINUING FROM THE ERROR HALT THE OLD SWR CONTENTS
IS DISPLAYED AND THE NEW CONTENTS CAN BE ENTERED.
IF ERROR HALTS ARE DISABLED, THE CONTROL-G RESPONSE OCCURS
IMMEDIATELY FOLLOWING THE TYPEOUT.

4.0 SUBROUTINE ABSTRACTS

4.1 TRAPCATCHER

THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION 0 DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS TO THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE NEXT LOCATION. THE NEXT LOCATION IS LOADED WITH A BREAK POINT TRAP (000003). THUS AN ILLEGAL TRAP OR INTERRUPT CAUSES A TRAP THROUGH THE BPT VECTOR(14) WHICH POINTS TO THE "CATCH" ROUTINE.

THE "CATCH" ROUTINE REPORTS THE PC THAT CAUSED THE ORIGINAL TRAP AND THE LOCATION OF THE TRAP VECTOR (IF UNDER APT, AN ERROR IS INDICATED TO APT). AFTER REPORTING THE ERROR THE PROGRAM HALTS. THE PROGRAM MUST BE RESTARTED AT THIS POINT.

4.2 WRPSW

THIS ROUTINE IS USED TO WRITE THE PSW BY POPPING VALUES FROM THE STACK. THIS METHOD IS USED TO BE COMPATIBLE WITH ALL 11 FAMILY PROCESSORS.

4.3 SCOPE

THIS ROUTINE CALL IS PLACED BETWEEN EACH SUBTEST. IT RECORDS THE STARTING ADDRESS OF EACH SUBTEST AS IT IS BEING ENTERED AND UPDATES THE TEST NUMBER. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUBTEST AT WHICH THE SCOPE LOOP IS REQUESTED.

4.4 ERROR

THIS ROUTINE CALL IS PLACED WHEREEVER AN ERROR REPORT IS DESIRED. THE LOWER BYTE OF THIS CALL IS USED AS THE ERROR NUMBER AND AS A POINTER INTO THE ERROR TABLE. THIS ROUTINE REPORTS ERRORS TO APT USING "\$APTYPE" AND TYPES ERROR REPORTS TO THE CONSOLE USING "\$ERRTYPE".

4.5 \$POWER

THIS ROUTINE SAVES ALL GENERAL REGISTERS DURING POWER-DOWN AND RESTORES THEM AT POWER-UP. IF A POWER FAILURE OCCURS 'POWER' IS PRINTED AT THE CONSOLE AFTER POWER IS RESTORED.

4.6 CKSWR

THIS ROUTINE CALL IS USED TO DETECT THE RECEPTION OF A CONTROL-G FROM THE CONSOLE. THE CALL USES "\$READ" TO PERFORM THE CONTROL-G SEQUENCE OF DISPLAYING THE CONTENTS OF THE SOFTWARE SWITCH REGISTER AND THE ENTERING THE NEW CONTENTS FROM THE TERMINAL.

%

```
422
423
424
425
426
427      .SBTTL  BASIC DEFINITIONS
428
429      ;*INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***
430      001100  STACK= 1100
431      .EQUIV  EMT,ERROR      ;;BASIC DEFINITION OF ERROR CALL
432      .EQUIV  IOT,SCOPE     ;;BASIC DEFINITION OF SCOPE CALL
433
434      ;*MISCELLANEOUS DEFINITIONS
435      000011  HT= 11          ;;CODE FOR HORIZONTAL TAB
436      000012  LF= 12          ;;CODE FOR LINE FEED
437      000015  CR= 15          ;;CODE FOR CARRIAGE RETURN
438      000200  CRLF= 200       ;;CODE FOR CARRIAGE RETURN-LINE FEED
439      177776  PS= 177776     ;;PROCESSOR STATUS WORD
440      .EQUIV  PS,PSW
441      177774  STKLMT= 177774  ;;STACK LIMIT REGISTER
442      177772  PIRQ= 177772   ;;PROGRAM INTERRUPT REQUEST REGISTER
443      177570  DSWR= 177570   ;;HARDWARE SWITCH REGISTER
444      177570  DDISP= 177570  ;;HARDWARE DISPLAY REGISTER
445
446      ;*GENERAL PURPOSE REGISTER DEFINITIONS
447      000000  R0= X0          ;;GENERAL REGISTER
448      000001  R1= X1          ;;GENERAL REGISTER
449      000002  R2= X2          ;;GENERAL REGISTER
450      000003  R3= X3          ;;GENERAL REGISTER
451      000004  R4= X4          ;;GENERAL REGISTER
452      000005  R5= X5          ;;GENERAL REGISTER
453      000006  R6= X6          ;;GENERAL REGISTER
454      000007  R7= X7          ;;GENERAL REGISTER
455      000006  SP= X6          ;;STACK POINTER
456      000007  PC= X7          ;;PROGRAM COUNTER
457
458      ;*PRIORITY LEVEL DEFINITIONS
459      000000  PR0= 0          ;;PRIORITY LEVEL 0
460      000040  PR1= 40         ;;PRIORITY LEVEL 1
461      000100  PR2= 100        ;;PRIORITY LEVEL 2
462      000140  PR3= 140        ;;PRIORITY LEVEL 3
463      000200  PR4= 200        ;;PRIORITY LEVEL 4
464      000240  PR5= 240        ;;PRIORITY LEVEL 5
465      000300  PR6= 300        ;;PRIORITY LEVEL 6
466      000340  PR7= 340        ;;PRIORITY LEVEL 7
467
468      ;*"SWITCH REGISTER" SWITCH DEFINITIONS
469      100000  SW15= 100000
470      040000  SW14= 40000
471      020000  SW13= 20000
472      010000  SW12= 10000
473      004000  SW11= 4000
474      002000  SW10= 2000
475      001000  SW09= 1000
476      000400  SW08= 400
477      000200  SW07= 200
```

BASIC DEFINITIONS

```
478      000100      SW06= 100
479      000040      SW05= 40
480      000020      SW04= 20
481      000010      SW03= 10
482      000004      SW02= 4
483      000002      SW01= 2
484      000001      SW00= 1
485      .EQUIV      SW09,SW9
486      .EQUIV      SW08,SW8
487      .EQUIV      SW07,SW7
488      .EQUIV      SW06,SW6
489      .EQUIV      SW05,SW5
490      .EQUIV      SW04,SW4
491      .EQUIV      SW03,SW3
492      .EQUIV      SW02,SW2
493      .EQUIV      SW01,SW1
494      .EQUIV      SW00,SW0
```

496 ;*DATA BIT DEFINITIONS (BIT00 TO BIT15)

```
497      100000      BIT15= 100000
498      040000      BIT14= 40000
499      020000      BIT13= 20000
500      010000      BIT12= 10000
501      004000      BIT11= 4000
502      002000      BIT10= 2000
503      001000      BIT09= 1000
504      000400      BIT08= 400
505      000200      BIT07= 200
506      000100      BIT06= 100
507      000040      BIT05= 40
508      000020      BIT04= 20
509      000010      BIT03= 10
510      000004      BIT02= 4
511      000002      BIT01= 2
512      000001      BIT00= 1
513      .EQUIV      BIT09,BIT9
514      .EQUIV      BIT08,BIT8
515      .EQUIV      BIT07,BIT7
516      .EQUIV      BIT06,BIT6
517      .EQUIV      BIT05,BIT5
518      .EQUIV      BIT04,BIT4
519      .EQUIV      BIT03,BIT3
520      .EQUIV      BIT02,BIT2
521      .EQUIV      BIT01,BIT1
522      .EQUIV      BIT00,BIT0
```

524 ;*BASIC "CPU" TRAP VECTOR ADDRESSES

```
525      000004      ERRVEC= 4          ;; TIME OUT AND OTHER ERRORS
526      000010      RESVEC= 10         ;; RESERVED AND ILLEGAL INSTRUCTIONS
527      000014      TBITVEC=14        ;; "T" BIT
528      000014      TRTVEC= 14         ;; TRACE TRAP
529      000014      BPTVEC= 14         ;; BREAKPOINT TRAP (BPT)
530      000020      IOTVEC= 20         ;; INPUT/OUTPUT TRAP (IOT) **SCOPE**
531      000024      PWRVEC= 24         ;; POWER FAIL
532      000030      EMTVEC= 30         ;; EMULATOR TRAP (EMT) **ERROR**
533      000034      TRAPVEC=34        ;; "TRAP" TRAP
```

BASIC DEFINITIONS

```
534      000060      TKVEC= 60      ;;TTY KEYBOARD VECTOR
535      000064      TPVEC= 64      ;;TTY PRINTER VECTOR
536      000240      PIRQVEC=240    ;;PROGRAM INTERRUPT REQUEST VECTOR
537      176500      ABASE= 176500
538      000300      AVECT1= 300
539      000400      AUSWR= 400
540      000001      $TN= 1
541      161000      $SWR= 161000
542      000003      BPT= 000003      ;THIS IS THE COMMAND FOR A TRAP
543                                     ; THROUGH 14 (BPT TRAP)
544
545      000000      .=0
546      ;*****
547      ;*ALL UNUSED LOCATIONS FROM 4-776 CONTAIN A ".+2,BPT"
548      ;*SEQUENCE TO CATCH ILLEGAL TRAPS & INTERRUPTS
549      ;*LOCATION 0 CONTAINS 0 TO CATCH IMPROPERLY LOADED VECTORS
550
551
552      000014      .=14      ;THE BPT TRAP VECTOR POINTS TO THE
553 000014 012254   .WORD  CATCH  ; ILLEGAL TRAP HANDLER "CATCH"
554 000016 000340   .WORD  340
555
556      000042      .= 42
557 000042 000000   .WORD  0
558
559
560
561
562      000174      .= 174
563 000174 000000   DISPREG: .WORD 0
564 000176 000000   SWREG:  .WORD 0
565
566      000200      .=200
567 000200 000137 002546  JMP  START      ;DO INTERFACE TEST
568 000204 000137 014762  JMP  ECHO       ;DO ECHO TEST
569 000210 000137 015202  JMP  OUTTST    ;DO OUTPUT TEST TO TERMINAL
```

BASIC DEFINITIONS

```
570
571      000500
572
573
574      .SBTTL      .=      500
575      .SBTTL      ACT11 HOOKS
576      ;:*****
577      ;HOOKS REQUIRED BY ACT11
578      $SVPC=.      ;SAVE PC
579      .=46
580      $ENDAD      ;;1)SET LOC.46 TO ADDRESS OF $ENDAD IN .SEOP
581      .=52
582      .WORD      0      ;;2)SET LOC.52 TO ZERO
583      .= $SVPC      ;; RESTORE PC
584      .SBTTL      APT PARAMETER BLOCK
585      ;:*****
586      ;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
587      ;:*****
588      .$X=.      ;;SAVE CURRENT LOCATION
589      .=24      ;;SET POWER FAIL TO POINT TO START OF PROGRAM
590      200      ;;FOR APT START UP
591      .=44      ;;POINT TO APT INDIRECT ADDRESS PNTR.
592      $APTHDR      ;;POINT TO APT HEADER BLOCK
593      .=.$X      ;;RESET LOCATION COUNTER
594      ;:*****
595      ;SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC
596      ;INTERFACE SPEC.
597      $APTHD:
598      $HIBTS: .WORD      0      ;;TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
599      $MBADR: .WORD      $MAIL      ;;ADDRESS OF APT MAILBOX (BITS 0-15)
600      $TSTM: .WORD      50      ;;RUN TIM OF LONGEST TEST
601      $PASTM: .WORD      60      ;;RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
602      $UNITM: .WORD      55      ;;ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
603      .WORD      $ETEND-$MAIL/2 ;;LENGTH MAILBOX-ETABLE(WORDS)
604
```

```
605          .SBTTL COMMON TAGS
606
607          ;:*****
608          ;*THIS TABLE CONTAINS VARIOUS COMMON STORAGE LOCATIONS
609          ;*USED IN THE PROGRAM.
610
611          001000          .=1000
612 001000          $CMTAG:          ;;START OF COMMON TAGS
613 001000 000000          .WORD          0          ;;CONTAINS THE TEST NUMBER
614 001002 000          $TSTNM: .BYTE          0          ;;CONTAINS ERROR FLAG
615 001003 000          $ERFLG: .BYTE          0          ;;CONTAINS SUBTEST ITERATION COUNT
616 001004 000000          $ICNT: .WORD          0          ;;CONTAINS SCOPE LOOP ADDRESS
617 001006 000000          $LPADR: .WORD          0          ;;CONTAINS SCOPE RETURN FOR ERRORS
618 001010 000000          $LPERR: .WORD          0          ;;CONTAINS TOTAL ERRORS DETECTED
619 001012 000000          $ERTTL: .WORD          0          ;;CONTAINS ITEM CONTROL BYTE
620 001014 000          $ITEMB: .BYTE          0          ;;CONTAINS MAX. ERRORS PER TEST
621 001015 001          $ERMAX: .BYTE          1          ;;CONTAINS PC OF LAST ERROR INSTRUCTION
622 001016 000000          $ERRPC: .WORD          0          ;;CONTAINS ADDRESS OF 'GOOD' DATA
623 001020 000000          $GDADR: .WORD          0          ;;CONTAINS ADDRESS OF 'BAD' DATA
624 001022 000000          $BDADR: .WORD          0          ;;CONTAINS 'GOOD' DATA
625 001024 000000          $GDDAT: .WORD          0          ;;CONTAINS 'BAD' DATA
626 001026 000000          $BDDAT: .WORD          0          ;;RESERVED--NOT TO BE USED
627 001030 000000          .WORD          0
628 001032 000000          .WORD          0
629 001034 000          $AUTOB: .BYTE          0          ;;AUTOMATIC MODE INDICATOR
630 001035 000          $INTAG: .BYTE          0          ;;INTERRUPT MODE INDICATOR
631 001036 000000          .WORD          0
632 001040 177570          SWR: .WORD          DSWR          ;;ADDRESS OF SWITCH REGISTER
633 001042 177570          DISPLAY: .WORD          DDISP          ;;ADDRESS OF DISPLAY REGISTER
634 001044 177560          $TKS: 177560          ;;TTY KBD STATUS
635 001046 177562          $TKB: 177562          ;;TTY KBD BUFFER
636 001050 177564          $TPS: 177564          ;;TTY PRINTER STATUS REG. ADDRESS
637 001052 177566          $TPB: 177566          ;;TTY PRINTER BUFFER REG. ADDRESS
638 001054 000          $NULL: .BYTE          0          ;;CONTAINS NULL CHARACTER FOR FILLS
639 001055 002          $FILLS: .BYTE          2          ;;CONTAINS # OF FILLER CHARACTERS REQUIRED
640 001056 012          $FILLC: .BYTE          12          ;;INSERT FILL CHARS. AFTER A 'LINE FEED'
641 001057 000          $TPFLG: .BYTE          0          ;;'TERMINAL AVAILABLE' FLAG (BIT<07>=0=YES)
642 001060 000000          $ESCAPE:0          ;;ESCAPE ON ERROR ADDRESS
643 001062 077          $QUES: .ASCII /?/          ;;QUESTION MARK
644 001063 015          $CRLF: .ASCII <15>          ;;CARRIAGE RETURN
645 001064 000012          $LF: .ASCIZ <12>          ;;LINE FEED
646          ;:*****
647          .SBTTL APT MAILBOX-ETABLE
648
649          ;:*****
650          .EVEN
651 001066          $MAIL:          ;;APT MAILBOX
652 001066 000000          $MSGTY: .WORD          MSGTY          ;;MESSAGE TYPE CODE
653 001070 000000          $FATAL: .WORD          AFATAL          ;;FATAL ERROR NUMBER
654 001072 000000          $TESTN: .WORD          ATESTN          ;;TEST NUMBER
655 001074 000000          $PASS: .WORD          APASS          ;;PASS COUNT
656 001076 000000          $DEVCT: .WORD          ADEVCT          ;;DEVICE COUNT
657 001100 000000          $UNIT: .WORD          AUNIT          ;;I/O UNIT NUMBER
658 001102 000000          $MSGAD: .WORD          AMSGAD          ;;MESSAGE ADDRESS
659 001104 000000          $MSGLG: .WORD          AMSGLG          ;;MESSAGE LENGTH
660 001106          $ETABLE:          ;;APT ENVIRONMENT TABLE
```

```
661 001106 000 $ENV: .BYTE AENV ;;ENVIRONMENT BYTE
662 001107 000 $ENVM: .BYTE AENVM ;;ENVIRONMENT MODE BITS
663 001110 000000 $SWREG: .WORD ASWREG ;;APT SWITCH REGISTER
664 001112 000400 $USWR: .WORD AUSWR ;;USER SWITCHES
665 001114 000000 $CPUOP: .WORD ACPUOP ;;CPU TYPE,OPTIONS
666 :* BITS 15-11=CPU TYPE
667 :* 11/04=01,11/05=02,11/20=03,11/40=04,11/45=05
668 :* 11/70=06,PDQ=07,Q=10
669 :* BIT 10=REAL TIME CLOCK
670 :* BIT 9=FLOATING POINT PROCESSOR
671 :* BIT 8=MEMORY MANAGEMENT
672 001116 000 $MAMS1: .BYTE AMAMS1 ;;HIGH ADDRESS,M.S. BYTE
673 001117 000 $MTYP1: .BYTE AMTYP1 ;;MEM. TYPE,BLK#1
674 :* MEM.TYPE BYTE -- (HIGH BYTE)
675 :* 900 NSEC CORE=001
676 :* 300 NSEC BIPOLAR=002
677 :* 500 NSEC MOS=003
678 001120 000000 $MADR1: .WORD AMADR1 ;;HIGH ADDRESS,BLK#1
679 :* MEM.LAST ADDR.=3 BYTES,THIS WORD AND LOW OF "TYPE" ABOVE
680 001122 000 $MAMS2: .BYTE AMAMS2 ;;HIGH ADDRESS,M.S. BYTE
681 001123 000 $MTYP2: .BYTE AMTYP2 ;;MEM.TYPE,BLK#2
682 001124 000000 $MADR2: .WORD AMADR2 ;;MEM.LAST ADDRESS,BLK#2
683 001126 000 $MAMS3: .BYTE AMAMS3 ;;HIGH ADDRESS,M.S.BYTE
684 001127 000 $MTYP3: .BYTE AMTYP3 ;;MEM.TYPE,BLK#3
685 001130 000000 $MADR3: .WORD AMADR3 ;;MEM.LAST ADDRESS,BLK#3
686 001132 000 $MAMS4: .BYTE AMAMS4 ;;HIGH ADDRESS,M.S.BYTE
687 001133 000 $MTYP4: .BYTE AMTYP4 ;;MEM.TYPE,BLK#4
688 001134 000000 $MADR4: .WORD AMADR4 ;;MEM.LAST ADDRESS,BLK#4
689 001136 000300 $VECT1: .WORD AVECT1 ;;INTERRUPT VECTOR#1,BUS PRIORITY#1
690 001140 000000 $VECT2: .WORD AVECT2 ;;INTERRUPT VECTOR#2BUS PRIORITY#2
691 001142 176500 $BASE: .WORD ABASE ;;BASE ADDRESS OF EQUIPMENT UNDER TEST
692 001144 000000 $DEVMM: .WORD ADEVMM ;;DEVICE MAP
693 001146
694 .MEXIT
```

ERROR POINTER TABLE

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.SBTTL ERROR POINTER TABLE

;*THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.
;*THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN
;*LOCATION \$ITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.
;*NOTE1: IF \$ITEMB IS 0 THE ONLY PERTINENT DATA IS (\$ERRPC).
;*NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:

;* EM ;;POINTS TO THE ERROR MESSAGE
;* DH ;;POINTS TO THE DATA HEADER
;* DT ;;POINTS TO THE DATA
;* DF ;;POINTS TO THE DATA FORMAT

\$ERRTB:

.\$ERRTB:

EM1	;;"CAN NOT ACCESS TCSR"
DH1	;;"TEST# ERR PC TCSR"
DT1	;;\$TESTN,\$ERRPC,TCSR
0	
EM2	;;"CAN NOT ACCESS TBUF"
DH2	;;"TEST# ERR PC TBUF"
DT2	;;\$TESTN,\$ERRPC,TBUF
0	
EM3	;;"TCSR DONE NOT CLEARED WITH TBUF FULL"
DH1	;;"TEST# ERR PC TCSR"
DT1	;;\$TESTN,\$ERRPC,TCSR
0	
EM4	;;"TCSR DONE NOT SET"
DH1	;;"TEST# ERR PC TCSR"
DT1	;;\$TESTN,\$ERRPC,TCSR
0	
EM5	;;TCSR DONE NOT SET WITH RESET
DH1	;;"TEST# ERR PC TCSR"
DT1	;;\$TESTN,\$ERRPC,TCSR
0	
EM6	;;"CAN NOT ACCESS RCSR"
DH6	;;"TEST# ERR PC RCSR"
DT6	;;\$TESTN,\$ERRPC,RCSR
0	
EM7	;;"CAN NOT ACCESS RBUF"
DH7	;;"TEST# ERR PC RBUF"
DT7	;;\$TESTN,\$ERRPC,RBUF
0	
EM10	;;"CAN NOT ACCESS LKS"
DH10	;;"TEST# ERR PC LKS"
DT10	;;\$TESTN,\$ERRPC,LKS
0	

751				
752	001246	015555	EM11	;'BIT0 OF TCSR NOT CLEAR AFTER RESET''
753	001250	021451	DH1	;'TEST# ERR PC TCSR''
754	001252	022204	DT1	;\$TESTN,\$ERRPC,TCSR
755	001254	000000	0	
756				
757	001256	015620	EM12	;'CAN NOT SET BIT0 OF TCSR''
758	001260	021451	DH1	;'TEST# ERR PC TCSR''
759	001262	022204	DT1	;\$TESTN,\$ERRPC,TCSR
760	001264	000000	0	
761				
762	001266	015651	EM13	;'CAN NOT CLEAR BIT0 OF TCSR''
763	001270	021451	DH1	;'TEST# ERR PC TCSR''
764	001272	022204	DT1	;\$TESTN,\$ERRPC,TCSR
765	001274	000000	0	
766				
767	001276	015704	EM14	;'RESET DID NOT CLEAR BIT0 OF TCSR''
768	001300	021451	DH1	;'TEST# ERR PC TCSR''
769	001302	022204	DT1	;\$TESTN,\$ERRPC,TCSR
770	001304	000000	0	
771				
772	001306	015745	EM15	;'BIT2 OF TCSR NOT CLEAR AFTER RESET''
773	001310	021451	DH1	;'TEST# ERR PC TCSR''
774	001312	022204	DT1	;\$TESTN,\$ERRPC,TCSR
775	001314	000000	0	
776				
777	001316	016010	EM16	;'CAN NOT SET BIT2 OF TCSR''
778	001320	021451	DH1	;'TEST# ERR PC TCSR''
779	001322	022204	DT1	;\$TESTN,\$ERRPC,TCSR
780	001324	000000	0	
781				
782	001326	016041	EM17	;'CAN NOT CLEAR BIT2 OF TCSR''
783	001330	021451	DH1	;'TEST# ERR PC TCSR''
784	001332	022204	DT1	;\$TESTN,\$ERRPC,TCSR
785	001334	000000	0	
786				
787	001336	016074	EM20	;'RESET DID NOT CLEAR BIT2 OF TCSR''
788	001340	021451	DH1	;'TEST# ERR PC TCSR''
789	001342	022204	DT1	;\$TESTN,\$ERRPC,TCSR
790	001344	000000	0	
791				
792	001346	016135	EM21	;'BIT6 OF TCSR NOT CLEAR AFTER RESET2
793	001350	021451	DH1	;'TEST# ERR PC TCSR''
794	001352	022204	DT1	;\$TESTN,\$ERRPC,TCSR
795	001354	000000	0	
796				
797	001356	016201	EM22	;'XMIT INTERRUPT WITH PRIORITY 7''
798	001360	021451	DH1	;'TEST# ERR PC TCSR''
799	001362	022204	DT1	;\$TESTN,\$ERRPC,TCSR
800	001364	000000	0	
801				
802	001366	016236	EM23	;'CAN NOT SET BIT6 OF TCSR''
803	001370	021451	DH1	;'TEST# ERR PC TCSR''
804	001372	022204	DT1	;\$TESTN,\$ERRPC,TCSR
805	001374	000000	0	
806				

ERROR POINTER TABLE

807	001376	016267	EM24	:"CAN NOT CLEAR BIT6 OF TCSR"
808	001400	021451	DH1	:"TEST# ERR PC TCSR"
809	001402	022204	DT1	;\$TESTN,\$ERRPC,TCSR
810	001404	000000	0	
811				
812	001406	016322	EM25	:"RESET DID NOT CLEAR BIT6 OF TCSR"
813	001410	021451	DH1	:"TEST# ERR PC TCSR"
814	001412	022204	DT1	;\$TESTN,\$ERRPC,TCSR
815	001414	000000	0	
816				
817	001416	016363	EM26	:"BIT6 OF RCSR NOT CLEAR AFTER RESET"
818	001420	021523	DH6	:"TEST# ERR PC RCSR"
819	001422	022224	DT6	;\$TESTN,\$ERRPC,RCSR
820	001424	000000	0	
821				
822	001426	016426	EM27	:"RCVR INTERRUPT WITH PRIORITY 7"
823	001430	021523	DH6	:"TEST# ERR PC RCSR"
824	001432	022224	DT6	;\$TESTN,\$ERRPC,RCSR
825	001434	000000	0	
826				
827	001436	016465	EM30	:"CAN NOT SET BIT6 OF RCSR"
828	001440	021523	DH6	:"TEST# ERR PC RCSR"
829	001442	022224	DT6	;\$TESTN,\$ERRPC,RCSR
830	001444	000000	0	
831				
832	001446	016516	EM31	:"CAN NOT CLEAR BIT6 OF RCSR"
833	001450	021523	DH6	:"TEST# ERR PC RCSR"
834	001452	022224	DT6	;\$TESTN,\$ERRPC,RCSR
835	001454	000000	0	
836				
837	001456	016551	EM32	:"CAN NOT CLEAR BIT6 OF RCSR WITH RESET2"
838	001460	021523	DH6	:"TEST# ERR PC RCSR"
839	001462	022224	DT6	;\$TESTN,\$ERRPC,RCSR
840	001464	000000	0	
841				
842	001466	016617	EM33	:"BIT6 OF LKS NOT CLEAR AFTER RESET"
843	001470	021575	DH10	:"TEST# ERR PC LKS"
844	001472	022244	DT10	;\$TESTN,\$ERRPC,LKS
845	001474	000000	0	
846				
847	001476	016661	EM34	:"LKS INTERRUPT WITH PRIORITY 7"
848	001500	021575	DH10	:"TEST# ERR PC LKS"
849	001502	022244	DT10	;\$TESTN,\$ERRPC,LKS
850	001504	000000	0	
851				
852	001506	016717	EM35	:"CAN NOT SET BIT6 OF LKS"
853	001510	021575	DH10	:"TEST# ERR PC LKS"
854	001512	022244	DT10	;\$TESTN,\$ERRPC,LKS
855	001514	000000	0	
856				
857	001516	016747	EM36	:"CAN NOT CLEAR BIT6 OF LKS"
858	001520	021575	DH10	:"TEST# ERR PC LKS"
859	001522	022244	DT10	;\$TESTN,\$ERRPC,LKS
860	001524	000000	0	
861				
862	001526	017001	EM37	:"RESET DID NOT CLEAR BIT6 OF LKS"

863	001530	021575	DH10	:"TEST# ERR PC LKS"
864	001532	022244	DT10	:\$TESTN,\$ERRPC,LKS
865	001534	000000	0	
866				
867	001536	017041	EM40	:"DUAL ADDRESSING ERROR"
868	001540	021621	DH40	:"TEST# ERR PC GOOD BAD"
869	001542	022254	DT40	:\$TESTN,\$ERRPC,\$GDADR,\$BDCSR
870	001544	000000	0	
871				
872	001546	017067	EM41	:"BIT7 OF LKS NOT SET AFTER RESET2"
873	001550	021575	DH10	:"TEST# ERR PC LKS"
874	001552	022244	DT10	:\$TESTN,\$ERRPC,LKS
875	001554	000000	0	
876				
877	001556	017127	EM42	:"CAN NOT CLEAR BIT7 OF LKS"
878	001560	021575	DH10	:"TEST# ERR PC LKS"
879	001562	022244	DT10	:\$TESTN,\$ERRPC,LKS
880	001564	000000	0	
881				
882	001566	017161	EM43	:"BIT7 OF LKS DOES NOT SET"
883	001570	021575	DH10	:"TEST# ERR PC LKS"
884	001572	022244	DT10	:\$TESTN,\$ERRPC,LKS
885	001574	000000	0	
886				
887	001576	017212	EM44	:"RTC INTERRUPT AT PRIORITY 7"
888	001600	021575	DH10	:"TEST# ERR PC LKS"
889	001602	022244	DT10	:\$TESTN,\$ERRPC,LKS
890	001604	000000	0	
891				
892	001606	017246	EM45	:"RTC INTERRUPTS WHEN DISABLED"
893	001610	021575	DH10	:"TEST# ERR PC LKS"
894	001612	022244	DT10	:\$TESTN,\$ERRPC,LKS
895	001614	000000	0	
896				
897	001616	017303	EM46	:"RTC INTERRUPT DID NOT OCCUR"
898	001620	021575	DH10	:"TEST# ERR PC LKS"
899	001622	022244	DT10	:\$TESTN,\$ERRPC,LKS
900	001624	000000	0	
901				
902	001626	017303	EM47	:"RTC INTERRUPT DID NOT OCCUR"
903	001630	021575	DH10	:"TEST# ERR PC LKS"
904	001632	022244	DT10	:\$TESTN,\$ERRPC,LKS
905	001634	000000	0	
906				
907	001636	017337	EM50	:"RTC DOUBLE INTERRUPT"
908	001640	021575	DH10	:"TEST# ERR PC LKS"
909	001642	022244	DT10	:\$TESTN,\$ERRPC,LKS
910	001644	000000	0	
911				
912	001646	017364	EM51	:"RESET DID NOT CLEAR RTC INTERRUPT"
913	001650	021575	DH10	:"TEST# ERR PC LKS"
914	001652	022244	DT10	:\$TESTN,\$ERRPC,LKS
915	001654	000000	0	
916				
917	001656	017414	EM52	:"RTC INTERRUPT DID NOT CLEAR WITH BIT7 OF LKS"
918	001660	021575	DH10	:"TEST# ERR PC LKS"

919	001662	022244	DT10	;\$TESTN,\$ERRPC,LKS
920	001664	000000	0	
921				
922	001666	017471	EM53	
923	001670	021655	DH53	;'TEST# ERR PC LKS CNT1 CNT2''
924	001672	022266	DT53	;\$TESTN,\$ERRPC,LKS,FIRST,SECND
925	001674	000000	0	
926				
927	001676	017515	EM54	;'XMIT INTERRUPTS WHEN DISABLED''
928	001700	021451	DH1	;'TEST# ERR PC TCSR''
929	001702	022204	DT1	;\$TESTN,\$ERRPC,TCSR
930	001704	000000	0	
931				
932	001706	017653	EM55	;'XMIT DID NOT INTERRUPT''
933	001710	021451	DH1	;'TEST# ERR PC TCSR''
934	001712	022204	DT1	;\$TESTN,\$ERRPC,TCSR
935	001714	000000	0	
936				
937	001716	017553	EM56	;'XMIT INTERRUPT AT PRIORITY 7''
938	001720	021451	DH1	;'TEST# ERR PC TCSR''
939	001722	022204	DT1	;\$TESTN,\$ERRPC,TCSR
940	001724	000000	0	
941				
942	001726	017611	EM57	;'XMIT INTERRUPTS WITH ENABLE CLEAR''
943	001730	021451	DH1	;'TEST# ERR PC TCSR''
944	001732	022204	DT1	;\$TESTN,\$ERRPC,TCSR
945	001734	000000	0	
946				
947	001736	017653	EM60	;'XMIT DID NOT INTERRUPT''
948	001740	021451	DH1	;'TEST# ERR PC TCSR''
949	001742	022204	DT1	;\$TESTN,\$ERRPC,TCSR
950	001744	000000	0	
951				
952	001746	017702	EM61	;'XMIT RE-INTERRUPTED''
953	001750	021451	DH1	;'TEST# ERR PC TCSR''
954	001752	022204	DT1	;\$TESTN,\$ERRPC,TCSR
955	001754	000000	0	
956				
957	001756	017726	EM62	;'LOADING TBUF DID NOT CLEAR INTERRUPT''
958	001760	021451	DH1	;'TEST# ERR PC TCSR''
959	001762	022204	DT1	;\$TESTN,\$ERRPC,TCSR
960	001764	000000	0	
961				
962	001766	017773	EM63	;'RCVR ACTIVE NOT SET''
963	001770	021523	DH6	;'TEST# ERR PC RCSR''
964	001772	022224	DT6	;\$TESTN,\$ERRPC,RCSR
965	001774	000000	0	
966				
967	001776	020017	EM64	;'RECEIVER DONE NEVER SET''
968	002000	021523	DH6	;'TEST# ERR PC RCSR''
969	002002	022224	DT6	;\$TESTN,\$ERRPC,RCSR
970	002004	000000	0	
971				
972	002006	020043	EM65	;'RCVR ACTIVE NOT CLEARED WITH DONE SET2
973	002010	021523	DH6	;'TEST# ERR PC RCSR''
974	002012	022224	DT6	;\$TESTN,\$ERRPC,RCSR

975	002014	000000	0	
976				
977	002016	020111	EM66	:"RESET DID NOT CLEAR RCVR DONE"
978	002020	021523	DH6	:"TEST# ERR PC RCSR"
979	002022	022224	DT6	:\$TESTN,\$ERRPC,RCSR
980	002024	000000	0	
981				
982	002026	020147	EM67	:"RDR ENABLE SET DID NOT CLEAR RCVR DONE"
983	002030	021523	DH6	:"TEST# ERR PC RCSR"
984	002032	022224	DT6	:\$TESTN,\$ERRPC,RCSR
985	002034	000000	0	
986				
987	002036	020212	EM70	:"READING RBUF DID NOT CLEAR RCVR DONE"
988	002040	021523	DH6	:"TEST# ERR PC RCSR"
989	002042	022224	DT6	:\$TESTN,\$ERRPC,RCSR
990	002044	000000	0	
991				
992	002046	020257	EM71	:"RCVR INTERRUPTS WITH ENABLE CLEAR"
993	002050	021523	DH6	:"TEST# ERR PC RCSR"
994	002052	022224	DT6	:\$TESTN,\$ERRPC,RCSR
995	002054	000000	0	
996				
997	002056	020426	EM72	:"RCVR DID NOT INTERRUPT"
998	002060	021523	DH6	:"TEST# ERR PC RCSR"
999	002062	022224	DT6	:\$TESTN,\$ERRPC,RCSR
1000	002064	000000	0	
1001				
1002	002066	020321	EM73	:"RCVR INTERRUPTS AT PRIORITY 7"
1003	002070	021523	DH6	:"TEST# ERR PC RCSR"
1004	002072	022224	DT6	:\$TESTN,\$ERRPC,RCSR
1005	002074	000000	0	
1006				
1007	002076	020357	EM74	:"RCVR INTERRUPT REQUEST PASSED WITH ENABLE CLEAR"
1008	002100	021523	DH6	:"TEST# ERR PC RCSR"
1009	002102	022224	DT6	:\$TESTN,\$ERRPC,RCSR
1010	002104	000000	0	
1011				
1012	002106	020426	EM75	:"RCVR DID NOT INTERRUPT"
1013	002110	021523	DH6	:"TEST# ERR PC RCSR"
1014	002112	022224	DT6	:\$TESTN,\$ERRPC,RCSR
1015	002114	000000	0	
1016				
1017	002116	020455	EM76	:"RECEIVER RE-INTERRUPTED"
1018	002120	021523	DH6	:"TEST# ERR PC RCSR"
1019	002122	022224	DT6	:\$TESTN,\$ERRPC,RCSR
1020	002124	000000	0	
1021				
1022	002126	020501	EM77	:"READING RBUF DID NOT CLEAR INTERRUPT"
1023	002130	021523	DH6	:"TEST# ERR PC RCSR"
1024	002132	022224	DT6	:\$TESTN,\$ERRPC,RCSR
1025	002134	000000	0	
1026				
1027	002136	020546	EM100	:"RESET DID NOT CLEAR RCVR INTERRUPT"
1028	002140	021523	DH6	:"TEST# ERR PC RCSR"
1029	002142	022224	DT6	:\$TESTN,\$ERRPC,RCSR
1030	002144	000000	0	

1031				
1032				
1033	002146	020611	EM101	;'OR FLAG DID NOT SET'
1034	002150	021523	DH6	
1035	002152	022224	DT6	;\$TESTN,\$ERRPC,RCSR
1036	002154	000000	0	
1037				
1038	002156	020637	EM102	;'ERROR' NOT SET WITH 'OR' FLAG'
1039	002160	021523	DH6	;'TEST# ERR PC RCSR'
1040	002162	022224	DT6	;\$TESTN,\$ERRPC,RCSR
1041	002164	000000	0	
1042				
1043	002166	020676	EM103	;'BREAK DID NOT TRANSMIT ALL ZEROES'
1044	002170	021722	DH103	;'TEST# ERR PC RCSR DATA'
1045	002172	022302	DT103	;\$TESTN,\$ERRPC,RCSR,\$BDDAT
1046	002174	000000	0	
1047				
1048	002176	020734	EM104	;'BREAK DID NOT SET FRAMING ERROR'
1049	002200	021523	DH6	;'TEST# ERR PC RCSR'
1050	002202	022224	DT6	;\$TESTN,\$ERRPC,RCSR
1051	002204	000000	0	
1052				
1053	002206	020771	EM105	;'DATA COMPARE ERROR'
1054	002210	021757	DH105	;'TEST# ERR PC RCSR GOOD BAD'
1055	002212	022314	DT105	;\$TESTN,\$ERRPC,RCSR,GD,BD
1056	002214	000000	0	
1057				
1058	002216	021014	EM106	;'DATA COMPARE ERROR WITH CABLE'
1059	002220	021757	DH105	;'TEST# ERR PC RCSR GOOD BAD'
1060	002222	022314	DT105	;\$TESTN,\$ERRPC,RCSR,GD,BD
1061	002224	000000	0	
1062				
1063	002226	021052	EM107	;'TIMEOUT IN EXERCISER TEST'
1064	002230	021523	DH6	;'TEST# ERR PC RCSR'
1065	002232	022224	DT6	;\$TESTN,\$ERRPC,RCSR
1066	002234	000000	0	
1067				
1068	002236	021104	EM110	;'INCORRECT RECEIVE COUNT
1069	002240	022023	DH110	;'TEST# ERR PC RCSR TRANS RCV'
1070	002242	022330	DT110	;\$TESTN,\$ERRPC,RCSR,XMTCNT,RCVCNT
1071	002244	000000	0	
1072				
1073	002246	021134	EM111	;'DATA COMPARE ERROR IN EXERCISER'
1074	002250	021757	DH105	;'TEST# ERR PC RCSR GOOD BAD'
1075	002252	022314	DT105	;\$TESTN,\$ERRPC,RCSR,GD,BD
1076	002254	000000	0	
1077				
1078	002256	021174	EM112	;'TRAP CATCHER'
1079	002260	022067	DH112	;'TEST# ERR PC RCSR OLDPC TRAP ADR'
1080	002262	022344	DT112	;\$TESTN,\$ERRPC,RCSR,OLDPC,BDVECT
1081	002264	000000	0	
1082				
1083	002266	021211	EM113	;'NO CLK INTERRUPT IN EXERCISER'
1084	002270	021575	DH10	;'TEST# ERR PC LKS'
1085	002272	022244	DT10	;\$TESTN,\$ERRPC,LKS
1086	002274	000000	0	

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1087
1088 002276 021247          EM114          ;''ERROR' NOT SET WITH 'FR' FLAG''
1089 002300 021523          DH6          ;'TEST# ERR PC RCSR''
1090 002302 022224          DT6          ;$TESTN,$ERRPC,RCSR
1091 002304 000000          0
1092
1093 002306 021306          EM115          ;RCV ACTVIE NOT CLEAR WITH INIT
1094 002310 021523          DH6          ;'TEST# ERR PC RCSR''
1095 002312 022224          DT6          ;$TESTN,$ERRPC,RCSR
1096 002314 000000          0
1097
1098 002316 021345          EM116          ;RCV ACTIVE WITHOUT ''START'' BIT
1099 002320 021523          DH6          ;'TEST# ERR PC RCSR''
1100 002322 022224          DT6          ;$TESTN,$ERRPC,RCSR
1101 002324 000000          0
1102
1103 002326 021404          EM117          ;RDR ENABLE NOT CLEAR WITH RCV ACTIVE
1104 002330 021523          DH6          ;'TEST# ERR PC RCSR''
1105 002332 022224          DT6          ;$TESTN,$ERRPC,RCSR
1106 002334 000000          0
1107
1108 002336 000000          CTSTFL: .WORD 0          ;CONSOLE UNDER TEST FLAG
1109 002340 000000          TMP1: .WORD 0          ;TEMP LOCATION FOR TABLE OFFSETS
1110 002342 000000          TMP2: .WORD 0          ;TEMP LOCATION FOR DEVICE COUNT
1111 002344 000000          TMP3: .WORD 0          ;LOCATION FOR DEVICE MAP BIT TEST MASK
1112          ;REGISTER AND VECTOR ADDRESSES FOR THE DL-11W UNDER TEST
1113
1114 002346 000000          RCSR: .WORD 0
1115 002350 000000          RBUF: .WORD 0
1116 002352 000000          TCSR: .WORD 0
1117 002354 000000          TBUF: .WORD 0
1118 002356 000000          RVECT: .WORD 0
1119 002360 000000          RPSW: .WORD 0
1120 002362 000000          TVECT: .WORD 0
1121 002364 000000          TPSW: .WORD 0
1122
1123          ;CONSOLE REGISTER AND VECTOR ADDRESSES FOR THE DL-11W
1124
1125 002366 177560          CRCSR: 177560          ;ADDRESS OF RECEIVER COMMAND/STATUS REGISTER
1126 002370 177562          CRBUF: 177562          ;ADDRESS OF RECEIVER BUFFER
1127 002372 177564          CTCRSR: 177564          ;ADDRESS OF TRANSMITTER COMMAND/STATUS REGISTER
1128 002374 177566          CTBUF: 177566          ;ADDRESS OF TRANSMITTER BUFFER
1129 002376 000060          CRVECT: 60          ;RECEIVER INTERRUPT VECTOR
1130 002400 000062          CRPSW: 62
1131 002402 000064          CTVECT: 64          ;TRANSMITTER INTERRUPT VECTOR
1132 002404 000066          CTPSW: 66
1133
1134          ;REAL TIME CLOCK REGISTER AND VECTOR ADDRESSES
1135 002406 177546          LKS: .WORD 177546
1136 002410 000100          RTCVT: .WORD 100
1137 002412 000102          RTCPSW: .WORD 102
1138
1139 002414 000020          ADRTBL: .BLKW 20
1140 002454 000020          VCTTBL: .BLKW 20
1141
1142
```

ERROR POINTER TABLE

```
1143 ;SUBROUTINE TO GENERATE DEVICE ADDRESS TABLE
1144
1145 002514 012702 002414 DEVADR: MOV #ADRTBL,R2 ;POINT R2 TO THE DEVICE ADDRESS TABLE
1146 002520 013700 001142 MOV $BASE,R0 ;LOAD BASE DEVICE ADDRESS IN R0
1147 002524 010001 MOV R0,R1 ;
1148 002526 062701 000170 ADD #170,R1 ;POINT R1 TO LAST DEVICE ADDRESS
1149 002532 010022 1$: MOV R0,(R2)+ ;MOVE DEVICE ADDRESS TO TABLE
1150 002534 062700 000010 ADD #10,R0 ;POINT R0 TO NEXT DEVICE ADDRESS
1151 002540 020001 CMP R0,R1 ;FINISHED GENERATING TABLE?
1152 002542 003773 BLE 1$ ;BR, IF LAST DEVICE ADDRESS NOT LOADED
1153 002544 000207 RTS PC
1154
1155
1156
1157 002546 005037 001070 START: CLR $FATAL ;CLEAR ERROR NO.
1158 002552 005037 001066 CLR $MSGTYP ;CLEAR MESSAGE TYPE
1159 002556 005037 001072 CLR $TESTN ;CLEAR TEST NO.
1160 002562 005037 002336 CLR CTSTFL ;CLEAR CONSOLE UNDER TEST FLAG
1161 002566 005037 001076 CLR $DEVCT ;CLEAR DEVICE COUNT
1162 002572 005037 001100 CLR $UNIT ;CLEAR UNIT NUMBER
1163 002576 005737 001112 TST $USWR ;IS $USWR LOADED?
1164 002602 001003 BNE 1$ ;BR IF YES
1165 002604 012737 000400 001112 MOV #400,$USWR ;ELSE, DEFAULT TO $USWR=400
1166 002612 012737 000006 000004 1$: MOV #6,@#4 ;INITIALIZE TIMEOUT VECTORS TO TRAP
1167 002620 012737 000003 000006 MOV #3,@#6 ; CATCHER ROUTINE
1168
1169 .SBTTL INITIALIZE THE COMMON TAGS
1170 ;;CLEAR THE COMMON TAGS ($CMTAG) AREA
1171 002626 012706 001000 MOV #$CMTAG,R6 ;;FIRST LOCATION TO BE CLEARED
1172 002632 005026 CLR (R6)+ ;;CLEAR MEMORY LOCATION
1173 002634 022706 001040 CMP #SWR,R6 ;;DONE?
1174 002640 001374 BNE -6 ;;LOOP BACK IF NO
1175 002642 012706 001000 MOV #1000,SP ;;SETUP THE STACK POINTER
1176
1177 ;;INITIALIZE A FEW VECTORS
1177 002646 012737 013000 000020 MOV $$SCOPE,@#IOTVEC ;;IOT VECTOR FOR SCOPE ROUTINE
1178 002654 012737 000340 000022 MOV #340,@#IOTVEC+2 ;;LEVEL 7
1179 002662 012737 012304 000030 MOV $ERROR,@#EMTVEC ;;EMT VECTOR FOR ERROR ROUTINE
1180 002670 012737 000340 000032 MOV #340,@#EMTVEC+2 ;;LEVEL 7
1181 002676 012737 014704 000034 MOV $TRAP,@#TRAPVEC ;;TRAP VECTOR FOR TRAP CALLS
1182 002704 012737 000340 000036 MOV #340,@#TRAPVEC+2;LEVEL 7
1183 002712 012737 012622 000024 MOV $PWRDN,@#PWRVEC ;;POWER FAILURE VECTOR
1184 002720 012737 000340 000026 MOV #340,@#PWRVEC+2 ;;LEVEL 7
1185 002726 013737 012132 012124 MOV $ENDCT,$EOPCT ;;SETUP END-OF-PROGRAM COUNTER
1186 002734 005037 001060 CLR $ESCAPE ;;CLEAR THE ESCAPE ON ERROR ADDRESS
1187 002740 112737 000001 001015 MOV #1,$ERMAX ;;ALLOW ONE ERROR PER TEST
1188 002746 012737 002746 001006 MOV #,$LPADR ;;INITIALIZE THE LOOP ADDRESS FOR SCOPE
1189 002754 012737 002754 001010 MOV #,$LPERR ;;SETUP THE ERROR LOOP ADDRESS
1190
1191 ;;SIZE FOR A HARDWARE SWITCH REGISTER. IF NOT FOUND OR IT IS
1191 ;;EQUAL TO A "-1", SETUP FOR A SOFTWARE SWITCH REGISTER.
1192 002762 013746 000004 MOV @#ERRVEC,-(SP) ;;SAVE ERROR VECTOR
1193 002766 012737 003022 000004 MOV #64,$@#ERRVEC ;;SET UP ERROR VECTOR
1194 002774 012737 177570 001040 MOV #DSWR,SWR ;;SETUP FOR A HARDWARE SWICH REGISTER
1195 003002 012737 177570 001042 MOV #DDISP,DISPLAY ;;AND A HARDWARE DISPLAY REGISTER
1196 003010 022777 177777 176022 CMP #-1,@SWR ;;TRY TO REFERENCE HARDWARE SWR
1197 003016 001012 BNE 66$ ;;BRANCH IF NO TIMEOUT TRAP OCCURRED
1198 ;;AND THE HARDWARE SWR IS NOT = -1
```

INITIALIZE THE COMMON TAGS

```
1199 003020 000403          BR      65$          ;;BRANCH IF NO TIMEOUT
1200 003022 012716 003030    64$:    MOV      #65$, (SP)  ;;SET UP FOR TRAP RETURN
1201 003026 000002          RTI
1202 003030 012737 000176 001040 65$:    MOV      #SWREG,SWR    ;;POINT TO SOFTWARE SWR
1203 003036 012737 000174 001042    MOV      #DISPREG,DISPLAY
1204 003044 012637 000004    66$:    MOV      (SP)+,@#ERRVEC ;;RESTORE ERROR VECTOR
1205
1206 003050 005037 001074          CLR      $PASS        ;;CLEAR PASS COUNT
1207 003054 132737 000200 001107    BITB    #APTSIZE,$ENVM ;;TEST USER SIZE UNDER APT
1208 003062 001403          BEQ      67$          ;;YES,USE NON-APT SWITCH
1209 003064 012737 001110 001040    MOV      #$$SWREG,SWR  ;;NO,USE APT SWITCH REGISTER
1210 003072
1211 003072 032777 000020 175740    67$:    BIT      #BIT4,@SWR    ;TEST CLOCK ONLY?
1212 003100 001404          BEQ      INIT        ;BR IF NOT
1213 003102 005237 002336          INC      CTSTFL      ;ELSE, SET CONSOLE TEST FLAG TO ENABLE CLOCK TESTS
1214 003106 000137 004056          JMP      ID          ; AND JUMP TO TYPE PROGRAM ID
1215 003112 132737 000001 001106    INIT:   BITB    #BIT0,$ENV  ;CHECK IF ON APT
1216 003120 001404          BEQ      MANL        ;BR IF NOT APT
1217 003122 132737 000200 001107    BITB    #BIT7,$ENVM   ;DID APT SIZE
1218 003130 001056          BNE      APTSZD      ;BR, IF APT SIZED
1219 003132 032777 000040 175700    MANL:   BIT      #BIT5,@SWR ;WAS "$DEVN" MANUALLY SET?
1220 003140 001052          BNE      APTSZD      ;IF YES, SKIP SELF-SIZING
1221
1222 003142 004737 002514    SIZE:   JSR      PC,DEVADR  ;GENERATE DEVICE ADDRESS TABLE
1223 003146 005037 002342          CLR      TMP2        ;CLR TEMP LOCATION TO KEEP DEVICE COUNT
1224 003152 005037 001144          CLR      $DEVN       ;CLEAR DEVICE MAP
1225 003156 013703 000004          MOV      @#4,R3      ;SAVE TIMEOUT VECTOR
1226 003162 012737 003212 000004    MOV      #4,@#4      ;SET TIMEOUT POINTER
1227 003170 013700 001142          MOV      $BASE,R0    ;LOAD BASE ADDRESS
1228 003174 062700 000160          ADD      #160,R0     ;POINT R0 TO UNIT #15 (UNIT#0=CONSOLE)
1229 003200 005710    3$:    TST      (R0)        ;CHECK FOR DEVICE EXISTANCE
1230 003202 005237 001144          INC      $DEVN       ;INDICATE DEVICE EXISTANCE IN DEVICE MAP
1231 003206 005237 002342          INC      TMP2        ;INCREMENT DEVICE COUNT
1232 003212 012706 001000    4$:    MOV      #1000,SP    ;RESET STACK POINTER
1233 003216 006337 001144          ASL      $DEVN       ;ADJUST DEVICE MAP FOR NEXT UNIT CHECK
1234 003222 162700 000010          SUB      #10,R0      ;POINT R0 TO NEXT DEVICE NUMBER
1235 003226 023700 001142          CMP      $BASE,R0    ;FINISHED SIZING?
1236 003232 003762          BLE      3$         ;BR, IF BASE ADDRESS HAS NOT BEEN CHECKED
1237 003234 013700 002366          MOV      CRCSR,R0    ;LOAD CONSOLE DEVICE ADDRESS
1238 003240 012737 003260 000004    MOV      #5,@#4      ;SET UP TIMEOUT POINTER
1239 003246 005710          TST      (R0)        ;TEST FOR CONSOLE EXISTANCE
1240 003250 005237 001144          INC      $DEVN       ;INDICATE CONSOLE EXISTANCE IN DEVICE MAP
1241 003254 005237 002342          INC      TMP2        ;INCREMENT DEVICE COUNT
1242 003260 010337 000004    5$:    MOV      R3,@#4      ;RESTORE TIMEOUT VECTOR
1243 003264 000415          BR      VCTADR       ;BR TO GENERATE VECTOR ADDRESS TABLE
1244
1245 003266 005037 002342    APTSZD: CLR      TMP2        ;CLEAR TEMP LOCATION TO KEEP DEVICE CNT
1246 003272 013702 001144          MOV      $DEVN,R2    ;MOVE DEVICE MAP TO R2
1247 003276 005702    TSTDVM: TST      R2      ;TEST MSB OF DEVICE MAP
1248 003300 100002          BPL      1$         ;BR, IF MSB IS ZERO
1249 003302 005237 002342          INC      TMP2        ;INCREMENT DEVICE COUNT, IF MSB=1
1250 003306 006302    1$:    ASL      R2          ;SHIFT NEXT BIT INTO MSB POSITION
1251 003310 001401          BEQ      DVADT       ;BR, IF NO OTHER BITS ARE SET IN $DEVN
1252 003312 000771          BR      TSTDVM      ;CONTINUE CHECKING $DEVN, IF MORE BITS SET
1253 003314 004737 002514    DVADT: JSR      PC,DEVADR ;GENERATE DEVICE ADDRESS TABLE
1254
```

INITIALIZE THE COMMON TAGS

```
1255 ;GENERATE VECTOR ADDRESS TABLE
1256
1257 003320 012702 002454 VCTADR: MOV #VCTTBL,R2 ;GET LOCATION OF VECTOR TABLE
1258 003324 113700 001136 MOVB @#$VECT1,R0 ;COPY BASE VECTOR
1259 003330 042700 177400 BIC #177400,R0 ;CLEAR BYTE SIGN EXTENSION
1260 003334 010001 MOV R0,R1 ;
1261 003336 062701 000170 ADD #170,R1 ;POINT R1 TO LAST DEVICE VECTOR
1262 003342 010022 1$: MOV R0,(R2)+ ;PUT VECTOR ADDRESS IN TABLE
1263 003344 062700 000010 ADD #10,R0 ;POINT R0 TO NEXT VECTOR ADDRESS
1264 003350 020001 CMP R0,R1 ;FINISHED GENERATING VECTOR TABLE?
1265 003352 003773 BLE 1$ ;BR, IF LAST VECTOR IS NOT LOADED
1266
1267 ;MOVE DEVICE COUNT INTO DEVICE COUNT MESSAGE
1268
1269 003354 013700 002342 MOV TMP2,R0 ;COPY DEVICE COUNT INTO R0
1270 003360 005001 CLR R1 ;CLEAR AUXILARY REGISTER
1271 003362 000300 SWAB R0 ;PUT DEVICE COUNT IN UPPER BYTE OF R0
1272 003364 006300 ASL R0 ;MOVE MSB OF COUNT INTO
1273 003366 006300 ASL R0 ;MSB OF R0
1274 003370 006300 SHIFT: ASL R0 ;PUT MSB OF COUNT INTO CARRY
1275 003372 106101 ROLB R1 ;MOVE MSB OF COUNT INTO R1
1276 003374 006300 ASL R0 ;MOVE NEXT BIT TO CARRY
1277 003376 106101 ROLB R1 ;MOVE INTO R1
1278 003400 006300 ASL R0 ;MOVE LAST BIT OF DIGIT
1279 003402 106101 ROLB R1 ;INTO R1
1280 003404 062701 000060 ADD #60,R1 ;CONVERT DIGIT TO ASCII
1281 003410 000301 SWAB R1 ;MOVE DIGIT TO UPPER BYTE
1282 003412 032701 000020 BIT #BIT4,R1 ;HAVE BOTH DIGITS BEEN MOVED TO R1?
1283 003416 001764 BEQ SHIFT ;BR, IF NOT
1284 003420 010137 022154 MOV R1,M2A ;MOVE DEVICE COUNT TO OUTPUT MESSAGE
1285
1286
1287 003424 052737 000002 002344 BEGIN: BIS #BIT1,TMP3 ;SET UP BIT MASK TO TEST $DEVN FOR DEVICES EXCEPT CONSOL
1288 003432 005037 002340 CLR TMP1 ;CLEAR LOCATION TO STORE TABLE OFFSETS
1289 003436 032737 000001 001144 BIT #BIT0,$DEVN ;IS CONSOLE TO BE TESTED?
1290 003444 001001 BNE TCONS ;BR, IF CONSOLE IS TO BE TESTED
1291 003446 000414 BR TSTDEV ;BR, TO TEST OTHER DEVICES
1292 003450 005237 002336 TCONS: INC CTSTFL ;INDICATE CONSOLE UNDER TEST
1293 003454 012700 002366 MOV #CRCSR,R0 ;SET UP CONSOLE DEVICE ADDRESSES
1294 003460 012701 002346 MOV #RCSR,R1 ;POINT R1 TO UUT ADDRESS TABLE
1295 003464 012021 1$: MOV (R0)+,(R1)+ ;TRANSFER CONSOLE ADDRESSES
1296 003466 022701 002364 CMP #TPSW,R1 ;FINISHED TRANSFER?
1297 003472 002374 BGE 1$ ;BR, IF NOT
1298 003474 000137 003622 JMP TST1 ;GO TEST CONSOLE INTERFACE
1299
1300 ;PREPARE ADDRESSES AND VECTORS FOR UUT
1301 003500 033737 002344 001144 TSTDEV: BIT TMP3,$DEVN ;CHECK TO SEE IF DEVICE IS TO BE TESTED
1302 003506 001010 BNE SETADR ;BR, IF YES
1303 003510 006337 002344 ASL TMP3 ;SHIFT MASK TO CHECK NEXT $DEVN BIT
1304 003514 062737 000002 002340 ADD #2,TMP1 ;INCREMENT TABLE INDEX
1305 003522 005237 001100 INC $UNIT ;INCREMENT UNIT NUMBER
1306 003526 000764 BR TSTDEV ;GO TEST NEXT BIT OF DEVICE MAP
1307
1308 003530 005237 001100 SETADR: INC $UNIT ;UPDATE UNIT NUMBER
1309 003534 006337 002344 ASL TMP3 ;UPDATE DEVICE MAP TEST MASK
1310 003540 013702 002340 MOV TMP1,R2 ;MOVE TABLE OFFSET TO R2
```

INITIALIZE THE COMMON TAGS

```
1311 003544 062737 000002 002340      ADD    #2,TMP1      ;UPDATE TABLE OFFSET FOR NEXT DEVICE
1312 003552 016200 002414              MOV    ADRTBL(R2),R0 ;PUT UUT ADDRESS INTO R0
1313 003556 012701 002346              MOV    #RCSR,R1     ;POINT R1 TO STORAGE AREA FOR UUT ADDRESSES
1314 003562 010021              ADR:  MOV    R0,(R1)+ ;TRANSFER UUT ADDRESS
1315 003564 062700 000002              ADD    #2,R0        ;POINT TO NEXT UUT REGISTER
1316 003570 030027 000006              BIT    R0,#6        ;FINISHED TRANSFER?
1317 003574 001372              BNE    ADR          ;BR, IF NOT
1318
1319 003576 016200 002454              MOV    VCTTBL(R2),R0 ;PUT UUT VECTOR INTO R0
1320 003602 010021              VECT: MOV    R0,(R1)+ ;TRANSFER UUT VECTORS TO ACTIVE TABLE AREA
1321 003604 062700 000002              ADD    #2,R0        ;POINT TO NEXT VECTOR
1322 003610 030027 000006              BIT    R0,#6        ;FINISHED TRANSFER?
1323 003614 001372              BNE    VECT        ;BR, IF NOT
1324 003616 000137 003622              JMP    TST1        ;GO TEST DEVICE
1325
1326
```

INITIALIZE THE COMMON TAGS

```
1327
1328
1329
1330
1331
1332 003622 000004
1333 003624 013703 000004
1334 003630 012737 003644 000004
1335 003636 005777 176510
1336 003642 000412
1337
1338 003644 022626
1339 003646 005737 002336
1340 003652 001002
1341 003654 104001
1342 003656 000404
1343 003660
1344 003660 004737 013170
1345 003664 000001
1346 003666 000000
1347 003670 010337 000004
1348
1349
1350
1351
1352
1353
1354 003674 000004
1355 003676 013703 000004
1356 003702 012737 003716 000004
1357 003710 005777 176440
1358 003714 000412
1359
1360 003716 022626
1361 003720 005737 002336
1362 003724 001002
1363 003726 104002
1364 003730 000404
1365 003732
1366 003732 004737 013170
1367 003736 000002
1368 003740 000000
1369 003742 010337 000004

;*****
;*TEST 1 TEST ABILITY TO REFERENCE TCSR
;*****
TST1: SCOPE
MOV @#4,R3 ;SAVE TIMEOUT VECTOR
MOV #1$,@#4 ;SET UP TIMEOUT VECTOR
TST @TCSR ;REFERENCE THE XMIT COMMAND/STATUS REG.
BR 4$ ;GO TO END OF TEST

1$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT
TST CTSTFL ;CHECK IF DEVICE IS CONSOLE
BNE 2$ ;IF YES, SKIP ERROR TYPEOUT
ERROR 1 ;REPORT ERROR TO APT & TTY
BR 4$ ;BR TO END OF TEST

2$: JSR PC,$ATY4 ;;ONLY REPORT A FATAL ERROR
1 ;;THE ERROR NUMBER (FROM APT LIST)

3$: HALT
4$: MOV R3,@#4 ;RESTORE TIMEOUT VECTOR

;*****
;*TEST 2 TEST ABILITY TO REFERENCE TBUF
;*****
TST2: SCOPE
MOV @#4,R3 ;SAVE TIMEOUT VECTOR
MOV #1$,@#4 ;SET UP TIMEOUT VECTOR
TST @TBUF ;REFERENCE THE XMIT BUFFER
BR 4$ ;GO TO END OF TEST

1$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT
TST CTSTFL ;CHECK IF DEVICE IS CONSOLE
BNE 2$ ;IF YES, SKIP ERROR TYPEOUT
ERROR 2 ;REPORT ERROR TO APT & TTY
BR 4$ ;BR TO END OF TEST

2$: JSR PC,$ATY4 ;;ONLY REPORT A FATAL ERROR
2 ;;THE ERROR NUMBER (FROM APT LIST)

3$: HALT
4$: MOV R3,@#4 ;RESTORE TIMEOUT VECTOR
```

```
1370
1371
1372
1373
1374
1375 003746 000004
1376 003750 005077 176400
1377 003754 105777 176372
1378 003760 100016
1379
1380
1381 003762 005077 176366
1382 003766 105777 176360
1383 003772 100011
1384
1385 003774 005737 002336
1386 004000 001002
1387 004002 104003
1388 004004 000404
1389 004006
1390 004006 004737 013170
1391 004012 000003
1392 004014 000000
1393 004016 005000
1394 004020 105777 176326
1395 004024 100414
1396 004026 005200
1397 004030 001373
1398
1399 004032 005737 002336
1400 004036 001002
1401 004040 104004
1402 004042 000405
1403 004044
1404 004044 004737 013170
1405 004050 000004
1406 004052 000000
1407 004054 000424
1408
1409
1410 004056 023737 000042 000046 ID:
1411 004064 001412
1412 004066 005737 001074
1413 004072 001007
1414 004074 005737 001076
1415 004100 001004
1416 004102 104401
1417 004104 022140
1418 004106 104401
1419 004110 022152
1420 004112 032777 000020 174720 6$:
1421 004120 001402
1422 004122 000137 005056

;*****
;*TEST 3 TEST THAT TCSR BIT7(DONE) CLEARS WHEN XBUF IS LOADED
;*****
TST3: SCOPE
      CLR @TBUF ;LOAD XBUF
      TSTB @TCSR ;CHECK DONE
      BPL 3$ ;BR IF CLEAR
      ;FILL SECOND BUFFER, BECAUSE REFRESH COULD CAUSE
      ; FIRST TEST TO FAIL
      CLR @TBUF ;FILL DOUBLE BUFFER
      TSTB @TCSR ;CHECK DONE
      BPL 3$ ;BR IF CLEAR

      TST CTSTFL ;CHECK IF DEVICE IS CONSOLE
      BNE 1$ ;IF YES, SKIP ERROR TYPEOUT
      ERROR 3 ;DONE NOT CLEARED WITH TBUF FULL
      BR 2$ ;BR TO END OF TEST

1$: JSR PC,$ATY4 ;:ONLY REPORT A FATAL ERROR
      3 ;:THE ERROR NUMBER (FROM APT LIST)
2$: HALT ;TCSR "DONE" NOT CLEARED WITH TBUF FULL
3$: CLR R0 ;CLEAR TIMER
4$: TSTB @TCSR ;CHECK FOR XMIT DONE
      BMI ID ;IF DONE SETS, BR TO END OF TEST
      INC R0 ;INCREMENT TIMER
      BNE 4$ ;BR IF TIMER NOT DONE

      TST CTSTFL ;CHECK IF DEVICE IS CONSOLE
      BNE 5$
      ERROR 4 ;TCSR "DONE" DOES NOT SET
      BR ID ;BR TO END OF TEST

5$: JSR PC,$ATY4 ;:ONLY REPORT A FATAL ERROR
      4 ;:THE ERROR NUMBER (FROM APT LIST)
      HALT
      BR TST4 ;BR TO NEXT TEST, AND SKIP THE TYPEOUT THAT FOLLOWS
      ; BECAUSE OF THIS FAILURE

      CMP @#42,@#46 ;UNDER ACT11?
      BEQ 6$ ;IF YES, SKIP IDENT. TYPEOUT
      TST $PASS ;IS THIS THE FIRST PASS?
      BNE 6$ ;IF NOT BR TO NEXT TEST & SKIP THE IDENTIFICATION TYPEOU
      TST $DEVCT ;IS THIS THE FIRST SUBPASS?
      BNE 6$ ;IF NOT, BR TO NEXT TEST
      TYPE ;TYPE PROGRAM IDENTIFICATION
      M1 ;TYPE NUMBER OF DEVICES UNDER TEST
      TYPE
      M2
      BIT #BIT4,@SWR ;CLOCK TEST ONLY?
      BEQ TST4 ;BR IF NOT
      JMP TCLOCK ;ELSE, JUMP TO TEST CLOCK
```

TEST THAT TCSR BIT7(DONE) CLEARS WHEN XBUF IS LOADED

```
1423
1424
1425
1426      ;*****
1427      ;*TEST 4      TEST THAT TCSR "DONE" SETS WITH RESET
1428      ;*****
1428 004126 000004
1429 004130 005077 176220
1430 004134 105777 176212
1431 004140 100375
1432 004142 005077 176206
1433 004146 000240
1434 004150 000005
1435 004152 105777 176174
1436 004156 100401
1437
1438 004160 104005
1439
1440
1441
1442      ;*****
1443      ;*TEST 5      TEST ABILITY TO ACCESS RCSR
1444      ;*****
1445 004162 000004
1446 004164 013703 000004
1447 004170 012737 004204 000004
1448 004176 005777 176144
1449 004202 000402
1450
1451 004204 022626
1452 004206 104006
1453 004210 010337 000004

TST4:  SCOPE
      CLR @TBUF ;LOAD TRANSMIT BUFFER
1$:    TSTB @TCSR ;WAIT FOR DONE
      BPL 1$
      CLR @TBUF ;LOAD SECOND BUFFER
      NOP
      RESET ;CLEAR DONE WITH RESET
      TSTB @TCSR ;CHECK FOR DONE SET
      BMI TST5 ;BR TO NEXT TEST IF DONE SET

      ERROR 5 ;TCSR "DONE" DOES NOT SET WITH RESET

TST5:  SCOPE
      MOV @#4,R3 ;SAVE TIMEOUT VECTOR
      MOV #1$,@#4 ;SET UP TIMEOUT VECTOR
      TST @RCSR ;ACCESS RCSR
      BR 2$ ;BR TO END OF TEST

1$:    CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT
      ERROR 6 ;CAN NOT ACCESS RCSR
2$:    MOV R3,@#4 ;RESTORE TIMEOUT VECTOR
```

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```
*****  
*TEST 6 TEST ABILITY TO ACCESS RBUF  
*****  
TST6: SCOPE  
MOV @#4,R3 ;SAVE TIMEOUT VECTOR  
MOV #1$,@#4 ;SET UP TIMEOUT VECTOR  
TST @RBUF ;ACCESS RBUF  
BR 2$ ;BR TO END OF TEST  
  
1$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT  
ERROR 7 ;CAN NOT ACCESS RBUF  
2$: MOV R3,@#4 ;RESTORE TIMEOUT VECTOR
```

```

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1475          ;:*****
1476          ;*TEST 7      TEST THAT BIT0(BREAK BIT) CAN BE SET & CLEARED & RESET
1477          ;:*****
1477 004246 000004          TST7:  SCOPE
1478 004250 032777 000400 174562      BIT      #BIT8,@SWR      ;IS BREAK FUNCTION ENABLED?
1479 004256 001545          BEQ      TST11          ;BR TO NEXT TEST, IF NOT
1480 004260 000005          RESET          ;CLEAR EVERYTHING
1481 004262 032777 000001 176062      BIT      #BIT0,@TCSR   ;CHECK BIT0 OF TCSR CLEAR
1482 004270 001411          BEQ      3$           ;BR IF CLEAR
1483 004272 005737 002336          TST      CTSTFL
1484 004276 001002          BNE      1$           .
1485 004300 104011          ERROR    11          ;BIT0 WAS NOT CLEAR AFTER RESET
1486 004302 000404          BR       3$
1487 004304          1$:
1488 004304 004737 013170          JSR      PC,$ATY4          ;;ONLY REPORT A FATAL ERROR
1489 004310 000011          11          ;;THE ERROR NUMBER (FROM APT LIST)
1490 004312 000000          2$:  HALT
1491
1492 004314 052777 000001 176030      3$:  BIS      #BIT0,@TCSR   ;SET BIT0 IN TCSR
1493 004322 032777 000001 176022      BIT      #BIT0,@TCSR   ;TEST BIT0 OF TCSR
1494 004330 001001          BNE      4$           ;BR IF SET
1495
1496 004332 104012          ERROR    12          ;BIT0 OF TCSR WILL NOT SET
1497
1498 004334 042777 000001 176010      4$:  BIC      #BIT0,@TCSR   ;CLEAR BIT0 OF TCSR
1499 004342 032777 000001 176002      BIT      #BIT0,@TCSR   ;TEST BIT0 OF TCSR
1500 004350 001411          BEQ      7$           !
1501 004352 005737 002336          TST      CTSTFL
1502 004356 001002          BNE      5$           .
1503 004360 104013          ERROR    13          ;BIT0 OF TCSR WILL NOT CLEAR
1504 004362 000404          BR       7$
1505 004364          5$:
1506 004364 004737 013170          JSR      PC,$ATY4          ;;ONLY REPORT A FATAL ERROR
1507 004370 000013          13          ;;THE ERROR NUMBER (FROM APT LIST)
1508 004372 000000          6$:  HALT
1509
1510 004374 052777 000001 175750      7$:  BIS      #BIT0,@TCSR   ;SET BIT0 IN TCSR
1511 004402 000005          RESET          ;CLEAR BIT0 WITH RESET
1512 004404 032777 000001 175740      BIT      #BIT0,@TCSR   ;TEST BIT0 CLEAR
1513 004412 001467          BEQ      TST11          ;BR IF CLEAR
1514 004414 042777 000001 175730      BIC      #BIT0,@TCSR   ;CLEAR BIT0, TO PRINT ERROR
1515 004422 104014          ERROR    14          ;RESET DID NOT CLEAR BIT0 OF TCSR
  
```

TEST THAT BIT0(BREAK BIT) CAN BE SET & CLEARED & RESET

```
1516
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1519          ;:*****
1520          ;*TEST 10      TEST THAT BIT2(MAINT. BIT) CAN BE SET & RESET
1521          ;:*****
1521 004424 000004          TST10: SCOPE
1522 004426 000005          RESET          ;CLEAR EVERYTHING
1523 004430 032777 000004 175714      BIT      #BIT2,@TCSR      ;TEST FOR BIT2 OF TCSR CLEAR
1524 004436 001411          BEQ      3$          ;BR IF CLEAR
1525
1526 004440 005737 002336          TST      CTSTFL          ;CHECK IF DEVICE IS CONSOLE
1527 004444 001002          BNE      1$          ;IF YES, SKIP ERROR TYPEOUT
1528 004446 104015          ERROR     15          ;BIT2 OF TCSR NOT CLEAR AFTER RESET
1529 004450 000404          BR      3$
1530
1531 004452          1$:
1532 004452 004737 013170          JSR      PC,$ATY4          ;:ONLY REPORT A FATAL ERROR
1533 004456 000015          15          ;:THE ERROR NUMBER (FROM APT LIST)
1534 004460 000000          2$: HALT
1535
1536 004462 052777 000004 175662      3$: BIS      #BIT2,@TCSR      ;SET BIT2 OF TCSR
1537 004470 032777 000004 175654      BIT      #BIT2,@TCSR      ;TEST FOR BIT2 SET
1538 004476 001001          BNE      4$          ;BR IF SET
1539
1540 004500 104016          ERROR     16          ;BIT2 OF TCSR WILL NOT SET
1541
1542 004502 042777 000004 175642      4$: BIC      #BIT2,@TCSR      ;CLEAR BIT2 OF TCSR
1543 004510 032777 000004 175634      BIT      #BIT2,@TCSR      ;TEST BIT2 CLEAR
1544 004516 001411          BEQ      7$          ;BR IF CLEAR
1545
1546 004520 005737 002336          TST      CTSTFL          ;CHECK IF DEVICE IS CONSOLE
1547 004524 001002          BNE      5$          ;IF YES, SKIP ERROR TYPEOUT
1548 004526 104017          ERROR     17
1549 004530 000404          BR      7$
1550
1551 004532 004737 013170          5$: JSR      PC,$ATY4          ;:ONLY REPORT A FATAL ERROR
1552 004536 000017          17          ;:THE ERROR NUMBER (FROM APT LIST)
1553 004540 000000          6$: HALT          ;BIT0 OF TCSR WILL NOT CLEAR
1554
1555 004542 052777 000004 175602      7$: BIS      #BIT2,@TCSR      ;SET BIT2 OF TCSR
1556 004550 000005          RESET          ;CLEAR BIT2 WITH RESET
1557 004552 032777 000004 175572      BIT      #BIT2,@TCSR      ;TEST FOR BIT2 CLEAR
1558 004560 001461          BEQ      TST12          ;IF CLEAR, GO TO NEXT TEST
1559
1560 004562 042777 000004 175562          BIC      #BIT2,@TCSR      ;CLEAR BIT2, TO PRINT ERROR
1561 004570 104020          ERROR     20
1562          ;RESET DID NOT CLEAR BIT2 OF TCSR
```

TEST THAT BIT2(MAINT. BIT) CAN BE SET & RESET

```
1563
1564
1565
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1568 004572 000004
1569 004574 000005
1570 004576 017703 175560
1571 004602 012777 004632 175552
1572 004610 004737 012242
1573 004614 000340
1574 004616 032777 000100 175526
1575 004624 001404
1576 004626 104021
1577
1578 004630 000402
1579
1580 004632 022626 1$:
1581 004634 104022
1582
1583
1584 004636 052777 000100 175506 2$:
1585 004644 032777 000100 175500
1586 004652 001001
1587
1588 004654 104023
1589
1590
1591 004656 042777 000100 175466 3$:
1592 004664 032777 000100 175460
1593 004672 001401
1594 004674 104024
1595
1596
1597 004676 052777 000100 175446 4$:
1598 004704 000005
1599 004706 032777 000100 175436
1600 004714 001401
1601
1602 004716 104025
1603
1604 004720 010377 175436 5$:
```

```
*****
*TEST 11 TEST THAT BIT6(XMIT INT EN) CAN BE SET & RESET
*****
TST11: SCOPE
        RESET ;CLEAR EVERYTHING
        MOV @TVECT,R3 ;SAVE XMIT VECTOR
        MOV #1$,@TVECT ;SET UP INTERRUPT VECTOR FOR ERROR REPORT
        JSR PC,WRPSW ;SET PSW TO PRIORITY=7
        .WORD 340
        BIT #BIT6,@TCSR ;TEST BIT6 OF TCSR
        BEQ 2$ ;BR IF ZERO
        ERROR 21 ;BIT6 IN TCSR NOT CLEAR AFTER RESET
        BR 2$
        CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
        ERROR 22
        ;XMIT INTERRUPT OCCURRED PRIO=7
        BIS #BIT6,@TCSR ;SET BIT6 OF TCSR
        BIT #BIT6,@TCSR ;TEST BIT6 OF TCSR
        BNE 3$ ;BR, IF SET
        ERROR 23
        ;CANNOT SET BIT6 OF TCSR
        BIC #BIT6,@TCSR ;CLEAR BIT6 OF TCSR
        BIT #BIT6,@TCSR ;TEST BIT6 OF TCSR
        BEQ 4$ ;BR IF CLEAR
        ERROR 24
        ;CANNOT CLEAR BIT6 OF TCSR
        BIS #BIT6,@TCSR ;SET BIT6 OF TCSR
        RESET ;CLEAR BIT6 WITH RESET
        BIT #BIT6,@TCSR ;TEST BIT6 OF TCSR
        BEQ 5$ ;BR IF CLEAR
        ERROR 25
        ;CANNOT CLEAR BIT6 OF TCSR WITH RESET
        MOV R3,@TVECT ;RESTORE XMIT VECTOR
```

```
1605
1606
1607
1608      ;*****
1609      ;*TEST 12      TEST THAT BIT6 OF RCSR CAN BE SET & RESET
1610      ;*****
1610      TST12:  SCOPE
1611              RESET                ;CLEAR EVERYTHING
1612      004724 000004
1613      004726 000005
1614      004730 017703 175422      MOV      @RVECT,R3      ;SAVE RECEIVE VECTOR
1615      004734 012777 004764 175414  MOV      #1$,@RVECT    ;SET UP INTERRUPT VECTOR FOR ERROR REPORT
1616      004742 004737 012242      JSR      PC,WRPSW      ;SET PSW TO PRIORITY=7
1617      004746 000340
1618      004750 032777 000100 175370  .WORD   340
1619      004756 001404      BIT      #BIT6,@RCSR   ;TEST BIT6 OF RCSR
1620      004760 104026      BEQ     2$
1621
1622              ERROR     26
1623
1624              ;BIT6 OF RCSR NOT CLEAR AFTER RESET
1625      004762 000402      BR      2$
1626
1627      004764 022626      1$:    CMP      (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
1628      004766 104027      ERROR   27
1629
1630              ;RCVR INTERRUPT WITH PRIORITY=7
1631      004770 052777 000100 175350  2$:    BIS      #BIT6,@RCSR ;SET BIT6 OF RCSR
1632      004776 032777 000100 175342  BIT      #BIT6,@RCSR   ;TEST BIT6 OF RCSR
1633      005004 001001      BNE     3$              ;BR, IF SET
1634
1635              ERROR     30
1636
1637              ;CANNOT SET BIT6 OF RCSR
1638      005010 042777 000100 175330  3$:    BIC      #BIT6,@RCSR ;CLEAR BIT6 OF RCSR
1639      005016 032777 000100 175322  BIT      #BIT6,@RCSR   ;TEST BIT6 OF RCSR
1640      005024 001401      BEQ     4$              ;BR, IF CLEAR
1641
1642              ERROR     31
1643
1644              ;CANNOT CLEAR BIT6 OF RCSR
1645      005030 052777 000100 175310  4$:    BIS      #BIT6,@RCSR ;SET BIT6 OF RCSR
1646      005036 000005      RESET   ;CLEAR BIT6 OF RCSR WITH RESET
1647      005040 032777 000100 175300  BIT      #BIT6,@RCSR   ;TEST BIT6 OF RCSR
1648      005046 001401      BEQ     5$              ;BR, IF CLEAR
1649
1650              ERROR     32
1651
1652              ;CANNOT CLEAR BIT6 OF RCSR WITH RESET
1653      005052 010377 175300      5$:    MOV      R3,@RVECT ;RESTORE RECEIVE VECTOR
1654
```

TEST THAT BIT6 OF RCSR CAN BE SET & RESET

```
1649
1650 005056 012737 000012 001002 TCLOCK: MOV #12,$TSTNM ;ADJUST TEST NUMBER TO (NEXT TEST - 1)
1651 ;*****
1652 ;*TEST 13 TEST ABILITY TO ACCESS LKS
1653 ;*****
1654 005064 000004 TST13: SCOPE
1655 005066 005737 002336 TST CTSTFL ;IS CONSOLE UNDER TEST?
1656 005072 001420 BEQ TST14 ;IF NOT, SKIP THIS TEST
1657 005074 032777 000100 173736 BIT #BIT6,@SWR ;ARE LINE CLOCK TESTS INHIBITED?
1658 005102 001014 BNE TST14 ;IF YES, SKIP THIS TEST
1659 005104 013703 000004 MOV @#4,R3 ;SAVE TIMEOUT VECTOR
1660 005110 012737 005124 000004 MOV #1$,@#4 ;SET UP TIMEOUT VECTOR
1661 005116 005777 175264 TST @LKS ;ACCESS LKS
1662 005122 000402 BR 2$ ;NO TIMEOUT - BR TO END OF TEST
1663
1664 005124 022626 1$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT
1665 005126 104010 ERROR 10 ;CAN NOT ACCESS LKS
1666
1667 005130 010337 000004 2$: MOV R3,@#4 ;RESTORE TIMEOUT VECTOR
1668
1669 ;*****
1670 ;*TEST 14 TEST THAT BIT6 OF LKS CAN BE SET & RESET
1671 ;*****
1672 005134 000004 TST14: SCOPE
1673 005136 005737 002336 TST CTSTFL ;IS CONSOLE UNDER TEST?
1674 005142 001460 BEQ TST15 ;IF NOT, SKIP THIS TEST
1675 005144 032777 000100 173666 BIT #BIT6,@SWR ;ARE LINE CLOCK TESTS INHIBITED?
1676 005152 001054 BNE TST15 ;IF YES, SKIP THIS TEST
1677 005154 000005 RESET
1678 005156 017703 175226 MOV @ARTCVT,R3 ;SAVE LINE CLOCK VECTOR
1679 005162 012777 005212 175220 MOV #1$,@ARTCVT ;SET UP INTERRUPT VECTOR FOR ERROR REPORT
1680 005170 004737 012242 JSR PC,WRPSW ;SET PSW TO PRIORITY 7
1681 005174 000340 .WORD 340
1682 005176 032777 000100 175202 BIT #BIT6,@LKS ;TEST BIT6 OF LKS
1683 005204 001404 BEQ 2$
1684 005206 104033 ERROR 33
1685 ;BIT6 OF LKS NOT CLEAR AFTER RESET
1686 005210 000402 BR 2$
1687
1688 005212 022626 1$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
1689 005214 104034 ERROR 34 ;LKS INTERRUPT WITH PRIORITY=7
1690
1691
1692 005216 052777 000100 175162 2$: BIS #BIT6,@LKS ;SET BIT6 OF LKS
1693 005224 032777 000100 175154 BIT #BIT6,@LKS ;TEST BIT6 OF LKS
1694 005232 001001 BNE 3$ ;BR IF SET
1695
1696 005234 104035 ERROR 35
1697 ;CANNOT SET BIT6 OF LKS
1698
1699 005236 042777 000100 175142 3$: BIC #BIT6,@LKS ;CLEAR BIT6 OF LKS
1700 005244 032777 000100 175134 BIT #BIT6,@LKS ;TEST BIT6 OF LK
1701 005252 001401 BEQ 4$
1702 005254 104036 ERROR 36
1703 ;CANNOT CLEAR BIT6 OF LKS
1704 005256 052777 000100 175122 4$: BIS #BIT6,@LKS ;SET BIT6 OF LKS
```

TEST THAT BIT6 OF LKS CAN BE SET & RESET

1705	005264	000005			RESET			;CLEAR BIT6 OF LKS WITH RESET
1706	005266	032777	000100	175112	BIT	#BIT6,@LKS		;TEST BIT6 OF LKS
1707	005274	001401			BEQ	5\$;BR IF CLEAR
1708								
1709	005276	104037			ERROR	37		
1710								
1711	005300	010377	175104	5\$:	MOV	R3,@RTCVT		;CANNOT CLEAR BIT6 OF LKS WITH RESET ;RESTORE LINE CLOCK VECTOR

TEST THAT BIT6 OF LKS CAN BE SET & RESET

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1712
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1717 005304 000004
1718 005306 013703 000004
1719 005312 013704 000006
1720 005316 012737 005450 000004
1721 005324 012737 000340 000006
1722 005332 000005
1723 005334 012700 000002
1724 005340 032777 000020 173472
1725 005346 001404
1726 005350 013737 002406 001020
1727 005356 000403
1728 005360 013737 002346 001020 1$:
1729 005366 013737 001020 001022 2$:
1730 005374 040037 001022
1731 005400 023737 001020 001022
1732 005406 001002
1733 005410 050037 001022
1734 005414 017737 173402 001024 3$:
1735 005422 052777 000100 173372
1736 005430 032777 000100 173362
1737 005436 001011
1738 005440 013777 001024 173354
1739 005446 000401
1740 005450 022626 4$:
1741 005452 006300 5$:
1742 005454 105700
1743 005456 100343
1744 005460 000401
1745
1746 005462 104040 6$:
1747
1748
1749
1750 005464 010337 000004 7$:
1751 005470 010437 000006

```

```

:*****
:*TEST 15 TEST FOR DUAL ADDRESSING OF REGISTERS
:*****
TST15: SCOPE
MOV @#4,R3 ;SAVE TIMEOUT VECTOR
MOV @#6,R4 ;SAVE TIMEOUT PSW
MOV #4,@#4 ;SET UP TIMEOUT VECTOR
MOV #340,@#6 ;KEEP PRIO=7
RESET ;CLEAR EVERYTHING
MOV #BIT1,R0 ;SET UP BIT MASK
BIT #BIT4,@SWR ;CLOCK TEST ONLY?
BEQ 1$ ;BR IF NOT
MOV LKS,$GDADR ;ELSE, MOVE GOOD LKS ADDRESS INTO $GDADR
BR 2$
1$: MOV RCSR,$GDADR ;MOVE GOOD RCSR ADDRESS INTO $GDADR
2$: MOV $GDADR,$BDADR ;MOVE GOOD ADDRESS INTO TEST ADDRESS LOCATION
BIC R0,$BDADR ;CREATE BAD ADDRESS BY COMPLEMENTING ONE BIT
CMP $GDADR,$BDADR ;ARE ADDRESSES IDENTICAL?
BNE 3$ ;IF NOT, TEST THIS ADDRESS
BIS R0,$BDADR ;ELSE, BIT SET THIS BIT POSITION TO GENERATE BAD ADDRESS
3$: MOV @BDADR,$GDDAT ;SAVE CONTENTS OF BAD ADDRESS IF IT EXISTS
BIS #BIT6,@BDADR ;SET BIT6 USING BAD ADDRESS
BIT #BIT6,@SGDADR ;CHECK TO SEE IF GOOD ADDRESS CONTAINS BIT6
BNE 6$ ;BR IF SET ---> ERROR
MOV $GDDAT,@BDADR ;RESTORE ANY MEMORY LOCATION THAT WAS ALTERED
BR 5$ ;BR TO CONTINUE TEST
4$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT
5$: ASL R0 ;SHIFT BIT MASK TO NEXT POSITION
TSTB R0 ;COMPLEMENTED ALL BITS FROM 1 - 7?
BPL 2$ ;BR, IF NOT.
BR 7$ ;BR TO NEXT TEST
6$: ERROR 40 ;DUAL ADDRESSING ERROR
;BDADR = DUAL ADDRESS
;SGDADR = GOOD ADDRESS
7$: MOV R3,@#4 ;RESTORE TIMEOUT VECTOR
MOV R4,@#6 ;RESTORE TIMEOUT PSW

```

T15 TEST FOR DUAL ADDRESSING OF REGISTERS

```

1752
1753
1754
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1757 005474 000004
1758 005476 005737 002336
1759 005502 001437
1760 005504 032777 000100 173326
1761 005512 001033
1762 005514 000005
1763 005516 105777 174664
1764 005522 100401
1765
1766 005524 104041
1767
1768 005526 042777 000200 174652
1769 005534 032777 000200 174644
1770 005542 001410
1771 005544 042777 000200 174634
1772 005552 032777 000200 174626
1773 005560 001401
1774
1775 005562 104042
1776
1777 005564 005000
1778 005566 105777 174614
1779 005572 100403
1780 005574 005200
1781 005576 001373
1782
1783 005600 104043
1784

```

```

*****
*TEST 16 TEST THAT BIT7 OF LKS SETS & CAN BE CLEARED
*****
TST16: SCOPE
TST CTSTFL ;IS CONSOLE UNDER TEST?
BEQ TST17 ;IF NOT, SKIP THIS TEST
BIT #BIT6,@SWR ;ARE LINE CLOCK TESTS INHIBITED?
BNE TST17 ;IF YES, SKIP THIS TEST
RESET ;CLEAR EVERYTHING & SET BIT7 OF LKS
1$: TSTB @LKS ;TEST FOR BIT7 OF LKS
BMI 2$ ;BR IF SET
ERROR 41 ;BIT7 OF LKS DID NOT SET WITH RESET
2$: BIC #BIT7,@LKS ;CLEAR BIT7 OF LKS
BIT #BIT7,@LKS ;TEST BIT7 OF LKS
BEQ 3$
1771 BIC #BIT7,@LKS ;TRY ONE MORE TIME BECAUSE THE CLOCK
1772 BIT #BIT7,@LKS ; MAY HAVE SET IMMEDIATELY AFTER THE FIRST CLEAR
1773 BEQ 3$
ERROR 42 ;CAN NOT CLEAR BIT7 OF LKS
3$: CLR R0 ;CLEAR TIMER
CONT: TSTB @LKS ;TEST FOR BIT7 OF LKS
BMI TST17 ;BR, IF SET
INC R0 ;INCREMENT TIMER
BNE CONT ;CONTINUE UNTIL TIME EXPIRES
ERROR 43 ;BIT7 OF LKS DOES NOT SET

```

TEST THAT BIT7 OF LKS SETS & CAN BE CLEARED

```
1785
1786
1787      ::*****
1788      :*TEST 17      TEST THAT THE REAL TIME CLOCK INTERRUPTS PROPERLY
1789      :*****
1789 005602 000004 TST17: SCOPE
1790 005604 005737 002336 TST CTSTFL ;IS CONSOLE UNDER TEST?
1791 005610 001503 BEQ TST20 ;IF NOT, SKIP THIS TEST
1792 005612 032777 000100 173220 BIT #BIT6,@SWR ;ARE LINE CLOCK TESTS INHIBITED?
1793 005620 001077 BNE TST20 ;IF YES, SKIP THIS TEST
1794 005622 004737 012242 JSR PC,WRPSW ;SET PSW TO PRIORITY 7
1795 005626 000340 .WORD 340
1796 005630 017703 174554 MOV @ARTCVT,R3 ;SAVE LINE CLOCK VECTOR
1797 005634 017704 174552 MOV @ARTCPW,R4 ;SAVE LINE CLOCK PSW VECTOR
1798 005640 012777 005702 174542 MOV #2,@ARTCVT ;SET RTC INTERRUPT VECTOR TO ERROR REPORT
1799 005646 012777 000340 174536 MOV #340,@ARTCPW ;KEEP PRIORITY AT 7
1800 005654 042777 000200 174524 BIC #BIT7,@LKS ;CLEAR CLOCK DONE FLAG
1801 005662 052777 000100 174516 BIS #BIT6,@LKS ;SET INTERRUPT ENABLE
1802 005670 105777 174512 1$: TSTB @LKS ;WAIT FOR RTC DONE(INTERRUPT REQUEST)
1803 005674 100375 BPL 1$
1804 005676 000240 NOP ;GIVE TIME FOR ANY INTERRUPTS
1805 005700 000402 BR 3$ ;BR, IF NO INTERRUPT OCCURS
1806
1807 005702 022626 2$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
1808 005704 104044 ERROR 44 ;RTC INTERRUPTS AT PRIORITY 7
1809
1810 005706 005077 174474 3$: CLR @LKS ;DISABLE RTC INTERRUPTS & CLEAR DONE
1811 005712 012777 005740 174470 MOV #4,@ARTCVT ;SET RTC INTERRUPT VECTOR FOR ERROR
1812 005720 004737 012242 JSR PC,WRPSW ;CHANGE PSW TO PRIORITY 5
1813 005724 000240 .WORD 240
1814 005726 105777 174454 20$: TSTB @LKS ;WAIT FOR DONE (INTERRUPT REQUEST)
1815 005732 100375 BPL 20$
1816 005734 000240 NOP ;GIVE TIME FOR ANY INTERRUPT
1817 005736 000402 BR 5$ ;IF NO INTERRUPT - BR TO CONTINUE TEST
1818
1819 005740 022626 4$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
1820 005742 104045 ERROR 45 ;RTC INTERRUPTS WITH INTERRUPTS DISABLED
1821
1822 005744 012777 006000 174436 5$: MOV #7,@ARTCVT ;POINT RTC VECTOR TO END OF TEST
1823 005752 042777 000200 174426 BIC #BIT7,@LKS ;CLEAR CLOCK DONE FLAG
1824 005760 052777 000100 174420 BIS #BIT6,@LKS ;ALLOW INTERRUPTS
1825 005766 105777 174414 6$: TSTB @LKS ;WAIT FOR RTC DONE
1826 005772 100375 BPL 6$
1827 005774 000240 NOP ;GIVE TIME FOR INTERRUPT
1828
1829 005776 104046 ERROR 46 ;RTC INTERRUPT DID NOT OCCUR
1830
1831 006000 022626 7$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
1832 006002 042777 000100 174376 BIC #BIT6,@LKS ;DISABLE INTERRUPTS
1833 006010 010377 174374 MOV R3,@ARTCVT ;RESTORE LINE CLOCK VECTOR
1834 006014 010477 174372 MOV R4,@ARTCPW ;RESTORE LINE CLOCK PSW VECTOR
1835
1836
```

TEST THAT THE REAL TIME CLOCK INTERRUPTS PROPERLY

```
1837
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1839
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1841
1842
1843 006020 000004
1844 006022 005737 002336
1845 006026 001457
1846 006030 032777 000100 173002
1847 006036 001053
1848 006040 000005
1849 006042 017703 174342
1850 006046 017704 174340
1851 006052 012777 006122 174330
1852 006060 012777 000340 174324
1853 006066 004737 012242
1854 006072 000240
1855 006074 042777 000200 174304
1856 006102 052777 000100 174276
1857 006110 105777 174272 1$:
1858 006114 100375
1859 006116 000240
1860
1861 006120 104047
1862
1863 006122 022626 2$:
1864 006124 012777 006144 174256
1865 006132 004737 012242
1866 006136 000240
1867 006140 000240
1868 006142 000402
1869
1870 006144 022626 3$:
1871 006146 104050
1872
1873
1874 006150 042777 000100 174230 4$:
1875 006156 010377 174226
1876 006162 010477 174224
```

```

;*****
;*TEST 20 TEST RTC FOR DOUBLE INTERRUPTS
;*****
TST20: SCOPE
TST CTSTFL ;IS CONSOLE UNDER TEST?
BEQ TST21 ;IF NOT, SKIP THIS TEST
BIT #BIT6,@SWR ;ARE LINE CLOCK TESTS INHIBITED?
BNE TST21 ;IF YES, SKIP THIS TEST
RESET ;CLEAR EVERYTHING
MOV @RTCVT,R3 ;SAVE LINE CLOCK VECTOR
MOV @RTCP SW,R4 ;SAVE LINE CLOCK PSW VECTOR
MOV #2$,@RTCVT ;SET UP RTC INTERRUPT VECTOR
MOV #340,@RTCP SW ;DISALLOW INTERRUPTS AFTER THE INTERRUPT
JSR PC,WRPSW ;SET PRIORITY TO 5
.WORD 240
BIC #BIT7,@LKS ;CLEAR CLOCK DONE FLAG
BIS #BIT6,@LKS ;ENABLE CLOCK INTERRUPTS
TSTB @LKS ;WAIT FOR DONE
BPL 1$
NOP ;GIVE TIME FOR ANY INTERRUPT
ERROR 47 ;RTC INTERRUPT DID NOT OCCUR
2$:
CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
MOV #3$,@RTCVT ;POINT RTC VECTOR TO ERROR REPORT
JSR PC,WRPSW ;SET PSW TO PRIORITY 5
.WORD 240
NOP ;GIVE SOME TIME FOR AN INTERRUPT
BR 4$ ;NO INTERRUPT - BR TO END OF TEST
3$:
CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 50 ;INTERRUPT SEQUENCE DID NOT CLEAR
;INTERRUPT REQUEST
4$:
BIC #BIT6,@LKS ;DISABLE CLOCK INTERRUPTS
MOV R3,@RTCVT ;RESTORE LINE CLOCK VECTOR
MOV R4,@RTCP SW ;RESTORE LINE CLOCK PSW VECTOR
```

```
1877
1878
1879
1880
1881
1882 006166 000004
1883 006170 005737 002336
1884 006174 001442
1885 006176 032777 000100 172634
1886 006204 001036
1887 006206 004737 012242
1888 006212 000340
1889 006214 017703 174170
1890 006220 012777 006272 174162
1891 006226 042777 000200 174152
1892 006234 052777 000100 174144
1893 006242 105777 174140 1$:
1894 006246 100375
1895 006250 000005
1896 006252 004737 012242
1897 006256 000240
1898 006260 000240
1899 006262 042777 000100 174116
1900 006270 000402
1901
1902 006272 022626 2$:
1903 006274 104051
1904
1905 006276 010377 174106 3$:
```

```
*****
: *TEST 21 TEST THAT RTC INTERRUPT CLEARS WITH RESET
: *****
TST21: SCOPE
TST CTSTFL ;IS CONSOLE UNDER TEST?
BEQ TST22 ;IF NOT, SKIP THIS TEST
BIT #BIT6,@SWR ;ARE LINE CLOCK TESTS INHIBITED?
BNE TST22 ;IF YES, SKIP THIS TEST
JSR PC,WRPSW ;SET PRIORITY TO 7
.WORD 340
MOV @RTCVT,R3 ;SAVE LINE CLOCK VECTOR
MOV #2$,@RTCVT ;POINT RTC VECTOR TO ERROR REPORT
BIC #BIT7,@LKS ;CLEAR CLOCK DONE FLAG
BIS #BIT6,@LKS ;ENABLE CLOCK INTERRUPTS
1$: TSTB @LKS ;WAIT FOR DONE (INTERRUPT REQUEST)
BPL 1$
RESET ;CLEAR PENDING INTERRUPT WITH RESET
JSR PC,WRPSW ;SET PRIORITY TO 5
.WORD 240
NOP ;GIVE TIME FOR ANY INTERRUPT
BIC #BIT6,@LKS ;DISALLOW INTERRUPTS
BR 3$ ;BR TO END OF TEST
2$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 51 ;RESET DID NOT CLEAR INTERRUPT
3$: MOV R3,@RTCVT ;RESTORE LINE CLOCK VECTOR
```

T21 TEST THAT RTC INTERRUPT CLEARS WITH RESET

```
1906
1907
1908
1909
1910
1911 006302 000004
1912 006304 005737 002336
1913 006310 001447
1914 006312 032777 000100 172520
1915 006320 001043
1916 006322 004737 012242
1917 006326 000340
1918 006330 017703 174054
1919 006334 012777 006412 174046
1920 006342 042777 000200 174036
1921 006350 052777 000100 174030
1922 006356 105777 174024
1923 006362 100375
1924 006364 042777 000200 174014
1925 006372 004737 012242
1926 006376 000240
1927 006400 000240
1928 006402 042777 000100 173776
1929 006410 000402
1930
1931
1932 006412 022626
1933 006414 104052
1934
1935 006416 010377 173766
1936 006422 004737 012242
1937 006426 000340

;*****
;*TEST 22 TEST THAT RTC INTERRUPT CLEARS BY CLEARING BIT7 OF LKS
;*****
TST22: SCOPE
TST CTSTFL ;IS CONSOLE UNDER TEST?
BEQ TST23 ;IF NOT, SKIP THIS TEST
BIT #BIT6,@SWR ;ARE LINE CLOCK TESTS INHIBITED?
BNE TST23 ;IF YES, SKIP THIS TEST
JSR PC,WRPSW ;SET PRIORITY TO 7
.WORD 340
MOV @RTCVT,R3 ;SAVE LINE CLOCK VECTOR
MOV #2,@RTCVT ;POINT RTC VECTOR TO ERROR REPORT
BIC #BIT7,@LKS ;CLEAR CLOCK DONE FLAG
BIS #BIT6,@LKS ;ENABLE CLOCK INTERRUPTS
1$: TSTB @LKS ;WAIT FOR DONE (INTERRUPT REQUEST)
BPL 1$
BIC #BIT7,@LKS ;CLEAR DONE & INTERRUPT
JSR PC,WRPSW ;ALLOW INTERRUPTS
.WORD 240
NOP ;GIVE TIME FOR ANY INTERRUPT
BIC #BIT6,@LKS ;DISALLOW INTERRUPTS
BR 3$ ;BR TO END OF TEST

2$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 52 ;CLEARING BIT7 OF LKS DID NOT CLEAR INTERRUPT

3$: MOV R3,@RTCVT ;RESTORE LINE CLOCK VECTOR
JSR PC,WRPSW ;RESTORE PRIORITY TO 7
.WORD 340
```

```
1938
1939
1940
1941
1942
1943 006430 000004
1944 006432 005737 002336
1945 006436 001462
1946 006440 032777 000100 172372
1947 006446 001056
1948 006450 042777 000100 173730
1949
1950 006456 005000
1951 006460 012701 177777
1952 006464 005002
1953 006466 005077 173714
1954 006472 105777 173710
1955 006476 100375
1956 006500 005077 173702
1957 006504 105777 173676
1958 006510 100003
1959 006512 005202
1960 006514 005077 173666
1961 006520 005200
1962 006522 001370
1963 006524 005201
1964 006526 001003
1965 006530 010237 006600
1966 006534 000753
1967 006536 013701 006600
1968 006542 160201
1969 006544 100001
1970 006546 005401
1971 006550 020127 000001
1972 006554 003403
1973
1974 006556 010237 006602
1975 006562 104053
1976
1977 006564 032777 000020 172246
1978 006572 001404
1979 006574 000137 012102
1980
1981 006600 000000
1982 006602 000000

;*****
;*TEST 23 TEST CLOCK REPEATABILITY
;*****
TST23: SCOPE
TST CTSTFL ;IS CONSOLE UNDER TEST?
BEQ TST24 ;IF NOT, SKIP THIS TEST
BIT #BIT6,@SWR ;ARE LINE CLOCK TESTS INHIBITED?
BNE TST24 ;IF YES, SKIP THIS TEST
BIC #BIT6,@LKS ;DISALLOW INTERRUPTS

CLR R0 ;CLEAR A TIMER
MOV #-1,R1 ;SET A FLAG INDICATING FIRST PASS THRU THIS LOOP
1$: CLR R2 ;CLEAR CLOCK COUNTER
CLR @LKS ;CLEAR DONE
2$: TSTB @LKS ;SYNC ON DONE
BPL 2$
CLR @LKS ;CLEAR DONE
3$: TSTB @LKS ;IS CLOCK DONE?
BPL 4$ ;BR IF NOT, TO INCREMENT TIMER
INC R2 ;IF DONE, INCREMENT CLOCK COUNT
CLR @LKS ;CLEAR DONE
4$: INC R0 ;INCREMENT TIMER
BNE 3$ ;BR IF TIME REMAINS
INC R1 ;INCREMENT LOOP PASS FLAG
BNE CMPARE ;BR IF TWO PASSES HAVE BEEN MADE
MOV R2,FIRST ;IF NOT, STORE FIRST CLOCK COUNT
BR 1$ ;DO LOOP AGAIN
CMPARE: MOV FIRST,R1 ;RECALL FIRST CLOCK COUNT
SUB R2,R1 ;CALCULATE DIFFERENCE OF TWO COUNTS
BPL TOLER ;IF POSITIVE,SKIP NEGATION OF DIFFERENCE
NEG R1 ;MAKE DIFFERENCE A POSITIVE NUMBER
TOLER: CMP R1,#1 ;COMPARE DIFFERENCE WITH DESIRED TOLERANCE
BLE 5$ ;BR, IF LOWER/EQUAL TO TOLERANCE

MOV R2,SECND ;STORE SECOND COUNT
ERROR 53 ;CLOCK REPEATABILITY ERROR

5$: BIT #BIT4,@SWR ;CLOCK TESTS ONLY?
BEQ TST24 ;BR IF NOT
JMP $EOP ;ELSE, JUMP TO END OF PASS ROUTINE

FIRST: .WORD 0
SECND: .WORD 0
```

```
1983  
1984  
1985  
1986  
1987  
1988 006604 000004  
1989 006606 042777 000100 173536  
1990 006614 017703 173542  
1991 006620 012777 006644 173534  
1992 006626 105777 173520  
1993 006632 100375  
1994 006634 004737 012242  
1995 006640 000140  
1996 006642 000402  
1997  
1998 006644 022626  
1999 006646 104054  
2000  
2001 006650 012777 006670 173504  
2002 006656 052777 000100 173466  
2003 006664 000240  
2004  
2005 006666 104055  
2006  
2007 006670 042777 000100 173454  
2008 006676 022626  
2009 006700 010377 173456  
2010
```

```
*****  
*TEST 24 TEST THAT XMIT INTERRUPTS ONLY WHEN ENABLED  
*****  
TST24: SCOPE  
BIC #BIT6,@TCSR ;CLEAR TRANSMIT INTERRUPT ENABLE  
MOV @TVECT,R3 ;SAVE XMIT VECTOR  
MOV #2$,@TVECT ;POINT XMIT VECTOR TO ERROR REPORT  
1$: TSTB @TCSR ;WAIT FOR DONE  
BPL 1$  
JSR PC,WRPSW ;SET PSW TO PRIORITY 3  
.WORD 140  
BR 3$  
2$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT  
ERROR 54  
3$: MOV #4$,@TVECT ;XMIT INTERRUPTS WITH INTERRUPT ENABLE CLEAR  
BIS #BIT6,@TCSR ;SET XMIT VECTOR TO END OF TEST  
NOP ;ENABLE INTERRUPTS  
ERROR 55 ;XMIT DID NOT INTERRUPT  
4$: BIC #BIT6,@TCSR ;DISABLE INTERRUPTS  
CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT  
MOV R3,@TVECT ;RESTORE XMIT VECTOR
```

TEST THAT XMIT INTERRUPTS ONLY WHEN ENABLED

```
2011
2012
2013      ;*****
2014      ;*TEST 25      TEST THAT XMIT INTERRUPTS DO NOT OCCUR WHEN DISABLED
2015      ;*****
2015 006704 000004      TST25: SCOPE
2016 006706 042777 000100 173436      BIC      #BIT6,@TCSR      ;DISABLE INTERRUPTS
2017 006714 004737 012242      JSR      PC,WRPSW      ;SET PSW TO PRIORITY 7
2018 006720 000340      .WORD   340
2019 006722 017703 173434      MOV      @TVECT,R3      ;SAVE XMIT VECTOR
2020 006726 012777 006754 173426      MOV      #2$,@TVECT      ;POINT XMIT VECTOR TO ERROR REPORT
2021 006734 105777 173412      1$:     TSTB     @TCSR      ;WAIT FOR DONE
2022 006740 100375      BPL      1$
2023 006742 052777 000100 173402      BIS      #BIT6,@TCSR      ;ENABLE INTERRUPT
2024 006750 000240      NOP
2025 006752 000402      BR       3$      ;CONTINUE TEST
2026
2027 006754 022626      2$:     CMP      (SP)+,(SP)+      ;RESTORE SP AFTER INTERRUPT
2028 006756 104056      ERROR   56
2029
2030 006760 042777 000100 173364      3$:     BIC      #BIT6,@TCSR      ;XMIT INTERRUPTS AT PRIORITY=7
2031 006766 012777 007006 173366      MOV      #4$,@TVECT      ;CLEAR INTERRUPT ENABLE
2032 006774 004737 012242      JSR      PC,WRPSW      ;POINT XMIT VECTOR TO ERROR REPORT
2033 007000 000140      .WORD   140      ;SET PSW TO PRIORITY 3
2034 007002 000240      NOP
2035 007004 000402      BR       5$      ;BR TO END OF TEST-NO INTERRUPT
2036
2037 007006 022626      4$:     CMP      (SP)+,(SP)+      ;RESTORE SP AFTER INTERRUPT
2038 007010 104057      ERROR   57
2039
2040 007012 010377 173344      5$:     MOV      R3,@TVECT      ;XMIT INTERRUPT OCCURES WITH BIT6 CLEAR
      ;RESTORE XMIT VECTOR
```

TEST THAT XMIT INTERRUPTS DO NOT OCCUR WHEN DISABLED

```
2041
2042
2043
2044      ;*****
2045      ;*TEST 26      TEST TRANSMITTER FOR DOUBLE INTERRUPTS
2046      ;*****
2046      TST26:  SCOPE
2047      007016  000004      BIC      #BIT6,@TCSR      ;CLEAR INTERRUPT ENABLE
2048      007020  042777  000100  173324      MOV      @TVECT,R3      ;SAVE XMIT VECTOR
2049      007026  017703  173330      MOV      @TPSW,R4      ;SAVE XMIT PSW VECTOR
2050      007032  017704  173326      MOV      #2$,@TVECT      ;SET UP XMIT VECTOR
2051      007036  012777  007100  173316      MOV      #340,@TPSW      ;SET PIO 7 AFTER INTERRUPT
2052      007044  012777  000340  173312      JSR      PC,WRPSW      ;SET PSW TO PRIORITY 3
2053      007052  004737  012242      .WORD   140
2054      007056  000140
2055      007060  105777  173266      1$:     TSTB   @TCSR      ;WAIT FOR DONE
2056      007064  100375      BPL
2057      007066  052777  000100  173256      BIS     #BIT6,@TCSR      ;ENABLE INTERRUPTS
2058      007074  000240      NOP
2059      007076  104060      ERROR   60
2060
2061      007100  022626      ;XMIT INTERRUPT DID NOT OCCUR
2062      007102  012777  007130  173252      2$:     CMP     (SP)+,(SP)+  ;RESTORE SP AFTER INTERRUPT
2063      007110  004737  012242      MOV     #4$,@TVECT      ;POINT XMIT VECTOR TO ERROR
2064      007114  000140      JSR     PC,WRPSW      ;SET PSW TO PRIORITY 3
2065      007116  000240      .WORD   140
2066      007120  042777  000100  173224      NOP     ;GIVE TIME FOR ANY INTERRUPTS
2067      007126  000402      BIC     #BIT6,@TCSR      ;DISABLE INTERRUPTS
2068      BR     5$          ;BR TO END OF TEST
2069      007130  022626      4$:     CMP     (SP)+,(SP)+  ;RESTORE SP AFTER INTERRUPT
2070      007132  104061      ERROR   61
2071
2072      007134  010377  173222      5$:     MOV     R3,@TVECT      ;XMIT RE-INTERRUPTED
2073      007140  010477  173220      MOV     R4,@TPSW      ;RESTORE XMIT VECTOR
2074      ;RESTORE XMIT PSW VECTOR
2075      ;*****
2076      ;*TEST 27      TEST THAT XMIT INTERRUPT CLEARS WITH LOADING TBUF
2077      ;*****
2078      TST27:  SCOPE
2079      007144  000004      BIC     #BIT6,@TCSR      ;DISABLE INTERRUPTS
2080      007146  042777  000100  173176      JSR     PC,WRPSW      ;SET PSW TO PRIORITY 7
2081      007154  004737  012242      .WORD   340
2082      007160  000340      MOV     @TVECT,R3      ;SAVE XMIT VECTOR
2083      007162  017703  173174      MOV     #2$,@TVECT      ;POINT XMIT VECTOR TO ERROR
2084      007166  012777  007240  173166      BIS     #BIT6,@TCSR      ;ENABLE INTERRUPTS
2085      007174  052777  000100  173150      CLR     @TBUF          ;LOAD TBUF
2086      007202  005077  173146      1$:     TSTB   @TCSR      ;WAIT FOR DONE (INTERRUPT)
2087      007206  105777  173140      BPL
2088      007212  100375      CLR     @TBUF          ;FILL SECOND BUFFER TO RESET INT.
2089      007214  005077  173134      JSR     PC,WRPSW      ;ALLOW INTERRUPTS
2090      007220  004737  012242      .WORD   140
2091      007224  000140      NOP     ;GIVE TIME FOR ANY INTERRUPTS
2092      007226  000240      BIC     #BIT6,@TCSR      ;DISABLE INTERRUPTS
2093      007230  042777  000100  173114      BR     3$          ;BR TO END OF TEST
2094      007236  000402
2095      007240  022626      2$:     CMP     (SP)+,(SP)+  ;RESTORE SP AFTER INTERRUPT
2096      007242  104062      ERROR   62
```

TEST THAT XMIT INTERRUPT CLEARS WITH LOADING TBUF

```
2097  
2098 007244 010377 173112 3$: MOV R3,@TVECT ;LOADING TBUF DID NOT CLEAR INTERRUPT.  
2099 ;RESTORE XMIT VECTOR
```

TEST THAT XMIT INTERRUPT CLEARS WITH LOADING TBUF

```
2100
2101
2102      ;*****
2103      ;*TEST 30      TEST THAT RCVR ACTIVE (11) & DONE (7) SET & CLEAR PROPERLY
2104      ;*****
2104 007250 000004      TST30: SCOPE
2105 007252 000005      RESET
2106 007254 052777 000004 173070      BIS #BIT2,@TCSR ;CLEAR EVERYTHING
2107 007262 005000      CLR RO ;SET MAINTENANCE WRAP
2108 007264 005077 173064      CLR @TBUF ;CLEAR A TIMER
2109 007270 032777 004000 173050 WACTV: BIT #BIT11,@RCSR ;LOAD TRANSMIT BUFFER
2110 007276 001006      BNE 2$ ;TEST RCVR ACTIVE BIT
2111 007300 005200      INC RO ;BR IF SET
2112 007302 001372      BNE WACTV ;INCREMENT TIMER IF NOT SET
2113 007304 042777 000004 173040      BIC #BIT2,@TCSR ;CONTINUE WAIT IF TIME REMAINS
2114
2115 007312 104063      ERROR 63 ;CLEAR MAINTENANCE BIT
2116
2117 007314 000005      2$: RESET ;RCVR ACTIVE DID NOT SET WHILE RECEIVING
2118 007316 032777 004000 173022      BIT #BIT11,@RCSR ;VERIFY "INIT" CLEARS RCV ACTIVE
2119 007324 001401      BEQ 3$
2120
2121 007326 104115      ERROR 115 ;INIT DID NOT CLEAR RCV ACTIVE
2122
2123 007330 005000      3$: CLR RO ;CLEAR A TIMER
2124 007332 052777 000004 173012      BIS #BIT2,@TCSR ;SET MAINTENANCE WRAP
2125 007340 062700 000000      WT: ADD #0,RO ;WAIT AT LEAST ONE BIT TIME
2126 007344 005200      INC RO
2127 007346 001374      BNE WT
2128 007350 033777 004000 172770      BIT BIT11,@RCSR ;VERIFY RCV ACTIVE STILL CLEAR
2129 007356 001404      BEQ 4$ ;BR IF CLEAR
2130
2131 007360 042777 000004 172764      BIC #BIT2,@TCSR ;CLEAR MAINTENANCE WRAP
2132 007366 104116      ERROR 116 ;RCV ACTIVE WITHOUT "START" BIT
2133
2134 007370 005000      4$: CLR RO ;CLEAR TIMER
2135 007372 005077 172756      CLR @TBUF ;LOAD TRANSMIT BUFFER
2136 007376 105777 172744      WDONE: TSTB @RCSR ;CHECK FOR RECEIVER DONE
2137 007402 100406      BMI 5$ ;BR, IF DONE
2138 007404 005200      INC RO ;INCREMENT TIMER, IF NOT DONE
2139 007406 001373      BNE WDONE ;CONTINUE WAIT IF TIME REMAINS
2140 007410 042777 000004 172734      BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
2141 007416 104064      ERROR 64
2142
2143
2144 007420 032777 004000 172720 5$: BIT #BIT11,@RCSR ;CHECK FOR RCVR ACTIVE CLEAR
2145 007426 001404      BEQ 6$ ;BR, IF CLEAR
2146 007430 042777 000004 172714      BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
2147 007436 104065      ERROR 65
2148
2149
2150 007440 000005      6$: RESET ;RCVR ACTIVE DID NOT CLEAR WITH RCVR DONE
2151 007442 105777 172700      TSTB @RCSR ;CLEAR DONE WITH RESET
2152 007446 001404      BEQ 7$ ;CHECK FOR DONE CLEAR
2153
2154 007450 042777 000004 172674      BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
2155 007456 104066      ERROR 66
```

TEST THAT RCVR ACTIVE (11) & DONE (7) SET & CLEAR PROPERLY

2156 ;RESET DID NOT CLEAR RCVR DONE
2157
2158 007460 042777 000004 172660 7\$: BIC #BIT2,@RCSR ;CLEAR MAINTENANCE BIT
2159 007466 000400 BR TST31 ;BR TO NEXT TEST

TEST THAT RCVR ACTIVE (11) & DONE (7) SET & CLEAR PROPERLY

2160
2161
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2186
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2188
2189
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2191
2192
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2198
2199
2200

*TEST 31 TEST THAT RDR ENABLE CLEARS RECEIVER DONE FLAG

```

TST31: SCOPE
        RESET                ;CLEAR EVERYTHING
        BIS #BIT0,@RCSR      ;SET RDR ENABLE
        BIS #BIT2,@TCSR      ;SET MAINTENANCE WRAP
        CLR @TBUF            ;LOAD TRANSMITTER
1$:     TSTB @RCSR           ;WAIT FOR RECEIVER DONE
        BPL 1$
        BIT #BIT0,@RCSR      ;VERIFY RCV ACTIVE CLEARED RDR ENABLE
        BEQ 2$              ;BR IF CLEAR
        ERROR 117          ;RDR ENABLE NOT CLEARED WITH RCV ACTIVE
2$:     BIS #BIT0,@RCSR      ;CLEAR DONE BY SETTING RDR ENABLE
        TSTB @RCSR          ;CHECK FOR DONE CLEAR
        BEQ TST32          ;BR, IF CLEAR TO NEXT TEST
        BIC #BIT2,@TCSR      ;CLEAR MAINTENANCE BIT
        ERROR 67
        ;SETTING RDR ENABLE DID NOT CLEAR RCVR DONE

```

*TEST 32 TEST THAT READING RBUF CLEARS RECEIVER DONE

```

TST32: SCOPE
        RESET                ;CLEAR EVERYTHING
        BIS #BIT2,@TCSR      ;SET MAINTENANCE WRAP
        CLR @TBUF            ;LOAD TRANSMITTER
1$:     TSTB @RCSR           ;WAIT FOR RECEIVER DONE
        BPL 1$
        MOV @RBUF,R0         ;READ RECEIVE BUFFER
        BIC #BIT2,@TCSR      ;CLEAR MAINTENANCE BIT
        TSTB @RCSR          ;CHECK FOR RECEIVE DONE CLEAR
        BEQ TST33          ;BR, IF CLEAR TO NEXT TEST
        ERROR 70
        ;READING RBUF DID NOT CLEAR RCVR DONE

```

T32 TEST THAT READING RBUF CLEARS RECEIVER DONE

```
2201
2202
2203
2204      ;:*****
2205      ;*TEST 33      TEST THAT RCVR INTERRUPTS ONLY WHEN ENABLED
2206      ;:*****
2206      007626 000004 TST33: SCOPE
2207      007630 042777 000100 172514 BIC #BIT6,@TCSR ;DISABLE TRANSMIT INTERRUPTS
2208      007636 042777 000100 172502 BIC #BIT6,@RCSR ;DISABLE RECEIVER INTERRUPTS
2209      007644 052777 000004 172500 BIS #BIT2,@TCSR ;SET MAINTENANCE WRAP
2210      007652 017703 172500 MOV @RVECT,R3 ;SAVE RECEIVE VECTOR
2211      007656 012777 007714 172472 MOV #2$,@RVECT ;POINT RCV VECTOR TO ERROR REPORT
2212      007664 004737 012242 JSR PC,WRPSW ;SET PSW TO PRIORITY 3
2213      007670 000140 .WORD 140
2214      007672 005077 172456 CLR @TBUF ;SEND A CHARACTER
2215      007676 105777 172444 1$: TSTB @RCSR ;WAIT FOR RECEIVER DONE
2216      007702 100375 BPL 1$
2217      007704 042777 000004 172440 BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
2218      007712 000405 BR 3$ ;CONTINUE TEST
2219
2220      007714 042777 000004 172430 2$: BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
2221      007722 022626 CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
2222      007724 104071 ERROR 71
2223
2224 ;RECEIVER INTERRUPTS WITH INT. ENABLE CLEAR
2225      007726 012777 007754 172422 3$: MOV #4$,@RVECT ;POINT RCV VECTOR TO END OF TEST
2226      007734 052777 000100 172404 BIS #BIT6,@RCSR ;ENABLE RCV INTERRUPTS
2227      007742 000240 NOP ;GIVE ANY INTERRUPTS TIME
2228      007744 042777 000004 172400 BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
2229      007752 104072 ERROR 72
2230
2231 ;RCVR DID NOT INTERRUPT
2232      007754 042777 000100 172364 4$: BIC #BIT6,@RCSR ;DISABLE INTERRUPTS
2233      007762 042777 000004 172362 BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
2234      007770 022626 CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
2235      007772 010377 172360 MOV R3,@RVECT ;RESTORE RECEIVE VECTOR
```

TEST THAT RCVR INTERRUPTS ONLY WHEN ENABLED

```
2236
2237
2238
2239      ;*****
2240      ;*TEST 34      TEST THAT RCVR INTERRUPTS DO NOT OCCUR WHEN DISABLED
2241      ;*****
2241      TST34:  SCOPE
2242      RESET          ;CLEAR EVERYTHING
2243      JSR      PC,WRPSW      ;SET PSW TO PRIORITY 7
2244      .WORD    340
2245      MOV      @RVECT,R3     ;SAVE RECEIVE VECTOR
2246      MOV      #2$,@RVECT   ;POINT RCVR VECTOR TO ERROR REPORT
2247      BIS      #BIT2,@TCSR  ;SET MAINTENANCE WRAP
2248      CLR      @TBUF        ;SEND A CHARACTER
2249      TSTB    @RCSR        ;WAIT FOR RECEIVER DONE
2250      BPL     1$
2251      BIS     #BIT6,@RCSR   ;ENABLE INTERRUPTS
2252      NOP
2253      BR     3$            ;GIVE TIME FOR INTERRUPT
2254      BIC     #BIT2,@TCSR  ;CONTINUE TEST
2255      CMP     (SP)+,(SP)+  ;CLEAR MAINTENANCE BIT
2256      ERROR   73          ;RESTORE SP AFTER INTERRUPT
2257
2258      ;RCVR INTERRUPTS AT PRIORITY 7
2259      BIC     #BIT6,@RCSR  ;CLEAR INTERRUPT ENABLE
2260      MOV     #4$,@RVECT  ;POINT RCVR VECTOR TO ERROR REPORT
2261      JSR     PC,WRPSW    ;SET PSW TO PRIORITY 3
2262      .WORD   140
2263      NOP
2264      BIC     #BIT2,@TCSR  ;GIVE TIME FOR ANY INTERRUPT
2265      BR     5$            ;CLEAR MAINTENANCE BIT
2266
2267      BIC     #BIT2,@TCSR  ;BR TO END OF TEST, IF NO INTERRUPT
2268      CMP     (SP)+,(SP)+  ;CLEAR MAINTENANCE BIT
2269      ERROR   74          ;RESTORE SP AFTER INTERRUPT
2270
2271      MOV     R3,@RVECT   ;RCVR INTERRUPT REQUEST PASSED WITH BIT6 CLEAR
2272      ;RESTORE RECEIVE VECTOR
```

```
2272
2273
2274
2275
2276
2277 010140 000004
2278 010142 000005
2279 010144 017703 172206
2280 010150 017704 172204
2281 010154 012777 010236 172174
2282 010162 012777 000340 172170
2283 010170 004737 012242
2284 010174 000140
2285 010176 052777 000004 172146
2286 010204 005077 172144
2287 010210 105777 172132 1$:
2288 010214 100375
2289 010216 042777 000004 172126
2290 010224 052777 000100 172114
2291 010232 000240
2292
2293 010234 104075
2294
2295
2296 010236 022626
2297 010240 012777 010276 172110 2$:
2298 010246 004737 012242
2299 010252 000140
2300 010254 000240
2301 010256 042777 000100 172062
2302 010264 010377 172066
2303 010270 010477 172064
2304 010274 000402
2305
2306 010276 022626 3$:
2307 010300 104076
2308
2309 010302 010377 172050 4$:
```

```
*****
*TEST 35 TEST RECEIVER FOR DOUBLE INTERRUPTS
*****
TST35: SCOPE
        RESET ;CLEAR EVERYTHING
        MOV @RVECT,R3 ;SAVE RECEIVE VECTOR
        MOV @RPSW,R4 ;SAVE RECEIVE PSW VECTOR
        MOV #2$,@RVECT ;POINT RCV VECTOR TO CONTINUE TEST
        MOV #340,@RPSW ;SET PRIORITY TO 7 AFTER INTERRUPT
        JSR PC,WRPSW ;SET PSW TO PRIORITY 3
        .WORD 140
        BIS #BIT2,@TCSR ;SET MAINTENANCE WRAP
        CLR @TBUF ;SEND A CHARACTER
        TSTB @RCSR ;WAIT FOR RCVR DONE
        BPL 1$
        BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
        BIS #BIT6,@RCSR ;ENABLE RCV INTERRUPTS
        NOP ;GIVE SOME TIME

        ERROR 75 ;RCVR INTERRUPT DID NOT OCCUR

        CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
        MOV #3$,@RVECT ;POINT RCV VECTOR TO ERROR REPORT
        JSR PC,WRPSW ;RESET PSW TO PRIORITY 3
        .WORD #140
        NOP ;GIVE SOME TIME
        BIC #BIT6,@RCSR ;CLEAR INTERRUPT ENABLE
        MOV R3,@RVECT ;RESTORE RECEIVE VECTOR
        MOV R4,@RPSW ;RESTORE RECEIVE PSW VECTOR
        BR 4$ ;BR TO END OF TEST

        CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
        ERROR 76

        MOV R3,@RVECT ;RECEIVER RE-INTERRUPTED
        ;RESTORE RECEIVE VECTOR
```

TEST RECEIVER FOR DOUBLE INTERRUPTS

```
2310
2311
2312
2313      ;*****
2314      ;*TEST 36      TEST THAT RCVR INTERRUPT CLEARS BY READING RBUF
2315      ;*****
2315 010306 000004      TST36:  SCOPE
2316 010310 000005      RESET          ;CLEAR EVERYTHING
2317 010312 004737 012242      JSR      PC,WRPSW      ;SET PSW PRIORITY TO 7
2318 010316 000340      .WORD    340
2319 010320 017703 172032      MOV      @RVECT,R3    ;SAVE RECEIVE VECTOR
2320 010324 012777 010412 172024      MOV      #2$,@RVECT   ;POINT RCV VECTOR TO ERROR REPORT
2321 010332 052777 000100 172006      BIS      #BIT6,@RCSR  ;SET RCVR INTERRUPT ENABLE
2322 010340 052777 000004 172004      BIS      #BIT2,@TCSR  ;SET MAINTENANCE WRAP
2323 010346 005077 172002      CLR      @TBUF        ;SEND A CHARACTER
2324 010352 105777 171770      1$:     TSTB      @RCSR   ;WAIT FOR DONE (INTERRUPT)
2325 010356 100375      BPL      1$
2326 010360 042777 000004 171764      BIC      #BIT2,@TCSR  ;CLEAR MAINTENANCE BIT
2327 010366 005077 171756      CLR      @RBUF        ;READ RBUF TO CLEAR PENDING INTERRUPT
2328 010372 004737 012242      JSR      PC,WRPSW      ;SET PSW TO PRIORITY 3
2329 010376 000140      .WORD    140
2330 010400 000240      NOP
2331 010402 042777 000100 171736      BIC      #BIT6,@RCSR  ;NO INTERRUPT-CLEAR INT. ENABLE
2332 010410 000402      BR       3$
2333
2334 010412 022626      2$:     CMP      (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
2335 010414 104077      ERROR   77           ;READING RBUF DID NOT CLEAR INTERRUPT
2336
2337 010416 010377 171734      3$:     MOV      R3,@RVECT  ;RESTORE RECEIVE VECTOR
2338
```

```
2339
2340
2341
2342
2343
2344 010422 000004
2345 010424 000005
2346 010426 004737 012242
2347 010432 000340
2348 010434 017703 171716
2349 010440 012777 010520 171710
2350 010446 052777 000100 171672
2351 010454 052777 000004 171670
2352 010462 012777 000377 171664
2353 010470 105777 171652 1$:
2354 010474 100375
2355 010476 000005
2356 010500 004737 012242
2357 010504 000140
2358 010506 000240
2359 010510 042777 000100 171630
2360 010516 000402
2361
2362
2363 010520 022626 2$:
2364 010522 104100
2365
2366 010524 010377 171626 3$:
```

```

:*****
:*TEST 37 TEST THAT RESET CLEARS RECEIVE INTERRUPT
:*****
TST37: SCOPE
RESET ;CLEAR EVERYTHING
JSR PC,WRPSW ;SET PSW TO PRIORITY 7
.WORD 340
MOV @RVECT,R3 ;SAVE RECEIVE VECTOR
MOV #2$,@RVECT ;POINT RCV VECTOR TO ERROR REPORT
BIS #BIT6,@RCSR ;SET RCV INTERRUPT ENABLE
BIS #BIT2,@TCSR ;SET MAINTENANCE WRAP
MOV #377,@TBUF ;SEND AN ALL 1'S CHARACTER
1$: TSTB @RCSR ;WAIT FOR RCV DONE
BPL 1$
RESET ;CLEAR RCV INTERRUPT & RBUF
JSR PC,WRPSW ;SET PSW TO PRIORITY 3
.WORD 140
NOP ;ALLOW TIME FOR AN ERRONEOUS INTERRUPT
BIC #BIT6,@RCSR ;NO INTERRUPT-CLEAR INT. ENABLE
BR 3$ ;CONTINUE TEST

2$: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 100 ;RESET DID NOT CLEAR RCVR INTERRUPT

3$: MOV R3,@RVECT ;RESTORE RECEIVE VECTOR
```

```
2367
2368
2369
2370
2371
2372 010530 000004
2373 010532 032777 002000 170300
2374 010540 001432
2375 010542 000005
2376 010544 052777 000004 171600
2377 010552 012700 000003
2378 010556 005077 171572 1$:
2379 010562 105777 171564 2$:
2380 010566 100375
2381 010570 005300
2382 010572 001371
2383 010574 042777 000004 171550
2384 010602 032777 040000 171540
2385 010610 001001
2386 010612 104101
2387
2388
2389 010614 032777 100000 171526 3$:
2390 010622 001001
2391 010624 104102
2392
2393 010626 4$:

;*****
;*TEST 40 TEST THAT THE 'OR' ERROR (BIT14) & 'ERROR' (BIT15) CAN BE SET
;*****
TST40: SCOPE
BIT #BIT10,@SWR ;IS THIS TEST ENABLED
BEQ TST41 ;IF NOT ENABLED, BR TO NEXT TEST
RESET ;CLEAR EVERYTHING
BIS #BIT2,@TCSR ;SET MAINTENANCE WRAP
MOV #3,R0 ;SET CHARACTER COUNT TO SEND 3 CHAR.
1$: CLR @TBUF ;LOAD TRANSMIT BUFFER
2$: TSTB @TCSR ;WAIT FOR TRANSMIT DONE
BPL 2$
DEC R0 ;DECREMENT CHARACTER COUNT
BNE 1$ ;BR IF ALL CHARACTERS NOT TRANSMITTED
BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
BIT #BIT14,@RBUF ;TEST FOR 'OR' ERROR FLAG
BNE 3$ ;BR, IF SET
ERROR 101 ;'OR' ERROR FLAG DID NOT SET

BIT #BIT15,@RBUF ;TEST 'ERROR' FLAG
BNE 4$ ;BR, IF SET
ERROR 102 ;'ERROR' FLAG DID NOT SET WITH 'OR' FLAG
```

TEST THAT THE 'OR' ERROR (BIT14) & 'ERROR' (BIT15) CAN BE SET

```
2394
2395
2396
2397
2398
2399 010626 000004
2400 010630 032777 000400 170202
2401 010636 001444
2402 010640 000005
2403 010642 052777 000004 171502
2404 010650 012777 177777 171476
2405 010656 105777 171464 1$:
2406 010662 100375
2407 010664 005077 171460
2408 010670 052777 000001 171454
2409 010676 005000
2410 010700 117737 171442 001026 2$:
2411 010706 100406
2412 010710 005200
2413 010712 001372
2414
2415 010714 042777 000005 171430
2416 010722 104103
2417
2418 010724 105777 171420
2419 010730 001404
2420 010732 042777 000005 171412
2421
2422 010740 104103
2423
2424 010742 042777 000005 171402 3$:
```

```
*****
*TEST 41 TEST THAT BREAK TRANSMITS ALL ZEROES
*****
TST41: SCOPE
BIT #BIT8,@SWR ;IS BREAK FUNCTION TEST ENABLED?
BEQ TST42 ;BR TO NEXT TEST, IF NOT ENABLED
RESET ;CLEAR EVERYTHING
BIS #BIT2,@TCSR ;SET MAINTENANCE WRAP
MOV #-1,@TBUF ;TRANSMIT ALL ONES TO RCVR
TSTB @RCSR ;WAIT FOR RCVR DONE
BPL 1$
CLR @RBUF ;CLEAR DONE (LEAVING ALL ONES IN RBUF)
BIS #BIT0,@TCSR ;TRANSMIT BREAK
CLR R0 ;CLEAR A TIMER
MOV @RCSR,$BDDAT ;WAIT FOR RCVR DONE
BMI CONT41 ;BR IF DONE
INC R0 ;IF NOT, INCREMENT TIMER
BNE 2$ ;BR IF TIME REMAINS

BIC #BIT0!BIT2,@TCSR ;CLEAR MAINTENANCE & BREAK BITS
ERROR 103 ;BREAK DID NOT TRANSMIT ANYTHING

CONT41: TSTB @RBUF ;CHECK RECEIVE BUFFER FOR ZERO
BEQ 3$ ;BR, IF ZERO
BIC #BIT0!BIT2,@TCSR ;CLEAR MAINTENANCE & BREAK BITS

ERROR 103 ;BREAK DID NOT TRANSMIT ALL ZEROES

BIC #BIT0!BIT2,@TCSR ;CLEAR MAINTENANCE & BREAK BITS
```

```
2425
2426
2427
2428
2429
2430 010750 000004
2431 010752 032777 002000 170060
2432 010760 001435
2433 010762 032777 000400 170050
2434 010770 001431
2435 010772 000005
2436 010774 052777 000004 171350
2437 011002 052777 000001 171342
2438 011010 005077 171340
2439 011014 105777 171326 1$:
2440 011020 100375
2441 011022 042777 000005 171322
2442 011030 032777 020000 171312
2443 011036 001001
2444
2445 011040 104104
2446
2447 011042 032777 100000 171300 2$:
2448 011050 001001
2449
2450 011052 104114
2451
2452 011054 3$:
```

```

*****
*TEST 42 TEST THAT 'FR' ERROR CAN BE SET DURING BREAK
*****
TST42: SCOPE
BIT #BIT10,@SWR ;IS THE 'TEST ERROR FLAGS' BIT SET
BEQ TST43 ;BR TO NEXT TEST, IF NOT SET
BIT #BIT8,@SWR ;IS BREAK FUNCTION ENABLED
BEQ TST43 ;BR TO NEXT TEST, IF NOT SET
RESET ;CLEAR EVERYTHING
BIS #BIT2,@TCSR ;SET MAINTENANCE WRAP
BIS #BIT0,@TCSR ;SEND BREAK
CLR @TBUF ;TRANSMIT A CHARACTER TO TIME BREAK
1$: TSTB @RCSR ;WAIT FOR RCVR DONE
BPL 1$
BIC #BIT0!BIT2,@TCSR ;CLEAR MAINTENANCE & BREAK BITS
BIT #BIT13,@RBUF ;CHECK FOR FRAMING ERROR FLAG
BNE 2$ ;BR, IF SET
ERROR 104
;BREAK DID NOT SET FRAMING ERROR
2$: BIT #BIT15,@RBUF ;TEST 'ERROR' FLAG
BNE 3$ ;BR, IF SET
ERROR 114
;'ERROR' FLAG DID NOT SET WITH 'OR' FLAG
3$:
```

```
2453
2454
2455
2456      ;:*****
2457      ;*TEST 43      TEST DATA PATH FROM TRANSMITTER TO RECEIVER USING MAINTENANCE WRAP
2458      ;:*****
2458 011054 000004      TST43: SCOPE
2459
2460      RESET      ;CLEAR EVERYTHING
2461 011060 005001      CLR      R1      ;CLEAR REGISTER FOR TEST DATA
2462 011062 052777 000004 171262      BIS      #BIT2,@TCSR      ;SET MAINTENANCE WRAP
2463      ;TRANSMIT A BINARY COUNT PATTERN - UP
2464      ;TO THE BIT POSITION INDICATED BY THE
2465      ;CONTENTS OF LOCATION '$USW '
2466 011070 005201      1$:      INC      R1      ;INCREMENT THE TEST DATA
2467 011072 010177 171256      MOV      R1,@TBUF      ;XMIT A CHARACTER
2468 011076 105777 171244      2$:      TSTB      @RCSR      ;WAIT FOR RECEIVER DONE
2469 011102 100375      BPL      2$
2470 011104 017702 171240      MOV      @RBUF,R2      ;GET RECEIVED CHARACTER
2471 011110 043701 001112      BIC      @#$USWR,R1      ;CLEAR LOWEST UNUSED DATA BIT POSITITON IN TEST DATA
2472 011114 020102      CMP      R1,R2      ;COMPARE DATA
2473 011116 001003      BNE      3$      ;BR, IF NON-COMPARE
2474 011120 105701      TSTB      R1      ;TEST XMIT DATA FOR ZERO
2475 011122 001411      BEQ      4$      ;BR, IF FINISHED
2476 011124 000761      BR      1$      ;CONTINUE IF NOT
2477 011126 010137 001024      3$:      MOV      R1,$GDDAT      ;STORE THE EXPECTED DATA
2478 011132 010237 001026      MOV      R2,$BDDAT      ;STORE RECEIVED DATA
2479 011136 042777 000004 171206      BIC      #BIT2,@TCSR      ;CLEAR MAINTENANCE BIT
2480 011144 104105      ERROR      105      ;DATA COMPARE DATA
2481
2482 011146 042777 000004 171176 4$:      BIC      #BIT2,@TCSR      ;CLEAR MAINTENANCE BIT
2483
2484
2485
2486      ;:*****
2487      ;*TEST 44      TEST DATA PATHS USING WRAP CABLE
2488      ;:*****
2489 011154 000004      TST44: SCOPE
2490 011156 032777 000200 167654      BIT      #BIT7,@SWR      ;IS THIS TEST ENABLED
2491 011164 001432      BEQ      TST45      ;BR, IF NOT
2492 011166 000005      RESET      ;CLEAR EVERYTHING
2493 011170 005001      CLR      R1      ;CLEAR REGISTER FOR TEST DATA
2494      ;TRANSMIT A BINARY COUNT PATTERN - UP
2495      ;TO THE BIT POSITION INDICATED BY THE
2496      ;CONTENTS OF LOCATION '$USWR'
2497 011172 105201      1$:      INCB      R1      ;INCREMENT THE TEST DATA
2498 011174 010177 171154      MOV      R1,@TBUF      ;XMIT A CHARACTER
2499 011200 005000      CLR      R0      ;CLEAR A TIMER
2500 011202 105777 171140      2$:      TSTB      @RCSR      ;WAIT FOR RECEIVER DONE
2501 011206 100403      BMI      3$      ;BR IF DONE
2502 011210 005200      INC      R0      ;INCREMENT TIMER IF NOT
2503 011212 001373      BNE      2$      ;BR IF TIME REMAINS
2504
2505      ERROR      64      ;RECEIVER DONE NOT SET
2506
2507 011216 017702 171126      3$:      MOV      @RBUF,R2      ;GET RECEIVED CHARACTER
2508 011222 043701 001112      BIC      @#$USWR,R1      ;CLEAR LOWEST UNUSED DATA BIT POSITITON IN TEST DATA
```

TEST DATA PATHS USING WRAP CABLE

```
2509 011226 020102      CMP      R1,R2      ;COMPARE DATA
2510 011230 001003      BNE      4$         ;BR, IF NON-COMPARE
2511 011232 105701      TSTB     R1         ;TEST XMIT DATA FOR ZERO
2512 011234 001406      BEQ      TST45      ;BR, IF FINISHED
2513 011236 000755      BR       1$         ;CONTINUE IF NOT
2514 011240 010137 001024 4$:      MOV      R1,$GDDAT  ;STORE EXPECTED DATA
2515 011244 010237 001026      MOV      R2,$BDDAT  ;STORE RECEIVED DATA
2516
2517 011250 104106      ERROR   106        ;DATA COMPARE ERROR WITH WRAP CABLE
```


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TEST DL11-W LOGIC BY EXERCISING THE XMIT, RECEIVE, & CLOCK (IF AVAILABLE) SIMULTAN
SEQ 0066

2630 011740 000000
2631 011742 000044
2632

SCPSW: .WORD 0
BUF: .BLKW 44


```
2678
2679 012206 005037 001076 GOAGIN: CLR $DEVCT ;CLEAR DEVICE COUNT
2680 012212 022737 000001 002342 CMP #1,TMP2 ;IS THERE ONLY ONE DEVICE UNDER TEST?
2681 012220 001004 BNE RSTRT ;BR, IF NOT
2682 012222 012706 001000 MOV #1000,SP ;RESET STACK POINTER
2683 012226 000137 003622 JMP TST1 ;GO DO ANOTHER PASS
2684
2685 012232 005037 001100 RSTRT: CLR $UNIT ;CLEAR UNIT NUMBER
2686 012236 000137 003424 JMP BEGIN
2687
2688 012242 011646 WRPSW: MOV(SP),-(SP) ;COPY RETURN PC
2689 012244 013616 MOV @ (SP)+,(SP) ;MOVE NEW PSW TO STACK
2690 012246 062746 000002 ADD #2,-(SP) ;ADJUST JSR RETURN
2691 012252 000002 RTI ;POP RETURN PC & NEW PSW
2692
2693 ;SUBROUTINE TO REPORT UNEXPECTED OR ERRONEOUS TRAPS OR INTERRUPTS
2694
2695 012254 012600 CATCH: MOV (SP)+,RO ;GET ADDRESS OF TRAP VECTOR + 4
2696 012256 162700 000004 SUB #4,RO ;ADJUST TO POINT TO TRAP ADDRESS
2697 012262 010037 012302 MOV RO,BDVECT ;STORE TRAP OR INTERRUPT ADDRESS
2698 012266 016637 000002 012300 MOV 2(SP),OLDPC ;GET PC WHERE TRAP OR INTERRUPT OCCURRED
2699 012274 104112 ERROR 112 ;REPORT ERROR
2700
2701 012276 000000 HALT ;PROGRAM MUST BE RESTARTED AT THIS POINT
2702 012300 000000 OLDPC: .WORD 0
2703 012302 000000 BDVECT: .WORD 0
2704
```


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PAGE 74
APT COMMUNICATIONS ROUTINE

J 6

SEQ 0074

2952	000200	APTSIZE=200
2953	000001	APTENV=001
2954	000100	APTSPool=100
2955	000040	APTCSUP=040
2956		

