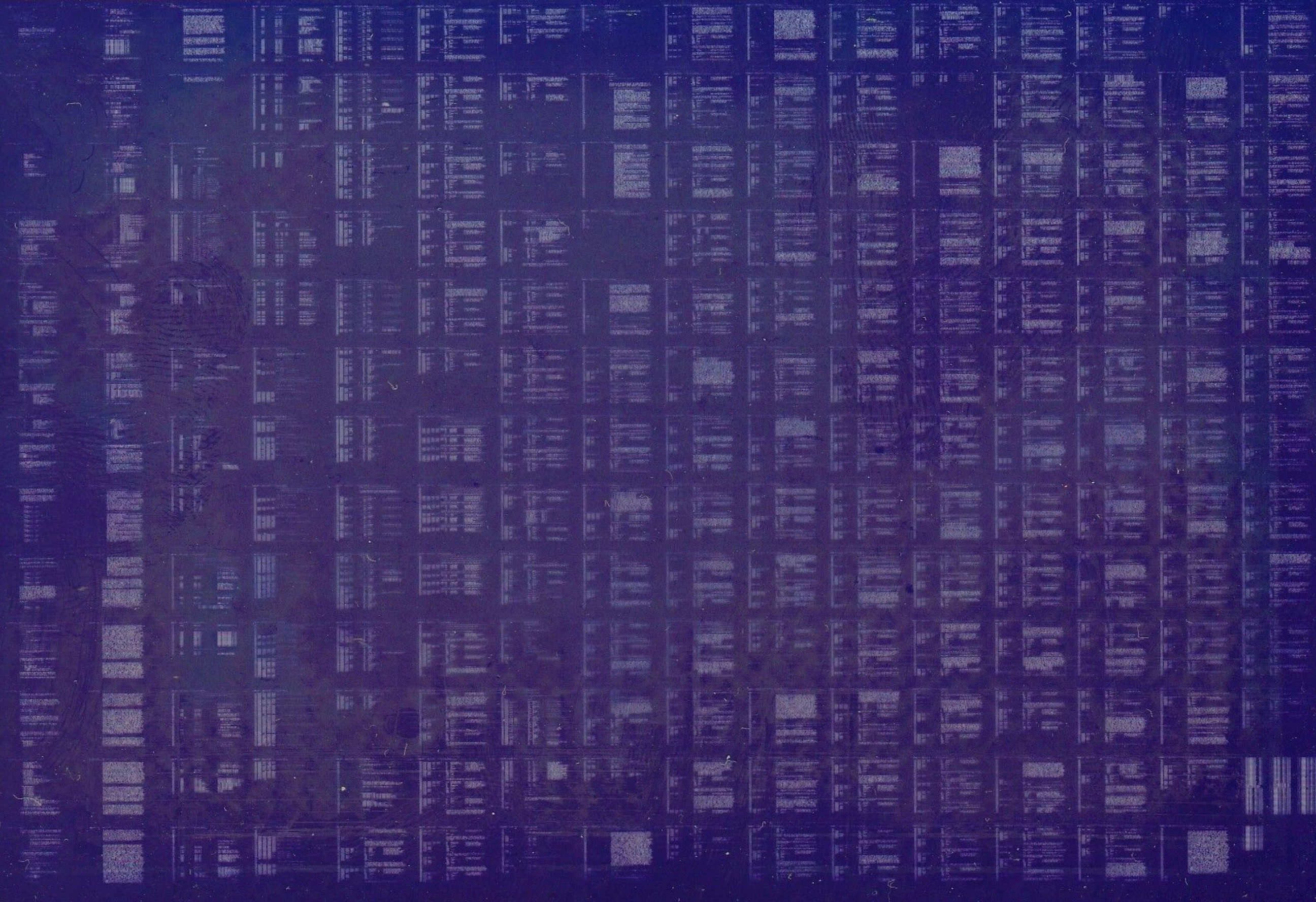


CDS-11

CDS11 SYS BUS DIAG
CVCDDAO

AH-T011A-MC
FICHE 1 OF 2

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CDS-11

CDS11 SYS BUS DIAG
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IDENTIFICATION

PRODUCT CODE: AC-T009A-MC
PRODUCT NAME: CVCDDA0 CDS-11 SYS BUS DIAG
PRODUCT DATE: SEPTEMBER 1981
MAINTAINER: DIAGNOSTIC ENGINEERING

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1.0 GENERAL INFORMATION

1.1 PROGRAM ABSTRACT

THE CDS-11 SYSTEM BUS DIAGNOSTIC WILL TEST THE LOGIC ON THE MEMORY SIMULATOR, THE STATE ANALYZER, THE POD, AND THE TARGET EMULATOR MODULES THAT WERE NOT TESTABLE RUNNING THE INDIVIDUAL CDS MODULE DIAGNOSTICS. THIS DIAGNOSTIC WILL NOT TEST THE SIGNALS TO AND FROM THE TARGET SYSTEM FROM THE POD MODULE. THE PROGRAM WILL USE EACH OF THE CDS MODULES TO SETUP THE LOGIC TO TEST THE LOGIC THAT WAS NOT TESTABLE PREVIOUSLY RUNNING THE INDIVIDUAL DIAGNOSTICS.

THIS DIAGNOSTIC HAS BEEN WRITTEN FOR USE WITH THE DIAGNOSTIC RUNTIME SERVICES SOFTWARE (SUPERVISOR). THESE SERVICES PROVIDE THE INTERFACE TO THE OPERATOR AND TO THE SOFTWARE ENVIRONMENT. THIS PROGRAM CAN BE USED WITH XXDP+, ACT, APT, SLIDE AND PAPER TAPE. FOR A COMPLETE DESCRIPTION OF THE RUNTIME SERVICES, REFER TO THE XXDP+ USER'S MANUAL. THERE IS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES IN SECTION 2 OF THIS DOCUMENT.

NOTE: THIS PROGRAM HAS NOT BEEN TESTED IN THE APT ENVIRONMENT, HOWEVER, THE APT INTERFACE HAS BEEN PROVIDED IN THE DIAGNOSTIC.

NOTE: THE T-11 POD MUST BE CONNECTED TO THE TARGET EMULATOR MODULE AND DISCONNECTED FROM THE TARGET SYSTEM BEFORE THE EXECUTION OF THIS DIAGNOSTIC.

1.2 SYSTEM REQUIREMENTS

1. LSI-11 OR EQUIVALENT TYPE CPU WITH Q-BUS
2. MINIMUM OF 16K WORDS OF MEMORY
3. CONSOLE TERMINAL AND CONTROLLER
4. CDS-11 BACKPLANE AND CABLES
5. MEMORY SIMULATOR MODULE (M8740)
6. STATE ANALYZER MODULE (M8741)
7. TARGET EMULATOR MODULE (M8742)
8. T-11 POD
9. MXV11 MODULE AND CDS-11 ROMS
10. STORAGE DEVICE WITH CONTROLLER (OPTIONAL)
11. XXDP+ MEDIA FOR STORAGE DEVICE (OPTIONAL)

1.3 RELATED DOCUMENTS AND STANDARDS

CHQUS? XXDP+ USER'S MANUAL (THE "?" IN CHQUS INDICATES THE REVISION LEVEL OF THE DOCUMENT. AT THE TIME THIS PROGRAM WAS WRITTEN, THE REVISION LEVEL WAS 'E').

1.4 DIAGNOSTIC HIERARCHY PREREQUISITES

ALL HARDWARE THAT IS SPECIFIED IN SECTION 1.2 OF THIS DOCUMENT MUST BE OPERATIONAL AND FREE OF ALL FAULTS.

1.5 ASSUMPTIONS

BEFORE THIS PROGRAM IS EXECUTED, IT IS ASSUMED THAT THE FOLLOWING DIAGNOSTICS HAVE RUN SUCCESSFULLY.

CDS-11 MEMORY SIMULATOR DIAGNOSTIC
CDS-11 STATE ANALYZER DIAGNOSTIC
CDS-11 TARGET EMULATOR DIAGNOSTIC

2.0 OPERATING INSTRUCTIONS

THIS SECTION CONTAINS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES. FOR DETAILED INFORMATION, REFER TO THE XXDP+ USER'S MANUAL (CHQUS).

2.1 COMMANDS

THERE ARE ELEVEN LEGAL COMMANDS FOR THE DIAGNOSTIC RUNTIME SERVICES (SUPERVISOR). THIS SECTION LISTS THE COMMANDS AND GIVES A VERY BRIEF DESCRIPTION OF THEM. THE XXDP+ USER'S MANUAL HAS MORE DETAILS.

COMMAND	EFFECT
START	START THE DIAGNOSTIC FROM AN INITIAL STATE
RESTART	START THE DIAGNOSTIC WITHOUT INITIALIZING
CONTINUE	CONTINUE AT TEST THAT WAS INTERRUPTED (AFTER ^C)
PROCEED	CONTINUE FROM AN ERROR HALT
EXIT	RETURN TO XXDP+ MONITOR (XXDP+ OPERATION ONLY!)
ADD	ACTIVATE A UNIT FOR TESTING (ALL UNITS ARE CONSIDERED TO BE ACTIVE AT START TIME)
DROP	DEACTIVATE A UNIT
PRINT	PRINT STATISTICAL INFORMATION (IF IMPLEMENTED BY THE DIAGNOSTIC - SECTION 4.0)
DISPLAY	TYPE A LIST OF ALL DEVICE INFORMATION
FLAGS	TYPE THE STATE OF ALL FLAGS (SEE SECTION 2.3)
ZFLAGS	CLEAR ALL FLAGS (SEE SECTION 2.3)

A COMMAND CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. SO YOU MAY, FOR EXAMPLE, TYPE 'STA' INSTEAD OF 'START'.

2.2 SWITCHES

THERE ARE SEVERAL SWITCHES WHICH ARE USED TO MODIFY SUPERVISOR OPERATION. THESE SWITCHES ARE APPENDED TO THE LEGAL COMMANDS. ALL OF THE LEGAL SWITCHES ARE TABULATED BELOW WITH A BRIEF DESCRIPTION OF EACH. IN THE DESCRIPTIONS BELOW, A DECIMAL NUMBER IS DESIGNATED BY 'DDDDD'.

SWITCH	EFFECT
/TESTS:LIST	EXECUTE ONLY THOSE TESTS SPECIFIED IN THE LIST. LIST IS A STRING OF TEST NUMBERS, FOR EXAMPLE - /TESTS:1:5:7-10. THIS LIST WILL CAUSE TESTS 1,5,7,8,9,10 TO BE RUN. ALL OTHER TESTS WILL NOT BE RUN.
/PASS:DDDDD	EXECUTE DDDDD PASSES (DDDDD = 1 TO 64000)
/FLAGS:FLGS	SET SPECIFIED FLAGS. FLAGS ARE DESCRIBED IN SECTION 2.3.
/EOP:DDDDD	REPORT END OF PASS MESSAGE AFTER EVERY DDDDD PASSES ONLY. (DDDDD = 1 TO 64000)

/UNITS:LIST TEST/ADD/DROP ONLY THOSE UNITS SPECIFIED
IN THE LIST. LIST EXAMPLE - /UNITS:0:5:10-12
USE UNITS 0,5,10,11,12 (UNIT NUMBERS = 0-63)

EXAMPLE OF SWITCH USAGE:

START/TESTS:1-5/PASS:1000/EOP:100

THE EFFECT OF THIS COMMAND WILL BE: 1) TESTS 1 THROUGH 5 WILL BE EXECUTED, 2) ALL UNITS WILL BE TESTED 1000 TIMES AND 3) THE END OF PASS MESSAGES WILL BE PRINTED AFTER EACH 100 PASSES ONLY. A SWITCH CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. YOU MAY, FOR EXAMPLE, TYPE "/TES:1-5" INSTEAD OF "/TESTS:1-5".

BELOW IS A TABLE THAT SPECIFIES WHICH SWITCHES CAN BE USED BY EACH COMMAND.

	TESTS	PASS	FLAGS	EOP	UNITS
START	X	X	X	X	X
RESTART	X	X	X	X	X
CONTINUE		X	X	X	
PROCEED			X		
DROP					X
ADD					X
PRINT					
DISPLAY					X
FLAGS					
ZFLAGS					
EXIT					

2.3 FLAGS

FLAGS ARE USED TO SET UP CERTAIN OPERATIONAL PARAMETERS SUCH AS LOOPING ON ERROR. ALL FLAGS ARE CLEARED AT STARTUP AND REMAIN CLEARED UNTIL EXPLICITLY SET USING THE FLAGS SWITCH. FLAGS ARE ALSO CLEARED AFTER A START COMMAND UNLESS SET USING THE FLAG SWITCH. THE ZFLAGS COMMAND MAY ALSO BE USED TO CLEAR ALL FLAGS. WITH THE EXCEPTION OF THE START AND ZFLAGS COMMANDS, NO COMMANDS AFFECT THE STATE OF THE FLAGS; THEY REMAIN SET OR CLEARED AS SPECIFIED BY THE LAST FLAG SWITCH.

FLAG	EFFECT
HOE	HALT ON ERROR - CONTROL IS RETURNED TO RUNTIME SERVICES COMMAND MODE
LOE	LOOP ON ERROR
IER*	INHIBIT ALL ERROR REPORTS
IBE*	INHIBIT ALL ERROR REPORTS EXCEPT FIRST LEVEL (FIRST LEVEL CONTAINS ERROR TYPE, NUMBER, PC, TEST AND UNIT)
IXE*	INHIBIT EXTENDED ERROR REPORTS (THOSE CALLED BY PRINTX MACRO'S)
PRI	DIRECT MESSAGES TO LINE PRINTER
PNT	PRINT TEST NUMBER AS TEST EXECUTES

BOE	'BELL' ON ERROR
UAM	UNATTENDED MODE (NO MANUAL INTERVENTION)
ISR	INHIBIT STATISTICAL REPORTS (DOES NOT APPLY TO DIAGNOSTICS WHICH DO NOT SUPPORT STATISTICAL REPORTING)
IDR	INHIBIT PROGRAM DROPPING OF UNITS
ADR	EXECUTE AUTODROP CODE
LOT	LOOP ON TEST
EVL	EXECUTE EVALUATION (ON DIAGNOSTICS WHICH HAVE EVALUATION SUPPORT)

*ERROR MESSAGES ARE DESCRIBED IN SECTION 3.1

SEE THE XXDP+ USER'S MANUAL FOR MORE DETAILS ON FLAGS. YOU MAY SPECIFY MORE THAN ONE FLAG WITH THE FLAG SWITCH. FOR EXAMPLE, TO CAUSE THE PROGRAM TO LOOP ON ERROR, INHIBIT ERROR REPORTS AND TYPE A 'BELL' ON ERROR, YOU MAY USE THE FOLLOWING STRING:

/FLAGS:LOE:IER:BOE

2.4 HARDWARE QUESTIONS

WHEN A DIAGNOSTIC IS STARTED, THE RUNTIME SERVICES WILL PROMPT THE USER FOR HARDWARE INFORMATION BY TYPING "CHANGE HW (L) ?" YOU MUST ANSWER "Y" AFTER A START COMMAND UNLESS THE HARDWARE INFORMATION HAS BEEN "PRELOADED" USING THE SETUP UTILITY (SEE CHAPTER 6 OF THE XXDP+ USER'S MANUAL). WHEN YOU ANSWER THIS QUESTION WITH A "Y", THE RUNTIME SERVICES WILL ASK FOR THE NUMBER OF UNITS (IN DECIMAL). YOU WILL THEN BE ASKED THE FOLLOWING QUESTIONS FOR EACH UNIT.

CSR ADDRESS:
VECTOR ADDRESS:
DEVICE NUMBER FOR MEMORY SIMULATOR:
DEVICE NUMBER FOR STATE ANALYZER:
DEVICE NUMBER FOR TARGET EMULATOR:

2.5 SOFTWARE QUESTIONS

AFTER YOU HAVE ANSWERED THE HARDWARE QUESTIONS OR AFTER A RESTART OR CONTINUE COMMAND, THE RUNTIME SERVICES WILL ASK FOR SOFTWARE PARAMETERS. THESE PARAMETERS WILL GOVERN SOME DIAGNOSTIC SPECIFIC OPERATION MODES. YOU WILL BE PROMPTED BY "CHANGE SW (L) ?" IF YOU WISH TO CHANGE ANY PARAMETERS, ANSWER BY TYPING "Y". THE SOFTWARE QUESTIONS AND THE DEFAULT VALUES ARE DESCRIBED IN THE NEXT PARAGRAPH(S).

THERE ARE NO SOFTWARE QUESTIONS IN THIS PROGRAM.

2.6 EXTENDED P-TABLE DIALOGUE

WHEN YOU ANSWER THE HARDWARE QUESTIONS, YOU ARE BUILDING ENTRIES

IN A TABLE THAT DESCRIBES THE DEVICES UNDER TEST. THE SIMPLEST WAY TO BUILD THIS TABLE IS TO ANSWER ALL QUESTIONS FOR EACH UNIT TO BE TESTED. IF YOU HAVE A MULTIPLEXED DEVICE SUCH AS A MASS STORAGE CONTROLLER WITH SEVERAL DRIVES OR A COMMUNICATION DEVICE WITH SEVERAL LINES, THIS BECOMES TEDIOUS SINCE MOST OF THE ANSWERS ARE REPETITIOUS.

TO ILLUSTRATE A MORE EFFICIENT METHOD, SUPPOSE YOU ARE TESTING A FICTIONAL DEVICE, THE XY11. SUPPOSE THIS DEVICE CONSISTS OF A CONTROL MODULE WITH EIGHT UNITS (SUB-DEVICES) ATTACHED TO IT. THESE UNITS ARE DESCRIBED BY THE OCTAL NUMBERS 0 THROUGH 7. THERE IS ONE HARDWARE PARAMETER THAT CAN VARY AMONG UNITS CALLED THE Q-FACTOR. THIS Q-FACTOR MAY BE 0 OR 1. BELOW IS A SIMPLE WAY TO BUILD A TABLE FOR ONE XY11 WITH EIGHT UNITS.

```
# UNITS (D) ? 8<CR>

UNIT 1
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 0<CR>
Q-FACTOR (O) 0 ? 1<CR>

UNIT 2
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 1<CR>
Q-FACTOR (O) 1 ? 0<CR>

UNIT 3
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 2<CR>
Q-FACTOR (O) 0 ? <CR>

UNIT 4
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 3<CR>
Q-FACTOR (O) 0 ? <CR>

UNIT 5
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 4<CR>
Q-FACTOR (O) 0 ? <CR>

UNIT 6
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 5<CR>
Q-FACTOR (O) 0 ? <CR>

UNIT 7
CSR ADDRESS (O) ? 160000<CR>
SUB-DEVICE # (O) ? 6<CR>
Q-FACTOR (O) 0 ? 1<CR>

UNIT 8
CSR ADDRESS (O) 160000<CR>
SUB-DEVICE # (O) ? 7<CR>
Q-FACTOR (O) 1 ? <CR>
```


NOTICE THAT THE DEFAULT VALUE FOR THE Q-FACTOR CHANGES WHEN A NON-DEFAULT RESPONSE IS GIVEN. BE CAREFUL WHEN SPECIFYING MULTIPLE UNITS!

AS YOU CAN SEE FROM THE ABOVE EXAMPLE, THE HARDWARE PARAMETERS DO NOT VARY SIGNIFICANTLY FROM UNIT TO UNIT. THE PROCEDURE SHOWN IS NOT VERY EFFICIENT.

THE RUNTIME SERVICES CAN TAKE MULTIPLE UNIT SPECIFICATIONS HOWEVER. LET'S BUILD THE SAME TABLE USING THE MULTIPLE SPECIFICATION FEATURE.

```
# UNITS (D) ? 8<CR>

UNIT 1
CSR ADDRESS (0) ? 160000<CR>
SUB-DEVICE # (0) ? 0,1<CR>
Q-FACTOR (0) 0 ? 1,0<CR>

UNIT 3
CSR ADDRESS (0) ? 160000<CR>
SUB-DEVICE # (0) ? 2-5<CR>
Q-FACTOR (0) 0 ? 0<CR>

UNIT 7
CSR ADDRESS (0) ? 160000<CR>
SUB-DEVICE # (0) ? 6,7<CR>
Q-FACTOR (0) 0 ? 1<CR>
```

AS YOU CAN SEE IN THE ABOVE DIALOGUE, THE RUNTIME SERVICES WILL BUILD AS MANY ENTRIES AS IT CAN WITH THE INFORMATION GIVEN IN ANY ONE PASS THROUGH THE QUESTIONS. IN THE FIRST PASS, TWO ENTRIES ARE BUILT SINCE TWO SUB-DEVICES AND Q-FACTORS WERE SPECIFIED. THE SERVICES ASSUME THAT THE CSR ADDRESS IS 160000 FOR BOTH SINCE IT WAS SPECIFIED ONLY ONCE. IN THE SECOND PASS, FOUR ENTRIES WERE BUILT. THIS IS BECAUSE FOUR SUB-DEVICES WERE SPECIFIED. THE "-" CONSTRUCT TELLS THE RUNTIME SERVICES TO INCREMENT THE DATA FROM THE FIRST NUMBER TO THE SECOND. IN THIS CASE, SUB-DEVICES 2, 3, 4 AND 5 WERE SPECIFIED. (IF THE SUB-DEVICE WERE SPECIFIED BY ADDRESSES, THE INCREMENT WOULD BE BY 2 SINCE ADDRESSES MUST BE ON AN EVEN BOUNDARY.) THE CSR ADDRESSES AND Q-FACTORS FOR THE FOUR ENTRIES ARE ASSUMED TO BE 160000 AND 0 RESPECTIVELY SINCE THEY WERE ONLY SPECIFIED ONCE. THE LAST TWO UNITS ARE SPECIFIED IN THE THIRD PASS.

THE WHOLE PROCESS COULD HAVE BEEN ACCOMPLISHED IN ONE PASS AS SHOWN BELOW.

```
# UNITS (D) ? 8<CR>

UNIT 1
CSR ADDRESS (0) ? 160000<CR>
SUB-DEVICE # (0) ? 0-7<CR>
Q-FACTOR (0) 0 ? 0,1,0,,,,1,1<CR>
```


AS YOU CAN SEE FROM THIS EXAMPLE, NULL REPLIES (COMMAS ENCLOSING A NULL FIELD) TELL THE RUNTIME SERVICES TO REPEAT THE LAST REPLY.

2.7 QUICK START-UP PROCEDURE (XXDP+)

NOTE: THE T-11 POD MUST BE CONNECTED TO THE TARGET EMULATOR AND DISCONNECTED FROM THE TARGET SYSTEM BEFORE EXECUTION OF THIS DIAGNOSTIC.

TO START-UP THIS PROGRAM:

1. BOOT XXDP+
2. ANSWER ANY QUESTIONS ASKED AND GIVE THE DATE.
3. TYPE 'R NAME', WHERE NAME IS THE NAME OF THE BIN OR BIC FILE FOR THIS PROGRAM
4. TYPE "START"
5. ANSWER THE "CHANGE HW" QUESTION WITH "Y"
6. ANSWER ALL THE HARDWARE QUESTIONS
7. ANSWER THE "CHANGE SW" QUESTION WITH "N"

WHEN YOU FOLLOW THIS PROCEDURE YOU WILL BE USING ONLY THE DEFAULTS FOR FLAGS AND SOFTWARE PARAMETERS. THESE DEFAULTS ARE DESCRIBED IN SECTIONS 2.3 AND 2.5.

3.0 ERROR INFORMATION

3.1 TYPES OF ERROR MESSAGES

THERE ARE THREE LEVELS OF ERROR MESSAGES THAT MAY BE ISSUED BY A DIAGNOSTIC: GENERAL, BASIC AND EXTENDED. GENERAL ERROR MESSAGES ARE ALWAYS PRINTED UNLESS THE "IER" FLAG IS SET (SECTION 2.3). THE GENERAL ERROR MESSAGE IS OF THE FORM:

NAME TYPE NUMBER ON UNIT NUMBER TST NUMBER PC:XXXXXX
ERROR MESSAGE

,WHERE; NAME = DIAGNOSTIC NAME
TYPE = ERROR TYPE (SYS FATAL, DEV FATAL, HARD OR SOFT)
NUMBER = ERROR NUMBER
UNIT NUMBER = 0 - N (N IS LAST UNIT IN PTABLE)
TST NUMBER = TEST AND SUBTEST WHERE ERROR OCCURRED
PC:XXXXXX = ADDRESS OF ERROR MESSAGE CALL

BASIC ERROR MESSAGES ARE MESSAGES THAT CONTAIN SOME ADDITIONAL INFORMATION ABOUT THE ERROR. THESE ARE ALWAYS PRINTED UNLESS THE "IER" OR "IBE" FLAGS ARE SET (SECTION 2.3). THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL MESSAGE.

EXTENDED ERROR MESSAGES CONTAIN SUPPLEMENTARY ERROR INFORMATION SUCH AS REGISTER CONTENTS OR GOOD/BAD DATA. THESE ARE ALWAYS

PRINTED UNLESS THE "IER", "IBE" OR "IXE" FLAGS ARE SET (SECTION 2.3). THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL ERROR MESSAGE AND ANY ASSOCIATED BASIC ERROR MESSAGES.

3.2 SPECIFIC ERROR MESSAGES

WHEN AN ERROR IS REPORTED ON THE CONSOLE TERMINAL, THE USER SHOULD REFER TO THE PROGRAM LISTING FOR THE TEST SEQUENCE BEING PERFORMED AT THE TIME THE ERROR WAS DETECTED. THE "PC" REPORTED IN THE ERROR MESSAGE INDICATES THE ADDRESS OF THE ERROR CALL. EACH STEP OF A TEST IS DESCRIBED IN DETAIL TO HELP THE USER UNDERSTAND THE TEST SEQUENCE. ONCE UNDERSTANDING THE TEST SEQUENCE, THE USER SHOULD BE ABLE TO DETERMINE THE FAULT OR FAULTS WHICH COULD CAUSE THE ERROR.

AN EXAMPLE OF AN ERROR PRINTOUT IS SHOWN BELOW:

```
CVCDD DVC FTL ERR 0000X ON UNIT 00 TST 001 SUB 000 PC: XXXXXX  
ERROR TYPE MESSAGE (SEE BELOW)  
CONTROL REG X ERROR  
REGX = LOAD: XXXXXX READ: XXXXXX  
OR  
REGX = LOAD: XXXXXX GOOD: XXXXXX READ: XXXXXX
```

THE FIRST LINE OF THE ERROR PRINTOUT ABOVE IS DESCRIBED IN SECTION 3.1 OF THIS DOCUMENT. THE ERROR NUMBER, 0000X, IN THE FIRST LINE OF THE ERROR PRINTOUT WILL INDICATE THE CONTROL REGISTER THAT THE PROGRAM DETECTED AN ERROR IN, AND THE MODULE THAT WAS SELECTED AT THE TIME THE ERROR OCCURED. USING THE ERROR NUMBER PRINTED IN THE ERROR MESSAGE, DETERMINE FROM THE TABLE BELOW WHICH MODULE WAS SELECTED AND WHICH CONTROL REGISTER WAS IN ERROR.

CONTROL REG IN ERROR	MEMORY SIMULATOR ERROR NUMBERS	STATE ANALYZER ERROR NUMBERS	TARGET EMULATOR ERROR NUMBERS
0	1	5	9
2	2	6	10
4	3	7	11
6	4	8	12

TO HELP THE USER TO DETERMINE THE FAILURE, THE PROGRAM WILL PRINT THE SECOND LINE OF THE ABOVE ERROR MESSAGE. THIS MESSAGE WILL ATTEMPT TO INDICATE TO THE USER THE AREA OF LOGIC BEING TESTED AT THE TIME THE FAILURE OCCURED. THIS "ERROR TYPE MESSAGE" WILL NOT BE PRINTED FOR ALL ERRORS.

THE "ERROR TYPE MESSAGES" ARE LISTED BELOW BY MODULES AND THE CONTROL REGISTERS FOR WHICH THEY ARE REPORTED.

```
MEMORY SIMULATOR MODULE  
CONTROL REGISTER 0  
NO "ERROR TYPE MESSAGES" FOR THIS CONTROL REGISTER  
CONTROL REGISTER 2  
TE TO MS ADDRESS BUS ERROR - MSAD 17:16  
MAP PROTECT LOGIC ERROR  
CONTROL REGISTER 4
```


MSAD 15:0 REG ERROR
TE TO MS ADDRESS BUS ERROR - MSAD 15:0
CONTROL REGISTER 6
DATA ERROR IN MAP PROTECT RAM
DATA ERROR IN MODULE SELECT RAM 0
DATA ERROR IN MODULE SELECT RAM 1
DATA ERROR IN MEMORY SIMULATOR RAM

STATE ANALYZER MODULE

CONTROL REGISTER 0
CDAL 15:0 REG ERROR
CONTROL REGISTER 2
PDAL 7:0 REG ERROR
CONTROL REGISTER 4
OR ARRAY RAM DATA ERROR - ORO 7:0
FUSL7 FLIP-FLOP - OR ARRAY RAM DATA ERROR
CONTROL REGISTER 6
TE TO SA ADDRESS BUS ERROR - TRDI 15:0
TE TO SA - XSEL1, EDSELO, ADDR 17:16 + BTS 3:0 ERROR - TRDI 47:32
TE CTL BUS 7:0 TO SA TRDI BUS BITS 47:40 ERROR
MS RAM DATA TO SA TRDI BUS BITS 31:16 ERROR
TRACE RAM ADDRESS REG ERROR - TRAD 10:0
OR ADDRESS REG ERROR - ORAD 3:0
FUSL 3:0 FLIP-FLOP ERROR

TARGET EMULATOR MODULE

CONTROL REGISTER 0
GDAL 15:0 REG ERROR
CONTROL REGISTER 2
ADAL 15:0 REG ERROR
CONTROL REGISTER 4
VDAL 7:0 OR PAUSE STATE MACHINE ERROR
CONTROL REGISTER 6
HDAL 15:0 REG ERROR
MR 15:0 REG ERROR
FDAL 7:0 REG ERROR
EOAI 7:0 OR FDAL 7:0 REG ERROR
CTL 7:0 OR FDAL 7:0 REG ERROR
DIAG ADDR 15:0 REG ERROR
FORCE JUMP ADDRESS READBCK REG ERROR
MS RAM DATA TO TE EODAL BUS ERROR VIA SYSTEM DATA BUS
MS RAM DATA TO TE EIDAL BUS ERROR VIA EODAL + SYSTEM DATA BUS
MS RAM DATA TO TE EIDAL BUS ERROR VIA TDAL BUS LATCHES
MEMBRK H FAILED TO SET BREAK FLIP-FLOP OR FAILED TO INTERRUPT
FDAL REG 7:2 TO EODAL BUS ERROR
FDAL REG 7:2 TO EIDAL BUS ERROR
FDAL REG 7:2 TO TDAL LATCHES TO EIDAL BUS ERROR

THE THIRD LINE OF THE ERROR PRINTOUT, WHICH MAY BE THE SECOND LINE IF THE 'ERROR TYPE MESSAGE' IS NOT PRINTED, WILL INDICATE THE CONTROL REGISTER (0, 2, 4 OR 6) THAT THE PROGRAM DETECTED IN ERROR.

THE LAST PORTION OF THE ERROR PRINTOUT WILL INDICATE CONTROL REGISTER INFORMATION. ON SOME ERRORS, DATA FOR MORE THEN ONE CONTROL REGISTER WILL BE PRINTED OUT. THIS IS DONE TO HELP THE USER TO DETERMINE THE FAULT ON ERRORS WHICH REQUIRE PREVIOUS CONTROL REGISTER SETUP. IF

MORE THEN ONE CONTROL REGISTER IS PRINTED, THE PREVIOUS MESSAGE "CONTROL REG X ERROR" WILL INDICATE THE CONTROL REGISTER THAT THE PROGRAM FOUND IN ERROR. A DESCRIPTION OF THE WORDS USED TO INDICATE CONTROL REGISTER INFORMATION IS AS FOLLOWS:

REGX: 'X' OF 'REGX' WILL INDICATE THE CONTROL REGISTER FOR WHICH THE FOLLOWING DATA IS REPORTED. 'X' WILL BE A 0, 2, 4 OR 6.

LOAD: DATA THAT WAS LOADED INTO THE CONTROL REGISTER OR THE EXPECTED DATA TO BE IN THE CONTROL REGISTER ON A READ.

GOOD: EXPECTED DATA TO BE IN THE CONTROL REGISTER ON A READ. THIS PORTION OF THE CONTROL REGISTER INFORMATION WILL ONLY BE PRINTED IN THE PROGRAM EXPECTS "READ ONLY" BITS OF THE CONTROL REGISTER TO BE SET.

READ: DATA THAT WAS READ FROM CONTROL REGISTER VIA THE PROGRAM

XXXXXX: SIX OCTAL DIGITS INDICATING THE DATA FOR THE ABOVE WORDS

4.0 PERFORMANCE AND PROGRESS REPORTS

AT THE END OF EACH PASS, THE PASS COUNT IS GIVEN ALONG WITH THE TOTAL NUMBER OF ERRORS REPORTED SINCE THE DIAGNOSTIC WAS STARTED. THE "EOP" SWITCH CAN BE USED TO CONTROL HOW OFTEN THE END OF PASS MESSAGE IS PRINTED. SECTION 2.2 DESCRIBES SWITCHES.

5.0 DEVICE INFORMATION TABLES

5.1 DEVICE INFORMATION FOR MEMORY SIMULATOR

CONTROL REGISTER 0 (163010)

15	ID H	BIT15 = 1 READ DEVICE TYPE IN BITS 11:8, MEMORY SIMULATOR DEVICE TYPE EQUALS 1 (0400)
		BIT 15 = 0 READ DEVICE NUMBER INTO BITS 11:8
14	SIG14H	ALWAYS A 0 ON READ
13	SIG13H	ALWAYS A 0 ON READ
12	SIG12H	ALWAYS A 0 ON READ
		BITS 11:8 ARE USED TO SELECT THE DEVICE NUMBER OF THE MEMORY SIMULATOR. THESE BITS MUST BE EQUAL TO THE SETTING OF SWITCHES DEV 3, DEV 2, DEV 1 AND DEV 0.
11	SIG11H	DEVICE NUMBER/TYPE
10	SIG10H	DEVICE NUMBER/TYPE
9	SIG9H	DEVICE NUMBER/TYPE
8	SIG8H	DEVICE NUMBER/TYPE
7		SPARE
6	CKH	CLOCK HIGH (R/W)
5	WRVH	WRITE VIOLATION F/F (READ ONLY)

- 4 RDVH READ VIOLATION F/F (READ ONLY)
- 3 8BITH 8 BIT MODE (1) - 16 BIT MODE (0) - (R/W)
- 2 MPH MAP PROTECT SELECT (R/W)
- 1 CTSH MEM ACCESS FROM LSI-11 BUS (0) - (R/W)
- MEM ACCESS FROM SYSTEM BUS (1) - (R/W)
- 0 RSTH BIT 0 = 1 RESET MEMORY SIMULATOR MODULE (R/W)

CONTROL REGISTER 2 (163012)

15:8 THESE BITS ARE NOT AVAILABLE IN THIS CONTROL REGISTER

- 7 MSBRKH MEMORY SIMULATOR BREAK (READ ONLY)
- 6 WRENH MAP PROTECT RAM SIGNAL WRE H (READ ONLY)
- 5 ESRH MAP PROTECT RAM SIGNAL MPIN H (READ ONLY)

4 SPARE - ALWAYS A 0 ON READ (READ ONLY)

- 3 MSEL1H MEMORY SELECT (R/W)
- 2 MSEL0H MEMORY SELECT (R/W)

MSEL1	MSEL0	
0	0	SELECT SIMULATOR MEMORY - SSM L
0	1	SELECT MODULE SELECT MEMORY 0 - SMDS0 L
1	0	SELECT MAP PROTECT MEMORY - SMPM L
1	1	SELECT MODULE SELECT MEMORY 1 - SMDS1 L

- 1 MSAD17H MEMORY SIMULATOR ADDRESS 17 (R/W)
- 0 MSAD16H MEMORY SIMULATOR ADDRESS 16 (R/W)

CONTROL REGISTER 4 (163014) - MSAD 15:0 REGISTER

- 15 MSAD15H MEMORY SIMULATOR ADDRESS 15 (R/W)
- 14 MSAD14H MEMORY SIMULATOR ADDRESS 14 (R/W)
- 13 MSAD13H MEMORY SIMULATOR ADDRESS 13 (R/W)
- 12 MSAD12H MEMORY SIMULATOR ADDRESS 12 (R/W)
- 11 MSAD11H MEMORY SIMULATOR ADDRESS 11 (R/W)
- 10 MSAD10H MEMORY SIMULATOR ADDRESS 10 (R/W)
- 9 MSAD9H MEMORY SIMULATOR ADDRESS 09 (R/W)
- 8 MSAD8H MEMORY SIMULATOR ADDRESS 08 (R/W)
- 7 MSAD7H MEMORY SIMULATOR ADDRESS 07 (R/W)
- 6 MSAD6H MEMORY SIMULATOR ADDRESS 06 (R/W)
- 5 MSAD5H MEMORY SIMULATOR ADDRESS 05 (R/W)
- 4 MSAD4H MEMORY SIMULATOR ADDRESS 04 (R/W)
- 3 MSAD3H MEMORY SIMULATOR ADDRESS 03 (R/W)
- 2 MSAD2H MEMORY SIMULATOR ADDRESS 02 (R/W)
- 1 MSAD1H MEMORY SIMULATOR ADDRESS 01 (R/W)
- 0 MSAD0H MEMORY SIMULATOR ADDRESS 00 (R/W)

CONTROL REGISTER 6 (163016)

WHEN THE MAP PROTECTION RAM IS SELECTED VIA CONTROL REGISTER 2,
THE FOLLOWING BITS ARE LOADED INTO OR READ FROM THE MAP PROTECTION
RAMS VIA CONTROL REGISTER 6

- 3 MUTBH NOT USED

2 RDEH BIT 2 = 1 MEMORY IS READ ENABLED
1 WREH BIT 1 = 1 MEMORY IS WRITE ENABLED
0 MPINH BIT 0 = 1 SELECT MEMORY SIMULATOR RAM NOT TARGET RAM

WHEN MODULE SELECT RAM 0 OR 1 IS SELECTED VIA CONTROL REGISTER 2,
THE FOLLOWING BITS ARE LOADED INTO OR READ FROM MODULE SELECT RAMS
0 OR 1 VIA CONTROL REGISTER 6.

3 EN3H SELECTS 4TH BANK OF MEMORY SIMULATOR MEMORY
2 EN2H SELECTS 3RD BANK OF MEMORY SIMULATOR MEMORY
1 EN1H SELECTS 2ND BANK OF MEMORY SIMULATOR MEMORY
0 EN0H SELECTS 1ST BANK OF MEMORY SIMULATOR MEMORY

WHEN THE MEMORY SIMULATOR RAMS ARE SELECTED VIA CONTROL REGISTER 2,
ALL 16 BITS ARE LOADED INTO AND READ FROM THE SIMULATOR MEMORY RAMS
VIA CONTROL REGISTER 2.

5.2 DEVICE INFORMATION FOR STATE ANALYZER

CONTROL REGISTER 0 (163010) - CDAL REGISTER

15 CDAL15 BIT 15 = 1 READ DEVICE TYPE IN BITS 11:8. STATE
ANALYZER DEVICE TYPE EQUALS 2 (1000)

BIT 15 = 0 READ DEVICE NUMBER INTO BITS 11:8.

14 CDAL14 ALWAYS A 0 ON READ
13 CDAL13 ALWAYS A 0 ON READ
12 CDAL12 ALWAYS A 0 ON READ

BITS 11:8 ARE USED TO SELECT THE DEVICE NUMBER OF
THE STATE ANALYZER. THESE BITS MUST BE EQUAL TO THE
SETTING OF SWITCHES DEV 3, DEV 2, DEV 1 AND DEV 0.

11 CDAL11 DEVICE NUMBER/TYPE
10 CDAL10 DEVICE NUMBER/TYPE
9 CDAL9 DEVICE NUMBER/TYPE
8 CDAL8 DEVICE NUMBER/TYPE

7 CDAL7 1 - DISABLE OUTPUTS OF "OR ADDRESS REG" - ENABLE
FOUT 3:0 TO DRIVE "OR" ADDRESS
0 - ENABLE OUTPUTS OF "OR ADDRESS REG"

6 CDAL6 1/0 CLOCK THE SIGNAL "TRANST H"

5 CDAL5 1 - STOP TRACING WHEN "TRAD10 H" SET HIGH
0 - CONTINUOUS TRACING

4 CDAL4 1 - ENABLE ALL AND/OR ARRAY RAMS
0 - ENABLE ONLY ONE AND/OR ARRAY RAM AT A TIME

3 CDAL3 TRACE RAM BUS SELECT
2 CDAL2 TRACE RAM BUS SELECT

CDAL3 CDAL2

0	0	ENABLE OUTPUTS OF TRACE RAM DATA IN BUFFER ONTO TRACE RAM BUS
0	1	ENABLE TRACE RAM DATA ONTO TRACE RAM BUS
1	0	ENABLE SYSTEM BUS AND SBL 59:56 FLIP-FLOPS ONTO TRACE RAM BUS

- 1 CDAL1 1 - ENABLE FUNCTION SELECT FLIP-FLOPS ONTO SYSTEM BUS
0 - DISABLE FUNCTION SELECT FLIP-FLOPS FROM SYSTEM BUS
- 0 CDAL0 1 - CLEAR TRACE RAM ADDRESS REGISTER, CLEAR TRACING FLIP FLOP, CLEAR SBL 59:56 FLIP-FLOPS, AND RELOAD EVENT COUNTERS FROM EVENT COUNTER REGISTERS.

CONTROL REGISTER 2 (163012) - PDAL REGISTER

15:8 BITS 15:8 ARE NOT AVAILABLE FOR THIS REGISTER

7	PDAL7	1 - CLEAR EVENT COUNTERS
6	PDAL6	1 - PRESET TRACING FLIP-FLOP
5	PDAL5	0 - PRESET FUNCTION SELECT FLIP-FLOPS
4	PDAL4	1 - EXTERNAL PROBE "CLK" SIGNAL WILL LOAD EXTP 7:0 FLIP-FLOPS WHEN "CLK" IS SET LOW. 0 - EXTERNAL PROBE "CLK" SIGNAL WILL LOAD EXTP 7:0 FLIP-FLOPS WHEN "CLK" IS SET HIGH.
3	PDAL3	SELECT POINTER REGISTER
2	PDAL2	SELECT POINTER REGISTER
1	PDAL1	SELECT POINTER REGISTER
0	PDAL0	SELECT POINTER REGISTER

STATE ANALYZER'S POINTER REGISTER AND CONTROL REGISTER 4 (163014)

PDAL BITS 3:0 - SIGNAL - DESCRIPTION

00	PTER0 L	WRITE/READ AND ARRAY RAM 0
01	PTER1 L	WRITE/READ AND ARRAY RAM 1
02	PTER2 L	WRITE/READ AND ARRAY RAM 2
03	PTER3 L	WRITE/READ AND ARRAY RAM 3
04	PTER4 L	WRITE/READ AND ARRAY RAM 4
05	PTER5 L	WRITE/READ AND ARRAY RAM 5
06	PTER6 L	WRITE/READ AND ARRAY RAM 6
07	PTER7 L	WRITE/READ AND ARRAY RAM 7
10	PTER8 L	WRITE/READ AND ARRAY RAM 8
11	PTER9 L	WRITE/READ AND ARRAY RAM 9
12	PTER10 L	WRITE/READ AND ARRAY RAM 10
13	PTER11 L	WRITE/READ AND ARRAY RAM 11
14	PTER12 L	WRITE/READ AND ARRAY RAM 12
15	PTER13 L	WRITE/READ AND ARRAY RAM 13
16	PTER14 L	WRITE/READ AND ARRAY RAM 14
17	PTER15 L	WRITE/READ OR ARRAY RAM'S

STATE ANALYZER'S POINTER REGISTER AND CONTROL REGISTER 6 (163016)

PDAL BITS 3:0 - SIGNAL - DESCRIPTION

00	PTER0 L	WRITE/READ TRACE RAM (TRAM) ADDRESS REG
01	PTER1 L	WRITE TRAM 15:0 WITH TRDI DATA FROM

02	PTER2 L	TRAM BUS SELECTED. READ TRDI 15:0 DATA FROM TRAM BUS SELECTED WRITE TRAM 31:16 WITH TRDI DATA FROM TRAM BUS SELECTED.
03	PTER3 L	READ TRDI 31:16 DATA FROM TRAM BUS SELECTED WRITE TRAM 47:32 WITH TRDI DATA FROM TRAM BUS SELECTED.
04	PTER4 L	READ TRDI 47:32 DATA FROM TRAM BUS SELECTED WRITE TRAM 55:48 WITH TRDI DATA FROM TRAM BUS SELECTED.
05	PTER5 L	READ TRDI 59:48 DATA FROM TRAM BUS SELECTED. WRITE TRAM DATA IN BUFFER 15:0 FROM Q-BUS DATA BITS 15:0
06	PTER6 L	WRITE TRAM DATA IN BUFFER 31:16 FROM Q-BUS DATA BITS 15:0.
07	PTER7 L	WRITE TRAM DATA IN BUFFER 47:32 FROM Q-BUS DATA IN BITS 15:0.
10	PTER8 L	WRITE TRAM DATA IN BUFFER 59:48 FROM Q-BUS DATA IN BITS 15:0
11	PTER9 L	LOAD EVENT COUNTER REGISTER 0 AND EVENT COUNTER 0. CLEAR SBL56 FLIP-FLOP.
12	PTER10 L	LOAD EVENT COUNTER REGISTER 1 AND EVENT COUNTER 1. CLEAR SBL57 FLIP-FLOP.
13	PTER11 L	LOAD EVENT COUNTER REGISTER 2 AND EVENT COUNTER 2. CLEAR SBL58 FLIP-FLOP.
14	PTER12 L	LOAD EVENT COUNTER REGISTER 3 AND EVENT COUNTER 3. CLEAR SBL59 FLIP-FLOP.
15	PTER13 L	NOT USED
16	PTER14 L	NOT USED
17	PTER15 L	READ/WRITE 'OR ADDRESS REGISTER' (CDAL7=0) READ FOUT F/F'S ON OR ADDRESS BITS (CDAL7=1)

NOTE: THE TRACE RAM (TRAM) BUS SELECTED IS CONTROLLED BY CONTROL REGISTER 0 BITS CDAL3 AND CDAL2.

5.3 DEVICE INFORMATION FOR TARGET EMULATOR MODULE

CONTROL REGISTER 0 (163010) - GDAL REGISTER

15 GDAL15 BIT 15 = 1 READ DEVICE TYPE IN BITS 15-8. TARGET EMULATOR DEVICE TYPE EQUALS 0 (0000)

BIT 15 = 0 READ DEVICE NUMBER INTO BITS 11:8.

14 GDAL14 ALWAYS A 0 ON READ
13 GDAL13 ALWAYS A 0 ON READ
12 GDAL12 ALWAYS A 0 ON READ

BITS 11:8 ARE USED TO SELECT THE DEVICE NUMBER OF THE TARGET EMULATOR. THESE BITS MUST BE EQUAL TO THE SETTING OF SWITCHES DEV 3, DEV 2, DEV 1 AND DEV 0.

11 GDAL11 DEVICE NUMBER/TYPE
10 GDAL10 DEVICE NUMBER/TYPE
9 GDAL9 DEVICE NUMBER/TYPE
8 GDAL8 DEVICE NUMBER/TYPE

- 7 GDAL7 SINGLE STEP BREAK INDICATOR (READ ONLY)
- 6 GDAL6 TIMEOUT BREAK INDICATOR (READ ONLY)
- 5 GDAL5 MEMORY SIMULATOR BREAK INDICATOR (READ ONLY)
- 4 GDAL4 STATE ANALYZER BREAK INDICATOR (READ ONLY)
- 3 GDAL3 TARGET EMULATOR INTERRUPT ENABLE (R/W)
- 2 GDAL2 POINTER FOR EXTENDED REGISTER SELECT (R/W)
- 1 GDAL1 POINTER FOR EXTENDED REGISTER SELECT (R/W)
- 0 GDAL0 POINTER FOR EXTENDED REGISTER SELECT (R/W)

EXTENDED REGISTER SELECTED VIA GDAL BITS 2:0

GDAL2	GDAL1	GDAL0	REGISTER SELECTED VIA R/W TO CONTROL REGISTER 6
0	0	0	WRITE DIAGNOSTIC ADDRESS REGISTER READBACK OF ADDRESS BUS
0	0	1	WRITE NEW FORCE JUMP ADDRESS REGISTER READBACK OF FORCE JUMP ADDRESS READBACK REG
0	1	0	WRITE FDAL AND EOAI REGISTER READBACK OF FDAL/EOAI OR FDAL/CTL REG
0	1	1	READ/WRITE HDAL REGISTER
1	0	0	READ/WRITE MODE REGISTER
1	0	1	READBACK OF TARGET MODE REGISTER
1	1	0	READBACK OF EIDAL BUS
1	1	1	READBACK OF EODAL BUS

CONTROL REGISTER 2 (163012) - ADAL REGISTER

- 15 ADAL15 SELECT COLUMN AI FOR STATE ANALYZER (1)
- 14 ADAL14 SELECT ROW/COLUMN AI FOR STATE ANALYZER (1)
- 13 ADAL13 SELECT SERVICE AI FOR STATE ANALYZER (0)
- 12 ADAL12 ENABLE SERVICE FROM TARGET EMULATOR (1)
ENABLE SERVICE FROM THE TARGET (0)
- 11 ADAL11 ENABLE MODE FROM TARGET EMULATOR (1)
ENABLE MODE FROM THE TARGET (0)
- 10 ADAL10 DISABLE SERVICE TO THE TARGET (1)
ENABLE SERVICE TO THE TARGET (0)
- 9 ADAL9 MASTER SWITCH
- 8 ADAL8 ENABLE STATE ANALYZER CLOCKS (1)
ENABLE TIMEOUT BREAK (1)
DISABLE TIMEOUT BREAK (0)
- 7 ADAL7 ENABLE REFRESH TO STATE ANALYZER (1)
DISBALE REFRESH TO STATE ANALYZER (0)
- 6 ADAL6 SPARE
- 5 ADAL5 ENABLE SINGLE STEP BREAK (1)
DISABLE SINGLE STEP BREAK (0)
- 4 ADAL4 ENABLE PAUSE STATE TO RUN MODE (1)
ENABLE PAUSE STATE TO PAUSE MODE (0)
- 3 ADAL3 POWER UP FROM TARGET (1)
- 2 ADAL2 POWER UP FROM TARGET EMULATOR
- 1 ADAL1 SELECT TARGET EMULATOR CRYSTAL CLOCK (1)
SELECT CLOCK FROM THE STATE ANALYZER (0)
- 0 ADAL0 RESET BREAK LOGIC - ZEROES BREAK LATCH FLIP-FLOP, SINGLE
STEP BREAK FLIP-FLOP AND MEMORY SIMULATOR BREAK LATCH
FLIP-FLOP

CONTROL REGISTER 4 (163014) - VDAL REGISTER

15	VDAL15	TNFJ H - TAKE NEW FORCE JUMP ADDRESS F/F (READ)
14	VDAL14	EP8N H - 8 BIT ADDRESS HB F/F (READ)
13	VDAL13	EP8G H - 8 BIT ADDRESS LB F/F (READ)
12	VDAL12	EP8F H - 8 BIT INSTRUCTION HB F/F (READ)
11	VDAL11	EPFN H - 16 BIT ADDRESS F/F (READ)
10	VDAL10	EPSF H - PAUSE STATE SYNC F/F (READ)
9	VDAL9	PSMW H - PAUSE STATE WORKING F/F (READ)
8	VDAL8	OUTNEW H - GET NEW ADDRESS F/F (READ)
7	VDAL7	DIAGNOSTIC FETCT H (READ/WRITE)
6	VDAL6	MSDI H - DATA IN LOGIC LEVEL (READ)
5	VDAL5	BTS1 H -
4	VDAL4	EDEOC H - LOGIC LEVEL OF STATE ANALYZER CLOCK (READ)
3	VDAL3	READ H - LOGIC LEVEL OF REAT H (READ)
2	VDAL2	DIAGNOSTIC RESET OF THE TARGET EMULATOR MODULE AND CLOCKS THE TAI AND TDAL LATCHES (READ/WRITE)
1	VDAL1	SPARE (READ/WRITE)
0	VDAL0	ENABLE TAI AND TDAL READBACK FROM POD (READ/WRITE)

CONTROL REGISTER 6 (163016) - FDAL REGISTER (EOAI/CTL ON FDAL 15:8)

7	FDAL7	INTERRUPT VECTOR
6	FDAL6	INTERRUPT VECTOR
5	FDAL5	INTERRUPT VECTOR
4	FDAL4	INTERRUPT VECTOR
3	FDAL3	INTERRUPT VECTOR
2	FDAL2	INTERRUPT VECTOR
1	FDAL1	SPARE
0	FDAL0	SELECT EOAI REG TO BE READBACK ON FDAL BITS 15:8 (1) SELECT CTL REG TO BE READBACK ON FDAL BITS 15:8 (0)

CONTROL REGISTER 6 (163016) - HDAL REGISTER - DIAGNOSTIC CONTROL BITS

15	HDAL15	DIAGNOSTIC CONTROL OF PPI L WHEN HDAL2 EQUALS A ONE
14	HDAL14	DIAGNOSTIC CONTROL OF EIDAL17 H WHEN HDAL2 EQUALS A ONE
13	HDAL13	DIAGNOSTIC CONTROL OF PCAS H WHEN HDAL2 EQUALS A ONE
12	HDAL12	DIAGNOSTIC CONTROL OF PRAS H WHEN HDAL2 EQUALS A ONE
11	HDAL11	DIAGNOSTIC CONTROL OF EIDAL16 H WHEN HDAL2 EQUALS A ONE
10	HDAL10	SPARE
9	HDAL9	ENABLE DIAGNOSTIC ADDRESS REGISTER TO ADDRESS BUS
8	HDAL8	DIAGNOSTIC CONTROL OF CREADY L WHEN HDAL2 EQUALS A ONE
7	HDAL7	DIAGNOSTIC CONTROL OF PBCLR H WHEN HDAL2 EQUALS A ONE
6	HDAL6	DIAGNOSTIC CONTROL OF PSEL1 L WHEN HDAL2 EQUALS A ONE
5	HDAL5	DIAGNOSTIC CONTROL OF PSEL0 L WHEN HDAL2 EQUALS A ONE
4	HDAL4	DIAGNOSTIC CONTROL OF PR/WHB L WHEN HDAL2 EQUALS A ONE
3	HDAL3	DIAGNOSTIC CONTROL OF PR/WLB L WHEN HDAL2 EQUALS A ONE
2	HDAL2	ENABLES PROGRAM TO GENERATE T-11 SIGNALS LISTED IN HDAL (1) ENABLES T-11 TO GENERATE T-11 SIGNALS LISTED IN HDAL (0)
1	HDAL1	SPARE
0	HDAL0	DIAGNOSTIC CONTROL OF MSDI H WHEN HDAL2 EQUALS A ONE

CONTROL REGISTER 6 (163016) - MODE REGISTER

15	MR15	T-11 START/RESTART ADDRESS SELECT
14	MR14	T-11 START/RESTART ADDRESS SELECT

13	MR13	T-11 START/RESTART ADDRESS SELECT
12	MR12	T-11 USER MODE (1)
		T-11 TESTER MODE (0)
11	MR11	SELECT 8 BIT BUS (1)
		SELECT 16 BIT BUS (0)
10	MR10	T-11 DYNAMIC MODE ONLY - SELECTS 4K/16K (1)
		T-11 DYNAMIC MODE ONLY - SELECTS 64K (0)
9	MR9	T-11 STATIC MEMORY SELECT (1)
		T-11 DYNAMIC MEMORY SELECT (0)
8	MR8	T-11 DELAYED READ/WRITE SELECT (1)
		T-11 NROMAL READ/WRITE SELECT (0)
7	MR7	NOT DEFINED
6	MR6	NOT DEFINED
5	MR5	NOT DEFINED
4	MR4	NOT DEFINED
3	MR3	NOT DEFINED
2	MR2	NOT DEFINED
1	MR1	T-11 STANDARD MICROCYCLE (1)
		T-11 LONG MICROCYCLE (0)
0	MR0	T-11 PROCESSOR CLOCK (1)
		T-11 CONSTANT CLOCK (0)

6.0 TEST SUMMARIES

TEST 1:

~~THIS TEST WILL BE EXECUTED AS THE FIRST TEST IN THE PROGRAM AND AT THE BEGINNING OF EACH TEST IN THE PROGRAM.~~ THE PURPOSE OF THIS TEST IS TO INITIALIZE THE CDS-11 MODULES (MEMORY SIMULATOR, STATE ANALYZER AND TARGET EMULATOR) TO A KNOWN STATE. THE TEST SEQUENCE IS DESCRIBED BELOW.

CDS-11 MEMORY SIMULATOR MODULE INITIALIZATION SEQUENCE:

1. LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVICE NUMBER TO SELECT THE MEMORY SIMULATOR MODULE.
2. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND THE BIT TO SET THE SIGNAL 'RST H' TO THE HIGH STATE. WHEN THE SIGNAL 'RST H' IS SET HIGH, THE 'RDV' AND 'WRV' FLIP-FLOPS WILL BE PRESET TO A ONE THUS CAUSING THE SIGNALS 'RDV H' AND 'WRV H' TO BE ASSERTED LOW. THE SIGNALS 'RDV H' AND 'WRV H' SHOULD BE READ AS ZEROES WHEN CONTROL REGISTER 0 IS READ.
3. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND BIT 15 SET TO A ONE. THE BIT WHICH SET THE SIGNAL 'RST H' TO THE HIGH STATE WILL BE CLEARED THUS SETTING THE SIGNAL LOW. WHEN BIT 15 IS SET TO A ONE, THE DEVICE TYPE WILL BE READ BACK ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE NUMBER.
4. CLEAR BIT 15 IN CONTROL REGISTER 0 AND THEN READ AND CHECK CONTROL REGISTER 0 FOR THE DEVICE NUMBER.
5. LOAD, READ AND CHECK CONTROL REGISTER 2'S READ/WRITE BITS 3:0 WITH A DATA PATTERN OF ZEROES. THESE BITS WILL SET THE SIGNALS MSEL1 H, MSEL0 H, MSAD17 H, AND MSAD16 H TO THE LOW STATE. THE READ ONLY SIGNALS MSBRK H, WREN H, AND ESR H WILL BE IGNORED AT THIS POINT IN TIME.
6. LOAD, READ AND CHECK CONTROL REGISTER 4'S READ/WRITE BITS 15:0 WITH A DATA PATTERN OF ALL ZEROES. THESE BITS WILL SET THE SIGNALS MSAD 15:0 H TO THE LOW STATE.

CDS-11 STATE ANALYZER MODULE INITIALIZATION

1. LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVIE NUMBER TO SELECT THE STATE ANALYZER MODULE.
2. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND THE BIT TO SET THE SIGNAL "CDALO H" TO THE HIGH STATE. WHEN THE SIGNAL "CDALO H" IS SET HIGH, THE TRACE RAM ADDRESS REGISTER, THE TRACING AND SBL FLIP-FLOPS WILL BE CLEARED AND THE EVENT COUNTERS WILL BE LOADED WITH DATA FROM THE EVENT COUNTER REGISTERS.
3. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND THE BIT TO SET THE SIGNAL CDAL15 H TO A ONE. THE BIT WHICH SET "CDALO H" TO THE HIGH STATE WILL BE CLEARED THUS SETTING THE SIGNAL "CDALO H" TO THE LOW STATE. WHEN "CDAL15 H" IS SET TO A ONE, THE DEVICE TYPE WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE NUMBER.
4. CLEAR THE BIT WHICH SET "CDAL15 H" TO THE HIGH STATE AND THEN READ AND CHECK CONTROL REGISTER 0 FOR THE DEVICE NUMBER.
5. LOAD, READ AND CHECK CONTROL REGISTER 4'S PDAL REGISTER WITH A DATA PATTERN OF ALL ZEROES. THIS WILL CAUSE THE SIGNALS "PDAL 7:0 H" TO BE ASSERTED LOW. THIS WILL ALSO CAUSE THE SIGNAL PTERO L TO BE ASSERTED LOW IN THE POINTER REGISTER.

CDS-11 TARGET EMULATOR MODULE INITIALIZATION

1. LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVICE NUMBER TO SELECT THE TARGET EMULATOR MODULE.
2. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND ALL READ/WRITE BITS SET TO A ZERO. THE READ ONLY SIGNALS SSBK H, TOBRK H, AND MEMBRK H WILL BE IGNORED DURING THE READING OF CONTROL REGISTER 0.
3. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND THE BIT TO SET THE SIGNAL "GDAL15 H" TO THE HIGH STATE. WHEN THE SIGNAL "GDAL15 H" IS SET HIGH (1), THE DEVICE TYPE WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE NUMBER.
4. SET THE SIGNAL "GDAL15 H" TO THE LOW STATE BY CLEARING THE BIT IN CONTROL REGISTER 0. ALSO SET THE READ/WRITE BITS "GDAL1 H" AND "GDALO H" TO A ONE. ALL OTHER READ/WRITE BITS WILL BE LOADED WITH ZEROES. WHEN "GDAL2 H" IS SET TO A ZERO AND THE SIGNALS "GDAL1 H" AND "GDALO H" ARE SET TO ONES, THE HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
5. LOAD, READ AND CHECK HDAL REGISTER WITH A DATA PATTERN OF 4 WHICH WILL CAUSE THE SIGNAL "HDAL2 H" TO BE ASSERTED HIGH (1) AND ALL OTHER HDAL BITS TO BE ASSERTED LOW (0). WHEN "HDAL2 H" IS ASSERTED HIGH, THE PROGRAM CAN GENERATE THE T-11 TIMING AND CONTROL SIGNALS.
6. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND WITH "GDAL2 H" SET TO A ONE AND GDAL BITS 1 AND 0 SET TO A ZERO. THIS WILL CAUSE THE MODE REGISTER TO BE SELECTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
7. LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES. MODE REGISTER BIT MR11 H ON A ZERO WILL SELECT 16 BIT ADDRESS MODE.

8. LOAD, READ AND CHECK CONTROL REGISTER 2'S ADAL REGISTER WITH ADALO H SET TO A ONE AND THEN A ZERO. SETTING AND CLEARING THE SIGNAL ADALO H WILL CAUSE A PULSE TO BE ISSUED ON THE SIGNAL 'BRKRES L'. ALL OTHER ADAL REGISTER BITS WILL BE LOADED AND CHECKED WITH ZERES. PULSING THE SIGNAL 'BRKRES L' WILL CLEAR THE SINGLE STEP SYNC FLIP-FLOP, THE BREAK INTERRUPT LATCH FLIP-FLOP, THE MEMORY SIMULATOR BREAK LATCH FLIP-FLOP (MEMBRK) AND THE TIMEOUT BREAK ONE SHOT WILL BE RESET.
9. READ AND CHECK CONTROL REGISTER 0 TO CHECK THAT ALL THE BREAK SIGNALS ARE READ AS ZEROES. THESE SIGNALS ARE SSBK H, TOBRK H, MEMBRK H AND EDBRK H.
10. LOAD, READ AND CHECK CONTROL REGISTER 4'S VDAL REGISTER WITH VDAL2 H SET TO A ONE AND THEN A ZERO. ALL OTHER VDAL REGISTER READ/WRITE BITS WILL BE LOADED AND CHECKED FOR ZEROES. SETTING AND CLEARING THE SIGNAL VDAL2 H WILL CAUSE A PULSE TO BE ISSUED ON THE SIGNAL INV D L. A PULSE ON THE SIGNAL INV D L WILL CAUSE ALL THE FLIP-FLOP'S AND SOME REGISTERS NOT CLEARED BY THE SIGNAL 'BRKRES L' PREVIOUSLY TO BE INITIALIZED TO SOME PREDEFINED STATE. THE READ ONLY BITS WILL BE CHECKED TO BE ZERO AS A RESULT OF THE SIGNAL 'INV D L' BEING PULSED.

TEST 2:

THIS TEST WILL CHECK THAT THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER AND ADDRESS BITS 17:16 CAN BE ENABLED TO THE SYSTEM ADDRESS BUS AND THAT THE ADDRESS BUS BITS 17:0 CAN BE CLOCKED INTO THE MEMORY SIMULATOR AND STATE ANALYZER SYSTEM BUS LATCHES FOR THESE BITS DURING A NORMAL T-11 TIMING CYCLE. A NORMAL T-11 TIMING CYCLE OCCURS WHEN RAS, CAS AND PI ARE SET TO THEIR ASSERTED STATE IN THE ORDER LISTED AND THEN DEASSERTED IN THE FOLLOWING ORDER: CAS, PI AND RAS. THE ADDRESS BUS DATA PATTERNS USED DURING THIS TEST ARE AS FOLLOWS: 577777, 252525, 725252 AND 000000. TARGET EMULATOR HDAL REGISTER BITS 14 AND 11 CONTROL THE STATE OF ADDRESS BITS 17 AND 16.

WHEN PRAS H IS SET HIGH, THE SIGNAL 'ADVAL H' WILL BE SET HIGH THUS CLOCKING SYSTEM ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES. WHEN XRAS H IS SET HIGH, THE SIGNALS 'EDCK0 H' AND 'EDCK1 H' WILL BE SET HIGH THUS CLOCKING SYSTEM ADDRESS BUS BITS 15:0 INTO THE STATE ANALYZERS SYSTEM ADDRESS BUS LATCHES FOR THESE BITS. WHEN XPI L IS SET LOW, THE SIGNAL 'EDCK4 H' WILL BE SET HIGH THUS CLOCKING THE SYSTEM BUS SIGNALS XSEL1 H, EDSEL0 H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS. ALL THE SIGNALS MENTIONED ABOVE ARE GENERATED ON THE TARGET EMULATOR MODULE. THE PROGRAM WILL CHECK THAT SYSTEM ADDRESS BUS BITS 17:0 WERE CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES BY ENABLING THE LATCHES TO MSAD BITS 17:0 VIA THE SIGNAL 'CTS L' AND THEN READING AND CHECKING THESE BITS VIA CONTROL REGISTER 2 AND 4. THE PROGRAM WILL CHECK THAT SYSTEM ADDRESS BUS BITS 17:0 AND THE SIGNALS XSEL1 H, EDSEL0 H, AND OBTS BITS 3:0 WERE CLOCKED INTO THE STATE ANALYZER SYSTEM BUS LATCHES FOR THESE BITS. THE STATE ANALYZERS SYSTEM BUS LATCHES ARE ENABLED TO STATE ANALYZERS TRDI BUS BY SETTING THE SIGNAL 'TRSL2 L' TO THE LOW STATE. THE PROGRAM WILL THEN READ AND CHECK TRDI BUS BITS 15:0 AND 39:32 FOR THE SYSTEM BUS DATA.

TEST 3:

THIS TEST WILL CHECK THAT DATA, WRITTEN INTO LOCATIONS OF THE MEMORY SIMULATOR RAM, CAN BE ENABLED TO THE TARGET EMULATOR MODULE AND CLOCKED INTO THE STATE ANALYZER MODULE VIA THE SYSTEM DATA BUS WHEN A 'READ' OPERATION IS BEING EXECUTED FROM THE TARGET EMULATOR MODULE IN 16 BIT MODE. ADDRESSES 0, 20000, 40000 AND 60000, WHICH ARE THE FIRST LOCATIONS OF EACH 4K BANK OF MEMORY SIMULATOR RAM, WILL BE WRITTEN WITH A DATA PATTERN OF 125252, 052525, 177777, AND 000000 RESPECTIVELY. LOCATIONS OF THE MEMORY SIMULATOR RAM WILL BE ADDRESSED VIA THE DIAGNOSTIC ADDRESS REGISTER ON THE TARGET EMULATOR MODULE DURING A NORMAL T-11 TIMING CYCLE. A NORMAL T-11 TIMING CYCLE OCCURS WHEN RAS, CAS AND PI ARE ASSERTED IN THE ORDER LISTED AND THEN DE-ASSERTED IN THE FOLLOWING ORDER CAS, PI AND RAS. THE PROGRAM WILL CHECK THAT THE SYSTEM ADDRESS BUS WAS CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES AND THE STATE ANALYZERS SYSTEM BUS LATCHES WHEN THE SIGNALS XRAS H AND PRAS H ARE ASSERTED HIGH ON THE TARGET EMULATOR MODULE. WHEN THE TARGET EMULATOR SIGNALS XR/WLB H, XR/WHB H, XRAS H, AND XCAS H ARE ASSERTED HIGH, THE TARGET EMULATOR SIGNALS 'READ H' AND 'MSDI H' WILL BE ASSERTED HIGH. THE SIGNAL 'READ H' BEING ASSERTED WILL ENABLE MEMORY SIMULATOR RAM DATA ADDRESSED BY THE TARGET EMULATOR MODULE ONTO THE SYSTEM DATA BUS. THE SYSTEM DATA BUS WILL BE ENABLED TO THE TARGET EMULATOR'S EODAL BUS VIA THE SIGNAL 'MSDI H' AND THE EODAL BUS WILL BE ENABLED TO THE TARGET EMULATOR'S EIDAL BUS VIA THE SIGNALS COHB L AND COLB L. THE SIGNALS COHB L AND COLB L ARE ASSERTED LOW AS A RESULT OF THE SIGNALS ETR L, PR/WLB H, PR/WHB H, PPI H, DMG L, AND MR11 L BEING ASSERTED HIGH. THE PROGRAM WILL READ AND CHECK THE TARGET EMULATOR'S EODAL AND EIDAL BUS TO CONTAIN THE EXPECTED MEMORY SIMULATOR RAM DATA. WHEN THE SIGNAL XCAS L IS RETURNED TO ITS DE-ASSERTED STATE, THE SIGNALS 'EDCK2 H' AND 'EDCK3 H' WILL GO FROM A LOW TO A HIGH STATE THUS CLOCKING THE SYSTEM DATA BUS INTO THE STATE ANALYZER SYSTEM DATA BUS LATCHES. THE PROGRAM WILL CHECK THAT THE SYSTEM DATA BUS WAS CLOCKED INTO THE STATE ANALYZER'S SYSTEM DATA BUS LATCHES BY ENABLING THE LATCHES TO THE STATE ANALYZER'S TRDI BUS VIA THE SIGNAL TRSL2 L AND THEN READING TRDI BUS BITS 31:16 TO CONTAIN THE EXPECTED MEMORY SIMULATOR RAM DATA. THE PROGRAM WILL ALSO CHECK THAT THE STATE ANALYZER'S TRACE RAM ADDRESS REGISTER WAS INCREMENTED BY ONE VIA THE SIGNAL 'CTR L' WHEN THE TARGET EMULATOR SIGNAL 'EDEOC H' WAS SET HIGH.

TEST 4:

THIS TEST WILL CHECK THAT DATA WRITTEN INTO ADDRESS 0 AND 2 OF THE MEMORY SIMULATOR RAM CAN BE ENABLED TO THE TARGET EMULATOR MODULE VIA THE LOW BYTE OF THE SYSTEM DATA BUS WHEN A 'READ' OPERATION IS BEING EXECUTED FROM THE TARGET EMULATOR MODULE IN 8 BIT MODE. THE TARGET EMULATOR MODULE WILL BE SETUP TO 8 BIT MODE AND THE MEMORY SIMULATOR MODULE WILL BE SETUP TO 8 BIT MODE AFTER THE DATA HAS BEEN WRITTEN INTO THE MEMORY SIMULATOR RAM AND CHECKED. ADDRESS 0 AND 2 OF THE MEMORY SIMULATOR RAM WILL BE WRITTEN WITH A DATA PATTERN OF 125125 AND 052652 RESPECTIVELY. ADDRESSES 0, 1, 2 AND 3 OF THE MEMORY SIMULATOR RAM WILL BE ADDRESSED VIA THE TARGET EMULATORS DIAGNOSTIC ADDRESS REGISTER WHEN A NORMAL T-11 TIMING CYCLE OCCURS. A NORMAL T-11 TIMING CYCLE OCCURS WHEN RAS, CAS AND PI ARE ASSERTED IN THE ORDER GIVEN AND THEN DE-ASSERTED IN THE FOLLOWING ORDER CAS, PI AND THEN RAS. THE PROGRAM WILL CHECK THAT THE SYSTEM ADDRESS BUS WAS CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS BUS LATCHES WHEN THE SIGNAL PRAS H WAS ASSERTED HIGH ON THE TARGET EMULATOR MODULE. WHEN THE TARGET EMULATOR SIGNALS XR/WLB H, XRAS H, XCAS H AND MR11 H ARE ASSERTED HIGH, THE TARGET EMULATOR SIGNALS

'READ H' AND 'MSDI H' WILL BE ASSERTED HIGH. THE SIGNAL 'READ H' BEING ASSERTED WILL ENABLE THE LOW BYTE OF MEMORY SIMULATOR RAM DATA TO THE LOW BYTE OF THE SYSTEM DATA BUS IF THE ADDRESS WAS EVEN, OR THE HIGH BYTE OF THE MEMORY SIMULATOR RAM DATA WILL BE ENABLED TO THE LOW BYTE OF THE SYSTEM DATA BUS IF THE ADDRESS WAS ODD. THE DATA ENABLED TO THE LOW BYTE OF THE SYSTEM DATA BUS WILL BE 125, 252, 252 AND 125 FOR ADDRESSES 0, 1, 2 AND 3 RESPECTIVELY. THE SYSTEM DATA BUS WILL BE ENABLED TO THE LOW BYTE OF THE TARGET EMULATOR'S EODAL BUS VIA THE SIGNAL 'MSDI H' AND THE LOW BYTE OF THE EODAL BUS WILL BE ENABLED TO THE LOW BYTE OF THE TARGET EMULATOR'S EIDAL BUS VIA THE SIGNAL 'COLB L'. THE SIGNAL 'COLB L' WILL BE ASSERTED LOW AS A RESULT OF THE SIGNALS ETR L, PR/WLB H, PPI H AND DMG L BEING ASSERTED HIGH. THE PROGRAM WILL READ AND CHECK THE TARGET EMULATORS EODAL AND EIDAL BUSES TO CONTAIN THE EXPECTED BYTE OF MEMORY SIMULATOR RAM DATA.

TEST 5:

THIS TEST WILL CHECK THAT DATA FROM THE MEMORY SIMULATOR RAM CAN BE ENABLED TO THE TARGET EMULATOR'S TDAL BUS AND CLOCKED INTO THE TDAL DIAGNOSTIC LATCHES WHEN A 'READ' OPERATION IS BEING EXECUTED FROM THE TARGET EMULATOR MODULE. THE TEST WILL CHECK THAT THE TDAL DIAGNOSTIC LATCHES CAN BE ENABLED TO THE SYSTEM DATA BUS AND THAT THE SYSTEM DATA BUS CAN BE WRITTEN BACK INTO THE MEMORY SIMULATOR RAM LOCATION WHEN A 'WRITE' OPERATION IS BEING EXECUTED FROM THE TARGET EMULATOR MODULE. THE TEST WILL INITIALLY LOAD AND CHECK MEMORY SIMULATOR RAM LOCATIONS 000000, 020000, 040000 AND 060000 WITH DATA PATTERNS 125252, 146314, 000377 AND 000000 RESPECTIVELY. ONCE EACH LOCATION HAS BEEN WRITTEN AND CHECKED, THE PROGRAM WILL ISSUE A 'READ' OPERATION FROM THE TARGET EMULATOR MODULE TO ONE OF THE MEMORY SIMULATOR RAM LOCATIONS AND CHECK THAT THE DATA IS PRESENT ON THE TARGET EMULATOR'S EODAL AND EIDAL BUSES. MEMORY SIMULATOR RAM DATA WILL ALSO BE ENABLED TO THE TARGET EMULATOR'S TDAL BUS. TO CAPTURE THIS DATA, THE PROGRAM MUST SET AND CLEAR THE SIGNAL 'VDAL2 H' TO CLOCK THE TDAL BUS DATA INTO THE TDAL DIAGNOSTIC LATCHES. ONCE MEMORY SIMULATOR RAM DATA HAS BEEN CLOCKED INTO THE TDAL DIAGNOSTIC LATCHES, THE PROGRAM WILL WRITE THE ONE'S COMPLEMENT OF THE INITIAL MEMORY SIMULATOR RAM DATA BACK INTO THE LOCATION ADDRESSED AND THEN CHECK THAT THE LOCATION CONTAINS THE ONE'S COMPLEMENT OF THE INITIAL DATA. THE PROGRAM WILL NOW ENABLE THE TDAL DIAGNOSTIC LATCHES, WHICH CONTAINS THE INITIAL MEMORY SIMULATOR RAM DATA, TO THE SYSTEM DATA BUS AND THEN WRITE THIS DATA VIA A 'WRITE' OPERATION FROM THE TARGET EMULATOR MODULE BACK INTO THE MEMORY SIMULATOR RAM LOCATION INITIALLY READ. THE PROGRAM WILL NOW READ AND CHECK THE MEMORY SIMULATOR RAM LOCATION TO CONTAIN THE INITIAL DATA.

TEST 6:

THIS TEST WILL READ DATA FROM THE MEMORY SIMULATOR RAM IN 16 BIT MODE AND STORE THE DATA READ IN THE TARGET EMULATOR'S TDAL DIAGNOSTIC LATCHES. ONCE THE DATA HAS BEEN STORED IN THE TDAL DIAGNOSTIC LATCHES, THE PROGRAM WILL CHANGE THE DATA STORED IN THE MEMORY SIMULATOR RAM LOCATION TO ALL ZEROES. THE PROGRAM WILL NOW SET THE MEMORY SIMULATOR MODULE TO 8 BIT MODE; LOAD THE EVEN ADDRESS OF THE MEMORY SIMULATOR RAM LOCATION INTO THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER; ENABLE THE TDAL DIAGNOSTIC LATCHES TO THE SYSTEM DATA BUS; AND THEN PERFORM A NORMAL T-11 TIMING CYCLE BY PULSING THE SIGNALS RAS, CAS AND PI. THE ABOVE OPERATION WILL CAUSE THE LOW BYTE OF THE SYSTEM BUS DATA TO BE WRITTEN INTO THE LOW

BYTE OF THE MEMORY SIMULATOR RAM LOCATION. THE PROGRAM WILL CHECK THAT THE CORRECT ADDRESS WAS CLOCKED INTO THE MEMORY SIMULATOR'S SYSTEM BUS ADDRESS LATCHES AND THAT THE LOW BYTE OF THE INITIAL DATA WAS WRITTEN INTO THE MEMORY SIMULATOR RAM LOCATION. THE HIGH BYTE OF THE LOCATION SHOULD REMAIN ALL ZEROES DURING THIS WRITE OPERATION. THE PROGRAM WILL NOW RESET THE MEMORY SIMULATOR MODULE TO 8 BIT MODE; LOAD THE ODD ADDRESS OF THE MEMORY SIMULATOR LOCATION INTO THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER; AND THEN PERFORM A NORMAL T-11 TIMING CYCLE. THE ABOVE OPERATION WILL CAUSE THE LOW BYTE OF THE SYSTEM BUS DATA, WHICH CONTAINS THE DATA OF THE LOW BYTE OF THE TDAL DIAGNOSTIC LATCH, TO BE WRITTEN INTO THE HIGH BYTE OF THE MEMORY SIMULATOR RAM LOCATION. THE PROGRAM WILL CHECK THAT THE CORRECT ADDRESS WAS CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES AND THAT THE LOW BYTE OF THE INITIAL DATA WAS WRITTEN INTO THE HIGH BYTE OF THE MEMORY SIMULATOR RAM LOCATION. THE LOW BYTE OF THE LOCATION SHOULD REMAIN UNCHANGED DURING THIS WRITE OPERATION. THE ABOVE SEQUENCE WILL BE PERFORMED FOR ADDRESSES 0, 20000, 40000 AND 60000. THESE ADDRESSES ARE THE FIRST ADDRESSES OF EACH 4K BANK OF MEMORY SIMULATOR RAM. THE DATA LOADED INTO THE ADDRESSES ARE 052652, 146063, 000377 AND 125125 RESPECTIVELY. AFTER THE DATA HAS BEEN WRITTEN BACK INTO THE MEMORY SIMULATOR RAM IN 8 BIT MODE, THE DATA IN THESE ADDRESSES SHOULD BE 125252, 031463, 177777, AND 052525 RESPECTIVELY. THE LAST PORTION OF THIS TEST WILL READ AND CHECK EACH ADDRESS TO CONTAIN THE CORRECT DATA. THIS IS DONE TO CHECK THE RAM WRITE AND SELECT LOGIC.

TEST 7:

THIS TEST WILL CHECK THAT TARGET EMULATOR SIGNALS XSEL1 H, EDSELO H, ADDR17 H, ADDR16 H, BTS3 H, BTS2 H, BTS1 H AND BTS0 H CAN BE ENABLED TO THE SYSTEM BUS AS SIGNALS CTL 11:8 H AND OBTS 3:0 H RESPECTIVELY, AND THAT THESE SIGNALS CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES FOR THESE BITS VIA THE TARGET EMULATOR'S SYSTEM BUS CLOCKING SIGNAL 'ENCK4 H'. THE PROGRAM WILL CHECK THAT THESE BITS ARE CLOCKED INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES BY READING THESE LATCHES ON THE STATE ANALYZER'S TRDI BUS BITS 39:32. THE TARGET EMULATOR SIGNALS 'ADDR17 H' AND 'ADDR16 H' HAVE BEEN CHECKED IN PREVIOUS TEST, THEREFORE, THESE SIGNALS WILL ONLY BE CHECKED FOR ZEROES IN THIS TEST. THE PROGRAM WILL SET THE SIGNALS XSEL1 H, EDSELO H AND BTS BITS 3:0 H TO ONES AND ZEROES BY MANIPULATING THE ASSOCIATED LOGIC. THE TEST WILL THEN CLOCK THE CORRESPONDING SYSTEM BUS SIGNALS INTO THE STATE ANALYZER SYSTEM BUS LATCHES AND CHECK THAT THE SYSTEM BUS LATCHES CONTAIN THE CORRECT DATA PATTERN. THE PROGRAM WILL ALSO CHECK THAT THE TARGET EMULATOR SYSTEM BUS CLOCKING SIGNAL 'ENCK4 H' CAN BE GENERATED IN DIFFERENT WAYS.

TEST 8:

THIS TEST WILL CHECK THAT DATA LOADED INTO THE TARGET EMULATOR'S EOAI REGISTER CAN BE ENABLED TO THE CTL BUS, WHICH IS ON THE SYSTEM BUS, AND THAT THE CTL BUS CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM BUS CTL 7:0 LATCHES VIA THE TARGET EMULATOR'S CLOCKING SIGNAL 'ENCK5 H'. THE TEST WILL ALSO CHECK THAT THE EOAI REGISTER CAN BE CLOCKED INTO THE TARGET EMULATOR'S CTL REGISTER WHEN THE SIGNAL 'XCAS L' IS RETURNED TO THE DE-ASSERTED STATE AFTER HAVING BEEN ASSERTED. TO CHECK THAT THE EOAI REGISTER WAS CLOCKED INTO THE CTL REGISTER, THE PROGRAM WILL READ THE TARGET EMULATOR'S CTL REGISTER AND CHECK THE DATA TO BE THE ONE'S COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER. THE SYSTEM BUS CLOCKING SIGNAL 'ENCK5 H' IS GENERATED ON THE TARGET EMULATOR MODULE AS

THE SIGNAL "CKAI H". THE PROGRAM WILL CAUSE THE SIGNAL "CKAI H" TO BE PULSED IN DIFFERENT WAYS DURING THIS TEST. TO CHECK THAT THE EOAI REGISTER DATA CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM BUS CTL LATCHES AND THAT A PULSE CAN BE GENERATED ON THE SIGNAL "ENCK5 H", THE PROGRAM WILL READ THE CTL 7:0 SYSTEM BUS LATCHES ON THE STATE ANALYZER'S TRDI BUS BITS 47:40 AND CHECK THAT THE DATA READ IS THE ONE'S COMPLEMENT OF THE DATA LOADED INTO THE TARGET EMULATOR'S EOAI REGISTER. THE TEST WILL ALSO CHECK THAT THE TARGET EMULATOR SIGNALS XSEL1 H, EDSELO H, ADDR17 H, ADDR16 H AND BTS BITS 3:0 H CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES BY READING THESE BITS ON STATE ANALYZER'S TRDI BUS BITS 39:32. THE TEST WILL LOAD THE EOAI REGISTER WITH THE FOLLOWING DATA PATTERNS 377, 000, 252, 125 AND 314.

TEST 9:

THIS TEST WILL CHECK THAT THE MEMORY SIMULATOR "RDV" FLIP-FLOP CAN BE CLEARED WHEN A READ OPERATION IS EXECUTED FROM THE TARGET EMULATOR MODULE TO AN ADDRESS WHICH IS MAPPED IN THE MEMROY SIMULATOR'S MAP PROTECTION RAM TO INHIBIT READS AND WRITES. THE "RDV" FLIP-FLOP WILL BE CLOCKED TO A ZERO AS A RESULT OF THE SIGNAL "RDE H" BEING ASSERTED LOW AND A PULSE ON THE SIGNAL "RDS H". THE SIGNAL "RDS H" WILL BE PULSED WHEN THE MEMORY SIMULATOR SIGNAL "CTS H" IS ASSERTED HIGH AND A PULSE IS ISSUED ON THE TARGET EMULATOR SIGNAL "READ H". A PULSE WILL OCCUR ON THE SIGNAL "READ H" WHEN A T-11 READ OPERATION IS BEING EXECUTED BY THE TARGET EMULATOR MODULE. THE PROGRAM WILL CHECK THAT THE MEMORY SIMULATOR SIGNAL "MSBRK H" IS ASSERTED HIGH AS A RESULT OF THE "RDV" FLIP-FLOP BEING CLEARED. THE PROGRAM WILL CHECK THE TARGET EMULATOR MODULES "MEMBRK" FLIP-FLOP TO BE CLEARED AND THEN CAUSE A PULSE TO BE ISSUED ON TARGET EMULATOR SIGNAL "XRAS H". THE PROGRAM WILL NOW CHECK THE "MEMBRK" FLIP-FLOP TO BE SET TO A ONE AS A RESULT OF A PULSE ON "XRAS H" AND THE MEMORY SIMULATOR'S SYSTEM BUS SIGNAL "MSBRK H" BEING ASSERTED HIGH. THE PROGRAM WILL NOW PRESET THE "RDV" FLIP-FLOP BY PULSING MEMORY SIMULATOR SIGNAL "RST H". THE PROGRAM WILL CHECK THAT THE "RDV" FLIP-FLOP PRESET AND THAT THE SIGNAL "MSBRK H" WENT TO THE LOW STATE AS A RESULT OF THE "RDV" FLIP-FLOP BEING PRESET. THE PROGRAM WILL NOW PULSE THE TARGET EMULATOR SIGNAL "XRAS H" AGAIN AND CHECK THAT THE "MEMBRK" FLIP-FLOP IS STILL SET TO A ONE AS A RESULT OF THE FLIP-FLOP BEING LATCHED ONCE IT HAS BEEN SET. THE PROGRAM WILL NOW PULSE TARGET EMULATOR SIGNAL "BRKRES L" AND CHECK THAT THE "MEMBRK" FLIP-FLOP WAS CLEARED. THE PROGRAM WILL NOW SET THE TARGET EMULATOR SIGNAL "FETCT H" TO THE HIGH STATE AND PULSE THE SIGNAL "XRAS H". A PULSE ON "XRAS H" WILL CAUSE THE EDFET FLIP-FLOP TO BE SET AND THE ADDRESS TO BE CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES. THE ADDRESS WILL ADDRESS MEMORY ON THE MEMORY SIMULATOR MODULE WHICH IS MAPPED TO INHIBIT READS AND WRITES, THEREFORE, THE SYSTEM BUS SIGNAL "RDE L" WILL BE ASSERTED HIGH. AS A RESULT OF "RDE L", "EDFET H", "PSMW L" BEING ASSERTED HIGH AND A PULSE ON "XRASD H", THE "MEMBRK" FLIP-FLOP WILL BE DIRECT SET TO A ONE. THE SIGNAL "MEMBRK H" ASSERTED HIGH WILL CAUSE THE SIGNAL "SOP H" TO BE ASSERTED HIGH. WHEN "SOP H" AND "EDFET H" ARE ASSERTED HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE. THE PROGRAM WILL CHECK THAT THE "MEMBRK" AND "PSMW" FLIP-FLOPS ARE SET TO ONES. THE PROGRAM WILL NOW SET THE TARGET EMULATOR'S INTERRUPT ENBALE BIT AND LOWER THE CPU PRIORITY LEVEL TO ALLOW INTERRUPTS. THE BREAK INTERRUPT FLIP-FLOP WAS SET TO A ONE PREVIOUSLY AS A RESULT OF "MEMBRK H" BEING ASSERTED HIGH AND A PULSE BEING ISSUED ON "XRAS L". THE PROGRAM WILL NOW CHECK THAT AN INTERRUPT OCCURED AS A RESULT OF THE

INTERRUPT ENABLE BIT BEING SET, THE BREAK INTERRUPT FLIP-FLOP BEING SET, AND THE CPU PRIORITY LEVEL BEING LOWERED TO ALLOW INTERRUPTS. THE PROGRAM WILL ISSUE A PULSE ON 'BRKRES L' AND CHECK THAT THE 'MEMBRK' FLIP-FLOP WAS CLEARED BY THE PULSE ON 'BRKRES L'.

TEST 10:

THIS TEST WILL CHECK THAT THE MEMORY SIMULATOR 'WRV' FLIP-FLOP CAN BE CLEARED WHEN A 'WRITE' OPERATION IS EXECUTED FROM THE TARGET EMULATOR MODULE TO AN ADDRESS WHICH IS MAPPED IN THE MEMORY SIMULATOR MAP PROTECTION RAM TO INHIBIT READS AND WRITES. THE 'WRV' FLIP-FLOP WILL BE CLOCKED TO A ZERO AS A RESULT OF THE SIGNAL 'WRE H' BEING ASSERTED LOW AND PULSES ON THE SIGNALS 'WRHB H' AND 'WRLB H'. THE SIGNALS 'WRHB H' AND 'WRLB H' ARE PULSED BY THE TARGET EMULATOR MODULE AT 'PI' TIME WHEN THE TARGET EMULATOR MODULE IS EXECUTING A T-11 WRITE OPERATION. THE PROGRAM WILL CHECK THAT THE MEMORY SIMULATOR SIGNAL 'MSBRK H' IS ASSERTED HIGH AS A RESULT OF THE 'WRV' FLIP-FLOP BEING CLEARED. THE PROGRAM WILL CHECK THE TARGET EMULATOR MODULES 'MEMBRK' FLIP-FLOP TO BE CLEARED AND THEN CAUSE A PULSE TO BE ISSUED ON TARGET EMULATOR MODULE SIGNAL 'XRAS H'. THE PROGRAM WILL NOW CHECK THE 'MEMBRK' FLIP-FLOP TO BE SET TO A ONE AS A RESULT OF A PULSE ON 'XRAS H' AND THE MEMORY SIMULATOR SYSTEM BUS SIGNAL 'MSBRK H' BEING ASSERTED HIGH. THE PROGRAM WILL PRESET THE 'WRV' FLIP-FLOP BY PULSING MEMORY SIMULATOR SIGNAL 'RST H' AND CHECK THAT THE SIGNAL 'MSBRK H' WENT TO THE LOW STATE AS A RESULT OF THE 'WRV' FLIP-FLOP BEING PRESET. THE PROGRAM WILL CLEAR THE 'MEMBRK' FLIP-FLOP BY PULSING TARGET EMULATOR SIGNAL 'BRKRES L' AND CHECK THAT THE 'MEMBRK' FLIP-FLOP CLEARED.

TEST 11:

THIS TEST WILL CHECK THAT TARGET EMULATOR FDAL REGISTER BITS 7:2 CAN BE CLOCKED INTO THE TDAL DIAGNOSTIC LATCHES IN 16 BIT MODE WHEN THE TARGET EMULATOR MODULE IS ADDRESSING A LOCATION WHICH IS MAPPED ON THE MEMORY SIMULATOR MODULE TO ALLOW READS AND WRITES TO THE TARGET RAM. TO CHECK THAT THE TDAL LATCHES WERE CLOCKED WITH FDAL REGISTER DATA, THE PROGRAM WILL ENABLE THE TDAL LATCHES TO THE EIDAL BUS WITH THE TARGET RAM STILL BEING ADDRESSED. THE PROGRAM WILL THEN READ AND CHECK THE EIDAL BUS TO CONTAIN THE CORRECT FDAL REGISTER DATA.

TEST 12:

THIS TEST WILL CHECK THAT TARGET EMULATOR FDAL REGISTER BITS 7:2 CAN BE CLOCKED INTO THE TDAL DIAGNOSTIC LATCHES IN 8 BIT MODE WHEN THE TARGET EMULATOR MODULE IS ADDRESSING A LOCATION WHICH IS MAPPED ON THE MEMORY SIMULATOR MODULE TO ALLOW READS AND WRITES TO THE TARGET RAM. TO CHECK THAT THE TDAL LATCHES WERE CLOCKED WITH FDAL REGISTER DATA, THE PROGRAM WILL ENABLE THE TDAL LATCHES TO THE EIDAL BUS WITH THE TARGET RAM STILL BEING ADDRESSED. THE PROGRAM WILL THEN READ AND CHECK THE EIDAL BUS TO CONTAIN THE CORRECT FDAL REGISTER DATA.

TEST 13:

THIS TEST WILL CHECK THAT STATE ANALYZER SIGNAL 'EDBRK H' CAN BE ASSERTED HIGH AND LOW WHEN STATE ANALYZER FUNCTION SELECT FLIP-FLOP 'FUSL2' IS CLEARED AND SET. THE OUTPUT OF FUNCTION SELECT FLIP-FLOP 'FUSL2' IS ENABLED TO THE SYSTEM BUS AS THE SIGNAL 'EDBRK H' WHEN THE

SIGNAL "CDAL1 H" IS ASSERTED HIGH. THE PROGRAM WILL CHECK THAT THE SIGNAL "EDBRK H" IS ASSERTED HIGH AND LOW BY READING THE SIGNAL IN TARGET EMULATORS CONTROL REGISTER 0. THE TEST WILL ALSO CHECK THAT THE SIGNAL "EDBRK H" WILL CAUSE THE TARGET EMULATOR'S PAUSE STATE LOGIC TO BE ENTERED IN "RUN" MODE WHEN THE SIGNAL "FETCT H" IS ASSERTED HIGH AND A PULSE IS ISSUED ON THE SIGNAL "XRAS H".

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1464 002001 126
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1466 002003 104
1467 002004 104
1468 002005 000
1469 002006 000
1470 002007 000
1471 002010
1472 002010 101
1473 002011
1474 002011 060
1475 002012
1476 002012 000001
1477 002014
1478 002014 000074
1479 002016
1480 002016 035140
1481 002020
1482 002020 000000
1483 002022
1484 002022 002160
1485 002024
1486 002024 000000
1487 002026
1488 002026 035446
1489 002030
1490 002030 000000
1491 002032
1492 002032 000000
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.TITLE PROGRAM HEADER AND TABLES
.SBTTL PROGRAM HEADER

.ENABL ABS
.ENABL AMA
.DSABL GBL
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BGNMOD

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: THE PROGRAM HEADER IS THE INTERFACE BETWEEN
: THE DIAGNOSTIC PROGRAM AND THE SUPERVISOR.
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POINTER BGNSETUP

HEADER CVCDD,A,0,60,0,PRI07
L\$NAME:: ;DIAGNOSTIC NAME
.ASCII /C/
.ASCII /V/
.ASCII /C/
.ASCII /D/
.ASCII /D/
.BYTE 0
.BYTE 0
.BYTE 0
L\$REV:: ;REVISION LEVEL
.ASCII /A/
L\$DEPO:: ;0
.ASCII /0/
L\$UNIT:: ;NUMBER OF UNITS
.WORD T\$PTHV
L\$TIML:: ;LONGEST TEST TIME
.WORD 60.
L\$HPCP:: ;POINTER TO H.W. QUES.
.WORD L\$HARD
L\$SPCP:: ;POINTER TO S.W. QUES.
.WORD 0
L\$HPTP:: ;PTR. TO DEF. H.W. PTABLE
.WORD L\$HW
L\$SPTP:: ;PTR. TO S.W. PTABLE
.WORD 0
L\$LADP:: ;DIAG. END ADDRESS
.WORD L\$LAST
L\$STA:: ;RESERVED FOR APT STATS
.WORD 0
L\$CO::
.WORD 0
L\$DTYP:: ;DIAGNOSTIC TYPE
.WORD 0
L\$APT:: ;APT EXPANSION
.WORD 0

1497	002040		LSDTP::		;PTR. TO DISPATCH TABLE
1498	002040	002124		.WORD	LSDISPATCH
1499	002042		L\$PRIO::		;DIAGNOSTIC RUN PRIORITY
1500	002042	000340		.WORD	PRI07
1501	002044		L\$ENVI::		;FLAGS DESCRIBE HOW IT WAS SETUP
1502	002044	000000		.WORD	0
1503	002046		L\$EXP1::		;EXPANSION WORD
1504	002046	000000		.WORD	0
1505	002050		L\$MREV::		;SVC REV AND EDIT #
1506	002050	003		.BYTE	C\$REVISION
1507	002051	003		.BYTE	C\$EDIT
1508	002052		L\$EF::		;DIAG. EVENT FLAGS
1509	002052	000000		.WORD	0
1510	002054	000000		.WORD	0
1511	002056		L\$SPC::		
1512	002056	000000		.WORD	0
1513	002060		L\$DEVP::		; POINTER TO DEVICE TYPE LIST
1514	002060	002354		.WORD	L\$DVTYP
1515	002062		L\$REPP::		;PTR. TO REPORT CODE
1516	002062	000000		.WORD	0
1517	002064		L\$EXP4::		
1518	002064	000000		.WORD	0
1519	002066		L\$EXP5::		
1520	002066	000000		.WORD	0
1521	002070		L\$AUT::		;PTR. TO ADD UNIT CODE
1522	002070	000000		.WORD	0
1523	002072		L\$DUT::		;PTR. TO DROP UNIT CODE
1524	002072	000000		.WORD	0
1525	002074		L\$LUN::		;LUN FOR EXERCISERS TO FILL
1526	002074	000000		.WORD	0
1527	002076		L\$DESP::		;POINTER TO DIAG. DESCRIPTION
1528	002076	002364		.WORD	L\$DESC
1529	002100		L\$LOAD::		;GENERATE SPECIAL AUTOLOAD EMT
1530	002100	104035		EMT	ESLOAD
1531	002102		L\$ETP::		;POINTER TO ERR_TBL
1532	002102	000000		.WORD	0
1533	002104		L\$IICP::		;PTR. TO INIT CODE
1534	002104	013110		.WORD	L\$INIT
1535	002106		L\$CCP::		;PTR. TO CLEAN-UP CODE
1536	002106	013344		.WORD	L\$CLEAN
1537	002110		L\$ACP::		;PTR. TO AUTO CODE
1538	002110	013342		.WORD	L\$AUTO
1539	002112		L\$PRT::		;PTR. TO PROTECT TABLE
1540	002112	013102		.WORD	L\$PROT
1541	002114		L\$TEST::		;TEST NUMBER
1542	002114	000000		.WORD	0
1543	002116		L\$DLY::		;DELAY COUNT
1544	002116	000000		.WORD	0
1545	002120		L\$HIME::		;PTR. TO HIGH MEM
1546	002120	000000		.WORD	0
1547					

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1553
1554
1555 002122
1556 002122 000015
1557 002124
1558 002124 013376
1559 002126 013404
1560 002130 014264
1561 002132 015666
1562 002134 016766
1563 002136 021130
1564 002140 023750
1565 002142 025426
1566 002144 026610
1567 002146 030114
1568 002150 031070
1569 002152 032572
1570 002154 034304
1571

.SBTTL DISPATCH TABLE

;++
: THE DISPATCH TABLE CONTAINS THE STARTING ADDRESS OF EACH TEST.
: IT IS USED BY THE SUPERVISOR TO DISPATCH TO EACH TEST.
:--

DISPATCH 13.

.WORD 13
L\$DISPATCH::
.WORD T1
.WORD T2
.WORD T3
.WORD T4
.WORD T5
.WORD T6
.WORD T7
.WORD T8
.WORD T9
.WORD T10
.WORD T11
.WORD T12
.WORD T13


```
1572  
1573  
1574  
1575  
1576  
1577  
1578  
1579  
1580  
1581 002156  
1582 002156 000005  
1583 002160  
1584 002160  
1585  
1586 002160 163010  
1587 002162 000370  
1588 002164 000000  
1589 002166 000001  
1590 002170 000002  
1591  
1592  
1593 002172  
1594 002172  
1595  
1596  
1597  
1598  
1599  
1600  
1601  
1602  
1603  
1604  
1605 002172  
1606 002172 000000  
1607 002174  
1608 002174  
1609  
1610  
1611 002174  
1612 002174  
1613  
1614 002174
```

```
.SBTTL DEFAULT HARDWARE P-TABLE  
  
:++  
: THE DEFAULT HARDWARE P-TABLE CONTAINS DEFAULT VALUES OF  
: THE TEST-DEVICE PARAMETERS. THE STRUCTURE OF THIS TABLE  
: IS IDENTICAL TO THE STRUCTURE OF THE HARDWARE P-TABLES,  
: AND IS USED AS A 'TEMPLATE' FOR BUILDING THE P-TABLES.  
:--  
  
          BGNHW  DFPTBL  
          .WORD  L10000-L$HW/2  
L$HW::  
DFPTBL::  
  
          .WORD  163010          ;CSR ADDRESS  
          .WORD  370            ;VECTOR ADDRESS  
          .WORD  0              ;DEVICE SELECTION # FOR MEMORY SIMULATOR  
          .WORD  1              ;DEVICE SELECTION # FOR STATE ANALYZER  
          .WORD  2              ;DEVICE SELECTION # FOR TARGET EMULATOR  
  
          ENDDHW  
L10000:  
  
.SBTTL SOFTWARE P-TABLE  
  
:++  
: THE SOFTWARE TABLE CONTAINS VARIOUS DATA USED BY THE  
: PROGRAM AS OPERATIONAL PARAMETERS. THESE PARAMETERS ARE  
: SET UP AT ASSEMBLY TIME AND MAY BE VARIED BY THE OPERATOR  
: AT RUN TIME.  
:--  
  
          BGNSW  SFPTBL  
          .WORD  L10001-L$SW/2  
L$SW::  
SFPTBL::  
  
          ENDSW  
L10001:  
  
          ENDMOD
```

1615
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002174

002174

.TITLE GLOBAL AREAS
.SBTTL GLOBAL EQUATES SECTION

BGNMOD

;++
: THE GLOBAL EQUATES SECTION CONTAINS PROGRAM EQUATES THAT
: ARE USED IN MORE THAN ONE TEST.
:--

EQUALS

: BIT DIFINITIONS

100000	BIT15== 100000
040000	BIT14== 40000
020000	BIT13== 20000
010000	BIT12== 10000
004000	BIT11== 4000
002000	BIT10== 2000
001000	BIT09== 1000
000400	BIT08== 400
000200	BIT07== 200
000100	BIT06== 100
000040	BIT05== 40
000020	BIT04== 20
000010	BIT03== 10
000004	BIT02== 4
000002	BIT01== 2
000001	BIT00== 1
001000	BIT9== BIT09
000400	BIT8== BIT08
000200	BIT7== BIT07
000100	BIT6== BIT06
000040	BIT5== BIT05
000020	BIT4== BIT04
000010	BIT3== BIT03
000004	BIT2== BIT02
000002	BIT1== BIT01
000001	BIT0== BIT00

: EVENT FLAG DEFINITIONS
: EF32:EF17 RESERVED FOR SUPERVISOR TO PROGRAM COMMUNICATION

000040	EF.START== 32.	: START COMMAND WAS ISSUED
000037	EF.RESTART== 31.	: RESTART COMMAND WAS ISSUED
000036	EF.CONTINUE== 30.	: CONTINUE COMMAND WAS ISSUED
000035	EF.NEW== 29.	: A NEW PASS HAS BEEN STARTED
000034	EF.PWR== 28.	: A POWER-FAIL/POWER-UP OCCURRED

: PRIORITY LEVEL DEFINITIONS

1671	000340	PRI07== 340
1672	000300	PRI06== 300
1673	000240	PRI05== 240
1674	000200	PRI04== 200
1675	000140	PRI03== 140
1676	000100	PRI02== 100
1677	000040	PRI01== 40
1678	000000	PRI00== 0
1679		:
1680		:OPERATOR FLAG BITS
1681		:
1682	000004	EVL== 4
1683	000010	LOT== 10
1684	000020	ADR== 20
1685	000040	IDU== 40
1686	000100	ISR== 100
1687	000200	UAM== 200
1688	000400	BOE== 400
1689	001000	PNT== 1000
1690	002000	PRI== 2000
1691	004000	IXE== 4000
1692	010000	IBE== 10000
1693	020000	IER== 20000
1694	040000	LOE== 40000
1695	100000	HOE== 100000
1696		

```
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708      100000
1709
1710
1711
1712
1713
1714
1715
1716
1717      004000
1718      002000
1719      001000
1720      000400
1721
1722
1723
1724      000100
1725      000040
1726      000020
1727      000010
1728      000004
1729      000002
1730
1731      000001
1732
1733
1734
1735
1736
1737
1738
1739      000200
1740      000100
1741      000040
1742
1743
1744
1745      000010
1746      000004
1747
1748
1749
1750
1751
1752
```

```
*****
:
:       CDS-11 MEMORY SIMULATOR CONTROL REGISTER INFORMATION
:
:*****
:
:MEMORY SIMULATOR CONTROL REGISTER 0
:
:IDH==  BIT15
:
:BIT 15=1 READ DEVICE TYPE IN 15:8
:MS DEVICE TYPE EQUALS 400 (BIT8=1)
:
:BIT 15=0 READ DEVICE NUMBER INTO BITS 15:8
:
:BIT 14 ALWAYS READ AS A ZERO
:BIT 13 ALWAYS READ AS A ZERO
:BIT 12 ALWAYS READ AS A ZERO
:
:BITS 11-8 ARE USED TO SELECT THE
:DEVICE NUMBER TO ASSERT THE SIGNAL
:DEVE L. WHEN SELECTING MS THESE BITS
:MUST = THE SETTING OF SWITCHES DEV 3:0
:
:BIT 7 ALWAYS READ AS A ZERO (UNUSED)
:
:CKH==  BIT6
:WRVH== BIT5
:RDVH== BIT4
:BIT8H== BIT3
:MPH==  BIT2
:CTSH== BIT1
:
:RSTH== BIT0
:
:MEMORY SIMULATOR CONTROL REGISTER 2
:
:
:BITS 15:8 ARE NOT AVAILABLE
:
:MSBRKH==BIT7
:WRENH== BIT6
:ESRH==  BIT5
:
:BIT 4 ALWAYS READ AS A ZERO (UNUSED)
:
:MSEL1== BIT3
:MSEL0== BIT2
:
:MSEL1=0 MSEL0=0 - SELECT SIMULATOR MEMORY - SSM L
:MSEL1=0 MSEL0=1 - SELECT MODULE SELECT MEMORY 0 - SMDS0 L
:MSEL1=1 MSEL0=0 - SELECT MAP PROTECT MEMORY - SMPM L
:MSEL1=1 MSEL0=1 - SELECT MODULE SELECT MEMORY 1 - SMDS1 L
```



```
1753      000002      MSAD17==BIT1      :MEMORY SIMULATOR ADDRESS 17 (R/W)
1754      000001      MSAD16==BIT0      :MEMORY SIMULATOR ADDRESS 16 (R/W)
1755
1756
1757      :
1758      :MEMORY SIMULATOR CONTROL REGISTER 4
1759      :
1760      100000      MSAD15==BIT15     :MEMORY SIMULATOR ADDRESS 15 (R/W)
1761      040000      MSAD14==BIT14     :MEMORY SIMULATOR ADDRESS 14 (R/W)
1762      020000      MSAD13==BIT13     :MEMORY SIMULATOR ADDRESS 13 (R/W)
1763      010000      MSAD12==BIT12     :MEMORY SIMULATOR ADDRESS 12 (R/W)
1764      004000      MSAD11==BIT11     :MEMORY SIMULATOR ADDRESS 11 (R/W)
1765      002000      MSAD10==BIT10     :MEMORY SIMULATOR ADDRESS 10 (R/W)
1766      001000      MSAD9== BIT9      :MEMORY SIMULATOR ADDRESS 09 (R/W)
1767      000400      MSAD8== BIT8      :MEMORY SIMULATOR ADDRESS 08 (R/W)
1768      000200      MSAD7== BIT7      :MEMORY SIMULATOR ADDRESS 07 (R/W)
1769      000100      MSAD6== BIT6      :MEMORY SIMULATOR ADDRESS 06 (R/W)
1770      000040      MSAD5== BIT5      :MEMORY SIMULATOR ADDRESS 05 (R/W)
1771      000020      MSAD4== BIT4      :MEMORY SIMULATOR ADDRESS 04 (R/W)
1772      000010      MSAD3== BIT3      :MEMORY SIMULATOR ADDRESS 03 (R/W)
1773      000004      MSAD2== BIT2      :MEMORY SIMULATOR ADDRESS 02 (R/W)
1774      000002      MSAD1== BIT1      :MEMORY SIMULATOR ADDRESS 01 (R/W)
1775      000001      MSAD0== BIT0      :MEMORY SIMULATOR ADDRESS 00 (R/W)
1776
1777
1778      :
1779      :MEMORY SIMULATOR MAP PROTECT BITS - CONTROL REGISTER 6
1780      :
1781      000010      MUTB== BIT3       :
1782      000004      RDEH== BIT2       :READ ENABLED SIMULATOR MEMORY
1783      000002      WREH== BIT1       :WRITE ENABLED SIMULATOR MEMORY
1784      000001      MPINH== BIT0      :MAPPED INTO MEMORY SIMULATOR
```

```

1785      :*****
1786      :
1787      :
1788      :
1789      :*****
1790
1791
1792      :
1793      :CONTROL REGISTER 0 (CDAL BITS 15:0)
1794      :
1795
1796      100000      CDAL15==BIT15      ;BIT15=1 READ DEVICE TYPE IN BITS 15:8
1797      ;STATE ANALYZER DEVICE TYPE = 1000 (BIT9=1)
1798      ;
1799      ;BIT15=0 READ DEVICE NUMBER INTO
1800      ;BITS 15:8
1801
1802      040000      CDAL14==BIT14      ;ALWAYS READ AS A ZERO
1803      020000      CDAL13==BIT13      ;ALWAYS READ AS A ZERO
1804      010000      CDAL12==BIT12      ;ALWAYS READ AS A ZERO
1805
1806      004000      CDAL11==BIT11      ;BITS 11:8 ARE USED TO SELECT THE DEVICE
1807      002000      CDAL10==BIT10      ;NUMBER TO ASSERT THE SIGNAL DEVE L.
1808      001000      CDAL9== BIT9      ;WHEN SELECTING SA THESE BITS MUST EQUAL
1809      000400      CDAL8== BIT8      ;THE SETTING OF SWITCHES DEV 3:0
1810
1811      000200      CDAL7== BIT7      ;1 - DISABLE OUTPUTS OF OR ADDRESS REG
1812      ;
1813      ;
1814      ;
1815      000100      CDAL6== BIT6      ;1/0 - CLOCK SIGNAL "TRNST H"
1816
1817      000040      CDAL5== BIT5      ;1 - STOP TRACING WHEN TRAD10 H SET HIGH
1818      ;0 - CONTINUOUS TRACING
1819
1820      000020      CDAL4== BIT4      ;1 - ENABLE ALL AND/OR ARRAY RAMS
1821      ;0 - ENABLE ONLY ONE AND/OR ARRAY RAM
1822
1823      000010      CDAL3== BIT3      ;TRACE RAM BUS SELECT
1824      000004      CDAL2== BIT2      ;TRACE RAM BUS SELECT
1825
1826      000002      CDAL1== BIT1      ;ENABLE FUNCTION SELECTS ONTO SYSTEM BUS
1827
1828      000001      CDAL0== BIT0      ;1/0 - ZERO TRACE ADDRESS REG, TRACING
1829      ;
1830      ;
1831      ;
1832      :
1833      :CONTROL REGISTER 2 (PDAL BITS 7:0)
1834      :
1835
1836      ;BITS 15:8 ARE NOT AVAILABLE
1837
1838      000200      PDAL7== BIT7      ;1 - CLEAR EVENT COUNTERS
1839
1840      000100      PDAL6== BIT6      ;1 - PRESET TRACING FLIP-FLOP

```



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1841
1842      000040      PDAL5== BIT5      ;0 - CLEAR FUNCTION SELECT FLIP-FLOPS
1843
1844      000020      PDAL4== BIT4      ;1 - EXTERNAL PROBE "CLK" SIGNAL WILL
1845                                          :   LOAD EXTP 7:0 F/F'S WHEN "CLK" SET LOW
1846
1847                                          ;0 - EXTERNAL PROBE "CLK" SIGNAL WILL
1848                                          :   LOAD EXTP 7:0 F/F'S WHEN "CLK" SET HIGH
1849      000010      PDAL3== BIT3      ;SELECT POINTER REGISTER (SEE BELOW)
1850      000004      PDAL2== BIT2      ;SELECT POINTER REGISTER (SEE BELOW)
1851      000002      PDAL1== BIT1      ;SELECT POINTER REGISTER (SEE BELOW)
1852      000001      PDAL0== BIT0      ;SELECT POINTER REGISTER (SEE BELOW)
1853
1854      ;
1855      ;POINTER REGISTER PTER 15:0 (SELECTED BY PDAL 3:0)
1856      ;
1857
1858      000000      PTER0== 0          ;WPT0,RPT0,R/W TRAM ADDRESS 9:0
1859      000001      PTER1== PDAL0      ;WPT1,RPT1,R/W TRAM DATA LSI-11 TO TRDI 15:0
1860      000002      PTER2== PDAL1      ;WPT2,RPT2,R/W TRAM DATA LSI-11 TO TRDI 31:16
1861      000003      PTER3== PDAL1!PDAL0 ;WPT3,RPT3,R/W TRAM DATA LSI-11 TO TRDI 47:32
1862      000004      PTER4== PDAL2      ;WPT4,RPT4,R/W TRAM DATA LSI-11 TO TRDI 59:48
1863      000005      PTER5== PDAL2!PDAL0 ;WPT5, WRITE TRACE RAM DATA IN BUF 15:0
1864      000006      PTER6== PDAL2!PDAL1 ;WPT6, WRITE TRACE RAM DATA IN BUF 31:16
1865      000007      PTER7== PDAL2!PDAL1!PDAL0 ;WPT7, WRITE TRACE RAM DATA IN BUF 47:32
1866      000010      PTER8== PDAL3      ;WPT8, WRITE TRACE RAM DATA IN BUF 59:48
1867      000011      PTER9== PDAL3!PDAL0 ;WPT9, LOAD EVENT COUNTER 0
1868      000012      PTER10==PDAL3!PDAL1 ;WPT10,LOAD EVENT COUNTER 1
1869      000013      PTER11==PDAL3!PDAL1!PDAL0 ;WPT11,LOAD EVENT COUNTER 2
1870      000014      PTER12==PDAL3!PDAL2 ;WPT12,LOAD EVENT COUNTER 3
1871      000015      PTER13==PDAL3!PDAL2!PDAL0 ;NOT USED
1872      000016      PTER14==PDAL3!PDAL2!PDAL1 ;NOT USED
1873      000017      PTER15==PDAL3!PDAL2!PDAL1!PDAL0 ;WPT15,RPT15, R/W "OR" ADDRESS
1874
1875

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1883
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1885
1886
1887      100000      GDAL15==BIT15      ;BIT15=1 READ DEVICE TYPE IN 15:8
1888                                     ;TE DEVICE TYPE EQUALS 0000
1889                                     ;
1890                                     ;BIT15=0 READ DEVICE NUMBER INTO
1891                                     ;BITS 11:8
1892
1893      040000      GDAL14==BIT14      ;ALWAYS A 0 ON READ
1894      020000      GDAL13==BIT13      ;ALWAYS A 0 ON READ
1895      010000      GDAL12==BIT12      ;ALWAYS A 0 ON READ
1896
1897      004000      GDAL11==BIT11      ;BITS 11-8 ARE USED TO SELECT THE
1898      002000      GDAL10==BIT10      ;DEVICE NUMBER TO ASSERT THE SIGNAL
1899      001000      GDAL9== BIT9       ;DEVE L. WHEN SELECTING TE THESE BITS
1900      000400      GDAL8== BIT8       ;MUST = THE SETTING OF DEV 3 - DEV 0
1901
1902      000200      GDAL7== BIT7       ;SINGLE STEP BREAK INDICATOR (READ ONLY)
1903      000100      GDAL6== BIT6       ;TIMEOUT BREAK INDICATOR (READ ONLY)
1904      000040      GDAL5== BIT5       ;MEMORY SIM BREAK INDICATOR (READ ONLY)
1905      000020      GDAL4== BIT4       ;STATE ANALYZER BREAK INDICATOR (READ ONLY)
1906      00001C      GDAL3== BIT3       ;ENABLE INTERRUPTS WHEN = TO 1
1907      000004      GDAL2== BIT2       ;POINTER FOR EXTENDED REG SELECT
1908      000002      GDAL1== BIT1       ;POINTER FOR EXTENDED REG SELECT
1909      000001      GDAL0== BIT0       ;POINTER FOR EXTENDED REG SELECT
1910
1911      ;
1912      ;EXTENDED REGISTER SELECTED VIA GDAL BITS 2:0
1913      ;
1914
1915      000000      ADDRESS==0          ;WRITE DIAG ADDRESS REGISTER (WPT0)
1916                                     ;READ ADDRESS BUS (RPT0)
1917      000001      FJADR== GDAL0       ;WRITE NEW FORCE JUMP ADDRESS REG (WPT1)
1918                                     ;READ FORCE JUMP ADDRESS READBACK REG (RPT1)
1919      000002      FDAL== GDAL1        ;WRITE FDAL AND EOAI REGISTERS (WPT2)
1920                                     ;READ FDAL/EOAI OR FDAL/CTL REG (RPT2)
1921      000003      HDAL== GDAL1!GDAL0  ;WRITE/READ HDAL REGISTER (WPT3 /RPT3)
1922      000004      MODE== GDAL2        ;WRITE/READ MODEE REGISTER (WPT4/RPT4)
1923      000005      TARMOD==GDAL2!GDAL0 ;READ TARGET MODE REGISTER (RPT5)
1924      000006      EIDAL== GDAL2!GDAL1 ;READ EIDAL BUS (RPT6)
1925      000007      EODAL== GDAL2!GDAL1!GDAL0 ;READ EODAL BUS (RPT7)
1926
1927      ;
1928      ;OTHER BIT DEFINITIONS FOR GDAL BITS 7:4
1929      ;
1930
1931      000200      SSBK== GDAL7         ;SINGLE STEP BREAK INDICATOR (READ ONLY)

```


1932	000100	YORF == GDAL6	:TIMEOUT BREAK INDICATOR (READ ONLY)
1933	000040	MEMBR == GDAL5	:MEMORY SIM BREAK INDICATOR (READ ONLY)
1934	000020	EDBRK == GDAL4	:STATE ANALYZER BREAK INDICATOR (READ ONLY)
1935			
1936			
1937		:CONTROL REGISTER 2 (ADAL BITS 15:0)	
1938			
1939			
1940	100000	ADAL15==BIT15	:SELECT COLUMN AI FOR STATE ANALYZER
1941	040000	ADAL14==BIT14	:1 - SELECT ROW/COLUMN FOR AI TO STATE ANALYZER
1942			:0 - SELECT SERVICE FOR AI TO STATE ANALYZER
1943	020000	ADAL13==BIT13	:ENABLE SERVICE FOR EMULATOR
1944	010000	ADAL12==BIT12	:ENABLE MODE FROM EMULATOR
1945	004000	ADAL11==BIT11	:DISABLE SERVICE TO THE TARGET
1946	002000	ADAL10==BIT10	:MASTER SWITCH
1947	001000	ADAL9== BIT9	:ENABLE STATE ANALYZER CLOCKS (1)
1948	000400	ADAL8== BIT8	:ENABLE TIMEOUT BREAK
1949	000200	ADAL7== BIT7	:ENABLE REFRESH TO STATE ANALYZER
1950	000100	ADAL6== BIT6	
1951	000040	ADAL5== BIT5	:1 - ENABLE SINGLE STEP BREAK
1952			:0 - DISABLE SINGLE STEP BREAK
1953	000020	ADAL4== BIT4	:1 - PAUSE STATE MACHINE (RUN MODE)
1954			:0 - PAUSE STATE MACHINE (PAUSE MODE)
1955	000010	ADAL3== BIT3	:POWER-UP FROM TARGET (1)
1956	000004	ADAL2== BIT2	:POWER-UP FROM T-11
1957	000002	ADAL1== BIT1	:ENABLE INTERNAL CLOCK (1)
1958	000001	ADAL0== BIT0	:RESETS BREAK LOGIC (1)
1959			
1960			
1961		:CONTROL REGISTER 4 (VDAL BITS 15:0)	
1962			
1963			
1964	100000	VDAL15==BIT15	:TDFI H - TAKE NEW FORCE JUMP ADDRESS (READ ONLY)
1965	040000	VDAL14==BIT14	:EP8N H - 8 BIT ADDRESS HB F/F (READ ONLY)
1966	020000	VDAL13==BIT13	:EP8G H - 8 BIT ADDRESS LB F/F (READ ONLY)
1967	010000	VDAL12==BIT12	:EP8F H - 8 BIT INSTR HB F/F (READ ONLY)
1968	004000	VDAL11==BIT11	:EPFN H - 16 BIT ADDRESS F/F (READ ONLY)
1969	002000	VDAL10==BIT10	:EPSF H - PAUSE STATE SYNC F/F (READ ONLY)
1970	001000	VDAL9== BIT9	:PSMW H - PAUSE STATE WORKING F/F (READ ONLY)
1971	000400	VDAL8== BIT8	:PSMW H - GET NEW ADDRESS F/F (READ ONLY)
1972	000200	VDAL7== BIT7	:DIAGNOSTIC FETCT H (R/W)
1973	000100	VDAL6== BIT6	:MSDI H - LOGIC LEVEL MSDI H (READ ONLY)
1974	000040	VDAL5== BIT5	:BTS1 H - LOGIC LEVEL BTS1 H (READ ONLY)
1975	000020	VDAL4== BIT4	:EDEOC H - LOGIC LEVEL EDEOC H (READ ONLY)
1976	000010	VDAL3== BIT3	:READ H - LOGIC LEVEL READ H (READ ONLY)
1977	000004	VDAL2== BIT2	:CLOCK TAI, TDAL, 0 PAUSE STATE MACHINE (R/W)
1978	000002	VDAL1== BIT1	:SPARE
1979	000001	VDAL0== BIT0	:ENABLE TAI AND TDAL READBACK FROM POD (R/W)
1980			
1981			
1982		:CONTROL REGISTER 6 (HDAL BITS 15:0)	
1983			
1984			
1985	100000	HDAL15==BIT15	:1/0 - PULSE SIGNAL XPI L
1986	040000	HDAL14==BIT14	:1/0 - PULSE SIGNAL EIDAL17 H
1987	020000	HDAL13==BIT13	:1/0 - PULSE SIGNAL XCAS H

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1988      010000      HDAL12==BIT12      :1/0 - PULSE SIGNAL XRAS H
1989      004000      HDAL11==BIT11      :1/0 - PULSE SIGNAL EIDAL16 H
1990      002000      HDAL10==BIT10      :SPARE
1991      001000      HDAL9== BIT9       :1 - ENABLE DIAG ADDRESS TO ADDRESS BUS
1992      :           :           :0 - ENABLE EIDAL BUS TO ADDRESS BUS
1993      :           :           :   WHEN ADAL10 H IS SET TO A ONE AND
1994      :           :           :   DISABLE DIAG ADDRESS FROM ADDRESS BUS
1995      000400      HDAL8== BIT8       :1/0 - PULSE CREADY H
1996      000200      HDAL7== BIT7       :1/0 - PULSE PBCLR H
1997      000100      HDAL6== BIT6       :1/0 - PULSE PSEL1 H
1998      000040      HDAL5== BIT5       :1/0 - PULSE PSEL0 H
1999      000020      HDAL4== BIT4       :1/0 - PULSE PR/WHB L
2000      000010      HDAL3== BIT3       :1/0 - PULSE PR/WLB L
2001      000004      HDAL2== BIT2       :1 - ENABLES DIAG CONTROL OF T-11 TIMING
2002      :           :           :   AND CONTROL SIGNALS
2003      :           :           :0 - ENABLES T-11 TO GENERATE SIGNALS
2004      000002      HDAL1== BIT1       :SPARE
2005      000001      HDAL0== BIT0       :1/0 - PULSE MSDI H
2006      :
2007      :
2008      :           :CONTROL REGISTER 6 (MODE REG BITS MR 15:0)
2009      :
2010      :
2011      100000      MR15== BIT15      :
2012      040000      MR14== BIT14      :
2013      020000      MR13== BIT13      :
2014      010000      MR12== BIT12      :
2015      004000      MR11== BIT11      :1 - 8 BIT ADDRESS SELECTION
2016      :           :           :0 - 16 BIT ADDRESS SELECTION
2017      002000      MR10== BIT10     :
2018      001000      MR9== BIT9        :
2019      000400      MR8== BIT8        :
2020      000200      MR7== BIT7        :
2021      000100      MR6== BIT6        :
2022      000040      MR5== BIT5        :
2023      000020      MR4== BIT4        :
2024      000010      MR3== BIT3        :
2025      000004      MR2== BIT2        :
2026      000002      MR1== BIT1        :
2027      000001      MR0== BIT0        :
2028      :
2029      :
2030      :           :CONTROL REGISTER 6 (FDAL BITS 7:0)
2031      :
2032      :
2033      :
2034      :           :THE CTL REGISTER AND EOAI REGISTER ARE
2035      :           :MULTIPLICED INTO BITS 15:8. THE REGISTER
2036      :           :TO BE READ IS SELECTED BY FDAL0.
2037      000200      FDAL7== BIT7      :INTERRUPT VECTOR
2038      000100      FDAL6== BIT6      :INTERRUPT VECTOR
2039      000040      FDAL5== BIT5      :INTERRUPT VECTOR
2040      000020      FDAL4== BIT4      :INTERRUPT VECTOR
2041      000010      FDAL3== BIT3      :INTERRUPT VECTOR
2042      000004      FDAL2== BIT2      :INTERRUPT VECTOR
2043      000002      FDAL1== BIT1      :SPARE

```



```
2044      000001      FDAL0== BIT0      ;1 - ENABLES EOA; 7:0 BUS TO BE READ ON 15:8
2045                                          ;0 - ENABLES CTL 7:0 REG TO BE READ ON 15:8
2046
2047
2048      ; CONTROL REGISTER 6 (DIAG. ADDR BITS 15:0)
2049      ;
2050
2051      100000      ADDR15==BIT15      ;
2052      040000      ADDR14==BIT14      ;
2053      020000      ADDR13==BIT13      ;
2054      010000      ADDR12==BIT12      ;
2055      004000      ADDR11==BIT11      ;
2056      002000      ADDR10==BIT10      ;
2057      001000      ADDR9== BIT9      ;
2058      000400      ADDR8== BIT8      ;
2059      000200      ADDR7== BIT7      ;
2060      000100      ADDR6== BIT6      ;
2061      000040      ADDR5== BIT5      ;
2062      000020      ADDR4== BIT4      ;
2063      000010      ADDR3== BIT3      ;
2064      000004      ADDR2== BIT2      ;
2065      000002      ADDR1== BIT1      ;
2066      000001      ADDR0== BIT0      ;
2067
```

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2068      .SBTTL  GLOBAL DATA SECTION
2069
2070      :++
2071      : THE GLOBAL DATA SECTION CONTAINS DATA THAT ARE USED
2072      : IN MORE THAN ONE TEST.
2073      :--
2074
2075
2076      002174      ERRTBL
2077      002174      L$ERRTBL::
2078      002174      000000      ERRTYP::      .WORD      0
2079      002176      000000      ERRNBR::      .WORD      0
2080      002200      000000      ERRMSG::      .WORD      0
2081      002202      000000      ERRBLK::      .WORD      0
2082
2083
2084      :GLOBAL DATA FOR CONTROL REGISTER ADDRESSES AND DEVICE INFORMATION
2085      :
2086
2087      002204      163010      REG0::      .WORD      163010      ;CONTROL REGISTER 0
2088      002206      163012      REG2::      .WORD      163012      ;CONTROL REGISTER 2
2089      002210      163014      REG4::      .WORD      163014      ;CONTROL REGISTER 4
2090      002212      163016      REG6::      .WORD      163016      ;CONTROL REGISTER 6
2091
2092      002214      000000      TEVECT::      .WORD      0      ;TARGET EMULATOR VECTOR ADDRESS
2093
2094      002216      000000      MSDEV::      .WORD      0      ;MEMORY SIMULATOR DEVICE NUMBER
2095      002220      000000      MSTYPE::      .WORD      0      ;MEMORY SIMULATOR DEVICE TYPE
2096
2097      002222      000000      EDDEV::      .WORD      0      ;STATE ANALYZER DEVICE NUMBER
2098      002224      000000      EDTYPE::      .WORD      0      ;STATE ANALYZER DEVICE TYPE
2099
2100      002226      000000      TEDEV::      .WORD      0      ;TARGET EMULATOR DEVICE NUMBER
2101      002230      000000      TETYPE::      .WORD      0      ;TARGET EMULATOR DEVICE TYPE
2102
2103      002232      000000      UNITNB::      .WORD      0      ;NUMBER OF UNIT BEING TESTED (0-?)
2104
2105
2106      :
2107      :GLOBAL DATA FOR MEMORY SIMULATOR
2108      :
2109
2110      002234      000000      SOLOAD::      .WORD      0      ;WORD LOADED INTO REG 0
2111      002236      000000      SOGOOD::      .WORD      0      ;EXPECTED REGISTER 0 CONTENTS ON READ
2112      002240      000000      SOMASK::      .WORD      0      ;REG 0 MASK WORD
2113      002242      000000      SOREAD::      .WORD      0      ;ACTUAL REGISTER 0 READ FOR REG 0
2114
2115      002244      000000      S2LOAD::      .WORD      0      ;WORD LOADED INTO REGISTER 2
2116      002246      000000      S2GOOD::      .WORD      0      ;EXPECTED REGISTER 2 CONTENTS ON READ
2117      002250      000000      S2MASK::      .WORD      0      ;REGISTER 2 MASK WORD
2118      002252      000000      S2READ::      .WORD      0      ;REG 2 READ WITH MASK BITS CLEARED
2119
2120      002254      000000      S4LOAD::      .WORD      0      ;WORD LOADED INTO REG 4
2121      002256      000000      S4READ::      .WORD      0      ;ACTUAL REGISTER 4 READ
2122
2123      002260      000000      S6LOAD::      .WORD      0      ;WORD LOADED INTO REGISTER 6

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2124 002262 000000 S6GOOD::.WORD 0 :EXPECTED REGISTER 6 CONTENTS ON READ
2125 002264 000000 S6MASK::.WORD 0 :REGISTER 6 MASK WORD
2126 002266 000000 S6READ::.WORD 0 :ACTUAL REGISTER 6 READ
2127 002270 000000 S6BAD::.WORD 0 :REG 6 READ WITH MASK BITS CLEARED
2128
2129
2130 :GLOBAL DATA FOR STATE ANALYZER
2131 :
2132
2133 002272 000000 E0LOAD::.WORD 0 :WORD LOADED INTO REGISTER 0
2134 002274 000000 E0GOOD::.WORD 0 :EXPECTED REG 0
2135 002276 000000 E0READ::.WORD 0 :ACTUAL REG 0 READ
2136
2137 002300 000000 E2LOAD::.WORD 0 :WORD LOADED INTO REGISTER 2
2138 002302 000000 E2READ::.WORD 0 :ACTUAL REGISTER 2 READ
2139
2140 002304 000000 E4LOAD::.WORD 0 :WORD LOADED INTO REGISTER 4
2141 002306 000000 E4GOOD::.WORD 0 :EXPECTED REGISTER 4 DATA
2142 002310 000000 E4MASK::.WORD 0 :REGISTER 4 MASK WORD
2143 002312 000000 E4READ::.WORD 0 :ACTUAL REGISTER 4 READ
2144 002314 000000 E4BAD::.WORD 0 :REG 4 READ WITH MASKED BITS CLEARED
2145
2146 002316 000000 E6LOAD::.WORD 0 :WORD LOADED INTO REGISTER 6
2147 002320 000000 E6MASK::.WORD 0 :REGISTER 6 MASK WORD
2148 002322 000000 E6READ::.WORD 0 :REG 6 READ WITH MASKED BITS CLEARED
2149
2150 :GLOBAL DATA FOR TARGET EMULATOR
2151 :
2152 :
2153
2154 002324 000000 T0LOAD::.WORD 0 :WORD LOADED INTO REGISTER 0
2155 002326 000000 T0GOOD::.WORD 0 :EXPECTED REG 0
2156 002330 000000 T0MASK::.WORD 0 :BITS TO BE IGNORED ON COMPARE
2157 002332 000000 T0READ::.WORD 0 :DATA READ MASKED WITH TOMASK
2158
2159 002334 000000 T2LOAD::.WORD 0 :WORD LOADED INTO REGISTER 2
2160 002336 000000 T2READ::.WORD 0 :ACTUAL REG 2 READ
2161
2162 002340 000000 T4LOAD::.WORD 0 :WORD LOADED INTO REGISTER 4
2163 002342 000000 T4GOOD::.WORD 0 :EXPECTED DATA FROM REGISTER 4
2164 002344 000000 T4READ::.WORD 0 :DATA READ FROM REGISTER 4
2165
2166 002346 000000 T6LOAD::.WORD 0 :WORD LOADED INTO REGISTER 6
2167 002350 000000 T6READ::.WORD 0 :ACTUAL REGISTER 6 READ
2168 002352 000000 T6MASK::.WORD 0 :BITS TO BE IGNORED

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002354 042103 026523 030461
002362 000
002364

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002364 054523 052123 046505
002372 041040 051525 042040
002400 040511 027107 000
002406

002406 042524 052040 020117
002414 051515 040440 042104
002422 042522 051523 041040
002430 051525 042440 051122
002436 051117 026440 046440
002444 040523 020104 033461
002452 030472 000066
002456 040515 020120 051120
002464 052117 041505 020124
002472 047514 044507 020103
002500 051105 047522 000122

```
.SBTTL GLOBAL TEXT SECTION
:++
: THE GLOBAL TEXT SECTION CONTAINS FORMAT STATEMENTS,
: MESSAGES, AND ASCII INFORMATION THAT ARE USED IN
: MORE THAN ONE TEST.
:--

:
: NAMES OF DEVICES SUPPORTED BY PROGRAM
:
:      DEVTYP <CDS-11>
L$DVTYP::
:      .ASCIZ /CDS-11/
:      .EVEN

: TEST DESCRIPTION
:
:      DESCRIPT      <SYSTEM BUS DIAG.>
L$DESC::
:      .ASCIZ /SYSTEM BUS DIAG./
:      .EVEN

:*****
:      ERROR MESSAGES FOR MEMORY SIMULATOR MODULE
:*****

: CONTROL REGISTER 0 ERROR MESSAGES
:
: CONTROL REGISTER 2 ERROR MESSAGES
:
: TEMSA1::.ASCIZ /TE TO MS ADDRESS BUS ERROR - MSAD 17:16/
:
: MSGMPL::.ASCIZ /MAP PROTECT LOGIC ERROR/
:
:
```



```
2225 ;CONTROL REGISTER 4 ERROR MESSAGES
2226 ;
2227
2228 002506 051515 042101 030440 MSADRG::.ASCIZ /MSAD 15:0 REG ERROR/
2229 002514 035065 020060 042522
2230 002522 020107 051105 047522
2231 002530 000122
2232 002532 042524 052040 020117 TEMSAD::.ASCIZ /TE TO MS ADDRESS BUS ERROR - MSAD 15:0/
2233 002540 051515 040440 042104
2234 002546 042522 051523 041040
2235 002554 051525 042440 051122
2236 002562 051117 026440 046440
2237 002570 040523 020104 032461
2238 002576 030072 000
2239
2240 ;CONTROL REGISTER 6 ERROR MESSAGES
2241 ;
2242 ;
2243
2244 002601 104 052101 020101 MSGMP::.ASCIZ /DATA ERROR IN MAP PROTECT RAM/
2245 002606 051105 047522 020122
2246 002614 047111 046440 050101
2247 002622 050040 047522 042524
2248 002630 052103 051040 046501
2249 002636 000
2250 002637 104 052101 020101 MSGMS0::.ASCIZ /DATA ERROR IN MODULE SELECT RAM 0/
2251 002644 051105 047522 020122
2252 002652 047111 046440 042117
2253 002660 046125 020105 042523
2254 002666 042514 052103 051040
2255 002674 046501 030040 000
2256 002701 104 052101 020101 MSGMS1::.ASCIZ /DATA ERROR IN MODULE SELECT RAM 1/
2257 002706 051105 047522 020122
2258 002714 047111 046440 042117
2259 002722 046125 020105 042523
2260 002730 042514 052103 051040
2261 002736 046501 030440 000
2262 002743 104 052101 020101 MSGMSR::.ASCIZ /DATA ERROR IN MEMORY SIMULATOR RAM/
2263 002750 051105 047522 020122
2264 002756 047111 046440 046505
2265 002764 051117 020131 044523
2266 002772 052515 040514 047524
2267 003000 020122 040522 000115
```

```
2268 :*****
2269 :
2270 :          ERROR MESSAGES FOR STATE ANALYZER MODULE
2271 :
2272 :*****
2273 :
2274 :
2275 :
2276 :CONTROL REGISTER 0 ERROR MESSAGES
2277 :
2278 :
2279 003006 042103 046101 030440 CDALRG::.ASCIZ /CDAL 15:0 REG ERROR/
2280 003014 035065 020060 042522
2281 003022 020107 051105 047522
2282 003030 000122
2283 :
2284 :
2285 :CONTROL REGISTER 2 ERROR MESSAGES
2286 :
2287 :
2288 003032 042120 046101 033440 PDALRG::.ASCIZ /PDAL 7:0 REG ERROR/
2289 003040 030072 051040 043505
2290 003046 042440 051122 051117
2291 003054 000
2292 :
2293 :
2294 :CONTROL REGISTER 4 ERROR MESSAGES
2295 :
2296 :
2297 003055 117 020122 051101 ORDATA::.ASCIZ /OR ARRAY RAM DATA ERROR - ORO 7:0/
2298 003062 040522 020131 040522
2299 003070 020115 040504 040524
2300 003076 042440 051122 051117
2301 003104 026440 047440 047522
2302 003112 033440 030072 000
2303 003117 106 051525 033514 FUSL7::.ASCIZ /FUSL7 FLIP-FLOP - OR ARRAY RAM DATA ERROR/
2304 003124 043040 044514 026520
2305 003132 046106 050117 026440
2306 003140 047440 020122 051101
2307 003146 040522 020131 040522
2308 003154 020115 040504 040524
2309 003162 042440 051122 051117
2310 003170 000
2311 :
2312 :
2313 :CONTROL REGISTER 6 ERROR MESSAGES
2314 :
2315 :
2316 003171 124 020105 047524 TEEDAD::.ASCIZ /TE TO SA ADDRESS BUS ERROR - TRDI 15:0/
2317 003176 051440 020101 042101
2318 003204 051104 051505 020123
2319 003212 052502 020123 051105
2320 003220 047522 020122 020055
2321 003226 051124 044504 030440
2322 003234 035065 000060
2323 003240 042524 052040 020117 TEEDA1::.ASCIZ /TE TO SA - XSEL1, EDSEL0, ADDR 17:16 + BTS 3:0 ERROR - TRDI 47:32/
```


2324	003246	040523	026440	054040	
2325	003254	042523	030514	020054	
2326	003262	042105	042523	030114	
2327	003270	020054	042101	051104	
2328	003276	030440	035067	033061	
2329	003304	025440	041040	051524	
2330	003312	031440	030072	042440	
2331	003320	051122	051117	026440	
2332	003326	052040	042122	020111	
2333	003334	033464	031472	000062	
2334	003342	042524	041440	046124	TEEDCT::.ASCIZ /TE CTL BUS 7:0 TO SA TRDI BUS BITS 47:40 ERROR/
2335	003350	041040	051525	033440	
2336	003356	030072	052040	020117	
2337	003364	040523	052040	042122	
2338	003372	020111	052502	020123	
2339	003400	044502	051524	032040	
2340	003406	035067	030064	042440	
2341	003414	051122	051117	000	
2342					
2343	003421	115	020123	040522	MSEDDE::.ASCIZ /MS RAM DATA TO SA TRDI BUS BITS 31:16 ERROR/
2344	003426	020115	040504	040524	
2345	003434	052040	020117	040523	
2346	003442	052040	042122	020111	
2347	003450	052502	020123	044502	
2348	003456	051524	031440	035061	
2349	003464	033061	042440	051122	
2350	003472	051117	000		
2351	003475	124	040522	042503	TRADRS::.ASCIZ /TRACE RAM ADDRESS REG ERROR - TRAD 10:0/
2352	003502	051040	046501	040440	
2353	003510	042104	042522	051523	
2354	003516	051040	043505	042440	
2355	003524	051122	051117	026440	
2356	003532	052040	040522	020104	
2357	003540	030061	030072	000	
2358	003545	117	020122	042101	ORADER::.ASCIZ /OR ADDRESS REG ERROR - ORAD 3:0/
2359	003552	051104	051505	020123	
2360	003560	042522	020107	051105	
2361	003566	047522	020122	020055	
2362	003574	051117	042101	031440	
2363	003602	030072	000		
2364	003605	106	051525	020114	FUSL30::.ASCIZ /FUSL 3:0 FLIP-FLOP ERROR/
2365	003612	035063	020060	046106	
2366	003620	050111	043055	047514	
2367	003626	020120	051105	047522	
2368	003634	000122			

```

2369 :*****
2370 :
2371 :          ERROR MESSAGES FOR TARGET EMULATOR MODULE
2372 :
2373 :*****
2374 :
2375 :
2376 :ASCII MESSAGES USED BY ERROR CALLS
2377 :
2378 :CONTROL REGISTER 0 ERROR MESSAGES
2379 :
2380 003636 042107 046101 030440 GDALRG::.ASCIZ /GDAL 15:0 REG ERROR/
2381 003644 035065 020060 042522
2382 003652 020107 051105 047522
2383 003660 000122
2384 :
2385 :CONTROL REGISTER 2 ERROR MESSAGES
2386 :
2387 003662 042101 046101 030440 ADALRG::.ASCIZ /ADAL 15:0 REG ERROR/
2388 003670 035065 020060 042522
2389 003676 020107 051105 047522
2390 003704 000122
2391 :
2392 :CONTROL REGISTER 4 ERROR MESSAGES
2393 :
2394 003706 042126 046101 033440 VDALRG::.ASCIZ /VDAL 7:0 OR PAUSE STATE MACHINE ERROR/
2395 003714 030072 047440 020122
2396 003722 040520 051525 020105
2397 003730 052123 052101 020105
2398 003736 040515 044103 047111
2399 003744 020105 051105 047522
2400 003752 000122
2401 :
2402 :CONTROL REGISTER 6 ERROR MESSAGES
2403 :
2404 003754 042110 046101 030440 HDALRG::.ASCIZ /HDAL 15:0 REG ERROR/
2405 003762 035065 020060 042522
2406 003770 020107 051105 047522
2407 003776 000122
2408 004000 051115 030440 035065 MODREG::.ASCIZ /MR 15:0 REG ERROR/
2409 004006 020060 042522 020107
2410 004014 051105 047522 000122
2411 004022 042106 046101 033440 FDALRG::.ASCIZ /FDAL 7:0 REG ERROR/
2412 004030 030072 051040 043505
2413 004036 042440 051122 051117
2414 004044 000
2415 004045 0105 040517 020111 EOAIFD::.ASCIZ /EOAI 7:0 OR FDAL 7:0 REG ERROR/
2416 004052 035067 020060 051117
2417 004060 043040 040504 020114
2418 004066 035067 020060 042522
2419 004074 020107 051105 047522
2420 004102 000122
2421 004104 052103 020114 035067 CTLFDL::.ASCIZ /CTL 7:0 OR FDAL 7:0 REG ERROR/
2422 004112 020060 051117 043040
2423 004120 040504 020114 035067
2424 004126 020060 042522 020107

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2425	004134	051105	047522	000122	
2426	004142	044504	043501	040440	ADDRRG::.ASCIZ /DIAG ADDR 15:0 REG ERROR/
2427	004150	042104	020122	032461	
2428	004156	030072	051040	043505	
2429	004164	042440	051122	051117	
2430	004172	000			
2431	004173	106	051117	042503	FJADRG::.ASCIZ /FORCE JUMP ADDRESS READBACK REG ERROR/
2432	004200	045040	046525	020120	
2433	004206	042101	051104	051505	
2434	004214	020123	042522	042101	
2435	004222	040502	045503	051040	
2436	004230	043505	042440	051122	
2437	004236	051117	000		
2438	004241	115	020123	040522	MSTEDE::.ASCIZ /MS RAM DATA TO TE EODAL BUS ERROR VIA SYSTEM DATA BUS/
2439	004246	020115	040504	040524	
2440	004254	052040	020117	042524	
2441	004262	042440	042117	046101	
2442	004270	041040	051525	042440	
2443	004276	051122	051117	053040	
2444	004304	040511	051440	051531	
2445	004312	042524	020115	040504	
2446	004320	040524	041040	051525	
2447	004326	000			
2448	004327	115	020123	040522	MSTEEI::.ASCIZ /MS RAM DATA TO TE EIDAL BUS ERROR VIA EODAL + SYSTEM BUS/
2449	004334	020115	040504	040524	
2450	004342	052040	020117	042524	
2451	004350	042440	042111	046101	
2452	004356	041040	051525	042440	
2453	004364	051122	051117	053040	
2454	004372	040511	042440	042117	
2455	004400	046101	025440	051440	
2456	004406	051531	042524	020115	
2457	004414	052502	000123		
2458	004420	051515	051040	046501	MSTETD::.ASCIZ /MS RAM DATA TO TE EIDAL BUS ERROR VIA TDAL BUS LATCHES/
2459	004426	042040	052101	020101	
2460	004434	047524	052040	020105	
2461	004442	044505	040504	020114	
2462	004450	052502	020123	051105	
2463	004456	047522	020122	044526	
2464	004464	020101	042124	046101	
2465	004472	041040	051525	046040	
2466	004500	052101	044103	051505	
2467	004506	000			
2468	004507	115	046505	051102	NOINT::.ASCIZ /MEMBRK H FAILED TO SET BREAK FLIP-FLOP OR FAILED TO INTERRUPT/
2469	004514	020113	020110	040506	
2470	004522	046111	042105	052040	
2471	004530	020117	042523	020124	
2472	004536	051102	040505	020113	
2473	004544	046106	050111	043055	
2474	004552	047514	020120	051117	
2475	004560	043040	044501	042514	
2476	004566	020104	047524	044440	
2477	004574	052116	051105	052522	
2478	004602	052120	000		
2479	004605	106	040504	020114	FDEODL::.ASCIZ /FDAL REG 7:2 TO EODAL BUS ERROR/
2480	004612	042522	020107	035067	

GLOBAL AREAS
CVCDDA.P11

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GLOBAL TEXT SECTION

M 4

SEQ 0051

2481	004620	020062	047524	042440	
2482	004626	042117	046101	041040	
2483	004634	051525	042440	051122	
2484	004642	051117	000		
2485	004645	106	040504	020114	FDEIDL::.ASCIZ /FDAL REG 7:2 TO EIDAL BUS ERROR/
2486	004652	042522	020107	035067	
2487	004660	020062	047524	042440	
2488	004666	042111	046101	041040	
2489	004674	051525	042440	051122	
2490	004702	051117	000		
2491	004705	106	040504	020114	FDTDEI::.ASCIZ /FDAL REG 7:2 TO TDAL LATCHES TO EIDAL BUS ERROR/
2492	004712	042522	020107	035067	
2493	004720	020062	047524	052040	
2494	004726	040504	020114	040514	
2495	004734	041524	042510	020123	
2496	004742	047524	042440	042111	
2497	004750	046101	041040	051525	
2498	004756	042440	051122	051117	
2499	004764	000			
2500		004766			

.EVEN

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: FORMAT STATEMENTS USED IN PRINT CALLS
:*****

004766	040445	047503	052116	EMSGR0::ASCIZ	/%ACONTROL REG 0 ERROR%N/
004774	047522	020114	042522		
005002	020107	020060	051105		
005010	047522	022522	000116	EMSGR2::ASCIZ	/%ACONTROL REG 2 ERROR%N/
005016	040445	047503	052116		
005024	047522	020114	042522		
005032	020107	020062	051105		
005040	047522	022522	000116	EMSGR4::ASCIZ	/%ACONTROL REG 4 ERROR%N/
005046	040445	047503	052116		
005054	047522	020114	042522		
005062	020107	020064	051105		
005070	047522	022522	000116	EMSGR6::ASCIZ	/%ACONTROL REG 6 ERROR%N/
005076	040445	047503	052116		
005104	047522	020114	042522		
005112	020107	020066	051105		
005120	047522	022522	000116		
005126	040445	042522	030107	REG0EQ::ASCIZ	/%AREG0 = /
005134	036440	000040			
005140	040445	042522	031107	REG2EQ::ASCIZ	/%AREG2 = /
005146	036440	000040			
005152	040445	042522	032107	REG4EQ::ASCIZ	/%AREG4 = /
005160	036440	000040			
005164	040445	042522	033107	REG6EQ::ASCIZ	/%AREG6 = /
005172	036440	000040			

:
: FORMAT STATEMENTS FOR REPORTING ERROR INFORMATION
:

005176	040445	047514	042101	FSLR::ASCIZ	/%ALOAD: %06%S1%AREAD: %06%N/
005204	020072	047445	022466		
005212	030523	040445	042522		
005220	042101	020072	047445		
005226	022466	000116			
005232	040445	047514	042101	FSLGB::ASCIZ	/%ALOAD: %06%S1%AGOOD: %06%S1%AREAD: %06%N/
005240	020072	047445	022466		
005246	030523	040445	047507		
005254	042117	020072	047445		
005262	022466	030523	040445		
005270	042522	042101	020072		
005276	047445	022466	000116		

.EVEN

```

2551 .SBTTL GLOBAL ERROR REPORT SECTION FOR MEMORY SIMULATOR MODULE
2552
2553 005304 BGNMSG S0EROR
2554 005304 S0EROR::
2555 005304 004537 006760 JSR R5,PRNTBS ;GO PRINT CONTROL REGISTER THAT FA'LED
2556 005310 004766 .WORD EMSGR0
2557 005312 004737 005512 JSR PC,PRNTS0 ;GO PRINT CONTROL REGISTER 0 ERROR INFO
2558 005316 ENDMSG
2559 005316 L10002:
2560 005316 104423 TRAP C$MSG
2561
2562 005320 BGNMSG S2EROR
2563 005320 S2EROR::
2564 005320 004537 006760 JSR R5,PRNTBS ;GO PRINT CONTROL REGISTER THAT FAILED
2565 005324 005016 .WORD EMSGR2
2566 005326 004737 005632 JSR PC,PRNTS2 ;GO PRINT CONTROL REGISTER 2 ERROR INFO
2567 005332 ENDMSG
2568 005332 L10003:
2569 005332 104423 TRAP C$MSG
2570
2571 005334 BGNMSG S4EROR
2572 005334 S4EROR::
2573 005334 004537 006760 JSR R5,PRNTBS ;GO PRINT CONTROL REGISTER THAT FAILED
2574 005340 005046 .WORD EMSGR4
2575 005342 004737 005752 JSR PC,PRNTS4 ;GO PRINT CONTROL REGISTER 4 ERROR INFO
2576 005346 ENDMSG
2577 005346 L10004:
2578 005346 104423 TRAP C$MSG
2579
2580 005350 BGNMSG S6EROR
2581 005350 S6EROR::
2582 005350 004537 006760 JSR R5,PRNTBS ;GO PRINT CONTROL REGISTER THAT FAILED
2583 005354 005076 .WORD EMSGR6
2584 005356 004737 006024 JSR PC,PRNTS6 ;GO PRINT CONTROL REGISTER 6 ERROR INFO
2585 005362 ENDMSG
2586 005362 L10005:
2587 005362 104423 TRAP C$MSG
2588
2589 005364 BGNMSG S02ERR
2590 005364 S02ERR::
2591 005364 004537 006760 JSR R5,PRNTBS ;GO PRINT CONTROL REGISTER THAT FAILED
2592 005370 005016 .WORD EMSGR2
2593 005372 004737 005512 JSR PC,PRNTS0 ;GO PRINT CONTROL REGISTER 0 ERROR INFO
2594 005376 004737 005632 JSR PC,PRNTS2 ;GO PRINT CONTROL REGISTER 2 ERROR INFO
2595 005402 ENDMSG
2596 005402 L10006:
2597 005402 104423 TRAP C$MSG
2598
2599 005404 BGNMSG S04ERR
2600 005404 S04ERR::
2601 005404 004537 006760 JSR R5,PRNTBS ;GO PRINT CONTROLREGISTER THAT FAILED
2602 005410 005046 .WORD EMSGR4
2603 005412 004737 005512 JSR PC,PRNTS0 ;GO PRINT CONTROL REGISTER 0 ERROR INFO
2604 005416 004737 005752 JSR PC,PRNTS4 ;GO PRINT CONTROL REGISTER 4 ERROR INFO
2605 005422 ENDMSG
2606 005422 L10007:

```



```

2607 005422 104423          TRAP  C$MSG
2608
2609 005424          BGNMSG SOALLR
2610 005424          SOALLR::
2611 005424 004537 006760      JSR   R5,PRNTBS      ;GO PRINT CONTROL REGISTER THAT FA'ILED
2612 005430 004766          .WORD EMSGR0
2613 005432 004737 005470      JSR   PC,PRNTAL     ;GO PRINT ALL CONTROL REGISTER'S INFO
2614 005436          ENDMSG
2615 005436          L10010:
2616 005436 104423          TRAP  C$MSG
2617
2618 005440          BGNMSG S2ALLR
2619 005440          S2ALLR::
2620 005440 004537 006760      JSR   R5,PRNTBS     ;GO PRINT CONTROL REGISTER THAT FAILED
2621 005444 005016          .WORD EMSGR2
2622 005446 004737 005470      JSR   PC,PRNTAL     ;GO PRINT ALL CONTROL REGISTER'S INFO
2623 005452          ENDMSG
2624 005452          L10011:
2625 005452 104423          TRAP  C$MSG
2626
2627 005454          BGNMSG S6ALLR
2628 005454          S6ALLR::
2629 005454 004537 006760      JSR   R5,PRNTBS     ;GO PRINT CONTROL REGISTER THAT FAILED
2630 005460 005076          .WORD EMSGR6
2631 005462 004737 005470      JSR   PC,PRNTAL     ;GO PRINT ALL CONTROL REGISTER'S INFO
2632 005466          ENDMSG
2633 005466          L10012:
2634 005466 104423          TRAP  C$MSG
2635
2636          ;
2637          ;ROUTINE TO PRINT ALL CONTROL REGISTERS ERROR INFORMATION
2638          ;
2639
2640 005470 004737 005512      PRNTAL::JSR   PC,PRNTS0 ;GO PRINT CONTROL REGISTER 0 ERROR INFO
2641 005474 004737 005632      JSR   PC,PRNTS2     ;GO PRINT CONTROL REGISTER 2 ERROR INFO
2642 005500 004737 005752      JSR   PC,PRNTS4     ;GO PRINT CONTROL REGISTER 4 ERROR INFO
2643 005504 004737 006024      JSR   PC,PRNTS6     ;GO PRINT CONTROL REGISTER 6 ERROR INFO
2644 005510 000207          RTS    PC           ;RETURN BACK TO THE ERROR ROUTINE
2645
2646          ;PRINT CONTROL REGISTER 0 ERROR INFORMATION
2647
2648 005512          PRNTS0::PRINTX #REGOEQ
2649 005512 012746 005126      MOV   #REGOEQ,-(SP)
2650 005516 012746 000001      MOV   #1,-(SP)
2651 005522 010600          MOV   SP,R0
2652 005524 104415          TRAP  C$PNTX
2653 005526 062706 000004      ADD   #4,SP
2654 005532 023737 002234 002236      CMP   SOLOAD,SOGOOD ;CHECK LOADED DIFFERENT THEN EXPECTED
2655 005540 001417          BEQ   1$           ;IF NOT THEN PRINT 'LOAD' AND 'READ'
2656 005542          PRINTX #FSLGB,SOLOAD,SOGOOD,SOREAD
2657 005542 013746 002242      MOV   SOREAD,-(SP)
2658 005546 013746 002236      MOV   SOGOOD,-(SP)
2659 005552 013746 002234      MOV   SOLOAD,-(SP)
2660 005556 012746 005232      MOV   #FSLGB,-(SP)
2661 005562 012746 000004      MOV   #4,-(SP)
2662 005566 010600          MOV   SP,R0

```

```

2663 005570 104415
2664 005572 062706 000012
2665 005576 000414
2666 005600
2667 005600 013746 002242
2668 005604 013746 002234
2669 005610 012746 005176
2670 005614 012746 000003
2671 005620 010600
2672 005622 104415
2673 005624 062706 000010
2674 005630 000207
2675
2676
2677
2678 005632
2679 005632 012746 005140
2680 005636 012746 000001
2681 005642 010600
2682 005644 104415
2683 005646 062706 000004
2684 005652 023737 002244 002246
2685 005660 001417
2686 005662
2687 005662 013746 002252
2688 005666 013746 002246
2689 005672 013746 002244
2690 005676 012746 005232
2691 005702 012746 000004
2692 005706 010600
2693 005710 104415
2694 005712 062706 000012
2695 005716 000414
2696 005720
2697 005720 013746 002252
2698 005724 013746 002244
2699 005730 012746 005176
2700 005734 012746 000003
2701 005740 010600
2702 005742 104415
2703 005744 062706 000010
2704 005750 000207
2705
2706
2707
2708 005752
2709 005752 012746 005152
2710 005756 012746 000001
2711 005762 010600
2712 005764 104415
2713 005766 062706 000004
2714 005772
2715 005772 013746 002256
2716 005776 013746 002254
2717 006002 012746 005176
2718 006006 012746 000003
    
```

```

TRAP C$PNTX
ADD #12,SP
BR 2$
1$: PRINTX #FSLR,S0LOAD,S0READ
MOV S0READ,-(SP)
MOV S0LOAD,-(SP)
MOV #FSLR,-(SP)
MOV #3,-(SP)
MOV SP,R0
TRAP C$PNTX
ADD #10,SP
2$: RTS PC
    
```

;PRINT CONTROL REGISTER 2 ERROR INFORMATION

```

PRNTS2::PRINTX #REG2EQ
MOV #REG2EQ,-(SP)
MOV #1,-(SP)
MOV SP,R0
TRAP C$PNTX
ADD #4,SP
CMP S2LOAD,S2GOOD ;CHECK IF LOADED DIFFERENT THEN EXPECTED
BEQ 1$ ;IF NOT THEN PRINT 'LOAD' AND 'READ'
PRINTX #FSLGB,S2LOAD,S2GOOD,S2READ
MOV S2READ,-(SP)
MOV S2GOOD,-(SP)
MOV S2LOAD,-(SP)
MOV #FSLGB,-(SP)
MOV #4,-(SP)
MOV SP,R0
TRAP C$PNTX
ADD #12,SP
BR 2$
1$: PRINTX #FSLR,S2LOAD,S2READ
MOV S2READ,-(SP)
MOV S2LOAD,-(SP)
MOV #FSLR,-(SP)
MOV #3,-(SP)
MOV SP,R0
TRAP C$PNTX
ADD #10,SP
2$: RTS PC
    
```

;PRINT CONTROL REGISTER 4 ERROR INFORMATION

```

PRNTS4::PRINTX #REG4EQ
MOV #REG4EQ,-(SP)
MOV #1,-(SP)
MOV SP,R0
TRAP C$PNTX
ADD #4,SP
PRINTX #FSLR,S4LOAD,S4READ
MOV S4READ,-(SP)
MOV S4LOAD,-(SP)
MOV #FSLR,-(SP)
MOV #3,-(SP)
    
```


GLOBAL AREAS
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E 5

GLOBAL ERROR REPORT SECTION FOR MEMORY SIMULATOR MODULE

SEQ 0056

2719 006012 010600
2720 006014 104415
2721 006016 062706 000010
2722 006022 000207
2723
2724
2725
2726 006024
2727 006024 012746 005164
2728 006030 012746 000001
2729 006034 010600
2730 006036 104415
2731 006040 062706 000004
2732 006044 023737 002260 002262
2733 006052 001417
2734 006054
2735 006054 013746 002270
2736 006060 013746 002262
2737 006064 013746 002260
2738 006070 012746 005232
2739 006074 012746 000004
2740 006100 010600
2741 006102 104415
2742 006104 062706 000012
2743 006110 000414
2744 006112
2745 006112 013746 002270
2746 006116 013746 002260
2747 006122 012746 005176
2748 006126 012746 000003
2749 006132 010600
2750 006134 104415
2751 006136 062706 000010
2752 006142 000207

```
MOV SP,R0
TRAP C$PNTX
ADD #10,SP
RTS PC

;PRINT CONTROL REGISTER 6 ERROR INFORMATION
PRNTS6::PRINTX #REG6EQ
MOV #REG6EQ,-(SP)
MOV #1,-(SP)
MOV SP,R0
TRAP C$PNTX
ADD #4,SP
CMP S6LOAD,S6GOOD ;CHECK IF LOADED DIFFERENT THEN EXPECTED
BEQ 1$ ;IF NOT THEN PRINT 'LOAD' AND 'READ'
PRINTX #FSLGB,S6LOAD,S6GOOD,S6BAD
MOV S6BAD,-(SP)
MOV S6GOOD,-(SP)
MOV S6LOAD,-(SP)
MOV #FSLGB,-(SP)
MOV #4,-(SP)
MOV SP,R0
TRAP C$PNTX
ADD #12,SP
BR 2$
1$: PRINTX #FSLR,S6LOAD,S6BAD
MOV S6BAD,-(SP)
MOV S6LOAD,-(SP)
MOV #FSLR,-(SP)
MOV #3,-(SP)
MOV SP,R0
TRAP C$PNTX
ADD #10,SP
2$: RTS PC
```

```

2753      .SBTTL  GLOBAL ERROR REPORT SECTION FOR STATE ANALYZER MODULE
2754
2755      BGNMSG  E0EROR
2756      E0EROR::
2757      JSR      R5,PRNTBS      ;GO PRINT CONTROL REG THAT FAILED
2758      .WORD    EMSGR0
2759      JSR      PC,PRNTE0     ;GO PRINT CONTROL REGISTER 0 INFO
2760      ENDMSG
2761      L10013:
2762      TRAP    C$MSG
2763
2764      BGNMSG  E2EROR
2765      E2EROR::
2766      JSR      R5,PRNTBS      ;GO PRINT CONTROL REG THAT FAILED
2767      .WORD    EMSGR2
2768      JSR      PC,PRNTE2     ;GO PRINT CONTROL REGISTER 2 INFO
2769      ENDMSG
2770      L10014:
2771      TRAP    C$MSG
2772
2773      BGNMSG  E4EROR
2774      E4EROR::
2775      JSR      R5,PRNTBS      ;GO PRINT CONTROL REG THAT FAILED
2776      .WORD    EMSGR4
2777      JSR      PC,PRNTAR     ;GO PRINT ALL CONTROL REGISTERS
2778      ENDMSG
2779      L10015:
2780      TRAP    C$MSG
2781
2782      BGNMSG  E026ER
2783      E026ER::
2784      JSR      R5,PRNTBS      ;GO PRINT CONTROL REG THAT FAILED
2785      .WORD    EMSGR6
2786      JSR      PC,PR026E     ;GO PRINT CONTROL REG'S 0, 2, AND 6
2787      ENDMSG
2788      L10016:
2789      TRAP    C$MSG
2790
2791      BGNMSG  E6ALLR
2792      E6ALLR::
2793      JSR      PC,PRNTBS      ;GO PRINT CONTROL REGISTER THAT FAILED
2794      .WORD    EMSGR6
2795      JSR      PC,PRNTAR     ;GO PRINT ALL CONTROL REGISTER'S INFO
2796      ENDMSG
2797      L10017:
2798      TRAP    C$MSG
2799
2800      ;ROUTINE TO PRINT CONTROL REGISTER 0, 2, AND 6 ERROR INFORMATION
2801
2802      PR026E::JSR      PC,PRNTE0     ;GO PRINT CONTROL REGISTER 0 INFO
2803      JSR      PC,PRNTE2     ;GO PRINT CONTROL REGISTER 2 INFO
2804      JSR      PC,PRNTE6     ;GO PRINT CONTROL REGISTER 6 INFO
2805      RTS      PC
2806
2807      ;ROUTINE TO PRINT ALL THE CONTROL REGISTERS ERROR INFORMATION
2808

```



```
2809 006256 004737 006300 PRNTAR::JSR PC,PRNTE0 ;GO PRINT CONTROL REGISTER 0 INFO
2810 006262 004737 006420 JSR PC,PRNTE2 ;GO PRINT CONTROL REGISTER 2 INFO
2811 006266 004737 006472 JSR PC,PRNTE4 ;GO PRINT CONTROL REGISTER 4 INFO
2812 006272 004737 006612 JSR PC,PRNTE6 ;GO PRINT CONTROL REGISTER 6 INFO
2813 006276 000207 RTS PC
```

;PRINT CONTROL REGISTER 0 ERROR INFORMATION

```
2817 006300 PRNTE0::PRINTX #REG0EQ
2818 006300 012746 005126 MOV #REG0EQ,-(SP)
2819 006304 012746 000001 MOV #1,-(SP)
2820 006310 010600 MOV SP,R0
2821 006312 104415 TRAP C$PNTX
2822 006314 062706 000004 ADD #4,SP
2823 006320 023737 002272 002274 CMP E0LOAD,E0GOOD ;CHECK IF LOADED DIFFERENT THEN EXPECTED
2824 006326 001417 BEQ 1$ ;IF NOT PRINT 'LOAD' AND 'READ:'
2825 006330 PRINTX #FSLGB,E0LOAD,E0GOOD,E0READ
2826 006330 013746 002276 MOV E0READ,-(SP)
2827 006334 013746 002274 MOV E0GOOD,-(SP)
2828 006340 013746 002272 MOV E0LOAD,-(SP)
2829 006344 012746 005232 MOV #FSLGB,-(SP)
2830 006350 012746 000004 MOV #4,-(SP)
2831 006354 010600 MOV SP,R0
2832 006356 104415 TRAP C$PNTX
2833 006360 062706 000012 ADD #12,SP
2834 006364 000414 BR 2$
2835 006366 1$: PRINTX #FSLR,E0LOAD,E0READ
2836 006366 013746 002276 MOV E0READ,-(SP)
2837 006372 013746 002272 MOV E0LOAD,-(SP)
2838 006376 012746 005176 MOV #FSLR,-(SP)
2839 006402 012746 000003 MOV #3,-(SP)
2840 006406 010600 MOV SP,R0
2841 006410 104415 TRAP C$PNTX
2842 006412 062706 000010 ADD #10,SP
2843 006416 000207 2$: RTS PC
```

;PRINT CONTROL REGISTER 2 ERROR INFORMATION

```
2847 006420 PRNTE2::PRINTX #REG2EQ
2848 006420 012746 005140 MOV #REG2EQ,-(SP)
2849 006424 012746 000001 MOV #1,-(SP)
2850 006430 010600 MOV SP,R0
2851 006432 104415 TRAP C$PNTX
2852 006434 062706 000004 ADD #4,SP
2853 006440 PRINTX #FSLR,E2LOAD,E2READ
2854 006440 013746 002302 MOV E2READ,-(SP)
2855 006444 013746 002300 MOV E2LOAD,-(SP)
2856 006450 012746 005176 MOV #FSLR,-(SP)
2857 006454 012746 000003 MOV #3,-(SP)
2858 006460 010600 MOV SP,R0
2859 006462 104415 TRAP C$PNTX
2860 006464 062706 000010 ADD #10,SP
2861 006470 000207 RTS PC
```

;PRINT CONTROL REGISTER 4 ERROR INFORMATION

2862
2863
2864

2865	006472			PRNTE4::PRINTX	#REG4EQ	
2866	006472	012746	005152	MOV	#REG4EQ,-(SP)	
2867	006476	012746	000001	MOV	#1,-(SP)	
2868	006502	010600		MOV	SP,R0	
2869	006504	104415		TRAP	C\$PNTX	
2870	006506	062706	000004	ADD	#4,SP	
2871	006512	023737	002304	CMP	E4LOAD,E4GOOD	;CHECK IF LCADED DIFFERENT THEN EXPECTED
2872	006520	001417		BEQ	1\$;IF NOT THEN PRINT 'LOAD' AND 'READ'
2873	006522			PRINTX	#FSLGB,E4LOAD,E4GOOD,E4BAD	
2874	006522	013746	002314	MOV	E4BAD,-(SP)	
2875	006526	013746	002306	MOV	E4GOOD,-(SP)	
2876	006532	013746	002304	MOV	E4LOAD,-(SP)	
2877	006536	012746	005232	MOV	#FSLGB,-(SP)	
2878	006542	012746	000004	MOV	#4,-(SP)	
2879	006546	010600		MOV	SP,R0	
2880	006550	104415		TRAP	C\$PNTX	
2881	006552	062706	000012	ADD	#12,SP	
2882	006556	000414		BR	2\$	
2883	006560			1\$: PRINTX	#FSLR,E4LOAD,E4BAD	
2884	006560	013746	002314	MOV	E4BAD,-(SP)	
2885	006564	013746	002304	MOV	E4LOAD,-(SP)	
2886	006570	012746	005176	MOV	#FSLR,-(SP)	
2887	006574	012746	000003	MOV	#3,-(SP)	
2888	006600	010600		MOV	SP,R0	
2889	006602	104415		TRAP	C\$PNTX	
2890	006604	062706	000010	ADD	#10,SP	
2891	006610	000207		2\$: RTS	PC	
2892						
2893						
2894						
2895	006612					
2896	006612	012746	005164	PRNTE6::PRINTX	#REG6EQ	
2897	006616	012746	000001	MOV	#REG6EQ,-(SP)	
2898	006622	010600		MOV	#1,-(SP)	
2899	006624	104415		MOV	SP,R0	
2900	006626	062706	000004	TRAP	C\$PNTX	
2901	006632			ADD	#4,SP	
2902	006632	013746	002322	PRINTX	#FSLF E6LOAD,E6READ	
2903	006636	013746	002316	MOV	E6READ,-(SP)	
2904	006642	012746	005176	MOV	E6LOAD,-(SP)	
2905	006646	012746	000003	MOV	#FSLR,-(SP)	
2906	006652	010600		MOV	#3,-(SP)	
2907	006654	104415		MOV	SP,R0	
2908	006656	062706	000010	TRAP	C\$PNTX	
2909	006662	000207		ADD	#10,SP	
2910				RTS	PC	


```

2911      .SBTTL  GLOBAL ERROR REPORT SECTION FOR TARGET EMULATOR MODULE
2912
2913      :++
2914      : THE GLOBAL ERROR REPORT SECTION CONTAINS MESSAGE PRINTING AREAS
2915      : USED BY MORE THAN TEST TO OUTPUT ADDITIONAL ERROR INFORMATION. PRINTB
2916      : (BASIC) AND PRINTX (EXTENDED) CALLS ARE USED TO CALL PRINT SERVICES.
2917      :--
2918
2919
2920      006664      BGNMSG  T0EROR
2921      006664      T0EROR::
2922      006664      004537 006760      JSR      R5,PRNTBS      ;GO PRINT CONTROL REG THAT FAILED
2923      006670      004766      .WORD    EMSGR0
2924      006672      004737 007052      JSR      PC,PRNTT0     ;GO PRINT CONTROL REGISTER 0 INFO
2925      006676      ENDMSG
2926      006676      L10020:
2927      006676      104423      TRAP     C$MSG
2928
2929      006700      BGNMSG  T2EROR
2930      006700      T2EROR::
2931      006700      004537 006760      JSR      R5,PRNTBS      ;GO PRINT CONTROL REG THAT FAILED
2932      006704      005016      .WORD    EMSGR2
2933      006706      004737 007172      JSR      PC,PRNTT2     ;GO PRINT CONTROL REGISTER 2 INFO
2934      006712      ENDMSG
2935      006712      L10021:
2936      006712      104423      TRAP     C$MSG
2937
2938      006714      BGNMSG  T4EROR
2939      006714      T4EROR::
2940      006714      004537 006760      JSR      R5,PRNTBS      ;GO PRINT CONTROL REG THAT FAILED
2941      006720      005046      .WORD    EMSGR4
2942      006722      004737 007244      JSR      PC,PRNTT4     ;GO PRINT CONTROL REGISTER 4 INFO
2943      006726      ENDMSG
2944      006726      L10022:
2945      006726      104423      TRAP     C$MSG
2946
2947      006730      BGNMSG  T06ERR
2948      006730      T06ERR::
2949      006730      004537 006760      JSR      R5,PRNTBS      ;GO PRINT CONTROL REG THAT FAILED
2950      006734      005076      .WORD    EMSGR6
2951      006736      004737 007000      JSR      PC,PR06T      ;GO PRINT CONTROL REG 0 AND 6 INFO
2952      006742      ENDMSG
2953      006742      L10023:
2954      006742      104423      TRAP     C$MSG
2955
2956      006744      BGNMSG  T6ALLR
2957      006744      T6ALLR::
2958      006744      004537 006760      JSR      R5,PRNTBS      ;GO PRINT CONTROL REG THAT FAILED
2959      006750      005076      .WORD    EMSGR6
2960      006752      004737 007030      JSR      PC,ALPRNT     ;GO PRINT ALL CONTROL REGISTER INFO
2961      006756      ENDMSG
2962      006756      L10024:
2963      006756      104423      TRAP     C$MSG
2964
2965      ;ROUTINE TO PRINT WHAT CONTROL REGISTER DETECTED THE ERROR.
2966

```

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SEQ 0061

2967 006760
 2968 006760 012546
 2969 006762 012746 000001
 2970 006766 010600
 2971 006770 104414
 2972 006772 062706 000004
 2973 006776 000205
 2974
 2975
 2976
 2977 007000 004737 007052
 2978 007004 004737 007364
 2979 007010 000207
 2980
 2981
 2982
 2983 007012 004737 007052
 2984 007016 004737 007172
 2985 007022 004737 007364
 2986 007026 000207
 2987
 2988
 2989
 2990 007030 004737 007052
 2991 007034 004737 007172
 2992 007040 004737 007244
 2993 007044 004737 007364
 2994 007050 000207
 2995
 2996
 2997
 2998 007052
 2999 007052 012746 005126
 3000 007056 012746 000001
 3001 007062 010600
 3002 007064 104415
 3003 007066 062706 000004
 3004 007072 023737 002324 002326
 3005 007100 001417
 3006 007102
 3007 007102 013746 002332
 3008 007106 013746 002326
 3009 007112 013746 002324
 3010 007116 012746 005232
 3011 007122 012746 000004
 3012 007126 010600
 3013 007130 104415
 3014 007132 062706 000012
 3015 007136 000414
 3016 007140
 3017 007140 013746 002332
 3018 007144 013746 002324
 3019 007150 012746 005176
 3020 007154 012746 000003
 3021 007160 010600
 3022 007162 104415

```

PRNTBS::PRINTB (R5)+
              MOV (R5)+,-(SP)
              MOV #1,-(SP)
              MOV SP,R0
              TRAP C$PNTB
              ADD #4,SP
              RTS R5

;ROUTINE TO PRINT CONTROL REGISTER 0 AND 6 ERROR INFORMATION
PR06T:: JSR PC,PRNTT0
        JSR PC,PRNTT6
        RTS PC

;ROUTINE TO PRINT CONTROL REGISTER 0, 2 AND 6 ERROR INFORMATION
PR026T::JSR PC,PRNTT0 ;GO PRINT CONTROL REGISTER 0 INFO
        JSR PC,PRNTT2 ;GO PRINT CONTROL REGISTER 2 INFO
        JSR PC,PRNTT6 ;GO PRINT CONTROL REGISTER 6 INFO
        RTS PC

;ROUTINE TO PRINT ALL TARGET EMULATORS CONTROL REGISTER INFORMATION
ALPRNT::JSR PC,PRNTT0 ;GO PRINT CONTROL REGISTER 0 INFO
        JSR PC,PRNTT2 ;GO PRINT CONTROL REGISTER 2 INFO
        JSR PC,PRNTT4 ;GO PRINT CONTROL REGISTER 4 INFO
        JSR PC,PRNTT6 ;GO PRINT CONTROL REGISTER 6 INFO
        RTS PC

;PRINT CONTROL REGISTER 0 ERROR INFORMATION
PRNTT0::PRINTX #REGOEQ
        MOV #REGOEQ,-(SP)
        MOV #1,-(SP)
        MOV SP,R0
        TRAP C$PNTX
        ADD #4,SP
        CMP TOLOAD,TOGOOD ;CHECK IF LOADED DIFFERENT THEN EXPECTED
        BEQ 1$ ;IF NOT THEN PRINT 'LOAD' AND 'READ'
        PRINTX #FSLGB,TOLOAD,TOGOOD,TOREAD
        MOV TOREAD,-(SP)
        MOV TOGOOD,-(SP)
        MOV TOLOAD,-(SP)
        MOV #FSLGB,-(SP)
        MOV #4,-(SP)
        MOV SP,R0
        TRAP C$PNTX
        ADD #12,SP
        BR 2$
1$: PRINTX #FSLR,TOLOAD,TOREAD
    MOV TOREAD,-(SP)
    MOV TOLOAD,-(SP)
    MOV #FSLR,-(SP)
    MOV #3,-(SP)
    MOV SP,R0
    TRAP C$PNTX

```


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SEQ 0062

3023 007164 062706 000010
3024 007170 000207
3025
3026
3027
3028 007172
3029 007172 012746 005140
3030 007176 012746 000001
3031 007202 010600
3032 007204 104415
3033 007206 062706 000004
3034 007212
3035 007212 013746 002336
3036 007216 013746 002334
3037 007222 012746 005176
3038 007226 012746 000003
3039 007232 010600
3040 007234 104415
3041 007236 062706 000010
3042 007242 000207
3043
3044
3045
3046 007244
3047 007244 012746 005152
3048 007250 012746 000001
3049 007254 010600
3050 007256 104415
3051 007260 062706 000004
3052 007264 023737 002340 002342
3053 007272 001417
3054 007274
3055 007274 013746 002344
3056 007300 013746 002342
3057 007304 013746 002340
3058 007310 012746 005232
3059 007314 012746 000004
3060 007320 010600
3061 007322 104415
3062 007324 062706 000012
3063 007330 000414
3064 007332
3065 007332 013746 002344
3066 007336 013746 002340
3067 007342 012746 005176
3068 007346 012746 000003
3069 007352 010600
3070 007354 104415
3071 007356 062706 000010
3072 007362 000207
3073

DD #10,SP
2\$: PC
:PRINT CONTROL REGISTER 2 ERROR INFORMATION
PRNTT2::PRINTX #REG2EQ
MOV #REG2EQ,-(SP)
MOV #1,-(SP)
MOV SP,R0
TRAP C\$PNTX
ADD #4,SP
PRINTX #FSLR,T2LOAD,T2READ
MOV T2READ,-(SP)
MOV T2LOAD,-(SP)
MOV #FSLR,-(SP)
MOV #3,-(SP)
MOV SP,R0
TRAP C\$PNTX
ADD #10,SP
RTS PC

:PRINT CONTROL REGISTER 4 ERROR INFORMATION

PRNTT4::PRINTX #REG4EQ
MOV #REG4EQ,-(SP)
MOV #1,-(SP)
MOV SP,R0
TRAP C\$PNTX
ADD #4,SP
CMP T4LOAD,T4GOOD ;CHECK IF LOADED DIFFERENT THEN EXPECTED
BEQ 1\$;IF NOT THEN PRINT 'LOAD' AND 'READ'
PRINTX #FSLGB,T4LOAD,T4GOOD,T4READ
MOV T4READ,-(SP)
MOV T4GOOD,-(SP)
MOV T4LOAD,-(SP)
MOV #FSLGB,-(SP)
MOV #4,-(SP)
MOV SP,R0
TRAP C\$PNTX
ADD #12,SP
BR 2\$
1\$: PRINTX #FSLR,T4LOAD,T4READ
MOV T4READ,-(SP)
MOV T4LOAD,-(SP)
MOV #FSLR,-(SP)
MOV #3,-(SP)
MOV SP,R0
TRAP C\$PNTX
ADD #10,SP
2\$: RTS PC

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SEQ 0063

:PRINT CONTROL REGISTER 6 ERROR INFORMATION

```
PRNTT6::PRINTX #REG6EQ
MOV #REG6EQ,-(SP)
MOV #1,-(SP)
MOV SP,R0
TRAP C$PNTX
ADD #4,SP
PRINTX #FSLR,T6LOAD,T6READ
MOV T6READ,-(SP)
MOV T6LOAD,-(SP)
MOV #FSLR,-(SP)
MOV #3,-(SP)
MOV SP,R0
TRAP C$PNTX
ADD #10,SP
RTS PC
```

```
3074
3075
3076
3077 007364
3078 007364 012746 005164
3079 007370 012746 000001
3080 007374 010600
3081 007376 104415
3082 007400 062706 000004
3083 007404
3084 007404 013746 002350
3085 007410 013746 002346
3086 007414 012746 005176
3087 007420 012746 000003
3088 007424 010600
3089 007426 104415
3090 007430 062706 000010
3091 007434 000207
3092
```



```
3093      .SBTTL GLOBAL SUBROUTINES SECTION
3094
3095      :++
3096      : THE GLOBAL SUBROUTINES SECTION CONTAINS THE SUBROUTINES
3097      : THAT ARE USED IN MORE THAN ONE TEST.
3098      :--
3099
3100      :++
3101      : FUNCTIONAL DESCRIPTION:
3102      :   SUBROUTINE TO....SELECT AND INITIALIZE TARGET EMULATOR
3103
3104      : INPUTS:
3105      :   LOCATION TEDEV CONTAINS USER DEFINED DEVICE NUMBER IN BITS 11-8
3106      :   LOCATION TETYPE CONTAINS TARGET EMULATOR DEVICE TYPE AND GDAL BIT 15
3107
3108
3109
3110      : IMPLICIT INPUTS:
3111
3112
3113      : OUTPUTS:
3114      :   TLOAD CONTAINS USER DEFINED UNIT NUMBER IN BITS 11-8
3115      :   T2LOAD CONTAINS ALL ZEROES TO INDICATE CONTROL REGISTER 2 WAS CLEARED
3116      :   T4LOAD CONTAINS ALL ZEROES TO INDICATE CONTROL REGISTER 4 WAS CLEARED
3117      :   T6LOAD CONTAINS ALL ZEROES TO INDICATE MODE REGISTER WAS CLEARED
3118
3119      :   TOMASK EQUALS 0 TO CHECK ALL CONTROL REGISTER 0 BITS
3120      :   T6MASK EQUALS 0 TO CHECK ALL CONTROL REGISTER 6 BITS
3121
3122
3123      : IMPLICIT OUTPUTS:
3124
3125
3126      : SUBORDINATE ROUTINES USED:
3127      :   LDRDT0 ROUTINE TO LOAD, READ AND COMPARE REGISTER 0
3128      :   LDRDT1 ROUTINE TO LOAD, READ AND COMPARE REGISTER 0 (USED FOR DEVICE TYPE)
3129      :   LDRDT2 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 2
3130      :   LDRDT4 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 4
3131      :   LDRDT6 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 6
3132
3133
3134      : FUNCTIONAL SIDE EFFECTS:
3135      :   TARGET EMULATOR SELECTED
3136      :   CONTROL REGISTER 0 LOW BYTE EQUALS 0 (GDAL 7:0)
3137      :   CONTROL REGISTER 2 EQUALS 0 (ADAL 15:0)
3138      :   CONTROL REGISTER 4 LOW BYTE EQUALS 0 (VDAL 15:0)
3139      :   CONTROL REGISTER 6 - HDAL 15:0 REGISTER EQUALS FOUR
3140      :   CONTROL REGISTER 6 - MODE REGISTER 15:0 EQUALS ZERO
3141
3142
3143      : CALLING SEQUENCE:
3144      :   JSR PC,INITTE
3145
3146      :--
3147
3148
```

```

3149 ;NOTE: ON A START OR RESTART COMMAND TO THE DIAGNOSTIC SUPERVISOR, A
3150 ; BUS RESET INSTRUCTION WILL BE ISSUED TO CLEAR ALL MODULES. THIS
3151 ; IS NEEDED TO CLEAR SIGNALS COMING INTO THE TARGET EMULATOR THAT
3152 ; MAY BE SET ON THE MEMORY SIMULATOR MODULE OR STATE ANALYZER MODULE.
3153
3154
3155
3156

```

```

3157 007436 INITMD::
3158 007436 INITMS::BGNSEG
3159 007436 104404 TRAP C$BSEG
3160

```

```

3161 ;THE FOLLOWING SECTION OF CODE WILL SELECT AND INITIALIZE THE MEMORY
3162 ;SIMULATOR MODULE. THE SIGNAL RST H WILL BE SET TO A ONE IN CONTROL
3163 ;REGISTER 0 TO PRESET THE RDV AND WRV FLIP-FLOPS. WHEN THE RDV AND
3164 ;WRV FLIP-FLOPS ARE PRESET, THE SIGNALS 'RDV H' AND 'WRV H' WILL BE
3165 ;READ AS ZEROES IN CONTROL REGISTER 0. ALL OTHER READ/WRITE BITS IN
3166 ;CONTROL REGISTER 0 WILL BE LOADED AND CHECKED FOR ZEROES.
3167

```

```

3168 007440 013737 002216 002234 MOV MSDEV,SLOAD ;GET USER DEFINED DEVICE NUMBER
3169 007446 005237 002234 INC SLOAD ;SET BIT TO SET RST H TO A ONE
3170 007452 005037 002240 CLR SOMASK ;CLEAR REGISTER 0 MASK WORD
3171 007456 013701 002204 MOV REG0,R1 ;GET CONTROL REGISTER 0 DEVICE ADDRESS
3172 007462 113761 002217 000001 MOVB MSDEV+1,1(R1) ;LOAD HIGH BYTE WITH DEVICE NUMBER
3173 007470 004737 010504 JSR PC,LDRDOS ;GO LOAD, READ AND CHECK REGISTER 0
3174 007474 001405 BEQ 1$ ;IF LOADED OK THEN CONTINUE
3175 007476 ERRDF 1,SOEROR ;MEM SIM REG 0 NOT EQUAL EXPECTED
3176 007476 104455 TRAP C$ERRDF
3177 007500 000001 .WORD 1
3178 007502 000000 .WORD 0
3179 007504 005304 .WORD SOEROR
3180 007506 CKLOOP
3181 007506 104406 TRAP C$CLP1
3182

```

```

3183 ;THE FOLLOWING SECTION WILL SET CONTROL REGISTER 0 BIT 15 TO A ONE.
3184 ;WHEN CONTROL REGISTER 0 BIT 15 IS SET TO A ONE, THE MODULES DEVICE
3185 ;TYPE WILL BE READBACK ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD
3186 ;OF THE MODULES DEVICE NUMBER. THE MEMORY SIMULATORS DEVICE TYPE SHOULD
3187 ;EQUAL ONE (400). THE SIGNAL RST H WILL BE LOADED AND CHECKED TO BE
3188 ;ZERO.
3189

```

```

3190 007510 013737 002216 002234 1$: MOV MSDEV,SLOAD ;GET USER DEFINED DEVICE NUMBER
3191 007516 052737 100000 002234 BIS #1DH,SLOAD ;SELECT DEVICE TYPE INSTEAD OF NUMBER
3192 007524 013737 002220 002236 MOV MSTYPE,SOGOOD ;GET DEVICE TYPE AND SAVE (400)
3193 007532 004737 010512 JSR PC,LDRDOS ;GO LOAD, READ AND CHECK REGISTER 0
3194 007536 001405 BEQ 2$ ;IF LOADED OK THEN CONTINUE
3195 007540 ERRDF 1,SOEROR ;DEVICE TYPE OR LOW BYTE NOT = EXPECTED
3196 007540 104455 TRAP C$ERRDF
3197 007542 000001 .WORD 1
3198 007544 000000 .WORD 0
3199 007546 005304 .WORD SOEROR
3200 007550 CKLOOP
3201 007550 104406 TRAP C$CLP1
3202

```

```

3203 ;SET CONTROL REGISTER 0 BIT 15 TO A ZERO AND CHECK THAT THE DEVICE
3204 ;NUMBER CAN BE READBACK AGAIN INSTEAD OF THE DEVICE TYPE.

```



```
3205
3206 007552 042737 100000 002234 2$: BIC #IDH,SOLOAD ;SETUP TO READBACK DEVICE NUMBER
3207 007560 004737 010504 JSR PC,LDRDSO ;GO LOAD, READ AND CHECK REGISTER 0
3208 007564 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
3209 007566 ERRDF 1,SOEROR ;DEVICE # OR LOW BYTE NOT = EXPECTED
3210 007566 104455 TRAP C$ERDF
3211 007570 000001 .WORD 1
3212 007572 000000 .WORD 0
3213 007574 005304 .WORD SOEROR
3214 007576 CKLOOP
3215 007576 104406 TRAP C$CLP1
3216
3217 ;SET THE SIGNALS MSEL1 H, MSEL2 H, MSAD17 H AND MSAD16 H TO ZEROES IN
3218 ;CONTROL REGISTER 2 AND CHECK THAT THESE SIGNALS ARE READBACK AS ZEROES.
3219 ;AS A RESULT OF THE SIGNAL MP H BEING A ZERO IN CONTROL REGISTER 0,
3220 ;CONTROL REGISTER 2 READ ONLY BITS ESR H, WREN H AND MEMBRK H WILL NOT BE
3221 ;CHECKED AT THIS POINT IN TIME BECAUSE THEY SHOULD BE TRI-STATE.
3222
3223 007600 005037 002244 002250 3$: CLR S2LOAD ;SETUP TO CLEAR R/W BITS
3224 007604 012737 177740 MOV #177740,S2MASK ;IGNORE READ ONLY AND UNUSED BITS
3225 007612 004737 010544 JSR PC,LDRDS2 ;GO LOAD, READ AND CHECK REGISTER 2
3226 007616 001405 BEQ 4$ ;IF LOADED OK THEN CONTINUE
3227 007620 ERRDF 2,S2EROR ;REGISTER 2 NOT EQUAL TO ZERO
3228 007620 104455 TRAP C$ERDF
3229 007622 000002 .WORD 2
3230 007624 000000 .WORD 0
3231 007626 005320 .WORD S2EROR
3232 007630 CKLOOP
3233 007630 104406 TRAP C$CLP1
3234
3235 ;CLEAR MSAD BITS 15:0 IN CONTROL REGISTER 4 AND CHECK THAT THESE BITS
3236 ;ARE CLEARED BY READING BACK CONTROL REGISTER 4.
3237
3238 007632 005037 002254 4$: CLR S4LOAD ;SETUP TO CLEAR ALL MSAD BITS (15:0)
3239 007636 004737 010604 JSR PC,LDRDS4 ;GO LOAD, READ AND CHECK REGISTER 4
3240 007642 001404 BEQ 5$ ;IF LOADED OK THEN CONTINUE
3241 007644 ERRDF 3,MSADRG,S4EROR ;CONTROL REGISTER 4 NOT EQUAL TO 0
3242 007644 104455 TRAP C$ERDF
3243 007646 000003 .WORD 3
3244 007650 002506 .WORD MSADRG
3245 007652 005334 .WORD S4EROR
3246 007654 012737 177760 002264 5$: MOV #177760,S6MASK ;SETUP REG 6 MASK WORD FOR FUTURE USE
3247 007662 ENDSEG
3248 007662 10000$: TRAP C$ESEG
3249 007662 104405
3250
3251 007664 INITED::BGNSEG
3252 007664 104404 TRAP C$BSEG
3253
3254 ;THE FOLLOWING SECTION OF CODE WILL SELECT AND INITIALIZE THE STATE
3255 ;ANALYZER MODULE. THE SIGNAL "CDALO H" WILL BE SET TO A ONE TO CLEAR
3256 ;THE TRACE RAM ADDRESS REGISTER, TO CLEAR THE TRACING AND SBL FLIP-FLOPS,
3257 ;AND TO LOAD THE EVENT COUNTERS FROM THE EVENT COUNTER REGISTERS. ALL
3258 ;OTHER READ/WRITE BITS WILL BE LOADED AND CHECKED FOR ZEROES.
3259
3260 007666 013737 002222 002272 MOV EDDEV,E0LOAD ;GET USER DEFINED DEVICE NUMBER
```

```
3261 007674 005237 002272      INC      EOLOAD      ;SET BIT CDALO H TO A ONE
3262 007700 013701 002204      MOV      REG0,R1     ;GET DEVICE'S REGISTER 0 ADDRESS
3263 007704 113761 002223 000001  MOVB     EDDEV+1,1(R1) ;LOAD HIGH BYTE WITH DEVICE NUMBER
3264 007712 004737 010676      JSR      PC,LDRDE0   ;GO LOAD, READ AND CHECK REGISTER 0
3265 007716 001405      BEQ      1$         ;IF LOADED OK THEN CONTINUE
3266 007720      ERRDF     5,CDALRG,E0EROR ;STATE ANALYZER REG 0 NOT = EXPECTED
3267 007720 104455      TRAP     C$ERDF
3268 007722 000005      .WORD    5
3269 007724 003006      .WORD    CDALRG
3270 007726 006144      .WORD    E0EROR
3271 007730      CKLOOP
3272 007730 104406      TRAP     C$CLP1
3273
3274      ;THE FOLLOWING SECTION WILL SET CONTROL REGISTER 0 BIT 15 TO A ONE.
3275      ;WHEN CDAL15 H IS SET TO A ONE, THE MODULES DEVICE TYPE WILL BE READ-
3276      ;BACK ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE
3277      ;NUMBER. THE STATE ANALYZERS DEVICE TYPE SHOULD EQUAL TWO (1000). THE
3278      ;SIGNAL "CDALO H" WILL BE LOADED AND CHECKED FOR ZEROES.
3279
3280 007732 013737 002222 002272 1$:  MOV      EDDEV,E0LOAD ;GET USER DEFINED DEVICE NUMBER
3281 007740 052737 100000 002272      BIS      #CDAL15,E0LOAD ;SELECT DEVICE TYPE TO BE READ
3282 007746 013737 002224 002274      MOV      EDTYPE,E0GOOD ;GET DEVICE TYPE AND SAVE (1000)
3283 007754 004737 010704      JSR      PC,LDRDOE   ;GO LOAD, READ AND CHECK REGISTER 0
3284 007760 001405      BEQ      2$         ;IF LOADED OK THEN CONTINUE
3285 007762      ERRDF     5,CDALRG,E0EROR ;DEVICE TYPE OR LOW BYTE NOT = EXPECTED
3286 007762 104455      TRAP     C$ERDF
3287 007764 000005      .WORD    5
3288 007766 003006      .WORD    CDALRG
3289 007770 006144      .WORD    E0EROR
3290 007772      CKLOOP
3291 007772 104406      TRAP     C$CLP1
3292
3293      ;SET CONTROL REGISTER 0 BIT 15 TO A ZERO AND CHECK THAT THE DEVICE
3294      ;NUMBER CAN BE READBACK AGAIN INSTEAD OF THE DEVICE TYPE.
3295
3296 007774 042737 100000 002272 2$:  BIC      #CDAL15,E0LOAD ;SELECT DEVICE NUMBER TO BE READ
3297 010002 004737 010676      JSR      PC,LDRDE0   ;GO LOAD, READ AND CHECK REGISTER 0
3298 010006 001405      BEQ      3$         ;IF LOADED OK THEN CONTINUE
3299 010010      ERRDF     5,CDALRG,E0EROR ;DEVICE # OR LOW BYTE NOT = EXPECTED
3300 010010 104455      TRAP     C$ERDF
3301 010012 000005      .WORD    5
3302 010014 003006      .WORD    CDALRG
3303 010016 006144      .WORD    E0EROR
3304 010020      CKLOOP
3305 010020 104406      TRAP     C$CLP1
3306
3307      ;LOAD, READ AND CHECK CONTROL REGISTER 2 WITH A DATA PATTERN OF ALL
3308      ;ZEROES. THE HIGH BYTE OF CONTROL REGISTER 2 IS NOT AVAILABLE,
3309      ;THEREFORE, ON A READ COMMAND TO CONTROL REGISTER 2, THE HIGH BYTE
3310      ;WILL BE IGNORED.
3311
3312 010022 005037 002300 3$:  CLR      E2LOAD      ;SETUP TO CLEAR ALL READ/WRITE BITS
3313 010026 004737 010730      JSR      PC,LDRDE2   ;GO LOAD, READ AND CHECK REGISTER 2
3314 010032 001404      BEQ      4$         ;IF LOADED OK THEN CONTINUE
3315 010034      ERRDF     6,PDALRG,E2EROR ;PDAL 7:0 REGISTER NOT EQUAL TO ZERO
3316 010034 104455      TRAP     C$ERDF
```



```

3317 010036 000006          .WORD 6
3318 010040 003032          .WORD PDALRG
3319 010042 006160          .WORD E2EROR
3320 010044 005037 002310 4$: CLR E4MASK ;SET REGISTER 4 MASK WORD TO ZERO
3321 010050 005037 002320 CLR E6MASK ;SET REGISTER 6 MASK WORD TO ZERO
3322 010054          ENDSEG
3323 010054          10001$:
3324 010054 104405          TRAP C$ESEG
3325
3326 010056          INITTE: :BGNSEG ;ROUTINE TO INIT TE MODULE
3327 010056 104404          TRAP C$BSEG
3328
3329          ;THE FOLLOWING SECTION OF CODE WILL SELECT AND INITIALIZE THE TARGET
3330          ;EMULATOR MODULE. THE READ/WRITE BITS WILL BE LOADED AND CHECKED
3331          ;FOR ZEROES. THE READ ONLY BITS, EXCEPT EDBRK H, WILL BE IGNORED
3332          ;AT THIS POINT IN TIME. THE SIGNAL 'EDBRK H' SHOULD BE READ AS A ZERO
3333          ;AS A RESULT OF THE SIGNAL 'CDAL1 H' BEING LOADED TO A ZERO IN CONTROL
3334          ;REGISTER ZERO OF THE STATE ANALYZER MODULE.
3335
3336 010060 013737 002226 002324 MOV TEDEV,TOLOAD ;GET USER DEFINED DEVICE NUMBER
3337 010066 012737 000340 002330 MOV #SSBRK!TOBRK!MEMBRK,TOMASK ;SETUP TO IGNORE READ ONLY BITS
3338 010074 013701 002204 MOV REG0,R1 ;GET DEVICE'S CONTROL REGISTER 0 ADDRESS
3339 010100 113761 002227 000001 MOVB TEDEV+1,1(R1) ;LOAD HIGH BYTE WITH THE DEVICE NUMBER
3340 010106 004737 011076 JSR PC,LDRD0 ;GO LOAD,READ AND COMPARE REG 0
3341 010112 001404 BEQ 1$ ;IF COMPARE WAS GOOD THEN CONT
3342 010114 ERRDF 9,GDALRG,TOEROR ;DEVICE # OR LB NOT = EXPECTED
3343 010114 104455 TRAP C$ERDF
3344 010116 000011 .WORD 9
3345 010120 003636 .WORD GDALRG
3346 010122 006664 .WORD TOEROR
3347
3348          ;THE FOLLOWING SECTION WILL SET CONTROL REGISTER 0 BIT 15 TO A ONE.
3349          ;WHEN GDAL15 H IS SET TO A ONE, THE MODULES DEVICE TYPE WILL BE READ-
3350          ;BACK ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE
3351          ;NUMBER. THE TARGET EMULATORS DEVICE TYPE SHOULD EQUAL ZERO (000000).
3352
3353 010124 052737 100000 002324 1$: BIS #GDAL15,TOLOAD ;SETUP TO READ DEVICE TYPE
3354 010132 013737 002230 002326 MOV TETYPE,TOGOOD ;SETUP EXPECTED DATA
3355 010140 004737 011104 JSR PC,LDRD0 ;LOAD, READ AND COMPARE REG 0
3356 010144 001405 BEQ 2$ ;IF EQUAL THEN DEVICE TYPE COMPARED
3357 010146 ERRDF 9,GDALRG,TOEROR ;DEVICE TYPE NOT EQUAL EXPECTED
3358 010146 104455 TRAP C$ERDF
3359 010150 000011 .WORD 9
3360 010152 003636 .WORD GDALRG
3361 010154 006664 .WORD TOEROR
3362 010156 CKLOOP
3363 010156 104406 TRAP C$CLP1
3364
3365          ;RESET THE SIGNAL GDAL15 H TO A 0 SO THAT THE DEVICE NUMBER WILL BE
3366          ;READ AGAIN. SET GDAL1 H AND GDAL0 H TO ONES AND GDAL2 H TO A ZERO.
3367          ;THIS IS DONE SO THAT THE HDAL REGISTER CAN BE SELECTED AND INITIALIZED.
3368
3369 010160 013737 002226 002324 2$: MOV TEDEV,TOLOAD ;GET USER DEFINED DEVICE NUMBER
3370 010166 052737 000003 002324 BIS #GDAL1!GDAL0,TOLOAD ;SET BITS TO SELECT THE HDAL REGISTER
3371 010174 004737 011076 JSR PC,LDRD0 ;GO LOAD, READ AND CHECK GDAL REGISTER
3372 010200 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE

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3373 010202          ERRDF  9,GDALRG,TOEROR      ;GDAL REGISTER NOT EQUAL TO EXPECTED
3374 010202 104455  TRAP    C$ERDF
3375 010204 000011  .WORD  9
3376 010206 003636  .WORD  GDALRG
3377 010210 006664  .WORD  TOEROR
3378 010212
3379 010212 104406  CKLOOP
3380 TRAP    C$CLP1
3381
3382 ;LOAD, READ AND CHECK THE HDAL REGISTER WITH A DATA PATTERN OF FOUR.
3383 ;HDAL2 H SET TO A ONE WILL ENABLE THE PROGRAM TO GENERATE AND CONTROL
3384 ;THE T-11 TIMING AND CONTROL SIGNALS INSTEAD OF THE T-11 GENERATING THEM.
3385 ;ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 1 AND 0 SET,
3386 ;PULSES WILL OCCUR ON THE SIGNALS WPT3 LB H AND WPT3 HB H. THESE
3387 ;PULSES WILL LOAD THE DATA INTO THE HDAL REGISTER. ON A READ COMMAND
3388 ;TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REGISTER
3389 ;VIA THE SIGNAL RPT3 L.
3390 010214 012737 000004 002346 3$: MOV    #HDAL2,T6LOAD      ;SETUP BIT TO BE LOADED
3391 010222 005037 002352          CLR    T6MASK           ;SETUP MASK WORK TO COMPARE ALL BITS
3392 010226 004737 011214          JSR    PC,LDRDT6        ;GO LOAD, READ AND CHECK HDAL REGISTER
3393 010232 001405          BEQ    4$              ;IF LOADED OK THEN CONTINUE
3394 010234          ERRDF  12,HDALRG,TO6ERR      ;HDAL REGISTER NOT EQUAL TO EXPECTED.
3395 010234 104455  TRAP    C$ERDF
3396 010236 000014  .WORD  12
3397 010240 003754  .WORD  HDALRG
3398 010242 006730  .WORD  TO6ERR
3399 010244          CKLOOP
3400 010244 104406  TRAP    C$CLP1
3401
3402 ;SELECT THE MODE REGISTER BY SETTING GDAL BIT 2 TO A ONE AND GDAL BITS
3403 ;1 AND 0 TO ZEROES. THIS IS DONE SO THAT THE MODE REGISTER CAN BE
3404 ;SELECTED AND CLEARED.
3405
3406 010246 013737 002226 002324 4$: MOV    TEDEV,TOLOAD      ;GET USER DEFINED DEVICE NUMBER
3407 010254 052737 000004 002324  BIS    #GDAL2,TOLOAD    ;GET BIT TO SELECT MODE REGISTER
3408 010262 004737 011076          JSR    PC,LDRDT0        ;GO LOAD, READ AND CHECK MODE REGISTER
3409 010266 001405          BEQ    5$              ;IF LOADED OK THEN CONTINUE
3410 010270          ERRDF  9,GDALRG,TOEROR      ;GDAL REGISTER NOT EQUAL EXPECTED
3411 010270 104455  TRAP    C$ERDF
3412 010272 000011  .WORD  9
3413 010274 003636  .WORD  GDALRG
3414 010276 006664  .WORD  TOEROR
3415 010300          CKLOOP
3416 010300 104406  TRAP    C$CLP1
3417
3418 ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES.
3419 ;ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BIT 2 SET TO A ONE
3420 ;AND GDAL BITS 1 AND 0 SET TO ZEROES, PULSES WILL OCCUR ON THE SIGNALS
3421 ;WPT4 LB H AND WPT4 HB H. THESE PULSES WILL LOAD THE DATA ON THE WRITE
3422 ;COMMAND INTO THE MODE REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6,
3423 ;DATA WILL BE READBACK FROM THE MODE REGISTER VIA THE SIGNAL RPT4 L.
3424
3425 010302 005037 002346          CLR    T6LOAD           ;SETUP TO LOAD ALL ZEROES INTO MODE REG
3426 010306 004737 011214          JSR    PC,LDRDT6        ;GO LOAD, READ AND CHECK MODE REGISTER
3427 010312 001405          BEQ    6$              ;IF LOADED OK THEN CONTINUE
3428 010314          ERRDF  12,MODREG,TO6ERR      ;MODE REGISTER NOT EQUAL EXPECTED

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3429 010314 104455 TRAP C$ERDF
3430 010316 000014 .WORD 12
3431 010320 004000 .WORD MODREG
3432 010322 006730 .WORD T06ERR
3433 010324 CKLOOP
3434 010324 104406 TRAP C$CLP1
3435
3436 ;SET AND CLEAR ADALO H IN CONTROL REGISTER 2 TO CLEAR THE SINGLE STEP
3437 ;BREAK FLIP-FLOP AND THE MEMORY SIMULATOR BREAK LATCH (MEMBRK) FLIP-FLOP.
3438 ;ALL OTHER BITS IN CONTROL REGISTER 2 WILL BE CLEARED. ADAL8 H ON A ZERO
3439 ;WILL INHIBIT THE TIMEOUT BREAK ONE SHOT OUTPUT TO BE READ IN ITS LOGICAL
3440 ;STATE. THE SIGNAL "TOBRK H" WILL BE ASSERTED LOW WHEN ADAL8 H IS A ZERO.
3441 ;AFTER SETTING AND CLEARING ADALO H IN CONTROL REGISTER 2, THE TEST WILL
3442 ;READ CONTROL REGISTER 0 AND CHECK THAT SINGLE STEP BREAK FLIP-FLOP,
3443 ;MEMORY SIMULATOR BREAK FLIP-FLOP, AND TIMEOUT BREAK SIGNALS ARE READ
3444 ;BACK AS ZEROES.
3445
3446 010326 012737 000001 002334 6$: MOV #ADALO,T2LOAD ;SETUP BIT TO BE LOADED TO 0 SSBK F/F
3447 010334 004737 011136 JSR PC,LDRDT2 ;GO LOAD, READ AND CHECK REGISTER 2
3448 010340 001405 BEQ 7$ ;IF LOADED OK THEN CONTINUE
3449 010342 ERRDF 10,ADALRG,T2EROR ;REGISTER 2 NOT EQUAL TO ADALO
3450 010342 104455 TRAP C$ERDF
3451 010344 000012 .WORD 10
3452 010346 003662 .WORD ADALRG
3453 010350 006700 .WORD T2EROR
3454 010352 CKLOOP
3455 010352 104406 TRAP C$CLP1
3456 010354 005037 002334 7$: CLR T2LOAD ;SETUP TO CLEAR ADALO
3457 010360 004737 011136 JSR PC,LDRDT2 ;GO LOAD, READ AND CHECK REGISTER 2
3458 010364 001405 BEQ 8$ ;IF LOADED OK THEN CONTINUE
3459 010366 ERRDF 10,ADALRG,T2EROR ;REGISTER 2 NOT EQUAL EXPECTED
3460 010366 104455 TRAP C$ERDF
3461 010370 000012 .WORD 10
3462 010372 003662 .WORD ADALRG
3463 010374 006700 .WORD T2EROR
3464 010376 CKLOOP
3465 010376 104406 TRAP C$CLP1
3466
3467 ;LOAD, READ AND CHECK CONTROL REGISTER 0. CHECK TIMEOUT BREAK SIGNAL
3468 ;TO BE ZERO AND CHECK MEMORY SIMULATOR BREAK AND SINGLE STEP BREAK FLIP-
3469 ;FLOPS TO BE CLEARED.
3470
3471 010400 005037 002330 8$: CLR TOMASK ;CLEAR MASK TO CHECK ALL BITS IN REG 0
3472 010404 105037 002324 CLRB TLOAD ;SETUP TO CLEAR THE LOWER BYTE
3473 010410 004737 011076 JSR PC,LDRDT0 ;GO LOAD, READ AND CHECK GDAL REGISTER
3474 010414 001405 BEQ 9$ ;IF ALL BITS CHECKED THEN CONTINUE
3475 010416 ERRDF 9,GDALRG,TOEROR ;REGISTER 0 NOT EQUAL TO DEVICE NUMBER
3476 010416 104455 TRAP C$ERDF
3477 010420 000011 .WORD 9
3478 010422 003636 .WORD GDALRG
3479 010424 006664 .WORD TOEROR
3480 010426 CKLOOP
3481 010426 104406 TRAP C$CLP1
3482
3483 ;SET AND CLEAR VDAL2 IN CONTROL REGISTER 4. WHEN VDAL2 IS SET TO A
3484 ;ONE, THE PAUSE STATE MACHINE FLIP-FLOPS WILL BE CLEARED. THESE F/F'S

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3485                                     ;ARE READBACK IN VDAL REGISTER BITS 15:8. THE REMAINING VDAL READ/
3486                                     ;WRITE BITS WILL BE LOADED AND CHECKED FOR ZEORES.
3487
3488 010430 012737 000004 002340 9$:  MOV    #VDAL2,T4LOAD      ;SETUP BIT TO BE LOADED
3489 010436 004737 011162           JSR    PC,LDRDT4        ;GO LOAD, READ AND CHECK VDAL REG
3490 010442 001405                   BEQ    10$              ;IF LOADED OK THEN CONTINUE
3491 010444                           ERRDF  11,VDALRG,T4EROR  ;VDAL REGISTER NOT EQUAL TO 2
3492 010444 104455                   TRAP  C$ERDF
3493 010446 000013                   .WORD 11
3494 010450 003706                   .WORD VDALRG
3495 010452 006714                   .WORD T4EROR
3496 010454                           CKLOOP
3497 010454 104406                   TRAP  C$CLP1
3498 010456 005037 002340 10$:  CLR    T4LOAD          ;SETUP TO CLEAR VDAL2
3499 010462 004737 011162           JSR    PC,LDRDT4        ;GO LOAD, READ AND CHECK VDAL REG
3500 010466 001404                   BEQ    11$              ;IF LOADED OK THEN CONTINUE
3501 010470                           ERRDF  11,VDALRG,T4EROR  ;VDAL REG NOT EQUAL TO 0
3502 010470 104455                   TRAP  C$ERDF
3503 010472 000013                   .WORD 11
3504 010474 003706                   .WORD VDALRG
3505 010476 006714                   .WORD T4EROR
3506 010500                           11$:  ENDSEG
3507 010500                           10002$:
3508 010500 104405                   TRAP  C$ESEG
3509
3510 010502 000207                   RTS    PC                ;RETURN BACK TO TEST
3511

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3512 :*****
3513 :
3514 :       CDS-11 MEMORY SIMULATOR ROUTINES TO LOAD CONTROL REGISTERS 0, 2, 4, + 6
3515 :
3516 :*****
3517
3518
3519 ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF MEMORY SIMULATOR CONTROL REGISTER
3520 ;0.  CONDITION CODES ARE SET ON EXIT AS A RESULT OF THE "CMP" INSTRUCTION.
3521
3522 010504 013737 002234 002236 LDRDS0: :MOV      S0LOAD,S0GOOD      ;PUT DATA LOADED INTO EXPECTED
3523 010512 013777 002234 171464 LDRDS0: :MOV      S0LOAD,@REG0      ;WRITE WORD TO REGISTER 0
3524 010520 017737 171460 002242 READS0: :MOV      @REG0,S0READ      ;READ REGISTER CONTENTS BACK
3525 010526 043737 002240 002242          BIC      S0MASK,S0READ      ;CLEAR UNWANTED BITS OF REG 0
3526 010534 023737 002236 002242          CMP      S0GOOD,S0READ      ;COMPARE EXPECTED WITH THAT READ
3527 010542 000207          RTS      PC              ;EXIT WITH CONDITION CODES SET
3528
3529 ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF MEMORY SIMULATOR CONTROL REGISTER
3530 ;2.  CONDITION CODES ARE SET ON EXIT AS A RESULT OF THE "CMP" INSTRUCTION.
3531
3532 010544 013737 002244 002246 LDRDS2: :MOV      S2LOAD,S2GOOD      ;PUT DATA TO BE LOADED INTO EXPECTED
3533 010552 013777 002244 171426 LDRDS2: :MOV      S2LOAD,@REG2      ;WRITE BITS INTO REGISTER 2
3534 010560 017737 171422 002252 READS2: :MOV      @REG2,S2READ      ;READ REGISTER 2 BACK AND SAVE
3535 010566 043737 002250 002252          BIC      S2MASK,S2READ      ;CLEAR UNWANTED BITS IN REG 2
3536 010574 023737 002246 002252          CMP      S2GOOD,S2READ      ;CHECK IF EXPECTED = ACTUAL READ
3537 010602 000207          RTS      PC              ;EXIT WITH CONDITION CODES SET
3538
3539 ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF MEMORY SIMULATOR CONTROL REGISTER
3540 ;4.  CONDITION CODES ARE SET ON EXIT AS A RESULT OF THE "CMP" INSTRUCTION.
3541
3542 010604 013777 002254 171376 LDRDS4: :MOV      S4LOAD,@REG4      ;WRITE WORD INTO REGISTER 4
3543 010612 017737 171372 002256 READS4: :MOV      @REG4,S4READ      ;READ WORD BACK FROM REG 4
3544 010620 023737 002254 002256          CMP      S4LOAD,S4READ      ;COMPARE LOADED WITH WORD READ
3545 010626 000207          RTS      PC              ;RETURN WITH CONDITON CODES SET
3546
3547 ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF MEMORY SIMULATOR CONTROL REGISTER
3548 ;6.  CONDITION CODES ARE SET ON EXIT AS A RESULT OF THE "CMP" INSTRUCTION.
3549
3550 010630 013737 002260 002262 LDRDS6: :MOV      S6LOAD,S6GOOD      ;COPY DATA TO BE LOADED
3551 010636 013777 002260 171346 LDRDS6: :MOV      S6LOAD,@REG6      ;WRITE WORD INTO REGISTER 6
3552 010644 017737 171342 002266 READS6: :MOV      @REG6,S6READ      ;READ CONTROL REGISTER 6 BACK
3553 010652 013737 002266 002270          MOV      S6READ,S6BAD      ;COPY DATA READ
3554 010660 043737 002264 002270          BIC      S6MASK,S6BAD      ;CLEAR UNWANTED BITS IN WORD READ
3555 010666 023737 002262 002270          CMP      S6GOOD,S6BAD      ;COMPARE EXPECTED WITH ACTUAL READ
3556 010674 000207          RTS      PC              ;EXIT WITH CONDITON CODES SET
3557
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3558 :*****
3559 :
3560 :       CDS-11 STATE ANALYZER ROUTINES USED TO LOAD CONTROL REGISTERS 0, 2, 4, + 6
3561 :
3562 :*****
3563 :
3564 :ROUTINE TO LOAD, READ AND COMPARE THE CONTENTS OF STATE ANALYZER CONTROL
3565 :REGISTER 0.  CONDITION CODES ARE SET ON EXIT AS A RESULT OF "CMP" INSTRUCTION.
3566 :
3567 010676 013737 002272 002274 LDRDE0::MOV      E0LOAD,E0GOOD      ;PUT DATA LOADED INTO EXPECTED
3568 010704 013777 002272 171272 LDRD0E::MOV      E0LOAD,@REG0      ;WRITE WORD INTO REGISTER 0
3569 010712 017737 171266 002276 READE0::MOV      @REG0,E0READ      ;READ REGISTER 0 CONIENTS BACK
3570 010720 023737 002274 002276      CMP      E0GOOD,E0READ      ;COMPARE EXPECTED WITH ACTUAL
3571 010726 000207      RTS      PC      ;EXIT WITH CONDITON CODES SET
3572 :
3573 :ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF STATE ANALYZER CONTROL REGISTER 2.
3574 :CONDITON CODES ARE SET ON EXIT AS A RESULT OF "CMP" INSTRUCTION.
3575 :
3576 010730 013777 002300 171250 LDRDE2::MOV      E2LOAD,@REG2      ;WRITE WORD INTO REGISTER 2
3577 010736 017737 171244 002302 READE2::MOV      @REG2,E2READ      ;READ CONTENTS OF REGISTER 2 BACK
3578 010744 042737 177400 002302      BIC      #177400,E2READ      ;CLEAR HIGH BYTE BITS
3579 010752 023737 002300 002302      CMP      E2LOAD,E2READ      ;COMPARE LOADED WITH ACTUAL READ
3580 010760 000207      RTS      PC      ;EXIT WITH CONDITON CODES SET
3581 :
3582 :ROUTINE TO LOAD, READ AND CHECK CONTENTS OF STATE ANALYZER CONTROL REGISTER 4.
3583 :CONDITON CODES WILL BE SET ON EXIT AS A RESULT OF "CMP" INSTRUCTION.
3584 :
3585 010762 013737 002304 002306 LDRDAR::MOV      E4LOAD,E4GOOD      ;COPY DATA TO BE LOADED
3586 010770 000337 002306      SWAB     E4GOOD      ;LOW TO HIGH BYTE TO SIMULATE READBACK
3587 010774 000403      BR      LDRD4E      ;GO LOAD READ + CHECK AND ARRAY
3588 :
3589 010776 013737 002304 002306 LDRDE4::MOV      E4LOAD,E4GOOD      ;COPY DATA LOADED TO EXPECTED DATA
3590 011004 013777 002304 171176 LDRD4E::MOV      E4LOAD,@REG4      ;WRITE WORD INTO REGISTER 4
3591 011012 017737 171172 002312 READE4::MOV      @REG4,E4READ      ;READ WORD BACK FROM REGISTER 4
3592 011020 013737 002312 002314      MOV      E4READ,E4BAD      ;COPY DATA READ
3593 011026 043737 002310 002314      BIC      E4MASK,E4BAD      ;CLEAR UNWANTED BITS
3594 011034 023737 002306 002314      CMP      E4GOOD,E4BAD      ;COMPARE WORD EXPECTED WITH ACTUAL
3595 011042 000207      RTS      PC      ;RETURN WITH CONDITION CODES SET
3596 :
3597 :ROUTINE TO LOAD, READ AND CHECK CONTENTS OF STATE ANALYZER CONTROL REGISTER 6.
3598 :CONDITON CODES WILL BE SET ON EXIT AS A RESULT OF "CMP" INSTRUCTION.
3599 :
3600 011044 013777 002316 171140 LDRDE6::MOV      E6LOAD,@REG6      ;WRITE WORD INTO REGISTER 6
3601 011052 017737 171134 002322 READE6::MOV      @REG6,E6READ      ;READ THE WORD BACK
3602 011060 043737 002320 002322      BIC      E6MASK,E6READ      ;CLEAR UNWANTED BITS
3603 011066 023737 002316 002322      CMP      E6LOAD,E6READ      ;COMPARE DATA LOADED WITH ACTUAL READ
3604 011074 000207      RTS      PC      ;EXIT WITH CONDITION CODES SET
3605 :

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3606 :*****
3607 :
3608 :       CDS-11 TARGET EMULATOR ROUTINES TO LOAD CONTROL REGISTERS 0, 2, 4, + 6
3609 :*****
3610 :
3611 :
3612 :ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF TARGET EMULATOR CONTROL REGISTER 0.
3613 :CONDITION CODES ARE SET ON EXIT AS RESULT OF THE "CMP" INSTRUCTION.
3614 :
3615 011076 013737 002324 002326 LDRDT0::MOV      T0LOAD,T0GOOD      ;PUT DATA LOADED INTO EXPECTED
3616 011104 013777 002324 171072 LDRDOT::MOV     T0LOAD,@REG0    ;WRITE WORD TO REGISTER 0
3617 011112 017737 171066 002332 READT0::MOV     @REG0,T0READ    ;READ REGISTER CONTENTS BACK
3618 011120 043737 002330 002332      BIC      TOMASK,T0READ    ;CLEAR OUT UNWANTED BITS
3619 011126 023737 002326 002332      CMP      T0GOOD,T0READ    ;COMPARE EXPECTED WITH THAT READ
3620 011134 000207      RTS      PC              ;EXIT WITH CONDITION CODES SET
3621 :
3622 :ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF TARGET EMULATOR CONTROL REGISTER 2.
3623 :CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION
3624 :
3625 011136 013777 002334 171042 LDRDT2::MOV     T2LOAD,@REG2    ;WRITE BITS INTO REGISTER 2
3626 011144 017737 171036 002336 READT2::MOV     @REG2,T2READ    ;READ REGISTER 2 BACK
3627 011152 023737 002334 002336      CMP      T2LOAD,T2READ    ;CHECK IF EXP EQUALS ACTUAL
3628 011160 000207      RTS      PC              ;EXIT WITH CONDITION CODES SET
3629 :
3630 :ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF TARGET EMULATOR CONTROL REGISTER 4.
3631 :CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION.
3632 :
3633 011162 013737 002340 002342 LDRDT4::MOV     T4LOAD,T4GOOD    ;SETUP EXPECTED DATA
3634 011170 013777 002340 171012 LDRD4T::MOV    T4LOAD,@REG4    ;WRITE WORD INTO REGISTER 4
3635 011176 017737 171006 002344 READT4::MOV     @REG4,T4READ    ;READ WORD BACK FROM REGISTER 4
3636 011204 023737 002342 002344      CMP      T4GOOD,T4READ    ;COMPARE WORD EXPECTED WITH READ
3637 011212 000207      RTS      PC              ;RETURN WITH CONDITION CODES SET
3638 :
3639 :ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF TARGET EMULATOR CONTROL REGISTER 6.
3640 :CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION.
3641 :
3642 011214 013777 002346 170770 LDRDT6::MOV     T6LOAD,@REG6    ;WRITE WORD INTO REGISTER 6
3643 011222 017737 170764 002350 READT6::MOV     @REG6,T6READ    ;READ THE WORD BACK
3644 011230 043737 002352 002350      BIC      T6MASK,T6READ    ;CLEAR OUT ANY UNWANTED BITS
3645 011236 023737 002346 002350      CMP      T6LOAD,T6READ    ;COMPARE DATA LOADED WITH DATA READ
3646 011244 000207      RTS      PC              ;EXIT WITH CONDITON CODES SET
3647 :

```

```

*****
:
: CDS-11 MEMORY SIMULATOR SUBROUTINES USED BY THE PROGRAM
:
*****

```

;ROUTINE TO SELECT THE MEMORY SIMULATOR MODULE

```

SLCTMS::MOV      R1,-(SP)          ;SAVE CPU REGISTER 0
          MOV      REG0,R1        ;GET DEVICE'S REGISTER 0 ADDRESS
          MOVVB   SOLOAD+1,1(R1)  ;LOAD USER DEFINED DEVICE NUMBER
          MOV      (SP)+,R1       ;RESTORE CPU REGISTER
          RTS      PC             ;RETURN BACK TO PROGRAM

```

;ROUTINE TO PULSE THE SIGNAL 'RST H'. A PULSE ON 'RST H' WILL PRESET
;THE RDV AND WRV FLIP-FLOP'S TO A ONE. WHEN THE FLIP-FLOP'S ARE SET TO
;A ONE, THE SIGNAL 'BRK L' WILL BE ASSERTED HIGH, THUS NO BREAK CONDITION
;IS GENERATED.

```

MSRSTH::BGNSEG
          TRAP    C$BSEG
          BIS     #RSTH,SOLOAD    ;SETUP BIT TO SET RST H TO HIGH STATE
          BIC     #RDVH!WRVH,SOMASK ;SETUP TO EXPECT RDV + WRV F/F'S A 0
          JSR    PC,LDRDSO       ;GO LOAD, READ AND CHECK REG 0
          BEQ    1$              ;IF LOADED OK THEN CONTINUE
          ERRDF  1,,SOEROR       ;MEM SIM CONTROL REG 0 NOT = EXPECTED
          TRAP    C$ERDF
          .WORD  1
          .WORD  0
          .WORD  SOEROR
          CKLOOP
          TRAP    C$CLP1
          BIC     #RSTH,SOLOAD    ;SETUP BIT TO SET RST H TO LOW STATE
          JSR    PC,LDRDSO       ;GO LOAD, READ AND CHECK REGISTER 0
          BEQ    2$              ;IF LOADED OK THEN CONTINUE
          ERRDF  1,,SOEROR       ;MEM SIM CONTROL REG 0 NOT = EXPECTED
          TRAP    C$ERDF
          .WORD  1
          .WORD  0
          .WORD  SOEROR
          2$:
          10003$:
          ENDSEG
          TRAP    C$ESEG
          RTS     PC             ;RETURN BACK TO TEST

```

;THE FOLLOWING ROUTINE WILL LOAD, READ AND CHECK THE MEMORY SIMULATOR
;MAP PROTECTION RAM. THE MAP PROTECTION RAM WILL BE SETUP TO ALLOW
;READS AND WRITES IN THE FIRST 16K WORDS OF MEMORY SIMULATOR RAM. THE
;FIRST 16K OF MEMORY WILL INCLUDE ADDRESSES 0 TO 077776. ALL ADDRESSES
;ABOVE 16K WILL BE SETUP TO CAUSE A READ OR WRITE VIOLATION IF ADDRESSED.
;ALL MEMORY WILL BE MAPPED TO THE MEMORY SIMULATOR MODULE.

```

MPRAM:: BGNSEG
        TRAP  C$BSEG

```

```

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3649
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3651
3652
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3654
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3656
3657 011246 010146
3658 011250 013701 002204
3659 011254 113761 002235 000001
3660 011262 012601
3661 011264 000207
3662
3663
3664
3665
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3667
3668 011266
3669 011266 104404
3670 011270 052737 000001 002234
3671 011276 042737 000060 002240
3672 011304 004737 010504
3673 011310 001405
3674 011312
3675 011312 104455
3676 011314 000001
3677 011316 000000
3678 011320 005304
3679 011322
3680 011322 104406
3681 011324 042737 000001 002234 1$:
3682 011332 004737 010504
3683 011336 001404
3684 011340
3685 011340 104455
3686 011342 000001
3687 011344 000000
3688 011346 005304
3689 011350
3690 011350
3691 011350 104405
3692 011352 000207
3693
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3700
3701 011354
3702 011354 104404
3703

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3760
3761 011452 012737 177760 002264 3$: MOV #177760,S6MASK ;SETUP TO CHECK ONLY LOWER 4 BITS
3762 011460 012737 000011 002260 MOV #MUTB!MPINH,S6LOAD ;SETUP DATA PATTERN OF 11
3763 011466 032737 000003 002244 BIT #MSAD17!MSAD16,S2LOAD ;CHECK IF ADDRESS ABOVE 16K WORDS
3764 011474 001006 BNE 4$ ;IF YES - LOAD R/W VIOLATION SETUP
3765 011476 005737 002254 TST S4LOAD ;CHECK IF OVER 16K WORDS
3766 011502 100403 BMI 4$ ;IF YES - LOAD R/W VIOLATION SETUP
3767 011504 052737 000006 002260 BIS #WREH!RDEH,S6LOAD ;SETUP TO ALLOW R/W TO 1ST 16K WORDS
3768 011512 004737 010630 4$: JSR PC,LDRDS6 ;LOAD,READ AND CHECK MAP PROTECT RAM
3769 011516 001405 BEQ 5$ ;IF LOADED OK THEN CONTINUE
3770 011520 ERRDF 4,MSGMP,S6ALLR ;MAP PROTECT RAM DATA ERROR
3771 011520 104455 TRAP C$ERDF
3772 011522 000004 .WORD 4
3773 011524 002601 .WORD MSGMP
3774 011526 005454 .WORD S6ALLR
3775 011530 CKLOOP
3776 011530 104406 TRAP C$CLP1
3777
3778 ;CHECK MAP PROTECT RAM DATA BITS 'MPIN H' AND 'WRE H' IN CONTROL
3779 ;REGISTER 2 AS 'ESR H' AND 'WREN H' RESPECTIVELY.
3780
3781 011532 042737 000140 002250 5$: BIC #ESRH!WRENH,S2MASK ;SETUP TO CHECK ESR H AND WREN H
3782 011540 052737 000140 002246 BIS #ESRH!WRENH,S2GOOD ;EXPECT ESR H AND WREN H TO BE ONES
3783 011546 032737 000006 002260 BIT #WREH!RDEH,S6LOAD ;CHECK IF RAM WAS W/R ENABLED
3784 011554 001003 BNE 6$ ;IF YES THEN GO READ CONTROL REGISTER 2
3785 011556 042737 000100 002246 BIC #WRENH,S2GOOD ;THIS ADDRESS WAS NOT WRITE ENABLED
3786 011564 004737 010560 6$: JSR PC,READS2 ;GO READ AND CHECK CONTROL REGISTER 2
3787 011570 001404 BEQ 7$ ;IF OK THEN CONTINUE
3788 011572 ERRDF 2,MSGMPL,S2ALLR ;REGISTER 2 NOT EQUAL EXPECTED
3789 011572 104455 TRAP C$ERDF
3790 011574 000002 .WORD 2
3791 011576 002456 .WORD MSGMPL
3792 011600 005440 .WORD S2ALLR
3793 011602 7$: ENDSEG
3794 011602 10005$: TRAP C$ESEG
3795 011602 104405
3796
3797 ;UPDATE THE ADDRESSES MSAD 15:0 AND MSAD 17:16
3798
3799 011604 062737 000400 002254 ADD #MSAD8,S4LOAD ;UPDATE MSAD BITS 15:8 BY ONE
3800 011612 001273 BNE 1$ ;IF NOT 0 THEN GO LOAD NEXT RAM LOCATION
3801 011614 005237 002244 INC S2LOAD ;UPDATE MSAD BITS 17:16 BY ONE
3802 011620 032737 000004 002244 BIT #MSEL0,S2LOAD ;CHECK IF RAM LOCATIONS DONE
3803 011626 001665 BEQ 1$ ;IF NOT THEN LOAD NEXT LOCATION
3804 011630 005337 002244 DEC S2LOAD ;RESET CONTROL REG 2 VALUE TO ACTUAL
3805 011634 ENDSEG
3806 011634 10004$: TRAP C$ESEG
3807 011634 104405
3808
3809 011636 000207 RTS PC ;RETURN BACK TO THE TEST
3810
3811 ;THE FOLLOWING ROUTINE WILL SELECT MODULE SELECT RAM 0 AND LOAD DATA
3812 ;PATTERNS 1, 2, 4, 10, 0, 0, 0, AND 0 INTO CONSECUTIVE LOCATIONS OF
3813 ;MODULE SELECT RAM 0 STARTING AT ADDRESS 0 OF MODULE SELECT RAM 0.
3814 ;MODULE SELECT RAM 0 WILL BE SETUP TO SELECT THE FIRST 16K WORDS OF
3815 ;MEMORY STARTING AT ADDRESS 0 AND ENDING WITH ADDRESS 0777760.

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3816
3817 011640 012737 000001 002260 MSRAM0::MOV #BIT0,S6LOAD ;SETUP STARTING PATTERN TO BE 1
3818 011646 005037 002254 CLR S4LOAD ;SET STARTING ADDRESS TO BE 0
3819
3820 011652 1$: BGNSEG
3821 011652 104404 TRAP C$BSEG
3822
3823 ;SET CONTROL REGISTER 2 BIT 'MSELO H' TO A ONE AND BITS 'MSEL1 H',
3824 ;'MSAD17 H' AND 'MSAD16 H' TO ZEROES. 'MSELO H' ON A ONE AND 'MSEL1 H'
3825 ;ON A ZERO WILL CAUSE THE SIGNAL 'SMDSO L' TO BE ASSERTED ON A WRITE OR
3826 ;READ COMMAND TO CONTROL REGISTER 6. 'SMDSO L' WILL SELECT MODULE
3827 ;SELECT RAM 0.
3828
3829 011654 012737 000004 002244 MOV #MSELO,S2LOAD ;SETUP BITS TO BE LOADED
3830 011662 012737 177540 002250 MOV #177540,S2MASK ;SETUP REGISTER 2 MASK WORD
3831 011670 004737 010544 JSR PC,LDRDS2 ;LOAD, READ AND CHECK CONTROL REG 2
3832 011674 001405 BEQ 2$ ;IF LOADED OK THEN CONTINUE
3833 011676 ERRDF 2,,S2EROR ;REGISTER 2 NOT EQUAL EXPECTED
3834 011676 104455 TRAP C$ERDF
3835 011700 000002 .WORD 2
3836 011702 000000 .WORD 0
3837 011704 005320 .WORD S2EROR
3838 011706 CKLOOP
3839 011706 104406 TRAP C$CLP1
3840
3841 ;LOAD THE ADDRESS OF MODULE SELECT RAM 0 TO BE TESTED INTO CONTROL
3842 ;REGISTER 4. CONTROL REGISTER 4 MSAD BITS 15:13 ARE USED TO SELECT
3843 ;THE ADDRESS OF MODULE SELECT RAM 0.
3844
3845 011710 004737 010604 2$: JSR PC,LDRDS4 ;LOAD, READ AND CHECK CONTROL REG 4
3846 011714 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
3847 011716 ERRDF 3,MSADRG,S4EROR ;MSAD 15:0 REGISTER ERROR
3848 011716 104455 TRAP C$ERDF
3849 011720 000003 .WORD 3
3850 011722 002506 .WORD MSADRG
3851 011724 005334 .WORD S4EROR
3852 011726 CKLOOP
3853 011726 104406 TRAP C$CLP1
3854
3855 ;WRITE THE DATA PATTERN INTO MODULE SELECT RAM 0 AND CHECK THAT THE
3856 ;PATTERN WAS LOADED CORRECTLY. THE FOLLOWING PATTERN WILL BE WRITTEN
3857 ;INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS
3858 ;0: 1, 2, 4, 10, 0, 0, 0, AND 0. THESE PATTERNS WILL CAUSE THE FIRST
3859 ;16K WORDS OF THE MEMORY SIMULATOR MEMORY TO BE SELECTED WHEN ADDRESSED.
3860
3861 011730 012737 177760 002264 3$: MOV #177760,S6MASK ;SETUP TO IGNORE UNWANTED BITS
3862 011736 004737 010630 JSR PC,LDRDS6 ;LOAD, READ AND CHECK MODULE SELECT RAM 0
3863 011742 001404 BEQ 4$ ;IF LOADED OK THEN CONTINUE
3864 011744 ERRDF 4,MSGMS0,S6ALLR ;DATA ERROR IN MODULE SELECT RAM 0
3865 011744 104455 TRAP C$ERDF
3866 011746 000004 .WORD 4
3867 011750 002637 .WORD MSGMS0
3868 011752 005454 .WORD S6ALLR
3869 011754 4$: ENDSEG
3870 011754 10006$:
3871 011754 104405 TRAP C$ESEG
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3872
3873 011756 006337 002260          ASL      S6LOAD          ;UPDATE MODULE SELECT RAM 0 DATA PATTERN
3874 011762 043737 002264 002260    BIC      S6MASK,S6LOAD   ;IF PATTERN WAS 20 THEN SET IT TO 0
3875 011770 062737 020000 002254    ADD      #MSAD13,S4LOAD  ;UPDATE ADDRESS TO MODULE SELECT RAM 0
3876 011776 001325                BNE      1$              ;IF NOT 0 LOAD NEXT ADDRESS OF RAM 0
3877 012000 162737 020000 002254    SUB      #MSAD13,S4LOAD  ;RESET WORD TO ACTUAL MSAD ADDRESS
3878 012006 000207                RTS       PC              ;RETURN BACK TO THE TEST
3879
3880                                ;THE FOLLOWING ROUTINE WILL SELECT MODULE SELECT RAM 1 AND LOAD THE
3881                                ;DATA PATTERNS 17, 0, 0 AND 0 INTO CONSECUTIVE LOCATIONS OF MODULE
3882                                ;SELECT RAM 1 STARTING AT ADDRESS 0.  MODULE SELECT RAM 1 WILL BE SETUP
3883                                ;TO SELECT THE FIRST 32K WORDS OF MEMORY SIMULATOR RAM STARTING AT
3884                                ;ADDRESS 0 AND ENDING WITH ADDRESS 177776.
3885
3886 012010 012737 000017 002260    MSRAM1:;MOV      #17,S6LOAD   ;SETUP STARTING DATA PATTERN
3887 012016 012737 000001 002262    MOV      #1,S6GOOD      ;WHEN A PATTERN OF ALL 1'S IS LOADED,
3888                                ;A PATTERN OF 1 WILL BE READBACK FROM RAM
3889 012024 012737 000014 002244    MOV      #MSEL1!MSEL0,S2LOAD ;SETUP STARTING ADDRESS (MSAD 17:16=0)
3890
3891 012032                1$:    BGNSEG
3892 012032 104404          TRAP     C$BSEG
3893
3894                                ;SET CONTROL REGISTER 2 BITS 'MSEL1 H' AND 'MSEL0 H' TO ONES AND 'MSAD17 H'
3895                                ;AND 'MSAD16 H' TO MODULE SELECT RAM 1'S ADDRESS TO BE TESTED.  'MSEL1 H'
3896                                ;AND 'MSEL0 H' SET TO ONES WILL CAUSE THE SIGNAL 'SMDS1 L' TO BE ASSERTED
3897                                ;ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.  THE SIGNAL 'SMDS1 L'
3898                                ;WILL SELECT MODULE SELECT RAM 1.
3899
3900 012034 012737 177540 002250    MOV      #177540,S2MASK  ;SETUP TO IGNORE UNWANTED BITS
3901 012042 004737 010544                JSR      PC,LDRDS2      ;LOAD, READ AND CHECK CONTROL REG 2
3902 012046 001405                BEQ      2$              ;IF LOADED OK THEN CONTINUE
3903 012050                ERRDF   2,S2EROR    ;REGISTER 2 NOT EQUAL EXPECTED
3904 012050 104455          TRAP     C$ERDF
3905 012052 000002                .WORD   2
3906 012054 000000                .WORD   0
3907 012056 005320                .WORD   S2EROR
3908 012060                CKLOOP
3909 012060 104406          TRAP     C$CLP1
3910

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3918 012062 012737 177760 002264 2$: MOV #177760,S6MASK ;SETUP TO IGNORE UNWANTED BITS
3919 012070 004737 010636 JSR PC,LDRD6S ;LOAD READ + CHECK MODULE SELECT RAM 1
3920 012074 001404 BEQ 3$ ;IF LOADED OK THEN CONTINUE
3921 012076 ERRDF 4,MSGMS1,S6ALLR ;DATA ERROR IN MODULE SELECT RAM 1
3922 012076 104455 TRAP C$ERDF
3923 012100 000004 .WORD 4
3924 012102 002701 .WORD MSGMS1
3925 012104 005454 .WORD S6ALLR
3926 012106 3$: ENDSEG
3927 012106 10007$:
3928 012106 104405 TRAP C$ESEG
3929
3930 0,2110 005037 002260 CLR S6LOAD ;SET DATA PATTERN TO 0 AFTER 1ST LOAD
3931 012114 005037 002262 CLR S6GOOD ;EXPECT PATTERN OF 0 TO BE READ
3932 012120 005237 002244 INC S2LOAD ;UPDATE MODULE SELECT RAM 1 ADDRESS BY 1
3933 012124 032737 000004 002244 BIT #MSELO,S2LOAD ;CHECK IF ALL ADDRESSES WRITTEN
3934 012132 001737 BEQ 1$ ;IF NOT THEN LOAD NEXT ADDRESS
3935 012134 005337 002244 DEC S2LOAD ;RESET ADDRESS TO ACTUAL ADDRESS LOADED
3936 012140 000207 RTS PC ;RETURN BACK TO THE TEST BEING EXECUTED

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012142 010146
012144 013701 002204
012150 113761 002273 000001
012156 012601
012160 000207

012162 012537 002300
012166
012166 104404
012170 004737 010730
012174 001404
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012176 104455
012200 000006
012202 003032
012204 006160
012206
012206 104405
012210 000205

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*****
CDS-11 STATE ANALYZER SUBROUTINES USED BY THE PROGRAM
*****

;ROUTINE TO SELECT THE STATE ANALYZER MODULE
SLCTED::MOV R1,-(SP) ;SAVE CPU REGISTER 0
MOV REG0,R1 ;GET DEVICE'S REGISTER 0 ADDRESS
MOVVB ELOAD+1,1(R1) ;LOAD USER DEFINED DEVICE NUMBER
MOV (SP)+,R1 ;RESTOR CPU REGISTER 0
RTS PC ;RETURN BACK TO PROGRAM

;THE FOLLOWING ROUTINE WILL LOAD THE STATE ANALYZER'S PDAL REGISTER
;WITH THE WORD FOLLOWING THE CALL TO THIS ROUTINE.
LDPDAL::MOV (R5)+,E2LOAD ;GET THE WORD TO BE LOADED
BGNSEG
TRAP C$BSEG
JSR PC,LDRDE2 ;LOAD, READ AND CHECK CONTROL REGISTER 2
BEQ 1$ ;IF LOADED OK THEN CONTINUE
ERRDF 6,PDALRG,E2EROR ;PDAL REGISTER NOT EQUAL WORD LOADED
TRAP C$ERDF
.WORD 6
.WORD PDALRG
.WORD E2EROR
1$:
10010$:
ENDSEG
TRAP C$ESEG
RTS R5 ;RETURN BACK TO THE TEST BEING PERFORMED

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012212 010146
012214 013701 002204
012220 113761 002325, 000001
012226 012601
012230 000207

012232
012232 104404
012234 111537 002324
012240 004737 011076
012244 001404
012246
012246 104455
012250 000011
012252 003636
012254 006664
012256
012256
012256 104405
012260 005725
012262 000205

: CDS-11 TARGET EMULATOR SUBROUTINES USED BY THE PROGRAM
:*****

:ROUTINE TO SELECT THE TARGET EMULATOR MODULE
SLCTTE::MOV R1,-(SP) ;SAVE CPU REGISTER 0
MOV REG0,R1 ;GET DEVICE'S REGISTER 0 ADDRESS
MOVB TOLOAD+1,1(R1) ;LOAD USER DEFINED DEVICE NUMBER
MOV (SP)+,R1 ;RESTOR CPU REGISTER 0
RTS PC ;RETURN BACK TO PROGRAM

:THE FOLLOWING ROUTINE WILL SELECT THE POINTER REGISTER SPECIFIED BY THE WORD
:FOLLOWING THE CALL TO THIS ROUTINE. THE REGISTER SELECTED WILL NOT BE ACCESSED
:UNTIL A WRITE OR READ COMMAND IS ISSUED TO TARGET EMULATOR CONTROL REGISTER 6.
:THE EXTENDED REGISTER WILL BE SELECTED BY GDAL BITS 2:0 IN TARGET EMULATOR
:CONTROL REGISTER 0. THE REGISTERS SELECTED BY GDAL BITS 2:0 ARE AS FOLLOWS:
: ADDRES - GDAL 2:0 = 0 - WRITE DIAGNOSTIC ADDRESS REGISTER (WPT0)
: READ ADDRESS BUS (RPT0)
: FJADR - GDAL 2:0 = 1 - WRITE NEW FORCE JUMP ADDRESS REGISTER (WPT1)
: READ FORCE JUMP ADDRESS READBACK REGISTER (RPT1)
: FDAL - GDAL 2:0 = 2 - WRITE FDAL AND EOAI REGISTERS (WPT2)
: READ FDAL/EOAI REGISTERS OR FDAL/CTL REGISTERS (RPT2)
: HDAL - GDAL 2:0 = 3 - WRITE/READ HDAL REGISTER (WPT3/RPT3)
: MODE - GDAL 2:0 = 4 - WRITE/READ MODE REGISTER (WPT4/RPT4)
: TARMOD - GDAL 2:0 = 5 - READ TARGET MODE REGISTER (RPT5)
: EIDAL - GDAL 2:0 = 6 - READ EIDAL BUS (RPT6)
: EODAL - GDAL 2:0 = 7 - READ EODAL BUS (RPT7)
:THE ROUTINE IS CALLED IN THE FOLLOWING WAY WITH THE REGISTER TO BE SELECTED IN
:THE LOCATION AFTER THE CALL

: JSR R5,SELTER ;CALL TO THIS ROUTINE
: .WORD ADDRES ;WORD TO SELECT THE EXTENDED REGISTER

SELTER::BGNSEG
TRAP C\$BSEG
MOVB (R5),TOLOAD ;GET THE REGISTER BITS TO BE SELECTED
JSR PC,LDRDTC ;GO LOAD, READ AND CHECK GDAL REGISTER
BEQ 1\$;IF LOADED OK THEN CONTINUE
ERRDF 9,GDALRG,TOEROR ;GDAL REGISTER NOT EQUAL EXPECTED
TRAP C\$ERDF
.WORD 9
.WORD GDALRG
.WORD TOEROR
1\$:
ENDSEG
10011\$:
TRAP C\$ESEG
TST (R5)+ ;UPDATE RETURN POINTER TO PROGRAM
RTS R5 ;RETURN BACK TO THE TEST

:THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL12 IN THE HDAL REGISTER. HDAL12
:BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNALS "XRAS L" AND
:"XRAS H". HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL
:THE T-11 TIMING AND CONTROL SIGNALS.

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4026
4027 012264 004737 012276      XCRAS:: JSR      PC,XCRASH      ;GO SET XCRAS H (HIGH) AND XCRAS L (LOW)
4028 012270 004737 012330      JSR      PC,XCRASL     ;GO SET XCRAS H (LOW) AND XCRAS L (HIGH)
4029 012274 000207              RTS      PC              ;RETURN BACK TO TEST
4030
4031 ;THE FOLLOWING ROUTINE WILL SET HDAL12 H AND HDAL2 H TO ONES. HDAL2 H ON A ONE
4032 ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
4033 ;HDAL12 H ON A ONE WILL CAUSE THE SIGNAL XCRAS H TO BE ASSERTED HIGH AND THE
4034 ;SIGNAL XCRAS L TO BE ASSERTED LOW
4035
4036 012276      XCRASH:: BGNSEG
4037 012276 104404      TRAP     C$BSEG
4038 012300 052737 010004 002346  BIS      #HDAL12!HDAL2,T6LOAD ;SETUP BIT TO BE LOADED
4039 012306 004737 011214      JSR      PC,LDRDT6     ;GO LOAD, READ AND CHECK HDAL REGISTER
4040 012312 001404      BEQ     1$            ;IF LOADED OK THEN CONTINUE
4041 012314      ERRDF    12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
4042 012314 104455      TRAP     C$ERDF
4043 012316 000014      .WORD   12
4044 012320 003754      .WORD   HDALRG
4045 012322 006730      .WORD   T06ERR
4046 012324      1$:      ENDSEG
4047 012324      10012$:
4048 012324 104405      TRAP     C$ESEG
4049 012326 000207      RTS      PC              ;RETURN BACK TO TEST
4050
4051 ;THE FOLLOWING ROUTINE WILL SET HDAL12 H TO A ZERO AND HDAL2 H TO A ONE.
4052 ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND
4053 ;CONTROL SIGNALS. HDAL12 H ON A ZERO WILL CAUSE THE SIGNAL XCRAS H TO BE
4054 ;ASSERTED LOW AND THE SIGNAL XCRAS L TO BE ASSERTED HIGH.
4055
4056 012330      XCRASL:: BGNSEG
4057 012330 104404      TRAP     C$BSEG
4058 012332 052737 000004 002346  BIS      #HDAL2,T6LOAD     ;SETUP DIAGNOSTIC CONTROL BIT
4059 012340 042737 010000 002346  PIC      #HDAL12,T6LOAD   ;SETUP BIT TO BE CLEARED
4060 012346 004737 011214      JSR      PC,LDRDT6     ;GO LOAD, READ AND CHECK HDAL REGISTER
4061 012352 001404      BEQ     1$            ;IF LOADED OK THEN CONTINUE
4062 012354      ERRDF    12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
4063 012354 104455      TRAP     C$ERDF
4064 012356 000014      .WORD   12
4065 012360 003754      .WORD   HDALRG
4066 012362 006730      .WORD   T06ERR
4067 012364      1$:      ENDSEG
4068 012364      10013$:
4069 012364 104405      TRAP     C$ESEG
4070 012366 000207      RTS      PC              ;RETURN BACK TO TEST
4071
4072 ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL13 IN THE HDAL REGISTER. HDAL13
4073 ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNALS "XCAS L" AND
4074 ;"XCAS H". HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL
4075 ;THE T-11 TIMING AND CONTROL SIGNALS SUCH AS ABOVE.
4076
4077 012370 004737 012402      XCRAS:: JSR      PC,XCRASH      ;GO SET XCRAS H (HIGH) AND XCRAS L (LOW)
4078 012374 004737 012434      JSR      PC,XCRASL     ;GO SET XCRAS H (LOW) AND XCRAS L (HIGH)
4079 012400 000207      RTS      PC
4080
4081 ;THE FOLLOWING ROUTINE WILL SET HDAL13 H AND HDAL2 H TO ONES. HDAL2 H ON A ONE
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4082 ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS. HDAL13 H
 4083 ;ON A ONE WILL CAUSE THE SIGNAL XCAS H TO BE ASSERTED HIGH AND THE SIGNAL XCAS L
 4084 ;TO BE ASSERTED LOW.

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4085
4086 012402          XCASH:: BGNSEG
4087 012402 104404   TRAP      C$BSEG
4088 012404 052737 020004 002346  BIS      #HDAL13!HDAL2,T6LOAD ;SETUP BITS TO BE LOADED
4089 012412 004737 011214          JSR      PC,LDRDT6 ;GO LOAD, READ AND CHECK HDAL REGISTER
4090 012416 001404          BEQ      1$ ;IF LOADED OK THEN CONTINUE
4091 012420          ERRDF    12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
4092 012420 104455   TRAP      C$ERDF
4093 012422 000014   .WORD    12
4094 012424 003754   .WORD    HDALRG
4095 012426 006730   .WORD    T06ERR
4096 012430          1$:      ENDSEG
4097 012430          10014$:
4098 012430 104405   TRAP      C$ESEG
4099 012432 000207   RTS      PC
  
```

4100 ;THE FOLLOWING ROUTINE WILL SET HDAL13 H TO A ZERO AND HDAL2 H TO A ONE.
 4101 ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND
 4102 ;CONTROL SIGNALS. HDAL13 H ON A ZERO WILL CAUSE THE SIGNAL XCAS H TO BE
 4103 ;ASSERTED LOW AND THE SIGNAL XCAS L TO BE ASSERTED HIGH.

```

4104
4105
4106 012434          XCASL:: BGNSEG
4107 012434 104404   TRAP      C$BSEG
4108 012436 052737 000004 002346  BIS      #BIT2,T6LOAD ;SETUP DIAGNOSTIC CONTROL BIT
4109 012444 042737 020000 002346  BIC      #HDAL13,T6LOAD ;SETUP BIT TO BE CLEARED
4110 012452 004737 011214          JSR      PC,LDRDT6 ;GO LOAD, READ AND CHECK HDAL REGISTER
4111 012456 001404          BEQ      1$ ;IF LOADED OK THEN CONTINUE
4112 012460          ERRDF    12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
4113 012460 104455   TRAP      C$ERDF
4114 012462 000014   .WORD    12
4115 012464 003754   .WORD    HDALRG
4116 012466 006730   .WORD    T06ERR
4117 012470          1$:      ENDSEG
4118 012470          10015$:
4119 012470 104405   TRAP      C$ESEG
4120 012472 000207   RTS      PC ;RETURN BACK TO TEST
  
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4121 ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL15 IN THE HDAL REGISTER. HDAL15
 4122 ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNAL "XPI H".
 4123 ;HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL THE T-11
 4124 ;TIMING AND CONTROL SIGNALS SUCH AS ABOVE.

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4125
4126
4127 012474 004737 012506  XPI::  JSR      PC,XPIH ;GO SET PPI L AND XPI L TO THE LOW STATE
4128 012500 004737 012540  JSR      PC,XPIL ;GO SET PPI L AND XPI L TO HIGH STATE
4129 012504 000207          RTS      PC ;RETURN BACK TO TEST
  
```

4130 ;THE FOLLOWING ROUTINE WILL SET HDAL15 H AND HDAL2 H TO ONES. HDAL2 H ON A ONE
 4131 ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS. HDAL15 H
 4132 ;ON A ONE WILL ASSERT THE SIGNALS PPI L AND XPI L TO THE LOW STATE.

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4133
4134
4135 012506          XPIH:: BGNSEG
4136 012506 104404   TRAP      C$BSEG
4137 012510 052737 100004 002346  BIS      #HDAL15!HDAL2,T6LOAD ;SETUP BITS TO BE LOADED
  
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GLOBAL SUBROUTINES SECTION

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4138 012516 004737 011214      JSR    PC,LDRDT6      ;GO LOAD, READ AND CHECK HDAL REGISTER
4139 012522 001404              BEQ    1$             ;IF LOADED OK THEN CONTINUE
4140 012524              ERRDF  12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
4141 012524 104455              TRAP  C$ERDF
4142 012526 000014              .WORD 12
4143 012530 003754              .WORD HDALRG
4144 012532 006730              .WORD T06ERR
4145 012534              1$: ENDSEG
4146 012534              10016$:
4147 012534 104405              TRAP  C$ESEG
4148 012536 000207              RTS    PC             ;RETURN BACK TO TEST

```

;THE FOLLOWING ROUTINE WILL SET HDAL15 H TO A ZERO AND HDAL2 H TO A ONE. HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS. HDAL15 H ON A ZERO WILL CAUSE THE SIGNALS PPI L AND XPI L TO BE ASSERTED HIGH.

```

4154 012540              XPIL:: BGNSEG
4155 012540 104404              TRAP  C$BSEG
4156 012542 052737 000004 002346      BIS   #HDAL2,T6LOAD ;SETUP DIAGNOSTIC CONTROL BIT
4157 012550 042737 100000 002346      BIC   #HDAL15,T6LOAD ;SETUP BIT TO BE CLEARED
4158 012556 004737 011214              JSR   PC,LDRDT6      ;GO LOAD, READ AND CHECK HDAL REGISTER
4159 012562 001404              BEQ   1$             ;IF LOADED OK THEN CONTINUE
4160 012564              ERRDF  12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
4161 012564 104455              TRAP  C$ERDF
4162 012566 000014              .WORD 12
4163 012570 003754              .WORD HDALRG
4164 012572 006730              .WORD T06ERR
4165 012574              1$: ENDSEG
4166 012574              10017$:
4167 012574 104405              TRAP  C$ESEG
4168 012576 000207              RTS    PC             ;RETURN BACK TO TEST

```

;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL7 IN THE HDAL REGISTER. HDAL7 BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNAL XBCLR H + PBCLR H. HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS SUCH AS ABOVE.

```

4175 012600 004737 012612      XBCLR:: JSR    PC,XBCLRH ;SET XBCLR H AND PBCLR H TO HIGH STATE
4176 012604 004737 012644      JSR    PC,XBCLR L     ;SET XBCLR H AND PBCLR H TO LOW STATE
4177 012610 000207              RTS    PC             ;RETURN BACK TO TEST

```

;THE FOLLOWING ROUTINE WILL SET HDAL7 H AND HDAL2 H TO ONES. HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS. HDAL7 H ON A ONE WILL ASSERT THE SIGNALS XBCLR H AND PBCLR H TO THE HIGH STATE

```

4183 012612              XBCLRH::BGNSEG
4184 012612 104404              TRAP  C$BSEG
4185 012614 052737 000204 002346      BIS   #HDAL7!HDAL2,T6LOAD ;SETUP BITS TO BE LOADED
4186 012622 004737 011214              JSR   PC,LDRDT6      ;GO LOAD, READ AND CHECK HDAL REGISTER
4187 012626 001404              BEQ   1$             ;IF LOADED OK THEN CONTINUE
4188 012630              ERRDF  12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
4189 012630 104455              TRAP  C$ERDF
4190 012632 000014              .WORD 12
4191 012634 003754              .WORD HDALRG
4192 012636 006730              .WORD T06ERR
4193 012640              1$: ENDSEG

```



```

4194 012640 10020$:
4195 012640 104405 TRAP C$ESEG
4196 012642 000207 RTS PC ;RETURN BACK TO TEST
4197
4198 ;THE FOLLOWING ROUTINE WILL SET HDAL7 H TO A ZERO AND HDAL2 H TO A ONE. HDAL2 H
4199 ;ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
4200 ;HDAL7 H ON A ZERO WILL CAUSE THE SIGNALS XBCLR H AND PBCLR H TO BE ASSERTED LOW
4201
4202 012644 XBCLRL: :BGNSEG
4203 012644 104404 TRAP C$BSEG
4204 012646 052737 000004 002346 BIS #VDAL2,T4LOAD ;SETUP DIAGNOSTIC CONTROL BIT
4205 012654 042737 000200 002346 BIC #VDAL7,T6LOAD ;SETUP BIT TO BE CLEARED
4206 012662 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK HDAL REGISTER
4207 012666 001404 BEQ 1$ ;IF LOADED OK THEN CONTINUE
4208 012670 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
4209 012670 104455 TRAP C$ERDF
4210 012672 000014 .WORD 12
4211 012674 003754 .WORD HDALRG
4212 012676 006730 .WORD T06ERR
4213 012700 1$: ENDSEG
4214 012700 10021$:
4215 012700 104405 TRAP C$ESEG
4216 012702 000207 RTS PC ;RETURN BACK TO TEST
4217
4218 ;THE FOLLOWING ROUTINE WILL SET AND CLEAR VDAL2 H IN CONTROL REGISTER 4. VDAL2 H
4219 ;ON A ONE WILL CLEAR THE FOLLOWING FLIP-FLOPS:
4220 : PAUSE STATE WORKING PSM H 0
4221 : PAUSE STATE SYNC EPSF H 0
4222 : 16 BIT ADDRESS EPFN H 0
4223 : 8 BIT INSTRUCTION HB EP8F H 0
4224 : 8 BIT ADDRESS LB EP8G H 0
4225 : 8 BIT ADDRESS HB EP8N H 0
4226 : TAKE NEW F.J. ADDRESS TNFI H 0
4227 : GET NEW ADDRESS FLIP-FLOP OUT NEW H
4228 : PAUSE MODE FLIP-FLOP PAUSE L 0
4229 : REFRESH FLIP-FLOP REFR H 0
4230 : FETCT LATCH FLIP-FLOP EDFET H 0
4231 ;SETTING AND CLEARING VDAL2 H WILL ALSO CLOCK THE TAI AND TDAL BUSES INTO THE
4232 ;DIAGNOSTIC LATCHES.
4233
4234 012704 CLRPSM: :BGNSEG
4235 012704 104404 TRAP C$BSEG
4236 012706 052737 000004 002340 BIS #VDAL2,T4LOAD ;SETUP BIT TO SET VDAL2 H TO A ONE
4237 012714 004737 011162 JSR PC,LDRDT4 ;GO LOAD, READ AND CHECK VDAL REGISTER
4238 012720 001405 BEQ 1$ ;IF ALL OTHER BITS CLEARED THEN CONT
4239 012722 ERRDF 11,VDALRG,T4EROR ;VDAL REG OR PAUSE STATE MACHINE ERROR
4240 012722 104455 TRAP C$ERDF
4241 012724 000013 .WORD 11
4242 012726 003706 .WORD VDALRG
4243 012730 006714 .WORD T4EROR
4244 012732 CKLOOP
4245 012732 104406 TRAP C$CLP1
4246 012734 042737 000004 002340 1$: BIC #VDAL2,T4LOAD ;SETUP TO CLEAR VDAL2 H
4247 012742 004737 011162 JSR PC,LDRDT4 ;GO LOAD, READ AND CHECK VDAL REGISTER
4248 012746 001404 BEQ 2$ ;IF LOADED OK THEN CONTINUE
4249 012750 ERRDF 11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR

```

```

4250 012750 104455          TRAP  C$ERDF
4251 012752 000013          .WORD 11
4252 012754 003706          .WORD VDALRG
4253 012756 006714          .WORD T4EROR
4254 012760                2$:  ENDSEG
4255 012760                10022$:
4256 012760 104405          TRAP  C$ESEG
4257 012762 000207          RTS   PC                ;RETURN BACK TO TEST
4258
4259                        ;THE FOLLOWING ROUTINE WILL SET ADALO H TO A ONE AND THEN ZERO. ADALO H BEING
4260                        ;SET AND CLEARED WILL CAUSE A PULSE ON THE SIGNAL 'BRKRES L'. THE SIGNAL
4261                        ;'BRKRES L' WILL CLEAR THE SINGLE STEP BREAK FLIP-FLOP AND INTERRUPT RELATED
4262                        ;LOGIC.
4263
4264 012764                BRKRES::BGNSEG
4265 012764 104404          TRAP  C$BSEG
4266 012766 052737 000001 002334 BIC   #ADALO,T2LOAD      ;SETUP BIT TO BE LOADED
4267 012774 004737 011136          JSR   PC,LDRDT2          ;GO LOAD, READ AND CHECK ADAL REGISTER
4268 013000 001405          BEQ   1$                ;IF LOADED OK THEN CONTINUE
4269 013002                ERRDF  10,ADALRG,T2EROR          ;ADAL REGISTER NOT EQUAL EXPECTED
4270 013002 104455          TRAP  C$ERDF
4271 013004 000012          .WORD 10
4272 013006 003662          .WORD ADALRG
4273 013010 006700          .WORD T2EROR
4274 013012                CKLOOP
4275 013012 104406          TRAP  C$CLP1
4276 013014 042737 000001 002334 1$: BIC   #ADALO,T2LOAD      ;SETUP BIT TO BE CLEARED
4277 013022 004737 011136          JSR   PC,LDRDT2          ;GO LOAD, READ AND CHECK ADAL REGISTER
4278 013026 001404          BEQ   2$                ;IF LOADED OK THEN CONTINUE
4279 013030                ERRDF  10,ADALRG,T2EROR          ;ADAL REGISTER NOT EQUAL EXPECTED
4280 013030 104455          TRAP  C$ERDF
4281 013032 000012          .WORD 10
4282 013034 003662          .WORD ADALRG
4283 013036 006700          .WORD T2EROR
4284 013040                2$:  ENDSEG
4285 013040                10023$:
4286 013040 104405          TRAP  C$ESEG
4287 013042 000207          RTS   PC                ;RETRUN BACK TO TEST
4288
4289                        ;TARGET EMULATOR INTERRUPT SERVICE ROUTINE
4290
4291 013044                BGNSRV  INTSRV
4292 013044                INTSRV::
4293 013044 017737 167134 002332 MOV   @REG0,T0READ      ;READ GDAL REGISTER AND SAVE
4294 013052 012702 177777          MOV   #-1,R2           ;SET SOFTWARE INTERRUPT FLAG
4295 013056                ENDSRV  #PRI07
4296 013056                L10025:
4297 013056 142766 000340 000002 BICB  #340,2(SP)
4298 013064 152766 000340 000002 BISB  #PRI07,2(SP)
4299 013072 000002          RTI
4300
4301 013074                ENDMOD
4302

```



```
4303 .TITLE MISCELLANEOUS SECTIONS
4304 .SBTTL REPORT CODING SECTION
4305
4306 013074 BGNMOD
4307
4308 :++
4309 : THE REPORT CODING SECTION CONTAINS THE
4310 : 'PRINTS' CALLS THAT GENERATE STATISTICAL REPORTS.
4311 :--
4312
4313 013074 BGNRPT
4314 013074 L$RPT::
4315
4316
4317 013074 EXIT RPT
4318 013074 000167 .WORD JSJMP
4319 013076 000000 .WORD L10026-2-.
4320
4321
4322 .EVEN
4323
4324 013100 ENDRPT
4325 013100 L10026:
4326 013100 104425 TRAP C$RPT
4327
4328 .SBTTL PROTECTION TABLE
4329
4330 :++
4331 : THIS TABLE IS USED BY THE RUNTIME SERVICES
4332 : TO PROTECT THE LOAD MEDIA.
4333 :--
4334
4335 013102 BGNPROT
4336 013102 L$PROT::
4337
4338 013102 177777 -1 ;OFFSET INTO P-TABLE FOR CSR ADDRESS
4339 013104 177777 -1 ;OFFSET INTO P-TABLE FOR MASSBUS ADDRESS
4340 013106 177777 -1 ;OFFSET INTO P-TABLE FOR DRIVE NUMBER
4341
4342 013110 ENDPROT
4343
```

.SBTTL INITIALIZE SECTION

```

:++
: THE INITIALIZE SECTION CONTAINS THE CODING THAT IS PERFORMED
: AT THE BEGINNING OF EACH PASS.
:--
  
```

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4344
4345
4346
4347
4348
4349
4350
4351 013110
4352 013110
4353 013110
4354 013110 012700 000040
4355 013114 104447
4356 013116
4357 013116 103410
4358 013120
4359 013120 012700 000037
4360 013124 104447
4361 013126
4362 013126 103404
4363 013130
4364 013130 012700 000034
4365 013134 104447
4366 013136
4367 013136 103014
4368 013140
4369 013140 104433
4370 013142
4371 013142 012746 000002
4372 013146 012746 000102
4373 013152 012746 000100
4374 013156 012746 000003
4375 013162 104437
4376 013164 062706 000010
4377 013170
4378 013170 012700 000035
4379 013174 104447
4380 013176
4381 013176 103003
4382 013200 012737 177777 002232
4383 013206
4384 013206 012700 000036
4385 013212 104447
4386 013214
4387 013214 103444
4388 013216 005237 002232
4389 013222
4390 013222 013700 002232
4391 013226 104442
4392 013230 010005
4393 013232
4394 013232 103371
4395 013234 012701 002204
4396 013240 005002
4397 013242 011511
4398 013244 060221
4399 013246 005202
  
```

```

      BGNINIT
L$INIT::
      READEF #EF.START          ;SEE IF A START COMMAND
      MOV    #EF.START,R0
      TRAP  C$REFG
      BCOMPLETE 1$           ;BRANCH IF START COMMAND
      BCS   1$
      READEF #EF.RESTART       ;SEE IF A RESTART COMMAND
      MOV    #EF.RESTART,R0
      TRAP  C$REFG
      BCOMPLETE 1$           ;BRANCH IF RESTART
      BCS   1$
      READEF #EF.PWR           ;SEE IF RECOVERING FROM A POWER FAIL
      MOV    #EF.PWR,R0
      TRAP  C$REFG
      BNCOMPLETE 2$          ;IF NOT CHECK IN CONTINUE
      BCC   2$
1$:    BRESET                  ;ISSUE A BUS RESET
      TRAP  C$RESET
      SETVEC #100,#102,#RTI   ;SETUP CLOCK VECTOR TO DO A RETURN
      MOV   #RTI,-(SP)
      MOV   #102,-(SP)
      MOV   #100,-(SP)
      MOV   #3,-(SP)
      TRAP  C$$SVEC
      ADD   #10,SP
2$:    READEF #EF.NEW          ;SEE IF A NEW PASS
      MOV    #EF.NEW,R0
      TRAP  C$REFG
      BNCOMPLETE 3$          ;IF NOT GO CHECK IF CONTINUE
      BCC   3$
      MOV   #-1,UNITNB        ;SETUP TO INIT UNIT NUMBER
3$:    READEF #EF.CONTINUE     ;CHECK IF CONTINUE
      MOV    #EF.CONTINUE,R0
      TRAP  C$REFG
      BCOMPLETE 6$           ;IF YES THEN EXIT
      BCS   6$
4$:    INC    UNITNB           ;INC TO NEW UNIT NUMBER
      GPHARD UNITNB,R5        ;GET DEVICE INFORMATION
      MOV    UNITNB,R0
      TRAP  C$GPHRD
      MOV    R0,R5
      BNCOMPLETE 4$          ;GO TRY ANOTHER UNIT
      BCC   4$
      MOV    #REGO,R1         ;ADDRESS OF SA DEVICE ADDRESS TABLE
5$:    CLR    R2               ;CLEAR OFFSET TO ADD TO TABLE ADDRESS
      MOV    (R5),(R1)        ;GET ADDRESS AND SAVE
      ADD   R2,(R1)+         ;ADD OFFSET TO ADDRESS
      INC   R2                ;UPDATE OFFSET BY 2
  
```



```

4400 013250 005202          INC      R2
4401 013252 022702 000010  CMP      #10,R2
4402 013256 001371          BNE      5$
4403 013260 005725          TST      (R5)+
4404 013262 012521          MOV      (R5)+,(R1)+
4405 013264 005011          CLR      (R1)
4406 013266 105721          TSTB    (R1)+
4407 013270 111521          MOVB    (R5),(R1)+
4408 013272 005725          TST      (R5)+
4409 013274 012721 100400  MOV      #IDH!SIG8H,(R1)+
4410 013300 005011          CLR      (R1)
4411 013302 105721          TSTB    (R1)+
4412 013304 111521          MOVB    (R5),(R1)+
4413 013306 005725          TST      (R5)+
4414 013310 012721 101000  MOV      #CDAL15!CDAL9,(R1)+
4415 013314 005011          CLR      (R1)
4416 013316 105721          TSTB    (R1)+
4417 013320 111521          MOVB    (R5),(R1)+
4418 013322 012711 100000  MOV      #GDAL15,(R1)
4419 013326          6$: SETPRI  #PRI07
4420 013326 012700 000340  MOV      #PRI07,R0
4421 013332 104441          TRAP    C$SPRI
4422
4423
4424 013334          EXIT    INIT
4425 013334 104432          TRAP    C$EXIT
4426 013336 000002          .WORD  L10030-.
4427
4428
4429          .EVEN
4430
4431 013340          ENDINIT
4432 013340          L10030:
4433 013340 104411          TRAP    C$INIT
4434
4435          .SBTTL AUTODROP SECTION
4436
4437          ;++
4438          ; THIS CODE IS EXECUTED IMMEDIATELY AFTER THE INITIALIZE CODE IF
4439          ; THE "ADR" FLAG WAS SET. THE UNIT(S) UNDER TEST ARE CHECKED TO
4440          ; SEE IF THEY WILL RESPOND. THOSE THAT DON'T ARE IMMEDIATELY
4441          ; DROPPED FROM TESTING.
4442          ;--
4443
4444 013342          BGNAUTO
4445 013342          L$AUTO::
4446
4447
4448 013342          ENDAUTO
4449 013342          L10031:
4450 013342 104461          TRAP    C$AUTO

```

4451
4452
4453
4454
4455
4456
4457
4458 013344
4459 013344
4460 013344
4461 013344 012700 000340
4462 013350 104441
4463 013352
4464 013352 104433
4465
4466 013354
4467 013354 104432
4468 013356 000002
4469
4470
4471
4472
4473 013360
4474 013360
4475 013360 104412
4476
4477
4478
4479
4480
4481
4482
4483
4484 013362
4485 013362
4486
4487
4488 013362
4489 013362 000167
4490 013364 000000
4491
4492
4493
4494
4495 013366
4496 013366
4497 013366 104453

.SBTTL CLEANUP CODING SECTION

:++
: THE CLEANUP CODING SECTION CONTAINS THE CODING THAT IS PERFORMED
: AFTER THE HARDWARE TESTS HAVE BEEN PERFORMED.
:--

BGNCLN
L\$CLEAN::
SETPRI #PRI07 ;RAISE THE CPU PRIORITY LEVEL TO 7
MOV #PRI07,R0
TRAP C\$SPRI
BRESE ;DO A RESET TO CLEAR ALL CDS-11 MODULES
TRAP C\$RESET

EXIT CLN
TRAP C\$EXIT
.WORD L10032-

.EVEN

ENDCLN
L10032: TRAP C\$CLEAN

.SBTTL DROP UNIT SECTION

:++
: THE DROP-UNIT SECTION CONTAINS THE CODING THAT CAUSES A DEVICE
: TO NO LONGER BE TESTED.
:--

BGNDU
L\$DU::

EXIT DU
.WORD JSJMP
.WORD L10033-2-

.EVEN

ENDDU
L10033: TRAP C\$DU

4498
4499
4500
4501
4502
4503
4504
4505
4506
4507
4508
4509
4510
4511
4512
4513
4514
4515
4516
4517
4518
4519
4520
4521
4522

013370
013370

013370
013370 000167
013372 000000

013374
013374
013374 104452

013376

```
.SBTTL ADD UNIT SECTION  
:++  
: THE ADD-UNIT SECTION CONTAINS ANY CODE THE PROGRAMMER WISHES  
: TO BE EXECUTED IN CONJUNCTION WITH THE ADDING OF A UNIT BACK  
: TO THE TEST CYCLE.  
:--  
  
L$AU:: BGNAU  
  
EXIT AU  
.WORD JSJMP  
.WORD L10034-2-  
  
.EVEN  
ENDAU  
L10034: TRAP C$AU  
  
ENDMOD
```

4523
4524
4525
4526
4527 013376
4528
4529
4530
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4537
4538
4539
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4541
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.TITLE HARDWARE TESTS

.SBTTL TEST 1: INITIALIZE ALL CDS-11 SYSTEM MODULES

BGNMOD

:++

THIS TEST WILL BE EXECUTED AS THE FIRST TEST IN THE PROGRAM AND AT THE BEGINNING OF EACH TEST IN THE PROGRAM. THE PURPOSE OF THIS TEST IS TO INITIALIZE THE CDS-11 MODULES (MEMORY SIMULATOR, STATE ANALYZER AND TARGET EMULATOR) TO A KNOWN STATE. THE TEST SEQUENCE IS DESCRIBED BELOW.

CDS-11 MEMORY SIMULATOR MODULE INITIALIZATION SEQUENCE:

1. LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVICE NUMBER TO SELECT THE MEMORY SIMULATOR MODULE.
2. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND THE BIT TO SET THE SIGNAL 'RST H' TO THE HIGH STATE. WHEN THE SIGNAL 'RST H' IS SET HIGH, THE 'RDV' AND 'WRV' FLIP-FLOPS WILL BE PRESET TO A ONE THUS CAUSING THE SIGNALS 'RDV H' AND 'WRV H' TO BE ASSERTED LOW. THE SIGNALS 'RDV H' AND 'WRV H' SHOULD BE READ AS ZEROES WHEN CONTROL REGISTER 0 IS READ.
3. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND BIT 15 SET TO A ONE. THE BIT WHICH SET THE SIGNAL 'RST H' TO THE HIGH STATE WILL BE CLEARED THUS SETTING THE SIGNAL LOW. WHEN BIT 15 IS SET TO A ONE, THE DEVICE TYPE WILL BE READ BACK ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE NUMBER.
4. CLEAR BIT 15 IN CONTROL REGISTER 0 AND THEN READ AND CHECK CONTROL REGISTER 0 FOR THE DEVICE NUMBER.
5. LOAD, READ AND CHECK CONTROL REGISTER 2'S READ/WRITE BITS 3:0 WITH A DATA PATTERN OF ZEROES. THESE BITS WILL SET THE SIGNALS MSEL1 H, MSEL0 H, MSAD17 H, AND MSAD16 H TO THE LOW STATE. THE READ ONLY SIGNALS MSBRK H, WREN H, AND ESR H WILL BE IGNORED AT THIS POINT IN TIME.
6. LOAD, READ AND CHECK CONTROL REGISTER 4'S READ/WRITE BITS 15:0 WITH A DATA PATTERN OF ALL ZEROES. THESE BITS WILL SET THE SIGNALS MSAD 15:0 H TO THE LOW STATE.

CDS-11 STATE ANALYZER MODULE INITIALIZATION

1. LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVIE NUMBER TO SELECT THE STATE ANALYZER MODULE.
2. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND THE BIT TO SET THE SIGNAL 'CDALO H' TO THE HIGH STATE. WHEN THE SIGNAL 'CDALO H' IS SET HIGH, THE TRACE RAM ADDRESS REGISTER, THE TRACING AND SBL FLIP-FLOPS WILL BE CLEARED AND THE EVENT COUNTERS WILL BE LOADED WITH DATA FROM THE EVENT COUNTER REGISTERS.
3. LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER AND THE BIT TO SET THE SIGNAL CDAL15 H TO A ONE. THE BIT WHICH SET 'CDALO H' TO THE HIGH STATE WILL BE CLEARED THUS SETTING THE SIGNAL 'CDALO H' TO THE LOW STATE. WHEN 'CDAL15 H' IS SET TO A ONE, THE DEVICE TYPE WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE NUMBER.
4. CLEAR THE BIT WHICH SET 'CDAL15 H' TO THE HIGH STATE AND THEN


```

4708 ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL "CKAI H" TO BE PULSED VIA THE
4709 ;THE SIGNAL "RASP L" LATER ON IN THIS TEST. ADAL REGISTER BIT 4 ON A
4710 ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
4711 ;THE SIGNAL XRAS H IS SET HIGH LATER IN THIS TEST.
4712
4713 013426 012737 043020 002334 MOV #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
4714 013434 004737 012764 JSR PC,BRKRES ;SET BITS 14, 10 + 9 AND TOGGLE ADALO H
4715
4716 ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
4717 ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
4718 ;REGISTER 6.
4719
4720 013440 004537 012232 JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
4721 013444 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
4722
4723 ;SET HDAL REGISTER BITS 9 AND 2 TO A ONE AND HDAL BITS 14 AND 11 TO DATA
4724 ;PATTERN TO BE TESTED FOR ADDRESS BITS 17 AND 16. HDAL2 H ON A ONE WILL
4725 ;ENABLE THE PROGRAM TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS.
4726 ;HDAL9 H ON A ONE WILL ENABLE THE DIGNOSTIC ADDRESS REGISTER ONTO THE
4727 ;ADDRESS BUS. ADDRESS BUS BITS 17 AND 16 WILL BE LOADED WITH A TEST
4728 ;PATTERN VIA HDAL REGISTER BITS 14 AND 11 RESPECTIVELY.
4729
4730 013446 012737 001004 002346 MOV #HDAL9!HDAL2,T6LOAD ;SET HDAL9 H AND HDAL2 H TO ONES
4731 013454 056137 000010 002346 BIS 10(R1),T6LOAD ;SETUP ADDRESS BITS 17 AND 16
4732 013462 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK HDAL REGISTER
4733 013466 001405 BEQ 1$ ;IF LOADED OK THEN CONTINUE
4734 013470 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
4735 013470 104455 TRAP C$ERRDF
4736 013472 000014 .WORD 12
4737 013474 003754 .WORD HDALRG
4738 013476 006730 .WORD T06ERR
4739 013500 CKLOOP
4740 013500 104406 TRAP C$CLP1
4741
4742 ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
4743 ;REGISTER 4. PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
4744 ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY "BRKRES L".
4745
4746 013502 005037 002340 1$: CLR T4LOAD ;SETUP TO CLEAR ALL OTHER R/W BITS
4747 013506 004737 012704 JSR PC,CLRPSM ;PULSE INVD L VIA VDAL2 H
4748
4749 ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4. ON
4750 ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
4751 ;BE WRITTEN OR READ.
4752
4753 013512 004537 012232 JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
4754 013516 000004 .WORD MODE ;SELECT THE MODE REGISTER
4755
4756 ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
4757 ;ZEROS. MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
4758
4759 013520 005037 002346 CLR T6LOAD ;SETUP TO CLEAR ALL MODE REGISTER BITS
4760 013524 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK MODE REGISTER
4761 013530 001405 BEQ 2$ ;IF LOADED OK THEN CONTINUE
4762 013532 ERRDF 12,MODREG,T06ERR ;MODE REGISTER NOT EQUAL EXPECTED
4763 013532 104455 TRAP C$ERRDF

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4764 013534 000014 .WORD 12
4765 013536 004000 .WORD MODREG
4766 013540 006730 .WORD T06ERR
4767 013542 CKLOOP
4768 013542 104406 TRAP C$CLP1
4769
4770 ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
4771 ;TO A 2. THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
4772 ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
4773 ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
4774 ;TER WILL BE ADDRESSED.
4775
4776 013544 004537 012232 2$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
4777 013550 000002 .WORD FDAL ;SELECT EOAI AND FDAL REGISTER
4778
4779 ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER. THE EOAI REGISTER WILL
4780 ;BE LOADED AND CHECKED FOR ZEROES. THE FDAL REGISTER WILL BE LOADED AND
4781 ;CHECKED FOR A DATA PATTERN OF ONE (FDALO H = 1).
4782
4783 013552 012737 000001 002346 MOV #FDALO,T6LOAD ;SETUP EOAI AND FDAL REG DATA PATTERN
4784 013560 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK EOAI + FDAL REG
4785 013564 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
4786 013566 ERRDF 12,EOAIFD,T06ERR ;EOAI OR FDAL REGISTER ERROR
4787 013566 104455 TRAP C$ERDF
4788 013570 000014 .WORD 12
4789 013572 004045 .WORD EOAIFD
4790 013574 006730 .WORD T06ERR
4791 013576 CKLOOP
4792 013576 104406 TRAP C$CLP1
4793
4794 ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
4795 ;2:0 TO A 0. THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH THE
4796 ;TEST PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6. THE DIAGNOSTIC
4797 ;ADDRESS REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER
4798 ;BIT 9 BEING SET TO A ONE PREVIOUSLY. ON A READ COMMAND TO CONTROL
4799 ;REGISTER 6, THE DIAGNOSTIC ADDRESS REGISTER WILL BE READBACK.
4800
4801 013600 004537 012232 3$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
4802 013604 000000 .WORD ADDRES ;SELECT THE DIAG ADDRESS REG AND ADDR BUS
4803
4804 ;LOAD READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH THE TEST PATTERN
4805 ;FROM THE DATA TABLE ADDRESSES BY R1
4806
4807 013606 011137 002346 MOV (R1),T6LOAD ;GET THE TEST PATTERN FROM THE TABLE
4808 013612 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK DIAG ADDRESS REG
4809 013616 001405 BEQ 4$ ;IF LOADED OK THEN CONTINUE
4810 013620 ERRDF 12,ADDRRG,T06ERR ;DIAGNOSTIC ADDRESS REGISTER ERROR
4811 013620 104455 TRAP C$ERDF
4812 013622 000014 .WORD 12
4813 013624 004142 .WORD ADDR RG
4814 013626 006730 .WORD T06ERR
4815 013630 CKLOOP
4816 013630 104406 TRAP C$CLP1
4817
4818 ;SELECT HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3. THE
4819 ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO

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4820                                     ;CONTROL REGISTER 6.
4821
4822 013632 004537 012232          4$: JSR    R5,SELTER          ;SELECT REGISTER SPECIFIED BY NEXT WORD
4823 013636 000003                .WORD  HDAL          ;SELECT THE HDAL REGISTER
4824
4825                                     ;PERFORM A T-11 MACHINE CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE:
4826                                     : 1. SET XRAS H AND PRAS H TO THE HIGH STATE
4827                                     : 2. SET XCAS H AND PCAS H TO THE HIGH STATE
4828                                     : 3. SET XPI L AND PPI L TO THE LOW STATE
4829                                     : 4. SET XCAS H AND PCAS H TO THE LOW STATE
4830                                     : 5. SET XPI L AND PPI L TO THE HIGH STATE
4831                                     : 6. SET XRAS H AND PRAS H TO THE LOW STATE
4832                                     ;PULSING THE SIGNAL PRAS H WILL CAUSE A PULSE TO BE ISSUED ON THE SIGNAL
4833                                     ;"ADVAL H". THE SIGNAL "ADVAL H" WILL CLOCK THE ADDRESS BUS SIGNALS
4834                                     ;"ADDR 17:0" INTO THE MEMORY SIMULATOR ADDRESS LATCHES. PULSING THE
4835                                     ;SIGNAL XRAS H WILL CAUSE PULSES TO BE ISSUED ON THE SIGNALS "EDCK0 H"
4836                                     ;"EDCK1 H". THESE TWO PULSES WILL CLOCK THE ADDRESS BUS SIGNALS "ADDR
4837                                     ;15:0" INTO THE STATE ANALYZER'S ADDRESS BUS LATCHES. PULSING THE SIGNAL
4838                                     ;XRAS H WILL ALSO CAUSE THE RASP ONE SHOT TO BE FIRED. A PULSE WILL BE
4839                                     ;ISSUED ON THE SIGNAL "CKAI H" AS A RESULT OF THE RASP ONE SHOT BEING
4840                                     ;FIRED. A PULSE ON THE SIGNAL "CKAI H" WILL CAUSE A PULSE ON THE SIGNAL
4841                                     ;"EDCK5 H". THE SIGNAL "EDCK5 H" WILL CLOCK THE CTL 7:0 BUS INTO THE
4842                                     ;STATE ANALYZER'S SYSTEM BUS LATCHES FOR THESE BITS. PULSING THE SIGNAL
4843                                     ;XPI L WILL CAUSE A PULSE ON THE SIGNAL "EDCK4 H". THE SIGNAL "EDCK4 H"
4844                                     ;WILL CLOCK SYSTEM BUS SIGNALS "CTL 11:8" AND "BTS 3:0" INTO THE STATE
4845                                     ;ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS.
4846
4847 013640 012737 001004 002346      MOV    #HDAL9!HDAL2,T6LOAD      ;SETUP PREVIOUSLY LOADED BITS
4848 013646 056137 000010 002346      BIS    10(R1),T6LOAD
4849 013654 004737 012276                JSR    PC,XRASH          ;SET XRAS H AND PRAS H TO HIGH STATE
4850 013660 004737 012402                JSR    PC,XCASH          ;SET XCAS H AND PCAS H TO HIGH STATE
4851 013664 004737 012506                JSR    PC,XPIH           ;SET XPI L AND PPI L TO THE LOW STATE
4852 013670 004737 012434                JSR    PC,XCASL          ;SET XCAS H AND PCAS H TO LOW STATE
4853 013674 004737 012540                JSR    PC,XPIL           ;SET XPI L AND PPI L TO THE HIGH STATE
4854 013700 004737 012330                JSR    PC,XRASL          ;SET XRAS H AND PRAS H TO LOW STATE
4855
4856                                     ;READ CONTROL REGISTER 0 TO CHECK THAT NO BREAK BITS ARE SET AS A RESULT
4857                                     ;OF XRAS H AND PRAS H BEING PULSED.
4858
4859 013704 004737 011112                JSR    PC,READT0         ;READ AND CHECK REGISTER 0
4860 013710 001405                BEQ    5$                ;IF OK THEN CONTINUE
4861 013712                                ERRDF  9,GDALRG,TOEROR    ;GDAL REGISTER NOT EQUAL EXPECTED
4862 013712 104455                TRAP   C$ERDF
4863 013714 000011                .WORD  9
4864 013716 003636                .WORD  GDALRG
4865 013720 006664                .WORD  TOEROR
4866 013722                                CKLOOP
4867 013722 104406                TRAP   C$CLP1
4868
4869                                     ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER). THE SIGNAL EDEOC H
4870                                     ;SHOULD BE SET TO A ONE.
4871
4872 013724 052737 000020 002342 5$:    BIS    #VDAL4,T4GOOD      ;CHECK THAT EDEOC H IS SET TO A ONE
4873 013732 004737 011176                JSR    PC,READT4         ;READ AND CHECK V^AL REGISTER
4874 013736 001405                BEQ    6$                ;IF NO CHANGES THEN CONTINUE
4875 013740                                ERRDF  11,VDALRG,T4EROR  ;VDAL OR PAUSE STATE MACHINE ERROR

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4876 013740 104455 TRAP C$ERDF
4877 013742 000013 .WORD 11
4878 013744 003706 .WORD VDALRG
4879 013746 006714 .WORD T4EROR
4880 013750 CKLOOP
4881 013750 104406 TRAP C$CLP1
4882
4883 ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
4884 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
4885
4886 013752 004737 011246 6$: JSR PC,SLCTMS ;SELECT MEMORY SIMULATOR MODULE
4887
4888 ;SET THE SIGNAL CTS H TO A ONE IN CONTROL REGISTER 0 OF THE MEMORY
4889 ;SIMULATOR MODULE. THIS WILL ENABLE THE SYSTEM BUS SIGNALS RECEIVED
4890 ;TO THE MEMORY SIMULATOR LOGIC. IN THIS TEST, CTS H ON A ONE WILL
4891 ;ENABLE THE SYSTEM BUS ADDRESSES TO MEMORY SIMULATOR SIGNALS MSAD 17:0.
4892
4893 013756 112737 000002 002234 MOVB #CTSH,S0LOAD ;SETUP BIT TO SET CTS H TO A ONE
4894 013764 004737 010504 JSR PC,LDRDSO ;GO LOAD, READ AND CHECK REGISTER 0
4895 013770 001405 BEQ 7$ ;IF LOADED OK THEN CONTINUE
4896 013772 ERRDF 1,,S0EROR ;MEM SIM REG 0 NOT EQUAL EXPECTED
4897 013772 104455 TRAP C$ERDF
4898 013774 000001 .WORD 1
4899 013776 000000 .WORD 0
4900 014000 005304 .WORD S0EROR
4901 014002 CKLOOP
4902 014002 104406 TRAP C$CLP1
4903
4904 ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE
4905 ;ADDRESSES CLOCKED INTO THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS
4906 ;REGISTER WAS CLOCKED INTO THE MEMORY SIMULATOR ADDRESS LATCHES BY THE
4907 ;SIGNAL "ADVAL H". THE SIGNAL "ADVAL H" WAS GENERATED BY PULSING THE
4908 ;SIGNAL "PRAS H" ON THE TARGET EMULATOR MODULE. THE MEMORY SIMULATOR'S
4909 ;ADDRESS LATCHES ARE ENABLED TO MSAD BITS 17:0 AS A RESULT OF CTS H
4910 ;BEING ASSERTED HIGH AND CTS L BEING ASSERTED LOW.
4911
4912 014004 011137 002254 7$: MOV (R1),S4LOAD ;GET PATTERN LOADED INTO TARGET EMULATOR
4913 014010 004737 010612 JSR PC,READS4 ;READ AND CHECK CONTROL REGISTER 4
4914 014014 001405 BEQ 8$ ;IF OK THEN CONTINUE
4915 014016 ERRDF 3,TEMSAD,S04ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
4916 014016 104455 TRAP C$ERDF
4917 014020 000003 .WORD 3
4918 014022 002532 .WORD TEMSAD
4919 014024 005404 .WORD S04ERR
4920 014026 CKLOOP
4921 014026 104406 TRAP C$CLP1
4922
4923 ;READ AND CHECK MSAD BITS 17 AND 16 IN CONTROL REGISTER 2 TO SEE IF THEY
4924 ;ARE THE SAME AS SET ON THE TARGET EMULATOR MODULE. ADDRESS BITS 17 AND
4925 ;16 ARE CLOCKED INTO THE MEMORY SIMULATOR ADDRESS LATCH BY THE SIGNAL
4926 ;"ADVAL H". THE SIGNAL "ADVAL H" WAS GENERATED BY PULSING THE SIGNAL
4927 ;"PRAS H" ON THE TARGET EMULATOR MODULE. THE MEMORY SIMULATOR'S ADDRESS
4928 ;LATCHES ARE ENABLED TO MSAD BITS 17:0 AS A RESULT OF "CTS H" AND "CTS L"
4929 ;BEING ASSERTED HIGH AND LOW RESPECTIVELY.
4930
4931 014030 052737 000014 002250 8$: BIS #MSEL1!MSEL0,S2MASK ;SETUP TO IGNORE MSEL1 H AND MSEL0 H

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4932 014036 016137 000020 002244      MOV      20(R1),S2LOAD      ;GET EXPECTED MSAD BITS 17 AND 16
4933 014044 016137 000020 002246      MOV      20(R1),S2GOOD     ;SAVE FOR COMPARISONS ON A READ COMMAND
4934 014052 004737 010560                JSR      PC,READS2         ;READ AND CHECK CONTROL REGISTER 2
4935 014056 001405                BEQ      9$                ;IF OK THEN CONTINUE
4936 014060                ERRDF    2,TEMSA1,S02ERR   ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
4937 014060 104455                TRAP    C$ERDF
4938 014062 000002                .WORD   2
4939 014064 002406                .WORD   TEMSA1
4940 014066 005364                .WORD   S02ERR
4941 014070                CKLOOP
4942 014070 104406                TRAP    C$CLP1
4943
4944                ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
4945                ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
4946
4947 014072 004737 012142      9$:      JSR      PC,SLCTED        ;SELECT STATE ANALYZER MODULE
4948
4949                ;SET THE SIGNAL TRSL2 L TO THE LOW STATE BY SETTING CDAL REGISTER BIT
4950                ;3 TO A ONE AND CDAL REGISTER BIT 2 TO A ZERO. THE SIGNAL TRSL2 L WILL
4951                ;ENABLE THE STATE ANALYZERS SYSTEM BUS LATCHES TO THE STATE ANALYZERS
4952                ;TRDI 59:0 BUS.
4953
4954 014076 004737 000010 002272      MOVVB   #CDAL3,E0LOAD     ;SETUP BITS TO SET TRSL2 L TO LOW STATE
4955 014104 004737 010676      JSR      PC,LDRDE0        ;GO LOAD, READ AND CHECK CONTROL REG 0
4956 014110 001405                BEQ      10$              ;IF LOADED OK THEN CONTINUE
4957 014112                ERRDF    5,CDALRG,E0EROR  ;CDAL REGISTER NOT EQUAL EXPECTED
4958 014112 104455                TRAP    C$ERDF
4959 014114 000005                .WORD   5
4960 014116 003006                .WORD   CDALRG
4961 014120 006144                .WORD   E0EROR
4962 014122                CKLOOP
4963 014122 104406                TRAP    C$CLP1
4964
4965                ;ASSERT THE SIGNAL PTER1 L IN THE POINTER REGISTER BY LOADING THE
4966                ;APPROPRIATE BITS IN THE PDAL REGISTER (CONTROL REGISTER 2)
4967
4968 014124 004537 012162      10$:     JSR      R5,LDPDAL        ;LOAD AND CHECK PDAL REG WITH NEXT WORD
4969 014130 000001                .WORD   PTER1            ;SETUP TO READ TRDI BUS BITS 15:0
4970
4971                ;AS A RESULT OF A PULSE ON THE TARGET EMULATOR'S SIGNAL "XRAS H" AT THE
4972                ;BEGINNING OF THIS TEST, THE TARGET EMULATOR'S ADDRESS BUS WAS CLOCKED
4973                ;INTO THE STATE ANALYZER'S ADDRESS LATCHES VIA THE CLOCKING SIGNALS
4974                ;"EDCK0 H" AND "EDCK1 H". THE PROGRAM HAS ALREADY ASSERTED THE SIGNAL
4975                ;"TRSL2 L" WHICH WILL ENABLE THE SYSTEM BUS LATCHES ONTO THE STATE
4976                ;ANALYZER'S TRDI 59:0 BUS. WHEN THE PROGRAM ISSUES A READ COMMAND TO
4977                ;CONTROL REGISTER 6 AND THE PDAL REGISTER IS SETUP TO SELECT PTER1 L,
4978                ;A PULSE WILL BE ISSUED ON THE SIGNAL RPT1 L. THIS SIGNAL WILL READ
4979                ;TRDI BUS BITS 15:0 WHICH ARE THE ADDRESS LATCHES FOR SYSTEM BUS
4980                ;ADDRESSES 15:0.
4981
4982 014132 011137 002316      MOV      (R1),E6LOAD      ;GET DATA LOADED INTO TARGET EMULATOR
4983 014136 004737 011052      JSR      PC,READE6        ;READ ADDRESSES 15:0 ON TRDI 15:0
4984 014142 001405                BEQ      11$              ;IF OK THEN CONTINUE
4985 014144                ERRDF    8,TEEDAD,E026ER  ;TE TO SA ADDRESS BUS ERROR - TRDI 15:0
4986 014144 104455                TRAP    C$ERDF
4987 014146 000010                .WORD   8

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4988 014150 003171      .WORD  TEEDAD
4989 014152 006210      .WORD  E026ER
4990 014154              CKLOOP
4991 014154 104406      TRAP   C$CLP1
4992
4993                      ;ASSERT THE SIGNAL 'PTER3 L' IN THE POINTER REGISTER BY LOADING THE
4994                      ;APPROPRIATE BITS IN CONTROL REGISTER 2'S P'AL REGISTER.
4995
4996 014156 004537 012162 11$: JSR    R5,LDPDAL      ;LOAD AND CHECK PDAL REG NEXT WORD
4997 014162 000003              .WORD  PTER3        ;SETUP TO READ TRDI BUS BITS 47:32
4998
4999                      ;AS A RESULT OF PULSES ON THE TARGET EMULATOR'S SIGNALS 'RASP L' AND
5000                      ;'XPI L', PULSES SHOULD HAVE OCCURED ON THE SIGNALS 'EDCK5 H' AND
5001                      ;'EDCK4 H' RESPECTIVELY. THE PULSE 'EDCK5 H' WILL CLCOK THE CTL SYSTEM
5002                      ;BUS BITS 7:0 INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES FOR THESE
5003                      ;BITS. THESE BITS WILL BE READ ONTO THE STATE ANALYZERS TRDI BUS BITS
5004                      ;47:40. THIS TEST WILL NOT CHECK THESE BITS AT THIS TIME. THE PULSE,
5005                      ;'EDCK4 H', WILL CLOCK SYSTEM BUS ADDRESS BITS 17 AND 16, AND THE TARGET
5006                      ;EMULATOR'S SIGNALS BTS 3:0 INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES
5007                      ;FOR THESE BITS. THESE BITS WILL BE READ ONTO THE STATE ANALYZERS TRDI
5008                      ;BUS BITS 39:32. TRDI BUS BITS 47:40 WILL BE IGNORED DURING THIS TEST.
5009                      ;THE SIGNAL BTS0 H WILL BE READ AS A ONE ON TRDI BIT 32 AS A RESULT OF
5010                      ;THE TARGET EMULATOR'S SIGNALS BEING SET ACCORDINGLY:
5011                      :      XR/WHB L - HIGH STATE
5012                      :      MR11 L  - HIGH STATE
5013                      :      XR/WLB H - LOW STATE
5014                      :      INTER L - HIGH STATE
5015
5016 014164 016137 000030 002316 MOV    30(R1),E6LOAD      ;GET EXPECTED TRDI 39:32 PATTERN
5017 014172 012737 177400 002320 MOV    #177400,E6MASK    ;SETUP TO IGNORE UNWANTED BITS
5018 014200 004737 011052          JSR    PC,READE6        ;READ BTS 3:0 + ADDR 17:16 ON TRDI 39:32
5019 014204 001404              BEQ    12$              ;IF OK THEN CONTINUE
5020 014206              ERRDF  8,TEEDA1,E026ER      ;TE TO SA XSEL1,EDSELO,ADDR 17:16 + BTS 3:0 ERRO
5021 014206 104455      TRAP   C$ERDF
5022 014210 000010      .WORD  8
5023 014212 003240      .WORD  TEEDA1
5024 014214 006210      .WORD  E026ER
5025 014216              12$: ENDSEG
5026 014216              10000$:
5027 014216 104405      TRAP   C$ESEG
5028
5029 014220 000420      BR     31$
5030
5031                      ;DATA PATTERN FOR ADDRESS BITS 15:0 TO BE LOADED INTO DIAGNOSTIC ADDRESS
5032                      ;REGISTER.
5033
5034 014222 177777      30$: .WORD  177777
5035 014224 052525      .WORD  052525
5036 014226 125252      .WORD  125252
5037 014230 000000      .WORD  000000
5038
5039                      ;HDAL REGISTER ADDRESS BITS ON TARGET EMULATOR MODULE TO SET ADDRESS
5040                      ;BITS 17 AND 16
5041
5042 014232 040000      .WORD  HDAL14        ;ADDRESS 17
5043 014234 004000      .WORD  HDAL11        ;ADDRESS 16

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5044 014236 044000      .WORD  HDAL14!HDAL11      :ADDRESS 17 AND 16
5045 014240 000000      .WORD  0                  :ADDRESS 17 AND 16 SET TO A 0
5046
5047                      ;EXPECTED MEMORY SIMULATOR CONTROL REGISTER 2 MSAD BITS FOR 17 AND 16
5048
5049 014242 000002      .WORD  MSAD17
5050 014244 000001      .WORD  MSAD16
5051 014246 000003      .WORD  MSAD17!MSAD16
5052 014250 000000      .WORD  0
5053
5054                      ;EXPECTED STATE ANALYZER BITS FOR XSEL1 H, EDSELO H, ADDRESSES 17:16
5055                      ;AND BTS BITS 3:0
5056
5057 014252 000041      .WORD  BIT5!BIT0          :ADDRESS 17 AND BTS0 H
5058 014254 000021      .WORD  BIT4!BIT0          :ADDRESS 16 AND BTS0 H
5059 014256 000061      .WORD  BIT5!BIT4!BIT0     :ADDRESS 17 AND 16 AND BTS0 H
5060 014260 000001      .WORD  BIT0               :BTS0 H
5061
5062 014262              31$:  ENDTST
5063 014262              L10036:
5064 014262 104401      TRAP  C$ETST
5065

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.SBTTL TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE

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THIS TEST WILL CHECK THAT DATA, WRITTEN INTO LOCATIONS OF THE MEMORY SIMULATOR RAM, CAN BE ENABLED TO THE TARGET EMULATOR MODULE AND CLOCKED INTO THE STATE ANALYZER MODULE VIA THE SYSTEM DATA BUS WHEN A 'READ' OPERATION IS BEING EXECUTED FROM THE TARGET EMULATOR MODULE IN 16 BIT MODE. ADDRESSES 0, 20000, 40000 AND 60000, WHICH ARE THE FIRST LOCATIONS OF EACH 4K BANK OF MEMORY SIMULATOR RAM, WILL BE WRITTEN WITH A DATA PATTERN OF 125252, 052525, 177777, AND 000000 RESPECTIVELY. LOCATIONS OF THE MEMORY SIMULATOR RAM WILL BE ADDRESSED VIA THE DIAGNOSTIC ADDRESS REGISTER ON THE TARGET EMULATOR MODULE DURING A NORMAL T-11 TIMING CYCLE. A NORMAL T-11 TIMING CYCLE OCCURS WHEN RAS, CAS AND PI ARE ASSERTED IN THE ORDER LISTED AND THEN DE-ASSERTED IN THE FOLLOWING ORDER CAS, PI AND RAS. THE PROGRAM WILL CHECK THAT THE SYSTEM ADDRESS BUS WAS CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES AND THE STATE ANALYZER'S SYSTEM BUS LATCHES WHEN THE SIGNALS XRAS H AND PRAS H ARE ASSERTED HIGH ON THE TARGET EMULATOR MODULE. WHEN THE TARGET EMULATOR SIGNALS XR/WLB H, XR/WHB H, XRAS H, AND XCAS H ARE ASSERTED HIGH, THE TARGET EMULATOR SIGNALS 'READ H' AND 'MSDI H' WILL BE ASSERTED HIGH. THE SIGNAL 'READ H' BEING ASSERTED WILL ENABLE MEMORY SIMULATOR RAM DATA ADDRESSED BY THE TARGET EMULATOR MODULE ONTO THE SYSTEM DATA BUS. THE SYSTEM DATA BUS WILL BE ENABLED TO THE TARGET EMULATOR'S EODAL BUS VIA THE SIGNAL 'MSDI H' AND THE EODAL BUS WILL BE ENABLED TO THE TARGET EMULATOR'S EIDAL BUS VIA THE SIGNALS COHB L AND COLB L. THE SIGNALS COHB L AND COLB L ARE ASSERTED LOW AS A RESULT OF THE SIGNALS ETR L, PR/WLB H, PR/WHB H, PPI H, DMG L, AND MR11 L BEING ASSERTED HIGH. THE PROGRAM WILL READ AND CHECK THE TARGET EMULATOR'S EODAL AND EIDAL BUS TO CONTAIN THE EXPECTED MEMORY SIMULATOR RAM DATA. WHEN THE SIGNAL XCAS L IS RETURNED TO ITS DE-ASSERTED STATE, THE SIGNALS 'EDCK2 H' AND 'EDCK3 H' WILL GO FROM A LOW TO A HIGH STATE THUS CLOCKING THE SYSTEM DATA BUS INTO THE STATE ANALYZER'S SYSTEM DATA BUS LATCHES. THE PROGRAM WILL CHECK THAT THE SYSTEM DATA BUS WAS CLOCKED INTO THE STATE ANALYZER'S SYSTEM DATA BUS LATCHES BY ENABLING THE LATCHES TO THE STATE ANALYZER'S TRDI BUS VIA THE SIGNAL TRSL2 L AND THEN READING TRDI BUS BITS 31:16 TO CONTAIN THE EXPECTED MEMORY SIMULATOR RAM DATA. THE PROGRAM WILL ALSO CHECK THAT THE STATE ANALYZER'S TRACE RAM ADDRESS REGISTER WAS INCREMENTED BY ONE VIA THE SIGNAL 'CTR L' WHEN THE TARGET EMULATOR SIGNAL 'EDEOC H' WAS SET HIGH.

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T3:: BGNTST
      JSR    PC,INITMD          ;INITIALIZE CDS-11 SYSTEM MODULES
      BGNSEG
      TRAP  C$BSEG
      CLR    E6MASK            ;CLEAR REGISTER 6 MASK WORD FOR LOOPING
      ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
      ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
      JSR    PC,SLCTTE         ;SELECT TARGET EMULATOR MODULE
      ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL 'BRKRES L'
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5122                                     ;BY TOGGING ADAL REGISTER BIT 0. ADAL10 H AND ADAL9 H SET TO ONES WILL
5123                                     ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS. PULSING
5124                                     ;THE SIGNAL 'BRKRES L' VIA ADALO H WILL CLEAR THE BREAK LOGIC ON THE
5125                                     ;TARGET EMULATOR MODULE. ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
5126                                     ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL 'CKAI H' TO BE PULSED VIA THE
5127                                     ;THE SIGNAL 'RASP L' LATER ON IN THIS TEST. ADAL REGISTER BIT 4 ON A
5128                                     ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
5129                                     ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
5130
5131 014302 012737 043020 002334      MOV      #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
5132 014310 004737 012764              JSR      PC,BRKRES                       ;SET BITS 14, 10 + 9 AND TOGGLE ADALO H
5133
5134                                     ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
5135                                     ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
5136                                     ;REGISTER 6.
5137
5138 014314 004537 012232      JSR      R5,SELTER                       ;SELECT REGISTER SPECIFIED BY NEXT WORD
5139 014320 000003              .WORD   HDAL                            ;SELECT THE HDAL REGISTER
5140
5141                                     ;SET HDAL REGISTER BITS 9,4,3 + 2 TO A ONE AND HDAL BITS 14 AND 11 TO A
5142                                     ;ZERO. HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
5143                                     ;AND CONTROL SIGNALS. HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
5144                                     ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS. HDAL REGISTER
5145                                     ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
5146                                     ;HDAL REGISTER BITS 4 AND 3 SET TO ONES WILL SET THE SIGNALS XR/WLB H
5147                                     ;AND XR/WHB H TO THE HIGH STATE. THESE SIGNALS WILL CAUSE THE SIGNAL
5148                                     ;'REAT H' TO BE ASSERTED HIGH LATER IN THIS TEST WHEN THE SIGNALS XRAS H
5149                                     ;AND XCAS H ARE ASSERTED HIGH.
5150
5151 014322 012737 001034 002346      MOV      #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SET HDAL BITS 9,4,3 + 2 TO ONES
5152 014330 004737 011214      JSR      PC,LDRDT6                      ;GO LOAD, READ AND CHECK HDAL REGISTER
5153 014334 001405      BEQ      1$                             ;IF LOADED OK THEN CONTINUE
5154 014336              ERRDF      12,HDALRG,T06ERR      ;HDAL REGISTER NOT EQUAL EXPECTED
5155 014336 104455      TRAP     C$ERDF
5156 014340 000014      .WORD   12
5157 014342 003754      .WORD   HDALRG
5158 014344 006730      .WORD   T06ERR
5159 014346              CKLOOP
5160 014346 104406      TRAP     C$CLP1
5161
5162                                     ;PULSE THE SIGNAL 'INVD L' BY SETTING AND CLEARING VDAL2 H IN CONTROL
5163                                     ;REGISTER 4. PULSING THE SIGNAL 'INVD L' WILL INITIALIZE ALL THE
5164                                     ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L'.
5165
5166 014350 005037 002340      CLR      T4LOAD                          ;SETUP TO CLEAR ALL OTHER R/W BITS
5167 014354 004737 012704      JSR      PC,CLRPSM                      ;PULSE INVD L VIA VDAL2 H
5168
5169                                     ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4. ON
5170                                     ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
5171                                     ;BE WRITTEN OR READ.
5172
5173 014360 004537 012232      JSR      R5,SELTER                       ;SELECT REGISTER SPECIFIED BY NEXT WORD
5174 014364 000004      .WORD   MODE                            ;SELECT THE MODE REGISTER
5175
5176                                     ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
5177                                     ;ZEROS. MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE

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5178
5179 014366 005037 002346          CLR      T6LOAD          ;SETUP TO CLEAR ALL MODE REGISTER BITS
5180 014372 004737 011214          JSR      PC,LDRDT6      ;GO LOAD, READ AND CHECK MODE REGISTER
5181 014376 001405                   BEQ      2$              ;IF LOADED OK THEN CONTINUE
5182 014400                   ERRDF   12,MODREG,T06ERR ;MODE REGISTER NOT EQUAL EXPECTED
5183 014400 104455                   TRAP    C$ERDF
5184 014402 000014                   .WORD   12
5185 014404 004000                   .WORD   MODREG
5186 014406 006730                   .WORD   T06ERR
5187 014410                   CKLOOP
5188 014410 104406                   TRAP    C$CLP1
5189
5190                               ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
5191                               ;TO A 2. THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
5192                               ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
5193                               ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
5194                               ;TER WILL BE ADDRESSED.
5195
5196 014412 004537 012232          2$:   JSR      R5,SELTER      ;SELECT REGISTER SPECIFIED BY NEXT WORD
5197 014416 000002                   .WORD   FDAL            ;SELECT EOAI AND FDAL REGISTER
5198
5199                               ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER. THE EOAI REGISTER WILL
5200                               ;BE LOADED AND CHECKED FOR ZEROES. THE FDAL REGISTER WILL BE LOADED AND
5201                               ;CHECKED FOR A DATA PATTERN OF ONE (FDALO H = 1).
5202
5203 014420 012737 000001 002346      MOV      #FDALO,T6LOAD   ;SETUP EOAI AND FDAL REG DATA PATTERN
5204 014426 004737 011214          JSR      PC,LDRDT6      ;GO LOAD, READ AND CHECK EOAI + FDAL REG
5205 014432 001405                   CEQ     3$              ;IF LOADED OK THEN CONTINUE
5206 014434                   ERRDF   12,EOAIFD,T06ERR ;EOAI OR FDAL REGISTER ERROR
5207 014434 104455                   TRAP    C$ERDF
5208 014436 000014                   .WORD   12
5209 014440 004045                   .WORD   EOAIFD
5210 014442 006730                   .WORD   T06ERR
5211 014444                   CKLOOP
5212 014444 104406                   TRAP    C$CLP1
5213
5214                               ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
5215                               ;CHANGES OCCURED DOING THE PAST SEQUENCES.
5216
5217 014446 004737 011176          3$:   JSR      PC,READT4      ;READ AND CHECK VDAL REGISTER
5218 014452 001404                   BEQ     4$              ;IF NO CHANGES THEN CONTINUE
5219 014454                   ERRDF   11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
5220 014454 104455                   TRAP    C$ERDF
5221 014456 000013                   .WORD   11
5222 014460 003706                   .WORD   VDALRG
5223 014462 006714                   .WORD   T4EROR
5224 014464                   4$:   ENDSEG
5225 014464                   10000$:
5226 014464 104405                   TRAP    C$ESEG
5227
5228 014466                   BGNSEG
5229 014466 104404                   TRAP    C$BSEG
5230
5231                               ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5232                               ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5233

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5234 014470 004737 011246 JSR PC,SLCTMS ;SELECT MEMORY SIMULATOR MODULE
5235
5236 ;GO LOAD, READ AND CHECK THE MEMORY SIMULATOR MAP PROTECTION RAM. THE
5237 ;MAP PROTECTION RAM WILL HAVE THE BITS 'MUTB H' AND 'MPIN H' SET TO
5238 ;ONES FOR ALL ADDRESSES IN THE MAP PROTECTION RAM. MAP PROTECTION RAM
5239 ;BITS 'WRE H' AND 'RDE H' WILL BE SET TO ONES FOR THE FIRST 16K WORDS OF
5240 ;MEMORY SIMULATOR RAM AND TO ZEROES FOR ALL ADDRESSES ABOVE 16K WORDS.
5241 ;WHEN 'RDE H' AND 'WRE H' ARE SET TO ONES, READ AND WRITES ARE ALLOWED
5242 ;TO THOSE ADDRESSES.
5243
5244 014474 004737 011354 JSR PC,MPRAM ;GO LOAD, READ AND CHECK MAP PROTECT RAM
5245
5246 ;GO LOAD, READ AND CHECK MODULE SELECT RAM 0. THE FOLLOWING DATA
5247 ;PATTERNS: 1, 2, 4, 10, 0, 0, 0, AND 0 WILL BE LOADED INTO CONSECUTIVE
5248 ;LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS 0. THESE PATTERNS
5249 ;WILL ENABLE THE FIRST 16K WORDS OF THE MEMORY SIMULATOR RAM TO BE
5250 ;ADDRESSED.
5251
5252 014500 004737 011640 JSR PC,MSRAM0 ;LOAD, READ AND CHECK MODULE SELECT RAM 0
5253
5254 ;GO LOAD, READ AND CHECK MODULE SELECT RAM 1. THE FOLLOWING DATA PATTERNS
5255 ;WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
5256 ;AT ADDRESS 0; 17, 0, 0 AND 0. THESE PATTERNS WILL ENABLE THE FIRST 32K
5257 ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
5258
5259 014504 004737 012010 JSR PC,MSRAM1 ;LOAD, READ AND CHECK MODULE SELECT RAM 1
5260
5261 014510 012701 015644 MOV #30$,R1 ;SETUP POINTER TO ADDRESS TABLE
5262
5263 014514 5$: BGNSEG
5264 014514 104404 TRAP C$BSEG
5265
5266 ;LOAD MEMORY SIMULATOR RAM ADDRESS TO BE TESTED INTO CONTROL REGISTER 4.
5267 ;ADDRESSES TO BE LOADED ARE 0, 20000, 40000 AND 60000.
5268
5269 014516 011137 002254 MOV (R1),S4LOAD ;GET ADDRESS FROM ADDRESS TABLE
5270 014522 004737 010604 JSR PC,LDRDS4 ;LOAD READ AND CHECK CONTROL REG 4
5271 014526 001405 BEQ 6$ ;IF LOADED OK THEN CONTINUE
5272 014530 ERRDF 3,MSADRG,S4EROR ;MSAD 15:0 REGISTER ERROR
5273 014530 104455 TRAP C$ERDF
5274 014532 000003 .WORD 3
5275 014534 002506 .WORD MSADRG
5276 014536 005334 .WORD S4EROR
5277 014540 CKLOOP
5278 014540 104406 TRAP C$CLP1
5279
5280 ;CLEAR BITS MSEL1 H, MSEL0 H, MSAD17 H AND MSAD16 H IN CONTROL REGISTER
5281 ;2. MSEL0 H AND MSEL1 H ON A ZERO WILL CAUSE THE SIGNAL 'SSM L' TO BE
5282 ;ASSERTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6. ON A WRITE
5283 ;OR READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE WRITTEN INTO OR
5284 ;READ FROM MEMORY SIMULATOR RAM ADDRESSES BY CONTROL REGISTER 2 AND 4.
5285 ;THE MEMORY SIMULATOR RAM'S ARE ENABLED BY THE DATA PATTERNS PREVIOUSLY
5286 ;WRITTEN INTO MODULE SELECT RAMS 0 AND 1. MSAD17 H AND MSAD16 H WILL BE
5287 ;LOADED AND CHECKED WITH ZEROES. THE PROGRAM WILL EXPECT CONTROL REGIS-
5288 ;TER 2 BITS 'ESR H' AND 'WREN H' TO BE READ AS ONES AS A RESULT OF MAP
5289 ;PROTECTION RAM BITS 'MPIN H' AND 'WRE H' BEING SET TO ONES.

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5290
5291 014542 005037 002244      6$: CLR      S2LOAD      ;SET ALL BITS IN REG 2 TO ZEROES
5292 014546 013737 002244 002246 MOV      S2LOAD,S2GOOD ;COPY DATA LOADED TO EXPECTED
5293 014554 052737 000140 002246 BIS      #ESRH!WRENH,S2GOOD ;EXPECT ESR H AND WREN H TO BE ONES
5294 014562 012737 177400 002250 MOV      #177400,S2MASK ;SETUP TO COMPARE LOW BYTE
5295 014570 004737 010552 JSR      PC,LDRD2S ;LOAD, READ AND CHECK CONTROL REG 2
5296 014574 001405 BEQ      7$ ;IF LOADED OK THEN CONTINUE
5297 014576 ERRDF 2,,S2EROR ;CONTROL REGISTER 2 NOT = EXPECTED
5298 014576 104455 TRAP    C$ERDF
5299 014600 000002 .WORD 2
5300 014602 000000 .WORD 0
5301 014604 005320 .WORD S2EROR
5302 014606 CKLOOP
5303 014606 104406 TRAP    C$CLP1
5304
5305 ;LOAD DATA PATTERN INTO MEMORY SIMULATOR RAM ADDRESSED BY CONTROL
5306 ;REGISTER 2 AND 4. THE ADDRESS AND DATA PATTERN LOADED ARE AS FOLLOWS:
5307 ;
5308 ; ADDRESS DATA
5309 ; 000000 125252
5310 ; 020000 052525
5311 ; 040000 177777
5312 ; 060000 000000
5313 014610 005037 002264      7$: CLR      S6MASK      ;SETUP TO COMPARE ALL BITS
5314 014614 016137 000010 002260 MOV      10(R1),S6LOAD ;GET DATA PATTERN FROM THE TABLE
5315 014622 004737 010630 JSR      PC,LDRDS6 ;GO LAOD, READ AND CHECK RAM LOCATION
5316 014626 001404 BEQ      8$ ;IF LOADED OK THEN CONTINUE
5317 014630 ERRDF 4,MSGMSR,S6ALLR ;DATA ERROR IN MEMORY SIMULATOR RAM
5318 014630 104455 TRAP    C$ERDF
5319 014632 000004 .WORD 4
5320 014634 002743 .WORD MSGMSR
5321 014636 005454 .WORD S6ALLR
5322 014640 8$: ENDSEG
5323 014640 10002$:
5324 014640 104405 TRAP    C$ESEG
5325
5326 014642 005761 000010 TST     10(R1) ;CHECK IF LAST DATA PATTERN
5327 014646 001402 BEQ     9$ ;IF YES THEN START NEXT SETUP
5328 014650 005721 TST     (R1)+ ;UPDATE POINTER TO ADDRESS TABLE
5329 014652 000720 BR      5$ ;GO LOAD NEXT ADDRESS AND DATA PATTERN
5330
5331 ;SET THE SIGNAL "CTS H" TO A ONE IN CONTROL REGISTER 0. THIS WILL
5332 ;ENABLE THE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR LOGIC.
5333 ;IN THIS TEST, "CTS H" ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO
5334 ;THE MEMORY SIMULATOR MODULE AND THE MEMORY SIMULATOR RAM DATA ONTO THE
5335 ;SYSTEM BUS.
5336
5337 014654 052737 000002 002234 9$: BIS      #CTSH,S0LOAD ;SETUP BIT TO BE LOADED
5338 014662 004737 010504 JSR      PC,LDRDS0 ;GO LOAD, READ AND CHECK CONTROL REG 2
5339 014666 001404 BEQ     10$ ;IF LOADED OK THEN CONTINUE
5340 014670 ERRDF 1,,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
5341 014670 104455 TRAP    C$ERDF
5342 014672 000001 .WORD 1
5343 014674 000000 .WORD 0
5344 014676 005304 .WORD S0EROR
5345 014700 10$: ENDSEG
  
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TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE

SEQ 0109

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5346 014700          10001$:
5347 014700 104405      TRAP    C$ESEG
5348
5349 014702 012701 015644      MOV    #30$,R1          ;GET POINTER TO ADDRESS AND DATA TABLES
5350
5351 014706          11$:      BGNSEG
5352 014706 104404      TRAP    C$BSEG
5353
5354                      ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5355                      ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5356
5357 014710 004737 012212      JSR    PC,SLCTTE
5358
5359                      ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
5360                      ;2:0 TO A 0. THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH THE
5361                      ;TEST PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6. THE DIAGNOSTIC
5362                      ;ADDRESS REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER
5363                      ;BIT 9 BEING SET TO A ONE PREVIOUSLY. ON A READ COMMAND TO CONTROL
5364                      ;REGISTER 6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
5365
5366 014714 004537 012232      JSR    R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
5367 014720 000000          .WORD  ADDR5           ;SELECT THE DIAG ADDRESS REG AND ADDR BUS
5368
5369                      ;LOAD READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A TEST PATTERN
5370                      ;TO SELECT ADDRESS 0 OF EACH BANK OF THE MEMORY SIMULATOR RAM. THE
5371                      ;ADDRESSES LOADED ARE AS FOLLOWS TO SELECT THE BANK OF MEMORY:
5372                      ; 000000 - SFLECTS 1ST 4K OF MEMORY SIMULATOR MEMORY
5373                      ; 020000 - SELECTS 2ND 4K OF MEMORY SIMULATOR MEMORY
5374                      ; 040000 - SELECTS 3RD 4K OF MEMORY SIMULATOR MEMORY
5375                      ; 060000 - SELECTS 4TH 4K OF MEMORY SIMULATOR MEMORY
5376                      ;EACH BANK OF MEMORY SIMULATOR MEMORY CONSISTS OF 2K WORDS OR 4K BYTES.
5377
5378 014722 011137 002346      MOV    (R1),T6LOAD     ;GET THE TEST PATTERN FROM THE TABLE
5379 014726 004737 011214      JSR    PC,LDRDT6      ;GO LOAD, READ AND CHECK DIAG ADDRESS REG
5380 014732 001405          BEQ    12$             ;IF LOADED OK THEN CONTINUE
5381 014734          ERRDF  12,ADDRRG,T06ERR ;DIAGNOSTIC ADDRESS REGISTER ERROR
5382 014734 104455          TRAP    C$ERRDF
5383 014736 000014          .WORD  12
5384 014740 004142          .WORD  ADDRRG
5385 014742 006730          .WORD  T06ERR
5386 014744          CKLOOP
5387 014744 104406          TRAP    C$CLP1
5388
5389                      ;SELECT HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3. THE
5390                      ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
5391                      ;CONTROL REGISTER 6.
5392
5393 014746 004537 012232      12$:  JSR    R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
5394 014752 000003          .WORD  HDAL           ;SELECT THE HDAL REGISTER
5395
5396                      ;RELOAD HDAL REGISTER BITS FOR SCOPE LOOPING PURPOSES ONLY. THIS IS
5397                      ;DONE TO SET ALL THE TIMING SIGNALS BACK TO THE NON-ASSERTED STATE.
5398
5399 014754 012737 001034 002346      MOV    #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;GET BITS PREVIOUSLY LOADED
5400 014762 004737 011214      JSR    PC,LDRDT6      ;LOAD, READ AND CHECK HDAL REGISTER
5401 014766 001405          BEQ    13$             ;IF LOADED OK THEN CONTINUE

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5402 014770 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
5403 014770 104455 TRAP C$ERDF
5404 014772 000014 .WORD 12
5405 014774 003754 .WORD HDALRG
5406 014776 006730 .WORD T06ERR
5407 015000 CKLOOP
5408 015000 104406 TRAP C$CLP1
5409
5410 ;START A T-11 MACHINE CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE
5411 ; 1. SET XRAS H AND PRAS H TO THE HIGH STATE
5412 ; 2. SET XCAS H AND PCAS H TO THE HIGH STATE
5413 ; 3. SET XPI L AND PPI L TO THE LOW STATE
5414 ;SETTING THE SIGNAL PRAS H TO THE HIGH STATE WILL CAUSE THE SIGNAL
5415 ;'ADVAL H' TO GO FROM A LOW TO A HIGH STATE, THUS CLOCKING THE SYSTEM
5416 ;ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR ADDRESS BUS LATCHES.
5417 ;SETTING THE SIGNAL XRAS H TO THE HIGH STATE WILL CAUSE THE SIGNALS
5418 ;EDCK0 H AND EDCK1 H TO GO FROM THE LOW STATE TO THE HIGH STATE, THUS
5419 ;CLOCKING SYSTEM ADDRESS BUS BITS 15:0 INTO THE STATE ANALYZERS ADDRESS
5420 ;BUS LATCHES FOR THESE BITS. SETTING THE SIGNAL XRAS H TO THE HIGH
5421 ;STATE WILL CAUSE THE RASP ONE SHOT TO BE FIRED, THUS CAUSING A PULSE
5422 ;TO BE ISSUED ON THE SIGNAL CKAI H. A PULSE ON CKAI H WILL CAUSE A
5423 ;PULSE ON THE SIGNAL EDCK5 H. THE SIGNAL EDCK5 H WILL CLOCK THE CTL 7:0
5424 ;SYSTEM BUS BITS INTO THE STATE ANALYZERS LATCHES FOR THESE BITS.
5425 ;SETTING THE SIGNAL XPI L TO THE LOW STATE WILL CAUSE THE SIGNAL EDCK4 H
5426 ;TO GO FROM THE LOW STATE TO THE HIGH STATE, THUS CLOCKING THE SYSTEM
5427 ;BUS SIGNALS CTL 11:8 AND BTS 3:0 INTO THE STATE ANALYZERS SYSTEM BUS
5428 ;LATCHES FOR THESE BITS. WHEN THE SIGNALS XRAS H AND XLAS H ARE ASSERTED
5429 ;HIGH, THE SIGNAL REAT H WILL GO FROM A LOW TO A HIGH STATE, THUS CAUSING
5430 ;THE SIGNAL READ H TO GO FROM A LOW TO A HIGH STATE. THE TARGET EMULATORS
5431 ;SIGNAL READ H ALONG WITH THE MEMORY SIMULATOR'S SIGNALS CTS H AND ESR H
5432 ;WILL CAUSE THE MEMORY SIMULATOR RAM DATA TO BE PUT ONTO THE SYSTEM DATA
5433 ;BUS. WHEN THE TARGET EMULATORS SIGNAL REAT H IS ASSERTED HIGH, THE
5434 ;TARGET EMULATORS SIGNAL MSDI H WILL BE ASSERTED HIGH, THUS ENABLING
5435 ;THE SYSTEM DATA BUS TO THE TARGET EMULATORS EODAL BUS. THE MEMORY
5436 ;SIMULATOR RAM'S ARE ADDRESSED BY THE MEMORY SIMULATOR SYSTEM BUS ADDRESS
5437 ;LATCHES WHICH WERE CLOCKED BY THE SIGNAL ADVAL H. THE DATA ON SYSTEM
5438 ;ADDRESS BUS COMES FROM THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER.
5439
5440 015002 004737 012276 13$: JSR PC,XRASH ;SET XRAS H AND PRAS H TO HIGH STATE
5441 015006 004737 012402 JSR PC,XCASH ;SET XCAS H AND PCAS H TO HIGH STATE
5442 015012 004737 012506 JSR PC,XPIH ;SET XPI H AND PPI H TO THE LOW STATE
5443
5444 ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H ARE
5445 ;ASSERTED HIGH (1'S).
5446
5447 015016 012737 000110 002342 MOV #VDAL6!VDAL3,T4GOOD ;EXPECT READ H AND MSDI H TO BE ONES
5448 015024 004737 011176 JSR PC,READT4 ;READ VDAL AND PAUSE STATE MACHINE REG
5449 015030 001405 BEQ 14$ ;IF DATA OK THEN CONTINUE
5450 015032 ERRDF 11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
5451 015032 104455 TRAP C$ERDF
5452 015034 000013 .WORD 11
5453 015036 003706 .WORD VDALRG
5454 015040 006714 .WORD T4EROR
5455 015042 CKLOOP
5456 015042 104406 TRAP C$CLP1
5457
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5458                                     :SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5459                                     :REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5460
5461 015044 004737 011246      14$: JSR      PC,SLCTMS                ;SELECT THE MEMORY SIMULATOR MODULE
5462
5463                                     :READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
5464                                     :TARGET EMULATOR MODULE SET THE SIGNALS ADVAL H AND READ H TO THE
5465                                     :HIGH STATE FROM THE LOW STATE.
5466
5467 015050 004737 010520      JSR      PC,READS0                ;READ AND CHECK CONTROL REGISTER 0
5468 015054 001405      BEQ      15$                    ;IF NO CHANGES THEN CONTINUE
5469 015056      ERRDF 1,S0EROR                ;CONTROL REGISTER 0 NOT = EXPECTED
5470 015056 104455      TRAP    C$ERRDF
5471 015060 000001      .WORD   1
5472 015062 000000      .WORD   0
5473 015064 005304      .WORD   S0EROR
5474 015066      CKLOOP
5475 015066 104406      TRAP    C$CLP1
5476
5477                                     :READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
5478                                     :SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
5479                                     :SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H. THE SIGNAL ADVAL H
5480                                     :WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
5481                                     :SIGNAL PRAS H WAS SET HIGH FROM THE LOW STATE. THE MEMORY SIMULATORS
5482                                     :SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
5483                                     :BITS VIA THE SIGNALS CTS H AND CTS L.
5484
5485 015070 011137 000054      15$: MOV      (R1),S4LOAD                ;GET TE DIAG ADDRESS REG DATA LOADED
5486 015074 004737 010612      JSR      PC,READS4                ;READ AND CHECK CONTROL REGISTER 4
5487 015100 001405      BEQ      16$                    ;IF DATA = TE DIAG ADDRESS REG - CONT
5488 015102      ERRDF 3,TEMSAD,S04ERR        ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
5489 015102 104455      TRAP    C$ERRDF
5490 015104 000003      .WORD   3
5491 015106 002532      .WORD   TEMSAD
5492 015110 005404      .WORD   S04ERR
5493 015112      CKLOOP
5494 015112 104406      TRAP    C$CLP1
5495
5496                                     :READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
5497                                     :ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
5498                                     :ZEROS FOR THESE TWO ADDRESSES. ADDRESS BITS 17 AND 16 WERE CLOCKED
5499                                     :INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
5500                                     :ADVAL H. THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
5501                                     :MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE FROM
5502                                     :THE LOW STATE. THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
5503                                     :ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
5504                                     :MEMORY SIMULATOR MODULE.
5505
5506 015114 052737 000014 002250 16$: BIS      #MSEL0!MSEL1,S2MASK        ;IGNORE TRI-STATE BIT WHEN CTS H SET
5507 015122 005037 002244      CLR      S2LOAD                    ;EXPECT MSAD 17:16 TO BE ZERO
5508 015126 013737 002244 002246      MOV      S2LOAD,S2GOOD            ;COPY DATA LOADED TO EXPECTED
5509 015134 052737 000140 002246      BIS      #ESRH!WRENH,S2GOOD        ;EXPECT MAP PROTECT BITS TO BE ONES
5510 015142 004737 010560      JSR      PC,READS2                ;READ AND CHECK CONTROL REGISTER 2
5511 015146 001405      BEQ      17$                    ;IF DATA OK THEN CONTINUE
5512 015150      ERRDF 2,TEMSA1,S02ERR        ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
5513 015150 104455      TRAP    C$ERRDF

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5514 015152 000002      .WORD 2
5515 015154 002406      .WORD TEMSA1
5516 015156 005364      .WORD S02ERR
5517 015160             CKLOOP
5518 015160 104406      TRAP C$CLP1
5519
5520             ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
5521             ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5522
5523 015162 004737 012142 17$: JSR PC,SLCTED             ;SELECT STATE ANALYZER MODULE
5524
5525             ;SET THE SIGNAL TRSL2 L TO THE LOW STATE BY SETTING CDAL REGISTER BIT
5526             ;3 TO A ONE AND CDAL REGISTER BIT 2 TO A ZERO. THE SIGNAL TRSL2 L WILL
5527             ;ENABLE THE STATE ANALYZER'S SYSTEM BUS LATCHES TO THE EVENT DETECTORS
5528             ;TRDI 59:0 BUS.
5529
5530 015166 112737 000010 002272 MOVB #CDAL3,E0LOAD             ;SETUP BITS TO SET TRSL2 L TO LOW STATE
5531 015174 004737 010676 JSR PC,LDRDE0             ;GO LOAD, READ AND CHECK CONTROL REG 0
5532 015200 001405 BEQ 18$             ;IF LOADED OK THEN CONTINUE
5533 015202 ERRDF 5,CDALRG,E0EROR             ;CDAL REGISTER NOT EQUAL EXPECTED
5534 015202 104455 TRAP C$ERDF
5535 015204 000005 .WORD 5
5536 015206 003006 .WORD CDALRG
5537 015210 006144 .WORD E0EROR
5538 015212 CKLOOP
5539 015212 104406 TRAP C$CLP1
5540
5541             ;ASSERT THE SIGNAL PTER1 L IN THE POINTER REGISTER BY LOADING THE
5542             ;APPROPRIATE BITS IN THE PDAL REGISTER (CONTROL REGISTER 2)
5543
5544 015214 004537 012162 18$: JSR R5,LDPDAL             ;LOAD AND CHECK PDAL REG WITH NEXT WORD
5545 015220 000001 .WORD PTER1             ;SETUP TO READ TRDI BUS BITS 15:0
5546
5547             ;AS A RESULT OF SETTING THE SIGNAL "XRAS H" TO THE HIGH STATE ON THE
5548             ;TARGET EMULATOR MODULE, THE TARGET EMULATOR'S ADDRESS BUS WAS CLOCKED
5549             ;INTO THE STATE ANALYZER'S ADDRESS LATCHES VIA THE CLOCKING SIGNALS
5550             ;"EDCK0 H" AND "EDCK1 H". THE PROGRAM HAS ALREADY ASSERTED THE SIGNAL
5551             ;"TRSL2 L" WHICH WILL ENABLE THE SYSTEM BUS LATCHES ONTO THE STATE
5552             ;ANALYZER'S TRDI 59:0 BUS. WHEN THE PROGRAM ISSUES A READ COMMAND TO
5553             ;CONTROL REGISTER 6 AND THE PDAL REGISTER IS SETUP TO SELECT PTER1 L,
5554             ;A PULSE WILL BE ISSUED ON THE SIGNAL RPT1 L. THIS SIGNAL WILL READ
5555             ;TRDI BUS BITS 15:0 WHICH ARE THE ADDRESS LATCHES FOR SYSTEM BUS
5556             ;ADDRESSES 15:0.
5557
5558 015222 011137 002316 MOV (R1),E6LOAD             ;GET DATA LOADED INTO TARGET EMULATOR
5559 015226 005037 002320 CLR E6MASK             ;SETUP TO READ ALL 16 BITS
5560 015232 004737 011052 JSR PC,READE6             ;READ ADDRESSES 15:0 ON TRDI 15:0
5561 015236 001405 BEQ 19$             ;IF OK THEN CONTINUE
5562 015240 ERRDF 8,TEEDAD,E026ER             ;TE TO SA ADDRESS BUS ERROR - TRDI 15:0
5563 015240 104455 TRAP C$ERDF
5564 015242 000010 .WORD 8
5565 015244 003171 .WORD TEEDAD
5566 015246 006210 .WORD E026ER
5567 015250 CKLOOP
5568 015250 104406 TRAP C$CLP1
5569

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5570 ;ASSERT THE SIGNAL 'PTER3 L' IN THE POINTER REGISTER BY LOADING THE
5571 ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.
5572
5573 015252 004537 012162 19$: JSR R5,LDPDAL ;LOAD AND CHECK PDAL REG WITH NEXT WORD
5574 015256 000003 .WORD PTER3 ;SETUP TO READ TRDI BUS BITS 47:32
5575
5576 ;AS A RESULT OF PULSES ON THE TARGET EMULATOR'S SIGNALS 'RASP L' AND
5577 ;'XPI L', PULSES SHOULD HAVE OCCURED ON THE SIGNALS 'EDCK5 H' AND
5578 ;'EDCK4 H' RESPECTIVELY. THE PULSE 'EDCK5 H' WILL CLCOK THE CTL SYSTEM
5579 ;BUS BITS 7:0 INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES FOR THESE
5580 ;BITS. THESE BITS WILL BE READ ONTO THE STATE ANALYZERS TRDI BUS BITS
5581 ;47:40. THIS TEST WILL NOT CHECK THESE BITS AT THIS TIME. THE PULSE,
5582 ;'EDCK4 H', WILL CLOCK SYSTEM BUS ADDRESS BITS 17 AND 16, AND THE TARGET
5583 ;EMULATOR'S SIGNALS BTS 3:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES
5584 ;FOR THESE BITS. THESE BITS WILL BE READ ONTO THE STATE ANALYZERS TRDI
5585 ;BUS BITS 39:32. TRDI BITS 47:40 WILL BE IGNORED DURING THIS TEST.
5586
5587 015260 005037 002316 CLR E6LOAD ;EXPECT TRDI BITS 39:32 TO BE ZERO
5588 015264 012737 177400 002320 MOV #177400,E6MASK ;SETUP TO IGNORE UNWANTED BITS
5589 015272 004737 011052 JSR PC,READE6 ;READ BTS 3:0 + ADDR 17:16 ON TRDI 39:32
5590 015276 001405 BEQ 20$ ;IF OK THEN CONTINUE
5591 015300 ERRDF 8,TEEDA1,E026ER ;TE TO SA XSEL1,EDSELO,ADDR 17:16 + BTS 3:0 ERRO
5592 015300 104455 TRAP C$ERDF
5593 015302 000010 .WORD 8
5594 015304 003240 .WORD TEEDA1
5595 015306 006210 .WORD E026ER
5596 015310 CKLOOP
5597 015310 104406 TRAP C$CLP1
5598
5599 ;ASSERT THE SIGNAL 'PTERO L' IN THE POINTER REGISTER BY LOADING THE
5600 ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER. ON A WRITE
5601 ;OR READ COMMAND TO CONTROL REGISTER 6 WHEN PTERO L IS ASSERTED, THE
5602 ;TRACE RAM ADDRESS REGISTER WILL BE WRITTEN AND READ. PDAL REGISTER
5603 ;BIT 6 WILL ALSO BE SET TO A ONE TO CAUSE THE TRACING FLIP-FLOP TO
5604 ;BE SET TO THE ONE STATE. THIS IS DONE SO THAT A PULSE WILL BE ISSUED
5605 ;ON THE SIGNAL 'CTR L' LATER ON IN THIS TEST WHEN THE TARGET EMULATOR'S
5606 ;SIGNAL 'EDEOC H' IS SET TO A ONE.
5607
5608 015312 004537 012162 20$: JSR R5,LDPDAL ;LOAD AND CHECK PDAL REG WITH NEXT WORD
5609 015316 000100 .WORD PDAL6!PTERO ;SETUP TO WRITE/READ TRAM ADDRESS REG
5610
5611 ;LOAD, READ AND CHECK THE TRACE RAM ADDRES REGISTER WITH A DATA PATTERN
5612 ;OF ALL ONES (3777). WHEN THE SIGNAL 'EDEOC H' IS SET TO A ONE LATER IN
5613 ;THIS TEST, THE TRACE RAM ADDRESS REGISTER SHOULD BE INCREMENTED TO
5614 ;ZERO BY THE CLOCKING SIGNAL EDEOC H.
5615
5616 015320 012737 174000 002320 MOV #174000,E6MASK ;SETUP TO IGNORE UNUSED BITS
5617 015326 012737 003777 002316 MOV #3777,E6LOAD ;SETUP TO LOAD ALL ONES
5618 015334 004737 011044 JSR PC,LDRDE6 ;LOAD READ AND CHECK TRAM ADDRESS REG
5619 015340 001404 BEQ 21$ ;IF LOADED OK THEN CONTINUE
5620 015342 ERRDF 8,TRADRS,E026ER ;TRACE RAM ADDRESS REG NOT = 3777
5621 015342 104455 TRAP C$ERDF
5622 015344 000010 .WORD 8
5623 015346 003475 .WORD TRADRS
5624 015350 006210 .WORD E026ER
5625

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TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE

SEQ 0114

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5626 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5627 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5628
5629 015352 004737 012212 21$: JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE
5630
5631 ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO A 7. THE EODAL BUS
5632 ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
5633
5634 015356 004537 012232 JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
5635 015362 000007 .WORD EODAL ;SELECT THE EODAL BUS TO BE READ
5636
5637 ;AT THIS TIME THE MEMORY SIMULATOR RAM DATA SHOULD BE ENABLED ON THE
5638 ;SYSTEM DATA BUS AND ENABLED TO THE TARGET EMULATORS EODAL BUS VIA THE
5639 ;TARGET EMULATOR SIGNALS READ H AND MSDI H RESPECTIVELY. THE MEMORY
5640 ;SIMULATOR RAM IS ADDRESSED BY THE TARGET EMULATORS DIAGNOSTIC ADDRESS
5641 ;REGISTER WHICH WAS CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS
5642 ;BUS LATCHES VIA THE SIGNAL ADVAL H. THE ADDRESSES AND DATA PATTERNS
5643 ;STORED IN THE RAM ADDRESSES SELECTED ARE AS FOLLOWS
5644 : RAM ADDRESS 000000 WAS LOADED WITH 125252
5645 : RAM ADDRESS 020000 WAS LOADED WITH 052525
5646 : RAM ADDRESS 040000 WAS LOADED WITH 177777
5647 : RAM ADDRESS 060000 WAS LOADED WITH 000000
5648
5649 015364 016137 000010 002346 MOV 10(R1),T6LOAD ;GET DATA LOADED INTO MS RAM ADDRESSED
5650 015372 004737 011222 JSR PC,READT6 ;READ SYSTEM DATA BUS ON THE EODAL BUS
5651 015376 001405 BEQ 22$ ;IF DATA = MS RAM DATA THEN CONTINUE
5652 015400 ERRDF 12,MSTEDE,T6ALLR ;MS RAM DATA TO TE EODAL BUS ERROR
5653 015400 104455 TRAP C$ERDF
5654 015402 000014 .WORD 12
5655 015404 004241 .WORD MSTEDE
5656 015406 006744 .WORD T6ALLR
5657 015410 CKLOOP
5658 015410 104406 TRAP C$CLP1
5659
5660 ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6. THE EIDAL BUS
5661 ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
5662
5663 015412 004537 012232 22$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
5664 015416 000006 .WORD EIDAL ;SELECT THE EIDAL BUS TO BE READ
5665
5666 ;IN THE PREVIOUS DATA CHECK, THE PROGRAM VERIFIED THAT THE MEMORY SIMU-
5667 ;LATOR RAM DATA WAS ENBALED TO THE EODAL BUS VIA THE SYSTEM DATA BUS.
5668 ;IN THIS SECTION, THE PROGRAM WILL CHECK THAT THE EODAL BUS IS ENABLED
5669 ;TO THE EIDAL BUS VIA THE CDAL BUS AS A RESULT OF THE SIGNALS COHB L AND
5670 ;COLB L BEING ASSERTED LOW. THE SIGNALS COHB L AND COLB L ARE ASSERTED
5671 ;LOW AS A RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED HIGH: ETR L,
5672 ;PR/WLB H, PR/WHB H, PPI H, DMG L, AND MR11 L. THE DATA READ SHOULD BE
5673 ;THE SAME AS THAT WHICH WAS ENABLED TO THE EODAL BUS. THE ADDRESSES
5674 ;AND DATA PATTERNS STORED IN THE RAM ADDRESSES SELECTED ARE AS FOLLOWS:
5675 : RAM ADDRESS 000000 WAS LOADED WITH 125252
5676 : RAM ADDRESS 020000 WAS LOADED WITH 052525
5677 : RAM ADDRESS 040000 WAS LOADED WITH 177777
5678 : RAM ADDRESS 060000 WAS LOADED WITH 000000
5679
5680 015420 016137 000010 002346 MOV 10(R1),T6LOAD ;GET DATA LOADED INTO MS RAM ADDRESSED
5681 015426 004737 011222 JSR PC,READT6 ;READ SYSTEM DATA BUS ON EIDAL VIA EODAL

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5682 015432 001405      BEQ      23$      ;IF DATA OK THEN CONTINUE
5683 015434             ERRDF    12,MSTEEI,T6ALLR ;MS RAM DATA TO EIDAL BUS VIA EODAL BUS
5684 015434 104455      TRAP    C$ERDF
5685 015436 000014      .WORD   12
5686 015440 004327      .WORD   MSTEEI
5687 015442 006744      .WORD   T6ALLR
5688 015444             CKLOOP
5689 015444 104406      TRAP    C$CLP1
5690
5691                    ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
5692                    ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
5693                    ;REGISTER 6.
5694
5695 015446 004537 012232 23$: JSR      R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
5696 015452 000003      .WORD   HDAL      ;SELECT THE HDAL REGISTER
5697
5698                    ;FINISH THE T-11 TIMING CYCLE BY DOING THE FOLLOWING SEQUENCE:
5699                    ; 1. SET XCAS H AND PCAS H TO THE LOW STATE
5700                    ; 2. SET XPI L AND PPI L TO THE HIGH STATE
5701                    ; 3. SET XRAS H AND PRAS H TO THE LOW STATE
5702                    ;SETTING THE SIGNAL XCAS H TO THE LOW STATE AND XCAS L TO THE HIGH STATE
5703                    ;WILL CAUSE THE SIGNALS EDCK2 H AND EDCK3 H TO BE SET HIGH FROM THE LOW
5704                    ;STATE, THUS CAUSING THE SYSTEM DATA BUS TO BE CLOCKED INTO THE STATE
5705                    ;ANALYZERS SYSTEM DATA BUS LATCHES.
5706
5707 015454 012737 001034 002346 MOV     #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SETUP PREVIOUSLY LOADED BITS
5708 015462 004737 012434 JSR     PC,XCASL ;SET XCAS H AND PCAS H TO LOW STATE
5709 015466 004737 012540 JSR     PC,XPIL ;SET XPI L AND PPI L TO THE HIGH STATE
5710 015472 004737 012330 JSR     PC,XRASL ;SET XRAS H AND PRAS H TO LOW STATE
5711
5712                    ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H
5713                    ;WENT TO A ZERO AS A RESULT OF SETTING THE SIGNALS XCAS H AND XRAS H
5714                    ;TO THE LOW STATE. CHECK THAT THE SIGNAL EDEOC H WHEN TO A ONE AS
5715                    ;A RESULT OF XRAS H AND XCAS H BEING SET LOW AND THE SINGLE STEP SYNC
5716                    ;FLIP-FLOP BEING SET TO A ONE VIA XCAS H.
5717
5718 015476 012737 000020 002342 MOV     #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE SET TO A ONE
5719 015504 004737 011176 JSR     PC,READT4 ;READ AND CHECK VDAL REGISTER
5720 015510 001405      BEQ      24$      ;IF OK THEN CONTINUE
5721 015512             ERRDF    11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
5722 015512 104455      TRAP    C$ERDF
5723 015514 000013      .WORD   11
5724 015516 003706      .WORD   VDALRG
5725 015520 006714      .WORD   T4EROR
5726 015522             CKLOOP
5727 015522 104406      TRAP    C$CLP1
5728
5729                    ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
5730                    ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5731
5732 015524 004737 012142 24$: JSR     PC,SLCTED ;SELECT STATE ANALYZER MODULE
5733
5734                    ;ASSERT THE SIGNAL 'PTER2 L' IN THE POINTER REGISTER BY LOADING THE
5735                    ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER
5736
5737 015530 004537 012162 JSR     R5,LDPDAL ;LOAD AND CHECK PDAL REG WITH NEXT WORD

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5738 015534 000002      .WCRD  PTER2                ;SETUP TO READ TRDI BUS BITS 31:16
5739
5740                  ;TARGET EMULATOR SIGNALS EDCK2 H AND EDCK3 H WERE SET HIGH AS A RESULT
5741                  ;OF THE TARGET EMULATOR SIGNAL XCAS L BEING SET HIGH.  THE SIGNALS
5742                  ;EDCK2 H AND EDCK3 H WILL CLOCK THE SYSTEM DATA BUS INTO THE STATE
5743                  ;ANALYZERS SYSTEM DATA BUS LATCHES FOR THESE BITS.  THESE BITS WILL
5744                  ;BE READ ON THE STATE ANALYZERS TRDI BUS BITS 31:16.  THE DATA WAS PUT
5745                  ;ONTO THE SYSTEM DATA BUS DURING A READ OPERATION TO THE MEMORY
5746                  ;SIMULATOR MODULE.  ON A READ COMMAND TO STATE ANALYZERS CONTROL
5747                  ;REGISTER 6, THE SIGNAL RPT2 H WILL BE GENERATED THUS READING TRDI
5748                  ;SYSTEM BUS LATCHES FOR BITS 31:16.  THE ADDRESSES AND DATA PATTERNS
5749                  ;STORED IN THE RAM ADDRESSES SELECTED ARE AS FOLLOWS:
5750                  ;
5751                  ;      RAM ADDRESS 000000 WAS LOADED WITH 125252
5752                  ;      RAM ADDRESS 020000 WAS LOADED WITH 052525
5753                  ;      RAM ADDRESS 040000 WAS LOADED WITH 177777
5754                  ;      RAM ADDRESS 060000 WAS LOADED WITH 000000
5755 015536 016137 000010 002316  MOV    10(R1),E6LOAD        ;GET MS DATA LOADED INTO RAM
5756 015544 005037 002320          CLR    E6MASK              ;SETUP TO READ ALL 16 BITS
5757 015550 004737 011052          JSR    PC,READE6          ;READ SYSTEM DATA BUS LATCHES - TRDI 31:16
5758 015554 001405          BEQ    25$                ;IF OK THEN CONTINUE
5759 015556          ERRDF  8,MSEDDE,E026ER      ;MS RAM DATA TO SA TRDI 31:16 BUS ERROR
5760 015556 10          TRAP  C$ERRDF
5761 015560 000010          .WORD  8
5762 015562 003421          .WORD  MSEDDE
5763 015564 006210          .WORD  E026ER
5764 015566          CKLOOP
5765 015566 104406          TRAP  C$CLP1
5766
5767                  ;ASSERT THE SIGNAL 'PTERO L' IN THE POINTER REGISTER BY LOADING THE
5768                  ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.  ON A READ
5769                  ;COMMAND TO CONTROL REGISTER 6 WITH PTERO L ASSERTED LOW, THE TRACE
5770                  ;RAM ADDRESS REGISTER WILL BE READ VIA THE SIGNAL 'RPTO H'.
5771
5772 015570 004537 012162          25$: JSR    R5,LDPDAL          ;LOAD AND CHECK PDAL REG WITH NEXT WORD
5773 015574 000000          .WORD  PTERO              ;SELECT TRAM ADDRESS REG TO BE READ
5774
5775                  ;CHECK THAT THE TRACE RAM ADDRESS REGISTER WAS INCREMENTED TO ZERO BY
5776                  ;A PULSE BEING ISSUED ON THE SIGNAL 'CTR L'.  THE TRACE RAM ADDRESS
5777                  ;REGISTER WAS LOADED WITH ALL ONES (3777) EARLIER IN THIS TEST SECTION.
5778                  ;WHEN THE TARGET EMULATOR'S SIGNAL XCAS L WAS SET TO THE HIGH STATE BY
5779                  ;SETTING XCAS H TO THE LOW STATE, THE SIGNAL 'EDEOC H' SHOULD GO FROM
5780                  ;A LOW TO A HIGH STATE.  WHEN THE SIGNAL 'EDEOC H' GOES FROM A LOW TO
5781                  ;A HIGH STATE, THE STATE ANALYZER SIGNAL 'TRANST H' SHOULD ALSO GO FROM
5782                  ;A LOW TO A HIGH STATE.  WHEN THE SIGNAL 'TRANST H' GOES TO THE HIGH
5783                  ;STATE, THE TRACE WRITE WIDTH ONE SHOT WILL BE FIRED.  AS A RESULT OF
5784                  ;THE TRACING FLIP-FLOP BEING SET TO A ONE VIA PDAL6 H AND THE TRACE
5785                  ;WRITE WIDTH ONE SHOT BEING FIRED, A PULSE SHOULD OCCUR ON THE SIGNAL
5786                  ;'CTR L'.  A PULSE ON 'CTR L' WILL INCREMENT THE TRACE RAM ADDRESS
5787                  ;REGISTER BY ONE THUS CLCOKING THE TRACE RAM ADDRESS REGISTER FROM
5788                  ;ALL ONES TO ALL ZEROES.
5789
5790 015576 005037 002316          CLR    E6LOAD              ;EXPECT TRAM ADDRESS REGISTER TO BE 0
5791 015602 012737 174000 002320  MOV    #174000,E6MASK      ;SETUP TO IGNORE UNUSED BITS
5792 0156 0 004737 011052          JSR    PC,READE6          ;READ AND CHECK TRAM ADDRESS REGISTER
5793 0156 4 001404          BEQ    26$                ;IF 0 THEN CONTINUE
  
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TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE

SEQ 0117

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5794 015616 ERRDF 8,TRADRS,E026ER ;CTR L DIDN'T +1 TRAM ADDRESS REGISTER
5795 015616 104455 TRAP C$ERDF
5796 015620 000010 .WORD 8
5797 015622 003475 .WORD TRADRS
5798 015624 006210 .WORD E026ER
5799 015626 26$: ENDSEG
5800 015626 10003$:
5801 015626 104405 TRAP C$ESEG
5802
5803 015630 005761 000010 TST 10(R1) ;CHECK IF THIS WAS LAST DATA PATTERN
5804 015634 001413 BEQ 31$ ;IF YES THEN END OF TEST
5805 015636 005721 TST (R1)+ ;UPDATE POINTER TO ADDRESS TABLE
5806 015640 000137 014706 JMP 11$ ;GO CHECK NEXT DATA PATTERN
5807
5808 ;DATA PATTERN FOR ADDRESS BITS 15:0 TO BE LOADED INTO DIAGNOSTIC ADDRESS
5809 ;REGISTER.
5810
5811 015644 000000 30$: .WORD 000000
5812 015646 020000 .WORD 020000
5813 015650 040000 .WORD 040000
5814 015652 060000 .WORD 060000
5815
5816 ;DATA PATTERN FOR ADDRESS 0 OF EACH 4K MEMORY SIMULATOR RAM
5817
5818 015654 125252 .WORD 125252
5819 015656 052525 .WORD 052525
5820 015660 177777 .WORD 177777
5821 015662 000000 .WORD 000000
5822
5823 015664 31$: ENDTST
5824 015664 L10037:
5825 015664 104401 TRAP C$ETST
5826
    
```


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SEQ 0119

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5883                                     ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
5884
5885 015700 012737 043020 002334      MOV    #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
5886 015706 004737 012764              JSR    PC,BRKRES                       ;SET BITS 14, 10 + 9 AND TOGGLE ADALO H
5887
5888                                     ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
5889                                     ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
5890                                     ;REGISTER 6.
5891
5892 015712 004537 012232              JSR    R5,SELTER                       ;SELECT REGISTER SPECIFIED BY NEXT WORD
5893 015716 000003                      .WORD  HDAL                            ;SELECT THE HDAL REGISTER
5894
5895                                     ;SET HDAL REGISTER BITS 9,3 + 2 TO A ONE AND HDAL BITS 14 AND 11 TO A
5896                                     ;ZERO. HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
5897                                     ;AND CONTROL SIGNALS. HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
5898                                     ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS. HDAL REGISTER
5899                                     ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
5900                                     ;HDAL REGISTER BIT 4 ON A ZERO AND BIT3 ON A ONE WILL SET THE SIGNAL
5901                                     ;XR/WHB H LOW AND XR/WLB H HIGH RESPECTIVELY. THESE TWO SIGNALS SET TO
5902                                     ;THIS STATE WILL CAUSE THE SIGNAL 'REAT H' TO BE ASSERTED HIGH LATER IN
5903                                     ;THIS TEST WHEN THE SIGNALS XRAS H AND XCAS H ARE ASSERTED HIGH.
5904
5905 015720 012737 001014 002346      MOV    #HDAL9!HDAL3!HDAL2,T6LOAD ;SET HDAL BITS 9,3 + 2 TO ONES
5906 015726 005037 002352              CLR    T6MASK                          ;SETUP MASK TO CHECK ALL BITS
5907 015732 004737 011214              JSR    PC,LDRDT6                       ;GO LOAD, READ AND CHECK HDAL REGISTER
5908 015736 001405                      BEQ    1$                               ;IF LOADED OK THEN CONTINUE
5909 015740                              ERRDF  12,HDALRG,T06ERR                ;HDAL REGISTER NOT EQUAL EXPECTED
5910 015740 104455                      TRAP   C$ERRDF
5911 015742 000014                      .WORD  12
5912 015744 003754                      .WORD  HDALRG
5913 015746 006730                      .WORD  T06ERR
5914 015750                              CKLOOP
5915 015750 104406                      TRAP   C$CLP1
5916
5917                                     ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
5918                                     ;REGISTER 4. PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
5919                                     ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L'.
5920
5921 015752 005037 002340 1$:          CLR    T4LOAD                          ;SETUP TO CLEAR ALL OTHER R/W BITS
5922 015756 004737 012704              JSR    PC,CLRPSM                       ;PULSE INVD L VIA VDAL2 H
5923
5924                                     ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4. ON
5925                                     ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
5926                                     ;BE WRITTEN OR READ.
5927
5928 015762 004537 012232              JSR    R5,SELTER                       ;SELECT REGISTER SPECIFIED BY NEXT WORD
5929 015766 000004                      .WORD  MODE                            ;SELECT THE MODE REGISTER
5930
5931                                     ;LOAD, READ AND CHECK MODE REGISTER WITH MODE REGISTER BIT 11 SET TO A
5932                                     ;ONE AND ALL OTHER MODE REGISTER BITS SET TO A ZERO. WHEN MODE REGISTER
5933                                     ;BIT 11 IS SET TO A ONE, 8 BIT MODE IS SELECTED.
5934
5935 015770 012737 004000 002346      MOV    #MR11,T6LOAD                   ;SETUP BIT TO SELECT 8 BIT MODE
5936 015776 004737 011214              JSR    PC,LDRDT6                       ;GO LOAD, READ AND CHECK MODE REGISTER
5937 016002 001405                      BEQ    2$                               ;IF LOADED OK THEN CONTINUE
5938 016004                              ERRDF  12,MODREG,T06ERR                ;MODE REGISTER NOT EQUAL EXPECTED

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5939 016004 104455 TRAP C$ERDF
5940 016006 000014 .WORD 12
5941 016010 004000 .WORD MODREG
5942 016012 006730 .WORD T06ERR
5943 016014 CKLOOP
5944 016014 104406 TRAP C$CLP1
5945
5946 ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
5947 ;TO A 2. THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
5948 ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
5949 ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
5950 ;TER WILL BE ADDRESSED.
5951
5952 016016 004537 012232 2$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
5953 016022 000002 .WORD FDAL ;SELECT EOAI AND FDAL REGISTER
5954
5955 ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER. THE EOAI REGISTER WILL
5956 ;BE LOADED AND CHECKED FOR ZEROES. THE FDAL REGISTER WILL BE LOADED AND
5957 ;CHECKED FOR A DATA PATTERN OF ONE (FDALO H = 1).
5958
5959 016024 012737 000001 002346 MOV #FDALO,T6LOAD ;SETUP EOAI AND FDAL REG DATA PATTERN
5960 016032 004737 01214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK EOAI + FDAL REG
5961 016036 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
5962 016040 ERRDF 12,EOAIFD,T06ERR ;EOAI OR FDAL REGISTER ERROR
5963 016040 104455 TRAP C$ERDF
5964 016042 000014 .WORD 12
5965 016044 004045 .WORD EOAIFD
5966 016046 006730 .WORD T06ERR
5967 016050 CKLOOP
5968 016050 104406 TRAP C$CLP1
5969
5970 ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
5971 ;CHANGES OCCURED DOING THE PAST SEQUENCES.
5972
5973 016052 004737 011176 3$: JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
5974 016056 001404 BEQ 4$ ;IF NO CHANGES THEN CONTINUE
5975 016060 ERRDF 11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
5976 016060 104455 TRAP C$ERDF
5977 016062 000013 .WORD 11
5978 016064 003706 .WORD VDALRG
5979 016066 006714 .WORD T4EROR
5980 016070 4$: ENDSEG
5981 016070 10000$: TRAP C$ESEG
5982 016070 104405
5983
5984 016072 BGNSEG
5985 016072 104404 TRAP C$BSEG
5986
5987 ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5988 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5989
5990 016074 004737 011246 JSR PC,SLCTMS ;SELECT MEMORY SIMULATOR MODULE
5991
5992 ;GO LOAD, READ AND CHECK THE MEMORY SIMULATOR MAP PROTECTION RAM. THE
5993 ;MAP PROTECTION RAM WILL HAVE THE BITS 'MUTB H' AND 'MPIN H' SET TO
5994 ;ONES FOR ALL ADDRESSES IN THE MAP PROTECTION RAM. MAP PROTECTION RAM

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SEQ 0121

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5995 ;BITS 'WRE H' AND 'RDE H' WILL BE SET TO ONES FOR THE FIRST 16K WORDS OF
5996 ;MEMORY SIMULATOR RAM AND TO ZEROES FOR ALL ADDRESSES ABOVE 16K WORDS.
5997 ;WHEN 'RDE H' AND 'WRE H' ARE SET TO ONES, READ AND WRITES ARE ALLOWED
5998 ;TO THOSE ADDRESSES.
5999
6000 016100 004737 011354 JSR PC,MPRAM ;GO LOAD, READ AND CHECK MAP PROTECT RAM
6001
6002 ;GO LOAD, READ AND CHECK MODULE SELECT RAM 0. THE FOLLOWING DATA
6003 ;PATTERNS: 1, 2, 4, 10, 0, 0, 0, AND 0 WILL BE LOADED INTO CONSECUTIVE
6004 ;LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS 0. THESE PATTERNS
6005 ;WILL ENABLE THE FIRST 16K WORDS OF THE MEMORY SIMULATOR RAM TO BE
6006 ;ADDRESSED.
6007
6008 016104 004737 011640 JSR PC,MSRAM0 ;LOAD, READ AND CHECK MODULE SELECT RAM 0
6009
6010 ;GO LOAD, READ AND CHECK MODULE SELECT RAM 1. THE FOLLOWING DATA PATTERNS
6011 ;WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
6012 ;AT ADDRESS 0; 17, 0, 0 AND 0. THESE PATTERNS WILL ENABLE THE FIRST 32K
6013 ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
6014
6015 016110 004737 012010 JSR PC,MSRAM1 ;LOAD, READ AND CHECK MODULE SELECT RAM 1
6016
6017 016114 005037 002254 CLR S4LOAD ;START ADDRESS AT ADDRESS ZERO
6018 016120 012737 125125 002260 MOV #125125,S6LOAD ;DATA PATTERN FOR ADDRESS ZERO
6019
6020 016126 5$: BGNSEG
6021 016126 104404 TRAP C$BSEG
6022
6023 ;LOAD MEMORY SIMULATOR RAM ADDRESS TO BE TESTED INTO CONTROL REGISTER 4.
6024 ;ADDRESSES TO BE LOADED ARE 0, 20000, 40000 AND 60000.
6025
6026 016130 004737 010604 JSR PC,LDRDS4 ;LOAD READ AND CHECK CONTROL REG 4
6027 016134 001405 BEQ 6$ ;IF LOADED OK THEN CONTINUE
6028 016136 ERRDF 3,MSADRG,S4EROR ;MSAD 15:0 REGISTER ERROR
6029 016136 104455 TRAP C$ERDF
6030 016140 000003 .WORD 3
6031 016142 002506 .WORD MSADRG
6032 016144 005334 .WORD S4EROR
6033 016146 CKLOOP
6034 016146 104406 TRAP C$CLP1
6035
6036 ;CLEAR BITS MSEL1 H, MSEL0 H, MSAD17 H AND MSAD16 H IN CONTROL REGISTER
6037 ;2. MSEL0 H AND MSEL1 H ON A ZERO WILL CAUSE THE SIGNAL "SSM L" TO BE
6038 ;ASSERTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6. ON A WRITE
6039 ;OR READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE WRITTEN INTO OR
6040 ;READ FROM MEMORY SIMULATOR RAM ADDRESSES BY CONTROL REGISTER 2 AND 4.
6041 ;THE MEMORY SIMULATOR RAM'S ARE ENABLED BY THE DATA PATTERNS PREVIOUSLY
6042 ;WRITTEN INTO MODULE SELECT RAMS 0 AND 1. MSAD17 H AND MSAD16 H WILL BE
6043 ;LOADED AND CHECKED WITH ZEROES. THE PROGRAM WILL EXPECT CONTROL REGIS-
6044 ;TER 2 BITS 'ESR H' AND 'WREN H' TO BE READ AS ONES AS A RESULT OF MAP
6045 ;PROTECTION RAM BITS 'MPIN H' AND 'WRE H' BEING SET TO ONES.
6046
6047 016150 005037 002244 6$: CLR S2LOAD ;SET ALL BITS IN REG 2 TO ZEROES
6048 016154 013737 002244 002246 MOV S2LOAD,S2GOOD ;COPY DATA LOADED TO EXPECTED
6049 016162 052737 000140 002246 BIS #ESRH!WRENH,S2GOOD ;EXPECT ESR H AND WREN H TO BE ONES
6050 016170 012737 177400 002250 MOV #177400,S2MASK ;SETUP TO COMPARE LOW BYTE

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6051 016176 004737 010552 JSR PC,LDRD2S ;LOAD, READ AND CHECK CONTROL REG 2
6052 016202 001405 BEQ 7$ ;IF LOADED OK THEN CONTINUE
6053 016204 ERRDF 2,S2EROR ;CONTROL REGISTER 2 NOT = EXPECTED
6054 016204 104455 TRAP C$ERDF
6055 016206 000002 .WORD 2
6056 016210 000000 .WORD 0
6057 016212 005320 .WORD S2EROR
6058 016214 CKLOOP
6059 016214 104406 TRAP C$CLP1
6060
6061 ;LOAD DATA PATTERN INTO MEMORY SIMULATOR RAM ADDRESSED BY CONTROL
6062 ;REGISTER 2 AND 4. THE ADDRESS AND DATA PATTERN LOADED ARE AS FOLLOWS:
6063 ; ADDRESS DATA
6064 ; 000000 125125
6065 ; 000002 052652
6066
6067 016216 C05037 002264 7$: CLR S6MASK ;SETUP TO COMPARE ALL BITS
6068 016222 004737 010630 JSR PC,LDRDS6 ;GO LOAD, READ AND CHECK RAM LOCATION
6069 016226 001404 BEQ 8$ ;IF LOADED OK THEN CONTINUE
6070 016230 ERRDF 4,MSGMSR,S6ALLR ;DATA ERROR IN MEMORY SIMULATOR RAM
6071 016230 104455 TRAP C$ERDF
6072 016232 000004 .WORD 4
6073 016234 002743 .WORD MSGMSR
6074 016236 005454 .WORD S6ALLR
6075 016240 8$: ENDSEG
6076 016240 10002$:
6077 016240 104405 TRAP C$ESEG
6078
6079 016242 005737 002254 TST S4LOAD ;CHECK IF FIRST TIME THROUGH
6080 016246 001006 BNE 9$ ;IF NOT THEN ADDRESS 0 AND 2 LOADED
6081 016250 062737 000002 002254 ADD #2,S4LOAD ;UPDATE ADDRESS TO ADDRESS 2
6082 016256 005137 002260 COM S6LOAD ;1'S COMPLEMENT THE DATA
6083 016262 000721 BR 5$ ;GO LOAD ADDRESS 2 WITH 052652
6084
6085 ;SET THE SIGNALS "CTS H" AND "8BIT H" TO ONES IN CONTROL REGISTER 0.
6086 ;"CTS H" ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO THE MEMORY
6087 ;SIMULATOR LOGIC. IN THIS TEST, "CTS H" ON A ONE WILL ENABLE THE
6088 ;SYSTEM BUS ADDRESSES TO THE MEMORY SIMULATOR MODULE AND THE MEMORY
6089 ;SIMULATOR RAM DATA ONTO THE SYSTEM BUS IN 8 BIT MODE. THE SIGNAL
6090 ;"8BIT H" ON A ONE WILL ENABLE 8 BIT ADDRESSING AND DATA MODE. EITHER
6091 ;THE HIGH OR LOW BYTE OF RAM DATA WILL BE ENABLED TO THE LOW BYTE OF THE
6092 ;SYSTEM BUS DEPENDING UPON THE ADDRESS SELECTED.
6093
6094 016264 052737 000012 002234 9$: BIS #CTSH!BIT8H,S0LOAD ;SETUP BIT TO BE LOADED
6095 016272 004737 010504 JSR PC,LDRDS0 ;GO LOAD, READ AND CHECK CONTROL REG 2
6096 016276 001404 BEQ 10$ ;IF LOADED OK THEN CONTINUE
6097 016300 ERRDF 1,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
6098 016300 104455 TRAP C$ERDF
6099 016302 000001 .WORD 1
6100 016304 000000 .WORD 0
6101 016306 005304 .WORD S0EROR
6102 016310 10$: ENDSEG
6103 016310 10001$:
6104 016310 104405 TRAP C$ESEG
6105
6106 016312 012701 016742 MOV #30$,R1 ;GET POINTER TO ADDRESS AND DATA TABLES

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6107
6108 016316          11$:  BGNSEG
6109 016316 104404  TRAP   C$BSEG
6110
6111                ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6112                ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6113
6114 016320 004737 012212 JSR   PC,SLCTTE
6115
6116                ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
6117                ;2:0 TO A 0. THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH THE
6118                ;TEST PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6. THE DIAGNOSTIC
6119                ;ADDRESS REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER
6120                ;BIT 9 BEING SET TO A ONE PREVIOUSLY. ON A READ COMMAND TO CONTROL
6121                ;REGISTER 6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
6122
6123 016324 004537 012232 JSR   R5,SELER           ;SELECT REGISTER SPECIFIED BY NEXT WORD
6124 016330 000000        .WORD  ADDRES           ;SELECT THE DIAG ADDRESS REG AND ADDR BUS
6125
6126                ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
6127                ;FOLLOWING ADDRESSES DEPENDING UPON THE ADDRESS BEING TESTED: 0,1,2 OR 3.
6128
6129 016332 011137 002346 MOV   (R1),T6LOAD        ;GET THE TEST ADDRESS FROM THE TABLE
6130 016336 005037 002352 CLR   T6MASK            ;SETUP TO CHECK ALL 16 BITS
6131 016342 004737 011214 JSR   PC,LDRDT6         ;GO LOAD, READ AND CHECK DIAG ADDRESS REG
6132 016346 001405        BEQ   12$              ;IF LOADED OK THEN CONTINUE
6133 016350                ERRDF 12,ADDRRG,T06ERR        ;DIAGNOSTIC ADDRESS REGISTER ERROR
6134 016350 104455        TRAP  C$ERDF
6135 016352 000014        .WORD  12
6136 016354 004142        .WORD  ADDR RG
6137 016356 006730        .WORD  T06ERR
6138 016360                CKLOOP
6139 016360 104406        TRAP  C$CLP1
6140
6141                ;SELECT HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3. THE
6142                ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
6143                ;CONTROL REGISTER 6.
6144
6145 01636? 004537 012232 12$: JSR   R5,SELER           ;SELECT REGISTER SPECIFIED B. NEXT WORD
6146 01636, 000003        .WORD  HDAL           ;SELECT THE HDAL REGISTER
6147
6148                ;RELOAD HDAL REGISTER BITS FOR SCOPE LOOPING PURPOSES ONLY. THIS IS
6149                ;DONE TO SET ALL THE TIMING SIGNALS BACK TO THE NON-ASSERTED STATE.
6150
6151 016370 012737 001014 002346 MOV   #HDAL9!HDAL3!HDAL2,T6LOAD ;GET BITS PREVIOUSLY LOADED
6152 016376 004737 011214 JSR   PC,LDRDT6         ;LOAD, READ AND CHECK HDAL REGISTER
6153 016402 001405        BEQ   13$              ;IF LOADED OK THEN CONTINUE
6154 016404                ERRDF 12,HDALRG,T06ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
6155 016404 104455        TRAP  C$ERDF
6156 016406 000014        .WORD  12
6157 016410 003754        .WORD  HDALRG
6158 016412 006730        .WORD  T06ERR
6159 016414                CKLOOP
6160 016414 104406        TRAP  C$CLP1
6161
6162                ;START A T-11 MACHINE CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE

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6163 : 1. SET XRAS H AND PRAS H TO THE HIGH STATE
6164 : 2. SET XCAS H AND PCAS H TO THE HIGH STATE
6165 : 3. SET XPI L AND PPI L TO THE LOW STATE
6166 :SETTING THE SIGNAL PRAS H TO THE HIGH STATE WILL CAUSE THE SIGNAL
6167 :ADVAL H TO GO FROM A LOW TO A HIGH STATE, THUS CLOCKING THE SYSTEM
6168 :ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR ADDRESS BUS LATCHES.
6169 :WHEN THE SIGNALS XRAS H AND XCAS H ARE ASSERTED HIGH, THE SIGNAL REAT H
6170 :WILL GO FROM A LOW TO A HIGH STATE, THUS CAUSING THE SIGNAL READ H TO
6171 :GO FROM A LOW TO A HIGH STATE. THE TARGET EMULATORS SIGNAL READ H
6172 :ALONG WITH THE MEMORY SIMULATOR'S SIGNALS CTS H AND ESR H WILL CAUSE
6173 :THE MEMORY SIMULATOR RAM DATA TO BE PUT ONTO THE SYSTEM DATA BUS. IF THE
6174 :ADDRESS IS ODD IN 8 BIT MODE, THE HIGH BYTE OF THE RAM LOCATION WILL BE
6175 :ENABLED TO THE LOW BYTE OF THE DATA BUS. WHEN THE TARGET EMULATOR'S
6176 :SIGNAL REAT H IS ASSERTED HIGH, THE TARGET EMULATOR'S SIGNAL MSDI H
6177 :WILL BE ASSERTED HIGH THUS ENABLING THE SYSTEM DATA BUS TO THE TARGET
6178 :EMULATOR'S EODAL BUS. IN 8 BIT MODE, ALL DATA WILL BE READ IN ON THE
6179 :LOW BYTE OF THE EODAL BUS. THE MEMORY SIMULATOR RAMS ARE ADDRESSED BY
6180 :THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES WHICH WERE CLOCKED BY
6181 :THE SIGNAL ADVAL H. THE DATA ON THE SYSTEM ADDRESS BUS COMES FROM THE
6182 :TARGET EMULATORS DIAGNOSTIC ADDRESS REGISTER.
6183
6184 016416 004737 012276 13$: JSR PC,XRASH ;SET XRAS H AND PRAS H TO HIGH STATE
6185 016422 004737 012402 JSR PC,XCASH ;SET XCAS H AND PCAS H TO HIGH STATE
6186 016426 004737 012506 JSR PC,XPIH ;SET XPI H AND PPI H TO THE LOW STATE
6187
6188 :READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H ARE
6189 :ASSERTED HIGH (1'S).
6190
6191 016432 012737 000110 002342 MOV #VDAL6!VDAL3,T4GOOD ;EXPECT READ H AND MSDI H TO BE ONES
6192 016440 004737 011176 JSR PC,READT4 ;READ VDAL AND PAUSE STATE MACHINE REG
6193 016444 001405 BEQ 14$ ;IF DATA OK THEN CONTINUE
6194 016446 ERRDF 11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
6195 016446 104455 TRAP C$ERRDF
6196 016450 000013 .WORD 11
6197 016452 003706 .WORD VDALRG
6198 016454 006714 .WORD T4EROR
6199 016456 CKLOOP
6200 016456 104406 TRAP C$CLP1
6201
6202 :SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6203 :REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6204
6205 016460 004737 011246 14$: JSR PC,SLCTMS ;SELECT THE MEMORY SIMULATOR MODULE
6206
6207 :READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
6208 :TARGET EMULATOR MODULE SET THE SIGNALS ADVAL H AND READ H TO THE
6209 :HIGH STATE FROM THE LOW STATE.
6210
6211 016464 004737 010520 JSR PC,READS0 ;READ AND CHECK CONTROL REGISTER 0
6212 016470 001405 BEQ 15$ ;IF NO CHANGES THEN CONTINUE
6213 016472 ERRDF 1,SOEROR ;CONTROL REGISTER 0 NOT = EXPECTED
6214 016472 104455 TRAP C$ERRDF
6215 016474 000001 .WORD 1
6216 016476 000000 .WORD 0
6217 016500 005304 .WORD SOEROR
6218 016502 CKLOOP
  
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6219 016502 104406 TRAP C$CLP1
6220
6221 ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
6222 ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
6223 ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H. THE SIGNAL ADVAL H
6224 ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
6225 ;SIGNAL PRAS H WAS SET HIGH FROM THE LOW STATE. THE MEMORY SIMULATORS
6226 ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
6227 ;BITS VIA THE SIGNALS CTS H AND CTS L.
6228
6229 016504 011137 002254 15$: MOV (R1),S4LOAD ;GET TE DIAG ADDRESS REG DATA LOADED
6230 016510 004737 010612 JSR PC,READS4 ;READ AND CHECK CONTROL REGISTER 4
6231 016514 001405 BEQ 16$ ;IF DATA = TE DIAG ADDRESS REG - CONT
6232 016516 ERRDF 3,TEMSAD,S04ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
6233 016516 104455 TRAP C$ERDF
6234 016520 000003 .WORD 3
6235 016522 002532 .WORD TEMSAD
6236 016524 005404 .WORD S04ERR
6237 016526 CKLOOP
6238 016526 104406 TRAP C$CLP1
6239
6240 ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
6241 ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
6242 ;ZEROS FOR THESE TWO ADDRESSES. ADDRESS BITS 17 AND 16 WERE CLOCKED
6243 ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
6244 ;ADVAL H. THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
6245 ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE FROM
6246 ;THE LOW STATE. THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
6247 ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
6248 ;MEMORY SIMULATOR MODULE.
6249
6250 016530 052737 000014 002250 16$: BIS #MSEL0!MSEL1,S2MASK ;IGNORE TRI-STATE BIT WHEN CTS H SET
6251 016536 005037 002244 CLR S2LOAD ;EXPECT MSAD 17:16 TO BE ZERO
6252 016542 013737 002244 002246 MOV S2LOAD,S2GOOD ;COPY DATA LOADED TO EXPECTED
6253 016550 052737 000140 002246 BIS #ESRH!WRENH,S2GOOD ;EXPECT MAP PROTECT BITS TO BE ONES
6254 016556 004737 010560 JSR PC,READS2 ;READ AND CHECK CONTROL REGISTER 2
6255 016562 001405 BEQ 17$ ;IF DATA OK THEN CONTINUE
6256 016564 ERRDF 2,TEMSA1,S02ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
6257 016564 104455 TRAP C$ERDF
6258 016566 000002 .WORD 2
6259 016570 002406 .WORD TEMSA1
6260 016572 005364 .WORD S02ERR
6261 016574 CKLOOP
6262 016574 104406 TRAP C$CLP1
6263
6264 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6265 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6266
6267 016576 004737 012212 17$: JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE
6268
6269 ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO A 7. THE EODAL BUS
6270 ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
6271
6272 016602 004537 012232 JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
6273 016606 000007 .WORD EODAL ;SELECT THE EODAL BUS TO BE READ
6274

```



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6275 :AT THIS TIME THE MEMORY SIMULATOR RAM DATA SHOULD BE ENABLED ON THE
6276 :SYSTEM DATA BUS AND ENABLED TO THE TARGET EMULATORS EODAL BUS VIA THE
6277 :TARGET EMULATOR SIGNALS READ H AND MSDI H RESPECTIVELY. IF THE ADDRESS
6278 :IS ODD IN 8 BIT MODE, THE HIGH BYTE OF RAM LOCATION IS ENABLED TO THE
6279 :LOW BYTE OF THE CDS-11 SYSTEM DATA BUS. THE MEMORY SIMULATOR RAM IS
6280 :ADDRESSED BY THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER WHICH
6281 :WAS CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA TA
6282 :THE SIGNAL ADVAL H. THE ADDRESSES AND DATA PATTERNS STORED IN THE RAM
6283 :ADDRESSES SELECTED ARE AS FOLLOWS:
6284 :   RAM ADDRESS 0 LOW BYTE WAS LOADED WITH 125
6285 :   RAM ADDRESS 0 HIGH BYTE WAS LOADED WITH 252
6286 :   RAM ADDRESS 2 LOW BYTE WAS LOADED WITH 252
6287 :   RAM ADDRESS 2 HIGH BYTE WAS LOADED WITH 125
6288
6289 016610 016137 000010 002346 MOV 10(R1),T6LOAD ;GET DATA LOADED INTO MS RAM ADDRESSED
6290 016616 012737 177400 002352 MOV #177400,T6MASK ;SETUP TO IGNORE HIGH BYTE
6291 016624 004737 011222 JSR PC,READT6 ;READ SYSTEM DATA BUS ON THE EODAL BUS
6292 016630 001405 BEQ 18$ ;IF DATA = MS RAM DATA THEN CONTINUE
6293 016632 ERRDF 12,MSTEDE,T6ALLR ;MS RAM DATA TO TE EODAL BUS ERROR
6294 016632 104455 TRAP C$ERDF
6295 016634 000014 .WORD 12
6296 016636 004241 .WORD MSTEDE
6297 016640 006744 .WORD T6ALLR
6298 016642 CKLOOP
6299 016642 104406 TRAP C$CLP1
6300
6301 :SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
6302 :REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
6303 :REGISTER 6.
6304
6305 016644 004537 012232 18$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
6306 016650 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
6307
6308 :FINISH THE T-11 TIMING CYCLE BY DOING THE FOLLOWING SEQUENCE:
6309 : 1. SET XCAS H AND PCAS H TO THE LOW STATE
6310 : 2. SET XPI L AND PPI L TO THE HIGH STATE
6311 : 3. SET XRAS H AND PRAS H TO THE LOW STATE
6312
6313 016652 012737 001034 002346 MOV #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SETUP PREVIOUSLY LOADED BITS
6314 016660 005037 002352 CLR T6MASK ;SETUP TO CHECK ALL 16 BITS
6315 016664 004737 012434 JSR PC,XCASL ;SET XCAS H AND PCAS H TO LOW STATE
6316 016670 004737 012540 JSR PC,XPIL ;SET XPI L AND PPI L TO THE HIGH STATE
6317 016674 004737 012330 JSR PC,XRASL ;SET XRAS H AND PRAS H TO LOW STATE
6318
6319 :READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H
6320 :WENT TO A ZERO AS A RESULT OF SETTING THE SIGNALS XCAS H AND XRAS H
6321 :TO THE LOW STATE. CHECK THAT THE SIGNAL EDEOC H WENT TO A ONE AS
6322 :A RESULT OF XRAS H AND XCAS H BEING SET LOW AND THE SINGLE STEP SYNC
6323 :FLIP-FLOP BEING SET TO A ONE VIA XCAS H.
6324
6325 016700 012737 000020 002342 MOV #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE SET TO A ONE
6326 016706 004737 011176 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
6327 016712 001404 BEQ 19$ ;IF OK THEN CONTINUE
6328 016714 ERRDF 11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
6329 016714 104455 TRAP C$ERDF
6330 016716 000013 .WORD 11
  
```

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TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE

SEQ 0127

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6331 016720 003706          .WORD  VDALRG
6332 016722 006714          .WORD  T4EROR
6333 016724          19$:  ENDSEG
6334 016724          10003$:
6335 016724 104405          TRAP   C$ESEG
6336
6337 016726 005761 000012          TST   12(R1)          ;CHECK IF THIS WAS LAST DATA PATTERN
6338 016732 001414          BEQ   31$             ;IF YES THEN END OF TEST
6339 016734 005721          TST   (R1)+          ;UPDATE POINTER TO ADDRESS TABLE
6340 016736 000137 016316          JMP   11$             ;GO CHECK NEXT DATA PATTERN
6341
6342
6343          ;DATA PATTERN FOR ADDRESS BITS 15:0 TO BE LOADED INTO DIAGNOSTIC ADDRESS
6344          ;REGISTER.
6345 016742 000000          30$:  .WORD  000000
6346 016744 000001          .WORD  000001
6347 016746 000002          .WORD  000002
6348 016750 000003          .WORD  000003
6349
6350          ;DATA PATTERN FOR ADDRESSES 0 AND 2 OF THE 1ST 4K OF MEMORY SIMULATOR RAM
6351
6352 016752 000125          .WORD  125           ;DATA FOR LOW BYTE OF ADDRESS 0 (0)
6353 016754 000252          .WORD  252           ;DATA FOR HIGH BYTE OF ADDRESS 0 (1)
6354 016756 000252          .WORD  252           ;DATA FOR LOW BYTE OF ADDRESS 2 (2)
6355 016760 000125          .WORD  125           ;DATA FOR HIGH BYTE OF ADDRESS 2 (3)
6356 016762 000000          .WORD  0             ;TABLE TERMINATOR
6357
6358 016764          31$:  ENDTST
6359 016764          L10040:
6360 016764 104401          TRAP   C$ETST
6361

```


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TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE

SEQ 0129

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6418 017002 004737 011640      JSR      PC,MSRAM0      ;LOAD, READ AND CHECK MODULE SELECT RAM 0
6419
6420                          ;GO LOAD, READ AND CHECK MODULE SELECT RAM 1. THE FOLLOWING DATA PATTERNS
6421                          ;WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
6422                          ;AT ADDRESS 0: 17, 0, 0 AND 0. THESE PATTERNS WILL ENABLE THE FIRST 32K
6423                          ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
6424
6425 017006 004737 012010      JSR      PC,MSRAM1      ;LOAD, READ AND CHECK MODULE SELECT RAM 1
6426
6427 017012 005001      CLR      R1              ;SETUP STARTING ADDRESS TO EQUAL ZERO
6428 017014 012702 021106      MOV      #50$,R2        ;SETUP POINTER TO DATA TABLE
6429 017020 012703 000002      MOV      #2,R3          ;SETUP TO DO EACH ADDRESS TWICE
6430
6431 017024          1$:      BGNSEG
6432 017024 104404          TRAP     C$BSEG
6433
6434                          ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6435                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6436
6437 017026 004737 012212      JSR      PC,SLCTTE      ;SELECT TARGET EMULATOR MODULE
6438
6439                          ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL 'BRKRES L'
6440                          ;BY TOGGING ADAL REGISTER BIT 0. ADAL10 H AND ADAL9 H SET TO ONES WILL
6441                          ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS. PULSING
6442                          ;THE SIGNAL 'BRKRES L' VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
6443                          ;TARGET EMULATOR MODULE. ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
6444                          ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL 'CKAI H' TO BE PULSED VIA THE
6445                          ;THE SIGNAL 'RASP L' LATER ON IN THIS TEST. ADAL REGISTER BIT 4 ON A
6446                          ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
6447                          ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
6448
6449 017032 012737 043020 002334      MOV      #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
6450 017040 004737 012764          JSR      PC,BRKRES      ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
6451
6452                          ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
6453                          ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
6454                          ;REGISTER 6.
6455
6456 017044 004537 012232      JSR      R5,SELTERR     ;SELECT REGISTER SPECIFIED BY NEXT WORD
6457 017050 000003          .WORD   HDAL           ;SELECT THE HDAL REGISTER
6458
6459                          ;SET HDAL REGISTER BITS 9,4,3 + 2 TO A ONE AND HDAL BITS 14 AND 11 TO A
6460                          ;ZERO. HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
6461                          ;AND CONTROL SIGNALS. HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
6462                          ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS. HDAL REGISTER
6463                          ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
6464                          ;HDAL REGISTER BITS 4 AND 3 SET TO ONES WILL SET THE SIGNALS XR/WLB H
6465                          ;AND XR/WHB H TO THE HIGH STATE. THESE SIGNALS WILL CAUSE THE SIGNAL
6466                          ;'REAT H' TO BE ASSERTED HIGH LATER IN THIS TEST WHEN THE SIGNALS XRAS H
6467                          ;AND XCAS H ARE ASSERTED HIGH.
6468
6469 017052 012737 001034 002346      MOV      #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SET HDAL BITS 9,4,3 + 2 TO ONES
6470 017060 004737 011214          JSR      PC,LDRDT6     ;GO LOAD, READ AND CHECK HDAL REGISTER
6471 017064 001405          BEQ     2$             ;IF LOADED OK THEN CONTINUE
6472 017066          ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
6473 017066 104455          TRAP     C$ERRDF

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6474 017070 000014      .WORD 12
6475 017072 003754      .WORD HDALRG
6476 017074 006730      .WORD T06ERR
6477 017076             CKLOOP
6478 017076 104406      TRAP C$CLP1
6479
6480                    ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
6481                    ;REGISTER 4. PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
6482                    ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L'.
6483
6484 017100 005037 002340      2$: CLR T4LOAD      ;SETUP TO CLEAR ALL OTHER R/W BITS
6485 017104 004737 012704      JSR PC,CLRPSM   ;PULSE INVD L VIA VDAL2 H
6486
6487                    ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4. ON
6488                    ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
6489                    ;BE WRITTEN OR READ.
6490
6491 017110 004537 012232      JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
6492 017114 000004             .WORD MODE      ;SELECT THE MODE REGISTER
6493
6494                    ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
6495                    ;ZEROS. MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
6496
6497 017116 005037 002346      CLR T6LCAD      ;SETUP TO CLEAR ALL MODE REGISTER BITS
6498 017122 004737 011214      JSR PC,LDRDT6  ;GO LOAD, READ AND CHECK MODE REGISTER
6499 017126 001405             BEQ 3$         ;IF LOADED OK THEN CONTINUE
6500 017130             ERRDF 12,MODREG,T06ERR ;MODE REGISTER NOT EQUAL EXPECTED
6501 017130 104455      TRAP C$ERDF
6502 017132 000014      .WORD 12
6503 017134 004000      .WORD MODREG
6504 017136 006730      .WORD T06ERR
6505 017140             CKLOOP
6506 017140 104406      TRAP C$CLP1
6507
6508                    ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
6509                    ;TO A 2. THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
6510                    ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
6511                    ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
6512                    ;TER WILL BE ADDRESSED.
6513
6514 017142 004537 012232      3$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
6515 017146 000002             .WORD FDAL      ;SELECT EOAI AND FDAL REGISTER
6516
6517                    ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER. THE EOAI REGISTER WILL
6518                    ;BE LOADED AND CHECKED FOR ZEROES. THE FDAL REGISTER WILL BE LOADED AND
6519                    ;CHECKED FOR A DATA PATTERN OF ONE (FDALO H = 1).
6520
6521 017150 012737 000001 002346  MOV #FDALO,T6LOAD ;SETUP EOAI AND FDAL REG DATA PATTERN
6522 017156 004737 011214      JSR PC,LDRDT6  ;GO LOAD, READ AND CHECK EOAI + FDAL REG
6523 017162 001405             BEQ 4$         ;IF LOADED OK THEN CONTINUE
6524 017164             ERRDF 12,EOAIFD,T06ERR ;EOAI OR FDAL REGISTER ERROR
6525 017164 104455      TRAP C$ERDF
6526 017166 000014      .WORD 12
6527 017170 004045      .WORD EOAIFD
6528 017172 006730      .WORD T06ERR
6529 017174             CKLOOP

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TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE

SEQ 0131

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6530 017174 104406          TRAP    C$CLP1
6531
6532                        ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
6533                        ;CHANGES OCCURED DOING THE PAST SEQUENCES.
6534
6535 017176 004737 011176    4$:    JSR     PC,READT4          ;READ AND CHECK VDAL REGISTER
6536 017202 001405          BEQ     5$                  ;IF NO CHANGES THEN CONTINUE
6537 017204          ERRDF  11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
6538 017204 104455          TRAP    C$ERDF
6539 017206 000013          .WORD  11
6540 017210 003706          .WORD  VDALRG
6541 017212 006714          .WORD  T4EROR
6542 017214
6543 017214 104406          CKLOOP
6544          TRAP    C$CLP1
6545
6546                        ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6547                        ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6548 017216 004737 011246    5$:    JSR     PC,SLCTMS          ;SELECT MEMORY SIMULATOR MODULE
6549
6550                        ;SET THE SIGNAL 'MP H' TO A ONE AND PULSE THE SIGNAL 'RST H'. THE
6551                        ;SIGNAL 'MP H' ON A ONE WILL ENABLE THE MAP PROTECTION RAM BITS
6552                        ;TO THE SYSTEM BUS ALONG WITH THE SIGNAL MSBRX H. PULSING THE SIGNAL
6553                        ;'RST H' WILL PRESET THE RDV AND WRV FLIP-FLOP'S TO A ONE. WHEN THE
6554                        ;FLIP-FLOP'S ARE SET TO A ONE, THE SIGNAL 'BRK L' WILL BE ASSERTED
6555                        ;HIGH, THUS NO BREAK CONDITION IS GENERATED FROM THE MEMORY SIMULATOR.
6556
6557 017222 112737 000004 002234  MOVB   #MPH,SLOAD          ;SET THE SIGNAL MP H TO HIGH STATE
6558 017230 004737 011266    JSR     PC,MSRSTH          ;SET RST H TO ONE AND PULSE RST H
6559
6560                        ;LOAD MEMORY SIMULATOR RAM ADDRESS TO BE TESTED INTO CONTROL REGISTER 4.
6561                        ;THE ADDRESSES TO BE TESTED ARE 000000, 020000, 040000 OR 060000.
6562
6563 017234 010137 002254    MOV     R1,S4LOAD          ;SETUP TO LOAD ADDRESS TO BE TESTED
6564 017240 004737 010604    JSR     PC,LDRDS4          ;LOAD READ AND CHECK CONTROL REG 4
6565 017244 001405          BEQ     6$                  ;IF LOADED OK THEN CONTINUE
6566 017246          ERRDF  3,MSADRG,S4EROR ;MSAD 15:0 REGISTER ERROR
6567 017246 104455          TRAP    C$ERDF
6568 017250 000003          .WORD  3
6569 017252 002506          .WORD  MSADRG
6570 017254 005334          .WORD  S4EROR
6571 017256
6572 017256 104406          CKLOOP
6573          TRAP    C$CLP1
6574
6575                        ;CLEAR BITS MSEL1 H, MSEL0 H, MSAD17 H AND MSAD16 H IN CONTROL REGISTER
6576                        ;2. MSEL0 H AND MSEL1 H ON A ZERO WILL CAUSE THE SIGNAL "SSM L" TO BE
6577                        ;ASSERTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6. ON A WRITE
6578                        ;OR READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE WRITTEN INTO OR
6579                        ;READ FROM MEMORY SIMULATOR RAM ADDRESSES BY CONTROL REGISTER 2 AND 4.
6580                        ;THE MEMORY SIMULATOR RAM'S ARE ENABLED BY THE DATA PATTERNS PREVIOUSLY
6581                        ;WRITTEN INTO MODULE SELECT RAMS 0 AND 1. MSAD17 H AND MSAD16 H WILL BE
6582                        ;LOADED AND CHECKED WITH ZEROES. THE PROGRAM WILL EXPECT CONTROL REGIS-
6583                        ;TER 2 BITS 'ESR H' AND 'WREN H' TO BE READ AS ONES AS A RESULT OF MAP
6584                        ;PROTECTION RAM BITS 'MPIN H' AND 'WRE H' BEING SET TO ONES.
6585 017260 005037 002244    6$:    CLR     S2LOAD          ;SET ALL BITS IN REG 2 TO ZEROES

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6586 017264 013737 002244 002246      MOV      S2LOAD,S2GOOD      ;COPY DATA LOADED TO EXPECTED
6587 017272 052737 000140 002246      BIS      #ESRH!WRENH,S2GOOD ;EXPECT ESR H AND WREN H TO BE ONES
6588 017300 012737 177400 002250      MOV      #177400,S2MASK    ;SETUP TO COMPARE LOW BYTE
6589 017306 004737 010552              JSR      PC,LDRD2S         ;LOAD, READ AND CHECK CONTROL REG 2
6590 017312 001405              BEQ      7$                ;IF LOADED OK THEN CONTINUE
6591 017314              ERRDF   2,,S2EROR         ;CONTROL REGISTER 2 NOT = EXPECTED
6592 017314 104455              TRAP    C$ERDF
6593 017316 000002              .WORD   2
6594 017320 000000              .WORD   0
6595 017322 005320              .WORD   S2EROR
6596 017324              CKLOOP
6597 017324 104406              TRAP    C$CLP1
6598
6599
6600              ;LOAD DATA PATTERN INTO MEMORY SIMULATOR RAM ADDRESSED BY CONTROL
6601              ;REGISTER 2 AND 4. ONE OF THE FOLLOWING DATA PATTERNS WILL BE LOADED
6602              ;INTO THE TEST ADDRESS LISTED BELOW:
6603              ; ADDRESS 000000 WILL BE LOADED WITH 125252 AND 052525
6604              ; ADDRESS 020000 WILL BE LOADED WITH 146314 AND 031463
6605              ; ADDRESS 040000 WILL BE LOADED WITH 000377 AND 177400
6606              ; ADDRESS 060000 WILL BE LOADED WITH 000000 AND 177777
6607 017326 005037 002264      7$: CLR      S6MASK          ;SETUP TO COMPARE ALL BITS
6608 017332 011237 002260      MOV      (R2),S6LOAD      ;GET THE DATA PATTERN FROM THE TABLE
6609 017336 004737 010630      JSR      PC,LDRDS6       ;GO LOAD, READ AND CHECK RAM LOCATION
6610 017342 001405              BEQ      8$                ;IF LOADED OK THEN CONTINUE
6611 017344              ERRDF   4,MSGMSR,S6ALLR  ;DATA ERROR IN MEMORY SIMULATOR RAM
6612 017344 104455              TRAP    C$ERDF
6613 017346 000004              .WORD   4
6614 017350 002743              .WORD   MSGMSR
6615 017352 005454              .WORD   S6ALLR
6616 017354              CKLOOP
6617 017354 104406              TRAP    C$CLP1
6618
6619
6620              ;SET THE SIGNAL "CTS H" TO A ONE IN CONTROL REGISTER 0. THIS WILL
6621              ;ENABLE THE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR LOGIC.
6622              ;IN THIS TEST, "CTS H" ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO
6623              ;THE MEMORY SIMULATOR MODULE AND THE MEMORY SIMULATOR RAM DATA ONTO THE
6624              ;SYSTEM BUS.
6625 017356 052737 000002 002234 8$: BIS      #CTSH,S0LOAD     ;SETUP BIT TO BE LOADED
6626 017364 004737 010504      JSR      PC,LDRDS0       ;GO LOAD, READ AND CHECK CONTROL REG 2
6627 017370 001405              BEQ      9$                ;IF LOADED OK THEN CONTINUE
6628 017372              ERRDF   1,,S0EROR       ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
6629 017372 104455              TRAP    C$ERDF
6630 017374 000001              .WORD   1
6631 017376 000000              .WORD   0
6632 017400 005304              .WORD   S0EROR
6633 017402              CKLOOP
6634 017402 104406              TRAP    C$CLP1
6635
6636              ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6637              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6638
6639 017404 004737 012212      9$: JSR      PC,SLCTTE
6640
6641              ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS

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6642 ;2:0 TO A 0. THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH THE
6643 ;TEST PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6. THE DIAGNOSTIC
6644 ;ADDRESS REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER
6645 ;BIT 9 BEING SET TO A ONE PREVIOUSLY. ON A READ COMMAND TO CONTROL
6646 ;REGISTER 6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
6647
6648 017410 004537 012232 JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
6649 017414 000000 .WORD ADDRES ;SELECT THE DIAG ADDRESS REG AND ADDR BUS
6650
6651 ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
6652 ;FOLLOWING ADDRESSES: 000000, 020000, 040000, OR 060000.
6653
6654 017416 010137 002346 MOV R1,T6LOAD ;GET THE TEST ADDRESS TO BE LOADED
6655 017422 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ + CHECK DIAG ADDRESS REG
6656 017426 001405 BEQ 10$ ;IF LOADED OK THEN CONTINUE
6657 017430 ERRDF 12,ADDRRG,T06ERR ;DIAGNOSTIC ADDRESS REGISTER ERROR
6658 017430 104455 TRAP C$ERRDF
6659 017432 000014 .WORD 12
6660 017434 004142 .WORD ADDRRG
6661 017436 006730 .WORD T06ERR
6662 017440 CKLOOP
6663 017440 104406 TRAP C$CLP1
6664
6665 ;SELECT HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3. THE
6666 ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
6667 ;CONTROL REGISTER 6.
6668
6669 017442 004537 012232 10$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
6670 017446 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
6671 017450 012737 001034 002346 MOV #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;GET BITS PREVIOUSLY LOADED
6672
6673 ;START A T-11 MACHINE CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE
6674 ; 1. SET XRAS H AND PRAS H TO THE HIGH STATE
6675 ; 2. SET XCAS H AND PCAS H TO THE HIGH STATE
6676 ; 3. SET XPI L AND PPI L TO THE LOW STATE
6677 ;SETTING THE SIGNAL PRAS H TO THE HIGH STATE WILL CAUSE THE SIGNAL
6678 ;'ADVAL H' TO GO FROM A LOW TO A HIGH STATE, THUS CLOCKING THE SYSTEM
6679 ;ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR ADDRESS BUS LATCHES.
6680 ;WHEN THE SIGNALS XRAS H AND XCAS H ARE ASSERTED
6681 ;HIGH, THE SIGNAL REAT H WILL GO FROM A LOW TO A HIGH STATE, THUS CAUSING
6682 ;THE SIGNAL READ H TO GO FROM A LOW TO A HIGH STATE. THE TARGET EMULATORS
6683 ;SIGNAL READ H ALONG WITH THE MEMORY SIMULATOR'S SIGNALS CTS H AND ESR H
6684 ;WILL CAUSE THE MEMORY SIMULATOR RAM DATA TO BE PUT ONTO THE SYSTEM DATA
6685 ;BUS. WHEN THE TARGET EMULATORS SIGNAL REAT H IS ASSERTED HIGH, THE
6686 ;TARGET EMULATORS SIGNAL MSDI H WILL BE ASSERTED HIGH, THUS ENABLING
6687 ;THE SYSTEM DATA BUS TO THE TARGET EMULATORS EODAL BUS. THE MEMORY
6688 ;SIMULATOR RAM'S ARE ADDRESSED BY THE MEMORY SIMULATOR SYSTEM BUS ADDRESS
6689 ;LATCHES WHICH WERE CLOCKED BY THE SIGNAL ADVAL H. THE DATA ON SYSTEM
6690 ;ADDRESS BUS COMES FROM THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER.
6691
6692 017456 004737 012276 JSR PC,XRASH ;SET XRAS H AND PRAS H TO HIGH STATE
6693 017462 004737 012402 JSR PC,XCASH ;SET XCAS H AND PCAS H TO HIGH STATE
6694 017466 004737 012506 JSR PC,XPIH ;SET XPI H AND PPI H TO THE LOW STATE
6695
6696 ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H ARE
6697 ;ASSERTED HIGH (1'S).

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6698
6699 017472 012737 000110 002342      MOV      #VDAL6!VDAL3,T4GOOD      ;EXPECT READ H AND MSDI H TO BE ONES
6700 017500 004737 011176              JSR      PC,READT4                ;READ VDAL AND PAUSE STATE MACHINE REG
6701 017504 001405                      BEQ      11$                      ;IF DATA OK THEN CONTINUE
6702 017506                                ERRDF   11,VDALRG,T4EROR          ;VDAL OR PAUSE STATE MACHINE ERROR
6703 017506 104455                      TRAP    C$ERDF
6704 017510 000013                      .WORD  11
6705 017512 003706                      .WORD  VDALRG
6706 017514 006714                      .WORD  T4EROR
6707 017516                                CKLOOP
6708 017516 104406                      TRAP    C$CLP1
6709
6710                                ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6711                                ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6712
6713 017520 004737 011246      11$:   JSR      PC,SLCTMS                ;SELECT THE MEMORY SIMULATOR MODULE
6714
6715                                ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
6716                                ;TARGET EMULATOR MODULE SET THE SIGNALS ADVAL H AND READ H TO THE
6717                                ;HIGH STATE FROM THE LOW STATE.
6718
6719 017524 004737 010520      JSR      PC,READS0                ;READ AND CHECK CONTROL REGISTER 0
6720 017530 001405                      BEQ      12$                      ;IF NO CHANGES THEN CONTINUE
6721 017532                                ERRDF   1,,S0EROR                ;CONTROL REGISTER 0 NOT = EXPECTED
6722 017532 104455                      TRAP    C$ERDF
6723 017534 000001                      .WORD  1
6724 017536 000000                      .WORD  0
6725 017540 005304                      .WORD  S0EROR
6726 017542                                CKLOOP
6727 017542 104406                      TRAP    C$CLP1
6728
6729                                ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
6730                                ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
6731                                ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H. THE SIGNAL ADVAL H
6732                                ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
6733                                ;SIGNAL PRAS H WAS SET HIGH FROM THE LOW STATE. THE MEMORY SIMULATORS
6734                                ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
6735                                ;BITS VIA THE SIGNALS CTS H AND CTS L.
6736
6737 017544 010137 002254      12$:   MOV      R1,S4LOAD                ;GET THE EXPECTED ADDRESS LOADED
6738 017550 004737 010612      JSR      PC,READS4                ;READ AND CHECK CONTROL REGISTER 4
6739 017554 001405                      BEQ      13$                      ;IF DATA = TE DIAG ADDRESS REG - CONT
6740 017556                                ERRDF   3,TEMSAD,S04ERR          ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
6741 017556 104455                      TRAP    C$ERDF
6742 017560 000003                      .WORD  3
6743 017562 002532                      .WORD  TEMSAD
6744 017564 005404                      .WORD  S04ERR
6745 017566                                CKLOOP
6746 017566 104406                      TRAP    C$CLP1
6747
6748                                ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
6749                                ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
6750                                ;ZERUES FOR THESE TWO ADDRESSES. ADDRESS BITS 17 AND 16 WERE CLOCKED
6751                                ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
6752                                ;ADVAl H. THE SIGNAL ADVAl H WAS GENERATED ON THE TARGET EMULATOR
6753                                ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE FROM

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6754                                     ;THE LOW STATE. THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
6755                                     ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
6756                                     ;MEMORY SIMULATOR MODULE.
6757
6758 017570 052737 000014 002250 13$: BIS #MSELO!MSEL1,S2MASK ;IGNORE TRI-STATED BITS WHEN CTS H SET
6759 017576 005037 002244 CLR S2LOAD ;EXPECT MSAD 17:16 TO BE ZERO
6760 017602 013737 002244 002246 MOV S2LOAD,S2GOOD ;COPY DATA LOADED TO EXPECTED
6761 017610 052737 000140 002246 BIS #ESRH!WRENH,S2GOOD ;EXPECT MAP PROTECT BITS TO BE ONES
6762 017616 004737 010560 JSR PC,READS2 ;READ AND CHECK CONTROL REGISTER 2
6763 017622 001405 BEQ 14$ ;IF DATA OK THEN CONTINUE
6764 017624 ERRDF 2,TEMSA1,S02ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
6765 017624 104455 TRAP C$ERDF
6766 017626 000002 .WORD 2
6767 017630 002406 .WORD TEMSA1
6768 017632 005364 .WORD S02ERR
6769 017634 CKLOOP
6770 017634 104406 TRAP C$CLP1
6771
6772                                     ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6773                                     ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6774
6775 017636 004737 012212 14$: JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE
6776
6777                                     ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO A 7. THE EODAL BUS
6778                                     ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
6779
6780 017642 004537 012232 JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
6781 017646 000007 .WORD EODAL ;SELECT THE EODAL BUS TO BE READ
6782
6783                                     ;AT THIS TIME THE MEMORY SIMULATOR RAM DATA SHOULD BE ENABLED ON THE
6784                                     ;SYSTEM DATA BUS AND ENABLED TO THE TARGET EMULATORS EODAL BUS VIA THE
6785                                     ;TARGET EMULATOR SIGNALS READ H AND MSDI H RESPECTIVELY. THE MEMORY
6786                                     ;SIMULATOR RAM IS ADDRESSED BY THE TARGET EMULATORS DIAGNOSTIC ADDRESS
6787                                     ;REGISTER WHICH WAS CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS
6788                                     ;BUS LATCHES VIA THE SIGNAL ADVAL H. THE DATA PATTERNS LOADED INTO
6789                                     ;THE TEST ADDRESSES OF THE MEMORY SIMULATOR RAM'S ARE LISTED BELOW:
6790                                     ; ADDRESS 000000 WAS LOADED WITH 125252 AND 052525
6791                                     ; ADDRESS 020000 WAS LOADED WITH 146314 AND 031463
6792                                     ; ADDRESS 040000 WAS LOADED WITH 000377 AND 177400
6793                                     ; ADDRESS 060000 WAS LOADED WITH 000000 AND 177777
6794
6795 017650 013737 002260 002346 MOV S6LOAD,T6LOAD ;GET DATA LOADED INTO MS RAM ADDRESSED
6796 017656 004737 011222 JSR PC,READT6 ;READ SYSTEM DATA BUS ON THE EODAL BUS
6797 017662 001405 BEQ 15$ ;IF DATA = MS RAM DATA THEN CONTINUE
6798 017664 ERRDF 12,MSTEDE,T6ALLR ;MS RAM DATA TO TE EODAL BUS ERROR
6799 017664 104455 TRAP C$ERDF
6800 017666 000014 .WORD 12
6801 017670 004241 .WORD MSTEDE
6802 017672 006744 .WORD T6ALLR
6803 017674 CKLOOP
6804 017674 104406 TRAP C$CLP1
6805
6806                                     ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6. THE EIDAL BUS
6807                                     ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
6808
6809 017676 004537 012232 15$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD

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6810 017702 000006      .WORD  EIDAL      ;SELECT THE EIDAL BUS TO BE READ
6811
6812      ;IN THE PREVIOUS DATA CHECK, THE PROGRAM VERIFIED THAT THE MEMORY SIMU-
6813      ;LATOR RAM DATA WAS ENBALED TO THE EODAL BUS VIA THE SYSTEM DATA BUS.
6814      ;IN THIS SECTION, THE PROGRAM WILL CHECK THAT THE EODAL BUS IS ENABLED
6815      ;TO THE EIDAL BUS VIA THE CDAL BUS AS A RESULT OF THE SIGNALS COHB L AND
6816      ;COLB L BEING ASSERTED LOW. THE SIGNALS COHB L AND COLB L ARE ASSERTED
6817      ;LOW AS A RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED HIGH: ETR L,
6818      ;PR/WLB H, PR/WHB H, PPI H, DMG L, AND MR11 L. THE DATA READ SHOULD BE
6819      ;THE SANE AS THAT WHICH WAS ENABLED TO THE EODAL BUS. THE DATA PATTERNS
6820      ;LOADED INTO THE TEST ADDRESS OF THE MEMORY SIMULATOR RAMS ARE AS FOLLOWS:
6821      ; ADDRESS 000000 WAS LOADED WITH 125252 AND 052525
6822      ; ADDRESS 020000 WAS LOADED WITH 146314 AND 031463
6823      ; ADDRESS 040000 WAS LOADED WITH 000377 AND 177400
6824      ; ADDRESS 060000 WAS LOADED WITH 000000 AND 177777
6825
6826 017704 013737 002260 002346  MOV  S6LOAD,T6LOAD      ;GET DATA LOADED INTO MS RAM ADDRESSED
6827 017712 004737 011222          JSR  PC,READT6        ;READ SYSTEM DATA BUS ON EIDAL VIA EODAL
6828 017716 001405          BEQ  16$             ;IF DATA OK THEN CONTINUE
6829 017720          ERRDF 12,MSTEEI,T6ALLR      ;MS RAM DATA TO EIDAL BUS VIA EODAL BUS
6830 017720 104455          TRAP C$ERDF
6831 017722 000014          .WORD 12
6832 017724 004327          .WORD MSTEEI
6833 017726 006744          .WORD T6ALLR
6834 017730          CKLOOP
6835 017730 104406          TRAP C$CLP1
6836
6837      ;IN THE PREVIOUS DATA CHECKS, MEMORY SIMULATOR RAM DATA WAS ENABLED TO
6838      ;THE SYSTEM DATA BUS WHICH ALSO WAS ENABLED TO THE EODAL, CDAL AND EIDAL
6839      ;BUSES. IN ADDITION TO THESE BUSES, MEMORY SIMULATOR RAM DATA WILL BE
6840      ;ENABLED TO THE TDAL BUS VIA THE CDAL BUS BY THE SIGNALS DTHB L AND
6841      ;DTLB H. THE SIGNALS DTHB L AND DTLB L ARE ASSERTED LOW AS A RESULT OF
6842      ;THE SIGNALS PSEL1 L, PSEL0 L, PBCLR L AND CPIW L BEING ASSERTED HIGH AND
6843      ;THE T-11 SIGNAL CCAS H BEING ASSERTED LOW. TO CAPTURE THE MEMORY
6844      ;SIMULATOR RAM DATA ON THE TDAL BUS, THE PROGRAM WILL SET VDAL2 H TO A
6845      ;ONE AND THEN A ZERO TO CLOCK THE TDAL BUS DATA INTO THE TDAL DIAGNOSTIC
6846      ;LATCHES.
6847
6848 017732 052737 000004 002340 16$:  BIS  #VDAL2,T4LOAD      ;SET BIT TO CLOCK TDAL DIAG LATCHES
6849 017740 052737 000004 002342      BIS  #VDAL2,T4GOOD      ;EXPECT VDAL2 H TO BE SET ON READ
6850 017746 004737 011170          JSR  PC,LDRD4T         ;LOAD, READ AND CHECK VDAL REGISTER
6851 017752 001405          JEQ  17$             ;IF LOADED OK THEN CONTINUE
6852 017754          ERRDF 11,VDALRG,T4EROR      ;VDAL REGISTER NOT EQUAL EXPECTED
6853 017754 104455          TRAP C$ERDF
6854 017756 000013          .WORD 11
6855 017760 003706          .WORD VDALRG
6856 017762 006714          .WORD T4EROR
6857 017764          CKLOOP
6858 017764 104406          TRAP C$CLP1
6859 017766 042737 000004 002340 17$:  BIC  #VDAL2,T4LOAD      ;SET CLOCK SIGNAL TO A ZERO
6860 017774 042737 000004 002342      BIC  #VDAL2,T4GOOD      ;EXPECT VDAL2 H TO BE 0 ON A READ
6861 020002 004737 011170          JSR  PC,LDRD4T         ;LOAD, READ AND CHECK VDAL REGISTER
6862 020006 001405          BEQ  18$             ;IF LOADED OK THEN CONTINUE
6863 020010          ERRDF 11,VDALRG,T4EROR      ;VDAL REGISTER NOT EQUAL EXPECTED
6864 020010 104455          TRAP C$ERDF
6865 020012 000013          .WORD 11
  
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6866 020014 003706      .WORD  VDALRG
6867 020016 006714      .WORD  T4EROR
6868 020020              CKLOOP
6869 020020 104406      TRAP   C$CLP1
6870
6871                      ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
6872                      ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
6873                      ;REGISTER 6.
6874
6875 020022 004537 012232 18$: JSR    R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
6876 020026 000003              .WORD  HDAL           ;SELECT THE HDAL REGISTER
6877
6878                      ;FINISH THE T-11 TIMING CYCLE BY DOING THE FOLLOWING SEQUENCE:
6879                      ; 1. SET XCAS H AND PCAS H TO THE LOW STATE
6880                      ; 2. SET XPI L AND PPI L TO THE HIGH STATE
6881                      ; 3. SET XRAS H AND PRAS H TO THE LOW STATE
6882
6883 020030 012737 001034 002346 MOV    #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SETUP PREVIOUSLY LOADED BITS
6884 020036 004737 012434      JSR    PC,XCASL      ;SET XCAS H AND PCAS H TO LOW STATE
6885 020042 004737 012540      JSR    PC,XPIL      ;SET XPI L AND PPI L TO THE HIGH STATE
6886 020046 004737 012330      JSR    PC,XRASL     ;SET XRAS H AND PRAS H TO LOW STATE
6887
6888                      ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H
6889                      ;WENT TO A ZERO AS A RESULT OF SETTING THE SIGNALS XCAS H AND XRAS H
6890                      ;TO THE LOW STATE.
6891
6892 020052 005037 002342      CLR    T4GOOD       ;EXPECT VDAL REGISTER TO BE A 0
6893 020056 004737 011176      JSR    PC,READT4    ;READ AND CHECK VDAL REGISTER
6894 020062 001405              BEQ    19$          ;IF OK THEN CONTINUE
6895 020064              ERRDF  11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
6896 020064 104455      TRAP   C$ERRDF
6897 020066 000013      .WORD  11
6898 020070 003706      .WORD  VDALRG
6899 020072 006714      .WORD  T4EROR
6900 020074              CKLOOP
6901 020074 104406      TRAP   C$CLP1
6902
6903                      ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6904                      ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6905
6906 020076 004737 011246 19$: JSR    PC,LCTMS      ;SELECT THE MEMORY SIMULATOR MODULE
6907
6908                      ;SET THE SIGNAL CTS H TO THE LOW STATE BY CLEARING THE BIT IN CONTROL
6909                      ;REGISTER 0. THIS WILL DISABLE THE SYSTEM BUS SIGNALS TO AND FROM
6910                      ;THE MEMORY SIMULATOR MODULE.
6911
6912 020102 112737 000004 002234 MOVB   #MPH,SOLOAD   ;CLEAR CTS H AND LEAVE MP H SET TO A 1
6913 020110 004737 010504      JSR    PC,LDRDSO    ;LOAD, READ AND CHECK CONTROL REG 0
6914 020114 001405              BEQ    20$          ;IF LOADED OK THEN CONTINUE
6915 020116              ERRDF  1,SOEROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
6916 020116 104455      TRAP   C$ERRDF
6917 020120 000001      .WORD  1
6918 020122 000000      .WORD  0
6919 020124 005304      .WORD  SOEROR
6920 020126              CKLOOP
6921 020126 104406      TRAP   C$CLP1

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6922
6923           ;READ CONTROL REGISTER 4 TO CHECK THAT THE MEMORY SIMULATOR ADDRESS
6924           ;LOADED PREVIOUSLY IS STILL LOADED
6925
6926 020130 004737 010612      20$: JSR    PC,READS4           ;READ AND CHECK CONTROL REGISTER 4
6927 020134 001405           BEQ    21$             ;IF ADDRESS 0 THEN CONTINUE
6928 020136           ERRDF  3,MSADRG,S4EROR ;MSAD 15:0 REGISTER ERROR
6929 020136 104455           TRAP  C$ERDF
6930 020140 000003           .WORD 3
6931 020142 002506           .WORD MSADRG
6932 020144 005334           .WORD S4EROR
6933 020146           CKLOOP
6934 020146 104406           TRAP  C$CLP1
6935
6936           ;READ CONTROL REGISTER 0 TO CHECK THAT THE DATA LOADED INTO IT PREVIOUSLY
6937           ;HAS NOT CHANGED. THE FOLLOWING SIGNALS SHOULD BE READ AS ZEROES:
6938           ;MSAD16 H, MSAD17 H, MSEL0 L, MSEL1 L AND MSBPK H. THE SIGNALS ESR H
6939           ;AND WREN H SHOULD BE READ AS ONES.
6940
6941 020150 012737 177400 002250 21$: MOV    #177400,S2MASK ;SETUP TO CHECK ALL OFF LOW BYTE
6942 020156 004737 010560           JSR    PC,READS2     ;READ AND CHECK CONTROL REGISTER 2
6943 020162 001405           BEQ    22$             ;IF NO CHANGE THEN CONTINUE
6944 020164           ERRDF  2,,S2EROR ;CONTROL REG 2 NOT EQUAL EXPECTED
6945 020164 104455           TRAP  C$ERDF
6946 020166 000002           .WORD 2
6947 020170 000000           .WORD 0
6948 020172 005320           .WORD S2EROR
6949 020174           CKLOOP
6950 020174 104406           TRAP  C$CLP1
6951
6952           ;WRITE INTO THE MEMORY SIMULATOR RAM'S TEST ADDRESS THE ONES COMPLEMENT
6953           ;OF THE DATA WHICH WAS PREVIOUSLY WRITTEN INTO IT.
6954
6955 020176 005137 002260      22$: COM    S6LOAD ;MAKE THE 1'S COMPLEMENT OF PREVIOUS DATA
6956 020202 004737 010630           JSR    PC,LDRDS6    ;GO LOAD, READ AND CHECK MEM SIM RAM LOC
6957 020206 001405           BEQ    23$             ;IF LOADED OK THEN CONTINUE
6958 020210           ERRDF  4,MSGMSR,S6ALLR ;DATA ERROR IN MEMORY SIMULATOR RAM
6959 020210 104455           TRAP  C$ERDF
6960 020212 000004           .WORD 4
6961 020214 002743           .WORD MSGMSR
6962 020216 005454           .WORD S6ALLR
6963 020220           CKLOOP
6964 020220 104406           TRAP  C$CLP1
6965
6966           ;SET THE SIGNAL CTS H TO A ONE IN CONTROL REGISTER 0. THIS WILL ENABLE
6967           ;THE SYTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR MODULE.
6968
6969 020222 052737 000002 002234 23$: BIS    #CTSH,S0LOAD ;SETUP BIT TO BE LOADED
6970 020230 004737 010504           JSR    PC,LDRDS0    ;LOAD, READ AND CHECK REGISTER 0
6971 020234 001405           BEQ    24$             ;IF LOADED OK THEN CONTINUE
6972 020236           ERRDF  1,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
6973 020236 104455           TRAP  C$ERDF
6974 020240 000001           .WORD 1
6975 020242 000000           .WORD 0
6976 020244 005304           .WORD S0EROR
6977 020246           CKLOOP
  
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6978 020246 104406 TRAP C$CLP1
6979
6980 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6981 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6982
6983 020250 004. 2212 24$: JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE.
6984
6985 ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 2. THE
6986 ;EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR READ COMMAND TO
6987 ;CONTROL REGISTER 6.
6988
6989 020254 004537 012232 JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
6990 020260 000002 .WORD FDAL ;SELECT EOAI AND FDAL REGISTER
6991
6992 ;LOAD, READ AND CHECK EOAI AND FDAL REGISTER. THE EOAI REGISTER WILL BE
6993 ;LOADED AND CHECKED FOR A DATA PATTERN OF ALL ZEROES. THE FDAL REGISTER
6994 ;WILL BE LOADED AND CHECKED FOR A DATA PATTERN OF 3 (FDAL1 H AND FDAL0 H).
6995 ;FDAL0 H ON A ONE WILL SELECT THE EOAI REGISTER TO BE READ ON A READ COMMAND
6996 ;TO CONTROL REGISTER 6 INSTEAD OF THE CTL REGISTER. FDAL1 H ON A ONE WILL
6997 ;ENABLE THE SIGNALS WR HB H AND WR LB H TO THE SYSTEM BUS WHEN THE SIGNAL
6998 ;DMG L IS ASSERTED LOW LATER ON IN THIS TEST.
6999
7000 020262 012737 000003 002346 MOV #FDAL1!FDAL0,T6LOAD ;SETUP BITS TO BE LOADED
7001 020270 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK EOAI AND FDAL REGISTER
7002 020274 001405 BEQ 25$ ;IF LOADED OK THEN CONTINUE
7003 020276 ERRDF 12,EOAIFD,T06ERR ;EOAI 7:0 OR FDAL 7:0 REGISTER ERROR
7004 020276 104455 TRAP C$ERRDF
7005 020300 000014 .WORD 12
7006 020302 004045 .WORD EOAIFD
7007 020304 006730 .WORD T06ERR
7008 020306 CKLOOP
7009 020306 104406 TRAP C$CLP1
7010
7011 ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL REGISTER
7012 ;WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
7013
7014 020310 004537 012232 25$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
7015 020314 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
7016
7017 ;SET THE SIGNALS PSEL0 L AND PSEL1 L TO THE LOW STATE BY SETTING HDAL
7018 ;REGISTER BITS 5 AND 6 TO ONES. SETTING THESE SIGNALS LOW WILL CAUSE
7019 ;THE SIGNALS DBHB L AND DBLB L TO BE ASSERTED LOW THUS ENABLING THE
7020 ;FDAL BUS TO THE CDAL BUS AND EIDAL BUS. SETTING PSEL0 L AND PSEL1 L
7021 ;WILL ALSO CAUSE THE SIGNAL DMG L TO BE ASSERTED LOW. SET THE SIGNALS
7022 ;XR/WHB L AND XR/WLB L TO THE HIGH STATE BY SETTING HDAL REGISTER BITS
7023 ;4 AND 3 TO A ZERO. THIS WILL SET THE READ/WRITE CONTROL LOGIC TO DO
7024 ;A WRITE WHEN THE SIGNAL XPI H IS SET HIGH. HDAL9 H WILL BE SET TO A
7025 ;ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS
7026 ;BUS. THE DIAGNOSTIC ADDRESS REGISTER WAS LOADED WITH ADDRESS 0 EARLIER
7027 ;IN THIS TEST. HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM
7028 ;TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS.
7029
7030 020316 012737 001144 002346 MOV #HDAL9!HDAL6!HDAL5!HDAL2,T6LOAD ;SETUP BITS TO BE LOADED
7031 020324 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK HDAL REGISTER
7032 020330 001405 BEQ 26$ ;IF LOADED OK THEN CONTINUE
7033 020332 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
  
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TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE

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7034 020332 104455 TRAP CSERDF
7035 020334 000014 .WORD 12
7036 020336 003754 .WORD HDALRG
7037 020340 006730 .WORD T06ERR
7038 020342 CKLOOP
7039 020342 104406 TRAP CSCLP1
7040
7041 ;SET VDALO H TO A ONE TO ENABLE THE OUTPUTS OF THE TDAL DIAGNOSTIC
7042 ;LATCHES ONTO THE TDAL BUS. THE TDAL BUS WILL BE ENABLED TO THE CDAL
7043 ;BUS VIA DBHB L AND DBLB L. THE CDAL BUS WILL BE ENABLED TO THE EIDAL
7044 ;BUS UNCONDITIONALLY.
7045
7046 020344 012737 000001 002340 26$: MOV #VDALO,T4LOAD ;SETUP BIT TO BE LOADED
7047 020352 004737 011162 JSR PC,LDRDT4 ;LOAD, READ AND CHECK VDAL REGISTER
7048 020356 001405 BEQ 27$ ;IF LOADED OK THEN CONTINUE
7049 020360 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
7050 020360 104455 TRAP CSERDF
7051 020362 000013 .WORD 11
7052 020364 003706 .WORD VDALRG
7053 020366 006714 .WORD T4EROR
7054 020370 CKLOOP
7055 020370 104406 TRAP CSCLP1
7056
7057 ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6. ON A READ
7058 ;COMMAND TO CONTROL REGISTER 6 THE EIDAL BUS WILL BE READ.
7059
7060 020372 004537 012232 27$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
7061 020376 000006 .WORD EIDAL ;SELECT THE EIDAL BUS TO BE READ
7062
7063 ;AT THIS POINT IN TIME THE EIDAL BUS SHOULD HAVE THE TDAL DIAGNOSTIC
7064 ;LATCHES ENABLED TO IT BY THE SIGNALS DBHB L AND DBLB L BEING ASSERTED
7065 ;LOW AND VDALO H BEING SET TO A ONE. THE TDAL LATCHES WERE CLOCKED
7066 ;EARLIER IN THE TEST BY THE SIGNAL VDAL2 H. THESE LATCHES WERE
7067 ;CLOCKED WITH THE DATA FROM THE MEMORY SIMULATOR RAM DURING A READ
7068 ;OPERATION OF THE MEMORY SIMULATOR RAM TEST ADDRESS.
7069
7070 020400 011237 002346 MOV (R2),T6LOAD ;GET 1ST DATA WRITTEN TO MS RAM
7071 020404 004737 011222 JSR PC,READT6 ;READ AND CHECK EIDAL BUS
7072 020410 001405 BEQ 28$ ;IF DATA OK THEN CONTINUE
7073 020412 ERRDF 12,MSTETD,T6ALLR ;MS RAM DATA TO EIDAL BUS VIA TDAL BUS
7074 020412 104455 TRAP CSERDF
7075 020414 000014 .WORD 12
7076 020416 004420 .WORD MSTETD
7077 020420 006744 .WORD T6ALLR
7078 020422 CKLOOP
7079 020422 104406 TRAP CSCLP1
7080
7081 ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
7082 ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
7083 ;REGISTER 6.
7084
7085 020424 004537 012232 28$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
7086 020430 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
7087 020432 012737 001144 002346 MOV #HDAL9!HDAL6!HDAL5!HDAL2,T6LOAD ;SETUP PREVIOUSLY LOADED BITS
7088
7089 ;AT THE PRESENT TIME, MEMORY SIMULATOR DATA WHICH WAS READ FROM THE TEST

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7090 ;ADDRESS OF THE MEMORY SIMULATOR RAM EARLIER IN THIS TEST, IS NOW ENABLED
7091 ;TO THE SYSTEM DATA BUS VIA THE TDAL DIAGNOSTIC LATCHES. THIS DATA WAS
7092 ;PRESENT ON THE EIDAL BUS IN THE LAST DATA CHECK ABOVE. THE EIDAL BUS
7093 ;IS ENABLED TO THE SYSTEM DATA BUS BY THE SIGNAL MSDO H BEING ASSERTED
7094 ;HIGH. THE PROGRAM WILL NOW WRITE THE DATA ON THE SYSTEM DATA BUS BACK
7095 ;INTO ADDRESS ZERO ON THE MEMORY SIUMULATOR RAM BY DOING A NORMAL T-11
7096 ;TIMING CYCLE. WHEN PRAS H IS SET HIGH, THE ADDRESS BUS WHICH CONTAINS
7097 ;THE DIAGNOSTIC ADDRESS REGISTER DATA, WILL BE CLOCKED INTO THE MEMORY
7098 ;SIMULATOR SYSTEM ADDRESS BUS LATCHES. WHEN XPI H IS SET HIGH IN THE
7099 ;FOLLOWING TIMING SEQUENCE, THE DATA WILL BE WRITTEN INTO ADDRESS ZERO
7100 ;OF THE MEMORY SIMULATOR RAM. THE WRITE SIGNALS FROM THE TARGET
7101 ;EMULATOR MODULE TO THE MEMORY SIMULATOR MODULE ARE WT HB H AND WT LB H.
7102
7103 020440 004737 012276 JSR PC,XRASH ;SET XRAS H AND PRAS H TO HIGH STATE
7104 020444 004737 012402 JSR PC,XCASH ;SET XCAS H AND PCAS H TO HIGH STATE
7105 020450 004737 012506 JSR PC,XPIH ;SET XPI H AND PPI H TO HIGH STATE
7106 020454 004737 012434 JSR PC,XCASL ;SET XCAS H AND PCAS H TO LOW STATE
7107 020460 004737 012540 JSR PC,XPIL ;SET XPI H AND PPIH TO LOW STATE
7108 020464 004737 012330 JSR PC,XRASL ;SET XRAS H AND PRAS H TO LOW STATE
7109
7110 ;READ VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A ONE
7111 ;IN THE VDAL REGISTER AS A RESULT OF THE ABOVE T-11 TIMING SEQUENCE.
7112
7113 020470 052737 000020 002342 BIS #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE SET TO A ONE
7114 020476 004737 011176 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
7115 020502 001405 BEQ 29$ ;IF OK THEN CONTINUE
7116 020504 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
7117 020504 104455 TRAP C$ERDF
7118 020506 000013 .WORD 11
7119 020510 003706 .WORD VDALRG
7120 020512 006714 .WORD T4EROR
7121 020514 CKLOOP
7122 020514 104406 TRAP C$CLP1
7123
7124 ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE ON CONTROL
7125 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7126
7127 020516 004737 011246 29$: JSR PC,SLCTMS ;SELECT THE MEMORY SIMULATOR MODULE
7128
7129 ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
7130 ;TARGET EMULATOR MODULE PULSED THE SIGNAL ADVAL H BY TOGGLING THE
7131 ;SIGNAL PRAS H.
7132
7133 020522 004737 010520 JSR PC,READSO ;READ AND CHECK CONTROL REGISTER 0
7134 020526 001405 BEQ 30$ ;IF NO CHANGES THEN CONTINUE
7135 020530 ERRDF 1,SOEROR ;CONTROL REGISTER 0 NOT = EXPECTED
7136 020530 104455 TRAP C$ERDF
7137 020532 000001 .WORD 1
7138 020534 000000 .WORD 0
7139 020536 005304 .WORD SOEROR
7140 020540 CKLOOP
7141 020540 104406 TRAP C$CLP1
7142
7143 ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
7144 ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
7145 ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H. THE SIGNAL ADVAL H

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7146                                     ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
7147                                     ;SIGNAL PRAS H WAS SET TO A ONE AND THEN A ZERO. THE MEMORY SIMULATORS
7148                                     ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
7149                                     ;BITS VIA THE SIGNALS CTS H AND CTS L.
7150
7151 020542 010137 002254          30$:  MOV    R1,S4LOAD          ;SETUP THE EXPECTED ADDRESS TO BE READ
7152 020546 004737 010612        JSR    PC,READS4        ;READ AND CHECK CONTROL REGISTER 4
7153 020552 001405                BEQ    31$              ;IF DATA = TE DIAG ADDRESS REG - CONT
7154 020554                ERRDF  3,TEMSAD,S04ERR      ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
7155 020554 104455                TRAP  C$ERDF
7156 020556 000003                .WORD 3
7157 020560 002532                .WORD TEMSAD
7158 020562 005404                .WORD S04ERR
7159 020564                CKLOOP
7160 020564 104406                TRAP  C$CLP1
7161
7162                                     ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
7163                                     ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
7164                                     ;ZEROS FOR THESE TWO ADDRESSES. ADDRESS BITS 17 AND 16 WERE CLOCKED
7165                                     ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
7166                                     ;ADVAL H. THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
7167                                     ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE AND THEN TO
7168                                     ;THE LOW STATE. THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
7169                                     ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
7170                                     ;MEMORY SIMULATOR MODULE.
7171
7172 020566 052737 000014 002250 31$:  BIS    #MSEL0!MSEL1,S2MASK  ;IGNORE TRI-STATE BIT WHEN CTS H SET
7173 020574 005037 002244                CLR    S2LOAD          ;EXPECT MSAD 17:16 TO BE ZERO
7174 020600 013737 002244 002244        MOV    S2LOAD,S2GOOD    ;COPY DATA LOADED TO EXPECTED
7175 020606 052737 000140 002244        BIS    #ESRH!WRENH,S2GOOD ;EXPECT MAP PROTECT BITS TO BE ONES
7176 020614 004737 010560                JSR    PC,READS2        ;READ AND CHECK CONTROL REGISTER 2
7177 020620 001405                BEQ    32$              ;IF DATA OK THEN CONTINUE
7178 020622                ERRDF  2,TEMSA1,S02ERR  ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
7179 020622 104455                TRAP  C$ERDF
7180 020624 000002                .WORD 2
7181 020626 002406                .WORD TEMSA1
7182 020630 005364                .WORD S02ERR
7183 020632                CKLOOP
7184 020632 104406                TRAP  C$CLP1
7185
7186                                     ;SET THE SIGNAL CTS H TO THE LOW STATE BY CLEARING THE BIT IN CONTROL
7187                                     ;REGISTER 0. THIS WILL DISABLE THE SYSTEM BUS SIGNALS TO AND FROM
7188                                     ;THE MEMORY SIMULATOR MODULE.
7189
7190 020634 112737 000004 002234 32$:  MOVB   #MPH,S0LOAD      ;CLEAR CTS H AND LEAVE MP H SET TO A 1
7191 020642 004737 010504                JSR    PC,LDRDS0        ;LOAD, READ AND CHECK CONTROL REG 0
7192 020646 001405                BEQ    33$              ;IF LOADED OK THEN CONTINUE
7193 020650                ERRDF  1,S0EROR        ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
7194 020650 104455                TRAP  C$ERDF
7195 020652 000001                .WORD 1
7196 020654 000000                .WORD 0
7197 020656 005304                .WORD S0EROR
7198 020660                CKLOOP
7199 020660 104406                TRAP  C$CLP1
7200
7201                                     ;READ CONTROL REGISTER 4 TO CHECK THAT THE MEMORY SIMULATOR ADDRESS

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7202                                     ;LOADED PREVIOUSLY IS STILL LOADED
7203
7204 020662 004737 010612          33$: JSR      PC,READS4          ;READ AND CHECK CONTROL REGISTER 4
7205 020666 001405                BEQ      34$          ;IF ADDRESS 0 THEN CONTINUE
7206 020670                ERRDF   3,MSADRG,S4EROR      ;MSAD 15:0 REG ERROR
7207 020670 104455                TRAP    C$ERDF
7208 020672 000003                .WORD   3
7209 020674 002506                .WORD   MSADRG
7210 020676 005334                .WORD   S4EROR
7211 020700                CKLOOP
7212 020700 104406                TRAP    C$CLP1
7213
7214                                     ;READ CONTROL REGISTER 2 TO CHECK THAT THE DATA LOADED INTO IT PREVIOUSLY
7215                                     ;HAS NOT CHANGED. THE FOLLOWING SIGNALS SHOULD BE READ AS ZEROES:
7216                                     ;MSAD16 H, MSAD17 H, MSEL0 L, MSEL1 L AND MSBRK H. THE SIGNALS ESR H
7217                                     ;AND WREN H SHOULD BE READ AS ONES.
7218
7219 020702 012737 177400 002250 34$: MOV      #177400,S2MASK      ;SETUP TO CHECK ALL OFF LOW BYTE
7220 020710 004737 010560                JSR      PC,READS2      ;READ AND CHECK CONTROL REGISTER 2
7221 020714 001405                BEQ      35$          ;IF NO CHANGE THEN CONTINUE
7222 020716                ERRDF   2,,S2EROR      ;CONTROL REG 2 NOT EQUAL EXPECTED
7223 020716 104455                TRAP    C$ERDF
7224 020720 000002                .WORD   2
7225 020722 000000                .WORD   0
7226 020724 005320                .WORD   S2EROR
7227 020726                CKLOOP
7228 020726 104406                TRAP    C$CLP1
7229
7230                                     ;READ CONTENTS OF THE MEMORY SIMULATOR RAM ADDRESS TO CHECK THAT THE DATA
7231                                     ;INITIALLY LOADED INTO IT WAS WRITTEN BACK INTO IT FROM THE TARGET
7232                                     ;EMULATOR MODULE DURING A WRITE OPERATION. IN THE FIRST PART OF THIS
7233                                     ;TEST THE DATA WAS READ FROM THE MEMORY SIMULAOTR RAM INTO THE TARGET
7234                                     ;EMULATOR AND SAVED IN THE TARGET EMULATORS TDAL DIAGNOSTIC LATCHES.
7235                                     ;THE PROGRAM THEN COMPLEMENTED THE DATA PATTERN WRITTEN INTO THE ADDRESS
7236                                     ;OF THE MEMORY SIMULATOR RAM. THE PROGRAM THEN ENABLED THE TDAL DIAG-
7237                                     ;NOSTIC LATCHES TO THE TDAL BUS AND WROTE THE DATA BACK INTO THE ADDRESS
7238                                     ;OF THE MEMORY SIMULATOR RAM. THE FOLLOWING CHECK WILL TEST THAT THIS
7239                                     ;HAPPENED CORRECTLY.
7240
7241 020730 011237 002260          35$: MOV      (R2),S6LOAD      ;GET INITIAL MS RAM DATA LOADED
7242 020734 013737 002260 002262  MOV      S6LOAD,S6GOOD    ;COPY DATA FOR COMPARE IN SUBROUTINE
7243 020742 004737 010644                JSR      PC,READS6      ;READ AND CHECK MS LOC 0 RAM DATA
7244 020746 001404                BEQ      36$          ;IF DATA OK THEN CONTINUE
7245 020750                ERRDF   4,MSGMSR,S6ALLR  ;DATA ERROR IN MEMORY SIMULATOR RAM
7246 020750 104455                TRAP    C$ERDF
7247 020752 000004                .WORD   4
7248 020754 002743                .WORD   MSGMSR
7249 020756 005454                .WORD   S6ALLR
7250 020760                36$: ENDSEG
7251 020760          10000$:
7252 020760 104405                TRAP    C$ESEG
7253
7254 020762 005722                TST     (R2)+          ;UPDATE THE DATA TABLE POINTER
7255 020764 005303                DEC     R3            ;CHECK IF ADDRESS DONE TWICE
7256 020766 001402                BEQ     37$          ;IF YES THEN UPDATE TEST ADDRESS
7257 020770 000137 017024                JMP     1$            ;DO SAME ADDRESS WITH NEW PATTERN

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TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE

SEQ 0144

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7258 020774 012703 000002      37$:  MOV    #2,R3           ;UPDATE TO DO NEXT ADDRESS TWICE
7259 021000 062701 020000      ADD    #MSAD13,R1        ;UPDATE ADDRESS TO NEXT MS RAM BANK
7260 021004 100402              BMI    38$              ;IF DONE EACH BANK OF MEMORY - EXIT
7261 021006 000137 017024      JMP    1$               ;GO DO TWO PATTERNS WITH THIS ADDRESS
7262
7263                          ;TO CHECK THAT ADDRESS 0 OF EACH 4K BANK OF MEMORY SIMULATOR RAM WAS
7264                          ;SELECTED AND WRITTEN CORRECTLY, THE PROGRAM WILL READ THE FIRST ADDRESS
7265                          ;OF EACH 4K BANK OF MEMORY SIMULATOR RAM AND CHECK THE DATA TO BE EQUAL
7266                          ;TO WHAT WAS WRITTEN INTO IT PREVIOUSLY.  THE ADDRESSES AND THE DATA
7267                          ;PATTERNS EXPECTED ARE AS FOLLOWS:
7268                          ;   ADDRESS 000000 WAS WRITTEN WITH 052525
7269                          ;   ADDRESS 020000 WAS WRITTEN WITH 031463
7270                          ;   ADDRESS 040000 WAS WRITTEN WITH 177400
7271                          ;   ADDRESS 060000 WAS WRITTEN WITH 177777
7272
7273 021012 005001              38$:  CLR    R1               ;SETUP STARTING ADDRESS TO BE 0
7274 021014 012702 021110      MOV    #50$+2,R2        ;SETUP ADDRESS OF DATA TABLE
7275
7276                          ;LOAD, READ AND CHECK CONTROL REGISTER 4 WITH THE ADDRESS OF THE LOCATION
7277                          ;TO BE CHECKED.  THE ADDRESSES TO BE LOADED ARE 0, 20000, 40000, AND 60000.
7278
7279 021020 010137 002254      39$:  MOV    R1,S4LOAD      ;GET THE ADDRESS TO BE LOADED
7280 021024 004737 010604      JSR    PC,LDRDS4        ;LOAD, READ AND CHECK CONTROL REGISTER 4
7281 021030 001405              BEQ    40$              ;IF LOADED OK THEN CONTINUE
7282 021032              ERRDF  3,MSADRG,S4EROR ;MSAD 15:0 REGISTER ERROR
7283 021032 104455              TRAP  C$ERDF
7284 021034 000003              .WORD 3
7285 021036 002506              .WORD MSADRG
7286 021040 005334              .WORD S4EROR
7287 021042              CKLOOP
7288 021042 104406              TRAP  C$CLP1
7289
7290                          ;EARLIER IN THIS TEST, CONTROL REGISTER 2 BITS MSAD16 H, MSAD17 H, MSEL1 L,
7291                          ;AND MSEL0 L WERE WRITTEN TO ZEROES.  WHEN A READ COMMAND IS ISSUED TO
7292                          ;CONTROL REGISTER 6 AND THE SIGNALS MSEL1 L AND MSEL0 L ARE ASSERTED LOW,
7293                          ;A PULSE WILL BE ISSUED ON THE SIGNAL SSM L.  THIS SIGNAL ALONG WITH THE
7294                          ;READ COMMAND, WILL READ THE DATA FROM THE MEMORY SIMULATOR RAM ADDRESSED
7295                          ;BY CONTROL REGISTER 2 AND 4 BITS.
7296
7297 021044 011237 002260      40$:  MOV    (R2),S6LOAD    ;GET THE DATA FROM THE TABLE
7298 021050 012237 002262      MOV    (R2)+,S6GOOD     ;COPY DATA FOR DATA COMPARE
7299 021054 005722              TST   (R2)+             ;UPDATE POINTER TO NEXT EXPECTED DATA
7300 021056 004737 010644      JSR    PC,READS6        ;READ AND CHECK MEMORY SIM RAM DATA
7301 021062 001405              BEQ    41$              ;IF DATA OK THEN CONTINUE
7302 021064              ERRDF  4,MSGMSR,S6ALLR ;DATA ERROR IN MEMORY SIMULATOR RAM
7303 021064 104455              TRAP  C$ERDF
7304 021066 000004              .WORD 4
7305 021070 002743              .WORD MSGMSR
7306 021072 005454              .WORD S6ALLR
7307 021074              CKLOOP
7308 021074 104406              TRAP  C$CLP1
7309
7310 021076 062701 020000      41$:  ADD    #MSAD13,R1        ;UPDATE THE ADDRESS TO NEXT 4K MEMORY
7311 021102 100346              BPL   39$              ;IF NOT DONE CHECK THIS 4K MEMORY BANK
7312 021104 000410              BR    51$              ;EXIT THE TEST
7313

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TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE

SEQ 0145

7314	021106	125252
7315	021110	052525
7316	021112	146314
7317	021114	031463
7318	021116	000377
7319	021120	177400
7320	021122	000000
7321	021124	177777
7322		
7323	021126	
7324	021126	
7325	021126	104401
7326		

50\$:	.WORD	125252	:	ADDRESS 000000 DATA PATTERNS
	.WORD	052525	:	
	.WORD	146314	:	ADDRESS 020000 DATA PATTERNS
	.WORD	031463	:	
	.WORD	000377	:	ADDRESS 040000 DATA PATTERNS
	.WORD	177400	:	
	.WORD	000000	:	ADDRESS 060000 DATA PATTERNS
	.WORD	177777	:	

51\$:	ENDTST
Li0041:	TRAP C\$ETST


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7383
7384 :GO LOAD, READ AND CHECK MODULE SELECT RAM 0. THE FOLLOWING DATA
7385 :PATTERNS: 1, 2, 4, 10, 0, 0, 0, AND 0 WILL BE LOADED INTO CONSECUTIVE
7386 :LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS 0. THESE PATTERNS
7387 :WILL ENABLE THE FIRST 16K WORDS OF THE MEMORY SIMULATOR RAM TO BE
7388 :ADDRESSED.
7389
7390 021144 004737 011640 JSR PC,MSRAM0 ;LOAD, READ AND CHECK MODULE SELECT RAM 0
7391
7392 :GO LOAD, READ AND CHECK MODULE SELECT RAM 1. THE FOLLOWING DATA PATTERNS
7393 :WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
7394 :AT ADDRESS 0; 17, 0, 0 AND 0. THESE PATTERNS WILL ENABLE THE FIRST 32K
7395 :WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
7396
7397 021150 004737 012010 JSR PC,MSRAM1 ;LOAD, READ AND CHECK MODULE SELECT RAM 1
7398
7399 021154 005001 CLR R1 ;SETUP STARTING ADDRESS TO EQUAL ZERO
7400 021156 012702 023736 MOV #52$,R2 ;SETUP POINTER TO DATA TABLE
7401
7402 021162 1$: BGNSEG
7403 021162 104404 TRAP C$BSEG
7404
7405 :SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7406 :REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7407
7408 021164 004737 012212 JSR PC,SLCTTE ;SELECT TARGET EMULATOR MODULE
7409
7410 :SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL 'BRKRES L'
7411 :BY TOGGING ADAL REGISTER BIT 0. ADAL10 H AND ADAL9 H SET TO ONES WILL
7412 :ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS. PULSING
7413 :THE SIGNAL 'BRKRES L' VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
7414 :TARGET EMULATOR MODULE. ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
7415 :BIT 15 ON A ZERO WILL CAUSE THE SIGNAL 'CKAI H' TO BE PULSED VIA THE
7416 :THE SIGNAL 'RASP L' LATER ON IN THIS TEST. ADAL REGISTER BIT 4 ON A
7417 :ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
7418 :THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
7419
7420 021170 012737 043020 002334 MOV #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
7421 021176 004737 012764 JSR PC,BRKRES ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
7422
7423 :SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
7424 :REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
7425 :REGISTER 6.
7426
7427 021202 004537 012232 JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
7428 021206 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
7429
7430 :SET HDAL REGISTER BITS 9,4,3 + 2 TO A ONE AND HDAL BITS 14 AND 11 TO A
7431 :ZERO. HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
7432 :AND CONTROL SIGNALS. HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
7433 :DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS. HDAL REGISTER
7434 :BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
7435 :HDAL REGISTER BITS 4 AND 3 SET TO ONES WILL SET THE SIGNALS XR/WLB H
7436 :AND XR/WHB H TO THE HIGH STATE. THESE SIGNALS WILL CAUSE THE SIGNAL
7437 :'REAT H' TO BE ASSERTED HIGH LATER IN THIS TEST WHEN THE SIGNALS XRAS H
7438 :AND XCAS H ARE ASSERTED HIGH.

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7439
7440 021210 012737 001034 002346      MOV      #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SET HDAL BITS 9,4,3 + 2 TO ONES
7441 021216 04737 011214              JSR      PC,LDRDT6 ;GO LOAD, READ AND CHECK HDAL REGISTER
7442 021222 00140                      BEQ      2$ ;IF LOADED OK THEN CONTINUE
7443 021224                                ERRDF   12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
7444 021224 104455                      TRAP    C$ERDF
7445 021226 000014                      .WORD  12
7446 021230 003754                      .WORD  HDALRG
7447 021232 006730                      .WORD  T06ERR
7448 021234                                CKLOOP
7449 021234 104406                      TRAP    C$CLP1
7450
7451                                ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
7452                                ;REGISTER 4. PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
7453                                ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY "BRKRES L".
7454
7455 021236 005037 002340              2$:    CLR      T4LOAD ;SETUP TO CLEAR ALL OTHER R/W BITS
7456 021242 004737 012704              JSR      PC,CLRPSM ;PULSE INVD L VIA VDAL2 H
7457
7458                                ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4. ON
7459                                ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
7460                                ;BE WRITTEN OR READ.
7461
7462 021246 004537 012232              JSR      R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
7463 021252 000004                      .WORD  MODE ;SELECT THE MODE REGISTER
7464
7465                                ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
7466                                ;ZEROES. MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
7467
7468 021254 005037 002346              CLR      T6LOAD ;SETUP TO CLEAR ALL MODE REGISTER BITS
7469 021260 004737 011214              JSR      PC,LDRDT6 ;GO LOAD, READ AND CHECK MODE REGISTER
7470 021264 001405                      BEQ      3$ ;IF LOADED OK THEN CONTINUE
7471 021266                                ERRDF   12,MODREG,T06ERR ;MODE REGISTER NOT EQUAL EXPECTED
7472 021266 104455                      TRAP    C$ERDF
7473 021270 0000.4                      .WORD  12
7474 021272 004000                      .WORD  MODREG
7475 021274 006730                      .WORD  T06ERR
7476 021276                                CKLOOP
7477 021276 104406                      TRAP    C$CLP1
7478
7479                                ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
7480                                ;TO A 2. THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
7481                                ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
7482                                ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
7483                                ;TER WILL BE ADDRESSED.
7484
7485 021300 004537 012232              3$:    JSR      R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
7486 021304 000002                      .WORD  FDAL ;SELECT EOAI AND FDAL REGISTER
7487
7488                                ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER. THE EOAI REGISTER WILL
7489                                ;BE LOADED AND CHECKED FOR ZEROES. THE FDAL REGISTER WILL BE LOADED AND
7490                                ;CHECKED FOR A DATA PATTERN OF ONE (FDALO H = 1).
7491
7492 021306 012737 000001 002346      MOV      #FDALO,T6LOAD ;SETUP EOAI AND FDAL REG DATA PATTERN
7493 021314 004737 011214              JSR      PC,LDRDT6 ;GO LOAD, READ AND CHECK EOAI + FDAL REG
7494 021320 001405                      BEQ      4$ ;IF LOADED OK THEN CONTINUE

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7495 021322          ERRDF 12,EOAIFD,T06ERR      ;EOAI OR FDAL REGISTER ERROR
7496 021322 104455  TRAP   C$ERDF
7497 021324 000014  .WORD 12
7498 021326 004045  .WORD EOAIFD
7499 021330 006730  .WORD T06ERR
7500 021332          CKLOOP
7501 021332 104406  TRAP   C$CLP1
7502
7503          ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
7504          ;CHANGES OCCURED DOING THE PAST SEQUENCES.
7505
7506 021334 004737 011176 4$: JSR    PC,READT4          ;READ AND CHECK VDAL REGISTER
7507 021340 001405          BEQ    5$              ;IF NO CHANGES THEN CONTINUE
7508 021342          ERRDF 11,VDALRG,T4EROR      ;VDAL OR PAUSE STATE MACHINE ERROR
7509 021342 104455  TRAP   C$ERDF
7510 021344 000013  .WORD 11
7511 021346 003706  .WORD VDALRG
7512 021350 006714  .WORD T4EROR
7513 021352          CKLOOP
7514 021352 104406  TRAP   C$CLP1
7515
7516          ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7517          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7518
7519 021354 004737 011246 5$: JSR    PC,SLCTMS          ;SELECT MEMORY SIMULATOR MODULE
7520
7521          ;SET THE SIGNAL 'MP H' TO A ONE AND PULSE THE SIGNAL 'RST H'. THE
7522          ;SIGNAL 'MP H' ON A ONE WILL ENABLE THE MAP PROTECTION RAM BITS
7523          ;TO THE SYSTEM BUS ALONG WITH THE SIGNAL MSBRK H. PULSING THE SIGNAL
7524          ;'RST H' WILL PRESET THE RDV AND WRV FLIP-FLOP'S TO A ONE. WHEN THE
7525          ;FLIP-FLOP'S ARE SET TO A ONE, THE SIGNAL 'BRK L' WILL BE ASSERTED
7526          ;HIGH, THUS NO BREAK CONDITION IS GENERATED FROM THE MEMORY SIMULATOR.
7527
7528 021360 112737 000004 002234 MOVB  #MPH,SLOAD      ;SET THE SIGNAL MP H TO HIGH STATE
7529 021366 004737 011266 JSR    PC,MSRSTH      ;SET RST H TO ONE AND PULSE RST H
7530
7531          ;LOAD MEMORY SIMULATOR RAM ADDRESS TO BE TESTED INTO CONTROL REGISTER 4.
7532          ;THE ADDRESSES TO BE TESTED ARE 000000, 020000, 040000 OR 060000.
7533
7534 021372 010137 002254 MOV    R1,S4LOAD      ;SETUP TO LOAD ADDRESS TO BE TESTED
7535 021376 004737 010604 JSR    PC,LDRDS4      ;LOAD READ AND CHECK CONTROL REG 4
7536 021402 001405          BEQ    6$              ;IF LOADED OK THEN CONTINUE
7537 021404          ERRDF 3,MSADRG,S4EROR      ;MSAD 15:0 REGISTER ERROR
7538 021404 104455  TRAP   C$ERDF
7539 021406 000003  .WORD 3
7540 021410 002506  .WORD MSADRG
7541 021412 005334  .WORD S4EROR
7542 021414          CKLOOP
7543 021414 104406  TRAP   C$CLP1
7544
7545          ;CLEAR BITS MSEL1 H, MSEL0 H, MSAD17 H AND MSAD16 H IN CONTROL REGISTER
7546          ;2. MSEL0 H AND MSEL1 H ON A ZERO WILL CAUSE THE SIGNAL 'SSM L' TO BE
7547          ;ASSERTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6. ON A WRITE
7548          ;OR READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE WRITTEN INTO OR
7549          ;READ FROM MEMORY SIMULATOR RAM ADDRESSES BY CONTROL REGISTER 2 AND 4.
7550          ;THE MEMORY SIMULATOR RAM'S ARE ENABLED BY THE DATA PATTERNS PREVIOUSLY

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7551                                     ;WRITTEN INTO MODULE SELECT RAMS 0 AND 1. MSAD17 H AND MSAD16 H WILL BE
7552                                     ;LOADED AND CHECKED WITH ZEROES. THE PROGRAM WILL EXPECT CONTROL REGIS-
7553                                     ;TER 2 BITS 'ESR H' AND 'WREN H' TO BE READ AS ONES AS A RESULT OF MAP
7554                                     ;PROTECTION RAM BITS 'MPIN H' AND 'WRE H' BEING SET TO ONES.
7555
7556 021416 005037 002244 6$: CLR S2LOAD ;SET ALL BITS IN REG 2 TO ZEROES
7557 021422 013737 002244 002246 MOV S2LOAD,S2GOOD ;COPY DATA LOADED TO EXPECTED
7558 021430 052737 000140 002246 BIS #ESRH!WRENH,S2GOOD ;EXPECT ESR H AND WREN H TO BE ONES
7559 021436 012737 177400 002250 MOV #177400,S2MASK ;SETUP TO COMPARE LOW BYTE
7560 021444 004737 010552 JSR PC,LDRD2S ;LOAD, READ AND CHECK CONTROL REG 2
7561 021450 001405 BEQ 7$ ;IF LOADED OK THEN CONTINUE
7562 021452 ERRDF 2,S2EROR ;CONTROL REGISTER 2 NOT = EXPECTED
7563 021452 104455 TRAP C$ERDF
7564 021454 000002 .WORD 2
7565 021456 000000 .WORD 0
7566 021460 005320 .WORD S2EROR
7567 021462 CKLOOP
7568 021462 104406 TRAP C$CLP1
7569
7570                                     ;LOAD DATA PATTERN INTO MEMORY SIMULATOR RAM ADDRESSED BY CONTROL
7571                                     ;REGISTER 2 AND 4. ONE OF THE FOLLOWING DATA PATTERNS WILL BE LOADED
7572                                     ;INTO THE TEST ADDRESS LISTED BELOW:
7573                                     ; ADDRESS 000000 WILL BE LOADED WITH 052652
7574                                     ; ADDRESS 020000 WILL BE LOADED WITH 146063
7575                                     ; ADDRESS 040000 WILL BE LOADED WITH 000377
7576                                     ; ADDRESS 060000 WILL BE LOADED WITH 125125
7577
7578 021464 005037 002264 7$: CLR S6MASK ;SETUP TO COMPARE ALL BITS
7579 021470 011237 002260 MOV (R2),S6LOAD ;GET THE DATA PATTERN FROM THE TABLE
7580 021474 004737 010630 JSR PC,LDRDS6 ;GO LOAD, READ AND CHECK RAM LOCATION
7581 021500 001405 BEQ 8$ ;IF LOADED OK THEN CONTINUE
7582 021502 ERRDF 4,MSGMSR,S6ALLR ;DATA ERROR IN MEMORY SIMULATOR RAM
7583 021502 104455 TRAP C$ERDF
7584 021504 000004 .WORD 4
7585 021506 002743 .WORD MSGMSR
7586 021510 005454 .WORD S6ALLR
7587 021512 CKLOOP
7588 021512 104406 TRAP C$CLP1
7589
7590                                     ;SET THE SIGNAL 'CTS H' TO A ONE IN CONTROL REGISTER 0. THIS WILL
7591                                     ;ENABLE THE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR LOGIC.
7592                                     ;IN THIS TEST, 'CTS H' ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO
7593                                     ;THE MEMORY SIMULATOR MODULE AND THE MEMORY SIMULATOR RAM DATA ONTO THE
7594                                     ;SYSTEM BUS.
7595
7596 021514 052737 000002 002234 8$: BIS #CTSH,S0LOAD ;SETUP BIT TO BE LOADED
7597 021522 004737 010504 JSR PC,LDRDS0 ;GO LOAD, READ AND CHECK CONTROL REG 2
7598 021526 001405 BEQ 9$ ;IF LOADED OK THEN CONTINUE
7599 021530 ERRDF 1,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
7600 021530 104455 TRAP C$ERDF
7601 021532 000001 .WORD 1
7602 021534 000000 .WORD 0
7603 021536 005304 .WORD S0EROR
7604 021540 CKLOOP
7605 021540 104406 TRAP C$CLP1
7606

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7607                                     ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7608                                     ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7609
7610 021542 004737 012212          9$: JSR      PC,SLCTTE
7611
7612                                     ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
7613                                     ;2:0 TO A 0. THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH THE
7614                                     ;TEST PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6. THE DIAGNOSTIC
7615                                     ;ADDRESS REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER
7616                                     ;BIT 9 BEING SET TO A ONE PREVIOUSLY. ON A READ COMMAND TO CONTROL
7617                                     ;REGISTER 6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
7618
7619
7620 021546 004537 012232          JSR      R5,SELTERR          ;SELECT REGISTER SPECIFIED BY NEXT WORD
7621 021552 000000                  .WORD   ADDRES          ;SELECT THE DIAG ADDRESS REG AND ADDR BUS
7622
7623                                     ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
7624                                     ;FOLLOWING ADDRESSES: 000000, 020000, 040000, OR 060000.
7625
7626 021554 010137 002346          MOV      R1,T6LOAD          ;GET THE TEST ADDRESS TO BE LOADED
7627 021560 004737 011214          JSK      PC,LDRDT6          ;GO LOAD, READ + CHECK DIAG ADDRESS REG
7628 021564 001405                  BEQ      10$                ;IF LOADED OK THEN CONTINUE
7629 021566                          ERRDF   12,ADDRRG,T06ERR      ;DIAGNOSTIC ADDRESS REGISTER ERROR
7630 021566 104455                  TRAP    C$ERDF
7631 021570 000014                  .WORD   12
7632 021572 004142                  .WORD   ADDRREG
7633 021574 006730                  .WORD   T06ERR
7634 021576                          CKLOOP
7635 021576 104406                  TRAP    C$CLP1
7636
7637                                     ;SELECT HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3. THE
7638                                     ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
7639                                     ;CONTROL REGISTER 6.
7640
7641 021600 004537 012232          10$: JSR      R5,SELTERR          ;SELECT REGISTER SPECIFIED BY NEXT WORD
7642 021604 000003                  .WORD   HDAL              ;SELECT THE HDAL REGISTER
7643 021606 012737 001034 002346  MOV      #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;GET BITS PREVIOUSLY LOADED
7644
7645                                     ;START A T-11 MACHINE CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE
7646                                     ; 1. SET XRAS H AND PRAS H TO THE HIGH STATE
7647                                     ; 2. SET XCAS H AND PCAS H TO THE HIGH STATE
7648                                     ; 3. SET XPI L AND PPI L TO THE LOW STATE
7649                                     ;SETTING THE SIGNAL PRAS H TO THE HIGH STATE WILL CAUSE THE SIGNAL
7650                                     ;"ADVAL H" TO GO FROM A LOW TO A HIGH STATE, THUS CLOCKING THE SYSTEM
7651                                     ;ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR ADDRESS BUS LATCHES.
7652                                     ;WHEN THE SIGNALS XRAS H AND XCAS H ARE ASSERTED
7653                                     ;HIGH, THE SIGNAL REAT H WILL GO FROM A LOW TO A HIGH STATE, THUS CAUSING
7654                                     ;THE SIGNAL READ H TO GO FROM A LOW TO A HIGH STATE. THE TARGET EMULATORS
7655                                     ;SIGNAL READ H ALONG WITH THE MEMORY SIMULATOR'S SIGNALS CTS H AND ESR H
7656                                     ;WILL CAUSE THE MEMORY SIMULATOR RAM DATA TO BE PUT ONTO THE SYSTEM DATA
7657                                     ;BUS. WHEN THE TARGET EMULATORS SIGNAL REAT H IS ASSERTED HIGH, THE
7658                                     ;TARGET EMULATORS SIGNAL MSDI H WILL BE ASSERTED HIGH, THUS ENABLING
7659                                     ;THE SYSTEM DATA BUS TO THE TARGET EMULATORS EODAL BUS. THE MEMORY
7660                                     ;SIMULATOR RAM'S ARE ADDRESSED BY THE MEMORY SIMULATOR SYSTEM BUS ADDRESS
7661                                     ;LATCHES WHICH WERE CLOCKED BY THE SIGNAL ADVAL H. THE DATA ON SYS EM
7662                                     ;ADDRESS BUS COMES FROM THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER.

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7663
7664 021614 004737 012276      JSR      PC,XRASH      ;SET XRAS H AND PRAS H TO HIGH STATE
7665 021620 004737 012402      JSR      PC,XCASH      ;SET XCAS H AND PCAS H TO HIGH STATE
7666 021624 004737 012506      JSR      PC,XPIH       ;SET XPI H AND PPI H TO THE LOW STATE
7667
7668                               ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H ARE
7669                               ;ASSERTED HIGH (1'S).
7670
7671 021630 012737 000110 002342  MOV      #VDAL6!VDAL3,T4GOOD ;EXPECT READ H AND MSDI H TO BE ONES
7672 021636 004737 011176         JSR      PC,READT4      ;READ VDAL AND PAUSE STATE MACHINE REG
7673 021642 001405         BEQ      11$           ;IF DATA OK THEN CONTINUE
7674 021644         ERRDF  11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
7675 021644 104455         TRAP    C$ERDF
7676 021646 000013         .WORD  11
7677 021650 003706         .WORD  VDALRG
7678 021652 006714         .WORD  T4EROR
7679 021654         CKLOOP
7680 021654 104406         TRAP    C$CLP1
7681
7682                               ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7683                               ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7684
7685 021656 004737 011246 11$: JSR      PC,SLCTMS      ;SELECT THE MEMORY SIMULATOR MODULE
7686
7687                               ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
7688                               ;TARGET EMULATOR MODULE SET THE SIGNALS ADVAL H AND READ H TO THE
7689                               ;HIGH STATE FROM THE LOW STATE.
7690
7691 021662 004737 010520      JSR      PC,READS0     ;READ AND CHECK CONTROL REGISTER 0
7692 021666 001405      BEQ      12$           ;IF NO CHANGES THEN CONTINUE
7693 021670         ERRDF  1,S0EROR ;CONTROL REGISTER 0 NOT = EXPECTED
7694 021670 104455         TRAP    C$ERDF
7695 021672 000001         .WORD  1
7696 021674 000000         .WORD  0
7697 021676 005304         .WORD  S0EROR
7698 021700         CKLOOP
7699 021700 104406         TRAP    C$CLP1
7700
7701                               ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
7702                               ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
7703                               ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H. THE SIGNAL ADVAL H
7704                               ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
7705                               ;SIGNAL PRAS H WAS SET HIGH FROM THE LOW STATE. THE MEMORY SIMULATORS
7706                               ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
7707                               ;BITS VIA THE SIGNALS CTS H AND CTS L.
7708
7709 021702 010137 002254 12$: MOV      R1,S4LOAD      ;GET THE EXPECTED ADDRESS LOADED
7710 021706 004737 010612      JSR      PC,READS4     ;READ AND CHECK CONTROL REGISTER 4
7711 021712 001405      BEQ      13$           ;IF DATA = TE DIAG ADDRESS REG - CONT
7712 021714         ERRDF  3,TEMSAD,S04ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
7713 021714 104455         TRAP    C$ERDF
7714 021716 000003         .WORD  3
7715 021720 002532         .WORD  TEMSAD
7716 021722 005404         .WORD  S04ERR
7717 021724         CKLOOP
7718 021724 104406         TRAP    C$CLP1
  
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7719
7720 ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
7721 ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
7722 ;ZEROS FOR THESE TWO ADDRESSES. ADDRESS BITS 17 AND 16 WERE CLOCKED
7723 ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
7724 ;ADVAL H. THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
7725 ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE FROM
7726 ;THE LOW STATE. THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
7727 ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
7728 ;MEMORY SIMULATOR MODULE.
7729
7730 021726 052737 000014 002250 13$: BIS #MSEL0!MSEL1,S2MASK ;IGNORE TRI-STATED BITS WHEN CTS H SET
7731 021734 005037 002244 CLR S2LOAD ;EXPECT MSAD 17:16 TO BE ZERO
7732 021740 013737 002244 002246 MOV S2LOAD,S2GOOD ;COPY DATA LOADED TO EXPECTED
7733 021746 052737 000140 002246 BIS #ESRH!WRENH,S2GOOD ;EXPECT MAP PROTECT BITS TO BE ONES
7734 021754 004737 010560 JSR PC,READS2 ;READ AND CHECK CONTROL REGISTER 2
7735 021760 001405 BEQ 14$ ;IF DATA OK THEN CONTINUE
7736 021762 ERRDF 2,TEMSA1,S02ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
7737 021762 104455 TRAP C$ERDF
7738 021764 000002 .WORD 2
7739 021766 002406 .WORD TEMSA1
7740 021770 005364 .WORD S02ERR
7741 021772 CKLOOP
7742 021772 104406 TRAP C$CLP1
7743
7744 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7745 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7746
7747 021774 004737 012212 14$: JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE
7748
7749 ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO A 7. THE EODAL BUS
7750 ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
7751
7752 022000 004537 012232 JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
7753 022004 000007 .WORD EODAL ;SELECT THE EODAL BUS TO BE READ
7754
7755 ;AT THIS TIME THE MEMORY SIMULATOR RAM DATA SHOULD BE ENABLED ON THE
7756 ;SYSTEM DATA BUS AND ENABLED TO THE TARGET EMULATORS EODAL BUS VIA THE
7757 ;TARGET EMULATOR SIGNALS READ H AND MSDI H RESPECTIVELY. THE MEMORY
7758 ;SIMULATOR RAM IS ADDRESSED BY THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS
7759 ;REGISTER WHICH WAS CLOCKED INTO THE MEMORY SIMULATOR'S SYSTEM ADDRESS
7760 ;BUS LATCHES VIA THE SIGNAL ADVAL H. THE DATA PATTERNS LOADED INTO
7761 ;THE TEST ADDRESSES OF THE MEMORY SIMULATOR RAM'S ARE LISTED BELOW:
7762 ; ADDRESS 000000 WILL BE LOADED WITH 052652
7763 ; ADDRESS 020000 WILL BE LOADED WITH 146063
7764 ; ADDRESS 040000 WILL BE LOADED WITH 000377
7765 ; ADDRESS 060000 WILL BE LOADED WITH 125125
7766
7767 022006 013737 002260 002346 MOV S6LOAD,T6LOAD ;GET DATA LOADED INTO MS RAM ADDRESSED
7768 022014 00737 011222 JSR PC,READT6 ;READ SYSTEM DATA BUS ON THE EODAL BUS
7769 022020 01405 BEQ 15$ ;IF DATA = MS RAM DATA THEN CONTINUE
7770 022022 ERRDF 12,MSTEDE,T6ALLR ;MS RAM DATA TO TE EODAL BUS ERROR
7771 022022 104455 TRAP C$ERDF
7772 022024 000014 .WORD 12
7773 022026 004241 .WORD MSTEDE
7774 022030 006744 .WORD T6ALLR

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7775 022032          CKLOOP
7776 022032 104406  TRAP   C$CLP1
7777
7778                ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6. THE EIDAL BUS
7779                ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
7780
7781 022034 004537 012232 15$: JSR    R5,SELTER          ;SELECT REGISTER SPECIFIED BY NEXT WORD
7782 022040 000006          .WORD  EIDAL          ;SELECT THE EIDAL BUS TO BE READ
7783
7784                ;IN THE PREVIOUS DATA CHECK, THE PROGRAM VERIFIED THAT THE MEMORY SIMU-
7785                ;LATOR RAM DATA WAS ENBALED TO THE EODAL BUS VIA THE SYSTEM DATA BUS.
7786                ;IN THIS SECTION, THE PROGRAM WILL CHECK THAT THE EODAL BUS IS ENABLED
7787                ;TO THE EIDAL BUS VIA THE CDAL BUS AS A RESULT OF THE SIGNALS COHB L AND
7788                ;COLB L BEING ASSERTED LOW. THE SIGNALS COHB L AND COLB L ARE ASSERTED
7789                ;LOW AS A RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED HIGH: ETR L,
7790                ;PR/WLB H, PR/WHB H, PPI H, DMG L, AND MR11 L. THE DATA READ SHOULD BE
7791                ;THE SAME AS THAT WHICH WAS ENABLED TO THE EODAL BUS. THE DATA PATTERNS
7792                ;LOADED INTO THE TEST ADDRESS OF THE MEMORY SIMULATOR RAMS ARE AS FOLLOWS:
7793                ; ADDRESS 000000 WILL BE LOADED WITH 052652
7794                ; ADDRESS 020000 WILL BE LOADED WITH 146063
7795                ; ADDRESS 040000 WILL BE LOADED WITH 000377
7796                ; ADDRESS 060000 WILL BE LOADED WITH 125125
7797
7798 022042 013737 002260 002346 MOV    S6LOAD,T6LOAD          ;GET DATA LOADED INTO MS RAM ADDRESSED
7799 022050 004737 011222          JSR    PC,READT6          ;READ SYSTEM DATA BUS ON EIDAL VIA EODAL
7800 022054 001405          BEQ    16$                ;IF DATA OK THEN CONTINUE
7801 022056          ERRDF  12,MSTEEI,T6ALLR          ;MS RAM DATA TO EIDAL BUS VIA EODAL BUS
7802 022056 104455          TRAP   C$ERDF
7803 022060 000014          .WORD  12
7804 022062 004327          .WORD  MSTEEI
7805 022064 006744          .WORD  T6ALLR
7806 022066          CKLOOP
7807 022066 104406          TRAP   C$CLP1
7808
7809                ;IN THE PREVIOUS DATA CHECKS, MEMORY SIMULATOR RAM DATA WAS ENABLED TO
7810                ;THE SYSTEM DATA BUS WHICH ALSO WAS ENABLED TO THE EODAL, CDAL AND EIDAL
7811                ;BUSES. IN ADDITION TO THESE BUSES, MEMORY SIMULATOR RAM DATA WILL BE
7812                ;ENABLED TO THE TDAL BUS VIA THE CDAL BUS BY THE SIGNALS DTHB L AND
7813                ;DTLB H. THE SIGNALS DTHB L AND DTLB L ARE ASSERTED LOW AS A RESULT OF
7814                ;THE SIGNALS PSEL1 L, PSEL0 L, PBCLR L AND CPIW L BEING ASSERTED HIGH AND
7815                ;THE T-11 SIGNAL CCAS H BEING ASSERTED LOW. TO CAPTURE THE MEMORY
7816                ;SIMULATOR RAM DATA ON THE TDAL BUS, THE PROGRAM WILL SET VDAL2 H TO A
7817                ;ONE AND THEN A ZERO TO CLOCK THE TDAL BUS DATA INTO THE TDAL DIAGNOSTIC
7818                ;LATCHES.
7819
7820 022070 052737 000004 002340 16$: BIS    #VDAL2,T4LOAD          ;SET BIT TO CLOCK TDAL DIAG LATCHES
7821 022076 052737 000004 002342 BIS    #VDAL2,T4GOOD          ;EXPECT VDAL2 H TO BE SET ON READ
7822 022104 004737 011170          JSR    PC,LDRD4T          ;LOAD, READ AND CHECK VDAL REGISTER
7823 022110 001405          BEQ    17$                ;IF LOADED OK THEN CONTINUE
7824 022112          ERRDF  11,VDALRG,T4EROR          ;VDAL REGISTER NOT EQUAL EXPECTED
7825 022112 104455          TRAP   C$ERDF
7826 022114 000013          .WORD  11
7827 022116 003706          .WORD  VDALRG
7828 022120 006714          .WORD  T4EROR
7829 022122          CKLOOP
7830 022122 104406          TRAP   C$CLP1

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7831 022124 042737 000004 002340 $: BIC #VDAL2,T4LOAD ;SET CLOCK SIGNAL TO A ZERO
7832 022132 042737 000004 002342 BIC #VDAL2,T4GOOD ;EXPECT VDAL2 H TO BE 0 ON A READ
7833 022140 004737 011170 JSR PC,LDRD4T ;LOAD, READ AND CHECK VDAL REGISTER
7834 022144 001405 BEQ 18$ ;IF LOADED OK THEN CONTINUE
7835 022146 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
7836 022146 104455 TRAP C$ERDF
7837 022150 000013 .WORD 11
7838 022152 003706 .WORD VDA'RG
7839 022154 006714 .WORD T4EROR
7840 022156 CKLOOP
7841 022156 104406 TRAP C$CLP1
7842
7843 ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
7844 ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
7845 ;REGISTER 6.
7846
7847 022160 004537 012232 18$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
7848 022164 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
7849
7850 ;FINISH THE T-11 TIMING CYCLE BY DOING THE FOLLOWING SEQUENCE:
7851 ; 1. SET XCAS H AND PCAS H TO THE LOW STATE
7852 ; 2. SET XPI L AND PPI L TO THE HIGH STATE
7853 ; 3. SET XRAS H AND PRAS H TO THE LOW STATE
7854
7855 022166 012737 001034 002346 MOV #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SETUP PREVIOUSLY LOADED BITS
7856 022174 004737 012434 JSR PC,XCASL ;SET XCAS H AND PCAS H TO LOW STATE
7857 022200 004737 012540 JSR PC,XPIL ;SET XPI L AND PPI L TO THE HIGH STATE
7858 022204 004737 012330 JSR PC,XRASL ;SET XRAS H AND PRAS H TO LOW STATE
7859
7860 ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H
7861 ;WENT TO A ZERO AS A RESULT OF SETTING THE SIGNALS XCAS H AND XRAS H
7862 ;TO THE LOW STATE.
7863
7864 022210 005037 002342 CLR T4GOOD ;EXPECT VDAL REGISTER TO BE A 0
7865 022214 004737 011176 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
7866 022220 001405 BEQ 19$ ;IF OK THEN CONTINUE
7867 022222 ERRDF 11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
7868 022222 104455 TRAP C$ERDF
7869 022224 000013 .WORD 11
7870 022226 003706 .WORD VDALRG
7871 022230 006714 .WORD T4EROR
7872 022232 CKLOOP
7873 022232 104406 TRAP C$CLP1
7874
7875 ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7876 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7877
7878 022234 004737 011246 19$: JSR PC,SLCTMS ;SELECT THE MEMORY SIMULATOR MODULE
7879
7880 ;SET THE SIGNAL CTS H TO THE LOW STATE BY CLEARING THE BIT IN CONTROL
7881 ;REGISTER 0. THIS WILL DISABLE THE SYSTEM BUS SIGNALS TO AND FROM
7882 ;THE MEMORY SIMULATOR MODULE.
7883
7884 022240 112737 000004 002234 MOVB #MPH,SOLOAD ;CLEAR CTS H AND LEAVE MP H SET TO A 1
7885 022246 004737 010504 JSR PC,LDRDSO ;LOAD, READ AND CHECK CONTROL REG 0
7886 022252 001405 BEQ 20$ ;IF LOADED OK THEN CONTINUE

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7887 022254          ERRDF 1,,S0EROR          ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
7888 022254 104455  TRAP  C$ERDF
7889 022256 000001  .WORD 1
7890 022260 000000  .WORD 0
7891 022262 005304  .WORD S0EROR
7892 J22264
7893 022264 104406  CKLOOP
7894 TRAP  C$CLP1
7895
7896 ;READ CONTROL REGISTER 4 TO CHECK THAT THE MEMORY SIMULATOR ADDRESS
7897 ;LOADED PREVIOUSLY IS STILL LOADED
7898 022266 004737 010612 20$: JSR  PC,READS4          ;READ AND CHECK CONTROL REGISTER 4
7899 022272 001405  BEQ  21$          ;IF ADDRESS 0 THEN CONTINUE
7900 022274          ERRDF 3,MSADRG,S4EROR      ;MSAD 15:0 REGISTER ERROR
7901 022274 104455  TRAP  C$ERDF
7902 022276 000003  .WORD 3
7903 022300 002506  .WORD MSADRG
7904 022302 005334  .WORD S4EROR
7905 022304          CKLOOP
7906 022304 104406  TRAP  C$CLP1
7907
7908 ;READ CONTROL REGISTER 0 TO CHECK THAT THE DATA LOADED INTO IT PREVIOUSLY
7909 ;HAS NOT CHANGED. THE FOLLOWING SIGNALS SHOULD BE READ AS ZEROES:
7910 ;MSAD16 H, MSAD17 H, MSEL0 L, MSEL1 L AND MSBRK H. THE SIGNALS ESR H
7911 ;AND WREN H SHOULD BE READ AS ONES.
7912
7913 022306 012737 177400 002250 21$: MOV  #177400,S2MASK      ;SETUP TO CHECK ALL OFF LOW BYTE
7914 022314 004737 010560 JSR  PC,READS2      ;READ AND CHECK CONTROL REGISTER 2
7915 022320 001405  BEQ  22$          ;IF NO CHANGE THEN CONTINUE
7916 022322          ERRDF 2,,S2EROR          ;CONTROL REGISTER 2 NOT EQUAL EXPECTED
7917 022322 104455  TRAP  C$ERDF
7918 022324 000002  .WORD 2
7919 022326 000000  .WORD 0
7920 022330 005320  .WORD S2EROR
7921 022332          CKLOOP
7922 022332 104406  TRAP  C$CLP1
7923
7924 ;WRITE INTO THE MEMORY SIMULATOR RAM'S TEST ADDRESS A DATA PATTERN OF
7925 ;ALL ZEROES. THIS IS DONE TO CHECK THAT DATA CAN BE WRITTEN BACK INTO
7926 ;THIS ADDRESS LATER ON IN THIS TEST IN 8 BIT MODE.
7927
7928 022334 005037 002260 22$: CLR  S6LOAD          ;SET NEW DATA PATTERN TO ALL ZEROES
7929 022340 004737 010630 JSR  PC,LDRDS6      ;GO LOAD, READ AND CHECK MEM SIM RAM LOC
7930 022344 001405  BEQ  23$          ;IF LOADED OK THEN CONTINUE
7931 022346          ERRDF 4,MSGMSR,S6ALLR      ;DATA ERROR IN MEMORY SIMULATOR RAM
7932 022346 104455  TRAP  C$ERDF
7933 022350 000004  .WORD 4
7934 022352 002743  .WORD MSGMSR
7935 022354 005454  .WORD S6ALLR
7936 022356          CKLOOP
7937 022356 104406  TRAP  C$CLP1
7938
7939 ;SET THE SIGNALS CTS H AND 8 BIT H TO ONES IN CONTROL REGISTER 0. CTS H
7940 ;ON A ONE WILL ENABLE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR
7941 ;MODULE. 8 BIT H ON A ONE WILL SET THE MEMORY SIMULATOR MODULE TO 8 BIT
7942 ;DATA MODE.

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7943
7944 022360 052737 000012 002234 23$: BIS #CTSH!BIT8H,SLOAD ;SETUP BITS TO BE LOADED
7945 022366 004737 010504 JSR PC,LDRDSO ;LOAD, READ AND CHECK REGISTER 0
7946 022372 001405 BEQ 24$ ;IF LOADED OK THEN CONTINUE
7947 022374 ERRDF 1,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
7948 022374 104455 TRAP C$ERRDF
7949 022376 000001 .WORD 1
7950 022400 000000 .WORD 0
7951 022402 005304 .WORD S0EROR
7952 022404 CKLOOP
7953 022404 104406 TRAP C$CLP1
7954
7955 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7956 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7957
7958 022406 004737 012212 24$: JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE.
7959
7960 ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 2. THE
7961 ;EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR READ COMMAND TO
7962 ;CONTROL REGISTER 6.
7963
7964 022412 004537 012232 JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
7965 022416 000002 .WORD FDAL ;SELECT EOAI AND FDAL REGISTER
7966
7967 ;LOAD, READ AND CHECK EOAI AND FDAL REGISTER. THE EOAI REGISTER WILL BE
7968 ;LOADED AND CHECKED FOR A DATA PATTERN OF ALL ZEROES. THE FDAL REGISTER
7969 ;WILL BE LOADED AND CHECKED FOR A DATA PATTERN OF 3 (FDAL1 H AND FDAL0 H).
7970 ;FDAL0 H ON A ONE WILL SELECT THE EOAI REGISTER TO BE READ ON A READ COMMAND
7971 ;TO CONTROL REGISTER 6 INSTEAD OF THE CTL REGISTER. FDAL1 H ON A ONE WILL
7972 ;ENABLE THE SIGNALS WR HB H AND WR LB H TO THE SYSTEM BUS WHEN THE SIGNAL
7973 ;DMG L IS ASSERTED LOW LATER ON IN THIS TEST.
7974
7975 022420 012737 000003 002346 MOV #FDAL1!FDAL0,T6LOAD ;SETUP BITS TO BE LOADED
7976 022426 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK EOAI AND FDAL REGISTER
7977 022432 001405 BEQ 25$ ;IF LOADED OK THEN CONTINUE
7978 022434 ERRDF 12,EOAIFD,T06ERR ;EOAI 7:0 OR FDAL 7:0 REGISTER ERROR
7979 022434 104455 TRAP C$ERRDF
7980 022436 000014 .WORD 12
7981 022440 004045 .WORD EOAIFD
7982 022442 006730 .WORD T06ERR
7983 022444 CKLOOP
7984 022444 104406 TRAP C$CLP1
7985
7986 ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL REGISTER
7987 ;WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
7988
7989 022446 004537 012232 25$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
7990 022452 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
7991
7992 ;SET THE SIGNALS PSEL0 L AND PSEL1 L TO THE LOW STATE BY SETTING HDAL
7993 ;REGISTER BITS 5 AND 6 TO ONES. SETTING THESE SIGNALS LOW WILL CAUSE
7994 ;THE SIGNALS DBHB L AND DBLB L TO BE ASSERTED LOW THUS ENABLING THE
7995 ;TDAL BUS TO THE CDAL BUS AND EIDAL BUS. SETTING PSEL0 L AND PSEL1 L
7996 ;WILL ALSO CAUSE THE SIGNAL DMG L TO BE ASSERTED LOW. SET THE SIGNALS
7997 ;XR/WHB L AND XR/WLB L TO THE HIGH STATE BY SETTING HDAL REGISTER BITS
7998 ;4 AND 3 TO A ZERO. THIS WILL SET THE READ/WRITE CONTROL LOGIC TO DO

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7999 ;A WRITE WHEN THE SIGNAL XPI H IS SET HIGH. HDAL9 H WILL BE SET TO A
8000 ;ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS
8001 ;BUS. THE DIAGNOSTIC ADDRESS REGISTER WAS LOADED WITH THE TEST ADDRESS EARLIER
8002 ;IN THIS TEST. HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM
8003 ;TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS.
8004
8005 022454 012737 001144 002346 MOV #HDAL9!HDAL6!HDAL5!HDAL2,T6LOAD ;SETUP BITS TO BE LOADED
8006 022462 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK HDAL REGISTER
8007 022466 001405 BEQ 26$ ;IF LOADED OK THEN CONTINUE
8008 022470 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
8009 022470 104455 TRAP C$ERDF
8010 022472 000014 .WORD 12
8011 022474 003754 .WORD HDALRG
8012 022476 006730 .WORD T06ERR
8013 022500 CKLOOP
8014 022500 104406 TRAP C$CLP1
8015
8016 ;SET VDAL0 H TO A ONE TO ENABLE THE OUTPUTS OF THE TDAL DIAGNOSTIC
8017 ;LATCHES ONTO THE TDAL BUS. THE TDAL BUS WILL BE ENABLED TO THE CDAL
8018 ;BUS VIA DBHB L AND DBLB L. THE CDAL BUS WILL BE ENABLED TO THE EIDAL
8019 ;BUS UNCONDITIONALLY.
8020
8021 022502 012737 000001 002340 26$: MOV #VDALO,T4LOAD ;SETUP BIT TO BE LOADED
8022 022510 004737 011162 JSR PC,LDRDT4 ;LOAD, READ AND CHECK VDAL REGISTER
8023 022514 001405 BEQ 27$ ;IF LOADED OK THEN CONTINUE
8024 022516 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
8025 022516 104455 TRAP C$ERDF
8026 022520 000013 .WORD 11
8027 022522 003706 .WORD VDALRG
8028 022524 006714 .WORD T4EROR
8029 022526 CKLOOP
8030 022526 104406 TRAP C$CLP1
8031
8032 ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6. ON A READ
8033 ;COMMAND TO CONTROL REGISTER 6 THE EIDAL BUS WILL BE READ.
8034
8035 022530 004537 012232 27$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
8036 022534 000006 .WORD EIDAL ;SELECT THE EIDAL BUS TO BE READ
8037
8038 ;AT THIS POINT IN TIME THE EIDAL BUS SHOULD HAVE THE TDAL DIAGNOSTIC
8039 ;LATCHES ENABLED TO IT BY THE SIGNALS DBHB L AND DBLB L BEING ASSERTED
8040 ;LOW AND VDAL0 H BEING SET TO A ONE. THE TDAL LATCHES WERE CLOCKED
8041 ;EARLIER IN THE TEST BY THE SIGNAL VDAL2 H. THESE LATCHES WERE
8042 ;CLOCKED WITH THE DATA FROM THE MEMORY SIMULATOR RAM DURING A READ
8043 ;OPERATION OF THE MEMORY SIMULATOR RAM TEST ADDRESS.
8044
8045 022536 011237 002346 MOV (R2),T6LOAD ;GET 1ST DATA WRITTEN TO MS RAM
8046 022542 004737 011222 JSR PC,READT6 ;READ AND CHECK EIDAL BUS
8047 022546 001405 BEQ 28$ ;IF DATA OK THEN CONTINUE
8048 022550 ERRDF 12,MSTETD,T6ALLR ;MS RAM DATA TO EIDAL BUS VIA TDAL BUS
8049 022550 104455 TRAP C$ERDF
8050 022552 000014 .WORD 12
8051 022554 004420 .WORD MSTETD
8052 022556 006744 .WORD T6ALLR
8053 022560 CKLOOP
8054 022560 104406 TRAP C$CLP1

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8055
8056
8057
8058
8059
8060 022562 004537 012232      28$: JSR    R5,SELTERR          ;SELECT REGISTER SPECIFIED BY NEXT WORD
8061 022566 000003              .WORD  HDAL              ;SELECT THE HDAL REGISTER
8062 022570 012737 001144 002346 MOV    #HDAL9!HDAL6!HDAL5!HDAL2,T6LOAD ;SETUP PREVIOUSLY LOADED BITS
8063
8064
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8078 022576 004737 012276      JSR    PC,XRASH          ;SET XRASH AND PRASH TO HIGH STATE
8079 022602 004737 012402      JSR    PC,XCASH          ;SET XCASH AND PCASH TO HIGH STATE
8080 022606 004737 012506      JSR    PC,XPIH           ;SET XPIH AND PPIH TO HIGH STATE
8081 022612 004737 012434      JSR    PC,XCASL          ;SET XCASH AND PCASH TO LOW STATE
8082 022616 004737 012540      JSR    PC,XPIL           ;SET XPIH AND PPIH TO LOW STATE
8083 022622 004737 012330      JSR    PC,XRASL          ;SET XRASH AND PRASH TO LOW STATE
8084
8085
8086
8087
8088 022626 052737 000020 002342 BIS    #VDAL4,T4GOOD      ;EXPECT EDEOC H TO BE SET TO A ONE
8089 022634 004737 011176      JSR    PC,READT4         ;READ AND CHECK VDAL REGISTER
8090 022640 001405              BEQ    29$               ;IF OK THEN CONTINUE
8091 022642              ERRDF  11,VDALRG,T4EROR  ;VDAL REGISTER NOT EQUAL EXPECTED
8092 022642 104455              TRAP  C$ERRDF
8093 022644 000013              .WORD  11
8094 022646 003706              .WORD  VDALRG
8095 022650 006714              .WORD  T4EROR
8096 022652              CKLOOP
8097 022652 104406              TRAP  C$CLP1
8098
8099
8100
8101
8102 022654 004737 011246      29$: JSR    PC,SLCTMS          ;SELECT THE MEMORY SIMULATOR MODULE
8103
8104
8105
8106
8107
8108 022660 004737 010520      JSR    PC,READSO         ;READ AND CHECK CONTROL REGISTER 0
8109 022664 001405              BEQ    30$               ;IF NO CHANGES THEN CONTINUE
8110 022666              ERRDF  1,,S0EROR        ;CONTROL REGISTER 0 NOT = EXPECTED

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;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
;REGISTER 6.
;AT THE PRESENT TIME, MEMORY SIMULATOR DATA WHICH WAS READ FROM THE TEST
;ADDRESS OF THE MEMORY SIMULATOR RAM EARLIER IN THIS TEST, IS NOW ENABLED
;TO THE SYSTEM DATA BUS VIA THE TDAL DIAGNOSTIC LATCHES. THIS DATA WAS
;PRESENT ON THE EIDAL BUS IN THE LAST DATA CHECK ABOVE. THE EIDAL BUS
;IS ENABLED TO THE SYSTEM DATA BUS BY THE SIGNAL MSDO H BEING ASSERTED
;HIGH. THE PROGRAM WILL NOW WRITE THE DATA ON THE SYSTEM DATA BUS BACK
;INTO THE TEST ADDRESS ON THE MEMORY SIUMULATOR RAM BY DOING A NORMAL T-11
;TIMING CYCLE. WHEN PRASH IS SET HIGH, THE ADDRESS BUS WHICH CONTAINS
;THE DIAGNOSTIC ADDRESS REGISTER DATA, WILL BE CLOCKED INTO THE MEMORY
;SIMULATOR SYSTEM ADDRESS BUS LATCHES. WHEN XPIH IS SET HIGH IN THE
;FOLLOWING TIMING SEQUENCE, THE DATA WILL BE WRITTEN INTO THE LOW BYTE
;OF THE MEMORY SIMULATOR RAM ADDRESS. THE WRITE SIGNALS FROM THE TARGET
;EMULATOR MODULE TO THE MEMORY SIMULATOR MODULE ARE WT HB H AND WT LB H.

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;READ VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A ONE
;IN THE VDAL REGISTER AS A RESULT OF THE ABOVE T-11 TIMING SEQUENCE.

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;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE ON CONTROL
;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.

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8111 022666 104455 TRAP C$ERDF
8112 022670 000001 .WORD 1
8113 022672 000000 .WORD 0
8114 022674 005304 .WORD S0EROR
8115 022676 CKLOOP
8116 022676 104406 TRAP C$CLP1
8117
8118 ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
8119 ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
8120 ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H. THE SIGNAL ADVAL H
8121 ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
8122 ;SIGNAL PRAS H WAS SET TO A ONE AND THEN A ZERO. THE MEMORY SIMULATORS
8123 ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
8124 ;BITS VIA THE SIGNALS CTS H AND CTS L.
8125
8126 022700 010137 002254 30$: MOV R1,S4LOAD ;SETUP THE EXPECTED ADDRESS TO BE READ
8127 022704 004737 010612 JSR PC,READS4 ;READ AND CHECK CONTROL REGISTER 4
8128 022710 001405 BEQ 31$ ;IF DATA = TE DIAG ADDRESS REG - CONT
8129 022712 ERRDF 3,TEMSAD,S04ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
8130 022712 104455 TRAP C$ERDF
8131 022714 000003 .WORD 3
8132 022716 002532 .WORD TEMSAD
8133 022720 005404 .WORD S04ERR
8134 022722 CKLOOP
8135 022722 104406 TRAP C$CLP1
8136
8137 ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
8138 ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
8139 ;ZEROS FOR THESE TWO ADDRESSES. ADDRESS BITS 17 AND 16 WERE CLOCKED
8140 ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
8141 ;ADVAL H. THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
8142 ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE AND THEN TO
8143 ;THE LOW STATE. THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
8144 ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
8145 ;MEMORY SIMULATOR MODULE.
8146
8147 022724 052737 000014 002250 31$: BIS #MSEL0!MSEL1,S2MASK ;IGNORE TRI-STATE BIT WHEN CTS H SET
8148 022732 005037 002244 CLR S2LOAD ;EXPECT MSAD 17:16 TO BE ZERO
8149 022736 013737 002244 002246 MOV S2LOAD,S2GOOD ;COPY DATA LOADED TO EXPECTED
8150 022744 052737 000140 002246 BIS #ESRH!WRENH,S2GOOD ;EXPECT MAP PROTECT BITS TO BE ONES
8151 022752 004737 010560 JSR PC,READS2 ;READ AND CHECK CONTROL REGISTER 2
8152 022756 001405 BEQ 32$ ;IF DATA OK THEN CONTINUE
8153 022760 ERRDF 2,TEMSA1,S02ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
8154 022760 104455 TRAP C$ERDF
8155 022762 000002 .WORD 2
8156 022764 002406 .WORD TEMSA1
8157 022766 005364 .WORD S02ERR
8158 022770 CKLOOP
8159 022770 104406 TRAP C$CLP1
8160
8161 ;SET THE SIGNAL CTS H TO THE LOW STATE BY CLEARING THE BIT IN CONTROL
8162 ;REGISTER 0. THIS WILL DISABLE THE SYSTEM BUS SIGNALS TO AND FROM
8163 ;THE MEMORY SIMULATOR MODULE. THE MODULE WILL BE SET BACK TO 16 BIT DATA
8164 ;MODE BY CLEARING THE SIGNAL 8 BIT H IN CONTROL REGISTER 0. THIS IS DONE
8165 ;TO CHECK THAT ONLY THE LOW BYTE OF THE DATA WAS WRITTEN INTO THE MEMORY
8166 ;SIMULATOR RAM IN 8 BIT MODE.

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8167
8168 022772 112737 000004 002234 32$:  MOVB    #MPH,SLOAD          ;CLEAR CTS H AND LEAVE MP H SET TO A 1
8169 023000 004737 010504                JSR     PC,LDRDSO          ;LOAD, READ AND CHECK CONTROL REG 0
8170 023004 001405                BEQ     33$                ;IF LOADED OK THEN CONTINUE
8171 023006                ERRDF   1,SOEROR          ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
8172 023006 104455                TRAP   C$ERDF
8173 023010 000001                .WORD  1
8174 023012 000000                .WORD  0
8175 023014 005304                .WORD  SOEROR
8176 023016                CKLOOP
8177 023016 104406                TRAP   C$CLP1
8178
8179                ;READ CONTROL REGISTER 4 TO CHECK THAT THE MEMORY SIMULATOR ADDRESS
8180                ;LOADED PREVIOUSLY IS STILL LOADED
8181
8182 023020 004737 010612 33$:  JSR     PC,READS4          ;READ AND CHECK CONTROL REGISTER 4
8183 023024 001405                BEQ     34$                ;IF ADDRESS 0 THEN CONTINUE
8184 023026                ERRDF   3,MSADRG,S4EROR  ;MSAD 15:0 REG ERROR
8185 023026 104455                TRAP   C$ERDF
8186 023030 000003                .WORD  3
8187 023032 002506                .WORD  MSADRG
8188 023034 005334                .WORD  S4EROR
8189 023036                CKLOOP
8190 023036 104406                TRAP   C$CLP1
8191
8192                ;READ CONTROL REGISTER 2 TO CHECK THAT THE DATA LOADED INTO IT PREVIOUSLY
8193                ;HAS NOT CHANGED. THE FOLLOWING SIGNALS SHOULD BE READ AS ZEROES:
8194                ;MSAD16 H, MSAD17 H, MSEL0 L, MSEL1 L AND MSBRK H. THE SIGNALS ESR H
8195                ;AND WREN H SHOULD BE READ AS ONES.
8196
8197 023040 012737 177400 002250 34$:  MOV     #177400,S2MASK     ;SETUP TO CHECK ALL OFF LOW BYTE
8198 023046 004737 010560                JSR     PC,READS2          ;READ AND CHECK CONTROL REGISTER 2
8199 023052 001405                BEQ     35$                ;IF NO CHANGE THEN CONTINUE
8200 023054                ERRDF   2,S2EROR          ;CONTROL REG 2 NOT EQUAL EXPECTED
8201 023054 104455                TRAP   C$ERDF
8202 023056 000002                .WORD  2
8203 023060 000000                .WORD  0
8204 023062 005320                .WORD  S2EROR
8205 023064                CKLOOP
8206 023064 104406                TRAP   C$CLP1
8207
8208                ;READ CONTENTS OF THE MEMORY SIMULATOR RAM ADDRESS TO CHECK THAT THE LOW BYTE OF
8209                ;DATA INITIALLY LOADED INTO IT WAS WRITTEN BACK INTO IT FROM THE TARGET
8210                ;EMULATOR MODULE DURING A WRITE OPERATION. IN THE FIRST PART OF THIS
8211                ;TEST THE DATA WAS READ FROM THE MEMORY SIMULATOR RAM INTO THE TARGET
8212                ;EMULATOR AND SAVED IN THE TARGET EMULATORS TDAL DIAGNOSTIC LATCHES.
8213                ;THE PROGRAM THEN CLEARED THE DATA PATTERN WRITTEN INTO THE ADDRESS
8214                ;OF THE MEMORY SIMULATOR RAM. THE PROGRAM THEN ENABLED THE TDAL DIAG-
8215                ;NOSTIC LATCHES TO THE TDAL BUS AND WROTE THE LOW BYTE OF DATA BACK INTO THE ADD-
8216                ;OF THE MEMORY SIMULATOR RAM. THE FOLLOWING CHECK WILL TEST THAT THIS
8217                ;HAPPENED CORRECTLY.
8218
8219 023066 005037 002260 35$:  CLR     S6LOAD            ;CLEAR THE HIGH BYTE OF EXPECTED WORD
8220 023072 111237 002260                MOVB   (R2),S6LOAD        ;GET INITIAL LOW BYTE OF MS RAM DATA
8221 023076 013737 002260 002262                MOV    S6LOAD,S6GOOD     ;COPY DATA FOR COMPARE IN SUBROUTINE
8222 023104 004737 010644                JSR    PC,READS6          ;READ AND CHECK MS RAM DATA
  
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8223 023110 001405      BEQ      36$      ;IF DATA OK THEN CONTINUE
8224 023112              ERRDF    4,MSGMSR,S6ALLR ;DATA ERROR IN MEMORY SIMULATOR RAM
8225 023112 104455      TRAP    C$ERDF
8226 023114 000004      .WORD   4
8227 023116 002743      .WORD  MSGMSR
8228 023120 005454      .WORD  S6ALLR
8229 023122              CKLOOP
8230 023122 104406      TRAP    C$CLP1
8231
8232              ;SET THE SIGNALS CTS H AND 8 BIT H TO ONES IN CONTROL REGISTER 0. CTS H
8233              ;ON A ONE WILL ENABLE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR
8234              ;RAM. 8 BIT H ON A ONE WILL SET THE MODULE UP IN 8 BIT DATA MODE.
8235
8236 023124 052737 000012 002234 36$:  BIS     #CTS H!BIT8H,S0LOAD ;SETUP BITS TO BE LOADED
8237 023132 004737 010504              JSR     PC,LDRDSO ;LOAD, READ AND CHECK CONTROL REG 0
8238 023136 001405              BEQ     37$      ;IF LOADED OK THEN CONTINUE
8239 023140              ERRDF    1,,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
8240 023140 104455      TRAP    C$ERDF
8241 023142 000001      .WORD   1
8242 023144 000000      .WORD   0
8243 023146 005304      .WORD  S0EROR
8244 023150              CKLOOP
8245 023150 104406      TRAP    C$CLP1
8246
8247              ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
8248              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8249
8250 023152 004737 012212 37$:  JSR     PC,SLCTTE ;SELECT TARGET EMULATOR MODULE
8251
8252              ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO A
8253              ;0. THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN ON A WRITE COMMAND
8254              ;TO CONTROL REGISTER 6. THE DIAGNOSTIC ADDRESS REGISTER WILL BE ENABLED
8255              ;TO THE ADDRESS BUS BY HDAL9 H BEING SET TO A ONE, WHICH IT IS. ON A READ
8256              ;COMMAND TO CONTROL REGISTER 6, THE DIAGNOSTIC ADDRESS REGISTER WILL BE READ.
8257
8258 023156 004537 012232  JSR     R5,SELER ;SELECT REGISTER SPECIFIED BY NEXT WORD
8259 023162 000000      .WORD  ADDRES ;SELECT DIAG ADDRESS REG AND ADDRESS BUS
8260
8261              ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
8262              ;FOLLOWING ADDRESSES: 000001, 020001, 040001, OR 060001.
8263
8264 023164 010137 002346  MOV     R1,T6LOAD ;GET THE TEST ADDRESS
8265 023170 005237 002346  INC     T6LOAD ;MAKE THE ADDRESS ODD
8266 023174 004737 011214  JSR     PC,LDRDT6 ;LOAD, READ AND CHECK DIAG ADDRESS REG
8267 023200 001405      BEQ     38$      ;IF LOADED OK THEN CONTINUE
8268 023202              ERRDF    12,ADDRRG,T06ERR ;DIAG ADDRESS REG NOT EQUAL EXPECTED
8269 023202 104455      TRAP    C$ERDF
8270 023204 000014      .WORD  12
8271 023206 004142      .WORD  ADDRRG
8272 023210 006730      .WORD  T06ERR
8273 023212              CKLOOP
8274 023212 104406      TRAP    C$CLP1
8275
8276              ;SLECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6. ON A READ COMMAND
8277              ;TO CONTROL REGISTER 6, THE EIDAL BUS WILL BE READ BACK TO THE LSI-11.
8278

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8279 023214 004537 012232      38$: JSR      R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
8280 023220 000006              .WORD    EIDAL              ;SELECT THE EIDAL BUS TO BE READ
8281
8282                               ;AT THIS POINT IN TIME THE EIDAL BUS SHOULD HAVE THE TDAL DIAGNOSTIC
8283                               ;LATCHES ENABLED TO IT BY THE SIGNALS DBHB L AND DBLB L BEING ASSERTED
8284                               ;LOW AND THE SIGNAL VDALO H BEING SET TO A ONE. THE TDAL LATCHES WERE
8285                               ;CLOCKED EARLIER IN THE TEST BY THE SIGNAL VDAL2 H. THESE LATCHES WERE
8286                               ;CLOCKED WITH THE DATA FROM THE MEMORY SIMULATOR RAM DURING A READ
8287                               ;OPERATION FROM THE MEMORY SIMULATOR RAM'S TEST ADDRESS.
8288
8289 023222 011237 002346      MOV      (R2),T6LOAD        ;GET 1ST DATA WRITTEN TO MS RAM
8290 023226 004737 011222      JSR      PC,READT6        ;READ AND CHECK EIDAL BUS
8291 023232 001405              BEQ      39$              ;IF DATA OK THEN CONTINUE
8292 023234                               ERRDF    12,MSTETD,T6ALLR   ;MS RAM DATA TO EIDAL BUS VIA TDAL BUS
8293 023234 104455              TRAP    C$ERRDF
8294 023236 000014              .WORD    12
8295 023240 004420              .WORD    MSTETD
8296 023242 006744              .WORD    T6ALLR
8297 023244                               CKLOOP
8298 023244 104406              TRAP    C$CLP1
8299
8300                               ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
8301                               ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
8302                               ;REGISTER 6.
8303
8304 023246 004537 012232      39$: JSR      R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
8305 023252 000003              .WORD    HDAL            ;SELECT THE HDAL REGISTER
8306 023254 012737 001144 002346  MOV      #HDAL9!HDAL6!HDAL5!HDAL2,T6LOAD ;SETUP BITS PREVIOUSLY LOADED
8307
8308                               ;AT THE PRESENT TIME, MEMORY SIMULATOR DATA WHICH WAS READ FROM THE TEST
8309                               ;ADDRESS EARLIER IN THIS TEST, IS NOW ENABLED TO THE SYSTEM DATA BUS VIA
8310                               ;THE TDAL DIAGNOSTIC LATCHES. THIS DATA WAS PRESENT ON THE EIDAL BUS IN
8311                               ;THE LAST DATA CHECK ABOVE. THE EIDAL BUS IS ENABLED TO SYSTEM DATA BUS
8312                               ;BY THE SIGNAL MSDO H BEING ASSERTED HIGH. THE PROGRAM WILL NOW WRITE THE
8313                               ;LOW BYTE OF THE SYSTEM BUS DATA INTO THE HIGH BYTE OF THE MEMORY SIMULATOR
8314                               ;RAM ADDRESSED. THIS IS DONE BY DOING A NORMAL T-11 TIMING CYCLE. WHEN
8315                               ;PRAS H IS SET HIGH, THE ADDRESS BUS, WHICH CONTAINS THE DIAGNOSTIC ADDRESS
8316                               ;REGISTER DATA, WILL BE CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS
8317                               ;BUS LATCHES. WHEN XF H IS SET HIGH, THE LOW BYTE OF DATA WILL BE
8318                               ;WRITTEN INTO THE HIGH BYTE OF THE MEMORY SIMULATOR RAM ADDRESSED. THE
8319                               ;WRITE SIGNALS FROM THE TARGET EMULATOR MODULE TO THE MEMORY SIMULATOR
8320                               ;MODULE ARE WT HB H AND WT LB H.
8321
8322 023262 004737 012276      JSR      PC,XRASH         ;SET XRAS H AND PRAS H TO HIGH STATE
8323 023266 004737 012402      JSR      PC,XCASH         ;SET XCAS H AND PCAS H TO HIGH STATE
8324 023272 004737 012506      JSR      PC,XPIH          ;SET XPI H AND PPI H TO HIGH STATE
8325 023276 004737 012434      JSR      PC,XCASL         ;SET XCAS H AND PCAS H TO LOW STATE
8326 023302 004737 012540      JSR      PC,XPIL          ;SET XPI H AND PPI H TO LOW STATE
8327 023306 004737 012330      JSR      PC,XRASL         ;SET XRAS H AND PRAS H TO LOW STATE
8328
8329                               ;READ THE VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A
8330                               ;ONE AS A RESULT OF THE ABOVE TIMING SEQUENCE.
8331
8332 023312 052737 000020 002342  BIS      #VDAL4,T4GOOD    ;EXPECT EDEOC H TO BE SET TO A ONE
8333 023320 004737 011176      JSR      PC,READT4        ;READ AND CHECK VDAL REGISTER
8334 023324 001405              BEQ      40$              ;IF OK THEN CONTINUE
  
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8335 023326 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
8336 023326 104455 TRAP C$ERDF
8337 023330 000013 .WORD 11
8338 023332 003706 .WORD VDALRG
8339 023334 006714 .WORD T4EROR
8340 023336 CKLOOP
8341 023336 104406 TRAP C$CLP1
8342
8343 ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
8344 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8345
8346 023340 004737 011246 40$: JSR PC,SLCTMS ;SELECT THE MEMORY SIMULATOR MODULE
8347
8348 ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
8349 ;TARGET EMULATOR MODULE PERFORMED A NORMAL T-11 TIMING CYCLE.
8350
8351 023344 004737 010520 JSR PC,READSL ;READ AND CHECK CONTROL REGISTER 0
8352 023350 001405 BEQ 41$ ;IF NO CHANGES THEN CONTINUE
8353 023352 ERRDF 1,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
8354 023352 104455 TRAP C$ERDF
8355 023354 000001 .WORD 1
8356 023356 000000 .WORD 0
8357 023360 005304 .WORD S0EROR
8358 023362 CKLOOP
8359 023362 104406 TRAP C$CLP1
8360
8361 ;READ AND CHECK MSAD BITS 15:0 IN CONTROLR REGISTER 4 TO SEE IF THE
8362 ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
8363 ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H. THE SIGNAL ADVAL H
8364 ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE SIGNAL PRAS H WAS
8365 ;SET TO A ONE FROM A ZERO. THE MEMORY SIMULATOR SYSTEM ADDRESS BUS
8366 ;LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0 BITS VIA THE SIGNALS
8367 ;CTS H AND CTS L.
8368
8369 023364 010137 002254 41$: MOV R1,S4LOAD ;GET THE EVEN TEST ADDRESS
8370 023370 005237 002254 INC S4LOAD ;MAKE THE ADDRESS ODD
8371 023374 004737 010612 JSR PC,READS4 ;READ AND CHECK MSAD BITS 15:0
8372 023400 001405 BEQ 42$ ;IF OK THEN CONTINUE
8373 023402 ERRDF 3,TEMSAD,S04ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
8374 023402 104455 TRAP C$ERDF
8375 023404 000003 .WORD 3
8376 023406 002532 .WORD TEMSAD
8377 023410 005404 .WORD S04ERR
8378 023412 CKLOOP
8379 023412 104406 TRAP C$CLP1
8380
8381 ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
8382 ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE. ADDRESS BITS
8383 ;17 AND 16 WERE CLOCKED INTO MEMORY SIMULATOR ADDRESS BUS LATCHES VIA
8384 ;THE SIGNAL ADVAL H. THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET
8385 ;EMULATOR MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE
8386 ;AND THEN TO THE LOW STATE. THE MEMORY SIMULATOR SYSTEM BUS LATCHES
8387 ;ARE ENABLED TO MSAD BITS 17:0 VIA THE SIGNALS CTS H AND CTS L ON THE
8388 ;MEMORY SIMULATOR MODULE.
8389
8390 023414 052737 000014 002250 42$: BIS #MSEL1!MSEL0,S2MASK ;IGNORE TRI-STATED BITS WHEN CTS H SET

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8391 023422 005037 002244 CLR S2LOAD ;EXPECT MSAD BITS 17 + 16 TO BE 0
8392 023426 013737 002244 002246 MOV S2LOAD,S2GOOD ;COPY DATA FOR DATA COMPARE
8393 023434 052737 000140 002246 BIS #ESRH!WRENH,S2GOOD ;EXPECT MAP PROTECT BITS TO BE ONES
8394 023442 004737 010560 JSR PC,READS2 ;READ AND CHECK CONTROL REGISTER 2
8395 023446 001405 BEQ 43$ ;IF DATA OK THEN CONTINUE
8396 023450 ERRDF 2,TEMSA1,S02ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
8397 023450 104455 TRAP C$ERDF
8398 023452 000002 .WORD 2
8399 023454 002406 .WORD TEMSA1
8400 023456 005364 .WORD S02ERR
8401 023460 CKLOOP
8402 023460 104406 TRAP C$CLP1
8403
8404 ;SET THE SIGNALS CTS H AND 8 BIT H TO THE LOW STATES BY CLEARING THESE
8405 ;BITS IN CONTROL REGISTER 0. CTS H ON A ZERO WILL DISABLE THE SYSTEM
8406 ;BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR MODULE. WHEN 8 BIT H IS
8407 ;SET TO A ZERO, THE MEMORY SIMULATOR MODULE WILL BE SETUP TO 16 BIT DATA
8408 ;MODE. THIS IS DONE TO CHECK THAT THE LOW BYTE OF DATA ON THE SYSTEM
8409 ;BUS WAS WRITTEN INTO THE HIGH BYTE OF THE MEMORY SIMULATOR RAM LOCATION
8410
8411 023462 112737 000004 002234 43$: MOVB #MPH,S0LOAD ;CLEAR CTS H AND 8 BIT H
8412 023470 004737 010504 JSR PC,LDRDS0 ;LOAD, READ AND CHECK CONTROL REG 0
8413 023474 001405 BEQ 44$ ;IF LOADED OK THEN CONTINUE
8414 023476 ERRDF 1,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
8415 023476 104455 TRAP C$ERDF
8416 023500 000001 .WORD 1
8417 023502 000000 .WORD 0
8418 023504 005304 .WORD S0EROR
8419 023506 CKLOOP
8420 023506 104406 TRAP C$CLP1
8421
8422 ;READ CONTROL REGISTER 4 TO CHECK THAT THE MEMORY SIMULATOR ADDRESS
8423 ;LOADED PREVIOUSLY HAS NOT CHANGED. THIS ADDRESS SHOULD BE EVEN.
8424
8425 023510 010137 002254 44$: MOV R1,S4LOAD ;GET THE ADDRESS BEING TESTED
8426 023514 004737 010612 JSR PC,READS4 ;PEAD AND CHECK MSAD BITS 15:0
8427 023520 001405 BEQ 45$ ;IF ADDRESS OK THEN CONTINUE
8428 023522 ERRDF 3,MSADRG,S4EROR ;MSAD 15:0 REGISTER ERROR
8429 023522 104455 TRAP C$EPDF
8430 023524 000003 .WORD 3
8431 023526 002506 .WORD M.DRG
8432 023530 005334 .WORD S4EROR
8433 023532 CKLOOP
8434 023532 104406 TRAP C$CLP1
8435
8436 ;READ CONTROL REGISTER 2 TO CHECK THAT THE DATA LOADED INTO IT BEFORE
8437 ;HAS NOT CHANGED. THE FOLLOWING SIGNALS SHOULD BE READ AS ZEROES:
8438 ;MSAD16 H, MSAD17 H, MSEL0 L, MSEL1 L AND MSBRK H. THE SIGNALS ESR H
8439 ;WREN H SHOULD BE READ AS ONES.
8440
8441 023534 012737 177400 002250 45$: MOV #177400,S2MASK ;SETUP TO CHECK ALL OF LOW BYTE
8442 023542 004737 010560 JSR PC,READS2 ;READ AND CHECK CONTROL REGISTER 2
8443 023546 001405 BEQ 46$ ;IF OK THEN CONTINUE
8444 023550 ERRDF 2,S2EROR ;CONTROL REGISTER 2 NOT EQUAL EXPECTED
8445 023550 104455 TRAP C$ERDF
8446 023552 000002 .WORD 2

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TEST 6: READ MS DATA TO TF - WRITE DATA TO MS VIA TE - 8 BIT MODE

SEQ 0166

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8447 023554 000000 .WORD 0
8448 023556 005320 .WORD S2EROR
8449 023560 CKLOOP
8450 023560 104406 TRAP C$CLP1
8451
8452 ;READ CONTENTS OF MEMORY SIMULATOR RAM ADDRESS TO CHECK THAT THE LOW
8453 ;BYTE OF DATA INITIALLY LOADED INTO IT WAS WRITTEN BACK INTO THE HIGH
8454 ;BYTE OF THE LOCATION FROM THE TARGET EMULATOR MODULE DURING A WRITE
8455 ;OPERATION. IN THE FIRST PART OF THE TEST, THE DATA WAS READ FROM THE
8456 ;MEMORY SIMULATOR RAM INTO THE TARGET EMULATOR DIAGNOSTIC TDAL LATCHES
8457 ;AND SAVED IN THESE LATCHES. THE PROGRAM THEN CLEARED THE MEMORY
8458 ;SIMULATOR RAM LOCATION AND WROTE THE LOW BYTE OF THE LOCATION WITH DATA
8459 ;FROM THE TARGET EMULATOR'S TDAL LATCHES VIA THE DATA BUS. THE LAST
8460 ;PORTION OF THIS TEST WILL CAUSE THE HIGH BYTE OF THE MEMORY SIMULATOR
8461 ;RAM TO BE WRITTEN WITH THE LOW BYTE OF DATA FROM THE TARGET EMULATOR'S
8462 ;TDAL LATCHES VIA THE DATA BUS.
8463
8464 023562 011237 002260 46$: MOV (R2),S6LOAD ;GET INITIAL DATA PATTERN
8465 023566 111237 002261 MOVB (R2),S6LOAD+1 ;COPY LOW BYTE TO HIGH BYTE
8466 023572 013737 002260 002262 MOV S6LOAD,S6GOOD ;COPY DATA FOR DATA COMPARE
8467 023600 004737 010644 JSR PC,READS6 ;READ AND CHECK MS RAM DATA
8468 023604 001404 BEQ 47$ ;IF DATA OK THEN HIGH BYTE WRITTEN OK
8469 023606 ERRDF 4,MSGMSR,S6ALLR ;DATA ERROR IN MEMORY SIMULATOR RAM
8470 023606 104455 TRAP C$ERDF
8471 023610 000004 .WORD 4
8472 023612 002743 .WORD MSGMSR
8473 023614 005454 .WORD S6ALLR
8474 023616 47$: ENDSEG
8475 023616 10000$:
8476 023616 104405 TRAP C$ESEG
8477
8478 023620 005722 TST (R2)+ ;UPDATE THE DATA TABLE POINTER
8479 023622 062701 020000 ADD #MSAD13,R1 ;UPDATE ADDRESS TO NEXT MS RAM BANK
8480 023626 100402 BMI 48$ ;IF DONE EACH BANK OF MEMORY - EXIT
8481 023630 000137 021162 JMP 1$ ;GO DO TWO PATTERNS WITH THIS ADDRESS
8482
8483 ;TO CHECK THAT ADDRESS 0 OF EACH 4K BANK OF MEMORY SIMULATOR RAM WAS
8484 ;SELECTED AND WRITTEN CORRECTLY, THE PROGRAM WILL READ THE FIRST ADDRESS
8485 ;OF EACH 4K BANK OF MEMORY SIMULATOR RAM. THE DATA WILL BE DIFFERENT
8486 ;THEN THAT WHICH WAS WRITTEN INTO IT INITIALLY. WHEN THE MEMORY SIMULATOR
8487 ;RAM WAS SETUP TO 8 BIT MODE AND DATA WAS WRITTEN INTO IT FROM THE TARGET
8488 ;EMULATOR MODULE, THE LOW BYTE OF THE INITIAL DATA PATTERN WILL BE WRITTEN
8489 ;INTO THE LOW BYTE OF THE ADDRESS WHEN THE ADDRESS IS EVEN AND THE LOW
8490 ;BYTE OF THE INITIAL DATA PATTERN WILL BE WRITTEN INTO THE HIGH BYTE OF
8491 ;THE ADDRESS WHEN THE ADDRESS IS ODD. THE ADDRESSES LOADED INITIALLY
8492 ;AND THE EXPECTED DATA PATTERNS TO BE IN THE ADDRESSES NOW ARE LISTED BELOW:
8493 ; ADDRESS 000000 WAS 052652 NOW SHOULD BE 125252
8494 ; ADDRESS 020000 WAS 146063 NOW SHOULD BE 031463
8495 ; ADDRESS 040000 WAS 000377 NOW SHOULD BE 177777
8496 ; ADDRESS 060000 WAS 125125 NOW SHOULD BE 052525
8497
8498 023634 005001 48$: CLR R1 ;SETUP STARTING ADDRESS TO BE 0
8499 023636 012702 023736 MOV #52$,R2 ;SETUP ADDRESS OF DATA TABLE
8500
8501 ;LOAD, READ AND CHECK CONTROL REGISTER 4 WITH THE ADDRESS OF THE LOCATION
8502 ;TO BE CHECKED. THE ADDRESSES TO BE LOADED ARE 0, 20000, 40000, AND 60000.

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8503
8504 023642 010137 002254      49$:  MOV      R1,S4LOAD      ;GET THE ADDRESS TO BE LOADED
8505 023646 004737 010604      JSR      PC,LDRDS4      ;LOAD, READ AND CHECK CONTROL REGISTER 4
8506 023652 001405              BEQ      50$            ;IF LOADED OK THEN CONTINUE
8507 023654 010455              ERRDF   3,MSADRG,S4EROR ;MSAD 15:0 REGISTER ERROR
8508 023654 104455              TRAP    C$ERDF
8509 023656 000003              .WORD   3
8510 023660 002506              .WORD   MSADRG
8511 023662 005334              .WORD   S4EROR
8512 023664
8513 023664 104406              CKLOOP
8514
8515
8516
8517
8518
8519
8520
8521
8522 023666 011237 002260      50$:  MOV      (R2),S6LOAD      ;GET THE DATA FROM THE TABLE
8523 023672 111237 002261      MOVB    (R2),S6LOAD+1    ;COPY LOW BYTE TO HIGH BYTE
8524 023676 013737 002260 002262      MOV     S6LOAD,S6GOOD    ;SETUP EXPECTED DATA
8525 023704 004737 010644      JSR     PC,READS6        ;READ AND CHECK MEMORY SIM RAM DATA
8526 023710 001405              BEQ     51$            ;IF DATA OK THEN CONTINUE
8527 023712              ERRDF   4,MSGMSR,S6ALLR ;DATA ERROR IN MEMORY SIMULATOR RAM
8528 023712 104455              TRAP    C$ERDF
8529 023714 000004              .WORD   4
8530 023716 002743              .WORD   MSGMSR
8531 023720 005454              .WORD   S6ALLR
8532 023722
8533 023722 104406              CKLOOP
8534
8535 023724 005722              51$:  TST     (R2)+          ;UPDATE POINTER TO DATA TABLE
8536 023726 062701 020000      ADD     #MSAD13,R1      ;UPDATE THE ADDRESS TO NEXT 4K MEMORY
8537 023732 100343              BPL    49$             ;IF NOT DONE CHECK THIS 4K MEMORY BANK
8538 023734 000404              BR     53$            ;EXIT THE TEST
8539
8540 023736 052652              52$:  .WORD   052652        ;ADDRESS 000000 DATA PATTERN
8541 023740 146063              .WORD   146063        ;ADDRESS 020000 DATA PATTERN
8542 023742 000377              .WORD   000377        ;ADDRESS 040000 DATA PATTERN
8543 023744 125125              .WORD   125125        ;ADDRESS 060000 DATA PATTERN
8544
8545 023746              53$:  ENDTST
8546 023746              L10042:
8547 023746 104401              TRAP    C$ETST
8548
8549
8550
8551

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8552 .SBTTL TEST 7: CHECK TE SIGNALS XSEL1 H, EDSELO H, + BTS BITS 3:0 TO ED
8553
8554 :++
8555 : THIS TEST WILL CHECK THAT TARGET EMULATOR SIGNALS XSEL1 H, EDSELO H,
8556 : ADDR17 H, ADDR16 H, BTS3 H, BTS2 H, BTS1 H AND BTS0 H CAN BE ENABLED
8557 : TO THE SYSTEM BUS AS SIGNALS CTL 11:8 H AND OBTS 3:0 H RESPECTIVELY,
8558 : AND THAT THESE SIGNALS CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM
8559 : BUS LATCHES FOR THESE BITS VIA THE TARGET EMULATOR'S SYSTEM BUS CLOCKING
8560 : SIGNAL 'ENCK4 H'. THE PROGRAM WILL CHECK THAT THESE BITS ARE CLOCKED
8561 : INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES BY READING THESE LATCHES
8562 : ON THE STATE ANALYZERS TRDI BUS BITS 39:32. THE TARGET EMULATOR SIGNALS
8563 : 'ADDR17 H' AND 'ADDR16 H' HAVE BEEN CHECKED IN PREVIOUS TEST, THEREFORE,
8564 : THESE SIGNALS WILL ONLY BE CHECKED FOR ZEROES IN THIS TEST. THE PROGRAM
8565 : WILL SET THE SIGNALS XSEL1 H, EDSELO H AND BTS BITS 3:0 H TO ONES AND
8566 : ZEROES BY MANIPULATING THE ASSOCIATED LOGIC. THE TEST WILL THEN CLOCK
8567 : THE CORRESPONDING SYSTEM BUS SIGNALS INTO THE STATE ANALYZER SYSTEM BUS
8568 : LATCHES AND CHECK THAT THE SYSTEM BUS LATCHES CONTAIN THE CORRECT DATA
8569 : PATTERN. THE PROGRAM WILL ALSO CHECK THAT THE TARGET EMULATOR SYSTEM
8570 : BUS CLOCKING SIGNAL 'ENCK4 H' CAN BE GENERATED IN DIFFERENT WAYS.
8571 :--
8572
8573 023750 BGNTST
8574 023750 T7::
8575 023750 004737 007436 JSR PC,INITMD ;INITIALIZE CDS-11 SYSTEM MODULES
8576 023754 BGNSEG
8577 023754 104404 TRAP C$BSEG
8578 023756 005037 002320 CLR E6MASK ;CLEAR REGISTER 6 MASK WORD FOR LOOPING
8579
8580 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
8581 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8582
8583 023762 004737 012212 JSR PC,SLCTTE ;SELECT TARGET EMULATOR MODULE
8584
8585 ;SET ADAL REGISTER BITS 14, 10, 9, 7, AND 4 TO A ONE AND PULSE THE
8586 ;SIGNAL 'BRKRES L' BY SETTING AND CLEARING ADAL REGISTER BIT 0.
8587 : ADAL14H = 1 ALLOWS RASP L TO PULSE CKAI H WHEN XRAS H PULSED
8588 : ADAL10H = 1 ENABLES TE SIGNALS TO CDS-11 SYSTEM BUS
8589 : ADAL9H = 1 WHEN ADAL10H = 1 ENABLES EDCK 5:0 SIGNALS TO BUS
8590 : ADAL7H = 1 ALLOWS 'REFR' FLIP-FLOP TO BE CLOCKED VIA XRAS H
8591 : ADAL4H = 1 SETS PAUSE MODE F/F TO RUN MODE WHEN CLOCKED BY XRAS H
8592
8593 023766 012737 043220 002334 MOV #ADAL14!ADAL10!ADAL9!ADAL7!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
8594 023774 004737 012764 JSR PC,BRKRES ;SET BITS 14, 10 + 9 AND TOGGLE ADALO H
8595
8596 ;SELECT THE HDAL REG BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL REG
8597 ;WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REG 6.
8598
8599 024000 004537 012232 JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
8600 024004 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
8601
8602 ;SET HDAL REGISTER BITS TO THE FOLLOWING BIT SETTINGS:
8603 : HDAL14H = 0 ;SETS ADDR17 H TO LOW STATE (0)
8604 : HDAL11H = 0 ;SETS ADDR16 H TO LOW STATE (0)
8605 : HDAL9H = 1 ;ENABLES PIAG ADDRESS REG TO SYSTEM ADDRESS BUS
8606 : HDAL6H = 0 ;SETS XSEL1 L TO HIGH STATE
8607 : HDAL5H = 1 ;SETS XSELO L TO LOW STATE

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8608      ; HDAL4H = 0          ;SET XR/WHB L TO HIGH STATE
8609      ; HDAL3H = 1          ;SET XR/WLB L TO LOW STATE
8610      ; HDAL2H = 1          ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
8611
8612 024006 012737 001054 002346  MOV #HDAL9!HDAL5!HDAL3!HDAL2,T6LOAD ;SET HDAL BITS 9,5,3 + 2 TO ONES
8613 024014 004737 011214          JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK HDAL REGISTER
8614 024020 001405          BEQ 1$ ;IF LOADED OK THEN CONTINUE
8615 024022          ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
8616 024022 104455          TRAP C$ERDF
8617 024024 000014          .WORD 12
8618 024026 003754          .WORD HDALRG
8619 024030 006730          .WORD T06ERR
8620 024032          CKLOOP
8621 024032 104406          TRAP C$CLP1
8622
8623      ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
8624      ;REGISTER 4. PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
8625      ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L'.
8626
8627 024034 005037 002340 1$: CLR T4LOAD ;SETUP TO CLEAR ALL OTHER R/W BITS
8628 024040 004737 012704          JSR PC,CLRPSM ;PULSE INVD L VIA VDAL2 H
8629
8630      ;SELECT MODE REG BY SETTING GDAL REG BITS 2:0 TO A 4. ON A WRITE OR READ
8631      ;COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL BE WRITTEN OR READ.
8632
8633 024044 004537 012232          JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
8634 024050 000004          .WORD MODE ;SELECT THE MODE REGISTER
8635
8636      ;LOAD, READ AND CHECK THE MODE REGISTER WITH BIT 11 SET TO A ONE AND
8637      ;ALL OTHER READ/WRITE BITS CLEARED. THIS WILL SET THE TARGET EMULATOR
8638      ;MODULE TO 8 BIT ADDRESSING MODE.
8639
8640 024052 012737 004000 002346  MOV #MR11,T6LOAD ;SETUP BIT TO SET MR11 H TO HIGH STATE
8641 024060 004737 011214          JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK MODE REGISTER
8642 024064 001405          BEQ 2$ ;IF LOADED OK THEN CONTINUE
8643 024066          ERRDF 12,MODREG,T06ERR ;MODE REGISTER NOT EQUAL EXPECTED
8644 024066 104455          TRAP C$ERDF
8645 024070 000014          .WORD 12
8646 024072 004000          .WORD MODREG
8647 024074 006730          .WORD T06ERR
8648 024076          CKLOOP
8649 024076 104406          TRAP C$CLP1
8650
8651      ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
8652      ;TO A 2. THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
8653      ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
8654      ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
8655      ;TER WILL BE ADDRESSED.
8656
8657 024100 004537 012232 2$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
8658 024104 000002          .WORD FDAL ;SELECT EOAI AND FDAL REGISTER
8659
8660      ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER. THE EOAI REGISTER WILL
8661      ;BE LOADED AND CHECKED FOR ZEROES. THE FDAL REGISTER WILL BE LOADED AND
8662      ;CHECKED FOR A DATA PATTERN OF ONE (FDALO H = 1).
8663

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TEST 7: CHECK TE SIGNALS XSEL1 H, EDSELO H, + BTS BITS 3:0 TO ED

SEQ 0170

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8664 024106 012737 000001 002346 MOV #FDALO,T6LOAD ;SETUP EOAI AND FDAL REG DATA PATTERN
8665 024114 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK EOAI + FDAL REG
8666 024120 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
8667 024122 ERRDF 12,EOAIFD,T06ERR ;EOAI OR FDAL REGISTER ERROR
8668 024122 104455 TRAP C$ERDF
8669 024124 000014 .WORD 12
8670 024126 004045 .WORD EOAIFD
8671 024130 006730 .WORD T06ERR
8672 024132 CKLOOP
8673 024132 104406 TRAP C$CLP1
8674
8675 ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO A 0.
8676 ;THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN ON A WRITE COMMAND TO
8677 ;CONTROL REGISTER 6. THE DIAGNOSTIC ADDRESS REGISTER WILL BE ENABLED TO
8678 ;THE SYSTEM ADDRESS BUS VIA THE SIGNAL HDAL9 H. ON A READ COMMAND TO
8679 ;CONTROL REGISTER 6, THE SYTEM ADDRESS BUS WILL BE READ.
8680
8681 024134 004537 012232 3$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
8682 024140 000000 .WORD ADDRES ;SELECT THE DIAGNOSTIC ADDRESS REGISTER
8683
8684 ;LOAD READ AND CHECK DIAGNOSTIC ADDRESS REG WITH A DATA PATTERN OF 0'S
8685
8686 024142 005037 002346 CLR T6LOAD ;SETUP DATA PATTERN OF ALL ZEORES
8687 024146 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK DIAG ADDRESS REG
8688 024152 001405 BEQ 4$ ;IF LOADED OK THEN CONTINUE
8689 024154 ERRDF 12,ADDRRG,T06ERR ;DIAG ADDRESS REG NOT EQUAL TO ZERO
8690 024154 104455 TRAP C$ERDF
8691 024156 000014 .WORD 12
8692 024160 004142 .WORD ADDRRG
8693 024162 006730 .WORD T06ERR
8694 024164 CKLOOP
8695 024164 104406 TRAP C$CLP1
8696
8697 ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE
8698 ;IN CONTROL REGISTER 4.
8699
8700 024166 012737 000200 002340 4$: MOV #VDAL7,T4LOAD ;SETUP BIT TO SET FETCT H TO HIGH STATE
8701 024174 004737 011162 JSR PC,LDRDT4 ;LOAD, READ AND CHECK VDAL REGISTER
8702 024200 001405 BEQ 5$ ;IF LOADED OK THEN CONTINUE
8703 024202 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
8704 024202 104455 TRAP C$ERDF
8705 024204 000013 .WORD 11
8706 024206 003706 .WORD VDALRG
8707 024210 006714 .WORD T4EROR
8708 024212 CKLOOP
8709 024212 104406 TRAP C$CLP1
8710
8711 ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
8712 ;REG WILL BE WRITTEN AND READ ON A WRITE AND READ COMMAND TO CONTROL REG 6
8713
8714 024214 004537 012232 5$: JSR R5,SELTERR ;SELECT REG SPECIFIED BY THE NEXT WORD
8715 024220 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
8716
8717 ;TOGGLE THE SIGNAL XRAS H AND XRAS L BY SETTING AND CLEARING HDAL REGISTER
8718 ;BIT 12. WHEN XRAS H IS SET HIGH FROM BEING ASSERTED LOW, THE FOLLOWING
8719 ;FLIP-FLOPS WILL BE SET AS LISTED.

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8720 : PAUSE F/F = 1 THUS SETTING PAUSE L TO LOW STATE
8721 : ENCLK F/F = 1 THUS SETTING ENCLK H TO HIGH STATE
8722 : EDFET F/F = 1 THUS SETTING EDFET H TO HIGH STATE
8723 : BTFET F/F = 1 THUS SETTING BTFET L TO LOW STATE
8724 : EDSELO F/F = 0 THUS SETTING EDSELO H TO HIGH STATE
8725 : REFR F/F = 1 THUS SETTING REFR H TO HIGH STATE
8726 : ENEDC F/F = 1 THUS SETTING ENEDC H TO HIGH STATE
8727 : WHEN XRAS L IS RETURNED TO THE HIGH STATE AFTER HAVING BEEN ASSERTED
8728 : LOW, THE SIGNAL REFP L WILL BE ASSERTED LOW AS A RESULT OF THE REFR
8729 : FLIP-FLOP BEING SET TO A ONE. WHEN THE SIGNAL REFP L IS SET LOW, THE
8730 : SIGNAL EDCK4 H WILL BE SET TO THE HIGH STATE THUS CLOCKING THE SIGNALS
8731 : XSEL1 H, EDSELO H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0 INTO THE STATE
8732 : ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).
8733
8734 024222 012737 001054 002346 MOV #HDAL9!HDAL5!HDAL3!HDAL2,T6LOAD ;BITS PREVIOUSLY LOADED
8735 024230 004737 012264 JSR PC,XRAS ;GO PULSE XRAS H AND XRAS L VIA HDAL12
8736
8737 :READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL OBTS1 H IS SET TO A ONE
8738 :AS A RESULT OF THE BTFET FLIP-FLOP BEING SET TO A ONE AND THE SIGNAL
8739 :INTER L BEING ASSERTED HIGH. THE SIGNAL EDEOC H SHOULD ALSO BE READ AS
8740 :A ONE IN THE VDAL REGISTER AS A RESULT OF THE FOLLOWING SIGNALS BEING
8741 :ASSERTED HIGH: CYCLE L, ENEDC H, PSM L, AND SOP L.
8742
8743 024234 052737 000060 002342 BIS #VDAL5!VDAL4,T4GOOD ;EXPECT OBTS1 H AND EDEOC H TO BE ONES
8744 024242 004737 011176 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
8745 024246 001405 BEQ 6$ ;IF OK THEN CONTINUE
8746 024250 ERRDF 11,VDALRG,T4EROR ;BTS1 H OR EDEOC H PROBABLY NOT SET TO A ONE
8747 024250 104455 TRAP C$ERDF
8748 024252 000013 .WORD 11
8749 024254 003706 .WORD VDALRG
8750 024256 006714 .WORD T4EROR
8751 024260 CKLOOP
8752 024260 104406 TRAP C$CLP1
8753
8754 :READ CONTROL REGISTER 0 AND CHECK THAT NO CHANGES OCCURED AS A RESULT
8755 :OF PULSING THE SIGNALS XRAS H AND XRAS L.
8756
8757 024262 004737 011112 6$: JSR PC,READT0 ;READ AND CHECK THE GDAL REGISTER
8758 024266 001405 BEQ 7$ ;IF NO CHANGE THEN CONTINUE
8759 024270 ERRDF 9,GDALRG,TOEROR ;GDAL REG CHANGED AFTER PULSING XRAS
8760 024270 104455 TRAP C$ERDF
8761 024272 000011 .WORD 9
8762 024274 003636 .WORD GDALRG
8763 024276 006664 .WORD TOEROR
8764 024300 CKLOOP
8765 024300 104406 TRAP C$CLP1
8766
8767 :SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
8768 :REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8769
8770 024302 004737 012142 7$: JSR PC,SLCTED ;SELECT THE STATE ANALYZER MODULE
8771
8772 :SET THE SIGNAL TRSL2 L TO THE LOW STATE BY SETTING CDAL REGISTER BIT
8773 :3 TO A ONE AND CDAL REGISTER BIT 2 TO A ZERO. THE SIGNAL TRSL2 L WILL
8774 :ENABLE THE STATE ANALYZER'S SYSTEM BUS LATCHES ONTO TRDI BUS BITS 59:0.
8775

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TEST 7: CHECK TE SIGNALS XSEL1 H, EDSELO H, + BTS BITS 3:0 TO ED

SEQ 0172

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8776 024306 112737 000010 002272      MOVB    #CDAL3,ELOAD      ;SETUP BITS TO SET TRSL2 L TO LOW STATE
8777 024314 004737 010676              JSR     PC,LDRDEO        ;LOAD, READ AND CHECK CDAL REGISTER
8778 024320 001405                      BEQ     8$               ;IF LOADED OK THEN CONTINUE
8779 024322                      ERRDF   5,CDALRG,E0EROR   ;CDAL REGISTER NOT EQUAL EXPECTED
8780 024322 104455                      TRAP   C$ERDF
8781 024324 000005                      .WORD  5
8782 024326 003006                      .WORD  CDALRG
8783 024330 006144                      .WORD  E0EROR
8784 024332                      CKLOOP
8785 024332 104406                      TRAP   C$CLP1
8786
8787                      ;ASSERT THE SIGNAL PTER3 L IN THE POINTER REGISTER BY LOADING THE
8788                      ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.
8789
8790 024334 004537 012162      8$:   JSR     R5,LDPDAL        ;LOAD AND CHECK PDAL REG WITH NEXT WORD
8791 024340 000003              .WORD  PTER3           ;SETUP TO READ TRDI BUS BITS 47:32
8792
8793                      ;AS A REUSLT OF THE TARGET EMULATOR'S REFR FLIP-FLOP BEING SET AND A
8794                      ;PULSE ON THE TARGET EMULATOR SIGNALS XRAS H AND XRAS L, THE TARGET
8795                      ;EMULATOR SIGNAL EDCK4 H WILL GO FROM A LOW TO A HIGH STATE THUS
8796                      ;CLOCKING THE TARGET EMULATOR SIGNALS XSEL1 H, EDSELO H, ADDR17 H,
8797                      ;ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZER'S SYSTEM BUS
8798                      ;LATCHES FOR THESE BITS. CHECK TRDI BITS 38, 35 AND 33 TO BE SET AS
8799                      ;A RESULT OF TARGET EMULATOR SIGNALS EDSELO H, BTS3 H, AND BTS1 H BEING
8800                      ;ASSERTED TO THE HIGH STATE.
8801
8802 024342 012737 177400 002320      MOV     #177400,E6MASK   ;SETUP TO IGNORE TRDI BITS 47:40
8803 024350 012737 000112 002316      MOV     #BIT6!BIT3!BIT1,E6LOAD ;EXPECT EDSELO, OBTS3 AND BTS1 TO BE SET
8804 024356 004737 011052              JSR     PC,READE6        ;READ AND CHECK TRDI BITS 39:32
8805 024362 001405                      BEQ     9$               ;IF OK THEN CONTINUE
8806 024364                      ERRDF   8,TEEDA1,E026ER  ;TE TO SA XSEL1,EDSELO,ADDR 17:16 + BTS 3:0 ERRO
8807 024364 104455                      TRAP   C$ERDF
8808 024366 000010                      .WORD  8
8809 024370 003240                      .WORD  TEEDA1
8810 024372 006210                      .WORD  E026ER
8811 024374                      CKLOOP
8812 024374 104406                      TRAP   C$CLP1
8813
8814                      ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
8815                      ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8816
8817 024376 004737 012212      9$:   JSR     PC,SLCTTE        ;SELECT THE TARGET EMULATOR MODULE
8818
8819                      ;SET THE SIGNAL XSELO L TO THE HIGH STATE BY CLEARING HDAL REGISTER
8820                      ;BIT 5. THE HDAL REGISTER WILL BE LOADED WITH THE FOLLOWING BITS:
8821                      ; HDAL14H = 0          ;SETS ADDR17 H TO LOW STATE (0)
8822                      ; HDAL11H = 0          ;SETS ADDR16 H TO LOW STATE (0)
8823                      ; HDAL9H = 1           ;ENABLES DIAG ADDRESS REG TO SYSTEM ADDRESS BUS
8824                      ; HDAL6H = 0          ;SETS XSEL1 L TO HIGH STATE
8825                      ; HDAL5H = 0          ;SETS XSELO L TO HIGH STATE
8826                      ; HDAL4H = 0          ;SET XR/WHB L TO HIGH STATE
8827                      ; HDAL3H =           ;SET XR/WLB L TO LOW STATE
8828                      ; HDAL2H = 1          ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
8829
8830 024402 012737 001014 002346      MOV     #HDAL9!HDAL3!HDAL2,T6LOAD ;SETUP TO SET XSELO L TO LOW STATE
8831 024410 004737 011214              JSR     PC,LDRDT6        ;LOAD, READ AND CHECK HDAL REGISTER

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8832	024414	001405			BEQ	10\$;IF LOADED OR THEN CONTINUE
8833	024416				ERRDF	12,HDALRG,T06ERR		;HDAL REGISTER NOT EQUAL EXPECTED
8834	024416	104455			TRAP	C\$ERDF		
8835	024420	000014			.WORD	12		
8836	024422	003754			.WORD	HDALRG		
8837	024424	006730			.WORD	T06ERR		
8838	024426				CKLOOP			
8839	024426	104406			TRAP	C\$CLP1		
8840								
8841								
8842								
8843								
8844								
8845								
8846								
8847								
8848								
8849								
8850								
8851								
8852								
8853								
8854								
8855								
8856								
8857	024430	004737	012264	10\$:	JSR	PC,XRAS		;GO PULSE XRAS H AND XRAS L VIA HDAL12
8858								
8859								
8860								
8861	024434	004737	011176		JSR	PC,READT4		;READ AND CHECK VDAL REGISTER
8862	024440	001405			BEQ	11\$;IF NO CHANGE THEN CONTINUE
8863	024442				ERRDF	11,VDALRG,T4EROR		;VDAL REGISTER NOT EQUAL EXPECTED
8864	024442	104455			TRAP	C\$ERDF		
8865	024444	000013			.WORD	11		
8866	024446	003706			.WORD	VDALRG		
8867	024450	006714			.WORD	T4EROR		
8868	024452				CKLOOP			
8869	024452	104406			TRAP	C\$CLP1		
8870								
8871								
8872								
8873								
8874	024454	004737	011112	11\$:	JSR	PC,READT0		;READ AND CHECK GDAL REGISTER
8875	024460	001405			BEQ	12\$;IF NO CHANGE THEN CONTINUE
8876	024462				ERRDF	9,GDALRG,TOEROR		;GDAL REGISTER NOT EQUAL EXPECTED
8877	024462	104455			TRAP	C\$ERDF		
8878	024464	000011			.WORD	9		
8879	024466	003636			.WORD	GDALRG		
8880	024470	006664			.WORD	TOEROR		
8881	024472				CKLOOP			
8882	024472	104406			TRAP	C\$CLP1		
8883								
8884								
8885								
8886								
8887	024474	004737	012142	12\$:	JSR	PC,SLCTED		;SELECT THE STATE ANALYZER MODULE

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;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
;WHEN XRAS H IS SET HIGH, THE PAUSE MODE FLIP-FLOP WILL BE SET TO RUN
;MODE THUS SETTING THE SIGNAL PAUSE L TO THE LOW STATE; THE EDFET FLIP-
;FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL EDFET H TO THE HIGH
;STATE; THE BTFET FLIP-FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL
;BTFET L TO THE LOW STATE; THE EDSELO FLIP-FLOP WILL BE SET TO A
;ZERO THUS SETTING THE SIGNAL EDSELO H TO THE LOW STATE; AND THE REFR
;FLIP-FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL REFR H TO THE
;HIGH STATE. WHEN XRAS L IS RETURNED TO THE HIGH STATE AFTER HAVING
;BEEN ASSERTED TO THE LOW STATE, THE SIGNAL REFP L WILL BE ASSERTED
;LOW AS A RESULT OF THE REFR FLIP-FLOP BEING SET TO A ONE. WHEN THE
;SIGNAL REFP L IS SET LOW AFTER HAVING BEEN ASSERTED HIGH, THE SIGNAL
;EDCK4 H WILL BE SET HIGH THUS CLOCKING TARGET EMULATOR SIGNALS XSEL1 H,
;EDSELO H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZER
;SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).
  
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8888
8889
8890
8891
8892
8893
8894 024500 004737 010712
8895 024504 001405
8896 024506
8897 024506 104455
8898 024510 000005
8899 024512 003006
8900 024514 006144
8901 024516
8902 024516 104406
8903
8904
8905
8906
8907
8908
8909
8910
8911
8912
8913
8914
8915 024520 012737 000012 002316 13$:
8916 024526 004737 011052
8917 024532 001405
8918 024534
8919 024534 104455
8920 024536 000010
8921 024540 003240
8922 024542 006210
8923 024544
8924 024544 104406
8925
8926
8927
8928
8929 024546 004737 012212 14$:
8930
8931
8932
8933 024552 004737 011112
8934 024556 001405
8935 024560
8936 024560 104455
8937 024562 000011
8938 024564 003636
8939 024566 006664
8940 024570
8941 024570 104406
8942
8943

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:ON THE PREVIOUS SELECTION OF THE STATE ANALYZER MODULE, CDAL3 H WAS
:SET TO A ONE IN CONTROL REGISTER 0 TO SET THE SIGNAL TRSL2 L TO THE
:LOW STATE. WHEN TRSL2 L IS ASSERTED LOW, THE SYSTEM BUS LATCHES
:ARE ENABLED TO TRDI BUS BITS 59:0. READ AND CHECK CONTROL REGISTER 0.

JSR PC,READE0 ;READ AND CHECK CDAL REGISTER
BEQ 13$ ;IF OK THEN CONTINUE
ERRDF 5,CDALRG,E0EROR ;CDAL REGISTER NOT EQUAL EXPECTED
TRAP C$ERDF
.WORD 5
.WORD CDALRG
.WORD E0EROR
CKLOOP
TRAP C$CLP1

:THE PDAL REGISTER WAS LOADED PREVIOUSLY WITH BITS TO SET THE SIGNAL
:PTER3 L TO THE LOW STATE IN THE POINTER REGISTER. AS A RESULT OF
:THE TARGET EMULATOR SIGNALS REFR FLIP-FLOP BEING SET TO A ONE AND A
:PULSE BEING ISSUED ON THE TARGET EMULATOR SIGNALS XRAS H AND XRAS L,
:THE TARGET EMULATOR SIGNAL EDCK4 H WILL GO FROM A LOW TO A HIGH
:STATE VIA THE REFP L, THUS CLOCKING THE TARGET EMULATOR SIGNALS XSEL1 H
:EDSELO H, ADDR17 H, ADDR16 H, AND OBTS BITS 3:0 INTO THE STATE ANALYZER
:TRDI SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32). CHECK TRDI BITS
:35 AND 33 TO BE ONES AS A RESULT OF THE TARGET EMULATOR SIGNALS OBTS3 H
:AND OBTS1 H BEING ASSERTED HIGH.

MOV #BIT3:BIT1,E6LOAD ;EXPECT OBTS1 H AND OBTS3 H TO BE ONES
JSR PC,READE6 ;READ AND CHECK TRDI BITS 39:32
BEQ 14$ ;IF OK THEN CONTINUE
ERRDF 8,TEEDA1,E026ER ;TE TO SA XSEL1,EDSELO,ADDR 17:16 + BTS 3:0 ERRO
TRAP C$ERDF
.WORD 8
.WORD TEEDA1
.WORD E026ER
CKLOOP
TRAP C$CLP1

:SELECT TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
:REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.

JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE
;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES HAVE OCCURED.

JSR PC,READT0 ;READ AND CHECK GDAL REGISTER
BEQ 15$ ;IF NO CHANGES THEN CONTINUE
ERRDF 9,GDALRG,TOEROR ;GDAL REGISTER NOT EQUAL EXPECTED
TRAP C$ERDF
.WORD 9
.WORD GDALRG
.WORD TOEROR
CKLOOP
TRAP C$CLP1

:SET THE SIGNAL FETCT H TO THE LOW STATE AND PULSE THE SIGNAL INVD L

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8944 ;BY SETTING AND CLEARING VDAL2 H. A PULSE ON INVD L WILL CLEAR/SET
8945 ;ALL FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY THE
8946 ;SIGNAL BRKRES L. FOR THIS PARTICULAR TEST, A PULSE ON INVD L WILL
8947 ;CLEAR THE BTJET AND EDSELO FLIP-FLOPS.
8948
8949 024572 005037 002340 15$: CLR T4LOAD ;SETUP TO CLEAR FETCT H
8950 024576 004737 012704 JSR PC,CLRPSM ;SET FETCT H LOW AND PULSE INVD L
8951
8952 ;SET THE SIGNAL XSELO L TO THE LOW STATE BY SETTING HDAL REGISTER BIT
8953 ;5 TO A ONE. THE HDAL REGISTER WILL BE LOADED WITH THE FOLLOWING BITS:
8954 ; HDAL14H = 0 ;SETS ADDR17 H TO LOW STATE (0)
8955 ; HDAL11H = 0 ;SETS ADDR16 H TO LOW STATE (0)
8956 ; HDAL9H = 1 ;ENABLES DIAG ADDRESS REG TO SYSTEM ADDRESS BUS
8957 ; HDAL6H = 0 ;SETS XSEL1 L TO HIGH STATE
8958 ; HDAL5H = 1 ;SETS XSELO L TO LOW STATE
8959 ; HDAL4H = 0 ;SET XR/WHB L TO HIGH STATE
8960 ; HDAL3H = 1 ;SET XR/WLB L TO LOW STATE
8961 ; HDAL2H = 1 ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
8962
8963 024602 012737 001054 002346 MOV #HDAL9!HDAL5!HDAL3!HDAL2,T6LOAD ;SETUP BITS TO BE LOADED
8964 024610 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK HDAL REGISTER
8965 024614 001405 BEQ 16$ ;IF LOADED OK THEN CONTINUE
8966 024616 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
8967 024616 104455 TRAP C$ERDF
8968 024620 000014 .WORD 12
8969 024622 003754 .WORD HDALRG
8970 024624 006730 .WORD T06ERR
8971 024626 CKLOOP
8972 024626 104406 TRAP C$CLP1
8973
8974 ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL REGISTER BIT 13.
8975 ;A PULSE ON XCAS H WILL CAUSE THE ENCLK FLIP-FLOP AND THE ENEDC FLIP-FLOP
8976 ;TO BE SET TO GNES. THE EDSELO FLIP-FLOP WILL BE CLOCKED TO A ZERO THUS
8977 ;SETTING THE SIGNAL EDSELO H TO THE HIGH STATE
8978
8979 024630 004737 012370 16$: JSR PC,XCAS ;GO PULSE XCAS H AND XCAS L VIA HDAL13 H
8980
8981 ;READ VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A ONE
8982 ;AS A RESULT OF CYCLE L, PSM L, ENEDC H AND SOP L BEING ASSERTED HIGH.
8983
8984 024634 052737 000020 002342 BIS #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE SET TO A ONE
8985 024642 004737 011176 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
8986 024646 001405 BEQ 17$ ;IF OK THEN CONTINUE
8987 024650 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
8988 024650 104455 TRAP C$ERDF
8989 024652 000013 .WORD 11
8990 024654 003706 .WORD VDALRG
8991 024656 006714 .WORD T4EROR
8992 024660 CKLOOP
8993 024660 104406 TRAP C$CLP1
8994
8995 ;TOGGLE THE SIGNAL XPI L BY SETTING AND CLEARING HDAL REGISTER BIT 15.
8996 ;WHEN XPI L IS TOGGLED, A PULSE WILL OCCUR ON THE SIGNAL EDCK4 H. A
8997 ;PULSE ON EDCK4 H WILL CLOCK THE TARGET EMULATOR SIGNALS XSEL1 H,
8998 ;EDSELO H, ADDR17 H, ADDR16 H, AND OBTS BITS 3:0 INTO THE STATE ANALYZERS
8999 ;SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).

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9000
9001 024662 004737 012474      17$: JSR      PC,XPI                ;GO PULSE XPI L VIA HDAL15 H
9002
9003                               ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9004                               ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9005
9006 024666 004737 012142      JSR      PC,SLCTED              ;SELECT THE STATE ANALYZER MODULE
9007
9008                               ;FROM PREVIOUS SELECTIONS OF THE STATE ANALYZER MODULE, CDAL3 H WAS
9009                               ;SET TO A ONE IN CONTROL REGISTER 0 AND BITS WERE LOADED INTO CONTROL
9010                               ;REGISTER 2'S PDAL REGISTER TO SET THE SIGNAL PTER3 L IN THE POINTER
9011                               ;REGISTER. WHEN CDAL3 H IS SET TO A ONE AND CDAL2 H IS SET TO A ZERO,
9012                               ;THE SIGNAL TRSL2 L IS SET TO THE LOW STATE. THE SIGNAL TRSL2 L WILL
9013                               ;ENABLE THE STATE ANALYZER SYSTEM BUS LATCHES ONTO TRDI BUS BITS 59:0.
9014                               ;WHEN PTER3 L IS ASSERTED LOW IN THE POINTER REGISTER AND A READ COMMAND
9015                               ;IS ISSUED TO CONTROL REGISTER 6, TRDI BUS BITS 47:32 WILL BE READ. AS
9016                               ;A RESULT OF PULSING THE TARGET EMULATOR SIGNAL XPI L, A PULSE SHOULD
9017                               ;HAVE OCCURED ON THE TARGET EMULATOR SIGNAL EDCK4 H. A PULSE ON THE
9018                               ;SIGNAL EDCK4 H SHOULD HAVE CLOCKED THE TARGET EMULATOR SIGNALS XSEL1 H,
9019                               ;EDSELO H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZERS
9020                               ;TRDI SYSTEM BUS LATCHES FOR BITS 39:32. AS A RESULT OF PULSING INVD L
9021                               ;ON THE TARGET EMULATOR MODULE, THE ONLY BIT THAT SHOULD BE ASSERTED
9022                               ;HIGH WHEN READ IS THE BIT FOR EDSELO H, TRDI BIT 38. INVD L SHOULD
9023                               ;HAVE CLEARED THE TARGET EMULATOR FLIP-FLOPS BTFET, EDSELO, AND REFR.
9024                               ;A PULSE ON XCAS H SHOULD HAVE CAUSED THE EDSELO FLIP-FLOP TO BE CLOCKED
9025                               ;TO A ZERO THUS SETTING THE SIGNAL EDSELO H TO THE HIGH STATE. THE
9026                               ;SIGNAL XSELO L WAS ASSERTED LOW IN THE LAST SELECTION OF THE TARGET
9027                               ;EMULATOR MODULE. THE PROGRAM CAN NOT TEST THAT THE SIGNAL INVD L CLEARED
9028                               ;THE EDSELO FLIP-FLOP BECAUSE THE ENCLK FLIP-FLOP IS ALSO CLEARED BY
9029                               ;THE SIGNAL INVD L.
9030
9031 024672 012737 000100 002316  MOV      #BIT6,E6LOAD          ;EXPECT EDSELO H TO BE A 1 ON TRDI38 H
9032 024700 004737 011052          JSR      PC,READE6            ;READ TRDI BUS BITS 47:32
9033 024704 001405                  BEQ      18$                  ;IF LOADED OK THEN CONTINUE
9034 024706                          ERRDF  8,TEFDA1,E026ER        ;TE TO SA XSEL1,EDSELO,ADDR 17:16 + BTS 3:0 ERRO
9035 024706 104455                  TRAP    C$ERRDF
9036 024710 000010                  .WORD   8
9037 024712 003240                  .WORD   TEEDA1
9038 024714 006210                  .WORD   E026ER
9039 024716                          CKLOOP
9040 024716 104406                  TRAP    C$CLP1
9041
9042                               ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
9043                               ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9044
9045 024720 004737 012212      18$: JSR      PC,SLCTTE              ;SELECT TARGET EMULATOR MODULE
9046
9047                               ;SET THE SIGNALS INTER L AND INTER H TO THE LOW AND HIGH STATE RESPECTIVELY
9048                               ;BY SETTING THE SIGNAL XSELO L TO THE HIGH STATE AND XSEL1 L TO THE LOW
9049                               ;STATE. TO DO THIS THE PROGRAM WILL LOAD HDAL REGISTER WITH THE FOLLOWING
9050                               ;BIT PATTERNS:
9051                               ; HDAL14H = 0                ;SETS ADDR17 H TO LOW STATE (0)
9052                               ; HDAL11H = 0                ;SETS ADDR16 H TO LOW STATE (0)
9053                               ; HDAL9H  = 1                ;ENABLES DIAG ADDRESS REG TO SYSTEM ADDRESS BUS
9054                               ; HDAL6H  = 1                ;SETS XSEL1 L TO LOW STATE
9055                               ; HDAL5H  = 0                ;SETS XSELO L TO HIGH STATE
  
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9056      ; HDAL4H = 0      ;SET XR/WHB L TO HIGH STATE
9057      ; HDAL3H = 1      ;SET XR/WLB L TO LOW STATE
9058      ; HDAL2H = 1      ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
9059
9060 024724 012737 001114 002346  MOV #HDAL9!HDAL6!HDAL3!HDAL2,T6LOAD ;SETUP HDAL BITS TO BE LOADED
9061 024732 004737 011214  JSR PC,LDRDT6 ;LOAD, READ AND CHECK HDAL REGISTER
9062 024736 001405  BEQ 19$ ;IF LOADED OK THEN CONTINUE
9063 024740  ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
9064 024740 104455  TRAP C$ERDF
9065 024742 000014  .WORD 12
9066 024744 003754  .WORD HDALRG
9067 024746 006730  .WORD T06ERR
9068 024750  CKLOOP
9069 024750 104406  TRAP C$CLP1
9070
9071      ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL REG-
9072      ;ISTER BIT 12. WHEN XRAS H IS SET TO THE HIGH STATE, THE PAUSE MODE
9073      ;FLIP-FLOP WILL BE SET TO RUN MODE THUS SETTING THE SIGNAL PAUSE L TO
9074      ;THE LOW STATE; THE EDFET FLIP-FLOP WILL BE SET TO A ZERO THUS SETTING
9075      ;THE SIGNAL EDFET H TO THE LOW STATE; THE BTRET FLIP-FLOP WILL BE SET TO
9076      ;A ZERO THUS SETTING THE SIGNAL BTRET L TO THE HIGH STATE; THE EDSELO
9077      ;FLIP-FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL EDSELO H TO THE
9078      ;LOW STATE WHEN XRAS H IS SET TO THE HIGH STATE, THE REFR FLIP-FLOP
9079      ;WILL BE SET TO A ZERO THUS SETTING THE SIGNAL REFR L TO THE HIGH STATE.
9080      ;A PULSE WILL OCCUR ON THE SIGNAL EDCK4 H WHEN XRAS H IS TOGGLED AS A
9081      ;RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED HIGH: INTER H, XPI L,
9082      ;AND REFP. WHEN THE SIGNAL EDCK4 H IS PULSED, THE SIGNALS XSEL1 H,
9083      ;EDSELO H, DR17 H, ADDR16 H, AND OBTS BITS 3:0 ARE CLOCKED INTO THE
9084      ;STATE AND THE CPU'S SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).
9085
9086 024752 004737 012264 19$: JSR P AS ;GO PULSE XRAS H AND XRAS L VIA HDAL12
9087
9088      ;CHECK THE SIGNAL OBTS1 H TO BE SET TO A ONE IN CONTROL REGISTER 4 AS A
9089      ;RESULT OF THE SIGNAL INTER L BEING ASSERTED LOW AND THE BTRET FLIP-
9090      ;FLOP BEING SET TO A ZERO. CHECK THAT THE SIGNAL EDEOC H IS ALSO SET TO
9091      ;A ONE AS A RESULT OF CYCLE L, ENEDC H, PSM L, AND SOP L BEING ASSERTED
9092      ;TO THE HIGH STATES.
9093
9094 024756 012737 000060 002342  MOV #VDAL5!VDAL4,T4GOOD ;EXPECT OBTS1 H AND EDEOC H TO BE ONES
9095 024764 004737 011176  JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
9096 024770 001405  BEQ 20$ ;IF NO CHANGES THEN CONTINUE
9097 024772  ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
9098 024772 104455  TRAP C$ERDF
9099 024774 000013  .WORD 11
9100 024776 003706  .WORD VDALRG
9101 025000 006714  .WORD T4EROR
9102 025002  CKLOOP
9103 025002 104406  TRAP C$CLP1
9104
9105      ;READ CONTROL REGISTER 0, GDAL REGISTER, AND CHECK THAT NO CHANGES
9106      ;OCCURED AS A RESULT OF PULSING THE SIGNALS XRAS H AND XRAS L.
9107
9108 025004 004737 011112 20$: JSR PC,READT0 ;READ AND CHECK GDAL REGISTER
9109 025010 001405  BEQ 21$ ;IF NO CHANGES THEN CONTINUE
9110 025012  ERRDF 9,GDALRG,TOEROR ;GDAL REGISTER NOT EQUAL EXPECTED
9111 025012 104455  TRAP C$ERDF

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9112 025014 000011 .WORD 9
9113 025016 003636 .WORD GDALRG
9114 025020 006664 .WORD TOEROR
9115 025022 CKLOOP
9116 025022 104406 TRAP C$CLP1
9117
9118 ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9119 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9120
9121 025024 004737 012142 21$: JSR PC,SLCTED ;SELECT STATE ANALYZER MODULE
9122
9123 ;IN PREVIOUS SELECTIONS OF THE STATE ANALYZER MODULE, CDAL3 H WAS SET
9124 ;TO A ONE AND CDAL2 H WAS SET TO A ZERO TO ASSERT THE SIGNAL TRSL2 L.
9125 ;WHEN TRSL2 L IS ASSERTED LOW, THE STATE ANALYZER'S SYSTEM BUS LATCHES
9126 ;ARE ENABLED TO THE STATE ANALYZER'S TRDI BUS BITS 59:0. BITS WERE ALSO
9127 ;LOADED INTO CONTROL REGISTER 2'S PDAL REGISTER TO ASSERT THE SIGNAL
9128 ;PTER3 L TO THE LOW STATE IN THE POINTER REGISTER. WHEN A READ COMMAND
9129 ;IS ISSUED TO CONTROL REGISTER 6 AND PTER3 L IS ASSERTED LOW, TRDI BUS
9130 ;BITS 47:32 WILL BE READ. AS A RESULT OF PULSING XRAS H ON THE TARGET
9131 ;EMULATOR MODULE WHEN THE SIGNAL INTER H WAS ASSERTED HIGH, A PULSE
9132 ;SHOULD HAVE OCCURED ON THE TARGET EMULAO TR SIGNAL EDCK4 H. A PULSE
9133 ;ON THE SIGNAL EDCK4 H WILL CLOCK THE TARGET EMULATOR SIGNALS XSEL1 H,
9134 ;EDSELO H, ADDR17 H, ADDR16 H, AND OBTS BITS 3:0 INTO THE STATE ANALYZERS
9135 ;SYSTEM BUS LATCHES FOR THESE BITS, TRDI BUS BITS 39:32. STATE ANALYZER
9136 ;TRDI BITS 39, 33 AND 32 SHOULD BE READ AS ONES AS A RESULT OF XSEL1 H
9137 ;BEING ASSERTED HIGH AND INTER L BEING ASSERTED LOW ON THE TARGET
9138 ;EMULATOR MODULE.
9139
9140 025030 012737 000203 002316 MOV #BIT7!BIT1.BIT0,E6LOAD ;EXPECT XSEL1 H,OBTS1 H + BTS0 H TO = 1
9141 025036 004737 011052 JSR PC,READE6 ;READ AND CHECK TRDI BUS BITS 39:32
9142 025042 001405 BEQ 22$ ;IF OK THEN CONTINUE
9143 025044 ERRDF 8,TEEDA1,E026ER ;TE TO SA XSEL1,EDSELO,ADDR 17:16 + BTS 3:0 ERRO
9144 025044 104455 TRAP C$ERDF
9145 025046 000010 .WORD 8
9146 025050 003240 .WORD TEEDA1
9147 025052 006210 .WORD E026ER
9148 025054 CKLOOP
9149 025054 104406 TRAP C$CLP1
9150
9151 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
9152 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9153
9154 025056 004737 012212 22$: JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE
9155
9156 ;SET THE SIGNALS INTER L AND INTER H TO THE HIGH AND LOW STATES RESPEC-
9157 ;TIVELY. SET THE SIGNAL DMG L TO THE LOW STATE BY SETTING XSEL1 L
9158 ;AND XSELO L TO THE LOW STATES VIA BITS IN THE HDAL REGISTER. THE HDAL
9159 ;REGISTER WILL BE LOADED WITH THE FOLLOWING BITS
9160 ; HDAL14H = 0 ;SETS ADDR17 H TO LOW STATE (0)
9161 ; HDAL11H = 0 ;SETS ADDR16 H TO LOW STATE (0)
9162 ; HDAL9H = 1 ;ENABLES DIAG ADDRESS REG TO SYSTEM ADDRESS BUS
9163 ; HDAL6H = 1 ;SETS XSEL1 L TO LOW STATE
9164 ; HDAL5H = 1 ;SETS XSELO L TO LOW STATE
9165 ; HDAL4H = 0 ;SET XR/WHB L TO HIGH STATE
9166 ; HDAL3H = 1 ;SET XR/WLB L TO LOW STATE
9167 ; HDAL2H = 1 ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
    
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9168
9169 025062 012737 01154 002346 MOV #HDAL9!HDAL6!HDAL5!HDAL3!HDAL2,T6LOAD ;SETUP HDAL REG BITS
9170 025070 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK HDAL REGISTER
9171 025074 001405 BEQ 23$ ;IF LOADED OK THEN CONTINUE
9172 025076 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
9173 025076 104455 TRAP C$ERDF
9174 025100 000014 .WORD 12
9175 025102 003754 .WORD HDALRG
9176 025104 006730 .WORD T06ERR
9177 025106 CKLOOP
9178 025106 104406 TRAP C$CLP1
9179
9180 ;SET ADAL REGISTER BIT 7 TO A ZERO TO HOLD THE REFR FLIP-FLOP IN THE
9181 ;ZERO STATE. WHEN THE REFR FLIP-FLOP IS HELP CLEARED, THE SIGNALS
9182 ;REFR L AND REFP L WILL BE HELD TO THE HIGH STATE.
9183
9184 025110 042737 000200 002334 23$: BIC #ADAL7,T2LOAD ;SETUP BIT TO HOLD REFR F/F CLEARED
9185 025116 004737 011136 JSR PC,LDRDT2 ;LOAD, READ AND CHECK ADAL REGISTER
9186 025122 001405 BEQ 24$ ;IF LOADED OK THEN CONTINUE
9187 025124 ERRDF 10,ADALRG,T2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
9188 025124 104455 TRAP C$ERDF
9189 025126 000012 .WORD 10
9190 025130 003662 .WORD ADALRG
9191 025132 006700 .WORD T2EROR
9192 025134 CKLOOP
9193 025134 104406 TRAP C$CLP1
9194
9195 ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL
9196 ;REGISTER BIT 12. WHEN THESE SIGNALS ARE TOGGLED, THE PAUSE MODE FLIP-
9197 ;FLOP WILL BE SET TO RUN MODE THUS SETTING THE SIGNAL PAUSE L TO THE
9198 ;LOW STATE; THE EDFET FLIP-FLOP WILL BE SET TO A ZERO THUS SETTING THE
9199 ;SIGNAL EDFET H TO THE LOW STATE; THE BTRET FLIP-FLOP WILL BE SET TO A
9200 ;ZERO THUS SETTING THE SIGNAL BTRET L TO THE HIGH STATE; AND THE EDSELO
9201 ;FLIP-FLOP WILL BE SET TO A ZERO THUS SETTING THE SIGNAL EDSELO H TO THE
9202 ;HIGH STATE.
9203
9204 025136 004737 012264 24$: JSR PC,XRAS ;GO PULSE XRAS H AND XRAS L VIA HDAL12
9205
9206 ;TOGGLE THE SIGNAL XPI L BY SETTING AND CLEARING HDAL REGISTER BIT 15.
9207 ;WHEN XPI L IS SET LOW AND THE SIGNAL INTER H IS ASSERTED LOW AND THE
9208 ;SIGNAL REFP L IS ASSERTED HIGH, THE SIGNAL EDCK4 H WILL GO FROM A LOW
9209 ;TO A HIGH STATE THUS CLOCKING THE SIGNALS XSEL1 H, EDSELO H, ADDR17 H,
9210 ;ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES
9211 ;FOR THESE BITS, TRDI 39:32. THE SIGNALS XSEL1 H, EDSELO H AND OBTS2 H
9212 ;SHOULD BE ASSERTED HIGH AT THIS POINT IN TIME. WHEN XPI L IS RETURNED
9213 ;TO THE HIGH STATE, THE SIGNAL EDCK4 H WILL BE SET LOW.
9214
9215 025142 004737 012474 JSR PC,XPI ;GO PULSE XPI L VIA HDAL REG BIT 15
9216
9217 ;CHECK OBTS1 H TO BE A ZERO IN CONTROL REGISTER 4 AS A RESULT OF THE
9218 ;SIGNAL INTER L BEING ASSERTED HIGH AND THE BTRET FLIP-FLOP BEING SET
9219 ;TO A ZERO. EXPECT EDEOC H TO BE READ AS A ONE AS A RESULT OF THE
9220 ;SIGNALS CYCLE L, ENEDC H, PSM L AND SOP L BEING ASSERTED HIGH.
9221
9222 025146 012737 000020 002342 MOV #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE SET TO A ONE
9223 025154 004737 011176 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER

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9224 025160 001405      BEQ      25$      ;IF NO CHANGES THEN CONTINUE
9225 025162              ERRDF    11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
9226 025162 104455      TRAP    C$ERDF
9227 025164 000013      .WORD   11
9228 025166 003706      .WORD   VDALRG
9229 025170 006714      .WORD   T4EROR
9230 025172              CKLOOP
9231 025172 104406      TRAP    C$CLP1
9232
9233              ;READ CONTROL REGISTER 0'S GDAL REGISTER AND CHECK THAT NO CHANGES
9234              ;OCCURED AS A RESULT OF PULSING XRAS AND XPI.
9235
9236 025174 004737 011112 25$: JSR      PC,READT0 ;READ AND CHECK GDAL REGISTER
9237 025200 001405      BEQ      26$      ;IF NO CHANGES THEN CONTINUE
9238 025202              ERRDF    9,GDALRG,TOEROR ;GDAL REGISTER NOT EQUAL EXPECTED
9239 025202 104455      TRAP    C$ERDF
9240 025204 000011      .WORD   9
9241 025206 003636      .WORD   GDALRG
9242 025210 006664      .WORD   TOEROR
9243 025212              CKLOOP
9244 025212 104406      TRAP    C$CLP1
9245
9246              ;SELECT STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9247              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9248
9249 025214 004737 012142 26$: JSR      PC,SLCTED ;SELECT STATE ANALYZER MODULE
9250
9251              ;IN PREVIOUS SELECTIONS OF THE STATE ANALYZER, MODULE, CDAL3 H WAS SET TO
9252              ;A ONE AND CDAL2 H WAS SET TO A ZERO. THIS WAS DONE TO ASSERT THE
9253              ;SIGNAL TRSL2 L. WHEN TRSL2 L IS ASSERTED LOW, THE STATE ANALYZER'S
9254              ;SYSTEM BUS LATCHES ARE ENABLED TO THE STATE ANALYZERS TRDI BUS BITS 59:0.
9255              ;BITS WERE ALSO LOADED INTO CONTROL REGISTER 2'S PDAL REGISTER TO ASSERT
9256              ;THE SIGNAL PTER3 L IN THE POINTER REGISTER. WHEN A READ COMMAND IS
9257              ;ISSUED TO CONTROL REGISTER 6 AND PTER3 L IS ASSERTED LOW, TRDI BUS BITS
9258              ;47:32 ARE READ. AS A RESULT OF PULSING XPI L ON THE TARGET EMULATOR
9259              ;MODULE, A PULSE SHOULD HAVE OCCURED ON THE SIGNAL EDCK4 H. A PULSE
9260              ;ON THE SIGNAL EDCK4 H WILL CLOCK THE TARGET EMULATOR SIGNALS XSEL1 H,
9261              ;EDSELO H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZERS
9262              ;SYSTEM BUS LATCHES FOR THESE BITS, TRDI BUS BITS 39:32. WHEN THESE
9263              ;BITS ARE READ, TRDI BITS 39, 38 AND 34 SHOULD BE SET TO ONES AS A
9264              ;RESULT OF XSEL1 H, EDSELO H AND OBTS2 H BEING ASSERTED HIGH ON THE
9265              ;TARGET EMULATOR MODULE. OBTS2 H IS ASSERTED HIGH AS A RESULT OF
9266              ;TARGET EMULATOR SIGNALS DMG L BEING LOW AND ASPI L BEING HIGH.
9267
9268 025220 012737 000304 002316 MOV     #BIT7!BIT6!BIT2,E6LOAD ;EXPECT XSEL1 H, EDSELO H AND OBTS2 H
9269 025226 004737 011052 JSR     PC,RADE6 ;READ AND CHECK TRDI BUS BITS 39:32
9270 025232 001405      BEQ      27$      ;IF OK THEN CONTINUE
9271 025234              ERRDF    8,TEEDA1,E026ER ;TE TO SA XSEL1,EDSELO,ADDR 17:16 + BTS 3:0 ERRO
9272 025234 104455      TRAP    C$ERDF
9273 025236 000010      .WORD   8
9274 025240 003240      .WORD   TEEDA1
9275 025242 006210      .WORD   E026ER
9276 025244              CKLOOP
9277 025244 104406      TRAP    C$CLP1
9278
9279              ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL

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9336
9337 025314 004737 012434 JSR PC,XCASL ;SET XCAS H LOW AND XCAS L HIGH
9338 025320 004737 012540 JSR PC,XPIL ;SET XPI H LOW AND XPI L HIGH
9339
9340 ;READ THE VDAL REGISTER AND CHECK THAT THE ONLY SIGNAL SET IN THE
9341 ;VDAL REGISTER IS BIT 4, WHICH IS THE SIGNAL EDEOC H.
9342
9343 025324 052737 000020 002342 BIS #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE A ONE
9344 025332 004737 011176 JSR PC,READT4 ;READ AND CHEKC VDAL REGISTER
9345 025336 001405 BEQ 29$ ;IF EDEOC H SET THEN CONTINUE
9346 025340 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
9347 025340 104455 TRAP C$ERDF
9348 025342 000013 .WORD 11
9349 025344 003706 .WORD VDALRG
9350 025346 006714 .WORD T4EROR
9351 025350 CKLOOP
9352 025350 104406 TRAP C$CLP1
9353
9354 ;READ AND CHECK CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED
9355 ;WHEN XRAS, XCAS AND XPI WERE TOGGLED.
9356
9357 025352 004737 011112 29$: JSR PC,READT0 ;READ AND CHECK GDAL REGISTER
9358 025356 001405 BEQ 30$ ;IF NO CHANGES THEN CONTINUE
9359 025360 ERRDF 9,GDALRG,TOEROR ;GDAL REGISTER NOT EQUAL EXPECTED
9360 025360 104455 TRAP C$ERDF
9361 025362 000011 .WORD 9
9362 025364 003636 .WORD GDALRG
9363 025366 006664 .WORD TOEROR
9364 025370 CKLOOP
9365 025370 104406 TRAP C$CLP1
9366
9367 ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9368 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9369
9370 025372 004737 012142 30$: JSR PC,SLCTED ;SELECT THE STATE ANALYZER MODULE
9371
9372 ;IN PREVIOUS SELECTIONS OF THE STATE ANALYZER MODULE, CDAL3 H WAS SET
9373 ;TO A ONE AND CDAL2 H WAS SET TO A ZERO. THIS WAS DONE TO ASSERT THE
9374 ;SIGNAL TRSL2 L. WHEN TRSL2 L IS ASSERTED LOW, THE STATE ANALYZER
9375 ;SYSTEM BUS LATCHES ARE ENABLED TO THE STATE ANALYZERS TRDI BUS BITS
9376 ;59:0. BITS WERE ALSO LOADED INTO CONTROL REGISTER 2'S PDAL REGISTER TO
9377 ;SET THE SIGNAL PTER3 L IN THE POINTER REGISTER. WHEN A READ COMMAND IS
9378 ;ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER3 L IS ASSERTED LOW,
9379 ;TRDI BUS BITS 47:32 ARE READ. AS A RESULT OF PULSING THE SIGNAL XPI L
9380 ;ON THE TARGET EMULATOR MODULE, A PULSE SHOULD HAVE OCCURED ON THE
9381 ;SIGNAL EDCK4 H. A PULSE ON THE SIGNAL EDCK4 H WILL CLOCK THE TARGET
9382 ;EMULATOR SIGNALS XSEL1 H, EDSELO H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0
9383 ;INTO THE STATE ANALYZER SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).
9384 ;AT THE TIME XPI L WAS SET LOW, THE TARGET EMULATOR SIGNAL ASPI L WAS
9385 ;ALSO SET LOW, THUS SETTING THE SIGNALS OBTS2 H AND OBTS3 H TO THE HIGH
9386 ;STATE, THEREFORE THESE BITS SHOULD BE READ AS ONES ON STATE ANALYZER
9387 ;TRDI BITS 34 AND 35.
9388
9389 025376 012737 000014 002316 MOV #BIT3!BIT2,E6LOAD ;EXPECT OBTS3 H AND OBTS2 H TO BE ONES
9390 025404 004737 011052 JSR PC,READE6 ;READ AND CHECK TRDI BITS 39:32
9391 025410 001404 BEQ 31$ ;IF OK THEN CONTINUE

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.SBTTL TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40

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THIS TEST WILL CHECK THAT DATA LOADED INTO THE TARGET EMULATOR'S EOAI REGISTER CAN BE ENABLED TO THE CTL BUS, WHICH IS ON THE SYSTEM BUS, AND THAT THE CTL BUS CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM BUS CTL 7:0 LATCHES VIA THE TARGET EMULATOR'S CLOCKING SIGNAL 'ENCK5 H'. THE TEST WILL ALSO CHECK THAT THE EOAI REGISTER CAN BE CLOCKED INTO THE TARGET EMULATOR'S CTL REGISTER WHEN THE SIGNAL 'XCAS L' IS RETURNED TO THE DE-ASSERTED STATE AFTER HAVING BEEN ASSERTED. TO CHECK THAT THE EOAI REGISTER WAS CLOCKED INTO THE CTL REGISTER, THE PROGRAM WILL READ THE TARGET EMULATOR'S CTL REGISTER AND CHECK THE DATA TO BE THE ONE'S COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER. THE SYSTEM BUS CLOCKING SIGNAL 'ENCK5 H' IS GENERATED ON THE TARGET EMULATOR MODULE AS THE SIGNAL 'CKAI H'. THE PROGRAM WILL CAUSE THE SIGNAL 'CKAI H' TO BE PULSED IN DIFFERENT WAYS DURING THIS TEST. TO CHECK THAT THE EOAI REGISTER DATA CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM BUS CTL LATCHES AND THAT A PULSE CAN BE GENERATED ON THE SIGNAL 'ENCK5 H', THE PROGRAM WILL READ THE CTL 7:0 SYSTEM BUS LATCHES ON THE STATE ANALYZER'S TRDI BUS BITS 47:40 AND CHECK THAT THE DATA READ IS THE ONE'S COMPLEMENT OF THE DATA LOADED INTO THE TARGET EMULATOR'S EOAI REGISTER. THE TEST WILL ALSO CHECK THAT THE TARGET EMULATOR SIGNALS XSEL1 H, EDSELO H, ADDR17 H, ADDR16 H AND BTS BITS 3:0 H CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES BY READING THESE BITS ON STATE ANALYZER'S TRDI BUS BITS 39:32. THE TEST WILL LOAD THE EOAI REGISTER WITH THE FOLLOWING DATA PATTERNS 377, 000, 252, 125 AND 314.

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9433 025426
 9434 025426
 9435
 9436 025426 004737 007436
 9437
 9438 025432 012701 026574
 9439
 9440 025436
 9441 025436 104404
 9442
 9443
 9444
 9445
 9446 025440 004737 012212
 9447
 9448
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 9451
 9452
 9453
 9454
 9455
 9456 025444 012737 023020 002334
 9457 025452 004737 012764
 9458
 9459
 9460

T8:: BGNTST

JSR PC,INITMD ;INITIALIZE CDS-11 SYSTEM MODULES

MOV #30\$,R1 ;GET ADDRESS OF CTL DATA TABLE

1\$: BGNSEG

TRAP C\$BSEG

;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.

JSR PC,SLCTTE ;SELECT TARGET EMULATOR MODULE

;SET ADAL REGISTER BITS 13, 10, 9 AND 4 TO A ONE AND PULSE THE SIGNAL BRKRES L BY SETTING AND CLEARING ADAL REGISTER BIT 0.

: ADAL14H = 0 SELECTS CLOCKING EDGE OF XCAS TO PULSE CKAI H
 : ADAL13H = 1 ALLOWS ATC L TO GO LOW WHEN PPI L SET LOW
 : ADAL10H = 1 ENABLES TE SIGNALS TO CDS-11 SYSTEM BUS
 : ADAL9H = 1 WHEN ADAL10H=1 ENABLES EDCK 5:0 TO SYS BUS
 : ADAL4H = 1 SETS PAUSE MODE F/F TO RUN MODE WHEN XRAS H PULS

MOV #ADAL13!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED

JSR PC,BRKRES ;LOAD ABOVE BITS + PULSE BRKRES L

;SELECT THE MODE REGISTER BY SETTING GDAL BITS 2:0 TO 4. ON A WRITE OR
 ;READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL BE WRITTEN

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9461 ;OR READ.
9462
9463 025456 004537 012232 JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
9464 025462 000004 .WORD MODE ;SELECT THE MODE REGISTER
9465
9466 ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
9467 ;ZEROES. MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE.
9468
9469 025464 005037 002346 CLR T6LOAD ;SETUP DATA PATTERN OF ALL ZEROES
9470 025470 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK MODE REGISTER
9471 025470 001405 BEQ 2$ ;IF LOADED OK THEN CONTINUE
9472 025476 ERRDF 12,MODREG,T06ERR ;MODE REGISTER NOT EQUAL EXPECTED
9473 025476 104455 TRAP C$ERRDF
9474 025500 000014 .WORD 12
9475 025502 004000 .WORD MODREG
9476 025504 006730 .WORD T06ERR
9477 025506 CKLOOP
9478 025506 104406 TRAP C$CLP1
9479
9480 ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO
9481 ;A 2. THE EOAI AND FDAL REGISTER WILL BE ADDRESSES ON A WRITE OR READ
9482 ;COMMAND TO CONTROL REGISTER 6. THE EOAI REGISTER WILL BE SELECTED ON
9483 ;A READ COMMAND WHEN FDAL REGISTER BIT 0 IS SET TO A ONE.
9484
9485 025510 004537 012232 2$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
9486 025514 000002 .WORD FDAL ;SELECT EOAI AND FDAL REGISTER
9487
9488 ;WRITE THE EOAI REGISTER WITH THE DATA PATTERN FROM THE DATA TABLE. THIS
9489 ;DATA PATTERN WILL BE PLACED ONTO THE CTL BUS LATER ON IN THIS TEST.
9490 ;FDAL REGISTER BIT 0 WILL BE LOADED WITH A ONE AND ALL OTHER FDAL REGIS-
9491 ;TER BITS WILL BE LOADED WITH A ZERO. FDAL0 H ON A ONE WILL CAUSE THE
9492 ;EOAI REGISTER TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 INSTEAD
9493 ;OF THE CTL REGISTER.
9494
9495 025516 011137 002346 MOV (R1),T6LOAD ;GET DATA PATTERN FROM DATA TABLE
9496 025522 052737 000001 002346 BIS #FDALO,T6LOAD ;SET FDALO H TO A ONE
9497 025530 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK EOAI AND FDAL REG
9498 025534 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
9499 025536 ERRDF 12,EOAIFD,T06ERR ;EOAI OR FDAL REGISTER ERROR
9500 025536 104455 TRAP C$ERRDF
9501 025540 000014 .WORD 12
9502 025542 004045 .WORD EOAIFD
9503 025544 006730 .WORD T06ERR
9504 025546 CKLOOP
9505 025546 104406 TRAP C$CLP1
9506
9507 ;SELECT THE HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3. THE
9508 ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
9509 ;CONTROL REGISTER 6.
9510
9511 025550 004537 012232 3$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
9512 025554 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
9513
9514 ;SET ALL HDAL REGISTER BITS TO A ZERO EXCEPT HDAL REGISTER BIT 2. HDAL
9515 ;REGISTER BIT 2 ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
9516 ;TIMING AND CONTROL SIGNALS.

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9517
9518 025556 012737 000004 002346      MOV      #HDAL2,T6LOAD      ;SETUP BITS TO BE LOADED
9519 025564 004737 011214                JSR      PC,LDRDT6         ;LOAD, READ AND CHECK HDAL REGISTER
9520 025570 001405                BEQ      4$                ;IF LOADED OK THEN CONTINUE
9521 025572                ERRDF   12,HDALRG,T06ERR   ;HDAL REGISTER NOT EQUAL EXPECTED
9522 025572 104455                TRAP    C$ERDF
9523 025574 000014                .WORD   12
9524 025576 003754                .WORD   HDALRG
9525 025600 006730                .WORD   T06ERR
9526 025602
9527 025602 104406                CKLOOP
9528
9529                                TRAP    C$CLP1
9530                                ;PULSE THE SIGNAL INV D L BY SETTING AND CLEARING VDAL2 H IN CONTROL
9531                                ;REGISTER 4. PULSING THE SIGNAL INV D L ON THE TARGET EMULATOR MODULE
9532                                ;WILL INITIALIZE ALL THE FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT
9533                                ;INITIALIZED BY THE SIGNAL BRKRES L.
9534 025604 005037 002340      4$:    CLR      T4LOAD            ;SETUP TO CLEAR ALL OTHER R/W BITS
9535 025610 004737 012704                JSR      PC,CLRPSM        ;PULSE INV D L VIA VDAL2 H.
9536
9537                                ;PERFORM A T-11 TIMING CYCLE BY DOING THE FOLLOWING SEQUENCE:
9538                                ; 1. SET XRAS H AND XRAS L TO HIGH AND LOW STATE RESPECTIVELY
9539                                ; 2. SET XCAS H AND XCAS L TO HIGH AND LOW STATE RESPECTIVELY
9540                                ; 3. SET XPI H AND XPI L TO HIGH AND LOW STATE RESPECTIVELY
9541                                ; 4. SET XCAS H AND XCAS L TO LOW AND HIGH STATE RESPECTIVELY
9542                                ; 5. SET XPI H AND XPI L TO LOW AND HIGH STATE RESPECTIVELY
9543                                ; 6. SET XRAS H AND XCAS H TO LOW AND HIGH STATE RESPECTIVELY
9544                                ;AS A RESULT OF THE ABOVE TIMING SEQUENCE, A PULSE WILL BE ISSUED ON THE
9545                                ;SIGNALS EDCK4 H AND EDCK5 H. A PULSE ON EDCK4 H WILL CLOCK THE SIGNALS
9546                                ;XSEL1 H, EDSEL0 H, ADDR17 H, ADDR16 H, AND BTS BITS 3:0 INTO THE STATE
9547                                ;ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32). A PULSE ON
9548                                ;EDCK5 H, WHICH WAS GENERATED BY A PULSE ON THE SIGNAL CKAI H, WILL CLOCK
9549                                ;CTL BUS BITS 7:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE
9550                                ;BITS (TRDI 47:40). THE EOAI REGISTER IS ONLY ENABLED TO THE CTL BUS
9551                                ;WHEN PPI L IS ASSERTED LOW. WHEN PPI L IS ASSERTED LOW, THE EOAI
9552                                ;REGISTER WILL BE ENABLED TO THE CAI BUS VIA THE SIGNAL ATC L. THE
9553                                ;CAI BUS WILL BE ENABLED TO THE EIAI BUS UNCONDITIONALLY AND THE EIAI
9554                                ;BUS WILL BE ENABLED TO THE CTL BUS VIA THE SIGNAL ADAL10 H. THE
9555                                ;SIGNALS CKAI H AND EDCK5 H WILL GO FROM A HIGH STATE TO A LOW STATE AND
9556                                ;BACK TO A HIGH STATE WHEN THE SIGNAL XCAS L IS PULSED IN THE ABOVE
9557                                ;TIMING SEQUENCE. WHEN XCAS L IS RETURNED TO THE HIGH STATE, THE CTL
9558                                ;BUS DATA WILL BE CLOCKED INTO THE TARGET EMULATORS CTL REGISTER AND INTO
9559                                ;THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS. THE DATA CLOCKED
9560                                ;INTO THE TARGET EMULATORS CTL REGISTER AND THE STATE ANALYZERS SYSTEM
9561                                ;BUS LATCHES WILL BE THE ONES COMPLEMENT OF THE DATA LOADED INTO THE
9562                                ;EOAI REGISTER AT THE BEGINNING OF THIS TEST.
9563
9564 025614 004737 012276                JSR      PC,XRASH         ;SET XRAS H HIGH AND XRAS L LOW
9565 025620 004737 012402                JSR      PC,XCASH         ;SET XCAS H HIGH AND XCAS L LOW
9566 025624 004737 012506                JSR      PC,XPIH          ;SET XPI H HIGH AND XPI L LOW
9567 025630 004737 012434                JSR      PC,XCASL         ;SET XCAS H LOW AND XCAS L HIGH
9568 025634 004737 012540                JSR      PC,XPIL          ;SET XPI H LOW AND XPI L HIGH
9569 025640 004737 012330                JSR      PC,XRASL         ;SET XRAS H LOW AND XRAS L HIGH
9570
9571                                ;READ VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A ONE
9572                                ;AS A RESULT OF THE ABOVE TIMING SEQUENCE.

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9573
9574 025644 012737 000020 002342      MOV      #VDAL4,T4GOOD      ;EXPECT EDEOC H TO BE SET TO A ONE
9575 025652 004737 011176              JSR      PC,READT4         ;READ AND CHECK VDAL REGISTER
9576 025656 001405              BEQ      5$                ;IF OK THEN CONTINUE
9577 025660              ERRDF   11,VDALRG,T4EROR   ;VDAL REGISTER NOT EQUAL EXPECTED
9578 025660 104455              TRAP    C$ERDF
9579 025662 000013              .WORD   11
9580 025664 003706              .WORD   VDALRG
9581 025666 006714              .WORD   T4EROR
9582 025670
9583 025670 104406              CKLOOP
9584                                TRAP    C$CLP1
9585                                ;SELECT THE CTL/EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
9586                                ;TO A 2. THE CTL AND FDAL REGISTER WILL BE ADDRESSED ON A READ COMMAND
9587                                ;TO CONTROL REGISTER 6 WHEN FDALO H IS SET TO A ZERO.
9588
9589 025672 112737 000002 002324 5$:      MOVVB   #FDAL,T0LOAD      ;GET GDAL BITS TO BE LOADED
9590 025700 004737 011076              JSR      PC,LDRD10        ;LOAD, READ AND CHECK GDAL REGISTER
9591 025704 001405              BEQ      6$                ;IF LOADED OK THEN CONTINUE
9592 025706              ERRDF   9,GDALRG,TOEROR   ;GDAL REGISTER NOT EQUAL EXPECTED
9593 025706 104455              TRAP    C$ERDF
9594 025710 000011              .WORD   9
9595 025712 003636              .WORD   GDALRG
9596 025714 006664              .WORD   TOEROR
9597 025716
9598 025716 104406              CKLOOP
9599                                TRAP    C$CLP1
9600                                ;WRITE ALL ZEROES INTO THE FDAL REGISTER. THE EOAI REGISTER WILL NOT
9601                                ;BE CHANGED AT THIS POINT IN TIME. WHEN FDALO H IS SET TO A ZERO, THE
9602                                ;CTL REGISTER WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6
9603                                ;INSTEAD OF THE EOAI REGISTER.
9604
9605 025720 112777 000000 154264 6$:      MOVVB   #0,@REG6          ;WRITE 0'S INTO FDAL REGISTER ONLY
9606
9607                                ;READ THE CTL AND FDAL REGISTER TO CHECK THAT THE DATA READ IS THE 1'S
9608                                ;COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER AT THE BEGINNING
9609                                ;OF THIS TEST. THE CTL BUS DATA WAS CLOCKED INTO THE CTL REGISTER WHEN
9610                                ;THE SIGNAL XCAS L WAS SET TO THE HIGH STATE AFTER HAVING BEEN SET LOW.
9611
9612 025726 016137 000002 002346      MOV      2(R1),T6LOAD     ;GET 1'S COMPLEMENT OF EOAI REG DATA
9613 025734 004737 011222              JSR      PC,READT6        ;READ CTL AND FDAL REGISTER
9614 025740 001405              BEQ      7$                ;IF DATA OK THEN CONTINUE
9615 025742              ERRDF   12,CTLFDL,T06ERR  ;CTL 7:0 OR FDAL 7:0 REG ERROR
9616 025742 104455              TRAP    C$ERDF
9617 025744 000014              .WORD   12
9618 025746 004104              .WORD   CTLFDL
9619 025750 006730              .WORD   T06ERR
9620 025752
9621 025752 104406              CKLOOP
9622                                TRAP    C$CLP1
9623                                ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9624                                ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9625
9626 025754 004737 012142              JSR      PC,SLCTED        ;SELECT STATE ANALYZER MODULE
9627
9628                                ;SET THE SIGNAL TRSL2 L TO THE LOW STATE BY SETTING CDAL3 H TO A ONE AND
  
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9629                                     ;CDAL2 H TO A ZERO IN CONTROL REGISTER 0. THE SIGNAL TRSL2 L WILL ENABLE
9630                                     ;THE STATE ANALYZER'S SYSTEM BUS LATCHES TO TRDI BUS BITS 59:0.
9631
9632 025760 112737 000010 002272      MOVB    #CDAL3,E0LOAD          ;SETUP CDAL REGISTER BITS TO LOAD
9633 025766 004737 010676              JSR     PC,LDRDE0            ;LOAD, READ AND CHECK CDAL REGISTER
9634 025772 001405                      BEQ     8$                  ;IF LOADED OK THEN CONTINUE
9635 025774                                ERRDF   5,CDALRG,E0EROR      ;CDAL REGISTER NOT EQUAL EXPECTED
9636 025774 104455                      TRAP   C$ERDF
9637 025776 000005                      .WORD  5
9638 026000 003006                      .WORD  CDALRG
9639 026002 006144                      .WORD  E0EROR
9640 026004                                CKLOOP
9641 026004 104406                      TRAP   C$CLP1
9642
9643                                     ;ASSERT THE SIGNAL PTER3 L IN THE POINTER REGISTER BY LOADING THE
9644                                     ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.
9645
9646 026006 004537 012162      8$:   JSR     R5,LDPDAL          ;LOAD AND CHECK PDAL REGISTER
9647 026012 000003              .WORD  PTER3                ;SETUP TO READ TRDI BUS BITS 47:32
9648
9649                                     ;AS A RESULT OF PERFORMING A NORMAL T-11 TIMING CYCLE, A PULSE SHOULD
9650                                     ;HAVE OCCURED ON THE SIGNAL EDCK4 H AND A PULSE SHOULD HAVE OCCURED
9651                                     ;ON THE SIGNAL EDCK5 H. A PULSE ON EDCK4 H WILL CLOCK THE TARGET
9652                                     ;EMULATOR SIGNALS XSEL1 H, EDSELO H, ADDR17 H, ADDR16 H, AND BTS BITS
9653                                     ;3:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS. THESE
9654                                     ;BITS WILL BE READ ON TRDI BUS BITS 39:32. A PULSE ON EDCK5 H WILL
9655                                     ;CLOCK THE TARGET EMULATORS CTL BUS INTO THE STATE ANALYZERS SYSTEM BUS
9656                                     ;LATCHES FOR THESE BITS. THESE BITS WILL BE READ ON TRDI BUS BITS 47:40.
9657                                     ;A PULSE ON THE SIGNAL EDCK5 H, VIA THE SIGNAL CKAI H WILL CLOCK THE
9658                                     ;CTL BUS DATA, WHICH HAS EOAI REGISTER DATA ENABLED TO IT VIA THE CAI
9659                                     ;AND EIAI BUS, INTO THE STATE ANALYZERS SYTEM BUS LATCHES. THE DATA
9660                                     ;READ ON TRDI BUS BITS 47:40 WILL BE THE ONES COMPLEMENT OF THE DATA
9661                                     ;LOADED INTO THE TARGET EMULATORS EOAI REGISTER. THE SIGNAL BTS0 H
9662                                     ;SHOULD BE SET TO A ONE ON THE TARGET EMULATOR MODULE, THEREFORE, TRDI
9663                                     ;BIT 32 SHOULD BE READ AS A ONE ALSO.
9664
9665 026014 016137 000002 002316      MOV     2(R1),E6LOAD         ;GET 1'S COMP OF EOAI REG DATA LOADED
9666 026022 052737 000001 002316      BIS     #BIT0,E6LOAD         ;EXPECT BTS0 H TO BE SET TO A ONE
9667 026030 004737 011052              JSR     PC,READE6            ;READ AND CHECK TRDI BUS BITS 47:32
9668 026034 001405                      BEQ     9$                  ;IF DATA OK THEN CONTINUE
9669 026036                                ERRDF   8,TEEDCT,E026ER      ;TE CTL BUS 7:0 TO SA TRDI BUS BITS 47:40 ERROR
9670 026036 104455                      TRAP   C$ERDF
9671 026040 000010                      .WORD  8
9672 026042 003342                      .WORD  TEEDCT
9673 026044 006210                      .WORD  E026ER
9674 026046                                CKLOOP
9675 026046 104406                      TRAP   C$CLP1
9676
9677                                     ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
9678                                     ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9679
9680 026050 004737 012212      9$:   JSR     PC,SLCTTE          ;SELECT THE TARGET EMULATOR MODULE
9681
9682                                     ;LOAD, READ AND CHECK THE EOAI AND FDAL REGISTER. THE FDAL REGISTER
9683                                     ;WAS SELECTED IN THE PREVIOUS SELECTION OF THE TARGET EMULATOR MODULE.
9684                                     ;THE EOAI REGISTER WILL BE LOADED WITH THE ONES COMPLEMENT OF THE DATA

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9685 ;LOADED INTO IT IN THE PREVIOUS SELECTION OF THE TARGET EMULATOR MODULE.
9686
9687 026054 016137 000002 002346 MOV 2(R1),T6LOAD ;GET THE DATA FROM THE DATA TABLE
9688 026062 052737 000001 002346 BIS #FDAL0,T6LOAD ;SELECT EOAI REGISTER TO BE READ
9689 026070 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK EOAI + FDAL REG
9690 026074 001405 BEQ 10$ ;IF LOADED OK THEN CONTINUE
9691 026076 ERRDF 12,EOA:FD,T06ERR ;EOAI 7:0 OF FDAL 7:0 REG ERROR
9692 026076 104455 TRAP C$ERDF
9693 026100 000014 .WORD 12
9694 026102 004045 .WORD EOAI:FD
9695 026104 006730 .WORD T06ERR
9696 026106 CKLOOP
9697 026106 104406 TRAP C$CLP1
9698
9699 ;SET ADAL REGISTER BITS 15 AND 14 TO ONES. WHEN THESE TWO BITS ARE SET
9700 ;TO ONES, THE SIGNALS CKAI H AND EDCK5 H WILL BE SET HIGH WHEN THE
9701 ;SIGNAL XCAS H IS SET HIGH. THE SIGNAL EDCK5 H GOING FROM A LOW TO A
9702 ;HIGH STATE WILL CLOCK THE CTL BUS INTO THE STATE ANALYZERS SYSTEM BUS
9703 ;LATCHES FOR THOSE BITS.
9704
9705 026110 052737 140000 002334 10$: BIS #ADAL15!ADAL14,T2LOAD ;SETUP ADAL BITS TO BE LOADED
9706 026116 004737 011136 JSR PC,LDRDT2 ;LOAD, READ AND CHECK ADAL REGISTER
9707 026122 001405 BEQ 11$ ;IF LOADED OK THEN CONTINUE
9708 026124 ERRDF 10,ADALRG,T2EROR ;ADAL REGISTER NOT EQUAL EXPECTED
9709 026124 104455 TRAP C$ERDF
9710 026126 000012 .WORD 10
9711 026130 003662 .WORD ADALRG
9712 026132 006700 .WORD T2EROR
9713 026134 CKLOOP
9714 026134 104406 TRAP C$CLP1
9715
9716 ;SELECT THE HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3. ON
9717 ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL
9718 ;BE WRITTEN OR READ.
9719
9720 026136 004537 012232 11$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
9721 026142 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
9722
9723 ;SET THE SIGNALS XR/WHB L AND XR/WLB L TO THE LOW STATE BY SETTING HDAL
9724 ;REGISTER BITS 4 AND 3 TO ONES. SETTING THESE TWO SIGNALS LOW WILL
9725 ;CAUSE THE SIGNAL BTSO H TO GO FROM A HIGH TO A LOW STATE. THIS IS DONE
9726 ;TO CHECK THAT A PULSE IS ISSUED ON THE SIGNAL EDCK4 H WHEN THE SIGNAL
9727 ;XPI L IS SET TO THE LOW STATE FROM THE HIGH STATE.
9728
9729 026144 012737 000034 002346 MOV #HDAL4!HDAL3!HDAL2,T6LOAD ;SETUP BITS TO BE LOADED
9730 026152 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK HDAL REGISTER
9731 026156 001405 BEQ 12$ ;IF LOADED OK THEN CONTINUE
9732 026160 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
9733 026160 104455 TRAP C$ERDF
9734 026162 000014 .WORD 12
9735 026164 003754 .WORD HDALRG
9736 026166 006730 .WORD T06ERR
9737 026170 CKLOOP
9738 026170 104406 TRAP C$CLP1
9739
9740 ;SET THE SIGNALS XPI L AND PPI L TO THE LOW STATE BY SETTING HDAL REGIS-

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9741 ;TER BIT 15 TO A ONE. WHEN PPI L IS SET LOW, THE SIGNAL ATC L WILL BE
9742 ;ASSERTED LOW THUS ENABLING THE EOAI REGISTER TO THE CAI BUS. THE CAI
9743 ;BUS WILL BE ENABLED TO THE EIAI BUS UNCONDITIONALLY AND THE EIAI BUS
9744 ;WILL BE ENABLED TO THE CTL BUS BY ADAL REGISTER BIT 10 BEING SET TO A
9745 ;ONE. WHEN XPI L IS SET LOW, THE SIGNAL EDCK4 H WILL GO FROM A LOW TO
9746 ;A HIGH STATE THUS CLOCKING THE SIGNALS XSEL1 H, EDSELO H, ADDR17 H,
9747 ;ADDR16 H AND BTS BITS 3:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES
9748 ;FOR THESE BITS (TRDI BUS BITS 39:32).
9749
9750 026172 004737 012506 12$: JSR PC,XPIH ;SET XPI L AND PPI L TO LOW STATE
9751
9752 ;SET THE SIGNAL XCAS H TO THE HIGH STATE AND THE SIGNAL XCAS L TO THE
9753 ;LOW STATE. WHEN XCAS H IS SET HIGH, THE SIGNALS CKAI H AND EDL45 H
9754 ;WILL GO FROM A LOW TO A HIGH STATE, THUS CLOCKING THE CTL 7:0 BUS INTO
9755 ;THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS (TRDI BUS BITS 47:40).
9756
9757 C26176 004737 012402 JSR PC,XCASH ;SET XCAS H HIGH AND XCAS L LOW
9758
9759 ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H WENT TO A ZERO
9760 ;WHEN XCAS L WAS ASSERTED LOW.
9761
9762 026202 005037 002342 CLR T4GOOD ;EXPECT ALL VDAL BITS TO BE A ZERO
9763 C26206 004737 011170 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
9764 026212 001405 BEQ 13$ ;IF ALL ZERO THEN CONTINUE
9765 026214 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
9766 026214 104455 TRAP C$ERRDF
9767 026216 000013 .WORD 11
9768 026220 003706 .WORD VDALRG
9769 026222 006714 .WORD T4EROR
9770 026224 CKLOOP
9771 026224 104406 TRAP C$CLP1
9772
9773 ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9774 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9775
9776 026226 004737 012142 13$: JSR PC,SLCTED ;SELECT THE STATE ANALYZER MODULE
9777
9778 ;IN THE PREVIOUS SELECTION OF THE STATE ANALYZER MODULE, THE SIGNAL
9779 ;TRSL2 L WAS ASSERTED LOW TO ENABLE THE STATE ANALYZERS SYSTEM BUS
9780 ;LATCHES ONTO TRDI BUS BITS 59:0, AND PTER3 L WAS ASSERTED LOW IN
9781 ;THE POINTER REGISTER SO THAT TRDI BUS BITS 47:32 COULD BE READ ON A
9782 ;READ COMMAND TO CONTROL REGISTER 6. THIS NEXT SECTION WILL READ TRDI
9783 ;BUS BITS 47:32 TO CHECK THAT THE TARGET EMULATORS CTL BUS BITS 7:0 AND
9784 ;THE SIGNALS XSEL1 H, EDSELO H, ADDR17 H, ADDR16 H, AND BTS BITS 3:0
9785 ;WERE CLOCKED INTO THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE
9786 ;BITS VIA THE TARGET EMULATORS SIGNALS EDCK5 H AND EDCK4 H. WHEN THE
9787 ;CTL BUS IS READ ON TRDI BUS BITS 47:40, THE DATA WILL BE THE ONES
9788 ;COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER IN THE PREVIOUS
9789 ;SELECTION OF THE TARGET EMULATOR MODULE. THE SIGNAL BTSO H SHOULD BE
9790 ;REAL AS A ZERO ON TRDI BUS BIT 32.
9791
9792 026232 011137 002316 MOV (R1),E6LOAD ;GET 1'S COMP OF EOAI DATA LOADED
9793 026236 004737 011052 JSR PC,READE6 ;READ AND CHECK TRDI BUS BITS 47:32
9794 026242 001405 BEQ 14$ ;IF DATA OK THEN CONTINUE
9795 026244 ERRDF 8,TEEDCT,E026ER ;TE CTL BUS 7:0 TO SA TRDI BUS BITS 47:32 ERROR
9796 026244 104455 TRAP C$ERRDF
  
```

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TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40

SEQ 0191

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9797 026246 000010      .WORD      8
9798 026250 003342      .WORD      TEEDCT
9799 026252 006210      .WORD      E026ER
9800 026254              CKLOOP
9801 026254 104406      TRAP      C$CLP1
9802
9803                      ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
9804                      ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9805
9806 026256 004737 012212 14$: JSR      PC,SLCTTE      ;SELECT THE TARGET EMULATOR MODULE
9807
9808                      ;SET THE SIGNAL XCAS H TO THE LOW STATE AND THE SIGNAL XCAS L TO THE
9809                      ;HIGH STATE.  SETTING XCAS L TO THE HIGH STATE WILL CLOCK THE CTL BUS
9810                      ;INTO THE CTL REGISTER.  ALSO SET THE SIGNALS XPI L AND PPI L TO THE
9811                      ;HIGH STATE.  SETTING PPI L TO THE HIGH STATE WILL DISABLE THE EOAI
9812                      ;REGISTER TO THE CAI BUS.
9813
9814 026262 004737 012434 JSR      PC,XCASL      ;SET XCAS H LOW AND XCAS L HIGH
9815 026266 004737 012540 JSR      PC,XPIL      ;SET XPI L HIGH AND PPI L HIGH.
9816
9817                      ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H IS SET TO
9818                      ;A ONE AS A RESULT OF XCAS L BEING SET TO THE HIGH STATE.
9819
9820 026272 012737 000020 002342 MOV      #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE SET TO A ONE
9821 026300 004737 011176 JSR      PC,READT4    ;READ AND CHECK VDAL REGISTER
9822 026304 001405 BEQ      15$         ;IF LOADED OK THEN CONTINUE
9823 026306 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
9824 026306 104455 TRAP     C$ERDF
9825 026310 000013 .WORD    11
9826 026312 003706 .WORD    VDALRG
9827 026314 006714 .WORD    T4EROR
9828 026316 CKLOOP
9829 026316 104406 TRAP     C$CLP1
9830
9831                      ;SELECT THE CTL/EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
9832                      ;TO A 2.  THE CTL AND FDAL REGISTER WILL BE ADDRESSED ON A READ COMMAND
9833                      ;COMMAND TO CONTROL REGISTER 6 WHEN FDAL REGISTER BIT 0 IS A ZERO.
9834
9835 026320 112737 000002 002324 15$: MOVB     #FDAL,TOLOAD ;GET GDAL BITS TO BE LOADED
9836 026326 004737 011076 JSR      PC,LDRD0    ;LOAD, READ AND CHECK GDAL REGISTER
9837 026332 001405 BEQ      16$         ;IF LOADED OK THEN CONTINUE
9838 026334 ERRDF 9,GDALRG,TOEROR ;GDAL REGISTER NOT EQUAL EXPECTED
9839 026334 104455 TRAP     C$ERDF
9840 026336 000011 .WORD    9
9841 026340 003636 .WORD    GDALRG
9842 026342 006664 .WORD    TOEROR
9843 026344 CKLOOP
9844 026344 104406 TRAP     C$CLP1
9845
9846                      ;WRITE ALL ZEROES INTO THE FDAL REGISTER.  THE EOAI REGISTER DATA WILL
9847                      ;NOT BE CHANGED ON THIS WRITE COMMAND.  WHEN FDALO H IS SET TO A ZERO,
9848                      ;THE CTL AND FDAL REGISTER WILL BE READ ON A READ COMMAND TO CONTROL
9849                      ;REGISTER 6 INSTEAD OF THE EOAI AND FDAL REGISTER.
9850
9851 026346 112777 000000 153636 16$: MOVB     #0,@REG6    ;LOAD FDAL REG WITH ALL ZEROES
9852

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9853                                     :READ THE CTL AND FDAL REGISTER TO CHECK THAT THE DATA READ FROM THE
9854                                     :CTL REGISTER IS THE ONES COMPLEMENT OF THE DATA LOADED INTO THE EOAI
9855                                     :REGISTER. THE CTL BUS DATA WAS CLOCKED INTO THE CTL REGISTER WHEN THE
9856                                     :SIGNAL XCAS L WAS SET FROM A LOW TO A HIGH STATE.
9857
9858 026354 011137 002346                 MOV      (R1),T6LOAD                :GET 1'S COMP OF EOAI REGISTER DATA
9859 026360 004737 011222                 JSR      PC,READT6                :READ CTL AND FDAL REGISTER DATA
9860 026364 001405                         BEQ      17$                      :IF DATA OK THEN CONTINUE
9861 026366                                 ERRDF   12,CTLFDL,T06ERR          :CTL 7:0 OR FDAL 7:0 REGISTER ERROR
9862 026366 104455                         TRAP    C$ERDF
9863 026370 000014                         .WORD   12
9864 026372 004104                         .WORD   CTLFDL
9865 026374 006730                         .WORD   T06ERR
9866 026376                                 CKLOOP
9867 026376 104406                         TRAP    C$CLP1
9868
9869                                     :LOAD, READ AND CHECK EOAI AND FDAL REGISTER. THE EOAI REGISTER WILL
9870                                     :BE LOADED WITH A DATA PATTERN OF 314. THE FDAL REGISTER WILL BE LOADED
9871                                     :WITH A DATA PATTERN OF 001. WHEN FDALO H IS SET TO A ONE AND A READ
9872                                     :COMMAND IS ISSUED TO CONTROL REGISTER 6, THE EOAI AND FDAL REGISTER
9873                                     :WILL BE READ INSTEAD OF THE CTL AND FDAL REGISTERS.
9874
9875 026400 012737 146001 002346 17$:     MOV      #146001,T6LOAD           :GET EOAI AND FDAL DATA PATTERNS
9876 026406 004737 011214                 JSR      PC,LDRDT6                :LOAD, READ AND CHECK EOAI AND FDAL
9877 026412 001405                         BEQ      18$                      :IF LOADED OK THEN CONTINUE
9878 026414                                 ERRDF   12,EOAIFD,T06ERR          :EOAI 7:0 OR FDAL 7:0 REGISTER ERROR
9879 026414 104455                         TRAP    C$ERDF
9880 026416 000014                         .WORD   12
9881 026420 004045                         .WORD   EOAIFD
9882 026422 006730                         .WORD   T06ERR
9883 026424                                 CKLOOP
9884 026424 104406                         TRAP    C$CLP1
9885
9886                                     :SET ADAL REGISTER BIT 15 TO A ZERO AND LEAVE BIT 14 SET TO A ONE. WHEN
9887                                     :ADAL BIT 15 IS SET TO A ZERO AND BIT 14 IS SET TO A ONE AND A PULSE IS
9888                                     :ISSUED ON THE SIGNAL XRAS H, A PULSE WILL BE ISSUED ON THE SIGNAL RASP L
9889                                     :WHICH WILL CAUSE A PULSE TO BE ISSUED ON THE SIGNALS CKAI H AND EDCK, H.
9890                                     :A PULSE ON THE SIGNAL EDCK5 H WILL CLOCK THE CTL BUS DATA INTO THE STATE
9891                                     :ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS (TRDI 47:40).
9892
9893 026426 042737 100000 002334 18$:     BIC      #ADAL15,T2LOAD           :SETUP TO CLEAR ADAL BIT 15
9894 026434 004737 011136                 JSR      PC,LDRDT2                :LOAD, READ AND CHECK ADAL REGISTER
9895 026440 001405                         BEQ      19$                      :IF LOADED OK THEN CONTINUE
9896 026442                                 ERRDF   10,ADALRG,T2EROR          :ADAL REGISTER NOT EQUAL EXPECTED
9897 026442 104455                         TRAP    C$ERDF
9898 026444 000012                         .WORD   10
9899 026446 003662                         .WORD   ADALRG
9900 026450 006700                         .WORD   T2EROR
9901 026452                                 CKLOOP
9902 026452 104406                         TRAP    C$CLP1
9903
9904                                     :SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. ON A WRITE
9905                                     :OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE
9906                                     :WRITTEN OR READ.
9907
9908 026454 004537 012232                 JSR      R5,SELTERR              :SELECT REGISTER SPECIFIED BY NEXT WORD

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9909 026460 000003          .WORD  HDAL          ;SELECT THE HDAL REGISTER
9910
9911                      ;SET THE SIGNALS XR/WHB L AND XR/WLB L BACK TO THE HIGH STATE BY SETTING
9912                      ;HDAL REGISTER BITS 4 AND 3 TO A ZERO. THIS WILL CAUSE THE SIGNAL BTSO H
9913                      ;TO BE SET TO THE HIGH STATE (1).
9914
9915 026462 012737 000004 002346  MOV    #HDAL2,T6LOAD    ;SETUP BIT TO BE LOADED
9916 026470 004737 011214          JSR    PC,LDRDT6      ;LOAD, READ AND CHECK HDAL REGISTER
9917 026474 001405          BEQ    20$           ;IF LOADED OK THEN CONTINUE
9918 026476          ERRDF  12,HDALRG,T06ERR    ;HDAL REGISTER NOT EQUAL EXPECTED
9919 026476 104455          TRAP  C$ERRDF
9920 026500 000014          .WORD  12
9921 026502 003754          .WORD  HDALRG
9922 026504 006730          .WORD  T06ERR
9923 026506          CKLOOP
9924 026506 104406          TRAP  C$CLP1
9925
9926                      ;SET THE SIGNALS XPI L AND PPI L TO THE LOW STATE BY SETTING HDAL REGISTER
9927                      ;BIT 15 TO A ONE. WHEN XPI L IS SET TO THE LOW STATE, THE SIGNAL EDCK4 H
9928                      ;WILL BE SET HIGH THUS CLOCKING THE SIGNALS XSEL1 H, EDSELO H, ADDR17 H,
9929                      ;ADDR16 H, AND BTS BITS 3:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES
9930                      ;FOR THESE BITS (TRDI 39:32). SETTING THE SIGNAL PPI L TO THE LOW STATE
9931                      ;WILL CAUSE THE SIGNAL ATC L TO BE SET LOW WHICH WILL ENABLE THE EOAI
9932                      ;REGISTER TO THE CAI BUS. THE CAI BUS WILL BE ENABLED TO THE EIAI BUS
9933                      ;AND TO THE CTL BUS VIA ADAL10 H.
9934
9935 026510 004737 012506          20$:  JSR    PC,XPIH          ;SET XPI L AND PPI L TO LOW STATE
9936
9937                      ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL REGISTER BIT 12.
9938                      ;WHEN XRAS H IS PULSED, A PULSE WILL OCCUR ON THE SIGNAL RASP L. WHEN
9939                      ;ADAL BIT 15 IS A ZERO AND ADAL BIT 14 IS A ONE AND A PULSE IS ISSUED
9940                      ;ON THE SIGNAL RASP L, A PULSE WILL OCCUR ON THE SIGNAL CKAI H WHICH WILL
9941                      ;CAUSE A PULSE TO OCCUR ON THE SIGNAL EDCK5 H. A PULSE ON THE SIGNAL
9942                      ;EDCK5 H WILL CLOCK THE TARGET EMULATORS CTL BUS INTO THE STATE ANALYZERS
9943                      ;SYSTEM BUS LATCHES FOR THESE BITS (TRDI BITS 47:40).
9944
9945 026514 004737 012264          JSR    PC,XRAS          ;GO PULSE XRAS H VIA HDAL12 H
9946
9947                      ;DISABLE THE EOAI REGISTER FROM THE CTL BUS BY SETTING THE SIGNALS XPI L
9948                      ;AND PPI L TO THE HIGH STATE BY SETTING HDAL REGISTER BIT 15 TO A ZERO.
9949
9950 026520 004737 012540          JSR    PC,XPIL          ;SET XPI L AND PPI L TO HIGH STATE
9951
9952                      ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9953                      ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9954
9955 026524 004737 012142          JSR    PC,SLCTED       ;SLECT THE STATE ANALYZER MODULE
9956
9957                      ;IN A PREVIOUS SELECTION OF THE STATE ANALYZER MODULE, THE SIGNAL
9958                      ;TPSL2 L WAS ASSERTED LOW TO ENABLE THE STATE ANALYZERS SYSTEM BUS
9959                      ;LATCHES ONTO TRDI BUS BITS 59:0, AND PTER3 L WAS ASSERTED LOW IN
9960                      ;THE POINTER REGISTER SO THAT TRDI BUS BITS 47:32 COULD BE READ ON A
9961                      ;READ COMMAND TO CONTROL REGISTER 6. THIS NEXT SECTION WILL READ TRDI
9962                      ;BITS 47:32 TO CHECK THAT THE TARGET EMULATORS CTL BUS BITS 7:0 AND
9963                      ;THE SIGNALS XSEL1 H, EDSELO H, ADDR17 H, ADDR16 H, AND BTS BITS 3:0
9964                      ;WERE CLOCKED INTO THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE

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.SBTTL TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT

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THIS TEST WILL CHECK THAT THE MEMORY SIMULATOR 'RD.' FLIP-FLOP CAN BE CLEARED WHEN A READ OPERATION IS EXECUTED FROM THE TARGET EMULATOR MODULE TO AN ADDRESS WHICH IS MAPPED IN THE MEMROY SIMULATOR'S MAP PROTECTION RAM TO INHIBIT READS AND WRITES. THE 'RDV' FLIP-FLOP WILL BE CLOCKED TO A ZERO AS A RESULT OF THE SIGNAL 'RDE H' BEING ASSERTED LOW AND A PULSE ON THE SIGNAL 'RDS H'. THE SIGNAL 'RDS H' WILL BE PULSED WHEN THE MEMORY SIMULATOR SIGNAL 'CTS H' IS ASSERTED HIGH AND A PULSE IS ISSUED ON THE TARGET EMULATOR SIGNAL 'READ H'. A PULSE WILL OCCUR ON THE SIGNAL 'READ H' WHEN A T-11 READ OPERATION IS BEING EXECUTED BY THE TARGET EMULATOR MODULE. THE PROGRAM WILL CHECK THAT THE MEMORY SIMULATOR SIGNAL 'MSBRK H' IS ASSERTED HIGH AS A RESULT OF THE 'RDV' FLIP-FLOP BEING CLEARED. THE PROGRAM WILL CHECK THE TARGET EMULATOR MODULES 'MEMBRK' FLIP-FLOP TO BE CLEARED AND THEN CAUSE A PULSE TO BE ISSUED ON TARGET EMULATOR SIGNAL 'XRAS H'. THE PROGRAM WILL NOW CHECK THE 'MEMBRK' FLIP-FLOP TO BE SET TO A ONE AS A RESULT OF A PULSE ON 'XRAS H' AND THE MEMORY SIMULATOR'S SYSTEM BUS SIGNAL 'MSBRK H' BEING ASSERTED HIGH. THE PROGRAM WILL NOW PRESET THE 'RDV' FLIP-FLOP BY PULSING MEMORY SIMULATOR SIGNAL 'RST H'. THE PROGRAM WILL CHECK THAT THE 'RDV' FLIP-FLOP PRESET AND THAT THE SIGNAL 'MSBRK H' WENT TO THE LOW STATE AS A RESULT OF THE 'RDV' FLIP-FLOP BEING PRESET. THE PROGRAM WILL NOW PULSE THE TARGET EMULATOR SIGNAL 'XRAS H' AGAIN AND CHECK THAT THE 'MEMBRK' FLIP-FLOP IS STILL SET TO A ONE AS A RESULT OF THE FLIP-FLOP BEING LATCHED ONCE IT HAS BEEN SET. THE PROGRAM WILL NOW PULSE TARGET EMULATOR SIGNAL 'BRKRES L' AND CHECK THAT THE 'MEMBRK' FLIP-FLOP WAS CLEARED. THE PROGRAM WILL NOW SET THE TARGET EMULATOR SIGNAL 'FETCT H' TO THE HIGH STATE AND PULSE THE SIGNAL 'XRAS H'. A PULSE ON 'XRAS H' WILL CAUSE THE EDFET FLIP-FLOP TO BE SET AND THE ADDRESS TO BE CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES. THE ADDRESS WILL ADDRESS MEMORY ON THE MEMORY SIMULATOR MODULE WHICH IS MAPPED TO INHIBIT READS AND WRITES, THEREFORE, THE SYSTEM BUS SIGNAL 'RDE L' WILL BE ASSERTED HIGH. AS A RESULT OF 'RDE L', 'EDFFT H', 'PSMW L' BEING ASSERTED HIGH AND A PULSE ON 'XRASD H', THE 'MEMBRK' FLIP-FLOP WILL BE DIRECT SET TO A ONE. THE SIGNAL 'MEMBRK H' ASSERTED HIGH WILL CAUSE THE SIGNAL 'SOP H' TO BE ASSERTED HIGH. WHEN 'SOP H' AND 'EDFET H' ARE ASSERTED HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE. THE PROGRAM WILL CHECK THAT THE 'MEMBRK' AND 'PSMW' FLIP-FLOPS ARE SET TO ONES. THE PROGRAM WILL NOW SET THE TARGET EMULATOR'S INTERRUPT ENBALE BIT AND LOWER THE CPU PRIORITY LEVEL TO ALLOW INTERRUPTS. THE BREAK INTERRUPT FLIP-FLOP WAS SET TO A ONE PREVIOUSLY AS A RESULT OF 'MEMBRK H' BEING ASSERTED HIGH AND A PULSE BEING ISSUED ON 'XRAS L'. THE PROGRAM WILL NOW CHECK THAT AN INTERRUPT OCCURED AS A RESULT OF THE INTERRUPT ENABLE BIT BEING SET, THE BREAK INTERRUPT FLIP-FLOP BEING SET, AND THE CPU PRIORITY LEVEL BEING LOWERED TO ALLOW INTERRUPTS. THE PROGRAM WILL ISSUE A PULSE ON 'BRKRES L' AND CHECK THAT THE 'MEMBRK' FLIP-FLOP WAS CLEARED BY THE PULSE ON 'BRKRES L'.

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T9: BGNTST

JSR PC,INITMD ;INITIALIZE CDS-11 SYSTEM MODULES

BGNSEG TRAP CSBSEG

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026610
026610
026610 004737 007436
026614
026614 104404


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10053
10054 026616          SETPRI #PRI07          ;RAISE CPU PRIORITY TO 7
10055 026616 012700 000340 MOV #PRI07,R0
10056 026622 104441 TRAP C$SPRI
10057
10058 ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10059 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10060
10061 026624 004737 011246 JSR PC,SLCTMS          ;SELECT MEMORY SIMULATOR MODULE
10062
10063 ;GO LOAD, READ AND CHECK THE MEMORY SIMULATOR MAP PROTECTION RAM. THE
10064 ;MAP PROTECTION RAM WILL HAVE THE BITS 'MUTB H' AND 'MPIN H' SET TO
10065 ;ONES FOR ALL ADDRESSES IN THE MAP PROTECTION RAM. MAP PROTECTION RAM
10066 ;BITS 'WRE H' AND 'RDE H' WILL BE SET TO ONES FOR THE FIRST 16K WORDS OF
10067 ;MEMORY SIMULATOR RAM AND TO ZEROES FOR ALL ADDRESSES ABOVE 16K WORDS.
10068 ;WHEN 'RDE H' AND 'WRE H' ARE SET TO ONES, READ AND WRITES ARE ALLOWED
10069 ;TO THOSE ADDRESSES.
10070
10071 026630 004737 011354 JSR PC,MPRAM          ;GO LOAD, READ AND CHECK MAP PROTECT RAM
10072
10073 ;GO LOAD, READ AND CHECK MODULE SELECT RAM 0. THE FOLLOWING DATA
10074 ;PATTERNS: 1, 2, 4, 10, 0, 0, 0, AND 0 WILL BE LOADED INTO CONSECUTIVE
10075 ;LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS 0. THESE PATTERNS
10076 ;WILL ENABLE THE FIRST 16K WORDS OF THE MEMORY SIMULATOR RAM TO BE
10077 ;ADDRESSED.
10078
10079 026634 004737 011640 JSR PC,MSRAM0        ;LOAD, READ AND CHECK MODULE SELECT RAM 0
10080
10081 ;GO LOAD, READ AND CHECK MODULE SELECT RAM 1. THE FOLLOWING DATA PATTERNS
10082 ;WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
10083 ;AT ADDRESS 0; 17, 0, 0 AND 0. THESE PATTERNS WILL ENABLE THE FIRST 32K
10084 ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
10085
10086 026640 004737 012010 JSR PC,MSRAM1        ;LOAD, READ AND CHECK MODULE SELECT RAM 1
10087
10088 ;SET THE SIGNAL 'CTS H' TO A ONE IN CONTROL REGISTER 0. THIS WILL
10089 ;ENABLE THE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR LOGIC.
10090 ;IN THIS TEST, 'CTS H' ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO
10091 ;THE MEMORY SIMULATOR MODULE AND THE MEMORY SIMULATOR RAM DATA ONTO THE
10092 ;SYSTEM BUS.
10093
10094 026644 052737 000002 002234 BIS #CTSH,SLOAD      ;SETUP BIT TO BE LOADED
10095 026652 004737 010504 JSR PC,LDRDS0        ;GO LOAD, READ AND CHECK CONTROL REG 2
10096 026656 001405 BEQ 1$              ;IF LOADED OK THEN CONTINUE
10097 026660 ERRDF 1,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
10098 026660 104455 TRAP C$ERRDF
10099 026662 000001 .WORD 1
10100 026664 000000 .WORD 0
10101 026666 005304 .WORD S0EROR
10102 026670 CKLOOP
10103 026670 104406 TRAP C$CLP1
10104
10105 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10106 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10107
10108 026672 004737 012212 1$: JSR PC,SLCTTE          ;SELECT TARGET EMULATOR MODULE

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10109
10110 ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL 'BRKRES L'
10111 ;BY TOGGING ADAL REGISTER BIT 0. ADAL10 H AND ADAL9 H SET TO ONES WILL
10112 ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS. PULSING
10113 ;THE SIGNAL 'BRKRES L' VIA ADALO H WILL CLEAR THE BREAK LOGIC ON THE
10114 ;TARGET EMULATOR MODULE. ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
10115 ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL 'CKAI H' TO BE PULSED VIA THE
10116 ;THE SIGNAL 'RASP L' LATER ON IN THIS TEST. ADAL REGISTER BIT 4 ON A
10117 ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
10118 ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
10119
10120 026676 012737 043020 002334 MOV #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
10121 026704 004737 012764 JSR PC,BRKRES ;SET BITS 14, 10 + 9 AND TOGGLE ADALO H
10122
10123 ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
10124 ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
10125 ;REGISTER 6.
10126
10127 026710 004537 012232 JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
10128 026714 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
10129
10130 ;SET HDAL REGISTER BITS 9,4,3 + 2 TO A ONE AND HDAL BITS 14 AND 11 TO A
10131 ;ZERO. HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
10132 ;AND CONTROL SIGNALS. HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
10133 ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS. HDAL REGISTER
10134 ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
10135 ;HDAL REGISTER BITS 4 AND 3 SET TO ONES WILL SET THE SIGNALS XR/WLB H
10136 ;AND XR/WHB H TO THE HIGH STATE. THESE SIGNALS WILL CAUSE THE SIGNAL
10137 ;'REAT H' TO BE ASSERTED HIGH LATER IN THIS TEST WHEN THE SIGNALS XRAS H
10138 ;AND XCAS H ARE ASSERTED HIGH.
10139
10140 026716 012737 001034 002346 MOV #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SET HDAL BITS 9,4,3 + 2 TO ONES
10141 026724 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK HDAL REGISTER
10142 026730 001405 BEQ 2$ ;IF LOADED OK THEN CONTINUE
10143 026732 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
10144 026732 104455 TRAP C$ERDF
10145 026734 000014 .WORD 12
10146 026736 003754 .WORD HDALRG
10147 026740 006730 .WORD T06ERR
10148 026742 CKLOOP
10149 026742 10440L TRAP C$CLP1
10150
10151 ;PULSE THE SIGNAL 'INVD L' BY SETTING AND CLEARING VDAL2 H IN CONTROL
10152 ;REGISTER 4. PULSING THE SIGNAL 'INVD L' WILL INITIALIZE ALL THE
10153 ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L'.
10154
10155 026744 005037 002340 2$: CLR T4LOAD ;SETUP TO CLEAR ALL OTHER R/W BITS
10156 026750 004737 012704 JSR PC,CLRPSM ;PULSE INVD L VIA VDAL2 H
10157
10158 ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4. ON
10159 ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
10160 ;BE WRITTEN OR READ.
10161
10162 026754 004537 012232 JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
10163 026760 000004 .WORD MODE ;SELECT THE MODE REGISTER
10164

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10221 027064 ERRDF 12,ADDRRG,T06ERR ;DIAGNOSTIC ADDRESS REGISTER ERROR
10222 027064 104455 TRAP C$ERDF
10223 027066 000014 .WORD 12
10224 027070 004142 .WORD ADDR RG
10225 027072 006730 .WORD T06ERR
10226 027074 CKLOOP
10227 027074 104406 TRAP C$CLP1
10228
10229 ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
10230 ;CHANGES OCCURED DURING THE PAST SEQUENCES.
10231
10232 027076 004737 011176 5$: JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
10233 027102 001405 BEQ 6$ ;IF NO CHANGES THEN CONTINUE
10234 027104 ERRDF 11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
10235 027104 104455 TRAP C$ERDF
10236 027106 000013 .WORD 11
10237 027110 003706 .WORD VDALRG
10238 027112 006714 .WORD T4EROR
10239 027114 CKLOOP
10240 027114 104406 TRAP C$CLP1
10241
10242 ;RE-SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE
10243 ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
10244 ;CONTROL REGISTER 6.
10245
10246 027116 004537 012232 6$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
10247 027122 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
10248
10249 027124 012737 001034 002346 MOV #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;BITS THAT WERE PREVIOUSLY LOADED
10250
10251 ;PERFORM A T-11 TIMING CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE:
10252 ; 1. SET XRAS H AND PRAS H TO THE HIGH STATE
10253 ; 2. SET Y_AS H AND PCAS H TO THE HIGH STATE
10254 ; 3. SET XPI L AND PPI L TO THE LOW STATE
10255 ; 4. SET XCAS H AND PCAS H TO THE LOW STATE
10256 ; 5. SET XPI L AND PPI L TO THE HIGH STATE
10257 ; 6. SET XRAS H AND PRAS H TO THE LOW STATE
10258 ;WHEN PRAS H IS SET HIGH, THE SYSTEM ADDRESS BUS, WHICH CONTAINS THE
10259 ;TARGET EMULATORS DIAGNOSTIC ADDRESS REGISTER DATA, WILL BE CLOCKED INTO
10260 ;THE MEMORY SIMULATORS SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.
10261 ;WHEN XRAS H AND XCAS H ARE ASSERTED HIGH, THE TARGET EMULATOR SIGNALS
10262 ;REAT H AND READ H WILL BE ASSERTED HIGH. THE SIGNAL READ H WILL ATEMPT
10263 ;TO READ DATA FROM THE MEMORY SIMULATOR RAM. HOWEVER, IN THIS TEST, THE
10264 ;MAP PROTECT RAM IS SETUP TO INHIBIT READS AND WRITES TO THE ADDRESS
10265 ;SELECTED (10000). THEREFORE, A READ VIOLATION SHOULD OCCUR THUS CAUSING
10266 ;THE SIGNAL MSBRK H TO BE ASSERTED HIGH. THE READ VIOLATION FLIP-FLOP
10267 ;WILL BE CLOCKED VIA THE SIGNAL RDS H. THE SIGNAL RDS H WILL BE ASSERTED
10268 ;HIGH WHEN CTS H IS ASSERTED HIGH AND THE SIGNAL READ H GOES FROM A LOW
10269 ;TO A HIGH STATE. THE SIGNAL MSBRK H WILL NOT BE CLOCKED INTO THE TARGET
10270 ;EMULATORS MEMBRK FLIP-FLOP UNTIL THE SIGNAL XRAS H IS PULSED AGAIN.
10271
10272 027132 004737 012276 JSR PC,XRASH ;SET XRAS H AND PRAS H TO HIGH STATE
10273 027136 004737 012402 JSR PC,XCASH ;SET XCAS H AND PCAS H TO HIGH STATE
10274 027142 004737 012506 JSR PC,XPIH ;SET XPI L AND PPI L TO LOW STATE
10275 027146 004737 012434 JSR PC,XCASL ;SET XCAS H AND PCAS H TO LOW STATE
10276 027152 004737 012540 JSR PC,XPIL ;SET XPI L AND PPI L TO HIGH STATE

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10277 027156 004737 012330      JSR      PC,XRASL                ;SET XRAS H AND PRAS H TO LOW STATE
10278
10279                          ;READ TARGET EMULATORS GDAL REGISTER TO CHECK THAT NO CHANGES HAVE
10280                          ;OCCURED AS A RESULT OF THE ABOVE TIMING SEQUENCE. THE SIGNAL MEMBRK H
10281                          ;SHOULD BE ASSERTED LOW UNTIL A PULSE IS ISSUED ON THE SIGNAL XRAS H
10282                          ;AGAIN.
10283
10284 027162 004737 011112      JSR      PC,READTO              ;READ AND CHECK GDAL REGISTER
10285 027166 001405      BEQ      7$                    ;IF DATA OK THEN CONTINUE
10286 027170                      ERRDF   9,GDALRG,TOEROR          ;GDAL REGISTER NOT EQUAL EXPECTED
10287 027170 104455      TRAP    C$ERDF
10288 027172 000011      .WORD   9
10289 027174 003636      .WORD   GDALRG
10290 027176 006664      .WORD   TOEROR
10291 027200
10292 027200 104406      CKLOOP
10293                          TRAP    C$CLP1
10294
10295                          ;READ VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H IS ASSERTED HIGH
10296                          ;AS A RESULT OF THE SIGNALS CYCLE L, ENEDC H, PSM L, AND SOP L BEING
10297                          ;ASSERTED TO THE HIGH STATE.
10298 027202 052737 000020 002342 7$:  BIS      #VDAL4,T4GOOD          ;EXPECT EDEOC H TO BE A ONE
10299 027210 004737 011176      JSR      PC,READT4              ;READ AND CHECK VDAL REGISTER
10300 027214 001405      BEQ      8$                    ;IF OK THEN CONTINUE
10301 027216                      ERRDF   11,VDALRG,T4EROR          ;VDAL REGISTER NOT EQUAL EXPECTED
10302 027216 104455      TRAP    C$ERDF
10303 027220 000013      .WORD   11
10304 027222 003706      .WORD   VDALRG
10305 027224 006714      .WORD   T4EROR
10306 027226
10307 027226 104406      CKLOOP
10308                          TRAP    C$CLP1
10309
10310                          ;SELECT MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10311                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10312 027230 004737 011246      JSR      PC,SLCTMS              ;SELECT THE MEMORY SIMULATOR MODULE
10313
10314                          ;READ CONTROL REGISTER 4 BITS MSAD 15:0 TO CHECK THAT THE TARGET EMULATORS
10315                          ;DIAGNOSTIC ADDRESS REGISTER, WHICH WAS ENABLED TO THE SYSTEM ADDRESS
10316                          ;BUS, WAS CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS BUS LATCHES.
10317                          ;THE ADDRESS READ SHOULD BE EQUAL TO 10000.
10318
10319 027234 012737 100000 002254      MOV      #MSAD15,S4LOAD          ;SETUP EXPECTED ADDRESS FOR COMPARE
10320 027242 004737 010612      JSR      PC,READS4              ;READ AND CHECK MSAD BITS 15:0
10321 027246 001405      BEQ      9$                    ;IF ADDRESS OK THEN CONTINUE
10322 027250                      ERRDF   3,TEMSAD,S04ERR          ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
10323 027250 104455      TRAP    C$ERDF
10324 027252 000003      .WORD   3
10325 027254 002532      .WORD   TEMSAD
10326 027256 005404      .WORD   S04ERR
10327 027260
10328 027260 104406      CKLOOP
10329                          TRAP    C$CLP1
10330
10331                          ;READ AND CHECK CONTROL REGISTER 2 BITS. MSAD16 H AND MSAD17 H SHOULD
10332                          ;BE READ AS ZEROES AS A RESULT OF DATA LOADED INTO THE TARGET EMULATOR
10333                          ;MODULE. THE SIGNALS MSEL0 H AND MSEL1 H WILL BE IGNORED BECAUSE THESE

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10333 ;SIGNALS ARE TRI-STATED AS A RESULT OF THE SIGNAL CTS H BEING ASSERTED
10334 ;HIGH. THE SIGNALS ESR H AND MSBRK H SHOULD BE READ AS ONES. THE SIGNAL
10335 ;MSBRK H SHOULD BE A ONE AS A RESULT OF TRYING TO READ ADDRESS 10000 WHICH
10336 ;WAS MAPPED TO INHIBIT READS AND WRITES. THE RDV FLIP-FLOP SHOULD BE
10337 ;CLEARED THUS CAUSING THE SIGNAL BRK L TO BE ASSERTED LOW WHICH WILL
10338 ;CAUSE THE SIGNAL MSBRK H TO BE ASSERTED HIGH.
10339
10340 027262 012737 177414 002250 9$: MOV #177414,S2MASK ;SETUP TO IGNORE UNWANTED BITS
10341 027270 005037 002244 CLR S2LOAD ;SETUP VALUES FOR R/W BITS
10342 027274 012737 000240 002246 MOV #ESRH!MSBRKH,S2GOOD ;EXPECT ESR H AND MSBRK H TO BE ONES
10343 027302 004737 010560 JSR PC,READS2 ;READ AND CHECK CONTROL REGISTER 2
10344 027306 001405 BEQ 10$ ;IF DATA OK THEN CONTINUE
10345 027310 ERRDF 2,S2EROR ;CONTROL REGISTER 2 NOT EQUAL EXPECTED
10346 027310 104455 TRAP C$ERDF
10347 027312 000002 .WORD 2
10348 027314 000000 .WORD 0
10349 027316 005320 .WORD S2EROR
10350 027320 CKLOOP
10351 027320 104406 TRAP C$CLP1
10352
10353 ;READ CONTROL REGISTER 0 TO CHECK THAT THE RDV F/F IS SET TO A ONE
10354
10355 027322 052737 000020 002236 10$: BIS #RDVH,S0GOOD ;EXPECT RDV FLIP-FLOP TO BE A ONE
10356 027330 004737 010520 JSR PC,READS0 ;READ AND CHECK CONTROL REGISTER 0
10357 027334 001405 BEQ 11$ ;IF OK THEN CONTINUE
10358 027336 ERRDF 1,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
10359 027336 104455 TRAP C$ERDF
10360 027340 000001 .WORD 1
10361 027342 000000 .WORD 0
10362 027344 005304 .WORD S0EROR
10363 027346 CKLOOP
10364 027346 104406 TRAP C$CLP1
10365
10366 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10367 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10368
10369 027350 004737 012212 11$: JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE
10370
10371 ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL REGISTER BIT 12.
10372 ;WHEN XRAS H IS PULSED, THE SIGNAL MSBRK H FROM THE MEMORY SIMULATOR
10373 ;MODULE, WHICH IS HIGH, SHOULD BE CLOCKED INTO THE MEMBRK FLIP-FLOP THUS
10374 ;SETTING THE SIGNAL MEMBRK H TO THE HIGH STATE
10375
10376 027354 004737 012264 JSR PC,XRAS ;GO PULSE XRAS H VIA HDAL12 H
10377
10378 ;READ GDAL REGISTER TO CHECK THAT THE SIGNAL MEMBRK H IS ASSERTED HIGH
10379 ;AS A RESULT OF MSBRK H BEING HIGH AND A PULSE ON THE SIGNAL XRAS H.
10380 ;THE MEMBRK FLIP-FLOP SHOULD NOW BE SET TO A ONE.
10381
10382 027360 052737 000040 002326 BIS #MEMBRK,TOGOOD ;EXPECT MEMBRK H TO BE A ONE
10383 027366 004737 011112 JSR PC,READT0 ;READ AND CHECK GDAL REGISTER
10384 027372 001405 BEQ 12$ ;IF OK THEN CONTINUE
10385 027374 ERRDF 9,GDALRG,TOEROR ;MEMBRK FLIP-FLOP PROBABLY NOT SET
10386 027374 104455 TRAP C$ERDF
10387 027376 000011 .WORD 9
10388 027400 003636 .WORD GDALRG
  
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10389 027402 006664 .WORD TOEROR
10390 027404 CKLOOP
10391 027404 104406 TRAP C$CLP1
10392
10393 ;READ VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H IS ASSERTED LOW
10394 ;WHEN MEMBRK H IS ASSERTED HIGH AND SOP L IS ASSERTED LOW.
10395
10396 027406 042737 000020 002342 12$: BIC #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE A 0
10397 027414 004757 011176 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
10398 027420 001405 BEQ 13$ ;IF OK THEN CONTINUE
10399 027422 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
10400 027422 104455 TRAP C$ERDF
10401 027424 000013 .WORD 11
10402 027426 003706 .WORD VDALRG
10403 027430 006714 .WORD T4EROR
10404 027432 CKLOOP
10405 027432 104406 TRAP C$CLP1
10406
10407 ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10408 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10409
10410 027434 004737 011246 13$: JSR PC,SLCTMS ;SELECT THE MEMORY SIMULATOR MODULE
10411
10412 ;TO CHECK THAT THE MEMBRK FLIP-FLOP ON THE TARGET EMULATOR MODULE ONCE
10413 ;SET WILL REMAIN SET UNTIL CLEARED BY BRKRES L, THE PROGRAM WILL PRESET
10414 ;THE RDV AND WRV FLIP-FLOPS BY PULSING THE SIGNAL RST H THUS SETTING THE
10415 ;SIGNAL MSBRK H TO THE LOW STATE.
10416
10417 027440 004737 011266 JSR PC,MSRSTH ;GO PULSE RST H TO PRESET WRV + RDV F/F'S
10418
10419 ;READ CONTROL REGISTER 2 TO CHECK THAT THE SIGNAL MSBRK H WENT TO A
10420 ;ZERO AS A RESULT OF PULSING RST H.
10421
10422 027444 042737 000200 002246 BIC #MSBRKH,S2GOOD ;EXPECT MSBRK H TO BE A ZERO
10423 027452 004737 010560 JSR PC,READS2 ;READ AND CHECK CONTROL REGISTER 2
10424 027456 001405 BEQ 14$ ;IF OK THEN CONTINUE
10425 027460 ER.DF 2,S2EROR ;MSBRK H PROBABLY NOT 0 AFTER RST H
10426 027460 104455 TRAP C$ERDF
10427 027462 000002 .WORD 2
10428 027464 000000 .WORD 0
10429 027466 005320 .WORD S2EROR
10430 027470 CKLOOP
10431 027470 104406 TRAP C$CLP1
10432
10433 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10434 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10435
10436 027472 004737 012212 14$: JSR PC,SLCTTE ;SELECT TARGET EMULATOR MODULE
10437
10438 ;WITH MSBRK H ASSERTED LOW AND MEMBRK H ASSERTED HIGH, PULSE XRAS H
10439 ;TO CHECK THAT THE MEMBRK FLIP-FLOP WILL REMAIN LATCHED TO THE ONE
10440 ;STATE.
10441
10442 027476 004737 012254 JSR PC,XRAS ;PULSE XRAS H VIA HDAL12 H
10443
10444 ;READ CONTROL REGISTER 0 TO CHECK THAT THE SIGNAL MEMBRK H IS STILL

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10445 ;ASSERTED HIGH EVEN THOUGH MSBRK H IS LOW AND A PULSE WAS ISSUED ON THE
10446 ;SIGNAL XRAS H. THE MEMBRK FLIP-FLOP SHOULD REMAIN LATHCED TO A ONE
10447 ;UNTIL CLEARED BY A PULSE ON THE SIGNAL BRKRES L.
10448
10449 027502 004737 011112 JSR PC,READTO ;READ AND CHECK GDAL REGISTER
10450 027506 001405 BEQ 15$ ;IF NO CHANGE THEN CONTINUE
10451 027510 ERRDF 9,GDALRG,TOEROR ;GDAL REGISTER NOT EQUAL EXPECTED
10452 027510 104455 TRAP C$ERDF
10453 027512 000011 .WORD 9
10454 027514 003636 .WORD GDALRG
10455 027516 006664 .WORD TOEROR
10456 027520 CKLOOP
10457 027520 104406 TRAP C$CLP1
10458
10459 ;GO PULSE THE SIGNAL BRKRES L BY SETTING AND CLEARING ADAL REGISTER BIT
10460 ;ZERO. A PULSE ON THE SIGNAL BRKRES L WILL CAUSE THE MEMBRK FLIP-FLOP
10461 ;TO BE CLEARED.
10462
10463 027522 004737 012764 15$: JSR PC,BRKRES ;GO PULSE BRKRES L VIA ADALO H
10464
10465 ;READ GDAL REGISTER TO CHECK THAT BRKRES L CLEARED MEMBRK FLIP-FLOP
10466
10467 027526 042737 000040 002326 BIC #MEMBRK,TOGOOD ;EXPECT MEMBRK H TO BE A ZERO
10468 027534 004737 011112 JSR PC,READTO ;READ AND CHECK GDAL REGISTER
10469 027540 001405 BEQ 16$ ;IF OK THEN CONTINUE
10470 027542 ERRDF 9,GDALRG,TOEROR ;MEMBRK F/F PROBABLY NOT 0 AFTER RST H
10471 027542 104455 TRAP C$ERDF
10472 027544 000011 .WORD 9
10473 027546 003636 .WORD GDALRG
10474 027550 006664 .WORD TOEROR
10475 027552 CKLOOP
10476 027552 104406 TRAP C$CLP1
10477
10478 ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL REGISTER BIT 7
10479 ;TO A ONE AND CHECK THAT THE SIGNAL EDEOC H IS NOW SET TO A ONE AS A
10480 ;RESULT OF THE SIGNAL SOP L RETURNING TO THE HIGH STATE AFTER THE SIGNAL
10481 ;MEMBRK H WENT TO THE LOW STATE.
10482
10483 027554 012737 000200 002340 16$: MOV #VDAL7,T4LOAD ;SETUP BIT TO BE LOADED
10484 027562 013737 002340 002342 MOV T4LOAD,T4GOOD ;COPY DATA LOADED TO EXPECTED
10485 027570 052737 000020 002342 BIS #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE A ONE
10486 027576 004737 011170 JSR PC,LDRD4T ;LOAD, READ AND CHECK VDAL REGISTER
10487 027602 001405 BEQ 17$ ;IF VDAL REGISTER OK THEN CONTINUE
10488 027604 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
10489 027604 104455 TRAP C$ERDF
10490 027606 000013 .WORD 11
10491 027610 003706 .WORD VDALRG
10492 027612 006714 .WORD T4EROR
10493 027614 CKLOOP
10494 027614 104406 TRAP C$CLP1
10495
10496 ;TOGGLE THE SIGNALS XRAS AND PRAS BY SETTING AND CLEARING HDAL12 H.
10497 ;SETTING THE SIGNAL XRAS H TO THE HIGH STATE WILL CLOCK THE EDFET, BTFET
10498 ;AND PAUSE MODE FLIP-FLOPS TO A ONE THUS SETTING THE SIGNAL EDFET H TO
10499 ;THE HIGH STATE, AND THE SIGNALS BTFET L AND PAUSE L TO THE LOW STATES.
10500 ;SETTING PRAS H TO THE HIGH STATE WILL SET THE SIGNAL ADVAL H TO THE

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10501 ;HIGH STATE WHICH WILL CAUSE THE SYSTEM ADDRESS BUS TO BE CLOCKED INTO
10502 ;THE MEMORY SIMULATOR'S SYSTEM ADDRESS BUS LATCHES. THE ADDRESS CLOCKED
10503 ;WILL BE 100000 WHICH IS MAPPED ON THE MEMORY SIMULATOR MODULE TO INHIBIT
10504 ;READS AND WRITES. THEREFORE, THE MEMORY SIMULATOR SIGNAL RDE L SHOULD
10505 ;BE ASSERTED HIGH. AS A RESULT OF RDE L BEING ASSERTED HIGH, THE EDFET
10506 ;FLIP-FLOP BEING SET TO A ONE, THE PAUSE STATE WORKING FLIP-FLOP BEING
10507 ;A ZERO AND A PULSE BEING ISSUED ON THE SIGNAL XRASD H, THE MEMBRK FLIP-
10508 ;FLOP WILL BE DIRECT SET TO A ONE THUS CAUSING THE SIGNALS MEMBRK H
10509 ;AND PSMW H TO BE ASSERTED HIGH. WHEN XRAS L IS RETURNED TO THE HIGH
10510 ;STATE AFTER HAVING BEEN SET LOW, THE STATE OF MEMBRK H WILL BE CLOCKED
10511 ;INTO THE INTERRUPT BREAK FLIP-FLOP THUS CAUSING THAT FLIP-FLOP TO BE
10512 ;SET TO A ONE.
10513
10514 027616 004737 012264 17$: JSR PC,XRAS ;GO PULSE XRAS H AND PRAS H VIA HDAL12
10515
10516 ;READ GDAL REGISTER TO CHECK THAT MEMBRK FLIP-FLOP WAS DIRECT SET TO
10517 ;A ONE BY A PULSE ON XRASD H AND THE FOLLOWING SIGNALS BEING ASSERTED
10518 ;HIGH: RDE L, EDFET H, AND PSMW L.
10519
10520 027622 052737 000C40 002326 BIS #MEMBRK,TOGOOD ;EXPECT MEMBRK F/F TO BE SET
10521 027630 004737 011112 JSR PC,READTO ;READ AND CHECK VDAL REGISTER
10522 027634 001405 BEQ 18$ ;IF OK THEN CONTINUE
10523 027636 ERRDF 9,GDALRG,TOEROR ;MEMBRK F/F PROBABLY NOT DIRECT SET TO 1
10524 027636 104455 TRAP C$ERDF
10525 027640 000011 .WORD 9
10526 027642 003636 .WORD GDALRG
10527 027644 006664 .WORD TOEROR
10528 027646 CKLOOP
10529 027646 104406 TRAP C$CLP1
10530
10531 ;READ THE VDAL REGISTER AND CHECK THAT THE PAUSE STATE WORKING FLIP-
10532 ;FLOP WAS SET TO A ONE VIA EDFET H AND SOP H. THE SIGNAL SOP H IS SET
10533 ;HIGH VIA MEMBRK H. CHECK EDEOC H TO BE A ZERO AS A RESULT OF SOP L
10534 ;BEING ASSERTED LOW. BTS1 H WILL BE A ONE AS A RESULT OF THE BTFET
10535 ;FLIP-FLOP BEING SET TO A ONE WHEN XRAS H WAS PULSED.
10536
10537 027650 042737 000020 002342 18$: BIC #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE A ZERO
10538 027656 052737 001040 002342 BIS #VDAL9,VDAL5,T4GOOD ;EXPECT PSMW H AND BTS1 H TO BE HIGH
10539 027664 004737 011176 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
10540 027670 001405 BEQ 19$ ;IF OK THEN CONTINUE
10541 027672 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
10542 027672 104455 TRAP C$ERDF
10543 027674 000013 .WORD 11
10544 027676 003706 .WORD VDALRG
10545 027700 006714 .WORD T4EROR
10546 027702 CKLOOP
10547 027702 104406 TRAP C$CLP1
10548
10549 ;SETUP TARGET EMULATOR INTERRUPT VECTOR TO THE VECTOR SPECIFIED BY
10550 ;THE USER AT PROGRAM START TIME. THE CPU PRIORITY LEVEL WILL BE RESET
10551 ;TO PRIORITY LEVEL 7 WHEN AN INTERRUPT OCCURS.
10552
10553 027704 19$: SETVEC TEVECT,#INTSRV,#PRI07 ;SETUP INTERRUPT VECTOR
10554 027704 012746 000340 MOV #PRI07,-(SP)
10555 027710 012746 013044 MOV #INTSRV,-(SP)
10556 027714 013746 002214 MOV TEVECT,-(SP)

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10557	027720	012746	000003		MOV	#3, -(SP)	
10558	027724	104437			TRAP	C\$SVEC	
10559	027726	062706	000010		ADD	#10, SP	
10560	027732	005002			CLR	R2	;CLEAR SOFTWARE INTERRUPT FLAG
10561							
10562							;SET TARGET EMULATORS INTERRUPT ENABLE BIT TO A ONE BY SETTING GDAL
10563							;REGISTER BIT 3 TO A ONE.
10564							
10565	027734	052737	000010	002324	BIS	#GDAL3, TOLOAD	;SETUP BIT TO BE LOADED TO SET INT ENA
10566	027742	052737	000010	002326	BIS	#GDAL3, TOGOOD	;SETUP BIT TO BE EXPECTED ON READ
10567	027750	004737	011104		JSR	PC, LDRDOT	;LOAD, READ AND CHECK GDAL REGISTER
10568	027754	001405			BEQ	20\$;IF LOADED OK THEN CONTINUE
10569	027756				ERRDF	9, GDALRG, TOEROR	;GDAL REGISTER NOT EQUAL EXPECTED
10570	027756	104455			TRAP	C\$ERDF	
10571	027760	000011			.WORD	9	
10572	027762	003636			.WORD	GDALRG	
10573	027764	006664			.WORD	TOEROR	
10574	027766				CKLOOP		
10575	027766	104406			TRAP	C\$CLP1	
10576							
10577							;LOWER THE CPU PRIORITY LEVEL TO ZERO. AN INTERRUPT SHOULD OCCUR AS
10578							;A RESULT OF THE BREAK INTERRUPT FLIP-FLOP BEING SET AND THE TARGET
10579							;EMULATORS INTERRUPT ENABLE BIT BEING SET TO A ONE.
10580							
10581	027770				20\$:	SETPRI	#PRI00 ;LOWER THE CPU PRIORITY LEVEL
10582	027770	012700	000000		MOV	#PRI00, P0	
10583	027774	104441			TRAP	C\$SPRI	
10584							
10585							;CHECK THAT AN INTERRUPT OCCURED AS A RESULT OF THE CPU PRIORITY LEVEL
10586							;BEING SET TO ZERO, THE BREAK INTERRUPT FLIP-FLOP BEING SET TO A ONE,
10587							;AND THE TARGET EMULATOR'S INTERRUPT ENBALE BIT BEING SET TO A ONE.
10588							;THE BREAK INTERRUPT FLIP-FLOP WAS SET TO A ONE AS A RESULT OF MEMBRK H
10589							;BEING ASSERTED HIGH AND A PULSE ON THE SIGNAL XRAS L.
10590							
10591	027776	000240			NOP		;DO A DUMMY INSTRUCTION TO ALLOW INTERRUPT
10592	030000	005702			TST	R2	;CHECK IF AN INTERRUPT OCCURED
10593	030002	001005			BNE	21\$;IF YES THEN CONTINUE
10594	030004				ERRDF	9, NOINT, TOEROR	;FAILED TO INTERRUPT WITH MEMBRK H SET
10595	030004	104455			TRAP	C\$ERDF	
10596	030006	000011			.WORD	9	
10597	030010	004507			.WORD	NOINT	
10598	030012	006664			.WORD	TOEROR	
10599	030014				CKLOOP		
10600	030014	104406			TRAP	C\$CLP1	
10601							
10602							;AT THIS POINT IN TIME THE CPU PRIORITY LEVEL IS AT 7 AS A RESULT OF
10603							;AN INTERRUPT. CHECK THE PREVIOUS GDAL REGISTER AGAINST THE GDAL
10604							;REGISTER READ IN THE INTERRUPT SERVICE ROUTINE.
10605							
10606	030016	023737	002326	002332	21\$:	CMP	TOGOOD, TOREAD ;CHECK PREVIOUS AGAINST READ FROM INTERRUPT
10607	030024	001405			BEQ	22\$;IF THE SAME THEN CONTINUE
10608	030026				ERRDF	9, GDALRG, TOEROR	;GDAL REG CHANGED AFTER AN INTERRUPT
10609	030026	104455			TRAP	C\$ERDF	
10610	030030	000011			.WORD	9	
10611	030032	003636			.WORD	GDALRG	
10612	030034	006664			.WORD	TOEROR	


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10613 030036          CKLOOP
10614 030036 104406   TRAP   C$CLP1
10615
10616                ;ISSUE A PULSE ON THE SIGNAL BRKRES L TO CLEAR THE MEMBRK FLIP-FLOP AND
10617                ;THE BREAK INTERRUPT FLIP-FLOP.
10618
10619 030040 004737 012764 22$: JSR   PC, BRKRES          ;GO PULSE BRKRES L VIA ADALO H
10620
10621                ;READ THE GDAL REGISTER TO CHECK THAT THE MEMBRK FLIP-FLOP WAS CLEARED
10622                ;BY A PULSE ON THE SIGNAL BRKRES L.
10623
10624 030044 042737 000040 002326 BIC   #MEMBRK, TOGOOD      ;EXPECT MEMBRK H TO BE A ZERO
10625 030052 004737 011112          JSR   PC, READTO          ;READ AND CHECK GDAL REGISTER
10626 030056 001405          BEQ   23$                ;IF OK THEN CONTINUE
10627 030060          ERRDF  9, GDALRG, TOEROR      ;GDAL REGISTER NOT EQUAL EXPECTED
10628 030060 104455          TRAP  C$ENDF
10629 030062 000011          .WORD 9
10630 030064 003636          .WORD GDALRG
10631 030066 006664          .WORD TOEROR
10632 030070
10633 030070 104406   CKLOOP
10634                TRAP   C$CLP1
10635
10636                ;ISSUE A PULSE ON THE SIGNAL INVD L TO INITIALIZE ALL OTHER FLIP-FLOPS
10637                ;NO CLEARED BY THE SIGNAL BRKRES L.
10638 030072 005037 002340 23$: CLR   T4LOAD          ;SETUP TO CLEAR ALL VDAL R/W BITS
10639 030076 004737 012704          JSR   PC, CLRPSM        ;PULSE INVD L VIA VDAL2 H
10640
10641 030102          CLRVEC  TEVECT          ;RELEASE TARGET EMULATOR VECTOR
10642 030102 013700 002214          MOV   TEVECT, R0
10643 030106 104436          TRAP  C$CVEC
10644
10645 030110          ENDSEG
10646 030110          10000$: TRAP  C$ESEG
10647 030110 104405
10648
10649 030112          ENDTST
10650 030112          L10045: TRAP  C$TST
10651 030112 104401
10652

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10709 ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
10710
10711 030136 004737 012010 JSR PC,MSRAM1 ;LOAD, READ AND CHECK MODULE SELECT RAM 1
10712
10713 ;SET THE SIGNAL "CTS H" TO A ONE IN CONTROL REGISTER 0. THIS WILL
10714 ;ENABLE THE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR LOGIC.
10715 ;IN THIS TEST, "CTS H" ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO
10716 ;THE MEMORY SIMULATOR MODULE AND THE MEMORY SIMULATOR RAM DATA ONTO THE
10717 ;SYSTEM BUS.
10718
10719 030142 052737 000002 002234 BIS #CTSH,SLOAD ;SETUP BIT TO BE LOADED
10720 030150 004737 010504 JSR PC,LDRDSO ;GO LOAD, READ AND CHECK CONTROL REG 2
10721 030154 001405 BEQ 1$ ;IF LOADED OK THEN CONTINUE
10722 030156 ERRDF 1,,SOEROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
10723 030156 104455 TRAP C$ERRDF
10724 030160 000001 .WORD 1
10725 030162 000000 .WORD 0
10726 030164 005304 .WORD SOEROR
10727 030166 CKLOOP
10728 030166 104406 TRAP C$CLP1
10729
10730 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10731 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10732
10733 030170 004737 012212 1$: JSR PC,SLCTTE ;SELECT TARGET EMULATOR MODULE
10734
10735 ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL "BRKRES L"
10736 ;BY TOGGING ADAL REGISTER BIT 0. ADAL10 H AND ADAL9 H SET TO ONES WILL
10737 ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS. PULSING
10738 ;THE SIGNAL "BRKRES L" VIA ADALO H WILL CLEAR THE BREAK LOGIC ON THE
10739 ;TARGET EMULATOR MODULE. ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
10740 ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL "CKAI H" TO BE PULSED VIA THE
10741 ;THE SIGNAL "RASP L" LATER ON IN THIS TEST. ADAL REGISTER BIT 4 ON A
10742 ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
10743 ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
10744
10745 030174 012737 043020 002334 MOV #ADAL14!ADAL10!ADAL9!ADAL4,TLOAD ;SETUP BITS TO BE LOADED
10746 030202 004737 012764 JSR PC,BRKRES ;SET BITS 14, 10 + 9 AND TOGGLE ADALO H
10747
10748 ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
10749 ;REG WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REG 6
10750
10751 030206 004537 012232 JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
10752 030212 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
10753
10754 ;SET HDAL REGISTER BITS 9 AND 2 TO A ONE AND HDAL BITS 14, 11, 4 + 3 TO A
10755 ;ZERO. HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
10756 ;AND CONTROL SIGNALS. HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
10757 ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS. HDAL REGISTER
10758 ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
10759 ;HDAL REGISTER BITS 4 AND 3 SET TO ZEROES WILL SET THE SIGNALS XR/WLB L
10760 ;AND XR/WHBL TO THE HIGH STATE. THESE SIGNALS WILL CAUSE THE SIGNALS
10761 ;"WT HB H AND WT LB H" TO BE ASSERTED HIGH LATER IN THIS TEST WHEN THE
10762 ;SIGNAL XPI H IS SET TO THE HIGH STATE FROM THE LOW STATE.
10763
10764 030214 012737 001004 002346 MOV #HDAL9!HDAL2,T6LOAD ;SET HDAL BITS 9 AND 2 TO ONES

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10765 030222 004737 011214      JSR      PC,LDRDT6      ;GO LOAD, READ AND CHECK HDAL REGISTER
10766 030226 001405              BEQ      2$             ;IF LOADED OK THEN CONTINUE
10767 030230                    ERRDF    12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
10768 030230 104455              TRAP    C$ERDF
10769 030232 000014              .WORD   12
10770 030234 003754              .WORD   HDALRG
10771 030236 006730              .WORD   T06ERR
10772 030240                    CKLOOP
10773 030240 104406              TRAP    C$CLP1
10774
10775                          ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
10776                          ;REGISTER 4. PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
10777                          ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L'.
10778
10779 030242 005037 002340      2$:   CLR      T4LOAD      ;SETUP TO CLEAR ALL OTHER R/W BITS
10780 030246 004737 012704      JSR      PC,CLRPSM     ;PULSE INVD L VIA VDAL2 H
10781
10782                          ;SELECT MODE REG BY SETTING GDAL REGISTER BITS 2:0 TO A 4. ON A WRITE OR
10783                          ;READ COMMAND TO CONTROL REG 6, THE MODE REG WILL BE WRITTEN OR READ
10784
10785 030252 004537 012232      JSR      R5,SELTERR   ;SELECT REGISTER SPECIFIED BY NEXT WORD
10786 030256 000004              .WORD   MODE          ;SELECT THE MODE REGISTER
10787
10788                          ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
10789                          ;ZEROS. MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
10790
10791 030260 005037 002346      CLR      T6LOAD      ;SETUP TO CLEAR ALL MODE REGISTER BITS
10792 030264 004737 011214      JSR      PC,LDRDT6   ;GO LOAD, READ AND CHECK MODE REGISTER
10793 030270 001405              BEQ      3$           ;IF LOADED OK THEN CONTINUE
10794 030272                    ERRDF    12,MODREG,T06ERR ;MODE REGISTER NOT EQUAL EXPECTED
10795 030272 104455              TRAP    C$ERDF
10796 030274 000014              .WORD   12
10797 030276 004000              .WORD   MODREG
10798 030300 006730              .WORD   T06ERR
10799 030302                    CKLOOP
10800 030302 104406              TRAP    C$CLP1
10801
10802                          ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
10803                          ;TO A 2. THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
10804                          ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
10805                          ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
10806                          ;TER WILL BE ADDRESSED.
10807
10808 030304 004537 012232      3$:   JSR      R5,SELTERR   ;SELECT REGISTER SPECIFIED BY NEXT WORD
10809 030310 000002              .WORD   FDAL          ;SELECT EOAI AND FDAL REGISTER
10810
10811                          ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER. THE EOAI REGISTER WILL
10812                          ;BE LOADED AND CHECKED FOR ZEROES. THE FDAL REGISTER WILL BE LOADED AND
10813                          ;CHECKED FOR A DATA PATTERN OF ONE (FDALO H = 1).
10814
10815 030312 012737 000001 002346  MOV      #FDALO,T6LOAD ;SETUP EOAI AND FDAL REG DATA PATTERN
10816 030320 004737 011214      JSR      PC,LDRDT6   ;GO LOAD, READ AND CHECK EOAI + FDAL REG
10817 030324 001405              BEQ      4$           ;IF LOADED OK THEN CONTINUE
10818 030326                    ERRDF    12,EOAIFD,T06ERR ;EOAI OR FDAL REGISTER ERROR
10819 030326 104455              TRAP    C$ERDF
10820 030330 000014              .WORD   12

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10821 030332 004045      .WORD  EOAIFD
10822 030334 006730      .WORD  T06ERR
10823 030336          CKLOOP
10824 030336 104406      TRAP   C$CLP1
10825
10826      ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
10827      ;2:0 TO A 0. THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH A DATA
10828      ;PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6. THE DIAGNOSTIC ADDRESS
10829      ;REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER BIT 10
10830      ;BEING SET TO A ONE PREVIOUSLY. ON A READ COMMAND TO CONTROL REGISTER
10831      ;6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
10832
10833 030340 004537 012232 4$: JSR    R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
10834 030344 000000      .WORD  ADDRES      ;SELECT DIAG ADDRESS REG AND ADDRESS BUS
10835
10836      ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA PATTERN
10837      ;OF 100000. THIS WILL CAUSE MEMORY NOT MAPPED TO BE SELECTED LATER ON IN
10838      ;THIS TEST. ADDRESS BITS 17 AND 16 WERE SET TO A ZERO EARLIER IN THIS
10839      ;TEST VIA THE HDAL REGISTER.
10840
10841 030346 012737 100000 002346 MOV    #ADDR15,T6LOAD      ;SETUP DATA PATTERN OF 100000
10842 030354 004737 011214 JSR    PC,LDRDT6      ;LOAD, READ AND CHECK DIAG ADDRESS REG
10843 030360 001405 BEQ    5$      ;IF LOADED OK THEN CONTINUE
10844 030362 ERRDF 12,ADDRRG,T06ERR      ;DIAGNOSTIC ADDRESS REGISTER ERROR
10845 030362 104455 TRAP  C$ERDF
10846 030364 000014 .WORD  12
10847 030366 004142 .WORD  ADDR RG
10848 030370 006730 .WORD  T06ERR
10849 030372 CKLOOP
10850 030372 104406 TRAP  C$CLP1
10851
10852      ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
10853      ;CHANGES OCCURED DURING THE PAST SEQUENCES.
10854
10855 030374 004737 011176 5$: JSR    PC,READT4      ;READ AND CHECK VDAL REGISTER
10856 030400 001405 BEQ    6$      ;IF NO CHANGES THEN CONTINUE
10857 030402 ERRDF 11,VDALRG,T4EROR      ;VDAL OR PAUSE STATE MACHINE ERROR
10858 030402 104455 TRAP  C$ERDF
10859 030404 000013 .WORD  11
10860 030406 003706 .WORD  VDALRG
10861 030410 006714 .WORD  T4EROR
10862 030412 CKLOOP
10863 030412 104406 TRAP  C$CLP1
10864
10865      ;RE-SELECT THE HDAL REG BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL REG
10866      ;WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REG 6.
10867
10868 030414 004537 012232 6$: JSR    R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
10869 030420 000003 .WORD  HDAL      ;SELECT THE HDAL REGISTER
10870 030422 012737 001004 002346 MOV    #HDAL9!HDAL2,T6LOAD      ;BITS THAT WERE PREVIOUSLY LOADED
10871
10872      ;PERFORM A T-11 TIMING CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE:
10873      ; 1. SET XRAS H AND PRAS H TO THE HIGH STATE
10874      ; 2. SET XCAS H AND PCAS H TO THE HIGH STATE
10875      ; 3. SET XPI L AND PPI L TO THE LOW STATE
10876      ; 4. SET XCAS H AND PCAS H TO THE LOW STATE
  
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10877 ; 5. SET XPI L AND PPI L TO THE HIGH STATE
10878 ; 6. SET XRAS H AND PRAS H TO THE LOW STATE
10879 ; WHEN PRAS H IS SET HIGH, THE SYSTEM ADDRESS BUS, WHICH CONTAINS THE
10880 ; TARGET EMULATORS DIAGNOSTIC ADDRESS REGISTER DATA, WILL BE CLOCKED INTO
10881 ; THE MEMORY SIMULATORS SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.
10882 ; WHEN XPI H IS SET HIGH AND THE SIGNALS XR/WHB L AND XR/WLB L ARE
10883 ; ASSERTED HIGH, THE SIGNALS WT HB H AND WT LB H WILL BE SET TO THE HIGH
10884 ; STATE. THESE TWO SIGNALS WILL ATTEMPT TO WRITE DATA INTO THE MEMORY
10885 ; SIMULATOR MODULE'S RAMS. HOWEVER, THE ADDRESS UNDER TEST (100000) IS
10886 ; MAPPED TO INHIBIT READS AND WRITES, THEREFORE, THE MEMORY SIMULATOR'S
10887 ; WRV (WRITE VIOLATION) FLIP-FLOP SHOULD BE CLEARED VIA PULSES ON THE
10888 ; SIGNALS WRHB L AND WRLB L WHEN THE SIGNAL WRE H IS ASSERTED LOW. AS A
10889 ; RESULT OF THE WRV FLIP-FLOP BEING CLEARED, THE SIGNAL MSBRK H WILL BE
10890 ; ASSERTED HIGH VIA THE SIGNAL BRK L. THE SIGNAL MSBRK H WILL NOT BE
10891 ; CLOCKED INTO THE TARGET EMULATOR'S MEMBRK FLIP-FLOP UNTIL THE SIGNAL
10892 ; XRAS H IS PULSED ON THE TARGET EMULATOR MODULE.
10893
10894 030430 004737 012276 JSR PC,XRASH ;SET XRAS H AND PRAS H TO HIGH STATE
10895 030434 004737 012402 JSR PC,XCASH ;SET XCAS H AND PCAS H TO HIGH STATE
10896 030440 004737 012506 JSR PC,XPIH ;SET XPI L AND PPI L TO LOW STATE
10897 030444 004737 012434 JSR PC,XCASL ;SET XCAS H AND PCAS H TO LOW STATE
10898 030450 004737 012540 JSR PC,XPIL ;SET XPI L AND PPI L TO HIGH STATE
10899 030454 004737 012330 JSR PC,XRASL ;SET XRAS H AND PRAS H TO LOW STATE
10900
10901 ;READ TARGET EMULATORS GDAL REGISTER TO CHECK THAT NO CHANGES HAVE
10902 ; OCCURED AS A RESULT OF THE ABOVE TIMING SEQUENCE. THE SIGNAL MEMBRK H
10903 ; SHOULD BE ASSERTED LOW UNTIL A PULSE IS ISSUED ON THE SIGNAL XRAS H AGAIN.
10904
10905 030460 004737 011112 JSR PC,READTO ;READ AND CHECK GDAL REGISTER
10906 030464 001405 BEQ 7$ ;IF DATA OK THEN CONTINUE
10907 030466 ERRDF 9,GDALRG,TOEROR ;GDAL REGISTER NOT EQUAL EXPECTED
10908 030466 104455 TRAP C$ERDF
10909 030470 000011 .WORD 9
10910 030472 003636 .WORD GDALRG
10911 030474 006664 .WORD TOEROR
10912 030476 CKLOOP
10913 030476 104406 TRAP C$CLP1
10914
10915 ;READ VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H IS ASSERTED HIGH
10916 ; ASA RESULT OF THE SIGNALS CYCLE L, ENEDC H, PSM L, AND SOP L BEING
10917 ; ASSERTED TO THE HIGH STATE.
10918
10919 030500 052737 000020 002342 7$: BIS #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE A ONE
10920 030506 004737 011176 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
10921 030512 001405 BEQ 8$ ;IF OK THEN CONTINUE
10922 030514 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
10923 030514 104455 TRAP C$ERDF
10924 030516 000013 .WORD 11
10925 030520 003706 .WORD VDALRG
10926 030522 006714 .WORD T4EROR
10927 030524 CKLOOP
10928 030524 104406 TRAP C$CLP1
10929
10930 ;SELECT MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10931 ; REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10932

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10933 030526 004737 011246      8$: JSR PC,SLCTMS ;SELECT THE MEMORY SIMULATOR MODULE
10934
10935 ;READ CONTROL REGISTER 4 BITS MSAD 15:0 TO CHECK THAT THE TARGET EMULATORS
10936 ;DIAGNOSTIC ADDRESS REGISTER, WHICH WAS ENABLED TO THE SYSTEM ADDRESS
10937 ;BUS, WAS CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS BUS LATCHES.
10938 ;THE ADDRESS READ SHOULD BE EQUAL TO 10000.
10939
10940 030532 012737 100000 002254 MOV #MSAD15,S4LOAD ;SETUP EXPECTED ADDRESS FOR COMPARE
10941 030540 004737 010612 JSR PC,READS4 ;READ AND CHECK MSAD BITS 15:0
10942 030544 001405 BEQ 9$ ;IF ADDRESS OK THEN CONTINUE
10943 030546 ERRDF 3,TEMSAD,S04ERR ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
10944 030546 104455 TRAP C$ERRDF
10945 030550 000003 .WORD 3
10946 030552 002532 .WORD TEMSAD
10947 030554 005404 .WORD S04ERR
10948 030556 CKLOOP
10949 030556 104406 TRAP C$CLP1
10950
10951 ;READ AND CHECK CONTROL REGISTER 2 BITS. MSAD16 H AND MSAD17 H SHOULD
10952 ;BE READ AS ZEROES AS A RESULT OF DATA LOADED INTO THE TARGET EMULATOR
10953 ;MODULE. THE SIGNALS MSEL0 H AND MSEL1 H WILL BE IGNORED BECAUSE THESE
10954 ;SIGNALS ARE TRI-STATED AS A RESULT OF THE SIGNAL CTS H BEING ASSERTED
10955 ;HIGH. THE SIGNALS ESR H AND MSBRK H SHOULD BE READ AS ONES. THE SIGNAL
10956 ;MSBRK H SHOULD BE A ONE AS A RESULT OF TRYING TO WRITE ADDRESS 10000 WHICH
10957 ;WAS MAPPED TO INHIBIT READS AND WRITES. THE WRV FLIP-FLOP SHOULD BE
10958 ;CLEARED THUS CAUSING THE SIGNAL BRK L TO BE ASSERTED LOW WHICH WILL
10959 ;CAUSE THE SIGNAL MSBRK H TO BE ASSERTED HIGH.
10960
10961 030560 012737 177414 002250 9$: MOV #177414,S2MASK ;SETUP TO IGNORE UNWANTED BITS
10962 030566 005037 002244 CLR S2LOAD ;SETUP VALUES FOR R/W BITS
10963 030572 012737 000240 002246 MOV #ESRH!MSBRKH,S2GOOD ;EXPECT ESR H AND MSBRK H TO BE ONES
10964 030600 004737 010560 JSR PC,READS2 ;READ AND CHECK CONTROL REGISTER 2
10965 030604 001405 BEQ 10$ ;IF DATA OK THEN CONTINUE
10966 030606 ERRDF 2,,S2EROR ;CONTROL REGISTER 2 NOT EQUAL EPXETCED
10967 030606 104455 TRAP C$ERRDF
10968 030610 000002 .WORD 2
10969 030612 000000 .WORD 0
10970 030614 005320 .WORD S2EROR
10971 030616 CKLOOP
10972 030616 104406 TRAP C$CLP1
10973
10974 ;READ CONTROL REGISTER 0 TO CHECK THAT THE WRV F/F IS SET TO A ONE
10975
10976 030620 052737 000040 002236 10$: BIS #WRVH,S0GOOD ;EXPECT WRV FLIP-FLOP TO BE A ONE
10977 030626 004737 010520 JSR PC,READS0 ;READ AND CHECK CONTROL REGISTER 0
10978 030632 001405 BEQ 11$ ;IF OK THEN CONTINUE
10979 030634 ERRDF 1,S0EROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
10980 030634 104455 TRAP C$ERRDF
10981 030636 000001 .WORD 1
10982 030640 000000 .WORD 0
10983 030642 005304 .WORD S0EROR
10984 030644 CKLOOP
10985 030644 104406 TRAP C$CLP1
10986
10987 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10988 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.

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10989
10990 030646 004737 012212      11$: JSR    PC,SLCTTE                ;SELECT THE TARGET EMULATOR MODULE
10991
10992                               ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL REGISTER BIT 12.
10993                               ;WHEN XRAS H IS PULSED, THE SIGNAL MSBRK H FROM THE MEMORY SIMULATOR
10994                               ;MODULE, WHICH IS HIGH, SHOULD BE CLOCKED INTO THE MEMBRK FLIP-FLOP THUS
10995                               ;SETTING THE SIGNAL MEMBRK H TO THE HIGH STATE
10996
10997 030652 004737 012264      JSR    PC,XRAS                    ;GO PULSE XRAS H VIA HDAL12 H
10998
10999                               ;READ GDAL REGISTER TO CHECK THAT THE SIGNAL MEMBRK H IS ASSERTED HIGH
11000                               ;AS A RESULT OF MSBRK H BEING HIGH AND A PULSE ON THE SIGBAL XRAS H.
11001                               ;THE MEMBRK FLIP-FLOP SHOULD NOW BE SET TO A ONE.
11002
11003 030656 052737 000040 002326  BIS    #MEMBRK,TOGOOD            ;EXPECT MEMBRK H TO BE A ONE
11004 030664 004737 011112      JSR    PC,READT0                ;READ AND CHECK GDAL REGISTER
11005 030670 001405                BEQ    12$                      ;IF OK THEN CONTINUE
11006 030672                ERRDF  9,GDALRG,TOEROR          ;MEMBRK FLIP-FLOP PROBABLY NOT SET
11007 030672 104455                TRAP  C$ERRDF
11008 030674 000011                .WORD 9
11009 030676 003636                .WORD GDALRG
11010 030700 006664                .WORD TOEROR
11011 030702                CKLOOP
11012 030702 104406                TRAP  C$CLP1
11013
11014                               ;READ VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H IS ASSERTED LOW
11015                               ;WHEN MEMBRK H IS ASSERTED HIGH AND SOP L IS ASSERTED LOW.
11016
11017 030704 042737 000020 002342 12$: BIC    #VDAL4,T4GOOD            ;EXPECT EDEOC H TO BE A 0
11018 030712 004737 011176      JSR    PC,READT4                ;READ AND CHECK VDAL REGISTER
11019 030716 001405                BEQ    13$                      ;IF OK THEN CONTINUE
11020 030720                ERRDF  11,VDALRG,T4EROR          ;VDAL REGISTER NOT EQUAL EXPECTED
11021 030720 104455                TRAP  C$ERRDF
11022 030722 000013                .WORD 11
11023 030724 003706                .WORD VDALRG
11024 030726 006714                .WORD T4EROR
11025 030730                CKLOOP
11026 030730 104406                TRAP  C$CLP1
11027
11028                               ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11029                               ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11030
11031 030732 004737 011246      13$: JSR    PC,SLCTMS                ;SELECT THE MEMORY SIMULATOR MODULE
11032
11033                               ;THE PROGRAM WILL PRESET THE RDV AND WRV FLIP-FLOPS BY PULSING THE
11034                               ;SIGNAL RST H. WHEN THE RDV AND WRV FLIP-FLOPS ARE BRESET THE SIGNAL
11035                               ;MSBRK H WILL BE SET TO THE LOW STATE.
11036
11037 030736 004737 011266      JSR    PC,MSRSTH                ;GO PULSE RST H TO PRESET WRV + RDV F/F'S
11038
11039                               ;READ REG 2 TO CHECK THAT MSBRK H WENT TO A 0 AS A RESULT OF PULSING RST H.
11040
11041 030742 042737 000200 002246  BIC    #MSBRKH,S2GOOD            ;EXPECT MSBRK H TO BE A ZERO
11042 030750 004737 010560      JSR    PC,READS2                ;READ AND CHECK CONTROL REGISTER 2
11043 030754 001405                BEQ    14$                      ;IF OK THEN CONTINUE
11044 030756                ERRDF  2,,S2EROR              ;MSBRK H PROBABLY NOT 0 AFTER RST H

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11045 030756 104455 TRAP C$ERDF
11046 030760 000002 .WORD 2
11047 030762 000000 .WORD 0
11048 030764 005320 .WORD S2EROR
11049 030766 CKLOOP
11050 030766 104406 TRAP C$CLP1
11051
11052 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11053 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11054
11055 030770 004737 012212 14$: JSR PC,SLCTTE ;SELECT TARGET EMULATOR MODULE
11056
11057 ;GO PULSE THE SIGNAL BRKRES L BY SETTING AND CLEARING ADAL REGISTER BIT
11058 ;0. A PULSE ON THE SIGNAL BRKRES L WILL CAUSE THE MEMBRK F/F TO BE 0'ED.
11059
11060 030774 004737 012764 JSR PC,BRKRES ;GO PULSE BRKRES L VIA ADALO H
11061
11062 ;READ GDAL REGISTER TO CHECK THAT BRKRES L CLEARED MEMBRK FLIP-FLOP
11063
11064 031000 042737 000040 002326 BIC #MEMBRK,TOGOOD ;EXPECT MEMBRK H TO BE A ZERO
11065 031006 004737 011112 JSR PC,READT0 ;READ AND CHECK GDAL REGISTER
11066 031012 001405 BEQ 15$ ;IF OK THEN CONTINUE
11067 031014 ERRDF 9,GDALRG,TOEROR ;MEMBRK F/F PROBABLY NOT 0 AFTER RST H
11068 031014 104455 TRAP C$ERDF
11069 031016 000011 .WORD 9
11070 031020 003636 .WORD GDALRG
11071 031022 006664 .WORD TOEROR
11072 031024 CKLOOP
11073 031024 104406 TRAP C$CLP1
11074
11075 ;CHECK THAT THE SIGNAL EDEOC H IS NOW SET TO A 1 AS A RESULT OF THE SIGNAL
11076 ;SOP L RETURNING TO THE HIGH STATE AFTER THE SIGNAL MEMBRK H WENT TO LOW STATE.
11077
11078 031026 052737 000020 002342 15$: BIS #VDAL4,T4GOOD ;EXPECT EDEOC H TO BE A ONE
11079 031034 004737 011176 JSR PC,READT4 ;READ AND CHECK THE VDAL REGISTER
11080 031040 001405 BEQ 16$ ;IF VDAL REGISTER OK THEN CONTINUE
11081 031042 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
11082 031042 104455 TRAP C$ERDF
11083 031044 000013 .WORD 11
11084 031046 003706 .WORD VDALRG
11085 031050 006714 .WORD T4EROR
11086 031052 CKLOOP
11087 031052 104406 TRAP C$CLP1
11088
11089 ;ISSUE A PULSE ON THE SIGNAL INV D L TO INITIALIZE ALL OTHER FLIP-FLOPS
11090 ;ON THE MODULE NOT CLEARED VIA THE SIGNAL BRKRES L.
11091
11092 031054 005037 002340 16$: CLR T4LOAD ;SETUP TO CLEAR ALL VDAL R/W BITS
11093 031060 004737 012704 JSR PC,CLRPSM ;PULSE INV D L VIA VDAL2 H
11094 031064 ENDSEG
11095 031064 10000$: TRAP C$ESEG
11096 031064 104405 TRAP C$ESEG
11097 031066 ENDTST
11098 031066 L10046: TRAP C$ESEG
11099 031066 104401 TRAP C$ESEG

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11100      .SBTTL TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE
11101
11102      :++
11103      :
11104      : THIS TEST WILL CHECK THAT TARGET EMULATOR FDAL REGISTER BITS 7:2 CAN
11105      : BE CLOCKED INTO THE TDAL DIAGNOSTIC LATCHES IN 16 BIT MODE WHEN THE
11106      : TARGET EMULATOR MODULE IS ADDRESSING A LOCATION WHICH IS MAPPED ON THE
11107      : MEMORY SIMULATOR MODULE TO ALLOW READS AND WRITES TO THE TARGET RAM.
11108      : TO CHECK THAT THE TDAL LATCHES WERE CLOCKED WITH FDAL REGISTER DATA,
11109      : THE PROGRAM WILL ENABLE THE TDAL LATCHES TO THE EIDAL BUS WITH THE
11110      : TARGET RAM STILL BEING ADDRESSED. THE PROGRAM WILL THEN READ AND CHECK
11111      : THE EIDAL BUS TO CONTAIN THE CORRECT FDAL REGISTER DATA.
11112      :--
11113      031070      BGNTST
11114      031070      T11::
11115
11116      031070      004737      007436      JSR      PC,INITMD      ;INITIALIZE CDS-11 SYSTEM MODULES
11117
11118      031074      BGNSEG
11119      031074      104404      TRAP     C$BSEG
11120
11121      ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11122      ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11123
11124      031076      004737      011246      JSR      PC,SLCTMS      ;SELECT THE MEMORY SIMULATOR MODULE
11125
11126      ;TOGGLE THE SIGNAL RST H IN CONTROL REGISTER 0 AND SET THE SIGNAL MP H
11127      ;TO A ONE. A PULSE ON THE SIGNAL RST H WILL PRESET THE WRV AND RDV
11128      ;FLIP-FLOPS THUS CAUSING THE SIGNAL BRK L TO BE ASSERTED HIGH. SETTING
11129      ;THE SIGNAL MP H TO A ONE WILL ENABLE MAP PROTECTION BITS MPIN H,
11130      ;WRE H AND RDE H TO THE SYSTEM BUS ALONG WITH THE SIGNAL BRK L. THESE
11131      ;SIGNALS WILL BE ENABLED TO THE SYSTEM BUS AS ETR H, WVIOL H, MSBRK H
11132      ;AND RDE L. SETTING THE SIGNAL MP H WILL ALSO ENABLE THE SIGNALS MPIN H
11133      ;WRE H, AND BRK L TO CONTROL REGISTER 2 AS SIGNALS ESR H, WREN H AND
11134      ;MSBRK H RESPECTIVELY.
11135
11136      031102      112737      000005      002234      MOVB     #RSTH!MPH,SLOAD      ;SETUP BITS TO BE LOADED
11137      031110      004737      011266      JSR      PC,MSRSTH      ;PULSE RST H AND SET MP H TO A ONE
11138
11139      ;THE FOLLOWING SECTION WILL LOAD, READ AND CHECK THE MEMORY SIMULATOR
11140      ;MAP PROTECTION RAM. THE MAP PROTECTION RAM WILL BE SETUP TO ALLOW
11141      ;READS AND WRITES TO THE FIRST 128 WORDS OF MEMORY. THE FIRST 128
11142      ;WORDS OF MEMORY WILL BE MAPPED TO SELECT THE TARGET MEMORY. THE
11143      ;REMAINING LOCATIONS OF THE MAP PROTECTION RAM WILL BE MAPPED TO THE
11144      ;MEMORY SIMULATOR RAM AND SETUP TO INHIBIT READS AND WRITES TO THOSE
11145      ;LOCATIONS (777776-000400).
11146
11147      031114      005037      002254      CLR      S4LOAD      ;SETUP STARTING MSAD 15:0 BITS
11148      031120      012737      000010      002244      MOV      #MSEL1,S2LOAD      ;SETUP STARTING MSAD 17:16 BITS AND
11149      ;BITS TO SELECT MAP PROTECTION RAM
11150
11151      031126      1$:      BGNSEG
11152      031126      104404      TRAP     C$BSEG
11153
11154      ;SET THE SIGNAL MSEL1 H TO A ONE AND MSEL0 H TO A ZERO. THIS WILL
11155      ;CAUSE THE MAP PROTECTION RAM TO BE SELECTED VIA THE SIGNAL SMPM H

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11156                                     ;WHEN A READ OR WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6. MSAD
11157                                     ;BITS 17 AND 16 IN CONTROL REGISTER 2 WILL BE LOADED AND CHECKED FOR
11158                                     ;THE ADDRESS BEING TESTED.
11159
11160 031130 012737 177540 002250      MOV      #177540,S2MASK      ;SETUP TO IGNORE ESR H + WREN H
11161 031136 004737 010544              JSR      PC,LDRDS2         ;LOAD, READ AND CHECK CONTROL REG 2
11162 031142 001405                      BEQ      2$                ;IF LOADED OK THEN CONTINUE
11163 031144                                ERRDF   2,,S2EROR         ;CONTROL REG 2 NOT EQUAL EXPECTED
11164 031144 104455                      TRAP    C$ERDF
11165 031146 000002                      .WORD   2
11166 031150 000000                      .WORD   0
11167 031152 005320                      .WORD   S2EROR
11168 031154                                CKLOOP
11169 031154 104406                      TRAP    C$CLP1
11170
11171                                     ;LOAD, READ AND CHECK CONTROL REGISTER 4 FOR THE ADDRESS BEING TESTED.
11172                                     ;CONTROL REGISTER 4 CONTAINS BITS FOR MSAD ADDRESS BITS 15:0.
11173
11174 031156 004737 010604              2$:    JSR      PC,LDRDS4         ;LOAD, READ AND CHECK CONTROL REG 4
11175 031162 001405                      BEQ      3$                ;IF LOADED OK THEN CONTINUE
11176 031164                                ERRDF   3,MSADRG,S4EROR  ;MSAD BITS 15:0 NOT EQUAL EXPECTED
11177 031164 104455                      TRAP    C$ERDF
11178 031166 000003                      .WORD   3
11179 031170 002506                      .WORD   MSADRG
11180 031172 005334                      .WORD   S4EROR
11181 031174                                CKLOOP
11182 031174 104406                      TRAP    C$CLP1
11183
11184                                     ;LOAD, READ AND CHECK MAP PROTECTION RAM LOCATION ADDRESSED BY MSAD
11185                                     ;BITS 17:0. ADDRESSES 0 TO 376 WILL BE LOADED AND CHECKED WITH A
11186                                     ;DATA PATTERN OF 16. ALL OTHER ADDRESSES WILL BE LOADED AND CHECKED
11187                                     ;WITH A DATA PATTERN OF 11.
11188
11189 031176 012737 177760 002264      3$:    MOV      #177760,S6MASK      ;SETUP TO IGNORE UNUSED BITS
11190 031204 012737 000011 002260      MOV      #MUTB!MPINH,S6LOAD ;SETUP FOR ADDRESSES OVER 376
11191 031212 032737 000003 002244      BIT      #MSAD17!MSAD16,S2LOAD ;CHECK IF ADDRESS ABOVE 16K WORDS
11192 031220 001006                      BNE     4$                ;IF YES - LOAD R/W VIOLATION SETUP
11193 031222 005737 002254                      TST     S4LOAD            ;CHECK IF ADDRESS WAS OVER 376
11194 031226 001003                      BNE     4$                ;IF YES - LOAD R/W VIOLATION SETUP
11195 031230 012737 000016 002260      MOV      #MUTB!RDEH!WREH,S6LOAD ;SETUP TO ALLOW R/W TO FIRST 128 WORDS
11196 031236 004737 010630      4$:    JSR      PC,LDRDS6         ;LOAD, READ AND CHECK MAP PROTECT RAM
11197 031242 001405                      BEQ      5$                ;IF LOADED OK THEN CONTINUE
11198 031244                                ERRDF   4,MSGMP,S6ALLR   ;MAP PROTECT RAM DATA ERROR
11199 031244 104455                      TRAP    C$ERDF
11200 031246 000004                      .WORD   4
11201 031250 002601                      .WORD   MSGMP
11202 031252 005454                      .WORD   S6ALLR
11203 031254                                CKLOOP
11204 031254 104406                      TRAP    C$CLP1
11205
11206                                     ;CHECK MAP PROTECTION RAM DATA BITS MPIN H AND WRE H IN CONTROL
11207                                     ;REGISTER 2 AS ESR H AND WREN H RESPECTIVELY.
11208
11209 031256 042737 000140 002250      5$:    BIC      #ESRH!WRENH,S2MASK ;SETUP TO CHECK ESR H AND WREN H
11210 031264 052737 000100 002246      BIS      #WRENH,S2GOOD     ;EXPECT WREN H TO BE A ONE
11211 031272 032737 000006 002260      BIT      #WREH!RDEH,S6LOAD ;CHECK IF RAM WAS W/R ENABLED

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11212 031300 001006          BNE      6$          ;IF YES THEN GO READ CONTROL REG 2
11213 031302 042737 000100 002246    BIC      #WRENH,S2GOOD ;THIS ADDRESS WAS NOT WRITE ENABLED
11214 031310 052737 000040 002246    BIS      #ESRH,S2GOOD  ;EXPECT ESR H TO BE SET TO A ONE
11215 031316 004737 010560          JSR      PC,READS2     ;GO READ AND CHECK CONTROL REG 2
11216 031322 001404          BEQ      7$          ;IF OK THEN CONTINUE
11217 031324          ERRDF    2,MSGMPL,S2ALLR ;REGISTER 2 NOT EQUAL EXPECTED
11218 031324 104455          TRAP    C$ERDF
11219 031326 000002          .WORD   2
11220 031330 002456          .WORD   MSGMPL
11221 031332 005440          .WORD   S2ALLR
11222 031334          7$:      ENDSEG
11223 031334          10001$:
11224 031334 104405          TRAP    C$ESEG
11225
11226          ;UPDATE CONTROL REGISTERS 4 AND 2 FOR MSAD ADDRESS TO BE TESTED
11227
11228 031336 062737 000400 002254    ADD      #MSAD8,S4LOAD ;UPDATE MSAD BITS 15:8 BY ONE
11229 031344 001270          BNE     1$          ;IF NOT 0 THEN LOAD NEXT RAM LOCATION
11230 031346 005237 002244          INC     S2LOAD      ;UPDATE MSAD BITS 17:16 BY ONE
11231 031352 032737 000004 002244    BIT     #MSELO,S2LOAD ;CHECK IF ALL RAM LOCATIONS DONE
11232 031360 001662          BEQ     1$          ;IF NOT THEN LOAD NEXT RAM LOCATION
11233 031362 005337 002244          DEC     S2LOAD      ;RESET REG 2 TO ACTUAL VALUE LOADED
11234
11235          ;SET THE SIGNAL CTS H TO A ONE IN CONTROL REGISTER 0. WHEN CTS H IS
11236          ;SET TO A ONE, THE SYSTEM BUS LATCHES WILL BE ENABLED TO THE MEMORY
11237          ;SIMULATOR MODULE.
11238
11239 031366 052737 000002 002234    BIS     #CTSH,S0LOAD  ;SETUP BIT TO SET CTS H TO A ONE
11240 031374 004737 010504          JSR     PC,LDRDSO    ;GO LOAD, READ AND CHECK REG 0
11241 031400 001404          BEQ     8$          ;IF LOADED OK THEN CONTINUE
11242 031402          ERRDF    1,,SOEROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
11243 031402 104455          TRAP    C$ERDF
11244 031404 000001          .WORD   1
11245 031406 000000          .WORD   0
11246 031410 005304          .WORD   SOEROR
11247 031412          8$:      ENDSEG
11248 031412          10000$:
11249 031412 104405          TRAP    C$ESEG
11250
11251 031414          BGNSEG
11252 031414 104404          TRAP    C$BSEG
11253
11254          ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11255          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11256
11257 031416 004737 012212          JSR     PC,SLCTTE    ;SELECT THE TARGET EMULATOR MODULE
11258
11259 031422 005037 002352          CLR     T6MASK      ;RESET CONTROL REGISTER 6 MASK WORD
11260
11261          ;SET ADAL REGISTER BITS 14,10 AND 9 TO A ONE AND PULSE THE SIGNAL 'BRKRES L'
11262          ;BY TOGGING ADAL REGISTER BIT 0. ADAL10 H AND ADAL9 H SET TO ONES WILL
11263          ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS. PULSING
11264          ;THE SIGNAL 'BRKRES L' VIA ADALO H WILL CLEAR THE BREAK LOGIC ON THE
11265          ;TARGET EMULATOR MODULE. ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
11266          ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL 'CKAI H' TO BE PULSED VIA THE
11267          ;THE SIGNAL 'RASP L' LATER ON IN THIS TEST. ADAL REGISTER BIT 4 ON A

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11268
11269
11270
11271 031426 012737 043000 002334
11272 031434 004737 012764
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11278 031440 004537 012232
11279 031444 000003
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11297 031446 012737 001104 002346
11298 031454 004737 011214
11299 031460 001405
11300 031462
11301 031462 104455
11302 031464 000014
11303 031466 003754
11304 031470 006730
11305 031472
11306 031472 104406
11307
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11312
11313
11314
11315
11316
11317 031474 012737 000204 002340 9\$:
11318 031502 013737 002340 002342
11319 031510 052737 000040 002342
11320 031516 004737 011170
11321 031522 001405
11322 031524
11323 031524 104455

;ZERO WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE PAUSE MODE WHEN
;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.

MOV #ADAL14!ADAL10!ADAL9,T2LOAD ;SETUP BITS TO BE LOADED
JSR PC,BRKRES ;SET BITS 14, 10 + 9 AND TOGGLE ADALO H

;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
;REGISTER 6.

JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
.WORD HDAL ;SELECT THE HDAL REGISTER

;SET HDAL REGISTER BITS 9, 6 AND 2 TO A ONE AND HDAL BITS 14, 11, 5, 4
;AND 3 TO A ZERO. HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO CONTROL
;THE T-11 TIMING AND CONTROL SIGNALS. HDAL9 H ON A ONE WILL ENABLE THE
;OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER TO THE SYSTEM ADDRESS BUS.
;HDAL14 H AND HDAL11 H ON A ZERO WILL SET SYSTEM ADDRESS BITS 17 AND 16
;TO A ZERO. HDAL4 H AND HDAL3 H SET TO ZEROES WILL SET THE SIGNALS
;PR/WHB L AND PR/WLB L TO THE HIGH STATE. THESE TWO SIGNALS WILL CAUSE
;THE SIGNALS DTLB L AND DTHB L TO BE ASSERTED LOW LATER ON IN THE TEST
;WHEN SOME OTHER GATING SIGNALS ARE ENABLED HIGH. DTHB L AND DTLB L
;ASSERTED LOW WILL ENABLE THE CDAL BUS TO THE TDAL BUS. HDAL5 H ON A
;ZERO AND HDAL6 H ON A ONE WILL CAUSE THE SIGNAL PSEL0 L TO BE ASSERTED
;HIGH AND PSEL1 L TO BE ASSERTED LOW. PSEL1 L SET LOW WILL DISABLE ONE
;OF THE DATA PATHS TO THE TDAL BUS. WITH PSEL0 L SET HIGH AND PSEL1 L
;SET LOW, THE SIGNAL INTER L WILL BE ASSERTED LOW THUS ENABLING FDAL
;REGISTER BITS 7:2 TO THE EODAL BUS AND CLEARING THE EOAI REGISTER.

MOV #HDAL9!HDAL6!HDAL2,T6LOAD ;SET HDAL BITS 9, 6 AND 2 TO ONES
JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK HDAL REGISTER
BEQ 9\$;IF LOADED OK THEN CONTINUE
ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
TRAP C\$ERDF
.WORD 12
.WORD HDALRG
.WORD T06ERR
CKLOOP
TRAP C\$CLP1

;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
;REGISTER 4. PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
;FLIP-FLOPS ON THE MODULE NOT CLEARED BY THE SIGNAL "BRKRES L". SET
;THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE.
;ON A READ COMMAND TO CONTROL REGISTER 4, THE SIGNAL BTS1 H WILL BE SET
;TO A ONE AS A RESULT OF THE SIGNAL INTER L BEING ASSERTED LOW. THE
;SIGNAL INTER L IS ASSERTED LOW AS A RESULT OF PSEL0 L BEING ASSERTED
;HIGH AND PSEL1 L BEING ASSERTED LOW.

MOV #VDAL7!VDAL2,T4LOAD ;SETUP BITS TO BE LOADED
MOV T4LOAD,T4GOOD ;COPY LOADED TO EXPECTED
BIS #VDAL5,T4GOOD ;EXPECT BTS1 H TO BE A ONE
JSR PC,LDRD4T ;GO LOAD, READ AND CHECK VDAL REG
BEQ 10\$;IF OK THEN CONTINUE
ERRDF 11,VDALRG,T4EROR ;VDAL REG NOT EQUAL TO EXPECTED
TRAP C\$ERDF


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11324 031526 000013 .WORD 11
11325 031530 003706 .WORD VDALRG
11326 031532 006714 .WORD T4EROR
11327 031534 CKLOOP
11328 031534 104406 TRAP C$CLP1
11329 031536 042737 000004 002340 10$: BIC #VDAL2,T4LOAD ;SET VDAL2 H TO THE LOW STATE
11330 031544 042737 000004 002342 BIC #VDAL2,T4GOOD ;SETUP TO EXPECT IT TO BE ZERO
11331 031552 004737 011170 JSR PC,LDRD4T ;GO LOAD, READ AND CHECK VDAL REG
11332 031556 001405 BEQ 11$ ;IF OK THEN CONTINUE
11333 031560 ERRDF 11,VDALRG,T4EROR ;VDAL REG NOT EQUAL TO EXPECTED
11334 031560 104455 TRAP C$ERDF
11335 031562 000013 .WORD 11
11336 031564 003706 .WORD VDALRG
11337 031566 006714 .WORD T4EROR
11338 031570 CKLOOP
11339 031570 104406 TRAP C$CLP1
11340
11341 ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4. ON
11342 ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
11343 ;BE WRITTEN OR READ.
11344
11345 031572 004537 012232 11$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
11346 031576 000004 .WORD MODE ;SELECT THE MODE REGISTER
11347
11348 ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
11349 ;ZEROES. MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
11350
11351 031600 005037 002346 CLR T6LOAD ;SETUP TO CLEAR ALL MODE REGISTER BITS
11352 031604 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK MODE REGISTER
11353 031610 001405 BEQ 12$ ;IF LOADED OK THEN CONTINUE
11354 031612 ERRDF 12,MODREG,T06ERR ;MODE REGISTER NOT EQUAL EXPECTED
11355 031612 104455 TRAP C$ERDF
11356 031614 000014 .WORD 12
11357 031616 004000 .WORD MODREG
11358 031620 006730 .WORD T06ERR
11359 031622 CKLOOP
11360 031622 104406 TRAP C$CLP1
11361
11362 ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
11363 ;TO A 2. THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
11364 ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
11365 ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
11366 ;TER WILL BE ADDRESSED.
11367
11368 031624 004537 012232 12$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
11369 031630 000002 .WORD FDAL ;SELECT EOAI AND FDAL REGISTER
11370
11371 ;LOAD, READ AND CHECK THE FDAL AND EOAI REGISTER. THE EOAI REGISTER
11372 ;WILL BE HELD CLEARED BY THE SIGNAL INTER L BEING ASSERTED LOW. TO
11373 ;CHECK THIS, THE PROGRAM WILL ATTEMPT TO LOAD ALL ONES INTO THE EOAI
11374 ;REGISTER. ALL ZEROES SHOULD BE READ BACK FROM THE EOAI REGISTER WHEN
11375 ;THE SIGNAL INTER L IS HELD LOW. THE FDAL REGISTER WILL BE LOADED AND
11376 ;CHECKED WITH A DATA PATTERN OF 125. FDALO H ON A ONE WILL ENABLE THE
11377 ;EOAI REGISTER TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 INSTEAD
11378 ;OF THE CTL REGISTER.
11379

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11380 031632 012737 000125 002346      MOV      #125,T6LOAD      ;SETUP FDAL REGISTER BITS
11381 031640 012777 177525 150344      MOV      #177525,@REG6   ;LOAD EOAI AND FDAL REGISTER
11382 031646 004737 011222                JSR      PC,READT6       ;READ AND CHECK EOAI AND FDAL REGISTER
11383 031652 001405                BEQ      13$             ;IF LOADED OK THEN CONTINUE
11384 031654                ERRDF   12,EOAIFD,T06ERR ;INTER L PROBALLY DIDN'T CLEAR EOAI REG
11385 031654 104455                TRAP    C$ERDF
11386 031656 000014                .WORD   12
11387 031660 004045                .WORD   EOAIFD
11388 031662 006730                .WORD   T06ERR
11389 031664                CKLOOP
11390 031664 104406                TRAP    C$CLP1
11391
11392                ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
11393                ;2:0 TO A 0. THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH A DATA
11394                ;PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6. THE DIAGNOSTIC ADDRESS
11395                ;REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER BIT 10
11396                ;BEING SET TO A ONE PREVIOUSLY. ON A READ COMMAND TO CONTROL REGISTER
11397                ;6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
11398
11399 031666 004537 012232      13$:    JSR      R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
11400 031672 000000                .WORD   ADDRES          ;SELECT DIAG ADDRESS REG AND ADDRESS BUS
11401
11402                ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA PATTERN
11403                ;OF 000000. THIS WILL CAUSE TARGET MEMORY TO BE SELECTED LATER ON IN
11404                ;THIS TEST. ADDRESS BITS 17 AND 16 WERE SET TO A ZERO EARLIER IN THIS
11405                ;TEST VIA THE HDAL REGISTER.
11406
11407 031674 005037 002346      CLR      T6LOAD          ;SETUP TO LOAD ADDRESS 000000
11408 031700 004737 011214      JSR      PC,LDRDT6       ;LOAD, READ AND CHECK DIAG ADDRESS REG
11409 031704 001405                BEQ      14$             ;IF LOADED OK THEN CONTINUE
11410 031706                ERRDF   12,ADDRRG,T06ERR ;DIAGNOSTIC ADDRESS REGISTER ERROR
11411 031706 104455                TRAP    C$ERDF
11412 031710 000014                .WORD   12
11413 031712 004142                .WORD   ADDRREG
11414 031714 006730                .WORD   T06ERR
11415 031716                CKLOOP
11416 031716 104406                TRAP    C$CLP1
11417
11418                ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
11419                ;CHANGES OCCURED DURING THE PAST SEQUENCES.
11420
11421 031720 004737 011176      14$:    JSR      PC,READT4       ;READ AND CHECK VDAL REGISTER
11422 031724 001405                BEQ      15$             ;IF NO CHANGES THEN CONTINUE
11423 031726                ERRDF   11,VDALRG,T4EROR ;VDAL OR PAUSE STATE MACHINE ERROR
11424 031726 104455                TRAP    C$ERDF
11425 031730 000013                .WORD   11
11426 031732 003706                .WORD   VDALRG
11427 031734 006714                .WORD   T4EROR
11428 031736                CKLOOP
11429 031736 104406                TRAP    C$CLP1
11430
11431                ;RE-SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE
11432                ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
11433                ;CONTROL REGISTER 6.
11434
11435 031740 004537 012232      15$:    JSR      R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD

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HARDWARE TESTS MACY11 30(1046)
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TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE

SEQ 0221

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11436 031744 000003          .WORD  HDAL          ;SELECT THE HDAL REGISTER
11437
11438 031746 012737 001104 002346  MOV    #HDAL9!HDAL6!HDAL2,T6LOAD ;BITS THAT WERE PREVIOUSLY LOADED
11439
11440          ;SET THE SIGNALS XRAS H AND PRAS H TO THE HIGH STATES BY SETTING HDAL12 H
11441          ;TO A ONE.  WHEN XRAS H IS SET HIGH, THE PAUSE MODE FLIP-FLOP, THE
11442          ;EDFET FLIP-FLOP, AND THE BTFET FLIP-FLOP WILL BE CLOCKED TO ONES.
11443          ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE AS A
11444          ;RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH.  SOP H IS ASSERTED
11445          ;HIGH WHEN THE SIGNAL PAUSE L IS ASSERTED HIGH (PAUSE MODE).  WHEN
11446          ;PRAS H IS SET HIGH, THE ADDRESS BUS, WHICH CONTAINS THE DIAGNOSTIC
11447          ;ADDRESS REGISTER DATA, WILL BE CLOCKED INTO THE MEMORY SIMULATORS
11448          ;SYSTEM ADDRESS BUS LATCHES.  SELECTING ADDRESS ZERO ON THE MEMORY
11449          ;SIMULATOR MODULE WILL CAUSE THE SIGNALS ETR H AND WVIOL L TO BE
11450          ;ASSERTED HIGH.
11451
11452 031754 004737 012276      JSR    PC,XRASH          ;SET XRAS H AND PRAS H TO THE HIGH STATE
11453
11454          ;READ THE VDAL REGISTER AND CHECK THAT THE SIGNAL PSMW H IS ASSERTED
11455          ;HIGH AS A RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH.
11456
11457 031760 052737 001000 002342  BIS    #VDAL9,T4GOOD    ;EXPECT PSMW H TO BE A ONE
11458 031766 004737 011176      JSR    PC,READT4        ;READ AND CHECK VDAL REGISTER
11459 031772 001405              BEQ    16$              ;IF OK THEN CONTINUE
11460 031774          ERRDF  11,VDALRG,T4EROR    ;VDAL REGISTER NOT EQUAL EXPECTED
11461 031774 104455              TRAP  C$ERDF
11462 031776 000013              .WORD  11
11463 032000 003706              .WORD  VDALRG
11464 032002 006714              .WORD  T4EROR
11465 032004          CKLOOP
11466 032004 104406              TRAP  C$CLP1
11467
11468          ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11469          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11470
11471 032006 004737 011246      16$:  JSR    PC,SLCTMS
11472
11473          ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED AS A RESULT
11474          ;OF CLOCKING THE SYSTEM ADDRESS BUS INTO THE MEMORY SIMULATOR SYSTEM
11475          ;ADDRESS BUS LATCHES.
11476
11477 032012 004737 010520      JSR    PC,READS0        ;READD AND CHECK CONTROL REISTER 0
11478 032016 001405              BEQ    17$              ;IF OK THEN CONTINUE
11479 032020          ERRDF  1,SOEROR    ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
11480 032020 104455              TRAP  C$ERDF
11481 032022 000001              .WORD  1
11482 032024 000000              .WORD  0
11483 032026 005304              .WORD  SOEROR
11484 032030          CKLOOP
11485 032030 104406              TRAP  C$CLP1
11486
11487          ;READ CONTROL REGISTER 4 TO CHECK THAT ADDRESS 0 WAS CLOCKED INTO THE
11488          ;SYSTEM ADDRESS BUS LATCHES.  WHEN CTS H IS ASSERTED HIGH, THE SYSTEM
11489          ;ADDRESS BUS LATHCES ARE ENABLED TO MSAD BITS 17:0
11490
11491 032032 005037 002254      17$:  CLR    S4LOAD          ;SETUP TO EXPECT ADDRESS TO BE 0

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TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE

SEQ 0222

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11492 032036 004737 010612      JSR      PC,READS4      ;READ AND CHECK MSAD 15:0
11493 032042 001405              BEQ      18$            ;IF OK THEN CONTINUE
11494 032044              ERRDF    3,MSADRG,S04ERR ;MSAD 15:0 SYSTEM ADDRESS BUS LATCH ERROR
11495 032044 104455              TRAP    C$ERDF
11496 032046 000003              .WORD   3
11497 032050 002506              .WORD   MSADRG
11498 032052 005404              .WORD   S04ERR
11499 032054              CKLOOP
11500 032054 104406              TRAP    C$CLP1
11501
11502                          ;READ CONTROL REGISTER 2 TO CHECK THAT MSAD BITS 17 AND 16 ARE ZERO AND
11503                          ;THAT THE SIGNALS ESR H AND MSBRK H ARE ZERO. THE SIGNAL WREN H SHOULD
11504                          ;BE ASSERTED HIGH BECAUSE THE MAP PROTECTION RAM WAS SETUP TO ALLOW
11505                          ;READS AND WRITES TO ADDRESSES 0-376.
11506
11507 032056 052737 000014 002250 18$:  BIS      #MSEL1!MSEL0,S2MASK ;SETUP TO IGNORE TRI-STATED BITS
11508 032064 012737 000010 002244      MOV      #MSEL1,S2LOAD ;SETUP PREVIOUSLY LOADED BIT
11509 032072 012737 000100 002246      MOV      #WRENH,S2GOOD ;EXPECT WREN H TO BE ASSERTED HIGH
11510 032100 004737 010560      JSR      PC,READS2      ;READ AND CHECK CONTROL REGISTER 2
11511 032104 001405              BEQ      19$            ;IF OK THEN CONTINUE
11512 032106              ERRDF    2,S2EROR      ;CONTROL REGISTER 2 NOT EQUAL EXPECTED
11513 032106 104455              TRAP    C$ERDF
11514 032110 000002              .WORD   2
11515 032112 000000              .WORD   0
11516 032114 005320              .WORD   S2EROR
11517 032116              CKLOOP
11518 032116 104406              TRAP    C$CLP1
11519
11520                          ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11521                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11522
11523 032120 004737 012212      19$:  JSR      PC,SLCTTE      ;SELECT THE TARGET EMULATOR MODULE
11524
11525
11526                          ;SELECT THE EODAL BUS BY SETTING GDDAL BITS 2:0 TO A 7. ON A READ
11527                          ;COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE READ VIA THE
11528                          ;SIGNAL RPT7 L.
11529
11530 032124 004537 012232      JSR      R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
11531 032130 000007              .WORD   EODAL          ;SELECT THE EODAL BUS TO BE READ
11532
11533                          ;AT THIS POINT IN TIME, FDAL REGISTER BITS 7:2 SHOULD BE ENABLED TO THE
11534                          ;EODAL BUS VIA THE SIGNAL INTER L. THE FDAL REGISTER WAS LOADED
11535                          ;PREVIOUSLY WITH A DATA PATTERN OF 125. WHEN READ ON THE EODAL BUS,
11536                          ;BITS 1 AND 0 WILL BE READ AS A ZERO.
11537
11538 032132 012737 000124 002346      MOV      #124,T6LOAD    ;SETUP EXPECTED FDAL DATA TO EODAL BUS
11539 032140 012737 177400 002352      MOV      #177400,T6MASK ;SETUP TO IGNORE TRI-STATED HIGH BYTE
11540 032146 004737 011222      JSR      PC,READT6      ;READ AND CHECK THE EODAL BUS
11541 032152 001405              BEQ      20$            ;IF OK THEN CONTINUE
11542 032154              ERRDF    12,FDEODL,T6ALLR ;FDAL REG 7:2 TO EODAL BUS ERROR
11543 032154 104455              TRAP    C$ERDF
11544 032156 000014              .WORD   12
11545 032160 004605              .WORD   FDEODL
11546 032162 006744              .WORD   T6ALLR
11547 032164              CKLOOP

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TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE

SEQ 0223

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11548 032164 104406          TRAP      C$CLP1
11549
11550          ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
11551          ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
11552          ;REGISTER 6.
11553
11554 032166 004537 012232      20$:   JSR      R5,SELTERR          ;SELECT REGISTER SPECIFIED BY NEXT WORD
11555 032172 000003          .WORD   HDAL                ;SELECT THE HDAL REGISTER
11556
11557 032174 012737 011104 002346  MOV     #HDAL12!HDAL9!HDAL6!HDAL2,T6LOAD ;BITS PREVIOUSLY SET
11558 032202 005037 002352          CLR     T6MASK              ;CLEAR CONTROL REGISTER 6 MASK WORD
11559
11560          ;TO ENABLE THE EODAL BUS TO THE CDAL BUS THE PROGRAM MUST SET THE SIGNAL
11561          ;PPI H TO THE HIGH STATE BY SETTING HDAL15 H TO A ONE.  WHEN PPI H,
11562          ;PSMW H, AND MR11 L ARE ASSERTED HIGH, THE SIGNALS COHB L AND COLB L
11563          ;WILL BE ASSERTED LOW THUS ENABLING THE EODAL BUS TO THE CDAL BUS.
11564          ;THE EODAL BUS PRESENTLY CONTAINS DATA FROM FDAL REGISTER BITS 7:2 (124).
11565          ;THE CDAL BUS WILL UNCONDITIONALLY BE ENABLED TO THE EIDAL BUS.  THE CDAL
11566          ;BUS WILL ALSO BE ENABLED TO THE TDAL BUS BY THE SIGNALS DTHB L AND
11567          ;DTLB L BEING ASSERTED LOW.  THESE TWO SIGNALS ARE ASSERTED LOW AS A
11568          ;RESULT OF WVIOL L, ETR H, PR/WHB L, PR/WLB L, MR11 L, PBCLR L, AND
11569          ;PSELO L BEING ASSERTED HIGH.
11570
11571 032206 004737 012506          JSR     PC,XPIH              ;SET XPI H AND PPI H TO THE HIGH STATE
11572
11573          ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  ON A READ
11574          ;COMMAND TO CONTROL REGISTER 6, THE EIDAL BUS WILL BE READ VIA RPT6 L.
11575
11576 032212 004537 012232          JSR     R5,SELTERR          ;SELECT REG SPECIFIED BY NEXT WORD
11577 032216 000006          .WORD   EIDAL              ;SELECT THE EIDAL BUS TO BE READ
11578
11579          ;AT THE PRESENT TIME DATA FROM FDAL REGISTER BITS 7:2 (124) ARE ENABLED
11580          ;TO THE EODAL BUS, THE CDAL BUS, THE EIDAL BUS AND THE TDAL BUS VIA
11581          ;THE SIGNALS INTER L, COHB L, COLB L, DTHB L AND DTLB L.  THE
11582          ;FOLLOWING SECTION WILL READ THE EIDAL BUS TO CHECK THAT THE FDAL
11583          ;REGISTER DATA IS ENABLED TO IT VIA THE EODAL AND CDAL BUSES.
11584
11585 032220 012737 000124 002346  MOV     #124,T6LOAD          ;SETUP EXPECTED FDAL TO EIDAL BUS DATA
11586 032226 012737 177400 002352  MOV     #177400,T6MASK      ;SETUP TO IGNORE TRI-STATE HIGH BYTE
11587 032234 004737 011222          JSR     PC,READT6          ;READ AND CHECK EIDAL BUS DATA
11588 032240 001405          BEQ    21$                 ;IF DATA OK THEN CONTINUE
11589 032242          ERRDF 12,FDEIDL,T6ALLR   ;FDAL REG 7:2 TO EIDAL BUS ERROR VIA CDAL
11590 032242 104455          TRAP   C$ERRDF
11591 032244 000014          .WORD  12
11592 032246 004645          .WORD  FDEIDL
11593 032250 006744          .WORD  T6ALLR
11594 032252          CKLOOP
11595 032252 104406          TRAP   C$CLP1
11596
11597          ;AT THE PRESENT TIME DATA FROM FDAL REGISTER BITS 7:2 (124) ARE ENABLED
11598          ;TO THE EODAL BUS, THE CDAL BUS, THE EIDAL BUS AND THE TDAL BUS VIA THE
11599          ;SIGNALS INTER L, COHB L, COLB L, DTHB L, AND DTLB L.  TO CHECK
11600          ;THAT FDAL REGISTER BITS 7:2 ARE ENABLED TO THE TDAL BUS, THE
11601          ;PROGRAM MUST CLOCK THE DATA INTO THE TDAL DIAGNOSTIC LATCHES FIRST SO
11602          ;THAT THE DATA CAN BE READ BACK LATER ON IN THIS TEST.  TO CLOCK THE
11603          ;DATA INTO THE TDAL LATCHES, THE PROGRAM MUST SET THE SIGNAL VDAL2 H TO

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11604 ;A ONE AND THEN ZERO. PULSING THE SIGNAL VDAL2 H WILL CAUSE A PULSE ON
11605 ;THE SIGNAL "INVD L" WHICH WILL CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS,
11606 ;THE EDFET AND BTFET FLIP-FLOPS. WITH THESE FLIP-FLOPS CLEARED, THE
11607 ;FDAL REGISTER DATA WILL BE DISABLED FROM THE CDAL BUS, THE EIDAL BUS AND
11608 ;THE TDAL BUS. THE SIGNAL FETCT H WILL ALSO BE SET TO A ZERO IN THE
11609 ;FOLLOWING SECTION.
11610
11611 032254 012737 000004 002340 21$: MOV #VDAL2,T4LOAD ;SET FETCT H LOW AND SET VDAL2 H HIGH
11612 032262 013737 002340 002342 MOV T4LOAD,T4GOOD ;COPY DATA LOADED TO EXPECTED
11613 032270 052737 000040 002342 BIS #VDAL5,T4GOOD ;EXPECT BTS1 H TO BE A 1 VIA INTER L
11614 032276 004737 011170 JSR PC,LDRD4T ;LOAD, READ AND CHECK VDAL REGISTER
11615 032302 001405 BEQ 22$ ;IF LOADED OK THEN CONTINUE
11616 032304 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
11617 032304 104455 TRAP C$ERDF
11618 032306 000013 .WORD 11
11619 032310 003706 .WORD VDALRG
11620 032312 006714 .WORD T4EROR
11621 032314 CKLOOP
11622 032314 104406 TRAP C$CLP1
11623 032316 042737 000004 002340 22$: BIC #VDAL2,T4LOAD ;SETUP TO SET VDAL2 H LOW
11624 032324 042737 000004 002342 BIC #VDAL2,T4GOOD ;SETUP TO EXPECT VDAL2 H TO BE A 0
11625 032332 004737 011170 JSR PC,LDRD4T ;LOAD, READ AND CHECK VDAL REGISTER
11626 032336 001405 BEQ 23$ ;IF LOADED OK THEN CONTINUE
11627 032340 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
11628 032340 104455 TRAP C$ERDF
11629 032342 000013 .WORD 11
11630 032344 003706 .WORD VDALRG
11631 032346 006714 .WORD T4EROR
11632 032350 CKLOOP
11633 032350 104406 TRAP C$CLP1
11634
11635 ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
11636 ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
11637 ;REGISTER 6.
11638
11639 032352 004537 012232 23$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
11640 032356 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
11641
11642 ;THE FOLLOWING SECTION WILL SET THE SIGNALS XRAS H AND PPI H TO THE
11643 ;LOW STATE BY CLEARING HDAL REGISTER BITS 15 AND 12.
11644
11645 032360 012737 111104 002346 MOV #HDAL15!HDAL12!HDAL9!HDAL6!HDAL2,T6LOAD ;LOADED BITS
11646 032366 005037 002352 CLR T6MASK ;SETUP MASK WORD TO CHECK ALL BITS
11647 032372 004737 012540 JSR PC,XPIL ;SET XPI H AND PPI H LOW
11648 032376 004737 012330 JSR PC,XRASL ;SET XRAS H AND PRAS H LOW
11649
11650 ;SET HDAL REGISTER BITS 4 AND 3 TO A ONE TO SET THE SIGNALS PR/WHB H AND
11651 ;PR/WLB H TO THE HIGH STATE.
11652
11653 032402 052737 000030 002346 BIS #HDAL4!HDAL3,T6LOAD ;SET PR/WHB H AND PR/WLB H TO HIGH STATE
11654 032410 004737 011214 JSR PC,LDRDT6 ;LOAD, READ AND CHECK THE HDAL REGISTER
11655 032414 001405 BEQ 24$ ;IF LOADED OK THEN CONTINUE
11656 032416 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
11657 032416 104455 TRAP C$ERDF
11658 032420 000014 .WORD 12
11659 032422 003754 .WORD HDALRG
    
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TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE

SEQ 0225

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11660 032424 006730      .WORD  T06ERR
11661 032426             CKLOOP
11662 032426 104406      TRAP   C$CLP1
11663
11664                   ;SET THE SIGNAL VDALO H TO A ONE TO ENABLE THE OUTPUTS OF THE TDAL
11665                   ;DIAGNOSTIC LATCHES ONTO THE TDAL BUS. THE TDAL LATCHES WERE LOADED
11666                   ;WITH DATA FROM FDAL REGISTER BITS 7:2 (124) EARLIER IN THIS TEST.
11667
11668 032430 052737 000001 002340 24$:  BIS   #VDALO,T4LOAD      ;SETUP BIT TO BE LOADED
11669 032436 052737 000001 002342      BIS   #VDALO,T4GOOD     ;EXPECT VDALO H TO BE SET ON READ
11670 032444 004737 011170      JSR   PC,LDRD4T        ;LOAD, READ AND CHECK VDAL REGISTER
11671 032450 001405      BEQ   25$              ;IF LOADED OK THEN CONTINUE
11672 032452             ERRDF  11,VDALRG,T4EROR      ;VDAL REGISTER NOT EQUAL EXPECTED
11673 032452 104455      TRAP  C$ERDF
11674 032454 000013      .WORD  11
11675 032456 003706      .WORD  VDALRG
11676 032460 006714      .WORD  T4EROR
11677 032462             CKLOOP
11678 032462 104406      TRAP  C$CLP1
11679
11680                   ;THE FOLLOWING SIGNALS ETR H, MR11 L, PR/WHB H, PR/WLB H, AND PSMW L
11681                   ;SHOULD BE ASSERTED HIGH. THEREFORE, BY SETTING PPI H TO THE HIGH
11682                   ;STATE, THE SIGNALS DBHB L AND DBLB L SHOULD BE ASSERTED LOW. THESE
11683                   ;TWO SIGNALS WILL ENABLE THE TDAL BUS, WHICH HAS THE TDAL DIAGNOSTIC
11684                   ;LATCHES ENABLED TO IT, TO THE CDAL BUS AND THE CDAL BUS WILL BE ENABLED
11685                   ;TO THE EIDAL BUS UNCONDITIONALLY. THE TDAL LATCHES WERE LOADED EARLIER
11686                   ;IN THIS TEST WITH DATA FROM FDAL REGISTER BITS 7:2 (124).
11687
11688 032464 004737 012506      25$:  JSR   PC,XPIH          ;SET XPI H AND PPI H TO HIGH STATE
11689
11690                   ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6. ON A READ
11691                   ;COMMAND TO CONTROL REGISTER 6, THE EIDAL BUS WILL BE READ VIA THE
11692                   ;SIGNAL RPT6 L.
11693
11694 032470 004537 012232      JSR   R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
11695 032474 000006      .WORD  EIDAL          ;SELECT THE EIDAL BUS TO BE READ
11696
11697                   ;AT THE PRESENT TIME THE TDAL DIAGNOSTIC LATCHES ARE ENABLED TO THE
11698                   ;TDAL BUS, THE CDAL BUS AND THE EIDAL BUS VIA THE SIGNALS VDALO H,
11699                   ;DBHB L AND DBLB L. THE TDAL LATCHES WERE LOADED EARLIER IN THE TEST
11700                   ;WITH DATA FROM FDAL REGISTER BITS 7:2 (124). THE PROGRAM WILL
11701                   ;NOW READ THE EIDAL BUS TO CHECK THAT FDAL REGISTER BITS 7:2 DATA
11702                   ;(124) WAS LOADED INTO THE TDAL LATCHES AND THAT THE TDAL LATCHES
11703                   ;ARE ENABLED TO THE EIDAL BUS.
11704
11705 032476 012737 000124 002346      MOV   #124,T6LOAD     ;SETUP EXPECTED FDAL TO EIDAL BUS DATA
11706 032504 012737 177400 002352      MOV   #177400,T6MASK ;SETUP TO IGNORE TRI-STATE HIGH BYTE
11707 032512 004737 011222      JSR   PC,READT6      ;READ AND CHECK THE EIDAL BUS
11708 032516 001405      BEQ   26$              ;IF DATA OK THEN CONTINUE
11709 032520             ERRDF  12,FDTDEI,T6ALLR      ;FDAL TO TDAL LATCHES TO EIDAL BUS ERROR
11710 032520 104455      TRAP  C$ERDF
11711 032522 000014      .WORD  12
11712 032524 004705      .WORD  FDTDEI
11713 032526 006744      .WORD  T6ALLR
11714 032530             CKLOOP
11715 032530 104406      TRAP  C$CLP1

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11716
11717
11718 ;SELECT THE HDAL REGISER BY SETTING DGAL BITS 2:0 TO A 3. THE HDAL
11719 ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
11720 ;CONTROL REGISTER 6.
11721 032532 004537 012232 26$: JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
11722 032536 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
11723
11724 032540 012737 101034 002346 MOV #HDAL15!HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;BIT LOADED BEFORE - HDAL6 H
11725 032546 005037 002352 CLR T6MASK ;SETUP MASK TO CHECK ALL BITS
11726
11727 ;SET THE SIGNALS XPI H AND PPI H TO THE LOW STATE BY CLEARING HDAL
11728 ;REGISTER BIT 15. ALOS SET THE SIGNAL PSEL1 L TO THE HIGH STATE BY
11729 ;SETTING HDAL REGISTER BIT 6 TO A 0.
11730
11731 032552 004737 012540 JSR PC,XPIL ;SET XPI H AND PPI H TO LOW STATE
11732
11733 ;ISSUE A PULSE ON THE SIGNAL "INVD L" TO RE-INITIALIZE THE MODULE.
11734
11735 032556 005037 002340 CLR T4LOAD ;SETUP TO CLEAR ALL BITS
11736 032562 004737 012704 JSR PC,CLRPSM ;GO PULSE INVD L VIA VDAL2 H
11737
11738 032566 ENDSEG
11739 032566 10002$: TRAP C$ESEG
11740 032566 104405
11741
11742 032570 ENDTST
11743 032570 L10047: TRAP C$ETST
11744 032570 104401
11745

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11746 .SBTTL TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE
11747
11748 :++
11749 : THIS TEST WILL CHECK THAT TARGET EMULATOR FDAL REGISTER BITS 7:2 CAN
11750 : BE CLOCKED INTO THE TDAL DIAGNOSTIC LATCHES IN 8 BIT MODE WHEN THE
11751 : TARGET EMULATOR MODULE IS ADDRESSING A LOCATION WHICH IS MAPPED ON THE
11752 : MEMORY SIMULATOR MODULE TO ALLOW READS AND WRITES TO THE TARGET RAM.
11753 : TO CHECK THAT THE TDAL LATCHES WERE CLOCKED WITH FDAL REGISTER DATA,
11754 : THE PROGRAM WILL ENABLE THE TDAL LATCHES TO THE EIDAL BUS WITH THE
11755 : TARGET RAM STILL BEING ADDRESSED. THE PROGRAM WILL THEN READ AND CHECK
11756 : THE EIDAL BUS TO CONTAIN THE CORRECT FDAL REGISTER DATA.
11757 :--
11758
11759 032572 BGNTST
11760 032572 T12::
11761
11762 032572 004737 007436 JSR PC,INITMD ;INITIALIZE CDS-11 SYSTEM MODULES
11763
11764 032576 BGNSEG
11765 032576 104404 TRAP C$BSEG
11766
11767 ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11768 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11769
11770 032600 004737 011246 JSR PC,SLCTMS ;SELECT THE MEMORY SIMULATOR MODULE
11771
11772 ;TOGGLE THE SIGNAL RST H IN CONTROL REGISTER 0 AND SET THE SIGNAL MP H
11773 ;TO A ONE. A PULSE ON THE SIGNAL RST H WILL PRESET THE WRV AND RDV
11774 ;FLIP-FLOPS THUS CAUSING THE SIGNAL BRK L TO BE ASSERTED HIGH. SETTING
11775 ;THE SIGNAL MP H TO A ONE WILL ENABLE MAP PROTECTION BITS MPIN H,
11776 ;WRE H AND RDE H TO THE SYSTEM BUS ALONG WITH THE SIGNAL BRK L. THESE
11777 ;SIGNALS WILL BE ENABLED TO THE SYSTEM BUS AS ETR H, WVIOL H, MSBRK H
11778 ;AND RDE L. SETTING THE SIGNAL MP H WILL ALSO ENABLE THE SIGNALS MPIN H
11779 ;WRE H, AND BRK L TO CONTROL REGISTER 2 AS SIGNALS ESR H, WREN H AND
11780 ;MSBRK H RESPECTIVELY.
11781
11782 032604 112737 000005 002234 MOVB #RSTH!MPH,S0LOAD ;SETUP BITS TO BE LOADED
11783 032612 004737 011266 JSR PC,MSRSTH ;PULSE RST H AND SET MP H TO A ONE
11784
11785 ;THE FOLLOWING SECTION WILL LOAD, READ AND CHECK THE MEMORY SIMULATOR
11786 ;MAP PROTECTION RAM. THE MAP PROTECTION RAM WILL BE SETUP TO ALLOW
11787 ;READS AND WRITES TO THE FIRST 128 WORDS OF MEMORY. THE FIRST 128
11788 ;WORDS OF MEMORY WILL BE MAPPED TO SELECT THE TARGET MEMORY. THE
11789 ;REMAINING LOCATIONS OF THE MAP PROTECTION RAM WILL BE MAPPED TO THE
11790 ;MEMORY SIMULATOR RAM AND SETUP TO INHIBIT READS AND WRITES TO THOSE
11791 ;LOCATIONS (777776-000400).
11792
11793 032616 005037 002254 CLR S4LOAD ;SETUP STARTING MSAD 15:0 BITS
11794 032622 012737 000010 002244 MOV #MSEL1,S2LOAD ;SETUP STARTING MSAD 17:16 BITS AND
11795 ;BITS TO SELECT MAP PROTECTION RAM
11796
11797 032630 1$: BGNSEG
11798 032630 104404 TRAP C$BSEG
11799
11800 ;SET THE SIGNAL MSEL1 H TO A ONE AND MSEL0 H TO A ZERO. THIS WILL
11801 ;CAUSE THE MAP PROTECTION RAM TO BE SELECTED VIA THE SIGNAL SMPM H
```



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11802                                     ;WHEN A READ OR WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6. MSAD
11803                                     ;BITS 17 AND 16 IN CONTROL REGISTER 2 WILL BE LOADED AND CHECKED FOR
11804                                     ;THE ADDRESS BEING TESTED.
11805
11806 032632 012737 177540 002250      MOV      #177540,S2MASK      ;SETUP TO IGNORE ESR H + WREN H
11807 032640 004737 010544             JSR      PC,LDRDS2         ;LOAD, READ AND CHECK CONTROL REG 2
11808 032644 001405                     BEQ      2$,               ;IF LOADED OK THEN CONTINUE
11809 032646                               ERRDF   2,S2EROR          ;CONTROL REG 2 NOT EQUAL EXPECTED
11810 032646 104455                     TRAP    C$ERDF
11811 032650 000002                       .WORD   2
11812 032652 000000                       .WORD   0
11813 032654 005320                       .WORD   S2EROR
11814 032656                               CKLOOP
11815 032656 104406                     TRAP    C$CLP1
11816
11817                                     ;LOAD, READ AND CHECK CONTROL REGISTER 4 FOR THE ADDRESS BEING TESTED.
11818                                     ;CONTROL REGISTER 4 CONTAINS BITS FOR MSAD ADDRESS BITS 15:0.
11819
11820 032660 004737 010604             2$:    JSR      PC,LDRDS4         ;LOAD, READ AND CHECK CONTROL REG 4
11821 032664 001405                     BEQ      3$,               ;IF LOADED OK THEN CONTINUE
11822 032666                               ERRDF   3,MSADRG,S4EROR  ;MSAD BITS 15:0 NOT EQUAL EXPECTED
11823 032666 104455                     TRAP    C$ERDF
11824 032670 000003                       .WORD   3
11825 032672 002506                       .WORD   MSADRG
11826 032674 005334                       .WORD   S4EROR
11827 032676                               CKLOOP
11828 032676 104406                     TRAP    C$CLP1
11829
11830                                     ;LOAD, READ AND CHECK MAP PROTECTION RAM LOCATION ADDRESSED BY MSAD
11831                                     ;BITS 17:0. ADDRESSES 0 TO 376 WILL BE LOADED AND CHECKED WITH A
11832                                     ;DATA PATTERN OF 16. ALL OTHER ADDRESSES WILL BE LOADED AND CHECKED
11833                                     ;WITH A DATA PATTERN OF 11.
11834
11835 032700 012737 177760 002264       3$:    MOV      #177760,S6MASK      ;SETUP TO IGNORE UNUSED BITS
11836 032706 012737 000011 002260      MOV      #MUTB!MPINH,S6LOAD ;SETUP FOR ADDRESSES OVER 376
11837 032714 032737 000003 002244      BIT      #MSAD17!MSAD16,S2LOAD ;CHECK IF ADDRESS ABOVE 16K WORDS
11838 032722 001006                     BNE     4$,               ;IF YES - LOAD R/W VIOLATION SETUP
11839 032724 005737 002254             TST     S4LOAD           ;CHECK IF ADDRESS WAS OVER 376
11840 032730 001003                     BNE     4$,               ;IF YES - LOAD R/W VIOLATION SETUP
11841 032732 012737 000016 002260      MOV      #MUTB!RDEH!WREH,S6LOAD ;SETUP TO ALLOW R/W TO FIRST 128 WORDS
11842 032740 004737 010630             4$:    JSR      PC,LDRDS6         ;LOAD, READ AND CHECK MAP PROTECT RAM
11843 032744 001405                     BEQ      5$,               ;IF LOADED OK THEN CONTINUE
11844 032746                               ERRDF   4,MSGMP,S6ALLR   ;MAP PROTECT RAM DATA ERROR
11845 032746 104455                     TRAP    C$ERDF
11846 032750 000004                       .WORD   4
11847 032752 002601                       .WORD   MSGMP
11848 032754 005454                       .WORD   S6ALLR
11849 032756                               CKLOOP
11850 032756 104406                     TRAP    C$CLP1
11851
11852                                     ;CHECK MAP PROTECTION RAM DATA BITS MPIN H AND WRE H IN CONTROL
11853                                     ;REGISTER 2 AS ESR H AND WREN H RESPECTIVELY.
11854
11855 032760 042737 000140 002250       5$:    BIC      #ESRH!WRENH,S2MASK ;SETUP TO CHECK ESR H AND WREN H
11856 032766 052737 000100 002246      BIS      #WRENH,S2GOOD    ;EXPECT WREN H TO BE A ONE
11857 032774 032737 000006 002260      BIT      #WREH!RDEH,S6LOAD ;CHECK IF RAM WAS W/R ENABLED

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11858 033002 001006          BNE      6$          ;IF YES THEN GO READ CONTROL REG 2
11859 033004 042737 000100 002246 BIC      #WRENH,S2GOOD ;THIS ADDRESS WAS NOT WRITE ENABLED
11860 033012 052737 000040 002246 BIC      #ESRH,S2GOOD  ;EXPECT ESR H TO BE SET TO A ONE
11861 033020 004737 010560 6$: JSR      PC,READS2   ;GO READ AND CHECK CONTROL REG 2
11862 033024 001404          BEQ      7$          ;IF OK THEN CONTINUE
11863 033026          ERRDF  2,MSGMPL,S2ALLR ;REGISTER 2 NOT EQUAL EXPECTED
11864 033026 104455          TRAP    C$ERRDF
11865 033030 000002          .WORD   2
11866 033032 002456          .WORD   MSGMPL
11867 033034 005440          .WORD   S2ALLR
11868 033036 7$:          ENDSEG
11869 033036 10001$:
11870 033036 104405          TRAP    C$ESEG
11871
11872          ;UPDATE CONTROL REGISTERS 4 AND 2 FOR MSAD ADDRESS TO BE TESTED
11873
11874 033040 062737 000400 002254 ADD      #MSAD8,S4LOAD ;UPDATE MSAD BITS 15:8 BY ONE
11875 033046 001270          BNE      1$          ;IF NOT 0 THEN LOAD NEXT RAM LOCATION
11876 033050 005237 002244          INC      S2LOAD     ;UPDATE MSAD BITS 17:16 BY ONE
11877 033054 032737 000004 002244 BIT      #MSELO,S2LOAD ;CHECK IF ALL RAM LOCATIONS DONE
11878 033062 001662          BEQ      1$          ;IF NOT THEN LOAD NEXT RAM LOCATION
11879 033064 005337 002244          DEC      S2LOAD     ;RESET REG 2 TO ACTUAL VALUE LOADED
11880
11881          ;SET THE SIGNAL CTS H TO A ONE IN CONTROL REGISTER 0. WHEN CTS H IS
11882          ;SET TO A ONE, THE SYSTEM BUS LATCHES WILL BE ENABLED TO THE MEMORY
11883          ;SIMULATOR MODULE.
11884
11885 033070 052737 000002 002234 BIS      #CTSH,S0LOAD ;SETUP BIT TO SET CTS H TO A ONE
11886 033076 004737 010504          JSR      PC,LDRDSO  ;GO LOAD, READ AND CHECK REG 0
11887 033102 001404          BEQ      8$          ;IF LOADED OK THEN CONTINUE
11888 033104          ERRDF  1,,SOEROR ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
11889 033104 104455          TRAP    C$ERRDF
11890 033106 000001          .WORD   1
11891 033110 000000          .WORD   0
11892 033112 005304          .WORD   SOEROR
11893 033114 8$:          ENDSEG
11894 033114 10000$:
11895 033114 104405          TRAP    C$ESEG
11896
11897 033116          BGNSEG
11898 033116 104404          TRAP    C$BSEG
11899
11900          ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11901          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11902
11903 033120 004737 012212          JSR      PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE
11904
11905 033124 005037 002352          CLR      T6MASK    ;RESET CONTROL REGISTER 6 MASK WORD
11906
11907          ;SET ADAL REGISTER BITS 14,10 AND 9 TO A ONE AND PULSE THE SIGNAL 'BRKRES L'
11908          ;BY TOGGLING ADAL REGISTER BIT 0. ADAL10 H AND ADAL9 H SET TO ONES WILL
11909          ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS. PULSING
11910          ;THE SIGNAL 'BRKRES L' VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
11911          ;TARGET EMULATOR MODULE. ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
11912          ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL 'CKAI H' TO BE PULSED VIA THE
11913          ;THE SIGNAL 'RASP L' LATER ON IN THIS TEST. ADAL REGISTER BIT 4 ON A

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TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE

SEQ 0230

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11914 ;ZERO WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE PAUSE MODE WHEN
11915 ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
11916
11917 033130 012737 043000 002334 MOV #ADAL14!ADAL10!ADAL9,T2LOAD ;SETUP BITS TO BE LOADED
11918 033136 004737 012764 JSR PC,BRKRES ;SET BITS 14, 10 + 9 AND TOGGLE ADALO H
11919
11920 ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
11921 ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
11922 ;REGISTER 6.
11923
11924 033142 004537 012232 JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
11925 033146 000003 .WORD HDAL ;SELECT THE HDAL REGISTER
11926
11927 ;SET HDAL REGISTER BITS 9, 6, 4 AND 2 TO A ONE AND HDAL BITS 14, 11, 5
11928 ;AND 3 TO A ZERO. HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO CONTROL
11929 ;THE T-11 TIMING AND CONTROL SIGNALS. HDAL9 H ON A ONE WILL ENABLE THE
11930 ;OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER TO THE SYSTEM ADDRESS BUS.
11931 ;HDAL14 H AND HDAL11 H ON A ZERO WILL SET SYSTEM ADDRESS BITS 17 AND 16
11932 ;TO A ZERO. HDAL4 H ON A ONE AND HDAL3 H ON A ZERO WILL SET PR/WHB L
11933 ;LOW AND PR/WLB L HIGH. PR/WLB L ASSERTED HIGH WILL CAUSE THE SIGNAL
11934 ;DTLB L TO BE ASSERTED LOW LATER ON IN THE TEST WHEN SOME OTHER GATING
11935 ;SIGNALS ARE ASSERTED HIGH. DTHB L WILL ALSO BE ASSERTED LOW AS A RESULT
11936 ;OF DMG L, PBCLR L, AND MR11 H BEING ASSERTED HIGH. THE SIGNALS DTLB L AND
11937 ;DTHB L ASSERTED LOW WILL ENABLE THE CDAL BUS TO THE TDAL BUS. HDAL5 H ON A
11938 ;ZERO AND HDAL6 H ON A ONE WILL CAUSE THE SIGNAL PSELO L TO BE ASSERTED
11939 ;HIGH AND PSEL1 L TO BE ASSERTED LOW. PSEL1 L SET LOW WILL DISABLE ONE
11940 ;OF THE DATA PATHS TO THE TDAL BUS. WITH PSELO L SET HIGH AND PSEL1 L
11941 ;SET LOW, THE SIGNAL INTER L WILL BE ASSERTED LOW THUS ENABLING FDAL
11942 ;REGISTER BITS 7:2 TO THE EODAL BUS AND CLEARING THE EOAI REGISTER.
11943
11944 033150 012737 001124 002346 MOV #HDAL9!HDAL6!HDAL4!HDAL2,T6LOAD ;SET HDAL BITS 9, 6, 4 AND 2 TO 1'S
11945 033156 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK HDAL REGISTER
11946 033162 001405 BEQ 9$ ;IF LOADED OK THEN CONTINUE
11947 033164 ERRDF 12,HDALRG,T06ERR ;HDAL REGISTER NOT EQUAL EXPECTED
11948 033164 104455 TRAP C$ERDF
11949 033166 000014 .WORD 12
11950 033170 003754 .WORD HDALRG
11951 033172 006730 .WORD T06ERR
11952 033174 CKLOOP
11953 033174 104406 TRAP C$CLP1
11954
11955 ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
11956 ;REGISTER 4. PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
11957 ;FLIP-FLOPS ON THE MODULE NOT CLEARED BY THE SIGNAL "BRKRES L". SET
11958 ;THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE.
11959 ;ON A READ COMMAND TO CONTROL REGISTER 4, THE SIGNAL BTS1 H WILL BE SET
11960 ;TO A ONE AS A RESULT OF THE SIGNAL INTER L BEING ASSERTED LOW. THE
11961 ;SIGNAL INTER L IS ASSERTED LOW AS A RESULT OF PSELO L BEING ASSERTED
11962 ;HIGH AND PSEL1 L BEING ASSERTED LOW.
11963
11964 033176 012737 000204 002340 9$: MOV #VDAL7!VDAL2,T4LOAD ;SETUP BITS TO BE LOADED
11965 033204 013737 002340 002342 MOV T4LOAD,T4GOOD ;COPY LOADED TO EXPECTED
11966 033212 052737 000040 002342 BIS #VDAL5,T4GOOD ;EXPECT BTS1 H TO BE A ONE
11967 033220 004737 011170 JSR PC,LDRD4T ;GO LOAD, READ AND CHECK VDAL REG
11968 033224 001405 BEQ 10$ ;IF OK THEN CONTINUE
11969 033226 ERRDF 11,VDALRG,T4EROR ;VDAL REG NOT EQUAL TO EXPECTED

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SEQ 0231

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11970 033226 104455 TRAP C$ERDF
11971 033230 000013 .WORD 11
11972 033232 003706 .WORD VDALRG
11973 033234 006714 .WORD T4EROR
11974 033236 CKLOOP
11975 033236 104406 TRAP C$CLP1
11976 033240 042737 000004 002340 10$: BIC #VDAL2,T4LOAD ;SET VDAL2 H TO THE LOW STATE
11977 033246 042737 000004 002342 BIC #VDAL2,T4GOOD ;SETUP TO EXPECT IT TO BE ZERO
11978 033254 004737 011170 JSR PC,LDRD4T ;GO LOAD, READ AND CHECK VDAL REG
11979 033260 001405 BEQ 11$ ;IF OK THEN CONTINUE
11980 033262 ERRDF 11,VDALRG,T4EROR ;VDAL REG NOT EQUAL TO EXPECTED
11981 033262 104455 TRAP C$ERDF
11982 033264 000013 .WORD 11
11983 033266 003706 .WORD VDALRG
11984 033270 006714 .WORD T4EROR
11985 033272 CKLOOP
11986 033272 104406 TRAP C$CLP1
11987
11988 ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4. ON
11989 ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
11990 ;BE WRITTEN OR READ.
11991
11992 033274 004537 012232 11$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
11993 033300 000004 .WORD MODE ;SELECT THE MODE REGISTER
11994
11995 ;LOAD, READ AND CHECK THE MODE REGISTER WITH MR11 H SET TO A ONE AND
11996 ;ALL OTHER MODE REGISTER BITS SET TO A ZERO. MODE REGISTER BIT 11 SET
11997 ;TO A ONE WILL SET THE TARGET EMULATOR MODULE TO 8 BIT MODE.
11998
11999 033302 012737 004000 002346 MOV #MR11,T6LOAD ;SETUP BIT TO SET MR11 H TO HIGH STATE
12000 033310 004737 011214 JSR PC,LDRDT6 ;GO LOAD, READ AND CHECK MODE REGISTER
12001 033314 001405 BEQ 12$ ;IF LOADED OK THEN CONTINUE
12002 033316 ERRDF 12,MODREG,T06ERR ;MODE REGISTER NOT EQUAL EXPECTED
12003 033316 104455 TRAP C$ERDF
12004 033320 000014 .WORD 12
12005 033322 004000 .WORD MODREG
12006 033324 006730 .WORD T06ERR
12007 033326 CKLOOP
12008 033326 104406 TRAP C$CLP1
12009
12010 ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
12011 ;TO A 2. THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
12012 ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
12013 ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
12014 ;TER WILL BE ADDRESSED.
12015
12016 033330 004537 012232 12$: JSR R5,SELTER ;SELECT REGISTER SPECIFIED BY NEXT WORD
12017 033334 000002 .WORD FDAL ;SELECT EOAI AND FDAL REGISTER
12018
12019 ;LOAD, READ AND CHECK THE FDAL AND EOAI REGISTER. THE EOAI REGISTER
12020 ;WILL BE HELD CLEARED BY THE SIGNAL INTER L BEING ASSERTED LOW. TO
12021 ;CHECK THIS, THE PROGRAM WILL ATTEMPT TO LOAD ALL ONES INTO THE EOAI
12022 ;REGISTER. ALL ZEROES SHOULD BE READ BACK FROM THE EOAI REGISTER WHEN
12023 ;THE SIGNAL INTER L IS HELD LOW. THE FDAL REGISTER WILL BE LOADED AND
12024 ;CHECKED WITH A DATA PATTERN OF 251. FDALO H ON A ONE WILL ENABLE THE
12025 ;EOAI REGISTER TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 INSTEAD

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SEQ 0233

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12082
12083 033444 004537 012232      15$: JSR    R5,SELTERR      ;SELECT REGISTER SPECIFIED BY NEXT WORD
12084 033450 000003              .WORD  HDAL              ;SELECT THE HDAL REGISTER
12085
12086 033452 012737 001124 002346  MOV    #HDAL9!HDAL6!HDAL4!HDAL2,T6LOAD ;BITS THAT WERE PREVIOUSLY LOADED
12087
12088 ;SET THE SIGNALS XRAS H AND PRAS H TO THE HIGH STATES BY SETTING HDAL12 H
12089 ;TO A ONE. WHEN XRAS H IS SET HIGH, THE PAUSE MODE FLIP-FLOP, THE
12090 ;EDFET FLIP-FLOP, AND THE BTSET FLIP-FLOP WILL BE CLOCKED TO ONES.
12091 ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE AS A
12092 ;RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH. SOP H IS ASSERTED
12093 ;HIGH WHEN THE SIGNAL PAUSE L IS ASSERTED HIGH (PAUSE MODE). WHEN
12094 ;PRAS H IS SET HIGH, THE ADDRESS BUS, WHICH CONTAINS THE DIAGNOSTIC
12095 ;ADDRESS REGISTER DATA, WILL BE CLOCKED INTO THE MEMORY SIMULATORS
12096 ;SYSTEM ADDRESS BUS LATCHES. SELECTING ADDRESS ZERO ON THE MEMORY
12097 ;SIMULATOR MODULE WILL CAUSE THE SIGNALS ETR H AND WVIOL L TO BE
12098 ;ASSERTED HIGH.
12099
12100 033460 004737 012276      JSR    PC,XRASH          ;SET XRAS H AND PRAS H TO THE HIGH STATE
12101
12102 ;READ THE VDAL REGISTER AND CHECK THAT THE SIGNAL PSMW H IS ASSERTED
12103 ;HIGH AS A RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH.
12104
12105 033464 052737 001000 002342  BIS    #VDAL9,T4GOOD    ;EXPECT PSMW H TO BE A ONE
12106 033472 004737 011176      JSR    PC,READT4        ;READ AND CHECK VDAL REGISTER
12107 033476 001405              BEQ    16$              ;IF OK THEN CONTINUE
12108 033500              ERRDF  11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
12109 033500 104455              TRAP  C$ERDF
12110 033502 000013              .WORD  11
12111 033504 003706              .WORD  VDALRG
12112 033506 006714              .WORD  T4EROR
12113 033510              CKLOOP
12114 033510 104406              TRAP  C$CLP1
12115
12116 ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
12117 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
12118
12119 033512 004737 011246      16$: JSR    PC,SLCTMS
12120
12121 ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED AS A RESULT
12122 ;OF CLOCKING THE SYSTEM ADDRESS BUS INTO THE MEMORY SIMULATOR SYSTEM
12123 ;ADDRESS BUS LATCHES.
12124
12125 033516 004737 010520      JSR    PC,READS0        ;READD AND CHECK CONTROL REISTER 0
12126 033522 001405              BEQ    17$              ;IF OK THEN CONTINUE
12127 033524              ERRDF  1,SOEROR        ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
12128 033524 104455              TRAP  C$ERDF
12129 033526 000001              .WORD  1
12130 033530 000000              .WORD  0
12131 033532 005304              .WORD  SOEROR
12132 033534              CKLOOP
12133 033534 104406              TRAP  C$CLP1
12134
12135 ;READ CONTROL REGISTER 4 TO CHECK THAT ADDRESS 0 WAS CLOCKED INTO THE
12136 ;SYSTEM ADDRESS BUS LATCHES. WHEN CTS H IS ASSERTED HIGH, THE SYSTEM
12137 ;ADDRESS BUS LATHCES ARE ENABLED TO MSAD BITS 17:0

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SEQ 0234

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12138
12139 033536 005037 002254      17$: CLR      S4LOAD      ;SETUP TO EXPECT ADDRESS TO BE 0
12140 033542 004737 010612      JSR      PC,READS4   ;READ AND CHECK MSAD 15:0
12141 033546 001405                BEQ      18$         ;IF OK THEN CONTINUE
12142 033550                ERRDF    3,MSADRG,S04ERR ;MSAD 15:0 SYSTEM ADDRESS BUS LATCH ERROR
12143 033550 104455                TRAP    C$ERDF
12144 033552 000003                .WORD   3
12145 033554 002506                .WORD   MSADRG
12146 033556 005404                .WORD   S04ERR
12147 033560                CKLOOP
12148 033560 104406                TRAP    C$CLP1
12149
12150                ;READ CONTROL REGISTER 2 TO CHECK THAT MSAD BITS 17 AND 16 ARE ZERO AND
12151                ;THAT THE SIGNALS ESR H AND MSBRK H ARE ZERO. THE SIGNAL WREN H SHOULD
12152                ;BE ASSERTED HIGH BECAUSE THE MAP PROTECTION RAM WAS SETUP TO ALLOW
12153                ;READS AND WRITES TO ADDRESSES 0-376.
12154
12155 033562 052737 000014 002250 18$: BIS      #MSEL1!MSEL0,S2MASK ;SETUP TO IGNORE TRI-STATE BIT
12156 033570 012737 000010 002244      MOV      #MSEL1,S2LOAD ;SETUP PREVIOUSLY LOADED BIT
12157 033576 012737 000100 002246      MOV      #WRENH,S2GOOD ;EXPECT WREN H TO BE ASSERTED HIGH
12158 033604 004737 010560                JSR      PC,READS2   ;READ AND CHECK CONTROL REGISTER 2
12159 033610 001405                BEQ      19$         ;IF OK THEN CONTINUE
12160 033612                ERRDF    2,S2EROR    ;CONTROL REGISTER 2 NOT EQUAL EXPECTED
12161 033612 104455                TRAP    C$ERDF
12162 033614 000002                .WORD   2
12163 033616 000000                .WORD   0
12164 033620 005320                .WORD   S2EROR
12165 033622                CKLOOP
12166 033622 104406                TRAP    C$CLP1
12167
12168                ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
12169                ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
12170
12171 033624 004737 012212      19$: JSR      PC,SLCTTE    ;SELECT THE TARGET EMULATOR MODULE
12172
12173                ;SELECT THE EODAL BUS BY SETTING GDDAL BITS 2:0 TO A 7. ON A READ
12174                ;COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE READ VIA THE
12175                ;SIGNAL RPT7 L.
12176
12177 033630 004537 012232                JSR      R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
12178 033634 000007                .WORD   EODAL       ;SELECT THE EODAL BUS TO BE READ
12179
12180                ;AT THIS POINT IN TIME, FDAL REGISTER BITS 7:2 SHOULD BE ENABLED TO THE
12181                ;EODAL BUS VIA THE SIGNAL INTER L. THE FDAL REGISTER WAS LOADED
12182                ;PREVIOUSLY WITH A DATA PATTERN OF 251. WHEN READ ON THE EODAL BUS,
12183                ;BITS 1 AND 0 WILL BE READ AS A ZERO.
12184
12185 033636 012737 000250 002346      MOV      #250,T6LOAD ;SETUP EXPECTED FDAL DATA TO EODAL BUS
12186 033644 012737 177400 002352      MOV      #177400,T6MASK ;SETUP TO IGNORE TRI-STATE HIGH BYTE
12187 033652 004737 011222                JSR      PC,READT6   ;READ AND CHECK THE EODAL BUS
12188 033656 001405                BEQ      20$         ;IF OK THEN CONTINUE
12189 033660                ERRDF    12,FDEODL,T6ALLR ;FDAL REG 7:2 TO EODAL BUS ERROR
12190 033660 104455                TRAP    C$ERDF
12191 033662 000014                .WORD   12
12192 033664 004605                .WORD   FDEODL
12193 033666 006744                .WORD   T6ALLR

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SEQ 0235

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12194 033670          CKLOOP
12195 033670 104406   TRAP    C$CLP1
12196
12197
12198                ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
12199                ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
12200                ;REGISTER 6.
12201 033672 004537 012232      20$:   JSR     R5,SELTERR        ;SELECT REGISTER SPECIFIED BY NEXT WORD
12202 033676 000003                .WORD  HDAL              ;SELECT THE HDAL REGISTER
12203
12204 033700 012737 011124 002346   MOV     #HDAL12!HDAL9!HDAL6!HDAL4!HDAL2,T6LOAD ;BITS PREVIOUSLY SET
12205 033706 005037 002352                CLR     T6MASK          ;CLEAR CONTROL REGISTER 6 MASK WORD
12206
12207                ;TO ENABLE THE EODAL BUS TO THE CDAL BUS THE PROGRAM MUST SET THE SIGNAL
12208                ;PPI H TO THE HIGH STATE BY SETTING HDAL15 H TO A ONE.  WHEN PPI H,
12209                ;PSMW H, AND MR11 H ARE ASSERTED HIGH, THE SIGNAL COLB L WILL BE ASSERTED
12210                ;LOW THUS ENABLING THE LOW BYTE OF THE EODAL BUS TO THE CDAL BUS.
12211                ;THE EODAL BUS PRESENTLY CONTAINS DATA FROM FDAL REGISTER BITS 7:2 (250).
12212                ;THE CDAL BUS WILL UNCONDITIONALLY BE ENABLED TO THE EIDAL BUS.  THE CDAL
12213                ;BUS WILL ALSO BE ENABLED TO THE TDAL BUS BY THE SIGNALS DTHB L AND
12214                ;DTLB L BEING ASSERTED LOW.  THESE TWO SIGNALS ARE ASSERTED LOW AS A
12215                ;RESULT OF WVIOL L, ETR H, PR/WLB L, MR11 H, PBCLR L, AND PSELO L BEING
12216                ;ASSERTED HIGH.
12217
12218 033712 004737 012505                JSR     PC,XPIH          ;SET XPI H AND PPI H TO THE HIGH STATE
12219
12220                ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  ON A READ
12221                ;COMMAND TO CONTROL REGISTER 6, THE EIDAL BUS WILL BE READ VIA RPT6 L.
12222
12223 033716 004537 012232                JSR     R5,SELTERR        ;SELECT REG SPECIFIED BY NEXT WORD
12224 033722 000006                .WORD  EIDAL            ;SELECT THE EIDAL BUS TO BE READ
12225
12226                ;AT THE PRESENT TIME DATA FROM FDAL REGISTER BITS 7:2 (250) ARE ENABLED
12227                ;TO THE EODAL BUS, THE CDAL BUS, THE EIDAL BUS AND THE TDAL BUS VIA
12228                ;THE SIGNALS INTER L, COLB L, DTHB L AND DTLB L.  THE FOLLOWING SECTION
12229                ;WILL READ THE EIDAL BUS TO CHECK THAT THE FDAL REGISTER DATA IS ENABLED
12230                ;TO IT VIA THE EODAL AND CDAL BUSES.
12231
12232 033724 012737 000250 002346   MOV     #250,T6LOAD      ;SETUP EXPECTED FDAL TO EIDAL BUS DATA
12233 033732 012737 177400 002352   MOV     #177400,T6MASK   ;SETUP TO IGNORE TRI-STATE HIGH BYTE
12234 033740 004737 011222                JSR     PC,READT6        ;READ AND CHECK EIDAL BUS DATA
12235 033744 001405                BEQ     21$              ;IF DATA OK THEN CONTINUE
12236 033746                ERRDF  12,FDEIDL,T6ALLR ;FDAL REG 7:2 TO EIDAL BUS ERROR VIA CDAL
12237 033746 104455                TRAP   C$ERRDF
12238 033750 000014                .WORD  12
12239 033752 004645                .WORD  FDEIDL
12240 033754 006744                .WORD  T6ALLR
12241 033756                CKLOOP
12242 033756 104406                TRAP   C$CLP1
12243
12244                ;AT THE PRESENT TIME DATA FROM FDAL REGISTER BITS 7:2 (250) ARE ENABLED
12245                ;TO THE EODAL BUS, THE CDAL BUS, THE EIDAL BUS AND THE TDAL BUS VIA THE
12246                ;SIGNALS INTER L, COLB L, DTHB L, AND DTLB L.  TO CHECK
12247                ;THAT FDAL REGISTER BITS 7:2 (250) ARE ENABLED TO THE TDAL BUS, THE
12248                ;PROGRAM MUST CLOCK THE DATA INTO THE TDAL DIAGNOSTIC LATCHES FIRST SO
12249                ;THAT THE DATA CAN BE READ BACK LATER ON IN THIS TEST.  TO CLOCK THE

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TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE

SEQ 0236

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12250                                     ;DATA INTO THE TDAL LATCHES, THE PROGRAM MUST SET THE SIGNAL VDAL2 H TO
12251                                     ;A ONE AND THEN ZERO. PULSING THE SIGNAL VDAL2 H WILL CAUSE A PULSE ON
12252                                     ;THE SIGNAL "INVD L" WHICH WILL CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS,
12253                                     ;THE EDFET AND BTJET FLIP-FLOPS. WITH THESE FLIP-FLOPS CLEARED, THE
12254                                     ;FDAL REGISTER DATA WILL BE DISABLED FROM THE CDAL BUS, THE EIDAL BUS AND
12255                                     ;THE TDAL BUS. THE SIGNAL FETCT H WILL ALSO BE SET TO A ZERO IN THE
12256                                     ;FOLLOWING SECTION.
12257
12258 033760 012737 000004 002340 21$:  MOV    #VDAL2,T4LOAD      ;SET FETCT H LOW AND SET VDAL2 H HIGH
12259 033766 013737 002340 002342      MOV    T4LOAD,T4GOOD      ;COPY DATA LOADED TO EXPECTED
12260 033774 052737 000040 002342      BIS    #VDAL5,T4GOOD      ;EXPECT BTS1 H TO BE A 1 VIA INTER L
12261 034002 004737 011170              JSR    PC,LDRD4T          ;LOAD, READ AND CHECK VDAL REGISTER
12262 034006 001405                      BEQ    22$                ;IF LOADED OK THEN CONTINUE
12263 034010                                ERRDF  11,VDALRG,T4EROR   ;VDAL REGISTER NOT EQUAL EXPECTED
12264 034010 104455                      TRAP   C$ERRDF
12265 034012 000013                      .WORD  11
12266 034014 003706                      .WORD  VDALRG
12267 034016 006714                      .WORD  T4EROR
12268 034020                                CKLOOP
12269 034020 104406                      TRAP   C$CLP1
12270 034022 042737 000004 002340 22$:  BIC    #VDAL2,T4LOAD      ;SETUP TO SET VDAL2 H LOW
12271 034030 042737 000004 002342      BIC    #VDAL2,T4GOOD      ;SETUP TO EXPECT VDAL2 H TO BE A 0
12272 034036 004737 011170              JSR    PC,LDRD4T          ;LOAD, READ AND CHECK VDAL REGISTER
12273 034042 001405                      BEQ    23$                ;IF LOADED OK THEN CONTINUE
12274 034044                                ERRDF  11,VDALRG,T4EROR? ;VDAL REGISTER NOT EQUAL EXPECTED
12275 034044 104455                      TRAP   C$ERRDF
12276 034046 000013                      .WORD  11
12277 034050 003706                      .WORD  VDALRG
12278 034052 006714                      .WORD  T4EROR
12279 034054                                CKLOOP
12280 034054 104406                      TRAP   C$CLP1
12281
12282                                     ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3. THE HDAL
12283                                     ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
12284                                     ;REGISTER 6.
12285
12286 034056 004537 012232          23$:  JSR    R5,SELTERR        ;SELECT REGISTER SPECIFIED BY NEXT WORD
12287 034062 000003              .WORD  HDAL              ;SELECT THE HDAL REGISTER
12288
12289                                     ;THE FOLLOWING SECTION WILL SET THE SIGNALS XRAS H AND PPI H TO THE
12290                                     ;LOW STATE BY CLEARING HDAL REGISTER BITS 15 AND 12.
12291
12292 034064 012737 111124 002346      MOV    #HDAL15!HDAL12!HDAL9!HDAL6!HDAL4!HDAL2,T6LOAD ;LOADED BITS
12293 034072 005037 002352              CLR    T6MASK            ;SETUP MASK WORD TO CHECK ALL BITS
12294 034076 004737 012540              JSR    PC,XPIL           ;SET XPI H AND PPI H LOW
12295 034102 004737 012330              JSR    PC,XRASL          ;SET XRAS H AND PRAS H LOW
12296
12297                                     ;SET HDAL BIT 4 TO A ZERO AND HDAL BIT 3 TO A ONE TO SET PR/WHB L HIGH
12298                                     ;AND PR/WLB L LOW.
12299
12300 034106 042737 000020 002346      BIC    #HDAL4,T6LOAD      ;SET PR/WHB L HIGH
12301 034114 052737 000010 002346      BIS    #HDAL3,T6LOAD      ;SET PR/WLB L LOW
12302 034122 004737 011214              JSR    PC,LDRDT6         ;LOAD, READ AND CHECK THE HDAL REGISTER
12303 034126 001405                      BEQ    24$                ;IF LOADED OK THEN CONTINUE
12304 034130                                ERRDF  12,HDALRG,T06ERR  ;HDAL REGISTER NOT EQUAL EXPECTED
12305 034130 104455                      TRAP   C$ERRDF

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TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE

SEQ 0237

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12306 034132 000014 .WORD 12
12307 034134 003754 .WORD HDALRG
12308 034136 006730 .WORD T06ERR
12309 034140 CKLOOP
12310 034140 104406 TRAP C$CLP1
12311
12312 ;SET THE SIGNAL VDALO H TO A ONE TO ENABLE THE OUTPUTS OF THE TDAL
12313 ;DIAGNOSTIC LATCHES ONTO THE TDAL BUS. THE TDAL LATCHES WERE LOADED
12314 ;WITH DATA FROM FDAL REGISTER BITS 7:2 (250) EARLIER IN THIS TEST.
12315
12316 034142 052737 000001 002340 24$: BIS #VDALO,T4LOAD ;SETUP BIT TO BE LOADED
12317 034150 052737 000001 002342 BIS #VDALO,T4GOOD ;EXPECT VDALO H TO BE SET ON READ
12318 034156 004737 011170 JSR PC,LDRD4T ;LOAD, READ AND CHECK VDAL REGISTER
12319 034162 001405 BEQ 25$ ;IF LOADED OK THEN CONTINUE
12320 034164 ERRDF 11,VDALRG,T4EROR ;VDAL REGISTER NOT EQUAL EXPECTED
12321 034164 104455 TRAP C$ERDF
12322 034166 000013 .WORD 11
12323 034170 003706 .WORD VDALRG
12324 034172 006714 .WORD T4EROR
12325 034174 CKLOOP
12326 034174 104406 TRAP C$CLP1
12327
12328 ;THE FOLLOWING SIGNALS ETR H, MR11 H, PR/WHB L, AND PSMW L
12329 ;SHOULD BE ASSERTED HIGH. THEREFORE, BY SETTING PPI H TO THE HIGH
12330 ;STATE, THE SIGNAL DBLB L SHOULD BE ASSERTED LOW.. THIS
12331 ;SIGNAL WILL ENABLE THE TDAL BUS, WHICH HAS THE TDAL DIAGNOSTIC
12332 ;LATCHES ENABLED TO IT, TO THE CDAL BUS AND THE CDAL BUS WILL BE ENABLED
12333 ;TO THE EIDAL BUS UNCONDITIONALLY. THE TDAL LATCHES WERE LOADED EARLIER
12334 ;IN THIS TEST WITH DATA FROM FDAL REGISTER BITS 7:2 (250).
12335
12336 034176 004737 012506 25$: JSR PC,XPIH ;SET XPI H AND PPI H TO HIGH STATE
12337
12338 ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6. ON A READ
12339 ;COMMAND TO CONTROL REGISTER 6, THE EIDAL BUS WILL BE READ VIA THE
12340 ;SIGNAL RPT6 L.
12341
12342 034202 004537 012232 JSR R5,SELTERR ;SELECT REGISTER SPECIFIED BY NEXT WORD
12343 034206 000006 .WORD EIDAL ;SELECT THE EIDAL BUS TO BE READ
12344
12345 ;AT THE PRESENT TIME THE TDAL DIAGNOSTIC LATCHES ARE ENABLED TO THE
12346 ;TDAL BUS, THE CDAL BUS AND THE EIDAL BUS VIA THE SIGNALS VDALO H,
12347 ;DBLB L. THE TDAL LATCHES WERE LOADED EARLIER IN THE TEST
12348 ;WITH DATA FROM FDAL REGISTER BITS 7:2 (250). THE PROGRAM WILL
12349 ;NOW READ THE EIDAL BUS TO CHECK THAT FDAL REGISTER BITS 7:2 DATA
12350 ;(250) WAS LOADED INTO THE TDAL LATCHES AND THAT THE TDAL LATCHES
12351 ;ARE ENABLED TO THE EIDAL BUS.
12352
12353 034210 012737 000250 002346 MOV #250,T6LOAD ;SETUP EXPECTED FDAL TO EIDAL BUS DATA
12354 034216 012737 177400 002352 MOV #177400,T6MASK ;SETUP TO IGNORE TRI-STATE HIGH BYTE
12355 034224 004737 011222 JSR PC,READT6 ;READ AND CHECK THE EIDAL BUS
12356 034230 001405 BEQ 26$ ;IF DATA OK THEN CONTINUE
12357 034232 ERRDF 12,FDTDEI,T6ALLR ;FDAL TO TDAL LATCHES TO EIDAL BUS ERROR
12358 034232 104455 TRAP C$ERDF
12359 034234 000014 .WORD 12
12360 034236 004705 .WORD FDTDEI
12361 034240 006744 .WORD T6ALLR
    
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TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE

SEQ 0238

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12362 034242          CKLOOP
12363 034242 104406  TRAP   C$CLP1
12364
12365                ;SELECT THE HDAL REGISER BY SETTING DGAL BITS 2:0 TO A 3. THE HDAL
12366                ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
12367                ;CONTROL REGISTER 6.
12368
12369 034244 004537 012232      26$: JSR   R5,SELTER          ;SELECT REGISTER SPECIFIED BY NEXT WORD
12370 034250 000003          .WORD  HDAL          ;SELECT THE HDAL REGISTER
12371
12372 034252 012737 101014 002346  MOV   #HDAL15!HDAL9!HDAL3!HDAL2,T6LOAD ;BIT LOADED BEFORE - HDAL6 H
12373 034260 005037 002352          CLR   T6MASK          ;SETUP MASK TO CHECK ALL BITS
12374
12375                ;SET THE SIGNALS XPI H AND PPI H TO THE LOW STATE BY CLEARING HDAL
12376                ;REGISTER BIT 15. ALOS SET THE SIGNAL PSEL1 L TO THE HIGH STATE BY
12377                ;SETTING HDAL REGISTER BIT 6 TO A 0.
12378
12379 034264 004737 012540      JSR   PC,XPIL          ;SET XPI H AND PPI H TO LOW STATE
12380
12381                ;ISSUE A PULSE ON THE SIGNAL "INVD L" TO RE-INITIALIZE THE MODULE.
12382
12383 034270 005037 002340      CLR   T4LOAD          ;SETUP TO CLEAR ALL BITS
12384 034274 004737 012704      JSR   PC,CLRPSM       ;GO PULSE INVD L VIA VDAL2 H
12385
12386 034300          ENDSEG
12387 034300          10002$:
12388 034300 104405          TRAP  C$ESEG
12389
12390 034302          ENDTST
12391 034302          L10050:
12392 034302 104401          TRAP  C$ETST
12393

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034304 004737 007436
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034310 104404
034312 004737 012142
034316 105037 002272
034322 004737 010676
034326 001405
034330
034330 104455
034332 000005
034334 003006
034336 006144
034340 104406

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.SBTTL TEST 13: CHECK SA SIGNAL 'EDBRK H' TO TE MODULE

:++
: THIS TEST WILL CHECK THAT STATE ANALYZER SIGNAL 'EDBRK H' CAN BE ASSERTED HIGH
: AND LOW WHEN STATE ANALYZER'S FUNCTION SELECT FLIP-FLOP 'FUSL2' IS CLEARED AND
: SET. THE OUTPUT OF FUNCTION SELECT FLIP-FLOP 'FUSL2' IS ENABLED TO THE SYSTEM
: BUS WHEN THE SIGNAL 'CDAL1 H' IS ASSERTED HIGH. THE PROGRAM WILL CHECK THAT
: THE SIGNAL 'EDBRK H' IS ASSERTED HIGH AND LOW BY READING THIS SIGNAL IN THE
: TARGET EMULATOR'S CONTROL REGISTER 0. THE TEST WILL ALSO CHECK THAT THE SIGNAL
: 'EDBRK H' WILL CAUSE THE TARGET EMULATOR'S PAUSE STATE LOGIC TO BE ENTERED IN
: 'RUN' MODE WHEN THE SIGNAL 'FETCT H' IS ASSERTED HIGH AND A PULSE IS ISSUED ON
: THE SIGNAL 'XRAS H'.
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T13:: BGNTST

JSR PC,INITMD ;INITIALIZE THE SYSTEM MODULES

BGNSEG
TRAP C$BSEG

;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER

JSR PC,SLCTED ;SELECT THE STATE ANALYZER MODULE

;CLEAR LOW BYTE OF CONTROL REGISTER 0. CDAL7 H BEING SET TO A ZERO
;WILL ENBALE THE OUTPUTS OF THE OR ADDRESS REGISTER TO ORAD 3:0.
;CDAL4 H ON A ZERO WILL ENABLE ONLY ONE AND/OR ARRAY RAM TO BE SELECTED
;AT ONE TIME VIA THE POINTER REGISTER. IN THIS TEST PTER15 L WILL
;SELECT THE OR ARRAY RAM. CDAL1 H ON A ZERO WILL DISABLE THE SIGNAL
;FUSL2 H TO THE SYSTEM BUS SIGNAL EDBRK H.

CLRB EOLOAD ;SETUP TO CLEAR LOW BYTE
JSR PC,LDRDEO ;LOAD, READ AND CHECK CDAL REGISTER
BEQ 1$ ;IF LOADED OK THEN CONTINUE
ERRDF 5,CDALRG,EOEROR ;CDAL REGISTER NOT EQUAL EXPECTED
TRAP C$ERDF
.WORD 5
.WORD CDALRG
.WORD EOEROR
CKLOOP
TRAP C$CLP1

;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER BY LOADING THE
;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER. ON A WRITE
;OR READ COMMAND OT CONTROL REGISTER 6 WHEN PTER15 L IS ASSERTED, THE
;OR ADDRESS REGISTER WILL BE WRITTEN OR READ. PDAL REGISTER BIT 5 WILL
;REMAIN A ZERO TO HOLD THE FLIP-FLOP'S FUSL7 AND FUSL 3:0 TO THE PRESET
;STATE.

1$: JSR R5,LDPDAL ;LOAD AND CHECK PDAL REG WITH NEXT WORD
.WORD PTER15 ;SETUP TO WRITE/READ OR ADDRESS REG

;LOAD, READ AND CHECK THE OR ADDRESS REGISTER WITH A DATA PATTERN OF ALL
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12450 ;ZER0ES WHICH WILL CAUSE ADDRESS ZERO OF THE OR ARRAY RAM TO BE SELECTED.
12451 ;ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L
12452 ;ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H WHICH WILL LOAD
12453 ;THE 'OR ADDRESS REGISTER'. ON A READ COMMAND TO CONTROL REGISTER 6
12454 ;WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL
12455 ;RPT15 H WHICH WILL READ THE DATA FROM THE 'OR ADDRESS REGISTER'.
12456
12457 034350 005037 002316 CLR E6LOAD ;SETUP TO LOAD ALL ZEROES
12458 034354 012737 177760 002320 MOV #177760,E6MASK ;SETUP TO IGNORE UNWANTED BITS
12459 034362 004737 011044 JSR PC,LDRDE6 ;LOAD, READ AND CHECK 'OR ADDRESS REG'
12460 034366 001405 BEQ 2$ ;IF LOADED OK THEN CONTINUE
12461 034370 ERRDF 8,ORADER,E026ER ;'OR ADDRESS REG' ERKOR ORAD 3:0
12462 034370 104455 TRAP C$ERDF
12463 034372 000010 .WORD 8
12464 034374 003545 .WORD ORADER
12465 034376 006210 .WORD E026ER
12466 034400 CKLOOP
12467 034400 104406 TRAP C$CLP1
12468
12469 ;LOAD READ AND CHECK THE OR ARRAY RAM ADDRESSED BY THE OR ADDRESS
12470 ;REGISTER WITH A DATA PATTERN OF 004. THE SIGNALS OR07 L TO OR03 L
12471 ;AND OR01 L TO OR00 L WILL BE ASSERTED HIGH AND THE SIGNAL OR02 L
12472 ;WILL BE ASSERTED LOW.
12473
12474 034402 012737 000004 002304 2$: MOV #4,E4LOAD ;SETUP DATA TO BE LOADED
12475 034410 012737 177400 002310 MOV #177400,E4MASK ;SETUP MASK TO IGNORE UNWANTED BITS
12476 034416 004737 010776 JSR PC,LDRDE4 ;LOAD, READ AND CHECK OR ARRAY RAM
12477 034422 001405 BEQ 3$ ;IF LOADED OK THEN CONTINUE
12478 034424 ERRDF 7,ORDATA,E4EROR ;'OR ARRAY RAM' DATA ERROR
12479 034424 104455 TRAP C$ERDF
12480 034426 000007 .WORD 7
12481 034430 003055 .WORD ORDATA
12482 034432 006174 .WORD E4EROR
12483 034434 CKLOOP
12484 034434 104406 TRAP C$CLP1
12485
12486 ;DISABLE THE PRESET SIGNAL TO THE FUNCTION SELECT FLIP-FLOPS FUSL7,
12487 ;FUSL3, FUSL2, FUSL1 AND FUSL0 BY SETTING PDALS H TO A ONE. THE BITS
12488 ;TO ASSERT THE SIGNAL PTER15 L LOW WILL ALSO REMAIN SET.
12489
12490 034436 004537 012162 3$: JSR R5,LDPDAL ;LOAD READ + CHECK PDAL WITH NEXT WORD
12491 034442 000057 .WORD PDALS!PTER15 ;SET PDALS H TO 1 AND PTER15 L LOW
12492
12493 ;SET AND CLEAR THE SIGNAL CDAL6 H IN CONTROL REGISTER 0. SETTING AND
12494 ;CLEARING CDAL6 H WILL CAUSE THE 'AND STABLE' ONE SHOT TO FIRE WHICH
12495 ;WILL CAUSE THE 'OR STABLE' ONE SHOT TO FIRE. THE 'OR STABLE' ONE
12496 ;SHOT BEING FIRED WILL CLOCK THE 'OR ARRAY RAM' DATA INTO THE FUNCTION
12497 ;SELECT FLIP-FLOPS. WITH A DATA PATTERN OF 004 IN THE 'OR ARRAY RAM',
12498 ;FUNCTION SELECT FLIP-FLOP FUSL2 SHOULD BE CLEARED THUS SETTING THE
12499 ;SIGNAL FUSL2 H TO THE HIGH STATE. ALL OTHER FUNCTION SELECT FLIP-FLOPS
12500 ;WILL BE SET TO A ONE THUS SETTING THERE OUTPUTS LOW.
12501
12502 034444 052737 000100 002272 4$: BIS #CDAL6,E0LOAD ;SET THE SIGNAL TRANST H HIGH
12503 034452 004737 010676 JSR PC,LDRDE0 ;LOAD, READ AND CHECK CDAL REGISTER
12504 034456 001405 BEQ 5$ ;IF LOADED OK THEN CONTINUE
12505 034460 ERRDF 5,CDALRG,E0EROR ;CDAL REGISTER NOT EQUAL EXPECTED

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12506 034460 104455 TRAP C$ERDF
12507 034462 000005 .WORD 5
12508 034464 003006 .WORD CDALRG
12509 034466 006144 .WORD EOEROR
12510 034470 CKLOOP
12511 034470 104406 TRAP C$CLP1
12512 034472 042737 000100 002272 5$: BIC #CDAL6,EOLoad ;SET THE SIGNAL TRANST H LOW
12513 034500 004737 010676 JSR PC,LDRDE0 ;LOAD, READ AND CHECK CDAL REGISTER
12514 034504 001405 BEQ 6$ ;IF LOADED OK THEN CONTINUE
12515 034506 ERRDF 5,CDALRG,EOEROR ;CDAL REGISTER NOT EQUAL EXPECTED
12516 034506 104455 TRAP C$ERDF
12517 034510 000005 .WORD 5
12518 034512 0C3006 .WORD CDALRG
12519 034514 006144 .WORD EOEROR
12520 034516 CKLOOP
12521 034516 104406 TRAP C$CLP1
12522
12523 ;CHECK THAT FUNCTION SELECT FLIP-FLOP FUSL7 IS SET TO A ONE (LOW)
12524 ;BY READING THE OR ARRAY RAM DATA AND FUSL7 IN BIT 12 OF CONTROL
12525 ;REGISTER 4.
12526
12527 034520 042737 010000 002310 6$: BIC #BIT12,E4MASK ;SETUP TO READ FUSL7 H
12528 034526 004737 011012 JSR PC,READE4 ;READ OR ARRAY RAM DATA AND FUSL7 H
12529 034532 001405 BEQ 7$ ;IF OK THEN CONTINUE
12530 034534 ERRDF 7,FUSL7,E4EROR ;FUSL7 PROBABLY NOT SET TO ONE (LOW)
12531 034534 104455 TRAP C$ERDF
12532 034536 000007 .WORD 7
12533 034540 003117 .WORD FUSL7
12534 034542 006174 .WORD E4EROR
12535 034544 CKLOOP
12536 034544 104406 TRAP C$CLP1
12537
12538 ;ASSER THE SIGNAL PTER4 L IN THE POINTER REGISTER BY LOADING THE
12539 ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER. THE
12540 ;SIGNAL PDAL5 H WILL ALSO REMAIN SET.
12541
12542 034546 004537 012162 7$: JSR R5,LDPDAL ;LOAD AND CHECK PDAL REG WITH NEXT WORD
12543 034552 000044 .WORD PDAL5!PTER4 ;SETUP TO READ FUSL F/F'S 3:0
12544
12545 ;READ FUNCTION SELECT FLIP-FLOPS FUSL 3:0 VIA CONTROL REGISTER 6.
12546 ;FUSL2 SHOULD BE SET TO ONE ON A READ COMMAND AND ALL OTHER FUNCTION
12547 ;SELECT FLIP-FLOPS SHOULD BE READ AS A ZERO.
12548
12549 034554 012737 040000 002316 MOV #BIT14,E6LOAD ;SETUP FUSL2 BIT TO BE SET
12550 034562 012737 007777 002320 MOV #007777,E6MASK ;SETUP TO IGNORE TRDI BITS
12551 034570 004737 011052 JSR PC,READE6 ;READ AND CHECK FUSL F/F'S 3:0
12552 034574 001405 BEQ 8$ ;IF OK THEN CONTINUE
12553 034576 ERRDF 8,FUSL30,E6ALLR ;FUSL2 NOT 1 OR OTHER F/F'S SET
12554 034576 104455 TRAP C$ERDF
12555 034600 000010 .WORD 8
12556 034602 003605 .WORD FUSL30
12557 034604 006224 .WORD E6ALLR
12558 034606 CKLOOP
12559 034606 104406 TRAP C$CLP1
12560
12561 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL

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TEST 13: CHECK SA SIGNAL 'EDBRK H' TO TE MODULE

SEQ 0242

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12562                                     ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER
12563
12564 034610 004737 012212      8$: JSR      PC,SLCTTE          ;SELECT TARGET EMULATOR MODULE.
12565
12566                                     ;SET ADAL REGISTER BITS 10, 9 AND 4 TO A ONES AND ALL OTHER ADAL BITS TO
12567                                     ;A ZERO. PULSE THE SIGNAL 'BRKRES L' BY SETTING AND CLEARING ADAL
12568                                     ;REGISTER BIT 0. ADAL10 H AND ADAL9 H SET TO ONES WILL ENABLE THE
12569                                     ;TARGET EMULATOR SIGNALS TO THE SYSTEM BUS. ADAL4 H SET TO A ONE
12570                                     ;WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN A
12571                                     ;PULSE IS ISSUED ON THE SIGNAL XRAS H. A PULSE ON THE SIGNAL BRKRES L
12572                                     ;VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE MEMORY SIMULATOR MODULE.
12573
12574 034614 012737 003000 002334  MOV      #ADAL10!ADAL9,T2LOAD      ;SETUP ADAL REGISTER BITS TO LOAD
12575 034622 004737 012764          JSR      PC,BRKRES              ;SET BITS AND PULSE BRKRES L
12576
12577                                     ;READ CONTROL REGISTER 0 TO CHECK THAT NO BREAKS ARE SET IN GDAL
12578                                     ;BITS 7:4. ALSO LOAD BITS IN CONTROL REGISTER 0'S GDAL REGISTER TO
12579                                     ;SELECT THE HDAL REGISTER. THE HDAL REGISTER WILL BE WRITTEN OR READ
12580                                     ;ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
12581
12582 034626 112737 000003 002324  MOVVB   #HDAL,T0LOAD            ;SETUP BITS TO BE LOADED
12583 034634 004737 011076          JSR      PC,LDRDT0            ;LOAD, READ AND CHECK GDAL REGISTER
12584 034640 001405          BEQ      9$                  ;IF LOADED OK THEN CONTINUE
12585 034642          ERRDF   9,GDALRG,T0EROR      ;GDAL REGISTER NOT EQUAL TO EXPECTED
12586 034642 104455          TRAP   C$ERDF
12587 034644 000011          .WORD  9
12588 034646 003636          .WORD  GDALRG
12589 034650 006664          .WORD  T0EROR
12590 034652          CKLOOP
12591 034652 104406          TRAP   C$CLP1
12592
12593                                     ;SET HDAL REGISTER BIT 2 TO A ONE AND ALL OTHER HDAL BITS TO A ZERO.
12594                                     ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11 TIMING
12595                                     ;AND CONTROL SIGNALS.
12596
12597 034654 012737 000004 002346  9$:  MOV      #HDAL2,T6LOAD            ;SETUP BIT TO BE LOADED
12598 034662 004737 011214          JSR      PC,LDRDT6            ;LOAD, READ AND CHECK HDAL REGISTER
12599 034666 001405          BEQ      10$                 ;IF LOADED OK THEN CONTINUE
12600 034670          ERRDF   12,HDALRG,T06ERR      ;HDAL REGISTER NOT EQUAL TO EXPECTED
12601 034670 104455          TRAP   C$ERDF
12602 034672 000014          .WORD  12
12603 034674 003754          .WORD  HDALRG
12604 034676 006730          .WORD  T06ERR
12605 034700          CKLOOP
12606 034700 104406          TRAP   C$CLP1
12607
12608                                     ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL2 H IN CONTROL
12609                                     ;REGISTER 4. PULSING THE SIGNAL INVD L WILL INITIALIZE ALL THE
12610                                     ;FLIP-FLOP'S ON THE MODULE NOT CLEARED BY BRKRES L. SET THE SIGNAL
12611                                     ;FETCT H TO THE HIGH STATE BY SETTING VDAL REGISTER BIT 7 TO A ONE.
12612
12613 034702 012737 000200 002340  10$: MOV      #VDAL7,T4LOAD            ;SET BIT TO SET FETCT H HIGH
12614 034710 004737 012704          JSR      PC,CLRPSM           ;PULSE INVD L BY TOGGLING VDAL4 H
12615
12616                                     ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
12617                                     ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.

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```
12618
12619 034714 004737 012142 JSR PC,SLCTED ;SELECT THE STATE ANALYZER MODULE
12620
12621 ;SET THE SIGNAL CDAL1 H TO A ONE TO ENABLE FUNCTION SELECT FLIP-FLOP
12622 ;FUSL2 TO THE SYSTEM BUS AS THE SIGNAL EDBRK H. THE FLIP-FLOP SHOULD
12623 ;BE CLEARED THUS SETTING THE SIGNAL FUSL2 H TO THE HIGH STATE WHICH
12624 ;WILL CAUSE THE SIGNAL EDBRK H TO BE SET TO THE HIGH STATE.
12625
12626 034720 052737 000002 002272 BIS #CDAL1,ELOAD ;SETUP BIT TO BE LOADED
12627 034726 004737 010676 JSR PC,LDRDEO ;LOAD, READ AND CHECK CDAL REGISTER
12628 034732 001405 BEQ 11$ ;IF LOADED OK THEN CONTINUE
12629 034734 ERRDF 5,CDALRG,E0EROR ;CDAL REGISTER NOT EQUAL EXPECTED
12630 034734 104455 TRAP C$ERDF
12631 034736 000005 .WORD 5
12632 034740 003006 .WORD CDALRG
12633 034742 006144 .WORD E0EROR
12634 034744 CKLOOP
12635 034744 104406 TRAP C$CLP1
12636
12637 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
12638 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
12639
12640 034746 004737 012212 11$: JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE
12641
12642 ;READ CONTROL REGISTER 0 TO CHECK THAT STATE ANALYZER'S SIGNAL EDBRK H
12643 ;IS READ AS A ONE IN THE GDAL REGISTER. THE SIGNAL EDBRK H SHOULD BE
12644 ;ASSERTED HIGH AS A RESULT OF STATE ANALYZER'S FUNCTION SELECT FLIP-
12645 ;FLOP FUSL2 BEING CLEARED AND CDAL1 H BEING ASSERTED HIGH.
12646
12647 034752 052737 000020 002326 BIS #EDBRK,TOGOOD ;EXPECT EDBRK H TO BE A ONE
12648 034760 004737 011112 JSR PC,READTO ;READ AND CHECK GDAL REGISTER
12649 034764 001405 BEQ 12$ ;IF OK THEN CONTINUE
12650 034766 ERRDF 9,GDALRG,TOEROR ;EDBRK H PROBABLY NOT SET HIGH
12651 034766 104455 TRAP C$ERDF
12652 034770 000011 .WORD 9
12653 034772 003636 .WORD GDALRG
12654 034774 006664 .WORD TOEROR
12655 034776 CKLOOP
12656 034776 104406 TRAP C$CLP1
12657
12658 ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. WHEN XRAS H
12659 ;IS SET HIGH, THE PAUSE MODE FLIP-FLOP WILL BE SET TO RUN MODE THUS
12660 ;SETTING THE SIGNAL PAUSE L TO THE LOW STATE, THE EDFET FLIP-FLOP WILL
12661 ;BE SET TO A ONE THUS SETTING THE SIGNAL EDFET H TO THE HIGH STATE,
12662 ;AND THE BTFET FLIP-FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL
12663 ;BTFET L TO THE LOW STATE. AS A RESULT OF EDBRK H BEING ASSERTED HIGH,
12664 ;THE SIGNALS BRK H AND SOP H WILL BE ASSERTED HIGH. AS A RESULT OF
12665 ;SOP H AND EDFET H BEING ASSERTED HIGH, THE PAUSE STATE WORKING FLIP-
12666 ;FLOP WILL BE DIRECT SET TO A ONE THUS CAUSING THE SIGNAL PSMW H TO
12667 ;BE ASSERTED HIGH.
12668
12669 035000 004737 012264 12$: JSR PC,XRAS ;GO PULSE XRAS H VIA HDAL12 H
12670
12671 ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING FLIP-
12672 ;FLOP IS SET TO A ONE AS A RESULT OF EDBRK H AND EDFET H BEING
12673 ;ASSERTED HIGH. THE SIGNAL BTS1 H WILL ALSO BE SET TO A ONE AS A
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12674 ;RESULT OF THE BTJET FLIP-FLOP BEING SET TO A ONE AND THE SIGNAL INTER L
12675 ;BEING ASSERTED HIGH.
12676
12677 035004 052737 001040 002342 BIS #VDAL9!VDAL5,T4GOOD ;EXPECT PSMW H AND BTS1 H TO BE SET
12678 035012 004737 011176 JSR PC,READT4 ;READ AND CHECK VDAL REGISTER
12679 035016 001405 BEQ 13$ ;IF OK THEN CONTINUE
12680 035020 ERRDF 11,VDALRG,T4EROR ;EDBRK H PROBABLY DIDN'T SET BRK H HIGH
12681 035020 104455 TRAP C$ERDF
12682 035022 000013 .WORD 11
12683 035024 003706 .WORD VDALRG
12684 035026 006714 .WORD T4EROR
12685 035030 CKLOOP
12686 035030 104406 TRAP C$CLP1
12687
12688 ;SET THE SIGNAL FETCT H TO THE LOW STATE BY CLEARING VDAL7 H AND PULSE
12689 ;THE SIGNAL INVD L BY SETTING AND CLEARING THE SIGNAL VDAL2 H. A PULSE
12690 ;ON INVD L WILL CLEAR THE EDFET, PSMW AND BTJET FLIP-FLOPS.
12691
12692 035032 005037 002340 13$: CLR T4LOAD ;SETUP TO CLEAR ALL R/W BITS
12693 035036 004737 012704 JSR PC,CLRPSM ;GO PULSE INVD L VIA VDAL2 H
12694
12695 ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
12696 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
12697
12698 035042 004737 012142 JSR PC,SLCTED ;SELECT THE STATE ANALYZER MODULE
12699
12700 ;SET THE SIGNAL PDAL5 H TO THE LOW STATE BY CLEARING THE BIT IN
12701 ;CONTROL REGISTER 2'S PDAL REGISTER. PDAL5 H ON A ZERO WILL PRESET
12702 ;ALL THE FUNCTION SELECT FLIP-FLOPS TO A ONE THUS SETTING ALL THE
12703 ;ZERO OUTPUTS OF THE FUNCTION SELECT FLIP-FLOP'S TO THE LOW STATE.
12704 ;WHEN FUSL2 FLIP-FLOP IS PRESET TO A ONE, THE SIGNALS FUSL2 H AND
12705 ;EDBRK H WILL BE SET TO THE LOW STATE.
12706
12707 035046 004537 012162 JSR R5,LDPDAL ;LOAD AND CHECK PDAL REG WITH NEXT WORD
12708 035052 000004 .WORD PTER4 ;SETUP TO READ FUSL F/F'S 3:0
12709
12710 ;READ FUNCTION SELECT FLIP-FLOP'S FUSL 3:0 VIA CONTROL REGISTER 6
12711 ;TO CHECK THAT THESE FLIP-FLOPS ARE PRESET TO A ONE. WHEN THE FLIP-
12712 ;FLOPS ARE PRESET TO A ONE, THEY WILL BE READ AS ZEROES WHEN CONTROL
12713 ;REGISTER 6 IS READ.
12714
12715 035054 042737 040000 002316 BIC #BIT14,E6LOAD ;EXPECT FUSL2 TO BE A 0 WHEN READ
12716 035062 004737 011052 JSR PC,READE6 ;READ AND CHECK FUSL F/F'S 3:0
12717 035066 001405 BEQ 14$ ;IF OK THEN CONTINUE
12718 035070 ERRDF 8,FUSL30,E6ALLR ;PDAL5 PROBABLY FAILED TO PRESET F/F'S
12719 035070 104455 TRAP C$ERDF
12720 035072 000010 .WORD 8
12721 035074 003605 .WORD FUSL30
12722 035076 006224 .WORD E6ALLR
12723 035100 CKLOOP
12724 035100 104406 TRAP C$CLP1
12725
12726 ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
12727 ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER
12728
12729 035102 004737 012212 14$: JSR PC,SLCTTE ;SELECT THE TARGET EMULATOR MODULE

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12730
12731 ;READ CONTROL REGISTER 0'S GDAL REGISTER TO CHECK THAT THE SIGNAL
12732 ;EDBRK H IS READ AS A ZERO AFTER THE PROGRAM HAD PRESET THE STATE
12733 ;ANALYZERS FUNCTION SELECT FLIP-FLOP'S TO A ONE VIA PDAL5 H (0).
12734
12735 035106 042737 000020 002326 BIC #EDBRK,TOGOOD ;EXPECT EDBRK H TO BE A ZERO
12736 035114 004737 011112 JSR PC,READTO ;READ AND CHECK GDAL REGISTER
12737 035120 001404 BEQ 15$ ;IF OK THEN CONTINUE
12738 035122 ERRDF 9,GDALRG,TOEROR ;EDBRK H PROBABLY STILL SET HIGH
12739 035122 104455 TRAP C$ERDF
12740 035124 000011 .WORD 9
12741 035126 003636 .WORD GDALRG
12742 035130 006664 .WORD TOEROR
12743 035132 15$: ENDSEG
12744 035132 10000$:
12745 035132 104405 TRAP C$ESEG
12746
12747 035134 L10051: ENDTST
12748 035134
12749 035134 104401 TRAP C$ETST
12750 035136 ENDMOD
12751

```


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TEST 13: CHECK SA SIGNAL 'EDBRK H' TO TE MODULE

B 4

SEQ 0246

12752
12753
12754
12755 035136
12756
12757
12758
12759
12760
12761
12762
12763
12764
12765
12766 035136
12767 035136 000027
12768 035140
12769
12770
12771
12772
12773
12774
12775
12776
12777
12778
12779 035140
12780 035140 000031
12781 035142 035216
12782 035144 000000
12783 035146 177777
12784 035150
12785 035150 001031
12786 035152 035232
12787 035154 000000
12788 035156 000774
12789 035160
12790 035160 002032
12791 035162 035251
12792 035164 177777
12793 035166 000000
12794 035170 000017
12795 035172
12796 035172 003032
12797 035174 035314
12798 035176 177777
12799 035200 000000
12800 035202 000017
12801 035204
12802 035204 004032
12803 035206 035355
12804 035210 177777
12805 035212 000000
12806 035214 000017
12807 035216

.TITLE PARAMETER CODING
.SBTTL HARDWARE PARAMETER CODING SECTION

BGNMOD

..++
: THE HARDWARE PARAMETER CODING SECTION CONTAINS MACROS
: THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES. THE
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: INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES. THE
: MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
: WITH THE OPERATOR.
:--

BGNHRD

.WORD L10052-L\$HARD/2

L\$HARD::

: HARDWARE P-TABLE QUESTIONS

: ASK FOR CDS-11 CSR ADDRESS
: ASK FOR CDS-11 VECTOR ADDRESS
: ASK FOR CDS-11 MEORY SIMULATOR DEVICE NUMBER
: ASK FOR CDS-11 STATE ANALYZER DEVICE NUMBER
: ASK FOR CDS-11 TARGET EMULATOR DEVICE NUMBER

GPRMA MSG1,0,0,0,177777,YES
.WORD T\$CODE
.WORD MSG1
.WORD T\$LLOLIM
.WORD T\$HILIM
GPRMA MSG2,2,0,0,000774,YES
.WORD T\$CODE
.WORD MSG2
.WORD T\$LLOLIM
.WORD T\$HILIM
GPRMD MSG3,4,0,177777,0,000017,YES
.WORD T\$CODE
.WORD MSG3
.WORD 177777
.WORD T\$LLOLIM
.WORD T\$HILIM
GPRMD MSG4,6,0,177777,0,000017,YES
.WORD T\$CODE
.WORD MSG4
.WORD 177777
.WORD T\$LLOLIM
.WORD T\$HILIM
GPRMD MSG5,10,0,177777,0,000017,YES
.WORD T\$CODE
.WORD MSG5
.WORD 177777
.WORD T\$LLOLIM
.WORD T\$HILIM
ENDHRD

PARAMETER CODING
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HARDWARE PARAMETER CODING SECTION

SEQ 0247

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12808
12809 035216
12810
12811
12812
12813
12814
12815 035216 051503 020122 042101 MSG1: .ASCIZ /CSR ADDRESS/
12816 035224 051104 051505 000123
12817 035232 042526 052103 051117 MSG2: .ASCIZ /VECTOR ADDRESS/
12818 035240 040440 042104 042522
12819 035246 051523 000
12820 035251 104 053105 041511 MSG3: .ASCIZ /DEVICE NUMBER FOR MEMORY SIMULATOR/
12821 035256 020105 052516 041115
12822 035264 051105 043040 051117
12823 035272 046440 046505 051117
12824 035300 020131 044523 052515
12825 035306 040514 047524 000122
12826 035314 042504 044526 042503 MSG4: .ASCIZ /DEVICE NUMBER FOR STATE ANALYZER/
12827 035322 047040 046525 042502
12828 035330 020122 047506 020122
12829 035336 052123 052101 020105
12830 035344 047101 046101 055131
12831 035352 051105 000
12832 035355 104 053105 041511 MSG5: .ASCIZ /DEVICE NUMBER FOR TARGET EMULATOR/
12833 035362 020105 052516 041115
12834 035370 051105 043040 051117
12835 035376 052040 051101 042507
12836 035404 020124 046505 046125
12837 035412 052101 051117 000
12838
12839
12840
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SOFTWARE PARAMETER CODING SECTION

SEQ 0248

12841
12842
12843
12844
12845
12846
12847
12848
12849
12850
12851
12852 035420
12853 035420 000000
12854 035422
12855
12856
12857
12858
12859 035422
12860
12861 035422
12862
12863 035422
12864 035422 000010
12865
12866 035442
12867
12868 035442 035464
12869 035444 000007
12870 035446
12871 035446
12872
12873 035446
12874 035446
12875 035446 000000
12876 035450 000005
12877 035452
12878 035452 163010
12879 035454 000370
12880 035456 000000
12881 035460 000001
12882 035462 000002
12883 035464
12884 035464
12885 035464
12886 000001

```
.SBTTL SOFTWARE PARAMETER CODING SECTION
:++
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: WITH THE OPERATOR.
:--

      BGNSFT
      .WORD L10053-L$SOFT/2
L$SOFT::

      .EVEN
      ENDSFT
      .EVEN
L10053:

$PATCH::
      .BLKW 10

      LASTAD
      .EVEN
      .WORD T$FREE
      .WORD T$SIZE
L$LAST::
      ENDMOD

      BGNSETUP          1.
      BGNPTAB
      .WORD 0
      .WORD L10056-./2-1
L10054:
      .WORD 163010
      .WORD 370
      .WORD 0
      .WORD 1
      .WORD 2
      ENDPTAB
L10056:
      ENDSETUP

.END
```


E 4

PARAMETER CODING MACY11 30(1046) 16-SEP-81 15:55 PAGE 250
 CVCDDA.P11 10-SEP-81 12:14 CROSS REFERENCE TABLE -- USER SYMBOLS SEQ 0249

ADALRG	003662	G	2387#	3452	3462	4272	4282	9190	9711	9899					
ADALO =	000001	G	1958#	3446	4266	4276									
ADAL1 =	000002	G	1957#												
ADAL10=	002000	G	1946#	4713	5131	5885	6449	7420	8593	9456	10120	10745	11271	11917	12574
ADAL11=	004000	G	1945#												
ADAL12=	010000	G	1944#												
ADAL13=	020000	G	1943#	9456											
ADAL14=	040000	G	1941#	4713	5131	5885	6449	7420	8593	9705	10120	10745	11271	11917	
ADAL15=	100000	G	1940#	9705	9893										
ADAL2 =	000004	G	1956#												
ADAL3 =	000010	G	1955#												
ADAL4 =	000020	G	1953#	4713	5131	5885	6449	7420	8593	9456	10120	10745			
ADAL5 =	000040	G	1951#												
ADAL6 =	000100	G	1950#												
ADAL7 =	000200	G	1949#	8593	9184										
ADAL8 =	000400	G	1948#												
ADAL9 =	001000	G	1947#	4713	5131	5885	6449	7420	8593	9456	10120	10745	11271	11917	12574
ADDRES=	000000	G	1915#	4802	5367	6124	6649	7621	8259	8682	10211	10834	11400	12048	
ADDRRG	004142	G	2426#	4813	5384	6136	6660	7632	8271	8692	10224	10847	11413	12061	
ADDR0 =	000001	G	2066#												
ADDR1 =	000002	G	2065#												
ADDR10=	002000	G	2056#												
ADDR11=	004000	G	2055#												
ADDR12=	010000	G	2054#												
ADDR13=	020000	G	2053#												
ADDR14=	040000	G	2052#												
ADDR15=	100000	G	2051#	10218	10841										
ADDR2 =	000004	G	2064#												
ADDR3 =	000010	G	2063#												
ADDR4 =	000020	G	2062#												
ADDR5 =	000040	G	2061#												
ADDR6 =	000100	G	2060#												
ADDR7 =	000200	G	2059#												
ADDR8 =	000400	G	2058#												
ADDR9 =	001000	G	2057#												
ADR =	000020	G	1684#												
ALPRNT	007030	G	2960	2990#											
ASSEMB=	000010	G	1445												
BIT0 =	000001	G	1657#	1731	1754	1775	1784	1828	1852	1909	1958	1979	2005	2027	2044
			2066	3817	5057	5058	5059	5060	9140	9666					
BIT00 =	000001	G	1646#	1657											
BIT01 =	000002	G	1645#	1656											
BIT02 =	000004	G	1644#	1655											
BIT03 =	000010	G	1643#	1654											
BIT04 =	000020	G	1642#	1653											
BIT05 =	000040	G	1641#	1652											
BIT06 =	000100	G	1640#	1651											
BIT07 =	000200	G	1639#	1650											
BIT08 =	000400	G	1638#	1649											
BIT09 =	001000	G	1637#	1648											
BIT1 =	000002	G	1656#	1729	1753	1774	1783	1826	1851	1908	1957	1978	2004	2026	2043
			2065	8803	8915	9140									
BIT10 =	002000	G	1636#	1718	1765	1807	1898	1946	1969	1990	2017	2056			
BIT11 =	004000	G	1635#	1717	1764	1806	1897	1945	1968	1989	2015	2055			
BIT12 =	010000	G	1634#	1763	1804	1895	1944	1967	1988	2014	2054	12527			
BIT13 =	020000	G	1633#	1762	1803	1894	1943	1966	1987	2013	2053				

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CROSS REFERENCE TABLE -- USER SYMBOLS

F 4

SEQ 0250

BIT14 = 040000 G	1632#	1761	1802	1893	1941	1965	1986	2012	2052	12549	12715		
BIT15 = 100000 G	1631#	1708	1760	1796	1887	1940	1964	1985	2011	2051			
BIT2 = 000004 G	1655#	1728	1746	1773	1782	1824	1850	1907	1956	1977	2001	2025	2042
	2064	4108	9268	9389									
BIT3 = 000010 G	1654#	1727	1745	1772	1781	1823	1849	1906	1955	1976	2000	2024	2041
	2063	8803	8915	9389									
BIT4 = 000020 G	1653#	1726	1771	1820	1844	1905	1953	1975	1999	2023	2040	2062	5058
	5059												
BIT5 = 000040 G	1652#	1725	1741	1770	1817	1842	1904	1951	1974	1998	2022	2039	2061
	5057	5059											
BIT6 = 000100 G	1651#	1724	1740	1769	1815	1840	1903	1950	1973	1997	2021	2038	2060
	8803	9031	9268										
BIT7 = 000200 G	1650#	1739	1768	1811	1838	1902	1949	1972	1996	2020	2037	2059	9140
	9268												
BIT8 = 000400 G	1649#	1720	1767	1809	1900	1948	1971	1995	2019	2058			
BIT8H = 000010 G	1727#	6094	7944	8236									
BIT9 = 001000 G	1648#	1719	1766	1808	1899	1947	1970	1991	2018	2057			
BOE = 000400 C	1688#												
BRKRES 012764 G	4264#	4714	5132	5886	6450	7421	8594	9457	10121	10463	10619	10746	11060
	11272	11918	12575										
CDALRG 003006 G	2279#	3269	3288	3302	4960	5536	8782	8899	9638	12434	12508	12518	12632
CDALO = 000001 G	1828#												
CDAL1 = 000002 G	1826#	12626											
CDAL10 = 002000 G	1807#												
CDAL11 = 004000 G	1806#												
CDAL12 = 010000 G	1804#												
CDAL13 = 020000 G	1803#												
CDAL14 = 040000 G	1802#												
CDAL15 = 100000 G	1796#	3281	3296	4414									
CDAL2 = 000004 G	1824#												
CDAL3 = 000010 G	1823#	4954	5530	8776	9632								
CDAL4 = 000020 G	1820#												
CDAL5 = 000040 G	1817#												
CDAL6 = 000100 G	1815#	12502	12512										
CDAL7 = 000200 G	1811#												
CDAL8 = 000400 G	1809#												
CDAL9 = 001000 G	1808#	4414											
CKH = 000100 G	1724#												
CLRPSM 012704 G	4234#	4747	5167	5922	6485	7456	8628	8950	9535	10156	10639	10780	11093
	11736	12384	12614	12693									
CTLFDL 004104 G	2421#	9618	9864										
CTSH = 000002 G	1729#	4893	5337	6094	6625	6969	7596	7944	8236	10094	10719	11239	11885
C\$AU = 000052	1445#	4519											
C\$AUTO = 000061	1445#	4450											
C\$BRK = 000022	1445#												
C\$BSEG = 000004	1445#	3159	3252	3327	3669	3702	3723	3821	3892	3956	4007	4037	4057
	4087	4107	4136	4155	4184	4203	4235	4265	4694	5112	5229	5264	5352
	5868	5985	6021	6109	6432	7403	8577	9441	10052	10682	11119	11152	11252
	11765	11798	11898	12414									
C\$BSUB = 000002	1445#												
C\$CEFG = 000045	1445#												
C\$CLCK = 000062	1445#												
C\$CLEA = 000012	1445#	4475											
C\$CLOS = 000035	1445#												
C\$CLP1 = 000006	1445#	3181	3201	3215	3233	3272	3291	3305	3363	3379	3400	3416	3434
	3455	3465	3481	3497	3680	3741	3754	3776	3839	3853	3909	4245	4275

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SEQ 0251

4740	4768	4792	4816	4867	4881	4902	4921	4942	4963	4991	5160	5188
5212	5278	5303	5387	5408	5456	5475	5494	5518	5539	5568	5597	5658
5689	5727	5765	5915	5944	5968	6034	6059	6139	6160	6200	6219	6238
6262	6299	6478	6506	6530	6543	6572	6597	6617	6634	6663	6708	6727
6746	6770	6804	6835	6858	6869	6901	6921	6934	6950	6964	6978	7009
7039	7055	7079	7122	7141	7160	7184	7199	7212	7228	7288	7308	7449
7477	7501	7514	7543	7568	7588	7605	7635	7680	7699	7718	7742	7776
7807	7830	7841	7873	7893	7906	7922	7937	7953	7984	8014	8030	8054
8097	8116	8135	8159	8177	8190	8206	8230	8245	8274	8298	8341	8359
8379	8402	8420	8434	8450	8513	8533	8621	8649	8673	8695	8709	8752
8765	8785	8812	8839	8869	8882	8902	8924	8941	8972	8993	9040	9069
9103	9116	9149	9178	9193	9231	9244	9277	9305	9352	9365	9478	9505
9527	9583	9598	9621	9641	9675	9697	9714	9738	9771	9801	9829	9844
9867	9884	9902	9924	10103	10149	10177	10201	10227	10240	10292	10307	10328
10351	10364	10391	10405	10431	10457	10476	10494	10529	10547	10575	10600	10614
10633	10728	10773	10800	10824	10850	10863	10913	10928	10949	10972	10985	11012
11026	11050	11073	11087	11169	11182	11204	11306	11328	11339	11360	11390	11416
11429	11466	11485	11500	11518	11548	11595	11622	11633	11662	11678	11715	11815
11828	11850	11953	11975	11986	12008	12038	12064	12077	12114	12133	12148	12166
12195	12242	12269	12280	12310	12326	12363	12437	12467	12484	12511	12521	12536
12559	12591	12606	12635	12656	12686	12724						
1445#	10643											
1445#												
1445#												
1445#												
1445#	4497											
1445#	1507											
1445#	3176	3196	3210	3228	3242	3267	3286	3300	3316	3343	3358	3374
3395	3411	3429	3450	3460	3476	3492	3502	3675	3685	3736	3749	3771
3789	3834	3848	3865	3904	3922	3960	4012	4042	4063	4092	4113	4141
4161	4189	4209	4240	4250	4270	4280	4735	4763	4787	4811	4862	4876
4897	4916	4937	4958	4986	5021	5155	5183	5207	5220	5273	5298	5318
5341	5382	5403	5451	5470	5489	5513	5534	5563	5592	5621	5653	5684
5722	5760	5795	5910	5939	5963	5976	6029	6054	6071	6098	6134	6155
6195	6214	6233	6257	6294	6329	6473	6501	6525	6538	6567	6592	6612
6629	6658	6703	6722	6741	6765	6799	6830	6853	6864	6896	6916	6929
6945	6959	6973	7004	7034	7050	7074	7117	7136	7155	7179	7194	7207
7223	7246	7283	7303	7444	7472	7496	7509	7538	7563	7583	7600	7630
7675	7694	7713	7737	7771	7802	7825	7836	7868	7888	7901	7917	7932
7948	7979	8009	8025	8049	8092	8111	8130	8154	8172	8185	8201	8225
8240	8269	8293	8336	8354	8374	8397	8415	8429	8445	8470	8508	8528
8616	8644	8668	8690	8704	8747	8760	8780	8807	8834	8864	8877	8897
8919	8936	8967	8988	9035	9064	9098	9111	9144	9173	9188	9226	9239
9272	9300	9347	9360	9393	9473	9500	9522	9578	9593	9616	9636	9670
9692	9709	9733	9766	9796	9824	9839	9862	9879	9897	9919	9975	10098
10144	10172	10196	10222	10235	10287	10302	10323	10346	10359	10386	10400	10426
10452	10471	10489	10524	10542	10570	10595	10609	10628	10723	10768	10795	10819
10845	10858	10908	10923	10944	10967	10980	11007	11021	11045	11068	11082	11164
11177	11199	11218	11243	11301	11323	11334	11355	11385	11411	11424	11461	11480
11495	11513	11543	11590	11617	11628	11657	11673	11710	11810	11823	11845	11864
11889	11948	11970	11981	12003	12033	12059	12072	12109	12128	12143	12161	12190
12237	12264	12275	12305	12321	12358	12432	12462	12479	12506	12516	12531	12554
12586	12601	12630	12651	12681	12719	12739						

C\$CVEC= 000036
C\$DCLN= 000044
C\$DODU= 000051
C\$DRPT= 000024
C\$DU = 000053
C\$EDIT= 000003
C\$EFDF= 000055

C\$ERHR= 000056
C\$ERRO= 000060
C\$ERSF= 000054

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SEQ 0252

C\$ERSO= 000057	1445#													
C\$ESCA= 000010	1445#													
C\$ESEG= 000005	1445#	3249	3324	3508	3691	3795	3807	3871	3928	3966	4018	4048	4069	
	4098	4119	4147	4167	4195	4215	4256	4286	5027	5226	5324	5347	5801	
	5982	6077	6104	6335	7252	8476	9399	9981	10647	11096	11224	11249	11740	
	11870	11895	12388	12745										
C\$ESUB= 000003	1445#													
C\$ETST= 000001	1445#	4650	5064	5825	6360	7325	8547	9403	9995	10651	11099	11744	12392	
	12749													
C\$EXIT= 000032	1445#	4425	4467											
C\$GETB= 000026	1445#													
C\$GETW= 000027	1445#													
C\$GMAN= 000043	1445#													
C\$GPHR= 000042	1445#	4391												
C\$GPLO= 000030	1445#													
C\$GPRI= 000040	1445#													
C\$INIT= 000011	1445#	4433												
C\$INLP= 000020	1445#													
C\$MANI= 000050	1445#													
C\$MEM = 000031	1445#													
C\$MESSG = 000023	1445#	2560	2569	2578	2587	2597	2607	2616	2625	2634	2762	2771	2780	
	2789	2798	2927	2936	2945	2954	2963							
C\$OPEN= 000034	1445#													
C\$PNTB= 000014	1445#	2971												
C\$PNTF= 000017	1445#													
C\$PNTS= 000016	1445#													
C\$PNTX= 000015	1445#	2652	2663	2672	2682	2693	2702	2712	2720	2730	2741	2750	2821	
	2832	2841	2851	2859	2869	2880	2889	2899	2907	3002	3013	3022	3032	
	3040	3050	3061	3070	3081	3089								
C\$QIO = 000377	1445#													
C\$RDBU= 000007	1445#													
C\$REFG= 000047	1445#	4355	4360	4365	4379	4385								
C\$RESE= 000033	1445#	4369	4464											
C\$REVI= 000003	1445#	1506												
C\$RFLA= 000021	1445#													
C\$RPT = 000025	1445#	4326												
C\$SEFG= 000046	1445#													
C\$SPRI= 000041	1445#	4421	4462	10056	10583									
C\$SVEC= 000037	1445#	4375	10558											
C\$TPRI= 000013	1445#													
DFPTBL 002160 G	1584#													
DIAGMC= 000000	1445													
EDBRK = 000020 G	1934#	12647	12735											
EDDEV 002222 G	2097#	3260	3263	3280										
EDTYPE 002224 G	2098#	3282												
EF.CON= 000036 G	1664#	4384												
EF.NEW= 000035 G	1665#	4378												
EF.PWR= 000034 G	1666#	4364												
EF.RES= 000037 G	1663#	4359												
EF.STA= 000040 G	1662#	4354												
EIDAL = 000006 G	1924#	5664	6810	7061	7782	8036	8280	11577	11695	12224	12343			
EMSGRO 004766 G	2508#	2556	2612	2758	2923									
EMSGR2 005016 G	2512#	2565	2592	2621	2767	2932								
EMSGR4 005046 G	2516#	2574	2602	2776	2941									
EMSGR6 005076 G	2520#	2583	2630	2785	2794	2950	2959							
EOAIFD 004045 G	2415#	4789	5209	5965	6527	7006	7498	7981	8670	9502	9694	9881	10198	

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SEQ 0253

EODAL = 000007 G	10821	11387	12035											
ERRBLK 002202 G	1925#	5635	6273	6781	7753	11531	12178							
ERRMSG 002200 G	2081#													
ERRNBR 002176 G	2080#													
ERRTYP 002174 G	2079#													
ESRH = 000040 G	2078#													
	1741#	3781	3782	5293	5509	6049	6253	6587	6761	7175	7558	7733	8150	
	8393	10342	10963	11209	11214	11855	11860							
EVL = 000004 G	1682#													
E\$END = 002100	1445#													
E\$LOAD = 000035	1445#	1530												
EOEROR 006144 G	2756#	3270	3289	3303	4961	5537	8783	8900	9639	12435	12509	12519	12633	
EOGOOD 002274 G	2134#	2823	2827	3282*	3567*	3570								
EOLOAD 002272 G	2133#	2823	2828	2837	3260*	3261*	3280*	3281*	3296*	3567	3568	3947	4954*	
	5530*	8776*	9632*	12428*	12502*	12512*	12626*							
EOREAD 002276 G	2135#	2826	2836	3569*	3570									
E026ER 006210 G	2783#	4989	5024	5566	5595	5624	5763	5798	8810	8922	9038	9147	9275	
	9396	9673	9799	9978	12465									
E2EROR 006160 G	2765#	3319	3963											
E2LOAD 002300 G	2137#	2855	3312*	3576	3579	3954*								
E2READ 002302 G	2138#	2854	3577*	3578*	3579									
E4BAD 002314 G	2144#	2874	2884	3592*	3593*	3594								
E4EROR 006174 G	2774#	12482	12534											
E4GOOD 002306 G	2141#	2871	2875	3585*	3586*	3589*	3594							
E4LOAD 002304 G	2140#	2871	2876	2885	3585	3589	3590	12474*						
E4MASK 002310 G	2142#	3320*	3593	12475*	12527*									
E4READ 002312 G	2143#	3591*	3592											
E6ALLR 006224 G	2792#	12557	12722											
E6LOAD 002316 G	2146#	2903	3600	3603	4982*	5016*	5558*	5587*	5617*	5755*	5790*	8803*	8915*	
	9031*	9140*	9268*	9389*	9665*	9666*	9792*	9971*	12457*	12549*	12715*	.		
E6MASK 002320 G	2147#	3321*	3602	4696*	5017*	5114*	5559*	5588*	5616*	5756*	5791*	8578*	8802*	
	12458*	12550*												
E6READ 002322 G	2148#	2902	3601*	3602*	3603									
FDAL = 000002 G	1919#	4777	5197	5953	6515	6990	7486	7965	8658	9486	9589	9835	10186	
	10809	11369	12017											
FDALRG 004022 G	2411#													
FDALO = 000001 G	2044#	4783	5203	5959	6521	7000	7492	7975	8664	9496	9688	10192	10815	
FDAL1 = 000002 G	2043#	7000	7975											
FDAL2 = 000004 G	2042#													
FDAL3 = 000010 G	2041#													
FDAL4 = 000020 G	2040#													
FDAL5 = 000040 G	2039#													
FDAL6 = 000100 G	2038#													
FDAL7 = 000200 G	2037#													
FDEIDL 004645 G	2485#	11592	12239											
FDEODL 004605 G	2479#	11545	12192											
FDTDEI 004705 G	2491#	11712	12360											
FJADR = 000001 G	1917#													
FJADRG 004173 G	2431#													
FSLGB 005232 G	2542#	2660	2690	2738	2829	2877	3010	3058						
FSLR 005176 G	2537#	2669	2699	2717	2747	2838	2856	2886	2904	3019	3037	3067	3086	
FUSL30 003605 G	2364#	12556	12721											
FUSL7 003117 G	2303#	12533												
F\$AU = 000015	1445#	4507	4518											
F\$AUTO = 000020	1445#	4445	4449											
F\$BGN = 000040	1445#	1452	1615	1620	2554	2563	2572	2581	2590	2600	2610	2619	2628	

LDRDAR	010762	G	3585#																		
LDRDE0	010676	G	3264	3297	3567#	4955	5531	8777	9633	12429	12503	12513	12627								
LDRDE2	010730	G	3313	3576#	3957																
LDRDE4	010776	G	3589#	12476																	
LDRDE6	011044	G	3600#	5618	12459																
LDRDS0	010504	G	3173	3207	3522#	3672	3682	4894	5338	6095	6626	6913	6970	7191	7597						
			7885	7945	8169	8237	8412	10095	10720	11240	11886										
LDRDS2	010544	G	3225	3532#	3733	3831	3901	11161	11807												
LDRDS4	010604	G	3239	3542#	3746	3845	5270	6026	6564	7280	7535	8505	11174	11820							
LDRDS6	010630	G	3550#	3768	3862	5315	6068	6609	6956	7580	7929	11196	11842								
LDRDT0	011076	G	3340	3371	3408	3473	3615#	4009	9590	9836	12583										
LDRDT2	011136	G	3447	3457	3625#	4267	4277	9185	9706	9894											
LDRDT4	011162	G	3489	3499	3633#	4237	4247	7047	8022	8701											
LDRDT6	011214	G	3392	3426	3642#	4039	4060	4089	4110	4138	4158	4186	4206	4732	4760						
			4784	4808	5152	5180	5204	5379	5400	5907	5936	5960	6131	6152	6470						
			6498	6522	6655	7001	7031	7441	7469	7493	7627	7976	8006	8266	8613						
			8641	8665	8687	8831	8964	9061	9170	9297	9470	9497	9519	9689	9730						
			9876	9916	10141	10169	10193	10219	10765	10792	10816	10842	11298	11352	11408						
			11654	11945	12000	12056	12302	12598													
LDRDOE	010704	G	3283	3568#																	
LDRDOS	010512	G	3193	3523#																	
LDRDOT	011104	G	3355	3616#	10567																
LDRD2S	010552	G	3533#	5295	6051	6589	7560														
LDRD4E	011004	G	3587	3590#																	
LDRD4T	011170	G	3634#	6850	6861	7822	7833	10486	11320	11331	11614	11625	11670	11967	11978						
			12261	12272	12318																
LDRD6S	010636	G	3551#	3919																	
LOE =	040000	G	1694#																		
LOT =	000010	G	1683#																		
L\$ACP	002110	G	1537#																		
L\$APT	002036	G	1495#																		
L\$AU	013370	G	4507#																		
L\$AUT	002070	G	1521#																		
L\$AUTO	013342	G	1538	4445#																	
L\$CCP	002106	G	1535#																		
L\$CLEA	013344	G	1536	4459#																	
L\$CO	002032	G	1491#																		
L\$DEPO	002011	G	1473#																		
L\$DESC	002364	G	1528	2190#																	
L\$DESP	002076	G	1527#																		
L\$DEVP	002060	G	1513#																		
L\$DISP	002124	G	1498	1557#																	
L\$DLY	002116	G	1543#																		
L\$DTP	002040	G	1497#																		
L\$DTYP	002034	G	1493#																		
L\$DU	013362	G	4485#																		
L\$DUT	002072	G	1523#																		
L\$DVTY	002354	G	1514	2181#																	
L\$EF	002052	G	1508#																		
L\$ENVI	002044	G	1501#																		
L\$ERRT	002174	G	2077#																		
L\$ETP	002102	G	1531#																		
L\$EXP1	002046	G	1503#																		
L\$EXP4	002064	G	1517#																		
L\$EXP5	002066	G	1519#																		
L\$HARD	035140	G	1480	12767	12768#																

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SEQ 0258

L\$HIME	002120	G	1545#		
L\$HPCP	002016	G	1479#		
L\$HPTP	002022	G	1483#		
L\$HW	002160	G	1484	1582	1583#
L\$ICP	002104	G	1533#		
L\$INIT	013110	G	1534	4352#	
L\$LADP	002026	G	1487#		
L\$LAST	035446	G	1488	12870#	12886
L\$LOAD	002100	G	1529#		
L\$LUN	002074	G	1525#		
L\$MREV	002050	G	1505#		
L\$NAME	002000	G	1462#		
L\$PRIO	002042	G	1499#		
L\$PROT	013102	G	1540	4336#	
L\$PRT	002112	G	1539#		
L\$REPP	002062	G	1515#		
L\$REV	002010	G	1471#		
L\$RPT	013074	G	4314#		
L\$SOFT	035422	G	12853	12854#	
L\$SPC	002056	G	1511#		
L\$SPCP	002020	G	1481#		
L\$SPTP	002024	G	1485#		
L\$STA	002030	G	1489#		
L\$SW	002174	G	1606	1607#	
L\$TEST	002114	G	1541#		
L\$TIML	002014	G	1477#		
L\$UNIT	002012	G	1475#		
L10000	002172		1582	1594#	
L10001	002174		1606	1612#	
L10002	005316		2559#		
L10003	005332		2568#		
L10004	005346		2577#		
L10005	005362		2586#		
L10006	005402		2596#		
L10007	005422		2606#		
L10010	005436		2615#		
L10011	005452		2624#		
L10012	005466		2633#		
L10013	006156		2761#		
L10014	006172		2770#		
L10015	006206		2779#		
L10016	006222		2788#		
L10017	006236		2797#		
L10020	006676		2926#		
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L10030	013340		4426	4432#	
L10031	013342		4449#		
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PARAMETER CODING
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12:16

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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0262

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			4293	4395											
REG0EQ	005126	G	2524#	2649	2818	2999									
REG2	002206	G	2088#	3533*	3534	3576*	3577	3625*	3626						
REG2EQ	005140	G	2526#	2679	2848	3029									
REG4	002210	G	2089#	3542*	3543	3590*	3591	3634*	3635						
REG4EQ	005152	G	2528#	2709	2866	3047									
REG6	002212	G	2090#	3551*	3552	3600*	3601	3642*	3643	9605*	9851*	11381*	12029*		
REG6EQ	005164	G	2530#	2727	2896	3078									
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9583	9584	9593	9594	9595	9596	9597	9598	9599	9616	9617	9618	9619
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9673	9674	9675	9676	9692	9693	9694	9695	9696	9697	9698	9709	9710
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9767	9768	9769	9770	9771	9772	9796	9797	9798	9799	9800	9801	9802
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10454	10455	10456	10457	10458	10471	10472	10473	10474	10475	10476	10477	10489
10490	10491	10492	10493	10494	10495	10524	10525	10526	10527	10528	10529	10530

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I 5

SEQ 0266

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12039	12059	12060	12061	12062	12063	12064	12065	12072	12073	12074	12075	12076	
12077	12078	12109	12110	12111	12112	12113	12114	12115	12128	12129	12130	12131	
12132	12133	12134	12143	12144	12145	12146	12147	12148	12149	12161	12162	12163	
12164	12165	12166	12167	12190	12191	12192	12193	12194	12195	12196	12237	12238	
12239	12240	12241	12242	12243	12264	12265	12266	12267	12268	12269	12270	12275	
12276	12277	12278	12279	12280	12281	12305	12306	12307	12308	12309	12310	12311	
12321	12322	12323	12324	12325	12326	12327	12358	12359	12360	12361	12362	12363	
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12438	12462	12463	12464	12465	12466	12467	12468	12479	12480	12481	12482	12483	
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	2596	2597	2606	2607	2615	2616	2624	2625	2633	2634	2761	2762	2770
	2771	2779	2780	2788	2789	2797	2798	2926	2927	2935	2936	2944	2945
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SEQ 0269

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T\$HILI= 000017
T\$LAST= 000001
T\$LOLI= 000000
T\$LSYM= 010000

1445#														
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1445#	12868#	12874												
12780#	12782	12785#	12787	12790#	12793	12796#	12799	12802#	12805					
1445#	1595	1613	2560	2569	2578	2587	2597	2607	2616	2625	2634	2762		
2771	2780	2789	2798	2927	2936	2945	2954	2963	4297	4326	4433	4450		
4475	4497	4519	4650	5064	5825	6360	7325	8547	9403	9995	10651	11099		
11744	12392	12749	12810	12862										

T\$LTNO= 000015
T\$NEST= 177777

12871#														
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2577#	2581#	2586#	2590#	2596#	2600#	2606#	2610#	2615#	2619#	2624#	2628#	2633#		
2756#	2761#	2765#	2770#	2774#	2779#	2783#	2788#	2792#	2797#	2921#	2926#	2930#		
2935#	2939#	2944#	2948#	2953#	2957#	2962#	3159#	3248#	3252#	3323#	3327#	3507#		
3669#	3690#	3702#	3723#	3794#	3806#	3821#	3870#	3892#	3927#	3956#	3965#	4007#		
4017#	4037#	4047#	4057#	4068#	4087#	4097#	4107#	4118#	4136#	4146#	4155#	4166#		
4184#	4194#	4203#	4214#	4235#	4255#	4265#	4285#	4292#	4296#	4302#	4307#	4314#		
4325#	4336#	4343#	4352#	4432#	4445#	4449#	4459#	4474#	4485#	4496#	4507#	4518#		
4522#	4528#	4643#	4649#	4689#	4694#	5026#	5063#	5109#	5112#	5225#	5229#	5264#		
5323#	5346#	5352#	5800#	5824#	5865#	5868#	5981#	5985#	6021#	6076#	6103#	6109#		
6334#	6359#	6395#	6432#	7251#	7324#	7367#	7403#	8475#	8546#	8575#	8577#	9398#		
9402#	9435#	9441#	9980#	9994#	10049#	10052#	10646#	10650#	10680#	10682#	11095#	11098#		
11115#	11119#	11152#	11223#	11248#	11252#	11739#	11743#	11761#	11765#	11798#	11869#	11894#		
11898#	12387#	12391#	12410#	12414#	12744#	12748#	12751#	12756#	12767#	12808#	12853#	12860#		

T\$NSO = 000000
T\$NS1 = 000005

12872#														
1452#	1615	1620#	4302	4307#	4522	4528#	12751	12756#	12872					
1582#	1594	1606#	1612	2554#	2559	2563#	2568	2572#	2577	2581#	2586	2590#		
2596	2600#	2606	2610#	2615	2619#	2624	2628#	2633	2756#	2761	2765#	2770		
2774#	2779	2783#	2788	2792#	2797	2921#	2926	2930#	2935	2939#	2944	2948#		
2953	2957#	2962	3159#	3248	3252#	3323	3327#	3507	3669#	3690	3702#	3806		
3821#	3870	3892#	3927	3956#	3965	4007#	4017	4037#	4047	4057#	4068	4087#		
4097	4107#	4118	4136#	4146	4155#	4166	4184#	4194	4203#	4214	4235#	4255		
4265#	4285	4292#	4296	4314#	4325	4336#	4343	4352#	4432	4445#	4449	4459#		
4474	4485#	4496	4507#	4518	4643#	4649	4689#	5063	5109#	5824	5865#	6359		
6395#	7324	7367#	8546	8575#	9402	9435#	9994	10049#	10650	10680#	11098	11115#		

T\$NS2 = 000003

11743	11761#	12391	12410#	12748	12767#	12808	12853#	12860						
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6103	6109#	6334	6432#	7251	7403#	8475	8577#	9398	9441#	9980	10052#	10646		
10682#	11095	11119#	11248	11252#	11739	11765#	11894	11898#	12387	12414#	12744			

T\$NS3 = 000003
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T\$PTAB= 010055
T\$PTHV= 000001
T\$PTNU= 000001
T\$SAVL= 177777
T\$SEGL= 177777

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3702#	3723#	3794#	3796	3806#	3808	3821#	3870#	3872	3892#	3927#	3929	3956#		
3965#	3967	4007#	4017#	4019	4037#	4047#	4049	4057#	4068#	4070	4087#	4097#		
4099	4107#	4118#	4120	4136#	4146#	4148	4155#	4166#	4168	4184#	4194#	4196		
4203#	4214#	4216	4235#	4255#	4257	4265#	4285#	4287	4694#	5026#	5028	5112#		
5225#	5227	5229#	5264#	5323#	5325	5346#	5348	5352#	5800#	5802	5868#	5981#		
5983	5985#	6021#	6076#	6078	6103#	6105	6109#	6334#	6336	6432#	7251#	7253		
7403#	8475#	8477	8577#	9398#	9400	9441#	9980#	9982	10052#	10646#	10648	10682#		
11095#	11097	11119#	11152#	11223#	11225	11248#	11250	11252#	11739#	11741	11765#	11798#		
11869#	11871	11894#	11896	11898#	12387#	12389	12414#	12744#	12746					
3159#	3248	3252#	3323	3327#	3507	3669#	3690	3702#	3806	3821#	3870	3892#		
3927	3956#	3965	4007#	4017	4037#	4047	4057#	4068	4087#	4097	4107#	4118		

T\$SEK0= 010000

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SEQ 0270

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T\$SUBN= 000000	6432#	7251	7403#	8475	8577#	9398	9441#	9980	10052#	10646	10682#	11095	11119#
	11248	11252#	11739	11765#	11894	11898#	12387	12414#	12744				
	3723#	3794	5264#	5323	6021#	6076	11152#	11223	11798#	11869			
	12869	12886#											
	1445#	4642#	4688#	5108#	5864#	6394#	7366#	8574#	9434#	10048#	10679#	11114#	11760#
T\$TAGL= 177777	12409#												
T\$TAGN= 010057	1445#	1582#	1606#	2554#	2563#	2572#	2581#	2590#	2600#	2610#	2619#	2628#	2756#
	2765#	2774#	2783#	2792#	2921#	2930#	2939#	2948#	2957#	4292#	4314#	4336#	4352#
	4445#	4459#	4485#	4507#	4643#	4689#	5109#	5865#	6395#	7367#	8575#	9435#	10049#
T\$TEMP= 000000	10680#	11115#	11761#	12410#	12767#	12853#	12874#	12875#	12876#				
	1558#	1559#	1560#	1561#	1562#	1563#	1564#	1565#	1566#	1567#	1568#	1569#	1570#
	1571#	1594#	1612#	1615#	2559#	2568#	2577#	2586#	2596#	2606#	2615#	2624#	2633#
	2761#	2770#	2779#	2788#	2797#	2926#	2935#	2944#	2953#	2962#	3248#	3323#	3507#
	3690#	3794#	3806#	3870#	3927#	3965#	4017#	4047#	4068#	4097#	4118#	4146#	4166#
	4194#	4214#	4255#	4285#	4296#	4302#	4318#	4319	4325#	4343#	4425#	4426	4432#
	4449#	4467#	4468	4474#	4489#	4490	4496#	4511#	4512	4518#	4522#	4649#	5026#
	5063#	5225#	5323#	5346#	5800#	5824#	5981#	6076#	6103#	6334#	6359#	7251#	7324#
	8475#	8546#	9398#	9402#	9980#	9994#	10646#	10650#	11095#	11098#	11223#	11248#	11739#
	11743#	11869#	11894#	12387#	12391#	12744#	12748#	12751#	12780#	12785#	12790#	12796#	12802#
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	2821	2832	2841	2851	2859	2869	2880	2889	2899	2907	2927	2936	2945
	2954	2963	2971	3002	3013	3022	3032	3040	3050	3061	3070	3081	3089
	3159	3176	3181	3196	3201	3210	3215	3228	3233	3242	3249	3252	3267
	3272	3286	3291	3300	3305	3316	3324	3327	3343	3358	3363	3374	3379
	3395	3400	3411	3416	3429	3434	3450	3455	3460	3465	3476	3481	3492
	3497	3502	3508	3669	3675	3680	3685	3691	3702	3723	3736	3741	3749
	3754	3771	3776	3789	3795	3807	3821	3834	3839	3848	3853	3865	3871
	3892	3904	3909	3922	3928	3956	3960	3966	4007	4012	4018	4037	4042
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	4155	4161	4167	4184	4189	4195	4203	4209	4215	4235	4240	4245	4250
	4256	4265	4270	4275	4280	4286	4326	4355	4360	4365	4369	4375	4379
	4385	4391	4421	4425	4433	4450	4462	4464	4467	4475	4497	4519	4650
	4694	4735	4740	4763	4768	4787	4792	4811	4816	4862	4867	4876	4881
	4897	4902	4916	4921	4937	4942	4958	4963	4986	4991	5021	5027	5064
	5112	5155	5160	5163	5188	5207	5212	5220	5226	5229	5264	5273	5278
	5298	5303	5318	5324	5341	5347	5352	5382	5387	5403	5408	5451	5456
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	5653	5658	5684	5689	5722	5727	5760	5765	5795	5801	5825	5868	5910
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	6071	6077	6098	6104	6109	6134	6139	6155	6160	6195	6200	6214	6219
	6233	6238	6257	6262	6294	6299	6329	6335	6360	6432	6473	6478	6501
	6506	6525	6530	6538	6543	6567	6572	6592	6597	6612	6617	6629	6634
	6658	6663	6703	6708	6722	6727	6741	6746	6765	6770	6799	6804	6830
	6835	6853	6858	6864	6869	6896	6901	6916	6921	6929	6934	6945	6950
	6959	6964	6973	6978	7004	7009	7034	7039	7050	7055	7074	7079	7117
	7122	7136	7141	7155	7160	7179	7184	7194	7199	7207	7212	7223	7228
	7246	7252	7283	7288	7303	7308	7325	7403	7444	7449	7472	7477	7496
	7501	7509	7514	7538	7543	7563	7568	7583	7588	7600	7605	7630	7635
	7675	7680	7694	7699	7713	7718	7737	7742	7771	7776	7802	7807	7825

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CROSS REFERENCE TABLE -- USER SYMBOLS

SEQ 0272

TSSSRV= 010025	4292#	4296												
TSSSW = 010001	1606#	1612												
TSSTES= 010051	4643#	4649	4689#	5063	5109#	5824	5865#	6359	6395#	7324	7367#	8546	8575#	
TOEROR 006664 G	9402	9435#	9994	10049#	10650	10680#	11098	11115#	11743	11761#	12391	12410#	12748	
	2921#	3346	3361	3377	3414	3479	4015	4865	8763	8880	8939	9114	9242	
	9363	9596	9842	10290	10389	10455	10474	10527	10573	10598	10612	10631	10911	
TOGOOD 002326 G	11010	11071	12589	12654	12742									
	2155#	3004	3008	3354*	3615*	3619	10382*	10467*	10520*	10566*	10606	10624*	11003*	
	11064*	12647*	12735*											
TOLGAD 002324 G	2154#	3004	3009	3018	3336*	3353*	3369*	3370*	3406*	3407*	3472*	3615	3616	
	3980	4008*	9589*	9835*	10565*	12582*								
TOMASK 002330 G	2156#	3337*	3471*	3618										
TOREAD 002332 G	2157#	3007	3017	3617*	3618*	3619	4293*	10606						
T06ERR 006730 G	2948#	3398	3432	4045	4066	4095	4116	4144	4164	4192	4212	4738	4766	
	4790	4814	5158	5186	5210	5385	5406	5913	5942	5966	6137	6158	6476	
	6504	6528	6661	7007	7037	7447	7475	7499	7633	7982	8012	8272	8619	
	8647	8671	8693	8837	8970	9067	9176	9303	9476	9503	9525	9619	9695	
	9736	9865	9882	9922	10147	10175	10199	10225	10771	10798	10822	10848	11304	
	11358	11388	11414	11660	11951	12006	12036	12062	12308	12604				
T1 013376 G	1558	4642#												
T10 030114 G	1567	10679#												
T11 031070 G	1568	11114#												
T12 032572 G	1569	11760#												
T13 034304 G	1570	12409#												
T2 013404 G	1559	4688#												
T2EROR 006700 G	2930#	3453	3463	4273	4283	9191	9712	9900						
T2LOAD 002334 G	2159#	3036	3446*	3456*	3625	3627	4266*	4276*	4713*	5131*	5885*	6449*	7420*	
	8593*	9184*	9456*	9705*	9893*	10120*	10745*	11271*	11917*	12574*				
T2READ 002336 G	2160#	3035	3626*	3627										
T3 014264 G	1560	5108#												
T4 015666 G	1561	5864#												
T4EROR 006714 G	2939#	3495	3505	4243	4253	4879	5223	5454	5725	5979	6198	6332	6541	
	6706	6856	6867	6899	7053	7120	7512	7678	7828	7839	7871	8028	8095	
	8339	8707	8750	8867	8991	9101	9229	9350	9581	9769	9827	10238	10305	
	10403	10492	10545	10861	10926	11024	11085	11326	11337	11427	11464	11620	11631	
	11676	11973	11984	12075	12112	12267	12278	12324	12684					
T4GOOD 002342 G	2163#	3052	3056	3633*	3636	4872*	5447*	5718*	6191*	6325*	6699*	6849*	6860*	
	6892*	7113*	7671*	7821*	7832*	7864*	8088*	8332*	8743*	8984*	9094*	9222*	9343*	
	9574*	9762*	9820*	10298*	10396*	10484*	10485*	10537*	10538*	10919*	11017*	11078*	11318*	
	11319*	11330*	11457*	11612*	11613*	11624*	11669*	11965*	11966*	11977*	12105*	12259*	12260*	
	12271*	12317*	12677*											
T4LOAD 002340 G	2162#	3052	3057	3066	3488*	3498*	3633	3634	4236*	4246*	4746*	5166*	5921*	
	6484*	6848*	6859*	7046*	7455*	7820*	7831*	8021*	8627*	8700*	8949*	9534*	10155*	
	10483*	10484	10638*	10779*	11092*	11317*	11318	11329*	11611*	11612	11623*	11668*	11735*	
	11964*	11965	11976*	12258*	12259	12270*	12316*	12383*	12613*	12692*				
T4READ 002344 G	2164#	3055	3065	3635*	3636									
T5 016766 G	1562	6394#												
T6 021130 G	1563	7366#												
T6ALLR 006744 G	2957#	5656	5687	6297	6802	6833	7077	7774	7805	8052	8296	11546	11593	
	11713	12193	12240	12361										
T6LOAD 002346 G	2166#	3085	3390*	3425*	3642	3645	4038*	4058*	4059*	4088*	4108*	4109*	4137*	
	4156*	4157*	4185*	4204*	4205*	4730*	4731*	4759*	4783*	4807*	4847*	4848*	5151*	
	5179*	5203*	5378*	5399*	5649*	5680*	5707*	5905*	5935*	5959*	6129*	6151*	6289*	
	6313*	6469*	6497*	6521*	6654*	6671*	6795*	6826*	6883*	7000*	7030*	7070*	7087*	
	7440*	7468*	7492*	7626*	7643*	7767*	7798*	7855*	7975*	8005*	8045*	8062*	8264*	
	8265*	8289*	8306*	8612*	8640*	8664*	8686*	8734*	8830*	8963*	9060*	9169*	9296*	

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SEQ 0273

		9469*	9495*	9496*	9518*	9612*	9687*	9688*	9729*	9858*	9875*	9915*	10140*	10168*
		10192*	10218*	10249*	10764*	10791*	10815*	10841*	10870*	11297*	11351*	11380*	11407*	11438*
		11538*	11557*	11585*	11645*	11653*	11705*	11724*	11944*	11999*	12028*	12055*	12086*	12185*
		12204*	12232*	12292*	12300*	12301*	12353*	12372*	12597*					
T6MASK	002352 G	2168#	3391*	3644	5906*	6130*	6290*	6314*	11259*	11539*	11558*	11586*	11646*	11706*
		11725*	11905*	12186*	12205*	12233*	12293*	12354*	12373*					
T6READ	002350 G	2167#	3084	3643*	3644*	3645								
T7	023750 G	1564	8574#											
T8	025426 G	1565	9434#											
T9	026610 G	1566	10048#											
UAM	= 000200 G	1687#												
UNITNB	002232 G	2103#	4382*	4388*	4390									
VDALRG	003706 G	2394#	3494	3504	4242	4252	4878	5222	5453	5724	5978	6197	6331	6540
		6705	6855	6866	6898	7052	7119	7511	7677	7827	7838	7870	8027	8094
		8338	8706	8749	8866	8990	9100	9228	9349	9580	9768	9826	10237	10304
		10402	10491	10544	10860	10925	11023	11084	11325	11336	11426	11463	11619	11630
		11675	11972	11983	12074	12111	12266	12277	12323	12683				
VDAL0	= 000001 G	1979#	7046	8021	11668	11669	12316	12317						
VDAL1	= 000002 G	1978#												
VDAL10	= 002000 G	1969#												
VDAL11	= 004000 G	1968#												
VDAL12	= 010000 G	1967#												
VDAL13	= 020000 G	1966#												
VDAL14	= 040000 G	1965#												
VDAL15	= 100000 G	1964#												
VDAL2	= 000004 G	1977#	3488	4236	4246	6848	6849	6859	6860	7820	7821	7831	7832	11317
		11329	11330	11611	11623	11624	11964	11976	11977	12258	12270	12271		
VDAL3	= 000010 G	1976#	5447	6191	6699	7671								
VDAL4	= 000020 G	1975#	4872	5718	6325	7113	8088	8332	8743	8984	9094	9222	9343	9574
		9820	10298	10396	10485	10537	10919	11017	11078					
VDAL5	= 000040 G	1974#	8743	9094	10538	11319	11613	11966	12260	12677				
VDAL6	= 000100 G	1973#	5447	6191	6699	7671								
VDAL7	= 000200 G	1972#	8700	10483	11317	11964	12613							
VDAL8	= 000400 G	1971#												
VDAL9	= 001000 G	1970#	10538	11457	12105	12677								
WREH	= 000002 G	1783#	3767	3783	11195	11211	11841	11857						
WRENH	= 000100 G	1740#	3781	3782	3785	5293	5509	6049	6253	6587	6761	7175	7558	7733
		8150	8393	11209	11210	11213	11509	11855	11856	11859	12157			
WRVH	= 000040 G	1725#	3671	10976										
XBCLR	012600 G	4175#												
XBCLRH	012612 G	4175	4183#											
XBCLRL	012644 G	4176	4202#											
XCAS	012370 G	4077#	8979											
XCASH	012402 G	4077	4086#	4850	5441	6185	6692	7104	7665	8079	8323	9329	9565	9757
		10273	10895											
XCASL	012434 G	4078	4106#	4852	5708	6315	6884	7106	7856	8081	8325	9337	9567	9814
		10275	10897											
XPI	012474 G	4127#	9001	9215										
XPIH	012506 G	4127	4135#	4851	5442	6186	6694	7105	7666	8080	8324	9330	9566	9750
		9935	10274	10896	11571	11688	12218	12336						
XPIL	012540 G	4128	4154#	4853	5709	6316	6885	7107	7857	8082	8326	9338	9568	9815
		9950	10276	10898	11647	11731	12294	12379						
XRAS	012264 G	4027#	8735	8857	9086	9204	9316	9945	10376	10442	10514	10997	12669	
XRASH	012276 G	4027	4036#	4849	5440	6184	6692	7103	7664	8078	8322	9564	10272	10894
		11452	12100											
XRASL	012330 G	4028	4056#	4854	5710	6317	6886	7108	7858	8083	8327	9569	10277	10899

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SEQ 0274

	11648	12295																	
X\$ALWA=	000000	1445#																	
X\$FALS=	000040	1445#																	
X\$OFFS=	000400	1445#																	
X\$TRUE=	000020	1445#																	
\$PATCH	035422 G	12863#																	
.	= 035464	1449#	2184#	2194#	2500#	4319	4426	4468	4490	4512	12838#	12864#	12876	12886					

. ABS. 035464 000

ERRORS DETECTED: 0

CVCDDA.BIC,CVCDDA/CRF:SYM/SOL/NL:TOC=SVC/ML,CVCDDA.P11
RUN-TIME: 63 69 4 SECONDS
RUN-TIME RATIO: 1054/137=7.6
CORE USED: 19K (38 PAGES)