

**KD11-Z**

11/44 CPU/EIS  
**CKKAAAO**

AH-F620A-MC

JAN 1980

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FICHE 1 OF 2

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IDENTIFICATION

Product Code: AC-F618A-MC  
Product Name: CKKAAA0 11/44 CPU/EIS  
Date Created: MARCH 1979  
Maintainer: Diagnostic Group  
Author: CHUCK ROBINSON

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\* SUMMARY OF OPERATING INSTRUCTIONS \*  
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The following procedure can be used to run this diagnostic  
in a standard configuration with at least 8K of memory  
and a teletype. If the program does not run successfully  
consult the following document for assistance.

Operating Procedures:

1. Load the program using normal procedures
2. Start the program at Location 200
3. Program should print 'END OF PASS' within  
the 1st second and repeatably thereafter  
at approx. 5 sec. intervals WITH CACHE ON.  
( APPROX. 10 SEC INTERVALS WITH CACHE OFF )
4. If the program does not run as described above,  
consult the full operating instructions which  
follow.

1.0 GENERAL PROGRAM INFORMATION

1.1 PROGRAM PURPOSE

This diagnostic program is designed to be a comprehensive check of the PDP-11/44 Basic Instruction Set. The program exercises all of the processor logic and microcode for all instructions except the Trap and Memory Management Instructions. The program does not test instructions or hardware related to the Trap or Interrupt mechanisms of the 11/44 (E.G. RTT, RTI, WAIT, RESET, TRAP, EMT).

NOTE: HOWEVER, IF THE OPTIONAL CPU/CIS TESTS ARE RUN THEN THE BREAKPOINT TRAP INSTRUCTION AND THE ABILITY TO TRAP UNDER ILLEGAL INSTRUCTION (TRAP TO 10) WILL BE ASSUMED TO BE FUNCTIONAL. (SEE SECT.2.3)

1.2 SYSTEM REQUIREMENTS

1.2.1 HARDWARE

PDP-11/44 Processor  
16K Memory -- The program uses Locations 0 - 36000

1.2.2 SOFTWARE

This program is written to be run as a Stand-Alone program. However, the program is designed to run under Automated Product Test System (APT) in all three modes.

The program can also be run under the ACT 11 Monitor

1.3 RELATED DOCUMENTS AND STANDARDS

PDP-11/44 MICROCODE LISTING

PDP-11/44 ELECTRICAL SCHEMATICS

1.4 DIAGNOSTIC HIERARCHY PREREQUISITES

None

1.5 FAILURE ASSUMPTIONS

None

2.0 OPERATING INSTRUCTIONS

2.1 Loading And Starting Procedures

2.1.1 LOADING

Use normal procedures for Loading Absolute Binary Tapes.

2.1.2 NORMAL START

This is the procedure for normal program running (I.E., starting with Test 1 and executing entire diagnostic).

START AT ADDRESS = 200

2.1.3 SUBTEST START

This is the procedure for starting at a Subtest other than 1.

1. LOAD \$TESTN (in Mailbox Section) with the number of Subtest minus one (in Octal). For example, to start at Subtest 100, \$TESTN=77.
2. Load Starting Address of Subtest in Loc. 216
3. START AT ADDRESS = 204

2.2 SPECIAL ENVIRONMENTS

This program is written to comply with all the requirements of the APT Interface Specification. It will run under APT in either Quick Verify, program or Run-Time modes.

This program is written to comply with all of the requirements of programs to run under the ACT11 Monitor.

THE EXECUTION TIMES PROVIDED IN THE APT SCRIPT THAT FOLLOWS  
ARE FOR EXECUTION WITH A 11/44 PROCESSOR, CACHE,  
16K CORE MEMORY, AND 300 BAUD.

THE FOLLOWING IS A PROGRAM LOAD FILE USED BY APT:

1. E TABLE 'A' IS USED FOR APT DUMP MODE.  
A. IN ADDITION TO NORMAL CPU DIAGNOSTIC TESTS THIS TABLE WILL  
SELECT THE OPTIONAL CACHE AND CIS TESTS.(\$SWREG=400)
2. E TABLE 'B' IS USED FOR APT QV MODE WHILE RUNNING ON A  
MANUFACTURING QV STATION.  
IT ACCOMPLISHES WHAT ETABLE 'A' DOES BUT ADDITIONALLY  
SUPPRESSES TYPEOUTS.(\$ENVVM=240)
3. ETABLE 'C' IS USED FOR APT QV OR RUNTIME MODES WHILE RUNNING  
ON SYSTEMS OTHER THAN MFG. QV STATIONS. THIS TABLE DESELECTS  
THE OPTIONAL CACHE AND CIS TESTS.

1ST PASS RUN TIME	LONGEST TEST TIME	ADDITIONAL RUN TIME
10	10	0

..... E TABLES .....

E-MODE/S-MODE (\$ENVVM/\$ENV)	A 200/000	B 240/001	C 240/001
SWITCH REGISTER 1 (\$SWREG)	000400	000400	000000
SWITCH REGISTER 2 CPU TYPE/OPTIONS	000000 00/0000	000000 00/0000	000000 00/0000

### 2.3 PROGRAM OPTIONS

This program is intended to be a Basic Processor Test. It is intended to be the lowest level diagnostic run. **HOWEVER, IT DOES PROVIDE FOR OPTIONAL CACHE AND CIS TESTS.** THESE TESTS CAN BE SELECTED AND RUN IN MANUFACTURING ON THE MFG. QV STATION. THE TESTS ARE SPECIALLY DESIGNED TO EXERCISE THOSE SIGNALS ON THE CPU DATA PATH/CONTROL MODULES WHICH RELATE TO THE CACHE AND CIS. IT IS ASSUMED THAT CACHE AND CIS MODULES ARE KNOWN GOOD. RUNNING THESE TESTS ELIMINATE HAVING TO RUN THE CACHE AND CIS DIAGNOSTICS IN THE CPU APT QUICK VERIFY SCRIPT.

THE OPTIONAL TESTS ARE SELECTED THROUGH APT SCRIPTING OR BY LOADING BIT08 OF HARDWARE SWITCH REGISTER(177570). SEE SECTION 2.2.1.

### 2.4 EXECUTION TIMES

The diagnostic completes the first pass in less than 1 sec. Subsequent PRINTING OF END OF PASS MESSAGE REQUIRE APPROXIMATELY. 5 TO 10 SECS. INTERVALS  
The program will run continuously until externally Halted.

### 3.0 ERROR INFORMATION

#### 3.1 ERROR TYPES

There are two basic types of Errors in the diagnostic.

##### 3.1.1 FUNCTIONAL ERRORS

These are Errors which represent a malfunction of an Instruction or Sequence of Instruction. (E.G., the proper condition code not set or improper result of an Arithmetic or Logical Operation).

##### 3.1.2 SEQUENCE ERRORS

The result of a Test being executed out of Sequence. (E.G. Wild Machine or improper Branch or Jump).

#### 3.2 ERROR REPORTING PROCEDURES

The diagnostic responds to the detection of all Errors by storing certain information in Memory and Halting the Processor. The information stored in Memory can be used by the operator to identify the Error detected.

Certain failures will cause the Processor to Hang.

H 1

This type of failure is indicated if the program  
does not print its END OF PASS indication within a reasonable  
amount of time. (First message should appear within 1 sec.)

SEQ 0007

### 3.3 ERROR DESCRIPTOR INFORMATION

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The diagnostic Mailbox holds the Error information necessary to identify the detected Error. This information has been designed for compliance with the APT diagnostic interface specification. It is the primary medium for identifying Errors.

#### 3.3.1 \$MSGTYP

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This Location is incremented from zero to one before the program comes to a programmed Halt. If this Location is not one, then the diagnostic has come to an unprogrammed Halt. Check the Stack and PC for a clue to the cause. Suspect a Trap.

#### 3.3.2 \$FATAL

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This Location is Loaded with a number before a Halt is executed. Each programmed Halt has a unique number associated with it which can be used to identify the Error which has been detected.

#### 3.3.3 \$PASS

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This Location is incremented for every complete pass of the diagnostic. Monitoring the Location will indicate whether or not the program is Hung. It will also indicate the number of successful passes completed before the Error Halt. A high pass count might indicate that the Error Halt is associated with an intermittent fault.

#### 3.3.4 \$TESTN

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This Location is incremented in each new Subtest. This should indicate the Test being executed when the Error was detected. This Location is also used to detect a Sequence Error.

### 3.4 ERROR IDENTIFICATION

Because of the overhead associated with each Halt in an APT compatible program the sequence check code will share the Error Halt or Functional Error within each Subtest. To determine which Error is being reported, Locations \$FATAL and \$TESTN are used together. When an Error Halt occurs, check \$FATAL to determine the number of the Error detected. Now, check that the test number where this Error is detected corresponds to the value in \$TESTN. If these agree the Error was a Functional Error as described in the Listings. If these numbers do not agree, then a Sequence Error was detected. In this case \$TESTN will contain one more than the number of the last Test successfully completed. Sequence Errors which share the Error Halts of Functional Errors will always be reported by the last Halt in Subtest in which they were discovered.

### 4.0 PROGRESS REPORT

The message CKKAAAO 11/44 CPU/EIS is printed on the console Teletype after the first PASS, and following every subsequent 400 PASSES.

## 5.0 TROUBLE SHOOTING

When the program discovers a Fault it will Halt. to determine the cause of the Halt, the diagnostic provides Error information. This information is stored in the API mailbox and is the primary source of Error identification.

Upon finding an Error, the following procedure should aid in isolating the fault.

## 5.1 CHECK THE MAILBOX

1. \$MSGTY This Location should contain a 1. if the Processor Halts and this Location is zero, then the processor has come to an unexpected Halt. First suspect a Trap. Check the PC and if a Trap check R6 and the stack for the Location of the failing instruction.
2. \$FATAL This location is used to hold the number of the error which has detected. Each Error being checked by the diagnostic is assigned a unique number which is stored in \$FATAL when that Error is detected.

When an Error is detected, check the listing to see that the Error number stored in \$FATAL is one which is detected in the test whose number is in \$TESTN. If there is a disagreement then the Error being reported is a Sequence Error. \$TESTN contains one more than the last test which was successfully completed.

3. \$TESTN This Location is used to indicate the number of the test which was being executed when the fault was detected. \$TESTN is used in conjunction with \$FATAL to distinguish between Sequence and Functional Errors. (See 2. this Section)
4. \$PASS This Location is used to indicate the number of successful passes which the diagnostic has completed. This will give an indication that the diagnostic has not just been Hung in a Loop

If an Error has been detected \$PASS will show whether it was a Hard Error discovered during the first try or whether it was intermittent or developed during the running of the diagnostic.

5.2 SCOPING  
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While this diagnostic is primarily intended to be a fault detection program, provisions are made to assist a technician who might want to use the program as a trouble shooting test.

The procedure for scoping a Subtest involves modifying several Memory Locations in the test itself. The philosophy is to provide a Scoping Loop which will include the code where the Error was detected. The Loop is set up so that the Loop will not be terminated should the Error intermittantly disappear.

The procedure is as follows:

1. Determine which Error is to be Scoped. Use \$FATAL and \$TESTN for this (See above)
2. Locate the Error routine in the listing.
3. Clear the right Byte of the Conditional Branch Instruction associated with the Error. (This is marked with <===='s in the listing.)
4. Replace the Instruction following <MOV #XXX,-(R2) with the Scoping Branch provided in the listing comments.
5. Restart the program. The program may be restarted from the beginning or from the Subtest (See 2.0).

6.0 LISTING  
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```

97 .TITLE CKKAAAO 11/44 CPU/EIS
98 000000 .ENABLE ABS
99 001000 STBOT=1000
100 .NLIST CND,MC,MD
101 .LIST ME
102 000240 SCOPE=NOP
103 000007 R7=%7
104 000006 R6=%6
105 177776 PS=177776
106 177564 TPS=177564
107 177566 TPB=177566
108 140000 USRM=140000
109 030000 PUSRMM=30000
110 177772 PIRQ=177772
111 000020 BIT4=20
112 000007 MFPT=7
120 .MCALL .SAPTHDR,.SAPTBLS,.SACT11
121 .MCALL .SCATCH,.1170
122 .SBTTL BASIC DEFINITIONS
;*INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***
001100 STACK= 1100      ;:FIRST ADDRESS OF THE STACK
001100 KERSTK= STACK   ;:KERNEL STACK
000700 SUPSTK= STACK-200 ;:SUPERVISOR STACK
000600 USESTK= STACK-300 ;:USER STACK
104000 ERROR=EMT
000004 SCOPE=IOT
177776 PS= 177776      ;:PROCESSOR STATUS WORD
177776 PSW=PS
177774 STKLMT= 177774  ;:STACK LIMIT REGISTER
177772 PIRQ= 177772    ;:PROGRAM INTERRUPT REQUEST REGISTER
177570 DSWR= 177570    ;:HARDWARE SWITCH REGISTER
177570 DDISP= 177570   ;:HARDWARE DISPLAY REGISTER
177546 LKS= 177546     ;:LINE CLOCK (KW11-L) STATUS REGISTER
;*MISCELLANEOUS DEFINITIONS
000011 HT= 11          ;:CODE FOR HORIZONTAL TAB
000012 LF= 12          ;:CODE LINE FEED
000015 CR= 15          ;:CODE CARRIAGE RETURN
000200 CRLF= 200       ;:CODE FOR CARRIAGE RETURN-LINE FEED
;*GENERAL PURPOSE REGISTER DEFINITIONS
000000 R0= %0           ;:GENERAL REGISTER
000001 R1= %1           ;:GENERAL REGISTER
000002 R2= %2           ;:GENERAL REGISTER
000003 R3= %3           ;:GENERAL REGISTER
000004 R4= %4           ;:GENERAL REGISTER
000005 R5= %5           ;:GENERAL REGISTER
000006 R6= %6           ;:GENERAL REGISTER
000007 R7= %7           ;:GENERAL REGISTER
000000 R10=R0
000001 R11=R1
000002 R12=R2
000003 R13=R3
000004 R14=R4
000005 R15=R5
000006 SP= %6           ;:STACK POINTER
000006 KSP=SP
000006 SSP=SP
000006 USP=SP

```

000007 PC= %7 ;PROGRAM COUNTER  
;\*PRIORITY LEVEL DEFINITIONS  
000000 PR0= 0 ;PRIORITY LEVEL 0  
000040 PR1= 40 ;PRIORITY LEVEL 1  
000100 PR2= 100 ;PRIORITY LEVEL 2  
000140 PR3= 140 ;PRIORITY LEVEL 3  
000200 PR4= 200 ;PRIORITY LEVEL 4  
000240 PR5= 240 ;PRIORITY LEVEL 5  
000300 PR6= 300 ;PRIORITY LEVEL 6  
000340 PR7= 340 ;PRIORITY LEVEL 7  
;\*SWITCH REGISTER" SWITCH DEFINITIONS  
100000 SW15= 100000  
040000 SW14= 40000  
020000 SW13= 20000  
010000 SW12= 10000  
004000 SW11= 4000  
002000 SW10= 2000  
001000 SW09= 1000  
000400 SW08= 400  
000200 SW07= 200  
000100 SW06= 100  
000040 SW05= 40  
000020 SW04= 20  
000010 SW03= 10  
000004 SW02= 4  
000002 SW01= 2  
000001 SW00= 1  
001000 SW9=SW09  
000400 SW8=SW08  
000200 SW7=SW07  
000100 SW6=SW06  
000040 SW5=SW05  
000020 SW4=SW04  
000010 SW3=SW03  
000004 SW2=SW02  
000002 SW1=SW01  
000001 SW0=SW00  
;\*DATA BIT DEFINITIONS (BIT00 TO BIT15)  
100000 BIT15= 100000  
040000 BIT14= 40000  
020000 BIT13= 20000  
010000 BIT12= 10000  
004000 BIT11= 4000  
002000 BIT10= 2000  
001000 BIT09= 1000  
000400 BIT08= 400  
000200 BIT07= 200  
000100 BIT06= 100  
000040 BIT05= 40  
000020 BIT04= 20  
000010 BIT03= 10  
000002 BIT02= 4  
000001 BIT01= 2  
001000 BIT00= 1  
BIT9=BIT09  
BIT8=BIT08  
BIT7=BIT07

000100                   BIT6=BIT06  
000040                   BIT5=BIT05  
000020                   BIT4=BIT04  
000010                   BIT3=BIT03  
000004                   BIT2=BIT02  
000002                   BIT1=BIT01  
000001                   BIT0=BIT00  
  
;\*BASIC "CPU" TRAP VECTOR ADDRESSES  
000004                   ERRVEC= 4                   ; TIME OUT AND OTHER ERRORS  
000010                   RESVEC= 10                  ; RESERVED AND ILLEGAL INSTRUCTIONS  
000014                   TBITVEC=14                  ; 'T' BIT  
000014                   TRTVEC= 14                  ; TRACE TRAP  
000014                   BPTVEC= 14                  ; BREAKPOINT TRAP (BPT)  
000020                   IOTVEC= 20                  ; INPUT/OUTPUT TRAP (IOT) \*\*SCOPE\*\*  
000024                   PWRVEC= 24                  ; POWER FAIL  
000030                   EMTVEC= 30                  ; EMULATOR TRAP (EMT) \*\*ERROR\*\*  
000034                   TRAPVEC=34                  ; 'TRAP' TRAP  
000060                   TKVEC= 60                  ; TTY KEYBOARD VECTOR  
000064                   TPVEC= 64                  ; TTY PRINTER VECTOR  
000100                   LKVEC= 100                 ; LINE CLOCK (KW11-L) VECTOR  
000114                   CACHVEC=114                 ; CACHE ERROR INTERRUPT VECTOR  
000240                   PIRQVEC=240                 ; PROGRAM INTERRUPT REQUEST VECTOR  
000250                   MMVEC= 250                 ; MEMORY MANAGEMENT VECTOR  
  
.SBTTL CACHE REGISTER DEFINITIONS  
177740                   LOADRS = 177740           ; LOWER 16 BITS OF ADDRESS THAT CAUSED ERROR  
177742                   HIADRS = 177742           ; UPPER SIX BITS OF ADDRESS THAT CAUSED ERROR  
177744                   MEMERR = 177744           ; CACHE ERROR REGISTER  
177746                   CONTRL = 177746           ; MEMORY CONTROL REGISTER  
177750                   MAINT = 177750           ; MEMORY MAINTENENCE REGISTER  
177752                   HITMIS = 177752           ; HIT MISS REGISTER '1' IMPLIES HIT IN CACHE  
  
.SBTTL CPU REGISTER DEFINITIONS  
177760                   SIZELO = 177760           ; MEMORY SIZE REGISTER NUMBER TO PUT INTO A PAR  
177762                   SIZEHI = 177762           ; TO GET TO THE LAST 32 WORDS OF MEMORY  
177764                   SYSTID = 177764           ; HIGH SIZE REGISTER, RESERVED FOR FUTURE USE  
177766                   CPUERR = 177766           ; CURRENTLY ALL ZERO  
177766                   CPUERR = 177766           ; SYSTEM ID REGISTER  
177766                   CPUERR = 177766           ; CPU ERROR REGISTER HOLDS CONDITION THAT CAUSED  
177766                   CPUERR = 177766           ; THE TRAP TO ERRVEC (000004)  
  
.SBTTL MEMORY MANAGEMENT DEFINITIONS  
;\*MEMORY MANAGEMENT STATUS REGISTER ADDRESSES  
177572                   MMR0= 177572  
177574                   MMR1= 177574  
177576                   MMR2= 177576  
172516                   MMR3= 172516  
177572                   SR0=MMR0  
177574                   SR1=MMR1  
177576                   SR2=MMR2  
172516                   SR3=MMR3  
  
;\*USER "I" PAGE DESCRIPTOR REGISTERS  
177600                   UIPDR0= 177600  
177602                   UIPDR1= 177602  
177604                   UIPDR2= 177604  
177606                   UIPDR3= 177606  
177610                   UIPDR4= 177610  
177612                   UIPDR5= 177612  
177614                   UIPDR6= 177614  
177616                   UIPDR7= 177616

\*USER 'D' PAGE DESCRIPTOR REGISTERS  
177620 UDPDR0= 177620  
177622 UDPDR1= 177622  
177624 UDPDR2= 177624  
177626 UDPDR3= 177626  
177630 UDPDR4= 177630  
177632 UDPDR5= 177632  
177634 UDPDR6= 177634  
177636 UDPDR7= 177636  
\*USER 'I' PAGE ADDRESS REGISTERS  
177640 UIPAR0= 177640  
177642 UIPAR1= 177642  
177644 UIPAR2= 177644  
177646 UIPAR3= 177646  
177650 UIPAR4= 177650  
177652 UIPAR5= 177652  
177654 UIPAR6= 177654  
177656 UIPAR7= 177656  
\*USER 'D' PAGE ADDRESS REGISTERS  
177660 UDPAR0= 177660  
177662 UDPAR1= 177662  
177664 UDPAR2= 177664  
177666 UDPAR3= 177666  
177670 UDPAR4= 177670  
177672 UDPAR5= 177672  
177674 UDPAR6= 177674  
177676 UDPAR7= 177676  
\*SUPERVISOR 'I' PAGE DESCRIPTOR REGISTERS  
172200 SIPDR0= 172200  
172202 SIPDR1= 172202  
172204 SIPDR2= 172204  
172206 SIPDR3= 172206  
172210 SIPDR4= 172210  
172212 SIPDR5= 172212  
172214 SIPDR6= 172214  
172216 SIPDR7= 172216  
\*SUPERVISOR 'D' PAGE DESCRIPTOR REGISTERS  
172220 SDPDR0= 172220  
172222 SDPDR1= 172222  
172224 SDPDR2= 172224  
172226 SDPDR3= 172226  
172230 SDPDR4= 172230  
172232 SDPDR5= 172232  
172234 SDPDR6= 172234  
172236 SDPDR7= 172236  
\*SUPERVISOR 'I' PAGE ADDRESS REGISTERS  
172240 SIPAR0= 172240  
172242 SIPAR1= 172242  
172244 SIPAR2= 172244  
172246 SIPAR3= 172246  
172250 SIPAR4= 172250  
172252 SIPAR5= 172252  
172254 SIPAR6= 172254  
172256 SIPAR7= 172256  
\*SUPERVISOR 'D' PAGE ADDRESS REGISTERS  
172260 SDPAR0= 172260  
172262 SDPAR1= 172262

172264 SDPAR2= 172264  
172266 SDPAR3= 172266  
172270 SDPAR4= 172270  
172272 SDPAR5= 172272  
172274 SDPAR6= 172274  
172276 SDPAR7= 172276  
;\*KERNEL "I" PAGE DESCRIPTOR REGISTERS  
172300 KIPDR0= 172300  
172302 KIPDR1= 172302  
172304 KIPDR2= 172304  
172306 KIPDR3= 172306  
172310 KIPDR4= 172310  
172312 KIPDR5= 172312  
172314 KIPDR6= 172314  
172316 KIPDR7= 172316  
;\*KERNEL "D" PAGE DESCRIPTOR REGISTERS  
172320 KDPDR0= 172320  
172322 KDPDR1= 172322  
172324 KDPDR2= 172324  
172326 KDPDR3= 172326  
172330 KDPDR4= 172330  
172332 KDPDR5= 172332  
172334 KDPDR6= 172334  
172336 KDPDR7= 172336  
;\*KERNEL "I" PAGE ADDRESS REGISTERS  
172340 KIPAR0= 172340  
172342 KIPAR1= 172342  
172344 KIPAR2= 172344  
172346 KIPAR3= 172346  
172350 KIPAR4= 172350  
172352 KIPAR5= 172352  
172354 KIPAR6= 172354  
172356 KIPAR7= 172356  
;\*KERNEL "D" PAGE ADDRESS REGISTERS  
172360 KDPAR0= 172360  
172362 KDPAR1= 172362  
172364 KDPAR2= 172364  
172366 KDPAR3= 172366  
172370 KDPAR4= 172370  
172372 KDPAR5= 172372  
172374 KDPAR6= 172374  
172376 KDPAR7= 172376  
.SBTTL UNIBUS MAP REGISTER DEFINITIONS  
;\*THE LOWER 16 BITS OF THE MAP REGISTERS ARE LABELED "MAPLXX"  
;\*THE UPPER 6 BITS OF THE MAP REGISTERS ARE LABELED "MAPHXX"  
170200 MAPL00 = 170200  
170202 MAPH00 = 170202  
170204 MAPL01 = 170204  
170206 MAPH01 = 170206  
170210 MAPL02 = 170210  
170212 MAPH02 = 170212  
170214 MAPL03 = 170214  
170216 MAPH03 = 170216  
170220 MAPL04 = 170220  
170222 MAPH04 = 170222  
170224 MAPL05 = 170224  
170226 MAPH05 = 170226

170230	MAPL06 = 170230
170232	MAPH06 = 170232
170234	MAPL07 = 170234
170236	MAPH07 = 170236
170240	MAPL10 = 170240
170242	MAPH10 = 170242
170244	MAPL11 = 170244
170246	MAPH11 = 170246
170250	MAPL12 = 170250
170252	MAPH12 = 170252
170254	MAPL13 = 170254
170256	MAPH13 = 170256
170260	MAPL14 = 170260
170262	MAPH14 = 170262
170264	MAPL15 = 170264
170266	MAPH15 = 170266
170270	MAPL16 = 170270
170272	MAPH16 = 170272
170274	MAPL17 = 170274
170276	MAPH17 = 170276
170300	MAPL20 = 170300
170302	MAPH20 = 170302
170304	MAPL21 = 170304
170306	MAPH21 = 170306
170310	MAPL22 = 170310
170312	MAPH22 = 170312
170314	MAPL23 = 170314
170316	MAPH23 = 170316
170320	MAPL24 = 170320
170320	MAPH24 = 170320
170324	MAPL25 = 170324
170326	MAPH25 = 170326
170330	MAPL26 = 170330
170332	MAPH26 = 170332
170334	MAPL27 = 170334
170336	MAPH27 = 170336
170340	MAPL30 = 170340
170342	MAPH30 = 170342
170344	MAPL31 = 170344
170346	MAPH31 = 170346
170350	MAPL32 = 170350
170352	MAPH32 = 170352
170354	MAPL33 = 170354
170356	MAPH33 = 170356
170360	MAPL34 = 170360
170362	MAPH34 = 170362
170364	MAPL35 = 170364
170366	MAPH35 = 170366
170370	MAPL36 = 170370
170372	MAPH36 = 170372
170374	MAPL37 = 170374
170376	MAPH37 = 170376
170200	MAPL0=MAPL00
170202	MAPH0=MAPH00
170204	MAPL1=MAPL01
170206	MAPH1=MAPH01
170210	MAPL2=MAPL02



```

:SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
;*****$X=. ;:SAVE CURRENT LOCATION
;*****.=24 ;:SET POWER FAIL TO POINT TO START OF PROGRAM
;*****.200 ;:FOR APT START UP
;*****.=44 ;:POINT TO APT INDIRECT ADDRESS PNTR.
;*****.$APTHDR ;:POINT TO APT HEADER BLOCK
;*****.=.$X ;:RESET LOCATION COUNTER
;*****$APTHD:
;*****$HIBTS: .WORD 0 ;:TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
;*****$MBADR: .WORD $MAIL ;:ADDRESS OF APT MAILBOX (BITS 0-15)
;*****$TSTM: .WORD 10 ;:RUN TIM OF LONGEST TEST
;*****$PASTM: .WORD 10 ;:RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
;*****$UNITM: .WORD 0 ;:ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
;*****.WORD $ETEND-$MAIL/2 ;:LENGTH MAILBOX-ETABLE(WORDS)

128
129
130
131
132 000004 036370
133 000006 000000
134 000010 036400
135 000012 000000
136 000014 036410
137 000016 000000
138
139 000030 036420
140 000032 000000
141 000034 036430
142 000036 000000
143
144 000114 036440
145 000116 000000
146
147 000244 036450
148 000246 000000
149 000250 036460
150 000252 000000
151
152
153
154
155 000370 000000
156 000370 000000 000000 000000
157 000376 000000 000000 000000
158 000404 000001 000001 177777
159
160
161
162
163 000200 000157 000674
164
165 000204 012706 001000

:SET UP STARTING ADDRESS
:$X=.
.=200
JMP    START
MOV    #STBOT,R6          ;SET STACK POINTER

```

166 000210	012702	000304	MOV	#\$TESTN,R2	;SET MAILBOX POINTER
167 000214	000137		JMP	a(PC)+	;JUMP TO SUBTEST
168 000216	000000		C		;ADDR. OF SUBTEST GOES HERE
169					
170	001100		=.SX		
171	000302		\$ERROR=\$FATAL		
172	000304		\$STSTNM=\$TESTN		
173 001100	012737	036254 000024	START:	MOV #PWRDN,a#24	:SET UP FOR POWER FAIL
174 001106	012737	000000 000306		MOV #0,a#\$PASS	:CLEAR PASS COUNT
175 001114	012737	177777 036066		MOV #-1,a#\$PASSPT	:SET PRINT COUNTER
176 001122	012706	001000	RESTRRT:	MOV #STBOT,R6	:INITIALIZE STACK POINTER
177 001126	012702	000304		MOV #\$TESTN,R2	:SET UP POINTER TO MESSAGE TYPE
178 001132	012737	000000 000304		MOV #0,a#\$STSTNM	:CLEAR TEST NUMBER
179 001140	012737	000000 000302		MOV #0,a#\$ERROR	:CLEAR ERROR NUMBER
180 001146	012737	000000 000300		MOV #0,a#\$MSGTY	:CLEAR MESSAGE TYPE(FOR APT)

182

001154 005212  
 001156 022712 000001  
 001162 001024  
 183 001164 000257  
 184 001166 001401  
 185 001170 000404

:\*\*\*\*\*  
 :TEST 1 CHECK BRANCHES ON Z BIT  
 :\*\*\*\*\*  
 TST1: INC (R2) ;UPDATE TEST NUMBER  
 CMP #1, (R2) ;SEQUENCE ERROR?  
 BNE TST2-10 ;BR TO ERROR HALT ON SEQ ERROR  
 CCC ;CLEAR ALL CONDITION CODES  
 BEQ BR1 ;SHOULD BRANCH  
 BR BR2 ;BAD BRANCH OF Z-BIT  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 ; BRANCH INSTRUCTION AND <=====  
 ; REPLACE THE MOVE INSTRUCTION <=====  
 ; FOLLOWING W/ 774 <=====  
 ;

186  
 187  
 188  
 189  
 190 001172  
 001172 012742 000001  
 001176 005242  
 001200 000000  
 191 001202  
 001202 001004

BR1: MOV #1,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 1 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;SHOULD HAVE BRANCHED: Z=0  
 ;

001204 012742 000002  
 001210 005242  
 001212 000000  
 192 001214 000264  
 193 001216 001001  
 194 001220 000404

BR2: BNE BR3 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 ; CONDITIONAL BRANCH INST. AND <=====  
 ; REPLACE THE MOVE INSTRUCTION <=====  
 ; WHICH FOLLOWS W/ 767 <=====  
 ;  
 MOV #2,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 2 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;

195  
 196  
 197  
 198  
 199 001222  
 001222 012742 000003  
 001226 005242  
 001230 000000  
 200 001232  
 001232 001404

BR3: SEZ ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 BNE BR4 ;BRANCH INSTRUCTION AND <=====  
 BR BR5 ;REPLACE THE MOVE INSTRUCTION <=====  
 ; FOLLOWING W/ 760 <=====  
 ;  
 MOV #3,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 3 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;SHOULD NOT HAVE BRANCHED HERE ON Z=1  
 ;

001234 012742 000004  
 001240 005242  
 001242 000000

BR4: BEQ TST2 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 ; CONDITIONAL BRANCH INST. AND <=====  
 ; REPLACE THE MOVE INSTRUCTION <=====  
 ; WHICH FOLLOWS W/ 753 <=====  
 ;  
 MOV #4,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 4 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;SHOULD HAVE BRANCHED ON Z=1  
 ; OR SEQUENCE ERROR  
 ;

201  
 202  
 203  
 204  
 205  
 206  
 207  
 208  
 209  
 210

:\*\*\*\*\*  
 :SBTTL DATA PATH TESTS  
 :  
 : THE DATA PATH TESTS ARE USED TO VERIFY THAT VARIOUS  
 : DATA PATTERNS CAN BE SUCCESSFULLY MOVED THROUGH THE DATA PATHS  
 : MOVE AND COMPARE MODE 2,3 INSTRUCTIONS ARE USED TO PASS AND  
 : TEST VARIOUS DATA PATTERNS IN THE DATA PATHS.  
 : THE TEST EXERCISES THE INTERNAL DATA PATHS, THE UNIBUS  
 : DATA TRANSCIEVERS, AND AMUX CONTROL FOR ALU AND UBUS INPUTS.

211 : IF THESE TESTS FAIL, EXAMINE THE TARGET LOCATION (LOC. 0)  
212 : TO SEE WHICH BITS OF THE DATA PATH ARE FAILING. IF THIS PROVIDES  
213 : INCONCLUSIVE DATA, TRY TO CHECK MODE 3 IR DECODE BY RUNNING  
214 : JUST THE MICROCODE AND IR DECODE TESTS FOR THE MOVE AND COMPARE  
215 : INSTRUCTIONS.  
216

\*\*\*\*\*  
TEST 2 TEST OF ZEROES IN THE DATA PATH

001244	005212		TST2:	INC (R2)	:UPDATE TEST NUMBER	<====
001246	022712	000002		CMP #2,(R2)	:SEQUENCE ERROR?	<====
001252	001006			BNE TST3-10	:BR TO ERROR HALT ON SEQ ERROR	<====
217 001254	012737	000000	000000	MOV #0,a#0	:MOVE ZEROES THRU ADDRESS LINES, DATA	
218				TST a#0	:LINES AND INTERNAL PATHS	
219 001262	005737	000000		BEQ TST3	:SUCCESSFUL?	
220 001266	001404					
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<====
					CONDITIONAL BRANCH INST. AND	<====
					REPLACE THE MOVE INSTRUCTION	<====
					WHICH FOLLOWS W/ 771	<====
001270	012742	000005		MOV #5,-(R2)	:MOVE TO MAILBOX # ***** 5 *****	
001274	005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR	
001276	000000			HALT	:DATA INCORRECT	
					: OR SEQUENCE ERROR	

221  
222

\*\*\*\*\*  
TEST 3 TEST OF PATTERN 125252 IN DATA PATH

001300	005212		TST3:	INC (R2)	:UPDATE TEST NUMBER	<====
001302	022712	000003		CMP #3,(R2)	:SEQUENCE ERROR?	<====
001306	001007			BNE TST4-10	:BR TO ERROR HALT ON SEQ ERROR	<====
223 001310	012737	125252	000000	MOV #125252,a#0	:MOVE ALTERNATING ONES AND ZEROES	
224					:THRU DATA PATHS	
225 001316	022737	125252	000000	CMP #125252,a#0	:SUCCESSFUL	
226 001324	001404			BEQ TST4		
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<====
					CONDITIONAL BRANCH INST. AND	<====
					REPLACE THE MOVE INSTRUCTION	<====
					WHICH FOLLOWS W/ 770	<====
001326	012742	000006		MOV #6,-(R2)	:MOVE TO MAILBOX # ***** 6 *****	
001332	005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR	
001334	000000			HALT	:DATA INCORRECT	
					: OR SEQUENCE ERROR	

227  
228

\*\*\*\*\*  
TEST 4 TEST OF PATTERN 052525 IN DATA PATH

001336	005212		TST4:	INC (R2)	:UPDATE TEST NUMBER	<====
001340	022712	000004		CMP #4,(R2)	:SEQUENCE ERROR?	<====
001344	001007			BNE TST5-10	:BR TO ERROR HALT ON SEQ ERROR	<====
229 001346	012737	052525	000000	MOV #052525,a#0	:MOVE ALTERNATING ZEROES AND ONES	
230					:THRU DATA PATH	
231 001354	022737	052525	000000	CMP #052525,a#0	:SUCCESSFUL?	
232 001362	001404			BEQ TST5		
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<====
					CONDITIONAL BRANCH INST. AND	<====
					REPLACE THE MOVE INSTRUCTION	<====
					WHICH FOLLOWS W/ 770	<====

001364	012742	000007	MOV #7,-(R2)	:MOVE TO MAILBOX # ***** 7 *****
001370	005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
001372	000000		HALT	:DATA INCORRECT : OR SEQUENCE ERROR

233  
234

```
***** TEST 5 TEST OF ALL ONES IN DATA PATH *****
TST5: INC (R2) :UPDATE TEST NUMBER
      CMP #5,(R2) :SEQUENCE ERROR?
      BNE TST6-10 :BR TO ERROR HALT ON SEQ ERROR
      MOV #177777,a#0 :MOVE ONES THRU DATA PATH
      CMP #177777,a#0 :SUCCESSFUL
      BEQ TST6
```

235 001404 012737 177777 000000  
236 001412 022737 177777 000000  
237 001420 001404

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
: CONDITIONAL BRANCH INST. AND  
: REPLACE THE MOVE INSTRUCTION  
: WHICH FOLLOWS W/ 770 <=====  
<=====  
<=====  
<=====<=====

001422	012742	000010	MOV #10,-(R2)	:MOVE TO MAILBOX # ***** 10 *****
001426	005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
001430	000000		HALT	:DATA INCORRECT : OR SEQUENCE ERROR

238

```
***** SBTTL B-REGISTER TEST *****
: THE B-REGISTER SHIFTING LOGIC TESTS ARE USED TO TEST THAT THE
: B-REGISTER CAN HOLD VARIOUS DATA PATTERNS AND THAT THE ASSOCIATED
: LOGIC SUPPORTS THE SHIFTING FUNCTIONS WITHIN THE B-REGISTER AND C-BIT.
```

240  
241  
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243  
244  
245  
246  
247  
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249  
250  
251  
252  
253  
254

:A ONE IS SHIFTED THROUGH EVERY BIT IN THE B-REGISTER AND C-BIT IN
: BOTH DIRECTIONS.

: THE B-REGISTER ITSELF IS TESTED IN ITS ABILITY AS A BUFFER AND AS
: A SHIFT REGISTER. DATA IS ALSO PASSED THROUGH THE DATA PATH AND ALU,
: IF THESE TESTS FAIL, EXAMINE THE TARGET LOCATION (LOC. 0) TO SEE
: WHICH BITS OF THE B-REGISTER MAY BE FAILING. IF THIS PROVIDES
: INCONCLUSIVE DATA TRY TO CHECK THE MODE 3 IR DECODE BY RUNNING JUST
: THE MICROCODE AND IR DECODE TESTS FOR THE PARTICULAR INSTRUCTIONS.

```
***** TEST 6 SHIFT BIT 0 TO BIT 1 *****
TST6: INC (R2) :UPDATE TEST NUMBER
      CMP #6,(R2) :SEQUENCE ERROR?
      BNE TST7-10 :BR TO ERROR HALT ON SEQ ERROR
      CLC
```

255 001442 000241  
256 001444 012737 000001 000000  
257 001452 006137 000000  
258 001456 022737 000002 000000  
259 001464 001404

:CLEAR CARRY BIT
 MOV #1,a#0 :LOAD A 1
 ROL a#0 :SHIFT LEFT
 CMP #2,a#0 :SUCCESSFUL
 BEQ TST7

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
: CONDITIONAL BRANCH INST. AND  
: REPLACE THE MOVE INSTRUCTION  
: WHICH FOLLOWS W/ 765 <=====  
<=====  
<=====  
<=====<=====

001466	012742	000011	MOV #11,-(R2)	:MOVE TO MAILBOX # ***** 11 *****
001472	005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
001474	000000		HALT	:BIT 1 NOT SET : OR SEQUENCE ERROR

260  
261

;\*\*\*\*\*  
;TEST 7 SHIFT CARRY INTO BIT 0  
;\*\*\*\*\*  
001476 005212 TST7: INC (R2) ;UPDATE TEST NUMBER  
001500 022712 000007 CMP #7,(R2) ;SEQUENCE ERROR?  
001504 001017 BNE TST10-10 ;BR TO ERROR HALT ON SEQ ERROR  
262 001506 012737 000000 000000 MOV #0,a#0 ;CLEAR LOCATION  
263 001514 000261 SEC ;SET CARRY  
264 001516 006137 000000 ROL a#0 ;ROTATE CARRY BIT TO BIT 0  
265 001522 103014 BCC TST10 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 770 <=====  
;=====

001524 012742 000012  
001530 005242  
001532 000000  
266 001534 022737 000001 000000  
267 001542 001404

MOV #12,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 12 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;CARRY CLEAR  
; OR SEQUENCE ERROR  
CMP #1,a#0 ;BIT 0 SET  
BEQ TST10 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 760 <=====  
;=====

001544 012742 000013  
001550 005242  
001552 000000

MOV #13,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 13 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;BIT 0 NOT SET  
; OR SEQUENCE ERROR

268  
269

;\*\*\*\*\*  
;TEST 10 LEFT SHIFT FROM BIT 0 TO C-BIT  
;\*\*\*\*\*  
001554 005212 TST10: INC (R2) ;UPDATE TEST NUMBER  
001556 022712 000010 CMP #10,(R2) ;SEQUENCE ERROR?  
001562 001014 BNE TST11-10 ;BR TO ERROR HALT ON SEQ ERROR  
270 001564 012737 000001 000000 MOV #1,a#0 ;SET BIT 0  
271 001572 012700 177757 MOV #-21,R0 ;SET BIT COUNTER  
272 001576 000241 CLC ;CLEAR C-BIT  
273 001600 005200 SHL: INC R0 ;INCREMENT BIT COUNTER  
274 001602 001404 BEQ SHLE ;BR TO ERROR HALT IF BIT IS LOST  
275 001604 006137 000000 ROL a#0 ;SHIFT LEFT ONE POSITION  
276 001610 103373 BCC SHL ;BRANCH IF C-BIT NOT SET  
277 001612 001404 BEQ TST11 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 763 <=====  
;=====

001614 012742 000014  
001614 005242  
001620 000000  
001622 000000

SHLE: MOV #14,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 14 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;LEFT SHIFTING LOGIC FAILED  
; OR SEQUENCE ERROR

278  
279

;\*\*\*\*\*  
;TEST 11 SHIFT BIT 15 TO BIT 14  
;\*\*\*\*\*

001624 005212 TST11: INC (R2) :UPDATE TEST NUMBER  
 001626 022712 000011 CMP #11,(R2) :SEQUENCE ERROR?  
 001632 001012 BNE TST12-10 :BR TO ERROR HALT ON SEQ ERROR  
 280 001634 012737 100000 000000 MOV #100000,a#0 :SET BIT 15  
 281 001642 000241 CLC :CLEAR CARRY  
 282 001644 006037 000000 ROR a#0 :SHIFT BIT 15 TO BIT 14  
 283 001650 022737 040000 000000 CMP #40000,a#0 :SUCCESSFUL  
 284 001656 001404 BEQ TST12  
 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 : CONDITIONAL BRANCH INST. AND  
 : REPLACE THE MOVE INSTRUCTION  
 : WHICH FOLLOWS W/ 765 <=====  
 001660 012742 000015 MOV #15,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 15 \*\*\*\*\*  
 001664 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 001666 000000 HALT :BIT 14 NOT SET  
 : OR SEQUENCE ERROR  
 285  
 286 :\*\*\*\*\* TEST 12 RIGHT SHIFT FROM BIT 15 TO C-BIT \*\*\*\*\*  
 001670 005212 TST12: INC (R2) :UPDATE TEST NUMBER  
 001672 022712 000012 CMP #12,(R2) :SEQUENCE ERROR?  
 001676 001014 BNE TST13-10 :BR TO ERROR HALT ON SEQ ERROR  
 287 001700 012737 100000 000000 MOV #100000,a#0 :SET BIT 15  
 288 001706 012700 177757 MOV #-21,R0 :SET BIT COUNTER  
 289 001712 000241 CLC :CLEAR C-BIT  
 290 001714 005200 SHR: INC R0 :INCREMENT BIT COUNTER  
 291 001716 001404 BEQ SHRE :BR TO ERROR HALT IF BIT IS LOST  
 292 001720 006037 000000 ROR a#0 :ROTATE RIGHT ONE POSITION  
 293 001724 103373 BCC SHR :BRANCH IF C-BIT CLEAR  
 294 001726 001404 BEQ TST13  
 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 : CONDITIONAL BRANCH INST. AND  
 : REPLACE THE MOVE INSTRUCTION  
 : WHICH FOLLOWS W/ 763 <=====  
 001730 SHRE:  
 001730 012742 000016 MOV #16,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 16 \*\*\*\*\*  
 001734 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 001736 000000 HALT :RIGHT SHIFT LOGIC FAILED  
 : OR SEQUENCE ERROR  
 295  
 296  
 297 :\*\*\*\*\* SBTTL SCRATCH PAD TESTS \*\*\*\*\*  
 298  
 299 : THE SCRATCH PAD TESTS ARE USED TO VERIFY THAT VARIOUS  
 300 : DATA PATTERNS CAN BE SUCCESSFULLY HELD IN THE SCRATCH PAD  
 301 : CIRCUITRY. MOVE AND COMPARE INSTRUCTIONS ARE USED TO TEST THAT  
 302 : R0 CAN HOLD VARIOUS DATA PATTERNS. EACH DATA PATTERN IS  
 303 : MOVED AND TESTED IN A SMALL LOOP CONVENIENT FOR SCOPING. THE  
 304 : SUCCESSFUL COMPLETION OF THESE TESTS SHOULD VERIFY THE CIRCUITRY EXTERNAL  
 305 : TO THE SCRATCH PAD ITSELF.  
 306 : THE REMAINDER OF THE GENERAL REGISTERS ARE TESTED BY MOVING  
 307 : A BIT INTO BIT 0 OF THE REGISTER AND SHIFTING IT LEFT ONE  
 308 : BIT AT A TIME INTO THE CARRY BIT. THE RESULT IS THEN CHECKED TO INSURE THAT  
 309 : NO BITS WERE PICKED. THE PROCEDURE IS THEN REPEATED UNDER OPPOSITE  
 310 : CONDITIONS. THE GENERAL REGISTER AND THE CARRY BIT ARE SET TO  
 311 : ALL ONES, AND A ZERO IS SHIFTED LEFT FROM BIT 0 INTO THE CARRY BIT.

312 :THE RESULT IS THEN CHECKED TO INSURE THAT NO ZEROES WERE PICKED.  
 313 :AT THIS POINT ALL OF THE GENERAL REGISTERS HAVE BEEN EXERCISED  
 314 :AS WELL AS REGISTER 11. REGISTERS 10 AND 12 HAVE BEEN ACCESSED BY  
 315 :THE INSTRUCTIONS. REGISTERS 13,14,AND 17 WILL BE TESTED LATER IN THE  
 316 :MICROCODE TESTS.  
 317 :IF THE PATTERN TESTS WITH REGISTER 0 FAIL CHECK THE RESULTANT  
 318 :DATA FOR A CLUE TO A FAULT IN THE EXTERNAL CIRCUITRY. IF THE  
 319 :PATTERN TESTS WITH R0 ARE SUCCESSFUL BUT THE TESTS WITH THE OTHER  
 320 :REGISTERS FAIL, SUSPECT THE REGISTER SELECT LINES AND THEN THE SCRATCH  
 321 :PAD ITSELF.  
 322  
 323

			TEST 13 TEST IF R0 CAN HOLD ALL ZEROES		
001740	005212		TST13:	INC (R2)	:UPDATE TEST NUMBER
001742	022712	000013		CMP #13,(R2)	:SEQUENCE ERROR?
001746	001004			BNE TST14-10	:BR TO ERROR HALT ON SEQ ERROR
324					
325	001750	012700	000000	MOV #0,R0	:MOVE ZEROES TO R0
326	001754	005700		TST R0	:SUCCESSFUL?
327	001756	001404		BEQ TST14	
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 773
					<==== <==== <==== <====
001760	012742	000017	MOV #17,-(R2)		:MOVE TO MAILBOX # ***** 17 *****
001764	005242		INC -(R2)		:SET MSGTYP TO FATAL ERROR
001766	000000		HALT		:R0 NOT 0 : OR SEQUENCE ERROR
328					
329					
			TEST 14 TEST IF R0 CAN HOLD ONES AND ZEROES		
001770	005212		TST14:	INC (R2)	:UPDATE TEST NUMBER
001772	022712	000014		CMP #14,(R2)	:SEQUENCE ERROR?
001776	001005			BNE TST15-10	:BR TO ERROR HALT ON SEQ ERROR
330	002000	012700	125252	MOV #125252,R0	:MOVE ALTERNATING ONES AND ZEROES TO R0
331	002004	020027	125252	CMP R0,#125252	:SUCCESSFUL?
332	002010	001404		BEQ TST15	
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 772
					<==== <==== <==== <====
002012	012742	000020	MOV #20,-(R2)		:MOVE TO MAILBOX # ***** 20 *****
002016	005242		INC -(R2)		:SET MSGTYP TO FATAL ERROR
002020	000000		HALT		:R0 NOT 125252 : OR SEQUENCE ERROR
333					
334					
			TEST 15 TEST IF R0 CAN HOLD ZEROES AND ONES		
002022	005212		TST15:	INC (R2)	:UPDATE TEST NUMBER
002024	022712	000015		CMP #15,(R2)	:SEQUENCE ERROR?
002030	001005			BNE TST16-10	:BR TO ERROR HALT ON SEQ ERROR
335	002032	012700	052525	MOV #052525,R0	:MOVE ALTERNATING ZEROES AND ONES TO R0
336	002036	020027	052525	CMP R0,#052525	:SUCCESSFUL?
337	002042	001404		BEQ TST16	

002044 012742 000021  
002050 005242  
002052 000000

MOV #21,-(R2)  
INC -(R2)  
HALT

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 772 <=====  
; MOVE TO MAILBOX # \*\*\*\*\* 21 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; R0 NOT 52525  
; OR SEQUENCE ERROR <=====

338  
339

002054 005212  
002056 022712 000016  
002062 001005  
340 002064 012700 177777  
341 002070 020027 177777  
342 002074 001404

:TEST 16 TEST IF R0 CAN HOLD ALL ONES  
TST16: INC (R2) ;UPDATE TEST NUMBER  
CMP #16,(R2) ;SEQUENCE ERROR?  
BNE TST17-10 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #177777,R0 ;MOVE ALL ONES TO R0  
CMP R0,#177777 ;SUCCESSFUL?  
BEQ TST17

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 772 <=====  
; MOVE TO MAILBOX # \*\*\*\*\* 22 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; R0 NOT 177777  
; OR SEQUENCE ERROR <=====

002076 012742 000022  
002102 005242  
002104 000000

MOV #22,-(R2)  
INC -(R2)  
HALT

343  
344

002106 005212  
002110 022712 000017  
002114 001012  
345 002116 012701 000001  
346 002122 012700 177757  
347 002126 000241  
348 002130 005200  
349 002132 001403  
350 002134 006101  
351 002136 103374  
352 002140 001404

:TEST 17 TEST IF R1 CAN HOLD A ONE IN ALL BITS  
TST17: INC (R2) ;UPDATE TEST NUMBER  
CMP #17,(R2) ;SEQUENCE ERROR?  
BNE TST20-10 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #1,R1 ;SET BIT 0  
MOV #-21,R0 ;SET BIT COUNTER  
CLC ;CLEAR C-BIT  
REG1: INC R0 ;INCREMENT BIT COUNTER  
BEQ REG1E ;BR TO ERROR HALT IF BIT IS LOST  
ROL R1 ;ROTATE 1 POSITION  
BCC REG1 ;ALL DONE  
BEQ TST20

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 765 <=====

002142 012742 000023  
002146 005242  
002150 000000

REG1E:  
MOV #23,-(R2)  
INC -(R2)  
HALT

; MOVE TO MAILBOX # \*\*\*\*\* 23 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; FAILURE WITH R1  
; OR SEQUENCE ERROR

353  
354

002152 005212  
002154 022712 000020  
002160 001014

:TEST 20 TEST IF R1 CAN HOLD A ZERO IN ALL BITS  
TST20: INC (R2) ;UPDATE TEST NUMBER  
CMP #20,(R2) ;SEQUENCE ERROR?  
BNE TST21-10 ;BR TO ERROR HALT ON SEQ ERROR

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T20 TEST IF R1 CAN HOLD A ZERO IN ALL BITS

SEQ 0028

355 002162 012701 177776		MOV #2,R1	:SET ALL ONES IN R1 EXCEPT FOR BIT 0
356 002166 012700 177757		MOV #21,R0	:SET BIT COUNTER
357 002172 000261		SEC	:SET C-BIT
358 002174 005200		INC R0	:INCREMENT COUNTER
359 002176 001405		BEQ R1ERR	:BR TO ERROR HALT IF COUNTER=0
360 002200 006101		ROL R1	:ROTATE 1 POSITION
361 002202 103774		BCS REG1A	:CONTINUE UNTIL C-BIT IS CLEAR
362 002204 022701 177777		CMP #1,R1	:CHECK DATA IN R1
363 002210 001404		BEQ TST21	
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
			CONDITIONAL BRANCH INST. AND <=====
			REPLACE THE MOVE INSTRUCTION <=====
			WHICH FOLLOWS W/ 763 <=====
002212		R1ERR:	
002212 012742 000024		MOV #24,-(R2)	:MOVE TO MAILBOX # ***** 24 *****
002216 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
002220 000000		HALT	:FAILURE WITH R1 OR SEQUENCE ERROR
364			*****
			:TEST 21 TEST IF R2 CAN HOLD A ONE IN ALL BITS
			*****
002222 005212		TST21: INC (R2)	:UPDATE TEST NUMBER
002224 022712 000021		CMP #21,(R2)	:SEQUENCE ERROR?
002230 001012		BNE REG2A-14	:BR TO ERROR HALT ON SEQ ERROR
365 002232 012702 000001		MOV #1,R2	:SET BIT 0
366 002236 012700 177757		MOV #21,R0	:SET BIT COUNTER
367 002242 000241		CLC	:CLEAR C-BIT
368 002244 005200		INC R0	:INCREMENT BIT COUNTER
369 002246 001403		BEQ REG2A-14	:BR TO ERROR HALT IF BIT IS LOST
370 002250 006102		ROL R2	:ROTATE 1 POSITION
371 002252 103374		BCC REG2	:ALL DONE
372 002254 001406		BEQ REG2A	
373			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
374			BRANCH INSTRUCTION AND <=====
375			REPLACE THE MOVE INSTRUCTION <=====
376			FOLLOWING W/ 771 <=====
377 002256 012702 000304		MOV #\$TESTN,R2	:RESTORE POINTER
378 002262 012742 000025		MOV #25,-(R2)	:MOVE TO MAILBOX # ***** 25 *****
002266 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
002270 000000		HALT	:FAILURE WITH R2
379 002272 012702 000304		REG2A: MOV #\$TESTN,R2	:RESTORE POINTER
380			*****
381			:TEST 22 TEST IF R2 CAN HOLD A ZERO IN ALL BITS
			*****
002276 005212		TST22: INC (R2)	:UPDATE TEST NUMBER
002300 022712 000022		CMP #22,(R2)	:SEQUENCE ERROR?
002304 001020		BNE TST23-10	:BR TO ERROR HALT ON SEQ ERROR
382 002306 012702 177776		MOV #2,R2	:SET ALL ONES IN R2 EXCEPT FOR BIT 0
383 002312 012700 177757		MOV #21,R0	:SET BIT COUNTER
384 002316 000261		SEC	:SET C-BIT
385 002320 005200		INC R0	:INCREMENT BIT COUNTER
386 002322 001407		BEQ R2ERR	:BR TO ERROR HALT IF COUNTER=0
387 002324 006102		ROL R2	:ROTATE 1 POSITION
388 002326 103774		BCS REG2B	:CONTINUE UNTIL C-BIT IS CLEAR
389 002330 022702 177777		CMP #1,R2	:CHECK DATA IN R2
390 002334 001406		BEQ REG2C	

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391 002336 012702 000304           MOV    #$TESTN,R2      ;RESTORE POINTER
392 002342           R2ERR:      MOV    #26,-(R2)      ;MOVE TO MAILBOX # ***** 26 *****
393 002342 012742 000026           INC    -(R2)        ;SET MSGTYP TO FATAL ERROR
394 002346 005242           HALT      ;FAILURE WITH R2
395 002350 000000           REG2C:      MOV    #$TESTN,R2      ;RESTORE POINTER
396 002352 012702 000304           :***** TEST 23 TEST IF R3 CAN HOLD A ONE IN ALL BITS *****
397 002356 005212           TST23:      INC    (R2)        ;UPDATE TEST NUMBER
398 002360 022712 000023           CMP    #23,(R2)      ;SEQUENCE ERROR?
399 002364 001012           BNE    TST24-10     ;BR TO ERROR HALT ON SEQ ERROR
400 002366 012703 000001           MOV    #1,R3        ;SET BIT 0
401 002372 012700 177757           MOV    #-21,RO      ;SET BIT COUNTER
402 002376 000241           REG3:      CLC      ;CLEAR C-BIT
403 002400 005200           INC    R0          ;INCREMENT BIT COUNTER
404 002402 001403           BEQ    REG3E      ;BR TO ERROR HALT IF BIT IS LOST
405 002404 006103           ROL    R3          ;ROTATE 1 POSITION
406 002406 103374           BCC    REG3      ;ALL DONE
407 002410 001404           BEQ    TST24      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
408 002412           REG3E:      MOV    #27,-(R2)      ;MOVE TO MAILBOX # ***** 27 *****
409 002412 012742 000027           INC    -(R2)        ;SET MSGTYP TO FATAL ERROR
410 002416 005242           HALT      ;FAILURE WITH R3
411 002420 000000           :***** TEST 24 TEST IF R3 CAN HOLD A ZERO IN ALL BITS *****
412 002422 005212           TST24:      INC    (R2)        ;UPDATE TEST NUMBER
413 002424 022712 000024           CMP    #24,(R2)      ;SEQUENCE ERROR?
414 002430 001014           BNE    TST25-10     ;BR TO ERROR HALT ON SEQ ERROR
415 002432 012703 177776           MOV    #-2,R3        ;SET ALL ONES IN R3 EXCEPT FOR BIT 0
416 002436 012700 177757           MOV    #-21,RO      ;SET BIT COUNTER
417 002442 000261           REG3A:      SEC      ;SET C-BIT
418 002444 005200           INC    R0          ;INCREMENT BIT COUNTER
419 002446 001405           BEQ    R3ERR      ;BR TO ERROR HALT IF COUNTER=0
420 002450 006103           ROL    R3          ;ROTATE 1 POSITION
421 002452 103774           BCS    REG3A      ;CONTINUE UNTIL C-BIT IS CLEAR
422 002454 022703 177777           CMP    #-1,R3        ;CHECK DATA
423 002460 001404           BEQ    TST25      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
424 002462           R3ERR:      MOV    #30,-(R2)      ;MOVE TO MAILBOX # ***** 30 *****
425 002462 012742 000030           INC    -(R2)        ;SET MSGTYP TO FATAL ERROR
426 002466 005242           HALT      ;FAILURE WITH R3
427 002470 000000           :***** *****

```

:TEST 25 TEST IF R4 CAN HOLD A ONE IN ALL BITS

\*\*\*\*\*

002472 005212	TST25: INC (R2)	;UPDATE TEST NUMBER
002474 022712	CMP #25, (R2)	;SEQUENCE ERROR?
002500 001012	BNE TST26-10	;BR TO ERROR HALT ON SEQ ERROR
417 002502 012704	MOV #1, R4	;SET BIT 0
418 002506 012700	MOV #21, R0	;SET BIT COUNTER
419 002512 000241	CLC	;CLEAR C-BIT
420 002514 005200	INC R0	;INCREMENT BIT COUNTER
421 002516 001403	BEQ REG4E	;BR TO ERROR HALT IF BIT IS LOST
422 002520 006104	ROL R4	;ROTATE 1 POSITION
423 002522 103374	BCC REG4	;ALL DONE
424 002524 001404	BEQ TST26	
		; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <===== ; CONDITIONAL BRANCH INST. AND <===== ; REPLACE THE MOVE INSTRUCTION <===== ; WHICH FOLLOWS W/ 765 <=====
002526 012742 000031	REG4E: MOV #31, -(R2)	;MOVE TO MAILBOX # ***** 31 *****
002532 005242	INC -(R2)	;SET MSGTYP TO FATAL ERROR
002534 000000	HALT	;FAILURE WITH R4 ; OR SEQUENCE ERROR

425

426 :TEST 26 TEST IF R4 CAN HOLD A ZERO IN ALL BITS

\*\*\*\*\*

002536 005212	TST26: INC (R2)	;UPDATE TEST NUMBER
002540 022712	CMP #26, (R2)	;SEQUENCE ERROR?
002544 001014	BNE TST27-10	;BR TO ERROR HALT ON SEQ ERROR
427 002546 012704	MOV #2, R4	;SET ALL ONES IN R4 EXCEPT FOR BIT 0
428 002552 012700	MOV #21, R0	;SET BIT COUNTER
429 002556 000261	SEC	;SET C-BIT
430 002560 005200	INC R0	;INCREMENT BIT COUNTER
431 002562 001405	BEQ R4ERR	;BR TO ERROR HALT IF COUNTER=0
432 002564 006104	ROL R4	;ROTATE 1 POSITION
433 002566 103774	BCS REG4A	;CONTINUE UNTIL C-BIT IS CLEAR
434 002570 022704	CMP #1, R4	;CHECK DATA
435 002574 001404	BEQ TST27	
		; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <===== ; CONDITIONAL BRANCH INST. AND <===== ; REPLACE THE MOVE INSTRUCTION <===== ; WHICH FOLLOWS W/ 763 <=====
002576 012742 000032	R4ERR: MOV #32, -(R2)	;MOVE TO MAILBOX # ***** 32 *****
002602 005242	INC -(R2)	;SET MSGTYP TO FATAL ERROR
002604 000000	HALT	;FAILURE WITH R4 ; OR SEQUENCE ERROR

436

437

438 :TEST 27 TEST IF R5 CAN HOLD A ONE IN ALL BITS

\*\*\*\*\*

002606 005212	TST27: INC (R2)	;UPDATE TEST NUMBER
002610 022712	CMP #27, (R2)	;SEQUENCE ERROR?
002614 001012	BNE TST30-10	;BR TO ERROR HALT ON SEQ ERROR
439 002616 012705	MOV #1, R5	;SET BIT 0
440 002622 012700	MOV #21, R0	;SET BIT COUNTER

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T27 TEST IF R5 CAN HOLD A ONE IN ALL BITS

SEQ 0031

441 002626 000241		CLC		:CLEAR C-BIT	
442 002630 005200		INC	R0	:INCREMENT BIT COUNTER	
443 002632 001403		BEQ	REG5E	:BR TO ERROR HALT IF BIT IS LOST	
444 002634 006105		ROL	R5	:ROTATE 1 POSITION	
445 002636 103374		BCC	REG5	:ALL DONE	
446 002640 001404		BEQ	TST30		
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
				CONDITIONAL BRANCH INST. AND	<=====
				REPLACE THE MOVE INSTRUCTION	<=====
				WHICH FOLLOWS W/ 765	<=====
002642		REG5E:			
002642 012742 000033		MOV	#33,-(R2)	:MOVE TO MAILBOX # ***** 33 *****	
002646 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
002650 000000		HALT		:FAILURE WITH R5	
				: OR SEQUENCE ERROR	
447					
448					
				:***** TEST 30 TEST IF R5 CAN HOLD A ZERO IN ALL BITS	
				:*****	
002652 005212		TST30:	INC	(R2)	:UPDATE TEST NUMBER
002654 022712	000030		CMP	#30,(R2)	:SEQUENCE ERROR?
002660 001014			BNE	TST31-10	:BR TO ERROR HALT ON SEQ ERROR
449 002662 012705	177776		MOV	#-2,R5	:SET ALL ONES IN R5 EXCEPT FOR BIT 0
450 002666 012700	177757		MOV	#-21,R0	:SET BIT COUNTER
451 002672 000261			SEC		:SET C-BIT
452 002674 005200		REG5A:	INC	R0	:INCREMENT BIT COUNTER
453 002676 001405			BEQ	R5ERR	:BR TO ERROR HALT IF COUNTER=0
454 002700 006105			ROL	"	:ROTATE 1 POSITION
455 002702 103774			BCS	REG5A	:CONTINUE UNTIL C-BIT IS C;EAR
456 002704 022705	177777		CMP	#-1,R5	:CHECK DATA
457 002710 001404			BEQ	TST31	
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
				CONDITIONAL BRANCH INST. AND	<=====
				REPLACE THE MOVE INSTRUCTION	<=====
				WHICH FOLLOWS W/ 763	<=====
002712		R5ERR:			
002712 012742 000034		MOV	#34,-(R2)	:MOVE TO MAILBOX # ***** 34 *****	
002716 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
002720 000000		HALT		:FAILURE WITH R5	
				: OR SEQUENCE ERROR	
458					
459					
				:***** TEST 31 TEST IF R6 CAN HOLD A ONE IN ALL BITS	
				:*****	
002722 005212		TST31:	INC	(R2)	:UPDATE TEST NUMBER
002724 022712	000031		CMP	#31,(R2)	:SEQUENCE ERROR?
002730 001012			BNE	TST32-10	:BR TO ERROR HALT ON SEQ ERROR
460 002732 012706	000001		MOV	#1,R6	:SET BIT 0
461 002736 012700	177757		MOV	#-21,R0	:SET BIT COUNTER
462 002742 000241			CLC		:CLEAR C-BIT
463 002744 005200		REG6:	INC	R0	:INCREMENT BIT COUNTER
464 002746 001403			BEQ	REG6E	:BR TO ERROR HALT IF BIT IS LOST
465 002750 006106			ROL	R6	:ROTATE 1 POSITION
466 002752 103374			BCC	REG6	:ALL DONE
467 002754 001404			BEQ	TST32	
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
				CONDITIONAL BRANCH INST. AND	<=====

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 765 <=====  
 002756 012742 000035 REG6E: MOV #35,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 35 \*\*\*\*\*  
 002756 005242 -INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 002762 000000 HALT ;FAILURE WITH R6  
 ; OR SEQUENCE ERROR

468  
 469 :TEST 32 TEST IF R6 CAN HOLD A ZERO IN ALL BITS  
 002766 005212 000032 TST32: INC (R2) ;UPDATE TEST NUMBER  
 002770 022712 000032 CMP #32,(R2) ;SEQUENCE ERROR?  
 002774 001014 BNE TST33-10 ;BR TO ERROR HALT ON SEQ ERROR  
 470 002776 012706 177776 MOV #2,R6 ;SET ALL ONES IN R6 EXCEPT FOR BIT 0  
 471 003002 012700 177757 MOV #21,R0 ;SET BIT COUNTER  
 472 003006 000261 SEC ;SET C-BIT  
 473 003010 005200 REG6A: INC R0 ;INCREMENT BIT COUNT  
 474 003012 001405 BEQ R6ERR ;BR TO ERROR HALT IF COUNTER=0  
 475 003014 006106 ROL R6 ;ROTATE 1 POSITION  
 476 003016 103774 BCS REG6A ;CONTINUE UNTIL C-BIT IS CLEAR  
 477 003020 022706 177777 CMP #1,R6 ;CHECK DATA  
 478 003024 001404 BEQ TST33 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 763 <=====

003026 012742 000036 R6ERR: MOV #36,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 36 \*\*\*\*\*  
 003026 005242 -INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 003032 000000 HALT ;FAILURE WITH R6  
 ; OR SEQUENCE ERROR

479  
 480  
 481 SBTTL PSW TESTS  
 482  
 483 THE PSW TESTS ARE USED TO VERIFY THAT VARIOUS DATA  
 484 PATTERNS CAN BE SUCCESSFULLY HELD IN THE PSW AND THAT THE  
 485 PSW ADDRESSING LOGIC IS FUNCTIONING. MOVE AND COMPARE INSTRUCTIONS  
 486 ARE USED TO TEST THAT THE PSW CAN HOLD VARIOUS DATA PATTERNS.  
 487 EACH DATA PATTERN IS MOVED AND TESTED IN A SMALL LOOP CONVENIENT FOR  
 488 SCOPING.  
 489 THE PSW REGISTER ITSELF IS TESTED AS WELL AS THE ADDRESS  
 490 SELECT CIRCUITRY. THE AMUX INPUTS TO THE PSW MUX ARE TESTED. THE  
 491 CC INPUTS ARE TESTED LATER IN THE MICROCODE TESTS. SETTING OF  
 492 THE T-BIT BY THE TEST PATTERNS IS PURPOSELY AVOIDED; TESTING OF THE  
 493 T-BIT TRAP CIRCUITRY IS LEFT FOR THE TRAP TEST.

494  
 495 :TEST 33 TEST IF PSW WILL HOLD ZEROS  
 003036 005212 000033 TST33: INC (R2) ;UPDATE TEST NUMBER  
 003040 022712 000033 CMP #33,(R2) ;SEQUENCE ERROR?  
 003044 001010 BNE TST34-10 ;BR TO ERROR HALT ON SEQ ERROR  
 496 003046 012706 001000 MOV #STBOT,R6  
 497 003052 012737 000000 177776 MOV #0,0#PS ;SET PSW TO ZERO  
 498 003060 005737 177776 TST 0#PS ;SUCCESSFUL

499 003064 001404

BEQ TST34

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 767 <=====  
; MOVE TO MAILBOX # \*\*\*\*\* 37 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; PSW NOT 0  
; OR SEQUENCE ERROR

003066 012742 000037  
003072 005242  
003074 000000

MOV #37,-(R2)  
INC -(R2)  
HALT

500  
501

;\*\*\*\*\* TEST 34 TEST IF PSW WILL HOLD ONES AND ZEROES \*\*\*\*\*

003076 005212 000034  
003100 022712  
003104 001007  
502 003106 012737 000252 177776  
503 003114 023727 177776 000252  
504 003122 001404

TST34: INC (R2) ;UPDATE TEST NUMBER  
CMP #34,(R2) ;SEQUENCE ERROR?  
BNE TST35-10 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #252,&PS ;MOVE ALT. ONES AND ZEROES TO PSW  
CMP &PS,#252 ;SUCCESSFUL?  
BEQ TST35

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 770 <=====  
; MOVE TO MAILBOX # \*\*\*\*\* 40 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; PSW NOT 252  
; OR SEQUENCE ERROR

003124 012742 000040  
003130 005242  
003132 000000

MOV #40,-(R2)  
INC -(R2)  
HALT

505  
506

;\*\*\*\*\* TEST 35 TEST IF PSW (EXCEPT T-BIT) WILL HOLD 0'S & 1'S \*\*\*\*\*

003134 005212 000035  
003136 022712  
003142 001007  
507 003144 012737 000105 177776  
508 003152 023727 177776 000105  
509 003160 001404

TST35: INC (R2) ;UPDATE TEST NUMBER  
CMP #35,(R2) ;SEQUENCE ERROR?  
BNE TST36-10 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #105,&PS ;MOVE ALT. ONES AND ZEROES TO PSW  
CMP &PS,#105 ;SUCCESSFUL?  
BEQ TST36

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 770 <=====  
; MOVE TO MAILBOX # \*\*\*\*\* 41 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; PSW NOT 105  
; OR SEQUENCE ERROR

003162 012742 000041  
003166 005242  
003170 000000

MOV #41,-(R2)  
INC -(R2)  
HALT

510  
511

;\*\*\*\*\* TEST 36 TEST IF PSW (EXCEPT T-BIT) WILL HOLD ALL ONES \*\*\*\*\*

003172 005212 000036  
003174 022712  
003200 001007  
512 003202 012737 000357 177776  
513 003210 023727 177776 000357  
514 003216 001404

TST36: INC (R2) ;UPDATE TEST NUMBER  
CMP #36,(R2) ;SEQUENCE ERROR?  
BNE TST37-10 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #357,&PS ;MOVE ONES TO PSW  
CMP &PS,#357 ;SUCCESSFUL?  
BEQ TST37

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND <=====

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 770 <=====  
 003220 012742 000042 MOV #42,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 42 \*\*\*\*\*  
 003224 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 003226 000000 HALT :PSW NOT 357  
 : OR SEQUENCE ERROR

515 .SBTLL CONDITION CODE TEST  
 516  
 517 \*\*\*\*\*  
 518  
 519 : THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE Z-BIT.  
 520 : THE Z-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS  
 521 : BEQ AND BNE ARE TESTED FOR PROPER EXECUTION. THEN THE Z-BIT IS  
 522 : SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED  
 523 : AGAIN FOR PROPER OPERATION.  
 524 : THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION  
 525 : CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL  
 526 : BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR  
 527 : LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY  
 528 : USED IN THE TEST ARE VERIFIED HERE.  
 529  
 530 \*\*\*\*\*

:TEST 37 TEST BRANCHES AROUND Z-BIT

003230 005212 TST37: INC (R2) :UPDATE TEST NUMBER  
 003232 022712 000037 CMP #37,(R2) :SEQUENCE ERROR?  
 003236 001014 BNE TST40-10 :BR TO ERROR HALT ON SEQ ERROR  
 :FIRST WITH Z-BIT ON  
 531 003240 000257 CCC :CC=0100: JUST Z-BIT  
 532 003242 000264 SEZ :CHECK OPPOSITE CONDITION  
 533 003244 001001 BNE BRZ1 :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 534 003246 001404 BEQ BRZ2 :CONDITIONAL BRANCH INST. AND  
 :REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 773 <=====  
 : <=====  
 : <=====  
 : <=====  
 003250 012742 000043 BRZ1:  
 003250 012742 000043 MOV #43,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 43 \*\*\*\*\*  
 003254 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 003256 000000 HALT :IMPROPER BR W/ Z=1  
 :CHECK WITH Z-BIT OFF  
 536 003260 000277 BRZ2:  
 537 003262 000244 SCC :CC=1011: ALL BUT Z-BIT  
 538 003264 001401 CLZ  
 540 003266 001004 BEQ BRZ3  
 BNE TST40 :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 :CONDITIONAL BRANCH INST. AND  
 :REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 763 <=====  
 : <=====  
 : <=====  
 : <=====  
 003270 012742 000044 BRZ3:  
 003270 012742 000044 MOV #44,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 44 \*\*\*\*\*  
 003274 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 003276 000000 HALT :IMPROPER BR W/ Z=0  
 : OR SEQUENCE ERROR

541  
 542  
 543 \*\*\*\*\*

544                    THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE N-BIT.  
545                    THE N-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS  
546                    BMI AND BPL ARE TESTED FOR PROPER EXECUTION. THEN THE N-BIT IS  
547                    SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED  
548                    AGAIN FOR PROPER OPERATION.  
549                    THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION  
550                    CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL  
551                    BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR  
552                    LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY  
553                    USED IN THE TEST ARE VERIFIED HERE.  
554  
555

\*\*\*\*\*  
TEST 40            TEST BRANCHES AROUND N-BIT  
\*\*\*\*\*  
003300 005212      000040  
003302 022712  
003306 001014  
556  
557 003310 000257  
558 003312 000270  
559 003314 100001  
560 003316 100404  
TST40: INC        (R2)            ;UPDATE TEST NUMBER  
          CMP        #40, (R2)     ;SEQUENCE ERROR?  
          BNE        TST41-10     ;BR TO ERROR HALT ON SEQ ERROR  
          ;FIRST WITH N-BIT ON  
          CCC  
          SEN  
          BPL        BRN1        ;CHECK OPPOSITE CONDITION  
          BMI        BRN2  
          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
          ; CONDITIONAL BRANCH INST. AND        <=====  
          ; REPLACE THE MOVE INSTRUCTION     <=====  
          ; WHICH FOLLOWS W/ 773            <=====

003320 012742      000045  
003324 005242  
003326 000000  
561  
562 003330 000277  
563 003332 000250  
564 003334 100401  
565 003336 100004  
BRN1:  
          MOV        #45,-(R2)     ;MOVE TO MAILBOX # \*\*\*\*\* 45 \*\*\*\*\*  
          INC        -(R2)        ;SET MSGTYP TO FATAL ERROR  
          HALT  
          ;CHECK WITH N-BIT OFF  
BRN2:  
          SCC  
          CLN  
          BMI        BRN3        ;CHECK OPPOSITE CONDITION  
          BPL        TST41  
          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
          ; CONDITIONAL BRANCH INST. AND        <=====  
          ; REPLACE THE MOVE INSTRUCTION     <=====  
          ; WHICH FOLLOWS W/ 763            <=====

003340 012742      000046  
003344 005242  
003346 000000  
566  
567  
568  
569  
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571  
572  
573  
574  
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576  
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578  
BRN3:  
          MOV        #46,-(R2)     ;MOVE TO MAILBOX # \*\*\*\*\* 46 \*\*\*\*\*  
          INC        -(R2)        ;SET MSGTYP TO FATAL ERROR  
          HALT  
          ;OR SEQUENCE ERROR

\*\*\*\*\*  
THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE V-BIT.  
THE V-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS  
BVS AND BVC ARE TESTED FOR PROPER EXECUTION. THEN THE V-BIT IS  
SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED  
AGAIN FOR PROPER OPERATION.  
THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION  
CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL  
BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR  
LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY  
USED IN THE TEST ARE VERIFIED HERE.

579  
580003350 005212  
003352 022712 000041  
003356 001014  
581  
582 003360 000257  
583 003362 000262  
584 003364 102001  
585 003366 102404

```
;*****  
;TEST 41      TEST BRANCHES AROUND V-BIT  
;*****  
TST41: INC   (R2)      :UPDATE TEST NUMBER  
       CMP   #41,(R2)    :SEQUENCE ERROR?  
       BNE   TST42-10    :BR TO ERROR HALT ON SEQ ERROR  
;FIRST WITH V-BIT ON  
       CCC  
       SEV  
       BVC   BRV1        :CHECK OPPOSITE CONDITION  
       BVS   BRV2  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 773      <=====
```

003370 012742 000047  
003370 005242  
003374 000000  
586  
587 003400 000277  
588 003402 000242  
589 003404 102401  
590 003406 102004

```
BRV1:  
       MOV   #47,-(R2)  :MOVE TO MAILBOX # ***** 47 *****  
       INC   -(R2)  
       HALT  
;CHECK WITH V-BIT OFF  
       SCC  
       CLV  
       BVS   BRV3        :CHECK OPPOSITE CONDITION  
       BVC   TST42  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 773      <=====
```

003410 012742 000050  
003410 005242  
003414 000000  
003416

```
BRV3:  
       MOV   #50,-(R2)  :MOVE TO MAILBOX # ***** 50 *****  
       INC   -(R2)  
       HALT  
; OR SEQUENCE ERROR
```

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602  
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604  
605

```
;*****  
; THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE C-BIT.  
; THE C-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS  
; BCS AND BCC ARE TESTED FOR PROPER EXECUTION. THEN THE C-BIT IS  
; SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED  
; AGAIN FOR PROPER OPERATION.  
; THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION  
; CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL  
; BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR  
; LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY  
; USED IN THE TEST ARE VERIFIED HERE.
```

003420 005212  
003422 022712 000042  
003426 001014  
606  
607 003430 000257  
608 003432 000261

```
;*****  
;TEST 42      TEST BRANCHES AROUND C-BIT  
;*****  
TST42: INC   (R2)      :UPDATE TEST NUMBER  
       CMP   #42,(R2)    :SEQUENCE ERROR?  
       BNE   TST43-10    :BR TO ERROR HALT ON SEQ ERROR  
;FIRST WITH C-BIT ON  
       CCC  
       SEC  
;CC=0001: JUST C-BIT
```

609 003434 103001  
610 003436 103404BCC  
BCSBR<sub>C1</sub>  
BR<sub>C2</sub>

;CHECK OPPOSITE CONDITION

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 773 <=====003440  
003440 012742 000051  
003444 005242  
003446 000000  
611 003450 000277  
613 003452 000241  
614 003454 103401  
615 003456 100404BR<sub>C1</sub>:MOV #51,-(R2)  
INC -(R2)  
HALT;MOVE TO MAILBOX # \*\*\*\*\* 51 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;IMPROPER BR W/ C=1BR<sub>C2</sub>:SCC  
CLC  
BCS  
BMI

;CC=1110

BR<sub>C3</sub>  
TST43

;CHECK OPPOSITE CONDITION

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 763 <=====003460  
003460 012742 000052  
003464 005242  
003466 000000BR<sub>C3</sub>:MOV #52,-(R2)  
INC -(R2)  
HALT;MOVE TO MAILBOX # \*\*\*\*\* 52 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;IMPROPER BR W/ C=0  
; OR SEQUENCE ERROR

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\*\*\*\*\*  
SBTLL MICROCODE TESTSTHE MICROCODE TESTS ARE USED TO VERIFY THE MICROPROGRAMM  
FLOW. THE GOAL OF THESE TESTS IS TO EXERCISE EVERY POSSIBLE  
BRANCH IN THE MICROPROGRAM FLOW.THE TEST EXERCISES EVERY BRANCH IN THE MICROCODE BY  
TESTING AT LEAST ONE INSTRUCTION FROM EVERY CLASS OF INSTRUCTION IN  
ALL POSSIBLE MODES. FOR EXAMPLE, TO TEST THE SINGLE OPERAND INSTRUCTIONS,  
AT LEAST ONE SINGLE OPERAND INSTRUCTION IS VERIFIED IN ALL UNIQUE  
ADDRESSING MODES. BYTE MODES ARE ALSO TESTED. AS EACH NEW  
MODE IS INTRODUCED THE SAME INSTRUCTION IS TRIED AND TESTED IN  
A SMALL LOOP CONVENIENT FOR SCOPING. THE TEST IS SET UP USING  
ONLY INSTRUCTIONS AND ADDRESSING MODES WHICH HAVE BEEN PREVIOUSLY  
VERIFIED.IF THESE TESTS FAIL, CHECK THE RESULTS FOR A CLUE TO THE  
FAULT.\*\*\*\*\*  
THE CLR INSTRUCTION IS USED TO INTRODUCE EACH ADDRESSING  
MODE WITH THE SINGLE OPERAND INSTRUCTION. FOLLOWING THE SEQUENCE CHECK,  
THE CLR INSTRUCTION IS EXECUTED AND A BRANCH TEST IS EXECUTED WHICH  
CHECKS THAT THE Z-BIT WAS PROPERLY SET. THIS SMALL TEST IS SELF-SUFFICIENT  
AND CAN BE SCOPED TO TROUBLE SHOOT ALL OF THE IR DECODE LOGIC AND  
MICROCODE FOR SOP INSTRUCTIONS WITH MODE 0. FOLLOWING THIS TEST  
SEVERAL OTHER SOP INSTRUCTIONS ARE INTRODUCED WITH MODE 0. THESE  
INSTRUCTIONS MANIPULATE DATA AND SERVE TO CHECK THE DATA RESULTS

649  
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652:OF THE SOP INSTRUCTIONS IN THIS TEST. THE DATA IN THIS TEST IS  
:OPERATED ON BY EACH INSTRUCTION WITHOUT REINITIALIZING.003470 005212  
003472 022712 000043  
003476 001020  
653 003500 005000  
654 003502 001404:\*\*\*\*\*  
:TEST 43 TEST MODE 0 USING SOP INST.  
:\*\*\*\*\*

TST43:	INC (R2)	:UPDATE TEST NUMBER	<=====
	CMP #43,(R2)	:SEQUENCE ERROR?	<=====
	BNE TST44-10	:BR TO ERROR HALT ON SEQ ERROR	<=====
	CLR R0	:TRY THE CLEAR INST.	<=====
	BEQ SOPOA	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 775	<=====
003504 012742 000053	MOV #53,-(R2)	:MOVE TO MAILBOX # ***** 53 *****	<=====
003510 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
003512 000000	HALT	:CLR DID NOT SET Z-BIT	<=====
655 003514 005200	INC R0	:TRY THE INCREMENT INST.	<=====
656 003516 005100	COM R0	:TRY COMPLEMENT	<=====
657 003520 005200	INC R0	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 765	<=====
658 003522 100404	BMI SOPOB	:MOVE TO MAILBOX # ***** 54 *****	<=====
003524 012742 000054	MOV #54,-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
003530 005242	INC -(R2)	:NEGATE DID NOT SET N-BIT	<=====
003532 000000	HALT	:TRY COMPLEMENT INST.	<=====
659 003534 005100	COM R0	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 757	<=====
660 003536 001404	BEQ TST44	:MOVE TO MAILBOX # ***** 55 *****	<=====
003540 012742 000055	MOV #55,-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
003544 005242	INC -(R2)	:CUMMULATIVE RESULT OF CLR,INC,NEG AND COM INSTS. FAILED	<=====
003546 000000	HALT	: OR SEQUENCE ERROR	<=====

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672:\*\*\*\*\*  
: THIS TEST INTRODUCES THE REMAINING SOP INSTRUCIONS AND TESTS  
: THEM IN MODE 0. THE PURPOSE IS TO PROVIDE A BASELINE OF  
: INSTRUCTIONS FOR USE IN THE SUBSEQUENT TESTS. SINCE THE MICROCODE FOR  
: THESE INSTRUCTIONS IS IDENTICAL TO THAT ALREADY TESTED, ANY TROUBLE  
: SHOOTING EFFORTS SHOULD BE AIMED AT THE ACTUAL IR DECODE AND ALU  
: FUNCTIONING.:\*\*\*\*\*  
:TEST 44 TEST REMAINDER OF SOP INSTS IN MODE 0  
:\*\*\*\*\*003550 005212  
003552 022712 000044  
003556 001021  
673 003560 005000

TST44:	INC (R2)	:UPDATE TEST NUMBER	<=====
	CMP #44,(R2)	:SEQUENCE ERROR?	<=====
	BNE TST45-10	:BR TO ERROR HALT ON SEQ ERROR	<=====
	CLR R0	:INITIALIZE	<=====

674 003562 005300		DEC	R0	: TRY DECREMENT INST.	
675 003564 100404		BMI	SOPOC		
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 774	<=====
				; MOVE TO MAILBOX # ***** 56 *****	<=====
				; SET MSGTYP TO FATAL ERROR	<=====
				; N-BIT NOT SET ON DEC	<=====
003566 012742 000056		MOV	#56,-(R2)	; INITIALIZE CARRY	<=====
003572 005242		INC	-(R2)	; TRY ADD CARRY INST	<=====
003574 000000		HALT			
676 003576 000261		SOPOC:	SEC		
677 003600 005500		ADC	R0		
678 003602 001007		BNE	SOPOD		
679 003604 000261		SEC			
680 003606 005600		SBC	R0		
681 003610 100004		BPL	SOPOD		
682 003612 005100		COM	R0		
683 003614 005200		INC	R0		
684 003616 005300		DEC	R0		
685 003620 001404		BEQ	TST45		
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 756	<=====
003622					
003622 012742 000057		SOPOD:	MOV	#57,-(R2)	; MOVE TO MAILBOX # ***** 57 *****
003626 005242		INC	-(R2)	; SET MSGTYP TO FATAL ERROR	<=====
003630 000000		HALT		; CUMMULATIVE RESULT OF ADC,SBC,COM,INC AND DEC INSTS. FAILE	<=====
686				; OR SEQUENCE ERROR	
687					
688					
689					
690					
691					
692					
693					
				***** THIS TEST INTRODUCES THE BYTE CONTROL LOGIC OF THE PROCESSOR. THE MODE 0 BYTE MICROCODE IS TESTED. THE METHOD AND SEQUENCE OF TESTING IS THE SAME AS THAT USED IN THE SOP MODE 0 TESTS.	
				***** TEST 45 TEST MODE 0 EVEN BYTE USING SOP INST	
003632 005212		TST45:	INC	(R2)	; UPDATE TEST NUMBER
003634 022712	000045		CMP	#45,(R2)	; SEQUENCE ERROR?
003640 001012			BNE	TST46-10	; BR TO ERROR HALT ON SEQ ERROR
694 003642 105000			CLRB	R0	; TRY CLEARING EVEN BYTE OF REGISTER
695 003644 001404			BEQ	SOPBOA	
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 775	<=====
003646 012742 000060			MOV	#60,-(R2)	; MOVE TO MAILBOX # ***** 60 *****
003652 005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
003654 000000			HALT		; CLRB DID NOT SET Z-BIT
696 003656 105100		SOPBOA:	COMB	R0	; TRY SETTING EVEN BYTE OF REGISTER
697 003660 100002			BPL	SOPB0B	
698 003662 105200			INC&	R0	; TRY INCREMENTING EVEN BYTE OF REGISTER>>
699 003664 001404			BEQ	TST46	
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION	<=====

003666  
003666 012742 000061  
003672 005242  
003674 000000

## SOPB0B:

MOV #61,-(R2)  
INC -(R2)  
HALT

; WHICH FOLLOWS W/ 765  
; MOVE TO MAILBOX # \*\*\*\*\* 61 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; TEST CUMMULATIVE RESULT OF ABOVE BYTE INST.  
; OR SEQUENCE ERROR

700  
701  
702  
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709

\*\*\*\*\* THIS TEST USES THE CLR INSTRUCTION TO INTRODUCE AND TEST  
SINGLE OPERAND MODE 1 INSTRUCTIONS. AGAIN, THE CLR INSTRUCTION  
IS USED TO INTRODUCE THE MICROCODE AND TO TEST THAT THE PROPER  
CONDITION CODES ARE SET. OTHER SOP INSTRUCTIONS ARE USED TO MANIPULATE  
COMMON DATA TO VERIFY THAT THE CORRECT DATA IS PRODUCED.

003676 005212  
003700 022712 000046  
003704 001014  
710 003706 005000  
711 003710 005010  
712 003712 001404

TST46: INC (R2) ;UPDATE TEST NUMBER  
CMP #46,(R2) ;SEQUENCE ERROR?  
BNF TST47-10 ;BR TO ERROR HALT ON SEQ ERROR  
CLR R0 ;INITIALIZE R0  
CLR (R0) ;TRY CLEAR INST W/MODE 1  
BEQ SOP1A

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 774

003714 012742 000062  
003720 005242  
003722 000000  
713 003724 005310  
714 003726 100003  
715 003730 000261  
716 003732 005510  
717 003734 001404

SOP1A: MOV #62,-(R2)  
INC -(R2)  
HALT  
DEC (R0)  
BPL SOP1B  
SEC  
ADC (R0)  
BEQ TST47

; MOVE TO MAILBOX # \*\*\*\*\* 62 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; CLR DID NOT SET Z-BIT  
; TRY DECREMENT INST W/MODE 1  
; INITIALIZE CARRY  
; TRY ADD-CARRY W/MODE 1

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 763

003736 012742 000063  
003736 005242  
003742 000000

SOP1B: MOV #63,-(R2)  
INC -(R2)  
HALT

; MOVE TO MAILBOX # \*\*\*\*\* 63 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; TEST CUMMULATIVE RESULT OF ABOVE INST  
; OR SEQUENCE ERROR

718  
719  
720  
721  
722  
723  
724  
725  
726

\*\*\*\*\* THIS TEST VERIFIES THE BYTE INSTRUCTION MICROCODE FOR MODE 1  
SINGLE OPERAND INSTRUCTIONS.  
THIS IS THE FIRST PLACE THE SIGN EXTEND LOGIC IS EXERCISED  
AND VERIFIED.

003746 005212

TEST 47 TEST MODE 1 EVEN BYTE USING SOP INST  
TST47: INC (R2) ;UPDATE TEST NUMBER

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T47 TEST MODE 1 EVEN BYTE USING SOP INST

SEQ 0041

003750 022712 000047	CMP #47, (R2)	; SEQUENCE ERROR?	<=====
003754 0C1020	BNE TST50-10	; BR TO ERROR HALT ON SEQ ERROR	<=====
727 003756 005000	CLR R0	; INITIALIZE R0	<=====
728 003760 005010	CLR (R0)	; INITIALIZE LOC. 0	<=====
729 003762 005110	COM (R0)		
730 003764 105010	CLRB (R0)		
731 003766 001404	BEQ SOPB1A	; TRY TO CLEAR BYTE 0	
		; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 772	<=====
003770 012742 000064	MOV #64, -(R2)	; MOVE TO MAILBOX # ***** 64 *****	<=====
003774 005242	INC -(R2)	; SET MSGTYP TO FATAL ERROR	<=====
003776 000000	HALT	; CLRB DID NOT SET Z-BIT	<=====
732 004000 005210	SOPB1A: INC (R0)	; INCREMENT TO TEST WORD	<=====
733 004002 100005	BPL SOPB1B		
734 004004 105110	COMB (R0)	; COMPLEMENT: ODD BYTE = 376	
735 004006 105210	INC B (R0)	; INC: ODD BYTE = 377	
736 004010 100002	BPL SOPB1B		
737 004012 105210	INC B (R0)	; INCREMENT ODD BYTE=0	
738 004014 001404	BEQ TST50		
		; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 757	<=====
004016 012742 000065	SOPB1B: MOV #65, -(R2)	; MOVE TO MAILBOX # ***** 65 *****	<=====
004016 012742	INC -(R2)	; SET MSGTYP TO FATAL ERROR	<=====
004022 005242	HALT	; CHECK CUMMULATIVE RESULT OF ABOVE INST	<=====
004024 000000		; OR SEQUENCE ERROR	<=====
739		*****	
740		*****	
741		*****	
742		*****	
743		THIS TEST VERIFIES THAT SINGLE OPERAND BYTE INSTRUCTIONS WILL	
744		FUNCTION CORRECTLY FOR ODD BYTES.	
745		THIS IS THE FIRST TIME THAT ADDRESS LINE 0 HAS BEEN	
746		EXERCISED. CHECKS ARE MADE THAT THE PROPER BYTE IS MODIFIED AND	
747		THE CONDITION CODES ARE CHECKED. IT IS ALSO VERIFIED THAT THE UNADDRESSED	
748		BYTE IS NOT ALTERED BY THE INSTRUCTION.	
749		*****	
750		TEST 50 TEST MODE 1 ODD BYTE USING SOP INST	
004026 005212	TST50: INC (R2)	; UPDATE TEST NUMBER	<=====
004030 022712	CMP #50, (R2)	; SEQUENCE ERROR?	<=====
004034 001022	BNE TST51-10	; BR TO ERROR HALT ON SEQ ERROR	<=====
751 004036 005000	CLR R0	; INITIALIZE R0	<=====
752 004040 005010	CLR (R0)	; INITIALIZE LOC. 0	<=====
753 004042 005110	COM (R0)		
754 004044 005200	INC R0	; R0=ODD BYTE	
755 004046 105010	CLRB (R0)	; TRY TO CLEAR BYTE 1	
756 004050 001404	BEQ SOPB1C		
		; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 771	<=====

004052	012742	000066	MOV #66,-(R2)	;MOVE TO MAILBOX # ***** 66 *****
004056	005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
004060	000000		HALT	:CLRB DID NOT SET Z-BIT
757 004062	005300	SOPB1C:	DEC R0	:R0=WORD ADDR.
758 004064	005210		INC (R0)	;INCREMENT TO TEST WORD
759 004066	005200		INC R0	:R0=ODD BYTE
760 004070	105110		COMB (R0)	;TRY TO COMPLEMENT BYTE 1
761 004072	105210		INC B (R0)	
762 004074	100002		BPL SOPB1D	
763 004076	105210		INC B (R0)	;TRY TO INCREMENT BYTE 1
764 004100	001404		BEQ TST51	
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 755 <====<====<====<====<====				
004102	012742	000067	SOPB1D:	
004102	005242		MOV #67,-(R2)	;MOVE TO MAILBOX # ***** 67 *****
004106	000000		INC -(R2)	:SET MSGTYP TO FATAL ERROR
004110			HALT	:TEST CUMMULATIVE RESULT OF ABOVE INST. : OR SEQUENCE ERROR
765				
766				
767				
768				THIS TEST VERIFIES MODE 2 SINGLE-OPERAND INSTRUCTIONS. PREVIOUSLY
769				TESTED INSTRUCTIONS ARE USED TO SET A POINTER IN R0 TO LOC. 400.
770				LOC. 400 IS INITIALIZED TO -1 BEFORE A CLR MODE 2 IS EXECUTED.
771				THEN R0 IS DECREMENTED BY TWO TO AGAIN POINT TO 400 BEFORE EACH
772				OF SEVERAL MODE 2 INSTRUCTIONS ARE USED TO VERIFY THE DATA RESULTS OF
773				THE TEST. THIS PROCEDURE ALSO VERIFIES THE PROPER INCREMENTING OF THE
774				REGISTER.
775				
776				
***** TEST 51 TEST MODE 2 USING SOP INST. *****				
004112	005212	000051	TST51:	INC (R2) :UPDATE TEST NUMBER
004114	022712		CMP #51,(R2)	:SEQUENCE ERROR?
004120	001023		BNE TST52-10	:BR TO ERROR HALT ON SEQ ERROR
777 004122	005000		CLR R0	:SET R0=400
778 004124	105100		COMB R0	
779 004126	005200		INC R0	
780 004130	005C10		CLR (R0)	:CLEAR 400
781 004132	005110		COM (R0)	:INITIALIZE: 400=-1
782 004134	005020		CLR (R0)+	:TRY CLEARING WITH MODE 2
783 004136	001404		BEQ SOPZA	
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 770 <====<====<====<====<====				
004140	012742	000070	MOV #70,-(R2)	;MOVE TO MAILBOX # ***** 70 *****
004144	005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
004146	000000		HALT	:CLRB INST DID NOT SET Z-BIT
784 004150	005300	SOPZA:	DEC R0	:RESET R0
785 004152	005300		DEC R0	
786 004154	005120		COM (R0)+	;TRY COMPLEMENTING WITH MODE 2
787 004156	100004		BPL SOP2B	
788 004160	005300		DEC R0	
789 004162	005300		DEC R0	:RESET R0

CKKAAAO 11/44 CPU/EIS MACRO M1111 28-SEP-79 10:10 PAGE 3-22  
T51 TEST MODE 2 USING SOP INST.

SEQ 0043

790 004164 005220  
791 004166 001404

INC  
BEQ  
(R0)+  
TST52

:TRY INCREMENTING WITH MODE 2

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 754 <=====

004170  
004170 012742 000071  
004174 005242  
004176 000000

SOP2B:

MOV  
INC  
HALT  
#71,-(R2)  
(R2)

:MOVE TO MAILBOX # \*\*\*\*\* 71 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:CHECK CUMMULATIVE RESULT OF ABOVE INST  
: OR SEQUENCE ERROR

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THIS TEST VERIFIES MODE 2 SINGLE OPERAND INSTRUCTIONS WHICH  
ADDRESS EVEN BYTES. R0 IS SET TO 400 AND USED TO INITIALIZE LOCATION  
400 TO -1. CLR B INSTRUCTION IS THEN EXECUTED ON BYTE 400 WITH  
MODE 2.

R0 IS THEN DECREMENTED BEFORE EACH OF SEVERAL MODE 2 INSTRUCTIONS  
WHICH ARE USED TO VERIFY THE DATA RESULTS OF THE TEST. THIS PROCEDURE ALSO  
VERIFIES THE PROPER INCREMENTING OF THE REGISTER.

\*\*\*\*\* TEST 52 TEST MODE 2 EVEN BYTE USING SOP INST. \*\*\*\*\*

004200 005212  
004202 022712 000052  
004206 001023  
804 004210 005000  
805 004212 105100  
806 004214 005200  
807 004216 005010  
808 004220 005110  
809 004222 105020  
810 004224 001404

TST52: INC (R2)  
CMP #52,(R2)  
BNE TST53-10  
CLR R0  
COMB R0  
INC R0  
CLR (R0)  
COM (R0)  
CLRB (R0)+  
BEQ SOPB2A  
:UPDATE TEST NUMBER  
:SEQUENCE ERROR?  
:BR TO ERROR HALT ON SEQ ERROR  
:SET R0=400  
:CLEAR 400  
:INITIALIZE: 400=-1  
:TRY TO CLEAT 400 W/MODE 2

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 770 <=====

004226 012742 000072  
004232 005242  
004234 000000  
811 004236 005300  
812 004240 005210  
813 004242 105110  
814 004244 105220  
815 004246 100003  
816 004250 005300  
817 004252 105220  
818 004254 001404

MOV #72,-(R2)  
INC -(R2)  
HALT  
SOPB2A: DEC R0  
INC (R0)  
COMB (R0)  
INC B (R0)+  
BPL SOPB2B  
DEC R0  
INC B (R0)+  
BEQ TST53  
:MOVE TO MAILBOX # \*\*\*\*\* 72 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:CLR DID NOT SET Z-BIT  
:RESULT R0=400  
:INC 400 TO TEST WORD  
:TRY TO INC EVEN BYTE  
:RESET R0=400  
:TRY INCREMENT OF EVEN BYTE

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 754 <=====

004256 012742 000073  
004262 005242

SOPB2B:  
MOV #73,-(R2)  
INC -(R2)

:MOVE TO MAILBOX # \*\*\*\*\* 73 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR

004264 000000

HALT

;TEST CUMMULATIVE RESULT OF ABOVE INST.  
; OR SEQUENCE ERROR

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;\*\*\*\*\*  
; THIS TEST FOLLOWS THE SAME PROCEDURE DESCRIBED IN THE PREVIOUS  
; TEST. HERE, THE BYTE INSTRUCTION IS USED TO ADDRESS AN ODD BYTE.;\*\*\*\*\*  
;TEST 53 TEST MODE 2 ODD BYTE USING SOP INST.  
;\*\*\*\*\*004266 005212  
004270 022712 000053  
004274 001026  
826 004276 005000  
827 004300 105100  
828 004302 005200  
829 004304 005010  
830 004306 005110  
831 004310 005200  
832 004312 105020  
833 004314 001404TST53: INC (R2) ;UPDATE TEST NUMBER  
CMP #53, (R2) ;SEQUENCE ERROR?  
BNE TST54-10 ;BR TO ERROR HALT ON SEQ ERROR  
CLR R0 ;SET R0=400  
COMB R0  
INC R0  
CLR (R0) ;CLEAR LOC 400  
COM (R0) ;INITIALIZE: 400=-1  
INC R0 ;R0=ODD BYTE  
CLRB (R0)+ ;TRY TO CLEAR ODD BYTE  
BEQ SOPB2C; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 767  
;=====004316 012742 000074  
004322 005242  
004324 000000  
834 004326 005300  
835 004330 005300  
836 004332 005220MOV #74,-(R2)  
INC -(R2)  
HALT  
SOPB2C: DEC R0  
DEC R0  
INC (R0)+;MOVE TO MAILBOX # \*\*\*\*\* 74 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;CLRB DID NOT SET Z-BIT  
;R0=WORD ADDR.  
;INCREMENT WORD

838 004334	005300		DEC	R0	:POINT TO ODD BYTE	
839 004336	105110		COMB	(R0)	:COMPLEMENT ODD BYTE	
840 004340	105220		INC B	(R0)+	:TRY TO INCREMENT ODD BYTE	
841 004342	100003		BPL	SOPB2D		
842 004344	005300		DEC	R0	:RESET R0 TO ODD BYTE	
843 004346	105220		INC B	(R0)+	:TRY TO INCREMENT ODD BYTE	
844 004350	001404		BEQ	TST54		

					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
					: CONDITIONAL BRANCH INST. AND	<=====
					: REPLACE THE MOVE INSTRUCTION	<=====
					: WHICH FOLLOWS W/ 751	<=====

004352			SOPB2D:		MOV #75,-(R2)	:MOVE TO MAILBOX # ***** 75 *****
004352	012742	000075			INC -(R2)	:SET MSGTYP TO FATAL ERROR
004356	005242				HALT	:TEST CUMMULATIVE RESULT OF ABOVE INST.
004360	000000					: OR SEQUENCE ERROR

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:\*\*\*\*\* THESE TESTS CHECK THE NEGATE INSTRUCTION IN ALL MODES. PREVIOUSLY  
TESTED SINGLE-OPERAND INSTRUCTIONS ARE USED TO TEST THE NEGATE INSTRUCTION.

:\*\*\*\*\* TEST 54 TEST MODE 0 USING NEGATE INSTRUCTION

004362	005212	000054	TST54:	INC (R2)	:UPDATE TEST NUMBER	
004364	022712			CMP #54,(R2)	:SEQUENCE ERROR?	
004370	001035			BNE TST55-10	:BR TO ERROR HALT ON SEQ ERROR	
852 004372	005000			CLR R0	:SET R0=0	
853 004374	005200			INC R0	: R0=1	
854 004376	005400			NEG R0	:TRY NEGATE MODE 0: R0=-1	
855 004400	100003			BPL NEG00	:CC=1001?	
856 004402	001402			BEQ NEG00		
857 004404	102401			BVS NEG00		
858 004406	103404			BCS NEG01		

					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
					: CONDITIONAL BRANCH INST. AND	<=====
					: REPLACE THE MOVE INSTRUCTION	<=====
					: WHICH FOLLOWS W/ 770	<=====

004410			NEG00:		MOV #76,-(R2)	:MOVE TO MAILBOX # ***** 76 *****
004410	012742	000076			INC -(R2)	:SET MSGTYP TO FATAL ERROR
004414	005242				HALT	:NEGATE DID NOT SET CC'S CORRECTLY
004416	000000					

859			NEG01:	INC R0	:TEST DATA RESULT	
860 004420	005200			BEQ NEG02		
861 004422	001404					

					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
					: CONDITIONAL BRANCH INST. AND	<=====
					: REPLACE THE MOVE INSTRUCTION	<=====
					: WHICH FOLLOWS W/ 762	<=====

004424	012742	000077		MOV #77,-(R2)	:MOVE TO MAILBOX # ***** 77 *****
004430	005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR
004432	000000			HALT	:DATA RESULT OF NEGATE INCORRECT

862			NEG02:	COMB R0	:R0=377	
863 004434	105100			NEGB R0	:R0=1	
864 004436	105400			BMI NEG03	:CC=0001?	
865 004440	100403					

866 004442 001402  
 867 004444 102401  
 868 004446 103404

BEQ NEG03  
 BVS NEG03  
 BCS NEG04

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 750 <=====

004450 012742 000100  
 004450 005242  
 004454 000000  
 004456 000000  
 869 004460 005300  
 870 004462 001404

NEG03:  
 MOV #100,-(R2)  
 INC -(R2)  
 HALT  
 NEG04:  
 DEC R0  
 BEQ TST55

;MOVE TO MAILBOX # \*\*\*\*\* 100 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;NEGB DID NOT SET CC'S CORRECTLY  
 ;TEST DATA RESULT

004464 012742 000101  
 004470 005242  
 004472 000000

MOV #101,-(R2)  
 INC -(R2)  
 HALT

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 742 <=====

;MOVE TO MAILBOX # \*\*\*\*\* 101 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;DATA RESULT OF NEGB INCORRECT  
 ; OR SEQUENCE ERROR

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\*\*\*\*\*  
 :TEST 55 TEST MODE 1 USING NEGATE INST.  
 \*\*\*\*\*

004474 005212 000055  
 004476 022712  
 004502 001040  
 872 004504 005000  
 873 004506 005010  
 874 004510 005210  
 875 004512 005410  
 876 004514 100003  
 877 004516 001402  
 878 004520 102401  
 879 004522 103404

TST55:  
 INC (R2)  
 CMP #55,(R2)  
 BNE TST56-10  
 CLR R0  
 CLR (R0)  
 INC (R0)  
 NEG (R0)  
 BPL NEG10  
 BVS NEG10  
 BCS NEG11

;UPDATE TEST NUMBER  
 ;SEQUENCE ERROR?  
 ;BR TO ERROR HALT ON SEQ ERROR  
 ;POINT TO LOC. 0  
 ;CLEAR LOC. 0  
 ;LOC. 0=1  
 ;TRY NEG. LOC. 0=-1  
 ;CC=1001

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 767 <=====

004524 012742 000102  
 004524 005242  
 004530 000000  
 880 004532 000000  
 881 004534 005237  
 882 004540 001404

NEG10:  
 MOV #102,-(R2)  
 INC -(R2)  
 HALT

;MOVE TO MAILBOX # \*\*\*\*\* 102 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;NEGATE DID NOT SET CC'S CORRECTLY

NEG11:  
 INC @#0  
 BEQ NEG12

;TEST DATA RESULT

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 760 <=====

004542 012742 000103  
 004546 005242  
 004550 000000  
 883 004552 105110  
 884 004554 105410  
 885 004556 100403  
 886 004560 001402

NEG12:  
 MOV #103,-(R2)  
 INC -(R2)  
 HALT  
 COMB (R0)  
 NEGB (R0)  
 BMI NEG13  
 BEQ NEG13

;MOVE TO MAILBOX # \*\*\*\*\* 103 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;DATA RESULT OF NEGATE INCORRECT  
 ;LOC. 0=377  
 ;TRY NEGB LOC. 0=1  
 ;CC=0001?

887 004562 102401  
888 004564 103404BVS  
BCS  
NEG13  
NEG14; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 746 <=====004566  
004566 012742 000104  
004572 005242  
004574 000000  
889 004576 005337 000000  
890 004602 001404NEG13:  
MOV #104,-(R2)  
INC -(R2)  
HALT  
NEG14:  
DEC @#0  
BEQ TST56; MOVE TO MAILBOX # \*\*\*\*\* 104 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; NEGB DID NOT SET CC'S CORRECTLY  
; TEST DATA RESULT004604 012742 000105  
004610 005242  
004612 000000MOV #105,-(R2)  
INC -(R2)  
HALT; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 737 <=====

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\*\*\*\*\*  
:TEST 56 TEST MODE 2 USING NEGATE INSTRUCTION  
\*\*\*\*\*004614 005212  
004616 022712 000056  
004622 001032  
892 004624 005000  
893 004626 005010  
894 004630 005210  
895 004632 005420  
896 004634 100003  
897 004636 001402  
898 004640 102401  
899 004642 103404TST56:  
INC (R2)  
CMP #56, (R2)  
BNE TST57-10  
CLR R0  
CLR (R0)  
INC (R0)  
NEG (R0)+  
BPL NEG20  
BEQ NEG20  
BVS NEG20  
BCS NEG21; UPDATE TEST NUMBER  
; SEQUENCE ERROR?  
; BR TO ERROR HALT ON SEQ ERROR  
; POINT TO LOC. 0  
; CLEAR LOC. 0  
; LOC. 0=1  
; TRY NEG.: LOC. 0=-1  
; CC=1001?; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 767 <=====004644 012742 000106  
004644 005242  
004650 000000  
004652 000000  
900 004654 105300  
901 004656 105300  
902 004660 105420  
903 004662 105420  
904 004664 105340  
905 004666 005300  
906 004670 001404NEG20:  
MOV #106,-(R2)  
INC -(R2)  
HALT  
NEG21:  
DECB R0  
DECB R0  
NEGB (R0)+  
NEGB (R0)+  
DECB -(R0)  
DEC R0  
BEQ NEG22; MOVE TO MAILBOX # \*\*\*\*\* 106 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; NEGB DID NOT SET CC'S CORRECTLY  
; R0=LOC. 0  
; BYTE 0=1 R0=1  
; BYTE 1=1 R0=2  
; R0=1 LOC. 0=01  
; R0=0; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 754 <=====004672 012742 000107  
004676 005242  
004700 000000  
907 004702 005337 000000MOV #107,-(R2)  
INC -(R2)  
HALT  
NEG22:  
DEC @#0; MOVE TO MAILBOX # \*\*\*\*\* 107 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; REGISTER NOT INCREMENTED CORRECTLY  
; LOC. 0=0

908 004706 001404

BEQ TST57

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 745  
; MOVE TO MAILBOX # \*\*\*\*\* 110 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; NEG BYTE INSTRUCTIONS FAILED  
; OR SEQUENCE ERROR

004710 012742 000110  
004714 005242  
004716 000000

MOV #110,-(R2)  
INC -(R2)  
HALT

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;\*\*\*\*\*  
; THIS TEST VERIFIES MODE 3 SINGLE OPERAND INSTRUCTIONS. IT  
; USES LOCATION 0 AS ITS TARGET DATA. A TABLE LOCATED AT LOC. 400  
; THRU 402 IS USED TO SUPPLY THE ADDRESS OF LOCATION 0 TO THE  
; INSTRUCTIONS UNDER TEST.  
; R0 IS SET TO 400, THE START OF THE ADDRESS TABLE, AND A CLR  
; INSTRUCTION IS EXECUTED WITH MODE 3 TO CLEAR LOC. 0. THEN R0  
; IS DECREMENTED BY TWO AND TWO OTHER MODE 3 INSTRUCTIONS OPERATE ON  
; LOC. 0 TO VERIFY THE DATA RESULTS OF THE TEST. THE PROPER INCREMENTING  
; OF THE REGISTER IS ALSO VERIFIED IN THIS MANNER.  
; IF A FAILURE IS DETECTED BE SURE TO VERIFY THAT THE TABLE  
; (LOC. 400-402) HAS THE PROPER VALUES (0).  
;\*\*\*\*\*

;TEST 57 TEST MODE 3 USING SOP INST.

004720 005212  
004722 022712 000057  
004726 001020  
925 004730 005000  
926 004732 105100  
927 004734 005200  
928 004736 005010  
929 004740 005030  
930 004742 001404

TST57: INC (R2) ;UPDATE TEST NUMBER  
CMP #57, (R2) ;SEQUENCE ERROR?  
BNE TST60-10 ;BR TO ERROR HALT ON SEQ ERROR  
CLR R0 ;SET R0=400  
COMB R0  
INC R0  
CLR (R0) ;CLEAR LOC 400  
CLR @R0)+ ;TRY TO CLEAR LOC 0 USING MODE 3 ;R0=402  
BEQ SOP3A ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 771

004744 012742 000111  
004750 005242  
004752 000000  
931 004754 005300  
932 004756 005300  
933 004760 005130  
934 004762 100002  
935 004764 005230  
936 004766 001404

MOV #111,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 111 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;CLR DID NOT SET Z-BIT  
SOP3A: DEC R0 ;RESET R0=400  
DEC R0  
COM @R0)+ ;TRY TO COMPLEMENT LOC 0 OF MODE 3 ;R0=402  
BPL SOP3B  
INC @R0)+ ;TRY TO INCREMENT LOC 0 W/MODE 3 ;R0=404  
BEQ TST60 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 757

004770 012742 000112  
004774 005242  
004776 000000

SOP3B: MOV #112,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 112 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;CUMMULATIVE RESULT OF ABOVE INST FAILED

; OR SEQUENCE ERROR

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THIS TEST VERIFIES MODE 3 SINGLE OPERAND BYTE INSTRUCTIONS WHICH ADDRESS EVEN BYTES. AGAIN, THE TARGET LOCATION 0 IS USED AND THE SAME TABLE AT 400 IS EMPLOYED. AFTER POINTING R4 TO THE TABLE (400) AND SETTING LOCATION 0 TO -1, A CLRB INSTRUCTION IS USED TO CLEAR BYTE 0. SEVERAL OTHER MODE 3 INSTRUCTIONS ARE THEN USED WITH THE TABLE TO VERIFY THE DATA RESULTS AND THE PROPER INCREMENTING OF THE REGISTER. IF A FAILURE IS DETECTED, BE SURE THAT THE TABLE (LOCATION 400-402) HAS THE PROPER VALUES (0).

;TEST 60 TEST MODE 3 EVEN BYTE USING SOP INST.

005000	005212	
005002	022712	000060
005006	001026	
951 005010	005004	
952 005012	105104	
953 005014	005204	
954 005016	005000	
955 005020	005010	
956 005022	005110	
957 005024	105034	
958 005026	001404	

TST60:	INC	(R2)	:UPDATE TEST NUMBER
	CMP	#60, (R2)	:SEQUENCE ERROR?
	BNE	TST61-10	:BR TO ERROR HALT ON SEQ ERROR
	CLR	R4	:SET R4=400
	COMB	R4	
	INC	R4	
	CLR	R0	:INITIALIZE LOC. 0=-1
	CLR	(R0)	
	COM	(R0)	:LOC. 0=-1
	CLRB	@(R4)+	:TRY TO CLEAR EVEN BYTE ;LOC. 0=177400 R4=402
	BEQ	SOPB3A	
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
			CONDITIONAL BRANCH INST. AND <=====
			REPLACE THE MOVE INSTRUCTION <=====
			WHICH FOLLOWS W/ 767 <=====

005030	012742	000113
005034	005242	
005036	000000	
959 005040	005304	
960 005042	005304	
961 005044	005234	
962 005046	100006	
963 005050	105434	
964 005052	100004	
965 005054	005304	
966 005056	005304	
967 005060	105234	
968 005062	001404	

	MOV	#113,-(R2)	:MOVE TO MAILBOX # ***** 113 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:CLRB DID NOT SET Z-BIT
SOPB3A:	DEC	R4	:RESET POINTER R4=400
	DEC	R4	
	INC	@(R4)+	:TRY INCREMENTING WORD LOC.0=177401 R4=402
	BPL	SOPB3B	
	NEGB	@(R4)+	:TRY TO NEGATE EVEN BYTE ;LOC.0=-1 R4=404
	BPL	SOPB3B	
	DEC	R4	:R4=402
	DEC	R4	
	INCB	@(R4)+	:TRY TO INCREMENT EVEN BYTE ;LOC. 0=17400
	BEQ	TST61	
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
			CONDITIONAL BRANCH INST. AND <=====
			REPLACE THE MOVE INSTRUCTION <=====
			WHICH FOLLOWS W/ 751 <=====

005064	012742	000114
005064	005242	
005070	000000	
005072	000000	

SOPB3B:	MOV	#114,-(R2)	:MOVE TO MAILBOX # ***** 114 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:CUMMULATIVE RESULT OF ABOVE INST FAILED
			: OR SEQUENCE ERROR

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972 ; THIS TEST VERIFIES MODE 3 SINGLE OPERAND BYTE INSTRUCTIONS  
973 ; WHICH ADDRESS ODD BYTES. THE TARGET IS BYTE 1. A TABLE AT  
974 ; LOC. 400-406 IS USED. R0 SERVES AS THE TABLE POINTER.  
975 ; R0 IS INITIALIZED TO 400. LOC. 0 IS SET TO -1 USING THE  
976 ; FIRST TWO TABLE ENTRIES. A CLRB MODE 3 IS EXECUTED ON BYTE 1 USING  
977 ; TABLE ADDRESS AT 404. R0 IS DECREMENTED TO 402 AND SEVERAL SOP  
978 ; MODE 3 INSTRUCTIONS ARE USED TO VERIFY DATA RESULTS AND PROPER  
979 ; REGISTER INCREMENTING.  
980 ; THE TABLE (400-406) SHOULD CONTAIN 0,0,1,1 BEFORE AND  
981 ; AFTER THE TEST IS RUN.

			;TEST 61		TEST MODE 3 ODD BYTE USING SOP INST.	
			TST61: INC (R2)		;UPDATE TEST NUMBER	
			CMP #61, (R2)		;SEQUENCE ERROR?	
			BNE TST62-10		;BR TO ERROR HALT ON SEQ ERROR	
			CLR R0		;SET R0=400	
			COMB R0			
			INC R0			
			CLR @R0+		;INITIALIZE	
			COM @R0+		;LOC 0=-1 R0=404	
			CLRB @R0+		;TRY TO CLEAR ODD BYTE LOC. 0=377 R0=406	
			BEQ SOPB3C			
					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 770	
					<=====	
					<=====	
					<=====	
					<=====	
			MOV #115,-(R2)		;MOVE TO MAILBOX # ***** 115 *****	
			INC -(R2)		;SET MSGTYP TO FATAL ERROR	
			HALT		;CLRB DID NOT SET Z-BIT	
			SOPB3C: DEC R0		;RESET R0=402	
			DEC R0		;POINT TO EVEN BYTE ADDR.	
			DEC R0			
			DEC R0			
			INC @R0+		;INCREMENT WORD LOC. 0=400 R0=404	
			NEG B @R0+		;TRY TO NEGATE ODD BYTE LOC. 0=177400 R0=406	
			BPL SOPB3D			
			INC B @R0+		;TRY TO INCREMENT ODD BYTE LOC. 0=0 R0=410	
			BEQ TST62			
					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 753	
					<=====	
					<=====	
					<=====	
					<=====	
			SOPB3D: MOV #116,-(R2)		;MOVE TO MAILBOX # ***** 116 *****	
			INC -(R2)		;SET MSGTYP TO FATAL ERROR	
			HALT		;CUMMULATIVE RESULT OF ABOVE INSTS FAILED ; OR SEQUENCE ERROR	
			;TEST 62		TEST MODE 3 USING NEGATE INSTRUCTION	
			TST62: INC (R2)		;UPDATE TEST NUMBER	
			CMP #62, (R2)		;SEQUENCE ERROR?	
			BNE TST63-10		;BR TO ERROR HALT ON SEQ ERROR	
			CLR R0		;R0=400	
			COMB R0			

1003 005200	005200		INC	R0				
1004 005202	005010		CLR	(R0)	;LOC. 400=0			
1005 005204	005004		CLR	R4	;R4=0			
1006 005206	005014		CLR	(R4)	;LOC. 0=0			
1007 005210	005214		INC	(R4)	;LOC. 0=1			
1008 005212	005430		NEG	@(R0)+	;TRY NEGATE LOC. 0=-1 R0=402			
1009 005214	100003		BPL	NEG30	;CC=1001?			
1010 005216	001402		BEQ	NEG30				
1011 005220	102401		BVS	NEG30				
1012 005222	103404		BCS	NEG31				
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 763 <=====								
005224			NEG30:					
005224 012742	000117		MOV	#117,-(R2)	;MOVE TO MAILBOX # ***** 117 *****			
005230 005242			INC	-(R2)	;SET MSGTYP TO FATAL ERROR			
005232 000000			HALT		;NEG DID NOT SET CC'S CORRECTLY			
1013 005234 005214			INC	(R4)	;LOC. 0=0			
1014 005236 001404			BEQ	NEG32				
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 755 <=====								
005240 012742	000120		NEG32:					
005244 005242			MOV	#120,-(R2)	;MOVE TO MAILBOX # ***** 120 *****			
005246 000000			INC	-(R2)	;SET MSGTYP TO FATAL ERROR			
1015 005250 105137	000001		HALT		;DATA RESULT OF NEG INCORRECT			
1016 005254 005237	000000		COMB	@#1	;LOC 0=177400			
1017 005260 105430			INC	@#0	;LOC. 0=177401			
1018 005262 100404			NEGB	@(R0)+	;TRY NEGB LOC. 0=177777 R0=404			
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 743 <=====								
005264 012742	000121		NEG33:					
005270 005242			MOV	#121,-(R2)	;MOVE TO MAILBOX # ***** 121 *****			
005272 000000			INC	-(R2)	;SET MSGTYP TO FATAL ERROR			
1019 005274 105430			HALT		;NEGB FAILED WITH EVEN BYTE			
1020 005276 100004			NEGB	@(R0)+	;TRY NEGB LOC.0=777 R0=406			
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 735 <=====								
005300 012742	000122		NEG34:					
005304 005242			MOV	#122,-(R2)	;MOVE TO MAILBOX # ***** 122 *****			
005306 000000			INC	-(R2)	;SET MSGTYP TO FATAL ERROR			
1021 005310 105137	000001		HALT		;NEGB FAILED WITH ODD BYTE			
1022 005314 105237	000001		COMB	@#1	;LOC. 0=177377			
1023 005320 005214			INC	@#1	;LOC. 0=177777			
1024 005322 001404			INC	(R4)	;LOC. 0=0			
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 723 <=====								
005324 012742	000123		BEQ	TST63				
005330 005242			MOV	#123,-(R2)	;MOVE TO MAILBOX # ***** 123 *****			
;SET MSGTYP TO FATAL ERROR <=====								

005332 000000

HALT

;DATA RESULT OF NEGB'S INCORRECT  
; OR SEQUENCE ERROR1025  
1026  
1027  
1028  
1029  
1030  
1031  
1032  
1033  
1034

\*\*\*\*\*  
 THIS TEST VERIFIES MODE 4 SINGLE OPERAND INSTRUCTIONS.  
 R0 IS SET TO 400. A CLR INSTRUCTION IS EXECUTED IN MODE 4 TO CLEAR  
 LOC. 376. R0 IS RESET TO 400 AND A COM INSTRUCTION USING MODE 4  
 COMPLEMENTS LOC.376.  
 TWO INC INSTRUCTIONS AND A MODE 4 INSTRUCTION ARE EXECUTED  
 TO COMPLETE THE TEST.

;TEST 63 TEST MODE 4 USING SOP INSTS

005334	005212	
005336	022712	000063
005342	001021	
1035 005344	005000	
1036 005346	105100	
1037 005350	005200	
1038 005352	005040	
1039 005354	001404	

TST63:	INC	(R2)	:UPDATE TEST NUMBER
	CMP	#63,(R2)	:SEQUENCE ERROR?
	BNE	TST64-10	:BR TO ERROR HALT ON SEQ ERROR
	CLR	R0	:SET R0=400
	COMB	R0	
	INC	R0	
	CLR	-(R0)	:TRY TO CLEAR USING MODE 4
	BEQ	SOP4A	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND   
 REPLACE THE MOVE INSTRUCTION   
 WHICH FOLLOWS W/ 772   
 =====

005356	012742	000124
005362	005242	
005364	000000	
1040 005366	005200	
1041 005370	005200	
1042 005372	005140	
1043 005374	100004	
1044 005376	005200	
1045 005400	005200	
1046 005402	005240	
1047 005404	001404	

	MOV	#124,-(R2)	:MOVE TO MAILBOX # ***** 124 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:CLR DID NOT SET Z-BIT
SOP4A:	INC	R0	:RESET R0
	INC	R0	
	COM	-(R0)	:TRY TO COMPLEMENT USING MODE 4
	BPL	SOP4B	
	INC	R0	:MOVE POINTER
	INC	R0	
	INC	-(R0)	
	BEQ	TST64	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND   
 REPLACE THE MOVE INSTRUCTION   
 WHICH FOLLOWS W/ 756   
 =====

005406	012742	000125
005406	005242	
005412	000000	

SOP4A:	MOV	#125,-(R2)	:MOVE TO MAILBOX # ***** 125 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:CHECK CUMMULATIVE RESULT OF ABOVE INST.
			: OR SEQUENCE ERROR

1048  
1049  
1050  
1051  
1052  
1053  
1054  
1055  
1056  
1057  
1058

\*\*\*\*\*  
 THIS TEST VERIFIES MODE 5 SINGLE OPERAND INSTRUCTIONS. IT  
 USES LOCATION 0 AS ITS TARGET DATA. A TABLE LOCATED AT LOC. 372  
 THRU 374 IS USED TO SUPPLY THE ADDRESS OF LOCATION 0 TO THE  
 INSTRUCTIONS UNDER TEST.  
 R0 IS SET TO 376, (THE START OF THE ADDRESS TABLE) +2,  
 AND A CLR INSTRUCTION IS EXECUTED WITH MODE 3 TO CLEAR  
 LOC. 0. THEN R0 IS INCREMENTED BY TWO AND TWO OTHER MODE 3  
 INSTRUCTIONS OPERATE ON LOC. 0 TO VERIFY THE DATA RESULTS OF

T63 TEST MODE 4 USING SOP INSTS

SEQ 0053

1059 :THE TEST. THE PROPER DECREMENTING OF THE REGISTER IS ALSO  
 1060 :VERIFIED IN THIS MANNER.  
 1061 : IF A FAILURE IS DETECTED BE SURE TO VERIFY THAT THE TABLE  
 1062 :(LOC. 372 THRU 374) HAS THE PROPER VALUES (0).

1064 :\*\*\*\*\*  
 :TEST 64 TEST MODE 5 USING SOP INSTS  
 :\*\*\*\*\*

005416 005212	000064	TST64: INC (R2)	:UPDATE TEST NUMBER
005420 022712		CMP #64, (R2)	:SEQUENCE ERROR?
005424 001017		BNE TST65-10	:BR TO ERROR HALT ON SEQ ERROR
1065 005426 005000		CLR R0	:SET R0=376
1066 005430 005020		CLR (R0)+	
1067 005432 105400		NEGB R0	
1068 005434 005050		CLR @-(R0)	:TRY TO CLEAR LOC 0 W/MODE 5
1069 005436 001404		BEQ SOP5A	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 : CONDITIONAL BRANCH INST. AND <=====  
 : REPLACE THE MOVE INSTRUCTION <=====  
 : WHICH FOLLOWS W/ 772 <====

005440 012742 000126	SOP5A: MOV #126,-(R2)	:MOVE TO MAILBOX # ***** 126 *****
005444 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR
005446 000000	HALT	:CLR DID NOT SET Z-BIT
1070 005450 005200	INC R0	:RESET R0
1071 005452 005200	INC R0	
1072 005454 005150	COM @-(R0)	:TRY TO COMPLEMENT LOC. 0 W/MODE 5
1073 005456 100002	BPL SOP5B	
1074 005460 005250	INC @-(R0)	:TRY TO INCREMENT LOC. 0 W/MODE 5
1075 005462 001404	BEQ TST65	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 : CONDITIONAL BRANCH INST. AND <=====  
 : REPLACE THE MOVE INSTRUCTION <=====  
 : WHICH FOLLOWS W/ 760 <====

005464 012742 000127	SOP5B: MOV #127,-(R2)	:MOVE TO MAILBOX # ***** 127 *****
005464 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR
005470 000000	HALT	:TEST CUMMULATIVE RESULT OF ABOVE INSTS
		: OR SEQUENCE ERROR

1076 :\*\*\*\*\*  
 1077 :  
 1078 :  
 1079 : THIS TEST VERIFIES MODE 6 SINGLE OPERAND INSTRUCTIONS. IT  
 1080 :USES LOCATION 0 AS ITS TARGET DATA. R0 IS SET TO 400 USING  
 1081 :PREVIOUSLY TESTED INSTRUCTIONS AND A MODE 6 CLR INSTRUCTION IS  
 1082 :EXECUTED ON LOC. 0 USING R0 AND A -400 OFFSET. COM AND INC  
 1083 :INSTRUCTIONS ARE THEN USED TO VERIFY THE DATA.

1084 :\*\*\*\*\*  
 1085 :TEST 65 TEST MODE 6 USING SOP INSTS  
 :\*\*\*\*\*

005474 005212	000065	TST65: INC (R2)	:UPDATE TEST NUMBER
005476 022712		CMP #65, (R2)	:SEQUENCE ERROR?
005502 001020		BNE TST66-10	:BR TO ERROR HALT ON SEQ ERROR
1086 005504 005000		CLR R0	:SET R0=400
1087 005506 105100		COMB R0	
1088 005510 005200		INC R0	
1089 005512 005060	177400	CLR -400(R0)	:TRY TO CLEAR LOCATION 0 W/MODE 6

1090 005516 001404		BEQ	SOP6A	; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 771	<=====	
005520 012742 000130		MOV	#130,-(R2)	;MOVE TO MAILBOX # ***** 130 *****	<=====	
005524 005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	<=====	
005526 000000		HALT		;CLR DID NOT SET Z-BIT	<=====	
1091 005530 005160 177400		SOP6A:	COM	;TRY TO COMPLEMENT LOCATION 0 W/MODE 6		
1092 005534 100003		BPL	SOP6B			
1093 005536 005260 177400		INC	-400(R0)	;TRY TO INCREMENT LOCATION 0 W/MODE 6		
1094 005542 001404		BEQ	TST66			
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 757	<=====	
005544 012742 000131		SOP6B:	MOV	#131,-(R2)	;MOVE TO MAILBOX # ***** 131 *****	<=====
005544 005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	<=====	
005550 000000		HALT		;TEST CUMMULATIVE RESULT OF ABOVE INSTS	<=====	
				; OR SEQUENCE ERROR	<=====	
1095						
1096						
1097						
1098				THIS TEST VERIFIES MODE 7 SINGLE OPERAND INSTRUCTIONS. IT USES		
1099				THE POINTER TO LOC. 0 WHICH IS STORED AT LOC. 402.		
1100				RO IS SET TO 400 AND A MODE 7 CLR INSTRUCTION IS		
1101				EXECUTED WITH A +2 OFFSET TO CLEAR LOC. 0.		
1102				SEVERAL OTHER MODE 7 INSTRUCTIONS ARE THEN USED ON THE COMMON		
1103				LOCATION TO VERIFY THE DATA RESULTS.		
1104						
1105						
				TEST 66 TEST MODE 7 USING SOP INST.		
005554 005212 000066		TST66:	INC	(R2)	;UPDATE TEST NUMBER	<=====
005556 022712			CMP	#66,(R2)	;SEQUENCE ERROR?	<=====
005562 001021			BNE	TST67-10	;BR TO ERROR HALT ON SEQ ERROR	<=====
1106 005564 005000			CLR	RO	;SET RO=400	<=====
1107 005566 105100			COMB	RO		
1108 005570 005200			INC	RO		
1109 005572 005210			INC	(R0)	;R0=1	
1110 005574 005070 000002			CLR	a2(R0)	;TRY TO CLEAR LOC. 0 W/MODE 7	
1111 005600 001404			BEQ	SOP7A		
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 770	<=====	
005602 012742 000132		MOV	#132,-(R2)	;MOVE TO MAILBOX # ***** 132 *****	<=====	
005606 005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	<=====	
005610 000000		HALT		;CLR DID NOT SET Z-BIT	<=====	
1112 005612 005170 000002		SOP7A:	COM	;TRY TO COMPLEMENT LOC. 0 W/MODE 7		
1113 005616 100003		BPL	SOP7B			
1114 005620 005270 000002		INC	a2(R0)	;TRY TO INCREMENT LOC. 0 W/MODE 7		
1115 005624 001404		BEQ	TST67			
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION	<=====	

				; WHICH FOLLOWS W/ 756 <=====
005626	012742	000133	SOP7B:	MOV #133,-(R2) ;MOVE TO MAILBOX # ***** 133 *****
005626	005242			INC -(R2) ;SET MSGTYP TO FATAL ERROR
005632	000000			HALT ;TEST CUMMULATIVE RESULT OF ABOVE INSTS.
005634				; OR SEQUENCE ERROR
1116				
1117				
				;***** TEST 67 TEST MODE 4 WITH NEGATE INSTRUCTION *****
005636	005212	000067	TST67:	INC (R2) ;UPDATE TEST NUMBER
005640	022712			CMP #67,(R2) ;SEQUENCE ERROR?
005644	001024			BNE TST70-10 ;BR TO ERROR HALT ON SEQ ERROR
1118	005646	005000		CLR R0
1119	005650	005010		CLR (R0)
1120	005652	005120		COM (R0)+ ;LOC. 0=177777, R0=2
1121	005654	005440		NEG -(R0) ;TRY NEGATE, LOC. 0=1
1122	005656	100403		RMI NEG40 ;CC=0001?
1123	005660	001402		BEQ NEG40
1124	005662	102401		BVS NEG40
1125	005664	103404		BCS NEG41
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
				CONDITIONAL BRANCH INST. AND <=====
				REPLACE THE MOVE INSTRUCTION <=====
				WHICH FOLLOWS W/ 767 <=====
005666	012742	000134	NEG40:	MOV #134,-(R2) ;MOVE TO MAILBOX # ***** 134 *****
005666	005242			INC -(R2) ;SET MSGTYP TO FATAL ERROR
005672	000000			HALT ;NEG DID NOT SET CC'S CORRECTLY
1126	005676	005400	NEG41:	NEG R0 ;TST R0 WITH A NEG.
1127	005700	001404		BEQ NEG42
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
				CONDITIONAL BRANCH INST. AND <=====
				REPLACE THE MOVE INSTRUCTION <=====
				WHICH FOLLOWS W/ 761 <=====
005702	012742	000135	NEG42:	MOV #135,-(R2) ;MOVE TO MAILBOX # ***** 135 *****
005706	005242			INC -(R2) ;SET MSGTYP TO FATAL ERROR
005710	000000			HALT ;R0 NOT DECREMENTED PROPERLY
1128	005712	005310		DEC (R0) ;TEST DTA RESULT OF NEG
1129	005714	001404		BEQ TST70
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
				CONDITIONAL BRANCH INST. AND <=====
				REPLACE THE MOVE INSTRUCTION <=====
				WHICH FOLLOWS W/ 753 <=====
005716	012742	000136	MOV	#136,-(R2) ;MOVE TO MAILBOX # ***** 136 *****
005722	005242		INC	-(R2) ;SET MSGTYP TO FATAL ERROR
005724	0000C0		HALT	
				; DATA RESULT OF NEG INCORRECT <=====
				; OR SEQUENCE ERROR <=====
1130				;***** TEST 70 TEST MODE 5 WITH NEGATE INSTRUCTION *****
005726	005212	000070	TST70:	INC (R2) ;UPDATE TEST NUMBER
005730	022712			CMP #70,(R2) ;SEQUENCE ERROR?
005734	001031			BNE TST71-10 ;BR TO ERROR HALT ON SEQ ERROR
1131	005736	005000		CLR R0 ;R0=0
1132	005740	005010		CLR (R0) ;LOC. 0=0
1133	005742	105100		COMB R0 ;R0=377

1134 005744 005200		INC R0	:R0=400	
1135 005746 005010		CLR (R0)	:SET 400 = 0	
1136 005750 005004		CLR R4	:R4=0	
1137 005752 005314		DEC (R4)	:LOC. 0=177777	
1138 005754 005450		NEG @-(R0)	:TRY NEGATE: LOC. 0=1	
1139 005756 100403		BMI NEG50	:CC=0001?	
1140 005760 001402		BEQ NEG50		
1141 005762 102401		BVS NEG50		
1142 005764 103404		BCS NEG51		
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 763 <=====				
005766 012742 000137	NEG50:	MOV #137,-(R2)	:MOVE TO MAILBOX # ***** 137 *****	
005772 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR	
005774 000000		HALT	:NEG DID NOT SET CC'S CORRECTLY	
1143 005776 005314	NEG51:	DEC (R4)		
1144 006000 001404		BEQ NEG52		
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 755 <=====				
006002 012742 000140		MOV #140,-(R2)	:MOVE TO MAILBOX # ***** 140 *****	
006006 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR	
006010 000000		HALT	:DATA RESULT OF NEG INCORRECT	
1145 006012 105100	NEG52:	COMB R0		
1146 006014 005300		DEC R0		
1147 006016 001404		BEQ TST71		
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 746 <=====				
006020 012742 000141		MOV #141,-(R2)	:MOVE TO MAILBOX # ***** 141 *****	
006024 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR	
006026 000000		HALT	:REGISTER NOT DECREMENTED PROPERLY : OR SEQUENCE ERROR	
1148	***** TEST MODE 6 WITH NEGATE *****			
006030 005212	TST71:	INC (R2)	:UPDATE TEST NUMBER	
006032 022712 000071		CMP #71,(R2)	:SEQUENCE ERROR?	
006036 001022		BNE TST72-10	:BR TO ERROR HALT ON SEQ ERROR	
1149 006040 005000		CLR R0	:R0=0	
1150 006042 005004		CLR R4	:R4=0	
1151 006044 105100		COMB R0	:R0=377	
1152 006046 005014		CLR (R4)	:LOC. 0=0	
1153 006050 105024		CLRB (R4)+	:LOC. 0=177777, R4=1	
1154 006052 105114		COMB (R4)	:LOC. 0=177400	
1155 006054 005460 177401		NEG -377(R0)	:LOC. 0=400	
1156 006060 100403		BMI NEG60	:CC=0001	
1157 006062 001402		BEQ NEG60		
1158 006064 102401		BVS NEG60		
1159 006066 103404		BCS NEG61		
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION <=====				

006070			NEG60:		: WHICH FOLLOWS W/ 763 <=====
006070	012742	000142		MOV #142,-(R2)	: MOVE TO MAILBOX # ***** 142 *****
006074	005242			INC -(R2)	: SET MSGTYP TO FATAL ERROR
006076	000000			HALT	: NEG DID NOT SET CC'S CORRECTLY
1160	006100	105314	NEG61:	DEC B (R4)	
1161	006102	001404		BEQ TST72	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 755 <=====
006104	012742	000143		MOV #143,-(R2)	: MOVE TO MAILBOX # ***** 143 ***** <=====
006110	005242			INC -(R2)	: SET MSGTYP TO FATAL ERROR <=====
006112	000000			HALT	: DATA RESULT OF NEG INCORRECT <=====
1162					: OR SEQUENCE ERROR *****
					: TEST 72 TEST MODE 7 W/ NEGATE *****
006114	005212		TST72:	INC (R2)	: UPDATE TEST NUMBER <=====
006116	022712	000072		CMP #72,(R2)	: SEQUENCE ERROR? <=====
006122	001024			BNE TST73-10	: BR TO ERROR HALT ON SEQ ERROR <=====
1163	006124	005000		CLR R0	: R0=0 <=====
1164	006126	005010		CLR (R0)	: LOC. 0=0 <=====
1165	006130	005110		COM (R0)	: LOC. 0=177777 <=====
1166	006132	105100		COMB R0	: R0=377 <=====
1167	006134	105470	000005	NEGB @5(R0)	: R0+5=404, 404=1, LOC. 0=777 <=====
1168	006140	100403		BMI NEG70	: CC=0001? <=====
1169	006142	001402		BEQ NEG70	
1170	006144	102401		BVS NEG70	
1171	006146	103404		BCS NEG71	
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 765 <=====
006150			NEG70:		
006150	012742	000144		MOV #144,-(R2)	: MOVE TO MAILBOX # ***** 144 ***** <=====
006154	005242			INC -(R2)	: SET MSGTYP TO FATAL ERROR <=====
006156	000000			HALT	: NEG DID NOT SET CC'S CORRECTLY <=====
1172	006160	105100	NEG71:	COMB R0	: R0=0 <=====
1173	006162	105120		COMB (R0)+	: LOC. 0=400, R0=1 <=====
1174	006164	105310		DEC B (R0)	: LOC. 0=0 <=====
1175	006166	005467	171606	NEG 0	: USE NEG MODE 67 TO TST FOR ZERO <=====
1176	006172	001404		BEQ TST73	
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 753 <=====
006174	012742	000145		MOV #145,-(R2)	: MOVE TO MAILBOX # ***** 145 ***** <=====
006200	005242			INC -(R2)	: SET MSGTYP TO FATAL ERROR <=====
006202	000000			HALT	: DATA RESULT OF NEG WAS INCORRECT <=====
1177					: OR SEQUENCE ERROR *****
1178					
1179					
1180					
1181					
1182					
					: THIS TEST VERIFIES PROGRAM COUNTER ADDRESSING WITH SOP INSTRUCTIONS. CLR MODE 77 IS USED TO CLEAR THE LOCATION FOLLOWING THE INSTRUCTION (SOPX). THEN SINGLE OPERAND INSTRUCTIONS WITH MODES 37, 67, AND

1183  
1184  
1185  
1186:77, USING INDIRECT POINTER SOPXAD ARE USED TO VERIFY THE DATA RESULTS  
OF THESE INSTRUCTIONS.006204 005212  
006206 022712 000073  
006212 001017  
1187 006214 005027  
1188 006216 177777  
1189 006220 001404

:TEST 73 TEST SOP OPCODE MODES 2,3,6,7 WITH P.C.

TST73: INC (R2) :UPDATE TEST NUMBER  
CMP #73,(R2) :SEQUENCE ERROR?  
BNE SOPB :BR TO ERROR HALT ON SEQ ERROR  
CLR (R7)+ :CLEAR NEXT LOCATION: (SOPX)  
SOPX: -1 :USE MODE 27BEQ SOPA : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
: CONDITIONAL BRANCH INST. AND <=====  
: REPLACE THE MOVE INSTRUCTION <=====  
: WHICH FOLLOWS W/ 774 <=====  
: MOVE TO MAILBOX # \*\*\*\*\* 146 \*\*\*\*\*006222 012742 000146  
006226 005242  
006230 000000  
1190 006232 005237 006216  
1191 006236 005467 177754  
1192 006242 100003  
1193 006244 005277 000012  
1194 006250 001405MOV #146,-(R2) :SET MSGTYP TO FATAL ERROR  
INC -(R2) :CLR DID NOT SET Z-BIT  
HALT :INC SOPX W/MODE 37  
SOPA: INC @#SOPX :NEGATE SOPX W/MODE 67  
NEG SOPX :INC SOPX W/MODE 77  
BPL SOPB  
INC @SOPXAD  
BEQ TST74: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
: CONDITIONAL BRANCH INST. AND <=====  
: REPLACE THE MOVE INSTRUCTION <=====  
: WHICH FOLLOWS W/ 760 <=====  
: MOVE TO MAILBOX # \*\*\*\*\* 146 \*\*\*\*\*006252 012742 000147  
006256 005242  
006260 000000SOPB: MOV #147,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 147 \*\*\*\*\*  
INC -(R2) :SET MSGTYP TO FATAL ERROR  
HALT :INC DID NOT SET Z-BIT  
: OR SEQUENCE ERROR  
SOPXAD: SOPX :INDIRECT ADDRESS OF SOPX

1195 006262 006216

: THIS TEST VERIFIES SINGLE OPERAND NON-MODIFYING INSTRUCTIONS  
: USING MODE 0. R0 IS SET TO ZERO AND THE CONDITION CODES ARE SET  
: TO THE COMPLEMENT OF THAT EXPECTED BY THE INSTRUCTION. A TST INSTRUCTION  
: IS EXECUTED AND CONDITIONAL BRANCHES ARE USED TO TEST THE CONDITION  
: CODES.1196  
1197  
1198  
1199  
1200  
1201  
1202  
1203  
1204  
1205

:TEST 74 TEST MODE 0 SOP NON-MODIFYING

006264 005212  
006266 022712 000074  
006272 001010  
1206 006274 005000  
1207 006276 000277  
1208 006300 000244  
1209 006302 005700  
1210 006304 102403  
1211 006306 100402  
1212 006310 103401  
1213 006312 001404TST74: INC (R2) :UPDATE TEST NUMBER  
CMP #74,(R2) :SEQUENCE ERROR?  
BNE TST75-10 :BR TO ERROR HALT ON SEQ ERROR  
CLR R0 :INITIALIZE R0=0  
SCC :SET CC=1011  
CLZ :TRY TST W/ MODE 0  
TST R0 :CHECK THAT CC=0100  
BVS SNMOA  
BMI SNMOA  
BCS SNMOA  
BEQ TST75

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 767 <=====

006314 012742 000150  
006314 005242 000000  
006320 005242 000000  
006322 000000

SNMOA:

MOV	#150,-(R2)	;MOVE TO MAILBOX # ***** 150 *****
INC	-(R2)	;SET MSGTYP TO FATAL ERROR
HALT		;CONDITION CODES NOT SET PROPERLY
		; OR SEQUENCE ERROR

1214  
1215  
1216  
1217  
1218  
1219  
1220  
1221  
1222  
1223

;\*\*\*\*\*  
; THIS TEST VERIFIES SINGLE OPERAND NON-MODIFYING BYTE INSTRUCTIONS WITH MODE 0.  
; R0 IS SET TO 377 AND COMPLEMENT OF THE EXPECTED CONDITION CODES  
; IS LOADED IN PSW. A TSTB INSTRUCTION IS EXECUTED AND THE RESULTS  
; ARE CHECKED WITH SEVERAL CONDITIONAL BRANCH INSTRUCTIONS.  
; THIS VERIFIES THAT THE PROPER BYTE WAS TESTED.  
;\*\*\*\*\*

;TEST 75 TEST MODE 0 EVEN BYTE W/ SOP NON-MODIFYING

006324 005212 000075  
006326 022712 000075  
006332 001010 000000  
1224 006334 005000 000000  
1225 006336 105100 000000  
1226 006340 000277 000000  
1227 006342 000250 000000  
1228 006344 105700 000000  
1229 006346 102402 000000  
1230 006350 101401 000000  
1231 006352 100404 000000

TST75:	INC	(R2)	;UPDATE TEST NUMBER
	CMP	#75,(R2)	;SEQUENCE ERROR?
	BNE	TST76-10	;BR TO ERROR HALT ON SEQ ERROR
	CLR	R0	;INITIALIZE
	COMB	R0	;R0=377
	SCC		;SET CC=0111
	CLN		
	TSTB	R0	;TRY TST EVEN BYTE
	BVS	SNMBOA	;CHECK CC=1000
	BLOS	SNMBOA	
	BMI	TST76	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 767 <=====

006354 012742 000151  
006354 005242 000000  
006360 005242 000000  
006362 000000

SNMBOA:

MOV	#151,-(R2)	;MOVE TO MAILBOX # ***** 151 *****
INC	-(R2)	;SET MSGTYP TO FATAL ERROR
HALT		;CONDITION CODES NOT SET PROPERLY
		; OR SEQUENCE ERROR

1232  
1233  
1234  
1235  
1236  
1237  
1238  
1239  
1240  
1241

;\*\*\*\*\*  
; THIS TEST VERIFIES SINGLE OPERAND INSTRUCTIONS WITH MODE 1.  
; R0 IS USED TO POINT TO AND CLEAR LOC. 0. THE COMPLEMENT OF THE  
; EXPECTED CONDITION CODES ARE LOADED IN THE PSW. A TST INSTRUCTION  
; IS THEN EXECUTED ON LOC. 0 USING R0 AND CONDITIONAL BRANCHES TEST  
; THE RESULTS.  
;\*\*\*\*\*

;TEST 76 TEST MODE 1 SOP NON-MODIFYING

006364 005212 000076  
006366 022712 000076  
006372 001011 000000  
1242 006374 005000

IST76:	INC	(R2)	;UPDATE TEST NUMBER
	CMP	#76,(R2)	;SEQUENCE ERROR?
	BNE	TST77-10	;BR TO ERROR HALT ON SEQ ERROR
	CLR	R0	;POINT TO LOC 0

1243 006376 005010		CLR (R0)	:CLEAR LOC 0	
1244 006400 000277		SCC	:INITIALIZE	
1245 006402 000244		CLZ	:CC=1011	
1246 006404 005710		TST (R0)	:TRY TST W/ MODE 1	
1247 006406 102403		BVS SNM1A	:CHECK CC=0100	
1248 006410 103402		BCS SNM1A		
1249 006412 100401		BMJ SNM1A		
1250 006414 001404		BEQ TST77		
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 766	<=====

006416 012742 000152		SNM1A:	MOV #152,-(R2)	:MOVE TO MAILBOX # ***** 152 *****
006416 005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR
006424 000000			HALT	:CC'S NOT SET PROPERLY : OR SEQUENCE ERROR

1251				
1252				
1253				
1254				: THIS TEST SETS LOCATION 0 TO 377 AND THEN USES R0 TO TEST
1255				: THE EVEN BYTE AND THE ODD BYTE USING SOP BYTE INSTRUCTIONS WITH MODE 1.
1256				: AGAIN, CONDITIONAL BRANCHES ARE USED TO VERIFY THE SETTING OF THE
1257				: PROPER CONDITION CODE BITS.
1258				
1259				

			:TEST 77 TEST MODE 1 BYTE INST. NON-MODIFYING	
006426 005212		TST77: INC (R2)	:UPDATE TEST NUMBER	
006430 022712	000077	CMP #77,(R2)	:SEQUENCE ERROR?	
006434 001026		BNE TST100-10	:BR TO ERROR HALT ON SEQ ERROR	
1260 006436 005000		CLR R0	:POINT TO LOC 0	
1261 006440 005010		CLR (R0)	:CLEAR LOC 0	
1262 006442 105110		COMB (R0)	:COMPLEMENT BYTE 0	
1263 006444 000277		SCC	:SET CC=0111	
1264 006446 000250		CLN		
1265 006450 105710		TSTB (R0)	:TRY TST ON EVEN BYTE	
1266 006452 102402		BVS SNMB1A		
1267 006454 101401		BLOS SNMB1A		
1268 006456 100404		BMI SNMB1B		
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 766	<=====

006460 012742 000153		SNMB1A:	MOV #153,-(R2)	:MOVE TO MAILBOX # ***** 153 *****
006464 005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR
006466 000000			HALT	:CC'S NOT CORRECT
1269 006470 005000		SNMB1B: CLR R0		
1270 006472 005200		INC R0		
1271 006474 000277		SCC	:SET CC=1011	
1272 006476 000244		CLZ		
1273 006500 105710		TSTB (R0)	:TRY TO TST AN ODD BYTE	
1274 006502 102403		BVS SNMB1C	:CHECK CC=0100	
1275 006504 103402		BCS SNMB1C		
1276 006506 100401		BMJ SNMB1C		
1277 006510 001404		BEQ TST100		

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 751 <=====

006512 012742 000154  
006512 005242 000000  
006516 005242 000000  
006520 000000

SNMB1C:

MOV #154,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 154 \*\*\*\*\*  
INC -(R2) :SET MSGTYP TO FATAL ERROR  
HALT :CC'S NOT CORRECT  
: OR SEQUENCE ERROR

1278  
1279  
1280  
1281  
1282  
1283  
1284  
1285  
1286

;\*\*\*\*\* THIS TEST VERIFIES THE SINGLE-OPERAND NON-MODIFYING INSTRUCTIONS  
:USING MODE 2. IT USES THE IDENTICAL PROCEDURE EMPLOYED IN THE  
:MODE 1 TESTS. ADDITIONALLY, THE REGISTER IS CHECKED TO ASSURE THAT  
:IT IS INCREMENTED PROPERLY.

;TEST 100 TEST MODE 2 WITH SOP NON-MODIFYING

006522 005212 000100  
006524 022712 000100  
006530 001020 000100  
1287 006532 005000 000100  
1288 006534 005010 000100  
1289 006536 000277 000100  
1290 006540 000244 000100  
1291 006542 005720 000100  
1292 006544 102403 000100  
1293 006546 103402 000100  
1294 006550 100401 000100  
1295 006552 001404 000100

TST100: INC (R2) :UPDATE TEST NUMBER  
CMP #100,(R2) :SEQUENCE ERROR?  
BNE TST101-10 :BR TO ERROR HALT ON SEQ ERROR  
CLR R0 :INITIALIZE R0=0  
CLR (R0) :CLEAR LOC 0  
SCC :SET CC=1011  
CLZ  
TST (R0)+ :TRY TST W/ MODE 2  
BVS SNM2A :CHECK CC=0100  
BCS SNM2A  
BMI SNM2A  
BEQ SNM2B

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 766 <=====

006554 012742 000155  
006554 005242 000000  
006560 005242 000000  
006562 000000 000000  
1296 006564 005300 000000  
1297 006566 005300 000000  
1298 006570 001404 000000

SNM2A:

MOV #155,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 155 \*\*\*\*\*  
INC -(R2) :SET MSGTYP TO FATAL ERROR  
HALT :CC'S NOT CORRECT

SNM2B: DEC R0 :RESET R0  
DEC R0  
BEQ TST101

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 757 <=====

006572 012742 000156  
006576 005242 000000  
006600 000000

MOV #156,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 156 \*\*\*\*\*  
INC -(R2) :SET MSGTYP TO FATAL ERROR  
HALT :MODE 2 DID NOT INC REQ CORRECTLY  
: OR SEQUENCE ERROR

1299  
1300  
1301  
1302  
1303  
1304

;\*\*\*\*\* THIS TEST VERIFIES MODE 2 SINGLE OPERAND NON-MODIFYING BYTE  
:INSTRUCTIONS IT USES R0 TO POINT TO LOC. 0. WITH LOCATION 0  
:SET TO 377, THE EVEN AND ODD BYTE IS TESTED WITH TSTB INSTRUCTIONS

1305  
1306  
1307  
1308;TO VERIFY THE CORRECT CC ARE SET. THE REGISTER IS CHECKED FOR  
;PROPER INCREMENTING.

006602	005212	
006604	022712	000101
006610	001042	
1309 006612	005000	
1310 006614	005010	
1311 006616	105110	
1312 006620	000277	
1313 006622	000250	
1314 006624	105720	
1315 006626	102402	
1316 006630	101401	
1317 006632	100404	

;TEST 101 TEST MODE 2 - BYTE W/ SOP NON-MODIFYING

TST101: INC	(R2)	UPDATE TEST NUMBER
CMP	#101, (R2)	:SEQUENCE ERROR?
BNE	TST102-10	:BR TO ERROR HALT ON SEQ ERROR
CLR	R0	:CLEAR R0
CLR	(R0)	:CLEAR LOC 0
COMB	(R0)	:SET LOC 0=377
SCC		:SET CC=0111
CLN		
TSTB	(R0)+	;TRY TST OF EVEN BYTE
BVS	SNMB2A	
BLOS	SNMB2A	
BMI	SNMB2B	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 766

006634	012742	000157
006634	005242	
006640	000000	
1318 006644	005300	
1319 006646	001404	

SNMB2A:	MOV	#157,-(R2)	;MOVE TO MAILBOX # ***** 157 *****
	INC	-(R2)	;SET MSGTYP TO FATAL ERROR
	HALT		;CC'S NOT SET CORRECTLY
SNMB2B:	DEC	R0	;DECREMENT R0
	BEQ	SNMB2C	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 760

006650	012742	000160
006654	005242	
006656	000000	
1320 006660	005200	
1321 006662	000277	
1322 006664	000244	
1323 006666	105720	
1324 006670	102403	
1325 006672	103402	
1326 006674	100401	
1327 006676	001404	

SNMB2C:	MOV	#160,-(R2)	;MOVE TO MAILBOX # ***** 160 *****
	INC	-(R2)	;SET MSGTYP TO FATAL ERROR
	HALT		;MODE 2 DID NOT INC REG CORRECTLY
	INC	R0	;POINT TO ODD BYTE
	SCC		;SET CC=1011
	CLZ		
	TSTB	(R0)+	;TRY TST OF ODD BYTE
	BVS	SNMB2D	;CHECK CC'S=0100
	BCS	SNMB2D	
	BMI	SNMB2D	
	BEQ	SNMB2E	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 744

006700	012742	000161
006700	005242	
006704	000000	
1328 006710	005300	
1329 006712	005300	
1330 006714	001404	

SNMB2D:	MOV	#161,-(R2)	;MOVE TO MAILBOX # ***** 161 *****
	INC	-(R2)	;SET MSGTYP TO FATAL ERROR
	HALT		;CC'S NOT CORRECT
SNMB2E:	DEC	R0	
	DEC	R0	
	BEQ	TST102	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION

006716 012742 000162  
006722 005242  
006724 000000MOV #162,-(R2)  
INC -(R2)  
HALTWHICH FOLLOWS W/ 735  
;MOVE TO MAILBOX # \*\*\*\*\* 162 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;R0 DID NOT INCREMENT PROPERLY  
; OR SEQUENCE ERROR

&lt;====

1331  
1332  
1333  
1334  
1335  
1336  
1337  
1338  
1339\*\*\*\*\* THIS TEST VERIFIES MODE 3 SINGLE OPERAND NON-MODIFYING INSTRUCTIONS.  
A POINTER IN A TABLE AT LOC. 376 IS USED TO TEST LOCATION 0.  
THE CC'S AND THE REGISTER ARE CHECKED FOLLOWING THE  
TST MODE 3 INSTRUCTION.

\*\*\*\*\* TEST 102 TEST MODE 3 W/ SOP NON-MODIFYING INSTS \*\*\*\*\*

006726 005212  
006730 022712 000102  
006734 001022  
1340 006736 005000  
1341 006740 005010  
1342 006742 105100  
1343 006744 005300  
1344 006746 000277  
1345 006750 000244  
1346 006752 005730  
1347 006754 102403  
1348 006756 103402  
1349 006760 100401  
1350 006762 001404TST102: INC (R2) ;UPDATE TEST NUMBER  
CMP #102,(R2) ;SEQUENCE ERROR?  
BNE TST103-10 ;BR TO ERROR HALT ON SEQ ERROR  
CLR R0 ;R0=0  
CLR (R0) ;CLEAR LOC 0  
COMB R0 ;R0=376  
DEC R0 ;  
SCC ;SET CC=1011  
CLZ ;  
TST @R0+ ;TRY TST W/ MODE 3  
BVS SNM3A ;CHECK CC=0100  
BCS SNM3A  
BMI SNM3A  
BEQ SNM3B; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 764<====  
<====  
<====  
<====006764 012742 000163  
006766 005242  
006770 000000  
1351 006774 005300  
1352 006776 105100  
1353 007000 001404SNM3A:  
MOV #163,-(R2)  
INC -(R2)  
HALT;MOVE TO MAILBOX # \*\*\*\*\* 163 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;CC'S NOT CORRECTSNM3B:  
DEC R0 ;R0=377  
COMB R0 ;R0=0  
BEQ TST103; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 755<====  
<====  
<====  
<====007002 012742 000164  
007006 005242  
007010 000000MOV #164,-(R2)  
INC -(R2)  
HALT;MOVE TO MAILBOX # \*\*\*\*\* 164 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;MODE 3 DID NOT INC REG CORRECTLY  
; OR SEQUENCE ERROR1354  
1355  
1356  
1357  
1358  
1359  
1360  
1361\*\*\*\*\* THIS TEST VERIFIES SOP NON-MODIFYING BYTE INSTRUCTIONS MODE 3  
LOC. 0 IS SET TO 377. TABLE AT LOC. 402-404 IS USED TO TEST  
BYTE 0 AND BYTE 1. THE REGISTER IS CHECKED FOR PROPER INCREMENTING AND  
THE CC'S ARE VERIFIED.  
THE TABLE AT LOC. 402-404 SHOULD CONTAIN 0 AND 1 BEFORE AND

1362  
1363  
1364

:AFTER THE TEST IS RUN.

:TEST 103 TEST MODE 3 - BYTES W/ SOP NON-MODIFYING INSTS.

007012	005212	
007014	022712	000103
007020	001036	
1365	007022	005000
1366	007024	005010
1367	007026	105110
1368	007030	105100
1369	007032	005200
1370	007034	005720
1371	007036	000277
1372	007040	000250
1373	007042	105730
1374	007044	102402
1375	007046	101401
1376	007050	100404

TST103:	INC	(R2)	:UPDATE TEST NUMBER
	CMP	#103, (R2)	:SEQUENCE ERROR?
	BNE	TST104-10	:BR TO ERROR HALT ON SEQ ERROR
	CLR	R0	:R0=0
	CLR	(R0)	:CLEAR LOC 0
	COMB	(R0)	:LOC. 0 =377
	COMB	R0	
	INC	R0	
	TST	(R0)+	:R0=402
	SCC		:CC=0111
	CLN		
	TSTB	@(R0)+	:TRY TST OF EVEN BYTE
	BVS	SNMB3A	:CHECK CC=1000
	BLOS	SNMB3A	
	BMI	SNMB3B	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND   
REPLACE THE MOVE INSTRUCTION   
WHICH FOLLOWS W/ 763   
=====

007052		
007052	012742	000165
007056	005242	
007060	000000	
1377	007062	000277
1378	007064	000244
1379	007066	105730
1380	007070	102403
1381	007072	103402
1382	007074	100401
1383	007076	001404

SNMB3A:	MOV	#165,-(R2)	:MOVE TO MAILBOX # ***** 165 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:CC'S NOT CORRECT
	SNMB3B:	SCC	:SET CC=1011
	CLZ		
	TSTB	@(R0)+	:TRY TST OF ODD BYTE
	BVS	SNMB3C	:CHECK CC=0100
	BCS	SNMB3C	
	BMI	SNMB3C	
	BEQ	SNMB3D	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND   
REPLACE THE MOVE INSTRUCTION   
WHICH FOLLOWS W/ 750   
=====

007100		
007100	012742	000166
007104	005242	
007106	000000	
1384	007110	005720
1385	007112	005710
1386	007114	100404

SNMB3C:	MOV	#166,-(R2)	:MOVE TO MAILBOX # ***** 166 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:CC'S NOT CORRECT
	SNMB3D:	TST	:R0=410
		(R0)+	
		(R0)	
		TST104	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND   
REPLACE THE MOVE INSTRUCTION   
WHICH FOLLOWS W/ 741   
=====

007116	012742	000167
007122	005242	
007124	000000	

MOV	#167,-(R2)	:MOVE TO MAILBOX # ***** 167 *****
INC	-(R2)	:SET MSGTYP TO FATAL ERROR
HALT		:TSTB DID NOT INCREMENT R0 CORRECTLY
		: OR SEQUENCE ERROR

1387  
1388  
1389

;	*****	*****
;	THIS TEST VERIFIES MODE 4 SOP NON-MODIFYING INSTRUCTIONS.	

1390 :LOC. 0 IS SET TO -1 AND THE CC'S ARE SET TO THE COMPLEMENT OF THE  
 1391 :EXPECTED RESULTS. R0 AND SET TO 2 AND A TST MODE 4 IS EXECUTED.  
 1392 :THE CC'S ARE CHECKED WITH CONDITIONAL BRANCH INSTRUCTIONS AND THE REGISTER  
 1393 :IS CHECKED FOR PROPER DECREMENTING.  
 1394  
 1395

\*\*\*\*\* TEST 104 TEST MODE 4 W/ SOP NON-MODIFYING INSTS \*\*\*\*\*

007126 005212	007130 022712	007134 001017	000104	TST104: INC (R2) ;UPDATE TEST NUMBER CMP #104, (R2) ;SEQUENCE ERROR? BNE TST105-10 ;BR TO ERROR HALT ON SEQ ERROR CLR R0 ;R0=0 CLR (R0) ;LOC 0=0 COM (R0)+ ;LOC 0=-1 SCC ;SET CC=1011 CLZ TST -(R0) ;TRY TST W/ MODE 4 BVS SNM4A ;CHECK CC=0100 BLOS SNM4A BMI SNM4B
1396 007136 005000	1397 007140 005010	1398 007142 005120		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND <===== : REPLACE THE MOVE INSTRUCTION <===== : WHICH FOLLOWS W/ 766 <=====
1399 007144 000277	1400 007146 000244	1401 007150 005740		
1402 007152 102402	1403 007154 101401	1404 007156 100404		
007160 012742 000170	007164 005242	007166 000000		SNM4A: MOV #170,-(R2) ;MOVE TO MAILBOX # ***** 170 ***** INC -(R2) ;SET MSGTYP TO FATAL ERROR HALT ;CC'S NOT CORRECT
1405 007170 005700	1406 007172 001404			SNM4B: TST R0 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS BEQ TST105 ;CONDITIONAL BRANCH INST. AND <===== : REPLACE THE MOVE INSTRUCTION <===== : WHICH FOLLOWS W/ 760 <=====
007174 012742 000171	007200 005242	007202 000000		MOV #171,-(R2) ;MOVE TO MAILBOX # ***** 171 ***** INC -(R2) ;SET MSGTYP TO FATAL ERROR HALT ;TST MODE 4 DID NOT DEC R0 CORRECTLY ; OR SEQUENCE ERROR

1407  
1408  
1409  
1410  
1411  
1412  
1413  
1414  
1415

\*\*\*\*\* THIS TEST VERIFIES MODE 5 SOP NON-MODIFYING INSTRUCTIONS.  
IT USES A POINTER AT LOC. 376 TO TEST LOC. 0. R0 IS SET  
TO 400, A TST MODE 5 INSTRUCTION IS EXECUTED AND THE CC'S CHECKED.  
R0 IS CHECKED TO INSURE PROPER DECREMENTING. \*\*\*\*\*

\*\*\*\*\* TEST 105 TEST MODE 5 W/ SOP NON-MODIFYING INSTS \*\*\*\*\*

007204 005212	007206 022712	007212 001022	000105	TST105: INC (R2) ;UPDATE TEST NUMBER CMP #105, (R2) ;SEQUENCE ERROR? BNE TST106-10 ;BR TO ERROR HALT ON SEQ ERROR CLR R0 ;R0=0 CLR (R0) ;LOC 0=0 COM (R0) ;LOC 0=-1 COMB R0 ;R0=377 INC R0 ;R0=400
1416 007214 005000	1417 007216 005010	1418 007220 005110		
1419 007222 105100	1420 007224 005200			

1421 007226 000277 SCC :SET CC=0111  
 1422 007230 000250 CLN  
 1423 007232 005750 TST @-(R0) :TRY TST W/ MODE 5  
 1424 007234 102402 BVS SNM5A :CHECK CC=1000  
 1425 007236 101401 BLOS SNM5A  
 1426 007240 100404 BMI SNM5B  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 764 <=====  
 ; =====  
 ; =====  
 ; =====  
 ; =====  
 007242 012742 000172 SNM5A:  
 007246 005242 000000 INC #172,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 172 \*\*\*\*\*  
 007250 000000 HALT -(R2) :SET MSGTYP TO FATAL ERROR  
 1427 007252 005200 INC CC'S NOT SET PROPERLY  
 1428 007254 105100 COMB R0 :R0=377  
 1429 007256 001404 BEQ RO :R0=0  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 755 <=====  
 ; =====  
 ; =====  
 ; =====  
 007260 012742 000173 MOV #173,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 173 \*\*\*\*\*  
 007264 005242 000000 INC :SET MSGTYP TO FATAL ERROR  
 007266 000000 HALT :MODE 5 DID NOT DEC R0 CORRECTLY  
 ; OR SEQUENCE ERROR  
 1430  
 1431  
 1432  
 1433 :\*\*\*\*\* THIS TEST VERIFIES MODE 6 SOP NON-MODIFYING INSTRUCTIONS.  
 1434 :RO IS SET TO 377 AND A MODE 6 TST INSTRUCTION IS EXECUTED  
 1435 :USING RO AND AN OFFSET OF -377. THE CC'S ARE CHECKED AS WELL  
 1436 :AS R0 TO INSURE IT WAS NOT ALTERED.  
 1437  
 1438 :\*\*\*\*\* TEST 106 TEST MODE 6 W/ SOP NON-MODIFYING INSTS :\*\*\*\*\*  
 007270 005212 000106 TST106: INC (R2) :UPDATE TEST NUMBER  
 007272 022712 000106 CMP #106,(R2) :SEQUENCE ERROR?  
 007276 001021 BNE TST107-10 :BR TO ERROR HALT ON SEQ ERROR  
 1439 007300 005000 CLR R0 :R0=0  
 1440 007302 005010 CLR (R0) :LOC 0=0  
 1441 007304 005110 COM (R0) :LOC 0=-1  
 1442 007306 105100 COMB R0 :R0=377  
 1443 007310 000277 SCC :SET CC=0111  
 1444 007312 000250 CLN  
 1445 007314 005760 177401 TST -377(R0) :TRY TST W/ MODE 6  
 1446 007320 102402 BVS SNM6A :CHECK CC=1000  
 1447 007322 101401 BLOS SNM6A  
 1448 007324 100404 BMI SNM6B  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 764 <=====  
 ; =====  
 ; =====  
 ; =====  
 007326 012742 000174 SNM6A:  
 007326 005242 000000 MOV #174,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 174 \*\*\*\*\*  
 007332 005242 000000 INC :SET MSGTYP TO FATAL ERROR  
 007334 000000 HALT :CC'S INCORRECT

1449 007336 105100  
1450 007340 001404SNM6B: COMB R0  
BEQ TST107

;R0=0

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 756  
;=====

007342 012742 000175  
007346 005242  
007350 000000

MOV #175,-(R2)  
INC -(R2)  
HALT

;MOVE TO MAILBOX # \*\*\*\*\* 175 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;TST MODE 6 INCORRECTLY CHANGED R0  
; OR SEQUENCE ERROR

1451  
1452  
1453  
1454  
1455  
1456  
1457  
1458  
1459

;\*\*\*\*\*  
;  
; THIS TEST VERIFIES MODE 7 SOP NON-MODIFYING INSTRUCTIONS.  
; IT USES A POINTER TO LOC. 0 STORED AT LOC. 400 TO TST LOC. 0.  
; R0 IS SET TO 377 AND LOC. 0 IS TESTED THRU THE POINTER AT 400 USING  
; R0 AND AN OFFSET OF 1.

;\*\*\*\*\*  
;TEST 107 TEST MODE 7 W/ SOP NON-MODIFYING INSTS.  
;\*\*\*\*\*

007352 005212  
007354 022712 000107  
007360 001021  
1460 007362 005000  
1461 007364 005010  
1462 007366 005110  
1463 007370 105100  
1464 007372 000277  
1465 007374 000250  
1466 007376 005770 000001  
1467 007402 102402  
1468 007404 101401  
1469 007406 100404

TST107: INC (R2) ;UPDATE TEST NUMBER  
CMP #107,(R2) ;SEQUENCE ERROR?  
BNE TST110-10 ;BR TO ERROR HALT ON SEQ ERROR  
CLR R0 ;R0=0  
CLR (R0) ;LOC 0=0  
COM (R0) ;LOC 0=-1  
COMB R0 ;R0=377  
CLN ;CC=0111  
TST @1(R0) ;TRY TST W/ MODE 7  
BVS SNM7A ;CHECK CC=1000  
BLOS SNM7A  
BMI SNM7B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 764  
;=====

007410 012742 000176  
007414 005242  
007416 000000  
1470 007420 105100  
1471 007422 001404

SNM7A:  
MOV #176,-(R2)  
INC -(R2)  
HALT

SNM7B: COMB R0  
BEQ TST110

;MOVE TO MAILBOX # \*\*\*\*\* 176 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;CC'S NOT CORRECT  
;R0=0

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 756  
;=====

007424 012742 000177  
007430 005242  
007432 000000

MOV #177,-(R2)  
INC -(R2)  
HALT

;MOVE TO MAILBOX # \*\*\*\*\* 177 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;TST MODE 7 INCORRECTLY CHANGED R0  
; OR SEQUENCE ERROR

1472  
1473  
1474  
1475  
1476

;\*\*\*\*\*  
;  
; THIS TEST VERIFIES MODE 0 DOUBLE OPERAND INSTRUCTIONS. IT SETS  
; DATA IN R0 AND R4 AND USES THE ADD INSTRUCTION TO TEST THE DOP

1477  
1478  
1479

;MICROCODE.

007434	005212	
007436	022712	000110
007442	001006	
1480	007444	005000
1481	007446	005100
1482	007450	005004
1483	007452	060004
1484	007454	005204
1485	007456	001404

;TEST 110 TEST MODE 0 DOUBLE-OPERAND (DOP) INSTS.  
;\*\*\*\*\*  
;IST110: INC (R2) ;UPDATE TEST NUMBER  
; CMP #110, (R2) ;SEQUENCE ERROR?  
; BNE TST111-10 ;BR TO ERROR HALT ON SEQ ERROR  
; CLR R0 ;R0=0  
; COM R0 ;R0=-1  
; CLR R4 ;R4=0  
; ADD R0,R4 ;TRY ADD: R4=-1  
; INC R4 ;R4=0  
; BEQ TST111 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; ; CONDITIONAL BRANCH INST. AND <=====  
; ; REPLACE THE MOVE INSTRUCTION <=====  
; ; WHICH FOLLOWS W/ 771 <=====  
; ; MOVE TO MAILBOX # \*\*\*\*\* 200 \*\*\*\*\*  
; ; SET MSGTYP TO FATAL ERROR  
; ; ADD INST. FAILED W/ MODE 0  
; ; OR SEQUENCE ERROR

007460	012742	000200
007464	005242	
007466	000000	

MOV #200,-(R2)  
INC -(R2)  
HALT

;MOVE TO MAILBOX # \*\*\*\*\* 200 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;ADD INST. FAILED W/ MODE 0  
;OR SEQUENCE ERROR

1486  
1487  
1488  
1489  
1490  
1491  
1492

;\*\*\*\*\*  
; THIS TEST VERIFIES THE MOVE INSTRUCTION WITH MODE 0 TO MODE 0.  
; THIS TEST IS NECESSARY BECAUSE THIS PARTICULAR INSTRUCTION UTILIZES UNIQUE  
;MICROCODE.  
;

1494

```

;***** TEST 111      MOV MODE 0 TO MODE 0 *****
;***** TST111: INC (R2)          :UPDATE TEST NUMBER *****
;*****          CMP #111, (R2)       :SEQUENCE ERROR? *****
;*****          BNE TST112-10      :BR TO ERROR HALT ON SEQ ERROR *****
;*****          CLR R0            :R0=0 *****
;*****          CLR R4            :R4=0 *****
;*****          COM R0            :R0=-1 *****
;*****          MOV R0,R4          :TRY MOVE -1 TO R4 *****
;*****          INC R4            :INC R4 *****
;*****          BEQ TST112         :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;*****                                CONDITIONAL BRANCH INST. AND
;*****                                REPLACE THE MOVE INSTRUCTION
;*****                                WHICH FOLLOWS W/ 771      <=====

007470 005212 000111
007472 022712
1495 007500 005000
1496 007502 005004
1497 007504 005100
1498 007506 010004
1499 007510 005204
1500 007512 001404

007514 012742 000201
007520 005242
007522 000000

1501
1502
1503
1504
1505
1506
1507
1508

;***** THIS TEST VERIFIES THE SUBTRACT INSTRUCTION WITH MODE 0,0.
;***** THIS TEST IS NECESSARY BECAUSE THIS PARTICULAR INSTRUCTION UTILIZES SOME
;***** UNIQUE MICROCODE.

;***** TEST 112      TEST SUB MODE 0,0 *****
;***** TST112: INC (R2)          :UPDATE TEST NUMBER *****
;*****          CMP #112, (R2)       :SEQUENCE ERROR? *****
;*****          BNE TST113-10      :BR TO ERROR HALT ON SEQ ERROR *****
;*****          CLR R0            :R0=0 *****
;*****          CLR R4            :R4=0 *****
;*****          INC R4            :R4=1 *****
;*****          SUB R4,R0          :TRY SUB 0,0    R0=-1
;*****          BPL SUB0           :CC=1001 *****
;*****          BEQ SUB0           :
;*****          BVS SUB0           :
;*****          BCS SUB0A          :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;*****                                CONDITIONAL BRANCH INST. AND
;*****                                REPLACE THE MOVE INSTRUCTION
;*****                                WHICH FOLLOWS W/ 767      <=====

007524 005212 000112
007526 022712
007532 001016
1509 007534 005000
1510 007536 005004
1511 007540 005204
1512 007542 160400
1513 007544 100003
1514 007546 001402
1515 007550 102401
1516 007552 103404

007554 012742 000202
007554 005242
007560 000000
007562 000000
1517 007564 005200
1518 007566 001404

007570 012742 000203
007574 005242

SUB0:          MOV #202,-(R2)      :MOVE TO MAILBOX # ***** 202 *****
              INC -(R2)           :SET MSGTYP TO FATAL ERROR
              HALT                :CONDITION CODE FAILED ON SUB

SUB0A:         INC R0             :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
              BEQ TST113          :CONDITIONAL BRANCH INST. AND
                                      REPLACE THE MOVE INSTRUCTION
                                      WHICH FOLLOWS W/ 761      <=====

MOV #203,-(R2)      :MOVE TO MAILBOX # ***** 203 *****
INC -(R2)           :SET MSGTYP TO FATAL ERROR

```

007576 000000

HALT

;DATA RESULT OF SUB FAILED  
; OR SEQUENCE ERROR1519  
1520  
1521  
1522  
1523  
1524  
1525  
1526  
1527  
1528

\*\*\*\*\*  
 THIS TEST QUICKLY VERIFIES THE REMAINING DOP MODIFYING INSTRUCTIONS  
 WITH MODE 0,0 TO PROVIDE A BASELINE FOR SUBSEQUENT TESTS.  
 SINGLE OPERAND INSTRUCTIONS ARE USED TO SET UP DATA IN R0 AND R4  
 BEFORE EACH OF THE SEVERAL DOP MODIFYING INSTRUCTIONS ARE USED AND  
 VERIFIED.

\*\*\*\*\*  
 TEST 113 TEST ALL THE DOP INSTRUCTIONS W/ SOURCE MODE 0,0  
 \*\*\*\*\*

007600	005212	
007602	022712	000113
007606	001051	
1529 007610	005000	
1530 007612	010004	
1531 007614	001404	

TST113:	INC	(R2)	:UPDATE TEST NUMBER
	CMP	#113, (R2)	:SEQUENCE ERROR?
	BNE	TST114-10	:BR TO ERROR HALT ON SEQ ERROR
	CLR	R0	:R0=0
	MOV	R0,R4	:TRY MOVE MODE 0,0
	BEQ	DOP0A	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 774 <=====

007616	012742	000204
007622	005242	
007624	000000	
1532 007626	005200	
1533 007630	005100	
1534 007632	005104	
1535 007634	040004	
1536 007636	005304	
1537 007640	001404	

	MOV	#204,-(R2)	:MOVE TO MAILBOX # ***** 204 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:Z-BIT NOT SET
DOP0A:	INC	R0	:R0=1
	COM	R0	:R0=177776
	COM	R4	:R4=177777
	BIC	R0,R4	:TRY BIC: R4=1
	DEC	R4	:R4=0
	BEQ	DOP0B	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 762 <=====

007642	012742	000205
007646	005242	
007650	000000	
1538 007652	050004	
1539 007654	005204	
1540 007656	005204	
1541 007660	001404	

	MOV	#205,-(R2)	:MOVE TO MAILBOX # ***** 205 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:BIC CLEAR RESULT INCORRECT
DOP0B:	BIS	R0,R4	:TRY BIS: R4=177777
	INC	R4	
	INC	R4	:R4=0
	BEQ	DOP0C	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 752 <=====

007662	012742	000206
007666	005242	
007670	000000	
1542 007672	005000	
1543 007674	105100	
1544 007676	005004	
1545 007700	005104	
1546 007702	040004	
1547 007704	060004	

	MOV	#206,-(R2)	:MOVE TO MAILBOX # ***** 206 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:RESULT OF BIS INCORRECT
DOP0C:	CLR	R0	:R0=0
	COMB	R0	:R0=377
	CLR	R4	:R4=0
	COM	R4	:R4=177777
	BIC	R0,R4	:R4=177400
	ADD	R0,R4	:TRY ADD: R4=177777

1548 007706 005204		INC BEQ	R4 DOPOD	;R4=0  ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 736 ;=====
1549 007710 001404				
007712 012742 000207		MOV	#207,-(R2)	MOVE TO MAILBOX # ***** 207 *****
007716 005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR
007720 000000		HALT		;RESULT OF ADD INCORRECT
1550 007722 160004		DOPOD:	SUB R0,R4	;177401=R4
1551 007724 105404			NEGB R4	;R4=177777
1552 007726 005204			INC R4	;RD=0
1553 007730 001404			BEQ TST114	 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 726 ;=====
007732 012742 000210		MOV	#210,-(R2)	MOVE TO MAILBOX # ***** 210 *****
007736 005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR
007740 000000		HALT		;RESULT OF SUB INCORRECT ; OR SEQUENCE ERROR
1554				
1555				
1556				
1557				THIS TEST VERIFIES MODE 0,X DOUBLE OPERAND INSTRUCTIONS. IT SETS
1558				DATA IN R0 AND LOCATION 0 AND OPERATES UPON IT USING DOP INSTRUCTIONS.
1559				
1560				
***** TEST 114 TEST MODE 0,X DOUBLE-OPERAND INSTRUCTIONS *****				
007742 005212	000114	TST114:	INC (R2)	UPDATE TEST NUMBER
007744 022712			CMP #114,(R2)	;SEQUENCE ERROR?
007750 001024			BNE TST115-10	;BR TO ERROR HALT ON SEQ ERROR
1561 007752 005000			CLR R0	;R0=0
1562 007754 005010			CLR (R0)	;LOC. 0=0
1563 007756 105110			COMB (R0)	;LOC. 0=377
1564 007760 005220			INC (R0)+	;LOC. 0=400 R0=2
1565 007762 005400			NEG R0	;R0=-2
1566 007764 060037	000000		ADD R0,0#0	;TRY ADD 0,3; LOC. 0=376
1567 007770 100403			BMI DOP03A	;CC=0001?
1568 007772 001402			BEQ DOP03A	
1569 007774 102401			BVS DOP03A	
1570 007776 103404			BCS DOP03B	 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 764 ;=====
010000		DOP03A:	MOV #211,-(R2)	MOVE TO MAILBOX # ***** 211 *****
010000	012742 000211		INC -(R2)	;SET MSGTYP TO FATAL ERROR
010004	005242		HALT	;CC'S NOT SET CORRECTLY
010006	000000	DOP03B:	COMB 0#0	;LOC. 0=1
1571 010010 105137	000000		DEC 0#0	;LOC. 0=0
1572 010014 005337	000000		BEQ TST115	 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ;=====
1573 010020 001404				

010022 012742 000212  
010026 005242  
010030 000000

MOV #212,-(R2)  
INC -(R2)  
HALT

WHICH FOLLOWS W/ 753  
MOVE TO MAILBOX # \*\*\*\*\* 212 \*\*\*\*\*  
SET MSGTYP TO FATAL ERROR  
DATA RESULT INCORRECT  
OR SEQUENCE ERROR

◀====

1574  
1575  
1576  
1577  
1578  
1579  
1580

THIS TEST VERIFIES MODE 0,0 DOP NON-MODIFYING INSTRUCTIONS.  
R0 AND R4 ARE PRESET TO 0 AND 1 RESPECTIVELY. COMPARE INSTRUCTIONS ARE  
THEN EXECUTED AND CHECKED. FIRST R4 IS COMPARED TO R0 THEN R0 TO R4.

	010032	005212
	010034	022712
	010040	001042
1581	010042	005000
1582	010044	005004
1583	010046	005204
1584	010050	020400
1585	010052	003004

```
IST115: INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #115, (R2)    ;SEQUENCE ERROR?
        BNE      TST116-10   ;BR TO ERROR HALT ON SEQ ERROR
        CLR      R0            ;R0=0
        CLR      R4            ;R4=0
        INC      R4            ;R4=1
        CMP      R4, R0        ;TRY COMPARE R4 TO R0
        BGT      DNM1
```

```
;UPDATE TEST NUMBER  
;SEQUENCE ERROR?  
;BR TO ERROR HALT ON SEQ ERROR  
;R0=0  
;R4=0  
;R4=1  
;TRY COMPARE R4 TO R0  
  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
;           CONDITIONAL BRANCH INST. AND <=====  
;           REPLACE THE MOVE INSTRUCTION <=====  
;           WHICH FOLLOWS W/ 772 <=====
```

010054	012742	000213
010060	005242	
010062	000000	
1586	010064	020004
1587	010066	002404

	MOV	#213,-(R2)
	INC	-(R2)
DNM1:	HALT	
	CMP	R0,R4
	BLT	DNM2

:MOVE TO MAILBOX # \*\*\*\*\* 213 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:CC'S NOT CORRECT FOR CMP  
:TRY COMPARE R0 TO R4

10

010070	012742	000214
010074	005242	
010076	000000	
1588	010100	005200
1589	010102	020400
1590	010104	001604

```

MOV      #214,-(R2)
INC      -(R2)
HALT
DNM2:   INC      R0
          CMP      R4,R0
          BEQ      DNM3

```

WHICH FOLLOWS W/ 784  
MOVE TO MAILBOX # \*\*\*\*\* 214 \*\*\*\*\*

	010106	012742	000215
	010112	005242	
	010114	000000	
1591	010116	005000	
1592	010120	005100	
1593	010122	005004	
1594	010124	030004	
1595	010126	001404	

MOV	#215,-(R2)
INC	-(R2)
HALT	
DNM3:	
CLR	R0
COM	R0
CLR	R4
BIT	R0,R4
BFA	DNM4

;MOVE TO MAILBOX # \*\*\*\*\* 215 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;CC'S NOT CORRECT (Z=1) FOR CMP  
;R0=0  
;R0=177777  
;R4=0  
;TRY BIT R0 TO R4

010130	012742	000216	MOV #216,-(R2)	:MOVE TO MAILBOX # ***** 216 *****
010134	005242		INC -(R2)	;SET MSGTYP TO FATAL ERROR
010136	000000		HALT	;CC'S NOT CORRECT FOR BIT
1596	010140	005304	DNM4: DEC R4	;R4=177777
1597	010142	030004	BIT R0,R4	;TRY BIT AGAIN
1598	010144	100404	BMI TST116	
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 735 <=====
010146	012742	000217	MOV #217,-(R2)	:MOVE TO MAILBOX # ***** 217 *****
010152	005242		INC -(R2)	;SET MSGTYP TO FATAL ERROR
010154	000000		HALT	;CC'S NOT CORRECT FOR BIT ; OR SEQUENCE ERROR <=====
1599				*****
1600				*****
1601				THIS TEST VERIFIES MODE 0,X DOUBLE OPERAND NON-MODIFYING INSTRUCTIONS.
1602				;IT SETS DATA IN R0 AND LOCATION 0 AND COMPARES THEM USING DOPNM INSTRUCTIONS.
1603				*****
1604				;TEST 116 TEST MODE 0,X DOUBLE-OPERAND NON-MODIFYING INSTS. *****
010156	005212	000116	TST116: INC (R2)	:UPDATE TEST NUMBER <=====
010160	022712		CMP #116,(R2)	;SEQUENCE ERROR? <=====
010164	001022		BNE TST117-10	;BR TO ERROR HALT ON SEQ ERROR <=====
1605	010166	005000	CLR R0	;R0=0 <=====
1606	010170	005010	CLR (R0)	;LOC. 0=0 <=====
1607	010172	005110	COM (R0)	;LOC. 0=177777 <=====
1608	010174	005200	INC R0	;R0=1 <=====
1609	010176	020037	CMP R0, #0	;TRY CMP MODE 0,3 <=====
1610	010202	100403	BMI DNM03A	;CC=0001 <=====
1611	010204	001402	BEQ DNM03A	
1612	010206	102401	BVS DNM03A	
1613	010210	103404	BCS DNM03B	
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 765 <=====
010212	012742	000220	DNM03A:	
010216	005242		MOV #220,-(R2)	:MOVE TO MAILBOX # ***** 220 *****
010220	000000		INC -(R2)	;SET MSGTYP TO FATAL ERROR
1614	010222	005300	HALT	;CC'S NOT SET CORRECTLY
1615	010224	001002	DNM03B: DEC R0	
1616	010226	005210	BNE DNM03C	
1617	010230	001404	INC (R0)	
				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 755 <=====
010232	012742	000221	DNM03C:	
010236	005242		MOV #221,-(R2)	:MOVE TO MAILBOX # ***** 221 *****
010240	000000		INC -(R2)	;SET MSGTYP TO FATAL ERROR
				;DATA INCORRECTLY MODIFIED BY CMP ; OR SEQUENCE ERROR <=====
1618				*****
1619				*****

1620 ; THIS TEST VERIFIES MODE 1 DOP INSTRUCTIONS. R0 IS SET TO -1  
1621 ; AND LOC 0 TO 1. R4 IS THEN CLEARED AND USED TO POINT TO LOC 0.  
1622 ; IN THE ADD MODE 1 INSTRUCTION, LOC 0 IS ADDED TO R0 AND THE  
1623 ; RESULTS VERIFIED.  
1624 ;

;TEST 117			TEST MODE 1 W/ DOP INST.		
;*****			*****		
010242 005212		000117	TST117: INC	(R2)	:UPDATE TEST NUMBER
010244 022712			CMP	#117, (R2)	:SEQUENCE ERROR?
010250 001007			BNE	TST120-10	:BR TO ERROR HALT ON SEQ ERROR
1626 010252 005000			CLR	R0	:R0=0
1627 010254 005100			COM	R0	:R0=177777
1628 010256 005004			CLR	R4	:R4=0
1629 010260 005014			CLR	(R4)	:LOC 0=0
1630 010262 005214			INC	(R4)	:LOC 0=1
1631 010264 061400			ADD	(R4), R0	:TRY ADD SOURCE MODE 1
1632 010266 001404			BEQ	TST120	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 770
010270 012742 000222			MOV	#222,-(R2)	===== 222 =====
010274 005242			INC	-(R2)	:MOVE TO MAILBOX # ***** 222 ***** SET MSGTYP TO FATAL ERROR
010276 000000			HALT		:RESULT OF ADD INCORRECT OR SEQUENCE ERROR

1633  
1634  
1635  
1636 THIS TEST VERIFIES MODE 1 DOP BYTE INSTRUCTIONS WHICH ADDRESS  
1637 EVEN BYTES. LOC. 0 IS SET TO -1 AND R4 IS CLEARED. THEN R4 IS  
1638 SET TO -1 USING A BISB THRU R0 WITH MODE 1.  
1639  
1640

			:TEST 120	TEST MODE 1 - EVEN BYTE W/ DOP INSTS.	
			:*****		
010300	005212		TST120: INC	(R2)	:UPDATE TEST NUMBER
010302	022712	000120	CMP	#120,(R2)	:SEQUENCE ERROR?
010306	001007		BNE	TST121-10	:BR TO ERROR HALT ON SEQ ERROR
1641	010310	005000	CLR	R0	:R0=0
1642	010312	005010	CLR	(R0)	:LOC. 0=0
1643	010314	005110	COM	(R0)	:LOC. 0=177777
1644	010316	005004	CLR	R4	:R4=0
1645	010320	151004	BISB	(R0),R4	:TRY MODE 1- EVEN BYTE W/ DOP
1646	010322	105104	COMB	R4	:R4=0
1647	010324	001404	BEQ	TST121	
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 770		
			<=====		
			<=====		
			<=====		
			<=====		
010326	012742	000223	MOV	#223,-(R2)	:MOVE TO MAILBOX # ***** 223 *****
010332	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR
010334	000000		HALT		:RESULT OF BISB IS INCORRECT : OR SEQUENCE ERROR

1651 : THIS TEST VERIFIES MODE 1 DOP NON-MODIFYING INSTRUCTIONS  
1652 : WHICH ADDRESS EVEN BYTES. LOC. 0 IS SET TO -1 AND R0 IS CLEARED  
1653 : AND USED AS THE ADDRESSING REGISTER. R4 IS SET TO 377 AND A  
1654 : MODE 1,0 CMPB INSTRUCTION IS USED THE RESULTS VERIFIED.  
1655

TEST 121 TEST MODE 1 - EVEN BYTE W/ DOP NON-MOD INST

	010336	005212
	010340	022712
	010344	001007
1657	010346	005000
1658	010350	005010
1659	010352	005110
1660	010354	005004
1661	010356	105104
1662	010360	121004
1663	010362	001404

```

TST121: INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #121,(R2)       ;SEQUENCE ERROR?
        BNE      TST122-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLR      R0              ;R0=0
        CLR      (R0)           ;LOC 0=0
        COM      (R0)           ;LOC 0=177777
        CLR      R4              ;R4=0
        COMB    R4              ;R4=377
        CMPB    (R0),R4         ;TRY MODE 1 - EVEN BYTE W/ DOP
        BEQ      TST122

```

010364 012742 000224  
010370 005242  
010372 000000

MOV #224,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 224 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;RESULT OF CMPB INCORRECT  
; OR SEQUENCE ERROR

1664  
1665  
1666  
1667  
1668  
1669  
1670  
1671  
1672  
1673  
1674  
1675  
1676

THIS TEST VERIFIES MODE 1,0 MOVB INSTRUCTIONS WHICH ADDRESS EVEN BYTES. LOC. 0 IS SET TO 177400 R0 IS CLEARED AND R4 IS SET TO -1. MOVB ARE USED TO MOVE BYTE 0 TO R4. THIS VERIFIES THAT THE PROPER BYTE WAS SELECTED AND THAT THE SIGN-X-TEND FUNCTION WITH MODE 0.

THE LOC. 0 IS COMPLEMENTED AND THE SAME PROCEDURE EXERCISES  
THE LOGIC FOR COMPLEMENTARY DATA.  
THIS TEST EXERCISES UNIQUE MICROCODE.

## TEST 122 TEST MOV INSTRUCTION MODE 1,0 EVEN BYTE

	010374	005212
	010376	022712
	010402	001020
1677	010404	005000
1678	010406	005010
1679	010410	105110
1680	010412	005110
1681	010414	005004
1682	010416	005104
1683	010420	111004
1684	010422	005704
1685	010424	001404

```

TST122: INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #122,(R2)       ;SEQUENCE ERROR?
        BNE      TST123-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLR      R0              ;R0=0
        CLR      (R0)           ;LOC 0=0
        COMB    (R0)           ;LOC 0=177400
        COM      (R0)
        CLR      R4              ;R4=0
        COM      R4              ;R4=177777
        MOVB   (R0),R4         ;R4=0
        TST      R4              ;CHECK SIGN OF WORD
        BEQ      DOP1

```

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 766

010426 012742 000225      MOV #225,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 225 \*\*\*\*\*  
 010432 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 010434 000000      HALT ;MOVVB SHOULD SIGN X-TEND  
 1686 010436 005110      DOP1: COM (R0) ;LOC 0=177777  
 1687 010440 111004      MOVB (R0),R4 ;DO MOVVB W/ EVEN BYTE  
 1688 010442 100404      BMI TST123 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                                   ; CONDITIONAL BRANCH INST. AND  
                                   ; REPLACE THE MOVE INSTRUCTION  
                                   ; WHICH FOLLOWS W/ 757

010444 012742 000226      MOV #226,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 226 \*\*\*\*\*  
 010450 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 010452 000000      HALT ;MOVVB SHOULD SIGN X-TEND  
                                   ; OR SEQUENCE ERROR

1689  
1690  
1691  
1692  
1693  
1694  
1695  
1696  
1697

\*\*\*\*\*  
 : THIS TEST VERIFIES MODE 1 DOP INSTRUCTIONS WHICH REFERENCE  
 : ODD BYTES. LOC. 0 IS SET TO 177400. R0 IS SET TO 0 AND R4 IS  
 : SET TO 1. THE BISB INSTRUCTION USES THE DATA IN BYTE 1 TO SET BYTE 0.  
 : THE RESULT IS CHECKED BY INCREMENTING THE WORD (LOC. 0) TO ZERO.

\*\*\*\*\*  
 :TEST 123 TEST MODE 1-ODD BYTE W/ DOP INSTS.

010454 005212      TST123: INC (R2) ;UPDATE TEST NUMBER  
 010456 022712 000123      CMP #123,(R2) ;SEQUENCE ERROR?  
 010462 001010      BNE TST124-10 ;BR TO ERROR HALT ON SEQ ERROR  
 1698 010464 005000      CLR R0 ;R0=0  
 1699 010466 005010      CLR (R0) ;LOC. 0=0  
 1700 010470 005004      CLR R4 ;R4=0  
 1701 010472 005204      INC R4 ;R4=1  
 1702 010474 105114      COMB (R4) ;LOC. 0=177400  
 1703 010476 151410      BISB (R4),(R0) ;TRY TO BIS LOW ORDER BITS W/ MODE 1  
 1704 010500 005210      INC (R0) ;CHECK RESULT  
 1705 010502 001404      BEQ TST124 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                                   ; CONDITIONAL BRANCH INST. AND  
                                   ; REPLACE THE MOVE INSTRUCTION  
                                   ; WHICH FOLLOWS W/ 767

010504 012742 000227      MOV #227,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 227 \*\*\*\*\*  
 010510 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 010512 000000      HALT ;RESULT OF BISB INCORRECT  
                                   ; OR SEQUENCE ERROR

1706  
1707  
1708  
1709  
1710  
1711  
1712  
1713  
1714

\*\*\*\*\*  
 : THIS TEST VERIFIES MODE 2 DOP INSTRUCTIONS. LOC. 0 IS SET TO -1.  
 : R0 IS CLEARED AND USED AS THE MODE 2 ADDRESSING REGISTER TO MOVE LOC. 0  
 : TO R7. THE DATA RESULTS ARE VERIFIED AND THE INCREMENTING OF THE REGISTER  
 : IS CHECKED.

\*\*\*\*\*  
 :TEST 124 TEST MODE 2 W/ DOP INSTS.

010514 005212      TST124: INC (R2) ;UPDATE TEST NUMBER  
 010516 022712 000124      CMP #124,(R2) ;SEQUENCE ERROR?

1715 010522 001015                    BNE      TST125-10      ;BR TO ERROR HALT ON SEQ ERROR  
 1715 010524 005000                    CLR      R0              ;R0=0  
 1716 010526 005010                    CLR      (R0)          ;LOC. 0=0  
 1717 010530 005110                    COM      (R0)          ;LOC. 0=177777  
 1718 010532 012004                    MOV      (R0)+,R4     ;TRY MOVE MODE 2,0  
 1719 010534 005204                    INC      R4              ;CHECK R4  
 1720 010536 001404                    BEQ      DOP2          ;  
  
 1721 010540 012742 000230            MOV      #230,-(R2)    ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 1721 010544 005242                    INC      -(R2)          CONDITIONAL BRANCH INST. AND  
 1721 010546 000000                    HALT                    REPLACE THE MOVE INSTRUCTION  
 1722 010550 005300                    DOP2:                WHICH FOLLOWS W/ 771  
 1722 010552 005300                    DEC      R0              <=====  
 1723 010554 001404                    DEC      R0              <=====  
 1723 010556 012742 000231            BEQ      TST125        <=====  
  
 1724 010556 012742 000231            MOV      #231,-(R2)    ;MOVE TO MAILBOX # \*\*\*\*\* 231 \*\*\*\*\*  
 1724 010562 005242                    INC      -(R2)          ;SET MSGTYP TO FATAL ERROR  
 1724 010564 000000                    HALT                    ;RESULT OF MOV INST INCORRECT  
  
 1725 1726 1727 1728 1729 1730 1731 1732 1733 1734                    DOP2:                ;TEST R0 AFTER MODE 2  
  
 1735 010566 005212                    TST125:            : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 1735 010570 022712 000125            INC      (R2)          CONDITIONAL BRANCH INST. AND  
 1735 010574 001016                    CMP      #125,(R2)    REPLACE THE MOVE INSTRUCTION  
 1735 010576 005000                    BNE      TST126-10    WHICH FOLLOWS W/ 771  
 1736 010600 010010                    CLR      R0              <=====  
 1736 010602 005110                    MOV      R0,(R0)     <=====  
 1737 010604 142010                    COM      (R0)          <=====  
 1738 010606 105737 000001            BICB     (R0)+,(R0)    <=====  
 1739 010606 105737 000001            TSTB     @#1            TRY TO CLEAR BYTE 1 FROM BYTE 0 W/ BICB  
 1740 010612 001404                    BEQ      DOPB2A        ;CHECK RESULT  
  
 1741 010614 012742 000232            MOV      #232,-(R2)    ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 1741 010620 005242                    INC      -(R2)          CONDITIONAL BRANCH INST. AND  
 1741 010622 000000                    HALT                    REPLACE THE MOVE INSTRUCTION  
 1742 010624 105137 000000            DOPB2A:            WHICH FOLLOWS W/ 770  
 1742 010630 001404                    COMB     @#0              <=====  
 1742 010630 001404                    BEQ      TST126        <=====  
  
 1743 1744 1745 1746 1747 1748 1749 1750 1751 1752                    DOPB2A:            ;MOVE TO MAILBOX # \*\*\*\*\* 232 \*\*\*\*\*  
 1743 1744 1745 1746 1747 1748 1749 1750 1751 1752                    SET MSGTYP TO FATAL ERROR  
 1743 1744 1745 1746 1747 1748 1749 1750 1751 1752                    BICB DESTINATION INCORRECT  
 1743 1744 1745 1746 1747 1748 1749 1750 1751 1752                    CHECK BICB SOURCE  
  
 1743 1744 1745 1746 1747 1748 1749 1750 1751 1752                    ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====

010632 012742 000233  
010636 005242  
010640 000000

MOV #233,-(R2)  
INC -(R2)  
HALT

CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 761  
MOVE TO MAILBOX # \*\*\*\*\* 233 \*\*\*\*\*  
SET MSGTYP TO FATAL ERROR  
BICB SOURCE INCORRECTLY CHANGED  
OR SEQUENCE ERROR

1743  
1744  
1745  
1746  
1747  
1748  
1749  
1750

\*\*\*\*\* THIS TEST VERIFIES MODE 2 DOP BYTE INSTRUCTIONS WHICH REFERENCE  
ODD BYTES. R0 IS SET TO 1, LOC. 0 IS SET TO 177400, AND R4 IS CLEARED.  
A MODE 2 MOVB USES R0 TO MOVE BYTE 1 TO R4. AN INCREMENT  
IS USED TO CHECK THAT THE PROPER BYTE WAS MOVED AND SIGN X-TENDED.

TEST 126 TEST MODE 2 - ODD BYTE W/ DOP INST.

010642 005212  
010644 022712 000126  
010650 001017  
1751 010652 005000  
1752 010654 005004  
1753 010656 005010  
1754 010660 005110  
1755 010662 105120  
1756 010664 112004  
1757 010666 005204  
1758 010670 001404

TST126: INC (R2) ;UPDATE TEST NUMBER  
CMP #126,(R2) ;SEQUENCE ERROR?  
BNE TST127-10 ;BR TO ERROR HALT ON SEQ ERROR  
CLR R0 ;R0=0  
CLR R4 ;R4=0  
CLR (R0) ;LOC. 0=0  
COM (R0) ;LOC. 0=177777  
COMB (R0)+ ;LOC 0=177400; R0=1  
MOVB (R0)+,R4 ;TRY DOP MODE 2 W/ ODD BYTE  
INC R4 ;CHECK RESULT OF MOVB  
BEQ DOPB2B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 767

010672 012742 000234  
010676 005242  
010700 000000  
1759 010702 005740  
1760 010704 005700  
1761 010706 001404

MOV #234,-(R2)  
INC -(R2)  
HALT  
DOPB2B: TST -(R0)  
TST R0  
BEQ TST127

MOVE TO MAILBOX # \*\*\*\*\* 234 \*\*\*\*\*  
SET MSGTYP TO FATAL ERROR  
RESULT OF MOVB INCORRECT  
BUMP R0 DOWN BY 2  
CHECK R0

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 760

010710 012742 000235  
010714 005242  
010716 000000

MOV #235,-(R2)  
INC -(R2)  
HALT

MOVE TO MAILBOX # \*\*\*\*\* 235 \*\*\*\*\*  
SET MSGTYP TO FATAL ERROR  
MODE 2 BYTE DID NOT INCREMENT REG. CORRECTLY  
; OR SEQUENCE ERROR

1762  
1763  
1764  
1765  
1766  
1767  
1768  
1769  
1770

\*\*\*\*\* THIS TEST VERIFIES MODE 3 DOUBLE-OPERAND INSTRUCTIONS.  
LOC. 0 IS LOADED WITH ALTERNATING ZEROES AND ONES; AND R0 IS LOADED  
WITH ALTERNATING ONES AND ZEROES. A MODE 3 BIS IS USED TO SET R0  
TO -1 BY USING LOC. 0 AS THE SOURCE TO BIS THE ZEROES IN R0. THE  
RESULT IS TESTED BY INCREMENTING R0 AND CHECKING FOR ZERO.

TEST 127 TEST MODE 3 W/ DOP INSTS.

T127 TEST MODE 3 W/ DOP INSTS.

SEQ 0079

010720 005212	000127	TST127: INC (R2)	:UPDATE TEST NUMBER	<=====
010722 022712		CMP #127, (R2)	:SEQUENCE ERROR?	<=====
010726 001011		BNE TST130-10	:BR TO ERROR HALT ON SEQ ERROR	<=====
1771 010730 012737 052525 000000		MOV #052525, a#0	:MOVE 52525 TO LOC. 0	<=====
1772 010736 012700 125252 000000		MOV #125252, R0	:SET ALT. ONE AND ZERO IN R0	<=====
1773 010742 053700 000000		BIS a#0, R0	:TRY TO SET ALL OTHER BITS W/ MODE 3	<=====
1774 010746 005200		INC R0	:TEST RESULT	<=====
1775 010750 001404		BEQ TST130		
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 766				
010752 012742 000236		MOV #236, -(R2)	:MOVE TO MAILBOX # ***** 236 *****	<=====
010756 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
010760 000000		HALT	:BIS W/ MODE 3 INCORRECT RESULT : OR SEQUENCE ERROR	<=====
*****				
1776				
1777				
1778			THIS TEST VERIFIES MODE 3 DOUBLE OPERAND BYTE INSTRUCTIONS WHICH	
1779			ADDRESS EVEN BYTES. BYTE 0 IS SET TO ALTERNATING 1'S AND 0'S; BYTE 1,	
1780			ALTERNATING 0'S AND 1'S. R0 IS CLEARED AND A BISB IS USED TO	
1781			SET THE LOW BYTE OF R0 TO 252.	
1782			*****	
1783			TEST 130 TEST MODE 3 - EVEN BYTE W/ DOP INSTS.	
*****				
010762 005212	000130	TST130: INC (R2)	:UPDATE TEST NUMBER	<=====
010764 022712		CMP #130, (R2)	:SEQUENCE ERROR?	<=====
010770 001011		BNE TST131-10	:BR TO ERROR HALT ON SEQ ERROR	<=====
1784 010772 012737 052652 000000		MOV #52652, a#0	:MOVE 1'S AND 0' PATTERN TO LOC. 0	<=====
1785 011000 005000		CLR R0	:R0=0	<=====
1786 011002 153700 000000		BISB a#0, R0	:TRY R0=252 W/ MODE 3 - EVEN BYTE	<=====
1787 011006 022700 000252		CMP #252, R0	:BISB W/ EVEN BYTE SUCCESSFUL?	<=====
1788 011012 001404		BEQ TST131		
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 766				
011014 012742 000237		MOV #237, -(R2)	:MOVE TO MAILBOX # ***** 237 *****	<=====
011020 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
011022 000000		HALT	:BISB W/ MODE 3 - EVEN BYTE FAILED : OR SEQUENCE ERROR	<=====
*****				
1789				
1790				
1791			THIS TEST VERIFIES MODE 3 DOUBLE OPERAND BYTE INSTRUCTIONS	
1792			WHICH ADDRESS ODD BYTES. THE SAME PROCEDURE USED IN PREVIOUS	
1793			TEST IS USED HERE. THIS TIME BYTE 1 IS USED AS THE SOURCE BYTE.	
1794			THE EXPECTED RESULT IS: R0 = 125.	
1795			*****	
1796			TEST 131 TEST MODE 3 - ODD BYTE W/ DOP INSTS.	
*****				
011024 005212	000131	TST131: INC (R2)	:UPDATE TEST NUMBER	<=====
011026 022712		CMP #131, (R2)	:SEQUENCE ERROR?	<=====
011032 001011		BNE TST132-10	:BR TO ERROR HALT ON SEQ ERROR	<=====
1797 011034 012737 052652 000000		MOV #52652, a#0	:MOVE 1'S AND 0'S PATTERN TO LOC 0	<=====
1798 011042 005000		CLR R0	:R0=0	<=====

1799 011044	153700	000001	BISB	#1, R0	: TRY R0=152 W/ MODE 3 - ODD BYTE	<=====
1800 011050	022700	000125	CMP	#125, R0	: R0=125?	<=====
1801 011054	001404		BEQ	TST132	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766	<=====
011056	012742	000240	MOV	#240, -(R2)	: MOVE TO MAILBOX # ***** 240 *****	<=====
011062	005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR	<=====
011064	000000		HALT		: BISB W/ MODE 3 - ODD BYTE FAILED OR SEQUENCE ERROR	<=====
1802			***** TEST 132 TEST DEST. MODE 0-BYTE W/ DOP NON-MODIFYING MST *****			
1803			***** TST132: INC (R2) : UPDATE TEST NUMBER			
011066	005212		CMP	#132, (R2)	: SEQUENCE ERROR?	<=====
011070	022712	000132	BNE	TST133-10	: BR TO ERROR HALT ON SEQ ERROR	<=====
011074	001017		CLR	R0	: R0=0	<=====
1804 011076	005000		COMB	R0	: R0=377	<=====
1805 011100	105100		+SEC!SEV		: SET C AND V BITS	<=====
1806 011102	000263		BITB	#200, R0	: TRY DOPNM DEST. MODE 0-BYTE	<=====
1807 011104	132700	000200	BEQ	DNMBOA	: BR TO ERROR IF Z BIT SET	<=====
1808 011110	001403		BVS	DNMBOA	: BR TO ERROR IF V BIT SET	<=====
1809 011112	102402		BCC	DNMBOA	: BR TO ERROR IF C BIT CLEAR.	<=====
1810 011114	103001		BMI	DNMBOB		
1811 011116	100404				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766	<=====
011120	012742	000241	***** DNMBOA: *****			
011120	012742	000241	MOV	#241, -(R2)	: MOVE TO MAILBOX # ***** 241 *****	<=====
011124	005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR	<=====
011126	000000		HALT		: CC'S INCORRECT	<=====
1812 011130	105100		DNMBOB: COMB	R0	: CHECK DESTINATION DATA	<=====
1813 011132	001404		BEQ	TST133		
011134	012742	000242	***** TST133 TEST DEST. MODE 1 W/ DOP NON-MODIFYING INST *****			
011140	005242		MOV	#242, -(R2)	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 760	<=====
011142	000000		INC	-(R2)	: MOVE TO MAILBOX # ***** 242 *****	<=====
1814			HALT		: SET MSGTYP TO FATAL ERROR	<=====
1815					: DEST. DATA MODIFIED	<=====
					: OR SEQUENCE ERROR	<=====
011144	005212		***** TST133: *****			
011146	022712	000133	INC	(R2)	: UPDATE TEST NUMBER	<=====
011152	001017		CMP	#133, (R2)	: SEQUENCE ERROR?	<=====
1816 011154	005000		BNE	TST134-10	: BR TO ERROR HALT ON SEQ ERROR	<=====
1817 011156	005010		CLR	R0	: R0=0	<=====
1818 011160	000241		CLR	(R0)	: LOC. 0=0	<=====
1819 011162	032710	177777	CLC		: CLEAR C BIT	<=====
1820 011166	100403		BIT	#177777, (R0)	: TRY DOPNM DEST. MODE 1	<=====
1821 011170	102402		BMI	DNM1A	: BR TO ERROR IF N BIT SET	<=====
			BVS	DNM1A	: BR TO ERROR IF V BIT SET	<=====

1822 011172 103401		BCS	DNM1A	:BR TO ERROR IF C BIT SET	
1823 011174 001404		BEQ	DNM1B	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766	<=====
011176 012742 000243	DNM1A:	MOV	#243,-(R2)	:MOVE TO MAILBOX # ***** 243 *****	<=====
011176 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
011202 000000		HALT		:COND. CODES INCORRECT	<=====
1824 011206 005710	DNM1B:	TST	(R0)	:CHECK TEST DATA	<=====
1825 011210 001404		BEQ	TST134	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 760	<=====
011212 012742 000244		MOV	#244,-(R2)	:MOVE TO MAILBOX # ***** 244 *****	<=====
011216 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
011220 000000		HALT		:DESTINATION DATA MODIFIED : OR SEQUENCE ERROR	<=====
1826		;***** TEST 134 TEST DEST. MODE 2 W/ DOP NON-MODIFYING INST.			
1827		;*****			
011222 005212 000134	TST134:	INC	(R2)	:UPDATE TEST NUMBER	
011224 022712		CMP	#134,(R2)	:SEQUENCE ERROR?	
011230 001027		BNE	TST135-10	:BR TO ERROR HALT ON SEQ ERROR	
1828 011232 005000		CLR	R0	:R0=0	
1829 011234 005010		CLR	(R0)	:LOC. 0=0	
1830 011236 052710 125252		BIS	#125252,(R0)	:LOC. 0=125252	
1831 011242 032720 077777		BIT	#77777,(R0)+	:TRY DOPNM INST W/ MODE 2	
1832 011246 102402		BVS	DNM2A	:BR TO ERROR IF V BIT SET	
1833 011250 001401		BEQ	DNM2A	:BR TO ERROR IF Z-BIT SET	
1834 011252 100004		BPL	DNM2B	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766	<=====
011254 012742 000245	DNM2A:	MOV	#245,-(R2)	:MOVE TO MAILBOX # ***** 245 *****	<=====
011254 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
011260 000000		HALT		:COND. CODES INCORRECT	<=====
1835 011264 005300	DNM2B:	DEC	R0	:DECREMENT R0 TO CHECK IT.	<=====
1836 011266 005300		DEC	R0		
1837 011270 001404		BEQ	DNM2D	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 757	<=====
011272 012742 000246	DNM2C:	MOV	#246,-(R2)	:MOVE TO MAILBOX # ***** 246 *****	<=====
011272 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
011300 000000		HALT		:MODE 2 REGISTER NOT INCREMENTED BY 2	<=====
1838 011302 022710 125252	DNM2D:	CMP	#125252,(R0)	:CHECK DEST. DATA	<=====
1839 011306 001404		BEQ	TST135	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND	<=====

T134 TEST DEST. MODE 2 W/ DOP NON-MODIFYING INST.

SEQ 0082

1840  
1841

011320	005212	
011322	022712	000135
011326	001051	
1842 011330	005000	
1843 011332	005010	
1844 011334	052710	052652
1845 011340	000263	
1846 011342	132720	000201
1847 011346	001403	
1848 011350	103002	
1849 011352	102401	
1850 011354	100404	

MOV #247,-(R2)  
INC -(R2)  
HALT

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 750 <=====  
MOVE TO MAILBOX # \*\*\*\*\* 247 \*\*\*\*\* <=====  
SET MSGTYP TO FATAL ERROR  
DEST. DATA MODIFIED  
OR SEQUENCE ERROR

;\*\*\*\*\* TEST 135 TEST DEST. MODE 2-BYTE, W/DOP NON-MODIFYING INST \*\*\*\*\*

T135:	INC	(R2)
	CMP	#135,(R2)
	BNE	TST136-10
	CLR	R0
	CLR	(R0)
	BIS	#52652,(R0)
+SEC!SEV		
	BITB	#201,(R0)+
	BEQ	DNMB2A
	BCC	DNMB2A
	BVS	DNMB2A
	BMI	DNMB2B

UPDATE TEST NUMBER  
SEQUENCE ERROR?  
BR TO ERROR HALT ON SEQ ERROR  
R0=0  
LOC. 0=0  
LOC. 0=52652  
SET C AND V BITS  
TRY DOPNM INST. W/ MODE 2 EVEN BYTE  
BR TO ERROR IF Z-BIT SET  
BR TO ERROR IF C-BIT CLEAR  
BR TO ERROR IF V-BIT SET

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 764 <=====  
<=====  
<=====  
<=====

011356	012742	000250
011356	012742	
011362	005242	
011364	000000	
1851 011366	005300	
1852 011370	001404	

DNMB2A:  
MOV #250,-(R2)  
INC -(R2)  
HALT

DNMB2B: DEC R0  
BEQ DNMB2C

MOVE TO MAILBOX # \*\*\*\*\* 250 \*\*\*\*\*  
SET MSGTYP TO FATAL ERROR  
COND. CODES INCORRECT  
CHECK DEST. REGISTER.

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 764 <=====  
<=====  
<=====  
<=====

011372	012742	000251
011376	005242	
011400	000000	
1853 011402	005200	
1854 011404	132720	000201
1855 011410	001402	
1856 011412	102401	
1857 011414	100004	

DNMB2C:  
MOV #251,-(R2)  
INC -(R2)  
HALT

INC R0  
BITB #201,(R0)+  
BEQ DNMB2D ;BR TO ERROR IF Z-BIT SET  
BVS DNMB2D ;BR TO ERROR IF V-BIT SET  
BPL DNMB2E

MOVE TO MAILBOX # \*\*\*\*\* 251 \*\*\*\*\*  
SET MSGTYP TO FATAL ERROR  
DEST. REGISTER NOT INCREMENTED BY 1  
R0=1  
TRY DOPNM INST. W/MODE 2-CDD BYTE  
;BR TO ERROR IF Z-BIT SET  
;BR TO ERROR IF V-BIT SET

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 744 <=====  
<=====  
<=====  
<=====

011416	012742	000252
011416	012742	
011422	005242	
011424	000000	
1858 011426	005300	
1859 011430	005300	
1860 011432	001404	

DNMB2D:  
MOV #252,-(R2)  
INC -(R2)  
HALT

DEC R0  
DEC R0  
BEQ DNMB2F

MOVE TO MAILBOX # \*\*\*\*\* 252 \*\*\*\*\*  
SET MSGTYP TO FATAL ERROR  
COND. CODES INCORRECT  
DEC R0 TO CHECK IT.

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND <=====  
<=====

					REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 735 <=====
011434	012742	000253	MOV	#253,-(R2)	:MOVE TO MAILBOX # ***** 253 ***** <=====
011440	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR <=====
011442	000000		HALT		:DEST. REGISTER NOT INCREMENTED BY 1 <=====
1861	011444	022710	DNMB2F:	CMP #52652,(R0)	:CHECK DEST. DATA IS UNMODIFIED <=====
1862	011450	001404	BEQ	TST136	
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
					CONDITIONAL BRANCH INST. AND <=====
					REPLACE THE MOVE INSTRUCTION <=====
					WHICH FOLLOWS W/ 726 <=====
011452	012742	000254	MOV	#254,-(R2)	:MOVE TO MAILBOX # ***** 254 ***** <=====
011456	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR <=====
011460	000000		HALT		:DEST. DATA WAS MODIFIED. <=====
					: OR SEQUENCE ERROR <=====
1863					
1864					
1865					
					:***** TEST 136 TEST DEST. MODE 3-BYTES W/DOP NON-MODIFYING INST. *****
011462	005212	000136	TST136:	INC (R2)	:UPDATE TEST NUMBER <=====
011464	022712			CMP #136,(R2)	:SEQUENCE ERROR? <=====
011470	001050			BNE TST137-10	:BR TO ERROR HALT ON SEQ ERROR <=====
1866	011472	005000		CLR R0	:R0=0 <=====
1867	011474	005010		CLR (R0)	:LOC. 0=0 <=====
1868	011476	052710		BIS #125125,(R0)	:LOC. 0=125125 <=====
1869	011502	105100		COMB R0	:R0=377 <=====
1870	011504	005200		INC R0	:R0=400 <=====
1871	011506	005010		CLR (R0)	:LOC. 400=0 <=====
1872	011510	000263	+SEC!SEV		:C-BIT=V-BIT=1 <=====
1873	011512	132730	000201	BITB #201,a(R0)+	:TRY DOPNM W/MODE 3-EVEN BYTE <=====
1874	011516	001403		BEQ DNMB3A	:BR TO ERROR IF Z BIT SET <=====
1875	011520	102402		BVS DNMB3A	:BR TO ERROR IF V BIT SET <=====
1876	011522	103001		BCC DNMB3A	:BR TO ERROR IF C BIT CLEAR <=====
1877	011524	100004		BPL DNMB3B	
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
					CONDITIONAL BRANCH INST. AND <=====
					REPLACE THE MOVE INSTRUCTION <=====
					WHICH FOLLOWS W/ 761 <=====
011526	012742	000255	DNMB3A:	MOV #255,-(R2)	:MOVE TO MAILBOX # ***** 255 ***** <=====
011526	005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR <=====
011532	000000			HALT	:COND. CODES INCORRECT <=====
1878	011536	022700	DNMB3B:	CMP #402,R0	:CHECK DEST. REGISTER INC. BY 2 AND INC BY 2 AGAIN <=====
1879	011542	001404	BEQ	DNMB3C	
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
					CONDITIONAL BRANCH INST. AND <=====
					REPLACE THE MOVE INSTRUCTION <=====
					WHICH FOLLOWS W/ 752 <=====
011544	012742	000256	DNMB3C:	MOV #256,-(R2)	:MOVE TO MAILBOX # ***** 256 ***** <=====
011550	005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR <=====
011552	000000			HALT	:DEST. REGISTER NOT INCREMENTED BY 2 <=====
1880	011554	005200		INC R0	:R0=404 <=====
1881	011556	005200		INC R0	
1882	011560	132730	000201	BITB #201,a(R0)+	:TRY DOPNM DEST MODE 3-BYTE(ODD) <=====
1883	011564	001402		BEQ DNMB3D	:BR TO ERROR IF Z BIT SET <=====
1884	011566	102401		BVS DNMB3D	:BR TO ERROR IF V BIT SET <=====

1885 011570 100404

BMI DNMB3E

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 737 <=====

011572 012742 000257  
011576 005242  
011600 000000  
1886 011602 005004  
1887 011604 022714 125125  
1888 011610 001404

DNMB3D:

MOV #257,-(R2)  
INC -(R2)  
HALT

DNMB3E:

CLR R4  
CMP #125125,(R4)  
BEQ TST137

;MOVE TO MAILBOX # \*\*\*\*\* 257 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;COND. CODES INCORRECT  
;R4=0  
;CHECK DEST. DATA

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 727 <=====

011612 012742 000260  
011616 005242  
011620 000000

MOV #260,-(R2)  
INC -(R2)  
HALT

;MOVE TO MAILBOX # \*\*\*\*\* 260 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;DEST. DATA MODIFIED  
; OR SEQUENCE ERROR

1889  
1890

;\*\*\*\*\* TEST 137 TEST DEST. MODE 4 W/DOP NON-MODIFYING INST.

011622 005212  
011624 022712 000137  
011630 001033  
1891 011632 005000  
1892 011634 005010  
1893 011636 052710 125252  
1894 011642 052700 000002  
1895 011646 000277  
1896 011650 032740 020000  
1897 011654 100403  
1898 011656 102402  
1899 011660 103001  
1900 011662 001004

TST137: INC (R2)  
CMP #137,(R2)  
BNE TST140-10  
CLR R0  
CLR (R0)  
BIS #125252,(R0)  
BIS #2,R0  
SCC  
BIT #20000,-(R0)  
BMI DNM4A  
BVS DNM4A  
BCC DNM4A  
BNE DNM4B

;UPDATE TEST NUMBER  
;SEQUENCE ERROR?  
;BR TO ERROR HALT ON SEQ ERROR  
;R0=0  
;LOC. 0=0  
;LOC. 0=125125  
;R0=2  
;SET ALL COND. CODE BITS  
;TRY DOPNM W/ MODE 4  
;BR TO ERROR IF N-BIT SET  
;BR TO ERROR IF V-BIT SET  
;BR TO ERROR IF C-BIT CHAR

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 762 <=====

011664 012742 000261  
011664 005242  
011670 000000  
1901 011674 005700  
1902 011676 001404

DNM4A:

MOV #261,-(R2)  
INC -(R2)

DNM4B:

TST R0  
BEQ DNM4C

;MOVE TO MAILBOX # \*\*\*\*\* 261 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;COND. CODES INCORRECT  
;CHECK DEST. REGISTER

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 754 <=====

011700 012742 000262  
011704 005242  
011706 000000  
1903 011710 022737 125252 000000 DNM4C:  
1904 011716 001404

MOV #262,-(R2)  
INC -(R2)  
HALT  
CMP #125252,0#0  
BEQ TST140

;MOVE TO MAILBOX # \*\*\*\*\* 262 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;DEST. REGISTER NOT DECREMENTED BY 2  
;CHECK DEST. DATA

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====

						CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 744	<==== <==== <====
011720	012742	000263	MOV	#263,-(R2)		:MOVE TO MAILBOX # ***** 263 *****	
011724	005242		INC	-(R2)		:SET MSGTYP TO FATAL ERROR	
011726	000000		HALT			:DEST. DATA MODIFIED	
						: OR SEQUENCE ERROR	
1905							
1906							
						;***** TEST 140 TEST DEST. MODE 4-BYTE W/ DOP NON-MODIFYING INST.	
011730	005212	000140	TST140:	INC (R2)		:UPDATE TEST NUMBER	
011732	022712			CMP #140,(R2)		:SEQUENCE ERROR?	
011736	001051			BNE TST141-10		:BR TO ERROR HALT ON SEQ ERROR	
1907 011740	005000			CLR R0		:R0=0	
1908 011742	005010			CLR (R0)		:LOC. 0=0	
1909 011744	052710	052652		BIS #52652,(R0)		:LOC. 0=52652	
1910 011750	052700	000002		BIS #2,R0		:R0=2	
1911 011754	000257			CCC		:COND. CODES=C	
1912 011756	132740	000201		BITB #201,-(R0)		:TRY DOPNM INST W/MODE 4 ODD BYTE	
1913 011762	102403			BVS DNMB4A		:BR TO ERROR IF V BIT SET	
1914 011764	001402			BEQ DNMB4A		:BR TO ERROR IF Z BIT SET	
1915 011766	103401			BCS DNMB4A		:BR TO ERROR IF C BIT SET	
1916 011770	001004			BNE DNMB4B			
						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 762	<==== <==== <==== <====
011772							
011772	012742	000264	DNMB4A:	MOV #264,-(R2)		:MOVE TO MAILBOX # ***** 264 *****	
011776	005242			INC -(R2)		:SET MSGTYP TO FATAL ERROR	
012000	000000			HALT		:COND. CODES INCORRECT	
1917 012002	022700	000001	DNMB4B:	CMP #1,R0		:CHECK DEST. REGISTER	
1918 012006	001404			BEQ DNMB4C			
						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 753	<==== <==== <==== <====
012010	012742	000265		MOV #265,-(R2)		:MOVE TO MAILBOX # ***** 265 *****	
012014	005242			INC -(R2)		:SET MSGTYP TO FATAL ERROR	
012016	000000			HALT		:DEST REG. NOT DECREMENTED BY 1	
1919 012020	132740	000201	DNMB4C:	BITB #201,-(R0)		:TRY DOPNM INST. W/MODE 4 EVEN BYTE	
1920 012024	001401			BEQ DNMB4D		:BR TO ERROR IF Z-BIT SET	
1921 012026	100404			BMI DNMB4E			
						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 743	<==== <==== <==== <====
012030							
012030	012742	000266	DNMB4D:	MOV #266,-(R2)		:MOVE TO MAILBOX # ***** 266 *****	
012034	005242			INC -(R2)		:SET MSGTYP TO FATAL ERROR	
012036	000000			HALT		:COND. CODES INCORRECT	
1922 012040	005700		DNMB4E:	TST R0		:CHECK DEST. REGISTER	
1923 012042	001404			BEQ DNMB4F			
						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION	<==== <==== <====

012044	012742	000267		MOV	#267,-(R2)	WHICH FOLLOWS W/ 735 MOVE TO MAILBOX # ***** 267 ***** SET MSGTYP TO FATAL ERROR DEST. REG. NOT DECREMENTED BY 1 CHECK DESTINATION DATA	<=====	
012050	005242			INC	-(R2)			
012052	000000			HALT				
1924	012054	022710	052652	DNMB4F:	CMP #52652,(R0)			
1925	012060	001404		BEQ	TST141			
						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 726	<=====	
							<=====	
							<=====	
							<=====	
012062	012742	000270		MOV	#270,-(R2)	MOVE TO MAILBOX # ***** 270 ***** SET MSGTYP TO FATAL ERROR DEST. DATA MODIFIED OR SEQUENCE ERROR	<=====	
012066	005242			INC	-(R2)			
012070	000000			HALT				
1926								
1927								
						***** TEST 141 TEST DEST MODE 5 W/DOP NON-MODIFYING INST. *****		
012072	005212			TST141:	INC (R2)	UPDATE TEST NUMBER	<=====	
012074	022712	000141		CMP	#141,(R2)	SEQUENCE ERROR?	<=====	
012100	001034			BNE	TST142-10	BR TO ERROR HALT ON SEQ ERROR	<=====	
1928	012102	005000		CLR	R0	R0=0	<=====	
1929	012104	005010		CLR	(R0)	LOC 0=0	<=====	
1930	012106	052710	100000	BIS	#100000,(R0)	LOC. 0=100000	<=====	
1931	012112	052700	000402	BIS	#402,R0	R0=2	<=====	
1932	012116	000277		SCC		SET ALL COND. CODE BITS	<=====	
1933	012120	032750	100000	BIT	#100000,a-(R0)	TRY DOPNM W/MODE 5	<=====	
1934	012124	102403		BVS	DNM5A	BR TO ERROR IF V-BIT SET	<=====	
1935	012126	103002		BCC	DNM5A	BR TO ERROR IF C-BIT CLEAR	<=====	
1936	012130	001401		BEQ	DNM5A	BR TO ERROR IF Z-BIT SET	<=====	
1937	012132	100404		BMI	DNM5B			
						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 762	<=====	
							<=====	
							<=====	
012134				DNM5A:				
012134	012742	000271		MOV	#271,-(R2)	MOVE TO MAILBOX # ***** 271 ***** SET MSGTYP TO FATAL ERROR	<=====	
012140	005242			INC	-(R2)			
012142	000000			HALT		COND. CODES INCORRECT	<=====	
1938	012144	022700	000400	DNM5B:	CMP #400,R0	CHECK DEST. REGISTER	<=====	
1939	012150	001404		BEQ	DNM5C			
						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 753	<=====	
							<=====	
							<=====	
012152	012742	000272		MOV	#272,-(R2)	MOVE TO MAILBOX # ***** 272 ***** SET MSGTYP TO FATAL ERROR	<=====	
012156	005242			INC	-(R2)			
012160	000000			HALT		DEST. REGISTER NOT DECREMENTED BY 2	<=====	
1940	012162	022737	100000	000000	DNM5C:	CMP #100000,a#0	CHECK DESTINATION DATA	<=====
1941	012170	001404		BEQ	TST142			
						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 743	<=====	
							<=====	
							<=====	
012172	012742	000273		MOV	#273,-(R2)	MOVE TO MAILBOX # ***** 273 ***** SET MSGTYP TO FATAL ERROR	<=====	
012176	005242			INC	-(R2)			
012200	000000			HALT		DEST. DATA INCORRECTLY MODIFIED	<=====	

1942  
 1943

; . OR SEQUENCE ERROR

012202	005212		
012204	022712	000142	
012210	001033		
1944 012212	005000		
1945 012214	005010		
1946 012216	052710	000001	
1947 012222	005100		
1948 012224	032760	000001 000001	
1949 012232	001403		
1950 012234	102402		
1951 012236	103001		
1952 012240	100004		

;\*\*\*\*\* TEST 142 TEST DEST. MODE 6 W/DOP NON-MODIFYING INST.\*\*\*\*\*

TST142: INC	(R2)	;UPDATE TEST NUMBER
CMP	#142, (R2)	;SEQUENCE ERROR?
BNE	TST143-10	;BR TO ERROR HALT ON SEQ ERROR
CLR	R0	;R0=0
CLR	(R0)	;LOC> 0=0
BIS	#1, (R0)	;LOC. 0=1
COM	R0	;R0=-1 C-BIT=1
BIT	#1,1(R0)	;TRY DOPNM W/MODE 6
BEQ	DNM6A	;BR TO ERROR IF Z-BIT SET
BVS	DNM6A	;BR TO ERROR IF V-BIT SET
BCC	DNM6A	;BR TO ERROR IF C-BIT CLEAR
BPL	DNM6B	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 763 <=====

012242			
012242	012742	000274	
012246	005242		
012250	000000		
1953 012252	022700	177777	
1954 012256	001404		

DNM6A:	MOV	#274,-(R2)	MOVE TO MAILBOX # ***** 274 *****
	INC	-(R2)	;SET MSGTYP TO FATAL ERROR
	HALT		;COND CODES INCORRECT
DNM6B:	CMP	#-1,R0	;CHECK DEST. REGISTER
	BEQ	DNM6C	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 754 <=====

012260	012742	000275	
012264	005242		
012266	000000		
1955 012270	022737	000001 000000	DNM6C:
1956 012276	001404		

	MOV	#275,-(R2)	MOVE TO MAILBOX # ***** 275 *****
	INC	-(R2)	;SET MSGTYP TO FATAL ERROR
	HALT		;DEST. REGISTER MODIFIED
	CMP	#1,&#0	;CHECK DEST. DATA
	BEQ	TST143	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 744 <=====

012300	012742	000276	
012304	005242		
012306	000000		

	MOV	#276,-(R2)	MOVE TO MAILBOX # ***** 276 *****
	INC	-(R2)	;SET MSGTYP TO FATAL ERROR
	HALT		;DEST. DATA MODIFIED

; OR SEQUENCE ERROR <=====

1957  
 1958

;\*\*\*\*\* TEST 143 TEST DEST MODE 7 W/DOP NON-MODIFYING INST.\*\*\*\*\*

012310	005212		
012312	022712	000143	
012316	001034		
1959 012320	005000		
1960 012322	005010		
1961 012324	052710	125125	
1962 012330	052700	000001	
1963 012334	132770	000125	000403
1964 012342	102403		

TST143: INC	(R2)	;UPDATE TEST NUMBER
CMP	#143, (R2)	;SEQUENCE ERROR?
BNE	TST144-10	;BR TO ERROR HALT ON SEQ ERROR
CLR	R0	;R0=0
CLR	(R0)	;LOC. 0=0 C-BIT=0
BIS	#125125, (R0)	;LOC. 0=125125
BIS	#1,R0	;R0=1
BITB	#125,&#403(R0)	;TRY DOPNM W/MODE 7
BVS	DNM7A	;BR TO ERROR IF V-BIT SET

1965 012344	100402		BMI	DNM7A	:BR TO ERROR IF N-BIT SET	<=====	
1966 012346	103401		BCS	DNM7A	:BR TO ERROR IF C-BIT SET	<=====	
1967 012350	001404		BEQ	DNM7B	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 762	<=====	
012352		DNM7A:	MOV	#277,-(R2)	:MOVE TO MAILBOX # ***** 277 *****	<=====	
012352	012742	000277	INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====	
012356	005242		HALT		:COND. CODES INCORRECT	<=====	
012360	000000		CMP	#1,R0	:CHECK DEST. REGISTER	<=====	
1968 012362	022700	000001	BEQ	DNM7C	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 753	<=====	
1969 012366	001404		MOV	#300,-(R2)	:MOVE TO MAILBOX # ***** 300 *****	<=====	
012370	012742	000300	INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====	
012374	005242		HALT		:DESTINATION REGISTER MODIFIED	<=====	
1970 012400	022737	125125 000000	DNM7C:	CMP	#125125,a#0	:CHECK DEST. DATA	<=====
1971 012406	001404		BEQ	TST144	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 743	<=====	
012410	012742	000301	MOV	#301,-(R2)	:MOVE TO MAILBOX # ***** 301 *****	<=====	
012414	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====	
012416	000000		HALT		:DEST. DATA INCORRECT	<=====	
1972					: OR SEQUENCE ERROR	<=====	
1973							
1974							
1975					THIS TEST VERIFIES THE MOV DESTINATION MODE 1 INSTRUCTION.		
1976					:DATA IS SET IN R0 USING SOP INSTRUCTIONS AND THEN MOVED TO LOC. 0		
1977					:USING MOV SRC MODE 0, DEST. MODE 1.		
1978							
1979							
012420	005212		TST144:	TEST 144	TEST MOV DESTINATION MODE 1		
012422	022712	000144	INC	(R2)	:UPDATE TEST NUMBER	<=====	
012426	001016		CMP	#144,(R2)	:SEQUENCE ERROR?	<=====	
1980 012430	005000		BNE	TST145-10	:BR TO ERROR HALT ON SEQ ERROR	<=====	
1981 012432	005010		CLR	R0	:R0=0	<=====	
1982 012434	005100		CLR	(R0)	:LOC. 0=0	<=====	
1983 012436	005004		COM	R0	:R0=-1	<=====	
1984 012440	010014		CLR	R4	:R4 POINTS TO LOC. 0	<=====	
1985 012442	102402		MOV	R0,(R4)	:TRY MOVE MODE 0,1	<=====	
1986 012444	001401		BVS	MDM1A	:BR TO ERROR IF V SET	<=====	
1987 012446	100404		BEQ	MDM1A	:BR TO ERROR IF Z SET	<=====	
			BMI	MDM1B	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVF INSTRUCTION WHICH FOLLOWS W/ 767	<=====	
012450	012742	000302	MDM1A:	MOV	#302,-(R2)	:MOVE TO MAILBOX # ***** 302 *****	<=====

012454	005242		INC	- (R2)	: SET MSGTYP TO FATAL ERROR	
012456	000000		HALT		: CONDITION CODE NOT CORRECT	
1988	012460	005704	MDM1B:	TST	R4	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
1989	012462	001404		BEQ	TST145	CONDITIONAL BRANCH INST. AND
					REPLACE THE MOVE INSTRUCTION	
					WHICH FOLLOWS W/ 761	
					<=====	
012464	012742	000303	MOV	#303,-(R2)	: MOVE TO MAILBOX # ***** 303 *****	
012470	005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR	
012472	000000		HALT		: DESTINATION REGISTER INCORRECTLY ALTERED	
					: OR SEQUENCE ERROR	
					<=====	
1990						
1991						
1992						
1993					THIS TEST VERIFIES THE MOV DESTINATION MODE 2 INSTRUCTION.	
1994					DATA IS SET IN R0 USING SOP INSTRUCTIONS AND THEN MOVED	
1995					TO LOCATION 0 USING MOV SRC MODE 0, DEST. MODE 1.	
1996						
1997						
					***** TEST 145 TEST MOV DESTINATION MODE 2 *****	
012474	005212		TST145:	INC	(R2)	: UPDATE TEST NUMBER
012476	022712	000145		CMP	#145,(R2)	: SEQUENCE ERROR?
012502	001025			BNE	TST146-10	: BR TO ERROR HALT ON SEQ ERROR
1998	012504	005000		CLR	R0	: R0=0
1999	012506	005010		CLR	(R0)	: LOC. 0=0
2000	012510	005110		COM	(R0)	: LOC. 0= 1
Z	2001	012512	010020	MOV	R0,(R0)+	: TRY MOVE MODE 0,2
	2002	012514	100402	BMI	MDM2A	: BR TO ERROR IF N SET
	2003	012516	102401	BVS	MDM2A	: BR TO ERROR IF V SET
	2004	012520	001404	BEQ	MDM2B	
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	
					CONDITIONAL BRANCH INST. AND	
					REPLACE THE MOVE INSTRUCTION	
					WHICH FOLLOWS W/ 770	
					<=====	
012522			MDM2A:	MOV	#304,-(R2)	: MOVE TO MAILBOX # ***** 304 *****
012522	012742	000304		INC	-(R2)	: SET MSGTYP TO FATAL ERROR
012526	005242			HALT		: CC'S INCORRECT
012530	000000		MDM2B:	DEC	R0	
2005	012532	005300		DEC	R0	
2006	012534	005300		BEQ	MDM2D	
2007	012536	001404				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
					CONDITIONAL BRANCH INST. AND	
					REPLACE THE MOVE INSTRUCTION	
					WHICH FOLLOWS W/ 761	
					<=====	
012540			MDM2C:	MOV	#305,-(R2)	: MOVE TO MAILBOX # ***** 305 *****
012540	012742	000305		INC	-(R2)	: SET MSGTYP TO FATAL ERROR
012544	005242			HALT		: DESTINATION REGISTER NOT INCREMENTED PROPERLY
012546	000000		MDM2D:	TST	#0	
2008	012550	005737		BEQ	TST146	
2009	012554	001404				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
					CONDITIONAL BRANCH INST. AND	
					REPLACE THE MOVE INSTRUCTION	
					WHICH FOLLOWS W/ 752	
					<=====	

012556 012742 000306  
012562 005242  
012564 000000MOV #306,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 306 \*\*\*\*\*  
INC -(R2) :SET MSGTYP TO FATAL ERROR  
HALT :DESTINATION DATA INCORRECT  
: OR SEQUENCE ERROR2010  
2011  
2012  
2013  
2014  
2015  
2016;\*\*\*\*\* THIS TEST VERIFIES DESTINATION MODE 2 W/MOVB INSTS. TWO DIFFERENT MOV  
;INSTRUCTIONS ARE USED TO MOVE A TEST PATTERN FIRST TO BYTE 0 THEN TO BYTE 1.

;TEST 146 TEST MOV-BYTE DESTINATION MODE 2

012566 005212  
012570 022712 000146  
012574 001046  
2017 012576 005000  
2018 012600 005010  
2019 012602 112720 000125  
2020 012606 102402  
2021 012610 001401  
2022 012612 100004TST146: INC (R2) :UPDATE TEST NUMBER  
CMP #146,(R2) :SEQUENCE ERROR?  
BNE TST147-10 :BR TO ERROR HALT ON SEQ ERROR  
CLR R0 :R0=0  
CLR (R0) :LOC. 0=0  
MOV #125,(R0)+ :TRY DESTINATION MODE 2 W/EVEN BYTE  
BVS MBDM2A :BR TO ERROR IF V SET  
BEQ MBDM2A :BR TO ERROR IF Z SET  
BPL MBDM2B: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
: CONDITIONAL BRANCH INST. AND <=====  
: REPLACE THE MOVE INSTRUCTION <=====  
: WHICH FOLLOWS W/ 770 <=====012614  
012614 012742 000307  
012620 005242  
012622 000000  
2023 012624 022700 000001  
2024 012630 001404MBDM2A:  
MOV #307,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 307 \*\*\*\*\*  
INC -(R2) :SET MSGTYP TO FATAL ERROR  
HALT :CC'S INCORRECT  
MBDM2B: CMP #1,R0  
BEQ MBDM2C: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
: CONDITIONAL BRANCH INST. AND <=====  
: REPLACE THE MOVE INSTRUCTION <=====  
: WHICH FOLLOWS W/ 761 <=====012632 012742 000310  
012636 005242  
012640 000000  
2025 012642 112720 000252  
2026 012646 102402  
2027 012650 001401  
2028 012652 100404MBDM2C:  
MOV #310,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 310 \*\*\*\*\*  
INC -(R2) :SET MSGTYP TO FATAL ERROR  
HALT :REGISTER NOT INCREMENTED BY ONE  
MOV #252,(R0)+ :TRY DESTINATION MODE 2 W/ODD BYTE  
BVS MBDM2D  
BEQ MBDM2D  
BMI MBDM2E: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
: CONDITIONAL BRANCH INST. AND <=====  
: REPLACE THE MOVE INSTRUCTION <=====  
: WHICH FOLLOWS W/ 750 <=====012654 012742 000311  
012660 005242  
012662 000000  
2029 012664 022700 000002  
2030 012670 001404MBDM2D:  
MOV #311,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 311 \*\*\*\*\*  
INC -(R2) :SET MSGTYP TO FATAL ERROR  
HALT :CC'S NOT SET CORRECT  
MBDM2E: CMP #2,R0  
BEQ MBDM2F: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
: CONDITIONAL BRANCH INST. AND <=====  
: REPLACE THE MOVE INSTRUCTION <=====  
: WHICH FOLLOWS W/ 741 <=====



013022	000000		HALT		DESTINATION DATA INCORRECT	
2051	013024	112737	000125	000000	MDM3D: MOVB #125, <sup>a#0</sup>	TRY MOVB DESTINATION MODE 2 EVEN BYTE
2052	013032	022737	125125	000000	CMP #125125, <sup>a#0</sup>	CHECK DATA
2053	013040	001404			BEQ MDM3E	
						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 733 <=====
013042	012742	000317			MOV #317,-(R2)	MOVE TO MAILBOX # ***** 317 *****
013046	005242				INC -(R2)	SET MSGTYP TO FATAL ERROR
013050	000000				HALT	DESTINATION DATA INCORRECT
2054	013052	112737	000525	000001	MDM3E: MOVB #525, <sup>a#1</sup>	TRY MOVB DESTINATION MODE 2 ODD BYTE
2055	013060	022737	052525	000000	CMP #52525, <sup>a#0</sup>	CHECK DATA
2056	013066	001404			BEQ TST150	
						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 720 <=====
013070	012742	000320			MOV #320,-(R2)	MOVE TO MAILBOX # ***** 320 *****
013074	005242				INC -(R2)	SET MSGTYP TO FATAL ERROR
013076	000000				HALT	
2057						
2058						
2059						
2060						THIS TEST VERIFIES THE MOV DESTINATION MODE 4 INSTRUCTION.
2061						SOP INSTRUCTIONS ON R0 ARE USED TO CLEAR TARGET LOCATION 0.
2062						R4 IS USED AS THE MODE 4 ADDRESSING REGISTER, AND
2063						CONDITIONAL BRANCHES ARE USED TO VERIFY THE DATA.
2064						
2065						
						TEST 150 TEST MOV DESTINATION MODE 4
013100	005212				TST150: INC (R2)	UPDATE TEST NUMBER
013102	022712	000150			CMP #150,(R2)	SEQUENCE ERROR?
013106	001026				BNE TST151-10	BR TO ERROR HALT ON SEQ ERROR
2066	013110	005000			CLR R0	R0=0
2067	013112	005010			CLR (R0)	LOC 0=0
2068	013114	012704	000002		MOV #2,R4	R4=2
2069	013120	012744	012345		MOV #12345,-(R4)	TRY MOV DEST. MODE 4
2070	013124	102402			BVS MDM4A	BR TO ERROR IF V-BIT SET
2071	013126	001401			BEQ MDM4A	BR TO ERROR IF Z-BIT SET
2072	013130	100004			BPL MDM4B	
						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766 <=====
013132						
013132	012742	000321			MDM4A: MOV #321,-(R2)	MOVE TO MAILBOX # ***** 321 *****
013136	005242				INC -(R2)	SET MSGTYP TO FATAL ERROR
013140	000000				HALT	CC'S NOT CORRECT
2073	013142	005704			MDM4B: TST R4	CHECK DECREMENTING OF MODE 4 REG.
2074	013144	001404			BEQ MDM4C	
						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 760 <=====
013146	012742	000322			MOV #322,-(R2)	MOVE TO MAILBOX # ***** 322 *****

013152 005242	INC	- (R2)	:SET MSGTYP TO FATAL ERROR
013154 000000	HALT		:DESTINATION MODE REGISTER NOT DECREMENTED BY 2
2075 013156 022710 012345	MDM4C:	CMP #12345, (R0)	:CHECK DESTINATION DATA
2076 013162 001404		BEQ TST151	

2077  
2078  
2079  
2080  
2081  
2082  
2083  
2084  
2085  
2086

THIS TEST VERIFIES THE MOVB DESTINATION MODE 4 INSTRUCTION ON BOTH ODD AND EVEN BYTES. SOP INSTRUCTIONS ON R4 ARE USED TO CLEAR TARGET LOCATION 0. R0 IS USED AS THE MODE 4 ADDRESSING REGISTER, AND CMP AND CONDITIONAL BRANCH INSTRUCTIONS ARE USED TO VERIFY THE DATA.

TEST 151 TEST MOVB DESTINATION MODE 4

	013174	005212
	013176	022712
	013202	001046
2087	013204	005004
2088	013206	005014
2089	013210	012700
2090	013214	112740
2091	013220	020027
2092	013224	001404

```

IST151: INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #151, (R2)    ;SEQUENCE ERROR?
        BNE      TST152-10   ;BR TO ERROR HALT ON SEQ ERROR
        CLR      R4            ;R4=0
        CLR      (R4)          ;LOC. 0=0
        MOV      #2, R0         ;R0 = 2
        MOVB    #125125, -(R0) ;TRY MOVB DEST. MODE 4-ODD BYTE
        CMP      R0, #1         ;CHECK THAT DEST. REG. WAS DECREMENTED

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 766 <=====

013226	012742	000324	
013232	005242		
013234	000000		
2093	013236	021427	052400
2094	013242	001404	

MOV #324,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 324 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;DESTINATION REG. NOT DECREMENTED BY 1  
MBDM4A: CMP (R4),#52400 ;CHECK DEST. DATA

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 757 <=====

	013244	012742	000325
	013250	005242	
	013252	000000	
2095	013254	112740	125125
2096	013260	102402	
2097	013262	001401	
2098	013264	100004	

		WHICH FOLLOWS W/ 757
MOV	#325,-(R2)	:MOVE TO MAILBOX # ***** 325 *****
INC	-(R2)	:SET MSGTYP TO FATAL ERROR
HALT		:DEST. DATA NOT CORRECT
MBDM4B:	MOVB #125125,-(R0)	:TRY MOVB DEST. MODE 4--EVEN BYTE
BVS	MBDM4C	:BR. TO ERROR IF V-BIT SET
BEQ	MBDM4C	:BR TO ERROR IF Z-BIT SET
BPL	MBDM4D	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 746 <=====

013266		MBDM4C:	MOV #326,-(R2)	;MOVE TO MAILBOX # ***** 326 *****	<=====
013266	012742	000326	INC -(R2)	;SET MSGTYP TO FATAL ERROR	<=====
013272	005242		HALT	;COND. CODES INCORRECT	<=====
013274	000000			;CHECK MODE 4 DEST. REGISTER	<=====
2099	013276	005700	TST R0		
2100	013300	001404	BEQ MBDM4E		

013302	012742	000327	MOV #327,-(R2)	;MOVE TO MAILBOX # ***** 327 *****	<=====
013306	005242		INC -(R2)	;SET MSGTYP TO FATAL ERROR	<=====
013310	000000		HALT	;DESTINATION REG NOT DECREMENTED BY 1	<=====
2101	013312	021427	CMP (R4),#52525	;CHECK DEST. DATA	<=====
2102	013316	001404	BEQ TST152		

013320	012742	000330	MOV #330,-(R2)	;MOVE TO MAILBOX # ***** 330 *****	<=====
013324	005242		INC -(R2)	;SET MSGTYP TO FATAL ERROR	<=====
013326	000000		HALT	;DESTINATION DATA INCORRECT	<=====

2103  
2104  
2105  
2106  
2107  
2108  
2109  
2110  
2111  
2112  
2113

\*\*\*\*\*  
 THIS TEST VERIFIES THE MOV DESTINATION MODE 5 AND THE MOVB DESTINATION MODE 5 - EVEN BYTE INSTRUCTIONS. R4 IS A POINTER TO TARGET LOCATION 0 AND R0 IS SETUP TO POINT TO LOCATION 376 FOR THE MOV, AND LOCATION 404 FOR THE MOVB INSTRUCTIONS. CMP INSTRUCTIONS ARE USED TO VERIFY PROPER ADDRESSING AND DATA.

013330	005212		TST152: INC (R2)	;TEST 152 TEST MOV DESTINATION MODE 5	<=====
013332	022712	000152	CMP #152,(R2)	*****	<=====
013336	001051		BNE TST153-10	;UPDATE TEST NUMBER	<=====
2114	013340	005004	CLR R4	;SEQUENCE ERROR?	<=====
2115	013342	005014	CLR (R4)	;BR TO ERROR HALT ON SEQ ERROR	<=====
2116	013344	012700	MOV #400,R0	;R4=0	<=====
2117	013350	012750	MOV #4321,&-(R0)	;LOC. 0 = 0	<=====
2118	013354	102402	BVS MDM5A	;RO=400	<=====
2119	013356	001401	BEQ MDM5A	;TRY MOV DEST. MODE 5	<=====
2120	013360	100004	BPL MDM5B	;BR TO ERROR IF V-BIT SET	<=====

013362				;BR TO ERROR IF Z-BIT SET	<=====
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013362	012742	000331	MDM5A: MOV #331,-(R2)	;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
013366	005242		INC -(R2)	CONDITIONAL BRANCH INST. AND	<=====
013370	000000		HALT	REPLACE THE MOVE INSTRUCTION	<=====

2121	013372	022700	MDM5B: CMP #376,R0	;WHICH FOLLOWS W/ 766	<=====
2122	013376	001404	BEQ MDM5C		

013362					
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2147 013522 100004

BPL MDM6B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 766 <=====

013524 012742 000336  
013524 005242  
013530 000000  
013532 022700 000001

MDM6A:

MOV #336,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 336 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;COND. CODES INCORRECT  
MDM6B: CMP #1,R0 ;CHECK DEST. REGISTER UNALTERED

2150 013540 001404		BEQ	MDM6C	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 757 <=====
013542 012742 000337		MOV	#337,-(R2)	: MOVE TO MAILBOX # ***** 337 ***** <=====
013546 005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR <=====
013550 000000		HALT		: DEST. REGISTER INCORRECTLY ALTERED <=====
2151 013552 022737 052525 000000	MDM6C:	CMP	#52525,a#0	: CHECK DEST. DATA <=====
2152 013560 001404		BEQ	MDM6D	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 747 <=====
013562 012742 000340		MOV	#340,-(R2)	: MOVE TO MAILBOX # ***** 340 ***** <=====
013566 005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR <=====
013570 000000		HALT		: DEST. DATA INCORRECT <=====
2153 013572 012700 000002	177777	MDM6D:	MOV	#2,R0 <=====
2154 013576 112760 000377		MOVB	#377,-1(R0)	: TRY MOVB DEST. MODE 6 <=====
2155 013604 022700 000002		CMP	#2,R0	: CHECK DEST. REGISTER UNALTERED <=====
2156 013610 001404		BEQ	MDM6E	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 733 <=====
013612 012742 000341		MOV	#341,-(R2)	: MOVE TO MAILBOX # ***** 341 ***** <=====
013616 005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR <=====
013620 000000		HALT		: DEST. REGISTER INCORRECTLY ALTERED <=====
2157 013622 022737 177525 000000	MDM6E:	CMP	#177525,a#0	: CHECK DEST. DATA <=====
2158 013630 001404		BEQ	TST154	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 723 <=====
013632 012742 000342		MOV	#342,-(R2)	: MOVE TO MAILBOX # ***** 342 ***** <=====
013636 005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR <=====
013640 000000		HALT		: DEST. DATA INCORRECT <=====
2159				: OR SEQUENCE ERROR <=====
2160				*****
2161				*****
2162				: THIS TEST VERIFIES THE MOV DESTINATION MODE 7 AND MOVB - ODD BYTE
2163				: DESTINATION MODE 7 INSTRUCTIONS. R4 POINTS TO TARGET LOC.0 AND R0
2164				: IS USED AS THE MODE 7 ADDRESSING REGISTER. CMP INSTRUCTIONS ARE
2165				: USED TO VERIFY PROPER ADDRESSING AND DATA.
2166				*****
2167				*****
				: TEST 154 TEST MOV DESTINATION MODE 7
				*****
013642 005212		INC	(R2)	: UPDATE TEST NUMBER
013644 022712 000154		CMP	#154,(R2)	: SEQUENCE ERROR?
013650 001053		BNE	TST155-10	: BR TO ERROR HALT ON SEQ ERROR
2168 013652 005004		CLR	R4	: R4=0
2169 013654 005014		CLR	(R4)	: LOC.0=0
2170 013656 012700 000403	177777	MOV	#403,R0	: R0=403
2171 013662 012770 070707		MOV	#70707,a-1(R0)	: TRY MOV W/DEST MODE 7
2172 013670 102402		BVS	MDM7A	: BR. TO ERROR IF V-BIT SET

2173 013672 001401		BEQ	MDM7A	:BR TO ERROR IF Z-BIT SET	
2174 013674 100004		BPL	MDM7B	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 765	<=====
013676		MDM7A:			
013676 012742 000343		MOV	#343,-(R2)	:MOVE TO MAILBOX # ***** 343 *****	<=====
013702 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
013704 000000		HALT		:COND. CODES INCORRECT	<=====
2175 013706 022700 000403		CMP	#403,R0	:CHECK DEST. REGISTER	<=====
2176 013712 001404		BEQ	MDM7C	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 756	<=====
013714 012742 000344		MOV	#344,-(R2)	:MOVE TO MAILBOX # ***** 344 *****	<=====
013720 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
013722 000000		HALT		:DEST. REGISTER INCORRECTLY ALTERED	<=====
2177 013724 022737 070707 000000	MDM7C:	CMP	#70707,a#0	:CHECK DEST. DATA	
2178 013732 001404		BEQ	MDM7D	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 746	<=====
013734 012742 000345		MOV	#345,-(R2)	:MOVE TO MAILBOX # ***** 345 *****	<=====
013740 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
013742 000000		HALT		:DEST. DATA INCORRECT	<=====
2179 013744 112770 107070 000001	MDM7D:	MOVB	#107070,a1(R0)	:TRY MOVB W/DEST MODE 7--ODD BYTE	
2180 013752 022700 000403		CMP	#403,R0	:CHECK MODE 7 DEST. REG.	
2181 013756 001404		BEQ	MDM7E	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 734	<=====
013760 012742 000346		MOV	#346,-(R2)	:MOVE TO MAILBOX # ***** 346 *****	<=====
013764 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
013766 000000		HALT		:DEST. DATA INCORRECT	<=====
2182 013770 022737 034307 000000	MDM7E:	CMP	#34307,a#0	:CHECK DEST. DATA	
2183 013776 001404		BEQ	TST155	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 724	<=====
014000 012742 000347		MOV	#347,-(R2)	:MOVE TO MAILBOX # ***** 347 *****	<=====
014004 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	<=====
014006 000000		HALT		:DESTINATION DATA INCORRECT	<=====
2184				: OR SEQUENCE ERROR	
2185					
2186					
2187					
2188				THIS TEST VERIFIES MODE 4 DOUBLE OPERAND INSTRUCTIONS.	
2189				THE TEST USES MODE 4 ADDRESSING WITH REGISTER 0 TO MOVE THRU A	
2190				TABLE OF OPERANDS. THE TABLE OF OPERANDS AND THE WORK LOCATION IS	
2191				STORED FOLLOWING THE TEST CODE. A SERIES OF 5 DOP INSTRUCTIONS UTILIZES	
2192				THE DATA IN THE TABLE TO CYCLE THE WORK LOCATION THRU A SET OF	
				VALUE. THE DATA HAS BEEN CHOSEN TO INSURE THAT NO SINGLE ERROR WILL	

\*\*\*\*\*  
 THIS TEST VERIFIES MODE 4 DOUBLE OPERAND INSTRUCTIONS.  
 THE TEST USES MODE 4 ADDRESSING WITH REGISTER 0 TO MOVE THRU A  
 TABLE OF OPERANDS. THE TABLE OF OPERANDS AND THE WORK LOCATION IS  
 STORED FOLLOWING THE TEST CODE. A SERIES OF 5 DOP INSTRUCTIONS UTILIZES  
 THE DATA IN THE TABLE TO CYCLE THE WORK LOCATION THRU A SET OF  
 VALUE. THE DATA HAS BEEN CHOSEN TO INSURE THAT NO SINGLE ERROR WILL

2193 :GO UNDETECTED. WORD AND BYTE INSTRUCTION ACCESSING BOTH EVEN AND  
 2194 :ODD ADDRESSES ARE USED IN THE TEST. THE LISTING SHOWS THE  
 2195 :EXPECTED INTERMEDIATE RESULT AS EACH INSTRUCTION IS EXECUTED.  
 2196  
 2197

\*\*\*\*\*  
 :TEST 155 TEST MODE 4 W/ DOP INSTS.

014010 005212	TST155: INC (R2)	UPDATE TEST NUMBER
014012 022712	CMP #155,(R2)	:SEQUENCE ERROR?
014016 001015	BNE DOP4	:BR TO ERROR HALT ON SEQ ERROR
2198 014020 012700	MOV #TBL1,R0	:INITIALIZE R0
2199 014024 014037	MOV -(R0),@#TBL1	:TBL1=125252
2200 014030 064037	ADD -(R0),@#TBL1	:TBL1=000377
2201 014034 144037	BICB -(R0),@#TBL1	:TBL1=000252
2202 014040 154037	BISB -(R0),@#TBL1+1	:TBL1=125252
2203 014044 024037	CMP -(R0),@#TBL1	:CHECK RESULT
2204 014050 001411	BEQ TST156	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 : CONDITIONAL BRANCH INST. AND <=====  
 : REPLACE THE MOVE INSTRUCTION <=====  
 : WHICH FOLLOWS W/ 762 <=====

014052	DOP4:	MOV #350,-(R2)	MOVE TO MAILBOX # ***** 350 *****
014052 012742	INC -(R2)	:SET MSGTYP TO FATAL ERROR	
014056 005242	HALT	:RESULT OF MODE 4 INSTS. INCORRECT	
014060 000000		: OR SEQUENCE ERROR	

2205		125252	
2206 014062	125252	52652	
2207 014064	052652	53125	
2208 014066	053125	125252	
2209 014070	125252		
2210 014072	000000		

TBL1: 0

2211  
 2212  
 2213  
 2214 : THIS TEST VERIFIES MODE 5 DOUBLE OPERAND INSTRUCTIONS.  
 2215 : THE TEST USES AN ADDRESS TABLE STORED FOLLOWING THE TEST CODE.  
 2216 : THIS TABLE IS SIMPLY A TABLE OF ADDRESS POINTERS WHICH ADDRESS  
 2217 : THE DATA TABLE USED IN THE PREVIOUS TEST. THE TEST IS IDENTICAL TO  
 2218 : THE PREVIOUS TEST EXCEPT THE DATA IS REFERENCED USING THIS ADDRESS  
 2219 : TABLE AND MODE 5 ADDRESSING. (SEE PREVIOUS TEST).  
 2220  
 2221

\*\*\*\*\*  
 :TEST 156 TEST MODE 5 W/ DOP INSTS.

014074 005212	TST156: INC (R2)	UPDATE TEST NUMBER
014076 022712	CMP #156,(R2)	:SEQUENCE ERROR?
014102 001015	BNE DOP5	:BR TO ERROR HALT ON SEQ ERROR
2222 014104 012700	MOV #TBL2+2,R0	:INITIALIZE R0
2223 014110 015037	MOV @-(R0),@#TBL1	:TBL1=125252
2224 014114 065037	ADD @-(R0),@#TBL1	:TBL1=000377
2225 014120 145037	BICB @-(R0),@#TBL1	:TBL1=000252
2226 014124 155037	BISB @-(R0),@#TBL1+1	:TBL1=125252
2227 014130 025037	CMP @-(R0),@#TBL1	:CHECK RESULT
2228 014134 001411	BEQ TST157	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 : CONDITIONAL BRANCH INST. AND <=====

REPLACE THE MOVE INSTRUCTION <=====  
 WHICH FOLLOWS W/ 762 <=====

014136		DOP5:	MOV #351,-(R2)	;MOVE TO MAILBOX #, ***** 351 *****
014136	012742	000351	INC -(R2)	;SET MSGTYP TO FATAL ERROR
014142	005242		HALT	;RESULT OF MODE 5 INSTS. INCORRECT
014144	000000			; OR SEQUENCE ERROR
2229	014146	014062	TBL1-10	
2230	014150	014064	TBL1-6	
2231	014152	014065	TBL1-5	
2232	014154	014066	TBL1-4	
2233	014156	014070	TBL2: TBL1-2	
2234				*****
2235				
2236				THIS TEST VERIFIES MODE 6 DOUBLE OPERAND INSTRUCTIONS.
2237				; IT USES THE SAME DATA AS THAT USED IN THE MODE 4 TESTS.
2238				; THIS TIME THE DATA IS ACCESSED USING MODE 6. R0 IS SET
2239				; TO POINT TO THE MIDDLE OF THE TABLE. THE TABLE IS ACCESSED FROM
2240				; BOTTOM TO TOP BY VARYING THE OFFSET IN THE MODE 6 INSTRUCTIONS.
2241				; THE DATA RESULTS ARE IDENTICAL TO THOSE EXPECTED IN THE MODE 4
2242				; TESTS.
2243				*****
2244				TEST 157 TEST MODE 6 W/ DOP INSTS.
014160	005212	TST157: INC (R2)	;UPDATE TEST NUMBER	
014162	022712	000157 CMP #157,(R2)	;SEQUENCE ERROR?	
014166	001022	BNE TST160-10	;BR TO ERROR HALT ON SEQ ERROR	
2245	014170	012700 014066 MOV #TBL1-4,R0	;INITIALIZE R0	
2246	014174	016037 000002 014072 MOV 2(R0),@#TBL1	;TBL1=125252	
2247	014202	066037 000000 014072 ADD 0(R0),@#TBL1	;TBL1=000377	
2248	014210	146037 177777 014072 BICB -1(R0),@#TBL1	;TBL1=000252	
2249	014216	156037 177776 014073 BISB -2(R0),@#TBL1+1	;TBL1=125252	
2250	014224	026037 177774 014072 CMP -4(R0),@#TBL1	;CHECK RESULT	
2251	014232	001404 BEQ TST160	; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 755	<=====
014234	012742	000352 MOV #352,-(R2)	;MOVE TO MAILBOX #, ***** 352 *****	
014240	005242	INC -(R2)	;SET MSGTYP TO FATAL ERROR	
014242	000000	HALT	;RESULT OF MODE 6 INSTS. INCORRECT	
014242			; OR SEQUENCE ERROR	<=====
2252				*****
2253				
2254				THIS TEST VERIFIES MODE 7 DOUBLE OPERAND INSTRUCTIONS.
2255				; THIS TEST USES THE SAME ADDRESS TABLE AND DATA TABLE USED BY
2256				; THE MODE 5 TESTS. THIS TIME THE DATA IS ACCESSED USING MODE 7.
2257				; R0 IS SET TO POINT TO THE MIDDLE OF THE ADDRESS TABLE IN THE MODE 5
2258				; TEST. THE TABLE IS ACCESSED FROM BOTTOM TO TOP BY VARYING THE OFFSET
2259				; IN THE MODE 7 INSTRUCTIONS. THE DATA RESULTS ARE IDENTICAL TO
2260				; THOSE EXPECTED IN THE MODE 5 TESTS.
2261				*****
2262				TEST 160 TEST MODE 7 W/ DOP INSTS.
014244	005212	TST160: INC (R2)	;UPDATE TEST NUMBER	

014246 022712 000160	CMP #160,(R2)	:SEQUENCE ERROR?	<=====
014252 001022	BNE TST161-10	:BR TO ERROR HALT ON SEQ ERROR	<=====
2263 014254 012700 014152	MOV #TBL2-4,R0	:INITIALIZE R0	<=====
2264 014260 017037 000004 014072	MOV @4(R0),@#TBL1	:TBL1=125252	<=====
2265 014266 067037 000002 014072	ADD @2(R0),@#TBL1	:TBL1=000377	<=====
2266 014274 147037 000000 014072	BICB @0(R0),@#TBL1	:TBL1=000252	<=====
2267 014302 157037 177776 014073	BISB @-2(R0),@#TBL1+1	;TBL1=125252	<=====
2268 014310 027037 177774 014072	CMP @-4(R0),@#TBL1	:CHECK RESULT	<=====
2269 014316 001404	BEQ TST161		
		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 755	<=====
014320 012742 000353	MOV #353,-(R2)	:MOVE TO MAILBOX # ***** 353 *****	<=====
014324 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
014326 000000	HALT	:RESULT OF MODE 7 INSTS INCORRECT : OR SEQUENCE ERROR	<=====
2270	*****		
2271			
2272	THIS TEST VERIFIES THE ROTATE MODE 0 INSTRUCTIONS.		
2273	:R0 IS LOADED WITH A DATA PATTERN, THE C-BIT IS LOADED, AND		
2274	:AN ROL INSTRUCTION IS EXECUTED WITH MODE 0. THE OPERATION IS CHECKED		
2275	:BY TESTING THE RESULTING DATA AND THE STATE OF THE C AND V BITS.		
2276	:NEXT, THE SAME PROCEDURE IS EXECUTED TO TEST MODE 0 BYTE INSTRUCTIONS.		
2277	*****		
2278	TEST 161 TEST ROTATE INSTRUCTIONS OF MODE 0		
014330 005212	TST161: INC (R2)	:UPDATE TEST NUMBER	<=====
014332 022712 000161	CMP #161,(R2)	:SEQUENCE ERROR?	<=====
014336 001026	BNE TST162-10	:BR TO ERROR HALT ON SEQ ERROR	<=====
2279 014340 012700 125252	MOV #125252,R0	:INITIALIZE DATA	<=====
2280 014344 000261	SEC	:SET C-BIT	<=====
2281 014346 006100	ROL RO	:TRY ROL W/ MODE 0	<=====
2282 014350 102004	BVC ROTOA	:CC=0011	<=====
2283 014352 103003	BCC ROTOA		
2284 014354 022700 052525	CMP #052525,R0	:CHECK DATA	<=====
2285 014360 001404	BEQ ROTOB		
		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 766	<=====
014362	ROTOA:		
014362 012742 000354	MOV #354,-(R2)	:MOVE TO MAILBOX # ***** 354 *****	<=====
014366 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
014370 000000	HALT	:ROL MODE 0 FAILED	<=====
2286 014372 012700 125252	ROTOB: MOV #125252,R0	:INITIALIZE DATA	<=====
2287 014376 000261	SEC	:SET C-BIT	<=====
2288 014400 106100	ROLB RO	:TRY ROL W/ MODE 0 EVEN BYTE	<=====
2289 014402 102004	BVC ROTOC	:CC=0011	<=====
2290 014404 103003	BCC ROTOC		
2291 014406 022700 125125	CMP #125125,R0	:CHECK DATA	<=====
2292 014412 001404	BEQ TST162		
		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 751	<=====

014414                    ROTOC:  
 014414 012742 000355            MOV      #355,-(R2)      ;MOVE TO MAILBOX # \*\*\*\*\* 355 \*\*\*\*\*  
 014420 005242            INC      -(R2)      ;SET MSGTYP TO FATAL ERROR  
 014422 000000            HALT                    ;ROLB MODE 0 FAILED  
                           ; OR SEQUENCE ERROR

2293  
2294  
2295  
2296  
2297  
2298  
2299  
2300  
2301  
2302  
2303

;\*\*\*\*\* THIS TEST VERIFIES THE ROTATE MODE 1 INSTRUCTIONS.  
;THE DATA TO BE ROTATED IS IN LOC 0. R0 IS USED AS THE  
;ADDRESSING REGISTER. THE C-BIT IS LOADED AND AN ROL IS EXECUTED.  
;THE RESULTS ARE CHECKED BY COMPARING THE DATA RESULTS AND TESTING  
;THE C AND V BITS. THIS PROCEDURE IS THEN REPEATED TWICE MORE  
;TO TEST THE BYTE ROTATES. FIRST ON BYTE 0, THEN ON BYTE 1.  
;\*\*\*\*\*

## TEST 162    TEST ROTATE INSTRUCTIONS W/ MODE 1

014424	005212		TST162: INC      (R2)      ;UPDATE TEST NUMBER										
- 014426	022712	000162	CMP      #162,(R2)      ;SEQUENCE ERROR?										
014432	001051		BNE      TST163-10      ;BR TO ERROR HALT ON SEQ ERROR										
2304 014434	005000		CLR      R0      ;POINT TO LOC. 0										
2305 014436	012710	052525	MOV      #52525,(R0)      ;INITIALIZE DATA										
2306 014442	000241		CLC                     ;CLEAR C-BIT										
2307 014444	006110		ROL      (R0)      ;TRY ROL W/ MODE 1										
2308 014446	102005		BVC      ROT1A      ;CC=1010										
2309 014450	103404		BCS      ROT1A      ;CHECK RESULT										
2310 014452	023727	000000 125252	CMP      @#0,#125252      ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <td>2311 014460</td> <td>001404</td> <td></td> <td>CONDITIONAL BRANCH INST. AND      ======  <td></td> <td></td> <td>REPLACE THE MOVE INSTRUCTION      ======  <td></td> <td></td> <td>WHICH FOLLOWS W/ 764      ======</td> </td></td>	2311 014460	001404		CONDITIONAL BRANCH INST. AND      ====== <td></td> <td></td> <td>REPLACE THE MOVE INSTRUCTION      ======  <td></td> <td></td> <td>WHICH FOLLOWS W/ 764      ======</td> </td>			REPLACE THE MOVE INSTRUCTION      ====== <td></td> <td></td> <td>WHICH FOLLOWS W/ 764      ======</td>			WHICH FOLLOWS W/ 764      ======

014462		ROT1A:	MOV      #356,-(R2)      ;MOVE TO MAILBOX # ***** 356 *****												
014462	012742	000356	INC      -(R2)      ;SET MSGTYP TO FATAL ERROR												
014466	005242		HALT                    ;ROL MODE 1 FAILED												
014470	000000		ROT1B: SEC                     ;INITIALIZE DATA												
2312 014472	000261		MOV      #125252,(R0)      ;TRY ROLB W/ MODE 1 EVEN BYTE												
2313 014474	012710	125252	ROLB     (R0)      ;CC=1011												
2314 014500	106110		BVC      ROT1C      ;TEST RESULT												
2315 014502	102005		ROT1C: BCC     ROT1C      ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <td>2316 014504</td> <td>103004</td> <td></td> <td>CONDITIONAL BRANCH INST. AND      ======  <td>2317 014506</td> <td>022737</td> <td>125125 000000</td> <td>REPLACE THE MOVE INSTRUCTION      ======  <td>2318 014514</td> <td>001404</td> <td></td> <td>WHICH FOLLOWS W/ 746      ======</td> </td></td>	2316 014504	103004		CONDITIONAL BRANCH INST. AND      ====== <td>2317 014506</td> <td>022737</td> <td>125125 000000</td> <td>REPLACE THE MOVE INSTRUCTION      ======  <td>2318 014514</td> <td>001404</td> <td></td> <td>WHICH FOLLOWS W/ 746      ======</td> </td>	2317 014506	022737	125125 000000	REPLACE THE MOVE INSTRUCTION      ====== <td>2318 014514</td> <td>001404</td> <td></td> <td>WHICH FOLLOWS W/ 746      ======</td>	2318 014514	001404		WHICH FOLLOWS W/ 746      ======

014516		ROT1C:	MOV      #357,-(R2)      ;MOVE TO MAILBOX # ***** 357 *****
014516	012742	000357	INC      -(R2)      ;SET MSGTYP TO FATAL ERROR
014522	005242		HALT                    ;ROLB W/ MODE 1 EVEN BYTE FAILED
014524	000000		ROT1D: MOV      #125252,(R0)      ;POINT TO ODD BYTE
2319 014526	012710	125252	CLR      R0      ;SET C-BIT
2320 014532	005000		INC      R0      ;TRY ROLB W/ MODE 1 ODD BYTE
2321 014534	005200		SEC
2322 014536	000261		ROLB     (R0)
2323 014540	106110		

2324 014542 102005                    BVC      ROT1E      ;CC=0011  
 2325 014544 103004                    BCC      ROT1E      ;  
 2326 014546 022737 052652 000000    CMP      #052652,a#0    ;CHECK DATA  
 2327 014554 001404                    BEQ      TST163     ;  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS        <=====  
; CONDITIONAL BRANCH INST. AND                <=====  
; REPLACE THE MOVE INSTRUCTION                <=====  
; WHICH FOLLOWS W/ 726                        <=====

014556                                ROT1E:  
 014556 012742 000360                MOV      #360,-(R2)    ;MOVE TO MAILBOX # \*\*\*\*\* 360 \*\*\*\*\*  
 014562 005242                        INC      -(R2)        ;SET MSGTYP TO FATAL ERROR  
 014564 000000                        HALT                ;ROLB W/ MODE 1 ODD BYTE FAILED  
; OR SEQUENCE ERROR

2328  
 2329  
 2330  
 2331  
 2332                                ;\*\*\*\*\* THIS TEST VERIFIES MODE 2 ROTATE INSTRUCTIONS.  
 2333                                ;THE SAME PROCEDURE AS IN THE OTHER ROTATE TESTS ARE USED. R0  
 2334                                ;IS USED AS THE ADDRESSING REGISTER AND IS CHECKED FOR PROPER  
 2335                                ;INCREMENTING. BYTE INSTRUCTIONS ARE ALSO CHECKED.  
 2336  
;\*\*\*\*\* TEST 163                        TEST ROTATE INSTRUCTIONS W/ MODE 2  
;\*\*\*\*\*

014566 005212                        TST163: INC      (R2)      ;UPDATE TEST NUMBER  
 014570 022712 000163                CMP      #163,(R2)    ;SEQUENCE ERROR?  
 014574 001057                        BNE      TST164-10    ;BR TO ERROR HALT ON SEQ ERROR  
 2337 014576 005000                   CLR      R0            ;POINT TO LOC 0  
 2338 014600 012710 173737        MOV      #173737,(R0)    ;INITIALIZE DATA  
 2339 014604 000241                   CLC                ;CLEAR C-BIT  
 2340 014606 006120                   ROL      (R0)+        ;TRY ROL W/ MODE 2  
 2341 014610 103007                   BCC      ROT2A        ;CHECK C-BIT  
 2342 014612 022737 167676 000000    CMP      #167676,a#0    ;CHECK DATA  
 2343 014620 001003                   BNE      ROT2A        ;BRANCH IF RESULT INCORRECT  
 2344 014622 005300                   DEC      R0            ;TEST R0  
 2345 014624 005300                   DEC      R0            ;  
 2346 014626 001404                   BEQ      ROT2B        ;  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS        <=====  
; CONDITIONAL BRANCH INST. AND                <=====  
; REPLACE THE MOVE INSTRUCTION                <=====  
; WHICH FOLLOWS W/ 762                        <=====

014630                                ROT2A:  
 014630 012742 000361                MOV      #361,-(R2)    ;MOVE TO MAILBOX # \*\*\*\*\* 361 \*\*\*\*\*  
 014634 005242                        INC      -(R2)        ;SET MSGTYP TO FATAL ERROR  
 014636 000000                        HALT                ;ROL W/ MODE 2 FAILED  
 2347 014640 005000                   CLR      R0            ;POINT TO LOC 0  
 2348 014642 012710 004040        MOV      #4040,(R0)    ;INITIALIZE DATA  
 2349 014646 000241                   CLC                ;CLEAR C-BIT  
 2350 014650 106120                   ROLB     (R0)+        ;TRY ROLB W/ MODE 2 EVEN BYTE  
 2351 014652 103406                   BCS      ROT2C        ;CHECK C-BIT  
 2352 014654 022737 004100 000000    CMP      #4100,a#0    ;CHECK DATA  
 2353 014662 001002                   BNE      ROT2C        ;BRANCH IF DATA INCORRECT  
 2354 014664 005300                   DEC      R0            ;CHECK R0  
 2355 014666 001404                   BEQ      ROT2D        ;  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS        <=====  
; CONDITIONAL BRANCH INST. AND                <=====  
; REPLACE THE MOVE INSTRUCTION                <=====

WHICH FOLLOWS W/ 742 <=====

014670	012742	000362	ROT2C:	MOV #362,-(R2) INC -(R2) HALT	: MOVE TO MAILBOX # ***** 362 ***** : SET MSGTYP TO FATAL ERROR : ROLB W/ MODE 2 EVEN BYTE FAILED	
014674	005242		ROT2D:	CLR R0 MOV #4040,(R0) INC R0 SEC	: POINT TO LOC 0 : INITIALIZE DATA : POINT TO ODD BYTE OF DATA : SET C-BIT	
014676	000000			ROLB (R0)+ BCS ROT2E CMP #10440,&#0 BNE ROT2E DEC R0 DEC R0 BEQ TST164	: TRY ROL W/ MODE 2 ODD BYTE : CHECK C-BIT : CHECK DATA : BRANCH IF DATA INCORRECT : CHECK R0	
2356	014700	005000			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 720 <=====	
2357	014702	012710	004040			
2358	014706	005200				
2359	014710	000261				
2360	014712	106120				
2361	014714	103407				
2362	014716	022737	010440 000000			
2363	014724	001003				
2364	014726	005300				
2365	014730	005300				
2366	014732	001404				
014734	012742	000363	ROT2E:	MOV #363,-(R2) INC -(R2) HALT	: MOVE TO MAILBOX # ***** 363 ***** : SET MSGTYP TO FATAL ERROR : ROLB W/ MODE 2 ODD BYTE FAILED : OR SEQUENCE ERROR	
2367						
2368						
2369						
2370						
2371						
2372						
2373						
2374						
2375						
014744	005212	000164	TST164:	INC (R2) CMP #164,(R2) BNE TST165-10 MOV #52525,&#0 SEC ROL &#0 BCS ROT3A CMP #125253,&#0 BEQ ROT3B	: TEST 164 TEST ROTATE INSTRUCTIONS /W MODE 3 : UPDATE TEST NUMBER : SEQUENCE ERROR? : BR TO ERROR HALT ON SEQ ERROR : INITIALIZE DATA IN LOC 0 : SET C-BIT : TRO ROL W/ MODE 3 : CHECK C-BIT : CHECK DATA	
014746	022712					
014752	001051					
2376	014754	012737	052525 000000			
2377	014762	000261				
2378	014764	006137	000000			
2379	014770	103404				
2380	014772	022737	125253 000000			
2381	015000	001404				
015002	012742	000364	ROT3A:	MOV #364,-(R2) INC -(R2) HALT	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 764 <=====	
015006	005242					
015010	000000					
2382	015012	012737	125252 000000	ROT3B:	MOV #125252,&#0 CLC ROLB &#0 BCC ROT3C	: MOVE TO MAILBOX # ***** 364 ***** : SET MSGTYP TO FATAL ERROR : ROL W/ MODE 3 FAILED : INITIALIZE DATA : CLEAR C-BIT : TRY ROL W/ MODE 3 EVEN BYTE : CHECK C-BIT
2383	015020	000241				
2384	015022	106137	000000			
2385	015026	103004				

2386 015030 023727 000000 125124 4\$: CMP a#0, #125124 ;CHECK DATA  
 2387 015036 001404 BEQ ROT3D ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                                   CONDITIONAL BRANCH INST. AND  
                                   REPLACE THE MOVE INSTRUCTION  
                                   WHICH FOLLOWS W/ 745 <=====  
  
 015040 012742 000365 ROT3C: MOV #365,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 365 \*\*\*\*\*  
 015044 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 015046 000000 HALT ;ROL W/ MODE 3 EVEN BYTE FAILED  
 2388 015050 012737 125252 000000 ROT3D: MOV #125252,a#0 ;INITIALIZE DATA IN LOC. 0  
 2389 015056 000261 SEC ;SET C-BIT  
 2390 015060 106137 000001 ROLB a#1 ;TRY ROL W/ MODE 3 ODD BYTE  
 2391 015064 103004 BCC ROT3E ;CHECK C-BIT  
 2392 015066 022737 052652 000000 CMP #052652,a#0 ;CHECK DATA  
 2393 015074 001404 BEQ TST165 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                                   CONDITIONAL BRANCH INST. AND  
                                   REPLACE THE MOVE INSTRUCTION  
                                   WHICH FOLLOWS W/ 726 <=====  
  
 015076 012742 000366 ROT3E: MOV #366,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 366 \*\*\*\*\*  
 015102 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 015104 000000 HALT ;ROL W/ MODE 3 ODD BYTE FAILED  
                                   ; OR SEQUENCE ERROR  
  
 2394  
 2395  
 2396  
 2397  
 2398 THIS TEST VERIFIES MODE 4 ROTATE INSTRUCTIONS. THE DATA IS  
 2399 STORED IN LOC. 0. R0 IS SET TO 2 AND THE CARRY IS SET. AN ROL MODE 4  
 2400 IS USED TO ROTATE LOCATION 0 USING R0. THE DATA IS CHECKED  
 2401 AND THE C AND V BITS ARE TESTED. THE PROPER DECREMENTING OF  
 2402 R0 IS VERIFIED.  
 2403  
 :TEST 165 TEST MODE 4 W/ ROTATE INSTRUCTIONS  
  
 015106 005212 TST165: INC (R2) ;UPDATE TEST NUMBER  
 015110 022712 000165 CMP #165,(R2) ;SEQUENCE ERROR?  
 015114 001016 BNE TST166-10 ;BR TO ERROR HALT ON SEQ ERROR  
 2404 015116 012737 070707 000000 MOV #070707,a#0 ;INITIALIZE DATA IN LOC. 0  
 2405 015124 012700 000002 MOV #2,R0 ;INITIALIZE R0 AS POINTER  
 2406 015130 000261 SEC ;SET C-BIT  
 2407 015132 006140 ROL -(R0) ;TRY ROL W/ MODE 4  
 2408 015134 103406 BCS ROT4 ;CHECK C-BIT  
 2409 015136 022737 161617 000000 CMP #161617,a#0 ;CHECK DATA  
 2410 015144 001002 BNE ROT4 ;BRANCH IF DATA INCORRECT  
 2411 015146 005700 TST R0 ;CHECK MODE 4 REGISTER  
 2412 015150 001404 BEQ TST166 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                                   CONDITIONAL BRANCH INST. AND  
                                   REPLACE THE MOVE INSTRUCTION  
                                   WHICH FOLLOWS W/ 761 <=====  
  
 015152 012742 000367 ROT4: MOV #367,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 367 \*\*\*\*\*  
 015156 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 015160 000000 HALT ;ROL MODE 4 FAILED

; OR SEQUENCE ERROR

2413  
2414  
2415  
2416  
2417  
2418  
2419  
2420  
2421  
2422  
2423  
2424

\*\*\*\*\* THIS TEST VERIFIES MODE 5 ROTATE INSTRUCTIONS.  
THE DATA IS STORED IN A WORK LOCATION (ROTX) AT THE END OF THE  
TEST CODE. LOC. 0 IS LOADED WITH THE ADDRESS OF THE DATA (ROTX).  
R0 IS SET TO 2. THE CARRY IS CLEARED AND A MODE 5 ROL  
IS EXECUTED USING R0 AS AN ADDRESSING REGISTER. THE DATA IS  
CHECKED, THE C AND V BITS TESTED, AND R0 CHECKED FOR PROPER  
DECREMENTING.

\*\*\*\*\* TEST 166 TEST MODE 5 W/ ROTATE INSTRUCTIONS\*\*\*\*\*

015162	005212		TST166: INC (R2)	; UPDATE TEST NUMBER
015164	022712	000166	CMP #166,(R2)	; SEQUENCE ERROR?
015170	001021		BNE ROT5	; BR TO ERROR HALT ON SEQ ERROR
2425 015172	012737	015244 000000	MOV #ROTX,2#0	; MOVE POINTER TO LOC. 0
2426 015200	012700	000002	MOV #2,R0	; SET MODE 5 REG. TO LOC. 0
2427 015204	012767	107070 000032	MOV #107070,ROTX	; INITIALIZE DATA
2428 015212	000241		CLC	; CLEAR C-BIT
2429 015214	006150		ROL @-(R0)	; TRY ROL W/ MODE 5
2430 015216	103006		BCC ROT5	; CHECK C-BIT
2431 015220	022737	016160 015244	CMP #016160,@#ROTX	; CHECK DATA
2432 015226	001002		BNE ROT5	; BRANCH IF DATA INCORRECT
2433 015230	005700		TST R0	; CHECK MODE 5 REGISTER
2434 015232	001405		BEQ TST167	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 756 <=====

015234		ROT5:		
015234	012742	000370	MOV #370,-(R2)	; MOVE TO MAILBOX # ***** 370 *****
015240	005242		INC -(R2)	; SET MSGTYP TO FATAL ERROR
015242	000000		HALT	; ROL MODE 5 FAILED ; OR SEQUENCE ERROR

2435 015244 000000 ROTX: 0

\*\*\*\*\* THIS TEST VERIFIES MODE 6 ROTATE INSTRUCTIONS.  
IT USES THE SAME PROCEDURE AS THE ABOVE TEST EXCEPT THE  
ROTATE INSTRUCTION USES MODE 6 ADDRESSING WITH REGISTER 7.  
THE DATA IS STILL OPERATED ON IN LOC. ROTX (SEE PREVIOUS TEST).

\*\*\*\*\* TEST 167 TEST MODE 6 W/ ROTATE INSTRUCTIONS\*\*\*\*\*

015246	005212		TST167: INC (R2)	; UPDATE TEST NUMBER
015250	022712	000167	CMP #167,(R2)	; SEQUENCE ERROR?
015254	001013		BNE TST170-10	; BR TO ERROR HALT ON SEQ ERROR
2445 015256	012737	125252 015244	MOV #125252,@#ROTX	; INITIALIZE DATA
2446 015264	000261		SEC	; SET C-BIT
2447 015266	006167	177752	ROL ROTX	; TRY ROL W/ MODE 6
2448 015272	103004		BCC ROT6	; CHECK C-BIT
2449 015274	022737	052525 015244	CMP #52525,@#ROTX	; CHECK DATA

2450 015302 001404

BEQ TST170

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 764 <=====

015304  
015304 012742 000371  
015310 005242  
015312 000000

ROT6:

MOV #371,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 371 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;ROL W/ MODE 6 FAILED  
; OR SEQUENCE ERROR

2451  
2452  
2453  
2454  
2455  
2456  
2457  
2458  
2459

;\*\*\*\*\*  
;THIS TEST VERIFIES MODE 7 ROTATE INSTRUCTIONS.  
;THE DATA IS SET IN LOC. ROTX, (SEE PREVIOUS TEST). THE ROL INSTRUCTION  
;ADDRESSES IT INDIRECTLY USING MODE 7 AND INDIRECT ADDRESS LOCATION  
;(ROTXAD) FOLLOWING THE TEST CODE.  
;\*\*\*\*\*

;TEST 170 TEST MODE 7 W/ ROTATE INSTRUCTIONS  
;\*\*\*\*\*

015314 005212  
015316 022712 000170  
015322 001016  
2460 015324 012737 052525 015244  
2461 015332 012737 015244 015370  
2462 015340 000241  
2463 015342 006177 000022  
2464 015346 103404  
2465 015350 023727 015244 125252  
2466 015356 001405

TST170: INC (R2) ;UPDATE TEST NUMBER  
CMP #170,(R2) ;SEQUENCE ERROR?  
BNE ROT7 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #52525,@#ROTX ;INITIALIZE DATA  
MOV #ROTX,@#ROTXAD ;INITIALIZE ADDRESS POINTER  
CLC ;CLEAR C-BIT  
ROL @ROTXAD ;TRY ROL W/ MODE 7  
BCS ROT7 ;CHECK C-BIT  
CMP @ROTX,#125252 ;CHECK DATA  
BEQ TST171

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 761 <=====

015360  
015360 012742 000372  
015364 005242  
015366 000000

ROT7:

MOV #372,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 372 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;ROL W/ MODE 7 FAILED  
; OR SEQUENCE ERROR

2467 015370 000000

ROTXAD: 0

2468  
2469  
2470  
2471  
2472  
2473  
2474  
2475  
2476  
2477

;\*\*\*\*\*  
; THIS TEST VERIFIES MODE 0 SWAB INSTRUCTION. R0 IS SET TO  
; 177400. A SWAB MODE 0 IS EXECUTED AND THE CONDITIONAL BRANCH  
; IS USED TO CHECK THE SIGN OF THE RESULT. ALSO, A COMPARISON  
; IS MADE TO CHECK THE DATA RESULTS.  
;\*\*\*\*\*

;TEST 171 TEST MODE 0 W/ SWAB INST.  
;\*\*\*\*\*

015372 005212  
015374 022712 000171  
015400 001013  
2478 015402 012700 177400

TST171: INC (R2) ;UPDATE TEST NUMBER  
CMP #171,(R2) ;SEQUENCE ERROR?  
BNE TST172-10 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #177400,R0 ;MOVE TEST PATTERN TO R0

T171 TEST MODE 0 W/ SWAB INST.

SEQ 0108

2479 015406 000300  
2480 015410 100404SWAB  
BMIR0  
SBO

;TRY SWAB MODE 0

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 773 <=====015412 012742 000373  
015416 005242  
015420 000000  
2481 015422 022700 000377  
2482 015426 001404MOV  
INC  
HALT  
SBO:  
CMP  
BEQ#373,-(R2)  
-(R2)  
#377,R0  
TST172;MOVE TO MAILBOX # \*\*\*\*\* 373 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;SWAB DID NOT SET CC'S CORRECT  
;CHECK RESULT; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 764 <=====015430 012742 000374  
015434 005242  
015436 000000MOV  
INC  
HALT#374,-(R2)  
-(R2);MOVE TO MAILBOX # \*\*\*\*\* 374 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;RESULT OF SWAB MODE 0 FAILED  
; OR SEQUENCE ERROR2483  
2484  
2485  
2486  
2487  
2488  
2489  
2490  
2491\*\*\*\*\*  
THIS TEST VERIFIES MODE 1 SWAB INSTRUCTION. THE TEST  
PATTERN IS MOVED TO LOC 0. R0 IS CLEARED AND USED AS THE ADDRESSING  
REGISTER IN THE MODE 1 SWAB. THE DATA RESULTS ARE CHECKED WITH  
A COMPARE.015440 005212  
015442 022712 000172  
015446 001011  
2492 015450 012737 125652 000000  
2493 015456 005000  
2494 015460 000310  
2495 015462 022737 125253 000000  
2496 015470 001404TEST 172: TST172: INC  
CMP  
BNE  
MOV  
CLR  
SWAB  
CMP  
BEQ(R2)  
#172,(R2)  
TST173-10  
#125652,a#0  
R0  
(R0)  
#125253,a#0  
TST173;UPDATE TEST NUMBER  
;SEQUENCE ERROR?  
;BR TO ERROR HALT ON SEQ ERROR  
;MOVE TEST PATTERN TO LOC. 0  
;R0=0  
;TRY SWAB MODE 1  
;CHECK RESULT; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 766 <=====015472 012742 000375  
015476 005242  
015500 000000MOV  
INC  
HALT#375,-(R2)  
-(R2);MOVE TO MAILBOX # \*\*\*\*\* 375 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;RESULT OF SWAB MODE 1 FAILED  
; OR SEQUENCE ERROR2497  
2498  
2499  
2500  
2501  
2502  
2503  
2504  
2505  
2506\*\*\*\*\*  
THIS TEST VERIFIES MODE 2 SWAB INSTRUCTION. THE TEST  
PATTERN IS MOVED TO LOC 0. R0 IS CLEARED AND USED AS THE MODE  
2 ADDRESSING REGISTER. THE RESULTS ARE CHECKED WITH A COMPARE.  
R0 IS CHECKED FOR PROPER DECREMENTING.\*\*\*\*\*  
TEST 173 TEST MODE 2 W/ SWAB INST

T172 TEST MODE 1 W/ SWAB INST

SEQ 0109

```

015502 005212      ;*****
015504 022712 000173 TST173: INC   (R2)      ;UPDATE TEST NUMBER
015510 001020      CMP   #173,(R2)    ;SEQUENCE ERROR?
2507 015512 012737 125152 000000 BNE   TST174-10 ;BR TO ERROR HALT ON SEQ ERROR
2508 015520 005000      MOV   #125152,a#0 ;MOVE TEST PATTERN TO LOC. 0
2509 015522 000320      CLR   R0          ;R0=0
2510 015524 022737 065252 000000 SWAB  (R0)+    ;TRY SWAB MODE 2
2511 015532 001404      CMP   #65252,a#0 ;CHECK RESULT
                                BEQ   SB2          ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
                                                ;CONDITIONAL BRANCH INST. AND
                                                ;REPLACE THE MOVE INSTRUCTION
                                                ;WHICH FOLLOWS W/ 766      <=====

015534 012742 000376      MOV   #376,-(R2) ;MOVE TO MAILBOX # ***** 376 *****
015540 005242      INC   -(R2)        ;SET MSGTYP TO FATAL ERROR
015542 000000      HALT          ;RESULT OF SWAB MODE 0 FAILED
2512 015544 162700 000002      SB2: SUB   #2,R0    ;CHECK EFFECT OF REG.
2513 015550 001404      BEQ   TST174      ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
                                                ;CONDITIONAL BRANCH INST. AND
                                                ;REPLACE THE MOVE INSTRUCTION
                                                ;WHICH FOLLOWS W/ 757      <=====

015552 012742 000377      MOV   #377,-(R2) ;MOVE TO MAILBOX # ***** 377 *****
015556 005242      INC   -(R2)        ;SET MSGTYP TO FATAL ERROR
015560 000000      HALT          ;REGISTER VALUE INCORRECT
                                ; OR SEQUENCE ERROR      <=====

2514
2515
2516
2517
2518
2519
2520
2521
2522
2523
                                ;*****
                                ;THIS TEST VERIFIES MODE 3 SWAB INSTRUCTION. THE TEST
                                ;PATTERN IS MOVED TO LOC 0. A MODE 3 SWAB INSTRUCTION IS EXECUTED
                                ;USING R7 AS THE ADDRESSING REGISTER. A COMPARE VERIFIES THE
                                ;DATA RESULTS.
                                ;*****
                                ;TEST 174      TEST MODE 3 W/SWAB INST.
                                ;*****
015562 005212      ;*****
015564 022712 000174 TST174: INC   (R2)      ;UPDATE TEST NUMBER
015570 001011      CMP   #174,(R2)    ;SEQUENCE ERROR?
2524 015572 012737 000377 000000 BNE   TST175-10 ;BR TO ERROR HALT ON SEQ ERROR
2525 015600 000337 000000      MOV   #377,a#0 ;MOVE TEST PATTERN TO LOC. 0
2526 015604 022737 177400 000000 SWAB  a#0       ;TRY SWAB W/ MODE 3
2527 015612 001404      CMP   #177400,a#0 ;CHECK RESULT
                                BEQ   TST175      ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
                                                ;CONDITIONAL BRANCH INST. AND
                                                ;REPLACE THE MOVE INSTRUCTION
                                                ;WHICH FOLLOWS W/ 766      <=====

015614 012742 000400      MOV   #400,-(R2) ;MOVE TO MAILBOX # ***** 400 *****
015620 005242      INC   -(R2)        ;SET MSGTYP TO FATAL ERROR
015622 000000      HALT          ;RESULT OF SWAB INCORRECT
                                ; OR SEQUENCE ERROR      <=====

2528
2529
2530
2531
                                ;*****

```

T174 TEST MODE 3 W/SWAB INST.

SEQ 0110

2532 : THIS TEST VERIFIES MODE 4 SWAB INSTRUCTIONS. THE DATA  
 2533 : IS MOVED TO LOC 0. R0 IS SET TO 2 AND USED AS THE MODE 4 ADDRESSING  
 2534 : REGISTER. THE DATA IS CHECKED WITH A COMPARE AND R0 IS CHECKED  
 2535 : FOR PROPER DECREMENTING.

2536 :\*\*\*\*\*  
 2537 :TEST 175 TEST MODE 4 W/ SWAB INST

015624 005212	015626 022712	000175	TST175: INC (R2)	:UPDATE TEST NUMBER
015626 022712			CMP #175, (R2)	:SEQUENCE ERROR?
015632 001020			BNE TST176-10	:BR TO ERROR HALT ON SEQ ERROR
2538 015634 012737	125652	000000	MOV #125652, @#0	:MOVE TEST PATTERN TO LOC. 0
2539 015642 012700	000002		MOV #2, R0	:SET UP REGISTER POINTER
2540 015646 000340			SWAB -(R0)	:TRY SWAB MODE 4
2541 015650 022737	125253	000000	CMP #125253, @#0	:CHECK RESULT
2542 015656 001404			BEQ SB4	
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====				
: CONDITIONAL BRANCH INST. AND <=====				
: REPLACE THE MOVE INSTRUCTION <=====				
: WHICH FOLLOWS W/ 765 <=====				
015660 012742 000401			MOV #401, -(R2)	:MOVE TO MAILBOX # ***** 401 *****
015664 005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR
015666 000000			HALT	:RESULT OF SWAB INCORRECT
2543 015670 005700			SB4: TST R0	:CHECK EFFECT ON REG.
2544 015672 001404			BEQ TST176	
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====				
: CONDITIONAL BRANCH INST. AND <=====				
: REPLACE THE MOVE INSTRUCTION <=====				
: WHICH FOLLOWS W/ 757 <=====				
015674 012742 000402			MOV #402, -(R2)	:MOVE TO MAILBOX # ***** 402 *****
015700 005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR
015702 000000			HALT	:REGISTER VALUE INCORRECT
				: OR SEQUENCE ERROR

2545 :\*\*\*\*\*  
 2546  
 2547  
 2548  
 2549 :THIS TEST VERIFIES MODE 5 SWAB INSTRUCTION. THE TEST USES  
 2550 :TWO LOCATIONS FOLLOWING THE TEST CODE. SB5XAD HOLDS THE DATA;  
 2551 :SB5XAD IS A POINTER TO THE DATA LOCATION. THE DATA IS MOVED TO  
 2552 :SB5X AND R0 IS SET TO TWO PLUS THE ADDRESS OF SB5XAD. FOLLOWING  
 2553 :THE MODE 5 SWAB SB5X IS CHECKED FOR THE PROPER DATA. R0 IS  
 2554 :CHECKED TO SEE THAT IT WAS DECREMENTED PROPERLY.

2555 :\*\*\*\*\*  
 2556 :TEST 176 TEST MODE 5 W/ SWAB INST.

015704 005212	015706 022712	000176	TST176: INC (R2)	:UPDATE TEST NUMBER
015706 022712			CMP #176, (R2)	:SEQUENCE ERROR?
015712 001021			BNE SB5	:BR TO ERROR HALT ON SEQ ERROR
2557 015714 012700	015772		MOV #SB5XAD+2, R0	:SET UP POINTER TO WORK LOCATION
2558 015720 012767	125125	000040	MOV #125125, SB5X	:MOVE PATTERN TO WORK LOCATION
2559 015726 000350			SWAB @-(R0)	:TRY SWAB MODE 5
2560 015730 022767	052652	000030	CMP #52652, SB5X	:CHECK RESULT
2561 015736 001404			BEQ SB5A	
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====				
: CONDITIONAL BRANCH INST. AND <=====				

T176 TEST MODE 5 W/ SWAB INST.

015740 012742 000403  
 015744 005242  
 015746 000000  
 2562 015750 020027 015770  
 2563 015754 001406

SB5A: MOV #403,-(R2)  
 INC -(R2)  
 HALT  
 CMP R0,#SB5XAD  
 BEQ TST177

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 765  
 MOVE TO MAILBOX # \*\*\*\*\* 403 \*\*\*\*\*  
 SET MSGTYP TO FATAL ERROR  
 RESULT OF SWAB INCORRECT  
 CHECK RESULT OF REG.

&lt;=====

&lt;=====

015756 012742 000404  
 015756 005242  
 015762 000000  
 2564 015766 000000  
 2565 015770 015766  
 2566  
 2567  
 2568  
 2569

SB5: MOV #404,-(R2)  
 INC -(R2)  
 HALT  
 SB5X: 0  
 SB5XAD: SB5X

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 756

&lt;=====

&lt;=====

&lt;=====

&lt;=====

2570  
 2571  
 2572  
 2573  
 2574  
 2575  
 2576  
 2577

\*\*\*\*\*  
 THIS TEST VERIFIES MODE 6 SWAB INSTRUCTION. THIS TEST  
 USES A WORK LOCATION (SB6X) FOLLOWING THE TEST CODE. TEST DATA  
 IS LOADED INTO THE WORK LOCATION. R0, THE ADDRESSING REGISTER  
 IS LOADED WITH 6 LESS THEN THE ADDRESS OF THE WORK LOCATION.  
 THE MODE 6 SWAB IS EXECUTED WITH A +6 OFFSET. THE DATA IS  
 VERIFIED WITH A COMPARE.

015772 005212 000177  
 015774 022712 000177  
 016000 001013  
 2578 016002 012767 125125 000030  
 2579 016010 012700 016032  
 2580 016014 000360 000006  
 2581 016020 022760 052652 000006  
 2582 016026 001405

TST177: INC (R2)  
 CMP #177,(R2)  
 BNE SB6  
 MOV #125125,SB6X  
 MOV #SB6X-6,R0  
 SWAB 6(R0)  
 CMP #52652,6(R0)  
 BEQ TST200

UPDATE TEST NUMBER  
 SEQUENCE ERROR?  
 BR TO ERROR HALT ON SEQ ERROR  
 MOVE PATTERN TO WORK LOCATION  
 MOVE OFFSET POINTER TO R0  
 TRY SWAB W/ MODE 6  
 CHECK RESULT

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 764

&lt;=====

&lt;=====

&lt;=====

&lt;=====

016030 012742 000405  
 016034 005242  
 016036 000000  
 2583 016040 000000  
 2584  
 2585  
 2586  
 2587

SB6: MOV #405,-(R2)  
 INC -(R2)  
 HALT  
 SB6X: 0

MOVE TO MAILBOX # \*\*\*\*\* 405 \*\*\*\*\*  
 SET MSGTYP TO FATAL ERROR  
 RESULT OF SWAB INCORRECT  
 OR SEQUENCE ERROR  
 WORK LOCATION

2588  
 2589  
 2590

\*\*\*\*\*  
 THIS TEST VERIFIES MODE 7 SWAB INSTRUCTION. THIS TEST  
 USES TWO LOCATIONS FOLLOWING THE TEST CODE: A WORK LOCATION  
 (SB7X) AND A POINTER TO THE WORK LOCATION (SB7XAD). DATA IS MOVED

2591 :TO THE WORK LOCATION. R0 IS LOADED WITH 72 LESS THAN THE ADDRESS  
2592 :OF THE ADDRESS POINTER. THE DATA IS SWAB'ED USING A MODE 7  
2593 :INSTRUCTION WITH AN OFFSET OF +72. THE DATA IS VERIFIED WITH A  
2594 :COMPARE.  
2595  
2596

\*\*\*\*\* TEST 200 TEST MODE 7 W/ SWAB INST. \*\*\*\*\*

016042	005212		TST200: INC (R2)	:UPDATE TEST NUMBER	
016044	022712	000200	CMP #200,(R2)	:SEQUENCE ERROR?	
016050	001013		BNE SB7	:BR TO ERROR HALT ON SEQ ERROR	
2597 016052	012767	177400	000030	MOV #177400,SB7X	:MOVE PATTERN TO WORK LOCATION
2598 016060	012700	016020	MOV #SB7XAD-72,R0	:MOVE OFFSET POINTER TO R0	
2599 016064	000370	000072	SWAB @72(R0)	:TRY SWAB MODE 7	
2600 016070	027027	000072	CMP @72(R0),#377	:CHECK RESULTS	
2601 016076	001406		BEQ TST201		

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
: CONDITIONAL BRANCH INST. AND   
: REPLACE THE MOVE INSTRUCTION   
: WHICH FOLLOWS W/ 764   
=====

016100		SB7:	MOV #406,-(R2)	:MOVE TO MAILBOX # ***** 406 *****
016100	012742	000406	INC -(R2)	:SET MSGTYP TO FATAL ERROR
016104	005242		HALT	:RESULT OF SWAB INCORRECT : OR SEQUENCE ERROR
2602 016110	000000	SB7X:	0	:WORK LOCATION
2603 016112	016110	SB7XAD:	SB7X	:POINTER TO WORK LOCATION

2604  
2605  
2606  
2607  
2608 : THIS TEST VERIFIES ALL LEGAL MODES OF THE JMP INSTRUCTION.  
2609 : BECAUSE OF THE NATURE OF THE INSTRUCTION UNDER TEST, THIS TEST  
2610 : UTILIZES SEVERAL DIFFERENT TECHNIQUES. THE CODE IS NOT EXECUTED  
2611 : IN A LINEAR FASHION. THE DIFFERENT MODES ARE EXECUTED IN ORDER  
2612 : FROM 1-7; HOWEVER, THE CODE IS ARRANGED SO THAT CONTROL LEAP  
2613 : FROGS THRU THE TEST CODE. THE ORDER OF APPEARANCE OF THE CODE  
2614 : IS:  
2615 : JMP MODE 1  
2616 : JMP MODE 3  
2617 : JMP MODE 2  
2618 : JMP MODE 4  
2619 : JMP MODE 6  
2620 : JMP MODE 5  
2621 : JMP MODE 7

2622 : AN INTERNAL SEQUENCE TEST (JMPSEQ) IS USED TO INSURE THAT THE  
2623 : JUMPS ARE OCCURRING IN THE PROGRAMMED SEQUENCE.  
2624 : THE TEST IS MADE UP OF SEVERAL BLOCKS OF CODE. EACH CODE  
2625 : BEGINS WITH A LABEL WHICH INDICATES THE MODE BEING EXECUTED IN  
2626 : THAT BLOCK. A SIMPLE PROCEDURE IS FOLLOWED IN EACH BLOCK. FOR  
2627 : EXAMPLE THE CODE BEGINNING AT JMP3 WILL FIRST COMPARE THE RESULTS  
2628 : OF THE PREVIOUS MODE 2 JUMP. (ANY REGISTER CHANGES ARE VERIFIED  
2629 : AND THE SEQUENCE CHECK IS MADE). THEN THE REGISTERS ARE SETUP  
2630 : FOR A MODE 3 JUMP TO THE NEXT TEST BLOCK (HERE, JMP4), THE SEQUENCE  
2631 : CHECKER IS UPDATED AND THE JUMP IS EXECUTED.  
2632 : IF A FAILURE OCCURS, THE SEQUENCE CHECKER WILL ASSIST IN  
2633 : DETERMINING JUST WHICH MODE FAILED. IF THE SEQUENCE IS CORRECT

2634 :THEN THE ERROR DETECTED WAS A MODE FAILURE (E.G. FAILURE OF THE  
 2635 :REGISTER TO BE INCREMENTED IN MODE 2 JUMP.)  
 2636 :  
 2637 :\*\*\*\*\*  
 ;TEST 201 TEST THE JMP INSTRUCTION IN ALL MODES  
 ;\*\*\*\*\*

016114 005212	TST201: INC (R2)	:UPDATE TEST NUMBER	<=====
016116 022712	CMP #201,(R2)	:SEQUENCE ERROR?	<=====
016122 001150	BNE JMPCK+6	:BR TO ERROR HALT ON SEQ ERROR	<=====
2638 016124 005067	CLR JMPSEQ	:ESTABLISH A SEQUENCE CHECKER	<=====
2639 016130 012700	MOV #JMP2,R0	:SET R0=JUMP TARGET	<=====
2640 016134 000110	JMP (R0)	:TRY JMP MODE 1	<=====
2641 016136 022700	JMP3: CMP #.+2,R0	:CHECK RESULT OF MODE 2 JUMP	<=====
2642 016142 001404	BEQ JMP3A	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 767	<=====
016144 012742 000407	MOV #407,-(R2)	:MOVE TO MAILBOX # ***** 407 *****	<=====
016150 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
016152 000000	HALT	:REGISTER VALUE AFTER JMP MODE 2 INCORRECT	<=====
2643 016154 026727	JMP3A: CMP JMPSEQ,#1	:MAKE SURE JMPS ARE IN SEQUENCE: JMPSEQ=1?	<=====
2644 016162 001404	BEQ JMP3B	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 757	<=====
016164 012742 000410	MOV #410,-(R2)	:MOVE TO MAILBOX # ***** 410 *****	<=====
016170 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
016172 000000	HALT	:SHOULD BE HERE FROM JMP MODE 2 ONLY	<=====
2645 016174 012700	JMP3B: MOV #IJMP4,R0	:POINT R0 TO INDIRECT JMP ADDR.	<=====
2646 016200 005267	INC JMPSEQ	:UPDATE SEQUENCE CHECKER	<=====
2647 016204 000130	JMP @R0)+	:TRY JMP MODE 3	<=====
2648 016206 016240	IJMP4: JMP4	:ADDRESS INDIRECT JUMP	<=====
2649 016210 005767	JMP2: TST JMPSEQ	:CHECK THAT JMPS ARE IN SEQUENCE: JMPSEQ=0?	<=====
2650 016214 001404	BEQ JMP2A	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 742	<=====
016216 012742 000411	MOV #411,-(R2)	:MOVE TO MAILBOX # ***** 411 *****	<=====
016222 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
016224 000000	HALT	:SHOULD BE HERE FROM JMP MODE 1 ONLY	<=====
2652 016226 005267	JMP2A: INC JMPSEQ	:UPDATE SEQUENCE CHECKER	<=====
2653 016232 012700	MOV #JMP3,R0	:SET R0=JUMP TARGET	<=====
2654 016236 000120	JMP (R0)+	:TRY A JUMP MODE 2 TO "JMP3"	<=====
2655 016240 022700	JMP4: CMP #IJMP4+2,R0	:CHECK RESULT OF REGISTER IN MODE 3 JUMP	<=====
2656 016244 001404	BEQ JMP4A	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 726	<=====
016246 012742 000412	MOV #412,-(R2)	:MOVE TO MAILBOX # ***** 412 *****	<=====
016252 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
016254 000000	HALT	:REGISTER VALUE AFTER MODE 3 JUMP INCORRECT	<=====
2657 015256 022767	JMP4A: CMP #2,JMPSEQ	:CHECK JUMP SEQUENCE: JMPSEQ=2?	<=====

2658 016264 001404		BEQ	JMP4B	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 716 =====
016266 012742 000413		MOV	#413,-(R2)	: MOVE TO MAILBOX # ***** 413 *****
016272 005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR
016274 000000		HALT		: SHOULD BE ONLY FROM MODE 3 JUMP
2659 016276 012700 016346	JMP4B:	MOV	#JMP5+2,R0	: SET UP POINTER TO JUMP TARGET
2660 016302 005267 000150		INC	JMPSEQ	: UPDATE SEQUENCE CHECKER
2661 016306 000140		JMP	-(R0)	: TRY JUMP MODE 4 TO 'JMP4'
2662				
2663 016310 022767 000004 000140	JMP6:	CMP	#4,JMPSEQ	: CHECK THAT JUMPS ARE IN SEQUENCE: JMPSEQ=4?
2664 016316 001404		BEQ	JMP6A	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 701 =====
016320 012742 000414		MOV	#414,-(R2)	: MOVE TO MAILBOX # ***** 414 *****
016324 005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR
016326 000000		HALT		: SHOULD BE HERE ONLY FROM MODE 5 JUMP
2665 016330 012700 016776	JMP6A:	MOV	#JMP7+376,R0	: SET UP OFFSET POINTER TO JUMP TARGET
2666 016334 005267 000116		INC	JMPSEQ	: UPDATE JUMP SEQUENCE
2667 016340 000160 177402		JMP	-376(R0)	: TRY MODE 6 JUMP
2668				
2669 016344 022767 000003 000104	JMP5:	CMP	#3,JMPSEQ	: CHECK THAT JUMPS ARE IN SEQUENCE: JMPSEQ=3?
2670 016352 001404		BEQ	JMP5A	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 663 =====
016354 012742 000415		MOV	#415,-(R2)	: MOVE TO MAILBOX # ***** 415 *****
016360 005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR
016362 000000		HALT		: SHOULD ONLY BE HERE FROM MODE 4 JUMP
2671 016364 012700 016400	JMP5A:	MOV	#IJMP5+2,R0	: SET UP POINTER TO INDIRECT JUMP ADDR.
2672 016370 005267 000062		INC	JMPSEQ	: UPDATE JUMP SEQUENCE
2673 016374 000150		JMP	@-(R0)	: TRY JUMP MODE 5 TO 'JMP6'
2674 016376 016310	IJMP5:	JMP6		: INDIRECT ADDRESS POINTER
2675				
2676 016400 022767 000005 000050	JMP7:	CMP	#5,JMPSEQ	: CHECK JUMPS IN SEQUENCE: JMPSEQ=5?
2677 016406 001404		BEQ	JMP7A	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 645 =====
016410 012742 000416		MOV	#416,-(R2)	: MOVE TO MAILBOX # ***** 416 *****
016414 005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR
016416 000000		HALT		: SHOULD ONLY BE HERE FROM MODE 6 JUMP
2678 016420 012700 016444	JMP7A:	MOV	#IJMP+10,R0	: SET UP OFFSET POINTER TO INDIRECT ADDR.
2679 016424 005267 000026		INC	JMPSEQ	: UPDATE JUMP SEQUENCE
2680 016430 000170 177770		JMP	@-10(R0)	: TRY MODE 7 JUMP
2681 016434 016436	IJMP:	JMPCK		: INDIRECT ADDRESS
2682				
2683 016436 026727 000014 000006	JMPCK:	CMP	JMPSEQ,#6	: CHECK JUMPS IN SEQUENCE: JMPSEQ
2684 016444 001405		BEQ	TST202	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND =====

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 626 <=====  
 016446 012742 000417 MOV #417,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 417 \*\*\*\*\*  
 016452 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 016454 000000 HALT ;SHOULD ONLY BE HERE FROM MODE 6 JUMP  
 ; OR SEQUENCE ERROR

2685 016456 000000 JMPSEQ: 0

\*\*\*\*\*

THIS TEST VERIFIES ALL LEGAL MODES OF THE JSR INSTRUCTION.  
 THE CONCEPT OF LEAP FROGGING AND SEQUENCE CHECKING (JSRSEQ) IS  
 IDENTICAL TO THAT USED IN JMP TEST (SEE PREVIOUS TEST). EACH  
 BLOCK OF CODE VERIFIES THE PREVIOUS JSR BY CHECKING THE SEQUENCE,  
 CHECKING THAT THE PC WAS SAVED IN THE SPECIFIED REGISTER, CHECKING  
 THAT THE SP WAS DECREMENTED, CHECKING THAT THE REGISTER WAS  
 SAVED ON THE STACK, AND FINALLY CHECKING THAT ANY MODE ADDRESS  
 REGISTER ALTERATIONS (E.G. INCREMENT REGISTER IN MODE 2) WERE  
 SUCCESSFUL. R1 IS USED AS THE REGISTER IN ALL JSR INSTRUCTIONS.  
 IF A FAILURE OCCURS, THE SEQUENCE CHECKER WILL ASSIST IN  
 DETERMINING JUST WHICH MODE FAILED. IF THE SEQUENCE IS CORRECT  
 THEN THE ERROR DETECTED WAS A FUNCTIONAL FAILURE (E.G., INCORRECT  
 REGISTER SAVED).

TEST 202 TEST JSR INSTRUCTION W/ ALL MODES

TST202: INC (R2) ;UPDATE TEST NUMBER  
 CMP #202,(R2) ;SEQUENCE ERROR?  
 BNE JSR0 ;BR TO ERROR HALT ON SEQ ERROR

JSR0: BR JSR1

JSR1: MOV #STBOT,R6 ;SET STACK POINTER  
 MOV #JSR2,R0 ;SET TARGET ADDRESS  
 CLR @#JSRSEQ ;INITIALIZE SEQUENCE CHECKER  
 CLR R1 ;INITIALIZE R1  
 COM R1  
 JSR R1,(R0) ;TRY JSR MODE 1  
 ; TO SCOPE: REPLACE THE MOVE INSTRUCTION FOLLOWING W/ 774 <=====  
 <=====

JSR1A:

MOV #420,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 420 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;JSR MODE 1 FAILED

JSR3: CMP #1,@# JSRSEQ ;CHECK SEQUENCE: JSRSEQ=1?  
 BNE JSR3A ;BRANCH IF OUT OF SEQUENCE  
 CMP R1,#JSR4 ;PROPER PC SAVED?  
 BNE JSR3A ;BRANCH IF PC WRONG  
 CMP #STBOT-2,R6 ;STACK POINTER DECREMENTED?  
 BNE JSR3A ;BRANCH IF SP WRONG  
 CMP #125252,(R6) ;REG SAVED ON STACK?  
 BNE JSR3A ;BRANCH IF REG. NOT SAVED  
 CMP #JSR3+2,R0 ;MODE 2 INCREMENT CORRECT?  
 BEO JSR3B ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====



					WHICH FOLLOWS W/ 644	<=====
016756	012742	000424	JSR6A:	MOV #424,-(R2)	: MOVE TO MAILBOX # ***** 424 *****	
016756	005242			INC -(R2)	; SET MSGTYP TO FATAL ERROR	
016762	000000			HALT	; JSR MODE 5 FAILED	
2758	016766	005237	017106	JSR6B: INC @#JSRSEQ	; UPDATE SEQUENCE CHECKER	
2759	016772	004167	000046	JSR R1,JSR7	; TRY JSR MODE 6	
2760	016776	022767	000003	JSR5: CMP #3,JSRSEQ	; CHECK SEQUENCE: JSRSEQ=3?	
2761	017004	001006		BNE JSR5A	; BRANCH IF OUT OF SEQUENCE	
2762	017006	022701	016732	CMP #JSR6,R1	; PROPER PC SAVED?	
2763	017012	001003		BNE JSR5A	; BRANCH IF PC WRONG	
2764	017014	022700	016776	CMP #JSR5,R0	; CHECK MODE 4 REGISTER	
2765	017020	001404		BEQ JSR5B		
					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	
					CONDITIONAL BRANCH INST. AND	
					REPLACE THE MOVE INSTRUCTION	
					WHICH FOLLOWS W/ 622	
017022	012742	000425	JSR5A:	MOV #425,-(R2)	: MOVE TO MAILBOX # ***** 425 *****	
017022	005242			INC -(R2)	; SET MSGTYP TO FATAL ERROR	
017026	000000			HALT	; JSR MODE 4 MALFUNCTIONED	
2766	017032	005237	017106	JSR5B: INC @#JSRSEQ	; UPDATE SEQUENCE CHECKER	
2767	017036	012700	017104	MOV #JSR6AD+2,R0	; POINT R0 TO TARGET ADDRESS	
2768	017042	004150		JSR R1,@-(R0)	; TRY JSR MODE 5	
2769						
2770	017044	022737	000005	017106 JSR7: CMP #5,@#JSRSEQ	; CHECK SEQUENCE: JSRSEQ=5?	
2771	017052	001003		BNE JSR7A	; BRANCH IF OUT OF SEQUENCE	
2772	017054	022701	016776	CMP #JSR5,R1	; PROPER PC SAVED?	
2773	017060	001404		BEQ JSR7B		
					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	
					CONDITIONAL BRANCH INST. AND	
					REPLACE THE MOVE INSTRUCTION	
					WHICH FOLLOWS W/ 602	
017062	012742	000426	JSR7A:	MOV #426,-(R2)	: MOVE TO MAILBOX # ***** 426 *****	
017062	005242			INC -(R2)	; SET MSGTYP TO FATAL ERROR	
017070	000000			HALT	; JSR MODE 6 FAILED	
2774	017072	005237	017106	JSR7B: INC @#JSRSEQ	; UPDATE SEQUENCE CHECKER	
2775	017076	004177	000002	JSR R1,@JSRCKAD	; TRY JSR MODE 7	
2776						
2777	017102	016732		JSR6AD: JSR6	; MODE 5 TARGET ADDRESS	
2778	017104	017110		JSRCKAD:JSRCK	; MODE 7 TARGET ADDRESS	
2779	017106	000000		JSRSEQ: 0	; SEQUENCE CHECKER	
2780						
2781	017110	022767	000006	177770 JSRCK: CMP #6,JSRSEQ	; CHECK SEQUENCE: JSRSEQ=6?	
2782	017116	001003		BNE JSRCK1	; BRANCH IF OUT OF SEQUENCE	
2783	017120	022701	017102	CMP #JSR6AD,R1	; PROPER PC SAVED?	
2784	017124	001404		BEQ TST203		
					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	
					CONDITIONAL BRANCH INST. AND	
					REPLACE THE MOVE INSTRUCTION	
					WHICH FOLLOWS W/ 560	
017126	012742	000427	JSRCK1:	MOV #427,-(R2)	: MOVE TO MAILBOX # ***** 427 *****	
017126	005242			INC -(R2)	; SET MSGTYP TO FATAL ERROR	
017132	000000			HALT	; JSR MODE 7 MALFUNCTIONED	
017134					; OR SEQUENCE ERROR	

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\*\*\*\*\*  
THIS TEST VERIFIES THE RTS INSTRUCTION. THE STACK POINTER  
IS INITIALIZED AND A TEST PATTERN STORED ON STACK. R0 IS LOADED  
WITH RETURN ADDRESS. AN RTS IS EXECUTED, AND, AT THE TARGET  
ADDRESS, A CHECK IS MADE THAT R0 WAS PROPERLY RESTORED FROM THE  
STACK.

\*\*\*\*\*  
TEST 203 TEST RTS INSTRUCTION  
\*\*\*\*\*

017136	005212	
017140	022712	000203
017144	001016	
2795 017146	012706	001000
2796 017152	012746	052525
2797 017156	012700	017174
2798 017162	000200	

TST203:	INC	(R2)	:UPDATE TEST NUMBER	
	CMP	#203,(R2)	:SEQUENCE ERROR?	
	BNE	TST204-10	:BR TO ERROR HALT ON SEQ ERROR	
	MOV	#STBOT,R6	:INITIALIZE STACK POINTER	
	MOV	#52525,-(R6)	:INITIALIZE TOP OF STACK	
	MOV	#RTS1,R0	:INITIALIZE RETURN REGISTER	
	RTS	R0	:TRY RTS THROUGH R0	
			: TO SCOPE: REPLACE THE MOVE INSTRUCTION <===== FOLLOWING W/ 770 <=====	
2800	017164	012742	000430	MOV #430,-(R2) :MOVE TO MAILBOX # ***** 430 *****
	017170	005242		INC -(R2) :SET MSGTYP TO FATAL ERROR
	017172	000000		HALT :RTS FAILED
2802 017174	022700	052525	RTS1: CMP #52525,R0 :CHECK THAT R0 RESTORED FROM STACK	
2803 017200	001404		BEQ TST204 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <===== CONDITIONAL BRANCH INST. AND <===== REPLACE THE MOVE INSTRUCTION <===== WHICH FOLLOWS W/ 761 <===== : MOVE TO MAILBOX # ***** 431 *****	
017202	012742	000431	MOV #431,-(R2) :MOVE TO MAILBOX # ***** 431 *****	
017206	005242		INC -(R2) :SET MSGTYP TO FATAL ERROR	
017210	000000		HALT :RTS MALFUNCTIONED : OR SEQUENCE ERROR	

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THESE NEXT FOUR TESTS VERIFY THE FUNCTIONING OF A GROUP OF FOUR INSTRUCTIONS. THE GROUP CONSISTS OF THE INSTRUCTIONS: MOV, BIC, BIT, AND BIS. THESE INSTRUCTIONS ARE SIMILAR IN THE WAY THEY EFFECT THE C AND V BITS. THEY ALL LEAVE THE V-BIT CLEAR AND THE C-BIT UNAFFECTED.

THE TEST PROCEDURE IS AS FOLLOWS: THE N, Z, AND V BITS ARE LOADED WITH THE COMPLEMENT OF THE EXPECTED RESULTS, THE C-BIT IS LOADED WITH THE DESIRED RESULT. THE INSTRUCTION IS EXECUTED WITH DIFFERENT DATA PATTERNS AND THE RESULTS ARE VERIFIED WITH A SERIES OF CONDITIONAL BRANCH INSTRUCTIONS. THE DATA IS CHOSEN TO PRODUCT ALL POSSIBLE COMBINATIONS OF THE C AND V BITS.

## \*\*\*\*\* TEST 204 TEST MOV INSTRUCTION \*\*\*\*\*

017212 005212  
017214 022712 000204  
017220 001022  
2820 017222 000277  
2821 017224 000251  
2822 017226 012700 100000  
2823 017232 101402  
2824 017234 102401  
2825 017236 100404

TST204: INC (R2) ;UPDATE TEST NUMBER  
CMP #204, (R2) ;SEQUENCE ERROR?  
BNE TST205-10 ;BR TO ERROR HALT ON SEQ ERROR  
SCC ;CC=0110  
+CLN!CLC  
MOV #100000, R0 ;CC=1000  
BLOS MOV1  
BVS MOV1  
BMI MOV2

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 770 <=====

017240 012742 000432  
017244 005242  
017246 000000  
2826 2827 017250 000277  
2828 017252 000244  
2829 017254 012700 000000  
2830 017260 101002  
2831 017262 102401  
2832 017264 100004

MOV1:  
MOV #432,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 432 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;MOV DID NOT SET CC'S CORRECTLY  
MOV2:  
SCC ;CC=1011  
CLZ  
MOV #0, R0 ;CC=0101  
BHI MOV3 ;C OR Z = 0?  
BVS MOV3 ;V=1?  
BPL TST205

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 755 <=====

017266 012742 000433  
017266 005242  
017272 000000  
2833

MOV3:  
MOV #433,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 433 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;MOV DID NOT SET CC'S CORRECTLY  
; OR SEQUENCE ERROR

017276 005212  
017300 022712 000205  
017304 001024  
2834 017306 012700 100001  
2835 017312 000277

TEST 205 TEST BIT INSTRUCTION  
\*\*\*\*\*  
TST205: INC (R2) ;UPDATE TEST NUMBER  
CMP #205, (R2) ;SEQUENCE ERROR?  
BNE TST206-10 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #100001, R0 ;CC=0110  
SCC

T205 TEST BIT INSTRUCTION

SEQ 0120

2836 017314 000251		+CLN!CLC				
2837 017316 032700	100000	BIT #100000,R0		;CC=1000		
2838 017322 101402		BLOS XBIT1				
2839 017324 102401		BVS XBIT1				
2840 017326 100404		BMI XBIT2				
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766		<=====
017330		XBIT1:				
017330 012742 000434		MOV #434,-(R2)		:MOVE TO MAILBOX # ***** 434 *****		
017334 005242		INC -(R2)		;SET MSGTYP TO FATAL ERROR		
017336 000000		HALT		;BIT DID NOT SET CC'S CORRECTLY		
2841		XBIT2:				
2842 017340 000277		SCC		;CC=1011		
2843 017342 000244		CLZ				
2844 017344 032700	077776	BIT #77776,R0		;CC=0101		
2845 017350 101002		BHI XBIT3				
2846 017352 102401		BVS XBIT3				
2847 017354 100004		BPL TST206				
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 753		<=====
017356		XBIT3:				
017356 012742 000435		MOV #435,-(R2)		:MOVE TO MAILBOX # ***** 435 *****		
017362 005242		INC -(R2)		;SET MSGTYP TO FATAL ERROR		
017364 000000		HALT		;BIT DID NOT SET CC'S CORRECTLY ; OR SEQUENCE ERROR		
2848				***** TEST 206 TEST BIC INSTRUCTION *****		
017366 005212 000206		TST206: INC (R2)		:UPDATE TEST NUMBER		
017370 022712		CMP #206,(R2)		;SEQUENCE ERROR?		
017374 001024		BNE TST207-10		;BR TO ERROR HALT ON SEQ ERROR		
2849 017376 012700	177777	MOV #177777,R0				
2850 017402 000277		SCC		;CC=0110		
2851 017404 000251		+CLN!CLC				
2852 017406 042700	077777	BIC #77777,R0		;CC=1000		
2853 017412 101402		BLOS BIC1				
2854 017414 102401		BVS BIC1				
2855 017416 100404		BMI BIC2				
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766		<=====
017420		BIC1:				
017420 012742 000436		MOV #436,-(R2)		:MOVE TO MAILBOX # ***** 436 *****		
017424 005242		INC -(R2)		;SET MSGTYP TO FATAL ERROR		
017426 000000		HALT		;BIC DID NOT SET CC'S CORRECTLY		
2856 017430 000277		SCC		;CC=1011		
2857 017432 000244		CLZ				
2858 017434 042700	100000	BIC #100000,R0		;CC=0101		
2859 017440 101002		BHI BIC3				
2860 017442 102401		BVS BIC3				
2861 017444 100004		BPL TST207				
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS		<=====

T206 TEST BIC INSTRUCTION

SEQ 0121

CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 753 <=====

017446 012742 000437  
017446 005242 000000  
017452 000000  
017454

BIC3:

MOV #437,-(R2)  
INC -(R2)  
HALT

:MOVE TO MAILBOX # \*\*\*\*\* 437 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:BIC DID NOT SET CC'S CORRECTLY  
:OR SEQUENCE ERROR

2862

:\*\*\*\*\* TEST 207 TEST BIS INSTRUCTION \*\*\*\*\*

017456 005212 000207  
017460 022712 000000  
017464 001025  
2863 017466 005000  
2864 017470 000277  
2865 017472 000251  
2866 017474 052700 000000  
2867 017500 103403  
2868 017502 102402  
2869 017504 100401  
2870 017506 001404

TST207: INC (R2)  
CMP #207,(R2)  
BNE TST210-10  
CLR R0  
SCC  
+CLN!CLC  
BIS #0,R0  
BCS BIS1  
BVS BIS1  
BMI BIS1  
BEQ BIS2

:UPDATE TEST NUMBER  
:SEQUENCE ERROR?  
:BR TO ERROR HALT ON SEQ ERROR  
:R0=0  
:CC=1010  
:CC=0100 R0=0

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
: CONDITIONAL BRANCH INST. AND  
: REPLACE THE MOVE INSTRUCTION  
: WHICH FOLLOWS W/ 766 <=====

017510 012742 000440  
017514 005242  
017516 000000  
2871 017520 000277  
2872 017522 000250  
2873 017524 052700 177777  
2874 017530 103003  
2875 017532 102402  
2876 017534 001401  
2877 017536 100404

BIS1:

MOV #440,-(R2)  
INC -(R2)  
HALT

:MOVE TO MAILBOX # \*\*\*\*\* 440 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:BIS DID NOT SET CC'S CORRECTLY  
:CC=0111

BIS2:

SCC  
CLN  
BIS #177777,R0  
BCC BIS3  
BVS BIS3  
BEQ BIS3  
BMI TST210

:CC=1001

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
: CONDITIONAL BRANCH INST. AND  
: REPLACE THE MOVE INSTRUCTION  
: WHICH FOLLOWS W/ 752 <=====

017540 012742 000441  
017544 005242  
017546 000000

BIS3:

MOV #441,-(R2)  
INC -(R2)  
HALT

:MOVE TO MAILBOX # \*\*\*\*\* 441 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:BIS DID NOT SET CC'S CORRECTLY  
:OR SEQUENCE ERROR

2878  
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:\*\*\*\*\* THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE INC AND  
:DEC INSTRUCTIONS. THESE INSTRUCTIONS BOTH EFFECT THE C AND V  
:BITS THE SAME; THE C-BIT IS LEFT UNCHANGED AND THE V-BIT IS DEPENDENT  
:UPON THE DATA RESULTS. THE SAME PROCEDURE IS USED. THE CONDITION  
:CODE BITS ARE INITIALIZED, THE INSTRUCTION IS EXECUTED AND THE  
:RESULTS ARE VERIFIED WITH A SERIES OF CONDITIONAL BRANCH INSTRUCTIONS.  
:THIS PROCEDURE IS REPEATED WITH SEVERAL DATA PATTERNS TO PRODUCE  
:DIFFERENT COMBINATIONS OF THE C AND V BITS.

T207 TEST BIS INSTRUCTION

SEQ 0122

2889  
2890

017550	005212	
017552	022712	000210
017556	001037	
2891 017560	012700	077777
2892 017564	000257	
2893 017566	000264	
2894 017570	005200	
2895 017572	101402	
2896 017574	100001	
2897 017576	102404	

```

:***** TEST 210 TEST INC INSTRUCTION *****
:TST210: INC (R2) :UPDATE TEST NUMBER
          CMP #210,(R2)
          BNE TST211-10 :SEQUENCE ERROR?
          MOV #077777,RO :BR TO ERROR HALT ON SEQ ERROR
          CCC
          SEZ
          INC R0 :CC=1010 R0=10000
          BLOS INC1
          BPL INC1
          BVS INC2
          : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
          : CONDITIONAL BRANCH INST. AND <=====
          : REPLACE THE MOVE INSTRUCTION <=====
          : WHICH FOLLOWS W/ 767 <=====

017600
017600 012742 000442
017604 005242
017606 000000
2898 017610 052700 077777
2899 017614 000261
2900 017616 000244
2901 017620 005200
2902 017622 100403
2903 017624 102402
2904 017626 103001
2905 017630 001404

INC1:   MOV #442,-(R2) :MOVE TO MAILBOX # ***** 442 *****
          INC -(R2) :SET MSGTYP TO FATAL ERROR
          HALT :INC DID NOT SET CC'S CORRECTLY
          INC2: BIS #77777,RO :R0=177777
          SEC
          CLZ
          INC R0 :CC=0101 R0=0
          BMI INC3
          BVS INC3
          BCC INC3
          BEQ INC4
          : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
          : CONDITIONAL BRANCH INST. AND <=====
          : REPLACE THE MOVE INSTRUCTION <=====
          : WHICH FOLLOWS W/ 752 <=====

017632
017632 012742 000443
017636 005242
017640 000000
2906
2907 017642 000277
2908 017644 000241
2909 017646 005200
2910 017650 101402
2911 017652 100401
2912 017654 100004

INC3:   MOV #443,-(R2) :MOVE TO MAILBOX # ***** 443 *****
          INC -(R2) :SET MSGTYP TO FATAL ERROR
          HALT :INC DID NOT SET CC'S CORRECTLY
          INC4: SCC
          CLC
          INC R0 :CC=1110
          BLOS INC5
          BMI INC5
          BPL TST211
          : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
          : CONDITIONAL BRANCH INST. AND <=====
          : REPLACE THE MOVE INSTRUCTION <=====
          : WHICH FOLLOWS W/ 740 <=====

017656
017656 012742 000444
017662 005242
017664 000000
2913
2914

INC5:   MOV #444,-(R2) :MOVE TO MAILBOX # ***** 444 *****
          INC -(R2) :SET MSGTYP TO FATAL ERROR
          HALT :INC DID NOT SET CC'S CORRECTLY
          : OR SEQUENCE ERROR
          :***** TEST 211 TEST DEC INSTRUCTION *****

```

T210 TEST INC INSTRUCTION

SEQ 0123

017666	005212		TST211: INC (R2)	:UPDATE TEST NUMBER	<=====
017670	022712	000211	CMP #211, (R2)	:SEQUENCE ERROR?	<=====
017674	001051		BNE TST212-10	:BR TO ERROR HALT ON SEQ ERROR	<=====
2915 017676	012700	000002	MOV #2, R0	:R0=2	<=====
2916 017702	000277		SCC	:CC=1111	<=====
2917 017704	005300		DEC R0	:CC=0001 R0=1	<=====
2918 017706	100403		BMI DEC1		
2919 017710	001402		BEQ DEC1		
2920 017712	102401		BVS DEC1		
2921 017714	103404		BCS DEC2		
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 767 <=====					
017716			DEC1: MOV #445, -(R2)	:MOVE TO MAILBOX # ***** 445 *****	<=====
017716	012742	000445	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
017722	005242		HALT	:DEC DID NOT SET CC'S CORRECTLY	<=====
017724	000000		SEC	:CC=1011	<=====
2922 017726	000261		CLZ		
2923 017730	000244		DEC R0	:CC=0101 R0=0	<=====
2924 017732	005300		BHI DEC3		
2925 017734	101002		BMI DEC3		
2926 017736	100401		BVC DEC4		
2927 017740	102004		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 755 <=====		
017742			DEC3: MOV #446, -(R2)	:MOVE TO MAILBOX # ***** 446 *****	<=====
017742	012742	000446	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
017746	005242		HALT	:DEC DID NOT SET CC'S CORRECTLY	<=====
017750	000000		SCC	:CC=0110	<=====
2928 017752	000277		+CLN!CLC		
2929 017754	000251		DEC R0	:CC=1000 R0=177777	<=====
2930 017756	005300		BLOS DEC5		
2931 017760	101402		BVS DEC5		
2932 017762	102401		BMI DEC6		
2933 017764	100404		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 743 <=====		
017766			DEC5: MOV #447, -(R2)	:MOVE TO MAILBOX # ***** 447 *****	<=====
017766	012742	000447	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
017772	005242		HALT	:DEC DID NOT SET CC'S CORRECTLY	<=====
017774	000000		SCC	:R0=100000	<=====
2934 017776	042700	077777	BIC #777777, R0	:CC=0101	<=====
2935 020002	000277		+CLN!CLV		
2936 020004	000252		DEC R0	:CC=1011 R0=77777	<=====
2937 020006	005300		BMI DEC7	:CC=0011	<=====
2938 020010	100403		BEQ DEC7		
2939 020012	001402		BVC DEC7		
2940 020014	102001		BCS TST212		
2941 020016	103404		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND <=====		

T211 TEST DEC INSTRUCTION

SEQ 0124

 020020 012742 000450  
 020020 005242  
 020024 000000

DEC7:

 MOV #450,-(R2)  
 INC -(R2)  
 HALT

 : REPLACE THE MOVE INSTRUCTION <=====  
 WHICH FOLLOWS W/ 726 <=====  
 : MOVE TO MAILBOX # \*\*\*\*\* 450 \*\*\*\*\*  
 : SET MSGTYP TO FATAL ERROR  
 : DEC DID NOT SET CC'S CORRECTLY  
 : OR SEQUENCE ERROR

 2942  
 2943  
 2944  
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 2951  
 2952  
 2953

\*\*\*\*\* THESE NEXT THREE TESTS VERIFY THE FUNCTIONING OF THE CLR, TST, AND SWAB INSTRUCTIONS. THESE THREE INSTRUCTIONS ALL LEAVE THE C AND V BITS CLEARED. AGAIN, THE CONDITION CODES ARE PRESET, THE INSTRUCTION EXECUTED AND THE RESULTS CHECKED WITH CONDITIONAL BRANCH INSTRUCTIONS. THE PROCEDURE IS REPEATED TO PRODUCE OTHER COMBINATIONS OF CONDITION CODES.

TEST 212 TEST CLR INSTRUCTION

 020030 005212  
 020032 022712 000212  
 020036 001007  
 2954 020040 000277  
 2955 020042 000244  
 2956 020044 005000  
 2957 020046 100403  
 2958 020050 102402  
 2959 020052 103401  
 2960 020054 001404

 TST212: INC (R2) :UPDATE TEST NUMBER  
 CMP #212,(R2) :SEQUENCE ERROR?  
 BNE TST213-10 :BR TO ERROR HALT ON SEQ ERROR  
 SCC :CC=1011  
 CLZ  
 CLR R0 :CC=0100 R0=0  
 BMI CLR1  
 BVS CLR1  
 BCS CLR1  
 BEQ TST213

 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 CONDITIONAL BRANCH INST. AND <=====  
 REPLACE THE MOVE INSTRUCTION <=====  
 WHICH FOLLOWS W/ 770 <=====>

 020056 012742 000451  
 020056 005242  
 020062 000000

 CLR1: MOV #451,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 451 \*\*\*\*\*  
 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 HALT :CLR DID NOT SET CC'S CORRECTLY  
 : OR SEQUENCE ERROR

 2961  
 2962

TEST 213 TEST TST INSTRUCTION

 020066 005212  
 020070 022712 000213  
 020074 001022  
 2963 020076 000277  
 2964 020100 000244  
 2965 020102 005700  
 2966 020104 100403  
 2967 020106 102402  
 2968 020110 103401  
 2969 020112 001404

 TST213: INC (R2) :UPDATE TEST NUMBER  
 CMP #213,(R2) :SEQUENCE ERROR?  
 BNE TST214-10 :BR TO ERROR HALT ON SEQ ERROR  
 SCC :CC=1011  
 CLZ  
 TST R0 :CC=0100  
 BMI TEST1  
 BVS TEST1  
 BCS TEST1  
 BEQ TEST2

 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 CONDITIONAL BRANCH INST. AND <=====  
 REPLACE THE MOVE INSTRUCTION <=====>

T213 TEST TST INSTRUCTION

SEQ 0125

020114			TEST1:	MOV #452,-(R2)	: WHICH FOLLOWS W/ 770	<=====
020114	012742	000452		INC -(R2)	: MOVE TO MAILBOX # ***** 452 *****	
020120	005242			HALT	: SET MSGTYP TO FATAL ERROR	
020122	000000				: TEST DID NOT SET CC'S CORRECTLY	
2970	020124	005300	TEST2:	DEC R0	: MAKE R0 NEGATIVE	
2971	020126	000277		SCC	: CC=0111	
2972	020130	000250		CLN		
2973	020132	005700		TST R0	: CC=1000	
2974	020134	101402		BLOS TEST3		
2975	020136	102401		BVS TEST3		
2976	020140	100404		BMI TST214		
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
					: CONDITIONAL BRANCH INST. AND	<=====
					: REPLACE THE MOVE INSTRUCTION	<=====
					: WHICH FOLLOWS W/ 755	<=====
020142			TEST3:	MOV #453,-(R2)	: MOVE TO MAILBOX # ***** 453 *****	
020142	012742	000453		INC -(R2)	: SET MSGTYP TO FATAL ERROR	
020146	005242			HALT	: TEST DID NOT SET CC'S CORRECTLY	
020150	000000				: OR SEQUENCE ERROR	
2977				***** TEST 214 *****	TEST SWAB INSTRUCTION	
020152	005212		TST214:	INC (R2)	: UPDATE TEST NUMBER	
020154	022712	000214		CMP #214,(R2)	: SEQUENCE ERROR?	
020160	001023			BNE TST215-10	: BR TO ERROR HALT ON SEQ ERROR	
2978	020162	012700		MOV #170000,R0	: R0=170000	
2979	020166	000277		SCC	: CC=0111	
2980	020170	000250		CLN		
2981	020172	000300		SWAB R0	: CC=1000 R0=360	
2982	020174	101402		BLOS SWB1		
2983	020176	102401		BVS SWB1		
2984	020200	100404		BMI SWB2		
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
					: CONDITIONAL BRANCH INST. AND	<=====
					: REPLACE THE MOVE INSTRUCTION	<=====
					: WHICH FOLLOWS W/ 767	<=====
020202			SWB1:	MOV #454,-(R2)	: MOVE TO MAILBOX # ***** 454 *****	
020202	012742	000454		INC -(R2)	: SET MSGTYP TO FATAL ERROR	
020206	005242			HALT	: SWAB DID NOT SET CC'S CORRECTLY	
020210	000000				: CC=1011	
2985	020212	000277	SWB2:	SCC		
2986	020214	000244		CLZ		
2987	020216	000300		SWAB R0	: CC=0100 R0=170000	
2988	020220	102403		BVS SWB3		
2989	020222	103402		BCS SWB3		
2990	020224	100401		BMI SWB3		
2991	020226	001404		BEQ TST215		
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
					: CONDITIONAL BRANCH INST. AND	<=====
					: REPLACE THE MOVE INSTRUCTION	<=====
					: WHICH FOLLOWS W/ 754	<=====
020230			SWB3:	MOV #455,-(R2)	: MOVE TO MAILBOX # ***** 455 *****	
020230	012742	000455		INC -(R2)	: SET MSGTYP TO FATAL ERROR	
020234	005242			HALT		
020236	000000					

2992  
2993  
2994  
2995  
2996  
2997  
2998  
2999  
3000  
3001  
3002  
3003

THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE ADD AND ADC INSTRUCTIONS. BOTH OF THESE INSTRUCTIONS HANDLE THE C AND V BITS IDENTICALLY. THE PROCEDURE IS TO PRESET THE CONDITION CODES, EXECUTE THE INSTRUCTION WITH A PARTICULAR SET OF DATA, AND THEN CHECK THE RESULTS BY EXECUTING A SERIES OF CONDITIONAL BRANCHES. THIS PROCEDURE IS REPEATED SEVERAL TIMES WITH DIFFERENT DATA TO PRODUCE EVERY COMBINATION OF C AND V BITS.

020240 005212  
020242 022712 000215  
020246 001062  
3004 020250 012700 040000  
3005 020254 000277  
3006 020256 062700 030000  
3007 020262 101402  
3008 020264 102401  
3009 020266 100004

TST215: INC (R2) ;UPDATE TEST NUMBER  
          CMP #215,(R2) ;SEQUENCE ERROR?  
          BNE TST216-10 ;BR TO ERROR HALT ON SEQ ERROR  
          MOV #40000,R0 ;R0=40000  
          SCC ;CC=1111  
          ADD #30000,R0 ;CC=0000 R0=70000  
          BLOS ADD1  
          BVS ADD1  
          BPL ADD2

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 767 <=====

020270 012742 000456  
020270 005242  
020274 000000  
3010 020300 000264  
3011  
3012 020302 062700 010000  
3013 020306 101402  
3014 020310 102001  
3015 020312 100404

ADD1: MOV #456,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 456 \*\*\*\*\*  
          INC -(R2) ;SET MSGTYP TO FATAL ERROR  
          HALT ;ADD DID NOT SET CC'S CORRECTLY  
ADD2: SEZ ;CC=0100  
          ADD #10000,R0 ;CC=1010 40=100000  
          BLOS ADD3  
          BVC ADD3  
          BMI ADD4

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 755 <=====

020314 012742 000457  
020314 005242  
020320 000000  
3016 020324 000257  
3017 020326 000270  
3018 020330 062700 100000  
3019 020334 101002  
3020 020336 102001  
3021 020340 100004

ADD3: MOV #457,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 457 \*\*\*\*\*  
          INC -(R2) ;SET MSGTYP TO FATAL ERROR  
          HALT ;ADD DID NOT SET CC'S CORRECTLY  
ADD4: CCC ;CC=1000  
          SEN  
          ADD #100000,R0 ;CC=0111 R0=0  
          BHI ADD5  
          BVC ADD5  
          BPL ADD6

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 742 <=====

020342 012742 000460

ADD5: MOV #460,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 460 \*\*\*\*\*

020346 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 020350 000000 HALT :ADD DID NOT SET CC'S CORRECTLY  
 3022 020352 062700 177777 ADD6: ADD #177777,R0 ;CC=1000 R0=177777  
 3023 020356 101402 BLOS ADD7  
 3024 020360 102401 BVS ADD7  
 3025 020362 100404 BMI ADD8  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 731 <=====  
 020364 012742 000461 ADD7: MOV #461,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 461 \*\*\*\*\*  
 020370 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 020372 000000 HALT :ADD DID NOT SET CC'S CORRECTLY  
 3026 020374 000277 SCC ;CC=1010  
 3027 020376 000245 +CLC!CLZ  
 3028 020400 062700 000001 ADD #1,R0 ;CC=0101 R=0  
 3029 020404 102403 BVS ADD9  
 3030 020406 103002 BCC ADD9  
 3031 020410 100401 BMI ADD9  
 3032 020412 001404 BEQ TST216  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 715 <=====  
 020414 012742 000462 ADD9: MOV #462,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 462 \*\*\*\*\*  
 020420 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 020422 000000 HALT :ADD DID NOT SET CC'S CORRECTLY  
 ; OR SEQUENCE ERROR  
 3033  
 3034 :\*\*\*\*\*  
 ;TEST 216 TEST ADC INSTRUCTION  
 ;\*\*\*\*\*  
 020424 005212 TST216: INC (R2) :UPDATE TEST NUMBER  
 020426 022712 000216 CMP #216,(R2) :SEQUENCE ERROR?  
 020432 001037 BNE TST217-10 :BR TO ERROR HALT ON SEQ ERROR  
 3035 020434 012700 077777 MOV #077777,R0  
 3036 020440 000277 SCC ;CC=0101  
 3037 020442 000252 +CLN!CLV  
 3038 020444 005500 ADC R0 ;CC=1010  
 3039 020446 101402 BLOS ADC1  
 3040 020450 102001 BVC ADC1  
 3041 020452 100404 BMI ADC2  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 767 <=====  
 020454 012742 000463 ADC1: MOV #463,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 463 \*\*\*\*\*  
 020454 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 020460 000000 HALT :ADC DID NOT SET CC'S CORRECTLY  
 3042 020464 052700 077777 ADC2: BIS #777777,R0 ;CC=1011  
 3043 020470 000277 SCC  
 3044 020472 000244 CLZ  
 3045 020474 005500 ADC R0 ;CC=0101 R0=0  
 3046 020476 101002 BHI ADC3

3047 020500 102401  
3048 020502 100004BVS ADC3  
BPL ADC4; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 753 <=====  
<=====  
<=====  
<=====020504  
020504 012742 000464  
020510 005242  
020512 000000  
3049 020514 000277  
3050 020516 000245  
3051 020520 005500  
3052 020522 102403  
3053 020524 103402  
3054 020526 100401  
3055 020530 001404ADC3:  
MOV #464,-(R2)  
INC -(R2)  
HALT  
SCC  
+CLZ!CLC  
ADC R0  
BVS ADC5  
BCS ADC5  
BMI ADC5  
BEQ TST217;MOVE TO MAILBOX # \*\*\*\*\* 464 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;ADC DID NOT SET CC'S CORRECTLY  
;CC=1010  
;CC=0100; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; W. ICH FOLLOWS W/ 740 <=====  
<=====  
<=====  
<=====020532  
020532 012742 000465  
020536 005242  
020540 000000ADC5:  
MOV #465,-(R2)  
INC -(R2)  
HALT;MOVE TO MAILBOX # \*\*\*\*\* 465 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;ADC DID NOT SET CC'S CORRECTLY  
; OR SEQUENCE ERROR3056  
3057  
3058  
3059  
3060  
3061  
3062  
3063  
3064  
3065  
3066  
3067;\*\*\*\*\*  
; THESE NEXT THREE TESTS VERIFY THE FUNCTIONING OF THE NEG,  
; CMP, AND COM INSTRUCTIONS. EACH OF THESE INSTRUCTIONS GENERATE  
; THE C AND V BITS IDENTICALLY. THE CONDITION CODES ARE PRESET,  
; THE INSTRUCTIONS EXECUTED, AND THE RESULTS CHECKED WITH A SERIES  
; OF CONDITIONAL BRANCH INSTRUCTIONS. THIS PROCEDURE IS REPEATED  
; SEVERAL TIMES WITH DIFFERENT DATA IN ORDER TO GENERATE DIFFERENT  
; COMBINATIONS OF THE C AND V BITS.  
;\*\*\*\*\*020542 005212  
020544 022712 000217  
020550 001042  
3068 020552 012700 000001  
3069 020556 000277  
3070 020560 000251  
3071 020562 005400  
3072 020564 103003  
3073 020566 102402  
3074 020570 001401  
3075 020572 100404TST217: INC (R2) :UPDATE TEST NUMBER  
CMP #217,(R2) :SEQUENCE ERROR?  
BNE TST220-10 :BR TO ERROR HALT ON SEQ ERROR  
MOV #1,R0  
SCC  
+CLN!CLC  
NEG R0 :CC=0110  
BCC NEG1  
BVS NEG1  
BEQ NEG1  
BMI NEG2; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 766 <=====  
<=====  
<=====  
<=====020574  
020574 012742 000466NEG1:  
MOV #466,-(R2)

;MOVE TO MAILBOX # \*\*\*\*\* 466 \*\*\*\*\*

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T217 TEST NEG INSTRUCTION

M 10

SEQ 0129

020600	005242		INC	- (R2)	:SET MSGTYP TO FATAL ERROR
020602	000000		HALT		:NEG DID NOT SET CC'S CORRECTLY
3076	020604	042700	077777	NEG2:	BIC #77777, R0
3077	020610	000257			CCC
3078	020612	000264			SEZ
3079	020614	005400			NEG R0
3080	020616	102003			BVC NEG3
3081	020620	103002			BCC NEG3
3082	020622	001401			BEQ NEG3
3083	020624	100404			BMI NEG4
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 751
					<=====
					<=====
					<=====
					<=====
020626			NEG3:		
020626	012742	000467	MOV	#467,-(R2)	:MOVE TO MAILBOX # ***** 467 *****
020632	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR
020634	000000		HALT		:NEG DID NOT SET CC'S CORRECTLY
3084	020636	005000	NEG4:	CLR R0	:CC=1011
3085	020640	000277		SCC	
3086	020642	000244		CLZ	
3087	020644	005400		NEG R0	:CC=0100 R0=0
3088	020646	102403		BVS NEG5	
3089	020650	103402		BCS NEG5	
3090	020652	001001		BNE NEG5	
3091	020654	100004		BPL TST220	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 735
					<=====
					<=====
					<=====
					<=====
020656			NEG5:		
020656	012742	000470	MOV	#470,-(R2)	:MOVE TO MAILBOX # ***** 470 *****
020662	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR
020664	000000		HALT		:NEG DID NOT SET CC'S CORRECTLY : OR SEQUENCE ERROR
3092					
3093					
020666	005212		TST220:	INC (R2)	:UPDATE TEST NUMBER
020670	022712	000220		CMP #220, (R2)	:SEQUENCE ERROR?
020674	001060			BNE TST221-10	:BR TO ERROR HALT ON SEQ ERROR
3094	020676	012700		MOV #5,R0	:CC=1010
3095	020702	000257		CCC	
3096	020704	000271		+SEN!SEC	
3097	020706	022700		CMP #5,R0	:CC=0101
3098	020712	101002		BHI CMP1	
3099	020714	102401		BVS CMP1	
3100	020716	100004		BPL CMP2	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766
					<=====
					<=====
					<=====
					<=====
020720			CMP1:		
020720	012742	000471	MOV	#471,-(R2)	:MOVE TO MAILBOX # ***** 471 *****
020724	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR
020726	000000		HALT		:CMP DID NOT SET CC'S CORRECTLY

T220 TEST CMP INSTRUCTION

SEQ 0130

3101 020730 012700 100000	CMP2:	MOV #100000,R0 SCC CLV CMP R0,#77777 BLCS CMP3 BVC CMP3 BPL CMP4	:CC=1101 :CC=0010	
3102 020734 000277				<====
3103 020736 000242				<====
3104 020740 020027 077777				<====
3105 020744 101402				<====
3106 020746 102001				<====
3107 020750 100004				<====
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 751	
020752	CMP3:			
020752 012742 000472		MOV #472,-(R2) INC -(R2)	:MOVE TO MAILBOX # ***** 472 ***** :SET MSGTYP TO FATAL ERROR	
020756 005242		HALT	:CMP DID NOT SET CC'S CORRECTLY	
020760 000000	CMP4:	BIS #40000,R0 CCC SEZ CMP #40000,R0	:R0=140000 :CC=0100	
3108 020762 052700 040000		BVC CMP5 BCC CMP5 BEQ CMP5 BMI CMP6	:CC=1011	
3109 020766 000257				
3110 020770 000264				
3111 020772 022700 040000				
3112 020776 102003				
3113 021000 103002				
3114 021002 001401				
3115 021004 100404				
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 733	
021006	CMP5:			
021006 012742 000473		MOV #473,-(R2) INC -(R2)	:MOVE TO MAILBOX # ***** 473 ***** :SET MSGTYP TO FATAL ERROR	
021012 005242		HALT	:CMP DID NOT SET CC'S CORRECTLY	
021014 000000	CMP6:	BIC #40000,R0 SCC CMP #-1,R0	:CC=1111 :CC=0000	
3116 021016 042700 040000		BLOS CMP7 BVS CMP7 BPL TST221		
3117 021022 000277				
3118 021024 022700 177777				
3119 021030 101402				
3120 021032 102401				
3121 021034 100004				
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 717	
021036	CMP7:			
021036 012742 000474		MOV #474,-(R2) INC -(R2)	:MOVE TO MAILBOX # ***** 474 ***** :SET MSGTYP TO FATAL ERROR	
021042 005242		HALT	:CMP DID NOT SET CC'S CORRECTLY	
021044 000000			: OR SEQUENCE ERROR	
3122				
3123				
		***** TEST 221 ***** TEST COM INSTRUCTION		
		***** TEST 221 ***** TEST COM INSTRUCTION		
021046 005212	TST221:	INC (R2)	:UPDATE TEST NUMBER	
021050 022712 000221		CMP #221,(R2)	:SEQUENCE ERROR?	
021054 001010		BNE TST222-10	:BR TO ERROR HALT ON SEQ ERROR	
3124 021056 012700 177777		MOV #-1,R0		
3125 021062 000257		CCC	:CC=1010	
3126 021064 000265		+SEC!SEZ		
3127 021066 005100		COM R0	:CC=0101	

T221 TEST COM INSTRUCTION

SEQ 013<sup>1</sup>
 3128 021070 101002  
 3129 021072 102401  
 3130 021074 100004

 BHI COM1  
 BVS COM1  
 BPL TST222

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 767 <=====

 021076 012742 000475  
 021102 005242  
 021104 000000

COM1:

 MOV #475,-(R2)  
 INC -(R2)  
 HALT

;MOVE TO MAILBOX # \*\*\*\*\* 475 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;COM DID NOT SET CC'S CORRECTLY  
 ; OR SEQUENCE ERROR

 3131  
 3132  
 3133  
 3134  
 3135  
 3136  
 3137  
 3138  
 3139  
 3140  
 3141  
 3142  
 3143

;\*\*\*\*\* THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE SUB  
 ;AND SBC INSTRUCTIONS. BOTH OF THESE INSTRUCTIONS HANDLE THE  
 ;C AND V BITS IDENTICALLY. THE PROCEDURE IS TO PRESET THE CONDITION  
 ;CODES, EXECUTE THE INSTRUCTION WITH A PARTICULAR SET OF DATA, AND  
 ;THEN CHECK THE RESULTS BY EXECUTING A SERIES OF CONDITIONAL  
 ;BRANCHES. THIS PROCEDURE IS REPEATED SEVERAL TIMES WITH DIFFERENT  
 ;DATA PATTERNS TO PROVIDE EVERY COMBINATION OF THE C AND V BITS.

 021106 005212  
 021110 022712 000222  
 021114 001055  
 3144 021116 012700 125252  
 3145 021122 000257  
 3146 021124 000271  
 3147 021126 162700 125252  
 3148 021132 101002  
 3149 021134 102401  
 3150 021136 100004

TST222: INC (R2) ;UPDATE TEST NUMBER  
 CMP #222,(R2) ;SEQUENCE ERROR?  
 BNE TST223-10 ;BR TO ERROR HALT ON SEQ ERROR  
 MOV #125252,R0 ;CC=1010  
 CCC  
 +SEN!SEC  
 SUB #125252,R0 ;CC=0101 R0=0  
 BHI SUB1  
 BVS SUB1  
 BPL SUB2

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 766 <=====

 021140 012742 000476  
 021144 005242  
 021146 000000  
 3151 021150 052700 100000  
 3152 021154 000277  
 3153 021156 000242  
 3154 021160 162700 077777  
 3155 021164 101402  
 3156 021166 102001  
 3157 021170 100004

SUB1: MOV #476,-(R2)  
 INC -(R2)  
 HALT  
 SUB2: BIS #100000,R0  
 SCC  
 CLV  
 SUB #77777,R0 ;CC=0010 R0=1  
 BLOS SUB3  
 BVC SUB3  
 BPL SUB4

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 751 <=====

021172

SUB3:

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C 11

SEQ 0132

021172	012742	000477		MOV #477,-(R2)	;MOVE TO MAILBOX # ***** 477 *****
021176	005242			INC -(R2)	;SET MSGTYP TO FATAL ERROR
021200	000000		SUB4:	HALT	
3158	021202	005100		COM R0	;R0=177777
3159	021204	000277		SCC	;CC=11111
3160					
3161	021206	162700	100000	SUB #100000,R0	;CC=0000 R0=77777
3162	021212	101402		BLOS SUB5	
3163	021214	102401		BVS SUB5	
3164	021216	100004		BPL SUB6	
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 736 <=====
021220			SUB5:	MOV #500,-(R2)	;MOVE TO MAILBOX # ***** 500 *****
021220	012742	000500		INC -(R2)	;SET MSGTYP TO FATAL ERROR
021224	005242			HALT	;SUB DID NOT SET CC'S CORRECTLY
021226	000000		SUB6:	CCC	;CC=0100
3165	021230	000257		SEZ	
3166	021232	000264		SUB #140000,R0	;CC=1011
3167	021234	162700	140000	BVC SUB7	
3168	021240	102003		BCC SUB7	
3169	021242	103002		BEQ SUB7	
3170	021244	001401		BMI TST223	
3171	021246	100404			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 722 <=====
021250			SUB7:	MOV #501,-(R2)	;MOVE TO MAILBOX # ***** 501 *****
021250	012742	000501		INC -(R2)	;SET MSGTYP TO FATAL ERROR
021254	005242			HALT	
021256	000000				
3172					
3173					
					: TEST 223 TEST SBC INSTRUCTION
021260	005212		TST223:	INC (R2)	;UPDATE TEST NUMBER
021262	022712	000223		CMP #223,(R2)	;SEQUENCE ERROR?
021266	001053			BNE TST224-10	;BR TO ERROR HALT ON SEQ ERROR
3174	021270	012700		MOV #1,R0	
3175	021274	000277		SCC	;CC=1011
3176	021276	000244		CLZ	
3177	021300	005600		SBC R0	;CC=0100 R=0
3178	021302	103403		BCS SBC1	
3179	021304	102402		BVS SBC1	
3180	021306	100401		BMI SBC1	
3181	021310	001404		BEQ SBC2	
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766 <=====
021312			SBC1:	MOV #502,-(R2)	;MOVE TO MAILBOX # ***** 502 *****
021312	012742	000502		INC -(R2)	;SET MSGTYP TO FATAL ERROR
021316	005242			HALT	;SBC DID NOT SET CC'S CORRECTLY
021320	000000		SBC2:	SCC	;CC=1010
3182	021322	000277			

3183 021324 000245		+CLZ!CLC			
3184 021326 005600		SBC R0	:CC=0100 R=0		
3185 021330 103403		BCS SBC3			
3186 021332 102402		BVS SBC3			
3187 021334 100401		BMI SBC3			
3188 021336 001404		BEQ SBC4			
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 753	<=====	
021340		SBC3:			
021340 012742 000503		MOV #503,-(R2)	:MOVE TO MAILBOX # ***** 503 *****		
021344 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR		
021346 000000		HALT	:SBC DID NOT SET CC'S CORRECTLY		
3189 021350 000277		SBC4:	:CC=0111		
3190 021352 000250		CLN			
3191 021354 005600		SBC R0	:CC=1001 R0=177777		
3192 021356 103003		BCC SBC5			
3193 021360 102402		BVS SBC5			
3194 021362 001401		BEQ SBC5			
3195 021364 100404		BMI SBC6			
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 740	<=====	
021366		SBC5:			
021366 012742 000504		MOV #504,-(R2)	:MOVE TO MAILBOX # ***** 504 *****		
021372 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR		
021374 000000		HALT	:SBC DID NOT SET CC'S CORRECTLY		
3196 021376 042700 077777		SBC6:	:BIC #777777,R0		
3197 021402 000277		SCC	:R0=100000		
3198 021404 000242		CLV	:CC=1101		
3199 021406 005600		SBC R0	:CC=0010		
3200 021410 101402		BLOS SBC7			
3201 021412 102001		BVC SBC7			
3202 021414 100004		BPL TST224			
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 724	<=====	
021416		SBC7:			
021416 012742 000505		MOV #505,-(R2)	:MOVE TO MAILBOX # ***** 505 *****		
021422 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR		
021424 000000		HALT	:SBC DID NOT SET CC'S CORRECTLY		
			: OR SEQUENCE ERROR		
3203					
3204					
3205					
3206					
3207			THESE NEXT FOUR TESTS VERIFY THE FUNCTIONING OF THE ROL,		
3208			:ROR, ASL AND ASR INSTRUCTIONS. SPECIAL DATA PATTERNS ARE LOADED		
3209			:AND ROTATED SEVERAL TIMES FOR EACH TEST. THE CONDITION CODES		
3210			:ARE PRESET BEFORE EACH ROTATION AND THE CONDITION CODES ARE		
3211			:CHECKED AFTER EACH ROTATION. THE FINAL CHECK IN EACH TEST IS		
3212			:TO VERIFY THE COMMULATIVE DATA RESULT. THE DATA PATTERNS HAVE		
3213			:BEEN SELECTED TO PRODUCE ALL COMBINATIONS OF THE C AND V BITS.		
3214					

T223 TEST SBC INSTRUCTION

SEQ 0134

:TEST 224 TEST ROL INSTRUCTION

\*\*\*\*\*

021426 005212	TST224: INC (R2)	:UPDATE TEST NUMBER
021430 022712	CMP #224, (R2)	:SEQUENCE ERROR?
021434 001053	BNE TST225-10	:BR TO ERROR HALT ON SEQ ERROR
3215 021436 012700	MOV #144000, R0	:R0=144000
3216 021442 000257	CCC	:CC=0110
3217 021444 000266	+SEZ!SEV	
3218 021446 006100	ROL R0	:CC=1001 R0=110000
3219 021450 103003	BCC ROL1	
3220 021452 102402	BVS ROL1	
3221 021454 001401	BEQ ROL1	
3222 021456 100404	BMI ROL2	
		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766 <=====
021460 012742 000506	ROL1: MOV #506,-(R2)	:MOVE TO MAILBOX # ***** 506 *****
021464 005242	INC -(R2)	:SET MSGTYP 10 FATAL ERROR
021466 000000	HALT	
3223 021470 000277	SCC	:CC=1100
3224 021472 000243	+CLV!CLC	
3225 021474 006100	ROL R0	:CC=0011 R0=020000
3226 021476 103003	BCC ROL3	
3227 021500 102002	BVC ROL3	
3228 021502 001401	BEQ ROL3	
3229 021504 100004	BPL ROL4	
		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 753 <=====
021506 012742 000507	ROL3: MOV #507,-(R2)	:MOVE TO MAILBOX # ***** 507 *****
021512 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR
021514 000000	HALT	:ROL DID NOT SET CC'S CORRECTLY
3230 021516 000277	SCC	:CC=0111
3231 021520 000250	CLN	
3232 021522 006100	ROL R0	:CC=0000 R0=040001
3233 021524 101402	BLOS ROL5	
3234 021526 102401	BVS ROL5	
3235 021530 100004	BPL ROL6	
		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 741 <=====
021532 012742 000510	ROL5: MOV #510,-(R2)	:MOVE TO MAILBOX # ***** 510 *****
021536 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR
021540 000000	HALT	:ROL DID NOT SET CC'S CORRECTLY
3236 021542 000257	CCC	:CC=0101
3237 021544 000265	+SEZ!SEC	
3238 021546 006100	ROL R0	:CC=1010 R0=100003
3239 021550 101405	BLOS ROL7	
3240 021552 102004	BVC ROL7	
3241 021554 100003	BPL ROL7	
3242 021556 022700	CMP #100003, R0	

3243 021562 001404

BEQ TST225

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 724 <=====

021564 012742 000511  
021570 005242  
021572 000000

ROL7:

MOV #511,-(R2)  
INC -(R2)  
HALT

;MOVE TO MAILBOX # \*\*\*\*\* 511 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;ROL MALFUNCTIONED  
; OR SEQUENCE ERROR

3244

;\*\*\*\*\* TEST 225 TEST ROR INSTRUCTION \*\*\*\*\*

021574 005212 000225  
021576 022712 000225  
021602 001051 000023  
3245 021604 012700 000023  
3246 021610 000277  
3247 021612 000250  
3248 021614 006000  
3249 021616 102403  
3250 021620 103002  
3251 021622 001401  
3252 021624 100404

TST225: INC (R2)  
CMP #225,(R2)  
BNE TST226-10  
MOV #23,R0  
SCC  
CLN  
ROR R0  
BVS ROR1  
BCC ROR1  
BEQ ROR1  
BMI ROR2

;UPDATE TEST NUMBER  
;SEQUENCE ERROR?  
;BR TO ERROR HALT ON SEQ ERROR  
;R0=23  
;CC=0111  
;CC=1001 R0=100011

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 766 <=====

021626 012742 000512  
021626 005242  
021632 000000  
021634 000000  
3253 021636 000257  
3254 021640 000274  
3255 021642 006000  
3256 021644 102003  
3257 021646 103002  
3258 021650 001401  
3259 021652 100004

ROR1:  
MOV #512,-(R2)  
INC -(R2)  
HALT

ROR2:  
CCC  
+SEN!SEZ  
ROR R0  
BVC ROR3  
BCC ROR3  
BEQ ROR3  
BPL ROR4

;MOVE TO MAILBOX # \*\*\*\*\* 512 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;ROR DID NOT SET CC'S CORRECTLY  
;CC=1100  
;CC=0011 R0=040004

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 753 <=====

021654 012742 000513  
021654 005242  
021660 000000  
021662 000000  
3260 021664 000277  
3261 021666 000241  
3262 021670 006000  
3263 021672 101403  
3264 021674 102402  
3265 021676 001401  
3266 021700 100004

ROR3:  
MOV #513,-(R2)  
INC -(R2)  
HALT

ROR4:  
SCC  
CLC  
ROR R0  
BLOS ROR5  
BVS ROR5  
BEQ ROR5  
BPL ROR6

;MOVE TO MAILBOX # \*\*\*\*\* 513 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;ROR DID NOT SET CC'S CORRECTLY  
;CC=1110  
;CC=0000 R0=020002

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION <=====



3289 022026 000277	ASL4:	SCC	:CC=0111		
3290 022030 000250		CLN			
3291 022032 006300		ASL	R0	:CC=0000 R0=040000	
3292 022034 101402		BLOS	ASL5		
3293 022036 102401		BVS	ASL5		
3294 022040 100004		BPL	ASL6		
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 741 <=====	
022042	ASL5:	MOV #520,-(R2)	:MOVE TO MAILBOX # ***** 520 *****		
022042 012742 000520		INC -(R2)	:SET MSGTYP TO FATAL ERROR		
022046 005242		HALT	:ASL DID NOT SET CC'S CORRECTLY		
022050 000000		CCC	:CC=0101		
3295 022052 000257	ASL6:	+SEZ!SEC			
3296 022054 000265		ASL R0	:CC=1010 R0=100000		
3297 022056 006300		BCS ASL7			
3298 022060 103406		BEO ASL7			
3299 022062 001405		BVC ASL7			
3300 022064 102004		BPL ASL7			
3301 022066 100003		CMP #100000,R0			
3302 022070 022700 100000		BEQ TST227			
3303 022074 001404				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 723 <=====	
022076	ASL7:	MOV #521,-(R2)	:MOVE TO MAILBOX # ***** 521 *****		
022076 012742 000521		INC -(R2)	:SET MSGTYP TO FATAL ERROR		
022102 005242		HALT	:ASL MALFUNCTIONED		
022104 000000			: OR SEQUENCE ERROR		
3304	***** TEST 227 TEST ASR INSTRUCTION *****				
022106 005212	TST227:	INC (R2)	:UPDATE TEST NUMBER		
022110 022712 000227		CMP #227,(R2)	:SEQUENCE ERROR?		
022114 001060		BNE TST230-10	:BR TO ERROR HALT ON SEQ ERROR		
3305 022116 012700 100023		MOV #100023,R0	:R0=100023		
3306 022122 000277		SCC	:CC=0110		
3307 022124 000250		CLN			
3308 022126 006200		ASR R0	:CC=1001 RP=140011		
3309 022130 102403		BVS ASR1			
3310 022132 103002		BCC ASR1			
3311 022134 001401		BEQ ASR1			
3312 022136 100404		BMI ASR2			
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766 <=====	
022140	ASR1:	MOV #522,-(R2)	:MOVE TO MAILBOX # ***** 522 *****		
022140 012742 000522		INC -(R2)	:SET MSGTYP TO FATAL ERROR		
022144 005242		HALT	:ASR DID NOT SET CC'S CORRECTLY		
022146 000000		BIC #100000,R0	:R0=40011		
3313 022150 042700 100000	ASR2:	SCC	:CC=1100		
3314 022154 000277		+CLV!CLC			
3315 022156 000243					

3316 022160 006200		ASR	RO	:CC=0011 RO=020004	
3317 022162 102003		BVC	ASR3		<=====
3318 022164 103002		BCC	ASR3		<=====
3319 022166 001401		BEQ	ASR3		<=====
3320 022170 100004		BPL	ASR4		<=====
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 751	
022172		ASR3:			<=====
022172 012742 000523		MOV	#523,-(R2)	:MOVE TO MAILBOX # ***** 523 *****	
022176 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
022200 000000		HALT		:ASR DID NOT SET CC'S CORRECTLY	
3321 022202 000277		ASR4:	SCC	:CC=1111	
3322					
3323 022204 006200		ASR	RO	:CC=0000 RO=010002	
3324 022206 101403		BLOS	ASR5		
3325 022210 102402		BVS	ASR5		
3326 022212 001401		BEQ	ASR5		
3327 022214 100004		BPL	ASR6		
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 737	
022216		ASR5:			<=====
022216 012742 000524		MOV	#524,-(R2)	:MOVE TO MAILBOX # ***** 524 *****	
022222 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
022224 000000		HALT		:ASR DID NOT SET CC'S CORRECTLY	
3328 022226 052700 100000		ASR6:	BIS #100000,RO	:RO=110002	
3329 022232 000257		CCC		:CC=0101	
3330 022234 000265		+SEZ!SEC			
3331 022236 006200		ASR	RO	:C=1010 RO=144001	
3332 022240 101406		BLOS	ASR7		
3333 022242 102005		BVC	ASR7		
3334 022244 100004		BPL	ASR7		
3335 022246 001403		BEQ	ASR7		
3336 022250 022700 144001		CMP #144001,RO		:CHECK RESULT OF ASR'S	
3337 022254 001404		BEQ	TST230		
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 717	
022256		ASR7:			<=====
022256 012742 000525		MOV	#525,-(R2)	:MOVE TO MAILBOX # ***** 525 *****	
022262 005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
022264 000000		HALT		:ASR DID NOT FUNCTION CORRECTLY	
				; OR SEQUENCE ERROR	
3344					
3345					
3346					
3347					
3348					
3349					
3350					
3351					
3352					
3353					
				***** THIS TEST VERIFIES THE SXT INSTRUCTION. CONDITION CODES ARE PREFSET IN EACH OF THE TWO POSSIBLE CASES. WITH THE N-BIT SET. THE TEST CHECKS FOR ALL ONES IN THE DESTINATION. WITH THE N-BIT CLEAR, THE DESTINATION SHOULD CONTAIN ALL ZEROES. THE DATA IS VERIFIED BY CONDITIONAL BRANCHES.	

3354  
3355

022266	005212	
022270	022712	000230
022274	001033	
3356	022276	005000
3357	022300	000277
3358	022302	000244
3359	022304	006700
3360	022306	100006
3361	022310	001405
3362	022312	102404
3363	022314	103003
3364	022316	022700 177777
3365	022322	001404

```
***** TEST 230 TEST THE SXT INSTRUCTION *****
TST230: INC (R2) ;UPDATE TEST NUMBER
         CMP #230, (R2) ;SEQUENCE ERROR?
         BNE TST231-10 ;BR TO ERROR HALT ON SEQ ERROR
         CLR R0
         SCC
         CLZ
         SXT R0 ;TRY SXT
         BPL SXTO ;TEST CC=1001
         BEQ SXTO
         BVS SXTO
         BCC SXTO
         CMP #-1, R0 ;CHECK DATA RESULT
         BEQ SXTI
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
; CONDITIONAL BRANCH INST. AND <=====
; REPLACE THE MOVE INSTRUCTION <===== WHICH FOLLOWS W/ 764 <=====
```

022324		
022324	012742	000526
022330	005242	
022332	000000	
3366	022334	005000
3367	022336	005010
3368	022340	005110
3369	022342	000257
3370	022344	000266
3371	022346	006710
3372	022350	001005
3373	022352	103404
3374	022354	102403
3375	022356	100402
3376	022360	005710
3377	022362	001404

```
SXTO:
MOV #526,-(R2) ;MOVE TO MAILBOX # ***** 526 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;RESULTS OF SXT INCORRECT
SXT1: CLR R0 ;R0=0
       CLR (R0) ;LOC. 0=0
       COM (R0) ;LOC. 0=177777
       CCC ;SET CC=0110
+SEZ!SEV
SXT (R0)
BNE SXTO ;TEST CC=0100
BCS SXT2
BVS SXT2
BMI SXT2
TST (R0)
BEQ TST231
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
; CONDITIONAL BRANCH INST. AND <=====
; REPLACE THE MOVE INSTRUCTION <===== WHICH FOLLOWS W/ 744 <=====
```

022364		
022364	012742	000527
022370	005242	
022372	000000	

```
SXT2:
MOV #527,-(R2) ;MOVE TO MAILBOX # ***** 527 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;RESULTS OF SXT INCORRECT
; OR SEQUENCE ERROR
```

3378		
3379		
3380		
3381		
3382		
3383		
3384		
3385		
3386		

```
***** THIS TEST VERIFIES THE XOR INSTRUCTION. UNIQUE PATTERNS *****
OF ONES AND ZEROES ARE MOVED TO DATA REGISTERS R0 AND R1.
AFTER THE FIRST XOR INSTRUCTION R0=36146. AN XOR IS THEN
EXECUTED WITH THIS NEW VALUE AND THE CONTENTS OF R1 TO
REPRODUCE THE ORIGINAL VALUE IF R0=31525.
```

```
***** TEST 231 TEST THE XOR INSTRUCTION *****
```

022374 005212	000231	TST231: INC (R2)	:UPDATE TEST NUMBER	
022376 022712	000231	CMP #231, (R2)	:SEQUENCE ERROR?	
022402 001035		BNE TST232-10	:BR TO ERROR HALT ON SEQ ERROR	
3387 022404	012700	007463	MOV #7463,R0	:SET UP R0
3388 022410	012701	031525	MOV #31525,R1	:SET UP R1
3389 022414	000277	SCC	:SET CC=1110	
3390 022416	000241	CLC		
3391 022420	074100	XOR R1,R0	:TRY XOR	
3392 022422	101406	BLOS XOR1	:CC=0000?	
3393 022424	102405	BVS XOR1		
3394 022426	001404	BEQ XOR1		
3395 022430	100403	BMI XOR1		
3396 022432	022700	036146	CMP #36146,R0	:DATA RESULT CORRECT?
3397 022436	001404	BEQ XOR2		
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
				CONDITIONAL BRANCH INST. AND <=====
				REPLACE THE MOVE INSTRUCTION <=====
				WHICH FOLLOWS W/ 761 <=====
022440	012742	000530	XOR1: MOV #530,-(R2)	:MOVE TO MAILBOX # ***** 530 *****
022444	005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
022446	000000		HALT	:
3398 022450	010104		XOR2: MOV R1,R4	:CC=1110
3399 022452	000261		SEC	:CC=1110
3400 022454	000241		CLC	
3401 022456	074400		XOR R4,R0	:TRY XOR MODE 0,0
3402 022460	101406		BLOS XOR3	:CC=0000?
3403 022462	102405		BVS XOR3	
3404 022464	001404		BEQ XOR3	
3405 022466	100403		BMI XOR3	
3406 022470	022700	007463	CMP #7463,R0	
3407 022474	001404		BEQ TST232	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
				CONDITIONAL BRANCH INST. AND <=====
				REPLACE THE MOVE INSTRUCTION <=====
				WHICH FOLLOWS W/ 742 <=====
022476	012742	000531	XOR3: MOV #531,-(R2)	:MOVE TO MAILBOX # ***** 531 *****
022502	005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
022504	000000		HALT	:RESULT OF XOR INCORRECT
3408				: OR SEQUENCE ERROR
3409				*****
3410				THIS TEST VERIFIES THE SOB INSTRUCTION. R4 IS USED AS A
3411				COUNTER WHILE R0 IS THE ADDRESS REGISTER. CONDITIONAL
3412				BRANCHES ARE USED TO VERIFY PROPER TRANSFER OF CONTROL
3413				WHILE R4 IS CHECKED TO INSURE PROPER DECREMENTING OF R0.
3414				*****
3415				TEST 232 TEST SOB INSTRUCTION
022506 005212	000232	TST232: INC (R2)	:UPDATE TEST NUMBER	
022510 022712	000232	CMP #232, (R2)	:SEQUENCE ERROR?	
022514 001023		BNE TST233-10	:BR TO ERROR HALT ON SEQ ERROR	
3416 022516	012700	000525	MOV #525,R0	
3417 022522	010004		MOV R0,R4	
3418 022524	000277	SCC	:SET CC=1111	

3419 022526 101002		SOB1: BHI S0B2 ;CC=1111?	
3420 022530 100001		BPL S0B2	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND
3421 022532 102404		BVS S0B3	REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 770
022534		S0B2: MOV #532,-(R2)	: MOVE TO MAILBOX # ***** 532 *****
022534 012742 000532		INC -(R2)	: SET MSGTYP TO FATAL ERROR
022540 005242		HALT	: COUNT ITERATIONS
022542 000000		S0B3: DEC R4	:CC=1111
3422 022544 005304		SCC R0,S0B1	:DO SOB W/ R0
3423 022546 000277		S0B4	:CHECK CC=1111
3424 022550 077012		BHI	: TST233 - ;ITERATION COUNT OK?
3425 022552 101004		S0B4	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND
3426 022554 100003		BPL	REPLACE THE MOVE INSTRUCTION
3427 022556 102002		BVC	WHICH FOLLOWS W/ 754
3428 022560 005704		TST	: INCORRECT # OF BRANCHES OR CC'S CHANGED
3429 022562 001404		R4	: OR SEQUENCE ERROR
022564		S0B4: MOV #533,-(R2)	: MOVE TO MAILBOX # ***** 533 *****
022564 012742 000533		INC -(R2)	: SET MSGTYP TO FATAL ERROR
022570 005242		HALT	: INCORRECT # OF BRANCHES OR CC'S CHANGED
022572 000000			: OR SEQUENCE ERROR
3430		***** THIS TEST VERIFIES THE MARK INSTRUCTION. THE EFFECTS	
3431		OF THE MARK INSTRUCTION ARE SIMULATED BY THE PROGRAM INSTRUCTIONS.	
3432		THE CONTENTS OF R5 AND THE STACK POINTER ARE CHECKED AFTER EACH	
3433		OF THE TWO ROUTINES IN THE TEST.	
3434		 *****	
3435		TEST 233 TEST MARK INSTRUCTION	
3436		 *****	
3437		 *****	
022574 005212		TST233: INC (R2)	: UPDATE TEST NUMBER
022576 022712 000233		CMP #233,(R2)	: SEQUENCE ERROR?
022602 001062		BNE TST234-10	: BR TO ERROR HALT ON SEQ ERROR
3438 022604 012706 001000		MOV #STBOT,SP	: PUT R5 VALUE ON STACK
3439 022610 012746 125252		MOV #125252,-(SP)	: EFFECTIVELY PUT 36 ARGUMENTS ON STACK
3440 022614 162706 000074		SUB #74,SP	: SET NEW PC IN R5
3441 022620 012705 022646		MOV #MRK1,R5	: PUT MARK 36 INST. ON STACK
3442 022624 012746 006436		MOV #6436,-(SP)	: SET CC=1111
3443 022630 000277		SCC	: XFER CONTL TO MARK 36 INST. ON STACK
3444 022632 000137 000700		JMP @#700	: MOVE TO MAILBOX # ***** 534 *****
3445 022636 012742 000534		MOV #534,-(R2)	: SET MSGTYP TO FATAL ERROR
022642 005242		INC -(R2)	: MARK INST. SHOULD HAVE JUMPED TO MRK1
022644 000000		HALT	: TEST CC UNAFFECTED
3446 022646 101010		MRK1: BHI MRK2	: IE. CC=1111
3447 022650 100007		BPL MRK2	: CHECK R5 RESTORED FROM STACK
3448 022652 102006		BVC MRK2	: CHECK STACK POINTER READJUSTED CORRECTLY.
3449 022654 020527 125252		CMP R5,#125252	
3450 022660 001003		BNE MRK2	
3451 022662 022706 001000		CMP #STBOT,R6	

3452 022666 001404

BEQ MRK3

022670			MRK2:
022670	012742	000535	MOV #535,-(R2)
022674	005242		INC -(R2)
022676	000000		HALT
3453	022700	012746	MRK3:
3454	022704	052525	MOV #52525,-(SP)
3455	022710	012746	MOV #6400,-(SP)
3456	022712	006400	MOV SP,R5
3457	022716	010605	JSR PC,@#MRK4
3458	022722	004737	JMP @#MRK5
3459	022724	022722	RTS R5
022730	005242	000536	MOV #536,-(R2)
022732	000000		INC -(R2)
3460	022734	022734	HALT
			MRK5: CMP #STBOT,R6

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND   
; REPLACE THE MOVE INSTRUCTION   
; WHICH FOLLOWS W/ 745 <=====  
  
; MOVE TO MAILBOX # \*\*\*\*\* 535 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; RESULTS OF MARK INCORRECT  
  
; PUT MARK 0 INST. ON STACK  
; SET ADDR. OF MARK INST. IN R5  
; DO JSR  
  
; DO RTS WITH R5 TO MARK INST ON STACK  
; MOVE TO MAILBOX # \*\*\*\*\* 536 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; RTS,MARK SEQUENCE FAILED  
; STACK ADJUSTED CORRECTLY

3462 022740 001003  
3463 022742 022705 052525  
3464 022746 001404

BNE MRK6 ;IF NOT: BR  
CMP #52525,R5 ;CHECK IF R5 RESTORED FROM STACK  
BEQ TST234

; IF NOT: BR  
; CHECK IF R5 RESTORED FROM STACK  
  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 715 <=====

022750 012742 000537  
022750 005242  
022754 000000  
022756

MRK6:  
MOV #537,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 537 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;RESULTS OF MARK INCORRECT  
; OR SEQUENCE ERROR

3465  
3466  
3467  
3468  
3469  
3470  
3471  
3472  
3473

THIS TEST VERIFIES THAT RESET DOES NOT CLEAR THE PSW. THE PSW IS LOADED WITH ONES, A RESET IS ISSUED, AND THE CONTENTS OF THE PSW ARE CHECKED TO VERIFY THAT THEY HAVE NOT CHANGED. THIS TEST IS EXECUTED ONLY ONCE EVERY 256 (DECIMAL) PASSES.

TEST 234 TEST THAT RESET DOES NOT CLEAR PSW

	022760	005212		
	022762	022712	000234	
	022766	001014		
3474	022770	123727	036066	000377
3475	022776	001014		
3476	023000	012737	000357	177776
3477	023006	000005		
3478	023010	022737	000357	177776
3479	023016	001404		

```

IST234: INC      (R2)          :UPDATE TEST NUMBER
        CMP      #234, (R2)       :SEQUENCE ERROR?
        BNE      TST235-10      :BR TO ERROR HALT ON SEQ ERROR
        CMPB     @#PASSPT, #377   :ONLY DUE RESET EVERY 256. PASSES
        BNE      REST           :BR IF TO SKIP TEST
        MOV      #357, @#PS       :MOV ONES TO PSW
        RESET
        CMP      #357, @#PS       :PSW CORRECT?
        BEQ      TST235

```

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
: CONDITIONAL BRANCH INST. AND <=====  
: REPLACE THE MOVE INSTRUCTION <=====  
: WHICH FOLLOWS W/ 763 <=====

023020 012742 000540  
023024 005242  
023026 000000

MOV #540,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 540 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;RESET ALTERED PSW  
; OR SEQUENCE ERROR

3480 023030  
3481  
3482  
3483  
3484  
3485  
3486  
3487

REST.

THE FOLLOWING TEST CHECKS THE INDEPENDENT FUNCTIONING OF BASIC DATA PATH COMPONENTS WITH USER/SUPERVISOR MODE SET.

023030	005212			
023032	022712	000235		
023036	001034			
3488	023040	052767	140000	154730
3489	023046	012706	000001	
3490	023052	000241		
3491	023054	006106		

```

;TEST 235      TEST USER/SUPER S.P. CAN HOLD A 1 IN EVERY BIT
***** TST235: INC    (R2)          ;UPDATE TEST NUMBER
      CMP    #235, (R2)        ;SEQUENCE ERROR?
      BNE    TST236-10       ;BR TO ERROR HALT ON SEQ ERROR
      BIS    #USRM,PS         ;SET USER MODE
      MOV    #1,R6             ;SET BIT0
      CLC
USP1:   ROL    R6             ;CLEAR C-BIT
                  ;ROTATE 1 POSITION

```

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T235 TEST USER/SUPER S.P. CAN HOLD A 1 IN EVERY BIT

B 12

SEQ 0144

3522 023236 001404

BEQ USP3

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 743 <=====

023240	012742	000544	MOV	#544,-(R2)			
023244	005242		INC	-(R2)			
023246	000000		HALT				
3523	023250	052767	140000	154520	USP3:	BIS	#USR,M,PS
3524	023256	022706	011111			CMP	#011111,R6
3525	023262	001404				BEQ	USP4

MOVE TO MAILBOX # \*\*\*\*\* 544 \*\*\*\*\*  
SET MSGTYP TO FATAL ERROR  
DUAL ADDRESSING SEQUENCE ERROR  
;SET USER MODE  
:VERIFY R6 WITH USER

023264	012742	000545			MOV	#545,-(R2)	
023270	005242				INC	-(R2)	
023272	000000				HALT		
3526	023274	042767	140000	154474	USP4:	BIC	#140000,PS
3527	023302	012706	044444			MOV	#044444,R6
3528	023306	052767	040000	154462		BIS	#040000,PS
3529	023314	012706	055555			MOV	#055555,R6
3530	023320	052767	140000	154450		BIS	#140000,PS
3531	023326	012706	066666			MOV	#066666,R6
3532	023332	022706	066666			CMP	#066666,R6
3533	023336	001404				BEQ	USP5

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 731 <=====

023340	012742	000546	MOV	#546,-(R2)			
023344	005242		INC	-(R2)			
023346	000000		HALT				
3534	023350	042767	100000	154420	USP5:	BIC	#100000,PS
3535	023356	022706	055555			CMP	#055555,RE
3536	023362	001404				BEQ	USP6

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 703 <=====

	023364	012742	000547		MOV	#547,-(R2)	
	023370	005242			INC	-(R2)	
	023372	000000			HALT		
3537	023374	042767	140000	154374	USP6:	BIC	#140000,PS
3538	023402	022706	044444			CMP	#044444,RE
3539	023406	001404				BFO	TST237

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 671

023410 012742 000550  
023414 005242  
023416 000000

MOV #550,-(R2)  
INC -(R2)  
HALT

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 657 <=====  
MOVE TO MAILBOX # \*\*\*\*\* 550 \*\*\*\*\*  
SET MSGTYP TO FATAL ERROR  
DUAL ADDRESSING SEQUENCE ERROR  
OR SEQUENCE ERROR

3540  
3541  
3542

3543  
3544  
3545  
3546

THESE NEXT TWO TESTS VERIFY MFPI AND MTPI INSTRUCTIONS  
WITH R6 IN MODE 0.

\*\*\*\*\* TEST 237 TEST MFPI WITH R6 IN MODE 0 \*\*\*\*\*

023420 005212	023422 022712	000237	TST237: INC (R2)	:UPDATE TEST NUMBER
023426 001033			CMP #237,(R2)	:SEQUENCE ERROR?
3547 023430 012706	012706	001000	BNE TST240-10	:BR TO ERROR HALT ON SEQ ERROR
3548 023434 012767	140000	154334	MOV #STBOT,R6	:INITIALIZE KERNEL STACK POINTER
3549 023442 012706	036370		MOV #USRMR,PS	:SET USER MODE.PREVIOUS KERNEL
3550 023446 006506			MOV #USTBOT,R6	:INITIALIZE USER STACK POINTER
3551 023450 022767	140000	154320	MFPI R6	:TRY MFPI WITH MODE 0
3552 023456 001410			CMP #140000,PS	:CHECK PSW
3553 023460 042767	140000	154310	BEQ MFPIO	:BR IF NO ERROR
3554 023466 001417			BIC #USRMR,PS	:CLEAR USER MODE
			BEQ TST240	
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND <span style="float: right;">=====</span> REPLACE THE MOVE INSTRUCTION <span style="float: right;">=====</span> WHICH FOLLOWS W/ 757 <span style="float: right;">=====</span>
023470 012742 000551			MOV #551,-(R2)	:MOVE TO MAILBOX # ***** 551 *****
023474 005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR
023476 000000			HALT	:INCORRECT PSW FROM MFPI :OR SEQUENCE ERROR
3555 023500 022767	001000	012660	MFPIO: CMP #STBOT,USTBOT-2	:CHECK DATA ON STACK
3556 023506 001407			BEQ MFPIOA	:BR IF NO ERROR
3557 023510 042767	140000	154260	BIC #USRMR,PS	:CLEAR USER MODE
3558 023516 012742	000552		MOV #552,-(R2)	:MOVE TO MAILBOX # ***** 552 *****
023522 005242			INC -(R2)	:SET MSGTYP TO FATAL ERROR
023524 000000			HALT	:INCORRECT DATA FROM MFPI
3559 023526			MFPIOA:	
3560				
3561				
023526 005212	023530 022712	000240	TST240: INC (R2)	:UPDATE TEST NUMBER
023534 001033	005067	154234	CMP #240,(R2)	:SEQUENCE ERROR?
3562 023536 005067			BNE TST241-10	:BR TO ERROR HALT ON SEQ ERROR
3563 023542 005006			CLR PS	:SET KERNEL MODE
3564 023544 012767	140000	154224	CLR R6	:INITIALIZE KERNEL R6
3565 023552 012706	036370		MOV #USRMR,PS	:SET USER MODE/PREVIOUS KERNEL
3566 023556 012746	001000		MOV #USTBOT,R6	:INITIALIZE USER STACK POINTER
3567 023562 006606			MOV #STBOT,-(R6)	:SET UP TARGET DATA
3568 023564 022767	140000	154204	MTPI R6	:TRY MODE 0 MTPI
3569 023572 001407			CMP #USRMR,PS	:CHECK PSW
3570 023574 042767	140000	154174	BEQ MTPIO	:BR IF NO ERROR
3571 023602 012742	000553		BIC #USRMR,PS	:CLEAR USER MODE
023606 005242			MOV #553,-(R2)	:MOVE TO MAILBOX # ***** 553 *****
023610 000000			INC -(R2)	:SET MSGTYP TO FATAL ERROR
3572 023612 005067	154160		HALT	:PS INCORRECT FOLLOWING MTPI
3573 023616 020627	001000		MTPIO: CLR PS	:SET KERNEL MODE
3574 023622 001404			CMP R6,#STBOT	:CHECK TARGET DATA
			BEQ TST241	
				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND <span style="float: right;">=====</span> REPLACE THE MOVE INSTRUCTION <span style="float: right;">=====</span>

T240 TEST MTPI WITH R6 IN MODE 0

SEQ 0147

 023624 012742 000554  
 023630 005242  
 023632 000000

 MOV #554,-(R2)  
 INC -(R2)  
 HALT

WHICH FOLLOWS W/ 744  
 =====  
 ;MOVE TO MAILBOX # \*\*\*\*\* 554 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;DATA INCORRECT FOLLOWING MTPI  
 ; OR SEQUENCE ERROR

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3599

3600

\*\*\*\*\* THIS TEST VERIFIES THE CONTENTS OF THE BRANCH ROM. THE TEST  
 EXECUTES EVERY POSSIBLE BRANCH WITH EVERY POSSIBLE CONDITION  
 CODE COMBINATION.

THE ROUTINE USES TWO TABLES. THE BRANCH TABLE HOLDS ALL THE  
 POSSIBLE BRANCH INSTRUCTIONS, THE OTHER TABLE (YNTAB) HOLDS BIT MAPS FOR  
 EACH BRANCH. A ONE IN THE BIT MAP INDICATES THAT THE CORRESPONDING  
 BRANCH INSTRUCTION SHOULD BRANCH FOR THE CONDITION CODE SETTING WHICH  
 CORRESPONDS TO THE BIT POSITION WITHIN THE MAP. FOR EXAMPLE IF THE LEFT  
 MOST BIT IS A ONE THEN THE CORRESPONDING BRANCH INSTRUCTION SHOULD BRANCH  
 WHEN THE CONDITION CODES ARE 0.

THE ROUTINE CONSISTS OF NESTED LOOPS; THE OUTER LOOP SETS UP  
 ALL THE POSSIBLE BRANCH INSTRUCTIONS. THE INNER LOOP SETS UP EVERY POSSIBLE  
 CONDITION CODE FOR EACH BRANCH.

THE BIT MAP IS USED TO SET THE ADDRESS LOCATION IN TWO  
 JUMP MODE 3 INSTRUCTIONS. THE ADDRESSES ARE CHANGED TO ALLOW THE  
 PROGRAM TO CONTINUE OR JUMP TO AN ERROR ROUTINE DEPENDING UPON  
 WHETHER IT HANDLED THE BRANCH INSTRUCTION CORRECTLY.

AT ANY ERROR HALT, LOCATION, BRH, HOLDS THE BRANCH INSTRUCTION  
 UNDER TEST AND LOCATION, CC, HOLDS THE VALUE OF THE CONDITION CODES  
 AT THE TIME THE BRANCH WAS EXECUTED.

## TEST 241 TEST THE BRANCH ROM

 023634 005212  
 023636 022712 000241  
 023642 001062  
 3601 023644 012700 036142  
 3602 023650 012704 036216  
 3603 023654 012767 000017 000142  
 3604 023662 012067 000110  
 3605 023666 012401  
 3606 023670 012767 177777 000074  
 3607 023676 012703 000020  
 3608 023702 005267 000064  
 3609 023706 032701 100000  
 3610 023712 013705 177776  
 023716 042705 177773  
 023722 000165 023726  
 023726 000167 000020  
 3611 023732 012767 024026 000042  
 3612 023740 012767 024010 000040  
 3613 023746 000167 000014  
 3614 023752 012767 024010 000022  
 3615 023760 012767 024026 000020  
 3616 023766 006101  
 3617  
 3618 023770 012737

TST241: INC (R2) ;UPDATE TEST NUMBER  
 CMP #241,(R2) ;SEQUENCE ERROR?  
 BNE ER ;BR TO ERROR HALT ON SEQ ERROR  
 SETUP: MOV #BRTAB,R0 ;INITIALIZE BRANCH TABLE POINTER  
 MOV #YNTAB,R4 ;INITIALIZE YES/NO BRANCH MAP POINTER  
 MOV #15.,BRCT ;INITIALIZE BRANCH TABLE COUNT  
 SETBR: MOV (R0)+,BRH ;GET NEXT BRANCH INST.  
 MOV (R4)+,R1 ;GET NEXT BRANCH MAP  
 MOV #-1,CC ;INITIALIZE CONDITION CODE VALUE  
 MOV #16.,R3 ;INITIALIZE CONDITION CODE COUNT  
 SETCC: INC CC ;SET FOR NEXT CC VALUE  
 BIT #100000,R1 ;SEE IF SHOULD BR W/ THESE CC'S  
 MOV @#177776,R5 ;SIMULATE A JNE  
 BIC #177773,R5 ;(JUMP NOT EQUAL)  
 JMP .+4(R5) ;TO SET2BR  
 SET2BR: JMP SET2BR  
 MOV #CONT,NBR ;SET TO CONTINUE IF NO BRANCH  
 MOV #ER,YBR ;SET TO REPORT ERROR IF BRANCH  
 JMP AROUND ;GO AROUND OPPOSITE CONDITION  
 SET2BR: MOV #ER,NBR ;SET TO REPORT ERROR IF NO BRANCH  
 MOV #CONT,YBR ;SET TO CONTINUE IF BRANCH  
 AROUND: ROL R1 ;UPDATE BIT MAP  
 MOV (PC)+,@(PC)+ ;SET CONDITION CODE

T241 TEST THE BRANCH ROM

SFQ 0148

3619	023772	000000	CC:	0	;NEW CC VALUE GOES HERE
3620	023774	177776	BRH:	177776	;BRANCH INST. GOES HERE
3621	023776	000000	NBR:	0	;THIS JUMP IF NO BRANCH
3622	024000	000137		JMP @PC+	;WHERE TO GO IF NO BRANCH OCCURS
3623	024002	000000		JMP @PC+	;THIS JUMP IF BRANCH OCCURS
3624	024004	000137	YBR:	0	;WHERE TO GO IF BRANCH OCCURS
3625	024006	000000	ER:	MOV #\$TESTN,R2	;RESTORE POINTER
3626	024010	012702		MOV #555,-(R2)	;MOVE TO MAILBOX # ***** 555 *****
3627	024014	012742		INC -(R2)	;SET MSGTYP TO FATAL ERROR
	024020	005242			;
	024022	000000			;
3628	024024	000000	BRCT:	0	;
3629	024026	005303	CONT:	DEC R3	;CC'S DONE?
3630	024030	013705		MOV @#177776,R5	;SIMULATE A JNE
	024034	042705		BIC #177773,R5	; (JUMP NOT EQUAL)
	024040	000165		JMP .+4(R5)	; TO SETCC
	024044	000167		JMP SETCC	;
3631	024050	005367		DEC BRCT	;BR'S DONE?
3632	024054	013705		MOV @#177776,R5	;SIMULATE A JNE
	024060	042705		BIC #177773,R5	; (JUMP NOT EQUAL)
	024064	000165		JMP .+4(R5)	; TO SETBR
	024070	000167		JMP SETBR	;

3633

3634

3635

3636

:THE FOLLOWING TEST VERIFIES THAT NO DUAL ADDRESSING OF THE GENERAL  
:REGISTERS OCCURS. ALL REGISTERS ARE CLEARED, AND A UNIQUE BIT IS SET  
:IN EACH. CMP INSTRUCTIONS CHECK THAT ONLY ONE BIT IS SET IN EACH  
:REGISTER.

3639

3640

3641

## ;TEST 242 DUAL REGISTER ADDRESSING TEST

024074	005212		TST242:	INC (R2)	;UPDATE TEST NUMBER
024076	022712	000242		CMP #242,(R2)	;SEQUENCE ERROR?
024102	001052			BNE DAERR	;BR TO ERROR HALT ON SEQ ERROR
3642	024104	005000	BITCLR:	CLR R0	;INITIALIZE ALL REGISTERS
3643	024106	005001		CLR R1	
3644	024110	005002		CLR R2	
3645	024112	005003		CLR R3	
3646	024114	005004		CLR R4	
3647	024116	005005		CLR R5	
3648	024120	005006		CLR R6	
3649	024122	052700	BITSET:	BIS #1,R0	;SET R0=1
3650	024126	052701		BIS #2,R1	;R1=2
3651	024132	052702		BIS #4,R2	;R2=4
3652	024136	052703		BIS #10,R3	;R3=10
3653	024142	052704		BIS #20,R4	;R4=20
3654	024146	052705		BIS #40,R5	;R5=40
3655	024152	052706		BIS #100,R6	;R6=100
3656	024156	022706		BITCHK: CMP #100,R6	;TEST THAT NO DUAL ADDRESSING OCCURRED
3657	024162	001022		BNE DAERR	;BR TO ERROR HALT IF ANY OTHER BITS ARE SET
3658	024164	022705		CMP #40,R5	
3659	024170	001017		BNE DAERR	
3660	024172	022704		CMP #20,R4	
3661	024176	001014		BNE DAERR	
3662	024200	022703		CMP #10,R3	

3663	024204	001011		BNE	DAERR
3664	024206	022702	000004	CMP	#4,R2
3665	024212	001006		BNE	DAERR
3666	024214	022701	000002	CMP	#2,R1
3667	024220	001003		BNE	DAERR
3668	024222	022700	000001	CMP	#1,R0
3669	024226	001404		BEQ	BITCON

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 725 <=====

024230				DAERR:	
024230	012742	000556		MOV	#556,-(R2)
024234	005242			INC	-(R2)
024236	000000			HALT	
3670	024240	012702	000304	BITCON:	MOV #\$TESTN,R2

;MOVE TO MAILBOX # \*\*\*\*\* 556 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;DUAL ADDRESSING ERROR  
;RESTORE POINTER

3671					
3672					
3673					
3674					
3675					
3676					
3677					
3678					

024244	005212			TST243: INC	(R2)
024246	022712	000243		CMP	#243,(R2)
024252	001012			BNE	BTERR
3679	024254	052737	170357 177776	BIS	#170357,@#PS
3680	024262	105037	177776	CLRB	@#PS
3681	024266	013700	177776	MOV	@#PS,R0
3682	024272	032700	170000	BIT	#170000,R0
3683	024276	001006		BNE	BTCON
3684	024300	005037	177776	BTERR: CLR	@#PS
3685	024304	012742	000557	MOV	#557,-(R2)
024310	005242			INC	-(R2)
024312	000000			HALT	
3686	024314	005037	177776	BTCON: CLR	@#PS

;UPDATE TEST NUMBER  
;SEQUENCE ERROR?  
;BR TO ERROR HALT ON SEQ ERROR  
;SET ALL POSSIBLE BITS IN PSW  
;CLR PR LEVEL AND CC'S  
;COPY CONTENTS OF PSW  
;TEST THAT UPPER BYTE IS UNAFFECTED  
;CONTINUE IF OK  
;RETURN TO KERNEL MODE  
;MOVE TO MAILBOX # \*\*\*\*\* 557 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;BYTE INSTRUCTION ALTERED PSW  
;RETURN TO KERNEL MODE

3687					
3688					
3689					
3690					
3691					
3692					
3693					
3694					

024320	005212			TST244: INC	(R2)
024322	022712	000244		CMP	#244,(R2)
024326	001010			BNE	TST245-10
3695	024330	000277		SCC	
3696	024332	000252		+CLN!CLV	
3697	024334	000167	000000	JMP	JMPT
3698	024340	100403		BMI	JMPERR
3699	024342	001002		BNE	JMPERR

;UPDATE TEST NUMBER  
;SEQUENCE ERROR?  
;BR TO ERROR HALT ON SEQ ERROR  
;CC=0101  
;JUMP TO TEST PSW  
;BR TO ERROR HALT IF N-BIT IS SET  
;BR TO ERROR HALT IF Z-BIT IS CLEAR

T244 TEST THAT JMP OPCODE DOES NOT AFFECT C.C.'S

SEQ 0150

3700 024344 102401  
3701 024346 103404BVS  
BCSJMPERR  
TST245

;BR TO ERROR HALT IF V-BIT IF SET

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 767 <=====024350  
024350 012742 000560  
024354 005242  
024356 000000

JMPERR:

MOV  
INC  
HALT#560,-(R2)  
-(R2);MOVE TO MAILBOX # \*\*\*\*\* 560 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;JMP INSTRUCTION AFFECTED CC'S  
;OR SEQUENCE ERROR3702  
3703  
3704  
3705  
3706  
3707  
3708  
3709  
3710  
3711  
3712  
3713  
3714  
3715  
3716

\*\*\*\*\* THIS TEST VERIFIES THE SET AND CLEAR CONDITION CODE INSTRUCTIONS.  
 THE TEST CONSISTS OF TWO ROUTINES, ONE TO TEST ALL CLEAR CC  
 INSTRUCTIONS, AND THE SECOND TO TEST ALL SET CC INSTRUCTIONS. ALL  
 POSSIBLE COMBINATIONS OF CONDITION CODES ARE TESTED, INCLUDING NOP'S.  
 TO TEST THE CLEAR CC INSTRUCTIONS, ALL CONDITION CODES ARE  
 INITIALLY SET. THE INSTRUCTION IS EXECUTED, AND THE PSW IS CHECKED  
 TO VERIFY THE PROPER COMBINATION OF CONDITION CODES.  
 TO TEST THE SET CC INSTRUCTIONS, THE CONDITION CODES ARE  
 INITIALLY CLEARED, AND ONLY THE REQUIRED BITS ARE SET BY THE SET CC  
 INSTRUCTION. THE CONTENTS OF THE PSW ARE CHECKED TO VERIFY THAT  
 ONLY THE REQUIRED BITS WERE SET.

;TEST 245 TEST SET CC AND CLEAR CC INSTRUCTIONS

024360 005212  
024362 022712 000245  
024366 001062  
3717 024370 012767 000240 000024  
3718 024376 012767 000017 000032  
3719 024404 012767 000261 000102  
3720 024412 012767 000001 000110  
3721 024420 000277  
3722 024422 000000  
3723 024424 013704 177776  
3724 024430 042704 177760  
3725 024434 022704  
3726 024436 000000  
3727 024440 001404

TST245: INC (R2) ;UPDATE TEST NUMBER  
 CMP #245, (R2) ;SEQUENCE ERROR?  
 BNE CCERR ;BR TO ERROR HALT ON SEQ ERROR  
 MOV #240, CC1 ;INITIALIZE CLR CC INSTRUCTION CODES  
 MOV #17, CC2 ;INITIALIZE OCTAL MAP  
 MOV #261, SC3 ;INITIALIZE SET CC INSTRUCTION CODES  
 MOV #1, SC4 ;INITIALIZE OCTAL MAP  
 CLRC: SCC ;SET ALL CONDITION CODES  
 CC1: 0 ;CONDITION CODE INSTRUCTION  
 MOV @#PS, R4 ;COPY THE PSW  
 BIC #177760, R4 ;ISOLATE CONDITION CODES  
 CMP (PC)+, R4 ;CHECK THAT PROPER CC'S WERE CLEARED  
 CC2: 0 ;OCTAL REPRESENTATION OF CC'S  
 REQ CON1

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 752 <=====024442 012742 000561  
024446 005242  
024450 000000  
3728 024452 005367 177760  
3729 024456 005267 177740  
3730 024462 026727 177734 000257  
3731 024470 003753  
3732 024472 026727 177724 000260  
3733 024500 001004  
3734 024502 012767 000017 177726  
3735 024510 000743CON1: MOV #561, -(R2)  
INC -(R2)  
HALT  
DEC CC2  
INC CC1  
CMP CC1, #257  
BLE CLRCD  
CMP CC1, #260  
BNE SETCD  
MOV #17, CC2  
BR CLRCD;MOVE TO MAILBOX # \*\*\*\*\* 561 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;CLEAR CC INSTRUCTION FAILED  
;SET NEXT OCTAL MAP OF CC'S  
;GET NEXT CLEAR CC INSTRUCTION  
;TEST FOR CCC INSTRUCTION  
;GO TEST NEXT INSTRUCTION IF NOT FOUND  
;CHECK FOR NOP=260  
;GO TEST SET CC INSTRUCTIONS  
;SET OCTAL MAP TO TEST NOP  
;GO TEST NOP

3736 024512 000257 SETCD: CCC :CLEAR ALL CONDITION CODES  
 3737 024514 000000 SC3: 0 :CONDITION CODE INSTRUCTION  
 3738 024516 013704 177776 MOV @#PS,R4 :COY PSW  
 3739 024522 042704 177760 BIC #177760,R4 :CLEAR AWAY UNWANTED BITS  
 3740 024526 022704 CMP (PC)+,R4 :CHECK THAT PROPER CC'S WERE SET  
 3741 024530 000000 SC4: 0 :OCTAL REPRESENTATION OF CC'S  
 3742 024532 001404 BEQ CON2  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 715 <=====  
 ;<=====  
 ;<=====  
 ;<=====  
 024534 012742 000562 CCERR:  
 024540 005242 MOV #562,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 562 \*\*\*\*\*  
 024542 000000 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 3743 024544 005267 177760 HALT :SET CC FAILED OR SEQUENCE ERROR  
 3744 024550 005267 177740 CON2: INC SC4 :SET NEXT OCTAL MAP  
 3745 024554 026727 177734 000277 INC SC3 :PREPARE NEXT SET CC INSTRUCTION  
 3746 024562 003753 CMP SC3,#277 :FINISHED?  
 3747 BLE SETCD :BR IF NO  
 ;\*\*\*\*\*  
 3748  
 3749  
 3750 THESE NEXT TWO TEST VERIFY MFpd AND MTPD INSTRUCTIONS  
 3751 WITH R6 IN MODE 0.  
 3752  
 3753  
 ;TEST 246 TEST MFpd WITH R6 IN MODE 0  
 ;\*\*\*\*\*  
 024564 005212 TST246: INC (R2) :UPDATE TEST NUMBER  
 024566 022712 000246 CMP #246,(R2) :SEQUENCE ERROR?  
 024572 001032 BNE TST247-10 :BR TO ERROR HALT ON SEQ ERROR  
 3754 024574 012706 001000 MOV #STBOT,R6 :INITIALIZE KERNEL STACK POINTER  
 3755 024600 012767 140000 153170 MOV #USRm,PS :SETUP USER MODE .PREVIOUS KERNEL  
 3756 024606 012706 036370 MOV #USTBOT,R6 :INITIALIZE USER STACK POINTER  
 3757 024612 106506 MFPD R6 :TRY MFpd WITH MODE 0  
 3758 024614 022767 140000 153154 CMP #140000,PS :CHECK PSW  
 3759 024622 001407 BEQ MFPDO :BR IF NO ERROR  
 3760 024624 042767 140000 153144 BIC #USRm,PS :CLEAR USER MODE  
 3761 024632 012742 000563 MOV #563,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 563 \*\*\*\*\*  
 024636 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 024640 000000 HALT :INCORRECT PSW FROM MFpd  
 3762 024642 022767 001000 011516 MFPDO: CMP #STBOT,USTBOT-2 :CHECK DATA ON STACK  
 3763 024650 001407 BEQ MFPDOA :BR IF NO ERROR  
 3764 024652 042767 140000 153116 BIC #USRm,PS :CLEAR USER MODE  
 3765 024660 012742 000564 MOV #564,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 564 \*\*\*\*\*  
 024664 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 024666 000000 HALT :INCORRECT DATA FROM MFpd  
 3766 024670 MFPDOA:  
 ;\*\*\*\*\*  
 3767  
 3768 ;TEST 247 TEST MTPD WITH R6 IN MODE 0  
 ;\*\*\*\*\*  
 024670 005212 TST247: INC (R2) :UPDATE TEST NUMBER  
 024672 022712 000247 CMP #247,(R2) :SEQUENCE ERROR?  
 024676 001031 BNE TST250-10 :BR TO ERROR HALT ON SEQ ERROR  
 3769 024700 005067 153072 CLR PS :SET KERNEL MODE  
 3770 024704 005006 CLR R6 :INITIALIZE KERNEL R6

3771 024706 012767 140000 153062	MOV #USR,M,PS	:SET USER MODE/PREVIOUS KERNEL
3772 024714 012746 001000	MOV #STBOT,-(R6)	:SET UP TARGET DATA
3773 024720 106606	MTPD R6	:TRY MODE 0 MTPD
3774 024722 022767 140000 153046	CMP #USR,M,PS	:CHECK PSW
3775 024730 001407	BEQ MTPD0	:BR IF NO ERROR
3776 024732 042767 140000 153036	BIC #USR,M,PS	:CLEAR USER MODE
3777 024740 012742 000565	MOV #565,-(R2)	:MOVE TO MAILBOX # ***** 565 *****
024744 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR
024746 000000	HALT	:PS INCORRECT FOLLOWING MTPD
3778 024750 005067 153022	MTPD0: CLR PS	:SET KERNEL MODE
3779 024754 020627 001000	CMP R6,#STBOT	:CHECK TARGET DATA
3780 024760 001404	BEQ TST250	
		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 746
024762 012742 000566	MOV #566,-(R2)	:MOVE TO MAILBOX # ***** 566 *****
024766 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR
024770 000000	HALT	:DATA INCORRECT FOLLOWING MTPD
3781		: OR SEQUENCE ERROR
3782		
3783		
		:TEST 250 TEST MFPT INSTRUCTION
024772 005212	TST250: INC (R2)	:UPDATE TEST NUMBER
024774 022712 000250	CMP #250,(R2)	:SEQUENCE ERROR?
025000 001005	BNE TST251-10	:BR TO ERROR HALT ON SEQ ERROR
3784 025002 005000	CLR R0	:SET UP R0
3785 025004 000007	MFPT	:MOVE FROM PROCESSOR TYPE
3786 025006 122700 000001	CMPB #1,R0	:CHECK FOR A ONE IN R0
3787 025012 001404	BEQ TST251	
		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 772
025014 012742 000567	MOV #567,-(R2)	:MOVE TO MAILBOX # ***** 567 *****
025020 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR
025022 000000	HALT	:MFPT FAILED TO RETURN A 1, IN R0
3788		: OR SEQUENCE ERROR
3789		
3790		
3791		
3792		:SBTTL BIT TEST OF PIRQ REGISTER
3793		:A COUNT PATTERN IS THEN RUN THRU THE REGISTER TO ENSURE THAT
3794		:THE ENCODER FUNCTIONS PROPERLY.
3795		
3796		
		:TEST 251 BIT TEST OF PIRQ REGISTER
025024 005212	TST251: INC (R2)	:UPDATE TEST NUMBER
025026 022712 000251	CMP #251,(R2)	:SEQUENCE ERROR?
025032 001064	BNE TST252-10	:BR TO ERROR HALT ON SEQ ERROR
3797 025034 012706 001000	MOV #STBOT,SP	:INITIALIZE THE SP
3798 025040 012767 025054 011144	MOV #4\$,SLPADR	:SETUP LOOP ADR
3799 025046 012767 025054 011140	MOV #4\$,SLPERR	:SETUP ERROR LOOP

3800 025054 052737 000340 177776 4\$:	BIS #340, <del>@#177776</del>	:SET THE CPU PRIORITY AT 7.
3801 025062 005067 011112	CLR \$TMPO	:SETUP COMPARISON LOCATION
3802 025066 005037 177772	CLR @#PIRQ	:CLEAR PIRQ REGISTER
3803 025072 026737 011102 177772	CMP \$TMPO, <del>@#PIRQ</del>	:DID PIRQ CLEAR
3804 025100 001035	BNE 1\$	:BRANCH IF NO
3805 025102 012700 000177	MOV #177,R0	:SETUP ITERATION COUNT
3806 025106 012767 001042 011064	MOV #1042,\$TMPO	:SETUP COMPARISON LOCATION
3807 025114 012701 000002	MOV #2,R1	:SETUP R1
3808 025120 062737 001000 177772 2\$:	ADD #1000, <del>@#PIRQ</del>	:START COUNT PATTERN
3809 025126 026737 011046 177772	CMP \$TMPO, <del>@#PIRQ</del>	:DID REGISTER SET CORRECT?
3810 025134 001017	BNE 1\$	:BRANCH IF NO
3811 025136 120137 177773	CMPB R1, <del>@#PIRQ+1</del>	:IS PIRQ READY TO GO TO NEXT LEVEL?
3812 025142 001005	BNE 3\$	:BRANCH IF NO
3813 025144 062767 000042 011026	ADD #42,\$TMPO	:INCREMENT ENCODED VALUE IN TEST LOC.
3814 025152 005201	INC R1	:SETUP R1 FOR ROTATE
3815 025154 006101	ROL R1	:SET R1 TO NEXT CHECK LEVEL
3816 025156 062767 001000 011014 3\$:	ADD #1000,\$TMPO	:INC. PIRQ LEVEL IN TEST LOCATION
3817 025164 077023	SOB R0,2\$	:CONTINUE COUNT
3818 025166 005037 177772	CLR @#PIRQ	:ENSURE PIRQ CLEAR
3819 025172 000410	BR EIS	:GO TO NEXT TEST
3820 025174 013767 177772 011006 1\$:	MOV @#PIRQ,SEPIRQ	:SAVE PIRQ FOR ERRCR CHECKING
3821 025202 001404	BEQ TST252	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND =====  
REPLACE THE MOVE INSTRUCTION =====  
WHICH FOLLOWS W/ 713 =====

:MOVE TO MAILBOX # \*\*\*\*\* 570 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:PIRQ REG. FAILED  
: OR SEQUENCE ERROR

025204 012742 000570  
025210 005242  
025212 000000

MOV #570,-(R2)  
INC -(R2)  
HALT

3822 025214

EIS:

3824  
3825  
3826  
3827  
3828  
3829

.SBTTL EIS ASH/ASCH/MUL/DIV TESTS  
.SBTTL ASH SHIFTING RIGHT USING DM2 REG 7  
;SHIFT RIGHT CLEAR N-BIT AND C-BIT  
;MODE 2-REG 7

025214	005212		
025216	022712	000252	
025222	001026		
3830	025224	012706	001000
3831	025230	005037	177776
3832	025234	012700	040000
3833	025240	072027	177765
3834	025244	013767	177776
3835	025252	122767	000000
3836	025260		011216
			011210
			001404

;TEST 252 ASH 40000 SHIFTED BY 177765=10 PS=0

TST252:	INC	(R2)	UPDATE TEST NUMBER
	CMP	#252,(R2)	SEQUENCE ERROR?
	BNE	TST253-10	BR TO ERROR HALT ON SEQ ERROR
	MOV	#STBOT,R6	
	CLR	@#PS	
	MOV	#40000,R0	:LOAD R0 WITH 40000
	ASH	#177765,R0	:SHIFT R0 BY 177765
	MOV	@#PS,SPSW	:SAVE PS
	CMPB	#0,SPSW	:IS THE PS 0?
	BEQ	1\$	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 760

025262	012742	000571	
025266	005242		
025270	000000		
3837	025272	022700	000010
3838	025276		001404

1\$: MOV #571,-(R2)  
INC -(R2)  
HALT

MOV	#571,-(R2)	MOVE TO MAILBOX # ***** 571 *****
INC	-(R2)	SET MSGTYP TO FATAL ERROR
HALT		THE PS IS NOT EQUAL TO 0

:IS THE RESULT 10?

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 751

025300	012742	000572	
025304	005242		
025306	000000		

MOV	#572,-(R2)	MOVE TO MAILBOX # ***** 572 *****
INC	-(R2)	SET MSGTYP TO FATAL ERROR
HALT		R0 IS NOT EQUAL TO 10

: OR SEQUENCE ERROR

3839  
3840  
3841  
3842

:SHIFT RIGHT SET N-BIT CLEAR C-BIT  
;MODE 2 /REG 7

;TEST 253 ASH 125252 SHIFTED BY -2=165252 PS=11

TST253:	INC	(R2)	UPDATE TEST NUMBER
	CMP	#253,(R2)	SEQUENCE ERROR?
	BNE	TST254-10	BR TO ERROR HALT ON SEQ ERROR
	MOV	#125252,R0	:LOAD R0 WITH 125252
	ASH	#-2,R0	:SHIFT R0 BY -2
	MOV	@#PS,SPSW	:SAVE PS
	CMPB	#11,SPSW	:IS THE PS 11?
	BEQ	1\$	

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 764

025346	012742	000573	
025352	005242		
025354	000000		
3848	025356	022700	165252

MOV	#573,-(R2)	MOVE TO MAILBOX # ***** 573 *****
INC	-(R2)	SET MSGTYP TO FATAL ERROR
HALT		THE PS IS NOT EQUAL TO 11

:IS THE RESULT 165252?

3849 025362 001404

BEQ TST254

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 755 <=====

025364 012742 000574  
025370 005242  
025372 000000

MOV #574,-(R2)  
INC -(R2)  
HALT

;MOVE TO MAILBOX # \*\*\*\*\* 574 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;R0 IS NOT EQUAL TO 165252  
; OR SEQUENCE ERROR

3850  
3851  
3852  
3853

;SHIFT RIGHT CLEAR N-BIT SET Z-BIT  
;MODE 2 /REG 7

;\*\*\*\*\* TEST 254 ASH 0 SHIFTED BY -16. =0 PS=4 \*\*\*\*\*

025374 005212  
025376 022712 000254  
025402 001022  
3854 025404 012700 000000  
3855 025410 072027 177760  
3856 025414 013767 177776 011046  
3857 025422 122767 000004 011040  
3858 025430 001404

TST254: INC (R2)  
CMP #254,(R2)  
BNE TST255-10  
MOV #0,R0  
ASH #16.,R0  
MOV @#PS,SPSW  
CMPB #4,SPSW  
BEQ 1\$

;UPDATE TEST NUMBER  
;SEQUENCE ERROR?  
;BR TO ERROR HALT ON SEQ ERROR  
;LOAD R0 WITH 0  
;SHIFT R0 BY -16.  
;SAVE PS  
;IS THE PS 4?

025432 012742 000575  
025436 005242  
025440 000000  
3859 025442 022700 000000  
3860 025446 001404

1\$: CMP #0,R0  
BEQ TST255

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 764 <=====

;MOVE TO MAILBOX # \*\*\*\*\* 575 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;THE PS IS NOT EQUAL TO 4  
;IS THE RESULT 0?

025450 012742 000576  
025454 005242  
025456 000000

MOV #576,-(R2)  
INC -(R2)  
HALT

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 755 <=====

;MOVE TO MAILBOX # \*\*\*\*\* 576 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;R0 IS NOT EQUAL TO 0  
; OR SEQUENCE ERROR

3861  
3862  
3863  
3864  
3865

.SBTTL ASH SHIFTING LEFT STORE ASH DM2 REG 7  
;SHIFT LEFT SET C-BIT=0 STORE ASH  
;MODE 2 /REG 7

;\*\*\*\*\* TEST 255 ASH 0 SHIFTED BY 0=0 PS=4 \*\*\*\*\*

025460 005212  
025462 022712 000255  
025466 001022  
3866 025470 012700 000000  
3867 025474 072027 000000  
3868 025500 013767 177776 010762  
3869 025506 122767 000004 010754  
3870 025514 001404

TST255: INC (R2)  
CMP #255,(R2)  
BNE TST256-10  
MOV #0,R0  
ASH #0,R0  
MOV @#PS,SPSW  
CMPB #4,SPSW  
BEQ 1\$

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND <=====

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 764 <=====  
 025516 012742 000577 MOV #577,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 577 \*\*\*\*\*  
 025522 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 025524 000000 HALT ;THE PS IS NOT EQUAL TO 4  
 3871 025526 022700 000000 1\$: CMP #0, R0 ;IS THE RESULT 0?  
 3872 025532 001404 BEQ TST256 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                                   ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 755 <=====  
 025534 012742 000600 MOV #600,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 600 \*\*\*\*\*  
 025540 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 025542 000000 HALT ;R0 IS NOT EQUAL TO 0  
 ; OR SEQUENCE ERROR  
 3873  
 3874  
 3875 .SBTTL ASH SHIFTING LEFT DM6 REG 7  
 3876 ;SHIFT LEFT SET C-BIT=1  
 3877 ;MODE 6 /REG 7  
 3878 :\*\*\*\*\*  
 :TEST 256      ASH 125252 SHIFTED BY S1=125250 PS=12  
 :\*\*\*\*\*  
 025544 005212 TST256: INC (R2) ;UPDATE TEST NUMBER  
 025546 022712 000256 CMP #256, (R2) ;SEQUENCE ERROR?  
 025552 001024 BNE TST257-10 ;BR TO ERROR HALT ON SEQ ERROR  
 3879 025554 012700 125252 MOV #125252, R0 ;LOAD R0 WITH 125252  
 3880 025560 012704 036476 MOV #S1, R4 ;SET UP R4  
 3881 025564 072067 010706 ASH S1, R0 ;SHIFT R0 BY S1  
 3882 025570 013767 177776 010672 MOV @PS, SPSW ;SAVE PS  
 3883 025576 122767 000012 010664 CMPB #12, SPSW ;IS THE PS 12?  
 3884 025604 001404 BEQ 1\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                           ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 762 <=====  
 025606 012742 000601 MOV #601,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 601 \*\*\*\*\*  
 025612 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 025614 000000 HALT ;THE PS IS NOT EQUAL TO 12  
 3885 025616 022700 125250 1\$: CMP #125250, R0 ;IS THE RESULT 125250?  
 3886 025622 001404 BEQ TST257 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                           ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 753 <=====  
 025624 012742 000602 MOV #602,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 602 \*\*\*\*\*  
 025630 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 025632 000000 HALT ;R0 IS NOT EQUAL TO 177525  
                           ; OR SEQUENCE ERROR  
 3887 .SBTTL ASH SHIFTING LEFT TEST SIGN Z-BIT DM7 REG 7  
 3888 ;SHIFT LEFT COUNT DOWN TO ZERO TEST SIGN Z-BIT  
 3889 ;MODE 7 /REG 7  
 3890 :\*\*\*\*\*  
 :TEST 257      ASH 125252 SHIFTED BY @S2= 177525 PS=10  
 :\*\*\*\*\*  
 025634 005212 TST257: INC (R2) ;UPDATE TEST NUMBER

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T257 ASH 125252 SHIFTED BY @S2= 177525 PS=10

B 13

SEQ 0157

025636 022712 000257      CMP #257,(R2) ;SEQUENCE ERROR?  
025642 001024      BNE TST260-10 ;BR TO ERROR HALT ON SEQ ERROR  
3892 025644 012700 125252      MOV #125252,R0 ;LOAD R0 WITH 125252  
3893 025650 012703 036504      MOV #S4,R3 ;SET UP R3  
3894 025654 072077 010624      ASH @S4,R0 ;SHIFT R0 BY @S2  
3895 025660 013767 177776 010602      MOV @#PS,SPSW ;SAVE PS  
3896 025666 122767 000010 010574      CMPB #10,SPSW ;IS THE PS 10?  
3897 025674 001404      BEQ 1\$ ;  
  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 762 <=====  
  
025676 012742 000603      MOV #603,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 603 \*\*\*\*\*  
025702 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
025704 000000      HALT ;THE PS IS NOT EQUAL TO 10  
3898 025706 022700 177525      1\$: CMP #177525,R0 ;IS RESULT 177525?  
3899 025712 001404      BEQ TST260 ;  
  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 753 <=====  
  
025714 012742 000604      MOV #604,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 604 \*\*\*\*\*  
025720 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
025722 000000      HALT ;R0 IS NOT EQUAL TO 177525  
; OR SEQUENCE ERROR  
  
3900 .SBTTL ASH SHIFTING LEFT TESTING IR9 FOR ASH/ASHC DM3 REG 7  
3901 ;SHIFT LEFT TEST IR9 TO DETERMINE ASH/ASHC  
3902 ;MODE 3 /REG 7  
3903  
3904 ;\*\*\*\*\*  
;TEST 260 ASH 125252 SHIFTED BY @S1=177525 PS=10  
;\*\*\*\*\*  
  
025724 005212      TST260: INC (R2) ;UPDATE TEST NUMBER  
025726 022712 000260      CMP #260,(R2) ;SEQUENCE ERROR?  
025732 001024      BNE TST261-10 ;BR TO ERROR HALT ON SEQ ERROR  
3905 025734 012700 125252      MOV #125252,R0 ;LOAD R0 WITH 125252  
3906 025740 012704 036502      MOV #S3,R4 ;SET UP R4  
3907 025744 072037 036502      ASH @#S3,R0 ;SHIFT R0 BY @S1  
3908 025750 013767 177776 010512      MOV @#PS,SPSW ;SAVE PS  
3909 025756 122767 000010 010504      CMPB #10,SPSW ;IS THE PS 10?  
3910 025764 001404      BEQ 1\$ ;  
  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 762 <=====  
  
025766 012742 000605      MOV #605,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 605 \*\*\*\*\*  
025772 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
025774 000000      HALT ;THE PS IS NOT EQUAL TO 10  
3911 025776 022700 177525      1\$: CMP #177525,R0 ;IS THE RESULT 177525?  
3912 026002 001404      BEQ TST261 ;  
  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 753 <=====  
  
026004 012742 000606      MOV #606,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 606 \*\*\*\*\*  
026010 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
026012 000000      HALT ;R0 IS NOT EQUAL TO 177525

; OR SEQUENCE ERROR

3913  
 3914  
 3915  
 3916  
 3917  
 3918  
 3919

.SBTTL ASH SHIFTING LEFT USING DM6 REG 7  
 :SHIFT LEFT TEST R17 TO DETERMINE C-BIT  
 :CLEAR BX TO INDICATE C-BIT=0  
 :MODE 6 /REG 7

;\*\*\*\*\*  
 ;TEST 261 ASH 025252 SHIFTED S1=125250 PS=12  
 ;\*\*\*\*\*

026014	005212			
026016	022712	000261		
026022	001024			
3920	026024	012700	025252	
3921	026030	012704	036476	
3922	026034	072067	010436	
3923	026040	013767	177776	010422
3924	026046	122767	000012	010414
3925	026054	001404		

TST261:	INC	(R2)	:UPDATE TEST NUMBER
	CMP	#261,(R2)	:SEQUENCE ERROR?
	BNE	TST262-10	:BR TO ERROR HALT ON SEQ ERROR
	MOV	#025252,R0	:LOAD R0 WITH 025252
	MOV	#\$1,R4	:SET UP R4
	ASH	S1,R0	:SHIFT R0 BY S1
	MOV	@#PS,SPSW	:SAVE PS
	CMPB	#12,SPSW	
	BEQ	1\$	:IS THE PS 10?

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 : CONDITIONAL BRANCH INST. AND <=====  
 : REPLACE THE MOVE INSTRUCTION <=====  
 : WHICH FOLLOWS W/ 762 <=====

026056	012742	000607		
026062	005242			
026064	000000			
3926	026066	022700	125250	
3927	026072	001404		

	MOV	#607,-(R2)	:MOVE TO MAILBOX # ***** 607 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:THE PS IS NOT EQUAL TO 10
1\$:	CMP	#125250,R0	:IS THE RESULT 125250
	BEQ	TST262	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 : CONDITIONAL BRANCH INST. AND <=====  
 : REPLACE THE MOVE INSTRUCTION <=====  
 : WHICH FOLLOWS W/ 753 <=====

026074	012742	000610		
026100	005242			
026102	000000			

	MOV	#610,-(R2)	:MOVE TO MAILBOX # ***** 610 *****
	INC	-(R2)	:SET MSGTYP TO FATAL ERROR
	HALT		:R0 IS NOT EQUAL TO 077525

; OR SEQUENCE ERROR

3928  
 3929  
 3930  
 3931  
 3932  
 3933

.SBTTL ASHC SHIFTING POS.USING DMO REG 2  
 :MODE 0 REG 4

;\*\*\*\*\*  
 ;TEST 262 ASHC 125252,125252,SHIF BY R4=177525 52525 PS=10  
 ;\*\*\*\*\*

026104	005212			
026106	022712	000262		
026112	001035			
3934	026114	012700	125252	
3935	026120	012701	125252	
3936	026124	000241		
3937	026126	012704	177771	
3938	026132	073004		
3939	026134	013767	177776	010326
3940	026142	122767	000010	010320
3941	026150	001404		

TST262:	INC	(R2)	:UPDATE TEST NUMBER
	CMP	#262,(R2)	:SEQUENCE ERROR?
	RNE	TST263-10	:BR TO ERROR HALT ON SEQ ERROR
	MOV	#125252,R0	:LOAD R0 WITH 125252
	MOV	#125252,R1	:LOAD R0!1 WITH 125252
	CLC		
	MOV	#-7,R4	:SET UP R4
	ASHC	R4,R0	:SHIFT R0,R0!1 BY R4
	MOV	@#PS,SPSW	:SAVE PS
	CMPB	#10,SPSW	
	BEQ	1\$	:IS THE PS 10?

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 : CONDITIONAL BRANCH INST. AND <=====

						REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 760 <=====	
026152	012742	000611	MOV	#611,-(R2)	:MOVE TO MAILBOX # ***** 611 ***** <=====		
026156	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR <=====		
026160	000000		HALT		:THE PS IS NOT EQUAL TO 10 <=====		
3942	026162	022700	CMP	#177525,R0	:IS RESULT 177525? <=====		
3943	026166	001404	BEG	2\$			
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====		
					CONDITIONAL BRANCH INST. AND <=====		
					REPLACE THE MOVE INSTRUCTION <=====		
					WHICH FOLLOWS W/ 751 <=====		
026170	012742	000612	MOV	#612,-(R2)	:MOVE TO MAILBOX # ***** 612 ***** <=====		
026174	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR <=====		
026176	000000		HALT		:R0 IS NOT EQUAL TO 177525 <=====		
3944	026200	022701	CMP	#52525,R1	:IS THE RESULT 52525? <=====		
3945	026204	001404	BEQ	TST263			
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====		
					CONDITIONAL BRANCH INST. AND <=====		
					REPLACE THE MOVE INSTRUCTION <=====		
					WHICH FOLLOWS W/ 742 <=====		
026206	012742	000613	MOV	#613,-(R2)	:MOVE TO MAILBOX # ***** 613 ***** <=====		
026212	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR <=====		
026214	000000		HALT		:R1 IS NOT EQUAL TO 52525 <=====		
					: OR SEQUENCE ERROR <=====		
3946			.SBTTL ASHC SHIFTING NEG. USING DM4 REG 3				
3947							
3948							
3949							
			***** TEST 263 *****				
026216	005212		TST263:	INC	(R2) :UPDATE TEST NUMBER <=====		
026220	022712	000263		CMP	#263,(R2) :SEQUENCE ERROR? <=====		
026224	001035			BNE	TST264-10 :BR TO ERROR HALT ON SEQ ERROR <=====		
3950	026226	012700	125252	MOV	#125252,R0 :LOAD R0 WITH 125252 <=====		
3951	026232	012701	125252	MOV	#125252,R1 :LOAD R0:1 WITH 125252 <=====		
3952	026236	000241		CLC			
3953	026240	012703	036504	MOV	#S3+2,R3 :SET UP R3 <=====		
3954	026244	073043		ASHC	-(R3),R0 :SHIFT R0,R0:1 BY -(3) <=====		
3955	026246	013767	177776	010214	MOV	@#PS,SPSW :SAVE PS <=====	
3956	026254	122767	000010	010206	CMPB	#10,SPSW :IS THE PS 10? <=====	
3957	026262	001404		BEQ	1\$		
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====		
					CONDITIONAL BRANCH INST. AND <=====		
					REPLACE THE MOVE INSTRUCTION <=====		
					WHICH FOLLOWS W/ 760 <=====		
026264	012742	000614	MOV	#614,-(R2)	:MOVE TO MAILBOX # ***** 614 ***** <=====		
026270	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR <=====		
026272	000000		HALT		:THE PS IS NOT EQUAL TO 10 <=====		
3958	026274	022700	177525	CMP	#177525,R0 :IS THE RESULT 177525 <=====		
3959	026300	001404	BEG	2\$			
					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====		
					CONDITIONAL BRANCH INST. AND <=====		
					REPLACE THE MOVE INSTRUCTION <=====		
					WHICH FOLLOWS W/ 751 <=====		
026302	012742	000615	MOV	#615,-(R2)	:MOVE TO MAILBOX # ***** 615 ***** <=====		
026306	005242		INC	-(R2)	:SET MSGTYP TO FATAL ERROR <=====		
026310	000000		HALT		:R0 IS NOT EQUAL TO 177525 <=====		

3960 026312 022701 052525	2\$: CMP BEQ	#52525,R1 TST264	: IS THE RESULT 52525?  : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 742 <=====
3961 026316 001404			<=====
026320 012742 000616	MOV INC HALT	#616,-(R2) -(R2)	: MOVE TO MAILBOX # ***** 616 ***** : SET MSGTYP TO FATAL ERROR : R0!1 IS NOT EQUAL TO 52525 : OR SEQUENCE ERROR <=====
026324 005242			<=====
026326 000000			<=====
3962			
3963			
3964			
3965			
			.SBTTL ASHC SHIFTED BY @-(4) DM5 REG 4 : MODE 5 REG 4
			;***** TEST 264 ASHC 125252 SHIFTED BY @-(4)=177525 52525 PS=10 *****
026330 005212	TST264: INC	(R2)	: UPDATE TEST NUMBER <=====
026332 022712	CMP	#264,(R2)	: SEQUENCE ERROR? <=====
026336 001035	BNE	TST265-10	: BR TO ERROR HALT ON SEQ ERROR <=====
3966 026340 012700	MOV	#125252,R0	: LOAD R0 WITH 125252 <=====
3967 026344 012701	MOV	#125252,R1	: LOAD R0!1 WITH 125252 <=====
3968 026350 000241	CLC		
3969 026352 012704	MOV	#S4+2,R4	: SET UP R4 <=====
3970 026356 073054	ASHC	@-(R4),R0	: SHIFT R0,!1 BY @-(4) <=====
3971 026360 013767	MOV	@#PS,SPSW	: SAVE PS <=====
3972 026366 122767	CMPB	#10,SPSW	: IS THE PS 10? <=====
3973 026374 001404	BEQ	1\$	
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 760 <=====
026376 012742 000617	MOV	#617,-(R2)	: MOVE TO MAILBOX # ***** 617 ***** <=====
026402 005242	INC	-(R2)	: SET MSGTYP TO FATAL ERROR <=====
026404 000000	HALT		: THE PS IS NOT EQUAL TO 10 <=====
3974 026406 022700	CMP	#177525,R0	: IS THE RESULT 177525? <=====
3975 026412 001404	BEQ	2\$	
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 751 <=====
026414 012742 000620	MOV	#620,-(R2)	: MOVE TO MAILBOX # ***** 620 ***** <=====
026420 005242	INC	-(R2)	: SET MSGTYP TO FATAL ERROR <=====
026422 000000	HALT		: R0 IS NOT EQUAL TO 177525 <=====
3976 026424 022701	CMP	#52525,R1	: IS THE RESULT 52525? <=====
3977 026430 001404	BEQ	TST265	
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS : CONDITIONAL BRANCH INST. AND : REPLACE THE MOVE INSTRUCTION : WHICH FOLLOWS W/ 742 <=====
026432 012742 000621	MOV	#621,-(R2)	: MOVE TO MAILBOX # ***** 621 ***** <=====
026436 005242	INC	-(R2)	: SET MSGTYP TO FATAL ERROR <=====
026440 000000	HALT		: R0!1 IS NOT EQUAL TO 52525 <=====
			: OR SEQUENCE ERROR <=====
3978			
3979			
3980			
3981			
			.SBTTL ASHC SHIFTED BY @-(4) DM7 REG 4 : MODE 7 REG 4
			;*****

; TEST 265 ASHC 1252552,125252,SHIF,@(4)=177525,52525 PS=10  
 ;\*\*\*\*\*  
 026442 005212 000265 TST265: INC (R2) ;UPDATE TEST NUMBER  
 026444 022712 000265 CMP #265,(R2) ;SEQUENCE ERROR?  
 026450 001036 BNE TST266-10 ;BR TO ERROR HALT ON SEQ ERROR  
 3982 026452 012700 125252 MOV #125252,R0 ;LOAD R0 WITH 125252  
 3983 026456 012701 125252 MOV #125252,R1 ;LOAD R0:1 WITH 125252  
 3984 026462 000241 CLC  
 3985 026464 012704 036504 MOV #S4,R4 ;SET UP R4  
 3986 026470 073074 000000 ASHC @R4,R0 ;SHIFT R0,R0:1 BY @(4)  
 3987 026474 013767 177776 007766 MOV @#PS,SPSW ;SAVE PS  
 3988 026502 122767 000010 007760 CMPB #10,SPSW ;IS THE PS 10?  
 3989 026510 001404 BEQ 1\$ ;  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 ; CONDITIONAL BRANCH INST. AND <=====  
 ; REPLACE THE MOVE INSTRUCTION <=====  
 ; WHICH FOLLOWS W/ 757 <=====  
 026512 012742 000622 MOV #622,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 622 \*\*\*\*\*  
 026516 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 026520 000000 HALT ;THE PS IS NOT EQUAL TO 10  
 3990 026522 022700 177525 1\$: CMP #177525,R0 ;IS THE RESULT 177525?  
 3991 026526 001404 BEQ 2\$ ;  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 ; CONDITIONAL BRANCH INST. AND <=====  
 ; REPLACE THE MOVE INSTRUCTION <=====  
 ; WHICH FOLLOWS W/ 750 <=====  
 026530 012742 000623 MOV #623,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 623 \*\*\*\*\*  
 026534 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 026536 000000 HALT ;R0 IS NOT EQUAL TO 177525  
 3992 026540 022701 052525 2\$: CMP #52525,R1 ;IS THE RESULT 52525?  
 3993 026544 001404 BEQ TST266 ;  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 ; CONDITIONAL BRANCH INST. AND <=====  
 ; REPLACE THE MOVE INSTRUCTION <=====  
 ; WHICH FOLLOWS W/ 741 <=====  
 026546 012742 000624 MOV #624,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 624 \*\*\*\*\*  
 026552 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 026554 000000 HALT ;R0:1 IS NOT EQUAL TO 52525  
 ; OR SEQUENCE ERROR  
 3994 .SBTTL ASHC SHIFTED BY -32. DM2 REG 7  
 3995 ;MODE 2 REG 7  
 3996 ;  
 3997 ;TEST 266 ASHC 100000 0 SHIFTED BY -32.=-1 -1 PS=11  
 ;\*\*\*\*\*  
 026556 005212 000266 TST266: INC (R2) ;UPDATE TEST NUMBER  
 026560 022712 000266 CMP #266,(R2) ;SEQUENCE ERROR?  
 026564 001034 BNE TST267-10 ;BR TO ERROR HALT ON SEQ ERROR  
 3998 026566 012700 100000 MOV #100000,R0 ;LOAD R0 WITH 100000  
 3999 026572 012701 000000 MOV #0,R1 ;LOAD R0:1 WITH 0  
 4000 026576 000241 CLC  
 4001 026600 073027 177740 ASHC #-32.,R0 ;SHIFT R0,R0:1 BY -32.  
 4002 026604 013767 177776 007656 MOV @#PS,SPSW ;SAVE PS  
 4003 026612 122767 000011 007650 CMPB #11,SPSW ;IS THE PS 11?  
 4004 026620 001404 BEQ 1\$ ;  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 ; CONDITIONAL BRANCH INST. AND <=====

					REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 761	<=====
026622	012742	000625	MOV	#625,-(R2)	MOVE TO MAILBOX # ***** 625 *****	<=====
026626	005242		INC	-(R2)	SET MSGTYP TO FATAL ERROR	<=====
026630	000000		HALT		THE PS IS NOT EQUAL TO 11	<=====
4005 026632	022700	177777	1\$: CMP	#-1,R0	IS THE RESULT -1?	<=====
4006 026636	001404		BEQ	2\$		
					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
					CONDITIONAL BRANCH INST. AND	<=====
					REPLACE THE MOVE INSTRUCTION	<=====
					WHICH FOLLOWS W/ 752	<=====
026640	012742	000626	MOV	#626,-(R2)	MOVE TO MAILBOX # ***** 626 *****	<=====
026644	005242		INC	-(R2)	SET MSGTYP TO FATAL ERROR	<=====
026646	000000		HALT		RO IS NOT EQUAL TO -1	<=====
4007 026650	022701	177777	2\$: CMP	#-1,R1 :IS THE RESULT -1?		
4008 026654	001404		BEQ	TST267		
					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
					CONDITIONAL BRANCH INST. AND	<=====
					REPLACE THE MOVE INSTRUCTION	<=====
					WHICH FOLLOWS W/ 743	<=====
026656	012742	000627	MOV	#627,-(R2)	MOVE TO MAILBOX # ***** 627 *****	<=====
026662	005242		INC	-(R2)	SET MSGTYP TO FATAL ERROR	<=====
026664	000000		HALT		RO!1 IS NOT EQUAL TO -1	<=====
					; OR SEQUENCE ERROR	
4009						
4010					.SBTTL ASHC SHIFTED BY 15 DM2 REG 7	
4011					:MODE 2 REG 7	
4012					***** TEST 267 ASHC 0 -1 SHIFTED BY 15.=77777 100000 PS=0 *****	
026666	005212		TEST267: INC	(R2)	UPDATE TEST NUMBER	<=====
026670	022712	000267	CMP	#267,(R2)	SEQUENCE ERROR?	<=====
026674	001034		BNE	TST270-10	BR TO ERROR HALT ON SEQ ERROR	<=====
4013 026676	012700	000000	MOV	#0,R0	LOAD RO WITH 0	<=====
4014 026702	012701	177777	MOV	#-1,R1 ;LOAD RO!1 WITH -1		
4015 026706	000241		CLC			
4016 026710	073027	000017	ASHC	#15.,R0	:SHIFT RO,RO!1 BY 15.	<=====
4017 026714	013767	177776	MOV	@#PS,SPSW	:SAVE PS	<=====
4018 026722	122767	000000	CMPB	#0,SPSW	:IS THE PS 0?	<=====
4019 026730	001404		BEQ	1\$		
					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
					CONDITIONAL BRANCH INST. AND	<=====
					REPLACE THE MOVE INSTRUCTION	<=====
					WHICH FOLLOWS W/ 761	<=====
026732	012742	000630	MOV	#630,-(R2)	MOVE TO MAILBOX # ***** 630 *****	<=====
026736	005242		INC	-(R2)	SET MSGTYP TO FATAL ERROR	<=====
026740	000000		HALT		THE PS IS NOT EQUAL TO 0	<=====
4020 026742	022700	077777	1\$: CMP	#77777,R0	IS THE RESULT 77777?	<=====
4021 026746	001404		BEQ	2\$		
					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
					CONDITIONAL BRANCH INST. AND	<=====
					REPLACE THE MOVE INSTRUCTION	<=====
					WHICH FOLLOWS W/ 752	<=====
026750	012742	000631	MOV	#631,-(R2)	MOVE TO MAILBOX # ***** 631 *****	<=====
026754	005242		INC	-(R2)	SET MSGTYP TO FATAL ERROR	<=====
026756	000000		HALT		RO IS NOT EQUAL TO 77777	<=====
4022 026760	022701	100000	2\$: CMP	#100000,R1	IS THE RESULT 100000?	<=====

4023 026764 001404

BEQ TST270

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 743 <=====

026766 012742 000632  
026772 005242  
026774 000000

MOV #632,-(R2)  
INC -(R2)  
HALT

:MOVE TO MAILBOX # \*\*\*\*\* 632 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:R0!1 IS NOT EQUAL TO 100000  
: OR SEQUENCE ERROR

4024

4025

4026

4027

.SBTTL ASHC SHIFTED BY 16. DM2 REG 7  
:MODE 2 REG 7

:\*\*\*\*\* TEST 270 ASHC 0 52525 SHIFTED BY 16.=52525 0 PS=0 \*\*\*\*\*

026776 005212 000270  
027000 022712 000270  
027004 001034  
4028 027006 012700 000000  
4029 027012 012701 052525  
4030 027016 000241  
4031 027020 073027 000020  
4032 027024 013767 177776 007436  
4033 027032 122767 000000 007430  
4034 027040 001404

TST270: INC (R2)  
CMP #270,(R2)  
BNE TST271-10  
MOV #0,R0  
MOV #52525,R1  
CLC  
ASHC #16.,R0  
MOV @#PS,SPSW  
CMPB #0,SPSW  
BEQ 1\$

:UPDATE TEST NUMBER  
:SEQUENCE ERROR?  
:BR TO ERROR HALT ON SEQ ERROR  
:LOAD R0 WITH 0  
:LOAD R0!1 WITH 52525  
:SHIFT R0,R0!1 BY 16.  
:SAVE PS  
:IS THE PS 0?

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 761 <=====

027042 012742 000633  
027046 005242  
027050 000000  
4035 027052 022700 052525  
4036 027056 001404

1\$: CMP #52525,R0  
BEQ 2\$

:MOVE TO MAILBOX # \*\*\*\*\* 633 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:THE PS IS NOT EQUAL TO 0  
:IS THE RESULT 52525?

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 752 <=====

027060 012742 000634  
027064 005242  
027066 000000  
4037 027070 022701 000000  
4038 027074 001404

2\$: CMP #0,R1  
BEQ TST271

:MOVE TO MAILBOX # \*\*\*\*\* 634 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:R0 IS NOT EQUAL TO 52525  
:IS THE RESULT 0?

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 743 <=====

027076 012742 000635  
027102 005242  
027104 000000

MOV #635,-(R2)  
INC -(R2)  
HALT

:MOVE TO MAILBOX # \*\*\*\*\* 635 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:R0!1 IS NOT EQUAL TO 0  
: OR SEQUENCE ERROR

4039

4040

:MODE 2 REG 7

4042

027106	005212	
027110	022712	000271
027114	001034	
4043 027116	012700	177777
4044 027122	012701	000000
4045 027126	000241	
4046 027130	073027	000020
4047 027134	013767	177776 007326
4048 027142	122767	000007 007320
4049 027150	001404	

```

:***** TEST 271 ASHC -1 0 SHIFTED BY 16. =0 0 PS=7 *****
:TST271: INC (R2) :UPDATE TEST NUMBER
           CMP #271,(R2) :SEQUENCE ERROR?
           BNE TST272-10 :BR TO ERROR HALT ON SEQ ERROR
           MOV #1,R0 :LOAD R0 WITH -1
           MOV #0,R1 :LOAD R0!1 WITH 0
           CLC
           ASHC #16.,R0 :SHIFT R0,R0!1 BY 16.
           MOV @#PS,SPSW :SAVE PS
           CMPB #7,SPSW :IS THE PS 7?
           BEQ 1$ :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
                      CONDITIONAL BRANCH INST. AND
                      REPLACE THE MOVE INSTRUCTION
                      WHICH FOLLOWS W/ 761 <=====

027152 012742 000636      MOV #636,-(R2) :MOVE TO MAILBOX # ***** 636 *****
027156 005242             INC -(R2) :SET MSGTYP TO FATAL ERROR
027160 000000             HALT :THE PS IS NOT EQUAL TO 7
4050 027162 022700 000000   1$: CMP #0,R0 :IS THE RESULT 0?
4051 027166 001404             BEQ 2$ :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
                      CONDITIONAL BRANCH INST. AND
                      REPLACE THE MOVE INSTRUCTION
                      WHICH FOLLOWS W/ 752 <=====

027170 012742 000637      MOV #637,-(R2) :MOVE TO MAILBOX # ***** 637 *****
027174 005242             INC -(R2) :SET MSGTYP TO FATAL ERROR
027176 000000             HALT :R0 IS NOT EQUAL TO 0
4052 027200 022701 000000   2$: CMP #0,R1 :IS THE RESULT 0?
4053 027204 001404             BEQ TST272 :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
                      CONDITIONAL BRANCH INST. AND
                      REPLACE THE MOVE INSTRUCTION
                      WHICH FOLLOWS W/ 743 <=====

027206 012742 000640      MOV #640,-(R2) :MOVE TO MAILBOX # ***** 640 *****
027212 005242             INC -(R2) :SET MSGTYP TO FATAL ERROR
027214 000000             HALT :R0!1 IS NOT EQUAL TO 0
                                : OR SEQUENCE ERROR

4054
4055
4056
4057 .SBTTL ASHC SHIFTED BY @4 DM7 REG 4
          ;MODE 7 REG 4
:***** TEST 272 ASHC 125252,125252,SHIF,@4=177525,52525 PS=10 *****
:TST272: INC (R2) :UPDATE TEST NUMBER
           CMP #272,(R2) :SEQUENCE ERROR?
           BNE TST273-10 :BR TO ERROR HALT ON SEQ ERROR
           MOV #125252,R1 :LOAD R0!1 WITH 125252
           MOV #125252,R0 :LOAD R0 WITH 125252
           CLC
           MOV #S4,R4 :SET UP R4
           ASHC @,(R4),R0 :SHIFT R0,R0!1 BY @4
           MOV @#PS,SPSW :SAVE PS
           CMPB #10,SPSW :IS THE PS 10?
           BEQ 1$ :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
```

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T272 ASMC 125252,125252,SHIF, @4)=177525,52525 PS=10

J 13

SEQ 0165

027266	012742	000641		MOV	#641,-(R2)	WHICH FOLLOWS W/ 757 MOVE TO MAILBOX # ***** 641 *****	<=====	
027272	005242			INC	-(R2)	;SET MSGTYP TO FATAL ERROR		
027274	000000			HALT		;THE PS IS NOT EQUAL TO 10		
4066	027276	022701	052525	1\$:	CMP	#52525,R1	;IS THE RESULT 52525?	
4067	027302	001404		BEQ	2\$			
						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 750	<=====	
						MOVE TO MAILBOX # ***** 642 *****	<=====	
027304	012742	000642		MOV	#642,-(R2)	;SET MSGTYP TO FATAL ERROR	<=====	
027310	005242			INC	-(R2)	;R0!1 IS NOT EQUAL TO 52525	<=====	
027312	000000			HALT		;IS THE RESULT 177525?	<=====	
4068	027314	022700	177525	2\$:	CMP	#177525,R0		
4069	027320	001404		BEQ	TST273			
						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 741	<=====	
						MOVE TO MAILBOX # ***** 643 *****	<=====	
027322	012742	000643		MOV	#643,-(R2)	;SET MSGTYP TO FATAL ERROR	<=====	
027326	005242			INC	-(R2)	;R0 IS NOT EQUAL TO 177525	<=====	
027330	000000			HALT		;OR SEQUENCE ERROR	<=====	

4073  
4074

## .SBTTL MUL USING DM2 REG 7

027332	005212		
027334	022712	000273	
027340	001035		
4075	027342	012706	001000
4076	027346	005037	177776
4077	027352	012700	100000
4078	027356	070027	100000
4079	027362	013767	177776
4080	027370	122767	000001
4081	027376	001404	

;TEST 273 MUL 100000 \* #100000 = 40000 0 PS=1  
;TST273: INC (R2) ;UPDATE TEST NUMBER  
;CMP #273, (R2) ;SEQUENCE ERROR?  
;BNE TST274-10 ;BR TO ERROR HALT ON SEQ ERROR  
;MOV #STBOT,R6  
;CLR @#PS  
;MOV #100000,R0 ;LOAD MULTIPLICAN WITH 100000  
;MUL #100000,R0 ;MULTIPLY 100000 BY #100000  
;MOV @#PS,SPSW ;SAVE PS  
;CMPB #1,SPSW ;IS PS = 1  
;BEQ 1\$

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 760 <=====

027400	012742	000644	
027404	005242		
027406	000000		
4082	027410	022700	040000
4083	027414	001404	

1\$: MOV #644,-(R2)  
INC -(R2)  
HALT  
CMP #40000,R0  
BEQ 2\$

;MOVE TO MAILBOX # \*\*\*\*\* 644 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;PS IS WRONG  
;IS HIGH ORDER = 40000

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 751 <=====

027416	012742	000645	
027422	005242		
027424	000000		
4084	027426	022701	000000
4085	027432	001404	

2\$: MOV #645,-(R2)  
INC -(R2)  
HALT  
CMP #0,R1  
BEQ TST274

;MOVE TO MAILBOX # \*\*\*\*\* 645 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;HIGH ORDER IS WRONG  
;IS LOWER = 0

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 742 <=====

027434	012742	000646
027440	005242	
027442	000000	

MOV #646,-(R2)  
INC -(R2)  
HALT

;MOVE TO MAILBOX # \*\*\*\*\* 646 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;LOW ORDER IS WRONG  
;OR SEQUENCE ERROR

4086
4087
4088
4089

;TEST MSB OF LOWER PRODUCT CLEAR C-BIT  
;MODE 2 /REG7

027444	005212		
027446	022712	000274	
027452	001031		
4090	027454	012700	070707
'091	027460	070027	070707
4092	027464	013767	177776
4093	027472	122767	000001
4094	027500	001404	

;TEST 274 MUL 70707 \* #70707 = 31221 44261 PS=1  
;TST274: INC (R2) ;UPDATE TEST NUMBER  
;CMP #274, (R2) ;SEQUENCE ERROR?  
;BNE TST275-10 ;BR TO ERROR HALT ON SEQ ERROR  
;MOV #70707,R0 ;LOAD MULTIPLICAN WITH 70707  
;MUL #70707,R0 ;MULTIPLY 70707 BY #70707  
;MOV @#PS,SPSW ;SAVE PS = 1  
;CMPB #1,SPSW ;IS PS = 1  
;BEQ 1\$

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION <=====

027502 012742 000647      MOV #647,-(R2) ; WHICH FOLLOWS W/ 764   
 027506 005242      INC -(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 647 \*\*\*\*\*   
 027510 000000      HALT ; SET MSGTYP TO FATAL ERROR   
 4095 027512 022700 031221      1\$: CMP #31221,R0 ; PS IS WRONG   
 4096 027516 001404      BEQ 2\$ ; IS HIGH ORDER =31221  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 ; CONDITIONAL BRANCH INST. AND   
 ; REPLACE THE MOVE INSTRUCTION   
 ; WHICH FOLLOWS W/ 755  
 027520 012742 000650      MOV #650,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 650 \*\*\*\*\*   
 027524 005242      INC -(R2) ; SET MSGTYP TO FATAL ERROR   
 027526 000000      HALT ; HIGH ORDER IS WRONG   
 4097 027530 022701 044261      2\$: CMP #44261,R1 ; IS LOWER ORDER =44261  
 4098 027534 001404      BEQ TST275 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 ; CONDITIONAL BRANCH INST. AND   
 ; REPLACE THE MOVE INSTRUCTION   
 ; WHICH FOLLOWS W/ 746  
 027536 012742 000651      MOV #651,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 651 \*\*\*\*\*   
 027542 005242      INC -(R2) ; SET MSGTYP TO FATAL ERROR   
 027544 000000      HALT ; LOW ORDER IS WRONG   
 ; OR SEQUENCE ERROR  
 4099  
 4100  
 4101  
 4102 :STORE UPPER PRODUCT AND SET C-BIT NEG #  
 :MODE 2 /REG 7  
 :\*\*\*\*\*  
 :TEST 275      MUL 107070 \* #107070 = 31222 26100 PS=1  
 :\*\*\*\*\*  
 027546 005212      TST275: INC (R2) ; UPDATE TEST NUMBER  
 027550 022712 000275      CMP #275,(R2) ; SEQUENCE ERROR?  
 027554 001031      BNE TST276-10 ; BR TO ERROR HALT ON SEQ ERROR  
 4103 027556 012700 107070      MOV #107070,R0 ; LOAD MULTIPLICAN WITH 107070  
 4104 027562 070027 107070      MUL #107070,R0 ; MULTIPLY 107070 BY #107070  
 4105 027566 013767 177776 006674      MOV @#PS,SPSW ; SAVE PS  
 4106 027574 122767 000001 006666      CMPB #1,SPSW ; IS PS = 1  
 4107 027602 001404      BEQ 1\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 ; CONDITIONAL BRANCH INST. AND   
 ; REPLACE THE MOVE INSTRUCTION   
 ; WHICH FOLLOWS W/ 764  
 027604 012742 000652      MOV #652,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 652 \*\*\*\*\*   
 027610 005242      INC -(R2) ; SET MSGTYP TO FATAL ERROR   
 027612 000000      HALT ; PS IS WRONG   
 4108 027614 022700 031222      1\$: CMP #31222,R0 ; IS HIGH ORDER = 31222  
 4109 027620 001404      BEQ 2\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 ; CONDITIONAL BRANCH INST. AND   
 ; REPLACE THE MOVE INSTRUCTION   
 ; WHICH FOLLOWS W/ 755  
 027622 012742 000653      MOV #653,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 653 \*\*\*\*\*   
 027626 005242      INC -(R2) ; SET MSGTYP TO FATAL ERROR   
 027630 000000      HALT ; IS LOW ORDER = 26100  
 4110 027632 022701 026100      2\$: CMP #26100,R1 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 4111 027636 001404      BEQ TST276 ; CONDITIONAL BRANCH INST. AND

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REPLACE THE MOVE INSTRUCTION <=====  

WHICH FOLLOWS W/ 746 <=====  

027640 012742 000654      MOV   #654,-(R2) :MOVE TO MAILBOX # ***** 654 *****  

027644 005242             INC   -(R2)  :SET MSGTYP TO FATAL ERROR  

027646 000000             HALT :LOW ORDER IS WRONG  

                            : OR SEQUENCE ERROR  

4112                           :PUT MULTIPLIER IN R12 AND TEST SIGN FOR ZERO  

4113                           :MODE 2 /REG 7  

4114                           :*****  

                           :TEST 276      MUL  77777 * #100000 = 140000 100000 PS=11  

                           :*****  

027650 005212             TST276: INC  (R2) :UPDATE TEST NUMBER  

027652 022712             CMP   #276,(R2) :SEQUENCE ERROR?  

027656 001031             BNE   TST277-10 :BR TO ERROR HALT ON SEQ ERROR  

4115 027660 012700             MOV   #77777,R0 :LOAD MULTIPLICAN WITH 77777  

4116 027664 070027             MUL   #100000,R0 :MULTIPLY 77777 BY #100000  

4117 027670 013767             MOV   @#PS,SPSW :SAVE PS  

4118 027676 122767             CMPB  #11,SPSW :IS PS = 11  

4119 027704 001404             BEQ   1$  

                            : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  

                            : CONDITIONAL BRANCH INST. AND <=====  

                            : REPLACE THE MOVE INSTRUCTION <=====  

                            : WHICH FOLLOWS W/ 764 <=====  

027706 012742 000655      MOV   #655,-(R2) :MOVE TO MAILBOX # ***** 655 *****  

027712 005242             INC   -(R2)  :SET MSGTYP TO FATAL ERROR  

027714 000000             HALT :PS IS WRONG  

4120 027716 022700             1$:   CMP   #140000,R0 :IS HIGH ORDER = 140000  

4121 027722 001404             BEQ   2$  

                            : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  

                            : CONDITIONAL BRANCH INST. AND <=====  

                            : REPLACE THE MOVE INSTRUCTION <=====  

                            : WHICH FOLLOWS W/ 755 <=====  

027724 012742 000656      MOV   #656,-(R2) :MOVE TO MAILBOX # ***** 656 *****  

027730 005242             INC   -(R2)  :SET MSGTYP TO FATAL ERROR  

027732 000000             HALT :HIGH ORDER IS WRONG  

4122 027734 022701             2$:   CMP   #100000,R1 :IS LOW ORDER = 100000  

4123 027740 001404             BEQ   TST277  

                            : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  

                            : CONDITIONAL BRANCH INST. AND <=====  

                            : REPLACE THE MOVE INSTRUCTION <=====  

                            : WHICH FOLLOWS W/ 746 <=====  

027742 012742 000657      MOV   #657,-(R2) :MOVE TO MAILBOX # ***** 657 *****  

027746 005242             INC   -(R2)  :SET MSGTYP TO FATAL ERROR  

027750 000000             HALT :LOW ORDER IS WRONG  

                            : OR SEQUENCE ERROR  

4124                           :SET Z-BIT R17 = 0  

4125                           :MODE 2 /REG 7  

4126                           :*****  

4127                           :TEST 277      MUL  -1 * #0 = 0 0 PS=4  

                           :*****  

027752 005212             TST277: INC  (R2) :UPDATE TEST NUMBER  

027754 022712             CMP   #277,(R2) :SEQUENCE ERROR?  

027760 001031             BNE   TST300-10 :BR TO ERROR HALT ON SEQ ERROR  

4128 027762 012700             MOV   #-1,R0 :LOAD MULTIPLICAN WITH -1  

4129 027766 070027             MUL   #0,R0 :MULTIPLY -1 BY #0  

4130 027772 013767             MOV   @#PS,SPSW :SAVE PS

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4131 030000 122767 000004 006462 CMPB #4,SPSW ;IS PS = 4  
 4132 030006 001404 BEQ 1\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                           ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 764 <=====  
                           ; MOVE TO MAILBOX # \*\*\*\*\* 660 \*\*\*\*\*  
                           ; SET MSGTYP TO FATAL ERROR  
                           ; PS IS WRONG  
                           ; IS HIGH ORDER = 0 <=====  
                           ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                           ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 755 <=====  
                           ; MOVE TO MAILBOX # \*\*\*\*\* 661 \*\*\*\*\*  
                           ; SET MSGTYP TO FATAL ERROR  
                           ; HIGH ORDER IS WRONG  
                           ; IS LOW ORDER = 0 <=====  
                           ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                           ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 746 <=====  
                           ; MOVE TO MAILBOX # \*\*\*\*\* 662 \*\*\*\*\*  
                           ; SET MSGTYP TO FATAL ERROR  
                           ; LOW ORDER IS WRONG  
                           ; OR SEQUENCE ERROR <=====  
                           ; TEST UPPER PRODUCT FOR ALL ONES,CLEAR C-BIT  
                           ; MODE 2 /REG 7  
 4137  
 4138  
 4139  
 4140 ;\*\*\*\*\*  
       ;TEST 300           MUL -1 \* #77777 = 100001 100001 PS=10  
       ;\*\*\*\*\*  
       ;\*\*\*\*\*  
 030054 005212 TST300: INC (R2) ;UPDATE TEST NUMBER  
 030056 022712 000300 CMP #300,(R2) ;SEQUENCE ERROR?  
 030062 001031 BNE TST301-10 ;BR TO ERROR HALT ON SEQ ERROR  
 4141 030064 012701 177777 MOV #-1,R1 ;LOAD MULTIPLICAN WITH -1  
 4142 030070 070127 077777 MUL #77777,R1 ;MULTIPLY -1 BY #77777  
 4143 030074 013767 177776 006366 MOV @#PS,SPSW ;SAVE PS  
 4144 030102 122767 000010 006360 CMPB #10,SPSW ;IS PS = 10  
 4145 030110 001404 BEQ 1\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                           ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 764 <=====  
                           ; MOVE TO MAILBOX # \*\*\*\*\* 663 \*\*\*\*\*  
                           ; SET MSGTYP TO FATAL ERROR  
                           ; PS IS WRONG  
                           ; IS HIGH ORDER = 100001 <=====  
                           ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                           ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 755 <=====  
                           ; MOVE TO MAILBOX # \*\*\*\*\* 664 \*\*\*\*\*  
                           ; SET MSGTYP TO FATAL ERROR  
 030112 012742 000663 MOV #663,-(R2) ;  
 030116 005242 INC -(R2) ;  
 030120 000000 HALT ;  
 4146 030122 022701 100001 1\$: CMP #100001,R1 ;  
 4147 030126 001404 BEQ 2\$ ; IS HIGH ORDER = 100001 <=====  
                           ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                           ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 755 <=====  
                           ; MOVE TO MAILBOX # \*\*\*\*\* 664 \*\*\*\*\*  
                           ; SET MSGTYP TO FATAL ERROR

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T300 MUL -1 \* #77777 = 100001 100001 PS=10

B 14

SEQ 0170

030136 000000  
4148 030140 022701 100001 2\$: HALT  
4149 030144 001404 CMP BEQ #100001,R1 ;HIGHT ORDER IS WRONG  
;IS LOW ORDER = 100001  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 746 <=====  
030146 012742 000665 MOV #665,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 665 \*\*\*\*\*  
030152 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
030154 000000 HALT ;LOW ORDER IS WRONG  
; OR SEQUENCE ERROR  
4150 ;MODE 2 /REG 7  
4151 ;TEST 301 MUL 2 \* #2 = 0 4 PS=0  
;\*\*\*\*\*  
030156 005212 TST301: INC (R2) ;UPDATE TEST NUMBER  
030160 022712 000301 CMP #301,(R2) ;SEQUENCE ERROR?  
030164 001031 BNE TST302-10 ;BR TO ERROR HALT ON SEQ ERROR  
4152 030166 012700 000002 MOV #2,R0 ;LOAD MULTIPLICAN WITH 2  
4153 030172 070027 000002 MUL #2,R0 ;MULTIPLY 2 BY #2  
4154 030176 013767 177776 006264 MOV @PS,SPSW ;SAVE PS  
4155 030204 122767 000000 006256 CMPB #0,SPSW ;IS PS=0  
4156 030212 001404 BEQ 1\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 764 <=====  
030214 012742 000666 MOV #666,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 666 \*\*\*\*\*  
030220 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
030222 000000 HALT ;PS IS WRONG  
4157 030224 022700 000000 1\$: CMP #0,R0 ;IS HIGH ORDER =0  
4158 030230 001404 BEQ 2\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 755 <=====  
030232 012742 000667 MOV #667,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 667 \*\*\*\*\*  
030236 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
030240 000000 HALT ;HIGH ORDER IS WRONG  
4159 030242 022701 000004 2\$: CMP #4,R1 ;IS LOW ORDER =4  
4160 030246 001404 BEQ TST302 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 746 <=====  
030250 012742 000670 MOV #670,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 670 \*\*\*\*\*  
030254 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
030256 000000 HALT ;LOW ORDER IS WRONG  
; OR SEQUENCE ERROR  
4161 ;MODE 2 /REG 7  
4162 ;TEST 302 MUL 1 \* #-1 = -1 -1 PS=10  
4163 ;\*\*\*\*\*  
030260 005212 TST302: INC (R2) ;UPDATE TEST NUMBER  
030262 022712 000302 CMP #302,(R2) ;SEQUENCE ERROR?  
030266 001031 BNE TST303-10 ;BR TO ERROR HALT ON SEQ ERROR

4164 030270 012700 000001      MOV #1, R0 ;LOAD MULTIPLICAN WITH 1  
 4165 030274 070027 177777      MUL #-1, R0 ;MULTIPLY 1 BY #-1  
 4166 030300 013767 177776 006162      MOV @#PS, SPSW ;SAVE PS  
 4167 030306 122767 000010 006154      CMPB #10, SPSW ;IS PS =10  
 4168 030314 001404      BEQ 1\$

                                        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
  CONDITIONAL BRANCH INST. AND  
  REPLACE THE MOVE INSTRUCTION  
  WHICH FOLLOWS W/ 764      <=====

030316 012742 000671      MOV #671, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 671 \*\*\*\*\*  
 030322 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 030324 000000      HALT ;PS IS WRONG  
 4169 030326 022700 177777      1\$: CMP #-1, R0 ;IS HIGH ORDER =-1  
 4170 030332 001404      BEQ 2\$

                                        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
  CONDITIONAL BRANCH INST. AND  
  REPLACE THE MOVE INSTRUCTION  
  WHICH FOLLOWS W/ 755      <=====

030334 012742 000672      MOV #672, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 672 \*\*\*\*\*  
 030340 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 030342 000000      HALT ;HIGH ORDER IS WRONG  
 4171 030344 022701 177777      2\$: CMP #-1, R1 ;IS LOW ORDER =-1  
 4172 030350 001404      TST303

                                        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
  CONDITIONAL BRANCH INST. AND  
  REPLACE THE MOVE INSTRUCTION  
  WHICH FOLLOWS W/ 746      <=====

030352 012742 000673      MOV #673, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 673 \*\*\*\*\*  
 030356 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 030360 000000      HALT ;LOW ORDER IS WRONG  
 4173                                 ; OR SEQUENCE ERROR  
 4174

                                        ; MODE 2 /REG 7

;\*\*\*\*\* TEST 303 MUL -1 \* #100000 = 0 100000 PS=1\*\*\*\*\*

030362 005212      TST303: INC (R2) ;UPDATE TEST NUMBER  
 030364 022712 000303      CMP #303, (R2) ;SEQUENCE ERROR?  
 030370 001031      BNE TST304-10 ;BR TO ERROR HALT ON SEQ ERROR  
 4175 030372 012700 177777      MOV #-1, R0 ;LOAD MULTIPLICAN WITH -1  
 4176 030376 070027 100000      MUL #100000, R0 ;MULTIPLY -1 BY 100000  
 4177 030402 013767 177776 006060      MOV @#PS, SPSW ;SAVE PS  
 4178 030410 122767 000001 006052      CMPB #1, SPSW ;IS PS =1  
 4179 030416 001404      BEQ 1\$

                                        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
  CONDITIONAL BRANCH INST. AND  
  REPLACE THE MOVE INSTRUCTION  
  WHICH FOLLOWS W/ 764      <=====

030420 012742 000674      MOV #674, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 674 \*\*\*\*\*  
 030424 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 030426 000000      HALT ;PS IS WRONG  
 4180 030430 022700 000000      1\$: CMP #0, R0 ;IS HIGH ORDER = 0  
 4181 030434 001404      BEQ 2\$

                                        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
  CONDITIONAL BRANCH INST. AND  
  REPLACE THE MOVE INSTRUCTION  
  WHICH FOLLOWS W/ 755      <=====

030436 012742 000675      MOV #675, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 675 \*\*\*\*\*

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T303 MUL -1 \* #100000 = 0 100000 PS=1

D 14

SEQ 0172

030442 005242  
030444 000000  
4182 030446 022701 100000  
4183 030452 001404

2\$: INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;HIGH ORDER IS WRONG  
CMP #100000,R1 ;IS LOW ORDER =100000  
BEQ TST304

030454 012742 000676  
030460 005242  
030462 000000

MOV #676,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 676 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;LOW ORDER IS WRONG  
; OR SEQUENCE ERROR

4184  
4185  
4186  
4187  
4188

.SBTTL DIV USING DM6 REG ?

030464 005212  
030466 022712 000304  
030472 001035  
4189 030474 012700 000000  
4190 030500 012701 052525  
4191 030504 012703 036476  
4192 030510 071067 005762  
4193 030514 013767 177776 005746  
4194 030522 122767 000000 005740  
4195 030530 001404

TST304: INC (R2) ;UPDATE TEST NUMBER  
CMP #304,(R2) ;SEQUENCE ERROR?  
BNE TST305-10 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #0,R0 ;LOAD HIGH ORDER WITH R0  
MOV #52525,R1 ;LOAD LOW ORDER WITH 52525  
MOV #S1,R3 ;SET UP R3  
DIV S1,R0 ;DIVIDE BY S1  
MOV @#PS,SPSW ;SAVE PS  
CMPB #0,SPSW ;IS PS=0  
BEQ 1\$

030532 012742 000677  
030536 005242  
030540 000000  
4196 030542 022700 025252  
4197 030546 001404

1\$: MOV #677,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 677 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;PS IS WRONG  
CMP #25252,R0 ;IS QUOTIENT =25252  
BEQ 2\$

030550 012742 000700  
030554 005242  
030556 000000  
4198 030560 022701 000001  
4199 030564 001404

2\$: MOV #700,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 700 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;QUOTIENT IS WRONG  
CMP #1,R1 ;IS REMAINDER =1  
BEQ TST305

030566 012742 000701  
030572 005242  
030574 000000

MOV #701,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 701 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;REMAINDER IS WRONG  
; OR SEQUENCE ERROR

4200  
4201

.SBTTL DIV USING DM7 REG ?

4202

```

;***** TEST 305 DUV 0 52525/@S2 =25252 REM=1 PS=0 *****
;TST305: INC (R2) ;UPDATE TEST NUMBER
          CMP #305,(R2) ;SEQUENCE ERROR?
          BNE TST306-10 ;BR TO ERROR HALT ON SEQ ERROR
          MOV #0,R0 ;LOAD HIGH ORDER WITH R0
          MOV #52525,R1 ;LOAD LOW ORDER WITH 52525
          MOV #S2,R4 ;SET UP R4
          DIV @S2,R0 ;DIVIDE BY @S2
          MOV @PS,SPSW ;SAVE PS
          CMPB #0,SPSW ;IS PS=0

          BEQ 1$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
          ; CONDITIONAL BRANCH INST. AND <=====
          ; REPLACE THE MOVE INSTRUCTION <=====
          ; WHICH FOLLOWS W/ 760 <=====

          MOV #702,-(R2) ;MOVE TO MAILBOX # ***** 702 *****
          INC -(R2) ;SET MSGTYP TO FATAL ERROR
          HALT ;PS IS WRONG
          CMP #25252,R0 ;IS QUOTIENT =25252

          BEQ 1$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
          ; CONDITIONAL BRANCH INST. AND <=====
          ; REPLACE THE MOVE INSTRUCTION <=====
          ; WHICH FOLLOWS W/ 751 <=====

          MOV #703,-(R2) ;MOVE TO MAILBOX # ***** 703 *****
          INC -(R2) ;SET MSGTYP TO FATAL ERROR
          HALT ;QUOTIENT IS WRONG
          CMP #1,R1 ;IS REMINDER =1
          BEQ TST306 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
          ; CONDITIONAL BRANCH INST. AND <=====
          ; REPLACE THE MOVE INSTRUCTION <=====
          ; WHICH FOLLOWS W/ 742 <=====

          MOV #704,-(R2) ;MOVE TO MAILBOX # ***** 704 *****
          INC -(R2) ;SET MSGTYP TO FATAL ERROR
          HALT ;REMINDER IS WRONG
          HALT ; OR SEQUENCE ERROR

          .SBTLL DIV USING DM3 REG 7
          ;CLEAR V-BIT MODE 3 REG 7

;***** TEST 306 DIV 0 52525/@S1 =25252 REM=1 PS=0 *****
;TST306: INC (R2) ;UPDATE TEST NUMBER
          CMP #306,(R2) ;SEQUENCE ERROR?
          BNE TST307-10 ;BR TO ERROR HALT ON SEQ ERROR
          MOV #0,R0 ;LOAD HIGH ORDER WITH R0
          MOV #52525,R1 ;LOAD LOW ORDER WITH 52525
          MOV #S1,R3 ;SET UP R3
          DIV @S1,R0 ;DIVIDE BY @S1
          MOV @PS,SPSW ;SAVE PS
          CMPB #0,SPSW ;IS PS=0

          BEQ 1$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====

```

4214

4215

4216

4217

4218

030756 012742 000705      MOV #705,-(R2) ; CONDITIONAL BRANCH INST. AND  
 030762 005242      INC -(R2) ; REPLACE THE MOVE INSTRUCTION  
 030764 000000      HALT ; WHICH FOLLOWS W/ 760  
 4226 030766 022700 025252      1\$: CMP #25252,R0 ; MOVE TO MAILBOX # \*\*\*\*\* 705 \*\*\*\*\*  
 4227 030772 001404      BEQ 2\$ ; SET MSGTYP TO FATAL ERROR  
; PS IS WRONG  
; IS QUOTIENT =25252  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 751  
030774 012742 000706      MOV #706,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 706 \*\*\*\*\*  
031000 005242      INC -(R2) ; SET MSGTYP TO FATAL ERROR  
031002 000000      HALT ; QUOTIENT IS WRONG  
4228 031004 022701 000001      2\$: CMP #1,R1 ; IS REMAINDER =1  
4229 031010 001404      BEQ TST307 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 742  
031012 012742 000707      MOV #707,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 707 \*\*\*\*\*  
031016 005242      INC -(R2) ; SET MSGTYP TO FATAL ERROR  
031020 000000      HALT ; REMAINDER IS WRONG  
; OR SEQUENCE ERROR  
4230  
4231  
4232  
4233 .SBTTL DIV USING DMO REG 4  
; MODE 0 REG 2  
:\*\*\*\*\* TEST 307 DIV 0 52525 /R4=25252 REM=1 PS=0 :\*\*\*\*\*  
031022 005212      TST307: INC (R2) ; UPDATE TEST NUMBER  
031024 022712 000307      CMP #307,(R2) ; SEQUENCE ERROR?  
031030 001034      BNE TST310-10 ; BR TO ERROR HALT ON SEQ ERROR  
4234 031032 012700 000000      MOV #0,R0 ; LOAD HIGH ORDER WITH 0  
4235 031036 012701 052525      MOV #52525,R1 ; LOAD LOW ORDER WITH 52525  
4236 031042 012704 000002      MOV #2,R4 ; SET UP R4  
4237 031046 071004      DIV R4,R0 ; DIVIDE BY R4  
4238 031050 013767 177776 005412      MOV @PS,SPSW ; SAVE PS  
4239 031056 122767 000000 005404      CMPB #0,SPSW ; IS PS=0  
4240 031064 001404      BEQ 1\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 761  
031066 012742 000710      MOV #710,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 710 \*\*\*\*\*  
031072 005242      INC -(R2) ; SET MSGTYP TO FATAL ERROR  
031074 000000      HALT ; PS IS WRONG  
4241 031076 022700 025252      1\$: CMP #25252,R0 ; IS QUOTIENT=25252  
4242 031102 001404      BEQ 2\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 752  
031104 012742 000711      MOV #711,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 711 \*\*\*\*\*  
031110 005242      INC -(R2) ; SET MSGTYP TO FATAL ERROR  
031112 000000      HALT ; QUOTIENT IS WRONG

4243 031114 022701 000001      2\$:      CMP      #1,R1      ;IS REMAINDER =1  
 4244 031120 001404                BEQ      TST310      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 $\cdot$                                          CONDITIONAL BRANCH INST. AND      <=====  
 $\cdot$                                          REPLACE THE MOVE INSTRUCTION      <=====  
 $\cdot$                                          WHICH FOLLOWS W/ 743      <=====  
 $\cdot$   
 031122 012742 000712      MOV      #712,-(R2)      ;MOVE TO MAILBOX # \*\*\*\*\* 712 \*\*\*\*\*  
 031126 005242                INC      -(R2)      ;SET MSGTYP TO FATAL ERROR  
 031130 000000                HALT      ;REMAINDER IS WRONG  
 $\cdot$                                     ; OR SEQUENCE ERROR  
 4245  
 4246  
 4247  
 4248      .SBTTL DIV USING DM4 REG 3  
 $\cdot$                                     ;MODE 4 REG 3  
 $\cdot$   
 :\*\*\*\*\*  
 :TEST 310      DIV 0 52525 /-(3)=25252 REM=1 PS=0  
 :\*\*\*\*\*  
 031132 005212      INC      (R2)      ;UPDATE TEST NUMBER  
 031134 022712 000310      CMP      #310,(R2)      ;SEQUENCE ERROR?  
 031140 001034      BNE      TST311-10      ;BR TO ERROR HALT ON SEQ ERROR  
 4249 031142 012700 000000      MOV      #0,R0      ;LOAD HIGH ORDER WITH 0  
 4250 031146 012701 052525      MOV      #52525,R1      ;LOAD LOW ORDER WITH 52525  
 4251 031152 012703 036500      MOV      #S1+2,R3      ;SET UP R3  
 4252 031156 071043      DIV      -(R3),R0      ;DIVIDE BY -(3)  
 4253 031160 013767 177776      MOV      @#PS,SPSW      ;SAVE PS  
 4254 031166 122767 000000      CMPB     #0,SPSW      ;IS PS=0  
 4255 031174 001404      BEQ      1\$      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 $\cdot$                                          CONDITIONAL BRANCH INST. AND      <=====  
 $\cdot$                                          REPLACE THE MOVE INSTRUCTION      <=====  
 $\cdot$                                          WHICH FOLLOWS W/ 761      <=====  
 031176 012742 000713      MOV      #713,-(R2)      ;MOVE TO MAILBOX # \*\*\*\*\* 713 \*\*\*\*\*  
 031202 005242                INC      -(R2)      ;SET MSGTYP TO FATAL ERROR  
 031204 000000                HALT      ;PS IS WRONG  
 4256 031206 022700 025252      1\$:      CMP      #25252,R0      ;IS QUOTIENT =25252  
 $\cdot$                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 $\cdot$                                          CONDITIONAL BRANCH INST. AND      <=====  
 $\cdot$                                          REPLACE THE MOVE INSTRUCTION      <=====  
 $\cdot$                                          WHICH FOLLOWS W/ 752      <=====  
 031214 012742 000714      MOV      #714,-(R2)      ;MOVE TO MAILBOX # \*\*\*\*\* 714 \*\*\*\*\*  
 031220 005242                INC      -(R2)      ;SET MSGTYP TO FATAL ERROR  
 031222 000000                HALT      ;QUOTIENT IS WRONG  
 4258 031224 022701 000001      2\$:      CMP      #1,R1      ;IS REMAINDER =1  
 $\cdot$                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 $\cdot$                                          CONDITIONAL BRANCH INST. AND      <=====  
 $\cdot$                                          REPLACE THE MOVE INSTRUCTION      <=====  
 $\cdot$                                          WHICH FOLLOWS W/ 743      <=====  
 031232 012742 000715      MOV      #715,-(R2)      ;MOVE TO MAILBOX # \*\*\*\*\* 715 \*\*\*\*\*  
 031236 005242                INC      -(R2)      ;SET MSGTYP TO FATAL ERROR  
 031240 000000                HALT      ;REMAINDER IS WRONG  
 $\cdot$                                     ; OR SEQUENCE ERROR  
 4260      .SBTTL DIV USING DM5 REG 4  
 4261      ;MODE 5 REG 4  
 4262      :\*\*\*\*\*  
 :TEST 311      DIV 0 52525 /@-(4)=25252 REM=1 PS=0  
 :\*\*\*\*\*

T311 DIV 0 52525 /@-(4)=25252 REM=1 PS=0

SEQ 0176

031242 005212	TST311: INC (R2)	:UPDATE TEST NUMBER	<=====
031244 022712 000311	CMP #311, (R2)	:SEQUENCE ERROR?	<=====
031250 001034	BNE TST312-10	:BR TO ERROR HALT ON SEQ ERROR	<=====
4263 031252 012700 000000	MOV #0, R0	:LOAD HIGH ORDER WITH 0	<=====
4264 031256 012701 052525	MOV #52525, R1	:LOAD LOW ORDER WITH 52525	<=====
4265 031262 012704 036502	MOV #S2+2, R4	:SET UP R4	<=====
4266 031266 071054	DIV @-(R4), R0	:DIVIDE BY @-(4)	<=====
4267 031270 013767 177776 005172	MOV @PS, SPSW	:SAVE PS	<=====
4268 031276 122767 000000 005164	CMPB #0, SPSW	:IS PS = 0	<=====
4269 031304 001404	BEQ 1\$		
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 761 <=====			
031306 012742 000716	MOV #716, -(R2)	:MOVE TO MAILBOX # ***** 716 *****	<=====
031312 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
031314 000000	HALT	:PS IS WRONG	<=====
4270 031316 022700 025252	1\$: CMP #25252, R0	:IS QUOTIENT =25252	<=====
4271 031322 001404	BEQ 2\$		
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 752 <=====			
031324 012742 000717	MOV #717, -(R2)	:MOVE TO MAILBOX # ***** 717 *****	<=====
031330 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
031332 000000	HALT	:QUOTIENT IS WRONG	<=====
4272 031334 022701 000001	2\$: CMP #1, R1	:IS REMAINDER =1	<=====
4273 031340 001404	BEQ TST312		
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 743 <=====			
031342 012742 000720	MOV #720, -(R2)	:MOVE TO MAILBOX # ***** 720 *****	<=====
031346 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====
031350 000000	HALT	:REMAINDER IS WRONG ; OR SEQUENCE ERROR	<=====
4274	; MODE 5 REG 4		
4275			
4276			
***** TEST 312 *****			
DIV 0 52525 /@-(4)=100000 REM=0 PS=2			
031352 005212	TST312: INC (R2)	:UPDATE TEST NUMBER	<=====
031354 022712 000312	CMP #312, (R2)	:SEQUENCE ERROR?	<=====
031360 001034	BNE TST313-10	:BR TO ERROR HALT ON SEQ ERROR	<=====
4277 031362 012700 052525	MOV #52525, R0	:LOAD HIGH ORDER WITH 52525	<=====
4278 031366 012704 036502	MOV #S2+2, R4	:SET UP R4	<=====
4279 031372 012701 000000	MOV #0, R1	:LOAD LOW ORDER WITH 0	<=====
4280 031376 071054	DIV @-(R4), R0	:DIVIDE BY @-(4)	<=====
4281 031400 013767 177776 005062	MOV @PS, SPSW	:SAVE PS	<=====
4282 031406 122767 000002 005054	CMPB #2, SPSW	:IS PS=0	<=====
4283 031414 001404	BEQ 1\$		
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 761 <=====			
031416 012742 000721	MOV #721, -(R2)	:MOVE TO MAILBOX # ***** 721 *****	<=====
031422 005242	INC -(R2)	:SET MSGTYP TO FATAL ERROR	<=====

031424	000000		HALT		:PS IS WRONG	
4284	031426	022700	052525	1\$: CMP BEQ	#52525,R0 2\$	:IS QUOTIENT =52525
4285	031432	001404				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 752
031434	012742	000722	MOV INC HALT	#722,-(R2) -(R2)	: MOVE TO MAILBOX # ***** 722 ***** :SET MSGTYP TO FATAL ERROR	<=====
031440	005242		CMP	#0,R1	:QUOTIENT IS WRONG	<=====
031442	000000		BEQ	TST313	:IS REMAINDER =0	<=====
4286	031444	022701	000000	2\$: CMP BEQ		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 743
4287	031450	001404				<=====
031452	012742	000723	MOV INC HALT	#723,-(R2) -(R2)	: MOVE TO MAILBOX # ***** 723 ***** :SET MSGTYP TO FATAL ERROR	<=====
031456	005242				:REMAINDER IS WRONG	<=====
031460	000000				: OR SEQUENCE ERROR	<=====
4288						
4289						
4290						
4291						
031462	005212					
031464	022712	000313	TST313:	INC (R2) CMP #313,(R2) BNE TST314-10 MOV #1,R0 MOV #-4,R1 DIV #2,R0 MOV @#PS,SPSW CMPB #10,SPSW BEQ 1\$	: UPDATE TEST NUMBER :SEQUENCE ERROR? :BR TO ERROR HALT ON SEQ ERROR :LOAD HIGH ORDER WITH -1 :LOAD LOW ORDER WITH -4 :DIVIDE BY #2 :SAVE PS :IS PS =10	
031470	001033					
4292	031472	012700	177777			
4293	031476	012701	177774			
4294	031502	071027	000002			
4295	031506	013767	177776	004754		
4296	031514	122767	000010	004746		
4297	031522	001404				
031524	012742	000724	MOV INC HALT	#724,-(R2) -(R2)	: MOVE TO MAILBOX # ***** 724 ***** :SET MSGTYP TO FATAL ERROR	<=====
031530	005242		CMP	#-2,R0	:PS IS WRONG	<=====
031532	000000		BEQ	2\$	:IS QUOTIENT = -2	<=====
4298	031534	022700	177776	1\$: CMP		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 753
4299	031540	001404		BEQ		<=====
031542	012742	000725	MOV INC HALT	#725,-(R2) -(R2)	: MOVE TO MAILBOX # ***** 725 ***** :SET MSGTYP TO FATAL ERROR	<=====
031546	005242		CMP	#0,R1	:QUOTIENT IS WRONG	<=====
031550	000000		BEQ	TST314	:IS REMAINDER =0	<=====
4300	031552	022701	000000	2\$: CMP		: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 744
4301	031556	001404		BEQ		<=====

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T313 DIV -1 -4/#2= -2 REM=0 PS=10

J 14

SEQ 0178

031560 012742 000726  
031564 005242  
031566 000000

MOV #726,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 726 \*\*\*\*\*  
INC -(R2) ;SET MSGTYP TO FATAL ERROR  
HALT ;REMAINDER IS WRONG  
; OR SEQUENCE ERROR

4302  
4303  
4304

;MODE 2 REG 7

;TEST 314 DIV 0 0/ #1 = 0 REM=0 PS=4

031570 005212 000314  
031572 022712 000314  
031576 001033 000000  
4305 031600 012700 000000  
4306 031604 012701 000000  
4307 031610 071027 000001  
4308 031614 013767 177776 004646  
4309 031622 122767 000004 004640  
4310 031630 001404

TST314: INC (R2) ;UPDATE TEST NUMBER  
CMP #314,(R2) ;SEQUENCE ERROR?  
BNE TST315-10 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #0,R0 ;LOAD HIGH ORDER WITH 0  
MOV #0,R1 ;LOAD LOW ORDER WITH 0  
DIV #1,R0 ;DIVIDE BY #1  
MOV @#PS,SPSW ;SAVE PS  
CMPB #4,SPSW ;IS PS =4  
BEQ 1\$ ;

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 762 <=====

031632 012742 000727  
031636 005242  
031640 000000  
4311 031642 022700 000000  
4312 031646 001404

MOV #727,-(R2)  
INC -(R2)  
HALT  
1\$: CMP #0,R0  
BEQ 2\$

;MOVE TO MAILBOX # \*\*\*\*\* 727 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;PS IS WRONG  
;IS QUOTIENT =0

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 753 <=====

031650 012742 000730  
031654 005242  
031656 000000  
4313 031660 022701 000000  
4314 031664 001404

MOV #730,-(R2)  
INC -(R2)  
HALT  
2\$: CMP #0,R1  
BEQ TST315

;MOVE TO MAILBOX # \*\*\*\*\* 730 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;QUOTIENT IS WRONG  
;IS REMAINDER =0

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 744 <=====

031666 012742 000731  
031672 005242  
031674 000000

MOV #731,-(R2)  
INC -(R2)  
HALT

;MOVE TO MAILBOX # \*\*\*\*\* 731 \*\*\*\*\*  
;SET MSGTYP TO FATAL ERROR  
;REMAINDER IS WRONG  
; OR SEQUENCE ERROR

4315  
4316  
4317

;MODE 2 REG 7

;TEST 315 DIV 0 52525 / #2=25252 REM=1 PS=0

031676 005212 000315  
031700 022712 000315  
031704 001033 000000  
4318 031706 012700 000000  
4319 031712 012701 052525  
4320 031716 071027 000002  
4321 031722 013767 177776 004540  
4322 031730 122767 000000 004532

TST315: INC (R2) ;UPDATE TEST NUMBER  
CMP #315,(R2) ;SEQUENCE ERROR?  
BNE TST316-10 ;BR TO ERROR HALT ON SEQ ERROR  
MOV #0,R0 ;LOAD HIGH ORDER WITH 0  
MOV #52525,R1 ;LOAD LOW ORDER WITH 52525  
DIV #2,R0 ;DIVIDE BY #2  
MOV @#PS,SPSW ;SAVE PS  
CMPB #0,SPSW ;IS PS =0

4323 031736 001404

BEQ 1\$

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 762 <=====

031740 012742 000732  
 031744 005242  
 031746 000000  
 4324 031750 022700 025252  
 4325 031754 001404

1\$: MOV #732,-(R2)  
 INC -(R2)  
 HALT

CMP #25252,R0  
 BEQ 2\$

; MOVE TO MAILBOX # \*\*\*\*\* 732 \*\*\*\*\*  
 ; SET MSGTYP TO FATAL ERROR  
 ; PS IS WRONG  
 ; IS QUOTIENT =25252

031756 012742 000733  
 031762 005242  
 031764 000000  
 4326 031766 022701 000001  
 4327 031772 001404

2\$: MOV #733,-(R2)  
 INC -(R2)  
 HALT

CMP #1,R1  
 BEQ TST316

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 753 <=====

031774 012742 000734  
 032000 005242  
 032002 000000

MOV #734,-(R2)  
 INC -(R2)  
 HALT

; MOVE TO MAILBOX # \*\*\*\*\* 734 \*\*\*\*\*  
 ; SET MSGTYP TO FATAL ERROR  
 ; REMAINDER IS WRONG  
 ; OR SEQUENCE ERROR

4328

4329

4330

: MODE 2 REG 7

\*\*\*\*\* TEST 316 DIV 25253 0 / #125252=100000 REM=0 PS=10 \*\*\*\*\*

032004 005212  
 032006 022712 000316  
 032012 001033  
 4331 032014 012700 025253  
 4332 032020 012701 000000  
 4333 032024 071027 125252  
 4334 032030 013767 177776 004432  
 4335 032036 122767 000010 004424  
 4336 032044 001404

TST316: INC (R2)  
 CMP #316,(R2)  
 BNE TST317-10  
 MOV #25253,R0  
 MOV #0,R1  
 DIV #125252,R0  
 MOV @#PS,SPSW  
 CMPB #10,SPSW  
 BEQ 1\$

; UPDATE TEST NUMBER  
 ; SEQUENCE ERROR?  
 ; BR TO ERROR HALT ON SEQ ERROR  
 ; LOAD HIGH ORDER WITH 25253  
 ; LOAD LOW ORDER WITH 0  
 ; DIVIDE BY #125252  
 ; SAVE PS  
 ; IS PS =10

032046 012742 000735  
 032052 005242  
 032054 000000  
 4337 032056 022700 100000  
 4338 032062 001404

1\$: MOV #735,-(R2)  
 INC -(R2)  
 HALT

CMP #100000,R0  
 BEQ 2\$

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 762 <=====

; MOVE TO MAILBOX # \*\*\*\*\* 735 \*\*\*\*\*  
 ; SET MSGTYP TO FATAL ERROR  
 ; PS IS WRONG  
 ; IS QUOTIENT =100000

032064 012742 000736  
 032070 005242  
 032072 000000

MOV #736,-(R2)  
 INC -(R2)  
 HALT

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 753 <=====

; MOVE TO MAILBOX # \*\*\*\*\* 736 \*\*\*\*\*  
 ; SET MSGTYP TO FATAL ERROR  
 ; QUOTIENT IS WRONG



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T320 DIV 0 177777/M0=0 REM=0 PS=3

M 14

SEQ 0181

4356 032230 012704 177777  
 4357 032234 012705 000000  
 4358 032240 071427 000000  
 4359 032244 013767 177776 004216  
 4360 032252 042767 000014 004210  
 4361 032260 122767 000003 004202  
 4362 032266 001404

MOV #177777,R4 ;LOAD HIGH ORDER WITH 177777  
 MOV #0,R5 ;LOAD LOW ORDER WITH 0  
 DIV #0,R4 ;DIVIDE BY #2  
 MOV @#PS,SPSW ;SAVE PS  
 BIC #14,SPSW  
 CMPB #3,SPSW ;IS PS =3  
 BEQ TST321

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 757 <=====  
 ; =====<  
 ; =====<  
 ; =====<

032270 012742 000743  
 032274 005242  
 032276 000000

MOV #743,-(R2)  
 INC -(R2)  
 HALT

;MOVE TO MAILBOX # \*\*\*\*\* 743 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;PS IS WRONG  
 ; OR SEQUENCE ERROR

4363  
 4364  
 4365

;\*\*\*\*\* TEST 321 \*\*\*\*\*  
 ;\*\*\*\*\* DIV 0 100000 00000 /#100000 REM=0 PS=2 \*\*\*\*\*  
 ;\*\*\*\*\*  
 ;\*\*\*\*\* TST321: INC (R2) ;UPDATE TEST NUMBER  
 ;\*\*\*\*\* CMP #321,(R2) ;SEQUENCE ERROR?  
 ;\*\*\*\*\* BNE TST322-10 ;BR TO ERROR HALT ON SEQ ERROR  
 ;\*\*\*\*\* MOV #100000,R4 ;LOAD HIGH ORDER WITH 100000  
 ;\*\*\*\*\* MOV #0,R5 ;LOAD LOW ORDER WITH 0  
 ;\*\*\*\*\* DIV #2,R4 ;DIVIDE BY #2  
 ;\*\*\*\*\* MOV @#PS,SPSW ;SAVE PS  
 ;\*\*\*\*\* BIC #14,SPSW  
 ;\*\*\*\*\* CMPB #2,SPSW ;IS PS=2  
 ;\*\*\*\*\* BEQ TST322

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 757 <=====  
 ; =====<  
 ; =====<  
 ; =====<

032300 005212 000321  
 032302 022712  
 032306 001020  
 4366 032310 012704 100000  
 4367 032314 012705 000000  
 4368 032320 071427 000002  
 4369 032324 013767 177776 004136  
 4370 032332 042767 000014 004130  
 4371 032340 122767 000002 004122  
 4372 032346 001404

MOV #744,-(R2)  
 INC -(R2)  
 HALT

;MOVE TO MAILBOX # \*\*\*\*\* 744 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;PS IS WRONG  
 ; OR SEQUENCE ERROR

4373  
 4374  
 4375

;\*\*\*\*\* TEST 322 \*\*\*\*\*  
 ;\*\*\*\*\* DIV 0 77777/#0=0 REM=0 PS=3 \*\*\*\*\*  
 ;\*\*\*\*\*  
 ;\*\*\*\*\* TST322: INC (R2) ;UPDATE TEST NUMBER  
 ;\*\*\*\*\* CMP #322,(R2) ;SEQUENCE ERROR?  
 ;\*\*\*\*\* BNE TST323-10 ;BR TO ERROR HALT ON SEQ ERROR  
 ;\*\*\*\*\* MOV #0,R4 ;LOAD HIGH ORDER WITH 0  
 ;\*\*\*\*\* MOV #77777,R5 ;LOAD LOW ORDER WITH 77777  
 ;\*\*\*\*\* DIV #0,R4 ;DIVIDE BY 0  
 ;\*\*\*\*\* MOV @#PS,SPSW ;SAVE PS  
 ;\*\*\*\*\* BIC #14,SPSW  
 ;\*\*\*\*\* CMPB #3,SPSW ;IS PS =3  
 ;\*\*\*\*\* BEQ 2\$  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 757 <=====  
 ; =====<  
 ; =====<  
 ; =====<

032360 005212 000322  
 032362 022712  
 032366 001053  
 4376 032370 012704 000000  
 4377 032374 012705 077777  
 4378 032400 071427 000000  
 4379 032404 013767 177776 004056  
 4380 032412 042767 000014 004050  
 4381 032420 122767 000003 004042  
 4382 032426 001430



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T323 DIV 25253 0 / #125252=100000 REM=0 PS=10

B 15

SEQ 0183

```

032744 022712 000325      CMP    #325,(R2)      :SEQUENCE ERROR?
032750 001020              BNE    TST326-10     :BR TO ERROR HALT ON SEQ ERROR
4421 032752 012704 177777   MOV    #177777,R4    :LOAD HIGH ORDER WITH 17777
4422 032756 012705 000000   MOV    #0,R5       :LOAD LOW ORDER WITH 0
4423 032762 071427 000000   DIV    #0,R4       :DIVIDE BY #2
4424 032766 013767 177776  003474   MOV    @#PS,SPSW   :SAVE PS
4425 032774 042767 000014  003466   BIC    #14,SPSW
4426 033002 122767 000003  003460   CMPB   #3,SPSW
4427 033010 001404          BEQ    TST326      :IS PS =3

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====  

; CONDITIONAL BRANCH INST. AND                <=====  

; REPLACE THE MOVE INSTRUCTION                <=====  

; WHICH FOLLOWS W/ 757                      <=====

033012 012742 000756      MOV    #756,-(R2)    :MOVE TO MAILBOX # ***** 756 *****
033016 005242              INC    -(R2)        :SET MSGTYP TO FATAL ERROR
033020 000000              HALT
                                         :PS IS WRONG
                                         : OR SEQUENCE ERROR

4428
4429 ;***** TEST 326 DIV 0 100000 000000 /#2=100000 REM=0 PS=2 *****

033022 005212              TST326: INC    (R2)      :UPDATE TEST NUMBER
033024 022712 000326      CMP    #326,(R2)      :SEQUENCE ERROR?
033030 001020              BNE    TST327-10     :BR TO ERROR HALT ON SEQ ERROR
4430 033032 012704 100000   MOV    #100000,R4    :LOAD HIGH ORDER WITH 100000
4431 033036 012705 000000   MOV    #0,R5       :LOAD LOW ORDER WITH 0
4432 033042 071427 000002   DIV    #2,R4       :DIVIDE BY #2
4433 033046 013767 177776  003414   MOV    @#PS,SPSW   :SAVE PS
4434 033054 042767 000014  003406   BIC    #14,SPSW
4435 033062 122767 000002  003400   CMPB   #2,SPSW
4436 033070 001404          BEQ    TST327      :IS PS=2

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====  

; CONDITIONAL BRANCH INST. AND                <=====  

; REPLACE THE MOVE INSTRUCTION                <=====  

; WHICH FOLLOWS W/ 757                      <=====

033072 012742 000757      MOV    #757,-(R2)    :MOVE TO MAILBOX # ***** 757 *****
033076 005242              INC    -(R2)        :SET MSGTYP TO FATAL ERROR
033100 000000              HALT
                                         :PS IS WRONG
                                         : OR SEQUENCE ERROR

4437
4438 ;***** TEST 327 DIV 0 77777 /#0=0 REM=0 PS=3 *****

033102 005212              TST327: INC    (R2)      :UPDATE TEST NUMBER
033104 022712 000327      CMP    #327,(R2)      :SEQUENCE ERROR?
033110 001020              BNE    TST330-10     :BR TO ERROR HALT ON SEQ ERROR
4439 033112 012704 000000   MOV    #0,R4       :LOAD HIGH ORDER WITH 0
4440 033116 012705 077777   MOV    #77777,R5    :LOAD LOW ORDER WITH 77777
4441 033122 071427 000000   DIV    #0,R4       :DIVIDE BY 0
4442 033126 013767 177776  003334   MOV    @#PS,SPSW   :SAVE PS
4443 033134 042767 000014  003326   BIC    #14,SPSW
4444 033142 122767 000003  003320   CMPB   #3,SPSW
4445 033150 001404          BEQ    TST330      :IS PS =3

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====  

; CONDITIONAL BRANCH INST. AND                <=====  

; REPLACE THE MOVE INSTRUCTION                <=====  

; WHICH FOLLOWS W/ 757                      <=====
```

033152 012742 000760      MOV #760,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 760 \*\*\*\*\*  
 033156 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 033160 000000      HALT ;PS IS WRONG  
; OR SEQUENCE ERROR

4446 ;\*\*\*\*\* TEST 330 TEST SUB INSTRUCTION MODES 2-7\*\*\*\*\*

033162 005212 000330      TST330: INC (R2) ;UPDATE TEST NUMBER  
 033164 022712 000330      CMP #330,(R2) ;SEQUENCE ERROR?  
 033170 001075      BNE TST331-10 ;BR TO ERROR HALT ON SEQ ERROR  
 4447 033172 012700 177777      MOV #-1,R0 ;SETUP SOURCE TO -1  
 4448 033176 010037 033250      MOV R0,a#2\$+2 ;SET MODE 2 TO LOCATION TO A -1  
 4449 033202 0,2701 036474      MOV #SUBT+2,R1 ;SET R1 TO POINT TO BUFFER AREA +2  
 4450 033206 012761 177777 177776      MOV #-1,-2(R1) ;PUT -1 OP INTO DEST. BUFFER AREA  
 4451 033214 160041      SUB R0,-(R1) ;MODE-4 SUB SOURCE MODE 0 DEST MODE 4  
 4452 033216 001404      BEQ 1\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 764 <=====  
  
 033220 012742 000761      MOV #761,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 761 \*\*\*\*\*  
 033224 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 033226 000000      HALT ;SUB -1 FROM -1 FAILED TO GIVE ZERO RESULT IN MODE 4  
 4453 033230 022701 036472      1\$: CMP #SUBT,R1 ;VERIFY AUTO-DECREMENT OF R1 IN MODE 4 WORKED  
 4454 033234 001404      BEQ 2\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 755 <=====  
  
 033236 012742 000762      MOV #762,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 762 \*\*\*\*\*  
 033242 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 033244 000000      HALT ;R1 FAILED TO DECREMENT IN MODE 4  
 4455 033246 160027 177777      2\$: SUB R0,#-1 ;IF PROC HALTS AT PC=32650 THEN AUTO INC MODE FAILED  
 4456 033252 001404      BEQ 3\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 746 <=====  
  
 033254 012742 000763      MOV #763,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 763 \*\*\*\*\*  
 033260 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 033262 000000      HALT ;SUB -1 FROM -1 FAILED TO GIVE ZERO RESULT  
 4457 033264 012711 177777      3\$: MOV #-1,(R1) ;RESET SUBT TO A -1  
 4458 033270 160037 036472      SUB R0,a#SUBT ;SET MODE-3  
 4459 033274 001404      BEQ 4\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====  
; REPLACE THE MOVE INSTRUCTION <=====  
; WHICH FOLLOWS W/ 735 <=====  
  
 033276 012742 000764      MOV #764,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 764 \*\*\*\*\*  
 033302 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 033304 000000      HALT ;SUB -1 FROM -1 FAILED TO GIVE A ZERO RESULT  
 4460 033306 012703 036476      4\$: MOV #SUBT+4,R3 ;SETUP FOR MODE 5  
 4461 033312 012711 177777      MOV #-1,(R1) ;RESET SUBT TO A 1-  
 4462 033316 160053      SUB R0,a-(R3) ;SUB -1 FROM -1 USING MODE-5  
 4463 033320 001404      BEQ 5\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
; CONDITIONAL BRANCH INST. AND <=====

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 723 <=====  
 033322 012742 000765 MOV #765,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 765 \*\*\*\*\*  
 033326 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 033330 000000 HALT ;SUB -1 FROM -1 FAILED TO GIVE ZERO RESULT  
 4464 033332 012711 177777 5\$: MOV #-1,(R1) ;RESET SUBT TO A -1  
 4465 033336 160061 000000 SUB R0,0(R1) ;MODE-6  
 4466 033342 001404 BEQ 6\$ ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                           ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 712  
 033344 012742 000766 MOV #766,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 766 \*\*\*\*\*  
 033350 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 033352 000000 HALT ;SUB -1 FROM -1 FAILED TO GIVE ZERO RESULT  
 4467 033354 010011 6\$: MOV R0,(R1) ;RESET SUBT TO A -1  
 4468 033356 160071 000002 SUB R0,@2(R1) ;MODE-7  
 4469 033362 001404 BEQ TST331 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
                           ; CONDITIONAL BRANCH INST. AND  
                           ; REPLACE THE MOVE INSTRUCTION  
                           ; WHICH FOLLOWS W/ 702  
 033364 012742 000767 MOV #767,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 767 \*\*\*\*\*  
 033370 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 033372 000000 HALT ;SUB -1 FROM -1 FAILED TO GIVE ZERO RESULT  
 ; OR SEQUENCE ERROR  
 4470 ;\*\*\*\*\* TEST 331 TEST RTI KERNEL/USER MODE MICRO FLOW \*\*\*\*\*  
 ;\*\*\*\*\*  
 033374 005212 TST331: INC (R2) ;UPDATE TEST NUMBER  
 033376 022712 000331 CMP #331,(R2) ;SEQUENCE ERROR?  
 033402 001037 BNE TST332-10 ;BR TO ERROR HALT ON SEQ ERROR  
 4471 033404 012706 001000 MOV #STBOT,R6 ;SETUP KERNEL STACK  
 4472 033410 012767 140000 144360 MOV #USRMR,PS ;SETUP USER MODE  
 4473 033416 012706 036370 MOV #USTBOT,R6 ;SETUP USER STACK POINTER  
 4474 033422 012746 140000 MOV #USRMR,-(SP) ;PUSH USER R6 ON STACK  
 4475 033426 012746 033434 MOV #REN,-(SP) ;SETUP RETURN ADDRESS  
 4476 033432 000002 RTI ;CHECK PSW  
 4477 033434 022767 140000 144334 REN: CMP #140000,PS ;CLEAR USER MODE  
 4478 033442 001407 BEQ 1\$ ;MOVE TO MAILBOX # \*\*\*\*\* 770 \*\*\*\*\*  
 4479 033444 042767 140000 144324 BIC #USRMR,PS ;SET MSGTYP TO FATAL ERROR  
 4480 033452 012742 000770 MOV #770,-(R2) ;USER MODE DID NOT SET  
 033456 005242 INC -(R2) ;SET KERNAL MODE  
 033460 000000 HALT ;SET LEVEL 7  
 4481 033462 042767 140000 144306 1\$: BIC #USRMR,PS ;MOVE TO MAILBOX # \*\*\*\*\* 771 \*\*\*\*\*  
 4482 033470 012746 000340 MOV #340,-(SP) ;SET MSGTYP TO FATAL ERROR  
 4483 033474 012746 033512 MOV #TST332,-(SP) ;RTI DID NOT HAPPEN  
 4484 033500 000002 RTI ;\*\*\*\*\*  
 4485 033502 012742 000771 MOV #771,-(R2)  
 033506 005242 INC -(R2) ;THIS TEST IS OPTIONAL AND IS SELECTED BY SETTING MFM HARDWARE  
 033510 000000 HALT ;SWITCH REGISTER BIT 08 TO A 1 IN THE CASE OF STANDALONE OPERATION  
                           ; OF THE DIAGNOSTIC. IN THE CASE OF MANUFACTURING APT RUNTIME MODE  
                           ; THEN BIT 08 OF \$SWREG IS SET TO 1 THRU APT SCRIPTING.

4492  
4493  
4494  
4495  
4496  
4497  
4498  
4499  
4500  
4501  
4502  
4503  
4504  
4505

TEST DESCRIPTION:  
 THIS TEST VERIFIES THAT THE SWITCH REGISTER SELECT SIGNAL IS ISSUED FROM THE CPU DATA PATH MODULE TO THE MFM MODULE. WHEN THE HARDWARE SWITCH REGISTER IS READ, THE ADDRESS OF THE SWITCH REGISTER IS DECODED ON THE CPU DATA PATH CAUSING THE 'SR SELECT' SIGNAL TO BE ISSUED TO THE MFM. THE MFM USES THIS SIGNAL TO PLACE THE REGISTER CONTENTS ONTO THE PAX DATA BUS. CONTENTS OF THE SWITCH REGISTER OTHER THAN ALL 1'S SHOULD BE READ.(THERE IS A HI PROBABILITY THAT IF THE 'SR SELECT' SIGNAL IS NOT ISSUED ALL 1'S WILL BE READ ON PAX DATA.) IT IS ASSUMED THAT DATA OTHER THAN ALL 1'S IS LOCATED IN HARDWARE SWITCH REGISTER .

\*\*\*\*\*  
 TEST 332 SWITCH REGISTER SELECT TEST  
 \*\*\*\*\*

033512 005212	033514 022712	033520 001022	000332	TST332: INC (R2)	;UPDATE TEST NUMBER
				CMP #332,(R2)	;SEQUENCE ERROR?
				BNE TST333-10	;BR TO ERROR HALT ON SEQ ERROR
4506	033522 132767	000200	144571	BITB #200,\$ENVVM	;IS APT SIZING?
4507	033530 001405			BEQ 4\$	;NO;TRY HARDWARE SWITCH REGISTER
4508	033532 032767	000400	144562	BIT #400,\$SWREG	;YES APT IS SIZING;DOES APT SAY TO DO
4509					;THIS TEST
4510	033540 001413			BEQ 10\$	;NO;SKIP TEST
4511	033542 000404			BR 1\$	;YES,DO TEST
4512	033544 032737	000400	177570	4\$: BIT #400,@#177570	;DOES HARDWARE SWITCH REGISTER SAY TO
4513					;TO DO TEST?
4514	033552 001406			BEQ 10\$	;NO,SKIP TEST
4515					
4516	033554 013700	177570		1\$: MOV @#177570,R0	;READ HARDWARE SWITCH REGISTER CONTENTS
4517					;AND SAVE IN R0
4518	033560 022700	177777		CMP #-1,R0	;WERE ALL 1'S RECEIVED
4519				BNE 10\$	;NO,TEST PASSES
4520	033564 001001			HALT	; 'SR SELECT' ERROR OR SEQUENCE ERROR
4521	033566 000000				;ALL 1'S WERE RECEIVED WHEN HARDWARE SWITCH
4522					;REGISTER WAS READ. THIS INDICATES THAT THE
4523					;THE SWITCH REGISTER CONTENTS WAS NOT PUT ON
4524					;THE PAX DATA LINES AS A RESULT OF THE 'SR SELECT'
4525					;SIGNAL BEING RECEIVED BY THE MFM FROM THE
4526					;CPU DATA PATH MODULE
4527					
4528	033570 000240			10\$: NOP	;END OF TEST
4529	033572 000240			NOP	
4530	033574 000240			NOP	
4531					
4532					
4533					
4534					*****
4535					THIS TEST IS OPTIONAL AND IS SELECTED BY SETTING MFM HARDWARE
4536					SWITCH REGISTER BIT 08 TO A 1 IN THE CASE OF STANDALONE OPERATION
4537					OF THE DIAGNOSTIC. IN THE CASE OF MANUFACTURING APT RUNTIME MODE
4538					THEN BIT 08 OF \$SWREG IS SET TO 1 THRU APT SCRIPTING.
4539					
4540					
4541					
4542					
4543					

THIS TEST VERIFIES THE CACHE RESTART SIGNAL ON THE CPU CONTROL MODULE ISSUED FROM THE CACHE.

THIS TEST ASSUMES THAT ALL MODULES EXCEPT THE CPU DATA PATH/CONTROL STORE ARE KNOWN GOOD MODULES.

4544  
 4545  
 4546 THIS TEST TOGETHER WITH OTHER CACHE TESTS, ALLOW MFG. TO ELIMINATE  
 4547 HAVING TO RUN THE CACHE DIAGNOSTIC DURING QUICK  
 4548 VERIFY TESTING OF THE CPU MODULE.  
 4549  
 4550 TEST DESCRIPTION:  
 4551 VERIFY THAT A CACHE READ HIT WILL RESULT IN DATA BEING READ  
 4552 FROM CACHE DATA STORE, ASSURING THAT THE CACHE HAS ISSUED A  
 4553 A CPU CLOCK RESTART SIGNAL. ASSURE THAT ALL 0'S CAN BE CACHED  
 4554 OUT OF CACHE DATA STORE.  
 4555

---

TEST 333 CACHE RESTART SIGNAL TEST

---

033576	005212			TST333: INC (R2)	:UPDATE TEST NUMBER
033600	022712	000333		CMP #333, (R2)	:SEQUENCE ERROR?
033604	001115			BNE TST334-10	:BR TO ERROR HALT ON SEQ ERROR
4556 033606	132767	000200	144505	BITB #200,\$ENV	:IS APT SIZING?
4557 033614	001405			BEQ 4\$	:NO; TRY HARDWARE SWITCH REGISTER
4558 033616	032767	000400	144476	BIT #400,\$SWREG	:YES APT IS SIZING; DOES APT SAY TO DO
4559					:THIS TEST
4560 033624	001506			BEQ 10\$	:NO; SKIP TEST
4561 033626	000404			BR 1\$	:YES, DO TEST
4562 033630	032737	000400	177570	4\$: BIT #400,@#177570	:DOES HARDWARE SWITCH REGISTER SAY TO
4563					:TO DO TEST?
4564 033636	001501			BEQ 10\$	:NO, SKIP TEST
4565					
4566 033640			1\$:		
4567					
4568 033640	012701	040000		MOV #40000,R1	:ADDRESS 40000 TO R1
4569 033644	012705	060000		MOV #60000,R5	:ADDRESS 60000 TO R5
4570 033650	012737	033734	000014	MOV #3\$,@#14	:SETUP BPT TRAP VECTORS
4571 033656	012737	000340	000016	MOV #340,@#16	
4572 033664	005003			CLR R3	:CLEAR ERROR FLAGS
4573 033666	005004			CLR R4	
4574 033670	012706	060002		MOV #60002,R6	:STACK POINTER NOW POINTS TO ADDRESS 60002
4575 033674	005037	060000		CLR @#60000	:PRECONDITION MAIN MEMORY ADDRESS LOCATION
4576					:60000 WITH ALL 0'S
4577 033700	012767	000340	144070	MOV #340,PS	:PRECONDITION PS TO 340
4578 033706	112737	000002	177750	MOVB #2,@#177750	:HIT ON DESTINATION ONLY'(HODO) ALLOWS
4579					:CACHE UPDATES AND HITS
4580					:ONLY DURING THE DESTINATION MEMORY ACCESS
4581					:OF AN INSTRUCTION.
4582 033714	012737	000011	177746	MOV #11,@#177746	:NO BYPASS TO ALLOW WRITES TO CACHE STORES.
4583					:ENABLE LOW CACHE
4584 033722	000257			CCC	:CLEAR ALL CONDITION CODES
4585 033724	005711			TST (R1)	
4586 033726	005715			TST (R5)	:CACHE READ UPDATE. WRITE ALL 0'S FROM
4587					:MAIN MEMORY LOCATION TO CACHE DATA STORE
4588					:LOCATION 0000.
4589 033730	000003			BPT	:BREAKPOINT TRAP. DUE TO A TRAP, THE PSW
4590					:WILL BE WRITTEN TO THE STACK, WHICH NOW
4591					:POINTS TO ADDRESS 60000. THE TRAP INSTRUCTION
4592					:IS A NON-DESTINATION ACCESS INSTR. THEREFORE,
4593					:SINCE HODO IS BEING USED, A CACHE UPDATE
4594					:WILL BE INHIBITED. MAIN MEMORY
4595					:ADDRESS 60000 WILL CONTAIN PSW DATA OF 344, AND

4596 :THE LOCATION IN CACHE CORRESPONDING TO ADDRESS  
 4597 ;60000 WILL BE LEFT WITH ALL 0'S DATA.  
 4598  
 4599 033732 000000 HALT ;BPT TRAP DID NOT OCCUR  
 4600  
 4601 033734 042737 000002 177750 3\$: BIC #2,~~a#~~177750  
 4602 033742 011500 MOV (R5),R0 ;TRAP TO HERE;DISABLE HODO  
 4603 ;WHEN THIS INSTRUCTION READS  
 4604 ;ADDRESS 60000  
 4605 ;A CACHE READ HIT SHOULD RESULT AND A CPU CLOCK  
 4606 ;RESTART SIGNAL SHOULD BE ISSUED.  
 4607 ;THE CPU SHOULD READ DATA FROM CACHE DATA STORE  
 4608 033744 000240 NOP ;RATHER THAN MAIN MEMORY.  
 4609 033746 000240 NOP  
 4610 033750 005700 TST R0 ;R0 SHOULD CONTAIN ALL 0'S  
 4611 033752 001406 BEQ 7\$  
 4612 033754 022700 000344 CMP #344,R0 ;DID THE CPU READ MAIN MEMORY?  
 4613 033760 001002 BNE 6\$ ;NO, MUST HAVE READ CACHE BUT BAD DATA WAS RECEIVED.  
 4614 033762 005203 INC R3 ;INDICATE ERROR THAT MAIN MEMORY WAS READ  
 4615 033764 000401 BR 7\$  
 4616 033766 005204 6\$: INC R4 ;INDICATE ERROR THAT DATA WAS CACHED BUT  
 4617 ;BAD DATA WAS RECEIVED.  
 4618 033770 105037 177750 7\$: CLR B #a#177750 ;DISABLE MAINTENANCE MODE  
 4619 033774 012737 000000 177746 MOV #0,~~a#~~177746 ;TURN ON CACHE  
 4620 034002 012706 001000 MOV #STBOT,R6 ;RESET STACK POINTER  
 4621 034006 012737 036410 000014 MOV #T014,~~a#~~14 ;RESTORE BPT VECTORS  
 4622 034014 005037 000016 CLR a#16  
 4623 034020 005703 TST R3 ;WAS MAIN MEMORY READ?  
 4624 034022 001402 BEQ 8\$ ;NO  
 4625 034024 000000 HALT ;ERROR  
 4626 ;CPU CLOCK RESTART-CACHED DATA TESTS  
 4627  
 4628 ;ATTEMPTING TO CAUSE A READ HIT IN ORDER TO  
 4629 ;CACHE DATA RESULTED IN MAIN MEMORY BEING READ  
 4630 034026 000405 8\$: BR 10\$  
 4631 034030 005704 TST R4 ;NEXT TEST  
 4632 034032 001403 BEQ 10\$ ;WAS BAD DATA CACHED FROM CACHE DATA STORE?  
 4633 034034 000000 HALT ;NO, NEXT TEST  
 4634 ;ERROR  
 4635 ;CPU CLOCK RESTART-CACHED DATA TESTS  
 4636 ;CREATING A READ HIT BY READING ADDRESS 60000  
 4637 ;CACHED BAD DATA FROM CACHE DATA STORE  
 4638 034036 000401 10\$: BR 10\$  
 4639 034040 000000 HALT ;SEQUENCE ERROR  
 4640 034042 000402 10\$: BR .+6  
 4641 034044 000240 NOP  
 4642 034046 000240 NOP  
 4643 ;\*\*\*\*\*  
 4644 ;THIS TEST IS OPTIONAL AND IS SELECTED BY SETTING MFM HARDWARE  
 4645 ;SWITCH REGISTER BIT 08 TO A 1 IN THE CASE OF STANDALONE OPERATION  
 4646 ;OF THE DIAGNOSTIC. IN THE CASE OF MANUFACTURING APT RUNTIME MODE  
 4647 ;THEN BIT 08 OF \$SWREG IS SET TO 1 THRU APT SCRIPTING.  
 4648 ;  
 4649 ;  
 4650 ;  
 4651 ;  
 4652 ;  
 ;\* THIS TEST VERIFIES  
 ;\* THE CPU CONTROL SIGNAL TO THE CACHE WHICH INDICATES THAT AN ACCESS  
 ;\* TO THE UNIBUS IS BEING PERFORMED(PA TOP 128K L).

4653  
 4654 ;\* THIS TEST ASSUMES THAT ALL MODULES OTHER THAN CPU CONTROL/DATA PATH  
 4655 ;\* ARE KNOWN GOOD MODULES.  
 4656  
 4657 ;\* THIS TEST TOGETHER WITH OTHER CACHE TESTS, ALLOW MFG. TO ELIMINATE  
 4658 ;\* HAVING TO RUN THE CACHE DIAGNOSTIC DURING QUICK  
 4659 ;\* VERIFY TESTING OF THE CPU MODULE.  
 4660 ;\* TEST DESCRIPTION:  
 4661 ;\* VERIFY THAT THE CACHE WRITE CONTROL LOGIC WILL INHIBIT A CACHE  
 4662 ;\* READ UPDATE TO CACHE TAG STORE DUE TO AN ACCESS TO I/O PAGE.  
 4663  
 4664 ;\*\*\*\*\*  
 :TEST 334 CACHE WRITE CONTROL LOGIC TEST  
 :\*\*\*\*\*  
 034050 005212 000334 TST334: INC (R2) ;UPDATE TEST NUMBER  
 034052 022712 000200 144233 CMP #334, (R2) ;SEQUENCE ERROR?  
 034056 001051 BNE TST335-10 ;BR TO ERROR HALT ON SEQ ERROR  
 4665 034060 132767 000400 144224 BITB #200,\$ENV# ;IS APT SIZING?  
 4666 034066 001405 BEQ 4\$ ;NO; TRY HARDWARE SWITCH REGISTER  
 4667 034070 032767 000400 144224 BIT #400,\$SWREG ;YES APT IS SIZING; DOES APT SAY TO DO  
 4668  
 4669 034076 001442 BEQ 10\$ ;THIS TEST  
 4670 034100 000404 BR 1\$ ;NO; SKIP TEST  
 4671 034102 032737 000400 177570 4\$: BIT #400,@#177570 ;YES, DO TEST  
 4672  
 4673 034110 001435 BEQ 10\$ ;DOES HARDWARE SWITCH REGISTER SAY TO  
 4674  
 4675 034112 112737 000002 177750 1\$: TO DO TEST?  
 4676 034112 112737 000002 177750 MOV #2,@#177750 ;NO; SKIP TEST  
 4677  
 4678  
 4679  
 4680 034120 012737 000015 177746 MOV #15,@#177746 ;ALLOWS CACHE TAG FIELD BITS TO BE  
 4681 034126 005737 057744 TST @#57744 ;WRITTEN TO CHR<15:07> ONLY DURING  
 4682 034132 005737 077744 TST @#77744 ;THE DESTINATION MEMORY ACCESS  
 4683  
 4684  
 4685 034136 005737 177744 TST @#177744 ;OF AN INSTRUCTION  
 4686  
 4687  
 4688  
 4689  
 4690 034142 005737 057744 TST @#57744 ;NO UCB SO AS TO WRITE ENABLE CACHE STORE  
 4691  
 4692 034146 013700 177752 MOV @#177752,R0 ;READ UPDATE; LOAD BIT PATTERN  
 4693 034152 000240 NOP ;000000011 INTO TAG STORE LOCATION  
 4694 034154 000240 NOP  
 4695  
 4696 034156 105037 177750 CLRB @#177750 ;7762  
 4697 034162 012737 000000 177746 MOV #0,@#177746 ;ACCESS I/O PAGE BY READING CME REGISTER.  
 4698 034170 042700 000177 BIC #177,R0 ;THE CACHE COULD DO AN UPDATE TO  
 4699 034174 022700 000600 CMP #600,R0 ;TAG STORE LOCATION 7762 BUT THE ACCESS  
 4700 034200 001401 BEQ 10\$ ;TO I/O PAGE WILL INHIBIT WRITE CONTROL  
 4701 034202 000000 HALT ;LOGIC  
 4702  
 4703  
 4704 ;WRITE TAG STORE DATA FROM LOCATION  
 ;7762 INTO CHR<15:07>. ;SAVE CHR DATA  
 ;DISABLE MAINTENANCE MODE  
 ;TURN ON CACHE  
 ;PREPARE R0 FOR ERROR CHECK  
 ;BITS 15:07 SHOULD BE BIT PATTERN 000000011  
 ;PASS  
 ;CACHE WRITE CONTROL CPU LOGIC SIGNAL  
 ;OR SEQUENCE ERROR  
 ;READING TAG DATA BITS<21:13> THRU CACHE HIT REGISTE  
 ;DID NOT RESULT IN BIT PATTERN 000000011.

```
4705  
4706  
4707  
4708  
4709  
4710 034204 000240  
4711 034206 000240  
4712 034210 000240  
4713  
4714  
4715  
4716  
4717  
4718  
4719  
4720  
4721  
4722  
4723  
4724  
4725  
4726  
4727  
10$: NOP ;END OF TEST  
      NOP  
      NOP  
      *****  
      ;* THIS TEST IS OPTIONAL AND IS SELECTED BY SETTING MFM HARDWARE  
      ;* SWITCH REGISTER BIT 08 TO A 1 IN THE CASE OF STANDALONE OPERATION  
      ;* OF THE DIAGNOSTIC. IN THE CASE OF MANUFACTURING APT RUNTIME MODE  
      ;* THEN BIT 08 OF $SWREG IS SET TO 1 THRU APT SCRIPTING.  
      ;* THIS TEST VERIFIES  
      ;* THE CACHE BYPASS SIGNAL GENERATED FROM THE CPU TO THE CACHE(CACHE BYPASS L).  
      ;* THIS SIGNAL IS GENERATED WHEN THE ASRB INSTRUCTION IS EXECUTED.  
      ;*  
      ;* THIS TEST ASSUMES THAT ALL MODULES EXCEPT CPU DATA PATH/CONTROL STORE  
      ;* ARE KNOWN GOOD MODULES.  
      ;* THIS TEST TOGETHER WITH OTHER CACHE TESTS, ALLOW MFG. TO ELIMINATE
```

4729  
4730  
4731  
4732  
4733  
4734  
4735  
\*: HAVING TO RUN THE CACHE DIAGNOSTIC DURING QUICK  
VERIFY TESTING OF THE CPU MODULE.  
TEST DESCRIPTION:  
VERIFY THAT THE ASRB INSTRUCTION WILL CAUSE A CACHE BYPASS  
UNDER A READ HIT CONDITION.

\*\*\*\*\*  
TEST 335 ASRB CACHE BYPASS TEST  
\*\*\*\*\*

034212 005212		TST335: INC (R2)	:UPDATE TEST NUMBER	
034214 022712	000335	CMP #335,(R2)	:SEQUENCE ERROR?	
034220 001043		BNE TST336-10	:BR TO ERROR HALT ON SEQ ERROR	
4736 034222 132767	000200	144071	BITB #200,\$ENV#	:IS APT SIZING?
4737 034230 001405		BEQ 4\$	:NO;TRY HARDWARE SWITCH REGISTER	
4738 034232 032767	000400	144062	BIT #400,\$SWREG	:YES APT IS SIZING;DOES APT SAY TO DO
4739			:THIS TEST	
4740 034240 001434		BEQ 10\$	:NO;SKIP TEST	
4741 034242 000404		BR 1\$	:YES,DO TEST	
4742 034244 032737	000400	177570	4\$: BIT #400,@#177570	:DOES HARDWARE SWITCH REGISTER SAY TO
4743			:TO DO TEST?	
4744 034252 001427		BEQ 10\$	:NO,SKIP TEST	
4745				
4746 034254		1\$: MOV #60000,R0	:SETUP TEST LOCATION ADDRESS	
4747 034254 012700	060000		:IN R0	
4748			:HOD0 ALLOWS READ HITS TO BE CACHED,CACHE UPDATES,AN	
4749 034260 112737	000002	177750	CLOCKING OF OUTPUT OF CACHE HIT NAND	
4750			GATE INTO CMR ONLY DURING THE DESTINATION	
4751			ACCESS OF AN INSTRUCTION.	
4752			:NO UCB SO AS TO WRITE CACHE STORES	
4753 034266 012737	000011	177746	ENABLE LOW CACHE FOR A READ HIT	
4754				

CKKAAAO 11/44 CPU/EIS MACRO M1111 28-SEP-79 10:10 PAGE 13  
T335 ASRB CACHE BYPASS TEST

L 15

SEQ 0193

4756  
4757 034274 005710  
4758  
4759  
4760 034276 106210

TST (R0)

ASRB (R0)

;READING LOCATION SPECIFIED BY R0  
;WILL ASSURE A READ HIT WHEN THE  
;LOCATION IS READ AGAIN  
;ASRB INSTRUCTION WILL CAUSE A BYPASS

4762  
4763  
4764  
4765  
4766  
4767 034300 013701 177750  
4768 034304 000240  
4769 034306 000240  
4770 034310 105037 177750  
4771 034314 012737 000000 177746  
4772 034322 032701 C00400  
4773 034326 001001  
4774 034330 000000  
4775  
4776  
4777

MOV #177750,R1 ;SAVE CMR CONTENTS  
NOP  
NOP  
CLRB #177750 ;DISABLE MAINT MODE  
MOV #0,#177746 ;TURN ON CACHE  
BIT #400,R1 ;WAS CMR BIT 8 A 1  
BNE 10\$ ;PASS  
HALT ;CACHE BYPASS DID NOT OCCUR OR  
;SEQUENCE ERROR  
;READING OUTPUT OF CACHE HIT NAND GATE  
;THRU CMR<8> DID NOT RESULT IN A 1

```

4779 034332 000240          10$:    NOP          ;END OF TEST
4780 034334 000240
4781 034336 000240
4782
4783
4784
4785
4786
4787
4788
4789
4790
4791
4792
4793
4794
4795
4796
4797
4798
4799
4800
4801
4802
4803

      **** THIS TEST IS OPTIONAL AND IS SELECTED BY SETTING MFM HARDWARE
      **** SWITCH REGISTER BIT 08 TO A 1 IN THE CASE OF STANDALONE OPERATION
      **** OF THE DIAGNOSTIC. IN THE CASE OF MANUFACTURING APT RUNTIME MODE
      **** THEN BIT 08 OF $SWREG IS SET TO 1 THRU APT SCRIPTING.

      **** THIS TEST VERIFIES THE MICROCODE IN THE CPU CONTROL STORE ASSOCIATED
      **** WITH THE CIS INSTRUCTION SET. IT IS ASSUMED THAT ALL MODULES EXCEPT
      **** THE CPU DATA PATH AND CONTROL MODULE ARE ALL 'KNOWN GOOD MODULES'.

      **** THIS TEST ALLOWS MFG. TO ELIMINATE
      **** HAVING TO RUN THE CIS DIAGNOSTIC DURING QUICK
      **** VERIFY TESTING OF THE CPU MODULE.

      **** TEST DESCRIPTION:
      **** THE CPU MPC MICROADDRESSES ASSOCIATED WITH THE CPU ARE
      **** 740 THRU 776. IT HAS BEEN DETERMINED THAT BY EXECUTING THIS TEST
      **** ALL BUT MPC ADDRESS 772 AND 773 ARE COVERED.

      **** TEST 336      CIS CPU MPC ADDRESS COVERAGE TEST
      ****
      **** TST336: INC (R2)          :UPDATE TEST NUMBER
      **** CMP #336,(R2)           :SEQUENCE ERROR?
      **** BNE TST337-10          :BR TO ERROR HALT ON SEQ ERROR
      **** BITB #200,SENVM        :IS APT SIZING?
      **** BEQ 4$                 :NO;TRY HARDWARE SWITCH REGISTER
      **** BIT #400,$SWREG        :YES APT IS SIZING;DOES APT SAY TO DO
      ****                      :THIS TEST
      **** BEQ ENDMPC            :NO;SKIP TEST
      **** BR 1$                 :YES,DO TEST
      **** BIT #400,@#177570       :DOES HARDWARE SWITCH REGISTER SAY TO
      ****                      :TO DO TEST?
      **** BEQ ENDMPC            :NO,SKIP TEST
      ****
      **** 1$: MOV #2$,@#10          ;SETUP FOR POSSIBLE TRAP
      **** MOV #340,@#12
      **** 76001
      ****
      **** :THIS CIS INSTRUCTION SHOULD CAUSE A TRAP
      **** :TO OCCUR TO VECTOR 10 INDICATING THAT
      **** :SWITCH S1 OF CIS M7092 DATA PATH MODULE
      **** :IS OPEN. THE SWITCH MUST BE OPEN TO ALLOW
      **** :THIS TEST TO RUN.

      **** 034420 000240          NOP
      **** 034422 012737 C36400 000010  MOV #T010,@#10 :RESTORE VECTORS
      **** 034430 005037 000012    CLR @#12
      **** 034434 000000          HALT
      ****
      **** :CHECK TO SEE THAT SWITCH S1 OF M7092 CIS DATA
      **** :PATH MODULE IS OPEN.

      **** 034436 000406          2$: BR 5$          :READJUST STACK
      **** 034440 022626          CMP (SP)+(SP)+ :RESTORE VECTORS
      **** 034442 012737 036400 000010  MOV #T010,@#10
      **** 034450 005037 000012    CLR @#12

```

4831  
4832 034454 076150      5\$: ADDNI ;;NOW PERFORM CIS INSTRUCTION WHICH WILL  
4833                            .WORD A ;COVER MOST OF THE CPU MPC MICROADDRESSES  
4834 034456 034466      .WORD B  
4835 034460 034472      .WORD C  
4836 034462 034476      .WORD D  
4837  
4838 034464 000414      BR CHECK ;NOW CHECK RESULTS  
4839  
4840 076150      ADDNI=76150  
4841 034466 000006      A: .WORD 6  
4842 034470 034502      .WORD SA  
4843 034472 000006      B: .WORD 6  
4844 034474 034502      .WORD SA  
4845 034476 000006      D: .WORD 6  
4846 034500 034510      .WORD DA  
4847 034502 001002      SA: .WORD 1002  
4848 034504 001002      .WORD 1002  
4849 034506 031002      .WORD 31002  
4850 034510 000000      DA: .WORD 0  
4851 034512 000000      .WORD 0  
4852 034514 000000      .WORD 0  
4853  
4854 034516      CHECK:  
4855 034516 022737 032064 034510      CMP #32064,0#DA ;CHECK RESULTS  
4856 034524 001401      BEQ 6\$ ;PASS  
4857 034526 000000      HALT ;ERROR  
4858 034530 022737 032064 034512 6\$: CMP #32064,0#DA+2 ;CHECK RESULT  
4859 034536 001401      BEQ 7\$ ;PASS  
4860 034540 000000      HALT ;ERROR  
4861 034542 022737 032064 034514 7\$: CMP #32064,0#DA+4 ;CHECK RESULT  
4862 034550 001401      BEQ ENDMPC ;PASS  
4863 034552 000000      HALT ;CIS INSTRUCTION OR SEQUENCE ERROR  
4864  
4865 034554 000240      ENDMPC: NOP  
4866 034556 000240      NOP  
4867 034560 000240      NOP

=====  
WARNING!

4871  
4872  
4873 THE FOLLOWING CIS ABORT TEST MUST BE LOCATED BELOW  
4874 MEMORY LOCATION 40000 DUE TO THE MEMORY MANAGEMENT  
4875 SETUP REQUIRED IN THE TEST.

4876  
4877 ALSO THE TEST DESTROYS THE CONTENTS OF MEMORY IN THE  
4878 FOLLOWING RANGES:  
4879

4880 57670-60070  
4881 76000-76001

4882  
4883 THIS WARNING IS PRIMARILY AIMED AT FUTURE MODIFIERS OF THIS CPU DIAGNOSTIC.  
4884  
4885  
4886  
4887 =====

4888

4889

4890

4891

4892

4893

4894

4895

4896

4897

4898

4899

4900

4901

4902

4903

4904

4905

4906

4907

4908

4909

4910

4911

4912

4913

4914

4915

4916

000377

FILL=377

4917

076130

MOVCI=76130

4918

4919

.SBTTL CIS STACK PROBE AHEAD MEM MGMT ABORT TEST

4920

;\*\*\*\*\* TEST 337 CIS STACK PROBE AHEAD MEM MGMT ABORT TEST

4921

4922

4923

4924

034562

005212

TST337: INC (R2)

:UPDATE TEST NUMBER

4925

034564

022712

CMP #337,(R2)

:SEQUENCE ERROR?

4926

034570

001020

BNE 6\$

:BR TO ERROR HALT ON SEQ ERROR

4927

4928

034572

132767 000200 143521

BITB #200,\$ENVM

:IS APT SIZING?

4929

034600

001405

BEQ 4\$

:NO; TRY HARDWARE SWITCH REGISTER

4930

034602

032767 000400 143512

BIT #400,\$\$WREG

:YES APT IS SIZING; DOES APT SAY TO DO THIS TEST

4931

034610

001406

BEQ 5\$

:NO; SKIP TEST

4932

034612

000411

BR 1\$

:YES, DO TEST

4933

034614

032737 000400 177570

4\$: BIT #400,a#177570

:DOES HARDWARE SWITCH REGISTER SAY TO DO TEST?

4934

034622

001401

BEQ 5\$

:NO, SKIP TEST

4935

034624

000404

BR 1\$

:YES, DO TEST

4936

034626

000167

5\$: JMP ENDABO

4937

034632

000167 001072

6\$: JMP ENDPASS-10

4938

4939

:SETUP PAR'S FOR DIRECT MAPPING

4940

4941

034636

005037 172516

1\$: CLR @MMR3

:CLEAR OUT D-SPACE ENABLES

4942

034642

010667 001022

MOV SP,STK1

:SAVE THE STACK POINTER

4943

4944

034646

012737 000000 172340

MOV #0,@KIPARO

:SETUP KERNEL I-SPACE PAR'S

:\*\*\*\*\* CIS STACK 'PROBE AHEAD' MEMORY MANAGEMENT ABORT TESTS

THE NEXT THREE SUBTESTS ARE AIMED AT TESTING THE KT PAGE FAULT ROM (SCHEMATIC PAGE K1-8) AND ASSOCIATED LOGIC.  
NOTE: THESE 3 SUBTESTS ARE OPTIONAL AND ARE SELECTED BY SETTING MFM HARDWARE SWITCH REGISTER BIT 08 TO A 1 IN THE CASE OF STANDALONE OPERATION OF THE DIAGNOSTIC. IN THE CASE OF MANUFACTURING APT RUNTIME MODE THEN BIT 08 OF \$SWREG IS SET TO 1 THRU APT SCRIPTING.

EACH OF THESE 3 SUBTESTS SETUP THE STACK POINTER SUCH THAT WHEN THE CIS PROCESSOR CHECKS TO SEE IF THERE IS ENOUGH SPACE ON THE STACK (200 BYTES) THE ANSWER FOUND SHOULD BE NO BECAUSE A PORTION OF THE STACK IS IN PROTECTED MEMORY.

EACH OF THESE 3 SUBTESTS VERIFY THAT THE CIS INSTRUCTION ABORTS UNDER SEVERAL CONDITIONS OF MEMORY MANAGEMENT PAGE PROTECTION. ALL OF THE PAGE PROTECTION DATA IS LISTED IN TABLE 'PDRTAB'.

THIS TEST ALLOWS MFG. TO ELIMINATE HAVING TO RUN THE CIS DIAGNOSTIC DURING QUICK VERIFY TESTING OF THE CPU MODULE.

4945 034654 012737 000200 172342 MOV #200,<sup>a</sup>KIPAR1  
4946 034662 012737 000400 172344 MOV #400,<sup>a</sup>KIPAR2  
4947 034670 012737 000600 172346 MOV #600,<sup>a</sup>KIPAR3  
4948 034676 012737 001000 172350 MOV #1000,<sup>a</sup>KIPAR4  
4949 034704 012737 001200 172352 MOV #1200,<sup>a</sup>KIPAR5  
4950 034712 012737 001400 172354 MOV #1400,<sup>a</sup>KIPAR6  
4951 034720 012737 177600 172356 MOV #177600,<sup>a</sup>KIPAR7  
4952  
4953 034726 012737 000000 172240 MOV #0,<sup>a</sup>SIPAR0 ;SETUP SUPERVISOR I-SPACE PAR'S  
4954 034734 012737 000200 172242 MOV #200,<sup>a</sup>SIPAR1  
4955 034742 012737 000400 172244 MOV #400,<sup>a</sup>SIPAR2  
4956 034750 012737 000600 172246 MOV #600,<sup>a</sup>SIPAR3  
4957 034756 012737 001000 172250 MOV #1000,<sup>a</sup>SIPAR4  
4958 034764 012737 001200 172252 MOV #1200,<sup>a</sup>SIPAR5  
4959 034772 012737 001400 172254 MOV #1400,<sup>a</sup>SIPAR6  
4960 035000 012737 177600 172256 MOV #177600,<sup>a</sup>SIPAR7  
4961  
4962 035006 012737 000000 177640 MOV #0,<sup>a</sup>UIPAR0 ;SETUP USER I-SPACE PAR'S  
4963 035014 012737 000200 177642 MOV #200,<sup>a</sup>UIPAR1  
4964 035022 012737 000400 177644 MOV #400,<sup>a</sup>UIPAR2  
4965 035030 012737 000600 177646 MOV #600,<sup>a</sup>UIPAR3  
4966 035036 012737 001000 177650 MOV #1000,<sup>a</sup>UIPAR4  
4967 035044 012737 001200 177652 MOV #1200,<sup>a</sup>UIPAR5  
4968 035052 012737 001400 177654 MOV #1400,<sup>a</sup>UIPAR6  
4969 035060 012737 177600 177656 MOV #177600,<sup>a</sup>UIPAR7  
4970  
4971  
4972 :SETUP PDR'S FOR R/W ACCESS  
4973 :  
4974  
4975 035066  
4976 035066 012700 172300 MOV #KIPDRO,R0  
4977 035072 012720 177406 1\$: MOV #177406,(R0)+  
SETPDR:

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4979 035076 020027 172316           CMP R0,#KIPDR7
4980 035102 101773
4981
4982 035104 012700 172200          2$: MOV #SIPDRO, R0
4983 035110 012720 177406          MOV #177406,(R0) +
4984 035114 020027 172216          CMP R0,#SIPDR7
4985 035120 101773               BLOS 2$
4986
4987 035122 012700 177600          3$: MOV #UIPDR0, R0
4988 035126 012720 177406          MOV #177406,(R0) +
4989 035132 020027 177616          CMP R0,#UIPDR7
4990 035136 101773               BLOS 3$
4991
4992 ;KERNEL MODE CIS STACK PROBE AHEAD MEM MGMT ABORT SUBTEST
4993 ;
4994
4995 035140
4996 035140 012737 035546 000250   KMTSTS: MOV #MMHDLR,aMMVEC      ;SETUP MEM MGMT INTERRUPT VECTOR
4997 035146 012737 000340 000252   MOV #PR7,aMMVEC+2
4998 035154 012701 035224          MOV #1$,R1      ;SETUP INTR RETURN ADDRESS
4999 035160 012700 035672          MOV #PDRTAB,R0
5000 035164 012706 060070          MOV #60070,SP
5001
5002 035170 011037 172304          2$: MOV (R0),aKIPDR2      ;PROTECT PART OF STACK
5003 035174 012737 000001 177572   MOV #1,aMMR0      ;TURN ON MEMORY MGMT
5004
5005 035202 004767 000362          JSR PC,SAVR      ;SAVE REGISTERS
5006
5007 035206 076130               MOVCI          ;EXECUTE THE CIS INSTRUCTION
5008 035210 035560               SRC.PTR
5009 035212 035564               DST.PTR
5010 035214 000377               FILL
5011 035216 000240               NOP
5012 035220 000240               NOP
5013 035222 000000               HALT          ;CIS INSTRUCTION SHOULD HAVE ABORTED BUT DIDN'T
5014
5015 035224 004767 000372          1$: JSR PC,RESR      ;RESTORE REGISTERS
5016 035230 062700 000002          ADD #2,R0      ;UPDATE PROTECTION SCHEME TO NEXT TABLE CASE
5017 035234 005710               TST (R0)
5018 035236 001354               BNE 2$      ;ANY CASES LEFT TO TRY?
5019
5020 035240 005037 177572          CLR aMMR0      ;BRANCH IF YES
5021 035244 012737 177406 172304   MOV #177406,aKIPDR2
5022 035252 000400               BR SMTSTS      ;NO - PREPARE TO EXIT TEST
5023
5024
5025 ;SUPERVISOR MODE CIS STACK PROBEAHEAD MEMORY MGMT ABORT SUBTEST
5026 ;
5027
5028 035254
5029 035254 012737 035546 000250   SMTSTS: MOV #MMHDLR,aMMVEC      ;SETUP MEM MGMT INTERRUPT VECTOR
5030 035262 012737 040340 000252   MOV #040340,aMMVEC+2
5031 035270 012701 035354          MOV #1$,R1      ;SETUP INTR RETURN ADDRESS
5032 035274 012700 035672          MOV #PDRTAB,R0
5033 035300 012737 040340 177776   MOV #040340,aPSW
5034 035306 012706 060070          MOV #60070,SP      ;SWITCH TO SUPERVISOR MODE
5035

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5036 035312 011037 172204 2\$: MOV (R0),@#SIPDR2 :PROTECT PART OF STACK  
 5037 035316 012737 000001 177572 MOV #1,@#MMR0 :TURN ON MEMORY MGMT  
 5038  
 5039 035324 004767 000240 JSR PC,SAVR :SAVE REGISTERS  
 5040  
 5041 035330 076130 MOVCI :EXECUTE THE CIS INSTRUCTION  
 5042 035332 035560 SRC.PTR  
 5043 035334 035564 DST.PTR  
 5044 035336 000377 FILL  
 5045  
 5046 035340 000240 NOP  
 5047 035342 000240 NOP  
 5048 035344 012737 000340 177776 MOV #340,@#PSW :SWITCH BACK TO KERNEL MODE BEFORE HALT  
 5049 035352 000000 HALT :CIS INSTRUCTION SHOULD HAVE ABORTED BUT DIDN'T  
 5050  
 5051 035354 004767 000242 1\$: JSR PC,RESR :RESTORE REGISTERS  
 5052 035360 062700 000002 ADD #2,R0 :UPDATE PROTECTION SCHEME TO NEXT TABLE CASE  
 5053 035364 005710 TST (R0) :ANY CASES LEFT TO TRY?  
 5054 035366 001351 BNE 2\$ :BRANCH IF YES  
 5055  
 5056 035370 005037 177572 CLR @#MMR0 :NO - PREPARE TO EXIT TEST  
 5057 035374 012737 177406 172204 MOV #177406,@#SIPDR2 :RESTORE R/W ACCESS TO STACK AREA  
 5058 035402 000400 BR UMTSTS :GO TO NEXT TEST  
 5059  
 5060  
 5061 :USER MODE CIS STACK PROBEAHEAD MEM MGMT ABORT SUBTEST  
 5062 :  
 5063 :  
 5064 035404 UMTSTS:  
 5065 035404 012737 035546 000250 MOV @MMHDLR,@#MMVEC :SETUP MEM MGMT INTERRUPT VECTOR  
 5066 035412 012737 140340 000252 MOV #140340,@#MMVEC+2 :SETUP INTR RETURN ADDRESS  
 5067 035420 012701 035504 MOV #1\$,R1  
 5068 035424 012700 035672 MOV #PDRTAB,R0  
 5069 035430 012737 140340 177776 MOV #140340,@#PSW :SWITCH TO USER MODE  
 5070 035436 012706 060070 MOV #600070,SP  
 5071  
 5072 035442 011037 177604 2\$: MOV (R0),@#UIPDR2 :PROTECT PART OF STACK  
 5073 035446 012737 000001 177572 MOV #1,@#MMR0 :TURN ON MEMORY MGMT  
 5074  
 5075 035454 004767 000110 JSR PC,SAVR :SAVE REGISTERS  
 5076  
 5077 035460 076130 MOVCI :EXECUTE THE CIS INSTRUCTION  
 5078 035462 035560 SRC.PTR  
 5079 035464 035564 DST.PTR  
 5080 035466 000377 FILL  
 5081  
 5082 035470 000240 NOP  
 5083 035472 000240 NOP  
 5084 035474 012737 000340 177776 MOV #340,@#PSW :SWITCH BACK TO KERNEL MODE BEFORE HALT  
 5085 035502 000000 HALT :CIS INSTRUCTION SHOULD HAVE ABORTED BUT DIDN'T  
 5086  
 5087 035504 004767 000112 1\$: JSR PC,RESR :RESTORE REGISTERS  
 5088 035510 062700 000002 ADD #2,R0 :UPDATE PROTECTION SCHEME TO NEXT TABLE CASE  
 5089 035514 005710 TST (R0) :ANY CASES LEFT TO TRY?  
 5090 035516 001351 BNE 2\$ :BRANCH IF YES  
 5091  
 5092 035520 005037 177572 CLR @#MMR0 :NO - PREPARE TO EXIT TEST

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5093 035524 012737 177406 177604      MOV #177406,a#UIPDR2      ;RESTORE R/W ACCESS TO STACK AREA
5094 035532 012737 000340 177776      MOV #340,a#PSW          ;SWITCH BACK TO KERNEL MODE
5095 035540 016706 000124      MOV STK1,SP          ;RESTORE THE STACK POINTER
5096 035544 000472      BR ENDABO        ;GO TO NEXT TEST

5097
5098
5099
5100      :MEMORY MANAGEMENT TRAP HANDLER
5101
5102 035546
5103 035546 005037 177572      MMHDLR:
5104 035552 005726
5105 035554 005726
5106 035556 000111      CLR aMMRC          ;TURN OFF MEM MGMT
5107
5108
5109
5110      :CIS INSTRUCTION SOURCE AND DESTINATION DESCRIPTORS
5111
5112 035560 000001      SRC.PTR:     .WORD 1
5113 035562 076000
5114 035564 000001      DST.PTR:     .WORD 1
5115 035566 076001
5116
5117      :SUBROUTINES
5118
5119 035570 010067 000060      SAVR:       MOV R0,SVR0          ;SAVE, REGISTERS
5120 035574 010167 000056      MOV R1,SVR1
5121 035600 010267 000054      MOV R2,SVR2
5122 035604 010367 000052      MOV R3,SVR3
5123 035610 010467 000050      MOV R4,SVR4
5124 035614 010567 000046      MOV R5,SVR5
5125 035620 000207      RTS PC

5126
5127 035622 016700 000026      RESR:       MOV SVR0,R0          ;RESTORE REGISTERS
5128 035626 016701 000024      MOV SVR1,R1
5129 035632 016702 000022      MOV SVR2,R2
5130 035636 016703 000020      MOV SVR3,R3
5131 035642 016704 000016      MOV SVR4,R4
5132 035646 016705 000014      MOV SVR5,R5
5133 035652 000207      RTS PC

5134
5135 035654 000000      SVR0:      .WORD 0
5136 035656 000000      SVR1:      .WORD 0
5137 035660 000000      SVR2:      .WORD 0
5138 035662 000000      SVR3:      .WORD 0
5139 035664 000000      SVR4:      .WORD 0
5140 035666 000000      SVR5:      .WORD 0
5141
5142 035670 000000      STK1:      .WORD 0
5143
5144
5145      :PROTECTION TABLE (WORD FORMAT = PDR FORMAT)
5146 035672
5147 035672 177000      PDRTAB:    177000      ;ACF=00      ED=0  PLF=176
5148 035674 177410      177410      ;ACF=00      ED=1  PLF=177
5149 035676 177400      177400      ;ACF=00      ED=0  PLF=177

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CIS STACK PROBE AHEAD MEM MGMT ABORT TEST

H 16

SEQ 0202

5150 035700	100010	100010	;ACF=00	ED=1	PLF=0
5151					
5152 035702	177002	177002	;ACF=01	ED=0	PLF=176
5153 035704	177412	177412	;ACF=01	ED=1	PLF=177
5154 035706	177402	177402	;ACF=01	ED=0	PLF=177
5155 035710	100012	100012	;ACF=01	ED=1	PLF=0
5156					
5157 035712	177004	177004	;ACF=10	ED=0	PLF=176
5158 035714	177414	177414	;ACF=10	ED=1	PLF=177
5159 035716	177404	177404	;ACF=10	ED=0	PLF=177
5160 035720	100014	100014	;ACF=10	ED=1	PLF=0
5161					
5162 035722	177006	177006	;ACF=11	ED=0	PLF=176
5163 035724	177416	177416	;ACF=11	ED=1	PLF=177
5164 035726	000000	0			
5165					
5166					
5167 035730	000000	HALT	;TEST SEQUENCE ERROR		
5168 035732	000240	ENDABO:	NOP		
5169 035734	000240		NOP		
5170 035736	000240		NOP		
5171					

5173					***** END OF PASS SEQUENCE *****		
5174							
5175							
5176							
5177 035740 005212	000340		ENDPASS:	INC (R2) CMP #340,(R2) BNE EOP1		:UPDATE TEST NUMBER :SEQUENCE ERROR? :BR TO ERROR HALT ON SEQ ERROR	
5178 035742 022712				INC #4\$PASS			
5179 035746 001042				INCB PASSPT			
5180 035750 005237	000306			BNE GOAGIN			
5181 035754 105267	000106			BITB #40,\$ENVM			
5182 035760 001033				BNE ACT			
5183 035762 132767	000040	142331		CMP #42,#\$ENDAD			
5184 035770 001017				BEQ ACT			
5185 035772 023727	000042	036040		MOV #MSG,R0			
5186 036000 001413				WAIT: TSTB #4TPS			
5187 036002 012700	036070			BPL WAIT			
5188 036006 105737	177564			CMPB (R0),#377			
5189 036012 100375				BEQ ACT			
5190 036014 121027	000377			MOVB (R0)+,#TPB			
5191 036020 001403				BR WAIT			
5192 036022 112037	177566			ACT: MOV #42,R0			
5193 036026 000767				BEQ GOAGIN			
5194 036030 013700	000042		RESET				
5195 036034 001405				\$ENDAD: JSR PC,(R0)		:ACT HOOKS	
5196 036036 000005				NOP			
5197 036040 004710				NOP			
5198 036042 000240				NOP			
5199 036044 000240				GOAGIN: JMP RESTRT		:DO NEXT PASS	
5200 036046 000240				EOP1: MOV #772,-(R2)		:MOVE TO MAILBOX # ***** 772 *****	
5201 036050 000167	143046			INC -(R2)		:SET MSGTYP TO FATAL ERROR	
5202 036054 012742	000772			HALT		:SEQUENCE ERROR	
5203							
5204							
5205 036064 001100				START			
5206							
5207 036066 177777			PASSPT: -1				
5208 036070 015	012	000	MSG: .ASCII <15><12><0><0><0><0><0><0>.END OF.				
036073 000	000	000					
036076 000	000	105					
036101 116	104	040					
036104 117	106						
5209 036106 040	040	103		.ASCII . CKKAAAO 11/44 CPU/EIS.<0><0><0><377>			
036111 113	113	101					
036114 101	101	060					
036117 040	061	061					
036122 057	064	064					
036125 040	103	120					
036130 125	057	105					
036133 111	123	000					
036136 000	000	377					
5210			EVEN				
5211 036142 000402			BRTAB: BR .+6				
5212 036144 001002			BNE .+6				
5213 036146 001402			BEQ .+6				
5214 036150 002002			BGE .+6				

5215 036152 002402		BLT .+6	
5216 036154 003002		BGT .+6	
5217 036156 003402		BLE .+6	
5218 036160 100002		BPL .+6	
5219 036162 100402		BMI .+6	
5220 036164 101002		BHI .+6	
5221 036166 101402		BLOS .+6	
5222 036170 102002		BVC .+6	
5223 036172 102402		BVS .+6	
5224 036174 103002		BCC .+6	; SAME AS BHIS
5225 036176 103402		BCS .+6	; SAME AS BLO
5226 036200 000000		\$TMP0: .WORD 0	
5227 036202 000000		\$TMP1: .WORD 0	
5228 036204 000000		\$TMP2: .WORD 0	
5229 036206 000000		\$TMP3: .WORD 0	
5230 036210 000000		SEPIRQ: .WORD 0 ;ERROR PIRQ.	
5231 036212 000000		SLPADR: .WORD 0	
5232 036214 000000		SLPERR: .WORD 0 ;ERROR LOOP	
5233 000002	.RADIX 2		
5234 036216 177777	YNTAB:	1111111111111111	:BR
5235 036220 170360		1111000011110000	:BNE: Z=0
5236 036222 007417		0000111100001111	:BEQ: Z=1
5237 036224 146063		1100110000110011	:BGE: N XOR V =0
5238 036226 031714		0011001111001100	:BLT: N XOR V =1
5239 036230 140060		11000000000110000	:BGT: Z+(N XOR V) =0
5240 036232 037717		0011111110011111	:BLE: Z+(N XOR V) =1
5241			
5242 036234 177400		1111111100000000	:BPL: N=0
5243 036236 000377		0000000011111111	:BMI: N=1
5244 036240 120240		1010000010100000	:BHI: C+Z=0
5245 036242 057537		0101111101011111	:BLOS: C+Z=1
5246 036244 146314		1100110011001100	:BVC: V=0
5247 036246 031463		0011001100110011	:BVS: V=1
5248 036250 125252		1010101010101010	:BCC: C=0
5249 036252 052525		0101010101010101	:BCS: C=1
5250 000010	.RADIX 8		
5251			
5252 036254 012737	036264 000024	PWRDN: MOV #PWRUP, @#24	; SET UP FOR A POWER UP
5253 036262 000000		HALT	
5254			
5255 036264 012737	036254 000024	PWRUP: MOV #PWRDN, @#24	; SET UP FOR A POWER FAIL
5256 036272 012706	001000 142015	MOV #STBOT, R6	; SET UP STACK POINTER
5257 036276 132767	000040	BITB #40, \$ENV	; SHOULD PRINT?
5258 036304 001010		BNE PWR2	: IF NOT: BR
5259 036306 012700	036332	MOV #PFMES, R0	: GET POWER FAIL MESSG.
5260 036312 105737	177564	WATE: TSTB @#TPS	: TTY READY?
5261 036316 100375		BPL WATE	: IF NOT: BR
5262 036320 112037	177566	MOVB (R0)+, @#TPB	: PRINT NEXT CHAR.
5263 036324 001372		BNE WATE	: IF NOT DONE: BR
5264 036326 000137	001100	PWR2: JMP @#START	: START PROGRAM AGAIN
5265			
5266			
5267 036332 012	015 120	PFMES: .ASCIZ <12><15>.POWER FAILURE.<12><15>	
036335	117 127		105
036340	122 040		106
036343	101 111		114
036346	125 122		105

5268	036351	012	015	000	.EVEN			
5269	036354				.BLKW	6		
5270	036370				USTBOT:			
5271					;*****			
5272					; THE FOLLOWING ARE SPECIAL CPU TRAP			
5273					HANDLERS TO TRAP AND REPORT SPECIAL TRAPS.			
5274					;			
5275					;			
5276					;			
5277	036370				T04:			
	036370	012742	000773		MOV	#773,-(R2)	:MOVE TO MAILBOX # *****	773 *****
	036374	005242			INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
	036376	000000			HALT		:TRAPPED THRU LOC. 4	
5278	036400				T010:			
	036400	012742	000774		MOV	#774,-(R2)	:MOVE TO MAILBOX # *****	774 *****
	036404	005242			INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
	036406	000000			HALT		:TRAPPED THRU LOC. 10	
5279	036410				T014:			
	036410	012742	000775		MOV	#775,-(R2)	:MOVE TO MAILBOX # *****	775 *****
	036414	005242			INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
	036416	000000			HALT		:TRAPPED THRU LOC. 14	
5280	036420				T030:			
	036420	012742	000776		MOV	#776,-(R2)	:MOVE TO MAILBOX # *****	776 *****
	036424	005242			INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
	036426	000000			HALT		:TRAPPED THRU LOC. 30	
5281	036430				T034:			
	036430	012742	000777		MOV	#777,-(R2)	:MOVE TO MAILBOX # *****	777 *****
	036434	005242			INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
	036436	000000			HALT		:TRAPPED THRU LOC. 34	
5282	036440				T0114:			
	036440	012742	001000		MOV	#1000,-(R2)	:MOVE TO MAILBOX # *****	1000 *****
	036444	005242			INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
	036446	000000			HALT		:TRAPPED THRU LOC. 114	
5283	036450				T0244:			
	036450	012742	001001		MOV	#1001,-(R2)	:MOVE TO MAILBOX # *****	1001 *****
	036454	005242			INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
	036456	000000			HALT		:TRAPPED THRU LOC. 244	
5284	036460				T0250:			
	036460	012742	001002		MOV	#1002,-(R2)	:MOVE TO MAILBOX # *****	1002 *****
	036464	005242			INC	-(R2)	:SET MSGTYP TO FATAL ERROR	
	036466	000000			HALT		:TRAPPED THRU LOC. 250	
5285	036470	000000			SPSW:	0		
5286	036472	000000			SUBT:	.WORD	0	
5287	036474	036472			SUBT1:	.WORD	SUBT	
5288	036476	000002			S1:	2		
5289	036500	036476			S2:	S1		
5290	036502	177771			S3:	-7		
5291	036504	036502			S4:	S3		
5292					END:	0		
5293	036506	000000						
5294		000001						

A	034466	APASS = 000000	BIT7 = 000200	DEC5	017766	DOP2	010550
ABASE = 000000		APRIOR= 000000	BIT8 = 000400	DEC6	017776	DOP4	014052
ACDW1 = 000000		AROUND 023766	BIT9 = 001000	DEC7	020020	DOP5	014136
ACDW2 = 000000		ASL1 021770	BPTVEC= 000014	DISPRE	000174	DST.PT	035564
ACPUOP= 000000		ASL2 022000	BRCT 024024	DNMB0A	011120	DSWR =	177570
ACT 036030		ASL3 022016	BRC1 003440	DNMB0B	011130	EIS	025214
ADC1 020454		ASL4 022026	BRC2 003450	DNMB2A	011356	EMTVEC=	000030
ADC2 020464		ASL5 022042	BRC3 003460	DNMB2B	011366	END	036506
ADC3 020504		ASL6 022052	BRH 023776	DNMB2C	011402	ENDABO	035732
ADC4 020514		ASL7 022076	BRN1 003320	DNMB2D	011416	ENDMPC	034554
ADC5 020532		ASR1 022140	BRN2 003330	DNMB2E	011426	ENDPAS	035740
ADDNI = 076150		ASR2 022150	BRN3 003340	DNMB2F	011444	EOP1	036054
ADDW0 = 000000		ASR3 022172	BRTAB 036142	DNMB3A	011526	ER	024010
ADDW1 = 000000		ASR4 022202	BRV1 003370	DNMB3B	011536	ERROR =	104000
ADDW10= 000000		ASR5 022216	BRV2 003400	DNMB3C	011554	ERRVEC=	000004
ADDW11= 000000		ASR6 022226	BRV3 003410	DNMB3D	011572	FILL =	000377
ADDW12= 000000		ASR7 022256	BRZ1 003250	DNMB3E	011602	GOAGIN	036050
ADDW13= 000000		ASWREG= 000000	BRZ2 003260	DNMB4A	011772	HIADRS=	177742
ADDW14= 000000		ATESTN= 000000	BRZ3 003270	DNMB4B	012002	HITMIS=	177752
ADDW15= 000000		AUNIT = 000000	BR1 001172	DNMB4C	012020	HT =	000011
ADDW2 = 000000		AUSWR = 000000	BR2 001202	DNMB4D	012030	IJMP	016434
ADDW3 = 000000		AVECT1= 000000	BR3 001214	DNMB4E	012040	IJMP4	016206
ADDW4 = 000000		AVECT2= 000000	BR4 001222	DNMB4F	012054	IJMP5	016376
ADDW5 = 000000		B 034472	BR5 001232	DNM03A	010212	INC1	017600
ADDW6 = 000000		BIC1 017420	BTCON 024314	DNM03B	010222	INC2	017610
ADDW7 = 000000		BIC2 017430	BTERR 024300	DNM03C	010232	INC3	017632
ADDW8 = 000000		BIC3 017446	CACHVE= 000114	DNM1	010064	INC4	017642
ADDW9 = 000000		BIS1 017510	CC 023772	DNM1A	011176	INC5	017656
ADD1 020270		BIS2 017520	CCERR 024534	DNM1B	011206	IOTVEC=	000020
ADD2 020300		BIS3 017540	CC1 024422	DNM2	010100	JMPCK	016436
ADD3 020314		BITCHK 024156	CC2 024436	DNM2A	011254	JMPERR	024350
ADD4 020324		BITCLR 024104	CHECK 034516	DNM2B	011264	JMPSEQ	016456
ADD5 020342		BITCON 024240	CLRCRD 024420	DNM2C	011272	JMPT	024340
ADD6 020352		BITSET 024122	CLR1 020056	DNM2D	011302	JMP2	016210
ADD7 020364		BIT0 = 000001	CMP1 020720	DNM3	010116	JMP2A	016226
ADD8 020374		BIT00 = 000001	CMP2 020730	DNM4	010140	JMP3	016136
ADD9 020414		BIT01 = 000002	CMP3 020752	DNM4A	011664	JMP3A	016154
ADEVCT= 000000		BIT02 = 000004	CMP4 020762	DNM4B	011674	JMP3B	016174
ADEVVM = 000000		BIT03 = 000010	CMP5 021006	DNM4C	011710	JMP4	016240
AENV = 000000		BIT04 = 000020	CMP6 021016	DNM5A	012134	JMP4A	016256
AENVVM = 000000		BIT05 = 000040	CMP7 021036	DNM5B	012144	JMP4B	016276
AFATAL= 000000		BIT06 = 000100	COM1 021076	DNM5C	012162	JMP5	016344
AMADR1= 000000		BIT07 = 000200	CONT 024026	DNM6A	012242	JMP5A	016364
AMADR2= 000000		BIT08 = 000400	CTRL= 177746	DNM6B	012252	JMP6	016310
AMADR3= 000000		BIT09 = 001000	CON1 024452	DNM6C	012270	JMP6A	016330
AMADR4= 000000		BIT1 = 000002	CON2 024544	DNM7A	012352	JMP7	016400
AMAMS1= 000000		BIT10 = 002000	CPUERR= 177766	DNM7B	012362	JMP7A	016420
AMAMS2= 000000		BIT11 = 004000	CR = 000015	DNM7C	012400	JSRCK	017110
AMAMS3= 000000		BIT12 = 010000	CRLF = 000200	DOPB2A	010624	JSRCKA	017104
AMAMS4= 000000		BIT13 = 020000	D 034476	DOPB2B	010702	JSRCK1	017126
AMSGAD= 000000		BIT14 = 040000	DA 034510	DOP0A	007626	JSRSEQ	017106
AMSGLG= 000000		BIT15 = 100000	DAERR 024230	DOP0B	007652	JSR0	016472
AMSGTY= 000000		BIT2 = 000004	DDISP = 177570	DOP0C	007672	JSR1	016476
AMTYP1= 000000		BIT3 = 000010	DEC1 017716	DOP0D	007722	JSR1A	016520
AMTYP2= 000000		BIT4 = 000020	DEC2 017726	DOP03A	010000	JSR2	016610
AMTYP3= 000000		BIT5 = 000040	DEC3 017742	DOP03B	010010	JSR2A	016640
AMTYP4= 000000		BIT6 = 000100	DEC4 017752	DOP1	010436	JSR2B	016650

JSR3	016530	MAPH00= 170202	MAPL2 = 170210	MDM7A	013676	NEG50	005766	
JSR3A	016570	MAPH01= 170206	MAPL20= 170300	MDM7B	013706	NEG51	005776	
JSR3B	016600	MAPH02= 170212	MAPL21= 170304	MDM7C	013724	NEG52	006012	
JSR4	016672	MAPH03= 170216	MAPL22= 170310	MDM7D	013744	NEG60	006070	
JSR4A	016710	MAPH04= 170222	MAPL23= 170314	MDM7E	013770	NEG61	006100	
JSR4B	016720	MAPH05= 170226	MAPL24= 170320	MEMERR=	177744	NEG70	006150	
JSR5	016776	MAPH06= 170232	MAPL25= 170324	MFPD0	024642	NEG71	006160	
JSR5A	017022	MAPH07= 170236	MAPL26= 170330	MFPD0A	024670	PASSPT	036066	
JSR5B	017032	MAPH1 = 170206	MAPL27= 170334	MFPI0	023500	PDRTAB	035672	
JSR6	016732	MAPH10= 170242	MAPL3 = 170214	MFPI0A	023526	PFMES	036332	
JSR6A	016756	MAPH11= 170246	MAPL30= 170340	MFPT =	000007	PIRQ =	177772	
JSR6AD	017102	MAPH12= 170252	MAPL31= 170344	MMHDLR	035546	PIRQVE=	000240	
JSR6B	016766	MAPH13= 170256	MAPL32= 170350	MMR0 =	177572	PRO =	000000	
JSR7	017044	MAPH14= 170262	MAPL33= 170354	MMR1 =	177574	PR1 =	000040	
JSR7A	017062	MAPH15= 170266	MAPL34= 170360	MMR2 =	177576	PR2 =	000100	
JSR7B	017072	MAPH16= 170272	MAPL35= 170364	MMR3 =	172516	PR3 =	000140	
KDPAR0=	172360	MAPH17= 170276	MAPL36= 170370	MMVEC =	000250	PR4 =	000200	
KDPAR1=	172362	MAPH2 = 170212	MAPL37= 170374	MOVCI =	076130	PR5 =	000240	
KDPAR2=	172364	MAPH20= 170302	MAPL4 = 170220	MOV1	017240	PR6 =	000300	
KDPAR3=	172366	MAPH21= 170306	MAPL5 = 170224	MOV2	017250	PR7 =	000340	
KDPAR4=	172370	MAPH22= 170312	MAPL6 = 170230	MOV3	017266	PS =	177776	
KDPAR5=	172372	MAPH23= 170316	MAPL7 = 170234	MRK1	022646	PSW =	177776	
KDPAR6=	172374	MAPH24= 170320	MBDM2A	012614	MRK2	022670	PUSRNM =	030000
KDPAR7=	172376	MAPH25= 170326	MBDM2B	012624	MRK3	022700	PWRDN	036254
KDPDR0=	172320	MAPH26= 170332	MBDM2C	012642	MRK4	022722	PWRUP	036264
KDPDR1=	172322	MAPH27= 170336	MBDM2D	012654	MRK5	022734	PWRVEC=	000024
KDPDR2=	172324	MAPH3 = 170216	MBDM2E	012664	MRK6	022750	PWR2	036326
KDPDR3=	172326	MAPH30= 170342	MBDM2F	012702	MSG	036070	REG1	002130
KDPDR4=	172330	MAPH31= 170346	MBDM4A	013236	MTPD0	024750	REG1A	002174
KDPDR5=	172332	MAPH32= 170352	MBDM4B	013254	MTPIO	023612	REG1E	002142
KDPDR6=	172334	MAPH33= 170356	MBDM4C	013266	NBR	024002	REG2	002244
KDPDR7=	172336	MAPH34= 170362	MBDM4D	013276	NEG00	004410	REG2A	002272
KERSTK=	001100	MAPH35= 170366	MBDM4E	013312	NEG01	004420	REG2B	002320
KIPAR0=	172340	MAPH36= 170372	MDM1A	012450	NEG02	004434	REG2C	002352
KIPAR1=	172342	MAPH37= 170376	MDM1B	012460	NEG03	004450	REG3	002400
KIPAR2=	172344	MAPH4 = 170222	MDM2A	012522	NEG04,	004460	REG3A	002444
KIPAR3=	172346	MAPH5 = 170226	MDM2B	012532	NEG1	020574	REG3E	002412
KIPAR4=	172350	MAPH6 = 170232	MDM2C	012540	NEG10	004524	REG4	002514
KIPAR5=	172352	MAPH7 = 170236	MDM2D	012550	NEG11	004534	REG4A	002560
KIPAR6=	172354	MAPL0 = 170200	MDM3A	012756	NEG12	004552	REG4E	002526
KIPAR7=	172356	MAPL00= 170200	MDM3B	012766	NEG13	004566	REG5	002630
KIPDR0=	172300	MAPL01= 170204	MDM3C	013004	NEG14	004576	REG5A	002674
KIPDR1=	172302	MAPL02= 170210	MDM3D	013024	NEG2	020604	REG5E	002642
KIPDR2=	172304	MAPL03= 170214	MDM3E	013052	NEG20	004644	REG6	002744
KIPDR3=	172306	MAPL04= 170220	MDM4A	013132	NEG21	004654	REG6A	003010
KIPDR4=	172310	MAPL05= 170224	MDM4B	013142	NEG22	004702	REG6E	002756
KIPDR5=	172312	MAPL06= 170230	MDM4C	013156	NEG3	020626	REN	033434
KIPDR6=	172314	MAPL07= 170234	MDM5A	013362	NEG30	005224	RESR	035622
KIPDR7=	172316	MAPL1 = 170204	MDM5B	013372	NEG31	005234	REST	023030
KMTSTS	035140	MAPL10= 170240	MDM5C	013410	NEG32	005250	RESTR	001122
KSP =%	000006	MAPL11= 170244	MDM5D	013426	NEG33	005274	RESVEC=	000010
LF =	000012	MAPL12= 170250	MDM5E	013454	NEG34	005310	ROL1	021460
LKS =	177546	MAPL13= 170254	MDM6A	013524	NEG4	020636	ROL2	021470
LKVEC =	000100	MAPL14= 170260	MDM6B	013534	NEG40	005666	ROL3	021506
LOADRS=	177740	MAPL15= 170264	MDM6C	013552	NEG41	005676	ROL4	021516
MAINT =	177750	MAPL16= 170270	MDM6D	013572	NEG42	005712	ROL5	021532
MAPHO =	170202	MAPL17= 170274	MDM6E	013622	NEG5	020656	ROL6	021542

ROL7	021564	SB2	015544	SIZELO=	177760	SOP1B	003736	SW08	= 000400
ROR1	021626	SB4	015670	SMTSTS	035254	SOP2B	004170	SW09	= 001000
ROR2	021636	SB5	015756	SNMB0A	006354	SOP3A	004754	SW1	= 000002
ROR3	021654	SB5A	015750	SNMB1A	006460	SOP3B	004770	SW10	= 002000
ROR4	021664	SB5X	015766	SNMB1B	006470	SOP4A	005366	SW11	= 004000
ROR5	021702	SB5XAD	015770	SNMB1C	006512	SOP4B	005406	SW12	= 010000
ROR6	021712	SB6	016030	SNMB2A	006634	SOP5A	005450	SW13	= 020000
ROR7	021726	SB6X	016040	SNMB2B	006644	SOP5B	005464	SW14	= 040000
ROTX	015244	SB7	016100	SNMB2D	006700	SOP6A	005530	SW15	= 100000
ROTXAD	015370	SB7X	016110	SNMB2E	006710	SOP6B	005544	SW2	= 000004
ROTOA	014362	SB7XAD	016112	SNMB3A	007052	SOP7B	005626	SW3	= 000010
ROTOB	014372	SCOPE	= 000004	SNMB3B	007062	SPSW	036470	SW4	= 000020
ROTOC	014414	SC3	024514	SNMB3C	007100	SRC.PT	035560	SW5	= 000040
ROT1A	014462	SC4	024530	SNMB3D	007110	SR0	= 177572	SW6	= 000100
ROT1B	014472	SDPAR0	= 172260	SNM0A	006314	SR1	= 177574	SW7	= 000200
ROT1C	014516	SDPAR1	= 172262	SNM1A	006416	SR2	= 177576	SW8	= 000400
ROT1D	014526	SDPAR2	= 172264	SNM2A	006554	SR3	= 172516	SW9	= 001000
ROT1E	014556	SDPAR3	= 172266	SNM2B	006564	SSP	=%000006	SXT0	022324
ROT2A	014630	SDPAR4	= 172270	SNM3A	006764	SSP1A	023100	SXT1	022334
ROT2B	014640	SDPAR5	= 172272	SNM3B	006774	SSP2	023114	SXT2	022364
ROT2C	014670	SDPAR6	= 172274	SNM4A	007160	STACK	= 001100	SYSTID	= 177764
ROT2D	014700	SDPAR7	= 172276	SNM4B	007170	START	001100	S1	036476
ROT2E	014734	SDPDR0	= 172220	SNM5A	007242	STBOT	= 001000	S2	036500
ROT3A	015002	SDPDR1	= 172222	SNM5B	007252	STKLMT	= 177774	S3	036502
ROT3B	015012	SDPDR2	= 172224	SNM6A	007326	STK1	035670	S4	036504
ROT3C	015040	SDPDR3	= 172226	SNM6B	007336	SUBT	036472	TBITVE	= 000014
ROT3D	015050	SDPDR4	= 172230	SNM7A	007410	SUBT1	036474	TBL1	014072
ROT3E	015076	SDPDR5	= 172232	SNM7B	007420	SUB0	007554	TBL2	014156
ROT4	015152	SDPDR6	= 172234	SOB1	022526	SUB0A	007564	TEST1	020114
ROT5	015234	SDPDR7	= 172236	SOB2	022534	SUB1	021140	TEST2	020124
ROT6	015304	SETBR	023662	SOB3	022544	SUB2	021150	TEST3	020142
ROT7	015360	SETCC	023702	SOB4	022564	SUB3	021172	TKVEC	= 000060
RTS1	017174	SETCD	024512	SOPA	006232	SUB4	021202	T010	036400
R1ERR	002212	SETPDR	035066	SOPB	006252	SUB5	021220	T014	036440
R10	=%000000	SETUP	023644	SOPB0A	003656	SUB6	021230	T0244	036450
R11	=%000001	SET2BR	023752	SOPB0B	003666	SUB7	021250	T0250	036460
R12	=%000002	SHL	001600	SOPB1A	004000	SUPSTK	= 000700	T030	036420
R13	=%000003	SHLE	001614	SOPB1B	004016	SVR0	035654	T034	036430
R14	=%000004	SHR	001714	SOPB1C	004062	SVR1	035656	T04	036370
R15	=%000005	SHRE	001730	SOPB1D	004102	SVR2	035660	TPB	= 177566
R2ERR	002342	SIPAR0	= 172240	SOPB2A	004236	SVR3	035662	TPS	= 177564
R3ERR	002462	SIPAR1	= 172242	SOPB2B	004256	SVR4	035664	TPVEC	= 000064
R4ERR	002576	SIPAR2	= 172244	SOPB2C	004326	SVR5	035666	TRAPVE	= 000034
R5FRR	002712	SIPAR3	= 172246	SOPB2D	004352	SWB1	020202	TRTVEC	= 000014
R6	=%000006	SIPAR4	= 172250	SOPB3A	005040	SWB2	020212	TST1	001154
R6ERR	003026	SIPAR5	= 172252	SOPB3B	005064	SWB3	020230	TST10	001554
R7	=%000007	SIPAR6	= 172254	SOPB3C	005132	SWREG	000176	TST100	006522
SA	034502	SIPAR7	= 172256	SOPB3D	005154	SW0	= 000001	TST101	006602
SAVR	035570	SIPDR0	= 172200	SOPX	006216	SW00	= 000001	TST102	006726
SBC1	021312	SIPDR1	= 172202	SOPXAD	006262	SW01	= 000002	TST103	007012
SBC2	021322	SIPDR2	= 172204	SOPZA	004150	SW02	= 000004	TST104	007126
SBC3	021340	SIPDR3	= 172206	SOPOA	003514	SW03	= 000010	TST105	007204
SBC4	021350	SIPDR4	= 172210	SOPOB	003534	SW04	= 000020	TST106	007270
SBC5	021366	SIPDR5	= 172212	SOPOC	003576	SW05	= 000040	TST107	007352
SBC6	021376	SIPDR6	= 172214	SOPOD	003622	SW06	= 000100	TST111	001624
SBC7	021416	SIPDR7	= 172216	SOP1A	003724	SW07	= 000200	TST110	007434
SBO	015422	SIZEHI	= 177762						

TST111	007470	TST174	015562	TST256	025544	TST34	003076	UIPAR1= 177642
TST112	007524	TST175	015624	TST257	025634	TST35	003134	UIPAR2= 177644
TST113	007600	TST176	015704	TST26	002536	TST36	003172	UIPAR3= 177646
TST114	007742	TST177	015772	TST260	025724	TST37	003230	UIPAR4= 177650
TST115	010032	TST2	001244	TST261	026014	TST4	001336	UIPAR5= 177652
TST116	010156	TST20	002152	TST262	026104	TST40	003300	UIPAR6= 177654
TST117	010242	TST200	016042	TST263	026216	TST41	003350	UIPAR7= 177656
TST12	001670	TST201	016114	TST264	026330	TST42	003420	UIPDR0= 177600
TST120	010300	TST202	016460	TST265	026442	TST43	003470	UIPDR1= 177602
TST121	010336	TST203	017136	TST266	026556	TST44	003550	UIPDR2= 177604
TST122	010374	TST204	017212	TST267	026666	TST45	003632	UIPDR3= 177606
TST123	010454	TST205	017276	TST27	002605	TST46	003676	UIPDR4= 177610
TST124	010514	TST206	017366	TST270	026776	TST47	003746	UIPDR5= 177612
TST125	010566	TST207	017456	TST271	027106	TST5	001374	UIPDR6= 177614
TST126	010642	TST21	002222	TST272	027216	TST50	004026	UIPDR7= 177616
TST127	010720	TST210	017550	TST273	027332	TST51	004112	UMTSTS 035404
TST13	001740	TST211	017666	TST274	027444	TST52	004200	USESTK= 000600
TST130	010762	TST212	020030	TST275	027546	TST53	004266	USP =%000006
TST131	011024	TST213	020066	TST276	027650	TST54	004362	USP1 023054
TST132	011066	TST214	020152	TST277	027752	TST55	004474	USP2 023140
TST133	011144	TST215	020240	TST3	001300	TST56	004614	USP2A 023224
TST134	011222	TST216	020424	TST30	002652	TST57	004720	USP3 023250
TST135	011320	TST217	020542	TST300	030054	TST6	001432	USP4 023274
TST136	011462	TST22	002276	TST301	030156	TST60	005000	USP5 023350
TST137	011622	TST220	020666	TST302	030260	TST61	005074	USP6 023374
TST14	001770	TST221	021046	TST303	030362	TST62	005164	USRM = 140000
TST140	011730	TST222	021106	TST304	030464	TST63	005334	USTBOT 036370
TST141	012072	TST223	021260	TST305	030576	TST64	005416	WAIT 036006
TST142	012202	TST224	021426	TST306	030710	TST65	005474	WATE 036312
TST143	012310	TST225	021574	TST307	031022	TST66	005554	XBIT1 017330
TST144	012420	TST226	021736	TST31	002722	TST67	005636	XBIT2 017340
TST145	012474	TST227	022106	TST310	031132	TST7	001476	XBIT3 017356
TST146	012566	TST23	002356	TST311	031242	TST70	005726	XOR1 022440
TST147	012722	TST230	022266	TST312	031352	TST71	006030	XOR2 022450
TST15	002022	TST231	022374	TST313	031462	TST72	006114	XOR3 022476
TST150	013100	TST232	022506	TST314	031570	TST73	006204	YBR 024006
TST151	013174	TST233	022574	TST315	031676	TST74	006264	YNTAB 036216
TST152	013330	TST234	022760	TST316	032004	TST75	006324	SAPTHD 000330
TST153	013472	TST235	023030	TST317	032112	TST76	006364	SCPUP 000326
TST154	013642	TST236	023140	TST32	002766	TST77	006426	SDEVCT 000310
TST155	014010	TST237	023420	TST320	032220	UDPAR0=	177660	SENDAD 036040
TST156	014074	TST24	002422	TST321	032300	UDPAR1=	177662	SENV 000320
TST157	014160	TST240	023526	TST322	032360	UDPAR2=	177664	SENVM 000321
TST16	002054	TST241	023634	TST323	032526	UDPAR3=	177666	SEPIRQ 036210
TST160	014244	TST242	024074	TST324	032634	UDPAR4=	177670	SERN = 001003
TST161	014330	TST243	024244	TST325	032742	UDPAR5=	177672	SERROR= 000302
TST162	014424	TST244	024320	TST326	033022	UDPAR6=	177674	SETABL 000320
TST163	014566	TST245	024360	TST327	033102	UDPAR7=	177676	SETEND 000330
TST164	014744	TST246	024564	TST33	003036	UDPDR0=	177620	SFATAL 000302
TST165	015106	TST247	024670	TST330	033162	UDPDR1=	177622	SHIBTS 000330
TST166	015162	TST25	002472	TST331	033374	UDPDR2=	177624	SLPADR 036212
TST167	015246	TST250	024772	TST332	033512	UDPDR3=	177626	SLPERR 036214
TST17	002106	TST251	025024	TST333	033576	UDPDR4=	177630	SMAIL 000300
TST170	015314	TST252	025214	TST334	034050	UDPDR5=	177632	SMBADR 000332
TST171	015372	TST253	025310	TST335	034212	UDPDR6=	177634	MSGAD 000314
TST172	015440	TST254	025374	TST336	034340	UDPDR7=	177636	MSGLG 000316
TST173	015502	TST255	025460	TST337	034562	UIPAR0=	177640	MSGTY 000300

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SYMBOL TABLE

D 1

SEQ 0210

\$PASS 000306	\$SWREG 000322	\$TMP2 036204	\$TSTM= 000304	\$X = 034350
\$PASTM 000336	\$TESTN 000304	\$TMP3 036206	\$UNIT 000312	\$XX = 177703
\$SVPC = 000200	\$TMPO 036200	\$TN = 000337	\$UNITM 000340	\$XXX = 000702
\$SWR = 000000	\$TMP1 036202	\$TSTM 000334	\$USWR 000324	.\$X = 001100

. ABS. 036510 000  
000000 001

ERRORS DETECTED: 3

VIRTUAL MEMORY USED: 20354 WORDS ( 80 PAGES)

DYNAMIC MEMORY: 20434 WORDS ( 78 PAGES)

ELAPSED TIME: 00:16:02

CKKAAA,CKKAAA/-SP/CRF/NL:TOC=CKKAAA0.MLB/ML,CKKAAA.P11