

11/70-74

11/70-74 POW FAIL  
CEKBGB0

AH-7984B-MC

COPYRIGHT 75-80  
FICHE 1 OF 1

JAN 1980

digital

MADE IN USA

This microfiche card contains a grid of frames, each containing a page of data. The data is organized into columns and rows, with some frames containing headers and footers. The text is too small to read clearly but appears to be a list or index of information.





IDENTIFICATION

8 1

SEQ 0001

PRODUCT CODE: AC-7983B-MC

PRODUCT NAME: CEKBGBO PDP-11/70-74MP System Power Fail Test

PRODUCT DATE: MAY, 1979

MAINTAINER: Diagnostic Engineering

DIAGNOSTIC ENGINEER: BILL SCHLITZKUS

THE INFORMATION IN THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE AND SHOULD NOT BE CONSTRUED AS A COMMITMENT BY DIGITAL EQUIPMENT CORPORATION. DIGITAL EQUIPMENT CORPORATION ASSUMES NO RESPONSIBILITY FOR ANY ERRORS THAT MAY APPEAR IN THIS DOCUMENT.

THE SOFTWARE DESCRIBED IN THIS DOCUMENT IS FURNISHED TO THE PURCHASER UNDER A LICENSE FOR USE ON A SINGLE COMPUTER SYSTEM AND CAN BE COPIED (WITH INCLUSION OF DIGITAL'S COPYRIGHT NOTICE) ONLY FOR USE IN SUCH SYSTEM, EXCEPT AS MAY OTHERWISE BE PROVIDED IN WRITING BY DIGITAL.

NO RESPONSIBILITY IS ASSUMED FOR THE USE OR RELIABILITY OF SOFTWARE ON EQUIPMENT THAT IS NOT SUPPLIED BY DIGITAL OR ITS AFFILIATED COMPANIES. COPYRIGHT (C) 1975, 1979 BY DIGITAL EQUIPMENT CORPORATION.

CONTENTS

- 1.0 ABSTRACT
- 2.0 REQUIREMENTS
  - 2.1 Equipment
  - 2.2 Storage
  - 2.3 Preliminary Procedures
- 3.0 Loading Procedure
- 4.0 Starting Procedure
  - 4.1 Starting Address
  - 4.2 Control Switch Settings
  - 4.3 Restarting Procedure
  - 4.4 Program and/or Operator action.
- 5.0 Operating Procedures
  - 5.1 Modes of Operation
  - 5.2 Common Procedures
  - 5.3 Notes and Warnings
  - 5.4 Uniprocessor mode, no UBE
  - 5.5 Uniprocessor mode, with UBE
  - 5.6 Multiprocessor mode, no UBE
  - 5.7 Multiprocessor mode, with UBE
- 6.0 Errors and Error Reporting
- 7.0 Test Descriptions
- 8.0 Subroutine Abstracts
- 9.0 Restrictions
- 10.0 Miscellaneous

## 1.0 ABSTRACT

This diagnostic serves as a replacement to DEKBGA, the 11/70 Power Fail Test. It provides all of the coverage and features of the previous power fail test along with the added features of diagnostic support for multiprocessor systems using the KB11-CM Processor and the IIST interface.

The test is divided into two sections, Section 1 and Section 2. Section 1 completely replaces DEKBGA and basically serves as a test of CPU logic validity during a power fail sequence. This section can be run on a standard unmodified 11/70 processor as it utilizes no multiprocessor resources. Section 2 is enabled by enabling console switch 6. This section will be executed directly after section 1. This section provides testing for proper functionality of the Interprocessor Interrupt and Sanity Timer (IIST) powerfail procedures, and memory system activity during a loss of power on the system or one of its subsystems.

This diagnostic also supports the use of the UNIBUS Exerciser (UBE) to perform simulated powerfail sequences during the execution of Section 1.

## 2.0 REQUIREMENTS

### 2.1 Equipment

This test is designed to support three types of systems.

1. Standard single processor 11/70 systems with the KB-11B/C processor.
2. Standard single processor 11/74 systems with the KB-11CM processor
3. Standard multiprocessor 11/74 systems with MKA11 memory using KB-11CM central processors connected with an IIST interprocessor interface.

At least one console terminal is required for message and error reporting on any of the above specified systems.

Optional equipment includes Unibus Exercisers for all system types and mass storage devices (RPO 5/6, massbus Exercisor) for type 3 systems.

### 2.2 Storage

The Power Fail test runs in 12K words of memory. The first 4K is used for stack areas and common access data. The second 4K contains the program itself. The only data elements that reside here are type and error messages, and execution flow and control variables that are used

(modified) when the processor runs in multiprocessor mode. The next 4K is used as buffer space for massbus transfers that occur during test 21.

### 2.3 Preliminary Procedures.

All standard 11/70-74 CPU diagnostics should first be run to insure proper operation under a secure power condition. Specifically, the IIST diagnostic and Unibus Exerciser diagnostics should be run. If massbus devices are to be used for test 21 it might be wise to insure that the devices are in proper working order. The power fail diagnostic may use all massbus drives and memory boxes accessible by the CPUs participating in this diagnostic. Therefore, it is important to switch offline to participating CPUs all data storage equipment that the operator does not want corrupted by this diagnostic. Before starting the power-fail diagnostic the operator should also be sure that the CPU power-up action switches (on the IIST front panel) are all 'Run or Halt' for participating CPUs, the IIST enable switches are 'online', and the IIST configuration switches are all at the same system for all participating CPUs. All participating memory boxes should be online to all participating CPUs.

The operator of this test should be familiar with the MKA11 and IIST boot/control panel.

### 3.0 LOADING PROCEDURE

This diagnostic can be loaded within the standard XXDP loading procedure. Note that if this diagnostic is being run as part of a chain that it must be the last element in that chain.

This diagnostic is loadable under the APT system but can only be run under API in Uniprocessor mode with the UBE enabled.

### 4.0 STARTING PROCEDURE

#### 4.1 Starting Address

The starting address for this diagnostic is 200. The restart address is 220.

## 4.2 Control Switch Settings

The switch settings are as follows (when set to 1):

- SW15 - Halt on Error
- SW14 - Loop on test (Section 1 only)
- SW08 - Enable System Power Fail Test (Test 25)
- SW07 - Disable Section 1 Tests (Multiprocessor mode only)

SW6	SW5	
0	0	Uniprocessor mode, manual powerfail. (this mode can be used as a replacement for previous powerfail diagnostic)
0	1	Uniprocessor mode, automatic (UBE) powerfail (uniprocessor mode that should be used under APT)
1	0	Multiprocessor mode, manual powerfail. Both sections (1 and 2) are executed.
1	1	Multiprocessor mode, automatic (UBE) powerfail. Only Section 1 will use the UBE. Each CPU must have a UBE.

Note that for the multiprocessor modes (SW6 enabled) the IIST 'system' ID of each CPU participating in the test should be specified by setting the appropriate bit in Switches 0-3 in the switch register. For example, if all processors in a 4 processor system are to be tested then switches 0-3 should be enabled. If only CPU's 0 and 2 are to participate then only switches 0 and 2 should be enabled.

The switches are defined by the master CPU only (in multiprocessor mode), where the master is the CPU that starts or restarts the program. Each slave CPU uses the switch definitions of the master.

The Program will not interpret changes to the switches in multiprocessor mode while the program is running. The program must be restarted.

## 4.3 Restarting Procedures

The restart address for this diagnostic is 220. A restart should be considered a completely new session therefore be sure the proper switches are enabled for the features that you want.

## 4.4 Program And/Or Operator Action

## NOTE

SEQ 0006

Be sure to isolate the CPU's that are to participate in the powerfail test from other CPU's that are to remain functional. Participating CPU's should have the IIST configuration switches found on the IIST panel switched to the SYSTEM B position (if this is the default position for the installation then the SYSTEM A position could be used).

## 5.0 OPERATING PROCEDURES

## 5.1 Modes Of Operation

This diagnostic is designed to run in four basic modes specified by the selection of bits 5 & 6 in the console switch register. It should be noted that if a multiprocessor mode is chosen (SW6 enabled) that the first CPU started will become the 'master' and successively start the remaining participating CPU's, the 'Slaves'.

## 5.2 Common Procedures

Load address 200 and then enable the switches for the test mode that is desired. Remember to enable the appropriate CPU mask bit if you are running a multiprocessor mode. When this has been done insure that all slaves are powered up and have their halt switches in the 'enable' state if MP mode is to be used. Hit start - the program name will be typed followed by the mode the diagnostic is running in (uniprocessor or multi-processor) followed by the contents of the switch register and whether the Unibus Exerciser will be used to simulate power fails.

## 5.3 Notes And Warnings

1. Power failures in section 1 are only allowed when expected. Therefore in manual mode do not remove the power until the test number appears in the display register.
2. Power failures are not allowed during the execution of the End of Pass (EOP) routines. Note that the number displayed during the End of Pass is the Pass number NOT the test number.
3. When running the diagnostic in uniprocessor mode on a single CPU that is part of a multiprocessor system make sure that the IIST configuration switch for the respective CPU is in the STAND ALONE position and the IIST ENABLE switch is in the

OFF LINE position.

4. When running in multiprocessor mode insure that the subsystem under test is isolated from any system that is still running by switching the CPU's under test to an alternate position with the IIST CONFIGURATION switches. For example, if the default system normally runs on the 'SYSTEM A' position, switch the subsystem under test to the 'SYSTEM B' position.

#### 5.4 Uniprocessor Mode, No UBE

The diagnostic will instruct you to "interrupt the power after the test number appears on the display". Interrupt the power only at this time. If the test is successful then the next test number should appear in the display. When the End of Pass is reached the Pass count will be typed. There are no error reports in Section 1 (except for unexpected traps to 4 and 114.) Normally, an error results in a processor halt.

#### 5.5 Uniprocessor Mode, With UBE

In this mode the UBE is used to perform the power Fail procedure. No "interrupt the power..." message is typed before the UBE takes action. The test number and pass number however do appear in the display register. An EOP message is typed equivalent to that of Section 5.4. Note that in this mode only the CPU logic involved in the power-fail sequence is tested. Failures that may occur because of problems in the Power system will go undetected.

#### 5.6 Multiprocessor Mode, No UBE

In multiprocessor mode the CPU that is initially started becomes the 'MASTER' CPU. What this means is that all error messages and typeouts will appear on this CPU's console. This CPU is also responsible for startup of "slave" CPU's. Slave CPU's are the remaining CPU's that are scheduled to participate in the test by their appropriate bit being set in switches 0-3 of the master CPU's SWR. When start is depressed and multi-processor mode is specified the program name, test mode, and switch register setting will be typed upon the master CPU console. The remaining CPU's will then be booted and then interrupted through the masters IIST. This will be followed by an "interrupt the power..." message.

The ID of the processor responsible for typeouts and error messages will precede the message:

0>

1>



n>

Run each processor through section 1 one at a time. After power-failing the last test in Section 1 (Test 16) on one CPU go on to the next CPU, etc. After the last test on the last CPU has been completed in Section 1, the operator will receive instructions at console.

Whereas there are no prompts printed at the console in Section 1, all power fails in Section 2 must be done in exact agreement with the typed-out instructions.

Section 2 prompts the operator to remove the power from a particular element of the system. If the expected results occur then the next element is tried. When all relevant elements have been tried then the diagnostic precedes to the next test. Section 2 contains tests 17 through 25.

#### 5.7 Multiprocessor Mode, With UBE

This mode is the same as 'multiprocessor mode, no UBE' except that Section 1 will be done without manual intervention. ALL CPUs that are to participate must have a UBE module.

#### 6.0 ERRORS AND ERROR REPORTING

Error reports are always typed out on the console of the CPU that was first started. This is the 'master' CPU in multiprocessor mode. All error messages are preceded by a tag as follows 'n>' where n's the IIST self-ID of the CPU encountering the error. Typing in multiprocessor mode is always done by the master. If the master is without power when typing is required, the messages will be queued and printed when power has been restored.

## 7.0 TEST DESCRIPTIONS

The tests that are found in section I are simple power fail tests that guarantee that the proper machine states are entered on power fail and power up. The test names are self-explanatory.

Section 1

1. Simple Down/Up test (Kernal node)
2. Program Volatility Test  
Verify that the memory bank containing the program will not be corrupted by CPU power fails.
3. Simple Down/Up test (Supervisor mode)
4. Simple Down/Up Test (User mode)
5. Power fail with odd address
6. Power Fail in the Red Zone
7. Power Fail with memory timeout (kernal)
10. Power Fail in the yellow zone.
11. Power Fail with resets.
12. Power Fail with odd address (Supervisor).
13. Power Fail with Timeout (Supervisor)
14. Power Fail with odd address (User)
15. Power Fail with timeout (User)
16. Memory Management Abort Test

Section 2

After all CPUs reach the beginning of Section 2, each CPU sizes for RP04/5/6 massbus devices. If no devices are found the following message is printed:

No Massbus Device Available On CPU #n

If the only massbus device found has its PGM bit set, the following message is printed:

Warning: Drive #n  
On CPU #r,  
Is accessible over Ports A and B

and will be used later in this diagnostic.

17. Check 'BRK' & 'DCF' FLAGS during power fail. Insure that the IIST's of functioning CPU's receive BRK & DCF signals corresponding to the CPU that performed a Power Fail.

The operator will be prompted with messages of the following type:

Power Fail CPU #n

After restoring power, each of the other CPUs should report:

CPU Interrupt As Expected

20. Check power fail during high memory activity. Insure that power down sequences can be performed by a CPU while other CPU's are contending for the memory bus.

The operator will be prompted with messages of the following type:

Power Fail CPU #n

There is no report from the other CPUs after restoring power.

21. Check power fail during massbus transfer. Insure that power down sequences can be performed by a CPU while other CPU's are performing massbus read operations. Also verify that the read operations don't experience any loss of data due to the power condition of an uninvolved CPU.

The operator will be prompted with messages of the following type:

Power Fail CPU #n

If there are no massbus devices for the other CPUs to use, then the following messages are printed instead of the above message:

No Massbus Device Available On CPU #n Proceeding  
To Next CPU.

There is no report from the other CPUs after restoring power.

22. Insure that a loss of AC power on a MKA11 semiconductor memory box does not cause a power fail sequence to occur on any processor that has a disabled part to that box.

The operator will be prompted with messages of the type:

Get Set To Power Fail Mem Box #n

Put battery backup on all memory boxes  
Make all memory ports offline only on mem box to be power failed  
Make all CPU power-up switches 'Run or Halt'

Now Power Fail The Mem Box

Restore power 5 seconds after power fail  
Restore all memory ports online  
Then type any character at the master console  
No CPU should report a power fail

The master should report 'OK'.

23. Check AC power fail on memory box. Insure that a loss of AC power on a MKA11 semiconductor memory box causes a power fail sequence to occur on any processor that has an enabled port to that box.

The operator will be prompted with message of the type:

Get Set To Power Fail Mem Box #n

Put battery backup on all memory boxes  
Make all memory ports online  
Make all CPU power-up switches 'Run or Halt'

Now power fail the mem box

Restore power 5 seconds after power fail then type any character at the master console. Each CPU should report a power failure.

Each CPU should report the following message:

Power Failure On CPU As Expected

24. Check DC Power Loss on a memory box. Insure that the slave CPU(s) specified through the IIST Boot/control panel perform a boot operation when AC & DC power are restored to the memory box.

The operator will be prompted with message of the type:

Get Set To Power Fail Mem Box #n

Disable battery backup on mem box to be power-failed. Put all slave CPU mem ports online. Make master CPU mem port offline only on box to be power-failed. Make all CPU power-up switches 'RUN OR Boot'.

Now Power Fail The Mem Box

Restore power 5 seconds after power fail  
Restore all mem ports online  
Restore all CPU power-up switches to 'Run or Halt'  
Then type any character at the master console  
Each slave should report an interrupt

Each slave CPU should report the following message:

CPU Interrupt As Expected

25. Check system recovery on power fail. Insure that a total momentary loss of AC power on a system level is recoverable without operator intervention.

The operator will be prompted with the following message:

Get Set to Power Fail Entire System...

Put battery backup on all mem boxes  
Make all memory ports online  
Make all CPU power-up switches 'Run or Halt'

Now Power Fail the Entire System  
Restore power 5 seconds after power fail

Each CPU should report the following:

## 8.0 MISCELLANEOUS

Test 24 will not be done on the memory box with base address 0. Therefore, in order to fully test all system elements the operator should restart this diagnostic a second time and switch the box with base address 0 with another box (using the thumbwheels to switch base addresses). The operator should also switch master CPUs on the restart.



Test 22 will be skipped if there is only one MKA11 memory box. Power failing through Section 1 with the UBE will not necessarily test power fail during odd address trap, timeout, etc. (it depends on when the UBE starts the power down). Therefore, it is recommended to manually power fail Section 1.

89	BASIC DEFINITIONS
215	CACHE REGISTER DEFINITIONS
225	CPU REGISTER DEFINITIONS
238	MEMORY MANAGEMENT DEFINITIONS
386	UNIBUS MAP REGISTER DEFINITIONS
477	IIST REGISTER DEFINITIONS
496	CONSOLE SWITCH SETTINGS
514	RJPO4 DEVICE REGISTERS
535	POWER FAIL FUNCTION TABLE BIT DIFINITIONS
546	TRAP CATCHER
555	ACT11 HOOKS
565	LOAD START AND RESTART VECTORS
572	APT PARAMETER BLOCK
594	COMMON TAGS
720	APT MAILBOX-ETABLE
880	ERROR POINTER TABLE
1106	BOOT AND INITIALIZE THE SLAVE CPUS
1170	INITIALIZE THE COMMON TAGS
1263	T1 SIMPLE DOWN/UP TEST (KERNAL)
1318	T2 PROGRAM VOLATILITY TEST
1354	T3 SIMPLE DOWN/UP TEST (SUPERVISOR)
1390	T4 SIMPLE DOWN/UP TEST (USER)
1426	T5 POWER FAIL WITH ODD ADDRESS
1452	T6 POWER FAIL IN THE RED ZONE
1493	T7 POWER FAIL WITH TIME OUT (KERNAL)
1523	T10 POWER FAIL IN THE YELLOW ZONE (KERNAL)
1570	T11 POWER FAIL WITH RESETS
1595	T12 POWER FAIL WITH ODD ADDRESS (SUPERVISOR)
1626	T13 POWER FAIL WITH TIME OUT (SUPERVISOR)
1657	T14 POWER FAIL WITH ODD ADDRESS (USER)
1688	T15 POWER FAIL WITH TIME OUT (USER)
1719	T16 MEMORY MANAGEMENT ABORT TEST
1781	SECTION 2 INITIALIZATION
1874	T17 CHECK 'BRK' & 'DCF' FLAGS DURING POWERFAIL
1979	T20 CHECK POWERFAIL DURING HIGH MEMORY ACTIVITY
2049	T21 CHECK POWERFAIL SEQUENCE DURING MASSBUS XFER
2196	T22 CHECK AC POWERFAIL ON MEM BOXES, PORTS DISABLED
2355	T23 CHECK AC POWERFAIL ON MEM BOXES, PORTS ENABLED
2513	T24 CHECK DC POWERFAIL ON MEM BOXES, CPUS BOOT ON POWER UP
2672	T25 CHECK SYSTEM RECOVERY ON AC POWER FAIL
2711	MEMORY BOX TEST ROUTINES
2848	PARITY ERROR HANDLER
2861	SETUP MEMORY MANAGMENT REGISTERS
2881	MASSBUS TRANSFER ROUTINES
2908	LINE CLOCK ROUTINE
2926	POWER FAIL ROUTINE (SECTION 1)
3034	POWER FAIL ROUTINE (SECTION 2)
3166	END OF PASS ROUTINE
3312	SCOPE HANDLER ROUTINE
3358	ERROR HANDLER ROUTINE
3471	APT COMMUNICATIONS ROUTINE
3528	BINARY TO OCTAL (ASCII) AND TYPE
3613	CONVERT BINARY TO DECIMAL AND TYPE ROUTINE
3682	TYPE SERVICE
3786	TRAP DECODER
3812	TRAP TABLE

MAINDEC-11-CEKGB-B PDP-11/70,74 SYSTEM POWER FAIL MACY11 30A(1052) 06-JUN-79 09:12  
CEKGBB.P11 05-JUN-79 09:14 TABLE OF CONTENTS

SEQ 0015

3840 DATA AREA

1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26  
27  
28  
29  
30  
31  
32  
33  
34  
35  
36  
37  
38  
39  
40  
41  
42  
43  
44  
45  
46  
47  
48  
49  
50  
51  
52  
53  
54  
55  
56

.TITLE MAINDEC-11-CEKGB-B PDP-11/70,74 SYSTEM POWER FAIL  
:\*COPYRIGHT (C) 1978  
:\*DIGITAL EQUIPMENT CORP.  
:\*MAYNARD, MASS. 01754  
:\*  
:\*PROGRAM BY JIM LACEY, JEFF WHITE, BILL SCHLITZKUS  
:\*  
:\*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC  
:\*PACKAGE (MAINDEC-11-DZQAC-C3), JAN 19, 1977.  
:\*

\*\*\*\*\*  
\*  
\* 11-70/74 SYSTEM POWER FAIL DIAGNOSTIC \*  
\*-----\*  
\* THIS DIAGNOSTIC IS DIVIDED INTO TWO SECTIONS: SECTION 1 TESTS THE \*  
\* BASIC ABILITY OF A PROCESSOR TO SUCCESSFULLY ENTER AND RECOVER \*  
\* FROM A POWER FAIL CONDITION. THIS SECTION REPLACES, IN FUNC- \*  
\* TIONALITY, THE PREVIOUS POWER FAIL DIAGNOSTIC DEKGBA AND PROVIDES \*  
\* EQUIVALENT DIAGNOSTIC COVERAGE. THIS SECTION AND ONLY THIS \*  
\* SECTION WILL BE RUN IF THE MP SWITCH (SWITCH 6) IS DISABLED. \*  
\* SECTION 2 OF THIS DIAGNOSTIC PROVIDES DIAGNOSTIC COVERAGE \*  
\* FOR MULTIPROCESSOR CONFIGURATIONS UTILIZING THE IIST INTERFACE \*  
\* AS A MEANS OF INTERPROCESSOR COMMUNICATION. IF THE MP SWITCH \*  
\* (SWITCH 6) IS ENABLED BOTH SECTION 1 AND SECTION 2 ARE PERFORMED, \*  
\* ALSO THE IIST IS USED IN SECTION 1 TO INITIALIZE AND START ALL \*  
\* PARTICIPATING PROCESSORS. SECTION 2 TESTS THE ABILITY OF A MULTI- \*  
\* PROCESSOR SYSTEM TO SUCCESSFULLY RECOVER FROM A POWER FAILURE \*  
\* EITHER IN A SELECTIVE SUBSYSTEM (MEMORY BOX OR PROCESSOR) OR ON \*  
\* A SYSTEM WIDE LEVEL DURING VARIOUS KINDS OF MEMORY AND I/O ACTIV- \*  
\* ITY. \*  
\* IN THE MULTIPROCESSOR MODE, ALL CPUS MUST ARRIVE AT THE \*  
\* ENTRY POINT TO SECTION 2 BEFORE ANY CPU WILL BEGIN SECTION 2 \*  
\* TESTING. IF SECTION 1 IS NOT SKIPPED AND THE UNIBUS EXERCISER \*  
\* IS NOT BEING USED, THE OPERATOR MUST POWER FAIL EACH CPU \*  
\*

```
57      ;:* MANUALLY THRU THE 16 TESTS OF SECTION 1 TO GET THE CPU TO THE      *
58      ;:* ENTRY POINT OF SECTION 2.                                         *
59      ;:*   BEFORE STARTING THE PROGRAM, BE SURE THAT THE CPU POWER-UP      *
60      ;:*   ACTION SWITCHES (ON THE IIST FRONT PANEL) ARE ALL                *
61      ;:*   'RUN OF HALT', THE IIST ENABLE SWITCHES ARE ONLINE, AND          *
62      ;:*   THE IIST CONFIGURATION SWITCHES ARE EITHER ALL SYSTEM 0 OR 1.    *
63      ;:* ALL PARTICIPATING MEMORY BOXES SHOULD BE ONLINE TO ALL PARTIC-    *
64      ;:* IPATING CPUS.                                                       *
65      ;:*****
66
67      ;SWITCH REGISTER DEFINITIONS
68
69      ;THE SWITCHES ARE DEFINED BY THE MASTER CPU ONLY,
70      ;WHERE THE MASTER IS THE CPU THAT STARTS OR RESTARTS
71      ;THE PROGRAM. EACH SLAVE CPU USES THE SWITCH DEFINITIONS
72      ;OF THE MASTER.
73
74      ;THE PROGRAM WILL NOT INTERPRET CHANGES TO THE
75      ;SWITCHES IN MULTIPROCESSOR MODE WHILE THE PROGRAM IS RUNNING. THE
76      ;PROGRAM MUST BE RESTARTED.
77
78      ;SW15=1      HALT ON ERROR
79      ;SW14=1      LOOP ON TEST (SECTION 1 ONLY)
80      ;SW08=1      ENABLE SYSTEM POWER FAIL TEST (TEST 25)
81      ;SW07=1      DISABLE SECTION 1 TESTS (MULTIPROCESSOR MODE ONLY)
82      ;SW06=1      ENABLE MULTIPROCESSOR MODE/SECTION 2 TESTS
83      ;SW05=1      ENABLE UNIBUS EXERCISERS (SECTION 1 ONLY, EACH CPU MUST HAVE A UBE)
84      ;SW03=1      TEST CPU #3 (IIST SELF ID), MULTIPROCESSOR MODE ONLY
85      ;SW02=1      TEST CPU #2      ..      ..
86      ;SW01=1      TEST CPU #1      ..      ..
87      ;SW00=1      TEST CPU #0      ..      ..
88
89      .SBTTL BASIC DEFINITIONS
90
91      ;*INITIAL ADDRESS OF THE STACK POINTER
92      013776      STACK= 13776      ;;FIRST ADDRESS OF THE STACK
93      013776      KERSTK= STACK      ;;KERNEL STACK
94      013576      SUPSTK= STACK-200  ;;SUPERVISOR STACK
95      013476      USESTK= STACK-300  ;;USER STACK
96      .EQUIV EMT,ERROR      ;;BASIC DEFINITION OF ERROR CALL
97      .EQUIV IOT,SCOPE      ;;BASIC DEFINITION OF SCOPE CALL
98      PS= 177776      ;;PROCESSOR STATUS WORD
99      .EQUIV PS,PSW
100     177774      STKLMT= 177774      ;;STACK LIMIT REGISTER
101     177772      PIRQ= 177772      ;;PROGRAM INTERRUPT REQUEST REGISTER
102     177570      DSWR= 177570      ;;HARDWARE SWITCH REGISTER
103     177570      DDISP= 177570     ;;HARDWARE DISPLAY REGISTER
104     177546      LKS= 177546      ;;LINE CLOCK (KW11-L) STATUS REGISTER
105
106     ;*MISCELLANEOUS DEFINITIONS
107     000011      HT= 11      ;;CODE FOR HORIZONTAL TAB
108     000012      LF= 12      ;;CODE LINE FEED
109     000015      CR= 15      ;;CODE CARRIAGE RETURN
110     000200      CRLF= 200     ;;CODE FOR CARRIAGE RETURN-LINE FEED
111
112     ;*GENERAL PURPOSE REGISTER DEFINITIONS
113     000000      RO= %0      ;;GENERAL REGISTER
```



```

113      000001      R1=      %1          ;;GENERAL REGISTER
114      000002      R2=      %2          ;;GENERAL REGISTER
115      000003      R3=      %3          ;;GENERAL REGISTER
116      000004      R4=      %4          ;;GENERAL REGISTER
117      000005      R5=      %5          ;;GENERAL REGISTER
118      000006      R6=      %6          ;;GENERAL REGISTER
119      000007      R7=      %7          ;;GENERAL REGISTER
120      .EQUIV      R0,R10      ;;GENERAL REGISTER
121      .EQUIV      R1,R11      ;;GENERAL REGISTER
122      .EQUIV      R2,R12      ;;GENERAL REGISTER
123      .EQUIV      R3,R13      ;;GENERAL REGISTER
124      .EQUIV      R4,R14      ;;GENERAL REGISTER
125      .EQUIV      R5,R15      ;;GENERAL REGISTER
126      000006      SP=      %6          ;;STACK POINTER
127      .EQUIV      SP,KSP      ;;KERNEL STACK POINTER
128      .EQUIV      SP,SSP      ;;SUPERVISOR STACK POINTER
129      .EQUIV      SP,USP      ;;USER STACK POINTER
130      000007      PC=      %7          ;;PROGRAM COUNTER

```

;\*PRIORITY LEVEL DEFINITIONS

```

133      000000      PR0=      0          ;;PRIORITY LEVEL 0
134      000040      PR1=      40         ;;PRIORITY LEVEL 1
135      000100      PR2=      100        ;;PRIORITY LEVEL 2
136      000140      PR3=      140        ;;PRIORITY LEVEL 3
137      000200      PR4=      200        ;;PRIORITY LEVEL 4
138      000240      PR5=      240        ;;PRIORITY LEVEL 5
139      000300      PR6=      300        ;;PRIORITY LEVEL 6
140      000340      PR7=      340        ;;PRIORITY LEVEL 7

```

;'SWITCH REGISTER' SWITCH DEFINITIONS

```

143      100000      SW15=     100000
144      040000      SW14=     40000
145      020000      SW13=     20000
146      010000      SW12=     10000
147      004000      SW11=     4000
148      002000      SW10=     2000
149      001000      SW09=     1000
150      000400      SW08=     400
151      000200      SW07=     200
152      000100      SW06=     100
153      000040      SW05=     40
154      000020      SW04=     20
155      000010      SW03=     10
156      000004      SW02=     4
157      000002      SW01=     2
158      000001      SW00=     1
159      .EQUIV      SW09,SW9
160      .EQUIV      SW08,SW8
161      .EQUIV      SW07,SW7
162      .EQUIV      SW06,SW6
163      .EQUIV      SW05,SW5
164      .EQUIV      SW04,SW4
165      .EQUIV      SW03,SW3
166      .EQUIV      SW02,SW2
167      .EQUIV      SW01,SW1
168      .EQUIV      SW00,SW0

```

```

169
170      ;*DATA BIT DEFINITIONS (BIT00 TO BIT15)
171      100000      BIT15= 100000
172      040000      BIT14= 40000
173      020000      BIT13= 20000
174      010000      BIT12= 10000
175      004000      BIT11= 4000
176      002000      BIT10= 2000
177      001000      BIT09= 1000
178      000400      BIT08= 400
179      000200      BIT07= 200
180      000100      BIT06= 100
181      000040      BIT05= 40
182      000020      BIT04= 20
183      000010      BIT03= 10
184      000004      BIT02= 4
185      000002      BIT01= 2
186      000001      BIT00= 1
187      .EQUIV BIT09,BIT9
188      .EQUIV BIT08,BIT8
189      .EQUIV BIT07,BIT7
190      .EQUIV BIT06,BIT6
191      .EQUIV BIT05,BIT5
192      .EQUIV BIT04,BIT4
193      .EQUIV BIT03,BIT3
194      .EQUIV BIT02,BIT2
195      .EQUIV BIT01,BIT1
196      .EQUIV BIT00,BIT0
197
198      ;*BASIC "CPU" TRAP VECTOR ADDRESSES
199      000004      ERRVEC= 4      ;;TIME OUT AND OTHER ERRORS
200      000010      RESVEC= 10     ;;RESERVED AND ILLEGAL INSTRUCTIONS
201      000014      TBITVEC=14    ;;'T' BIT
202      000014      TRIVEC= 14    ;;TRACE TRAP
203      000014      BPTVEC= 14    ;;BREAKPOINT TRAP (BPT)
204      000020      IOTVEC= 20    ;;INPUT/OUTPUT TRAP (IOT) **SCOPE**
205      000024      PWRVEC= 24    ;;POWER FAIL
206      000030      EMTVEC= 30    ;;EMULATOR TRAP (EMT) **ERROR**
207      000034      TRAPVEC=34   ;;'TRAP' TRAP
208      000060      TKVEC= 60     ;;TTY KEYBOARD VECTOR
209      000064      TPVEC= 64     ;;TTY PRINTER VECTOR
210      000100      LKVEC= 100    ;;LINE CLOCK (KW11-L) VECTOR
211      000114      CACHVEC=114   ;;CACHE ERROR INTERRUPT VECTOR
212      000240      PIRQVEC=240   ;;PROGRAM INTERRUPT REQUEST VECTOR
213      000250      MMVEC= 250    ;;MEMORY MANAGEMENT VECTOR
214      .SBTTL CACHE REGISTER DEFINITIONS
215
216
217      177740      LOADRS = 177740 ;;LOWER 16 BITS OF ADDRESS THAT CAUSED ERROR
218      177742      HIADRS = 177742 ;;UPPER SIX BITS OF ADDRESS THAT CAUSED ERROR
219      177744      MEMERR = 177744 ;;CACHE ERROR REGISTER
220      177746      CONTRL = 177746 ;;MEMORY CONTROL REGISTER
221      177750      MAINT = 177750 ;;MEMORY MAINTENANCE REGISTER
222      177752      HITMIS = 177752 ;;HIT MISS REGISTER '1' IMPLIES HIT IN CACHE
223
224      .SBTTL CPU REGISTER DEFINITIONS
  
```

225  
226  
227 177760 SIZELO = 177760 ;;MEMORY SIZE REGISTER NUMBER TO PUT INTO A PAR  
228 ;;TO GET TO THE LAST 32 WORDS OF MEMORY  
229 177762 SIZEHI = 177762 ;;HIGH SIZE REGISTER, RESERVED FOR FUTURE USE  
230 ;;CURRENTLY ALL ZERO  
231 177764 SYSTID = 177764 ;;SYSTEM ID REGISTER  
232 177766 CPUERR = 177766 ;;CPU ERROR REGISTER HOLDS CONDITION THAT CAUSED  
233 ;;THE TRAP TO ERRVEC (G00004)  
234  
235

.SBTTL MEMORY MANAGEMENT DEFINITIONS

;\*MEMORY MANAGEMENT STATUS REGISTER ADDRESSES

241  
242 177572 MMR0= 177572  
243 177574 MMR1= 177574  
244 177576 MMR2= 177576  
245 172516 MMR3= 172516  
246 .EQUIV MMR0,SR0  
247 .EQUIV MMR1,SR1  
248 .EQUIV MMR2,SR2  
249 .EQUIV MMR3,SR3

;\*USER 'I' PAGE DESCRIPTOR REGISTERS

251  
252  
253 177600 UIPDR0= 177600  
254 177602 UIPDR1= 177602  
255 177604 UIPDR2= 177604  
256 177606 UIPDR3= 177606  
257 177610 UIPDR4= 177610  
258 177612 UIPDR5= 177612  
259 177614 UIPDR6= 177614  
260 177616 UIPDR7= 177616

;\*USER 'D' PAGE DESCRIPTOR REGISTERS

261  
262  
263  
264 177620 UDPDR0= 177620  
265 177622 UDPLR1= 177622  
266 177624 UDPDR2= 177624  
267 177626 UDPDR3= 177626  
268 177630 UDPDR4= 177630  
269 177632 UDPDR5= 177632  
270 177634 UDPDR6= 177634  
271 177636 UDPDR7= 177636

;\*USER 'I' PAGE ADDRESS REGISTERS

272  
273  
274  
275 177640 UIPAR0= 177640  
276 177642 UIPAR1= 177642  
277 177644 UIPAR2= 177644  
278 177646 UIPAR3= 177646  
279 177650 UIPAR4= 177650  
280 177652 UIPAR5= 177652

```
281      177654      UIPAR6= 177654
282      177656      UIPAR7= 177656
283
284      ;*USER 'D' PAGE ADDRESS REGISTERS
285
286      177660      UDPAR0= 177660
287      177662      UDPAR1= 177662
288      177664      UDPAR2= 177664
289      177666      UDPAR3= 177666
290      177670      UDPAR4= 177670
291      177672      UDPAR5= 177672
292      177674      UDPAR6= 177674
293      177676      UDPAR7= 177676
294
295      ;*SUPERVISOR 'I' PAGE DESCRIPTOR REGISTERS
296
297      172200      SIPDR0= 172200
298      172202      SIPDR1= 172202
299      172204      SIPDR2= 172204
300      172206      SIPDR3= 172206
301      172210      SIPDR4= 172210
302      172212      SIPDR5= 172212
303      172214      SIPDR6= 172214
304      172216      SIPDR7= 172216
305
306      ;*SUPERVISOR 'D' PAGE DESCRIPTOR REGISTERS
307
308      172220      SDPDR0= 172220
309      172222      SDPDR1= 172222
310      172224      SDPDR2= 172224
311      172226      SDPDR3= 172226
312      172230      SDPDR4= 172230
313      172232      SDPDR5= 172232
314      172234      SDPDR6= 172234
315      172236      SDPDR7= 172236
316
317      ;*SUPERVISOR 'I' PAGE ADDRESS REGISTERS
318
319      172240      SIPAR0= 172240
320      172242      SIPAR1= 172242
321      172244      SIPAR2= 172244
322      172246      SIPAR3= 172246
323      172250      SIPAR4= 172250
324      172252      SIPAR5= 172252
325      172254      SIPAR6= 172254
326      172256      SIPAR7= 172256
327
328      ;*SUPERVISOR 'D' PAGE ADDRESS REGISTERS
329
330      172260      SDPAR0= 172260
331      172262      SDPAR1= 172262
332      172264      SDPAR2= 172264
333      172266      SDPAR3= 172266
334      172270      SDPAR4= 172270
335      172272      SDPAR5= 172272
336      172274      SDPAR6= 172274
```

```
337      172276      SDPAR7= 172276
338
339      ;*KERNEL 'I' PAGE DESCRIPTOR REGISTERS
340
341      172300      KIPDR0= 172300
342      172302      KIPDR1= 172302
343      172304      KIPDR2= 172304
344      172306      KIPDR3= 172306
345      172310      KIPDR4= 172310
346      172312      KIPDR5= 172312
347      172314      KIPDR6= 172314
348      172316      KIPDR7= 172316
349
350      ;*KERNEL 'D' PAGE DESCRIPTOR REGISTERS
351
352      172320      KDPDR0= 172320
353      172322      KDPDR1= 172322
354      172324      KDPDR2= 172324
355      172326      KDPDR3= 172326
356      172330      KDPDR4= 172330
357      172332      KDPDR5= 172332
358      172334      KDPDR6= 172334
359      172336      KDPDR7= 172336
360
361      ;*KERNEL 'I' PAGE ADDRESS REGISTERS
362
363      172340      KIPAR0= 172340
364      172342      KIPAR1= 172342
365      172344      KIPAR2= 172344
366      172346      KIPAR3= 172346
367      172350      KIPAR4= 172350
368      172352      KIPAR5= 172352
369      172354      KIPAR6= 172354
370      172356      KIPAR7= 172356
371
372      ;*KERNEL 'D' PAGE ADDRESS REGISTERS
373
374      172360      KDPAR0= 172360
375      172362      KDPAR1= 172362
376      172364      KDPAR2= 172364
377      172366      KDPAR3= 172366
378      172370      KDPAR4= 172370
379      172372      KDPAR5= 172372
380      172374      KDPAR6= 172374
381      172376      KDPAR7= 172376
382
383
384
385      .SBTTL UNIBUS MAP REGISTER DEFINITIONS
386
387
388      ;*THE LOWER 16 BITS OF THE MAP REGISTERS ARE LABELED 'MAPLXX'
389      ;*THE UPPER 6 BITS OF THE MAP REGISTERS ARE LABELED 'MAPHXX'
390
391
392      170200      MAPL00 - 170200
```



393	170202	MAPH00 = 170202
394	170204	MAPL01 = 170204
395	170206	MAPH01 = 170206
396	170210	MAPL02 = 170210
397	170212	MAPH02 = 170212
398	170214	MAPL03 = 170214
399	170216	MAPH03 = 170216
400	170220	MAPL04 = 170220
401	170222	MAPH04 = 170222
402	170224	MAPL05 = 170224
403	170226	MAPH05 = 170226
404	170230	MAPL06 = 170230
405	170232	MAPH06 = 170232
406	170234	MAPL07 = 170234
407	170236	MAPH07 = 170236
408	170240	MAPL10 = 170240
409	170242	MAPH10 = 170242
410	170244	MAPL11 = 170244
411	170246	MAPH11 = 170246
412	170250	MAPL12 = 170250
413	170252	MAPH12 = 170252
414	170254	MAPL13 = 170254
415	170256	MAPH13 = 170256
416	170260	MAPL14 = 170260
417	170262	MAPH14 = 170262
418	170264	MAPL15 = 170264
419	170266	MAPH15 = 170266
420	170270	MAPL16 = 170270
421	170272	MAPH16 = 170272
422	170274	MAPL17 = 170274
423	170276	MAPH17 = 170276
424	170300	MAPL20 = 170300
425	170302	MAPH20 = 170302
426	170304	MAPL21 = 170304
427	170306	MAPH21 = 170306
428	170310	MAPL22 = 170310
429	170312	MAPH22 = 170312
430	170314	MAPL23 = 170314
431	170316	MAPH23 = 170316
432	170320	MAPL24 = 170320
433	170320	MAPH24 = 170320
434	170324	MAPL25 = 170324
435	170326	MAPH25 = 170326
436	170330	MAPL26 = 170330
437	170332	MAPH26 = 170332
438	170334	MAPL27 = 170334
439	170336	MAPH27 = 170336
440	170340	MAPL30 = 170340
441	170342	MAPH30 = 170342
442	170344	MAPL31 = 170344
443	170346	MAPH31 = 170346
444	170350	MAPL32 = 170350
445	170352	MAPH32 = 170352
446	170354	MAPL33 = 170354
447	170356	MAPH33 = 170356
448	170360	MAPL34 = 170360

```

449      170362      MAPH34 = 170362
450      170364      MAPL35 = 170364
451      170366      MAPH35 = 170366
452      170370      MAPL36 = 170370
453      170372      MAPH36 = 170372
454      170374      MAPL37 = 170374
455      170376      MAPH37 = 170376
456      .EQUIV      MAPL00,MAPL0
457      .EQUIV      MAPH00,MAPH0
458      .EQUIV      MAPL01,MAPL1
459      .EQUIV      MAPH01,MAPH1
460      .EQUIV      MAPL02,MAPL2
461      .EQUIV      MAPH02,MAPH2
462      .EQUIV      MAPL03,MAPL3
463      .EQUIV      MAPH03,MAPH3
464      .EQUIV      MAPL04,MAPL4
465      .EQUIV      MAPH04,MAPH4
466      .EQUIV      MAPL05,MAPL5
467      .EQUIV      MAPH05,MAPH5
468      .EQUIV      MAPL06,MAPL6
469      .EQUIV      MAPH06,MAPH6
470      .EQUIV      MAPL07,MAPL7
471      .EQUIV      MAPH07,MAPH7
472      170016      UBCR2=170016
  
```

.SBTTL IIST REGISTER DEFINITIONS

:: IIST INTERNAL REGISTERS

```

481      000000      PGTE = 0      ;;PROGRAM-GENERATED TRANSMISSION ENABLE
482      000001      PGCS = 1      ;;PROGRAM-GENERATED CONTROL STATUS
483      000002      STTE = 2      ;;SANITY-TIMER TRANSMISSION ENABLE
484      000003      STCS = 3      ;;SANITY-TIMER CONTROL STATUS
485      000004      IMSK = 4      ;;INPUT MASK
486      000005      PGF = 5      ;;PROGRAM GENERATED FLAGS
487      000006      STF = 6      ;;SANITY-TIMER FLAGS
488      000007      DCF = 7      ;;DCLO/DISCONNECT FLAGS
489      000010      EXC = 10     ;;EXCEPTIONS
490      000015      MTC = 15     ;;MAINTAINANCE CONTROL
  
```

::IIST INTERRUPT VECTOR

.SBTTL CONSOLE SWITCH SETTINGS

```

496      ;; WHEN THESE SWITCHES ARE ENABLED, IT SPECIFIES TO THE MASTER
497      ;; THAT THE CPU WITH THE IIST SELF ID CORRESPONDING TO THE
498      ;;EQUIVILENT BIT POSITION IS EXPECTED TO PARTICIPATE IN THIS TEST
  
```

```

499      000001      CP0=BIT0      ;CPU0 MASK LOCATION
500      000002      CP1=BIT1      ;CPU1 MASK LOCATION
501      000004      CP2=BIT2      ;CPU2 MASK LOCATION
502      000010      CP3=BIT3      ;CPU3 MASK LOCATION
503
504
  
```

```
505          ;; THE FOLLOWING SWITCHES CONTROL THE EXECUTION STREAM OF THE
506          ;; TEST.
507
508          000100          MPSW= BIT6          ;ENABLE FOR MULTIPROCESSOR CONFIGURATIONS
509          000040          UBESW= BIT5         ;ENABLE IF UNIBUS EXERCISER IS TO BE USED
510          001000          LOE= BIT9           ;ENABLE FOR LOOPING ON ERRORS
511          040000          LOT= BIT14          ;ENABLE FOR LOOPING ON TEST
512          100000          HOE= BIT15          ;HALT ON ERROR
```

```
513          .SBTTL RJP04 DEVICE REGISTERS
514          176700 RPCS1=176700      ;;CONTROL AND STATUS 1
515          176702 RPWC =176702      ;;WORD COUNT REGISTER
516          176704 RPBA =176704      ;;UNIBUS ADDRESS
517          176706 RPDA =176706      ;;DESIRED SECTOR/TRACK ADDRESS
518          176710 RPCS2=176710      ;;CONTROL AND STATUS 2
519          176712 RPDS =176712      ;;DRIVE STATUS
520          176714 RPER1=176714      ;;ERROR REGISTER 1
521          176716 RPAS =176716      ;;ATTENTION SUMMARY
522          176720 RPLA =176720      ;;LOOK-AHEAD REGISTER
523          176722 RPDB =176722      ;;DATA BUFFER REGISTER
524          176724 RPMR =176724      ;;MAINTENANCE REGISTER
525          176726 RPDT =176726      ;;DRIVE TYPE
526          176730 RPSN =176730      ;;SERIAL NUMBER REGISTER
527          176732 RPOF =176732      ;;OFFSET REGISTER
528          176734 RPDC =176734      ;;DESIRED CYLINDER REGISTER
529          176736 RPCC =176736      ;;CURRENT CYLINDER REGISTER
530          176740 RPER2=176740      ;;ERROR REGISTER 2
531          176742 RPER3=176742      ;;ERROR REGISTER 3
532          176744 RPEC1=176744      ;;ECC POSITION REGISTER
533          176746 RPEC2=176746      ;;ECC PATTERN REGISTER
```

```
534          .SBTTL POWER FAIL FUNCTION TABLE BIT DIFINITIONS
535
536          010000          NCX=BIT12          ;;DON'T SAVE MM REGISTERS
537          004000          TI =BIT11          ;;TIME THE POWER FAIL
538          002000          NS =BIT10          ;;DON'T PERFORM A REGISTER SAVE
539          001000          SID=BIT9           ;;SEND ERROR ON ILLEGAL DOWN
540          000400          SIU=BIT8           ;;SEND ERROR ON ILLEGAL UP
541          000200          SED=BIT7           ;;SEND ERROR ON DOWN
542          000100          SEU=BIT6           ;;SED ERROR ON UP
543          000040          SSD=BIT5           ;;SEND SIGNAL ON DOWN
544          000020          SSU=BIT4           ;;SEND SIGNAL ON UP.
545          .SBTTL TRAP CATCHER
546
547          000000          .=0
548          ;*ALL UNUSED LOCATIONS FROM 4 - 776 CONTAIN A ".+2,HALT"
549          ;*SEQUENCE TO CATCH ILLEGAL TRAPS AND INTERRUPTS
550          ;*LOCATION 0 CONTAINS 0 TO CATCH IMPROPERLY LOADED VECTORS
551          000174          .=174
552 000174 000000          DISPREG: .WORD 0          ;;SOFTWARE DISPLAY REGISTER
553 000176 000000          SWREG:  .WORD 0          ;;SOFTWARE SWITCH REGISTER
554          .SBTTL ACT11 HOOKS
555
556          ;:*****
557          ;HOOKS REQUIRED BY ACT11
558          000200          $SVPC=.          ;SAVE PC
559          000046          .=46
560 000046 035644          $ENDAD          ;;1)SET LOC.46 TO ADDRESS OF $ENDAD IN .$EOP
561          000052          .=52
562 000052 000000          .WORD 0          ;;2)SET LOC.52 TO ZERO
563          000200          . $SVPC          ;; RESTORE PC
```

```
564 .SBTTL LOAD START AND RESTART VECTORS
565 .=200
566 000200 000137 020064 JMP STRT ;LOAD 200 WITH A JUMP TO START OF TEST
567 000220 000220 .=220
568 000220 004737 020000 JSR PC, RESTRT ;LOAD 220 WITH A JUMP TO THE RESTART CODE
569 000224 000137 020064 JMP STRT
570
```

571  
572  
573  
574  
575  
576 000230  
577 000024  
578 000024 000200  
579 000044 000044  
580 000044 000230  
581 000230  
582  
583  
584  
585  
586 000230  
587 000230 000000  
588 000232 014336  
589 000234 000000  
590 000236 000000  
591 000240 000000  
592 000242 000052

.SBTTL APT PARAMETER BLOCK  
\*\*\*\*\*  
:SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT  
\*\*\*\*\*  
.\$X=. ;;SAVE CURRENT LOCATION  
.=24 ;;SET POWER FAIL TO POINT TO START OF PROGRAM  
200 ;;FOR APT START UP  
.=44 ;;POINT TO APT INDIRECT ADDRESS PNTR.  
\$APTHDR ;;POINT TO APT HEADER BLOCK  
.=.\$X ;;RESET LOCATION COUNTER  
\*\*\*\*\*  
:SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC  
:INTERFACE SPEC.  
\$APTHD:  
\$HIBTS: .WORD 0 ;;TWO HIGH BITS OF 18 BIT MAILBOX ADDR.  
\$MBADR: .WORD \$MAIL ;;ADDRESS OF APT MAILBOX (BITS 0-15)  
\$STMT: .WORD ;;RUN TIM OF LONGEST TEST  
\$PASTM: .WORD ;;RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)  
\$UNITM: .WORD ;;ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT  
.WORD \$ETEND-\$MAIL/2 ;;LENGTH MAILBOX-ETABLE(WORDS)

```
593      .SBTTL  COMMON TAGS
594
595      ;*****
596      ;*THIS TABLE CONTAINS VARIOUS COMMON STORAGE LOCATIONS
597      ;*USED IN THE PROGRAM.
598
599      014000      .=14000
600 014000 000000 $CMTAG:      .WORD 0      ;;START OF COMMON TAGS
601 014000 000000 $TSTNM:      .BYTE 0      ;;CONTAINS THE TEST NUMBER
602 014002 000      .BYTE 0
603 014003 000      .BYTE 0
604 014004 000      .BYTE 0
605 014005 000      .BYTE 0
606 014006 000      $ERFLG:      .BYTE 0      ;;CONTAINS ERROR FLAG
607 014007 000      .BYTE 0
608 014010 000      .BYTE 0
609 014011 000      .BYTE 0
610 014012 000000 $ICNT:      .WORD 0      ;;CONTAINS SUBTEST ITERATION COUNT
611 014014 000000      .WORD 0
612 014016 000000      .WORD 0
613 014020 000000      .WORD 0
614 014022 000000 $LPADR:      .WORD 0      ;;CONTAINS SCOPE LOOP ADDRESS
615 014024 000000      .WORD 0
616 014026 000000      .WORD 0
617 014030 000000      .WORD 0
618 014032 000000 $LPERR:      .WORD 0      ;;CONTAINS SCOPE RETURN FOR ERRORS
619 014034 000000      .WORD 0
620 014036 000000      .WORD 0
621 014040 000000      .WORD 0
622 014042 000000 $ERTTL:      .WORD 0      ;;CONTAINS TOTAL ERRORS DETECTED
623 014044 000000      .WORD 0
624 014046 000000      .WORD 0
625 014050 000000      .WORD 0
626 014052 000000      .WORD 0
627 014054 000      $ITEMB:      .BYTE 0      ;;CONTAINS ITEM CONTROL BYTE
628 014055 000      .BYTE 0
629 014056 000      .BYTE 0
630 014057 000      .BYTE 0
631 014060 001      $ERMAX:      .BYTE 1      ;;CONTAINS MAX. ERRORS PER TEST
632 014061 001      .BYTE 1
633 014062 001      .BYTE 1
634 014063 001      .BYTE 1
635 014064 000000 $ERRPC:      .WORD 0      ;;CONTAINS PC OF LAST ERROR INSTRUCTION
636 014066 000000      .WORD 0
637 014070 000000      .WORD 0
638 014072 000000      .WORD 0
639 014074 000000 $ERRSP:      .WORD 0      ;;CONTAINS SP OF CPU IN ERROR
640 014076 000000      .WORD 0
641 014100 000000      .WORD 0
642 014102 000000      .WORD 0
643 014104 000000 $GDADR:      .WORD 0      ;;CONTAINS ADDRESS OF 'GOOD' DATA
644 014106 000000      .WORD 0
645 014110 000000      .WORD 0
646 014112 000000      .WORD 0
647 014114 000000 $BDADR:      .WORD 0      ;;CONTAINS ADDRESS OF 'BAD' DATA
648 014116 000000      .WORD 0
```



```

649 014120 000000          .WORD 0
650 014122 000000          .WORD 0
651 014124 000000          $GDDAT: .WORD 0          ;;CONTAINS 'GOOD' DATA
652 014126 000000          .WORD 0
653 014130 000000          .WORD 0
654 014132 000000          .WORD 0
655 014134 000          $EOPSG: .BYTE 0          ;;THIS TABLE HOLDS THE END OF PASS
656 014135 000          .BYTE 0
657 014136 000          .BYTE 0
658 014137 000          .BYTE 0
659
660 014140 000000          $BDDAT: .WORD 0          ;;CONTAINS 'BAD' DATA
661 014142 000000          .WORD 0
662 014144 000000          .WORD 0
663 014146 000000          .WORD 0
664 014150 000000          .WORD 0          ;;RESERVED--NOT TO BE USED
665 014152 000000          .WORD 0
666 014154 000          $AUTOB: .BYTE 0          ;;AUTOMATIC MODE INDICATOR
667 014155 000          $INTAG: .BYTE 0          ;;INTERRUPT MODE INDICATOR
668 014156 000000          .WORD 0
669 014160 177570          SWR: .WORD DSWR          ;;ADDRESS OF SWITCH REGISTER
670 014162 177570          .WORD DSWR
671 014164 177570          .WORD DSWR
672 014166 177570          .WORD DSWR
673 014170 177570          DISPLAY: .WORD DDISP          ;;ADDRESS OF DISPLAY REGISTER
674 014172 177570          .WORD DDISP
675 014174 177570          .WORD DDISP
676 014176 177570          .WORD DDISP
677 014200 013776          $$STP: .WORD STACK          ;;STACK INITIALIZATION FOR CPU0
678 014202 011776          .WORD STACK-2000          ;;CPU1
679 014204 007776          .WORD STACK-4000          ;;CPU2
680 014206 003776          .WORD STACK-10000          ;;CPU3
681 014210 177560          $TKS: 177560          ;;TTY KBD STATUS
682 014212 177562          $TKB: 177562          ;;TTY KBD BUFFER
683 014214 177564          $TPS: 177564          ;;TTY PRINTER STATUS REG. ADDRESS
684 014216 177566          $TPB: 177566          ;;TTY PRINTER BUFFER REG. ADDRESS
685 014220 000          $NULL: .BYTE 0          ;;CONTAINS NULL CHARACTER FOR FILLS
686 014221 002          $FILLS: .BYTE 2          ;;CONTAINS # OF FILLER CHARACTERS REQUIRED
687 014222 012          $FILLC: .BYTE 12          ;;INSERT FILL CHARS. AFTER A 'LINE FEED'
688 014223 000          $TPFLG: .BYTE 0          ;;'TERMINAL AVAILABLE' FLAG (BIT<07>=0-YES)
689 014224 000000          $ERGBL: .WORD 0
690 014226 177777          $CPUID: .WORD -1          ;;THIS TABLE HOLDS THE PHYSICAL ID OF
691 014230 177777          .WORD -1          ;;THE PARTICIPATING PROCESSORS ARRANGED
692 014232 177777          .WORD -1          ;;IN LOGICAL ORDER.
693 014234 177777          .WORD -1
694 014236 000000          $REGAD: .WORD 0          ;;CONTAINS THE ADDRESS FROM
695          .WORD 0          ;;WHICH ($REG0) WAS OBTAINED
696 014240 000000 000000 000000 $REG0: .WORD 0,0,0,0          ;;CONTAINS (($REGAD)+0+6)
697 014246 000000          .WORD 0
698 014250 000000 000000 000000 $REG1: .WORD 0,0,0,0          ;;CONTAINS (($REGAD)+2+6)
699 014256 000000          .WORD 0
700 014260 000000 000000 000000 $REG2: .WORD 0,0,0,0          ;;CONTAINS (($REGAD)+4+6)
701 014266 000000          .WORD 0
702 014270 000000 000000 000000 $REG3: .WORD 0,0,0,0          ;;CONTAINS (($REGAD)+6+6)
703 014276 000000          .WORD 0
704 014300 000000 000000 000000 $REG4: .WORD 0,0,0,0          ;;CONTAINS (($REGAD)+10+6)
    
```

```

705 014306 000000
706 014310 000000 $TMPO: .WORD 0 ;;USER DEFINED
707 014312 000000 $TMP1: .WORD 0 ;;USER DEFINED
708 014314 000000 $TMP2: .WORD 0 ;;USER DEFINED
709 014316 000000 $TMP3: .WORD 0 ;;USER DEFINED
710 014320 000000 $TMP4: .WORD 0 ;;USER DEFINED
711 014322 000000 $ESCAPE:0 ;;ESCAPE ON ERROR ADDRESS
712 014324 000000 .WORD 0
713 014326 000000 .WORD 0
714 014330 000000 .WORD 0
715 014332 077 $QUES: .ASCII /?/ ;;QUESTION MARK
716 014333 015 $CRLF: .ASCII <15> ;;CARRIAGE RETURN
717 014334 000012 $LF: .ASCIIZ <12> ;;LINE FEED
718 *****
719 .SBTTL APT MAILBOX-ETABLE
720 *****
721 .EVEN
722 $MAIL: ;;APT MAILBOX
723 014336 $MSGTY: .WORD AMSGTY ;;MESSAGE TYPE CODE
724 014336 000000 $FATAL: .WORD AFATAL ;;FATAL ERROR NUMBER
725 014340 000000 $TESTN: .WORD ATESTN ;;TEST NUMBER
726 014342 000000 $PASS: .WORD APASS ;;PASS COUNT
727 014344 000000 $DEVCT: .WORD ADEVCT ;;DEVICE COUNT
728 014346 000000 $UNIT: .WORD AUNIT ;;I/O UNIT NUMBER
729 014350 000000 $MSGAD: .WORD AMSGAD ;;MESSAGE ADDRESS
730 014352 000000 $MSGLG: .WORD AMSGLG ;;MESSAGE LENGTH
731 014354 000000 $ETABLE: ;;APT ENVIRONMENT TABLE
732 014356 $ENV: .BYTE AENV ;;ENVIRONMENT BYTE
733 014356 000 $ENVM: .BYTE AENVM ;;ENVIRONMENT MODE BITS
734 014357 000 $SWREG: .WORD ASWREG ;;APT SWITCH REGISTER
735 014360 000000 $USWR: .WORD AUSWR ;;USER SWITCHES
736 014362 000000 $CPUOP: .WORD ACPUOP ;;CPU TYPE,OPTIONS
737 014364 000000
738 *
739 *
740 * 11/04=01,11/05=02,11/20=03,11/40=04,11/45=05
741 * 11/70=06,PDQ=07,Q=10
742 *
743 * BIT 10=REAL TIME CLOCK
744 * BIT 9=FLOATING POINT PROCESSOR
745 * BIT 8=MEMORY MANAGEMENT
746 014366 000 $MAMS1: .BYTE AMAMS1 ;;HIGH ADDRESS,M.S. BYTE
747 014367 000 $MTYP1: .BYTE AMTYP1 ;;MEM. TYPE,BLK#1
748 * MEM. TYPE BYTE -- (HIGH BYTE)
749 * 900 NSEC CORE=001
750 * 300 NSEC BIPOLAR=002
751 * 500 NSEC MOS=003
752 014370 000000 $MADR1: .WORD AMADR1 ;;HIGH ADDRESS,BLK#1
753 * MEM.LAST ADDR.=3 BYTES,THIS WORD AND LOW OF 'TYPE' ABOVE
754 014372 000 $MAMS2: .BYTE AMAMS2 ;;HIGH ADDRESS,M.S. BYTE
755 014373 000 $MTYP2: .BYTE AMTYP2 ;;MEM. TYPE,BLK#2
756 014374 000000 $MADR2: .WORD AMADR2 ;;MEM.LAST ADDRESS,BLK#2
757 014376 000 $MAMS3: .BYTE AMAMS3 ;;HIGH ADDRESS,M.S.BYTE
758 014377 000 $MTYP3: .BYTE AMTYP3 ;;MEM. TYPE,BLK#3
759 014400 000000 $MADR3: .WORD AMADR3 ;;MEM.LAST ADDRESS,BLK#3
760 014402 000 $MAMS4: .BYTE AMAMS4 ;;HIGH ADDRESS,M.S.BYTE
761 014403 000 $MTYP4: .BYTE AMTYP4 ;;MEM. TYPE,BLK#4
762 014404 000000 $MADR4: .WORD AMADR4 ;;MEM.LAST ADDRESS,BLK#4
    
```

```

761 014406 000000 $VECT1: .WORD AVECT1 ;; INTERRUPT VECTOR#1,BUS PRIORITY#1
762 014410 000000 $VECT2: .WORD AVECT2 ;; INTERRUPT VECTOR#2BUS PRIORITY#2
763 014412 000000 $BASE: .WORD ABASE ;; BASE ADDRESS OF EQUIPMENT UNDER TEST
764 014414 000000 $DEV: .WORD ADEV ;; DEVICE MAP
765 014416 000000 $CDW1: .WORD ACDW1 ;; CONTROLLER DESCRIPTION WORD#1
766 014420 000000 $CDW2: .WORD ACDW2 ;; CONTROLLER DESCRIPTION WORD#2
767 014422 000000 $DDW0: .WORD ADDW0 ;; DEVICE DESCRIPTOR WORD#0
768 014424 000000 $DDW1: .WORD ADDW1 ;; DEVICE DESCRIPTOR WORD#1
769 014426 000000 $DDW2: .WORD ADDW2 ;; DEVICE DESCRIPTOR WORD#2
770 014430 000000 $DDW3: .WORD ADDW3 ;; DEVICE DESCRIPTOR WORD#3
771 014432 000000 $DDW4: .WORD ADDW4 ;; DEVICE DESCRIPTOR WORD#4
772 014434 000000 $DDW5: .WORD ADDW5 ;; DEVICE DESCRIPTOR WORD#5
773 014436 000000 $DDW6: .WORD ADDW6 ;; DEVICE DESCRIPTOR WORD#6
774 014440 000000 $DDW7: .WORD ADDW7 ;; DEVICE DESCRIPTOR WORD#7
775 014442 000000 $DDW8: .WORD ADDW8 ;; DEVICE DESCRIPTOR WORD#8
776 014444 000000 $DDW9: .WORD ADDW9 ;; DEVICE DESCRIPTOR WORD#9
777 014446 000000 $DDW10: .WORD ADDW10 ;; DEVICE DESCRIPTOR WORD#10
778 014450 000000 $DDW11: .WORD ADDW11 ;; DEVICE DESCRIPTOR WORD#11
779 014452 000000 $DDW12: .WORD ADDW12 ;; DEVICE DESCRIPTOR WORD#12
780 014454 000000 $DDW13: .WORD ADDW13 ;; DEVICE DESCRIPTOR WORD#13
781 014456 000000 $DDW14: .WORD ADDW14 ;; DEVICE DESCRIPTOR WORD#14
782 014460 000000 $DDW15: .WORD ADDW15 ;; DEVICE DESCRIPTOR WORD#15

```

```

783
784
785 014462 $ETEND:
786
787 014462 000000 000000 000000 STOP: 0,0,0,0,0,0,0,0,0 ;; MEM BOX UPPER BOUND ADDRESS TABLE
788 014470 000000 000000 000000
789 014476 000000 000000

```

```

790 014502 000000 000000 000000 START: 0,0,0,0,0,0,0,0,0 ;; MEM BOX STARTING ADDRESS TABLE
791 014510 000000 000000 000000
792 014516 000000 000000

```

```

793 014522 000000 PWRFL: 0 ;; 0 DON'T EXPECT CPU POWER FAIL,=1 EXPECT IT
794 014524 000000 YYY: 0 ;; ERROR ROUTINE WORK LOC
795 014526 000000 BOOT: 0 ;; =0 DON'T EXPECT CPU BOOT, =1 EXPECT IT
796 014530 000000 PATCHK: 0 ;; -0 WRITE AND CHECK MEM PATTERN,=1 CHECK ONLY
797 014532 000000 HICORE: 0 ;; =1 TURN ON MM ON POWER-UP
798 014534 000000 RELOUP: 0 ;; =0 DON'T RELOCATE,=1 RELOCATE
799 014536 000000 RELODN: 0 ;; =0 DON'T RELOCATE,=1 RELOCATE
800 014540 000000 EXIT: 0 ;; =0 DON'T EXIT, =1 EXIT TEST
801 014542 000000 ENTR22: 0 ;; CONTROL ENTRY INTO TEST 22
802 014544 000000 ENTR23: 0 ;; CONTROL ENTRY INTO TEST 23
803 014546 000000 ENTR24: 0 ;; CONTROL ENTRY INTO TEST 24
804 014550 000000 HIBOX: 0 ;; RELOCATE TO THIS MEM BOX
805 014552 000000 000000 000000 SAVRG: 0,0,0,0 ;; A PLACE TO SAVE A REGISTER
806 014560 000000
807 014562 000000 000000 000000 ROUTE: 0,0,0,0 ;; TYPE TRAP ROUTE TABLE
808 014570 000000
809

```

```

810 014572 000000 000000 000000 SAV6: 0,0,0,0 ;; SOME PLACE TO PUT THE SP
811 014600 000000
812 014602 000000 000000 000000 FLAG: 0,0,0,0 ;; INSTRUCTION DOWN FLAG
813 014610 000000
814 014612 000000 000000 000000 PFFT: .WORD 0,0,0,0 ;; POWER FAIL FUNCTION TABLE
815 014620 000000
816 014622 000000 000000 000000 PFDT: .WORD 0,0,0,0 ;; POWER FAIL DURATION TABLE

```



873 017044 000400 000400 000400 YELLIM: .WORD 400,400,400,400  
874 017052 000400  
875 017054 177777  
876 017056 177777  
877 017060 006405  
878

;YELLOW ZONE BOUNDARY

PUT: -1 ;CPU UNDER TEST  
TYPLCK: -1 ;ERROR/TYPE SEMAPHORE  
FACTOR: 20000./6 ;POWER DWN FACTER  
.EVEN

```
879      .SBTTL  ERROR POINTER TABLE
880
881      ;*THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.
882      ;*THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN
883      ;*LOCATION $ITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.
884      ;*NOTE1:      IF $ITEMB IS 0 THE ONLY PERTINENT DATA IS ($ERRPC).
885      ;*NOTE2:      EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:
886
887      ;*      EM      ;;POINTS TO THE ERROR MESSAGE
888      ;*      DH      ;;POINTS TO THE DATA HEADER
889      ;*      DT      ;;POINTS TO THE DATA
890      ;*      DF      ;;POINTS TO THE DATA FORMAT
891
892
893      $ERRTB:
894      ;;ITEM 1
895      EM1      :UNEXPECTED POWER FAILURE ON CPU
896      DH10     :TESTNO ERRORPC
897      DT10     :$STNM,$ERRPC
898      0
899
900      ;;ITEM 2
901      EM2      :UNEXPECTED POWER UP SEQUENCE ON CPU
902      0
903      0
904      0
905
906      ;;ITEM 3
907      EM3      :ILLEGAL POWER DOWN SEQUENCE
908      0
909      0
910      0
911
912      ;;ITEM 4
913      EM4      :ILLEGAL POWER UP SEQUENCE
914      0
915      0
916      0
917
918      ;;ITEM 5
919      EM5      :UNEXPECTED TRAP TO LOCATION 4
920      DH5      :PID ERRORPC CPUERR
921      DT5      :$REG0,$ERRPC,$REG1
922      0
923
924      ;;ITEM 6
925      EM6      :UNEXPECTED TRAP TO 10
926      DH5      :PID ERRORPC CPUERR
927      DT5      :
928      0
929
930      ;;ITEM 7
931      EM7      :UNEXPECTED TRAP TO 114
932      DH7      :PID ERRORPC CPUERR MEMERR
933      DT7      :$REG0,$ERRPC,$REG1,$REG2
934      0
```

935					
936			:::ITEM	10	
937	017152	045400	EM10		:ADDRESS ON THE STACK IS WRONG
938	017154	046346	DH10		:TESTNO ERRORPC
939	017156	046752	DT10		:\$TSTNM,ERRORPC
940	017160	000000	0		
941					
942			:::ITEM	11	
943	017162	045434	EM11		:OLD PS IS WRONG
944	017164	046371	DH11		:TESTNO ERRORPC PS
945	017166	046760	DT11		:\$TSTNM,\$ERRPC,\$REGO
946	017170	000000	0		
947					
948			:::ITEM	12	
949	017172	045456	EM12		:ODD ADDRESS TRAP FAILED
950	017174	046346	DH10		
951	017176	046752	DT10		
952	017200	000000	0		
953					
954			:::ITEM	13	
955	017202	045510	EM13		:MEMORY CORRUPTED ON POWER FAIL
956	017204	046423	DH12		
957	017206	046770	DT12		
958	017210	000000	0		
959					
960			:::ITEM	14	
961	017212	045551	EM14		:TIMEOUT TRAP FAILED
962	017214	046512	DH14		:TESTNO ERRORPC CPUERR
963	017216	046760	DT11		:\$TSTNM,\$ERRPC,\$REGO
964	017220	000000	0		
965					
966			:::ITEM	15	
967	017222	045577	EM15		:POWER FAIL RETURNED TO SOON
968	017224	046346	DH10		
969	017226	046752	DT10		
970	017230	000000	0		
971					
972			:::ITEM	16	
973	017232	045636	EM16		:NOT ENOUGH OR TOO MABY INSTRUCTIONS EXECUTED
974	017234	046346	DH10		
975	017236	046752	DT10		
976	017240	000000	0		
977					
978			:::ITEM	17	
979	017242	045715	EM17		:NO MEM. MANG. VIOLATION OR TRAP TO 4
980	017244	046512	DH14		
981	017246	046760	DT11		
982	017250	000000	0		
983					
984			:::ITEM	20	
985	017252	045764	EM20		:NO IIST INTERRUPT
986	017254	046545	DH20		:TESTNO ISTID ACR PGTE PGCS
987	017256	047000	DT20		:\$TSTNM,\$REGO,\$REG1,\$REG2,\$REG3
988	017260	000000	0		
989					
990			:::ITEM	21	

991	017262	046010	EM21		: INCORRECT BRK AND/OR DCF FLAGS
992	017264	046622	DH21		: TESTNO ISTID FOUND SHOULD BE
993	017266	047014	DT21		: \$TSTNM, \$REG0, \$REG1, \$REG2
994	017270	000000	0		
995					
996			:: ITEM	22	
997	017272	046051	EM22		: CPU DID NOT TRAP TO 24
998	017274	046672	DH22		: TESTNO ISTID ERRORPC
999	017276	047026	DT22		: \$TSTNM, \$REG0, \$ERRPC
1000	017300	000000	0		
1001					
1002			:: ITEM	23	
1003	017302	046112	EM23		: CHECKSUM ON MASSBUS TRANSFER IS WRONG
1004	017304	046672	DH22		
1005	017306	047026	DT22		
1006	017310	000000	0		
1007					
1008			:: ITEM	24	
1009	017312	046162	EM24		: NO POWER FAIL ON CPU
1010	017314	046346	DH10		: TESTNO ERRORPC
1011	017316	046752	DT10		: \$TSTNM, \$ERRPC
1012	017320	000000	0		
1013					
1014			:: ITEM	25	
1015	017322	046211	EM25		: UNEXPECTED CPU INTERRUPT
1016	017324	046346	DH10		: TESTNO ERRORPC
1017	017326	046752	DT10		: \$TSTNM, \$ERRPC
1018	017330	000000	0		
1019					
1020					



```
1021      020000      020000      . =20000      ;:LOAD CODE ABOVE THE FIRST 4K (WORDS)
1022      020000
1023      020000      012704      016766      RESTRT:      MOV      #CPUACT,      R4      ;RESET THE VARIABLES
1024      020004      012724      000001      1$:      MOV      #1, (R4)+
1025      020010      022704      017020      CMP      #S2L1, R4
1026      020014      103373      BHIS
1027      020016      012704      014462      MOV      #STOP, R4
1028      020022      005024      2$:      CLR      (R4)+
1029      020024      022704      016764      CMP      #EXTRA, R4
1030      020030      103374      BHIS
1031      020032      012737      177777      017030      MOV      #-1, FIRST
1032      020040      012737      000400      017032      MOV      #400, BMSK
1033      020046      012737      177777      017034      MOV      #-1, PUT
1034      020054      012737      177777      017056      MOV      #-1, TYPLCK
1035      020062      000207      RTS      PC      ;RETURN
1036
1037      020064      013706      014200      STRT:      MOV      $$STP, SP      ;INITIALIZE THE STACK
1038      020070      012704      014226      MOV      #SCPUID, R4      ;:GET ADDRESS OF CPUID TABLE
1039      020074      012703      000004      MOV      #4, R3      ;:INIT COUNTER
1040      020100      012724      177777      4$:      MOV      #-1, (R4)+      ;:INIT TABLE WITH -1'S
1041      020104      077303      SOB      R3, 4$
1042
1043      020106      012737      036164      000030      ;:INITIALIZE A FEW VECTORS
1044      020114      005037      000032      MOV      #ERROR, @EMTVEC      ;:EMT VECTOR FOR ERROR ROUTINE
1045      020120      012737      040252      000034      CLR      @EMTVEC+2      ;:LEVEL 0
1046      020126      005037      000036      MOV      #STRAP, @TRAPVEC      ;:TRAP VECTOR FOR TRAP CALLS
1047      020132      012737      040340      000024      CLR      @TRAPVEC+2      ;:LEVEL 0
1048      020140      005037      000026      MOV      #PWRDIS, @PWRVEC      ;:POINT TO POWER FAIL DISPATCH ROUTINE
1049      020144      012737      020330      000004      CLR      @PWRVEC+2      ;:LEVEL 0
1050      020152      012737      014722      014716      MOV      #25$, @ERRVEC      ;:SET UP CPU ERROR VECTOR INCASE SWR IS'NT THERE
1051      020160      012737      014722      014720      MOV      #TYPQUE+4, TYPQUE      ;:INITIALIZE REAR POINTER
1052      020166      005000      CLR      R0      ;:INITIALIZE FORWARD POINTER
1053      020170      005001      CLR      R1      ;:SET ID IN DISPLACEMENT REGS.
1054      020172      023737      000042      000046      CMP      @#42, @#46      ;UNDER ACT AUTO MODE?
1055      020200      001402      BEQ      40$      ;BRANCH IF YES
1056      020202      104401      040376      TYPE      .TM1      ;TYPE PROGRAM NAME
1057      020206      40$:
1058      020206      012737      177570      014160      MOV      #177570, SWR      ;:SET SWR
1059      020214      132737      000200      014357      BITB      #APTSIZE, $ENVM      ;:SIZE UNDER APT?
1060      020222      001403      BEQ      50$      ;:BRANCH IF NO
1061      020224      012737      014360      014160      MOV      #SSWREG, SWR      ;:USE APT SWITCH REG
1062      020232      032777      000100      173720      50$:      BIT      #MPSW, @SWR      ;:IS HARDWARE SWITCH REG. THERE? AND MP SET?
1063      020240      001021      BNE      20$      ;:SWR IS THERE AND MP IS SET.
1064      020242      001435      BEQ      30$      ;:SWR IS THERE BUT MP IS NOT SET.
1065      020244      012737      040356      000004      MOV      #ERRDIS, @ERRVEC      ;:RESET CPU ERROR VECTOR
1066      020252      012760      040362      014702      MOV      #CPUER, ERRTAB(R0)      ;:FLAG ALL UNEXPECTED TRAPS TO 4
1067      020260      012737      014360      014160      MOV      #SSWREG, SWR      ;:SETUP FOR SOFTWARE SWITCH REG
1068      020266      012737      000174      014170      MOV      #DISPREG, DISPLAY
1069      020274      032777      000100      173656      BIT      #MPSW, @SWR      ;:IS MP SWITCH SET IN SOFTWARE SWITCH REG?
1070      020302      001415      BEQ      30$      ;:NOPE.
1071      020304      012737      040356      000004      20$:      MOV      #ERRDIS, @ERRVEC      ;:RESET ERROR VECTOR
1072      020312      012760      040362      014702      MOV      #CPUER, ERRTAB(R0)      ;:FLAG ALL UNEXPECTED TRAPS TO 4
1073      020320      152737      000001      016737      BISB      #BIT0, MPF      ;:SET THE MP FLAG.
1074      020326      000416      BR      31$      ;:LET'S GO
1075      020330      062716      000004      25$:      ADD      #4, (SP)      ;:SKIP RETURN
1076      020334      000002      RTI      ;:RETURN FROM TRAP
```

```

1077 020336 012737 040356 000004 30$: MOV #ERRDIS,@#ERRVEC ;;RESET ERROR VECTOR
1078 020344 012760 040362 014702 MOV #CPUER,ERRTAB(R0) ;;FLAG ALL UNEXPECTED TRAPS TO 4
1079 020352 105037 016737 CLRB MPF ;;CLEAR THE MP FLAG
1080 020356 104401 040663 TYPE ,TM7 ;;[UNIPROCESSOR MODE IS IN EFFECT]
1081 020362 000425 BR 42$ ;;ENTER INTO NON MP EXECUTION STREAM
1082 020364 104401 040616 31$: TYPE ,TM6 ;;[MULTIPROCESSOR MODE IS IN EFFECT]
1083 020370 017737 173564 014660 MOV @SWR,$PSWR ;;SET UP PSEUDO SWITCH REGISTER.
1084 020376 012704 014160 MOV #SWR,R4 ;;POINT TO SWR TABLE
1085 020402 012705 000004 MOV #4,R5 ;;SET COUNTER
1086 020406 012724 014660 41$: MOV #SPSWR,(R4)+ ;;LOAD THE SLAVE SWITCH REG. POINTERS
1087 020412 077503 SOB R5,41$ ;;LOOP TILL DONE
1088 020414 104401 040461 TYPE ,TM2 ;;'SWITCH REGISTER = ''
1089 020420 017746 173534 MOV @SWR,-(SP) ;;SAVE @SWR FOR TYPEOUT
1090 020424 104402 TYPOC ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
1091 020426 104401 014333 TYPE ,SCLRF ;;TYPE CRLF
1092 020432 104401 014333 TYPE ,SCLRF
1093 020436 032777 000040 173514 42$: BIT #UBESW,@SWR ;;UBE SWITCH SET?
1094 020444 001411 BEQ 43$ ;;NOT USED
1095 020446 032777 000200 173504 BIT #SW07, @SWR ;;WILL SECTION 1 BE SKIPPED?
1096 020454 001005 BNE 43$ ;;BRANCH IF YES
1097 020456 104401 040506 TYPE ,TM4 ;;'[UNIBUS EXERCISER WILL BE USED]''
1098 020462 105237 016740 INCB UBEF ;;SET UBE FLAG
1099 020466 000404 BR 65$
1100 020470 104401 040550 43$: TYPE ,TM5 ;;'[UNIBUS EXERCISER WILL NOT BE USED]''
1101 020474 105037 016740 CLRB UBEF ;;CLEAR THE UBE FLAG
1102 020500 105737 016737 65$: TSTB MPF ;;MULTIPROCESSOR MODE IN EFFECT?
1103 020504 001002 BNE 55$ ;;BRANCH IF YES
1104 020506 000137 021046 JMP STO ;;START SETTING UP VECTORS
1105 .SBTTL BOOT AND INITIALIZE THE SLAVE CPUS
1106 020512 017702 173442 55$: MOV @SWR,R2 ;;COPY SWITCH REGISTER INTO R2
1107 020516 012737 000001 016766 MOV #1,CPUACT ;;RESET # OF ACTIVE CPUS
1108 020524 052777 100000 176270 BIS #BIT15,@ACR ;;INITIALIZE THE IIST.
1109 020532 012777 000001 176262 81$: MOV #1,@ACR ;;ACCESS PGCS REGISTER
1110 020540 032777 004000 176256 BIT #BIT11,@ADR ;;IS IT 'ALMOST READY''
1111 020546 001771 BEQ 81$ ;;NOT YET.
1112 020550 012705 002000 MOV #2000,R5 ;;SET UP COUNTER
1113 020554 077501 SOB R5,81$ ;;WAIT UNTIL IIST IS REALLY READY
1114 020556 017705 176240 MOV @ACR,R5 ;;COPY ACR TO R5
1115 020562 072527 177770 ASH #-10,R5 ;;CREAT PHYSICAL ID
1116 020566 104401 041450 TYPE ,TM76 ;;IDENTIFY THE MASTER
1117 020572 010546 MOV R5,-(SP)
1118 020574 104405 TYPDS
1119 020576 010537 014226 MOV R5,$CPUID ;;SET SELF ID OF MASTER IN TABLE
1120 020602 005000 CLR R0 ;;REGO. CONTAINS WORD DISPLACE-
1121 ;;MENT INTO CPUID TABLE ***
1122 020604 005001 CLR R1 ;;R1 CONTAINS THE BYTE DISPLACEMENT,...
1123 ;;THE TRUE LOGICAL ID.
1124 020606 012777 000007 176206 MOV #DCF,@ACR ;;ACCESS DCF REGISTER OF IIST
1125 020614 017703 176204 MOV @ADR,R3 ;;COPY DCF INTO R3
1126 020620 072327 177770 ASH #-10,R3 ;;BRING BRK MASK INTO POSITION
1127 020624 012777 021110 176174 MOV #SLVENT,@ISTVEC ;;SET ENTRY POINT FOR SLAVES
1128
1129 020632 005004 CLR R4 ;;R4 CONTAINS THE DECIMAL VALUE
1130 ;;OF THE SELF ID OF THE CPU UNDER
1131 ;;INTEROGATION.
1132 020634 032702 000001 1$: BIT #BIT0,R2 ;;DO WE WANT THIS CPU?

```

```

1133 020640 001462          BEQ      2$          ;;NO,CONTINUE
1134 020642 032703 000001  BIT      #BIT0,R3    ;;IS IT ALIVE?
1135 020646 001413          BEQ      82$          ;;YES
1136 020650 010437 014310  MOV      R4,$TMP0    ;;SAVE CONTENTS OF R4
1137 020654 104401 014333  TYPE    , $CRLF      ;;NO,CRLF
1138 020660 104401 040761  TYPE    , TM11       ;;'CPU #'
1139 020664 013746 014310  MOV      $TMP0,-(SP) ;;SAVE $TMP0 FOR TYPEOUT
1140 020670 104405          TYPDS          ;;GO TYPE--DECIMAL ASCII WITH SIGN
1141 020672 104401 040772  TYPE    , TM12       ;;'SPECIFIED BUT NOT ACTIVE'
1142 020676 020437 014226          82$:  CMP      R4,$CPUID ;;IS THIS THE MASTER?
1143 020702 001441          BEQ      2$          ;;YES, IGNORE
1144 020704 012737 020000 000000  MOV      #20000,@#0  ;;M9312MP MOVES @#0 TO SP ON BOOT
1145 020712 012777 000000 176102  MOV      #PGTE,@ACR  ;;ACCESS PGTE REG.
1146 020720 013777 017032 176076  MOV      BMSK,@ADR  ;;SET TO BOOT AND THEN...
1147 020726 052777 000001 176070  BIS      #BIT0,@ADR  ;;BOOT THE CPU
1148 020734 012701 000200          MOV      #200, R1   ;;SET UP A LONG DELAY (5 SEC)
1149 020740 077001          SOB          ;;
1150 020742 077102          SOB      R1, 70$   ;;
1151 020744 012777 000001 176050 83$:  MOV      #PGCS,@ACR ;;CHECK FOR IIST READY
1152 020752 032777 004000 176044  BIT      #BIT11,@ADR
1153 020760 001771          BEQ      83$          ;;BRANCH IF NOT
1154 020762 005077 176034          84$:  CLR      @ACR      ;;RESET ACR (POINT TO PGTE)
1155 020766 013777 016772 176030  MOV      INTMSK,@ADR ;;SET UP TO INTERRUPT
1156 020774 052777 000001 176022  BIS      #BIT0,@ADR  ;;GO!, INTERRUPT SLAVE
1157 021002 005237 016766          INC      CPUACT    ;;COUNT ANOTHER ACTIVE CPU
1158 021006 020427 000003          2$:  CMP      R4,#3     ;;ALL CPUS STARTED?
1159 021012 002010          BGE          ;;YES
1160 021014 005204          INC      R4        ;;NEXT CPU TO ATTEMPT TO BOOT
1161 021016 006202          ASR      R2        ;;NEXT SWITCH REG. BIT
1162 021020 006203          ASR      R3        ;;NEXT BRK BIT TO SET
1163 021022 006337 017032          ASL      BMSK      ;;NEXT BOOT MASK
1164 021026 006337 016772          ASL      INTMSK    ;;NEXT INTERRUPT MASK
1165 021032 000700          BR       1$        ;;GO TRY ANOTHER
1166 021034 052737 001000 177746 3$:  BIS      #BIT9, CONTRL ;;SET CACHE BYPASS
1167 021042 005037 000000          CLR      @#0      ;;RESTORE LOC. 0
1168

```

```

1169          .SBTTL INITIALIZE THE COMMON TAGS
1170
1171
1172
1173          ;; CLEAR THE COMMON TAGS (%CMTAG) AREA
1174 021046 052737 000014 177746 STO:  BIS    #14,    CONTRL  ;;DISABLE CACHE
1175 021054 012706 014000          MOV    #%CMTAG,R6  ;;FIRST LOCATION TO BE CLEARED
1176 021060 005026          CLR    (R6)+      ;;CLEAR MEMORY LOCATION
1177 021062 022706 014160          CMP    #SWR,R6  ;;DONE?
1178 021066 001374          BNE    -6          ;;LOOP BACK IF NO
1179 021070 013706 014200          MOV    $$STP,SP   ;;SETUP THE STACK POINTER
1180 021074 013737 035200 035166  MOV    $ENDCT,$EOPCT ;;SETUP END-OF-PROGRAM COUNTER
1181 021102 005037 014344          CLR    $PASS     ;;CLEAR PASS COUNT
1182 021106 000432          BR    MSTENT
1183 021110
1184 021110 052737 001000 177746 SLVENT: BIS    #BIT9,@CONTRL ;;TURN OFF CACHE
1185 021116 005237 014644          INC    SLVID     ;;CREATE CPUID
1186 021122 013701 014644          MOV    SLVID,R1  ;;AND MOV TO R1
1187 021126 010100          MOV    R1,R0
1188 021130 006300          ASL    R0          ;;CREATE WORD INDEX INTO CPU TABLE
1189 021132 017705 175664          MOV    @ACR, R5   ;;COPY ACR
1190 021136 072527 177770          ASH    #-10, R5  ;;GET THE ID
1191 021142 010560 014226          MOV    R5,$CPUID(R0) ;;SET SELF-ID INTO TABLE
1192 021146 052777 100000 175646  BIS    #BIT15,@ACR ;;RESET THE IIST
1193 021154 012777 000001 175640  MOV    #PGCS,@ACR  ;;ENABLE INTERRUPTS
1194 021162 052777 000004 175634  BIS    #BIT2,@ADR
1195 021170 005037 177776          CLR    @PSW      ;;LOWER PROCESSOR PRIORITY
1196 021174
1197 021174 005060 014322          CLR    $ESCAPE(R0) ;;CLEAR THE ESCAPE(R0) ON ERROR ADDRESS
1198 021200 016060 021212 014032  MOV    10$(R0),$LPERR(R0) ;;SETUP FOR THE ERROR LOOP ADDRESS
1199 021206 000170 021222          JMP    @FORKTB(R0) ;;DISPATCH THE FOLLOWERS
1200 021212 021420          10$:  TST1
1201 021214 021420          TST1
1202 021216 021420          TST1
1203 021220 021420          TST1
1204 021222 021312          FORKTB: MS0
1205 021224 021232          SL1
1206 021226 021252          SL2
1207 021230 021272          SL3
1208 021232 016006 014200          SL1:  MOV    $$STP(R0),SP ;;INITIALIZE SLAVE STACK (CPU1)
1209 021236 000001          WAIT ;;WAIT FOR MASTER TO START VIA INTERRUPT
1210 021240 052777 100000 175554  BIS    #BIT15,@ACR ;;RESET THE IIST
1211 021246 000137 021420          JMP    TST1
1212 021252 016006 014200          SL2:  MOV    $$STP(R0),SP ;;INITIALIZE SLAVE STACK (CPU2)
1213 021256 000001          WAIT ;;WAIT FOR MASTER TO INTERRUPT
1214 021260 052777 100000 175534  BIS    #BIT15,@ACR ;;RESET THE IIST
1215 021266 000137 021420          JMP    TST1
1216 021272 016006 014200          SL3:  MOV    $$STP(R0),SP ;;INITIALIZE SLAVE STACK (CPU3)
1217 021276 000001          WAIT ;;WAIT FOR MASTER TO INTERRUPT
1218 021300 052777 100000 175514  BIS    #BIT15,@ACR ;;RESET THE IIST
1219 021306 000137 021420          JMP    TST1
1220 021312 105737 016737          MS0:  TSTB  MPF          ;;MP MODE?
1221 021316 001440          BEQ   BEGIN     ;;NO,DON'T TRY TO INTERRUPT CPUS
1222 021320 013702 017026          MOV    ISTVEC, R2 ;;SET UP RETURN FROM INTERRUPT
1223 021324 062702 000002          ADD    #2, R2
1224 021330 010277 175472          MOV    R2,@ISTVEC

```

```
1225 021334 012712 000002          MOV    #2, (R2)
1226 021340 012777 000000 175454    MOV    #PGTE,@ACR      ;ACCESS PGTE REGISTER
1227 021346 017702 172606          MOV    @SWR,R2        ;GET COPY OF SWR
1228 021352 042702 177760          BIC    #177760,R2     ;KEEP ONLY THE CPU MASK
1229 021356 010277 175442          MOV    R2,@ADR        ;SET THE INTERRUPT BITS
1230 021362 032737 000001 016766    BIT    #BIT0,CPUACT   ;EVEN OR ODD?
1231 021370 001404          BEQ    7$             ;BRANCH IF EVEN
1232 021372 012777 000005 175424    MOV    #5,@ADR        ;GO WITH NO PARITY,ENABLE INTERRUPTS
1233 021400 000403          BR     4$
1234 021402 012777 000007 175414 7$:    MOV    #7,@ADR        ;GO WITH PARITY,ENABLE INTS.
1235 021410 000001          4$:    WAIT                ;WAIT FOR IIST TO INTERRUPT
1236 021412 052777 100000 175402    BIS    #BIT15,@ACR    ;:RESET THE IIST
1237 021420          BEGIN:
```

1238  
1239  
1240  
1241  
1242  
1243  
1244  
1245  
1246  
1247  
1248  
1249  
1250  
1251  
1252  
1253  
1254  
1255  
1256  
1257  
1258  
1259  
1260  
1261

```
.....  
.....  
.....  
..... SECTION ONE .....  
.....  
.....  
.....
```

M  
C

```

1262
1263
1264
1265 021420
1266 021420 012777 000001 172542
1267 021426 012737 033530 014662
1268 021434 012737 033074 000114
1269 021442 012737 000001 033076
1270 021450 012737 040340 000024
1271 021456 005037 000026
1272 021462 032770 000200 014160
1273 021470 001402
1274 021472 000137 024170
1275 021476 005700 1$: TST R0 ;IS THIS THE MASTER?
1276 021500 001011 BNE 4$ ;BRANCH IF NO
1277 021502 104401 041370 TYPE .TM14 ;'ENTERING SECTION 1''
1278 021506 105737 016740 TSTB UBEF ;USING THE UBE?
1279 021512 001004 BNE 4$ ;BRANCH IF YES
1280 021514 104401 041024 TYPE .TM13 ;PRINT INSTRUCTIONS
1281 021520 104401 014333 TYPE .$CRLF
1282 021524 4$:
1283 021524 005037 177776 CLR @#PS ;SET KERNAL MODE
1284 021530 012703 021566 MOV #2$,R3 ;SET POWER UP RETURN
1285 021534 105737 016740 TSTB UBEF ;:USE UNIBUS EXERCISER?
1286 021540 001407 BEQ 64$ ;:BRANCH IF NO
1287 021542 106237 017014 ASRB UBELCK ;LOCK OUT OTHER CPUS FROM PROCEEDING
1288 021546 103375 BCC -4
1289 021550 000241 CLC
1290 021552 052737 000020 170016 BIS #BIT4,@#UBCR2 ;:SET TO POWER FAIL
1291 021560 64$:
1292 021560 3$:
1293 021560 005037 177776 CLR @#PS ;SET KERNAL MODE
1294 021564 000001 WAIT ;WAIT FOR THE POWER FAIL
1295 021566 010602 2$: MOV SP,R2 ;GET SP
1296 021570 016004 014200 MOV $$STP(R0),R4 ;R4 CONTAINS THE STACK INIT. VALUE
1297 021574 162704 000004 SUB #4,R4 ;STACK-4
1298 021600 020402 CMP R4,R2 ;CHECK STACK
1299 021602 001401 BEQ .+4 ;SKIP IF OK
1300 021604 000000 HALT ;SP NOT 'STACK-4''
1301 021606 016006 014200 MOV $$STP(R0),SP ;RESET SP
1302 021612 012402 MOV (R4)+,R2 ;GET RETURN ADDRESS
1303 021614 105737 016740 TSTB UBEF ;IS THE UBE BEING USED?
1304 021620 001004 BNE 72$ ;YES
1305 021622 022702 021566 70$: CMP #2$,R2 ;CHECK ADDRESS
1306 021626 001401 BEQ .+4 ;SKIP IF OK
1307 021630 000000 HALT ;ADDRESS ON STACK IS WRONG
1308 021632 011402 72$: MOV (R4),R2 ;GET OLD PS
1309 021634 022702 000000 CMP #0,R2 ;CHECK OLD PS
1310 021640 001401 BEQ .+4 ;SKIP IF OK
1311 021642 000000 HALT ;OLD PS IS WRONG
1312 021644 032770 040000 014160 BIT #SW14,@SWR(R0) ;LOOP ON TEST?
1313 021652 001262 BNE TST1 ;LOOP TO TST1
1314
1315
1316
1317

```

\*\*\*\*\*  
 ;\*TEST 2 PROGRAM VOLATILITY TEST

```

1318
1319 021654
1320 021654 012777 000002 172306
1321 021662 005037 177776
1322 021666 012702 010000
1323 021672 012703 020000
1324 021676 005060 014650
1325 021702 062360 014650
1326 021706 005560 014650
1327 021712 077205
1328 021714 012703 021750
1329 021720 105737 016740
1330 021724 001407
1331 021726 106237 017014
1332 021732 103375
1333 021734 000241
1334 021736 052737 000020 170016
1335 021744
1336 021744 000001
1337 021746 000000
1338 021750 012702 010000
1339 021754 012703 020000
1340 021760 005004
1341
1342 021762 062304
1343 021764 005504
1344 021766 077203
1345 021770 020460 014650
1346 021774 001401
1347 021776 000000
1348 022000 016006 014200
1349 022004 032770 040000 014160
1350 022012 001320
1351
1352
1353
1354 022014
1355 022014 012777 000003 172146
1356 022022 012737 040000 177776
1357 022030 012703 022070
1358 022034 105737 016740
1359 022040 001407
1360 022042 106237 017014
1361 022046 103375
1362 022050 000241
1363 022052 052737 000020 170016
1364 022060
1365 022060
1366 022060 012737 040000 177776
1367 022066 000001
1368 022070 016006 014200
1369 022074 016004 014200
1370 022100 162704 000004

```

```

*****
TST2:
MOV #2,@DISPLAY ;SET TEST NUMBER
CLR @#PS ;SET KERNAL MODE
MOV #10000,R2 ;INIT. COUNTER
MOV #20000,R3 ;INIT POINTER
CLR CKSUM(R0) ;RESET THE CHECKSUM LOCATION
1$: ADD (R3)+,CKSUM(R0) ;DO CHECKSUM ON 2ND 4K(W) BANK
ADC CKSUM(R0)
SOB R2,1$
MOV #2$,R3 ;POWER UP RETURN
TSTB UBEF ;:USE UNIBUS EXERCISER?
BEQ 64$ ;:BRANCH IF NO
ASRB UBELCK ;LOCK OUT OTHER CPUS FROM PROCEEDING
BCC -4
CLC
BIS #BIT4,@#UBCR2 ;:SET TO POWER FAIL
64$: WAIT ;WAIT FOR THE POWER TO FAIL
HALT ;BAD
2$: MOV #10000,R2
MOV #20000,R3
CLR R4
;VERIFY THAT EVERYTHING IS OK
3$: ADD (R3)+,R4
ADC R4
SOB R2,3$
CMP R4,CKSUM(R0) ;COMPARE NEW CHECKSUM WITH OLD
BEQ 5$ ;BRANCH IF OK
HALT ;ERROR
5$: MOV $$STP(R0),SP ;RESET THE STACK
BIT #SW14,@#SWR(R0) ;LOOP ON TEST?
BNE TST2 ;LOOP TO TST2
*****
*TEST 3 SIMPLE DOWN/UP TEST (SUPERVISOR)
*****
TST3:
MOV #3,@DISPLAY ;SET TEST NUMBER
MOV #40000,@#PS ;SET SUPERVISOR MODE
MOV #2$,R3 ;SET POWER UP RETURN
TSTB UBEF ;:USE UNIBUS EXERCISER?
BEQ 64$ ;:BRANCH IF NO
ASRB UBELCK ;LOCK OUT OTHER CPUS FROM PROCEEDING
BCC -4
CLC
BIS #BIT4,@#UBCR2 ;:SET TO POWER FAIL
64$:
3$: MOV #40000,@#PS ;SET SUPERVISOR MODE
WAIT ;WAIT FOR THE POWER FAIL
2$: MOV $$STP(R0),SP ;RESET
MOV $$STP(R0),R4
SUB #4,R4

```



```

1371 022104 012402          MOV      (R4)+,R2      ;GET RETURN ADDRESS
1372 022106 105737 016740    TSTB    UBEF          ;
1373 022112 001004          BNE     72$          ;
1374 022114 022702 022070    70$:    CMP      #2$,R2      ;CHECK ADDRESS
1375 022120 001401          BEQ     .+4          ;SKIP IF OK
1376 022122 000000          HALT    ;ADDRESS ON STACK IS WRONG
1377 022124 011402          72$:    MOV      (R4),R2      ;GET OLD PS
1378 022126 022702 040000    CMP     #40000,R2    ;CHECK OLD PS
1379 022132 001401          BEQ     .+4          ;SKIP IF OK
1380 022134 000000          HALT    ;OLD PS IS WRONG
1381 022136
1382 022136 032770 040000 014160 1$:      BIT     #SW14,@SWR(R0) ;LOOP ON TEST?
1383 022144 001323          BNE     TST3        ;LOOP TO TST3
1384
1385
1386
1387
1388
1389 022146
1390 022146 012777 000004 172014  TST4:   MOV     #4,@DISPLAY    ;SET TEST NUMBER
1391 022154 012737 140000 177776    MOV     #140000,@#PS  ;SET USER MODE
1392 022162 012703 022222          MOV     #2$,R3        ;SET POWER UP RETURN
1393 022166 105737 016740          TSTB    UBEF          ;:USE UNIBUS EXERCISER?
1394 022172 001407          BEQ     64$          ;:BRANCH IF NO
1395 022174 106237 017014          ASRB    UBELCK        ;LOCK OUT OTHER CPUS FROM PROCEEDING
1396 022200 103375          BCC     .-4          ;
1397 022202 000241          CLC
1398 022204 052737 000020 170016    BIS     #BIT4,@#UBCR2 ;:SET TO POWER FAIL
1399 022212
1400 022212          64$:
1401 022212 012737 140000 177776    3$:    MOV     #140000,@#PS  ;SET USER MODE
1402 022220 000001          WAIT   ;WAIT FOR THE POWER FAIL
1403 022222 016006 014200          2$:    MOV     $$STP(R0),SP ;RESET SP
1404 022226 016004 014200          MOV     $$STP(R0),R4 ;GET STACK INIT. VALUE
1405 022232 162704 000004          SUB     #4,R4         ;MINUS 4
1406 022236 012402          MOV     (R4)+,R2     ;GET STACK-4,AUTOINC. STACK
1407 022240 105737 016740          TSTB    UBEF          ;
1408 022244 001004          BNE     72$          ;
1409 022246 022702 022222    70$:    CMP     #2$,R2      ;CHECK ADDRESS
1410 022252 001401          BEQ     .+4          ;SKIP IF OK
1411 022254 000000          HALT    ;ADDRESS ON STACK IS WRONG
1412 022256 011402          72$:    MOV     (R4),R2      ;GET OLD PS
1413 022260 022702 140000    CMP     #140000,R2   ;CHECK OLD PS
1414 022264 001401          BEQ     .+4          ;SKIP IF OK
1415 022266 000000          HALT    ;OLD PS IS WRONG
1416 022270 032770 040000 014160    BIT     #SW14,@SWR(R0) ;LOOP ON TEST?
1417 022276 001323          BNE     TST4        ;LOOP TO TST4
1418
1419
1420
1421
1422
1423
1424 022300
1425 022300 012777 000005 171662  TST5:   MOV     #5,@DISPLAY    ;SET TEST NUMBER
1426 022306 005037 177776    CLR     @#PS         ;SET KERNAL MODE

```



```
1446
1447
1448
1449 022414
1450 022414 012777 000006 171546
1451 022422 005037 177776
1452 022426 012760 022476 014702
1453 022434 012703 022530
1454 022440 012706 000002
1455 022444 105737 016740
1456 022450 001407
1457 022452 106237 017014
1458 022456 103375
1459 022460 000241
1460 022462 052737 000020 170016
1461 022470
1462 022470 005037 177776
1463 022474 000001
1464 022476 012737 022504 014662
1465 022504
1466 022504 105737 016740
1467 022510 001403
1468 022512 042737 000020 170016
1469 022520
1470 022520 000000
1471 022522 012737 033530 014662
1472 022530 016006 014200
1473 022534 012760 040362 014702
1474 022542 013702 000002
1475 022546 023727 000002 000000
1476 022554 001401
1477 022556 000000
1478 022560 013702 000000
1479 022564 022737 040340 000000
1480 022572 001401
1481 022574 000000
1482 022576 032770 040000 014160
1483 022604 001303
1484
1485
1486
1487
1488
1489 022606
1490 022606 012777 000007 171354
1491 022614 005037 177776
1492 022620 012760 022656 014702
1493 022626 012703 022710
1494 022632 105737 016740
1495 022636 001407
1496 022640 106237 017014
1497 022644 103375
1498 022646 000241
1499 022650 052737 000020 170016
1500 022656
1501 022656 016006 014200
```

```
*****
*TEST 6 POWER FAIL IN THE RED ZONE
*****
TST6:
MOV #6,@DISPLAY ;SET TEST NUMBER
CLR @#PS ;SET KERNAL MODE
MOV #2$,ERRTAB(R0) ;SET TRAP REGISTER
MOV #1$,R3 ;SET POWER UP RETURN
MOV #2,SP ;SET STACK TO RED ZONE
TSTB UBEF ;;USE UNIBUS EXERCISER?
BEQ 64$ ;;BRANCH IF NO
ASRB UBELCK ;LOCK OUT OTHER CPUS FROM PROCEEDING
BCC -4
CLC
BIS #BIT4,@#UBCR2 ;;SET TO POWER FAIL
64$: CLR @#PS ;SET KERNAL MODE
WAIT ;WAIT FOR POWER FAIL TRAP
MOV #7$,PWRTAB ;SET UVEC TO HALT
7$: TSTB UBEF ;;USE UNIBUS EXERCISER?
BEQ 65$
BIC #BIT4,@#UBCR2 ;;CLEAR POWER FAIL ENABLE
65$: HALT ;ILLEGAL TRAP TO 4
MOV #POWDWN,PWRTAB ;RESET DVEC
1$: MOV $$STP(R0),SP ;RESET STACK
MOV #CPUER,ERRTAB(R0) ;RESET 4
MOV @#2,R2 ;GET FOR TYPING
CMP @#2,#0 ;IS 2 OK?
BEQ .+4 ;SKIP IF OK
HALT ;NO!
MOV @#0,R2 ;GET FOR TYPING
CMP #PWRDIS,@#0 ;IS 0 OK?
BEQ .+4 ;SKIP IF OK
HALT ;0 IS WRONG!
BIT #SW14,@SWR(R0) ;LOOP ON TEST?
BNE TST6 ;LOOP TO TST6
```

```
*****
*TEST 7 POWER FAIL WITH TIME OUT (KERNAL)
*****
TST7:
MOV #7,@DISPLAY ;SET TEST NUMBER
CLR @#PS ;SET KERNAL MODE
MOV #3$,ERRTAB(RC) ;SET TRAP VECTOR
MOV #1$,R3 ;SET UP RETURN ADDRESS FOR POWER FAIL
TSTB UBEF ;;USE UNIBUS EXERCISER?
BEQ 64$ ;;BRANCH IF NO
ASRB UBELCK ;LOCK OUT OTHER CPUS FROM PROCEEDING
BCC -4
CLC
BIS #BIT4,@#UBCR2 ;;SET TO POWER FAIL
64$: MOV $$STP(R0),SP ;SET STACK
3$:
```

```

1502 022662 005037 177776 CLR @#PS ;SET KERNAL MODE
1503 022666 010037 173000 MOV R0,@#173000 ;CAUSE A TIMEOUT
1504 022672 105737 016740 TSTB UBEF ;;USE UNIBUS EXERCISER?
1505 022676 001403 BEQ 65$
1506 022700 042737 000020 170016 BIC #BIT4,@#UBCR2 ;;CLEAR POWER FAIL ENABLE
1507 022706 65$:
1508 022706 000000 HALT ;TIMEOUT FAILED
1509 022710 016006 014200 1$: MOV $$STP(R0),SP ;SET STACK
1510 022714 012760 040362 014702 MOV #CPUER,ERRTAB(R0) ;RESET 4
1511 022722 032770 040000 014160 BIT #SW14,@SWR(R0) ;LOOP ON TEST?
1512 022730 001326 BNE TST7 ;LOOP TO TST7
1513
1514
1515 ;*****
1516 ;*TEST 10 POWER FAIL IN THE YELLOW ZONE (KERNAL)
1517 ;*****
1518 022732 TST10:
1519 022732 012777 000010 171230 MOV #10,@DISPLAY ;SET TEST NUMBER
1520 022740 005037 177776 CLR @#PS ;SET KERNAL MODE
1521 022744 005037 014602 CLR FLAG ;CLEAR THE FLAG
1522 022750 012760 023040 014702 MOV #2$,ERRTAB(R0) ;SET SICK TPAP ADDRESS
1523 022756 012706 000400 MOV #400,SP ;SET STACK TO YELLOW ZONE
1524 022762 012703 023020 MOV #1$,R3 ;SET RETURN ADDRESS FOR POWER FAIL
1525 022766 105737 016740 TSTB UBEF ;;USE UNIBUS EXERCISER?
1526 022772 001407 BEQ 64$ ;;BRANCH IF NO
1527 022774 106237 017014 ASRB UBELCK ;LOCK OUT OTHER CPUS FROM PROCEEDING
1528 023000 103375 BCC -4
1529 023002 000241 CLC
1530 023004 052737 000020 170016 BIS #BIT4,@#UBCR2 ;;SET TO POWER FAIL
1531 023012 64$:
1532 023012 005037 177776 CLR @#PS ;SET KERNAL MODE
1533 023016 000001 WAIT ;WAIT FOR POWER FAIL
1534 023020 1$:
1535 023020 105737 016740 TSTB UBEF ;;USE UNIBUS EXERCISER?
1536 023024 001403 BEQ 65$
1537 023026 042737 000020 170016 BIC #BIT4,@#UBCR2 ;;CLEAR POWER FAIL ENABLE
1538 023034 65$:
1539 023034 000000 HALT ;POWER FAIL RETURNED TOO SOON
1540 023036 000430 BR 4$ ;SKIP SP CHECK
1541 023040 012760 040362 014702 2$: MOV #CPUER,ERRTAB(R0) ;RESET 4
1542 023046 005737 014602 TST FLAG ;IS THE FIRST INSTRUCTION FLAG SET?
1543 023052 001016 BNE 5$ ;YES
1544 023054 012737 023062 014662 MOV #7$,PWRTAB ;SET UVEC TO HALT
1545 023062 7$:
1546 023062 105737 016740 TSTB UBEF ;;USE UNIBUS EXERCISER?
1547 023066 001403 BEQ 66$
1548 023070 042737 000020 170016 BIC #BIT4,@#UBCR2 ;;CLEAR POWER FAIL ENABLE
1549 023076 66$:
1550 023076 000000 HALT ;NOT ENOUGH OR TOO MANY INSTR. EXEC.
1551 023100 012737 033530 014662 MOV #POWDWN,PWRTAB ;SET DVEC
1552 023106 000404 BR 4$ ;GET OUT
1553 023110 012703 023120 5$: MOV #4$,R3 ;SET RETURN
1554 023114 000002 RTI ;GO TO THE POWER FAIL ROUTINE
1555 023116 000000 HALT ;SHOULD NOT RETURN HERE
1556 023120 4$:
1557 023120 032770 040000 014160 BIT #SW14,@SWR(R0) ;LOOP ON TEST?

```

```

1558 023126 001301          BNE      TST10          ;LOOP TO TST10
1559
1560
1561          ;:*****
1562          ;*TEST 11      POWER FAIL WITH RESETS
1563          ;:*****
1564 023130          TST11:
1565 023130 012777 000011 171032      MOV      #11,@DISPLAY      ;SET TEST NUMBER
1566 023136 005037 177776          CLR      @MPS              ;SET KERNAL MODE
1567 023142 012703 023206          MOV      #1$,R3           ;SET RETURN ADDRESS
1568 023146 016006 014200          MOV      $$STP(R0),SP     ;RESET STACK
1569 023152 105737 016740          TSTB    UBEF              ;;USE UNIBUS EXERCISER?
1570 023156 001407          BEQ      64$              ;;BRANCH IF NO
1571 023160 106237 017014          ASRB    UBELCK           ;LOCK OUT OTHER CPUS FROM PROCEEDING
1572 023164 103375          BCC     -.4
1573 023166 000241          CLC
1574 023170 052737 000020 170016      BIS     #BIT4,@UBCR2      ;;SET TO POWER FAIL
1575 023176          64$:
1576 023176 000005          3$:      RESET             ;RESETS
1577 023200 000005          RESET    ;TO WAIT
1578 023202 000005          RESET    ;IN
1579 023204 000774          BR       3$              ;LOOP
1580 023206 016006 014200          1$:      MOV      $$STP(R0),SP     ;RESET STACK
1581 023212 032770 040000 014160      BIT     #SW14,@SWR(R0)   ;LOOP ON TEST?
1582 023220 001343          BNE     TST11           ;LOOP TO TST11
1583
1584
1585          ;:*****
1586          ;*TEST 12      POWER FAIL WITH ODD ADDRESS (SUPERVISOR)
1587          ;:*****
1588 023222          TST12:
1589 023222 012777 000012 170740      MOV      #12,@DISPLAY     ;SET TEST NUMBER
1590 023230 012737 040000 177776      MOV      #40000,@MPS      ;SET SUPERVISOR MODE
1591 023236 012760 023274 014702      MOV      #3$,ERRTAB(R0)   ;SET TRAP VECTOR
1592 023244 012703 023334          MOV      #1$,R3           ;SET RETURN ADDRESS FOR POWER FAIL
1593 023250 105737 016740          TSTB    UBEF              ;;USE UNIBUS EXERCISER?
1594 023254 001407          BEQ      64$              ;;BRANCH IF NO
1595 023256 106237 017014          ASRB    UBELCK           ;LOCK OUT OTHER CPUS FROM PROCEEDING
1596 023262 103375          BCC     -.4
1597 023264 000241          CLC
1598 023266 052737 000020 170016      BIS     #BIT4,@UBCR2      ;;SET TO POWER FAIL
1599 023274          64$:
1600 023274 016006 014200          3$:      MOV      $$STP(R0),SP     ;RESET STACK
1601 023300 012737 040000 177776      MOV      #40000,@MPS      ;SET SUPERVISOR MODE
1602 023306 005737 000003          TST     @M3              ;CAUSE ODD ADDRESS TRAP
1603 023312 005037 177776          CLR     @MPS             ;SET KERNAL MODE
1604 023316 105737 016740          TSTB    UBEF              ;;USE UNIBUS EXERCISER?
1605 023322 001403          BEQ     65$
1606 023324 042737 000020 170016      BIC     #BIT4,@UBCR2      ;;CLEAR POWER FAIL ENABLE
1607 023332          65$:
1608 023332 000000          HALT    ;ODD ADDRESS TRAP FAILED
1609 023334 016006 014200          1$:      MOV      $$STP(R0),SP     ;RESET STACK POINTER
1610 023340 012760 040362 014702      MOV     #CPUER,ERRTAB(R0) ;RESET 4
1611 023346 032770 040000 014160      BIT     #SW14,@SWR(R0)   ;LOOP ON TEST?
1612 023354 001322          BNE     TST12           ;LOOP TO TST12
1613

```

```

1614
1615
1616
1617
1618 023356
1619 023356 012777 000013 170604
1620 023364 012737 040000 177776
1621 023372 012760 023430 014702
1622 023400 012703 023470
1623 023404 105737 016740
1624 023410 001407
1625 023412 106237 017014
1626 023416 103375
1627 023420 000241
1628 023422 052737 000020 170016
1629 023430
1630 023430 016006 014200
1631 023434 012737 040000 177776
1632 023442 010037 173000
1633 023446 005037 177776
1634 023452 105737 016740
1635 023456 001403
1636 023460 042737 000020 170016
1637 023466
1638 023466 000000
1639 023470 016006 014200
1640 023474 012760 040362 014702
1641 023502 032770 040000 014160
1642 023510 001322
1643
1644
1645
1646
1647
1648 023512
1649 023512 012777 000014 170450
1650 023520 012737 140000 177776
1651 023526 012760 023564 014702
1652 023534 012703 023624
1653 023540 105737 016740
1654 023544 001407
1655 023546 106237 017014
1656 023552 103375
1657 023554 000241
1658 023556 052737 000020 170016
1659 023564
1660 023564 016006 014200
1661 023570 012737 140000 177776
1662 023576 005737 000003
1663 023602 005037 177776
1664 023606 105737 016740
1665 023612 001403
1666 023614 042737 000020 170016
1667 023622
1668 023622 000000
1669 023624 016006 014200

```

```

*****
*TEST 13 POWER FAIL WITH TIME OUT (SUPERVISOR)
*****

```

```

TST13:
MOV #13,@DISPLAY ;SET TEST NUMBER
MOV #40000,@#PS ;SET SUPERVISOR MODE
MOV #3$,ERRTAB(R0) ;SET TRAP VECTOR
MOV #1$,R3 ;SET UP RETURN ADDRESS FOR POWER FAIL
TSTB UBEF ;:USE UNIBUS EXERCISER?
BEQ 64$ ;:BRANCH IF NO
ASRB UBELCK ;LOCK OUT OTHER CPUS FROM PROCEEDING
BCC -4
CLC
BIS #BIT4,@#UBCR2 ;:SET TO POWER FAIL
64$:
3$: MOV $$STP(R0),SP ;RESET STACK
MOV #40000,@#PS ;SET SUPERVISOR MODE
MOV R0,@#173000 ;CAUSE A TIMEOUT
CLR @#PS ;SET KERNAL MODE
TSTB UBEF ;:USE UNIBUS EXERCISER?
BEQ 65$
BIC #BIT4,@#UBCR2 ;:CLEAR POWER FAIL ENABLE
65$:
1$: HALT ;TIMEOUT FAILED
MOV $$STP(R0),SP ;RESET STACK
MOV #CPUER,ERRTAB(R0) ;RESET 4
BIT #SW14,@#SWR(R0) ;LOOP ON TEST?
BNE TST13 ;LOOP TO TST13

```

```

*****
*TEST 14 POWER FAIL WITH ODD ADDRESS (USER)
*****

```

```

TST14:
MOV #14,@DISPLAY ;SET TEST NUMBER
MOV #140000,@#PS ;SET USER MODE
MOV #3$,ERRTAB(R0) ;SET TRAP VECTOR
MOV #1$,R3 ;SET RETURN ADDRESS FOR POWER FAIL
TSTB UBEF ;:USE UNIBUS EXERCISER?
BEQ 64$ ;:BRANCH IF NO
ASRB UBELCK ;LOCK OUT OTHER CPUS FROM PROCFEDING
BCC -4
CLC
BIS #BIT4,@#UBCR2 ;:SET TO POWER FAIL
64$:
3$: MOV $$STP(R0),SP ;RESET STACK
MOV #140000,@#PS ;SET USER MODE
TST @#3 ;CAUSE ODD ADDRESS TRAP
CLR @#PS ;SET KERNAL MODE
TSTB UBEF ;:USE UNIBUS EXERCISER?
BEQ 65$
BIC #BIT4,@#UBCR2 ;:CLEAR POWER FAIL ENABLE
65$:
1$: HALT ;ODD ADDRESS TRAP FAILED
MOV $$STP(R0),SP ;RESET SP

```

```

1670 023630 012760 040362 014702
1671 023636 032770 040000 014160
1672 023644 001322
1673
1674
1675
1676
1677
1678 023646
1679 023646 012777 000015 170314
1680 023654 012737 140000 177776
1681 023662 012760 023720 014702
1682 023670 012703 023760
1683 023674 105737 016740
1684 023700 001407
1685 023702 106237 017014
1686 023706 103375
1687 023710 000241
1688 023712 052737 000020 170016
1689 023720
1690 023720 016006 014200
1691 023724 012737 140000 177776
1692 023732 010037 173000
1693 023736 005037 177776
1694 023742 105737 016740
1695 023746 001403
1696 023750 042737 000020 170016
1697 023756
1698 023756 000000
1699 023760 016006 014200
1700 023764 012760 040362 014702
1701 023772 032770 040000 014160
1702 024000 001322
1703
1704
1705
1706
1707
1708 024002
1709 024002 012777 000016 170160
1710 024010 005037 177776
1711 024014 012760 004000 014612
1712 024022 012760 024122 014702
1713 024030 004737 033142
1714 024034 012737 024076 000250
1715 024042 012703 024124
1716 024046 005237 177572
1717 024052 105737 016740
1718 024056 001407
1719 024060 106237 017014
1720 024064 103375
1721 024066 000241
1722 024070 052737 000020 170016
1723 024076
1724 024076 016006 014200
1725 024102 005237 140000

```

```

MOV #CPUER,ERRTAB(R0) ;RESET 4
BIT #SW14,@SWR(R0) ;LOOP ON TEST?
BNE TST14 ;LOOP TO TST14

:*****
:*TEST 15 POWER FAIL WITH TIME OUT (USER)
:*****
TST15:
MOV #15,@DISPLAY ;SET TEST NUMBER
MOV #140000,@NPS ;SET USER MODE
MOV #3$,ERRTAB(R0) ;SET TRAP VECTOR
MOV #1$,R3 ;SET UP RETURN ADDRESS FOR POWER FAIL
TSTB UBEF ;:USE UNIBUS EXERCISER?
BEQ 64$ ;:BRANCH IF NO
ASRB UBELCK ;LOCK OUT OTHER CPUS FROM PROCEEDING
BCC .-4
CLC
BIS #BIT4,@UBCR2 ;:SET TO POWER FAIL
64$:
3$: MOV $$STP(R0),SP ;RESET STACK
MOV #140000,@NPS ;SET USER MODE
MOV R0,@#173000 ;CAUSE A TIMEOUT
CLR @NFS ;SET KERNAL MODE
TSTB UBEF ;:USE UNIBUS EXERCISER?
BEQ 65$
BIC #BIT4,@UBCR2 ;:CLEAR POWER FAIL ENABLE
65$:
1$: HALT ;TIMEOUT FAILED
MOV $$STP(R0),SP ;RESET STACK
MOV #CPUER,ERRTAB(R0) ;RESET 4
BIT #SW14,@SWR(R0) ;LOOP ON TEST?
BNE TST15 ;LOOP TO TST15

```

```

:*****
:*TEST 16 MEMORY MANAGEMENT ABORT TEST
:*****
TST16:
MOV #16,@DISPLAY ;SET TEST NUMBER
CLR @NFS ;SET KERNAL MODE
MOV #TI, PFFT(R0) ;TIME THIS POWER FAIL
MOV #4$,ERRTAB(R0) ;SET FOR TIMEOUT
JSR PC,MAP ;MAP THE WORLD
MOV #3$,@MMVEC ;SET MEMORY MANAGEMENT VECTOR
MOV #1$,R3 ;LOAD PF RETURN
INC @MMR0 ;TURN MEMORY MANAGEMENT ON
TSTB UBEF ;:USE UNIBUS EXERCISER?
BEQ 64$ ;:BRANCH IF NO
ASRB UBELCK ;LOCK OUT OTHER CPUS FROM PROCEEDING
BCC .-4
CLC
BIS #BIT4,@UBCR2 ;:SET TO POWER FAIL
64$:
3$: MOV $$STP(R0),SP ;ZAP STACK
INC @#140000 ;ACCESS VIOLATION

```

```
1726 024106 105737 016740      TSTB  UBEF      ;;USE UNIBUS EXERCISER?
1727 024112 001403              BEQ    65$
1728 024114 042737 000020 170016  BIC    #BIT4,@#UBCR2 ;;CLEAR POWER FAIL ENABLE
1729 024122              65$:
1730 024122 000000              4$: HALT      ;NO VIOLATION OR TRAP TO 4
1731
1732 024124 005037 177572              1$: CLR    @MMRO      ;TURN OFF MEMORY MANAGEMENT
1733 024130 016006 014200              2$: MOV    $$STP(R0),SP ;MAKE A NEW STACK
1734 024134 012760 040362 014702      MOV    #CPUER,ERRTAB(R0) ;RESET 4
1735 024142 032770 040000 014160      BIT    #SW14,@SWR(R0) ;LOOP ON TEST?
1736 024150 001314              BNE    TST16      ;LOOP TO TST16
1737 024152 005077 170012      CLR    @DISPLA    ;CLEAR THE DISPLAY REGISTER.
1738 024156 105737 016737      TSTB  MPF        ;MP MODE?
1739 024162 001002              BNE    5$         ;BRANCH IF YES
1740 024164 000137 035060              JMP    $EOP       ;UUMP INTO EOP
1741 024170              5$:
```



1742

1743  
1744  
1745  
1746  
1747  
1748  
1749  
1750  
1751  
1752  
1753  
1754  
1755  
1756  
1757  
1758  
1759  
1760  
1761  
1762  
1763  
1764  
1765

:\*\*\*\*\*  
:\*\*\*\*\*  
:\*\*\*\*\*  
:\*\*\*\*\* SECTION TWO \*\*\*\*\*  
:\*\*\*\*\*  
:\*\*\*\*\*  
:\*\*\*\*\*

```

1766          .SBTTL SECTION 2 INITIALIZATION
1767 024170 012703 024214          SEC2: MOV #1$, R3          ;SET UP POWER FAIL RETURN IN CASE
1768 024174 106237 016770          ASRB SYNC.3          ;CONTROL THE ENTRY
1769 024200 103373                   BCC SEC2
1770 024202 005237 016716          INC S2LOG1          ;LOG INTO SEC2
1771 024206 012737 000001 016770  MOV #1, SYNC.3          ;LET THE OTHERS IN
1772 024214 023737 016716 016766  1$: CMP S2LOG1,CPUACT    ;:WAIT FOR EVERYONE TO GET ...
1773 024222 001374                   BNE 1$              ;:HERE
1774 024224 005700                   TST R0              ;:IS THIS THE MASTER?
1775 024226 001002                   BNE 3$              ;:BRANCH IF NO
1776 024230 104401 041420          TYPE ,TM15          ;:ENTERING SECTION 2''
1777 024234                   3$:
1778 024234 052777 100000 172560    BIS #BIT15,@ACR      ;INITIALIZE IIST
1779 024242 016006 014200          MOV $$STP(R0), SP   ;SET THE STACK
1780 024246 106237 017020          2$: ASRB S2L1          ;:TRY TO ENTER SECTION 2 INITIALIZATION
1781 024252 103375                   BCC 2$
1782 024254 012737 034220 000024    MOV #POWER,@#24     ;:SET NEW POWER FAIL HANDLER
1783 024262 012737 000340 000026    MOV #340,@#26
1784 024270 017705 172526          MOV @ACR, R5        ;COPY ACR
1785 024274 072527 177770          ASH #-10, R5        ;GET THE ID
1786 024300 010560 014240          MOV R5, $REGO(R0)  ;IDENTIFY CPU FOR ERROR TYPE-OUT
1787 024304 005002                   CLR R2              ;RESET FOR COUNT
1788 024306 026205 014226          65$: CMP $CPUID(R2),R5  ;SID MATCH?
1789 024312 001404                   BEQ 64$
1790 024314 005722                   TST (R2)+           ;INCREMENT R2 BY 2
1791 024316 020227 000010          CMP R2,#10
1792 024322 002771                   BLT 65$
1793 024324 010200          64$: MOV R2,R0          ;MOV LOGICAL ID TO 2ND OPERAND
1794 024326 010001          MOV R0, R1          ;SET UP R1
1795 024330 006201          ASR R1
1796 024332 012760 034412 014662    MOV #SPWRDN, PWRTAB(R0) ;SET UP FOR POWER DOWN
1797 024340 012760 024634 014702  SIZMBS: MOV #NORP,ERRTAB(R0) ;:SET UP CPU ERROR VECTOR IN CASE
1798                                     ;:THERE'S NO RPO/5/6
1799 024346 052737 000040 176710    BIS #BIT5,@RPCS2    ;:INIT. RP CONTROLLER,IF THERE.
1800 024354 012760 040362 014702    MOV #CPUER,ERRTAB(R0) ;:RESET ERROR VECTOR
1801 024362 005002                   CLR R2              ;:RESET COUNTER
1802 024364 010237 176710          RPSRC: MOV R2,@RPCS2 ;:SET DRIVE # IN CS REG.
1803 024370 032737 040000 176712    BIT #BIT14,@RPPDS  ;:IS THE DRIVE UP?
1804 024376 001024                   BNE NXTDRV          ;:BRANCH IF IT ISN'T
1805
1806 024400 032737 001000 176712    BIT #BIT9,@RPPDS   ;:IS THE PGM BIT SET FOR THIS DRIVE
1807 024406 001403                   BEQ 1$
1808 024410 005260 016742          INC RPPGM(R0)      ;:YES, FLAG THE CONDITION
1809 024414 000415                   BR NXTDRV           ;:AND, SEARCH FOR ANOTHER DRIVE
1810 024416 032737 000400 176712  1$: BIT #BIT8,@RPPDS ;:IS THIS PORT IN CONTROL?
1811 024424 001411                   BEQ NXTDRV          ;:NO, LOOK FOR ANOTHER
1812 024426 005060 014632          CLR MBDSW(R0)      ;:CLEAR MASSBUSS DEVICE SELECTION
1813 024432 013703 176710          MOV @RPCS2,R3      ;:COPY CS2
1814 024436 042703 177770          BIC #177770,R3     ;:GET RID OF OTHER INFO
1815 024442 110360 014632          MOV R3,MBDSW(R0)   ;:WRITE DRIVE ID INTO SELECTION W
1816 024446 000454                   BR SIZEND           ;:DEVICE HAS BEEN FOUND.
1817 024450 005202          NXTDRV: INC R2     ;:NEXT DRIVE
1818 024452 020227 000010          CMP R2,#10         ;:ALL DRIVES TESTED?
1819 024456 103742                   BLO RPSRC           ;:NO, TEST SOME MORE.
1820 024460 005760 016742          TST RPPGM(R0)      ;:ANY PROGRAMMABLE DRIVES?
1821 024464 001011                   BNE A               ;:YES.

```

```

1822 024466 104401 041533 NORH70: TYPE ,TM101 ;:'NO MASSBUS DEVICE AVAILABLE ON CPU #'
1823 024472 016046 014226 MOV $CPUID(R0),-(SP) ;:SAVE $CPUID(R0) FOR TYPEOUT
1824 024476 104405 TYPDS ;:GO TYPE--DECIMAL ASCII WITH SIGN
1825 024500 012760 001400 014632 MOV #1400,MBDSW(R0) ;:SET CODE FOR NO DEVICE
1826 024506 000434 BR SIZEND ;:EXIT SECTION 2 INITIALIZATION
1827 024510 005002 A: CLR R2 ;:RESET COUNTER
1828 024512 010237 176710 10$: MOV R2,@#RPCS2 ;:ACCESS DRIVE.
1829 024516 032737 001000 176712 BIT #BIT9,@#RPDS ;:PGM BIT SET?
1830 024524 001005 BNE 15$ ;:YES, FOUND ONE
1831 024526 005202 INC R2 ;:NO, NEXT DRIVE
1832 024530 020227 000010 CMP R2,#10 ;:ALL DRIVE TESTED
1833 024534 103766 BLO 10$ ;:NO.
1834 024536 000000 HALT ;:YES.
1835 024540 110260 014632 15$: MOVB R2,MBDSW(R0) ;:SET DRIVE #
1836 024544 052760 001000 014632 BIS #BIT9,MBDSW(R0) ;:SET PGMBIT
1837 024552 104401 043535 TYPE ,SPGM1 ;:TYPE SHARED DRIVE WARNING MSG
1838 024556 010246 MOV R2, -(SP)
1839 024560 104405 TYPDS
1840 024562 104401 043563 TYPE ,SPGM2
1841 024566 016046 014226 MOV $CPUID(R0), -(SP)
1842 024572 104405 TYPDS
1843 024574 104401 043577 TYPE ,SPGM3
1844 024600 012737 000001 017020 SIZEND: MOV #1,S2L1 ;:ALLOW ENTRY INTO SEC. 2
1845 024606 005237 016720 INC S2LOG2 ;:LOG OUT OF SECTION 2 INITIALIZATION
1846 024612 023737 016766 016720 1$: CMP CPUACT,S2LOG2 ;:WAIT FOR ALL THE CPUS TO GET HERE
1847 024620 001374 BNE 1$
1848 024622 012777 040334 172176 MOV #ISTDIS,@ISTVEC ;:POINT TO DISPATCHER
1849 024630 000137 024644 JMP TST17 ;:START THE TEST
1850
1851 024634 000240 NORP: NOP ;:THERE IS NO RP CONTROLLER
1852 024636 012716 024466 MOV #NORH70,(SP) ;:SET FOR TEST ENTRY RETURN
1853 024642 000002 RTI ;:RETURN
1854
1855
1856
1857
1858
  
```

```

1859
1860
1861
1862 024644
1863 024644 012777 000017 167316
1864
1865
1866
1867 024652 016006 014200
1868 024656 052777 100000 172136
1869 024664 106277 000122 70$:
1870 024670 103375
1871 024672 027737 000110 016766
1872
1873 024700 001021
1874 024702 013702 016766
1875 024706 005302
1876 024710 006302
1877 024712 027702 000072
1878 024716 001005
1879 024720 012777 000001 000064
1880 024726 000137 025362
1881 024732 062777 000002 000050 64$:
1882 024740 005077 000042
1883 024744 005277 000036 65$:
1884 024750 005037 014714
1885 024754 020077 000030
1886 024760 001005
1887 024762 012777 000001 000022
1888 024770 000137 025014
1889 024774 012777 000001 000010 66$:
1890 025002 000137 025136
1891
1892 025006 016722 67$:
1893 025010 016724 68$:
1894 025012 016776 69$:
1895
1896 025014 112761 000017 014002 TS17A:
1897 025022 010037 017054
1898 025026 005700
1899 025030 001007
1900 025032 104401 041476
1901 025036 005046
1902 025040 116116 014002
1903 025044 104403
1904 025046 000002
1905 025050 5$:
1906 025050 104401 041507
1907 025054 016046 014226
1908 025060 104405
1909 025062 104401 014333
1910 025066 012760 014020 014612
1911 025074 012760 025124 014672
1912 025102 005003
1913 025104 005037 014642
1914 025110 012737 177777 014712

:*****
:*TEST 17 CHECK 'BRK' & 'DCF' FLAGS DURING POWERFAIL
:*****
TST17:
MOV #17,@DISPLAY ;SET TEST NUMBER

:***** TS17A-FORK *****
MOV $$STP(R0), SP;SET UP THE STACK
BIS #BIT15,@ACR ;INITIALIZE THE IIST
ASRB @69$ ;ENTER CONTROL FORK
BCC 70$
CMP @67$,CPUACT ;HAVE WE REACHED THE END OF THE
;ROUTING CYCLE?
BNE 65$ ;BRANCH IF NO
MOV CPUACT,R2
DEC R2
ASL R2 ;(CPUACT-1)*2
CMP @68$,R2 ;ARE WE AT THE END OF THE TEST?
BNE 64$ ;BRANCH IF NO
MOV #1,@69$ ;EXIT
JMP TST20
ADD #2,@68$ ;INCREMENT 68$ BY 2
CLR @67$ ;CLEAR THE CHECKPOINT COUNTER
INC @67$ ;INCREMENT CHECKPOINT
CLR SYNC.2 ;CLEAR THE LOCK
CMP R0,@68$ ;ROUTE THIS PROCESSOR THROUGH TS17A?
BNE 66$ ;BRANCH IF NO
MOV #1,@69$ ;CLEAR LOCK
JMP TS17A ;JUMP TO BRANCH TS17A
MOV #1,@69$ ;CLEAR LOCK
JMP TS17B ;JUMP TO TS17B
:*****
C1
C2
C3

TS17A:
MOVB #17,$STSTM(R1) ;SET UP THE TEST NUMBER
MOV R0,PUT ;SET PROCESSOR UNDER TEST
TST R0 ;IS THIS THE MASTER?
BNE 5$ ;BRANCH IF NO
TYPE ,TM77 ;'TEST'
CLR -(SP)
MOVB $STSTM(R1),(SP) ;GET THE TEST NO.
TYPOS
.WORD 2 ;TYPE 2 DIGITS, NO LEADING 0
5$:
TYPE ,TM100 ;'POWER FAIL CPU #'
MOV $(CPUID(R0),-(SP) ;SAVE $(CPUID(R0) FOR TYPEOUT
TYPDS ;GO TYPE--DECIMAL ASCII WITH SIGN
TYPE ,$CRLF
MOV #SSU!TI!NCX,PFFT(R0) ;SEND SIG. ON UP, TIME, DON'T SAVE MM
MOV #BAD,IISTAB(R0) ;SET UP IIST VECTOR FOR THIS CPU.
CLR R3 ;RETURN AFTER THE WAIT ON POWER UP
CLR SIGNAL ;CLEAR THE POWER UP SIGNAL
MOV -1, SYNC.1 ;UNLOCK THE OTHER CPUS

```

```

1915 025116 000001          WAIT          ;WAIT FOR THE POWER TO FAIL.
1916 025120 000137 024644  JMP          TST17          ;GO TO CONTROL FORK
1917
1918
1919 025124 104025          BAD:  ERROR 25          ;UNEXPECTED CPU INTERRUPT
1920 025126 000000          HALT
1921 025130 012716 024644  MOV          #TST17, (SP)    ;CONTINUE TESTING
1922 025134 000002          RTI
1923
1924 025136 112761 000017 014002 TS17B:  MOVB      #17,      $TSTNM(R1)    ;SET UP THE TEST NUMBER
1925 025144 106237 014712  ASRB      SYNC.1          ;WAIT FOR P.U.T. TO SEND SIGNAL
1926 025150 103372          BCC      TS17B          ;LOOP UNTIL SENT
1927 025152 104401 014220  TYPE      , $NULL        ;FLUSH THE TYPE QUEUE
1928 025156 012760 025124 014672  MOV      #BAD,      I$TAB(R0) ;GET SET FOR BAD INTERRUPT
1929 025164 012777 000001 171630  MOV      #PGCS, @ACR      ;ACCESS PGCS REGISTER
1930 025172 052777 000004 171624  BIS      #BIT2, @ADR      ;SET THE INTERRUPT ENABLE BIT
1931
1932 025200 012777 000007 171614  MOV      #DCF, @ACR      ;COPY THE DCF REG.
1933 025206 017705 171612  MOV      @ADR, R5 ;INTO R5
1934 025212 012760 025264 014672  MOV      #STS17, I$TAB(R0) ;SET FOR EXPECTED INTERRUPT
1935 025220 106237 014642  1$:  ASRB      SIGNAL        ;WAIT ON POWER FAIL SIGNAL
1936 025224 103375          BCC      1$
1937 025226 017760 171570 014250  MOV      @ACR, $REG1(R0) ;SAVE THE ACR
1938 025234 012777 000000 171560  MOV      #PGTE, @ACR      ;ACCESS THE PGTE REG.
1939 025242 017760 171556 014260  MOV      @ADR, $REG2(R0) ;SAVE THE PGTE REG.
1940 025250 017760 171550 014270  MOV      @ADR, $REG3(R0) ;SAVE THE PGCS REG.
1941 025256 104020          ERROR 20          ;NO IIST INTERRUPT
1942 025260 000137 024644  JMP          TST17          ;DO IT AGAIN
1943 025264          STS17:
1944 025264 012777 000007 171530  MOV      #DCF, @ACR      ;ACCESS DCF REGISTER
1945 025272 013703 017054  MOV      PUT, R3          ;GET LOGICAL ID INTO R3
1946 025276 016304 014226  MOV      $CPUID(R3), R4   ;COPY IIST ID TO DESTINATION.
1947 025302 012703 000401  MOV      #401, R3        ;MAKE A MASK
1948 025306 072304          ASH      R4, R3          ;BRING IT INTO POSITION
1949 025310 050305          BIS      R3, R5          ;R5 IS WHAT THE DCF REG. SHOULD LOOK LIKE
1950 025312 077301          SOB      R3,             ;DELAY A SHORT WHILE
1951 025314 017702 171504  MOV      @ADR, R2 ;COPY DCF REGISTER
1952 025320 020205          CMP      R2, R5          ;EVERYTHING OK?
1953 025322 001405          BEQ      3$            ;BRANCH IF YES
1954 025324 010260 014250  MOV      R2, $REG1(R0)    ;THE DCF REG.
1955 025330 010560 014260  MOV      R5, $REG2(R0)    ;WHAT IT SHOULD BE
1956 025334 104021          ERROR 21          ;INCORRECT DCF REG. BITS
1957 025336 005060 017004  3$:  CLR      NOPRMP(R0)
1958 025342 104401 044746  TYPE      , TM11          ;INTERRUPT AS EXPECTED
1959 025346 106237 014712  4$:  ASRB      SYNC.1          ;WAIT FOR POWER-UP
1960 025352 103775          BCS      4$
1961 025354 012716 024644  MOV      #TST17, (SP)    ;CONTINUE
1962 025360 000002          RTI
  
```

```

1963      ::*****
1964      :*TEST 20      CHECK POWERFAIL DURING HIGH MEMORY ACTIVITY
1965      :*****
1966 025362 012777 000020 166600  TST20:  MOV      #20,@DISPLAY      ;SET TEST NUMBER
1967      :***** TS20A-FORK *****
1968      MOV      $$STP(R0),      SP;SET UP THE STACK
1969      BIS      #BIT15, @ACR      ;INITIALIZE THE IIST
1970 025370 016006 014200      ASRB     @69$      ;ENTER CONTROL FORK
1971 025374 052777 100000 171420 70$:  BCC      70$
1972 025402 106277 000122      CMP      @67$,CPUACT      ;HAVE WE REACHED THE END OF THE
1973 025406 103375      ;ROUTING CYCLE?
1974 025410 027737 000110 016766      BNE      65$      ;BRANCH IF NO
1975      MOV      CPUACT,R2
1976 025416 001021      DEC      R2
1977 025420 013702 016766      ASL      R2      ;(CPUACT-1)*2
1978 025424 005302      CMP      @68$,R2      ;ARE WE AT THE END OF THE TEST?
1979 025426 006302      BNE      64$      ;BRANCH IF NO
1980 025430 027702 000072      MOV      #1, @69$      ;EXIT
1981 025434 001005      JMP      TST21
1982 025436 012777 000001 000064 64$:  ADD      #2, @68$      ;INCREMENT 68$ BY 2
1983 025444 000137 025704      CLR      @67$      ;CLEAR THE CHECKPOINT COUNTER
1984 025450 062777 000002 000050 65$:  INC      @67$      ;INCREMENT CHECKPOINT
1985 025456 005077 000042      CLR      SYNC.2      ;CLEAR THE LOCK
1986 025462 005277 000036      CMP      R0,@68$      ;ROUTE THIS PROCESSOR THROUGH TS20A?
1987 025466 005037 014714      BNE      66$      ;BRANCH IF NO
1988 025472 020077 000030      MOV      #1,@69$      ;CLEAR LOCK
1989 025476 001005      JMP      TS20A      ;JUMP TO BRANCH TS20A
1990 025500 012777 000001 000022 66$:  MOV      #1,@69$      ;CLEAR LOCK
1991 025506 000137 025532      JMP      TS20A      ;JUMP TO BRANCH TS20A
1992 025512 012777 000001 000010 67$:  MOV      #1,@69$      ;CLEAR LOCK
1993 025520 000137 025634      JMP      TS20B      ;JUMP TO TS20B
1994      :*****
1995 025524 016726 67$:  D1
1996 025526 016730 68$:  D2
1997 025530 017000 69$:  D3
1998 025532 112761 000020 014002 TS20A: MOVB     #20, $TSTNM(R1)
1999 025540 010037 017054      MOV      R0,PUT      ;SET PROCESSOR UNDER TEST
2000 025544 005700      TST      R0      ;IS THIS THE MASTER?
2001 025546 001007      BNE      5$      ;BRANCH IF NO
2002 025550 104401 041476      TYPE     ,TM77      ;'TEST'
2003 025554 005046      CLR      -(SP)
2004 025556 116116 014002      MOVB     $TSTNM(R1),(SP) ;GET THE TEST NO.
2005 025562 104403      TYPOS
2006 025564 000002      .WORD   2      ;TYPE 2 DIGITS, NO LEADING 0
2007 025566 5$:  TYPE     ,TM100      ;'POWERFAIL CPU # '
2008 025566 104401 041507      MOV      $CPUID(R0),-(SP) ;SAVE $CPUID(R0) FOR TYPEOUT
2009 025572 016046 014226      TYPDS   ;GO TYPE--DECIMAL ASCII WITH SIGN
2010 025576 104405      TYPE     ,$CRLF
2011 025600 104401 014333      MOV      #SSU:TI.NCX,PFFT(R0) ;SEND SIGNAL ON UP,TIME,DON'T SAVE NN
2012 025604 012760 014020 014612      CLR      R3      ;SET FOR RTI RETURN
2013 025612 005003      CLR      SIGNAL      ;CLEAR THE POWER-UP SIGNAL
2014 025614 005037 014642      MOV      #-1, SYNC.1 ;UNLOCK THE OTHER CPUS
2015 025620 012737 177777 014712      WAIT
2016 025626 000001      ;WAIT FOR THE POWER TO FAIL
2017 025630 000137 025362      JMP      TST20
2018

```

2019	025634	112761	000020	014002	TS20B:	MOVB	#20,	\$TSTNM(R1);	SET UP THE TEST NUMBER
2020	025642	106237	014712			ASRB	SYNC.1		;WAIT FOR SYNC. SIGNAL
2021	025646	103372				BCC	TS20B		
2022	025650	104401	014220			TYPE	, \$NULL		;FLUSH THE TYPE QUEUE
2023	025654	012705	002000		1\$:	MOV	#2000,R5		;INITIALIZE COUNTER
2024	025660	011010			2\$:	MOV	(R0),(R0)		
2025	025662	011010				MOV	(R0),(R0)		
2026	025664	011010				MOV	(R0),(R0)		
2027	025666	011010				MOV	(R0),(R0)		
2028	025670	077505				SOB	R5,2\$		
2029	025672	106237	014642			ASRB	SIGNAL		;SIGNAL RECEIVED?
2030	025676	103366				BCC	1\$		;NO,CONTINUE WITH CONTENSION
2031	025700	000137	025362			JMP	TST20		



```

2032
2033
2034
2035 025704
2036 025704 012777 000021 166256
2037
2038
2039 025712 016006 014200
2040 025716 052777 100000 171076
2041 025724 106277 000122 70$:
2042 025730 103375
2043 025732 027737 000110 016766
2044
2045 025740 001021
2046 025742 013702 016766
2047 025746 005302
2048 025750 006302
2049 025752 027702 000072
2050 025756 001005
2051 025760 012777 000001 000064
2052 025766 000137 026632
2053 025772 062777 000002 000050 64$:
2054 026000 005077 000042
2055 026004 005277 000036 65$:
2056 026010 005037 014714
2057 026014 020077 000030
2058 026020 001005
2059 026022 012777 000001 000022
2060 026030 000137 026054
2061 026034 012777 000001 000010 66$:
2062 026042 000137 026434
2063
2064 026046 016732 67$:
2065 026050 016734 68$:
2066 026052 017002 69$:
2067 026054 112761 000021 014002 TS21A:
2068 026062 010037 017054
2069 026066 023737 016732 016766 4$:
2070 026074 001374
2071 026076 005700
2072 026100 001007
2073 026102 104401 041476
2074 026106 005046
2075 026110 116116 014002
2076 026114 104403
2077 026116 000002
2078 026120 5$:
2079 026120 013702 016766
2080 026124 006302
2081 026126 005005
2082 026130 020205 1$:
2083 026132 001407
2084 026134 022765 001400 014632
2085 026142 001020
2086 026144 062705 000002
2087 026150 000767

:*****
:*TEST 21 CHECK POWERFAIL SEQUENCE DURING MASSBUS XFER
:*****
TST21:
MOV #21,@DISPLAY ;SET TEST NUMBER
:***** TS21A-FORK *****
MOV $$STP(R0), SP;SET UP THE STACK
BIS #BIT15,@ACR ;INITIALIZE THE IIST
ASRB @69$ ;ENTER CONTRC. ORK
BCC 70$
CMP @67$,CPUACT ;HAVE WE REACHED THE END OF THE
;ROUTING CYCLE?
BNE 65$ ;BRANCH IF NO
MOV CPUACT,R2
DEC R2
ASL R2 ;(CPUACT-1)*2
CMP @68$,R2 ;ARE WE AT THE END OF THE TEST?
BNE 64$ ;BRANCH IF NO
MOV #1,@69$ ;EXIT
JMP TS22
ADD #2,@68$ ;INCREMENT 68$ BY 2
CLR @67$ ;CLEAR THE CHECKPOINT COUNTER
INC @67$ ;INCREMENT CHECKPOINT
CLR SYNC.2 ;CLEAR THE LOCK
CMP R0,@68$ ;ROUTE THIS PROCESSOR THROUGH TS21A?
BNE 66$ ;BRANCH IF NO
MOV #1,@69$ ;CLEAR LOCK
JMP TS21A ;JUMP TO BRANCH TS21A
MOV #1,@69$ ;CLEAR LOCK
JMP TS21B ;JUMP TO TS21B
:*****
E1
E2
E3
MOV #21,$STSTM(R1)
MOV R0,PUT ;SET PROCESSOR UNDER TEST
CMP E1,CPUACT ;LET THE OTHER CPUS CATCH UP
BNE 4$
TST R0 ;IS THIS THE MASTER?
BNE 5$ ;BRANCH IF NO
TYPE ,TM77 ;'TEST'
CLR -(SP)
MOVB $STSTM(R1),(SP) ;GET THE TEST NO.
TYPOS
.WORD 2 ;TYPE 2 DIGITS, NO LEADING 0
MOV CPUACT,R2 ;CHECK FOR MASSBUS DEVICES ON OTHER CPUS
ASL R2
CLR R5
CMP R2,R5
BEQ 2$
CMP #1400,MBDSW(R5)
BNE 3$
ADD #2,R5
BR 1$
  
```

M 5

MAINDEC-11-CEKGB-B PDP-11/70,74 SYSTEM POWER FAIL MACY11 30A(1052) 06-JUN-79 09:12 PAGE 50  
 CEKGBB.P11 05-JUN-79 09:14 T21 CHECK POWERFAIL SEQUENCE DURING MASSBUS XFER SEQ 0064

```

2088 026152 104401 043732      2$:  TYPE      NODEV      ;THERE ARE NO DEVICES TO TEST THIS CPU
2089 026156 016046 014226      MOV      $CPUID(R0),-(SP) ;:SAVE $CPUID(R0) FOR TYPEOUT
2090 026162 104405      TYPDS    ;:GO TYPE--DECIMAL ASCII WITH SIGN
2091 026164 104401 014333      TYPE      , $CRLF
2092 026170 104401 041604      TYPE      , TM102      ;'PROCEEDING TO NEXT CPU'
2093 026174 012737 177777 014714      MOV      #-1, SYNC.2
2094 026202 000640      BR      TST21      ;BRANCH TO START OF TEST
2095 026204 020005      3$:  CMP      R0, R5
2096 026206 001003      BNE     P21      ;BRANCH IF THERE IS A DEVICE ON ANOTHER CPU
2097 026210 062705 000002      ADD     #2, R5      ;THE DEVICE IS ON THIS CPU
2098 026214 000745      BR      1$
2099 026216 104401 041507      P21:  TYPE      , TM100      ;'POWER FAIL CPU #'
2100 026222 016046 014226      MOV      $CPUID(R0),-(SP) ;:SAVE $CPUID(R0) FOR TYPEOUT
2101 026226 104405      TYPDS    ;:GO TYPE--DECIMAL ASCII WITH SIGN
2102 026230 104401 014333      TYPE      , $CRLF
2103 026234 012760 014020 014612      MOV     #SSU.TI!NCX,PFFT(R0) ;SEND SIGNAL ON UP TIME, DON'T SAVE NN
2104 026242 012737 177777 014712      MOV     #-1, SYNC.1 ;UNLOCK THE OTHER CPU'S
2105 026250 005037 014642      CLR     SIGNAL      ;CLEAR THE POWER-UP SIGNAL
2106 026254 005003      CLR     R3          ;COME UP VIA RTI
2107 026256 022760 001400 014632      CMP     #1400,MBDSW(R0) ;DOES THIS CPU HAVE A MASSBUS DEVICE?
2108 026264 001006      BNE     1$          ;BRANCH IF YES
2109 026266 000001      WAIT
2110 026270 012737 177777 014714      MOV     #-1, SYNC.2 ;UNLOCK CPUS IF ANY ARE LOCKED
2111 026276 000137 025704      JMP     TST21      ;GO TO CONTROL FORK
2112 026302 016004 017034      1$:  MOV     BFADR(R0),R4 ;PUT ADDRESS OF BUFFER IN R4
2113 026306 012737 000070 176700      MOV     #70, @#RPCS1 ;DO A READ
2114 026314 004737 033274      JSR     PC,MBUSR   ;READ A RECORD
2115 026320 005060 014650      CLR     CKSUM(R0)  ;CLEAR CHECKSUM LOCATION
2116 026324 012702 004000      MOV     #4000,R2   ;INITIALIZE A COUNTER
2117 026330 016004 017034      MOV     BFADR(R0),R4 ;GET BUFFER POINTER
2118 026334 062460 014650      2$:  ADD     (R4)+,CKSUM(R0) ;PERFORM
2119 026340 005560 014650      ADC     CKSUM(R0)  ;CHECKSUM
2120 026344 077205      SOB     R2,2$     ;LOOP
2121 026346 016004 017034      4$:  MOV     BFADR(R0),R4 ;LOAD BUFFER ADDRESS
2122 026352 012737 000050 176700      MOV     #50, @#RPCS1 ;DO A WRITE CHECK
2123 026360 004737 033274      JSR     PC,MBUSR   ;READ FROM MASS BUS DEVICE
2124
2125 026364 005005      CLR     R5          ;CLEAR R5
2126 026366 012702 004000      MOV     #4000,R2   ;INITIALIZE COUNTER
2127 026372 016004 017034      MOV     BFADR(R0),R4 ;GET POINTER TO BUFFER
2128 026376 062405      5$:  ADD     (R4)+,R5   ;PERFORM
2129 026400 005505      ADC     R5          ;CHECKSUM
2130 026402 077203      SOB     R2,5$     ;
2131 026404 020560 014650      CMP     R5,CKSUM(R0) ;EVERYTHING OK?
2132 026410 001401      BEQ     6$          ;BRANCH IF YES
2133 026412 104023      ERROR   23         ;CHECKSUM IS WRONG
2134 026414 106237 014642      6$:  ASRB   SIGNAL
2135 026420 103352      BCC     4$          ;NO CONTINUE XFERS
2136 026422 012737 177777 014714      MOV     #-1, SYNC.2 ;UNLOCK CPUS IF ANY ARE LOCKED
2137 026430 000137 025704      JMP     TST21      ;GO TO CONTROL FORK
2138 026434 112761 000021 014002 TS21B: MOV     #21, $STNM(R1) ;SET THE TEST NUMBER
2139 026442 022760 001400 014632      CMP     #1400, MBDSW(R0) ;DOES THIS CPU HAVE A MASSBUS DEVICE?
2140 026450 001007      BNE     1$          ;BRANCH IF YES
2141 026452 106237 014714      10$: ASRB   SYNC.2   ;ELSE SET OUT THIS ROUND
2142 026456 103375      BCC     10$
2143 026460 104401 014220      TYPE      , $NULL   ;FLUSH THE TYPE QUEUE

```

```
2144 026464 000137 025704          JMP      TST21          ;JUMP INTO THE CONTROL LOOP
2145 026470          1$:          MOV      BFADR(R0),R4  ;PUT ADDRESS OF BUFFER IN R4
2146 026470 016004 017034          MOV      #70,0#RPCS1  ;DO A READ
2147 026474 012737 000070 176700          JSR      PC,MBUSR     ;READ A RECORD
2148 026502 004737 033274          CLR      CKSUM(R0)    ;CLEAR CHECKSUM LOCATION
2149 026506 005060 014650          MOV      #4000,R3     ;INITIALIZE A COUNTER
2150 026512 012703 004000          MOV      BFADR(R0),R4 ;GET BUFFER POINTER
2151 026516 016004 017034          ADD      (R4)+,CKSUM(R0) ;PERFORM...
2152 026522 062460 014650          ADC      CKSUM(R0)    ;CHECKSUM.
2153 026526 005560 014650          SOB      R3,2$       ;LOOP
2154 026532 077305          ASRB     SYNC.1      ;HOLD UP
2155 026534 106237 014712          BCC      7$
2156 026540 103375          TYPE     , $NULL    ;FLUSH THE QUEUE
2157 026542 104401 014220          MOV      BFADR(R0),R4 ;LOAD BUFFER ADDRESS
2158 026546 016004 017034          MOV      #50,0#RPCS1 ;DO A WRITE CHECK
2159 026552 012737 000050 176700          JSR      PC,MBUSR     ;READ FROM MASS BUS DEVICE
2160 026560 004737 033274          CLR      R5          ;CLEAR R5
2161 026564 005005          MOV      #4000,R3     ;INITIALIZE COUNTER
2162 026566 012703 004000          MOV      BFADR(R0),R4 ;GET POINTER TO BUFFER
2163 026572 016004 017034          ADD      (R4)+,R5    ;PERFORM...
2164 026576 062405          ADC      R5          ;CHECKSUM
2165 026600 005505          SOB      R3,5$
2166 026602 077303          CMP      R5,CKSUM(R0) ;EVERYTHING OK?
2167 026604 020560 014650          BEQ      6$          ;BRANCH IF YES
2168 026610 001401          ERROR   23          ;CHECKSUM IS WRONG
2169 026612 104023          ASRB     SIGNAL
2170 026614 106237 014642          BCC      4$          ;NO CONTINUE XFERS
2171 026620 103352          TYPE     , $NULL
2172 026622 104401 014220          JMP      TST21
2173 026626 000137 025704          ;JUMP INTO CONTROL LOOP
2174
2175
2176
2177
```

```

2178
2179
2180
2181 026632
2182 026632 012777 000022 165330
2183
2184 026640 112761 000022 014002
2185 026646 106237 016770
2186 026652 103375
2187 026654 005237 014542
2188 026660 012737 000001 016770
2189 026666 023737 016766 014542
2190 026674 001374
2191 026676 005037 014540
2192 026702 005037 177776
2193 026706 020027 000000
2194 026712 001001
2195 026714 000474
2196
2197 026716 052777 100000 170076
2198 026724 012777 000022 165236
2199 026732 016006 014200
2200 026736 005060 014612
2201 026742 012760 040362 014702
2202 026750 012703 027062
2203 026754 005737 014540
2204 026760 001404
2205 026762 005037 177572
2206 026766 000137 027654
2207 026772 005737 014534
2208 026776 001421
2209 027000 004737 032340
2210 027004 063737 014550 172340
2211 027012 063737 014550 172342
2212 027020 063737 014550 172344
2213 027026 052737 000001 177572
2214 027034 005037 014534
2215 027040 000726
2216 027042 005737 014536
2217 027046 001723
2218 027050 005037 177572
2219 027054 005037 014536
2220 027060 000716
2221
2222 027062 005737 014522
2223 027066 001002
2224 027070 104001
2225 027072 000711
2226 027074 005060 017004
2227 027100 104401 041635
2228 027104 000704
2229
2230
2231
2232 027106
2233 027106 005700

```

```

*****
*TEST 22 CHECK AC POWERFAIL ON MEM BOXES, PORTS DISABLED
*****
TST22:
MOV #22,@DISPLAY ;SET TEST NUMBER
MOVB #22,$STNM(R1) ;SET THE TEST NUMBER
ASRB SYNC.3 ;CONTROL THE ENTRY
BCC 2$
INC ENTR22 ;INCREMENT ENTER FLAG
MOV #1, SYNC.3 ;ALLOW THE OTHERS IN
CMP CPUACT, ENTR22 ;ARE ALL CPUS HERE?
BNE 1$ ;NOT YET
CLR EXIT ;CLEAR THE EXIT FLAG
CLR PSW ;SET KERNAL MODE
CMP R0, #0 ;IS THIS THE MASTER?
BNE TS22B ;BRANCH IF NO
BR TS22A ;THIS IS THE MASTER

TS22B:
BIS #BIT15,@ACR ;INITIALIZE THE IIST
MOV #22,@DISPLAY ;SET TEST NUMBER
MOV $$STP(R0), SP ;INITIALIZE THE STACK
CLR PFFT(R0) ;SPECIFY THE POWER FAIL
MOV #CPUER, ERRTAB(R0) ;SET FOR UNEXPECTED TRAPS TO 4
MOV #100$, R3 ;SET FOR POWER FAIL RETURN
TST EXIT ;FINISHED WITH THIS TEST?
BEQ 1$ ;BRANCH IF NO
CLR MMRO ;MAKE SURE MM IS TURNED OFF
JMP TST23 ;GO TO NEXT TEST
1$:
TST RELOUP ;TIME TO RELOCATE?
BEQ 2$ ;BRANCH IF NO
JSR PC, SETMM ;GET READY FOR RELOCATION
ADD HIBOX, KIPAR0
ADD HIBOX, KIPAR1
ADD HIBOX, KIPAR2
BIS #1, MMRO ;SLAVE IS NOW IN HIGH CORE
CLR RELOUP ;CLEAR RELOCATION FLAG
BR TS22B ;CONTINUE TESTING
2$:
TST RELODN ;TIME TO RELOCATE?
BEQ TS22B ;BRANCH IF NO
CLR MMRO ;RETURN TO LOW CORE
CLR RELODN ;CLEAR THE FLAG
BR TS22B ;CONTINUE

100$:
TST PWRFL ;SHOULD WE BE HERE?
BNE 101$ ;BRANCH IF YES
ERROR 1 ;UNEXPECTED CPU POWER FAIL
BR TS22B ;CONTINUE TESTING
101$:
CLR NOPRMP(R0) ;WANT TO IDENTIFY THE CPU
TYPE ,TM103 ;EXPECTED CPU POWER FAIL
BR TS22B ;CONTINUE TESTING

TS22A:
TST R0 ;IS THIS THE MASTER?

```

```

2234 027110 001007      BNE      5$      ;BRANCH IF NO
2235 027112 104401 041476  TYPE      ,TM77      ;'TEST'
2236 027116 005046      CLR      -(SP)
2237 027120 116116 014002  MOV      $TSTNM(R1),(SP) ;GET THE TEST NO.
2238 027124 104403      TYPOS
2239 027126 000002      .WORD      2      ;TYPE 2 DIGITS, NO LEADING 0
2240 027130
2241 027130 012737 000000 014522 5$:      MOV      #0,      PWRFL      ;SPECIFY WHETHER OR NOT TO EXPECT CPU POWER FAIL
2242 027136 012737 000000 014526      MOV      #0,      BOOT      ;SPECIFY WHETHER OR NOT TO EXPECT CPU BOOT AND I
2243 027144 004737 032076      JSR      PC,      MEMSIZ      ;FIND ALL THE MEM BOXES
2244 027150 005737 014540      TST      EXIT      ;WAS ONLY ONE MEM BOX FOUND?
2245 027154 001402      BEQ      1$      ;BRANCH IF NO
2246 027156 000137 027654      JMP      TST23      ;WE CAN'T DO THIS TEST
2247 027162 012702 000016      1$:      MOV      #16,      R2      ;POINT TO BOX #7
2248 027166 052777 100000 167626 2$:      BIS      #BIT15, @ACR      ;INITIALIZE THE IIST
2249 027174 012777 000022 164766      MOV      #22, @DISPLAY      ;SET THE TEST NUMBER
2250 027202 016006 014200      MOV      $$STP(R0),      SP      ;INIALIZE THE STACK
2251 027206 005060 014612      CLR      PFFT(R0)      ;SPECIFY THE POWER FAIL
2252 027212 012760 040362 0i4702      MOV      #CPUER, ERRTAB(R0) ;SET FOR UNEXPECTED TRAPS TO 4
2253 027220 005702      TST      R2      ;DID WE TEST ALL THE BOXES
2254 027222 002012      BGE      3$      ;BRANCH IF NO
2255 027224 012737 000112 000110      MOV      #112, @#110      ;RESTORE LOC 110
2256 027232 005037 000000      CLR      @#0      ;RESTORE LOC 0
2257 027236 012737 000001 014540      MOV      #1,      EXIT      ;SIGNAL THE SLAVES TO EXIT
2258 027244 000137 027654      JMP      TST23      ;GO TO THE NEXT TEST
2259 027250 005762 014502      3$:      TST      START(R2)      ;WHAT DO WE KNOW ABOUT THIS BOX?
2260 027254 003037      BGT      10$      ;BRANCH IF NOT THE BASE BOX
2261 027256 001403      BEQ      4$      ;BRANCH IF ITS THE BASE BOX
2262 027260 162702 000002      SUB      #2,      R2      ;THERE WAS NO BOX-POINT TO THE NEXT LOWER BOX
2263 027264 000740      BR      2$      ;CONTINUE
2264 027266 022737 000001 014646 4$:      CMP      #1,      BOXNUM      ;WAS THERE ONLY ONE MEM BOX?
2265 027274 002027      BGE      11$      ;BRANCH IF YES
2266 027276 005737 014526      TST      BOOT      ;IS THIS THE DC TEST?
2267 027302 001141      BNE      103$      ;BRANCH IF YES
2268 027304 004737 032576      JSR      PC,      RELOHI      ;TO TEST THE BASE BOX,
2269      ;RELOCATE THE PROGRAM FIRST TO THE NEXT HIGHER B
2270 027310 012737 000001 014532      MOV      #1,      HICORE      ;TURN MM ON ON POWER-UP
2271 027316 012737 000001 014534      MOV      #1,      RELOUP      ;SIGNAL SLAVES TO RELOCATE
2272 027324 063737 014550 172340      ADD      HIBOX, KIPAR0      ;GET READY TO GO TO HIGH CORE
2273 027332 063737 014550 172342      ADD      HIBOX, KIPAR1
2274 027340 063737 014550 172344      ADD      HIBOX, KIPAR2
2275 027346 052737 000001 177572      BIS      #1,      MMRO      ;WE ARE NOW IN HIGH CORE
2276 027354
2277 027354 005037 014530      10$:      CLR      PATCHK      ;SET TO WRITE PATTERN
2278 027360 004737 032434      11$:      JSR      PC,      PATTRN      ;WRITE THE PATTERN
2279 027364 004737 032322      JSR      PC,      BUFCLR      ;CLEAR THE KEYBOARD BUFFER
2280 027370 104401 042317      TYPE      ,TM106      ;TELL THE OPERATOR TO POWER FAIL THE MEMORY BOX
2281 027374 006202      ASR      R2
2282 027376 010246      MOV      R2,      -(SP)
2283 027400 104405      TYPDS
2284 027402 006302      ASL      R2
2285 027404 104401 043011      TYPE      ,TM108      ;SPECIFY THE CONDITIONS
2286 027410 012703 027552      MOV      #100$,      R3      ;SET UP THE POWER FAIL RETURN
2287 027414 005737 014526      TST      BOOT      ;IS THIS THE DC TEST?
2288 027420 001414      BEQ      12$      ;BRANCH IF NO
2289 027422 012737 020000 000000 13$:      MOV      #20000, @#0      ;MAKE BOOTING SLAVE SP=20000
  
```

```

2290 027430 005237 000110      INC      @#110      ;HANG THE SLAVES BOOT
2291 027434 105777 164550      TSTB     @STKS     ;IS CHARACTER IN BUFFER?
2292 027440 100370                BPL      13$      ;LOOP
2293 027442 012777 032762 167356  MOV      #ENTR, @1STVEC ;SET UP TO INTERRUPT SLAVES
2294 027450 000413                BR       14$      ;CONTINUE
2295 027452                12$:
2296 027452 105777 164532      TSTB     @STKS     ;IS CHARACTER IN THE BUFFER?
2297 027456 100375                BPL      12$      ;LOOP
2298 027460 005737 014522      17$: TST      PWRFL     ;SHOULD THE MASTER HAVE POWER FAILED?
2299 027464 001402                BEQ      18$      ;BRANCH IF NO
2300 027466 104024                ERROR    24      ;FAILURE TO POWER FAIL
2301 027470 000441                BR       102$     ;CONTINUE
2302 027472 104401 047036      18$: TYPE     ,OK
2303 027476 000436                BR       102$
2304 027500 017704 164454      14$: MOV      @SWR, R4      ;GET THE SWITCH VALUES
2305 027504 042704 177760      BIC      #177760, R4      ;SAVE ONLY CPU BITS
2306 027510 012777 000000 167304  MOV      #PGTE, @ACR      ;ACCESS PGTE REG
2307 027516 010477 167302      MOV      R4, @ADR      ;SET INTERRUPT BITS
2308 027522 032737 000001 016766  BIT      #BIT0, CPUACT    ;EVEN OR ODD?
2309 027530 001404                BEQ      15$      ;BRANCH IF EVEN
2310 027532 012777 000001 167264  MOV      #1, @ADR      ;INTERRUPTING AN EVEN NUMBER OF SLAVES
2311 027540 000422                BR       103$
2312 027542 012777 000003 167254  15$: MOV      #3, @ADR      ;INTERRUPTING AN ODD # OF SLAVES
2313 027550 000416                BR
2314
2315 027552 005737 014522      100$: TST      PWRFL     ;DID WE EXPECT POWER FAIL?
2316 027556 001002                BNE      101$     ;BRANCH IF YES
2317 027560 104001                ERROR    1      ;MASTER ERROREOUSLY POWER FAILED
2318 027562 000404                BR       102$     ;CONTINUE
2319 027564 005060 017004      101$: CLR      NOPRMP(R0)    ;ALLOW CPU IDENTIFICATION
2320 027570 104401 041635      TYPE     ,TM103     ;CPU POWER FAIL MSG
2321 027574 012737 000001 014530  102$: MOV      #1, PATCHK    ;SET UP FOR PATTERN CHECK
2322 027602 004737 032434      JSR      PC, PATTRN    ;CHECK THE PATTERN
2323 027606 032737 000001 177572  103$: BIT      #1, MMRO    ;ARE WE IN HIGH CORE?
2324 027614 001411                BEQ      104$     ;BRANCH IF NO
2325 027616 004737 032722      JSR      PC, RELOLO    ;ELSE RELOCATE
2326 027622 012737 000001 014536  MOV      #1, RELODN    ;SIGNAL THE SLAVES
2327 027630 005037 177572      CLR      MMRO         ;WE ARE NOW BACK DOWN IN LOW CORE
2328 027634 005037 014532      CLR      HICORE       ;MAKE SURE MM ON POWER-UP DISABLED
2329 027640 005005                CLR      R5           ;MAKE TS22A DELAY
2330 027642 077501                SOB      R5, R2
2331 027644 162702 000002      SUB      #2, R2
2332 027650 000137 027166      JMP      2$
2333
2334
2335

```

```

2336
2337
2338
2339 027654
2340 027654 012777 000023 164306
2341
2342 027662 112761 000023 014002
2343 027670 106237 016770
2344 027674 103375
2345 027676 005237 014544
2346 027702 012737 000001 016770
2347 027710 023737 016766 014544
2348 027716 001374
2349 027720 005037 014540
2350 027724 005037 177776
2351 027730 020027 000000
2352 027734 001001
2353 027736 000474
2354
2355 027740 052777 100000 167054
2356 027746 012777 000023 164214
2357 027754 016006 014200
2358 027760 005060 014612
2359 027764 012760 040362 014702
2360 027772 012703 030104
2361 027776 005737 014540
2362 030002 001404
2363 030004 005037 177572
2364 030010 000137 030676
2365 030014 005737 014534
2366 030020 001421
2367 030022 004737 032340
2368 030026 063737 014550 172340
2369 030034 063737 014550 172342
2370 030042 063737 014550 172344
2371 030050 052737 000001 177572
2372 030056 005037 014534
2373 030062 000726
2374 030064 005737 014536
2375 030070 001723
2376 030072 005037 177572
2377 030076 005037 014536
2378 030102 000716
2379
2380 030104 005737 014522
2381 030110 001002
2382 030112 104001
2383 030114 000711
2384 030116 005060 017004
2385 030122 104401 041635
2386 030126 000704
2387
2388
2389
2390 030130
2391 030130 005700

```

```

*****
:TEST 23 CHECK AC POWERFAIL ON MEM BOXES, PORTS ENABLED
*****
TST23:
MOV #23,@DISPLAY ;SET TEST NUMBER
MOV #23,$STNM(R1) ;SET THE TEST NUMBER
ASRB SYNC.3 ;CONTROL THE ENTRY
BCC 2$
INC ENTR23 ;INCREMENT ENTER FLAG
MOV #1, SYNC.3 ;ALLOW THE OTHERS IN
CMP CPUACT, ENTR23 ;ARE ALL CPUS HERE?
BNE 1$ ;NOT YET
CLR EXIT ;CLEAR THE EXIT FLAG
CLR PSW ;SET KERNAL MODE
CMP R0, #0 ;IS THIS THE MASTER?
BNE TS23B ;BRANCH IF NO
BR TS23A ;THIS IS THE MASTER

TS23B:
BIS #BIT15,@ACR ;INITIALIZE THE IIST
MOV #23,@DISPLAY ;SET TEST NUMBER
MOV $$STP(R0), SP ;INITIALIZE THE STACK
CLR PFFT(R0) ;SPECIFY THE POWER FAIL
MOV #CPUER, ERRTAB(R0) ;SET FOR UNEXPECTED TRAPS TO 4
MOV #100$, R3 ;SET FOR POWER FAIL RETURN
EXIT ;FINISHED WITH THIS TEST?
BEQ 1$ ;BRANCH IF NO
CLR MMRO ;MAKE SURE MM IS TURNED OFF
JMP TST24 ;GO TO NEXT TEST
1$:
TST RELOUP ;TIME TO RELOCATE?
BEQ 2$ ;BRANCH IF NO
JSR PC, SETMM ;GET READY FOR RELOCATION
ADD HIBOX, KIPAR0
ADD HIBOX, KIPAR1
ADD HIBOX, KIPAR2
BIS #1, MMRO ;SLAVE IS NOW IN HIGH CORE
CLR RELOUP ;CLEAR RELOCATION FLAG
BR TS23B ;CONTINUE TESTING
2$:
TST RELODN ;TIME TO RELOCATE?
BEQ TS23B ;BRANCH IF NO
CLR MMRO ;RETURN TO LOW CORE
CLR RELODN ;CLEAR THE FLAG
BR TS23B ;CONTINUE

100$:
TST PWRFL ;SHOULD WE BE HERE?
BNE 101$ ;BRANCH IF YES
ERROR 1 ;UNEXPECTED CPU POWER FAIL
BR TS23B ;CONTINUE TESTING
101$:
CLR NOPRMP(R0) ;WANT TO IDENTIFY THE CPU
TYPE ,TM103 ;EXPECTED CPU POWER FAIL
BR TS23B ;CONTINUE TESTING

TS23A:
TST R0 ;IS THIS THE MASTER?

```

```

2392 030132 001007          BNE      5$          ;BRANCH IF NO
2393 030134 104401 041476  TYPE      ,TM77      ;'TEST'
2394 030140 005046          CLR      -(SP)
2395 030142 116116 014002  MOV      $STNM(R1),(SP) ;GET THE TEST NO.
2396 030146 104403          TYPOS
2397 030150 000002          .WORD    2          ;TYPE 2 DIGITS, NO LEADING 0
2398 030152
2399 030152 012737 000001 014522 5$:      MOV      #1,      PWRFL      ;SPECIFY WHETHER OR NOT TO EXPECT CPU POWER FAIL
2400 030160 012737 000000 014526  MOV      #0,      BOOT       ;SPECIFY WHETHER OR NOT TO EXPECT CPU BOOT AND I
2401 030166 004737 032076          JSR      PC,      MEMSIZ     ;FIND ALL THE MEM BOXES
2402 030172 005737 014540          TST      EXIT      ;WAS ONLY ONE MEM BOX FOUND?
2403 030176 001402          BEQ      1$          ;BRANCH IF NO
2404 030200 000137 030676          JMP      TST24      ;WE CAN'T DO THIS TEST
2405 030204 012702 000016          MOV      #16,     R2       ;POINT TO BOX #7
2406 030210 052777 100000 166604 2$:      BIS      #BIT15, @ACR      ;INITIALIZE THE IIST
2407 030216 012777 000023 163744  MOV      #23,     @DISPLAY  ;SET THE TEST NUMBER
2408 030224 016006 014200          MOV      $$STP(R0), SP    ;INIALIZE THE STACK
2409 030230 005060 014612          CLR      PFFT(R0)      ;SPECIFY THE POWER FAIL
2410 030234 012760 040362 014702  MOV      #CPUER,  ERRTAB(R0) ;SET FOR UNEXPECTED TRAPS TO 4
2411 030242 005702          TST      R2          ;DID WE TEST ALL THE BOXES
2412 030244 002012          BGE      3$          ;BRANCH IF NO
2413 030246 012737 000112 000110  MOV      #112,    @#110    ;RESTORE LOC 110
2414 030254 005037 000000          CLR      @#0         ;RESTORE LOC 0
2415 030260 012737 000001 014540  MOV      #1,      EXIT     ;SIGNAL THE SLAVES TO EXIT
2416 030266 000137 030676          JMP      TST24      ;GO TO THE NEXT TEST
2417 030272 005762 014502          3$:      TST      START(R2)     ;WHAT DO WE KNOW ABOUT THIS BOX?
2418 030276 003037          BGT      10$        ;BRANCH IF NOT THE BASE BOX
2419 030300 001403          BEQ      4$          ;BRANCH IF ITS THE BASE BOX
2420 030302 162702 000002          SUB      #2,      R2       ;THERE WAS NO BOX-POINT TO THE NEXT LOWER BOX
2421 030306 000740          BR       2$          ;CONTINUE
2422 030310 022737 000001 014646 4$:      CMP      #1,      BOXNUM   ;WAS THERE ONLY ONE MEM BOX?
2423 030316 002027          BGE      11$        ;BRANCH IF YES
2424 030320 005737 014526          TST      BOOT       ;IS THIS THE DC TEST?
2425 030324 001141          BNE      103$       ;BRANCH IF YES
2426 030326 004737 032576          JSR      PC,      RELOHI   ;TO TEST THE BASE BOX,
2427                                ;RELOCATE THE PROGRAM FIRST TO THE NEXT HIGHER B
2428 030332 012737 000001 014532  MOV      #1,      HICORE   ;TURN MM ON ON POWER-UP
2429 030340 012737 000001 014534  MOV      #1,      RELOUP   ;SIGNAL SLAVES TO RELOCATE
2430 030346 063737 014550 172340  ADD      HIBOX,   KIPARO   ;GET READY TO GO TO HIGH CORE
2431 030354 063737 014550 172342  ADD      HIBOX,   KIPAR1
2432 030362 063737 014550 172344  ADD      HIBOX,   KIPAR2
2433 030370 052737 000001 177572  BIS      #1,      MMRO    ;WE ARE NOW IN HIGH CORE
2434 030376
2435 030376 005037 014530          10$:     CLR      PATCHK      ;SET TO WRITE PATTERN
2436 030402 004737 032434          11$:     JSR      PC,      PATTRN  ;WRITE THE PATTERN
2437 030406 004737 032322          JSR      PC,      BUFCLR  ;CLEAR THE KEYBOARD BUFFER
2438 030412 104401 042317          TYPE      ,TM106      ;TELL THE OPERATOR TO POWER FAIL THE MEMORY BOX
2439 030416 006202          ASR      R2
2440 030420 010246          MOV      R2,      -(SP)
2441 030422 104405          TYPDS
2442 030424 006302          ASL      R2
2443 030426 104401 042363          TYPE      ,TM107      ;SPECIFY THE CONDITIONS
2444 030432 012703 030574          MOV      #100$,   R3     ;SET UP THE POWER FAIL RETURN
2445 030436 005737 014526          TST      BOOT       ;IS THIS THE DC TEST?
2446 030442 001414          BEQ      12$        ;BRANCH IF NO
2447 030444 012737 020000 000000 13$:     MOV      #20000, @#0    ;MAKE BOOTING SLAVE SP=20000
  
```



6 6

MAINDEC-11-CEKGB-B PDP-11/70,74 SYSTEM POWER FAIL MACY11 30A(1052) 06-JUN-79 09:12 PAGE 57  
 CEKGB.P11 05-JUN-79 09:14 T23 CHECK AC POWERFAIL ON MEM BOXES, PORTS ENABLED SEQ 0071

```

2448 030452 005237 000110      INC      @#110      ;HANG THE SLAVES BOOT
2449 030456 105777 163526      TSTB     @STKS     ;IS CHARACTER IN BUFFER?
2450 030462 100370          BPL      13$      ;LOOP
2451 030464 012777 032762 166334      MOV      #ENTR, @ISTVEC ;SET UP TO INTERRUPT SLAVES
2452 030472 000413          BR       14$      ;CONTINUE
2453 030474          12$:
2454 030474 105777 163510      TSTB     @STKS     ;IS CHARACTER IN THE BUFFER?
2455 030500 100375          BPL      12$      ;LOOP
2456 030502 005737 014522      17$: TST      PWRFL     ;SHOULD THE MASTER HAVE POWER FAILED?
2457 030506 001402          BEQ      18$      ;BRANCH IF NO
2458 030510 104024          ERROR    24      ;FAILURE TO POWER FAIL
2459 030512 000441          BR       102$     ;CONTINUE
2460 030514 104401 047036      18$: TYPE     ,OK
2461 030520 000436          BR       102$
2462 030522 017704 163432      14$: MOV      @SWR, R4      ;GET THE SWITCH VALUES
2463 030526 042704 177760          BIC      #177760, R4 ;SAVE ONLY CPU BITS
2464 030532 012777 000000 166262      MOV      #PGTE, @ACR  ;ACCESS PGTE REG
2465 030540 010477 166260      MOV      R4, @ADR   ;SET INTERRUPT BITS
2466 030544 032737 000001 016766      BIT      #BIT0, CPUACT ;EVEN OR ODD?
2467 030552 001404          BEQ      15$      ;BRANCH IF EVEN
2468 030554 012777 000001 166242      MOV      #1, @ADR   ;INTERRUPTING AN EVEN NUMBER OF SLAVES
2469 030562 000422          BR       103$
2470 030564 012777 000003 166232      15$: MOV      #3, @ADR   ;INTERRUPTING AN ODD # OF SLAVES
2471 030572 000416          BR       103$
2472
2473 030574 005737 014522      100$: TST      PWRFL     ;DID WE EXPECT POWER FAIL?
2474 030600 001002          BNE      101$     ;BRANCH IF YES
2475 030602 104001          ERROR    1      ;MASTER ERROREOUSLY POWER FAILED
2476 030604 000404          BR       102$     ;CONTINUE
2477 030606 005060 017004      101$: CLR      NOPRMP(R0) ;ALLOW CPU IDENTIFICATION
2478 030612 104401 041635          TYPE     ,TM103  ;CPU POWER FAIL MSG
2479 030616 012737 000001 014530      102$: MOV      #1, PATCHK ;SET UP FOR PATTERN CHECK
2480 030624 004737 032434          JSR      PC, PATTRN ;CHECK THE PATTERN
2481 030630 032737 000001 177572      103$: BIT      #1, MMRO   ;ARE WE IN HIGH CORE?
2482 030636 001411          BEQ      104$     ;BRANCH IF NO
2483 030640 004737 032722          JSR      PC, RELOLO ;ELSE RELOCATE
2484 030644 012737 000001 014536      MOV      #1, RELODN ;SIGNAL THE SLAVES
2485 030652 005037 177572          CLR      MMRO     ;WE ARE NOW BACK DOWN IN LOW CORE
2486 030656 005037 014532          CLR      HICORE   ;MAKE SURE MM ON POWER-UP DISABLED
2487 030662 005005          104$: CLR      R5      ;MAKE TS23A DELAY
2488 030664 077501          SOB     R5, .
2489 030666 162702 000002      SUB     #2, R2     ;POINT TO NEXT BOX
2490 030672 000137 030210      JMP     2$        ;CONTINUE
2491
2492

```

```

2493      ::*****
2494      ::*TEST 24      CHECK DC POWERFAIL ON MEM BOXES, CPUS BOOT ON POWER UP
2495      ::*****
2496 030676      TST24:
2497 030676 012777 000024 163264      MOV      #24,@DISPLAY      ;SET TEST NUMBER
2498
2499 030704 112761 000024 014002      MOVB     #24, $STNM(R1)      ;SET THE TEST NUMBER
2500 030712 106237 016770      2$: ASRB     SYNC.3          ;CONTROL THE ENTRY
2501 030716 103375
2502 030720 005237 014546      INC     ENTR24          ;INCREMENT ENTER FLAG
2503 030724 012737 000001 016770      MOV     #1, SYNC.3      ;ALLOW THE OTHERS IN
2504 030732 023737 016766 014546      1$: CMP     CPUACT, ENTR24 ;ARE ALL CPUS HERE?
2505 030740 001374      BNE     1$             ;NOT YET
2506 030742 005037 014540      CLR     EXIT           ;CLEAR THE EXIT FLAG
2507 030746 005037 177776      CLR     PSW           ;SET KERNAL MODE
2508 030752 020027 000000      CMP     R0, #0         ;IS THIS THE MASTER?
2509 030756 001001      BNE     TS24B         ;BRANCH IF NO
2510 030760 000474      BR      TS24A         ;THIS IS THE MASTER
2511
2512 030762 052777 100000 166032      TS24B: BIS     #BIT15, @ACR   ;INITIALIZE THE IIST
2513 030770 012777 000024 163172      MOV     #24, @DISPLAY  ;SET TEST NUMBER
2514 030776 016006 014200      MOV     $$STP(R0), SP  ;INITIALIZE THE STACK
2515 031002 005060 014612      CLR     PFFT(R0)      ;SPECIFY THE POWER FAIL
2516 031006 012760 040362 014702      MOV     #CPUER, ERRTAB(R0) ;SET FOR UNEXPECTED TRAPS TO 4
2517 031014 012703 031126      MOV     #100$, R3     ;SET FOR POWER FAIL RETURN
2518 031020 005737 014540      TST     EXIT         ;FINISHED WITH THIS TEST?
2519 031024 001404      BEQ     1$           ;BRANCH IF NO
2520 031026 005037 177572      CLR     MMRO         ;MAKE SURE MM IS TURNED OFF
2521 031032 000137 031720      JMP     TST25        ;GO TO NEXT TEST
2522 031036 005737 014534      1$: TST     RELOUP     ;TIME TO RELOCATE?
2523 031042 001421      BEQ     2$           ;BRANCH IF NO
2524 031044 004737 032340      JSR     PC, SETMM    ;GET READY FOR RELOCATION
2525 031050 063737 014550 172340      ADD     HIBOX, KIPAR0
2526 031056 063737 014550 172342      ADD     HIBOX, KIPAR1
2527 031064 063737 014550 172344      ADD     HIBOX, KIPAR2
2528 031072 052737 000001 177572      BIS     #1, MMRO     ;SLAVE IS NOW IN HIGH CORE
2529 031100 005037 014534      CLR     RELOUP       ;CLEAR RELOCATION FLAG
2530 031104 000726      BR      TS24B        ;CONTINUE TESTING
2531 031106 005737 014536      2$: TST     RELODN     ;TIME TO RELOCATE?
2532 031112 001723      BEQ     TS24B        ;BRANCH IF NO
2533 031114 005037 177572      CLR     MMRO         ;RETURN TO LOW CORE
2534 031120 005037 014536      CLR     RELODN       ;CLEAR THE FLAG
2535 031124 000716      BR      TS24B        ;CONTINUE
2536
2537 031126 005737 014522      100$: TST     PWRFL     ;SHOULD WE BE HERE?
2538 031132 001002      BNE     101$        ;BRANCH IF YES
2539 031134 104001      ERROR   1          ;UNEXPECTED CPU POWER FAIL
2540 031136 000711      BR      TS24B        ;CONTINUE TESTING
2541 031140 005060 017004      101$: CLR     NOPRMP(R0) ;WANT TO IDENTIFY THE CPU
2542 031144 104401 041635      TYPE    ,TM103     ;EXPECTED CPU POWER FAIL
2543 031150 000704      BR      TS24B        ;CONTINUE TESTING
2544
2545
2546
2547 031152      TS24A:
2548 031152 005700      TST     R0           ;IS THIS THE MASTER?

```

```

2549 031154 001007      BNE      5$          ;BRANCH IF NO
2550 031156 104401 041476  TYPE      ,TM77      ;'TEST'
2551 031162 005046      CLR      -(SP)
2552 ^31164 116116 014002  MOVB     $STNM(R1),(SP) ;GET THE TEST NO.
2553 031170 104403      TYPOS
2554 031172 000002      .WORD     2          ;TYPE 2 DIGITS, NO LEADING 0
2555 031174
2556 031174 012737 000000 014522 5$:  MOV      #0,        PWRFL      ;SPECIFY WHETHER OR NOT TO EXPECT CPU POWER FAIL
2557 031202 012737 000001 014526  MOV      #1,        BOOT       ;SPECIFY WHETHER OR NOT TO EXPECT CPU BOOT AND I
2558 031210 004737 032076      JSR      PC,        MEMSIZ     ;FIND ALL THE MEM BOXES
2559 031214 005737 014540      TST     EXIT        ;WAS ONLY ONE MEM BOX FOUND?
2560 031220 001402      BEQ     1$          ;BRANCH IF NO
2561 031222 000137 031720      JMP     TST25       ;WE CAN'T DO THIS TEST
2562 031226 012702 000016      1$:  MOV      #16,       R2        ;POINT TO BOX #7
2563 031232 052777 100000 165562 2$:  BIS      #BIT15, @ACR        ;INITIALIZE THE IIST
2564 031240 012777 000024 162722  MOV      #24,       @DISPLAY   ;SET THE TEST NUMBER
2565 031246 016006 014200      MOV     $$STP(R0),  SP        ;INIALIZE THE STACK
2566 031252 005060 014612      CLR     PFFT(R0)     ;SPECIFY THE POWER FAIL
2567 031256 012760 040362 014702  MOV     #CPUER, ERRTAB(R0)    ;SET FOR UNEXPECTED TRAPS TO 4
2568 031264 005702      TST     R2          ;DID WE TEST ALL THE BOXES
2569 031266 002012      BGE     3$          ;BRANCH IF NO
2570 031270 012737 000112 000110  MOV     #112, @#110        ;RESTORE LOC 110
2571 031276 005037 000000      CLR     @#0         ;RESTORE LOC 0
2572 031302 012737 000001 014540  MOV     #1,        EXIT       ;SIGNAL THE SLAVES TO EXIT
2573 031310 000137 031720      JMP     TST25       ;GO TO THE NEXT TEST
2574 031314 005762 014502      3$:  TST     START(R2)     ;WHAT DO WE KNOW ABOUT THIS BOX?
2575 031320 003037      BGT     10$         ;BRANCH IF NOT THE BASE BOX
2576 031322 001403      BEC     4$          ;BRANCH IF ITS THE BASE BOX
2577 031324 162702 000002      SUB     #2,        R2        ;THERE WAS NO BOX-POINT TO THE NEXT LOWER BOX
2578 031330 000740      BR      2$          ;CONTINUE
2579 031332 022737 000001 014646 4$:  CMP     #1,        BOXNUM     ;WAS THERE ONLY ONE MEM BOX?
2580 031340 002027      BGE     11$         ;BRANCH IF YES
2581 031342 005737 014526      TST     BOOT        ;IS THIS THE DC TEST?
2582 031346 001141      BNE     103$        ;BRANCH IF YES
2583 031350 004737 032576      JSR     PC,        RELOHI     ;TO TEST THE BASE BOX,
2584
2585 031354 012737 000001 014532  MOV     #1,        HICORE     ;RELOCATE THE PROGRAM FIRST TO THE NEXT HIGHER B
2586 031362 012737 000001 014534  MOV     #1,        RELOUP     ;TURN MM ON ON POWER-UP
2587 031370 063737 014550 172340  ADD     HIBOX,     KIPAR0     ;SIGNAL SLAVES TO RELOCATE
2588 031376 063737 014550 172342  ADD     HIBOX,     KIPAR1     ;GET READY TO GO TO HIGH CORE
2589 031404 063737 014550 172344  ADD     HIBOX,     KIPAR2
2590 031412 052737 000001 177572  BIS     #1,        MMRO
2591 031420
2592 031420 005037 014530      10$: CLR     PATCHK     ;SET TO WRITE PATTERN
2593 031424 004737 032434      11$: JSR     PC,        PATTRN    ;WRITE THE PATTERN
2594 031430 004737 032322      JSR     PC,        BUFCLR    ;CLEAR THE KEYBOARD BUFFER
2595 031434 104401 042317      TYPE    ,TM106         ;TELL THE OPERATOR TO POWER FAIL THE MEMORY BOX
2596 031440 006202      ASR     R2
2597 031442 010246      MOV     R2,        -(SP)
2598 031444 104405      TYPDS
2599 031446 006302      ASL     R2
2600 031450 104401 044053      TYPE    ,TM110
2601 031454 012703 031616      MOV     #100$,    R3        ;SPECIFY THE CONDITIONS
2602 031460 005737 014526      TST     BOOT        ;SET UP THE POWER FAIL RETURN
2603 031464 001414      BEQ     12$         ;IS THIS THE DC TEST?
2604 031466 012737 020000 000000 13$: MOV     #20000, @#0        ;BRANCH IF NO
;MAKE BOOTING SLAVE SP 20000

```

```

2605 031474 005237 000110      INC      @#110      ;HANG THE SLAVES BOOT
2606 031500 105777 162504      TSTB    @#TKS      ;IS CHARACTER IN BUFFER?
2607 031504 100370          BPL     13$        ;LOOP
2608 031506 012777 032762 165312  MOV     #ENTR, @ISTVEC ;SET UP TO INTERRUPT SLAVES
2609 031514 000413          BR      14$        ;CONTINUE
2610 031516          12$:
2611 031516 105777 162466      TSTB    @#TKS      ;IS CHARACTER IN THE BUFFER?
2612 031522 100375          BPL     12$        ;LOOP
2613 031524 005737 014522 17$:
2614 031530 001402          TST     PWRFL      ;SHOULD THE MASTER HAVE POWER FAILED?
2615 031532 104024          BEQ     18$        ;BRANCH IF NO
2616 031534 000441          ERROR    24      ;FAILURE TO POWER FAIL
2617 031536 104401 047036 18$:
2618 031542 000436          BR      102$       ;CONTINUE
2619 031544 017704 162410 14$:
2620 031550 042704 177760      MOV     @SWR, R4    ;GET THE SWITCH VALUES
2621 031554 012777 000000 165240  BIC     #177760, R4 ;SAVE ONLY CPU BITS
2622 031562 010477 165236      MOV     #PGTE, @ACR ;ACCESS PGTE REG
2623 031566 032737 000001 016766  MOV     R4, @ADR    ;SET INTERRUPT BITS
2624 031574 001404          BIT     #BIT0, CPUACT ;EVEN OR ODD?
2625 031576 012777 000001 165220  BEQ     15$        ;BRANCH IF EVEN
2626 031604 000422          MOV     #1, @ADR   ;INTERRUPTING AN EVEN NUMBER OF SLAVES
2627 031606 012777 000003 165210  BR      103$       ;
2628 031614 000416          MOV     #3, @ADR   ;INTERRUPTING AN ODD # OF SLAVES
2629
2630 031616 005737 014522 100$:
2631 031622 001002          TST     PWRFL      ;DID WE EXPECT POWER FAIL?
2632 031624 104001          BNE     101$       ;BRANCH IF YES
2633 031626 000404          ERROR    1      ;MASTER ERROREOUSLY POWER FAILED
2634 031630 005060 017004 101$:
2635 031634 104401 041635          BR      102$       ;CONTINUE
2636 031640 012737 000001 014530 102$:
2637 031646 004737 032434          CLR     NOPRMP(R0) ;ALLOW CPU IDENTIFICATION
2638 031652 032737 000001 177572 103$:
2639 031660 001411          TYPE    ,TM103    ;CPU POWER FAIL MSG
2640 031662 004737 032722          MOV     #1, PATCHK ;SET UP FOR PATTERN CHECK
2641 031666 012737 000001 014536  JSR     PC, PATTRN ;CHECK THE PATTERN
2642 031674 005037 177572          BIT     #1, MMRO   ;ARE WE IN HIGH CORE?
2643 031700 005037 014532          BEQ     104$       ;BRANCH IF NO
2644 031704 005005          JSR     PC, RELOLO ;ELSE RELOCATE
2645 031706 077501          MOV     #1, RELODN ;SIGNAL THE SLAVES
2646 031710 162702 000002          CLR     MMRO      ;WE ARE NOW BACK DOWN IN LOW CORE
2647 031714 000137 031232          CLR     HICORE    ;MAKE SURE MM ON POWER-UP DISABLED
2648
2649
2650
2651
2652
2653
2654
2655
2656
2657
2658
2659
2660
2661
2662
2663
2664
2665
2666
2667
2668
2669
2670
2671
2672
2673
2674
2675
2676
2677
2678
2679
2680
2681
2682
2683
2684
2685
2686
2687
2688
2689
2690
2691
2692
2693
2694
2695
2696
2697
2698
2699
2700
2701
2702
2703
2704
2705
2706
2707
2708
2709
2710
2711
2712
2713
2714
2715
2716
2717
2718
2719
2720
2721
2722
2723
2724
2725
2726
2727
2728
2729
2730
2731
2732
2733
2734
2735
2736
2737
2738
2739
2740
2741
2742
2743
2744
2745
2746
2747
2748
2749
2750
2751
2752
2753
2754
2755
2756
2757
2758
2759
2760
2761
2762
2763
2764
2765
2766
2767
2768
2769
2770
2771
2772
2773
2774
2775
2776
2777
2778
2779
2780
2781
2782
2783
2784
2785
2786
2787
2788
2789
2790
2791
2792
2793
2794
2795
2796
2797
2798
2799
2800
2801
2802
2803
2804
2805
2806
2807
2808
2809
2810
2811
2812
2813
2814
2815
2816
2817
2818
2819
2820
2821
2822
2823
2824
2825
2826
2827
2828
2829
2830
2831
2832
2833
2834
2835
2836
2837
2838
2839
2840
2841
2842
2843
2844
2845
2846
2847
2848
2849
2850
2851
2852
2853
2854
2855
2856
2857
2858
2859
2860
2861
2862
2863
2864
2865
2866
2867
2868
2869
2870
2871
2872
2873
2874
2875
2876
2877
2878
2879
2880
2881
2882
2883
2884
2885
2886
2887
2888
2889
2890
2891
2892
2893
2894
2895
2896
2897
2898
2899
2900
2901
2902
2903
2904
2905
2906
2907
2908
2909
2910
2911
2912
2913
2914
2915
2916
2917
2918
2919
2920
2921
2922
2923
2924
2925
2926
2927
2928
2929
2930
2931
2932
2933
2934
2935
2936
2937
2938
2939
2940
2941
2942
2943
2944
2945
2946
2947
2948
2949
2950
2951
2952
2953
2954
2955
2956
2957
2958
2959
2960
2961
2962
2963
2964
2965
2966
2967
2968
2969
2970
2971
2972
2973
2974
2975
2976
2977
2978
2979
2980
2981
2982
2983
2984
2985
2986
2987
2988
2989
2990
2991
2992
2993
2994
2995
2996
2997
2998
2999
3000

```

```

2651
2652
2653
2654 031720
2655 031720 012777 000025 162242
2656 031726 112761 000025 014002
2657 031734 032770 000400 014160
2658 031742 001002
2659 031744 000137 035060
2660 031750
2661 031750 020027 000000
2662 031754 001002
2663 031756 000137 031766
2664 031762 000137 032020
2665 031766
2666 031766 005700
2667 031770 001007
2668 031772 104401 041476
2669 031776 005046
2670 032000 116116 014002
2671 032004 104403
2672 032006 000002
2673 032010
2674 032010 104401 014333
2675 032014 104401 041700
2676 032020 012760 004000 014612
2677 032026 005003
2678 032030 005037 014714
2679 032034 000001
2680 032036 106237 016770
2681 032042 103375
2682 032044 005237 014714
2683 032050 012737 000001 016770
2684 032056 023737 016766 014714
2685 032064 001374
2686 032066 104401 014220
2687 032072 000137 035060
2688
2689
2690 032076 005002
2691 032100 012704 172100
2692 032104 005037 014646
2693 032110
2694 032110 012760 032232 014702
2695 032116 052714 000010
2696 032122 012462 014462
2697 032126 000362 014462
2698 032132 042762 177600 014462
2699 032140 012462 014502
2700 032144 042762 177000 014502
2701 032152 016205 014502
2702 032156 072527 000012
2703 032162 010562 014502
2704 032166 016205 014462
2705 032172 072527 000012
2706 032176 010562 014462

::*****
:*TEST 25 CHECK SYSTEM RECOVERY ON AC POWER FAIL
:*****
TST25:
MOV #25,@DISPLAY ;SET TEST NUMBER
MOV #25,$STNM(R1) ;SET THE TEST NUMBER
BIT #SW08,@SWR(R0) ;SKIP THIS TEST?
BNE 1$ ;BRANCH IF NO
JMP $EOP ;ELSE GO TO EOP

1$:
CMP R0,#0 ;SWITCH THIS PROCESSOR?
BNE 64$ ;BRANCH IF NO
JMP TS25A ;YES, SWITCH TO A.
64$:
JMP TS25B ;NO, SWITCH TO B.

TS25A:
TST R0 ;IS THIS THE MASTER?
BNE 5$ ;BRANCH IF NO
TYPE ,TM77 ;'TEST'
CLR -(SP)
MOV $STNM(R1),(SP) ;GET THE TEST NO.
TYPOS
.WORD 2 ;TYPE 2 DIGITS, NO LEADING 0

5$:
TYPE ,$CRLF
TYPE ,TM104 ;'POWER FAIL ENTIRE SYSTEM'
TS25B:
MOV #1, PFFT(R0)
CLR R3
CLR SYNC.2
WAIT ;WAIT FOR POWER TO FAIL
3$:
ASRB SYNC.3 ;CONTROL THE CPUS
BCC 3$
INC SYNC.2 ;COUNT THE CPUS
MOV #1, SYNC.3 ;ALLOW ANOTHER IN
1$:
CMP CPUACT, SYNC.2
BNE 1$
TYPE ,NULL
JMP $EOP ;GO TO END OF PASS

.SBTTL MEMORY BOX TEST ROUTINES
MEMSIZ:
CLR R2 ;GET SET TO FILL THE START AND STOP TABLES
MOV #172100, R4 ;POINT TO THE FIRST CSR
CLR BOXNUM ;START WITH 0 BOXES

1$:
MOV #100$, ERRTAB(R0) ;SET UP FOR NO BOX
BIS #10, (R4) ;SET UP TO GET BOX CAPACITY
MOV (R4)+, STOP(R2)
SWAB STOP(R2)
BIC #177600, STOP(R2) ;NOW WE HAVE IT
MOV (R4)+, START(R2) ;NOW GET THE STARTING ADR.
BIC #177000, START(R2)
MOV START(R2), R5 ;MAKE IT LOOK LIKE A PAR
ASH #10., R5
MOV R5, START(R2)
MOV STOP(R2), R5 ;DO THE SAME FOR STOP
ASH #10., R5
MOV R5, STOP(R2)

```

```

2707 032202 066262 014502 014462      ADD      START(R2),      STOP(R2);STOP=START+CAPACITY
2708 032210 005237 014646      INC      BOXNUM          ;INCREMENT BOX COUNT
2709 032214 005762 014502      TST      START(R2)      ;IS THIS THE BASE BOX?
2710 032220 001413      BEQ      101$           ;BRANCH IF YES
2711 032222 016237 014502 014550      MOV      START(R2),      HIBOX ;GET A BOX TO RELOCATE TO
2712 032230 000407      BR       101$
2713 032232 012762 177777 014502 100$:  MOV      #-1,      START(R2) ;INDICATE NON-EXISTENT BOX
2714 032240 062706 000004      ADD      #4,      SP      ;RESTORE THE STACK
2715 032244 062704 000004      ADD      #4,      R4      ;POINT TO NEXT CSR PAIR
2716 032250 062702 000002      ADD      #2,      R2      ;POINT TO NEXT TABLE LOCATIONS
2717 032254 022702 000020      CMP      #20,     R2      ;HAVE WE LOOKED FOR EIGHT BOXES?
2718 032260 003313      BGT      1$           ;BRANCH IF NO
2719 032262 012760 040362 014702      MOV      #CPUER, ERRTAB(R0) ;RESET TRAP TO 4 POINTER
2720 032270 022737 000001 014646      CMP      #1,      BOXNUM  ;WAS THERE MORE THAN A SINGLE BOX?
2721 032276 002410      BLT      102$
2722 032300 005737 014522      TST      PWRFL
2723 032304 001005      BNE      102$
2724 032306 104401 043771      TYPE    ,TM109
2725 032312 012737 000001 014540      MOV      #1,      EXIT   ;SIGNAL TO EXIT
2726
2727 032320 000207      102$:  RTS      PC          ;RETURN
2728
2729 032322 105777 161662      BUF CLR: TSTB     @$TKS   ;IS THE BUFFER EMPTY?
2730 032326 100003      BPL      1$           ;BRANCH IF YES
2731 032330 117705 161656      MOV      @TKB,     R5     ;FLUSH IT
2732 032334 000772      BR       BUF CLR
2733 032336 000207      1$:    RTS      PC          ;RETURN
2734
2735 032340 005037 172340      SETMM:  CLR      KIPAR0   ;SET UP PARS 0,1,2,7
2736 032344 012737 077406 172300      MOV      #77406, KIPDR0
2737 032352 012737 000200 172342      MOV      #200,   KIPAR1
2738 032360 012737 077406 172302      MOV      #77406, KIPDR1
2739 032366 012737 000400 172344      MOV      #400,   KIPAR2
2740 032374 012737 077406 172304      MOV      #77406, KIPDR2
2741 032402 012737 177600 172356      MOV      #177600, KIPAR7
2742 032410 012737 077406 172316      MOV      #77406, KIPDR7
2743 032416 012737 000020 172516      MOV      #20,    MMR3
2744 032424 012737 033270 000250      MOV      #MMERR, MMVEC
2745 032432 000207      RTS      PC
2746
2747 032434 005737 014526      PATTRN: TST      BOOT     ;ARE WE DOING THE DC TEST?
2748 032440 001055      BNE      7$           ;BRANCH IF YES
2749 032442 005762 014502      TST      START(R2)   ;ARE WE DOING THE BASE BOX?
2750 032446 001452      BEQ      7$           ;BRANCH IF YES
2751 032450 004737 032340      JSR      PC,      SETMM ;SET UP PARS 0,1,2,7
2752 032454 016237 014502 172346      MOV      START(R2), KIPAR3 ;USE PAR3 TO WRITE PATTRN
2753 032462 012737 077406 172306      MOV      #77406, KIPDR3
2754 032470 012760 040362 014702      MOV      #CPUER, ERRTAB(R0) ;SET UP FOR UNEXPECTED TRAPS
2755 032476 052737 000001 177572      BIS      #1,      MMR0   ;TURN ON MM
2756 032504 012705 060000      1$:    MOV      #60000, R5    ;POINT TO PAR3 SPACE
2757 032510 026237 014462 172346      CMP      STOP(R2), KIPAR3 ;IS THIS THE END OF THE BOX?
2758 032516 003424      BLE      6$           ;BRANCH IF YES
2759 032520 005737 014530      2$:    TST      PATCHK    ;ARE WE WRITING A PATTERN?
2760 032524 001002      BNE      3$           ;BRANCH IF ONLY READING IT
2761 032526 012715 152525      MOV      #152525, (R5)  ;WRITE THE PATTERN
2762 032532 022725 152525      3$:    CMP      #152525, (R5)+ ;IS THE PATTERN CORRECT?
  
```

```

2763 032536 001405          BEQ      4$          ;BRANCH IF YES
2764 032540 013760 172346 014250  MOV     KIPAR3, $REG1(R0) ;SAVE THE BAD ADDRESS (PAR)
2765 032546 104013          ERROR   13          ;MEMORY IS CORRUPTED
2766 032550 000407          BR      6$          ;REPORT ONLY ONE ERROR
2767 032552 022705 100000 4$:  CMP     #100000,      R5 ;ARE WE STILL IN PAR3 SPACE?
2768 032556 003360          BGT     2$          ;BRANCH IF YES
2769 032560 062737 000200 172346  ADD     #200,  KIPAR3 ;ELSE RESET THE PAR
2770 032566 000746          BR      1$          ;AND CONTINUE
2771 032570          6$:
2772 032570 005037 177572          CLR     MMR0        ;END MM
2773 032574 000207          7$:  RTS     PC          ;RETURN
2774
2775 032576 004737 032340  RELOHI: JSR     PC,      SETMM ;SET UP PARS 0,1,2,7
2776 032602 012760 040362 014702  MOV     #CPUER, ERRTAB(R0) ;SET UP FOR TRAP TO 4
2777 032610 013737 014550 172346  MOV     HIBOX,  KIPAR3 ;PARS 3,4,5 WILL TAKE US TO HIGH CORE
2778 032616 012737 077406 172306  MOV     #77406, KIPDR3
2779 032624 013737 014550 172350  MOV     HIBOX,  KIPAR4
2780 032632 062737 000200 172350  ADD     #200,  KIPAR4
2781 032640 012737 077406 172310  MOV     #77406, KIPDR4
2782 032646 013737 014550 172352  MOV     HIBOX,  KIPAR5
2783 032654 062737 000400 172352  ADD     #400,  KIPAR5
2784 032662 012737 077406 172312  MOV     #77406, KIPDR5
2785 032670 012704 060000          MOV     #60000, R4 ;POINT TO PAR3
2786 032674 005005          CLR     R5          ;POINT TO PAR0
2787 032676 052737 000001 177572  BIS     #1,      MMR0 ;TURN ON MM
2788 032704 012524 1$:  MOV     (R5)+, (R4)+ ;RELOCATE THE PROGRAM
2789 032706 022705 060000          CMP     #60000, R5 ;ARE WE FINISHED?
2790 032712 003374          BGT     1$          ;BRANCH IF NO
2791 032714 005037 177572          CLR     MMR0        ;TURN OFF MM
2792 032720 000207          RTS     PC
2793
2794 032722 005037 172346  RELOLO: CLR     KIPAR3 ;USE PARS 3,4,5 TO RESTORE CODE TO LOW CORE
2795 032726 012737 000200 172350  MOV     #200,  KIPAR4
2796 032734 012737 000400 172352  MOV     #400,  KIPAR5
2797 032742 012704 060000          MOV     #60000, R4 ;POINT TO PAR 3
2798 032746 005005          CLR     R5          ;POINT TO PAR 0
2799 032750 012524 1$:  MOV     (R5)+, (R4)+ ;RESTORE THE PROGRAM
2800 032752 022705 060000          CMP     #60000, R5 ;ARE WE FINISHED?
2801 032756 003374          BGT     1$          ;BRANCH IF NO
2802 032760 000207          RTS     PC          ;RETURN-STILL EXECUTING IN HIGH CORE
2803
2804 032762 052737 001000 177746  ENTR:  BIS     #BIT9, CONTRL ;TURN OFF CACHE
2805 032770 017705 164026          MOV     @ACR,  R5 ;GET CPU ID
2806 032774 072527 177770          ASH     #-10,  R5
2807 033000 005004          CLR     R4          ;SET UP R0
2808 033002 026405 014226 65$:  CMP     $CPUID(R4), R5
2809 033006 001404          BEQ     64$
2810 033010 005724          TST     (R4)+
2811 033012 020427 000010          CMP     R4,      #10
2812 033016 002771          BLT     65$
2813 033020 010400 4$:  MOV     R4,      R0
2814 033022 010001          MOV     R0,      R1 ;SET UP R1
2815 033024 006201          ASR     R1
2816 033026 052777 100000 163766  BIS     #BIT15, @ACR ;INITIALIZE THE IIST
2817 033034 016006 014200          MOV     $$STP(R0), SP ;SET UP THE STACK
2818 033040 012760 034412 014662  MOV     #SPWRDN, PWRTAB(R0);SET UP FOR POWER DOWN
  
```

```
2819 033046 020027 000000      CMP      R0,      #0      ;SHOULD WE BE HERE?
2820 033052 001406      BEQ      1$          ;BRANCH IF NO
2821 033054 005060 017004      CLR      NOPRMP(R0)
2822 033060 104401 044746      TYPE    .TM111
2823 033064 000137 030762      JMP      1$24B      ;RETURN SLAVES
2824 033070 104025      1$:      ERROR     25    ;UNEXPECTED INTERRUPT
2825 033072 000000      HALT                                ;HALT THE MASTER
```



```

2826          .SBTTL  PARITY ERROR HANDLER
2827
2828 033074 005327  PARERR: DEC      (PC)+          ;FIRST TIME IN?
2829 033076 000001  PARFLG: .WORD    1
2830 033100 002001          BGE      1$                      ;BRANCH IS YES
2831 033102 000000          HALT                          ;ELSE HALT
2832 033104 013760 177766 014250 1$:  MOV      (PUERR, $REG1(R0)
2833 033112 013760 177744 014260  MOV      MEMERR, $REG2(R0)
2834 033120 104007          ERROR      7                      ;UNEXPECTED TRAP TO 114
2835 033122 000000          HALT
2836 033124 013737 177744 177744  MOV      @MEMERR,@MEMERR ;CLEAR ERROR INDICATORS
2837 033132 012737 000001 033076  MOV      #1,PARFLG          ;INITIALIZE PARITY ERROR FLAG
2838 033140 000002          RTI                          ;CONTINUE TESTING
2839          .SBTTL  SETUP MEMORY MANAGMENT REGISTERS
2840
2841 033142 012737 000000 172340 MAP:  MOV      #0,@KIPAR0          ;SETUP PAR0 FOR 1ST 4K
2842 033150 012737 077406 172300  MOV      #77406,@KIPDR0 ;4K, R/W, EXPAND UP
2843 033156 012737 000200 172342  MOV      #200,@KIPAR1     ;SETUP PAR0 FOR 2ND 4K
2844 033164 012737 077406 172302  MOV      #77406,@KIPDR1 ;4K,R/W,EXPAND UP
2845 033172 012737 000400 172344  MOV      #400,@KIPAR2     ;SETUP PAR2 FOR NEXT 4K
2846 033200 012737 077406 172304  MOV      #77406,@KIPDR2 ;4K,R/W,EXPAND UP
2847 033206 012737 000000 172352  MOV      #0,@KIPAR5       ;SET UP PAR5 FOR 1ST 4K
2848 033214 012737 077406 172312  MOV      #77406,@KIPDR5 ;4K, R/W, ED=UP
2849 033222 012737 000200 172354  MOV      #200,@KIPAR6     ;SET UP PAR6 FOR 2ND 4K
2850 033230 012737 000000 172314  MOV      #0,@KIPDR6       ;ABORT ALL REFERENCES
2851 033236 012737 177600 172356  MOV      #177600,@KIPAR7 ;SET UP PAR7 FOR I/O PAGE
2852 033244 012737 077406 172316  MOV      #77406,@KIPDR7 ;4K, R/W, ED=UP
2853 033252 012737 000020 172516  MOV      #BIT04,@MMR3     ;SET UP FOR 22-BIT MAPPING
2854 033260 012737 033270 000250  MOV      @MMERR,@MMVEC   ;SET UP MEMORY MANAGEMENT VECTOR
2855 033266 000207          RTS      PC                      ;RETURN FROM CALL
2856 033270 000000  MMERR:  HALT                          ;MEMORY MANAGEMENT ERROR
2857 033272 000776          BR      MMERR
2858
2859          .SBTTL  MASSBUS TRANSFER ROUTINES
2860
2861 033274 032737 000200 176700 MBUSR: 4$:  BIT      #BIT7, @#RPCS1          ;WAIT FOR CONTROLLER READY
2862 033302 001774          BEQ      4$
2863 033304 156037 014632 176710  BISB     MBD,$W(R0), @#RPCS2 ;GET THE DRIVE #
2864 033312 012737 174000 176702  MOV      #-4000,@#RPWC    ;;SET WORD COUNT
2865 033320 010437 176704          MOV      R4,@#RPRA        ;;SET MEMORY ADDRESS
2866 033324 005037 176706          CLR      @#RPDA          ;;READ SECTOR 0
2867 033330 032737 000200 176712 3$:  BIT      #BIT7, @#RPDS          ;WAIT FOR DRIVE READY
2868 033336 001774          BEQ      3$
2869 033340 052737 000001 176700  BIS      #BIT0,@#RPCS1    ;;
2870 033346 106237 033270 1$:  ASRB     MMERR            ;;DO ASRB DURING TRANSFER
2871 033352 106237 033270  ASRB     MMERR
2872 033356 106237 033270  ASRB     MMERR
2873 033362 106237 033270  ASRB     MMERR
2874 033366 106237 033270  ASRB     MMERR
2875 033372 106237 033270  ASRB     MMERR
2876 033376 106237 033270  ASRB     MMERR
2877 033402 106237 033270  ASRB     MMERR
2878 033406 106237 033270  ASRB     MMERR
2879 033412 106237 033270  ASRB     MMERR
2880 033416 032737 000200 176712  BIT      #BIT7,@#RPDS    ;;DEVICE READY?
2881 033424 001750          BEQ      1$              ;;BRANCH IF NO.

```

```

2882 033426 005737 176700          TST    @RPCS1          ;; ANY ERRORS?
2883 033432 100001          BPL    2$              ;; NO
2884 033434 000000          HALT                    ;; YES
2885 033436 000207          2$:   RTS    PC        ;; RETURN
2886          .SBTTL LINE CLOCK ROUTINE
2887 033440 012737 033460 000100 SETCLK: MOV    #5$,@#100  ;; SET THE INTERRUPT VECTOR FOR CLK
2888 033446 005204          INC    R4              ;; ADD 1 TO THE ARGUMENT PASSED
2889 033450 012737 000100 177546 MOV    #BIT6,@#LKS     ;; START THE CLOCK
2890 033456 000207          RTS    PC              ;; RETURN
2891 033460 052737 000340 177776 5$:   BIS    #340,@#PS      ;; HIGH PRIORITY
2892 033466 042737 000200 177546 BIC    #BIT7,@#LKS     ;; CLEAR THE MONITOR BIT
2893 033474 005304          DEC    R4              ;; ONE TICK
2894 033476 005704          TST    R4              ;; COUNT TO ZERO?
2895 033500 001010          BNE    6$              ;; NO DON'T STOP THE CLOCK
2896 033502 005037 177546          CLR    @#LKS          ;; TURN IT OFF
2897 033506 000240          NOP
2898 033510 000240          NOP
2899 033512 000240          NOP
2900 033514 000240          NOP
2901 033516 062716 000004          ADD    #4,(SP)         ;; SKIP RETURN
2902 033522 162716 000002          6$:   SUB    #2,(SP)         ;; IF COUNT ISN'T EXPIRED...
2903 033526 000002          7$:   RTI                    ;; RETURN TO THE WAIT

```

```

2904          .SBTTL POWER FAIL ROUTINE (SECTION 1)
2905
2906 033530 012737 034172 014662 POWDOWN: MOV #ILLUP,PWRTAB ;IF TOO FAST WITH POWER UP
2907 033536 105737 016740          TSTB  UBEF          ;;USE UNIBUS EXERCISER?
2908 033542 001403          BEQ    64$
2909 033544 042737 000020 170016          BIC    #BIT4,@#UBCR2 ;;CLEAR POWER FAIL ENABLE
2910 033552          64$:
2911 033552 022706 000440          CMP    #440,SP      ;YELLOW OR RED?
2912 033556 100402          BMI    1$          ;NO
2913 033560 016006 014200          MOV    $$STP(R0),SP ;SET EMERGENCY STACK
2914 033564 010246          1$:  MOV    R2,-(SP)      ;SAVE R2
2915 033566 012702 177572          MOV    #MMR0,R2     ;SAVE PSW THRU MMRO
2916 033572 012246          10$: MOV    (R2)+,-(SP)
2917 033574 022702 177676          CMP    #UDPAR7,R2
2918 033600 103374          BHIS  10$
2919 033602 013746 177776          MOV    @#PSW,-(SP)  ;SAVE PSW
2920 033606 013746 177746          MOV    @#CONTRL,-(SP) ;SAVE CACHE CONTROL
2921 033612 013746 172516          MOV    @#MMR3,-(SP) ;SAVE MMR3
2922 033616 012702 172200          MOV    #SIPDR0,R2  ;SAVE SIPDR0 THRU KDPAR7
2923 033622 012246          20$: MOV    (R2)+,-(SP)
2924 033624 022702 172376          CMP    #KDPAR7,R2
2925 033630 103374          BHIS  20$
2926 033632 012702 170200          MOV    #MAPL00,R2  ;SAVE THE UNIBUS MAP
2927 033636 012246          30$: MOV    (R2)+,-(SP)
2928 033640 022702 170376          CMP    #MAPH37,R2
2929 033644 103374          BHIS  30$
2930 033646 010046          MOV    R0,-(SP)    ;SAVE THE GENERAL REGISTERS
2931 033650 010146          MOV    R1,-(SP)
2932 033652 010346          MOV    R3,-(SP)
2933 033654 010446          MOV    R4,-(SP)
2934 033656 010546          MOV    R5,-(SP)
2935 033660 010637 014572          MOV    SP, SAV6    ;SAVE THE STACK
2936 033664 005060 016754          CLR    COUNT0(R0) ;CLEAR LOOP COUNTER
2937 033670 060000          ADD    R0, R0     ;INDEX TO THE RIGHT COUNTER
2938 033672 060000          ADD    R0, R0
2939 033674 060000          ADD    R0,R0
2940 033676 160100          SUB    R1,R0
2941 033700 160100          SUB    R1,R0
2942 033702 012737 034012 014662          MOV    #POWUP, PWRTAB ;ENABLE GOOD POWER-UP
2943 033710 012737 000001 016752          MOV    #1,LOOPS    ;# OF LOOPS FOR 2 MS (WORST CASE CONTENTION)
2944 033716 000160 033722          JMP    3$(R0)      ;START LOOPING UNTIL DC POWER FAILS
2945 033722 005237 016754          3$:  INC    COUNT0
2946
2947 033726 023737 016752 016754          CMP    LOOPS,COUNT0 ;2MS UP?
2948 033734 001372          BNE   3$          ;BRANCH IF NO
2949 033736 000000          HALT ;FINISHED
2950 033740 005237 016756          4$:  INC    COUNT1
2951 033744 023737 016752 016756          CMP    LOOPS,COUNT1
2952 033752 001372          BNE   4$
2953 033754 000000          HALT
2954 033756 005237 016760          5$:  INC    COUNT2
2955 033762 023737 016752 016760          CMP    LOOPS,COUNT2
2956 033770 001372          BNE   5$
2957 033772 000000          HALT
2958 033774 005237 016762          6$:  INC    COUNT3
2959 034000 023737 016752 016762          CMP    LOOPS,COUNT3
    
```

```

2960 034006 001372          BNE      6$
2961 034010 000000          HALT
2962
2963 034012                    POWUP:
2964 034012 012737 034176 014662  MOV     #ILLDWN,PWRTAB;SET TOO FAST DOWN VECTOR
2965 034020 013706 014572          MOV     SAV6,SP          ;RESET SP
2966 034024 012605          MOV     (SP)+,R5          ;RESTORE THE REGISTERS
2967 034026 012604          MOV     (SP)+,R4
2968 034030 012603          MOV     (SP)+,R3
2969 034032 012601          MOV     (SP)+,R1
2970 034034 012600          MOV     (SP)+,R0
2971 034036 012702 170400          MOV     #MAPH37+2,R2    ;RESTORE JNIBUS MAP
2972 034042 012642          10$:  MOV     (SP)+,-(R2)
2973 034044 022702 170200          CMP     #MAPL00,R2
2974 034050 103774          BLO     10$
2975 034052 012702 172400          MOV     #KDPAR7+2,R2    ;RESTORE K AND S PARS/PDRS
2976 034056 012642          20$:  MOV     (SP)+,-(R2)
2977 034060 022702 172200          CMP     #SIPDR0,R2
2978 034064 103774          BLO     20$
2979 034066 012637 172516          MOV     (SP)+,@MMR3      ;RESTORE MMR3
2980 034072 012637 177746          MOV     (SP)+,@CONTRL    ;RESTORE CACHE CONTRL
2981 034076 012637 177776          MOV     (SP)+,@PSW       ;RESTORE PSW
2982 034102 012702 177700          MOV     #UDPAR7+2,R2    ;RESTORE PSW THRU MMRO
2983 034106 012642          30$:  MOV     (SP)+,-(R2)
2984 034110 022702 177572          CMP     #MMR0,R2
2985 034114 103774          BLO     30$
2986 034116 012602          MOV     (SP)+,R2        ;RESTORE R2
2987 034120 004737 034202          JSR     PC, TIMIT        ;CHECK THE POWER-DOWN TIME
2988 034124 012737 033530 014662  MOV     #POWDWN,PWRTAB ;RESET THE DOWN VECTOR
2989 034132 105737 016740          TSTB   UREF              ;UBE BEING USED?
2990 034136 001403          BEQ     2$              ;BRANCH IF NO
2991 034140 012737 000001 017014  MOV     #1,UBELCK        ;CLEAR THE PF LOCK
2992 034146
2993 034146 105737 016737          TSTB   MPF              ;MULTIPROCESSOR MODE?
2994 034152 001403          BEQ     1$              ;BRANCH IF NO
2995 034154 052737 001000 177746  BIS     #1000,@CONTRL    ;BYPASS CACHE
2996 034162 052737 000014 177746  1$:  BIS     #14,@CONTRL      ;TURN OFF CACHE
2997 034170 000113          JMP     (R3)            ;JUMP INDIRECT TO R3
2998
2999 034172 000000          ILLUP: HALT              ;POWER UP BEFORE POWER DOWN COMPLETE
3000 034174 000776          BR      .-2            ;LOCK UP THE HALT
3001
3002 034176 000000          ILLDWN: HALT           ;POWERED DOWN BEFORE UP COMPLETE
3003 034200 000776          BR      .-2            ;LOCK UP THE HALT
3004
3005
3006 034202                    TIMIT:
3007 034202 023760 016752 016754  CMP     LOOPS,COUNT0(R0) ;DID WE HAVE ENOUGH POWER DOWN TIME?
3008 034210 001402          BEQ     1$              ;BRANCH IF YES
3009 034212 104401 045004          TYPE   ,$DOWN           ;NOT ENOUGH TIME
3010
3011 034216 000207          1$:  RTS     PC
  
```

```

3012          .SBTTL POWER FAIL ROUTINE (SECTION 2)
3013          $POWER:
3014 034220    005737 014532      TST      HICORE          ;DID WE POWER DOWN IN HIGH CORE?
3015 034224    001451              BEQ      1$             ;BRANCH IF NO
3016 034225    005037 172340      CLR      KIPARO         ;SET UP PARS 0,1,2,7
3017 034232    012737 077406 172300  MOV      #77406, KIPDR0
3018 034240    012737 000200 172342  MOV      #200, KIPAR1
3019 034246    012737 077406 172302  MOV      #77406, KIPDR1
3020 034254    012737 000400 172344  MOV      #400, KIPAR2
3021 034262    012737 077406 172304  MOV      #77406, KIPDR2
3022 034270    012737 177600 172356  MOV      #177600, KIPAR7
3023 034276    012737 077406 172316  MOV      #77406, KIPDR7
3024 034304    012737 000020 172516  MOV      #20, MMR3
3025 034312    012737 033270 000250  MOV      #MMERR, MMVEC
3026 034320    063737 014550 172340  ADD      HIBOX, KIPAR0
3027 034326    063737 014550 172342  ADD      HIBOX, KIPAP1
3028 034334    063737 014550 172344  ADD      HIBOX, KIPAR2
3029 034342    052737 000001 177572  BIS      #1, MMR0          ;POWER-UP IN HIGH CORE
3030 034350
3031 034350    017705 162446      1$:      MOV      @ACR, R5          ;COPY ACR
3032 034354    072527 177770      ASH      #-10, R5        ;GET THE ID
3033 034360    005004              CLR      R4             ;SET UP R0
3034 034362    026405 014226      65$:    CMP      $CPUID(R4), R5
3035 034366    001404              BEQ      64$
3036 034370    005724              TST      (R4)+
3037 034372    020427 000010      CMP      R4, #10
3038 034376    002771              BLT      65$
3039 034400    010400      64$:    MOV      R4, R0
3040 034402    010001      MOV      R0, R1
3041 034404    006201      ASR      R1
3042 034406    000170 014662      JMP      @PWRTAB(R0)     ;JUMP TO THE POWER ROUTINE
3043
3044
3045 034412    012760 035050 014662  $PWRDN: MOV      #SILLUP,PWRTAB(R0) ;SET UVECT FOR ILLEGAL UP
3046 034420    032760 000040 014612  BIT      #SSD,PFFT(R0)  ;SEND A SIGNAL?
3047 034426    001403              BEQ      10$           ;NO
3048 034430    012737 177777 014642  MOV      #-1, SIGNAL
3049
3050 034436
3051 034436    026006 017044      10$:    CMP      YELLIM(R0),SP   ;YELLOW OR RED?
3052 034442    100402              BMI      1$           ;NO
3053 034444    016006 014200      MOV      $$STP(R0),SP   ;SET EMERGENCY STACK
3054 034450    010246      1$:      MOV      R2,-(SP)       ;SAVE R2
3055 034452    012702 177572      MOV      #MMR0,R2      ;SAVE PSW THRU MMRO
3056 034456    012246      100$:   MOV      (R2)+,-(SP)
3057 034460    022702 177676      CMP      #UDPAR7,R2
3058 034464    103374              BHIS     100$
3059 034466    013746 177776      MOV      @PSW,-(SP)     ;SAVE PSW
3060 034472    013746 177746      MOV      @CONTRL,-(SP)  ;SAVE CACHE CONTRL
3061 034476    013746 172516      MOV      @MMR3,-(SP)   ;SAVE MMR3
3062 034502    012702 172200      MOV      #SIPDR0,R2    ;SAVE SIPDR0 THRU KDPAR7
3063 034506    012246      20$:    MOV      (R2)+,-(SP)
3064 034510    022702 172376      CMP      #KDPAR7,R2
3065 034514    103374              BHIS     20$
3066 034516    012702 170200      MOV      #MAPL00,R2    ;SAVE THE UNIBUS MAP
3067 034522    012246      30$:    MOV      (R2)+,-(SP)
    
```

```

3068 034524 022702 170376      CMP      #MAPH37,R2
3069 034530 103374      BHIS    30$
3070 034532 010046      MOV     R0,-(SP)      ;SAVE THE GENERAL REGISTERS
3071 034534 010146      MOV     R1,-(SP)
3072 034536 010346      MOV     R3,-(SP)
3073 034540 010446      MOV     R4,-(SP)
3074 034542 010546      MOV     R5,-(SP)
3075 034544 010660 014572      40$:   MOV     SP, SAV6(R0)      ;SAVE THE STACK
3076 034550 005060 016754      CLR     COUNT0(R0)    ;CLEAR THE LOOP COUNTER
3077 034554 012760 034676 014662      MOV     #SPWRUP, PWRTAB(R0);GET SET FOR POWER-UP
3078 034562 060000      ADD     R0, R0      ;
3079 034564 060000      ADD     R0, R0      ;INDEX TO THE RIGHT COUNTER
3080 034566 060000      ADD     R0,R0
3081 034570 160100      SUB     R1,R0
3082 034572 160100      SUB     R1,R0
3083 034574 012737 000001 016752      MOV     #1,LOOPS      ;# OF LOOPS FOR 2 MS (WORST CASE CONTENTION)
3084 034602 000160 034606      JMP     3$(R0)      ;START LOOPING UNTIL DC POWER FAILS
3085 034606 005237 016754      3$:   INC     COUNT0
3086
3087 034612 023737 016752 016754      CMP     LOOPS,COUNT0      ;2MS UP?
3088 034620 001372      BNE    3$          ;BRANCH IF NO
3089 034622 000000      HALT                    ;FINISHED
3090 034624 005237 016756      4$:   INC     COUNT1
3091 034630 023737 016752 016756      CMP     LOOPS,COUNT1
3092 034636 001372      BNE    4$
3093 034640 000000      HALT
3094 034642 005237 016760      5$:   INC     COUNT2
3095 034646 023737 016752 016760      CMP     LOOPS,COUNT2
3096 034654 001372      BNE    5$
3097 034656 000000      HALT
3098 034660 005237 016762      6$:   INC     COUNT3
3099 034664 023737 016752 016762      CMP     LOOPS,COUNT3
3100 034672 001372      BNE    6$
3101 034674 000000      HALT
3102
3103 034676 012760 035054 014662 $PWRUP: MOV     #ILLDN,PWRTAB(R0)      ;SET VECTOR FOR FAST DOWN
3104 034704 016006 014572      MOV     SAV6(R0),SP      ;RESTORE STACK
3105 034710 012605      MOV     (SP)+,R5      ;SAVE THE GENERAL REGISTERS
3106 034712 012604      MOV     (SP)+,R4
3107 034714 012603      MOV     (SP)+,R3
3108 034716 012601      MOV     (SP)+,R1
3109 034720 012600      MOV     (SP)+,R0
3110 034722 012702 170400      MOV     #MAPH37+2,R2      ;RESTORE UNIBUS MAP
3111 034726 012642      10$:   MOV     (SP)+,-(R2)
3112 034730 022702 170200      CMP     #MAPL00,R2
3113 034734 103774      BLO    10$
3114 034736 012702 172400      MOV     #KDPAR7+2,R2      ;RESTORE K AND S PARS/PDRS
3115 034742 012642      20$:   MOV     (SP)+,-(R2)
3116 034744 022702 172200      CMP     #SIPDR0,R2
3117 034750 103774      BLO    20$
3118 034752 012637 172516      MOV     (SP)+,@MMR3      ;RESTORE MMR3
3119 034756 012637 177746      MOV     (SP)+,@CONTRL    ;RESTORE CACHE CONTRL
3120 034762 012637 177776      MOV     (SP)+,@PSW      ;RFSTORE PSW
3121 034766 012702 177700      MOV     #UDPAR7+2,R2      ;RESTORE PSW THRU MMRO
3122 034772 012642      30$:   MOV     (SP)+,-(R2)
3123 034774 022702 177572      CMP     #MMR0,R2
  
```

```
3124 035000 103774      BLO      30$
3125 035002 012602      MOV      (SP)+,R2      ;RESTORE R2
3126 035004 004737 034202      JSR      PC, TIMIT    ;CHECK THE POWER DOWN
3127 035010 032760 000020 014612      BIT      #SSU,PFFT(R0) ;SEND SIGNALS?
3128 035016 001403      BEQ      45$          ;NO
3129 035020 012737 177777 014642      MOV      #-1, SIGNAL
3130 035026 005037 014712 45$:      CLR      SYNC.1      ;THIS MAY UNLOCK THE OTHER CPUS
3131 035032 012760 034412 014662      MOV      #SPWRDN,PWRTAB(R0) ;SET VECTOR FOR POWER FAIL
3132 035040 005703      TST      R3          ;IS R3 ZERO?
3133 035042 001401      BEQ      50$          ;YES
3134 035044 010316      MOV      R3,(SP)     ;FUDGE RETURN ADDRESS ON STACK
3135 035046 000002      50$:      RTI
3136
3137 035050      $ILLUP:
3138 035050 000000      HALT
3139 035052 000777      BR      .            ;POWER UP BEFORE POWER DOWN COMPLETE
3140
3141 035054      ILLDN:
3142 035054 000000      HALT
3143 035056 000777      BR      .            ;POWER DOWN BEFORE UP COMPLETE
```

```

3144      .SBTTL  END OF PASS ROUTINE
3145
3146      *****
3147      *INCREMENT THE PASS NUMBER ($PASS)
3148      *INDICATE END-OF-PROGRAM AFTER 1 PASSES THRU THE PROGRAM
3149      *TYPE 'END PASS #XXXXX TOTAL NUMBER OF ERRORS SINCE LAST REPORT'
3150      CPU #0 > AAAAA
3151      CPU #1 > BBBB
3152      CPU #2 > CCCCC
3153      CPU #3 > DDDDD
3154      TOTAL SYSTEM-WIDE ERRORS YYYYY'
3155      *WHERE XXXXX,AAAAA,BBBBB,CCCCC,DDDDD, AND YYYYY ARE DECIMAL NUMBERS
3156      *IF THERES A MONITOR GO TO IT
3157      *IF THERE ISN'T JUMP TO RESTAB
3158
3159      $EOP:
3160      035060 106237 016770      ASRB   SYNC.3      ;;CONTROL ENTRY
3161      035064 103375              BCC     $EOP
3162      035066 105737 016737      TSTB   MPF      ;;MP MODE?
3163      035072 001416              BEQ    4$      ;;BRANCH IF NO
3164      035074 005700              TST    R0      ;;IS THIS THE MASTER?
3165      035076 001414              BEQ    4$      ;;YES
3166      035100 005237 014134      INC     $EOPSG
3167      035104 012737 000001 016770  MOV     #1, SYNC.3 ;;ALLOW ANOTHER CPU IN
3168      035112 005737 014134      1$:    TST     $EOPSG ;;IS THE MASTER FINISHED?
3169      035116 001375              BNE    1$      ;;BRANCH IF NO
3170      035120 016006 014200      MOV     $$STP(R0),SP ;;RESET THE STACK
3171      035124 000170 036616      JMP     @RESTAB(R0)
3172      035130
3173      035130 005237 014134      4$:    INC     $EOPSG
3174      035134 012737 000001 016770  MOV     #1, SYNC.3 ;;ALLOW ANOTHER CPU IN
3175      035142 023737 014134 016766  5$:    CMP     $EOPSG, CPUACT
3176      035150 001374              BNE    5$
3177      035152 005237 014344      INC     $PASS ;;INCREMENT THE PASS NUMBER
3178      035156 042737 100000 014344  BIC     #100000,$PASS ;;DON'T ALLOW A NEG. NUMBER
3179      035164 005327              DEC     (PC)+ ;;LOOP?
3180      035166 000001      $EOPCT: .WORD 1
3181      035170 003402              BLE    1$      ;;YES
3182      035172 000137 035654      JMP     $DOAGN
3183      035176 012737      1$:    MOV     (PC)+,@(PC)+ ;;RESTORE COUNTER
3184      035200 000001      $ENDCT: .WORD 1
3185      035202 035166      $EOPCT
3186      035204 104401 035212      TYPE   ,65$ ;;TYPE ASCII STRING
3187      035210 000407              BR     64$ ;;GET OVER THE ASCIIZ
3188
3189      035230      ;;65$: .ASCIIZ <12><15>/END PASS #/
3190      035230 013746 014344      64$:  MOV     $PASS,-(SP) ;;SAVE $PASS FOR TYPEOUT
3191
3192      035234 104405              ;;TYPE PASS NUMBER
3193      035236 104401 035244      TYPDS ;;GO TYPE--DECIMAL ASCII WITH SIGN
3194      035242 000421              TYPE   ,67$ ;;TYPE ASCIIZ STRING
3195
3196      035306      ;;67$: .ASCIIZ / TOTAL ERRORS SINCE LAST REPORT /
3197      035306 105737 016737      66$:  TSTB   MPF
3198      035312 001524              BEQ    UNIEOP
3199      035314 104401 014333      TYPE   , $CRLF
    
```



```

3200 035320 104401 035326          TYPE      ,69$          ;;TYPE ASCIZ STRING
3201 035324 000404          BR          68$          ;;GET OVER THE ASCIZ
3202          ;;69$: .ASCIZ /CPU#0 /<76>
3203 035336          68$:
3204 035336 005003          CLR          R3
3205 035340 004737 035760          JSR          PC,EOPID
3206 035344 016346 014042          MOV          $ERTTL(R3),-(SP)          ;;SAVE $ERTTL(R3) FOR TYPEOUT
3207 035350 104405          TYPDS          ;;GO TYPE--DECIMAL ASCII WITH SIGN
3208 035352 104401 014333          TYPE      , $CRLF
3209 035356 104401 035364          TYPE      ,71$          ;;TYPE ASCIZ STRING
3210 035362 000404          BR          70$          ;;GET OVER THE ASCIZ
3211          ;;71$: .ASCIZ /CPU#1 /<76>
3212          70$:
3213 035374          MOV          #1,R3
3214 035400 004737 035760          JSR          PC,EOPID
3215 035404 016346 014042          MOV          $ERTTL(R3),-(SP)          ;;SAVE $ERTTL(R3) FOR TYPEOUT
3216 035410 104405          TYPDS          ;;GO TYPE--DECIMAL ASCII WITH SIGN
3217 035412 104401 014333          TYPE      , $CRLF
3218 035416 104401 035424          TYPE      ,73$          ;;TYPE ASCIZ STRING
3219 035422 000404          BR          72$          ;;GET OVER THE ASCIZ
3220          ;;73$: .ASCIZ /CPU#2 /<76>
3221          72$:
3222 035434          MOV          #2,R3
3223 035440 004737 035760          JSR          PC,EOPID
3224 035444 016346 014042          MOV          $ERTTL(R3),-(SP)          ;;SAVE $ERTTL(R3) FOR TYPEOUT
3225 035450 104405          TYPDS          ;;GO TYPE--DECIMAL ASCII WITH SIGN
3226 035452 104401 014333          TYPE      , $CRLF
3227 035456 104401 035464          TYPE      ,75$          ;;TYPE ASCIZ STRING
3228 035462 000404          BR          74$          ;;GET OVER THE ASCIZ
3229          ;;75$: .ASCIZ /CPU#3 /<76>
3230          74$:
3231 035474          MOV          #3,R3
3232 035500 004737 035760          JSR          PC,EOPID
3233 035504 016346 014042          MOV          $ERTTL(R3),-(SP)          ;;SAVE $ERTTL(R3) FOR TYPEOUT
3234 035510 104405          TYPDS          ;;GO TYPE--DECIMAL ASCII WITH SIGN
3235 035512 104401 014333          TYPE      , $CRLF
3236 035516 104401 035524          TYPE      ,77$          ;;TYPE ASCIZ STRING
3237 035522 000420          BR          76$          ;;GET OVER THE ASCIZ
3238          ;;77$: .ASCIZ /TOTAL SYSTEMWIDE ERROR COUNT = /
3239          76$:
3240          UNIEOP:
3241 035564 013746 014224          MOV          $ERGBL, -(SP)          ;;SAVE $ERGBL FOR TYPEOUT
3242 035570 104405          TYPDS          ;;GO TYPE--DECIMAL ASCII WITH SIGN
3243 035572 104401 014333          TYPE      , $CRLF
3244 035576 005037 014224          CLR          $ERGBL
3245 035602 012703 014042          MOV          #$ERTTL,R3          ;CLEAR THE
3246 035606 005023          CLR          (R3)+          ;ERROR TOTALS.
3247 035610 005023          CLR          (R3)+
3248 035612 005023          CLR          (R3)+
3249 035614 005023          CLR          (R3)+
3250 035616 005013          CLR          (R3)
3251 035620 000400          BR          99$          ;SKIP OVER IN SUBROUTINE
3252 035622 000404          99$: BR          $GET
3253 035624 013702 000042          $GET42: MOV          @#42,R2          ;;GET MONITOR ADDRESS
3254 035630 001411          BEQ          $DOAGN          ;;BRANCH IF NO MONITOR
3255 035632 000001          WAIT

```

```

3256 035634 013702 000042    $GET:  MOV    @#42,R2      ;;INSURE R2 CONTAINS THE MONITORS
3257 035640 001405                BEQ    $DOAGN           ;;RETURN ADDRESS
3258 035642 000005                RESET          ;;CLEAR THE WORLD
3259 035644 004712    $ENDAD: JSR    PC,(R2)    ;;GO TO MONITOR
3260 035646 000240                NOP            ;;SAVE ROOM
3261 035650 000240                NOP            ;;FOR
3262 035652 000240                NOP            ;;ACT11
3263 035654 013746 014660    $DOAGN: MOV    $PSWR, -(SP)
3264 035660 013746 014716        MOV    TYPQUE, -(SP)
3265 035664 013746 014720        MOV    TYPQUE+2, -(SP)
3266 035670 013746 016740        MOV    UBEF, -(SP)
3267 035674 013746 016766        MOV    CPUACT, -(SP)
3268 035700 013746 016736        MOV    FLAGB, -(SP)
3269 035704 004737 020000        JSR    PC, RESTRT
3270 035710 012637 016736        MOV    (SP)+, FLAGB
3271 035714 012637 016766        MOV    (SP)+, CPUACT
3272 035720 012637 016740        MOV    (SP)+, UBEF
3273 035724 012637 014720        MOV    (SP)+, TYPQUE+2
3274 035730 012637 014716        MOV    (SP)+, TYPQUE
3275 035734 012637 014660        MOV    (SP)+, $PSWR
3276 035740 005037 014134        CLR    $EOPSG          ;;CLEAR THE COUNT AND FREE SLAVES
3277 035744 016006 014200        MOV    $$STP(R0),SP    ;;RESET THE STACK
3278 035750 000170 036616        JMP    @RESTAB(R0)     ;RETURN
3279 035754      377      377    000 $ENULL: .BYTE  -1,-1,0    ;;NULL CHARACTER STRING
3280      035760      035760                .EVEN
3281 035760                EOPLID:
3282 035760 005002                CLR    R2              ;RESET FOR COUNT
3283 035762 026203 014226    65$:  CMP    $CPUID(R2),R3  ;SID MATCH?
3284 035766 001404                BEQ    64$
3285 035770 005722                TST    (R2)+           ;INCREMENT R2 BY 2
3286 035772 020227 000010        CMP    R2,#10
3287 035776 002771                BLT    65$
3288 036000 010203    64$:  MOV    R2,R3          ;MOV LOGICAL ID TO 2ND OPERAND
3289 036002 000207                RTS    PC

```

L 7

3290  
3291  
3292  
3293  
3294  
3295  
3296  
3297  
3298  
3299  
3300  
3301  
3302  
3303  
3304  
3305  
3306  
3307  
3308  
3309  
3310  
3311  
3312  
3313  
3314  
3315  
3316  
3317  
3318  
3319  
3320  
3321  
3322  
3323  
3324  
3325  
3326  
3327  
3328  
3329  
3330  
3331  
3332  
3333  
3334  
3335

036004  
036004 032770 040000 014160  
036012 001056  
036014 000416  
036016 013746 000004  
036022 012737 036042 000004  
036030 005737 177060  
036034 012637 000004  
036040 000423  
036042 022626  
036044 012637 000004  
036050 000411  
036052  
036052 105761 014006  
036056 001414  
036060 032770 001000 014160  
036066 001002  
036070 000160 036104  
036074 013760 014032 014022  
036102 000422  
036104 105061 014006  
036110 105261 014002  
036114 005710  
036116 001003  
036120 116137 014002 014342  
036126  
036126 011660 014022  
036132 011660 014032  
036136 005060 014322  
036142 112737 000001 014060  
036150 113771 014002 014170  
036156 016016 014022  
036162 000002

```

.SBTTL SCOPE HANDLER ROUTINE
:*****
:*THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
:*AND LOAD THE TEST NUMBER($STSTM) INTO THE DISPLAY REG.(DISPLAY<7:0>)
:*THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
:*SW14=1 LOOP ON TEST
:*SW09=1 LOOP ON ERROR
:*CALL
:* SCOPE ;;SCOPE=IOT

$SCOPE:
1$: BIT #BIT14,@SWR(R0) ;;LOOP ON PRESENT TEST?
   BNE $OVER ;;YES IF SW14=1
:####START OF CODE FOR THE XOR TESTER####
$XTSTR: BR 6$ ;;IF RUNNING ON THE 'XOR' TESTER CHANGE
   ;;THIS INSTRUCTION TO A 'NOP' (NOP-240)
   MOV @ERRVEC,-(SP) ;;SAVE THE CONTENTS OF THE ERROR VECTOR
   MOV #5,@ERRVEC ;;SET FOR TIMEOUT
   TST @177060 ;;TIME OUT ON XOR?
   MOV (SP)+,@ERRVEC ;;RESTORE THE ERROR VECTOR
   BR $SVLAD ;;GO TO THE NEXT TEST
5$: CMP (SP)+,(SP)+ ;;CLEAR THE STACK AFTER A TIME OUT
   MOV (SP)+,@ERRVEC ;;RESTORE THE ERROR VECTOR
   BR 7$ ;;LOOP ON THE PRESENT TEST
6$:####END OF CODE FOR THE XOR TESTER####
2$: TSTB $ERFLG(R1) ;;HAS AN ERROR OCCURRED?
   BEQ $SVLAD ;;BR IF NO
   BIT #BIT09,@SWR(R0) ;;LOOP ON ERROR?
   BNE 7$ ;;BR IF NO
   JMP 4$(R0)
7$: MOV $LPERR,$LPADR(R0) ;;SET LOOP ADDRESS TO LAST SCOPE
   BR $OVER
4$: CLRB $ERFLG(R1) ;;ZERO THE ERROR FLAG
$SVLAD: INCB $STSTM(R1) ;;COUNT TEST NUMBERS
   TST (R0) ;;IS THIS THE MASTER
   BNE 1$ ;;NO,
   MOVB $STSTM(R1),$TESTN ;;SET TEST NUMBER IN APT MAILBOX
1$: MOV (SP),$LPADR(R0) ;;SAVE SCOPE LOOP ADDRESS
   MOV (SP),$LPERR(R0) ;;SAVE ERROR LOOP ADDRESS
   CLR $ESCAPE(R0) ;;CLEAR THE ESCAPE FROM ERROR ADDRESS
   MOVB #1,$ERMAX ;;ONLY ALLOW ONE(1) ERROR ON NEXT TEST
$OVER: MOVB $STSTM,@DISPLAY(R1) ;;DISPLAY TEST NUMBER
   MOV $LPADR(R0),(SP) ;;FUDGE RETURN ADDRESS
   RTI ;;FIXES PS
    
```

```

3336      .SBTTL  ERROR HANDLER ROUTINE
3337
3338      ;*****
3339      ;*THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT,
3340      ;*SAVE THE ERROR ITEM NUMBER AND THE ADDRESS OF THE ERROR CALL
3341      ;*MADE BY THE FAILING PROCESSOR
3342      ;*AND TYPE OUT THE PROCESSOR ID AND PC OF THE ERROR INSTRUCTION
3343      ;*THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
3344      ;*SW15=1      HALT ON ERROR
3345      ;*SW09=1      LOOP ON ERROR
3346      ;*CALL
3347      ;*      ERROR      N      ;;ERROR=EMT AND N-ERROR ITEM NUMBER
3348
3349      $ERROR:
3350      036164 105261 014006 7$:      INCB      $ERFLG(R1)      ;;SET THE ERROR FLAG
3351      036170 001775      BEQ      7$      ;;DON'T LET THE FLAG GO TO ZERO
3352      036172 116170 014002 014170      MOVB      $TSTNM(R1),@DISPLAY(R0) ;;DISPLAY TEST NUMBER
3353      036200 005260 014042      INC      $ERTTL(R0)      ;;INC THE ERROR COUNT
3354      036204 005237 014224      INC      $ERGBL
3355      036210 011660 014064      MOV      (SP),$ERRPC(R0) ;;GET ADDRESS OF ERROR INSTRUCTION
3356      036214 162760 000002 014064      SUB      #2,$ERRPC(R0)
3357      036222 117061 014064 014054      MOVB      @ERRPC(R0),$ITEMB(R1) ;;STRIP AND SAVE THE ERROR ITEM CODE
3358      036230 010660 014074      MOV      SP,$ERRSP(R0) ;;SAVE THE CURRENT STACK POINTER
3359      036234 005770 014160      TST      @SWR(R0)      ;;HALT ON ERROR?
3360      036240 100025      BPL      10$      ;;SKIP IF CONTINUE
3361      036242 005700      TST      R0      ;;IS THIS THE MASTER?
3362      036244 001022      BNE      3$      ;;NO
3363      036246 104401 036254      TYPE      ,70$      ;;TYPE ASCIZ STRING
3364      036252 000417      BR      75$      ;;GET OVER THE ASCIZ
3365      036254 005015 040510 052114 70$:      .ASCIZ <15><12>/HALT ON MASTER IN $ERROR/<15><12>
3366      036262 047440 020116 040515
3367      036270 052123 051105 044440
3368      036276 020116 042444 051122
3369      036304 051117 005015      000
3370      036312      .EVEN
3371      036312      75$:
3372      036312 000000      3$:      HALT
3373      036314 000413      10$:      BR      6$
3374      036316 032770 001000 014160 4$:      BIT      #BIT9,@SWR(R0) ;;NO LOOP ON ERROR
3375      036324 001402      5$:      BEQ      5$      ;;LOOP ON ERROR SWITCH SET?
3376      036326 016016 014032      MOV      $LPERR(R0),(SP) ;;BR IF NO
3377      036332 005760 014322      5$:      TST      $ESCAPE(R0) ;;FUDGE RETURN ADDRESS
3378      036336 001402      6$:      BEQ      6$      ;;CHECK FOR AN ESCAPE ADDRESS
3379      036340 016016 014322      MOV      $ESCAPE(R0),(SP) ;;BR IF NONE
3380
3381      036344      6$:      MOV      $ESCAPE(R0),(SP) ;;FUDGE RETURN ADDRESS FOR ESCAPE
3382      036344 122737 000001 014356      CMPB      #APTENV,$ENV      ;;RUNNING IN APT MODE
3383      036352 001007      BNE      11$      ;;NO,SKIP APT ERROR REPORT
3384      036354 116137 014054 036366      MOVB      $ITEMB(R1),21$      ;;SET ITEM NUMBER AS ERROR NUMBER
3385      036362 004737 036644      JSR      PC,$ATY4      ;;REPORT FATAL ERROR TO APT
3386      036366      000      21$:      .BYTE      0
3387      036367      000      .BYTE      0
3388      036370 000777      22$:      BR      22$      ;;APT ERROR LOOP
3389      036372      11$:
3390      036372 022737 035644 000042      CMP      #SENDAD,@#42      ;;ACT-11 AUTO-ACCEPT?
3391      036400 001001      BNE      12$      ;;BRANCH IF NO
  
```

```

3392 036402 000000          HALT          ;;YES
3393 036404          12$:
3394 036404          $ERRTYP:
3395
3396 036404 106237 016774    64$:  ASRB      ERRLCK
3397 036410 103375          BCC      64$
3398 036412 010037 017056    MOV      R0,      TYPLCK      ;ALLOW THIS CPU TO ENTER TYPE ROUTINE
3399 036416 005060 017004    CLR      NOPRMP(R0)  ;;PRINT MESSAGES WITH PROMPTS
3400 036422 116105 014054    MOV      $ITEMB(R1),R5  ;;GET THE ERROR ITEM CODE
3401 036426 072527 000003    ASH      #3,      R5
3402 036432 162705 000010    SUB      #10,     R5
3403 036436 062705 017062    ADD      #$ERRTB,R5  ;;ADD THE ADDR. OF THE ERROR TABLE
3404 036442 011537 036450    MOV      (R5),1$      ;;SET UP TO...
3405 036446 104401          TYPE     ;;TYPE THE ERROR HEADER?
3406 036450 000000          1$:  .WORD    0
3407 036452 104401 014333    TYPE     , $CRLF
3408 036456 005725          TST     (R5)+        ;;INCREMENT R5 BY 2
3409 036460 005715          TST     (R5)         ;;IS THERE A DATA HEADER?
3410 036462 001406          BEQ     10$          ;;BRANCH IF NO
3411 036464 011537 036472    MOV      (R5),2$
3412 036470 104401          TYPE
3413 036472 000000          2$:  .WORD    0
3414 036474 104401 014333    TYPE     , $CRLF
3415 036500 005725          10$:  TST     (R5)+        ;;INCREMENT R5
3416 036502 005715          TST     (R5)         ;;IS THERE DATA TO BE TYPED?
3417 036504 001433          BEQ     20$
3418 036506 011505          MOV      (R5),R5     ;;GET THE DATA TABLE ADDRESS
3419 036510 005715          15$:  TST     (R5)         ;;ARE WE AT THE END OF THE DATA TABLE?
3420 036512 001430          BEQ     20$          ;;BRANCH IF YES
3421 036514 000240          NOP
3422 036516 011537 014524    MOV      (R5),      YYY     ;POINT TO THE LOCATION WITH THE NUMBER
3423 036522 022527 014002    CMP      (R5)+,     #$STNM
3424 036526 001405          BEQ     16$
3425 036530 060037 014524    ADD      R0,      YYY
3426 036534 017746 155764    MOV      @YYY,     -(SP)
3427 036540 000405          BR      17$
3428 036542 005046          16$:  CLR      -(SP)
3429 036544 060137 014524    ADD      R1,      YYY
3430 036550 117716 155750    MOV      @YYY,     (SP)
3431 036554 104402          17$:  TYPOC
3432 036556 000240          NOP
3433 036560 104401 036566    TYPE     ,66$        ;;TYPE ASCIZ STRING
3434 036564 000402          BR      65$        ;;GET OVER THE ASCIZ
3435
3436          ;;66$: .ASCIZ / /
3437          65$:
3438 036572 000746          BR      15$
3439 036574 104401 014333    20$:  TYPE     , $CRLF
3440 036600 012737 177777 017056    MOV      #-1,      TYPLCK  ;ALLOW ENTRY INTO TYPE ROUTINE
3441 036606 012737 000001 016774    MOV      #1,ERRLCK
3442 036614 000002          RTI          ;;RETURN
3443 036616 021420          RESTAB: TST1     ;;END OF PASS RETURN
3444 036620 021420          TST1
3445 036622 021420          TST1
3446 036624 021420          TST1
3447
    
```

3448

```

3449          .SBTTL  APT COMMUNICATIONS ROUTINE
3450
3451          ;:*****
3452 036626 112737 000001 037072 $ATY1:  MOVB  #1,$FFLG      ;;TO REPORT FATAL ERROR
3453 036634 112737 000001 037070 $ATY3:  MOVB  #1,$MFLG      ;;TO TYPE A MESSAGE
3454 036642 000403          BR      $ATYC
3455 036644 112737 000001 037072 $ATY4:  MOVB  #1,$FFLG      ;;TO ONLY REPORT FATAL ERROR
3456 036652          $ATYC:
3457 036652 010046          MOV    R0,-(SP)      ;;PUSH R0 ON STACK
3458 036654 010146          MOV    R1,-(SP)      ;;PUSH R1 ON STACK
3459 036656 105737 037070          TSTB  $MFLG      ;;SHOULD TYPE A MESSAGE?
3460 036662 001450          BEQ   5$          ;;IF NOT: BR
3461 036664 122737 000001 014356          CMPB  #APTENV,$ENV      ;;OPERATING UNDER APT?
3462 036672 001031          BNE   3$          ;;IF NOT: BR
3463 036674 132737 000100 014357          BITB  #APTSPOOL,$ENVM  ;;SHOULD SPOOL MESSAGES?
3464 036702 001425          BEQ   3$          ;;IF NOT: BR
3465 036704 017600 000004          MOV    @4(SP),R0      ;;GET MESSAGE ADDR.
3466 036710 062766 000002 000004          ADD    #2,4(SP)      ;;BUMP RETURN ADDR.
3467 036716 005737 014336          1$:  TST   $MSGTYPE      ;;SEE IF DONE W/ LAST XMISSION?
3468 036722 001375          BNE   1$          ;;IF NOT: WAIT
3469 036724 010037 014352          MOV    R0,$MSGAD      ;;PUT ADDR IN MAILBOX
3470 036730 105720          2$:  TSTB  (R0)+        ;;FIND END OF MESSAGE
3471 036732 001376          BNE   2$
3472 036734 163700 014352          SUB    $MSGAD,R0      ;;SUB START OF MESSAGE
3473 036740 006200          ASR   R0              ;;GET MESSAGE LNTH IN WORDS
3474 036742 010037 014354          MOV    R0,$MSGGLT     ;;PUT LENGTH IN MAILBOX
3475 036746 012737 000004 014336          MOV    #4,$MSGTYPE    ;;TELL APT TO TAKE MSG.
3476 036754 000413          BR    5$
3477 036756 017637 000004 037002 3$:  MOV    @4(SP),4$      ;;PUT MSG ADDR IN JSR LINKAGE
3478 036764 062766 000002 000004          ADD    #2,4(SP)      ;;BUMP RETURN ADDRESS
3479 036772 013746 177776          MOV    177776,-(SP)  ;;PUSH 177776 ON STACK
3480 036776 004737 037624          JSR   PC,$TYPE      ;;CALL TYPE MACRO
3481 037002 000000          4$:  .WORD  0
3482 037004          5$:
3483 037004 105737 037072          10$: TSTB  $FFLG          ;;SHOULD REPORT FATAL ERROR?
3484 037010 001416          BEQ   12$          ;;IF NOT: BR
3485 037012 005737 014356          TST   $ENV          ;;RUNNING UNDER APT?
3486 037016 001413          BEQ   12$          ;;IF NOT: BR
3487 037020 005737 014336          11$: TST   $MSGTYPE      ;;FINISHED LAST MESSAGE?
3488 037024 001375          BNE   11$          ;;IF NOT: WAIT
3489 037026 017637 000004 014340          MOV    @4(SP),$FATAL  ;;GET ERROR #
3490 037034 062766 000002 000004          ADD    #2,4(SP)      ;;BUMP RETURN ADDR.
3491 037042 005237 014336          INC   $MSGTYPE      ;;TELL APT TO TAKE ERROR
3492 037046 105037 037072          12$: CLRB  $FFLG          ;;CLEAR FATAL FLAG
3493 037052 105037 037071          CLRB  $LFLG          ;;CLEAR LOG FLAG
3494 037056 105037 037070          CLRB  $MFLG          ;;CLEAR MESSAGE FLAG
3495 037062 012601          MOV    (SP)+,R1      ;;POP STACK INTO R1
3496 037064 012600          MOV    (SP)+,R0      ;;POP STACK INTO R0
3497 037066 000207          RTS   PC            ;;RETURN
3498 037070          000          $MFLG: .BYTE 0      ;;MESSG. FLAG
3499 037071          000          $LFLG: .BYTE 0      ;;LOG FLAG
3500 037072          000          $FFLG: .BYTE 0      ;;FATAL FLAG
3501          037074          .EVEN
3502          000200          APTSIZE=200
3503          000001          APTENV=001
3504          000100          APTSPOOL=100
  
```

MAINDEC-11-CEKGB-B PDP-11/70,74 SYSTEM POWER FAIL MACY11 30A(1052) C6-JUN-79 09:12 PAGE 80  
CEKGB.P11 05-JUN-79 09:14 APT COMMUNICATIONS ROUTINE

D 8

SEQ 0094

3505 000040 APTCSUP=040



```

3506
3507
3508
3509
3510
3511
3512
3513
3514
3515
3516
3517
3518
3519
3520
3521
3522
3523
3524
3525
3526
3527
3528
3529
3530
3531 037074 017646 000000
3532 037100 116637 000001 037367
3533 037106 112637 037371
3534 037112 062716 000002
3535 037116 000406
3536 037120 112737 000001 037367
3537 037126 112737 000006 037371
3538 037134 112737 000005 037366
3539 037142 010346
3540 037144 010446
3541 037146 010546
3542 037150 113737 037371 037372
3543 037156 005437 037372
3544 037162 062737 000006 037372
3545 037170 113737 037372 037370
3546 037176 113737 037367 037372
3547 037204 016605 000012
3548 037210 005003
3549 037212 006105
3550 037214 000404
3551 037216 006105
3552 037220 006105
3553 037222 006105
3554 037224 010503
3555 037226 006103
3556 037230 105337 037370
3557 037234 100034
3558 037236 042703 177770
3559 037242 001003
3560 037244 005737 037372
3561 037250 001404

```

```

.SBTTL BINARY TO OCTAL (ASCII) AND TYPE
:*****
:*THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 6-DIGIT
:*OCTAL (ASCII) NUMBER AND TYPE IT.
:*$TYPOS---ENTER HERE TO SETUP SUPPRESS ZEROS AND NUMBER OF DIGITS TO TYPE
:*CALL:
:*      MOV      NUM,-(SP)      ;;NUMBER TO BE TYPED
:*      TYPOS    ;;CALL FOR TYPEOUT
:*      .BYTE   N              ;;N=1 TO 6 FOR NUMBER OF DIGITS TO TYPE
:*      .BYTE   M              ;;M=1 OR 0
:*                               ;;1=TYPE LEADING ZEROS
:*                               ;;0=SUPPRESS LEADING ZEROS
:*$TYPON---ENTER HERE TO TYPE OUT WITH THE SAME PARAMETERS AS THE LAST
:*$TYPOS OR $TYPOC
:*CALL:
:*      MOV      NUM,-(SP)      ;;NUMBER TO BE TYPED
:*      TYPON    ;;CALL FOR TYPEOUT
:*$TYPOC---ENTER HERE FOR TYPEOUT OF A 16 BIT NUMBER
:*CALL:
:*      MOV      NUM,-(SP)      ;;NUMBER TO BE TYPED
:*      TYPOC    ;;CALL FOR TYPEOUT
$TYPOS: MOV      @ (SP),-(SP)      ;;PICKUP THE MODE
        MOVB    1(SP), $OFILL    ;;LOAD ZERO FILL SWITCH
        MOVB    (SP)+, $OMODE+1  ;;NUMBER OF DIGITS TO TYPE
        ADD     #2, (SP)        ;;ADJUST RETURN ADDRESS
        BR      $TYPON
$TYPOC: MOVB    #1, $OFILL      ;;SET THE ZERO FILL SWITCH
        MOVB    #6, $OMODE+1    ;;SET FOR SIX(6) DIGITS
$TYPON: MOVB    #5, $OCNT      ;;SET THE ITERATION COUNT
        MOV     R3,-(SP)        ;;SAVE R3
        MOV     R4,-(SP)        ;;SAVE R4
        MOV     R5,-(SP)        ;;SAVE R5
        MOVB    $OMODE+1, DIGITS ;;GET THE NUMBER OF DIGITS TO TYPE
        NEG     DIGITS          ;;SUBTRACT IT FOR MAX. ALLOWED
        ADD     #6, DIGITS
        MOVB    DIGITS, $OMODE  ;;SAVE IT FOR USE
        MOVB    $OFILL, DIGITS  ;;GET THE ZERO FILL SWITCH
        MOV     12(SP), R5      ;;PICKUP THE INPUT NUMBER
        CLR     R3              ;;CLEAR THE OUTPUT WORD
        ROL    R5               ;;ROTATE MSB INTO 'C'
        BR     3$              ;;GO DO MSB
        ROL    R5               ;;FORM THIS DIGIT
        ROL    R5
        ROL    R5
        MOV     R5, R3
        ROL    R3              ;;GET LSB OF THIS DIGIT
        DECB   $OMODE          ;;TYPE THIS DIGIT?
        BPL    7$              ;;BR IF NO
        BIC    #177770, R3     ;;GET RID OF JUNK
        BNE    4$              ;;TEST FOR 0
        TST   DIGITS          ;;SUPPRESS THIS 0?
        BEQ   5$              ;;BR IF YES

```

```

3562 037252 005237 037372      4$: INC DIGITS      ;;DON'T SUPPRESS ANYMORE 0'S
3563 037256 052703 000060      BIS #'0,R3      ;;MAKE THIS DIGIT ASCII
3564 037262 052703 000040      5$: BIS #' ,R3   ;;MAKE ASCII IF NOT ALREADY
3565 037266 013704 037300      MOV 9$, R4      ;;POINT TO ERRBUF TABLE
3566 037272 110324      MOVB R3, (R4)+  ;;PUT THE CHARACTER IN THE TABLE
3567 037274 105014      CLRB (R4)       ;;MAKE IT A MINI-ASCII MSG
3568 037276 104401      TYPE           ;;GO TO $TYPE
3569 037300 047052      9$: ERRBUF      ;;HERE IS THE LOCATION OF MSG
3570 037302 062737 000002 037300 ADD #2, 9$      ;;MOVE TO NEXT TABLE LOC
3571 037310 023727 037300 111052 CMP 9$, #END    ;;AT THE END OF ALLOWED BUF AREA?
3572 037316 002403      BLT 7$         ;;BRANCH IF NO
3573 037320 012737 047052 037300 MOV #ERRBUF,9$  ;;ELSE POINT TO BEGINNING AGAIN
3574 037326 105337 037366      7$: DECB $OCNT  ;;COUNT BY 1
3575 037332 003331      BGT 2$        ;;BR IF MORE TO DO
3576 037334 002403      BLT 6$        ;;BR IF DONE
3577 037336 005237 037372      INC DIGITS     ;;INSURE LAST DIGIT ISN'T A BLANK
3578 037342 000725      BR 2$         ;;GO DO THE LAST DIGIT
3579 037344 012605      6$: MOV (SP)+,R5  ;;RESTORE R5
3580 037346 012604      MOV (SP)+,R4  ;;RESTORE R4
3581 037350 012603      MOV (SP)+,R3  ;;RESTORE R3
3582 037352 016666 000002 000004 MOV 2(SP),4(SP) ;;SET THE STACK FOR RETURNING
3583 037360 012616      MOV (SP)+,(SP)
3584 037362 000002      RTI          ;;RETURN
3585 037364 000      8$: .BYTE 0    ;;STORAGE FOR ASCII DIGIT
3586 037365 000      .BYTE 0      ;;TERMINATOR FOR TYPE ROUTINE
3587 037366 000      $OCNT: .BYTE 0 ;;OCTAL DIGIT COUNTER
3588 037367 000      $OFILL: .BYTE 0 ;;ZERO FILL SWITCH
3589 037370 000000      $OMODE: .WORD 0 ;;NUMBER OF DIGITS TO TYPE
3590 037372 000000      DIGITS: .WORD 0
  
```

3591  
3592  
3593  
3594  
3595  
3596  
3597  
3598  
3599  
3600  
3601  
3602  
3603  
3604  
3605  
3606  
3607  
3608  
3609  
3610  
3611  
3612  
3613  
3614  
3615  
3616  
3617  
3618  
3619  
3620  
3621  
3622  
3623  
3624  
3625  
3626  
3627  
3628  
3629  
3630  
3631  
3632  
3633  
3634  
3635  
3636  
3637  
3638  
3639  
3640  
3641  
3642  
3643  
3644  
3645  
3646

037374  
037374 010046  
037376 010146  
037400 010246  
037402 010346  
037404 010546  
037406 012746 020200  
037412 016605 000020  
037416 100004  
037420 005405  
037422 112766 000055 000001  
037430 005000  
037432 012703 037614  
037436 112723 00C040  
037442 005002  
037444 016001 037604  
037450 160105  
037452 002402  
037454 005202  
037456 000774  
037460 060105  
037462 005702  
037464 001002  
037466 105716  
037470 100407  
037472 106316  
037474 103003  
037476 116663 000001 177777  
037504 052702 000060  
037510 052702 000040  
037514 110223  
037516 005720  
037520 020027 000010  
037524 002746  
037526 003002  
037530 010502  
037532 000764  
037534 105726  
037536 100003  
037540 116663 177777 177776  
037546 105013  
037550 012605  
037552 012603  
037554 012602

```
.SBTTL CONVERT BINARY TO DECIMAL AND TYPE ROUTINE

:*****
:*THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 5-DIGIT
:*SIGNED DECIMAL (ASCII) NUMBER AND TYPE IT. DEPENDING ON WHETHER THE
:*NUMBER IS POSITIVE OR NEGATIVE A SPACE OR A MINUS SIGN WILL BE TYPED
:*BEFORE THE FIRST DIGIT OF THE NUMBER. LEADING ZEROS WILL ALWAYS BE
:*REPLACED WITH SPACES.
:*CALL:
:*      MOV      NUM,-(SP)      ;;PUT THE BINARY NUMBER ON THE STACK
:*      TYPDS                      ;;GO TO THE ROUTINE

$TYPDS:
MOV      R0,-(SP)      ;;PUSH R0 ON STACK
MOV      R1,-(SP)      ;;PUSH R1 ON STACK
MOV      R2,-(SP)      ;;PUSH R2 ON STACK
MOV      R3,-(SP)      ;;PUSH R3 ON STACK
MOV      R5,-(SP)      ;;PUSH R5 ON STACK
MOV      #20200,-(SP)   ;;SET BLANK SWITCH AND SIGN
MOV      20(SP),R5     ;;GET THE INPUT NUMBER
BPL      1$            ;;BR IF INPUT IS POS.
NEG      R5            ;;MAKE THE BINARY NUMBER POS.
MOVB     #'-,1(SP)     ;;MAKE THE ASCII NUMBER NEG.
CLR      R0            ;;ZERO THE CONSTANTS INDEX
MOV      #SDBLK,R3     ;;SETUP THE OUTPUT POINTER
MOVB     #' ,(R3)+     ;;SET THE FIRST CHARACTER TO A BLANK
2$:      CLR      R2            ;;CLEAR THE BCD NUMBER
MOV      $DTBL(R0),R1  ;;GET THE CONSTANT
3$:      SUB      R1,R5         ;;FORM THIS BCD DIGIT
BLT      4$            ;;BR IF DONE
INC      R2            ;;INCREASE THE BCD DIGIT BY 1
BR      3$
4$:      ADD      R1,R5         ;;ADD BACK THE CONSTANT
TST      R2            ;;CHECK IF BCD DIGIT=0
BNE      5$            ;;FALL THROUGH IF 0
TSTB     (SP)          ;;STILL DOING LEADING 0'S?
BMI      7$            ;;BR IF YES
5$:      ASLB     (SP)          ;;MSD?
BCC      6$            ;;BR IF NO
MOVB     1(SP),-1(R3)  ;;YES--SET THE SIGN
6$:      BIS      #'0,R2       ;;MAKE THE BCD DIGIT ASCII
7$:      BIS      #' ,R2       ;;MAKE IT A SPACE IF NOT ALREADY A DIGIT
MOVB     R2,(R3)+     ;;PUT THIS CHARACTER IN THE OUTPUT BUFFER
TST      (R0)+        ;;JUST INCREMENTING
CMP      R0,#10       ;;CHECK THE TABLE INDEX
BLT      2$            ;;GO DO THE NEXT DIGIT
BGT      8$            ;;GO TO EXIT
MOV      R5,R2        ;;GET THE LSD
BR      6$            ;;GO CHANGE TO ASCII
8$:      TSTB     (SP)+        ;;WAS THE LSD THE FIRST NON-ZERO?
BPL      9$            ;;BR IF NO
MOVB     -1(SP),-2(R3) ;;YES--SET THE SIGN FOR TYPING
9$:      CLRB     (R3)         ;;SET THE TERMINATOR
MOV      (SP)+,R5     ;;POP STACK INTO R5
MOV      (SP)+,R3     ;;POP STACK INTO R3
MOV      (SP)+,R2     ;;POP STACK INTO R2
```

3647	037556	012601		MOV	(SP)+,R1	::POP STACK INTO R1
3648	037560	012600		MOV	(SP)+,R0	::POP STACK INTO R0
3649	037562	000240		NOP		
3650	037564	104401	037614	TYPE	,\$DBLK	::NOW TYPE THE NUMBER
3651	037570	000240		NOP		
3652	037572	016666	000002 000004	MOV	2(SP),4(SP)	::ADJUST THE STACK
3653	037600	012616		MOV	(SP)+,(SP)	
3654	037602	000002		RTI		::RETURN TO USER
3655	037604	023420		\$DTBL:	10000.	
3656	037606	001750			1000.	
3657	037610	000144			100.	
3658	037612	000012			10.	
3659	037614	000004		\$DBLK:	.BLKW 4	

```

3660 .SBTTL TYPE SERVICE
3661 037624 $TYPE:
3662 037624 132737 000040 014357 BITB #40, $ENVM ;INHIBIT PRINT OUT?
3663 037632 001403 BEQ 6$ ;BRANCH IF NO
3664 037634 062716 000002 ADD #2, (SP) ;SET RETURN
3665 037640 000002 RTI
3666 037642 6$:
3667 037642 005737 016774 TST ERRLCK ;IS A CPU IN THE ERROR ROUTINE?
3668 037646 001003 BNE 3$ ;BRANCH IF NO
3669 037650 020037 017056 CMP R0, TYPLCK ;IS THIS CPU FROM THE ERROR ROUTINE?
3670 037654 001363 BNE $TYPE ;BRANCH IF NO
3671 037656 010246 3$: MOV R2, -(SP) ;STORE REGISTERS USED IN THIS PROGRAM
3672 037660 010346 MOV R3, -(SP)
3673 037662 010446 MOV R4, -(SP)
3674 037664 010546 MOV R5, -(SP)
3675 037666 105737 016737 TSTB MPF
3676 037672 001003 BNE 1$
3677 037674 012704 000400 MOV #400, R4 ;DONT TYPE A CPUID
3678 037700 000414 BR 2$
3679 037702 017705 157114 1$: MOV @ACR, R5 ;PUT SELF ID INTO R5
3680 037706 072527 177770 ASH #-10, R5
3681 037712 010504 MOV R5, R4 ;PUT ID INTO R4
3682 037714 016002 017004 MOV NOPRMP(R0),R2 ;COPY THE PROMPT FLAG
3683 037720 000302 SWAB R2 ;GET IT INTO THE LEFT HALF
3684 037722 050204 BIS R2,R4 ;PUT IT IN R5
3685 037724 012760 000001 017004 MOV #1, NOPRMP(R0)
3686 037732 106237 017016 2$: ASRB TQL1 ;ENTER TYPQUE CRITICAL SECTION
3687 037736 103375 BCC 2$
3688
3689 037740 013703 014720 ;:***** ENQUE *****
3690 037744 005723 MOV TYPQUE+2,R3 ;COPY REAR INDEX
3691 037746 010413 TST (R3)+ ;INCREMENT BY 2
3692 037750 010337 014720 64$: MOV R4,(R3) ;QUEUE THE ELEMENT
3693 037754 010337 MOV R3,TYPQUE+2 ;UPDATE THE REAR INDEX
3694 037754 4$: ;:***** ENQUE *****
3695
3696 037754 013703 014720 MOV TYPQUE+2,R3 ;COPY REAR INDEX
3697 037760 005723 TST (R3)+ ;INCREMENT BY 2
3698 037762 016613 000010 65$: MOV 10(SP),(R3) ;QUEUE THE ELEMENT
3699 037766 010337 014720 MOV R3,TYPQUE+2 ;UPDATE THE REAR INDEX
3700 ;:***** ENQUE *****
3701 037772 013343 MOV @R3+, -(R3) ;GET PC OF MSG
3702 037774 012737 000001 017016 5$: MOV #1,TQL1 ;CLEAR CRITICAL SECTION
3703 040002 005700 TST R0 ;IS THIS THE MASTER?
3704 040004 001407 BEQ 11$ ;BRANCH IF YES.
3705 040006 012605 MOV (SP)+, R5 ;RESTORE THE REGISTERS
3706 040010 012604 MOV (SP)+, R4
3707 040012 012603 MOV (SP)+, R3
3708 040014 012602 MOV (SP)+, R2
3709 040016 062716 000002 ADD #2, (SP)
3710 040022 000002 RTI ;RETURN
3711 040024 10$:
3712 040024 106237 017016 11$: ASRB TQL1 ;ENTER CRITICAL SECTOR
3713 040030 103375 BCC 11$
3714 040032 HERE:
3715 ;:***** DEQUE *****
    
```

```

3716 040032 023737 014716 014720      CMP      TYPQUE,TYPQUE+2 ;;ARE THE INDICIES EQUAL?
3717 040040 001456                      BEQ      13$              ;;YES,THE QUEUE IS EMPTY
3718 040042 013703 014716      MOV      TYPQUE,R3              ;;COPY FRONT INDEX INTO R3
3719 040046 005723                      TST      (R3)+                ;;INC. R3 BY TWO
3720 040050 011304                      MOV      (R3),R4 ;;DEQUEUE AN ELEMENT
3721 040052 010337 014716      MOV      R3,TYPQUE            ;;UPDATE FRONT INDEX
3722                                     ;;*****
3723 040056 032704 000400      BIT      #BIT8,R4              ;WAS THE NOPRMP(R0) BIT SET?
3724 040062 001025                      BNE      12$
3725 040064 062704 021060      ADD      #'0',R4                ;MAKE CPUID A CHARACTER
3726 040070 112702 000015      MOVB     #CR,R2                 ;TYPE # CARRAGE RETURN
3727 040074 004737 040236      JSR      PC,TYPIT              ;TYPE CRLF
3728 040100 112702 000012      MOVB     #LF,R2                 ;TYPE IT
3729 040104 004737 040236      JSR      PC,TYPIT              ;TYPE IT
3730 040110 110402                      MOVB     R4,R2                  ;CPU ID
3731 040112 004737 040236      JSR      PC,TYPIT              ;TYPE IT
3732 040116 112702 021076      MOVB     #'>',R2                ; '>'
3733 040122 004737 040236      JSR      PC,TYPIT              ;TYPE IT
3734 040126 112702 021040      MOVB     #' ',R2                ;TYPE A SPACE
3735 040132 004737 040236      JSR      PC,TYPIT
3736 040136                                     12$:
3737                                     ;;***** DEQUE *****
3738 040136 023737 014716 014720      CMP      TYPQUE,TYPQUE+2 ;;ARE THE INDICIES EQUAL?
3739 040144 001414                      BEQ      13$              ;;YES,THE QUEUE IS EMPTY
3740 040146 013703 014716      MOV      TYPQUE,R3              ;;COPY FRONT INDEX INTO R3
3741 040152 005723                      TST      (R3)+                ;;INC. R3 BY TWO
3742 040154 011304                      MOV      (R3),R4 ;;DEQUEUE AN ELEMENT
3743 040156 010337 014716      MOV      R3,TYPQUE            ;;UPDATE FRONT INDEX
3744                                     ;;*****
3745 040162 112402                                     14$: MOVB     (R4)+,R2          ;GET A CHARECTER
3746 040164 005702                      TST      R2
3747 040166 001721                      BEQ      HERE                ;WE'RE DONE ,R2 IS CLEAR
3748 040170 004737 040236      JSR      PC,TYPIT              ;TYPE THE CHARECTER
3749 040174 000772                      BR       14$                  ;LOOP
  
```

```

3750 04076 012737 014722 014716 13$: MOV #TYPQUE+4, TYPQUE
3751 040204 012737 014722 014720 MOV #TYPQUE+4, TYPQUE+2
3752 040212 012737 000001 017016 MOV #1, TQL1 ;RETURN
3753 040220 012605 MOV (SP)+, R5 ;RESTORE THE REGISTERS
3754 040222 012604 MOV (SP)+, R4
3755 040224 012603 MOV (SP)+, R3
3756 040226 012602 MOV (SP)+, R2
3757 040230 062716 000002 ADD #2, (SP)
3758 040234 000002 RTI
3759
3760 040236 105777 153752 TYPIT: TSTB @STPS ;WAIT UNTIL PRINTER IS READY
3761 040242 100375 BPL TYPIT
  
```

3762 040244 110277 153746            MOVB    R2,@\$TPB            ;TYPE THE CHARACTER  
3763 040250 000207            RTS      PC            ;RETURN



```

3764      .SBTTL TRAP DECODER
3765
3766      ;*****
3767      ;*THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE 'TRAP' INSTRUCTION
3768      ;*AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS
3769      ;*OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
3770      ;*GO TO THAT ROUTINE.
3771
3772      040252 010260 014552      $TRAP: MOV      R2,      SAVRG(R0)
3773      040256 011602              1$:  MOV      (SP),R2      ;;GET TRAP ADDRESS
3774      040260 005742              TST      -(R2)      ;;BACKUP BY 2
3775      040262 111202              MOVB     (R2),R2     ;;GET RIGHT BYTE OF TRAP
3776      040264 006302              ASL     R2          ;;POSITION FOR INDEXING
3777      040266 016202 040320      MOV     $TRPAD(R2),R2 ;;INDEX TO TABLE
3778      040272 010260 014562      MOV     R2,      ROUTE(R0)
3779      040276 016002 014552      MOV     SAVRG(R0), R2
3780      040302 000170 014562      JMP     @ROUTE(R0)
3781
3782
3783
3784      ;;THIS IS USE TO HANDLE THE 'GEIPRI' MACRO
3785
3786      040306 011646              $TRAP2: MOV     (SP),-(SP) ;;MOVE THE PC DOWN
3787      040310 016666 000004 000002  MOV     4(SP),2(SP) ;;MOVE THE PSW DOWN
3788      040316 000002              RTI                    ;;RESTORE THE PSW
3789
3790      .SBTTL TRAP TABLE
3791
3792      ;*THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED
3793      ;*BY THE 'TRAP' INSTRUCTION.
3794
3795      :      ROUTINE
3796      :      -----
3797      040320 040306      $TRPAD: .WORD  $TRAP2
3798      040322 037624      $TYPE  ;;CALL=TYPE      TRAP+1(104401) TTY TYPEOUT ROUTINE
3799      040324 037120      $TYPOC ;;CALL=TYPOC     TRAP+2(104402) TYPE OCTAL NUMBER (WITH LEADING ZEROS)
3800      040326 037074      $TYPOS  ;;CALL=TYPOS     TRAP+3(104403) TYPE OCTAL NUMBER (NO LEADING ZEROS)
3801      040330 037134      $TYPON  ;;CALL=TYPON     TRAP+4(104404) TYPE OCTAL NUMBER (AS PER LAST CALL)
3802      040332 037374      $TYPDS  ;;CALL=TYPDS     TRAP+5(104405) TYPE DECIMAL NUMBER (WITH SIGN)
3803
3804
3805
3806      040334 000170 014672      ISTDIS: JMP     @ISTTAB(R0) ;IIST INTERRUPT DISPATCHER
3807
    
```

```

3808 040340 012737 177777 014602 PWRDIS: MOV # -1, FLAG ;FIRST INSTRUCTION FLAG
3809 040346 005037 014602 CLR FLAG ;NOW CLEAR IT
3810 040352 000177 154304 JMP @PWRTAB
3811 040356 000170 014702 ERRDIS: JMP @ERRTAB(R0) ;CPU ERROR DISPATCHER
3812
3813 040362 CPUER:
3814 040362 015760 177766 014250 MOV @CPUERR,$REG1(P0) ;CPU ERROR REG.
3815 040370 104005 ERROR 5
3816 040372 000000 HALT
3817 040374 000002 RTI ;RETURN
3818
3819 040376 005015 042503 041113 TM1: .SBTTL DATA AREA
3820 040404 026507 020102 030440 .ASCIZ <CR><LF>\CEKGB-B 11/70-74MP SYSTEM POWER FAIL DIAGNOSTIC\
3821 040412 027461 030067 033455
3822 040420 046464 020120 054523
3823 040426 052123 046505 050040
3824 040434 053517 051105 043040
3825 040442 044501 020114 044504
3826 040450 043501 047516 052123
3827 040456 041511 000
3828 040461 015 051412 044527 TM2: .ASCIZ <CR><LF>\SWITCH REGISTER = \
3829 040466 041524 020110 042522
3830 040474 044507 052123 051105
3831 040502 036440 000040
3832 040506 005015 052533 044516 TM4: .ASCIZ <CR><LF>/[UNIBUS EXERCISER WILL BE USED]/
3833 040514 052502 020123 054105
3834 040522 051105 044503 042523
3835 040530 020122 044527 046114
3836 040536 041040 020105 051525
3837 040544 042105 000135
3838 040550 005015 052533 044516 TM5: .ASCIZ <CR><LF>/[UNIBUS EXERCISER WILL NOT BE USED]/
3839 040556 052502 020123 054105
3840 040564 051105 044503 042523
3841 040572 020122 044527 046114
3842 040600 047040 052117 041040
3843 040606 020105 051525 042105
3844 040614 000135
3845 040616 005015 046533 046125 TM6: .ASCIZ <CR><LF>/[MULTIPROCESSOR MODE IS IN EFFECT]/
3846 040624 044524 051120 041517
3847 040632 051505 047523 020122
3848 040640 047515 042504 044440
3849 040646 020123 047111 042440
3850 040654 043106 041505 056524
3851 040662 000
3852 040663 015 055412 047125 TM7: .ASCIZ <CR><LF>/[UNIPROCESSOR MODE IS IN EFFECT]/
3853 040670 050111 047522 042503
3854 040676 051523 051117 046440
3855 040704 042117 020105 051511
3856 040712 044440 020116 043105
3857 040720 042506 052103 000135
3858 040726 055440 052117 042510 TM10: .ASCIZ / [OTHER CPUS ARE RUNNING.]/
3859 040734 020122 050103 051525
3860 040742 040440 042522 051040
3861 040750 047125 044516 043516
3862 040756 056456 000
3863 040761 015 003412 050103 TM11: .ASCIZ <CR><LF><07>/CPU #/
    
```

3864	040766	020125	000043		
3865	040772	051440	042520	044503	TM12: .ASCIZ / SPECIFIED BUT NOT ACTIVE/
3866	041000	044506	042105	041040	
3867	041006	052125	047040	052117	
3868	041014	040440	052103	053111	
3869	041022	000105			

3870	041024	005015	047111	042524	TM13:	.ASCII <CR><LF>/INTERRUPT THE POWER AFTER THE TEST NUMBER APPEARS/
3871	041032	051122	050125	020124		
3872	041040	044124	020105	047520		
3873	041046	042527	020122	043101		
3874	041054	042524	020122	044124		
3875	041062	020105	042524	052123		
3876	041070	047040	046525	042502		
3877	041076	020122	050101	042520		
3878	041104	051101	123			
3879	041107	040	047111	052040		.ASCII / IN THE DISPLAY./<CR><LF>
3880	041114	042510	042040	051511		
3881	041122	046120	054501	006456		
3882	041130	012				
3883	041131	111	020106	047531		.ASCII /IF YOU HAVE AN RD CONSOLE, INTERRUPT THE POWER/
3884	041136	020125	040510	042526		
3885	041144	040440	020116	042122		
3886	041152	041440	047117	047523		
3887	041160	042514	020054	047111		
3888	041166	042524	051122	050125		
3889	041174	020124	044124	020105		
3890	041202	047520	042527	122		
3891	041207	015	040412	020124		.ASCII <CR><LF>/AT THE END OF THIS MESSAGE. THEREAFTER, INTERRUPT THE POWER 15(
3892	041214	044124	020105	047105		
3893	041222	020104	043117	052040		
3894	041230	044510	020123	042515		
3895	041236	051523	043501	027105		
3896	041244	020040	044124	051105		
3897	041252	040505	052106	051105		
3898	041260	044454	052116	051105		
3899	041266	052522	052120	052040		
3900	041274	042510	050040	053517		
3901	041302	051105	030440	024065		
3902	041310	024470	046440	051117		
3903	041316	020105	044524	042515		
3904	041324	123				
3905	041325	015	052012	020117		.ASCIZ <CR><LF>/TO REACH THE END OF SECTION 1./<CR><LF>
3906	041332	042522	041501	020110		
3907	041340	044124	020105	047105		
3908	041346	020104	043117	051440		
3909	041354	041505	044524	047117		
3910	041362	030440	006456	000012		
3911	041370	005015	042412	052116	TM14:	.ASCIZ<CR><LF><LF>/ENTERING SECTION 1/<CR><LF>
3912	041376	051105	047111	020107		
3913	041404	042523	052103	047511		
3914	041412	020116	006461	000012		
3915	041420	005015	042412	052116	TM15:	.ASCIZ<CR><LF><LF>/ENTERING SECTION 2/<CR><LF>
3916	041426	051105	047111	020107		
3917	041434	042523	052103	047511		
3918	041442	020116	006462	000012		
3919	041450	006412	044124	020105	TM76:	.ASCIZ<12><15>/THE MASTER IS CPU #/
3920	041456	040515	052123	051105		
3921	041464	044440	020123	050103		
3922	041472	020125	000043			
3923	041476	005012	052015	051505	TM77:	.ASCIZ<12><12><15>/TEST /
3924	041504	020124	000			
3925	041507	015	050012	053517	TM100:	.ASCIZ <CR><LF>/POWER FAIL CPU # /

3926	041514	051105	043040	044501	
3927	041522	020114	050103	020125	
3928	041530	020043	000		
3929	041533	015	005012	047516	TM101: .ASCIZ <CR><LF><LF>/NO MASSBUS DEVICE AVAILABLE ON CPU # /
3930	041540	046440	051501	041123	
3931	041546	051525	042040	053105	
3932	041554	041511	020105	053101	
3933	041562	044501	040514	046102	
3934	041570	020105	047117	041440	
3935	041576	052520	021440	000040	
3936	041604	005015	051120	041517	TM102: .ASCIZ <CR><LF>/PROCEEDING TO NEXT CPU/
3937	041612	042505	044504	043516	
3938	041620	052040	020117	042516	
3939	041626	052130	041440	052520	
3940	041634	000			
3941	041635	015	050012	053517	TM103: .ASCIZ <CR><LF>/POWER FAILURE ON CPU AS EXPECTED/
3942	041642	051105	043040	044501	
3943	041650	052514	042522	047440	
3944	041656	020116	050103	020125	
3945	041664	051501	042440	050130	
3946	041672	041505	042524	000104	
3947	041700	005015	042507	020124	TM104: .ASCII <CR><LF>/GET SET TO POWER FAIL ENTIRE SYSTEM.../
3948	041706	042523	020124	047524	
3949	041714	050040	053517	051105	
3950	041722	043040	044501	020114	
3951	041730	047105	044524	042522	
3952	041736	051440	051531	042524	
3953	041744	027115	027056		
3954	041750	005012	050015	052125	.ASCII<12><12><15>/PUT BATTERY BACKUP ON ALL MEM BOXES/
3955	041756	041040	052101	042524	
3956	041764	054522	041040	041501	
3957	041772	052513	020120	047117	
3958	042000	040440	046114	046440	
3959	042006	046505	041040	054117	
3960	042014	051505			
3961	042016	006412	040515	042513	.ASCII<12><15>/MAKE ALL MEMORY PORTS ONLINE/
3962	042024	040440	046114	046440	
3963	042032	046505	051117	020131	
3964	042040	047520	052122	020123	
3965	042046	047117	044514	042516	
3966	042054	006412	040515	042513	.ASCII<12><15>/MAKE ALL CPU POWER-UP SWITCHES 'RUN OR HALT'/
3967	042062	040440	046114	041440	
3968	042070	052520	050040	053517	
3969	042076	051105	052455	020120	
3970	042104	053523	052111	044103	
3971	042112	051505	021040	052522	
3972	042120	020116	051117	044040	
3973	042126	046101	021124		
3974	042132	005012	052015	042510	.ASCII<12><12><15>/THEN POWER FAIL THE ENTIRE SYSTEM/
3975	042140	020116	047520	042527	
3976	042146	020122	040506	046111	
3977	042154	052040	042510	042440	
3978	042162	052116	051111	020105	
3979	042170	054523	052123	046505	
3980	042176	005012	051015	051505	.ASCII<12><12><15>/RESTORE POWER 5 SECONDS AFTER POWER FAIL/
3981	042204	047524	042522	050040	

3982	042212	053517	051105	032440	
3983	042220	051440	041505	047117	
3984	042226	051504	040440	052106	
3985	042234	051105	050040	053517	
3986	042242	051105	043040	044501	
3987	042250	114			
3988	042251	012	042415	041501	.ASCIZ<12><15>/EACH CPU SHOULD REPORT A POWER FAIL/
3989	042256	020110	050103	020125	
3990	042264	044123	052517	042114	
3991	042272	051040	050105	051117	
3992	042300	020124	020101	047520	
3993	042306	042527	020122	040506	
3994	042314	046111	000		
3995	042317	015	005012	042507	TM106: .ASCIZ <CR><LF><LF>/GET SET TO POWER FAIL MEM BOX # /
3996	042324	020124	042523	020124	
3997	042332	047524	050040	053517	
3998	042340	051105	043040	044501	
3999	042346	020114	042515	020115	
4000	042354	047502	020130	020043	
4001	042362	000			
4002	042363	012	006412	052520	TM107: .ASCII<12><12><15> /PUT BATTERY BACKUP ON ALL MEMORY BOXES/
4003	042370	020124	040502	052124	
4004	042376	051105	020131	040502	
4005	042404	045503	050125	047440	
4006	042412	020116	046101	020114	
4007	042420	042515	047515	054522	
4008	042426	041040	054117	051505	
4009	042434	006412	040515	042513	.ASCII<12><15>/MAKE ALL MEMORY PORTS ONLINE/
4010	042442	040440	046114	046440	
4011	042450	046505	051117	020131	
4012	042456	047520	052122	020123	
4013	042464	047117	044514	042516	
4014	042472	006412	040515	042513	.ASCII<12><15>/MAKE ALL CPU POWER-UP SWITCHES 'RUN OR HALT'/
4015	042500	040440	046114	041440	
4016	042506	052520	050040	053517	
4017	042514	051105	052455	020120	
4018	042522	053523	052111	044103	
4019	042530	051505	021040	052522	
4020	042536	020116	051117	044040	
4021	042544	046101	021124		
4022	042550	005012	052015	042510	.ASCII<12><12><15>/THEN POWER FAIL THE MEM BOX/
4023	042556	020116	047520	042527	
4024	042564	020122	040506	046111	
4025	042572	052040	042510	046440	
4026	042600	046505	041040	054117	
4027	042606	005012	051015	051505	.ASCII<12><12><15>/RESTORE POWER 5 SECONDS AFTER POWER FAIL/
4028	042614	047524	042522	050040	
4029	042622	053517	051105	032440	
4030	042630	051440	041505	047117	
4031	042636	051504	040440	052106	
4032	042644	051105	050040	053517	
4033	042652	051105	043040	044501	
4034	042660	114			
4035	042661	012	052015	042510	.ASCII<12><15>/THEN TYPE ANY CHARACTER AT THE MASTER CONSOLE/
4036	042666	020116	054524	042520	
4037	042674	040440	054516	041440	

4038	042702	040510	040522	052103
4039	042710	051105	040440	020124
4040	042716	044124	020105	040515
4041	042724	052123	051105	041440
4042	042732	047117	047523	042514
4043	042740	006412	040505	044103
4044	042746	041440	052520	051440
4045	042754	047510	046125	020104
4046	042762	042522	047520	052122
4047	042770	040440	050040	053517
4048	042776	051105	043040	044501
4049	043004	052514	042522	000
4050	043011	012	006412	052520
4051	043016	020124	040502	052124
4052	043024	051105	020131	040502
4053	043032	045503	050125	047440
4054	043040	020116	046101	020114
4055	043046	042515	047515	054522
4056	043054	041040	054117	051505
4057	043062	006412	040515	042513
4058	043070	040440	046114	046440
4059	043076	046505	051117	020131
4060	043104	047520	052122	020123
4061	043112	043117	046106	047111
4062	043120	020105	047117	046440
4063	043126	046505	041040	054117
4064	043134	052040	020117	042502
4065	043142	050040	053517	051105
4066	043150	043055	044501	042514
4067	043156	104		
4068	043157	012	046415	045501
4069	043164	020105	046101	020114
4070	043172	050103	020125	047520
4071	043200	042527	026522	050125
4072	043206	051440	044527	041524
4073	043214	042510	020123	051042
4074	043222	047125	047440	020122
4075	043230	040510	052114	042
4076	043235	012	006412	044124
4077	043242	047105	050040	053517
4078	043250	051105	043040	044501
4079	043256	020114	044124	020105
4080	043264	042515	020115	047502
4081	043272	130		
4082	043273	012	006412	042522
4083	043300	052123	051117	020105
4084	043306	047520	042527	020122
4085	043314	020065	042523	047503
4086	043322	042116	020123	043101
4087	043330	042524	020122	047520
4088	043336	042527	020122	040506
4089	043344	046111		
4090	043346	006412	042522	052123
4091	043354	051117	020105	046101
4092	043362	020114	042515	047515
4093	043370	054522	050040	051117

.ASCII<12><15>/EACH CPU SHOULD REPORT A POWER FAILURE/

TM108: .ASCII<12><12><15>/PUT BATTERY BACKUP ON ALL MEMORY BOXES/

.ASCII<12><15>/MAKE ALL MEMORY PORTS OFFLINE ON MEM BOX TO BE POWER-FAILED/

.ASCII<12><15>/MAKE ALL CPU POWER-UP SWITCHES 'RUN OR HALT'/

.ASCII<12><12><15>/THEN POWER FAIL THE MEM BOX/

.ASCII<12><12><15>/RESTORE POWER 5 SECONDS AFTER POWER FAIL/

.ASCII<12><15>/RESTORE ALL MEMORY PORTS ONLINE/

4094	043376	051524	047440	046116	
4095	043404	047111	105		
4096	043407	012	052015	042510	.ASCII<12><15>/THEN TYPE ANY CHARACTER AT THE MASTER CONSOLE/
4097	043414	020116	054524	042520	
4098	043422	040440	054516	041440	
4099	043430	040510	040522	052103	
4100	043436	051105	040440	020124	
4101	043444	044124	020105	040515	
4102	043452	052123	051105	041440	
4103	043460	047117	047523	042514	
4104	043466	006412	047516	041440	.ASCIZ<12><15>/NO CPU SHOULD REPORT A POWER FAILURE/
4105	043474	052520	051440	047510	
4106	043502	046125	020104	042522	
4107	043510	047520	052122	040440	
4108	043516	050040	053517	051105	
4109	043524	043040	044501	052514	
4110	043532	042522	000		
4111	043535	012	005015	040527	\$PGM1: .ASCIZ <12><15><12>/WARNING: DRIVE # /
4112	043542	047122	047111	035107	
4113	043550	020040	051104	053111	
4114	043556	020105	020043	000	
4115	043563	012	047415	020116	\$PGM2: .ASCIZ<12><15> /ON CPU # /
4116	043570	050103	020125	020043	
4117	043576	000			
4118	043577	012	044415	020123	\$PGM3: .ASCII <12><15>/IS PROGRAMMABLE OVER BOTH A AND B PORTS/
4119	043604	051120	043517	040522	
4120	043612	046515	041101	042514	
4121	043620	047440	042526	020122	
4122	043626	047502	044124	040440	
4123	043634	040440	042116	041040	
4124	043642	050040	051117	051524	
4125	043650	006412	044124	020105	.ASCIZ<12><15>/THE DRIVE WILL BE USED LATER IN THIS DIAGNOSTIC/
4126	043656	051104	053111	020105	
4127	043664	044527	046114	041040	
4128	043672	020105	051525	042105	
4129	043700	046040	052101	051105	
4130	043706	044440	020116	044124	
4131	043714	051511	042040	040511	
4132	043722	047107	051517	044524	
4133	043730	000103			
4134	043732	006412	047516	046440	NODEV: .ASCIZ <12><15>/NO MASSBUS DEVICES ON CPU # /
4135	043740	051501	041123	051525	
4136	043746	042040	053105	041511	
4137	043754	051505	047440	020116	
4138	043762	050103	020125	020043	
4139	043770	000			
4140	043771	012	006412	047117	TM109: .ASCIZ <12><12><15>/ONLY ONE MEMORY BOX ONLINE- SKIPPING THIS TEST/
4141	043776	054514	047440	042516	
4142	044004	046440	046505	051117	
4143	044012	020131	047502	020130	
4144	044020	047117	044514	042516	
4145	044026	020055	045523	050111	
4146	044034	044520	043516	052040	
4147	044042	044510	020123	042524	
4148	044050	052123	000		
4149	044053	012	006412	044504	TM110: .ASCII<12><12><15>/DISABLE BATTERY BACKUP ON MEM BOX TO BE POWER-FAILED/



4150	044060	040523	046102	020105
4151	044066	040502	052124	051105
4152	044074	020131	040502	045503
4153	044102	050125	047440	020116
4154	044110	042515	020115	047502
4155	044116	020130	047524	041040
4156	044124	020105	047520	042527
4157	044132	026522	040506	046111
4158	044140	042105		
4159	044142	006412	052520	020124
4160	044150	046101	020114	046123
4161	044156	053101	020105	050103
4162	044164	020125	042515	020115
4163	044172	047520	052122	020123
4164	044200	047117	044514	042516
4165	044206	006412	040515	042513
4166	044214	046440	051501	042524
4167	044222	020122	050103	020125
4168	044230	042515	020115	047520
4169	044236	052122	047440	043106
4170	044244	044514	042516	047440
4171	044252	020116	047502	020130
4172	044260	047524	041040	020105
4173	044266	047520	042527	026522
4174	044274	040506	046111	042105
4175	044302	006412	040515	042513
4176	044310	040440	046114	041440
4177	044316	052520	050040	053517
4178	044324	051105	052455	020120
4179	044332	053523	052111	044103
4180	044340	051505	021040	052522
4181	044346	020116	051117	041040
4182	044354	047517	021124	
4183	044360	005012	052015	042510
4184	044366	020116	047520	042527
4185	044374	020122	040506	046111
4186	044402	052040	042510	046440
4187	044410	046505	041040	054117
4188	044416	005012	051015	051505
4189	044424	047524	042522	050040
4190	044432	053517	051105	032440
4191	044440	051440	041505	047117
4192	044446	051504	040440	052106
4193	044454	051105	050040	053517
4194	044462	051105	043040	044501
4195	044470	114		
4196	044471	012	051015	051505
4197	044476	047524	042522	040440
4198	044504	046114	046440	046505
4199	044512	050040	051117	051524
4200	044520	047440	046116	047111
4201	044526	105		
4202	044537	012	051015	051505
4203	044534	047524	042522	040440
4204	044542	046114	041440	052520
4205	044550	050040	053517	051105

.ASCII<12><15>/PUT ALL SLAVE CPU MEM PORTS ONLINE/

.ASCII<12><15>/MAKE MASTER CPU MEM PORT OFFLINE ON BOX TO BE POWER-FAILED/

.ASCII<12><15>/MAKE ALL CPU POWER-UP SWITCHES 'RUN OR BOOT'/

.ASCII<12><12><15>/THEN POWER FAIL THE MEM BOX/

.ASCII<12><12><15>/RESTORE POWER 5 SECONDS AFTER POWER FAIL/

.ASCII<12><15>/RESTORE ALL MEM PORTS ONLINE/

.ASCII<12><15>/RESTORE ALL CPU POWER-UP SWITCHES TO 'RUN OR HALT'/

4206 044556 052455 020120 053523  
4207 044564 052111 044103 051505  
4208 044572 052040 020117 051042  
4209 044600 047125 047440 020122  
4210 044606 040510 052114 042  
4211 044613 012 052015 042510  
4212 044620 020116 054524 042520  
4213 044626 040440 054516 041440  
4214 044634 040510 040522 052103  
4215 044642 051105 040440 020124  
4216 044650 044124 020105 040515  
4217 044656 052123 051105 041440  
4218 044664 047117 047523 042514  
4219 044672 006412 040505 044103  
4220 044700 051440 040514 042526  
4221 044706 041440 052520 051440  
4222 044714 047510 046125 020104  
4223 044722 042522 047520 052122  
4224 044730 040440 020116 047111  
4225 044736 042524 051122 050125  
4226 044744 000124  
4227 044746 006412 050103 020125  
4228 044754 047111 042524 051122  
4229 044762 050125 042524 020104  
4230 044770 051501 042440 050130  
4231 044776 041505 042524 000104  
4232 045004 006412 047520 042527  
4233 045012 020122 047504 047127  
4234 045020 052040 046511 020105  
4235 045026 040527 020123 047125  
4236 045034 042504 020122 020062  
4237 045042 044515 044514 042523  
4238 045050 047503 042116 020123  
4239 045056 000  
4240 045057 015 052412 042516  
4241 045064 050130 041505 042524  
4242 045072 020104 047520 042527  
4243 045100 020122 040506 046111  
4244 045106 051125 020105 047117  
4245 045114 041440 052520 000  
4246 045121 015 052412 042516  
4247 045126 050130 041505 042524  
4248 045134 020104 047520 042527  
4249 045142 020122 050125 051440  
4250 045150 050505 042525 041516  
4251 045156 020105 047117 041440  
4252 045164 052520 000  
4253 045167 015 044412 046114  
4254 045174 043505 046101 050040  
4255 045202 053517 051105 042040  
4256 045210 053517 020116 042523  
4257 045216 052521 047105 042503  
4258 045224 047440 020116 050103  
4259 045232 000125  
4260 045234 005015 046111 042514  
4261 045242 040507 020114 047520

.ASCII<12><15>/THEN TYPE ANY CHARACTER AT THE MASTER CONSOLE/

.ASCII<12><15>/EACH SLAVE CPU SHOULD REPORT AN INTERRUPT/

TM111: .ASCII<12><15>/CPU INTERRUPTED AS EXPECTED/

\$DOWN: .ASCII <12><15>/POWER DOWN TIME WAS UNDER 2 MILLISECONDS /

EM1: .ASCII <CR><LF>/UNEXPECTED POWER FAILURE ON CPU/

EM2: .ASCII <CR><LF>/UNEXPECTED POWER UP SEQUENCE ON CPU/

EM3: .ASCII <CR><IF>/ILLEGAL POWER DOWN SEQUENCE ON CPU/

EM4: .ASCII <CR><LF>/ILLEGAL POWER UP SEQUENCE/

4262	045250	042527	020122	050125		
4263	045256	051440	050505	042525		
4264	045264	041516	000105			
4265	045270	005015	047125	054105	EM5:	.ASCIZ <CR><LF>/UNEXPECTED TRAP TO 4/
4266	045276	042520	052103	042105		
4267	045304	052040	040522	020120		
4268	045312	047524	032040	000		
4269	045317	015	052412	042516	EM6:	.ASCIZ <CR><LF>/UNEXPECTED TRAP TO 10/
4270	045324	050130	041505	042524		
4271	045332	020104	051124	050101		
4272	045340	052040	020117	030061		
4273	045346	000				
4274	045347	015	052412	042516	EM7:	.ASCIZ <CR><LF>/UNEXPECTED TRAP TO 114/
4275	045354	050130	041505	042524		
4276	045362	020104	051124	050101		
4277	045370	052040	020117	030461		
4278	045376	000064				
4279	045400	005015	042101	051104	EM10:	.ASCIZ <CR><LF>/ADDRESS ON STACK IS WRONG/
4280	045406	051505	020123	047117		
4281	045414	051440	040524	045503		
4282	045422	044440	020123	051127		
4283	045430	047117	000107			
4284	045434	005015	046117	020104	EM11:	.ASCIZ <CR><LF>/OLD PS IS WRONG/
4285	045442	051520	044440	020123		
4286	045450	051127	047117	000107		
4287	045456	005015	042117	020104	EM12:	.ASCIZ <CR><LF>/ODD ADDRESS TRAP FAILED/
4288	045464	042101	051104	051505		
4289	045472	020123	051124	050101		
4290	045500	043040	044501	042514		
4291	045506	000104				
4292	045510	005015	042515	047515	EM13:	.ASCIZ <CR><LF>/MEMORY CORRUPTED ON POWER FAIL/
4293	045516	054522	041440	051117		
4294	045524	052522	052120	042105		
4295	045532	047440	020116	047520		
4296	045540	042527	020122	040506		
4297	045546	046111	000			
4298	045551	015	052012	046511	EM14:	.ASCIZ <CR><LF>/TIMEOUT TRAP FAILED/
4299	045556	047505	052125	052040		
4300	045564	040522	020120	040506		
4301	045572	046111	042105	000		
4302	045577	015	050012	053517	EM15:	.ASCIZ <CR><LF>/POWER FAIL RETURNED TOO SOON/
4303	045604	051105	043040	044501		
4304	045612	020114	042522	052524		
4305	045620	047122	042105	052040		
4306	045626	047517	051440	047517		
4307	045634	000116				
4308	045636	005015	047516	020124	EM16:	.ASCIZ <CR><LF>/NOT ENOUGH OR TOO MANY INSTRUCTIONS EXECUTED/
4309	045644	047105	052517	044107		
4310	045652	047440	020122	047524		
4311	045660	020117	040515	054516		
4312	045666	044440	051516	051124		
4313	045674	041525	044524	047117		
4314	045702	020123	054105	041505		
4315	045710	052125	042105	000		
4316	045715	015	047012	020117	EM17:	.ASCIZ <CR><LF>/NO MEM. MANG. VIOLATION OR TRAP TO 4/
4317	045722	042515	027115	046440		

4318	045730	047101	027107	053040					
4319	045736	047511	040514	044524					
4320	045744	047117	047440	020122					
4321	045752	051124	050101	052040					
4322	045760	020117	000064						
4323	045764	005015	047516	044440	EM20:	.ASCIIZ	<CR><LF>/NO IIST INTERRUPT/		
4324	045772	051511	020124	047111					
4325	046000	042524	051122	050125					
4326	046006	000124							
4327	046010	005015	047111	047503	EM21:	.ASCIIZ	<CR><LF>?INCORRECT BRK AND/OR DCF FLAGS?		
4328	046016	051122	041505	020124					
4329	046024	051102	020113	047101					
4330	046032	027504	051117	042040					
4331	046040	043103	043040	040514					
4332	046046	051507	000						
4333	046051	015	041412	052520	EM22:	.ASCIIZ	<CR><LF>/CPU DID NOT TRAP TO VIRTUAL 24/		
4334	046056	042040	042111	047040					
4335	046064	052117	052040	040522					
4336	046072	020120	047524	053040					
4337	046100	051111	052524	046101					
4338	046106	031040	000064						
4339	046112	005015	044103	041505	EM23:	.ASCIIZ	<CR><LF>/CHECKSUM ON MASSBUS TRANSFER IS WRONG/		
4340	046120	051513	046525	047440					
4341	046126	020116	040515	051523					
4342	046134	052502	020123	051124					
4343	046142	047101	043123	051105					
4344	046150	044440	020123	051127					
4345	046156	047117	000107						
4346	046162	006412	047516	050040	EM24:	.ASCIIZ	<12><15>/NO POWER FAIL ON CPU/		
4347	046170	053517	051105	043040					
4348	046176	044501	020114	047117					
4349	046204	041440	052520	000					
4350	046211	012	052415	042516	EM25:	.ASCIIZ	<12><15>/UNEXPECTED CPU INTERRUPT/		
4351	046216	050130	041505	042524					
4352	046224	020104	050103	020125					
4353	046232	047111	042524	051122					
4354	046240	050125	000124						
4355									
4356	046244	005015	044511	052123	DH5:	.ASCIIZ	<CR><LF>/IISTID PC CPUERR/		
4357	046252	042111	020011	050040					
4358	046260	020103	020040	020040					
4359	046266	020040	050103	042525					
4360	046274	051122	000						
4361	046277	015	020012	044440	DH7:	.ASCIIZ	<CR><LF>/ IISTID ERRORPC CPUERR MEMERR/		
4362	046304	051511	044524	020104					
4363	046312	020040	042440	051122					
4364	046320	051117	041520	020040					
4365	046326	050103	042525	051122					
4366	046334	020040	046440	046505					
4367	046342	051105	000122						
4368	046346	005015	042524	052123	DH10:	.ASCIIZ	<CR><LF>/TESTNO ERRORPC/		
4369	046354	047516	020040	042440					
4370	046362	051122	051117	041520					
4371	046370	000							
4372	046371	015	052012	051505	DH11:	.ASCIIZ	<CR><LF>/TESTNO ERRORPC PS/		
4373	046376	047124	020117	020040					

4374	046404	051105	047522	050122					
4375	046412	020103	020040	020040					
4376	046420	051520	000						
4377	046423	012	052015	051505	DH12:	.ASCIZ	<12><15>/TESTNO	ERRORPC	PAGE ADDRESS REGISTER OF BAD MEMORY/
4378	046430	047124	004517	051105					
4379	046436	047522	050122	020103					
4380	046444	020040	040520	042507					
4381	046452	040440	042104	042522					
4382	046460	051523	051040	043505					
4383	046466	051511	042524	020122					
4384	046474	043117	041040	042101					
4385	046502	046440	046505	051117					
4386	046510	000131							
4387	046512	005015	042524	052123	DH14:	.ASCIZ	<CR><LF>/TESTNO	ERRORPC	CPUERR/
4388	046520	047516	020040	042440					
4389	046526	051122	051117	041520					
4390	046534	020040	050103	042525					
4391	046542	051122	000						
4392	046545	015	052012	051505	DH20:	.ASCIZ	<CR><LF>/TESTNO	IISTID	ACR PGTE PGCS/
4393	046552	047124	020117	020040					
4394	046560	044440	051511	044524					
4395	046566	020104	020040	020040					
4396	046574	041501	020122	020040					
4397	046602	020040	043520	042524					
4398	046610	020040	020040	050040					
4399	046616	041507	000123						
4400	046622	005015	042524	052123	DH21:	.ASCIZ	<CR><LF>/TESTNO	IISTID	FOUND SHOULD BE/
4401	046630	047516	020040	020040					
4402	046636	044511	052123	042111					
4403	046644	020040	043040	052517					
4404	046652	042116	020040	020040					
4405	046660	044123	052517	042114					
4406	046666	041040	000105						
4407	046672	005015	042524	052123	DH22:	.ASCIZ	<CR><LF>/TESTNO	IISTID	ERRORPC/
4408	046700	047516	020040	044440					
4409	046706	051511	044524	020104					
4410	046714	020040	042440	051122					
4411	046722	051117	041520	000					
4412		046730					.EVEN		
4413									
4414	046730	014240	014064	014250	DT5:	\$REG0,\$ERRPC,\$REG1,0			
4415	046736	000000							
4416	046740	014240	014064	014250	DT7:	\$REG0,\$ERRPC,\$REG1,\$REG2,0			
4417	046746	014260	000000						
4418	046752	014002	014064	000000	DT10:	\$STNM,\$ERRPC,0			
4419	046760	014002	014064	014240	DT11:	\$STNM,\$ERRPC,\$REG0,0			
4420	046766	000000							
4421	046770	014002	014064	014250	DT12:	\$STNM,\$ERRPC,\$REG1,0			
4422	046776	000000							
4423	047000	014002	014240	014250	DT20:	\$STNM,\$REG0,\$REG1,\$REG2,\$REG3,0			
4424	047006	014260	014270	000000					
4425	047014	014002	014240	014250	DT21:	\$STNM,\$REG0,\$REG1,\$REG2,0			
4426	047022	014260	000000						
4427	047026	014002	014240	014064	DT22:	\$STNM,\$REG0,\$ERRPC,0			
4428	047034	000000							
4429	047036	005015	020133	045517	OK:	.ASCIZ	<CR><LF>/[ OK ] /		

4430 047044 056440 020040 000  
4431 047052 047052  
4432 047052 001000  
4433 051052 020000  
4434 111052 000000

.EVEN  
ERRBUF: .BLKW 1000  
DSKBUF: .BLKW 20000  
END: 0

;ERROR ASCII MSG STORAGE AREA  
;MASSBUS BUFFER AREA

4435  
4436           000001           .END





AVECT1=	000000	722	761															
AVECT2=	000000	722	762															
BAD	025124	1911	1919#	1928														
BEGIN	021420	1221	1237#															
BFADR	017034	871#	2112	2117	2121	2127	2146	2151	2158	2163								
BIT0 =	000001	196#	500	1073	1132	1134	1147	1156	1230	2308	2466	2623	2869					
BIT00 =	000001	186#	196															
BIT01 =	000002	185#	195															
BIT02 =	000004	184#	194															
BIT03 =	000010	183#	193															
BIT04 =	000020	182#	192	2853														
BIT05 =	000040	181#	191															
BIT06 =	000100	180#	190															
BIT07 =	000200	179#	189															
BIT08 =	000400	178#	188															
BIT09 =	001000	177#	187	3318														
BIT1 =	000002	195#	501															
BIT10 =	002000	176#	538															
BIT11 =	004000	175#	537	1110	1152													
BIT12 =	010000	174#	536															
BIT13 =	020000	173#																
BIT14 =	040000	172#	511	1803	3302													
BIT15 =	100000	171#	512	1108	1192	1210	1214	1218	1236	1778	1868	1971	2040	2197				
		2248	2355	2406	2512	2563	2816											
BIT2 =	000004	194#	502	1194	1930													
BIT3 =	000010	193#	503															
BIT4 =	000020	192#	544	1290	1334	1363	1398	1434	1440	1460	1468	1499	1506	1530				
		1537	1548	1574	1598	1606	1628	1636	1658	1666	1688	1696	1722	1728				
		2909																
BIT5 =	000040	191#	509	543	1799													
BIT6 =	000100	190#	508	542	2889													
BIT7 =	000200	189#	541	2861	2867	2880	2892											
BIT8 =	000400	188#	540	1810	3723													
BIT9 =	001000	187#	510	539	1166	1184	1806	1829	1836	2804	3374							
BMSK	017032	870#	1032*	1146	1163*													
BOOT	014526	795#	2242*	2266	2287	2400*	2424	2445	2557*	2581	2602	2747						
BOXNUM	014646	822#	2264	2422	2579	2692*	2708*	2720										
BPTVEC=	000014	203#																
BUF CLR	032322	2279	2437	2594	2729#	2732												
CACHVE=	000114	211#	1268*															
CKSUM	014650	823#	1324*	1325*	1326*	1345	2115*	2118*	2119*	2131	2149*	2152*	2153*	2167				
CONTRL=	177746	220#	1166*	1174*	1184*	2804*	2920	2980*	2995*	2996*	3060	3119*						
COUNT0	016754	849#	2936*	2945*	2947	3007	3076*	3085*	3087									
COUNT1	016756	850#	2950*	2951	3090*	3091												
COUNT2	016760	851#	2954*	2955	3094*	3095												
COUNT3	016762	852#	2958*	2959	3098*	3099												
CPUACT	016766	854#	1023	1107*	1157*	1230	1772	1846	1871	1874	1974	1977	2043	2046				
		2069	2079	2189	2308	2347	2466	2504	2623	2684	3175	3267	3271*					
CPUER	040362	1066	1072	1078	1443	1473	1510	1541	1610	1640	1670	1700	1734	1800				
		2201	2252	2359	2410	2516	2567	2719	2754	2776	3813#							
CPUERR=	177766	232#	2832	3814														
CP0 =	000001	500#																
CP1 =	000002	501#																
CP2 =	000004	502#																
CP3 =	000010	503#																
CR =	000015	108#	3726	3819	3828	3832	3838	3845	3852	3863	3870	3879	3891	3905				







MAPH22=	170312	429#				
MAPH23=	170316	431#				
MAPH24=	170320	433#				
MAPH25=	170326	435#				
MAPH26=	170332	437#				
MAPH27=	170336	439#				
MAPH3 =	170216	463#				
MAPH30=	170342	441#				
MAPH31=	170346	443#				
MAPH32=	170352	445#				
MAPH33=	170356	447#				
MAPH34=	170362	449#				
MAPH35=	170366	451#				
MAPH36=	170372	453#				
MAPH37=	170376	455#	2928	2971	3068	3110
MAPH4 =	170222	465#				
MAPH5 =	170226	467#				
MAPH6 =	170232	469#				
MAPH7 =	170236	471#				
MAPL0 =	170200	456#				
MAPL00=	170200	392#	456	2926	2973	3066 3112
MAPL01=	170204	394#	458			
MAPL02=	170210	396#	460			
MAPL03=	170214	398#	462			
MAPL04=	170220	400#	464			
MAPL05=	170224	402#	466			
MAPL06=	170230	404#	468			
MAPL07=	170234	406#	470			
MAPL1 =	170204	458#				
MAPL10=	170240	408#				
MAPL11=	170244	410#				
MAPL12=	170250	412#				
MAPL13=	170254	414#				
MAPL14=	170260	416#				
MAPL15=	170264	418#				
MAPL16=	170270	420#				
MAPL17=	170274	422#				
MAPL2 =	170210	460#				
MAPL20=	170300	424#				
MAPL21=	170304	426#				
MAPL22=	170310	428#				
MAPL23=	170314	430#				
MAPL24=	170320	432#				
MAPL25=	170324	434#				
MAPL26=	170330	436#				
MAPL27=	170334	438#				
MAPL3 =	170214	462#				
MAPL30=	170340	440#				
MAPL31=	170344	442#				
MAPL32=	170350	444#				
MAPL33=	170354	446#				
MAPL34=	170360	448#				
MAPL35=	170364	450#				
MAPL36=	170370	452#				
MAPL37=	170374	454#				
MAPL4 -	170220	464#				





























.S4OCA 1#  
.1170 1# 88

. ABS. 111054 000

ERRORS DETECTED: 0

DSKZ:CEKBGB.BIN,DSKZ:CEKBGB.LST/CRF/SOL-CEKBGB.SML,CEKBGB.P11  
RUN-TIME: 47 60 5 SECONDS  
RUN-TIME RATIO: 325/114=2.8  
CORE USED: 39K (77 PAGES)