

TO: Distribution

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0442

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DEPT: 11 Engineering

EXT: 5064 LOC: 1-2

SUBJ: Initial Feedback on Chapter Scheme

VAS MEMO #2

1. Problems

- (1) External representation of a process's loaded image will need to be an encoding of the internal representation because of the tagged stack. Needed, for example, in swapping out a process.
- (2) References to the tagged stack will not necessarily be through R6, e.g.,

```
MOV SP, R0
ADD (R0)+, B
```

Hence, the implementation must be able to recognize this.

2. Suggestions

- (1) The tag needed for stack entries could be bit 0 (PC <0> is redundant on the stack).
- (2) Allow 32-bit addresses in indirect addressing and use bit 0 as tag.
- (3) Make mode 5 do something useful.

3. Clarifications

- (1) Index mode, X(R6) goes through the stack entries one by one to the X'th one.
- (2) Rules for addresses in the registers:
  - a. registers always hold 32 bit address
  - b. loading a register always fills 32 bits

(a) Memory to register

- i. MOV:           c ← current chapter
- ii. LA:           c ← high 16 bits of operand

(b) Stack to register

- i. MOV when stack entry is short: c ← current chapter  
       "       "       "       " long: c ← high 16 bits of entry
- ii. LA       "       "       "       " long:       "  
       "       "       "       " short:       error

(c) Register to register  
Long address to long address

Distribution

- Bruce Delagi
- Bill Strecker
- Dave Rodgers
- Ron Brender
- Ed Marison
- Jega Arulpragasam
- John Levy
- Bill Demmer
- Len Hughes
- Bob Gray