DISTRIBUTED PLANT MANAGEMENT

DPM50 user guide

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DPM50 user guide

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

The DPM50 is an intelligent, real-time, factory floor process I/O subsystem with an intelligent interface to the DECdataway. The DECdataway provides bidirectional, multidrop communication between a central computing facility and DPM50 subsystems scattered through an industrial environment. This arrangement constitutes a Distributed Plant Management (DPM) system.

This user guide provides functional and physical descriptions, general software information, installation instructions, and maintenance procedures for the DPM50. It should be used with the following manuals.

I/O Subsystem User Guide	(EK-OPIOS-UG)
DECdataway User's Guide	(EK-ISB11-UG)
Microcomputer Processor Handbook	(EB-15836-18)
Microcomputer Interfaces Handbook	(EB-17723-20)

Chapter 1 provides functional, physical, and software descriptions, specifications, and a list of related documentation.

Chapter 2 provides installation and configuration information. This chapter relies on information contained in the manuals listed above.

Chapter 3 provides maintenance procedures and troubleshooting flowcharts.

Chapter 4 provides a detailed technical description of the ISV11-A DECdataway Communications Interface.

1.2 FUNCTIONAL DESCRIPTION

The DPM50 is an industrial I/O subsystem which uses an LSI-11 or LSI-11/23 based microcomputer and an interface to the DECdataway. This interface to the DECdataway makes the DPM50 a *subsystem* in a DPM *system*.

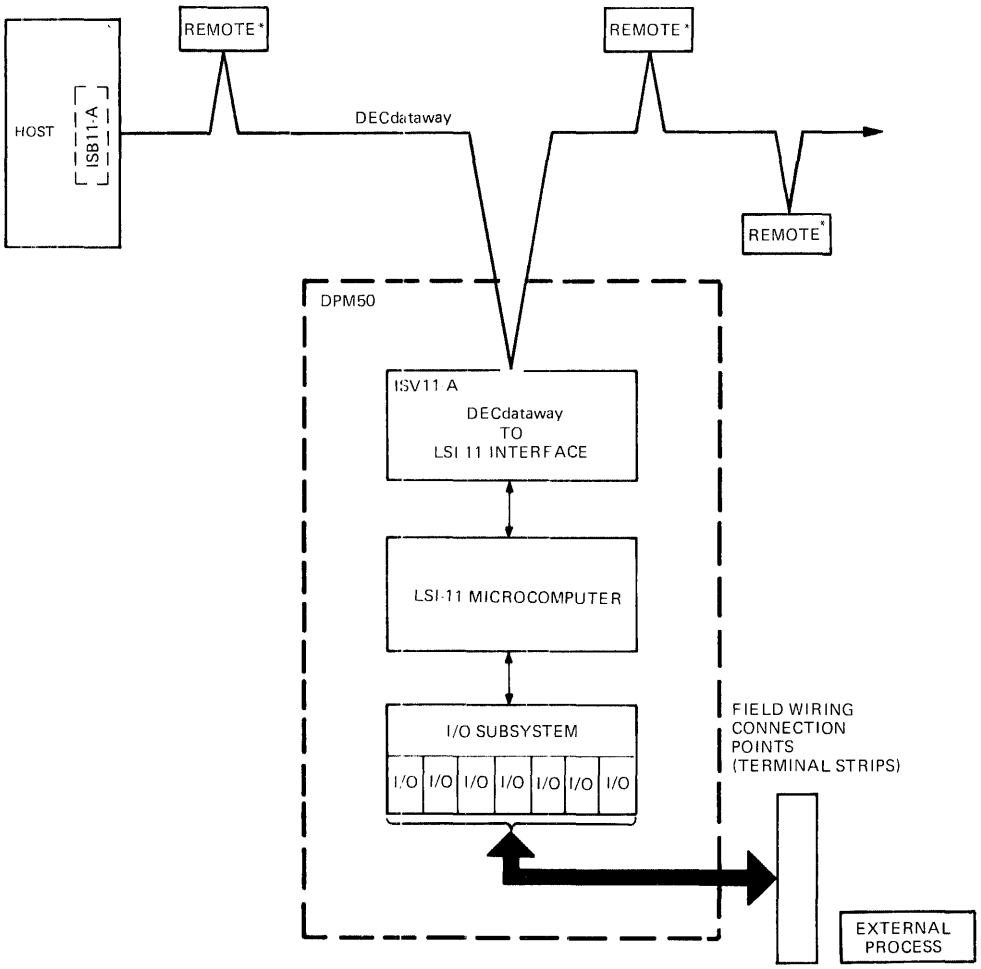


Figure 1-1 DPM50 Organization in a Typical DPM System

1.2.1 Distributed Plant Management Overview

DPM is a concept that connects a PDP-11 host computer to remote subsystems or terminals scattered through an industrial environment. DECdataway is the communication channel that links the host computer to these remote subsystems.

Figure 1-1 is a block diagram showing the DPM50 functional organization in a typical DPM system. It shows a host computer linked to various remote subsystems, including a DPM50, via a DECdataway. Refer to Figure 1-1 throughout the rest of this discussion.

The DECdataway consists of an ISB11-A interfaced to a PDP-11, and a cable. The dataway cable is a twisted shielded pair cable up to 15,000

feet (4572 meters) long that integrates processes throughout a large industrial complex. Connectors are placed along the cable, creating ports through which messages can pass to or from connected subsystems.

Communication over the DECdataway is synchronous serial at 55,556 bits per second. The host computer maintains control of all communications over the dataway. All transactions on the dataway consist of two messages: first, a command from the host to a port and second, a response from a port to the host. There is one exception, the host can broadcast a message to all ports simultaneously with no response allowed from any port. Each port connector has address jumpers installed so the host can select which remote to communicate with. A port can have more than one address associated with it. This is the case with a port connected to a DPM50 (which has two addresses). However, the number of addresses per DECdataway cannot exceed 63. Therefore one DECdataway can accommodate 31 DPM50s at most. A more in-depth discussion of the DECdataway is presented in the *DECdataway User's Guide*.

The DPM50 I/O subsystem is designed to monitor and/or control external processes. It does this through the use of a variety of digital and analog input/output (I/O) modules.

The LSI-11 directly controls the I/O subsystem (and therefore the external process) by executing user programs located in its own local memory. These programs are initially transferred by the host to the DPM50 as a series of messages over the DECdataway. These messages are received by the ISV11-A DECdataway interface and stored in the LSI-11 memory. This transfer of information from the host to a remote is referred to as *downline loading*.

The ISV11-A also can accept data from the LSI-11 microcomputer. Upon request from the host, the ISV11-A formats and transmits this data *upline* to the host.

After downline loading a program into a remote DPM50 the host only has to communicate with that task rather than control the external process itself. If the DPM50 is gathering data, the LSI-11 microcomputer can preprocess the raw data before it is upline loaded to the host. This division of work among various intelligent components in the system frees the host to communicate with other remotes on the DECdataway. Therefore the host maintains fundamental control over the entire system, but does so efficiently by delegating most of the work to individual remotes along the DECdataway. This arrangement typifies a DIGITAL Distributed Plant Management system.

1.2.2 The DPM50

A detailed functional diagram of the DPM50 is given in Figure 1-2. It shows the functional organization of major components and bus structures that make up the DPM50. The DPM50 is divided into the following three main functional areas.

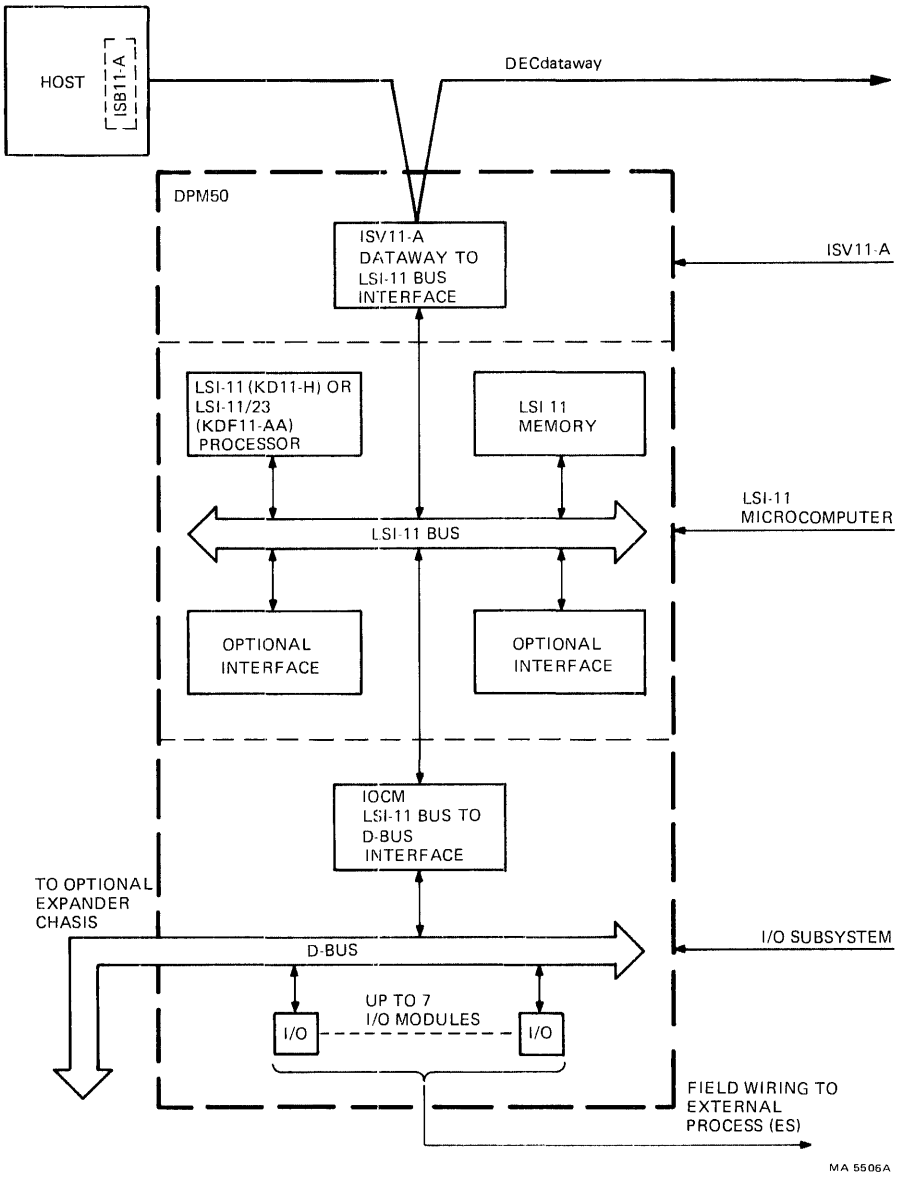


Figure 1-2 DPM50 Detailed Functional Diagram

The I/O Subsystem – interfaces directly to an external process through a variety of digital and analog I/O modules.

The LSI-11 Microcomputer – exercises direct local control over the I/O subsystem by executing user programs stored in its memory. These programs are initially downline loaded from the host computer.

The ISV11-A DECdataway Interface – manages DPM50 communication with the host computer over the DECdataway.

The next three sections describe each of the three main functional areas in detail. Refer to Figure 1-2 throughout the discussion.

1.2.2.1 I/O Subsystem – The I/O subsystem is capable of monitoring and controlling a wide range of industrial processes. Applications range from simple monitoring functions to controlling complex closed-loop systems. This flexibility is provided by the wide range of digital and analog I/O modules available. I/O modules are available to perform the following functions.

Input Sensing	Outputs Provided
DC voltages	DC switching
AC voltages	AC switching
Change of state	One-shot dc switching
Contact closure	D/A conversions
A/D conversions	Pulse trains
Event counting	
Frequency measurement	

All I/O modules in the DPM50 share a common bus; the D-bus (Figure 1-2). The D-bus, in the DPM50 master chassis, can accommodate up to seven I/O modules. It can be extended through the optional H334 expander chassis to add up to 70 I/O modules. This makes the DPM50 capable of being configured with up to 77 I/O modules. Connections between I/O modules and field wiring of external processes are generally made at screw terminal strips mounted on an H332 chassis.

The LSI-11 microcomputer (Figure 1-2) provides control over the D-bus through the M7958 I/O Control Module (IOCM). This module interfaces the LSI-11 bus to the D-bus. The IOCM accepts command signals from the LSI-11 microcomputer and generates D-bus signals for routing data to and from the I/O modules.

Refer to the *I/O Subsystem User Guide* for more detailed information about the I/O subsystem, the IOCM, and the I/O modules.

1.2.2.2 LSI-11 or LSI-11/23 Based Microcomputer – The LSI-11 microcomputer directly controls the I/O Subsystem as described in the previous paragraph. The DPM50 LSI-11 microcomputer is based upon either an LSI-11 (KD11-H) processor or an LSI-11/23 (KDF11-A) processor (Figure 1-2).

NOTE: To avoid confusion, the following conventions are followed in this user guide.

- *The term LSI-11 microcomputer refers to the entire microcomputer system, regardless of its processor.*
- *When a distinction is made between processors, the option designation (KDXXX-X) is always presented.*

The LSI-11 microcomputer exercises direct local control over the D-bus by executing user programs stored in its local memory. Within the DPM50 master chassis, space is provided in the LSI-11 bus backplane for adding optional interface modules (Figure 1-2). This allows local terminals and/or floppy disk mass storage units to be added to the system.

Complete information regarding the LSI-11 Microcomputer family of products is presented in the *Microcomputer Processor Handbook* and the *Microcomputer Interfaces Handbook*.

1.2.2.3 DECdataway Interface – The ISV11-A is an intelligent DECdataway interface. It manages DPM50 communications with the host computer over the DECdataway. It performs the following functions.

1. It facilitates downline loading of the RSX-11S operating system (with built-in tasks) into the LSI-11 microcomputer memory. (Refer to Section 1.4).

2. It starts or halts the LSI-11 microcomputer in response to commands from the host.

3. It allows bidirectional block transfers of information between the host and LSI-11 memory.

4. Upon power-up or in response to a host command, the ISV11-A runs ROM resident diagnostic tests on itself and the LSI-11 CPU (processor and memory). (Refer to Chapter 3.)

Figure 1-3 shows a detailed view of the ISV11-A and its relationship to the host computer and the rest of the DPM50. Through an *ISB11-A* controller, the host communicates over the dataway with the *ISV11-A*. The heart of the ISV11-A is an eight-bit microprocessor. This microprocessor executes a microprogram resident in 5K bytes of onboard read-only memory (ROM). It also uses 1K of random access memory (RAM) for stacks and local storage (Figure 1-3). Communication with the host/DECdataway is handled by the microprocessor through a serial line unit based on an LSI synchronous communications chip. It is called a USYNRT (Universal Synchronous Receiver/Transmitter).

The controlling element in the process I/O portion of the equipment is the LSI-11 microcomputer. Communication between the ISV11-A internal bus and the LSI-11 bus is through an interface in the ISV11-A. The microprocessor and the LSI-11 can interrupt each other and swap specific information through shared I/O registers in the LSI-11 bus interface. However, the principal means of communication is the transfer of information between LSI-11 memory and internal registers in the microprocessor. This transfer is under microprocessor control via DMA logic in the interface. Therefore, data from the host moves over the dataway, under microprocessor control through the serial line unit, internal microprocessor registers, LSI-11 bus interface, and eventually to LSI-11 memory. Once data

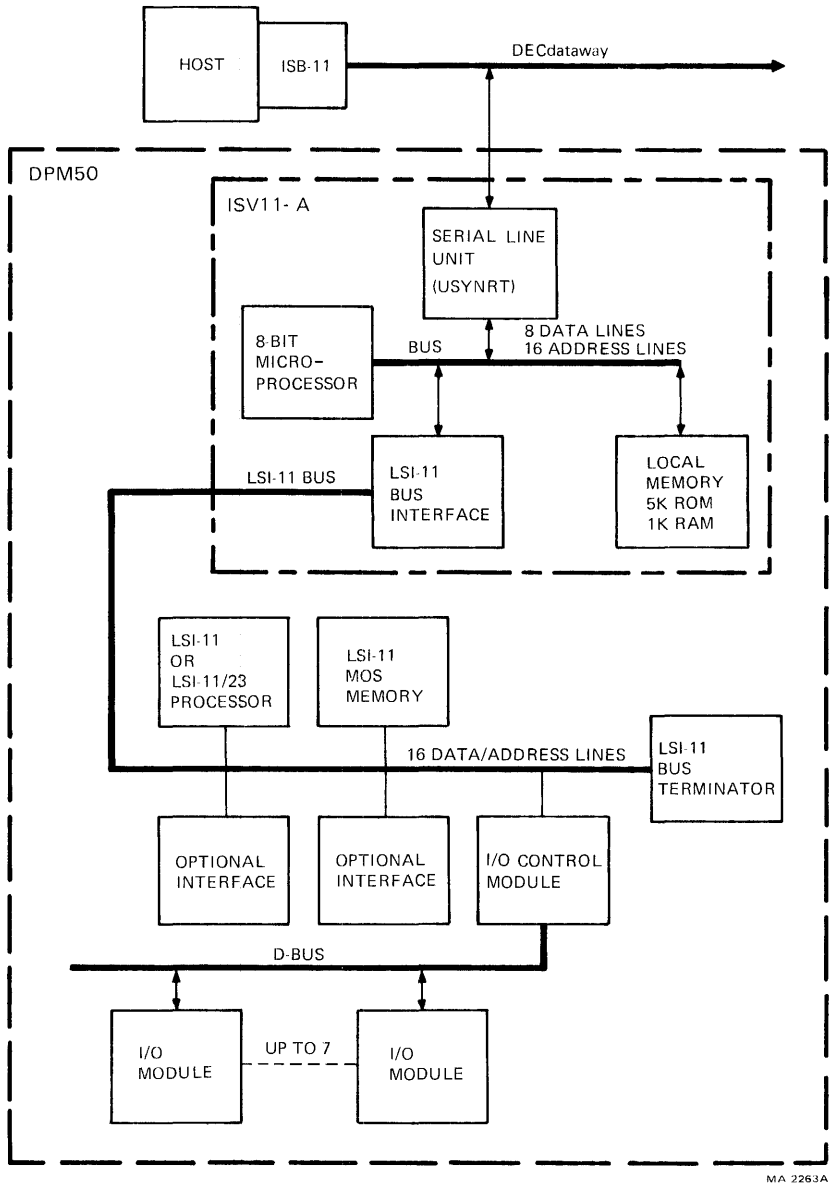


Figure 1-3 The ISV11-A in a DPM50 Subsystem

is there, the LSI-11 microcomputer can execute the data or operate on it. Data from the remote makes its way back to the host via the reverse route.

As stated earlier, there are 63 addresses available for ports on the dataway (address zero is not used). Each DPM50 uses a consecutive pair of these addresses. The lower address is wired into the dataway port connector. From there it can be read by the ISV11-A microprocessor. Since an ISV11-A uses two consecutive addresses, the highest address that can be wired into a connector is decimal 62. Reading address 63 in the

connector (octal 77, hex 3F) indicates to the 8-bit microprocessor that the ISV11-A is off-line (disconnected from the DECdataway). Although the dataway is half-duplex, using two addresses allows the ISV11-A to appear as a full-duplex channel to tasks running on the host and remote processors. This is useful because there can be both a read request and a write request outstanding at the same time. Which address is used for which transaction is determined by higher level software.

A technical description of the ISV11-A is presented in Chapter 4 of this user guide.

1.3 PHYSICAL DESCRIPTION

The principle DPM50 standard components are as follows.

- H333 master chassis with an H7870 power supply and an I/O control module (LSI-11 bus to D-bus interface)
- LSI-11 (KD11-H) or LSI-11/23 (KDF11-AA) processor
- MOS random-access memory (minimum 32K word)
- ISV11-A DECdataway Interface

1.3.1 Standard Versions of the DPM50

Currently there are two standard versions of the DPM50. Each is offered in a 115 Vac or 230 Vac input power configuration. Table 1-1 details the variations.

Figures 1-4 and 1-5 show the physical arrangement of the components within the H333 master chassis for the two standard versions.

For more detailed information about the H333 master chassis, the I/O modules, and the IOCM refer to the *I/O Subsystem User Guide*.

1.3.2 Controls, Fuses, Indicators

The H333 master chassis front panel controls and indicators are on the H7870 power supply (Figure 1-6). Table 1-2 details their functions.

Figure 1-7 shows the five LED indicators on the M7958 IOCM. For more information about these indicators, refer to Chapter 3 of the *I/O Subsystem User Guide.*

There are five LED indicators on the ISV11-A module. Refer to Figure 3-2 and Section 3.5.1 of this manual for their location and function respectively.

Table 1-1 DPM50-XX System Configuration

	DPM50-XX			
Standard Equipment	**-AA, -CA**	**-AB, -CB**	**-FA, -HA**	**-FB, -HB**
H333A master chassis 115 Vac	X		X	
H333B master chassis 230 Vac		X		X
M7958 I/O control module (IOCM)	X	X	X	X
KD11-H LSI-11 microprocessor (with KEV-11)	X	X		
KDF11-A LSI-11/23 microprocessor			X	X
MSV11-DD 16 bit × 32 Kw MOS memory	X (Note 1)	X (Note 1)	X	X
ISV11-A DECdataway to LSI-11 bus Interface	X	X	X (Note 2)	X (Note 2)
TEV-11 LSI-11 bus terminator	X	X	X	X

NOTE 1: Originally shipped with two MSV11-CD 16 bit × 16K MOS Memory Modules

NOTE 2: The ISV11-A must have ECO Rev 4 incorporated to operate in the DPM50-Fx and -Hx versions.

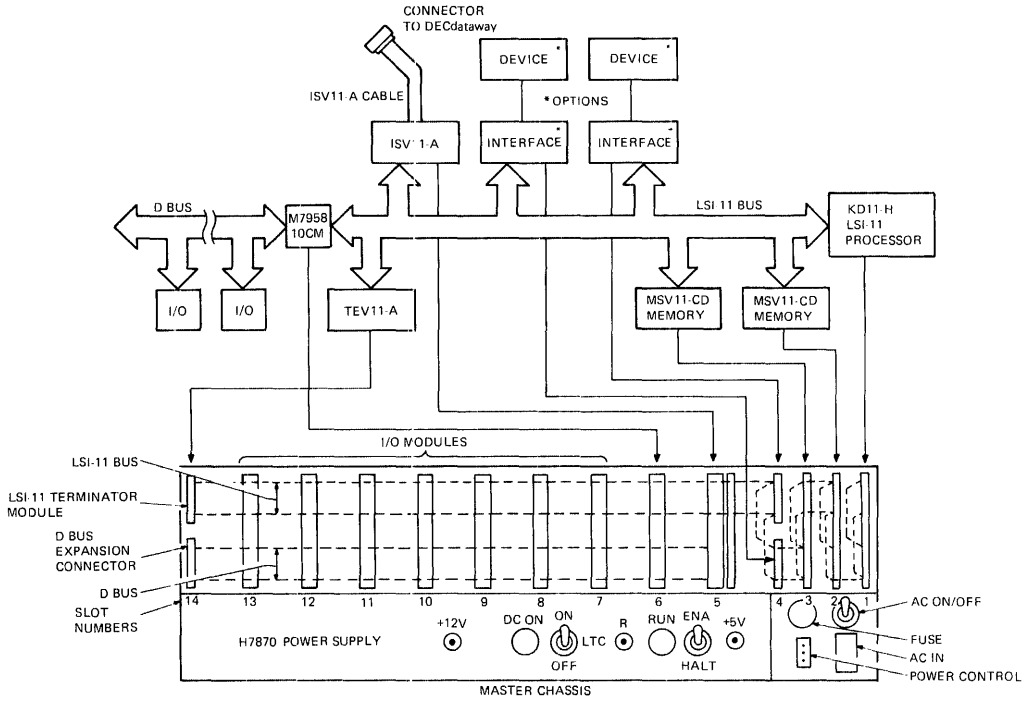
1.3.3 Hardware Options

The following hardware options are available for all current versions of the DPM50.

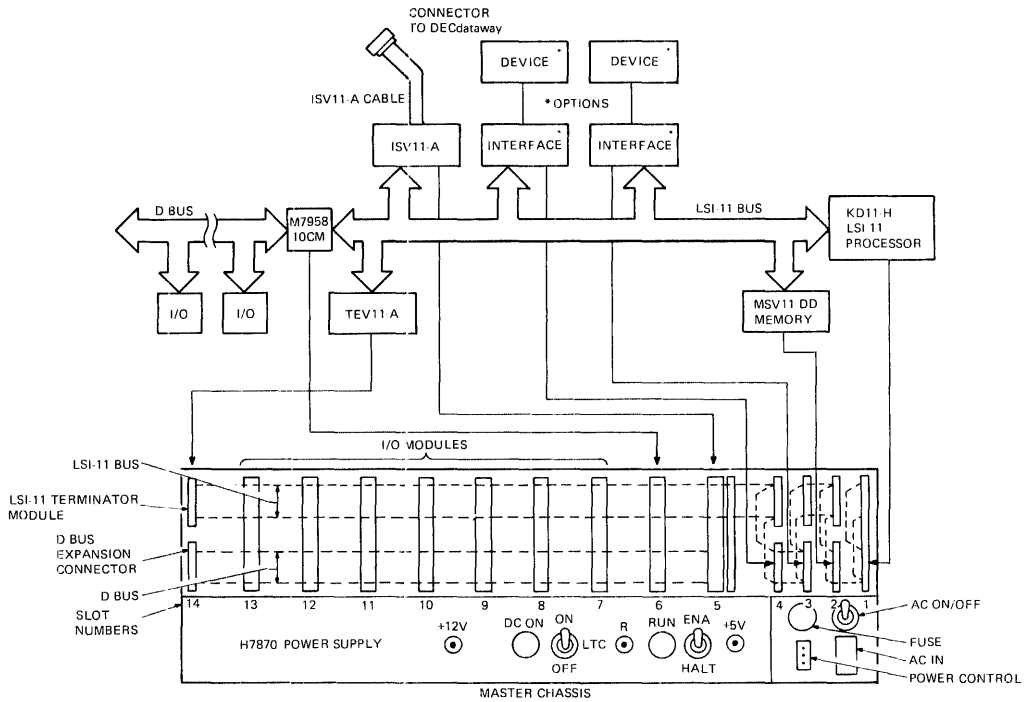
- Cabinetry - The DPM50 is a cabinet or rack mountable device. Typical cabinets used for DPM50 mounting are DEC H960-C cabinets and NEMA-12 cabinets.

- I/O Modules - A wide variety of analog and digital input and output modules is available for the DPM50.

- H334 Expander Chassis - This chassis is an extender chassis for the D-bus and can accommodate up to 10 I/O modules. A single DPM50 subsystem can accommodate up to seven (7) H334 expander chassis. This gives the DPM50 a total capacity for 77 I/O modules.



(A) EARLY SHIPMENTS



(B) CURRENT SHIPMENTS

NOTE:
A G7272 CONTINUITY MODULE MUST BE INSTALLED IN ANY UNUSED SLOT BETWEEN THE PROCESSOR AND THE ISV11-A.

MA-2261H

Figure 1-4 DPM50-Ax, -Cx Physical Layout

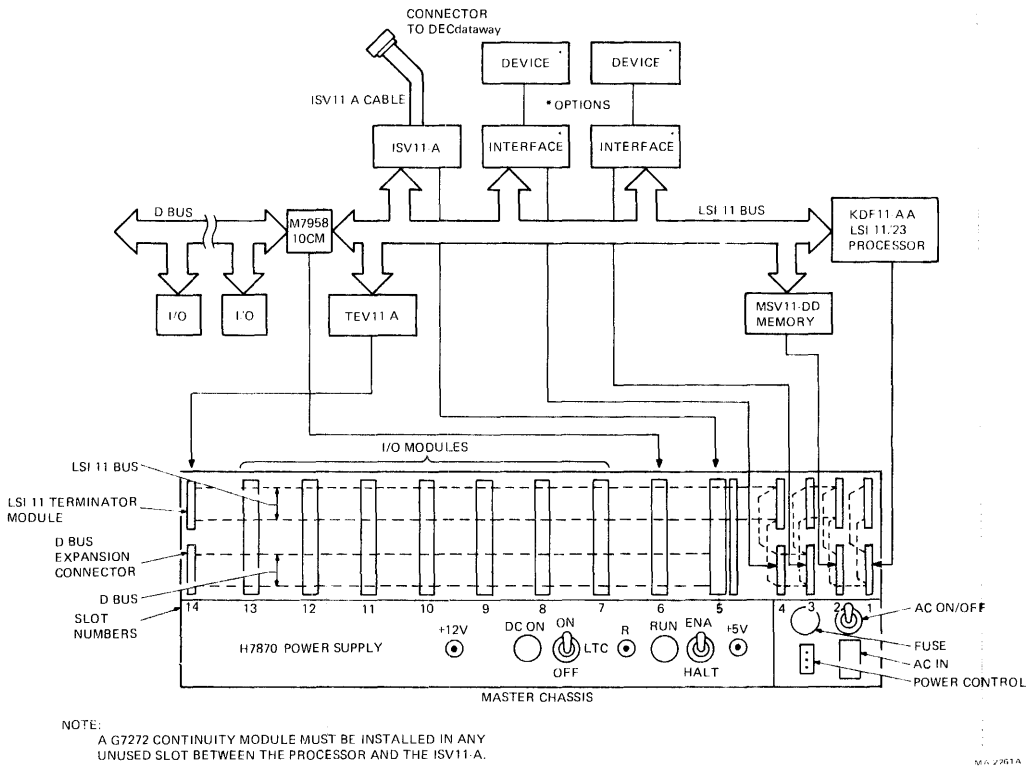


Figure 1-5 DPM50-Fx, -Hx Physical Layout

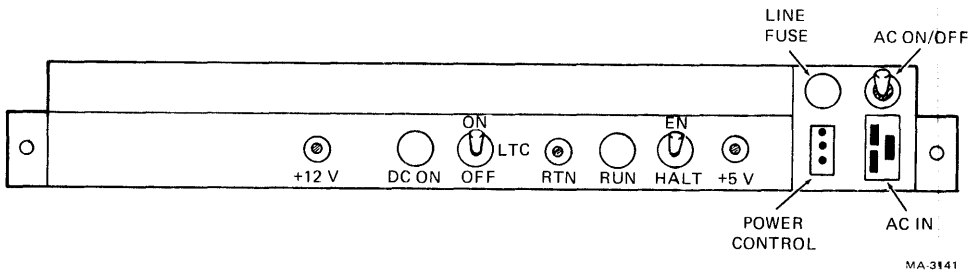


Figure 1-6 H7870 Power Supply

- H332 Mounting Rack with Terminal Strips - This provides a convenient point for connections between I/O modules and field wiring of external processes.

- H7006-A/B Filter Panel - This provides EMI filtering for serial interface cabling (20 mA or EIA RS232C) connecting the LSI-11 to modems or terminals outside the DPM50 cabinetry.

For information concerning the options listed previously (except the H7006-A/B Filter Panel), refer to the *I/O Subsystem User Guide*. Section

Table 1-2 H7870 Switches and Indicators

Switches and Indicators	Function
AC ON/OFF switch	Applies ac power to the H7870 and activates power control outlet
Line fuse	Protects against ac line overload; fuse rating is 6.25 A for 115 V operation, or 3 A for 230 V operation
Power control outlet	When connected to power control bus, ties ac power ON/OFF control of all power controllers to ac ON/OFF switch of the H333 chassis
Ground lug	Provides safety ground connection to power supply chassis
LTC switch	When on, enables B EVNT L which is an LSI-Bus compatible line frequency signal generated by the H7870 - must be on for normal operation
ENA/HALT switch	When on, enables program execution by the LSI-11; when off it places the processor in halt mode - must be in the ENA position for normal operation
DC ON indicator	Lights to indicate that dc power is on - should light when ac ON/OFF switch is turned on
RUN light	Lights to indicate that LSI-11 processor is running
+5 V test point	Measures +5 Vdc output
+12 V test point	Measures +12 Vdc output
RTN test point	Meter return for dc voltage measurement

2.4.3 of this manual provides H7006-A/B Filter Panel configuration and installation information. For information concerning the following options refer to the *Microcomputer Interfaces Handbook*.

The following options are available for the DPM50-AA, AB, CA, and CB versions. (Refer to Section 2.4 of this manual for option selection guidelines.)

- DLV11, DLV11-F, or DLV11-J Asynchronous Line Interface and associated terminals (because of cabling requirements the DLV11-J can be used only with the DLV11-KA option)
- DZV11-B Asynchronous Multiplexer Interface
- RXV21 or RXV11 dual-drive floppy disk system (requires the REV11 option for local boot capability)

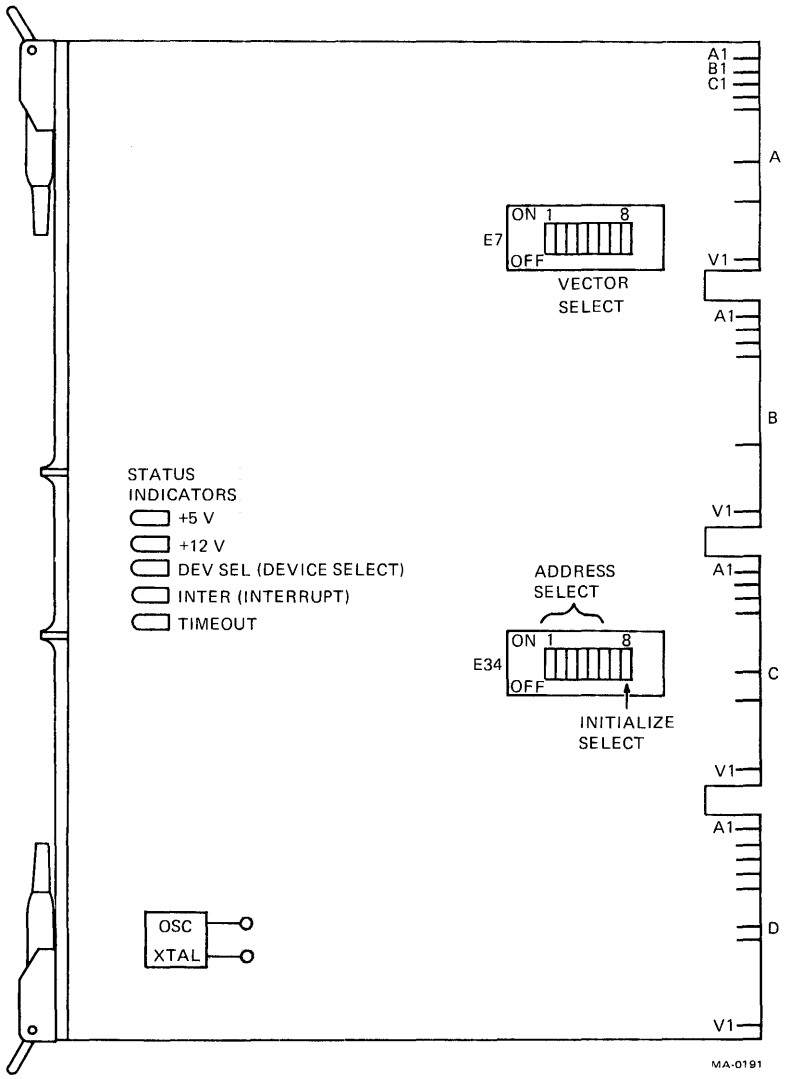


Figure 1-7 M7958 I/O Control Module

The following options are available for the DPM50-Fx and -Hx versions. (Refer to Section 2.4 of this user guide for option selection guidelines.)

- DLV11-F or DLV11-J Asynchronous Line Interface and associated terminal(s) (the DLV11-J can be used only with the DLV11-KA option)
- DZV11-B Asynchronous Multiplexer Interface
- RXV21 or RXV11 dual-drive floppy disk system (for local storage only with no local boot capability)
- An additional MSV11-DD 32KW MOS memory module

1.4 SOFTWARE

The host software is based on the RSX-11M or M-Plus real time operating system. The LSI-11 microcomputer in each DPM50 subsystem uses the RSX-11S operating system. Both have software extensions to allow full use of the Distributed Plant Management system.

Additional software at the host includes a device driver for the DECdataway and operating software to handle the following functions related to the DPM50.

1. Downline System Load
   The downline control task (DLC) is callable at the host through the monitor console routine (MCR). It allows the user to download a system image to a DPM50 and initialize host-remote communication.

2. Upline Crash Dump
   Another MCR-callable task, upline dump (ULD), allows the user to bring the DPM50 system image to a disk file at the host. It is stored there for later analysis by the RSX-11M crash dump utility.

3. Interactive Program to Program Communication
   An ancillary control processor (ACP) manages a single program-to-program connection between the host and each remote. A host program written in MACRO-11 (QIO interface) or FORTRAN IV + (CALL interface) can communicate with a user program in a DPM50 using ACP.

DPM50 diagnostic and maintenance software is discussed in Chapter 3. Additional software for the LSI-11 microcomputer in the DPM50 includes the following.

- ISV11-A DECdataway driver
- Complete support for the complement of process I/O modules
- Language support for MACRO-11 and FORTRAN IV+
- ACP to support the program-to-program link to the host

1.5 SPECIFICATIONS

Specifications for all LSI-11 microcomputer components in the DPM50 are provided in the *Microcomputer Processor Handbook* and the *Microcomputer Interfaces Handbook*.

Specifications for the remaining DPM50 components except the ISV11-A are provided in Section 1.4 of the *I/O Subsystem User Guide*. Specifications for the ISV11-A are provided in Table 1-3.

Table 1-3 ISV11-A Specifications

Features	Specifications
CSR addresses	160140, 160142, 160144
Interrupts	LSI-11 vector locations 300 and 304
Local memory in bytes	5K ROM (plus socket and address decoding for another 1K), 1K RAM
Port addresses assigned	Two consecutive, lower wired into connector on DECdataway
LEDs	M8080 — four programmable 54-13290 — modem dropout
Modem-dataway interface	
Operating mode	Half duplex
Data format	Synchronous, serial, LSB first
Character size	8 bits (contains 0-2 stuffing bits)
Data rate	55,556 bits-per-second
Transmission technique	Biphase modulation
Transmitter timing	Crystal clock
Receiver timing	Derived from received signal
Line interface	Transformer coupled
Transmitted signal	5 V p-p into terminated 200 ohm cable
Receivable signal threshold	150 mV p-p minimum
Error-free signal level	300 mV p-p minimum
Common mode isolation	350 Vac rms, 500 Vdc
Receiver bandpass	6 KHz to 130 KHz (-3 dB points)

The ISV11-A places one dc and four ac loads on the LSI-11 and has the following maximum current requirements.

+5 V	3.0 A
+12 V	0.37 A

1.6 DOCUMENTATION

The following documents are shipped with the DPM50.

DPM50 User Guide	EK-DPM50-UG
I/O Subsystem User Guide	EK-0PIOS-UG
KDF11-AA User's Guide	EK-KDF11-UG
Microcomputer Interfaces Handbook	EB-17723-20
Microcomputer Processor Handbook	EB-15836-18
LSI-11/23 Programming Card	EH-17898-20
LSI-11 Programming Card	EH-07043-53
MSV11-D, -E User's Manual	EK-MSV1D-OP
ISV11 Field Maintenance Print Set	MP00609

MSV11-D Field Maintenance Print Set	MP00566
H333 Field Maintenance Print Set	MP00424
KDF11-A Field Maintenance Print Set	MP00734
KD11-S Field Maintenance Print Set	MP00433
TEV11 Field Maintenance Print Set	MP00074

The following related documents can be purchased from Digital Equipment Corporation. Information on where to order these documents follows this list.

DPM50 Diagnostic User Guide	EK-DPM00-DM
DECdataway User's Guide	EK-ISB11-UG
Serial Bus Exerciser Writeup	MD-11-CZKCH-D
Remote Terminal Tester Writeup	MD-11-CZKCI-D
Diagnostic Monitor Writeup	MD-11-CZKMP-D
CVPCAD0 Process Control Subsystem Writeup	AC-A959D-MC
DPM/DPM-PLUS Documentation Set Consists of four manuals:	QJ651-GZ
DPM/DPM-PLUS DECdataway Intelligent Subsystem User Guide	AA-J529A-TC
DPM/DPM-PLUS Terminal User Guide	AA-J530A-TC
DPM/DPM-PLUS System Generation and Management Guide	AA-J531A-TC
DPM/DPM-PLUS Release Notes	AA-J906A-TC

For additional references refer to Section 1.5 in the *I/O Subsystem User Guide,* the *RSX-11M/RSX-11S Documentation Directory* (AA-2593E-TC) and the *RSX-11M-Plus Documentation Directory* (AA-H426A-TC).

These documents can be ordered from the following address.

Digital Equipment Corporation
444 Whitney Street
Northboro, Mass. 01532

Attn: Communication Services (NR2/M15)
Customer Services Section

For information concerning Microfiche Libraries, contact the following group.

Digital Equipment Corporation
Micropublishing Group
BU/D2
Bedford, Mass. 01730

CHAPTER 2
INSTALLATION

2.1 OVERVIEW

The DPM50 process I/O subsystem, with the addition of an ISV11-A DECdataway interface, is similar to an IP300 process I/O subsystem. Therefore, most site preparation and installation information for the DPM50 is in the latest *I/O Subsystem User Guide* (EK-0PIOS-UG). Chapter 3 of that manual describes unpacking, inspection, installation, configuration, and checkout procedures for a complete process I/O subsystem. However, there are subtle differences between some versions of the DPM50 and the IP300. Therefore, this chapter supplements the *I/O Subsystem User Guide* by providing configuration and installation information in the following areas.

H333	Section 2.2
Cabinetry	Section 2.2.2
ISV11-A	Section 2.3
LSI-11 Bus	Section 2.4.1
LSI-11 Bus Modules	Section 2.4.2
D-Bus	Section 2.5

The port connector on the DECdataway is of special interest to someone installing the DPM50. The ISV11-A cable plugs into this connector. The connector is wired with the lower of the two port addresses that the ISV11-A responds to. For information on configuring the DECdataway port connector refer to Chapter 3 of the *DECdataway User's Guide* (EK-ISB11-UG).

2.2 H333 INSTALLATION

The first part of this section gives general information applicable to all installations. The remaining three parts give specific information about systems delivered in DIGITAL cabinets or mounted in NEMA enclosures or other customer enclosures.

2.2.1 General Considerations

Every cabinet used for mounting any equipment in a system must be properly grounded. The correct procedure is described in Section 1, Chapter 3 of the *Digital Site Preparation Guide* (EK-0CORP-SP).

Any enclosure or free-standing piece of equipment must be situated for easy access and maintenance by Field Service. There must be good lighting and ample working space around the equipment. Wall-mounted enclosures must be a reasonable height above solid, safe, and roomy walkways. The site must also provide service outlets for scopes and other maintenance equipment.

In the H333 there is a filter on the power line in the H7870 power supply. In a standard DIGITAL installation, additional filtering is provided by an 861 series power controller. This controller has switched outlets that can be used for other system units (terminal or disk) provided they are always powered on and off with the H333. Other equipment (scopes, maintenance gear, or system units that can be turned on or off independently of the H333) should use independent outlets like the unswitched ones on the 861. Better yet, such equipment should have its own separate filter.

The power checkout procedure in Section 3.4.1 of the *I/O Subsystem User Guide* indicates that supply voltages should be within three percent of their nominal values. However, because of the ISV11-A present in the DPM50, the +5 V supply output must be adjusted to +5.1 V. To do this follow instructions in Section 7.4.1 of the *I/O Subsystem User Guide*. Also, for normal operation the LTC and HALT/ENA switches on the front panel of the supply must be up (ON and ENA, respectively).

2.2.2 DIGITAL Cabinet Installation

When a system is ordered in DIGITAL cabinets, all equipment is already configured as shown in several illustrations in Chapter 3 of the *I/O Subsystem User Guide*. The ISV11-A cable is not shown in that manual. This cable passes through the top of the H333 chassis and its dataway connector mounts on a bracket at the back of the cabinet (Figure 2-1).

2.2.3 NEMA Installation

Directions for installing the H333 and similar chassis in a NEMA enclosure are given in Section 3.3.5 of the *I/O Subsystem User Guide*. The bracket holding the dataway connector on the end of the ISV11-A cable must be on an enclosure wall within 75 cm (30 inches) of the right side of the H333 (Figure 2-1). Mounting requires a pair of holes for 10-32 hardware 0.554 cm diameter, drilled 4.445 cm apart (0.218 inches diameter, drilled 1.75 inches apart). Bracket location is unimportant as long as there is enough clearance to connect the DECdataway port connector.

The H333 master chassis, each H334 expander chassis, and each H332 screw-terminal chassis has a ground strap on the right side. Every one of these ground straps must be electrically well-connected to the cabinet.

Although the RX01 and RX02 floppy disk systems are standard options for the DPM50, DIGITAL does not supply hardware for mounting it in a NEMA cabinet. Customers must provide their own mounting bracket.

2.2.4 NEMA Power Dissipation Considerations

A circulating fan with a minimum capacity of 500 CFM must be mounted in

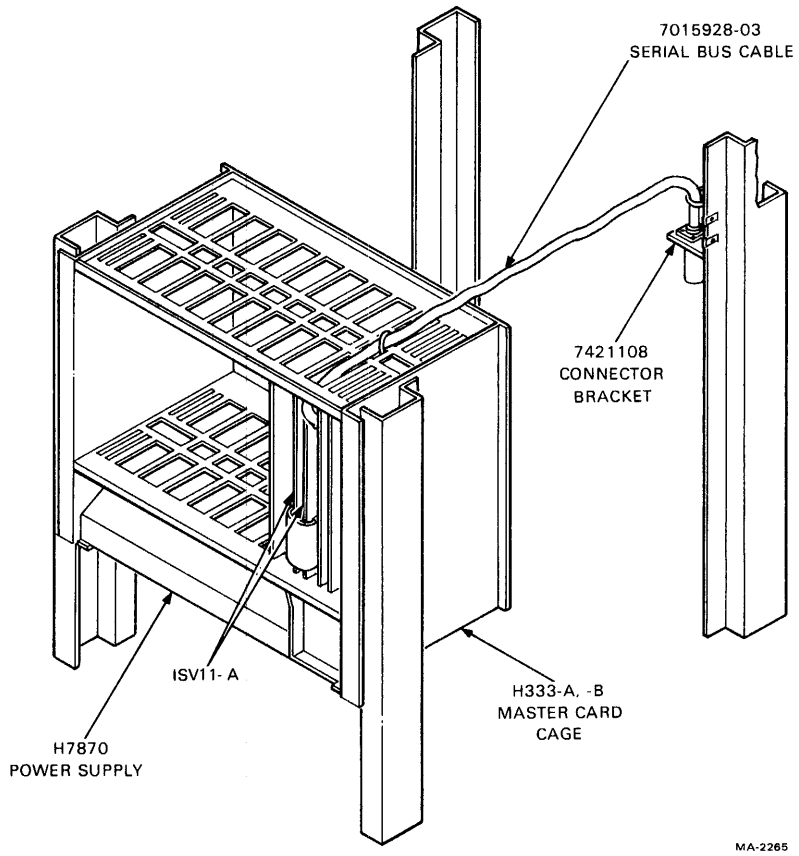


Figure 2-1 DECdataway Connector Mounting

the enclosure. An appropriate model is the Caravel 115 Vac, 550 CFM, DEC P/N 12-04826.

A typical NEMA-12 enclosure with a fan (6 feet × 5 feet × 1 foot) can be used to house an H333 and one H334. When there are two chassis in the enclosure, the H333 should be at the bottom in the cooler circulating air. Nothing else can be mounted in the box unless it is equipped with a heat exchanger or air conditioner (both standard NEMA accessories). Even then the remaining space should be used only for legitimate DPM50 options, expansion chassis for I/O modules, or screw-terminal chassis for field wiring. No other equipment should be mounted in the box. Power dissipation of the enclosed units should never exceed 18 watts per square foot of uninsulated enclosure surface unless special equipment is installed to remove excess heat. The temperature of air circulating into the LSI-11 area must never exceed 60°C.

Heat produced in a NEMA cabinet can only dissipate through the walls of the enclosure because the cabinets are totally enclosed, and lack external ventilation. The rate of heat loss through the cabinet walls is a direct function of the temperature difference between inside the cabinet and ambient temperature outside the cabinet. Maximum operating temperature

for electronic equipment (LSI, memory, and other modules) inside the cabinet is restricted to 60°C (140°F). Therefore, the maximum ambient temperature in which a NEMA-12 cabinet can be safely operated is also limited by the following considerations.

1. Total heat (P) produced by all electronic equipment inside the cabinet

2. Total cabinet surface area available for heat dissipation

Therefore, a user considering factory floor installation for the DPM50 in a NEMA-12 cabinet, must calculate the temperature limit within which the system can be safely installed. For NEMA cabinets DIGITAL has tested, the following empirical relation holds true for the DPM50.

$$P_{max} = 2 \times A\,(T_1 - T_2)$$

Where:

P_{max} = Heat produced by all the electronics equipment inside the cabinet expressed in Btu/hr

A = Area of cabinet available for heat dissipation

T_1 = Maximum allowable temperature for the electronics for any member of the I/O subsystem family ($T_1 = 60°C$)

T_2 = Maximum ambient temperature where a NEMA-12 cabinet is to be installed (°C)

For the cabinet under consideration (6 feet $\times$ 5 feet $\times$ 1 foot) the surface area is 82 square feet. If the cabinet is mounted against a wall or otherwise obstructed on one 6 feet $\times$ 5 feet side, the surface area available for heat dissipation is 52 square feet.

For any given application, P_{max} (the heat produced by the DPM50 subsystem) is calculated by adding the heat produced by the following things.

1. All I/O modules (See detailed module specifications in the *I/O Subsystem User Guide* and use only the heat dissipation specified as "due to field power source")

2. The power supply (See power supply specifications in *I/O Subsystem User Guide)*

3. The circulating fan (180 Btu/hr)

For some devices, the heat specification is only available in watts (1 watt = 3.41 Btu/hr).

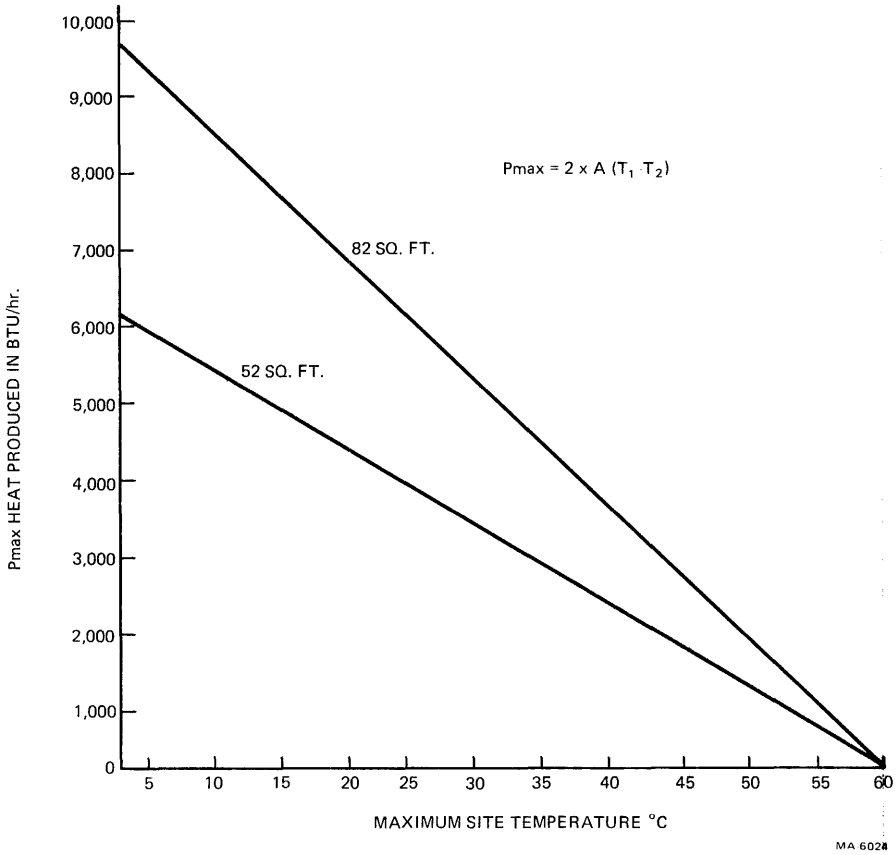


Figure 2-2 Cabinet Heat vs Site Temperature

Figure 2-2 shows the $P_{max} = 2 \times A (T_1 - T_2)$ relationship in graphic form. The curves are drawn to show the two most common cabinet installations, free-standing or against a wall.

When considering a NEMA-12 application for factory floor installation, the total heat produced by equipment in the cabinet must be calculated. Then, using the curve in Figure 2-2, the maximum allowable temperature where the cabinet is being installed can be determined.

For applications where the temperature outside the cabinet exceeds allowable limits, additional cooling is required. NEMA cabinets available for the DPM50 are provided with pipe fittings to allow circulation of clean air for cooling. The compressed air introduced into the cabinet also maintains a positive pressure inside the cabinet. This protects the equipment from dirt, dust, or other corrosive material in the factory environment. Air purging the NEMA cabinet is achieved by connecting an air source to a hole at the bottom of the cabinet, and opening a hole at the top of the cabinet. The air supply should be filtered and oil free. It should also have a shutoff valve to facilitate service, and a pressure relief valve in case the

cabinet exit port becomes obstructed. For a free-standing NEMA-12 installation, the following approximate relation between air flow, air temperature, heat dissipated, and ambient temperature holds true.

$$T_2 = T_1 + \frac{1.8\ A_F\ (T_1 - T_A) - P_{max}}{90}$$

Where:

T_2 = Maximum ambient temperature where the NEMA-12 cabinet is to be installed (°C)

T_1 = Maximum allowable temperature for the electronics for any member of the I/O subsystem family, $T_1 = 60°C$

A_F = Air flow in CFM

T_A = Temperature of purge air (°C)

P_{max} = Maximum heat produced inside the cabinet expressed in Btu/hr

Therefore, a user considering NEMA-12 applications, must calculate what temperature limits will allow reliable operations. These power dissipation relationships were derived under laboratory conditions and should only be used as guides for most normal installations. For NEMA cabinet applications in areas with an abnormal heat source these formulas should be modified to account for the specific environment.

The worst case dissipation for various chassis with all I/O slots filled is as follows.

H333	2493 Btu/hr (713 W)
H334 with power supply	2319 Btu/hr (680 W)
H334 without power supply	955 Btu/hr (280 W)

To determine the exact figure for a particular configuration, refer to the *I/O Subsystem User Guide* (the ISV11-A dissipates about 17 watts).

2.2.5 Other Enclosures

Customers can use any enclosure they want to protect the equipment. The mounting directions are the same as those given for a NEMA enclosure at the beginning of Section 2.2.3. However, when a non-DIGITAL, non-NEMA cabinet is used, the customer must maintain specified environmental conditions, such as the quality of the system ground. In particular, air circulating into the LSI-11 area must not be higher than 60°C.

2.3 ISV11-A CONFIGURATION

Physically the ISV11-A is comprised of two quad-height modules bolted together and connected by a 50-conductor ribbon cable. Figure 2-3 shows

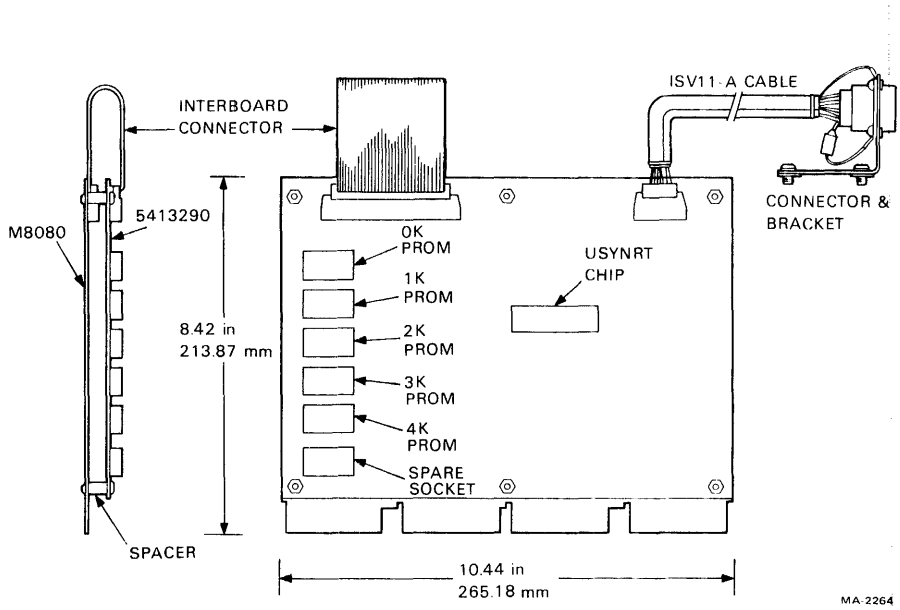


Figure 2-3 ISV11-A Physical Configuration

the two boards joined together, along details of the ISV11-A cable, dataway connector, and mounting bracket. As mounted in the chassis, the M8080 mother board (the one that plugs into the backplane) is on the left. This places the 54-13290 daughter board closer to the LSI-11 processor board. The ISV11-A must always be plugged into slot five of the backplane. (Refer to Figures 2-6 and 2-7 in Section 2.4.1).

All jumpers are set correctly at the factory. However, it is a good practice to verify the configuration at installation time. An in-depth technical description of the ISV11-A is presented in Chapter 4 of this manual.

Both ISV11-A boards have a number of jumpers that are factory installed for proper DPM50 operation. The jumper configuration on both boards is as follows.

M8080 In: W7, W8, W9, W10, W17, W18, W19, W20
Out: All others

Jumpers	**Use**
W1-8, W12, W13	LSI-11 bus address
W9-11, W14, W15	Vector address
W16	Hold on B SACK L
W17, W20	DMA timers
W18, W19	Connect pins
W21-23	Reserved

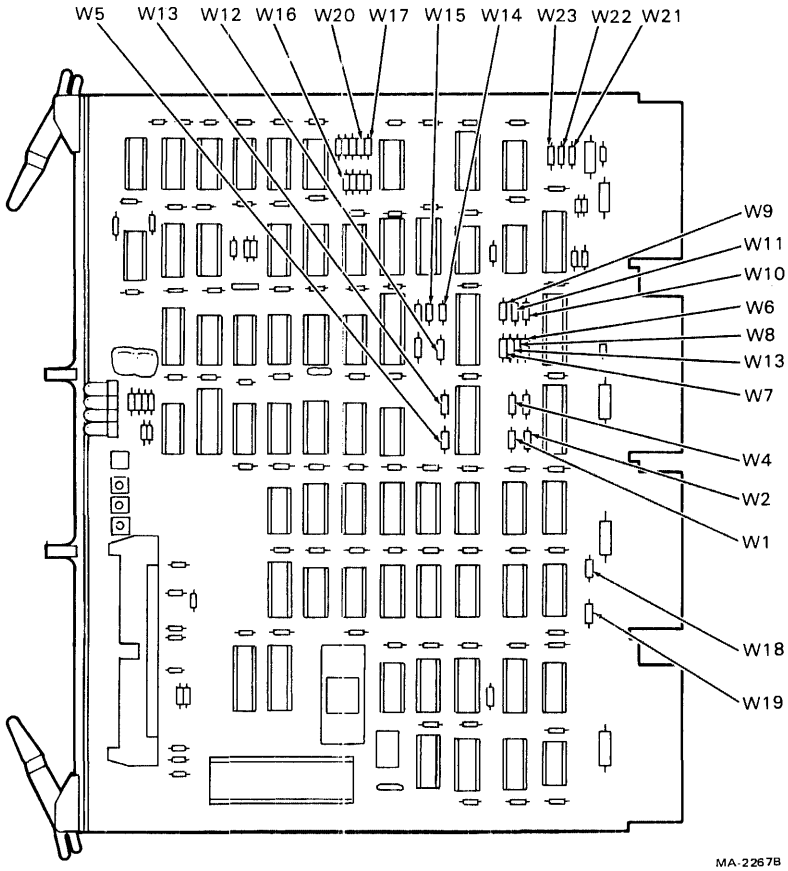


Figure 2-4 M8080 Board

54-13290 In: W1, W3, W5, W7, W9
Out: All others

Jumpers	Use
W7, W8	PROM selection
W1-W6, W9, W10	PROM power

Figures 2-4 and 2-5 locate the jumpers for M8080 and 54-13290 respectively.

2.4 LSI-11 MICROCOMPUTER CONFIGURATION

The LSI-11 modules must be configured correctly for proper DPM50 operation. System configuration refers to the position of the LSI-11 modules within the LSI-11 backplane, as well as switch and jumper settings on the modules themselves. This section assumes a basic familiarity with the LSI-11 bus. The reader who wants an in-depth discussion of the LSI-11 should refer to the *Microcomputer Processor Handbook* (EB-15836-18).

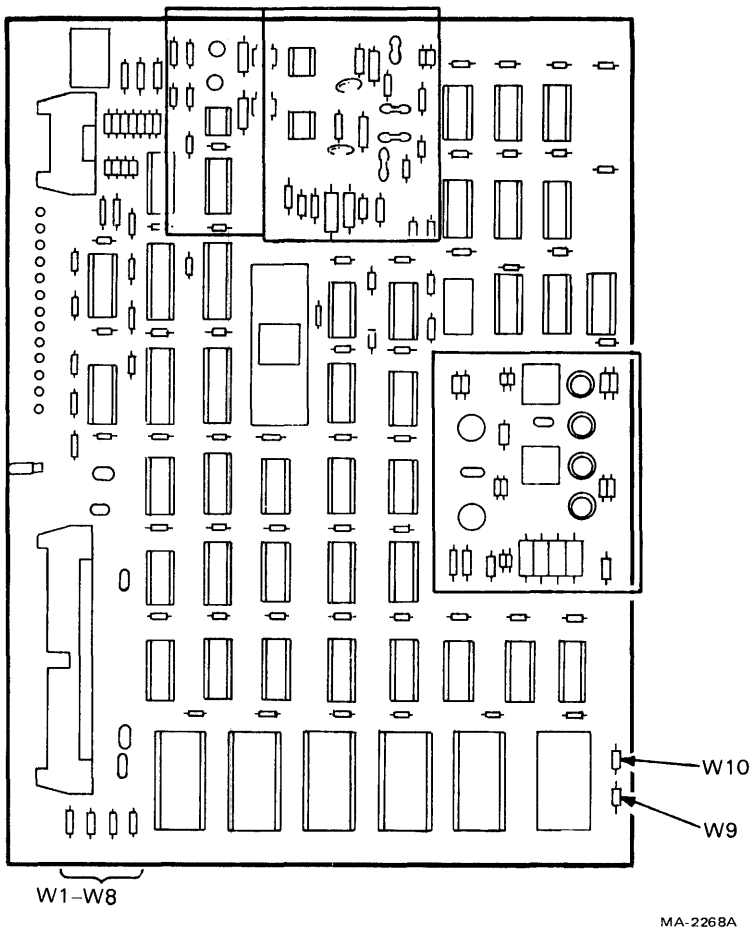


Figure 2-5 54-13290 Board

2.4.1 LSI-11 Bus Backplane Configuration

The recommended placement of LSI-11 modules in the LSI-11 backplane is shown in Figures 2-6 and 2-7. Figure 2-6 shows placement of these modules in the DPM50-AA, -AB, -CA, or -CB models. Some earlier versions of these models were shipped with MSV11-CD MOS memory modules. The early version is shown in Figure 2-6A. The current version is shown in Figure 2-6B. Standard equipment for these models include the following features.

- KD11-H (M7264-YA, -YC) LSI-11 CPU with the KEV11-A floating point option
- MSV11-DD (M8044-D) 32K × 16-bit MOS memory
- TEV11 (M9400-YB) LSI-11 Bus Terminator

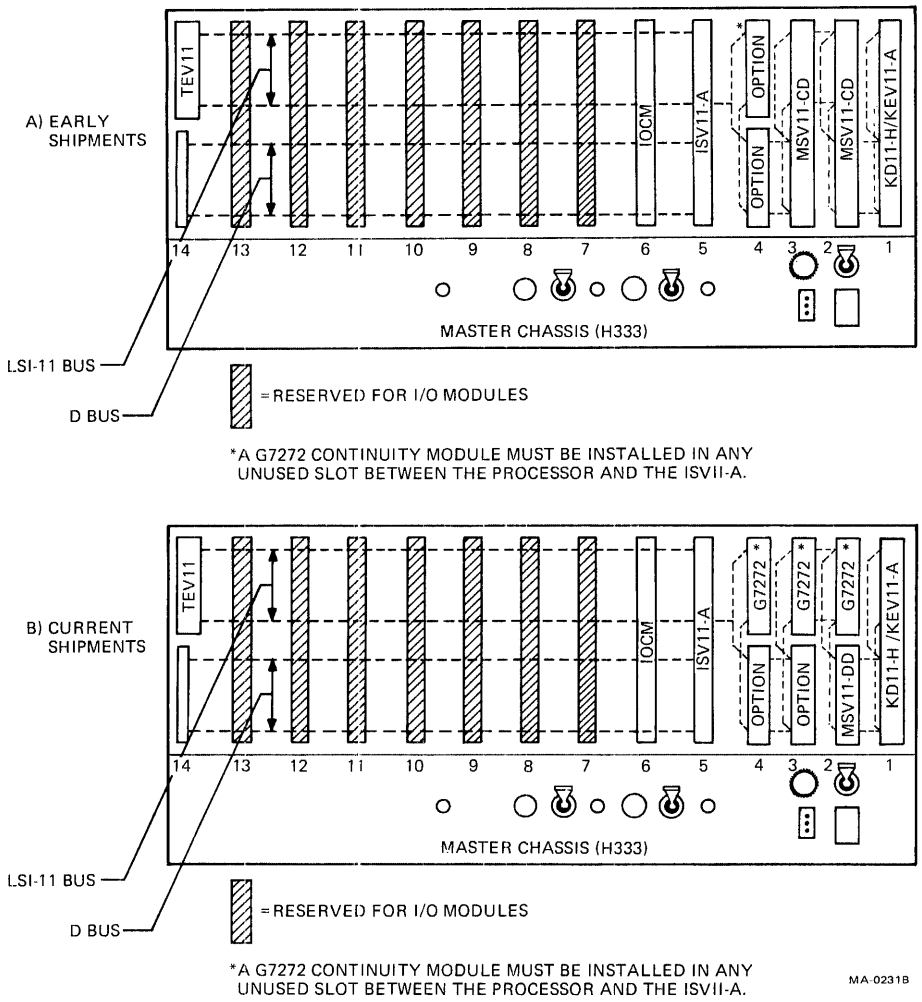


Figure 2-6 DPM50-AA, -AB, -CA, -CB, LSI-11 Module Placement

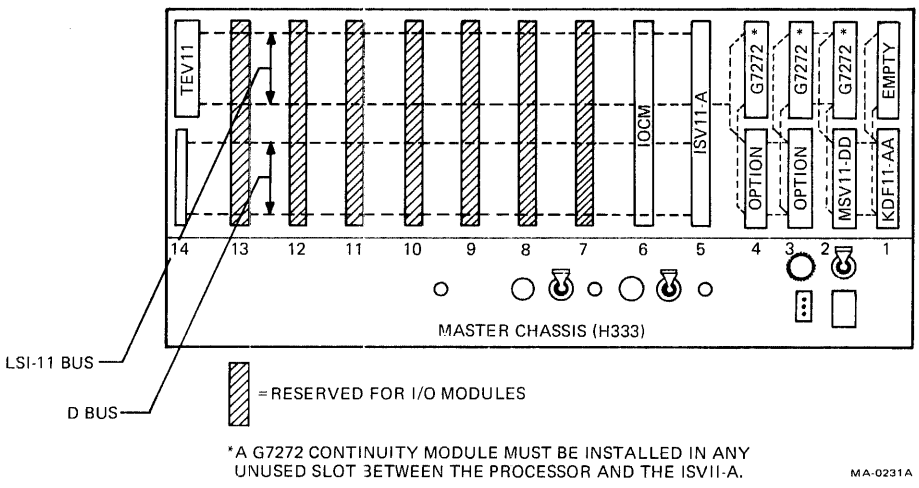


Figure 2-7 DPM50-FA, -FB, -HA, -HB LSI-11 Module Placement

The DPM50-AA, -AB, -CA, and -CB supported options (one from each category) are as follows.

- DLV11, DLV11-F, or DLV11-J Asynchronous Line Interface (because of cabling requirements the DLV11-J can only be used with the DLV11-KA option) - Field Service requires this interface for terminal connection to run local diagnostics.

- RXV11 or RXV21 Dual Drive Floppy Disk System - When this option is selected the TEV11 can be replaced with a REV11 to provide local boot capability.

The recommended placement of LSI-11 modules in the DPM50-FA, -FB, -HA, and -HB models is shown in Figure 2-7. Standard equipment for these models include the following features.

- KDF11-AA (M8186) LSI-11/23 CPU - This can be upgraded with the KEF11-A floating point chip hardware option.

- MSV11-DD (M8044-D) 32K × 16-bit MOS Memory

- TEV11 (M9400-YB) LSI-11 Bus Terminator

The DPM50-FA, -FB, -HA, and -HB models support up to two (2) of the options listed below. However, Field Service requires an asynchronous line unit to connect a terminal for diagnostic purposes. Therefore, if more than one option is desired, one must be an asynchronous line unit. Customers can choose from the following four supported options.

- DLV11-F or DLV11-J Asynchronous Line Unit - Because of cabling requirements the DLV11-J can only be used with the DLV11-KA option

- DZV11-B Four Channel Asynchronous Multiplexer Interface

- MSV11-DD 32K × 16-bit MOS Memory (additional)

- RXV11 or RXV21 Dual Drive Floppy Disk System - Because the LSI-11/23 (KDF11-A) and the REV11 are incompatible, local boot of the floppy disk system is not supported.

2.4.2 LSI-11 Module Configurations

All jumpers and switches on the LSI-11 modules are correctly set at the factory. However, the configuration should be verified at installation time. Location and function of the switches and jumpers on the modules can be found in handbooks supplied with the system. The *Microcomputer Processor Handbook* (EB-15836-18) supplies this information for the processor and memory modules. The *Microcomputer Interface Handbook* (EB-17723-18) supplies this information for all other LSI-11 bus options.

Table 2-1 shows the correct switch and jumper settings for standard modules shipped with the DPM50-AA, -AB, -CA, and -CB models. Table 2-2 contains the same information for the DPM50-FA, -FB, -CA, and -CB models.

Table 2-1 DPM50-AA, -AB, -CA, -CB LSI-11 Modules Jumper and Switch Settings

Module	Switches and Jumpers	Position
KD11H	W1, W2, W3, W5, W6, W10 & W11	Out
	W4 & W9	In
	W7 & W8	Do not change*
MSV11 CD #1 First 16K	All Jumpers	In
	SW1, SW2, SW3, SW4 & SW5	On
	SW6, SW7 & SW8	Off
	Remaining switches	Does not matter
	W16	Out
	All other jumpers	In
MSV11 CD #2 Second 16K	SW1, SW2, SW4 & SW5	On
	SW3, SW6, SW7, SW8	Off
	OR	
MSV11 DD	W3 & W2	In
	Pin W3	
	Pin 5-7	
	Pin 10-15	
	Pin 5-14	
	SW S5	On

*Critical factory parameter

Switch and jumper settings for additional LSI-11 option modules must be set to integrate the option into the existing system. This must be determined at the time of installation. Directions can be found in the handbooks referenced in the previous paragraph.

NOTE: If a DLV11-J is incorporated into the system, its vector address jumpers must be set 340 to avoid conflict with the ISV11-A.

2.4.3 Serial Line Interface Cable Filter (Optional)

The DPM50, mounted in a properly grounded H960 cabinet, is shielded from the EMI/RFI radiation commonly found in industrial environments. However, the EMI/RFI radiation may reach the cabinet via the interconnecting cable if the DPM50 LSI-11 microcomputer is interfaced to an external terminal or other serial device. Attaching an H7006 filter option where the cable enters the H960 eliminates this.

Table 2-2 DPM50-FA, -FB, -HA, -HB LSI-11 Modules Jumper and Switch Settings

Module	Switches and Jumpers	Position
KDF11-AA	W1	In
	W2,W3	Do not change*
	W4	Out
	W5,W6	Out
	W7	In
	W8-W15	Do not care
	W16-W18	In
MSV11-DD	Pin 1 to 3	In
	Pin 1 to 2	Out
	W2	In
	W3	In
	W4	Out
	W5	Out
	Pin 10 to 14	In
	Pin 16 To 15	In

* Critical factory parameter

Two versions of the H7006 filter assembly kit are available to meet the filtering needs of all supported LSI-11 serial line interfaces used in a DPM50. The H7006-A kit is used with the following LSI-11 bus options: DLV11, DLV11-E, DLV11-F, and DZV11.

The H7006-B is used with the DLV11-J 4-channel asynchronous line interface. Table 2-3 lists the contents of the H7006-A and 7006-B kits.

Table 2-3 H7006-A and -B Filter Assembly Kits

Part No.	Description	Quantity Per Kit H7006-A	H7006-B
7423332-00	Filter mounting panel*	1	1
BC06K-7K	40 conductor mirror image cable	1	0
H7004-B	40-pin bulkhead filter assembly	1	0
7017399-06	DLV11-J 20 mA filter cable	0	4
H7005	8-pin Mate-N-Lok filter assembly misc. mounting hardware	0	4

* Only one 7423332-00 filter mounting panel can be mounted per H960 cabinet. Mount filters from additional kits in the existing mounting panel (no more than six) if additional filtering is necessary.

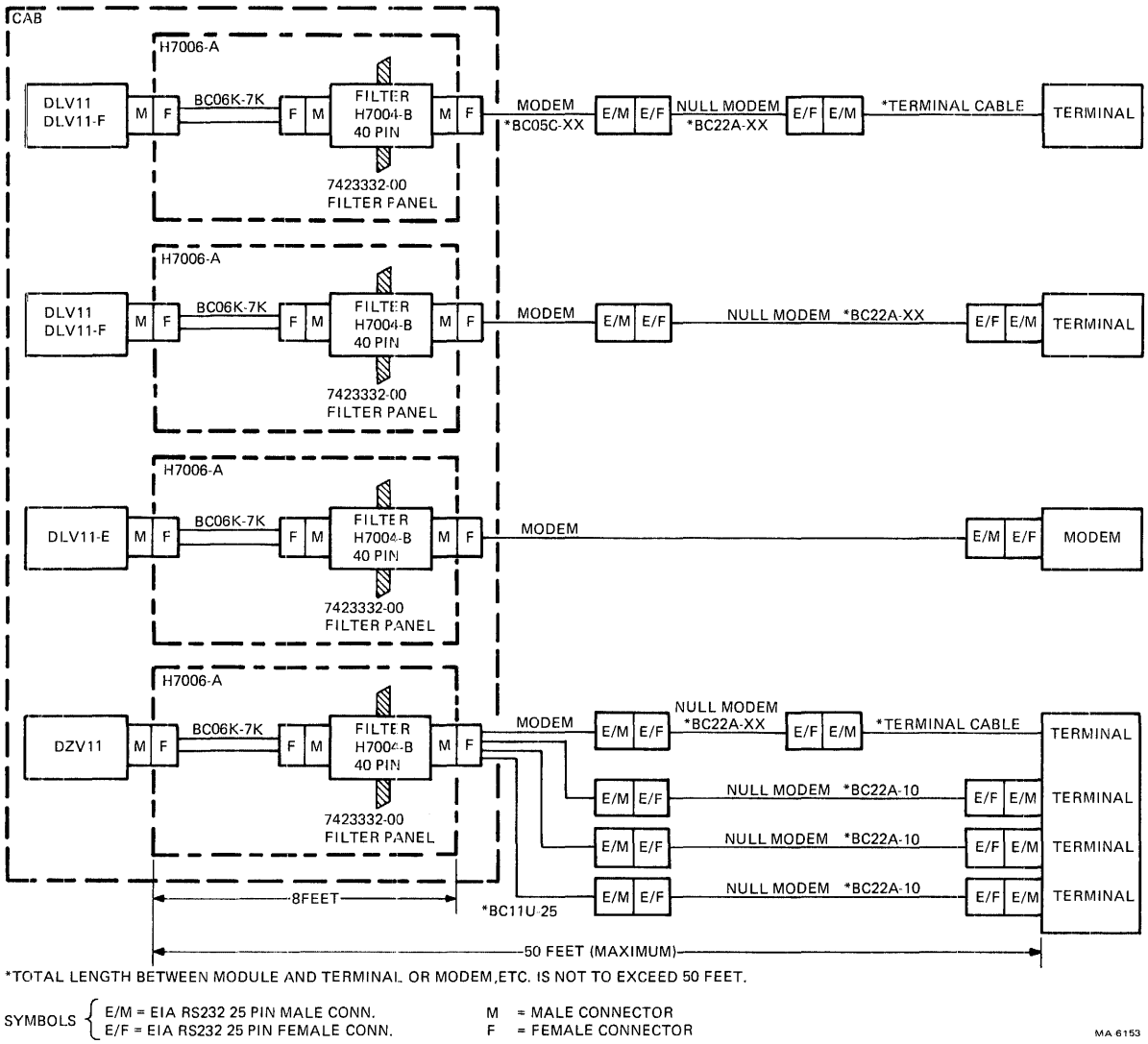


Figure 2-8 DPM50 Serial Line Filter Configuration - EIA (RS232C)

Figures 2-8 and 2-9 show DPM50 serial line filter cabling for various EIA and 20 mA configurations, respectively.

Refer to the H333 arrangement drawings in the *H333 Maintenance Print Set* for physical mounting and cable laying information and illustrations.

2.5 I/O CONTROL MODULE AND D-BUS OPTION CONFIGURATION

Procedures for configuring the I/O control module (IOCM), I/O modules, and placing them in the D-Bus can be found in Chapters 3 and 4 of the *I/O Subsystem User Guide*. However, the following information may be useful in determining power limitations imposed on the I/O modules by LSI-11 bus options in DPM50-Fx and -Hx systems.

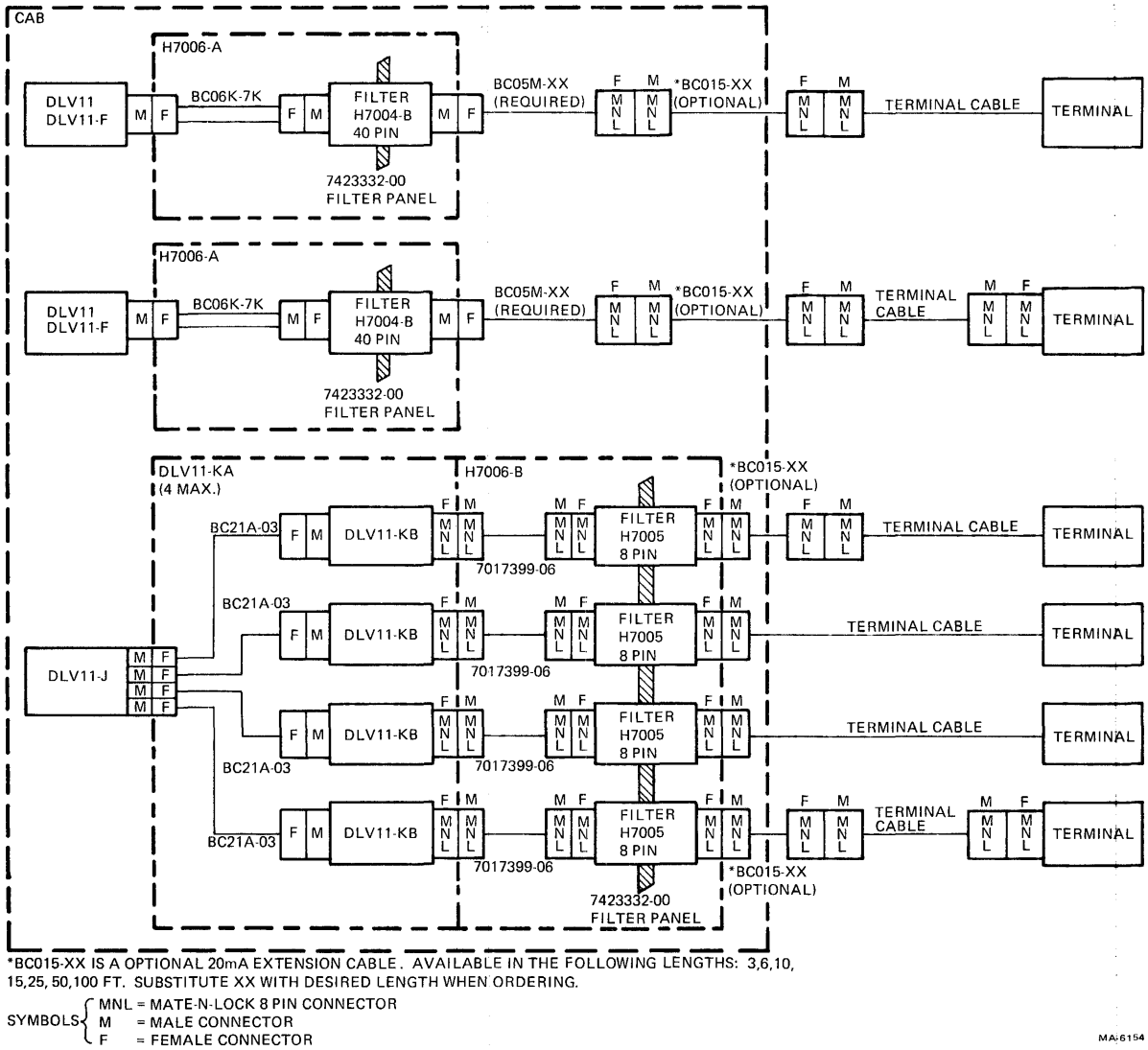


Figure 2-9 DPM50 Serial Line Filter Configuration - 20 mA Current Loop

The DPM50-Fx and -Hx have seven slots available for I/O modules in the H333. Due to power limitations, a close examination of power requirements for the I/O modules must be made based on which LSI-11 bus options are being used. The I/O modules use only +12 V from the H7870 power supply. The maximum current needed for each I/O module is specified in the *I/O Subsystem User Guide*.

Table 2-4 Available +12 V Current for I/O Modules

LSI-11 Bus Option	DLV11-F Console Interface	DLV11-J/DLV11-KA Console Interface
No option or console only	2.63 A	2.79 A minus 0.30 A/ DLV11-KA
DLV11-J/-KA	1.9 A minus 0.3 A/ DLV11-KA	Only one supported per system
RXV11, RXV21	1.87 A	2.02 A minus 0.30 A/ DLV11-KA
DZV11-B	1.49 A	1.64 A minus 0.30 A/ DLV11-KA
MSV11-D (second)	1.42 A	1.57 A minus 0.30 A/ DLV11-KA
DLV11-F	1.75 A	1.9 A minus 0.30 A/ DLV11-VA

The +12 V current available for the I/O modules varies depending on which LSI-11 bus options are present in the H333. Table 2-4 shows the amount of +12 V current available to the I/O modules for various LSI-11 bus configurations.

NOTE: Due to Field Service requirements outlined in Section 2.4.1, all specifications in Table 2-3 are based on the assumption that a console terminal interface (DLV11-F or DLV11-J) is present in the LSI-11 bus.

CHAPTER 3
MAINTENANCE

3.1 OVERVIEW

WARNING: Do not initiate any DPM50 diagnostic or maintenance software before checking with local site personnel for any safety precautions to be performed and/or any operating restrictions. The DPM50 is a remote process controller. Its I/O modules may control very sophisticated and perhaps dangerous industrial processes.

This chapter is divided into the following three main areas.

- Sections 3.2 through 3.4 are devoted to DPM50 related maintenance software and firmware.
- Sections 3.5 and 3.6 contain information about the ISV11-A and the H7870 power supply, respectively. This is DPM50 specific information not found in the *I/O Subsystem User Guide*.
- Section 3.7 contains DPM50 troubleshooting flowcharts.

Service personnel must take a system approach to maintaining a DPM50 with process I/O. This means distinguishing specific faults in the DPM50 from system-wide faults, such as problems in the host computer or DECdataway. It also means taking into account the hierarchical nature of the system. For example one cannot troubleshoot an LSI-11 bus device from the host if the ISV11-A connecting it to the dataway is not working properly. On the other hand, once system integrity from host to LSI-11 is verified, standard LSI-11 bus diagnostics (MAINDECs) are run on the LSI-11 for troubleshooting devices and I/O modules. The host plays no role in such troubleshooting except to download the diagnostics and communicate with the operator.

Figure 3-1 outlines the hierarchy of software and firmware used for DPM50 maintenance. It shows the functional areas associated with each software/firmware routine. Figure 3-1 can be used as an index to the particular paragraph in this chapter associated with each routine.

NOTE: Discussion of the above mentioned software/firmware routines in this chapter is brief and of an overview nature. In-depth procedures for running these routines can be found in the documentation listed in Section 1.6.

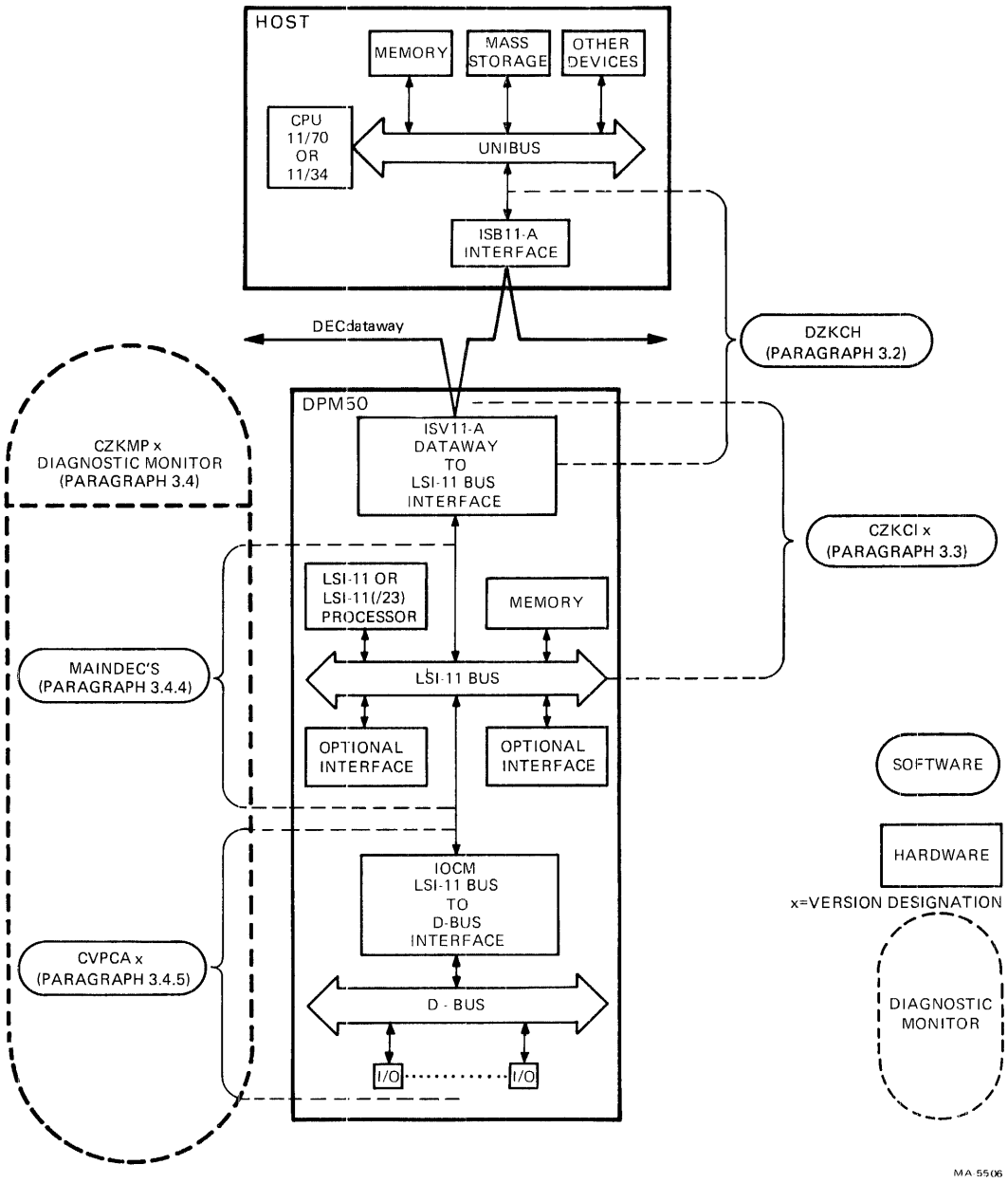


Figure 3-1 DPM50 Maintenance Software / Firmware Hierarchy

The North American (NORAM) industrial support team is chartered to provide all levels of support, including Field Service training for NORAM personnel. Support and training in European areas is provided by European Regional Support.

3.2 DZKCH – DECDATAWAY EXERCISER

The ability of the host to communicate with a DPM50 via the DECdataway must be verified before a valid diagnosis of a DPM50 can be performed. DZKCH is a task that runs under RSX11-M/M+ in the host. This task ex-

ercises the DECdataway and verifies integrity of the communications channel between the host and various devices on the dataway. With a DPM50, DZKCH checks communication up to and including the 8-bit microprocessor in the ISV11-A. It tests whether the 8-bit microprocessor can manage the DECdataway protocol and communicate with the host.

3.3 CZKCIx* AND ISV11-A ROM RESIDENT DIAGNOSTICS

CZKCIx is also a task that runs under RSX11-M/M+ in the host. When run, it starts internal diagnostics on selected devices connected to dataway ports. It receives and displays information on all but catastrophic errors.

With the DPM50, CZKCIx starts a series of ROM resident diagnostics in the ISV11-A. These tests also start automatically when the DPM50 is powered up and can be used as a basic standalone confidence check for the DPM50.

As stated earlier, CZKCIx can start the ISV11-A microprocessor running a series of diagnostic tests contained in its own ROM. As each test is executed, its test number is displayed in a set of LEDs mounted on the edge of the M8080 board. Refer to Section 3.5.1 to locate and interpret these LEDs. The first 9 tests (1-11 octal) are regarded as hardcore because they test basic characteristics confined to the ISV11-A. An error in any of these 9 tests causes the 8-bit microprocessor to loop within the test, thus continuously displaying the number of the first failed test. Diagnostics 12-14 (octal) check softcore characteristics involving the LSI-11 CPU (processor and memory). Test 13 takes about 11 seconds, but 12 and 14 are so fast their numbers may not be noticed in the LEDs. Errors in these tests are not allowed to shut down the system. However, if an error occurs, the test number flashes in the LEDs for 10 seconds and the number is upline loaded to the host for display.

3.3.1 Hardcore Diagnostics

The first 9 (1-11 octal) ISV11-A ROM-resident diagnostic tests are considered hardcore. If a hardcore error is encountered, CZKCIx fails and no error information is upline loaded to the host.

Table 3-1 describes the hardcore tests.

3.3.2 Softcore Diagnostics

Tests 12, 13, and 14 of the ISV11-A ROM resident diagnostic tests are considered softcore. For example, this type of error does not hinder the ISV11-A ability to communicate with the host. If a softcore error is encountered while running under CZKCIx, error information is upline loaded to the host and displayed at the operator's terminal.

Table 3-2 describes the softcore tests.

---

*x designates current version

Table 3-1 Hardcore Tests

Test	Module	Description
1	M8080	Checks power-up configuration of 8080 I/O registers 1 and 2, and does basic 8080 instruction test
2	54-13290	Does individual cyclic redundancy check on each 8080 ROM
3	54-13290	Checks writing and reading in the 8080 RAM and checks out RAM addresses
4	54-13290	Checks transmission and reception in USYNRT communications chip using maintenance mode
5	54-13290	If dataway connector is unplugged (i.e., address 77 is read), this test checks transmission and reception in the USYNRT through the modem; otherwise test is skipped
6	54-13290	Checks ISV11-A interrupt system
7	M8080	Checks 8080 I/O register 2 and 8080 I/O registers (3-5) that are common with LSI-11 control and status registers (CSR2 and 4)
10	M8080	Checks timeout feature of DMA logic for access to LSI-11 memory
11	Both	Checks LSI-11 interrupt circuit in ISV11-A

Table 3-2 Softcore Tests

Test	Module	Description
12	LSI-11	Loads a program into LSI-11 memory and then boots the LSI-11 – this checks ability of ISV11-A to interrupt the LSI-11 and vice versa
13	MSV11	Runs address and data tests on 28K words of LSI-11 memory
14	LSI-11	Runs LSI-11 instruction test by loading it into LSI-11 memory and booting the LSI-11 to run it

3.4 CZKMPx* DIAGNOSTIC MONITOR

If the ISV11-A and its communications channel to the host are in working order (i.e., DZKCHx and CZKCIx have run correctly), service personnel can execute standalone LSI-11 and I/O subsystem diagnostics in the DPM50. This is done with a diagnostic monitor that runs in the host computer. This monitor comes with every DPM system host. It is accompanied

*x designates current version

by a set of LSI-11 bus diagnostics, in image format, kept on file at the host. Note that the file names for these are the same as under XXDP but with the extension .IMG. (For information on these diagnostics, refer to Sections 3.4.4 and 3.4.5 of this user guide.)

CZKMPx allows service personnel to call various diagnostics for equipment on the LSI-11 bus in a DPM50 system. These diagnostics are downline loaded into LSI-11 memory and executed by the LSI-11. *Host mode*, *local mode*, and *communications mode* are available for carrying out this procedure. In host mode the operator remains at a host terminal and receives pass/fail and pass count information via upline reporting. Local mode allows operators to go to the remote site and run diagnostics from a terminal on the LSI-11 bus (connecting a portable terminal if necessary). This method allows operators to call and run diagnostics from the local terminal and receive complete error information. Communication mode is similar to host mode with one major advantage. The operator stays at the host terminal and receives not only pass/fail and pass count information, but also error messages generated by the diagnostic running in the DPM50.

CZKMPx runs as a task under RSX-11M/M+. To run it, the operator enters RUN CZKMPx in response to the MCR prompt character (>). In response to further prompts, the operator selects the mode, gives the number of the DECdataway ISB11-A controller, and gives the port address of the DPM50 to be tested.

3.4.1 Host Mode

Host mode is used to verify, from the host, individual component operation in several DPM50s. It is not as comprehensive as the testing process conducted in local mode at the DPM50 site. However, it provides an efficient method for service personnel to verify basic functionality of remote subsystems scattered over a large area along the dataway.

After the port is selected, the monitor starts the ROM-resident diagnostics in the ISV11-A. This takes the subsystem off-line. Failure of the port to come back on-line is interpreted by the host as a hardcore error. In this case a Field Service Technician must go to the remote site and fix the ISV11-A before that port can be further diagnosed from the host. For a softcore error, the host reports which of the three softcore tests failed. In any event, if the ISV11-A comes back on-line, the operator can continue selecting diagnostics to be run.

In host mode, the operator can select operation in single, script, or autoscript mode.

3.4.1.1 Single Diagnostic Mode – In single diagnostic mode the operator specifies a single diagnostic test to be called in from the disk. This test can be executed directly, or the operator can elect to patch it. If patched, the patched version can be saved, executed, or both.

3.4.1.2 Script Mode – In script mode the operator enters a series of diagnostic file names. The task then saves the created script in a special area on the disk, as well as executing the complete set. When this mode is selected, CZKMPx displays the message "Enter diagnostics to be scripted." The operator responds by listing diagnostic filenames and the number of times each is to be executed consecutively. Items in the list (filenames and numbers of passes) are separated by commas or a line feed at the end of a line. The entire list is terminated by a carriage return. The program then asks, "Do you wish to save this script?". A yes causes the question, "Under what name do you want this script stored?". The script is stored on the disk under the name given by the operator. However, a default name of ASCRPT is used if the operator responds to the question with a carriage return.

The monitor then downline loads each diagnostic in the script and executes it. As each test is downline loaded, its name appears on the operator's terminal. When the scripted diagnostics have all been run, an end message is issued and the operator is prompted to select a new mode.

3.4.1.3 Autoscript Mode – When this mode is selected, the monitor executes a script of diagnostics previously created in script mode.

3.4.2 Local Mode

In this mode, service personnel can communicate with the host for downline loading and running individual DPM50 diagnostics (kept on a disk at the host). Since they are right there at the remote site, they can deal with the equipment on the basis of information provided by the diagnostics. Therefore, service personnel can alter their troubleshooting strategy dynamically and use the diagnostic in conjunction with other types of test equipment (scopes, meters).

After selecting local mode, and the controller and terminal (dataway port) numbers, service personnel must go to the remote site and connect (if necessary) a portable terminal to the LSI-11 bus. At the local terminal, service personnel can downline load diagnostics from the host and control their execution in the DPM50 using ODT commands.

3.4.3 Communications Mode

Communications mode is similar to host mode. However, communication mode provides the operator with more detailed error information at terminals at the host. In host mode, the operator receives only pass/fail error messages. If a diagnostic fails in communication mode, any error message normally generated by the diagnostic is upline loaded to the host and displayed on the operator's terminal.

3.4.4 LSI-11 MAINDEC Diagnostics

The LSI-11 MAINDEC diagnostics in Table 3-3 are available for use with the CZKMPx diagnostic monitor.

Table 3-3 LSI-11 MAINDEC Diagnostics

DPM50 Device	Diagnostic	Comments
KD11-H	CVKAAC0	Basic Instruction test
(M7246)	DVKABA0	EIS Instruction test
	CVKACC1	FIS Instruction test
	CVKADC0	Traps test
KDF11	CJKDAC0	MEM Management
(M8186)		
	CJKDBC0	CPU - put a 1 in location 324 when running host mode
KEF11AA	CJKDCB0	Floating point chip n/a
	CJKDDB0	Floating point chip n/a
MSV11	CZKMAF0	MOS/COR 0-124 Exerciser
(M8044)		tests only 28K in host mode
DLV11	DVKAEB2	DLV11 test
(M7940)		
DLV11-J	CVDLAB0	DLV11-J test
(M8043)		
DLV11-F	CVDVCB0	Off-line test
(M8044)		
DLV11-E	CVDAC0	Off-line test
(M8017)		
DZV11-B	DVDZAA0	Four line ASYNC MUX test part 1
(M7957)	DVDZBA0	Four line ASYNC MUX test part 2
	DVDZCA0	Cable and echo test
RXV11	DZRXAE0	System reliability test
(M7946)	DZRXBF0	Interface DIAGS-NEEDS diskette
RXV21	ZRXDA0	RX02 floppy
IOCM	CVPCAD0	MDC I/O module test
(M7958)		

3.4.5 CVPCAx* I/O Subsystem Diagnostic

All information about the process I/O modules, the I/O control module on the LSI-11 bus, and the H333 chassis power supply is provided in the *I/O Subsystem User Guide.*

CVPCAx is a complete diagnostic for testing the entire I/O subsystem. The diagnostic and its use is described in the MAINDEC writeup (AC-A959D-MC). Its use is discussed briefly in Section 7.5.3.2 of the *I/O Subsystem User Guide.* The new version is automated process testing (APT) compatible and can, therefore, be run from the host. However, the only option that can be used when running from the host is the system test option, S. This option maps modules connected to the IOCM on the D-bus, and runs the appropriate tests on them individually. Of course, the entire diagnostic is used to its full capability if downline loaded from the host and run in local mode from a terminal on the LSI-11 bus.

*x designates current version

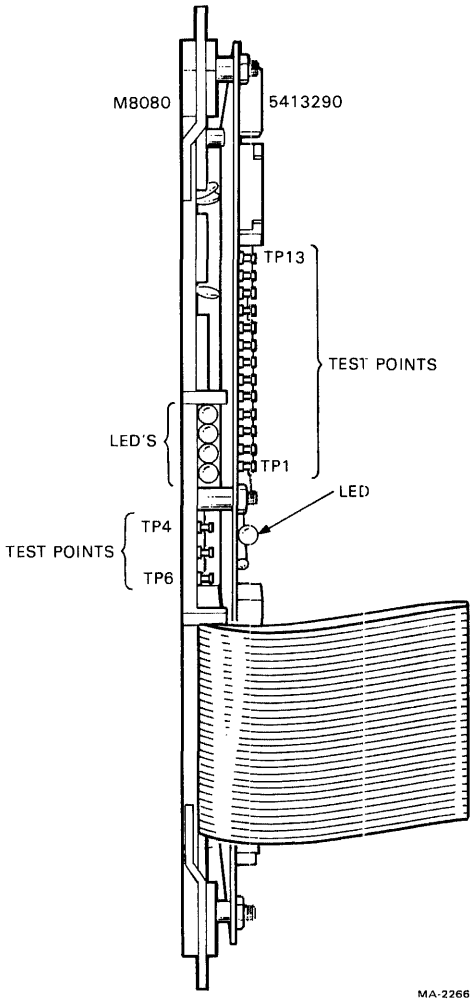


Figure 3-2 ISV11-A Boards, Edge-on

3.5 ISV11-A

The maintenance philosophy for the ISV11-A is option replacement. However, careful analysis of faults using diagnostics and available test points should permit service personnel to isolate a problem to one of the two modules. Section 3.5.3 of this user guide provides guidelines to aid in isolating a problem to one module. Note that the ISV11-A operates only as a unit, that is, with the M8080 and 54-13290 boards connected together. However they are not a matched set; a single board can be replaced if necessary.

3.5.1 LED Displays

As seen in the edge-on view of the boards (Figure 3-2), there are four LEDs on the M8080 board and one on the 54-13290. The single LED on the latter board is lit whenever a message is being transmitted to or from any port on the dataway - not just this ISV11-A. The light goes out at the end of every message but goes right back on again as soon as the next

message is detected. This is because the ISV11-A receiver picks up all transmissions on the dataway including its own transmission to the host. The light can be off for a significant time only if the dataway is inactive, out of order, or if something is wrong with the receiver.

The LEDs on the M8080 board are all on at power-up. If they remain on, the ISV11-A is broken so badly that the onboard 8080 microprocessor cannot even start its ROM resident diagnostics, which run automatically following power-up. As the diagnostics run, each displays its number in the LEDs (LSB at the top). The LEDs also signal failures (refer to Section 3.3).

During normal operation, the 8080 rotates an off light from top to bottom through the LEDs at a rate relative to the frequency at which it returns to its background routines. This means that the LEDs cycle slowly when there is a lot of dataway activity to the ISV11-A. The cycling speeds up as dataway activity decreases, and the LEDs cycle fastest when the system is inactive.

3.5.2 Test Points

The location and function of the ISV11-A test points are presented in the following discussion. This information is useful when troubleshooting the ISV11-A.

Lugs for the test points appear near the LEDs in the edge-on board view (Figure 3-2). On the M8080 the three test points are below the LEDs and are numbered 4-6 from the top down; on the 54-13290 they are above the LED and are numbered from the bottom up.

M8080 (Refer to Figure 3-3)

Point	Signal	Meaning
TP4	DMR H	Internal DMA request
TP5	FRPLY H	Failed to receive DMA reply
TP6	WAIT L	Force 8080 wait state

54-13290 (Refer to Figure 3-4)

Point	Signal (including print on which it appears)	Meaning
TP1	PCS2 BUS MEMR L	8080 memory read
TP2	SL5 T DATA H	USYNRT serial output to modem
TP3	+12 V through 1K	
TP4	SL5 T ENA H	USYNRT transmit enable to modem
TP5	−5 VB through 1K	
TP6	−12 V through 1K	
TP7	+5 V	
TP8	−5 VA through 1K	

54-13290 (Cont)

Point	Signal	Meaning
TP9	GND	
TP10	SL1 DROPOUT H	No signal on dataway
TP11	SL1 R DATA H	Received data to USYNRT
TP12	SL1 T CLOCK H	Transmitter clock from !2 (55.556 KHz)
TP13	SL1 R CLOCK H	Receiver clock to USYNRT

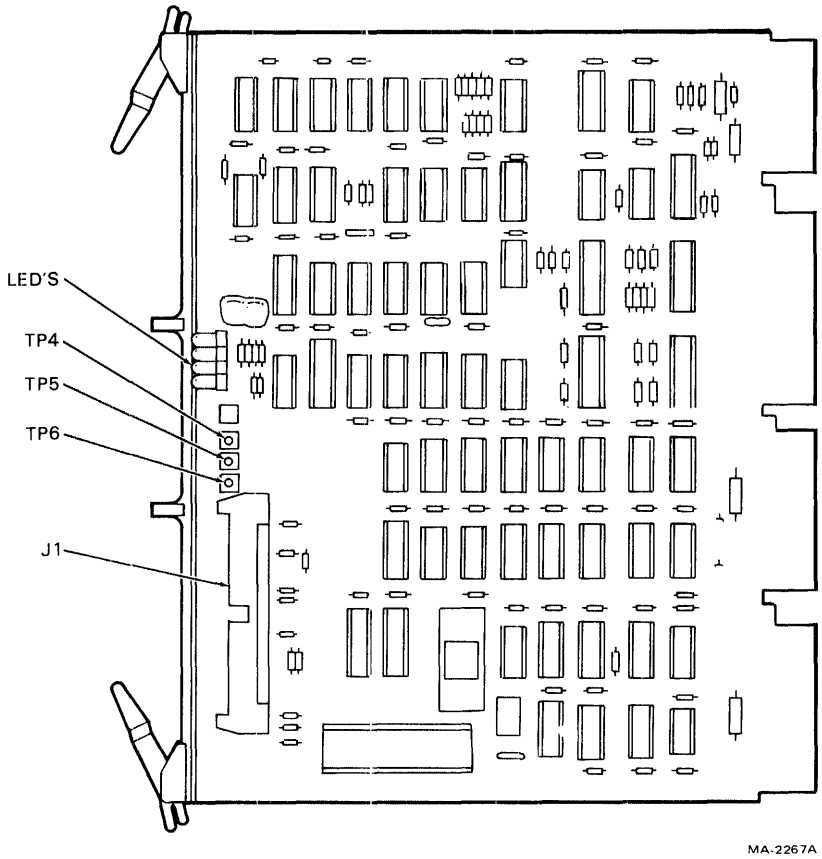


Figure 3-3 M8080 Board

3.5.3 Module Troubleshooting

The following procedures are helpful if it becomes necessary to troubleshoot an ISV11-A to one of its two boards.

Most ISV11-A checks can be performed with the modules installed because all test points and LEDs are located at the module edge. However, when it is necessary to access internal points on the boards, use the following set-up procedure.

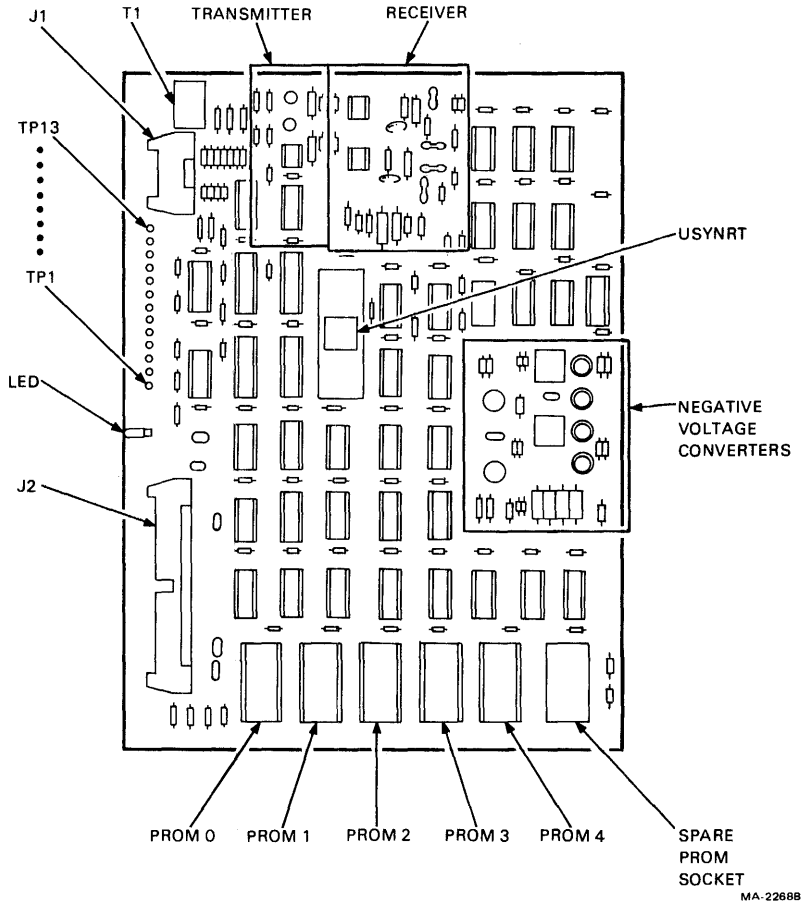


Figure 3-4 54-13290 Board

1. Remove the ISV11-A module set.
2. Install two double height module extenders, or one quad extender.
3. Remove the six screws that join the M8080 to the 54-13290.
4. Reverse the 54-13290, align its outside edge with the outside edge of the M8080, and join them with three screws. Make sure the short ribbon cable still connects them.
5. Plug the M8080 into the module extender.

QUICK CHECK FOR MAJOR PROBLEMS

These tests check the major functionality of ISV11-A modules. They are particularly useful if the 8080 does not run (all maintenance LEDs on). Unless otherwise indicated, all test points are on the outside edge of the 54-13290. Testing requires a voltmeter and an oscilloscope (preferred) or logic probe.

NOTE: TP7 (+5 V) and TP9 (GND) can be used to power the probe.

1. Using TP9 as a ground reference, ensure that the following supply voltages are present:

   +5 V ± 5 percent at TP7
   +12 V ± 5 percent at TP3
   −12 V ± 10 percent at TP6
   −5 VA ± 5 percent at TP8
   −5 VB ± 5 percent at TP5

2. Check that the modem transmitter clock, T CLOCK H, is present on TP12. It is a square wave with period 18 μs. This test also verifies that the 8080 clock generator is working.

3. Check that 8080 memory read pulses, BUS MEMR L, are present on TP1. This verifies that the 8080 is fetching instructions and running. If it is not, verify on the M8080 that BPOK H (E14-12) and READY H (E70-23) are asserted. Then replace the 8080 (E70).

4. The carrier detected LED should turn on (dim or bright glow) when a running dataway is connected and off when the dataway is removed. If the LED stays on, check that T ENA L (TP4) is high. If T ENA L is asserted, the USYNRT chip (E20 on the 54-13290) or the 8080 program flow is defective.

MANUAL MODEM TEST

This test should be performed if test 6 (modem test) in the power-up diagnostics fails. Test 6 is not executed unless the dataway is disconnected. Furthermore, this manual test should not be performed unless the dataway is disconnected to prevent disruption of its ongoing activity.

The test checks out most of the circuitry interfacing the USYNRT chip to the dataway. In particular, it verifies the following things.

1. The transmitter turns on and off.

2. The transmitter transmits ones and zeros.

3. The modem analog circuits transmit and receive data.

4. The receiver decodes ones and zeros.

5. The receiver detects the sync pattern (two successive zeros following a one) that locks in carrier detected.

6. The receiver detects the pattern that drops carrier detected (absence of any transition for 1-1 1/2 bit times).

NOTE: In either the analog or digital circuitry of the receiver, there may be subtle failures which can cause occasional CRC errors or other problems. However, these failures may not be detected by this test or test 6. If such a failure is suspected, replace the ISV11-A.

The following tools are required to perform this test.

- Two 6-inch jumpers with alligator clips or miniclips at each end
- Oscilloscope (or logic probe)

Success or failure is determined by observing the state of the carrier detected LED after each step.

		Effect	LED
1.	Power up ISV11-A with dataway	Transmitter idle	Off
2.	Connect jumper 1 from TP4 (E ENA L) to TP9 (GND)	Transmit 1s	Off
3.	Connect jumper 2 from TP2 (T DATA H) to TP9 (GND)	Transmit 0s	On
4.	Disconnect jumper 1	Transmit 1s	On
5.	Disconnect jumper 2	Transmitter idle	Off

If the test fails, repeat it, observing these points with the scope after each step.

Step	R CLOCK H (TP13)	R DATA H (TP11)
1	Logic 0	Logic 1
2	Logic 0	Square wave (18 μs)
3	Square wave (18 μs)	Logic 0
4	Square wave (18 μs)	Square wave (18 μs)
5	Logic 0	Logic 1

3.6 H7870 POWER SUPPLY

In a DPM50, the ISV11-A is mounted in an H333 chassis which contains its own power supply. The HALT/ENA switch on this power supply must be set to ENA. Furthermore, the +5 V output of the supply must be in the +5.1 V ± 0.15 V range. Instructions for adjusting the supply are given in Section 7.4.1 of the *I/O Subsystem User Guide.*

3.7 DPM50 TROUBLESHOOTING FLOWCHARTS

WARNING: Do not initiate any DPM50 diagnostic or maintenance software before checking with local site personnel for any safety precautions to be performed and/or any operating restrictions. The DPM50 is a remote process controller. Its I/O modules may control very sophisticated and perhaps dangerous industrial processes.

The rest of this chapter is a series of flowcharts (Figures 3-5 through 3-8) that define a troubleshooting procedure for the DPM50.

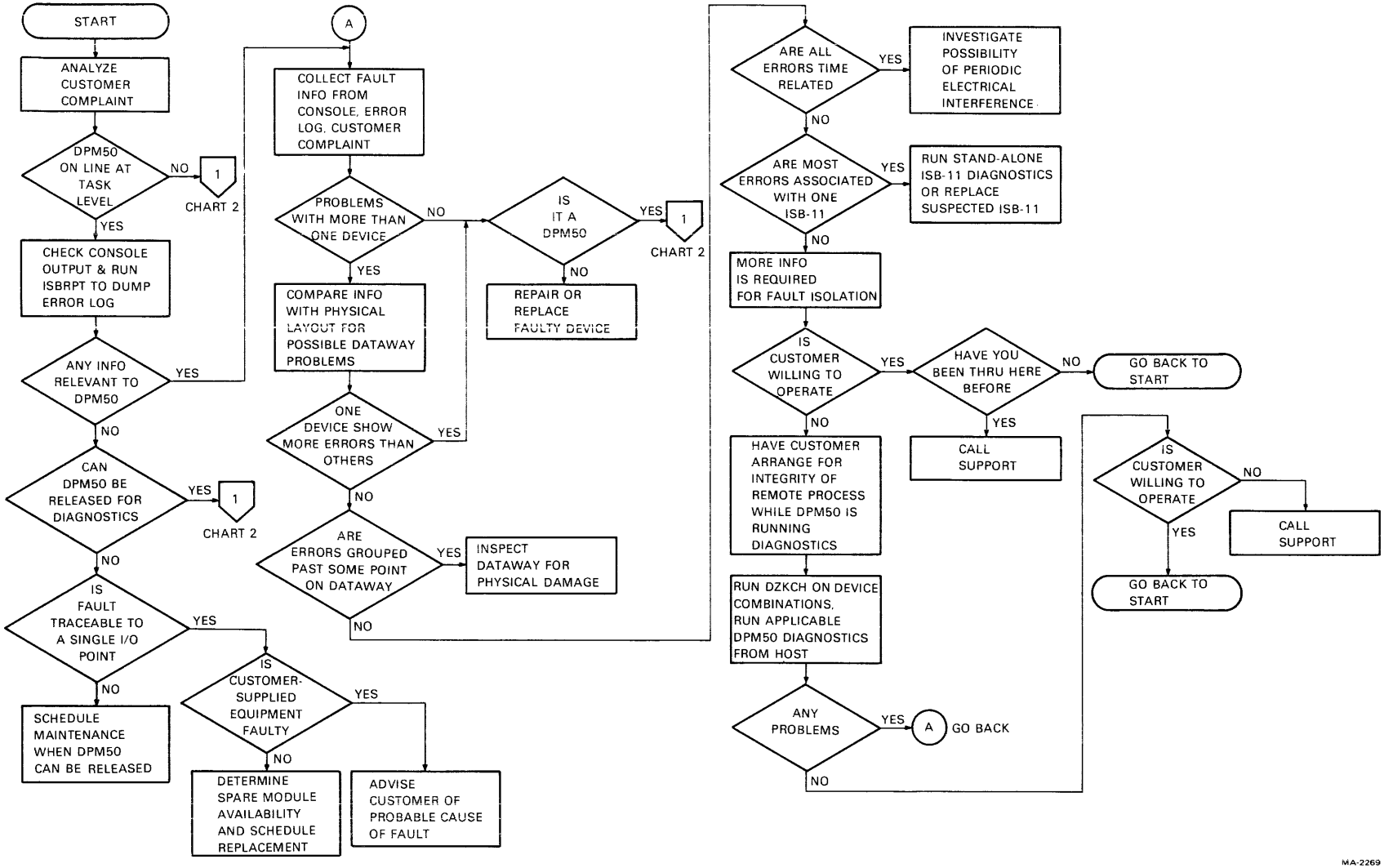


Figure 3-5 Troubleshooting Flowcharts
Chart 1 System Procedure

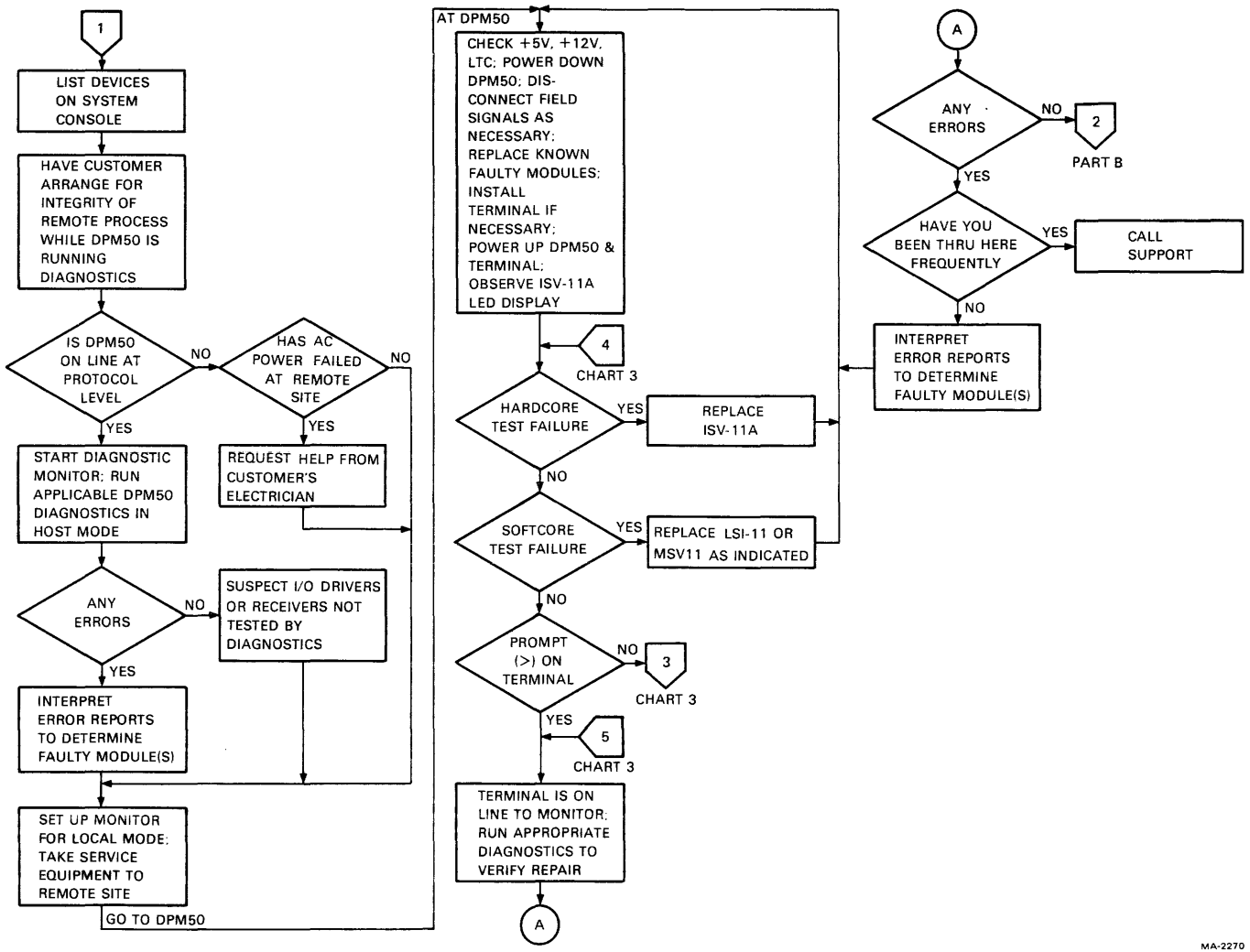


Figure 3-6 Troubleshooting Flowcharts
Chart 2 DPM50 Subsystem Procedure, Part A

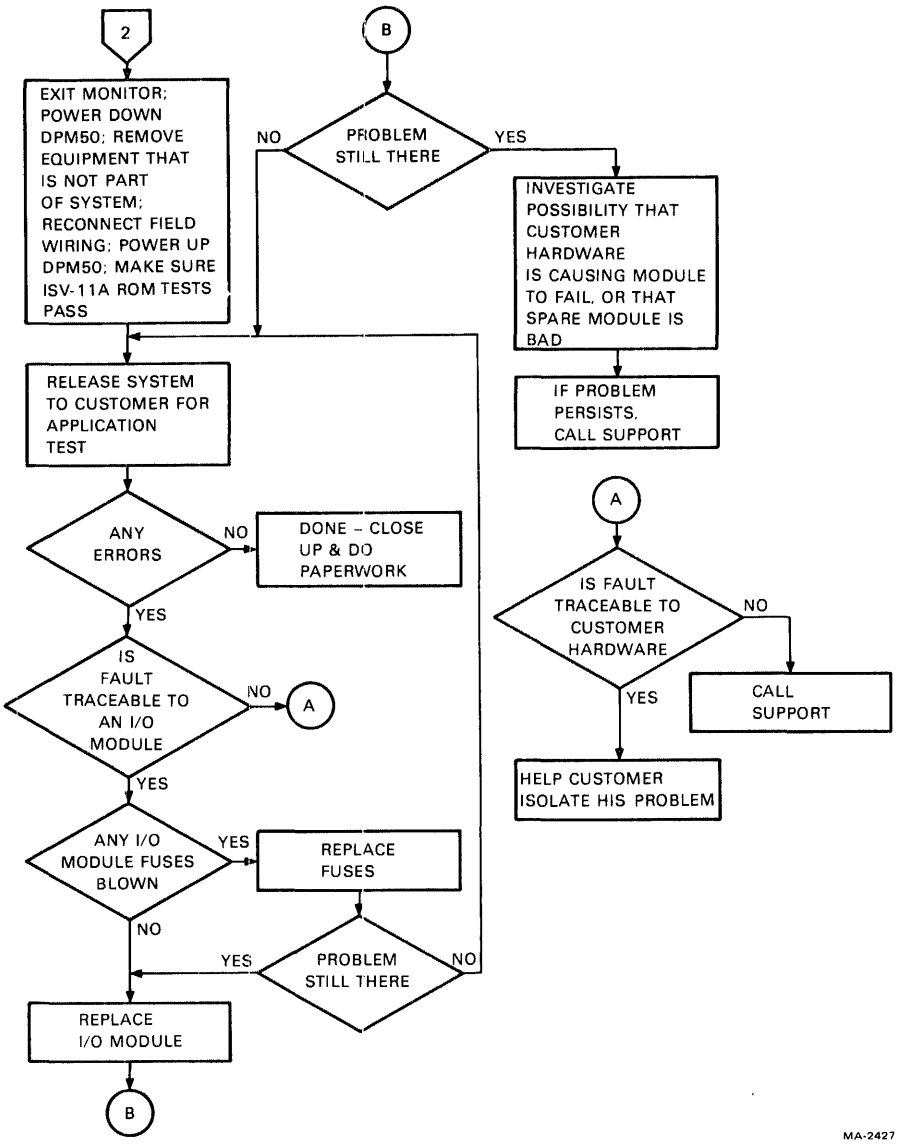


Figure 3-7 Troubleshooting Flowcharts
Chart 2 DPM50 Subsystem Procedure, Part B

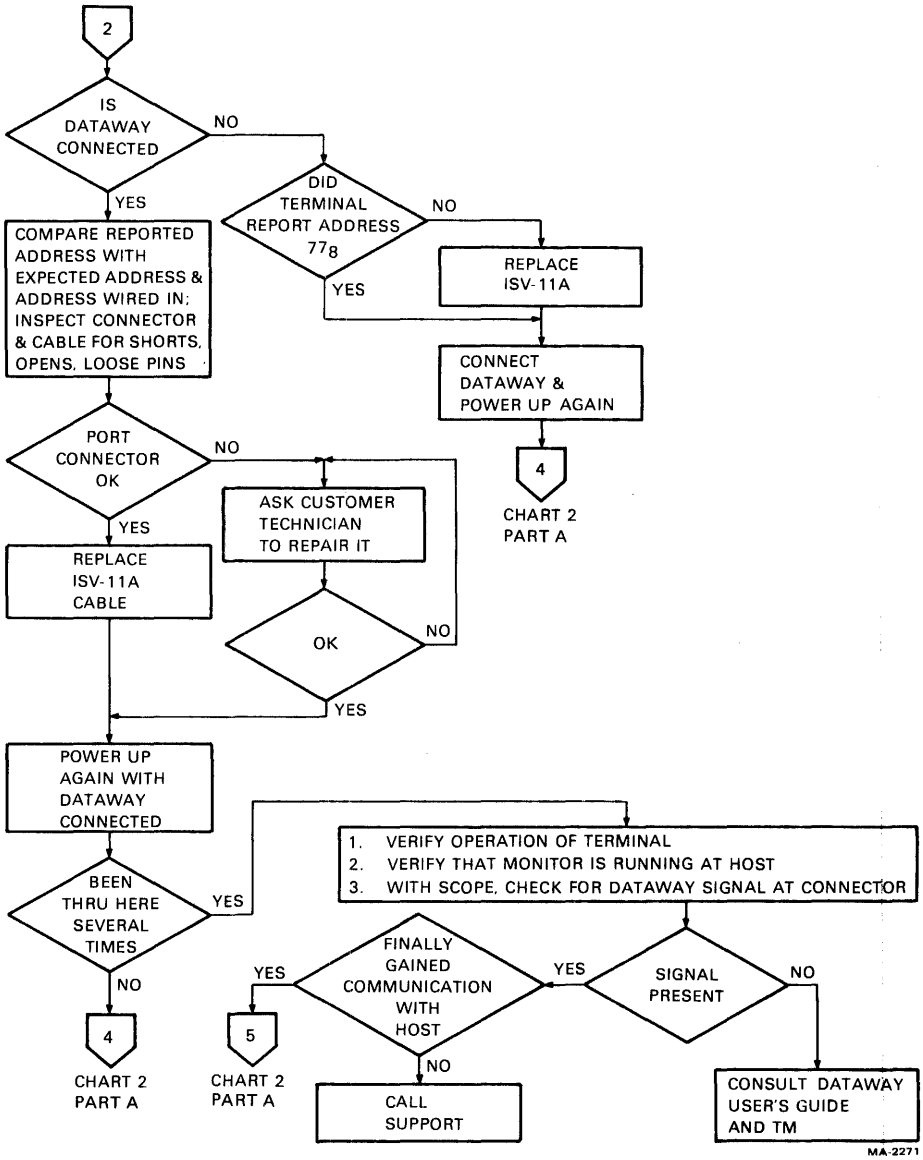


Figure 3-8 Troubleshooting Flowcharts
Chart 3 Port Address Checkout

CHAPTER 4
SYSTEM LOGIC

4.1 OVERVIEW

The ISV11-A is a dual quad-height printed circuit board option. It is built around two large-scale monolithic integrated circuits, an 8080 microprocessor, and an LSI synchronous communications device (USYNRT). In order to understand how the hardware functions, readers must be familiar with the operation of these two circuits as explained in the vendor manuals. A signal name glossary has been provided at the end of this manual.

Figure 4-1 is a block diagram showing the logical organization of the hardware on the M8080 ISV11-A microprocessor and the 54-13290 serial line unit. Logically the system has three major subdivisions organized around two internal buses, one of which is simply an extension of the LSI-11 bus. The processing unit is comprised of elements of both boards and is shown in the upper left quarter of the figure. It includes the 8080 microprocessor, its associated clock and gating circuits, and local memory. Communication between microprocessor and local memory is over the 8080 bus. This bus runs throughout both boards, connecting the processing unit to the other two major parts of the logic. The interface between the 8080 bus and the DECdataway is shown in the upper right quarter of the drawing, contained entirely on the 54-13290 board. This subsystem is based on the USYNRT communications chip and connects to the dataway by a modem. The remaining hardware is shown in the lower half of the figure, contained on the M8080 board. It includes registers, decoders, and other minor logic elements that connect the 8080 bus to the LSI-11 bus. The LSI-11 bus in turn connects to the LSI-11, its memory, and peripheral equipment.

The hardware on each board is shown in a set of circuit schematics, code CS. Each set has a drawing number in the form X-0-1 (X is the board designation). A revised schematic has a revision letter to the right of the drawing number. For convenient referencing the individual sheets of each drawing set are labeled. For example, the labels on the six sheets of 54-13290-0-1 are SL1-6, and those on the eight sheets of M8080-0-1 are PCS1-8. These labels are used as prefixes in signal names to indicate signal origin. They are also used in the text and the block diagrams for referencing individual prints. In Figure 4-1 these labels appear in the lower left corners of each block to indicate which print contains the logic represented by the block. Parts of a print are indicated by combining the letters

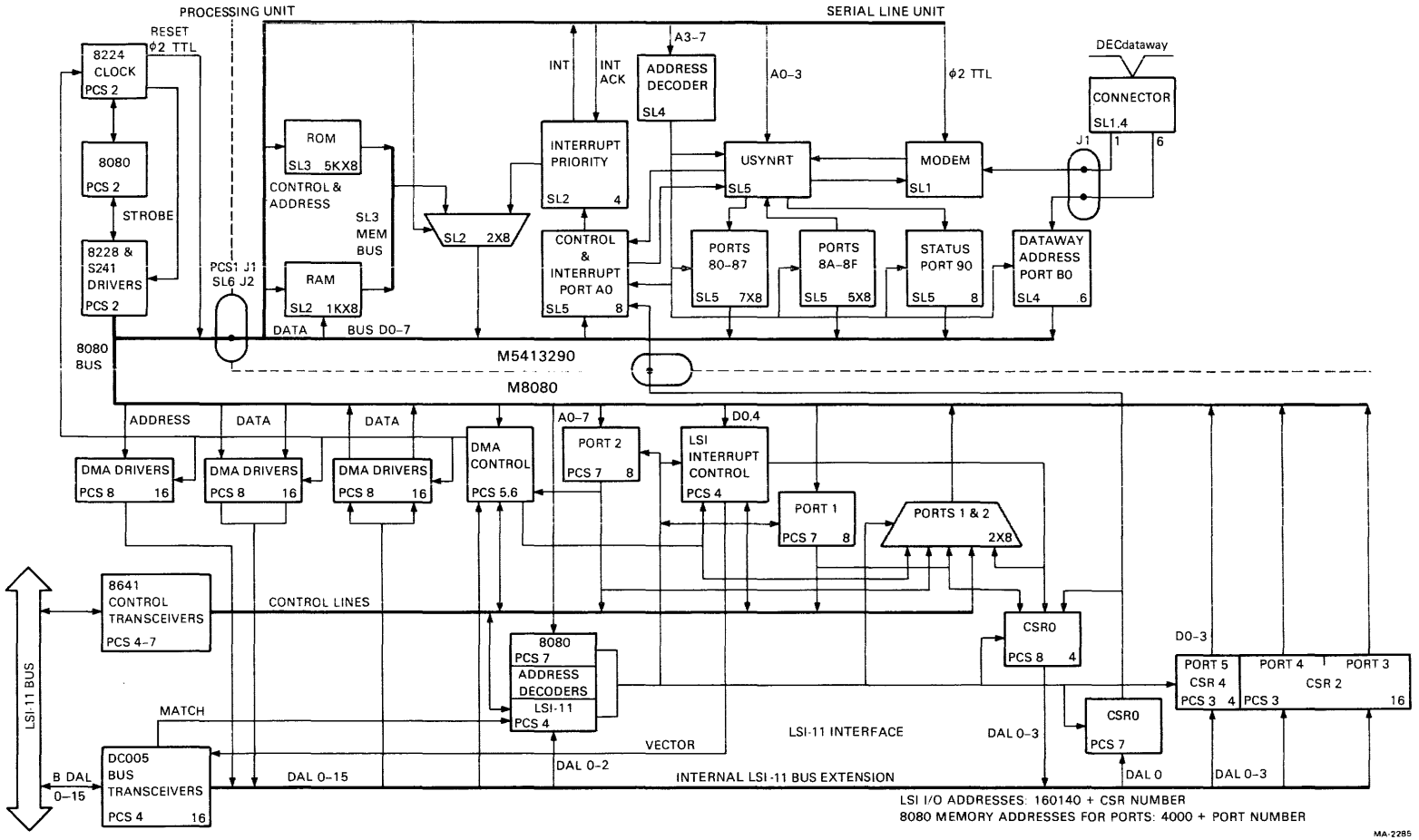


Figure 4-1 ISV11-A Logical Organization

and numbers along the edges. The following three sections give a detailed description of the hardware on the two boards. Discussion is geared to the prints, but readers should also refer to Figure 4-1 whenever necessary.

Some logic signals on the boards are available at test sockets shown in the lower-left on SL6 and the upper-right on PCS6. In some cases the lines to these test pins are not true logic signals at all, but gate inputs tied to +5 V. Therefore, they play no real role in system operation, but they can be pulled low to disable various parts of the logic for GR test purposes. These pseudosignals are identified on the prints by the word test.

4.2 PROCESSING UNIT

This unit occupies part of both boards and is shown on three prints; PCS2, SL2 and SL3. The first of these shows the 8080 microprocessor with its clock and gating circuits. The 8228 has bidirectional drivers for the 8 data lines in the 8080 bus; the two 74S241s below it provide unidirectional driving for the 16 address lines. The 8224 clock circuit at the left supplies the $\phi 1$ and $\phi 2$ clocks for the microprocessor chip, and the $\phi 2$ TTL clock for the serial line unit (all clocks are 2 MHz). At the beginning of every microprocessor machine cycle the 8080 places status information identifying the use of the cycle on its D outputs, and sends a sync signal to the 8224. This latter chip responds by sending a strobe to the 8228, causing it to load status into a set of latches. This frees the data lines for transfers during the cycle. The status information indicates the kinds of events that occur during the cycle. From the latched status bits and 8080 control signals WR and DBIN (write and data bus in), 8228 sets up memory, I/O control signals, and interrupt acknowledgement for the cycle. A memory read is for fetching an instruction, an operand, or an item from the stack; writing in memory can be for an operand or a stack item. Bus I/O control signals (in field DI on the print) are produced by the 8228 I/O outputs. However, they are also asserted by the memory control signals when the address is in the 4000-7FFF range. That is in the area of the ISV11-A address space reserved for I/O registers.

The ready input to the 8080 through the 8224 should always be high, except when a wait is required for a DMA operation. ENA DMA enables the 8093 so that WAIT goes low; when the acknowledgement appears, READY goes high and the 8080 continues. But, the DMA signals have no effect when I/O WR is true. This is done to prevent an unwanted wait from hanging up the 8080 if DMA signals are generated inadvertently because an I/O operation looks like a DMA operation to DMA logic. When the 8080 does an input or output instruction, it puts the one-byte address on both the upper and lower half of the address lines. Therefore an I/O port address of 80 or above puts a 1 on line 15, which may generate ENA DMA. The I/O WR prevents any wait during an IN instruction, but during an OUT it occurs later and the 8080 may enter the wait state for a single cycle.

The RAM and ROM that constitute local memory are on SL2 and SL3 respectively. The RAM is made up of 8 1K $\times$ 1 chips, each storing a single

bit of each byte in the 1K. Whereas the ROM is made up of 5 1K × 8 chips (with space for a sixth), each storing the entire byte for 1K locations. Logic gates at the upper-left on SL2 produce a memory select when the 8080 calls for a memory read or write with an address in the 0-1FFF range. The select, in turn, enables the decoding of address bit 10-12 at the lower-left on SL3 to select a single ROM chip or the set of eight RAM chips. The 10 least significant address bits are applied to the address inputs of all chips to select the individual location. When the RAM is selected and the function is write, bits from the eight data lines are written into the eight RAM chips. The output of the selected ROM, or set of RAMs, is available on the SL3 memory bus. During a read, the data is placed on the 8080 bus via the multiplexer at the upper-right on SL2. Drawing TD-ISV11A-0-7 shows the timing of the signals involved in the 8080 reading and writing memory.

4.3 SERIAL LINE UNIT

The heart of this unit is the USYNRT synchronous communications chip at the left on SL5. It is set up for byte operation by a high level at pin 22 and connecting corresponding pins for the left and right bytes of its 16 data inputs-outputs. These connect to the eight data lines of the 8080 bus. The 8080 governs the device by supplying control bytes and reading status. The USYNRT in turn uses the modem for handling communication over the serial DECdataway. Serial data received from the modem at RSI is assembled into bytes, and is available to the processing unit via the eight data lines. Transmit bytes supplied over data lines are passed on serially to the modem from TSO.

The 8080 moves bytes to and from the interface by means of its I/O ports. Port selection is made by the address decoder at the right on SL4. The number of ports is small, and an I/O bus control signal is generated by either an I/O transfer or memory access in the appropriate address range. Therefore, decoding a few address bits and the I/O signals is sufficient to select among ports 90, A0, B0, and the USYNRT registers. From port B0 the 8080 can learn its own dataway port address, wired into the DECdataway connector and available through the gates at the left. SEL 8X enables the USYNRT data lines. Selection among various registers is made by address bits 0-2, applied to the USYNRT address inputs on SL5. Register reading and writing uses separate addresses, so A03 is connected to the USYNRT write input. A one enables writing and drives the USYNRT data lines from the 8080 bus through the two 74S241s at the lower-right. When a zero places a register on the data lines, READ 8X from the address decoder drives the 8080 bus from them. The E30 gate below the decoder on SL4 prevents register selection at all if the 8080 should give a read function for a write port.

The remaining 2 ports are at the upper-right on SL5, where address 90 reads status bits from the USYNRT and the modem, the LSI-11 interrupt request through E22. Address A0 loads a byte from the 8080 bus into the register in E27. The control bits supplied include enables for transmitter and receiver in the USYNRT maintenance mode, and for various conditions that can request interrupts through gates at the upper-right. Selecting maintenance mode inhibits generation of the transmit enable to the

modem (T ENA at CI), even if the USYNRT transmitter is active (TX ACT). The interrupt request levels are applied to the latch and priority network at the upper-left on SL2. Any interrupt request produces the INT signal, which goes to the 8080. Response by the 8080 with an acknowledgement latches the current request, enables the multiplexer for the SL2 bus (8080 bus data lines), and selects as multiplexer input an RST instruction encoded from the number of the highest priority request. The 8080 then executes the RST as a call to the corresponding location (as listed in the table at the lower-right on SL5).

4.3.1 Serial Transmitter-Receiver

The modem for the serial line unit takes up most of SL1. The basic time reference is the ϕ2 TTL clock supplied by the 8224 clock circuit associated with the 8080 microprocessor. This clock drives the receiver directly. For the transmitter, the exclusive OR gate at A7 (with the delay introduced by two inverters at one of its inputs) acts as an edge detector to multiply the basic clock to 4 MHz. From this, the E28 counter produces the 8X clock by dividing by nine. This is accomplished by loading 7 at the clock following the carry out produced by a count of 15. The 8X clock counts the E23 counter, which runs on a continuous 16-count cycle so its two middle bits provide division by 4 and 8. The T (IX) clock drives the USYNRT transmitter and shifts out the data; the 1X and 2X clocks together are used for biphase encoding of data transmitted over the dataway. Characteristics of the various clocks are as shown in Table 4-1.

Table 4-1 Clock Characteristics

Clock	Period (μs)	Frequency
ϕ2 TTL	0.5	2 MHz
8X CLK	2.25	444.444 KHz
2X CLK	9	111.111 KHz
T CLOCK	18	55.555 KHz

The modem is coupled to the DECdataway by transformer T1; its secondary winding connects the serial line at pins 9 and 10 of the internal dataway connector. The transformer is the 1-1-1 type. That is, a pulse train in from the line generates two output trains, one positive and the other negative, but both have the same amplitude as the input. The transmitter uses only one primary coil each way, so the output is a 5 V signal, either positive or negative. The two zener diodes back-to-back (shown at the left of the connector) draw no current until the potential reaches 9 V and then they draw a great deal. This prevents a surge on the dataway from burning out the operational amplifiers. During transmission the zeners limit output to 9 V even though the transmitter circuit output is about 12 V. With the dataway connected there is an effective 100 ohm load. This is due to

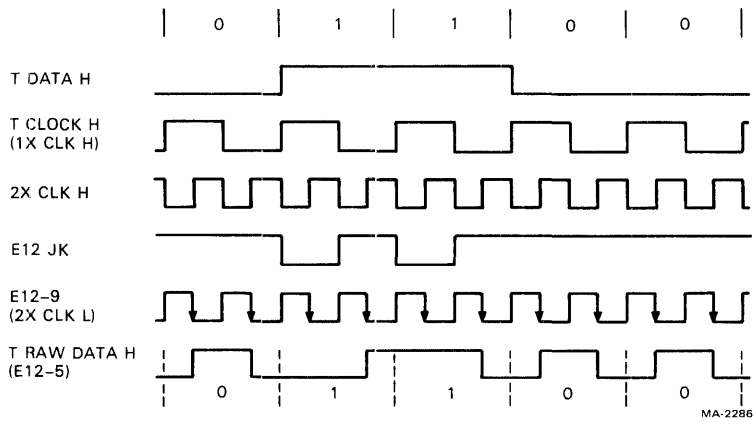


Figure 4-2 Transmitter Timing

either the 200 ohm terminating resistor in parallel with the cable or being mounted in the middle of the 200 ohm cable. Therefore, the line is actually driven at about 5 V.

The only control signal supplied by the USYNRT to the modem is T ENA at D8. When this signal is true, the T1 primary can be driven at one side or the other to drive the serial line. When T ENA is false the transmitter is disabled, and the receiver picks up any data coming from the DECdataway.

The disable and external inputs, as well as various outputs of the circuit, are available at the test socket on SL6. Test inputs allow for disabling the clock and the raw received data, so external inputs can be substituted for them. Conversely, without the disables, the external connections make the internal clock and raw data available at the test socket.

4.3.1.1 Transmitter – Data from the USYNRT enters the transmitter circuit at E31-13 (C8), ANDed with the T clock. The gate keeps the J and K inputs to the E12-5 flip-flop high, except when the data bit is one and T clock is high. Therefore, JK is enabled throughout the bit period on a zero; and for half the bit period on a one. This can be seen in Figure 4-2, which shows the relationship between data, flip-flop signals, and transmitter clocks. This means that the flip-flop toggles twice during a zero bit, but only once during a one. The state of the flip-flop drives one side or the other of the T1 primary. Therefore, there are two zero-crossings during transmission of a zero on the dataway, but only one during a one. This is the so-called biphase modulation technique of data transmission.

The circuit in D8 senses the +5 V. Should the voltage drop slightly, Q4 conducts and disables T ENA. Therefore, if the power is failing, the transmitter is disabled even if the USYNRT is sending data (which may be invalid).

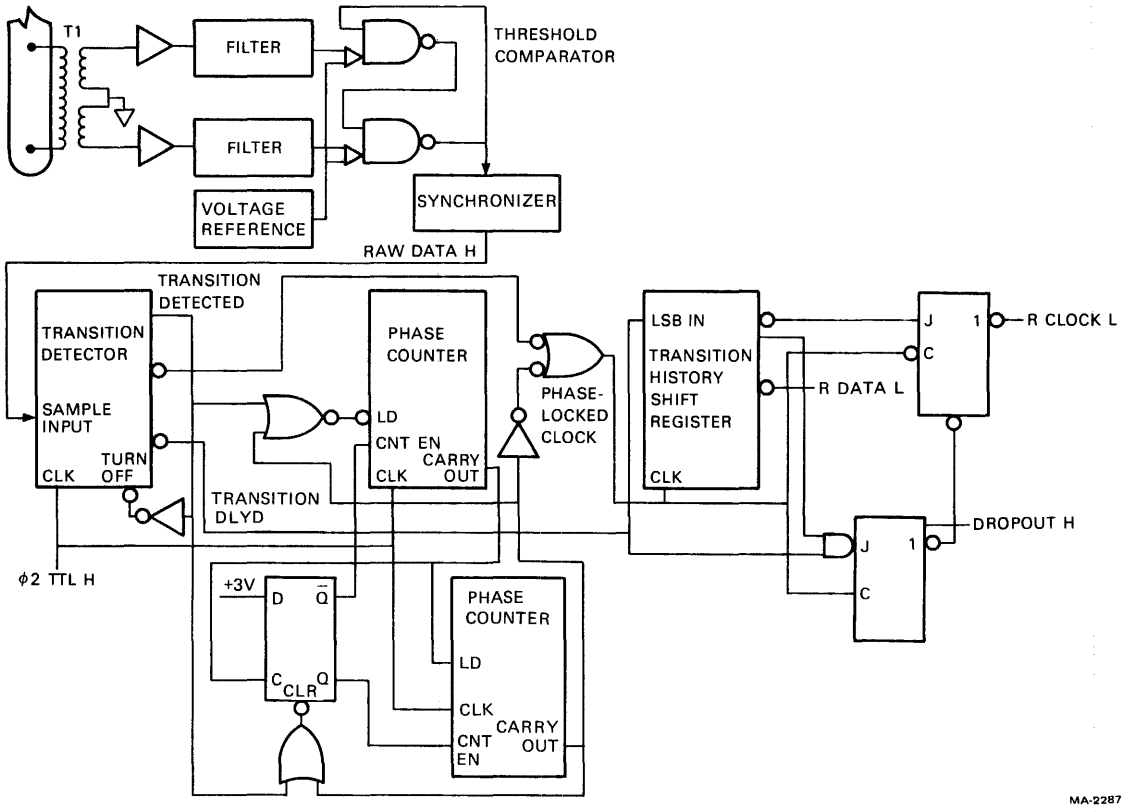


Figure 4-3 Receiver Simplified Block Diagram

4.3.1.2 Receiver – Changes in current flow through the T1 primary are sensed by the receiver circuit (shown at top-center on SL1). A switch in direction, caused either by the serial line (secondary) or transmitter, reverses the state of the raw data outputs (shown at the upper-right). A string of logic components is shown from left to right, across the center, and in the lower-right of the print. These logic components process this raw data to detect the start of message, derive data bits and a clock to be passed on to the USYNRT, and detect a dropout of the received signal. The logic is driven by the 2 MHz ϕ2 TTL clock, which runs at 36 times the bit rate of the dataway. Therefore the clock not only synchronizes the raw data to the ISV-11A, but also provides a finer resolution for sampling it.

Figure 4-3 is a simplified diagram of the receiver with most components in the same relative position as they appear on the print. The dual signal generated by the T1 primary from the dataway is applied to a pair of operational amplifiers. These have gain +1 and high input impedance for isolation. The 56K input resistors prevent a power turn-off in the ISV11-A receiver from dragging down the dataway. The bandpass of the filters at the amplifier outputs eliminates both high and low frequency noise, but it attenuates the signal to about one-third. For generating raw data, the threshold comparator uses a reference of 50 mV; this guarantees the spec of 100 mV, one-third of the 300 mV minimum dataway signal. A switch in the

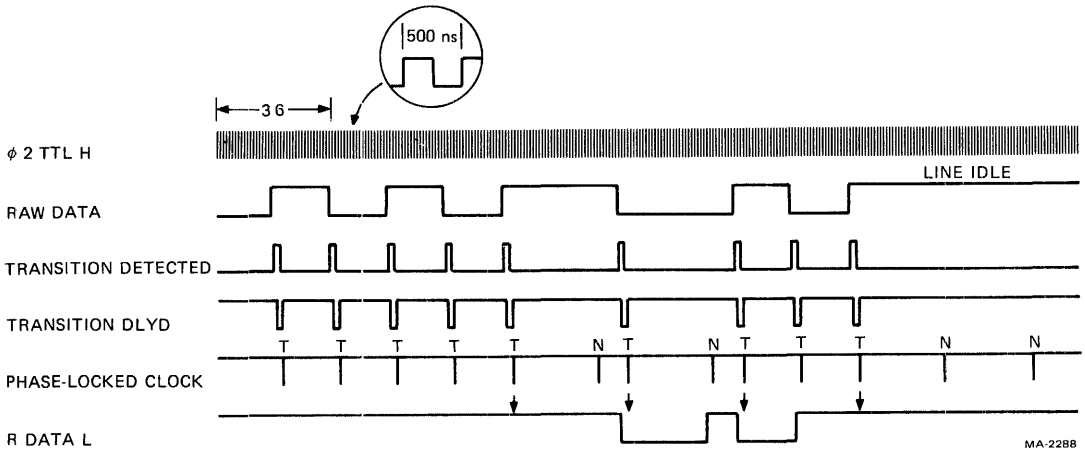


Figure 4-4 Receiver Timing

comparator outputs occurs only when the signal goes above the positive threshold after having been negative, or below the negative threshold after having been positive. Changes in the raw data are synchronized to the clock by a flip-flop.

The logic shown across the lower part of Figure 4-3 contains three main parts: a transition detector at the left, a phase-locked clock generator, and a shift register for recording recent transition history in raw data from the receiver circuit. This history is necessary for recognizing the start of message and modem dropout. It also distinguishes between zeros and ones in the received data it supplies to the USYNRT. Figure 4-4 shows the timing of major signals associated with this transition processing logic.

A message always starts with several ones followed by at least two zeros for synchronization. The timing diagram illustrates signal configuration for a message beginning with 100, followed by several arbitrary bits, and then a modem dropout. The transition detector generates three signals associated with a transition in the raw data. Following synchronization of a transition, the first 2 MHz clock produces the transition detected signal. This is on for two clock periods; during that time it turns off the detector to inhibit further sampling of the raw data. This filters out noise near the modem comparator threshold, preventing any noise surrounding a transition from being mistaken for another transition. The second signal, transition delayed, has the same form as transition detected but it has opposite polarity and is offset by one clock period. The difference in these two signals is that transition detected inhibits the detector (resetting the phase counter), and transition low actually represents the transition for processing by the remaining logic. The third signal from the detector produces the phase-locked clock, which occurs at the end of transition detected.

The phase counter is reset at every transition, but in the absence of transitions it simulates the phase-locked clock every time it reaches 30. The *T*s and *N*s in the timing diagram distinguish phase-locked clocks produced by transitions (*T*) from those that are not (*N*). The timing diagram is drawn with the exact theoretical timing for a serial signal from the bus. In a real situation, transitions can be quite late without adversely affecting reception.

Each phase-locked clock shifts the transition history. Where the bit shifted into the register reflects transition low, detection of a transition causes a zero to be entered. After the line has been idle, the phase-locked clock that occurs at the fifth consecutive transition (a one succeeded by two zeros) clears the dropout flag, turning on the LED. From that point on, the data represented by the bottom line in the diagram, is made available to the USYNRT from the second bit position in the history shift register. The USYNRT samples incoming data at the R clock, which is represented by arrows and occurs at the trailing edge of the phase-locked clock. The absence of two transitions in a row sets the dropout flag, turning off the receiver clock.

The above discussion is sufficient for a basic understanding of what the receiver does, and how the incoming data is supplied to the USYNRT. But to understand in detail how the logic works, readers should turn to the circuit schematic (print SL1) and the complete timing diagram (TD-ISV11A-0-8) which show all associated signals. Raw data synchronization is provided by flip-flop E8-9 located at B3 on the print. The transition detector at the left is made up of a shift register and three exclusive-OR gates. When pin 9 of E11 is high, each clock shifts the register, sampling the raw data at the LSB. When pin 9 is low, each clock loads it from the data inputs; but these are connected so the register still shifts, ignoring the raw data. Therefore, each transition is shifted through the register, giving a sequence of signals through the exclusive-OR gates. E9-11 and E9-6 are transition detected and transition delayed. These gates are driven from pins 13, 15, and 11 respectively, and not 14 of E11 so they generate signal trains with on times of two clock periods (the latter offset by one period). E9-8, which generates the phase-locked clock, is fed from E11-13 and 11, and thus occupies the second half of the transition delayed on time. Binary counters E3 and E1 are configured for a count of 30, 17 in E3 plus 13 in E1. Detection of a transition clears E3 and sets an enable-disable flip-flop (E8-5). This allows E3 to count the 2 MHz clock after transition detected goes off, but inhibits E1 from doing so. When E3 counts to 15, the carry out loads three into E1 and sets the flip-flop, disabling E3 and enabling E1, which can then continue the count. When E1 reaches 15 (total 30), the carry out produces a phase-locked clock and clears the flip-flop, so the next 2 MHz clock clears E3 to restart the count. Therefore, there is a phase-locked clock at each transition, and also when there is a count of 30 without a transition. E15 is the history shift register.

Initially the E11 bits are alike, so E9-11 is low, which causes the 2 MHz clock to shift E11; E9-8 is high so the phase-locked clock is low; and E9-6

is also high. When the raw data changes, the next 2 MHz clock shifts E11, causing pin 15 to be different from the other three outputs. In particular, pin 15 differs from pin 13, so E9-11 goes high, enabling the load function at both E11 and E3. The first clock after detection of the transition loads zero into E3 and shifts E11 without sampling the raw data. That is, pin 15 remains the same and the transition then lies between pins 14 and 13. With this change E9-6 supplies a low input to E15 D0 and E2 J. The second clock loads again, moving the transition between pins 13 and 11. This causes E9-8 to drop, producing a phase-locked clock which shifts E15 and loads zero into E15 R0 since E9-6 is still low. E9-11 also drops, reenabling shifting and counting. The third clock then counts E3 to one and shifts E11, resampling the raw data and shifting out the preceding transition. This raises both E9-6 and E9-8, dropping the phase-locked clock. If a transition were detected, E9-11 would again go high, starting the whole sequence over.

Transmission over the serial line always begins with a few ones followed by at least two zeros. The final one and the two zeros provide a string of five transitions, a half bit time apart. Following the just defined procedure we see that the first four transitions result in four zeros being shifted into E15. This enables the AND gates at the clear input to the dropout flip-flop E2. At the fifth transition, the phase-locked clock clears E2, removing both the dropout signal to the USYNRT and the hold-clear on flip-flop E12-3, generating the R clock for the USYNRT receiver. Once the system is synchronized to the incoming serial signal, a transition that occurs before a count of 30 following a preceding transition produces a phase-locked clock that loads a zero into E15. If there is no transition by clock 29, clock 30 counts E3 to 15, and the carry out produces a phase-locked clock that loads a one into E15 (since E9-6 is high). But subsequent detection of a transition before the next 29 count (restarting the count with no transition detected ships the extra load) generates a phase-locked clock that loads a zero into E15. Therefore, a zero data bit causes the loading of two successive zeros into the first two stages of E15. A one results in a zero in R0 and a one in R1 following a pair of shifts. Thus, at the end of each bit time, the received data is represented by the state of R1. Since at this time R0 is zero for either a zero or a one data bit, the trailing edge of the phase-locked clock sets E12-3 to start a cycle of the R clock. Since the K input is held high, the flip-flop clears in the middle of the next bit time regardless of what the first phase-locked clock brings into R0. The first data bit the USYNRT actually reads is the second zero in the sync pair.

If no transition is detected through the 58th clock, the 59th counts E3 to 15 a second time, producing a second nontransition phase-locked clock. With E9-6 still high and a one already in E15 R0, this sets E2, indicating a modem dropout and disabling the receiver clock.

4.3.1.3 Negative Voltage Converters – The circuit at the left on SL6 provides one −12 V and two −5 V supplies from +5 V. Two separate −5 V supplies are necessary for handling the large power requirements of the PROMs.

Each −5 V converter is comprised of an inverter oscillator using a saturable core transformer, a negative rectifier, a filter, and a three-terminal regulator chip that produces the regulated −5 V. Oscillator frequency is about 40 KHz. The transformer primary has a 9 V square wave centered at +5 V; the secondary has an 18 V square wave centered at ground. Filter output to the regulator is approximately −8 V.

The −12 V converter uses the 9 V square wave across the T3 primary to drive a charge pump (C55, D10, D11, C56). The pump output is superimposed on the −8 V rectified secondary output to produce an unregulated −17 V, which is converted to a regulated −12 V by zener diode D12.

To prevent large instantaneous switching currents in the oscillators from coupling into the main +5 V supply, they have separate inner-layer ground and V_{CC} planes. The separate V_{CC} plane is decoupled from the main plane by an LC filter, and the separate ground plane is connected to the main ground plane at a single point.

4.4 LSI-11 BUS INTERFACE

This unit handles all communication (programmed transfers, DMA transfers, and interrupts) between the ISV11-A and the LSI-11 processor and memory. The bidirectional LSI-11 internal bus extension (PCS4 DAL) interfaces to the bidirectional LSI-11 bus data and address lines (B DAL) by the DC005 transceivers at the left on PCS4. The XMIT input is enabled for driving the LSI-11 bus from its extension when one of two things is happening. When the LSI-11 is reading a control status register (CSR), or when the ISV11-A is sending DMA address or data to the LSI-11 memory or I/O bank. At all other times the REC input is enabled, driving the extension from the LSI-11 bus. However, enabling REC also allows high levels at the JAV inputs to drive the LSI-11 bus lines independently. These inputs are connected for VECTOR to place an interrupt vector on the B DAL lines, where a jumper in is a one.

When the I/O bank select signal BS7 is true at E23-13, the JA inputs are compared with levels on certain LSI-11 bus lines. The lines are not connected to the chips in order; this is so a comparison can be made between JA inputs and lines 3-12. The match output is true when BS7 is true and bus lines 3-12 contain the address of the ISV11-A CSRs set into the JA jumpers. A jumper in is a one.

Type 8641 transceivers are used for interfacing to LSI-11 bus control signals (usually bidirectional). These transceivers appear on various prints at those parts of the logic with which they are associated.

4.4.1 Port Transfers

Programmed transfers are handled through what are regarded as 16-bit control status registers from the LSI-11, and 8-bit ports from the 8080 microprocessor in the ISV11-A. Furthermore, since addressing is from different buses and the I/O banks occupy different parts of the processors' address spaces, there are two completely separate address decoders.

The LSI-11 decoder is a standard DC004 (PCS4 right) that is enabled by matching the ISV11-A CSR jumper address with the address supplied on the B DAL lines. Bus control signals to the DC004 come via the transceivers on PCS6, as the same signals are also involved in DMA control. The sync latches the three least significant address bits, which are decoded for selecting the CSRs (select signals are backward as high levels are applied to the DAL inputs). For output, DOUT generates a high or low byte strobe, or both, depending on DAL 0 and whether WTBT selects a byte or whole word. For input DIN gives an INWD strobe. Both the address latch and the data strobe produce a bus reply through the 8641.

The LSI-11 supplies the address of the transfer control block (TCB) via the CSRs on PCS3. The only other data to the ISV11-A is via CSR0, when a one on DAL 0 sets the flip-flop in the lower- right corner on PCS7 to request an 8080 interrupt. The gate just above provides a read strobe for CSR0, allowing the LSI-11 to read its own interrupt request and other status information via the 74LS367 (E7) at the lower-left corner on PCS8. For test purposes the ISV11-A can load the CSRs via the I/O page in LSI-11 address space.

Decoding addresses of 8080 ports in the LSI-11 bus interface is accomplished by the logic at the top on PCS7. There address bits 0-2 are decoded to select the port on an I/O function when bits 3-7 are all zero. Only ports 1 and 2 (the E39 and E36 registers below the decoder) can be written by the 8080, and for these the select lines also generate write signals on an I/O write. From these two ports, the only bit the LSI-11 can read is boot status (port 1 bit 1) through CSR0. Setting and clearing port 1 bit 7 boots the LSI-11 by simulating a power-up signal on the DCOK line of the LSI-11 bus. To halt the LSI-11 port 1 bit 6 is handled by a separate flip-flop, so it can also be set by a power failure. Port 2 bit 5 is not included in the register as it is used to clear the LSI interrupt request flip-flop at the lower-right. Port 1 bit 0 and port 2 bit 4 do not show up here at all; they are used to request interrupts at the LSI-11 as described in the following discussion.

The 8080 can read most of what it supplies to ports 1 and 2, along with a few other bits from interrupt and DMA control, via the E38 and E40 multiplexers at the left. Port 0 is not used, and ports 3, 4, and 5 correspond to the three bytes of the TCB address in CSR2, CSR3, and CSR4 (PCS3).

4.4.2 LSI-11 Interrupt Control

Interrupt requests from the 8080 to the LSI-11 are handled by the standard DC003 dual interrupt circuit at the upper-right on PCS4. The 8080 can make requests on two levels, A and B, associated respectively with vector locations 300 and 304 in the LSI-11. Request inputs to the DC003 are held high, so making and dropping requests on levels A and B, respectively, is under writing control in port 1 bit 0 and port 2 bit 4. Status of current interrupt requests (LSI-11 bus A and B) is available to the LSI-11 via CSR0, and to the M8080 via ports 1 and 2.

A request made on either level results in assertion of the BIRQ signal to the LSI-11. Once the LSI-11 responds with DIN and the acknowledgement BIAKI, the DC003 disables BIRQ and asserts VECTOR. This produces a bus reply through the DC004 below and places the vector address on the LSI-11 bus via the DC005 JAV inputs at the left. The signal VEC RQST B puts a zero or one on line two depending whether the interrupt is on level A or B.

4.4.3 DMA Transfers

The upper 32K-byte half of the 8080 address space is used for referencing any 32K-byte section of the LSI-11 address space by means of DMA transfers. Before initiating any DMA operation with a 28K memory, the 8080 must set up AD 15, which is port 2 bit 0 (PCS7 B4), as address bit 15 on the LSI-11 bus. This indicates which half of the LSI-11 address space is to be referenced when A15 on the 8080 bus is one. Then, simply by making a memory reference in the upper half of its own space, the 8080 references the selected half of the LSI-11 space using DMA request and control logic on PCS5 and PCS6. (A 124K memory would require that AD 16 and AD 17 be set up as well.) The 8080 must also set BS7 (port 2 bit 3) if the address location lies in the I/O bank. Two timing diagrams, TD-ISV-11A-0-5 and TD-ISU-11A-0-6, show the relationships among the various quantities involved in output and input DMA transfers: LSI-11 bus signals; control signals for the 8080; the 8080 clocks; and machine states. An R or T in parentheses by a signal name means it is received or transmitted by the ISV11-A over the LSI-11 bus.

Movement of addresses and data between the two buses is through the 74LS367 drivers on PCS8. The signal T ADDR EN places the address on the LSI-11 bus through parts of the driver chips at the left. However, only 15 bits come from the 8080 bus address lines; bit 15 (A8) comes from port 2 instead. Each data transfer is of a single byte, with the low or high position on the DAL lines selected by A00. Data is gated from 8080 bus to LSI-11 bus by T DATA EN with the low byte handled by E60 and part of E46, and the high byte by E59 and part of E51. Gating from LSI-11 bus to 8080 bus is controlled by a DMA signal derived directly from the 8080 memory read, with low byte through E61 and part of E7, and high through E52 and part of E51.

An 8080 memory reference in the 8000-FFFF range produces ENA DMA at the upper-left on PCS5. This causes the 8080 to wait by pulling down the 8224 ready input on PCS2. On PCS5 it generates the appropriate DMA memory read or write level, and a DMA request that both goes out on the LSI-11 bus and clears flip-flop E15-9 at the lower-left. When the LSI-11 sends the DMA grant in, E12-5 sets, preventing the grant from being passed out to the next device. With the grant on, negation of both the sync and the reply at the end of the current bus cycle sets E12-9. This generates SACK on the LSI-11 bus to acknowledge that the ISV11-A has become bus master, and drops the request, following which the LSI-11 drops the grant.

The acknowledgement also triggers a timing circuit based on shift register E9 at the upper-left on PCS6. SACK sets E19-5 to feed a one into the LSB register and causes the output of the E17-8 AND gate to go low. The output of this gate is fed back to one of its inputs. This makes the output oscillate, supplying a rising-edge clock with a period of 110 ns, beginning about half a period after SACK goes true. Since the setting of E9 R0 clears E19-5, the clock provides timing for the transfer by passing a single one through the shift register. This moving one, in turn, controls the column of flip-flops shown at the center of the drawing. A1 in R0 sets T ADDR EN to place the address on the LSI-11 bus, and to gate the state of BS7 from port 2 onto the B BS7 line. This is to indicate whether the transfer is for memory or the I/O bank. At the same time a write function turns on T WTBT to specify an output byte. Time 330 turns on T SYNC, and time 440 clears T ADDR EN. For writing, 440 also sets T DATA EN to gate the byte onto the LSI-11 bus, and 550 turns on T DOUT to make the slave accept it. But for reading, 550 turns on T DIN to tell the slave to send data, and the read level itself gates the DAL lines onto the 8080 bus with the transfer time determined by the slave.

With SACK still asserted, the reply from the slave produces the DMA acknowledgement (C7) that frees the 8080. The freed 8080 negates the memory signals, negating DMR (PCS5). DMR, in turn, cancels either T DOUT or T DIN, whichever is on. Finally the trailing edge of RRPLY triggers an identical reset timer based on shift register E10. Reset time R110 turns off T SYNC, T DATA EN and T WTBT (if on), and it also sets E15-9 (at the lower-left on PCS5) to turn off SACK.

Each request triggers the 39 μs one-shot in the timeout circuit at the bottom on PCS6. Completion of a transfer clears it and prevents the clearing from affecting the E15-5 flip-flop at the right. However, should the one-shot time out, indicating failure of the slave to reply in a reasonable time, the flip-flop sets to generate FRPLY. This signal produces the DMA ACK to free the 8080. When DMR subsequently goes off, it clears FRPLY but also sets E19-9, triggering the reset time to clear the DMA logic.

4.5 FUNCTIONAL FLOWS

Figures 4-5 through 4-10 show the system's major operations in terms of functional flow, that is, as the signal paths and logic elements that enter into their execution. All logic elements are labeled for the circuit schematics on which they appear. The objective of a drawing is to identify all significant elements that play a role in a given operational sequence to help pinpoint the trouble. The investigator can then turn to the referenced schematics for details of circuit, signals, and pin connections.

These flows are meant to stand alone; no written description accompanies them since the detailed description of the logic, geared to schematics, has already been presented. All lines are labeled with the actual signal names from the schematics, and wherever possible the logic elements are represented by the symbols in the schematics. It has, however, been necessary in some cases to employ ordinary blocks as logic elements. These are easily identified because the signal lines entering them

have arrowheads. None of the diagrammed operations are comprised of only a single sequence of events. Rather, each is made up of several logically distinct but interdependent sequences, such as an 8080 instruction followed by an interrupt, then another 8080 instruction. Another sequence is an 8080 instruction followed by a response from the LSI-11, followed by an action by the ISV11-A. The numbers in circles indicate the order in which the hardware parts are employed for these sequences. Sections of the hardware tested by power-up diagnostics are labeled with test numbers.

The six flows are in three pairs, and all operations shown involve the microprocessor. The first two drawings illustrate the movement of information in either direction through the serial line unit. The next pair shows DMA transfers through the LSI-11 bus interface. Figure 4-9 shows the request of an interrupt in the LSI-11 from the ISV11-A, and Figure 4-10 illustrates an interrupt request in the opposite direction, the only operation that employs elements of both interfaces in the ISV11-A. There are many other minor operations, such as the 8080 reading or writing a port, and the LSI-11 making a CSR transfer. Components that enter into these simpler operations can easily be identified directly from the circuit schematics.

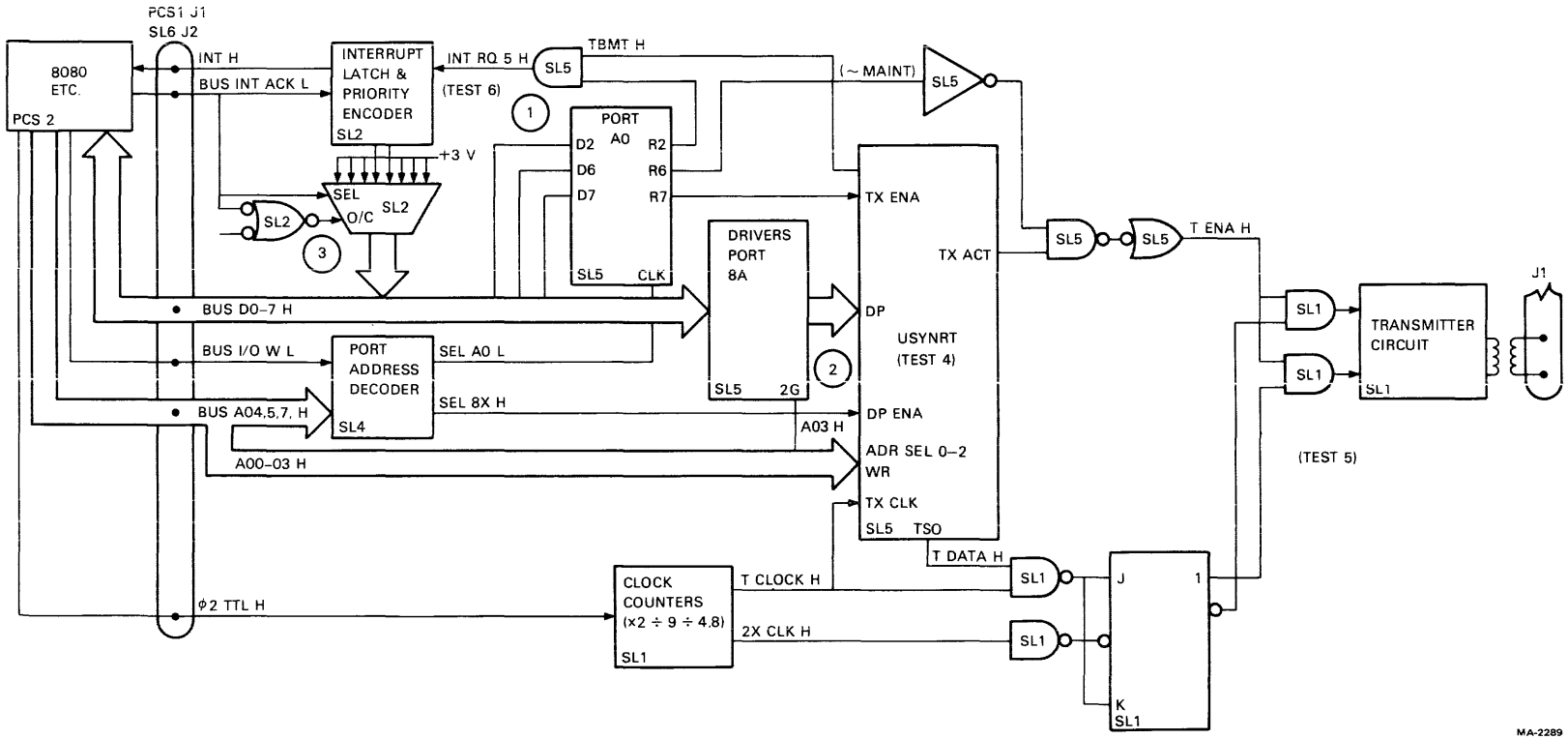


Figure 4-5 Serial Line Out

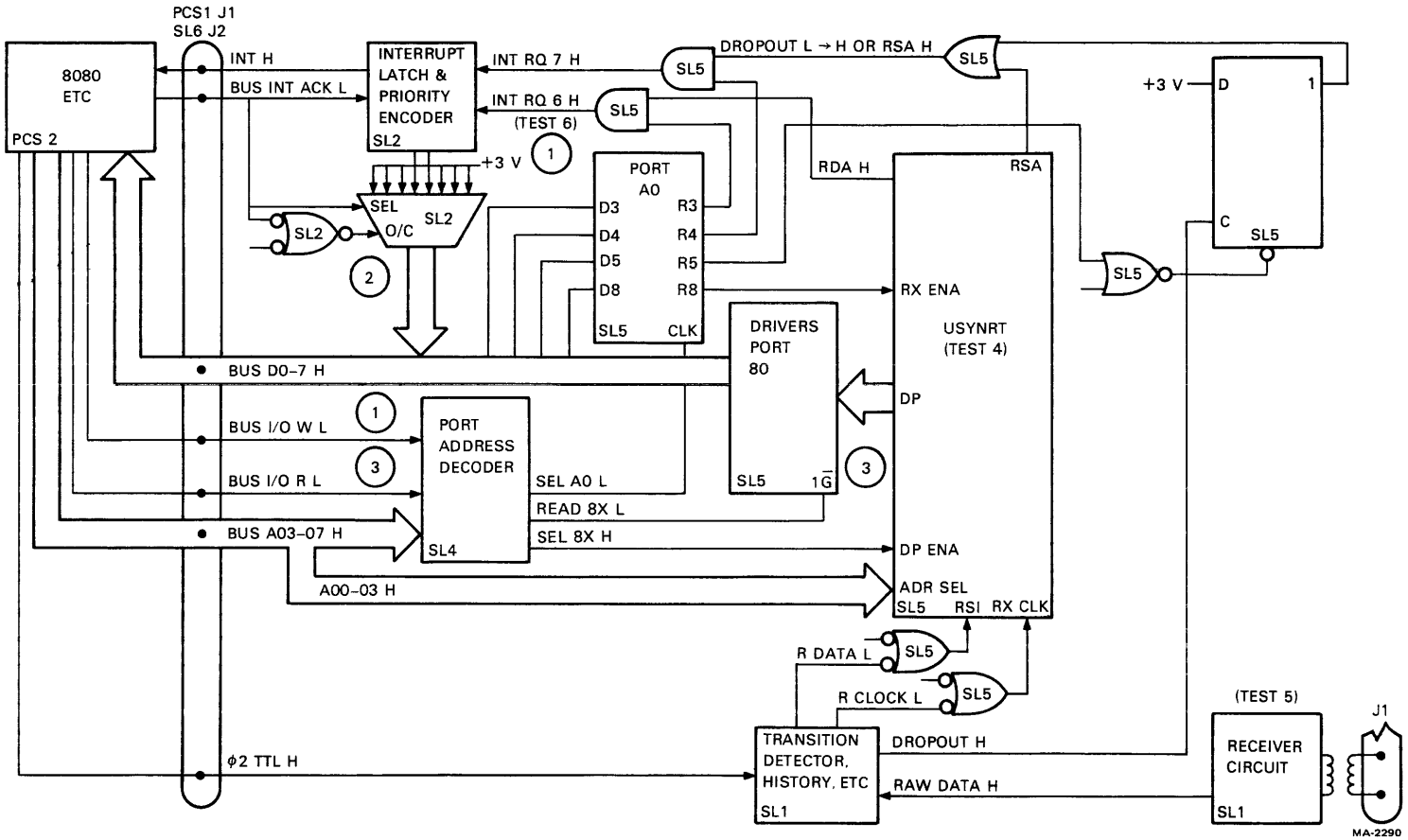


Figure 4-6 **Serial Line In**

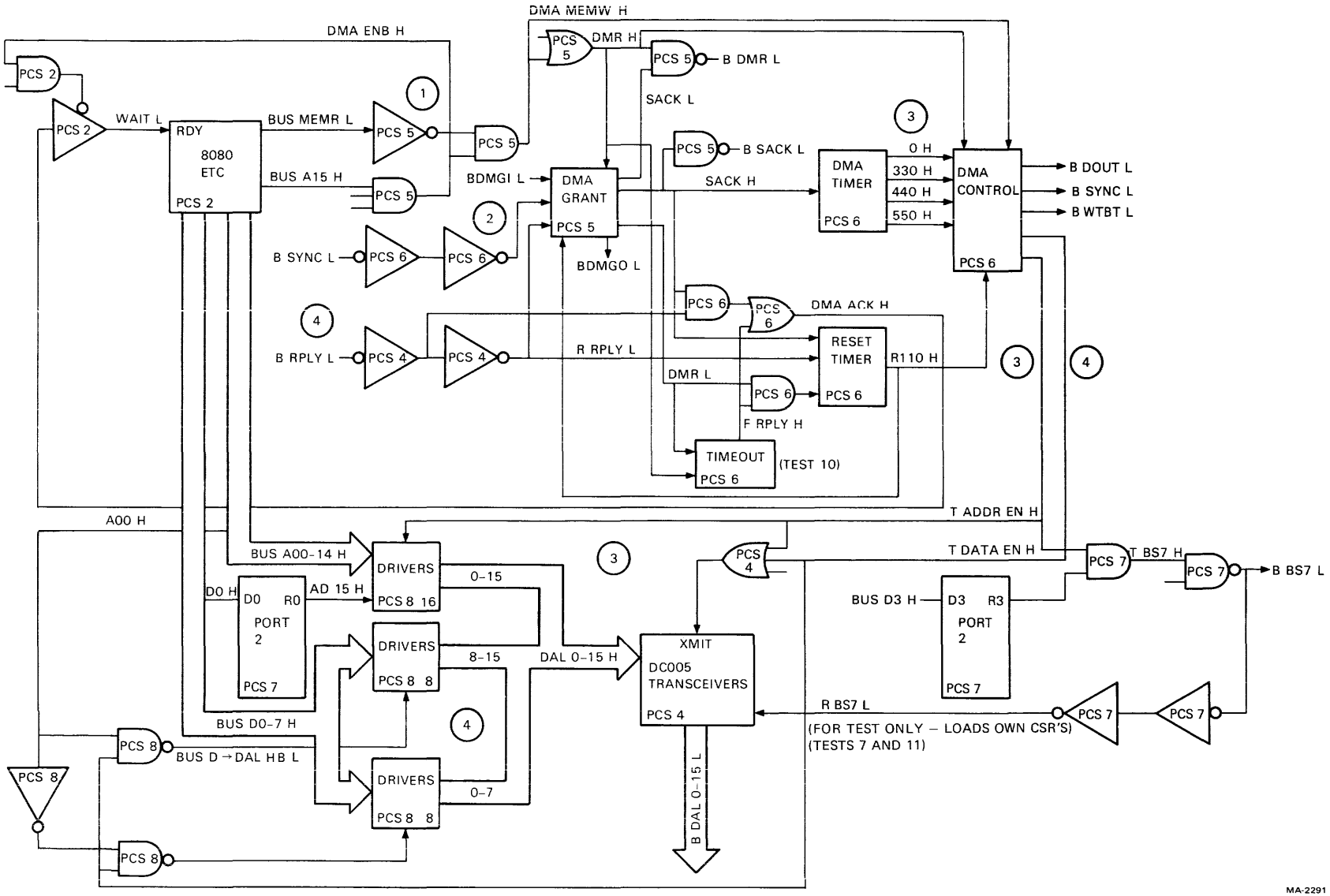


Figure 4-7 DMA Transfer Out

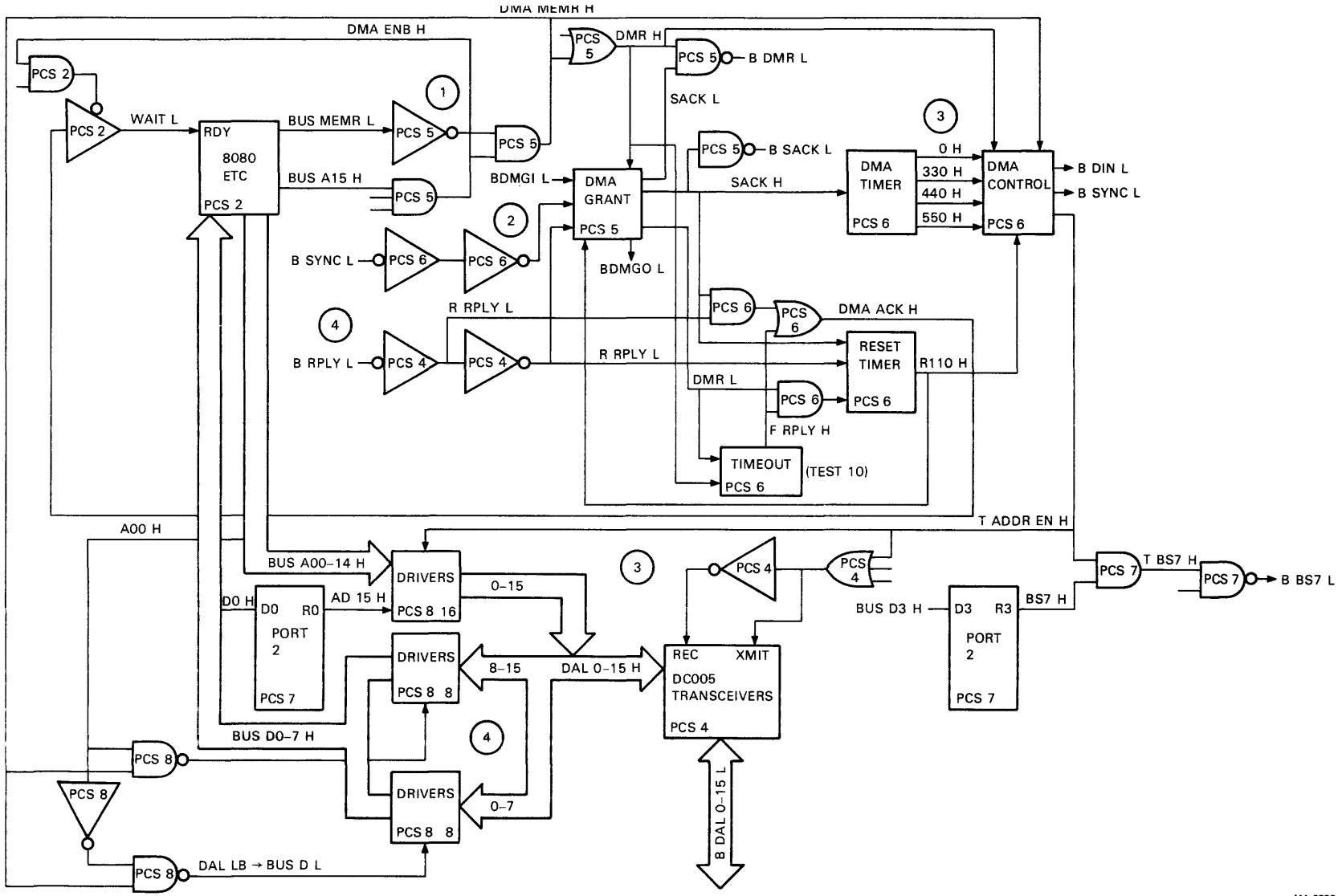


Figure 4-8 DMA Transfer In

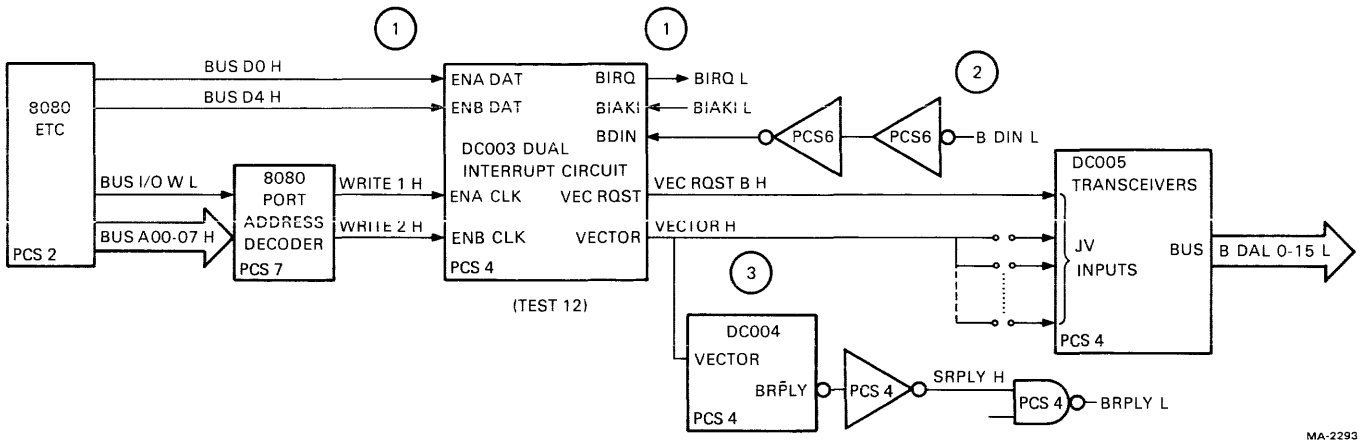


Figure 4-9 ISV11-A Interrupt Request To LSI-11

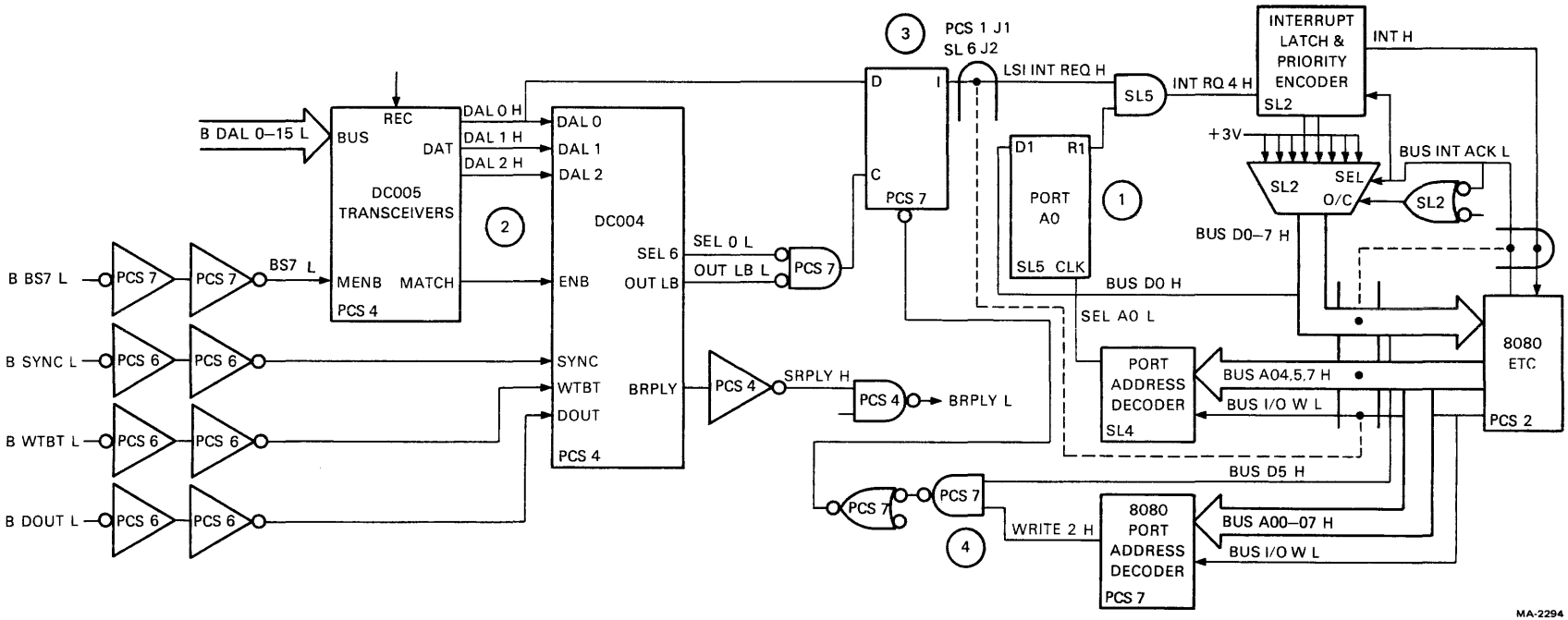


Figure 4-10 LSI Interrupt Request

APPENDIX A
LOGICAL DISCONNECTION OF A DPM 50 FROM THE HOST SYSTEM

Before downloading and running diagnostics on a DPM50, it is necessary to sever any open channel between it and the host system software. A channel may be open in one of the two following ways.

1. There may simply be an open channel established between an on-line DPM50 and host system software with no task actually using the channel. In this case, the procedure detailed below is sufficient to disconnect the DPM50 so that a diagnostic task may be attached to it.

2. There may be an active connection between a task in the host and one in the remote DPM50, as indicated by the status reporting task, ST5, detailed below.

WARNING: If an active connection exists, the channel should never be closed without permission from the system operator. The DPM50 is a process control device, and an untimely shutdown could cause a safety hazard.

PROCEDURE

1. Determine the DECdataway port numbers and corresponding SB numbers of the DPM50 to be diagnosed. The physical port addresses are associated with SB numbers in the operating system at SYSGEN time. On-line or off-line status of the SB numbers can be determined by using the command DEVices. In this example, the DPM50 is at DECdataway port addresses 1 and 2, SB numbers 1 and 2.

2. At an MCR terminal, type the following entry.

   ⟩ST5 (CR)

This prints a report of all open DPM50s. If the desired DPM50 does not appear, then it is not open and diagnostics can be run on it. The ST5 report looks like this (operator input is underlined):

```
⟩ST5 (CR)
DPM50 AT NODES 1, 2 LUNS2, 1 NAME=REMOTE
VCB 1 (RECV) AT 44560, STS=1502
VCB 2 (SEND) AT 44660, STS=0

DONE

⟩DLC/CL:1/NO:REMOTE (CR)
⟩ST5 (CR)

DONE

⟩
```

In this ST5 report, a DPM50 is shown with open channel at NODES (SB numbers) 1 and 2, temporary *L*ogical *U*nit *N*umber*S* (LUNS) 2 and 1, node *NAME* REMOTE. The *V*olume *C*ontrol *B*lock information is not important. However, if Status (STS) = OFFLINE, the DPM50 may be physically disconnected or powered down. Use the command DEVices to verify on-line and off-line status. This DPM50 does not have an ACTIVE CONNECTION reported, so it may be closed to allow diagnostics to attach to it.

The close command (CL:) for DLC has as an argument the lower of the two sequential SB numbers, in this case 1. The node name (NO:) is the word following NAME= in the first line of the ST5 report. After the DLC command to close the channel finished executing, the prompt character (⟩) prints. The close may take up to 30 seconds. Type ST5 again to verify that the operation was successful. If so, the DPM50 channel that was closed does not appear in the new ST5 report.

3. If an ACTIVE CONNECTION exists, the ST5 report looks like this:

```
⟩ST5 (CR)
DPM50 AT NODES 1, 2 LUNS 2, 1 NAME=REMOTE
VCB 1 (RECV) AT 44560, STS=1502
VCB 2 (SEND) AT 44660, STS=0
ACTIVE CONNECTION
WB AT 44210 HOST TASK=HEX1, REM TASK=REX1, STS=200

DONE
```

An active connection exists between a task in the host named HEX1 and a task in the DPM50 named REX1. Ask the system operator for permission, or ask for the tasks to be aborted, before closing the channel.

4. If a task has been running in the DPM50 LSI-11 microcomputer, not only does the connection between the task and the host need to be closed, the task within the DPM50 must be terminated. It can be terminated in any of the following ways.

   - Cycle the ENABLE/HALT switch on the DPM50 H333 master chassis.
   - Cycle the ON/OFF switch on the DPM50 H333 master chassis.
   - Run the CZKCHx serial bus exerciser between the host and the DPM50 in question.

APPENDIX B
SPECIAL CIRCUITS

B.1 DC003 INTERRUPT CONTROL (Figures B-1, B-2, and B-3)

The interrupt control chip is an 18-pin, 0.762 cm (0.300 in) center, DIP device. It provides circuits to perform an interrupt transaction in a computer system that uses a pass the pulse arbitration scheme. The device is used in peripheral interfaces and has two interrupt channels labeled A and B, with the A section at a higher priority than the B section. Bus signals use high impedance input circuits or high drive open collector outputs, which allow the device to attach directly to the computer system bus. Maximum current required from the V_{cc} supply is 140 mA.

B.2 DC004 I/O ADDRESS DECODER (Figures B-4, B-5, and B-6)

The protocol chip is a 20-pin 0.762 cm (0.300 in) center, DIP device. It functions as a register selector, providing signals necessary to control data flow into and out of up to four word registers (eight bytes). Bus signals can directly attach to the device because receivers and drivers are included on the chip. An RC delay circuit is provided to slow the peripheral interface response to data transfer requests. The circuit is designed so that if tight tolerance is not required, only an external 1K 20 percent resistor is necessary. External RCs can be added to vary the delay. Maximum current required from the V_{cc} supply is 120 mA.

B.3 DC005 BUS TRANSCEIVER (Figures B-7, and B-8)

The 4-bit transceiver is a 20-pin, 0.762 cm (0.300 in) center, DIP, low power Schottky device. Its primary use is in peripheral logic. In addition to the isolation function, the device also provides a comparison circuit for address selection and a constant generator, useful for interrupt vector addresses. The bus I/O port has high impedance inputs and high drive (70 mA) open collector outputs to allow direct connection to a computer's data bus. On the peripheral side, a bidirectional port is also provided, with standard TTL inputs and 20 mA three-state drivers. Data on this port is the logical inversion of the data on the bus side.

Three address jumper inputs are used to compare against three bus inputs and to generate the signal MATCH. The MATCH output is open-collector, which allows the output of several transceivers to be wired-ANDed to form a composite address match signal. The address jumpers can also be put into a third logical state that disconnects that jumper from the address match, allowing for "don't care" address bits. In addition to the

three address jumper inputs, a fourth high impedance input line is used to enable/disable the MATCH output.

Three vector jumper inputs are used to generate a constant that can be passed to the computer bus. The three inputs directly drive three of the bus lines, overriding control line action. Two control signals are decoded to give three operational states: receive data, transmit data, and disable. Maximum current required from the V_{cc} supply is 100 mA.

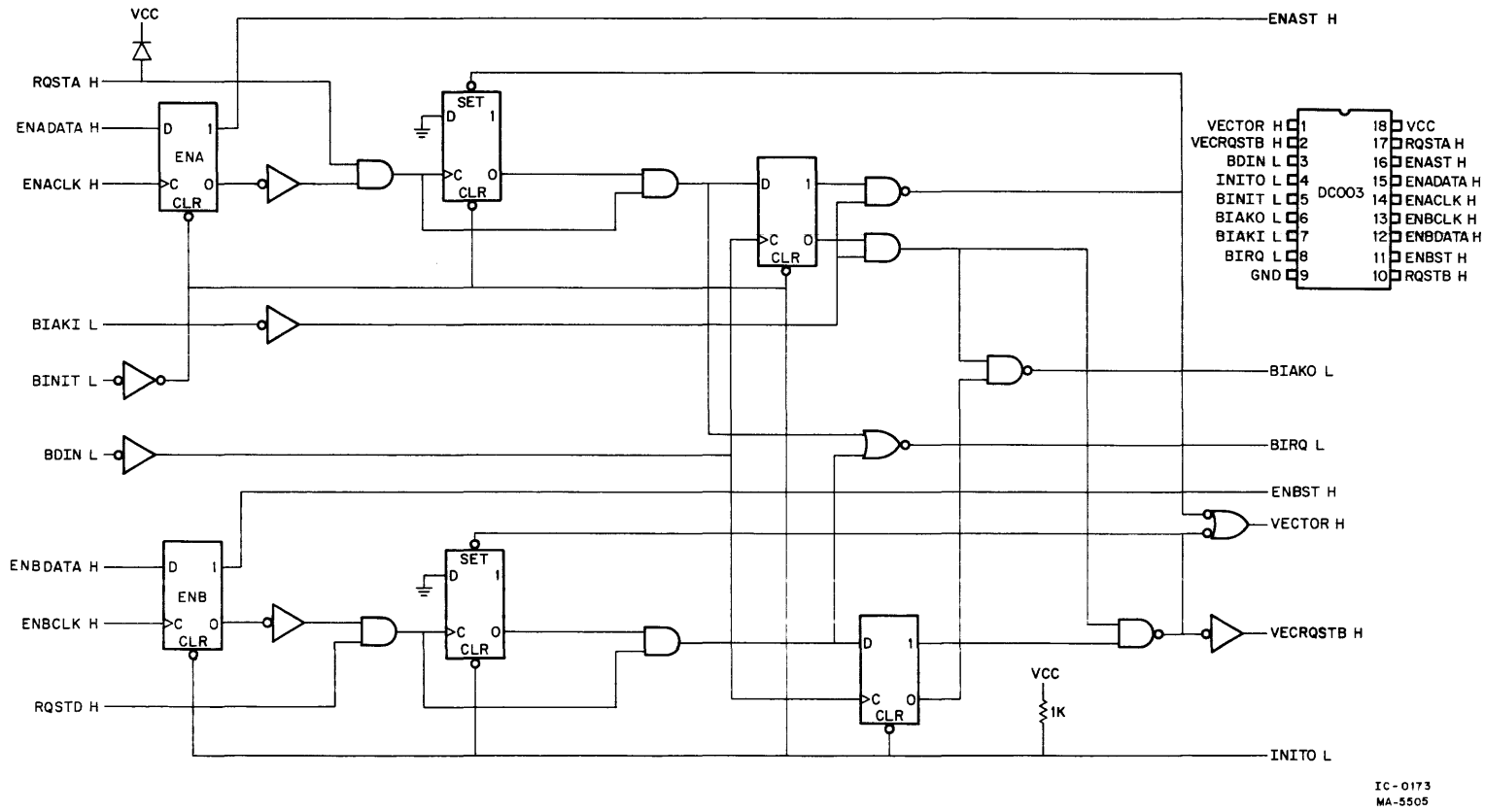


Figure B-1 DC003 Simplified Logic Diagram

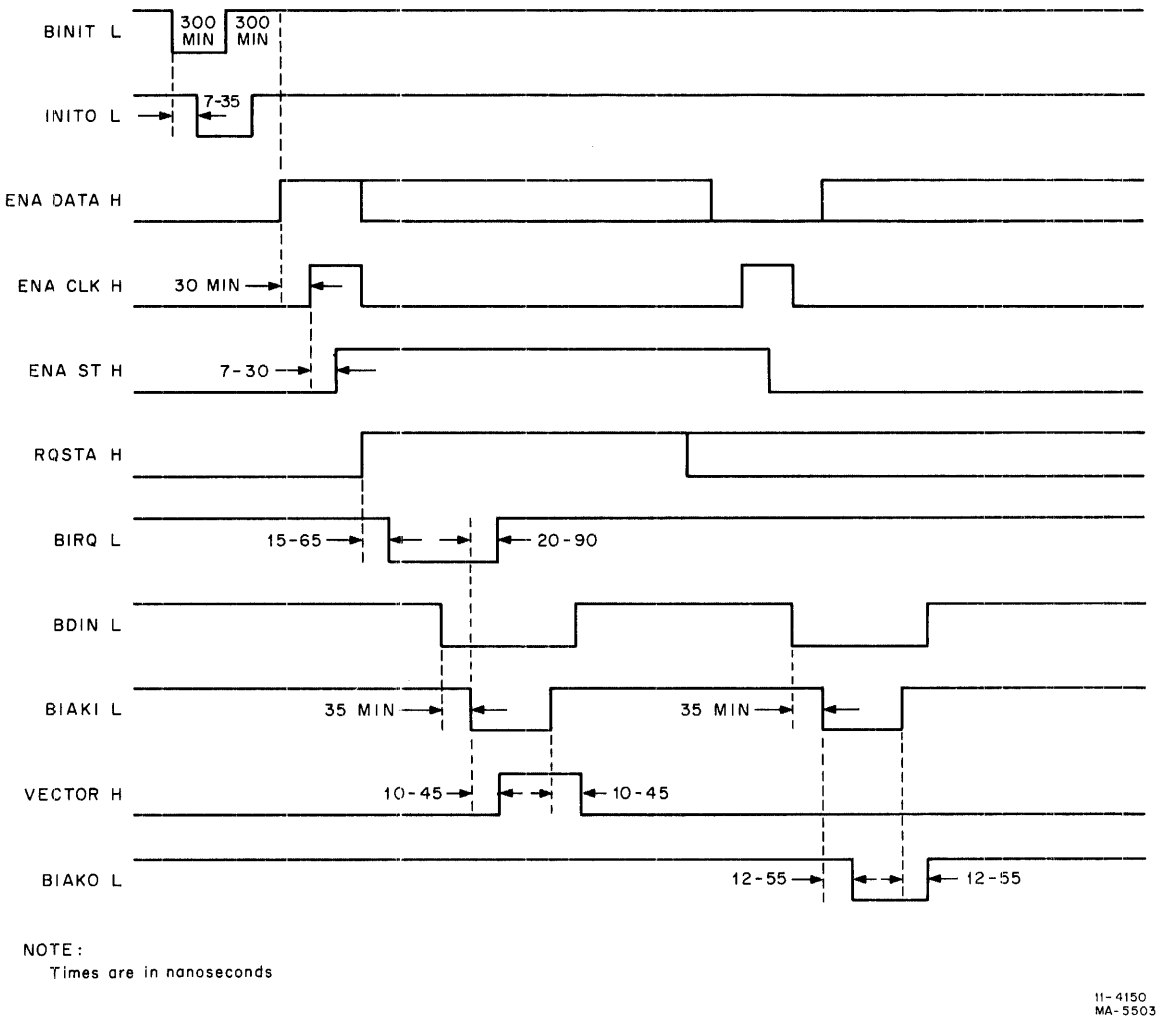
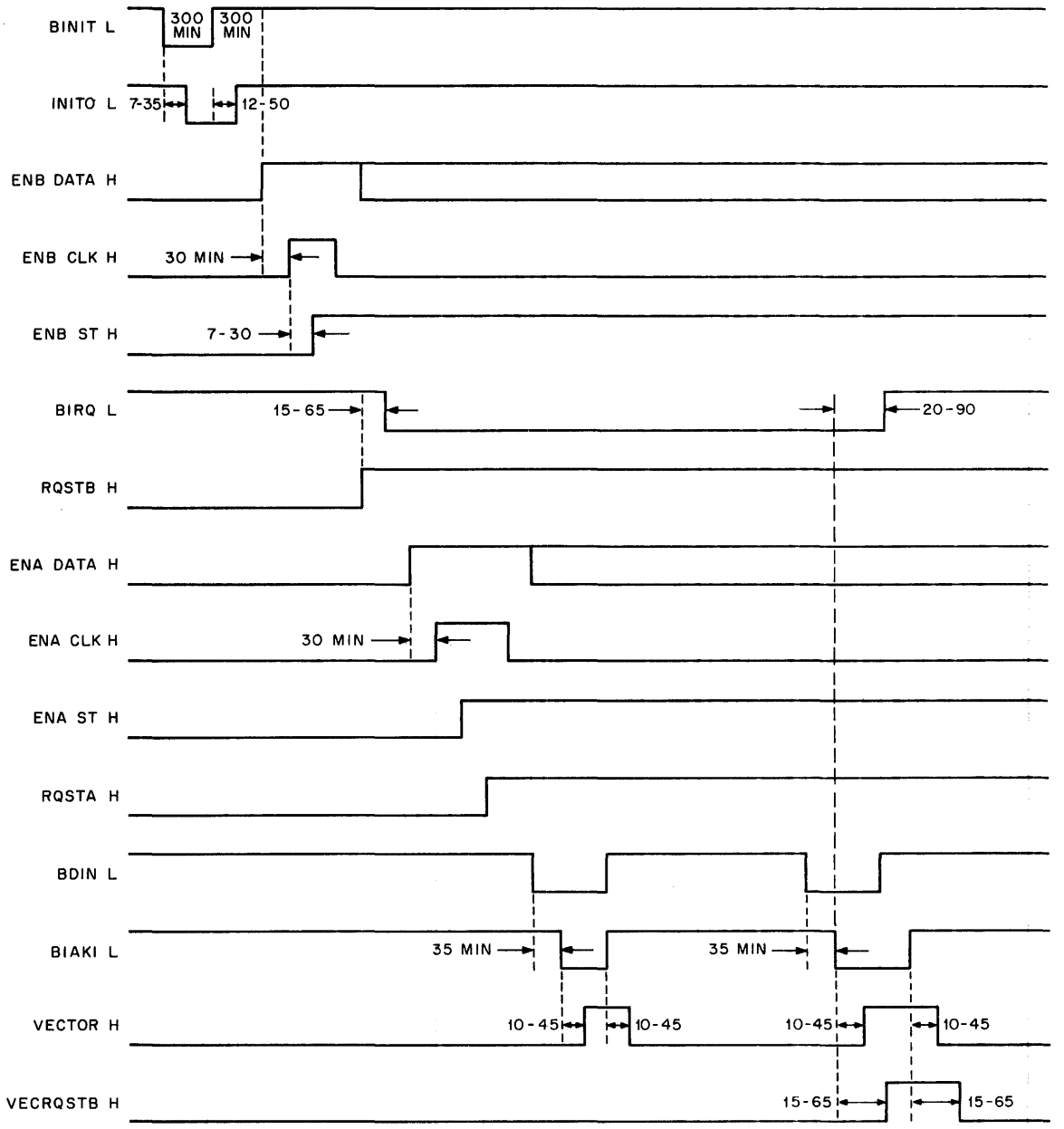


Figure B-2 DC003 Interrupt Section Timing Diagram



NOTE:
Times are in nanoseconds

11-4151
MA-5502

Figure B-3 DC003 Interrupt Section Timing Diagram
Sections A and B

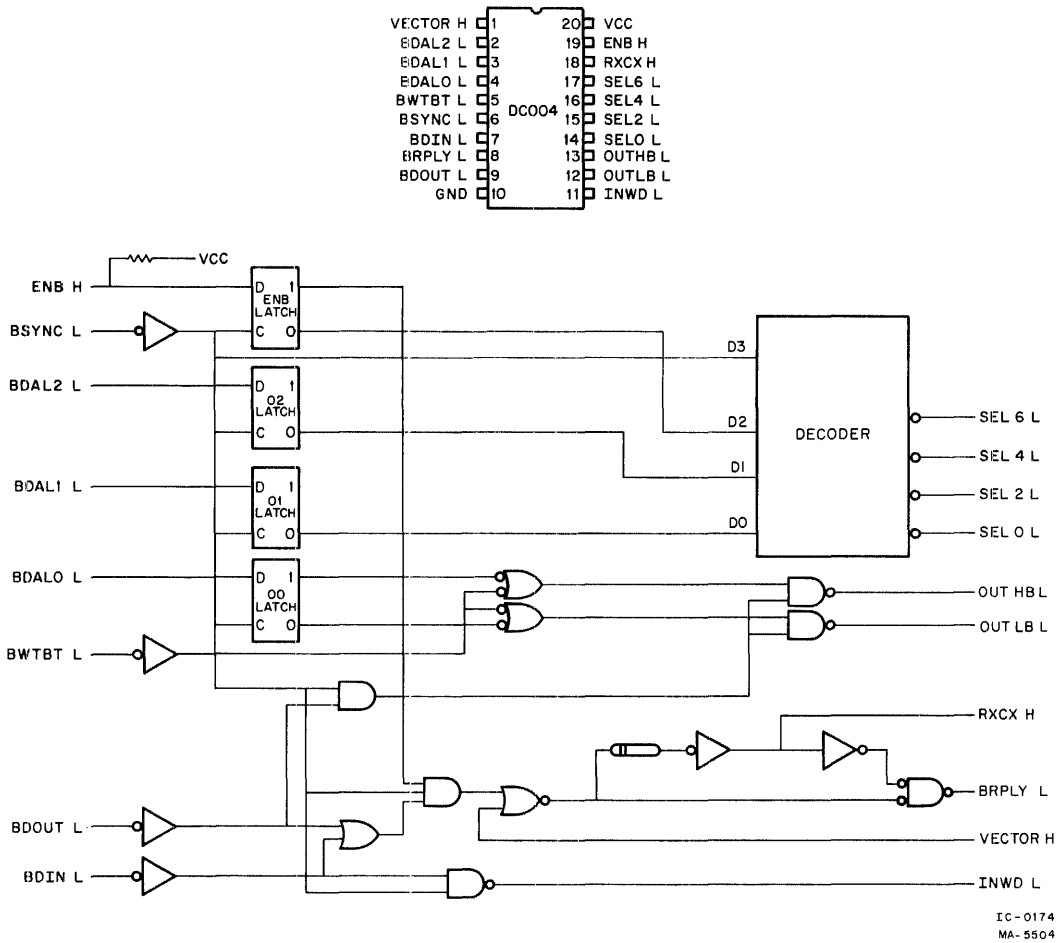


Figure B-4 DC004 Simplified Logic Diagram

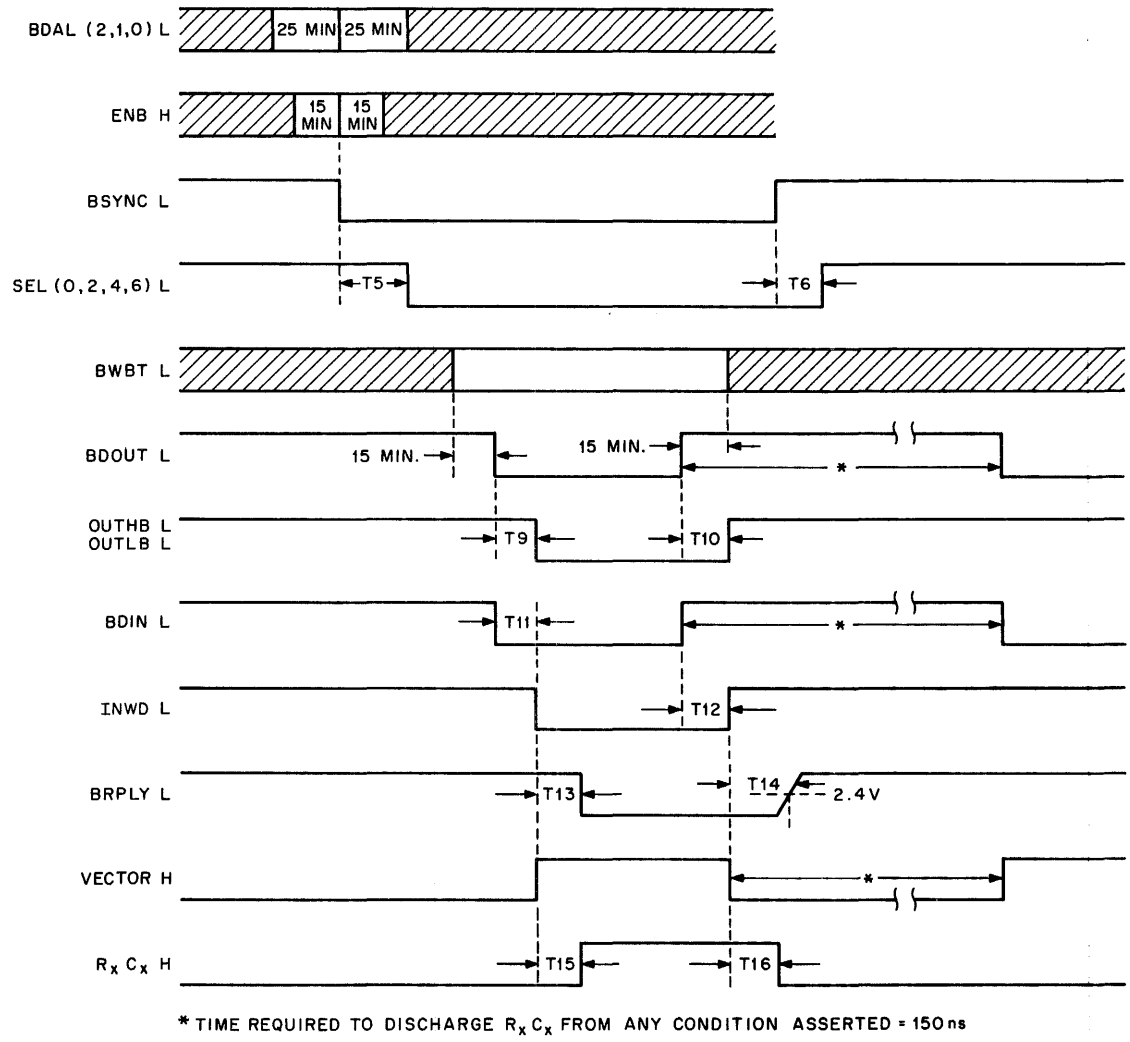


Figure B-5 DC004 Timing Diagram

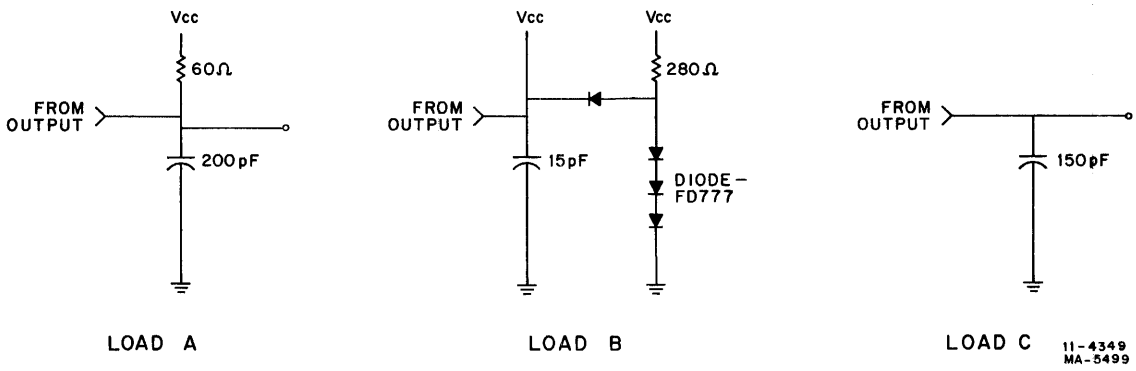


Figure B-6 DC004 Loading Configurations

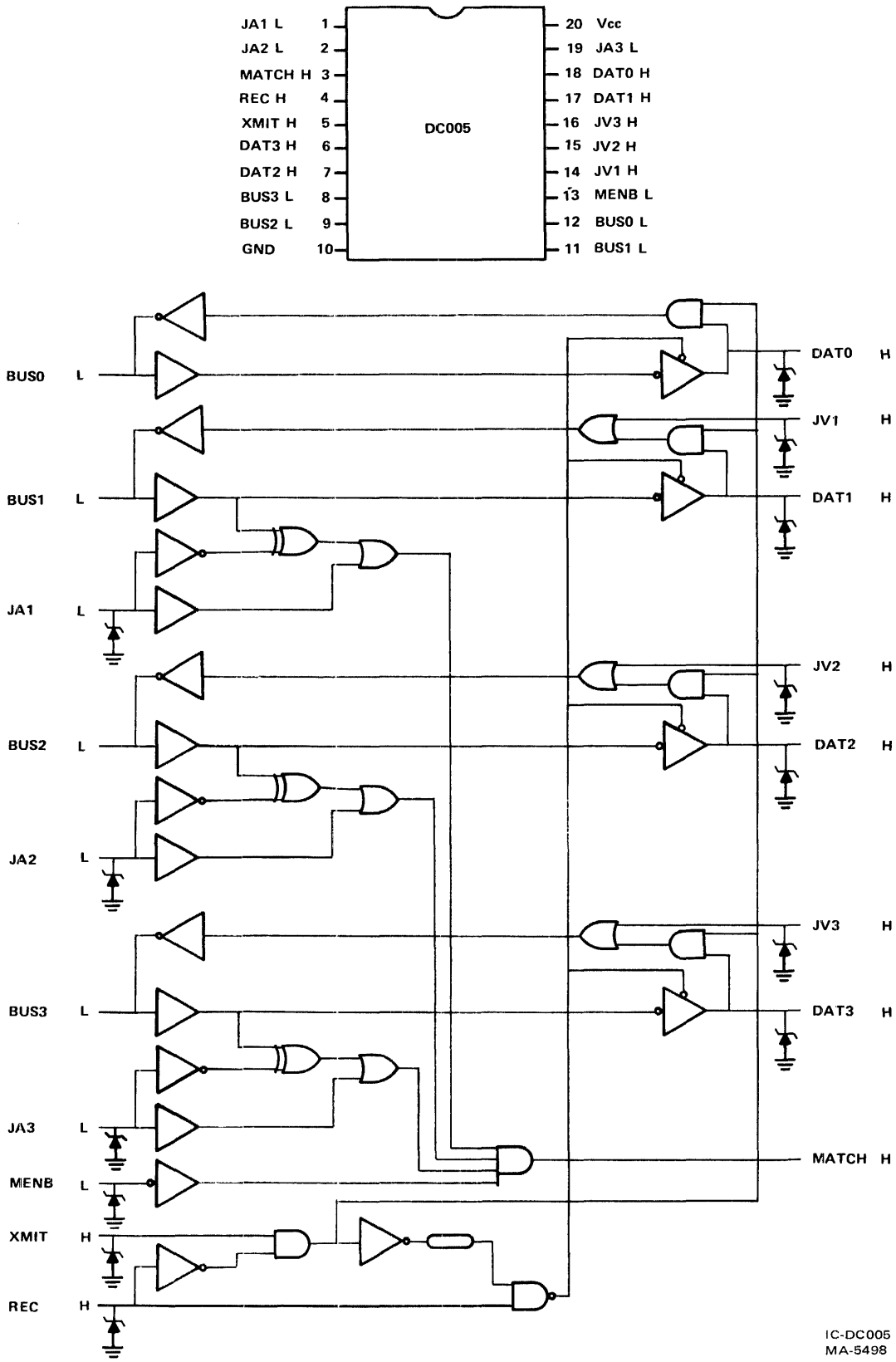


Figure B-7 DC005 Simplified Logic Diagram

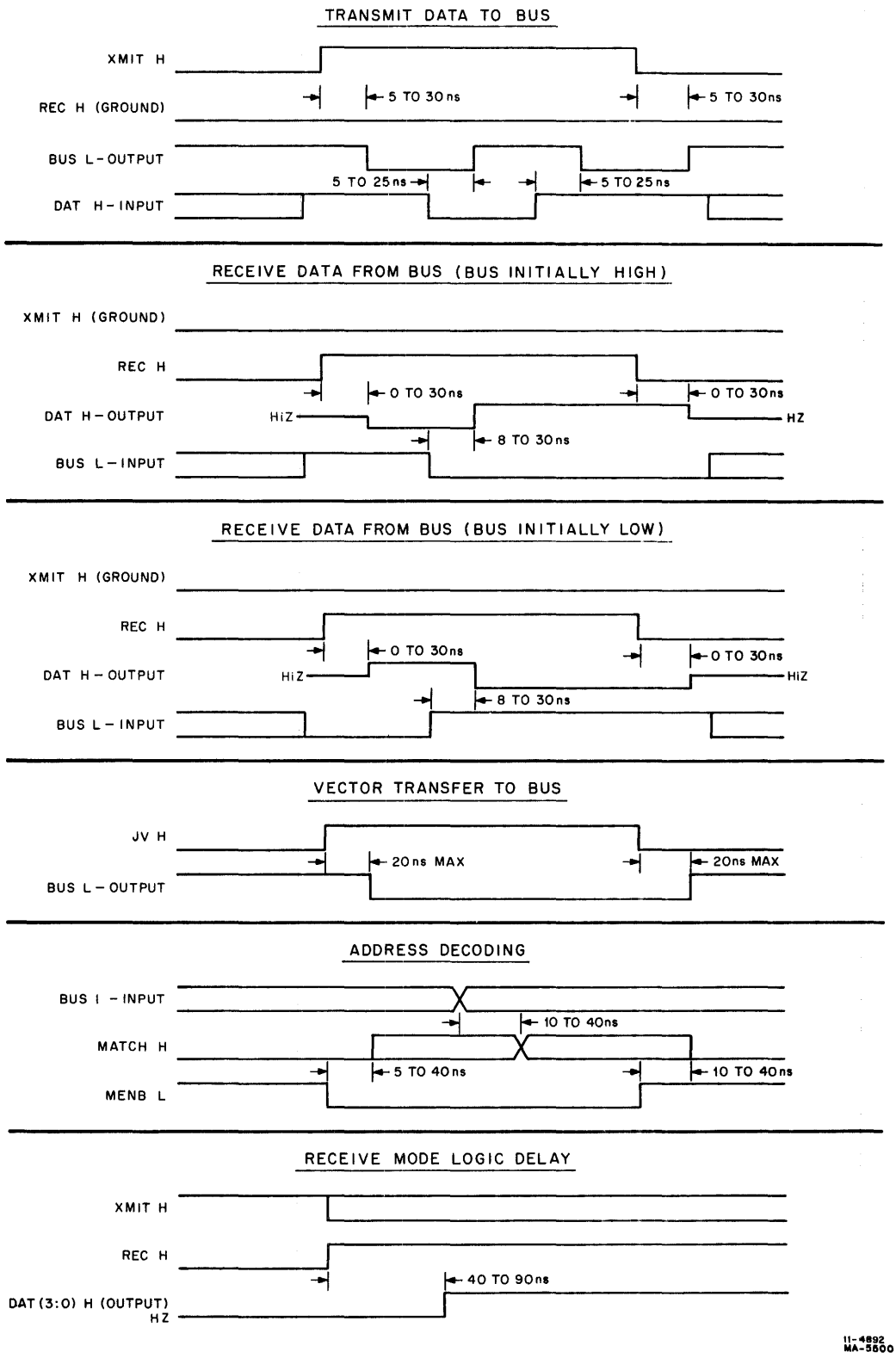


Figure B-8 DC005 Timing Diagram

SIGNAL GLOSSARY

This list identifies all signals that appear on the circuit schematics for the M8080 and 54-13290 boards, and gives the print on which each appear. Some bus signals are generated on several prints. Many LSI-11 bus signals originate outside the ISV11-A as well as inside it. A print designation in parentheses indicates a signal that appears on that print as an input but is never generated by the ISV11-A.

Signal	Print	Definition
ϕ1,2, CLOCK H	PCS2	2 MHz clocks generated by the 8224 for the 8080
ϕ2 TTL H	PCS2	2 MHz clocks generated by the 8224 for the USYNRT
1X CLK H	SL1	Equals T CLOCK H
2X CLK H	SL1	For biphase encoding, this clock has twice the frequency of T CLOCK
8X CLK H,L	SL1	Intermediate signal in transmitter clock (eight times dataway bit rate)
0 H 330 H 440 H 550 H	PCS6	Timing signals for DMA
AD 15-17 H	PCS7	High order address bits for DMA
BAD 16,17 L	PCS7	Expansion address bits for LSI-11 bus
B BS7 L	PCS7	Bank select 7 — LSI-11 bus signal to select I/O page in LSI-11 address space

Signal	Print	Definition
B DAL 0-15 L	PCS4	LSI-11 bus data and address lines
B DCOK H	PCS7	LSI-11 bus dc power okay
B DIN L	PCS6	LSI-11 bus — master requesting input, or LSI-11 getting vector address in response to interrupt
BDMGI L	(PCS5)	LSI-11 bus DMA grant in
BDMGO L	PCS5	LSI-11 bus DMA grant out
B DMR L	PCS5	LSI-11 bus DMA request
B DOUT L	PCS6	LSI-11 bus — master has data available for output
B HALT L	PCS7	LSI-11 bus — halt processor
BIAKI L	(PCS4)	LSI-11 bus interrupt acknowledge in
BIAKO L	PCS4	LSI-11 bus interrupt acknowledge out
B INIT L	(PCS4)	LSI-11 bus — in ISV11-A initializes only interrupt control
BIRQ L	PCS4	LSI-11 bus interrupt request (to LSI-11)
BOOT LSI H	PCS7	Boots LSI-11 by simulating power up (through control of B DCOK)
BPOK H	(PCS5)	LSI-11 bus ac power okay
BRPLY L	PCS4	LSI-11 bus reply
BS7 H	PCS7	Bank select 7 for I/O page — conditions TBS7 when address placed on LSI-11 bus
B SACK L	PCS5	LSI-11 bus — acknowledges that ISV11-A has been granted master status in DMA operation

Signal	Print	Definition
B SYNC L	PCS6	LSI-11 bus — master has placed address on bus
BUS A00 L	PCS7	From BUS A00 H
BUS A00-15 H	PCS2	8080 bus address lines
BUS D0-7 H	PCS2,3,7 SL2,4	8080 bus data lines
BUS D^2 DAL HB L	PCS8	8080 data to LSI-11 bus high byte
BUS INT ACK L	PCS2	8080 interrupt acknowledge
BUS I/O R L	PCS2	8080 reading an I/O register (port)
BUS I/O W L	PCS2	8080 writing an I/O register (port)
BUS OUT EN L	SL2	8080 reading local memory or receiving interrupt RST
BUS MEMR L	PCS2	8080 reading memory or I/O register addressed as memory
BUS MEMW L	PCS2	8080 writing memory or I/O register addressed as memory
B WTBT L	PCS6	LSI-11 bus write/byte
CARRIED LED	SL1	Controls carrier detected LED
CPU SYNCH H	PCS2	8080 signal to 8224 to indicate first state in each machine cycle
DAL 0-15 H	PCS4, 7	Data and address lines on LSI-11 bus extension
DAL LB^2 BUS D L	PCS8	LSI-11 bus data low byte to 8080
DIN L	PCS6	Received B WTBT
DIS 8X CLK L	SL6	GR test disable for 8X CLK
DIS I/O L	SL6	GR test disable for 8080 I/O address decoder

Signal	Print	Definition
DIS MEM L	SL6	GR test disable local memory
DIS RAW DATA L	SL6	GR test disable receiver
DMA ACK H	PCS6	DMA request has been acknowledged by LSI-11 bus
DMA MEMR H	PCS5	8080 reading in LSI-11 address space
DMA MEMW H	PCS5	8080 writing in LSI-11 address space
DMR H,L	PCS5	DMA request — generates B DMR for 8080 to access LSI-11 address space
DOUT L	PCS6	Received B DOUT
DROPOUT H,L	SL1	Dataway signal absent
DROPOUT L^2 H OR RSA H	SL5	Dataway signal dropped out (1-1/2 bit times sans transition) or USYNRT receiver status available
ENA DMA H	PCS5	8080 addressing LSI-11 space
EXT 8X CLK L	SL6	8X CLK at test socket, or can be used for external clock if DIS 8X CLK
EXT RAW DATA H	SL6	RAW DATA at test socket, or can be used for external data if DIS RAW DATA
EXT R CLOCK L	SL6	External test receiver clock for USYNRT
EXT R DATA L	SL6	External test received data for USYNRT
FRPLY H,L	DCS6	Forced bus reply
HALT LSI H	PCS7	Generates B HALT
INT H	SL2	Interrupt to 8080

Signal	Print	Definition
INT Q BUS A H	PCS4	LSI-11 bus interrupt control waiting for interrupt on A level or has vector 300 on B DAL lines
INT RQ 4-7 H	SL5	Interrupt requests to 8080
INWD L	PCS4	From B DIN sent by LSI-11 for CSR
I/O PAGE L	PCS2	8080 addressing I/O register as memory location
I/O R L	PCS2	8080 IN instruction (I/O read)
I/O W L	PCS2	8080 OUT instruction (I/O write)
I/O WR H	PCS7	Equals I/O R "OR" I/O W
JA	PCS4	Jumper address inputs to DC005s
JAV	PCS4	Jumper vector address inputs to DC005s
LITE 1-4 L	PCS7	Control M8080 LEDs
LSI INT REQ H	PCS7	Equals CSR0 bit 0; this is an LSI-11 request for an 8080 interrupt
MARGIN −5 V	SL6	GR test margin for −5 V for PROMs
MATCH	PCS4	Address on B DAL equals jumper address (JA) on DC005s (LSI-11 addressing ISV11-A CSRs)
MEM BUS D0-7 H	SL2,3	Data bus for output from local memory
MEMR H	PCS5	Equals BUS MEMR
MEMW H	PCS5	= BUS MEMW
MEM SEL L	SL2	8080 accessing local memory
MENB	PCS4	Enables match with JA in DC005s

Signal	Print	Definition
OUT HB H	PCS3	From OUT HB I
OUT HB L	PCS4	LSI-11 loading CSR high byte
OUT LB H	PCS3	From OUT LB L
OUT LB L	PCS4	LSI-11 loading CSR low byte
PHASE-LOCKED CLK H	SL1	A clock (train) geared to last signal transition detected on dataway
PORT ADDR 1-6 H	(SL4)	Port address wired into dataway connector
R110 H	PCS6	Reset time for DMA
RAM SEL L	SL3	8080 accessing the RAM
RAW DATA L	SL1	Output of modem receiver circuit
R BS7 L	PCS7	Received B BS7
R CLOCK H,L	SL1	Receiver clock derived from incoming bit stream
RDA H	SL5	USYNRT output — received data available
R DATA H,L	SL1	Modem received data output to USYNRT
R DCOK L	PCS7	Received B DCOK
READ 8X L	SL4	8080 reading I/O register in address range 80-87
READ CSR L	PCS7	LSI-11 reading CSR !
READY H	PCS2	Pulled down by the 8224 on a wait to idle the 8080
REC H	PCS4	ISV11-A is not now sending information on LSI-11 bus B DAL lines
RESET 1 H	PCS2	Generated by 8224 when BPOK H goes down

Signal	Print	Definition
RESET H,L	PCS2	Equals RESET 1
RESET H,L	SL6	5413290 reset from PCS2 RESET L
R HALT H	PCS7	Received B HALT
RPOK L	PCS5	Received BPOK
RRPLY H,L	PCS4	Received BRPLY
RSA H	SL5	USYNRT output — receiver status available
RX ACT H	SL5	USYNRT receiver active
SACK H	PCS5	Send B SACK for DMA
SEL 0,2,4 L	PCS4	CSR address decoder outputs
SEL 8X H	SL4	8080 accessing I/O register in address range 80-87
SEL 90 L	SL4	8080 reading I/O register 90 (USYNRT status)
SEL A0 L	SL4	8080 writing I/O register A0 (USYNRT control)
SEL B0 L	SL4	8080 reading I/O register B0 (port address)
SELECT 1-5 L	PCS7	Address decoder outputs for 8080 I/O registers in Q bus interface
SRPLY H	PCS4	Send BRPLY
STROBE	PCS2	Send 8224 to 8228 in response to CPU SYNC; latches 8080 cycle status in 8228
SYNC L	PCS6	Received B SYNC
T ADDR EN H,L	PCS6	Transmit address on B DAL for DMA
TBMT H	SL5	USYNRT transmit buffer empty

Signal	Print	Definition
TBS7 H	PCS7	Transmit B BS7
T CLOCK H	SL1	Transmitter clock — 55,556 KHz
T DATA H	SL5	USYNRT serial data output
T DATA EN H,L	PCS6	Transmit data on B DAL for DMA
T DIN H	PCS6	Transmit B DIN for DMA
T DOUT H	PCS6	Transmit B DOUT for DMA
T ENA H,L	SL5	Enable modem transmitter (when USYNRT transmitter active but not in maintenance mode)
TEST DISABLE 8080 L	PCS6	GR test disable 8080 operation
TEST DISABLE I/O L	PCS6	GR test disable 8080 I/O register addressing
TME H	PCS7	Timeout enable for DMA
TMO H	PCS7	DMA timeout
TMO ERR H	PCS7	Timeout error status bit (8080 to LSI-11)
TRANSITION DETECTED H	SL1	Receiver detected a zero-crossing
TRANSITION DLYD L	SL1	Transition detected inverted and delayed 500 ns.
T RAW DATA H	SL1	Flip-flop biphase-encoded data signal applied to transmitter circuit
T SYNC H	PCS6	Transmit B SYNC for DMA
T WTBT H	PCS6	Transmit B WTBT for DMA
TX ACT H	SL5	USYNRT transmitter active
VEC RQST B H	PCS4	Makes vector jumper address 304 when VECTOR is true

Signal	Print	Definition
VECTOR H	PCS4	Places vector jumper address (JAV) on B DAL when the 8080 interrupts the LSI-11
WAIT L	PCS2	Puts 8080 in wait state until DMA acknowledged
WRITE 1,2 H	PCS7	Select 8080 I/O registers 1 and 2 for writing
WTBT L	PCS6	Received B WTBT

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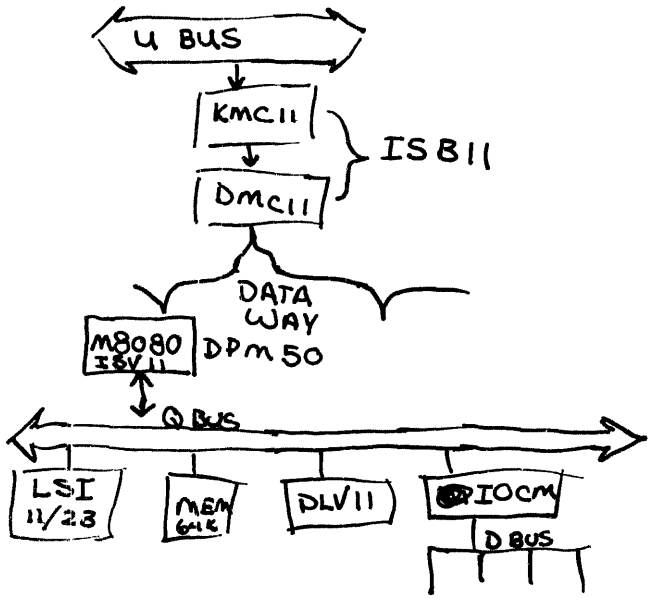
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