EK-11070-MM-002

PDP-11/70
maintenance and installation manual

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TABLES

CHAPTER 1
GENERAL DESCRIPTION

This chapter contains configuration information and lists of Technical Manuals and Engineering Drawings related to the PDP-11/70.

1.1 BASIC SYSTEM DESCRIPTION

The basic PDP-11/70 system components are located in a double cabinet (Figure 1-1). The cabinet on the left contains the KB11-B processor, the options for which the processor backplane is prewired, and certain optional peripheral devices which may be installed above the processor mounting box (Table 1-4). The cabinet on the right may contain only memory; a second memory cabinet may be installed to its right. The TU16 Magtape Drives are installed to the right of the memory cabinets. All other optional cabinets are installed to the left of the processor cabinet.

Table 1-1 lists the items supplied with the minimum PDP-11/70 configuration.

Table 1-2 lists the options that may be installed into prewired slots in the processor backplane.

Table 1-3 lists the available MJ11 memory options.

Table 1-4 lists the available MK11 memory options.

Table 1-5 lists the options that may be installed in the upper half of the processor cabinet.

A PDP-11/70 block diagram is shown in Figure 1-2. The PDP-11/70 system is compatible with the standard Unibus interface, with the exception of memory, which is on its own dedicated bus. Any other Unibus device may be used with the PDP-11/70. These devices are listed in Appendix F to this Manual.

An H960-C expansion cabinet option is available with the PDP-11/70 system. It is not included as part of the basic system, but may be ordered as required to house additional Unibus peripheral devices. No memory may be connected to the Unibus except through special arrangement with CSS (Computer Special Systems). The basic components that may be included in each expansion cabinet option are summarized in Appendix F. Chapter 4 provides instructions for interconnecting the H960-C remote power control to the CPU (Central Processor Unit) Cabinet Assembly.

The H960-C cabinet includes an 861-D or E power control and may be used to mount up to four BA11-K mounting boxes, each of which can house up to five system units. The BA11-K mounting box is described in the *BA11-K Mounting Box Manual,* EK-BA11K-MM-002.

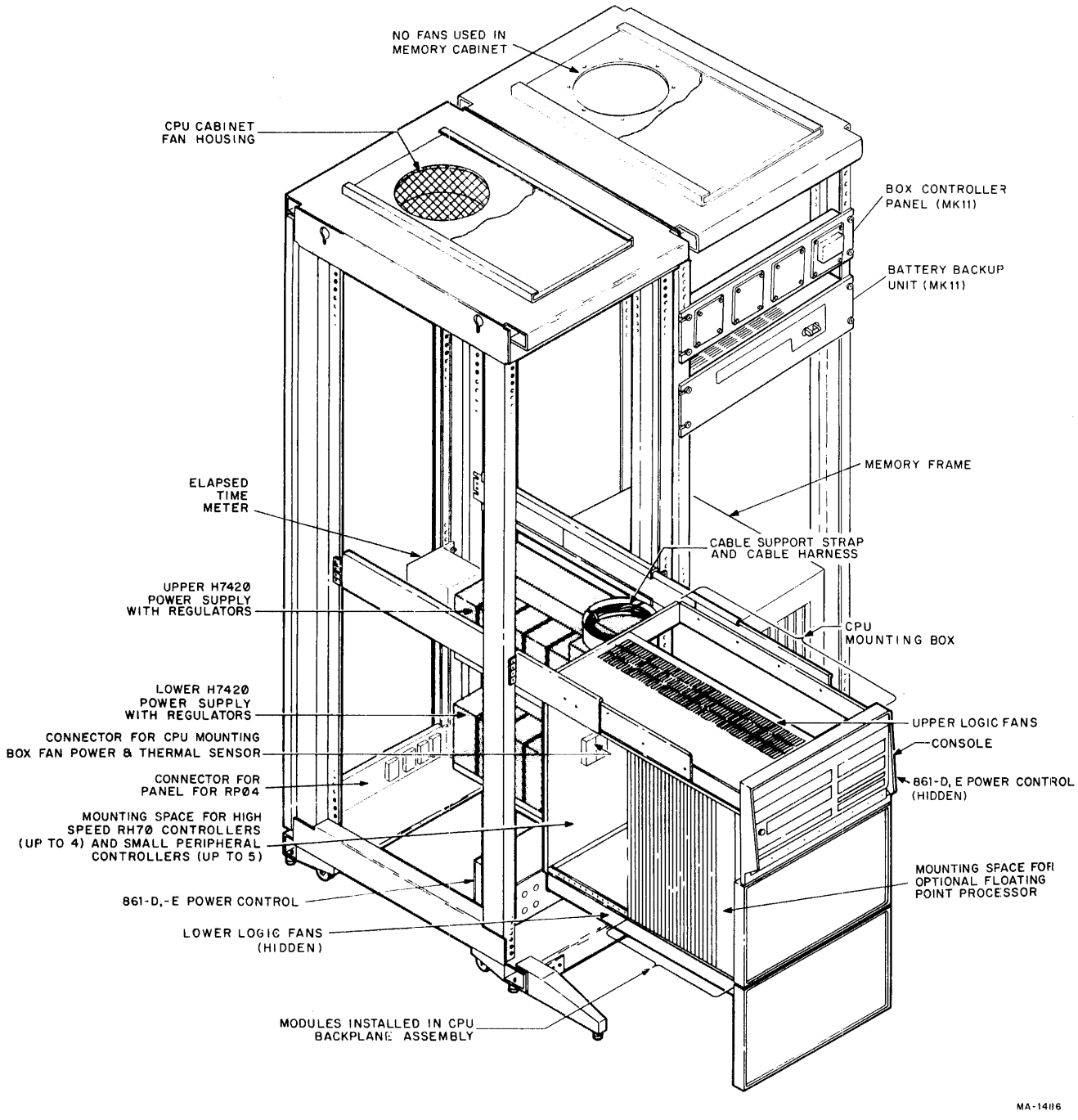


Figure 1-1 Location of Major Components and Assemblies

Table 1-1 Minimum PDP-11/70 Configuration

Item	Description
Cabinet Assembly	Refer to Figure 1-1. Consists of one processor cabinet and one memory cabinet.
	Processor Cabinet
CPU Mounting Box	Refer to Figure 1-1. Houses KB11-B/C processor, DL11-A and KW11-L or DL11-W, and M9301-YC/YH or M9312. The M9302 Unibus terminator is located at the end of the Unibus. If no Unibus devices are used outside of the CPU mounting box, the M9302 is inserted in slot 44, rows A and B. The CPU mounting box is also prewired for four optional RH70 controllers, a floating point processor and four additional small peripheral controllers (SPC).
KB11-C Processor	Basic 16-bit processor modules installed in wired CPU backplane (part number 7011051, Rev. D or higher). Accepts FP11-C Floating Point Processor option.
Consists of the following:	
M8130 DAP Module	Data Paths (slot 6)
M8131 GRA Module	General Registers and ALU control (slot 7)
M8132 IRC Module (CS REV. B or higher)	IR decode and Condition Codes (slot 8)
M8133 RAC Module	ROM and ROM Control (slot 9)
M8134 PDR Module	Processor Data and Unibus Registers (slot 10)
M8135 TMC Module	Trap and Miscellaneous Control (slot 11)
M8136 UBC Module	Unibus and Console Control (slot 12)
M8137 SAP Module	System Address Paths (slot 14)
M8138-YA SSR Module	System Status Registers (slot 15)
M8139 TIG Module	Timing Generator (slot 13)
M8140 SCC Module	System Descriptor/Console Cables (slot 16)
M8141 MAP Module	Unibus Map (slot 22)
M8142 CCB Module	Cache Control (slot 17)
M8143 ADM Module	Address Memory (slot 18)
M8144 DTM Module	Data Memory (slot 20)
M8145 CDP Module	Cache Data Paths (slot 21)
5411294 KNL Module	Console

Table 1-1 Minimum PDP-11/70 Configurations (Cont)

Item	Description
	Processor Cabinet (Cont)
KB11-B Processor	Basic 16-bit processor modules installed in wired CPU backplane (part number 7011051, any Rev.). Accepts FP11-B Floating Point Processor option.
Consists of the following:	
M8130 DAP Module	Data Paths (slot 6)
M8131 GRA Module	General Registers and ALU Control (slot 7)
M8132 IRC Module	IR Decode and Condition Codes (slot 8)
M8133 RAC Module	ROM and ROM Control (slot 9)
M8134 PDR Module	Processor Data and Unibus Registers (slot 10)
M8135 TMC Module	Trap and Miscellaneous Control (slot 11)
M8136 UBC Module	Unibus and Console Control (slot 12)
M8137 SAP Module	System Address Paths (slot 14)
M8138 SSR Module	System Status Registers (slot 15)
M8139 TIG Module	Timing Generator (slot 13)
M8140 SCC Module	System Descriptor/Console Cables (slot 16)
M8141 MAP Module	Unibus Map (slot 22)
M8142 CCB Module	Cache Control (slot 17)
M8143 ADM Module	Address Memory (slot 18)
M8144 DTM Module	Data Memory (slot 20)
M8145 CDP Module	Cache Data Paths (slot 21)
5411294 KNL Module	Console
DL11-A/W Asynchronous Serial Line Interface	LA36 Interface to Unibus. Described in related Manual (slot 40, rows C–F)
KW11-L Line Time Clock	Provides a signal for each cycle of the Tower line. Described in related Manual (slot 1, row D).
M9301-YC/YH, M9312	Unibus terminator and PDP-11/70 bootstrap loader and diagnostic (slot 1, rows E–F).
M9302	Unibus terminator (slot 44, rows A–B). See CPU Mounting Box.
H7420 Power Supplies	Refer to Figure 1-1. Two H7420s contain the dc power regulators for the CPU mounting box.
H744 +5 Regulators	Seven H744 +5 Vdc regulators supply dc power. Three H744s are mounted in the upper H7420 and four in the lower H7420. An additional H744 is required (slot A in upper H7420) if floating point processor is installed.
5411086 Modules	Each H7420 contains one 5411086 module which monitors the ac input voltage in addition to its function as a 15 Vdc regulator. The upper H7420 supplies +15 Vdc, the lower, –15 Vdc.

Table 1-1 Minimum PDP-11/70 Configurations (Cont)

Item	Description
Processor Cabinet (Cont)	
861-D (115 V) or 861-E (230 V) Power Control	Refer to Figure 1-1. Controls ac power input.
Memory Cabinet (MJ11)	
Memory Frame	Consists of a slide-mounted drawer, an MJ11 etched backplane, two H744 +5 Vdc regulators, two H754 +20, -5 Vdc regulators, one ac input box (which contains a 5411086 power line monitor), and one MJ11 memory controller.
The Memory Controller consists of the following:	Each controller can handle up to a total of four 16K word module pairs (256KB) or 32K word module pairs (512KB).
M8147/M8148 MCT Module*	Memory Control and Timing (slot 13)
M8149 MXR Module	Memory Transceiver Card (slot 14)
16K Word Modules (MJ11-A) } 18 bit words 32K Word Modules (MJ11-B) }	The system requires a minimum of 32K words (64KB) of MJ11-AA or 64K words (128KB) of MJ11-B memory and a memory controller to run the diagnostics. Refer to Figure 3-16 for placement of modules.
MJ11-A memory module pairs (64KB per pair) consist of two of the following:	
G114 SIN Module	Sense/Inhibit Module (slots 1, 4, 21, 24)
H217C STK Module	Stack Module (slots 2, 5, 22, 25)
G235 DRV Module	Drive Module (slots 3, 6, 23, 26)
MJ11-B memory module pairs (128KB per pair) consist of two of the following:	
G116 SIN Module	Sense/Inhibit Module (slots 1, 4, 21, 24)
H224C STK Module	Stack Module (slots 2, 5, 22, 25)
G236 DRV Module	Drive Module (slots 3, 6, 23, 26)
861-D (115 V) or 861-E (230 V) Power Control	Controls ac power input. See related manual.

*M8147 can be used in MJ11-A or MJ11-B; M8148 can only be used in MJ11-A.

Table 1-1 Minimum PDP-11/70 Configurations (Cont)

Item	Description
Memory Cabinet (MK11)	
Memory Frame	Consists of a slide-mounted drawer, an MK11 etched backplane, one H7441 +5 Vdc regulator, three 7014251 ±12 Vdc, +5 Vdc regulators, an ac input box, and interface and control modules.
Interface and Control Modules	
M8158	Address Interface Module
M8159	Data Buffer Module
M8160	Control A Module (2)
M8161	Control B Module (2)
Memory Modules	
MS11-KE	32K words MOS Array Module (4K MOS RAM chips).
Box Controller	Operator and maintenance control switches and indicators.
Battery Backup Units	Three H755 battery chargers and battery packs.
861-D (115 V) or 861-E (230 V) Power Control	Controls ac power input; see related manual.
Item not in Cabinets	
LA36 DECWRITER II	Serial I/O terminal. Described in related manual.

Table 1-2 Processor Backplane Options

Option	Description
FP11-C Floating-Point Processor	
Consists of the following:	Used with KB11-C Processor. Described in related manual. Logic modules mount in CPU backplane in slots indicated.
M8128 FRM Module	FP ROM and ROM control (slot 4)
M8129 FXP Module	FP exponent and data path (slot 5)
M8126 FRH Module	Fraction data path – high order (slot 2)
M8127 FRL Module	Fraction data path – low order (slot 3)
H744 +5 V Module	Mounts in space provided on upper H7420 Power Supply (slot A).
FP11-B Floating-Point Processor	
Consists of the following:	Used with KB11-B Processor. Described in related manual. Logic modules mount in CPU backplane in slots indicated.
M8112 FRM Module	FP ROM and ROM control (slot 4).
M8113 FXP Module	FP exponent and data path (slot 5).
M8114 FRH Module	Fraction data path – high order (slot 2).
M8115 FRL Module	Fraction data path – low order (slot 3).
H744 +5 V Module	Mounts in space provided on upper H7420 Power Supply (slot A).
High-Speed I/O Controllers (RH70)	
	Up to four RH70 Massbus controllers can be installed in prewired slots in the CPU backplane. Controller A in slots 24–27 Controller B in slots 28–31 Controller C in slots 32–35 Controller D in slots 36–39
Each controller consists of the following:	
M5904 MBS Module	Massbus transceivers (3 required) (slots 25–27, 29–31, 33–35 or 37–39, rows A and B).
M8150 MDP Module	Data buffer and parity (slots 24, 28, 32 or 36, rows A–F).
M8151 CST Module	Control and status (slots 25, 29, 33 or 37, rows C–F).

Table 1-2 Processor Backplane Options (Cont)

Option	Description
High-Speed I/O Controllers (RH70) (Cont)	
M8152 AWR Module	Word count and address (slots 26, 30, 34 or 38, rows C–F).
M8153 BCT Module	Unibus and register logic (slots 27, 31, 35 or 39, rows C–F).
	Each RH70 can control up to eight devices which must be of the same type.
Available Massbus options:	
TWU16	One RH70 Controller, up to eight TM02 formatters, each of which can control up to eight TU16 Magtape Drives.
RWP04	One RH70 Controller, up to eight RP04 Disk Drives.
RWS03	One RH70 Controller, up to eight RS03 Disk Drives.
RWS04	One RH70 Controller, up to eight RS04 Disk Drives.
DWR70	General Purpose Massbus Interface.
Small Peripheral Controllers (SPC)	
	Slots 41 through 43 (rows A through F) and slot 44 (rows C–F) are prewired for SPC. Refer to Appendix F and to the PDP-11 Peripheral Handbook.

Table 1-3 MJ11 Memory Options (see Figure 1-3)

Item	Description
MJ11-AE	64K byte (32K 16-bit word) memory module used to increase the amount of memory in a memory frame.
Consists of two of each of the following:	
G114 SIN Module	Sense/Inhibit Module (slots 4 and 21, 7 and 18 or 10 and 15).
H217C STK Module	Stack Module (slots 5 and 22, 8 and 19, or 11 and 16).
G235 DRV Module	Drive Module (slots 6 and 23, 9 and 20, or 12 and 17).
MJ11-AA (115 V), -AB (230 V)	Memory expansion frame. Must be mounted in an MJ11 memory cabinet.
Consists of the following:	
Memory Frame	Slide mounted drawer, MJ11 etched backplane, two H744 +5 Vdc regulators, two H754 +20, -5 Vdc regulators, ac input box and MJ11 Memory Controller.
The memory controller consists of the following:	
M8148 MCT Module	Memory Control and Timing (slot 13)
M8149 MXR Module	Memory Transceiver Card (slot 14)
One 64K byte (32K 16-bit word) memory module	Same as MJ11-AE.
MJ11-AG (115 V), -AH (230 V)	Memory expansion frame. Must be mounted in MJ11 memory cabinet. Same as MJ11-AA(AB) described above, but contains four 64K byte memory modules (256K baud).
MJ11-AC (115 V), -AD (230 V)	MJ11 memory expansion cabinet.
Consists of the following:	
Wired Cabinet	Includes 861-D (115 V) or -E (230 V) power control.
One 256K byte (128K 16-bit word) Memory Frame	Same as MJ11-AG (AH).

Table 1-3 MJ11 Memory Options (Cont)

Item	Description
MJ11-BE	128K byte (64K 16-bit word) memory module used to increase the amount of memory in a memory frame.
Consists of two of each of the following:	
G116 SIN Module	Sense/Inhibit Module (slots 4 and 21, 7 and 18 or 10 and 15).
H224C STK Module	Stack module (slots 5 and 22, 8 and 19 or 11 and 16).
G236 DRV Module	Drive module (slots 6 and 23, 9 and 20, or 12 and 17).
MJ11-BA (115 V), -BB (230 V)	Memory expansion frame. Must be mounted in an MJ11 memory cabinet.
Consists of the following:	
Memory Frame	Slide mounted drawer, MJ11 etched backplane, two H744 +5 Vdc regulators, two H754 +20, -5 Vdc regulators, ac input box and MJ11 memory controller.
The memory controller consists of the following:	
M8147 MCT Module	Memory Control and Timing (slot 13)
M8149 MXR Module	Memory Transceiver Card (slot 14).
Two 64K byte (32K 16-bit word) memory module	Same as MJ11-BE.
MJ11-BG (115 V), -BH (230 V)	Memory expansion frame. Must be mounted in MJ11 memory cabinet. Same as MJ11-BA (BB), but contains four 128K byte memory modules (512K baud).
MJ11-BC (115 V), -BD (230 V)	MJ11 memory expansion cabinet.
Consists of the following:	
Wired Cabinet	Includes 861-D (115 V) or -E (230 V) Power Control.
One 512K byte (256K 16-bit word) memory frame	Same as MJ11-BG (BH).

NOTE: Maximum system memory size of eight full frames in two memory cabinets is: MJ11-A: 2048K byte (1024K 16-bit words); MJ11-B: 4056K byte (2048K 16-bit words).

Table 1-4 MK11 Memory Options

Item	Description
MK11-BA (115 V), -BB (230 V)	Memory expansion frame, box controller, and three battery backup units. Must be mounted in a memory cabinet.
Consists of the following:	
Memory Frame	Slide mounted draw, MK11 etched backplane, one H7441 +5 Vdc regulator, three 7014251 ± 12 V, +5 Vdc regulators, ac input box, and interface and control modules.
Interface and Control Modules	
M8158	Address Interface Module
M8159	Data Buffer Module
M8160	Control A Module (2)
M8161	Control B Module (2)
64K words MOS memory	Two MS11-KE Memory Array Modules
Box Controller	
Battery Backup Units (3)	
MK11-BC (115 V), -BD (230 V) Consists of the following:	Memory expansion cabinet.
Wired Cabinet	Includes 861-D, -E Power Control.
Memory Frame, Box Controller, 3 Battery Backup Units, and 64K words MOS memory	Same as MK11-BA or MK11-BB.
MK11-BE	64K word expansion. Consists of two MS11-KE Array Modules to be added to an existing memory frame.
MK11-BF	256K word expansion. Consists of eight MS11-KE Array Modules to be added to an existing memory frame.
MK11-BG (115 V), -BH (230 V)	Memory expansion frame, box controller, and three battery backup units. Must be mounted in a memory cabinet. Same as MK11-BA or MK11-BB except with 512K words MOS memory.

Table 1-4 MK11 Memory Options (Cont)

Item	Description
MK11-BY (115 V), -BZ (230 V)	Memory expansion frame without cables. Same as MK11-BA or MK11-BB except without cables, box controller, or battery backup units.
MS11-KE	32K word MOS memory array module (M7984EB, EC, ED, EE, etc.). Array consists of 156 4K bit MOS RAM chips.
MS11-KD	32K word MOS memory array module (M7984DB, DC, etc.). Array consists of 39 16K bit MOS RAM chips.
MS11-KC	128K word MOS memory array module (M7984CB, CC, CD, etc.). Array consists of 156 16K bit MOS RAM chips.

Table 1-5 Processor Cabinet Options

Option	Description
The 10-1/2 inch slot immediately above the CPU mounting box may contain only one of the following options:	
PC11	High Speed Paper Tape Reader-Punch
PR11	High Speed Paper Tape Reader
TU60	Dual Cassette Drive
LPS11	Lab Peripheral System
VR14	Point Plot Display
The 10-1/2 inch slot above the slot just described may contain only one of the following options:	
LPS11	Lab Peripheral System
TS03	Magtape Drive
RX01	Disk Drive (Floppy disk)
TU60	Dual Cassette Drive. One or two TU60s may be installed in this 10-1/2 inch slot.

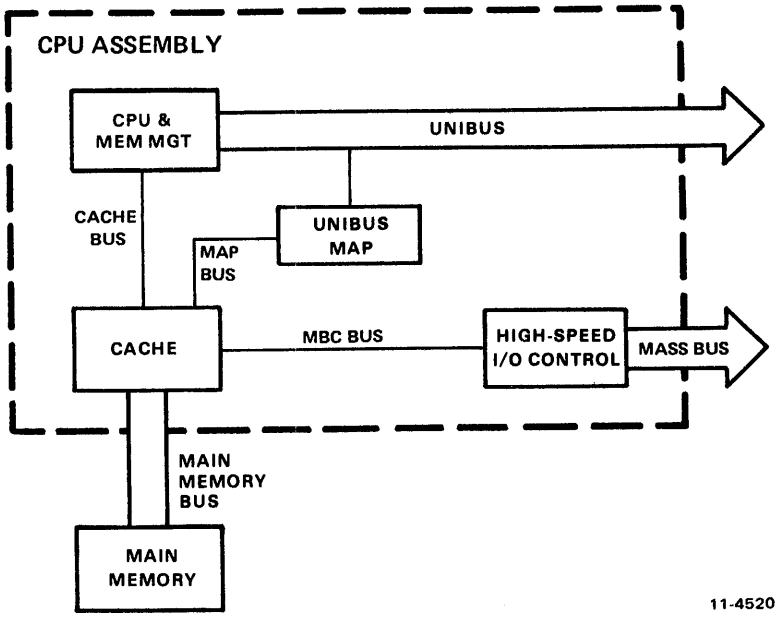
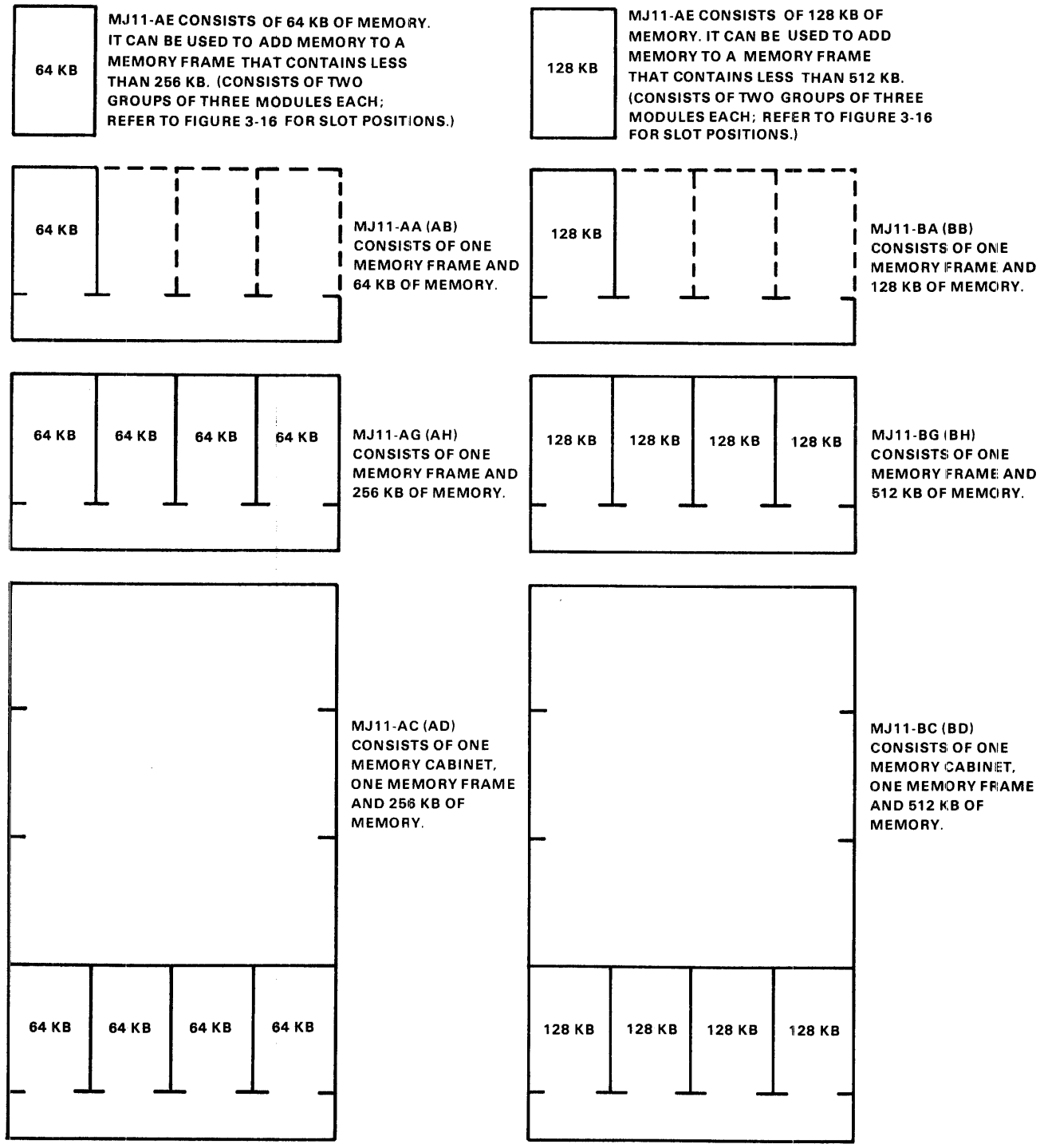


Figure 1-2 Block Diagram of PDP-11/70



NOTES:

1. A memory frame consists of one MJ11 drawer including a power supply, an etched backplane, a controller and from one to four 64 KB or 128 KB memory sets.
2. The minimum PDP-11/70 system includes one memory frame and 128 KB of memory.
3. See Table 1-3.

11-4521

Figure 1-3 MJ11 Memory Options

1.2 RELATED DOCUMENTATION

Table 1-6 lists the reference manuals for the minimum PDP-11/70 configuration and for the processor backplane options particular to the PDP-11/70.

Small Peripheral Controller (SPC) manuals other than the DL11, as well as manuals related to other peripheral options, are supplied with the equipment.

Table 1-6 Related Documentation

Title	Document Number
PDP-11/70 Manuals*	
KB11-B Processor Manual (PDP-11/70)	EK-KB11B-TM-001
MJ11 Memory System Maintenance Manual	EK-MJ11-MM-002
MK11 MOS Memory System Technical Manual	EK-MK11-TM-001
FP11-C Floating-Point Processor Maintenance Manual**	EK-FP11C-MM-PRE
FP11-B Floating-Point Processor Maintenance Manual**	EK-FP11-MM-003
LA36 DECwriter Maintenance Manual	EK-LA36-MM-001
DL11 Asynchronous Line Interface Manual	DEC-11-HDLAA-B-D
KW11-L Line Time Clock Manual	EK-KW11L-TM-002
861A-F Power Controller Maintenance Manual	EK-861AB-MM-002
RWS04/RWS05 Fixed Head Disk Subsystem Maintenance Manual**	EK-RWS04-MM-001
RWP04 Moving Head Disk Subsystem Maintenance Manual**	EK-RWP04-MM-001
TWU16 Magnetic Tape Subsystem Maintenance Manual**	EK-TWU16-MM-001
M9312 Bootstrap/Terminator Module Technical Reference Manual	EK-M9312-TM-001
M9301 Bootstrap/Terminator Module Maintenance and Operator's Manual	EK-M9301-TM-001
Reference Handbooks	
PDP-11/70 Processor Handbook	
PDP-11 Peripherals and Interfacing Handbook	

*A set of engineering drawings is provided with each of the components and options in the PDP-11 system.

**Optional

1.3 REFERENCE DRAWINGS

An Engineering Print Set, which includes all electrical schematics and mechanical assembly drawings related to a system, is supplied with each PDP-11/70.

1.3.1 DIGITAL Drawing Numbers

Figure 1-4 shows the numbering system used for DIGITAL drawings.

1.3.2 Drawing Conventions

Figure 1-5 illustrates some of the drawing conventions used on the PDP-11/70 circuit schematics.

In this figure, part A defines the meaning of each part of a typical signal mnemonic.

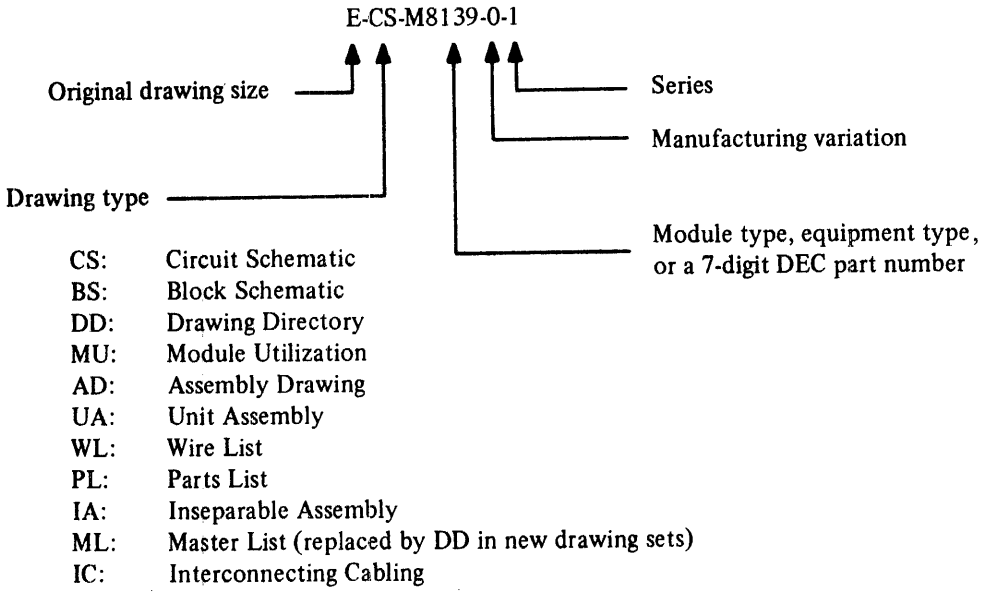


Figure 1-4 Drawing Nomenclature

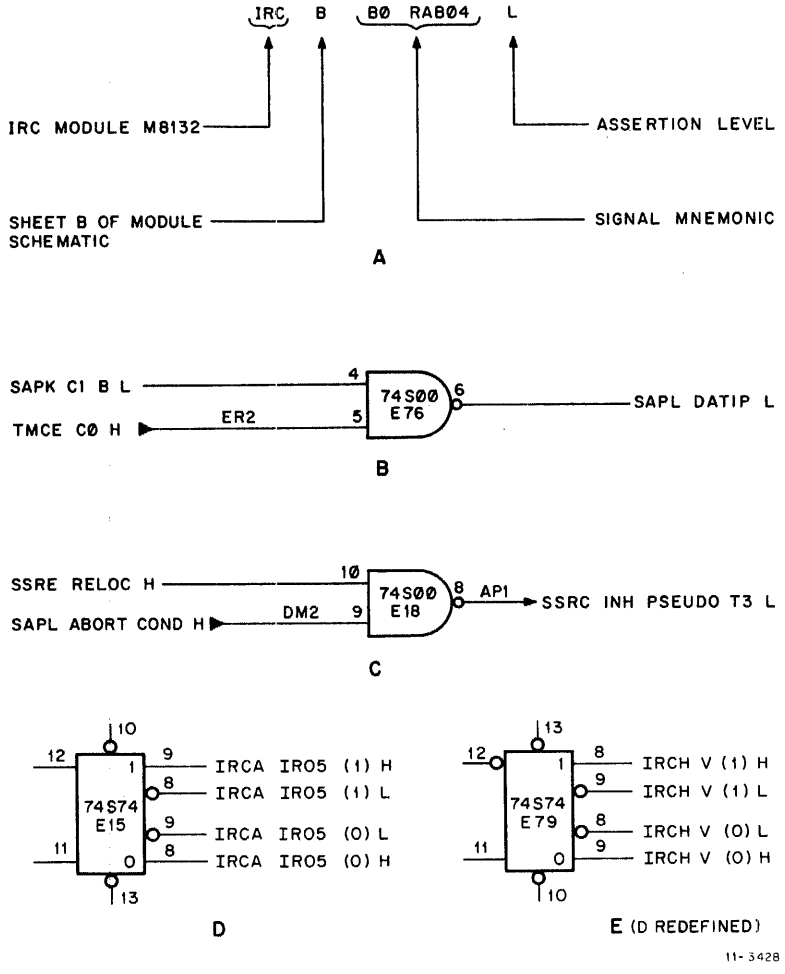


Figure 1-5 PDP-11/70 Drawing Convention Examples

Part B provides the following information:

1. SAPL DATIP L originates on the SAP (M8137) module and is shown on sheet L of the drawing. It is asserted when low (0 V); it is used only on SAP.

2. SAPK C1 B L also originates on the M8137 module, but is shown on sheet K of the schematic.

3. TMCE C0 H originates on the TMC (M8135) module, where it is shown on sheet E. It is input to the M8137 module at pin R2, row E (ER2).

4. The SAPL DATIP L NAND gate uses pins 4, 5, and 6 of the 74S00 IC at position E76 on the M8137 module.

Part C shows a function similar to that in part B. In this case, however, the output (SSRC INH PSEUDO T3 L) is brought out to pin P1, row A, of the module edge connector for use by another module.

Parts D and E show the flip-flop conventions. Note in D that IRCA IR05 (1) H is the same pin as IRCA IR05 (0) L, and that IRCA IR05 (1) L is the same pin as IRCA IR05 (0) H. The same type of flip-flop has been redefined in part E – the D input is inverted; the 1 and 0 outputs are interchanged as are the set and reset inputs.

1.3.3 Reference Drawings

Table 1-7 lists the schematic drawings for the minimum PDP-11/70 configuration and for the processor backplane options particular to the PDP-11/70.

Table 1-7 Reference Drawings

Title	Drawing Number
PDP-11/70 System Drawings	
Drawing Directory PDP-11/70	B-DD-11/70-0
Drawing Directory KB11-B	B-DD-KB11-B
Drawing Directory H7420	B-DD-H7420-0
Drawing Directory KW11-L	B-DD-KW11-L
Drawing Directory DL11-A	B-DD-DL11-A
Drawing Directory LA36	B-DD-LA36-0
Drawing Directory MJ11	B-DD-MJ11-0
Master Parts List KM11	A-ML-KM11-0
Terminator Bootstrap	D-CS-M9301-YC-1
Bus Terminator	D-CS-M9302-0-1
Terminator H873	D-CS-H873-0-1
Unit Assembly PDP-11/70	E-UA-11/70-0-0
Unit Assembly PDP-11/70 (PL)	A-PL-11/70-0-0
Power System Configuration	D-IC-11/70-0-2
Harness Power	J-IA-7011051-0-0
Wire List Power Harness	D-IC-7011051-0-1
I/O Cable BC06R	D-UA-BC06R-0-0
Accessory List PDP-11/70	A-AL-11/70-0-3
System Expansion PDP-11/70	E-AR-11/70-0-1

Table 1-7 Reference Drawings (Cont)

Title	Drawing Number
KB11-B, C Processor	
Drawing Directory KB11-B	B-DD-KB11-B
16-Bit Processor	A-PL-KB11-B-0
Flow Diagrams	D-FD-KB11-B-1
Block Diagram	D-BD-KB11-B-2
Block Diagram	D-BD-KB11-B-3
Unibus Cable and Grant Chain	D-IC-KB11-B-7
Data Paths	D-CS-M8130-0-1
Gen Reg and ALU. Controls	D-CS-M8131-0-1
IR Decode (KB11-C requires CS Rev. B or higher)	D-CS-M8132-0-1
Console Board	D-CS-5411294-0-1
Proc. Data and Unibus Control	C-CS-M8134-0-1
ROM and ROM Control*	D-CS-M8123-0-1
ROM and ROM Control**	D-CS-M8133-0-1
Timing Generator	D-CS-M8139-0-1
Traps and Misc. Control	D-CS-M8135-0-1
Unibus and Console Control	D-CS-M8136-0-1
Timing Diagram	D-TD-M8136-0-7
Flow Diagram	D-FD-M8136-0-8
Address Memory Board	D-CS-M8143-0-1
Cache Control Board	D-CS-M8142-0-1
Cache Data Paths	D-CS-M8145-0-1
Block Diagram	B-BD-M8145-0-7
Data Memory Board	D-CS-M8144-0-1
Memory Mgmt Block Diagram	D-BD-KB11-B-8
Memory Mgmt Registers	D-BD-KB11-B-4
Cache Address Timing	D-TD-KB11-B-10
Int. Reg. Cycle Timing	D-TD-KB11-B-9
Memory Mgmt Trap Timing	B-BD-KB11-B-5
System Address Paths	D-CS-M8137-0-1
System Descriptor and Console Cables**	D-CS-M8138-YA-0-1
System Descriptor and Console Cables*	D-CS-M8140-0-1
System Status Registers	D-CS-M8138-0-1
Unibus Map (M8141) B.D.	B-BD-KB11-B-6
Unibus Map	D-CS-M8141-0-1
Processor Backplane	E-AD-7010329-0-0
Awt Rev Status	A-WT-7010329-0
H7420 Power Supply	
Drawing Directory	B-DD-H7420-0
Wiring Diagram	D-CS-H7420-0-1
Power Line Monitor	D-CS-5411086-0-1
H7420 Power Supply	E-UA-H7420-0-0
H7420 Power Supply (P.L.)	A-PL-H7420-0-0

*KB11-C Processor
**KB11-B Processor

Table 1-7 Reference Drawings (Cont)

Title	Drawing Number
KW11-L Line Frequency Clock	
Timing Diagram	D-TD-KW11-L-02
Line Frequency Clock	D-BS-KW11-L-01
Line Clock	D-CS-M787-0-1
Line Frequency Clock	A-PL-KW11-L-0
Software List	A-SL-KW11-L-28
DL11-A Asynchronous Line Interface	
Drawing Directory	B-DD-DL11-0
Asynchronous Line Interface	C-UA-DL11-0-0
Asynchronous Line Interface (PL)	A-PL-DL11-0-0
Asynchronous Line Interface	E-CS-M7800-YA-11
Cable Assembly (KL8/E)	D-IA-7008360-0-0
Software List	A-SL-DL11-0-4
Accessory List	A-AL-DL11-0-5
Installation Procedure	A-S-DL11-0-2
LA36 DECwriter	
LA36 Option Arrangement	D-AR-LA36-0-1
LA36 Power Schematic	D-CS-LA36-0-5
Logic Board (LA36)	D-CS-M7722-0-1
LA36 Power Board	D-CS-5410805-0-1
MJ11 Memory System	
Drawing Directory MJ11-A	B-DD-MJ11-A
Unit Assembly MJ11-A	E-UA-MJ11-A-0
Power Supply (MJ11)	B-DD-7010694-0
Parts List MJ11-A	A-PL-MJ11-A
Block Diagram (MJ11) (M8148)	B-BD-MJ11-A-BD
Timing Diagram Read/Write	D-TD-MJ11-A-TD
Memory Control and Timing Module	D-CS-M8148-0-1
Memory Transceiver Card	D-CS-M8149-0-1
16K Sense Inhibit Board	D-CS-G114-0-1
16K × 18 Bit Stack	D-CS-H217-C-1
16K Memory Drive Board	D-CS-G235-0-1
Circuit Schematic Memory	D-CS-5411553-0-1
Circuit Schematic (MEM-EL-FAB)	D-CS-5411581-0-1
Circuit Schematic (MEM-EL-FAB)	D-CS-5411583-0-1
Power Harness	D-IA-7010580-0-0
Wire Harness ac/dc Low	D-IA-7010581-0-0
Power Control 861-D	B-DD-861-D
Power Control 861-E	B-DD-861-E
Exp. Data Cable Assembly	D-AD-7010824-0-0
Exp. Cable Assembly (Inter Bay)	D-AD-7010826-0-0

Table 1-7 Reference Drawings (Cont)

Title	Drawing Number
MJ11 Memory System (Cont)	
Cable Detail	D-IA-7010974-0-0
Packaging Instruction (Customer Ship)	A-SP-3700195-0-0
Packaging Instruction (Interplant)	A-SP-3700194-0-0
Memory Control and Timing Module	D-CS-M8147-0-1
32K Sense Inhibit Board	D-CS-G116-0-1
32K × 18 Bit Stack	D-CS-H224-0-1
32K Memory Drive Board	D-CS-G236-0-1
MK11 Memory System	
Drawing Directory MK11	B-DD-MK11-B
Unit Assembly MK11	E-UA-MK11-B-O
Parts List MK11	A-PL-MK11-B-O
11/70 System Expansion (MK11)	E-AR-11/70-0-5
Backplane MK11 Memory	E-AD-7014226-0
MK11 Block Diagram	D-BD-MK11-0-3
MK11 Timing Diagrams	D-TD-MK11-0-4
Power Control 861	B-DD-861-D
Power Supply H765	B-DD-H765-0
Battery Backup Regulator	B-DD-7014251-0
Power Supply Regulator	D-CS-5411086-0-1
MK11 Address Interface	D-CS-M8158-0-1
	D-UA-M8158-0-0
	B-PL-M8158-0-0
MK11 Data Buffer	D-CS-M8159-0-1
	D-UA-M8159-0-0
	B-PL-M8159-0-0
MK11 Control A	D-CS-M8160-0-1
	D-UA-M8160-0-0
	B-PL-M8160-0-0
MK11 Control B	D-CS-M8161-0-1
	D-UA-M8161-0-0
	B-PL-M8161-0-0
MK11 Box Controller	D-CS-5413018-0-1
	B-UA-5413018-0-0
	B-PL-5413018-0-0
M775 Battery Backup Unit	MP00014
H7441 +5 V Regulator	MP00271
MS11-K MOS Storage Array	MP00325

Table 1-7 Reference Drawings (Cont)

Title	Drawing Number
FP11-C Floating Point Processor (Optional)	
Drawing Directory	B-DD-FP11-C-0
Flow Diagrams	D-FD-FP11-C-
M8126 FRH Module Schematic	D-CS-M8126-0-1
M8127 FRL Module Schematic	D-CS-M8127-0-1
M8128 FRM Module Schematic	D-CS-M8128-0-1
M8129 FXP Module Schematic	D-CS-M8129-0-1
FP11-B Floating Point Processor (Optional)	
Drawing Directory	B-DD-FP11-B-0
M8112 FRM Module Schematic	E-CS-M8112-0-1
M8113 FXP Module Schematic	E-CS-M8113-0-1
M8114 FRH Module Schematic	E-CS-M8114-0-1
M8115 FRL Module Schematic	E-CS-M8115-0-1
FP Data Paths (Flows)	D-FD-FP11-B-
RH70 Controllers (Optional)	
Drawing Directory RH70	B-DD-RH70-0
Massbus Controller	D-UA-RH70-0-0
Massbus Data Path	D-CS-M8150-0-1
Control and Status	D-CS-M8151-0-1
Addr. and Word Count Regs.	D-CS-M8152-0-1
Unibus Control	D-CS-M8153-0-1
Massbus Transceiver	D-BS-RH70-0-1
Unibus Cable and Grant Chain	D-IC-KB11-B-7
RH70 Data Buffer Timing Diag.	D-TD-RH70-0-5
Write Massbus Timing Diag.	D-TD-RH70-0-6
Massbus Timing Diag.	D-TD-RH70-0-7
Write Command Flow Diag.	D-FD-RH70-0-2
Write Check Command Flow Diag.	D-FD-RH70-0-3
Read Command FLow Diag.	D-FD-RH70-0-4
Controller Transceiver	D-CS-M5904-0-1
Massbus Terminator	D-CS-H870-0-1

CHAPTER 2
SPECIFICATIONS

This chapter lists the power, mechanical, and environmental specifications of the basic components of the PDP-11/70 system, as well as those of the Massbus devices.

2.1 PROCESSOR AND MEMORY

2.1.1 Electrical

2.1.1.1 Power Requirements – The basic 120 V PDP-11/70 requires 90–132 Vac (phase to neutral), 47 to 63 Hz, 3-phase wye at 30 A/phase for each cabinet.

The basic 240 V PDP-11/70 requires 180–264 Vac (phase to neutral), 312–457 Vac (phase to phase), 47 to 63 Hz, 3-phase wye at 15 A/phase for each cabinet.

2.1.1.2 Power and Heat Dissipation – A PDP-11/70 with FP11, four high-speed I/O Controllers, five small peripheral controllers, and 128K baud of memory consumes approximately 3000 W and dissipates approximately 10,000 Btu/hr. Refer to Paragraph 4.3.2.

The same PDP-11/70 with a full interleaved MJ11 memory cabinet (1024K baud) consumes approximately 5000 W and dissipates approximately 18,000 Btu/hr.

An additional 1024K bytes of MJ11 memory would add approximately 2800 W and 8200 Btu/hr to these figures.

Each fully populated MK11 memory consumes approximately 500 W of power and dissipates approximately 1700 Btu/hr.

Power Surge	Processor cabinet (phases 1 and 2), 200 A/phase, 10 ms max.
	Each MJ11 frame adds 160 A/phase/10 ms max.

NOTE

The preceding figures can be considered worst case, although actual current demand is a function of activity and of variations in individual components.

The FP11-B and -C require 200 W max and dissipate 500 Btu/hr.

Each RH70 controller consumes 200 W and dissipates 700 Btu/hr.

Power requirements for small peripheral controllers are listed in Appendix F.

Detailed specifications for the 861-D, E Power Control are listed in Chapter 4 of this manual.

2.1.2 Mechanical Characteristics

The overall dimensions of the cabinets supplied with the PDP-11/70 are:

Height	181.3 cm (71-7/16 in)
Width	108 cm (43-3/8 in)
Depth	76 cm (30 in) With cabinet feet: 99 cm (39 in)
Weight without shipping pallets	
	CPU cabinet: 227 kg (500 lb) Memory cabinet with 64K bytes: 163 kg (360 lb) Memory frame with 64K bytes: 57 kg (125 lb)
Shipping pallets	Single cabinet: 17 kg (38 lb) Double cabinet: 29 kg (65 lb)

2.1.3 Environmental Specifications

Operating Environment Range

Temperature	10° C to 40° C (50° to 104° F)
Relative Humidity	10% to 90% with max wet bulb 28° C (82° F) and minimum dew point 2° C (36° F)
Altitude	To 2.4 km (8000 ft)

Non-Operating Environment Range

Temperature	-40° C to 66° C (-40° F to 151° F)
Relative Humidity	To 95%
Altitude	To 9.1 km (30,000 ft)

Recommended Operating Environment

Temperature	18.5°-23.8° C (65°-75° F)
Relative Humidity	40-60%

Peripheral media may restrict the ranges just described. Refer to Paragraph 2.2 and to Appendix F.

2.2 RH70 PERIPHERAL DEVICES

2.2.1 TU16 Magtape Drive

Electrical

Voltage and current (single phase)

94-126 V, 60 Hz ±2%, 8 A (9 A with TM02)
207-253 V, 50 Hz ±2%, 4 A (4.5 A with TM02)
Surge Current (max): 85 A at 94-126 V

Power Consumption and Heat Dissipation

1000 W, 3400 Btu/hr (1100 W, 3700 Btu/hr with TM02)

Mechanical

Weight	228 kg (500 lb) with cabinet
Size	181.3 cm h × 54 cm w × 76 cm d (72-7/16 in h × 21-11/16 in w × 30 in d)

Environmental

Operating Temperature	15° C to 35° C (60° F to 95° F)
Relative Humidity	20 to 80% (no condensation)

(Magnetic tape operation is more reliable if the temperature is limited to 18° C to 24° C (65° F to 75° F) and the relative humidity 40% to 60%.)

2.2.2 RP04 Disk Pack Drive

Electrical

Voltage and Current	
60 Hz ±1%	3-phase wye at 208 Vac ±10% Starting Current: 30 A/phase, 10 ms max Running Current: 8.2 A/phase at 208 Vac
50 Hz ±1%	3-phase wye at 380/408/420 Vac ±10% Starting Current: 16 A/phase, 10 ms max Running Current: 4.3 A/phase at 408 Vac
Power Consumption	2100 W
Heat Dissipation	7000 Btu/hr
Power Factor	0.7

Mechanical

Weight	270 kg (600 lb)
Size	102 cm h × 79 cm w × 81 cm d (40 in h × 31 in w × 32 in d)

Environmental

Operating Temperature	15° C to 32° C (60° F to 90° F)
Relative Humidity	20% to 80%, maximum wet bulb 25° C and minimum dew point 2° C

2.2.3 RS03 and RS04 Disk Drives

Electrical

Voltage and Current (single phase)	90–132 V, 60 ±1 Hz or 50 ±1 Hz, 6 A 180–264 V, 60 ±1 Hz or 50 ±1 Hz, 3 A
Surge Current	13 A at 90–132 V 6 A at 180–264 V
Power Consumption	700 W
Heat Dissipation	2400 Btu/hr

Mechanical (Drive Only)

Weight	RS04: 54.4 kg (120 lb) RS03: 50 kg (110 lb)
Size	400 mm h × 482.6 mm w × 665 mm d (15-3/4 in h × 19 in w × 26-1/4 in d
With Cabinet	
Weight	159 kg (350 lb)
Size	181.3 cm h × 54 cm w × 76 cm d (71-7/16 in h × 21-11/16 in w × 30 in d)

Environmental

Operating Temperature	10° C to 22° C (50° F to 104° F)
Relative Humidity	10% to 90% Max wet bulb: 22° C (82° F) Min dew point: 2° C (36° F)

2.3 UNIBUS INTERFACE

Specifications for the Unibus devices available to the PDP-11/70 are listed in Appendix F.

CHAPTER 3
SYSTEM INSTALLATION

3.1 GENERAL

This chapter contains installation information and recommendations to ensure a successful PDP-11/70 installation. Installation of new options in an existing PDP-11/70 system is also described in this chapter.

Customer assistance is provided during site planning, preparation, and installation; the final layout plan should be approved by both the customer and DIGITAL prior to delivery of the equipment.

Planning considerations should include:

- Shipping and access routines, e.g., door, hall, passageway, elevator restrictions, etc.
- Floor plan layout for equipment
- Electrical and environmental considerations
- Fire and safety precautions
- Storage facilities for accessories and supplies.

Site preparation is dictated by the customer's requirements and can range from providing the required source power to complete construction or remodeling of the selected installation site. Therefore, it is recommended that any and all requirements and restrictions be considered and effected prior to shipment and installation of the equipment.

3.2 SITE PREPARATION

Adequate site planning and preparation simplifies the installation process. DIGITAL Sales and Field Service Engineers are available for consultation and planning with customer representatives regarding objectives, course of action, and progress of the installation. The information in this paragraph is provided primarily to permit review of the site planning; use the site configuration worksheet to perform the initial site planning.

For more detailed information, refer to the *XXX Site Preparation and Planning Guide* (where "XXX" stands for a Product Line, e.g., TELCO, IPG, DECCOM).

3.2.1 Physical Dimensions

The overall dimensions and total weight of a particular system – the dimensions, weight of any optional cabinets, cable lengths, and the number of free-standing peripherals – should be known prior to shipment.

The route the equipment is to travel from the customer receiving area to the installation site should be studied; measurements of doors, passageways, etc., should be taken to facilitate delivery of the equipment. All measurements and floor plans should be submitted to the DIGITAL Sales Engineer and Field Service to ensure that the equipment is packed to suit the installation site facilities. Any restrictions (such as bends or obstructions in hallways, etc.) should be reported to DIGITAL.

If an elevator is to be used to transfer the PDP-11/70 and its related equipments to the installation site, DIGITAL should be notified of the size and gross weight limitations of the elevator so that the equipment can be shipped accordingly.

The site space requirements are determined by the specific system configuration to be installed and, when applicable, provisions should be made for future expansion. To determine the exact area required for a specific configuration, a machine-room floor plan layout is helpful. When applicable, space should be provided in the machine room for storing tape reels, printer forms, card files, etc. The integration of the work area with the storage area should be considered in relation to the work flow requirements between areas.

In large installations where test equipment is maintained, DIGITAL recommends that the test equipment storage area be within or adjacent to the machine room.

Operational requirements determine the specific location of the various options and free-standing peripherals of the system. Dimensions, weights, and cable lengths of free-standing peripheral equipment must be known prior to installation – preferably during site preparation and planning. The computer peripherals must not be located at distances where connecting cables exceed maximum limits. The following points should be considered when planning the system layout:

1. Ease of visual observation of input/output devices by operating personnel

2. Adequate work area for installing tapes, access to console, etc.

3. Space availability for contemplated future expansion

4. Proximity of the cabinets and peripherals to any humidity-controlling or air-conditioning equipment

5. Adequate access to equipment (e.g., rear door, etc.) for service personnel.

The final layout will be reviewed by the DIGITAL Sales Engineer, Field Service, and in-house engineering personnel to ensure that cable limitations have not been exceeded and that proper clearances have been maintained.

3.2.2 Fire and Safety Precautions

The following fire and safety precautions are presented to aid the customer in maintaining an installation that affords adequate operational safeguards for personnel and system components.

1. If an overhead sprinkler system is used, a dry pipe system is recommended. Upon detection of a fire, this system removes source power to the room and then opens a master valve to fill the room's overhead sprinklers.

2. If the fire detection system is the type that shuts the power to the installation off, a battery-operated emergency light source should be provided.

3. If an automatic carbon dioxide fire protection system is used, an alarm should sound prior to release of the CO_2 to warn personnel in the installation area.

4. If power connections are made beneath the floor of a raised floor installation, waterproof electrical receptacles and connections should be used.

5. An adequate earth ground connection should be provided to protect operating personnel.

3.2.3 Environmental Requirements

An ideal computer room environment has an air distribution system that provides cool, well-filtered, humidified air. The room air pressure should be kept higher than that of adjacent areas to prevent dust infiltration.

3.2.3.1 Humidity and Temperature – The PDP-11/70 specifications, as well as those of the peripheral devices that may be associated with it, are listed in Chapter 2 and in Appendix F.

3.2.3.2 Air-Conditioning – When used, computer room air-conditioning equipment should conform to the requirements of the "Standard for the Installation of Air-Conditioning and Ventilating Systems (non-residential)", N.F.P.A. No. 90A, as well as the requirements of the Standard for Electronic Computer Systems, N.F.P.A. No. 75.

3.2.3.3 Acoustical Damping – Some peripheral devices (such as line printers and magnetic tape transports) are quite noisy. In installations that use a group of high noise level devices, an acoustically damped ceiling will reduce the noise.

3.2.3.4 Lighting – If CRT peripheral devices (e.g., VT05, VT50) are part of the system, the illumination surrounding these peripherals should be reduced to enable the operator to observe the display conveniently.

3.2.3.5 Special Mounting Conditions – If the system will be subjected to rolling, pitching, or vibration of the mounting surface (e.g., aboard ship), the cabinetry should be securely anchored to the installation floor by mounting bolts. Such installations require modifications to the cabinet: arrangements for modifications of this type should be made through DIGITAL's Computer Special Systems Group.

3.2.3.6 Static Electricity – Static electricity can be an annoyance to operating personnel and may affect the operational characteristics of the PDP-11/70 and related peripheral equipments. If carpeting is installed on the computer floor, it should be of a type designed to minimize the effects of static electricity. Flooring consisting of metal panels, or flooring with metal edges should be adequately grounded.

3.2.4 Electrical Requirements

The PDP-11/70 operates from a nominal 3-phase 115 V, 50/60 Hz or 3-phase 230 V, 50/60 Hz, ac power source. The primary ac operational voltages should be maintained within the tolerances defined in Chapters 2 and 4.

For certain options that use synchronous motors, line voltage tolerance should be maintained within ±15 percent of the nominal values, and the 50/60 Hz line frequency should not vary more than ±2 Hz.

Primary power to the system should be provided on a line separate from lighting, air-conditioning, etc., so that computer operation will not be affected by voltage transients. The wiring should conform to the following general guidelines:

1. All electrical wiring must conform with the National Electric Code (NEC).

2. The ground terminal on the receptacle is normally a green screw; the neutral terminals are white or silver; and the "hot" terminals are brass-colored.

3. Under the NEC (in the U.S. only), the color coding for the neutral wire is either white or gray, and the ground wire is solid green, green with one or more yellow stripes, or bare. There are no specified colors for the "hot" wires.

The PDP-11/70 cabinet grounding point should be connected to the building power transformer ground or the building ground point. Direct any questions regarding power requirements and installation wiring to the local DIGITAL Sales Engineer and/or Field Service.

Chapter 4 contains a detailed description of the Power System and includes a list of connectors and plugs used.

3.2.5 Related Documents

The following documents contain information that may be of value during site preparation and planning operations:

1. Plant Engineering Handbook, by William Staniar (McGraw Hill)
2. National Electrical Code (NFPA 70)*
3. Protection of Electronic Computer/Data Processing Equipment (NFPA 75)*
4. Installation of Air-Conditioning and Ventilation Systems (non-residential) (NFPA 90A)*
5. Recommended Good Practice for the Maintenance and Use of Portable Fire Extinguishers (NFPA 10A)*
6. Installation of Portable Fire Extinguishers (NFPA 10)*
7. Lightning Protection Code (NFPA 78)*
8. ASHRAE Handbook, (American Society of Heating, Refrigeration, and Air-Conditioning Engineers)
9. Computer Talk, Vol. 1, No. 1, 3M Company
10. Computer Decisions, Vol. 2, No. 10
11. ANSI Standard X3.11 (1969)
12. ISO Recommendation R1681 (1970)
13. U.L. Handbook No. 478, Underwriters Laboratories, Inc.
14. NBFU No 70, National Board of Fire Underwriters
15. EIA Standard RS-232C, Electronics Industries Association
16. Digital Supplies Catalog, Digital Equipment Corporation
17. IEEE Standard 142-1972.

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*NFPA Standards and publications are available from the National Fire Protection Association, 60 Batterymarch Street, Boston, Massachusetts 02110.

3.3 INSTALLATION

The installation procedure for a PDP-11/70 is essentially the same as that for all other PDP-11s. This installation procedure is described in the PDP-11 Family Field Installation and Acceptance Procedure. EK-FS003-IN, which should be followed and initiated as shown as the various steps are performed.

This paragraph summarizes the PDP-11 Faily Field Installation and Acceptance Procedure; procedures and details that pertain especially to the PDP-11/70 are inserted.

The PDP-11 Family Field Installation and Acceptance Procedure should be used in conjunction with the Installation Checklist, a computer printout in three parts:

1. Stand alone diagnostics to be run
2. DEC/X11
3. System Software Exerciser (under development)

3.3.1 Chapter 2 of the PDP-11 Family Field Installation and Acceptance Procedure

WARNING

Do not unskid the equipment until the procedures outlined in this paragraph (3.3.1) have been completed.

Do not plug in the ac power until told to do so in Paragraph 3.3.3.3.

Check the shipment for damage and inventory as described in EK-FS003-IN.

Figures 3-1 through 3-4 show the shipping retainers used in the PDP-11/70 processor and memory cabinets:

1. Figure 3-1 shows the tie wrap that secures the front door of the memory cabinet.

2. Figure 3-2 is a front view of the memory cabinet and shows the shipping bracket that secures each memory frame during shipment.

3. Figure 3-3 shows the rear of the processor cabinet and the shipping bracket that must be removed before pulling out the CPU drawer.

The tie wrap mentioned in step 1 and the two brackets shown in Figures 3-2 and 3-3 are the only items that are added to the basic PDP-11/70 for shipping. Figure 3-4 shows the lower portion of the memory cabinet as it is shipped.

Document any damage and call it to the attention of the customer. If the damage is extensive, report it to the Branch Service Manager or Supervisor immediately. DIGITAL is not responsible for shipping damage on systems that are F.O.B. from the manufacturing facility.

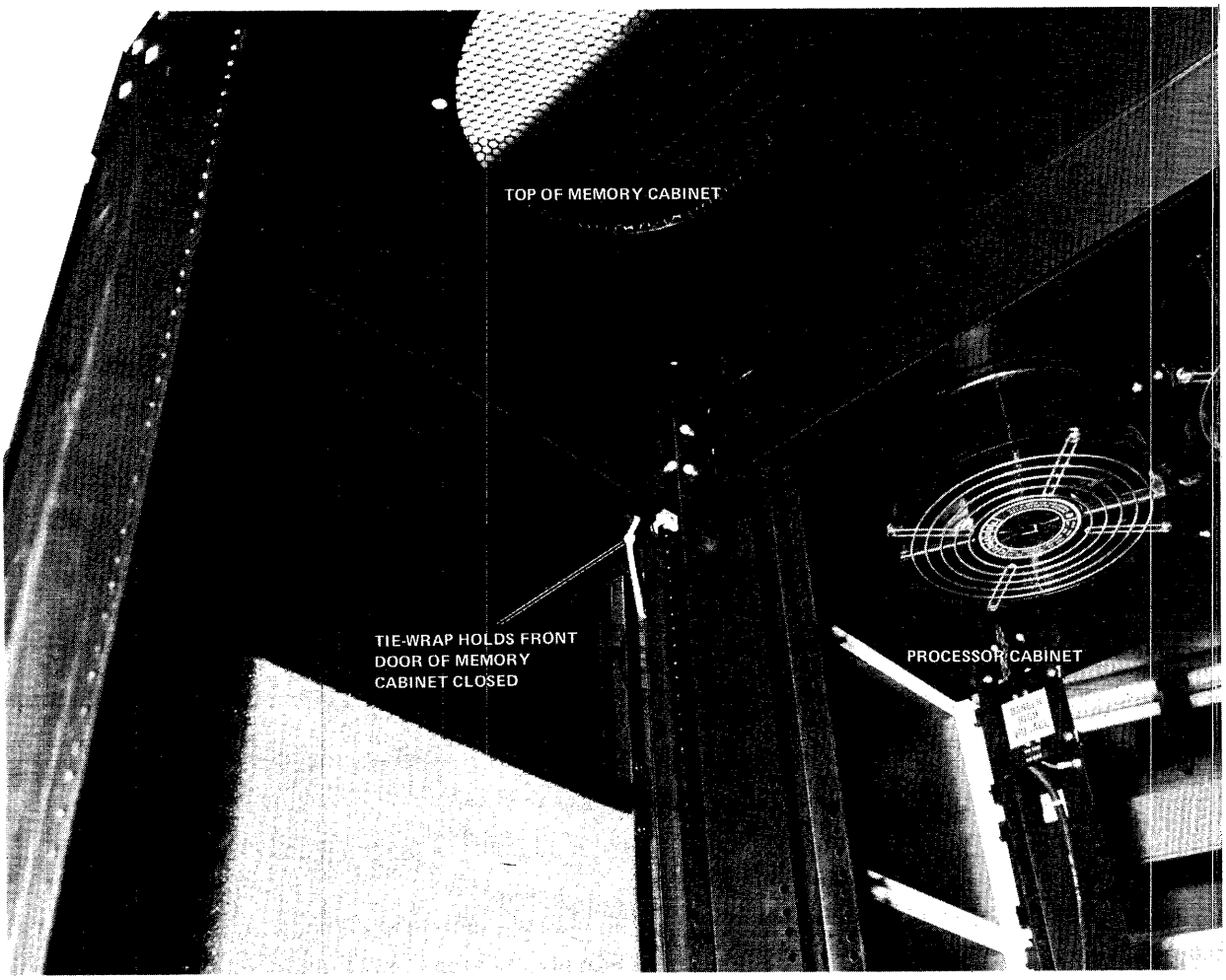
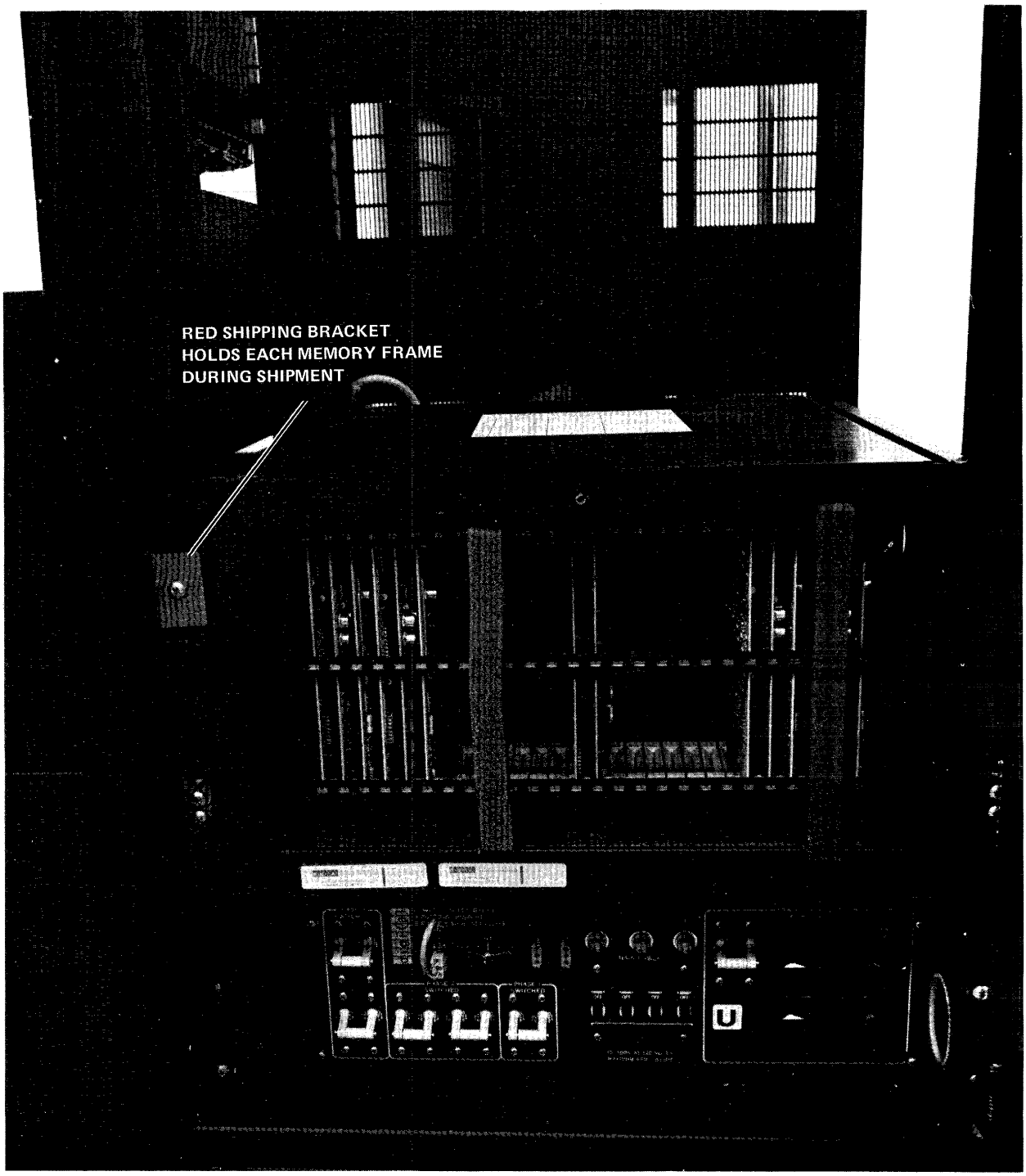


Figure 3-1 View of Inside Top of Memory Cabinet as Shipped



7554 1BW-A-0163

Figure 3-2 Front View of Memory Cabinet as Shipped

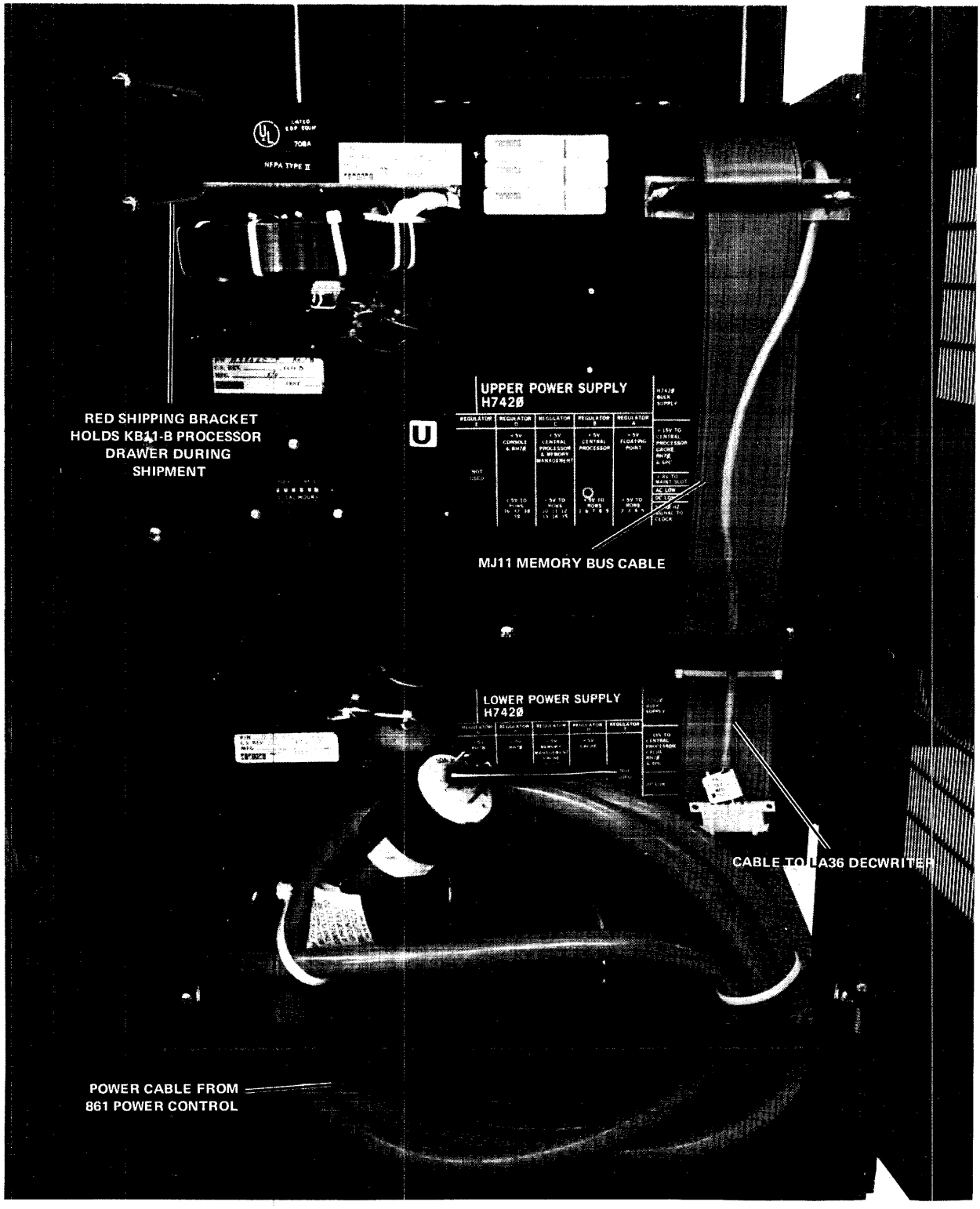
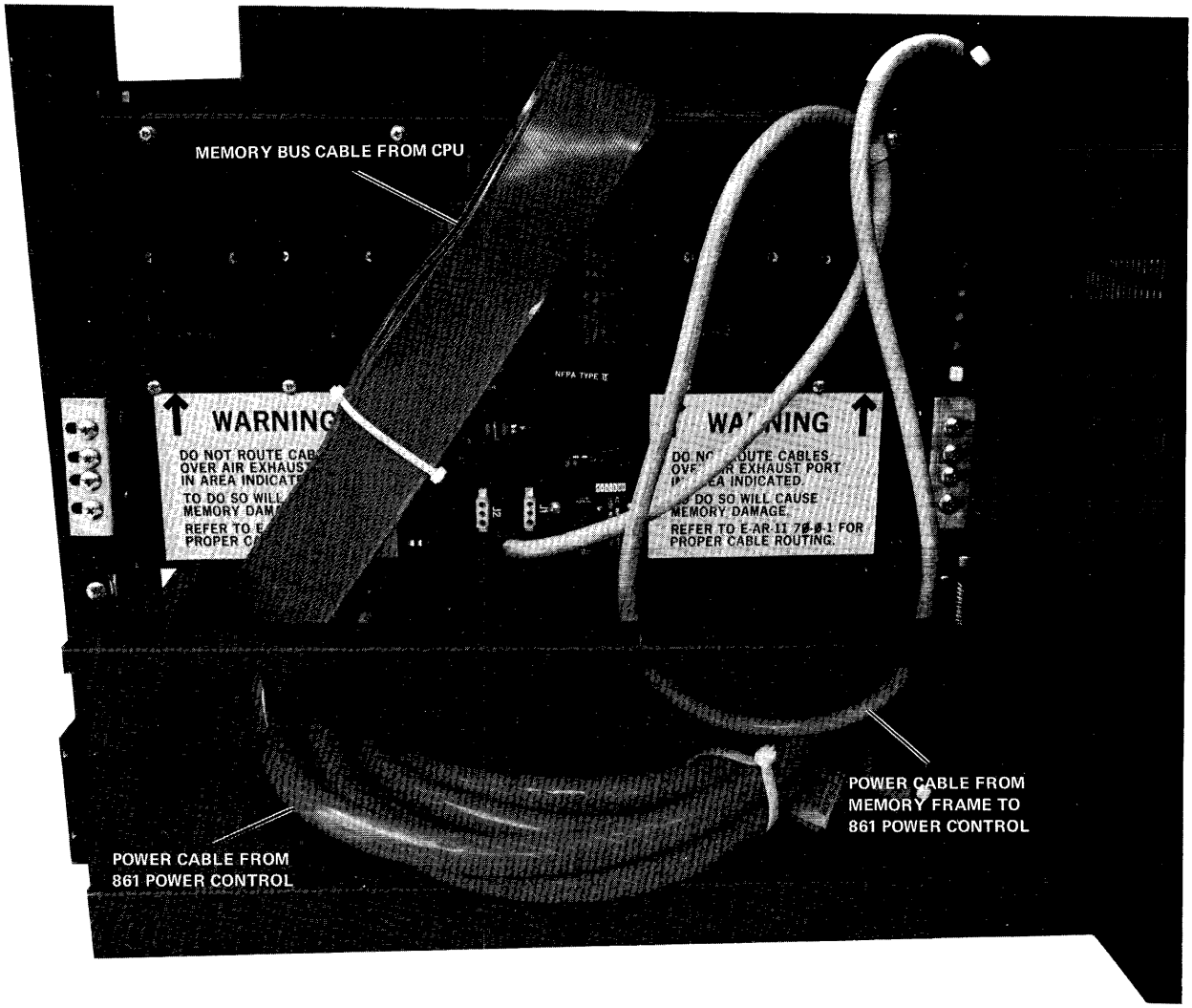


Figure 3-3 Rear View of Processor Cabinet as Shipped



7554-6-BW-A0164

Figure 3-4 Rear View of Memory Cabinet as Shipped

3.3.2 Chapter 3 of the PDP-11 Family Field Installation and Acceptance Procedure

Move the equipment to the installation site and remove the cabinets from the skids. Insert filler strips and bolt the cabinets together.

Lower the leveling feet so the cabinets are not resting on the roll-around casters. Ensure that all leveling feet are planted firmly on the floor and the system is kept level.

WARNING

System cabinets with heavy drawers fully extended are unstable when feet are not lowered.

Memory frames (drawers) must not be pulled out until the memory cabinet(s) are bolted to another cabinet.

Connect all ground straps; ensure that all ground connections are metal to metal, i.e., scrape off all paint at ground connection points. Lay out the I/O cables, but do not connect at this time. Check the physical layout with the configuration sheet.

3.3.3 Chapter 4 of the PDP-11 Family Field Installation and Acceptance Procedure

3.3.3.1 Grounding – Connect the system to the independent earth ground provided by the customer.

3.3.3.2 AC Power Supply Checks – Check the customer's ac power for proper voltage and phasing. Check that the power receptacles are wired correctly, and that ac ground is connected to all ground pins in all power receptacles for this system.

WARNING

It is very important that safety ground be maintained throughout the system to minimize the possibility of injury to personnel and damage to equipment.

Check the Customer's ac power as follows:

1. Refer to Figure 3-5, which shows the ac power receptacle required for the PDP-11/70. Measure the voltage between each of the three phases and neutral at the receptacle. The voltage should be between the limits defined in Chapter 2.

2. Approximately the same voltage should be read between each phase and the earth ground terminal.

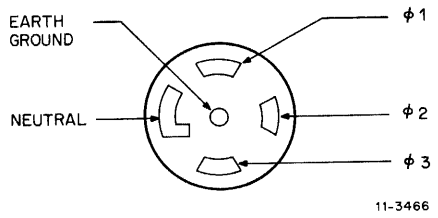


Figure 3-5 NEMA L21-30R Receptacle

In order to balance the three phases in the PDP-11/70, the phase rotation must be identical in all connectors used for the processor and memory cabinets (Figure 3-6).

1. Check the voltage between Phase 1 on one connector and the corresponding Phase 1 on another connector. Voltage reading should be 0 V.

2. Repeat step 1 for Phases 2 and 3.

3. If the voltage reading is not 0 V, one of the connectors is miswired. The customer must have the wiring corrected before plugging in the PDP-11/70.

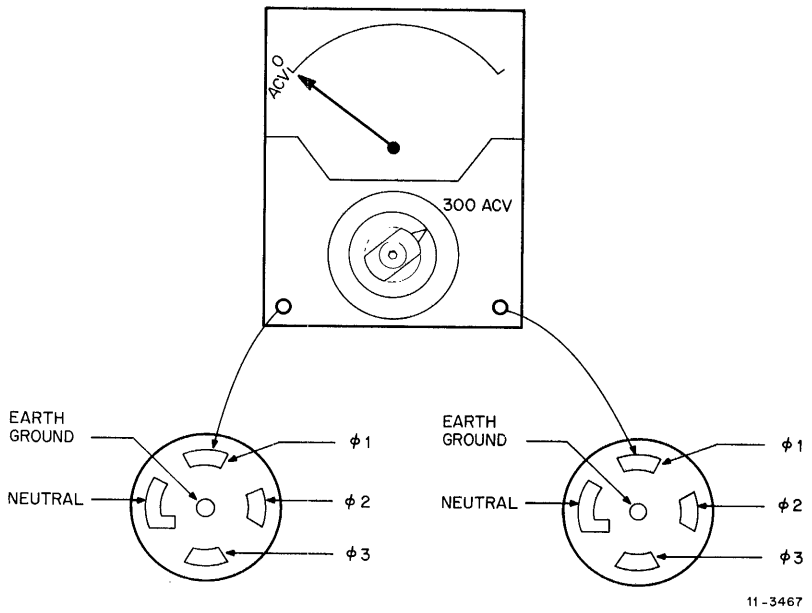


Figure 3-6 AC Phase Rotation

3.3.3.3 Equipment Power Checks

NOTE
The PDP-11/70 power system is described in Chapter 4 of this Manual.

Check all ac, dc, and signal cables.

Visually inspect all modules for any hardware that may be lodged between them. Vibrate all the modules to help dislodge any loose hardware or solder splashes.

Disconnect all Unibus cables that interconnect the system cabinets.

TURN OFF all the circuit breakers on all 861 power controls. Ensure that all fixed head disk motors are switched off at the unit (i.e., RS03, RS04) (Figure 3-7).

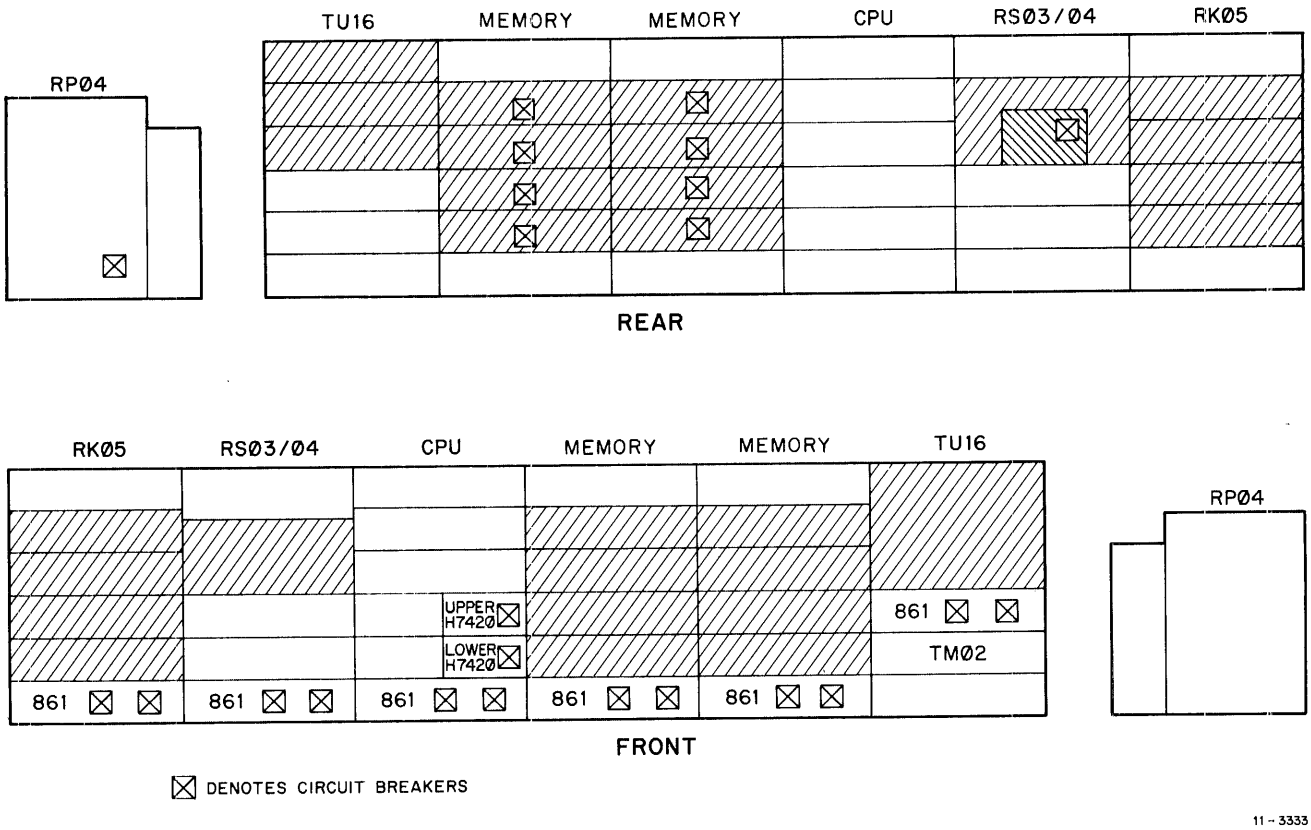


Figure 3-7 PDP-11/70 Circuit Breaker Location

Plug all the system 861 ac line cords into the customer receptacles. Put the LOCAL/REMOTE switch on all 861s to the LOCAL position.

NOTE

861-E power controls are shipped without a power cord.

3.3.3.4 System Cabinet Checks – Starting with the CPU cabinet, do the following for each cabinet in the system:

1. Turn ON the main ac circuit breaker on the 861 power control. Also turn on the console key in the case of the CPU cabinet.

2. Check for correct ac voltage output from all the 861 ac outlets: the meter reading between points P and N on Figure 3-8 should be 95 to 132 Vac on a 120 V system, and 180–264 Vac on a 240 Vac system; the reading between terminals P and G should be the same as those between P and N.

3. Check all fans.

4. Check all dc voltage levels and ripple with the proper test equipment and adjust to specification. Table 3-1 lists the voltage test points for the CPU and Table 3-2 lists those for the MJ11. Table 3-3 lists the voltage test points for the MK11. Test points for peripheral equipment are listed in their respective manuals.

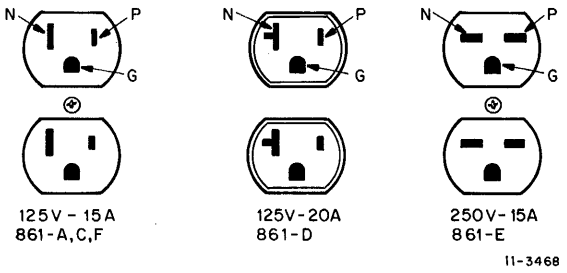


Figure 3-8 861 Power Control Outlets

Table 3-1 H7420 Voltage Measurements*

Output	Slots Supplied	Measure at CPU Backplane pin	Voltage	Max Ripple Peak-to-Peak V
H744 +5 V Regulator A	2–5	F02A2	+5 V	0.2 Vdc
H744 +5 V Regulator B	1, 6–9	F09A2	+5 V	0.2 Vdc
H744 +5 V Regulator C	10–15	F15A2	+5 V	0.2 Vdc
H744 +5 V Regulator D	36–44	F44A2	+5 V	0.2 Vdc
H744 +5 V Regulator H	20–22	F22A2	+5 V	0.2 Vdc
H744 +5 V Regulator J	16–18	F18A2	+5 V	0.2 Vdc
H744 +5 V Regulator K	24–28	F28A2	+15 V	0.2 Vdc
H744 +5 V Regulator L	29–35	F35A2	+5 V	0.2 Vdc
Upper H7420 5411086	1	B01B1	+8 V 61.2 Vdc	0.24 Vdc
Upper H7420 5411086	40–44	E13A1	+15 V 61.5 Vdc	0.45 Vdc
Lower H7420 5411086	2, 17, 25–27 29–31 33–35 37–44	E13B2	-15 V ±1.5 Vdc	0.45 Vdc

*Use a digital voltmeter, Data Technology Model 31, or Weston-Slumberger Model 4443, or equivalent.

Table 3-2 Regulator Test Points (MJ11)

M8149 Test Point*	Regulator	Voltage	Regulator Pins	Backplane Connector Pins
TP1	744 No. 4	+5 Vdc	J16-2,5	J21-5,6,7,8
TP2	744 No. 2	+5 Vdc	J14-2,5	J18-1,2,3,4
TP3	754 No. 3	+20 Vdc	J15-5	J21-3,4
TP4	754 No. 1	+20 Vdc	J13-5	J18-5,6
TP5	754 No. 3	-5 Vdc	J15-3	J21-1,2
TP6	754 No. 1	-5 Vdc	J13-3	J18-7,8
TP7		TP Ground		

*These test points are located approximately 1.5 inches from the edge of the M8149 that faces the front of the cabinet. TP1 is the top test point. Refer to Figure 4-43.

Table 3-3 Regulator Voltage Measurements (MK11)

Regulator	Voltage	Regulator Pins	Backplane Connector Pins	Backplane Slots Supplied
H7441	+5 Vdc	J14-1, 2, 5	J18-1, 2 J21-7	10–17
7014251 'A'	+5 Vdc	J13-4	J18-4	6–13
	+12 Vdc	J13-1	J18-5	6–13
	-12 Vdc	J13-6	J18-7	6–13
7014251 'B'	+5 Vdc	J15-4	J21-5	15–21
	+12 Vdc	J15-1	J21-4	15–21
	-12 Vdc	J15-6	J21-2	15–21
7014251 'C'	+5 Vdc	J16-4	J21-6	2–5, 22–25
	+12 Vdc	J16-1	J21-3	2–5, 22–25
	-12 Vdc	J16-6	J21-1	2–5, 22–25

5. Turn all ac power breakers to the OFF position.

6. Set all LOCAL/REMOTE switches to the REMOTE position, and verify that the remote sensing cables are installed.

7. Check all free-standing peripherals.

8. Install all the Unibus, Massbus, and peripheral cables. Install Unibus terminator at the end of the Unibus.

9. Put the ac breakers on the power control(s) and supplies to the ON position.

3.3.3.5 Preliminary System Check – Load all disk and magtape units with Scratch packs and tapes.

Since the PDP-11/70 bootstrap module (M9301-YC) contains a diagnostic, all the preliminary CPU checks listed in Chapter 4 of the PDP-11 Family Field Installation and Acceptance Procedure need not be performed.

Turn on the CPU key and ensure that the power comes up. Check ac/dc low on the Unibus for proper levels (>4.0 Vdc).

Figure 4-37, ACLO and DCLO CIRCUITS, shows all points where ACLO and DCLO may be checked.

3.4 SYSTEM CHECKOUT (Chapter 5 of PDP-11 Family Field Installation and Acceptance Procedure)

The system checkout is intended to prove the integrity of the PDP-11/70.

It consists of the following operations (refer to Figure 3-9):

1. Checking the console functions
2. Booting the XXDP diagnostic monitor via the M9301-YC
3. Running the CPU and applicable peripheral diagnostics, and
4. Running the system software exerciser, if available.

When these have been run successfully and the customer has accepted the system, the installation is complete.

If the system fails, refer to Chapter 5 (Maintenance) for troubleshooting procedures. No failures are permitted during the CPU, cache, main memory, memory management, Unibus map or (optional) floating point processor diagnostics. The error criteria for peripheral equipment are specified in the PDP-11 Family Field Installation and Acceptance Procedure.

Refer to Figure 3-9, which is a detailed installation checkout procedure. The several steps in this flowchart are explained in the paragraphs that follow.

3.4.1 Console Functions

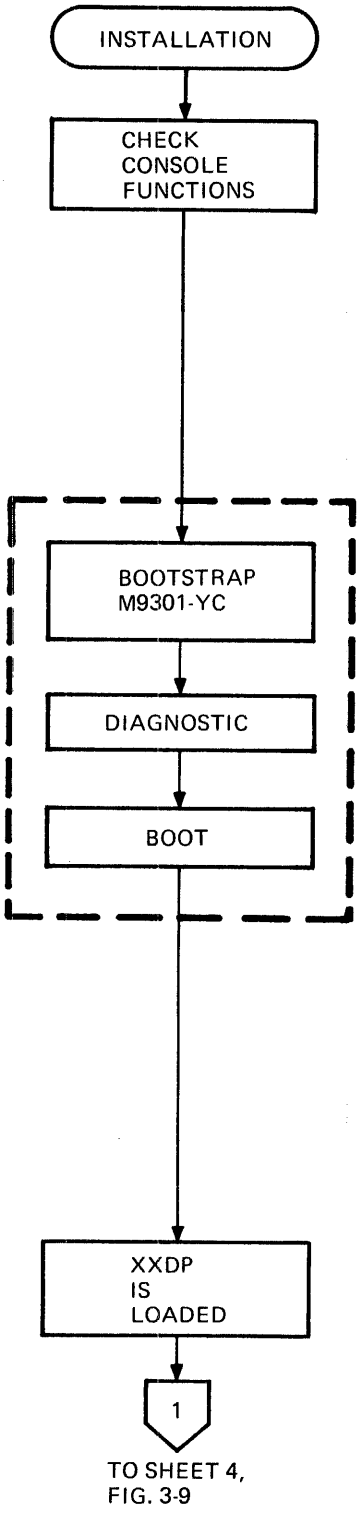
Refer to Section III, Chapter 1 of the KB11-B Processor Manual or to the *PD-11/70 Processor Handbook* for a detailed description of the console and its operation.

3.4.2 Bootstrap Modules

The M9301-YC, -YH, and M9312 modules contain ROM programs located on the peripheral page, as shown on the memory map in Figure 3-10; note that the programs take up part of the user addresses (17 765 000 – 17 765 776) and all the bootstrap addresses (17 773 000 – 17 773 776). Paragraph 5.4.11 lists the programs and a brief explanation of their operation.

The ROM programs check the CPU first, then main memory, and the cache. Then it boots the XXDP monitor from the device selected. Note that early versions of XXDP load only from drive unit number zero.

Figure 3-9 summarizes instructions for using the M9301 and M9312. If the low order byte of the Switch register contains 0, a default device and drive are selected by switches on the M9301.



LOAD ADDRESS
DEPOSIT & DEPOSIT/STEP }:
EXAMINE & EXAMINE/STEP }:
  { FROM GENERAL REGISTERS (ADDRESSES 17 777 700 - 17)
  { FROM MEMORY (ANY OTHER EXISTING ADDRESS)
START
CONTINUE

LOAD ADDRESS 17 765 000
LOAD DEVICE CODE (OCTAL) INTO SWITCH REGISTER <06:03>
(ALL DEVICES HAVE XXDP AVAILABLE AT THIS TIME)

1)	TM11/TU10	MAGNETIC TAPE, TM11
2)	TC11/TU56	DECtape, TC11-G
3)	RK11/RK05	DECpack DIS CARTRIDGE, RK11-D
4)	RP11/RP03	DISK PACK, RP11-C
5)	RK611/RK06 DISK*	
6)	RH70/TU16	MAGNETIC TAPE SYSTEM, TWU16
7)	RH70/RP04	DISK PACK, RWP04
10)	RH70/RS34	FIXED HEAD DISK, RWS04 (OR RSW03)
11)	RX11/RX01	DISKETTE

(*NOT AVAILABLE ON EARLY VERSIONS OF M9301-YC)
LOAD DRIVE NUMBER 000 INTO SWITCH REGISTER
<02:00> DRIVE 0 IS REQUIRED, SINCE XXDP
AT PRESENT LOADS ITS MONITOR FROM DRIVE 0.
LOAD THE PHYSICAL MEMORY BLOCK DESIRED (OCTAL) INTO
SWITCH REGISTER <15:12>.

0)	PHYSICAL MEMORY	00 000 000 - 00 077 776
1)	PHYSICAL MEMORY	00 100 000 - 00 177 776
2)	PHYSICAL MEMORY	00 200 000 - 00 277 776
3)	PHYSICAL MEMORY	00 300 000 - 00 377 776
4)	PHYSICAL MEMORY	00 400 000 - 00 477 776
5)	PHYSICAL MEMORY	00 500 000 - 00 577 776
6)	PHYSICAL MEMORY	00 600 000 - 00 677 776
7)	PHYSICAL MEMORY	00 700 000 - 00 777 776
10)	PHYSICAL MEMORY	01 000 000 - 01 077 776
11)	PHYSICAL MEMORY	01 100 000 - 01 177 776
12)	PHYSICAL MEMORY	01 200 000 - 01 277 776
13)	PHYSICAL MEMORY	01 300 000 - 01 377 776
14)	PHYSICAL MEMORY	01 400 000 - 01 477 776
15)	PHYSICAL MEMORY	01 500 000 - 01 577 776
16)	PHYSICAL MEMORY	01 600 000 - 01 677 776
17)	PHYSICAL MEMORY	01 700 000 - 01 777 776
⋮		
40)	PHYSICAL MEMORY	17 700 000 - 17 777 776

START

MESSAGE TYPED ON LA36. REFER TO "XXDP USER MANUAL," MAINDEC-11-DZQXA FOR DETAILED EXPLANATION.

TK-1465

Figure 3-9 System Checkout (Sheet 1 of 4)

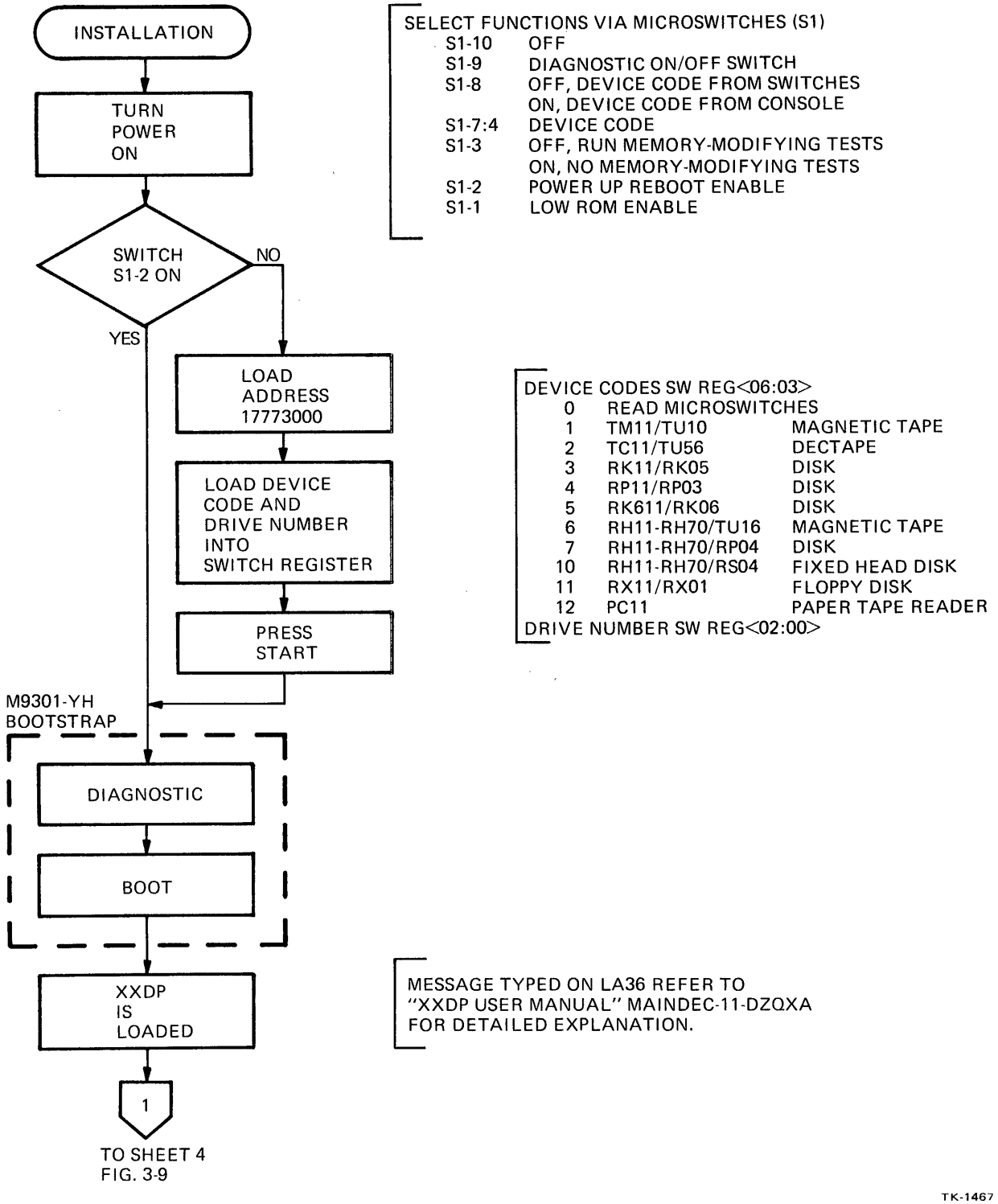


Figure 3-9 System Checkout (Sheet 2 of 4)

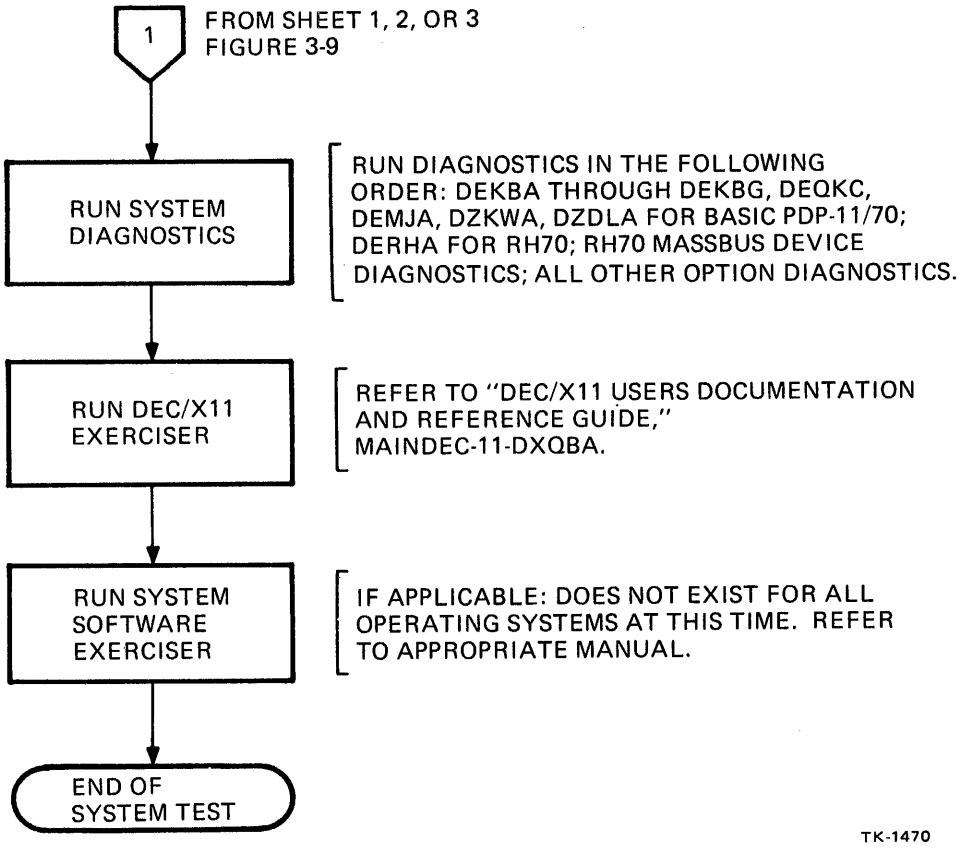


Figure 3-9 System Checkout (Sheet 4 of 4)

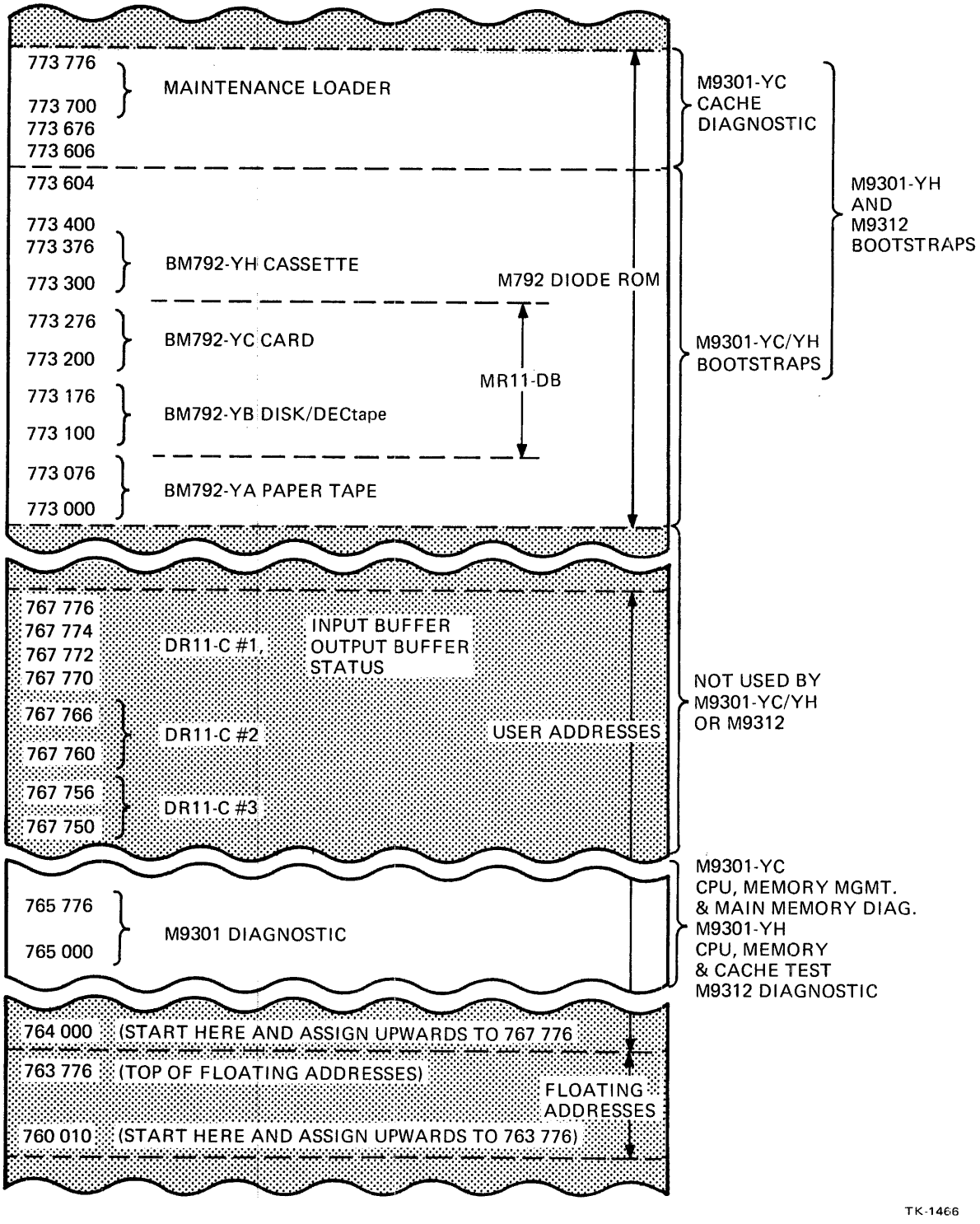


Figure 3-10 Location of M9301-YC, YH and M9312 in Peripheral Page
(Refer to PDP-11 Peripherals Handbook)

The diagnostic portion of the programs test the basic CPU, including the branches, the registers, all addressing modes, and most of the instructions in the PDP-11 repertoire. Then it sets the stack pointer to Kernel D-space PAR 7, checks and turns on, if requested, memory management and the Unibus map, and checks memory from virtual address 1000 to 157776. After main memory has been verified, with the cache off, the cache memory is tested to verify that hits occur properly. Then main memory is scanned again to ensure that the cache is working properly throughout the 28K of memory to be used in the boot operation.

If one of the cache memory tests fails, the operator can attempt to boot the system anyway by pressing CONTINUE. This causes the program to force MISSES in both groups of the cache before going to the bootstrap section of the program.

The bootstrap portion of the programs look at the lower byte of the Switch register to determine which device will attempt the boot for load-address start sequences. (Note that XXDP loads only from drive 0). With the M9301, switches (02:00) select the drive number (0–7 octal), and switches (06:03) select the device code (1–11 octal). If the lower byte of the Switch register is zero, the program reads the set of switches on the M9301 to determine the device and drive number. These switches can be set to select a default boot device. With the M9312, switch register switches (11:0) select the starting address of one of the ROM Boot Programs installed on the module. Each device has its own boot ROM, the address in the switch register selects one of the four ROMs on the module

Automatic boot on power-up is available with both the M9301-YH and the M9312. When enabled, the module will boot the device selected by switches on the module when the processor power is turned on.

If the bootstrap operation fails as a result of a hardware error in the peripheral device, the program will perform a RESET instruction and jump back to the test that sets up and turns on memory management and tests memory. Then the program attempts to boot again.

3.4.2.1 Starting Procedure, M9301-YC

Switch Settings – The lower byte of the Switch register should be set to have the drive number (0–7 octal) in switches (02:00), and the device code (1–11) in switches (06:03). Drive 0 is required for XXDP, since the XXDP monitor uses drive 0.

The upper byte of the Switch register (15:12) should be set to (0–17 octal) to have the bank number of the 32K block of memory which will be used for the bootstrap operation.

The device codes are as follows:

1 TM11/TU10 Magnetic Tape, TM11
2 TC11/TU56 DECtape, TC11-G
3 RK11/RK05 DECpack Disk Cartridge, RK11-D
4 RP11/RP03 Disk Pack, RP11-C
5 RK611/RK06 Disk Pack
6 RH70/TU16 Magnetic Tape System, TWU16
7 RH70/RP04 Disk Pack, RWP04
10 RH70/RS04 Fixed Head Disk, RWS04 (or RWS03)
11 RX11/RX01 Diskette (Floppy Disk)

The memory blocks are as follows:

0 Physical Memory 00 000 000 - 00 077 776
1 Physical Memory 00 100 000 - 00 177 776
2 Physical Memory 00 200 000 - 00 277 776
3 Physical Memory 00 300 000 - 00 377 776
4 Physical Memory 00 400 000 - 00 477 776
5 Physical Memory 00 500 000 - 00 577 776
6 Physical Memory 00 600 000 - 00 677 776
7 Physical Memory 00 700 000 - 00 777 776
10 Physical Memory 01 000 000 - 01 077 776
11 Physical Memory 01 100 000 - 01 177 776
12 Physical Memory 01 200 000 - 01 277 776
13 Physical Memory 01 300 000 - 01 377 776
14 Physical Memory 01 400 000 - 01 477 776
15 Physical Memory 01 500 000 - 01 577 776
16 Physical Memory 01 600 000 - 01 677 776
17 Physical Memory 01 700 000 - 01 777 776
.
.
.
40 Physical Memory 17 700 000 - 17 777 776

Starting Addresses, M9301-YC – The normal starting address for DEKBH is 17 765 000.

If the diagnostic portion of this program fails and the operator wants to attempt to boot anyway, he must follow these steps:

1. Set up memory management if booting into other than the lower 28K of memory.

2. If device is on Massbus, set stack pointer to a valid address and load that address with the memory bank number the operator would put into switches (15:12).

   If device is on Unibus, set up Unibus Map registers 0 through 6 to map to same memory as memory management.

3. Deposit address 173000 into the PC.

4. Set the device code and drive number in the lower byte of the Switch register.

5. Press CONTINUE.

   Examples:

   a. RP04: Set stack pointer to 40000
   Load 000000 into address 40000
   Load 173000 into the PC (17 777 707)
   Set 000070 into switches (RP04 Drive 0)
   Press CONTINUE

   b. RK05: Load 173000 into the PC (17 777 707)
   Set 000030 into switches (RK05 Drive 0)
   Press CONTINUE

Operator Action – If the diagnostic portion of the ROM fails, record the PC of the HALT instruction and refer to the listing (or to Chapter 5) to find out which portion of the machine failed.

3.4.2.2 Errors, M9301-YC – List of error halts indexed by the address displayed.

Address Displayed	Test Number and Subsystem Under Test
17765004	Test 1 Branch Test
17765020	Test 2 Branch Test
17765036	Test 3 Branch Test
17765052	Test 4 Branch Test
17765066	Test 5 Branch Test
17765076	Test 6 Branch Test
17765134	Test 7 Register Data Path Test
17765146	Test 10 Branch Test
17765166	Test 11 CPU Instruction Test
17765204	Test 12 CPU Instruction Test
17765214	Test 13 CPU Instruction Test
17765222	Test 14 "COM" Instruction Test
17765236	Test 14 CPU Instruction Test
17765260	Test 15 CPU Instruction Test
17765270	Test 16 Branch Test
17765312	Test 16 CPU Instruction Test
17765346	Test 17 CPU Instruction Test
17765360	Test 20 CPU Instruction Test
17765374	Test 20 CPU Instruction Test
17765450	Test 21 Kernel PAR Test
17765474	Test 22 Kernel PDR Test
17765510	Test 23 JSR Test
17765520	Test 23 JSR Test
17765530	Test 23 RTS Test
17765542	Test 23 RTI Test
17765550	Test 23 JMP Test
17765760	Test 25 Main Memory Data Compare Error
17766000	Test 25 Main Memory Parity Error (No recovery possible from this error)
17773644	Test 26 Cache Memory Data Compare Error
17773654	Test 26 Cache Memory No Hit Pressing CONTINUE here will cause boot attempt forcing misses
17773736	Test 27 Cache Memory Data Compare Error
17773746	Test 27 Cache Memory No Hit Pressing CONTINUE here will cause boot attempt forcing misses
17773764	Test 25 or 26 Cache Memory Parity Error Pressing CONTINUE here will cause boot attempt forcing misses

Error Recovery – Most of the preceding error halts are *hard* failures, which means that there is no recovery from them. The two main memory halts are not recoverable; attempt to boot into another 32K bank of memory if it appears to be a main memory failure.

If the processor halts in one of the two cache tests, the error is recoverable. By pressing CONTINUE, the program will either attempt to finish the test (if at either 17 773 644 or 17 773 736), or force MISSES in both groups of the cache and attempt to boot the system monitor with the cache fully disabled (if at either 17 773 654, 17 773 746, or 17 773 764).

3.4.2.3 Execution Time – The run time for this program is approximately three seconds.

3.4.2.4 M9301-YC Switches – Refer to schematic D-CS-M9301-0-1, revisions E and F.

Two different revisions of the M9301 are in the field: E and F. They are easily recognized by the number of Fastab connectors on the modules: Rev. E has two Fastabs while Rev. F has three (Figure 3-11).

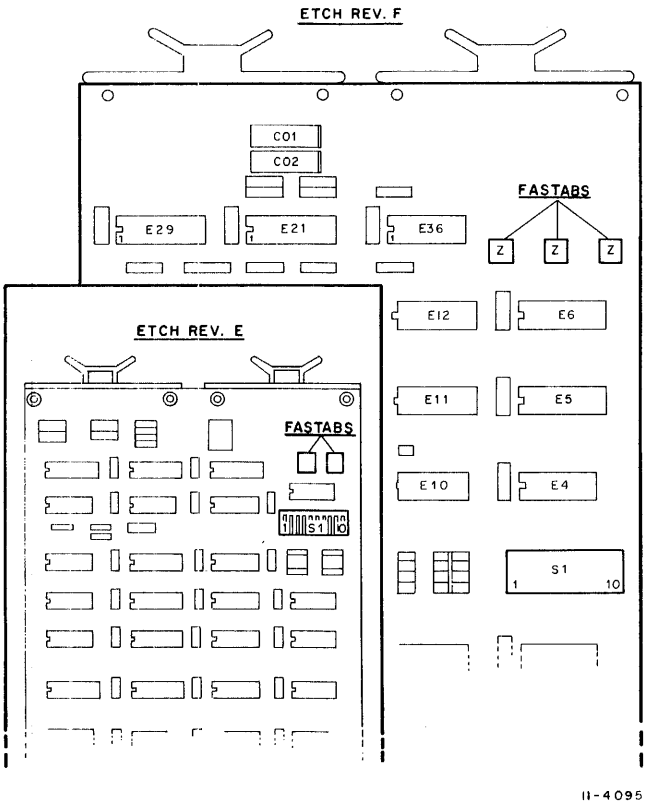


Figure 3-11 M9301-YC Etch Revisions

There is a 10-pole DIP switch, S1, on both versions of the M9301.

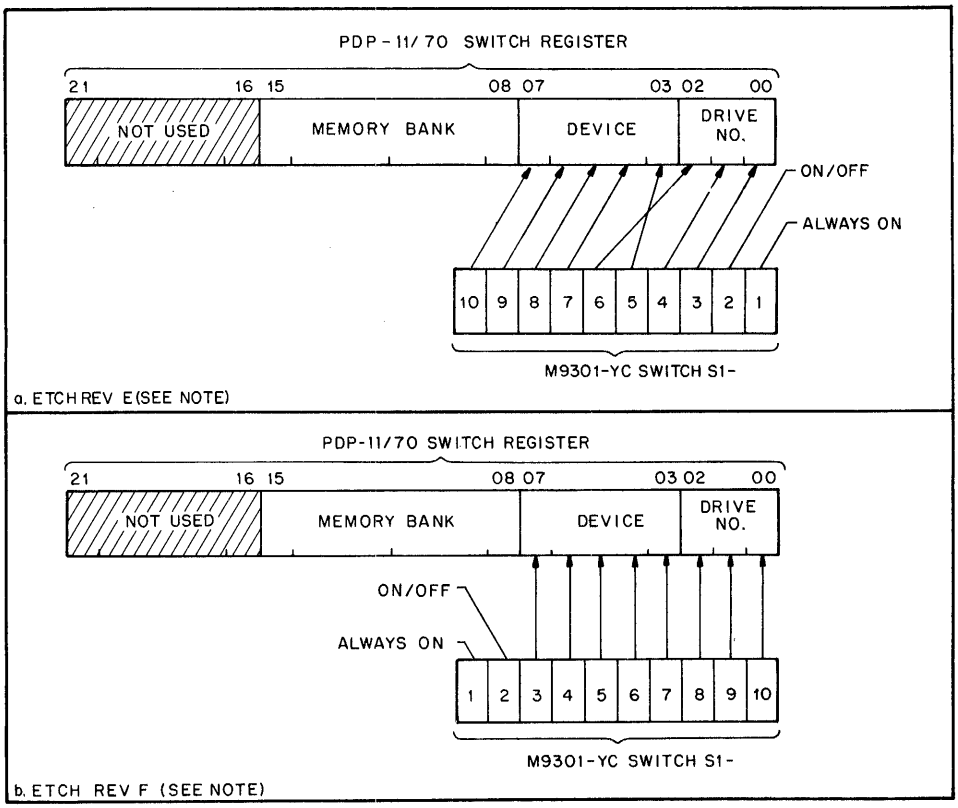
1. S1-1 must be always ON in the PDP-11/70. It allows reading locations 17 765 000 – 17 765 776.

2. S1-2 must be ON, for remote booting on power up. M9301 remote booting is available by installing M9301 ECO 5, M8138 ECO 5, M8136 ECO 4, M8130 ECOs 1–3, and >010329 ECO 8.

3. S1-3 through S1-10 determine the device and drive that are to be used if Switch register bits (07:00) are all 0s. Figure 3-12 shows the correspondence between S1-3 through S1-10 on both revisions of the M9301-YC. The switches must be OFF to generate a 1: refer to sheet 4 of the schematic and to Paragraph 5.4.12, Default Device and Drive.

NOTE

As of this writing, XXDP only loads to physical address 0 from drive 0. XXDP will be modified in the near future to load into any of the sixteen blocks of memory that can be specified by Switch register bits 15:12 (refer to Figure 3-9).



Note: When S1-3 through S1-10 are OFF, they correspond to a 1 in the Switch Register.

11-3471

Figure 3-12 Use of S1-1 through S1-10 on M9301-YC

3.4.2.5 Starting Procedure M9301-YH – The operation of the M9301-YH is similar to that of the M9301-YC. The M9301-YH provides the additional feature of booting automatically on power-up, or by a load-address start sequence.

M9301-YH Microswitch settings – Prior to installation, set the microswitches on the M9301 (S1) to select the desired functions and default device. The default device set by the switches will be booted during a power-up boot or a load-address start sequence if no device is specified by the console switch register. Note that jumpers W1–W5 on the M9301 must be inserted for PDP-11/70's and also that for the automatic power-up boot, ECO 5 must be installed (with jumper W-6 in).

Configure the microswitches as indicated below:

S1-1	Low ROM enable; normally ON, enables diagnostics
S1-2	Power-up boot enable; boots on power-up when ON
S1-3	Memory modifying test disable; when OFF, all diagnostic tests run, when ON, disables tests 21–24
S1-4:7	Default device code (S1-4 is the MSB)
S1-8	Device code source; OFF, device code read from microswitches ON, device code read from console switch register
S1-9	Diagnostic ON/OFF disables all diagnostics
S1-10	OFF for all PDP-11/70's

The device codes (S1-4:7) are as follows:

1	TM11/TU10	Magnetic Tape
2	TC11/TU56	DECtape
3	RK11/RK05	Disk
4	RP11/RP03	Disk
5	RK611/RK06	Disk
6	RH11-RH70/TU16	Magnetic Tape
7	RH11-RH70/RP04	Disk
10	RH11-RH70/RS04	Fixed Head Disk
11	RX11/RX01	Floppy Disk
12	PC11	Paper Tape Reader

The default device is always drive unit number zero.

Power-Up Boot – With microswitch S1-2 in the ON position an automatic boot on power-up will occur from the default device specified in the microswitches or optionally from the device specified by the console switch register. If switch S1-8 is OFF, the M9301 will always boot the default device specified by the microswitches. If switch S1-8 is ON, the device may be selected by loading a device code into the switch register prior to power-up. The M9301-YH will boot the default device with S1-8 ON if no device is specified by the switch register; that is, if the switch register low byte is equal to zero.

With switch S1-8 OFF, select the device with the switch register as follows:

SW REG(6:3)
Device Code

0	Use the device specified in microswitches (S1-7:S1-4)	
1	TM11/TU10	Magnetic Tape
2	TC11/TU56	DECtape
3	RK11/RK05	Disk
4	RK11/RP03	Disk
5	RK611/RK06	Disk
6	RH11/RH70/TU16	Magnetic Tape
7	RH11/RH70/RP04	Disk
10	RH11/RH70/RS04	Fixed Head Disk
11	RX11/RX01	Floppy Disk
12	PC11	Paper Tape Reader

SW REG (2:0) Drive Unit Number

Load Address Start Sequence – This mode allows the user to boot from any device and any unit number available for load address starts. Microswitch S1-2 must be OFF and microswitch S1-8 must be ON.

The boot procedure is as follows:

1. Turn power ON.
2. Load address 17773000.
3. Load switch register (6:3) with device code and (2:0) with drive number.
4. Start.

3.4.2.6 Errors, M9301-YH – The following is a list of error halt addresses and the corresponding test.

Address Displayed	Test Number and Subsystem Under Test
17765004	Test 1, Branch Test
17765020	Test 2, CLR and Conditional Branch Test
17765036	Test 3, DEC and Conditional Branch Test
17765052	Test 4, ROR and Conditional Branch Test
17765066	Test 5, Conditional Branch Test
17765076	Test 6, Conditional Branch Test
17765126	Test 7, Register Data Path Test
17765136	Test 10, Conditional Branch Test
17765154	Test 11, CPU Instruction Test
17765172	Test 12, CPU Instruction Test
17765202	Test 13, CPU Instruction Test
17765210	Test 14, CPU Instruction Test
17765224	Test 14, CPU Instruction Test
17765246	Test 15, CPU Instruction Test
17765256	Test 16, Branch Test
17765300	Test 16, CPU Instruction Test
17765334	Test 17, CPU Instruction Test
17765352	Test 20, CPU Instruction Test

17765376	Test 21, JSR Test
17765406	Test 21, JSR Test
17765416	Test 21, RTS Test
17765430	Test 21, RTI Test
17765436	Test 21, JMP Test
17765520	Test 22, Main Memory Data Compare Error
17765540	Test 22, Main Memory Data Compare Error, no recovery possible from this error
17765604	Test 23, Cache Memory Data Compare Error
17765614	Test 23, Cache Memory No Hit (pressing continue here will cause boot attempt, forcing cache misses)
17765720	Test 24, Cache Memory Data Compare Error
17765732	Test 24, Cache Memory No Hit (pressing continue here will cause boot attempt, forcing misses in the cache)
17765752	Test 22, 23, or 24, Cache Memory or Main Memory Parity Error. (Examine memory error register 777744 to find out more.) If cache parity error, pressing continue here will cause boot attempt forcing misses in cache:

Most of the errors listed are hard failures, and there may be no recovery from them.

If the processor halts in one of the two cache tests, error recovery is possible. When continue is pressed, the program will either attempt to finish the test (1776504 or 17765720) or force misses in both groups of the cache and attempt to boot with the cache fully disabled (1776514, 17765732, or 17765752).

If the program fails in an uncontrolled manner, it might be due to an unexpected trap to location 4 or 10. If this is suspected, then load the following.

Location	**Contents**
4	6
6	0
10	10
12	0

The preceding steps will cause all traps to vectors 4 and 10 to halt the processor at addresses 6 and 12, respectively (with addresses 10 and 14 in the display); the operator can examine the CPU error register at 17777766 to get more error information. Bits in CPU error register are defined as follows:

Bit 02 = Red Zone Stack Limit
Bit 03 = Yellow Zone Stack Limit
Bit 04 = Unibus Timeout
Bit 05 = Nonexistent Memory
Bit 06 = Odd Address Error
Bit 07 = Illegal Halt

3.4.2.7 Starting Procedure M9312 - The M9312 bootstrap module executes its diagnostic and boot routines initiated either automatically on power-up or by a load address start procedure. The bootstrap programs are stored in ROMs that plug into sockets on the M9312. Each device is booted only by its own ROM; up to four ROMs can be installed on the M9312. Devices for power-up booting are selected by specifying a starting address of one of the ROM boot routines. These functions are selected with microswitches (S1) on the module prior to installation. The location of S1 is shown in Figure 3-13.

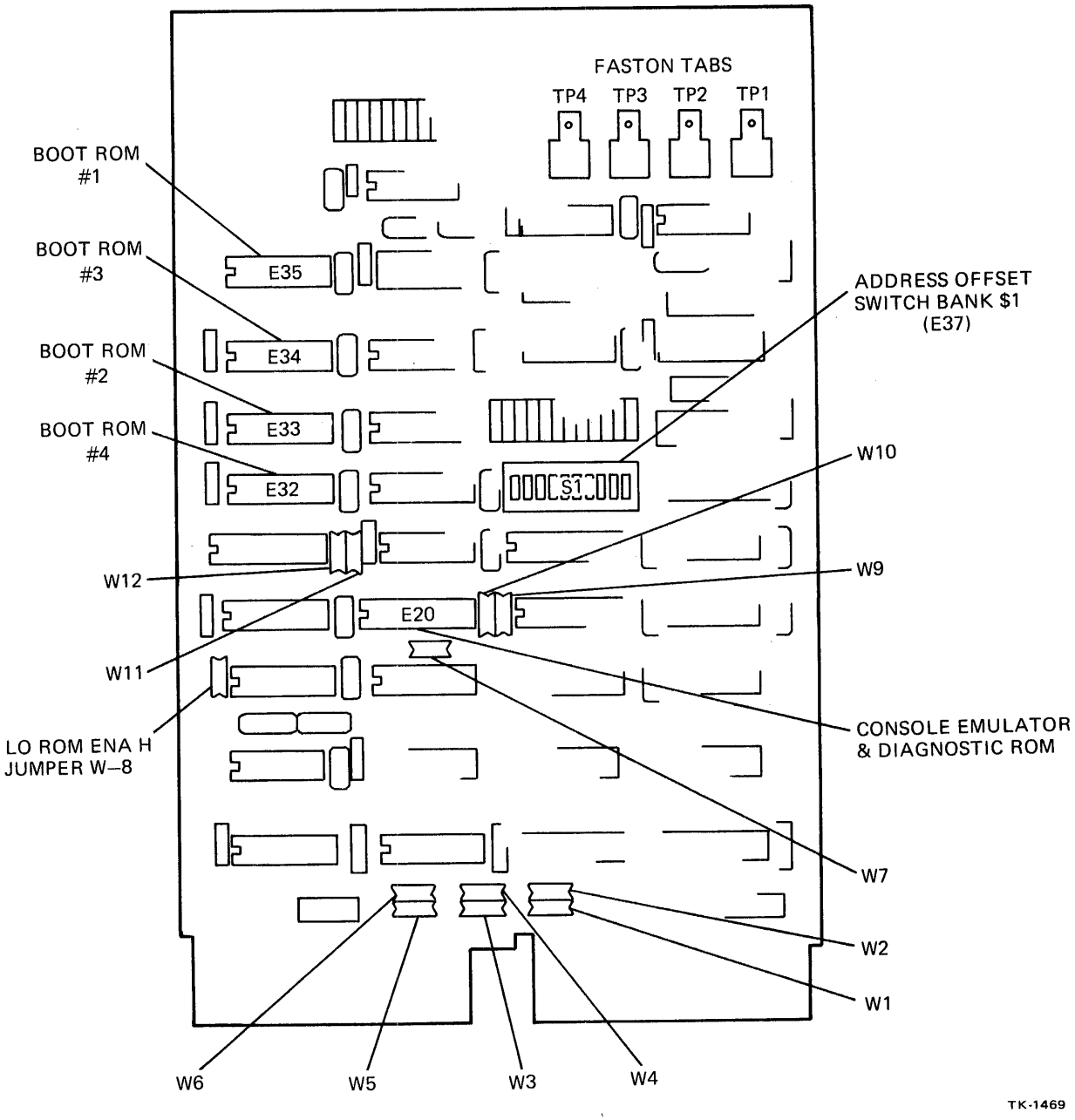


Figure 3-13 M9312 Bootstrap/Terminator Module

Power-Up Boot – The module performs a power-up boot when switch S1-2 is in the ON position. The device used will depend on the ROMs installed and the starting address selected by switches S1-3:9. Set the switches as follows:

S1-1	OFF
S1-2	ON for power-up boot
S1-3:9	Offset address of ROM program
S1-10	ON for diagnostics

The following lists the available ROMs by part number, the device or devices they boot, and the address to set in microswitches to select the device for booting.

Part Number	Device	S1 Switch Settings 5	6	7	8	9
23-751A9	RL01	OFF	OFF	OFF	OFF	ON
23-752A9	RX06/07	OFF	OFF	OFF	OFF	ON
23-753A9	RX01	OFF	OFF	OFF	OFF	ON
23-754A9	RX02	OFF	OFF	OFF	OFF	ON
23-755A9	RP02/03	OFF	OFF	OFF	OFF	ON
	RP04/516, RM02/3	OFF	ON	OFF	ON	OFF
23-756A9	RK03/05/05J (Unit 0)	OFF	OFF	OFF	OFF	ON
	RK03/05/05J (Unit 20	ON	ON	ON	OFF	ON
	TU55/56	OFF	OFF	ON	ON	ON
23-757A9	TU16/E16 (TM02/03)	OFF	OFF	OFF	OFF	ON
23-758A9	TU10/TE10, TS03	OFF	OFF	OFF	OFF	ON
23-759A9	RS03/04	OFF	OFF	OFF	OFF	ON
23-760A9	PC05	OFF	OFF	OFF	OFF	ON
	DL11A/W	OFF	OFF	ON	ON	ON
23-761A9	TU60	OFF	OFF	OFF	OFF	ON
23-762A9	RS11	OFF	OFF	OFF	OFF	ON
	RS64	OFF	ON	OFF	ON	OFF
23-763A9	CR11	OFF	OFF	OFF	OFF	ON

The setting of switches S1-3 and S1-4 depends on the ROM location in which the boot ROM is located.

ROM Slot	S1-3	S1-4
1	OFF	OFF
2	OFF	ON
3	ON	OFF
4	ON	ON

Load Address Start Sequence – When microswitch S1-2 is placed in the OFF position, the device is specified by the console switch register. The address loaded in the switch register depends on which ROMs are installed and in which ROM locations they are located.

The load address start sequence is as follows.

1. Turn power ON.
2. Load address 765744.
3. Load switch register (8:0) with starting address and (11:9) with drive unit number.
4. Press START.

Switch register bits (11:9) are loaded with an octal number that is the drive number of the device used for booting.

Switch register bits (8:6) correspond to the ROM socket number in which the ROM is located. Set switches (8:6) on the console as follows:

ROM Socket Number	SW Reg (8:6)
1	0
2	2
3	4
4	6

Switch register bits (5:0) point to the starting address of the ROM boot program in the ROM selected by switch register bits (8:6). The following lists the available ROMs by part number and their devices, along with the address to load in switch register bits (5:0).

Part Number	Device	SW REG (5:0)
23-751A9	RL01	12
23-752A9	RK06/07	12
23-753A9	RX01	12
23-754A9	RX02	12
23-755A9	RP02/03	12
	RP04/516, RM02/03	56
23-756A9	RK03/05/05J	12
	TU55/56	42
23-757A9	TU16/E16 (TM02/03)	12
23-758A9	TU10/TE10, TS03	12
23-759A9	RS03/04	12
23-760A9	PC05	12
	DL11A/W	42
23-761A9	TU60	12
23-762A9	RS11	12
	RS64	56
23-763A9	CR11	12

3.4.2.8 Errors - M9312 – The following is a list of diagnostic error halt addresses and the corresponding failing test. Most of the errors are hard failures and there will be no recovery from them. If one of the cache memory tests fails (test 23 at location 165564 or test 24 at location 165704), attempt to boot the system by pressing continue. This will cause the program to force misses in both groups of cache before going to the bootstrap portion of the program.

Address Displayed	Test Number	Failing Test
165050	1	Unconditional Branch Test
165064	2	CLR, BMI, BVS, BHI, BLOS Test
165102	3	DEC, BPL, BEQ, BGE, BGT, BLE Test
165116	4	ROR, BVC, THIS, BIT, BNE Test
165132	5	SEZ, BHI, BLT, BLOS Test
165142	6	CLZ, BLE, BGT Test
165160	11	ADD, INC, COM, BCS, BLE, Test
165176	12	ROR, BIS, ADD, BLO, BGE Test
165206	13	DEC, BLOS, BLT Test
165214	14	COM, BLOS Test
165230	14	BIC, BGT, BGE, BLE Test
165250	15	ADC, CMP, BIT, BNE, BGT, BEQ Test
165260	16	MOVB, BPL Test
165302	16	SOB, CLR, TST, BNE Test
165320	20	ASH, SWAB Test
165332	21	JSR Test
165342	21	JSR Test
165352	21	RTS Test
165364	21	RTI Test
165372	21	JMP Test
165470	22	Main Memory Data Compare Test
165510	22	Main Memory Complement Data Test
165724	22	Main Memory Parity Error
165554	23	Cache Data Compare Test
165564	23	Cache Miss (Press continue to boot)
165672	24	Cache Data Compare Test
165704	24	Cache Miss (Press continue to boot)
165724	24	Cache/Main Memory Parity Error

3.4.2.9 M9312 Boot ROM Identification – Every boot ROM contains an identification code stored in the ROM program. To identify the type of ROM installed, examine the contents of the ROM's ID location at the console switch register and then find the part number from the list included below.

To identify the ROM in ROM socket number one, examine address 773000. To identify the ROM in ROM location two, examine address 773200. To identify the ROM in ROM location three, examine address 773400; and for the ROM in ROM socket number four, examine address 773600.

Contents of ROM ID Address	ROM Part Number	Used with Device
042114	23-751A9	RL01
042115	23-752A9	RK06/07
042130	23-753A9	RX01
042131	23-754A9	RX02
042120	23-755A9	RP02/03, RP04/516, RM02/03
042113	23-756A9	RK03/05/05J, TU55/56
046515	23-757A9	TU16/E16, TM02/03
046524	23-758A9	TU10/TE10, TS03
042123	23-759A9	RS03/04

050122	23-760A9	PC05, DL11A/W
041524	23-761A9	TU60
042106	23-762A9	RS11, RS64
041522	23-763A9	CR11

3.4.3 Diagnostics

Locate the installation checklist, K-SP-7668010 (a computer print-out). Compare the configuration key, or transfer sheet to the installation checklist and check under "Run" the diagnostic tests for all options listed as being present in this system.

Load and run the diagnostics listed in the installation checklist which are applicable to the system for the time or number of passes specified.

The diagnostics should be run in the order specified on Figure 3-9. Abstracts of the CPU diagnostics are reproduced in Chapter 5. Operating procedures and listings for all diagnostics are contained in the MAINDECs for each program.

Operating procedures for the XXDP monitor are described in the *XXDP User Manual, MAINDEC-11-DZQXA.*

3.4.4 DEC/X11 System Exerciser

DEC/X11 is a system exerciser, i.e., it is an operating system that runs all devices in a system, using random data. Any errors are reported.

DEC/X11 must be configured for each individual system. The *DEC/X11 User's Documentation and Reference Guide,* MAINDEC-11-DXQBA contains all information required to configure and run DEC/X11 and to interpret the results of the tests performed. The XXDP DEC/X11 Programming Card, MAINDEC-11-DZZPA contains a summary of DEC/X11 features.

Turn to the system exerciser section of installation checklist and prepare to load DEC/X11. The system exerciser checklist numbering sequence begins with IBXXXX. To start the DEC/X11 package, see the notes at the beginning of the system exerciser section of the installation checklist.

3.4.5 System Software Exerciser (Under Development)

The system software exerciser will be similar to DEC/X11, except that it will use the system software operating system. Because of this, it will be a better test of the integrity of a system than DEC/X11. A printout will be available for each version of the software exerciser.

3.4.6 Summary and Final Acceptance

Go through each chapter of the PDP-11 Family Field Installation and Acceptance Procedure and ensure that all areas requiring an initial are so marked. If an initial is missing, investigate that section and complete if necessary.

Ensure that all paperwork is complete. The Field Service and/or installation reports should reflect any problems/repairs encountered during the installation. After completion, the reports and checklists should be returned to the office.

The installation is now complete. Have the customer sign the Field Service Report reflecting installation activity.

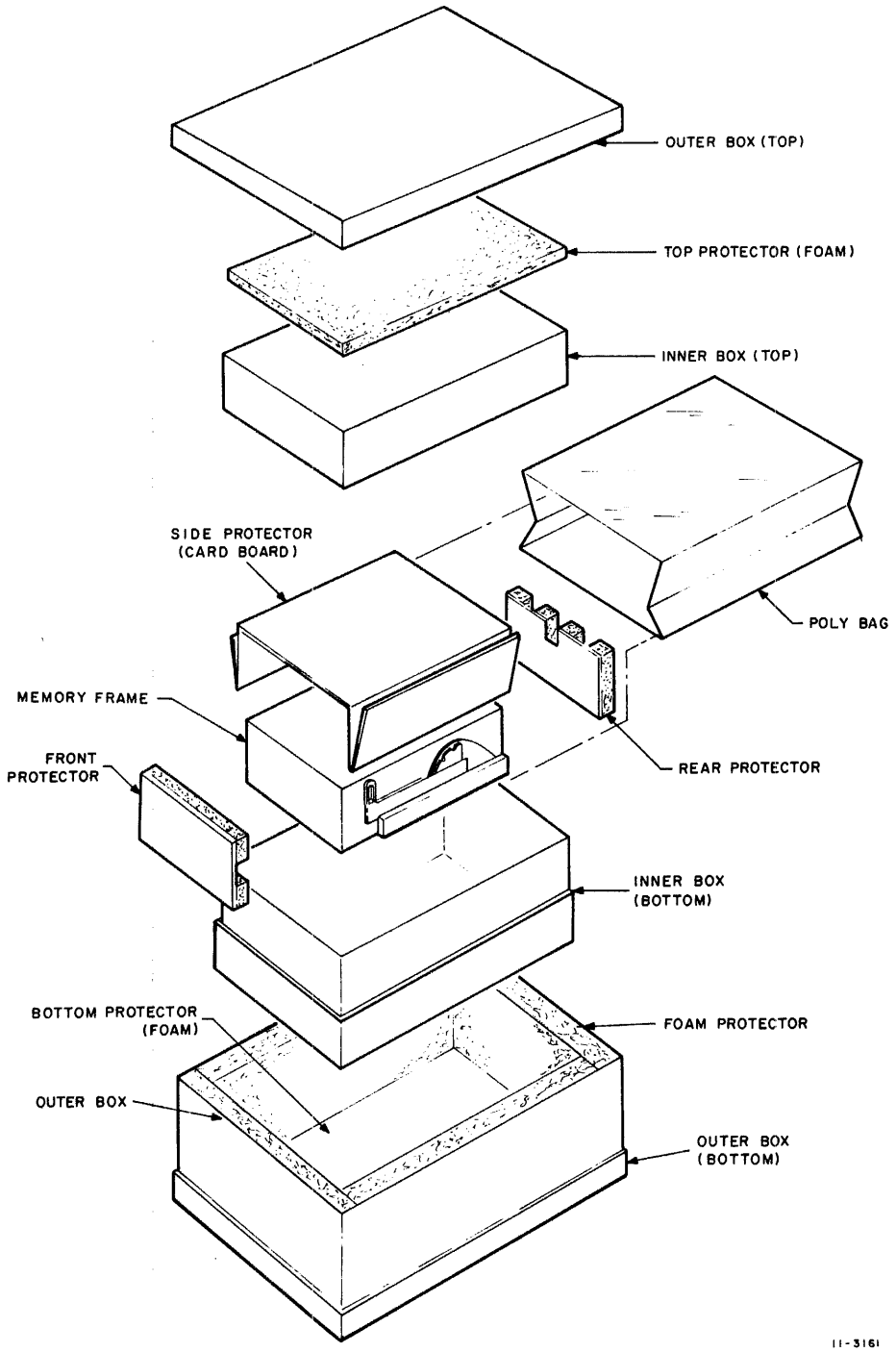


Figure 3-14 Memory Frame Packaging

3.5 MJ11 MEMORY EXPANSION

An MJ11 memory frame is shipped in a protective box (Figure 3-14). Remove the memory frame from the box and inspect for damage. Save the shipping cartons and packaging materials in case it becomes necessary to return the memory frame for service. The slide mounts are attached to the memory frame, but the mounting screws are packed in a bag placed in the shipping container.

Slide Mounting – The fixed slides must be mounted equidistant from and parallel to the floor at the proper cabinet frame hole number (Figure 3-15). The front of the fixed slide has an integral bracket and is mounted in the cabinet with four screws that are secured with captive (Tinnerman) nuts. The rear of the fixed slide is attached to a separate L-shaped bracket with two screws and nuts. The bracket is attached to the cabinet with two screws that are secured with captive nuts.

Lift the memory frame and slide it carefully into the fixed guides until the slide release engages. Unlock the slide release and push the memory frame fully into the cabinet. Extend the memory frame enough to allow access to the front mounting screws. Slightly loosen the front and rear slide mounting screws and slide the memory frame back and forth. This allows the slides to assume a position that results in minimum binding. Retighten the mounting screws.

Cable Retractor – The cable retractor rod (DEC Part No. 12-12173-00) prevents the main memory bus cables from tangling when memory frames are extended from the cabinet. Install the cable retractor rod at the holes indicated in Figure 3-15.

AC Power Connection – Plug the memory frame power cord into one of the switched outlets of the cabinet power controller.

NOTE

The load at the power controller outlets must be distributed among the three phases. No other device should be plugged into a power controller phase circuit loaded by two memory frames. Refer to Drawing E-AR-11/70-0-1 and Figure 3-16.

3.5.1 MJ11 Memory Configuration

Whenever memory capacity is expanded, the following guidelines must be adhered to:

1. Before installing memory controller modules (M8147/M8148, and M8149), ensure that the switches on the M8147/M8148 module are properly configured.

2. Lower addresses must be implemented in memory frames electrically closest to the bus master.

3. All interleaved memory frames must be closer to the bus master than non-interleaved memory frames.

4. When memory frames are interleaved, they must be physically and electrically adjacent, with the memory frame containing "even" addresses closer to the bus master.

5. Care should be taken that modules are installed in their designated slots, as indicated in the module utilization sticker (Figure 3-17).

6. When memory capacity is increased within a memory frame, stack module set pairs are installed at the left and right-hand side of the backplane, working toward the center. Thus the stack three (high and low word) modules are the last module sets added to a memory frame.

7. Record the serial number of the module group just installed in the appropriate slot on the module utilization sticker.

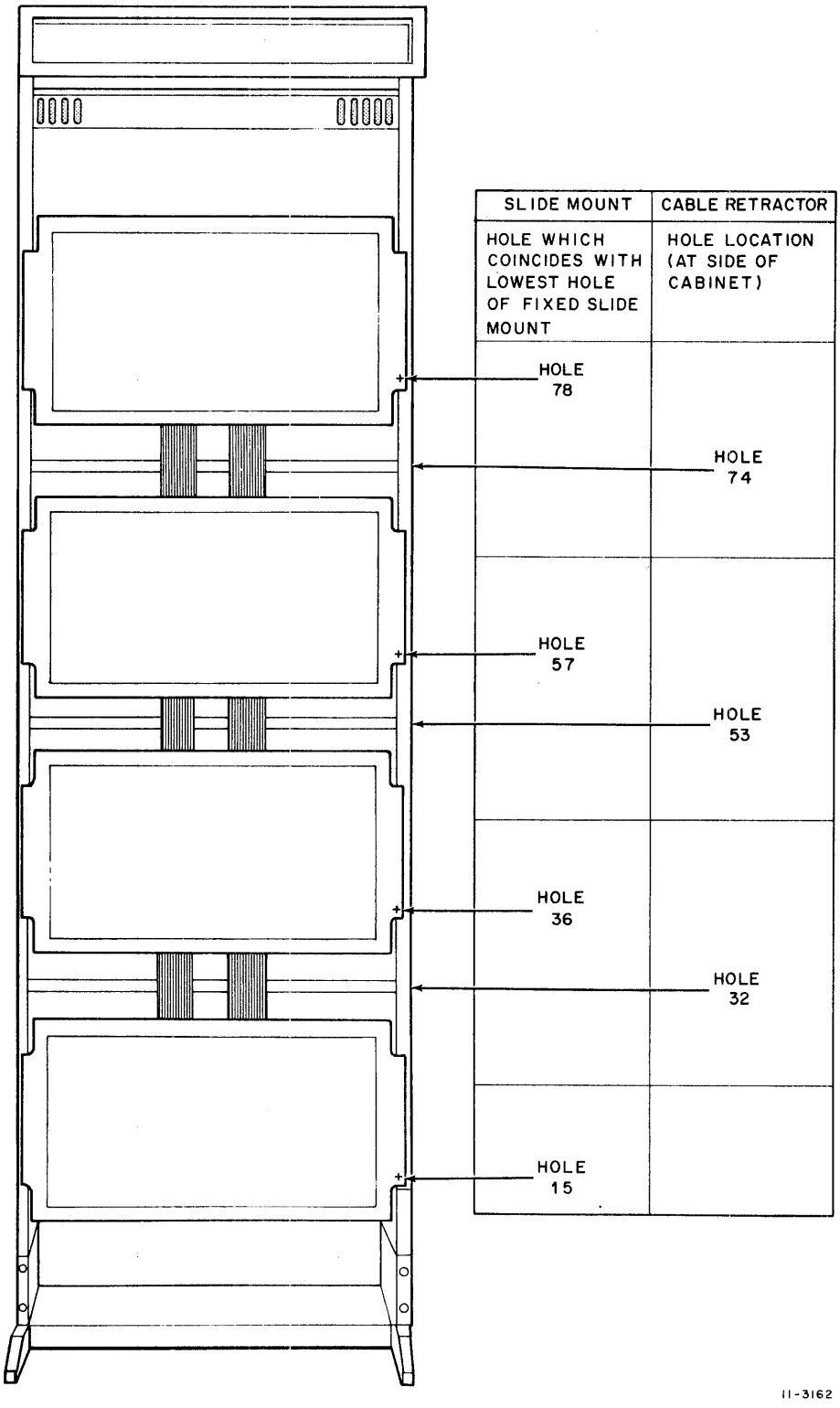


Figure 3-15 MJ11 Memory Frame and Cable Retractor Mounting

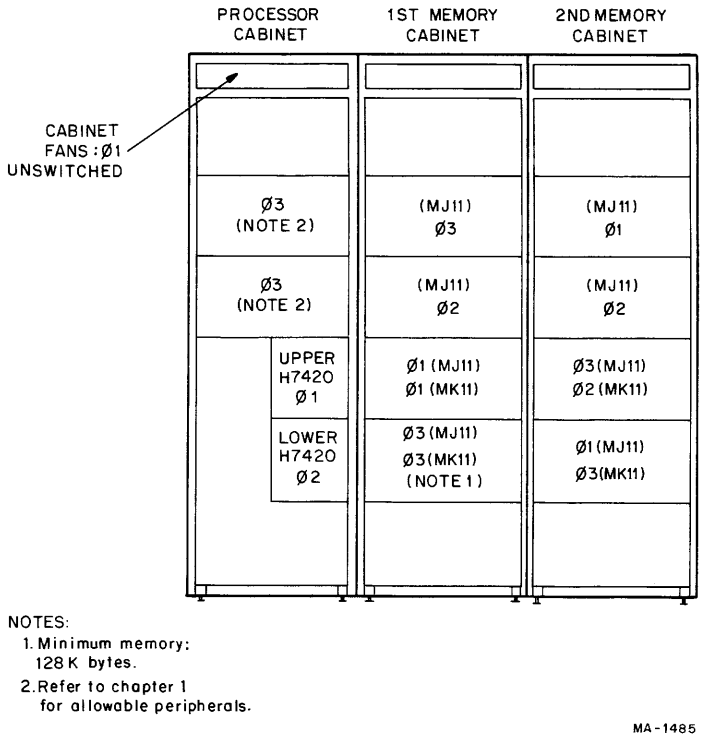


Figure 3-16 Phasing of Memory Frames

Starting Address Switch Configuration – Switches S1-1 through S1-7, S2-1, and S2-2 on the M8147/M8148 module (drawing MCTB and MCTJ) must be configured to represent the starting address of the memory controller. This is done by setting the switches to the binary number which represents the total number of 16K blocks of 36-bit double words controlled by memory controllers having lower starting addresses.

A closed switch (set to ON) represents a logic 0. Switch S1-1 represents the LSB and switch S2-2 the MSB.

The steps required to determine the starting address switch settings are shown in Figure 3-18 in flow-chart form. For example:

In an MJ11 Memory System, any two adjacent memory frames containing equal amounts of memory can be interleaved. If interleaving is desired, switch S2-3 on the M8147/M8148 modules (drawing MCTB) in both memory frames must be open (OFF). By convention, the memory controller located closer (electrically) to the bus master is required to respond to "even" addresses. Switch S2-4 in this controller must be closed (ON); switch S2-4 in the memory controller, which is farther from the bus master, should be open (OFF).

Switch Configuration Example – In a memory system consisting of three memory frames, assume that the first two frames (0 and 1) contain 128K of 18-bit words (i.e., 64K 36-bit blocks each, and that memory frame contains 32K 18-bit words (i.e., 16K 36-bit blocks). If memory frames 0 and 1 are interleaved, the memory frames are configured as follows:

Memory Frame 0 – Since no words precede this frame, 0 divided by 16K = 0 is set into switches S1-1:S2-2 (i.e., all nine switches are set to ON). Switch S2-3 is set for interleaved operation (OFF) and switch S2-4 is set for even addresses (ON).

mj11 memory system

CONTROLLER STARTING ADDRESS (OCTAL) _ _ _ _ _ _ _ _ _ _00000

INTERLEAVED ☐ YES ☐ NO | ☐ EVEN ☐ ODD

MEMORY SYSTEM SERIAL NO. | DATE INSTALLED

SLOT	MODULE TYPE		MODULE GROUP SER. NO.	MODULE (GROUP) FUNCTION
01	G114	SIN		STACK 0 HIGH WORD
02	H217C	STK		
03	G235	DRV		
04	G114	SIN		STACK 1 HIGH WORD
05	H217C	STK		
06	G235	DRV		
07	G114	SIN		STACK 2 HIGH WORD
08	H217C	STK		
09	G235	DRV		
10	G114	SIN		STACK 3 HIGH WORD
11	H217C	STK		
12	G235	DRV		
13	M8148	MCT		MEMORY CONTROL & TIMING
14	M8149	MXR		MEMORY TRANSCEIVER
15	G114	SIN		STACK 3 LOW WORD
16	H217C	STK		
17	G235	DRV		
18	G114	SIN		STACK 2 LOW WORD
19	H217C	STK		
20	G235	DRV		
21	G114	SIN		STACK 1 LOW WORD
22	H217C	STK		
23	G235	DRV		
24	G114	SIN		STACK 0 LOW WORD
25	H217C	STK		
26	G235	DRV		

MJ11-A

mj11 memory system

CONTROLLER STARTING ADDRESS (OCTAL) _ _ _ _ _ _ _ _ _ _00000

INTERLEAVED ☐ YES ☐ NO | ☐ EVEN ☐ ODD

MEMORY SYSTEM SERIAL NO. | DATE INSTALLED

SLOT	MODULE TYPE		MODULE GROUP SER. NO.	MODULE (GROUP) FUNCTION
01	G116	SIN		STACK 0 HIGH/ODD WORD
02	H224C	STK		
03	G236	DRV		
04	G116	SIN		STACK 1 HIGH/ODD WORD
05	H224C	STK		
06	G236	DRV		
07	G116	SIN		STACK 2 HIGH/ODD WORD
08	H224C	STK		
09	G236	DRV		
10	G116	SIN		STACK 3 HIGH/ODD WORD
11	H224C	STK		
12	G236	DRV		
13	M8147	MCT		MEMORY CONTROL & TIMING
14	M8149	MXR		MEMORY TRANSCEIVER
15	G116	SIN		STACK 3 LOW/EVEN WORD
16	H224C	STK		
17	G236	DRV		
18	G116	SIN		STACK 2 LOW/EVEN WORD
19	H224C	STK		
20	G236	DRV		
21	G116	SIN		STACK 1 LOW/EVEN WORD
22	H224C	STK		
23	G236	DRV		
24	G116	SIN		STACK 0 LOW/EVEN WORD
25	H224C	STK		
26	G236	DRV		

MJ11-B

11-3287

Figure 3-17 Module Utilization Labels

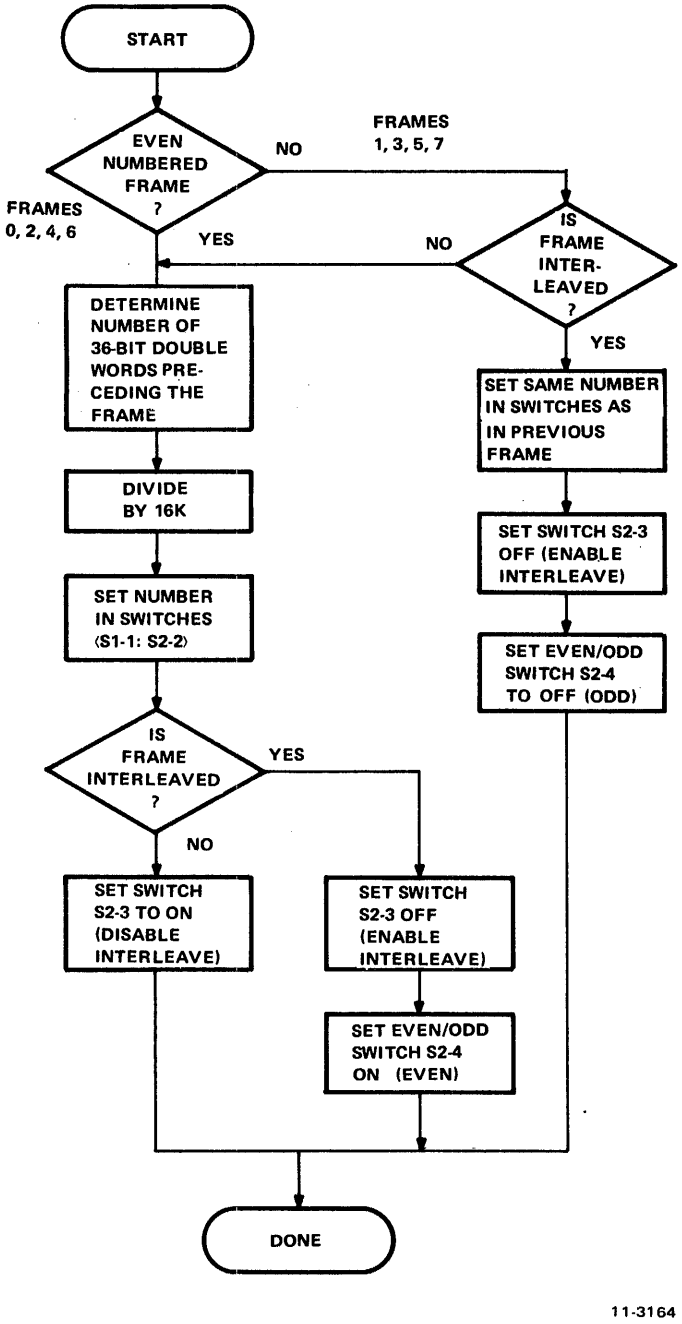


Figure 3-18 Procedure for Configuring M8147 (or M8148) Switches

Memory Frame 1 – Since this frame is interleaved, the starting address switches are configured as in memory frame 0. Switch S2-3 is set for interleaved operation (OFF) and switch S2-4 is set for odd addresses (OFF).

Memory Frame 2 – Since frames 0 and 1 contain a total of 128K 36-bit blocks, 128K divided by 16K = 8(10) = 10(8) = 000001000(2) is set into switches S1-2:S2-2 (i.e., S1-4 is set to OFF while the remaining switches are set ON). Switch S2-3 is set to ON to disable interleaving. With interleaving disabled, the state of switch S2-4 is irrelevant.

3.5.2 Main Memory Bus Cabling

1. Remove the M8147/M8148 and M8149 module comprising the last memory controller on the main memory bus.

2. Remove the H873 bus terminator from J2 and J4 on each module.

3. Install address cable assembly 7010824-1 in connectors J2 and J4 of the M8147/M8148 module.

4. Install the data cable assembly 7010824-0 in connectors J2 and J4 of the M8149 module.

5. Replace the modules in their proper backplane slots.

6. Route the main memory bus cables as shown in Figures 3-19 and 3-20. Ensure that the cables do not obstruct the air vents at the rear of the memory frame. Connect the cables to J1 and J3 on the M8147/M8148 and M8149 modules of the memory frame being installed.

7. Insert the main memory bus terminators in connectors J2 and J4 of the M8147/M8148 and M8149 modules, which are last on the main memory bus.

8. Install the modules in their proper backplane slots.

9. Secure the bus cables by tightening the cable clamps.

3.5.3 Voltage Checks

After installation has been completed, check regulator voltage outputs in all the memory frames (Table 3-2). Perform voltage adjustments (Paragraph 4.5.2.2) if necessary.

3.5.4 Memory Expansion in the PDP-11/70

Prior to installation verification, the PDP-11/70 System Size register must be reconfigured to represent the new memory size. Refer to drawing D-CS-M8140-0-1, sheet SCCN in the PDP-11/70 Engineering Drawings and to Figure 3-21.

3.5.5 Checkout

Run diagnostics as listed in Figure 3-9.

3.6 MK11 MEMORY EXPANSION

The MK11 memory frame is similar to the MJ11 memory frame. They are shipped in the same type of protective box (Figure 3-14) and have the same type of slide rail mounting brackets (Paragraph 3.5). Both memory frames are mounted in the memory cabinet in the same manner. In addition to installing the memory frame, the box controller and the three battery backup units must also be installed in the cabinet and cabled to the memory frame.

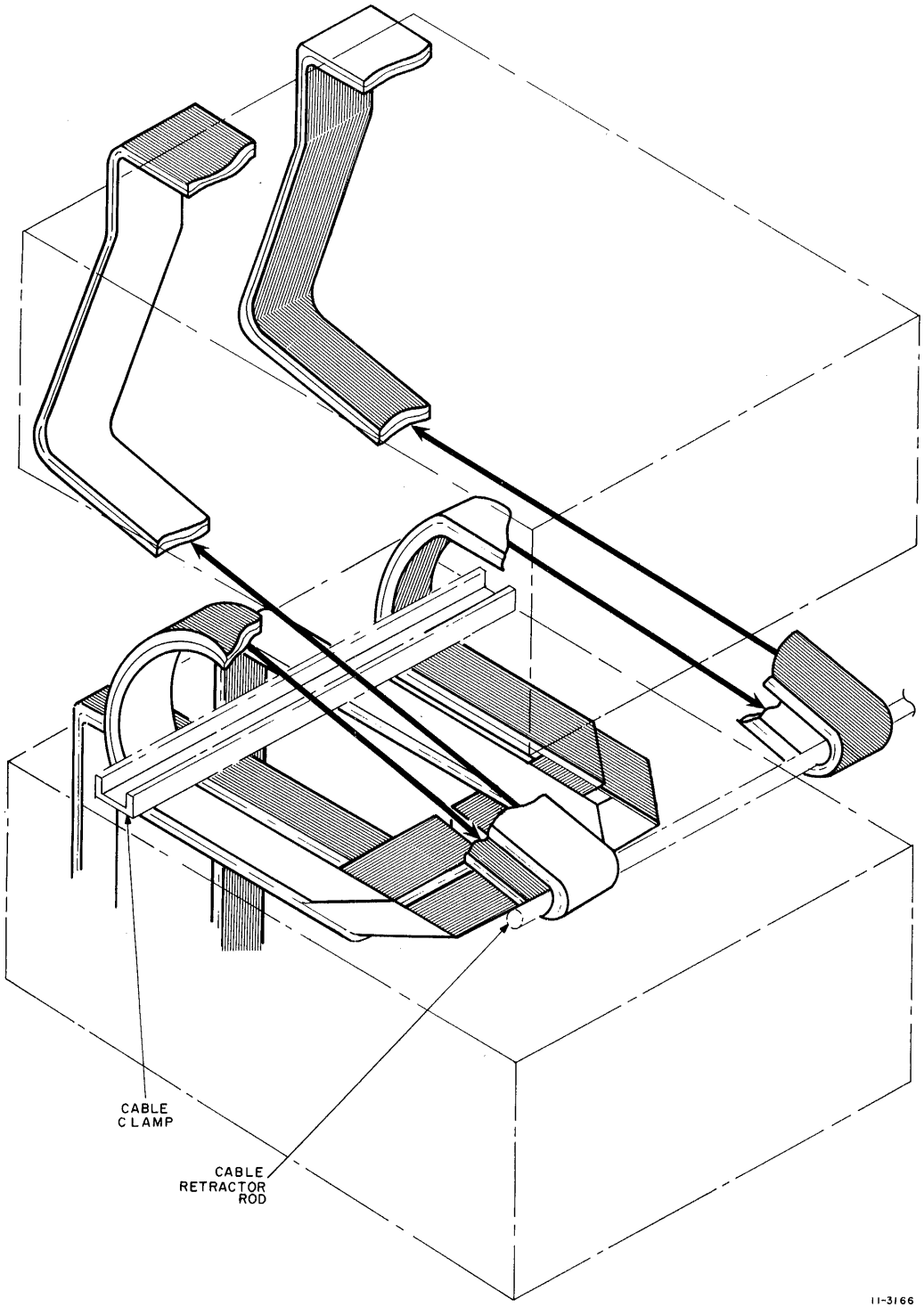


Figure 3-19 Typical MJ11 Cable Routing

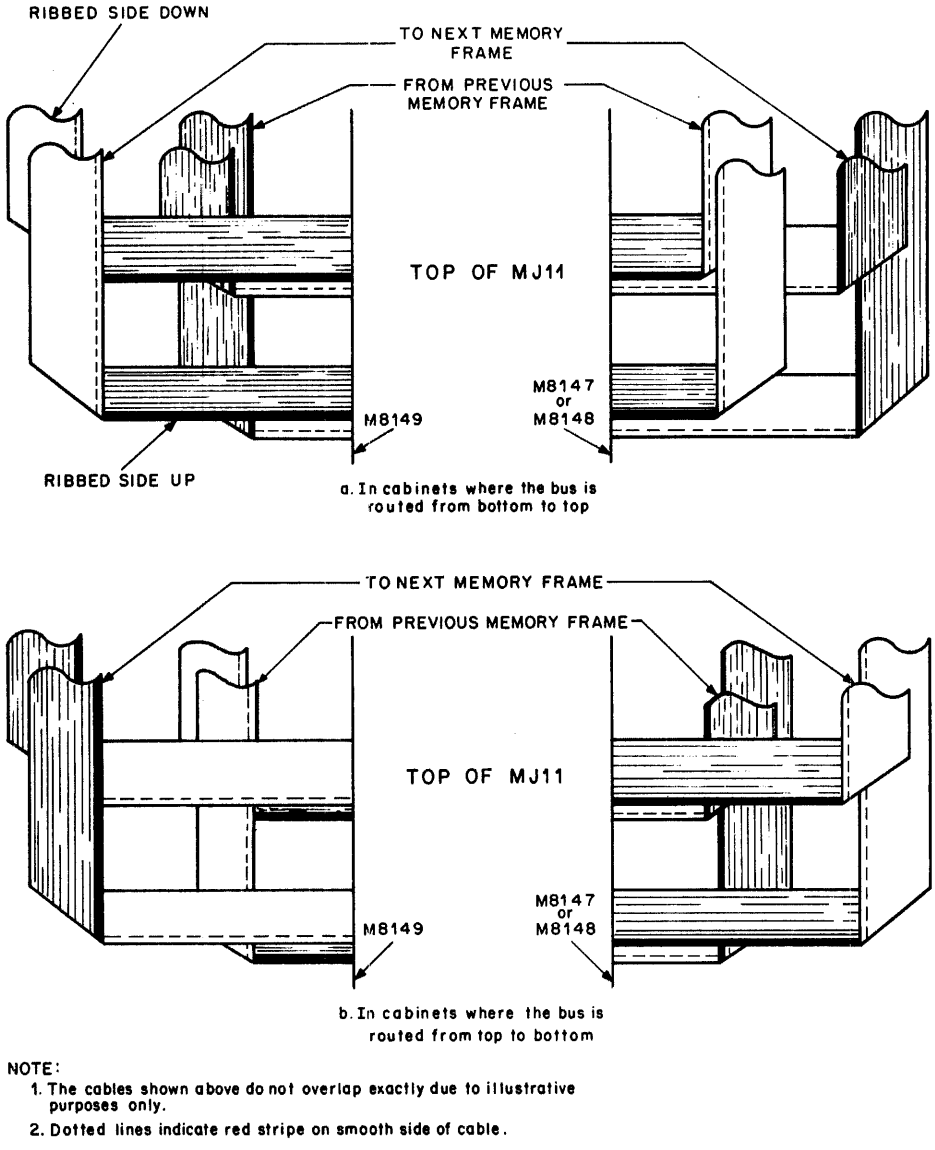
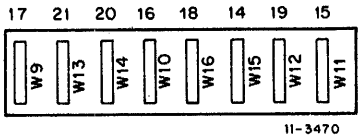


Figure 3-20 MJ11 Main Memory Bus Cable Routing



X = ON
– = OFF

Memory Size	Last Address	Switch Settings W9	W13	W14	W10	W16	W15	W12	W11
32K	00177776	X	X	X	X	X	X	—	—
64K	00377776	X	X	X	—	X	X	—	—
96K	00577776	—	X	X	X	X	X	—	—
128K	00777776	—	X	X	—	X	X	—	—
160K	01177776	X	X	X	X	—	X	—	—
192K	01377776	X	X	X	—	—	X	—	—
224K	01577776	—	X	X	X	—	X	—	—
256K	01777776	—	X	X	—	—	X	—	—
288K	02177776	X	X	X	X	X	—	—	—
320K	02377776	X	X	X	—	X	—	—	—
352K	02577776	—	X	X	X	X	—	—	—
384K	02777776	—	X	X	—	X	—	—	—
416K	03177776	X	X	X	X	—	—	—	—
448K	03377776	X	X	X	—	—	—	—	—
480K	03577776	—	X	X	X	—	—	—	—
512K	03777776	—	X	X	—	—	—	—	—
544K	04177776	X	X	—	X	X	X	—	—
576K	04377776	X	X	—	—	X	X	—	—
608K	04577776	—	X	—	X	X	X	—	—
640K	04777776	—	X	—	—	X	X	—	—
672K	05177776	X	X	—	X	—	X	—	—
704K	05377776	X	X	—	—	—	X	—	—
736K	05577776	—	X	—	X	—	X	—	—
768K	05777776	—	X	—	—	—	X	—	—
800K	06177776	X	X	—	X	X	—	—	—
832K	06377776	X	X	—	—	X	—	—	—
864K	06577776	—	X	—	X	X	—	—	—
896K	06777776	—	X	—	—	X	—	—	—
928K	07177776	X	X	—	X	—	—	—	—
960K	07377776	X	X	—	—	—	—	—	—
992K	07577776	—	X	—	X	—	—	—	—
1024K	07777776	—	X	—	—	—	—	—	—

Figure 3-21 System Size Register Switches (Sheet 1 of 2)
(refer to D-CS-M8148-0-1, Sheet 1, for Location of Switch Assembly)

X = ON
-- = OFF

Memory Size	Last Address	Switch Settings W9	W13	W14	W10	W16	W15	W12	W11
1032K	10177776	X	—	X	X	X	—	X	—
1064K	10377776	X	—	X	—	X	—	X	—
1096K	10577776	—	—	X	X	X	—	X	—
1128K	10777776	—	—	X	—	X	—	X	—
1160K	11177776	X	—	X	X	—	—	X	—
1192K	11377776	X	—	X	—	—	—	X	—
1224K	11577776	—	—	X	X	—	—	X	—
1256K	11777776	—	—	X	—	—	—	X	—
1288K	12177776	X	—	X	X	X	—	—	—
1320K	12377776	X	—	X	—	X	—	—	—
1352K	12577776	—	—	X	X	X	—	—	—
1384K	12777776	—	—	X	—	X	—	—	—
1416K	13177776	X	—	X	X	—	—	—	—
1448K	13377776	X	—	X	—	—	—	—	—
1480K	13577776	—	—	X	X	—	—	—	—
1512K	13777776	—	—	X	—	—	—	—	—
1544K	14177776	X	—	—	X	X	—	X	—
1576K	14377776	X	—	—	—	X	—	X	—
1608K	14577776	—	—	—	X	X	—	X	—
1640K	14777776	—	—	—	—	X	—	X	—
1672K	15177776	X	—	—	X	—	—	X	—
1704K	15377776	X	—	—	—	—	—	X	—
1736K	15577776	—	—	—	X	—	—	X	—
1768K	15777776	—	—	—	—	—	—	X	—
1800K	16177776	X	—	—	X	X	—	—	—
1832K	16377776	X	—	—	—	X	—	—	—
1864K	16577776	—	—	—	X	X	—	—	—
1896K	16777776	—	—	—	—	X	—	—	—
1928K	17177776	X	—	—	X	—	—	—	—
1960K	17377776	X	—	—	—	—	—	—	—
1992K	17577776	—	—	—	X	—	—	—	—
2048K	17777776	—	—	—	—	—	—	—	—

Figure 3-21 System Size Register Switches (Sheet 2 of 2)
(Refer to D-CS-M8148-0-1, Sheet 1, for Location of Switch Assembly)

Cable placement is critical in the memory cabinet. The cables will be damaged if the following procedure is not followed carefully. The following steps refer specifically to adding memory box no. 1 to the first memory cabinet. The procedure for installing expansion box no. 3 to the second memory cabinet is similar and can be generalized from the steps given in this section if the following guidelines are observed.

- Cable from lower numbered memory box to higher numbered box. Take up excess cable slack inside of higher numbered memory box.
- Keep smooth side up on incoming ribbon cables. Keep ribbed side up on outgoing ribbon cables.
- Memory boxes no. 0 and no. 2 have their incoming cables on the left-hand side of box. Memory boxes no. 1 and no. 3 have their incoming cables on the right.

Prior to installation, check contents of shipment against packing list, unpack containers, and inspect for obvious shipping damage. Remove the memory cabinet's front and rear doors.

Configure the power fail jumpers on the address buffer module (M8158) as shown in Table 3-4. This will allow any memory to be switched off-line and powered down without affecting the other memories or the processor.

The CSR address select switches must select the address corresponding to the memory's unit number. Consult Table 3-5 for the proper CSR address and set the switches on the address interface module. Apply unit number decal to memory box.

1. Extend memory box no. 0 from the cabinet. Remove the top cover and remove the strain relief bar. Remove address interface and data buffer modules (slots 13 and 15). Remove screws and unplug memory bus terminators from J2 and J4; see Figure 3-22 for their loca tion. Configure power fail jumpers as in Table 3-4. Plug in address and data bus cables, keeping ribbed side up and red stripe to left on component side of board. Replace address and data buffer modules.

2. Fold outgoing bus cables. Lay cables, ribbed side up, on right-hand side of memory box. Replace the strain relief bracket keeping cables between retaining screws. Flatten outgoing cables and pull them toward rear of box to take up any slack inside the box. Tighten strain relief bracket. Tie wrap outgoing cables to power supply assembly.

3. Tilt memory box no. 0 to the 90 degree service position. Align cables so they extend straight back into the cabinet, parallel to the slide rails. Tie wrap cables to front cable retractor bar as shown in Figure 3-28, taking up slack in cables between memory box and retractor. Route bus cables over cable retractor and into cabinet. Use tape to tie wrap the four cables together between memory box and front cable retractor. Place floating restraint under cables midway between memory box and cable retractor and tie wrap to cables.

4. Tilt memory box no. 0 to its level position and replace top cover. Slide box no. 0 into cabinet, guiding cables by hand if necessary.

5. Mount memory box no. 1 in cabinet, position slide rails at height indicated in Figure 3-23.

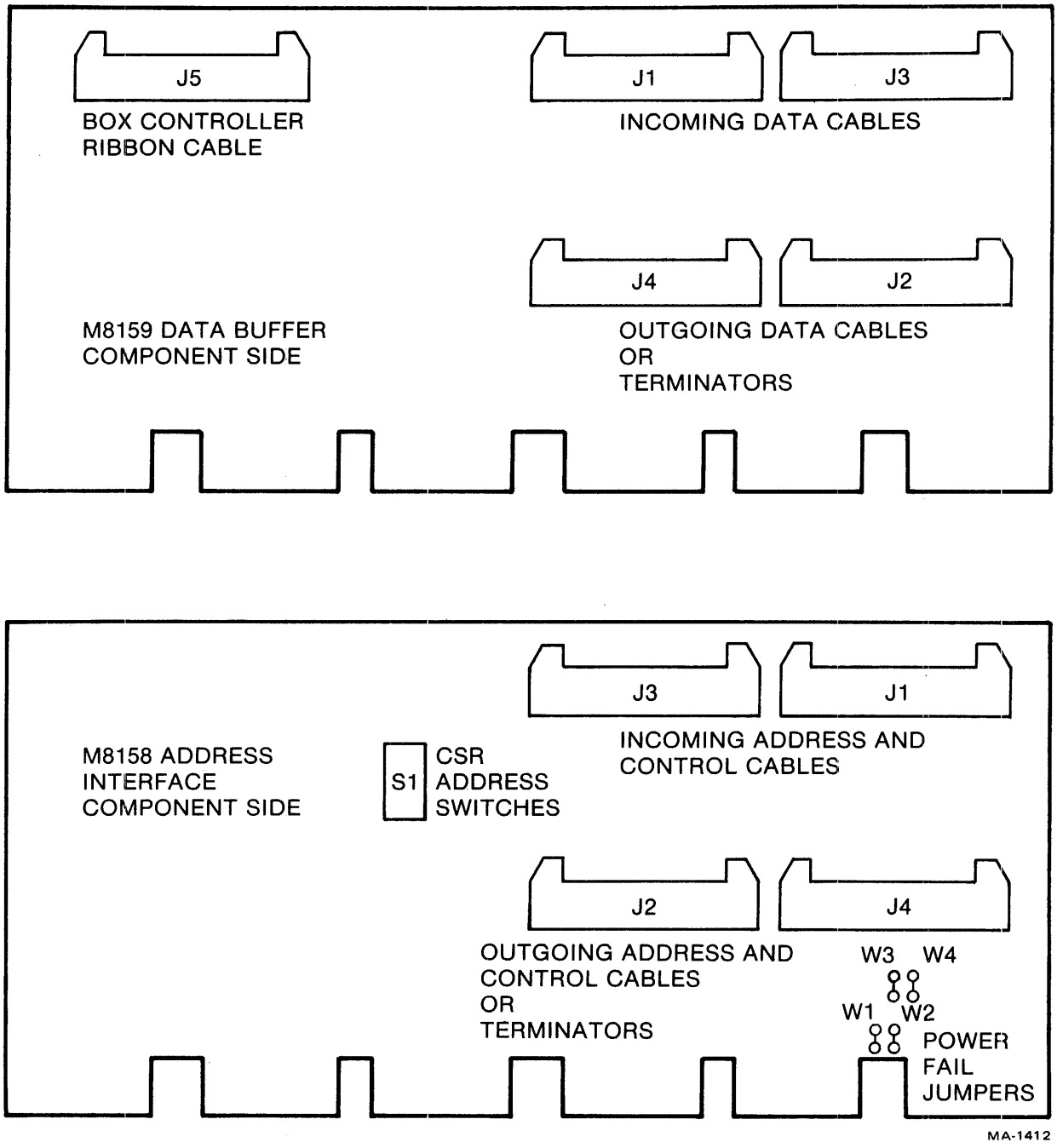


Figure 3-22 Address and Data Buffer Plug Locator

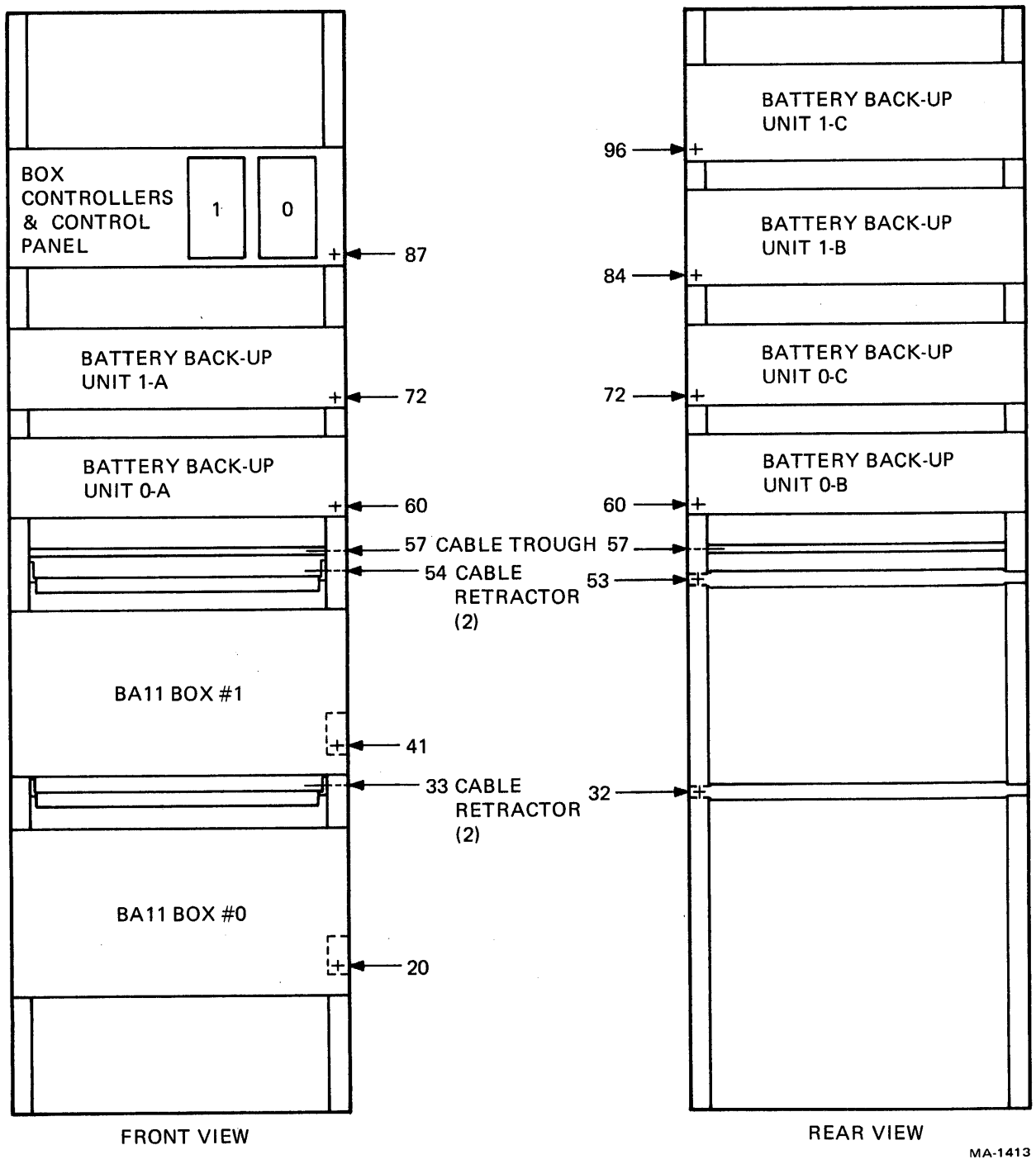


Figure 3-23 MK11 Memory Cabinet Configuration

6. Route power cables (Figure 3-24). Tilt box no. 1 to the 90 degree service position. Plug in battery backup and box controller power cables and tie wrap to power supply chassis. Overlap the two power cables on left side of box and tie wrap them to the front cable retractor, taking up any slack and keeping the cables parallel to the slide rails. Route cables straight back through the cabinet, under and around the rear cable retractor bar. Tie wrap power cables to cable retractor. On right side of box, route and tie wrap power and controller cables in the same fashion. Tie wrap cable bundles every six inches. Use tape to tie wrap cables between memory box and front cable retractor.

7. Install battery backup units 1B and 1C in the rear of the cabinet at the heights shown in Figure 3-23. Plug power cables into battery backup units. Take up slack in cables by tie wrapping loops into the cables as shown in Figure 3-25

8. Remove blank control panel cover. Pull controller power cable through cutout on top of control panel and out through front of panel. Plug cable into box controller and mount controller in control panel. Install battery backup unit 1A in cabinet and plug in power cable. Tie wrap loops into cables to take up slack as shown in Figure 3-26.

9. Return memory box no. 1 to level position. Remove top cover and strain relief bar. Lay the four incoming bus cables, from box no. 0, on the right-hand side of box, keeping smooth side of cables up. Replace strain relief bar (do not tighten) and position cables just to the left of the retaining screw. Pull bus cables forward under strain relief taking up enough slack in cables to allow service loop (Figures 3-27 and 3-28). Cables should be tight when memory box is pushed back into cabinet. If box is pushed into cabinet to check length of service loop, push box carefully and guide cables by hand to avoid damage to cables.

10. Remove data buffer and address buffer modules. Configure power fail jumpers and CSR address switches as two indicated in Tables 3-4 and 3-5. Plug terminators and secure with two screws and connect bus cables into modules as in Figure 3-22. Keep red stripe to left on component side of modules. Replace address and data buffer modules. Fold incoming bus cables to take up slack inside of memory box. Tie wrap incoming bus cables every six inches.

11. Plug box controller ribbon cable into data buffer board, fold, and lay on top of incoming bus cables, keeping smooth side up. Lift strain relief bar and slide cable under bar, position cable on top of bus cables (do not alter position of incoming bus cables). Flatten controller cable to remove slack and tighten strain relief bar. Replace top cover and tilt box to the 90 degree service position.

12. Route controller ribbon cable over front cable retractor bar then under and around rear cable retractor (Figure 3-26). Take up slack in cable and tie wrap to cable retractors as shown. Keep cable path parallel to slide rails. Bring cable across to front of cabinet and plug into box controller as in Figure 3-27. Plug cable in with smooth side of cable up on bracket behind controller. Take up slack in cable with folds and tie wrap to bottom of control panel. Install strain relief bracket behind controller panel. Tie wrap floating strain relief to cables mid-way between memory box and front retractor bar.

13. Return memory box to level position. Tie wrap power cord to rear cable retractor. Plug power cord into receptacle. Attach memory unit number decal corresponding to CSR address to memory box. Push memory box into cabinet, guiding cables by hand if necessary.

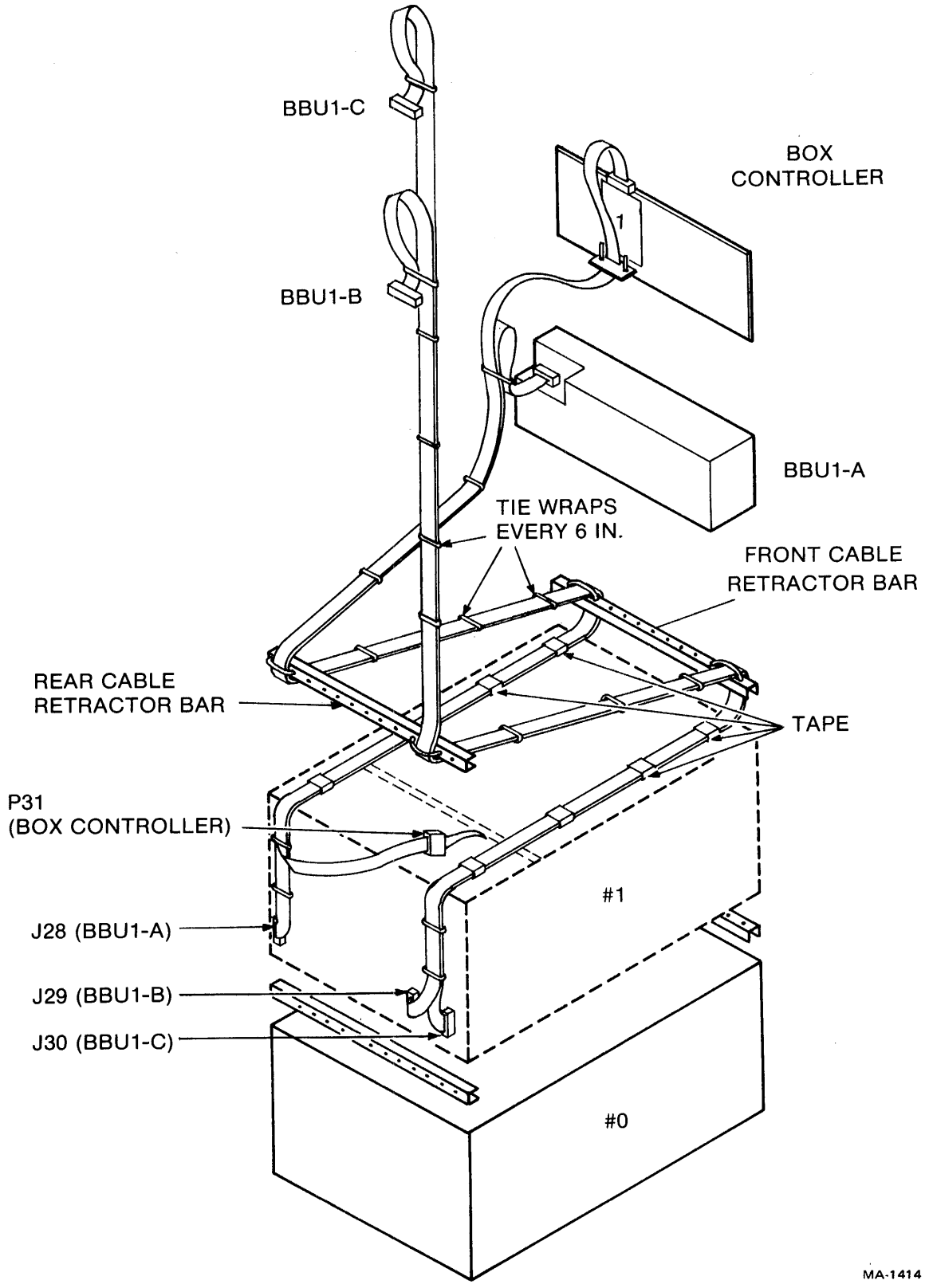


Figure 3-24 Box Controller and Battery Backup Power Cables

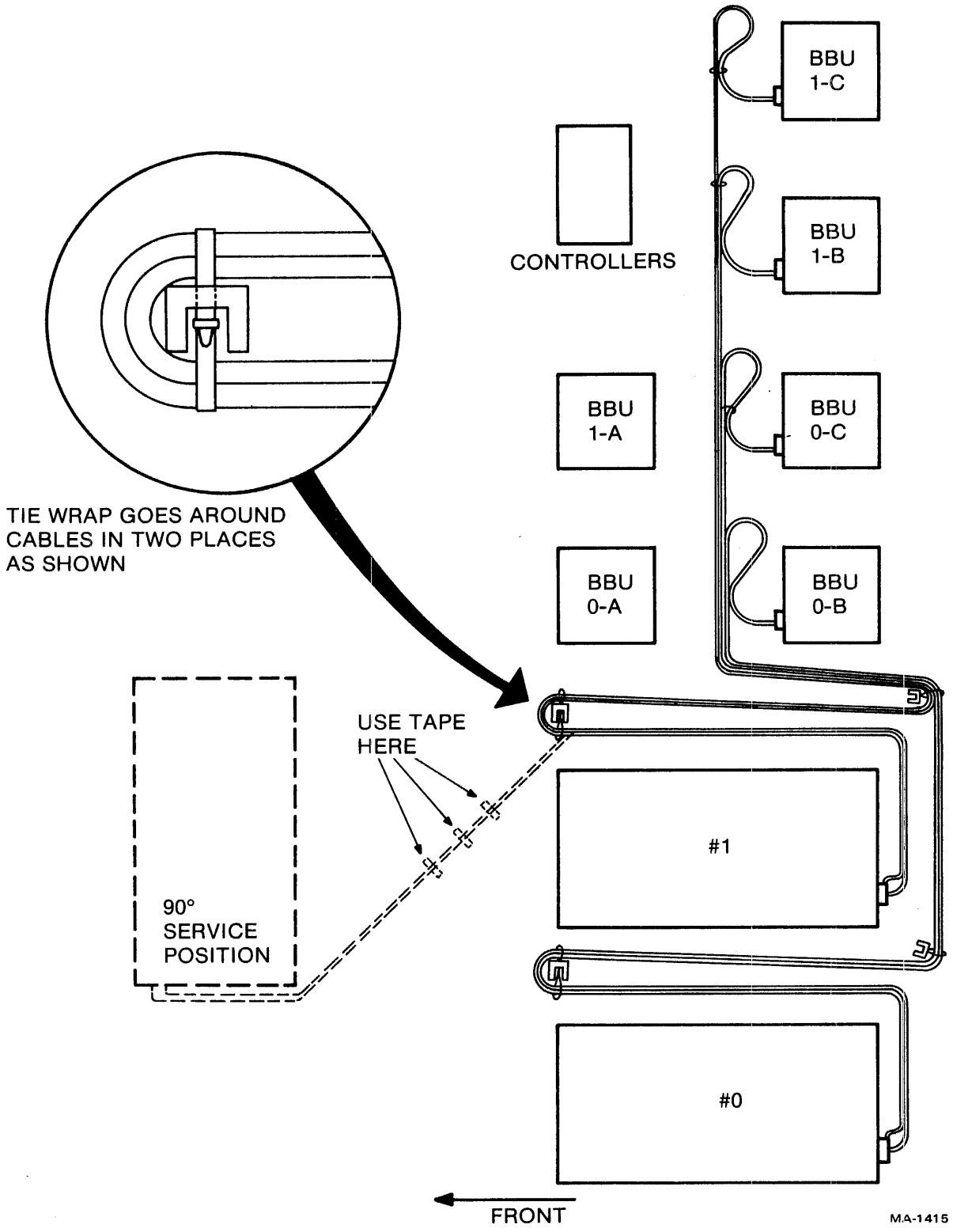


Figure 3-25 Battery Backup Power Cable Routing, First Memory Cabinet

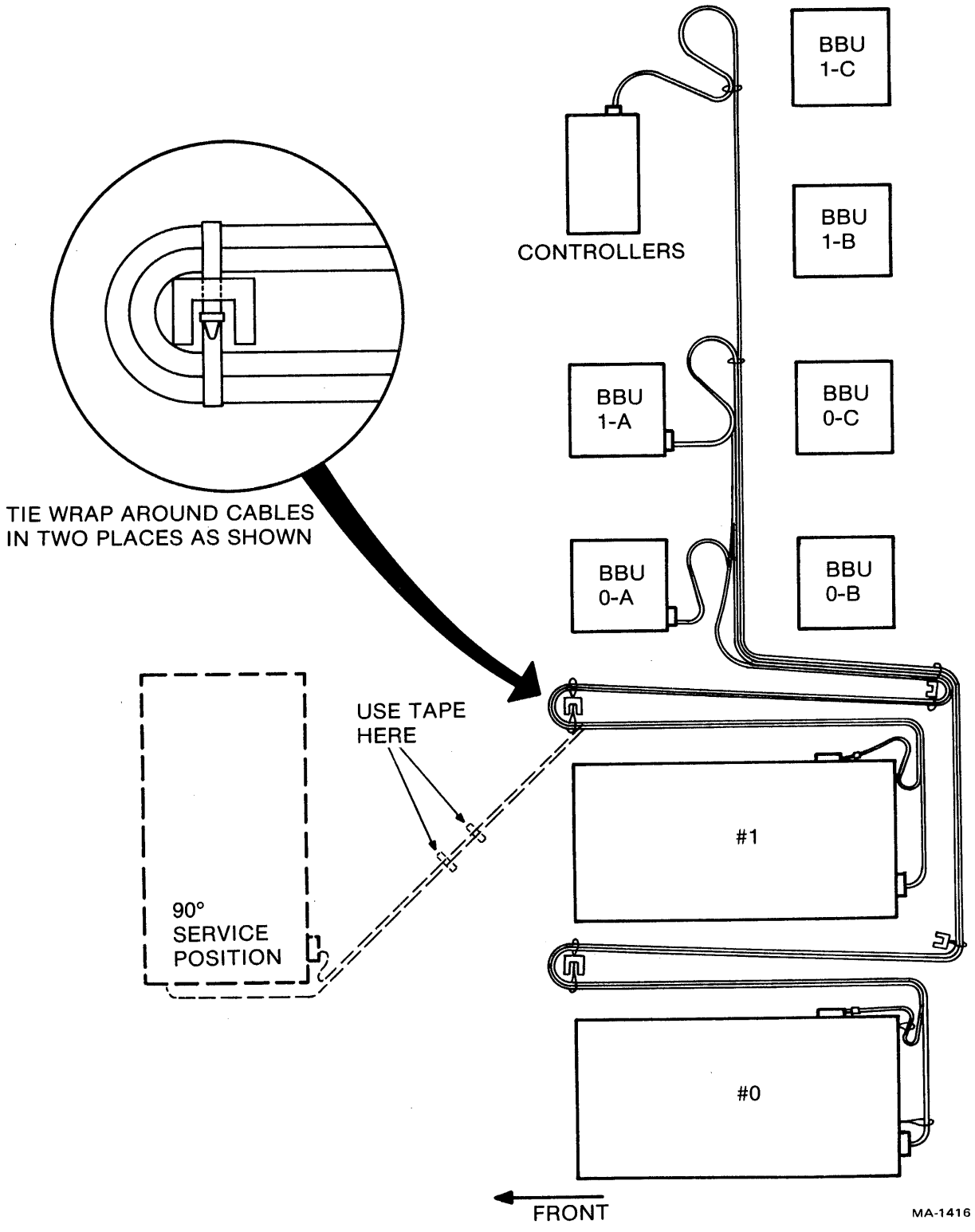


Figure 3-26 Box Controller and Battery Backup Cable Routing

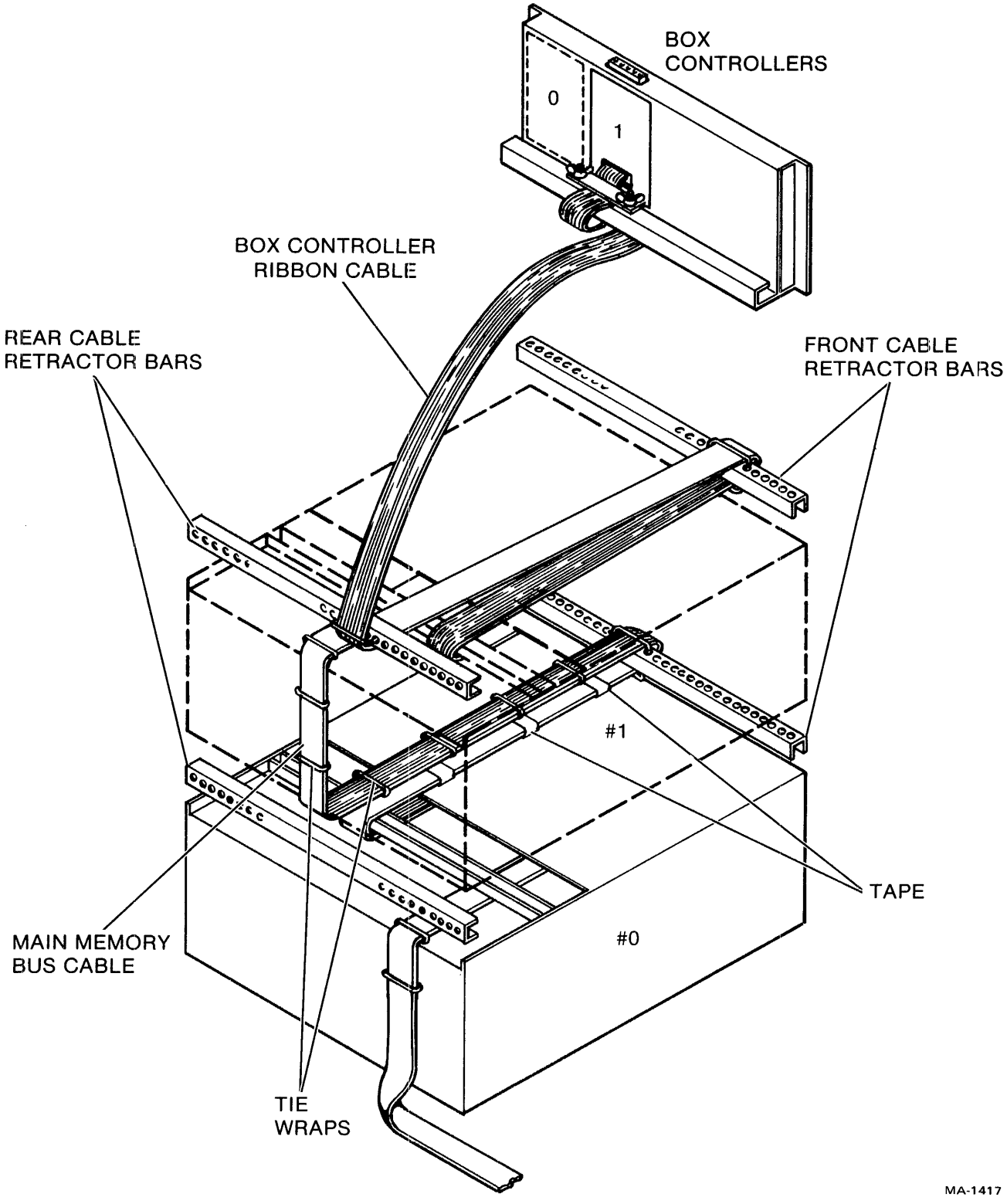


Figure 3-27 Main Memory Bus and Box Controller Cables

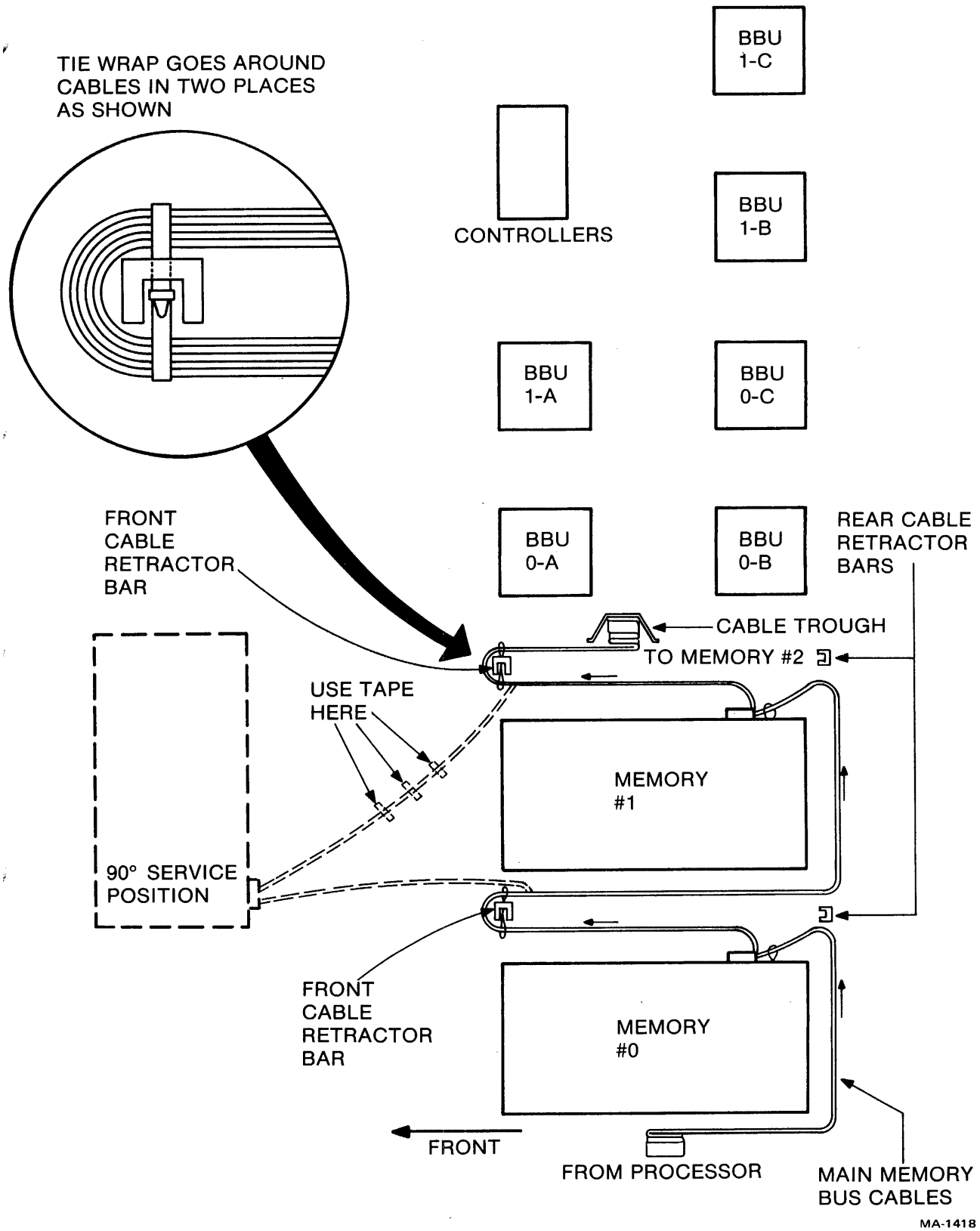


Figure 3-28 Main Memory Bus Cable Routing, First Memory Cabinet

Table 3-4 Power Fail Jumpers

Memory	W1	W2	W3	W4
Last Memory Box on Bus	Out	In	Out	In
All Other Memory Boxes	In	Out	In	Out

Table 3-5 CSR Address Selection

Unit Number	CSR Address	Switch Position		
		S1-3	S1-2	S1-1
0	X772100	Closed	Closed	Closed
1	X772104	Closed	Closed	Open
2	X772110	Closed	Open	Closed
3	X772114	Closed	Open	Open

X = 106 for direct addressing mode.
X = 17 for indirect addressing mode.

3.6.1 Memory Expansion Cabinet

Expansion memory cabinets are shipped with the memory box, battery backup units, and the box controller installed and cabled. The second memory cabinet is installed immediately to the right of the first memory cabinet. At most sites, this requires repositioning the tape or disk drive cabinet since these cabinets are positioned to the right of the memory cabinet(s).

Prior to installation, check contents of shipment against packing list and inspect for obvious shipping damage.

1. Remove shipping container and polyethylene covers from cabinet. Remove tape, plastic shipping pins and securing bolts from cabinet. Remove side panel from right side of first memory cabinet.

2. Raise leveling feet so that cabinet rests on its casters. Roll cabinet onto floor using suitable ramp. Push cabinet into position along side the first memory cabinet.

3. Install filler strips between memory cabinets. Lower leveling feet to align height of second memory cabinet to first memory cabinet. Tighten bolts securing cabinets together. Install ground strapping between cabinets. Remove shipping bracket from memory box.

4. Install memory bus cable trough at height indicated in Figure 3-23.

5. Extend memory box no. 1 to service position. Remove top cover. Remove strain relief bracket. Remove address buffer and data buffer modules. Note cable positions, do not alter folds in ribbon cables. Configure power fail jumpers per Table 3-4. Remove screws and unplug memory bus terminators. Connect main memory bus cables to modules keeping ribbed side up and red stripe to left on component side of board. Replace address interface and data buffer modules.

6. Fold outgoing bus cables, keeping ribbed side up and lay them on left side of memory box just to the right of strain relief bracket retaining screw. Return incoming cables to original position. Replace strain relief bracket, do not tighten. Pull outgoing cables backward to take slack out of memory box. Tighten strain relief bracket.

7. Replace top cover. Tilt memory box no. 1 to 90 degree service position. Tie wrap outgoing bus cables to front cable retractor bar as shown, taking up slack between memory box and cable retractor. Keep path of cables parallel to slide rails. Wrap cables together with tape. Tilt memory box no. 1 back to level position and push memory box back into cabinet.

8. Extend memory box no. 2 to service position. Remove top cover. Remove strain relief bracket. Note position of controller ribbon cable.

9. Fold and route memory bus cables through cable trough into second memory cabinet as shown in Figure 3-29. Exit cables with smooth side up through front of second memory cabinet on top of front cable retractor bar. Lay cables on left side of memory box just to the right of retaining screw. Straighten cables and tie wrap to front cable retractor bar.

10. Remove address buffer and data buffer modules. Configure power fail jumpers and CSR address select switches per Tables 3-4 and 3-5. Connect memory bus terminators and incoming bus cables. Replace address interface and data buffer modules. Replace strain relief bracket; do not tighten.

11. Tilt memory box no. 2 to the 90 degree service position. Pull upward on incoming bus cables to take up slack between front cable retractor and memory box. Ensure controller ribbon cable is returned to former position. Tighten strain relief bracket. Tape incoming cables together between cable retractor and memory box. Tie wrap cables to floating restraint.

12. Return memory box no. 2 to level position. Fold incoming cables to take up slack inside of memory box. Replace top cover.

13. Place unit number decal on memory box (Figure 3-30) to indicate CSR address as in Table 3-5. Plug in power cord. Verify cabling with diagrams.

3.6.2 MK11 Memory Configuration

Thumbwheel switches on the MK11 box controller select the starting address and the type of interleaving for the memory frame. The thumbwheel switches are eight position switches, labeled from zero through seven. The octal number displayed by the starting address switches represents the starting address of the memory frame in 32K word blocks (decimal). The interleave number selects the external interleaving between two or four memory frames. The control panel decal, Figure 3-31, summarizes the interleave switch settings and correlates the starting address switch settings to the starting address of the memory.

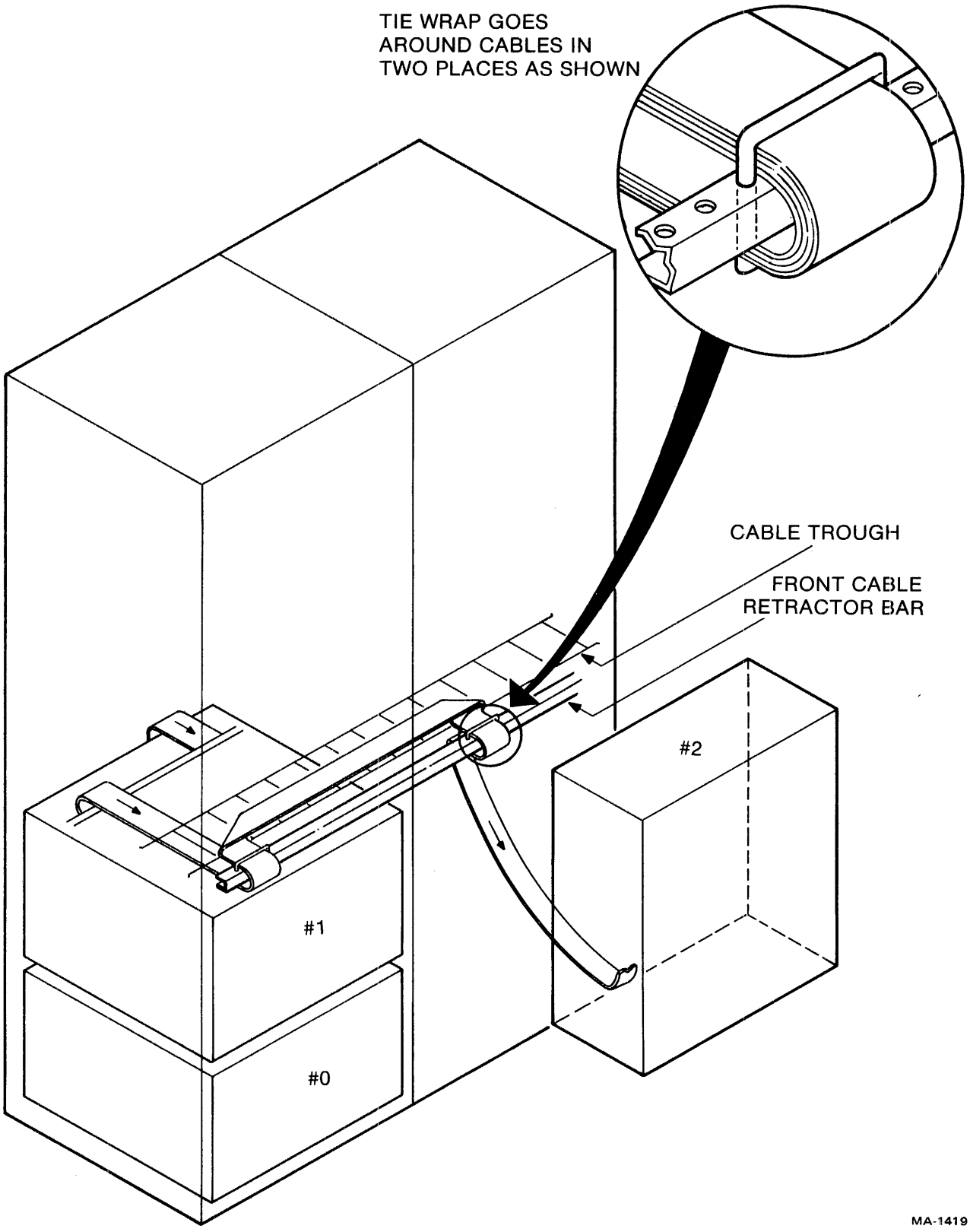


Figure 3-29 Main Memory Bus Cable Routing, Second Memory Cabinet

mk11 memory system

BOX STARTING ADDRESS (OCTAL) _____

CONTROL & STATUS REGISTER STARTING ADDRESS ☐ 1607721 ___ ☐ 177721 ___

INTERLEAVED ☐ EXT 2 WAY ☐ EXT 4 WAY | RESPONDS TO A∅2: _____ A∅3: _____

MEMORY SYSTEM SERIAL NO. _____ | DATE INSTALLED _____

SLOT	MODULE TYPE	MODULE GROUP SER. NO.	MODULE FUNCTION
01	NOT USED		
02	M7984 –		#14 STORAGE ARRAY
03	M7984 –		#12 STORAGE ARRAY
04	M7984 –		#10 STORAGE ARRAY
05	M7984 –		#8 STORAGE ARRAY
06	M7984 –		#6 STORAGE ARRAY
07	M7984 –		#4 STORAGE ARRAY
08	M7984 –		#2 STORAGE ARRAY
09	M7984 –		#0 STORAGE ARRAY
10	M8161		0 CONTROL B (DATA & ECC)
11	M8160		0 CONTROL A (TIMING & CONT.)
12	NOT USED		
13	M8158		ADDRESS BUFFER
14	NOT USED		
15	M8159		DATA BUFFER
16	M8160		1 CONTROL A (TIMING & CONT.)
17	M8161		1 CONTROL B (DATA & ECC)
18	M7984 –		#1 STORAGE ARRAY
19	M7984 –		#3 STORAGE ARRAY
20	M7984 –		#5 STORAGE ARRAY
21	M7984 –		#7 STORAGE ARRAY
22	M7984 –		#9 STORAGE ARRAY
23	M7984 –		#11 STORAGE ARRAY
24	M7984 –		#13 STORAGE ARRAY
25	M7984 –		#15 STORAGE ARRAY
26	NOT USED		

Figure 3-30 Memory Box Decal

BATTERY STATUS	
LED'S	FUNCTION
1. SLOW FLASH 2. ON 3. FAST FLASH 4. OFF	FAST CHARGE SLOW CHARGE DISCHARGE BATTERY OFF

INTERLEAVE
0 NO EXT INTERL 1 NOT USED 2 (2) WAY EXT INTERL BOX 0 3 (2) WAY EXT INTERL BOX 1 4 (4) WAY EXT INTERL BOX 0 5 (4) WAY EXT INTERL BOX 1 6 (4) WAY EXT INTERL BOX 2 7 (4) WAY EXT INTERL BOX 3

STARTING ADDRESS							
PANEL SET	K WORDS	PANEL SET	K WORDS	PANEL SET	K WORDS	PANEL SET	K WORDS
000	0	020	512	040	1024	060	1536
001	32	021	544	041	1056	061	1568
002	64	022	576	042	1088	062	1600
003	96	023	608	043	1120	063	1632
004	128	024	640	044	1152	064	1664
005	160	025	672	045	1184	065	1696
006	192	026	704	046	1216	066	1728
007	224	027	736	047	1248	067	1760
010	256	030	768	050	1280	070	1792
011	288	031	800	051	1312	071	1824
012	320	032	832	052	1344	072	1856
013	352	033	864	053	1376	073	1888
014	384	034	896	054	1408	074	1920
015	416	035	928	055	1440	075	1952
016	448	036	960	056	1472	076	1984
017	480	037	992	057	1504	077	2016

Figure 3-31 Control Panel Decal

Interleaving – Internal interleaving, between the right and left sides of the memory frame, is a function of the number and types of storage arrays installed in the memory. If both sides of the memory contain the same number of MS11-KE, MS11-KD, and MS11-KC arrays, then, at power up, the memory will be internally interleaved. If the memory frame is unbalanced, that is a different capacity or number of array modules on one side than the other, then the memory will not be internally interleaved. There is no way to force an unbalanced memory to be internally interleaved. Internal interleaving in a balanced memory, however, may be defeated. Consult the technical manual for the MK11 memory for defeating the internal interleaving.

External interleaving, between two memory frames or among four memory frames, is determined by the interleave switches on the box controllers. To interleave two memory frames (external two way), set the interleave switch on one box controller to 2, and the interleave switch on the second box controller to 3. The memory frame with its box controller interleave switch set to 2 responds to addresses with address bit A02 equal to zero. The memory frame with its box controller interleave switch set to 3 responds to addresses with address bit A02 equal to one.

Two memory frames may be two-way externally interleaved only if their capacities are equal. Also, both memory frames must have the same starting address.

Four memory frames may be four-way externally interleaved by using the interleave switch positions labeled 4, 5, 6, and 7. The switch settings and the addresses that the memory responds to are listed below.

	Interleave Switch Number	**Responds to Address Bits A03**	**A02**
Box 0	4	0	0
Box 1	5	0	1
Box 2	6	1	0
Box 3	7	1	1

In order to externally interleave the four memory frames, they must all have the same memory capacity. The same starting address must be selected for all four memory frames.

Interleave switch position 0 corresponds to no external interleaving. Use switch position 0 if there is only one MK11 memory frame in the system or if external interleaving among the boxes is not desired.

Interleave switch position 1 is not used.

Starting Address – Refer to the control panel decal shown in Figure 3-31. The decal correlates the octal starting address switch settings to the decimal starting addresses in 32K word blocks. The first memory frame in the system, box 0, will have its starting address switches set to 000. The starting address switch settings of the second memory frame, Box 1, are determined by the capacity of Box 0 (only if the two memories are not externally interleaved).

For example, if Box 0 contains 256K words of memory, the starting address switches for Box 1 are set to 010. The starting address for a third memory frame, Box 2, will be the total of the capacities of Box 0 and Box 1. For a fourth memory frame, total the capacities of Boxes 0, 1, and 2. If, in this case, all four memory frames contained 256K words, then the starting address of Box 2 would be 512K words. The starting address switches for Box 2 will be set to 020, from the decal. Box 3 will have a starting address of 256K + 256K + 256K or 768K and its starting address switches will be set to 030.

If any of the memory frames are externally interleaved, their box controllers must display the same starting address. Any memory interleaved with Box 0 will have a starting address of zero. To two-way interleave Boxes 0 and 1 of the preceding example, set the starting address switches of box controller 1 to 000 and set the interleave switches of Box 0 to 2 and Box 1 to 3. Similarily, Box 2 and Box 3 may be two-way interleaved by setting the starting address switches of Box 3 to 020, the starting address of Box 2. The interleave switches of Box 2 and Box 3 will then be changed from 0 to 2 and 3, respectively.

Set the starting address switches to 000 on all the box controllers for four-way external interleaving. The interleave switch settings will be 4, 5, 6, and 7. Remember that the memory capacity of the four frames must be equal for four-way external interleaving.

After configuring the MK11 memory system, enter the starting address, interleaving information, and the CSR address on the memory box decal. A sample memory box decal is shown in Figure 3-30.

3.6.3 Voltage Checks

After completing the installation and configuration procedures, verify the regulated voltage outputs of the memory frames (Table 3-3). Perform any necessary adjustments as described in Paragraph 4.5.2.2.

3.6.4 PDP-11/70 System Size Register

The system size register in the PDP-11/70 must be reconfigured to represent the new memory size. Refer to drawing D-CS-M8140-0-1, sheet SCCN in the PDP-11/70 engineering drawings and to Figure 3-21.

3.6.5 Checkout

Run diagnostics as listed in Figure 3-9.

3.7 NON-MEMORY ADD-ON INSTALLATION

Non-memory add-on installation may be:

1. System Unit (SU) options
2. Rack-mounted options
3. Cabinet options.

The options available to the PDP-11/70 are listed in Appendix F.

Installation in an existing system consists of:

1. Determination of the optimum electrical and physical position of the option on the Unibus or on the Massbus guidelines are supplied in Paragraphs 3.7.2 and 3.7.3 to aid in this determination.

2. Mechanical installation of the option.

3.7.1 Mechanical Installation

1. SUs are mounted in BA11-K boxes. All required information is supplied in the *BA11-K Mounting Box Manual,* EK-BA11K-MM.

2. Up to five SPCs may be mounted in the processor cabinet, slots 40-44. Refer to appropriate manual. Slot 40 is reserved for the DL11-A that controls the system terminal. Any additional SPCs must be mounted in BA11-K boxes.

3. Instructions for installation of rack-mounted and cabinet options are contained in their respective manuals.

3.7.2 System Configuration (Massbus)

The optimum configuration of the Massbus (RH70) is determined by the same rules used for Unibus NPR devices (Paragraph 3.7.3). The prepared order of priorities for RH70 devices is as follows:

1. CPU
2. RWS04
3. RWP04
4. RWS03
5. TWU16.

The DWR70 is a customer interface; the speed of this interface should determine the position of the DWR70 on the Massbus.

3.7.3 System Configuration (Unibus)

NOTE

System configuration is a function not only of the variables mentioned below, but also of size, available space, and power distribution. These factors are not discussed here, but must be taken into consideration when a system is reconfigured.

System configuration as defined here is a function of two variables:

1. The tolerance of each device for delays in service (maximum tolerable latency), and
2. The data transfer demand placed by each device on the system.

As the demand of device X increases, it increases the time that device Y must wait for service.

The order in which devices are serviced depends upon:

1. Their assigned priority, in descending order: NPR, BR7, BR6, BR5, BR4.
2. Within each priority, the order in which they are placed on the Unibus (electrical position).

The definitions that follow are taken from the glossary of the Unibus specification:

Latency is the delay between the time that a device initiates a transaction and the time that it receives a response.

Thus, if a device requests the use of the data section of the bus, is granted the use of the bus, and then receives the negation of BBSY (signifying that the previous master has released the data section of the bus), then latency is the delay between the assertion of the request and the receipt of the negation of BBSY by the requesting device.

Maximum Tolerable NPR Data Transfer Latency is the longest time that a device may be refused bus mastership before it loses data. It affects only devices that transfer data in a constant stream, e.g., a disk.

Maximum Tolerable BR Interrupt Latency is the longest time the computer may take to service an interrupt before the requesting device loses its data. The service time includes the execution of all higher priority interrupts and programs that may be pending, plus the time spent in the interrupt subroutine of the device in question.

From the preceding, general rules for configuration may be stated as follows ("behind" means farther from the processor):

1. In general, BR devices should be placed physically behind NPR devices; thus, the propagation delay of fast NPR devices is reduced and transfers are faster. For convenience, however, some BR devices are sometimes placed before NPR devices, e.g., DL11-A/LA36 is first on the Unibus in the PDP-11/70 (slot 40 of the processor backplane.)

2. Buffered devices (Category 2: see Figure 3-33 for definition) should be placed physically behind unbuffered devices (Category 1: see Figure 3-33).

3. In either category, devices with higher transfer speed rates should be placed ahead of devices with lower transfer speed rates.

4. Less used devices may be placed behind devices that are accessed more often, if required.

Figure 3-32 shows the optimum placement of Massbus and NPR Unibus devices in a PDP-11/70 system.

The flowchart (Figure 3-33) provides an algorithm by which these variables can be combined to produce an optimum Unibus system configuration of both NPR or BR devices. BR devices are placed behind NPR devices with the same data transfer rates, and before NPR devices with slower data transfer rates. The same algorithm is used. This flowchart is intended only as a guideline.

NOTE

The algorithm given in Figure 3-33 suggests the optimum positioning of contending devices on the Unibus. This positioning is not mandatory. If the configuration resulting from the use of this algorithm is not satisfactory, alternative placement of devices should be tried.

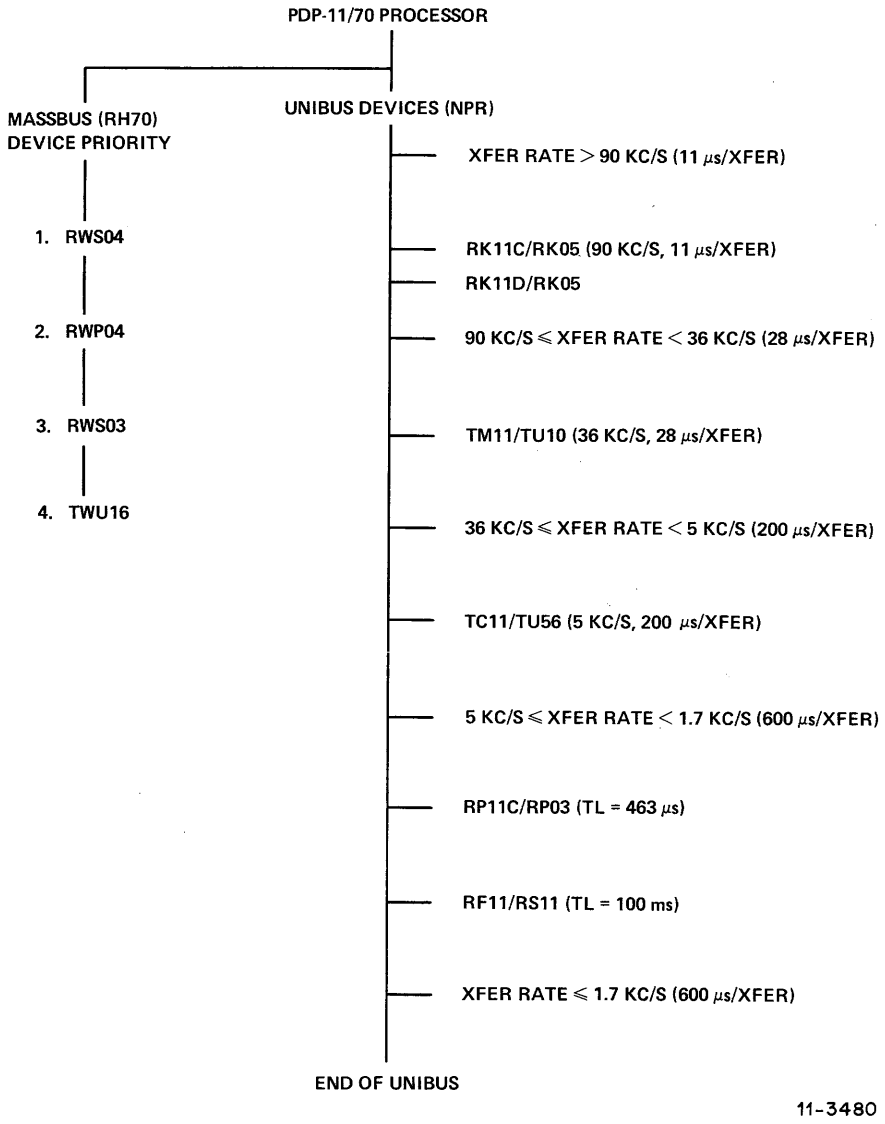


Figure 3-32 PDP-11/70 Configuration

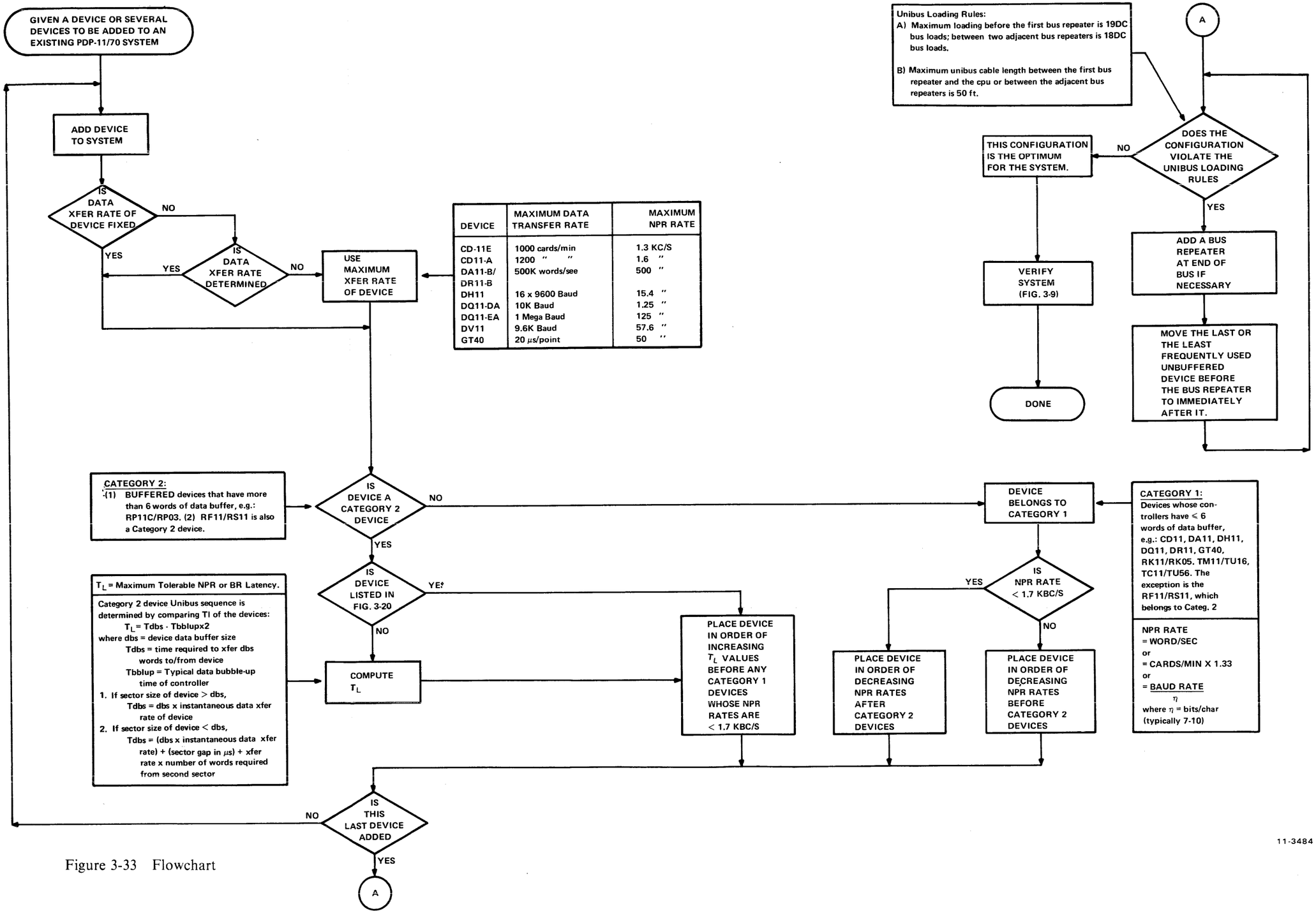


Figure 3-33 Flowchart

CHAPTER 4
POWER SYSTEM

4.1 SCOPE
This chapter describes ac and dc power in the PDP-11/70. Both the processor cabinet and the memory cabinet power systems are discussed. Included are descriptions of the power supplies, their location within the cabinets, how they function, voltage adjustments, and component removal procedures.

4.2 OVERALL SYSTEM DESCRIPTION
Figure 4-1 shows the physical location of the PDP-11/70 power system. The basic components are two 861-D/E power controls (one in the processor cabinet and one in the first memory cabinet), two H7420 power supplies (both located in the processor cabinet) and one power supply (per frame of memory), located in the memory cabinet. Additional power controls would be required if the basic system is expanded.

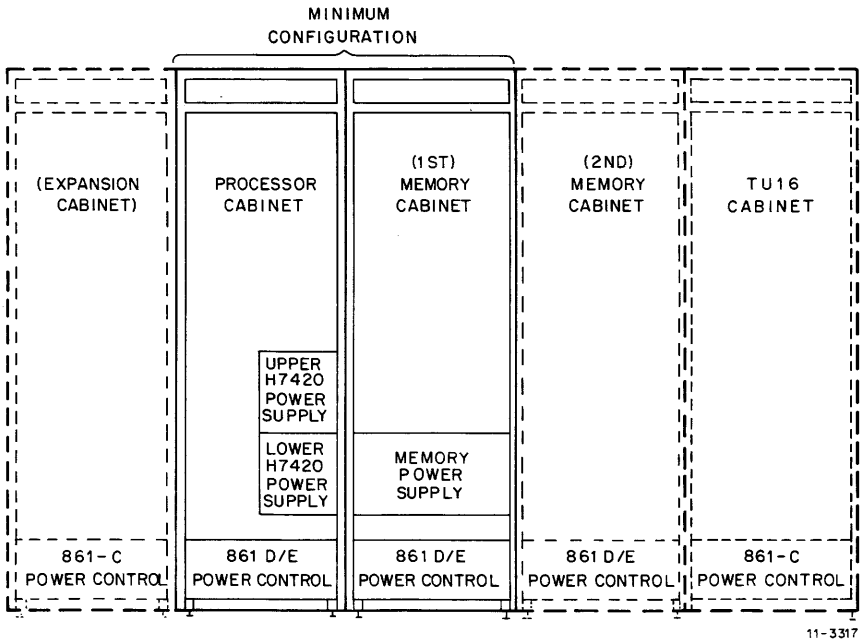
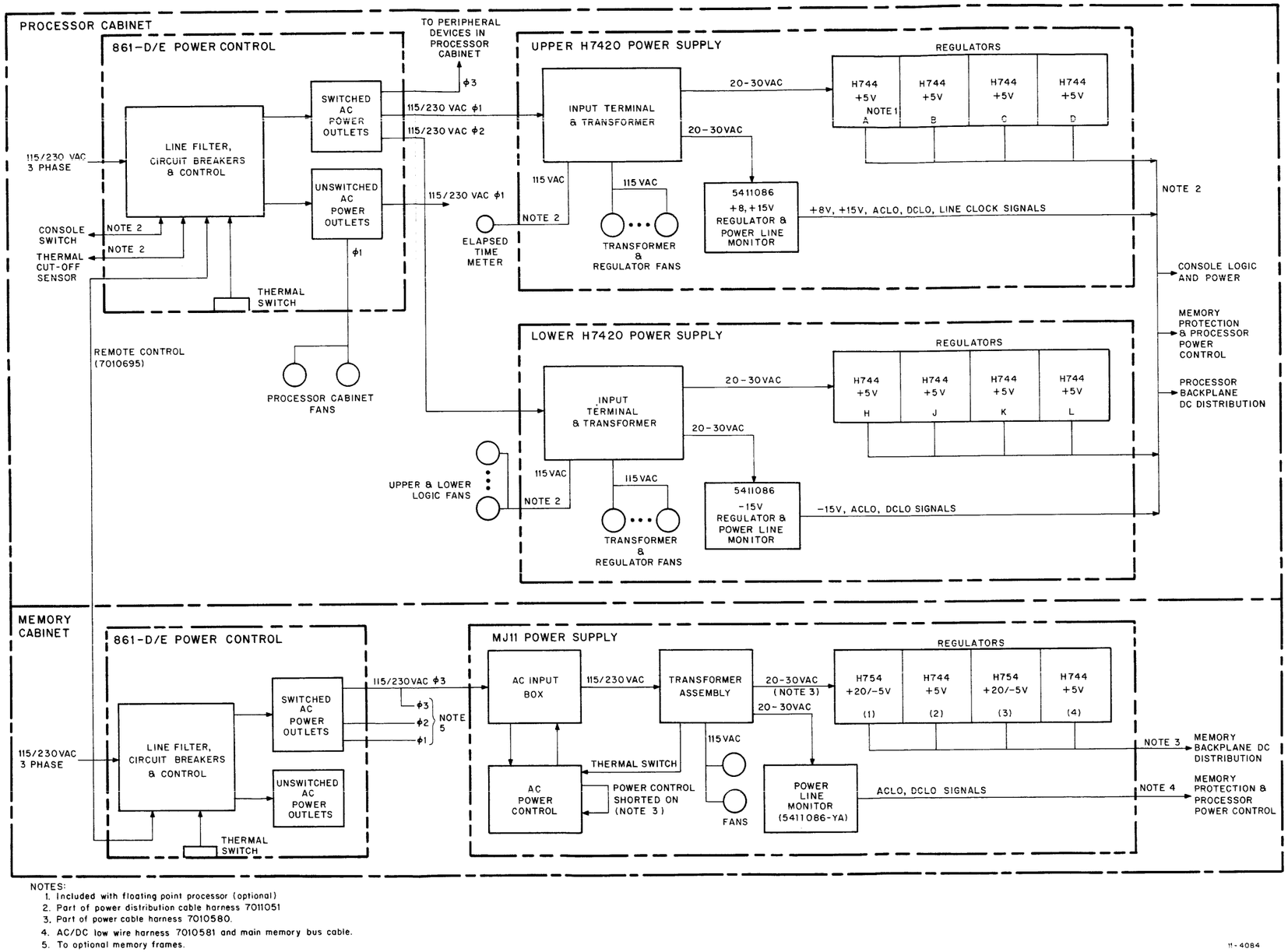


Figure 4-1 PDP-11/70 Power System, Physical Location

Figure 4-2 is a block diagram of the power system for a typical PDP-11/70. The processor and memory cabinets derive their ac and dc power from separate sources. In the processor cabinet, the basic devices are an 861-D power control (120 Vac line voltage) or an 861-E power control (240/415 Vac line voltage), and two H7420 power supplies. The memory cabinet contains a separate 861-D or E power control and a memory frame power supply. (Up to seven additional MJ11 memory frames or three additional MK11 memory frames can be installed. Each would require a separate memory frame power supply. Refer to Paragraph 4.3.2.).



NOTES:
1. Included with floating point processor (optional)
2. Part of power distribution cable harness 7011051
3. Part of power cable harness 7010580.
4. AC/DC low wire harness 7010581 and main memory bus cable.
5. To optional memory frames.

Figure 4-2 Typical PDP-11/70 Power System

4.2.1 Processor Cabinet

The processor cabinet 861 power control is connected to the building mains (120 or 240 Vac 3 phase wye) which must be capable of supplying 24A (861-D) or 15A (861-E) per pole. Two types of outlets are provided on the 861: switched and unswitched (Figure 4-2). The switched group of outlets, which can be controlled either locally or remotely, consist of phase one, two, and three outlets. The unswitched outlets, however, are controlled solely by the 861 front panel circuit breakers; they are all phase one. The processor cabinet 861 switched outlets are controlled remotely by a switch on the processor console and a thermal cut-off switch in the processor mounting box. A second thermal switch is flush mounted on the side of the 861 box. These switched outlets are de-energized if either sensor detects an over temperature or the console switch is turned to the OFF position. The memory cabinet 861 switched outlets are also de-energized at the same time since the 861s are connected by a remote control cable.

Two H7420 power supplies, designated the upper H7420 and the lower H7420 according to their cabinet mounting location, are connected to phase one and phase two switched outlets, respectively, on the 861 rear panel. Each H7420 power supply contains four H744 +5 V regulators (three in the upper H7420 if the floating point option is not included in the system). These regulators furnish +5 Vdc to the processor backplane and the processor console. Their applications are listed in Table 4-1. A circuit description of the H7420 is provided in Paragraph 4.4.4.

In addition to the H744 regulators, each H7420 contains a 5411086 regulator. The 5411086 regulator in the upper H7420 provides a +8 V and +15 V to the processor backplane and functions as the power line monitor for the upper supply. This upper 5411086 also produces the line clock output that is used to drive the KW11-L line frequency and KW11-P real-time clock option. The 5411086 in the lower H7420 furnishes -15 V to the processor and monitors the lower supply for a low voltage condition. AC LO and DC LO signals are asserted in the event of a low voltage input to either 5411086 regulator (Paragraph 4.4.6.1 and Figure 4-34).

Completing each H7420 power supply are the input terminal block and the transformer assembly. The input terminal block in the upper H7420 provides 115 Vac to the elapsed time meter (which is mounted at the rear of the processor cabinet) to the power supply fans (one for the transformer and three for the regulators), and to the transformer primary. The lower H7420 input terminal block provides similar connections. However, in place of the output to an elapsed time meter, the lower input terminal block supplies 115 Vac to the processor mounting box fans (five upper and four lower). The terminal block in an H7420 used in a 230 Vac environment (861-E power control) provides the same voltage outputs.This is accomplished through the use of a different jumper configuration on the terminal block itself (drawing D-CS-H7420-0-1 and Figure 4-28). The transformer produces 20–30 Vac at the secondary (the actual voltage is subject to input voltage fluctuations). Outputs are provided to the H744 and 5411086 regulators.

A single power distribution cable harness (7011051) distributes the power and signal outputs from both H7420s. In addition to delivering dc voltages to the processor console and the processor backplane, the cable routes the AC LO and DC LO signals to the memory protection logic and to the processor power control logic. The line clock signals go to the line time clock. Also contained in the cable harness are connecting wires from the processor console switch and the thermal cut-off sensor to the 861-D/E power control. Figure 4-3 illustrates how the power distribution cable connects the 861 and the H7420s with the processor backplane.

A more detailed description of the processor cabinet and the H7420 power supply is provided in Paragraph 4.4.4.

Table 4-1 Processor Power Supply Voltage Regulators

Type	Name	Quantity	Location (Note 1)	Application (Figure 4-20)
H744	+5 V Regulator	8 (Note 2)	A	+5 V to processor module slots 2-5. Included only with the FP11 option.
			B	+5 V to processor module slots 1, 6–9.
			C	+5 V to processor module slots 10–15.
			D	+5 V to processor module slots 36–44.
			H	+5 V to processor module slots 20–22.
			J	+5 V to processor module slots 16–18 and to the console.
			K	+5 V to processor module slots 24–28.
			L	+5 V to processor module slots 29–35.
5411086	+8, +15 V Regulator	1	Upper H7420	+8 and +15 V to processor backplane; AC LO and DC LO sensing for the upper H7420.
5411086	-15 V Regulator	1	Lower H7420	-15 V to processor backplane; AC LO and DC LO sensing for the lower H7420

Notes:
1. Location within the H7420s.

2. Seven if the FP11 option is not included.

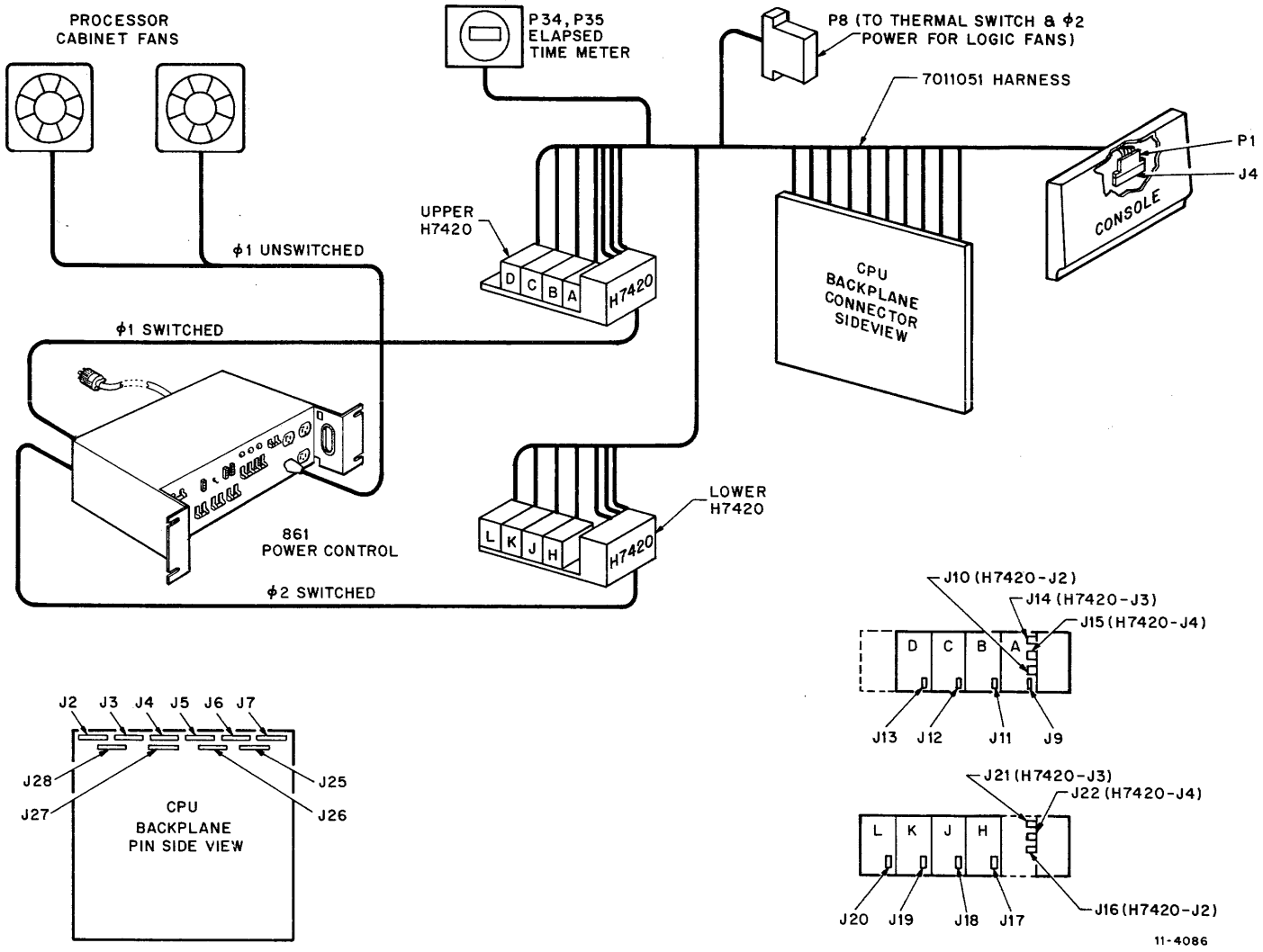


Figure 4-3 Processor Cabinet Power Connections

4.2.2 Memory Cabinet

As previously mentioned, the memory cabinet has its own power system (Figure 4-2). This system consists of an 861-D/E power control and a memory power supply. The 861s in the processor and memory cabinets are connected via a remote control cable (7010695). This cable connection allows the switched outlets on both power controls to be de-energized in the event either power control is shut down due to over temperature or if the console switch is turned to the OFF position (MJ11 only). The memory cabinet 861-D/E is connected to the building mains (120 or 240 Vac 3-phase wye). This source must be capable of supplying 24 A (861-D) or 15 A (861-E) per pole. Switched and unswitched outlets are provided on the 861; the switched outlets are the power source for the one or more memory frames included in the system. Switched phase 3 power is used if the minimum memory configuration of one frame is installed.

The MJ11 power supply (120 Vac: 7010694-00; 240 Vac: 7010694-01) consists of an ac input box with an associated power control circuit, a transformer assembly, a power line monitor circuit, four voltage regulators and two 1211714 fans.

The MK11 power supply (120 Vac: 7014227-00 240 Vac: 7014227-01) consists of an ac input box with an associated power control circuit, a transformer assembly, a power line monitor circuit, four voltage regulators, two 1211714 fans, and three H775 battery backup units.

The ac input box, under the direction of the ac power control circuit, routes the ac input power to the transformer assembly. Two types of boxes are used: one (7009811-1) for a 120 Vac input from an 861-D power control, and one (7009811-2) for a 240 Vac input from an 861-E power control. Only one ac input box is installed in each memory power supply. The ac power control circuit (5410993) controls the 120/240 Vac input to the transformer. A shorting wire in the MJ11 maintains the circuit in an ON condition, i.e., power is routed to the transformer. However, an input from a thermal switch attached to the transformer can open this circuit if an over-temperature condition is sensed. In the MK11, the power switch on the box controller switches ac power to the transformer via connector J4 on the ac input box.

In the 7010014 (MJ11) or 7011486 (MK11) transformer assembly, two terminal blocks, with power inputs from the ac input box, have outputs to two fans that cool the transformer. Other terminal block outputs are to the transformer, which steps down the line voltage (120/240 Vac) to the required 20/30 Vac input for the regulators and the power line monitor circuit.

The power line monitor circuit and 15 V regulator are part of the 5411086; the regulator portion of the card is not used in the MJ11 or MK11 application – 5411086-YA. If a low voltage condition occurs at the 20–30 Vac input from the transformer assembly, the 5411086-YA asserts AC LO and DC LO signals. These power fail signals are carried to the memory protection logic and to the processor power control logic via a wire harness (7010581) and the main memory bus cable.

There are four voltage regulators used in the MJ11 power supply, two H744 and two H754. The H744 regulators generate +5 V and the H754 regulators generate both –5 V and +20 V. These dc voltages are routed to the memory backplane through the power cable harness (7010580). This cable also carries the 20–30 Vac input to the regulators from the transformer.

There are four voltage regulators used in the MK11 power supply, one H7441 and three 7014251. The H7441 regulator generates +5 V and the 7014251 regulators generate +5 V, +12 V, and –12 V. Cable harness 7014228 routes the stepped down ac voltage to the regulators and also routes the regulated voltages from the regulators to the memory backplane.

Figure 4-4 shows the power and signal connections between the 861 power control, the MJ11 power supply and the memory backplane. Figure 4-5 shows the power and signal connections for the MK11 memory.

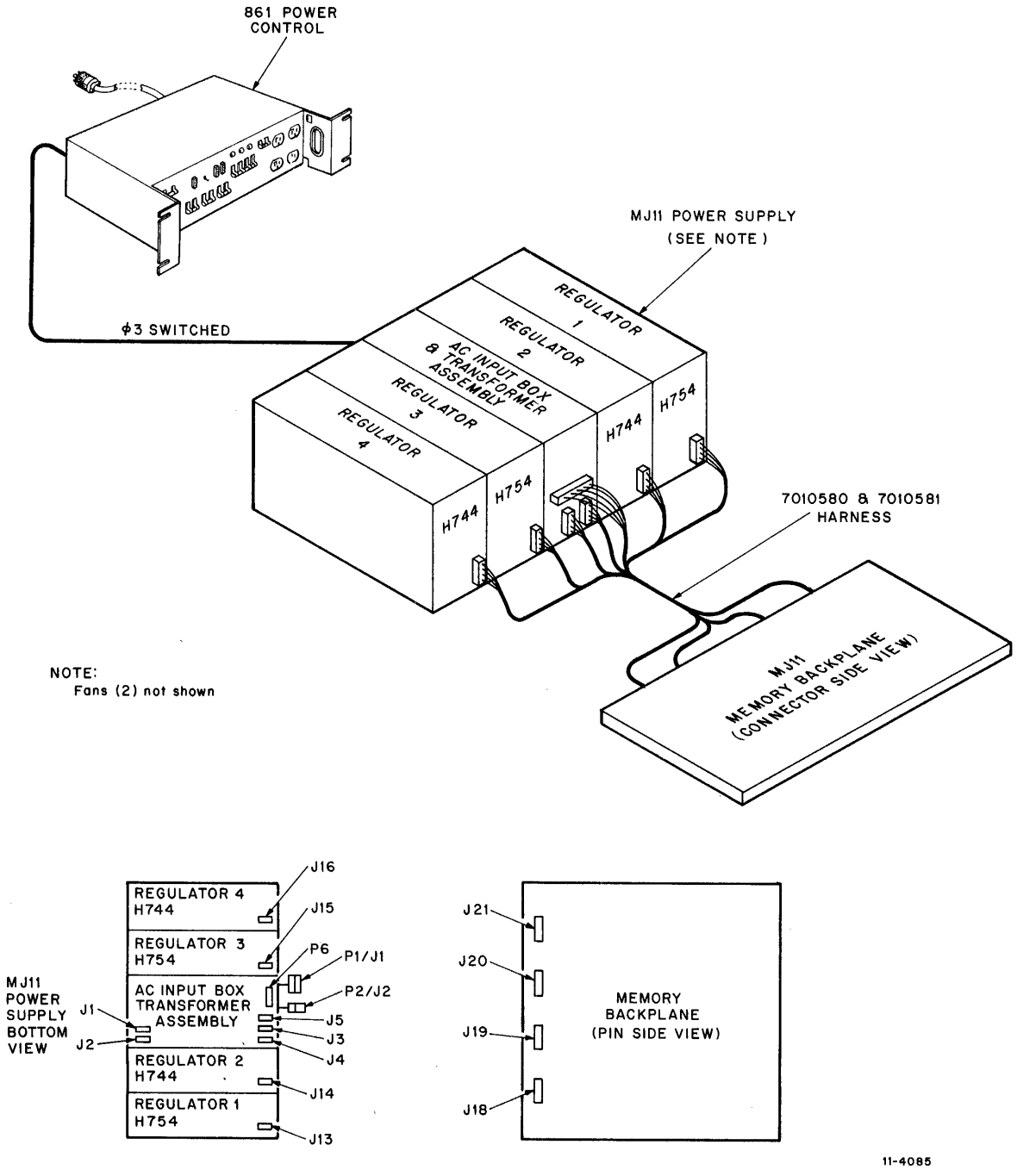


Figure 4-4 MJ11 Memory Cabinet Power Connections

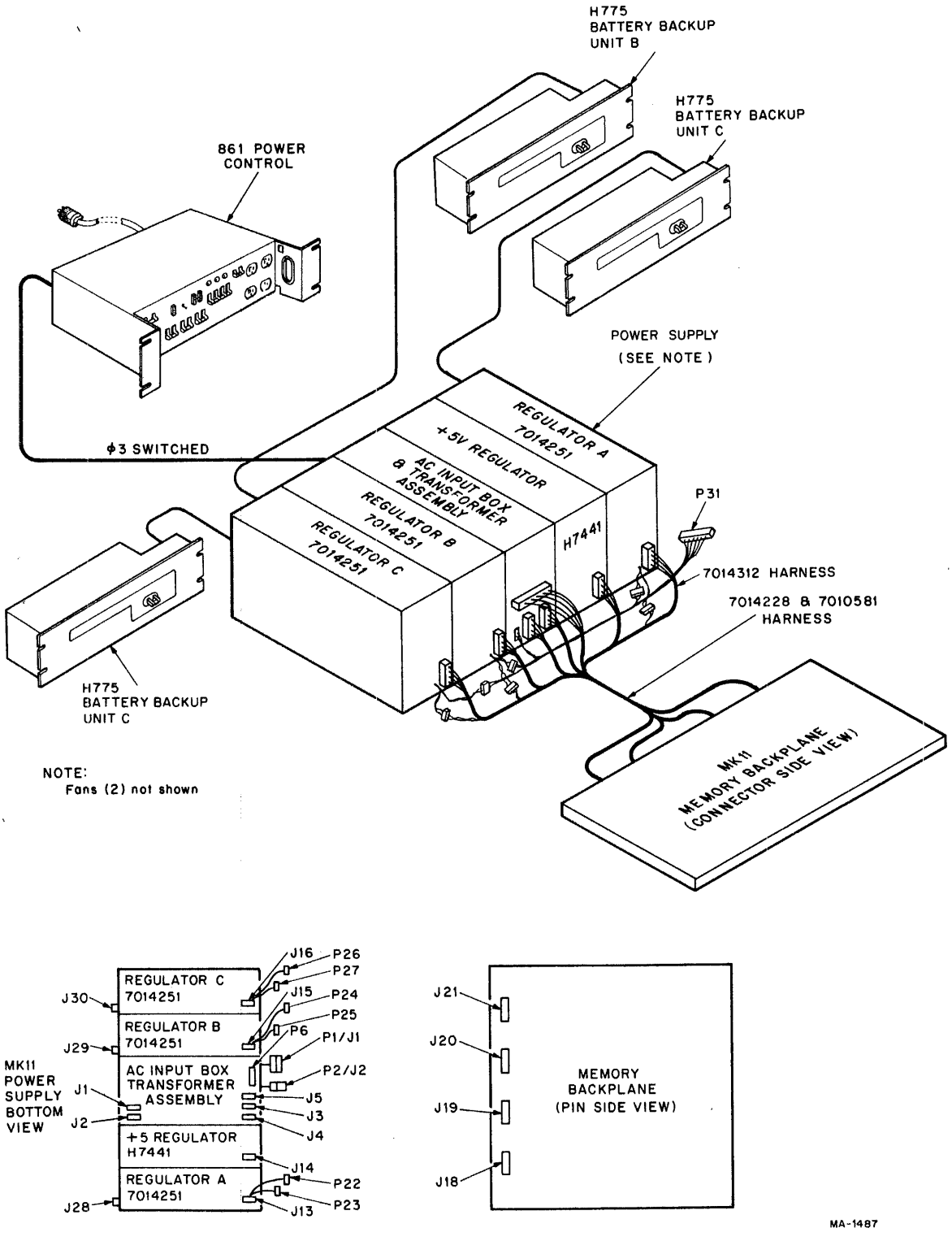


Figure 4-5 MK11 Memory Cabinet Power Connections

The contents of the power system are housed in a welded steel chassis. The chassis is rectangular and measures approximately 7-3/4 inches long by 10-1/2 inches high by 17 inches wide. The top power system cover is held in place by six screws. The main structural member contains cutouts and drill holes which enable screws to be inserted for securing the regulators, ac input box, transformer assembly, and fans. Cutouts for the regulators allow the regulator ON indicators to be monitored and the regulator output voltages to be adjusted.

A more detailed description of the memory cabinet and the power supply is provided in Paragraph 4.4.6 for the MJ11 and Paragraph 4.4.7 for the MK11.

4.3 PRIMARY AC POWER, 861 POWER CONTROL

Power from the building mains is applied to the system components in the processor, memory, and expansion cabinets through 861-D/E power control units. In a minimum configuration system consisting of a processor cabinet and a memory cabinet, power is controlled by two 861-D/E power controls, one in each cabinet. The controls are located at the bottom front of the cabinets (Figure 4-1).

The 861-D is used with 120 Vac, 3-phase lines; the 861-E is used with 240 Vac (415 Vac phase to phase), 3-phase lines. Both versions are contained on panels intended for mounting in racks or cabinets that accept standard 19-inch panels. Each power controller requires 5-3/16 inches of vertical mounting space and extends 11 inches into the mounting rack or cabinet.

Figure 4-6 is a simplified block diagram of the 861-D Power Controller. Four basic functions are performed:

1. Control of large amounts of power by control signals of small power content.
2. Convenient distribution of primary power to controlled devices.
3. Filtering of primary power to controlled devices.
4. Automatic removal of primary power from controlled devices in case of overload or overtemperature conditions.

Circuit descriptions of the 861-D and 861-E are given in Paragraph 4.3.5; ac power and remote power control connections are described in Paragraphs 4.3.2, 4.3.3, and 4.3.4.

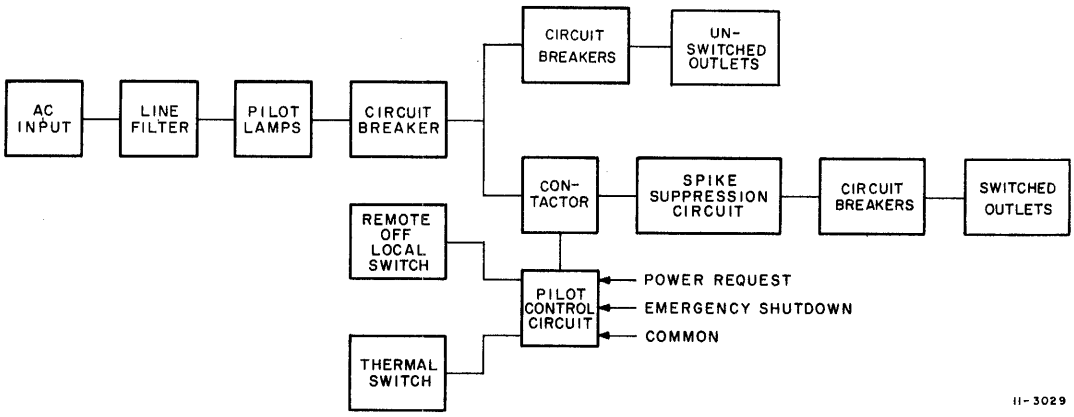


Figure 4-6 861 Power Controller Simplified Block Diagram

4.3.1 Power Control Specifications

Power control specifications are listed in Table 4-2. Reference should be made to the *861-A, B, C, D, E, F Power Controller Maintenance Manual* for additional information.

Table 4-2 Power Controller Specifications

Mechanical and Environmental	
Dimensions	12.7 cm h, 48.57 cm w, 27.94 cm d (5 in h × 19-1/8 in w × 11 in d)
Weight	12.24 kg. (approx) (27 lb)
Cooling Method	Convection
Mounting	Rack (standard 19 in)
Ambient Temperature (recommended temperature)	
Operating	0° to +70° C
Storage	-40° to 71° C
Relative Humidity	95% max (no condensation)
Altitude (max)	2438 m (8,000 ft)
Shock, Non-operating	40 G (duration 30 ms)
Vibration, Non-operating	1.89 G rms average, 8 G peak; varying from 10 to 50 Hz, 8 dB/octave roll-off, 50–200 Hz; each of six directions
Electrical	
Input Power	
Voltage–phase to neutral of 3-phase wye	861-D: 90 Vac – 132 Vac 861-E: 180 Vac – 264 Vac
–phase to phase	861-D: 156 Vac – 229 Vac 861-E: 312 Vac – 458 Vac
Phase	3-phase (120 degree displacement) wye connection
Frequency	47–63 Hz
Current	861-E: 24 A per phase 861-E: 15 A per phase
Power Requirements	
Full load	861-D: 8640 VA 861-E: 10800 VA
No load	10 VA maximum
Inrush Current Capability	600 A peak, 1/2 cycle per phase
Input Overvoltage Transient (power controller alone)	180/260 V, 1 second 360/720 V, 360 ms

Table 4-2 Power Controller Specifications (Cont)

High Voltage Transients	
Magnitude	1 kV
Duration	$\leq 0.1 \mu s$
Frequency	$\leq 10 \mu s$ once every 10 s
Average Power	≤ 0.5 W
Leakage Current	861-D: 1.75 mA max 861-E: 3.5 mA max
Activate Time	20 ms (from switch closing to power out)
Deactivate Time	10 ms (from switch opening to power out)
Input Breaker	Delayed action, manual reset, magnetic; 861-D: 30 A; 861-E: 15 A
Thermoswitch	Opens at 71.1° C (160° F), automatically resets at 49° C (120° F), (exposed to ambient air external to controller)
Input Power Connection	861-D: NEMA L21-30P (Table 4-3) 861-E: None provided
Remote Power Control	
Remote Switching Control Connectors	Three: Female, AP 1-480304-0 (DEC-12-09350-03) with Amp 61117-4 (DEC-12-09379) pins or equivalent. These mate with AMP 1-480305-0 (DEC-12-09351) connectors with AMP 61118-4 (DEC-12-09378) pins or equivalent.)
Remote Control Cable	DEC 7010695
Input Signal Current Levels (for worst case line voltage)	0.5 mA min, 40 mA max Power Request 0.5 mA min, 80 mA max Emergency Shutdown
Input Signal Voltage Levels (for worst case line voltage)	+3.0 V max = low; +35 V min = high
Bus Signal Line Overload Capability	125 Vac rms, 60 Hz, 13K ohms impedance in relation to pin 3 for two seconds with no damage
Power Control Impedance	Inductive (diode suppressed)
Power Control Capacitance	200 pF (max)
Output	
Outlets (power)	14 (10 switched, 4 unswitched)
Outlet Current Ratings	861-D: 15 A/outlet, 24 A/phase 861-E: 12 A/outlet, 15 A/phase

4.3.2 Power and Power Control Connections

The H7420 processor cabinet power supplies and the memory cabinet power supply are connected to the switched outlets of the two power controls. All power supplies within these cabinets are single phase. The upper H7420 is plugged into a phase 1, circuit 2 outlet while the lower H7420 is plugged into a phase 2, circuit 1 outlet on the processor cabinet 861 power control (Figure 4-7). If the system contains a single memory frame, the memory power supply is connected to a switched phase 3 outlet on the memory cabinet 861 power control. Additional memory frames use switched phase 1, 2, or 3 outlets on the 861, as shown in Figure 4-8.

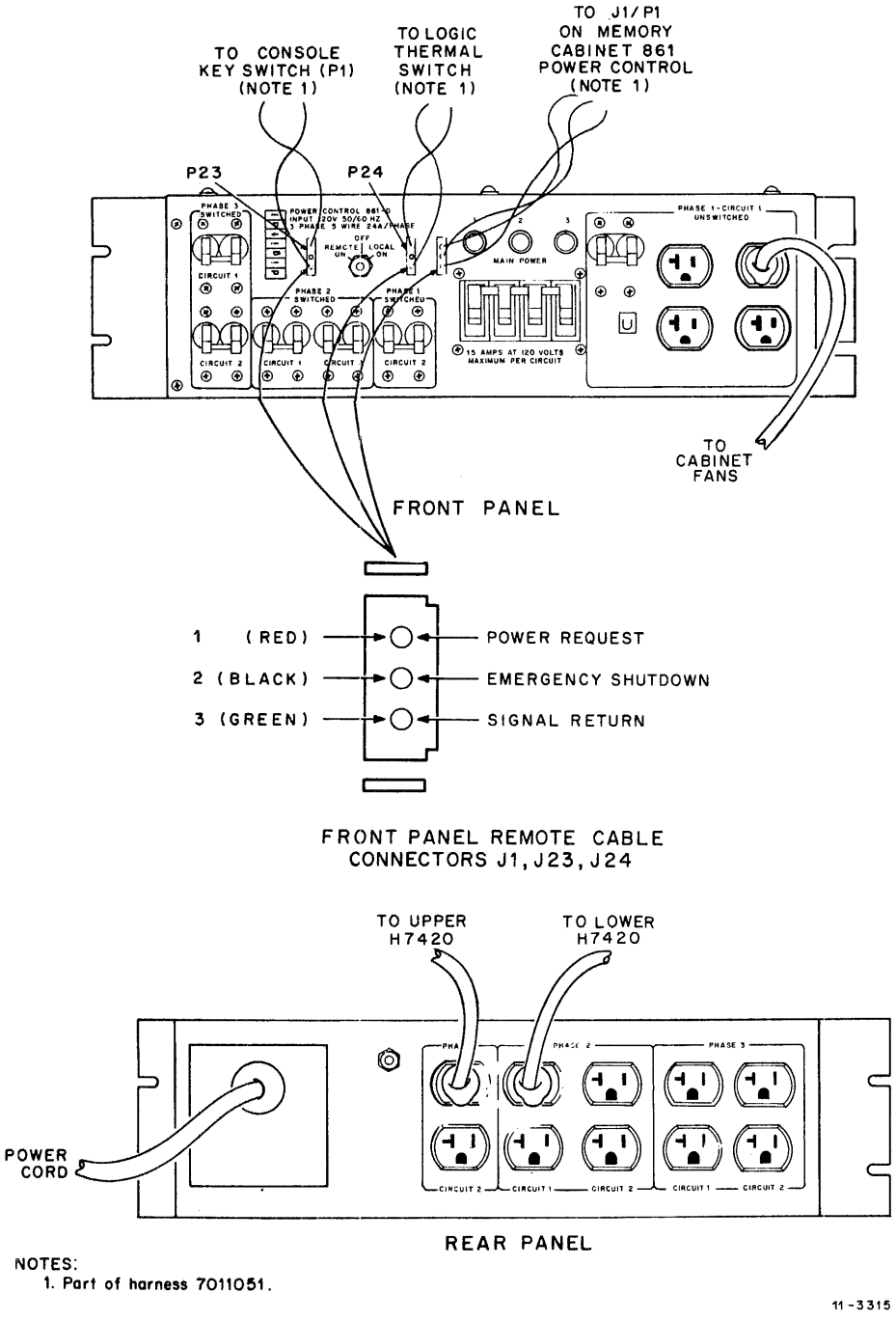


Figure 4-7 Processor Cabinet Power and Remote Control Connections

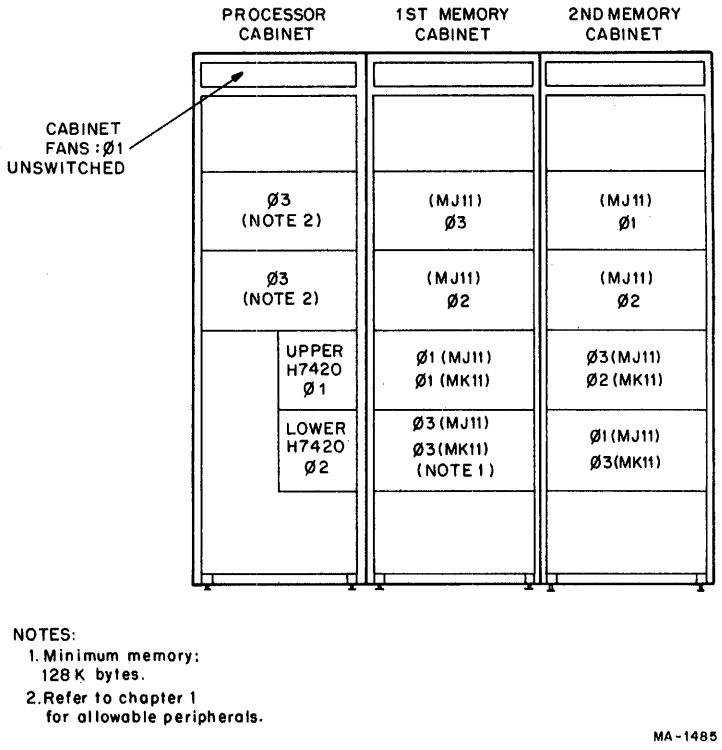


Figure 4-8 PDP-11/70 Power (Phase) Assignments

The 861-D/ E power controls in adjacent cabinets are interconnected to allow power in all cabinets of the system to be controlled from the processor console (power ON/OFF) or from emergency shutdown devices, i.e., thermal sensors. The remote power control cables used to interconnect the system cabinets contain three conductors and connect to three pin Mate-N-Lok connectors that are plugged into the 861 front panel (Figure 4-7). The following signals are routed to the pins:

Pin 1 POWER REQUEST - A ground on this line activates the power control circuits and energizes the device.

Pin 2 EMERGENCY SHUTDOWN - A ground on this line de-energizes the device.

Pin 3 GROUND RETURN - This is the ground return for the preceding two signals.

The three remote power control connectors on the power controller are connected in parallel. When power is turned on at the processor console, a ground is routed via the power request line to all the power controllers in the system, causing their switched outlets to be energized.

A more detailed description of remote power control is contained in Paragraph 4.3.4.

4.3.3 Primary AC Power Connections

Of the two 861 power control versions supplied with the PDP-11/70, only the 861-D is equipped with an input power cable and connector. This cable is 15 feet long and consists of insulated stranded conductors. The input power cable connector and receptacle part numbers are listed in Table 4-3. The primary power outlet (receptacle) at the installation site must be compatible with the input power cable connector on the 861-E, Figure 4-9 shows the 861-D connector and receptacle outlines in addition to wire color coding information.

NOTE

In MK11 memory cabinets, the 861 LOCAL/OFF/REMOTE switch must be in the LOCAL position. Power to the memory is controlled by the box controller power switch.

Table 4-3 861-D Input Power Connector

Description	Poles	Wires
120 Vac, 30, 30 A, 5-prong twist	4	5 No.10 AWG

Plug			Receptacle		
NEMA	DEC No.	Hubbell No.	NEMA	DEC No.	Hubbell No.
L21-30P	12-12314	2811	L21-30R	12-12315	2810

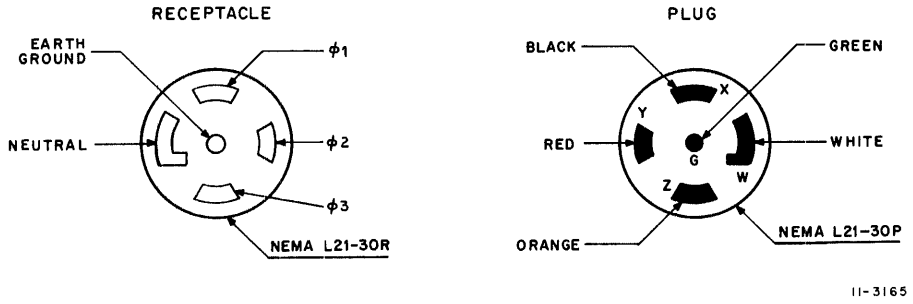


Figure 4-9 861-D Power Control Connector Outline

4.3.4 Remote Power Control Connections

Each cabinet in a PDP-11/70 system has one 861-D or 861-E power control. All the power controls are connected by a 3-wire bus that carries a remote turn-on signal (line 1), an emergency turn-off signal (line 2), and a control ground (line 3). These signals appear on pins 1, 2, and 3, respectively of the power control's J1, J23 and J24 connectors. Operation occurs as follows:

1. Connection between line 1 and line 3 energizes the power control relay and applies power to the components under control. When the LOCAL/OFF/REMOTE switch on the power control is in LOCAL, line 1 and line 3 are connected.

2. Connection between line 2 and line 3 overrides all other conditions to disconnect input power to the components under control.

3. If no connection exists between either lines 1 or 2 and line 3, the components will remain in the power off state unless the LOCAL/OFF/REMOTE switch is in LOCAL.

Table 4-4 summarizes these connectors.

Table 4-4 Power Control Operation

		Switch Position	
Connections Between Control Lines	**Local Switched Power is:**	**Off Switched Power is:**	**Remote Switched Power is:**
None	ON	OFF	OFF
1-3	ON	OFF	ON
2-3	OFF	OFF	OFF
1-3, 2-3	OFF	OFF	OFF

Three identical parallel-wired Mate-N-Lok connectors are provided on each power control. A 3-foot cable, DEC part number 7010695, is supplied with each cabinet to connect the power control of that cabinet to the power control in the next cabinet (Figure 4-10). Because each power control must be capable of connecting to the power controls in the preceding and following cabinets, two Mate-N-Lok connectors are reserved for the intercabinet cables; a third connector is provided for connection to thermal switches and other shut-off devices within the cabinet.

4.3.5 Power Controls 861-D and 861-E

Two versions of the power control are available for use in the PDP-11/70 (Figure 4-11):

1. 861-D 90–132 Vac, 47–63 Hz, 3-phase, 24 A/phase (30A circuit breaker)

2. 861-E 180–264 Vac, 47–63 Hz, 3-phase, 15 A/phase (15 A circuit breaker)

Circuit schematics of the 861-D and 861-E power controls are included in the engineering drawing set (D-CS-861-D-1 and D-CS-861-E-1).

Both versions of the 861 are similar. However, they are discussed separately in Paragraphs 4.3.6 and 4.3.7 for clarification purposes. The pilot control boards in the 861-D and 861-E are identical; they are described together in Paragraph 4.3.8.

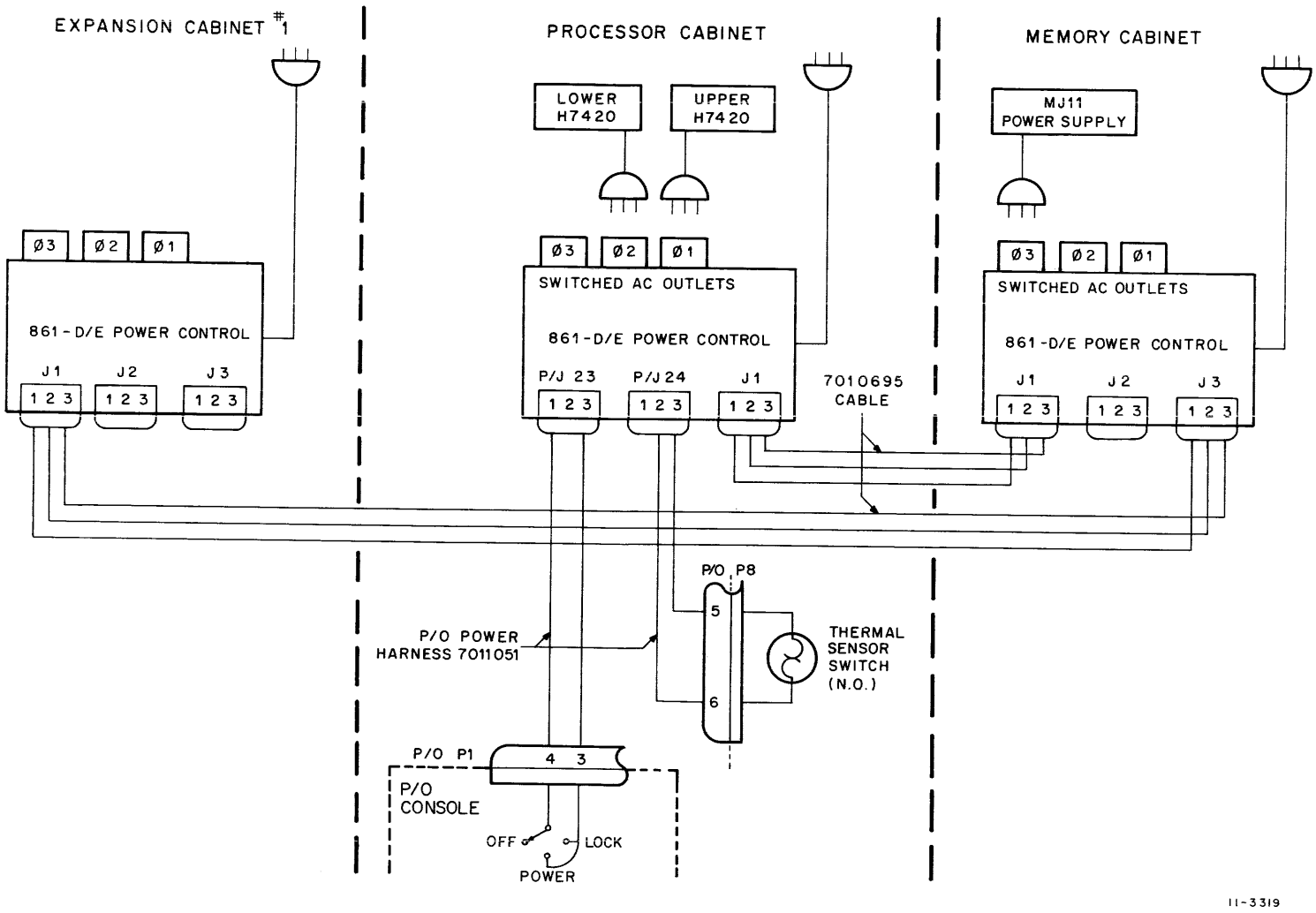
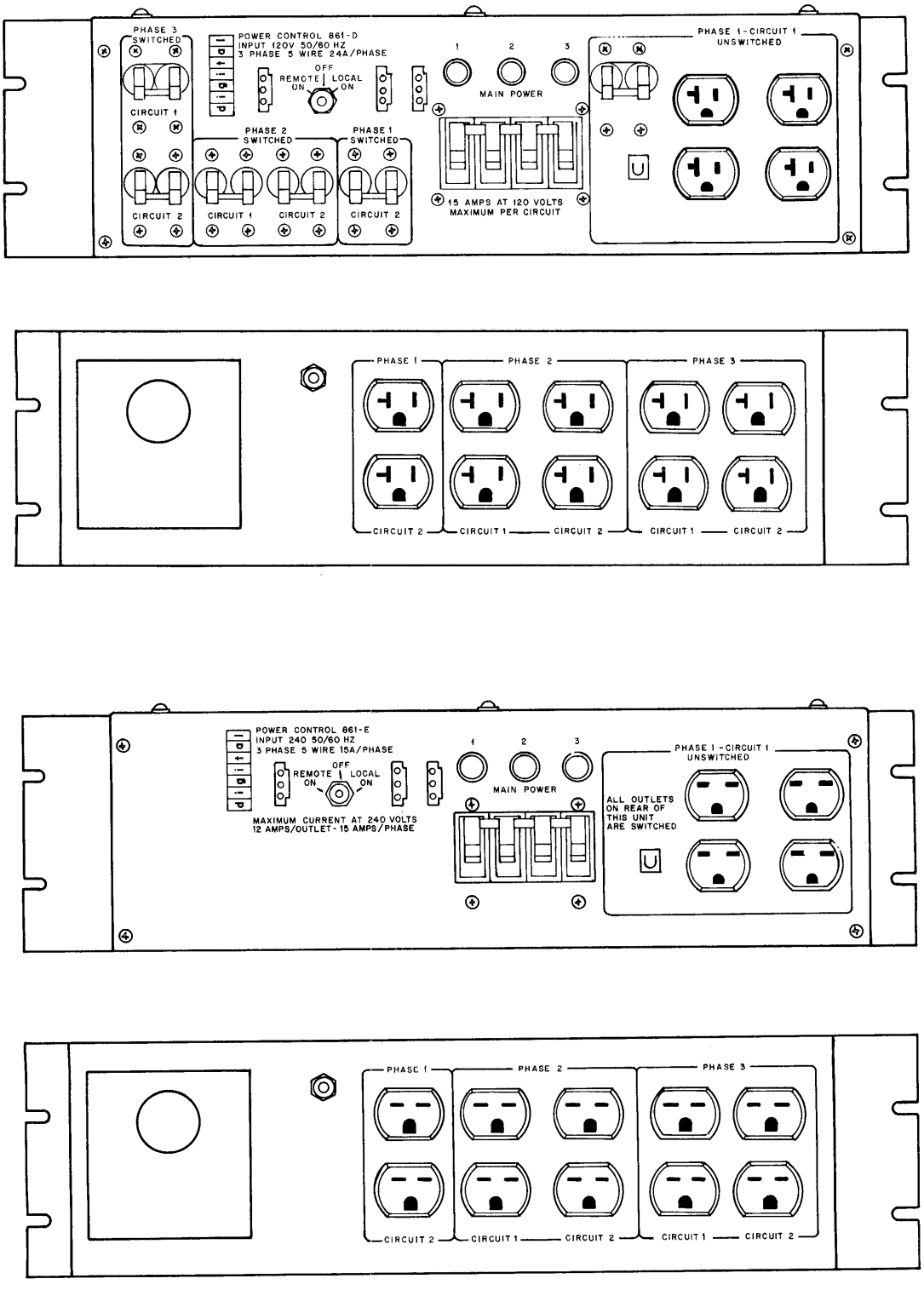


Figure 4-10 Example of Remote Power Control



CP-1730

Figure 4-11 861-D/E Power Control Panels

4.3.6 Type 861-D Circuit Description

Figure 4-12 is an 861-D simplified circuit schematic. The 861-D is a 90–132 Vac, 47–63 Hz, 3-phase power controller.

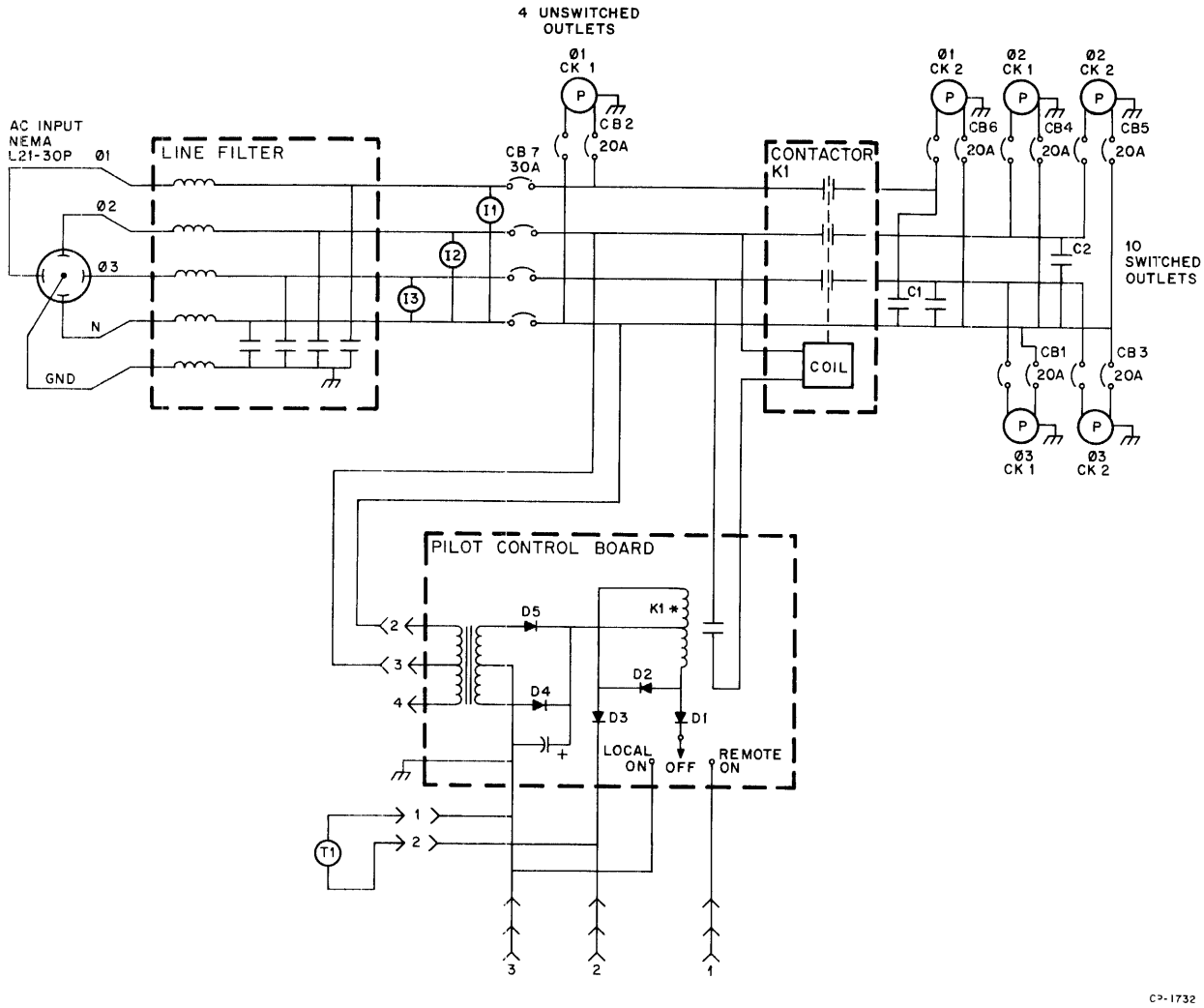


Figure 4-12 861-D Simplified Circuit Schematic

Power is applied to the terminal block mounted on the power line filter via a 15-foot line cord. This filter contains 0.03 μF capacitors which connect between neutral and each of the 3-phase lines, and between neutral and ground. Also contained in the filter are nine chokes, connected in series with each of the four lines and ground. The capacitors provide low impedance paths to ground for high frequency line components. The chokes present a high impedance to these components. If 90–132 Vac exists between phase 1 and neutral, I1 lights. If 90–132 Vac is present between phase 2 and neutral, I2 lights. Similarly, if 90–132 Vac is present between phase 3 and neutral, I3 lights.

All three lines are connected to 30 A elements in circuit breaker CB7. All loads connected to the power controller (both switched and unswitched) are controlled by individual 20 A circuit breakers, CB1 through CB6.

If the current through any of the lines exceeds 20 A, the respective circuit breaker trips, removing power from the loads. Phase 1, circuit 1 outlets connect across the main circuit breaker output. These outlets are energized (90–132 Vac) whenever the circuit breaker is closed. All outlet lines from CB7 are connected to a normally open contact on contactor K1. The field coil associated with K1 is energized by 156–229 Vac from the output of CB7 if a relay (K1*) on the pilot control board is closed (see Paragraph 4.3.8 for a description of the pilot control board).

When K1 is closed, 90–132 Vac is applied across phase 1, circuit 2, phase 2, circuits 1 and 2, and phase 3, circuits 1 and 2. The three 0.1 μF capacitors (C1 and C2), connected across the lines at the relay, reduce the amplitude of voltage spikes at the output of the controller when switching inductive loads, thereby preventing interference to nearby electronic data processing equipment.

4.3.7 Type 861-E Circuit Description

Figure 4-12 is a simplified circuit schematic of the 861-E, the 180–264 Vac (312–457 Vac phase to phase), 47–63 Hz, 3-phase version of the power controller.

Power is applied to the terminal block mounted on the power line filter. This filter contains 0.03 μF capacitors which connect between neutral and each of the 3-phase 180–264 Vac lines, and between neutral and ground. Also contained in the filter are nine chokes, connected in series with each of the four lines and ground. The capacitors provide low impedance paths to ground for high frequency line components. The chokes present a high impedance to these components. If 180–264 Vac is present across each line at the output of the line filter, I1, I2, and I3 light. Each side of the line connects to a 15 A element of circuit breaker CB1. All loads connected to the power controller (both switched and unswitched) are controlled by CB1. If the current through either line exceeds 15 A, CB1 trips, removing power from the load. Phase 1, circuit 1 connects across the output of CB1. These outlets are energized (180–264 Vac) whenever the circuit breaker is closed. Each output line from CB1 connects to a normally-open contact on contactor K1. The field coil associated with K1 is energized by 180–264 Vac from the output of CB1 if a relay (K1*) on the pilot control board (Paragraph 4.3.8) is closed. When K1 is closed, 180–264 Vac is applied across outlets phase 1, circuit 2, phase 2, circuits 1 and 2, and phase 3, circuit 1 and 2. The 0.1 μF capacitors (C1 and C2), connected across the lines at the relay, reduce the amplitude of voltage spikes at the output of the control when switching inductive loads, thereby preventing interference to nearby electronic data processing equipment.

4.3.8 Pilot Control Board Circuit Description

Figures 4-12 and 4-13 show the pilot control board simplified circuit schematic. The pilot control board contains the circuitry which allows remote turn-on and emergency turn-off of the switched power outlets in both 861 power controller versions. These functions are accomplished by controlling the voltage applied to the field coil of relay K1 in the 861 power controller.

Basically, the circuit consists of a full-wave rectifier loaded by the center-tapped field coil of a relay. Three control lines connect to the board. Pin 3 connects to the center-tapped secondary of the full-wave rectifier transformer. (The center tap is returned to chassis ground through a plug connection.) Pin 2 is the disable (emergency shutdown) line from the signal bus, pin 1 is the enable (power request) line from the signal bus. Two additional lines (from the thermal switch) are connected to the lines associated with pins 3 and 2.

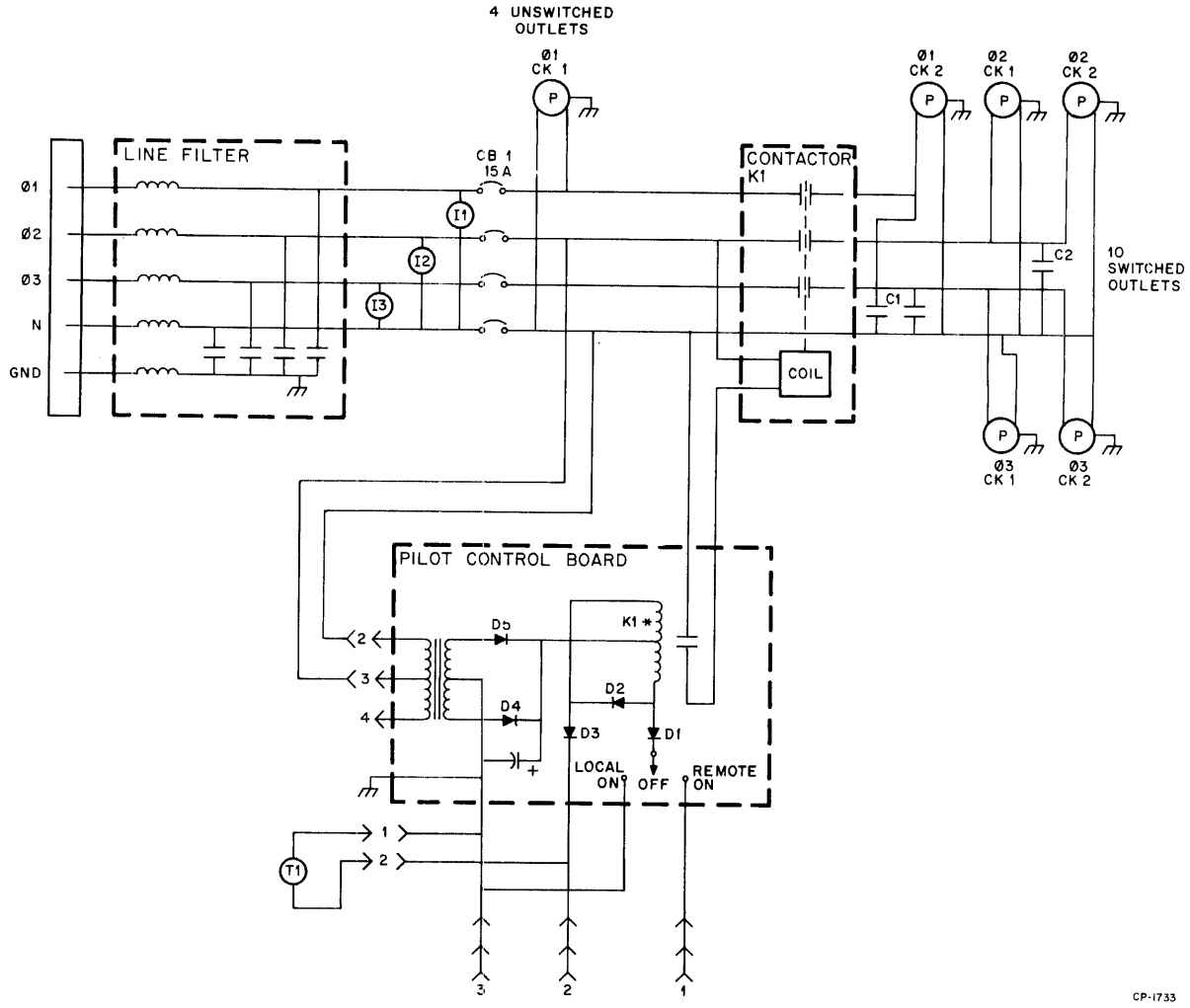


Figure 4-13 861-E Simplified Circuit Schematic

When the LOCAL/OFF/REMOTE switch is in the REMOTE position and pins 3 and 1 are connected, current flows through the lower portion of the center-tapped relay field coil to the full-wave rectifier transformer. This action closes the relay on the pilot control board and causes an energizing potential to be applied across the field coil associated with contactor K1 in the power controller, thereby energizing the controlled outlets. When pins 3 and 2 are connected (emergency shutdown is true), current flows through the lower and upper halves of the center-tapped field coil in different directions before returning to the power supply transformer. The resultant current through the field coil is less than that required for holding the relay closed. Therefore, energizing potential is not present at contactor K1 and power is removed from controlled outlets.

Diode D2 provides a current path in the lower section of the coil to prevent closing the relay in instances where pins 3 and 2 are connected, but no connection exists between pins 1 and 3.

Closing T1 (the thermal switch) performs the same function as emergency shutdown (connects pins 2 and 3 together). This switch is exposed to the ambient air surrounding the power controller. Temperatures above 71° C (160° F) close the switch (disabling the switched outlets). The switch resets automatically when the temperature drops below 49° C (120° F).

Placing the LOCAL/OFF/REMOTE switch in the LOCAL position provides a connection between pin 3 and the lower portion of the coil to energize relay K1, regardless of the state of the power request line on the signal bus. With MJ11 memories, this switch position is normally used for maintenance purposes; operations on the pilot control board are exactly the same for situations where a connection is provided between pins 3 and 1 of the signal bus connector due to closing of a circuit in an external device. MK11 memories require that this switch be in the LOCAL position. A connection between pins 2 and 3 disables the switched outlets, regardless of the position of the LOCAL/OFF/REMOTE switch.

4.3.9 AC Power Distribution

AC power distribution for both the processor and memory cabinets is depicted in Figure 4-2. In the processor cabinet the upper H7420 power supply is connected to a phase 1, circuit 2 outlet on the 861-D/E power controller (Figure 4-14). The lower H7420 uses a phase 2, circuit 1 outlet; those peripheral devices installed in the processor cabinet use phase 3 power. (These are all switched outlets.) The two processor cabinet fans (located at the top of the cabinet) obtain their power from an unswitched outlet on the 861 front panel. The ac power cord for the fans is routed through a terminal block that is attached to the inside surface of the top left part of the cabinet frame. The electrical hook-up at the terminal block is the same for both 115 and 230 Vac systems (Figure 4-14).

Several other devices in the processor cabinet use ac power from the 861-D/E power control. They are the transformer and regulator fans in both H7420s, the elapsed time meter (located at the rear of the cabinet), and the upper and lower processor box logic fans (Figure 4-2). The source of 115 Vac power for these devices is two terminal blocks (TB1) located in the upper and lower H7420s. The electrical jumper configuration at these terminal blocks is determined by the input voltage to the H7420: 115 Vac from an 861-D or 230 Vac from an 861-E (see note on Figure 4-14).

In the memory cabinet, the memory power supply obtains its power from a phase 3 switched outlet on the 861-D/E. Additional memory frames use phase 1 and phase 2 switched power from the 861 (Figure 4-8). Several connections in the memory (at two terminal blocks in the transformer assembly) provide 115 Vac to internal cooling fans (drawing E-AD-7010694-0-0).

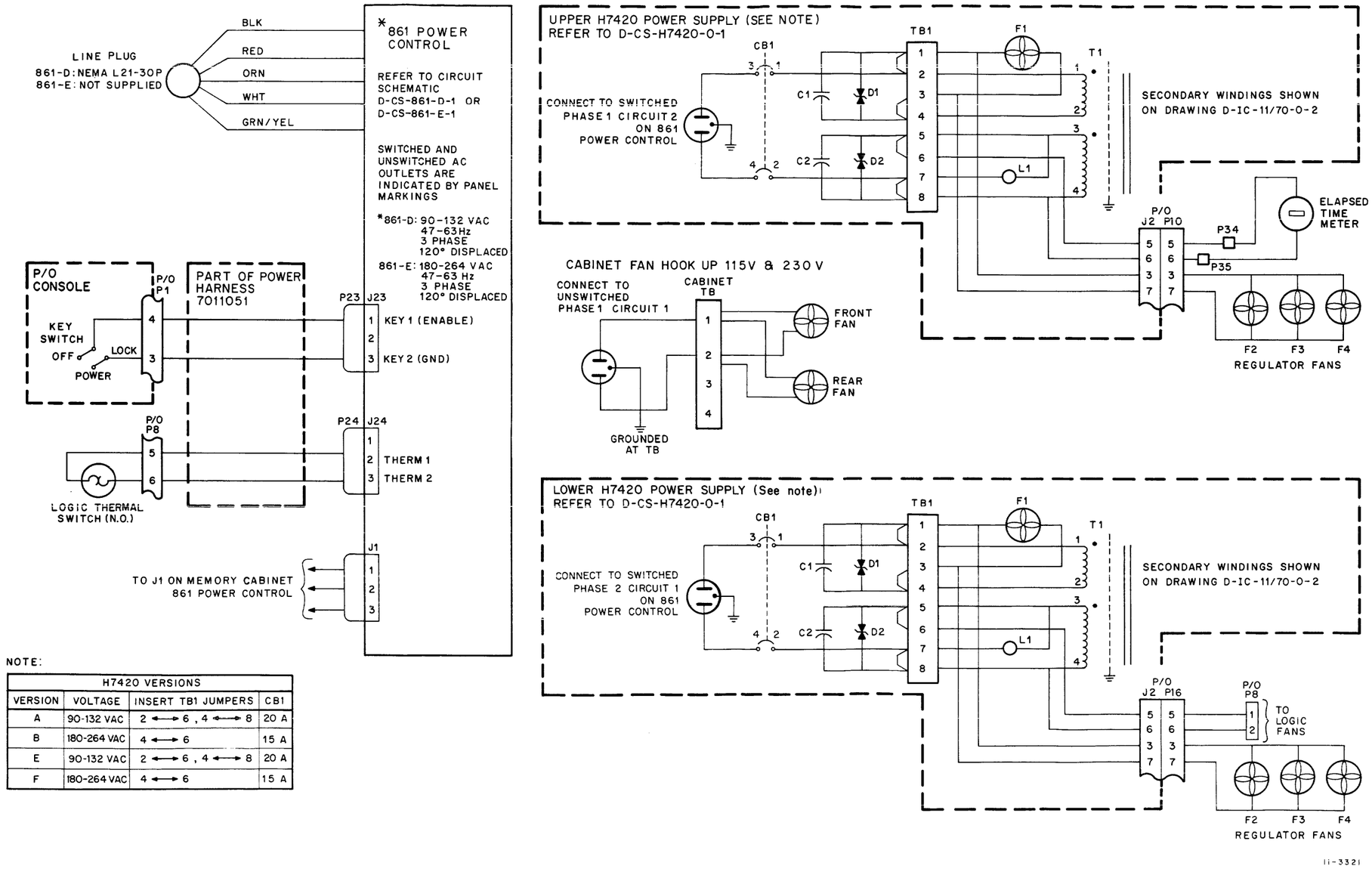
The distribution of the 20-30 Vac output of the H7420 and MJ11 transformer secondaries is described in Paragraphs 4.4.4 (for the H7420), and 4.4.7 (for the MJ11) and 4.4.7 (for the MK11).

4.4 DC POWER, H7420, MJ11, and MK11 POWER SUPPLIES

Switched ac power from the 861-D/E power controls in the processor and memory cabinets is routed to the H7420 and memory power supplies that generate the required dc voltage for the system (Figure 4-2, 4-3, 4-4, and 4-5).

4.4.1 DC Power Distribution

The outputs from the H7420 and MJ11 power supplies are channeled through three wire harnesses to the processor console and the processor and memory backplanes. AC power to the logic fans, to the elapsed time meter, and to the MJ11 voltage regulators is also sent through two of these harnesses (Figure 4-2).



NOTE:

H7420 VERSIONS			
VERSION	VOLTAGE	INSERT TB1 JUMPERS	CB1
A	90-132 VAC	2 ⟷ 6 , 4 ⟷ 8	20 A
B	180-264 VAC	4 ⟷ 6	15 A
E	90-132 VAC	2 ⟷ 6 , 4 ⟷ 8	20 A
F	180-264 VAC	4 ⟷ 6	15 A

Figure 4-14 AC Power Connections (Processor Cabinet)

4.4.2 Power Distribution Cable Harnesses

Three power distribution harnesses are used in the PDP-11/70: one in the processor cabinet, 7011051 (Figure 4-15) and two in the memory cabinet, 5010580 and 5010581 (Figure 4-16). In general, the power harness connectors are assigned a number with a "P" prefix; e.g., P1, P2, etc., whereas the connectors attached to the hardware (regulators, backplanes, etc.) have a "J" prefix. Several exceptions to this can be noted on Figure 4-15. These harnesses contain several different types of Mate-N-Lok connections (both male and female). They are shown in detail on drawings D-IA-7010580-0-0, D-IA-7010581-0-0 and D-IA-7011051-0-0. Figures 4-17, 4-18, and 4-19 are photographs of the processor and memory cabinets that show the harnesses in relation to the power supplies.

The 7010580 power distribution harness interconnects the transformer assembly, regulators, and the memory backplane. The harness routes 30 Vac to the regulators and regulated dc voltage to the memory backplane.

The 7010581 harness interconnects the transformer assembly, the 5411086-YA power line monitor board, and the memory backplane. The harness routes 30 Vac to the power line monitor board, and power fail signals (AC LO and DC LO) to the memory backplane.

4.4.3 MJ11 Backplane Power Distribution

Processor cabinet power is applied to the processor backplane via the power harness to ten connectors (Figure 4-15). Six are voltage inputs (P2 through P7) and four are ground connections (P25 through P28). Ground is established through three connectors (from P25, P27, and P28) fastened to the backplane with the wire harness cable clamps. A separate plug (P1) on te harness (Figure 4-20) is the power and signal connection to the processor console (J4). An additional plug (P8) provides a connection for power to the five upper and four lower processor mounting box fans. P8 also connects the thermal switch in the mounting box to the 861 power control. The processor backplane row and slot assignments are shown in Figure 4-20; backplane connectors and pins are shown in Figure 4-21. Table 4-5 lists all the processor cabinet power and signal connections. These connections are also shown on drawing D-IC-11/70-0-2.

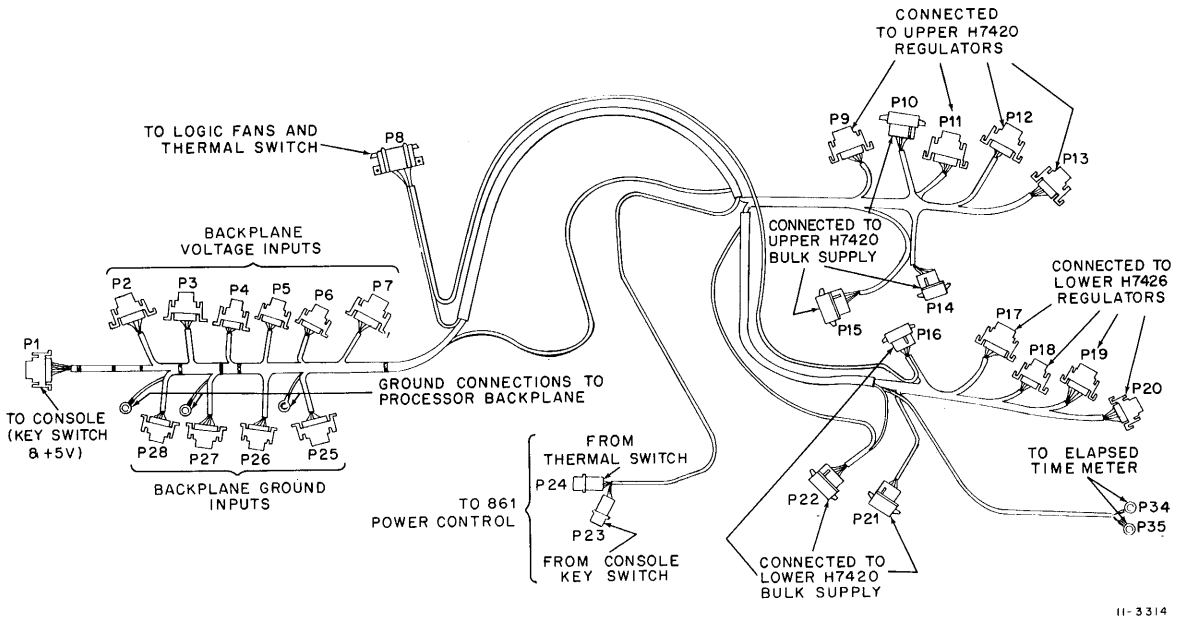
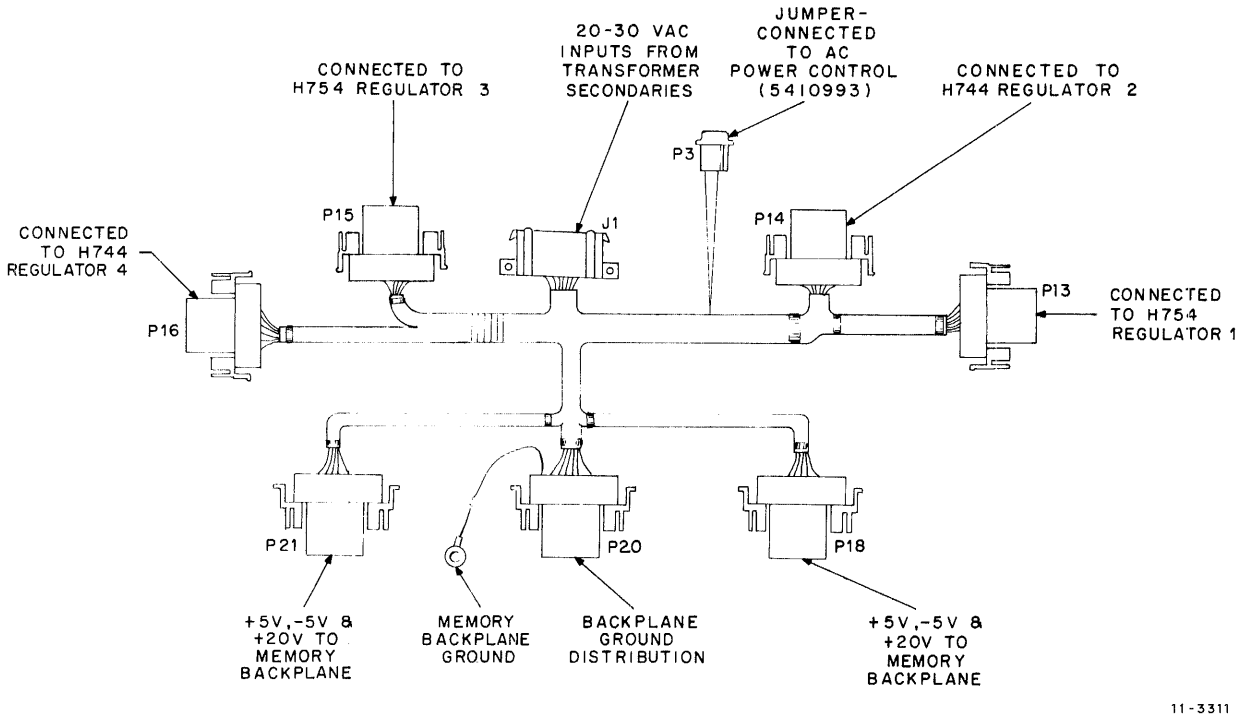
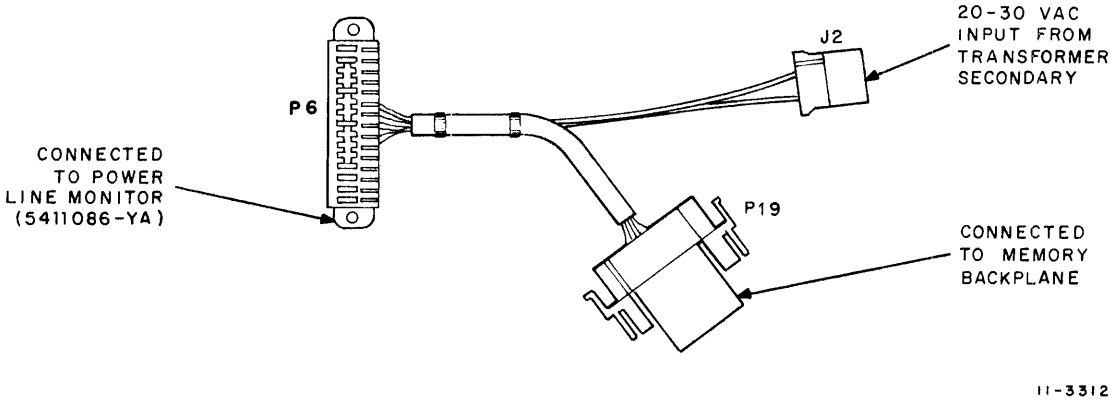


Figure 4-15 Power Distribution Cable Harness (Processor Cabinet) 7011051



Power Harness Assembly 5010580



AC LO DC LO Wire Harness Assembly 5010581

Figure 4-16 Power Distribution Cable Harnesses (Memory Cabinet)

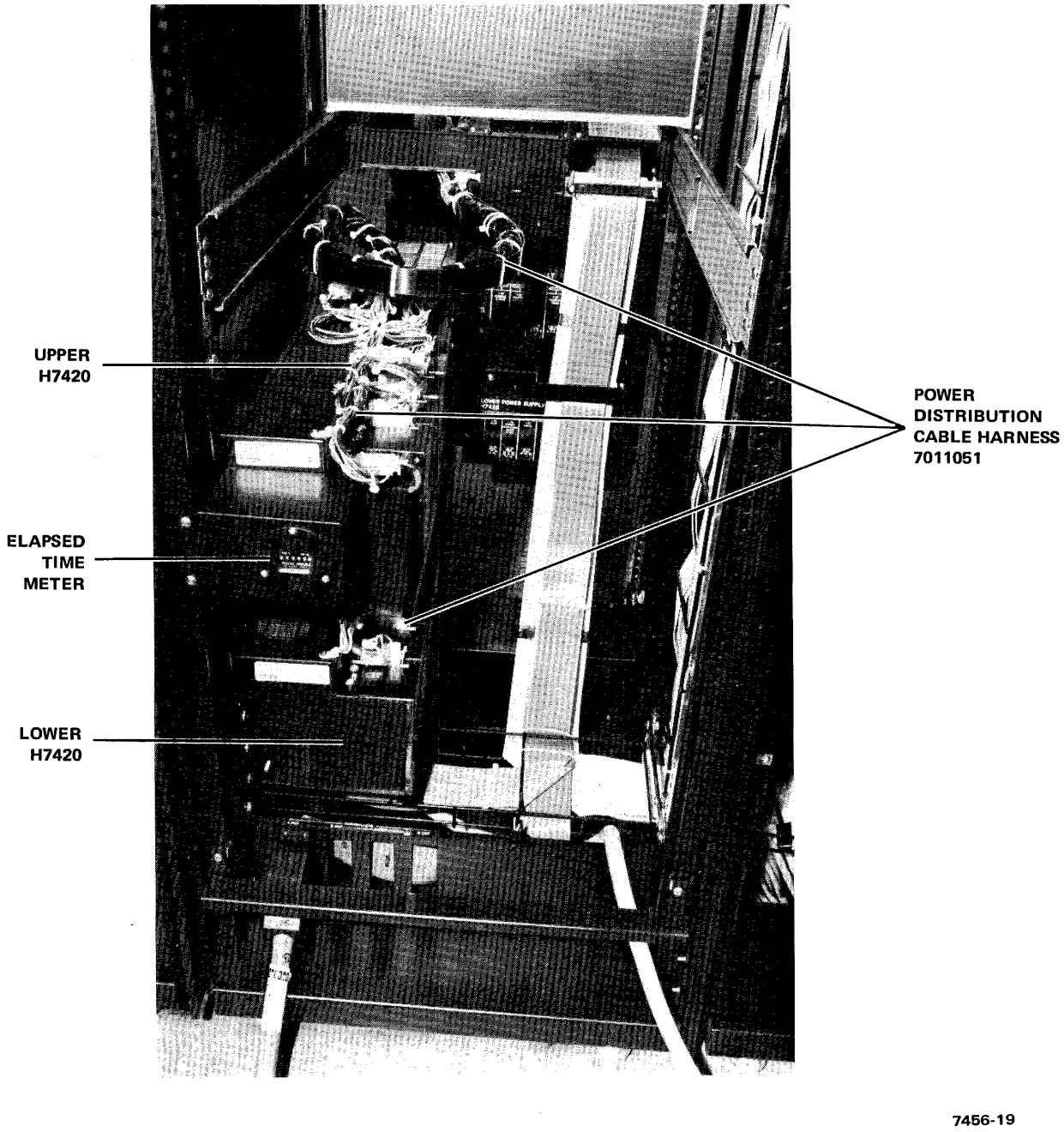


Figure 4-17 Processor Cabinet (Processor Mounting Box Extended)

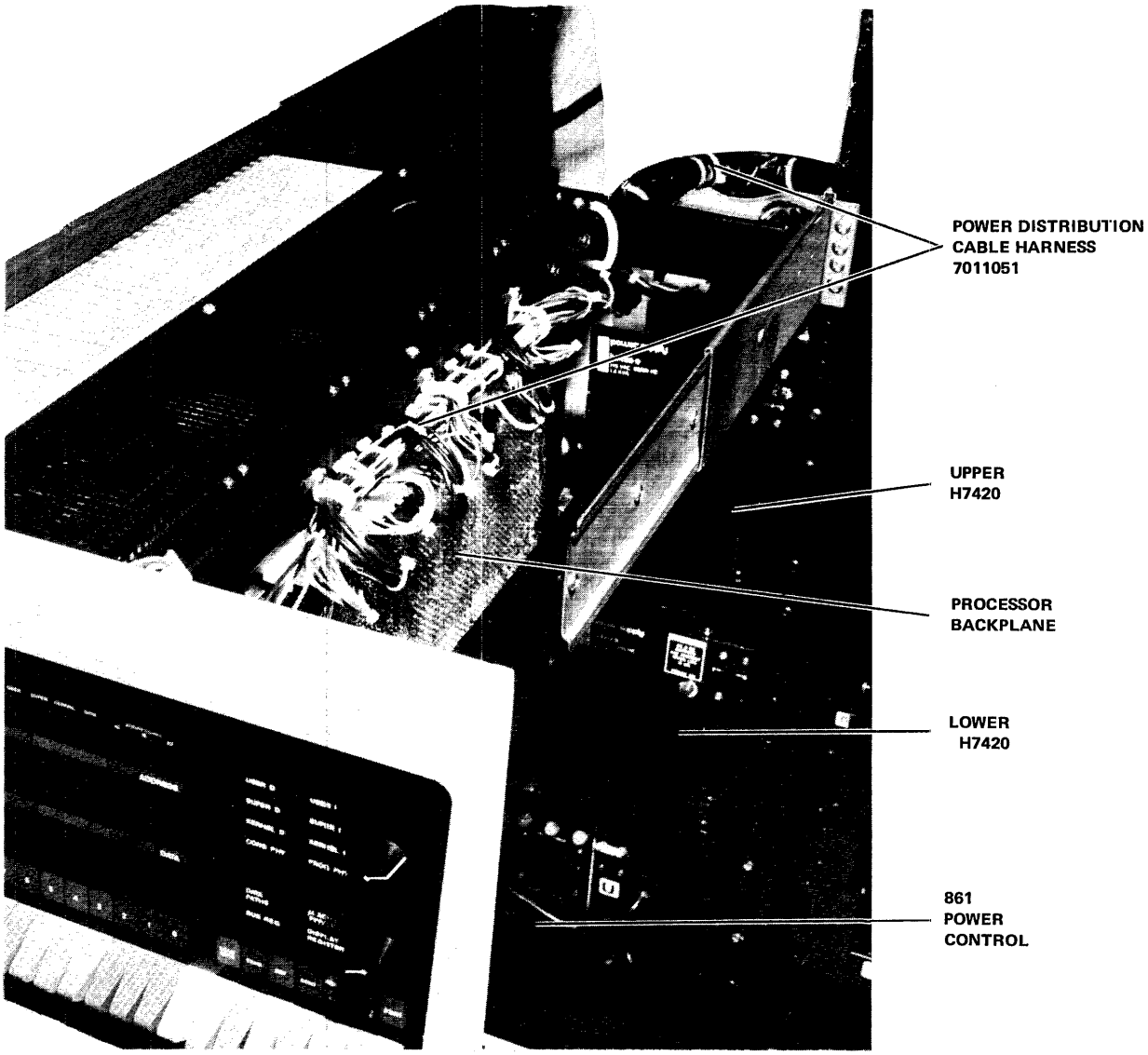


Figure 4-18 Processor Mounting Box

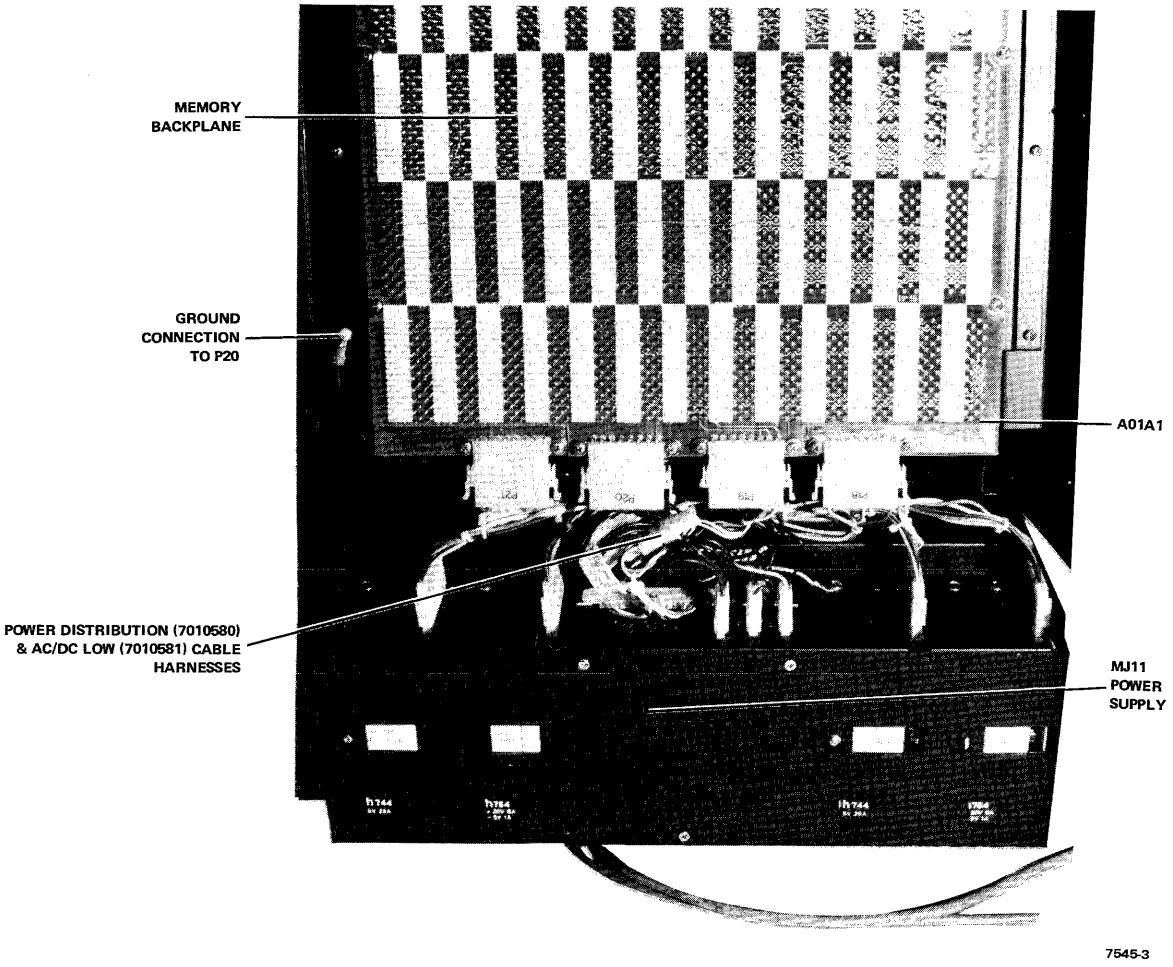
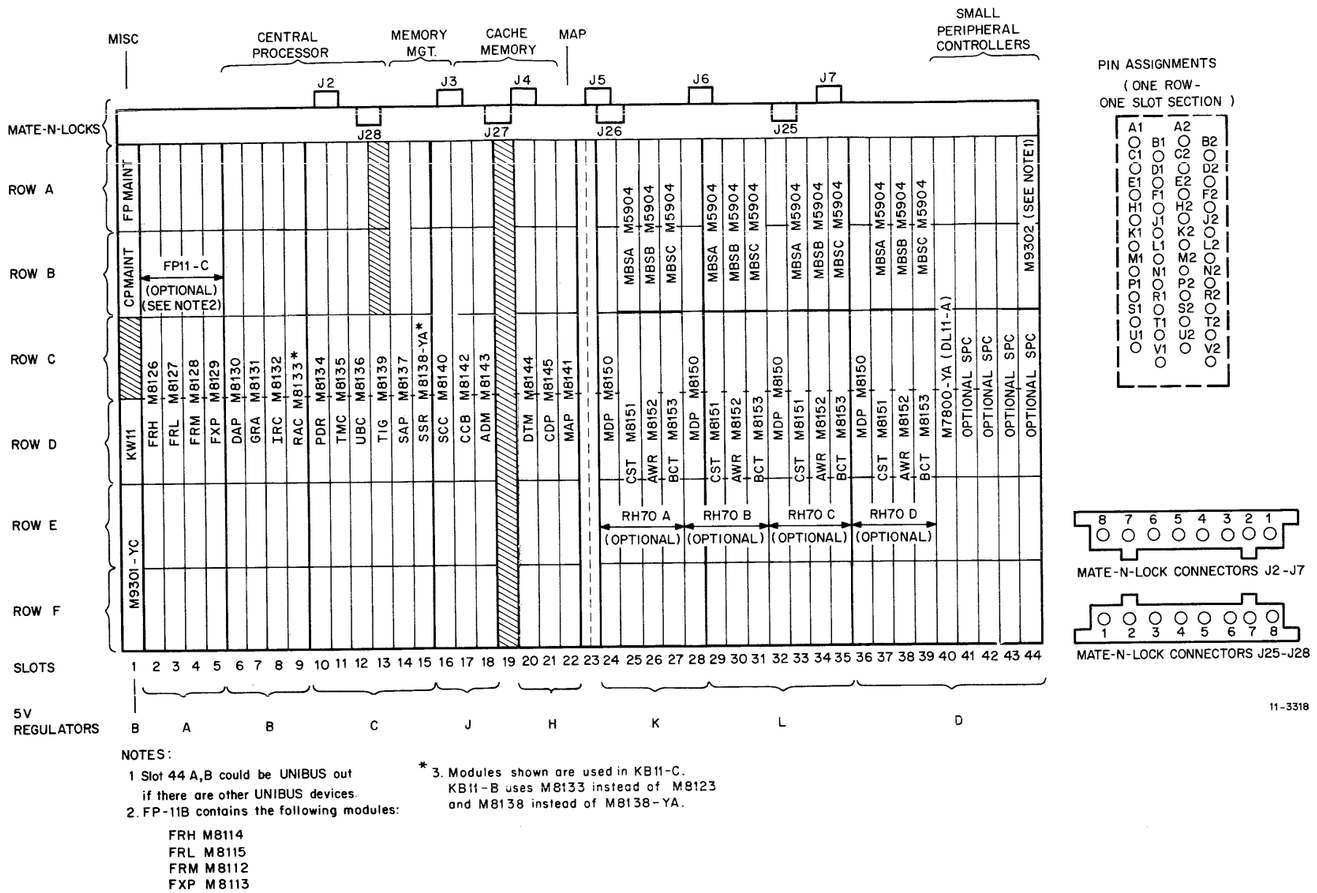


Figure 4-19 Memory Cabinet Power Supply (Bottom View)

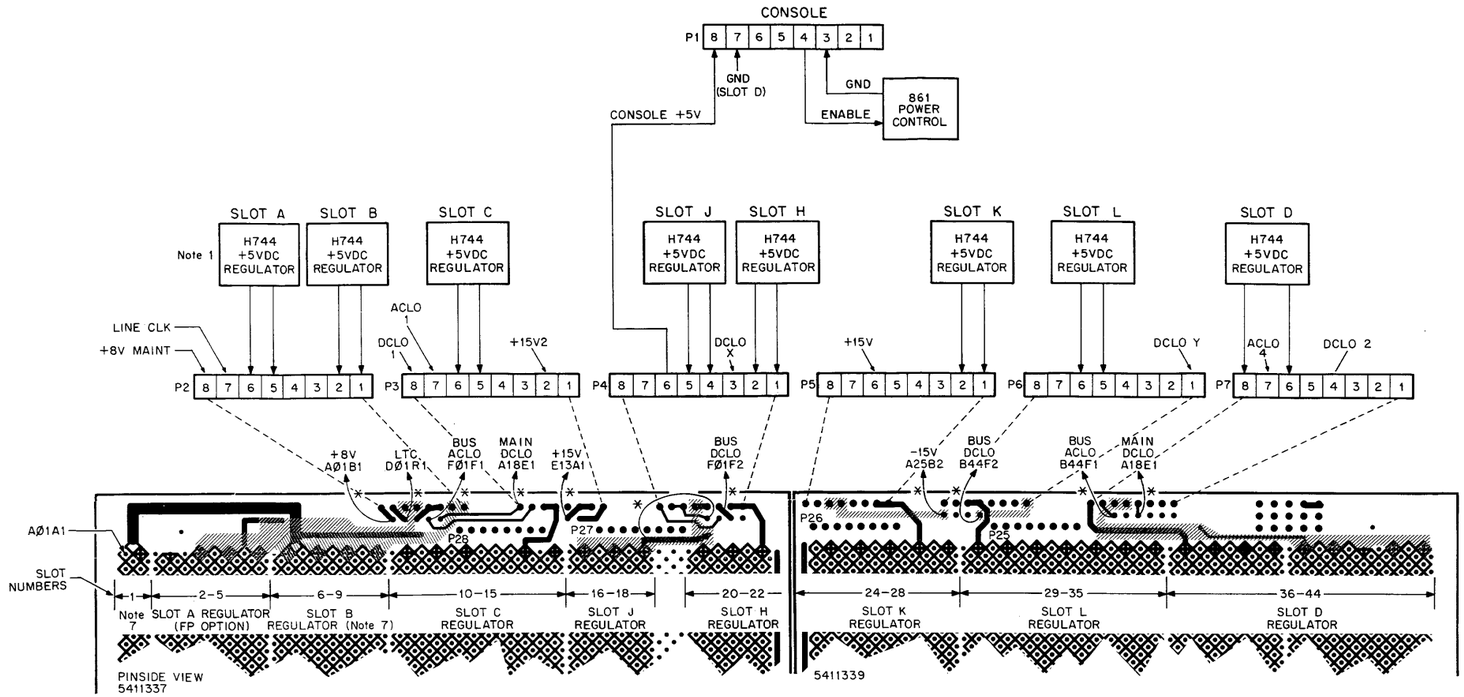


NOTES:

1. Slot 44 A,B could be UNIBUS out if there are other UNIBUS devices.
2. FP-11B contains the following modules:
   - FRH M8114
   - FRL M8115
   - FRM M8112
   - FXP M8113

* 3. Modules shown are used in KB11-C. KB11-B uses M8133 instead of M8123 and M8138 instead of M8138-YA.

Figure 4-20 KB11-B,C Processor Backplane Slot and Row Assignments (Pin Side View)



NOTES:

1. Used only if FP11 option is installed.
2. *Electrical Connection.
3. P25 through P28 are ground connections. (Refer to D-IC-11/70-0-2)
4. Shaded etch connections are on connector side.
5. -15 V, DCLO 2, and DCLO X are from lower H7420.
6. +8 V, +15 V, ACLO 1, DCLO Y, ACLO 4, LINE CLOCK, and DCLO 1 are from upper H7420.
7. Slot B regulator provides power to slots 1, 6-9.

11-3201

Figure 4-21 Processor Backplane Connectors and Pins

Table 4-5 Processor Cabinet Voltage/Signal Connections (Refer to Figures 4-19 and 4-20)

Voltage/ Signal	H744 Regulator	Regulator Plug-Pin	Backplane Plug-Pin	Processor/ Modules
+5 V	Slot A	P9-2, 5	P2-5, 6	Slots 2-5
	Slot B	P11-2, 5	P2-1, 2	Slots 1, 6-9
	Slot C	P12-2, 5	P3-5, 6	Slots 10-15
	Slot D	P13-2, 5	P7-6, 8	Slots 36-44
	Slot H	P17-2, 5	P4-1, 2	Slots 20-22
	Slot J	P18-2, 5	P4-4, 5	Slots 16-18 Also to processor console (P1-8) via P4-6
	Slot K	P19-2, 5	P5-1, 2	Slots 24-28
	Slot L	P20-2, 5	P6-5, 6	Slots 29-35
Ground	Slot A	P9-3, 4	P28-1, 2	All ground connections are common
	Slot B	P11-3, 4	P28-3, 4	
	Slot C	P12-3, 4	P28-5, 6	
	Slot D	P13-3, 4	P1-7; P27-4	
	Slot H	P17-3, 4	P25-1, 2	
	Slot J	P18-3, 4	P27-1, 2	
	Slot K	P19-3, 4	P25-3, 4	
	Slot L	P20-3, 4	P25-5, 6	
Voltage/ Signal	**H7420 Power Supply**	**Power Supply Plug-Pin**	**Backplane Plug-Pin**	**Processor/ Modules**
	Upper	P15-5	P28-8	
	Lower	P22-2, 3	P26-5	
Logic Ground	Upper	P15-7	P26-1	
	Lower	P22-7	P26-2	
+15 V	Upper	P15-3	P3-2, 3	Slots 40-44
-15 V	Lower	P22-4	P5-5,6	Slots 2, 17, 25-27, 29-31, 33-35, 37-44
+8 V	Upper	P15-1	P2-8	Slot 1 (CP Maintenance card)
Line Clock (LTC)	Upper	P15-11	P2-7	Slot 1 (KW11)
Bus AC LO L	Upper	P15-8	P3-7	Refer to Figure 4-37 for complete AC LO, DC LO Circuit
	Lower	P22-10	P3-7	

Table 4-5 Processor Cabinet Voltge/Signal Connections (Cont)

Voltage/ Signal	H7420 Power Supply	Power Supply Plug-Pin	Backplane Plug-Pin	Processor/ Modules
BUS AC LO L (Cont)	Upper Lower	P15-10 P22-8	P7-7 P7-7	
Bus DC LO L	Upper Lower	P15-9 P22-12	P6-1 P4-3	
Main DC LO L	Upper Lower	P15-12 P22-9	P3-8 P7-4	
Voltage/ Signal	**H7420 Power Supply**	**Power Supply Plug-Pin**	**Regulator Plug-Pin**	**Remarks**
20-30 Vac	Upper Lower	P10-1, 2 P14-1, 2 P14-7, 8 P10-8, 10 P21-7, 8 P21-1, 2 P16-8, 10 P16-1, 2	P9-6, 7 P11-6, 7 P12-6, 7 P13-6, 7 P17-6, 7 P18-6, 7 P19-6, 7 P20-6, 7	Regulator A Regulator B Regulator C Regulator D Regulator H Regulator J Regulator K Regulator L
Voltage/ Signal	**H7420 Power Supply**	**Power Supply Plug-Pin**	**H7420 Fan Connections**	**Remarks**
115 Vac	Upper	P10-3, 7	J10, J11 J8, J9 J6, J7	Upper H7420, Fan 2 Upper H7420, Fan 3 Upper H7420, Fan 4
	Lower	P16-3, 7	J10, J11 J8, J9 J6, J7	Lower H7420, Fan 2 Lower H7420, Fan 3 Lower H7420, Fan 4
Voltage/ Signal	**H7420 Power Supply**	**Power Supply Plug-Pin**	**Processor Cabinet Plug**	**Remarks**
	Upper	P10-5, 6	P34, P35	Elapsed Time Meter
	Lower	P16-5, 6	P8-1, 2	9Processor mounting box logic fans

Two plugs on the processor power harness, Pv3 and P24, connect the console ON/OFF switch (via P1) and the thermal switch (via P8) to the 861 power control (Figure 4-14).

Fourteen of the harness connectors are attached to the upper and lower H7420s. Seven (P9 through P15) go to the upper H7420 and seven (P16 through P22) go to the lower H7420. Figure 4-3 shows how the processor power harness plugs connect the backplane to the H7420s. The two remaining connectors on this harness, P34 and P35, are used to apply ac power to the elapsed time meter (Figure 4-17).

Memory cabinet power is distributed to the memory backplane via the power harness. The harness contains nine connectors (Figure 4-16). Two connectors (P18 and P21) apply dc voltage to the backplane (Table 4-6). A third connector (P20) is for ground distribution that originates at a chassis ground connection on the backplane (Figure 4-19). At the MJ11 power supply, four connectors (P13 through P16) are attached to the voltage regulators and one connector (J1) routes the ac input from the transformer secondary to the four regulators. The last connector on the harness is P3, which is functionally separate from the others. P3 is attached to the ac power control board in the MJ11 and contains a single shorting loop. This loop maintains the MJ11 in the ON mode during normal operation (Figure 4-2 and drawing E-AD-7010694-0-0).

Table 4-6 MJ11 Memory Cabinet Voltage/Signal Connections (Refer to Figure 4-21)

Voltage/Signal	Wire Color	Regulator	Regulator Plug Pin	Backplane Plug Pin
+5 V	Red	H744 (No. 4) H744 (No. 2)	P16-2,5 P14-2,5	P21-5,6,7,8 P18-1,2,3,4
+20 V	Orange	H754 (No. 3) H754 (No. 1)	P15-5 P13-5	P21-3,4 P18-5,6
-5 V	Brown	H754 (No. 3) H754 (No. 1)	P15-3 P13-3	P21-1,2 P18-7,8
Ground	Black	H754 (No. 1) H744 (No. 2) H754 (No. 3) H744 (No. 4) 5411086-YA	P13-2 P14-3,4 P15-2 P16-3,4 P6-4,11	(Note) P20-3 P20-4,5 P20-7 P20-6,8 P19-4,5
DC LO	Violet	5411086-YA	P6-1,2	P19-6,7
AC LO	Yellow	5411086-YA	P6-3, 8	P19-8

NOTE: Ground connections on J20 and J19 (layer 3) are common to each other. P20-2 is connected to chassis ground on the backplane (Figure 4-19).

A second wire harness is routed adjacent to the memory power harness in the MJ11. This is the ac/dc low wire harness (Figure 4-16). It is used to convey AC LO and DC LO power fail signals from the 5411086-YA low voltage detection circuit to the memory backplane, and ac power from the transformer to the 5411086-YA. Three connectors, P6, J2, and P12, are used for these functions.

Figure 4-22 depicts the MJ11 power supply and memory backplane connections made with the two wire harnesses (7010850 and 7010851) just described. In the drawing the four backplane layers are separated to show where each signal/voltage is applied. Layer four is the one observed when the backplane is viewed from the bottom (pin side). Some jack pins are common to each other due to an electrical connection on the associated backplane layer. Consequently, a voltage or signal may be present at more than one jack pin even though it is sent to just one plug pin. For example, –5 V is sent to P21-1 from regulator 3. However, –5 V is present at both J21-1 and J21-2 because of an etch connection on layer one between these two pins. Figure 4-23 is a cross-sectional view of this part of the backplane. Table 4-6 lists the backplane pins that are common to a particular voltage or signal. Pin A01A1, identified on each layer (Figure 4-22) to illustrate exactly how the four layers are overlayed, is in the lower right corner of the backplane when the memory drawer is in the raised (maintenance) position (Figure 4-19).

Drawing E-UA-MJ11-0-0 is a more comprehensive view of the backplane wire connections.

4.4.4 Processor Cabinet DC Power Supply (H7420)

The upper and lower H7420 power supplies in the processor cabinet provide the processor with the required dc voltage and low voltage signals. Each H7420 consists of a multiple output transformer, a power line monitor, 15 V regulator, and cooling for up to five H744 +5 V power supply modules. Figure 4-24 is a simplified schematic drawing of the two H7420s in the processor cabinet (only the unique parts of the lower H7420 are shown) and their connections to the processor cabinet, processor console, and processor backplane.

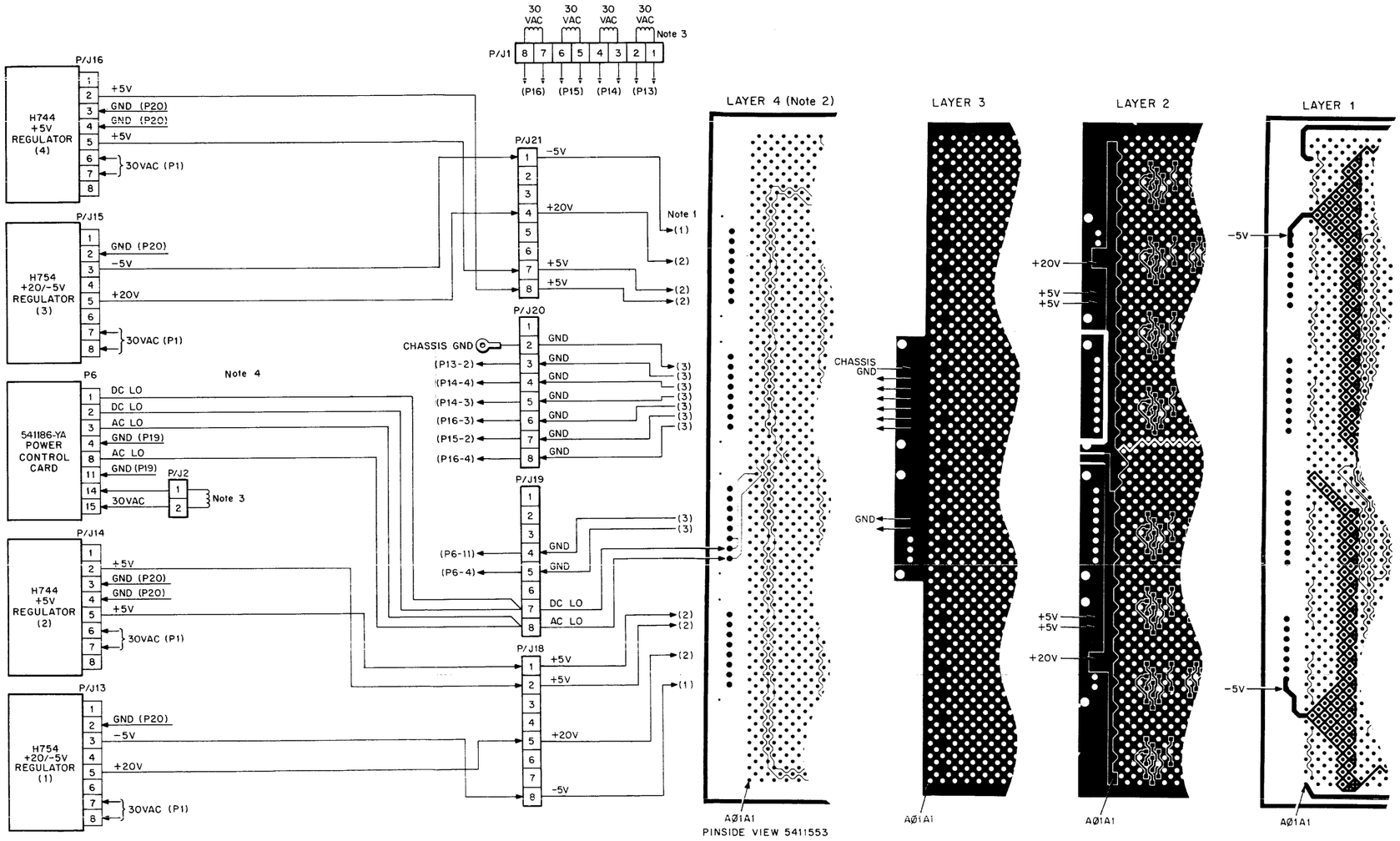
Figure 4-25 is a photograph of an H7420 with four regulators installed. In Figure 4-26, all the regulators have been removed and the top cover and the PC mounting board bracket have been detached to show the interior of the H7420. A front view of the power supply is shown in Figure 4-27.

Four versions of the H7420 are made: A, B, E, and F. The major differences are listed in Table 4-7.

The 115/230 Vac power input to the H7420 is through a circuit breaker (CB1) and a terminal block (TB1). (Refer to this part of the power supply on Figure 4-14). In the A and E versions, CB1 is a 20 A circuit breaker; the B and F versions use a 15 A circuit breaker. TB1 contains eight double terminals; adjacent terminal pairs are common as shown in Figure 4-28. In addition, jumpers are installed (Table 4-7) to provide 115 Vac outputs with either a 115 Vac or a 230 Vac input. Simplified circuit drawings of the two jumper-transformer configurations are shown on Figure 4-24. Also connected to TB1 are two capacitor-varistor assemblies (C1 and D1, C2 and D2) that function as input surge limiters.

The 115 Vac outputs from TB1 are connected to the two transformer primary windings, the regulator, and processor logic cooling fans, the elapsed time meter and the power indicator light (Figures 4-17, 4-26, and 4-27). The externally used outputs and the 115 Vac for the regulator fans are routed through J2 on the H7420 box (Figure 4-25).

The transformer secondary windings are connected to J2 (15-pin Mate-N-Lok) and J3 (9-pin Mate-N-Lok) on the H7420 box, and J5 (2-pin Mate-N-Lok). The output to J5 is the only one that is fused. These transformer outputs are 20–30 Vac (26 Vac is the nominal voltage). The two wires from P5 (J5) are routed to J1 (15 pin Molex right angle edge connector) on the 5411086 board (Figure 4-26).



NOTES:

1. Numbers denote backplane layer connected.
2. Layer 4 is the pinside layer.
3. Power transformer secondary.
4. Harness 7010581 connects P6 with P2 and P19. All other wires are contained in harness 7010580.

TK-1791

Figure 4-22 Memory Backplane Connectors and Pins

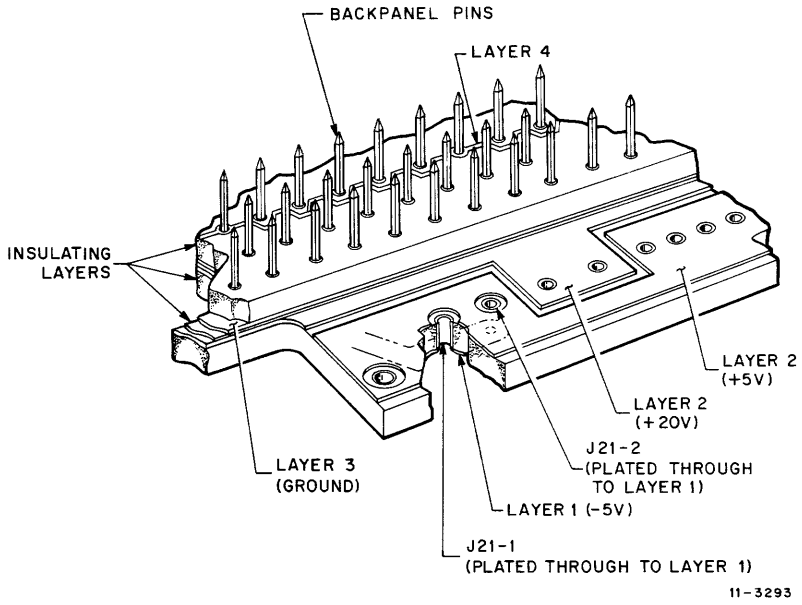
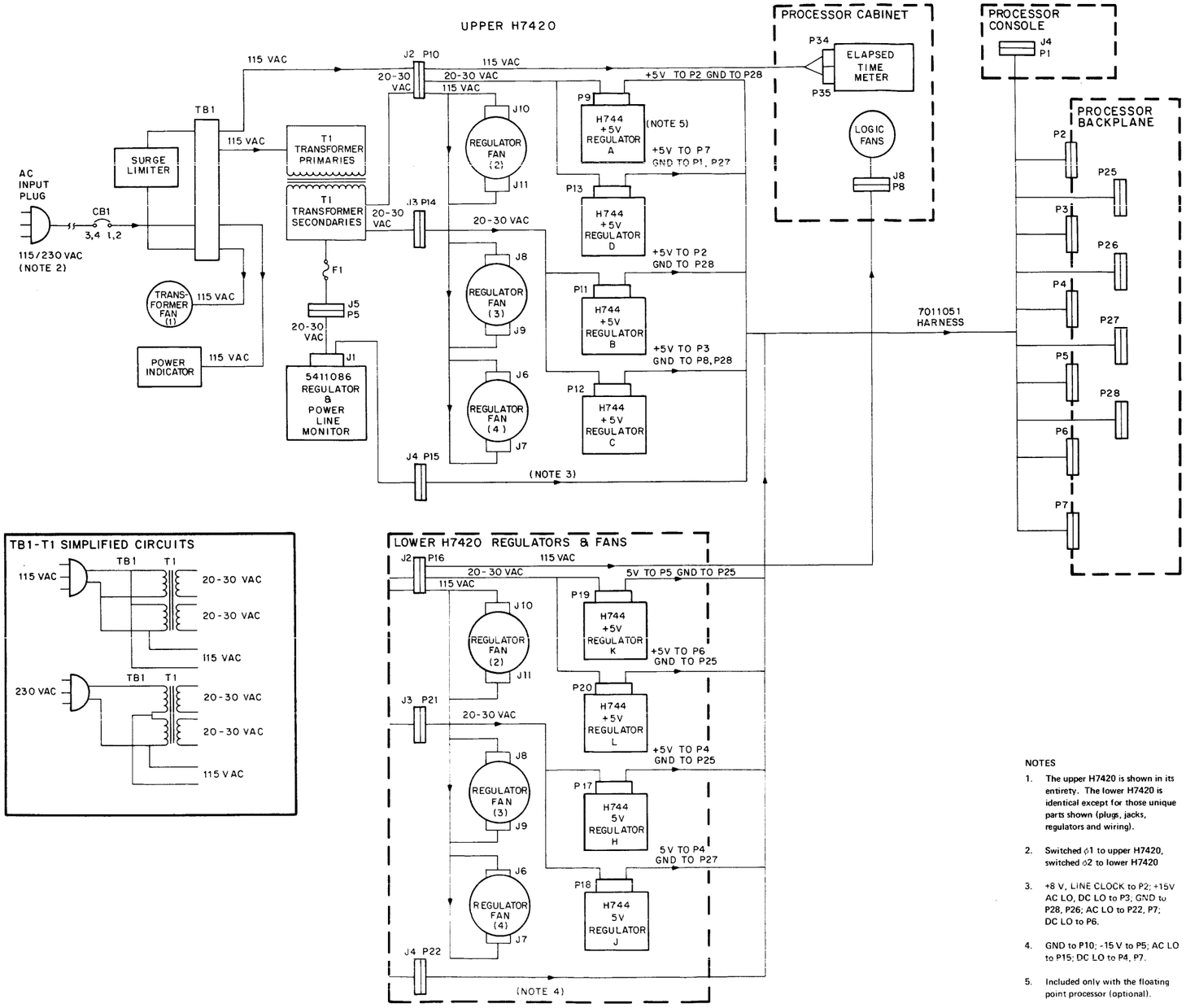


Figure 4-23 Memory Backplane Cross Section

Table 4-7 H7420 Versions

Version	Voltage	CB1	TB1 Jumper Connections	Apparent input Power (kVA max)
A	90-132 Vac	20 A	2-6, 4-8	1.44
B	180-264 Vac	15A	4-6	1.68
E	90-132 Vac	20A	2-6, 4-8	1.44
F	180-264 Vac	15 A	4-6	1.44

Version	Transformer Assy – DEC No.	Max Transformer Output Load*	Max No. Regulators
A	7011211	1220 VA	5
B	7011211	1220 VA	5
E	7010814	1020 VA	4
F	7010814	1020 VA	4



NOTES

1. The upper H7420 is shown in its entirety. The lower H7420 is identical except for those unique parts shown (plugs, jacks, regulators and wiring).
2. Switched ϕ1 to upper H7420, switched ϕ2 to lower H7420
3. +8 V, LINE CLOCK to P2; +15V AC LO, DC LO to P3; GND to P28, P26; AC LO to P22, P7; DC LO to P6.
4. GND to P10; -15 V to P5; AC LO to P15; DC LO to P4, P7.
5. Included only with the floating point processor (optional).

11-3320

Figure 4-24 H7420 Power Supply

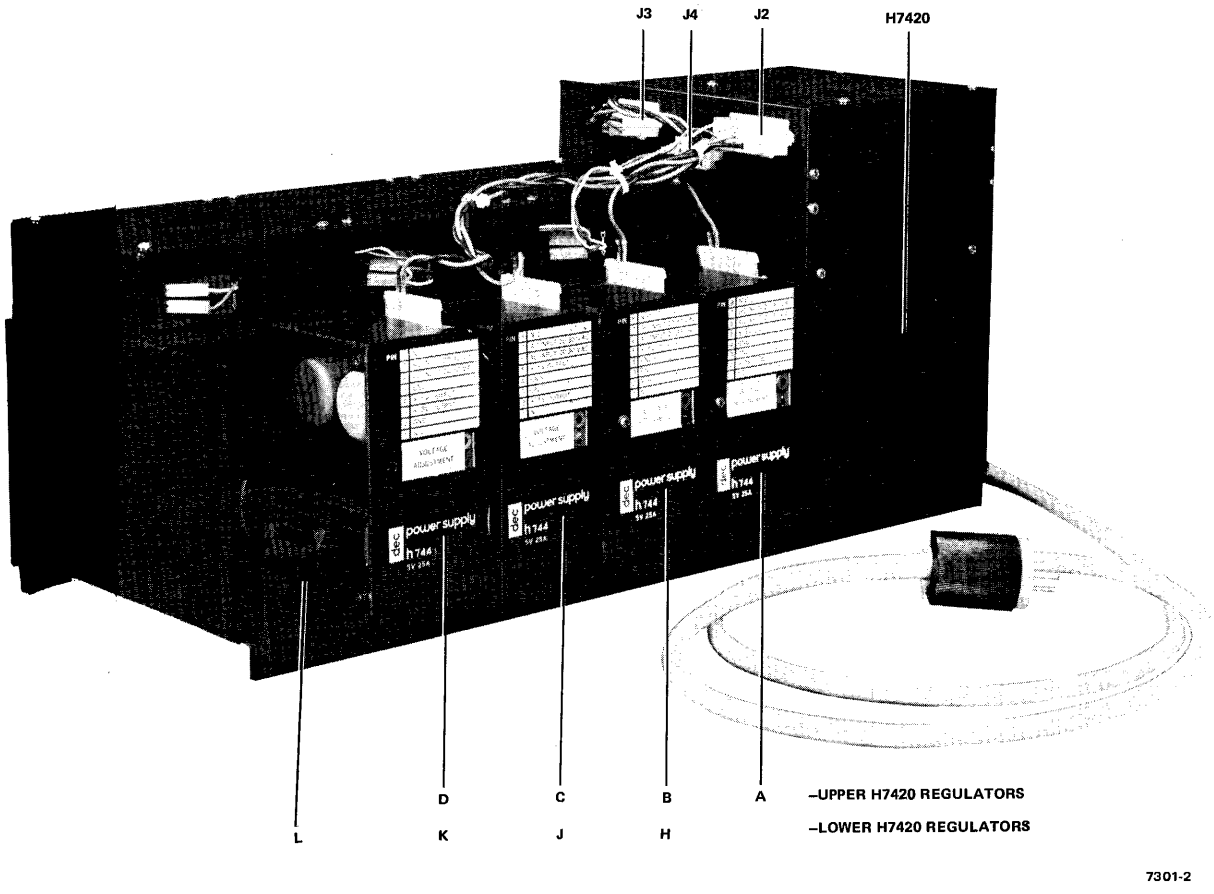


Figure 4-25 H7420 Power Supply with Regulators

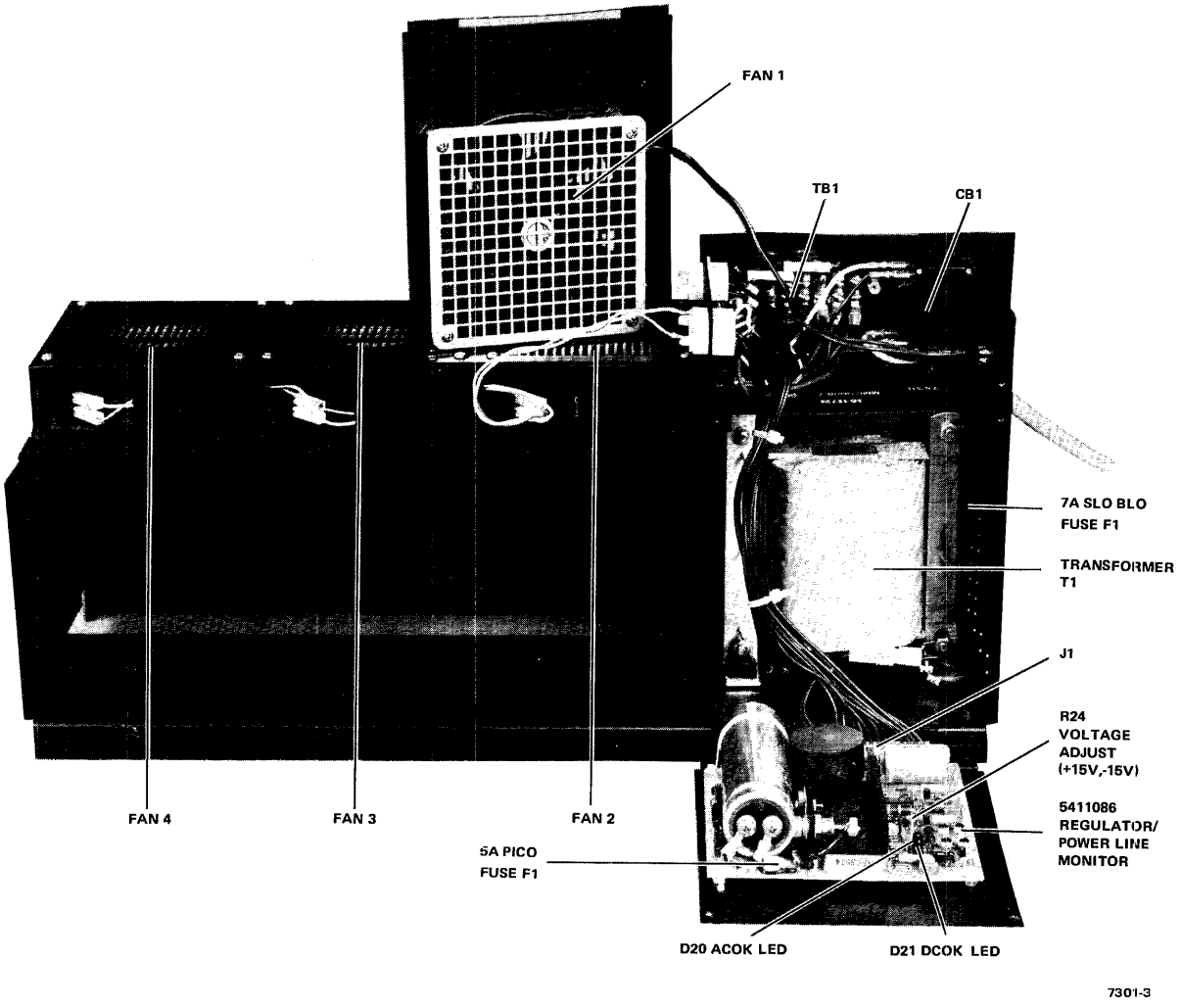


Figure 4-26 H7420 Power Supply (PC Mounting Board Bracket with Top Cover Removed)

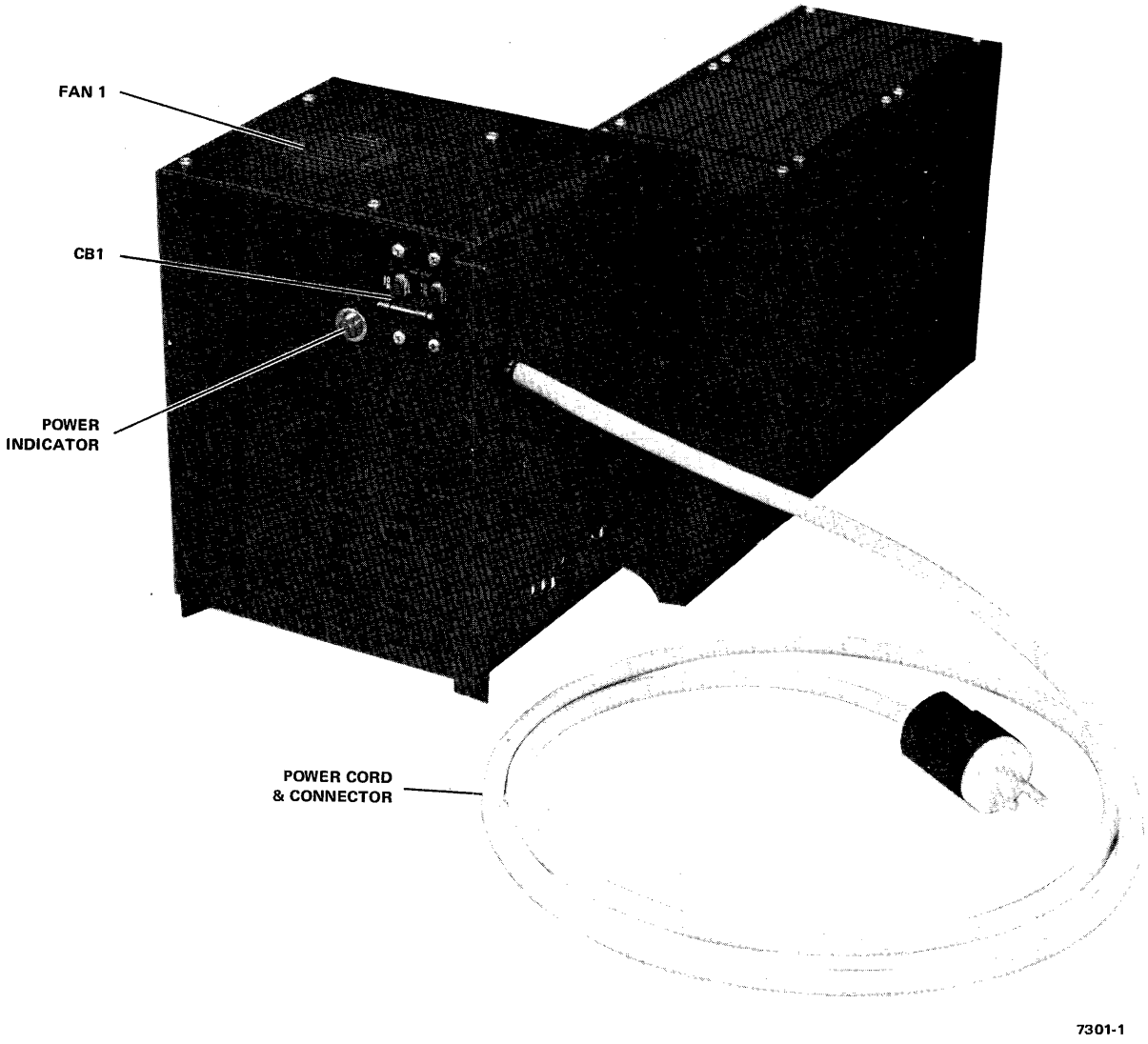


Figure 4-27 H7420 Power Supply, Front View

J2 and J3 are mated with P10 and P14 respectively, in the upper H7420 and P16 and P21 in the lower H7420. The 20–30 Vac wires from these plugs are connected to the seven (or eight if the floating point option is installed) H744 regulators in the H7420.

The 5411086 regulator and line monitor boards – one in each H7420 – furnish +8 V, –15 V, and +15 V along with AC LO and DC LO power fail signals to the processor backplane (notes 1 and 2 on Figure 4-23). These outputs are through two 12-pin Mate-N-Lok connectors on the H7420 boxes: J4/P15 on the upper H7420, and J4/P22 on the lower H7420. The 5411086, including the AC LO and DC LO circuits, is described in Paragraph 4.4.6.1.

Four 4-inch, sleeve bearing fans provide air flow to cool each H7420. One is mounted above the transformer assembly and three are mounted above the H744 regulators (Figures 4-24, 4-25, and 4-27). The regulator fans receive 115 Vac power through six connectors, J6 through J11. Additional fan specifications follow.

A minimum of seven H744, +5 V regulators are included in the processor cabinet power system: three in the upper H7420 and four in the lower H7420. The upper H7420 regulators occupy slots B, C, and D; the lower H7420 regulators use slots H, J, K, and L (Figures 4-24 and 4-25). An additional H744 is installed in slot A of the upper H7420 if the optional floating point processor is included in the PDP-11/70. An 8-pin Mate-N-Lok connector on each regulator is used for both the 20–30 Vac input, and the +5 V output to the processor backplane. The connectors for the upper H7420 regulators are P9 and P11 through P13. For the lower regulators, they are P17 through P20 (Table 4-5). These connectors, as well as the connectors on the backplane, and the associated wires, are contained in the 7011051 power harness (Figures 4-15, 4-17, and 4-24). The H744 regulator is described in Paragraph 4.4.6.2.

To convert a 240 Vac version H7420 to a 120 Vac version, or a 120 Vac version to a 240 Vac version, it is necessary to change the following components:

1. Circuit breaker CB1
2. The jumper configuration on TB1
3. The line cord and connector
4. The decal

Refer to Table 4-7 and Figures 4-28 and 4-65 for component sizes and locations. Illustrated Parts Breakdown (IPB) EK-H7420-IP-001 lists the appropriate part numbers.

NOTE

The H7420 A and B versions can be converted to E and F versions, but not vice versa. This is because the E and F versions can supply 20–30 Vac to a maximum of four regulators; the A and B versions may be equipped with up to five regulators.

4.4.5 H7420 Power Supply Specifications

Specifications for the H7420 are listed in Table 4-8. Reference should be made to engineering specification A-SP-H7420-0-2 for additional information.

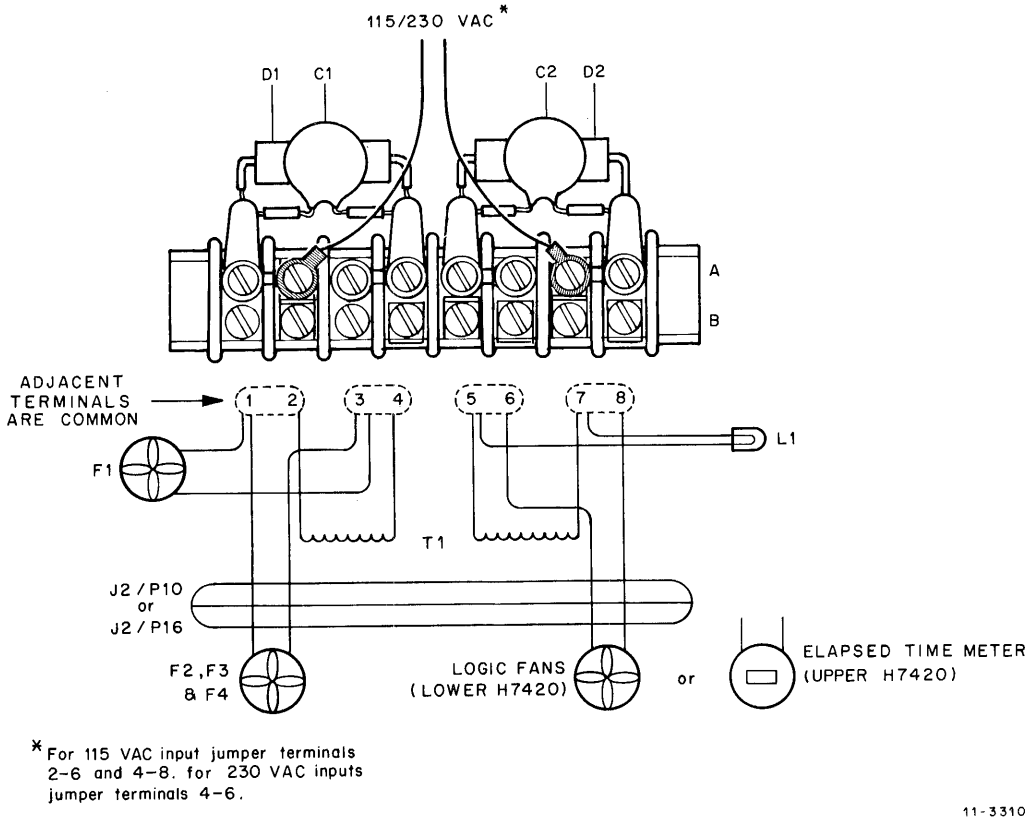


Figure 4-28 Terminal Block TB1

Table 4-8 H7420 Power Supply Specifications

Mechanical and Environmental	
Dimensions	25.4 cm h × 58.42 cm w × 20.32 cm d (10 in. h × 23 in w × 8 in d)
Weight	17.23 kg (38 lb), approximately without regulators. Regulators are 1.18 kg (4 lb), approximately
Cooling	4-inch sleeve bearing fans, DEC Part No. 12-09403-01 (IMC No. WS2107F-110-01, ROTRON No. CT 3 A2) Temp Rating -28.9° C to +54.4° C (-20° F to +130° F) Power Requirements: 115 Vac 0.24 A Air delivery: 18.87 l/s (40 ft^3/min)
Ambient Temperature:	Operating: 0° to 60°C (32° to 140° F) Storage: -40° to 70° C (-40° to 158° F)
Relative Humidity	10% to 90% (without condensation)
Altitude	3,048 meters (10,000 feet) max approximately
Electrical	
Input Power	
Voltage	90–132 Vac (H7420A, H7420E) 180–264 Vac (H7420B, H7420F)
Frequency	47–63 Hz
Current	12 A rms max at 120 Vac (A,E) 7 A rms max at 240 Vac (B) 6 A rms max at 240 Vac (F)
Inrush Current	260 A peak for 1/2 cycle at 120 Vac (A,E) 150 A peak for 1/2 cycle at 240 Vac (B,F)
Power (Apparent)	1.44 kVA max (A,E,F) 1.68 kVA max (B)
Conducted Noise	
(Noise on ac line)	
Transients	Single transient, without system degradation: 300 V at 0.2 W s Single transient, survival: 1000 V at 2.5 W s max. Average transient power survival: 0.5 W max.
CW Noise	10 KHz 3 MHz: 3 Vrms 3 MHz 50 MHz: 1 Vrms 500 MHz 1000 MHz: 0.5 Vrms

Table 4-8 H7420 Power Supply Specifications (Cont)

Conducted Noise (cont)			
RF Field Susceptibility			10 kHz–1000 MHz: 1 V/m
Ride-through Power			Upon power outage the voltage outputs are maintained within specified limits for ⩾20 ms. Control outputs are maintained within specified limits for ⩾5 ms. (Refer to Figure 4-36).
Output Power			
General			Output is through three Mate-N-Lok connectors, J2, J3, and J4, described in Paragraph 4.4.4 (Refer to Table 4-7)
J2	**Pins**	**Voltage**	**Max Load**
	1, 2, 8, 10	19–30 Vac	375 VA
	3, 7	90–132 Vac	N/A
	5, 6	90–132 Vac	4A
	4	0	Chassis Gnd
	9, 12	19–30 Vac	375 VA except E, F
	11, 13	Not used	
	14, 15	Not used	
J3	**Pins**	**Voltage**	**Max Load**
	1–8	19–30 Vac	375 VA except Pins 3-6 for E, F (no connection) Pins 1-2, 3-4 and 5-6, 7-8 are in parallel. Use only one set at one time.
	9	Not used	
J4	**Pins**	**Voltage/Remarks**	
	1	+8 V or –7 V if regulator used for –15 output	
	2, 3	+15 V or –15 V	
	4–6	Ground	
	7	AC LO/DC LO Grounds Connected to Pins 4, 5, and 6 if +15 V regulator; to pin 2 and 3 if –15 V regulator	
	8	AC LO 1	
	9	DC LO 1	
	10	AC LO 2	
	11	LTCL except when pins 2, 3, and 7 tied together (–15 V regulator)	
	12	DC LO 2	
5411086 Regulator – Refer to Paragraph 4.4.6.1			
AC LO, DC LO Circuits – Refer to Paragraph 4.4.6.1			

4.4.6 Memory Cabinet DC Power Supply (MJ11)

The MJ11 memory frame (Figure 4-29) is a 19 inch rack mountable expander box containing a 26-slot backplane and a power system which provides the regulated voltages and power fail signals required by the memory. There are two basic types of memory frame: the MJ11-AA, AC, BA, BC for 115 Vac, and the MJ11-AB, AD, BB, BD for 230 Vac. The MJ11-AA, AC, BA, BC (115 Vac) memory frame contains a 7009811-1 ac input box. The MJ11-AB, AD, BB, BD (230 Vac) contains a 7009811-2 ac input box. Aside from the ac input box, the two types of memory frames are physically identical. The memory frame can be converted from 115 Vac to 230 Vac operation or vice versa by installing the proper ac input box.

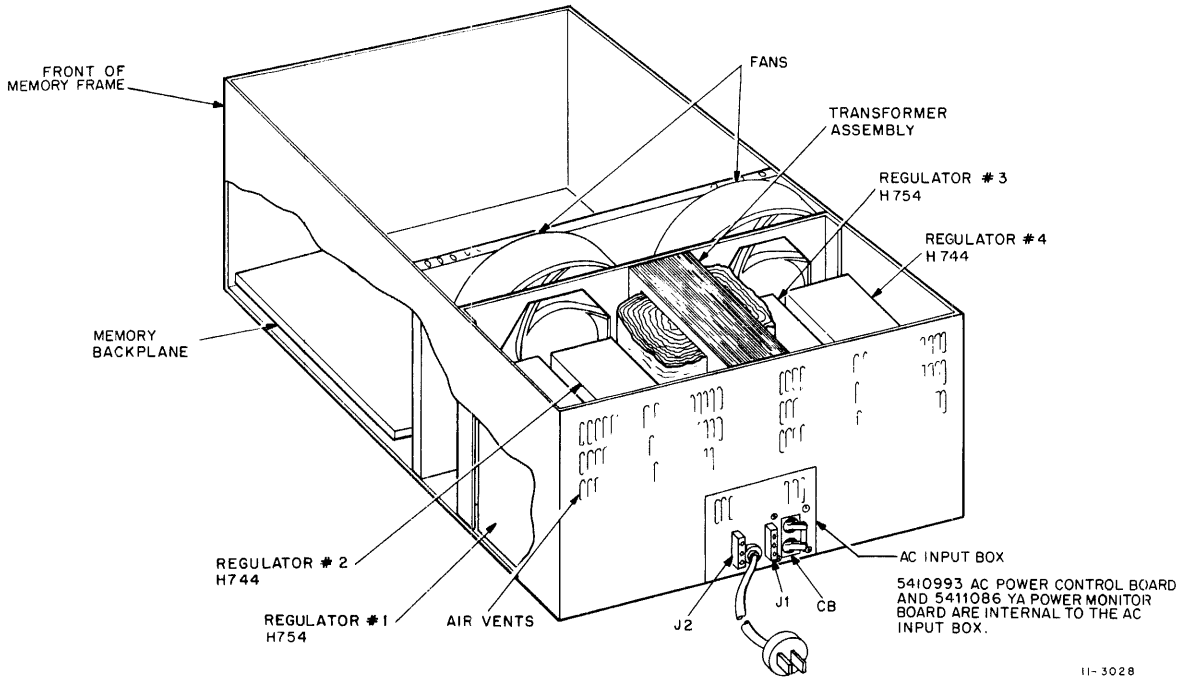


Figure 4-29 MJ11 Memory Frame Physical Layout

Table 4-9 lists the mechanical specifications of the memory frame.

The power supply is self-contained in its own chassis. It is secured to the main chassis with six screws. Two are special-purpose screws which function as hinges, enabling the power supply to be swung away from the main chassis during maintenance. The power supply contains four regulators, two fans, an ac input box, a transformer assembly, a power control card, and two power harnesses. The regulators are self-contained DIGITAL standard modular types. Table 4-10 lists the physical characteristics of the power supply. Tables 4-11 and 4-12 list the input power electrical specifications for the MJ11-AA, AC, BA, BC and MJ11-AB, AD, BB, BD memory frames.

Table 4-9 MJ11 Memory Frame Physical Characteristics

Dimensions	26.51 cm h × 43.48 cm w × 63.5 cm d (10.44 in h × 17.12 in w × 25 in d
Weight	40.82kg (90 lb)
Module Slots	26
Slide Extension (Three-section slide)	68.58 cm (27 in) maximum
Slide Weight Capacity	68.04 kg (150 lb) (frame fully extended)
Three-section slide pivotal positions	Horizontal, 45 degrees and 90 degrees (front panel facing up)
Fan air movement direction	Horizontally toward rear of memory frame
Cooling efficiency for both fans at 90 Vac, 50 Hz	Temperature rise no greater than 10° C (18° F) from inlet air temperature to exhaust air

Table 4-10 Power Supply Physical Characteristics

Item	Description
Power Supply Components	H744 Regulators (two) H754 Regulators (two) 5411086-YA Power Line Monitor Board 7010014 Transformer Assembly 7009811-1 or -2 AC Input Box with 5410993 Power Control Board 7010580 Power Distribution Harness 7010581 Harness 1211714 Box Fans (two)
Fan Size	15.2 cm (6 in) Diam., 3.8 cm (1-1/2 in) blade depth
Fan Type	Ball bearing, DEC No. 1211714
Fan Capacity at 115 V, 50 Hz	122.7 l/s (260 ft^3/min) at 0 static pressure
Fan efficiency at 90 Vac, 50 Hz	60%
7010014 Transformer Assembly Weight	11.34 kg (25 lb)

Table 4-11 MJ11-AA, AC, BA, BC Memory Frame Input Power Electrical Specifications

Parameter	Specification
Input Power	MJ11-AA, BA 90–132 Vac, 115 Vac nominal, 47–63 Hz, single phase MJ11-AC, BC 180–264 Vac (phase to neutral) (312–456 Vac phase to phase) 3-phase wye at 30 A/phase
Inrush Current	175 A peak for 10 ms max. at 115 V line voltage
Input Power	1200 W maximum at 115 V nominal line voltage
Input Current	12 A max at 115 Vac
Circuit Breaker rating	20 A at 115 Vac
Power Factor	The ratio of input power to apparent power will be greater than 0.85
Conducted Noise (Noise on ac Line)	
Transients	Single transient without loss of data: 300 V at 0.2 W/s max. Single transient, survival: 1000 V at 2.5 W s max. Average transient power survival: 0.5 W max.
CW Noise	10 KHz – 3 MHz: 3 Vrms 3 MHz – 500 MHz: 1 Vrms 500 MHz – 1000 MHz: 0.5 Vrms
RF Field Susceptibility	10 KHz – 1000 MHz: 1 V/m
Power Fail	The power supply is capable of withstanding power interruptions of any magnitude and duration without damage. Storage time of power supply at low line and full load shall be 20 ms minimum. Storage time is measured from the time the power outage occurs until the time the regulator voltages listed in Table 4-16 drop below their specified regulation limits.

Table 4-12 MJ11-AB, AD, BB, BD Memory Frame Input Power Electrical Specifications

Parameter	Specification
Input Power	180–264 Vac, 230 Vac nominal, 47–63 Hz, single phase
Inrush Current	80 A peak for 10 ms max at 230 Vac line voltage
Input Power	1200 W maximum at 230 Vac nominal line voltage
Input Current	6 A max at 230 Vac
Circuit Breaker Rating	10 A at 230 Vac
Power Factor	The ratio of input power to apparent power shall be greater than 0.85
Conducted Noise (Noise on ac Line)	
Transients	Single transient, without loss of data: 300 V at 0.2 W/s Single transient, survival: 1000 V at 2.5 W/s max Average transient power survival: 0.5 W max
CW Noise	10 KHz-3 MHz: 3 Vrms 3 MHz-50 MHz: 1 Vrms 500 MHz-1000 MHz: 0.5 Vrms
RF Field Susceptibility	10 KHz-1000 MHz: 1 V/m
Power Fail	The power supply is capable of withstanding power interruptions of any magnitude and duration without damage. Storage time of power supply at low line and full load shall be 20 ms minimum. Storage time is measured from the time the regulator voltages (listed in Table 4-16) drop below their specified regulation limits.

A functional block diagram of the power supply is shown in Figure 4-30. If the line cord is plugged into an energized outlet, line voltage is applied to the ac input box. The ac input box contains a circuit breaker, an ac power control board, and a power line monitor board. The circuit breaker is used as an ON/OFF switch, as well as an overcurrent protection device. The ac power control board and its associated relay (K2) allow remote control of ac power to the transformer assembly primaries by the thermal switch mounted on the transformer assembly. The memory frame cooling fans connect directly to the transformer primaries.

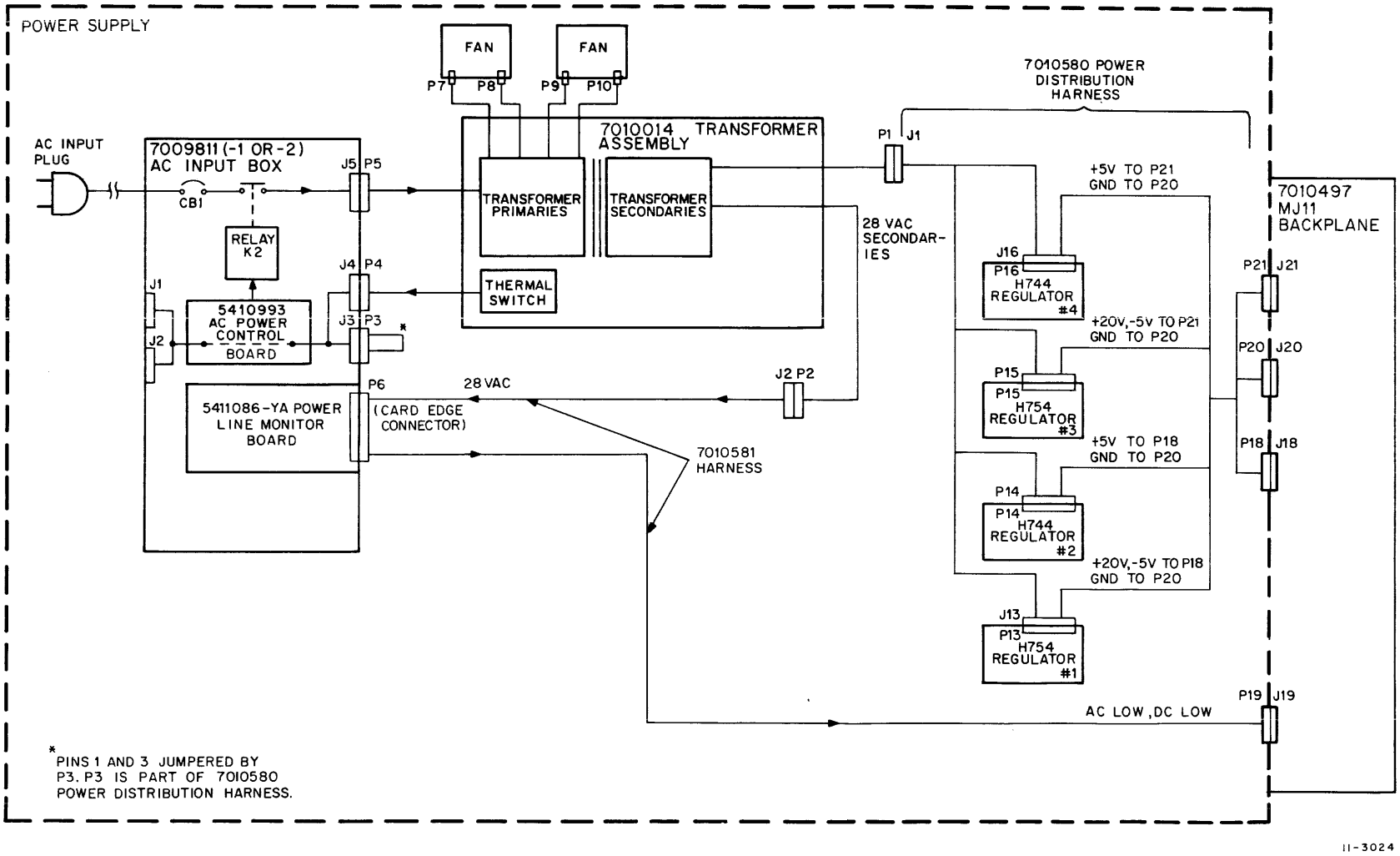


Figure 4-30 MJ11 Power Supply Functional Block Diagram

The 7010014 transformer assembly steps down the voltage from the ac input box to approximately 28 Vac and routes it to the two H744 regulators, the two H754 regulators, and the 5411086-YA power line monitor board in the ac input box. The H744 and H754 regulators produce the +5 V, +20 V, and -5 Vdc voltage required in the memory frame.

The 5411086-YA power line monitor generates the AC LO and DC LO power fail signals. It is mounted within the ac input box and is secured in place when the ac input box is installed in the power supply chassis. A card edge connector provides an electrical connection to a transformer secondary and to the memory backplane. Note that although the 5411086-YA is physically mounted in the ac input box, it is considered a separate assembly. The 5411086-YA, which is referred to as the power control card in some documentation, is described further in Paragraph 4.4.6.1.

The H744 (also used in the H7420) and H754 regulators are described in Paragraph 4.4.6.2. Drawings E-UA-MJ11-0-0 sheet 4 and E-AD-7010694 sheet 2 illustrate these circuits and their interrelation.

The following paragraphs describe, in detail, the ac input box, the transformer assembly, and the box fans.

The ac input box is mounted in the center of the power supply chassis with three Phillips head screws. The center rear of the power supply chassis is cut out, exposing the rear of the ac input box. This enables easy access to the ac line cord, circuit breaker, and remote power control Mate-N-Lok. The 5410993 ac power control board and the 5411086-YA power line monitor board are physically mounted in the ac control box.

The 115 V (7009811-1) and 230 V (7009811-2) ac input boxes are functionally identical. They differ physically in their components and in the way they are connected to the transformer assembly. Figure 4-31 is a simplified schematic of the 115 Vac power configuration. In this configuration, the power transformer windings are connected in parallel. In the 230 Vac power configuration (Figure 4-32), the power transformer windings are connected in series.

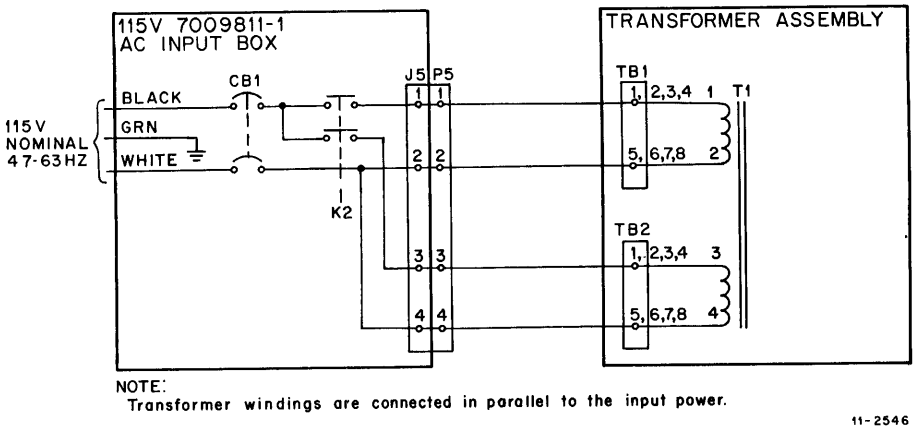


Figure 4-31 115 Vac Power Configuration

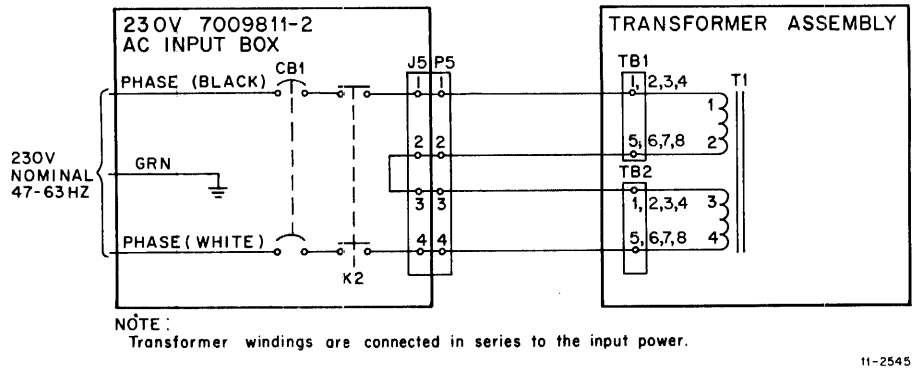


Figure 4-32 230 Vac Power Configuration

Utilizing the 115 Vac input box (7009811-1), the input line voltage is applied via a 20 A circuit breaker to relay K2 and transformer T1 on the power control board. Transformer T1 steps down the voltage to 24 Vac. The 24 Vac is rectified and applied to relay K1 (Figure 4-33). Energizing K1 completes the path to K2, switching the 115 Vac to the transformer assembly. The normally open thermal switch (TS1) (located in the transformer assembly) closes when an over-temperature condition is sensed. Closing TS1 applies 24 Vdc to half the K1 relay coil. This creates two opposing fields, causing K1 to de-energize. De-energizing K1 interrupts the ac power to the transformer assembly. The varistor (D6 or D7) across the coil of K2 suppresses voltage spikes in excess of 150 Vac for ac input box 7009811-1 and 275 Vac for ac input box 7009811-2.

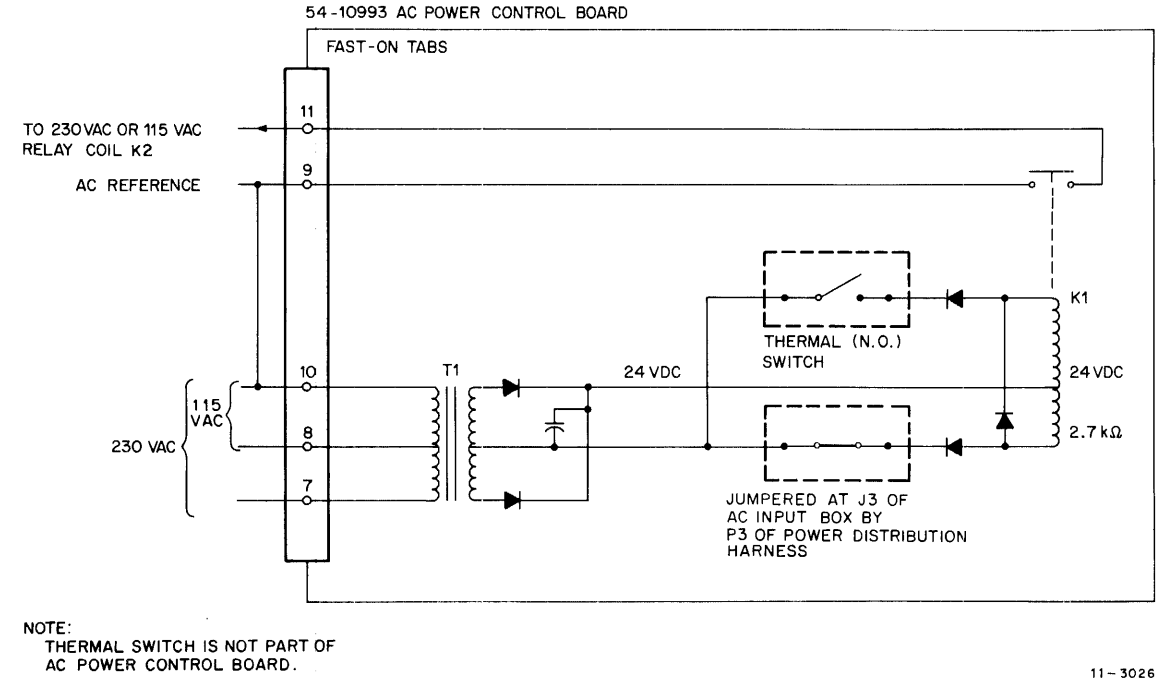


Figure 4-33 Power Control Board Simplified Diagram

The 7010014 transformer assembly is located in the center of the power supply chassis. Two capacitors, two varistors, and two terminal boards are mounted directly on the transformer. The transformer base plate is used to bolt the transformer to the chassis. The area around the transformer is open, enabling ample air flow from the two fans across the transformer. A thermistor is mounted directly to the transformer frame, enabling over-temperature monitoring. Output leads from the transformer, which go to other modules, are terminated in Mate-N-Lok connectors. A cable clamp is used to secure these leads to the chassis.

The primary function of the transformer assembly is to step down the 115 Vac or 230 Vac input voltage to 28 Vac. There are five separate secondary transformer windings, one for each regulator and one for the power line monitor board. In addition, the transformer assembly routes 115 Vac from TB1 and TB2 to box fans 1 and 2, respectively.

The two capacitors (C1, C2) connected across the primary of T1 function as input line filters. Two varistors (D1, D2), also connected across the T1 primary, suppress voltage spikes in excess of 150 Vac.

Two, 6-inch ball bearing box fans (1211714) are used in the power supply. They are mounted on the chassis between the module boards and regulators. Each fan is secured to the chassis with two screws.

4.4.6.1 5411086-YA Power Line Monitor – The 5411086 power line monitor (Figure 4-34) is a 15 V switching regulator that also produces real time clock (LTCL) and power fail (AC LO and DC LO) signals. A +8 V terminal is also provided. LTCL is a square wave, logic level, signal at line frequency. AC LO L indicates that the line voltage is below a prescribed minimum. DC LO L indicates that the line voltage is below the minimum operating tolerance and that the +15 V regulator circuit cannot be expected to produce an output within specified normal operating limits.

The 15 V output can be connected to provide either a -15 V or a +15 V source. If connected as a -15 V source, the LTCL and +8 V terminals should not be used. This is the case in the processor cabinet power system. The 5411086 in the upper H7420 power supply produces +15 V, +8 V, LTCL, and the AC LO–DC LO signals while the 5411086 in the lower H7420 produces only -15 V and the AC LO–DC LO signals.

NOTE

The MJ11 power supply is equipped with the -YA version of the 5411086 board. The 5411086-YA contains the line clock and power fail circuits just described, but not the regulator circuit.

The specifications for the 5411086 are listed in Table 4-13. Drawing D-CS-5411086-0-1 is a circuit schematic of the 5411086.

In the regulator circuit, the 20–30 Vac input is full-wave rectified by bridge D11 to provide dc voltage (25 to 45 Vdc, depending on line voltage and load on +15 V) across filter capacitor C1 and bleeder resistor R15. Operation centers on voltage regulator E1, which is configured as a positive switching regulator. A simplified schematic of E1 is shown in Figure 4-34. E1 is a monolithic integrated circuit that is used as a voltage regulator. It consists of a temperature-compensated reference amplifier, an error amplifier series pass power transistor, and the output circuit required to drive the external transistors. In addition to E1, the regulator circuit includes pass transistor Q7, predriver Q4, and level shifter Q6. Zener diode D17 is used with R11 to provide +15 V for E1.

The output circuit is standard for most switching regulators and consists of free-wheeling diode D12, choke coil L1, and output capacitor C3. These components make up the regulator output filter. Free-wheeling diode D12 is used to clamp the emitter of Q7 to ground when Q7 shuts off, providing a discharge path for L1.

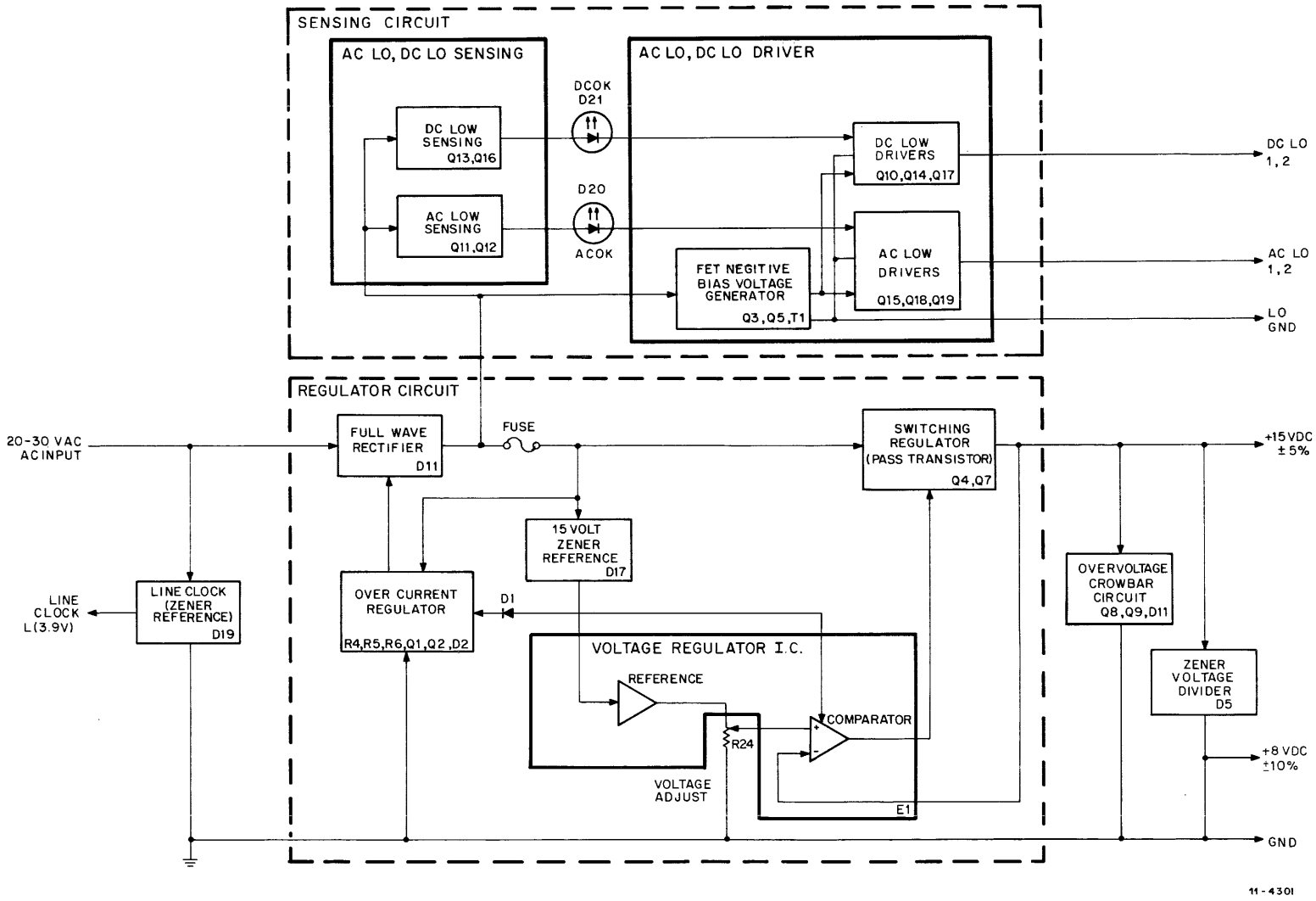


Figure 4-34 5411086 Block Diagram

Table 4-13 5411086 Specifications (+15 V)

Parameter	Specification
Input Voltage, Frequency	20–33 Vac rms, 47–63 Hz
Input Power	120 W (at nominal line, full load)
Output Voltage	+15 Vdc ±5% +8 Vdc ±10%
Output Load	+15 V: 0 - 4.0 A +8 V: 0 - 1.0 A The total of +15 V and +8 V loads must not exceed 4 A
Adjustment	15 V ±1.5 V (R 24) +8 V output is 6.8 V ±5% below 15 V output
Ripple	0.45 V peak-to-peak maximum
Backup Fuse	5.0 A
Over Voltage Protection	SCR crowbar trips at 16.5 V to 19.5 V
Output Signals	LTCL, AC LO (2), DC LO (2)
Indicators	2 LEDs (ACOK, DCOK)

In operation, Q7 is turned on and off, generating a square wave of voltage that is applied across D12 at the input of the LC filter (L1 and C10). Basically, this filter is an averaging device, and the square wave of voltage appears as an average voltage at the output terminal. By varying the period of conduction of Q7, the output (average) voltage may be varied or controlled, thus supplying regulation (Figure 4-36). The output voltage is sensed and fed back to E1, where it is compared with a fixed reference voltage. E1 turns pass transistor Q7 on and off, according to whether the output voltage level approaches its upper and lower limits (approximately +15.15 V and +14.85 V respectively).

During one full cycle of operation, the regulator operates as follows: Q7 is turned on and a high voltage (approximately +30 V) is applied across L1. If the output is already at a +15 V level, then a constant +15 V would be present across L1. This constant dc voltage causes a linear ramp of current to build up through L1. At the same time, output capacitor C10 absorbs this changing current, causing the output level (+15 V at this point) to increase. When the output, which is monitored by E1, reaches approximately +15.15 V, E1 shuts off, turning Q7 off; the emitter of Q7 is then clamped to ground. L1 reverses polarity and discharges through D12 into capacitor C10, and the load. Predriver Q4 is used to increase the effective gain of Q7, thus ensuring that Q7 can be turned on and off in a relatively short period of time.

Conversely, once Q7 is turned off and the output voltage begins to decrease, a predetermined value of approximately +14.85 V will be reached, causing E1 to turn on; E1 in turn, causes Q7 to conduct, beginning another cycle of operation.

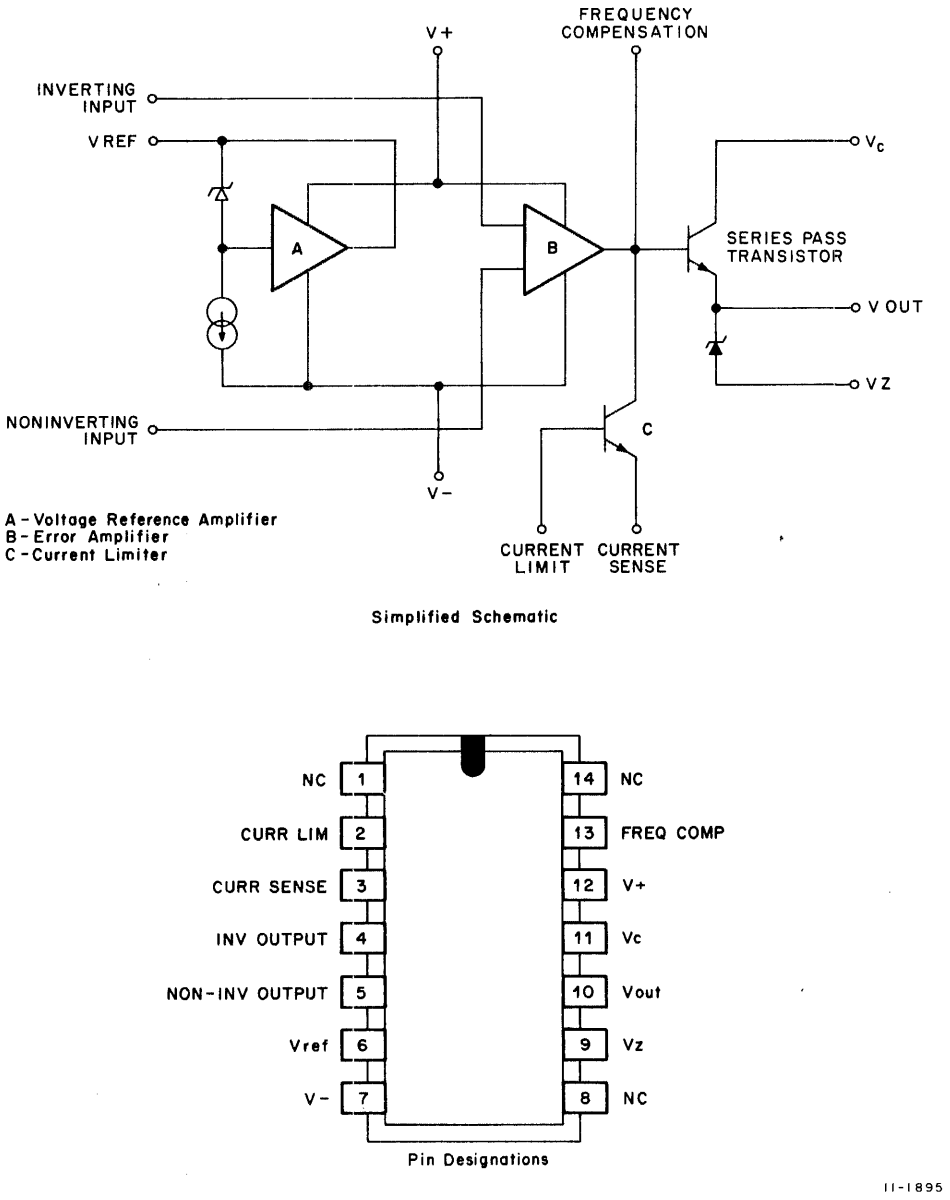


Figure 4-35 Voltage Regulator E1, Simplified Diagram

Thus, a ripple voltage is superimposed on the output and is detected as predetermined maximum (+15.15 V) and minimum (+14.85 V) values by E1. When +15.15 V is reached, E1 turns Q7 off; when +14.85 V is reached, E1 turns Q7 on. This type of circuit action is called a ripple regulator.

The overcurrent regulator circuit functions as a current regulator when the current, monitored at D11, exceeds 5 A. The current regulator consists of R4, R5, R6, Q1, Q2, and D2. During normal operation, Q1 and Q2 are not conducting. Q2 starts conducting when the voltage drop across R5 and R6 (sensed by D2) exceeds approximately 0.6 V. When Q2 conducts, D1 becomes forward biased and E1 is shut off, turning off the pass transistor Q7 and predriver Q4. The conduction of Q2 will also turn on Q1 providing a constant current source (1 mA) to the base of Q2. Q1 will hold Q2 on until the current across R5 and R6 drop below approximately 4 A.

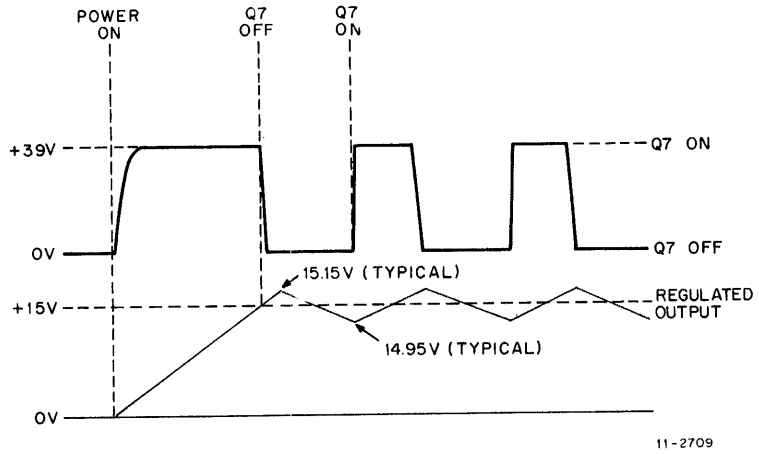


Figure 4-36 5411086 Regulator Waveforms

With Q1 and zener D2 tied to the +15 V zener reference for E1, the conduction of Q1 will hold E1 off. When Q1 and Q2 stop conducting, E1 will turn on, enabling the current to exceed the regulator limits. With a continuous overcurrent condition, Q1 and Q2 will be turning on and off, causing the circuit to become a constant current regulator.

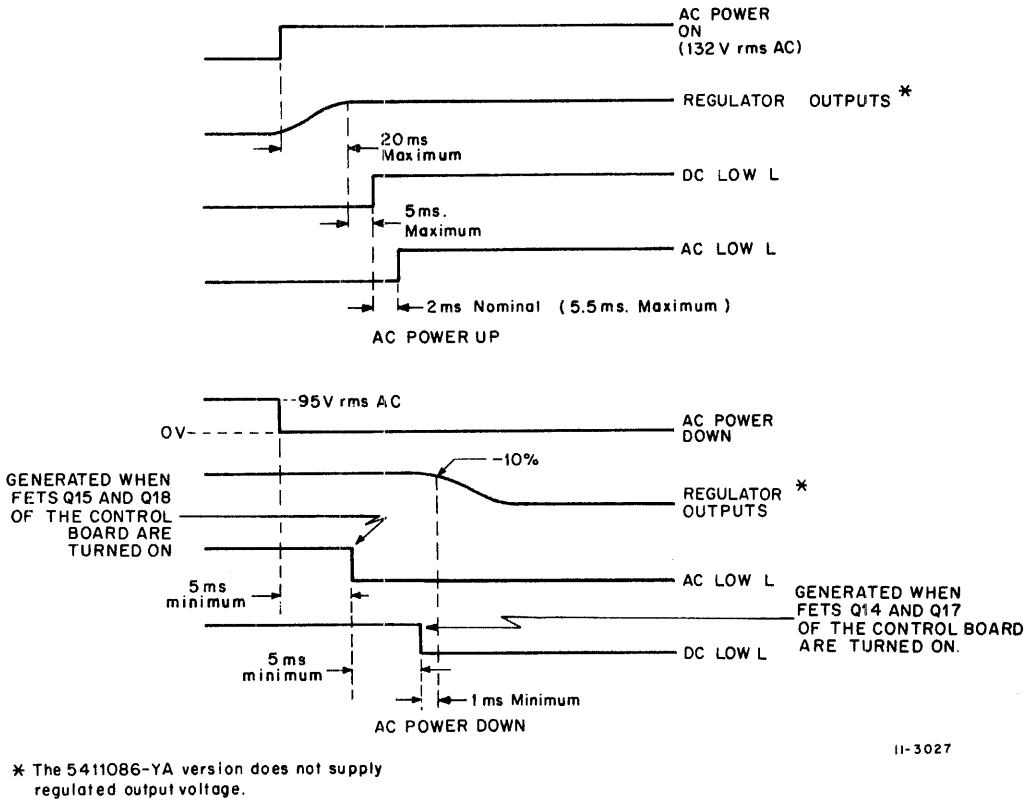
The +15 V overvoltage crowbar circuit consists of the following components: zener diode D18, silicon controlled rectifier (SCR) Q8, Q9, R38, R40, C13, and Q9. Under normal output voltage conditions, the trigger input to SCR D7 is at ground because the voltage across zener diode D3 is less than 18 V. If the output voltage becomes dangerously high (above 18.0 V), diode D18 conducts turning Q9 on, and the voltage drop across R40 draws gate current and triggers the SCR. The SCR fires, short circuits the +15 V output to ground, and turns off E1 by shorting out the +15 V reference at D17.

The line clock output (LTCL) is derived from one leg of full-wave rectifier bridge D11, by voltage divider R22 and zener diode D19. The clock output is a 0 to +3.9 V square wave at the line frequency of the power source (47 to 63 Hz). The clock output is used to drive the KW11 clock options.

The AC LO and DC LO sensing circuit has a 20–30 Vac input from a secondary winding of transformer T1. The sensing circuits are shown on drawing D-CS-5411086-0-1; a simplified version is shown in Figure 4-34. The ac input is rectified by diodes D15 and D16, and filtered by capacitors C20 and C24. A common reference voltage is derived by zener diodes D13 and D14. Both sensing circuits operate similarly; each contains a differential amplifier and associated circuits. The major difference is that the base of Q12 in the AC LO circuit differential amplifier is at a slightly lower value than that of Q16 in the DC LO differential amplifier. The operation of both sensing circuits depends on the voltage across capacitor C8. For AC LO and DC LO timing during power up and power down, refer to Figure 4-37. Table 4-14 lists some of the characteristics of the AC LO and DC LO circuits.

The AC LO and DC LO driver circuit produces the power fail signals that are sent to the memory backplane. When an ac low condition is sensed, the output of differential amplifier Q12 turns off Q9. Q19 in turn gates on FETs Q15 and Q18, generating AC LO 1 and AC LO 2 signals.

Approximately 7 ms after ac low is sensed, the dc low sensing circuit will generate DC LO. The dc low sensed output from differential amplifier Q16, turns off Q10. Q10 in turn gates on FETs Q14 and Q17, generating DC LO 1 and DC LO 2 signals.



* The 5411086-YA version does not supply regulated output voltage.

Figure 4-37 5411086 Power Up and Power Down

Table 4-14 AC LO and DC LO Circuit Specifications

Parameter	Specifications
Static Performance at Full Load	
Input Voltage Increasing	DC LO goes high at 75–80 Vac AC LO goes high at 85–90 Vac
Input Voltage Decreasing	AC LO goes low (asserted) at 83–88 Vac DC LO goes low (asserted) at 73–78 Vac
Hysteresis	2–4 Vac (approximately)
Output Characteristics	
Load	J FETs can sink 100 mA (max)
Rise/Fall Times	1 μs (max)

The +25 Vdc to +45 Vac from rectifier D11 is applied to T1, Q3, and Q5, Q3 and Q5, due to their switching action, create a pulsating dc which is applied to the primary of transformer T1. The output from the secondary of T1 (approximately 15 V) is rectified by D6, D7, D8, and D9, producing -10 Vdc to -15 Vdc. The -10 Vdc to -15 Vdc is a negative bias used to gate OFF J FETs Q15, Q18, Q14, and Q17 via Q19 and Q10. Unlike most transistors, the negative bias is used to turn off the J FETs. The J FETs are turned on when there is zero volts between gate (G) and source (S) terminals.

Light emitting diodes D20 (ACOK) and D21 (DCOK) are normally lit. When AC LO L and/or DC LO L are asserted, the light emitting diodes go off, indicating that this regulator is the source of AC LO L or DC LO L on the Unibus. (The location of D20 and D21 on the H7420 5411086 is shown in Figure 4-26.)

The following paragraphs describe AC LO and DC LO interconnections in the processor and memory cabinets. Figure 4-38 shows the routing of these signals through the system.

Each main memory drawer power supply and both processor cabinet power supplies contain a 5411086 power line monitor board (memory power supply contains a -YA version). The ac power monitor circuits (AC LO and DC LO) are on this board. AC LO and DC LO both have two independent open collector output drivers on each 5411086. Refer to the Engineering Print Set for a schematic of this circuit.

Table 4-15 lists the processor cabinet and main memory cabinet AC LO and DC LO signals.

The AC LO signals from all main memory power supplies are wire-ORed and transmitted to the cache (ADML) on the main memory bus cable. The signal is buffered, renamed ADML AC LO H and is one of two inputs to the processor power-up/power-down circuits on UBCE.

The processor power supply AC LO 1, AC LO 2, AC LO 3 and AC LO 4 signals are connected to the Unibus AC LO line (BUS AC LO L) at the backplane. This signal is the other input to the processor power-up/power-down circuits on UBCE, when it is ORed with ADML AC LO.

The output of the OR, UBCE AC LO L, is also input to the cache power-up circuits (ADMJ).

There are two separate DC LO lines in the PDP-11/70: BUS DC LO (Unibus) and MAIN DC LO (main memory). Two signal lines are required because:

1. The signal level on the Unibus (0 V to 5 V) is different from that on the main memory bus (0V to 3.5 V), and

2. The impedance of the Unibus (120 Ω) is different from that of the main memory bus (75 Ω).

BUS DC LO L is the wire-OR of DC LO Y (upper processor H7420 power supply), DC LO X (lower processor H7420) and the DC LO signals from all devices on the Unibus. It is one of two inputs to the processor power-up/power-down circuits on UBCE.

MAIN DC LO is the wire-OR of DC LO 1 (upper processor H7420), DC LO 2 (lower processor H7420), and both DC LO outputs from all main memory drawers (via the main memory bus cable). MAIN DC LO is buffered in the cache, renamed ADML MAIN DC LO H, and is the second input to the processor power-up/power-down circuits.

BUS DC LO and MAIN DC LO are ORed (UBCE) and input to both the cache power-up and to the processor power-up/power-down circuits. MAIN DC LO, however, is the only input to the main memory protection circuitry (MCTH). This circuitry inhibits the memory write operations on power-down 3 μs after receipt of DC LO.

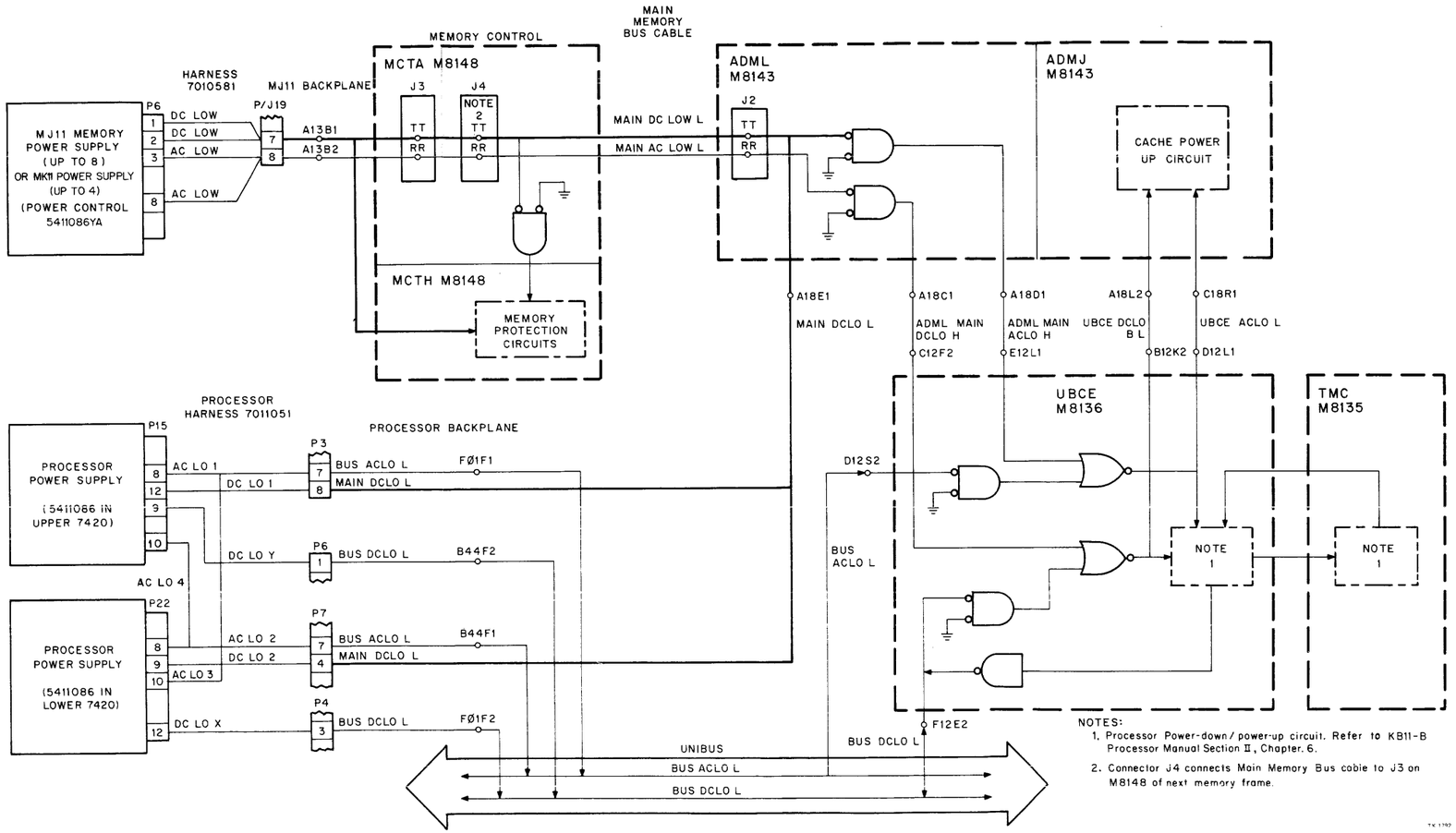


Figure 4-38 AC LO and DC LO Circuit

Table 4-15 AC LO and DC LO Driver Outputs

Signal Name	Unit	Connector Pin
AC LO 1	Upper processor H7420	P/J15-8
AC LO 2	Lower processor H7420	P/J22-8
AC LO 3	Lower processor H7420	P/J22-10
AC LO 4	Upper processor H7420	P/J15-10
AC LO	Main Memory P/S	P/J6-3
AC LO	Main Memory P/S	P/J6-8
DC LO 1	Upper processor H7420	P/J15-12
DC LO 2	Lower processor H7420	P/J22-9
DC LO X	Lower processor H7420	P/J22-12
DC LO Y	Upper processor H7420	P/J15-9
DC LO	Main Memory P/S	P/J6-1
DC LO	Main Memory P/S	P/J6-2

In the PDP-11/70, these interconnections are such that a power failure from any device (Unibus device, processor or main memory):

1. Causes the processor to trap to location 24 and to perform the power-down subroutine, and
2. Causes the cache to prevent all access to main memory when DC LO is asserted at the end of the 2 ms power-down subroutine time allotment.

In addition, when the power failure is a processor or a main memory failure, the main memory protection circuits are activated when MAIN DC LO is asserted by either the processor or the main memory power supplies.

4.4.6.2 H744 and H754 Regulators – There are seven (eight if the FP option is included) H744 regulators in the processor cabinet power system (Figure 4-3). In the MJ11 memory cabinet power supply, there are two H744 and two H754 regulators (Figure 4-4).

These regulators are secured to the power supply chassis with three screws and are installed with the heat sink upward. The mounting screws pass through the chassis holes and screw into the regulator. A plastic (Lexon) cover is installed on the component side of each regulator. This permits visual inspection of the regulator components when the regulator is removed from the chassis. The fuse, which is located on the component side, is accessed by removing the plastic cover. Table 4-16 lists the output power characteristics of the H744 and H754 regulators.

Circuit schematics for the H744 and H754 regulators are shown in drawings D-CS-H744-0-1 and D-CS-H754-0-1, respectively.

The following paragraphs describe the regulator circuit, overcurrent sensing circuit, and the overvoltage crowbar circuit for each regulator.

Table 4-16 Output Power Characteristics

Regulator	Voltage and Tolerance		Output Current (maximum per regulator)	Maximum Peak-to-Peak Ripple
H744	+5 Vdc	250 mV	25 A	200 mV
H754	+20 Vdc	1 V	8 A	5%*
	-5 Vdc	250 mV	1 A - 8 A**	5%*

*At backplane, typical ripple ±3 percent.

**Maximum -5 V current is dependent upon +20 V current. It is equal to 1 A plus the current of the +20 V supply, up to a total of 8 A.

In the H744 regulator circuit, the 20–30 Vac input is full-wave rectified by bridge D1 to provide dc voltage (24 to 40 Vdc, depending on line voltage) across filter capacitor C1 and bleeder resistor R1. Operation centers on voltage regulator E1, which is configured as a positive switching regulator. A simplified schematic of E1 is shown in Figure 4-34. E1 is a monolithic integrated circuit that is used as a voltage regulator. It consists of a temperature-compensated reference amplifier, an error amplifier series pass power transistor, and the output circuit required to drive the external transistors. In addition to E1, the regulator circuit includes pass transistor Q2, predrivers Q3 and Q4, and level shifter Q5. Zener diode D2 is used with Q5 and R2 to provide +15 V for E1. Q5 is used as a level shifter; most of the input voltage is absorbed across the collector-emitter of Q5. This is necessary because the raw input voltage is well above that required for E1 operation. While this +15 V input is supplied, D2, Q5, and R2 retain the ability to switch pass transistor Q2 on or off by drawing current down through the emitter of Q5.

The output circuit is standard for most switching regulators and consists of free-wheeling diode D5, choke coil L1, and output capacitors C8 and C9. These components make up the regulator output filter. Free-wheeling diode D5 is used to clamp the emitter of Q2 to ground when Q2 shuts off, providing a discharge path for L1.

In operation, Q2 is turned on and off, generating a square wave of voltage that is applied across D5 at the input of the LC filter (L1, C8, and C9). Basically, this filter is an averaging device, and the square wave of voltage appears as an average voltage at the output terminal. By varying the period of conduction of Q2, the output (average) voltage may be varied or controlled, supplying regulation (Figure 4-38). The output voltage is sensed and fed back to E1, where it is compared with a fixed reference voltage. E1 turns pass transistor Q2 on and off, according to whether the output voltage level increases or decreases. Defined upper and lower limits for the output are approximately +5.05 V and +4.95 V.

During one full cycle of operation, the regulator operates as follows: Q2 is turned on and a high voltage (approximately +30 V) is applied across L1. If the output is already at a +5 V level, then a constant +25 V would be present across L1. This constant dc voltage causes a linear ramp of current to build up through L1. At the same time, output capacitors C8 and C9 absorb this changing current, causing the output level (+5 V at this point) to increase. When the output, which is monitored by E1, reaches approximately +5.05 V, E1 shuts off, turning Q2 off; the emitter of Q2 is then clamped to ground. L1 discharges into capacitors C8, C9, and the load. Predrivers Q3 and Q4 are used to increase the effective gain of Q2, ensuring that Q2 can be turned on and off in a relatively short period of time.

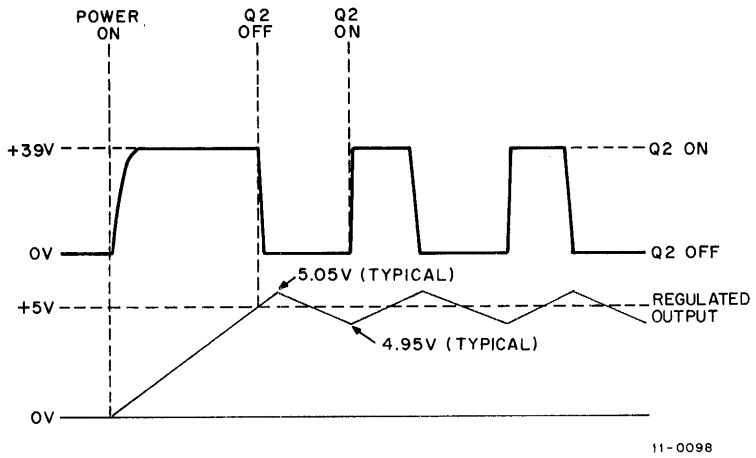


Figure 4-39 H744 Regulator Waveforms

Conversely, once Q2 is turned off and the output voltage begins to decrease, a predetermined value of approximately +4.95 V will be reached, causing E1 to turn on; E1 in turn, causes Q2 to conduct, beginning another cycle of operation.

Thus, a ripple voltage is superimposed on the output and is detected as predetermined maximum (+5.05 V) and minimum (+4.95 V) values by E1. When +5.05 V is reached, E1 turns Q2 off; when +4.95 V is reached, E1 turns Q2 on. This type of circuit action is called a ripple regulator.

The H744 +5 V overcurrent sensing circuit consists of Q1, R3 through R6, R25, R26, programmable unijunction Q7, and C4. Transistor Q1 is normally not conducting; however, if the output exceeds 30 A, the forward voltage across R4 is sufficient to turn Q1 on, causing C4 to begin charging. When C4 reaches a value equal to the voltage on the gate of Q7, Q7 turns on and E1 will be biased off, turning the pass transistor off. Thus, the output voltage is decreased as required to ensure that the output current is maintained below 35 A (approximately) and that the regulator is short circuit protected. The regulator continues to oscillate in this new mode until the overload condition is removed. C4 then discharges until E1 is allowed to turn on again and the cycle repeats.

The H744 +5 V overvoltage crowbar circuit contains the following components: zener diode D3, silicon-controlled rectifier (SCR) D7, D8, R22, R23, C7, and Q6. Under normal output voltage conditions, the trigger input to SCR D7 is at ground because the voltage across zener diode D3 is less than 5.1 V. If the output voltage becomes dangerously high (above 6.0 V), diode D3 conducts, and the voltage drop across R23 draws gate current and triggers the SCR. The SCR fires and short circuits the +5 V output to ground.

The regulator circuit in the H754 has a voltage doubler input, but the output consists of two shunt regulator circuits - one for the +20 V, the other for the -5 V. The +20 V shunt regulator consists of transistors Q4, Q10, and Q11; the -5 V shunt regulator consists of Q6 and Q9. Q10 and Q9 are the pass transistors.

The output of the basic regulator is 25 V (-5 to +20 V). The shunt regulators are connected across this output, with a tap to ground between pass transistors Q9 and Q10. The voltage at the bases of Q6 and Q4 will vary with respect to ground, depending on the relative amount of current drawn from the +20 V and -5 V outputs of the regulator. If the +20 V current increases while the -5 V current remains constant, the output voltage at the +20 V output will tend to go more negative with respect to ground; this will also cause the -5 V output to go more negative, since the output of the basic regulator is a fixed 25 V. This change is sensed at the bases of Q6 and Q4; Q6 will conduct, causing Q9 to conduct also, increasing the current between -5 V and ground until the balance between the +20 V and the -5 V is restored. At this time, neither Q6 nor Q4 will be conducting. If the -5 V current increases, Q4 and Q10 will conduct to balance the outputs.

The H754 has two crowbar circuits: Q7 and its associated components for the +20 V and the Q12 and is circuitry for the -5 V. Either one will trigger SCR D9.

The H754 overcurrent circuit comprises Q1, Q8, Q13, Q14, and associated circuitry. The total peak current is sampled through R4. When the peak current reaches approximately 14 A, Q1 turns on sufficiently to establish a voltage across R7 and R38, firing Q8. This pulls the voltage on pin 4 of the 723 up above the reference voltage on pin 5, shutting off Q2. D6 now conducts, and the current through R37 turns on Q14, which turns on Q13. This keeps Q8 on for a time which is determined by the output voltage and L1. This action, in turn, allows the off-time to increase as the overload current increases, thereby changing the duty cycle in proportion to the load. The output current is thus limited to approximately 10 A.

4.4.7 MK11 DC Power Supply

The MK11 power supply consists of an ac input box (7014420-1, 2), a transformer assembly (7011486), a +5 V regulator (H7441), three ±12 V and +5 V regulators (7014251), and three battery backup units (H755-D). A chassis, mounted at the back of the memory box, houses the ac input box, transformer assembly, the four voltage regulators, and two cooling fans. The three battery backup units and their battery packs are each housed in their own boxes, separate from the other power supply assemblies. Figure 4-40 identifies the major assemblies of the memory's power supply.

4.4.7.1 MK11 Power Supply Cables

External Power Cables

The external power cables interconnect the memory box and the box controller and battery backup units within the memory cabinet. Figure 4-41 is a simplified block diagram of these cables. For the actual cable routing, see Paragraph 3.6.

Box Controller Power Cable (7014311) - This cable harness connects the on/off power switch on the box controller to the memory's power supply for controlling power to the memory. This harness also carries signals to the battery status indicators, which show the operating mode of the three battery backup units.

Battery Backup Power Cable (7014520-08) - These three cables connect the battery backup units to their regulators. Power to charge the batteries or power from the batteries to run the memory is carried by these cables, along with control and battery status signals.

Internal Power Harnesses

The internal power harnesses connect the power supply assemblies to the memory backplane. These harnesses are shown in Figure 4-42.

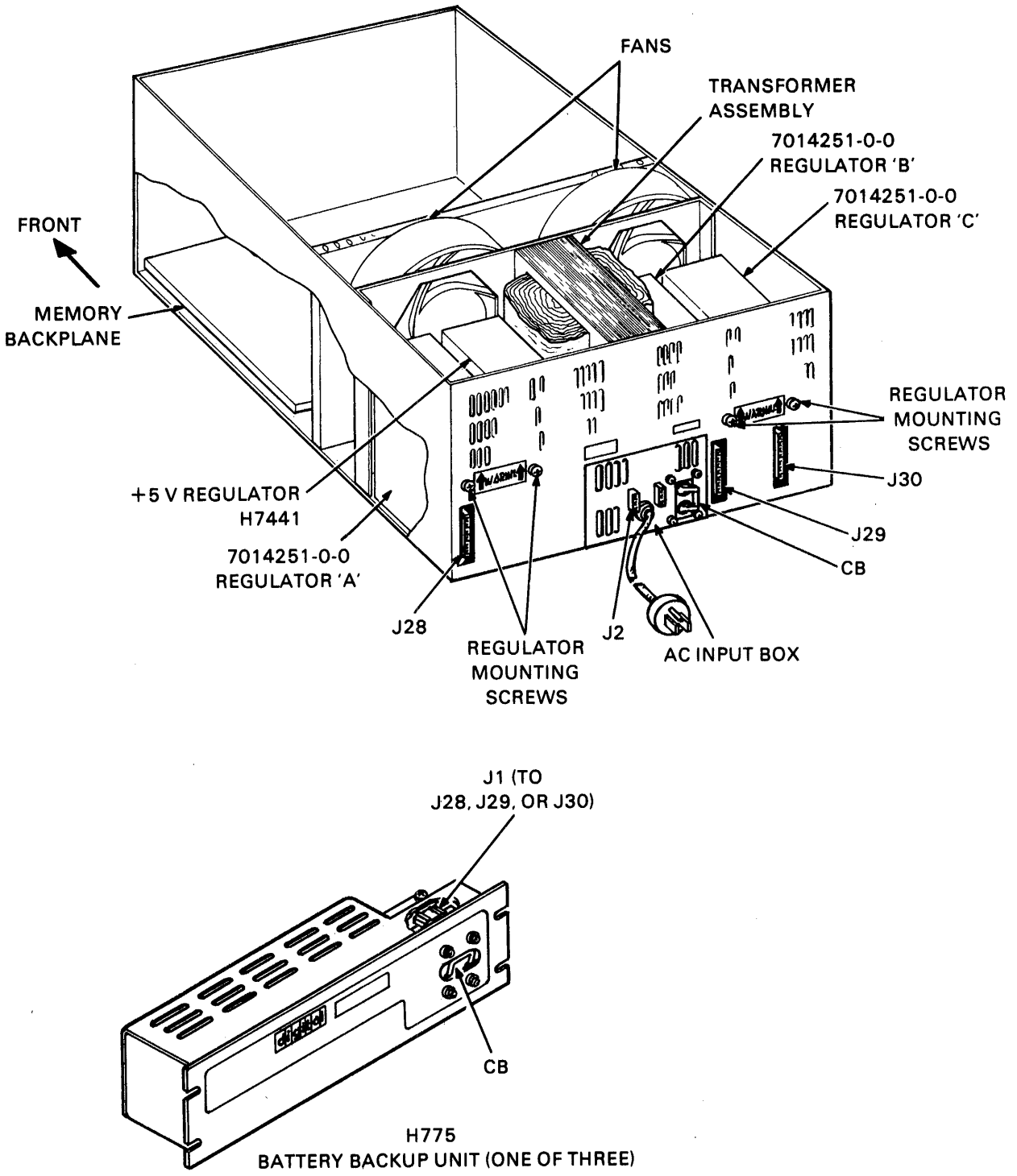


Figure 4-40 MK11 Power Supply Major Assemblies

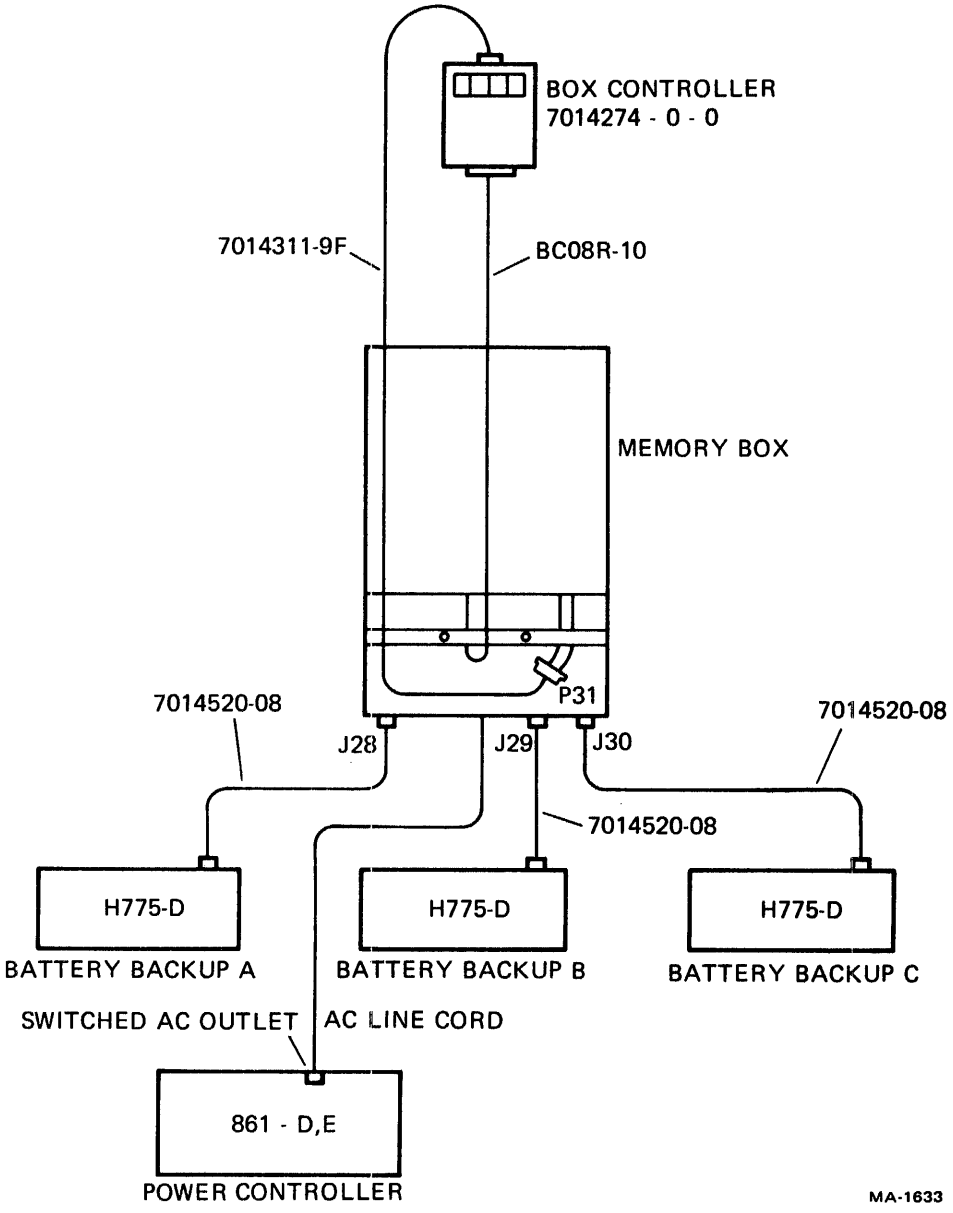


Figure 4-41 MK11 Power Supply External Cabling

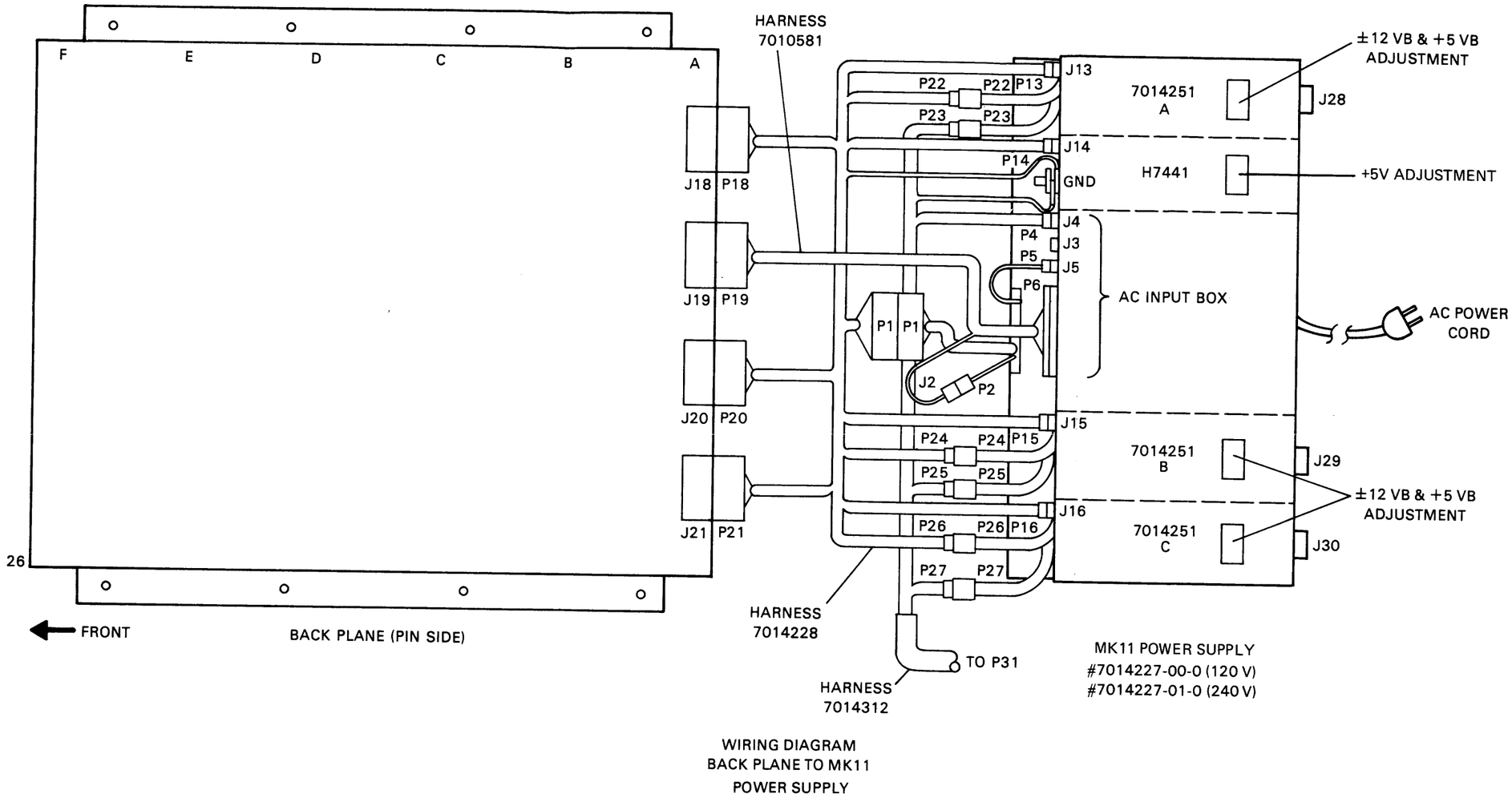


Figure 4-42 MK11 Power Supply Internal Cabling

Power Distribution Harness (7014228) – This harness carries low voltage ac power to the four regulator modules and connects the regulated output voltages to the backplane. Power fail and boot enable signals from the backplane are also sent by the 7014251 regulators via this harness.

Power Monitor Harness (7010581) – This harness carries the power fail signals to the memory backplane from the ac input box.

Box Controller Harness (7014312) – This harness connects the box controller power cable (7014311) to the power supply. It carries the power on signal to the ac input box, and power on and battery status signals between the three 7014251 regulators and P31.

4.4.7.2 Power Supply Major Assemblies

AC Input Box (7009811-1, 2)
The ac input box is mounted in the center of the power supply chassis with three Phillips head screws. A portion of the rear of the power supply chassis is cut out making the ac input box visible from the back of the memory. The ac power cord and a circuit breaker extend through the cutout. The primary function of the ac input box is to switch power to the transformer's primary windings. This assembly consists of a circuit breaker, a power control relay, an ac power control board (5410993), and a power line monitor board (5411086-YA).

The ac power control board operates the power relay that switches primary ac power to the transformer assembly. This allows remote power control for the power supply from the box controller power switch.

The power line monitor board receives a low voltage ac output from the transformer assembly. Sensing circuits monitor the ac voltage and generate the ac low and dc low signals for the memory if power is lost. Two LEDs indicate the generation of the power fail signals by turning off, flagging the memory that is the source of the ac low and dc low signals. Under normal conditions (ac low and dc low not asserted) these LEDs are lit.

Transformer Assembly (7011486)
The transformer assembly is located in the center of the power supply chassis. Two capacitors, two varistors, and two terminal boards are mounted directly on the transformer. Single phase 115 Vac or 230 Vac is stepped down by the transformer to approximately 30 Vac. There are five separate secondary windings, one for each regulator module and one for the power line monitor board. The cooling fans receive 115 Vac from the primary windings. The two capacitors filter the input line voltage and the varistors suppress voltage spikes that occur on the ac input voltage.

+5 Vdc Regulator (H7441)
The H7441 module mounts in the power supply chassis to the right of the transformer assembly (as viewed from the front.) It is secured in the chassis by three Phillips head screws. The input to the regulator is 30 Vac from one of the transformer's secondary windings; its output is a regulated +5 Vdc at up to 32 A.

The H7441 is a switching regulator and provides both overcurrent and overvoltage protection. An overcurrent sensing circuit protects the regulator from shorted loads. The current overload is a foldback type; the output voltage is decreased by limiting the duty cycle of the switching regulator to decrease the output current. Overvoltage protection is provided by an overvoltage crowbar circuit that shunts the output current to ground through an SCR when the output voltage exceeds 6 V.

An LED, visible from the bottom of the regulator (near the voltage adjustment potentiometer), lights whenever +5 V is present at the output of the regulator.

±12 VB and +5 VB Battery Backup Regulators (7014251) and Battery Backup Units (H755D)
The three 7014251 modules mount in the power supply chassis in the locations shown in Figure 4-40. Each regulator is secured in the chassis by three Phillips head screws. The regulators are cabled to their battery backup units through cutouts at the rear of the power supply chassis. The battery backup units are housed in their own enclosures that mount in the memory cabinet. Figure 4-43 is a block diagram of one of the regulator/backup unit pairs.

The ±12 VB and +5 VB regulator consists of a regulator board (5413075), an input rectifier board (5412411), and a controller board (5413073). The rectifier board rectifies the low voltage output from the transformers secondary windings, supplying the raw dc voltage to the rectifier. Raw dc from the rectifier also goes to the battery backup unit to supply the charging current for the batteries. In the regulator, the raw dc is modulated by a switching circuit. Energy in the switched dc waveform is transformer coupled to rectifiers that produce the +12, -12, and +5 V outputs. Regulation is accomplished by changing the duty cycle of the switched raw dc to keep +5 VB at 5 V. The regulator is overcurrent protected by a foldback current limiter and overvoltage protected by a crowbar circuit. The controller monitors the power fail and charge mode signals to control the operation of the batteries and indicate the battery status with the lights in the box controller. Operation of the regulator is enabled by the power switch on the box controller via the signal DC ON. A normally closed thermal switch in the DC ON path opens and shuts off the regulator if an over temperature condition exists.

The battery backup unit contains a battery charger printed circuit board (5411625) and two 12 V batteries (1212499). The battery charger consists of a regulator that supplies the charging current, charge status circuitry, and a relay that connects the batteries to the charger. When the memory is powered up, the controller in the 7014251 regulator connects the batteries to the charging regulator through the relay. The regulator supplies the charging current from the raw dc input, supplying a full charging current until the battery voltage reaches approximately 22 V. After this level is reached, the regulator supplies a trickle charge to maintain the charge on the batteries. The rate of charging is sensed by the charge status indicator circuitry that sends the charge mode signals to the 7014251 regulator.

Loss of ac input power causes the loss of the rectified raw dc from the 7014251 regulator. When this happens, the batteries supply the dc voltage to the regulator in the 7014251 instead of the rectifier board. The regulator will continue to produce +12, -12, and +5 V until the batteries discharge past 18 V. An 18 V reference is used by the relay to disconnect the batteries from the regulator to prevent the batteries from discharging completely.

4.4.7.3 Power Distribution – Figure 4-44 shows the interconnection of all the power supply assemblies identified in the previous paragraphs. Distribution of the power can be traced from the ac line input to the memory backplane with this diagram; specific pin numbers and color coding of wires are found in the field maintenance print set. Locations of the regulated inputs to the backplane are called out in Figure 4-45 which shows the backplane as viewed from the bottom (wire-wrap pin side).

Single-phase ac line voltage is present at the ac input box from the 861-D,E power controller. Turning the power switch on the box controller activates the power relay through the ac power control board. The power relay switches 115 Vac or 230 Vac to the primary windings of the transformer and to the two cooling fans. From the transformer secondary windings the stepped down 30 Vac is routed to the four regulator modules via harness 7014228. The power switch on the box controller also switches on the three 7014251 regulators and the battery backup units.

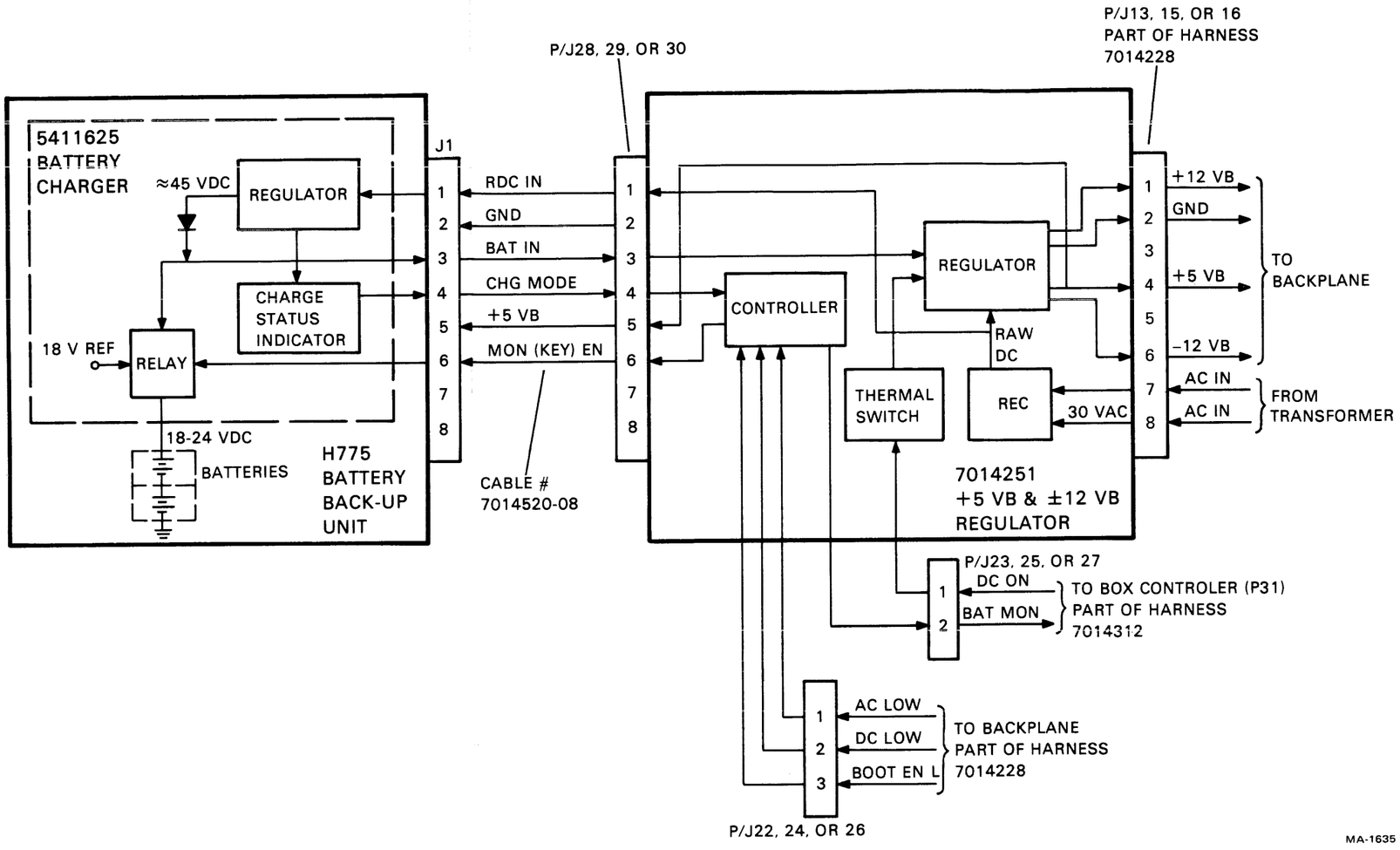


Figure 4-43 Battery Backup Regulator Block Diagram

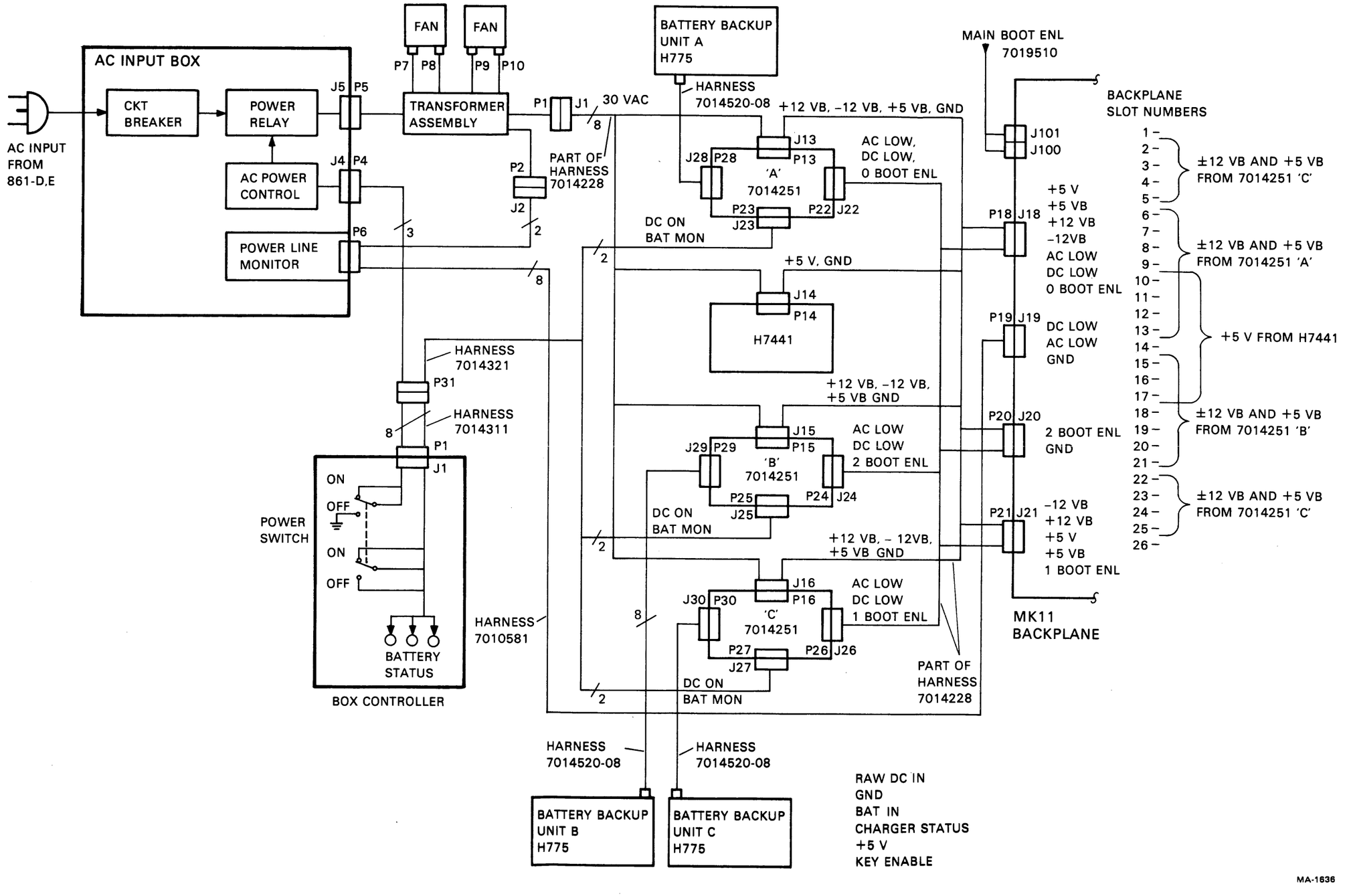


Figure 4-44 MK11 Power Distribution and Control

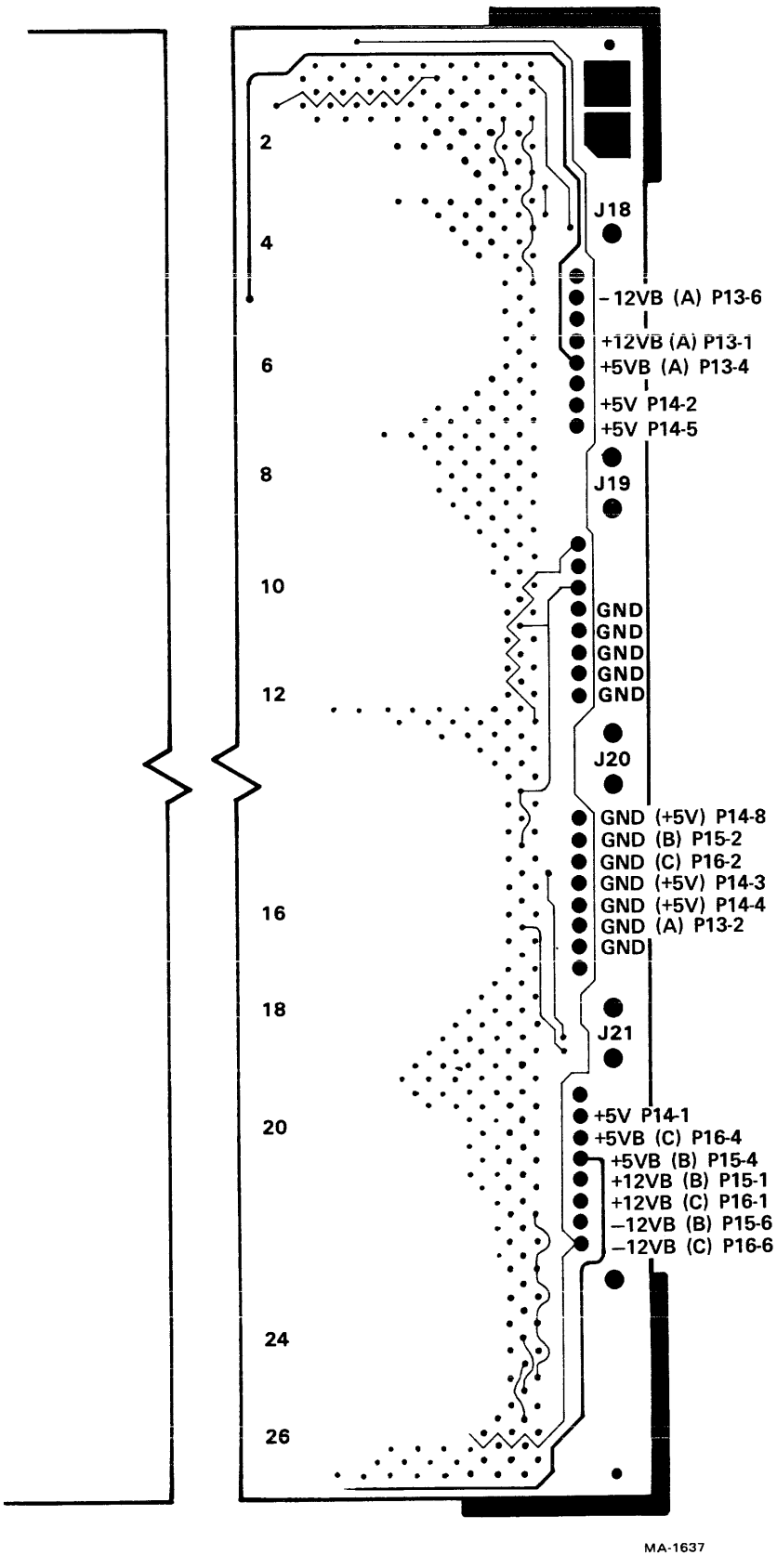


Figure 4-45 MK11 Backplane Power Connections

Thirty volts ac from one of the transformer's secondary windings is rectified and regulated by the four regulator modules. The H7441 +5 V regulated output is carried by harness 7014228 from J14 on the regulator module to backplane connectors J18 and J21 (ground return to J20.) From these connectors, the +5 V are routed to all backplane slots. The +5 V powers all the devices on the address buffer, data buffer, and the four control modules not flagged with asterisks in the schematic diagrams. A LED, on the bottom of the regulator near the adjustment potentiometer, illuminates while the H7441 is producing +5 V.

Three more secondary windings supply 30 Vac to the three 7014251 modules via harness 7014228. Regulator A produces +12, -12, and +5 Vdc (±12 VB, +5 VB) which are carried through harness 7014228 (J13) to the memory backplane connector J18 (ground returns to J20.) From J18, regulator A's voltages go to backplane slots 6 through 13. The A regulator provides power to all the devices indicated with asterisks on the address interface module, the control 0 pair of control A and B modules, and to the array modules in backplane slots 6, 7, 8, and 9.

Regulator B produces +12, -12, and +5 Vdc, which enter the memory backplane via harness 7014228 to connector J21 (ground returns to J20.) The B regulator powers backplane slots 14 through 21, which contain the data buffer module, the control 1 pair of control A and B modules and the arrays in slots 18, 19, 20, and 21. Only the devices indicated with asterisks on the schematic diagrams are powered by the B regulator.

Regulator C sends its ±12 VB and +5 VB voltages to the backplane via harness 7014228 to connector J21 (ground returns to J20.) Its regulated outputs power the array modules in backplane slots 2 through 5 and 22 through 25. Figure 4-45 locates the backplane connector pins that carry the regulated voltages and the source connectors and pin numbers.

A fifth secondary winding on the transformer supplies low voltage ac to the power line monitor located in the ac input box. When power is switched on, the power line monitor switches the dc low signal to a high level and then the ac low signal to a high level. Harness 7010581 carries these dc low and ac low signals to the memory backplane connector J19. The memory monitors the power fail signals from its own power line monitor and power fail signals from the main memory bus. From the backplane, dc low and ac low signals go to the 7014251 regulators (J22, J24, and J26) via harness 7014228. These same cables carry the boot enable signals to the 7014251 regulators. The source of the boot enable signal is cable 7019510, which plugs into connectors J100 and J101 on on memory box no. 0. Other memories in the system obtain the boot enable signal from the main memory bus.

Raw dc, rectified from the 30 Vac, is sent to the battery backup units by the 7014251 regulators via harness 7014520-08. This voltage powers the battery charger and supplies the charging current for the battery pack. The regulated output, +5 VB, also goes to the battery charger. The battery backup units send charger status information to the regulators, which send coded status signals to the box controller via harness 7014312 (P31). These battery monitor signals operate the battery status indicator LEDs in the box controller. The coding is as follows:

OFF, Battery off
SLOW FLASH, Battery receiving full charge
FAST FLASH, Battery supplying power to memory
ON, Battery receiving trickle charge

In the event of a power failure, the batteries in the backup units supply current to the 7014251 regulators which continue to produce their regulated output voltages. Power is then supplied only to the array modules and the devices flagged with asterisks on the schematic diagrams of the address buffer, data buffer, and control A and B modules. Battery power is used by the memory for refresh cycles only, no other memory cycles are allowed to run.

4.5 MAINTENANCE

Maintenance of the PDP-11/70 power system is discussed in the following paragraphs. Included are the preventive and corrective maintenance procedures for the 861-D, -E power control, the H7420 power supply, and the memory power supply. H7420 and memory subassembly removal procedures are also described.

The most important point in maintenance philosophy is that the user understand the normal operation of the PDP-11/70 power system as previously described in this chapter. A thorough comprehension of this information, plus the maintenance procedures described, are the best tools the user has to isolate and correct malfunctions.

4.5.1 861-D, -E Power Control

The 861 power controllers are constructed of high quality components (Figures 4-46 and 4-47) and can therefore be expected to provide trouble-free performance for extensive periods. No adjustment or alignment procedures exist. No special tools or equipment are required and no fuses are utilized. A 5000 Ω/V multimeter is adequate for accomplishing all voltage and resistance measurements.

Preventive maintenance procedures for the power controllers consist of periodic cleaning and inspection to detect any mechanical damage to wiring and components or evidence of overheating, etc. The operation of the thermal switch can be checked by holding a flame close to the sensing element while the controller is operating and observing that the switched outlets become disabled. Emergency shutdown response to devices on the signal bus can also be checked as a preventive maintenance procedure by connecting pins 3 and 2 of the remote switching control bus. Should a failure occur, proceed as described in the following paragraphs.

WARNING

Dangerous potentials exist within the power controller. Perform all measurements with properly insulated meter leads. Remove the main power plug before attaching or removing test leads.

Failures within the power controller occur in one of three failure modes:

1. No output (circuit breaker trips)
2. No output (circuit breaker not tripped)
3. No control (including emergency shutdown and overtemperature)

The flowcharts in Figures 4-48 and 4-49 present a logical troubleshooting sequence for the three failure modes.

4.5.1.1 No Output (Circuit Breaker Tripped) – If correct power is available from the mains, a tripped circuit breaker can be caused only by: a faulty circuit breaker, a low resistance load, or a low resistance within the power controller caused by component failure.

4.5.1.2 No Output (Circuit Breaker Not Tripped) – Failures within this mode are caused by: bad cable connections, open components in the line filter, improper relay operation, or a faulty circuit breaker.

4.5.1.3 No Control – Control failures are associated only with the switched outlets; the input circuits, line filter, and main circuit breaker are therefore not involved. These failures are caused by bad cable connections, secondary circuit breakers, relays, and diodes. A faulty thermal switch, T1, can cause loss of control. Control problems can be isolated to either the internal or external circuit by use of the LOCAL/OFF/REMOTE switch. With the switch in the LOCAL position, if T1 is operating properly, the switched outlets should be enabled. If not, the problem is within the controller circuitry. If operation is normal when in LOCAL, check the control signals from the external device.

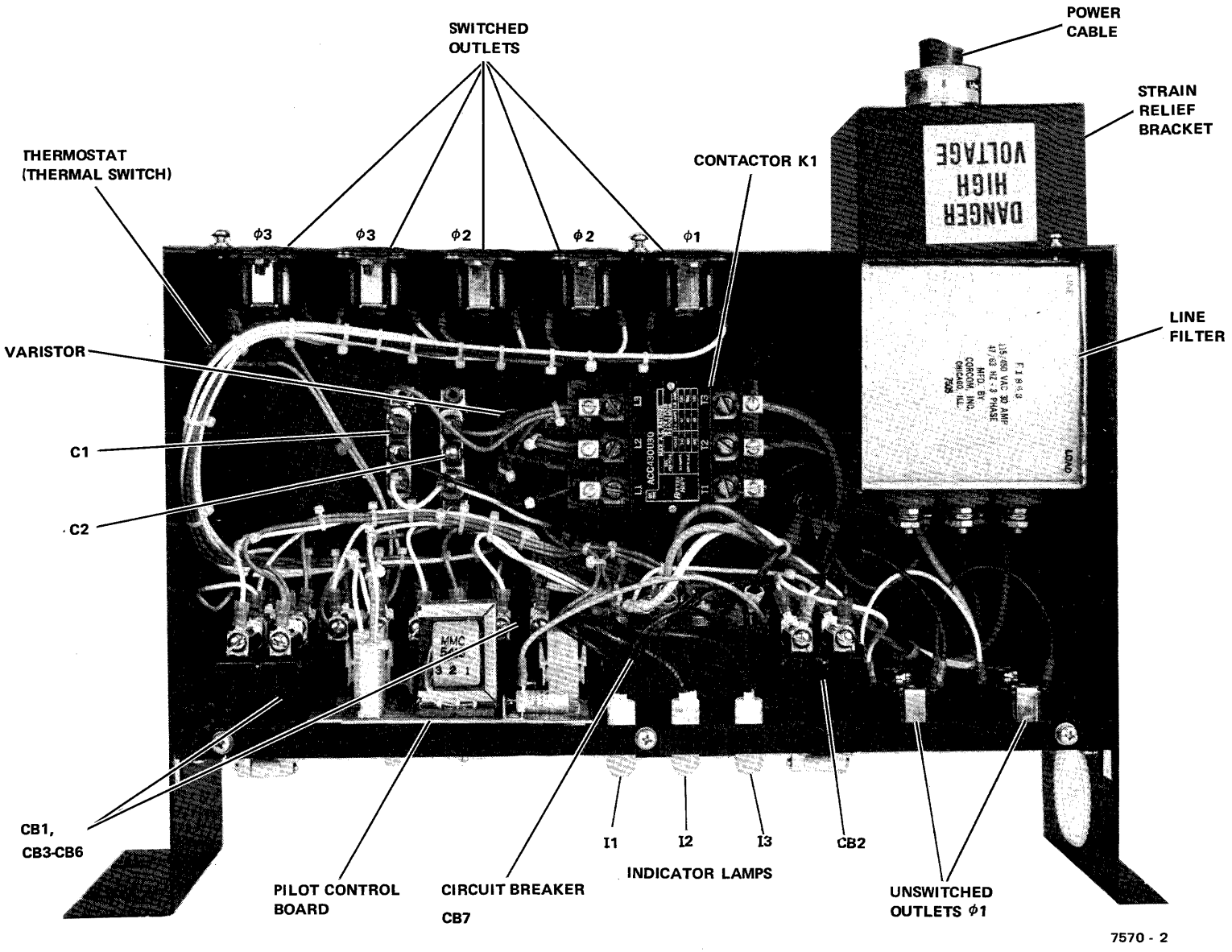


Figure 4-46 861-D Power Control Component Identification

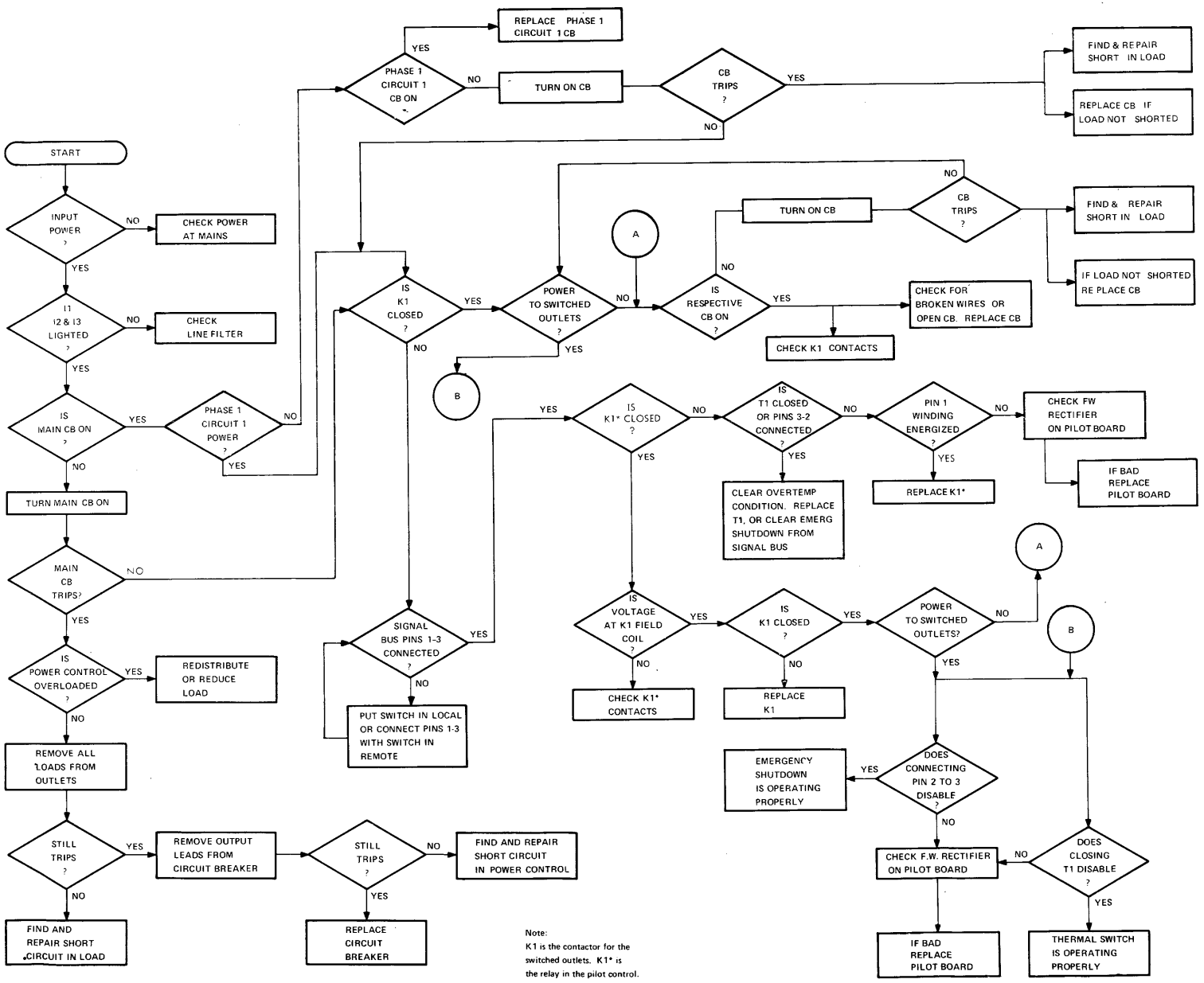


Figure 4-48 Troubleshooting Flow Diagram – 861-D

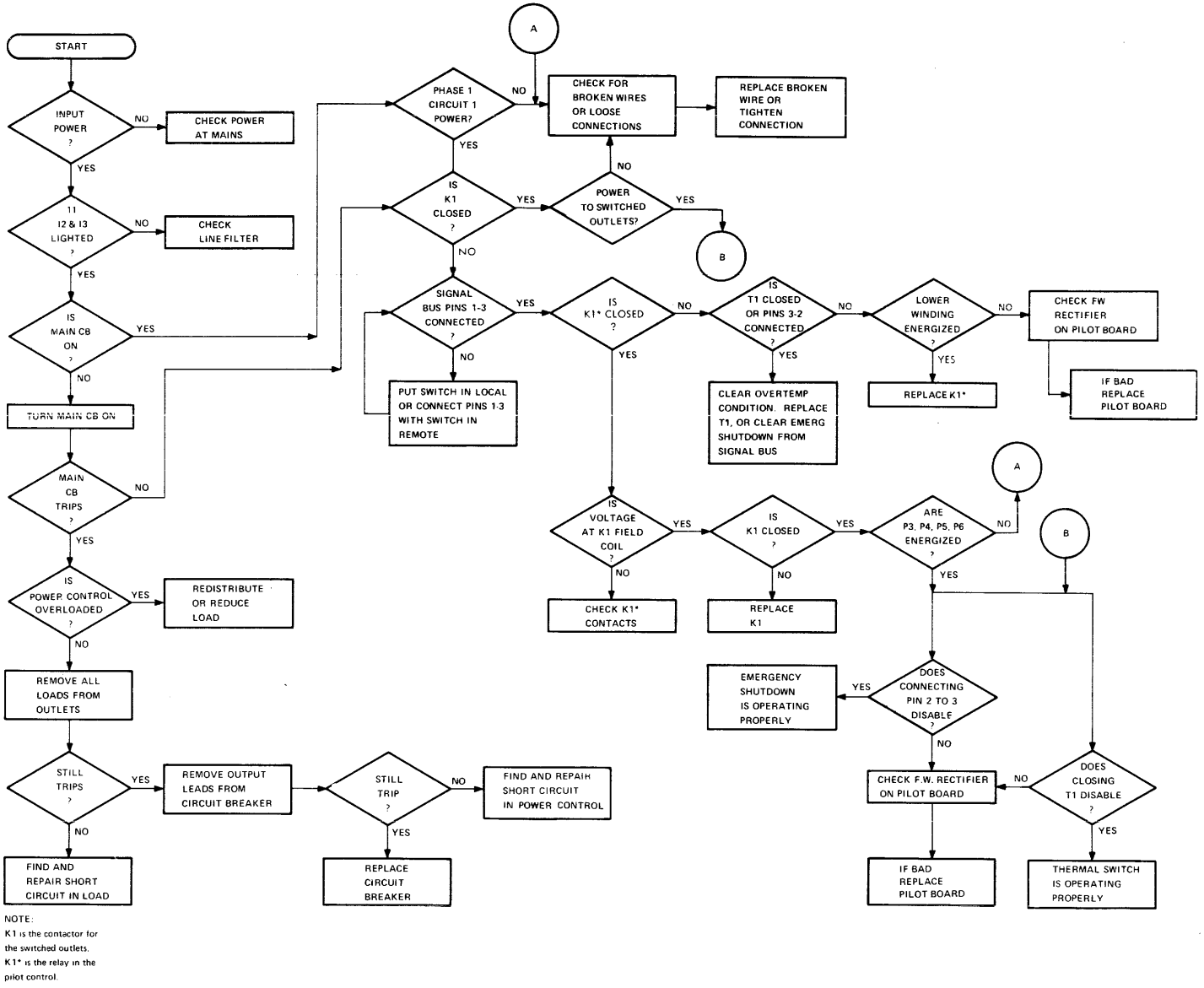


Figure 4-49 Troubleshooting Flow Diagram – 861-E

A digital voltmeter (Weston Schlumberger DVM Model 4443 or Data Technology Model 21) should be used for making the regulator voltage measurements. A calibrated oscilloscope may be used if a DVM is not available. An oscilloscope is necessary for measuring ripple voltage. A VOM is useful for making continuity and resistance checks within the power supply.

Visual Inspection

CAUTION

Make sure all power is off before performing the following steps.

1. Check all fans to ensure that they are not obstructed in any way. Clean air filters mounted on the inside of the cabinet door if required.

2. Visually inspect the modules and backplane for broken wires, connectors, or other obvious defects.

3. Inspect all wiring and cables for cuts, breaks, frays, deterioration, kinks, strain, and mechanical security. Repair or replace any defective wiring or cable covering.

4. Inspect the following for mechanical security; power supply regulators, fans, capacitors, etc. Tighten or replace as required.

5. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace as required.

Voltage Measurements (MJ11) – Turn on power and open the memory cabinet door. With a DVM, or a calibrated oscilloscope, measure the dc voltages at the M8149 regulator test points (Figure 4-50 and drawing D-CS-M8149-0-1, sheet 1). The procedure is described in Appendix G. Using an oscilloscope, measure the peak-to-peak content of all dc outputs. Table 4-7 lists the test points, the associated voltages and regulators, and the regulator and backplane connections. (Regulator specifications are listed in Table 4-19; regulator adjustments are described in Paragraph 4.5.2.2).

Voltage Measurement (MK11) – Turn on power and measure the +12 VB, -12 VB, +5 VB, and +5 V voltages at J18 and J21 of the memory backplane with a DVM (Figure 4-45). All voltages must be within ±5 percent tolerance as listed in Tables 4-18 and 4-19. If a voltage is found to be out of tolerance, perform the required voltage adjustment.

4.5.2.2 Memory Power Supply Corrective Maintenance – Before any adjustment procedure is undertaken, the MJ11 power supply should be inspected to ensure that the equipment is energized:

1. Check that the memory cabinet 861 power control indicators light.
2. Check that all fans are energized.
3. Check that all regulator indicators light.

Voltage Regulator Adjustments

NOTE

Read the entire procedure before making any adjustment.

The voltage regulator outputs (Table 4-17) must be adjusted to the tolerances indicated in Table 4-19. When performing the adjustments, ensure that the maximum voltages at the regulator are not exceeded. These voltages represent the maximum regulator voltage prior to crowbar. Figure 4-51 shows the location of the voltage regulator adjustment protentiometers.

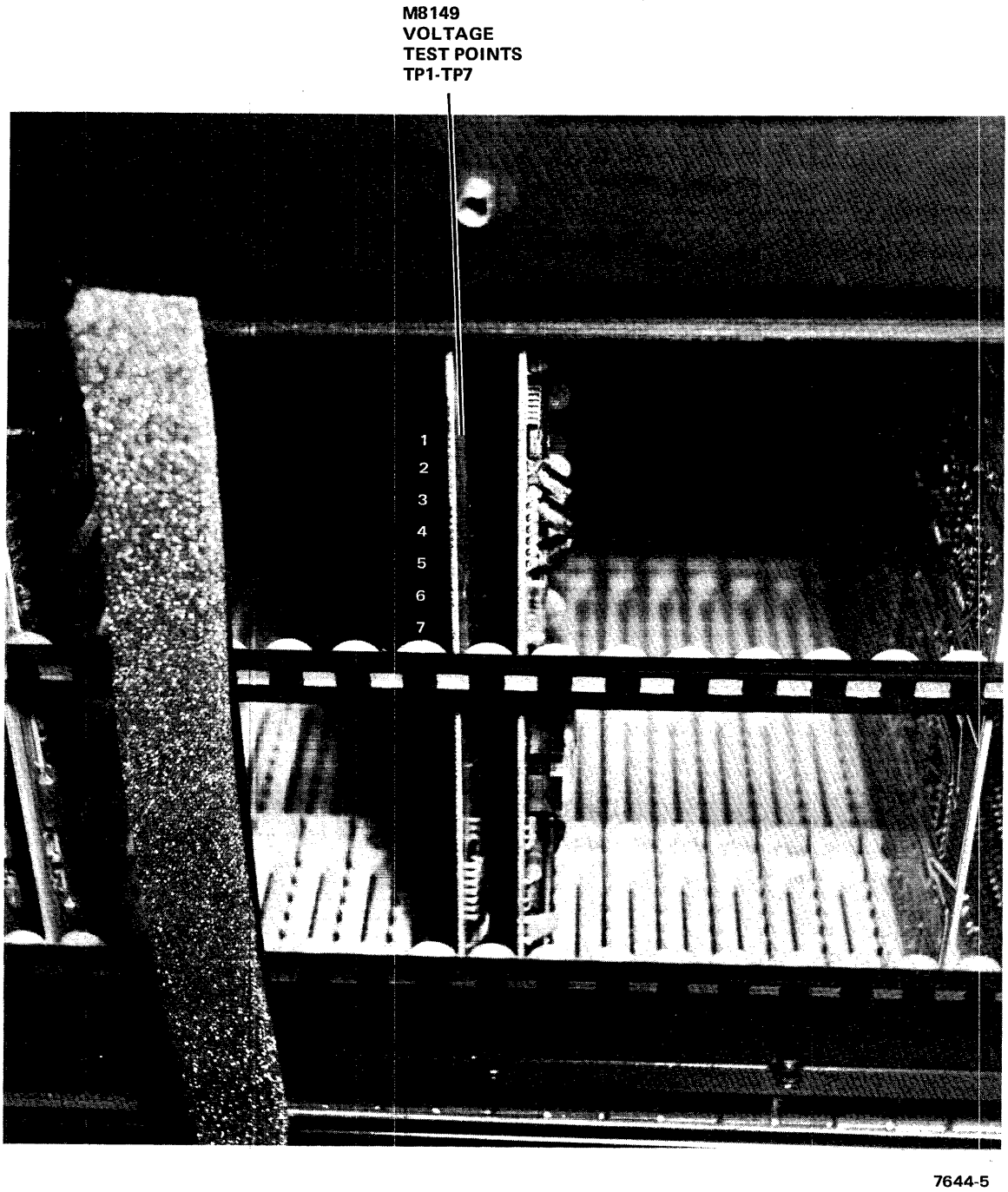


Figure 4-50 MJ11 Voltage Test Points

Table 4-17 Regulator Test Points (MJ11)

M8149 Test Point	Regulator	Voltage (Vdc)	Regulator Pins	Backplane Connector Pins
TP1	744 No. 4	+5	J16-2,5	J21-5,6,7,8
TP2	744 No. 2	+5	J14-2,5	J18-1,2,3,4
TP3	754 No. 3	+20	J15-5	J21-3,4
TP4	754 No. 1	+20	J13-5	J18-5,6
TP5	754 No. 3	-5	J15-3	J21-1,2
TP6	754 No. 1	-5	J13-3	J18-7,8
TP7		TP Ground		

Table 4-18 Regulator Voltage Measurements (MK11)

Regulator	Voltage	Regulator Pins	Backplane Connector Pins	Backplane Slots Supplied
H7441	+5 Vdc	J14-1, 2, 5	J18-1, 2 J21-7	10–17
7014251 'A'	+5 Vdc	J13-4	J18-4	6–13
	+12 Vdc	J13-1	J18-5	6–13
	-12 Vdc	J13-6	J18-7	6–13
7014251 'B'	+5 Vdc	J15-4	J21-5	15–21
	+12 Vdc	J15-1	J21-4	15–21
	-12 Vdc	J15-6	J21-2	15–21
7014251 'C'	+5 Vdc	J16-4	J21-6	2–5, 22–25
	+12 Vdc	J16-1	J21-3	2–5, 22–25
	-12 Vdc	J16-6	J21-1	2–5, 22–25

Table 4-19 Regulator Specifications

Regulator	Voltage and Tolerance at Backplane	Maximum Voltage at Regulator (Note 1)	Maximum Output Current Capability
H744	+5 Vdc ±250 mV	5.5 Vdc	25 A
H754 (Note 3)	+20 Vdc ±1 V -5 Vdc ±250 mV	21.5 Vdc -5.5 Vdc	8 A 1-8 A (Note 2)
H7441	+5 Vdc ±250 mV	5.5 Vdc	32 A
7014251	+5 Vdc ±250 mV ±12 Vdc ±600 mV	6.0 Vdc 13 Vdc	4 A 2 A

Regulator	Output Current Under Maximum Load (Per Regulator)	Maximum Peak-to-Peak Ripple
H744	17 A	0.2 Vdc
H754 (Note 3)	7.5 A 1.75 A	1.0 Vdc 1.0 Vdc
H7441	27 A	0.2 Vdc
7014251	3.5 A 1.3 A	1.0 Vdc 1.0 Vdc

NOTES:

1. Do not adjust the regulator to these voltages. They represent the maximum regulator voltage prior to crowbar.
2. Maximum -5 V current is dependent upon +20 V current. It is equal to 1 A plus the current of the +20 V supply up to a total of 8 A.
3. When adjusting the output of H754, adjust +20 Vdc first, then -5 Vdc. Refer to the H754 voltage regulator adjustment procedure.

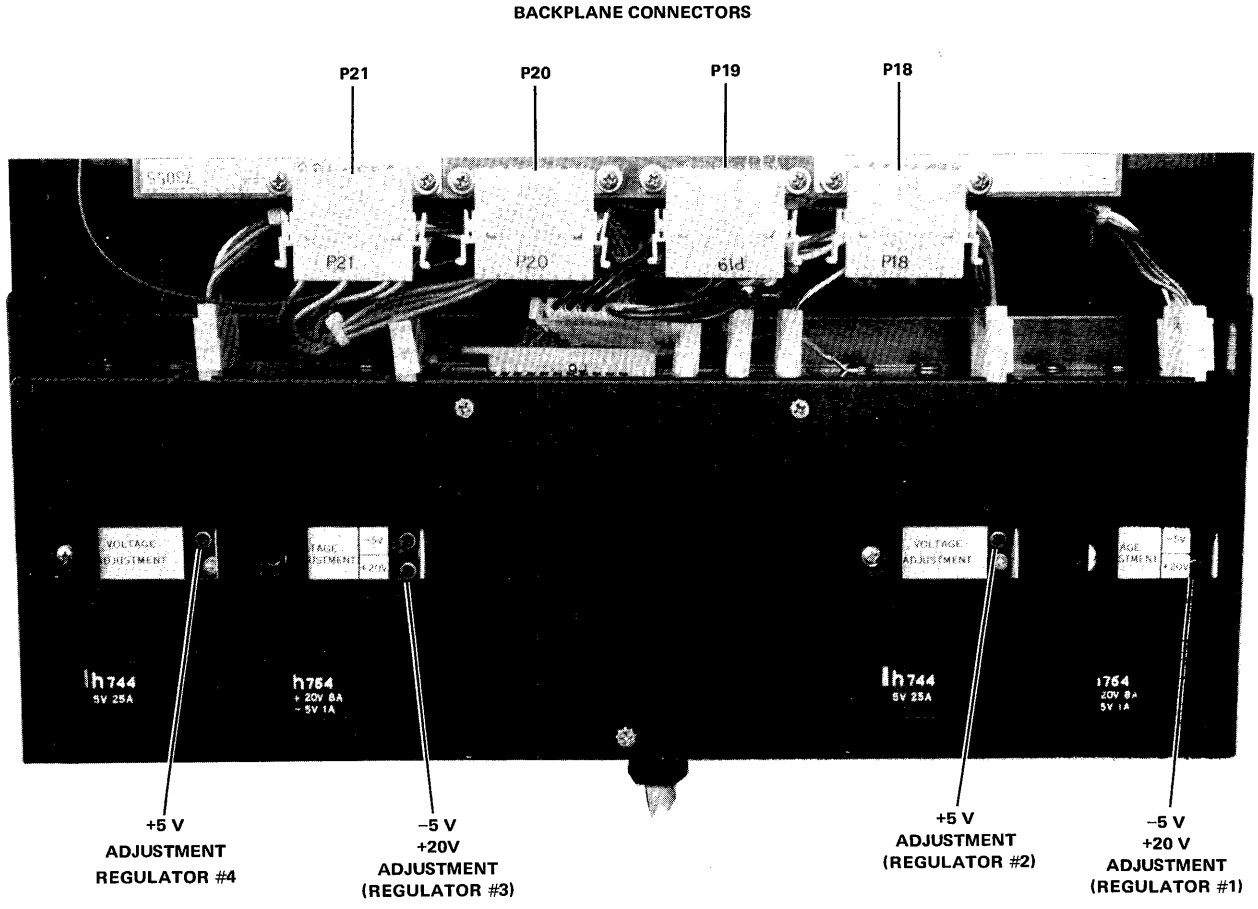


Figure 4-51 Regulator Adjustments

Correct power system voltages at the backplane are critical to a properly operating system. If a voltage regulator cannot be adjusted to meet the required tolerance, check for a faulty regulator or harness.

The regulator replacement procedure is described in Paragraph 4.5.2.3.

H754 Voltage Regulator Adjustment (+20 V, -5 V)

1. Power down the equipment.
2. Fully extend the memory frame from the rack, ensuring that the cables do not bind.
3. Refer to Figure 4-53. Pull the chassis slide operating handle to release the slide latch. Carefully rotate the memory frame 90 degrees to the upright position.
4. Power up the equipment.
5. Connect a digital voltmeter across the +20 V and -5 V test points (M8149) of the H754, i.e., TP3 and 5 or TP4 and 6.
6. Adjust the +20 V potentiometer (Figure 4-51) for a +25 V reading.
7. Connect the digital voltmeter between the -5 V and ground test points on the M8149, i.e., TP5 and 7 or TP6 and 7.
8. Adjust the -5 V potentiometer for -5 V. This procedure is necessary because the +20 V potentiometer (R17) actually sets the overall output of the regulator (25 V from +20 V to -5 V), while the -5 V adjustment (R21) controls the -5 V to ground output. (See Drawing D-CS-H754-0-1.)
9. Recheck the voltages at the M8149 test points, and if necessary, readjust the outputs.
10. Power down the equipment.
11. Return the memory frame to its original horizontal position (steps 2 and 3 above in reverse) or perform the +5 V adjustment described below (steps 3, 4, 5, and 6).

H744 Voltage Regulator Adjustment (+5 V)

1. Perform the procedure described above in steps 1, 2, and 3 of the H754 voltage regulator adjustment.
2. Power up the equipment.
3. Using a digital voltmeter, measure the +5 Vdc output voltages under normal load conditions at the M8149 test points (Table 4-17).

   Adjust voltages (Figure 4-51) at the backplane to the tolerances specified in Table 4-18 as required.
4. Power down the equipment.

5. Pull the chassis slide operating handle to release the slide latch. Carefully rotate the memory frame down to the horizontal position.

6. Carefully push the memory frame back into the cabinet, observing that the cables do not bind.

H7441 Voltage Regulator Adjustment, +5 V

1. Using a digital voltmeter, measure the voltage at J18 pin 1 or J21 pin 7 under normal load conditions.

2. Adjust the voltage to +5 V; see Figure 4-52 for location of adjustment potentiometer.

If the voltage cannot be adjusted to +5 V, check for faulty regulator or harness.

7014251 Voltage Regulator Adjustment, ±12 VB and +5 VB

1. Using a digital voltmeter, measure the voltage of +5 VB (A) at the backplane under normal load conditions. Figure 4-45 shows the backplane pin connections.

2. Adjust the voltage to +5 V; see Figure 4-52 for the location of the adjustment potentiometer.

3. Measure the voltage of +12 VB (A) and -12 VB (A).

4. Repeat Steps 1-3 for the +5 VB (B), ±12 VB (B) and +5 VB (C), ±12 VB (C) voltages.

If the +5 VB voltages cannot be adjusted to +5 V or if the ±12 VB voltages are out of tolerance, check for faulty regulators or harness.

4.5.2.3 Memory Power Supply Fault Isolation - The memory frame power supply consists of field replaceable modules. Once a power system failure is discovered, the following steps and associated flowchart (Figure 4-46) can be utilized to isolate to a faulty module:

1. Ensure that the power supply is plugged in and getting primary ac power (115 Vac/230 Vac).

2. Check CB1 on the ac input box.

3. Check the fans for proper operation.

4. Check the two LEDs on the 5411086-YA power line monitor. Both can be seen through the vent slots on the ac input box (Figure 4-29). They should be ON during normal operation, i.e., AC LO and DC LO not asserted (Paragraph 4.4.6.1).

5. Utilizing the flowchart (Figure 4-54) and power system schematic (drawing 7010694-0-0), isolate the faulty module.

6. Replace the module as described in Paragraph 4.5.2.4.

7. When a fault is isolated to a voltage regulator, refer to Paragraph 4.5.2.2 for voltage regulator checks and adjustments.

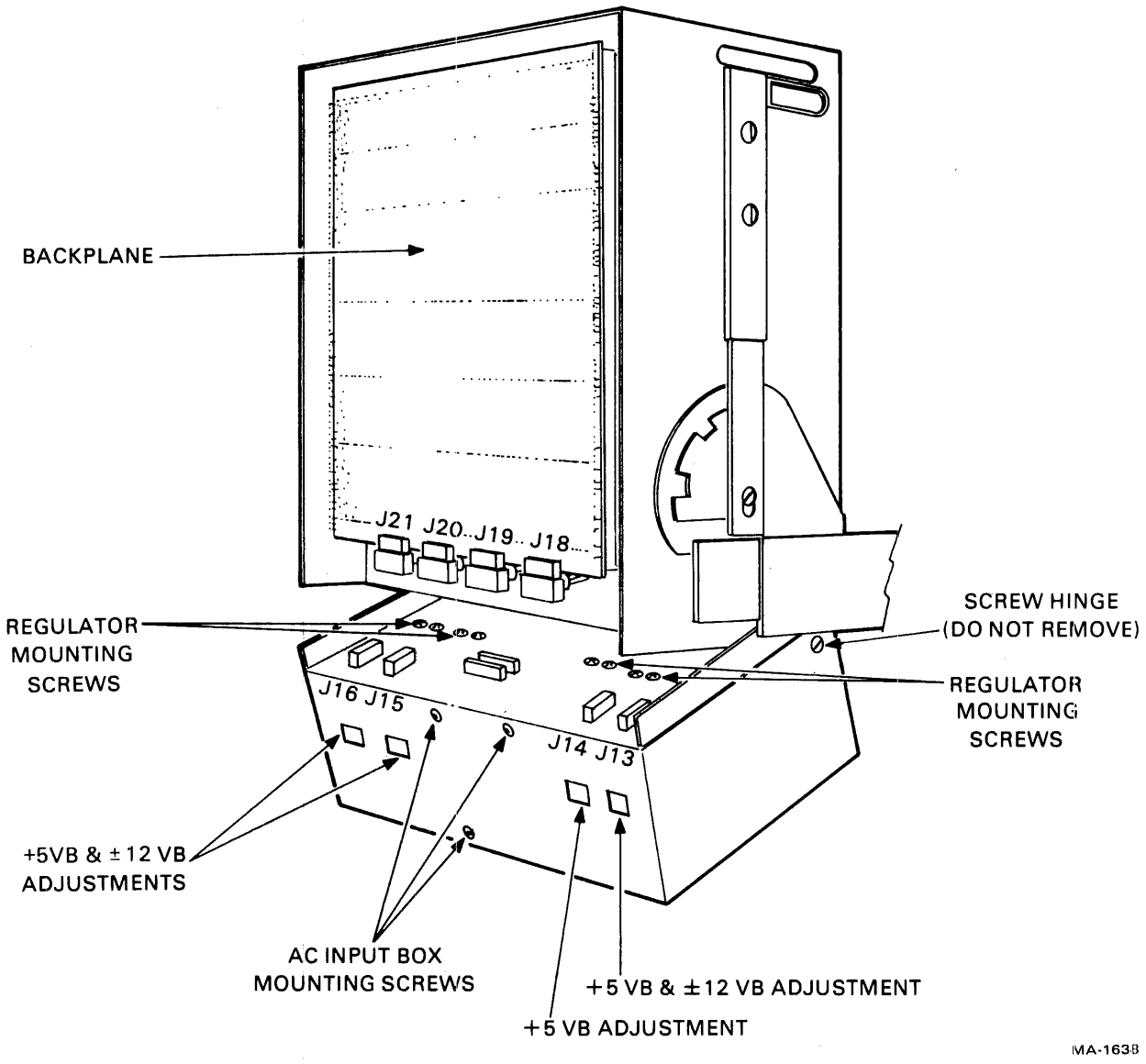


Figure 4-52 MK11 Power Supply in Maintenance Position

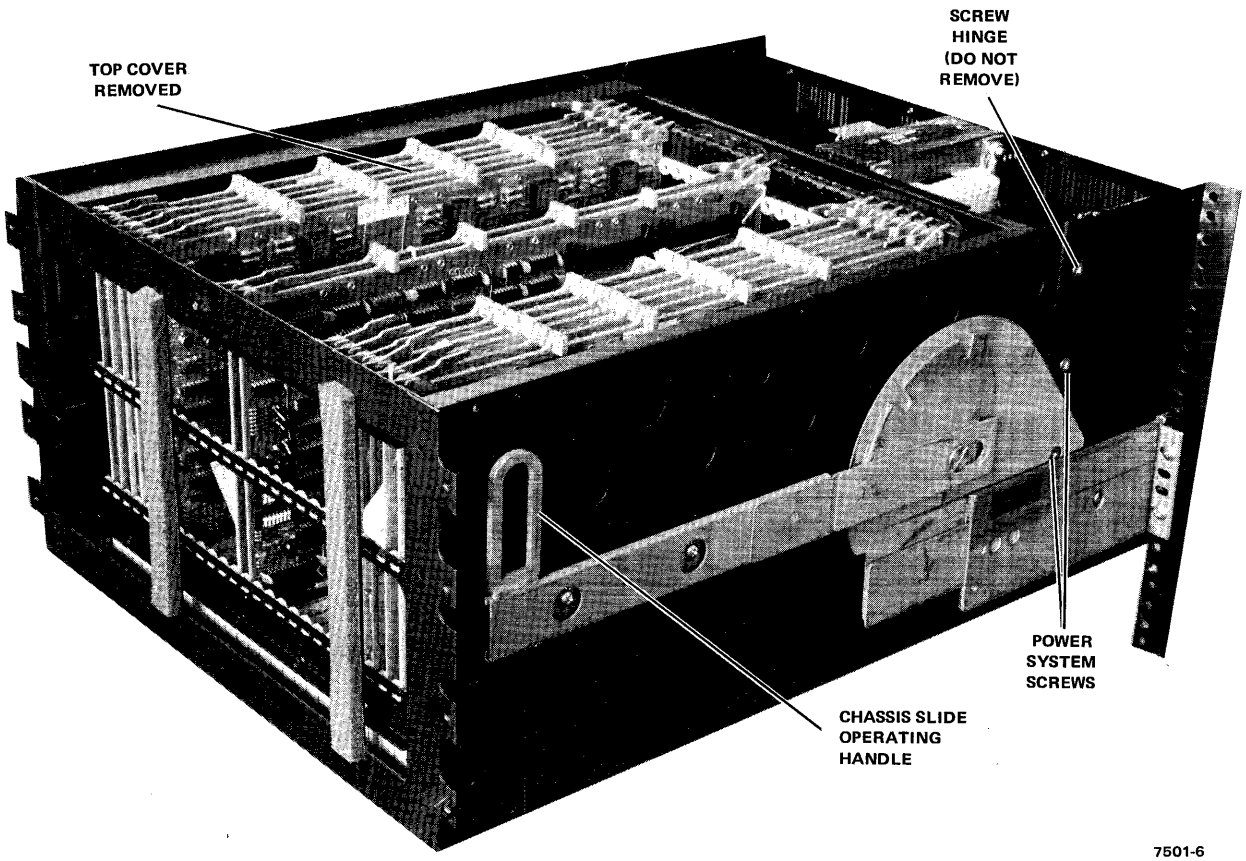


Figure 4-53 Power Supply Access (Main Memory Bus Cables Not Shown)

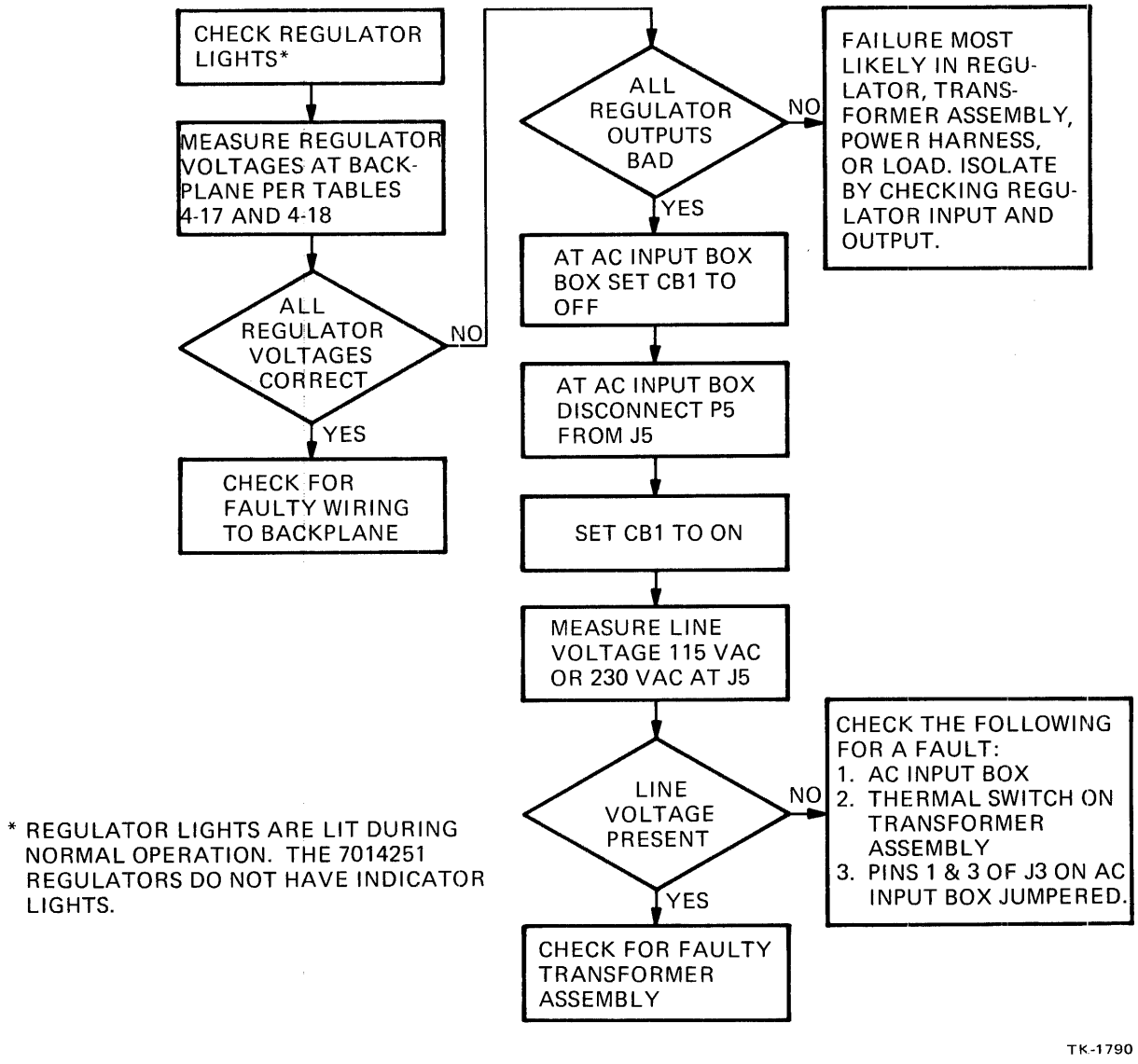


Figure 4-54 Memory Frame Power Supply Fault Isolation Flowchart

Voltage Regulator Troubleshooting – The voltage regulators are designed to be replaced when a failure is detected. However, there are unique situations when a regulator must be repaired in the field. Table 4-20 lists the primary fault indications, the most probable cause, and corrective action required. This table should be used in conjunction with the regulator's theory of operation (Paragraph 4.4.6.2) and the print set.

Once the repairs have been accomplished or a new regulator is installed (Paragraph 4.5.2.4), refer to Paragraph 4.5.2.2 for voltage regulator checks and adjustments.

Table 4-20 H744, H754 Voltage Regulator Troubleshooting Chart

Fault Indication	Most Probable Cause	Corrective Action
No output voltage	1. Q2, Q3, Q4 and Q5	Replace regulator or transistor.
	2. D5	Replace regulator or diode.
	3. D1 (bottom of D1 will appear burnt)	Replace regulator or D1.
	4. Faulty crowbar Q6 and Q7	Replace regulator or transistor.
	5. E1 (DEC 723, IC voltage regulator)	Replace regulator or E1.
	6. Misadjusted output voltage	Shut power off and turn voltage adjust fully ccw (below crowbar voltage). Turn power on and slowly increase voltage (Table 4-18) until correct value is obtained.
Blown fuse	1. Q2 (pass transistor)	Replace voltage regulator or pass transistor and associated components
	2. Excessive loading of voltage regulator	Replace fuse and check loads

Regulator Bench Test Procedures (H744 and H754) – The following paragraphs suggest procedures to troubleshoot and test the H744 +5 V regulator and H754 +20 V, -5 V regulator modules. The procedures are intended to aid in locating a fault, provided the fault has not destroyed the etched circuits.

When replacing a faulty voltage regulator, the new voltage regulator may need adjustment to compensate for the load. If the new regulator is initially adjusted too high, it may activate the crowbar circuit and provide no output when initially installed. If this happens, turn power off and rotate the adjustment potentiometer counterclockwise. Then reapply power (regulator should not crowbar) and adjust the regulator output.

Initial Tests – When a power system fault has been isolated to a voltage regulator (H744 or H754), examine internal fuse F1 (Figure 4-45). A blown fuse usually indicates that the main pass transistor Q2 and/or one of its drivers Q3 or Q4, has short-circuited.

1. Check for constantly tripped crowbar SCR. (V out = +1 to +1.5 Vdc and regulator "sings" too loud.)

2. Check for damage to base-emitter bleeder resistors and a scorched etched board in the area of Q3 (and Q4 if applicable).

3. If the pass transistor and drivers check OK on a VOM, the fault may be caused by continuous base drive to the first driver, Q4 (Q3 in H754). Check level shifter Q5 for a short circuit.

4. Check D5 for a short. A shorted D5 will usually destroy Q2, Q3, and Q4. Consequently, if the latter are bad, check D5 before powering up.

5. Check the resistance to ground at the input to precision voltage regulator integrated circuit E1 (pins 4 and 5) to determine if an external short circuit is affecting the IC.

6. Use the VOM to check for a short circuit between fuse terminals and ground. Possible short circuits involving mounting TO-3 components to the heat sink may be located by connecting VOM leads between TO-3 cases and a regulator bracket mounting screw on the end of the heat sink.

Output Short Circuit Tests – A voltage regulator that provides no output or low output without causing fuse F1 to blow, is probably working into a short-circuited output.

NOTE

An activated crowbar or a short-circuited output in an otherwise properly operating voltage regulator will not cause F1 to blow.

1. If fuse F1 is not blown and the area of etched circuit around the ac input to the bridge circuit is not damaged, it is safe to apply an ac input to the voltage regulator to determine if the regulator is overloaded by a short circuit across the output.

2. Connect the voltage regulator to a test bench source (Figure 4-56) and advance the Variac to about 90 V (20 Vac at voltage regulator input). If the output is near 0 V, turn the voltage adjustment fully counterclockwise and repeat the test.

3. If the regulator appears overloaded, check for a short circuit across the output and for a component failure in the crowbar circuit.

Testing a "Dead" Regulator – Use the following procedure to test a faulty regulator that does not exhibit the symptoms just described.

1. Apply 115 Vac to the test bench source (25 Vac at the voltage regulator input), with no load on the regulator output.

2. Check for 30 Vdc across filter capacitor C1 (and C2 if applicable).

3. Check for +15 Vdc at pin 12 of precision voltage regulator E1. No voltage at this point could mean zener diode D2 (H744) or D3 (H754) has failed.

4. Check for 6.8 – 7.5 Vdc at pin 6 of E1 with respect to ground, pin 7.

5. If all voltage measurements steps 2, 3, and 4 are OK and there is no output voltage, pin 5 of E1 should be positive with respect to pin 4.

E1, pin 2, should be +0.6 V with respect to pin 3. If it is not, connect the emitter and base of Q5. If a 0.6 V indication is obtained, precision voltage regulator E1 is OK and the fault is probably caused by Q5 or Q4 (Q3 in H754).

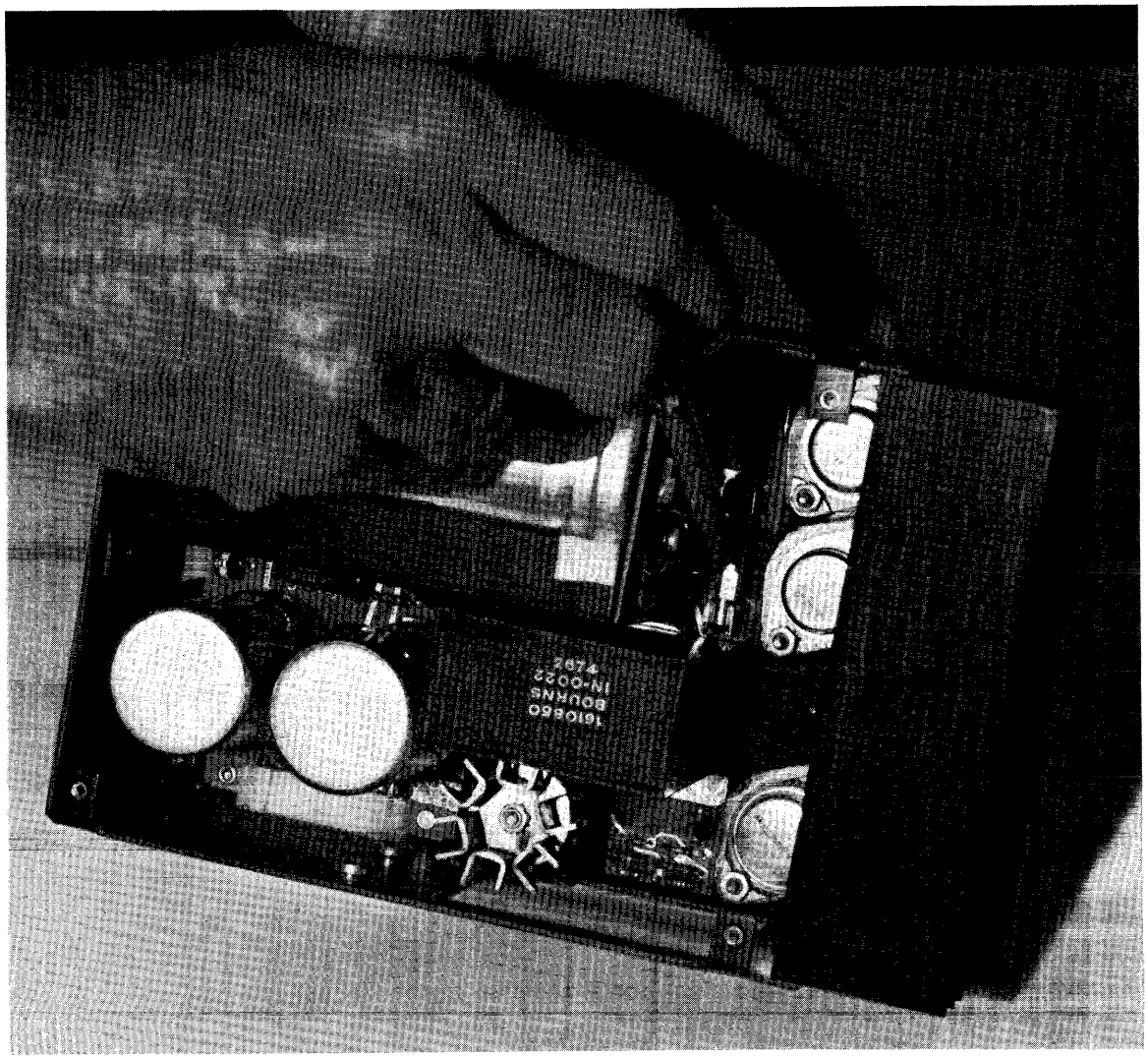


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Figure 4-55 H744 Regulator Fuse Location

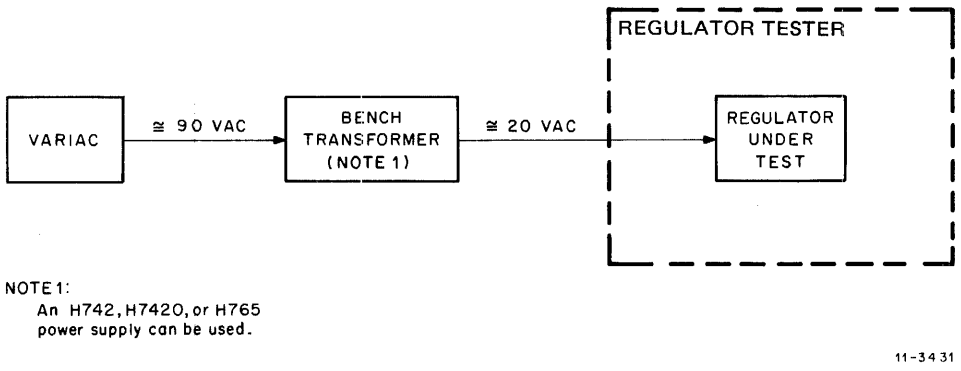


Figure 4-56 H744, H754 Bench Check

Testing a Voltage Regulator After Repairs – Before returning a repaired voltage regulator to service, it should be checked as follows:

1. Connect the repaired voltage regulator to the appropriate source connector.
2. Set the voltage adjustment fully counterclockwise and set the load to zero.
3. Close the input circuit breaker and advance the Variac until output voltage is indicated (at approximately 60–80 Vac input). No audible noise should be heard under no-load conditions.
4. Be sure Q2 is connected and soldered before loading the regulator.
5. Advance the Variac to 130 Vac and return to 115 Vac.
6. Apply a 30–50 percent load. The output voltage should remain nearly constant. A clean whistle may be heard. A buzz or harsh hissing sound indicates possible instability. Check waveforms as indicated in Figure 4-57.
7. Apply 100 percent load and set the voltage adjustment for nominal output as listed:

H744	+5.10 Vdc
H754	+25 Vdc between +20 and –5 outputs

8. Apply 200 percent load and clock for a decrease in the frequency and the output voltage.

CAUTION

If the output voltage does not decrease noticeably (approximately 1 V on H744, or 1 to 5 V on the H754), do not attempt the following short circuit test.

9. Short circuit the output. The regulator should continue to operate at a low frequency with a clean, smooth whistle and stable waveforms.

10. Increase the voltage adjustment and observe the output voltage when the crowbar circuit fires. The output voltage should be within the following ranges:

H744	6.00 – 6.65 V
H754	25.0 – 30.0 V and -6.00 to -7.00 V

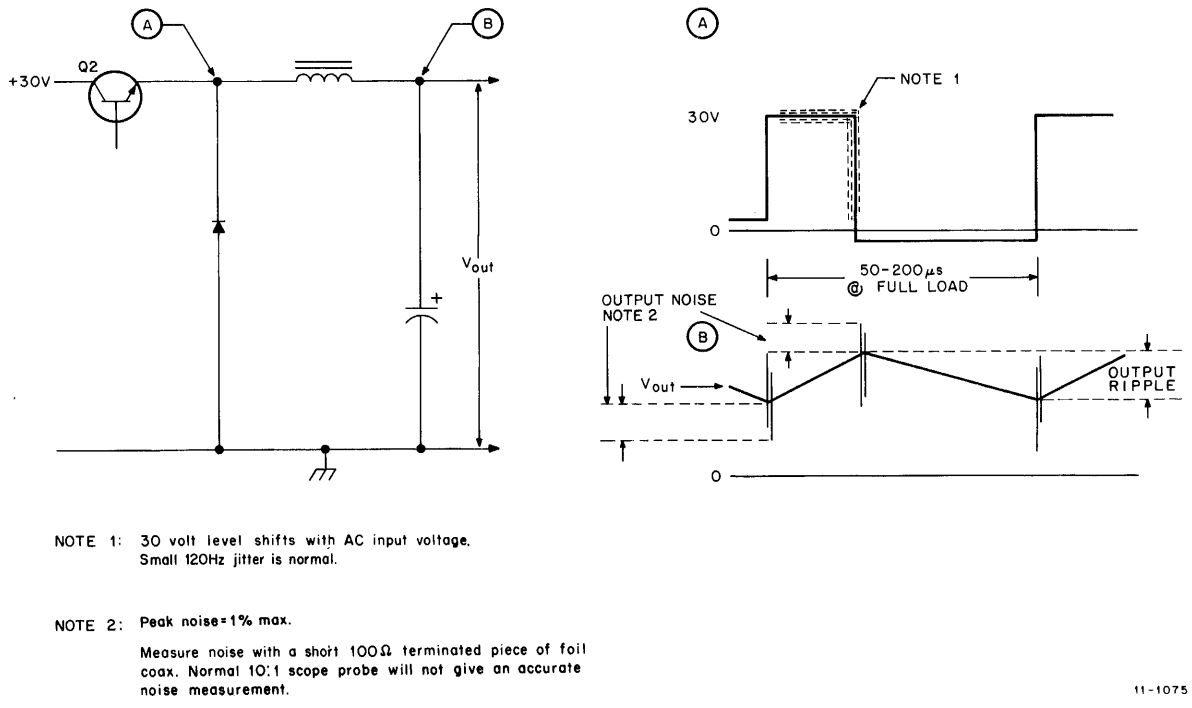


Figure 4-57 Typical Voltage Regulator Output Waveforms

4.5.2.4 Memory Power Supply Subassembly Removal Procedure – The power supply access procedure enables the supply to be accessed for adjustments and subassembly removal. The removal procedures include:

1. Power supply access procedure
2. H744, H754, H7441, and 7014251 regulator removal
3. AC power input box and 5411086-YA power line monitor board removal
4. Fan removal
5. Transformer assembly removal.

Power Supply Access Procedure

1. Power down the equipment.
2. Remove the ac power connection by disconnecting the line cord on the power supply from the 861 power control.
3. Fully extend the memory frame from the rack, ensuring that the cables do not bind (Figure 4-53).
4. Remove the memory frame's top cover by removing six screws.
5. Remove the cable clamps by removing four screws.
6. To remove the top cover of the power supply, loosen the top three screws and remove the back four screws.

Regulator Removal (Figure 4-58)

1. Perform the power supply access procedure just described.

CAUTION
Do not remove the power supply hinge screws when performing the next step.

2. Remove the two power screws on each side of the power supply (Figure 4-53).
3. Carefully rotate the memory frame 90 degrees and tilt the power supply (Figure 4-59).
4. Remove the bottom cover of the memory frame.

WARNING
Power must be removed prior to removing regulators.

5. Disconnect the Mate-N-Lok from the regulator to be removed.
6. Remove three screws, two on the top and one on the bottom of the regulator (Figures 4-58 and 4-60).
7. Rotate the memory frame 90 degrees to the horizontal position.
8. To remove the regulator, slide it out.
9. Install a new regulator as described in Paragraph 4.5.2.5.

CAUTION
Use correct length screws when installing a new regulator.

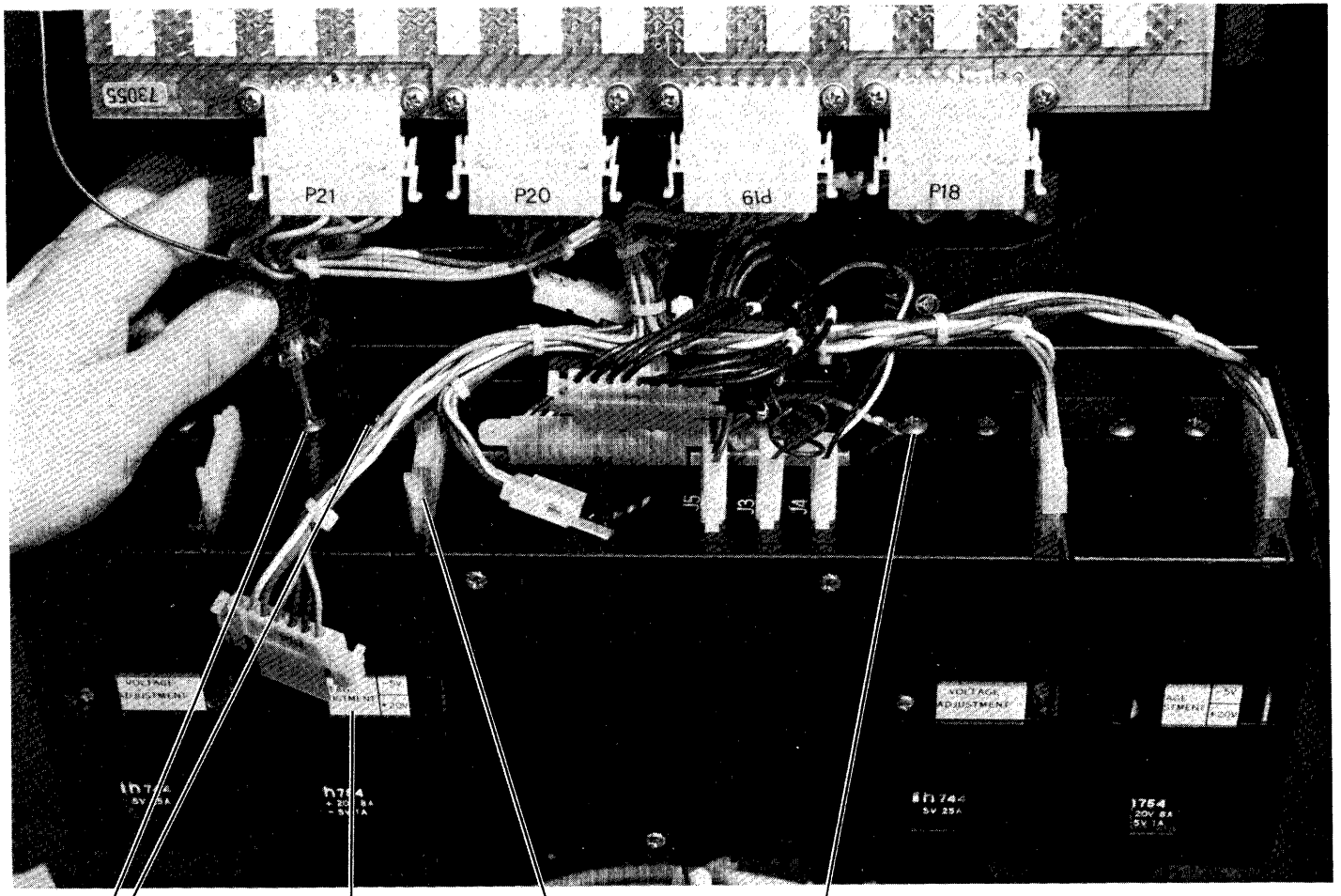


Figure 4-58 Regulator Removal

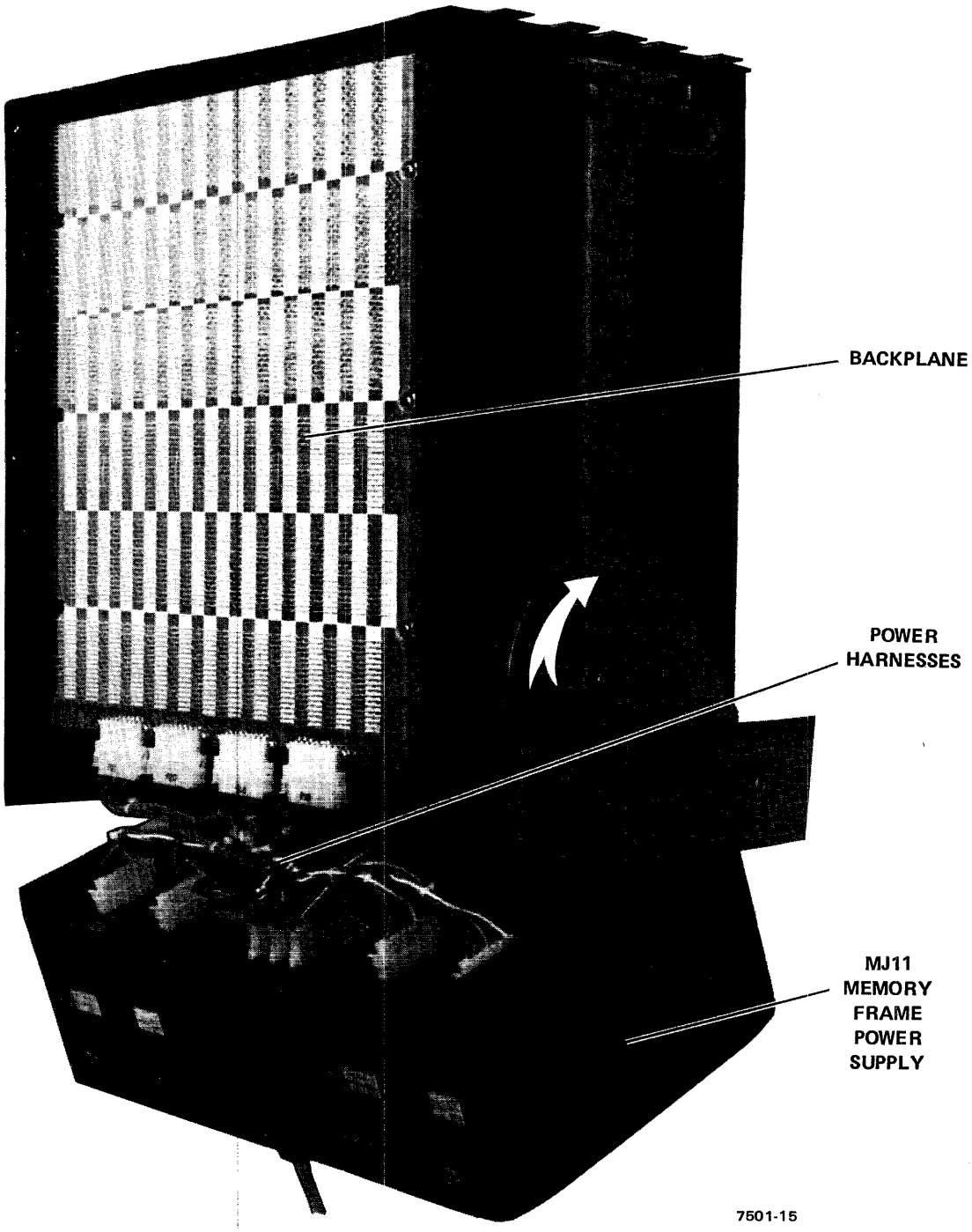


Figure 4-59 Power Supply in Maintenance Position

AC Input Box and 5411086-YA Power Line Monitor Board Removal

1. Perform the power supply access procedure just described.

CAUTION
Do not remove the power supply hinge screws when performing the next step.

2. Remove the two power system screws on each side of the power supply (Figure 4-53).

3. Carefully rotate the memory frame 90 degrees and tilt the power supply (Figure 4-59).

WARNING
Be sure that ac power is removed prior to removing the ac input box or 5411086-YA power line monitor board.

4. Disconnect all the Mate-N-Loks connected to the ac input box.

5. Disconnect the card edge connector from the 5411086-YA power line monitor board.

CAUTION
Hold the ac input box in place while performing the next step.

6. Remove three screws and slide out the ac input box (Figure 4-60).

7. Remove 5411086-YA power line monitor board from the ac input box.

Fan Removal

1. Perform the power supply access procedure just described.

NOTE
The memory frame should be in a horizontal position when removing fans.

WARNING
Ensure ac power is removed.

2. Remove all modules.

3. On the module side of the fan, remove the two screws holding the fan.

4. Slide the fan up and out of the power supply chassis and disconnect the jack (Figure 4-61) from the fan.

CAUTION
When installing the fan, do not tighten the screws beyond 10 in/lb. Tightening screws beyond 10 in/lb may cause the fan to bind.

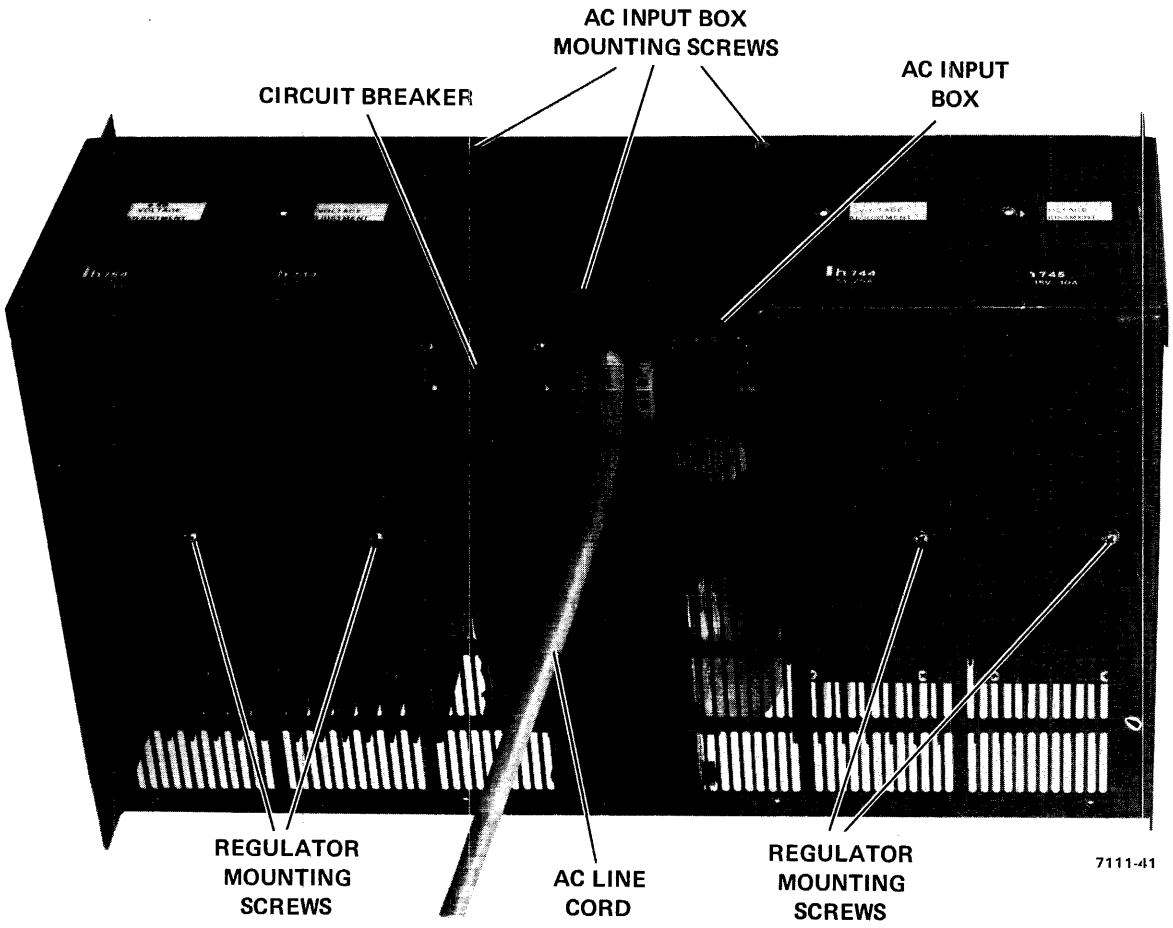


Figure 4-60 Memory Frame Power Supply

Transformer Assembly Removal

WARNING
Remove ac power before performing this procedure.

1. Remove all four regulators per previous directions.
2. Remove the ac input box. Refer to previous directions.
3. Remove both fans. Refer to previous directions.
4. Disconnect the transformer assembly's Mate-N-Loks.
5. Remove both screws from the transformer assembly's cable clamp (Figure 4-62, sheet 1).
6. Rotate the memory frame to the horizontal position.
7. Remove the transformer assembly's four mounting screws and nuts (Figure 4-62, sheet 2) and lift out the transformer assembly.

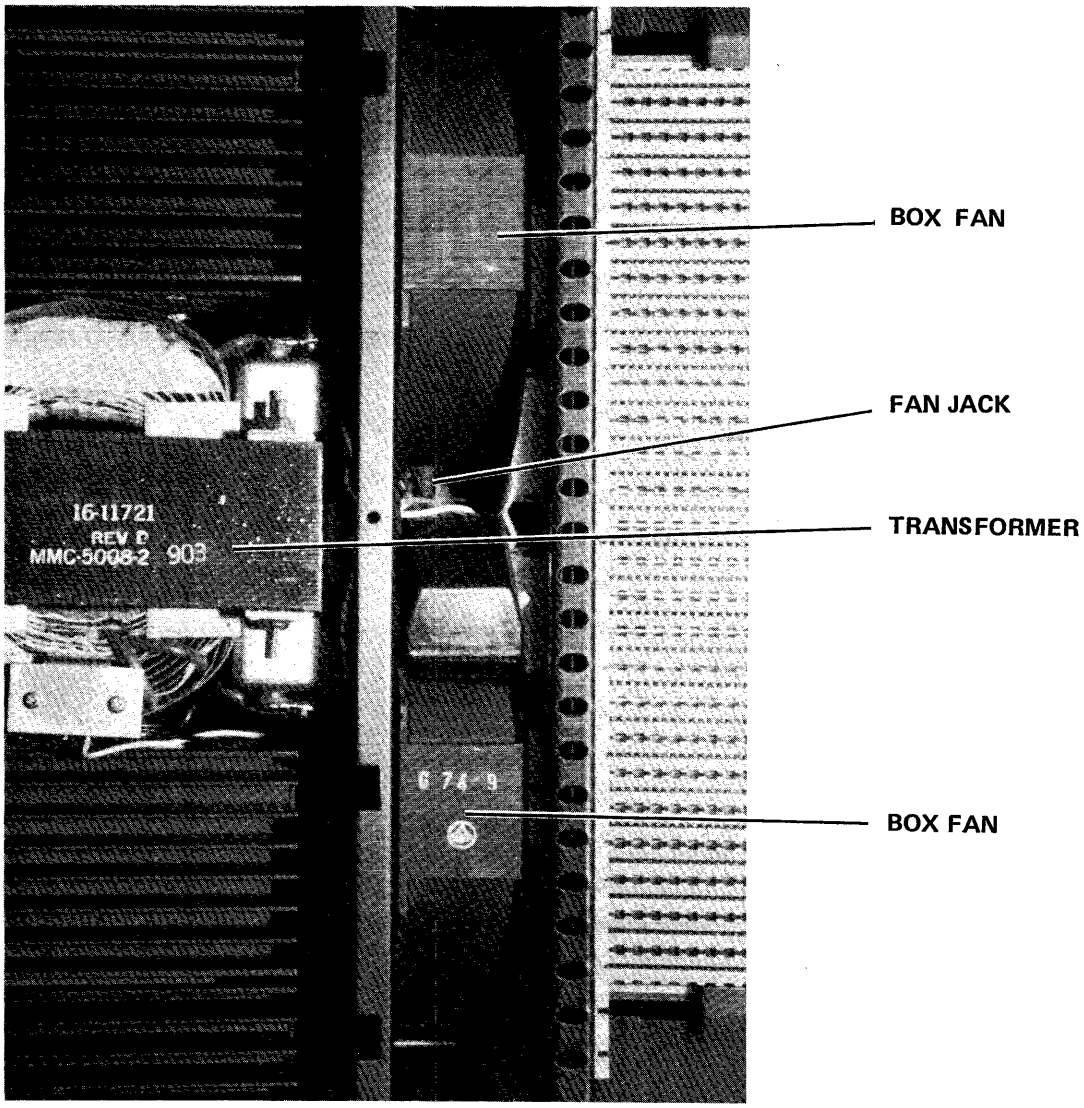


Figure 4-61 Fan Removal

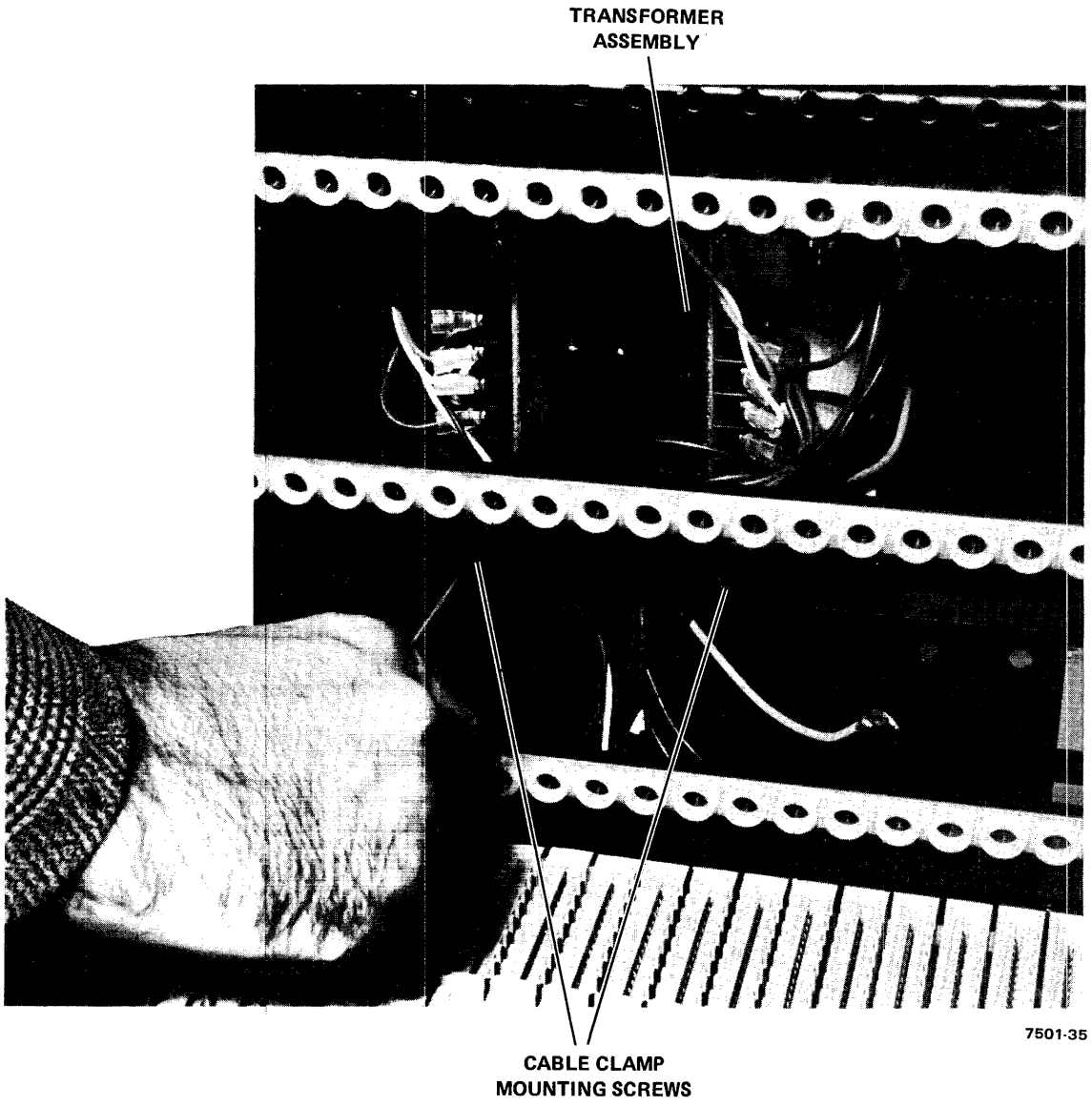


Figure 4-62 Transformer Assembly Removal (Sheet 1 of 2)

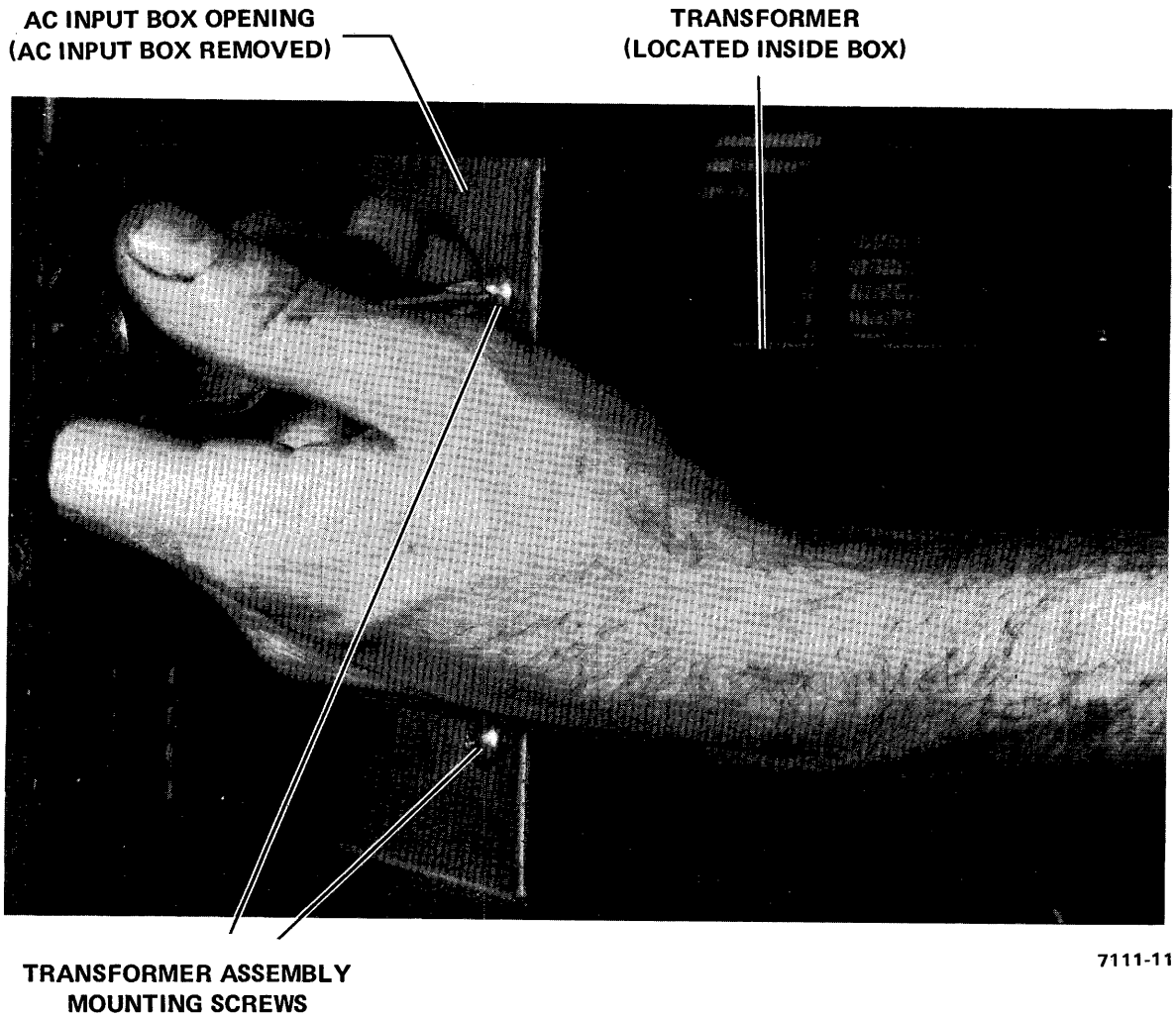


Figure 4-62 Transformer Assembly Removal (Sheet 2 of 2)

4.5.2.5 Regulator Installation Procedure – The following steps describe the procedure for installing the regulators.

1. Verify that power to the power supply is off.

2. Install the regulator. (Refer to Figures 4-58 and 4-60 for mounting screw locations.)

CAUTION
Use correct length screws when installing a new regulator.

3. Connect the regulator Mate-N-Lok to the installed regulator.

4. Turn on power to the regulator.

NOTE
If the regulator crowbars, turn power off and rotate the regulator voltage adjustment potentiometer fully counterclockwise (below crowbar voltage). Turn on power.

5. Using a DVM, measure the voltage(s) at the M8149 test point(s) (Paragraph 4.5.2) or at the backplane to ensure that the voltage(s) is(are) within limits specified in Table 4-19. Adjust voltage(s) if necessary (Paragraph 4.5.2.2).

6. Recheck the regulator voltage(s) at the backplane per Tables 4-17, 4-18, and 4-19. Adjust voltage(s) if necessary.

7. Turn off power and attach the bottom cover of the memory frame. Carefully rotate the memory frame to the horizontal position.

8. Install the two power system screws (Figure 4-53) and attach the top cover. Carefully push the frame back into the cabinet; be careful that the cables do not bind.

4.5.3 H7420 Power Supply

The following paragraphs describe the preventive and corrective maintenance procedures for the H7420 processor power supply.

4.5.3.1 Preventive Maintenance – The preventive maintenance philosophy for the MJ11 power supply, stated in Paragraph 4.5.2.1, is also applicable to the H7420, preventive maintenance (PM) of the H7420, consisting of periodic visual inspections and voltage measurements, help anticipate future equipment failures. The PDP-11/70 PM procedures, including those for the power system, are included in Appendix G; the listed PM schedule should be adhered to.

Monthly Field Service PM procedures (Appendix G) include visual inspection of the logic and power supply fans, cleaning the air filters, and replacing burned out indicators.

Quarterly PM procedures, also listed in Appendix G, include inspections and checks of the PDP-11/70 that are more comprehensive than the monthly procedures: a check of the wiring and etch conditions, cleaning the air vents and fan housings with a vacuum cleaner, and voltage checks of the regulators (Table 4-21).

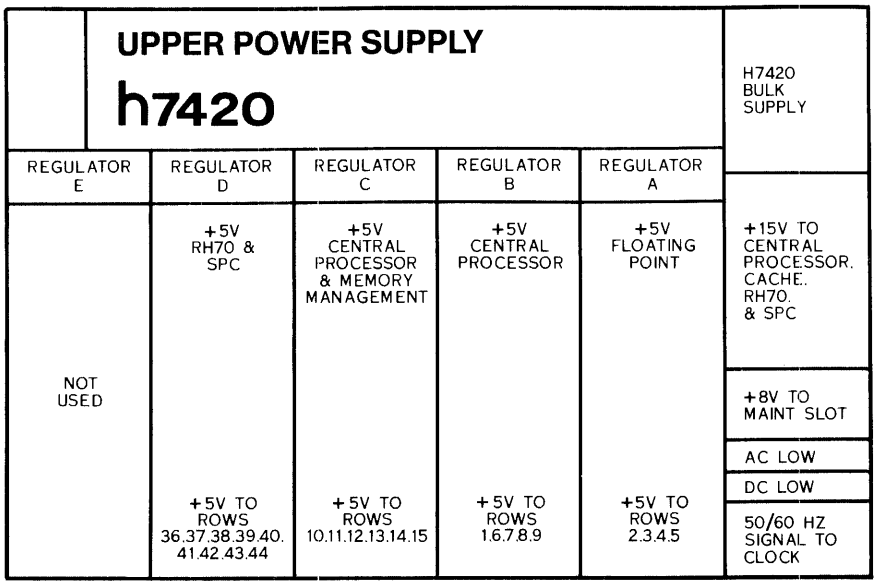
Figure 4-63 is a reproduction of the decals that are attached to the back of the processor box. The decals indicate where the +5 Vac from each regulator in the two H7420s is applied.

Table 4-21 H7420 Voltage Measurements

Output	Slots Supplied	Measure at CPU Backplane Pin	Voltage	Max Ripple Peak-to-Peak
H744 +5 V Regulator A	2-5	F02A2	+5 V	0.2 Vdc
H744 +5 V Regulator B	1, 6-9	F09A2	+5 V	0.2 Vdc
H744 +5 V Regulator C	10-15	F15A2	+5 V	0.2 Vdc
H744 +5 V Regulator D	36-44	F44A2	+5 V	0.2 Vdc
H744 +5 V Regulator H	20-22	F22A2	+5 V	0.2 Vdc
H744 +5 V Regulator J	16-18 and the console	F18A2	+5 V	0.2 Vdc
H744 +5 V Regulator K	24-28	F28A2	+5 V	0.2 Vdc
H744 +5 V Regulator L	29-35	F35A2	+5 V	0.2 Vdc
Upper H7420 5411086	1	B01B1	+8 V ± 1.2 Vdc	0.24 Vdc
Upper H7420 5411086	40-44	E13A1	+15 V ± 1.5 Vdc	0.45 Vdc
Lower H7420 5411086	2, 17, 25, 27, 29-31, 33-35 37-44	E13B2	-15 V ± 1.5 Vdc	0.45 Vdc

Measure and adjust (if necessary) the regulator voltages according to the instructions listed in Appendix G. (Refer to Paragraph 4.5.3.2 for adjustment procedures). Figure 4-64 shows the locations of the H744 voltage adjustment screws; the 5411086 voltage adjustment is identified in Figure 4-26. If a regulator cannot be adjusted to meet specifications, remove and replace the regulator (Paragraph 4.5.3.4 and 4.5.3.5).

A digital voltmeter (Weston Schlumberger DVM Model 4443 or Data Technology Model 21) should be used for making the regulator voltage measurements. A calibrated oscilloscope may be used if a DVM is not available. A VOM is useful for making continuity and resistance checks within the power supply. An oscilloscope is necessary for measuring ripple. (Ripple tolerances are listed in Table 4-21).



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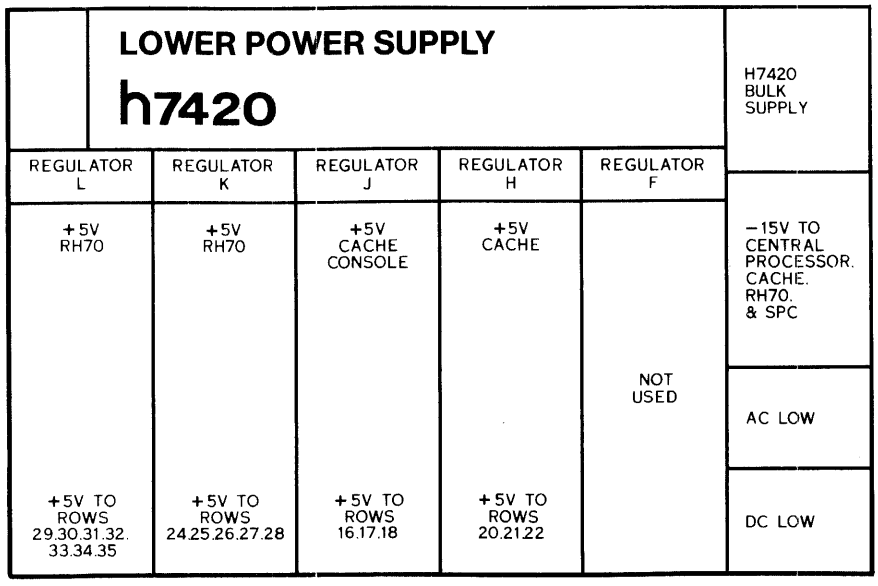

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Figure 4-63 H7420 Decals

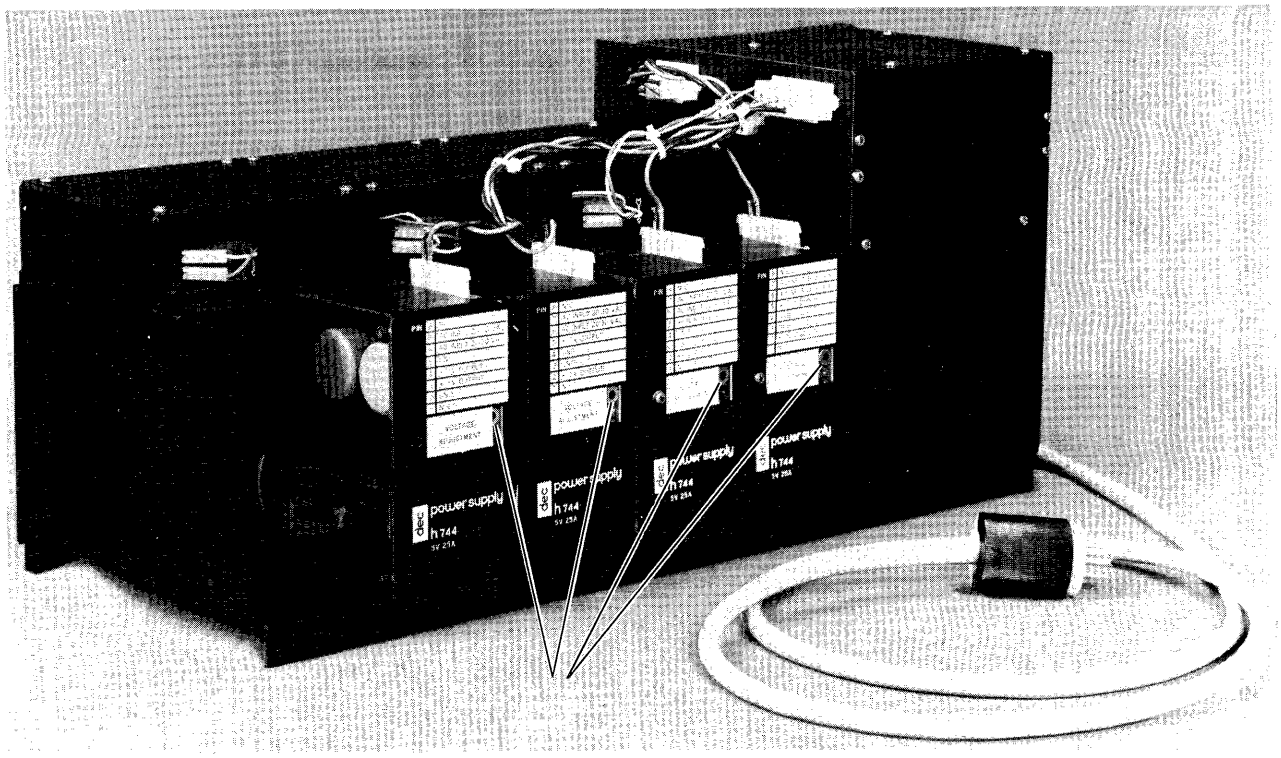

Figure 4-64 H744 Regulator Voltage Adjustment

Visual Inspection

CAUTION

Make sure all power is off before performing the following steps.

1. Check all fans to ensure that they are not obstructed in any way. Clean air filters mounted on the inside of t he cabinet door if required.

2. Visually inspect the modules and backplane for broken wires, connectors, or other obvious defects.

3. Inspect all wiring and cables for cuts, breaks, frays, deterioration, kinks, strain, and mechanical security. Repair or replace any defective wiring or cable covering.

4. Inspect the following for mechanical security: power supply regulators, fans, capacitors, etc. Tighten or replace as required.

5. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace as required.

4.5.3.2 H7420 Corrective Maintenance – Prior to making any adjustment, the H7420 power supply should be inspected to ensure that the equipment is energized.

1. Check that the processor cabinet 861 power control indicators light (Figure 4-46 and 4-47).

2. Check that all fans are energized.

3. Check that all regulator indicators light. The indicators are directly below the voltage adjustment screws (Figure 4-63) and are on during normal operation.

Voltage Regulator Adjustments – The H744 voltage regulator outputs (Table 4-17) must be adjusted to the tolerances indicated in Table 4-19. When performing the adjustments, ensure that the maximum voltages at the regulator are not exceeded. These voltages represent the maximum regulator voltage prior to crowbar. Figure 4-64 shows the location of the voltage regulator adjustment potentiometers.

Correct power system voltages at the backplane are critical to a properly operating system. If a voltage regulator cannot be adjusted to meet the required tolerance, check for a faulty regulator or harness.

The regulator replacement procedure is described in Paragraphs 4.5.3.4 and 4.5.3.5.

H744 Voltage Regulator Adjustment (+5 V)

1. Power down the equipment.

2. Fully extend the processor frame from the rack, ensuring that the cables do not bind.

3. Power up the equipment.

4. Using a digital voltmeter, or a calibrated oscilloscope, measure the +5 V outputs at the processor backplane (Table 4-21). Adjust these voltages to +5 Vac ± 250 mV. The adjustment screws are identified in Figure 4-64.

5. Power down the equipment.

6. Carefully push the processor frame back into the cabinet, observing that the cables do not bind.

4.5.3.3 H7420 Power Supply Fault Isolation – If a power system fault is suspected, visually inspect the system components for obvious fault indications. For example, each of the voltage regulator modules is provided with an output indicator lamp that lights when the output voltage is within range. If a single indicator lamp within the group (A-D or H-L) is not lit, the fault is probably within that voltage regulator module. This can be verified by swapping H744 modules. Once the fault has been isolated to a voltage regulator module, refer to the voltage regulator checkout procedure described in Paragraph 4.5.2.3. A decal (Figure 4-63) is placed on the rear of the processor rack chassis to indicate the location and function of each voltage regulator.

If none of the voltage regulator output indicator lamps in the group are lit, the fault is probably in the associated H7420 power supply or 861 power control. Visually inspect the power indicator lamps and circuit breakers provided with these devices to determine whether the fault can be isolated to either the H7420 or the power control. Figures 4-12, 4-24, 4-27, and 4-47 show where these indicator lamps and circuit breakers are located in each device. Figures 4-26 and 4-65 show the internal components of the H7420. A description of the 861 power control is given in Paragraph 4.3.5.

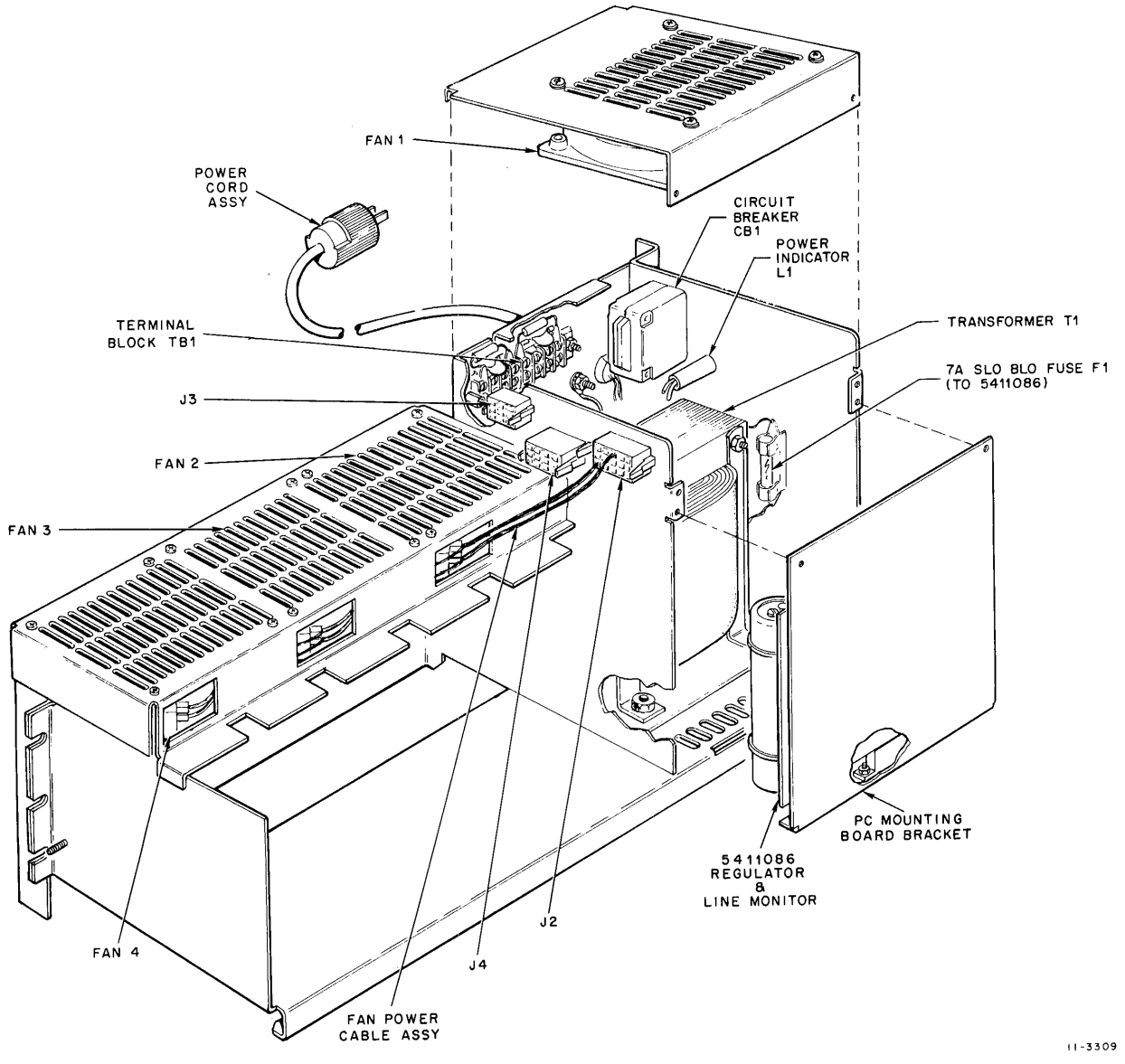

Figure 4-65 H7420 Power Supply Component Identification

The following steps can be used to aid in locating the cause of a power system failure:

1. Ensure that the H7420 is plugged in and getting primary power (115/230 Vac) from the 861 power control.

2. Check the power indicator and circuit breaker CB1 on the H7420 (Figure 4-27).

3. Check the individual regulator lights. (Regulator lights are lit during normal operation.)

4. Check the two LEDs on the 5411086 power line monitor (Figure 4-26). They should be on during normal operation, i.e., AC LO and DC LO are not asserted (Paragraph 4.4.6.1). The first two steps of the 5411086 removal procedure (Paragraph 4.5.3.4) must be performed in order to view the two indicators.

5. Measure regulator voltages at the processor backplane (Paragraph 4.5.3 and Table 4-21).

6. If all regulator outputs are within specifications, check the backplane for faulty wiring.

7. If one or more regulator outputs are incorrect, check the regulator fuse(s) (Figure 4-55), the transformer assembly, the power harness connections and the load.

8. If the +8 V, -15 V, or +15 V outputs are incorrect, check the 5411086 power line monitor. (Fuse locations are shown in Figure 4-26).

9. If the fault is isolated to a voltage regulator, refer to Paragraphs 4.5.2.3 and 4.5.3.2 for regulator troubleshooting and adjustment procedures. Table 4-20 lists several possible problem causes and their solution.

H744 regulator bench test procedures are described in Paragraph 4.5.2.3.

4.5.3.4 H7420 Power Supply Subassembly Removal Procedure - The power supply access procedure enables the supply to be accessed for adjustments and subassembly removal. The procedures listed below are described in the following paragraphs:

1. Power supply access procedure

2. H744 Regulator removal

3. 5411086 15 V regulator/power line monitor board removal

Power Supply Access Procedure

1. Power down the equipment.
2. Fully extend the processor frame from the rack, ensuring that the cables do not bind (Figure 4-17 and 4-18).

3. Remove the ac power connection by disconnecting the H7420 power cord (Figure 4-27) from the 861 power control.

CAUTION

Since both H7420s are connected to the same 861 (Figure 4-7), make certain that the correct H7420 power cord is disconnected.

H744 Regulator Removal

1. Perform the power supply access procedure just described.

WARNING
Power must be removed prior to removing regulators.

2. Disconnect the Mate-N-Lok connector from the regulator to be removed.

3. Remove the two screws and lockwashers that fasten the top of the regulator to the H7420 (Figure 4-66, sheet 1 of 2). Loosen, but do not remove, the knurled screw that fastens the bottom of the regulator to the H7420.

4. Slide the regulator out of the H7420 (Figure 4-66, sheet 2 of 2).

5. Install a new regulator as described in Paragraph 4.5.3.5.

5411086 15 V Regulator/Power Line Monitor Board Removal

1. Perform the power supply access procedures just described.

WARNING
Power must be removed prior to removing the 5410086 board.

2. Remove the two screws at the top of the PC mounting board bracket (Figure 4-67, sheet 1 of 3). The bracket then swings down from the top and remains suspended from the bottom edge.

3. Remove the two hex nuts from the end of the 5411086 board (Figure 4-67, sheet 2 of 3). Do not lose the attached hardware (screws, washers, and spacers).

4. Remove the 5411086 board from the PC mounting board bracket. This is accomplished by carefully pulling the board to separate the edge connector on the board from J1 (Figure 4-67, sheet 3 of 3).

5. Install a new 5411086 board as described in Paragraph 4.5.3.5.

4.5.3.5 H7420 Power Supply Subassembly Installation Procedure

H744 Regulator Installation –The following steps describe the procedure for installing H744 regulators in the H7420.

1. Perform the power supply access procedure (Paragraph 4.5.3.4).

WARNING
Power must be removed prior to installing regulators.

2. Place the H744 regulator in the correct position in the H7420. Tighten the knurled screw on the bottom of the H7420.

3. Fasten the top of the H744 to the H7420 with two screws and lock washers.

4. Connect the Mate-N-Lok connector (in the power harness) for this regulator position to the connector on the top of the regulator.

5. Turn on power and measure the regulator voltage at the processor backplane (Paragraph 4.5.3.1). Adjust the voltage (Paragraph 4.5.3.2) if the measured voltage is not within the tolerances listed in Table 4-19.

5411086 15 V Regulator/Power Line Monitor Board

1. Perform the power supply access and 5411086 removal procedures (Paragraph 4.5.3.4).

WARNING
Power must be removed prior to installing the 5411086 board.

2. Connect the edge connector on the 5411086 to J1 (Figure 4-67).

3. Fasten the opposite end of the board to the PC mounting board bracket with the necessary hardware (screws, washers, spacers, and hex nuts).

4. Attach the top of the PC mounting board to the H7420 chassis with two screws and washers.

5. Turn on power and check the backplane voltages (upper H7420: +15 V and +8 V; lower H7420: -15 V). Refer to Paragraphs 4.5.3.1 and 4.5.3.2 for 5411086 voltage check and adjustment procedures.

6. Power down the equipment.

7. Carefully push the processor frame into the cabinet, observing that the cables do not bind.

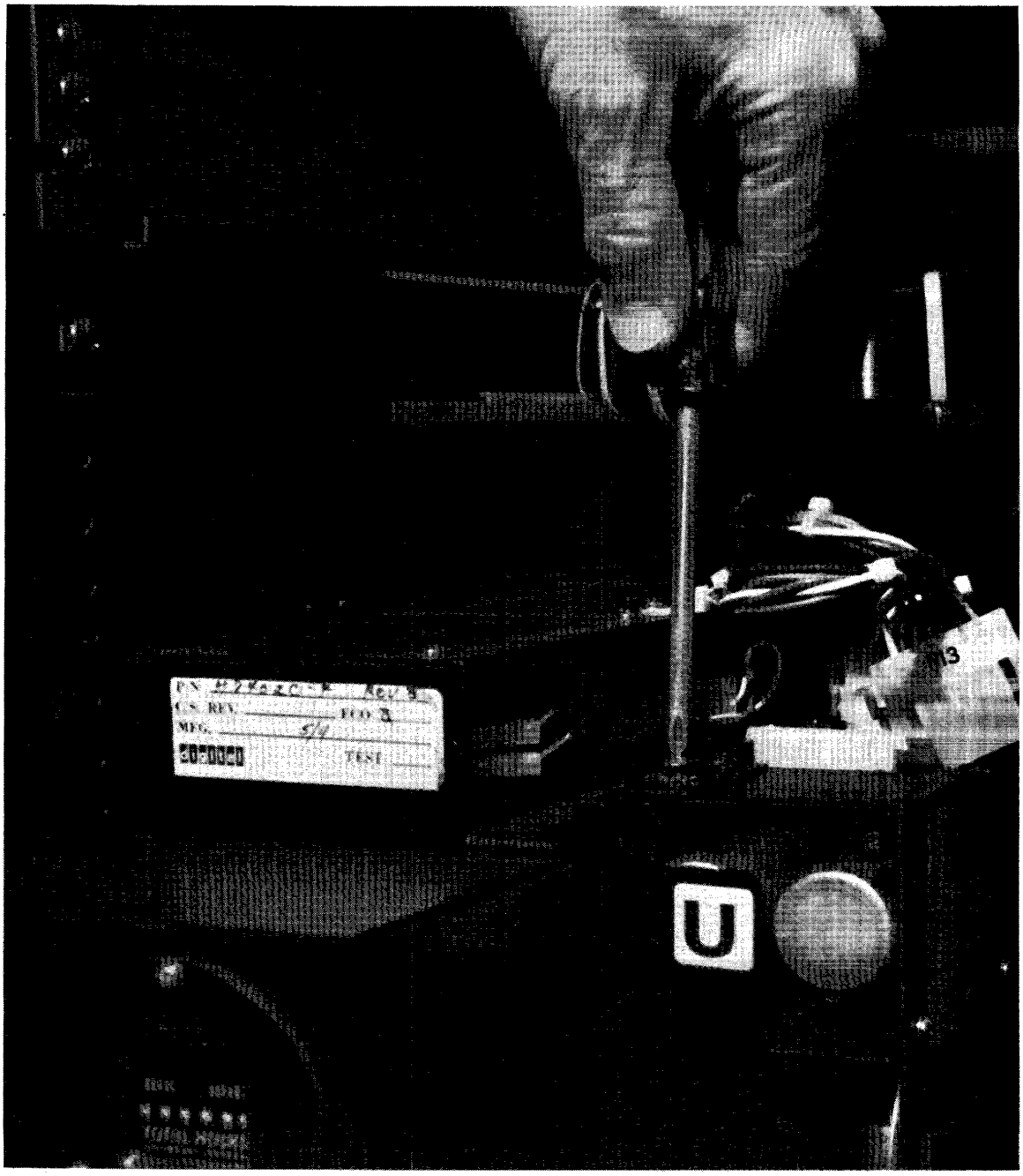

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Figure 4-66 H7420 Regulator Removal (Sheet 1 of 2)

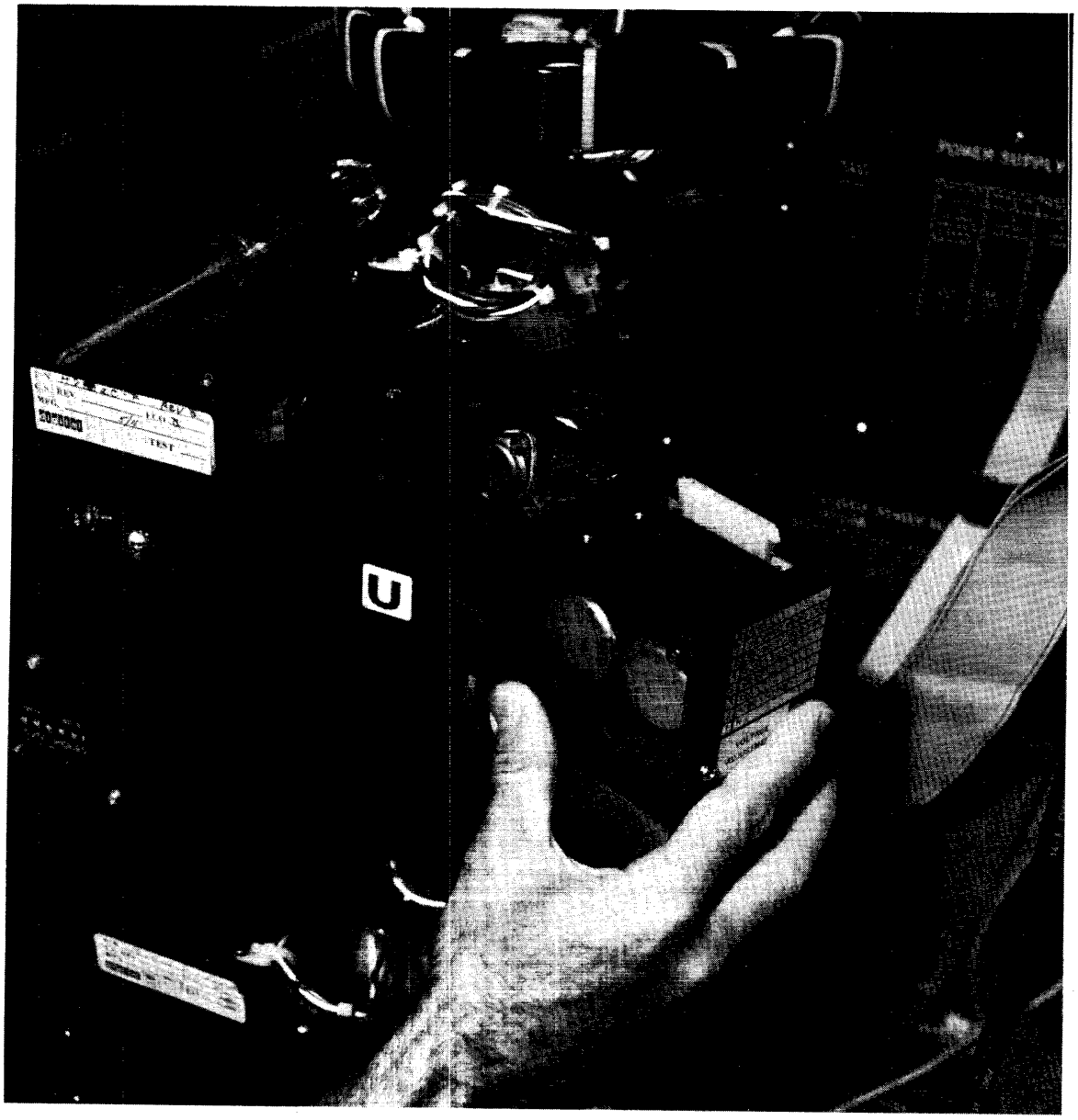

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Figure 4-66 H7420 Regulator Removal (Sheet 2 of 2)

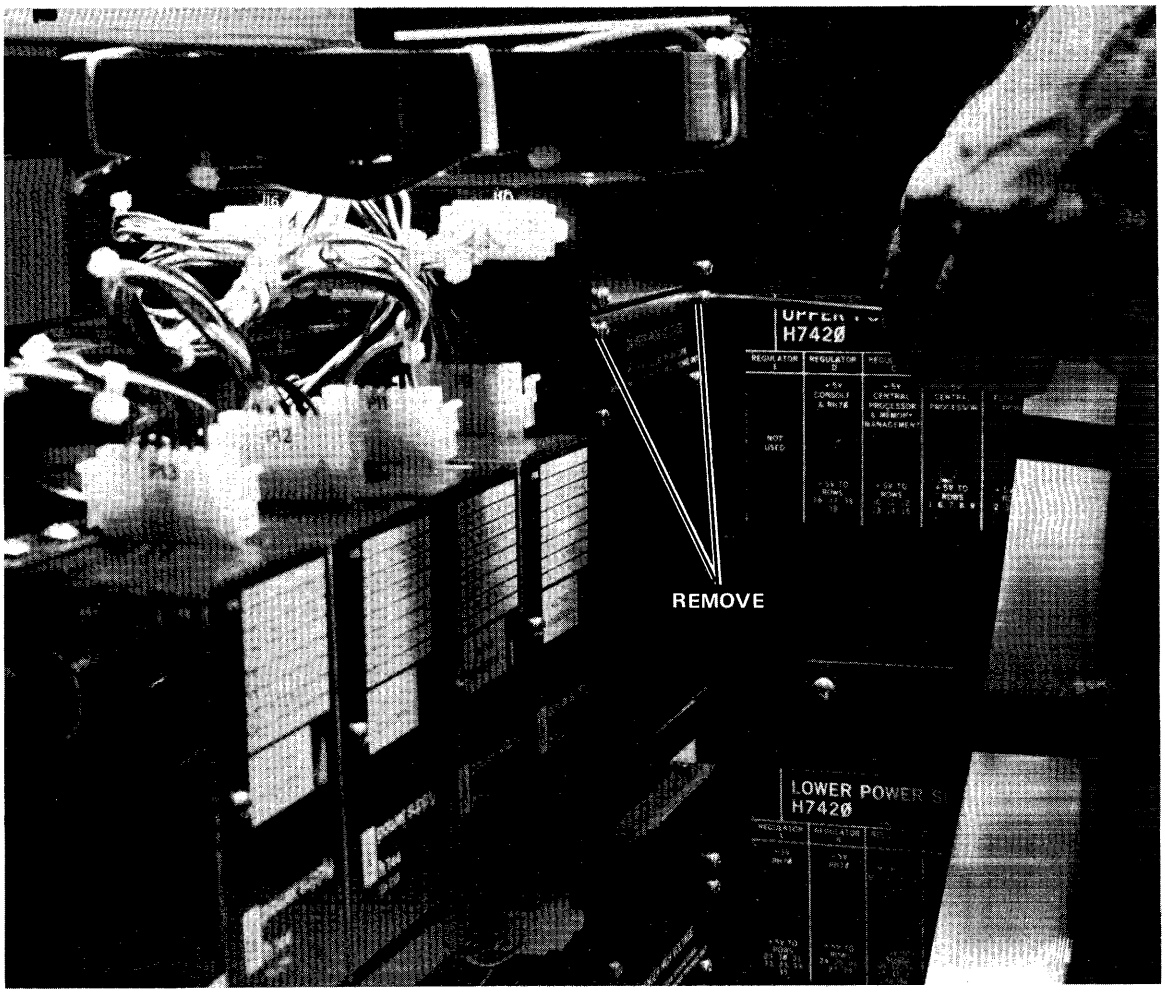

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Figure 4-67 5411086 Removal (H7420) (Sheet 1 of 3)

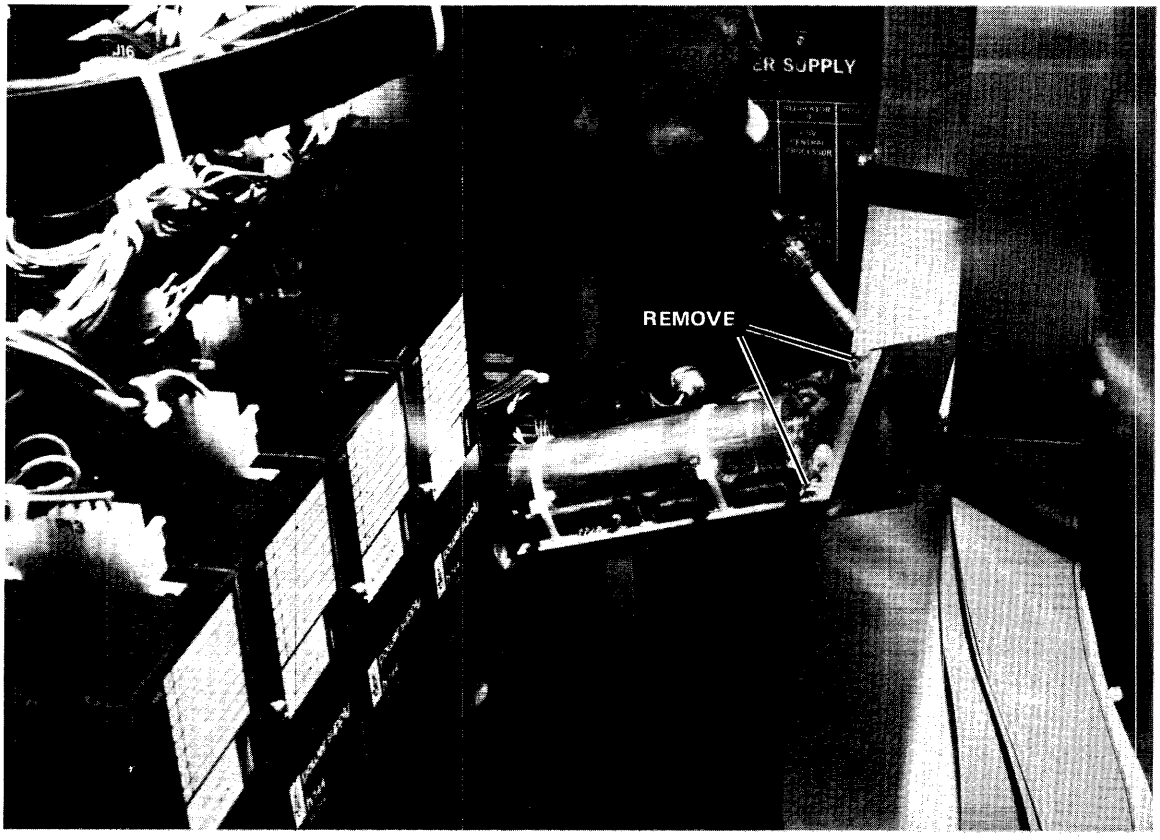

Figure 4-67 5411086 Removal (H7420) (Sheet 2 of 3)

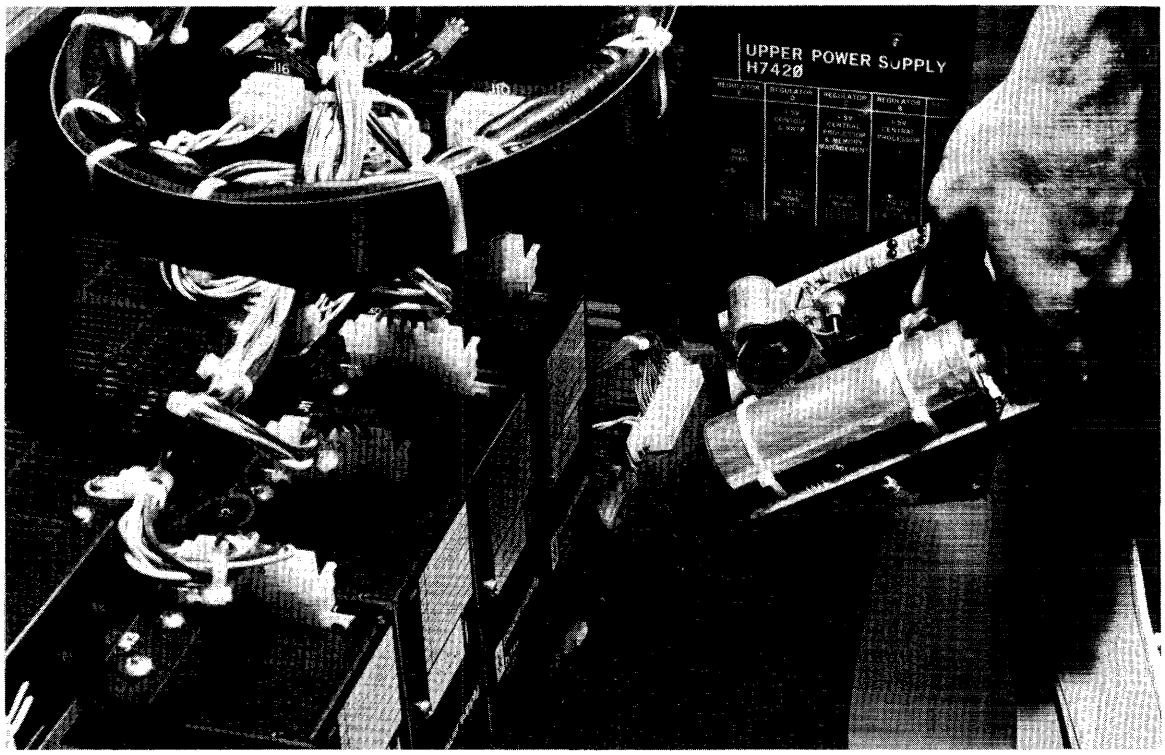

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Figure 4-67 5411086 Removal (H7420) (Sheet 3 of 3)

CHAPTER 5
MAINTENANCE

By use of on-line diagnostics, DEC/X11 or the PDP-11/70 subsystem diagnostic, system faults can be isolated to the appropriate subsystem; i.e., CPU, cache, memory management, Unibus map, Unibus device, main memory, Massbus controller or Massbus device.

Once the failing subsystem has been identified, the individual stand-alone diagnostic is used to locate the failing module. Once the bad module has been identified, it should be replaced and returned to the Maynard or European Depots for repair. Due to the complexity of the modules and the size (cost) of the PDP-11/70 systems in general, on-site component level repair of modules is discouraged. Component level repair should only be used as a back-up strategy or whenever the fault is obvious and can be repaired quickly.

Cold start maintenance (being unable to load diagnostics) is made easier by a hardware diagnostic routine included in the system bootstrap loader (standard on all machines). This loader, the M9301-YC, YH or M9312, contains 512 words, of which 256 words are used for diagnostic routines. The listing of the program stored in the M9301-YC (DEKBH), M9301-YH and M9312 are supplied at the end of this chapter (Paragraph 5.4.11); they contain detailed documentation to aid in troubleshooting a defective machine.

Basically the routines check the instructions used by the loader for loading programs and the first 28K of memory (basic address test). It also does a basic check of memory management and a basic check of the Unibus map. There are no routines in the diagnostic boot for checking the loading device. A paper tape diagnostic is supplied for this purpose. In addition to the bootstrap diagnostic, cold start maintenance is aided by the ability to eliminate the cache partially by forcing misses in half or all of the cache as well as forcing selection (upon word replacement) to a specific group.

System maintenance on the PDP-11/70 is enhanced by various registers and indicators (Paragraphs 5.3.1 and 5.3.2) within the CPU (Paragraph 5.3.1.1) and Massbus controllers as well as a "maintenance mode" of operation within each Massbus controller to allow complete checking of the RH70 data buffer. System problems are also aided by various bits within the parity registers (outline following) which enable one to find out easily where parity errors actually occurred, i.e., Unibus operations, CPU abort, memory bus timeouts, etc.

Memory system maintainability is improved because of the extensive use of parity throughout the memory system. Memory system failures are easily isolated because of six error registers which retain information on where the error occurred in addition to providing means of verifying the parity checkers and margining main memory.

The error registers are as follows:

1. Lo Error Address Register – Provides lower 16 bits of the 22-bit address where the parity error occurred.

2. Hi Error Address Register – Provides upper 6 bits of the 22-bit address as well as the cycle type which was being done, i.e., DATI, DATO, etc.

3. Error Register – Tells where the error actually occurred, i.e., lower word main memory, main memory bus, etc.

4. Control Register – Allows for the disabling of parity traps, forcing of cycles to bypass the cache or go to a specific group within the cache, etc.

5. Maintenance Register – Allows for margining of main memory currents and strobe, as well as forcing wrong parity checks.

6. Hit/Miss Register – This register tracks each processor cycle whether it was a hit (word present in cache memory) or a miss (word had to be obtained from slow memory).

Error indicators are easily checked by opening the memory cabinet front door. Indicators are present for incorrectly configured memory systems, memory address parity errors, and hung memory controllers.

The basic tools required for maintenance and repair of the PDP-11/70 system are listed in Table 5-1.

This chapter describes the maintenance aids available to Field Service personnel for diagnosis and repair of a defective system:

1. Guidelines for PDP-11/70 troubleshooting (Paragraph 5.1)

2. Basic checkout of a dead machine (Paragraph 5.2).

3. Troubleshooting aids (Paragraph 5.3), which include the system registers, indicators switches, and the maintenance module

4. A description of the PDP-11/70 diagnostic (Paragraph 5.4).

Table 5-1 Maintenance Equipment Required

Equipment or Tool	Manufacturer	Model, Type or Part No.	DEC Part No
Oscilloscope	Tektronix	453*	
Digital Voltmeter (DVM)	Weston (or the like)	6000	
Volt/Ohmmeter (VOM)	Triplett		29-13510
Unwrapping Tool	Gardner-Denver (DEC Catalog #H812A)	505 244-475	29-18387
Hand Wrap Tool	Gardner-Denver (DEC Catalog #H811A)	A-20557-29	29-18301
Diagonal Cutters	Utica	47-4	29-13460
Diagonal Cutters	Utica	466-4 (modified)	29-19551
Miniature Needle Nose Pliers	Utica	23-4-1/2	29-13462
Wire Strippers	Millers	101S	29-13467
Solder Extractor	Solder Pullit	Standard	29-13451
Soldering Iron (30W)	Paragon	615	29-13452
Soldering Iron Tip	Paragon	605	29-19333
16-Pin IC Clip	AP Incorporated	AP923700	29-10246
24-Pin IC Clip	AP Incorporated	AP923714	29-19556
Maintenance Cards	DEC		W131,W133**
Maintenance Card Overlay	DEC		5509974-0-1
Module Extender Boards (3)	DEC		W900

* Tektronix type 453 oscilloscope is adequate for most test procedures: type 454, or equivalent, may be required for some measurements.

** W133 is a dual version of W130. It provides the drivers for two W131 maintenance cards.

5.1 SYSTEM TROUBLESHOOTING

This paragraph describes typical procedures used when attempting to isolate a failure in a PDP-11/70 system. It is not intended as a method to be used for all types of failures, but rather as a guideline.

Refer to Figure 5-1: This flowchart points to the available maintenance aids, and thus may be used as a guide for troubleshooting a defective PDP-11/70.

5.1.1 Dead Machine

This is cold start troubleshooting. Refer to Paragraph 5.2.

5.1.2 System Repair

If the console functions work, attempt to bootstrap the XXDP monitor. If the bootstrap is successful, run the subsystem diagnostic. This program analyzes errors and points to the area of the system that is causing the primary trouble. Run the appropriate PDP-11/70 diagnostic, repair, and run the subsystem diagnostic again. If no errors are indicated, run DEC/X11 configured for the whole system, then the appropriate software exerciser. If no errors (within the limits set in the *PDP-11 Family Installation and Acceptance Procedure*) occur, the system should be good. If errors occur at any point in this series of tests, repair before proceeding.

If the bootstrap does not work (no message from XXDP), one of several conditions may occur:

1. The bootstrap halts at a location within its diagnostic. Refer to the diagnostic listing (Paragraph 5.12) to locate the defective instruction and repair. Use of the maintenance module and the KB11-B flowcharts may be indicated at this time.

2. The machine goes into a loop. Press the HALT switch and examine the PC. Also examine the PC if an unscheduled halt occurs and no parity error is indicated. If the PC contains a meaningless address, load all vector addresses with their own address plus 2, and the vector plus 2 with 0. Bootstrap again. The halt will then occur in the vector area, at address vector plus 4. Examination of the appropriate registers should then enable the field service engineer to start troubleshooting the appropriate area of the system. Examination of the various troubleshooting aids (indicators and test points) may save time at this point. The vectors that may be loaded are the following plus the vectors used by the Unibus devices installed on the system:

   004 CPU errors
   010 Illegal and reserved instructions
   014 BPT, breakpoint trap
   020 IOT, input/output trap
   024 Power Fail
   030 EMT, emulator trap
   034 TRAP instruction
   240 PIRQ, Program Interrupt Request
   244 Floating Point Error
   250 Memory Management

   Refer to Paragraph 5.3 for a description of the PDP-11/70 registers, and troubleshooting aids.

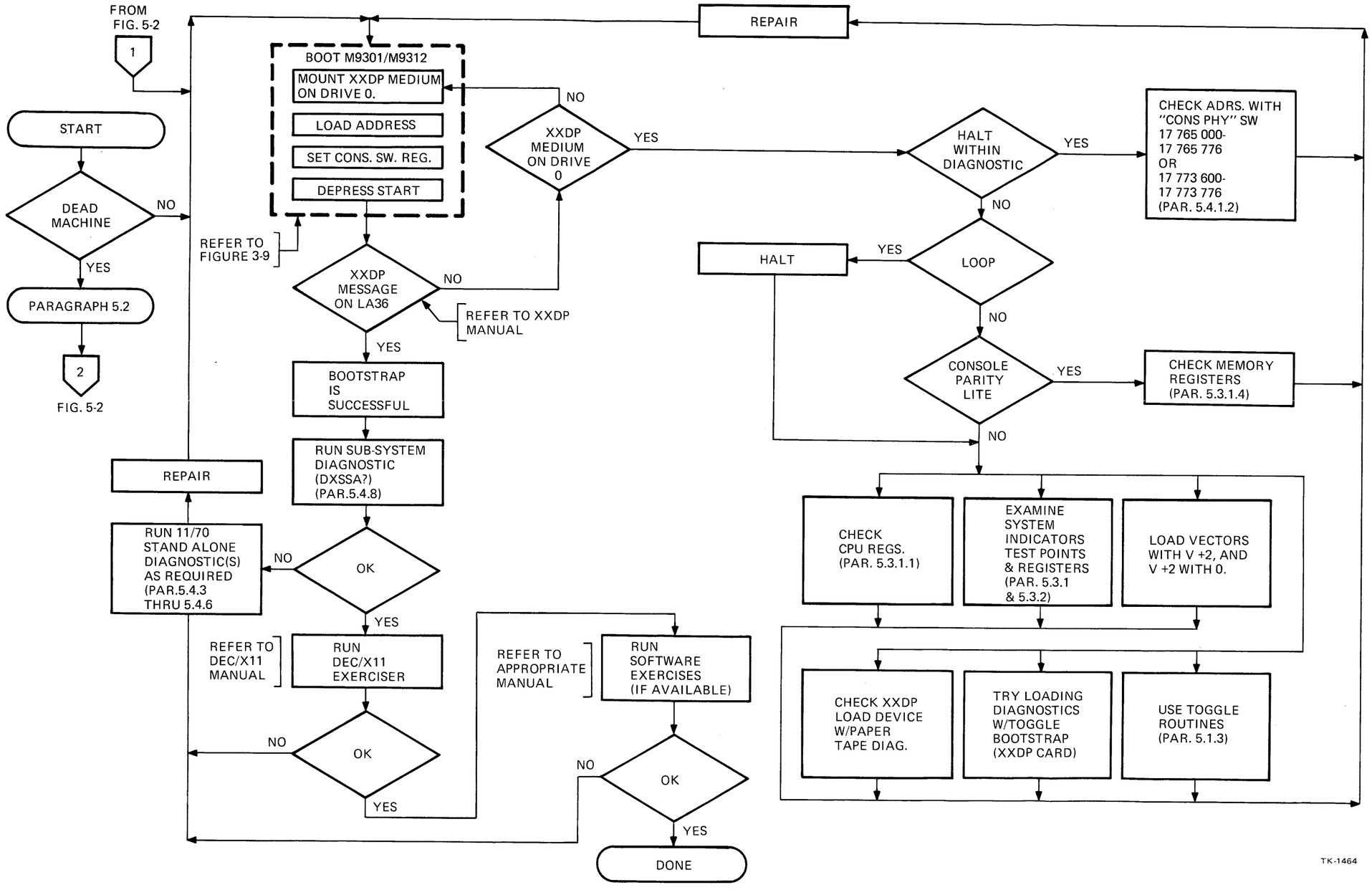


Figure 5-1 Guidelines for PDP-11/70 Troubleshooting

3. The machine halts with the Parity Console Indicator ON. Examine the Cache Error register and the other Cache registers (Paragraph 5.3.1.4).

4. If the memory system is not working at all, the toggle-in routines, which use the PARS instead of memory, may help (Paragraph 5.1.3).

5. It is of course possible that the ROM in the M9301 or M9312 is defective. This may be checked by examining the suspected locations from the console, if no spare M9301 or M9312 is available. Listings of the ROM programs on the M9301-YC (DEKBH) M9301-YH and M9312 are reproduced in Paragraph 5.4.11. Operating procedures for the M9301 and M9312 are given in Paragraph 3.4.2.

6. The XXDP-DEC/X11 program card lists toggle-in loaders for all XXDP media; this method of booting diagnostics may also be tried.

7. If a defective load medium device is suspected, and it is not convenient to change devices (it must be drive 0), a paper tape diagnostic is supplied to check this device. If no paper tape device is available at the site, a PMK01 should be used.

5.1.3 Toggle-in Routines

A few ideas that should aid in debugging failures in the cache memory of the PDP-11/70 are presented here. Many failures in this unit prohibit the normal troubleshooting technique of using standard diagnostics to isolate problems. This is because the cache in the PDP-11/70 is very much a part of the system hard core. Even a minor failure in this area could mean that the diagnostics could not be run because main memory may not be accessible from the processor. For these situations, the use of an alternate storage for short toggle-in routines is suggested: the memory management PARs.

The troubleshooter of course should attempt to run the standard PDP-11/70 diagnostics before attempting to use the methods that are outlined here. If these will not load or run properly, then the user should try to load and run them with the cache disabled, that is: forcing misses to both cache groups by depositing 14 (8) in the Cache Control register, 17 777 746.

NOTE

The Cache Control register is cleared by a console START as well as by a power-up. Therefore, it is necessary to use the CONTINUE switch instead of the START switch when using this procedure.

In this way two of the four modules in the cache memory unit can be turned off effectively. These are the cache address memory board, M8143, and the cache data memory board, M8144. There is no way to disable the logic on the other two boards, the cache control board (M8142), or the cache data paths board (M8145).

The memory management PARs are 16-bit registers which can, with a little programming skill, be used easily to store short routines to check much of the logic anywhere in the PDP-11/70 system. Suggestions will be given here for toggling in cache tests.

Before toggling in a routine, the troubleshooter should try to isolate the problem first to either the address paths and control or the data paths and control. This can usually be done using the console. For example, a good way to check out most of the address paths is to examine the Cache Error Address register (17 777 740 and 17 777 742). This register is toggled every time a cycle is executed. It thus contains the address being referenced anytime a reference is made: When the register itself is examined twice, it should contain its own address on the second EXAMINE. This is an easy way to ensure that the address multiplexer on the ADM (M8143) board can pass ones and that the address paths themselves can go to one. Another good way to isolate a problem to a subcomponent is to use the Cache Error register, which should indicate the source of any parity error. If the Error register indicates an address memory error, an address test should be run, etc.

If the troublshooter cannot isolate the failure from the console, he/she can pick routines that he/she thinks most general (or use one that was written by oneself).

As a simple example, consider the case in which it has been discovered that writing and reading data from a particular cache group (say group zero) will result in a parity error. Toggling the following routine into the KIPARs should be a great help in isolating the problem with or without the use of an oscilloscope:

```
Address     Data          Mnemonic
17772340    012737        MOV     #1$,@#114
17772342    172350
17772344    000114
17772346    005003        CLR     R3
17772350    012706  1$:   MOV     #500,SP
17772352    000500
17772354    005203        INC     R3
17772356    010337        MOV     R3,@#SWR
17772360    177570
17772362    013701  2$:   MOV     @#SWR,R1
17772364    177570
17772366    010110        MOV     R1,(R0)
17772370    021001        CMP     (R0),R1
17772372    001366        BNE     1$
17772374    000772        BR      2$
```

This routine will move the value constantly in the low order 16 Console Switch register switches to the address in R0. It will then compare what is in that location with what was written. If either this comparison fails or a parity error occurs, the contents of R3, which is displayed in the data lights of the display register, will be incremented. In this way the user can monitor the failure rate of a particular pattern, or try different patterns by changing the switches without stopping the program. Note that the parity traps (if any occur) will be dealt with properly.

As a more general approach which may be useful, the following program is provided. It has no parity check which eliminates machine halt on a parity error and thus may aid in troubleshooting. This program will write any pattern throughout memory from 0 to the system size register. It executes from the supervisor I and D space address registers. Deposit the pattern that you wish to use in R5. If you wish to clear memory, deposit 0 in R5.

```
17772300        077406
17772316        077406
17772340        000000
17772356        177600
17777700        000000
17777701        172340
17777702        177572
17777703        177760
17777704        172516
17777705        (PATTERN)

17772240        012714          MOV #20,(R4)
17772242        000020
17772244        005212          INC (R2)
17772246        010520  1$:     MOV R5,(R0)+
17772250        020027          CMP R0,#17776
17772252        017776
17772254        003774          BLE 1$
17772256        062711          ADD #200,(R1)
17772260        000200
17772262        021311          CMP (R3),(R1)
17772264        003402          BLE 2$
17772266        005000          CLR R0
17772270        000766          BR 1$
17772272        005312  2$:     DEC (R2)
17772274        000000          HALT
```

These were only examples. The routines presented are by no means general enough to catch any failure.

If the troubleshooter has determined the address paths to be the source of a problem which results in a parity error (or perhaps some addresses cannot be made hits) the following routine could be used:

```
17772340        012737          MOV     #1$,@#114
17772342        172350
17772344        000114
17772346        005003          CLR     R3
17772350        012706  1$:     MOV     #500,SP
17772352        000500
17772354        005203          INC     R3
17772356        010337          MOV     R3,@#SWR
17772360        177570
17772362        013700  2$:     MOV     @#SWR,R0
17772364        177570
17772366        021010          CMP     (R0),(R0)
17772370        006037          ROR     @#HITMISREG
17772372        177752
17772374        103365          BCC     1$
17772376        000771          BR      2$
```

In this test, whatever address is in the Switch register (bits 15 through 0) is referenced and a check is made to see if that address can be made a hit. If that address was not a hit when it should have been, or if a parity error occurred, then the contents or R3 will be incremented and shown in the Display Register Data Indicators.

Note that this and the preceding routine continually loop and use the contents of the Switch register to make the test. The Switch register can be changed at any time while the program is running and any errors are displayed by incrementing the Display register. In spite of the fact that both routines are too specific to be used in finding a general or completely unknown problem, they are good examples of what is desirable in a usable toggle in routine.

If the troubleshooter has discovered how to aggravate a particular failure, he should not be afraid to write and toggle in a short simple routine to help isolate it. Sometimes a simple:

```
1$:     TST   (R0)
        BR    1$
```

will be of considerable aid when used in conjunction with an oscilloscope, if it is put in the PARs.

Some very general more sophisticated toggle in routines follow. These may be helpful when the source of a failure is not clear.

Test 1 Data Memory Count Pattern Test

This test runs a count pattern through each cache memory data word. If one of the patterns is not stored correctly, a parity error will occur and the halt at 116 will be executed. When HALT is executed, the contents of R0, the address, will be displayed in the Data Paths Display lights. R1 will contain the last data pattern read from that location. If the routine is unable to make the address a hit, then the halt at 17 772 364 will be executed. If a parity error occurs, then the troubleshooter should examine the contents of the Cache Error registers. Note that this routine should be run twice, once for each group. It should be run first in group zero by forcing misses to group one and forcing selection of group zero (put 30 in the Cache Control register, 17 777 746), then in group one by forcing misses to group zero and selection of group one (by putting 44 in the Cache Control register, 17 777 746).

NOTE

The Cache Control register is cleared by a console START as well as by a power-up. Therefore, it is necessary to use the CONTINUE switch instead of the START switch when using this procedure.

The test will run continuously if no errors occur. It can be made to run just one pass by replacing the last instruction with a halt (000000 at 17 772 376).

```
SP              000500
00000114        000116
00000116        00000
17772340        012700  1$:     MOV     #4000.R0
17772342        004000
17772344        012702          MOV     #1000,R2
17772346        001000
17772350        044010  2$:     BIC     -(R0),(R0)
17772352        005310  3$:     DEC     (R0)
17772354        011001          MOV     (R0),R1
17772356        006037          ROR     @#HITMISREG
17772360        177752
17772362        103401          BCS     4$
17772364        000000          HALT
17772366        005110  4$:     COM     (R0)
17772370        005110          COM     (R0)
17772372        001367          BNE     3$
17772374        077212          SOB     R2,2$
17772376        000760          BR      1$
```

Test 2 Address Memory Count Pattern Test (Bits A10 Through A15 Test)

This test tries to make every address in the first 28K (addresses 0 through 00 157 776) a hit. It should be run twice (once in each group) as was outlined in Test 1. If a parity error occurs, the HALT at 116 is executed and the user should look at the Cache Error registers to see what happened. When the routine fails to make a particular address a hit, the halt at location 17 772 360 will be executed. If either of these halts is executed, R0 (the address being tested) will be displayed in the Display Register Indicators.

```
SP                  000500
00000114            000116
00000116            000000
17772340            005000  1$      CRL     R0
17772342            012701          MOV     #70000,R1
17772344            070000
17772346            005710  2$:     TST     (R0)
17772350            005720          TST     (R0)+
17772352            006037          ROR     @#HITMISREG
17772354            177752
17772356            103401          BCS     3$
17772360            000000          HALT
17772362            077107  3$:     SOB     R1,2$
17772364            000765          BR      1$
```

Test 3 Main Memory Dual Addressing Test 0 to 28K

This test runs a dual addressing test through the first 28K of main memory. It writes the address of each location into each location. Then it returns to check that each location contains its own address. If the halt at location 17 772 370 is executed, then the test has failed. The address that contained the bad data is in R0 (which is displayed in the data lights of the Display register). The user should then examine that location to see what the bad data is. This test should be run while forcing misses to both groups by first depositing 14 into the Cache Control register at 17 777 746.

```
SP                  000500
00000114            000116
00000116            000000          HALT
17772340            012700  1$:     MOV     #500,R0
17772342            000500
17772344            012701          MOV     #67540,R1
17772346            067540
17772350            010020  2$:     MOV     R0,(R0)+
17772352            077102          SOB     R1,2$
17772354            012700          MOV     #500,R0
17772356            000500
17772360            012701          MOV     #67540,R1
17772362            067540
17772364            020010  3$:     CMP     R0,(R0)
17772366            001401          BEQ     4$
17772370            000000          HALT
17772372            005120  4$:     COM     (R0)+
17772374            077105          SOB     R1,3$
17772376            000760          BR      1$
```

Test 4 Data Memory Dual Addressing Test

This routine performs a dual addressing test on the cache data memory. Each of the locations 2000 through 3776 is made a hit and the address of each location is written into itself. Then the routine goes back and makes sure each of those locations still contains its own address. If the halt at 17 772 362 is executed, then there is a dual addressing problem. If the halt at 17 772 370 is executed, then the address being tested should have been a hit but was not. This test should be run twice; once for each group as just outlined.

```
R3          002000
R4          001000
R5          177752
SP          000500
00000114    000116
00000116    000000          HALT
17772340    010300  1$:     MOV     R3,R0
17772342    010401          MOV     R4,R1
17772344    005710  2$:     TST     (R0)
17772346    010020          MOV     R0,(R0)+
17772350    077103          SOB     R1,2$
17772352    010300          MOV     R3,R0
17772354    010401          MOV     R4,R1
17772356    020010  3$:     CMP     R0,(R0)
17772360    001401          BEQ     4$
17772362    000000          HALT
17772364    006015  4$:     ROR     (R5)
17772366    103401          BCS     5$
17772370    000000          HALT
17772372    005120  5$:     COM     (R0)+
17772374    077110          SOB     R1,3$
17772376    000760          BR      1$
```

Test 5 Main Memory Data Patterns Test

This routine puts data patterns that the user designates in the Switch register in the lower 28K of memory. Since the program loops, the specified data pattern can be changed as the program runs. The test should be run while forcing misses to both cache groups (deposit 14 in the Cache Control register at 17 777 746). If the HALT at 116 is executed, then a parity error occurred with the designated data pattern at the address in R0. If the HALT at 17 772 366 is executed, then the data read from the location does not match the data written into it. If either HALT is executed, the address (R0) will be displayed on the console. A suggested data pattern to put in the Switch register is 125252 or 052525; 000000 and 177777 might also be tried.

```
SP              000500
00000114        000116
00000116        000000          HALT
17772340        012700  1$:     MOV     #500,R0
17772342        000500
17772344        012701          MOV     #067540,R1
17772346        067540
17772350        013703  2$:     MOV     @#SWR,R3
17772352        177570
17772354        010310          MOV     R3,(R0)
17772356        005110          COM     (R0)
17772360        005110          COM     (R0)
17772362        022003          CMP     (R0,+,R3
17772364        000401          BEQ     3$
17772366        000000          HALT
17772370        077111  3$:     SOB     R1,2$
17772372        000762          BR      1$
```

Test 6 Address Memory Dual Addressing Test

This routine performs a dual addressing test on the cache address memory. This sequence of tags (bits A10 through A21) is written into the address memory:

0
1
2
3
4
5
•
•
•
36
37
0
1
2
•
•
•

This is done by generating the sequence of addresses:

00002000
00002002
00004004
00004006
00006010
00006012
00010014
00010016
•
•
•

and making each a hit in one group. Then the routine goes back and re-references that same series of addresses to ensure that they all are still hits. Note how the addresses are made hits: The instruction at 17 772 350 (CMP (R0),(R0)+) is used, but when the routine goes back to check if the addresses are still hits, that instruction is changed to (CMP R0,(R0)+) by the XOR instruction. Then that instruction is changed back to (CMP (R0),(R0)+) by the XOR. This is done so when the addresses are originally made hits they are referenced twice; but when the routine goes back to see if they are still hits, only one reference is needed. If the HALT at 17 772 356 is executed, then an address which should have been a hit was not; the troubleshooter should examine location 17 772 350 to see if the routine was making the addresses hits for the first time, or if it was going back to ensure that they were all still hits. If the latter case is true, then three is a dual addressing problem in the address memory. This test should be run twice, once in each group as outlined in Test 1.

```
R2          100000
R3          002000
R4          000400
R5          177752
SP          001000
00000114    000116
00000116    000000          HALT
17772340    005000  1$:     CLR     R0
17772342    010401          MOV     R4,R1
17772344    060300  2$:     ADD     R3,R0
17772346    040200          BIC     R2,R0
17772350    021020  3$:     CMP     (R0),(R0)+
17772352    006015          ROR     (R5)
17772354    103401          BCS     5$
17772356    000000  4$:     HALT
17772360    005720  5$:     TST     (R0)+
17772362    006015          ROR     (R5)
17772364    103374          BCC     4$
17772366    077112          SOB     R1,2$
17772370    074737          XOR     SP,@#3$
17772372    172350
17772374    000761          BR      1$
```

Test 7 Main Memory Data Pattern Test

This routine can be used to run a data pattern test on any 4K bank of memory. The user specifies which bank by setting the switches in the Switch register to any 100 (8) word block of memory. For example: To test addresses 2000 through 22000, put 20 in the Switch register. The routine loops continually so that the Switch register can be changed dynamically to test another memory bank without restarting the program. The test is run with the data pattern in R4. That pattern is written into every tested word and complemented twice. Suggested patterns are 125252 or 052525. Note that memory management is turned on while running this test from the PARs themselves. The user should force misses to both cache groups to run this test; put 14 in the Cache Control register at 17 777 746. If the HALT at 116 is executed, then a parity error occurred at the address contained in R0, that is displayed when the HALT is executed. If the HALT at 17 772 340 is executed, then the data that was read out of the location being tested did not match the data that was written; the address in R0 will be displayed. Note that this test does not have 17 772 340 as its starting address as do all the other routines. Its starting address is 17 772 342. Also note that the user should be careful not to specify a test of non-existent memory that will cause a trap to 4. Any memory up to 2 million words can be checked.

```
R2              010000
R4              125252          THE DATA PATTERN
SP              000500
00000114        000116
00000116        000000          HALT
17777572        000001
17772516        000020
17772300        077406
17772306        077406
17772316        077406
17772340        000000  1$:     HALT
17772342        013727  2$:     MOV     @#SWR,#000000
17772344        177570
17772346        000000
17772350        012700          MOV     #060000,R0
17772352        060000
17772354        000401          BR      .+1
17772356        177600          .WORD   177600
17772360        010201          MOV     R2,R1
17772362        010410  3$:     MOV     R4,(R0)
17772364        005110          COM     (R0)
17772366        005110          COM     (R0)
17772370        020420          CMP     R4,(R0)+
17772372        001362          BNE     1$
17772374        077106          SOB     R1,3$
17772376        000761          BR      2$
```

Test 8 Address Memory Hits Test

This routine will check that any address in memory can be made a hit. It checks 4K at a time. The user specifies which 4K bank is to be tested using the Switch register. The user must specify the 100 (8) word block number of the starting address of the 4K bank he/she wishes to have tested. For example, if the user puts 1007 in the switches, addresses 00 100 700 through 00 120 700 will be tested. The routine loops continually so that the user can dynamically change the specified bank to another. If a parity error occurs, then the HALT at 116 will be executed. If the halt at 17 772 340 is executed, then the routine was unable to make the address in R0 a hit. The routine should be run twice, once for each group as outlined in Test 1.

```
SP              000500
00000114        000116
00000116        000000          HALT
17777572        000001
17772516        000020
17772300        077406
17772306        077406
17772316        077406
17772340        000000  1$:     HALT
17772342        013727  2$:     MOV     @#SWR,#000000
17772344        177570
17772346        000000
17772350        012700          MOV     #060000,R0
17772352        060000
17772354        000401          BR      .+1
17772356        177600          .WORD   177600
17772360        012701          MOV     #010000,R1
17772362        010000
17772364        021020  3$:     CP      (R0),(R0)+
17772366        006037          ROR     @#HITMISREG
17772370        177752
17772372        103362          BCC     1$
17772374        077105          SOB     R1,3$
17772376        000761          BR      1$
```

5.2 COLD START TROUBLESHOOTING

When a system is inoperative, the first things that should be checked and repaired if necessary include:

1. AC and dc power and cabling (Chapter 4)
2. Signal cabling (Paragraph 5.2.2 and Appendix A)
3. Console functions (Paragraph 5.2.3).

When the console is functioning properly, the diagnostics should be bootstrapped and the system verified. Refer to Figure 5-1.

The flowchart shown on Figure 5-2 suggests some steps that could be taken to bring a dead machine to the point at which the M9301-YC will operate. Console functions are described in detail in Section III of the *KB11-B Processor Manual* (PDP-11/70).

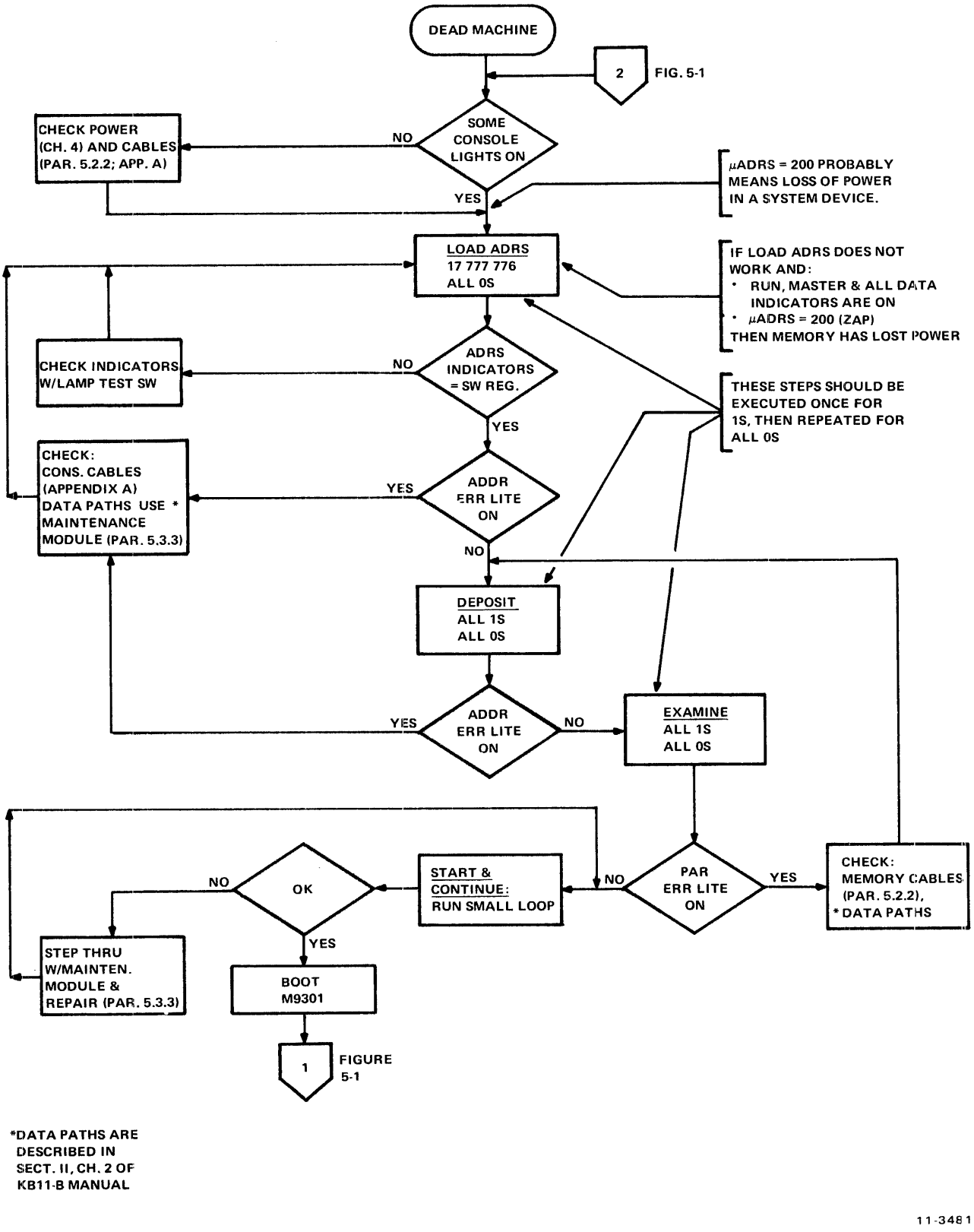


Figure 5-2 Troubleshooting Dead Machine

5.2.1 AC and DC Power
AC and dc power maintenance and troubleshooting are explained in Chapter 4 of this manual.

5.2.2 Cabling
This paragraph describes the cable routing for the memory, Massbus and Unibus, and console. Power (ac and dc) cabling is described in Chapter 4.

When looking at the top of the CPU box, the memory, Massbus, and Unibus cables are all routed to the rear of the cabinet. All these cables are ROUGH side up, RED STRIPE towards the backplane side of the modules. The console cables, on the other hand, are routed to the front of the box and have the SMOOTH side up, RED STRIPE toward the handle side of the modules (refer to Paragraph 5.2.2.4 for the console cables).

The SPC (small peripheral controller) cables are also routed toward the rear of the box.

SPC, MJ11, Massbus and Unibus cables are held in place at the rear of the CPU box by a clamp (Figure 5-3).

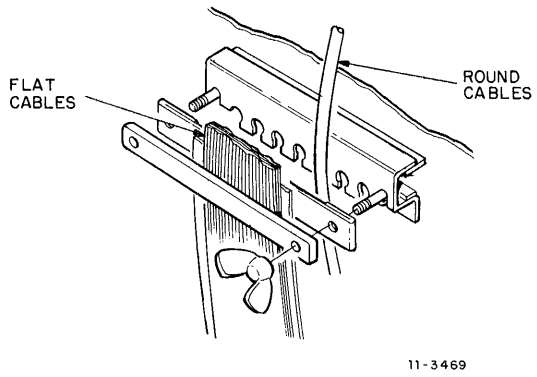


Figure 5-3 CPU Cable Holding Clamp

Some PDP-11/70 systems use wire cable troughs in which the cables are routed. Refer to Appendix H for details on this system.

5.2.2.1 MK11 Cabling -

1. All cables are marked at each end.

2. There are two address bus cables:

   From H8143 (ADML) J1 to M8158 (ABB) J1.
   From M8143 (ADML) J2 to M8158 (ABB) J3.

3. There are two data bus cables:

   From M8145 (CDPC) J1 to M8159 (DBB) J1.
   From M8145 (CDPC) J2 to M8159 (DBB) J3.

4. At the CPU end, the SMOOTH side of the bus cables face the module into which it is plugged. The red stripe is on the left (handle side of module).

5. At the MK11, the red stripe is on the left side as seen from the component side of the module. Incoming cables, from the CPU, have the SMOOTH side up; outgoing cables, to next memory frame, have the RIBBED side up.

6. There are two box controller cables:

   From box controller J1 to memory frame J31.
   From box controller J2 (SMOOTH side up) to M8159 (DBB) J5.
(SMOOTH side up, red stripe to left on component side of board).

7. There are three battery backup power cables:

   From memory frame J28 to H775 unit A, J1.
   From memory frame J29 to H775 unit B, J1.
   From memory frame J30 to H775 unit C, J1.

5.2.2.2 MJ11 Cabling

1. All cables are marked at each end.

2. There are two address cables:

   From M8143 (ADML) J1 to M8147/M8148 (MCTA) J1.
   From M8143 (ADML) J2 to M8147/M8148 (MCTA) J3.

3. There are two data cables:

   From M8145 (CDPC) J1 to M8149 (MXRA) J1.
   From M8145 (CDPD) J2 to M8149 (MXRB) J3.

4. At the CPU end, the SMOOTH side of the cables faces the module into which it is plugged. The red stripe is on the left (handle side of the module).

5. At the MJ11 end, the ROUGH side of the cable faces the module into which it is plugged. The red stripe is on the side of the cable closer to the front of the drawer (Figure 5-4).

5.2.2.3 Massbus Cabling

1. There are three Massbus cables per controller.

2. These cables plug into J1 of the three M5904 modules, SMOOTH side facing the module into which it is plugged.

3. The red stripe is on the left (handle side of module).

4. Refer to the several Massbus device maintenance manuals for the cable connections at the device.

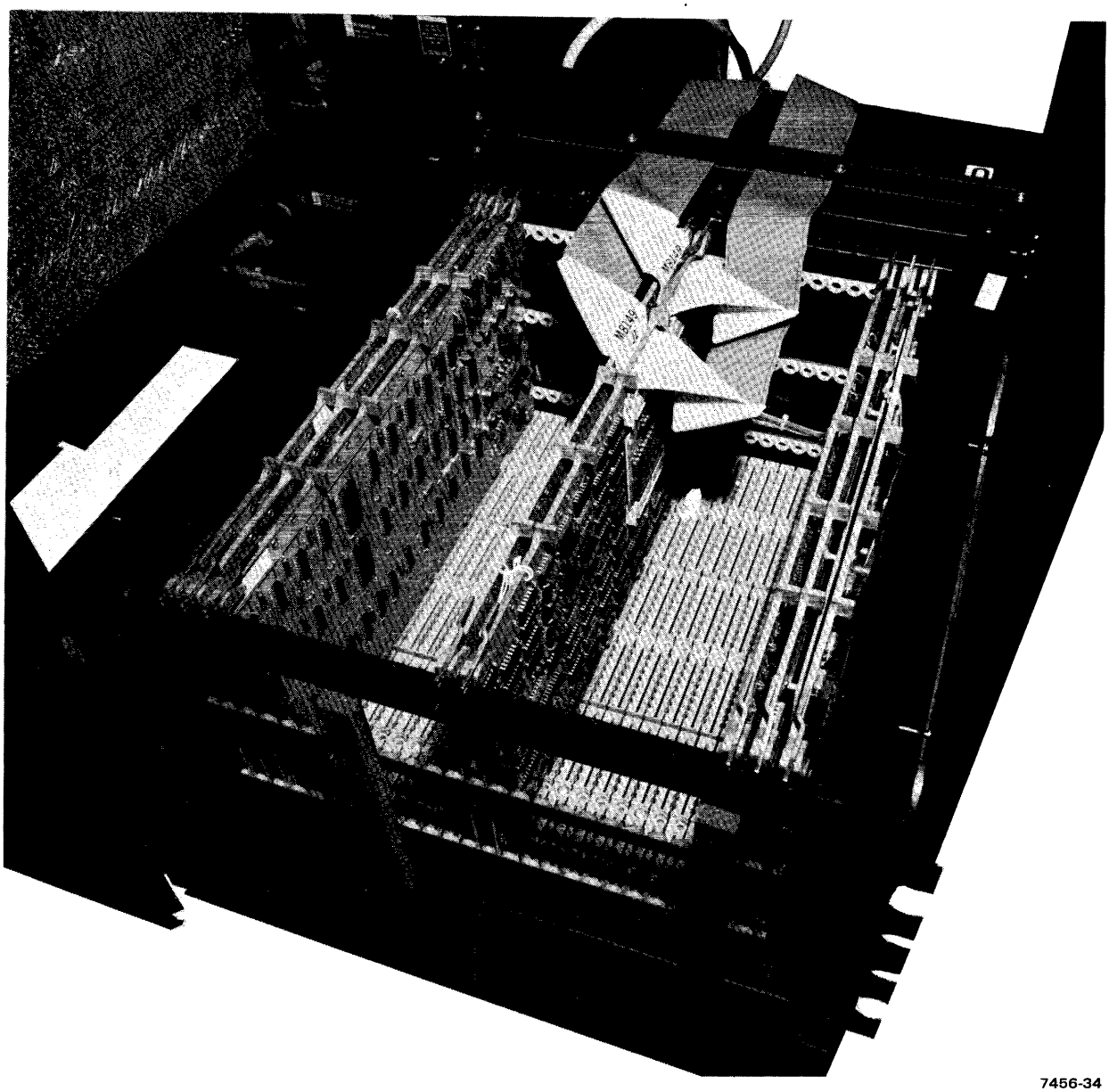


Figure 5-4 MJ11 Frame Cabling

5.2.2.4 PDP-11/70 Unibus Cabling - The BC11-A cable is the I/O bus that connects all Unibus system components external to the CPU cabinet. To connect the Unibus between the CPU cabinet and an expansion cabinet, insert the BC11-A cable in slot A44 of the CPU mounting box cabinet. The cable runs through a cable clamp in the upper left corner at the rear of the CPU mounting box and passes under the power supply mounting rails into the next cabinet. In the expansion cabinet, the cable passes through a similar cable clamp and is inserted in the appropriate slot of the first system unit of the BA11-K mounting box. Adjacent system units in a mounting box are connected by an M9202 Unibus connector module. The Unibus must be terminated at the CPU end (slots E01 and F01) by an M9301-YC.

If the Unibus interconnects more than 20 bus loads, or is longer than 50 feet, a DB11-A bus repeater must be used. Refer to Paragraph 3.6 for Unibus loading and configuration rules. A section of bus delimited by bus repeater(s) is called a bus segment, and must be terminated at both ends with an M930 bus terminator. The last terminator on the Unibus must be an M9302.

5.2.2.5 Console Cabling

Power Connector
Power is supplied to the console by processor harness plug P1. Insert this plug into console PC board connector J4.

Signal Connectors
Three flat signal cables connect the console to the processor modules.

1. J1 connects to J1 on M8134 (PDR, slot 10).

2. J2 connects to J1 on M8140 (SCC, slot 16): J3 connects to J2 on the same module. J1 on the M8140 is the connector closer to the edge of the module.

Installation of Signal Cables
The three signal cables are installed with the rough side facing the console PC board. The red stripe is on the side of the flat cables that is closer to the power harness connector J4. The smooth side of the cable faces the M8134 and M8140 modules.

5.2.3 Console Operations
The console operations, as listed below, can only be executed when the processor is in the HALT state (microprogram address = 170) and the console key is in the ON position.

Console operations are the following:

1. LOAD ADDRESS

2. DEPOSIT and DEPOSIT/STEP

   Memory (00 000 000 - SYSTEM SIZE REGISTER)
   Peripheral Page (17 777 776 - 17 760 000)
   General Register (17 777 717 - 17 777 700)

3. EXAMINE and EXAMINE/STEP

   Memory (00 000 000 - SYSTEM SIZE REGISTER)
   Peripheral Page (17 777 776 - 17 760 000)
   General Register (17 777 717 - 17 777 700)

4. START

5. CONTINUE

Section III of the *KB11-B Processor Manual* contains a description of these functions as well as those of the console indicators (Chapter 1), and a detailed description of the console logic (Chapter 2).

NOTE

It is important to use the correct setting of the address select switch:

VIRTUAL - Six positions: KERNEL, SUPER and USER I space and KERNEL, SUPER and USER D space. The address displayed is a 16-bit virtual address; bits 21 - 16 are always off.

CONS PHY - (Console Physical). The 22-bit address entered by a LOAD ADRS is the physical address of the console operation.

PROG PHY - (Program Physical). Displays the 22-bit physical address generated by memory management for the current Unibus or memory cycle.

5.3 TROUBLESHOOTING AIDS

5.3.1 PDP-11/70 Unibus Registers and Addresses

The peripheral page addresses of particular concern to the PDP-11/70 are listed below in numerical order.

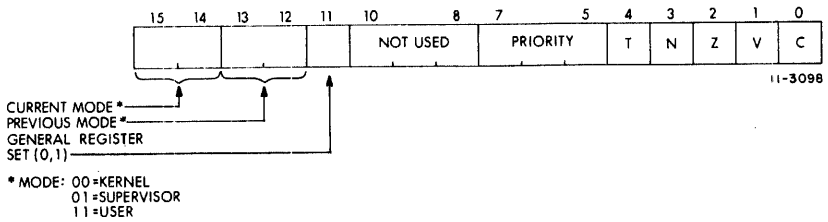
There are references to brief descriptions in this paragraph and to the appropriate manaul.

Address	Register	References
17 777 776	Processor Status Word (PS)	
17 777 774	Stack Limit (SL)	
17 777 772	Program Interrupt Request (PIR)	
17 777 770	Microprogram Break	
17 777 766	CPU Error	
17 777 764	System I/D	
17 777 762	Upper Size	
17 777 760	Lower Size	
17 777 756 17 777 754	Reserved for future use	
17 777 716	Supervisor SP	R6
17 777 715	General Registers,	R5
17 777 714	Set 1	R4
17 777 713		R3
17 777 712		R2
17 777 711		R1
17 777 710		R0
17 777 707	Program Counter	R7 (PC)
17 777 706	Kernel SP	R6
17 777 705	General Registers,	R5
17 777 704	Set 0	R4
17 777 703		R3
17 777 702		R2
17 777 701		R1
17 777 700		R0
17 777 676 through 17 777 660	User Data PAR, Reg 0–7	MM Registers (5.3.1.2)
17 777 656 through 17 777 640	User Instruction PAR, Reg 0–7	
17 777 636 through 17 777 620	User Data PDR, Reg 0–7	
17 777 616 through 17 777 600	User Instruction PDR, Reg 0–7	
17 777 576	Memory Mgmt Regs: (MMR2)	
17 777 574	Memory Mgmt Regs: (MMR1)	
17 777 572	Memory Mgmt Regs: (MMR0)	

Address	Register	References
17 777 570	Console Switch and Display Register	Refer to Chapter 3, Section II of KB11-B, C Processor Manual.
17 777 566 17 777 564 17 777 562 17 777 560	LA36 DECwriter Printer Data LA36 DECwriter Printer Status LA36 DECwriter Keyboard Data LA36 DECwriter Keyboard Status	Refer to LA36 Manual. These locations are reserved for KB0, the system console.
17 777 556	PC11/PR11, punch data	
17 772 376 through 17 772 360	Kernel Data PAR, Reg 0–7	
17 772 356 through 17 772 340	Kernel Instruction PAR, Reg 0–7	
17 772 336 through 17 772 320	Kernel Data PDR, Reg 0–7	
17 772 316 through 17 772 300	Kernel Instruction PDR, Reg 0–7	
17 772 276 through 17 772 260	Supervisor Data PAR, Reg 0–7	
17 772 256 through 17 772 240	Supervisor Instruction PAR, Reg 0–7	
17 772 236 through 17 772 220	Supervisor Data PDR, Reg 0–7	
17 772 216 through 17 772 200	Supervisor Instruction PDR, Reg 0–7	
17 770 366 through 17 770 200	Unibus Map	Refer to Paragraph 5.3.1.3
17 765 776 through 17 765 000	Part of PDP-11/70 diagnostic bootstrap	Refer to Paragraphs 3.4.2 and 5.4

5.3.1.1 CPU Registers – The CPU registers are briefly explained here. For complete details, refer to Section II, Chapter 3, of the *KB11-B Processor Manual.*

Processor Status Word 17 777 776



15-14: Current Mode
Specifies the current processor mode as follows:

1. When PS(15:14) = 0, the processor is in Kernel mode; all operations are legal.

2. When PS(15:14) = 01, the processor is in Supervisor mode; HALT, RESET, and SPL instructions either trap to location 4 (HALT) or are treated as NOP (RESET and SPL); SUPER address space is used if memory management is enabled.

3. PS(15:14) = 10 is an illegal mode; if memory management is enabled, a memory management abort occurs (refer to Section IV of the *KB11-B Processor Manual).*

4. When PS(15:14) = 11, the processor is in User mode; HALT, RESET, and SPL instructions either trap to location 4 (HALT) or are treated as NOP (RESET and SPL) USER address space is used if memory management is enabled.

13-12: Previous Mode
Specifies the processor mode prior to the last trap, interrupt, or loading of the PS.

11: Register Set
Specifies which general register set is used; if PS11 = 0, register set 0 is selected; if PS11 = 1, register set 1 is used.

10-08: Unused

07-05: Priority
Sets the processor priority; this priority determines which levels of programmed and external device interrupt requests are honored.

04: Trace
When PS04 = 1, the processor traps to the trace trap vector address (14 octal) after each instruction fetch; this facility is used to debug programs.

03: N Condition Code
This bit is set when the result of the last data manipulation is negative.

02: Z Condition Code
This bit is set when the result of the last data manipulation is 0.

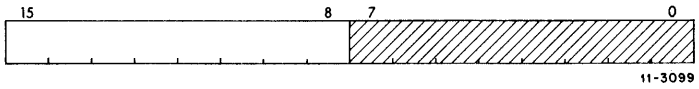
01: V Condition Code
This bit is set when the result of the last data manipulation causes an arithmetic overflow.

00: C Condition Code
This bit is set when a carry occurs during data manipulation.

Stack Limit Register 17 777 774
The stack limit allows program control of the lower limit for permissible stack addresses. This limit may be varied in increments of 400 (8) bytes or 200 (8) words, up to a maximum address of 177 400 (almost the top of a 32K memory).

The normal boundary for stack addresses is 400. The stack limit option allows this lower limit to be raised, providing more address space for interrupt vectors or other data that should not be destroyed by the program.

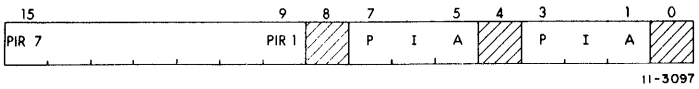
The Stack Limit register has the following format:



The Stack Limit register can be addressed as a word at location 17 777 774, or as a byte at location 17 777 775. The register is accessible to the processor and console, but not to any bus device.

The 8 bits, 15 through 8, contain the stack limit information. These bits are cleared by INIT. The lower 8 bits are not used. Bit 8 corresponds to a value of 400 (8) or 256 (10).

Program Interrupt Request Register (PIR) 17 777 772
A request is booked by setting one of the bits 15 through 9 (for PIR 7 - PIR 1) in the Program Interrupt register at location 17 777 772. The hardware sets bits 7-5 and 3-1 to the encoded value of the highest PIR bit set. This Program Interrupt Active (PIA) should be used to set the processor level and also index through a table of interrupt vectors for the seven software priority levels. The following figure shows the layout of the PIR register.

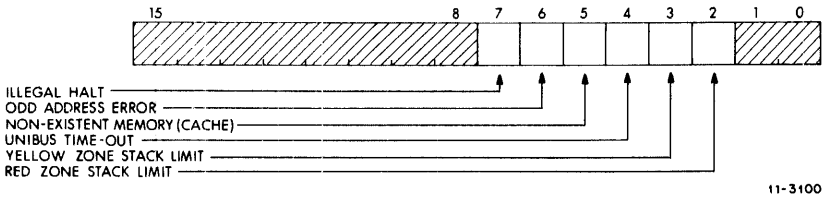


When the PIR is granted, the processor will trap to location 240 and pick up PC in 240 and the PSW in 242. It is the interrupt service routine's responsibility to queue requests within a priority level and to clear the PIR bit before the interrupt is dismissed.

Microprogram Break Register 17 777 770
This register is used for maintenance purposes only. It is used with maintenance equipment to provide timing synchronization and testing facilities. The microaddress in this register generates a sync pulse at T1 at pin F13K2 each time the cycle corresponding to the address is executed (TIGB PB SYNCH H); a pulse whose width is the same as that of the cycle is also generated at A10E1 (PDRC PB CMP H).

Refer to the *KB11-B* or *KB11-C Processor Manual* Section II, Paragraphs 3.6 and 4.9.2.

CPU Error Register 17 777 766



This register identifies the source of the abort or trap that used the vector at location 4.

7: Illegal Halt
Set when trying to execute a HALT instruction when the CPU is in User or Supervisor mode (not Kernel).

6: Odd Address Error
Set when a program attempts to do a word reference to an odd address.

5: Non-existent Memory
Set when the CPU attempts to read a word from a location higher than indicated by the System Size register. This does not include Unibus addresses.

4: Unibus Timeout
Set when there is no response on the Unibus within approximately 10 μs.

3: Yellow Zone Stack Limit
Set when a yellow zone trap occurs.

2: Red Zone Stack Limit
Set when a red zone abort occurs.

System I/D Register 17 777 764
This read only register contains information uniquely identifying each system. As of this writing, the bits are undefined.

Upper Size Register 17 777 762
This register is an extension of the lower size register, which is reserved for future use. It is read only and its contents are always read as zero.

Lower Size Register 17 777 760
This read only register specifies the memory size of the system. It is defined to indicate the last addressable block of 32 words in memory (bit 0 is equivalent to bit 6 of the Physical Address).

Refer to Paragraph 3.5.4 and to the *KB11-B Processor Manual*, Section IV, Chapter 5.

CPU General Registers 17 777 717 - 17 777 700
The general registers can be used as accumulators, index registers, auto-increment registers, auto-decrement registers, or as stack pointers for temporary storage of data. Arithmetic operations can be from one general register to another, from one memory or device register to another, or between memory or device register and a general register.

R7 is used as the machine's program counter (PC) and contains the address of the next instruction to be executed. It is a general register normally used only for addressing purposes and not as an accumulator for arithmetic operations.

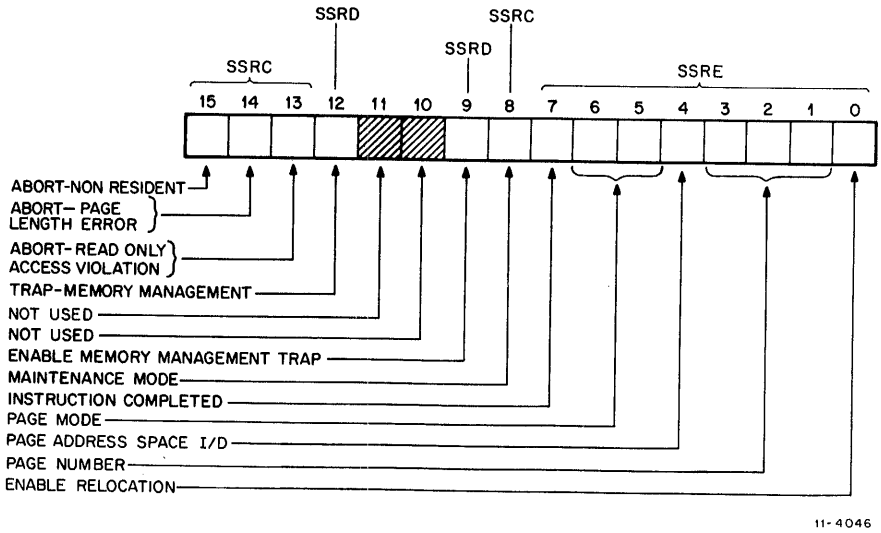
The R6 register is normally used as the processor stack pointer indicating the last entry in the appropriate stack (Kernel stack, Supervisor stack, and User stack). When the central processor is operating in Kernel mode it uses the Kernel stack, in Supervisor mode, the Supervisor stack, and in User mode, the User stack. When an interrupt or trap occurs, the PDP-11/70 automatically saves its current status on the Processor stack selected by the service routine.

The remaining 12 registers are divided into two sets of unrestricted registers, R0–R5. The current register set in operation is determined by the processor status word bit 11.

Refer to the *KB11-B Processor Manual,* Section II, Paragraphs 2.1.3 and 2.1.4.

5.3.1.2 Memory Management Registers – A brief description of the Memory Management registers follows. For a detailed description of their operation, refer to Section IV of the *KB11-B Processor Manual.*

Memory Management Register 0 (MMR0)
MMR0 contains error flags, the page number whose reference caused the abort, and various other status flags. The register is organized as follows:



Setting bit 0 of this register enables address relocation and error detection. This means that the bits in MMR0 become meaningful.

Bits 15–12 are the error flags. They may be considered to be in a "priority queue" in that "flags to the right" are less significant and should be ignored. That is, a "nonresident" fault-service routine would ignore length, access control, and memory management flags. A "page length" service routine would ignore access control and memory management faults, etc.

Bits 15–13, when set (error conditions), cause memory management to freeze the contents of bits 1-7 and Memory Management registers 1 and 2. This has been done to facilitate error recovery.

These bits may also be written under program control. No abort will occur, but the contents of the Memory Management registers will be locked up as in an abort.

15: Abort-Nonresident
Bit 15 is the abort-nonresident bit. It is set by attempting to access a page with an Access Control Field (ACF) key equal to 0, 3, or 7. It is also set by attempting to use memory relocation with a processor mode of 2.

14: Abort-Page Length
Bit 14 is the abort-page length bit. It is set by attempting to access a location in a page with a block number (virtual address bits, 12-6) that is outside the area authorized by the Page Length Field (PLF) of the Page Descriptor Register (PDR) for that page. Bits 14 and 15 may be set simultaneously by the same access attempt. Bit 14 is also set by attempting to use memory relocation with a processor mode of 2.

13: Abort-Read Only
Bit 13 is the abort-read only bit. It is set by attempting to write in a read-only page. Read only pages have access keys of 1 or 2.

12: Trap-Memory Management
Bit 12 is the trap-memory management bit. It is set whenever a memory management trap condition occurs; that is, a read operation which references a page with an Access Control Field (ACF) of 1 or 4, or a write operation to a page with an ACF key of 4 or 5.

11 and 10 – Spares
Bits 11 and 10 are spare and are always read as 0; they should never be written. They are unused and reserved for possible future expansion.

9: Enable Memory Management Traps
Bit 9 is the enable memory management traps bit. It is set or cleared by doing a direct write into MMR0. If bit 9 is 0, no memory management traps will occur. The A and W bits will, however, continue to log memory management trap conditions. When bit 9 is set to 1, the next memory management trap condition will cause a trap, vectored through Kernel virtual address 250.

Note that if an instruction which sets bit 9 to 0 (disable memory management trap) causes a memory management trap condition in any of its memory references prior to and including the one actually changing MMR0, then the trap will occur at the end of the instruction anyway.

8: Maintenance/Destination Mode
Bit 8 specifies that only destination mode references will be relocated using memory management. This bit may be used only for maintenance purposes.

7: Instruction Completed
Bit 7 indicates that the current instruction has been completed. It will be set to 1 during T bit, parity, odd address, and time out traps and interrupts. This provides error handling routines with an aid to determine whether the last instruction will have to be repeated in the course of an error recovery attempt. Bit 7 is read only (it cannot be written). It is initialized to a 1. Note that EMT, TRAP, BPT, and IOT do not set bit 7. Refer to Section IV, Paragraph 9.1.4 of the *KB11-B Processor Manual.*

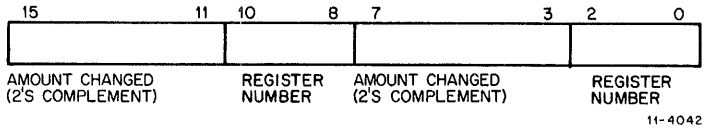
5 and 6: Processor Mode
Bits 5 and 6 indicate the CPU Mode (Kernel/Supervisor/User) associated with the page causing the abort (Kernel = 00, Supervisor = 01, User = 11, Illegal mode = 10). If an Illegal mode is specified, bits 15 and 14 will be set.

4: Page Address Space
Bit 4 indicates the type of address space (I or D) the Unit was in when a fault occurred (0 = I Space, 1 = D Space). It is used in conjunction with bits 3-1, Page Number.

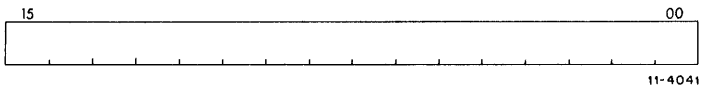
3 to 1: Page Number
Bits 3-1 contain the page number of a reference causing a memory management fault. Note that pages, like blocks, are numbered from 0 upward.

0: Enable Relocation
Bit 0 is the enable relocation bit. When it is set to 1, all addresses are relocated by the unit. When bit 0 is set to 0, the memory management unit is inoperative and addresses are not relocated or protected.

Memory Management Register 1 (MMR1) 17 777 574
MMR1 records any autoincrement/decrement of the general purpose registers, including explicit references through the PC. MMR1 is cleared at the beginning of each instruction fetch. Whenever a general purpose register is either autoincremented or autodecremented, the register number and the amount (in 2s complement notation) by which the register was modified, is written into MMR1.

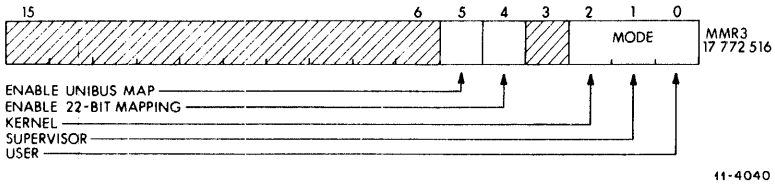


Memory Management Register 2 (MMR2) 17 777 576
MMR2 is loaded with the 16-bit virtual address (VA) at the beginning of each instruction fetch, or with the address trap vector at the beginning of an interrupt, T bit trap, parity, odd address, and timeout aborts and parity trap. Note that MMR2 does not get the trap vector on EMT, TRAP, BPT and IOT instructions. MMR2 is read only; it cannot be written. MMR2 is the Virtual Address Program Counter.



Memory Management Register 3 (MMR3) 17 772 516
Memory Management Register 3 (MMR3) enables or disables the use of the D space PARs and PDRs and 22-bit mapping and Unibus mapping. When D space is disabled, 11 references use the I space registers; when D space is enabled, both the I space and D space registers are used. Bit 0 refers to the User's registers, bit 1 to the Supervisors, and bit 2 to the Kernels. When the appropriate bits are set, D space is enabled; when clear, it is disabled. Bit 03 is read as zero and never written. It is reserved for future use. Bit 04 enables 22-bit mapping. If memory management is not enabled, bit 04 is ignored and 16-bit mapping is used.

If bit 4 is clear and memory management is enabled (bit 0 of MMR0 is set), the computer uses 18-bit mapping. If bit 4 is set and memory management is enabled, the computer uses 22-bit mapping. Bit 5 is set to enable relocation in the Unibus map; the bit is cleared to disable reloaction. Bits 6 to 15 are unused. On initialization, this register is set to 0 and only I space is in use.



Bit	State	Operation
5	0	Unibus map relocation disabled
	1	Unibus map relocation enabled
4	0	Enable 18-bit mapping } if bit 0 of MMR0
	1	Enable 22-bit mapping } is set
2	1	Enable Kernel D Space
1	1	Enable Supervisor D Space
0	1	Enable User D Space

Page Address Registers (PAR)
The Page Address Register (PAR) contains the Page Address Field (PAF), 16-bit field, which specifies the starting address of the page as a block number in physical memory.

The addresses of these registers are listed in Table 5-2.

The Page Address Register may be alternatively thought of as a Relocation register containing a relocation constant, or as a Base register containing a base address. Either interpretation indicates the basic importance of the Page Address Register (PAR) as a relocation tool.

There are six sets of eight PARs, one set for Kernel Data Space, one for Kernel Instruction Space, one for Supervisor Data Space, one for Supervisor Instruction Space, one for User Data Space, and one for User Intruction Space.

Page Descriptor Registers (PDR)
The Page Descriptor Register (PDP) contains information relative to page expansion, page length, and access control.

There are six sets of eight PDRs which are allocated in the same manner as the PARs. The addresses of these registers are listed in Table 5-2.

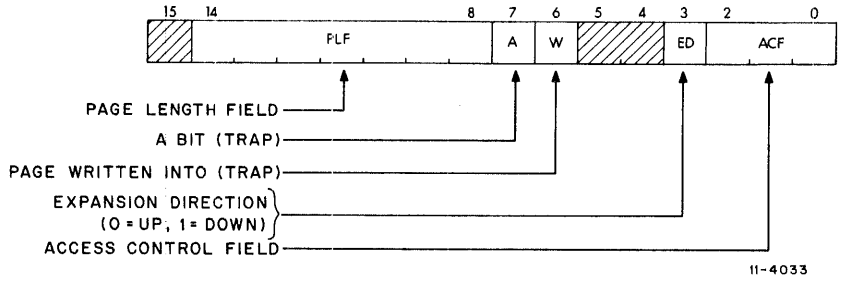


Table 5-2 PAR/PDR Unibus Addresses

Kernel

I Space			D Space		
No.	**PAR**	**PDR**	**No.**	**PAR**	**PDR**
0	17 772 340	17 772 300	0	17 772 360	17 772 320
1	17 772 342	17 772 302	1	17 772 362	17 772 322
2	17 772 344	17 772 304	2	17 772 364	17 772 324
3	17 772 346	17 772 306	3	17 772 366	17 772 326
4	17 772 350	17 772 310	4	17 772 370	17 772 330
5	17 772 352	17 772 312	5	17 772 372	17 772 332
6	17 772 354	17 772 314	6	17 772 374	17 772 334
7	17 772 356	17 772 316	7	17 772 376	17 772 336

Supervisor

I Space			D Space		
No.	**PAR**	**PDR**	**No.**	**PAR**	**PDR**
0	17 772 240	17 772 200	0	17 772 260	17 772 220
1	17 772 242	17 772 202	1	17 772 262	17 772 222
2	17 772 244	17 772 204	2	17 772 264	17 772 224
3	17 772 246	17 772 206	3	17 772 266	17 772 226
4	17 772 250	17 772 210	4	17 772 270	17 772 230
5	17 772 252	17 772 212	5	17 772 272	17 772 232
6	17 772 254	17 772 214	6	17 772 274	17 772 234
7	17 772 256	17 772 216	7	17 772 276	17 772 236

User

I Space			D Space		
No.	**PAR**	**PDR**	**No.**	**PAR**	**PDR**
0	17 777 640	17 777 600	0	17 777 660	17 777 620
1	17 777 642	17 777 602	1	17 777 662	17 777 622
2	17 777 644	17 777 604	2	17 777 664	17 777 624
3	17 777 646	17 777 606	3	17 777 666	17 777 626
4	17 777 650	17 777 610	4	17 777 670	17 777 630
5	17 777 652	17 777 612	5	17 777 672	17 777 632
6	17 777 654	17 777 614	6	17 777 674	17 777 634
7	17 777 656	17 777 616	7	17 777 676	17 777 636

2 to 0: Access Control Field (ACF)
This three-bit field, occupying bits 2-0 of the Page Descriptor Register (PDR) contains the access rights to this particular page. The access codes or "keys" specify the manner in which a page may be accessed and whether or not a given access should result in a trap or an abort of the current operation. A memory reference which causes an abort is not completed while a reference causing a trap is completed. In fact, when a memory reference causes a trap to occur, the trap does not occur until the entire instruction has been completed. Aborts are used to catch a "missing page fault," prevent illegal access, etc.; traps are used as an aid to gather memory management information.

In the context of access control, the term "write" is used to indicate the action of any instruction that modifies the contents of any addressable word.

The modes of access control are as follows:

000 Nonresident Abort all accesses

001 Read only Abort on write attempt, memory management trap on read

010 Read only Abort on write attempt

011 Unused Abort all accesses – reserved for future use

100 Read/write Memory management trap upon completion of a read or write

101 Read/write Memory management trap upon completion of a write

110 Read/write No system trap/abort action

111 Unused Abort all accesses – reserved for future use

It should be noted that the use of I Space provides the user with a further form of protection, execute only.

7: A Bit
This bit is used by software to determine whether any accesses to this page met the trap condition specified by the Access Control Field (AFC) (A = 1 is affirmative). The A Bit is used in the process of gathering memory management statistics.

6: W Bit
This bit indicates whether this page has been modified (i.e., written into) since either the PAR or PDR was loaded. (W = 1 is affirmative). The W Bit is useful in applications that involve disk swapping and memory overlays. It is used to determine which pages have been modified and hence must be saved in their new form, and which pages have not been modified and can be simply overlaid.

Note that A and W bits are "reset" to "0" whenever either PAR or PDR is modified (written into).

3: Expansion Direction (ED)
Bit 03 of the Page Description Register (PDR) specifies in which direction the page expands. If ED = 0 the page expands upwards from Block Number 0 to include blocks with higher addresses; if ED = 1, the page expands downwards from Block Number 127 to include blocks with lower addresses. Upward expansion is usually used for program space while downward expansion is used for stack space.

14 to 08: Page Length Field (PLF)
This 7-bit field specifies the block number, which defines the boundary of that page.

The block number of the virtual address is compared against the page length field to detect length errors. An error occurs when expanding upwards if the block number is greater than the page length field, and when expanding downwards if the block number is less than the page length field.

15, 5, and 4: Reserved Bits
Bits 15, 5, and 4 are spare, are always read as 0, and should never be written. They are unused and reserved for possible future expansion.

5.3.1.3 Unibus Map Registers 17 770 336 – 17 770 200 – There are a total of 31 mapping registers for address relocation. Each register is composed of a double 16-bit PDP-11 word (in consecutive locations) that holds the 22-bit base address.

If Unibus Map relocation is enabled, the five high order bits of the Unibus address are used to select one of the 31 mapping registers. The low order 13 bits of the incoming address are used as an offset from the base address contained in the 22-bit mapping register. To form the physical address, the 13 low order bits of the Unibus address are added to 22 bits of the selected mapping register to produce the 22-bit physical address. The lowest order bit of all mapping registers is always a zero, since relocation is always on word boundaries.

Table 5-3 shows the correspondence between the Unibus address when reading or writing the Unibus Map registers and the peripheral page addresses that will use these same registers for mapping.

For a detailed description of Unibus Map operation, refer to Section V, Chapters 1 and 3 of the *KB11-B Processor Manual.*

5.3.1.4 Cache Registers – The PDP-11/70 utilizes byte parity throughout the memory system. Parity is checked on each byte of a word (the sum of the bits, 8 data plus one parity should always be odd).

When a parity error occurs under normal operation, it causes a trap through location 114. Exception is made when parity traps are disabled.

In general, two types of action can be taken as the result of a parity error. One is an abort of the memory reference, where the cycle detecting the parity error is suspended and the CPU is immediately trapped through location 114. The other type of action is a trap. This occurs at the completion of the instruction being executed and also traps the CPU through vector 114. Since the PDP-11/70 fetches two 16-bit words from main memory into the cache on misses, it is possible for parity errors to occur on either of the words being fetched. One of the two words fetched is not used immediately.

Aborts, in general, are the result of parity errors occurring on the data word requested by the memory reference, while traps occur if the data word not needed by the reference is the cause of the parity error.

Table 5-3 Access to Unibus Map Registers

Register No.	Unibus Address Read or Write		Unibus Address for Memory Reference When Mapping
	Low Order Bits	High Order Bits	
0	17 770 200	02	17 000 000 – 17 017 777
1	17 770 204	06	17 020 000 – 17 037 777
2	17 770 210	12	17 040 000 – 17 057 777
3	17 770 214	16	17 060 000 – 17 077 777
4	17 770 220	22	17 100 000 – 17 117 777
5	17 770 224	26	17 120 000 – 17 137 777
6	17 770 230	32	17 140 000 – 17 157 777
7	17 770 234	36	17 160 000 – 17 177 777
10	17 770 240	42	17 200 000 – 17 217 777
11	17 770 244	46	17 220 000 – 17 237 777
12	17 770 250	52	17 240 000 – 17 257 777
13	17 770 254	56	17 260 000 – 17 277 777
14	17 770 260	62	17 300 000 – 17 317 777
15	17 770 264	66	17 320 000 – 17 337 777
16	17 770 270	72	17 340 000 – 17 357 777
17	17 770 274	76	17 360 000 – 17 377 777
20	17 770 300	02	17 400 000 – 17 417 777
21	17 770 304	06	17 420 000 – 17 437 777
22	17 770 310	12	17 440 000 – 17 457 777
23	17 770 314	16	17 460 000 – 17 477 777
24	17 770 320	22	17 500 000 – 17 517 777
25	17 770 324	26	17 520 000 – 17 537 777
26	17 770 330	32	17 540 000 – 17 557 777
27	17 770 334	36	17 560 000 – 17 577 777
30	17 770 340	42	17 600 000 – 17 617 777
31	17 770 344	46	17 620 000 – 17 637 777
32	17 770 350	52	17 640 000 – 17 657 777
33	17 770 354	56	17 660 000 – 17 677 777
34	17 770 360	62	17 700 000 – 17 717 777
35	17 770 364	66	17 720 000 – 17 737 777
36	17 770 370	72	17 740 000 – 17 757 777
*37	17 770 374	76	17 760 000 – 17 777 777

*Note: Can be read or written into, but not used for mapping.

In the case where the memory word that is not required causes the parity error, a trap is set up for execution at the end of the instruction. If this word then becomes a desired location prior to the completion of the instruction, the instruction is also aborted immediately during the reference when it is the desired word.

Memory System Troubleshooting Aids

The PDP-11/70 contains numerous memory system troubleshooting aids. The most significant of which are the Error registers, which store information at the time of error for future reference.

These registers are listed in this paragraph along with a short description of each.

In addition to these registers, the console panel provides a parity error indicator and two byte parity bits adjacent to the Data register.

The parity error indicator operates dynamically: it follows the parity error lines from the memory system. Thus, when running a program, this indicator will be ON when an error occurs, and is cleared once it has been acknowledged by the trap sequence in the microprogram. For console operations this light remains on (after a parity error resulting from an EXAMINE) until another console function is executed.

The two parity bits adjacent to the Data register are loaded along with the 16 data bits when examining a location from the console. They are cleared on DEPOSIT. These bits can be used to determine whether the correct parity exists for a word in cases where the parity checkers/generators are suspected as being bad. Note that when a location causes a parity error, neither the data nor the parity bits are loaded. Instead, the parity error indicator is lit and all information concerning the error is saved in the Error registers.

An important feature of the memory system Error registers is that in the case of multiple errors,

1. The Error registers preserve the information pertaining to the first error that occurred, and

2. In addition, they also flag the fact that a multiple error condition exists and that the memory system no longer can track the failures. These bits are explained in detail in the Memory System Error register bit description.

When a memory system error is detected, the processor traps to location 114. If location 114 is used as a trap catcher, the operator can examine the Memory System Error register to determine the type of error that has occurred. The Low Error Address registers can then be examined to determine where in the program, and during what type of cycle, the error occurred. If statistics on the hit ratio are desired, the Hit/Miss register can be read. The Control register can be read to determine what the control conditions were at the time the error occurred.

If location 114 is not used as a trap catcher, the previous tasks must be performed by the trap service routine.

The following points should be noted when troubleshooting the memory system:

1. The data patterns being written and read can affect detection of parity errors. For example, if a bit in the address memory or main memory is stuck high, a parity error will be detected only after writing a 0 into that bit position.

2. The replacement scheme within the cache is random. Thus:

   a. Whenever a miss occurs and a block of data within the cache must be overwritten, or

   b. Whenever a block of data is written immediately after power up,

   the group into which the word goes is selected at random.

3. Because of the replacement strategy, a parity error may be detected if data is read from a malfunctioning group, yet the same data will not generate a parity error when read from the non-malfunctioning group (or if fetched directly from main memory).

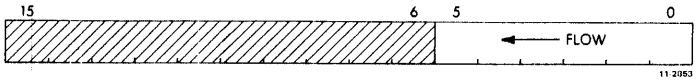
4. A parity check is made each time the address memory and fast data memory are accessed. A parity error can be detected even if the location being accessed is not stored in the cache (i.e., a miss). If the operation is a read, the data fetched from main memory will overwrite the location causing the parity error (i.e., random replacement is overridden). The next time the same location is read, no parity error may be detected.

In some cases, therefore, a solid error may appear to be intermittent, while an intermittent error may appear to be more intermittent than it really is.

Another factor to consider when working on the PDP-11/70 is that some of the older device diagnostics have not been rewritten to incorporate parity error handlers. This means that whenever a parity error occurs, the program will halt with 120 in the address lights. (Trap through 114). This condition should be treated in the same manner as any other memory parity error.

The Cache registers and their use are summarized in the following paragraphs. A complete description of these registers and of their operation may be found in Section VI of the *KB11-B Processor Manual.*

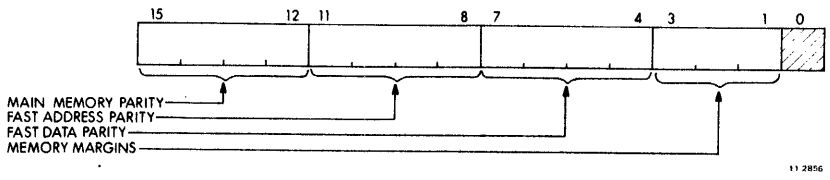
Hit/Miss Register 17 777 752



This register indicates whether the six most recent references by the CPU were hits or misses. A 1 indicates a read hit; a 0 indicates a read miss or a write. The lower numbered bits are for the more recent cycles.

All the bits are read only. The bits are undetermined after a power-up. They are not affected by a Console Start or a RESET instruction.

Maintenance Register 17 777 750



The Maintenance register is used mainly to check the parity checkers and generators in the PDP-11/70 memory system. Refer to the cache diagnostics for examples of the use of this register.

15-12: Main Memory Parity
Setting these bits causes the four parity bits to be 1s. This only causes an error if the byte(s) for which these bits are set to 1 contain an odd number of bits. There is 1 bit per byte; there are 4 bytes in the data block.

Bit Set	Byte
15	Odd word, high byte
14	Odd word, low byte
13	Even word, high byte
12	Even word, low byte

11-8: Fast Address Parity
Setting these bits causes the four parity bits for fast address memory to be wrong. This causes an error to be flagged immediately. Bits 11 and 10 affect group 1; bits 9 and 8 affect group 0.

7-4: Fast Data Parity
Setting these bits causes the four parity bits to be 1s. This only causes an error if the byte(s) for which these bits are set to 1 contain an odd number of bits.

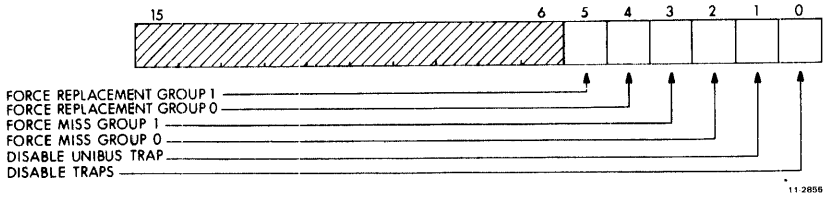
Bit Set	Byte
7	Group 1, high byte
6	Group 1, low byte
5	Group 0, high byte
4	Group 0, low byte

3-1: Memory Margins
These bits are encoded to perform maintenance checks on main memory.

	Bit 3	Bit 2	Bit 1	
0	0	0		Normal operation
0	0	1		Forces wrong address parity
0	1	0		Early strobe margin
0	1	1		Late strobe margin
1	0	0		Low current margin
1	0	1		High current margin
1	1	0		Reserved
1	1	1		Reserved

All main memory is margined simultaneously.

Control Register 17 777 746



The PDP-11/70 has the capability of running in a degraded mode if problems are detected in the cache. If group 0 of the cache is malfunctioning, it is possible to force all operations through group 1. If bits 2 and 5 of the Control register are set, and bits 3 and 4 are clear, the CPU will not be able to read data from group 0, and all main memory data replacements will occur within group 1. In this manner, half the cache will be operating, but system throughout will not decrease by 50 percent, since the statistics of read hit probability will still provide reasonably fast operation.

If group 1 is malfunctioning, bits 3 and 4 should be set, and bits 2 and 5 cleared so that only group 0 is operating. If all of the cache is malfunctioning, bits 2 and 3 should be set. The cache will be bypassed, and all references will be made directly to main memory.

Bits 1 and 0 can be set to disable trapping; more memory cycles will be performed, but overall system operation will produce correct results.

5-4: Force Replacement
Setting these bits forces data replacement within a group in the cache by main memory data on a read miss. Bit 5 selects group 1 for replacement; bit 4 selects group 0.

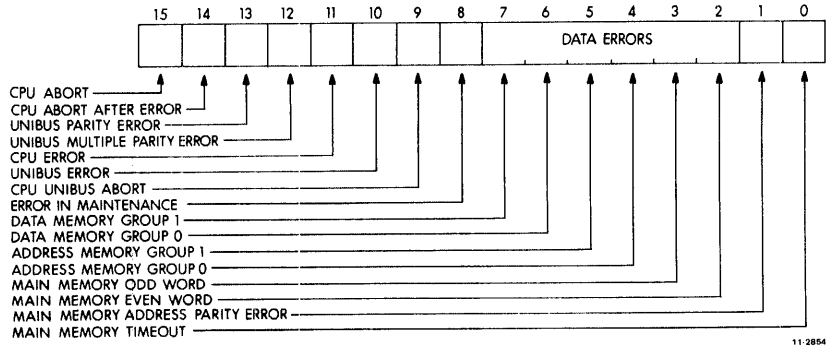
3-2: Force Miss
Setting these bits forces misses on reads to the cache. Bit 3 forces misses on group 1; bit 2 forces misses on group 0. Setting both bits forces all cycles to main memory and disables the cache.

1: Disable Unibus Trap
Set to disable traps to vector 114 when the parity error signal (PB=1, PA=0) is placed on the Unibus.

0: Disable Traps
Set to disable trap from non-fatal errors.

Bits 5 through 0 are read/write. The bits are cleared on Power-up or by Console Start.

Memory System Error Register 17 777 744



15: CPU Abort
Set if an error occurs that caused the cache to abort a processor cycle.

14: CPU Abort After Error
Set if an abort occurs with the Error Address register locked by a previous error.

If bit 14 (CPU abort after error) or bit 12 (Unibus multiple parity error) of the Memory System Error register is set, the address stored in the Low Error Address and High Error Address registers is the address of the first error and not the address at which the most recent error occurred. The address at which the most recent error occurred must be reconstructed from the contents of the SP (which points to the virtual address incremented by 2) and the appropriate memory management PAR.

The contents of the Memory System Error register and the High and Low Error Address registers indicates the failing section of the memory system.

13: Unibus Parity Error
Set if an error occurs that resulted in the Unibus Map asserting the parity error signal on the Unibus.

12: Unibus Multiple Parity Error
Set if an error occurs that caused the parity error to be asserted on the Unibus with the Error Address register locked by a previous error.

11: CPU Error
Set if any memory error occurs during a cache CPU cycle.

10: Unibus Error
Set if any memory errors occur during a cache cycle from the Unibus.

9: CPU Unibus Abort
Set if the processor traps to vector 114 because of Unibus parity error on a DATI or DATIP memory cycle.

8: Error in Maintenance
Set if an error occurs when any bit in the Maintenance register is set. The Maintenance register will then be cleared.

7-6: Data Memory
These bits are set if a parity error is detected in the fast data memory in the cache. Bit 7 is set if there is an error in group 1; bit 6 for group 0.

5-4: Address Memory
These bits are set if a parity error is detected in the address memory in the cache. Bit 5 is set if there is an error in group 1; bit 4 for group 0.

3-2: Main Memory
These bits are set if a parity error is detected on data from main memory. Bit 3 is set if there is an error in either byte of the odd word; bit 2 for the even word. (Main memory always transfers two words at a time.) An abort occurs if the error is in the word needed by a CPU reference. A trap occurs if the error is in the other word, or if it is a Unibus reference.

For example, if type MJ11-A (16K, core) memory is used in the system, and a main memory parity error bit is set in the Error register, all the information required to determine the failing 16K section of memory is present. The Low and High Error Address registers indicate the 32K section of memory in which the error occurred. The Error register indicates whether the error occurred on the odd or even addressed word. If, for instance, the error occurred in the odd addressed word, the 16K section containing odd addressed words should be replaced.

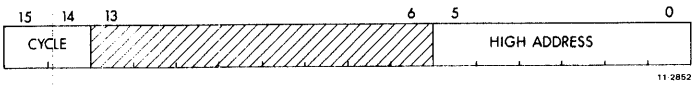
1: Main Memory Address Parity Error
Set if there is a parity error detected on the address and control lines on the main memory bus. If the main memory address parity bit is set, there may be a problem in the parity generator (Drawing ADMJ) or in a memory controller parity checker. A failure in the main memory bus address and control lines is the most likely cause for this error.

0: Main Memory Timeout
Set if there is no response from main memory. For CPU cycles, this error causes an abort. When a Unibus device requests a non-existent location, this bit will set, cause a time-out on the Unibus, and then cause the CPU to trap to vector 114. If the main memory time-out bit is set, the most probable cause is a memory controller failure. Another possible cause is a misconfiguration of the System Size register in the processor. (Refer to Paragraph 3.5.4.)

The bits are cleared on Power-up or by Console Start. They are unaffected by a RESET instruction.

When writing to the Memory System Error register, a bit is unchanged if a 0 is written to that bit, and it is cleared if a 1 is written to that bit. Thus, the register is cleared by writing the same data back to the register. This guarantees that if additional error bits were set between the read and the write, they will not be inadvertently cleared.

High Error Address Register 17 777 742



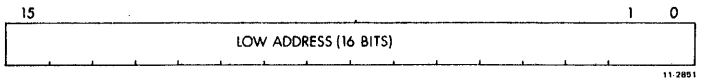
15-14: Cycle Type
These bits are used to encode the type of memory cycle that was being requested when the parity error occurred.

Bit 15	Bit 14	Cycle Type
0	1	Data In Pause
1	0	Data Out
1	1	Data Out Byte

5-0: Address
These bits contain the higher six of the 22-bit address of the first error. The most significant bit is bit 5.

All the bits are read only. The bits are undetermined after a power-up. They are not affected by a Console Start or RESET instruction.

Low Error Address Register 17 777 740



This register contains the lower 16 bits of the 22-bit address of the first error. The least significant bit is bit 0. The high order bits are contained in the High Error Address register.

All the bits are read only. The bits are undetermined after a Power-up. They are not affected by a Console Start or RESET instruction.

5.3.2 Indicators, Switches, Jumpers and Test Points

This paragraph describes the maintenance aids and the switches provided in the PDP-11/70.

5.3.2.1 SACK Timeout Indicator (UBCD) – If no response (SACK) is received from the Unibus 10 microseconds after a Unibus grant (NPG or BG) is issued, a SACK timeout is said to have occurred. This sets a flip-flop on UBCD, which turns on a LED indicator. The indicator stays on until the flip-flop is reset by INIT. Figure 5-5 in this maintenance manual shows the location of the LED. Refer to Section II, Paragraph 6.4, of the *KB11-B* or *KB11-C Processor Manual* (PDP-11/70).

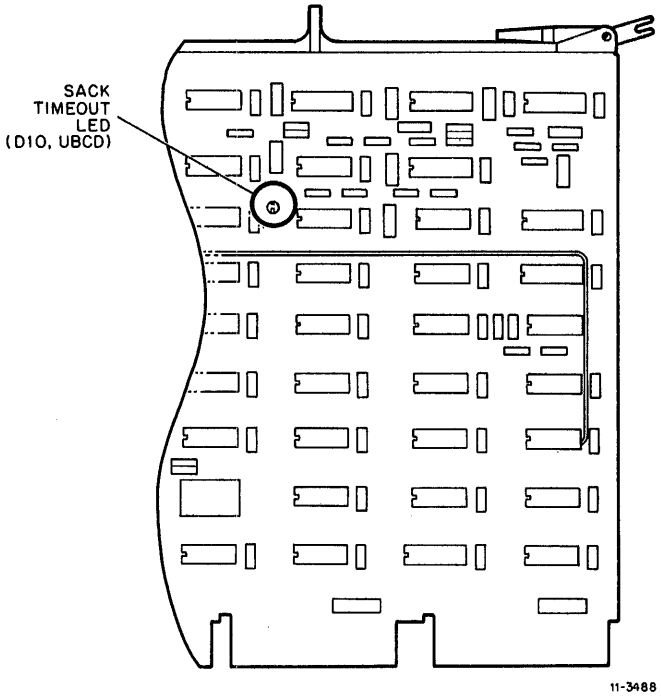


Figure 5-5 M8136 SACK Timeout LED

5.3.2.2 Start Vector (M8130-DAPE) – Jumpers W1 through W6, shown on DAPE, determine the start vector on power-up. The jumpers may be cut to provide a start vector between 00 000 000 and 00 000 174 (W6 OUT), or between 17 173 200 and 17 173 374 (W6 IN). Refer to Section II, Paragraph 2.1.9.4 of the *KB11-B* or *KB11-C Processor Manual* (PDP-11/70).

Bits 00 and 01 of the start vector are always 0. Bits 02:06 of the start vector are 0s if their respective jumpers (W1:W5) are OUT, and 1s if they are IN.

5.3.2.3 System Size Register (M8140-SCCN) – Refer to Paragraph 3.5.4, Figure 3-20, and Table 3-4 of this manual.

5.3.2.4 Massbus Controller Indicators and Jumpers

5.3.2.4.1 Indicators – The following light-emitting diodes are incorporated in the RH70 Massbus Controller logic BCT module (Figure 5-6) on the M8153.

SSYN (Slave Sync)	D-CS-M8153-0-1, Sheet 3 of 6
TRA (Transfer)	D-CS-M8153-0-1, Sheet 3 of 6
BG IN (Bus Grant In)	D-CS-M8153-0-1, Sheet 4 of 6
SACK (Selection Acknowledge)	D-CS-M8153-0-1, Sheet 4 of 6
BBSY (Bus Busy)	D-CS-M8153-0-1, Sheet 4 of 6

These LEDs are provided to aid maintenance personnel to isolate system faults as described below:

1. Unibus on PDP-11/70 is in "hung" condition (no operations can be performed on Unibus):

   a. Stuck SACK,
   b. Stuck BBSY, or
   c. Stuck SSYN

   The associated LED will be continuously illuminated. LEDs may flicker intermittently during normal operation.

2. The Unibus device interrupt sequence is not functioning properly (processor continuously loops in service routine and fails to execute instructions).

   This condition may be caused by discontinuity of the bus grant signal on the Unibus from the processor to the interrupting device and may be caused by missing grant continuity cards or effective circuitry which normally passes grant signals from device to device. This will cause the BG IN light-emitting diode to illuminate. If this LED is brightly illuminated, this indicates that the Unibus BG IN signal coming to that device is stuck high.

3. The processor attempts to read or write a Remote register in the RWS04 or RWS03 subsystem and receives an address error indication on the console (CPU traps to location 4).

   This condition may be caused by a stuck TRA signal on the Massbus which prevents the SSYN resonse frm the RH70.

   Determination of this condition may be made if local registers in the RH70 can be successfully accessed. If no register responds, the address jumpers may be improperly selected.

RH70 Jumpers

Address Selection Jumper (BCTA)	Address Bit	Device		
		RWS04 (14 REG)	RWP04 (22 REG)	TWU16 (16 REG)
W14	12	OUT	OUT	OUT
W10	11	IN	OUT	IN
W9	10	OUT	OUT	OUT
W8	9	IN	IN	IN
W11	8	IN	OUT	OUT
W13	7	IN	OUT	IN
W15	6	IN	OUT	IN
W12	5	OUT	IN	OUT
Slot E41 Jumper (BCTA)	**Binary Weight**			
(ADRS. Bit 5)				
1–16	—	IN	OUT	IN
2–25	—	IN	OUT	IN
3–14	—	OUT	IN	OUT
4–13	—	OUT	IN	OUT
(No. of Regs.)				
5–12	2	IN	IN	OUT
6–11	4	OUT	OUT	OUT
7–10	8	OUT	IN	out
8–9	16	IN	OUT	IN
Vector Jumper (BCTC)	**Vector Bit**			
W4	V8	OUT	OUT	OUT
W1	V7	IN	IN	IN
W5	V6	OUT	OUT	OUT
W2	V5	OUT	IN	OUT
W6	V4	OUT	OUT	IN
W3	V3	OUT	IN	OUT
W7	V2	IN	IN	IN

Figure 5-6 M8153 (BCT) Module (Sheet 1 of 2)

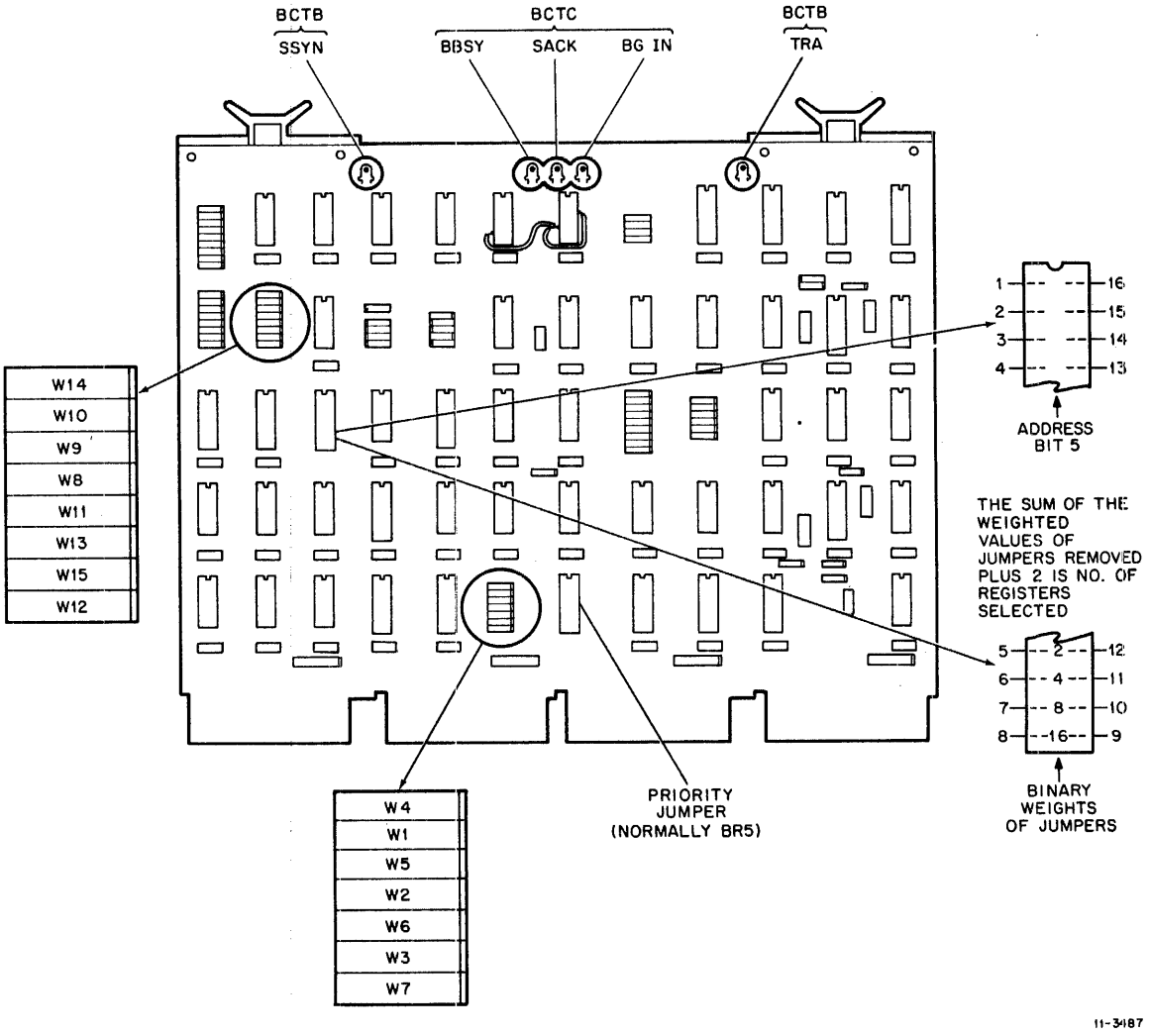


Figure 5-6 M8153 (BCT) Module (Sheet 2 of 2)

5.3.2.4.2 Jumper Configurations – The following paragraphs describe the various jumper configurations on the BCT (M8153), MDP (M8150), and CDP (M8145) modules.

BCT Module M8153
The BCT module contains jumpers for register selection, BR level interrupt, and vector address. Refer to Figure 5-6, which shows both jumper location and configurations.

Register Selection – The RH70 is capable of responding to 32 possible Unibus addresses. The number of addresses, however, is dependent on the Massbus device. Jumpers W8 through W15 select the block of Unibus addresses that the subsystem responds to. The standard addressing blocks assigned are as follows:

RWS04: 772 040 through 772 072
RWP04: 776 700 through 776 752
TWU16: 772 440 through 772 476

BR Level Interrupt – The priority jumper plug for the RH70 is normally set for the BR5 level. This plug is located in E022 (refer to D-CS-M8153-0-1, sheet 4 of 6).

Vector Address Jumpers – The interrupt vector transferred to the processor is jumper selectable via jumpers W1 through W7, representing vector bits 2 through 8. Vector assignments for the RH70 devices are the following:

RWS04: 204
RWP04: 254
TWU16: 224

MDP Module M8150
The MDP module contains jumpers that allow troubleshooting of the write-check error circuitry (Figure 5-7). These jumpers allow maintenance personnel to disconnect wired-OR connections from the exclusive-OR network used to detect write-check errors. These jumpers are designated W1 through W4 and are shown on MDPE. The jumpers provide maintenance personnel with a method of isolating a faulty output (stuck low) of the wired-OR bus to one of four integrated circuit (IC) chips which perform the exclusive-OR function during write-check operations. Fox example, if the output of E21 and E23 open-collector line is stuck low when scoping of the inputs indicate that it should be high, the faulty IC (E21 or E23) can be ascertained by removing jumpers W2 and W1. If, after removing the jumpers, the outputs of the exclusive-OR gates in E23 are still low, it indicates that the E23 chip is defective. If E23 outputs are high, then the E21 chip is defective (outputs stuck low).

CDP Module M8145
Jumpers W1, W2, and W3 determine the priority arbitration of the RH70 Massbus controllers. A complete description of the arbitration process is given in Section VI, Paragraph 4.6 of the *KB11-B Processor Manual* (PDP-11/70). The most common configuration is that which allocates priority to the controllers in the following order:

1. A (slots 24–27)
2. B (slots 28–31)
3. C (slots 32–35)
4. D (slots 36–39)

In this case, jumpers W1, W2, and W3 are all IN.

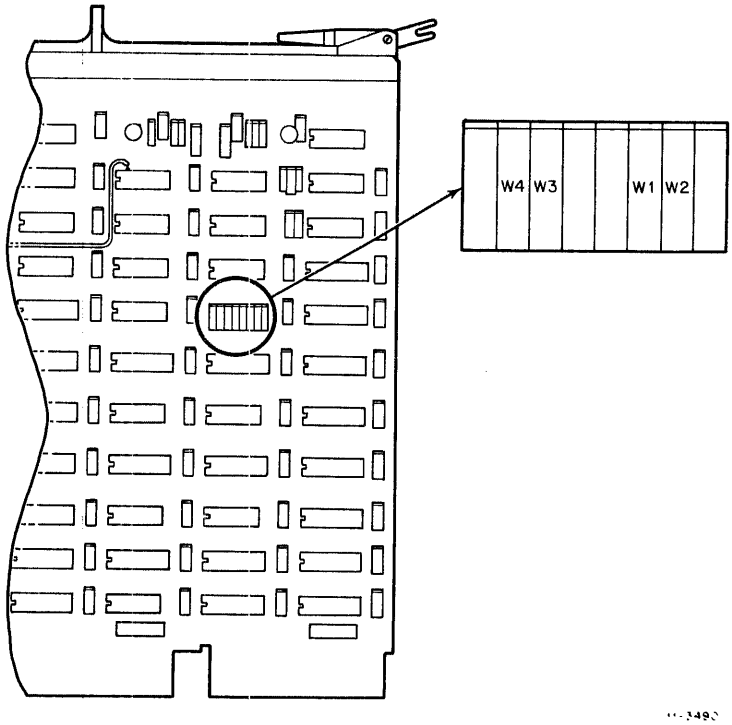


Figure 5-7 MDP Module - M8150

5.3.2.5 Main Memory (MK11) Maintenance Aids - Maintenance aids provided in the MK11 MOS memory include: control and status register (CSR), fault indicator lights on the memory frame modules, and indicator lights on the box controller. The format of the two word CSR is shown in Figure 5-8. The address of the CSR is indicated in the memory box decal (refer to Chapter 3, Figure 3-29). The CSR can be written to and read from the processor console, or through a terminal while running the memory system diagnostic program, CEMKAA.

The CSR can be accessed from the processor console in the following manner:

1. Halt all NPR activity in system.
2. Turn off cache 17777746 ← 14.
3. Set up map 0 17770200 ← 170000
   17770202 ← 77.
4. Turn on Unibus map 17772516 ← 40.
5. Turn display switch to CONSOLE PHYSICAL.
6. Examine and/or deposit SCRs as addresses 17002100 through 17002136 (address is indicated on the memory box decal).

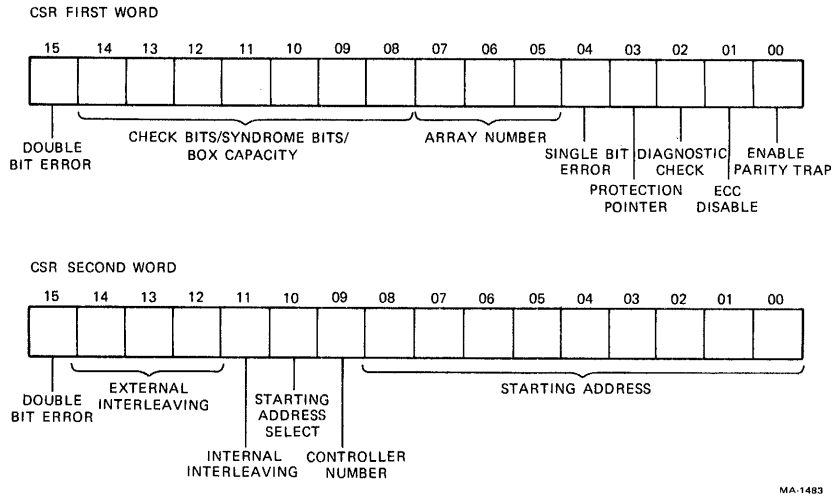


Figure 5-8 MK11 Control and Status Register

While running the memory system diagnostic program, the CSR can be accessed by entering the field service mode (control F) and typing command 1 to read the CSR or typing command 2 to load data into the CSR. Refer to the *MK11 MOS Memory Technical Manual* for a description of running the memory diagnostic.

CSR Bits - First Word

Bit 15 - Double Bit Error - When set to one, this bit indicates a double bit (uncorrectable) error was found in a 32-bit double word fetched from an array. The array number and controller number indicating the location of the error will be loaded into the CSR.

Bits (14:8) - Check Bits - In a diagnostic mode [bits (3:1) = 010] check bits can be written to and read from the check bit storage field on the array modules.

Bits (14:8) - Syndrome Bits - Bits 14 through 8 store the ECC syndrome bits when the ECC circuitry encounters a single bit error.

Bits (14:8) - Box Capacity - By writing a 100 into bits (3:1), the box capacity in 32K word blocks can then be read from bits (14:8).

Bits (7:5) - Array Number - These bits indicate the array that contained the single bit or double bit error flagged by bit 4 or bit 15.

Bit 4 - Single Bit Error - When set to one, this bit indicates that a single bit (correctable) error was found in a 32 bit double word fetched from an array. The array number, controller number, and syndrome bits will be loaded into the CSR.

Bit 3 - Protection Pointer - For diagnostic purposes, this bit selects which 32K word bank of memory is protected memory space. When zero, this bit indicates that the first 32K bank of each controller is protected. When one, this bit indicates that the second 32K bank of each controller is protected.

Bit 2 – Diagnostic Check – When set to one, this bit allows the reading and writing of check bits via SCR bits 14 through 8.

Bit 1 – ECC Disable – When set to one, this bit disables single bit error correction in all unprotected memory space.

Bit 0 – Enable Parity Trap – When one, enables parity traps. Memory will force bad parity on Main Memory Bus if ECC circuitry encounters an uncorrectable error.

CSR Bits – Second Word
Bit 15 – Double Bit Error – Same as CSR first word bit 15.

Bits (14:12) – External Interleaving – These bits indicate the number of ways the memory is externally interleaved. The interleave number from the box controller interleave switch is loaded into bits (14:12) at power up. See bit 10.

Bit 11 – Internal Interleaving – When one, this bit indicates that the memory is internally interleaved. Bit is set to one at power up if memory arrays in frame are balanced. When zero, this bit indicates that there is no internal interleaving. See bit 10.

Bit 10 – Starting Address Select – When zero, this bit selects the switches on the box controller as the source of the starting address and number of ways externally interleaved. When set to one, the bit allows writing SCR bits 14:12, 11, and 8:0 to select the external interleaving, internal interleaving, and starting address. To write these bits, the Address/Interleave switch on the box controller must be in the ALLOW PROG CONTROL position.

Bit 9 – Controller Number – This bit, along with first word bits (7:5), indicate the array that contained the single bit or double bit error flagged by first word bit 4 or bit 15. A zero is for controller pair zero (right side of frame); a one is for controller pair one (left side).

Bits (8:0) – Starting Address – These bits indicate the starting address of the memory frame in 32K word banks. The starting address from the box controller thumbwheel switches is loaded into bits (8:0) at power up. See bit 10.

Memory Frame Indicator Lights – Fault indicator lights (LEDs) in the memory frame are shown in Figure 5-9. These lights are mounted near the edge of address interface (M8158), data buffer (M8159), and control B (M8160) modules; they are visible through the opening at the front of the memory frame.

Address Parity Error Indicator – Lights when the memory receives incorrect address parity on the main memory bus. Indicator stays lit until the memory is powered down.

Configuration Error Indicator – Lights if MOS array modules are improperly installed in memory frame.

Double Bit Error Indicator – Lights when the error detection circuitry encounters an uncorrectable (double bit) error in the data during a read operation.

Memory Busy Indicator – Lights while memory controller is executing a memory cycle (read, write, refresh). Brightness of light indicates the rate at which the memory is accessed. Light glows dimly while controller is refreshing memory only. When off, light indicates that the controller is not functioning.

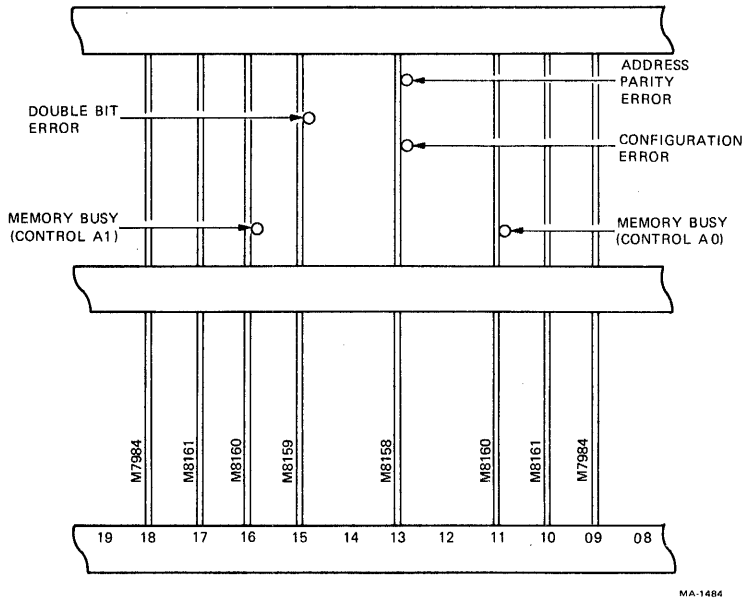


Figure 5-9 MK11 Memory Frame Error Indicators

Box Controller Indicator Lights – The box controller, shown in Figure 5-10, mounts in a controller panel near the top of the memory cabinet. It contains the following indicator lights.

Panel Selected – When lit, light indicates that the Address/Interleave switch is in the FORCE PANEL position and that the thumbwheel switches determine the starting address and interleaving. CSR second word bit 10 is held at zero.

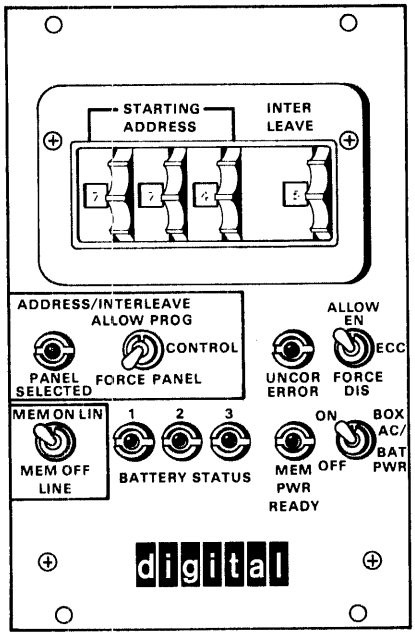
Uncor Error – When lit, light indicates that a double bit error was detected in memory. See CSR bit 15.

Battery Status – These lights indicate the operating status of the three battery backup units.

ON	– Battery receiving trickle charge
Fast Flash	– Battery delivering power to memory
Slow Flash	– Battery receiving full rate charge.
OFF	– Battery off or disconnected

MEM PWR Ready – When lit, light indicates that the power supply voltages are within tolerance. When off, light indicates that either main dc low or box dc low are asserted.

5.3.2.6 Main Memory (MJ11) Maintenance Aids – Refer to Figure 5-8, which shows the module layout (Rev C) of the M8148 module. This module contains all the logic indicators, test points and switches for an MJ11 frame. Seven power test points are provided on the M8149 module. Refer to Paragraph 4.5.2 of this manual.



MA-1420

Figure 5-10 Box Controller

The use of switches S1 and S2 is described in Paragraph 3.5.1 of this manual.

The following paragraphs describe the use of the indicators and test points. For additional maintenance information, refer to the *MJ11 Memory System Maintenance Manual,* EK-MJ11-MM.

Address and Control Parity Error Indicator and TP2 – MCTA WRONG PARITY is asserted when a memory controller detects bad parity on the A and C lines, at the time that it receives START. In this case, the controller does not respond to START and a memory bus time-out occurs. This in turn causes the memory cycle to be aborted. The Parity Error flip-flop is set, asserting MCTA PAR ERR (1) L. This asserts MAIN PAR ERR L on the main memory bus.

MCTA PAR ERR (1) L sets a flip-flop that lights the Parity Error LED indicator, which is visible from the front of the memory mounting box (Figure 5-11). The flip-flop is cleared on Power-up (MCTH RESET L asserted), or by grounding test point TP2 on the M8147/M8148 module.

TP1 – When grounded, TP1 causes the memory controller to cycle continuously. A console LOAD ADRS followed by a DEPOSIT or an EXAMINE would cause the read/write operation to be repeated until the ground is removed from TP1.

CAUTION

Do not power up memory system with TP1 grounded. To do so may cause failure of stack charge circuitry on H217C stacks controlled by this controller. Refer to the MJ11 Maintenance Manual for diagnostic procedures and proper use of TP1.

Mismatch Error Indicators – The MJ11 Memory Controller is designed to operate with different types of stack module sets (16K→MJ11-A, 32K→MJ11-B). The different types of stack modules have different control and timing requirements. The circuitry at the top center of Drawing MCTC determines whether the 16K block being addressed resides in a 16K or 32K stack. If a 16K stack is being addressed, the 16K flip-flop is clocked set when MCTF IACK H is asserted (i.e., when the memory controller initiates the memory cycle), thereby asserting MCTC 16K (B) H.

Stacks that operate in parallel must be of the same type. The eight Exclusive-OR gates on Drawing MCTC check that the stack module set pairs are properly matched. If a mismatch is detected, MCTC MISER L is asserted; this asserts MTB GO DISABLE H, which inhibits initiation of memory cycles by the memory controller. MCTC MISER L asserted also lights the Mismatch Error LED, which is visible from the front of the memory frame (Figure 5-11).

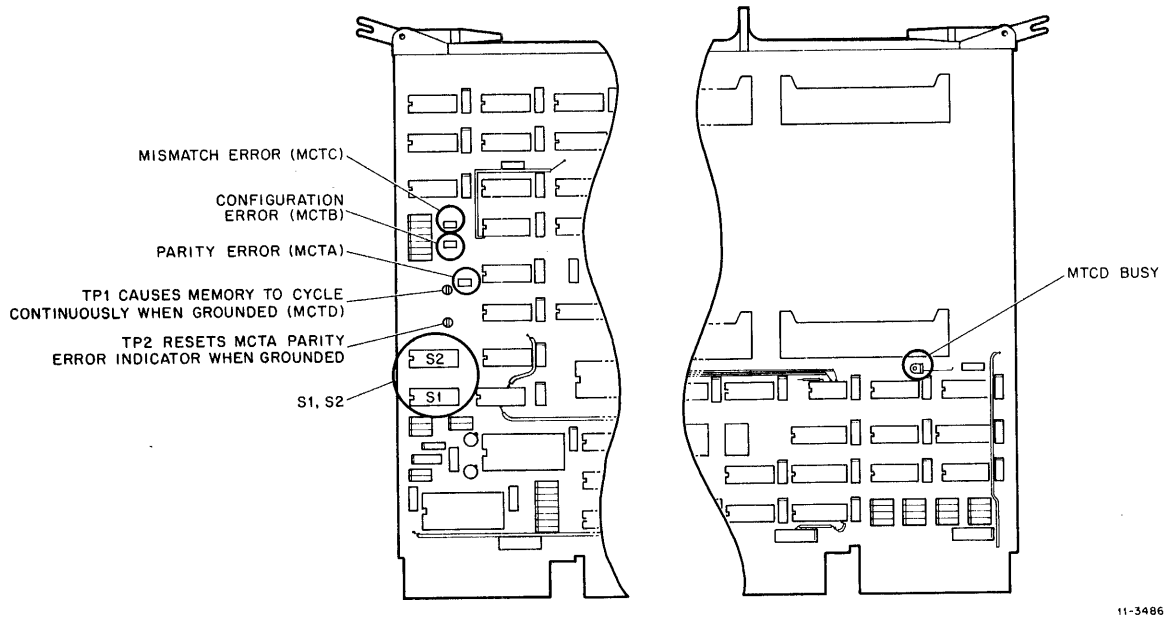


Figure 5-11 M8148 (MCT) Module

Configuration Error Indicator (Upper Limit Comparison) – Signals MCTB 16K BLK ADDR 2:0 H, which represent the effective 16K block address, are applied to the A inputs of the Upper Limit Compare ALU. The B inputs of the ALU are provided by the Memory Top Look-Up ROM. This ROM decodes the ID signals from the stack module sets installed in the memory frame and generates outputs that indicate the number of 16K blocks available to the memory controller. The Upper Limit Compare ALU output MCTB ABOVE TOP L is asserted if the effective 16K block address being accessed is greater than the number of 16K blocks available to the memory controller. If MCTB ABOVE TOP is asserted, MCTB GO DISABLE H is asserted, thereby inhibiting initiation of a memory cycle.

The Memory Top Look-Up ROM also checks for correct configuration of the stack module sets. A configuration error asserts MCTB CONER L, which asserts MCTB GO DISABLE, inhibiting all memory cycles by the memory controller. MCTB CONER L lights the LED which is visible from the front of the memory frame (Figure 5-11).

Busy Indicator – MCTD DELAY L starts the read timing sequence by turning on transistor Q1. This shunts the +5 V at the collector of Q1 to the input of a delay line, sending a positive pulse down the line. Taps along the delay line are located at 25 ns intervals and are labeled accordingly. The leading edge of the pulse asserts MCTD RDLY 0 H through MCTD RDLY 350 H as it travels down the delay line. MCTD RDLY 350 H is fed back and turns transistor Q1 off, thereby terminating the positive pulse. The width of the pulse traveling down the delay line is thus fixed at 350 ns. This means that the outputs at all the delay line taps are also 350 ns pulses. The signals output from the delay line are buffered by type 74S04 inverters to provide clean TTL-compatible signals with sufficient drive. The buffered outputs of the delay line are MCTD RT 0 through MCTD RT 350. MCTD RD 0 L direct sets the Busy flip-flop, which inhibits the memory controller from initiating memory cycles while the present cycle is in progress. The BUSY LED indicator (Figure 5-11) is set by the Busy flip-flop.

5.3.2.7 Unibus Map Response Switches (M8141-MAPF) – Jumpers W1 and W3–W6 (MAPF HIXX JUMPER H) determine the upper limit of responding Mapping registers to be compared with the Unibus address.

Jumpers W2 and W7–W10 (MAPF LOXX JUMPER H), are the lower limit of responding Mapping registers to be compared with the Unibus address.

In standard configurations, the HIXX jumpers are all 1s, and W1, W3–W6 are OUT; the LOXX jumpers are all 0s, and W2, W7–W10 are IN. This allows the Unibus Map to accept Unibus addresses 000 000 through 757 777.

Table 5-4 shows the limits that can be obtained by the jumper configurations. Note that if the HI jumpers are all 0s (IN), or if the LO jumpers are all 1s (OUT), no response can be obtained from the Unibus Map.

5.3.2.8 AC LO and DC LO Indicator – The Power Line Monitor/15 V Regulator Module (D-CS-5411086) contains two LED indicators which are ON when AC LO or DC LO are not asserted (=power OK).

In the MJ11, they may be observed through the ventilation slots in the AC input box. In the CPU cabinet, the H7420 power supply must be opened to observe these indicators. Refer to Paragraphs 4.5.2 (MJ11) and 4.5.3 (H7420) of this manual.

WARNING
Power must be shut off by turning the console key to OFF before assembling or disassembling the H7420.

Figure 5-12 shows the location of these indicators on the 5411086 module.

Table 5-4 Unibus Map Limit Jumpers (MAPF)

MAPF HI (17:13) JUMPER H (OCTAL)	Highest Possible Unibus Address	MAPF LO (17:13) JUMPER H (OCTAL)	Lowest Possible Unibus Address
37	757 777	37	None
36	737 777	36	740 000
35	717 777	35	720 000
34	677 777	34	700 000
33	657 777	33	660 000
32	637 777	32	640 000
31	617 777	31	620 000
30	577 777	30	600 000
27	557 777	27	560 000
26	537 777	26	540 000
25	517 777	25	520 000
24	477 777	24	500 000
23	457 777	23	460 000
22	437 777	22	440 000
21	417 777	21	420 000
20	377 777	20	400 000
17	357 777	17	360 000
16	337 777	16	340 000
15	317 777	15	320 000
14	277 777	14	300 000
13	257 777	13	260 000
12	237 777	12	240 000
11	217 777	11	220 000
10	177 777	10	200 000
07	157 777	07	160 000
06	137 777	06	140 000
05	117 777	05	120 000
04	077 777	04	100 000
03	057 777	03	060 000
02	037 777	02	040 000
01	017 777	01	020 000
00	None	00	000 000

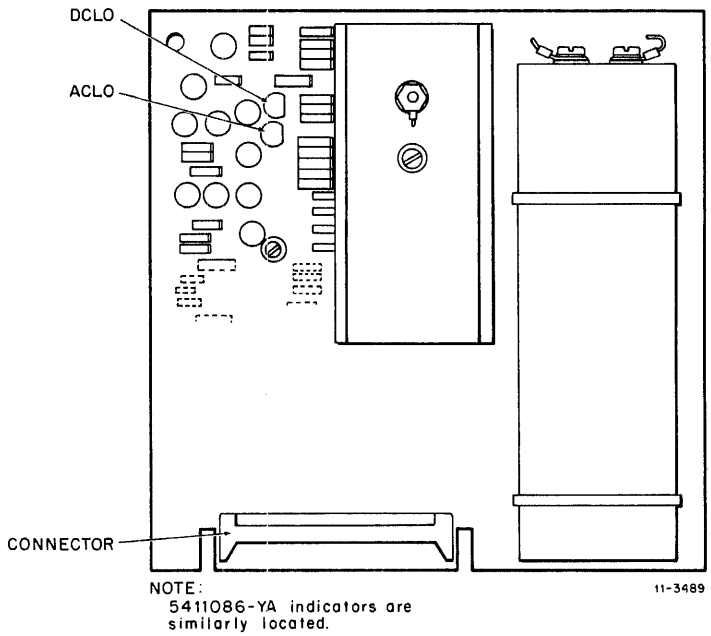


Figure 5-12 5411086 AC LO and DC LO Indicators

5.3.2.9 Sync Points – The microaddress in the Microprogram Break register (17 777 770) generates a sync pulse (TIGB PB SYNCH H) at T1 at pin F13K2 each time the cycle corresponding to the address is executed. PDRC PB CMP H generates a pulse whose width is the same as that of the microstate (pin A10E1).

5.3.3 How to Use Maintenance Cards

The maintenance card that is used to perform maintenance tests and troubleshooting procedures on the PDP-11/70 system is shown in Figure 5-13. The maintenance card is constructed from a W131 Maintenance module. The W131 is used with a W133 Driver module. Figure 5-11 shows the overlay that is used to designate switches and indicators for KB11-B, C and FP11-B test functions.

NOTE

The maintenance card is not used with the FP11-C, since it operates synchronously with the processor and has no RC clock.

The indicator lamp functions and the sources of the inputs from the KB11-B, C and FP11-B follow:

Indicator	Source		Signal Description
	KB11-B,C	FP11-B	
TPH	TIGA TPH MAT H	FRHJ MSTEP CLOCK (0) H	KB111-B,C: Basic processor timing pulse, whether crystal clock, RC clock, or MAINT STPR is selected. FP11-B: Indicates MAINT STPR clock pulse.
T1 through T5	TIGA (T1:T5) MAT H	FRHH (T1S:T4S) H	Indicate major time states for KB11-B,C and FP11-B. T5 is not used for FP11-B.
BUST	UBCE BUST MAT H	UBCE BUST MAT H	KB11-B,C bust cycle. Not asserted by FP11-B.
MEM	TIGA MEM SYNC H	TIGA MEM SNC H	Indicates the completion of a memory cycle. Asserted by CCBC MEM SYNC H.
AF2/BF2 AH2/BH2	No connection No connection	No connection No connection	Spare indicators. Inputs at pins F2 or H2.
SLOW CYCLE	CCBD SLOW CYCLE MAT H	CCBD SLOW CYCLE MAT H	Indicates that the memory cycle referenced main memory.
BBSY	UBCA BBSY MAT H	UBCA BBSY MAT H	Indicates Unibus is busy.

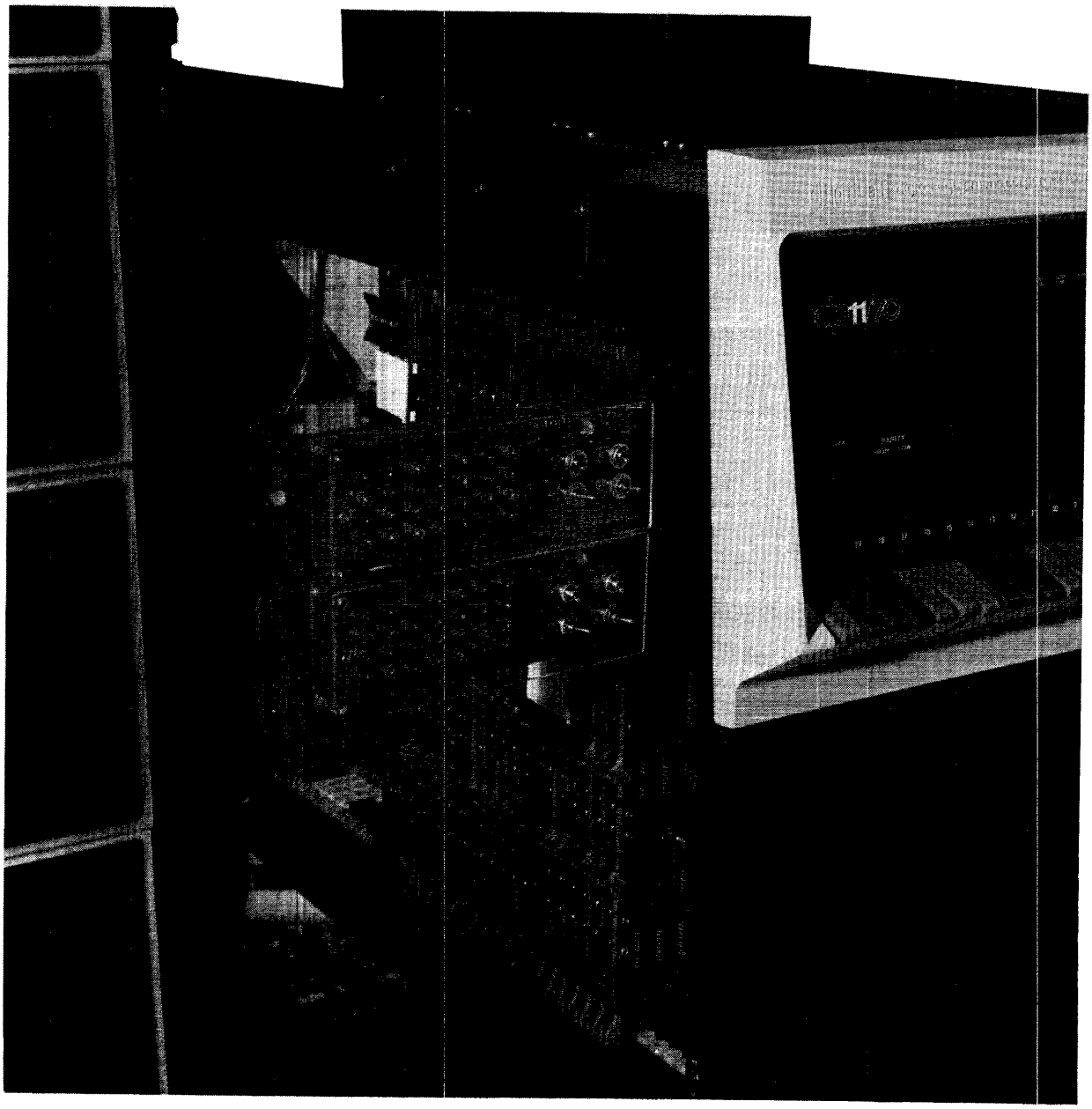
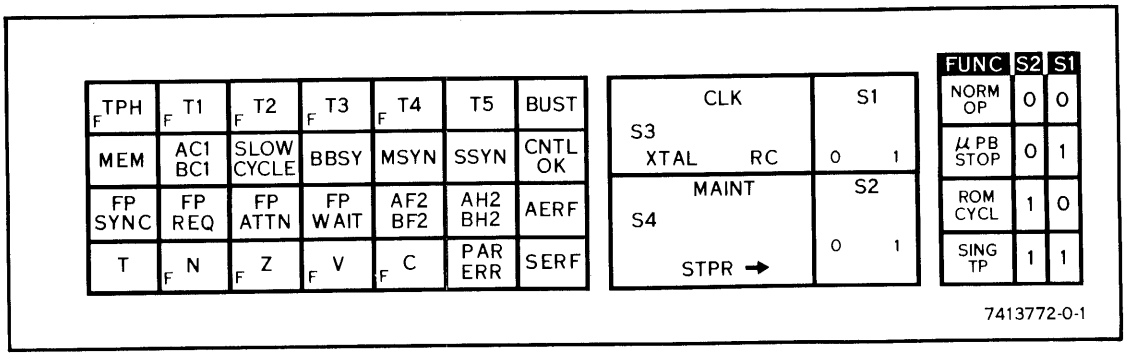


Figure 5-13 Maintenance Cards: for FP11-B (Top) and for KB11-B,C (Bottom)



11-3288

Figure 5-14 Maintenance Card Overlay

Indicator	Source		Signal Description
	KB11-B,C	FP11-B	
MSYN	MAPB MSYN B MAT H	MAPB MSYN B MAT H	Indicates Unibus Master Sync is asserted.
SSYN	UBCB SSYN MAT H	UBCB SSYN MAT H	Indicates Unibus Slave Sync is asserted.
CNTL OK	TMCE CONTROL OK H	TMCE CONTROL OK H	Asserted by processor to allow memory cycle to be completed.
FP SYNC	UBCD FP SYNC H	UBCD FP SYNC H	Indicates that the FP11-B is ready to send or receive data. Asserted by FRMJ FP SYNC L.
FP REQ	RACK FP REQ H	RACK FP REQ H	Used with FP SYNC to indicate to CPU that more data words are required. If FP SYNC is returned to CPU without FP REQ, the memory cycles are terminated.
FP ATTN	UBCD FP ATTN H	UBCD FP ATTN H	Decoded from CPU ROM states where MSC = 5, indicating floating-point instruction has been decoded.
FP WAIT	FRHH WAITS H	FRHH WAITS H	Represents the Wait state of the FP11-B.

Indicator	Source		Signal Description
	KB11-B,C	FP11-B	
AC1/BC1	No connection	No connection	Spare indicator, input at pin C1.
AERF	TMCC AERF MAT H	TMCC AERF MAT H	Indicates state of KB11-B,C Address Error Flag.
SERF	TMCC SERF MAT H	TMCC SERF MAT H	Indicates state of KB11-B,C Stack Error Flag.
PAR ERR	UBCB PARITY ERR MAT H	UBCB PARITY ERR MAT H	Indicates Unibus or memory has detected a parity error.
T	TMCB PS04 MAT H	TMCB PS04 MAT H	Indicates processor status word trace bit is set.
N	IRCH MAT N H	FRLP FN (1) H	KB11-B,C: N (negative) bit of the CPU Processor Status Word condition code. FP11-B: N bit of the FPP Program Status register.
Z	IRCH MAT Z H	FRLP FZ (1) H	KB11-B,C: Z (zero) bit of the CPU Processor Status Word condition code. FP11-B: Z bit of the FPP Program Status register.
V	IRCH MAT V H	FRLP FV (1) H	KB11-B,C: V (overflow) bit of the CPU Processor Status Word condition code. FP11-B: V bit of the FPP Program Status register.
C	IRCH MAT C H	FRLP FC (1) H	KB11-B,C: C (carry) bit of the CPU Processor Status Word condition code. FP11-B: C bit of the FPP Program Status register.

5.3.3.1 Clock Selection – CLK switch S3 is used to select the crystal clock (XTAL), the RC maintenance clock (RC), or the MAINT STPR switch as the timing source for the CPU or FP11-B. CPU timing and FP11-B timing are independent; thus, the switches on each maintenance card need not be set for the same selection when two cards are used.

When set to XTAL, the 33.3 MHz crystal clock is selected for the CPU timing source and the 18 MHz crystal clock is selected for the FP11-B. When the CLK switch is set to RC, the variable frequency RC maintenance clock is selected as the timing source. By adjusting the potentiometer, the useful range of the period of the RC maintenance clock pulse can be adjusted as follows:

KB11-B,C RC Clock: 28 to 50 ns
FP11-B RC Clock: 50 to 290 ns

NOTE

When using both CPU and FP11-B RC clocks, half of the FP11-B clock period must be shorter than two CPU ROM cycles. The FP11-C does not have a variable RC clock.

5.3.3.2 Maintenance Mode Control – Maintenance card switches S2 and S1 are used to select the Maintenance mode, as indicated below:

S2	S1	Mode	Operation
0	0	NRM OP	No effect on KB11-B,C or FP11-B operation.
0	1	μPB STOP	The KB11-B,C or FP11-B will execute instructions until the microprogram ROM address matches the contents of the Program Break (PB) register. It halts at T2 of that ROM state.
1	0	ROM CYCL	The KB11-B,C or FP11-B will execute a single ROM state each time the MAINT STPR is pressed.
1	1	SING TP	The basic clock changes state each time the MAINT STPR is pressed. Pressing MAINT STPR twice provides a single time pulse.

Single ROM Cycle – When Switches S1 and S2 are set for single ROM Cycle mode, the processor executes a single ROM cycle each time the console CONT switch is pressed. For convenience, MAINT STPR switch S4 on the maintenance card can also be used to initiate the single ROM cycle. In this mode of maintenance operation, the processor stops in T2 of each microstate.

MPB STOP – If CONT is pressed when switches S1 and S2 are set for PB (microprogram break) Stop mode, the KB11-B,C or FP11-B execute program instructions until the ROM Address register contents match the CPU Program Break (PB) register contents. When both microstate addresses are equal, the processor stops in T2 of the selected microstate. At that point, S1 and S2 can be set for SING TP mode as described in Paragraph 5.3.3.3. Load the PB with the desired microprogram address as follows:

1. Press HALT switch. Processor halts at microprogram CON.00 (CPU μADRS 170).
2. Set PB register address 17 777 770 into console Switch register.
3. Press LOAD ADRS. ADDRESS: Display will be 17 777 770.
4. Set desired microprogram break address into the low byte of the Switch register. For example, to stop at IRD.00, set 343(8) into the Switch register.

5. Press DEP. The DATA display will display this input in the low order byte with the Data Display Select switch set to DATA PATHS.

6. Set Maintenance module switches for PB STOP (S1=1, S2=0).

7. Press CONT. The processor executes program instructions until the RAR equals the PB, then stops.

Single Step – When switches S1 and S2 are set for SING TP mode, gating logic shown on drawing TIGB inhibits the source synchronizer from selecting either the crystal clock or the RC maintenance clock. Under these conditions, each time MAINT STPR switch S4 is pressed, TP H changes levels.

NOTE

MAINT STPR must be pressed twice to complete each time pulse. This feature allows events that occur on the leading edge or trailing edge of the same time pulse to be examined separately.

5.3.3.3 Using the Maintenance Card with KB11-B,C – Section II, Chapter 1 of the KB11-C and KB11-B Processor Manuals explains how to use the processor flow diagrams; an instruction example is also provided to familiarize the reader with the sequence of machine states used to execute a typical instruction. The same compare instruction example is used to demonstrate how to use the maintenance card for test purposes. Section II, Chapter 4 of the KB11-C and KB11-B Processor Manuals describes the maintenance board control logic on the M8139 module (TIG). Section III of the same manual explains the console logic in detail.

Deposit Test Intruction – Set the Address Display Select switch to CONS PHY, load address 1000, and deposit the following:

Address	Data	Comments
1000	022767	Compare instruction
1002	000015	Source operand immediate
1004	000100	Destination operand indexed
•		
•		
1106	000000	Word = 0

μPB Stop Mode

1. Set up the PB for a PB STOP at IRD.00 (CPU ADRS 343).
2. Load address 1000(8).
3. Set maintenance card switches S1 and S2 for PB STOP mode. (S1=1, S2=0)
4. Set ENABLE/HALT to ENABL and press START.

The processor stops at Ird.00 (343), in T2. The table below shows normal console indications as a result of these events.

Console Display		Contents (octal)
ADDRESS:	CON PHYS	1002
DATA:	DATA PATHS	1002
	BUS REGISTER	022767
	μADRS FPP/CPU	343*
PAUSE		

Maintenance card indicator T2 lights.

*In Low order byte.

Single ROM Cycle Mode – This setup causes the processor to execute one ROM cycle of the test instruction and stop in timestate 2 each time MAINT STPR switch S4 is toggled.

1. Set Maintenance Card switches S1 and S2 for single ROM Cycle mode. (S1=0, S2=1).
2. Press Maintenance Card MAINT STPR switch S4 or CONT switch on the console.

The table below lists normal ADDRESS and DATA displays resulting from each ROM cycle execution, starting with IRD.00, T2 of the example test intruction.

ROM μstate	Console Display			
	μADDRS CPU	Data Path	Bus Register	Address CON PHYS
IRD.00	343	1002	022767	1002
S13.00	021	1004	022767	1002 (BUST)**
S13.10	027	1004	022767	1002 (CNTL OK)**
D67.80	117	15	15	1004 (BUST)**
D67.00	006	1006	15	1004 (CNTL OK)**
D67.10	251	1106	100	1004
D10.30	122	15	100	1106 (BUST)**
D10.60	177	15	15	1106 (CNTL OK)**
TST.10	033	177762*	0	1006

*1's complement of 15(8).
**Maintenance Module Indicators

SING TP MODE – This procedure allows the maintenance card user to step through microstates of the test instructions example in the SING TP mode.

1. Set S1 and S2 to.
2. Set ENABL/HALT to HALT and press START.
3. Load the example instruction address 1000.
4. Set Maintenance Card switches S1 and S2 to μPB STOP mode. (S1=1, S2=1).
5. Set ENABL/HALT to ENABL and press START.

When the processor stops at T2 of FET.10 (CPU μADRS 260), set S1 and S2 to select SING TP mode. Then press MAINT STPR switch S4 twice to step through each time state.

NOTE

The T1 through T5 indicators on the Maintenance module are driven by the T1–T5 flip-flops on TIGA. Thus, a time pulse is only asserted when both its associated indicator and the TP H indicator are on.

5.4 PDP-11/70 DIAGNOSTICS

The principal PDP-11/70 diagnostic programs are briefly described in this paragraph.

NOTE

1. During an installation, the stand alone diagnostics described in Paragraphs 5.4.2–5.4.5 and 5.4.8 and 5.4.9 should all be run immediately after loading XXDP (Figure 3-9).

2. During a service call in which the failure is not obvious, the Subsystem Diagnostic (Paragraph 5.4.7) should be run; this program will then point to the stand-alone diagnostic(s) related to the area of the system that is failing (Figure 5-1).

5.4.1 PDP-11/70 XXDP

XXDP is a catch-all name for a group of binary packages available for loading devices listed in Figure 3-9.

All XXDP packages require a console device (teletype, LA36, VT05), and one of the diagnostic package media.

The above requirements are for loading and running diagnostic programs already stored in one of the diagnostic package media. They are also sufficient for implementing permanent patches on programs when required.

The XXDP monitor is loaded via the M9301-YC bootstrap module.

Complete documentation is contained in the XXDP user manual, MAINDEC-11-DZQXA. A programming card, MAINDEC-11-DZZPA is also available.

Disclaimers – The XXDP packages have been designed for diagnostic purposes only. The software used is not intended to be compatible with any other PDP-11 family software, any non-diagnostic uses of the software, or uses of the software in other than the manner described in the XXDP user manual are not supported.

The XXDP packages are binary packages only. They provide the PDP-11 family diagnostic programs in the various media described. Documentation for each of the programs stored in a XXDP package must be obtained separately. However, said documentation must be obtained at the same time as the package, in order to ensure that the documents and the programs match.

Contents of an XXDP Package – The basic parts of an XXDP package are:

1. A control program referred to as the *monitor.* The monitor provides the means to load programs under keyboard control, to obtain a directory of contents of the XXDP medium (DECtape, Magtape, etc.), to duplicate the medium, and to make up Chains of programs to be run sequentialy under Chain mode.

2. XXDP Update Program 1. This 4K program provides the means for modifying and updating the programs in the XXDP package. It is intended for use in 8K systems.

3. XXDP Update Program 2. A 6K program that provides a more comprehensive set of commands that provide more convenience and ease of updating the XXDP package.

4. The PDP-11 Family Diagnostic programs themselves, including DEC/X11 exerciser (Paragraph 5.4.6).

5.4.2 PDP-11/70 Stand Alone CPU Diagnostics

5.4.2.1 DEKBA and DEKBB (CPU Diagnostics parts 1 and 2) – DEKBA/B are programs designed to detect and report logic faults in the PDP-11/70 Central Processing Unit. They consists of 210(8) individual tests carefully designed and sequenced to detect and attempt to identify logic faults at a minimum hardware/software level. These tests are partitioned into two stand alone programs as described below.

1. Basic Instruction Test
   DEKBA consists of a logially sequenced set of instruction tests designed to verify the integrity of those intructions and logic operations used by the utility routines that provide error reporting and scope looping facilities for DEKBB.

   Any fault detected in this program causes the program to HALT with the console address lights indicating the error program counter and the console data lights showing the test number (for tests 24 and above). Additional fault identification information is available in the program annotation for the failing test.

   If the program halts at location 6 or 12 (address lights of 10 or 14), the program annotation for the indicated test number should give a clue to the problem. To loop on the error, the halt must be replaced by the octal code shown in the comment field of the HALT and the program restarted at 200, or the start address of that particular test.

2. Advanced Instruction and Miscellaneous Logic Test
   DEKBB consists of a logically sequenced set of instruction tests followed by a set of miscellaneous logic tests. The instruction tests complete the test of the PDP-11/70 instruction repertoire. The logic tests verify such things as:

   a. The internal registers
   b. Register set 1
   c. Internal interrupts
   d. Bus request levels 4, 5, and 6
   e. Internal traps and aborts
   f. Other mode selection
   g. External traps and aborts

Each test in this program calls a SCOPE LOOP utility that makes user control of test selection and execution via the console Switch register easier.

Upon detection of a logic fault, each test in this section calls an ERROR SERVICE that reports it as hard copy on the console terminal device. The error service routine also facilitates user control of the program sequence via console Switch register options. After reporting the error, the program continues on its normal sequence unless modified by the user activating the HALT ON ERROR switch option.

3. Important Note
The program annotation in DEKBA and the typed error reports in DEKBB are based upon the knowledge that all previous tests were faultless and that there is only one single point failure in the processor. This means that if either program, or the programs themselves, are not run in sequence, the error message may not be valid.

Although each error annotation and typed message conclusion has been proven by physical fault insertion (one signal stuck low), it is humanly impossible to guarantee that error report is 100% correct. The sole function of the error report is to direct the user to the most probable area of failure.

5.4.2.2 DEKBC and DEKBD (Cache diagnostic parts 1 and 2) – The programs, DEKBC and DEKBD, are intended to be used as aids for the repair and maintenance of the cache memory system in the PDP-11/70 computing system. The aim is to detect and report failing components of the cache unit. The failures are typically identified with a failing circuit when the report is made, but the overall diagnostic philosophy has been to locate the failing module (hex board) of which there are four in the cache unit. Note that when a failure is reported and the associated circuit identified, that circuit should not be taken in blind faith as the defective component; the identified component should rather be taken as the probable cause of the falure. There are four modules (hex boards) in the cache unit:

CCB Cache Control Board
CDP Cache Data Paths Board
ADM Cache Address Memory Board
DTM Cache Data Memory Board

The program DEKBC is designed to test the first two of these boards; the program DEKBD is designed to test the last two boards. Note that though the testing has been divided into two stand alone programs, each associated with two modules, it should not be assumed that a particular module is working after having run only one of the programs. Both programs should be run. For example, just running DEKBC without error does not rule out a faulty component on the CCB (Cache Control) board. To put it more simple, the testing has been divided into programs only because of the restrictions of core size, and not to provide a means of testing two of the boards with one program and the other two boards with a second program.

NOTE

DEKBD is designed to run after DEKBC. If this hierarchy is not heeded, that is, if DEKBD is run before DEKBC, then the error reporting from DEKBD cannot be strictly interpreted.

5.4.2.3 DEKBE (Memory Management Diagnostic) –This program will test all of the memory management logic and enable the field service represenative to isolate the detected failures to a replaceable module. It is assumed that both the CPU and the cache have been tested, or are known to be functioning correctly, and that the program is started from address 200. This will provide the earliest detection of memory management related errors and enable looping on the error involving minimum logic. This program may also expose faults that are on the interface between Memory Management and other sections of the computer.

This program has been segmened in the following way: All data tables, error mssages, and subroutines reside in low core (virtual pages 0 and 1 i.e., addresses 001100 through 037776). Right now the end of the subroutines is around 025000, so there is some room for future expansion. The test code starts at virtual page 2 (address 040000) and expands toward page 4 (address 100000). The end of the program is now around address 074000, so modifications can be made without resegmenting the program.

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The reason for this segmentation is two-fold. Fist it enables the operator to tell from the address lights exactly where the program has halted or hung-up. That is, did it halt in the error routine or in a trap routine because of a condition impossible to recover from (on page 0 or 1), or did it get hung-up in the test code on page 2 or 3. The other reason is that certain memory management functions lock up the virtual PC of the instruction and the program, and in order to operate properly, one must know where it is at all times. It seems much simpler for the code to start at a predetermined boundary so that if the messages change or a new subroutine is added, the page that the code is on will remain the same.

Each test will set the loop on error pointer ($LPERR) to the minimum necessary setup code, if any, for the function under test. A synchronization instruction (NOP) is provided before the intruction(s) that test(s) each new function. This will enable the field service representative to utilize the Micro Break register to generate an External Sync pulse on the backplane for better pulse resolution.

It should be noted that this program does not check out the console or the console cables that plug into the memory management boards. The program assumes that those components have been tested or are known to be good.

5.4.2.4 DEKBF (Unibus Map Diagnostic) – This program is designed to be run on a PDP-11/70 on which the CPU, cache, and memory management diagnostic programs have been run. The program will detect all errors that originate with the Unibus Map and provide looping capabilities so that the field service engineer can verify the failures. There may be some cases, such as the Cache register data path, and cache memory data path, where interaction between modules prohibits close isolation, but the failing function will be called out so the field service engineer can complete the isolation process.

If the program catches an error in an early test and is allowed to continue running through the later tests, the error indications from those later tests may be invalid. This is due to the structure of the program, which assumes that all areas tested prior to the current test are functioning properly.

The error type-outs will be in table format, with a message indicating the class of error, a header identifying each column, and a report of all pertinent data. When the test can produce more than one error condition, a summary of errors will be given at the end of that test consisting of: The logical AND and OR of the data previously reported, and the number of errors in this test.

The program loads 044 into the Micro Break register (17 777 770) so that a sync pulse is generated on pin A10E1 and F13K2 every time a NOP is executed. This should help to isolate the exact timing of bad or missing signals. Refer to Paragraph 5.3.2.8.

5.4.2.5 DEKBG (Power-Fail Test) –This program is made up of 16 subtests to check out the power fail on the PDP-11/70. The 2 ms power down and power up time is checked on each power fail. Initially, power fails are tried in all processor modes, then error conditions like Red Zone, Yellow Zone, Timeout, and Odd Address are tried in all the processor modes. Finally, a power fail is done with memory management aborts occurring and a memory volatility test is run on all available memory.

5.4.2.6 DEQKC (11/70 Instruction Exerciser) – This Diagnostic Program is designed to be a comprehensive check of the PDP-11/70 processor. The program executes each instruction in all address modes and includes tests for traps and the Teletype® interrupt sequence. The program relocates the test code throughout memory 0–512K. If selected, the program may be relocated by any of the available disks.

5.4.2.7 DEMJA (PDP-11/70 Memory Test) – Program DEMJA tests contiguous memory address from 000000 to 17757776. It verifies that each address is unique (an address test) and that each memory location can be read/written reliably (worst case noise tests). This program may be used to adjust/margin memory.

5.4.2.8 CEMKAA (PDP-11/70 Memory Diagnostic) – This program tests both MK11 memory systems and mixed memory systems containing both MJ11 (core) memory and MK11 (MOS) memory frames. Configuration maps and error printouts isolate memory faults to the board level. A field service mode allows test operations to be run directly from a terminal.

5.4.3 RWP04 Diagnostics

DERHA	RH70 Controller Diagnostic
DERPK	Read/Write and Mechanical
DERPL	Formatter program
DERPM	Head Alignment Verification
DERPN	Multidrive Exerciser
DERPS	Diskless Controller Test (Part 1), Static 1
DERPT	Diskless Controller Test (Part 2), Statis 1
DERPU	Functional Controller Test (Part 1), Static 2
DERPV	Functional Controller Test (Part 2), Static 2

Refer to appropriate MAINDEC documentation.

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5.4.4 RWS03 or RWS04 Diagnostics

DERHA	RH70 Controller Diagnostic
DERSA	Basic Function Test
DERSB	Data Reliability
DERSC	Diskless (RS03)
DERSD	Diskless (RS04)

Refer to appropriate MAINDEC documenation.

5.4.5 TU16 Diagnostics

DERHA	RH70 Controller Dignostic
DZTUA	Data Reliability
DZTUB	Basic Function Diagnostic
DZTUC	TM02/TU16 Control Logic Test
DZTUD	TM02 Drive Function Timer
DZTUE	TU16 Utility Driver

Refer to appropriate MAINDEC documentation.

5.4.6 PDP-11/70 DEC/X11

DEC/X11 is a comprehensive, easy to use software system that provides the user with the means to generate, run, control, and update interactive hardware system exerciser programs for PDP-11/70 systems.

Because of the dependency of the DEC/X11 software on the XXDP diagnostic package software, the user is urged to become thoroughly familiar with the uses of the XXDP packages. Refer to *XXDP User Manual,* MAINDEC-11-DZQXA.

DEC/X11 is documented in the *DEC/X11 User's Documentation and Reference Guide,* MAINDEC-11-DXQBA. A programming card, MAINDEC-11-DZZPA is also available.

5.4.7 PDP-11/70 Subsystem Diagnostic

The objectives of the PDP-11/70 subsystem diagnostics are:

1. To check the complete CPU cluster of the PDP-11/70 system. This cluster includes: CPU, cache, memory management, Unibus Map, and all of main memory, and will also ensure that the Unibus and Massbus are capable of performing data transfers.

2. To find subsystem problems *within the CPU cluster* and, through error analysis, attempt to isolate these problems to the failing subsystem.

3. To allow quick verification of a questionable system or to ensure the integrity of a newly-repaired system.

This program is intended:

1. To allow the Field Service Engineer to logically attack a problem on a system's level.

2. To allow rapid isolation of a problem in order to minimize MTTR (Mean Time To Repair).

3. To allow quick verification of a questionable system or to ensure the integrity of a newly repaired system.

The operator selects elements that are run under the PDP-11/70 system diagnostic, which in turn is a module run under the DEC/X11 monitor. Errors ocurring in the CPU cluster are analyzed. The results of this analysis, if errors are relatively concrete, will be isolation to some subsystem. Unibus and Massbus device transfers are attempted and any errors are reported. Errors are also logged and analyzed in an attempt to provide further isolation through the use of the stand alone diagnostics.

This program assumes that the diagnostic boot ROM (M9301-YC) has run successfully and that a successful load has occurred via the XXDP device.

The subsystem diagnostic programs are fully documented in MAINDEC-11-DTUMA.

5.4.8 DZKWA (Line Clock Test)

This program tests the KW11L line frequency clock. It validates proper operation under both Interrupt and Non-interrupt modes. It requires the operator to monitor its operation with a clock capable of measuring time in seconds.

5.4.9 DZKLA (TTY or DECwriter Test)

This MAINDEC consists of a package of test programs designed to test an ASR33, KSR33, ASR35, or KSR35 teletype when attached to a PDP-11 system through a KL11 or DL11A teletype control. All tests are included in a single object tape.

NOTE

The following programming format is illegal and is not used in this program: message, filler, filler, reset, and another message immediately.

The available test programs are listed here in numerical order:

PRG0	Combined Input-Output Logic Tests
PRG1	Reader Test
PRG2	Printer Test
PRG3	Punch Test
PRG4	Keyboard Test
PRG5	Combined Reader-Punch-Printer Test
PRG6	Reader Exerciser-Special Binary Count Pattern
PRG7	Printer Exerciser
PRG10	Special Binary Count Pattern Tape Generator
PRG11	Punch Clock Adjustment Routine
PRG12	Reader Clock Adjustment Routine
PRG13	Maintenance Mode Single Character Data Test
PRG14	Maintenance Mode Special Binary Count Pattern Test

Programs PRG0 through PRG5 are the actual teletype tests.
Programs PRG6 through PRG14 are utility and maintenance routines.

5.4.10 Maintenance Program Generator (MPG)

MPG (MAINDEC-11-DTUMA) is a compiler that uses english language statements. It provides hardware oriented technical personnel with the ability to easily generate and execute programs on the PDP-11 series of computers. While these programs may be written to perform any type of task, the major applications expected are programs that aid in the maintenance and repair of peripheral devices.

The XXDP Update Program 2 (UPD2 - MAINDEC - 11-ZQUB) is used for certain MPG media maintenance and creation functions. In addition, MPG uses the XXDP media and therefore is preceded by execution of the applicable XXDP Monitor.

Related Documents – For details concerning the operation of the XXDP monitor and the UPD2 program, refer to the XXDP User's Manual (MAINDEC-11-DZQXA).

A catalog of selected MPG User programs will be provided in the MPG User Program Manual (MAINDEC-11-DTUPA). These will be programs developed by MPG factory and field users.

5.4.11 M9301-YC and DEKBH

This paragraph contains both a listing of DEKBH, the ROM program contained on the M9301-YC, and a brief description of the interaction between DEKBH and the logic on the M9301.

The operation of the bootstrap module is described in Paragraph 3.4.2.

M9301/DEKBH Interaction – Refer to schematic D-CS-M9301-0-1 and to the DEKBH listing, which is reproduced at the end of Chapter 5.

The M9301 is a Unibus device which responds to addresses 17 765 000 – 17 765 776 and 17 773 000 – 17 773 776. The starting address is loaded (17 765 000) and, when START is pressed on the K11-B console, this address is decoded by the logic on sheet 3 of the schematic. When MSYN is received, ENAB DATA and 765XXX L are asserted, and the first ROM word is read by the processor; this is the first instruction of DEKBH.

Instructions are read from the ROM and executed in the following order (refer to DEKBH listing in Chapter 5):

1. 17 765 000 – 17 765 776 (diagnostic)
2. 17 773 606 – 17 773 776 (diagnostic)
3. 17 773 000 – 17 773 604 (bootstrap)

Location 17 765 772 contains a JMP to 17 773 606 at which time 773XX L is asserted. Location 17 773 774 contains a JMP to 17 773 000. 773XXX L also asserts ENAB DATA and allows the bootstrap portion of DEKBH to be executed.

If the diagnostic portion of the program finds an error, the program halts. Refer to Chapter 5 for an explanation of the use of the diagnostic.

Default Device and Drive – Refer to line numbers 716–724 of the DEKBH listing and to the lower right of sheet 4 of the schematic.

1. Line 715 moves the low order byte of the Switch register to R0. If R0 is not equal to 0, the program branches to 1$ (line 724), where R0 is moved to R4 and then decoded into device and drive parameters.

2. If R0 is equal to 0, the program does not branch (line 717), but moves the contents of the updated PC (17 773 024) to R0, then increments the PC and executes the next instruction, ASR R0, (line 723), which shifts the contents of location 17 773 024 right one bit. This location reflects the setting of S1–3 through S1–10 on the M9301-YC.

ENAB JUMP L is asserted when bits (08:01) of the Unibus address lines equal 024 octal, and the high order Unibus address is not 765 octal. If the program calls for 17 773 024 (step 2 above), 773XXX L is asserted, as is ENAB DATA L; the ROM data word [ROM D(15:01) L] at location 17 773 024 is 0. The 7402s on sheet 4 of the schematic are all asserted (outputs high); they enable the 8881 Unibus drivers for BUS D(08:01).

1. If any of the switches S1-3 through S1-10 are *OPEN* (off), the Unibus driver to which it is the input, is then asserted (low=1).

2. If any of the switches S1-3 through S1-10 are *CLOSED* (on), the Unibus driver to which it is the input, is not asserted (high=0) since ENAB JUMP L is asserted (low) and disables the Unibus driver.

3. The data from the switches is output on BUS D(08:01) L. This is the reason for the ASR on line 723 of DEKBH.

NOTE

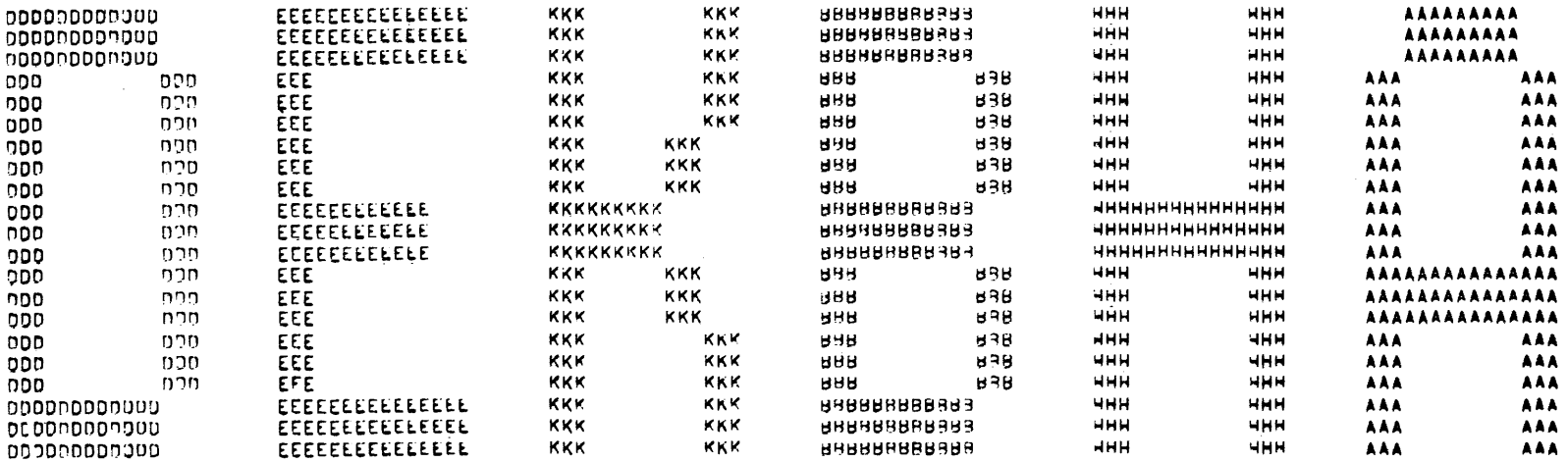
The preceding logic description corresponds to Rev F of the M9301. Rev E logic is slightly different, but overall operation is identical. Note also that the DEKBH program is the same in both revisions, but the ROMs are different. Check the revision before ordering spares.

5.4.12 M9301-YH and 60BOOT

The ROM program contained on the M9301-YH is called 60BOOT. For the M9301-YH, consult the bootstrap and diagnostic listing, 60BOOT LST. A current listing of 60BOOT is included in the documentation package supplied with the processor.

5.4.13 M9312 and DIAROM

The M9312 Bootstrap and Terminator Module contains the diagnostic ROM program DIAROM. For the M9312, consult Section II of the listing, DIAROM LST. A current listing of this diagnostic program is supplied with the documentation package shipped with the processor. Program listings for the bootstrap ROMs are supplied with the individual ROMs




```
LPTSPL Version 6(344)  Running on LPT0
 *START* User 21,ROEDGER [404,3143] Job  DEKBHA Seq, 2671 Date 18-Jun-75 17:22:41 Monitor CS2-518 507898 1070 T/M *SLAVE*
Request created: 18-Jun-75  17:00:10
File: JML10:DEKBHA.LIS[404,3143] Created: 17-Jun-75 10:04:00 <157>  Printed: 18-Jun-75 20:29:00
QUEUE Switches:  /PRINT:ARROW /FILE:ASCII /COPIES:15 /SPACING:1 /LIMIT:4966 /FORMS:JML1
File will be RENAMEd to <157> protection
```

```
.TITLE  PDP-11/70 DIAGNOSTIC/BOOTSTRAP (M9301-YC) PATTERN
;* COPYRIGHT (C) JUNE 21,1975
;* DIGITAL EQUIPMENT CORPORATION
;* MAYNARD, MASS. 01754
;*
;* PROGRAMMER DALE A. ROEDGER
;*

;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
;*
;*      TO INITIATE THE DIAGNOSTIC/BOOTSTRAP PROGRAM IN THE M9301-YC
;*      THE OPERATOR MUST: LOAD ADDRESS 17765000, SELECT THE DESIRED
;*      DEVICE CODE, DRIVE NUMBER, AND MEMORY BLOCK VIA THE SWITCH
;*      REGISTER, AND THEN PRESS "START".  AFTER THE PROGRAM HAS
;*      VERIFIED THE C.P.U., CACHE, AND THE 28K BLOCK OF MEMORY
;*      SELECTED TO BE USED (APPROXIMATELY 3 SECONDS) THE PERIPHERAL
;*      DEVICE WILL "BOOT" THE SYSTEM MONITOR.
;*
;*      THE DRIVE NUMBER DESIRED (0 - 7) MUST BE IN THE SWITCH REGISTER,
;*      SWITCHES <02 : 00>.
;*
;*      THE CODE FOR THE DESIRED DEVICE (1 - 11) MUST BE IN THE SWITCH
;*      REGISTER, SWITCHES <07 : 03>.
;*
;*      THE DEVICE CODES AND DEVICE NAMES ARE AS FOLLOWS:
;*      1)      TM11/TU10       MAGNETIC TAPE, TM11
;*      2)      TC11/TU56       DECTAPE, TC11-G
;*      3)      RK11/RK05       DECPACK DISK CARTRIDGE, RK11-D
;*      4)      RP11/RP03       DISK PACK, RP11-C
;*      5)      RESERVED
;*      6)      RH70/TU16       MAGNETIC TAPE SYSTEM, TWU16
;*      7)      RH70/RP04       DISK PACK, RWP04
;*      10)     RH70/RS04       FIXED HEAD DISK, RWS04 (OR RWS03)
;*      11)     RX11/RX01       DISKETTE
;*
;*      THE 32K MEMORY BLOCK NUMBER (0 - 17) IN WHICH TO "BOOT" THE
;*      SYSTEM MUST BE IN THE SWITCH REGISTER, SWITCHES <15 : 12>.
;*      MEMORY BLOCK 0 CORRESPONDS TO PHYSICAL 0 - 28K,
;*      MEMORY BLOCK 1 CORRESPONDS TO PHYSICAL 32K - 60K,
;*      MEMORY BLOCK 2 CORRESPONDS TO PHYSICAL 64K - 92K,
;*      .
;*      .
;*      MEMORY BLOCK 16 CORRESPONDS TO PHYSICAL 448K - 476K,
;*      MEMORY BLOCK 17 CORRESPONDS TO PHYSICAL 480K - 508K.
;*
;*      IF THE DIAGNOSTIC PORTION OF THE PROGRAM FAILS AND YOU WANT
;*      TO TRY TO BOOT ANYWAY, THEN YOU MUST LOAD ADDRESS 17773000,
;*      SELECT THE DRIVE NUMBER AND DEVICE CODE AS BEFORE.  NOW YOU
;*      MUST SET UP MEMORY MANAGEMENT IF YOU WISH TO "BOOT" INTO
;*      OTHER THAN THE LOWER 28K OF MEMORY, AND FOLLOW THE PROCEDURES
;*      LISTED BELOW FOR YOUR PERIPHERAL DEVICE.
;*
;*      1)  IF THE DEVICE IS ON THE MASS BUS:
;*      THE STACK POINTER (R6) MUST BE SETUP AND THE WORD THAT IT POINTS
;*      TO MUST CONTAIN THE BLOCK NUMBER OF THE 32K BOUNDARY THAT YOU
;*      WISH TO BOOT INTO.
;*
;*      2)  IF THE DEVICE IS ON THE UNIBUS:
;*      YOU MUST SET UP THE UNIBUS MAP IN ADDITION TO MEMORY MANAGEMENT.
;*
;***********************************************************************
```

```
                          ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                          ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                          ;*
                          ;*      IF THIS PROGRAM FAILS IN AN UNCONTROLLED MANNER IT MIGHT
                          ;*      BE DUE TO AN UNEXPECTED TRAP TO LOCATION 000004.  IF THIS IS
                          ;*      SUSPECTED THEN LOAD A "000006" INTO ADDRESS 000004 AND A
                          ;*      "000000" INTO LOCATION 000006.  THIS WILL CAUSE ALL TRAPS TO
                          ;*      LOCATION 000004 TO HALT WITH 00000010 IN THE ADDRESS LIGHTS SO
                          ;*      THAT THE OPERATOR CAN EXAMINE THE CPU ERROR REGISTER AT
                          ;*      LOCATION 17777766. .
                          ;*
                          ;*      THE BITS IN THE CPU ERROR REGISTER ARE DEFINED AS FOLLOWS:
                          ;*      BIT02   = RED ZONE STACK LIMIT
                          ;*      BIT03   = YELLOW ZONE STACK LIMIT
                          ;*      BIT04   = UNIBUS TIME-OUT
                          ;*      BIT05   = NON-EXISTANT MEMORY (CACHE)
                          ;*      BIT06   = ODD ADDRESS ERROR
                          ;*      BIT07   = ILLEGAL HALT
                          ;*
                          ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
                          ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

                          ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                          ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                          ;*
                          ;*      NOTE:   IN THE COMMENT FIELD OF THE BRANCHES THAT ARE BEING
                          ;*              TESTED, JUST PRECEEDING THE ROM ADDRESS INVOLVED, IS
                          ;*              A SYMBOL USED TO INDICATE WHETHER TO TAKE THE BRANCH
                          ;*              UNDER TEST OR TO FALL THROUGH TO THE NEXT INSTRUCTION.
                          ;*              A "V" INDICATES THAT THE BRANCH SHOULD NOT BE TAKEN,
                          ;*              AND THE NEXT INSTRUCTION SHOULD BE EXECUTED.  A "*"
                          ;*              INDICATES THAT THE BRANCH SHOULD BE EXECUTED, UNLESS
                          ;*              AN ERROR CONDITION OCCURS.
                          ;*
                          ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
                          ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

                165000            . = BASE1
                          ;;*******************************************************************
                                  .SBTTL  TEST1   THIS TEST VERIFIES THE UNCONDITIONAL BRANCH
                          ;*
                          ;*      THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
                          ;*      THIS TEST IS ENTERED AND THEY SHOULD REMAIN THAT WAY UPON
                          ;*      THE COMPLETION OF THIS TEST.
                          ;*
                          ;;*******************************************************************
      165000              TST1:
      165000    000401            BR      TST2                    ; * 326 BRANCH ALWAYS
      165002    000000            HALT

                          ;;*******************************************************************
                                  .SBTTL  TEST2   TEST "SUB", MODE "0", AND "BMI","BVS","BHI","BLOS"
                          ;*
                          ;*      THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
                          ;*      THIS TEST IS ENTERED.  UPON COMPLETION OF THIS TEST THE "SP"
                          ;*      (R6) SHOULD BE ZERO AND ONLY THE "Z" FLIP-FLOP WILL BE SET.
                          ;*
                          ;;*******************************************************************
      165004              TST2:

      165004    005006            CLR     SP                      ;N=0,Z=1;V=0,C=0,SP=000000
      165006    100403            BMI     1$                      ; V 324 BRANCH IF N=1
      165010    102402            BVS     1$                      ; V 324 BRANCH IF V=1
      165012    101001            BHI     1$                      ; V 321 BRANCH IF Z AND C ARE BOTH 0
      165014    101401            BLOS    TST3                    ; * 325 BRANCH IF (Z XOR C)=1
      165016    000000    1$:     HALT

                          ;;*******************************************************************
                                  .SBTTL  TEST3   TEST "DEC", MODE "0", AND "BPL","BEQ","BGE","BGT","BLE"
                          ;*
                          ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                          ;*      N = 0, Z = 1, V = 0, AND C = 0.
                          ;*      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                          ;*      R3 = ? R4 = ? R5 = ? SP = 000000
                          ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                          ;*      N = 1, Z = 0, V = 0, AND C = 0
                          ;*      THE REGISTERS AFFECTED BY THE TEST ARE:
                          ;*      SP = 177777
                          ;*
                          ;;*******************************************************************
      165020              TST3:
      165020    005306            DEC     SP                      ;N=1,Z=0;V=0,C=0,SP=177777
      165022    100004            BPL     1$                      ; V 321 BRANCH IF N=0
      165024    001403            BEQ     1$                      ; V 324 BRANCH IF Z=1
      165026    002002            BGE     1$                      ; V 322 BRANCH IF (N XOR V)=0
      165030    003001            BGT     1$                      ; V 322 BRANCH IF Z AND (N XOR V) ARE BOTH 0
      165032    003401            BLE     TST4                    ; * 326 BRANCH IF [Z OR (N XOR V)]=1
      165034    000000    1$:     HALT

                          ;;*******************************************************************
                                  .SBTTL  TEST4   TEST "ROR", MODE "0", AND "BVC","BHIS","BHI","BNE"
                          ;*
                          ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                          ;*      N = 1, Z = 0, V = 0, AND C = 0.
                          ;*      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                          ;*      R3 = ? R4 = ? R5 = ? SP = 177777
                          ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                          ;*      N = 0, Z = 0, V = 1, AND C = 1
                          ;*      THE REGISTERS AFFECTED BY THE TEST ARE:
                          ;*      SP = 077777
                          ;*
                          ;;*******************************************************************
      165036              TST4:
      165036    006006            ROR     SP                      ;N=0,Z=0;V=1,C=1,SP=077777
```

```
165040  102003                  BVC     1$              ; V 321 BRANCH IF V=0
165042  103002                  BHIS    1$              ; V 321 BRANCH IF C=0
165044  101001                  BHI     1$              ; V 321 BRANCH IF C AND Z ARE BOTH 0
165046  001001                  BNE     TST5            ; * 320 BRANCH IF Z=0
165050  000000          1$:     HALT

                        ;;**********************************************************************
                                .SBTTL  TEST5   TEST "BHI", "BLT", AND "BLOS"
                        ;*
                        ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 0, V = 1, AND C = 1,
                        ;*      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                        ;*      R3 = ? R4 = ? R5 = ? SP = 0/7777
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                        ;*      N = 1, Z = 1, V = 1, AND C = 1
                        ;*      THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.
                        ;*
                        ;;**********************************************************************
165052          TST5:
165052  000264                  SEZ                     ;N=0,Z=1;V=1,C=1
165054  101003                  BHI     1$              ; V 321 BRANCH IF Z AND C ARE BOTH 0
165056  000270                  SEN                     ;N=1,Z=1;V=1,C=1
165060  002401                  BLT     1$              ; V 324 BRANCH IF (N XOR V)=1
165062  101401                  BLOS    TST6            ; * 325 BRANCH IF (Z OR C)=1
165064  000000          1$:     HALT                    ;STOP HERE IF A BRANCH FAILED

                        ;;**********************************************************************
                                .SBTTL  TEST6   TEST "BLE" AND "BGT"
                        ;*
                        ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 1, Z = 1, V = 1, AND C = 1,
                        ;*      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                        ;*      R3 = ? R4 = ? R5 = ? SP = 07777
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                        ;*      N = 1, Z = 0, V = 1, AND C = 1
                        ;*      THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.
                        ;*
                        ;;**********************************************************************
165066          TST6:
165066  000244                  CLZ                     ;N=1,Z=0;V=1,C=1
165070  003401                  BLE     1$              ; V 324 BRANCH IF (Z OR (N XOR V))=1
165072  003001                  BGT     TST7            ; * 320 BRANCH IF Z AND (N XOR V) ARE BOTH 0
165074  000000          1$:     HALT                    ;STOP HERE IF A BRANCH FAILED

                        ;;**********************************************************************
                                .SBTTL  TEST7   TEST REGISTER DATA PATH AND MODES "2", "3", "6"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 1, Z = 0, V = 1, AND C = 1,
                        ;*      THE REGISTERS ARE: R0 = ?, R1 = ?, R2 = ?
                        ;*      R3 = ?, R4 = ?, R5 = ?, SP = 07777,
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0,
                        ;*      THE REGISTERS ARE LEFT AS FOLLOWS:
                        ;*      R0 = 125252, R1 = 000000, R2 = 125252, R3 = 125252
                        ;*      R4 = 125252, R5 = 125252, SP = 125252, AND MAPL00 = 125252
                        ;*
                        ;;**********************************************************************
165076          TST7:
165076  012706  125252          MOV     #125252,SP      ;N=1,Z=0;V=0,C=1,SP=125252
165102  010600                  MOV     SP,R0           ;N=1,Z=0;V=0,C=1,R0=125252
165104  010001                  MOV     R0,R1           ;N=1,Z=0;V=0,C=1,R1=125252
165106  010102                  MOV     R1,R2           ;N=1,Z=0,V=0,C=1,R2=125252
165110  010203                  MOV     R2,R3           ;N=1,Z=0,V=0,C=1,R3=125252
165112  010304                  MOV     R3,R4           ;N=1,Z=0;V=0,C=1,R4=125252
165114  010405                  MOV     R4,R5           ;N=1,Z=0,V=0,C=1,R5=125252
165116  010537                  MOV     R5,@(PC)+       ;N=1,Z=0,V=0,C=1
165120  170200          INDMAP: ,WORD   MAPL0           ;MAPL0=125252
165122  167701  177772                  SUB     @INDMAP,R1      ;N=0,Z=1,V=0,C=0, AND R1=000000
165126  002401                  BLT     1$              ; V 324 BRANCH IF (N XOR V)=1
165130  001401                  BEQ     TST10           ; * 326 BRANCH IF Z=1
165132  000000          1$:     HALT

                        ;;**********************************************************************
                                .SBTTL  TEST10  TEST "ROL", "BCC", "BLT", AND MODE "6"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0,
                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                        ;*      R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252.
                        ;*      MAPL00 = 125252
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 0, V = 1, AND C = 1,
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      MAPL00 WHICH SHOULD NOW EQUAL 052524,
                        ;*
                        ;;**********************************************************************
165134          TST10:
165134  006167  003040                  ROL     MAPL0           ;N=0,Z=0;V=1,C=1, AND MAPL00 = 052524
165140  103001                  BCC     1$              ; V 321 BRANCH IF C=0
165142  002401                  BLT     TST11           ; * 326 BRANCH IF (N XOR V)=1
165144  000000          1$:     HALT

                        ;;**********************************************************************
                                .SBTTL  TEST11  TEST "ADD", "INC", "COM", AND "BCS", "BLE
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 0, V = 1, AND C = 1,
                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                        ;*      R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252.
                        ;*      MAPL00 = 052524,
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0,
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R3 WHICH NOW EQUALS 000000, AND R1 WHICH IS ALSO 000000
                        ;*
                        ;;**********************************************************************
165146          TST11:
```

```
                                                        ;(MAPL00 = 052524) + (R3 = 125252)
165146  066703  003026          ADD     MAPL0,R3        ;N=1,Z=0,V=0,C=0, AND R3=177776
165152  005203                  INC     R3              ;N=1,Z=0,V=0,C=0, AND R3=177777
165154  005103                  COM     R3              ;N=0,Z=1,V=0,C=1, AND R3 = 000000
165156  060301                  ADD     R3,R1           ;N=0,Z=1,V=0,C=0, AND R1 = 000000
165160  103401                  BCS     1$              ; V 324 BRANCH IF C=1
165162  003401                  BLE     TST12           ; * 326 BRANCH IF [Z OR (N XOR V)]=1
165164  000000          1$:     HALT

                        ;;**********************************************************************
                                .SBTTL  TEST12  TEST "ROR", "BIS", "ADD", AND "BLO", "BGE"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                        ;*      R3 = 000000, R4 = 125252, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R3 WHICH SHOULD BE MODIFIED BACK TO 000000, AND
                        ;*      R4 WHICH SHOULD NOW EQUAL 052525
                        ;*
                        ;;**********************************************************************
165166          TST12:
165166  006004                  ROR     R4              ;N=0,Z=0,V=1,C=0, AND R4 = 052525
165170  050403                  BIS     R4,R3           ;N=0,Z=0,V=0,C=0, AND R3 = 052525
165172  060503                  ADD     R5,R3           ;N=1,Z=0,V=0,C=0, AND R3 = 177777
165174  005203                  INC     R3              ;N=0,Z=1,V=0,C=0, AND R3 = 000000
165176  103401                  BLO     1$              ; V 324 BRANCH IF C=1
165200  002001                  BGE     TST13           ; * 326 BRANCH IF (N XOR V)=0
165202  000000          1$:     HALT

                        ;;**********************************************************************
                                .SBTTL  TEST13  TEST "DEC" AND "BLOS", "BLT"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                        ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 1, Z = 0, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R1 WHICH SHOULD NOW EQUAL 177777
                        ;*
                        ;;**********************************************************************
165204          TST13:
165204  005301                  DEC     R1              ;N=1,Z=0,V=0,C=0,R1=177777
165206  101401                  BLOS    1$              ; V 324 BRANCH IF (Z OR C)=1
165210  002401                  BLT     TST14           ; * 326 BRANCH IF (N XOR V)=1
165212  000000          1$:     HALT

                        ;;**********************************************************************
                                .SBTTL  TEST14  TEST "COM", "BIC", AND "BGT", "BGE", "BLE"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 1, Z = 0, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 177777, R2 = 125252
                        ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 0, V = 1, AND C = 1.
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R0 WHICH SHOULD NOW EQUAL 052525, AND
                        ;*      R1 WHICH SHOULD NOW EQUAL 052524
                        ;*
                        ;;**********************************************************************
165214          TST14:
165214  005100                  COM     R0              ;N=0,Z=0,V=0,C=1, AND R0 = 052525
165216  101401                  BLOS    2$              ; * 325 BRANCH IF (Z OR C)=1
165220  000000                  HALT                    ;STOP HERE IF BRANCH FAILED
165222  040001          2$:     BIC     R0,R1           ;N=1,Z=0,V=0,C=1, AND R1 = 125252
165224  060101                  ADD     R1,R1           ;N=0,Z=0,V=1,C=1, AND R1 = 052524
165226  003002                  BGT     1$              ; V 322 BRANCH IF Z AND (N XOR V) ARE BOTH 0
165230  002001                  BGE     1$              ; V 322 BRANCH IF (N XOR V)=0
165232  003401                  BLE     TST15           ; * 326 BRANCH IF [Z OR (N XOR V)]=1
165234  000000          1$:     HALT

                        ;;**********************************************************************
                                .SBTTL  TEST15  TEST "ADC", "CMP", "BIT", AND "BNE","BGT","BEQ"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 0, V = 1, AND C = 1.
                        ;*      THE REGISTERS ARE: R0 = 052525, R1 = 052524, R2 = 125252
                        ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE NOW:
                        ;*      R0 = 052525, R1 = 000000, R2 = 125252, R3 = 000000
                        ;*      R4 = 052525, R5 = 052525, SP = 125252.
                        ;*
                        ;;**********************************************************************
165236          TST15:
165236  005501                  ADC     R1              ;N=0,Z=0,V=0,C=0, AND R1 = 052525
165240  020401                  CMP     R4,R1           ;N=0,Z=1,V=0,C=0
165242  001005                  BNE     1$              ; V 322 BRANCH IF Z=0
                                                        ;R1 = 052525  R5 = 125252
165244  030105                  BIT     R1,R5           ;N=0,Z=1,V=0,C=0
165246  003003                  BGT     1$              ; V 322 BRANCH IF Z AND (N XOR V) ARE BOTH 0
165250  005105                  COM     R5              ;N=0,Z=0,V=0,C=1, AND R5 = 052525
165252  160501                  SUB     R5,R1           ;N=0,Z=1,V=0,C=0, AND R1 = 000000
165254  001401                  BEQ     TST16           ; * 326 BRANCH IF Z=1
165256  000000          1$:     HALT

                        ;;**********************************************************************
                                .SBTTL  TEST16  TEST "MOVB", "SOB", "CLR", "TST" AND "BPL", "BNE"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE: R0 = 052525, R1 = 000000, R2 = 125252
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```
                        ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0,
                        ;*      R0 IS DECREMENTED BY A SOB INSTRUCTION TO 000000
                        ;*      R1 IS CLEARED AND THEN INCREMENTED AROUND TO 000000
                        ;*
                        ;;*************************************************************************
165260                  TST16:
165260  012700  177401          MOVB    #177401,R0      ;N=0,Z=0;V=0,C=0, AND R0 = 000001
165264  100001                  BPL     2$              ; = 320 BRANCH IF N=0
165266  000000          1$:     HALT                    ;STOP IF "BPL" FAILED
165270  077002          2$:     SOB     R0,1$           ;DO NOT LOOP SINCE (R0 - 1) = 0
165272  005001                  CLR     R1              ;N=0, Z=1, V=0, C=0, AND R1 = 000000
165274  005201          3$:     INC     R1              ;INCREMENT 64K TIMES (2 ** 16)
165276  077002                  SOB     R0,3$           ;LOOP BACK TO "INC" 64K TIMES
165300  005700                  TST     R0              ;N=0,Z=1,V=0,C=0, AND R0 = 000000
165302  001002                  BNE     4$              ; V 322 BRANCH IF Z=0
165304  005701                  TST     R1              ;N=0,Z=1,V=0,C=0, AND R1 = 000000
165306  001401                  BEQ     TST17           ; = 326 BRANCH IF Z=1
165310  000000          4$:     HALT
                        ;
                        ;;*************************************************************************
                                .SBTTL  TEST17: TEST "ASR", "ASL"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0,
                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                        ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252,
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 0, V = 0, AND C = 0,
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R0 WHICH IS NOW EQUAL TO 000000,
                        ;*      R1 WHICH IS NOW 000001, AND
                        ;*      R2 WHICH IS NOW 000000.
                        ;*
                        ;;*************************************************************************
165312                  TST17:
165312  012700  100000          MOV     #100000,R0      ;R0=100000
165316  005201                  INC     R1              ;R1=000001
165320  012702  000020          MOV     #^D16,R2        ;SET COUNTER TO 16 DECIMAL
165324  006200          1$:     ASR     R0              ;RIGHT SHIFT R0, SIGN EXTEND (16 TIMES)
165326  005500                  ADC     R0              ;ADD CARRY (0 UNTIL LAST TIME)
165330  006301                  ASL     R1              ;LEFT SHIFT R1 (16 TIMES)
165332  005501                  ADC     R1              ;ADD CARRY (0 UNTIL LAST TIME)
165334  077205                  SOB     R2,1$           ;LOOP BACK 16 DECIMAL TIMES
                                                        ;AT THE END OF THE LOOP
                                                        ;R0 = 000000  AND  R1 = 000001
165336  060001                  ADD     R0,R1           ;N=0,Z=0;V=0,C=0  R1=000001, R0=000000
165340  003401                  BLE     2$              ; V 324 BRANCH IF [Z OR (N XOR V)]=1
165342  003001                  BGT     TST20           ; = 320 BRANCH IF Z AND (N XOR V) ARE BOTH 0
165344  000000          2$:     HALT
                        ;
                        ;;*************************************************************************
                                .SBTTL  TEST20: TEST ASH, AND SWAB
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 0, V = 0, AND C = 0,
                        ;*      THE REGISTERS ARE: R0 = 000000, R1 = 000001, R2 = 000000
                        ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252,
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 1,
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R1 WHICH SHOULD NOW EQUAL 000000
                        ;*
                        ;;*************************************************************************
165346                  TST20:
165346  072127  000007          ASH     #7,R1           ;LEFT SHIFT BIT0 INTO BIT7
                                                        ;N=0,Z=0;V=0,C=0, AND R1 = 000200
165352  105701                  TSTB    R1              ;LOWER BYTE SHOULD BE NEGATIVE
                                                        ;N=1,Z=0,V=0,C=0
165354  100401                  BMI     1$              ; = 325 BRANCH IF N=1
165356  000000                  HALT                    ;"ASH" MUST HAVE FAILED
165360  000301          1$:     SWAB    R1              ;SWITCH BYTES OF R1, R1 = 100000
                                                        ;N=1,Z=0,V=0,C=0
165362  072127  177761          ASH     #-^D15,R1       ;RIGHT SHIFT R1 15 PLACES SIGN EXTEND
                                                        ;N=1,Z=0;V=0,C=0, R1 = 177777
165366  005201                  INC     R1              ;N=0,Z=1;V=0,C=1, R1 = 000000
165370  001401                  BEQ     TST21           ; = 326 BRANCH IF Z=1
165372  000000                  HALT                    ;EITHER "SWAB" OR "ASH" FAILED
                        ;
                        ;;*************************************************************************
                                .SBTTL  TEST21: TEST 16 KERNEL P.A.R.'S
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 1,
                        ;*      THE REGISTERS ARE: R0 = 000000, R1 = 000000, R2 = 000000
                        ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252,
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0,
                        ;*      THE REGISTERS NOW EQUAL:
                        ;*      R0 = 172400, R1 = 000000, R2 = 000000, R3 = 000000
                        ;*      R4 = 052525, R5 = 125252, SP = 125252,
                        ;*      ALL KERNEL P.A.R.'S = 125252.
                        ;*
                        ;;*************************************************************************
165374                  TST21:
165374  012700  172340          MOV     #KIPAR0,R0      ;FIRST "PAR" TO BE CHECKED
165400  012701  000020          MOV     #^D16,R1        ;DO KIPAR0 THRU KDPAR7
165404  005105                  COM     R5              ;R5=125252
165406  012420          1$:     MOV     R4,(R0)+        ;PAR=052525
165410  020460  177776          CMP     R4,-2(R0)       ;DID IT LOAD PROPERLY?
165414  001014                  BNE     2$              ; V BRANCH IF NO  R0 = PAR + 2
165416  105140                  COMB    -(R0)           ;COMPLEMENT HIGH BYTE  PAR=125125
165420  120510                  CMPB    R5,(R0)         ;CHECK THE HIGH BYTE
165422  001011                  BNE     2$              ; V BRANCH IF BAD  R0 = PAR + 1
165424  120440                  CMPB    R4,-(R0)        ;CHECK THE LOW BYTE DIDN'T CHANGE
165426  001007                  BNE     2$              ; V BRANCH IF IT CHANGED  R0 = PAR
165430  105110                  COMB    (R0)            ;COMPLEMENT THE LOW BYTE  PAR=125252
```

```
165432  120520                  CMPB    R5,(R0)+        ;CHECK THE LOW BYTE
165434  001004                  BNE     2$              ; V BRANCH IF BAD  R0 = PAR + 1
165436  120520                  CMPB    R5,(R0)+        ;CHECK THE HIGH BYTE
165440  001002                  BNE     2$              ; V BRANCH IF IT FAILED  R0 = PAR + 2
165442  077117                  SOB     R1,1$           ;LOOP UNTIL KDPAR7 HAS BEEN TESTED
165444  000401                  BR      TST22           ; * BRANCH TO NEXT TEST
165446  000000          2$:     HALT                    ;A P.A.R. FAILED TO HOLD THE RIGHT DATA
                                                        ;CHECK R0 FOR THE ADDRESS


                        ;!*****************************************************************
                                .SBTTL  TEST22  TEST AND LOAD KIPDR'S
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE: R0 = 172400, R1 = 000000, R2 = 000000
                        ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS THAT ARE MODIFIED ARE:
                        ;*      R0 = 172300, R1 = 000000, R2 = 077406
                        ;*      ALL KERNEL I-SPACE P.D.R.'S (172300 - 172316) = 077406
                        ;*
                        ;!*****************************************************************
165450                  TST22:
165450  012700  172320          MOV     #KIPDR7+2,R0    ;START WITH LAST "PDR"
165454  012701  000010          MOV     #^D8,R1         ;DO KIPDR7 THRU KIPDR0
165460  012702  077406          MOV     #077406,R2      ;PATTERN TO TEST "PDR'S"
165464  010240          1$:     MOV     R2,-(R0)        ;LOAD "PDR" UNDER TEST
165466  021002                  CMP     (R0),R2         ;SEE IF THE DATA LOADED IS CORRECT
165470  001401                  BEQ     2$              ;BRANCH IF THE DATA MATCHES
165472  000000                  HALT                    ;A "PDR" HAS FAILED
                                                        ;R0 HAS THE ADDRESS OF THE BAD "PDR"
                                                        ;R2 HAS THE EXPECTED DATA
165474  077105          2$:     SOB     R1,1$           ;LOOP UNTIL ALL EIGHT "PDR'S" HAVE BEEN
                                                        ;TESTED


                        ;!*****************************************************************
                                .SBTTL  TEST23  TEST "JSR", "RTS", "RTI", & "JMP"
                        ;*
                        ;*      THIS TEST FIRST SETS THE STACK POINTER TO "KDPAR7" (172376),
                        ;*      AND THEN VERIFIES THAT "JSR", "RTS", "RTI", AND "JMP"
                        ;*      ALL WORK PROPERLY.
                        ;*
                        ;*      ON ENTRY TO THIS TEST THE STACK POINTER "SP" IS INITIALIZED
                        ;*      TO 172376 AND IS LEFT THAT WAY ON EXIT.
                        ;*
                        ;!*****************************************************************
165476                  TST23:

165476  012706  172370          MOV     #KDPAR7,SP      ;SET UP THE STACK POINTER
165502  004767  000002          JSR     PC,1$           ;TRY TO JSR TO 1$
165506  000000          10$:    HALT                    ;THE "JSR" MUST HAVE FAILED
165510  022716  165506  1$:     CMP     #10$,(SP)       ;WAS THE CORRECT ADDRESS PUSHED?
165514  001401                  BEQ     2$              ;BRANCH IF YES
165516  000000                  HALT                    ;WRONG THING PUSHED ON STACK
165520  012716  165530  2$:     MOV     #3$,(SP)        ;CHANGE THE ADDRESS ON THE STACK
165524  000207                  RTS     PC              ;TRY TO RETURN TO 3$
165526  000000                  HALT                    ;DID NOT RETURN PROPERLY
165530  005046          3$:     CLR     -(SP)           ;PUSH A ZERO ON THE STACK
165532  012746  165542          MOV     #4$,-(SP)       ;PUSH THE RETURN ADDRESS ON STACK
165536  000002                  RTI                     ;SEE IF AN "RTI" WORKS
165540  000000                  HALT                    ;THE "RTI" FAILED
165542  000137  165550  4$:     JMP     @#5$            ;TRY TO "JMP"
165546  000000                  HALT                    ;THE "JMP" FAILED
165550                  5$:                             ;ADDRESS$ TO "JMP" TO


                        ;!*****************************************************************
                                .SBTTL  TEST24  LOAD AND TURN ON MEMORY MANAGEMENT AND THE UNIBUS MAP
                        ;*
                        ;*      THIS TEST IS ONLY EXECUTED IF THE UPPER 4 BITS <15:12> OF
                        ;*      THE SWITCH REGISTER ARE NON-ZERO.  THE TEST WILL LOAD MEMORY
                        ;*      MANAGEMENT TO RELOCATE TO THE 32K BLOCK NUMBER SPECIFIED,
                        ;*      IT WILL ALSO SET UP THE UNIBUS MAP REGISTERS 0 THRU 6 TO
                        ;*      RELOCATE THE UNIBUS ADDRESSES CORRECTLY. (IE, IF BITS <15:12>
                        ;*      SPECIFY BLOCK NUMBER 3, THEN YOU WANT TO BOOT INTO
                        ;*      MEMORY FROM 96K TO 128K,  THE KIPAR'S WILL BE LOADED AS FOLLOWS:
                        ;*      KIPAR0 = 000000, KIPAR1 = 006200, KIPAR2 = 006400, KIPAR3 = 006600
                        ;*      KIPAR4 = 007000, KIPAR5 = 007200, KIPAR6 = 007400,)
                        ;*      KIPAR7 WILL ALWAYS EQUAL 177600.
                        ;*      THE UNIBUS MAP REGISTERS WILL THEN BE SET AS FOLLOWS:
                        ;*      MAPL0 = 000000, MAPH0 = 03, MAPL1 = 020000, MAPH1 = 03,
                        ;*      MAPL2 = 040000, MAPH2 = 03, MAPL3 = 060000, MAPH3 = 03,
                        ;*      MAPL4 = 100000, MAPH4 = 03, MAPL5 = 120000, MAPH5 = 03,
                        ;*      MAPL6 = 140000, MAPH6 = 03.
                        ;*
                        ;!*****************************************************************
165550                  TST24:
165550  013702  177570          MOV     @#SWR,R2        ;READ THE SWITCH REGISTER
165554  001002                  BNE     10$             ;SKIP THE NEXT INSTRUCTION IF NOT ZERO
165556  013702  173024          MOV     @#173024,R2     ;READ THE SWITCHES ON THE M9301
165562  072227  177770  10$:    ASH     #-2,R2          ;RIGHT SHIFT BITS <15:12> 2 PLACES
165566  042702  141777          BIC     #^C03C00,R2     ;LEAVE ONLY BITS <13:10> IN R2
165572  001433                  BEQ     TST25           ;GO TO NEXT TEST IF R2 IS ZERO NOW
                        ;*
                        ;*      THIS NEXT PORTION OF CODE WILL BE RUN ONLY IF YOU ARE
                        ;*      BOOTING INTO MEMORY OTHER THAN PHYSICAL 0 TO 28K.
                        ;*
165574  012700  172340          MOV     #KIPAR0,R0      ;ADDRESS OF FIRST "PAR" TO LOAD
165600  012701  000007          MOV     #^D7,R1         ;LOAD KIPAR0 THRU KIPAR6
165604  010220          1$:     MOV     R2,(R0)+        ;LOAD THE KERNEL I-SPACE P.A.R.'S
165606  062702  000200          ADD     #200,R2         ;MAKE R2 POINT TO NEXT 4K BLOCK
165612  077104                  SOB     R1,1$           ;LOOP UNTIL KIPAR6 HAS BEEN LOADED
165614  012710  177600          MOV     #177600,(R0)    ;MAP KIPAR7 TO I/O PAGE
                        ;*
                        ;*      NOW LOAD THE UNIBUS MAP TO REFERENCE THE SAME MEMORY
                        ;*      AS MEMORY MANAGEMENT DOES.
```

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                        ;*
165622  172227  177766        ASH     #-^D10,R2       ;RIGHT SHIFT R2 10 PLACES
165624  005003              CLR     R3              ;START WITH R3 = 000000
165626  012700  170200        MOV     #MAPL0,R0       ;ADDRESS OF FIRST MAP REGISTER
165632  012701  000007        MOV     #^D7,R1         ;PREPARE TO LOAD SEVEN MAP REGISTERS
165636  010320          2$:   MOV     R3,(R0)+        ;LOAD LOWER 16 BITS OF THE MAP REGISTER
165640  010220              MOV     R2,(R0)+        ;LOAD UPPER 6 BITS OF THE MAP REGISTER
165642  062703  020000        ADD     #20000,R3       ;POINT TO THE NEXT 4K BLOCK
165646  077105              SOB     R1,2$           ;LOOP UNTIL SEVEN MAP REGS ARE LOADED

165650  012737  000860  172516    MOV     #60,@#MMR3      ;ENABLE 22-BIT MAPPING AND UNIBUS MAP
165656  005237  177572        INC     @#MMR0          ;TURN ON FULL RELOCATION


                        ;!************************************************************************
                                .SBTTL  TEST25  TEST MAIN MEMORY FROM VIRTUAL 1000 TO 20K
                        ;*
                        ;*      THIS TEST WILL TEST MAIN MEMORY WITH THE CACHE DISABLED, FROM
                        ;*      VIRTUAL ADDRESS 001000 TO 157776.  IF THE DATA DOES NOT COMPARE
                        ;*      PROPERLY THE TEST WILL HALT AT EITHER 165740 OR 165756. IF A
                        ;*      PARITY ERROR OCCURS THE TEST WILL HALT AT ADDRESS 165776, WITH
                        ;*      THE PC + 2 ON THE STACK WHICH IS IN THE KERNEL D-SPACE P.A.R.'S.
                        ;*
                        ;*      IN THIS TEST THE REGISTERS ARE INITIALIZED AS FOLLOWS:
                        ;*      R0 = 001000, R1 = DATA READ, R2 = 067400, R3 = 001000
                        ;*      R4 = 067400, R5 = 177746 (CONTROL REG.) SP = 172376
                        ;*
                        ;!************************************************************************
165662                  TST25:
165662  010216              MOV     R2,(SP)         ;SAVE R2 FOR THE UPPER SIX BITS
                                                    ;OF THE MASS BUS DEVICE'S BUS ADDRESS
                                                    ;IN ADDRESS 17772376 (KDPAR7)

165664  012737  165776  000114    MOV     #PAEHLT,@#114   ;SET UP PARITY VECTOR
165672  005037  000116        CLR     @#116           ;SET PROCESSOR STATUS WORD TO ZERO
165676  012705  177746        MOV     #177746,R5      ;CACHE CONTROL REGISTER ADDRESS
165702  012715  000014        MOV     #MISS,(R5)      ;FORCE MISS BOTH GROUPS
165706  012702  067400        MOV     #67400,R2       ;COUNT STORAGE
165712  012703  001000        MOV     #1000,R3        ;FIRST ADDRESS STORAGE
165716  010204              MOV     R2,R4           ;SETUP COUNTER
165720  010300              MOV     R3,R0           ;SETUP FIRST ADDRESS
165722  010020          1$:   MOV     R0,(R0)+        ;LOAD EACH ADDRESS WITH ITS
                                                    ;OWN ADDRESS
165724  077402              SOB     R4,1$           ;LOOP UNTIL DONE
165726  010204              MOV     R2,R4           ;SETUP COUNTER AND FIRST ADDRESS
165730  010300              MOV     R3,R0           ;SET STARTING ADDRESS IN R0
165732  011001          2$:   MOV     (R0),R1         ;GET THE DATA
165734  020001              CMP     R0,R1           ;IS IT CORRECT?
165736  001401              BEQ     3$              ;BRANCH IF YES
165740  000000              HALT                    ;R0=ADDRESS, R1=DATA
165742  005120          3$:   COM     (R0)+           ;COMPLEMENT DATA AND INCREMENT ADDRESS
165744  077406              SOB     R4,2$           ;LOOP UNTIL DONE
165746  014001          4$:   MOV     -(R0),R1        ;READ THE DATA (IT SHOULD NOW BE THE
                                                    ;COMPLEMENT OF THE ADDRESS)
165750  005101              COM     R1              ;COMPLEMENT BEFORE CHECKING
165752  020001              CMP     R0,R1           ;IS THE DATA CORRECT?
165754  001401              BEQ     5$              ;BRANCH IF YES
165756  000000              HALT                    ;R0=ADDRESS R1=-DATA
165760  077206          5$:   SOB     R2,4$           ;LOOP UNTIL DONE
165762  012737  173762  000114    MOV     #CONT,@#114     ;SET PARITY VECTOR TO CODE THAT
                                                    ;WILL TRY TO CONTINUE AND BOOT
                                                    ;IF THE CACHE FAILS.
165770  005046              CLR     -(SP)           ;SET THE CYCLE FLAG TO ZERO
165772  000137  173600        JMP     @#TST26         ;JUMP TO SECOND HALF OF THE ROM
165776  000000          PAEHLT: HALT                    ;HALTING HERE MEANS A PARITY ERROR
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                                   .SBTTL  BOOTSTRAP ENTRY POINT IS AT 17773000
                                   ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                   ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                   ;*
                                   ;*      THE REGISTER USAGE DURING THE BOOTSTRAP IS GENERALLY AS FOLLOWS:
                                   ;*
                                   ;*      R0 = THE DRIVE NUMBER RIGHT JUSTIFIED (0 - 7)
                                   ;*      R1 = THE ADDRESS OF THE MAIN CONTROL AND STATUS REGISTER
                                   ;*      R2 = THE DRIVE NUMBER POSITIONED FOR LOADING INTO DEVICE
                                   ;*      R3 = POINTER TO THE FUNCTION TABLE
                                   ;*      R4 = INDEX NUMBER TO GET THRU THE TABLES FOR THE CORRECT INFORMATION
                                   ;*
                                   ;*
                                   ;*      AFTER A SUCCESSFUL BOOT THE REGISTERS ARE AS FOLLOWS!
                                   ;*
                                   ;*      R0 = THE DRIVE NUMBER RIGHT JUSTIFIED (0 - 7)
                                   ;*      R1 = THE ADDRESS OF THE MAIN COMMAND AND STATUS REGISTER
                                   ;*
                                   ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
                                   ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++


        173000                             . = BASE2
173000  000405                     BOOT:   BR      START             ;BRANCH TO START OF BOOT STRAP

                                   .SBTTL  CODE TO WAIT FOR TU10 TO COME ON LINE

173002  032761  000001  177776     WAIT:   BIT     #TUR,-2(R1)       ;IS THE SELECTED DRIVE ON LINE
173010  001774                             BEQ     WAIT              ;WAIT FOR BIT TO BE SET BY DRIVE
173012  000430                             BR      TU102             ;BRANCH TO CONTINUE BOOTING FROM TU10


                                   .SBTTL  THIS IS THE CODE TO READ THE SWITCH REGISTER AND DECODE IT

173014  113700  177570             START:  MOVB    @#SWR,R0          ;READ SWITCH REGISTER INTO R0
173020  001003                             BNE     1$                ;BRANCH TO DECODE IF THE LOWER
                                                                     ;BYTE IS NOT ZERO
173022  012700                             MOV     (PC)+,R0          ;IF SWITCH REGISTER IS ZERO
                                                                     ;THEN READ SWITCHES ON THE M9301
                                                                     ;TO DETERMINE DEVICE TYPE AND NO,
173024  000000                             .WORD   0                 ;THIS WORD WILL BE ASSEMBLED AT 773024
173026  006200                             ASR     R0                ;RIGHT SHIFT R0 ONE PLACE
173030  010004                     1$:     MOV     R0,R4             ;COPY DEVICE AND UNIT NUMBER
173032  042704  177407                     BIC     #^C000370,R4      ;LEAVE DEVICE NUMBER IN R4
173036  072427  177776                     ASH     #-2,R4            ;SHIFT R4 RIGHT 2 PLACES TO BE 2 - 76
173042  005744                             TST     -(R4)             ;ADJUST R4 TO INDEX THRU TABLE (0 - 74)
173044  042700  177770                     BIC     #^C7,R0           ;LEAVE UNIT NUMBER IN R0
173050  010002                             MOV     R0,R2             ;COPY UNIT NUMBER INTO R2
173052  000302                             SWAB    R2                ;PUT UNIT NUMBER IN UPPER BYTE OF R2
173054  016401  173520                     MOV     CSRPTH(R4),R1     ;LOAD MAIN CSR ADDRESS INTO R1
173060  016403  173542                     MOV     CMDPTH(R4),R3     ;LOAD POINTER TO FUNCTION TABLE
173064  000174  173564                     JMP     @ADDRS(R4)        ;JUMP TO START OF PARTICULAR BOOT


                                   .SBTTL  THIS IS THE START OF THE TM11/TU10 BOOT STRAP (MAGNETIC TAPE, TM11)
                                           ;COMMAND REGISTER ADDRESS IS 172522


173070  010211                     TU10:   MOV     R2,(R1)           ;LOAD UNIT NUMBER INTO C.S.R.
173072  000743                             BR      WAIT              ;GO WAIT FOR SELECTED DRIVE TO COME ONLINE
173074  052311                     TU102:  BIS     (R3)+,(R1)        ;'OR' REWIND COMMAND INTO C.S.R.
                                                                     ;THIS COMMAND ALSO SETS 800 BPI 9 CHAN.
173076  105711                     1$:     TSTB    (R1)              ;SEE IF THE REWIND IS COMPLETE
173100  100376                             BPL     1$                ;WAIT FOR BIT 07 OF C.S.R. TO BE SET
173102  012761  177777  000002             MOV     #-1,2(R1)         ;SET RECORD COUNTER TO SKIP ONE RECORD
173110  112311                             MOVB    (R3)+,(R1)        ;LOAD SPACE FORWARD COMMAND INTO C.S.R.
173112  105711                     2$:     TSTB    (R1)              ;SEE IF THE SPACE IS COMPLETE
173114  100376                             BPL     2$                ;WAIT FOR BIT 07 OF C.S.R. TO BE SET
173116  005711                             TST     (R1)              ;CHECK THE ERROR FLAG FOR THE TM11/TU10
173120  100563                             BMI     AGAIN             ;RE-TRY BOOT IF THERE WAS AN ERROR
173122  000417                             BR      CMNSGO            ;BRANCH TO COMMON READ CODE IF NO ERRORS


                                   .SBTTL  THIS IS THE START OF THE TC11/TU56 BOOT STRAP (DECTAPE, TC11-G)
                                           ;COMMAND REGISTER ADDRESS IS 177342

173124  010211                     TU56:   MOV     R2,(R1)           ;LOAD UNIT NUMBER INTO C.S.R.
173126  052311                             BIS     (R3)+,(R1)        ;'OR' REWIND COMMAND INTO C.S.R.
173130  005711                     1$:     TST     (R1)              ;SEE IF ERROR BIT IS SET
173132  100376                             BPL     1$                ;WAIT UNTIL BIT 15 OF C.S.R. IS SET
173134  005761  177776                     TST     -2(R1)            ;IS THE ERROR  'END ZONE'
173140  100153                             BPL     AGAIN             ;BRANCH IF NOT 'END ZONE'
173142  010211                             MOV     R2,(R1)           ;RE-LOAD DRIVE NUMBER AND CLEAR REVERSE BIT
173144  000406                             BR      CMNSGO            ;BRANCH TO COMMON READ CODE


                                   .SBTTL  THIS IS THE START OF THE RK11/RK05 BOOT STRAP (DECPACK DISK CARTRIDGE, RK11-D)
                                           ;COMMAND REGISTER ADDRESS IS 177404

173146  072227  000005             RK05:   ASH     #5,R2             ;LEFT SHIFT UNIT NUMBER 5 PLACES
173152  010261  000006                     MOV     R2,6(R1)          ;LOAD UNIT NUMBER INTO DEVICE
173156  000401                             BR      CMNSGO            ;BRANCH TO COMMON READ CODE


                                   .SBTTL  THIS IS THE START OF THE RP11/RP03 BOOT STRAP (DISK PACK, RP11-C)
                                           ;COMMAND REGISTER ADDRESS IS 176714

173160  010211                     RP03:   MOV     R2,(R1)           ;LOAD THE UNIT NUMBER INTO THE COMMAND REG.

                                   .SBTTL  THIS IS THE START OF THE COMMON READ CODE

173162  012761  177000  000002     CMNSGO: MOV     #-512.,2(R1)      ;LOAD WORD COUNT OF 512 WORDS
173170  111311                             MOVB    (R3),(R1)         ;LOAD READ FUNCTION INTO C.S.R.
173172  105711                     1$:     TSTB    (R1)              ;SEE IF FUNCTION IS COMPLETE
173174  100376                             BPL     1$                ;WAIT UNTIL BIT 07 OF C.S.R. IS SET
173176  005711                             TST     (R1)              ;WERE THERE ANY ERRORS ON THE TRANSFER
173200  100007                             BPL     2$                ;IF NO ERRORS BRANCH TO SEC. BOOT
173202  022704  000012                     CMP     #12,R4            ;IS THIS THE RH70/TU16?
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789  173206  001130                          BNE     AGAIN           ;BRANCH IF NOT TO TRY AGAIN
790  173210  022761  001000  000014          CMP     #PCE,14(R1)     ;WAS ERROR A FRAME COUNT ERROR?
791  173216  001124                          BNE     AGAIN           ;BRANCH IF NOT TO TRY AGAIN
792  173220  005011                  2$:     CLR     (R1)            ;CLEAR COMMAND REGISTER THIS WILL STOP
793                                                                  ;THE DECTAPE MOTION IF DEVICE WAS TU56
794  173222  005007                          CLR     PC              ;START SECONDARY BOOT AT VIRTUAL ZERO
795
796  173224  165000                          .WORD   165000          ;VECTOR TO THE START OF M9301 BOOTSTRAP
797  173226  000340                          .WORD   000340          ;PROCESSOR STATUS TO ASSUME AT BOOT TIME
798
799
800                                  .SBTTL  THIS IS THE START OF THE RH70/TU16 BOOT STRAP (MAGNETIC TAPE SYSTEM, TMU16)
801                                          ;COMMAND REGISTER ADDRESS IS 172440
802
803  173230  010002                  TU16:   MOV     R0,R2           ;COPY UNIT NUMBER INTO R2
804  173232  052702  001300                  BIS     #001300,R2      ;'OR' 800 BPI & FORMAT, WITH SLAVE NUMBER
805  173236  010261  000032                  MOV     R2,32(R1)       ;LOAD UNIT NUMBER
806  173242  032761  010000  000012  1$:     BIT     #MOL,12(R1)     ;IS THE MEDIUM ON LINE
807  173250  001774                          BEQ     1$              ;WAIT FOR BIT 12 OF DRIVE STATUS REG
808  173252  112311                          MOVB    (R3)+,(R1)      ;ISSUE REWIND COMMAND
809  173254  105761  000012          2$:     TSTB    12(R1)          ;IS DRIVE READY BIT SET YET?
810  173260  100375                          BPL     2$              ;WAIT FOR DRIVE READY BIT
811  173262  112311                          MOVB    (R3)+,(R1)      ;ISSUE DRIVE CLEAR COMMAND
812  173264  105761  000012          3$:     TSTB    12(R1)          ;IS DRIVE READY BIT SET?
813  173270  100375                          BPL     3$              ;WAIT UNTIL BIT 07 IS SET
814  173272  012761  177777  000006          MOV     #-1,6(R1)       ;SET SKIP COUNT TO 1 RECORD
815  173300  112311                          MOVB    (R3)+,(R1)      ;ISSUE SPACE FORWARD COMMAND
816  173302  105761  000012          4$:     TSTB    12(R1)          ;HAS THE DRIVE FINISHED THE SPACE?
817  173306  100375                          BPL     4$              ;WAIT UNTIL BIT 07 IS SET
818  173310  011661  000034                  MOV     (SP),34(R1)     ;LOAD UPPER 6 BITS OF BUS ADDRESS
819  173314  000415                          BR      CMNSRH          ;GO JOIN COMMON RH70 CODE
820
821
822                                  .SBTTL  THIS IS THE START OF THE RH70/RP04 BOOT STRAP (DISK PACK, RHP04)
823                                          ;COMMAND REGISTER ADDRESS IS 176700
824
825  173316  110061  000010          RP04:   MOVB    R0,10(R1)       ;SELECT UNIT NUMBER TO BOOT FROM
826  173322  112311                          MOVB    (R3)+,(R1)      ;ISSUE READ-IN PRESET COMMAND
827  173324  012761  014000  000032          MOV     #14000,32(R1)   ;SET FMT22 & ECC INHIBIT BITS
828  173332  011661  000050                  MOV     (SP),50(R1)     ;LOAD UPPER 6 BITS OF BUS ADDRESS
829  173336  000404                          BR      CMNSRH          ;GO JOIN THE COMMON RH70 CODE
830
831
832                                  .SBTTL  THIS IS THE START OF THE RH70/RS04 BOOT STRAP (FIXED HEAD DISK, RHS04)
833                                          ;COMMAND REGISTER ADDRESS IS 172040
834
835  173340  110061  000010          RS04:   MOVB    R0,10(R1)       ;LOAD THE DRIVE NUMBER TO BOOT FROM
836  173344  011661  000030                  MOV     (SP),30(R1)     ;LOAD UPPER  6 BITS OF BUS ADDRESS
837
838
839                                  .SBTTL  THIS IS THE START OF THE COMMON RH-70 CODE
840
841  173350  216161  000010  000016  CMNSRH: MOV     10(R1),16(R1)   ;TURN OFF ANY ACTIVE ATTENTION FLAGS
842  173356  000701                          BR      CMNBOO          ;BRANCH TO COMMON READ CODE
843
844
845                                  .SBTTL  THIS IS THE START OF THE RX11/RX01 BOOT STRAP (FLOPPY DISK)
846                                          ;COMMAND REGISTER ADDRESS IS 177170
847
848  173360  042700  000006          RX01:   BIC     #6,R0           ;MAKE SURE UNIT NUMBER IS ZERO OR ONE
849  173364  001401                          BEQ     1$              ;SKIP NEXT INST IF UNIT NUMBER IS ZERO
850  173366  005203                          INC     R3              ;POINT TO UNIT ONE'S READ COMMAND
851  173370  132711  000040          1$:     BITB    #40,(R1)        ;IS THE "DONE" BIT SET?
852  173374  001775                          BEQ     1$              ;WAIT UNTIL THE DONE BIT IS SET
853  173376  111311                          MOVB    (R3),(R1)       ;LOAD THE READ COMMAND
854  173400  012702  000002                  MOV     #2,R2           ;LOAD LOOP COUNT INTO R2
855  173404  105711                  2$:     TSTB    (R1)            ;IS THE "TR" BIT SET?
856  173406  100376                          BPL     2$              ;WAIT UNTIL BIT 07 OF RXCS IS SET
857  173410  112761  000001  000002          MOVB    #1,2(R1)        ;LOAD SECTOR NUMBER OR TRACK ADDRESS
858  173416  077206                          SOB     R2,2$           ;LOOP BACK TO LOAD SECTOR NUMBER
859  173420  032711  100040          3$:     BIT     #100040,(R1)    ;CHECK FOR "ERROR" OR "DONE"
860  173424  001775                          BEQ     3$              ;WAIT UNTIL BIT 15 OR BIT 05 OF RXCS IS SET
861  173426  100420                          BMI     AGAIN           ;BRANCH TO TRY AGAIN IF ERROR
862  173430  112711  000003                  MOVB    #3,(R1)         ;LOAD "EMPTY BUFFER" COMMAND INTO RXCS
863  173434  105711                  4$:     TSTB    (R1)            ;IS 'TR' BIT SET?
864  173436  100376                          BPL     4$              ;WAIT UNTIL BIT 07 OF RXCS IS SET
865  173440  116122  000002                  MOVB    2(R1),(R2)+     ;STORE DATA (R2 STARTS AT 0 & GOES TO 177)
866  173444  105702                          TSTB    R2              ;IS BIT 07 OF MEMORY ADDRESS SET?
867  173446  100372                          BPL     4$              ;BRANCH IF NOT 128 BYTES YET
868  173450  005007                          CLR     PC              ;START SECONDARY BOOT AT VIRTUAL ZERO
869
870
871
872                                  .SBTTL  THIS IS THE START RESERVED FOR A FUTURE DEVICE
873
874  173452  000000          FUTDEV: HALT                            ;THERE IS NO BOOT YET
875  173454  000000                  .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
876  173456  000000                  .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
877  173460  000000                  .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
878  173462  000000                  .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
879  173464  000000                  .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
880  173466  000000                  .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
881
882
883  173470  000005          AGAIN:  RESET                           ;CLEAR THE WORLD AFTER ERROR
884  173472  000137  165550          JMP     @#TST24                 ;GO SETUP MEMORY MANAGEMENT AND TEST
885                                                                  ;MAIN MEMORY AND THE CACHE AGAIN.
```

```
886
887                                     .SBTTL  FUNCTION CODES FOR THE ALL OF THE DEVICES
888
889  173476  060017                     TU10$:  .WORD   060017            ;REWIND SELECTED DRIVE AND SET 800 BPI
890  173500     011                             .BYTE   011             ;SPACE FORWARD COMMAND FOR TU10
891  173501     003                             .BYTE   003             ;READ COMMAND FOR TU10
892
893  173502  004003                     TU56$:  .WORD   004003          ;SEARCH FOR BLOCK 0, REVERSE DIRECTION
894  173504                             RK05$:
895  173504     005                     RP03$:  .BYTE   005             ;READ COMMAND FOR TU56, RK05, RP03
896
897  173505     007                     TU16$:  .BYTE   007             ;REWIND SELECTED DRIVE
898  173506     011                             .BYTE   011             ;DRIVE CLEAR COMMAND
899  173507     031                             .BYTE   031             ;SPACE FORWARD
900  173510     071                             .BYTE   071             ;READ FORWARD
901
902  173511     021                     RP04$:  .BYTE   021             ;READ-IN PRESET
903  173512     071                     RS04$:  .BYTE   071             ;READ COMMAND FOR RP04 & RS04
904
905  173513     007                     RX01$:  .BYTE   007             ;READ SECTOR COMMAND FOR DRIVE ZERO
906  173514     027                             .BYTE   027             ;READ SECTOR COMMAND FOR DRIVE ONE
907
908  173515     000                     FUTDE$: .BYTE   0               ;SPACE FOR FUTURE DEVICE COMMAND
909  173516  000000                             .WORD   0               ;SPACE FOR MORE COMMANDS
910
911
912                                     .SBTTL  COMMAND AND STATUS REGISTER ADDRESS TABLE
913
914  173520  172522                     CSRPTR: .WORD   172522          ;THIS IS THE C.S.R. ADDRESS FOR TU10
915  173522  177342                             .WORD   177342          ;THIS IS THE C.S.R. ADDRESS FOR THE TU56
916  173524  177404                             .WORD   177404          ;THIS IS THE C.S.R. ADDRESS FOR THE RK05
917  173526  176714                             .WORD   176714          ;THIS IS THE C.S.R. ADDRESS FOR THE RP03
918  173530  000000                             .WORD   0               ;THIS IS THE C.S.R. ADDRESS OF A FUTURE DEVICE
919  173532  172440                             .WORD   172440          ;THIS IS THE C.S.R. ADDRESS FOR THE RH70/TU16
920  173534  176700                             .WORD   176700          ;THIS IS THE C.S.R. ADDRESS FOR THE RH70/RP04
921  173536  172040                             .WORD   172040          ;THIS IS THE C.S.R. ADDRESS FOR THE RH70/RS04
922  173540  177170                             .WORD   177170          ;THIS IS THE C.S.R. ADDRESS FOR RX11/RX01
923
924                                     .SBTTL  FUNCTION POINTER TABLE
925
926  173542  173476                     CMDPTR: .WORD   TU10$           ;POINTER TO FUNCTION TABLE FOR THE TU10
927  173544  173502                             .WORD   TU56$           ;POINTER TO FUNCTION TABLE FOR THE TU56
928  173546  173504                             .WORD   RK05$           ;POINTER TO FUNCTION TABLE FOR THE RK05
929  173550  173504                             .WORD   RP03$           ;POINTER TO FUNCTION TABLE FOR THE RP03
930  173552  173515                             .WORD   FUTDE$          ;POINTER TO FUNCTION TABLE FOR A FUTURE DEVICE
931  173554  173505                             .WORD   TU16$           ;POINTER TO FUNCTION TABLE FOR THE RH70/TU16
932  173556  173511                             .WORD   RP04$           ;POINTER TO FUNCTION TABLE FOR THE RH70/RP04
933  173560  173512                             .WORD   RS04$           ;POINTER TO FUNCTION TABLE FOR THE RH70/RS04
934  173562  173513                             .WORD   RX01$           ;POINTER TO FUNCTION TABLE FOR THE RX01
935
936                                     .SBTTL  STARTING ADDRESS TABLE
937
938  173564  173870                     ADDRS:  .WORD   TU10            ;STARTING ADDRESS FOR THE TM11/TU10
939  173566  173124                             .WORD   TU56            ;STARTING ADDRESS FOR THE TC11/TU56
940  173570  173146                             .WORD   RK05            ;STARTING ADDRESS FOR THE RK11/RK05
941  173572  173160                             .WORD   RP03            ;STARTING ADDRESS FOR THE RP11/RP03
942  173574  173452                             .WORD   FUTDEV          ;STARTING ADDRESS FOR A FUTURE DEVICE
943  173576  173238                             .WORD   TU16            ;STARTING ADDRESS FOR THE RH70/TU16
944  173600  173316                             .WORD   RP04            ;STARTING ADDRESS FOR THE RH70/RP04
945  173602  173340                             .WORD   RS04            ;STARTING ADDRESS FOR THE RH70/RS04
946  173604  173360                             .WORD   RX01            ;STARTING ADDRESS FOR THE RX11/RX01
947
948
949                                     .SBTTL  CACHE MEMORY DIAGNOSTIC TESTS
950
951                                     ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
952                                     ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
953
954                                     ;*
955                                     ;*      THE FOLLOWING TWO TESTS ARE CACHE MEMORY TESTS, IF EITHER OF
956                                     ;*      THEM FAILS TO RUN SUCCESSFULLY THEY WILL COME TO A HALT
957                                     ;*      IN THE M9301 ROM,  IF YOU DESIRE TO TRY TO BOOT YOUR SYSTEM, OR
958                                     ;*      DIAGNOSTIC ANYWAY, YOU CAN PRESS "CONTINUE" AND THE PROGRAM
959                                     ;*      WILL FORCE MISSES IN BOTH GROUPS OF THE CACHE AND GO TO THE
960                                     ;*      BOOT STRAP THAT HAS BEEN SELECTED.
961                                     ;*
962                                     ;**************************************************************************
963                                     ;**************************************************************************
964          173606                             . = BASE2 + 606
965
966                                     ;;*************************************************************************
967                                             .SBTTL  TEST20  TEST CACHE DATA MEMORY
968                                     ;*
969                                     ;*      THIS TEST WILL CHECK THE DATA MEMORY IN THE CACHE, FIRST GROUP
970                                     ;*      0 AND THEN GROUP 1,  IT LOADS 052525 INTO AN ADDRESS COMPLEMENTS
971                                     ;*      IT THICE AND THEN READS THE DATA, THEN IT CHECKS TO INSURE THAT
972                                     ;*      THE DATA WAS A HIT,  THEN THE SEQUENCE IS REPEATED ON THE SAME
973                                     ;*      ADDRESS WITH 125252 AS THE DATA,  ALL CACHE MEMORY DATA LOCATIONS
974                                     ;*      ARE TESTED IN THIS WAY.
975                                     ;*      IF EITHER GROUP FAILS AND THE OPERATOR PRESSES CONTINUE THE
976                                     ;*      PROGRAM WILL TRY TO BOOT WITH THE CACHE DISABLED.
977                                     ;*
978                                     ;*      THE REGISTERS ARE INITIALIZED AS FOLLOWS FOR THIS TEST:
979                                     ;*      R0 = 1000 (ADDRESS) R1 = 2 (COUNT), R2 = 1000 (COUNT)
980                                     ;*      R3 = 1000 (COUNT), R4 = 125252 (PATTERN) R5 = 177746 (CONTROL REG)
981                                     ;*      SP = 172374 (FLAG OF ZERO PUSHED ON STACK)
982                                     ;*
983                                     ;;*************************************************************************
984  173606                             TST20:
985  173606  012704  125252                     MOV     #125252,R4      ;SET UP R4 FOR THIS TEST
986  173612  012715  000030                     MOV     #CRPR,(R5)      ;FORCE REPLACE GROUP 0 AND FORCE MISS GROUP 1
987  173616  010302                     1$:     MOV     R3,R2           ;SET COUNT TO CONTENTS OF R3
988  173620  010200                             MOV     R2,R0           ;SET STARTING ADDRESS INTO R0
989  173622  012701  000002             2$:     MOV     #2,R1           ;USE 2 PATTERNS IN DATA MEMORY
990  173626  005104                     3$:     COM     R4              ;COMPLEMENT DATA IN R4
```

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  991  173630  010410                        MOV     R4,(R0)         ;WRITE THE TEST PATTERN
  992  173632  005110                        COM     (R0)            ;DOUBLE COMPLEMENT DATA AND
  993  173634  005110                        COM     (R0)            ;MAKE SURE DATA IS IN THE CACHE
  994  173636  021004                        CMP     (R0),R4         ;COMPARE DATA & SET BIT 8 IN HIT/MISS REG.
  995  173640  001401                        BEQ     5$              ;BRANCH IF DATA MATCHES
  996  173642  000000                        HALT                    ;DATA DIDN'T MATCH R0 = ADDRESS
  997  173644  006037  177752       5$:     ROR     @#177752        ;WAS THE LAST MEMORY REFERENCE A HIT?
  998  173650  103402                        BCS     4$              ;BRANCH IF YES
  999  173652  000003                        HALT                    ;CACHE FAILED TO HIT R0 = ADDRESS
 1000  173654  000444                        BR      BOOTMISS        ;ABORT REST OF TEST IF "CONTINUE" PRESSED
 1001  173656  077115                4$:     SOB     R1,3$           ;GO BACK ONE TIME TO TRY COMPLEMENT DATA
 1002  173660  005720                        TST     (R0)+           ;MOVE TO NEXT ADDRESS
 1003  173662  077221                        SOB     R2,2$           ;BRANCH IF NOT DONE
 1004  173664  012715  000044               MOV     #GRP1,(R5)      ;FORCE REPLACE GROUP 1 AND FORCE MISS GROUP 0
 1005  173670  005116                        COM     (SP)            ;COMPLEMENT THE CYCLE FLAG
 1006  173672  001351                        BNE     1$              ;LOOP IF NOT DONE
 1007
 1008                                  ;!*****************************************************************
 1009                                          .SBTTL  TEST2/  TEST VIRTUAL 28K WITH CACHE ON
 1010                                  ;*
 1011                                  ;*      THIS TEST CHECKS VIRTUAL MEMORY FROM 001000 THRU 157776
 1012                                  ;*      TO INSURE THAT YOU CAN GET HITS ALL THE WAY UP THROUGH MAIN
 1013                                  ;*      MEMORY,  IT STARTS WITH GROUP 1 ENABLED, THEN TESTS GROUP 0, AND
 1014                                  ;*      FINALLY CHECKS MEMORY WITH BOTH GROUPS ENABLED.  IF ANY OF
 1015                                  ;*      THE THREE PASSES FAIL THE TEST WILL HALT AT "CONT + 2".  THEN
 1016                                  ;*      IF THE OPERATOR PRESSES "CONTINUE", THE PROGRAM WILL TRY TO
 1017                                  ;*      BOOT WITH THE CACHE DISABLED.
 1018                                  ;*
 1019                                  ;*      UPON ENTRY THE REGISTERS WILL BE SET UP AS FOLLOWS:
 1020                                  ;*      R0 = 001000 (ADDRESS), R1 = 3 (PASS COUNT), R2 = 67400 (MEMORY COUNTER),
 1021                                  ;*      R3 = 1000 (FIRST ADDRESS), R4 = 67400 (MEMORY COUNTER),
 1022                                  ;*      R5 = 177746 (CONTROL REG.), SP = 172374 (POINTING TO CODE FOR CONTROL REG)
 1023                                  ;*
 1024                                  ;*      UPON COMPLETION OF THIS TEST MAIN MEMORY FROM VIRTUAL ADDRESS
 1025                                  ;*      001000 THRU 157776 WILL CONTAIN ITS OWN VIRTUAL ADDRESS.
 1026                                  ;*
 1027                                  ;!*****************************************************************
 1028  173674                          TST27:
 1029  173674  012702  067400                MOV     #67400,R2       ;COUNT STORAGE (28K - 1000 BYTES)
 1030  173700  010300                        MOV     R3,R0           ;FIRST ADDRESS IS 1000 OCTAL
 1031  173702  010204                        MOV     R2,R4           ;SETUP COUNTER
 1032  173704  010020                1$:     MOV     R0,(R0)+        ;FILL MEMORY WITH ADDRESSES
 1033  173706  077402                        SOB     R4,1$           ;LOOP UNTIL DONE
 1034  173710  012716  000030               MOV     #GRP0,(SP)      ;LOAD CODE TO FORCE GROUP 0 ONTO STACK
 1035  173714  012701  000003               MOV     #3,R1           ;SET PASS COUNT TO THREE
 1036  173720  010300                2$:     MOV     R3,R0           ;FIRST ADDRESS
 1037  173722  010204                        MOV     R2,R4           ;COUNTER
 1038  173724  005110                3$:     COM     (R0)            ;DOUBLE COMPLEMENT DATA AND
 1039  173726  005110                        COM     (R0)            ;MAKE SURE IT IS IN THE CACHE.
 1040  173730  020020                        CMP     R0,(R0)+        ;COMPARE DATA, AND SET BIT 0 IN HIT/MISS REG
 1041                                                                  ;ALSO POINT TO NEXT ADDRESS
 1042  173732  001401                        BEQ     5$              ;BRANCH IF DATA MATCHES
 1043  173734  000000                        HALT                    ;DATA DIDN'T MATCH R0 = ADDRESS + 2
 1044  173736  006037  177752       5$:     ROR     @#177752        ;WAS THE LAST MEMORY REFERENCE A HIT?
 1045  173742  103402                        BCS     4$              ;BRANCH IF YES
 1046  173744  000000                        HALT                    ;HIT FAILED TO OCCUR R0 = ADDRESS + 2
 1047  173746  000407                        BR      BOOTMISS        ;ABORT REST OF TEST IF "CONTINUE" PRESSED
 1048  173750  077413                4$:     SOB     R4,3$           ;LOOP UNTIL DONE
 1049  173752  011615                        MOV     (SP),(R5)       ;FORCE MISS GRP1 ON PASS 2, FULLY
 1050                                                                  ;ENABLE CACHE ON PASS THREE.
 1051  173754  005016                        CLR     (SP)            ;GET READY TO FULLY ENABLE CACHE ON PASS 3
 1052  173756  077120                        SOB     R1,2$           ;RUN THREE PASSES THRU THIS TEST
 1053  173760  000404                        BR      JUMP            ;GO TO BOOT STRAP CODE
 1054
 1055
 1056  173762  000000                CONT:   HALT                    ;STOP HERE IF THERE IS A CACHE ERROR
 1057  173764  022626                        CMP     (SP)+,(SP)+     ;ADJUST STACK POINTER AFTER ABORT
 1058  173766                          BOOTMISS:
 1059  173766  012715  000014               MOV     #MISS,(R5)      ;FORCE MISSES IN BOTH GROUPS OF CACHE
 1060  173772  005726                JUMP:   TST     (SP)+           ;POINT TO UPPER SIX BITS OF BUS ADDRESS
 1061                                                                  ;THAT DATA IS IN ADDRESS 1772376 (KUPAR7)
 1062  173774  000137  173000               JMP     @#BOOT          ;GO TO BOOT STRAP ENTRY POINT
 1063
 1064
 1065          000001                .END
```

```
ADDRS   173564          733     938#
AGAIN   173470          750     782     789     791     861     883#
BASE1 = 165000            1#    116
BASE2 = 173000            1#    784     964
BOOT    173000          705#    862
BOOTHI  173766         1000    1047    1058#
CMDPTR  173542          732     926#
CMNSGO  173162          751     784     772     782#    842
CMNSRH  173350          819     829     841#
CONT    173762          674    1056#
CSRPTR  173520          731     914#
DISPLA= 177570            1#
FCE   = 001000            1#    790
FUTDEV  173452          874#    942
FUTDES  173515          908#    930
GRP0  = 000030            1#    986    1034
GRP1  = 000044            1#   1004
INDMAP  165120          250#    251
JUMP    173772         1053    1060#
KDPAR0= 172360            1#
KDPAR7= 172376            1#    557
KIPAR0= 172340            1#    495     606
KIPAR7= 172356            1#
KIPDR0= 172300            1#
KIPDR7= 172316            1#    561
MAPL0 = 170200            1#    250     271*    292     618
MISS  = 000014            1#    651    1059
MMR0  = 177572            1#    626*
MMR3  = 172516            1#    625*
MOL   = 010000            1#    806
N     = 000003          117#    118     119     124     129#    130     131     136     146#    147     148     158     168#
                        169     170     180     189#    190     191     200     209#    210     211     220     227#    228
                        229     240     256#    257     258     269     276#    277     278     289     300#    301     302
                        313     323#    324     325     335     342#    343     344     355     367#    368     369     380
                        393#    394     395     405     420#    421     422     434     451#    452     453     463     479#
                        480     481     493     516#    517     518     529     544#    545     546     554     575#    576
                        577     59      629*    630     631     642     966#    967     968     983    1008#   1009    1010
                       1027
PAEHLT  165776          648     679#
PC    =%000007          249*    558*    564*    719     794*    868*
RK05    173146          770#    940
RK05$   173304          894#    928
RP03    173160          778#    941
RP03$   173504          895#    929
RP04    173316          825#    944
RP04$   173511          902#    932
RS04    173340          835#    945
RS04$   173512          903#    933
RX01    173360          848#    946
RX01$   173513          905#    934
R0    =%000000          243*    244     357*    360     407*    410*    413*    414     436*    439*    448*    446     495*
                        498*    499     501*    502     504     506*    507     509     531*    534*    535     606*    608*
                        611*    618*    620*    621*    655*    656*    660*    661     662     665*    667     670     716*
                        719*    723*    724     728*    729     803     825     838     848*    988*    991*    992*    993*
                        994    1002    1030*   1032*   1036*   1038*   1039*   1048
R1    =%000001          244*    245     251*    295*    337*    360*    361*    382*    383     386     389*    411*    412*
                        416     457*    441*    442*    446*    465*    467     471*    473*    475*    496*    511*    532*
                        540*    607*    610*    619*    623*    661*    662     667*    669*    670     709     731*    739*
                        741*    743     745*    746*    747     749     757*    758*    759     761     763*    771*    778*
                        782*    783*    784     786     790     792*    805*    806     808*    809     811*    812     814*
                        815*    816     818*    825*    826*    827*    828*    835*    836*    841*    851     853*    855
                        857*    859     862*    863     865     989*   1001*   1035*   1052*
R2    =%000002          245*    246     438*    443*    533*    534     535     596*    598*    599*    600*    608     609*
                        616*    621     644     652*    654     659     673*    729*    738*    739     757     763     778*
                        771     778     803*    804*    805     854*    858*    865*    866     987*    988    1003*   1029*
                       1031    1037
R3    =%000003          246*    247     292*    293*    294*    295     316*    317*    318*    617*    620     622*    653*
                        655     660     732*    741     746     758     783     808     811     815     826     858*    863
                        987    1030    1036
R4    =%000004          247*    248     315*    316     383     498     499     504     654*    658*    659*    806*    724*
                        725*    726*    727     731     732     733     788     985*    990*    991     994    1031*   1033*
                       1037*   1048*
R5    =%000005          248*    849     317     386     388*    389     497*    502     507     509     650*    651*    986*
                       1004*   1049*   1059*
SP    =%000006          139*    190*    182*    242*    243     957*    500     563*    566*    567*    644*    677*    818
                        828     836    1005*   1034*   1049    1051*   1057    1060
START   173014          705     716#
SWR   = 177570            1#    596     716
TST1    165000          125#
TST10   165134          253     278#
TST11   165146          273     290#
TST12   165166          297     314#
TST13   165204          320     336#
TST14   165214          339     356#
TST15   165236          364     381#
TST16   165260          390     406#
TST17   165312          417     435#
TST2    165004          126     137#
TST20   165346          448     464#
TST21   165374          476     494#
TST22   165450          512     538#
TST23   165476          535#
TST24   165550          595#    884
TST25   165662          601     643#
TST26   173606          678     984#
TST27   173674         1028#
TST3    165020          143     159#
TST4    165036          165     181#
TST5    165052          186     201#
TST6    165066          206     221#
TST7    165076          224     241#
TUR   = 000001            1#    709
TU10    173070          739#    938
TU10$   173476          889#    926
TU102   173074          711     741#
TU16    173230          803#    943
TU16$   173505          897#    931
TU56    173124          757#    939
```

```
TU56S    173502            893#    927
WAIT     173002            709#    710     740
STN    = 000030              1#    117     126#    129     138#    143     146     160#    165     168     182#    186     189
                           202#    206     209     222#    224     227     242#    253     256     271#    273     276     291#
                           297     300     315#    320     323     337#    339     342     357#    364     367     382#    390
                           393     407#    417     420     436#    448     451     465#    476     479     495#    512     516
                           531#    544     556#    575     596#    601     629     644#    966     985#    1008    1029#
       = 174000            116#    704#    964#
COMMEN      1#     77      100     603     951
ENDCOM      1#     96      112     700     961
MSG1      117#    119
MSG10     256#    258
MSG11     276#    278
MSG12     300#    302
MSG13     323#    325
MSG14     342#    344
MSG15     367#    369
MSG16     393#    395
MSG17     420#    422
MSG2      129#    131
MSG20     451#    453
MSG21     479#    481
MSG22     516#    518
MSG23     544#    546
MSG24     575#    577
MSG25     629#    631
MSG26     966#    968
MSG27    1008#   1010
MSG3      146#    148
MSG4      168#    170
MSG5      189#    191
MSG6      209#    211
MSG7      227#    229
NXTTST      1#    117      129     146     168     189     209     227     256     276     300     323     342     367     393
          420     451      479     516     544     575     629     966     1008
SKIP        1#    126      143     165     186     206     224     253     273     297     320     339     364     390     417
          448     476      512     601
STARS       1#    117      124     129     136     146     158     168     180     189     200     209     220     227     240
          256     269      276     289     300     313     323     335     342     355     367     380     393     409     420
          434     451      463     479     493     516     529     544     554     575     594     629     642     966     983
         1008    1027
SSNXT       1#    117      129     146     168     189     209     227     256     276     300     323     342     367     393
          420     451      479     516     544     575     629     966     1008
SSSKIP      1#    126      143     165     186     206     224     253     273     297     320     339     364     390     417
          448     476      512     601
ADC       382     440      442
ADD       292     295      317     361     446     609     622
ASH       465     473      599     616     726     770
ASL       441
ASR       439     723
BCC       272
BCS       296     998     1045
BEQ       162     253      390     417     476     536     561     601     663     671     710     807     849     852     860
          995    1042
BGE       163     320      363
BGT       164     224      362     387     448
BHI       142     185      203
BHIS      184
BIC       360     600      725     728     848
BIS       316     741      758     804
BIT       386     789      806     859
BITB      851
BLE       165     223      297     364     447
BLO       319
BLOS      143     206      338     358
BLT       205     252      273     339
BMI       140     469      750     861
BNE       186     384      415     500     503     505     508     510     597     717     789     791     1006
BPL       161     408      744     748     760     762     785     787     810     813     817     856     864     867
BR        126     512      705     711     740     751     764     772     819     829     842     1000    1047    1053
BVC       183
BVS       141
CLR       139     411      566     617     649     677     792     794     808     1051
CLZ       222
CMP       383     499      535     500     662     670     788     790     994     1040    1057
CMPB      502     504      507     509
COM       294     357      388     497     665     669     990     992     993     1008    1038    1039
COMB      501     506
DEC       160     337
HALT      127     144      166     187     207     225     254     274     298     321     340     359     365     391     409
          418     449      470     477     513     537     559     562     565     569     571     664     672     679     874
          996     999     1043    1046    1056
INC       293     318      412     437     475     626     858
JMP       570     678      733     884    1062
JSR       558
MOV       242     243      244     245     246     247     248     249     436     438     495     496     498     531     532
          533     534      557     563     567     596     598     606     607     608     611     618     619     620     621
          625     644      648     650     651     652     653     654     655     656     659     660     661     667     674
          719     724      729     731     732     739     745     757     763     771     778     782     803     809     814
          818     827      828     836     841     854     985     986     987     988     989     991     1004    1029    1030
         1031    1032     1034    1035    1036    1037    1049    1059
MOVB      407     716      746     783     808     811     815     825     826     835     853     857     862     865
RESET     883
ROL       271
ROR       182     315      997    1044
RTI       568
RTS       564
SEN       204
SEZ       202
```

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SOB       410   413   443   511   540   610   623   658   666   673   858  1001  1003  1033  1048
         1052
SUB       251   389
SWAB      471   730
TST       414   416   727   749   759   761   786  1002  1008
TSTB      467   743   747   784   809   812   816   855   863   866
.BYTE     890   891   895   897   898   899   900   902   903   905   986   988
.DSABL      1
.ENABL      1
.END     1065
.ENDC     118   125   127   130   137   144   147   159   166   169   181   187   190   201   207
          210   221   225   228   241   254   257   270   274   277   290   298   301   314   321
          324   336   340   343   356   365   368   381   391   394   406   418   421   435   449
          452   464   477   480   494   513   517   530   545   555   576   595   602   630   643
          967   984  1009  1028
.EQUIV      1
.IF       117   124   126   129   136   143   146   158   165   168   180   186   189   200   206
          209   220   224   227   240   253   256   269   273   276   289   297   300   313   320
          323   335   339   342   355   364   367   380   390   393   405   417   420   434   448
          451   463   476   479   493   512   516   529   544   554   575   594   601   629   642
          966   983  1008  1027
.IFF      117   124   126   129   136   143   146   158   165   168   180   186   189   200   206
          209   220   224   227   240   253   256   269   273   276   289   297   300   313   320
          323   335   339   342   355   364   367   380   390   393   405   417   420   434   448
          451   463   476   479   493   512   516   529   544   554   575   594   601   629   642
          966   983  1008  1027
.IIF      117   118   119   124   129   130   131   136   146   147   148   158   168   169   170
          180   189   190   191   200   209   210   211   220   227   228   229   240   256   257
          258   269   276   277   278   289   300   301   302   313   323   324   325   335   342
          343   344   355   367   368   369   380   393   394   395   405   420   421   422   434
          451   452   453   463   479   480   481   493   516   517   518   529   544   545   546
          554   575   576   577   594   629   630   631   642   966   967   968   983  1008  1009
         1010  1027
.LIST       1    77    96   100   112   117   126   129   138   146   160   168   182   189   202
          209   222   227   242   256   271   276   291   300   315   323   337   342   357   367
          382   393   407   420   436   451   465   479   495   516   531   544   556   575   596
          629   644   683   700   951   961   966   985  1008  1029
.MACRO      1   117   129   146   168   189   209   227   256   276   300   323   342   367   393
          420   451   479   510   544   575   629   966  1008
.NLIST      1    77    96   100   112   117   126   129   138   146   160   168   182   189   202
          209   222   227   242   256   271   276   291   300   315   323   337   342   357   367
          382   393   407   420   436   451   465   479   495   516   531   544   556   575   596
          629   644   683   700   951   961   966   985  1008  1029
.PAGE       1    21    75   601   886   911   948
.REPT      77    96   100   112   683   700   875   951   961
.SBTTL    118   130   147   169   190   210   228   257   277   301   324   343   368   394   421
          452   480   517   545   576   630   682   707   714   736   754   767   775   788   888
          822   832   839   845   872   887   912   924   936   949   967  1009
.TITLE     13
.WORD     250   722   796   797   875   876   877   878   879   888   889   893   909   914   915
          916   917   918   919   920   921   922   926   927   928   929   930   931   932   933
          934   938   939   940   941   942   943   944   945   946

ERRORS DETECTED:  0

*DEKBHA,DEKBHA.LIS/SOL/CRF=DEKBHA.P11
RUN-TIME:  10 15 2 SECONDS
CORE USED:  9K
```

APPENDIX A
MODULE AND CONSOLE ASSEMBLY, REMOVAL, AND REPLACEMENT

No special procedures are required to disassemble and reassemble most of the components and assemblies in the H960-C cabinet or the processor mounting box. This paragraph outlines the procedures for removing and replacing modules and the steps required to disassemble the console.

A.1 MODULE REMOAL AND REPLACEMENT

The multilayer modules used in the PDP-11/70 are equipped with lock/release type handles, and each slot in the backplane has card edge and center guides that allow the modules to be installed easily. The card guides ensure that the modules are not removed or inserted at an angle so great that module or connector slots are damaged. Even though these features are provided, always install and remove the modules carefully.

A.2 CONSOLE DISASSEMBLY

Refer to Figure A-1. The following steps are required to disassemble the console:

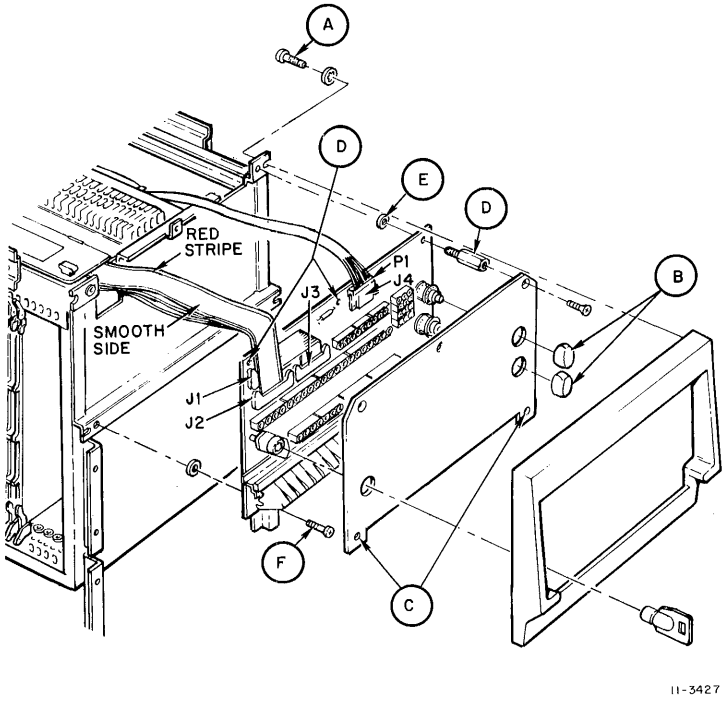


Figure A-1 Console Assembly

1. Turn power OFF at the circuit breakers.

2. Remove the four screws (A) that secure the bezel; remove the bezel.

3. Pull off the two switch knobs (B).

4. Remove the five nylon screws (C) and the console panel.

5. Unplug the harness power plug P1 from J4 and the signal cables from J1, J2 and J3.

6. Remove the three spacers (D) and the three screws (F) that hold the console PC board to the processor mounting box. Retain the six adhesive spacers (E) for reassembly.

A.3 CONSOLE REASSEMBLY

The console is reassembled by executing the steps in Paragraph A.2 in reverse order.

A.4 CONSOLE CABLES

A.4.1 Power Connector

Power is supplied to the console by processor harness plug P1. Insert this plug into console PC board connector J4.

A.4.2 Signal Connectors

Three flat signal cables connect the console to the processor modules.

1. J1 connects to J1 on M8134 (PDR, slot 10).

2. J2 connects to J1 on M8140 (SCC, slot 16); J3 connects to J2 on the same module. J1 on the M8140 is the connector closer to the edge of the module.

A.4.3 Installation of Signal Cables

The three signal cables are installed with the rough side facing the console PC board. The red stripe is on the side of the flat cable that is closer to the power harness connector J4. The smooth side of the cable faces the M8134 and M8140 modules.

APPENDIX B
REMOVAL AND REPLACEMENT OF ICs

The PDP-11/70 modules are multilayer etched circuit boards. The four layers consist of two (power and ground) internal planes, and two etched circuit external layers (Figure B-1). The inner power and ground planes form a decoupling capacitor between the power and ground planes, providing shielding between the etched circuit layers and reducing the possibility of noise and/or cross-talk. One advantage in using this type of module construction is that the need to route power and ground signals to each individual component and IC via etching on the two outer etched boards is eliminated, allowing a much greater component density on each board.

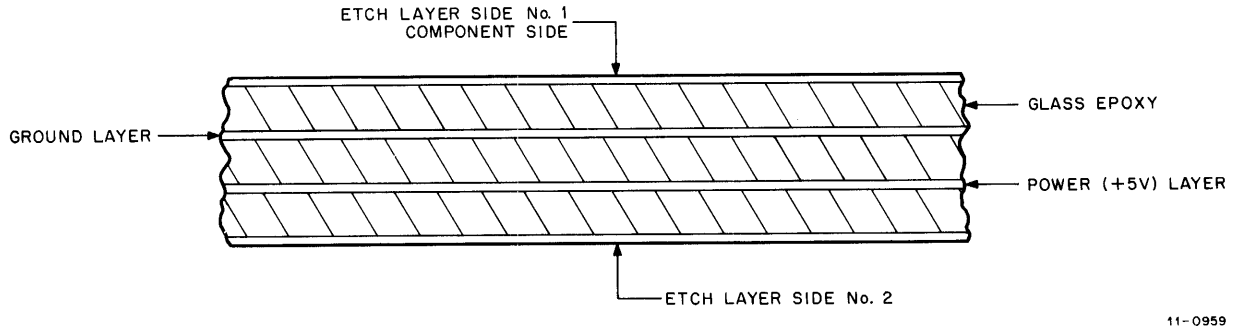


Figure B-1 Cross Section of Multilayer Board

B.1 LOCATION OF ICs

On the handle end of the board, the physical location of the last IC in each row is E-numbered to aid in locating ICs during maintenance and troubleshooting.

The first sheet of each module circuit schematic is a physical layout showing the location of the ICs and discrete components on that module.

When possible, some IC locations on most boards are not used; these spare locations, provided on a space available basis, ensure that if future ECOs (engineering change orders) involving additions are required, they can be implemented more easily.

When spare locations are provided on the module, each spare location has a number just like one of the ICs. The spare locations must also be counted when locating ICs on the board. Thus, when an IC is added to a board (e.g., because of an ECO), the IC assumes the preassigned number of the location into which it is installed. Thus, the numbered IC locations at the handle end of the board, as well as all other IC locations, always remain the same.

B.2 IC CONNECTIONS

IC and component connections to the power and/or ground inner layers are normally made as shown in Figure B-2A. The ICs and components are connected to the inner layers in this manner to allow the IC or component to be more easily replaced.

When a component is tied directly to an inner layer, as shown in Figure B-2B, instead of connecting through an etch as shown in Figure B-2A, it is difficult to remove the component because most of the heat from the soldering iron is absorbed by the inner layer, preventing the solder around the leads of the component or IC from melting. To minimize this difficulty, direct connections to the inner layer are made by a vein-type connection as shown in Figure B-3. This type of connection reduces the connected area between the plated-through hole and the inner layer. This reduces the amount of heat transfer to the inner layer when heat is applied to the plated-through hole when melting solder and removing component leads, or removing excess solder once the lead has been removed.

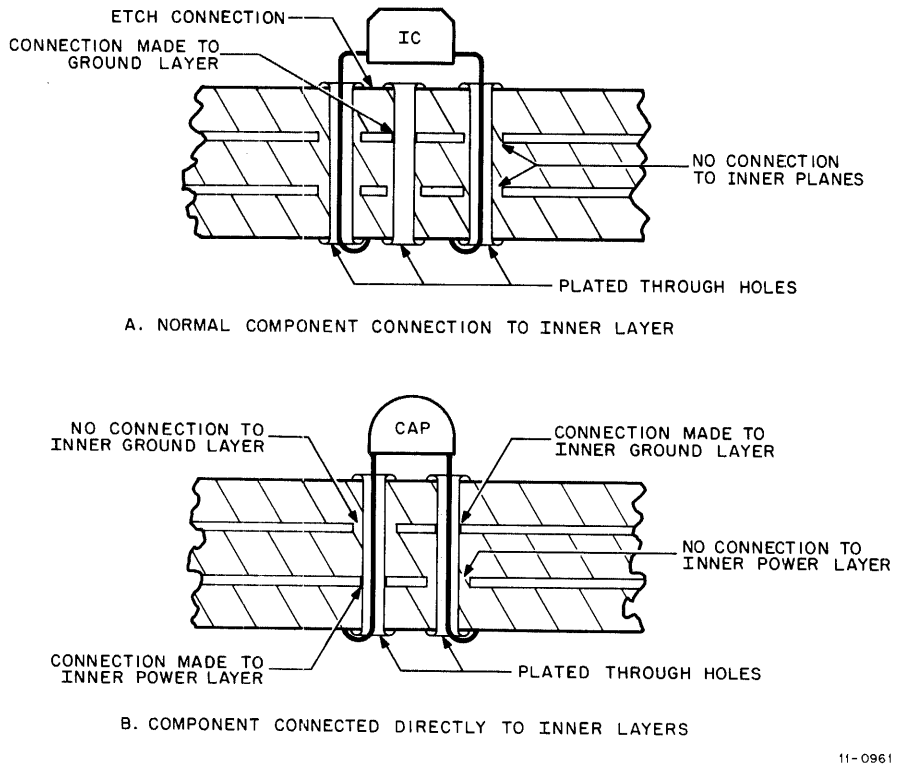


Figure B-2 Component Connections to Inner Layers

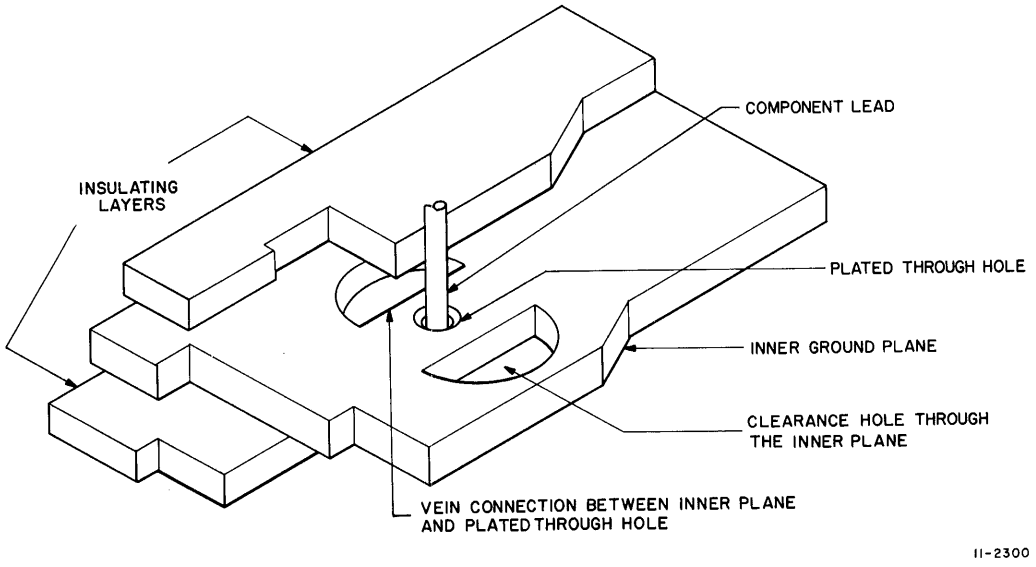


Figure B-3 Top View of Component Connection Made Directly to Inner Layer

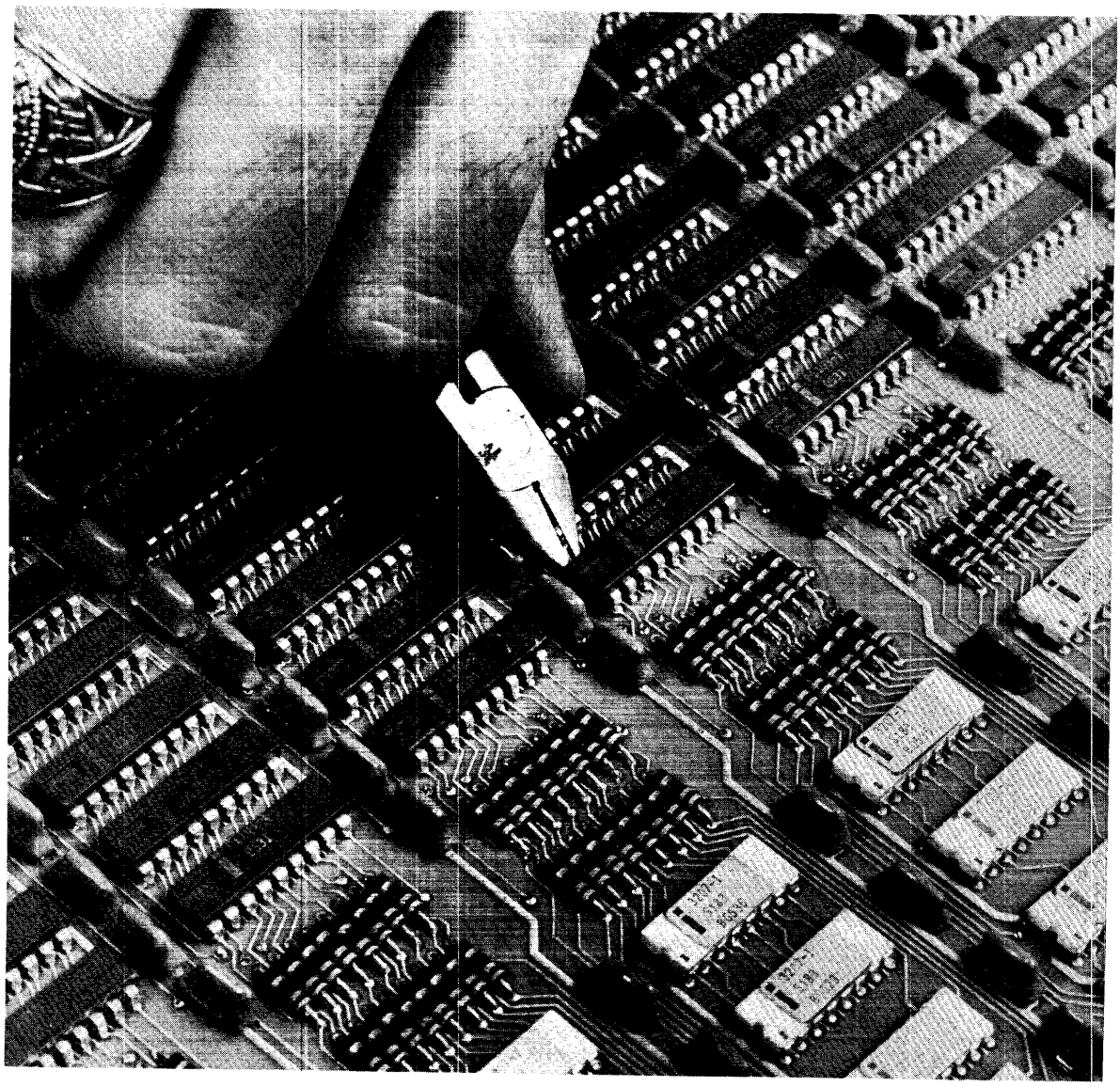
B.3 IC AND COMPONENT REMOVAL AND REPLACEMENT

Because the etch and plated-through hole eyelets are so small, extra care should be taken during the maintenance and repair of the multilayer modules, especially when soldering and unsoldering components. Certain tools (or their equivalent) are recommended for use during removal and replacement of ICs on the multilayer modules. The manufacturer and type of part number of each tool is indicated in the list below:

Small diagonal cutters, Utica No. 47-4
Soldering iron, Paragon No. 615
Pliers, Utica No. 23-4

B.4 REMOVAL AND REPLACEMENT OF PLASTIC CASE ICs

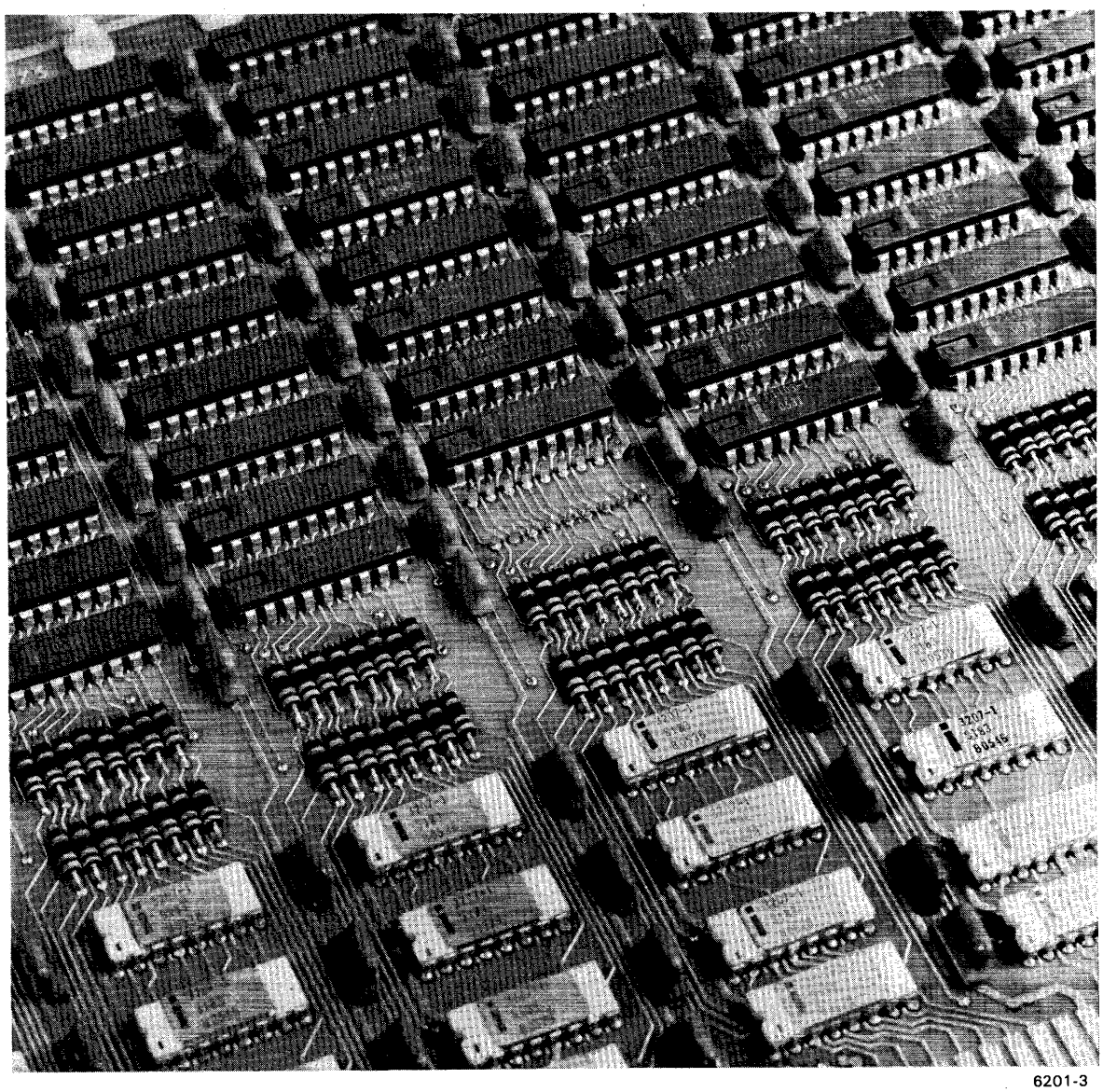
To remove and replace a plastic case IC and to preclude damage to the multilayer board, the procedure described by Figures B-4 through B-10 should be strictly adhered to.



6201-2

Figure B-4 Removing a Defective IC From the Module

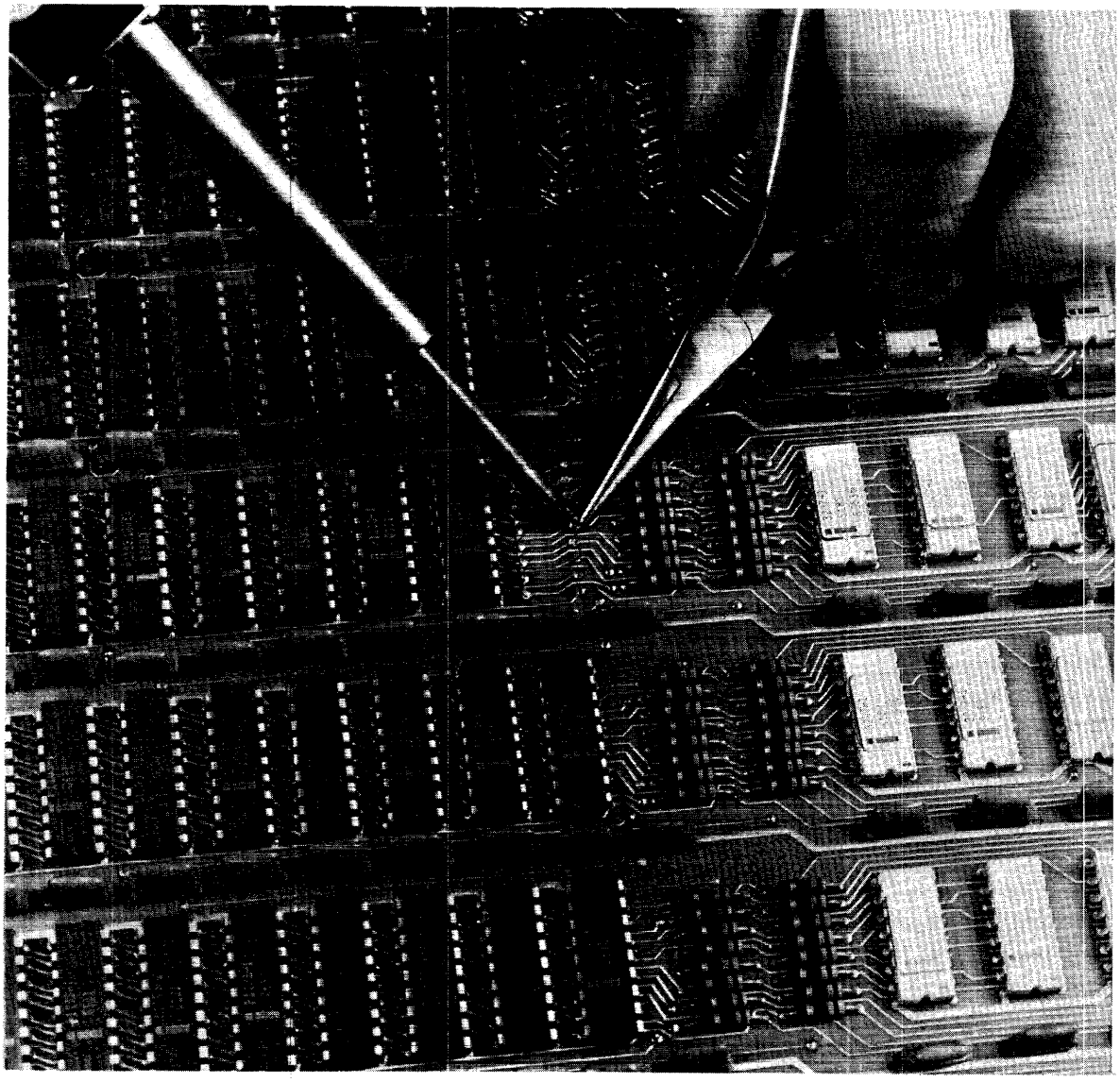
Defective IC leads are clipped, using small diagonal cutters (Utica, Part No. 47-4). Cut the leads as close to the body of the IC as possible to allow the remaining leads to be removed more easily.



6201-3

Figure B-5 Defective IC Removed

IC location after the IC has been removed – with the IC leads still in the board. Locate the leads of the IC just removed on the soldered (back) side of the board and cut all leads to avoid difficulty during their removal.



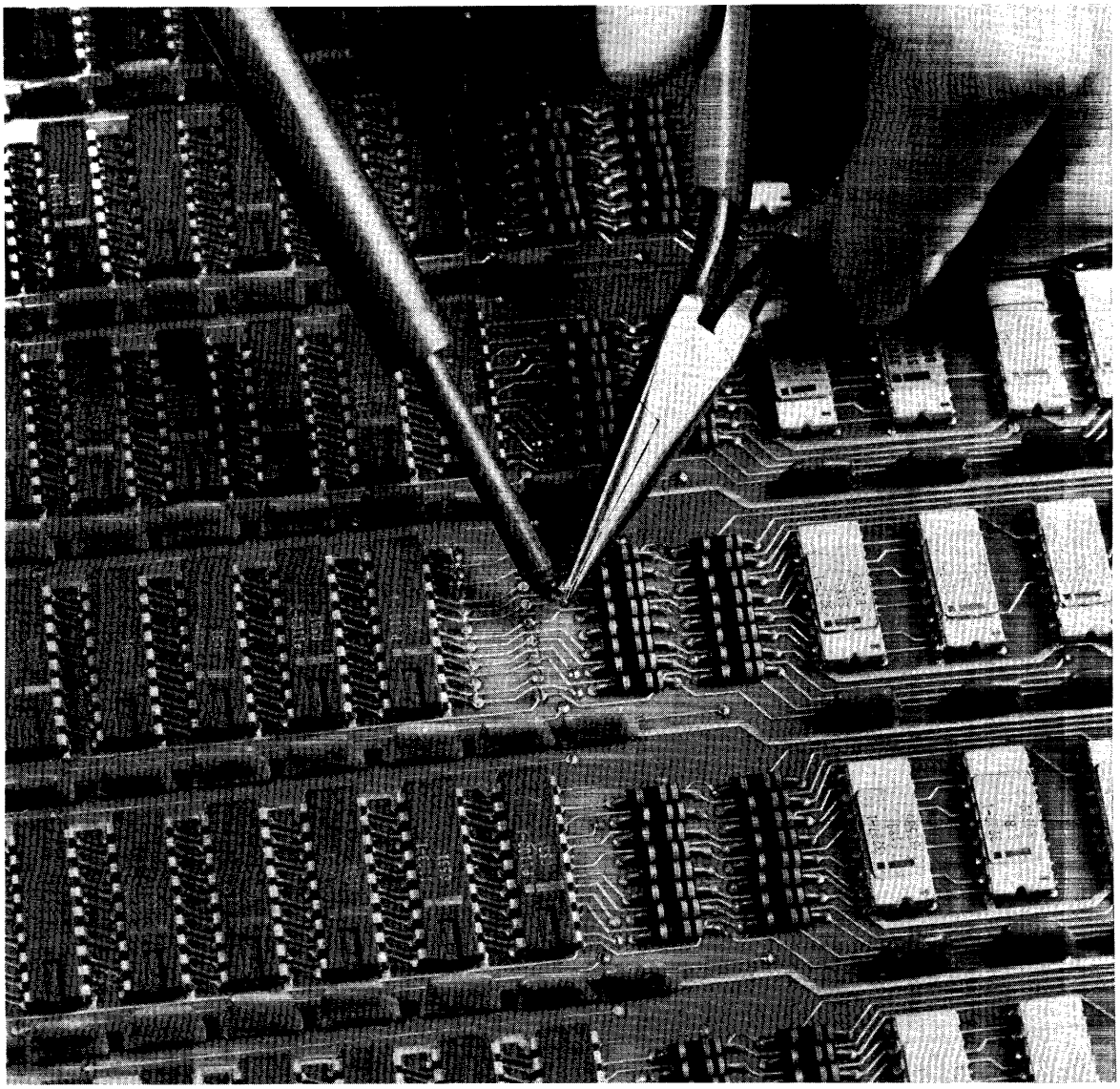
6201-4

Figure B-6 Removing IC Leads

IC leads being removed from side 1 of the board. Apply heat to the lead until the lead becomes loose. Then remove the lead by pinching with the soldering iron (Paragon, Part No. 615) and pliers (Utica, Part No. 23-4).

CAUTION

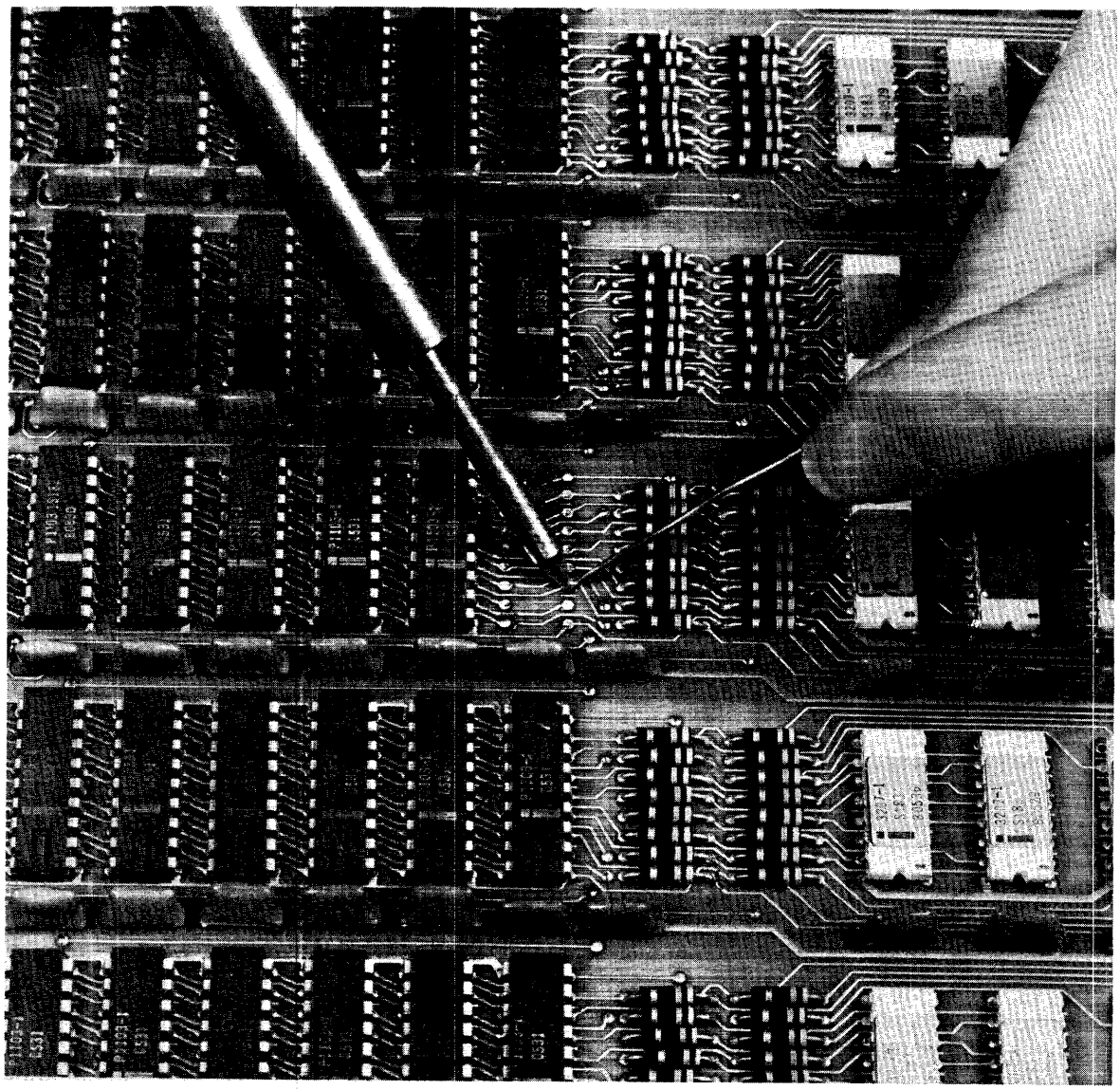
Leads that are connected to an inner layer require more heat because much of the heat is absorbed by the inner layer. It is helpful to add solder to the lead first causing more heat to be conducted to the solder in the eyelet around the lead.



6201-5

Figure B-7 IC Lead Removed

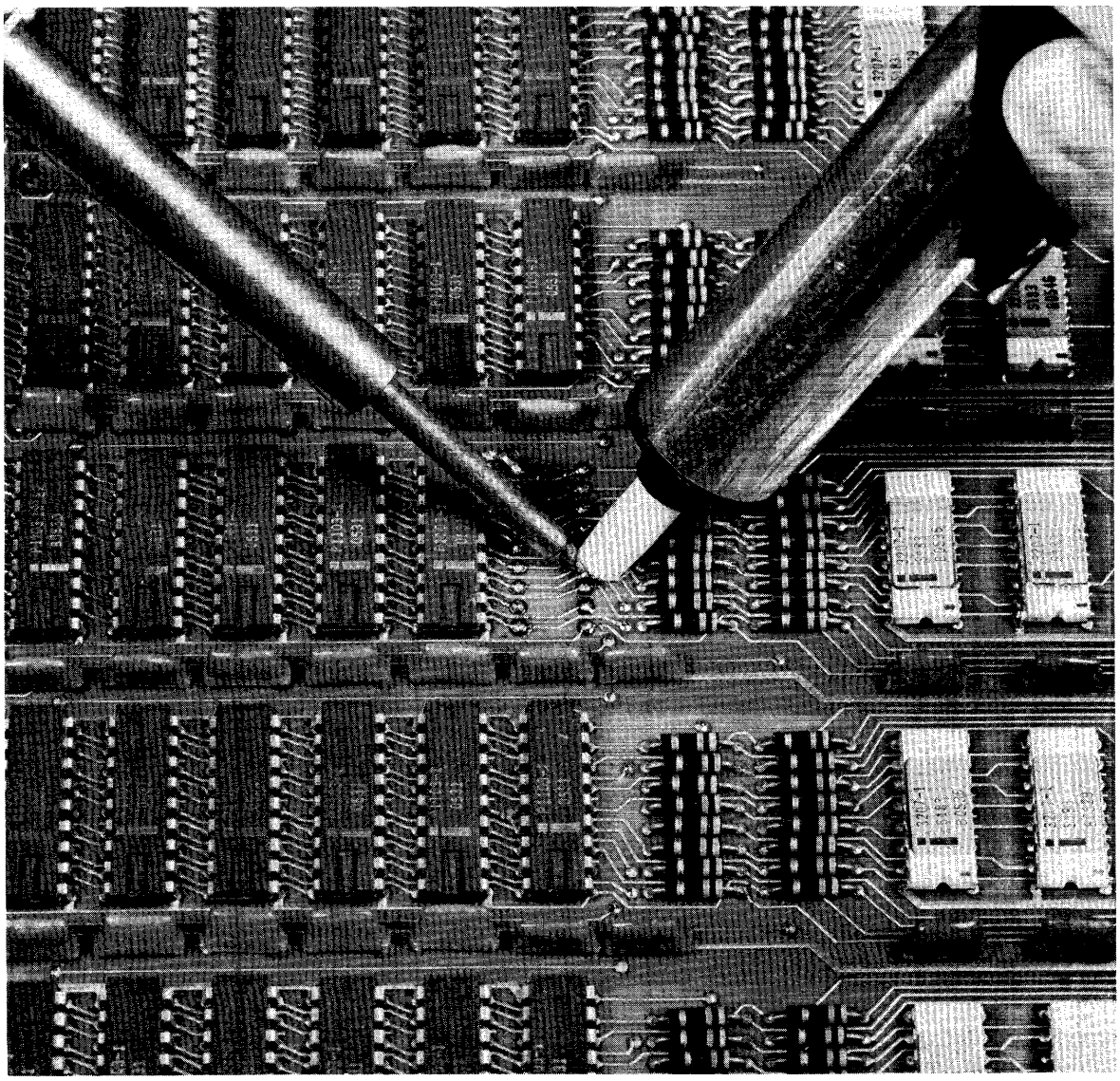
Lead directly after removal from the eyelet using the soldering iron and pliers.



6201-6

Figure B-8 Applying Solder to Refill Eyelet

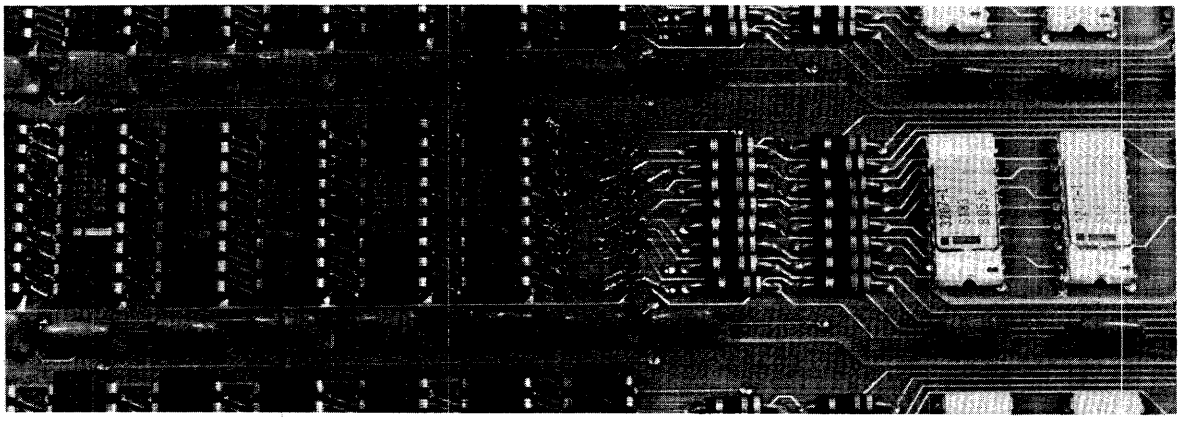
After all of the IC leads have been removed, remove the excess solder remaining in the eyelets prior to inserting the new IC. This figure shows solder being applied to the eyelets after all the leads have been removed. The extra solder absorbs excess heat and keeps it from being applied directly to the etch of the plated-through holes.



6201-9

Figure B-9 Removing Excess Solder From Eyelet

Once the eyelets have been refilled with solder, as described in Figure B-8, remove the solder using the soldering iron and solder extractor as shown above. In this figure, the eyelet has no connection to the board inner layers; thus, the solder can be extracted from the same side of the module to which the heat is applied. However, in cases where direct connections to the inner layer are made, heat must be applied to one side of the module and the solder must be extracted from the opposite side due to the heat sinking properties of the inner layers. In this case, the module should be in a vertical position to allow access to both sides of the module simultaneously.



6201-8

Figure B-10 IC Location Ready for Insertion of New IC

IC location after all the eyelets have been cleared of solder.

1. Inspect the eyelets to ensure that no excess solder remains. If all the solder is not removed, refill the hole as described in Figure B-8 and remove the solder again as described in Figure B-9. Continue this procedure as required, until all of the eyelets are cleared of excess solder.

2. Use a cleaning solvent and brush to clean the IC location of any excess solder flux.

3. Thoroughly inspect the IC location and surrounding area for solder splash and damage to etch lines and plated-through holes.

4. Ensure that none of the leads is bent, and insert the replacement IC in the holes. When inserting the replacement IC into place, avoid ending the leads on the opposite side of the module; this makes future removal of the IC easier, should it be necessary.

CAUTION

If the leads must be bent to hold the IC in position for soldering, avoid bending the leads more than 45 degrees, using only one lead at each end and on opposite sides of the IC.

5. Solder in the new IC from the opposite side of the module. Use enough solder to fill the holes and make a good connection. Avoid using an excess of solder to prevent overflow on the top side of the board, which could cause a short under the body of the IC.

6. Once all the solder connections are made, clean and inspect the area for any damage. Cut off IC leads close to the board. Take necessary corrective action for any defects that are found.

CAUTION

After installing the ECO or replacing a faulty IC on a module, ensure that no short circuit exists between the power and ground planes of the module. Do this before replacing the module in the equipment.

APPENDIX C
EQUIPMENT CONFIGURATION AND REVISION STATUS LABELS AND SHIPPING FORMS

The following paragraphs describe the MUL sticker, the ECO status sticker, and module revision status. The MUL sticker lists the equipment complement system serial number, etc.; the ECO status sticker provides information about the current ECO status of wire-wrap devices; module revision status shows the current ECO status of the module.

C.1 MECHANICAL STATUS STICKER

See Figure C-1. This sticker is located on the rear of the mounting box. Box type is PDP-11/70, H960-X. A letter designates the revision level at manufacturing. Field installed ECOs should be entered as performed.

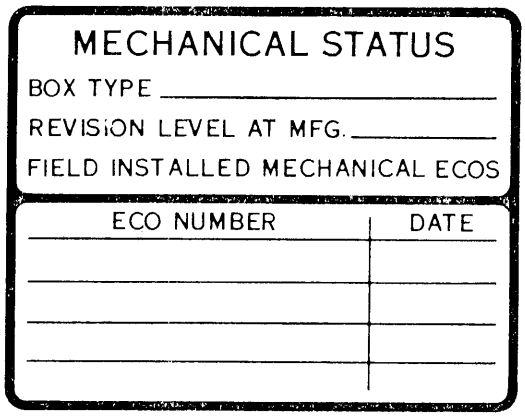


Figure C-1 Mechanical Status Sticker

C.2 ECO STATUS STICKER

The ECO status sticker, Figure C-2, is located on the inside of the module door in the CPU or BA11-FB mounting box. This sticker is filled out for installation of ECOs to wire-wrap devices such as the KB11-B, C or the various system units. Table C-1 describes how the various columns are to be filled out and the department responsible for filling out these items.

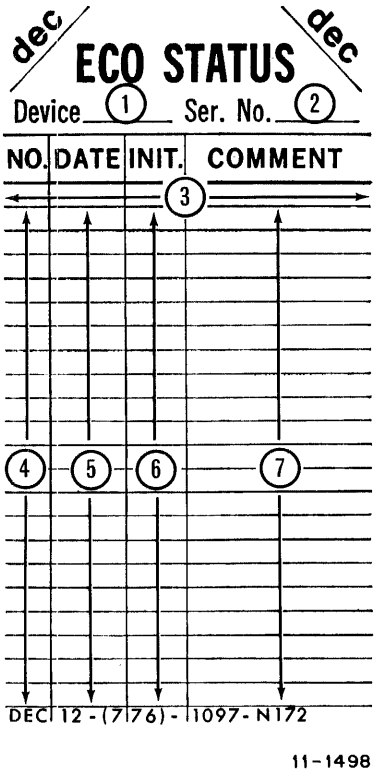


Figure C-2 ECO Sticker

Table C-1 Completing the ECO Status Sticker

Item No.	Responsibility	Description
1	Production	Option designation code for applicable device.
2	Production	Device serial number.
3	Production	Original wire wrap revision letter (e.g., ORIGINAL REV. B.)
4	Production/Field Service*	Numerical portion of ECO/FCO number
5	Production/Field Service*	Installation date of ECO/FCO.
6	Production/Field Service*	Initials of person installing ECO/FCO.
7	Production/Field Service*	Necessary comments about ECO/FCO or its installation, (e.g., only part 2 installed).

*If an option is installed in the factory, production has responsibility for filling out an ECO sticker. If the option is an add-on in the field, field service will fill out items 4 through 7.

NOTE: ECO Status Sticker is located on the inside of the module door of the mounting boxes.

C.3 MODULE ECOs

Each module is stamped with the alphabet (except for G, I, and O) to record various circuit schematic revisions to a module. When a module is shipped from the factory, the actual revision letter from production is stamped on the handle. When ECOs that revise modules are installed in the field, scratch off the appropriate letters from the module. For example, if an ECO corresponding to revision F of the module was installed and an ECO corresponding to revision E of the module was not installed, the letter F would be scratched out and the letter E would remain intact.

C.4 MODULE UTILIZATION LIST (MUL) STICKER

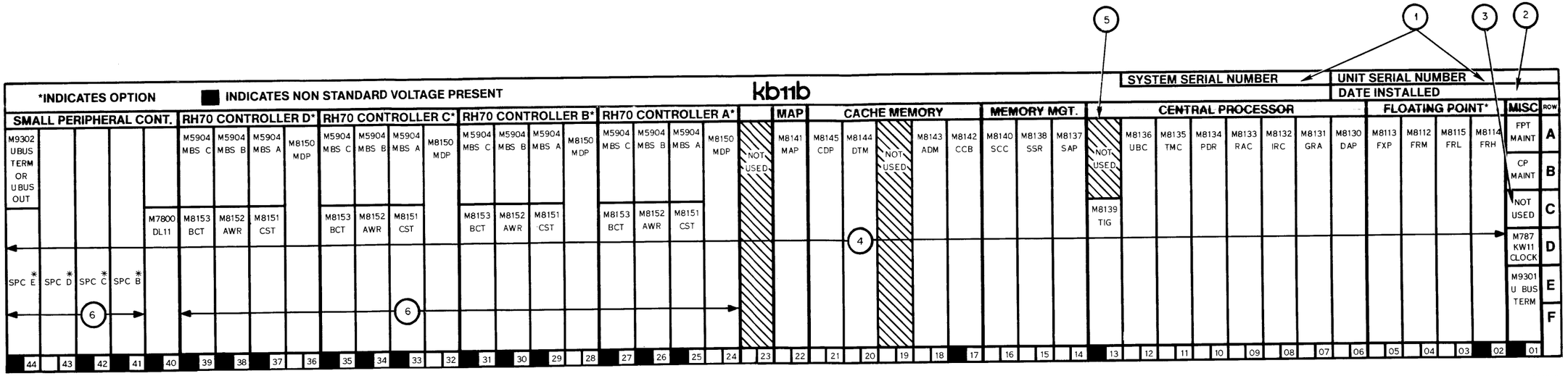
This sticker, Figure C-3, located on the top panel of the A11-FA mounting box (left-hand side), provides a quick, convenient tabulation of the various equipments located in a particular system. Additional information such as serial number, comments, technical tips, and installation of partial ECOs is also shown on the sticker. Table C-2 describes the manner in which the sticker is to be filled out and indicates the department (production/field service) responsible for filling out the various items.

Table C-2 Completing MUL Sticker

Item No.	Responsibility	Description
1	Production	System Serial Number, Unit Serial Number
2	Field Service	Acceptance Date of installation at customer site
3	None	Not Used
4	Field Service	Comment area. Note ECO/FCOs installed, partial ECO/FCOs, miscellaneous information about module or slot.
5	None	Not Used
6	Production/Field Service*	Enter device type as installed.

*To be filled out by production if option or device is factory installed. If option or device is an add-on in the field, field service will complete these items.

NOTE: The MUL Sticker is located on the top of the KB11-B, C cover over the modules.



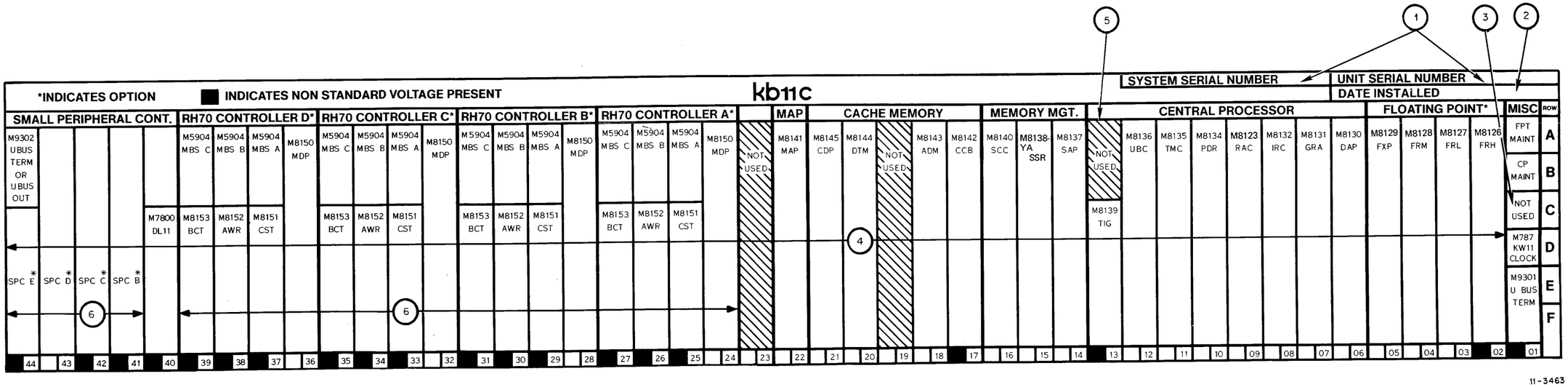


Figure C-3 MUL Stickers

APPENDIX D
IC DESCRIPTIONS

The following ICs are described in this appendix. The S or H version of an IC listed below merely indicates its a high-speed version.

3101	Random Access Memory
7474	D-Type Edge-Triggered Flip-Flops
7485	4-Bit Comparator
8598	Read-Only Memory
74112	Dual J–K Edge Triggered Flip-Flops
74151	8-Line to 1-Line Multiplexer
74153	Dual 4-Line to 1-Line Data Selectors/Multiplexers
74154	4-Line to 16-Line Demultiplexer
74155	3-Line to 8-Line Decoder
74157	Quadruple 2-Line to 1-Line Multiplexer
74158	Quadruple 2-Line to 1-Line Multiplexer
74161	4-Bit Binary Couner
74174	HEX D-Type Flip-Flops
74175	Quad D-Type Flip-Flops
74181	4-Bit Arithmetic Unit with Full Look-Ahead
74182	Look-Ahead Carry Generator
74187	1023-Bit Read-Only Memory
74191	4-Bit Binary Counter
74193	4-Bit Binary Counter
74194	Parallel Access Shift Register with Mode Control

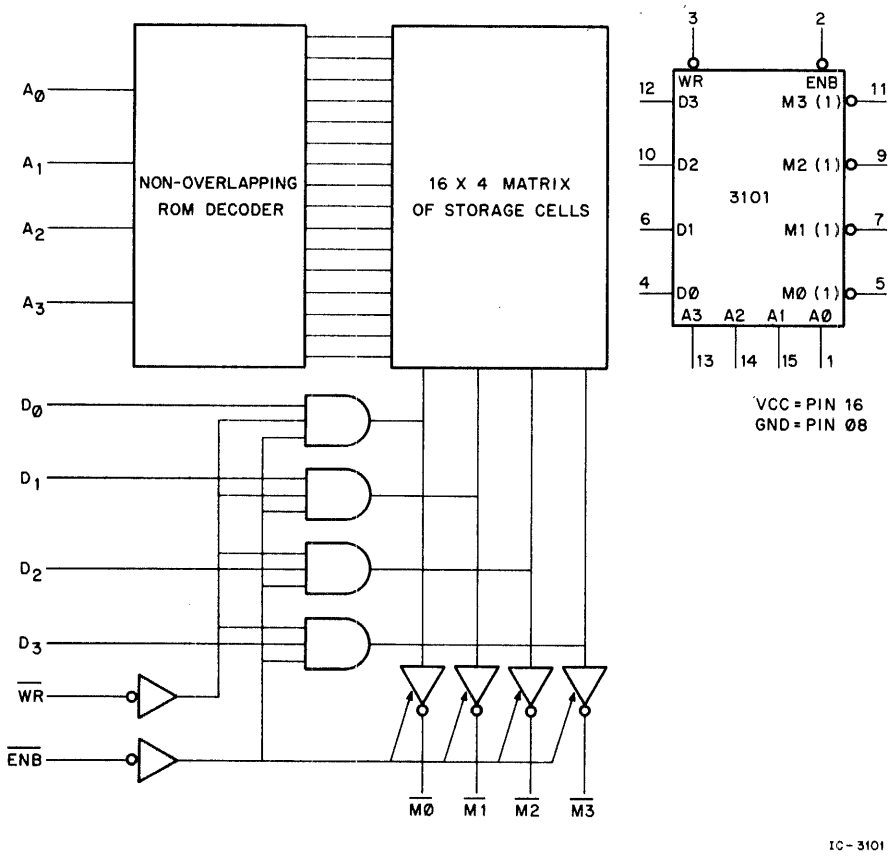
3101 16-WORD ×4-BIT MEMORY

Easy memory expansion is provided by an active LOW chip select (ENB) input and open collector OR tieable outputs.

An active LOW Write line WR controls the writing/reading operation of the memory. When the chip-select and write lines are LOW the information on the four data inputs D_0 to D_0 is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs M0 to M3.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

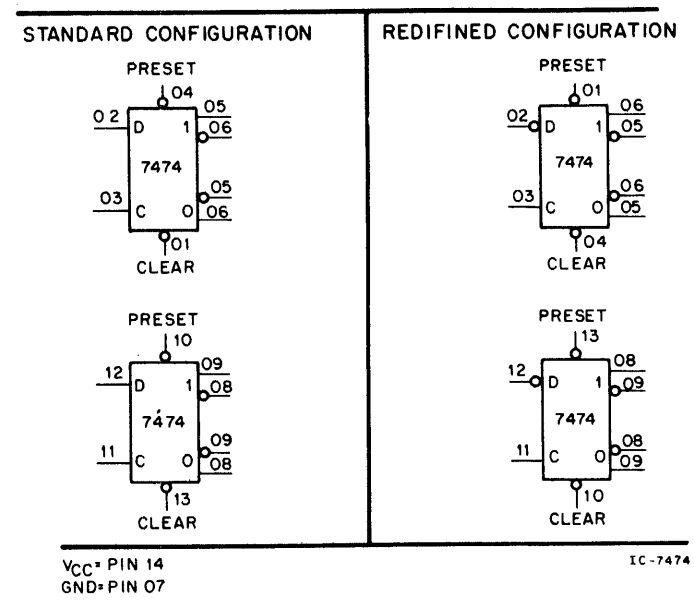


7474 DUAL FLIP-FLOP

TRUTH TABLE FOR
7474 STANDARD CONFIGURATION
(EACH FLIP-FLOP)

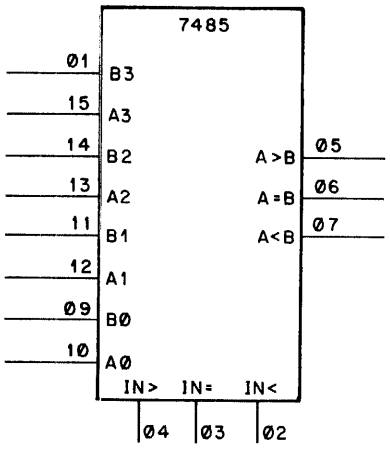
t_n			t_n+1	
Preset Pin 4(10)	Clear Pin 1(13)	D Input Pin 2(12)	1 Side Pin 5	0 Side Pin 6
High	High	Low	Low	High
High	High	High	High	Low
High	Low	X	Low	High
Low	High	X	High	Low
Low	Low	X	High	High

t_n = bit time before clock pulse.
t_n+1 = bit time after clock pulse.
X = irrelevant



7485 4-BIT COMPARATOR

The 7485 performs magnitude comparison of straight binary or straight BCD codes. Three fully decoded decisions (A > B, A < B, A = B) about two 4-bit words (A,B) are made and externally available at three outputs.



VCC = PIN 16
OND = PIN 08

TRUTH TABLE

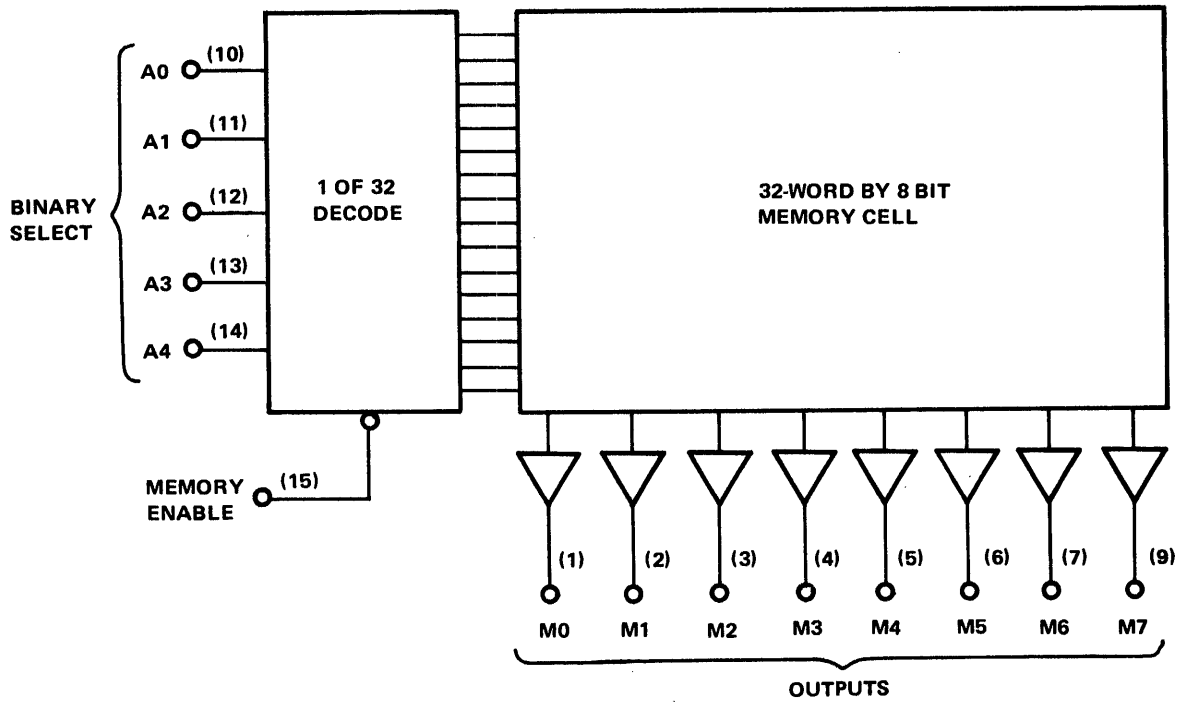
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	IN >	IN <	IN =	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

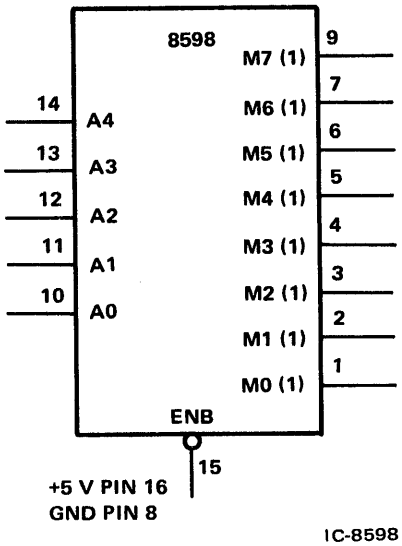
NOTE: H = high level, L = low level, X = irrelevant

IC-7485

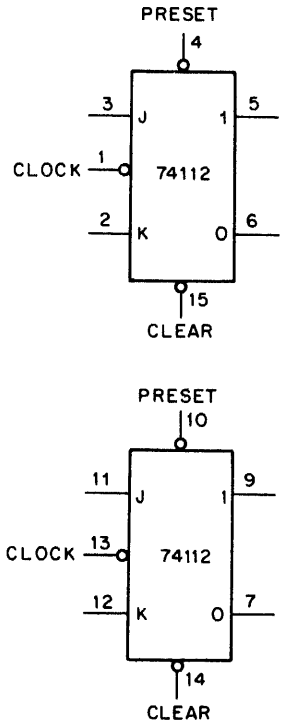
8598 READ-ONLY MEMORY

The 8598 is a 256-bit, read-only memory organized as 32 words of eight bits each. Addressing is accomplished in straight 5-bit binary with full decoding. An overriding memory enable input is provided which, when taken high, will inhibit the 32 address gates and cause all eight outputs to remain high.





74112 DUAL J-K FLIP-FLOP



74112 Truth Table

t_n		t_{n+1}
J	K	Pin 5 or 9
L	L	No change
L	H	L
H	L	H
H	H	Complement

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

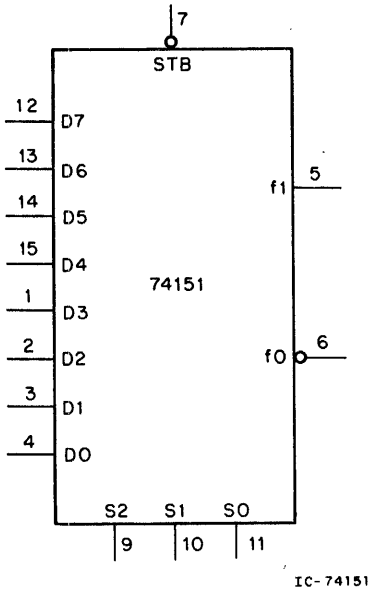
IC-74112

74151 8 TO 1 MULTIPLEXER

74151 TRUTH TABLE

Inputs												Outputs	
S2	S1	S0	STB	D0	D1	D2	D3	D4	D5	D6	D7	f1	f0
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

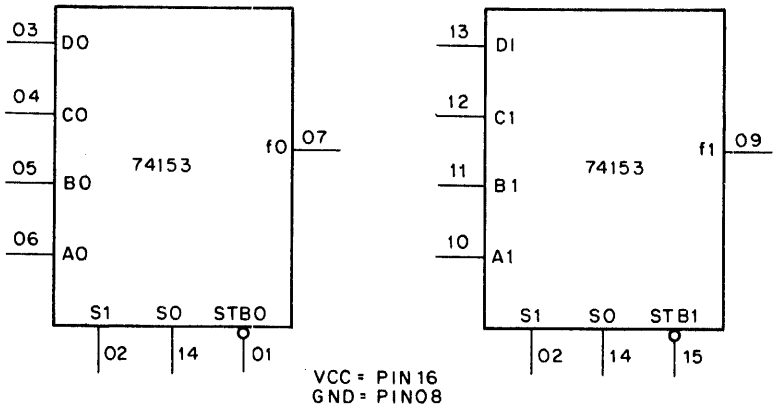
When used to indicate an input, X = irrelevant.



74153 DUAL 4 TO 1 MULTIPLEXER

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
S1	S0	A	B	C	D	STB	f
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

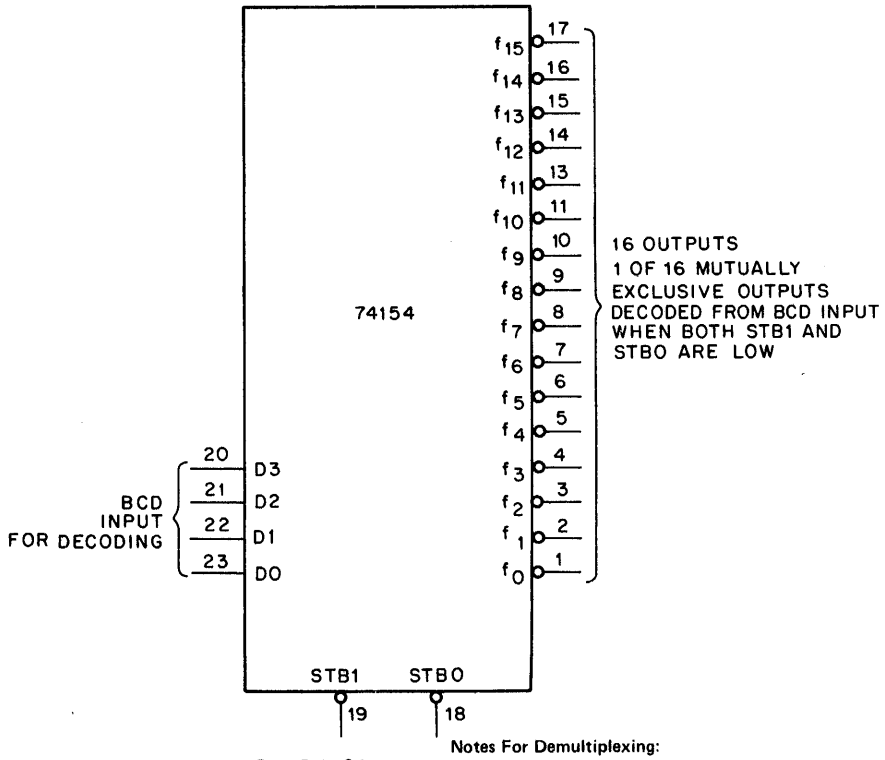
Address inputs S0 and S1 are common to both sections.
H = high level, L = low level, X = irrelevant.



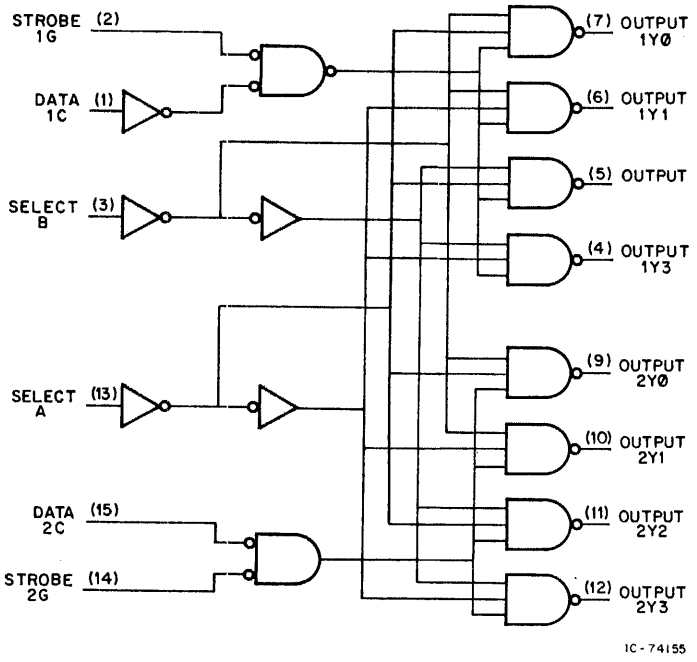
IC-74153

74154 4-LINE TO 16-LINE DECODER

The 74154 4-Line to 16-Line Decoder decodes four binary-coded inputs into one of 16 mutually-exclusive outputs when both strobe inputs (G1 and G2) are low. The decoding function is performed by using the four input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.



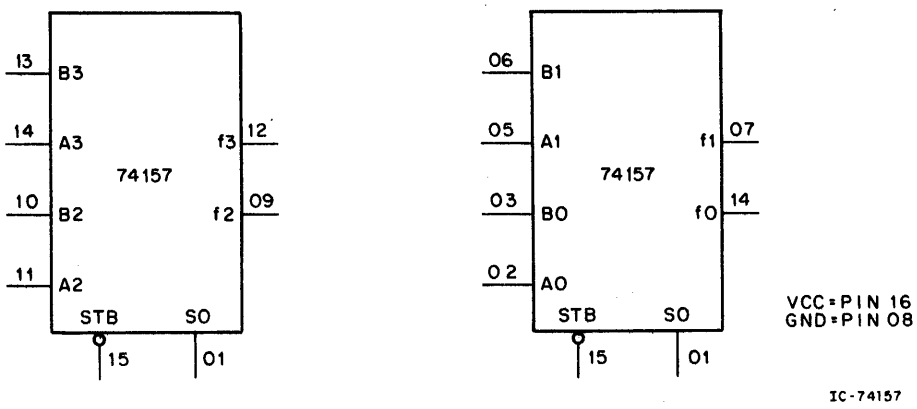
74155 3-LINE TO 8-LINE DECODER



74157 QUAD 2 TO 1 MULTIPLEXER

INPUTS				OUTPUT
STB	S0	A	B	f
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

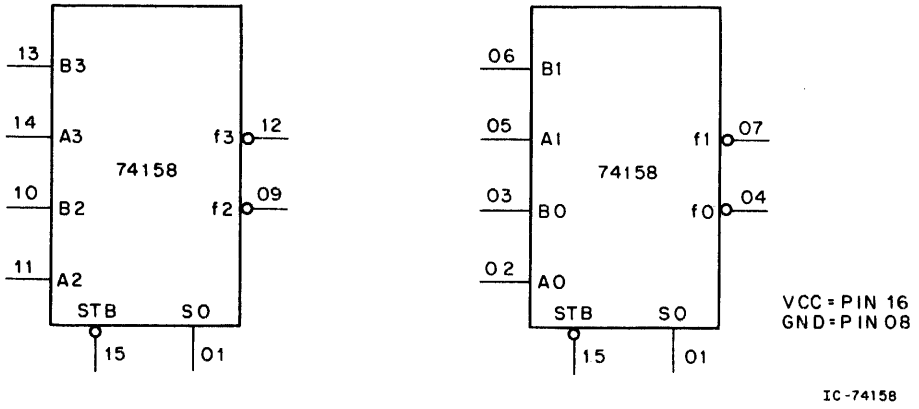
H = high level, L = low level, X = irrelevant.



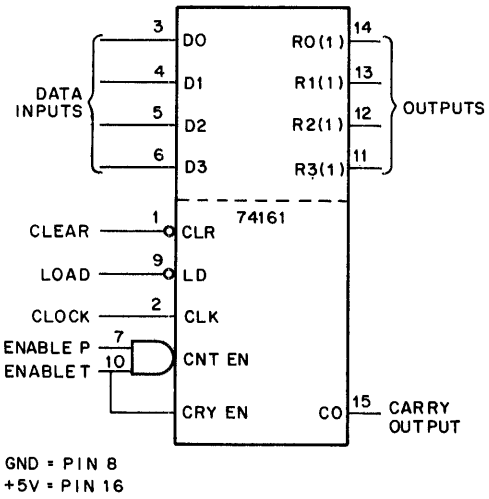
74158 QUAD 2 TO 1 MULTIPLEXER

INPUTS				OUTPUT
STB	S0	A	B	f
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant.



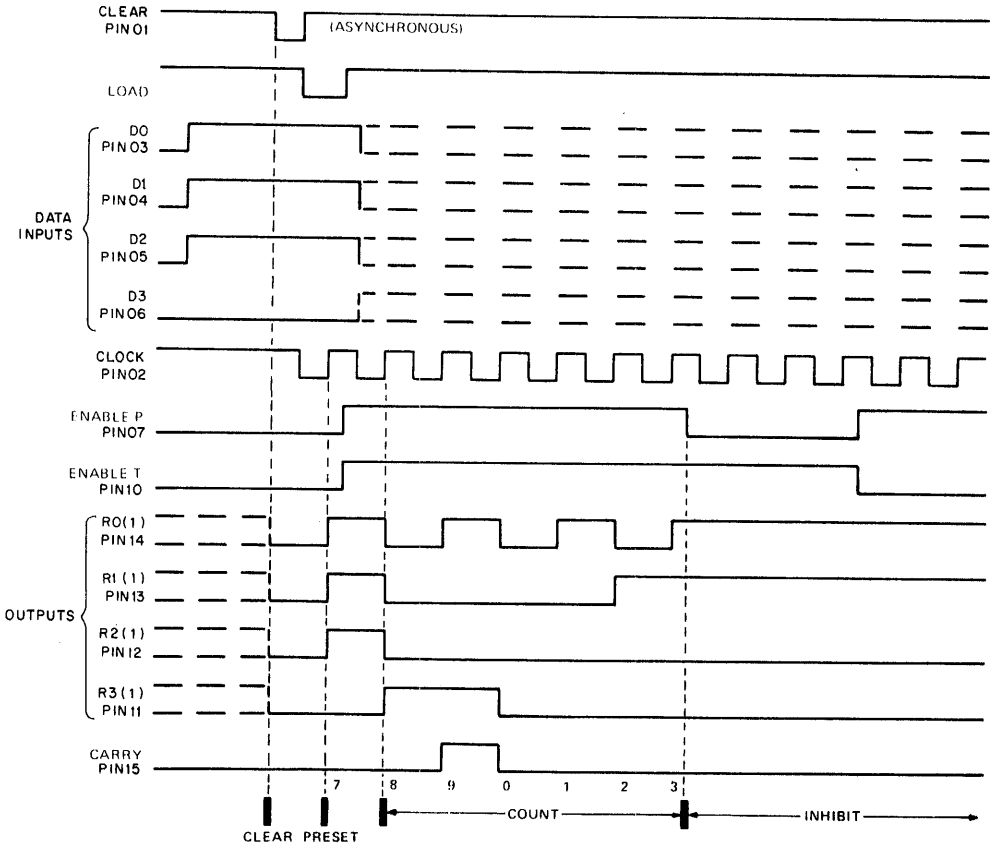
74161 SYNCHRONOUS 4-BIT COUNTER



typical clear, preset, count, and inhibit sequences for 74161

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



IC-74161

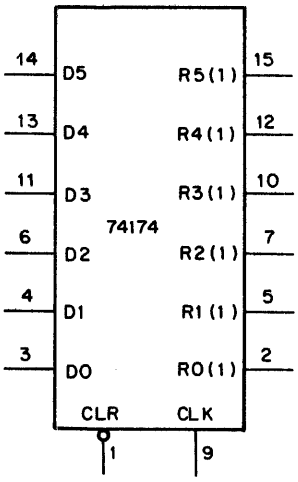
74174 HEX D FLIP-FLOP REGISTER

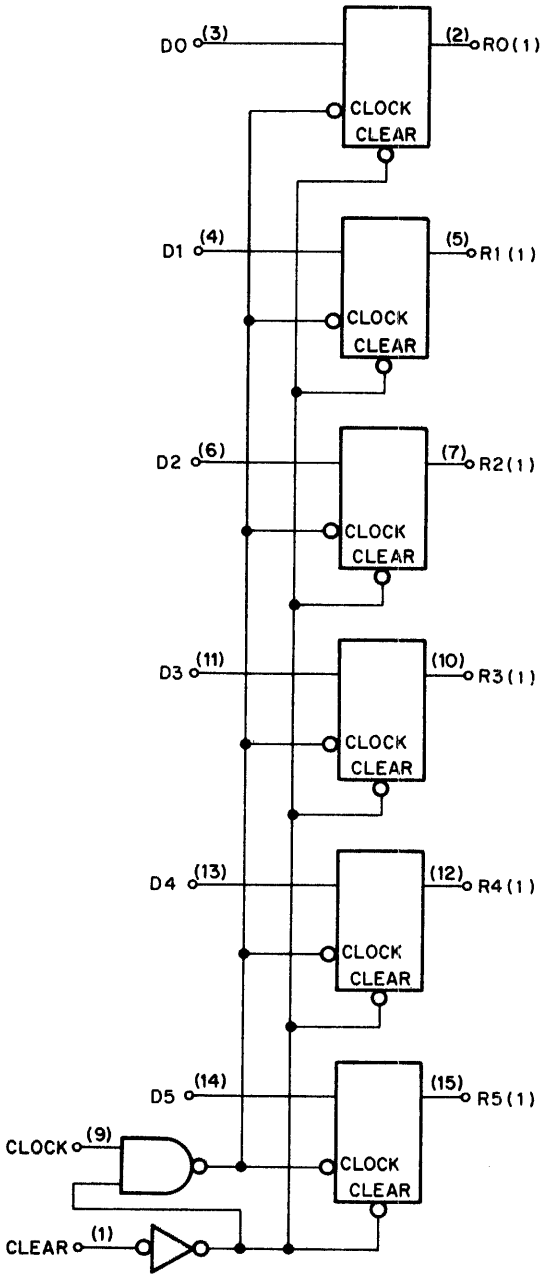
TRUTH TABLE

INPUT t_n D	OUTPUT t_{n+1} R(1)
H	H
L	L

t_n = Bit time before clock pulse.

t_{n+1} = Bit time after clock pulse.





Pin (16) = V_{CC}, Pin (8) = GND

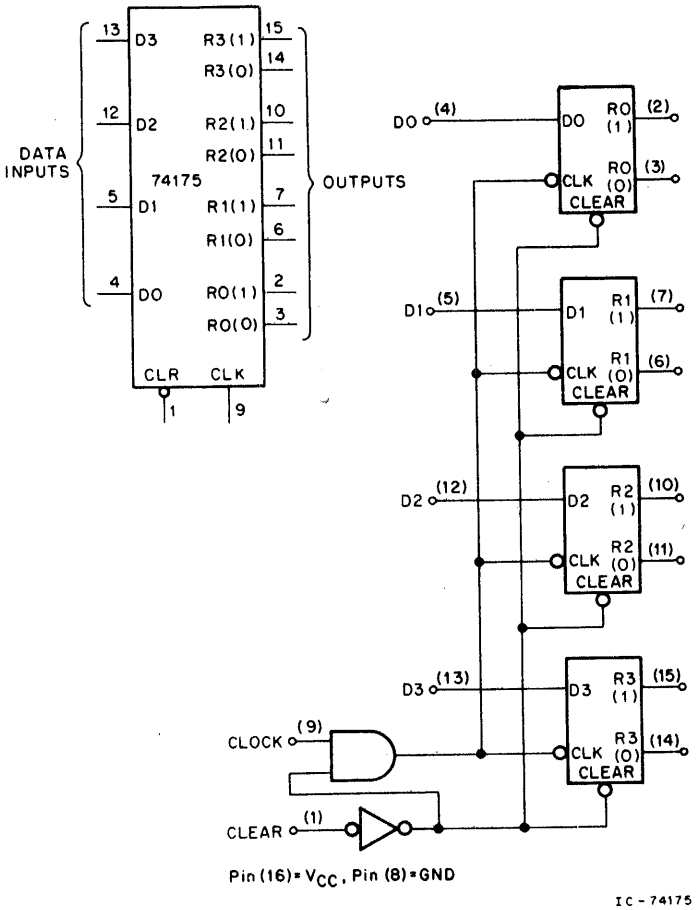
IC-74174

74175 QUAD STORAGE REGISTER

TRUTH TABLE

INPUT t_n D	OUTPUTS t_{n+1} R(1) R(0)
H	H L
L	L H

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.



Pin (16) = V_{CC}, Pin (8) = GND

IC - 74175

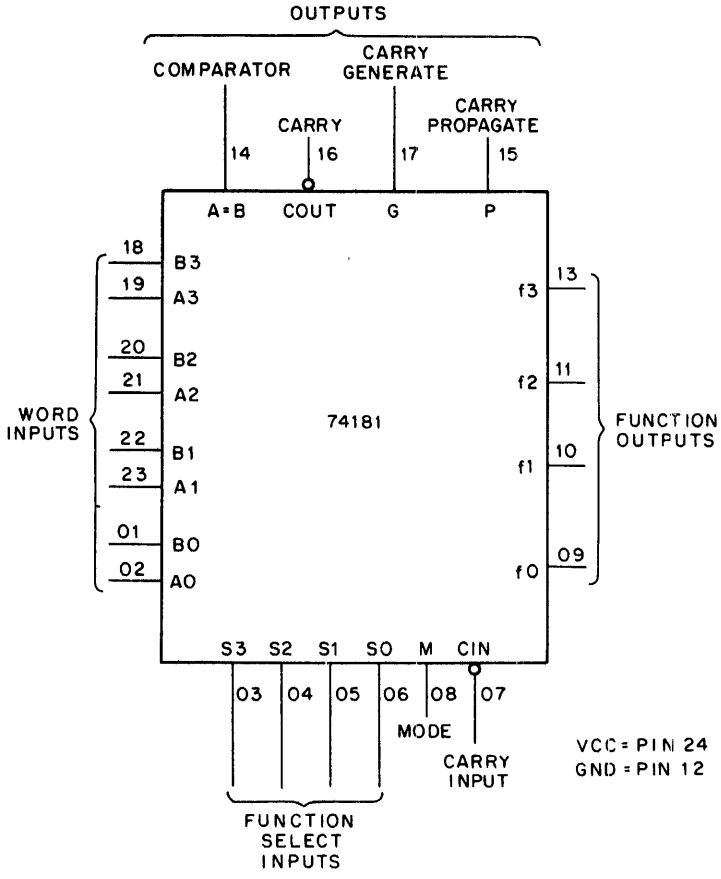
74181 4-BIT ARITHMETIC LOGIC UNIT, ACTIVE HIGH DATA

The 74181 performs up to 16 arithmetic and 16 logic functions. Arithmetic operations are selected by four function-select lines (S0, S1, S2, and S3) with a low-level voltage at the mode control input (M), and a low-level carry input. Logical operations are selected by the same four function-select lines except that the mode control input (M) must be high to disable the carry input.

74181
TABLE OF LOGIC FUNCTIONS

Function Select				Output Function	
S3	S2	S1	S0	Negative Logic	Positive Logic
L	L	L	L	$f = \overline{A}$	$f = \overline{A}$
L	L	L	H	$f = \overline{AB}$	$f = \overline{A + B}$
L	L	H	L	$f = \overline{A} + B$	$f = \overline{A}B$
L	L	H	H	f = Logical 1	f = Logical 0
L	H	L	L	$f = \overline{A + B}$	$f = A\overline{B}$
L	H	L	H	$f = \overline{B}$	$f = \overline{B}$
L	H	H	L	$f = \overline{A \oplus B}$	$f = A \oplus B$
L	H	H	H	$f = A + \overline{B}$	$f = A\overline{B}$
H	L	L	L	$f = \overline{A}B$	$f = \overline{A + B}$
H	L	L	H	$f = A \oplus B$	$f = \overline{A \oplus B}$
H	L	H	L	f = B	f = B
H	L	H	H	f = A + B	f = AB
H	H	L	L	f = Logical 0	f = Logical 1
H	H	L	H	$f = A\overline{B}$	$f = A + \overline{B}$
H	H	H	L	f = AB	f = A + B
H	H	H	H	f = A	f = A

With mode control (M) high: C_{in} irrelevant
For positive logic: logical 1 = high voltage
logical 0 = low voltage
For negative logic: logical 1 = low voltage
logical 0 = high voltage



IC-74181

74181
TABLE OF ARITHMETIC OPERATIONS

Function Select				Output Function	
S3	S2	S1	S0	Low Levels Active	High Levels Active
L	L	L	L	f = A minus 1	f = A
L	L	L	H	f = AB minus 1	f = A + B
L	L	H	L	$f = A\overline{B}$ minus 1	$f = A + \overline{B}$
L	L	H	H	f = minus 1 (2's complement)	f = minus 1 (2's complement)
L	H	L	L	f = A plus $[A + \overline{B}]$	$f = A$ plus $A\overline{B}$
L	H	L	H	f = AB plus $[A + \overline{B}]$	$f = [A + B]$ plus $A\overline{B}$
L	H	H	L	f = A minus B minus 1	f = A minus B minus 1
L	H	H	H	$f = A + \overline{B}$	$f = A\overline{B}$ minus 1
H	L	L	L	f = A plus [A + B]	f = A plus AB
H	L	L	H	f = A plus B	f = A plus B
H	L	H	L	$f = A\overline{B}$ plus [A + B]	$f = [A + \overline{B}]$ plus AB
H	L	H	H	f = A + B	f = AB minus 1
H	H	L	L	f = A plus A†	f = A plus A†
H	H	L	H	f = AB plus A	f = [A + B] plus A
H	H	H	L	$f = A\overline{B}$ plus A	$f = [A + \overline{B}]$ plus A
H	H	H	H	f = A	f = A minus 1

With mode control (M) and C_{in} low
† Each bit is shifted to the next more significant position.

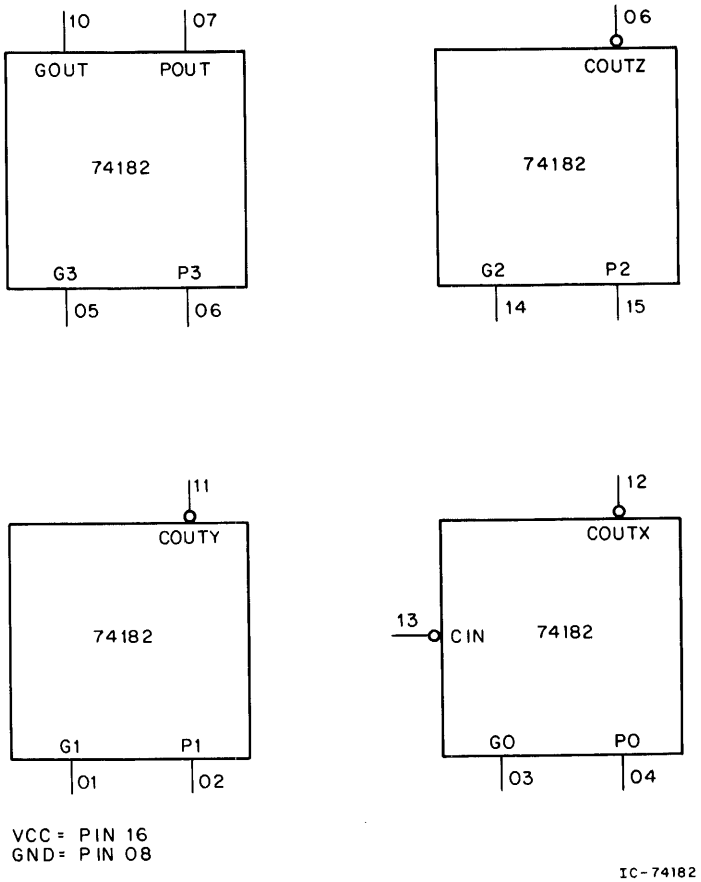
74182 LOOK-AHEAD CARRY GENERATOR

The 74182 Look-Ahead Carry Generator, when used with the 74181 ALU, provides carry look-ahead capability for up to n-bit words. Each 74182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits.

Carry inputs and outputs of the 74181 ALU are in their true form, and the carry propagate (POUT) and carry generate (GOUT) are in negated form.

PIN DESIGNATIONS

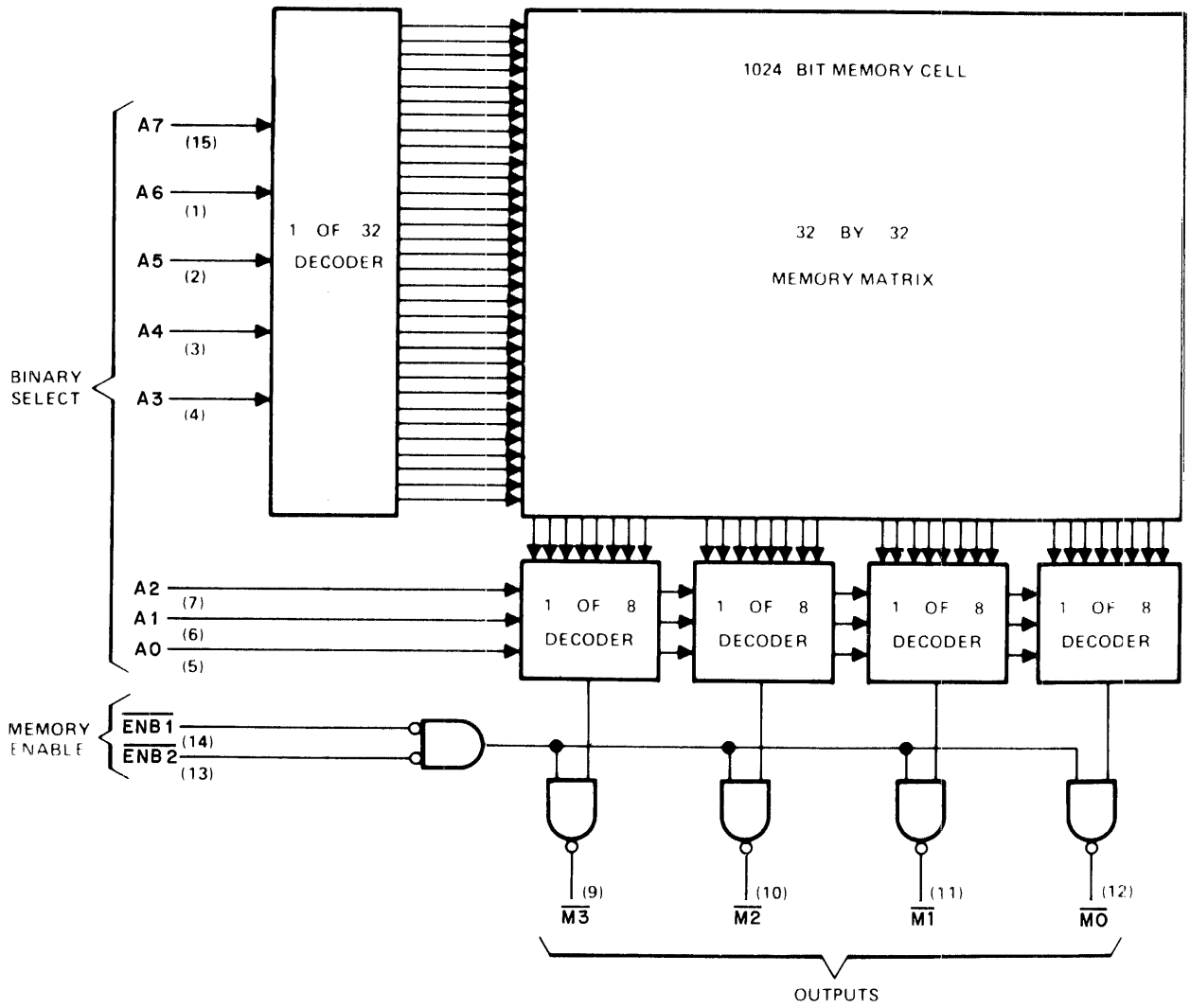
Designation	Pin No.	Function
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
CIN	13	CARRY INPUT
COUTX, COUTY, COUTZ	12, 11, 9	CARRY OUTPUTS
GOUT	10	ACTIVE-LOW CARRY GENERATE OUTPUT
POUT	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

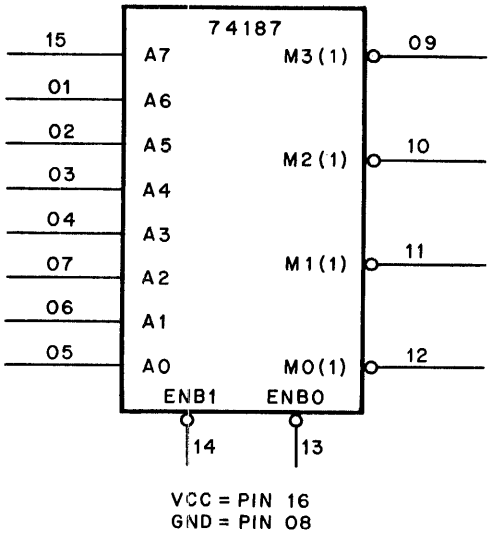


VCC = PIN 16
GND = PIN 08

IC-74182

74187 1023-BIT READ-ONLY MEMORY





VCC = PIN 16
GND = PIN 08

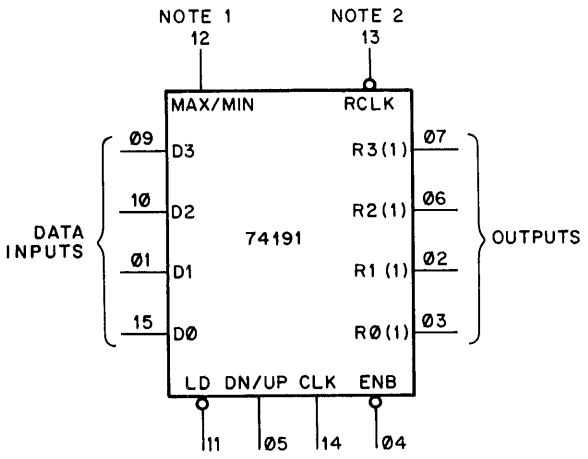
IC-74187

74191 4-BIT UP/DOWN COUNTER

The 74191 is a 4-bit binary counter that counts in BCD or binary and can operate as an up or down counter. The counter can be preset by the load control and uses a rippled clock output for cascading.

DOWN/UP	ENABLE	LOAD	MODE
X	X	L	Parallel Load
X	H	H	No Change
L	L	H	Count Up
H	L	H	Count Down

H = high level L = low level X = irrelevant



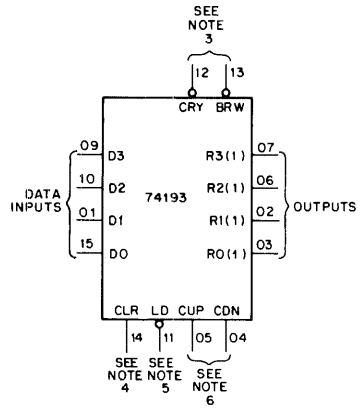
VCC = PIN 16
GND = PIN 08

NOTES:
1. MAX/MIN produces a high level output pulse when the counter overflows or underflows.
2. Ripple clock produces a low level output pulse when an overflow or underflow condition exists.

IC-74191A

74193 4-BIT UP/DOWN COUNTER

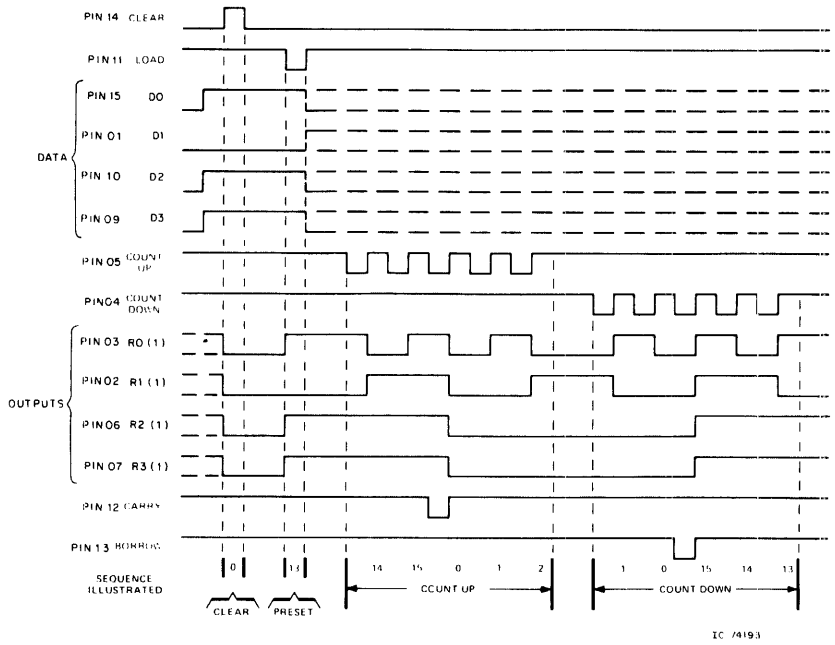
The 74193 binary counter has an individual asynchronous preset to each flip-flop, a fully independent clear input, internal cascading circuitry, and provides synchronous counting operations.



NOTES:
1. Clear overrides load, data, and count inputs.
2. When counting up, count down input must be high; when counting down, count-up input must be high.
3. Produce pulses equal to width of count pulses during: Underflow (BORROW)
   Overflow (CARRY)
4. CLR input high forces all outputs low. CLR overrides load, data and DN/UP inputs.
5. Preset to any state by applying input data with load input low. Output changes to agree with inputs independent of count pulses.
6. Select DN or UP clock while other is held high.

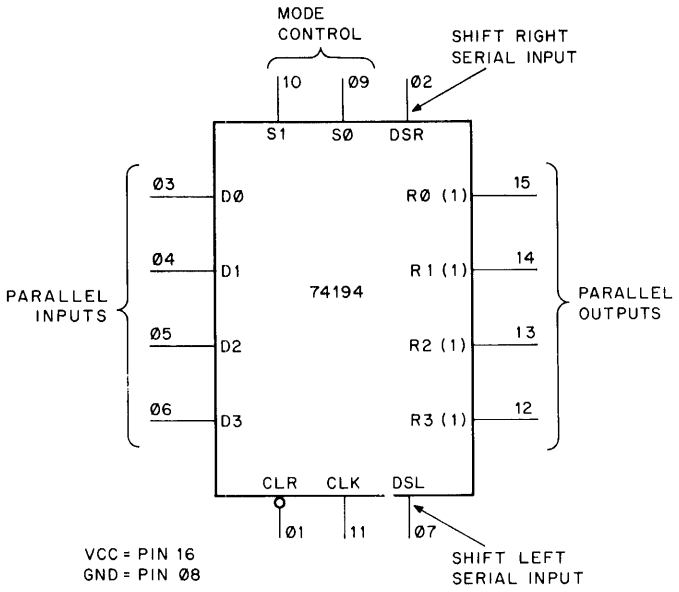
typical clear, load, and count sequences for 74193

Illustrated below is the following sequence
1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



74194 4-BIT SHIFT REGISTER

The 74194 is a parallel load, parallel output, shift register with left shift and right shift capability. Clocking is accomplished by positive-edge triggering. In addition, the IC contains an inhibit function and direct overriding clear input.



	MODE CONTROL	
	S1	S0
PARALLEL LOAD	H	H
SHIFT RIGHT (IN THE DIRECTION R0 TOWARD R3)	L	H
SHIFT LEFT (IN THE DIRECTION R3 TOWARD R0)	H	L
INHIBIT CLOCK (DO NOTHING)	L	L

IC-74194

APPENDIX E
PREVENTIVE MAINTENANCE SCHEDULE

Device	Period*	Time*	Weekly	Monthly	Quarterly	Semi-Annually	Annually
CR11/CR04	40 hr	15 min	–	–	1 hr	2 hr	–
DL11-A	–	–	–	–	15 min	–	20 min
FP11-B	–	–	–	–	1.5 hr	–	–
KB11-B,C	–	–	–	15 min	2.5 hr	–	3 hr
MJ11							
KW11-L	–	–	–	–	20 min	25 min	30 min
LA36	–	–	–	–	–	–	–
LP05	–	–	30 min	–	1.5 hr	4 hr	–
LP11 (ALL)	–	–	1 hr	–	2 hr	–	3 hr, 10 min
LPS11	–	–	–	–	3 hr	–	–
LV11/LV01	–	–	15 min	–	1 hr	3 hr	–
PC05	–	–	–	5 min	35 min	1.75 hr	–
RH70	–	–	–	–	30 min	–	–
RK05	–	–	–	10 min	1.75 hr	2.75 hr	3.75 hr
RP04	–	–	–	–	1.5 hr	3 hr	3.5 hr
RP11C/RP03	–	–	–	10 min	1.5 hr	3 hr	3 hr, 10 min
RS03/04	–	–	–	–	1.5 hr	2.5 hr	–
TU10	8 hr	15 min	–	15 min	1.5 hr	2.75 hr	4 hr
TU16	–	–	–	30 min	1 hr	2 hr	–
TU56	–	–	–	20 min	1 hr	2 hr	3.5 hr

* NOTE: These two columns show the maintenance required at odd intervals, e.g., 15 min of PM every 8 hrs on the TU10.

APPENDIX F
SUMMARY OF EQUIPMENT SPECIFICATIONS

This table provides mechanical, environmental, and programming information for the PDP-11/70 optional equipment. The equipment is arranged in alphanumeric order by Model Number.

NOTES

1. Mounting Codes

   CAB = Cabinet mounted. If a cabinet is included with the option, it is indicated by an X in the "Cab Incl" column.

   FS = Free standing unit. Height X Width X Depth dimensions are shown in inches.

   TT = Table top unit.

   PAN = Panel mounted. Front panel height is shown in inches. An included cabinet is indicated when applicable.

   SU = System Unit. SU mounting assembly is included with the option.

   SPC = Small Peripheral Controller. Option is a module that mounts in a quad module, SPC slot.

   MOD = Module. Height is single, double, or quad.

   ( ) = Option mounts in the same space as the equipment shown within the parentheses.

   Some options include 2 separate physical parts and are indicated by use of a plus (+) sign.

2. Cabinet and peripheral equipment (such as magnetic tape) are included in the specifications.

3. Relative humidity specifications mean without condensation.

4. Equipment that can supply current is indicated by parentheses ( ) around the number of amps in the POWER section.

5. Non-Processor Request Devices are indicated by an X in the "NPR" column.

6. MJ11 Memory specifications are stated in Chapter 2 of this manual.

CONVERSION FACTORS

(inches)	X 2.54	=	(cm)
(lbs)	X 0.454	=	(kg)
(Watts)	X 3.41	=	(Btu/hr)
$[(^\circ C) X \frac{9}{5}] + 32$		=	($^\circ F$)

Model Number	Description	MECHANICAL						ENVIRONMENTAL		POWER			PROGRAMMING		UNIBUS			Model Number
		Mounting Code	Size H × W × D (inches)	Cab Incl	Weight (lbs)	Power Harness		Oper Temp (°C)	Rel Humid (%)	Cur needed/(supplied)		Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
						BA11-K	H960-D			+5 V	115 Vac / other (amps)							
AA11-D	D/A Subsystem	SU				7009562	7009562	10–50	20–95	3	0.5	60	17 776 756	140,144	4, 5		1	AA11-D
AD01-D	A/D Subsystem	PAN	5¼		15			0–55	10–95		0.5	60	17 776 770	130	4–7		1	AD01-D
AFC11	A/D Subsystem	CAB						10–55	10–95		15	1700	17 772 570	134	4		1	AFC11
AR11-K	A/D Subsystem	SPC + PAN	5¼							4								AR11-K
BA11-K	Mounting Box	PAN	10½		100						12 @ 115 V 10A @ -15V 1A @ -5 V 50A @ +5 V 8A @ +20 V 4A @ +15 V	1380						BA11-K
BA614	D/A Converter	(AA11-D)																BA614
BB11	Blank Mntg Panel	SU																BB11
BB11-A	Blank Mounting Panel (non-slotted blocks)	SU																BB11-A
BB11-B	Blank double Mounting Panel, 9 × 6	2SU																BB11-B
BC11-A	Unibus Cable																	BC11-A
BM792-Y	Bootstrap Loader	SPC								0.3							1	BM792-Y
CB11	Telephone Switching Interface	Cab		X	300			10–50	10–90		5.6	650	17 764 000	float	4–7		1, 2	CB11
CD11-A/B	Card Reader	SU + TT	14 × 24 × 18		85	7010117	7009562	10–50	10–90	2.5	4	450	17 772 460	230	4	X	1	CD11-A
CD11-E	Card Reader	SU + TT	38 × 24 × 38		200	7010117	7009562	10–50	10–90	2.5	6	700	17 772 460	230	4	X	1	CD11-E
CM11-F	Card Reader	SPC + TT	11 × 19 × 14		60			10–50	10–90	1.5	4	400	17 777 160	230	6		1	CM11-F
CR11	Card Reader	SPC + TT	11 × 19 × 14		60			10–50	10–90	1.5	4	400	17 777 160	230	6		1	CR11
CTS-11	Card Reader/Punch	SU + FS	38 × 48 × 27		300	7009562	7009562	5–43	8–90	4.0			17 777 160	230	4		1	CTS-11
DA11-B	Unibus Link	SU				7009562	7009562			4			17 772 410	124	5	X	1	DA11-B
DA11-F	Unibus Window	SU				7010117	7009563	10–50	10–90	5			17 764 000	float	7	X	1	DA11-F
DB11-A	Bus Repeater	SU				7009562	7009562	5–50	10–95	3.2							1 + 1	DB11
DC11-A	Asynch Line Inter	SU				7010117	7009562	10–50	20–90		see Product Bull.		17 774 000	float	5		1	DC11-A
DD11-B	Periph Mntg Panel	SU				7010117	7009563											DD11-A
DECkit 01-A	Remote Analog Data Concentrator: 8 Channels, Serial	PAN	5¼ × 19 × 13		15			0–50	10–95		1.5 @ 115 Vac 0.75 @ 230 Vac	175						DECkit 01-A
DECkit 11-F	I/O Interface: 3 Words In/1 Word Out	SU				7009562		0–70	10–95	1.84			User	User	7		4	DECkit 11-F
DECkit 11-H	I/O Interface: 4 Words In/4 Words Out	SU				7009562		0–70	10–95	3.91			User	User	5–6		4	DECkit 11-H
DECkit 11-K	I/O Interface: 8 Words In	SU				7009562		0–70	10–95	1.97			User				2	DECkit 11-K
DECkit 11-M	I/O Interface: Instrumentation Interface	SU				7009562		0–70	10–95	1.75			User	User	4		2	DECkit 11-M
DF01-A	Acoustic Coupler	TT	6 × 7 × 12		6			0–60			0.3							DF01-A
DF11	Line Sig Cond	DF slot									see Product Bull.							DF11
DH11	Asynch Line MX	2 SU				7010118	7009561	5–45	10–95	8.4	0.24 A @ -15 V		float	float	5	X	2	DH11
DH11-AD	Asynch 6 Line MX	2 SU				7010118		10–40		10.8	0.4 A @ +15 V 0.65 A @ -15 V			float		X	2	DH11-AD

Model Number	Description	MECHANICAL						ENVIRONMENTAL		POWER			PROGRAMMING		UNIBUS			Model Number
		Mounting Code	Size H × W × D (inches)	Cab Incl	Weight (lbs)	Power Harness BA11-K	Power Harness H960-D	Oper Temp (°C)	Rel Humid (%)	Cur needed/(supplied) +5 V	Cur needed/(supplied) 115 Vac/other (amps)	Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
DH11-AE	Asynch 6 Line MX	2 SU				7010118		10–40		8.6	0.1 A @ +15 V 0.34 A @ -15 V			float		X	2	DH11-AE
DJ11-A	Asynch Line MX	SU				7010117	7009563			5	see Product Bull.		float	float	5		1	DJ11
DL11-A	Terminal Control	SPC								1.8	0.15 A @ -15 V		17 777 560	060,064	4		1	DL11-A
DL11 (others)	Asynch Line Inter	SPC								1.8	0.15 A @ -15 V		17 776 500	float	4		1	DL11 (others)
DM11-BB	Modem Ctr. MUX	(DH11)								2.8			17 775 000	float			1	DM11-BB
DN11-A	Auto Calling Unit	SU				7009562	7009562	0–40	20–90	1.4	0.10 A @ ±15 V		17 775 200	float	4		1	DN11
DP11	Synch Line Inter	SU				7009562	7009562	0–40	20–90	2.5	0.10 A @ ±15 V		17 774 400	float	5		1	DP11
DQ11	DMA Sync Line Interface	SU				7010117	7009563	10–50	10–90	5.7	0.04 A @ +15 V 0.07 A @ -15 V		float	float	5	X	1	DQ11
DR11-B	DMA Interface	SU				7009562	7009562	10–50	20–90	3.3			17 772 410	124	5	X	1	DR11-B
DR11-C	General Interface	SPC						10–50	20–90	1.5			17 767 770	float	5		1	DR11-C
DR11-K	General Interface																	DR11-K
DR11-L	Unibus 2-Word In	SPC						5–50	10–95	1.5			User	User	User		1	DR11-L
DR11-M	Unibus 2-Word Out	SPC						5–50	10–95	1.5			User	User	User		1	DR11-M
DT03-F	Unibus Switch	PAN	5¼								2			User	7		1 + 1	DT03-F
DU11	Sync Line Inter	SPC						10–50	20–95	2.2	0.7 A @ +15 V 0.17 A @ -15 V			float	5		1	DU11
DV11+ 2 DV11-BA	Sync MUX	2 SU				7010835		10–40	10–90	15	0.5 A @ +15 V 1.0 A @ -15 V	97		float	5-6	X	2	DV11+ 2 DV11-BA
DX11	IBM Chan. Interface	CAB		X	180			10–55	10–90		2.5	300	17 776 200	float	4-7	X	1	DX11-B
GT40	Graphics Terminal	TT	18 × 20 × 24		150			15–35	20–80		15	1500	float	float			1	GT40
H312-A	Null Modem																	H312-A
H720-E	Power Supply	(BA11)			30			0–50	20–95	(22)	6 (10 A) @ -15 V	700						H720
H722	Transformer	(PC11-A)									1.5 A @ 230 Vac							H722
H742	Power Supply	(H960-D)									8 (1 A) @ +15 V							H742
H744	+5 V Regulator	(H742)								(25)								H744
H745	-15 V Regulator	(H742)									(10 A) @ -15 V							H745
H754	+20, -5 V Regulator	(H742)									(8 A) @ +20 V (1 A) @ -5 V							H754
H933-C	Mounting Panel (H803 blocks)	SU																H933-C
H933-CB	Mounting Panel (slotted blocks)	SU																H933-CB
H933-D	Mounting Panel (H808 blocks)	SU																H933-D
H934-CB	Double Mounting Panel (slotted blocks)	2 SU																H934-CB
H960-C	Cabinet	FS	72 × 21 × 30	X	120													H960-C
H960-D	Cab (1 drawer)	FS	72 × 21 × 30	X	300		7009566			(75)	8 (20 A) @ -15 V	900						H960-D
H960-E	Cab (2 drawers)	FS	72 × 21 × 30	X	470		7009566			(150)	16 (40 A) @ -15 V	1800						H960-E
H961-A	Cab w/o side pan	FS	72 × 21 × 30	X	120													H961-A
KG11-A	Comm Arith Unit	SPC								1.5			17 770 700				1	KG11-A
KW11-L	Line Clock	MOD	single ht							0.8			17 777 546	100	6		1	KW11-L
KW11-P	Programmable Clock	SPC								1			17 772 540	104	6		1	KW11-P

Model Number	Description	MECHANICAL						ENVIRONMENTAL		POWER			PROGRAMMING		UNIBUS			Model Number
		Mounting Code	Size H x W x D (inches)	Cab Incl	Weight (lbs)	Power Harness BA11-K	Power Harness H960-D	Oper Temp (°C)	Rel Humid (%)	Cur needed / (supplied) +5 V	Cur needed / (supplied) 115 Vac / other (amps)	Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
LA36	DECwriter	FS	33.5 x 27.5 x 24		102			10–40	10–90		3	300						LA36
LC11-A	LA30 Control	SPC								1.5			17 777 560	060,064	4		1	LC11-A
LP11-F	Printer (80 col)	SPC + FS	46 x 24 x 22		200			10–43	15–80	1.5	2	250	17 777 514	200	4		1	LP11-F
LP11-J	Printer (132 col)	SPC + FS	46 x 48 x 25		575			10–43	15–80	1.5	4	500	17 777 514	200	4		1	LP11-J
LP11-R	Ptr (Heavy duty)	SPC + FS	48 x 49 x 36		800			10–43	15–80	1.5	17	2000	17 777 514	200	4		1	LP11-R
LPS11	Lab Periph System	PAN	5¼		80			5–43	20–80		3	300	float	float	4-6	opt	2	LPS11-S
LS11	Line Printer	SPC + TT	12 x 28 x 20		155			5–38	5–90	1.5	3	300	17 777 514	200	4		1	LS11
LT33	Teletype	FS	34 x 22 x 19		60			15–35	20–80		2	200						LT33
LV11	Electrostatic Ptr	SPC + FS	38 x 19 x 18		160			10–43	20–80	1.5	5	600	17 777 514	200	4		1	LV11
M105	Adrs Select Module	MOD	single ht							0.34								M105
M783	Bus Transmitter	MOD	single ht							0.2								M783
M784	Bus Receiver	MOD	single ht							0.2								M784
M785	Bus Transceiver	MOD	single ht							0.3								M785
M792	Diode ROM	SPC	quad ht							0.23			17 773 000				1	M792
M795	Word Count	MOD	double ht							0.6								M795
M796	Bus Control	MOD	single ht							0.13								M796
M920	Bus Jumper	MOD	double ht															M920
M9302	Bus Terminator	MOD	double ht							1.25								M9302
M1501	Bus Input Interface	MOD	single ht					0–70	10–95	0.3								M1501
M1502	Bus Output Inter	MOD	double ht					0–70	10–95	0.75								M1502
M1621	DVM Data Input Interface	MOD	quad ht					0–70	10–95	0.78								M1621
M1623	Instrument Remote Control Interface	MOD	quad ht					0–70	10–95	1.6								M1623
M1710	Unibus Interface Foundation	MOD & SPC	quad ht					0–70	10–95	0.79						opt		M1710
M1801	16-Bit Relay Output Interface	MOD	quad ht					0–70	10–95	1.46								M1801
M7821	Interrupt Control	MOD	single ht							0.55								M7821
PC11	Paper Tape	SPC + PAN	10½		50			13–38	20–95	1.5	3	350	17 777 550	070,074	4		1	PC11
PDM70	Programmable Data Mover	TT	5¼ x 19 x 23	X	55			0–40	10–95		115 Vac	250						PDM70
											230 Vac	250						
PR11	Paper Tape (rdr)	SPC + PAN	10½		50			13–38	20–95	1.5	3	350	17 777 550	070	4		1	PR11
RC11-A	Disk & Control	PAN	10½		115			17–50	20–80		2.2	250	17 777 440	210	5	X	1	RC11-A
RF11-A	Disk & Control	PAN + PAN	16 + 16	X	500			17–33	20–55		6.5	750	17 777 460	204	5	X	1	RF11-A
RK05	Disk Drive	PAN	10½		110			15–43	20–80		2	160						RK05
RK11-D	Disk & Control	SU + PAN	10½	X	250	7010115	7009562	15–43	20–80	7.5	2	200	17 777 400	220	5	X	1	RK11-D
RP03	Disk Drive	FS	40 x 30 x 24		415			15–33	10–80		6 A @ 230 Vac	1300						RP03
RP11-C	Disk & Control	CAB + FS		X	740			15–33	10–80		7 6 A @ 230 Vac	2100	17 776 710	254	5	X	1	RP11-C
RS11	Disk Drive	PAN	16		100			17–33	20–55		2	200						RS11
RS64	Disk	PAN	10½		65			17–50	20–80		2.2	250						RS64
RT01	Numeric Data Entry Terminal	TT	6.5 x 12.5 x 15	X	12			0–40	10–90		0.25 @ 115 Vac 0.12 @ 220 Vac	30						RT01
RT02	Alphanumeric Data Entry Terminal	TT	6.3 x 14.4 x 16	X	14			0–40	10–90		110 Vac	50						RT02
											220 Vac	50						
RWP04	Disk Drive and Massbus Control	FS	40 x 31 x 32		600			15–32	20–80		3 phase Y or Δ	2100	17 776 000	254	5	(MB)	1	RWP04
RWS03	Disk Drive & Massbus Control	PAN	16		110						6 A	700	17 772 040	204	5	(MB)	1	RWS03

Model Number	Description	MECHANICAL						ENVIRONMENTAL		POWER			PROGRAMMING		UNIBUS			Model Number
		Mounting Code	Size H × W × D (inches)	Cab Incl	Weight (lbs)	Power Harness BA11-K	Power Harness H960-D	Oper Temp (° C)	Rel Humid (%)	Cur needed / (supplied) +5 V	Cur needed / (supplied) 115 Vac / other (amps)	Power Dis (W)	1st Reg Address	Int Vector	BR Level	NPR	Bus Loads	
RWS04	Disk Drive & Massbus Control	PAN	16		120						6 A	700	17 772 040	204	5	(MB)	1	RWS04
RX11	Floppy Disk & Control	SPC + PAN	10½ × 19 × 17		60			15–32	20–80	1.5	4 A	400	17 177 170	264	5		2	RX11
TA11	Cassette	SPC + PAN	5¼					10–40	20–80	1.5	1	120	17 777 500	260	6		1	TA11
TC11-G	DECtape & Control	PAN + PAN	10½ + 10½	X	250			15–32	20–80		9	870	17 777 340	214	6	X	1	TC11-G
TMA-11	TU10 & Control	PAN + PAN	26 + 10½	X	500			15–32	20–80		9	1000	17 772 520	224	5	X	1	TMA-11
TMA-11-M	TS03 & Control	PAN + PAN	10½ + 10½		100			15–32	20–80		2	200	17 772 520	224	5	X	1	TMA-11-M
TS03	Magtape Transport	PAN	10½		40			15–32	20–80		1	100						TS03
TU10	Magtape Transport	PAN	26	X	450			15–32	20–80		9	1000						TU10
TU16	Magtape Transport	PAN	26	X	450			15–32	20–80		8	1000						TU16
TU45	Magtape Transport	PAN	26	X	450			15–32	20–80									TU45
TU56	DECtape Transport	PAN	10½		80			15–32	20–80		3	350						TU56
TU70	Magtape Transport																	
TWU16	Magtape Transport & Massbus Control	PAN	26	X	500			15–32	20–80		8 0.6 A @ -15 V	1000	17 772 440	224	5	(MB)	1	TWU16
TWU45	Magtape Transport & Massbus Control	PAN	26	X	450			15–32	20–80									TWU45
TWU70	Magtape Transport & Massbus Control																	TWU70
UDC11	I/O Subsystem	CAB						5–50	10–90		15	1700	17 771 774	234	4, 6		2	UDC11
VR01	Display	PAN	10½		30			10–50	10–90		1	120						VR01
VR14	Display	PAN	10½		75			10–50	10–90		4	400						VR14
VT01	Display	TT	12 × 12 × 23		50			0–50	10–80		2.2	250						VT01
VT05	Alphanum Terminal	TT	12 × 19 × 30		55			10–43	8–90		2	130						VT05
VT20	Alphanum Terminal	TT																VT20
VT50	Alphanum Terminal	TT	14 × 21 × 28		43			10–40	10–90		1	110						VT50
VT52	Alphanum Terminal	TT	14 × 21 × 28		44			10–40	10–90			110						VT52
VT55																		VT55
XY11	Plotter Control for Calcomp 563 & 565 Houston DP1 & DP10	SPC								1.4	0.1A @ -15 V		17 772 554	120	4		1	XY11
XY311	3 Pen Plotter (Calcomp 936)	SPC + FS	44 × 50 × 24										17 772 554	120	4		1	XY311

APPENDIX G
WIRE TROUGH SYSTEM

This appendix is included in this manual to acquaint service personnel with the wire trough cable routing system. Some PDP-11/70s are already cabled this way, and eventually, all will be.

The illustrations show part numbers as well as cable folding procedures.

G.1 GENERAL

The trough system (Wire Cable Basket System) provides an organized cable system that improves the appearance of the cabling and helps reduce cable damage. With this system, cables are routed in channel baskets (troughs) along the edge of a bay, thus eliminating the tangled clumps of cables that were previously inevitable (Figure G-1). This system protects cables from inadvertent snagging when servicing a box.

Figure G-6 illustrates a trough section and its associated hardware. The trough iself is merely a wire basket. Trough sections come in three lengths: 1-bay, which is used for horizontal and vertical applications, and 2- and 3-bay, which are used strictly for vertical applications extending up to the entire height of a bay.

Figure G-2 illustrates a typical system application.

G.2 CALCULATION OF REQUIREMENTS (CABLES AND TROUGHS)

There are two cases in which troughs are used. First, they are used in the initial factory assembly of a system. (Refer to Paragraphs G.2.1 and G.2.2 for a design procedure and example.) Secondly wire troughs are field-retrofitted in existing systems for system enhancement. (Refer to Paragraph G.2.2 for a general procedure for the location and installation of troughs.)

The following are basic rules for planning the installation and placement of troughs. These rules are not intended to be absolute, but merely a guide for planning.

1. Always install troughs at the rear of the bays. This makes it possible to install equipment in box space and prevents zig-zag trough patterns.

2. For an unwired system, always plan to channel cables down to the bottom, back edge of the system. This provides accessibility and causes minimum interference with boxes.

3. Allow enough extra cable in all boxes to remove cable connectors from modules.

4. A horizontal trough section must be available for each slide-mounted box.

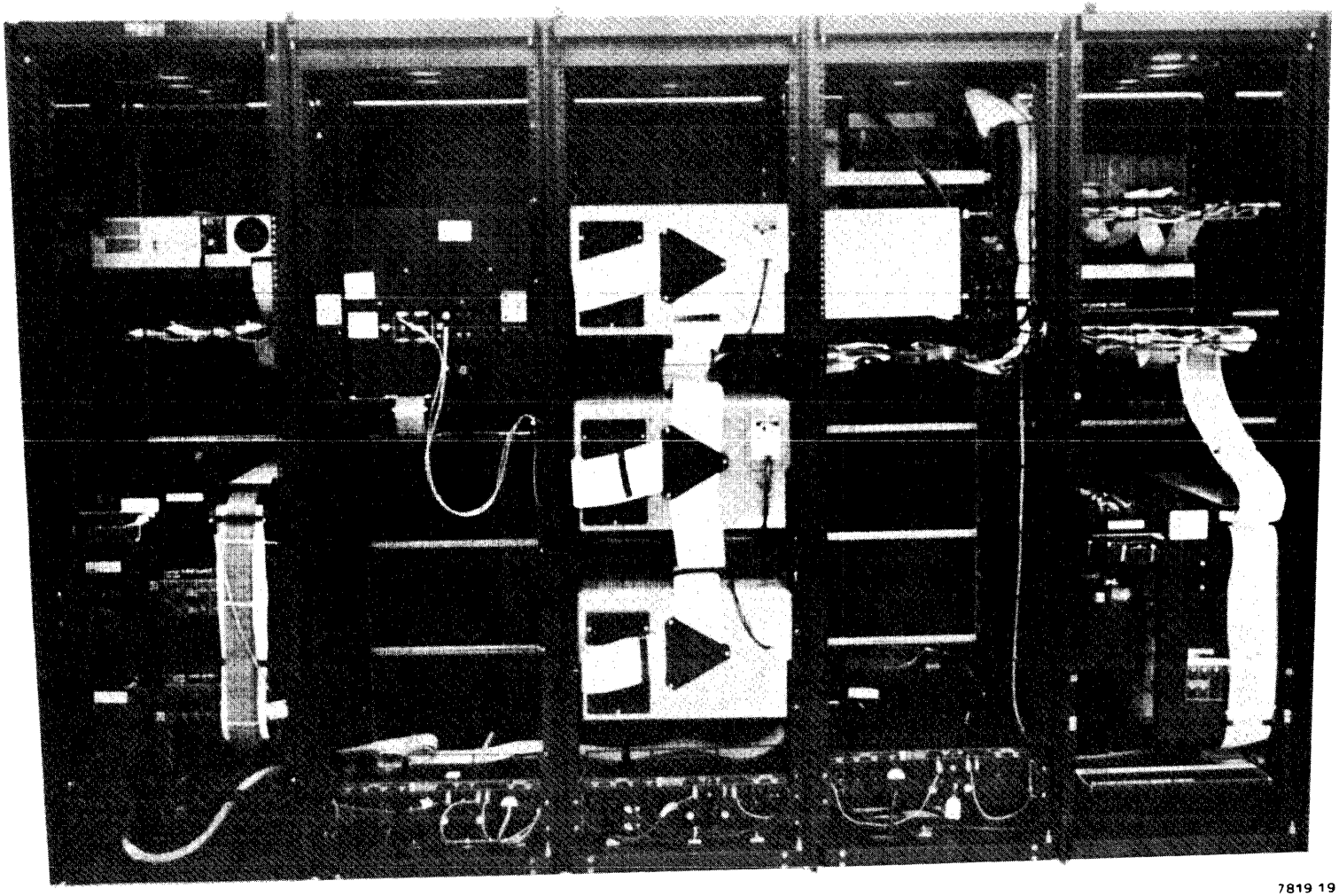


Figure G-1 Installed Wire Trough System

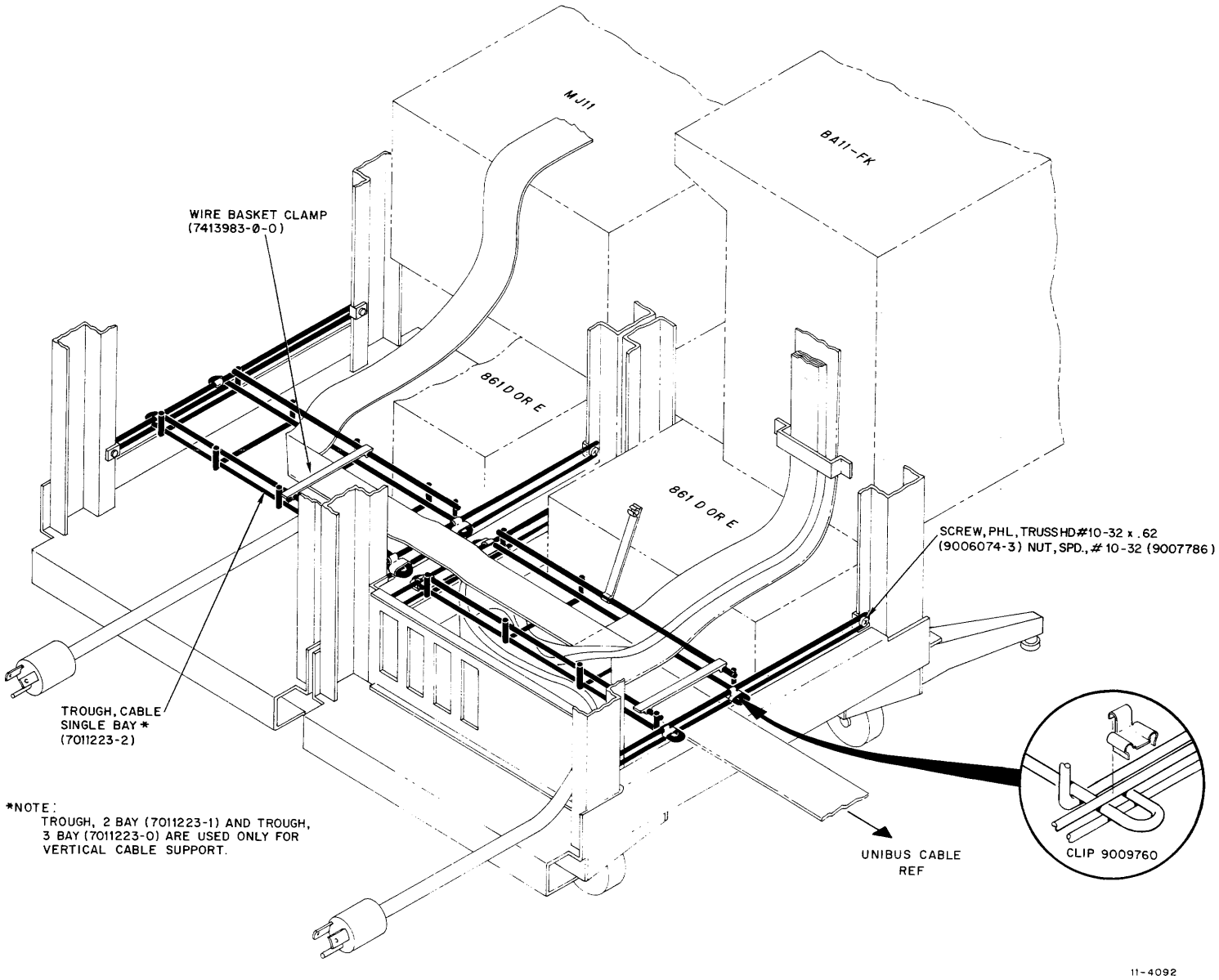


Figure G-2 PDP-11/70 with Cable Troughs

G.2.1 Determining Correct Cable Lengths

Most Unibus and I/O cables come in lengths of 1 foot increments. Thus, the accuracy of our calculations need not exceed ±0.5 feet. Cable should be conserved to cut costs, but should not be conserved at the expense of proper operation and safety.

The maximum Unibus cable length is approximately 50 feet. If the cable length exceeds the limit, cable rerouting should be considered. If this does not reduce it sufficiently, a bus repeater must be added.

Cable lengths can be determined as follows:

1. Set up a block diagram of the system and specify each type of box in its respective location as seen from the back of the system. (See example, Figure G-3a.)

2. List the desired cable connections (box-to-box; example: CU to BA11-F).

3. In the upper-left corner of the box, place an r, signifying Removable (slide-mounted), or an F, signifying Fixed. If Removable, also place an H or V within the box, signifying Horizontally or Vertically removable modules (i.e., modules that are removed from the side or from the top or bottom). This will assist in identifying the type of box for formula use (step 5).

4. Draw a U-type line connecting the box bases to represent the desired cable run. (Bottom of U rests on bottom of bays or top of box occupying bottom of bays.) Use a color code of your choice to define the different types of cables present in your system (i.e., red: Unibus; blue: round cables (line printer terminal); green: flat BC08 type).

5. For each cable connection (refer to the list made in step 2), calculate the proper length by using the formula shown below. Using destination direction (left or right), refer to the system block diagram (Figure G-3a) for A and B values. Table G-1 lists the cable lengths (feet) necessary to span from the rear of the box to an exit at the bay base (approximate the box level and adjust L (total cable length) according to level approximation). The exit (right or left will depend on the destination direction (for example, see Figure G-4). These values do not include service loop considerations.

NOTES

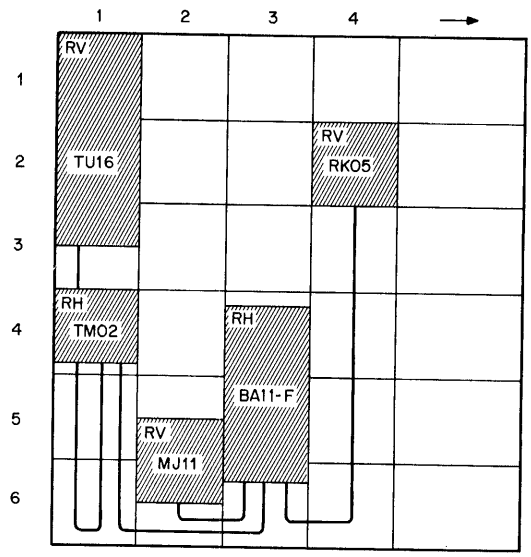
1. Total cable length, L, will be altered upon completion of trough planning.

2. Do not discard system block diagram as it will be used for calculations of trough sections and locations.

f301 6. Examine the system block diagram for obvious cable routes. (In the example, Figure G-3, cable need not run to the bottom of the cabinet in a connection of TU16 and TM02, or RK05 and BA11-F.) Note this type of connection for future trough planning.

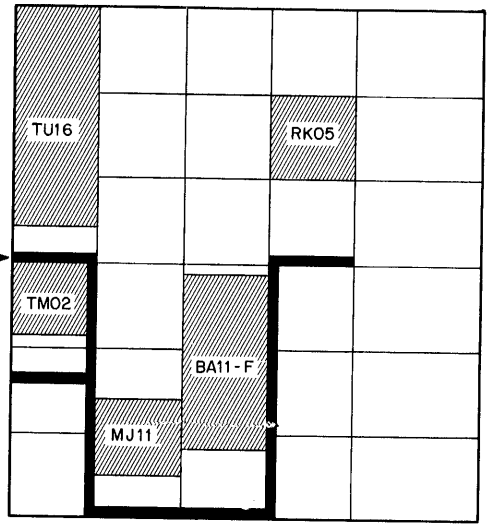
Certain options are usually connected and located in the same positions. This has generated usage of standard cable lengths. Cable connections from TU10 to TM11 and TU16 to TM02 require 6-foot lengths.

BLOCK DIAGRAM 1



TU16	TM02	L = 6 ft. (STANDARD LENGTH) (2 SERVICE LOOPS)
TM02	BA11-F	L = 6+6+2+2.5+2.5+0.5+0.5+0.5 = 20.5 ft.
MJ11	BA11-F	L = 5+6+0+2.5+2.5+0+0.5+0.5 =17 ft.
RK05	BA11-F	L = 10+5+0+2.5+2.5+0+0.5+0.5 =21 ft.

BLOCK DIAGRAM 2



CABLE LENGTH ALTERATIONS

TU16	TM02	L = 6 ft.
TM02	BA11-F	L = 20.5 ft.
MJ11	BA11-F	L = 17 + 2 = 19 ft.
RK05	BA11-F	L = 21 ft.

11-3651

Figure G-3 Example Problem

Table G-1 Option to Bay Base Cable Length

Option	Level	Cable Length from Rear of Box to Bay Exit at Base	
		Destination-Left	Destination-Right
BA11-F 21 in. High Max. Box Depth 2.0 ft	1, 2, & 3	8.0	7.0
	4, 5, & 6	5.0	4.0
BA11-K MJ11 10.5 in. High Max. Box Depth 2.0 ft	2	7.0	7.0
	3	6.0	6.0
	4	5.0	5.0
	5	4.0	4.0
BA11-D, B BA11-ES 10.5 in. High Max. Box Depth 2.0 ft	2	7.0	6.0
	3	6.0	5.0
	4	5.0	4.0
	5	4.0	3.0
BA11-L (PDP-11/04) 5.25 in. High Max. Box Depth 2.0 ft	2	7.0	6.0
	3	6.0	5.0
	4	5.0	4.0
	5	4.0	3.0
PDP-11/05 5.25 in. High Max. Box Depth 2.0 ft	2	7.0	6.0
	3	6.0	5.0
	4	5.0	4.0
	5	4.0	3.0
BA11-M (PDP-11/03) 3.50 in. High Max. Box Depth 15 in. or 1.25 ft	2	8.0	7.0
	3	7.0	6.0
	4	6.0	5.0
	5	5.0	4.0
TC11 DECtape Control	1	10.0	8.0
	2	9.0	7.0
	3	8.0	6.0
RF-11 Fixed Head Disk Control	1 & 2	9.0	7.0
	2 & 3	8.0	6.0

Table G-1 Option to Bay Base Cable Length (Cont)

Option	Level	Cable Length from Rear of Box to Bay Exit at Base	
		Destination-Left	Destination-Right
RP11 Disk Pack Control	2 & 3	8.0	6.0
TM11 (TU10) Max. Box Depth 1.5 ft	4 5	7.0 6.0	6.0 5.0
TM02 (TU16) Max. Box Depth 1.5 ft	4 5	7.0 6.0	6.0 5.0
RK11 RK05 10.5 in. High Max. Box Depth 2.0 ft	2 3 4 5	10.0 9.0 8.0 7.0	9.0 8.0 7.0 6.0
RJS04 RS04 15.75 in. High Max. Box Depth 2.0 ft	2 & 3 3 & 4 4 & 5	6.0 5.0 4.0	6.0 5.0 4.0
TA11 TU60 5.25 in. High Max. Box Depth 1.5 ft	2 3 4 5	7.0 6.0 5.0 4.0	6.0 5.0 4.0 3.0

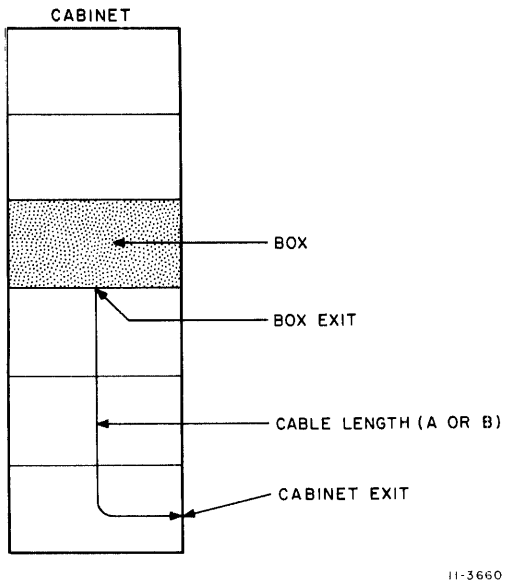


Figure G-4 Destination Direction – Right

The formula for calculating cable length is as follows:

$$L = A + B + nC + D_A + D_B + E_A + E_B$$

NOTE
0.5 is added to the total to prevent taut cables.

where L = Total cable length (feet or meters)

A = Cable length within starting unit bay (Table G-1)

B = Cable length within the destination unit bay (Table G-1)

n = Number of bays between cable termination bays

c = 2 feet (bay width)

D_A, D_B = 2.5 feet if box is slide-mounted or removable (R) for service loop

E_A, E_B = Estimated value for length of cable needed to reach connecting module inside the box from the back of the box (see Table G-1 for the maximum box depth); add 0.5 feet if the box is slide-mounted and modules are horizontally removable (H).

In calculating the cable length needed to reach a peripheral device located outside the system bays, the total, L, becomes L_X (L exterior).

$$L_X = A + D_A + E_A + P$$

where P = Length of cable needed from exit of bay to peripheral device.

NOTES

1. 0.5 is added to the total to prevent taut cables.

2. Total cable length may change once trough location is determined. This is due to possible additional cable needed to access a trough.

G.2.2 Determining Correct Trough Sections and Locations

To determine the correct trough sections and locations for a prewired system, follow the procedure below.

1. Examine the system from the rear and draw a sketch of the box locations including the cable system layout.

2. Plan trough locations referring to basic rules (Paragraph G.2).

NOTE

It may be necessary to plan various new cable routes and lengths.

3. Remove back doors to system wherever possible.

4. Examine the system and observe trough locations making plan alterations for obvious cable conservation.

5. Install troughs (Paragraph G.3.1).

6. Route cables in troughs individually using Unclamp-Reclamp method (Paragraph G.3.2).

If the system is an initial factory assembly, the cables are installed after the installation of all troughs is completed.

As a general rule, cables should be run across the back bottom edge of the bays (unless occupied by a box). One-bay horizontal trough sections are used to cross through a bay to another bay. A horizontal trough section is also used when a service loop is required for a slide-mounted box. The trough provides fixed anchorage for the one end of the service loop. The trough for service loop anchorage is usually planned for positioning on a level adjacent to the box.

Necessary trough sections and locations can be determined as follows:

1. Draw a second system block diagram (Figure G-1b) and label the appropriate boxes with the option designations.

2. Examine the first system block diagram (Figure G-1a) for required horizontal trough sections. Do not use 2- or 3-bay lengths when crossing the bays consecutively. This is physically difficult to install. Indicate the necessary horizontal trough sections on the second system block diagram.

3. Examine the first block diagram for vertical trough section locations. Observe adjacent bays to determine where vertical sections are required. Remember a vertical section need not extend fully to a slide-mounted box. Draw the required vertical trough sections on the second system block diagram. Leave as many box positions empty as possible in order to provide for possible future box additions.

4. Upon completion of trough planning, an alteration of cable lengths may be necessary. This is because positioning the vertical troughs for maximum cable access may have caused a more indirect cable route. Examine both diagrams and check each cable route for added cabling to access a trough. If the cable must be routed in the opposite direction from its destination, recalculate the corresponding A or B value for the opposite direction and add 2 feet. (This is done to allow for cabinet width.) Otherwise the total, L, remains unchanged. The same holds for L_X.

G.3 INSTALLATION

Before beginning installation of troughs and/or cables, examine the physical system to confirm correctness of planning approximations. When the necessary corrections are satisfactorily done, continue with the installation procedures.

NOTE

Care must be taken in trough positioning, to allow clearance for the fans on the top and/or bottom of the cabinet.

G.3.1 Installation of Troughs

Examine Figure G-6. Note the required parts and fastening hardware. Part numbers are included. The only required tools are pliers and a Phillips screwdriver (offset if available).

G.3.1.1 Basket Bar Assembly (Retaining Bracket) – Once a trough location is selected, fasten the retaining bracket to the bay frame. This retaining bracket may be connected on the inner or outer edges of the cabinet. Note that these brackets are always installed horizontally from back to front and act as a support for a horizontal and/or vertical trough. The connection to the cabinet is made at each end of the bracket by means of a Phillips truss-head machine screw and self-retaining speed nut (Figure G-6). If space restricts use of speed nuts, kep nuts can be used as replacements. Note the contact surface of the bracket in Figure G-5.

A retaining bracket is installed to support each end of the trough. When connecting a vertical trough section to a horizontal section, the adjoining bracket can act as a support for both.

G.3.1.2 Horizontal Troughs – After retaining brackets have been installed at each end of the desired trough location, slide hooked ends of trough through bars of bracket. Both ends are positioned at the same time (Figure G-7). Once the trough is in position, place clips on hooked ends (Figure G-2) with pliers. This will secure the trough.

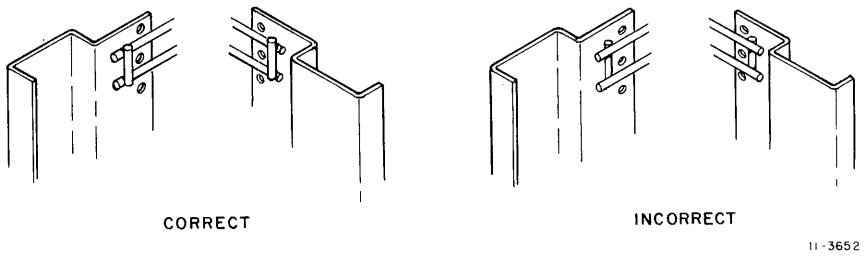
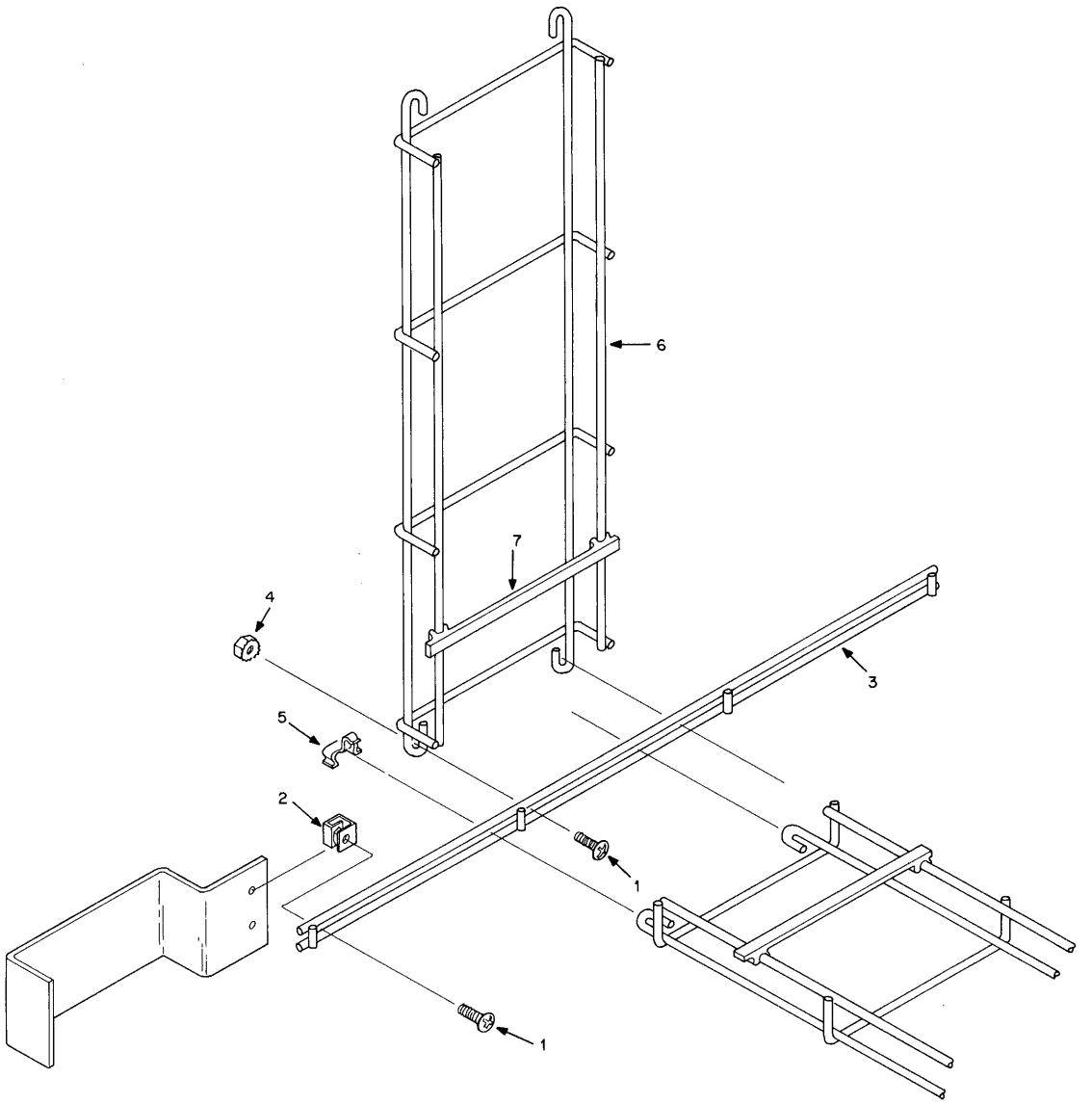


Figure G-5 Retaining Bracket Contact Surface



NOTE:
Troughs can be obtained in three lengths:
1 bay - 18.88 in.
2 bay - 39.68 in.
3 bay - 60.25 in.

Figure G-6 Trough Assembly

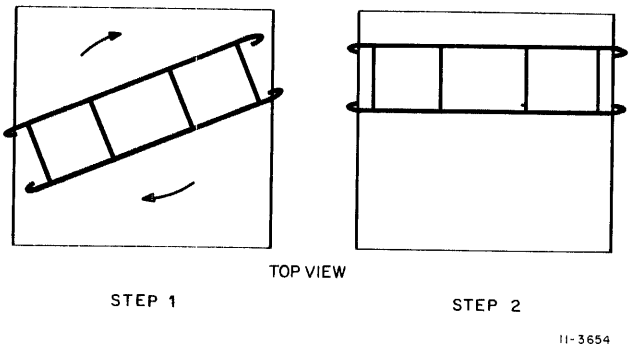


Figure G-7 Positioning Horizontal Trough Section

G.3.1.3 Vertical Troughs – A vertical trough is installed so that it correctly joins with the horizontal troughs and necessary retaining brackets. The second retaining bracket for a vertical trough is positioned by temporarily holding the trough in its location. Once both brackets are installed, the trough is again positioned and fastened to the retaining bracket. This is done by a nut and screw assembly through the hooked ends of the trough and bars of the retaining bracket (Figure G.3.2). The screw heads should appear on the inside of the bay to allow removal of the trough if necessary.

G.3.2 Installation of Cables

Examine Figure G-8. Note the way in which a cable enters and exits a trough.

Each cable will be installed completely before installation of the next cable. Begin at one cable end and make the proper cable connections to the box. Observe all length considerations before branching the cable onto the first trough. (Refer to Paragraphs G.2.1.) Folding will be necessary to keep cables flat and obtain desired polarity at the destination. (Refer to Paragraph G.3.2.1.) Apply clamps as the cable is routed down a trough at approximately 6-inch intervals. For successive cable routing through the same trough, one end of each clamp is unclamped and then reclamped as the cable is set in the trough. This is repeated down the entire cable path for each cable addition and is referred to as the Unclamp-Reclamp method. Cable ties are also used to bundle cables in troughs. Foam padding is required between adjacent Unibus cables to prevent cross talk.

G.3.2.1 Folding – In order to branch on or off a trough with a flat cable, a bend, fold, or number of folds are necessary (Figure G-8). Figures G-9 and G-10 provide various folding sequences to assist in cable manipulation.

Excess cable due to miscalculation is folded in an overlapping sequence and wrapped with a cable tie. If possible, this folding is stored inside the box to preserve the appearance of the system and may be utilized as an internal service loop for removing modules. Excess cable is necessary to provide an internal service loop for horizontally removable modules (Figure G-11).

G.3.2.2 Service Loops – A service loop consists of an excess unbound bundle of cables which allows a slide-mounted box to be extended from the cabinet without detaching cables (Figure G-12).

When a service loop is required, a horizontal trough is accessed within one level of the box position. This allows a fixed feedpoint for the cable. If a horizontal trough does not exist in this proximity, installation of one is required. Although it is usually located below the box, it may be positioned above the box. A service loop requires branching through (not over) the edge of a trough (Figure G-8).

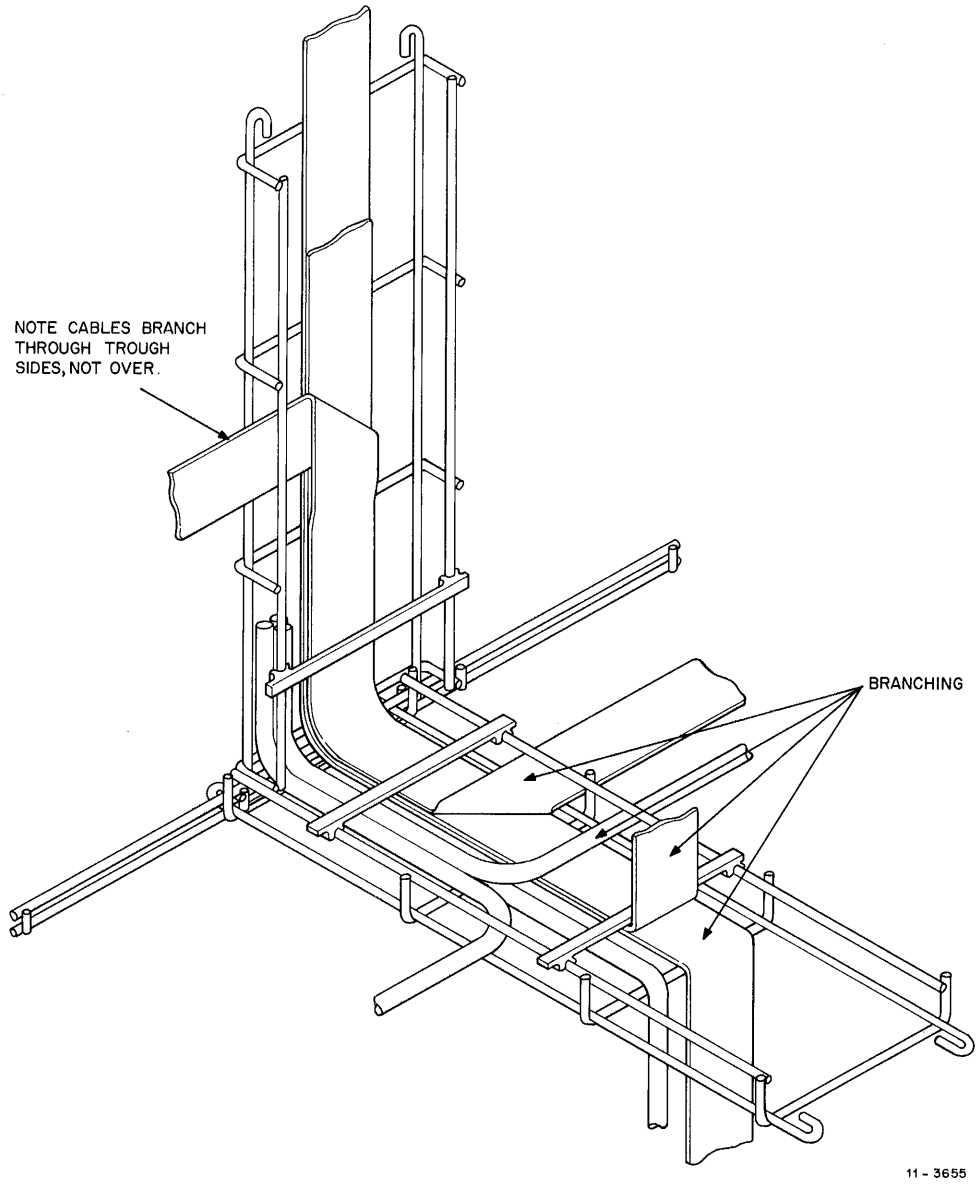


Figure G-8 Horizontal and Vertical Troughs with Cables

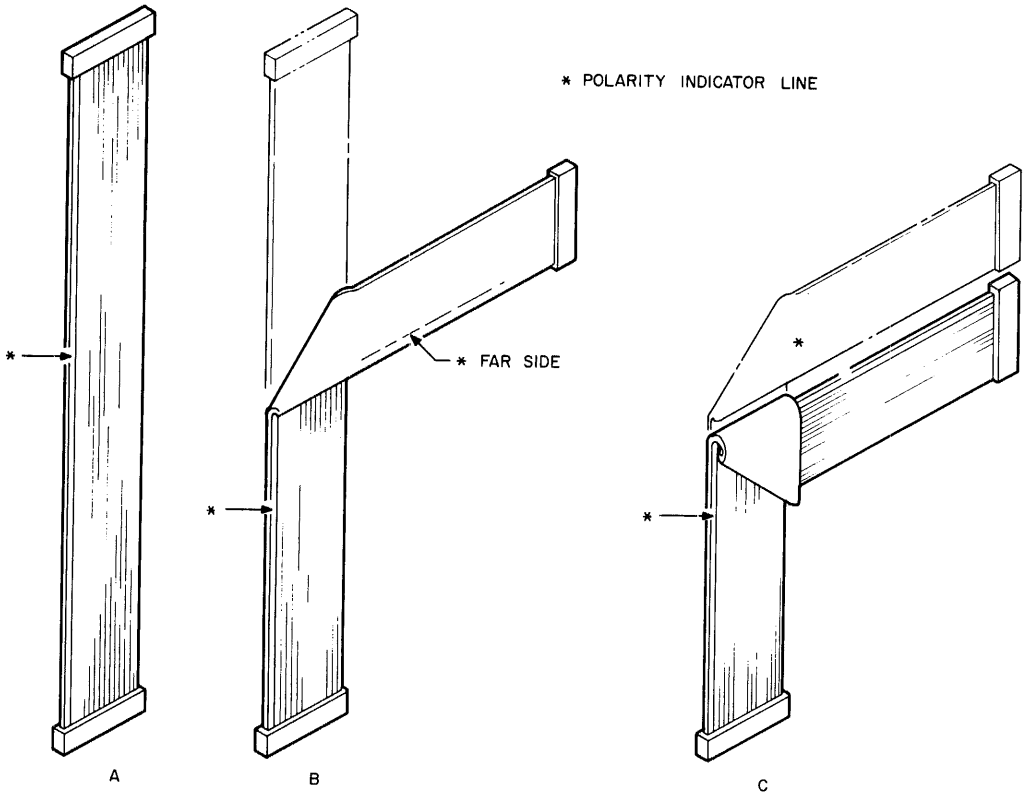


Figure G-9 Cable Fold

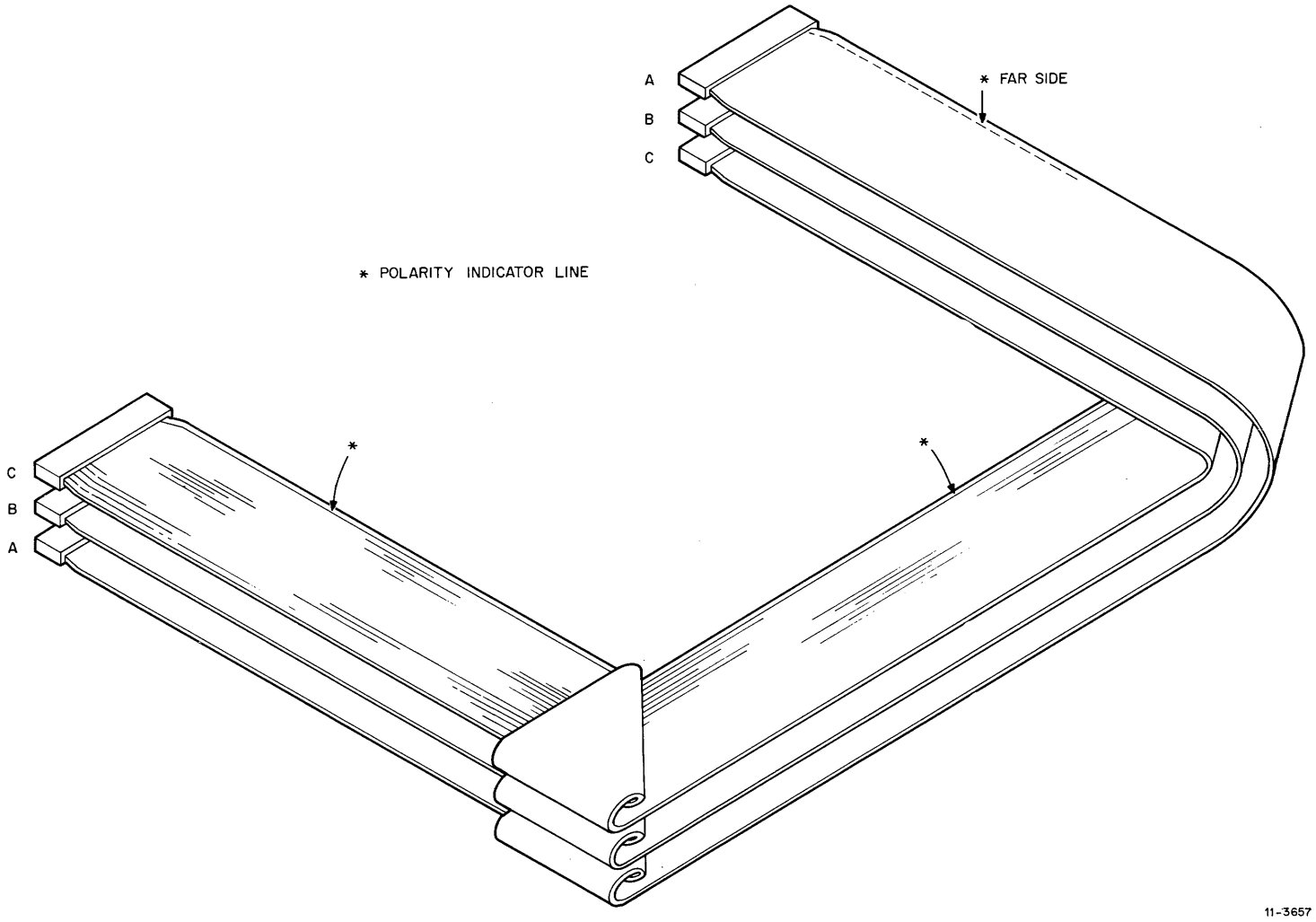


Figure G-10 TU16 Cables: Cables Inverted and Red Stripe on Same Side

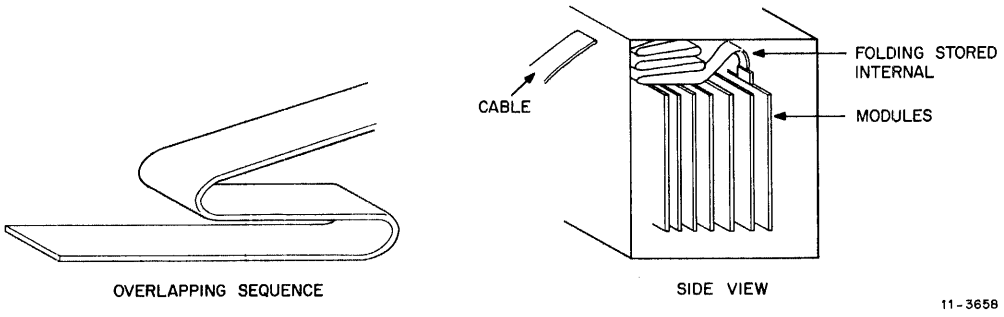


Figure G-11 Excess Cable Folding

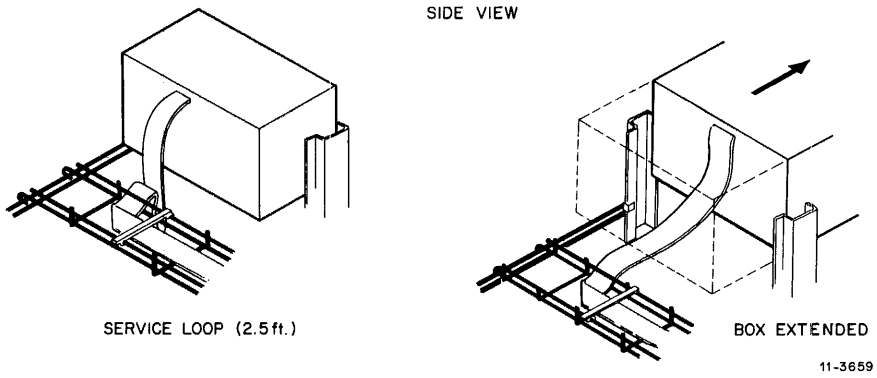


Figure G-12 Service Loop

APPENDIX H

PDP-11/70 BLOCK DIAGRAM ADDRESS AND DATA PATHS

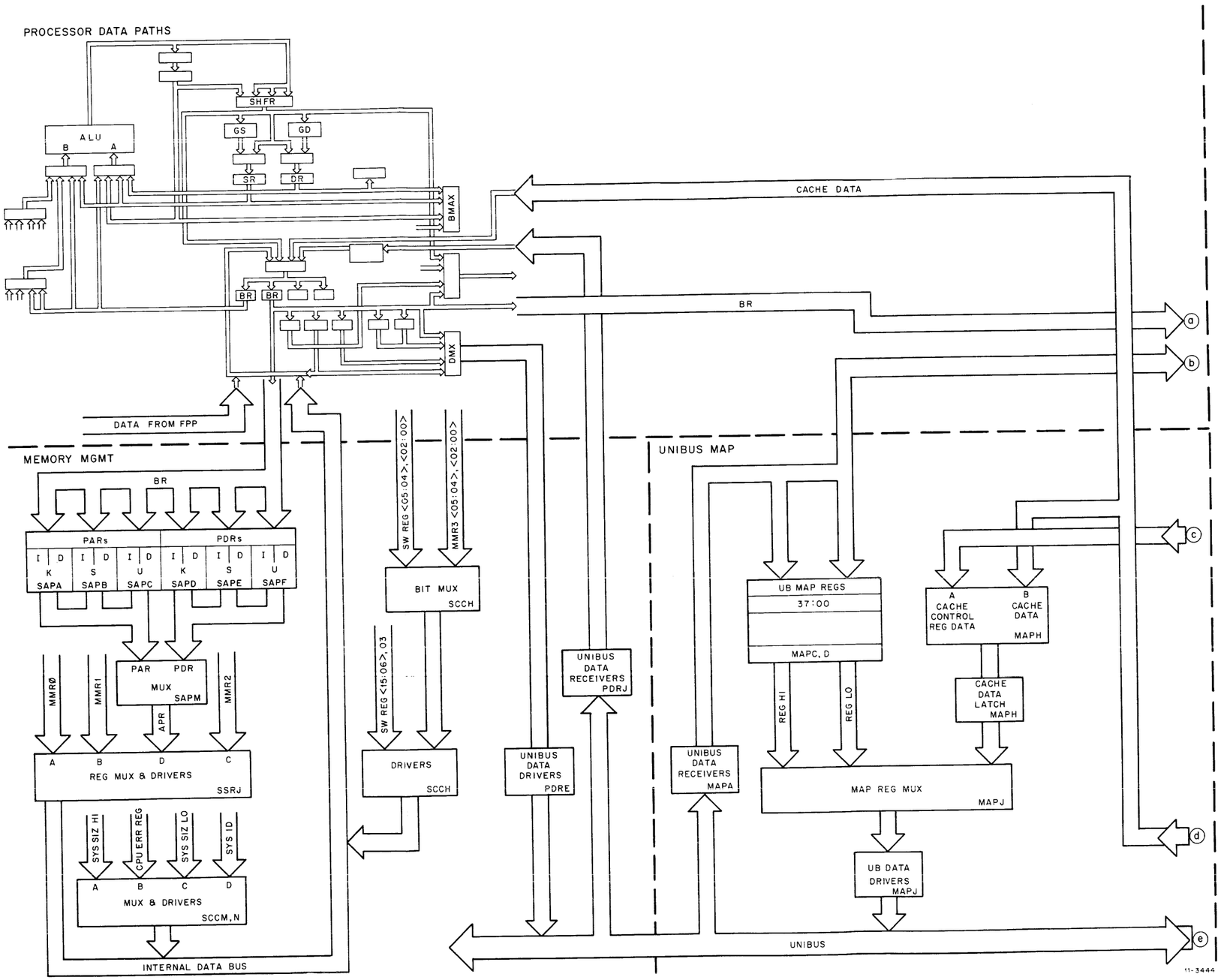


Figure H-1 PDP-11/70 Address Paths

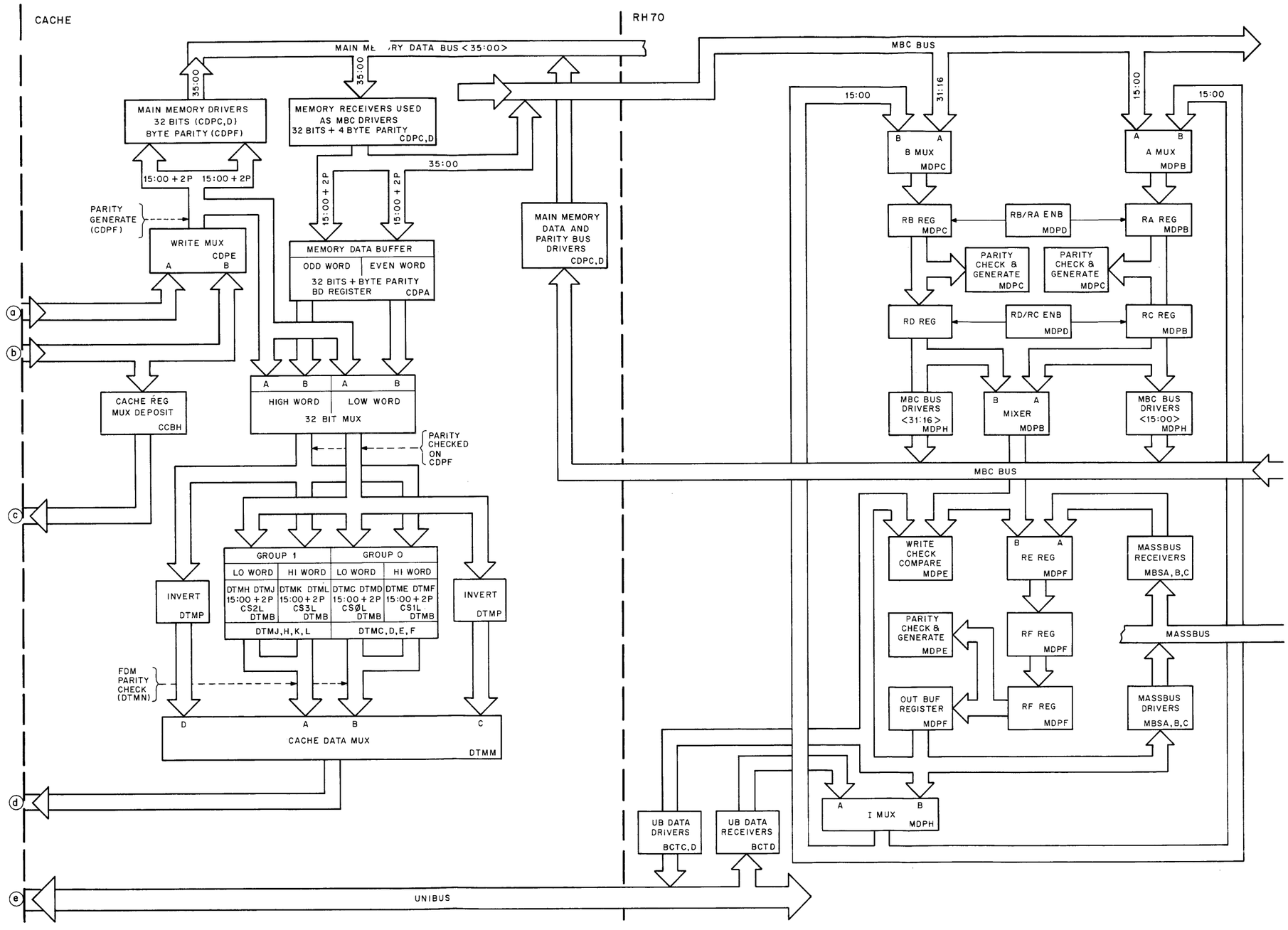


Figure H-2 PDP-11/70 Data Paths

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