TECHNICAL DOCUMENTATION CHANGE NOTICE

PDP-11/60
INSTALLATION AND
OPERATION MANUAL
(EK-11060-OP-002)
ERRATA SHEET

Replace the following pages with the revised pages included in this package.

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Model	DC Power Supplies	Comments
11X60-E	H7420A (7013050-0) H7420A (7013050-1)	7 S.U.s and 2 Quad SPC Expansion Space Available.
11X60-E	H7420B (7013050-2) H7420B (7013050-3)	Expansion Space Identical to the 11X60-BA.
11X60-C	H7420A (7013050-8)	1 S.U. and 2 Quad SPC Expansion Space Available in Base Card Cage.
11X60-C	H7420B (7013050-10)	Expansion Space Identical to the 11X60-CA. Expander Cage not included.
11Y60-E	H7420A (7013050-0) H7420A (7013050-0)	Expansion Space Identical to the 11X60-BA.
11Y60-E	H7420B (7013050-2) H7420B (7013050-3)	Expansion Space Identical to the 11X60-BA.
11Y60-I	H7420A (7013050-8)	Expansion Space Identical to the 11X60-CA. Expander Cage not included.
11Y60-I	H7420B (7013050-10)	Expansion Space Identical to the 11X60-CA. Expander Cage not included.
11S60-B	H7420A (7013050-0)	5 S.U.s of Expansion Space Available.
11S60-B	H7420B (7013050-2) H7420B (7013050-3)	Expansion Space Identical to the 11S60-BA.
11S60-B	H7420A (7013050-0) H7420A (7013050-1)	Expansion Space Identical to the 11S60-BA.
11S60-B	H7420B (7013050-2) H7420B (7013050-3)	Expansion Space Identical to the 11S60-BA.

NOTE:M
Btu/hr.

Table 2-5 PDP-11/60 Diagnostics

DOC/Order Codes	Title
MAINDEC-11-DQKDA	KD11-K Basic Logic Tests
MAINDEC-11-DQKDB	PDP-11/60 Trap Tests
MAINDEC-11-DQKTA	PDP-11 Memory Management Diagnostic
MAINDEC-11-DZQMC	0–124K Memory Exerciser
MAINDEC-11-DQKKA	PDP-11/60 Cache Diagnostic
MAINDEC-11-DQFPA	PDP-11/60 Floating Point Unit, Basic Instruction Tests
MAINDEC-11-DQFPB	PDP-11/60 Floating Point Advanced Instruction Tests
MAINDEC-11-DQFPC	PDP-11/60 Floating Point Unit Instruction Exerciser
MAINDEC-11-DQFPD	PDP-11/60 Floating Point ADD/SUB/MUL/DIV Exerciser
MAINDEC-11-DZDLD	DL11-W Diagnostic
MAINDEC-11-DQKDC	PDP-11/60 Series CPU Exerciser
MAINDEC-11-DZKAQ	PDP-11 Power Fail Tests
MAINDEC-11-DZM9A	PDP-11/60 Bootstrap/Terminator (M9301, M9400)
MAINDEC-11-DZKUA	Unibus System Exerciser
MAINDEC-11-DZKUB	Unibus Exerciser Module Diagnostic
MAINDEC-11-DZMML	MS11-K MOS Memory Tests
MAINDEC-11-DQM9A	PDP-11/60, PDP-11/70 ROM Bootstrap/Test Program (Document for listing at M9301-YH)
MAINDEC-11-DQKUA	PDP-11/60 WCS Diagnostic
MAINDEC-11-DQFPE	PDP-11/60 Hot Floating Point Diagnostic
MAINDEC-11-DQKUB	KD11-K Microdiagnostics (DCS Listing and Error Dictionary)

2.5.5.3 DEC/X11 System Exerciser – DEC/X11 is a system exerciser, i.e., it is an operating system that runs all devices in a system, using random data. Any errors are reported.

DEC/X11 must be configured for each individual system. The *DEC/X11 User's Documentation and Reference Guide*, MAINDEC-11-DXQBA, contains all information required to configure and run DEC/X11 and to interpret the results of the tests performed. The XXDP DEC/X11 Programming Card, MAINDEC-11-DZZPA, contains a summary of DEC/X11 features.

Turn to the system exerciser section of installation checklist and prepare to load DEC/X11. The system exerciser checklist numbering sequence begins with IBXXXX. To start the DEC/X11 package, refer to notes at the beginning of the system exerciser section of the installation checklist. Device test module QABM is used for the PDP-11/60.

2.5.6 Summary and Final Acceptance

Go through each chapter of the *PDP-11 Family Field Installation and Acceptance Procedure* and ensure that all areas requiring an initial are so marked. If an initial is missing, investigate that section and complete if necessary.

Ensure that all paperwork is complete. The field service and/or installation reports should reflect any problems/repairs encountered during the installation. After completion, the reports and checklists should be returned to the office.

The installation is now complete. Have the customer sign the field service report reflecting installation activity.

2.6 EXPANSION INSTALLATION

Add-on installation may be:

1. System Unit (SU) options
2. Rack-mounted options
3. Cabinet options

Installation in an existing system consists of:

1. Determination of the best electrical and physical position of the option on the Unibus. Guidelines are supplied in Paragraph 2.6.2 to aid in this determination.

2. Mechanical installation of the option.

2.6.1 Mechanical Installation

1. SUs are mounted in BA11-P boxes. All required information is supplied in the *PDP-11/60 Cabinet and Power Supply Manual.*

2. Refer to Figures 1-8 through 1-15 (configuration diagrams) for the amount of expansion space available in the processor cabinet. Any additional small peripheral controllers (SPCs) should be mounted with other I/O devices in the system, because of the potential cable congestion problem that may arise from the PDP-11/60's requirement to build the memory and I/O Unibus on separate cables.

3. Instructions for installation of rack-mounted and cabinet options are contained in their respective manuals.

2.6.2 System Configuration (Unibus)

NOTE

System configuration is a function not only of the variables mentioned below, but also of size, available space, and power distribution. These factors are not discussed here, but must be taken into consideration when a system is reconfigured.

BATT (Battery) – Battery monitor indicator. This indicator will function only in machines containing the battery backup option and has the following four states:

OFF – Indicates either no battery present, or battery depletion if battery is present.

ON (continuous) – Indicates that battery is present and is charged.

Flashing (Slow) – Indicates battery is charging.

Flashing (Fast) – Indicates loss of power and battery is discharging while maintaining MOS memory contents.

3.2.1.3 BOOT/RUN/HALT Slide Switch – Power-up action is determined by this switch's position, in conjunction with PANEL LOCK status. If the rotary switch is in LOCK position (deactivating all keypad functions), inadvertent operation of the slide switch has no effect. Upon power-up, the slide switch is treated as if it were in the RUN position, regardless of its physical position. If the battery is depleted (MOS memory system), RUN is altered to a BOOT action.

If the console is not in LOCK position, and power fail occurs, three choices of recovery (BOOT, RUN, and HALT) are available.

BOOT – Power-up to the M9301-YH bootstrap terminator.

RUN – Power-up to location 24, which contains the power-up vector. Note that this action occurs independent of battery status on a MOS memory system.

HALT – Power-up to the console. The CONSOLE light is illuminated and the console keypad switches are active.

3.2.1.4 Rotary Switch
STD BY – Removes dc power from processor and core memory (MOS memory battery charger is still on) and removes dc power from switched outlets (used for peripherals included in the system) on the 866D power controller.

POWER – Applies power to all units. All console controls are operable in console mode.

LOCK – Deactivates all keypad functions. With power switch in LOCK position, the position of the BOOT/RUN/HALT slide switch has no effect when power-up occurs; it is treated as if it were in the RUN position, unless a battery depletion causes BOOT within a system containing MOS memory.

R1 – Local control is deactivated to allow operation from a remote console. The octal display on the console will be blanked.

R2 – Console action is the same as R1.

3.2.1.5 Keypad Switches – The keypad contains twenty switches that are priority encoded into a unique 5-bit code. Simultaneous operation of the keys will allow the operation of the switch with the higher priority. The following paragraphs list the switches in order of their priorities with the highest priority listed first.

0–7 NUMERICS – Activation of any of the numeric keys causes the binary value of that key to be entered into the low-order three bits of the Temporary Switch Register (TMPSW). The previous contents are left shifted three bits. Each 3-bit binary value is displayed in octal. For each additional numeric key pressed, the TMPSW (one of four internal registers) is left-shifted three bits and the octal display is left-shifted one digit. Consequently, a 6-digit octal number is generated as octal digits enter from the right and are left-shifted. Operation of the numerics occurs in both console mode and run mode.

NOTE

The CNTRL (control) key is used in conjunction with some keys to prevent accidental operation of certain functions. When used, the CNTRL key must be pressed first and held down while the other key is pressed. Those keys that are interlocked with the CNTRL key are indicated with an asterisk.

HALT/SI (Halt/Single Instruction – Pressing this switch while the processor is in run mode will halt the processor, between instructions, after outstanding trap sequences and before bus requests. The processor is then put into console mode and the console indicator is illuminated.

The octal display indicates the program counter for both HALT and SINGLE INSTRUCTION functions. Pressing the HALT/SI switch, while in console mode, now causes a single instruction to be executed.

To initialize the system without a program start, it is necessary to press the HALT/SI key while holding the START switch down.

NOTE

The PDP-11/60 differs from other PDP-11 processors regarding the single instruction step function. An operator cannot simply load an address and immediately start single-stepping. To start from an arbitrary address, the program counter (PC) must be loaded using the maintenance key function; one can then single step by pressing the HALT/SI switch. Refer to the MAINT (Maintenance) paragraph for procedures to read from and write into the general-purpose registers.

(D)SWR, *(L)SWR (Display Switch Register, Load Switch Register) – A dual action key, when pressed and not used in conjunction with the CNTRL key the contents of the console switch register (CNSL SWR) are displayed, in both console and run modes.

If this switch is pressed while the CNTRL switch is held, the contents of the TMPSW are loaded into the CNSL SW. The contents of the CNSL SW are displayed. This switch is operative in both console and run modes.

13. Press the HALT/SI key.

NOTE

The processor has just performed the move instruction (010021) that was contained in memory address 000000, refer to the note preceding Step 13. 0.0.0.0.0.2 will be displayed; this is the address to which the PC is now pointing. When the HALT/SI key is pressed again, the processor will have performed the jump instruction (000112) contained in that memory location. Since the instruction says to jump to the address specified in R2, the PC (R7) will contain all zeros (contents of R2) and the display will contain all zeros.

To determine that the move instruction has been performed, read the contents of R1, (Steps 4, 5, and 6 in Paragraph 3.3.2.4). The contents will have incremented from 000006 to 000014.

3.3.2.7 Continue Procedure for Program No. 1 – This program can be run, in its entirety, from its present location, without beginning at the starting location by pressing the CONT key while holding in the CNTRL key. The same results as shown in Figure 3-2 will occur, as if we had begun at the starting location with the contents of R1 being memory address 000012.

3.3.2.8 Memory Loading Procedure for Program No. 2 – Refer to Table 3-2 if console procedures are known.

1. Press numeric keys 2–0–0.
2. Press the (L)ADRS key.
3. Press numeric keys 0–6–2–7–0–0.
4. Press the DEP key.
5. Press the numeric keys 1–0.
6. Press the DEP key.
7. Press the numeric keys 0–1–0–0–3–7.
8. Press the DEP key.
9. Press the numeric keys 1–7–7–5–7–0.
10. Press the DEP key.
11. Press the numeric key 0.
12. Press the DEP key.

3.3.2.9 Register Loading Procedure for Program No. 2

1. Press the numeric keys 2–0–0.
2. Press the (L)SWR key while holding in the CNTRL key.
3. Press the numeric keys 1–0.
4. Press the MAINT key while holding in the CNTRL key.

3.3.2.10 Memory Checking Procedure for Program No. 2

1. Press numeric keys 2–0–0.
2. Press the (L)ADRS key.
3. Press the EXAM key, 062700 should be displayed.
4. Press the EXAM key, 10 should be displayed.
5. Press the EXAM key, 010037 should be displayed.
6. Press the EXAM key, 177570 should be displayed.
7. Press the EXAM key, all zeros should be displayed.

3.3.2.11 Register Checking Procedure for Program No. 2

1. Press numeric key 0.
2. Press the (L)SWR key while holding in the CNTRL key.
3. Press the MAINT key while holding in the CNTRL key, 000010 should be displayed.

3.3.2.12 Starting Procedure for Program No. 1

1. Press numeric keys 2–0–0.
2. Press the (L)ADRS key.
3. Press the START key while holding in the CNTRL key.

NOTE

The display should contain the next memory address following the last instruction. The last instruction being located in memory address 210; the PC should be pointing at location 212.

4. Press the (D)ADRS key. This action displays the result of the program.

3.3.2.13 Console Switch Register Read/Write* Procedure – The address 177570 is the CNSL SW's Unibus address. To write in this address, from the console, the following procedure must be performed:

1. Load the TMPSW with the data to be written by pressing the applicable numeric keys.
2. Press the (L)SWR key while holding in the CNTRL key.
3. Press the numeric keys 7–7–7–5–7–0.
4. Press the (L)ADRS key.
5. Press the EXAM key.

The number you loaded in Step 1 should be displayed in the octal display. Figure 3-3 is a block diagam of the console registers (TMPSW, CNSL ADRS, CNSL SW, etc.) transfer process. For more detailed programming information, refer to the *PDP-11/60 Processor Handbook*.

*The console switch register cannot be written into via the conventional method (i.e., Load Address, Deposit, etc.). The first two steps of this procedure automatically load the console switch register. Steps 3, 4, and 5 are for reading the register.