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KY11-A programmer's console manual

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CHAPTER 1
INTRODUCTION

The KY11-A Programmer's Console provides the PDP-11/20 System with a necessary and useful programmer interface. This manual discusses the details of switch operation at the console flow diagram level with references to the specific logic implementation of the KA11 Processor. (See Drawing D FD KY11-A-CF at end of Chapter 2.) Power-fail operation is also discussed. The details of switch and display operation are presented in the *PDP-11/20 System Manual,* DEC-11-HR1B-D.

The KY11-A console physically consists of a single large circuit board, which fits into the first module location of the KA11 Processor. The circuit board contains switches, lamps, and logic; however, only the logic for the lamp drivers and switch filters are contained on this board. The control logic is within the KA11 Processor on the M724 Bus and Console Control module. The details of logic implementation require reference to the discussion and drawings associated with this module in the *KA11 Processor Manual,* DEC-11-HR2B-D.

Power-fail operation is presented with the console function because it can be activated with the console OFF/POWER/PANEL LOCK switch. The more usual and functional role of power fail is activation by disruption of input ac power. Power interruption traps the machine to the pre-assigned location, 000024. A subroutine (less than two milliseconds long) with a terminal HALT instruction is used to store volatile information and set a program flag indicating power is down. Upon restoration of ac power, the trap routine is again entered with address vector 000024. The previously set program flag is used by the subroutine to reload the stored information and restart the previously interrupted main program. This manual contains both flow diagrams and waveforms for the power-fail operation. The logic implementation is covered in the *KA11 Processor Manual* on the M825 Power Fail and Control module and the M824 Priority module.

CHAPTER 2
CONSOLE FUNCTIONS

The various console functions are presented in the following paragraphs with reference to the implementing signals and conditions.

2.1 LOAD ADDR

The LOAD ADDR function provides the means for an operator to manually insert the starting address of a program or the address for an examine (EXAM) or deposit (DEP) function.

When the LOAD ADDR function is used, the console is in control of the KA11 Processor and the Unibus®. Therefore K1-2 CLK RUN is in the 0 state; K1-2 CLK OFF is in the 1 state; K13-4 CONSF is in the 1 state and bus busy (BBSY) is asserted.

An address is inserted into the switch register (SR) and the LOAD ADDR key is depressed. Depression of this key starts the console timing. The timing is generated by the circuits shown on diagram K13-4 of the *KA11 Processor Manual* and proceeds through one complete cycle of operation which terminates with the signal P1 CSR0. The LOAD ADDR key also causes generation of the signal GATE BUS ← SR K13-2 which gates the SR contents to the Unibus and resets both K13-4 EXAMF and K13-4 DEPF. Time state K13-4 CSR1 is the first console time state to be entered. The K6-2 SET DATA WAIT signal occurs as a function of K13-4 P1 CSR and directly sets the K6-2 DATA WAIT flip-flop. The DATA WAIT clears LATCH A, LATCH B, and CARRY 00; and asserts the K6-4 GATE B ← B D15/0 signal. At this time the BUS D lines are loaded into the latches; the K13-4 P2 CSR signal directly sets the latches; and the SR value is stored in LATCH B with LATCH A cleared. The setting of LATCH A produces the 100-μs K6-2 P CLR DATA WAIT pulse which clears the DATA WAIT flip-flop.

The next console time state to be entered is K13-4 CSR3. The contents of the latches are applied through the adders and the output of the rotate/shift gating (K7 and K8) is applied directly to the D inputs of the bus address register (BAR). The time state signal, CSR3, creates the K13-3 CLK BAR signal which loads the BAR. The K4-2 RA/TEMP signal also appears and sets up the TEMP register addressing on K5-2. The K4-3 WRITE ENABLE 15/8 and WRITE ENABLE 7/0 signals appear during CSR3 time and the K13-4 P1 CSR signal activates K1-2 WRITE 15/8 and WRITE 7/0 signals. These latter two signals cause the output of the rotate/shift gating to be loaded into the TEMP register.

Console time state K13-4 CSR2 is entered next and clears K6-5 CARRY 00 and generates the K6-2 CLR LATCH A and CLR LATCH B signals. These signals set up the D inputs to both latches which are gated to 0 by the K1-2 REG GATE signal. The REG GATE signal appears at K13-4 P2 CSR time and clocks both latches. The K13-4 P3 CSR causes the K1-2 REG LATCH signal to be ANDed with K6-2 DATA WAIT (0) H signal to close both latches. At this point, the LOAD ADDR operation is complete. The console timing proceeds to CSR0 to complete the sequence. At no time during the operation was the KA11 Processor clock turned on nor was console control relinquished.

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2.2 EXAM

The examine (EXAM) function provides the means by which an operator can examine the content of a location. Note that EXAM is for addresses on even boundaries only.

2.2.1 Operation

When the EXAM function is used, the console is in control of the KA11 Processor and the Unibus. Therefore, K1-2 CLK RUN is in the 0 state; K1-2 CLK OFF is in the 1 state; K13-4 CONSF is in the 1 state and bus busy (BBSY) is asserted. The previous operation of LOAD ADDR has loaded the bus address register (BAR) and TEMP register.

Depression of the EXAM key starts a complete cycle of console timing which terminates with K13-4 P1 CSR0. The EXAM key causes direct reset of the K13-2 TIME DATA and TIME OUT flip-flops. If the address in the BAR is not an internal register address and K1-2 CLK OFF is in the 1 state, the K2-3 PARTIAL BSR ← 1 signal is generated. This signal indicates that a bus cycle is entered when BSR1 occurs and a DATI cycle occurs.

Depression of the EXAM key causes direct reset of K13-4 DEPF and setting of K13-4 EXAMF. If this is the second sequential EXAM key depression, the K13-4 INCF (increment flag) signal is generated as a result of ANDing EXAMF and EXAM. The INCF signal sets up the necessary gating for updating the current address 'ocation in TEMP to the next sequential location.

Console time state K13-4 CSR1 is entered. The CSR1 signal produces K4-2 RA/TEMP, K6-4 GATE B ← R 15/8 and K6-4 GATE B ← R 7/0 signals. These three signals qualify the gating of the contents of TEMP into LATCH B during the P2 CSR time pulse. If the INCF signal is present, K6-5 CARRY 00 1 occurs. The INCF signal also generates K6-5 ADD + 2 signal if the address in the BAR is not an internal register address (defined by the absence of the REG ADRS signal). The ADD + 2 signal causes gating of the true and complement conditions of R0 into LATCH A at P2 CSR. When REG ADRS signal is present, the INCF signal causes the address in the TEMP register to be incremented by 1; otherwise, the TEMP register is incremented by 2. The latter conforms to addressing on even boundaries. Unlike the normal KA11 program operation which increments the address after loading the BAR, incrementing of the EXAM register occurs just prior to loading the BAR. This allows the console ADDRESS indicators to display the actual address of the location which was examined.

Time state K13-4 CSR3 is entered next. The K4-2 RA/TEMP, K4-3 W/ENABLE 15/8, K4-3 W/ENABLE 7/0 and K13-3 CLK BAR signals are generated. The CLK BAR signal causes the output of the DATA PATHS gating to be clocked into the BAR. These same D lines are applied to the inputs of the K5-2 REGISTER. When K13-4 P1 CSR occurs, the K1-2 WRITE 15/8 and K1-2 WRITE 7/0 signals load the TEMP register. At this time, the BAR and TEMP register are loaded with the address to be examined.

Entry is now made into console time state CSR2. The K6-5 CARRY 00 is cleared; and, since ISR0 is present, the K6-2 CLR LATCH A and K6-2 CLR LATCH B signals are generated. At K13-4 P2 CSR time, the K1-2 REG GATE signal clears the latches; and at K13-4 P3 CSR time, the K1-2 REG LATCH signal sets both latches. Simultaneously, in CSR2 the following may occur.

If the REG ADRS signal is present, the K6-4 ENABLE B ← R signal appears. At K13-4 P2 CSR time, the REG GATE signal occurs and produces the K6-4 GATE B ← R 15/8 and K6-4 GATE B ← R 7/0 signals. The K4-3 GATE RA ← BAR signal occurs throughout CSR2 and CSR0, due to the gating of K13-4 CSR0 (0) L [CSR0 (1) H], provided the REG ADRS and EXAM signals are present. The GATE RA ← BAR signal qualifies the gating of one of the internal registers to the latch inputs. When the GATE B ← R 15/8 and GATE B ← R 7/0 signals occur, the register value is gated into LATCH B. The latches are opened and closed to accept the value as previously described.

Console timing progresses to K13-4 CSR0. An EXAM with a REG ADRS has completed its cycle and no further action occurs. There are, however, other possible conditions which require further action. The conditions are described in the subsequent paragraph and are based upon the conditions noted.

2.2.2 Not REG ADRS

The K2-3 PARTIAL BSR ← 1 signal was established when the EXAM key was depressed. When console timing pulse, K13-4 P1 CSR0 occurs, the 100-μs K1-2 P CLK RESTART pulse is generated. This pulse starts the KA11 clock by direct setting K1-2 CLK RUN. The starting of the processor clock causes the BSR1 time state since the BSR loading was set up by BSR ← 1. The K13-2 DATI ← 1 signal is generated due to the absence of both DATO ENTRY, and DATIP ← 1 at BSR1 time. This produces a DATI cycle which terminates at BSR7 and R/W2. At the completion of the DATI, the content of the address of the BAR is in LATCH B with LATCH A cleared. The DATA lights indicate the content of the address examined. All normal DATI BSR time states are entered in their regular sequence. All BSR time state address modification gating is nullified by the EXAM signal. No activity occurs until BSR3 time. The BAR was set up with the address to be examined prior to entry into DATI. It is now applied to the bus along with the BUS C0 and C1 lines. Then MSYN is asserted and BSR7 entered. Time out is not possible since the EXAM switch holds both TIME DATA and TIME OUT in a rest condition. The BSR stays in state 7 since the processor clock is not allowed to restart. Control of the bus was never released by the console.

2.3 DEP

The deposit (DEP) function provides the means for an operator to deposit a quantity into an address location. Deposits are to addresses on even boundaries only.

When the DEP function is used, the console is in control of the KA11 Processor and the Unibus. Therefore K1-2 CLK RUN is in the 0 state; K1-2 CLK OFF is in the 1 state; K13-4 CONSF is in the 1 state and bus busy (BBSY) is asserted. The switch register (SR) switches contain the value to be deposited. The previous operation of LOAD ADDR has loaded the bus address register (BAR) and TEMP register.

Depression of the DEP key starts a complete cycle of console timing which terminates with K13-4 P1 CSR0. The DEP key directly resets the K13-2 TIME DATA and TIME OUT flip-flops. If the address in the BAR is not an internal register address and K1-2 CLK OFF is in the 1 state, the signal K2-3 PARTIAL BSR←1 is generated. The generation of this signal indicates that a bus cycle will be entered when BSR1 occurs and a DATO cycle occurs.

Depressing the DEP key directly resets the EXAMF and sets the DEPF. If this is the second sequential DEP key depression, the K13-4 INCF (increment flag) signal is generated as a result of ANDing DEPF and DEP. The INCF signal sets up the necessary gating for updating the current address location to the next sequential location.

Console time state K13-4 CSR1 is entered. The CSR1 signal produces the K4-2 RA/TEMP, K6-4 GATE B←R 15/8, and K6-4 GATE B←R 7/0 signals. These signals qualify the gating of the contents of the TEMP register into LATCH B during the P2 CSR time pulse. If the INCF signal is present, K6-5 CARRY 00←1 signal occurs. The INCF also generates the K6-5 ADD+2 signal if the address in the BAR is not an internal register address (defined by the absence of the signal REG ADRS). The ADD+2 signal causes gating of the true and complement conditions of R0 into LATCH A at the time of the P2 CSR pulse. When REG ADRS is present, the INCF causes the address in the TEMP register to be incremented by 1, otherwise it is incremented by 2. The latter conforms to addressing on even boundaries. Unlike the normal KA11 program operation which increments the address after loading the BAR, incrementing of the DEP occurs just prior to loading the BAR. This allows the console ADDRESS indicators to display the actual address of the location to which the deposit was made.

Time state K13-4 CSR3 is entered next and the K4-2 RA/TEMP, K4-3 W/ENABLE 15/8, K4-3 W/ENABLE 7/0 and K13-3 CLK BAR signals are generated. The CLK BAR signal causes the output of the DATA PATHS gating to be clocked into the BAR. These D lines are also applied to the inputs of the K5-2 REGISTER. When the K13-4 P1 CSR signal occurs, the signal K1-2 WRITE 15/8 and K1-2 WRITE 7/0 signals load the TEMP register. At this point, the BAR and TEMP registers have the address to which the deposit applies.

Entry is now made into console time state CSR2. The K6-5 CARRY 00 is cleared, and, since ISR0 is present, the K6-2 CLR LATCH A and K6-2 CLR LATCH B signals are generated. At the time of K13-4 P2 CSR the K1-2 REG GATE signal clears the applicable latches; and at K13-4 P3 CSR time, K1-2 REG LATCH signal sets both latches. The K4-3 GATE RA←BAR signal occurs throughout CSR2 and CSR0, due to its gating by the K13-4 CSR0 (0) L [CSR0 (1) H] signal, provided REG ADRS and DEP signals are present. The GATE RA←BAR signal qualifies the gating of one of the internal registers to the latch inputs. When GATE B←R 15/8 and GATE B←R 7/0 signals occur, the register value is gated into LATCH B. The latches are opened and closed to accept this value as previously described.

Simultaneous with the CSR2 time state the following occurs.

The signal K13-2 GATE BUS←SR gates the content of the SR into the Unibus D lines. The occurrence of K13-4 P1 CSR generates the 100-ns K6-2 P SET DATA WAIT pulse, which sets the DATA WAIT flip-flop. The DATA WAIT flip-flop produces the 50-ns K6-2 P CLR LATCHES pulse which, in turn, clears both latches and causes the K6-4 GATE B←B D 15/0 signal which gates the bus D lines into LATCH B. The presence of the K13-4 P2 CSR signal, when ANDed with DATA WAIT (1), sets both latches and the value of the SR is loaded into LATCH B with LATCH A cleared.

Console timing progresses to K13-4 CSR0. In this time state there are various conditions and operations which may be required. They are described in the subsequent paragraphs according to the primary condition.

2.3.1 ST ADRS

The K10-4 GATE ST←D signal occurs; and, since the KA11 clock is off, GATE ST←D signal generates the K10-4 CLK N, Z, V, K10-4 CLK C, and K10-4 CLK T signals. These signals clock into the STATUS REG those bits of the DATA PATHS which correspond to their respective bits in STATUS. DATA PATHS D07, D06, D05, and D04 are directly applied to the D inputs of their respective STATUS bits and are clocked by CLK T. DATA PATHS D03, D02, and D01 are applied to the D inputs of their respective STATUS bits via K11-2 CODES DATA gating and are clocked by CLK N, Z, V. The D00 value is applied to the D input of the C STATUS bit via gating on K10-4 IR DECODE designated K10-4 C DATA. In this particular instance, the output of the Rotate/Shift gating, called D00, is not used but instead the output of the adder called ADD 00 is used. This provides the required polarity of signal in order to correctly load the C bit of STATUS.

2.3.2 REG ADRS

The GATE RA←BAR signal is still present from its generation in CSR2 and remains throughout CSR0. Therefore the selection of the register has been established and it is enabled. The K4-3 W/ENABLE 15/8 and W/ENABLE 7/0 signals also appear throughout CSR0. When the K13-4 P1 CSR signal occurs, the K1-2 WRITE 15/8 and WRITE 7/0 signals appear and cause the loading of DATA PATH data into the selected register.

2.3.3 Not REG ADRS

The K2-3 PARTIAL BSR←1 signal was established when the DEP key was depressed and when timing pulse K13-4 P1 CSR0 occurs, the 100-ns K1-2 P CLK RESTART pulse is generated. This pulse starts the KA11 clock by setting the K1-2 CLK RUN flip-flop. The processor clock causes BSR1 since BSR loading was established by BSR←1 signal. With K1-2 CLK OFF in the 0 state, due to the starting of the clock, and the DEP signal present, the K13-2 DATO ENTRY signal occurs. This sets up a DATO bus operation which terminates at BSR8 and R/W2. The data from the SR has been transferred to the BAR at the completion of the DATO. The DATA display indicates the data which was deposited.

All normal DATO BSR time states are entered in their normal KA11 Processor sequence; however, all address modification in BSR 1, 3 and 7 is nullified by the existence of the DEP signal. The BAR was set up prior to

entry into the DATO. In BSR3 time the BAR is gated to the bus as is the BUS C0 and C1 lines. These signals are true for the balance of the DATO. The next action to occur in a DEP is at BSR12 when the SR content is transferred to the bus and MSYN asserted. Time out is not possible since the DEP switch holds both TIME DATA and TIME OUT flip-flops in a reset condition. The BSR8 time state is entered and the cycle terminates regardless of whether SSYN is received or not. The KA11 clock does not restart and BSR8 is retained until some new operation occurs. Since console timing has finished and the processor clock has stopped, the control is at the console because bus control via CONSF (1) was never relinquished.

2.4 CONT

The continue (CONT) function provides for the continuance of a program sequence from the point of interruption (a HALT for instance) without initialization.

When the CONT function is used, the console is in control of the KA11 Processor and the Unibus. Therefore K1-2 CLR RUN is in the 0 state; K1-2 CLK OFF is in the 1 state; K13-4 CONSF is in the 1 state and bus busy (BBSY) is asserted.

Depression of the CONT key clears K13-4 CONSF to the 0 state. The BBSY signal, resulting from CONSF, is negated. The K2-3 PERIF RELEASE and K2-3 D PERIF RELEASE signals occur and generate the 100-μs K1-2 P CLK RESTART pulse, which starts processor operation. The first SCLK change, after K1-2 CLK RUN is set to the 1 state, clocks PERIF RELEASE and sets the KA11 Processor's K12-3 BBSYF to the 1 state. This places the KA11 Processor in full control and instructions are sequenced according to the program.

2.5 HALT

The HALT function provides a means to manually stop processor operation. Operation ceases in a manner determined by the position of the S-INST/S-CYCLE switch.

Assume the KA11 Processor is in control and the ENABLE/HALT switch is in the ENABLE position. When the ENABLE/HALT switch is moved to the HALT position, the K13-4 CONS BR signal or K13-4 CONS NPR signal is generated. The CONS BR signal occurs if the S-INST mode is enabled; CONS NPR occurs if the S-CYCLE mode is enabled. The HALT condition disables the K13-2 RESTART clocking for PWR UP conditions and also disqualifies the D input to K3-3 PDNF and the gate for setting K3-3 PUPF.

The CONS NPR or CONS BR signals are used on the K3-2 PRIORITY module on the D inputs of the K3-2 CNPRF or the K3-2 CBRF. The K2-3 CLK BR signal clocks the enabled flip-flop to the 1 state. Should CNPRF be set, it disqualifies the K3-2 NPRF signal and disables all gating for K3-2 PROC BG ⟨07:04⟩ and BRQ thereby disallowing any further bus NPR's or bus BR's to be granted. The CNPRF also disqualifies the gating for the K3-2 CBRF signal. This gating established the console NPR's as the highest possible priority. If CBRF is set, it also disqualifies all bus NPR and bus BR grants but it can be overridden by CNPRF. Console BR, therefore, is the second highest priority for the KA11 Processor.

The CBRF (1) signal generates the K2-3 REQUEST signal which is ANDed with SERVICE * ISR0 signal and, if K12-3 TRAPS signal is not present, the K2-2 PROC RELEASE signal is asserted. The signals - (TRAPS) * CBRF * SERVICE * ISR0 enable the D input of K12-3 CONS GRANT which is set to a 1 state during R/W2 time. The CBRF signal is used to disqualify the gating of K1-4 FETCH←1 so that SERVICE is entered upon completion of the present instruction.

The CNPRF (1) signal is ANDed with the K12-3 NPR ENTRY signal to enable the D input to K12-3 CONS GRANT which is clocked at R/W2 time. The NPR ENTRY signal establishes those points in the machine operation when NPR's can be serviced. The K2-2 PROC RELEASE is generated as a result of both NPR ENTRY and CNPRF (1) signals.

At this point, CONS GRANT is set by one of two possibilities and the PROC RELEASE signal is generated. The CONS GRANT (1) signal causes setting of the K13-4 CONSF and resetting of the K13-4 EXAMF and the K13-4 DEPF.

The PROC RELEASE signal disqualifies gating on the K1-2 Timing and Status module so that the CLK RUN is not allowed to be set. The KA11 clock is stopped or kept from restarting by the presence of the PROC RELEASE signal.

The following conditions exist with the CONSF (1) signal present: (1) the CNPRF is set; (2) CBRF, NPRF, BR ⟨ 07:04 ⟩ are all reset on the Priority module; (3) CONS GRANT is reset; (4) K4-3 W/ENABLE 15/8 and 7/0 are disqualified at BSRT time ; (5) K2-2 WAITING and K2-3 CLK BR are disqualified; (6) BBSYF is reset; and (7) K15-2 NPR ENABLE is disqualified. The presence of the CONSF signal disables any bus transfers, turns off the KA11 Processor bus control, and transfers bus control to the console. It also disables any writing into the internal registers during a bus cycle while the console is in control.

With the processor clock stopped, K1-2 CLK RUN is in the 0 state and K1-2 CLK OFF is in the 1 state. The CONSF is in the 1 state and its BBSY asserted, bringing the machine to the normal console control idle state.

2.6 START

The START function provides the means to initialize the entire PDP-11/20 system and to begin execution of the instruction specified by a previous LOAD ADDR operation.

With the console in control of the KA11 processor and the Unibus, the following signals are present: K1-2 CLK RUN (0), K1-2 CLK OFF (1), K13-4 CONSF (1), and BBSY is asserted by CONSF (1). Prior to depression of the START key, it is assumed that the operator had previously inserted the program starting address with the LOAD ADDR operation. If the LOAD ADDR has not been done, the starting address is the unspecified contents of the TEMP Register and LATCH A.

Depressing the START key results in the generation of the KY3 START L and KY3 INIT L signals. The START signal is applied to the clock input of K13-4 STARTF and upon switch release, clocks the flip-flop to a 1 state. The KY3 INIT L signal occurs during switch depression and produces K13-2 INIT and BUS INIT signals. The INIT signal is applied throughout the KA11 to initialize all flip-flops, shift registers, decoders, etc., to those conditions necessary for machine start up. The following is a listing of asserted conditions after application of INIT:

K1-2 CLK RUN (0)

K1-2 CLK OFF (1)

K1-2 R/W 0 (0)

K1-2 R/W 1 (1)

K1-3 ISR0

K1-3 BSR0

K1-4 SERVICE

K3-2 CNPRF (1)

K3-2 CBRF (0)

K3-2 NPRF (0)

K3-2 BR7 (0)

K3-2 BR6 (0)

K3-2 BR5 (0)

K3-2 BR4 (0)

K3-3 PDNF (0)

K3-3 PUPF (0)

K6-2 DATA WAIT (0) Done via WAIT CLR signal

K9-2, K9-3, K9-4, K9-5 } BAR 17/00 (0)

K9-3, K9-4, K9-5 } IR 15/00 (0)

K9-4 ST 07/05 (0)
K9-4 T (0)
K9-5 N (0)
K9-5 Z (0)
K9-5 V (0)
K9-5 C (0)
K12-2 OVFLF (0)
K12-2 BERRF (0) Done via CLR FLAGS signal
K12-2 HALTF (0)
K12-3 TRACF (0)
K12-3 TRAPF (0)
K12-3 INTRF (0)
K12-3 CONS GRANT (0) Done via CONSF (1) signal
K12-3 BBSYF (0) Done via CONSF (1) signal
K13-2 TIME SACK (0)
K13-2 NO SACK (0)
K13-2 TIME DATA (0)
K13-2 TIME OUT (0)
K13-2 BC0 (0)
K13-2 BC1 (0)
K13-3 MSYN (0)
K13-3 SSYN (0)
K13-4 CSR1 (0)
K13-4 CSR0 (0)
K13-4 EXAMF (0)
K13-4 DEPF (0)
K13-4 CONSF (1)
K15-2 ACLOF (0)

The BUS INIT signal is applied to all devices along the Unibus and causes initialization in accordance with their individual specifications. This signal enters the KA11 via the bus to reset K2-3 BR PTR and K2-3 NPR PTR.

Release of the START key sets the STARTF and starts the console timing cycle which terminates with a P1 CSR0 pulse.

Console time state K13-4 CSR1 is entered and this produces K4-2 RA/TEMP signal which selects the TEMP register for reading its data into the LATCH B. The CSR1 time state also produces the K6-4 ENABLE B←R signal. At the time of K13-4 P2 CSR, the K1-2 REG GATE signal occurs and gates the TEMP register into LATCH B. Simultaneously, with the REG GATE signal, LATCH B is opened because the ENABLE B←R signal is present. When the K13-4 P3 CSR signal occurs, this is gated with K6-2 DATA WAIT (0) signal to close LATCH B. LATCH A had been cleared by the LOAD ADRS operation and should still be in that condition. The result of this series has been to place the contents of the TEMP register into LATCH B. The LOAD ADRS was not the operation prior to the depression of the START key, then LATCH B contains the last value stored in the TEMP register by the processor operation.

The console time state K13-4 CSR3 is entered. The K4-2 RA/PC signal is generated which causes the register addressing to select the Program Counter (PC). The CSR3 time state also results in the generation of the K4-3 W/ENABLE 15/8 and K4-3 W/ENABLE 7/0 signals. The output of the DATA PATHS is clocked into the BAR due to generation of the K13-3 CLK BAR signal by CSR3. The K13-4 P1 CSR pulse writes the DATA PATHS data into the PC. At this point, the PC has just received the starting address for program operation.

The next time state to be entered is K13-4 CSR2. Since the ISR state is 0, this time state generates the K6-2 CLR LATCH A and K6-2 CLR LATCH B signals. These two signals open both latches upon application of the K1-2 REG GATE signal which results from the K13-4 P2 CSR. The K1-2 REG GATE signal is ANDed with K6-2 DATA WAIT (0) and results in the closing of both latches. This REG GATE signal is produced by the K13-4 P3 CSR timing pulse. The CSR2 signal also clears K6-5 CARRY 00.

Operation progresses to time state K13-4 CSR0. In this time state, the position of the ENABLE/HALT switch effects operation. If this switch is in the HALT position, then operation returns to the console via a modified version of the HALT operation. Modification means that most of the functions of the KA11 have been initialized by the INIT signal. Part of the HALT operation, therefore, has been set up before entry. In any case, the STARTF is reset by K13-4 P1 CSR0 signal.

If the ENABLE/HALT switch is in the ENABLE position, the presence of P1 CSR0 in START clocks K13-4 CONSF to a 0 state and CONSF (0) negates BBSY. This produces the K2-3 PERIF RELEASE signal and after a 600-microsecond delay produces the K2-3 D PERIF RELEASE signal. The K12-3 BBSYF signal is set when PERIF RELEASE signal appears thereby giving the KA11 Processor control of the bus. Occurring simultaneously with the PERIF RELEASE signal is the K15-2 FETCH ← SVC signal which produces the K1-4 FETCH ← 1 signal. This creates the loading input K1-3 BSR←1 signal (the output of E48 pin 8). The D PERIF RELEASE signal produces the K1-2 CLK RUN signal to be set via the K1-2 P CLK RESTART signal. The first K1-2 SCLK signal change, upon restarting the processor clock, places the KA11 Processor into FETCH * ISR0 * BSR1 and continues operation.

2.7 POWER FAIL

The power fail function of the PDP-11/20 System provides sufficient hardware sequences to allow programming accommodation of ac input power interruptions. Total system performance from several system elements is required: the power supplies (usually H720 supplies) must properly sequence the ACL0 and DCL0 signals; the Unibus "wire OR's" the signals from the power supplies for system use; the KA11 processor provides trap operation for program response; and volatile memories protect their contents when supply voltages become unstable.

This section of the manual reviews basic operation of the power fail function and presents the trap sequence effected by the KA11 processor. The description of the logic implementation is given in the KA11 Processor Manual on the M825 Power Fail and Control module and the M824 Priority module. Details of operation pertaining to power fail in the non-processor elements are noted in their respective manuals.

2.7.1 Basic Operation and Power Fail Waveforms

The power fail sequence consists of two segments: power fail down and power fail up. The former occurs upon removal of power; and the latter occurs upon application of power. Fundamental to both is the proper sequence of the two Unibus power signals BUS ACLO L and BUS DCLO L. The importance of the sequence of these two signals for proper power fail operation is such that the KA11 processor provides a sequence in parallel with the initiating sequence.

A normal sequence is shown in Figure 2-1 and in the waveforms on the KY11-A console flow diagram. Upon removal of ac power, the signal ACLO is activated by a power supply and initiates a power fail down sequence. Once the sequence is started, it must be completed. If the restoration of ac power removes the power signals from the power supply, the power signals of the KA11 processor provide for completion of the power fail down sequence and the initiation of a power fail up sequence. (Refer to waveforms on processor drawing K15-2 of KA11 Processor Manual.)

Seven milliseconds of proper dc supply voltages are required for machine operation after activation of the ACLO signal. During this time, the program response (2 milliseconds, maximum) is made to the power interruption. The DCLO signal occurs and indicates that the logic supply voltages are no longer sufficient to ensure reliable operation. The KA11 processor generates an initializing signal, BUS INIT L (K13-2), and volatile memory protects itself.

Restoration of ac power first provides the system with proper dc voltages. The DCLO power signal is deactivated with the KA11 processor generating an initializing signal, BUS INIT L (K13-2), and processor operation does not begin. After DCLO is deactivated, the ACLO signal is deactivated. The KA11 processor restarts if the ACLO signal is not reactivated within 70 milliseconds. This delay ensures adequate operating time to respond to an immediate power failure when the processor does restart (K15-2 GATED P RESTART L). The processor must be able to recover with a power fail up sequence and then process another power fail down sequence. These requirements are reflected in the signal, DELAY PWR DOWN (1) H (K15-2), on the waveforms of Figure 2-1 and the excess of seven milliseconds of proper voltage over the program limitation of two milliseconds.

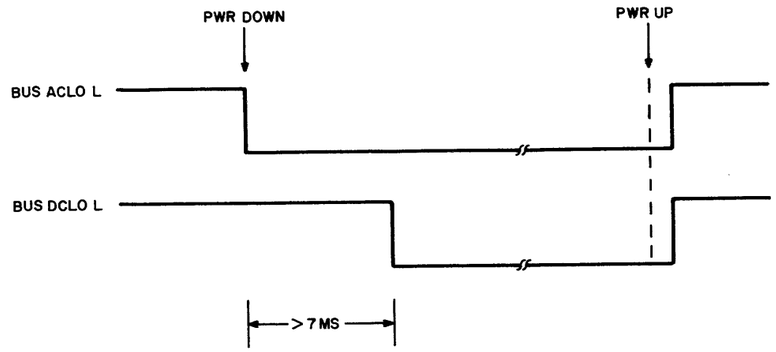

Figure 2-1 Sequence of Bus Power Signals

2.7.2 Power Fail Down

The power fail down sequence provides a trap sequence to the vector address 000024 after the current instruction or trap sequence. Two milliseconds of program operation allow storage of volatile information and conditioning of peripheral equipment for power down. Within this time, a program flag must be set in the subroutine to indicate that the next trap reference is for power up. A HALT instruction is necessary to properly terminate processor operation.

The power fail down sequence is initiated by the removal of input power and activation of the BUS ACLO signal, as indicated in the console flow diagram. The processor completes any power fail sequence that is begun and generates the necessary signals. Such a signal is the processor BUS ACLO signal that is activated by any BUS ACLO and prevents restarts for 15 milliseconds. The processor also produces a BUS DC LO signal for proper sequences. This signal completes the power down sequence and initiates the power up sequence if the power supply does not.

If the console ENABLE/HALT switch is in the HALT mode, the flow takes the right most branch after BUS ACLO. The trap sequence to vector address 000024 does not occur, and machine control is transferred to the console. After seven milliseconds, BUS DCLO and K13-2 INIT signals occur and all console and processor activity is terminated. The HALT mode also precludes completion of the power fail up sequence, with system control remaining with the console.

If the console ENABLE/HALT switch is in the ENABLE mode during the power fail down sequence, the flow continues through K15-2 ACLOF (1). This asynchronously set flag is synchronously transferred to the K15-2 PDNF (1) flag by the processor clock. This produces the K3-3 PWRF and K12-3 TRAPS signals which provide the trap sequence to vector address 000024. Two milliseconds of program operation are allowed with a required terminating HALT instruction. After seven milliseconds, the BUS DCLO and K13-2 INIT signals occur.

2.7.3 Power Fail Up

The power fail up sequence provides a modified trap sequence to vector address 000024. The DATO's within the trap sequence are eliminated since the address base from the volatile processor is incorrect; this is noted on the KA11 instruction flow diagram. The trap sequence occurs after sufficient restart delays to ensure power restoration and guarantees two milliseconds of program operation during the power fail up sequence before any power fail down sequence can begin.

The power fail up sequence begins with the deactivation of BUS DCLO. The K13-2 INIT signal occurs and the PUPF (1) flag is set if the ENABLE/HALT switch is in the ENABLE position. This results in the generation of the K13-3 PWR F and K12-3 TRAPS signals which provide for the power up trap sequence. The deactivation of BUS ACLO occurs a minimum of 15 milliseconds after its activation and begins the restarting of the processor. An integrating one-shot precludes the actual restart until BUS ACLO has remained deactivated for 70 milliseconds. Then a sequence of signals occur beginning with the K13-2 GATED P RESTART signal. The processor is restarted and the modified trap sequence to location 000024 results. A delay is set by K13-2 GATED P RESTART signal that precludes any power fail down sequence by inhibiting the setting of the K15-2 ACLOF (1) flag for five milliseconds. If a power interruption does occur during this period, the flag is set and serviced immediately after the five-millisecond delay.

If the ENABLE/HALT switch is in the HALT position, control is transferred to the console by the K13-2 INIT signal (on the deactivation of BUS DCLO) and the restart signal, K13-2 GATED P RESTART, is inhibited.

C

K1-2 CLK RUN (Ø)
K1-2 CLK OFF (1)
K13-4 CONSF (1)
BUS BBSY

LOAD ADRS

K13-2 GATE BUS ← SR
K13-4 EXAM F (Ø)
K13-4 DEPF (Ø)

CSR 1

K6-2 P CLR LATCHES — DATA WAIT (1)
K6-5 CARRY ØØ(Ø) — P CLR LATCHES
K6-4 GATE B ← B D15/Ø — DATA WAIT (1)
K6-2 P SET DATA WAIT

CSR 3

K13-3 CLK BAR
K4-2 RA/TEMP
K4-3 W/ENABLE 15/Ø

CSR 2

K6-5 CARRY ØØ(Ø)
K6-2 CLR LATCH A
K6-2 CLR LATCH B

CSR Ø

C

EXAM * DEP

K13-2 TIME DATA (Ø)
K13-2 TIME OUT (Ø)
K13-4 EXAMF (1) — EXAM
K13-4 DEPF (Ø)
K13-4 EXAMF (Ø)
K13-4 DEPF (1) — DEP
K13-4 INCF — [EXAMF (1) * EXAM] + [DEPF (1) * DEP]
K2-3 PARTIAL BSR ← I — REG ADRS * CLK OFF (1)

CSR 1

K4-2 RA/TEMP
K6-4 GATE B ← R15/Ø
K6-4 GATE B ← R7/Ø
K6-5 CARRY ØØ ← I — INCF
K6-3 GATE A ← RØ
K6-3 GATE A ← -RØ — INCF * -(REG ADRS)

CSR 3

K13-4 CLK BAR
K4-2 RA/TEMP
K4-3 W/ENABLE 15/Ø

CSR 2

K6-5 CARRY ØØ(Ø)
K6-2 CLR LATCH A
K6-2 CLR LATCH B
K13-2 GATE BUS ← SR
K6-2 P SET DATA WAIT — DEP
K6-2 P CLR LATCHES
K6-4 GATE B ← BD15/Ø — DATA WAIT (1)
K6-4 GATE B ← R15/Ø
K6-4 GATE B ← R7/Ø — EXAM * REG ADRS

CSR Ø

DEP * ST ADRS
K10-4 GATE ST ← D

EXAM * REG ADRS

DEP * REG ADRS
K4-3 GATE RA ← BAR
K4-3 W/ENABLE 15/Ø

-(REG ADRS)
K1-2 P CLK RESTART
K1-2 BSR1
K13-2 DATI ← I — EXAM * BSR1
K13-2 DATO ENTRY — DEP * CLK OFF (Ø)

EXAM
DATI
R/W2 * BSR7
LATCH B ← DATA BAR AND ADRS UNCHANGED

DEP
DATO
R/W2 * BSR8
BUS DATA ← SR BAR AND ADRS UNCHANGED

C

CONT

K13-4 CONSF (Ø)
K13-4 -(BUS BBSY) — CONSF (Ø) = -(BUS BBSY)
K2-3 D PERIF RELEASE — D PERIF RELEASE
K1-2 CLK RUN (1) — PERIF RELEASE
K12-3 BBSYF (1)

EXIT

HALT

K13-4 CONS NPR — S/CYCLE
K13-4 CONS BR — S/INSTR
K3-2 CNPRF (1) — CONS NPR * CLK BR
K3-2 CBRF (1) — CONS BR * CLK BR
K2-3 REQUEST — CBRF (1)
K12-3 CONS GRANT (1) — {SERVICE * ISRØ * [CBRF * -(TRAPS) + [HALTF (1)]} + {NPR ENTRY * CNPRF (1)}
K13-4 CONSF (1) — CONS GRANT (1)
K12-3 CONS GRANT (Ø) — CONSF (1)
K2-2 PROC RELEASE — {SERVICE * ISRØ * [HALT(1)] + [REQUEST * -(TRAPS)]} + {NPR ENTRY * CNPRF (1)}
K12-3 BBSYF (Ø) — CONSF (1)

C

REVISIONS	REV.	CHANGE NO.	CHK

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: KAII

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 | FRACTIONS ± 1/64 | ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

DRAWN	J.S. Nelson	DATE 7/14/70
CHKD.	[illegible]	DATE 7-27-70
ENG.	D.J. Brown	DATE 7-24-70
PROJ. ENG.	[illegible]	DATE 7-29-70
PROD.	[illegible]	DATE 7-31-70

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MAYNARD, MASSACHUSETTS

TITLE: KYII-A CONSOLE FLOW

SIZE D | CODE TD | NUMBER KYII-A-CF TD | REV.

SCALE NONE | SHEET 1 OF 2 | DIST.

DEC FORM NO. DRD 100

SIZE D | CODE TD | NUMBER KYII-A-CF TD | REV.

C

K1-2 CLK RUN (Ø)
K1-2 CLK OFF (1)
K13-4 CONSF (1)
K13-4 BUS BBSY

START

K13-4 STARTF (Ø)
K13-4 EXANF (Ø)
K13-4 DEPF (Ø)

INIT

K13-4 STARTF (1)

CSR 1

K6-4 GATE B ← R15/Ø
K6-4 GATE B ← R7/Ø
K4-2 RA/TEMP

CSR 3

K4-2 PA/PC
K4-3 W/ENABLE 15/Ø
K13-3 CLK BAR

CSR 2

K6-2 CLR LATCH A
K6-2 CLR LATCH B
K6-5 CARRY ØØ (Ø)

CSRB

K1-3 BSR ← 1 — FETCH ← 1

K13-4 STARTF (Ø)

ENABLE

K13-4 CONSF (Ø) — CONSF (Ø)
K13-4 -(BUS BBSY) — -(BUS BBSY)
K2-3 D PERIF RELEASE — D PERIF RELEASE
K1-2 CLK RUN (1) — D PERIF RELEASE
K12-3 BBSYF (1) — PERIF RELEASE

K1-4 FETCH ← 1 — FETCH ← SVC

F

HALT

C

PWR FAIL UP

-(BUS DC LO)

5MS PWR UP

K13-2 INIT
K3-3 PWRF — PUPF (1)
K12-3 TRAPS — PWRF

-(BUS AC LO)

HALT

ENABLE

70 MS RESTART

K13-2 GATED P RESTART
K13-4 CONSF (Ø) — GATED P RESTART
K13-4 -(BUS BBSY) — CONSF (Ø)
K2-3 D PERIF RELEASE — -(BUS BBSY)
K1-2 CLK RUN (1) — D PERIF RELEASE
K12-3 BBSYF (1) — PERIF RELEASE

SVC

TRAP TO PWRF VECTOR

PWR FAIL DOWN

BUS AC LO

PWR UP NOT POSSIBLE UNTIL DELAY TERMINATION

15 MS

PWR DOWN NOT POSSIBLE UNTIL DELAY TERMINATION

5MS

TRAP TO PWRF VECTOR, 2 MS OPERATION THEN HALT INSTR.

C

K15-2 ACLOF (1)

K15-2 PDNF (1) — PDNF(1)
K3-3 PWRF — PWRF
K12-3 TRAPS
K15-2 ACLOF (Ø)

7 MS

BUS DC LO
K13-2 INIT

C

CONSOLE WAVEFORMS

400 NS ± 200 NS

K13-4 TP2
K13-4 CSR Ø (1) H
K13-4 CSR 1 (1) H
K13-4 CSR Ø H
K13-4 CSR 1 H
K13-4 CSR 3 H
K13-4 CSR 2 H
K13-4 P1 CSR L
K13-4 P2 CSR L
K13-4 P3 CSR L
K13-4 P1 CSR Ø H

POWER FAIL WAVEFORMS

INPUT POWER
BUS AC LO (POWER SUPPLY)
BUS DC LO (POWER SUPPLY) — 7MS
BUS AC LO (K15-2) — 15MS
BUS DC LO (K15-2) — 7MS — 3MS
DELAY PWR DOWN(1)H(K15-2)
ACLOF (1) H (K15-2)
BUS INIT L (K13-2)
K15-2 GATED P RESTART L — 78 MS

NOTE: BUS SIGNALS ARE THE "OR" OF THE INDIVIDUAL SIGNALS SEPARATED ACCORDING TO SIGNAL SOURCE, NOTED IN PARENTHESES.

REVISIONS	REV.	CHANGE NO.	CHK

DEC FORM NO DRD 100

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PARTS LIST

FIRST USED ON OPTION/MODEL: KAII

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FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRWN		DATE 7/14/70
CHK'D		DATE 7-27-70
ENG		DATE 7-28-70
PROJ. ENG.		DATE 7-29-70
PROG		DATE 7-27-70

NEXT HIGHER ASSY

SCALE NONE

SHEET 2 OF 2

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TITLE: KYII-A CONSOLE FLOW

SIZE D | CODE TD | NUMBER KYII-A-CF TD | REV.

DIST.

CHAPTER 3
MODULE DESCRIPTION

The KY11-A console provides the KA11 Processor with its display and manual interface capability. Various data and control signals of the processor are displayed to indicate to the user various processor operational states. Data and control switches provide level conversion and filtering so that operator-initiated manual inputs can be provided to processor control logic. This chapter describes the console control logic. A description of the operation of the controls and indicators is contained in the *PDP 11/20 System Manual.*

NOTE

The following paragraphs refer to specific engineering drawings which are contained in the second volume entitled *KY11-A Programmer's Console, Engineering Drawings.*

The information on each of the following pages relates to only one specific print. The print number is in the upper corner or the page. For example, if a page has KY-3 in the upper corner, then all material on that page refers to print KY-3.

3.1 LAMP-DRIVER LOGIC

Lamp driver logic is shown on Drawing KY-2. All circuits of each of the 42 lamp driver circuits shown on this diagram are identical. Input signals are derived from processor output circuits. These signals are applied to non-inverting buffers that provide a high input impedance to the source signal. These buffers operate discrete lamp-driver transistors. Each drive transistor is shunted by a resistor connected across its collector-emitter junction. This resistor provides a low-current path through the indicator lamp; the current is not sufficient to turn the lamp on. Its purpose is to reduce turn-on transients when its drive transistor is switched into saturation.

3.2 SWITCH LOGIC

Inputs to the console ADDRESS REGISTER display drivers are derived from the bus address register (BAR) outputs; inputs to the DATA display drivers are derived from the bottom of the DATA PATHS and reflect the A and B input latch contents; inputs to the control displays represent various machine states.

Data and control signals originate from the console switches (Drawing KY-3). A relatively large negative voltage is used across the switch contacts to ensure adequate cleansing currents; diode clamps to ground limit low logic levels; pull-up resistors to +5 volts provide high logic levels.

The data input from the Switch Register is enabled by processor signal K15-2 GATE BUS ← SR H which is applied to the Unibus through bus drivers (BUS D ⟨15:00⟩ L).

Control switches within the processor (Bus and Console Control module, M724) drive input set-reset flip-flops to filter out contact bounce. Control signals which initiate machine operation require a single-switch transition; the set-reset flip-flops are set when a switch is activated; they are reset only if the switch is deactivated.

Additional filtering is provided for the EXAM, DEP and CONT switches by capacitors C36, C35 and C34, respectively. Control switches can be disabled by the panel lock switch. This switch removes negative switching voltage (K14-2 PNLK H) from the contact switches; an RC filter (R154, C33) eliminates switch noise.

Signal **KY-3 START L** is a filtered signal activated by the START switch; the release of the START switch clocks the STARTF flip-flop to one (K13-4 STARTF (1) H). Signal KY-3 START H is a test point.

Signal **KY-3 INIT L** is activated prior to a start operation when the START switch is depressed. Thus the signal initializes the PDP 11/20 system through the BUS INIT L and K13-2 INIT L signals.

Signal **KY-3 EXAM L** is a test point

Signal **KY-3 EXAM H** is a filtered signal activated by the EXAM switch; this signal is further gated to produce the K13-4 EXAM L signal.

Signal **KY-3 DEP L** is a test point.

Signal **KY-3 DEP H** is a filtered signal activated by the DEP switch; this signal is further gated to produce the K13-4 DEP L signal.

Signal **KY-3 HALT L** is a filtered signal activated by the ENABLE/HALT switch in the HALT position. This signal is used directly to inhibit power fail signal (K3-3 PWR F H), the setting of the RESTART one-shot signal (K13-2 TP 1 L), and the reset (loading of zeros) of the CONSF flip-flop (K13-4 CONSF (1) H). Depending on the position of the S-INSTR/S-CYCLE switch, the K13-4 CONSF (1) H signal enables K13-4 CONS BR H or K13-4 CONS NPR H for transfer of control to the console.

Signal **KY-3 HALT H** is a filtered signal activated by the ENABLE/HALT switch when in the HALT position. This signal is used to directly inhibit a restart after power fail (K15-2 GATED P RESTART L).

Signal **KY-3 LOAD ADRS L** is a filtered signal activated by the LOAD ADDR switch and used to clear the EXAMF and DEPF flip-flop of BUS & CONSOLE CNTL.

Signal **KY-3 LOAD ADRS H** is a filtered signal activated by the LOAD ADDR switch; it is further gated to produce the K13-4 LOAD ADRS L signal.

Signal **KY-3 CONT H** is a test point.

Signal **KY-3 CONT L** is a filtered signal activated by the CONT switch; it is used to reset (load to zero) the CONSF (K13-4 CONSF (1) H) which relinquishes console control.

Signal **KY-3 S/CYCLE L** is an unfiltered signal which reflects the S/CYCLE position of the S-INST/S-CYCLE switch. This signal is enabled by the HALT position of the ENAB/HLT switch and activates K13-4 CONS NPR H. Signal KY-3 S/INST L is an unfiltered signal which reflects the S/INST position of the S-INST/S-CYCLE switch. This signal is also enabled by the HALT position of the ENAB/HLT switch which activates K13-4 CONS BR H.

NOTE

Signals KY-3 SR17 L, KY-3 SR17 H, KY-3 SR16 L, and KY-3 SR16 H provide test points for the most significant two bits of the Switch Register.

Signal **BUS D ⟨15:00⟩ L** provides the Unibus interface with bits ⟨15:00⟩ of the Switch Register. Data from the Switch Register is transferred to the processor along the Unibus when the processor control signal K13-2 GATE BUS ← SR H is activated.

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