Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-10
Maintenance Manual

DC10
DATA LINE SCANNER

DEC-10-HDCAA-B-D

DC10
DATA LINE SCANNER MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual contains introductory material, installation and operating information, theory of operation, and maintenance information for the Type DC10 Data Line Scanner. Since this manual is intended to aid maintenance personnel, the equipment is discussed primarily from a maintenance point of view. A general description and physical description is included in the introductory section to provide a brief overall understanding of a data line scanner system. A working knowledge of the central processor and peripheral devices is assumed; but, to aid maintenance personnel in locating reference material, a list of pertinent documents is included in the introductory material. In the installation and operating information, general operating instructions are provided, along with option adjustments that are required by the customer during installation. The theory of operation is divided into three levels of coverage: first, a simplified system block diagram is used to identify the major system components and to describe the basic system operation; next, each of the major components are explained at the block diagram level, last, the circuits on the block schematics are related to the associated blocks on the block diagrams. In the maintenance section, troubleshooting information and adjustment procedures are provided to aid the maintenance personnel in locating and repairing system malfunctions.

1.2 GENERAL DESCRIPTION

The Type DC10 Data Line Scanner provides a timesharing two-way interface between the PDP-10 central processor and a maximum of 64 teletype-like stations. Any device which uses a 5-level or 8-level serial teletype code can be accommodated at signaling speeds of up to 100 kilobaud. Full-duplex, full-duplex with local copy, and half-duplex data line modes are available on each line serviced. Send-only or receive-only stations are also accommodated. Information is transferred between a device and the central processor on a time-sharing basis and under program control. The data lines to the devices are serviced either on demand or under program control, but servicing of the data lines is controlled by the central processor on a priority interrupt basis. Command signals are routed to the data line scanner via the input/output (I/O) bus and are used to control the I/O instructions. During a CONI or DATAI instruction, data is routed to the central processor from a device via the I/O bus. When a CONO or DATAO instruction is performed, data is routed from the central processor to a device via the I/O bus.

1.3 REFERENCE MATERIAL

The following DEC documents contain material which supplements information in this manual. These documents may be obtained from the nearest DEC office or from

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

1.3.1 Manuals

Digital Logic Handbook (C-105)	Specifications and descriptions of FLIP CHIP modules, plus simplified explanation of the selection and use of these modules in numerous applications.
PDP-10 Interface Manual DEC-10-HIFB-D	Implementation guidelines and requirements for the PDP-10 I/O Bus, memory bus, and data channel bus.
PDP-10 System Reference Manual DEC-10-HGAC-D	Programming and operating information for the computer, including programming information on the Type DC10 Data Line Scanner.

1.3.2 Maintenance Program

DC10 Data Line Scanner Test MAINDEC-10-D2CC-D

1.4 PHYSICAL DESCRIPTION

The DC10 Data Line Scanner is designed to fulfill a wide variety of system requirements. System components are purchased as options, thus the hardware configuration of a system depends upon the customer's requirements. The major components of a data line scanner system are identified in Figure 1-1. Table 1-1 lists the physical characteristics and provides a brief functional description for each of the DEC designed and manufactured options.

1.4.1 Physical Details

System components are purchased as options and are mounted in standard DEC 19-in. cabinets which are constructed with welded frames and metal sheet covering. Access doors are mounted on the front and rear of the cabinet and are held closed by magnetic latches. The power control, eight standard 25-pair connecting blocks, and the dc power supplies are mounted inside the rear door on a full-width plenum door that is latched by a spring-loaded pin at the top. Module mounting panels are mounted behind the front door with the wiring side facing outward. Blower assemblies mounted between the module mounting panels pass cooling air over the modules; the air is exhausted through an opening at the top of the cabinet.

In each system, the DC10A Control Unit is required. The cabinet supplied with this option contains the control unit, indicator panel, integrated circuit power supply, two blower assemblies, and 21 in. of panel mounting space. When additional panel mounting space is required for a larger system, the cabinet of the DC10F Expander Cabinet option is bolted to the control unit cabinet to form a contiguous unit. The expanded cabinet is similar to the first cabinet except an additional control unit is not required or supplied. Because of this, the cabinet addition provides 42 in. of panel mounting space.

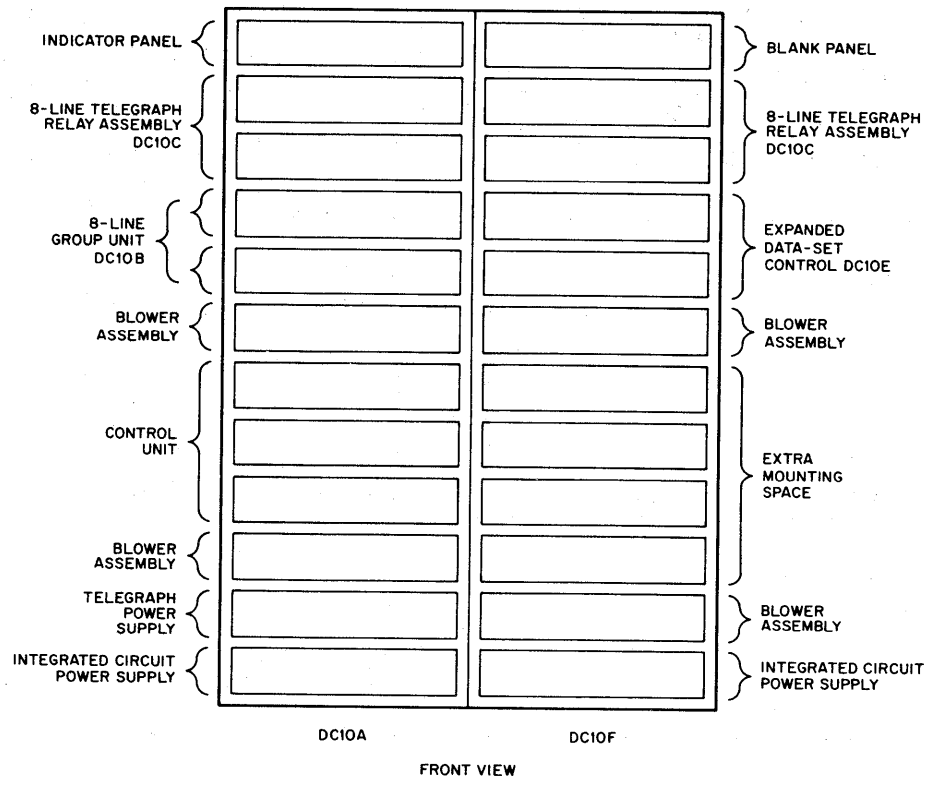


Figure 1-1 Data Line Scanner Components

Table 1-1
Physical Characteristics of the Data Line Scanner Options

Option	Function	Contains	Weight	Physical Requirements	Power[1] Requirements
DC10A Control Unit	Provides the necessary interface between the central processor and up to eight line groups.	a. One Control unit b. One cabinet with power supplies c. One set of I/O bus cables d. Four line group connecting blocks e. Four external cable blocks f. 21 in. of panel mounting space	500 lb.[1]	Requires 3 ft. in both front and rear for access and maintenance.	1500W.
DC10B 8-Line Group Unit	Provides the necessary interface between the control unit and eight teletype-like devices.	a. One 8-line group b. One set of cables to the control unit.	See DC10A	Requires 5-1/4 in. of panel mounting space and one equipment connecting block	See DC10A
DC10C 8-Line Telegraph Relay Assembly	Provides relay buffering for full or half duplex circuits.	a. One telegraph relay assembly b. One relay bias panel	See DC10A	Requires 10-1/2 in. of panel mounting space and two equipment connecting blocks	See DC10A
DC10D Telegraph Power Supply	Provides the necessary power to operate the telegraph lines associated with approximately four telegraph relay assemblies.	a. One 125 Vdc, 2A power supply	See DC10A	5-1/4 in. of panel mounting space allotted in DC10A cabinet	See DC10A
DC10E Expanded Data-Set Control	Provides status and operational controls for eight standard data sets, two with automatic calling provisions.	a. Eight expanded data set controls b. Two automatic call- c. One set of cables to the control unit	See DC10A	Requires 10-1/2 in. of panel mounting space and one equipment connecting block	See DC10A
DC10F Expander Cabinet	Provides additional panel mounting space for large data line scanner systems.	a. One cabinet with power supplies b. Four line group connecting blocks c. Four external cable connecting blocks d. 42 in. of panel mounting space	500 lb.[1]	Requires 3 ft. in both front and rear for access and maintenance	1500W

[1]Typical

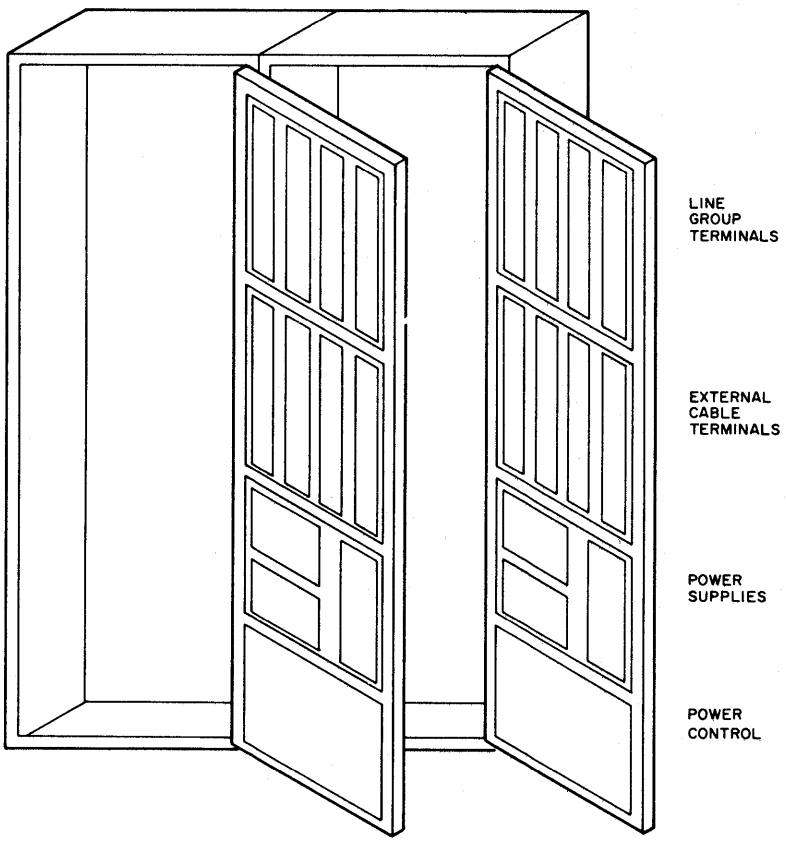


Figure 1-1 Data Line Scanner Components (cont)

CHAPTER 2
OPERATING INFORMATION AND INSTALLATION

2.1 INTRODUCTION

This chapter provides operating and installation information to aid data line scanner maintenance personnel. The contents of this chapter are organized in this manner: first, the control and indicators are identified and their functions are briefly explained; next, general operating instruction and programming notes provide an overall understanding of the data line scanner; then, detailed procedures for setting up various per-line options during installation are provided. To fully understand these procedures, maintenance personnel should read the theory of operation contained in Chapter 3.

2.2 CONTROLS AND INDICATORS

The controls and indicators associated with the data line scanner are identified in Figures 2-1 and 2-2. A thorough understanding of the controls and indicators on the maintenance and indicator panel, Figure 2-1, is a valuable aid to system personnel not only during maintenance mode but also during normal operation. Table 2-1 describes the function of each control or indicator on the panel. The power control panel shown in Figure 2-2 controls the application of the data-line scanner input power. From the power control panel, input power is turned on, the data line scanner power supplies are controlled, and either the local or remote power mode is selected (Table 2-2).

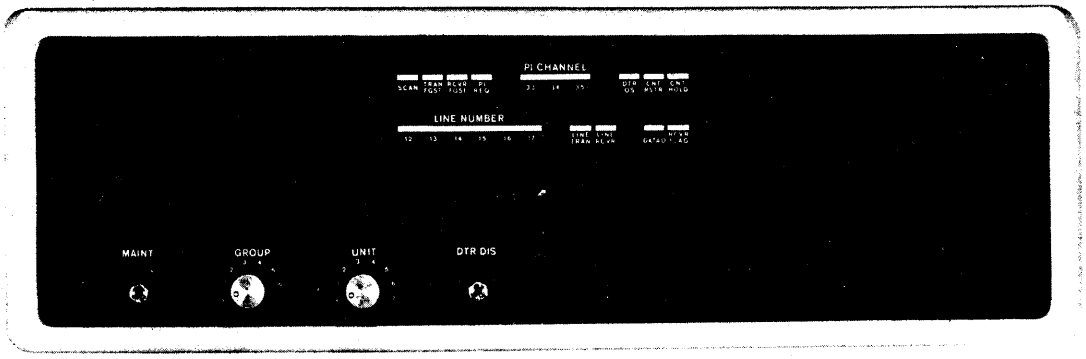


Figure 2-1 Indicator Panel

Table 2-1

Indicator Panel Functions

Number	Nomenclature	Item	Function
1	SCAN	Indicator	Indicates that the group selected by the group register has a flag on.
2	TRAN FG ST	Indicator	Indicates when the transmitter flag of the data line selected by the group and units registers is on.
3	RCVR FG ST	Indicator	Indicates when the receiver flag of the data line selected by the group and units registers is on.
4	PI REQ	Indicator	Indicates when the program interrupt flip-flop is set.
5	PI CHANNEL	3 Indicators	Indicates the octal program-interrupt channel number.
6	DTR OS	Indicator	Indicates when the data term ready one-shot is set.
7	CNT RSTR	Indicator	Indicates when the count restart flip-flop is set.
8	CNT HOLD	Indicator	Indicates when the count hold flip-flop is set.
9	RCVR FLAG	Indicator	Indicates when the receiver flag flip-flop is set.
10	DATAO	Indicator	Indicates when the DATAO flip-flop is set.
11	LINE RCVR	Indicator	Indicates when the receiver flag of the data line selected by the line number switches is on.
12	LINE TRAN	Indicator	Indicates when the transmitter flag of the data line selected by the line number switches is on.
13	LINE NUMBER	6 Indicators	Indicates the data line number selected by the scanner in octal form.
14	DTR DIS	Toggle Switch	When up, holds the data term ready one-shot in the one state.
15	UNIT	8 Position Rotary Switch	Selects a data line within the selected group.
16	GROUP	8 Position Rotary Switch	Selects the desired group number.
17	MAINT	Toggle Switch	When up, selects the maintenance mode.

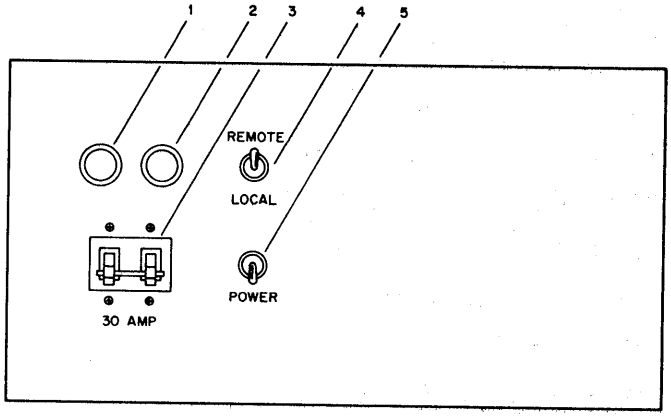


Figure 2-2 Power Control Panel

Table 2-2
Power Control Functions

Number	Nomenclature	Item	Function
1		Indicator - White	Illuminated when 115 Vac or 230 Vac line power is applied.
2		Indicator - Red	Illuminated when the line power is polarized wrong and when 230 Vac power is applied.
3	30 AMP	Circuit Breaker	Controls line power to the convenience outlets and the DC10D option and protects input line.
4	REMOTE/ LOCAL	Toggle Switch	Selects the local mode or the remote mode.
5	POWER	Toggle Switch	Controls line power to the power supplies and the data line scanner system.

2.3 OPERATING NOTES

In this section, operating notes are supplied to provide both operational and maintenance personnel with an understanding of the data line scanner operation. The information in this section is divided in the following manner: power application procedures during normal and maintenance operations are detailed; device selection for the data line scanner is discussed; and a brief description of the functions performed during the various I/O is provided.

2.3.1 Power Application

The application of power is controlled at the central processor's margin control panel when the following switches on the data line scanner power control(s) are placed in the following positions:

a. The LOCAL/REMOTE switch in the REMOTE position.

b. The POWER switch in the up position.

c. The circuit breaker in the up position.

This is the normal placement of the switches.

To control the application of power at the data-line scanner power control during maintenance operation, the LOCAL/REMOTE switch is placed in the LOCAL position and the circuit breaker is left in the up position. Then, the POWER switch may be used to control the application of power, as desired.

2.3.2 Device Selection

The data line scanner is selected by the central processor under program control. Seven complementary pairs of signals representing IOS 3 through IOS 9 of the I/O bus are routed to the device selection option card in the DC10A. At the device selection option card, jumpers are normally inserted to provide a device number of 0101000 (240_8). When this device number is routed to the option card via the I/O bus, the data line scanner is selected. Device number 240_8 is the standard device number for the data line scanner, but of course, it is possible to place the jumpers on the device option card so the data line scanner will respond to any device number. For additional information on device selection, refer to Section 2.5, Installation.

2.3.3 I/O Instruction

The data line scanner is designed to respond to the standard I/O instructions under program control. In the following table, each I/O instruction is identified and a brief summary of its functions is provided. The actual function of each instruction is dependent upon programming. Refer to Section 2.4, Programming Notes, for a general reference to data-line scanner programming.

Instruction	Functions
CONO (Conditions Out)	A transfer of data from the central processor to the data line scanner may perform one or more of the following: 1. Clear the data line scanner 2. Set the data terminal ready one-shot 3. Reset the scanner counters 4. Load the PI channel number into the PI storage register.

Instruction	Functions
CONI (Conditions In)	Transfer of conditions from the data line scanner to the central processor indicates the following: 1. The position of the data terminal ready disable (DTR DIS) switch. 2. The presence of a transmitter interrupt 3. The presence of a receiver interrupt 4. The data-line scanner PI channel number
DATAO (Data Out)	A transfer of data from the central processor to the data line scanner may perform one or more of the following: 1. Select a data line number 2. Transmit data to an idle data line 3. Transmit data to an interrupting data line 4. Clear a transmitter flag without sending data 5. Cause a program interrupt 6. Cause the off-hook enable flip-flop to change states 7. Cause a data-set to request a dial tone 8. Indicate the presence of a digit 9. Identify the digit to be dialed
DATAI (Data In)	A transfer of data from the data line scanner to the central processor will transfer the following: 1. The interrupting data line number 2. The presence of active data 3. A 5-bit or 8-bit character transfer or data line status word

2.4 PROGRAMMING NOTES[1]

2.4.1 Introduction

The DC10 Data Line Scanner interfaces up to 64 teletypewriter-like stations to the PDP-6 or PDP-10 computer. The DC10 Data Line Scanner accommodates any device which uses 5-level or

[1] Programming notes are effective as of September 22, 1967.

8-level, serial start-stop codes at speeds up to 100 kilobaud. Full-duplex, full-duplex with local copy (the usual switched network configuration), and half-duplex data line modes are available on each line serviced. Send-only and receive-only (simplex mode) stations are also accommodated. Each data line serviced can be connected for any of three signalling speeds.

The DC10 Data Line Scanner is constructed "building-block" style out of modularly functional units. Figure 2-3 shows the block diagram of a typical DC10 installation. The DC10A provides a 64-line scanner and the I/O bus interface for the data line scanner and also provides cabinet space and power supplies for the other units of the data line scanner.

The DC10B provides eight lines of serial-parallel conversion and data-line interfaces for both EIA standard RS-232-B[1] signaling and 20 mA full-duplex local loops. The EIA interface is provided for data-sets and Model 37 Teletype machines. The 20 mA local loops are provided for Model 28, 33, and 35 Teletype machines and other compatible equipment.

The DC10C Telegraph Relay Option provides interface conversion for long lines and/or electrically "dirty" environments; half-duplex capability is also provided by this option. The DC10D Telegraph Power Supply is a high voltage power supply used with one or more DC10C options. Both the DC10C and DC10D are invisible to the programmer except that the DC10C provides half-duplex capability for the DC10B.

Data-sets such as those used in the Dataphone, TWX, and Telex systems can be used directly with the DC10B with manual data-set control. The DC10E provides the computer with control over these data-sets. This option allows positive automatic control over the data-sets which is frequently useful in multi-user timesharing systems with switched network access. The DC10E provides control of eight data-sets and two associated automatic calling units.

The DC10F provides the additional cabinet space and power supplies required in expanded systems. It is invisible to the programmer.

The DC10 Data Line Scanner requires one I/O device number (standard: 240_8; mnemonic: DLS) and provides program interrupts on one PI channel. Although all data, status, and control are passed through the DC10A, the various aspects of programming are described in the various hardware-option oriented sections which follow.

2.4.2 DC10A Programming

The scanner in the DC10A continually monitors the eight possible 8-line groups (or expanded data-set controls) until it finds a group or control with a flag that is raised. The scanner then scans through the selected group or control, looking for the data line number (which may represent a data-set's

[1] "Interface between Data Processing Terminal Equipment and Data Communication Equipment"

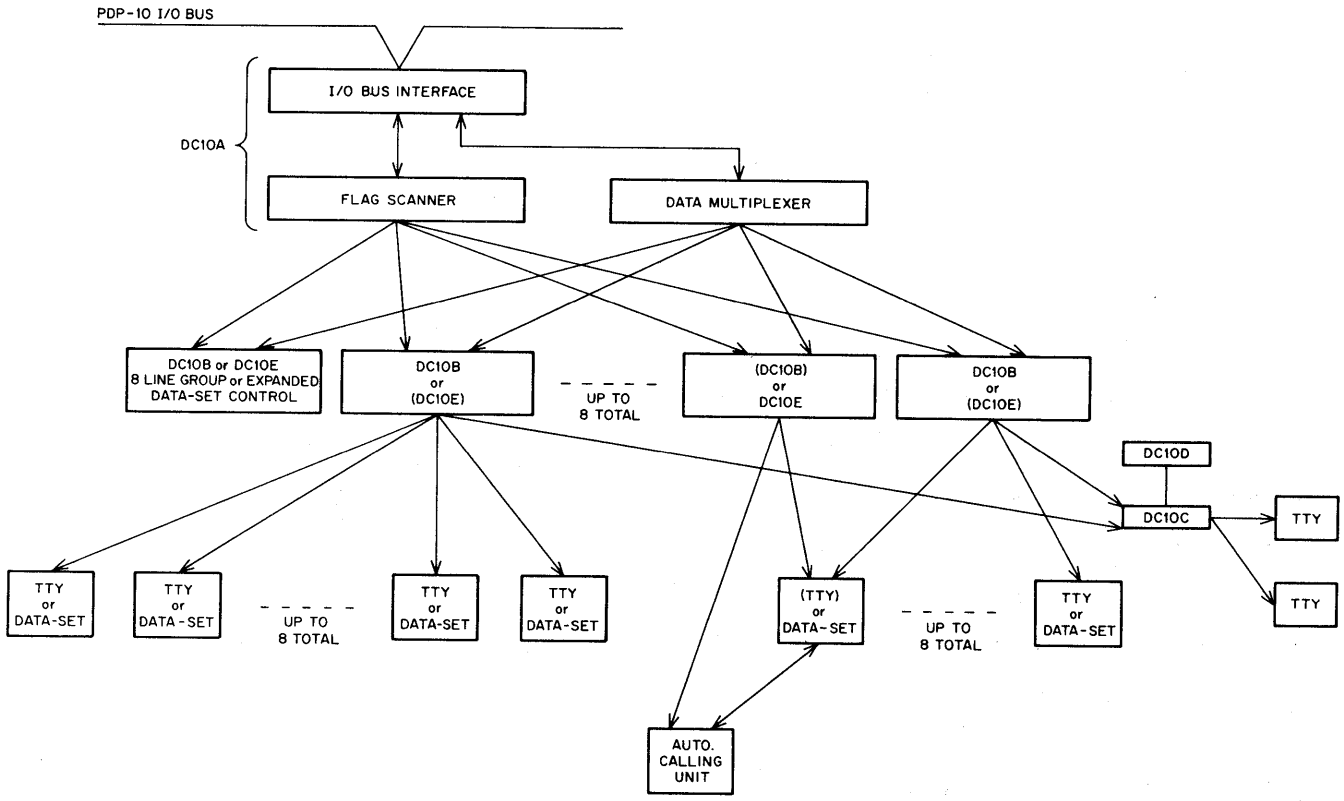


Figure 2-3 DC10 Block Diagram

status bits) which has its flag raised. When the scanner finds a line number requiring attention, it stops and causes a program interrupt on the PI channel assigned to the data line scanner. The maximum time required to find the next flag after having serviced a data line is approximately 20 μs.

The data line scanner control register is shown in Figure 2-4. A CONO to the data line scanner performs the following functions: bits 33 through 35 are loaded into the PI channel register and are used to determine what channel a PI will occur on; bit 32, when 1, resets the scanner to line number 00, thus providing higher priority for lower numbered lines than for higher numbered ones; bit 31, when 1, sets the data terminal ready one-shot used for data-set control. See Section 2.4.4 for details of data terminal ready operation. Bit 30, when a 1, clears the entire data line scanner system in exactly the same fashion as I/O reset does. It clears the PI channel register, clears the PI flip-flop and initializes all DC10B and DC10E registers, thus clearing all waiting or partially processed characters.

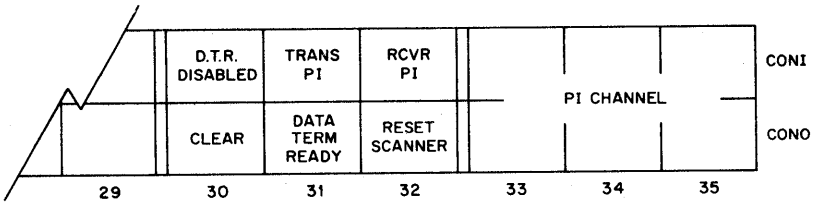


Figure 2-4 DC10A Control and Status

The data line scanner status bits are shown in Figure 2-4. Bits 33 through 35 indicate the setting of the PI channel register; bit 32 = 1, if the scanner is at a line which has its receiver flag raised; bit 31 = 1, if the scanner is at a line which has its transmitter flag raised; bit 30 = 1, if the disable data terminal ready switch is on.

The left-half (bits 11 through 17) of the DATAO and DATAI data contains line number information used in conjunction with the data in the right-half while programming the DC10B and DC10E. See succeeding sections for details.

2.4.3 DC10B Programming

Each DC10B provides serial to parallel and parallel to serial conversion for eight serial-data lines. Each line can be connected for one of the three data speeds provided in the DC10A. Each line may be connected for 5-bit or 8-bit asynchronous start-stop code and may be provided with 1 unit, 1-1/2 unit, or 2 unit stop codes and full- or half-duplex options. Each line uses a 20 mA local-loop interface or an EIA interface. The only options which affect programming are the 5-bit or 8-bit option and the half- or full-duplex option. The 8-bit full-duplex option will be treated in detail. The other cases will be treated as variations of this case. The DC10 is designed to minimize the number of central processor instructions required to service it. To achieve this, the data line number and the corresponding data are handled together in the left and right halves of the data words. Figure 2-5 details the bit configurations for DC10B operation. Several different operations are necessary in servicing teletypewriter lines, they are the following.

a. transmit a character on a presently idle line,

b. transmit a character on an active line (which is ready for its next character),

c. deactivate an active transmitter line (turn off its flag without sending another character),

d. read in a received character.

The heart of the DC10B is the teletype transmitter and teletype receiver modules provided with each line.

Data are loaded into the teletype transmitter module and, if the disable bit is not on, sent out in serial fashion as a proper teletypewriter code. When the transmitter has finished serializing

the data, it turns on its flag for the scanner to see. When the scanner reaches the transmitter's line number, it stops and causes a PI. When additional data is loaded into the transmitter module, its flag is turned off and it starts to send out the serial data. Loading the transmitter module with the disable bit on will clear the transmitter flag without sending out additional data.

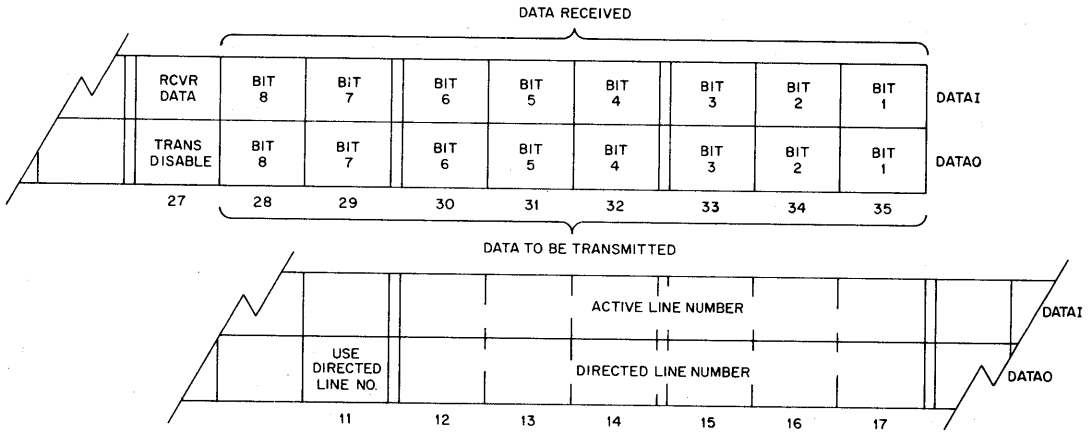


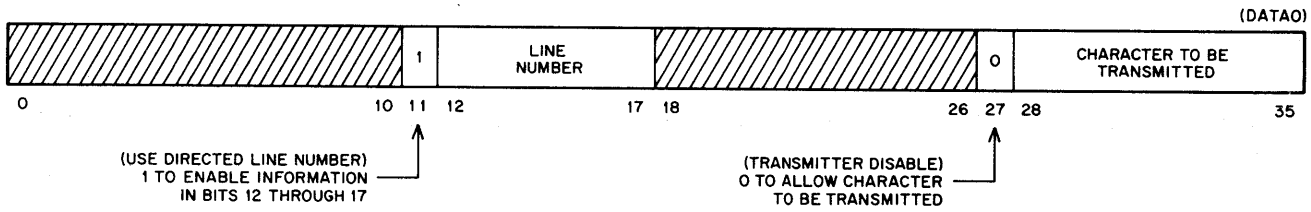
Figure 2-5 DC10B Data

The receiver module gathers serial data until it has received a full character, at that time it raises its flag for the scanner to see. When the scanner reaches the receiver's flag, it stops and causes a PI. Reading the data from the receiver module clears the receiver flag.

To transmit on an idle line, the instruction

DATAO DLS, CHARWD

may be executed, where CHARWD contains

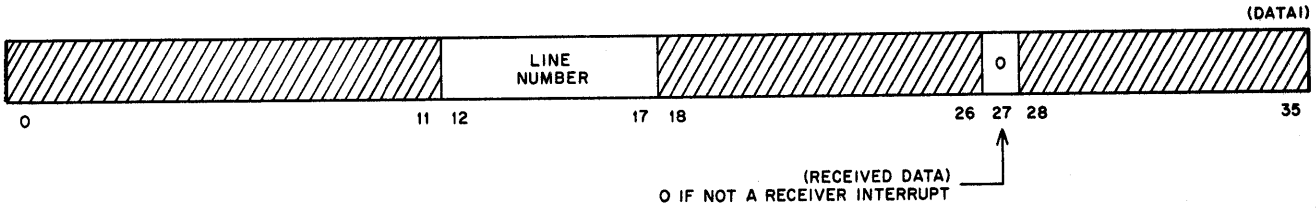


The 1 in bit 11 causes the line number in bits 12 through 17 to be used in place of the scanner register's line number for loading the transmitter module. The scanner is not loaded with bits 12 through 17, instead it continues scanning and resumes looking for lines requiring service after the instruction is finished If the line specified is not idle, the character transmitted will be garbled.

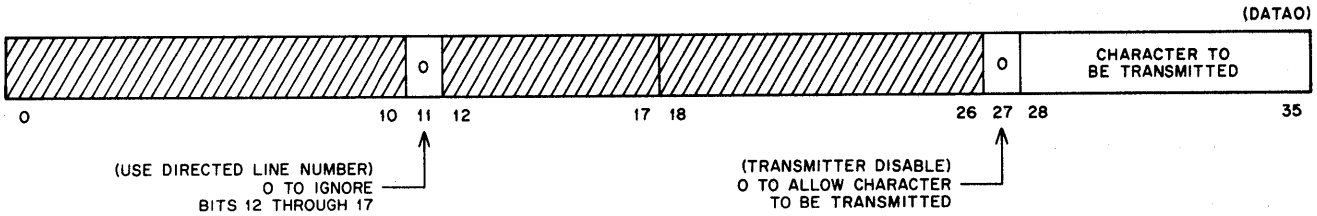
When the transmitter is finished sending a character to the data line (9.5 units after it started), it raises its flag. The scanner stops at the flag and sends a PI request to the central processor. To send another character, the PI may be serviced by

```
...                          ...
DATAI DLS, LINEWD            ;DATA INTO AC LINEWD
TRNE LINEWD, 400             ;IS THIS RECEIVED DATA
(Jump to Receiver Subroutine)  ;YES
(Look up next character)       ;NO, TRANSMITTER INTERRUPT
...
DATAO DLS, CHAR              ;LOAD NEXT CHARACTER INTO TRANSMITTER
...
(Dismiss interrupt)
```

LINEWD will contain



CHAR should contain



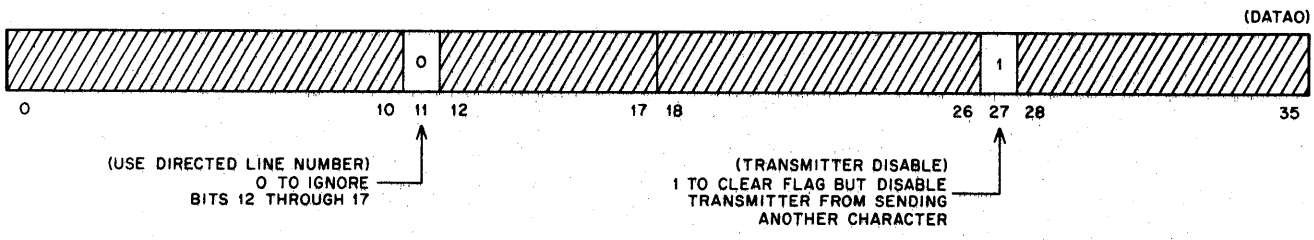
The DATAO will turn off the transmitter's flag (releasing the scanner) and allow the transmitter module to transmit the new character serially.

To maintain maximum speed on a line, the new character must be loaded within T_t where

$$T_t = \frac{\text{Number of stop units} - 1/2}{\text{line speed (baud) or units (bits) per second}} \text{ seconds}$$

NOTE: A CONI (or CONSO or CONSZ) servicing a PI request will indicate the state of the transmitter and receiver flag. After a PI request is made by the data line scanner, a receiver flag is not allowed to come up, if not already up, until after the PI request is serviced (or I/O reset occurs). This means that if only a transmitter is found with a CONI servicing a PI request, the right half-word data of the DATAI will be 0. If a receiver flag is found with a CONI servicing a PI request, the right half-word data of the DATAI will contain 1 in bit 27 and the character received in bits 28-35. If both a transmitter and receiver flag are on, the receiver flag takes precedence.

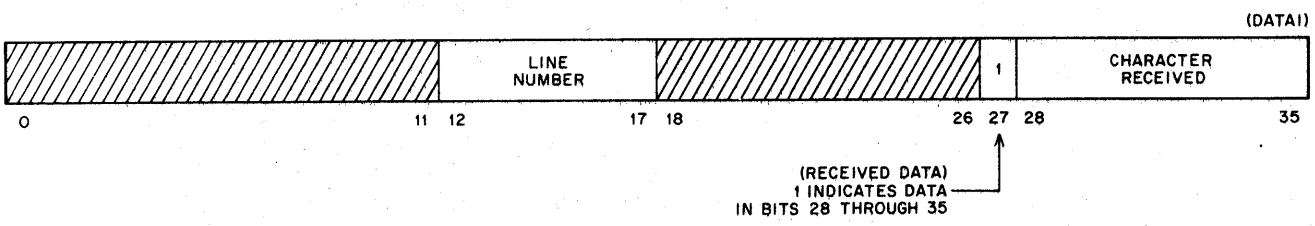
To turn off a transmitter flag, and thus release the scanner, without transmitting another character the DATAO DLS, CHAR should be replaced by DATAO DLS, NOCHAR where NOCHAR contains:



When a receiver module receives a complete character (in the middle of the eighth data bit), it raises its flag. The scanner stops at the flag and sends a PI request to the central processor. The received data is read into the central processor by

```
...
DATAI DLS, LINEWD          ;DATA INTO AC LINEWD
TRNE LINEWD, 400           ;IS THIS RECEIVED DATA
(Store Character)          ;YES
(Transmitter Subroutine)   ;NO, TRANSMITTER INTERRUPT
...
(Dismiss Interrupt)
```

LINEWD will contain



The receiver flag is turned off by this DATAI. To avoid garbling a character, receivers must be serviced within T_r, where

$$T_r = \frac{\text{Number of stop units} + 1/2}{\text{line speed (band or units (bits) per second)}} \text{ seconds}$$

If a data line scanner has many lines, or lines running at different speeds, each PI must be serviced within the T_r of the highest speed line to avoid "hanging" the scanner and losing data. Even though a PI is not serviced within T_r and the character is garbled, the DATAI must be done in order to clear the receiver module flag so that the end of the next character can be detected.

Operation of a line with 5-bit teletypewriter codes is identical to that with 8-bit codes except that bits 28 through 30 of DATAI and DATAO data words no longer carry information.

Operation of a line in full-duplex with local copy mode does not effect programming except that the transmitter module will not start transmitting a character until the associated receiver module is idle, in order to avoid garbled copy at the teleprinter. Hence, transmitter PIs may occur less frequently.

Operation of a line in the half-duplex mode is essentially identical to full-duplex operation. (The DC10C Telegraph Relay Option is required, of course.) However, any time a character is transmitted, it will subsequently be received by the receiver module associated with the same line. The received character should be checked by the program to see if it matches the transmitted character. If it does not, either a line error has occurred or the keyboard of the teletypewriter has been struck. This condition is often used to interrupt program output. A line's transmitter and receiver will both cause interrupts at the end of a character. The receiver PI request will occur one unit before the transmitter PI request. If a character is sent to the transmitter of a half-duplex line while its receiver is active, the transmitter will wait until the receiver has finished before starting to transmit. Thus a character may be loaded into the transmitter module at any time without garbling the character presently being received. (It may, however, garble the next character received.)

2.4.4 DC10E Programming

The DC10E Expanded Data-Set Control provides computer supervision of the control functions of the more common types of data-sets. A data set connected to a DC10E then has two line numbers assigned to it: the data line number to the DC10B and the control line number to the DC10E. Provision for two automatic calling units is included in each DC10E. The DC10E uses a control interface which conforms to EIA standard RS-232-B. Data-set status and control bits appear in the same bits of the I/O data words as characters from the DC10B. On the six lines (0 through 5) of the DC10E which are provided with data-set control only, the Clear to Send (CB[1]) and Restrain Detected (RD) signals are provided

[1] Two and three letter abbreviations (CD, RD, DLO etc.) are the signal lead names in the data set technical manuals.

to the data-set. On the two lines provided for control of automatic calling units, Data Line Occupied (DLO), Present Next Digit (PND), and Abandon Call and Retry (ACR) are provided from the automatic calling unit (ACU) in addition to CB and RD from the associated data-set. The signals Call Request (CRQ), Digit Presented (DPR) and NB8, NB4, NB2, and NB1 (binary-coded decimal digit to be dialed) are provided to the automatic calling unit in addition to CD which is provided to the data-set. Figure 2-6 details the bit configuration for the DC10E. As the data-set control information need not be retransmitted periodically, the data-set control never causes a transmitter interrupt. Similarly, the data-set status tends to remain constant for long periods of time. Therefore, only the more meaningful status bit transitions set the data-set status flag (receiver flag). The scanner stops at the data-set status flag and causes a PI request. In order to read out the status of a data-set whose flag is not set, a bit in the data-set control register causes the flag to be set artificially so that the scanner will stop the next time the line is scanned to allow the status to be read out.

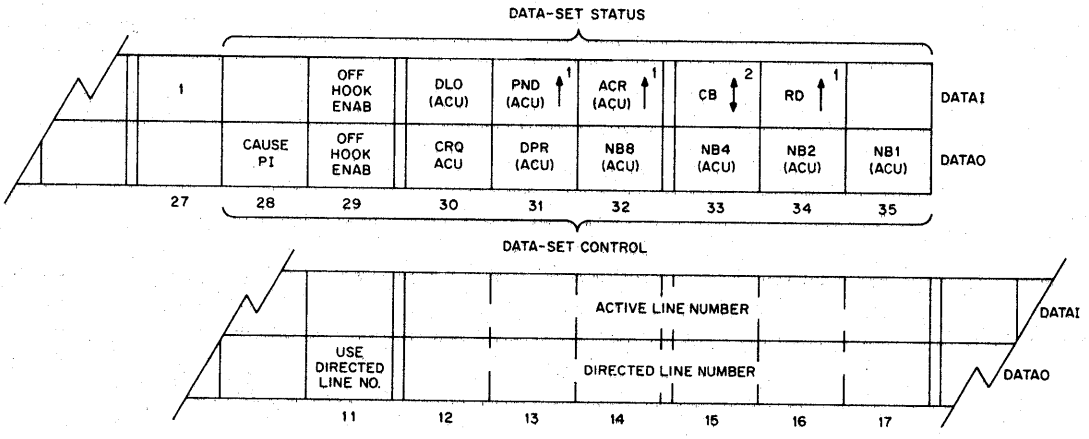


Figure 2-6 DC10E Data

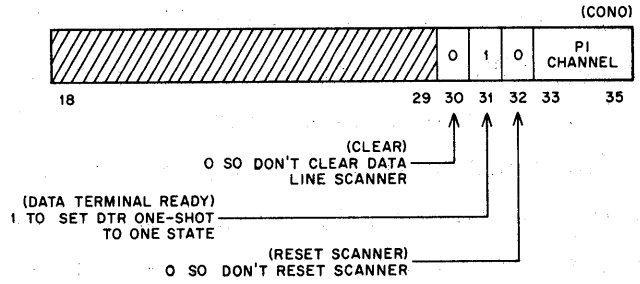
Data sets respond to their CD (data terminal ready) lead, as follows. Whenever the data-terminal ready signal is false, the data set is inactive; if the data terminal ready signal is true, the data-set answers an incoming call or allows an outgoing call to be completed. When data terminal ready goes from true to false, the data-set will break its connection and hang up. Data terminal ready control is provided in the DC10 in two stages. The DC10A contains an integrating one-shot which must

1 The "ON" transitions set the flag.
2 The "ON" and "OFF" transitions set the flag.

be kept in the 1 state by a CONO instruction every 500 ms. Use the instruction

```
CONO DLS, DTRWD          ;SET DATA TERM READY
```

where DTRWD is as follows:

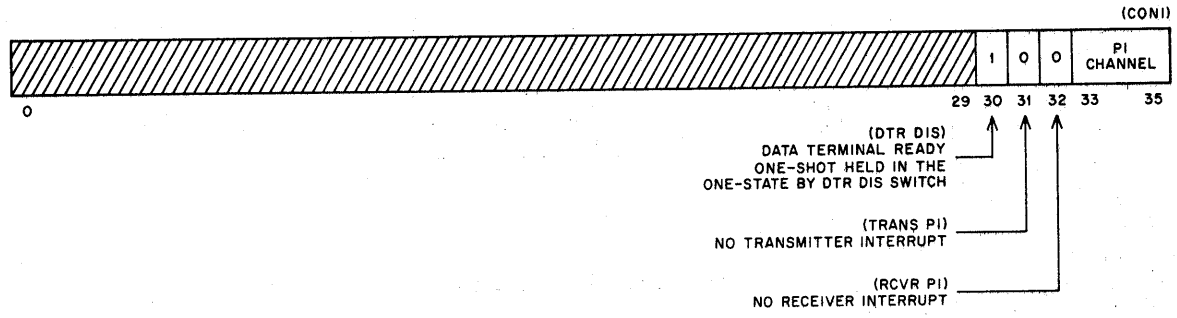


This feature may be eliminated for software debugging purposes by throwing the DTR DIS switch UP on the indicator panel of the DC10A. The DTR DIS switch holds the data terminal ready one-shot in the one state indefinitely and inhibits clearing of the off hook enable flip-flop by IOB RESET or by a CONO with bit 30 a 1.

The status of the DTR DIS switch can be determined with a CONI:

```
CONI DLS, CONIWD
```

where CONIWD will be:

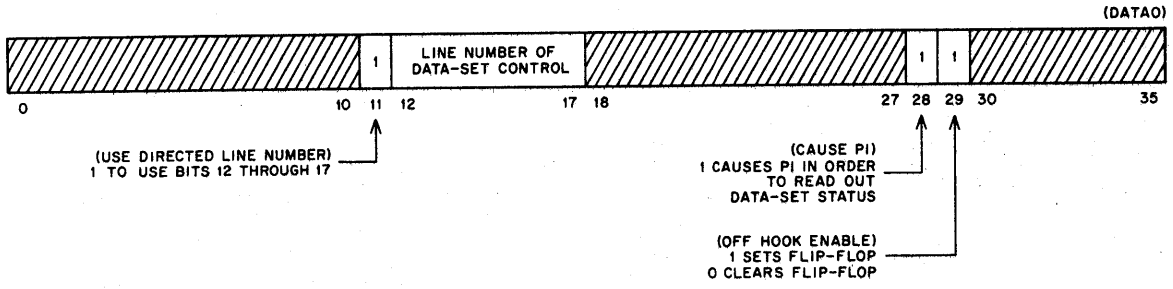


Each data-set line is equipped with an off hook enable flip-flop. When this flip-flop is in the 1 state and the data terminal ready one-shot is in the 1-state, the CD lead to the data set is ON. If the CD lead goes OFF, it is held off for 100 ms to insure that the data set disconnects properly.

A data-set only line is controlled by:

```
DATAO DLS, DSWD
```

where DSWD is as follows:



The off hook enable flip-flop may be cleared and set in successive instructions in order to disconnect a call and then allow the data-set to automatically answer another call.

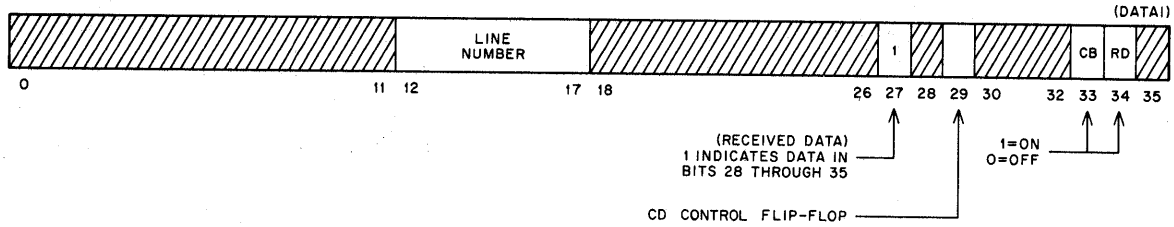
The state of the off hook enable flip-flop can be read out by a DATAI after the data-set flag has been raised. Two other bits of status are also read out. Clear to Send (CB) indicates that the data-set has shaken hands with another data-set and data may be transmitted. In the TWX system, and some other switched network systems, however, the transmission of data should wait until after the receipt of an "answerback" code from the called station if the call was originated at the computer end. If no answerback code appears within a few seconds, the call should probably be disconnected by using the off hook enable flip-flop described previously (switched network only). When answering a call in switched network systems, the computer may be required by the carrier's tariffs to send an answerback code when CB (clear to send) comes ON. When CB goes OFF, the data connection has been broken, either by the distant party disconnecting or by the connection being otherwise broken. Both the ON and OFF transitions of CB (clear to send) raise the data-set control line's receiver flag. Under some conditions the program may have to hang-up the local data-set (see DC10E special application notes below).

In switched network (TWX) service, a 4-row (100 or 150 word per minute)station (such as the computer/data-set conbination) may be connected to a 3-row (60 word per minute) station through an intermediate translator. In these or similar situations, a Restrain Detected (RD) signal informs the computer that the intermediate translator buffer is full and will not receive any more characters. The computer must stop sending until the restrain detected signal goes OFF again, or the translator will disconnect the data circuit. The ON transition of the RD (restrain detected) signal raises the data-set line's receiver flag.

Read the data-set status after a flag has been raised (artificial or other) by

```
...
DATAI DLS, LINEWD
TRNE LINEWD, 400              ;IS THIS RECEIVER DATA
(Jump to receiver rubroutine) ;YES
(Transmitter subroutine)      ;NO, TRANSMITTER INTERRUPT
                              (Must not be a data-set control)
...
(Dismiss Interrupt)
```

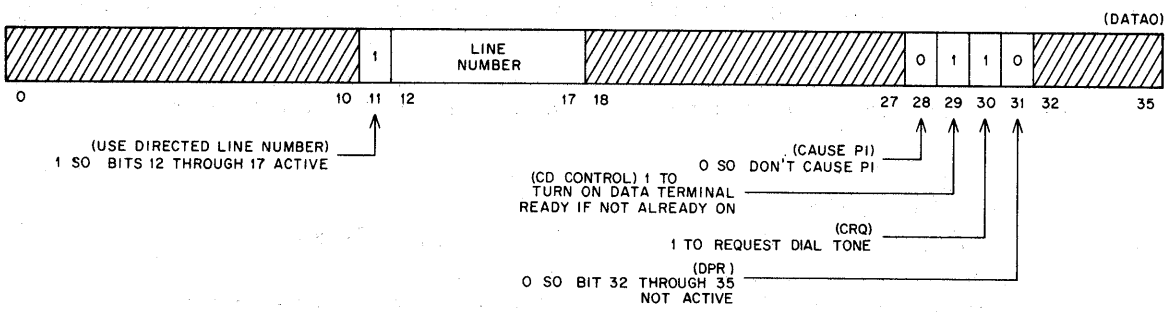
LINEWD will contain:



In switched network operations it is convenient to have the computer originate data calls. The DC10E provides control for two automatic calling (dialing) units (ACU's) in line positions 6 and 7. The automatic calling units are operated as follows. With the CD (data terminal ready) lead ON to the data-set, the CRQ (call request) lead to the automatic calling unit is turned ON. This picks up the telephone line and requests a dial tone. When the dial tone is received, the DLO (data line occupied) and PND (present next digit) lines come ON. Now the first digit of the number to be dialed is set up and transmitted as NB8 through NB1 with DPR (digit present) indicating that NB8 through NB1 are active. Each digit is loaded after PND comes ON. If a data connection is not established within 7 to 40s after the last digit (or if any other step is not completed within this time) (adjustable on the ACU) the ACR (abandon call and retry) line comes ON. The computer should turn OFF the CRQ (call request) line until the DLO (data line occupied) signal goes OFF (several seconds) and then retry the call. ON transitions of PND (present next digit) and ACR (abandon call and retry) raise the data-set line's receiver flag. The CRQ (call request) line may be turned OFF after CB (ready to send) is ON if the data set is strapped properly. All of the above ACU flip-flops are cleared by power clear.
Request a dial tone by

DATAO DLS, DIALRQ

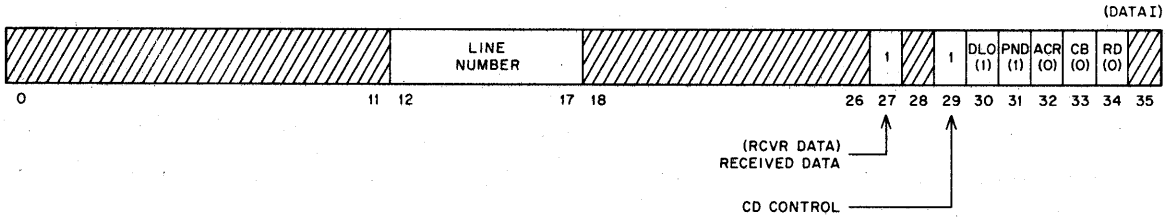
where DIALRQ contains:



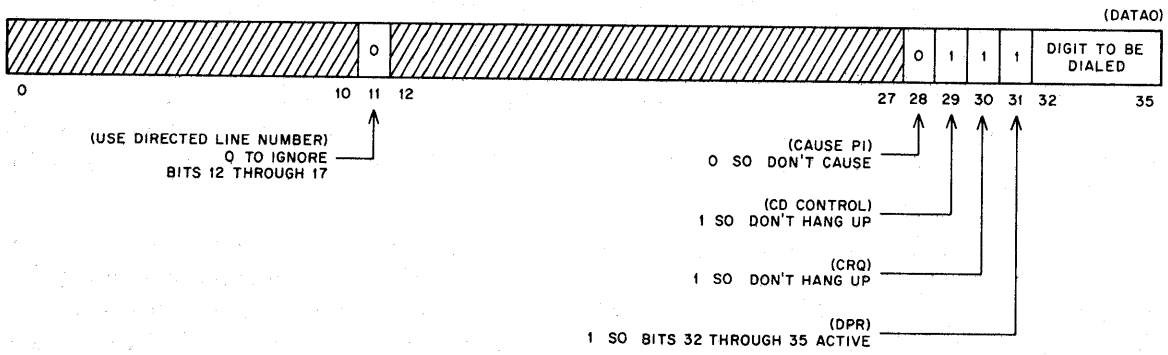
When the data-set line's flag is raised, do:

```
        ...
        DATAI DLS, LINEWD
        TRNE LINEWD, 400          ;IS THIS RECEIVED DATA
        (Jump to Receiver Subroutine)  ;YES
        (Transmitter Subroutine)  ;NO, TRANSMITTER INTERRUPT
        ...
        TRNE LINEWD, 20           ;IS PND ON
        DATAO DLS, DIGIT          ;YES
        -- --                     ;NO
        (Dismiss Interrrupt)
```

LINEWD will contain:



The DATAO sends the next digit to the automatic calling unit of the line interrupting. DIGIT should contain:



All of the above assume that the data-set and automatic calling units are equipped with the following options.

Automatic Answer (Data-Set)

Respond to Disconnect (Data-Set)

Long Space Disconnect (Data-Set)

Timer Stops upon Answer (Y Option) (ACU)

Drop CRQ after Answer (Z Option) (ACU)

Transfer to Data Set upon Answer (ACU)

Numerous other options are available and may be required for a particular type of service. For details, see, for example, Bell System Data Communications Technical Reference Manuals -- Station Arrangements to Provide TWX Service for Customer Provided Terminals (Data Auxiliary Set 811B); Data Auxiliary Set 801A (Automatic Calling Unit); Data Auxiliary Set 801C (Automatic Calling Unit); Data Set 103A etc., all Interface Manuals -- Data and Teletypewriter Planning Engineer, American Telephone and Telegraph Company or the equivalent interface manuals for other data-sets contemplated.

2.4.4.1 DC10E Special Application Notes - The exact signal from the data-set which is used by the DC10E is a function of the particular data-set and the circumstances in which the DC10E is used. When the DC10E is used with low speed (less than 300 baud) data sets (Bell System 103A, 811B, etc), the clear-to-send (CB) and carrier detector (CF) signals from the data-set are the same signal and either signal may be used to indicate to the DC10E that a data connection is established. In higher speed (1000-2000 baud) data sets (Bell System 202C, 202D, etc), the clear-to-send (CB) signal provides relatively little information whereas the carrier detected (CF) signal provides a meaningful indication that a data connection has been established.

In the low-speed case, the DC10E lead marked CLR TO SND EIA may be connected to either the CB or CF signal in the data-set. In the higher-speed case, the CLR TO SND EIA lead from the DC10E should be connected to the CF signal in the data set.

The DC10E lead marked RSTRN DETCTD EIA may be used to solve problems in the following three cases.

a. In 4-row TWX service, it should be connected to the RD lead of the data-set as described in the 811B manual ("Station Arrangements To Provide TWX Service For Customer-Provided Terminals (Data Auxiliary Set 811B) Interface Specifications Preliminary" November 1965) and detailed in DC10E programming.

b. In normal data-set service, the data-set may fail to hang up when called by a non-data-set telephone subscriber. In this case, either the data-set ready (CC) or ringing indicator (CE) signals may be connected to the RESTRN DETCTD EIA lead to allow the program to hang up the data-set (place it "on-hook") after a period of time with no carrier detected. (See the "Data Set 103A Interface specification," February 1967.) This arrangement is required only when certain types of Bell System equipment are servicing the data set (e.g., some types of dial foreign exchange equipment).

c. In an installation, it may be desired to have the program "answer the phone" when someone calls a data-set rather than allowing the data-set to answer automatically. In this case, the ringing indicator (CE) signal is connected to the RSTRN DETCTD EIA lead from the DC10E. When this signal becomes true, the program can (selectively, if desired) enable the DATA TERM READY EIA signal and allow the data-set to answer as described in the DC10E programming.

If the ringing indicator (CE) signal is used, features (b) and (c) can both be used. If none of these features using the RSTRN DETCTD EIA signal are desired, the RSTRN DETCTD EIA lead from the DC10E should be connected to a negative voltage of between -3V and -25V to maintain the signal OFF. A source of negative voltage is usually available at pin 10 of the data-set connector.

2.4.5 Maintenance Mode

When the MAINT switch is ON (UP), all scanner PI requests are inhibited and all I/O instructions addressed to the data line scanner are ignored. This effectively disconnects the data line scanner from the I/O bus. The only I/O bus function which is active in the MAINT mode is IOB RESET. In the MAINT mode, any character typed in from a teletypewriter will be echoed back to that teletypewriter. This feature serves as a gross check on the operation of the data line scanner and enables the checking of the teletypewriter circuits without the aid of the computer. Data terminal ready is false when the data line scanner is in the MAINT mode.

> NOTE: DATAI clears PI only if RCVR interrupt. DATAO clears PI unless IOB 12 (directed data) is 1. If simultaneous RCVR and TRANS interrupt occurs, the PI is cleared by DATAI but reappears within 1.8 μs, due to the TRANS interrupt.

CHAPTER 2A
INSTALLATION

This section contains general information on the DLS installation. Cross-connecting and cable terminating guidelines are provided as an aid to installation and installation planning. Option adjustments are required during installation because the DLS equipment contains a number of optional features. Guidelines for these option adjustments are explained under option card adjustments. Since actual installation procedures vary for each system, the information in this section is written in general terms and is intended as a guide for equipment installation.

2A.1 Cross Connecting and Cable Terminating Guidelines

The data lines of the DLS are interfaced at the quick-connect type terminal blocks located on the inside of the rear plenum door of the DC10A and DC10F. In either case, there are two rows of four connecting blocks in each cabinet. The connecting blocks in the upper row are called the line group terminals and are used to terminate the interface lines of the DC10B 8-Line Group Units, the DC10C Telegraph Relay Assembly, or the DC10E Expanded Data Set Control. The connecting blocks in the lower row are called the external cable terminals and are used for terminating external and intercabinet cables. The recommended external cable used to connect teletypes to the DLS is a 25-pair inside telephone cable of either 22 or 24 gage wire. It is terminated at the external cable terminals. When a data line located in one cabinet is connected to a cable terminated in another cabinet, an intercabinet cable is connected between the two cabinets and is terminated at the external cable terminals.

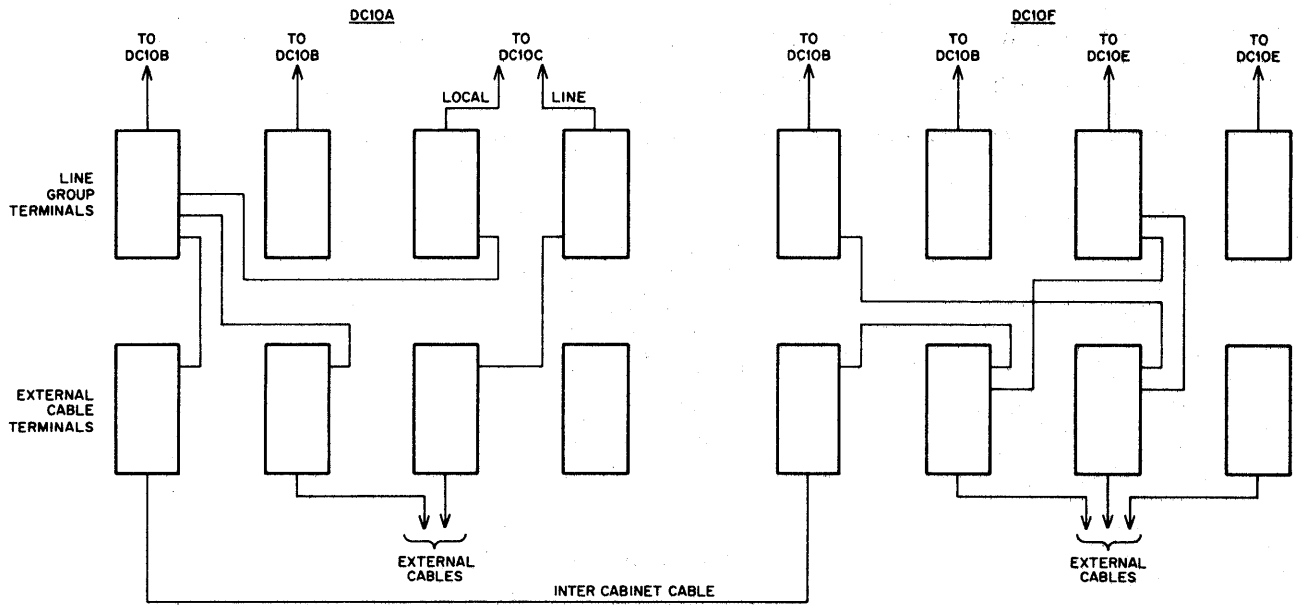
To prevent a DC10B line from receiving continuous space and interrupting with the character NULL (0_8), the "running open" condition, a jumper must be installed across the DC10B KYBD (DC) + and KYBD (DC) - terminals when no other wiring is present for a given line. To provide EIA printer signals, it is necessary to jumper the PRNTR (DC) + and PRNTR (DC) - terminals to activate the EIA printer output circuit. These jumpers may be inserted on the appropriate line group terminals. Refer to Table 2A-1 to obtain wire color to line name correspondence.

To connect a data line to a telephone cable, the necessary "cross-wire" pairs are installed between the line group terminals and the external cable terminals. Figure 2A-1 shows examples of typical wiring configurations.

Table 2A-1
Wire Color to Line Name Cross Reference Chart

Wire Color	DC1ØA (To DC1ØB)	See Note	DC1ØA (DC1ØC-LOCAL)	DC1ØA (DC1ØC-LINE)	DC1ØA (To DC1ØE)
White Blue	LØ KYBD (DC) + LØ KYBD (DC) -	1	LØ KYBD + LØ KYBD -	LØ KYBD + LØ KYBD -	LØ RSTRN DETCTD EIA (RD) LØ CLR TO SND EIA (CB)
White Orange	LØ PRNTR (DC) + LØ PRNTR (DC) -	2	LØ PRNTR + LØ PRNTR -	LØ PRNTR + LØ PRNTR -	LØ DATA TRM RDY EIA (CD) LØ AB (GND)
White Green	LØ KYBD EIA LØ PRNTR EIA	-	N/C N/C	N/C N/C	L1 RSTRN DETCTD EIA (RD) L1 CLR TO SND EIA (CB)
White Brown	L1 KYBD (DC) + L1 KYBD (DC) -	1	L1 KYBD + L1 KYBD -	L1 KYBD + L1 KYBD -	L1 DATA TRM RDY EIA (CD) L1 AB (GND)
White Slate	L1 PRNTR (DC) + L1 PRNTR (DC) -	2	L1 PRNTR + L1 PRNTR -	L1 PRNTR + L1 PRNTR -	L2 RSTRN DETCTD EIA (RD) L2 CLR TO SND EIA (CB)
Red Blue	L1 KYBD EIA L1 PRNTR EIA	-	N/C N/C	N/C N/C	L2 DATA TRM RDY EIA (CD) L2 AB (GND)
Red Orange	L2 KYBD (DC) + L2 KYBD (DC) -	1	L2 KYBD + L2 KYBD -	L2 KYBD + L2 KYBD -	L3 RSTRN DETCTD EIA (RD) L3 CLR TO SND EIA (CB)
Red Green	L2 PRNTR (DC) + L2 PRNTR (DC) -	2	L2 PRNTR + L2 PRNTR -	L2 PRNTR + L2 PRNTR -	L3 DATA TRM RDY EIA L3 AB (GND)
Red Brown	L2 KYBD EIA L2 PRNTR EIA	-	N/C N/C	N/C N/C	L4 RSTRN DETCTD EIA (RD) L4 CLR TO SND EIA (CB)
Red Slate	L3 KYBD (DC) + L3 KYBD (DC) -	1	L3 KYBD + L3 KYBD -	L3 KYBD + L3 KYBD -	L4 DATA TRM RDY EIA (CB) L4 AB (GND)
Black Blue	L3 PRNTR (DC) + L3 PRNTR (DC) -	2	L3 PRNTR + L3 PRNTR -	L3 PRNTR + L3 PRNTR -	L5 RSTRN DETCTD EIA (RD) L5 CLR TO SND EIA (CB)
Black Orange	L3 KYBD EIA L3 PRNTR EIA	-	N/C N/C	N/C N/C	L5 DATA TRM RDY EIA (CD) L5 AB (GND)
Black Green	L4 KYBD (DC) + L4 KYBD (DC) -	1	L4 KYBD + L4 KYBD -	L4 KYBD + L4 KYBD -	L6 RSTRN DETCTD EIA (RD) L6 CLR TO SND EIA (CB)
Black Brown	L4 PRNTR (DC) + L4 PRNTR (DC) -	2	L4 PRNTR + L4 PRNTR -	L4 PRNTR + L4 PRNTR -	L6 DATA TRM RDY EIA (CD) L6 PRSNT NXT DGT EIA (PND)
Black Slate	L4 KYBD EIA L4 PRNTR EIA	-	N/C N/C	N/C N/C	L6 ABNDN CALL EIA (ACR) L6 CALL REQ EIA (CRQ)
Yellow Blue	L5 KYBD (DC) + L5 KYBD (DC) -	1	L5 KYBD + L5 KYBD -	L5 KYBD + L5 KYBD -	L6 DIGIT PRESENT EIA (DPR) L6 NB1 EIA
Yellow Orange	L5 PRNTR (DC) + L5 PRNTR (DC) -	2	L5 PRNTR + L5 PRNTR -	L5 PRNTR + L5 PRNTR -	L6 NB2 EIA L6 NB4 EIA
Yellow Green	L5 KYBD EIA L5 PRNTR EIA	-	N/C N/C	N/C N/C	L6 NB8 EIA L6 DATA LINE OCC EIA (DLO)
Yellow Brown	L6 KYBD (DC) + L6 KYBD (DC) -	1	L6 KYBD + L6 KYBD -	L6 KYBD + L6 KYBD -	L6 AB (GND) L7 AB (GND)
Yellow Slate	L6 PRNTR (DC) + L6 PRNTR (DC) -	2	L6 PRNTR + L6 PRNTR -	L6 PRNTR + L6 PRNTR -	L7 RSTRN DETCTD EIA (RD) L7 CLR TO SND EIA (CB)
Purple Blue	L6 KYBD EIA L6 PRNTR EIA	-	N/C N/C	N/C N/C	L7 DATA TRM RDY EIA (CD) L7 PRSNT NXT DGT EIA (PND)
Purple Orange	L7 KYBD (DC) + L7 KYBD (DC) -	1	L7 KYBD + L7 KYBD -	L7 KYBD + L7 KYBD -	L7 ABNDN CALL EIA (ACR) L7 CALL REQ EIA (CRQ)
Purple Green	L7 PRNTR (DC) + L7 PRNTR (DC) -	2	L7 PRNTR + L7 PRNTR -	L7 PRNTR + L7 PRNTR -	L7 DIGIT PRESENT EIA (DPR) L7 NB1 EIA
Purple Brown	L7 KYBD EIA L7 PRNTR EIA	-	N/C N/C	N/C N/C	L7 NB2 EIA L7 NB4 EIA
Purple Slate	GND GND		N/C N/C	N/C N/C	L7 NB8 EIA L7 DATA LINE DCC EIA (DLO)

NOTES:
1. Jumper wires together when line is not in use.
2. Jumper wires together when PRNTR EIA line is in use.
   N/C - Not Connected



TYPICAL DC10 WIRING
(DC10A AND DC10F WITH FOUR 8-LINE GROUP UNITS, ONE TELEGRAPH RELAY ASSEMBLY, AND TWO EXPANDED DATA SET CONTROLS)

Figure 2A-1 Typical DC10 Cabling

Termination of cables and cross-wiring is performed using the 66A or 317B tool supplied with each system. This tool jams the wire onto the terminal and cuts off the excess wire. The wire is automatically stripped by the action of the quick connect terminals so that hand stripping is ordinarily unnecessary. When terminating wires, it is important to orient the tool so that it cuts the excess end of the wire rather than the conductor going to the cable.

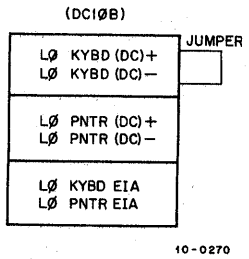
The connecting blocks will accommodate unstripped 20- to 26-gage wire which may be removed and the terminal reused an indefinite number of times. Stripped 18-gage wire is also accommodated by the connecting blocks, but this size wire permanently deforms the terminal so that only 18-gage wire can be used on the terminal thereafter. To prevent the inadvertent use of a deformed terminal for smaller wire, all deformed terminals should be marked with a felt tipped pen to identify them.

The recommended cable is a commerical 24 gage, 25-pair inside telephone wiring cables such as that available from Graybar Electric Company or Automatic Electric Company (offices in principal cities of the U.S.A.) or from any large cable or telephone supplies manufacturer.

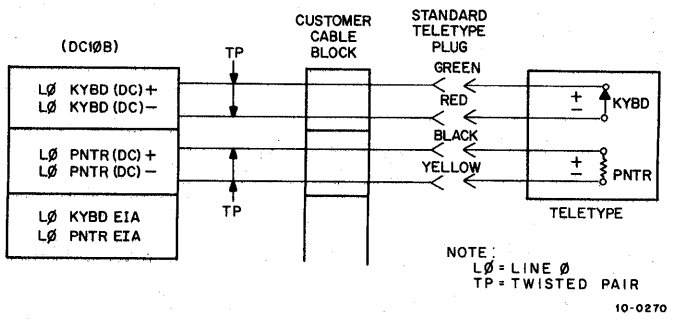
The standard color code for these cables is that shown in Table 2A-2. When a different color code is to be used, a cable pairing guide should be requested from the manufacturer. The tip and ring conductor notation used in Table 2A-2 comes from telephone switchboard usage. The tip conductor is always the topmost wire of the pair on the connecting block and is ordinarily the positive conductor of

the pair. Since keeping track of line-cable correspondence is a difficult and important job, a line assigner's book is provided with each DLS system.

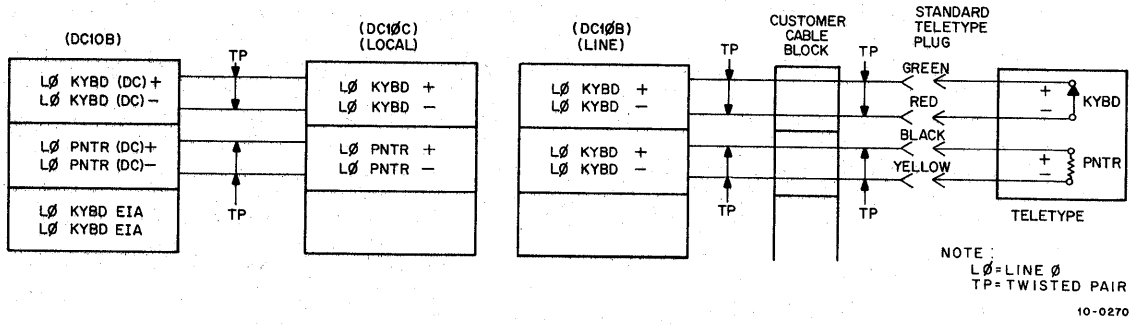
Examples of the most common cases of crosswiring are shown in Figure 2A-2.



A. Line Not in Use

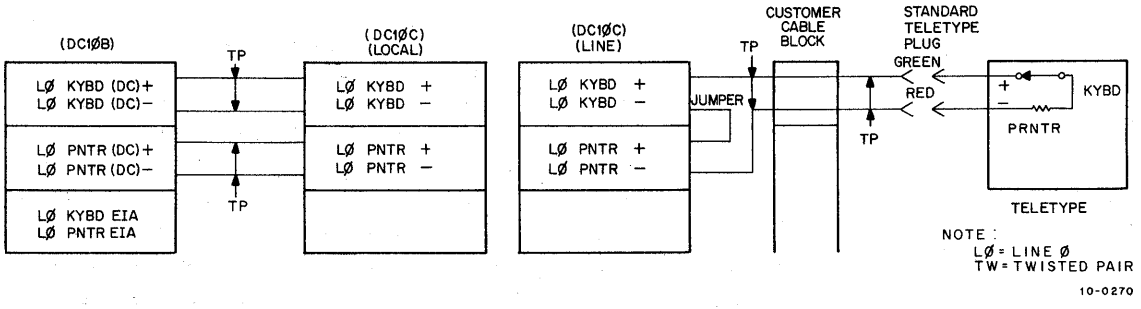


B. Local Line - Current Mode - Full Duplex
Model 33 or 35 Teletype

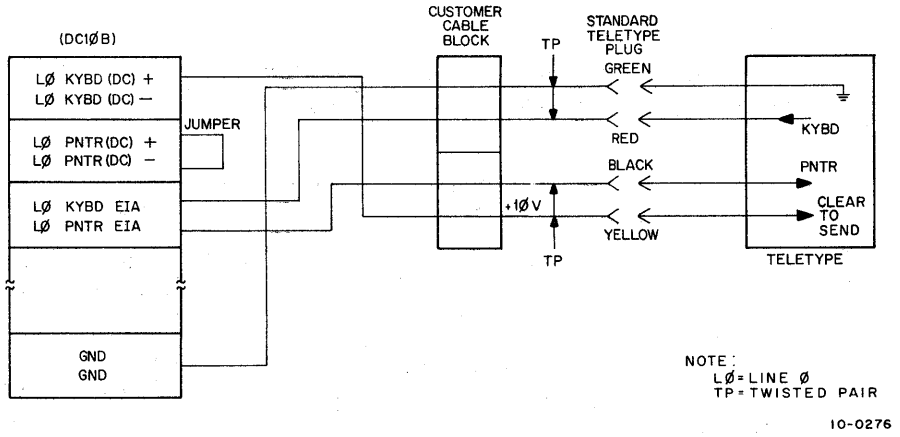


C. Long Line - Current Mode - Full Duplex

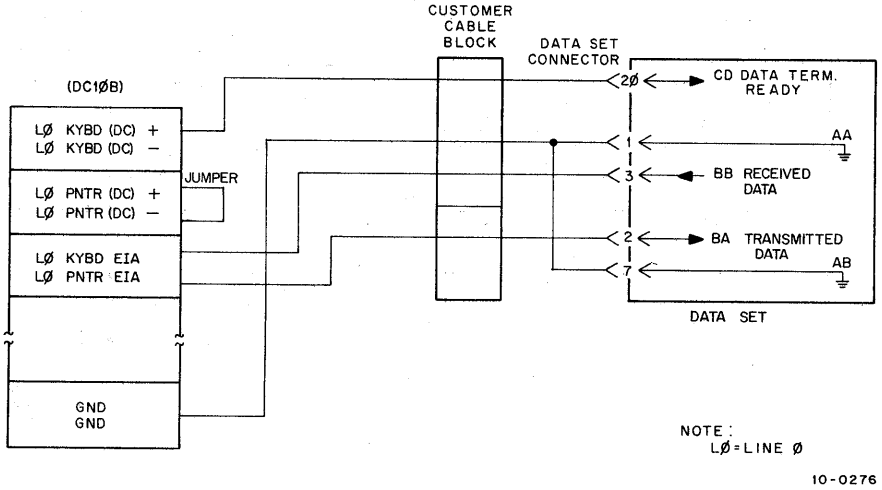
Figure 2A-2 Examples of Crosswiring



D. Long Line - Current Mode - Half Duplex

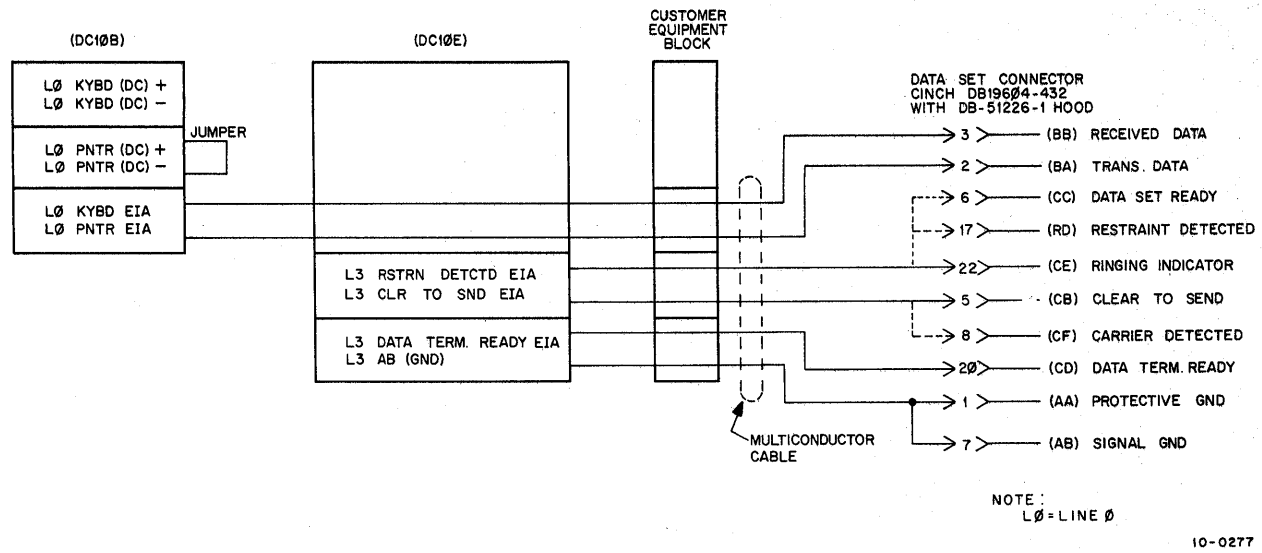


E. Local Line EIA - Model 37 Teletype

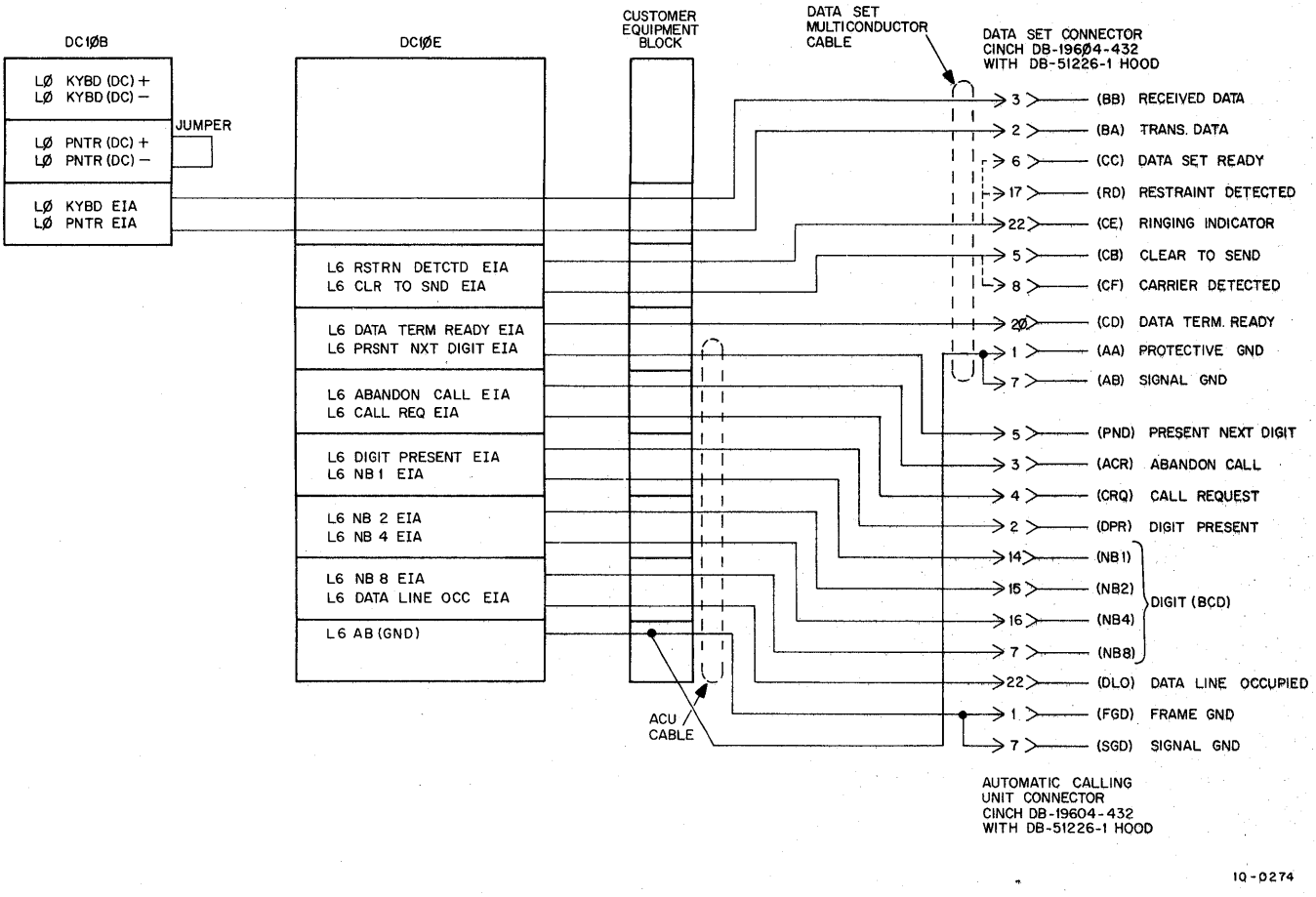


F. Local Line EIA - Western Electric 103A Data Set

Figure 2A-2 Examples of Crosswiring (Cont)



G. Connection to Data Set with DC10E
(Bell System 1Ø3A, 2Ø2C, 2Ø2D, 811B, etc.)



H. Connection to Data Set and Automatic Calling Unit
(Bell System 8Ø1A, etc.)

Figure 2A-2 Examples of Crosswiring (Cont)

2A.2 Option Card Adjustments

DLS equipment has been designed with a number of optional features that can be used to adapt the DLS to fulfill varying user requirements. Due to this fact, a number of adjustments may be required at the time of installation or whenever system requirements are changed after installation. To simplify these adjustments, option cards have been inserted at the points where these adjustments are required. The following information explains the function of these cards and explains the adjustment procedure for each.

Table 2A-2
Cable Pairing Guide

Pair Number	Tip Conductor	Ring Conductor	Pair Number	Tip Conductor	Ring Conductor
1	white	blue	14	black	brown
2	white	orange	15	black	slate
3	white	green	16	yellow	blue
4	white	brown	17	yellow	orange
5	white	slate	18	yellow	green
6	red	blue	19	yellow	brown
7	red	orange	20	yellow	slate
8	red	green	21	purple	blue
9	red	brown	22	purple	orange
10	red	slate	23	purple	green
11	black	blue	24	purple	brown
12	black	orange	25	purple	slate
13	black	green			

2A.2.1 Clock Divider Option Card - The Clock Divider Option Card (Type W990) is located in card slot D19 of the DC10A (see drawing D-BS-DC10A-0-CLKD). This option card is used to select the baud-rate clock frequencies for baud rates between 40 baud and 100 kilobaud by connecting jumpers into various configurations among the input and output pins listed in Table 2A-3. The output clock frequency is eight times the baud rate. For rates of 40 to 999 baud, the required clock frequency is 128 times the baud rate (5.12 kHz to 128 kHz) and the clock frequency is divided by 16 (128 ÷ 16 = 8). When the

desired baud rate is between 1 kilobaud and 100 kilobaud, the clock frequency is divided by one to provide the required clock frequency of eight times the baud rate (8 kHz to 1.6 MHz).

The selection of the crystal frequency of the three clocks (F1, F2, and F3) can be varied by installing the desired value clocks in card slots D10, D11, and D12. When frequencies are not specified by the customer, the DC10A is supplied with clocks for 110 baud (Model 33 and 35 Teletypes), 150 baud (Model 37 Teletype), and 1200 baud (Western Electric Model 202 Data Set or equivalent).

By various jumper configurations, the W990 provides three line speeds common to groups 0-3 (signals CLKD CLOCK F1 A IN through CLKD CLOCK F3 A IN) and three potentially different speeds for groups 4-7 (signals CLKD CLOCK F1 B IN through CLKD CLOCK F3 B IN). In addition, a variety of speeds is made available by using Clock F3 to provide for frequencies based on powers-of-two multiples of the line's required baud rate. For example, if line groups 0-3 require speeds of 110, 300, and 1200 baud and line groups 4-7 require speeds of 110, 150, and 56.84 baud, the jumper connections are as shown in Figure 2A-3.

Table 2A-3
Clock Frequency and Jumper Connections

Clock	Baud Rate	Clock Frequency (kHz)	Divide by	Jumper	
				From	To
F1 (D1Ø)	40-999	5.12-128	16	D	See Note 1
	1,000-200,000	8-1,600	1	F	
F2 (D11)	40-999	5.12-128	16	J	
	1,000-200,000	8-1,600	1	L	
F3 (D12)	40-999	5.12-128	16	N	
	1,000-200,000	8-1,600	1	R	
	80-1999	See Note 2	8	S	
	160-3999		4	T	
	320-7999		2	U	

NOTE 1: The output pins are as follows:

	Groups Ø-3			Groups 4-7		
Clock Signal	F1 A IN	F2 A IN	F3 A IN	F1 B IN	F2 B IN	F3 B IN
Pin	E	K	P	H	M	V

NOTE 2: The clock frequency is based on divide-by-one, e.g., if F3 is 1200 baud (9600 Hz at pin R), pin U supplies 600 baud (4800 Hz), pin T supplies 300 baud (2400 Hz), and pin S supplies 15Ø baud (1200 Hz).

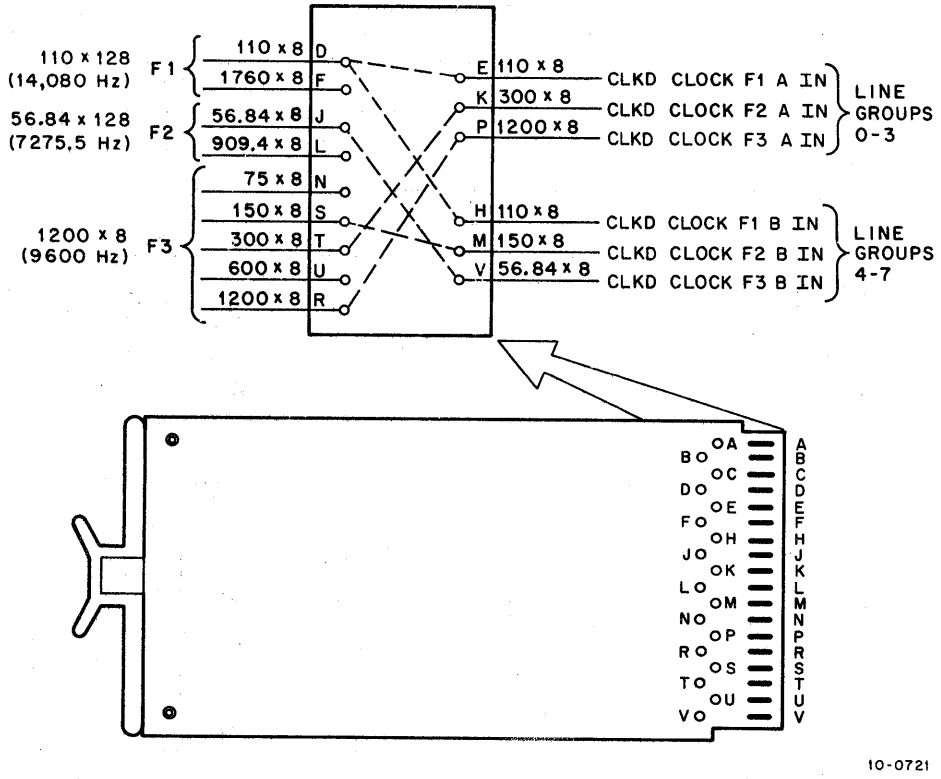


Figure 2A-3 Typical Jumper Configuration

2A.2.2 Device Number Option Cards - The device numbers from the central processor are routed to all devices connected to the I/O bus via the 14 device-selection lines (7 pairs) of the I/O bus. In the DLS, the device selection lines are terminated at the device-number option cards located in slots E17 and E18 of the DC10A. Jumpers located on these option cards can be arranged so the DLS will respond to any device number. If a device number has not been specified by the customer, the jumpers on the device number option cards are connected so that the DLS will respond to the standard device number 240_8. To prevent the DLS from responding to more than one device number, one jumper of each pair must always be connected.

Figure 2A-4 is provided to aid maintenance personnel in understanding the device number option cards. A schematic representation of the device number option cards as shown in drawing number D-BS-DC10A-0-DLS shows the jumper placement for the standard device number. The location of the jumper associated with each octal digit is shown in a pictorial representation. If a different device number is to be used, the tables on Figure 2A-4 may be used to determine the location of the jumpers as shown in the following example.

Example:

Standard Device Number 240_8

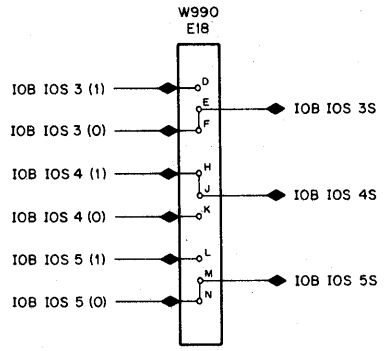
First Octal Digit			Second Octal Digit			Third Octal Digit
Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9
0	1	0	1	0	0	0

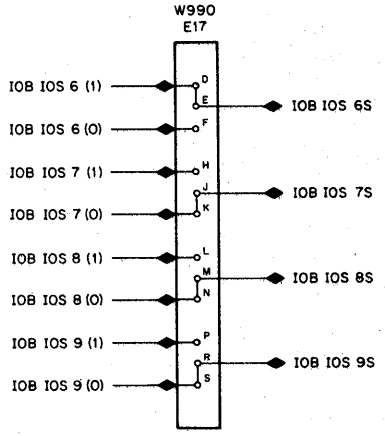
E18 Jumpers

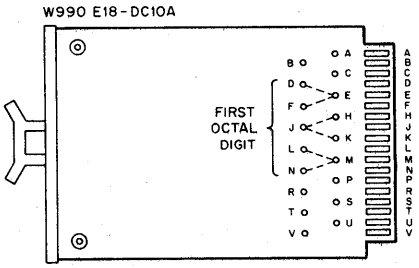
Bit 3 - E to F
Bit 4 - J to H
Bit 5 - M to N

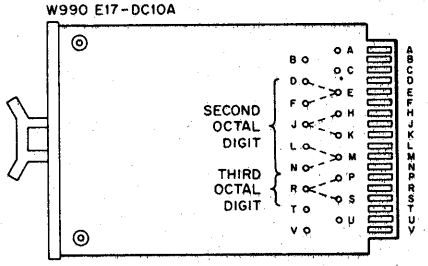
E17 Jumpers

Bit 6 - E to D
Bit 7 - J to K
Bit 8 - M to N
Bit 9 - R to S









DIGIT NO.	BIT NO.	E18 JUMPERS	
		FROM	TO
FIRST OCTAL DIGIT	BIT 3=1	E	D
	BIT 3=0		F
	BIT 4=1	J	H
	BIT 4=0		K
	BIT 5=1	M	L
	BIT 5=0		N

DIGIT NO.	BIT NO.	E17 JUMPERS	
		FROM	TO
SECOND OCTAL DIGIT	BIT 6=1	E	D
	BIT 6=0		F
	BIT 7=1	J	H
	BIT 7=0		K
	BIT 8=1	M	L
	BIT 8=0		N
THIRD OCTAL DIGIT	BIT 9=1	R	P
	BIT 9=0		S

Figure 2A-4 Device Number Option Cards (DC10A)

2A.2.3 Clock Line Option Card- The three clock frequencies used in establishing the signaling speeds of the data lines are generated in the DC10A. These clock frequencies are routed to and terminated at the clock line option card located in slot B30 of each DC10B. After the signaling speeds of the eight data lines associated with the DC10B are determined, all common clock lines that operate at the same signaling speed are jumpered together and are connected to their common input clock frequency at the clock line option cards. Figure 2A-5 shows a schematic representation of the clock line option card as shown on drawing D-BS-DC10B-0-COMM. A pictorial representation of the card is shown with its jumpers connected as follows: common clock lines 0,1,2, and 4 are connected to clock 1; common clock line 7 is connected to clock 2; and common clock lines 3, 5, and 6 are connected to clock 3. This example is not to be considered "typical" because the actual jumper placement for any system is dependent upon the signaling speeds of devices connected to the DLS via the data lines.

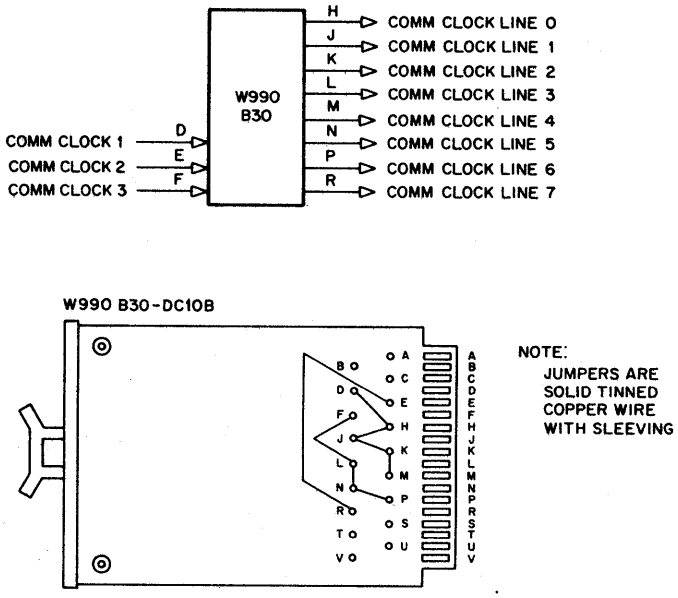
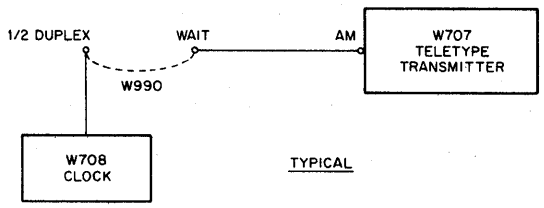
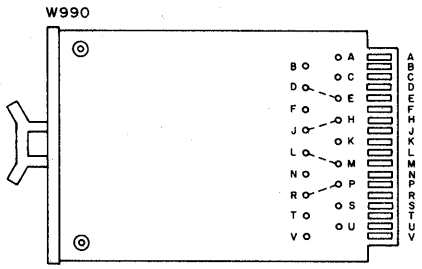


Figure 2A-5 Clock Line Option Card (DC10B)

2A.2.4 Half-Duplex Option Cards - Each data line in the DC10B may be operated as a full-duplex line, a full-duplex line with local copy, or a half-duplex line. All data lines are connected to operate as full-duplex lines when the DC10B is shipped. When it is desired to operate a data line as a full-duplex line with local copy or a half-duplex line, a jumper must be inserted on the appropriate half-duplex option card to adjust the logic characteristics of the transmitter timing. If this jumper is not connected, characters will be garbled when the teletype keyboard is in use at the same time as the central processor is sending characters.

Figure 2A-6 shows a typical schematic of the jumper connections and a pictorial representation of the half-duplex option card showing the jumper terminals. A table that identifies the card locations, data line numbers and jumper connections is also supplied. After the operating characteristics of each data line have been determined, a jumper is inserted according to the table in Figure 2A-6 for each data line that is to operate as a full-duplex line with local copy or a half-duplex line.





OPTION CARD LOCATION	DATA LINE	TO OBTAIN HALF DUPLEX CONNECT JUMPER		JUMPERS SHOWN ON ENGINEERING DRAWING
		FROM	TO	
B09-DC10B	0	D	E	D-BS-DC10B-0-L01
	1	H	J	
	2	L	M	D-BS-DC10B-0-L23
	3	P	R	
B24-DC10B	4	L	M	D-BS-DC10B-0-L45
	5	P	R	
	6	D	E	D-BS-DC10B-0-L67
	7	H	J	

Figure 2A-6 Half-Duplex Option Card (DC10B)

2A.2.5 Teletype Receiver Module - The Teletype Receiver Module W706, has several jumpers that are used to select either a 5-bit or 8-bit code with a 1, 1.5, or 2 unit stopping interval. A pictorial view of both revisions of the double-height modules available contained in Figure 2A-7 identifies the jumper locations. After the timing requirements for each data line are established, the appropriate jumpers are inserted on the modules. The table located on Figure 2A-7 identifies the DC10B card slots where the W706 modules associated with each data line are located. The most common jumpering for

PDP-10 usage is an 8-bit with the "NO RUN OPEN" option, but other configurations are used depending upon system specifications. The most common 5-bit code has a 7.42 unit code length (1 unit start, 5 unit code, and 1.42 unit stop). When this 5-bit code is used, the W706 module is jumpered for a 1 unit stop and the additional 0.42 unit is treated as intercharacter waiting time.

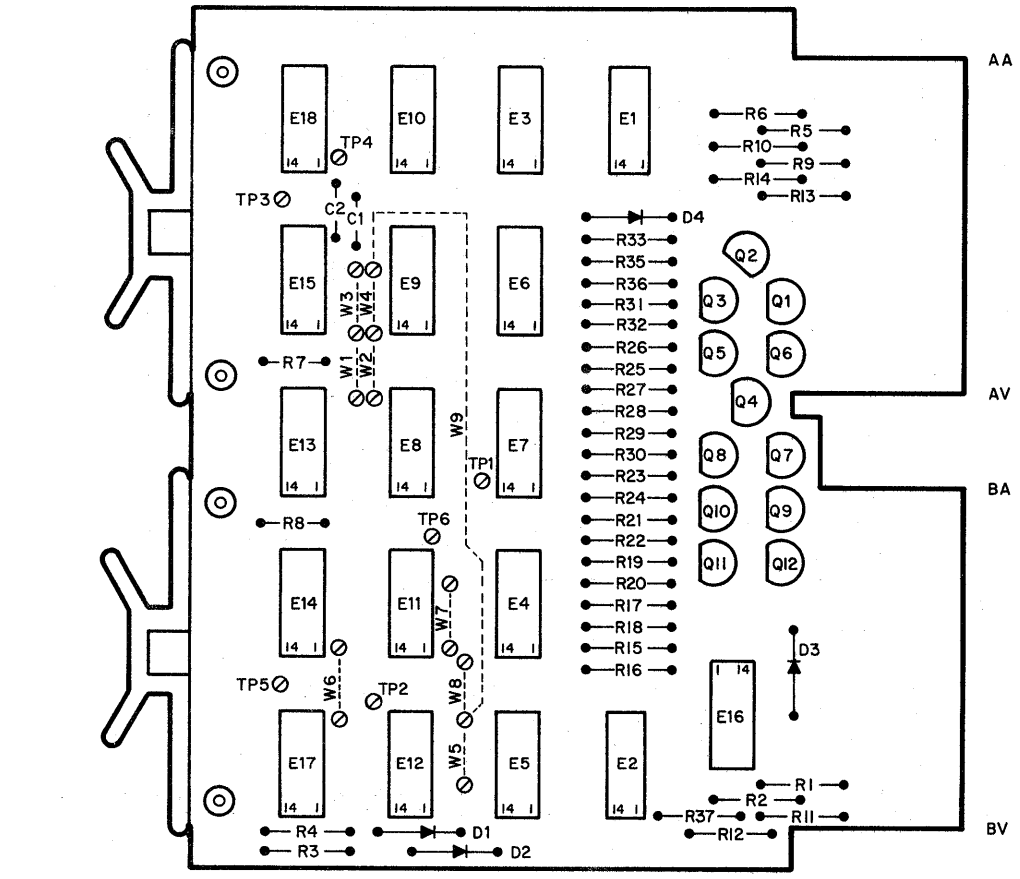
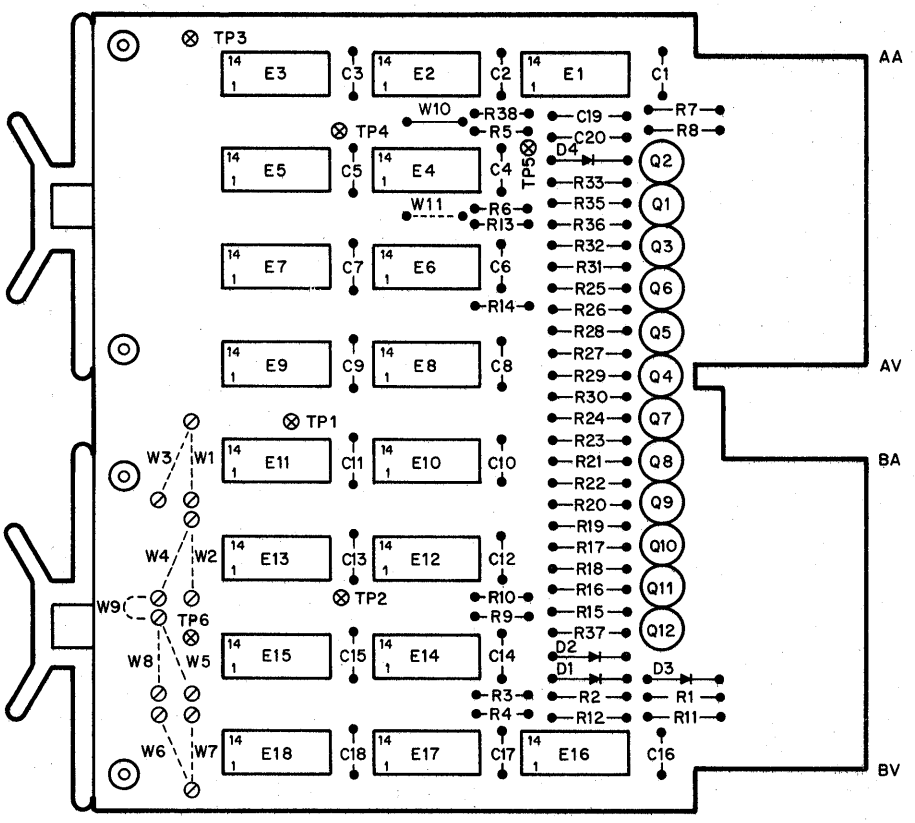


Figure 2A-7 Teletype Receiver Module W706
(Etch Rev. C, CS Rev. A, after PDP-10 Modification)



OPTION WIRING

5 BIT CODE: INSERT W3 & W4 REMOVE W1 & W2
8 BIT CODE: INSERT W1 & W2 REMOVE W3 & W4

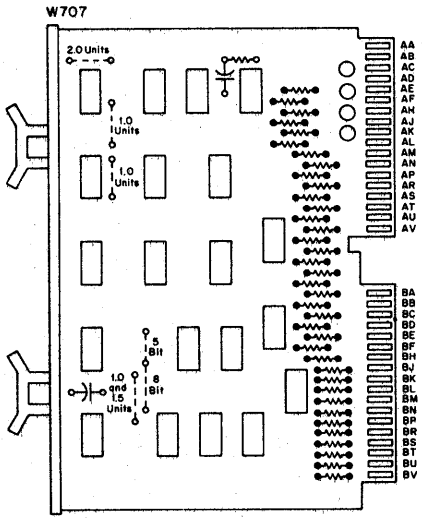
NO RUN OPEN: INSERT W6 & W9 REMOVE W5,W7 & W8 - (RECOMMENDED)
1.0 UNIT STOP: INSERT W5 & W6 REMOVE W7,W8 & W9
1.5 UNIT STOP: INSERT W5 & W6 REMOVE W7,W8 & W9
2.0 UNIT STOP: INSERT W7 & W8 REMOVE W5,W6 & W9
2.5 UNIT STOP: INSERT W6 & W8 REMOVE W5,W7 & W9

CLEAR FLAG ON READ STROBE (SPECIAL APPLICATIONS): INSERT W11 (INSULATED WIRE) REMOVE W10
DON'T CLEAR FLAG ON READ STROBE (FACTORY STANDARD): INSERT W10 REMOVE W11

10-0722

Figure 2A-7 Teletype Receiver Module W706 (Cont)
(Etch Rev. D, CS Rev. B, after PDP-10 Modification)

2A.2.6 Teletype Transmitter Module - The Teletype Transmitter Module, W707, has several jumpers that are used to select either a 5-bit or 8-bit code with a 1, 1.5, or 2 unit stopping interval. A pictorial view of the double height module contained in Figure 2A-8 is used to identify the jumper locations. After the timing requirements for each data line are established, the appropriate jumpers are inserted on the modules. A table located on Figure 2A-8 identifies the DC10B card slots where the W707 modules associated with each data line are located. A W707 module jumpered for an 8-bit code with a 2 unit stop is the most common jumpering arrangement used with the PDP-10. When a 5-bit code with 7.42 unit code length (1 unit starts, 5 unit code, and 1.42 unit stop) is used, a W707 module is jumpered for a 1.5 unit stopping interval thus insuring an adequate stopping interval (7.50 unit code length).



DATA LINE NO.	DC10B CARD SLOT NO.
0	AB08
1	AB11
2	AB14
3	AB17
4	AB20
5	AB23
6	AB26
7	AB29

Figure 2A-8 Teletype Transmitter Module W707 (DC10B)

2A.2.7 Telegraph Line Module - The G854 Telegraph Line Module has several split lug tie points. Jumpers are connected between the split lugs to condition the module for different types of operation. A pictorial view of the single height, double thickness FLIP CHIP module contained in Figure 2A-9 identifies the components, split lug locations and the DC10C card slots in which the modules are located. Sixteen G854 modules are supplied with each DC10C, one for each KYBD and PRNTR line.

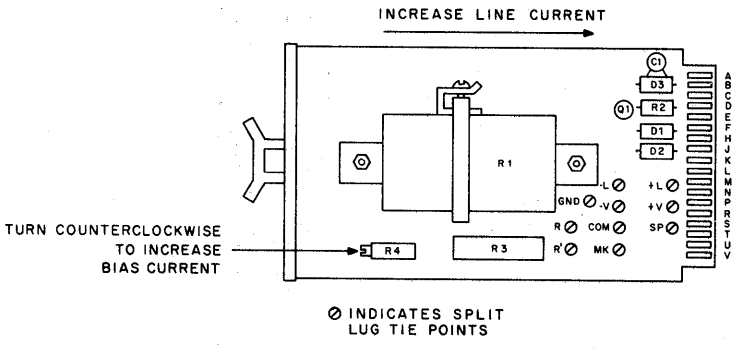
Since a G854 is used in both the transmit and receive circuits, Figure 2A-10 contains a schematic of each type of circuit to show the typical wiring. The split lug strapping required for the different applications is provided in tabular form below the associated schematic.

The polar relay bias circuit provides a high impedence bias circuit to set the operating point of the low resistance polar relay. Bias current I_b may be adjusted over a range of 3.5 to 60 mA. The bias voltage V_b across the polar relay should be approximately 4V or less to allow for transient voltage swings caused by relay operation without cutting off the bias circuit.

The following limitations apply (refer to Figure 2A-10):

$8 - V_b$ less than 20V (transistor breakdown)

$I_b\ (8 - V_b)$ less than 500 mW (transistor power limit)



KYBD		PRNTR	
LINE NO.	CARD SLOTS	LINE NO.	CARD SLOTS
0	A12	0	B12
1	A14	1	B14
2	A18	2	B18
3	A20	3	B20
4	A24	4	B24
5	A26	5	B26
6	A30	6	B30
7	A32	7	B32

Figure 2A-9 Telegraph Line Module G854 (DC10C)

Both of these limitations assume that the polar relay bias winding is returned to ground as shown in Figure 2A-10.

An adjustable resistor, R1, in the line resistance circuit controls the current in the telegraph line by padding out the total dc circuit resistance (wire resistance plus R1) to the required value.

Example: A 60 mA circuit with a 120V power supply requires a total circuit resistance of 2 kilohms. If the wire resistance is 500 ohms, R1 must be set at 1.5 kilohms to obtain the required total circuit resistance.

In addition to the line resistance, two clamp diodes, D1 and D2, are provided to partially meet the telegraph line interface requirements of various telecommunication administrations throughout the world. The diodes have a peak-inverse-voltage rating of 400V.

Example: The Borogardian Telecommunication Authority requires that telegraph line interfaces have the following properties:

a.	Open circuit voltage	-50V
b.	Current with line resistance of 2 kilohms	20 mA
c.	Short circuit current	30 mA

Refer to Figure 2A-11 for the following explanation. The first requirement is met by having a clamp power supply of -50V. (The clamp power supply does not supply power, but must absorb it instead. Most power supplies must be preloaded with a load resistor to allow this type of operation.)

The second requirement provides -40V across the interface terminals when rated load is applied which is not inconsistent with the first requirement. It requires

$$V_{supply} = 20\ mA\ (R1 + 2\ kilohms)$$

The third requirement requires

$$V_{supply} = 30\ mA\ (R1)$$

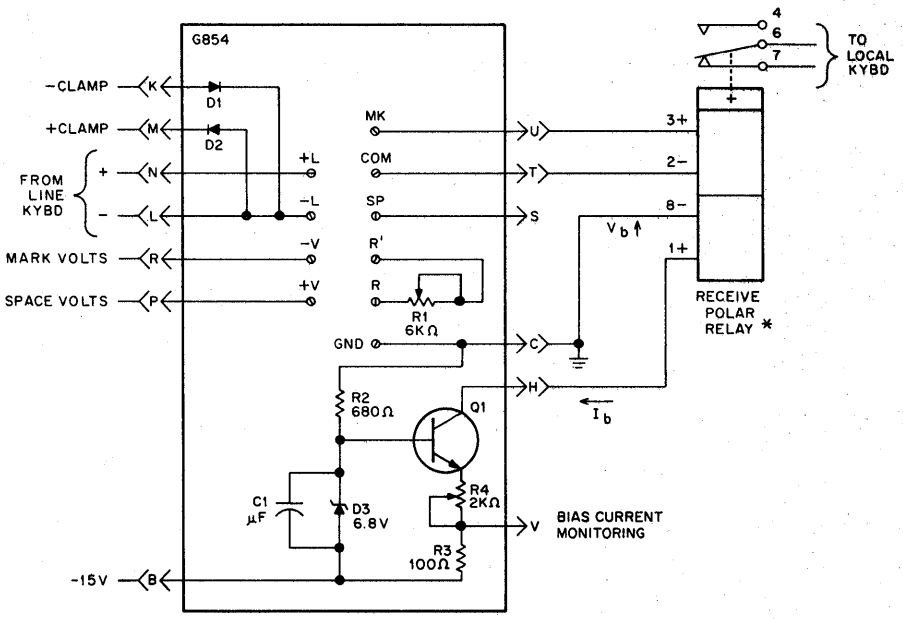
If $V_{supply} = -120V$ and $R1 = 4$ kilohms, requirements 2 and 3 are satisifed.

A 10 W adjustable power resistor, R1, is used to pad the total dc circuit resistance and obtain the desired line current. A trimpot, R4, is used to adjust the polar relay bias current and established the operating point of the polar relay. Perform the following procedures for each line during installation.

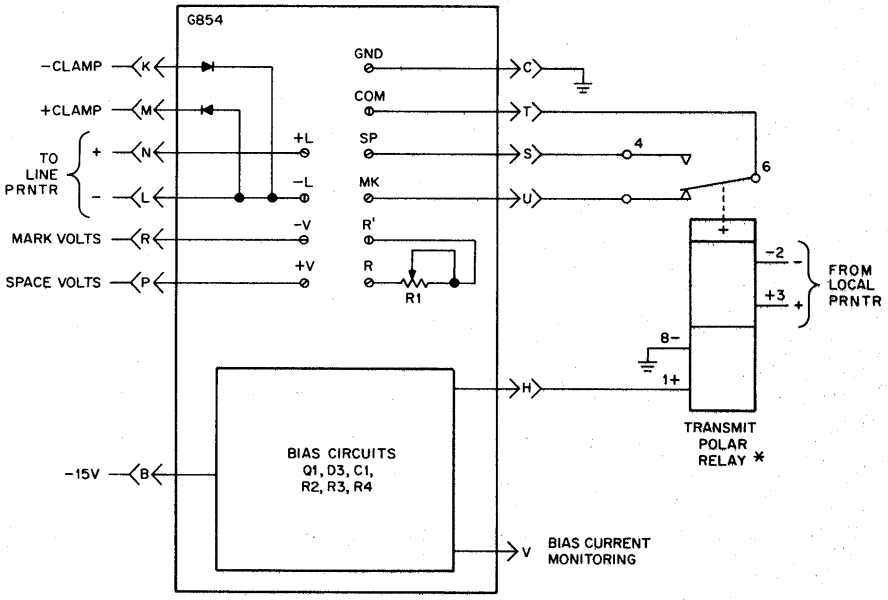
a. Line Current Adjustment - The following procedure provides the recommended line current adjustment procedure for the G854 Telegraph Line Module. Refer to Figure 2A-9 for component location and Figure 2A-10 for circuit schematic.

CAUTION

The adjustment slider of the line resistor R1 is connected to the 125V dc line. Injury to personnel or damage to equipment may result if the line current is adjusted with the line voltage applied.



TYPE OF OPERATION	SPLIT LUG STRAPPING			
NEUTRAL RECEIVER NEGATIVE MARK	GND TO +L	-L TO R	R' TO MK	COM TO -V
NEUTRAL RECEIVER EXTERNAL PWR. SUPPLY	+L TO COM	-L TO MK	—	—
POLAR RECEIVER	+L TO COM	-L TO MK	SET POLAR RELAY BIAS TO ZERO	



* TYPICAL POLAR RELAY : CURRENT FROM (+) TO (-) MOVES CONTACT TOWARD 7. CONTACTS ARE BISTABLE.

TYPE OF OPERATION	SPLIT LUG STRAPPING				
NEUTRAL TRANSMITTER NEGATIVE MARK	GND TO +L	-L TO R	R' TO COM	MK TO -V	—
NEUTRAL TRANSMITTER EXTERNAL PWR. SUPPLY	+L TO COM	-L TO MK	—	—	—
POLAR TRANSMITTER	GND TO +L	-L TO R	R' TO COM	MK TO -V	SP TO +V

Figure 2A-10 G854 Strapping (DC10C)

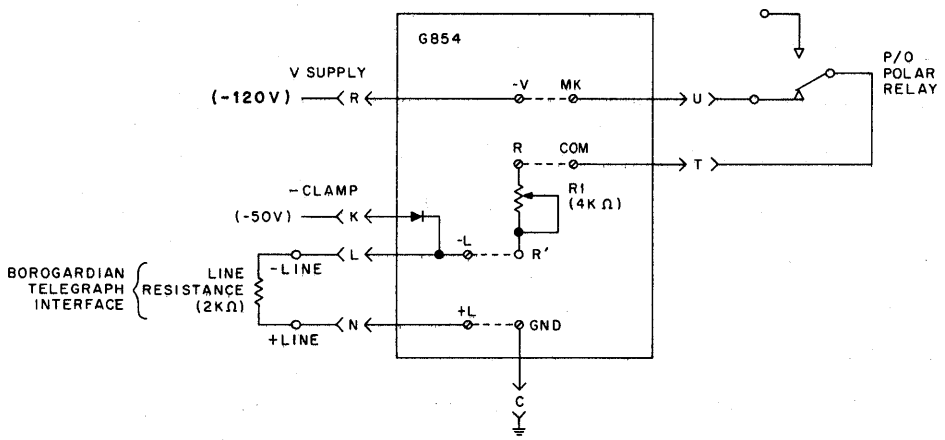


Figure 2A-11 Interface for the Borogardian Telecommunication Administration

1. Turn line voltage off and remove the G854 module to be adjusted from its connector.

2. Set the line resistor at maximum resistance (minimum line current). See Figure 2A-9.

3. Replace the G854 module. A W980 or G998 module extender may be used to extend the module during the adjustment procedure.

4. Set up an ammeter to measure the line current. (A Hewlett-Packard 428B Clip-On dc milliammeter is convenient for this purpose).

5. Turn on the line voltage. Read and compare the line current with the desired value of line current.

6. If the desired line current value is not observed, turn line voltage off and remove the G854 module, if a module extender is not used. Decrease the line resistance to increase the current or increase the line resistance to decrease line current (see Figure 2A-9).

7. Repeat steps (5) and (6) as a trial-and-error procedure until the measured line current equals the desired value.

b. Bias Current Adjustment - The bias current of the G854 Telegraph Line Module is adjusted in the following manner. Refer to Figure 2A-9 for component location and Figure 2A-10 for circuit schematic.

1. Determine the desired bias current I_b (normally one-half of the signal current).

2. Turn on the line voltage and connect a voltmeter (or suitable voltage measuring device) from pin B (-) to pin V (+) of the module's connecting block.

CAUTION

Use a plastic tuning tool or an insulated screwdriver to avoid shock if the adjusting tool should slip.

3. Observe the voltmeter and adjust R4 until the voltmeter reading equals .1 I_b in mA. Variations from this nominal value may be used in an attempt to correct for signal distortion.

2A.3 I/O Bus Connections

The DC10A is connected to the central processor via the I/O bus. In the PDP-10 system, the I/O bus cables are routed from the central processor and are looped through each of the PDP-10 options that operate from the I/O bus. The cables end in W851 connector modules that plug into the logic rack. The margin cable and the remote turn-on cable are looped through each of the PDP-10 options to complete the margin circuit and the remote turn-on circuit.

Since the floor plan for each PDP-10 system may vary, the routing of the I/O bus cables may also vary. Therefore, the I/O bus cables for each option may be custom manufactured to meet a specific system requirement. To determine the I/O bus routing for the DC10A, refer to the floor plan for the system. Guidelines for installation of the I/O bus cables are contained in the PDP-10 Installation Manual. Figure 2A-12 is provided to indicate the location of the I/O bus cables in the DC10A.

CABLE NO.	CONNECTOR MODULE	DC10A CARD SLOTS	
1	1A & 1B	EF 21	EF 25
	1C & 1D	EF 22	EF 26
2	2A & 2B	EF 23	EF 27
	2C & 2D	EF 24	EF 28

Figure 2A-12 Location of DC10A I/O Bus Connections

2A.4 Teletype Information

Teletypes and other user terminals need to meet only a minimum number of requirements to be used with the standard PDP-10 hardware-software system. Violation of any particular requirement requires the use of some hardware option, special interface, or a modification of the standard software. In many cases, the change is quite simple (e.g., supplying extra NUL characters to allow a slow carriage to return). PDP-10 software is designed around an ordinary (essentially unmodified) Teletype machine using the ASCII (USASCII) character codes.

In the following paragraphs, details of the standard interfaces are supplied.

a. The terminal must have a 20 mA, neutral, full-duplex or an EIA interface.

b. The terminal must use self-synchronizing, asynchronous, serial-by-bit, serial-by-character data transmission (i.e., ordinary, start-stop, teletype-style data transmission).

c. The printer or display part of the terminal must respond to the control characters CR (carriage return, 015_8) and LF (line feed, 012_8) in the ordinary way. Response to other control characters is not required.

d. The printer or display must have "continuous paper"-like characteristics. That is, a special control should not be required to "advance-to-the-next page" (erase the present display).

e. No waiting time beyond that provided by a CR LF sequence (carriage return, line feed) should be required to return the printing carriage to the beginning of the line.

f. The printer or display should respond to at least the first 64 graphics of ASCII (USASCII "figures"-040_8 to 077_8, and "upper case"-100_8 to 137_8). Any version of ASCII can be used with the user performing translations as necessary. All 95 graphics of USASCII can be used when available.

g. The keyboard must be able to generate at least one of the ALT-MODE or ESC (PREFIX) codes (033_8, 175_8, 176_8).

h. The keyboard must be able to generate the control characters of ASCII (000_8 to 037_8) and at least the first 64 graphics of ASCII.

i. The terminal should not have any "funny" or "strange" features (i.e., features not predictable from some reasonable interpretation of some revision of the ASCII standard).

Any terminal which meets the above requirements should be a usable terminal. An ordinary Teletype without PDP-10 modifications may not be as convenient to use as an ordinary Teletype with PDP-10 modifications, but it will be adequate for many uses.

Teletypes supplied by DEC for PDP-10 systems will have the following as standard features: LOCAL (off-line) mode; slashed zero (Ø), upward arrow, and left arrow characters; separate ALT MODE, ESC, or PREFIX key; and standard plug connector. When considered necessary by DEC engineering, various mechanical modifications will also be incorporated to provide improved reliability and user convenience.

Connections for 20 mA, neutral, full-duplex terminals (most Model 33 and 35 Teletypes and similar equipment) are completed as follows. Modify the machine for 20 mA line current and full-duplex operation as indicated on the drawing furnished by the manufacturer. Connect a 283B plug as shown in Figure 2A-13. Polarity must be as indicated.

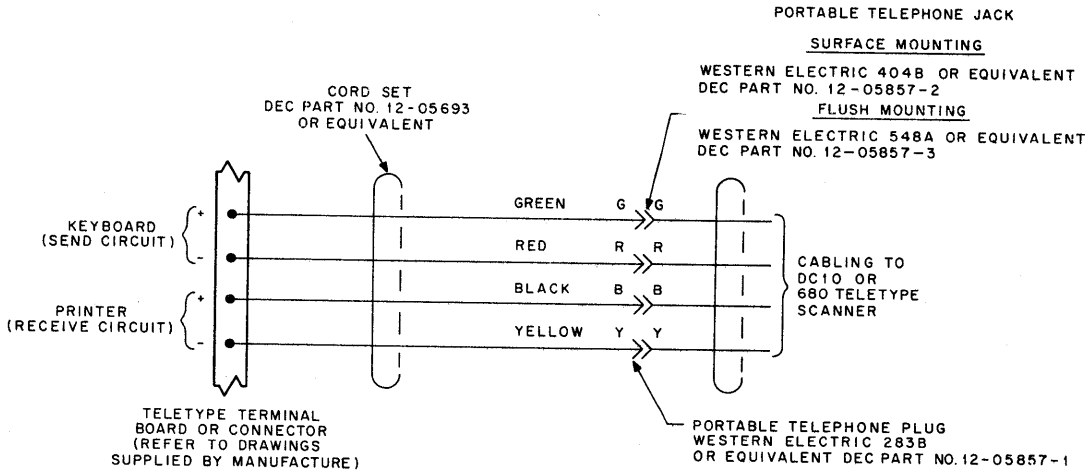


Figure 2A-13 20 mA, Full Duplex Terminals

EIA interface connections (EIA Standard RS-232-B) for Model 37 Teletypes and many other terminals are shown in Figure 2A-14.

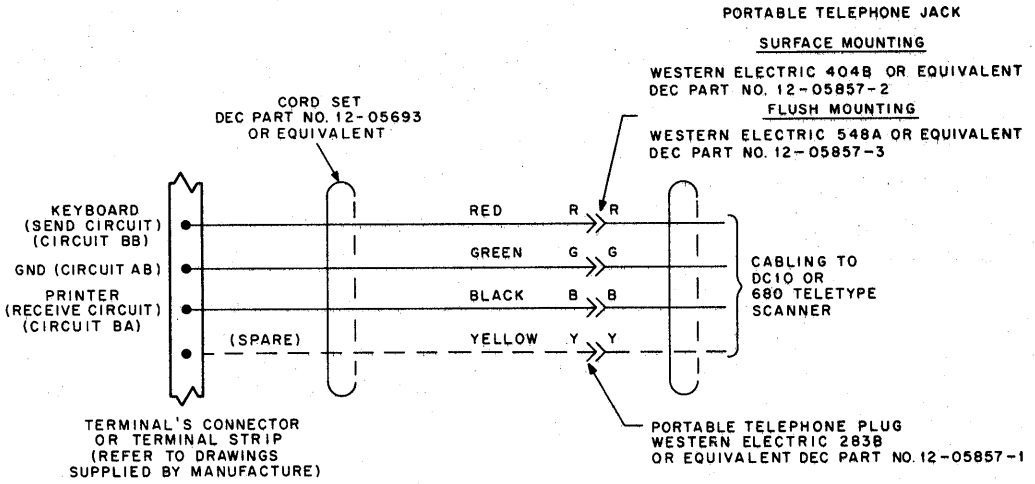


Figure 2A-14 EIA Interface Connections

CHAPTER 3
THEORY OF OPERATION

3.1 BLOCK DIAGRAM ANALYSIS

The major components used in a data line scanner (DLS) system are purchased as options and each system configuration is dependent upon the customer specifications. The one exception to this is the control unit which is required in all systems.

A block diagram of a DLS, Figure 3-1, is provided to support the following function description. The DLS is used to interface a maximum of 64 teletype-like devices with the central processor. Each device (teletypewriter or data-set) is connected to a line group by a data line and the line groups are interfaced with the control unit. Data and command signals are routed between the central processor and the control unit via the I/O bus under program control. During a central processor output instruction (DATAO or CONO), data and/or command signals are routed to the control unit. The control unit generates the required data transfer signals and the data transfer signals route the data to the selected data line via the control unit and the associated line group. When the central processor performs an input instruction (DATAI or CONI), command signals are routed from the central processor to the control unit. In the control unit, the command signals are used to generate the required data transfer signals. After generation, the data transfer signals route the data and/or status signals from the selected data line to the central processor via the associated line group and the control unit.

In the following discussions, a brief functional description of the major DLS components, shown in Figure 3-1, is provided. The system shown in the block diagram should not be considered typical, because each system will vary with the customer requirements.

A DC10A Control Unit is contained in each DLS installation. The control unit provides the necessary interface between the central processor I/O bus and the other major DLS components. The scanning logic in the control unit locates a data line that requires service by scanning the eight line groups sequentially for a data line flag that is set. Upon locating a set flag, the line group is scanned to locate the data line requiring service. The control unit indicates a service requirement to the central processor over the program interrupt line. Then, the data transfer logic, under the control of the central processor, transfers data and/or status signals onto and off of the I/O bus in a parallel fashion. The control unit also enables the central processor to communicate directly with a data line when this is required.

A maximum of eight line groups can be connected to and accommodated by the control unit. Two types of line groups are available: the Eight-Line Group Unit DC10B and the Expanded Data Set Control DC10E. The number of each type of line group will depend upon the system requirements.

The 8-line group unit provides serializing, deserializing and interface level conversions for eight data lines. The speed at which the information on the data lines is serialized and deserialized

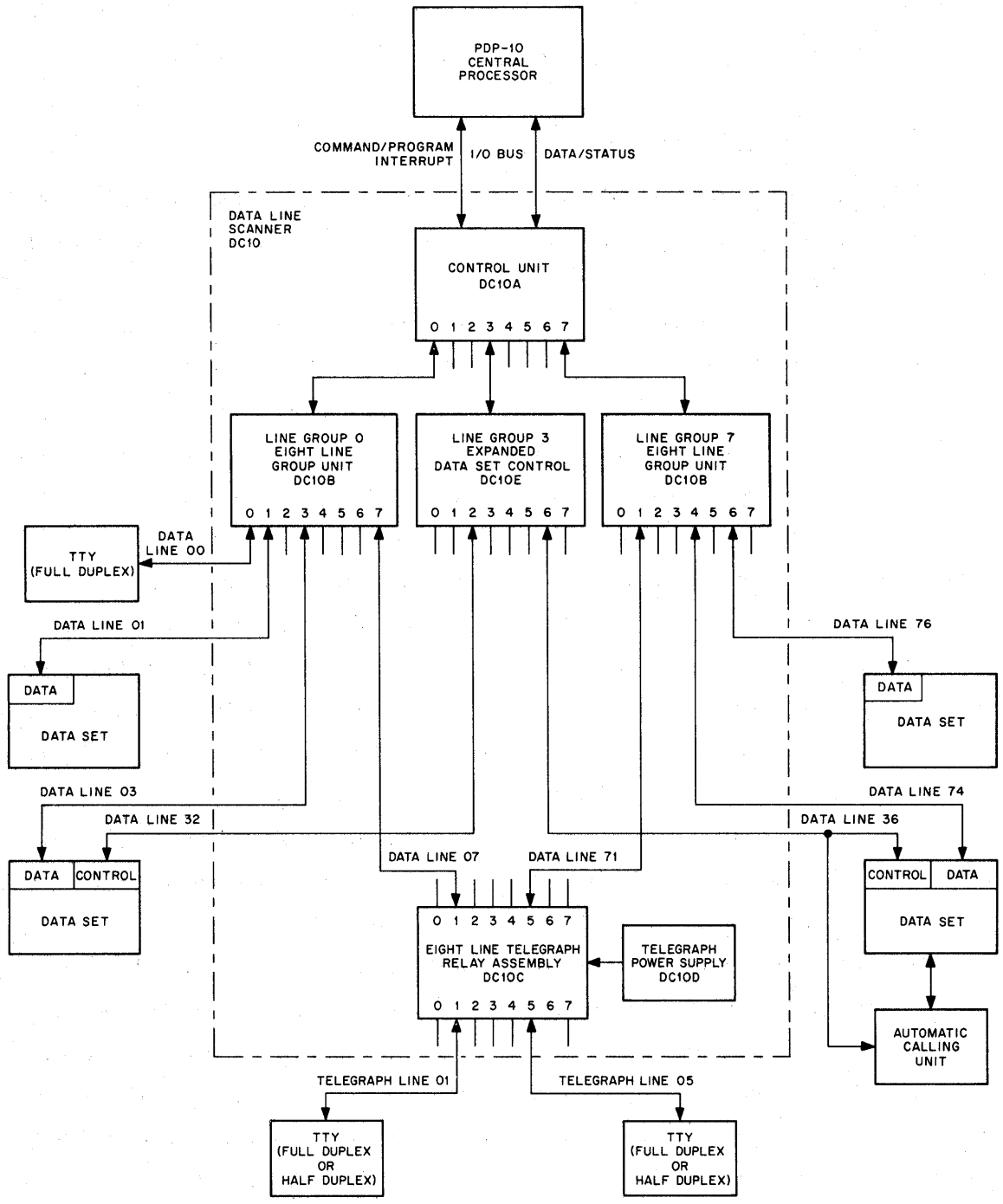


Figure 3-1 A Data Line Scanning Block Diagram

is determined by clocks located in the control unit. Data-sets such as Dataphone, TWX, and Telex apparatus may be interfaced to an 8-line group unit without special equipment. The signaling formats for the data-sets and Model 37 Teletypes are voltage levels conforming to EIA Standard RS-232-B.[1] Teletype Models 28, 33, 35 or similar equipment may be connected to an 8-line group unit if a 20 mA local line operating in full-duplex mode with or without local copy is used. In this case, a local line is defined as a line with a loop resistance of less than 50 ohms (e.g., 300m (1000 ft) of 24 gage cable) and operating in an electrically clean environment.

The expanded data-set control logically replaces an 8-line group unit and provides a control and status interface between the central processor and eight data-sets. Two of these interfaces have provision for automatic calling units. In the DC10E option, the data line carrying control information has a separate line number that is distanct from the data line carrying data. This reduces the number of stations that can be interfaced with the control processor, but it does provide the central processor with additional status information from and operational controls to standard data-sets that are useful in multi-user time sharing systems.

The Eight-Line Telegraph Relay Assembly DC10C provides the relay buffering required to drive a maximum of eight long d-c telegraph lines. These lines can be either 20 mA or 60 mA, polar or neutral circuits, and can be up to 36 km (22 miles) of 24 gage cable. The telegraph relay option limits signaling speed to 300 baud, but provides signals for long lines and/or dirty electrical environments. Half-duplex capability is also provided by this option. As shown in Figure 3-1, the data lines buffered by the telegraph relay assembly do not have to be associated with a single eight-line group unit. By using the various supply voltage inputs, the DC10C can be made to meet the requirements of various telecommunication authorities throughout the world.

The Telegraph Power Supply DC10D is a 125 Vac, 2A power supply that operates 20 mA or 60 mA, neutral data lines in conjunction with the telegraph relay assembly. With this option, 32 relay-buffered 60 mA half-duplexed data lines or 16 relay-buffered 60 mA full-duplex data lines may be operated. For 20 mA data lines, the number of lines that can be operated are 96 and 48, respectively. This option is required by the telegraph relay assembly option.

The last option associated with the data line scanner is the Expander Cabinet DC10F option. This option is not shown in Figure 3-1 but it is required when the total panel mounting space and/or connecting blocks required by a DLS system exceeds the panel mounting space or connecting blocks available in the first cabinet.

3.1.1 Control Unit DC10A

In each DLS system, the control unit provides the necessary interface between the central processor and the DLS. All communication between the central processor and the line units is routed

[1] "Interface between Data Processing Terminal Equipment and Data Communication Equipment"

through and controlled by the control unit. Figure 3-2, a simplified block diagram of the control unit, is used in the following discussion of the control unit interface. To simplify this discussion, the control unit function is explained with only one line group connected. When additional line groups are connected to the control unit, the circuit operation is identical except that each line group is serviced in a sequential fashion.

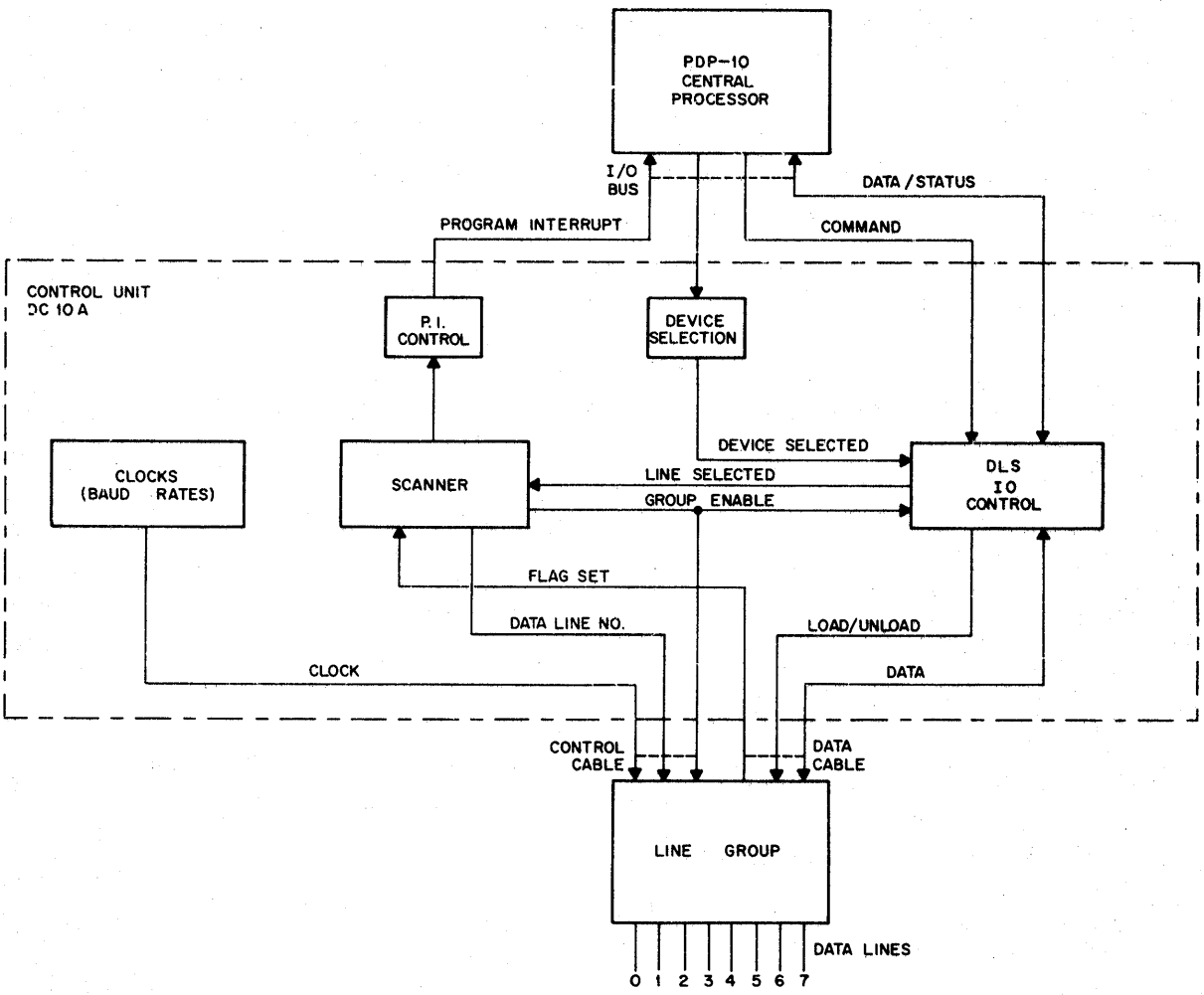


Figure 3-2 Control Unit DC10A Block Diagram

To indicate when a data line requires service, the data line and the line group flags are set. When the scanner scans the flag line of the line group, it locates the line group flag in the set condition and stops scanning the line groups. Then, the scanner scans the data line numbers 0 through 7 in the line group in a sequential fashion. The group enable signal and the active line number are used in

the line group to generate a data line flag strobe signal and the data line is strobed. In this fashion, each data line in the line group is checked for a set flag. When the set flag is located, the scanner stops and causes a program interrupt (PI). The PI signal is routed to the central processor over the I/O bus.

Upon receiving the PI signal, the central processor selects the DLS and sends out a command signal to the control unit. The command signal conditions the DLS I/O control to perform a function. During a CONI instruction, a status word that identifies the type of interrupt that has occurred and the DLS PI channel assignment is routed to the central processor. A DATAI instruction will obtain the interrupting data line number over the I/O bus. If a receiver interrupt has occurred, data from the interrupting data line is transferred to the central processor during the DATAI instruction. If a transmitter interrupt had occurred, the central processor must perform a DATAO instruction to transfer data to the interrupting data line. If both a receiver and a transmitter interrupt have occurred, the receiver interrupt takes precedence.

When the data transfer is complete, the line group flag returns to the cleared condition and the scanner rescans through the line units. When a line group with a set flag is located, the above action is repeated under program control.

A data transfer can be performed under program control even when a line group flag is not set. To accomplish this, the central processor places the data line number, the data and the DLS device number on the I/O bus and sends a DATAO signal to the control unit. The DATAO signal conditions the scanner to select the correct data line through the DLS I/O control. Then, the DLS I/O control loads the data into the register of the selected data line.

3.1.1.1 Scanner Operation - The scanner is used to clock the DLS operation. As explained in the discussion of the control unit, a line group sets a flag when one of its data lines requires service. The scanner monitors the line groups in a sequential fashion until a set flag is located. Then, the scanner scans each data line of the line unit sequentially until the data line with the set flag is located. At this time, the scanner causes a PI signal to be generated. The scanning is inhibited and the PI signal is routed to the central processor over the I/O bus.

The preceding paragraph describes the scanner function in basic terms. Figure 3-3 supports the more detailed explanation of the scanner operation which follows. Timing for the scanner is provided by a 600-ns clock. The SCNR COUNT CLOCK signal is used to increment the 3-stage group counter and the output from the group counter is applied to the group directed data switch. The output signal from the group directed data switch is decoded in the group decoder. In this fashion, the group enable signal for the selected line group is generated and routed to the group scanner control. In the group scanner control, the LSEL GROUP ENABLE signal for the selected line group is ANDed with the COMM SCAN GROUP signal from the selected line group. If the line group flag is not set, the SCNC

COUNT GROUP NO. signal is generated and routed to the group counter. At the same time, the SCNC SCAN and SCNC COUNT UNITS signals are in the false condition and the units counter is not conditioned to be incremented.

The SCNC COUNT GROUP NO. signal enables the group counter, and the SCNR COUNT CLOCK signal increments the group counter. The next line group is checked in the same fashion. This action is repeated until a line group with a set flag is located. At this time, the COMM SCAN GROUP signal from the selected line group is ANDed with its associated group enable signal and the following events occur: the SCNC SCAN signal is generated and routed to the unit scanner control; the SCNC COUNT GROUP NO. goes false and stops the group counter.

At this time, the units counter is set to 0. The output from the units counter is routed to the units directed data switch and the resultant signals from the units directed data switch are routed to the line groups. The LSEL GROUP ENABLE signal for the selected line group enables a line number decoder in the line group and the output signal from the decoder strobes data line 0. If data line 0 does not have a flag set, the SCNC FLAG STROBED signal is not generated and the SCNC COUNT UNITS signal is generated by the unit scanner control. The SCNC COUNT UNITS signal is routed to the units counter and the next SCNR COUNT CLOCK signal increments the units counter. This action is repeated for data lines 1 through 7 until the data line with the set flag is strobed.

When the interrupting data line is strobed, either a COMM TRANS FLAG STROBED signal or a COMM RCVR FLAG STROBED signal is generated in the line group and is routed to the associated flag gate in the scanner. The SCNC FLAG STROBED signal is generated and is ANDed with the SCNC SCAN signal to generate the SCNC SET PI REQ signal. The SCNC SET PI REQ signal is ANDed with the SCNR COUNT CLOCK signal and the resultant signal is used to set the count restart, count hold, and PI REQ flip-flops.

When the count hold flip-flop is set, the following events occur: the SCNR COUNT HOLD (0) signal goes false; the scanner clock control is disabled; the SCNR COUNT CLOCK signal goes false; the scanner counters are disabled; and the interrupting data line number remains in the scanner counters. When the PI REQ flip-flop is set, the SCNR PI REQ (1) signal goes true and enables the PI decoder. The PI channel assignment stored in the PI register is decoded and the resultant PI signal is routed to the central processor via the I/O bus.

The central processor performs the following instructions to service the interrupting data lines: a DATAI instruction to service a receiver interrupt and to identify the interrupting data line number; a DATAO instruction to service a transmitter interrupt after a DATAI has identified the interrupting data line number; or a DATAI instruction first and then a DATAO instruction if both a receiver and transmitter interrupt have occurred.

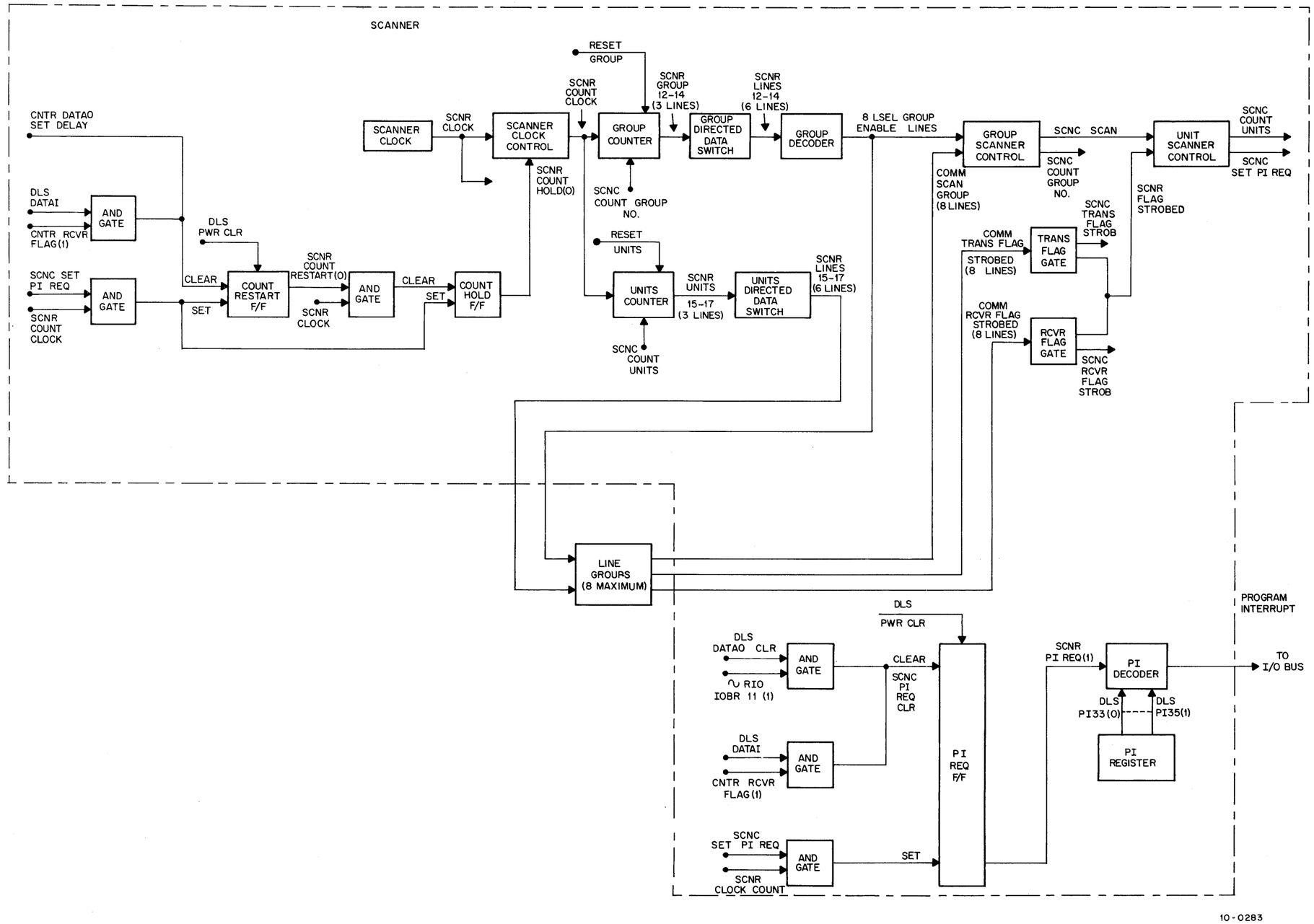


Figure 3-3 Scanner Block Diagram

During the performance of an instruction, the PI REQ flip-flop is cleared in one of the following ways: the DLS DATAO CLR signal is used if the R10 IOBR 11 (1) signal is false during a transmitter interrupt; or the DLS DATAI signal is used if a receiver interrupt was serviced.

After the data line has been serviced, the scanner is restarted. To restart the scanner counters, the following events occur: the count restart flip-flop is cleared by the signal resulting from the ANDing of the trailing edge of the DLS DATAI and the CNTR RCVR FLAG(1) signals or the trailing edge of the CNTR DATAO SET DLY signal; the count hold flip-flop is cleared by ANDing the SCNR COUNT RESTART (0) and the SNCR CLOCK signals; the scanner clock control is enabled; and the SCNR COUNT CLOCK signal is returned to the true condition.

3.1.1.2 Baud Rate Clock Operation - Clock signals are generated to accommodate any 5-level or 8-level teletype code at signaling speeds up to 100 kilobaud. Figure 3-4, the baud rate clock block diagram, shows three clock circuits that are identical except for their frequency. To establish the baud rate, the output signals from clocks 1 and 2, crystal-controlled oscillators, are routed to a divide-by-16 counter and the counter output is connected to a jumper terminal on the W990 Clock Divider Option Card. The output from the clock is also directly connected to another jumper terminal on the option card. When operating between 40 and 999 baud, a jumper is inserted to select the counter output, but when operating between 1 kilobaud and 100 kilobaud, the jumper is moved to select the direct output. An additional feature provides for clock 3 to be routed to the $\div 8$, $\div 4$, and $\div 2$ counter stages as well as the $\div 16$ and the direct $\div 1$ output. In addition, the line speed connections common to groups 0-3 and the separate connections to groups 4-7 allow the use of different speeds in these two sets of groups. Paragraph 2A.2.1 explains these features and provides an example of a typical jumper configuration. The selected frequencies are amplified and routed to the eight-line group units. The three baud rates will be determined by customer specifications, but if the baud rates are not specified, the clock frequencies supplied will establish rates of 110, 150, and 1200 baud.

3.1.1.3 DLS I/O Control Operation - These circuits are used to transfer data and command signals between the central processor and the control unit, under program control. To provide an understanding of the control unit operation, a separate functional block diagram is used to explain the control unit operation during the I/O instructions.

In the following discussions, different instructions are explained in what could be considered a typical sequence. First, the conditioning of the control unit and line groups during the CONO instruction is explained. The transfer of status information from the control unit to the central processor during the CONI instruction is explained next. Following that is an explanation of the transfer of data from the line group to the central processor during a DATAI instruction. The last of the I/O instructions, DATAO, is discussed to explain the transfer of data from the central processor to the line group. The

reset circuit which may or may not be activated under program control and the maintenance circuit which is under manual control are discussed last. Since the selection of the I/O instruction is performed under program control, the actual sequence of selection may vary, but circuit operation will remain the same.

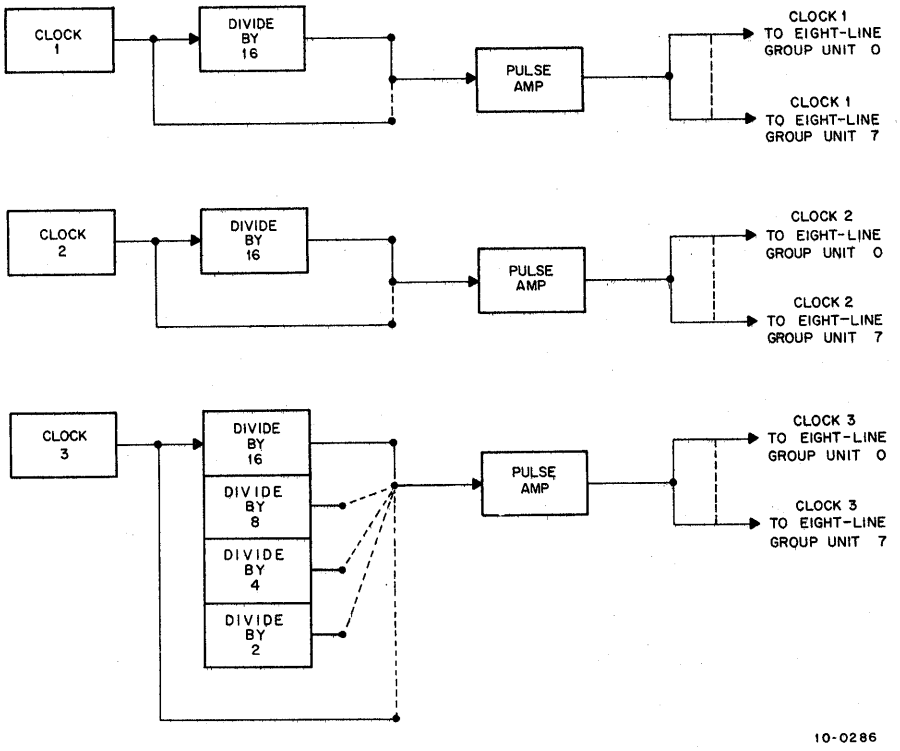


Figure 3-4 Baud Rate Clock Block Diagram

a. CONO Instruction - The CONO instruction is performed to establish known conditions in the DLS. Figure 3-5, CONO instruction block diagram, is used to support the following explanation. The DLS I/O Device number is routed from the central processor to the DLS device decoder over the 14 device selection lines of the I/O bus. The resultant signal from the decoder enables the CONO clear control gate. At the same time, the IOB CONO CLR signal is routed from the central processor to the CONO clear control gate and the DLS PI CLR signal is generated to clear the PI storage register.

The central processor under program control has placed the desired data on I/O bus data lines 30 through 35. The central processor generates the IOB CONO SET signal 1 μs after the IOB CONO CLR signal and routes the IOB CONO SET signal to the CONO set control gate. With the DLS device selected line still active, the DLS CONO SET signal is generated and is used to enable the input data gates. The data on I/O bus data lines 30 through 35 is loaded into the control unit and the following functions are performed:

(1) The PI channel assignment in bits 33 through 35 is loaded into the PI register. The six output lines from the PI register are routed to the PI decoder. When the scanner generates the PI REQ (1) signal, the PI decoder is enabled and the PI channel assignment is decoded. The resultant PI signal is routed to the central processor over the assigned PI line.

(2) When bit 32 = 1, the units counter and group counter in the scanner are reset to 0.

(3) When bit 31 = 1, the data terminal ready one-shot is reset and the resultant signal is routed to the expanded data-set controls. This must be performed every 500 ms to prevent the data-sets from being placed in the on-hook condition.

(4) When bit 30 = 1, a simulated power clear is performed and the DLS control circuits are reset.

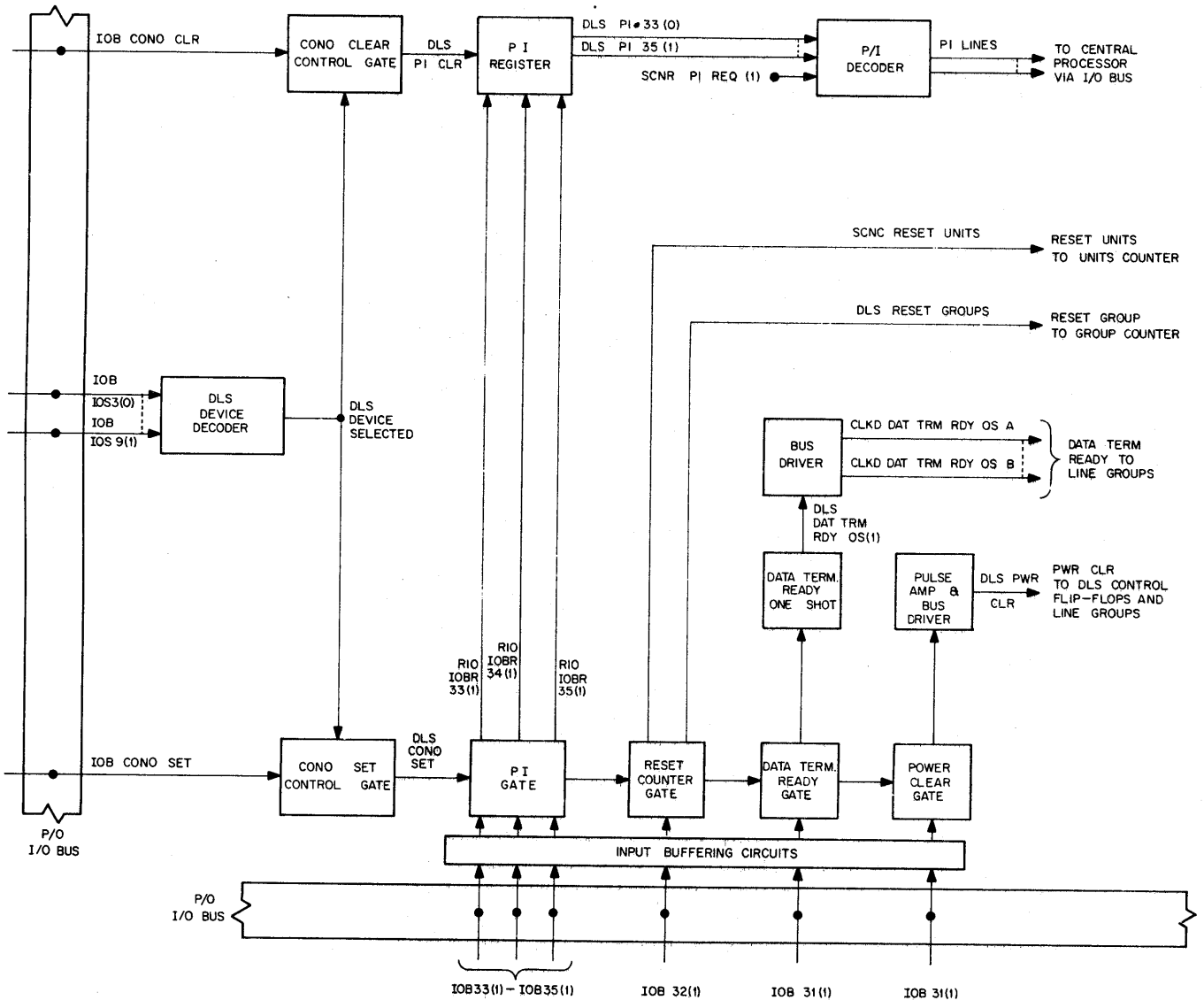


Figure 3-5 Control Unit DC10A Block Diagram - CONO Instruction

b. CONI Instruction - The central processor performs a CONI instruction to obtain DLS status information after a program interrupt has occurred. Referring to Figure 3-6, the CONI block diagram, will assist in understanding the following discussion.

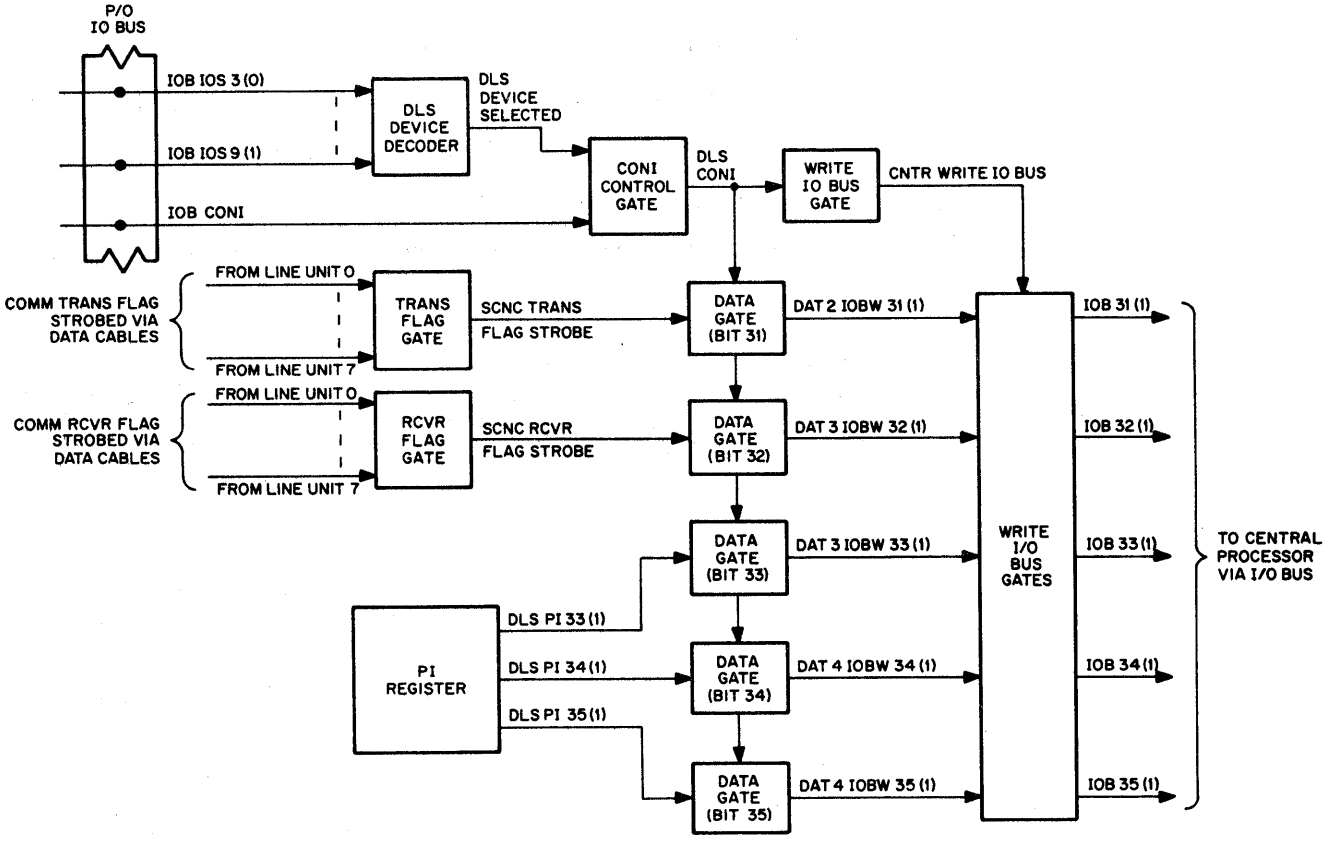


Figure 3-6 Control Unit DC10A Block Diagram - CONI Instruction

To perform a CONI instruction, the central processor generates the DLS I/O device number and the IOB CONI signal and routes them to the control unit via the I/O bus. In the control unit, the DLS device decoder decodes the DLS I/O device number and the resultant signal, DLS DEVICE SELECTED, enables the CONI control gate. The IOB CONI signal is routed to the enabled CONI control gate and the DLS CONI signal is generated. The DLS CONI signal enables the CONI data gates and activates the write I/O bus gate. When the CONI data gates are enabled, the following DLS status information are gated to the write I/O bus gates:

(1) DAT2 IOBW 30(1) is true, if the DTR DIS switch is on.

(2) DAT2 IOBW 31(1) is true, if the interrupting data line has its transmitter flag set.

(3) DAT3 IOBW 32(1) is true, if the interrupting data line has its receiver flag set.

(4) The PI channel assignment number from the PI register.

When the write I/O bus gate is activated, the CNTR WRITE I/O BUS signal is generated and is used to enable the write I/O bus gates. The DLS status information is gated through the enabled write I/O bus gates and is routed to the central processor via the I/O bus.

c. DATAI Instruction - The central processor performs a DATAI instruction to transfer a data word from an 8-line group unit or a status word from an expanded data-set control after a receiver interrupt has been identified during the performance of a CONI instruction. When a transmitter interrupt is identified during the performance of a CONI instruction, a DATAI instruction is performed to transfer the interrupting line number into the central processor. Figure 3-7, the DATAI instruction block diagram, is used to clarify the following circuit descriptions.

When a receiver interrupt is identified, the scanner is stopped to store the interrupting data line number. The number in the group counter is decoded in the group decoder and the resultant group enable signal is used to enable a line decoder in the interrupting line group and to enable the data gates in the control unit that are associated with the interrupting group. At the same time, the number stored in the units counter is routed to and decoded in the line decoder of the interrupting line group. The resultant line enable signal from the line decoder enables the data transfer logic for the interrupting data line.

The central processor routes the IOB DATAI signal to the DATAI control gate and the DLS I/O device number to the DLS device decoder. After the DLS I/O device number is decoded, the DATAI control gate is enabled by the DLS DEVICE SELECTED signal and the DLS DATAI signal is generated. The DLS DATAI signal performs the following functions. It is used to enable the RCVR flag strobed control and then it is ANDed with the resultant signal from the RCVR flag strobed control to generate the CLKD UNLOAD RCVR signal; it is used to enable the data gates in the control unit associated with the DATAI instruction; it is used to generate the CNTR WRITE IO BUS signal; and it is used to enable the RCVR flag AND gate.

The CLKD UNLOAD RCVR signal is routed to the line groups where it becomes the COMM UNLOAD RCVR signal. With the data transfer logic in the line group associated with the interrupting data line enabled by the line enable signal, the COMM UNLOAD RCVR signal gates a data word from an interrupting 8-line group unit or a status word from an interrupting expanded data-set control to the associated data gates in the control unit via the line group data cable. Since the control unit data gates associated with the interrupting line group are enabled by the group enable signal and the DLS DATAI signal, the data word or status word is routed to the write I/O bus gates. At the same time, the resultant signal from the RCVR flag AND gate and the interrupting data line number from the

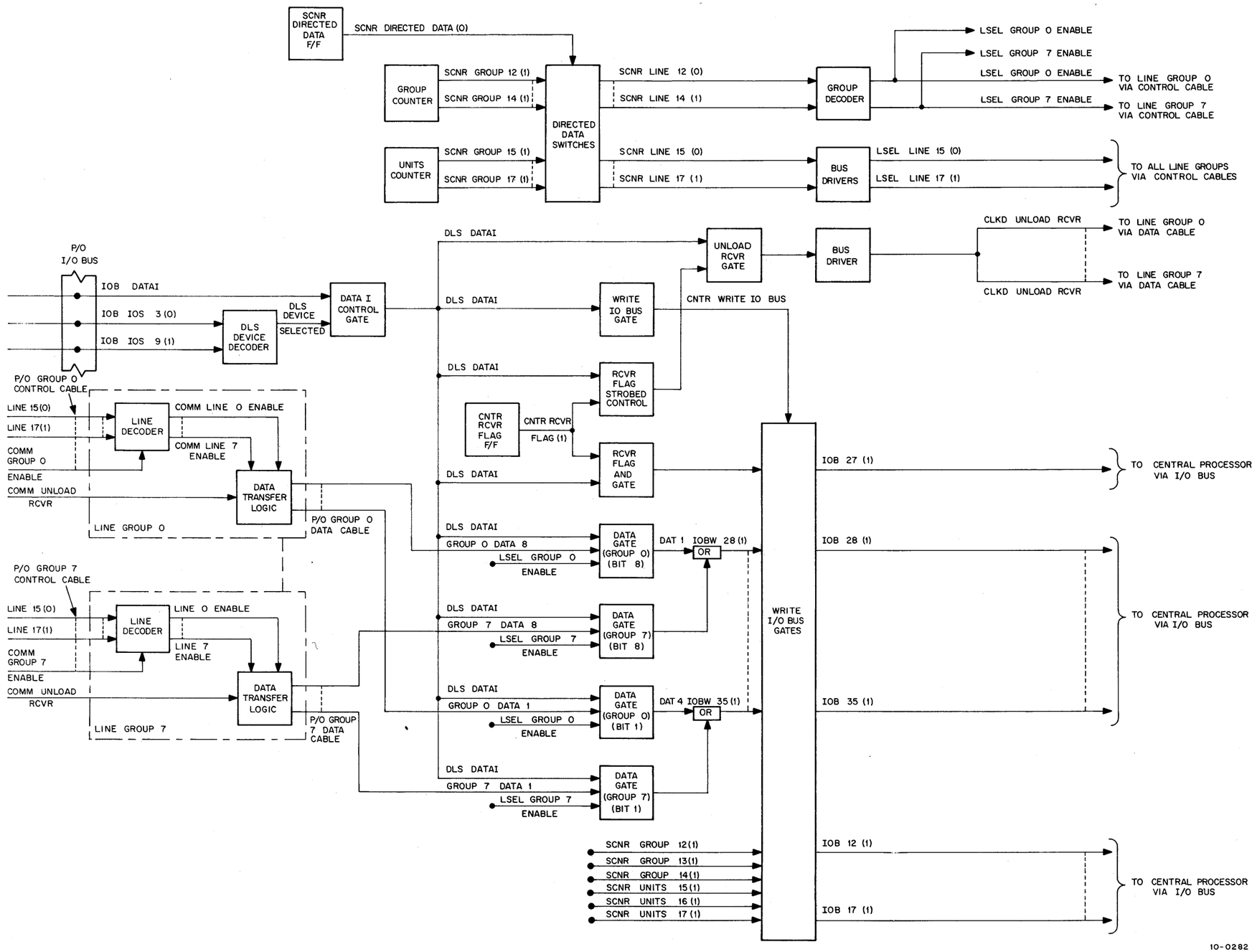


Figure 3-7 Control Unit DC10A, Block Diagram DATAI Instruction

group and unit registers are also routed to the write I/O bus gates. The CNTR WRITE IO BUS signal is used to enable the write I/O bus gates and the data is routed to the central processor via the I/O bus data lines.

The data transferred during a DATAI instruction will depend upon the type of line group that is being addressed. Refer to the programming notes contained in Section 2.4 of this manual for the contents of a data word from an 8-line group unit and the contents of a status word from an expanded data-set control.

When a transmitter interrupt is identified during a CONI, a DATAI is performed to load the interrupting data line number into the central processor. In this case, circuit operation is similar to that explained for the receiver interrupt. The main differences in a DATAI that follows a transmitter interrupt are as follows: the unload RCVR gate is not activated; data are not transferred from the line group; and the RCVR flag strobed control is not enabled because there is no output signal from the RCVR flag strobe gate. Because of these differences, the interrupting data line number is transferred over IOB12 (1) through IOB17 (1) and all other bits are 0.

d. DATAO Instruction - The central processor performs a DATAO instruction to transfer a data word to an 8-line group unit or a control word to an expanded data-set control. These transfers are initiated on a priority interrupt basis after a transmitter flag is detected or when the central processor is directed to initiate a transfer under program control.

The main difference between the two transfers is the way in which the DLS I/O control logic is enabled. When a transmitter flag is detected, the data line number stored in the scanner is used to enable the DLS I/O control logic, but when the central processor initiates a transfer, the data line number is routed from the central processor to the control unit along with the data. Then, this data line number is used to activate the DLS I/O control logic. The last major function performed during a DATAO instruction is the clearing of the transmitter flag after a transfer has been completed.

In the following discussion, a transfer initiated by the central processor is explained first, a transfer when a transmitter flag is detected is explained next, and the clearing of the transmitter flag is explained last. Figure 3-8, the DATAO instruction block diagram, is used to support the following discussions.

When the central processor initiates a transfer under program control, the following information is routed from the central processor to the control unit over the I/O bus. The DLS I/O device number is routed to the DLS device decoder, a 1 in IOB 11 (1) is routed to the directed data set gate, the desired data line number is routed to the directed data switches over data lines IOB 12 (1) through IOB 17 (1), a 0 in IOB 27 (1) is routed to the RIO BIT 27 flip-flop and the data to be transferred are routed to the input data buffering circuit over IOB 28 (1) through IOB 35 (1). At the same time, the IOB DATAO CLR signal is routed to the DATAO clear gate. The DATAO clear gate is enabled by the

DLS DEVICE SELECTED signal from the DLS device decoder and the DLS DATAO CLR signal is generated. The DLS DATAO CLR signal sets the CNTR DATAO and directed data flip-flops. The resultant signal from the set side of the CNTR DATAO flip-flop is used to generate the CNTR DATAO signal and the CNTR DATAO signal is routed to all group trans-enable gates and group data gates. At the same time, the set side of the directed data flip-flop conditions the directed data switches to pass the data line number contained in IOB 12 (1) through IOB 17 (1) and disables the output signals from the group and units counter. The number on SCNR lines 12 (0) through 14 (1) is used to generate the group enable signal for the selected group and the number on SCNR lines 15 (0) through 17 (1) is routed to all line units after passing through the bus drivers. The group enable signal enables the group data gates and the trans-enable gate associated with the selected line group. In the selected line group, the group enable signal enables a line decoder and the line decoder decodes the line number on lines 15 through 17.

The input data is routed in parallel from the input data buffering circuit to all group data gates as RIO IOBR 28 (1) through RIO IOBR 35 (1). Since the data gates associated with the selected line group are enabled by the group enable signal and the CNTR DATAO signal, the data on RIO IOBR 28 (1) through RIO IOBR 35 (1) are routed to the selected line group via the data cable. With IOB 27 (1) a 0, the RIO bit 27 flip-flop remains in the cleared condition and the RIO bit 27 (0) remains true. The trans-enable gate associated with the selected line group is enabled and the trans-enable signal is routed to the line group.

In reviewing the conditions up to this point, it is found that the selected data line is enabled, the trans-enable signal is routed to the selected line group, and the data are routed to the selected line group. Under these conditions, the selected line unit is conditioned to accept the transfer.

The transfer is completed in the following manner. The central processor generates the IOB DATAO SET signal 1-μs after the IOB DATAO CLR signal, and the IOB DATAO SET signal is routed to the DATAO SET gate. The resultant signal from the DATAO SET gate, DLS DATAO SET or ECHO, is used to generate the CLKD LOAD TRANS signal. The CLKD LOAD TRANS signal is routed to the line groups and is used to strobe the data into the transmitter buffer of the selected line group. After an 85-ns delay, the trailing edge of the resultant signal from the delay circuit clears the CNTR DATAO and directed data flip-flops. This disables the data gates and returns the data line selection to the group and units counters.

To perform a transfer after a transmitter flag has been detected, a similar procedure is followed except, in this case, IOB 11 (1) is 0 and IOB 12 (1) through IOB 17 (1) are not used. With IOB 11 (1) a 0, the directed data set gate is inhibited, the directed data flip-flop is not set by the DLS DATAO CLR signal and the interrupting data line number stored in the group and units counters is

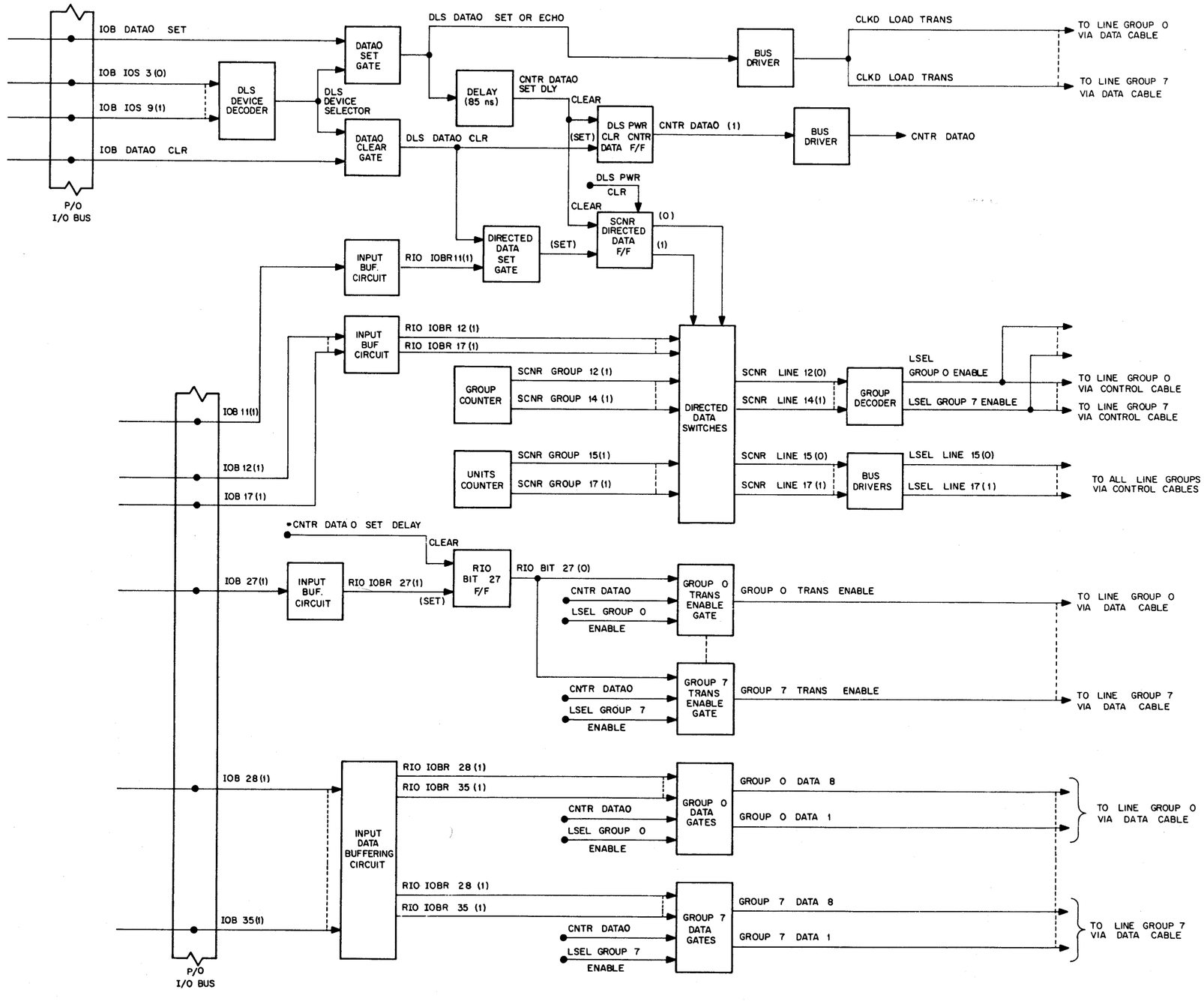


Figure 3-8 Control Unit DC10A, Block Diagram DATAO Instruction

routed through the directed data switches. This data line number is used to generate the group enable signal and the data line number. The remainder of this transfer is identical to a transfer initiated by the central processor under program control.

The last function that can be performed during a DATAO instruction is the clearing of a transmitter flag without transferring additional data. This function is performed after all the required data have been transferred. The manner in which this function is performed is similar to a transfer performed after a transmitter flag is detected. The main differences between the two transfers are as follows. No data are transferred over IOB 28 (1) through IOB 35 (1) and IOB 27 (1) is 1. The interrupting line number stored in the group and units counter is used to generate the group enable signal and the data line number. These signals condition the transfer circuit associated with the interrupting data line in the line group. With IOB 27 (1) a 1, the RIO BIT 27 flip-flop is set and the RIO BIT 27 (0) signal is false. With RIO BIT 27 (0) signal false, the trans-enable gate for the interrupting line is not enabled and the trans-enable signal is not generated. When the CLKD LOAD TRANS signal is generated, the data lines in the line group are strobed and the transmitter flag associated with the interrupting data line is cleared.

In the DATAO instruction, the information contained on data lines 28 through 35 will depend upon the type of line unit the central processor is addressing. Refer to the programming notes contained in Section 2.4 of this manual for the contents of this transfer.

e. Reset Circuit - The reset circuit is used to clear the DLS control circuits and is activated in three different ways. This circuit is activated to establish a known operation condition. Refer to Figure 3-9 for the following functional description.

The first method of activating the reset circuit to be discussed occurs when the DLS power is turned-on or turned-off or when the maintenance switch is turned-on or turned-off due to contact bounce. When either happens, the DLS PWR ON (1) signal from the DLS power-on one-shot is true and is applied to the power reset OR gate. The resultant signal, DLS PWR CLR, from the power reset OR gate is routed to the DLS control circuit.

The central processor can initiate a power clear in two ways. The central processor can perform a CONI instruction to the DLS with a 1 in bit 30 of the I/O data word. The DLS CONO SET and RIO IOBR 30 (1) signals are routed to the power clear gate and the resultant signal is used to generate the DLS PWR CLR signal; or it can generate the IOB RESET signal in any of several ways and route this signal to the reset gate. The resultant signal from the reset gate, DLS IOB RESET, is used to generate the DLS PWR CLR signal.

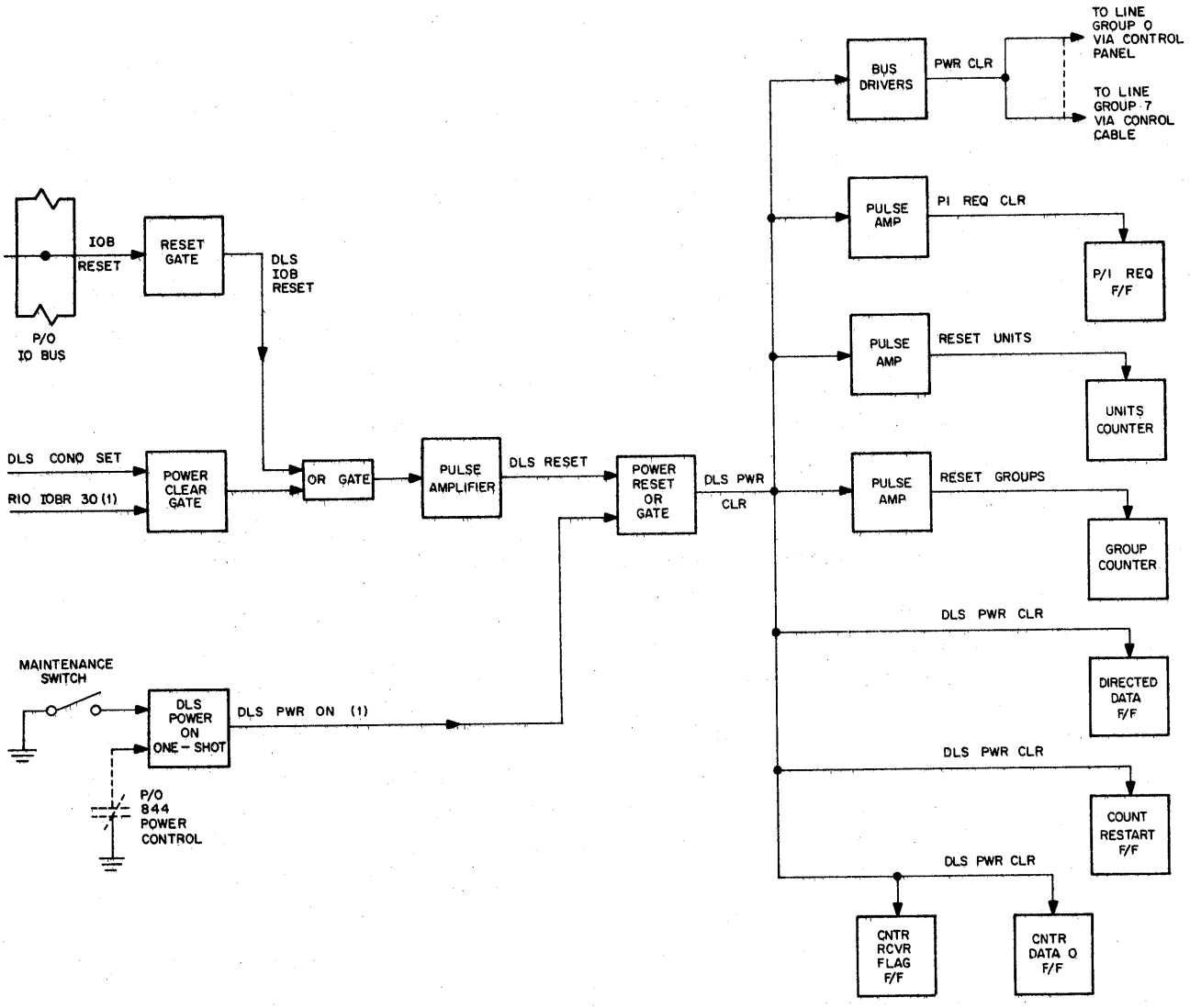


Figure 3-9 Data Line Scanner Reset Circuit

f. Maintenance Circuit - The maintenance circuit of the DLS consists of an echo control circuit and an indicator circuit that can be used by maintenance personnel to check system operation. The indicator circuit provides a quick check of system operation at all times and the echo control circuit provides an indication of the DLS I/O control operation for any full-duplex data line when the maintenance mode is selected.

(1) Indicator Circuit - The indicator circuit consists of an indicator panel, two rotary switches, and control logic shown in Figure 3-10.

Since the duration of the strobe signal from either the transmitter flag OR gate or receiver flag OR gate is short, the power available to illuminate an indicator is low. To provide a better indication, the indicator circuit provides the means to increase the available illuminating power on a selected line basis. The data line number is selected

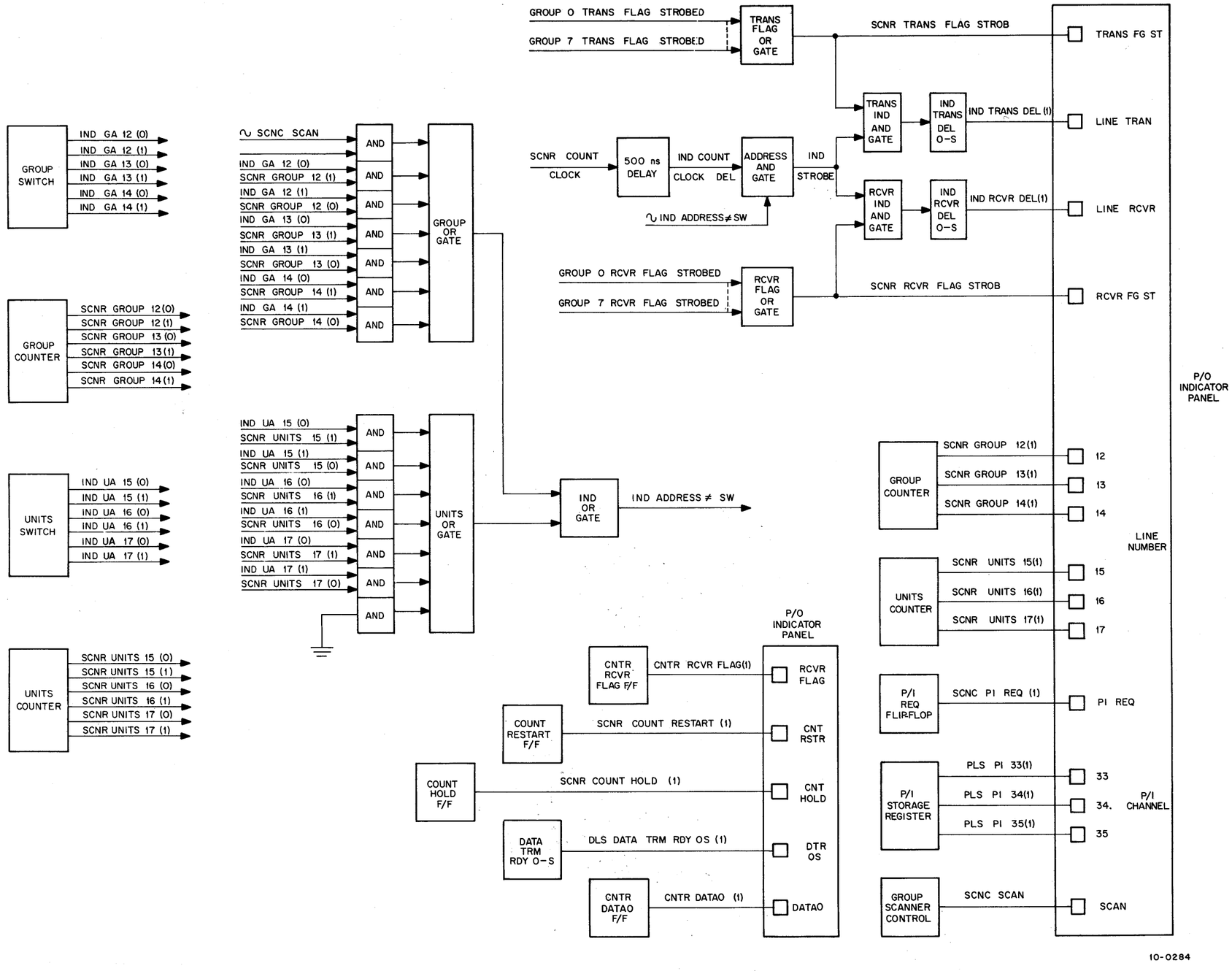


Figure 3-10 Indicator Circuit

by using the group and units switches on the indicator panel while the group and units counters in the scanner continue to scan through the groups. Each output line from the group switch is ANDed with a complementary signal line from the group counter and each output line from the units switch is ANDed in a similar fashion with lines from the units counter. The group AND gates are ORed together and the units AND gates are ORed together. Then, the resultant signals from the two OR gates are ORed in the IND OR gate. The resultant signal from the IND OR gate, IND ADDRESS $\neq$ SW, is true until the group and units counters reach the data line number that is set into the group and units switches and a data line flag associated with the selected data line is in the set condition. At this time, the $\sim$IND ADDRESS $\neq$ SW signal is true and is used to enable the address gate. The SCNR COUNT CLOCK signal from the scanner clock control is used to start a 500 ns delay. After the delay time, the resultant signal from the delay, IND COUNT CLOCK DEL, is true and is routed to enabled address AND gate. The output signal from the address AND gate is amplified in a pulse amplifier and the resultant signal from the pulse amplifier is used to enable the TRANS and RCVR IND AND gates.

Since circuit operation for either the transmitter or receiver circuit is identical, the remaining description is written in general terms and is intended to apply to either circuit. The strobed line from the selected line group is applied to a flag OR gate and the resultant signal from the flag OR gate is routed to the enabled IND AND gate. The resultant signal from the enabled IND AND gate starts a one-shot to effectively stretch the strobe signal and the set side of the one-shot illuminates the appropriate line indicator.

The remaining indicators provide an indication of the DLS operation. When any data line flag in any line group is set, the [TRAN FG ST] and, or [RCVR FG ST] indicator(s) are illuminated. As the scanner scans the data lines, the data line number is displayed in indicators [12] through [17]. The octal group number is displayed in the three left-hand indicators and the data line within the selected group is displayed in the three right-hand indicators. To indicate the assigned PI channel number, the set side from the three flip-flops in the PI register is routed to indicators [33] through [35]. The [SCAN] indicator is illuminated whenever a data line flag is set and the scan group line from one of the groups is active. The remaining indicators are used to provide an indication of when their associated flip-flops are in the set condition.

(2) Echo Circuit - The echo circuit shown in Figure 3-11 is used to check the I/O control for any full-duplex line. To activate the echo circuit, select the maintenance mode by turning on the MAINT switch and strike a character on the teletype keyboard.

The character is loaded into the teletype receiver circuit in a serial fashion via the serial input line and after the character is loaded, the receiver flag is set. When the scanner generates the selected group enable signal and the selected line number, the selected line enable signal is generated by the line decoder. The selected line enable signal strobes the teletype receiver circuit and the receiver flag strobed line is activated. The active receiver flag strobed line conditions the RCVR flag OR gate and the SCNC RCVR FLAG STROB signal is generated and routed to the RCVR AND gate. In the RCVR AND gate, the IND MAINT signal is ANDed with the SCNC RCVR FLAG STROB signal and the resultant signal is amplified and inverted to generate the IND ECHO signal. The IND ECHO signal is used to condition the following gates: the unload RCVR gate that generates the CLKD UNLOAD RCVR signal; the TRANS enable gate that generates the TRANS ENABLE signal; and the load TRANS gate that generates the CLKD LOAD TRANS signal. The CLKD UNLOAD RCVR signal gates the teletype character out of the teletype receiver circuit and onto the data lines in a parallel fashion. At the same time, the CLKD LOAD TRANS signal gates the teletype character from the data lines into the teletype transmitter circuit. The TRANS ENABLE signal conditions the serial transfer circuit in the teletype transmitter circuit and the teletype character is echoed to the printer in serial fashion via the serial output line.

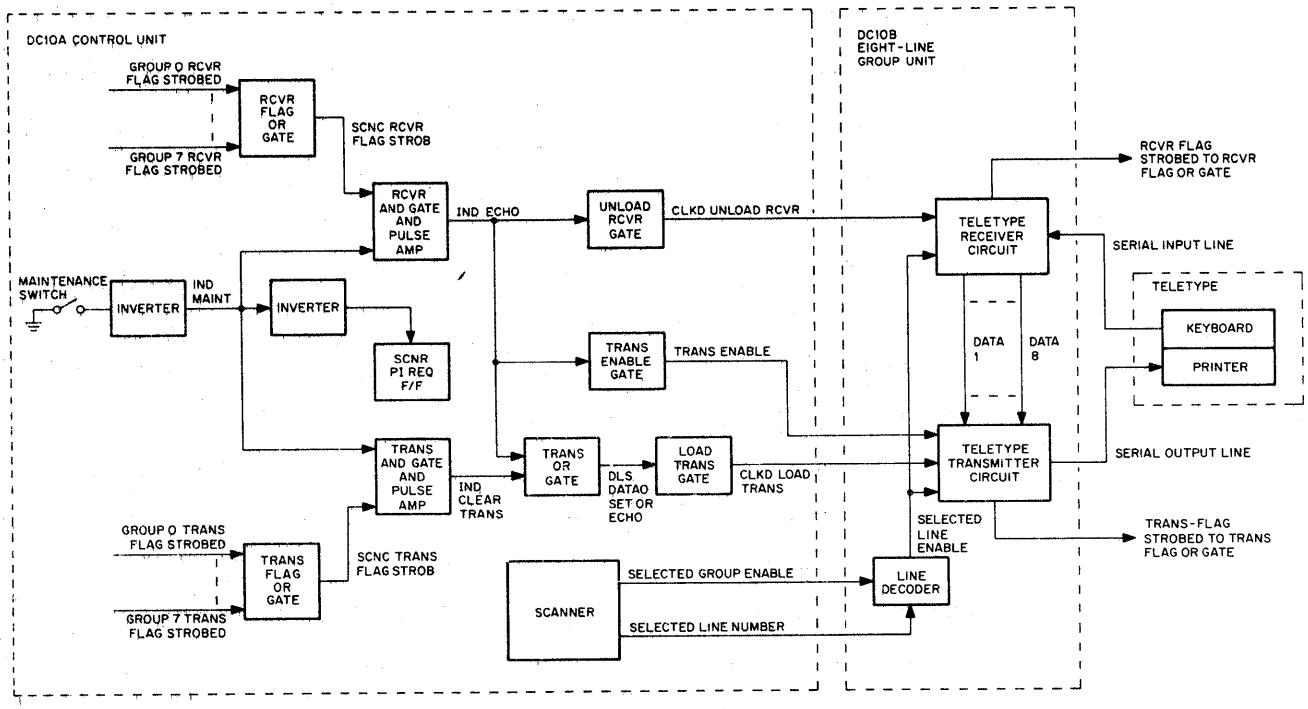


Figure 3-11 Echo Circuit

After completing the serial transfer, the teletype transmitter circuit sets its transmitter flag. Then, when the scanner strobes the selected teletype transmitter circuit, the transmitter flag strobe line is activated. The active transmitter flag strobed line conditions the TRANS flag OR gate to generate the SCNC TRANS FLAG STROB signal. In the TRANS AND gate, the IND MAINT signal and the SCNC TRANS FLAG STROB signal are ANDed to generate the IND CLEAR TRANS signal. The IND CLEAR TRANS signal is routed through the TRANS OR gate and the resultant signal, DLS DATAO SET OR ECHO is used to generate the CLKD LOAD TRANS signal. When the CLKD LOAD TRANS signal is applied to the teletype transmitter circuit, the transmitter flag is reset and the echo circuit is ready to receive another character from the teletype keyboard.

When maintenance mode is selected, the IND MAINT signal is used to inhibit the DLS device decoder and to maintain the PI REQ flip-flop in the clear condition. This prevents the central processor from selecting the DLS, and the DLS from initiating a program interrupt during maintenance operation.

3.1.2 Eight-Line Group Unit DC10B

The 8-line group unit is one of two line groups connected to the control unit. Each 8-line group unit provides eight identical two-way communication paths between the central processor and a maximum of eight Teletype machines or data-sets. Control signals for the 8-line group units are generated in the control unit under program control, and data in both the receive and transmit circuits are routed through the control unit. The receive circuit receives data from the keyboard and transmits the data to the central processor. In the transmit circuit, data are received from the central processor and are transmitted to the printer. As explained in Section 3.1, data-sets and/or Teletype machines connected in full-duplex over a local line may be interfaced directly to an 8-line group unit.

Since the control unit provides the interface between the central processor and 8-line group unit, a thorough understanding of control unit operation is required to understand the following 8-line group unit functional description. In this discussion, the receive circuit is described first, this is followed by the functional description of the transmit circuit.

a. Receive Circuit - The receive circuit provides the serial to parallel conversion, buffering, gating and synchronizing necessary to interface eight asynchronous-serial teletype lines with the central processor. Each line within the receive circuit is conditioned to assemble either a 5-bit serial character with a unit code length of 7.0, 7.5 or 8.0 units or an 8-bit serial character with a unit code length of 10.0, 10.5 or 11.0 units. As the teletype character is received in serial form, the character is assembled into parallel form. When the conversion is completed, the character is transferred in parallel form to the central processor via the control unit. This transfer is completed on a priority interrupt basis and under program control.

Figure 3-12, the receive circuit block diagram, is used to support the following functional description. The outputs from the three baud-rate clocks are routed to the clock line option card from the control unit. At the clock line option card, a series of jumpers are used to select a clock frequency that is eight-times the desired baud rate. From the clock line option card, the selected clock output is routed to the line clock associated with each module.

Since the circuit operation of each line is similar, the following functional discussion pertains to any one of the eight receive lines. The incoming signal from the keyboard is routed to the teletype receiver module via the serial input line. When a data-set or Model 37 Teletype is connected to a line unit, the EIA-DEC interface module is used for level conversion.

The serial input from the keyboard is monitored for the start element of an incoming character. When a start element is detected, a clock enable signal is routed to the line clock and the clock output is routed to the teletype receiver module to clock the incoming signal. Since the unit code length of an incoming signal can vary with different devices, a set of jumpers on each receiver module is used to adapt the module to the unit code length of the associated device.

As the serial bits of the character are received, they are loaded into the buffer register of the receiver module. When the last bit of the character is loaded, the receiver module flag is set and the COMM SCAN GROUP signal is routed to the control. As explained in the discussion of the scanner, the COMM SCAN GROUP signal causes the scanner to stop the group counter. The unit counter is started and line numbers 0 through 7 are routed to the line decoder in a sequential fashion along with the group enable signal. As the line numbers are decoded, a line enable signal is generated and routed to the associated flag strobe line. When the module with the set flag is strobed, the COMM RCVR FLAG STROBED signal is generated and routed to the control unit. The COMM RCVR FLAG STROBED signal stops the units counter and causes a PI signal to be generated and routed to the central processor.

At this time, the central processor program performs a CONI instruction and the control unit relays a receiver interrupt and the interrupting line number to the central processor. The receiver interrupt indicates that a teletype receiver module is loaded and ready to transfer a character; the interrupting line number indicates which data line is causing the interrupt. To unload the character, the central processor performs a DATAI instruction under program control. During the DATAI instruction, the control unit is conditioned to generate the COMM UNLOAD RCVR signal. Since the buffer/flag gate is enabled by the COMM LINE n ENABLE signal, the read buffer and clear flag lines are activated by the COMM UNLOAD RCVR signal. The read buffer line reads the character onto the data lines in parallel form and the clear flag line clears the receiver flag of the module. The character is routed

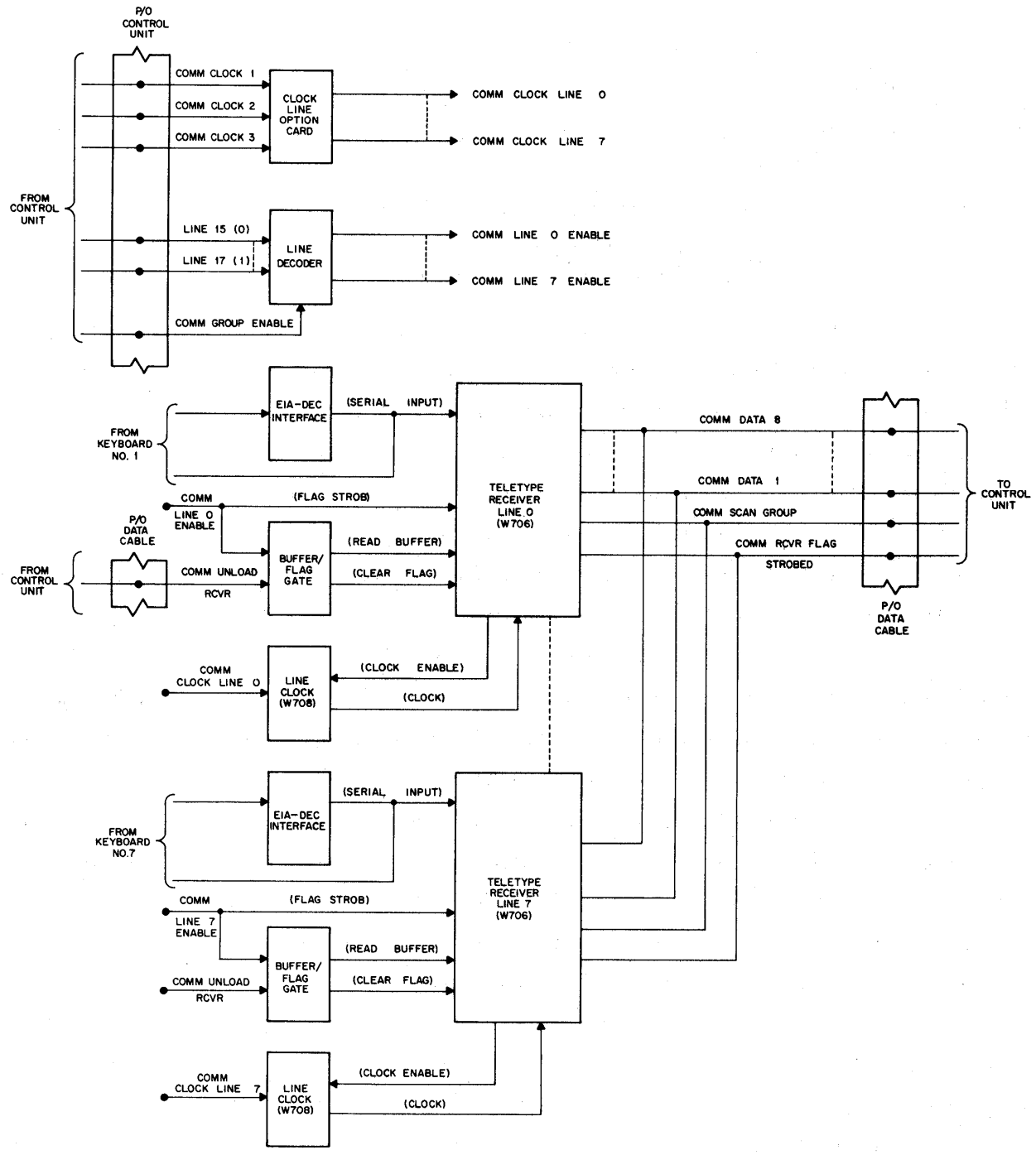


Figure 3-12 Eight-Line Group Unit DC10B - Receive Circuit

to the central processor via the control unit and the COMM SCAN GROUP signal goes to the false condition. At this time, the teletype receiver module is ready to receive another character from the device, without garbling the previous character, and the scanner is freed to scan the line units.

To avoid garbling the next incoming character, the character in the buffer register, must be transferred to the central processor within a time, T_r, where

$$T_r = \frac{\text{Number of stop units} + 1/2}{\text{Speed (baud or units (bits) per second)}} \text{ seconds}$$

b. Transmit Circuit - The transmit circuit provides the parallel to serial conversion, buffering, gating, and timing necessary to interface the central processor with eight asynchronous-serial teletype lines. Each line within the transmit circuit is conditioned to accept either a 5-bit or an 8-bit parallel character through the use of a series of jumpers located on the teletype transmitter module. The 5-bit character is assembled into a serial character with a unit code length of 7.0, 7.5 or 8.0 units and the 8-bit character is assembled into a serial character with a unit code length of 10.0, 10.5 or 11.0 units. A series of jumpers located on the transmitter modules is used to establish a unit code length that is identical to the unit code time base of the associated device.

A parallel character is transferred to the teletype transmitter module from the central processor via the control unit under program control during a DATAO. After receiving the character, the teletype module transfers the character to the printer of the associated device in a serial fashion and generates the start and stop signals at the required times.

The transmit circuit block diagram, Figure 3-13, is used to support the following functional description. The baud rate is selected by selecting the desired clock frequency at the clock line option card and is routed to the line clock as it was in the receive circuit. The data cable, the control cable, the clock patch, the line decoder, and the line clocks associated with each transmitter module are common to the items shown on the receive circuit block diagram.

Since a character is transferred to the teletype transmitter module during a DATAO instruction, a brief review of the DATAO instruction follows. The three main functions that can be performed under program control during DATAO instruction are as follows: the transfer of a character to a data line that is selected by the program; the transfer of a character to an interrupting data line; and the clearing of an interrupting transmitter flag. The transmit circuit operation is identical during the first two functions, so they are discussed first. Then, the transmit circuit operation during the third function is explained.

The data line number and the COMM GROUP ENABLE signals are routed to the line decoder. After the line number is decoded, the resultant line enable signal is routed to the buffer/flag gate associated with the selected data line. At the same time, the parallel character on lines COMM DATA 1 through COMM DATA 8 and the COMM TRANS ENABLE signal is routed from the control unit to the teletype transmitter modules.

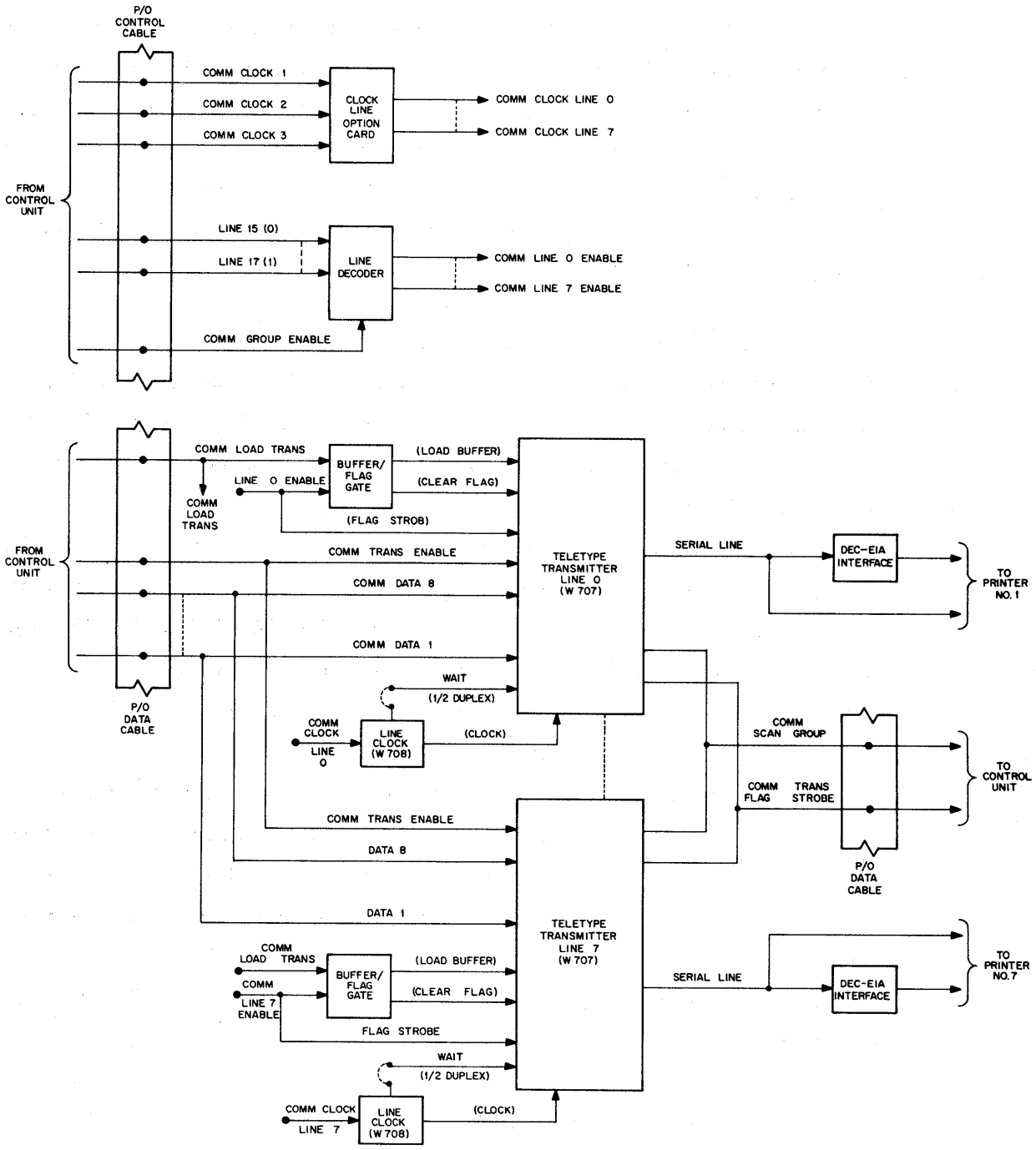


Figure 3-13 Eight-Line Group Unit DC10B - Transmit Circuit

The COMM LOAD TRANS signal is generated in the control unit 1 μs later and is routed to all teletype transmitter modules. When the COMM LOAD TRANS signal is applied to the enabled buffer/flag gate, the load buffer and the clear flag lines to the associated transmitter module are activated. The active load buffer line loads the character into a buffer register in a parallel fashion and the active clear flag line clears the transmitter flag. With the COMM TRANS ENABLE signal present at the module input, the active load buffer line also conditions the serial transfer circuit. To maintain maximum speed, a second character must be loaded within a time, T_t, where

$$T_t = \frac{\text{Number of stop units} - 1/2}{\text{Speed (baud or units (bits) per second)}} \text{ seconds}$$

When the data line is connected in half-duplex, a delay in the serial transfer is encountered if the teletype receiver module associated with the same data line is receiving a character. When this condition occurs, the transmitter module does not start its serial transfer until the transfer to the teletype receiver module is completed.

When the serial transfer is performed, the characters, including the start and stop signals, are transferred to the printer of the associated device in serial fashion. One half unit after the first stop unit is put on the serial line, the transmitter module flag is set. The COMM SCAN GROUP signal to the control unit goes to the true condition. The scanner strobes each data line in the interrupting group until the set flag is located, as explained in the receive circuit description. Upon locating a set flag, the scanner stops and a PI signal is routed to the central processor.

If the central processor has another character for this data line, it sends the character to the teletype transmitter module under program control, as explained above. When all characters have been transferred, the central processor performs a DATAO instruction to clear the transmitter flag. During this DATAO instruction, the COMM TRANS ENABLE signal goes false when the central processor routes an I/O data word to the control unit with a 1 in IOB 27 (1). With the COMM TRANS ENABLE signal false, the transmitter flag is cleared when the clear flag line is activated but additional data are not sent out over the serial line.

3.1.3 Eight-Line Telegraph Relay Assembly DC10C

This assembly provides relay buffering for eight independent telegraph lines. With this assembly, teletype machines can be operated over long dc telegraph lines and/or in dirty electrical environments. Half-duplex capability is allowed with this option, but signaling speed is limited to 300 baud. The eight data lines buffered by this assembly do not have to be operated at an identical speed or associated with a single 8-line group unit.

Refer to Figure 3-14 for the following circuit description. Each of the eight telegraph circuits in the DC10C provides a two-way interface between a Teletype and a data line in an 8-line group

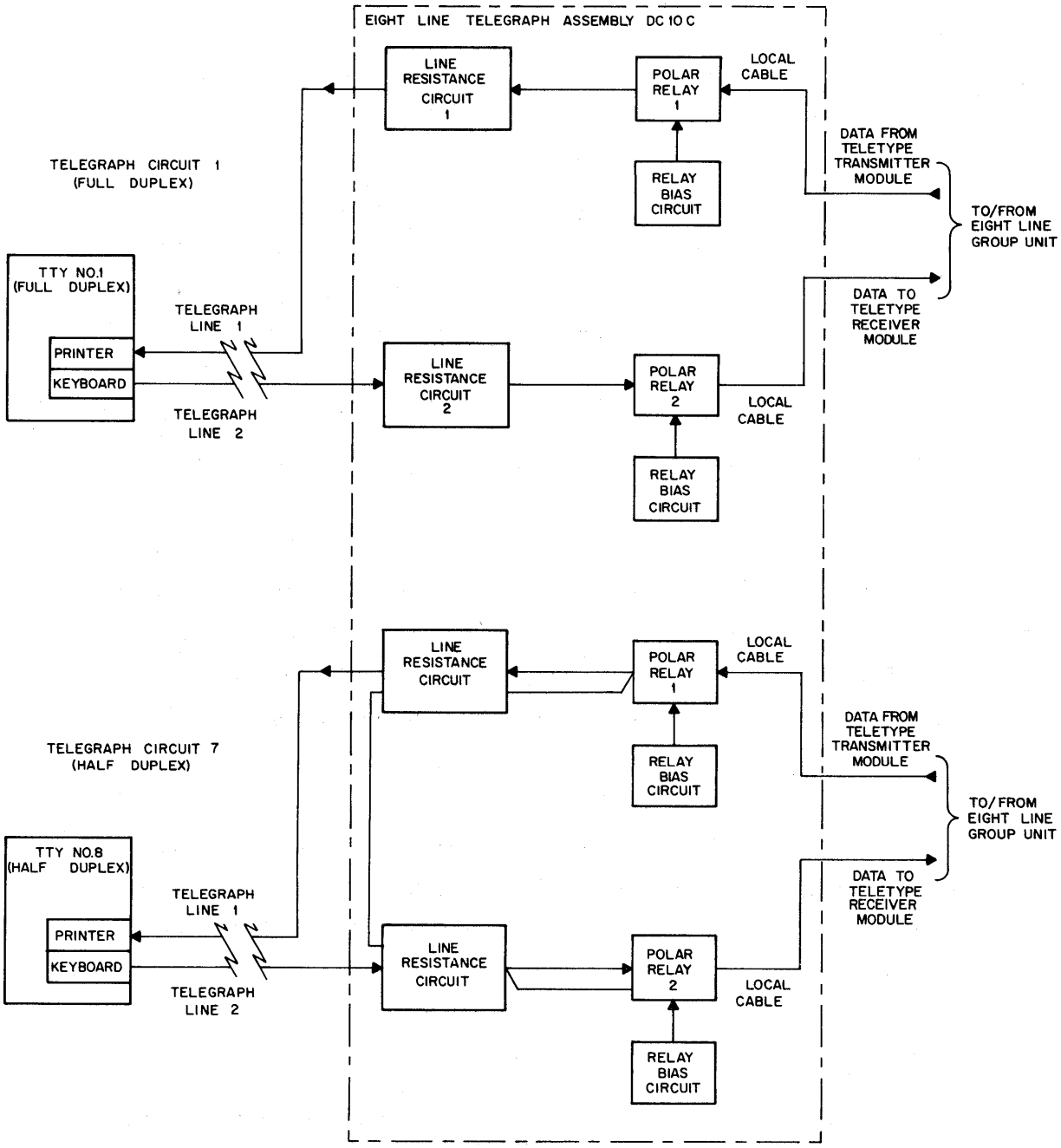


Figure 3-14 Eight-Line Telegraph Relay Assembly DC10C - Block Diagram

unit. The telegraph lines can be operated at current levels from 20 mA to 100 mA and can be operated in either the polar or neutral mode. Under most conditions, a telegraph line can be as long as 36 km (22 miles) of 24 gage cable.

Since each telegraph circuit is identical, a discussion of a typical telegraph circuit is provided. In this typical circuit, Telegraph line 2 connects the keyboard of a Teletype to polar relay 2 via line resistance circuit 2. Then, a local cable connects polar relay 2 to a receiver module in an 8-line group unit. A local cable connects the associated transmitter module in the 8-line group unit to polar relay 1. The output from polar relay 1 is routed through line resistance circuit 1 and to the te teletype printer via telegraph line 1.

Each polar relay is provided with a relay bias circuit. The relay bias circuit provides a high impedance bias current which sets the operating point for the low resistance polar relay. The bias current to the polar relay is adjustable over a range of 3.5 to 60 mA. The bias voltage across the polar relay may be as large as 4V, to allow for transient voltage swings caused by relay operation, without cutting off the bias circuit. The bias current to the polar relay is normally set to one-half of the relay signal current and this nominal current value is adjusted to correct for signal distortion.

The line resistance consists of an adjustable resistor used to control the current in the telegraph line by adjusting the total circuit resistance to the required value. For example, a 60 mA circuit with a 120V power supply requires a total circuit resistance of 2000 ohms. If the line resistance is 500 ohms, the line resistance circuit is adjusted to 1500 ohms.

The DC10C also provides half-duplex capability. In this mode, telegraph line 1 and telegraph line 2 are connected together at the Teletype and at the line resistance circuits. In half-duplex mode, circuit operation is similar to full-duplex except only one telegraph line can be used at one time without garbling the transmission.

3.1.4 Telegraph Power Supply DC10D

The telegraph power supply is a 125 Vdc, 2 A power supply used in conjunction with the 8-line telegraph relay assembly option. Each supply is capable of driving 32 relay-buffered 60 mA half-duplex lines or 16 relay-buffered 60 mA full-duplex lines operated in the neutral mode. If 20 mA lines are used, the supply is capable of driving 96 lines in half-duplex and 48 lines in full-duplex.

The following discussion is supported by Figure 3-15. An input voltage with a nominal range between 100 and 130 Vac for the DC10D-A or between 200 and 260 Vac for the DC10D-B is applied to a constant voltage transformer. Due to a unique design, the transformer maintains the voltage applied to the rectifier at a constant over the nominal range of the input line voltage. In this way, the output voltage is regulated to ± 1 percent for nominal input voltage and full load. From the transformer, the regulated voltage is rectified by a full-wave bridge rectifier and applied to an RC filter network. The

filter network keeps the output ripple to less than 1 percent under full load conditions, if the input voltage is within the nominal limits. Besides voltage regulation, the transformer also provides short-circuit protection for the supply. When a short-circuit occurs, the output voltage is reduced toward zero and the short-circuit current is limited to approximately 150 percent of full load current.

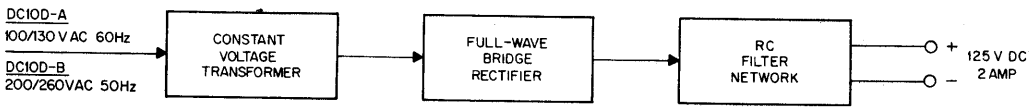


Figure 3-15 Telegraph Power Supply Block Diagram

3.1.5 Expanded Data-Set Control DC10E

Each expanded data-set control allows the central processor to exercise control over a maximum of eight data-sets, two of which may be equipped with automatic calling features. With this option, control information is transferred from the central processor to the data-set and data-set status information is transferred to the central processor via the DC10A on a priority interrupt basis under program control. The control interface of the expanded data-set control conforms to EIA standard RS232B. The data bits of the control and status words appear in bits 28 through 35 of the I/O data word. These are the same bits that are used to transfer a character to and from the 8-line group unit.

Since the function of the expanded data-set control differs from that of 8-line group unit when they are connected to a data-set, it is worthwhile to explain the main differences between the two-line groups. The main function of the eight-line group unit, it is recalled, is to transfer data (teletype characters) between the central processor and the data-set. The main function of the expanded data-set control is to provide the data-set with additional control features. Therefore, two separate data line numbers are associated with the data-set when the additional control features are utilized. One line is connected to the DC10B and is used for data transfer. The other line is connected to the DC10E and is used for control. Each of these lines is assigned a unique line number and is operated independent of the other.

A data-set connected to an 8-line group unit causes both a transmitter flag and a receiver flag to be set to indicate its data servicing requirements. A data-set also connected to an expanded data-set control operates in a slightly different manner. The expanded data-set control never causes a transmitter flag to be set because the data-set control information does not have to be periodically retransmitted.

Similarly, the data-set status remains constant for long periods of time. Therefore, only the more meaningful transitions of status information cause the receiver flag to be set. Provisions have been designed into the expanded data-set control to set the receiver flag artificially, as this is the only way to check the data-set status when no changes have occurred.

The DC10E option controls data-sets with and without the automatic calling feature. Due to this fact, two separate explanations of circuit operation at the block diagram level are provided. A typical data line without the automatic calling feature is explained and in the second discussion, the added circuits required for the automatic calling feature are detailed.

3.1.5.1 Data Line Without Automatic Calling - A block diagram of a typical DC10E data line without the automatic calling feature is shown in Figure 3-16. In each expanded data-set control (DC10E), there are six identical circuits that provide control of the data-sets that are connected to data lines 0 through 5. The data lines within the expanded data-set control are enabled by a line number decoder as they were enabled in the 8-line group unit. The following discussion will explain circuit operation in general terms to provide an understanding of the DC10E. Since this discussion explains the operation of a typical data line, some of the signal names shown on Figure 3-16 and used in the text are incomplete as shown. The following signal names should have a capital L and the line numbers as a prefix:

a. ARTIFICIAL FLAG (1)
b. OFF HOOK ENABLE (1)
c. CLR TO SND EIA (CB), CLR TO SND, and CLR TO SND FLG (1)
d. NOT CLR TO SND FLG (1)
e. RSTRN DETCTD EIA (RD), RSTRN DETCTD, and RSTRN DETCTD FLG (1)
f. UNLOAD
g. LOAD
h. CLEAR FLAGS
i. DATA TRM RDY EIA (CD)

The complete signal name for the line enable signal should include the line number, such as EDSC LINE 0 ENABLE, EDSC LINE 1 ENABLE, etc. The remaining signal names are complete as shown.

To control the data-set, the DATA TRM RDY EIA (CD) signal is routed from the DC10E to the data-set. The data-set responds to the DATA TRM RDY EIA (CD) signal as follows: the data-set is conditioned to answer an incoming call or to allow an outgoing call when the signal is true; the data-set connection is broken and the data-set is placed in the on-hook condition when the signal goes from true to false; and the data-set is placed in the inactive state when the signal is false. To maintain the DATA TRM RDY EIA (CD) signal in the true condition, the EDSC DATA TRM RDY OS and OFF HOOK ENAB (1) signals must be true. The EDSC DATA TRM RDY OS signal is kept in the true condition if a

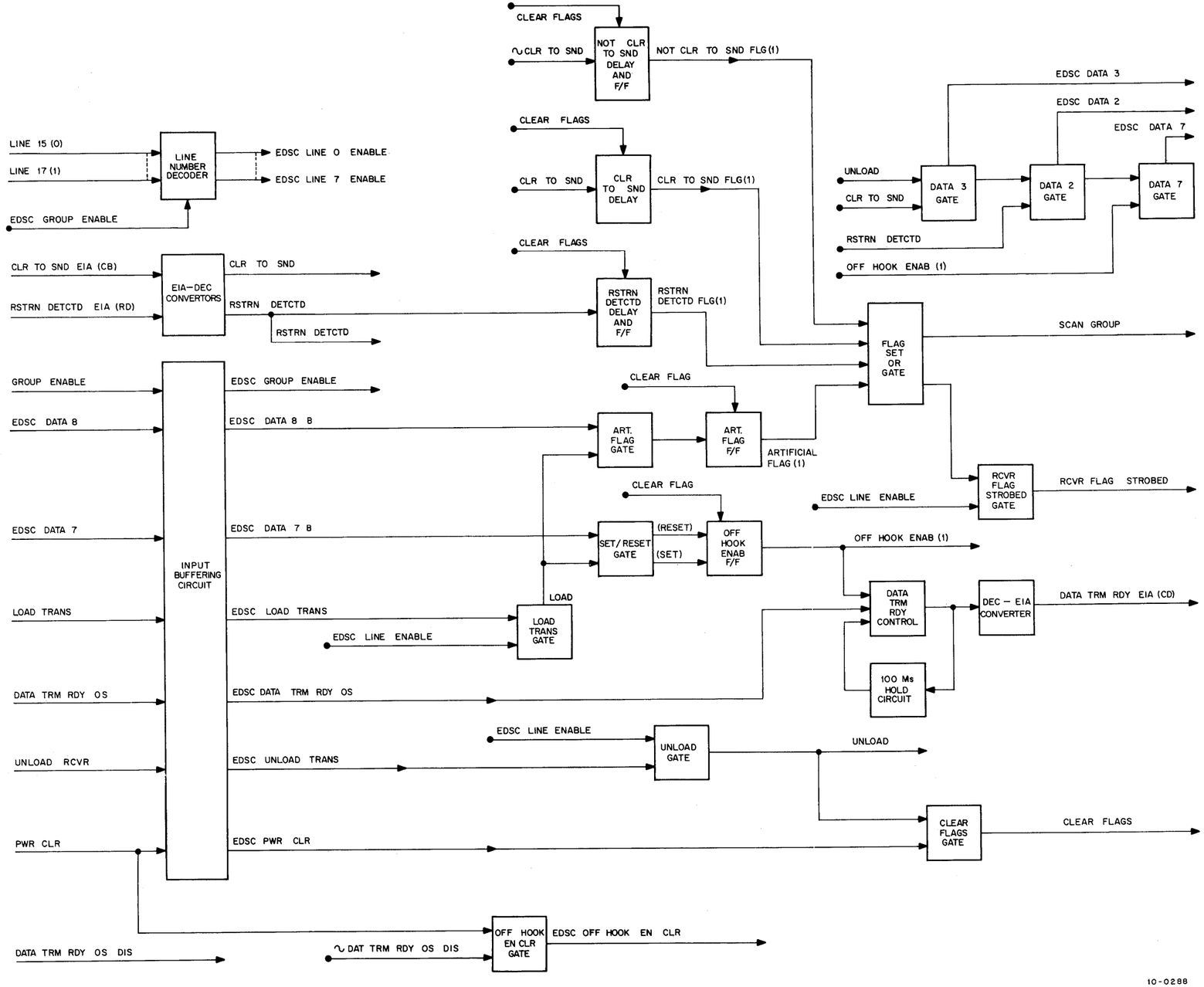


Figure 3-16 Expanded Data-Set Control
Typical Line Without Automatic Calling

CONO instruction is performed every 500 ms with bit 31 of the I/O word in the 1 state to maintain the DATA TRM RDY one-shot in the DC10A in the set condition. The OFF HOOK ENAB (1) signal is true when the OFF HOOK ENAB (off-hook enable) flip-flop is in the set condition. To set the OFF HOOK ENAB flip-flop, the central processor directs the data line number as explained in the discussion of the DC10A DATAO instruction, places a 1 in bit 29 of the I/O word, and performs a DATAO instruction. During the DATAO instruction, the 1 in bit 29 of the I/O word is routed to the DC10E from the DC10A via the line EDSC DATA 7. After passing through the input buffering circuit, the resultant signal, EDSC DATA 7B, is routed to a set/reset gate. During the DATAO instruction, the EDSC LOAD TRANS signal from the DC10A is ANDed with the EDSC LINE ENABLE signal for the selected data line in the LOAD TRANS gate and the resultant signal, LOAD, is used to enable the set/reset gate. The resultant signal from the set/reset gate sets the OFF HOOK ENAB flip-flop.

The EDSC DATA TRM RDY OS and OFF HOOK ENAB (1) signals are ANDed in the DATA TRM RDY control and the resultant signal is routed to a DEC-EIA converter. From the DEC-EIA converter, the DATA TRM RDY EIA (CD) signal is routed to the data-set and the data-set is enabled to answer incoming calls or complete outgoing calls.

If either the OFF HOOK ENAB (1) signal or the EDSC DATA TRM RDY OS signal goes to the false condition, the data-set connection is broken. The EDSC DATA TRM RDY OS signal goes to the false condition unless the central processor performs the required CONO instruction every 500 ms. Of course, this disconnects all data-sets because the EDSC DATA TRM RDY OS signal is common to all data lines. The OFF HOOK ENAB (1) signal goes to the false condition if the central processor performs a DATAO instruction with bit 29 of the I/O word in the 0 state. The 0 in bit 29 of the I/O word is routed through the DC10A and to the DC10E over the EDSC DATA 7 line. After passing through the input buffering circuit, the resultant signal, EDSC DATA 7B, is in the false condition and is applied to the set/reset gate. When the LOAD signal is generated during the DATAO instruction, the OFF HOOK ENAB flip-flop is reset and the DATA TRM RDY EIA (CD) signal associated with the selected data line is placed in the false condition. This breaks the associated data-set connection.

When either the OFF HOOK ENAB (1) signal or EDSC DATA TRM RDY OS signal goes to the false condition, a 100 ms hold circuit associated with the DATA TRM RDY control maintains the DATA TRM RDY EIA (CD) signal in the false condition for 100 ms to ensure that the data-set connection is broken. Of course, once the data-set connection is broken, the data set remains inactive until both the OFF HOOK ENAB (1) and EDSC DATA TRM RDY OS signals returns to the true condition.

The procedure that is used to transfer the status of a DC10E data line to the central processor is similar to the procedure used with the DC10B, but, of course, the type of information transferred is different. A CLR TO SND EIA (CB) signal is routed from the data-set to the DC10E and whenever the status of the data-set changes, the change in level of the CLR TO SND EIA (CB) signal is used to set either the NOT CLR TO SND (not clear to send) flip-flop or the CLR TO SND (clear to send) flip-flop.

A RSTRN DETCTD EIA (RD) signal is used to inform the central processor that the intermediate translator buffer in the data-set is full and the transfer of data is to be halted until the buffer is ready to accept new data. When this condition is detected, the level change of the RSTRN DETCTD EIA (RD) signal is used to set the RSTRN DETCTD (restrain detected) flip-flop. When one of these flip-flops is set, the resultant signal from the flip-flop is routed to the flag set OR gate and the SCAN GROUP signal is activated.

As the scanner in the DC10A scans the line groups, the active SCAN GROUP signal from the DC10E is detected in the true condition and each of the data lines in the DC10E is strobed in a sequential fashion. When the interrupting data line is located, the scanner is stopped and a program interrupt is initiated. The central processor performs a DATAI instruction on a priority basis after it has identified a receiver interrupt. During the DATAI instruction, the EDSC UNLOAD RCVR signal is in the true condition and is ANDed with the EDSC LINE ENABLE signal associated with the interrupting data line in the unload gate. The resultant signal from the unload gate, UNLOAD, gates the status of the CLR TO SND and RSTRN DETCTD signals and the condition of the OFF HOOK ENAB flip-flop to the central processor via the DC10A.

An additional feature of the DC10E allows the central processor to generate an artificial program interrupt under program control. To perform this function, a DATAO instruction is performed with a 1 in bit 28 of the I/O word. This signal is routed through the DC10A and the resultant signal is applied to the DC10E over the EDSC DATA 8 line. After being routed through the input buffering circuit, the resultant signal is ANDed with the LOAD signal in the ART FLAG (artificial flag) gate and the resultant signal is used to set the ARTIFICIAL FLAG flip-flop. The ARTIFICIAL FLAG (1) signal is applied to the flag set OR gate and a program interrupt is generated as explained above. In this fashion, the central processor can check the status of the data-set and the condition of the OFF HOOK ENAB flip-flop even when a change in status has not occurred.

3.1.5.2 Data Line With Automatic Calling - A block diagram of a typical DC10E data line with the automatic calling feature is shown in Figure 3-17. There are two identical data lines in each DC10E that are used to control the data-sets connected to data lines 6 and 7. When Figures 3-16 and 3-17 are compared, it is observed that all the circuits on Figure 3-16 are also contained in Figure 3-17. Since these circuits have been explained in the early discussion, they will not be discussed again here. Instead, the additional circuits for the automatic calling feature will be described.

The signal names that were incomplete in Figure 3-16 are also incomplete on Figure 3-17 and they are completed by adding an L6 or L7 as a prefix. A number of additional signal names shown in Figure 3-17 are also incomplete. To complete the following signal names, add an L6 or L7 as a prefix:

a. DATA LINE OCC EIA (DLO), DATA LINE OCC
b. PRSNT NXT DGT EIA (PND), PRSNT NXT DGT, and PRSNT NXT DGT FLG (1)

c. ABNDN CALL EIA (ACR), ABNDN CALL, ABNDN CALL FLG (1)

d. CALL REQ EIA (CRQ)

e. DIGIT PRESENT EIA (DPR)

f. NB8 EIA, NB4 EIA, NB2 EIA, and NB1 EIA

g. LOAD DIGIT

When a call is to be completed, the central processor performs a DATAO instruction with bits 29 and 30 of the I/O word in the 1 state. As earlier explained, bit 29 prevents the data-set from going to the on-hook condition. Bit 30 is routed through the DC10A and to the DC10E over the EDSC DATA 6 line. After passing through the input buffering circuit, the resultant signal, EDSC DATA 6B, is applied to a set/reset gate. The LOAD signal, generated during the DATAO instruction, enables the set/reset gate and the resultant signal from the set/reset gate sets the CALL REQ (call request) flip-flop. With the CALL REQ flip-flop in the set condition, the CALL REQ EIA (CRQ) signal is true and is routed to the data set.

The CALL REQ EIA (CRQ) signal causes the data-set to pick up a telephone line and request a dial tone. When the dial tone is received by the data-set, the DATA LINE OCC EIA (DLO) and PRSNT NXT DGT (PND) signal from the data-set go to the true condition. The PRSNT NXT DGT signal sets the PRSNT NXT DGT (present next digit) flip-flop and causes the SCAN GROUP signal to go to the true condition. As the scanner scans the line groups, it locates the interrupting data line and causes a program interrupt. The central processor identifies the type of interrupt and performs a DATAI instruction to transfer the status information. The status information indicates that the data-set is ready to receive a digit.

The central processor now performs a DATAO instruction with the following information in the I/O word: the first digit to be dialed in bits 32 through 35 (a BCD digit); a 1 in bit 31; a 1 in bit 30; and a 1 in bit 29. Bit 29 prevents the data set from going to the on-hook condition and bit 30 keeps the CALL REQ EIA signal in the true condition. At the same time, bits 31 through 35 are routed through DC10A and are applied to the DC10E and EDSC DATA 5 through EDSC DATA 1. After passing through the input buffering circuit, the EDSC DATA 5B signal is ANDed with the LOAD signal, generated during the DATAO instruction, in the load digit gate. The resultant signal, LOAD DIGIT, is used to enable the set/clear gates associated with EDSC DATA 4B through EDSC DATA 1B and to enable the DGT PRSNT (digit present) gate. With the PRSNT NXT DGT signal in the true condition, the DGT PRSNT flip-flop is set and with the set/clear gates associated with EDSC DATA 4B through EDSC DATA 1B enabled, the BCD digit is jammed into the associated flip-flops.

After DEC-EIA conversion, the resultant signals are routed to the data-set and the first digit is dialed. When the first digit has been dialed, the PRSNT NXT DGT signal goes to the true condition,

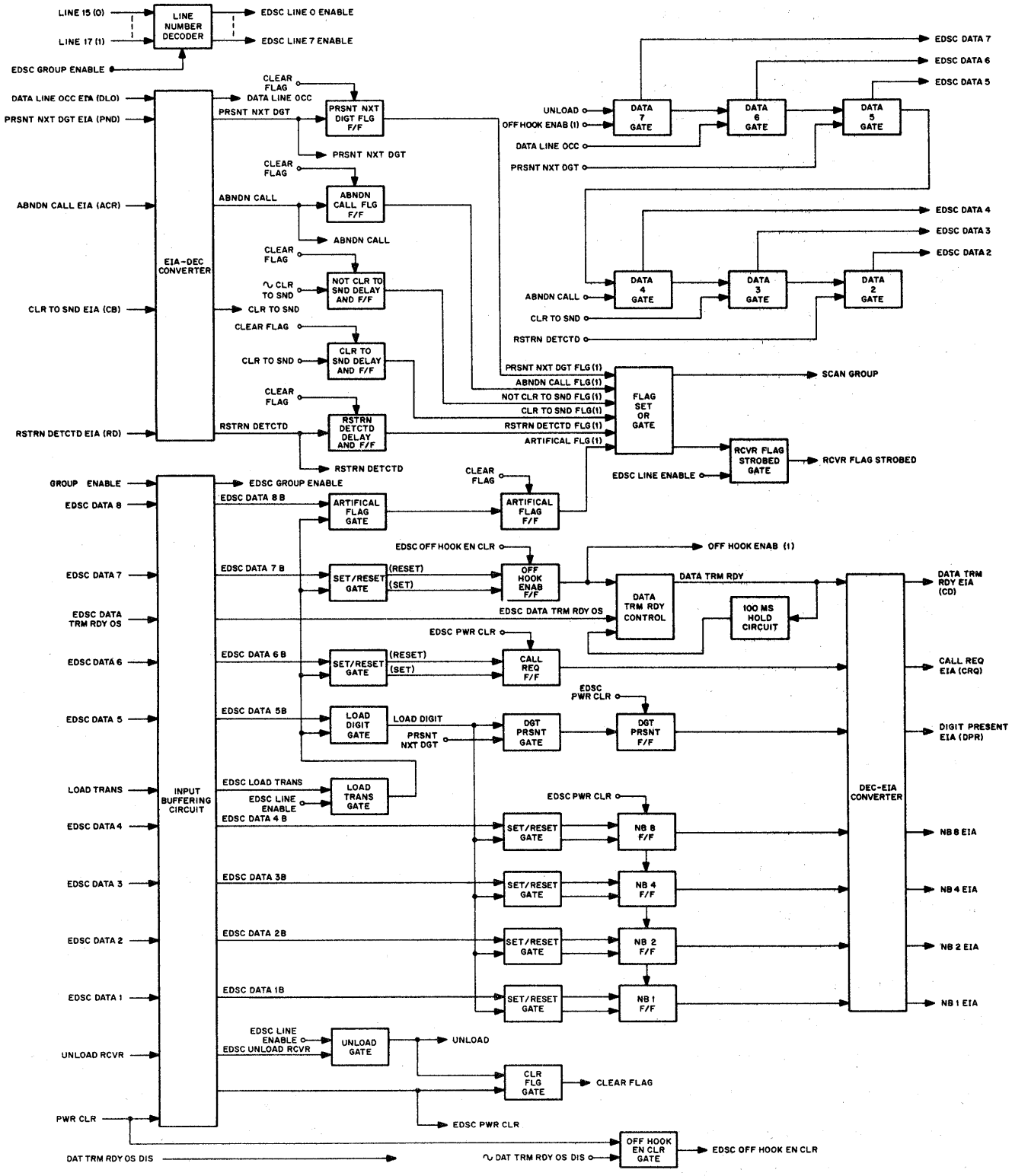


Figure 3-17 Expanded Data Set Control - Typical Line With Automatic Calling

the scanner causes a program interrupt and, after identifying the type of program interrupt, the central processor routes the next digit to the data-set by performing a DATAO instruction. This action is repeated for each digit until the complete number has been dialed.

If a data connection is not established within 7 to 40s after the last digit (screwdriver adjustment on front of automatic calling unit) the ABNDN CALL EIA (ACR) signal goes to the true condition. When the ABNDN CALL EIA (ACR) signal goes true, the scanner causes a program interrupt. The central processor identifies the program interrupt and causes the CALL REQ EIA (CRQ) signal to go false by performing a DATAO instruction with bit 30 of the I/O word a 0. Several seconds after the CALL REQ EIA (CRQ) signal to the data-set goes false, the DATA LINE OCC EIA (DLO) signal to the DC10E goes false. At this time, the central processor again tries to complete the call.

Status information for data lines 6 and 7 of the DC10E is transferred in a similar fashion as the status information for data lines 0 through 5. The main difference between the two types of transfers is the amount of information transferred. When the central processor performs a DATAI instruction for data line 6 or 7 of the DC10E, the condition of the DATA LINE OCC, PRSNT NXT DGT, and ABNDN CALL signals are identified along with the condition of the CLR TO SND, RSTRN DETCTD, and OFF HOOK ENAB (1) signals. The DATAI instruction is performed the same for both types of lines.

3.2 DETAILED DESCRIPTION

A description of each engineering drawing is provided in this section. Each description contains an explanation of the logic functions and flow diagrams shown on the drawing and, when possible, the logic functions are identified with the associated block on the preceding block diagrams. The level of detail in each description is sufficient to provide an understanding of the logic function but is not intended to explain the complete circuit operation. If additional detail is required to understand specific circuit operation, the maintenance personnel should refer to the DEC logic and module descriptions contained in the Digital Logic Handbook.

The engineering drawings for each DLS option are discussed under a separate subheading. Each drawing number is listed at the start of the paragraph that contains a discussion of the information shown on the drawing. To aid in the understanding of these discussions, refer to the engineering drawings contained in the separate engineering drawing volume.

3.2.1 D-FD-DC10A-0-FD

This drawing details all control unit operations and shows the scanner operation in a flow diagram form. The following discussion is supported by the two sheets of this drawing and is intended to provide maintenance personnel with a review of the above operations.

To understand a CONO instruction, it must be remembered that the DLS is selected and the IOB CONO SET signal is generated 1 μs after the IOB CONO CLR signal. Under these conditions, the IOB CONO CLR signal (D8, sheet 1) starts the CONO by clearing the PI register. Then, the IOB CONO SET signal (D6, sheet 1) is generated and the following functions are performed: the PI channel number on the lines IOB 33 through IOB 35 is stored in the PI register; the DLS power clear circuit is activated if IOB 30 (1) is true, and the DATA TRM RDY OS one-shot is set if IOB 31 (1) is true; and the group and units registers in the scanner are cleared if IOB 32 (1) is true.

To understand a DATAO instruction, it must be remembered that the IOB DATAO SET signal follows the IOB DATAO CLR signal by 1 μs. The IOB DATA CLR signal (D5, sheet 1) sets the CNTR DATAO flip-flop and also sets SCNR DIRECTED DATA flip-flop if IOB 11 (1) is true and clears SCNC PI REQ if IOB 11 (1) is false. If IOB 11 (1) is true, the SCNR DIRECTED DATA flip-flop enables the directed data switch and the data line number in IOB bits 12 through 17 selects the data line and conditions the data gates. When IOB 11 (1) is false, the line number in the scanner registers is used to select the data line and condition the data gates. With the CNTR DATAO flip-flop in the set condition, the data gates are enabled and the data are routed to the selected line group via the associated data cable.

The IOB DATAO SET signal (D2, sheet 1) is generated 1 μs and the LOAD TRANS A and B signals are generated and routed to the line groups. When the LOAD TRANS signal is applied to the selected line group, the data on the active data cable are loaded into the selected line unit and the selected line transmitter flag is cleared. The trailing edge of the DLS DATAO SET signal clears the CNTR DATAO, SCNR DIRECTED DATA, and the SCNR COUNT RESTART flip-flops and the scanner returns to normal operation.

The last operation shown on this diagram is the power reset. The IOB RESET signal (D7, sheet 1) is routed from the central processor and is used to generate reset signals for the DLS control circuits.

The scanner flow diagram is drawn in two parts. The second sheet of the flow diagram shows the scanning subroutine. When the SCNR PI REQ flip-flop is in the cleared condition, each group (line group) is checked for a set flag in sequential fashion. If a set flag is not located, the group counter is incremented and the next group is checked. When a true group flag is located, the lines (data lines) within this group are checked for a set flag in a sequential fashion. If the line flag is not set, the units counter is incremented and the next line is checked. When the set flag is located and the maintenance signal is not selected, the SCNR PI REQ flip-flop is set and the scanner is stopped. At this time, a PI signal is routed to the central processor and the interrupting data-line number is stored in the group and units counter.

3.2.2 D-BS-DC10A-0-CLKD

This drawing shows the baud-rate clock circuits and three control circuits. The baud-rate clock circuits (A1 through C8) contain three identical clock circuits that are used to establish the baud rates. Refer to the block diagram discussion for an explanation of circuit operation.

The unload RCVR gate (D7) is used to generate the CLKD UNLOAD RCVR A and B signals. In this gate, the signals CNTR RCVR FLAG (1) and DLS DATAI are ANDed and the resultant signal is routed to bus drivers where it is amplified. The amplified signal is routed to the line groups as the signal CLKD UNLOAD RCVR during a DATAI and is used to load the data into the central processor via the I/O bus. The signal IND ECHO is used to perform a similar function during the maintenance mode.

The CLKD LOAD TRANS A and B signals are generated in the following fashion. During a DATAO instruction, the DLS DATAO SET OR ECHO signal is routed to the bus drivers (D5) from the DATAO set gate. The resultant signal from the bus driver is routed to all line groups and is used to load the data on the active data cable into the line group.

The last signals that are shown on this drawing are the CLKD DAT TRM RDY OS A and B signals. When the DATA TRM RDY OS is in the 1-state, the DLS DAT TRM RDY OS (1) signal is routed from the DLS DATA TRM RDY OS and is applied to the bus drivers (D3). From the bus drivers, the resultant signals are routed to the line groups. This signal is used in the expanded data-set control option to permit the data-set to be in the off-hook condition.

3.2.3 D-BS-DC10A-0-CNTR

This drawing contains a series of control logic circuits. The group transmit enable gates (A7 through D7) generate the transmit enable (TRANS ENABLE) signal for the selected line group during a DATAO instruction, if IOB 27 (1) is false. To generate the TRANS ENABLE signal, the group enable signal for the selected line group is ANDed with the CNTR DATAO and ~RIO IOBR 27 (1) signals. The resultant signal from the selected group transmit enable gate is routed to the selected line group and is used to condition the transfer circuit.

During the maintenance mode, the IND ECHO signal is routed to a series of eight inverters. The resultant signals from the inverters are routed to the eight line groups as a TRANS ENABLE signal.

The DLY B311 delay (D5) is started by the DLS DATAO SET signal during the performance of a DATAO instruction. After an 85 ns delay, the trailing edge of the CNTR DATAO SET DLY signal clears the CNTR DATAO flip-flop, the SCNR DIRECTED DATA flip-flop and SCNR COUNT RESTART flip-flop.

The CNTR WRITE IO BUS signal is generated by the write I/O bus gate (C5) during a DATAI or CONI instruction. When the DLS DATAI signal or DLS CONI signal is applied to the write I/O bus gate, the resultant signal is routed to a bus driver. From the bus driver, the CNTR WRITE IO BUS signal is routed to the write I/O bus gates. The write I/O bus gates are conditioned and the data are transferred to the central processor via the I/O bus.

The receiver flag strobed control is shown at B5. During a DATAI instruction, the CNTR RCVR FLAG flip-flop is set if SCNC RCVR FLAG STROB signal and SCNC COUNT RESTART (1) signal

is true. The CNTR RCVR FLAG flip-flop stores the fact that there was a receiver flag even though the actual flag signal, SCNC RCVR FLAG STROB, is cleared early in the DATAI instruction cycle by the CLKD UNLOAD RCVR signal. In this way, it is assured that bit 27 of the DATAI I/O data word is correct. The CNTR RCVR FLAG flip-flop is cleared by the trailing edge of the DLS DATAI signal.

The CNTR DATAO flip-flop and associated bus drivers (B3 and C3) are used to generate the CNTR DATAO signal during a DATAO instruction. Signal DLS DATAO CLR sets the CNTR DATAO flip-flop and the 1 side of the CNTR DATAO flip-flop is connected to four bus drivers. The resultant signal from the bus driver is used to enable the selected group transmit enable gate and the selected group data gates throughout the DATAO instruction cycle. The trailing edge of the CNTR DATAO SET DLY signal clears the CNTR DATAO flip-flop and the DLS is ready for the next instruction 85 ns after the DLS DATAO SET signal was applied.

3.2.4 D-BS-DC10A-0-DAT1 Through D-BS-DC10A-0-DAT4

These drawings show the eight similar data mixer circuits required to perform the data transfers between the central processor and the eight line groups. Each data mixer consists of eight data gates that are used during a DATAO instruction, eight data gates that are used during a DATAI instruction and one data gate that is used during a CONI instruction. Since all data mixers are similar, the following explanation is used to explain the operation of one data mixer and is intended to cover the operation of all data mixers.

During a DATAO instruction, the data bit associated with the data mixer is routed in parallel from the input data buffering circuit to the eight data gates associated with the DATAO transfer. The CNTR DATAO signal is routed to the data gates associated with the DATAO transfer and is used to condition all of these data gates. Then, the selected group enable signal is routed to the data gate associated with the selected line group and the data gate for the selected line group is enabled. With the data group enabled, the data bit is routed through the enabled data gate and is routed to the selected line group via the data cable.

The operation of the data mixer during a DATAI instruction is similar to the data mixer operation during a DATAO instruction except that the data bit is routed from the selected line group to the data gate associated with the selected line group. The DLS DATAI signal is routed to the data gate associated with the DATAI instruction and is used to condition these gates. Then, the group enable signal for the selected line group enables the associated data gate and the data bit passes through the enabled data gate to the associated write I/O bus gate.

During a CONI instruction, the eight CONI data gates are conditioned but only the data mixers for bit 1 through bit 5 are used to transfer data. Signal ~SCNC TRANS FLAG STROB is routed

to a data gate associated with data mixer 5 and is false when a transmitter flag is set. A data gate associated with data mixer 4 receives the CNTR RCVR FLAG (0) signal and this signal is false when a receiver flag is set. The three 0 sides of the PI register are routed to data gates associated with data mixers 1 through 3. The false conditions of these signals are used to obtain the desired information transfer because there are three inversions between the data mixer data gates and the I/O bus. The three inversions are performed as follows: the first inversion is performed by a gated inverter in the data mixer data gate; the second inversion is performed by a gated inverter in the write I/O bus gates; and the third inversion is caused by the logic level change at the I/O bus interface. Then, the data gates associated with the CONI instruction are enabled by the DLS CONI signal during the performance of a CONI instruction. The information is routed through the enabled data gates and applied to the associated write I/O bus gates.

3.2.5 D-BS-DC10A-0-DLS

This drawing contains the logic that controls the DLS input/output operation. Since all I/O devices share the I/O bus, the DLS must be selected by the central processor before any input/output instruction is performed. To select the DLS, the central processor routes the device number over 14 lines of the I/O bus to the control unit. The 14 device-selection lines are connected to a pair of W990 Option Cards (B7 through D7) and the option cards are wired to select the desired 3-digit octal device number.

On this drawing the jumpers are connected to decode the device number 240_8. The output lines from the option cards are routed to the DLS device decoder (D6) along with the ~IND MAINT signal. When the DLS device number 240_8 is generated by the central processor and the maintenance mode is not selected, the device number is decoded and the DLS DEVICE SELECTED signal is true.

When a DATAO instruction is executed, the central processor generates the IOB DATAO CLR signal and the DLS device number. These signals are routed to the control unit via the I/O bus. The DLS device number is decoded and the DLS DEVICE SELECTED signal is used to enable the DATAO clear gate (D5). At the same time, the IOB DATAO CLR signal is inverted and the resultant signal is applied to the DATAO clear gate. The DATAO clear gate generates the DLS DATAO CLR signal and this signal is used to condition the control unit to perform the DATAO instruction by setting the CNTR DATAO flip-flop and possibly the SCNR DIRECTED DATA flip-flop. The central processor generates the IOB DATAO SET signal 1 μs after generating IOB DATAO CLR. With the DLS DEVICE SELECTED signal still true, the data clear gate (D5) is enabled. The IOB DATAO SET signal is inverted and the resultant signal is routed to the enabled DATAO clear gate. The DLS DATAO set signal is generated by the DATAO clear gate and the DLS DATAO SET OR ECHO signal is generated by the TRANS OR gate (B2) to complete

the DATAO instruction. The TRANS OR gate (B2) also generates the DLS DATAO SET or ECHO signal when the IND ECHO signal or the IND CLEAR TRANS signal is true during the maintenance mode.

To perform a CONO instruction, the DLS device number and the IOB CONO CLR signal are generated by the central processor. The DLS device number is decoded to generate the DLS DEVICE SELECTED signal and the DLS DEVICE SELECTED signal enables the CONO clear control gate (C5). The IOB CONO CLR signal is inverted and the resultant signal is routed to the enabled CONO clear control gate. At this time, the DLS PI CLR signal is generated and is used to clear the PI storage register (B4 and B5). The central processor generates the IOB CONO SET signal 1 μs after IOB CONO CLR signal. With the DLS DEVICE SELECTED signal still true, the CONO set control gate (C5) is enabled. The IOB CONO SET signal is inverted, the resultant signal is routed to the enabled CONO set control gate, and the DLS CONO SET signal is generated to execute the CONO instruction. During the CONO instruction, the following functions are performed: the 3-digit PI channel number on RIO IOBR 33 (1) through RIO IOBR 35 (1) is gated into the PI storage register (B4 and B5); the DLS DATA TRM RDY one-shot (B4) is reset, if RIO IOBR 31 (1) is true; the DLS RESET GROUP signal (A2) and the SCNC RESET UNITS signal are generated, if the RIO IOBR 32 (1) signal is true; the DLS RESET signal is generated and a power clear is initiated by the power reset gate (D3), if the RIO IOBR 30 (1) signal is true.

When a DATAI instruction is executed, the central processor generates the DLS device number and the IOB DATAI signal. The DLS device number is decoded and the DLS DEVICE SELECTED signal enables the DATAI control gate (B5). With the DATAI control gate enabled, the DLS DATAI signal is generated when the IOB DATAI signal is applied. The DLS DATAI signal conditions the DATAI data gates in the data mixers, generates the CNTR WRITE IO BUS signal, and conditions the unload RCVR gate and the RCVR flag strobed control as shown in the DATAI block diagram.

To execute a CONI instruction, the central processor generates the DLS device number and the IOB CONI signal. The DLS device number is decoded and the DLS DEVICE SELECTED signal is generated and is used to enable the CONI control gate (B5). When the IOB CONI signal is routed to the enabled CONI control gate, the DLS CONI signal is generated. The DLS CONI signal generates the WRITE IO BUS signal and enables the CONI data gates in the data mixers. The output lines from the PI storage register (A5 and A4) are connected to the CONI data gates in the data mixers and the line number stored in the PI storage register is routed to the central processor via the I/O bus when the CONI is executed.

The PI decoder (A6 and A7) is conditioned by the SCNR PI REQ (1) signal. With the SCNR PI REQ (1) signal true, the line number stored in the PI register is decoded and the output line from the decoder associated with the assigned PI channel is activated. The decoder output lines are routed to the central processor via the I/O bus and the active line identifies which PI channel has initiated the program interrupt.

The power clear circuit (B3, C1 through C4, and D1 through D4) is used to clear the DLS control circuits. This circuit is activated when the power switch is turned-on or turned-off, when the MAINT switch is turned off or on due to contact bounce, when the RIO IOBR 30 (1) signal is true during the execution of a CONI instruction, or when the central processor generates the IOB RESET signal (D8). When the last two conditions occur, the DLS RESET signal is generated and is routed to the power clear gate (D3). The power clear gate generates the DLS PWR CLR signal and the DLS control circuits are cleared. When the power switch is turned on, power is applied to the DLS but a normally-closed (NC) contact in the 844 Power Control remains in the NC position 4s. During the 4s delay, the ~DLS POWER UP signal is true and is used to set the DLS PWR ON one-shot. The DLS PWR ON (1) signal from the DLS PWR ON one-shot is true and is routed to the power reset gate where the DLS PWR CLR signal is generated. After the 4s delay, the NC contact opens and the DLS PWR ON one-shot returns to the clear condition after an additional 100 ms. When the power switch is turned off, the NC contact in the power control closes and DLS power remains in the on condition for 4s. When the NC contact closes, the ~DLS POWER UP signal is again true and the DLS PWR ON one-shot is set. At this time, the DLS PWR ON (1) signal to the power clear gate is true and the DLS PWR CLR signal is generated.

When the MAINT switch is turned on or off, the contact bounce sets the DLS PWR ON one-shot. The DLS PWR ON (1) signal is true, and of course, the DLS PWR CLR signals are generated.

3.2.6 D-BS-DC10A-0-IND

This drawing shows the circuits used in the maintenance circuit. In zones A6 through D8, the circuit that compares the setting of the group and units switches with the contents of the scanner counters is shown. Each output line from the switches is connected to a clamped load and an AND gate. A complementary signal from the scanner register is connected to the AND gate and the two signals are compared. When the switch-selected data line number is different than the data line number selected by the scanner, two or more of the AND gates are enabled and the IND ADDRESS $\neq$ SW signal is true. The scanner continues to scan through the line group until it reaches the switch-selected data line number. At this time, the IND ADDRESS $\neq$ SW goes false if the selected data line has either a transmitter or receiver flag in the set condition.

The inverter shown at A6 generates the IND MAINT signal when the MAINT switch on the indicator panel is turned on. When the IND MAINT signal is true, it inhibits the DLS device decoder, maintains the PI REQ flip-flop in the reset condition, and conditions the RCVR and TRANS AND gates in the echo control circuit.

A pair of clamped loads shown at D6 are used in the generation of the IND DTR OS DIS signal when the DTR DIS switch on the indicator panel is turned on. The IND DTR OS DIS signal is used during software debugging. In this way, the need to set the data term ready one-shot every 500 ms is eliminated.

At B1 through B3, the group switch is shown. The units switch is not shown, but it is identical to the group switch. Each switch is wired to generate one octal digit and the output lines from the switches are routed to the comparison circuit shown at A7 through D8.

At C1 and C2, the TRANS AND gate and pulse amplifier are shown and at C3 and C4, the RCVR AND gate, pulse amplifier and inverter are shown. The components are used in the echo circuit to generate the IND CLEAR TRANS signal and the IND ECHO signal, respectively.

The delay, gates, and pulse amplifier used in the indicator circuit is shown in zones D1 and D4. The SCNR COUNT CLOCK signal starts the 500 ns delay and at the end of the delay, the IND COUNT CLOCK DEL signal is routed to a DCD gate. When the switch-selected data line number is equal to the scanner-selected data line number and a data line flag associated with the selected data line is in the set condition, the ~IND ADDRESS ≠ SW signal is true and the DCD gate is enabled. When the IND COUNT CLOCK DEL is applied to the enabled DCD gate, a signal is applied to a pulse amplifier and the IND STROBE signal is generated by the pulse amplifier. The IND STROBE signal is used to enable the TRANS and RCVR DCD gates and the active strobed signal(s) is routed through its enable DCD gate. The resultant signal from the active DCD gate starts a one-shot and the associated indicator is illuminated.

In zones A4, B4, A5, B5, and B6, the connections for the indicators are shown. These indicators provide an indication of the DLS operation.

3.2.7 D-BS-DC10A-0-LSEL

This drawing shows the group decoder and the line number bus drivers. The six lines from the group control switch are connected to the group decoder (A7 through D7). The six lines of the octal group number associated with the selected group are decoded and the group enable signal for the selected group is generated. The selected group enabled signal is inverted and routed to the group scanner control, the data mixers and the line groups.

Each of the six output lines from the units control switch is routed to a bus driver and the selected line number is routed to the bus drivers over the six lines as an octal number. After power amplification in the bus drivers, the selected line number is routed to the line decoders in the line groups.

3.2.8 D-BS-DC10A-0-RIO

Shown in this drawing are the input buffering circuits between the central processor and the DLS. These circuits provide the required buffering during the execution of a DATAO or CONO instruction. The central processor routes a 1 over IOB 11 (1) (D7) and the selected data line number over IOB 12 (1) through IOB 17 (1) (B7 through D7) when the active data line is selected under program control

during a DATAO instruction. When data are transferred during a DATAO instruction, the central processor routes a 0 over IOB 27 (1) (B7) to maintain the RIO BIT 27 flip-flop in the cleared condition. The RIO BIT 27 flip-flop prevents the RIO BIT 27 (0) signal from going false before the CNTR DATAO signal and thus prevents a positive spike in the GROUP n ENABLE signals. After a series of transfers have been completed, the central processor performs a DATAO instruction with IOB 27 (1) a 1. The RIO BIT 27 flip-flop is set and the transmitter enable gates are inhibited. Under these conditions, the transmitter flag is cleared during the DATAO instruction and the scanner is freed to scan the line groups. At the end of the DATAO instruction, the RIO BIT 27 flip-flop is cleared by the CNTR DATAO SET DLY signal and the DLS is conditioned for the next instruction.

Data may be transferred over IOB 28 (1) through IOB 35 (1) (B5 through D5) during the execution of a DATAO instruction, and over IOB 30 (1) through IOB 35 (1) during the execution of a CONO instruction.

3.2.9 D-BS-DC10A-0-SCNC

This two sheet drawing shows the scanner control circuits. On sheet 1, the scanner control (B3 through B8 and D7), the units scanner control (C1 through C4), units counter reset circuit (D5) and the PI REQ flip-flop clear circuit (C5) are shown. The transmitter flag gate (A6 through D8) and the receiver flag gate (A2 through A4) are shown on sheet 2.

In each line group, the flag lines from the eight data lines are collector ORed and a common scan group line is returned to the scanner control. The scan group lines from the eight line groups are connected to their associated AND gate shown at B3 through B8 of sheet 1. As the count in the group counter is decoded, the group enable signal for the selected line group is generated and routed to its associated AND gate. In the AND gate, the group enable signal and the scan group line for the selected line group are ANDed. If all data line flags in the selected line group are in the cleared state, the signal on the scan group line is false and the SCNC SCAN signal is false. Under these conditions, the ~SCNC SCAN signal is true and the SCNC COUNT GROUP NO is generated (D7, sheet 1). The group counter is incremented by the SCNC COUNT CLOCK signal, the next sequential group enable signal is generated, and the next sequential scan group line is checked. When a line group with a data line flag in the set condition is checked, the SCNC SCAN signal is generated and the group counter is stopped because the ~SCNC SCAN signal goes to the false condition. With the SCNC SCAN signal true, the unit scanner control (C1 through C4) is enabled. At this time, the scanner sequentially scans each data line in the selected line group. If both the transmitter and receiver flag strobed signals associated with the data line being scanned are false, the SCNC TRANS FLAG STROB and SCNC RCVR FLAG STROB signal are false and the ~SCNC FLAG STROBED signal is true. Under these conditions, the ~SCNC FLAG STROBED signal is ANDed with SCNC SCAN signal to generate the SCNC UNITS signal and the

units counter is incremented. After the units counter is incremented, the next sequential data line in the selected line group is checked for a set data line flag. This action is repeated until the SCNC TRANS FLAG STROB signal and/or SCNC RCVR FLAG STROB signal becomes true to indicate a set data line flag or until line 7 is reached. At this time, the SCNC FLAG STROBED signal is inverted and the resultant signal is ANDed with the SCNC SCAN signal to generate the SCNC SET PI REQ signal. At this time, the scanner is stopped.

If all data lines in a line group have been checked without locating a set data line flag, an AND circuit (C7 and D7, sheet 1) in the group scanner control generates the SCNC COUNT GROUP NO signal when the units counter reaches the count of seven and the ~SCNC FLAG STROBED signal is true.

The SCNC RESET UNITS signal is generated by the circuit shown at D5 of sheet 1 and is used to reset the units counter under the following conditions: when the DLS PWR CLR signal is generated; when the SCNC COUNT GROUP NO signal is ANDed with the SCNR COUNT CLOCK signal; and during a CONO instruction, if IOB 32 (1) is a 1.

The circuit shown at C5 of sheet 1 is used to generate the SCNC PI REQ CLR signal during the execution of a DATAI when the CNTR RCVR FLAG (1) signal is true or during the execution of a DATAO instruction, if the ~RIO IOBR 11 (1) signal is true. The SCNC PI REQ CLR signal is used to clear the PI REQ flip-flop.

The transmitter flag gate is shown at A6 through D8 of sheet 2. In each line group, the transmitter flag strobed lines from the eight data lines are collector ORed and a common transmitter flag strobed line from each line group is returned to the transmitter flag gate. When the scanner locates a line group that requires service, each data line in the line group is strobed sequentially until a set transmitter flag is located. At this time, a TRANS FLAG STROBED signal is routed from the line group to the transmitter flag gate via the common transmitter flag strobed line. The TRANS FLAG STROBED signal is inverted and applied to an OR gate. The resultant signal from the OR gate is inverted and the SCNC TRANS FLAG STROB signal is generated and routed to the unit scanner control.

The receiver flag gate is shown at A2 through A4 of sheet 2. The operation of the receiver flag gate is identical to the transmitter flag gate. As in the transmitter flag circuit, the receiver flag strobed lines from the eight data lines in each line group are collector ORed and a common receiver flag strobed line from each line group is returned to the receiver flag gate. When the data lines in the selected line group are strobed, a RCVR FLAG STROBED signal is returned to the receiver flag gate, if the scanner locates a receiver flag in the set condition. The RCVR FLAG STROBED signal is used to generate the SCNC RCVR FLAG STROB signal that is routed to the unit scanner control.

When the unit scanner control receives SCNC RCVR FLAG STROB signal and/or the SCNC TRANS FLAG STROB signal, the scanner is stopped and a program interrupt signal is generated.

3.2.10 D-BS-DC10A-0-SCNR

This drawing shows the group counters (B5 through B7), the units counter (B3 through B5), the directed data flip-flop (B7 and B8), the group directed data switch (D1 through D8), the units directed data switch (C1 through C8), the scanner clock (B1), the scanner count restart flip-flop (B3), the scanner count hold flip-flop (B1), and the PI REQ flip-flop (B3).

The scanner clock is a 600 ns clock used to clock the scanner operation. The output from the clock, SCNR CLOCK, is routed to a DCD gate that is enabled when the SCNR COUNT HOLD flip-flop is in the reset condition or when the maintenance mode is selected. The output signal from the DCD gate is applied to a pulse amplifier and the resultant signal, SCNR COUNT CLOCK, is used to perform the following functions: increment the group counter when the SCNC COUNT GROUP NO signal is true; increment the units counter when the SCNC COUNT UNITS signal is true; set the PI REQ flip-flop when the SCNC SET PI REQ signal is true; start a delay in the indicator circuit; and set the SCNR COUNT RESTART and SCNC COUNT HOLD flip-flops when the SCNR SET PI REQ signal is true. During a program interrupt the PI REQ flip-flop is in the set condition, the DCD gate is disabled, and scanner operation is stopped.

The SCNR COUNT HOLD (hold) flip-flop is provided to perform the following functions: to stop the SCNR COUNT CLOCK signal at the same time as the PI REQ flip-flop; to allow the PI REQ flip-flop to be cleared when the DLS DATAO CLR signal or DLS DATAI signal becomes true; and to prevent the restarting of the SCNR COUNT CLOCK signal until the trailing edge of the DLS DATAI signal or CNTR DATAO SET DLY signal. The SCNR COUNT RESTART (restart) flip-flop forms the second half of the two flip-flop restart synchronizer with the COUNT HOLD flip-flop to facilitate restarting the SCNR COUNT CLOCK signal without getting a partial pulse. When a program interrupt is initiated, the SCNC SET PI REQ signal conditions the set gate to both flip-flops and the next SCNR COUNT CLOCK pulse sets both flip-flops. With the hold flip-flop in the set condition, the DCD gate at the scanner clock output is inhibited and the scanner operation is stopped until either the DLS DATAI signal or CNTR DATAO SET DLY signal becomes false after the interrupt has been serviced. At this time, the restart flip-flop is cleared by whichever signal goes false and the clear gate to the hold flip-flop is conditioned. The next SCNC CLOCK pulse from the scanner clock clears the hold flip-flop. With the hold flip-flop in the 0-state, the DCD gate at the output of the scanner clock is enabled and the scanner is returned to normal operation.

The group counter and the units counter are identical 3-stage flip-flop counters. The SCNR COUNT CLOCK signal increments the group counter when the SCNC COUNT GROUP NO signal is true and the units counter when the SCNC COUNT UNITS signal is true.

The SCNR DIRECTED DATA (directed data) flip-flop is used in the selection of the data line number. When the central processor generates the data line number during the execution of a DATAO

instruction, the selected group number is routed to the group directed data switch via IOB 12 (1) through IOB 14 (1) and the selected units number is routed to the units directed data switch via IOB 15 (1) through IOB 17 (1). At the same time, a 1 is routed from the central processor over IOB 11 (1) and after buffering, the resultant signal, RIO IOBR 11 (1), is used to condition the set gate of the directed data flip-flop. With the set gate conditioned, the directed data flip-flop is set by the DLS DATAO CLR signal. The set side of the directed data flip-flop enables the group and units control switches to select the group number and unit number that was directed by the central processor. These numbers are then used in the selection of the data line.

To clear the directed data flip-flop, the CNTR DATAO SET DLY signal is generated 85 ns after the IOB DATAO SET signal and is routed to the clear side of the directed data flip-flop and the flip-flop is cleared by the trailing edge. When the directed data flip-flop is cleared, the zero side of the directed data flip-flop enables the group and units control switches to select the group number and units number stored in the group and units counters, respectively. At this time, the control of the data line selection is returned to the scanner.

3.2.11 D-BS-DC10A-0-WIO

This drawing shows the write I/O bus gates that are used to gate data onto the I/O bus during the performance of a DATAI or CONI instruction.

During the execution of a CONI instruction, the DLS CONI signal gates the following data through the associated data gates of the data mixers; the resultant data are applied to the write I/O bus gates: the DAT 2 IOBW 30 (1) signal is true if the DTR DIS switch is on; the DAT 2 IOBW 31 (1) signal is true if the interrupting data line transmitter flag is set; the DAT 3 IOBW 32 (1) is true if the interrupting data line receiver flag is set; the octal PI channel number is contained in the DAT 3 IOBW 33 (1), DAT 4 IOBW 34 (1) and DAT 4 IOBW 35 (1) signals. The DLS CONI signal is used to generate the CNTR WRITE IO BUS signal and the data are gated through the write I/O bus gates and to the central processor via the I/O bus.

During the execution of a DATAI instruction, the interrupting line number, either a 5-bit or 8-bit teletype character, and a signal that identifies a receiver interrupt is routed to the central processor via the I/O bus. The interrupting line number stored in the group and units counter is routed to the write I/O bus gates associated with IOB 12 (1) through IOB 17 (1). Signal DLS DATAI is ANDed with the CNTR RCVR FLAG (1) signal; the resultant signal is routed to the write I/O bus gate associated with IOB 27 (1). When the interrupting line has a receiver flag in the set condition, the CNTR RCVR FLAG (1) signal is true, the resultant signal from the AND gate is true, and a 1 is routed to the central processor when the CNTR WRITE IO BUS signal is generated. The DLS DATAI signal gates either a 5- or 8-bit teletype character from the interrupting line group through the associated data gates in the data mixers;

the resultant data are applied to the write I/O bus gates. The write I/O bus gates associated with IOB 31 (1) through IOB 35 (1) receive the 5-bit character; or the write I/O bus gates associated with IOB 28 (1) through IOB 35 (1) receive the 8-bit character. At the same time, the DLS DATAI signal is used to generate the CNTR WRITE IO BUS signal which enables the write I/O bus gates. With the write I/O bus gates enabled, the data are routed to the central processor via the I/O bus.

3.2.12 D-MU-DC10A-0-MU

This two sheet drawing shows the module utilization charts. Each module and cable is identified by module number and by a brief functional description. To locate a module or cable, it should be remembered that the topmost row of the DC10A is the A row and that card slot 32 is located at the extreme left when viewed from the rear inside of the cabinet or the extreme right when viewed from the front of the cabinet.

3.2.13 D-BS-DC10B-0-COMM

On this drawing, the control and data cables that interface the DC10B with the DC10A and the common control circuits for the 8-line group unit are shown. At D5 through D7, the clock option card and its associated input and output lines are shown. The three baud rate clock frequencies generated in the DC10A are routed to the clock option card via the control cable. At the clock option card, a jumper is used to route the desired clock frequency to each of the eight clock lines.

The line number decoder is shown at B4 through C5. The octal line number associated with the selected data line is routed from the DC10A to the line number decoder in all line groups via six lines of the control cable. At the same time, the group enable signal is routed from the DC10A to the line number decoder in the selected line group via the control cable. When the group enable signal is true, the line number decoder is enabled, the line number is decoded, and the line enable signal for the selected data line is generated. The line enable signal is routed to the teletype receiver and the teletype transmitter associated with the selected data line.

3.2.14 D-BS-DC10B-0-L01 Through D-BS-DC10B-0-L67

This series of four drawings shows the eight data line circuits of the DC10B. The operation of each of the eight data line circuits is identical, except each data line has its own associated line enable signal and clock line. The clock frequency on each of the clock lines is selected through the use of a jumper on the clock option card; the line enable signal for the selected data line is generated by the line number decoder. Since the operation of all data line circuits is identical, a general description of a typical data line circuit is provided and is intended to cover the operation of all data lines.

Refer to the data line circuit for data line 0, located at A5 through D7 of drawing DC10B-0-L01, for the following discussion of circuit operation. This circuit consists of a W706 Teletype Receiver module, a W707 Teletype Transmitter module, a W708 Teletype Interface (clock) module, and associated circuits. From the engineering drawing, it may be observed that all receiver and transmitter modules share a common data bus; over this data bus, data are transferred in a parallel fashion. During an DATAO instruction, the central processor receives data from the receiver module via the DC10A.

Since the teletype receiver and transmitter modules operate independently of each other when the data line is operated in full-duplex, this type of operation is assumed at this time. The operation of the receiver module is explained first, and is followed by a discussion of the transmitter module operation. Following these discussions, the differences in the half-duplex and full-duplex with local copy operations are explained.

The keyboard of a device is connected to the appropriate keyboard terminal as follows: KYBD EIA terminal, if the output levels of the device conform to EIA Standard; RS-232-B; KYBD (DC) + and KYBD (DC)−, if the device operates with a local line. The receiver module monitors the serial input line (terminal AF), and when a start element of a teletype character is detected, the clock enable signal (Terminal BJ) enables the external W708 Clock Module. A clock signal from the clock module is routed to the receiver module (terminal BS) and is used to clock the incoming teletype character. As the serial bits of the teletype character are received, they are sampled and loaded into a buffer in the receiver module. One-half unit after the start of the 8-bit, the receiver flag is set (terminal AP).

Since all the flag lines in the line group are collector ORed together, the SCAN GROUP signal is true and is routed to the scanner in the DC10A. The scanner scans the line groups and, upon locating the SCAN GROUP signal from the interrupting group in the true condition, the scanner sequentially strobes the data lines of the interrupting group. When the flag strobed line (terminal AH) of the interrupting receiver module is strobed, the RCVR FLAG STROBED signal (terminal AN) becomes true. At this time, the scanner stops and initiates a program interrupt that is routed to the central processor.

The central processor services the interrupting receiver module by performing a DATAI instruction on a priority basis. During the DATAI instruction, the UNLOAD RCVR signal is generated in the DC10A and the LINE ENABLE signal is generated by the line number decoder. The UNLOAD RCVR and LINE ENABLE signals are ANDed and the resultant signal is applied to terminals BT and AD of the teletype receiver module.

With the signal at terminal BT true, the data in the receiver module buffer are transferred onto the data bus in a parallel fashion and the data on the data bus are routed to the central processor via the DC10A. At the same time, the signal at terminal AD clears the receiver flag and the receiver module is ready to receive another teletype character.

The central processor performs a DATAO instruction under program control to transfer data to the transmitter module. After the first character is transferred, the transmitter module sets its flag (terminal AD) to indicate that it has sent out the character and that the next character transfer may be performed. This action is repeated until all data are transferred. At this time, the central processor performs a DATAO instruction (with IOB bit 27 a 1 which inhibits the TRANS ENABLE signal) to clear the transmitter flag and release the scanner.

To transfer data to a transmitter module under program control, the central processor transfers the data line number and the data to the DC10A via the I/O bus during a DATAO instruction. In the DC10A, the directed data-line number is used to generate the selected group enable signal and the data line number. The data are routed through the DC10A and are placed on the data bus to the selected line group. The group enable signal and the data line number are routed to the line number decoder in the selected line group and the LINE ENABLE signal for the selected data line is generated. During the DATAO instruction, the DC10A also generates the LOAD TRANS and TRANS ENABLE signals. The LOAD TRANS signal is ANDed with the LINE ENABLE signal for the selected data line and the resultant signal is routed to terminals BE and AU of the transmitter module associated with the selected data line. At this time, the signal at terminal BE loads the data on the data bus into the buffer of the transmitter module, the signal at terminal AU clears the transmitter flag to free the scanner, and the TRANS ENABLE signal enables the serial transfer circuit of the transmitter module. The start and stop elements are assembled with the data to form a teletype character and the teletype character is transferred to the printer serially via the serial line (terminal AH). The serial transfer is clocked by the clock signal (terminal BD). The printer of the device is connected to the appropriate printer terminals as follows: the PRNTR EIA terminal is used, if the input levels of the device conform to EIA Standard RS-232-B; PRNTR (DC) + and PRNTR (DC)– terminals are used if the device operates with a local line. One-half unit after the stop element is placed on the serial line, the transmitter module indicates it is ready to receive another character by setting its flag (terminal AL) and the SCAN GROUP signal becomes true.

The scanner scans the line groups until it reaches the scan group line from the interrupting line group. Then, the scanner strobes each data line in the interrupting line group sequentially until the interrupting transmitter module is strobed (terminal AV). At this time, the TRANS FLAG STROBED signal from the interrupting line group becomes true and stops the scanner. The scanner initiates and routes a program interrupt to the central processor.

After determining that the interrupting data line is ready to receive additional data, the central processor performs a second DATAO instruction under program control and routes the next character to the interrupting transmitter module via the DC10A. During the second DATAO instruction, the data line number stored in the scanner is used to generate the necessary signal, and the central processor is not required to direct the data line number. Except for this one point, the second DATAO instruction is performed in the same manner as the first.

The central processor continues to perform the second type of DATAO instruction on a priority interrupt basis and routes data to the interrupting transmitter module one character at a time.

After all information has been transferred to the interrupting data line, as directed by the program, the central processor performs a third type of DATAO instruction during which clears the transmitter flag but transfers no data. During this type of a DATAO instruction, data are not placed on the data bus and the TRANS ENABLE signal is not generated. The LOAD TRANS signal is ANDed with the LINE ENABLE signal for the interrupting line and the resultant signal at terminal AU clears the transmitter flag. Once the transmitter flag is cleared, the central processor must direct additional servicing of this data line under program control.

In the above discussions, it was assumed that the data line was operating as a full-duplex line. When a data line is operated in half-duplex or full-duplex with local copy mode, circuit operation is slightly different because the transmitter module should not operate when the keyboard is in use. In these modes, the half-duplex jumper for the data line is inserted between its assigned terminals on the half-duplex option card to connect the WAIT line from the clock module to the transmitter module (terminal AM). With the half-duplex jumper in place, the transmitter module is loaded in a similar fashion, but its serial transfer circuit is disabled if the receiver module is operating. When the receiver module stops, the serial transfer circuit of the transmitter module is enabled and the character is transferred from the transmitter module to the printer via the serial line. In half-duplex operation, the transmitted character will be received by the receiver module and both will cause an interrupt at the end of the character (the receiver module first, the transmitter module one unit later).

CHAPTER 4
MAINTENANCE

4.1 SCOPE

Maintenance of the DC10 Data Line Scanner consists of preventive maintenance procedures that are performed periodically, adjustment procedures that are performed periodically or when a malfunction is located in the associated circuit, and troubleshooting procedures that are performed in the event of equipment malfunction. The procedures presented here assume that maintenance personnel are familiar with the data line scanner theory of operation contained in Chapter 3 of this manual, PDP-10 input/output programming described in the PDP-10 Handbook, data line scanner programming notes contained in Section 2.4 of this manual, and the operating principles of teletype systems.

4.2 EQUIPMENT REQUIRED

The test equipment required for maintenance activities is listed in Table 4-1. Only special maintenance equipment is listed, because standard hand tools, cleaners, test cables and probes are considered a part of every well-equipped maintenance activity.

Table 4-1
Special Maintenance Equipment

Equipment	Manufacturer	Model
Dual-Trace Oscilloscope 0.1V sensitivity, 15MHz frequency response	Tektronix	453, 454, 540 series, 580 series with dual trace plug-in units as required
Dual-beam Oscilloscope with viewing hood and plug-in units (See Note)	Tektronix	Type 551 with viewing hood and a CA or 1A1 plug-in unit
Module Extender	DEC	G998 or W980
Data Line Scanner Diagnostic Program Tape	DEC	MAINDEC-10-D2CC-D
Teletype Machine (See Note)	Teletype Corporation	ASR 33 or ASR 35

NOTE: The dual-beam oscilloscope and the ASR Teletype are not normally required. However, they are the only practical way of troubleshooting timing problems related to the time scale of the Teletype, due to the low-duty cycle and high-timing jitter involved. A suitable alternative to the dual-beam oscilloscope is a high-frequency, dual-trace or high-frequency chopping storage oscilloscope.

The following oscilloscopes in addition to the Tektronix 551 listed are suitable for this purpose:

1. Hewlett-Packard 141A with 1401A or 1402A plug-in unit and a suitable time base plug-in unit (not suitable for 10 μs signals)

2. Marconi TF2202 with two TM 6962 amplifiers, suitable time base plug-in unit and TD39601 visor (6MHz bandwidth)

3. Tektronix 555 or 556 with high-frequency vertical plug-in unit and suitable time base plug-in unit

4. Tektronix 564 with a 3A6 plug-in unit and suitable time base (not suitable for 4 microsecond signals)

5. Tektronix 565 with two 3A6, 3A7 or 3A8 plug-in units

4.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the DC10 Data Line Scanner and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks forestalls possible future failure by correcting minor damage and discovering progressive deterioration at an early stage. A log book used to record data found during the performance of each preventive maintenance task will indicate the rate of circuit deterioration and provide information which will enable maintenance personnel to determine when components should be replaced to prevent failure of the equipment. These tasks consist of the following checks: mechanical checks which include cleaning and visual inspections; power supplies checks; clock and delay module timing checks and adjustments; and margin checks which aggravate border-line conditions or intermittent failure so that they can be detected and corrected. All preventive maintenance tasks should be performed as a function of conditions at the installation site and the down-time limitations of equipment use. Perform the mechanical checks at least once each month or as often as required to maintain efficient functioning of the cooling equipment. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. For a typical application, a schedule of every four months or 1000 equipment operating hours, whichever occurs first, is suggested.

4.3.1 Mechanical Checks

The following steps should be performed during a mechanical check; the indicated corrective action should be performed, if a substandard condition is located.

a. Clean the exterior and the interior of each equipment cabinet housing the data line scanner by using a vacuum cleaner or clean cloths moistened in nonflammable nonconductive solvent. Be sure the solvent is not harmful to paint.

b. Clean dirt from the blower assemblies while using care not to damage cable assemblies or modules.

c. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas.

d. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring.

e. Inspect each row of modules to assure that each module is securely seated in its connector.

f. Verify that the proper I/O bus cables and all other interconnecting cables are firmly seated in their respective connectors.

g. Inspect power supply capacitors for leaks, bulges, or discolorations. Replace any capacitors giving these signs of malfunction.

4.3.2 Power Supply Checks

The data line scanner contains two types of power supplies. A DEC 779 or 779A Power Supply provides the power for the logic modules and a DEC 12-05949 Power Supply provides the power for the integrated circuits located in the DC10B. Check the output voltage and ripple content of the supplies and assure that they are within tolerances. Use a multimeter to check the output voltages without disconnecting the load and use an oscilloscope to measure the peak-to-peak ripple content on the dc output.

DEC 779 or 779A Power Supply - Check the two output voltages from this supply at the logic end. These voltages are not adjustable, so if the output voltage or ripple content is not within the tolerance specified, the supply is considered defective and troubleshooting procedures should be performed.

Check the +10V output between the red (+) and black (-) wires to assure that it is between +9.5 to +11.0V with less than 800 mV rms ripple. Check the -15V output between the blue (-) and black (+) wires to assure that it is between -14.5 and -16.0V with less than 1000 mV rms ripple. Note that the black wires are grounded at the logic frame and the power distribution strip.

DEC 12-05949 Power Supply - Check the output of the integrated circuit power supply between terminal J of module A15 in the DC10B to assure that it is +3.6V ±5%. This power supply has a voltage set adjustment that should be used if the output voltage is not within the stated tolerance. Adjust so that all ripple, noise, etc., is centered in the range of +3.42V to +3.78V and does not exceed this range.

4.3.3 Clock and Delay Adjustments

The number of clock and delay adjustments in the data line scanner have been kept to a minimum through careful equipment design but, of course, all adjustments could not be eliminated. In the following paragraphs, the scanner clock and indicator clock delay one-shot adjustment procedures are detailed. Then, the procedures for checking and adjusting the data terminal ready one-shot and the indicator one-shots are explained.

4.3.3.1 Scanner Clock Check and Adjustment - This procedure should be performed when the scanner clock module is replaced or when the scanner clock timing is suspected to be out of tolerance. To perform this procedure, perform the following steps:

a. Turn data line scanner power on.

b. Connect one channel of an oscilloscope dual-trace pre-amp to pin F07D of the scanner clock module (a type R401 module located at F07 of the DC10A).

c. Adjust oscilloscope to obtain a waveform on the oscilloscope that is similar to the scanner clock waveform shown in Figure 4-1.

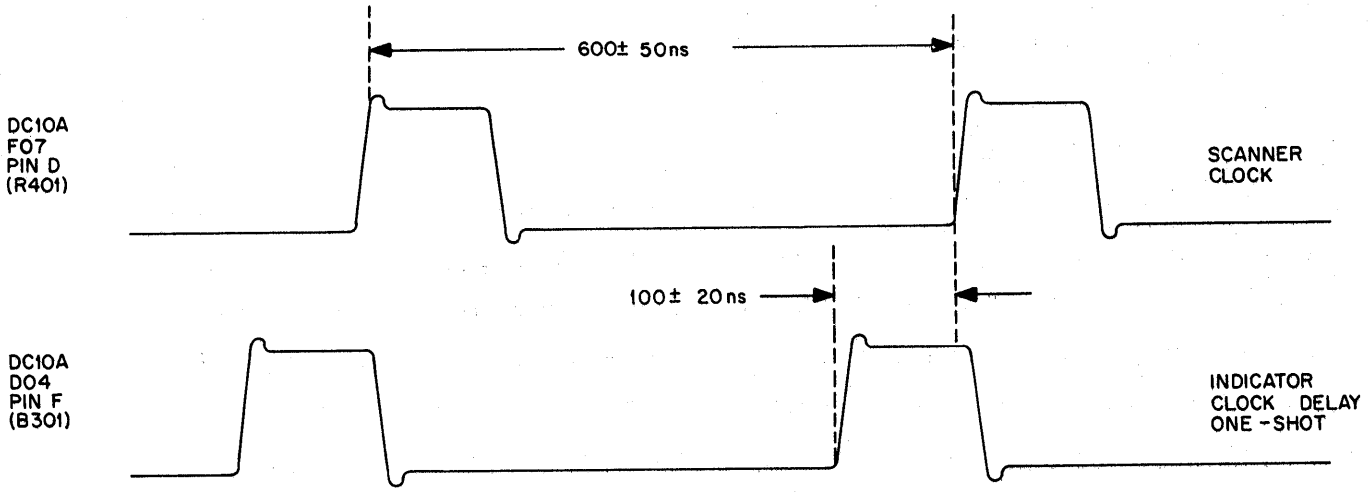


Figure 4-1 Scanner Clock Adjustment

d. Measure the time of one cycle to assure it is equal to 600 ±50 ns.

CAUTION

High voltage is present in the DC10 even though the logic power is turned off.

e. If the scanner clock waveform is out of tolerance, gain access to the scanner module through the rear of the DC10A cabinet and adjust the trimpot to bring the waveform within the tolerance. Use caution to avoid short circuiting or damaging the logic or the modules.

f. Leave the oscilloscope connected to pin D of the scanner clock module and perform the indicator clock delay one-shot check and adjustment procedure with the second scope probe.

4.3.3.2 Indicator Clock Delay One-Shot Check and Adjustment - This procedure is performed after the scanner clock has been adjusted. Perform the following steps:

a. Perform, but do not repeat, the scanner clock check and adjustment procedure.

b. Connect the second channel of the oscilloscope dual-trace preamp to pin D04F of the indicator clock delay one-shot module (Type B301 module located at D04 of the DC10A).

c. Adjust the oscilloscope to obtain a waveform on the oscilloscope that is similar to the indicator clock delay one-shot waveform shown in Figure 4-1.

d. Measure the time between the two waveforms as shown in Figure 4-1 to assure it is equal to 100±20 ns.

CAUTION

High voltage is present in the DC10 even though the logic is turned off.

e. If the waveform is not within the stated tolerance, gain access to the indicator clock delay one-shot module and adjust the trimpot to bring the waveforms within the tolerance. Use caution to avoid short-circuiting or damaging the logic or the modules.

4.3.3.3 Data Terminal Ready One-Shot Check and Adjustment - The DLS DATA TRM RDY one-shot (R303) module located at E11 of the DC10A) should be set for 500 ms. Part T6 of the DLS diagnostic program MAINDEC-10-D2CC-D sets the DLS DATA TRM RDY one-shot every 2s. Thus, DC10A pin E11D should be negative for 500 ms and at ground for 1500 ms when this test is performed and when the DTR DIS switch is off. To adjust the one-shot, perform part T5 of the DLS diagnostic program and adjust the one-shot by reducing the delay until pin E11D is not continuously negative and then increase the delay until pin E11D is negative all the time. This procedure will set the DLS DATA TRM RDY one-shot to approximately 500 ms.

4.3.3.4 Indicator One-Shot Check and Adjustment - The IND TRANS DEL (Type R303 module located at E03 of the DC10A), and IND RCVR DEL (R303 module located at E04 of the DC10A) one-shots are most conveniently adjusted by placing the DLS in the maintenance mode (MAINT switch in the up position) and typing characters on a Teletype connected to the DLS. Connect one probe of an oscilloscope dual-trace preamp to DC10A pin E03D and the other probe to DC10A pin E04D. Alternately adjust the one-shots with their associated trim pots while typing on the Teletype until both delays have been adjusted to approximately 100 ms. These adjustments are not critical because they do not affect the performance of the DLS.

4.3.3.5 Telegraph Line Current Check and Adjustment - The total dc circuit resistance of a telegraph line is adjusted to obtain the desired line current. Perform the line current adjustment procedure described in Section 2.5.2.7 to check the line current. When a defective Type G854 Telegraph Line Module is replaced, the strapping must be inserted and the line current adjustment procedure performed.

4.3.3.6 Telegraph Line Bias Current Check and Adjustment - The operating point of each polar relay is established by adjusting the bias current. To perform a bias current check, complete the bias current adjustment procedure in Section 2.5.2.7. This procedure should be performed when a defective Type G854 Telegraph Line Module or polar relay is replaced.

4.3.4 Margin Checks

Margin checks are performed to aggravate borderline conditions within the logic circuits, thereby revealing solid observable faults. In this way, marginal conditions can be corrected to forestall equipment downtime. Margin checks can also be used as a troubleshooting aid for locating marginal or intermittent components. Checks may be performed by varying the logic voltages manually at the margin control panel of the central processor while performing a diagnostic procedure under program control.

CAUTION

The voltage on the +3.6V input to the integrated circuit modules (W706, W707, and W708) should never be allowed to exceed +4.5V because the integrated circuits may be permanently damaged.

The integrated circuits may be margined by varying the voltage set adjustment on the 3.6V power supply.

4.4 CORRECTIVE MAINTENANCE

The data line scanner is constructed of highly reliable transistorized modules and standard circuits. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment downtime due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the system. Maintenance personnel should become thoroughly familiar with the theory of operation described in Chapter 3 of this manual, specific circuit modules described in the DEC Logic Handbook, the engineering drawings contained in Volume 2 of this manual, and the location of mechanical and electrical components described in Chapter 1.

Diagnosis and remedial action for a malfunction are performed in the following phases:

a. Preliminary investigation to gather all information and to determine the mechanical and electrical security of the data line scanner.

b. System troubleshooting to isolate the malfunction to a module through the use of diagnostic programming, signal tracing, or aggravation techniques.

c. Module troubleshooting to locate defective components within a module.

d. Repairs to correct the cause of the malfunction.

e. Validation test to assure that the malfunction has been corrected.

f. Log entry to record pertinent data.

4.4.1 Preliminary Investigation

It is virtually impossible to outline any specific procedures for locating malfunction within the data line scanner. Before beginning troubleshooting procedures, explore every possible source of information. Ascertain all possible information concerning any unusual function of the system prior to the malfunction and all possible program information such as the routine in progress, the condition of the indicators, etc. Search the maintenance log to determine if this type of malfunction has occurred before or if there is any cyclic history of this type of malfunction, and determine how this condition was previously corrected. When the entire data line scanner fails, perform a visual inspection to determine the mechanical and electrical integrity of all power sources, cables, connectors, etc. Assure that the power supplies are operational by performing the power supply checks as described under Preventive Maintenance.

4.4.2 System Troubleshooting

Do not attempt to troubleshoot the data line scanner without first gathering all information possible concerning the malfunction, as outlined under Preliminary Investigation.

Commence troubleshooting by repeating the operation during which the malfunction was initially observed, using the same conditions. Thoroughly check the operating conditions for proper control settings and note the operation of all indicators before and at the time of malfunction. Careful checks should be performed to assure that the system is actually at fault before continuing the corrective maintenance procedures. Loose or faulty cable connections can often give indications very similar to those caused by internal malfunctions. Faulty ground connections between pieces of equipment are a common source of trouble. The data line scanner must be properly grounded to prevent high voltage transients.

If the malfunction has been determined to lie within the data line scanner, but cannot be localized to a specific logic function, perform the diagnostic program procedure. When the malfunction has been isolated to a specific logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the malfunction is intermittent, a form of aggravation test should be employed to locate the malfunction.

The data line scanner flow chart supplied in Volume 2 of this manual is very useful in system troubleshooting. This chart illustrates the events that occur during normal operation and the sequence of the events. When an event does not occur at the proper moment, all possible conditions leading up to its

schedule occurrence can be located on the flow chart and can be checked for normal operation. All such information can be related to individual logic elements on the block schematics by cross references on the flow diagram.

Diagnostic Program - The most efficient means of troubleshooting the data line scanner makes use of the diagnostic program described in MAINDEC-10-D2CC-D. This routine provides a complete test of the data line scanner under operational conditions.

Signal Tracing - If a malfunction has been isolated to a specific logic element, program the central processor to repeat an instruction in which all functions of that logic element are utilized. If the central processor cannot be used for the required test, control flip-flops or register flip-flops can be cleared or set manually by momentarily placing a ground to the appropriate flip-flop output terminal. Counting operations of registers can be checked by grounding the appropriate DCD inputs to provide clocking of the registers. Under these conditions, use the oscilloscope to trace signal flow through the suspected logic element. The oscilloscope sweep may be synchronized with data-line scanner control signal by connecting the trigger input of the oscilloscope to the appropriate module terminal. Trace output signals from the connector to its final destination. The signal-tracing method can be used to determine with certainty the quality of pulse amplitude, duration, rise time, and the correct timing sequence of the signal. If an intermittent malfunction occurs, signal tracing should be combined with an appropriate form of aggravation test.

Intermittent Malfunctions - Intermittent malfunctions caused by poor wiring connections can often be revealed by tapping the modules while running a repetitive routine, such as the diagnostic program. Often, wiping the handle of a screwdriver across the back of a suspect row of modules is a useful technique. By repeatedly starting the program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector, the module connector for wear, misalignment, and malfunction, and the module wiring for a poor connection.

4.4.3 Module Troubleshooting

The procedure followed for troubleshooting and correcting the cause of a malfunction within modules and power supplies depends upon the downtime limitations. Where downtime must be kept at a mimum, it is suggested that a replacement parts program be adapted to maintain at least one spare module or power supply which can be inserted into the cabinet when system troubleshooting procedures have traced the fault to a particular component. A list of modules and power supplies is compiled from the engineering drawings contained in Volume 2 of this manual.

CAUTION

High voltage is present in the DC10 even though the logic power is turned off.

On-Line Dynamic Tests - Where downtime is not critical, the spare parts list can be reduced and signal tracing techniques can be utilized to troubleshoot modules. This type of procedure is performed as follows: remove suspected module; insert module extender into the module connector; insert suspected module into the module extender; and perform signal tracing procedure with an oscilloscope while the equipment is operated in a routine which exercises the module circuits.

4.4.4 Repair

For minimum system downtime, replace defective modules and/or system components that have been located during system troubleshooting procedures. When system downtime is not critical and module troubleshooting procedures are employed, perform repairs using good shop practices. Remove defective components by cutting the component leads and removing the leads from the printed board with a solder sucker. When soldering semiconductor devices, use a heat sink and the smallest soldering iron adequate for the work. Perform all soldering operations in the shortest possible time to prevent damage to components. Replace defective components with components of equal or greater quality or closer tolerance. Replace defective cross-connecting or interconnecting Teletype wiring using the 66A or 317B tool supplied with each system. When terminating wire, orient the tool so that it cuts the excess end of the wire rather than the active conductor.

4.4.5 Validation Test

Following the replacement of any electrical component, a test should be performed to assure the correction of the malfunction and to make necessary adjustments. This test should be taken from the preventive maintenance procedure most applicable to the portion of the system in which the malfunction was located. Normally, the diagnostic program serves this purpose if the malfunction was located in a logic element pertaining to data transfer functions. If the malfunction was located in control element, the control function should be checked by manually setting and clearing or by programmed exercise of the function.

When time permits, it is suggested that the entire preventive maintenance task be performed as a validation test. The reasons for this are as follows: other components may be marginal; while the equipment is down and available, preventive maintenance can be performed and need not be rescheduled for the normal period.

4.4.6 Log Entry

Corrective maintenance procedures are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the malfunction, the method of malfunction location, and any other information which would be helpful in maintaining the equipment in the future.

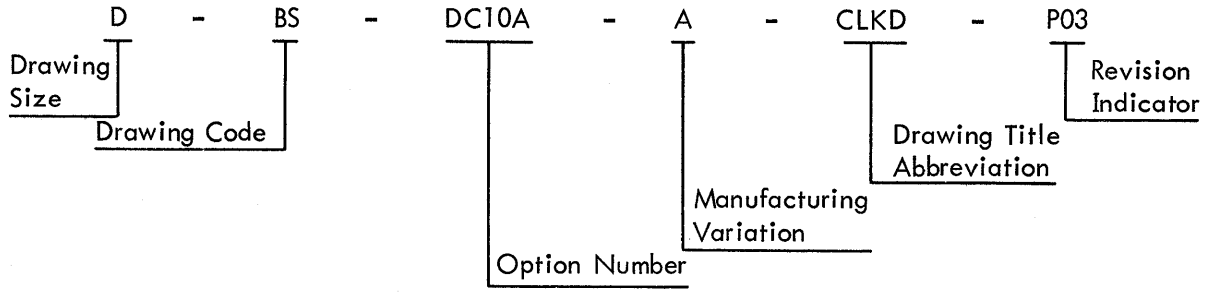
CHAPTER 5
ENGINEERING DRAWING LIST

5.1 INTRODUCTION

This chapter contains descriptions of DEC engineering drawing terminology and logic symbols and a list of applicable engineering drawings. The engineering drawings are contained in Volume 2 of this manual. In addition, a complete set of full-size drawings is supplied with each system. Should any discrepancy exist between the drawings in Volume 2 of this manual and those supplied with the equipment, assume the full-size drawings are correct. The full-size drawings should be used by maintenance personnel for work on the data line scanner because they show the variations peculiar to an individual installation. Replacement schematics are furnished for test and maintenance purposes. The circuits on these drawings are proprietary in nature and should be treated accordingly.

5.2 DRAWING TERMINOLOGY

The engineering drawing numbers for the data line scanner contain six fields of information, separated by hyphens. A typical example of a drawing number is shown below. Example:



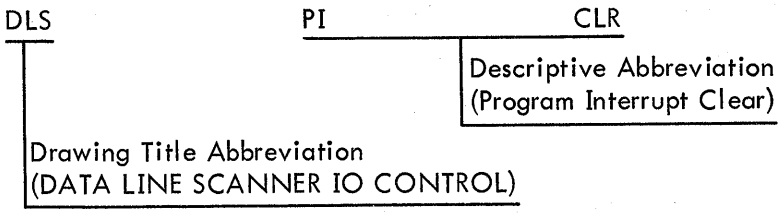
The drawing size, option number, and the drawing title abbreviation are self-explanatory. The manufacturing variation letter identifies the variation that the drawings reflect. For example: 0 reflects drawing applicable to all variations; A reflects the 60 Hertz equipment; etc. The drawing code identifies the type of drawing. A list of the common drawing codes follows.

1. BS - Block Schematic or Logic Diagram
2. CL - Cable List
3. CS - Circuit Schematic
4. FD - Flow Diagram
5. IC - Interconnection Drawing

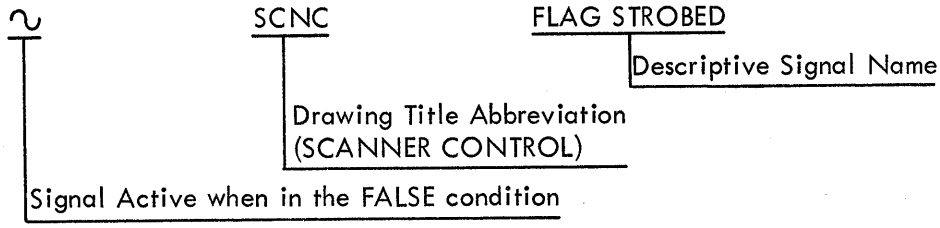
6. KS - Key Sheet
7. MU - Module Utilization
8. RS - Replacement Schematic
9. SD - System Diagram
10. TD - Timing Diagram
11. WD - Wiring Diagram

Signal names on the drawings cross reference the signal to the drawing where the signal originates. Two typical examples of signal names are shown below.

Example 1:



Example 2:



5.3 LOGIC SYMBOLS

The DEC standard logic symbols are shown at the input of most circuits to specify enabling condition required to produce a desired output. These symbols represent either standard DEC logic levels or standard DEC pulses. All pulses in the DC10 are R-series pulses.

Typical engineering symbols are shown in Figure 5-1.

5.4 LOGIC LEVELS

All logic signals are either standard DEC logic levels or standard DEC pulses. A standard DEC logic level is either a ground (0 to -0.5V) or -3V (-2.5 to -4.0V). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (—◇) indicates that the signal is a level and that ground represents assertion; a solid diamond (—◆) indicates that the signal is a level and that -3V represents assertion.

All logic levels applied to the conditioning-level inputs of capacitor-diode gates must be present either 100 or 400 ns (depending on the module used) before an input triggering pulse is applied to the gate.

The standard DEC negative pulse is indicated by a solid triangle (——▶) and goes from ground to -2.5 or -3V (-2.5 to -4.0V tolerances). The standard DEC positive pulse, indicated by an open triangle (——▷), goes from -3V to ground. The width of the standard pulses used in this equipment is either 100 or 400 ns, depending on the module and application.

Occasionally, the transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (—◆▷) is drawn to indicate this fact. The triangle is drawn open or solid depending, respectively, on whether the positive (-3V to ground) or the negative (ground to -3V) transition triggers circuit action. The shading of the diamond is opposite that of the triangle to indicate triggering on the trailing edge.

Any other signal is nonstandard and is indicated by an arrowhead (——⟩) pointing in the direction of signal flow.

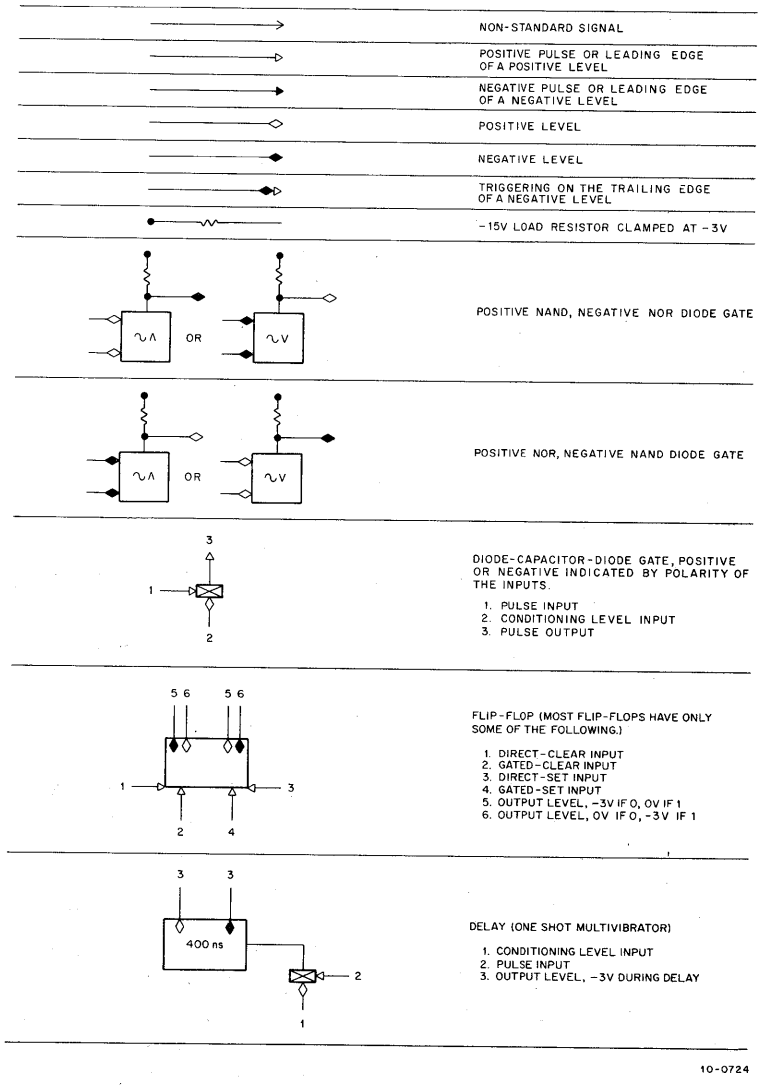
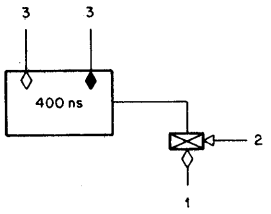


Figure 5-1 DEC Standard Logic Symbols



DELAY (ONE SHOT MULTIVIBRATOR)

1. CONDITIONING LEVEL INPUT
2. PULSE INPUT
3. OUTPUT LEVEL, -3V DURING DELAY

Figure 5-1 DEC Standard Logic Symbols (cont.)

5.5 FLIP CHIP PULSES

FLIP CHIP circuit operation in the data line scanner uses the DEC R-series pulses. The pulse produced by the R-series modules starts at -3V, goes to ground (-0.2V) for 100 or 400 ns, then returns to -3V. This pulse is idealized in Figure 5-2.

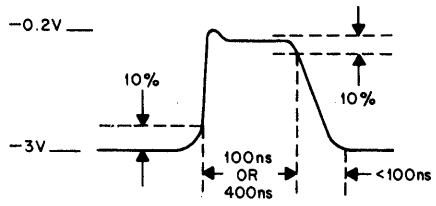


Figure 5-2 R-Series Pulse

5.6 ENGINEERING DRAWINGS

The following DEC drawings are contained in Volume 2 of this manual.

Option	Drawing Number	Title
DC10A	D-DI-DC10A-0-1	Drawing Index List
	D-UA-DC10A-0-0	Control Unit Assembly
	A-PL-DC10A-0-0	Control Unit Assembly, Parts List
	A-ML-DC10A	Master Drawing List
	D-FD-DC10A-0-FD1	Flow Diagram
	D-FD-DC10A-0-FD2	Flow Diagram
	D-BS-DC10A-0-CLKD	Clock and Control Drivers
	D-BS-DC10A-0-CNTR	Control Logic and Trans Enab
	D-BS-DC10A-0-DAT1	Data Mixers Bits 7 and 8
	D-BS-DC10A-0-DAT2	Data Mixers Bits 5 and 6
	D-BS-DC10A-0-DAT3	Data Mixers Bits 3 and 4
	D-BS-DC10A-0-DAT4	Data Mixers Bits 1 and 2
	D-BS-DC10A-0-DLS	Data Line Scanner I/O Control
	D-BS-DC10A-0-IND	Indicator

Engineering Drawings (Cont)

Option	Drawing Number	Title
DC10A (Cont)		
	D-BS-DC10A-0-LSEL	Line Select Drivers
	D-BS-DC10A-0-RIO	I/O Bus Read Logic
	D-BS-DC10A-0-SCNC	Scanner Control
	D-BS-DC10A-0-SCNR	Scanner Register
	D-BS-DC10A-0-WIO	I/O Bus Write Logic
	D-MU-DC10A-0-UML1	Module Utilization
	D-MU-DC10A-0-UML2	Module Utilization
	A-PL-DC10A-0-MC	Module Parts List
	D-IC-DC10A-0-2	Power Wiring AC and DC, 50-60 Hz
	C-AD-7006137-0-0	Cable Set DC10
	D-AD-7005466-0-0	Wired Assembly DC10A
	A-PL-7005466-0-0	Wired Assembly DC10A, Parts List
DC10B	D-DI-DC10B-0-1	Drawing Index List
	D-UA-DC10B-0-0	DC10B Unit Assembly
	A-PL-DC10B-0-0	DC10B Unit Assembly, Parts List
	A-ML-DC10B-0	Master Drawing List
	D-FD-DC10B-0-W706	Flow Diagram W706 Receiver
	D-FD-DC10B-0-W707	Flow Diagram W707 Transmitter
	D-FD-DC10B-0-W708	Flow Diagram W708
	D-BS-DC10B-0-COMM	8 Line Group Comm Control
	D-BS-DC10B-0-L01	8 Line Group Lines 0 and 1
	D-BS-DC10B-0-L23	8 Line Group Lines 2 and 3
	D-BS-DC10B-0-L45	8 Line Group Lines 4 and 5
	D-BS-DC10B-0-L67	8 Line Group Lines 6 and 7
	D-MU-DC10B-0-MU	Module Utilization List
	A-PL-DC10B-0-MU	Module Parts List
	B-CS-W708	Communications Interface W708
	C-CS-W706	Teletype Receiver W706
	C-CS-W707	Teletype Transmitter W707
	D-AD-7005502-0-0	Wired Assembly DC10B
	A-PL-7005502-0-0	Wired Assembly DC10B, Parts List
DC10C	D-DI-DC10C-0-1	Drawing Index List
	D-UA-DC10C-0-0	DC10C Unit Assembly
	A-PL-DC10C-0-0	DC10C Unit Assembly, Parts List
	A-ML-DC10C-0	Master Drawing List
	D-BS-DC10C-K01	Telegraph Relay Assembly Lines 0 and 1
	D-BS-DC10C-K23	Telegraph Relay Assembly Lines 2 and 3
	D-BS-DC10C-K45	Telegraph Relay Assembly Lines 4 and 5
	D-BS-DC10C-K67	Telegraph Relay Assembly Lines 6 and 7
	D-MU-DC10C-MUL	Module Utilization List
	A-PL-DC10C-MUL	Module Parts List
	C-AD-7005654-0-0	Wired Assembly DC10C
	A-PL-7005654-0-0	Wired Assembly DC10C, Parts List
DC10D	D-CS-DC10D-0-1	Line Power Supply Schematic

Engineering Drawings (Cont)

Option	Drawing Number	Title
DC10E	D-DI-DC10E-0-1	Drawing Index List
	C-UA-DC10E-0-0	DC10E Unit Assembly
	A-PL-DC10E-0-0	DC10E Unit Assembly, Parts List
	A-ML-DC10E-0	Master Drawing List
	D-BS-DC10E-0-EDSC	Expanded Data Set Control
	D-BS-DC10E-0-L0	Expanded Data Set Control Line 0
	D-BS-DC10E-0-L1	Expanded Data Set Control Line 1
	D-BS-DC10E-0-L2	Expanded Data Set Control Line 2
	D-BS-DC10E-0-L3	Expanded Data Set Control Line 3
	D-BS-DC10E-0-L4	Expanded Data Set Control Line 4
	D-BS-DC10E-0-L5	Expanded Data Set Control Line 5
	D-BS-DC10E-0-L6A	Expanded Data Set Control Line 6A
	D-BS-DC10E-0-L6B	Expanded Data Set Control Line 6B
	D-BS-DC10E-0-L6C	Expanded Data Set Control Line 6C
	D-BS-DC10E-0-L7A	Expanded Data Set Control Line 7A
	D-BS-DC10E-0-L7B	Expanded Data Set Control Line 7B
	D-BS-DC10E-0-L7C	Expanded Data Set Control Line 7C
	D-MU-DC10E-0-MU	Module Utilization List
	A-PL-DC10E-0-MU	Module Parts List
	D-CL-DC10E-0-ICL	Interface Cable List

READER'S COMMENTS

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DEC-10-HDCAA-B-D

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