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BA10 HARD COPY CONTROL MAINTENANCE MANUAL VOLUME I

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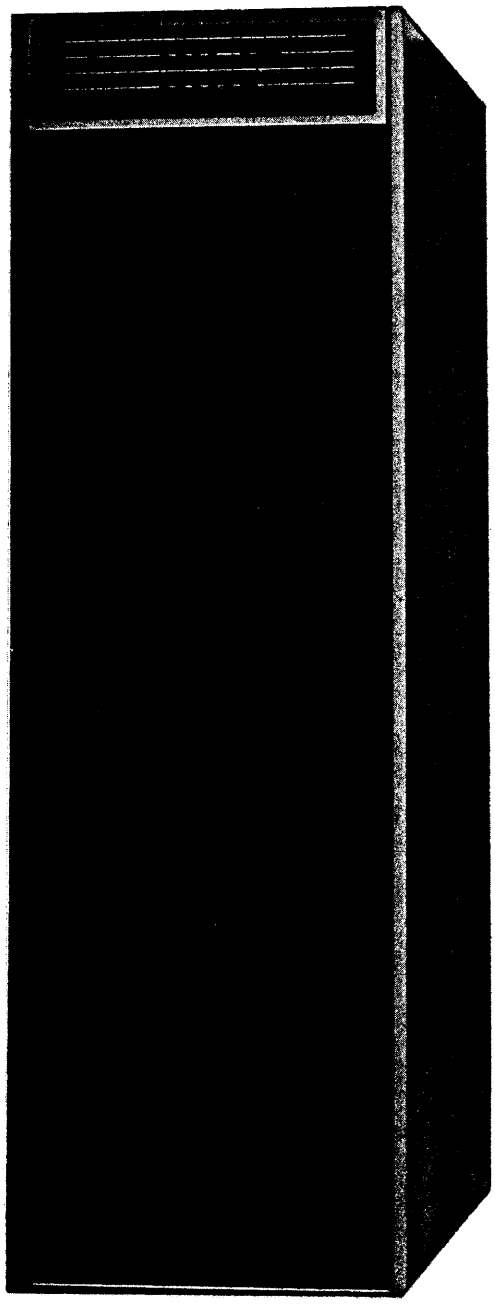


CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The BA10 Hard Copy Control is a DECsystem-10 option, which interfaces the I/O Bus with the CP10 Card Punches, CR10 Card Readers, LP10 Line Printers, and XY10 Plotters. The BA10 is capable of controlling one of each of the above devices (see Figure 1-1). When the BA10 is not present, the XY10 Control Logic may be located within the TD10 DECtape Control.

This manual and referenced documents provide information pertinent to the installation, operation, and maintenance of the BA10 Hard Copy Control, the XY10 Control Logic (if located in the TD10), and the associated electro-mechanical peripheral devices. Virtually all maintenance information for the peripheral devices is provided by separate manuals published by the respective manufacturers. Engineering drawings, (see Volume II) applicable to the BA10 include block (logic) schematics, flow diagrams, and module location diagrams.

The level of discussion in this manual assumes the reader is familiar with DEC logic, DECsystem-10 signal naming and notation, the I/O Bus (refer to the DECsystem-10 Interface Manual), and the general operation of the processor (refer to the DECsystem-10 System Reference Manual).

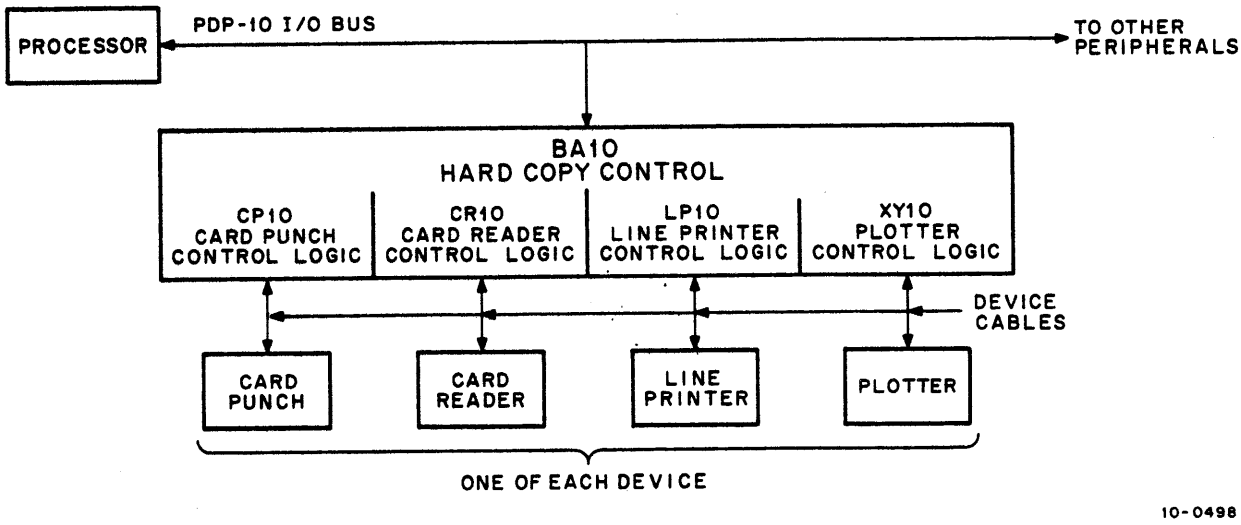


Figure 1-1 BA10 Hard Copy Control System

1.2 EQUIPMENT FEATURES

1.2.1 CP10 Card Punch Control

The CP10 Card Punch Control interfaces the CP10A Card Punch with the PDP-10 I/O Bus. This model is manufactured by Mohawk Data Sciences Corp. (formerly Soroban Engineering). (See Figure 1-2.)

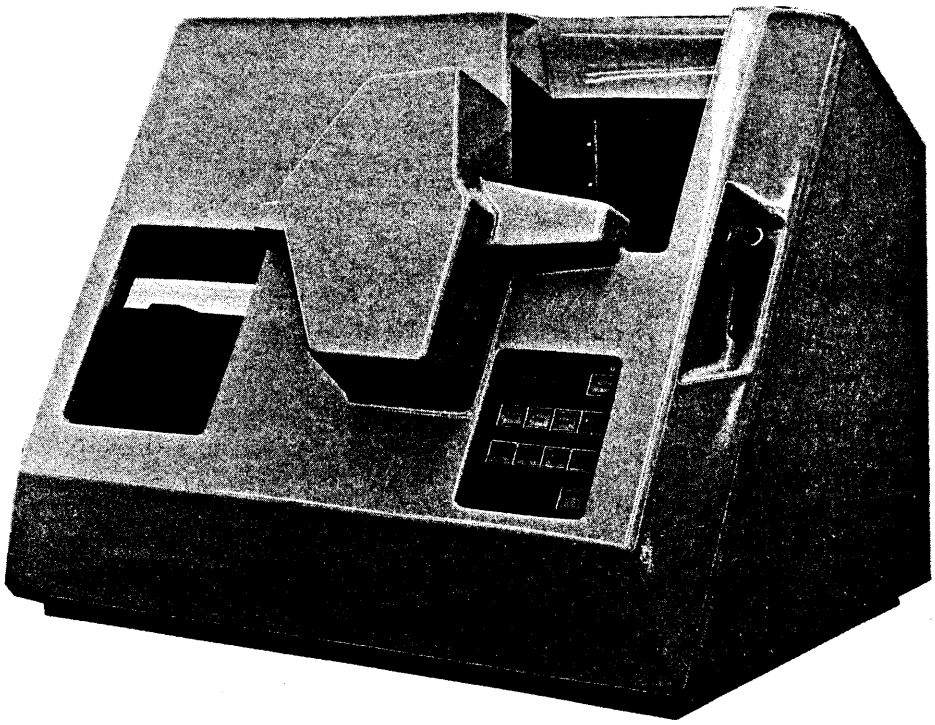


Figure 1-2 CP10A Card Punch

The CP10A Card Punch (compact model) offers the following features:

a. 200-cards-per-minute operating speed (punching all 80 columns)
b. 365-cards-per-minute operating speed (punching first 16 columns only)
c. 1000-card-capacity hopper and stacker
d. Programmable card offset
e. Column-by-column 12-bit parallel operation (code independent)
f. 50- and 60-Hz versions
g. Rugged, plug-in punch block
h. Easy access to card path
i. Standard 12-row, 80-column Hollerith cards
j. Punches four columns at a time using an interposer and cam punch mechanism.

1.2.2 CR10 Card Reader Control

The CR10 Card Reader Control interfaces the various card readers with the PDP-10 I/O Bus. The complete DEC designations for the 60- and 50-Hz versions of the card readers are as follows:

The CR10D Card Reader (Figure 1-4) offers the following features:

a. 1000 cards-per-minute continuous operating speed
b. 950 card capacity hopper/stacker
c. Standard 80-column EIA card type
d. 50- and 60-Hz versions
e. Column-by-column 12-bit parallel operation
f. Photo-transistor read station
g. Built-in error monitoring
h. Virtually jam-free picker mechanism
i. **Slant-top feature for easier loading and unloading on the fly.**

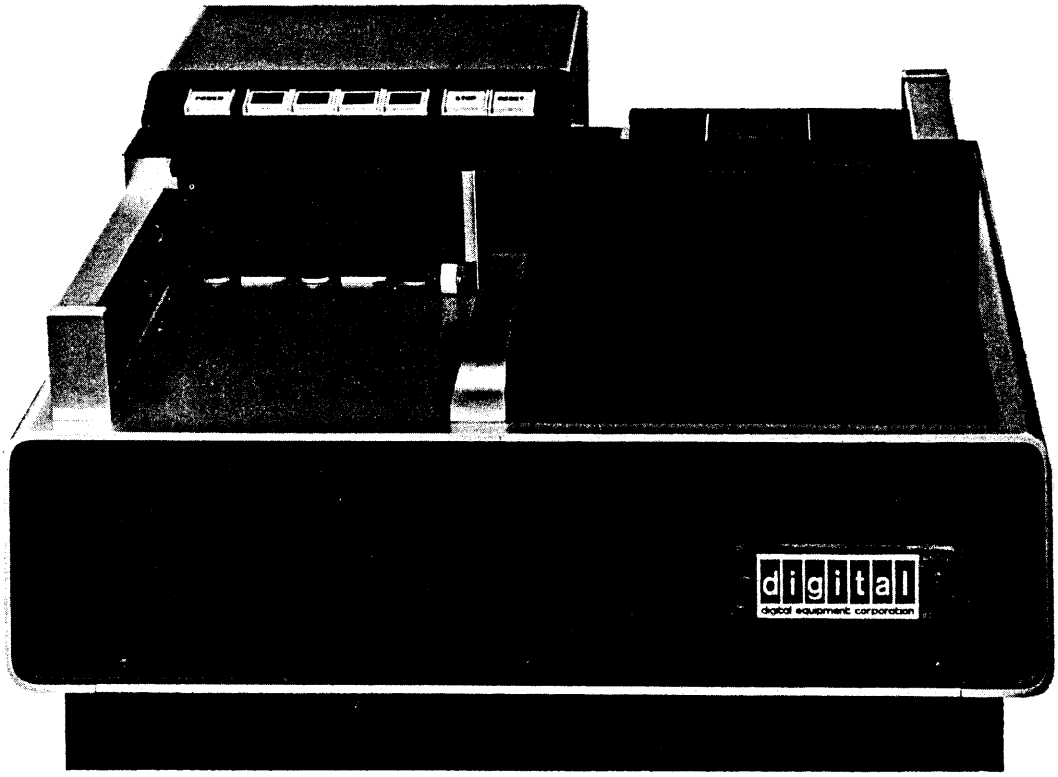


Figure 1-4 CR10D Card Reader

The CR10E Card Reader (Figure 1-5) offers the following features:

a. 1200 cards-per-minute continuous operating speed
b. 2200 card capacity hopper/stacker
c. Standard 80-column EIA card type
d. 50- and 60-Hz versions
e. Column-by-column 12-bit parallel operation
f. Photo-transistor read station
g. Built-in error monitoring
h. Virtually jam-free picker mechanism
i. End-of-file button

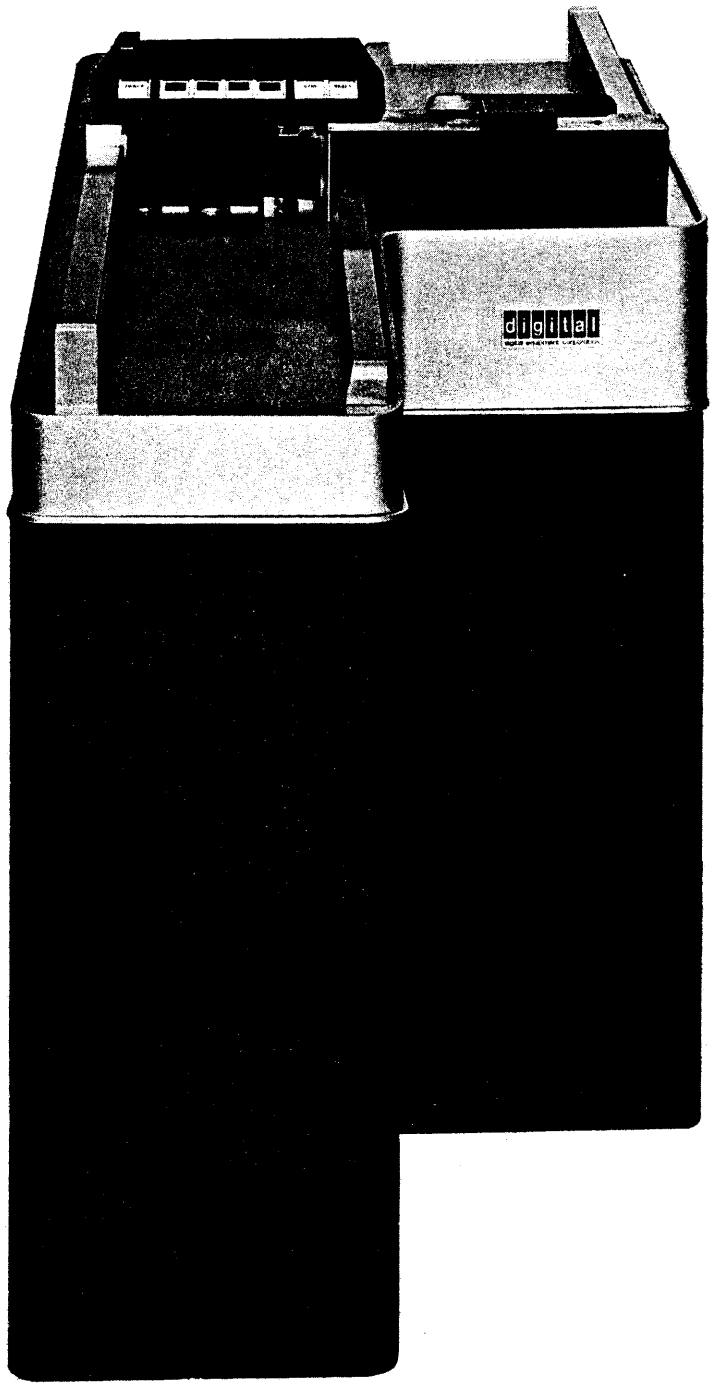


Figure 1-5 CR10E Card Reader

The CR10F Card Reader (Figure 1-6) offers the following features:

a. 300 cards-per-minute continuous operating speed
b. 550 card capacity hopper/stacker
c. Standard 80-column EIA card type
d. 50- and 60-Hz versions
e. Column-by-column 12-bit parallel operation
f. Photo-transistor read station
g. Built-in error monitoring
h. Virtually jam-free picker mechanism

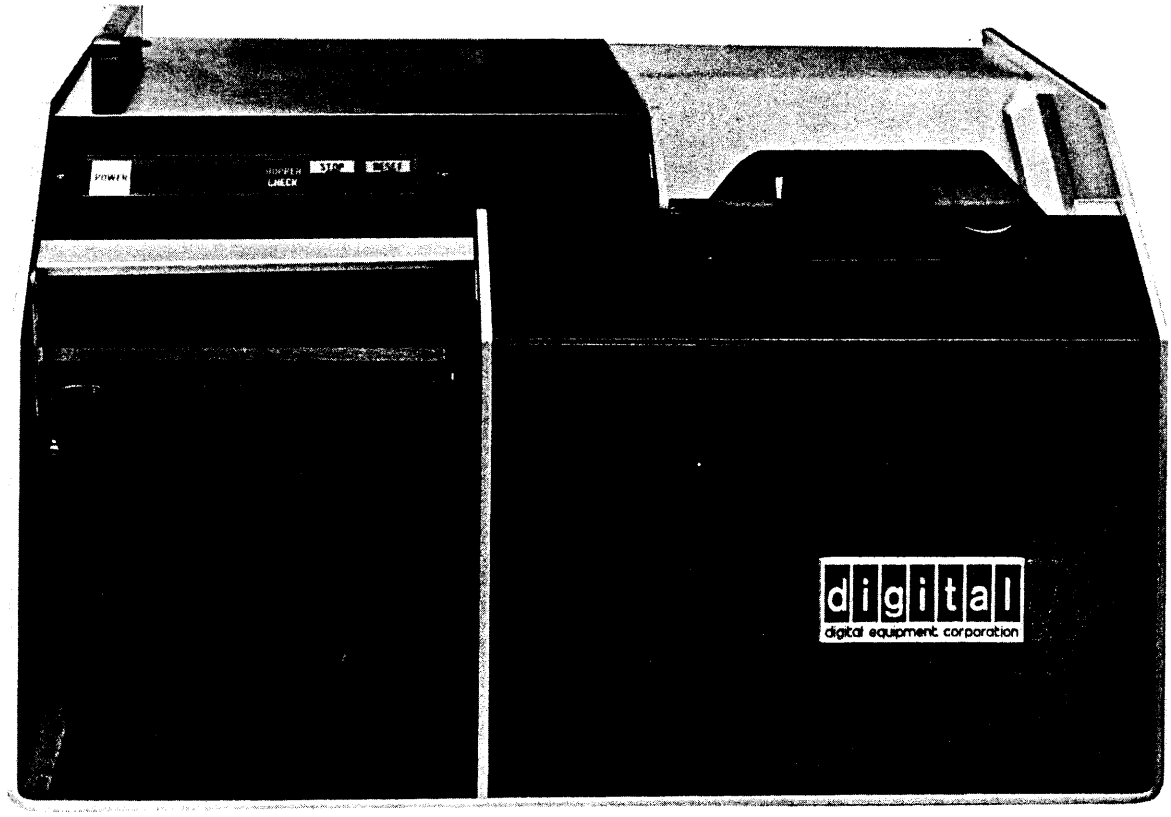


Figure 1-6 CR10F Card Reader

1.2.3 LP10 Line Printer Control

The LP10 Line Printer Control interfaces the LP10A, LP10B, LP10C, LP10D, LP10E, LP10F, or LP10H Line Printers with the PDP-10 I/O Bus. Models LP10A, LP10B, LP10C, LP10D, and LP10E are manufactured by Mohawk Data Sciences Corp. (formerly Anelex Corp.). (See Figures 1-7 and 1-8.) Models LP10F and LP10H are manufactured by Data Products Corp. (See Figure 1-9.)

Models LP10A, B, C, D, and E offer the following features:

a. 132 print columns
b. PDP-10 ASCII character set
c. 8-channel vertical format control tape
d. 50- and 60-Hz versions
e. Wide range of forms accommodated
f. Static eliminators
g. Asynchronous operation
h. Teleprinter operation simulation
i. Core memory buffer in line printer
j. Drum and hammer printing mechanism.

Models LP10F and LP10H offer the following features:

a. 132 print columns
b. PDP-10 ASCII character set
c. 8-channel optical vertical format unit
d. 50- and 60-Hz versions
e. Wide range of forms accommodated
f. Static eliminators
g. Asynchronous operation
h. Full line MOS memory buffer
i. 2-speed drum
j. Quick-change drum
k. Print time meter
l. Ribbon counter
m. Penetration control
n. Phasing control
o. 50-foot device cable with Quicklatch connector

The seven line printer models offer a variety of printing speeds and character sets (refer to Table 1-1).

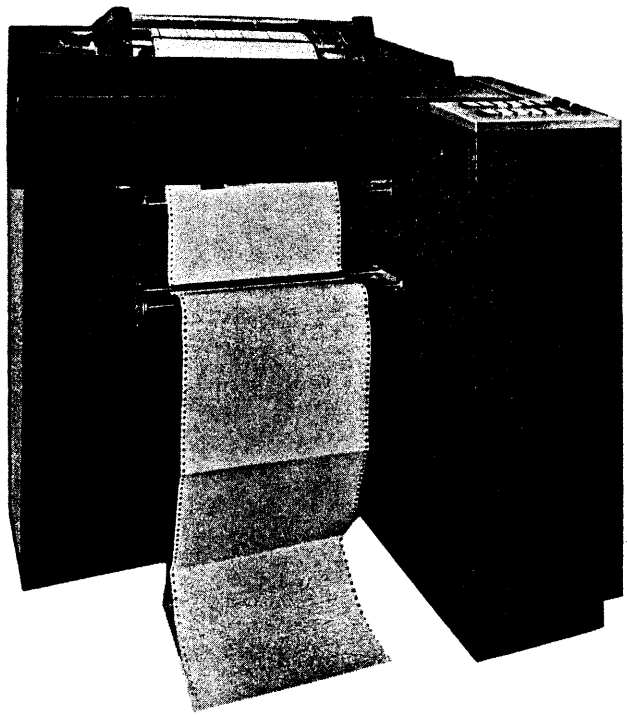


Figure 1-7 LP10A Line Printer

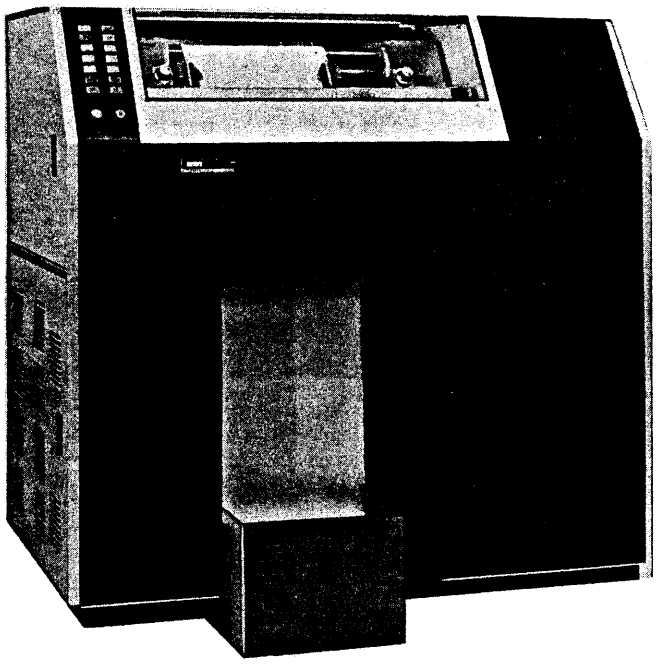


Figure 1-8 LP10B, C, D, E Line Printer

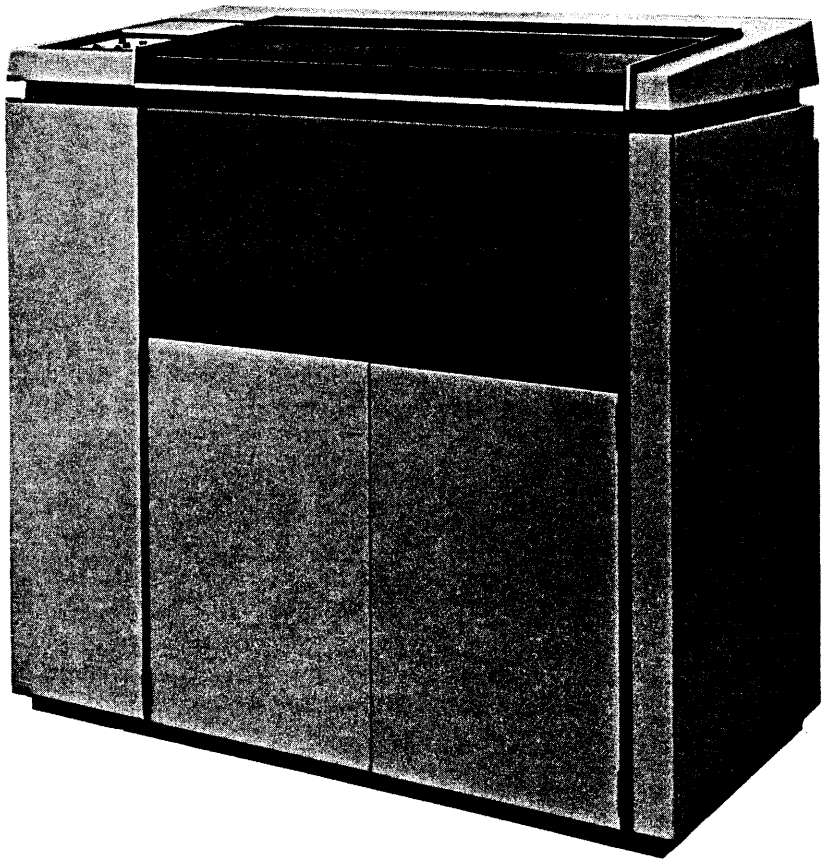


Figure 1-9 LP10F and LP10H Line Printer

Table 1-1
LP10 Line Printer Models

Type Number	Number of Characters	Printing Speed
LP10A (Series 4000)	64	300 lines/minute
LP10B (Series 5300)*	64	600 lines/minute
LP10C (Series 5300)	64	1000 lines/minute
LP10D (Series 5300)	96	600 lines/minute
LP10E (Series 5300)	128	500 lines/minute
LP10F (Series 2400)	64	1250/925 lines/minute
LP10H (Series 2400)	96	925/675 lines/minute

*Manufacture discontinued.

1.2.4 XY10 Plotter Control

The XY10 Plotter Control interfaces the XY10A or XY10B Plotters or equivalent with the PDP-10 I/O Bus. The XY10A and XY10B Plotters are manufactured by California Computer Products, Inc. (See Figures 1-10 and 1-11.)

The XY10A and XY10B Plotters offer the following features:

a. Drum-type plotters (bed-type plotters also available)
b. Wide variety of inch and step sizes
c. 50- and 60-Hz versions
d. 200-steps-per-second operating speed (Series 600 CalComp Plotter offers 900-steps-per-second operating speed)
e. Initial position set up manually
f. Eight directions of motion.

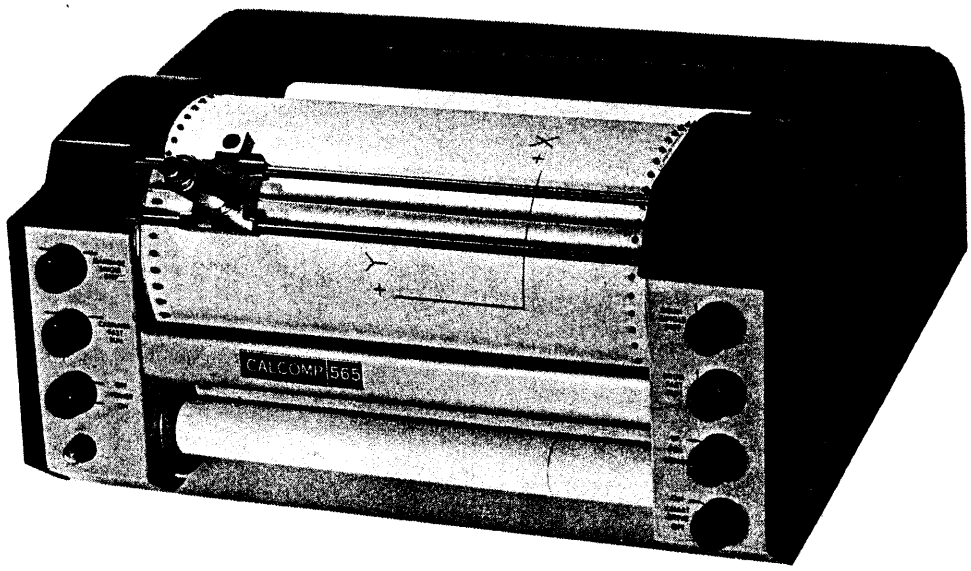


Figure 1-10 XY10A Plotter

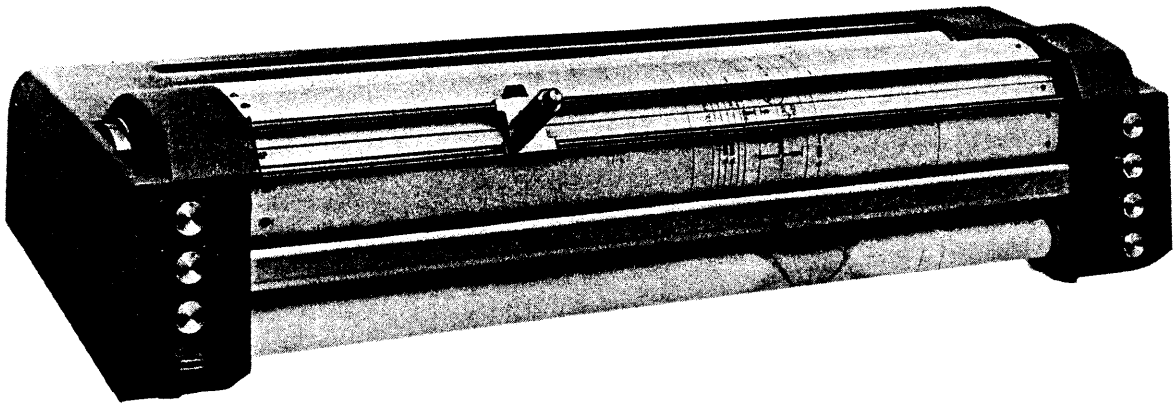


Figure 1-11 XY10B Plotter

1.3 BA10 MECHANICAL ASSEMBLY

Physically, the BA10 Hard Copy Control (see Figure 1-12) consists of DEC Type 1943 Mounting Panels, an indicator panel, and accessory hardware (power supply and control, fan assembly, etc.), housed in a standard DEC CAB-9B Cabinet.

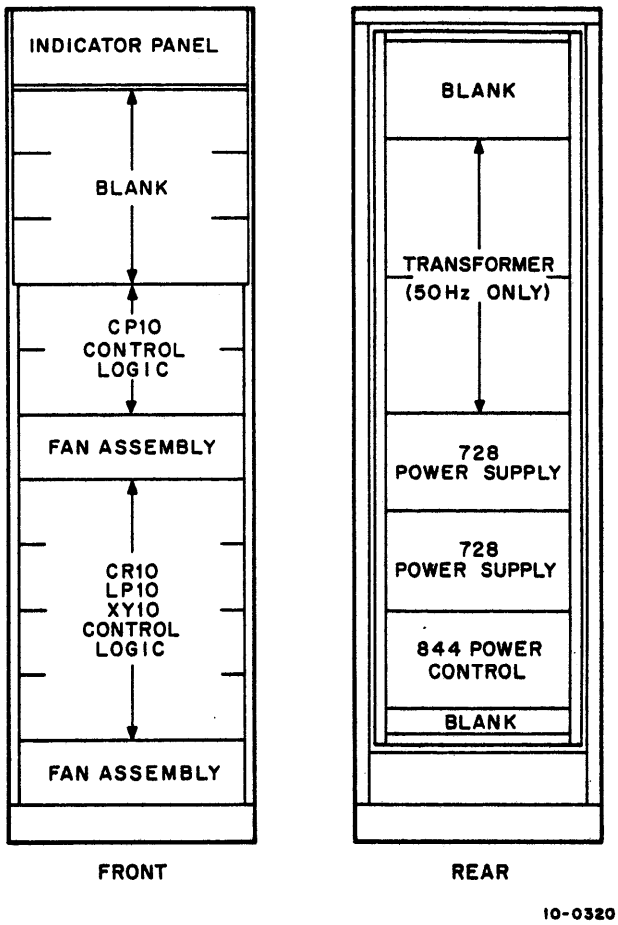


Figure 1-12 BA10 Unit Assembly Locations

The DEC mounting racks form two wire-wrap fields. One field contains four adjoining interconnected racks; when the appropriate modules are installed, this field contains control logic for the card reader, line printer, and plotter. The other field contains two adjoining interconnected racks; when the appropriate modules are installed, this field contains control logic for the card punch.

The DEC 844 Power Control provides ac power to the DEC 728 (or 728A) Power Supplies. The 844 Power Control and 728 (or 728A) Power Supplies are mounted inside the rear plenum door. Module mounting panels are mounted behind the front door with the wiring side facing the front of the cabinet. A fan at the bottom of the cabinet draws cooling air into the cabinet through a dust filter. The air is passed over the modules by a blower assembly mounted below the module mounting panels, and is exhausted through an opening at the top of the cabinet.

1.4 EQUIPMENT SPECIFICATIONS

Table 1-2 contains electrical, physical, and environmental specifications for the BA10 System.

Table 1-2
Electrical, Physical, and Environmental Specifications

	Voltage (Note 5)	Current @115V	Power/Heat Dissipation	Dimensions			Weight	Operating Temperature	Storage Temperature	Relative Humidity
				Height	Width	Depth				
BA10	115V, 60 Hz 230V, 50 Hz Single-phase	7A Surge: 24A	800 W 2700 Btu/hr.	69 in. 1.75m	22 in. 0.56m	29 in. 0.72m	350 lb 150 kg	60° to 95°F 15° to 35°C	40° to 110°F 5° to 45°C	20% to 80%
CP10A	115V, 60 Hz 230V, 50 Hz Single-phase	20A Surge: 50A	2500 W 8500 Btu/hr.	60 in. 1.52m	36 in. 0.91m	36 in. 0.91m	500 lb 230 kg	60° to 95°F 15° to 35°C (See Note 1)	40° to 110°F 5° to 45°C	20% to 80% (See Note 1)
CR10A	115V, 60 Hz 115V, 50 Hz Single-phase	16A Surge: 40A	1700 W 5800 Btu/hr.	37 in. 0.94m	36 in. 0.91m (See Note 2)	36 in. 0.91m	500 lb 230 kg	60° to 95°F 15° to 35°C (See Note 1)	40° to 110°F 5° to 45°C	30% to 90% (See Note 1)
CR10D	115V, 60 Hz 230V, 50 Hz Single-phase	4A Surge: 13A	470 W 1600 Btu/hr.	17 in. 43m	24 in. 61m	19 in. 48.3m	100 lb 45.4 kg	50° to 104°F 10° to 40°C	40° to 110°F 5° to 45°C	30% to 90% (See Note 1)
CR10E	115V, 60 Hz 230V, 50 Hz Single-phase	4.5A Surge: 26A	550 W 1900 Btu/hr	42 in. 1.07m	25 in. 63.5m	40 in. 101.6m	300 lb 136 kg	50° to 104°F 10° to 40°C	40° to 110°F 5° to 45°C	30% to 90% (See Note 1)
CR10F	115V, 60 Hz 230V, 50 Hz Single-phase	4A Surge: 13A	470 W 1600 Btu/hr.	13 in. 33m	20 in. 50.8m	15 in. 38m	70 lb 31.8 kg	50° to 104°F 10° to 40°C	40° to 110°F 5° to 45°C	30% to 90% (See Note 1)
LP10A	115V, 60 Hz 230V, 50 Hz Single-phase	11A Surge: 15A	1300 W 4300 Btu/hr.	51 in. 1.30m	43 in. 1.09m	30 in. 0.76m	1100 lb 500 kg	60° to 95°F 15° to 35°C	0° to 125°F -18° to 52°C	40% to 80%
LP10B	115V, 60 Hz 230V, 50 Hz Single-phase	20A Surge: 30A	2300 W 7800 Btu/hr.	56 in. 1.42m	56 in. 1.42m	30 in. 0.76m	1600 lb 725 kg	60° to 95°F 15° to 35°C	0°to 125°F -18° to 52°C	40% to 80%
LP10C LP10D LP10E	115V, 60 Hz 230V, 50 Hz Single-phase	20A Surge: 35A	2300 W 7800 Btu/hr.	56 in. 1.42m	56 in. 1.42m	30 in. 0.76m	1900 lb 850 kg	60° to 95°F 15° to 35°C	0° to 125°F -18° to 52°C	40% to 80%
LP10F LP10H	115V, 60 Hz 230V, 50 Hz Single-phase	See Note 3	6600 Btu/hr. Printing 3000 Btu/hr. Idle	48 in. 1.32m	48.5 in. 1.4m	36 in. 0.91m	800 lb 370 kg	50° to 110°F 10° to 43°C	0° to 150°F -18° to 66°C	30% to 90%
XY10A	115V, 60 Hz 115V, 50 Hz Single-phase	1.5A Surge: 1.5A	170 W 600 Btu/hr.	10 in. 0.25m	18 in. 0.46m	15 in. 0.38m	33 lb 15 kg	60° to 95°F 15° to 35°C	40° to 110°F 5° to 45°C	20% to 80%
XY10B	115V, 60 Hz 115V, 50 Hz Single-phase	1.5A Surge: 1.5A	170 W 600 Btu/hr.	10 in. 0.25m	40 in. 1.02m (See Note 4)	15 in. 0.38m	53 lb 24 kg	60° to 95°F 15° to 35°C	40° to 110°F 5° to 45°C	20% to 80%

NOTES

1. Refer to ANSI standard X3.11-1969 for further information on temperature and humidity specifications.
2. The CR10A is supplied with a table. The overall dimensions (card reader and table) are as follows:
   - Height: 56 in. (1.37m)
   - Width: 36 in. (0.91m)
   - Depth: 64 in. (1.67m)
3. Current:
   - 115V ≤ 18A/rms
   - 230V ≤ 9A/rms
   - Inrush ≤ 90A peak decaying to steady state ≤ 3 seconds.
4. The XY10B is supplied with a table. The overall dimensions and weight (plotter and table) are as follows:
   - Height: 40 in. (1.02m)
   - Width: 54 in. (1.37m)
   - Depth: 22 in. (0.56m)
   - Weight: 130 lb (60 kg)
5. The BA10 provides 50 Hz ac power to the CR10A Card Reader. The BA10 or TD10 provides 50 Hz ac power to the XY10A or XY10B Plotters.

1.5 REFERENCE MATERIAL

The following documents contain supplementary material. These documents may be obtained from the nearest DEC office or from:

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts

Title	Contents
Digital Logic Handbook	Specifications and descriptions of logic modules, simplified explanations of the selection, and use of these modules in numerous applications
KA10 Maintenance Manuals Volume I DEC-10-HMAB-D Volume II DEC-10-HMBB-D	Complete information on the internal operation of the KA10 logic, memory, basic input/output, and processor options
DECsystem-10 Interface Manual DEC-10-HIFC-D	PDP-10 interface requirements
DECsystem-10 Site Preparation Guide DEC-10-SITE-D	Site planning, equipment specifications, and floor plans
DECsystem-10 System Reference Manual DEC-10-HGAC-D	Programming and operating information for the PDP-10 System
MDS 4000 Series Printer Instruction Manual	Complete operating instructions, principles of operation, and maintenance information for the LP10A Line Printer
MDS 5300 Series Printer Service Manual	Complete operating instructions, principles of operation, and maintenance information for the LP10B, LP10C, LP10D, and LP10E Line Printers
Technical Manual for the Data Products Model 2470 Line Printer (2 vols)	Complete operating instructions and maintenance information for the LP10F and LP10H Line Printers.
Instruction Manual for the CalComp Digital Incremental Plotter, Models 563, 565, 502, and 518	Complete operating instructions, principles of operation, and maintenance instructions for the XY10 Digital Incremental Plotters
Technical Manuals for the Documation M-Series and Soroban (MDS) Card Readers	Complete operating instructions, principles of operation, and maintenance instructions for the CR10 Card Readers
Technical Manual for the Mohawk Data Sciences Card Punch	Complete operating instructions, principles of operation, and maintenance instructions for the CP10 Card Punch

CHAPTER 2
INSTALLATION

2.1 INSPECTION

On receipt of the equipment, inspect for any visible signs of damage in transit, such as dents and abrasions. Inspect the logic modules for foreign material that may have lodged in them during shipment. Immediately report any damage to the carrier and Digital Equipment Corporation. Check the contents of the cartons with the shipping documents and immediately report any omissions to Digital Equipment Corporation.

2.2 INSTALLATION

The BA10 System comprises a BA10 Hard Copy Control and hard copy devices such as the card punch, card reader, line printer, and plotter. The BA10 System can accommodate one of each of these devices. The installation procedure for the BA10 System is keyed specifically to the individual device.

2.2.1 Installation of the CR10, LP10, and XY10 Control Logic

Install the control logic in the following manner:

Step	Procedure
1	Remove the skid and discard.
2	Turn off system power.
3	Position the BA10 Cabinet as shown in the site plan.
4	Install the grounding cable as shown in the site plan.
5	Connect I/O Bus Cable No. 1 (IN) to locations HJ13, 14.
6	Connect I/O Bus Cable No. 2 (IN) to locations HJ15, 16.
7	Connect I/O Bus Cable No. 1 (OUT) between BA10 locations HJ17, 18 and the next device on the PDP-10 I/O Bus, unless this is the last device on the PDP-10 I/O Bus.
8	Connect I/O Bus Cable No. 2 (OUT) between BA10 locations HJ19, 20 and the next device on the PDP-10 I/O Bus, unless this is the last device on the PDP-10 I/O Bus.
9	Install the margin check cable from I/O Bus Cable No. 2 to J2 of the power bracket in the lower portion of the BA10 Cabinet.

Step	Procedure
10	If this is the last device on the PDP-10 Margin Check Bus, install the return plug into J1 of the power bracket. If this is not the last device, connect a margin check cable between J1 of the BA10 Margin Check Bus and J2 of the margin check bus of the next device on the PDP-10 Margin Check Bus.
11	Install a remote turn-on cable from the previous device to the 844 Power Control mounted on the rear plenum door of the BA10.
12	Connect a remote turn-on cable from the BA10 844 Power Control to the next device on the bus.
13	Install the hard copy devices included in the system (refer to Paragraphs 2.2.3 through 2.2.6).
14	Plug in the ac power cord.
15	Turn on system power and run the maintenance diagnostics to ensure satisfactory equipment operation.

2.2.2 Installation of the CP10 Control Logic

Install the CP10 Control Logic in the following manner:

Step	Procedure
1	If this is an add-on to an existing BA10, physically mount the CP10 logic racks as shown in Figure 1-12.
2	Connect I/O Bus Cable No. 1 (IN) to locations CD13, 14.
3	Connect I/O Bus Cable No. 2 (IN) to locations CD15, 16.
4	Connect I/O Bus Cable No. 1 (OUT) from locations CD17, 18 to the next device on the PDP-10 I/O Bus.
5	Connect I/O Bus Cable No. 2 (OUT) from locations CD19, 20 to the next device on the PDP-10 I/O Bus.
6	If this is an add-on to an existing BA10, connect the dc power wiring from the BA10 Logic Racks.

2.2.3 Card Punch Installation

Install the card punch in the following manner:

Step	Procedure
1	Remove the skid and discard.
2	Position the card punch as shown in the site plan.
3	Connect a ground cable between the card punch and the BA10 Cabinet.
4	Connect the device cable (W852 end) to locations CD29, 30 of the CP10 Control in the BA10 Cabinet and the other end to W2J1 inside the rear of the card punch logic rack.
5	Plug in the ac power cord.

2.2.4 Card Reader Installation

Install the card reader in the following manner:

Step	Procedure
1	Remove the skid and discard.
2	Position the card reader as shown in the site plan. Remove shipping screws on all models except CR10A or B.
3	Connect the device cable (W852 end) to BA10 locations CD19, 20; connect the other end of the device cable to the rear of the card reader.

Step	Procedure
4	Connect a ground cable between the card reader and the BA10 Cabinet.
5	For the CR10B model only, plug the ac power cord, one end of which is hard-wired to the BA10, into the power receptacle on the rear of the card reader.
6	In all card reader models except the CR10B, plug the ac power cord into the power source receptacle.

2.2.5 Line Printer Installation

Install the line printer in the following manner:

Step	Procedure
1	Remove the skid and discard.
2	Position the line printer as shown in the site plan.
3	For models LP10A, B, C, D, and E, connect the device cable (W851 end) to BA10 locations CD17, 18 and the Amphenol connector end to J901 located in the bottom right portion of the line printer. For models LP10F and H, connect the BC10M device cable (W858 end) to BA10 locations CO17, 18 and the Amphenol Quicklatch end to the mating Quicklatch receptacle on the bottom right of the line printer as viewed from the rear.
4	Connect a ground cable between the line printer and the BA10 Cabinet.
5	Plug in the ac power cord.

2.2.6 Plotter Installation

Install the plotter in the following manner:

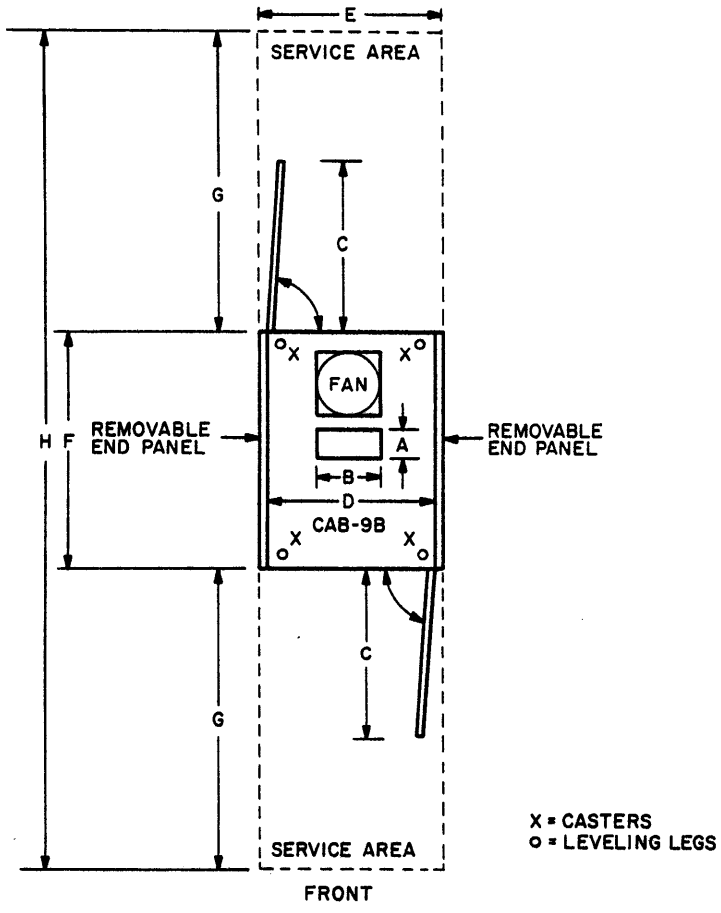
Step	Procedure
1	Position the plotter as shown in the site plan.
2	Connect the device cable (W012 end) to BA10 location F32 (TD10 location J32); connect the Cannon connector end to P5 of the plotter.
3	Connect a ground cable between the plotter and the BA10 (or TD10) Cabinet.
4	In 60-Hz systems, connect an ac power cord from J7 of the plotter to a convenient outlet; in 50-Hz systems, ac power is obtained from the BA10 (or TD10) Cabinet.

2.3 EQUIPMENT FLOOR PLANS

Floor plans for the BA10 and associated hard copy devices are presented in Figures 2-1 through 2-11.

NOTE

Figures 2-1 through 2-11 are all drawn to the same scale (0.5-inch = 12 inches).



DIMENSIONS	A	B	C	D	E	F	G	H
INCHES	3.5	7.0	19.3	20.3	22.0	29.0	36.0	100
METERS	0.09	0.18	0.49	0.52	0.54	0.72	0.90	2.50

10-0462

Figure 2-1 BA10 Hard Copy Control – Floor Plan

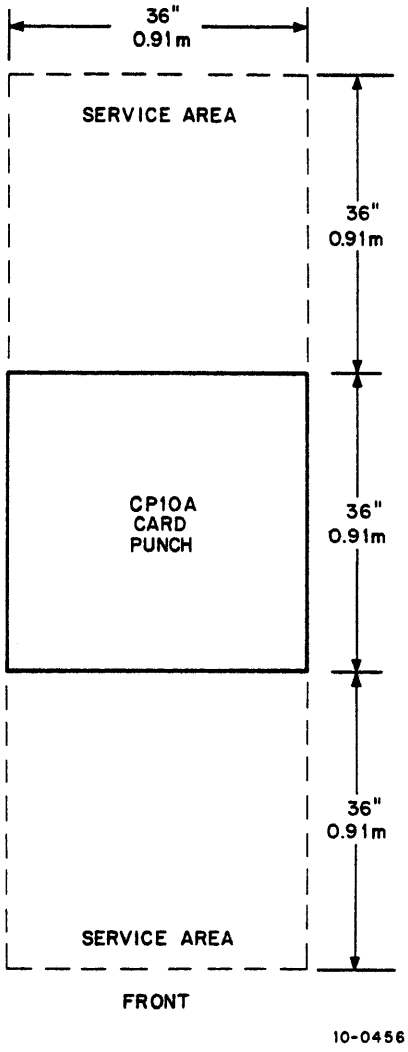
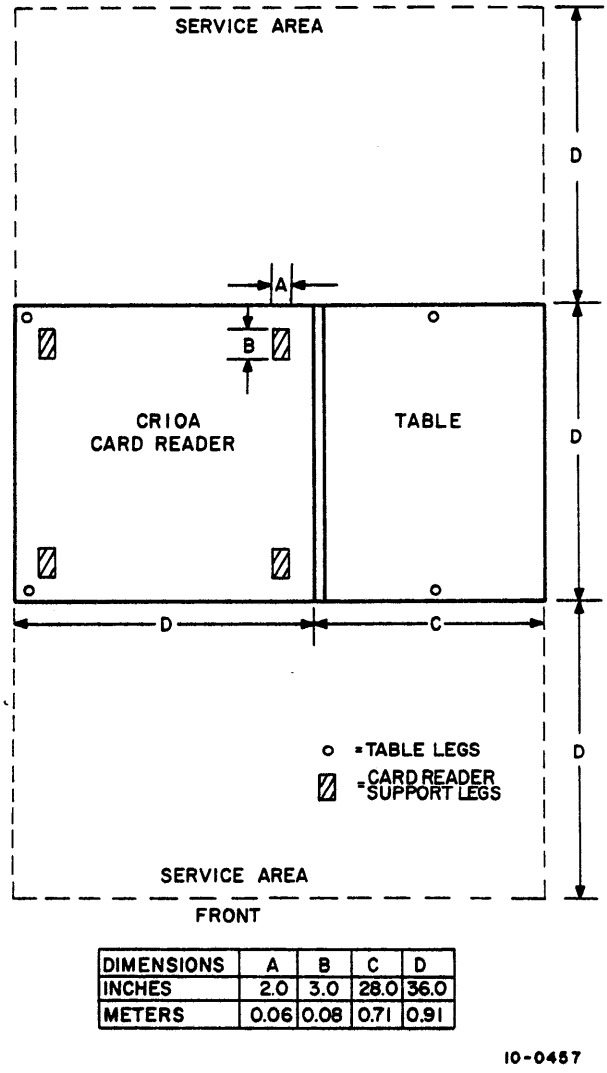


Figure 2-2 CP10A Card Punch – Floor Plan



DIMENSIONS	A	B	C	D
INCHES	2.0	3.0	28.0	36.0
METERS	0.06	0.08	0.71	0.91

Figure 2-3 CR10A Card Reader – Floor Plan

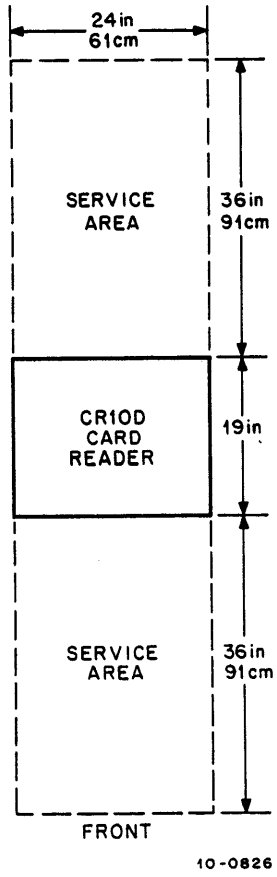


Figure 2-4 CR10D Card Reader – Floor Plan

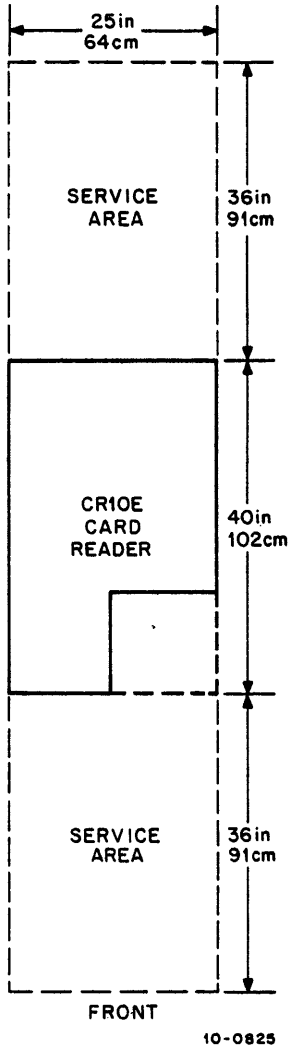


Figure 2-5 CR10E Card Reader – Floor Plan

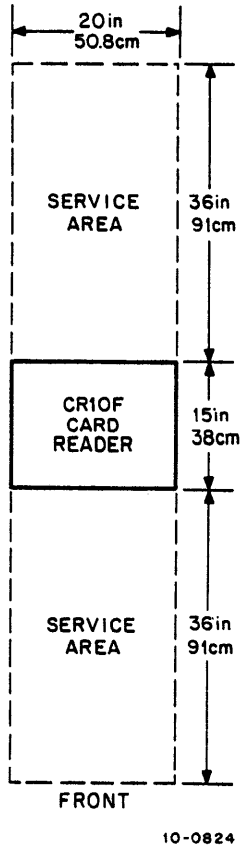
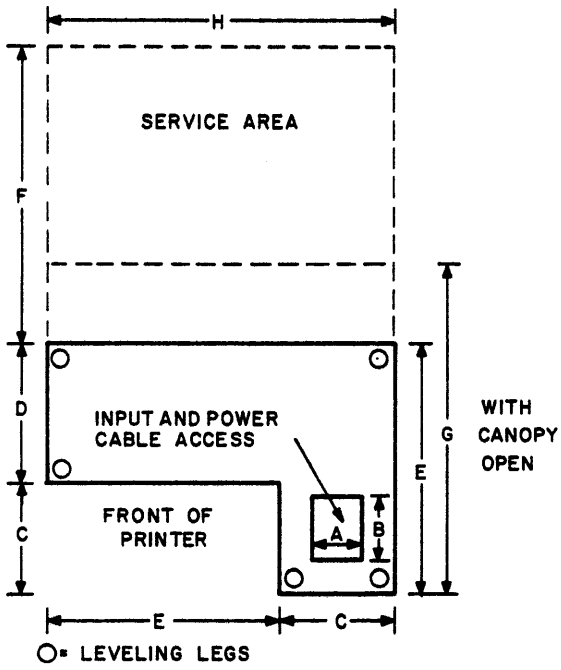


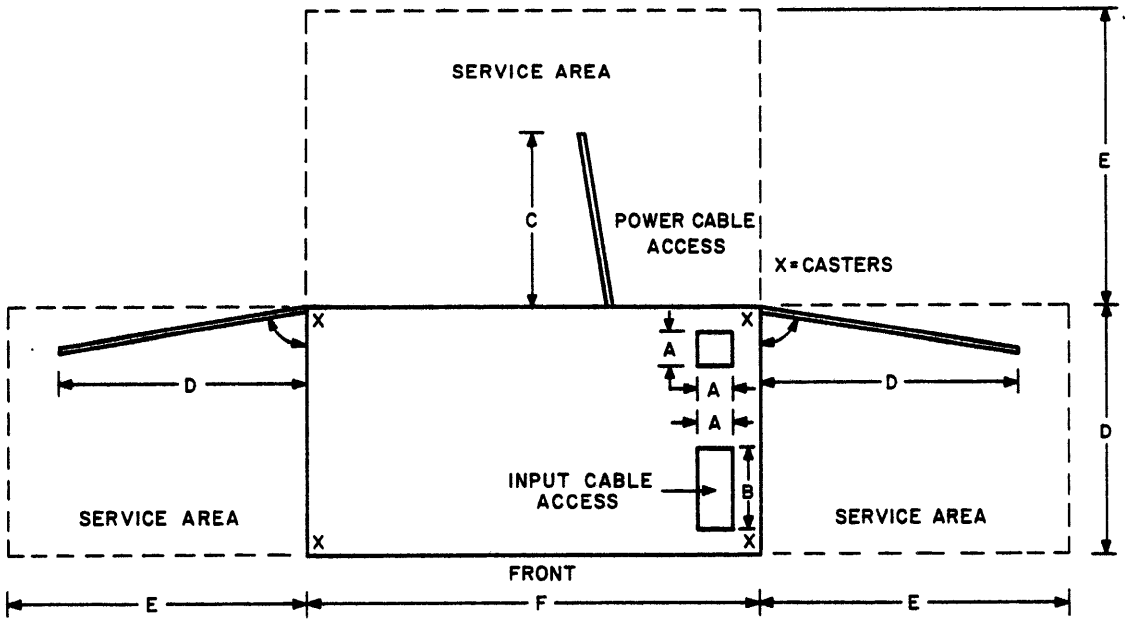
Figure 2-6 CR10F Card Reader – Floor Plan



DIMENSIONS	A	B	C	D	E	F	G	H
INCHES	6.0	8.0	13.5	16.5	30.0	36.0	40.0	43.0
METERS	0.15	0.22	0.34	0.42	0.76	0.91	1.02	1.09

10-0458

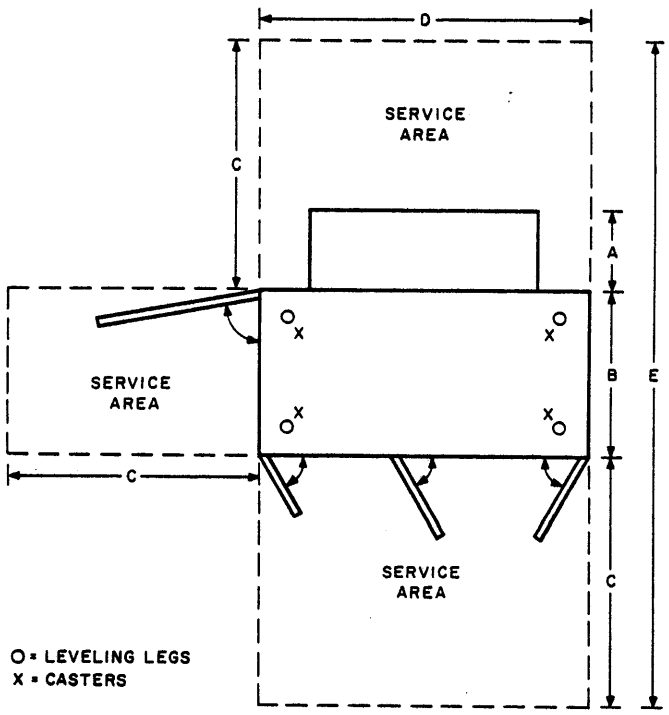
Figure 2-7 LP10A Line Printer – Floor Plan



DIMENSIONS	A	B	C	D	E	F
INCHES	4.0	10.0	21.0	30.0	36.0	56.0
METERS	0.10	0.25	0.53	0.76	0.91	1.42

10-0459

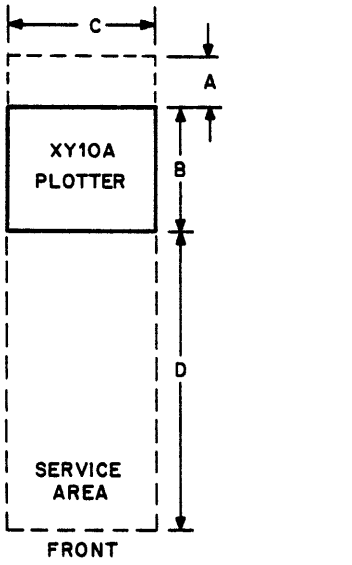
Figure 2-8 LP10B, C, D, E Line Printers – Floor Plan



DIMENSIONS	A	B	C	D	E
INCHES	11.5	24.5	36	48.5	96.5
METERS	0.29	0.62	0.91	1.23	2.44

10-0935

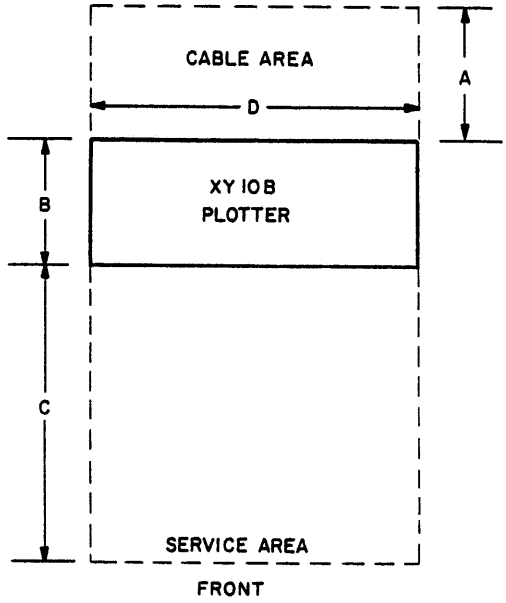
Figure 2-9 LP10F and LP10H Line Printer – Floor Plan



DIMENSIONS	A	B	C	D
INCHES	6.0	15.0	18.0	36.0
METERS	0.15	0.38	0.46	0.90

10-0460

Figure 2-10 XY10A Plotter – Floor Plan



DIMENSIONS	A	B	C	D
INCHES	6.0	15.0	36.0	40.0
METERS	0.15	0.38	0.91	1.02

10-0461

Figure 2-11 XY10B Plotter – Floor Plan

CHAPTER 3
BA10 COMMON LOGIC AND CABLING

3.1 INTRODUCTION

This section describes the logic and cabling common to all the devices that constitute the BA10 Hard Copy System.

The processor communicates with the BA10 Hard Copy System via the I/O bus. Table 3-1 provides a glossary of the signals on the I/O bus.

The I/O bus lines used by the devices are fed into a set of I/O bus receivers, the outputs of which are common to the CR10, LP10, and XY10 Control Logic (see Figure 3-1). The I/O bus lines are also fed into another set of I/O bus receivers in the CP10 Control Logic. Each device contains its own logic for transmitting information over the common I/O bus to the processor.

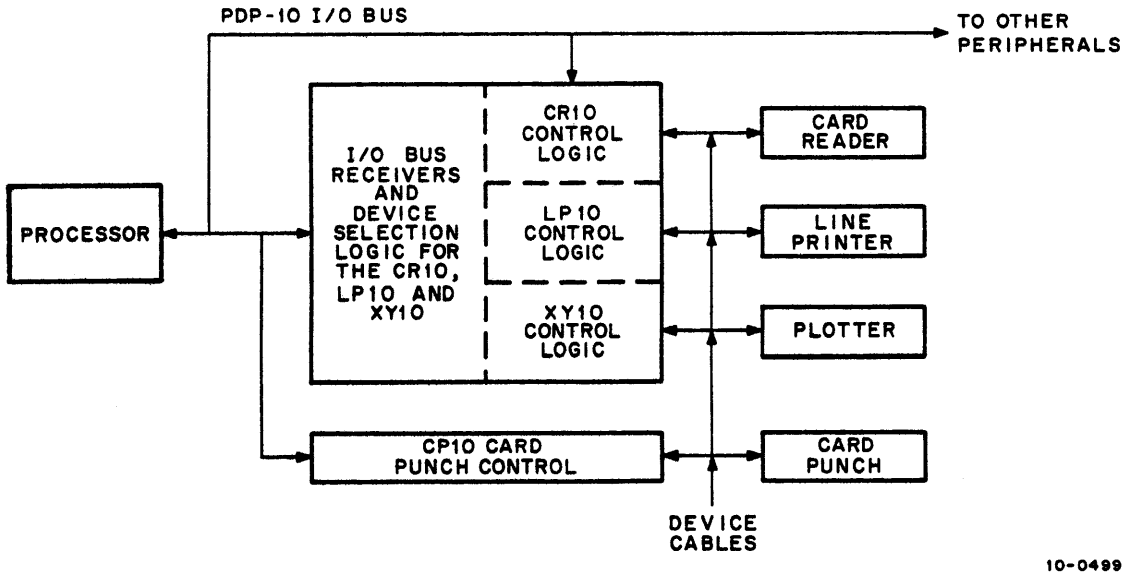


Figure 3-1 BA10 Hard Copy System

Table 3-1
I/O Bus Glossary

Signal	Function
IOB00-35	Used for: *a.* Bidirectional data transfer *b.* Transfer device control information to the device control logic *c.* Transfer device status information to the processor.
IOB RESET	Initializes all I/O devices.
IOS03-09	Used for I/O device selection.
IOB PI01-07	Seven levels at which I/O devices may interrupt the processor due to an error or completion of an I/O operation.
IOB RDI PULSE	Used for hardware read-in operation. When the read-in button is depressed, this signal causes the I/O device specified by the read-in switches to start reading data. Not used in the BA10 System.
IOB RDI DATA	Informs the processor that the I/O device is ready with data during a hardware read-in operation. Not used in the BA10 System.
IOB CONO CLR	During a PDP-10 CONO instruction, this pulse clears the control registers within the specified I/O device.
IOB CONO SET	During a PDP-10 CONO instruction, this pulse gates the control information, which is on the I/O bus, into the I/O device control registers.
IOB CONI	During a PDP-10 CONI instruction, this level gates the contents of the status registers, within the specified I/O device, onto the data lines (IOB00-35) to be read by the processor.
IOB DATAO CLR	During a PDP-10 DATAO instruction, this pulse clears the data buffer, of the specified I/O device, prior to loading the data buffer with new data.
IOB DATAO SET	During a PDP-10 DATAO instruction, this pulse gates the data, on I/O bus lines IOB00-35, into the data buffer of the specified I/O device.
IOB DATAI	During a PDP-10 DATAI instruction, this level gates the contents of the data register, within the specified I/O device, onto the data lines (IOB00-35) to be read by the processor.
IOB DR SPLIT	Not used in BA10 System.

3.2 DEVICE SELECTION

All PDP-10 I/O devices share the I/O bus; therefore, the program must specify the device when issuing an I/O instruction via bits 03 through 09 of the PDP-10 I/O instruction. Bits 03 through 09 comprise a 7-bit field, but for decoding convenience, a pair of complementary signals for each bit is transmitted over I/O bus lines IOS03(1), IOS03(0), through IOS09(1), IOS09(0). Each device has a unique device code and responds to the I/O instruction on detecting its code. This is accomplished by installing jumpers on W990 Modules to connect the proper IOS lines to the input of each of the device decoder modules. For example, in Figure 3-2 the XY10 Plotter is wired for standard device code 140_8. Therefore, IOC PL SELECT is true only when this code is present on the PDP-10 I/O bus. The selection of the LP10, CR10, and CP10 Control Logics is the same except for the wiring of their respective W990 Modules. Refer to Table 3-2 for the W990 locations, standard device codes, and jumpers.

If any of the BA10 devices are not connected to the BA10, the select logic for that device must be inhibited in the following manner:

Step	Procedure
1	Remove one of the W990 Modules associated with the BA10 device.
2	Remove any jumpers connected to pin E of the W990 Module.

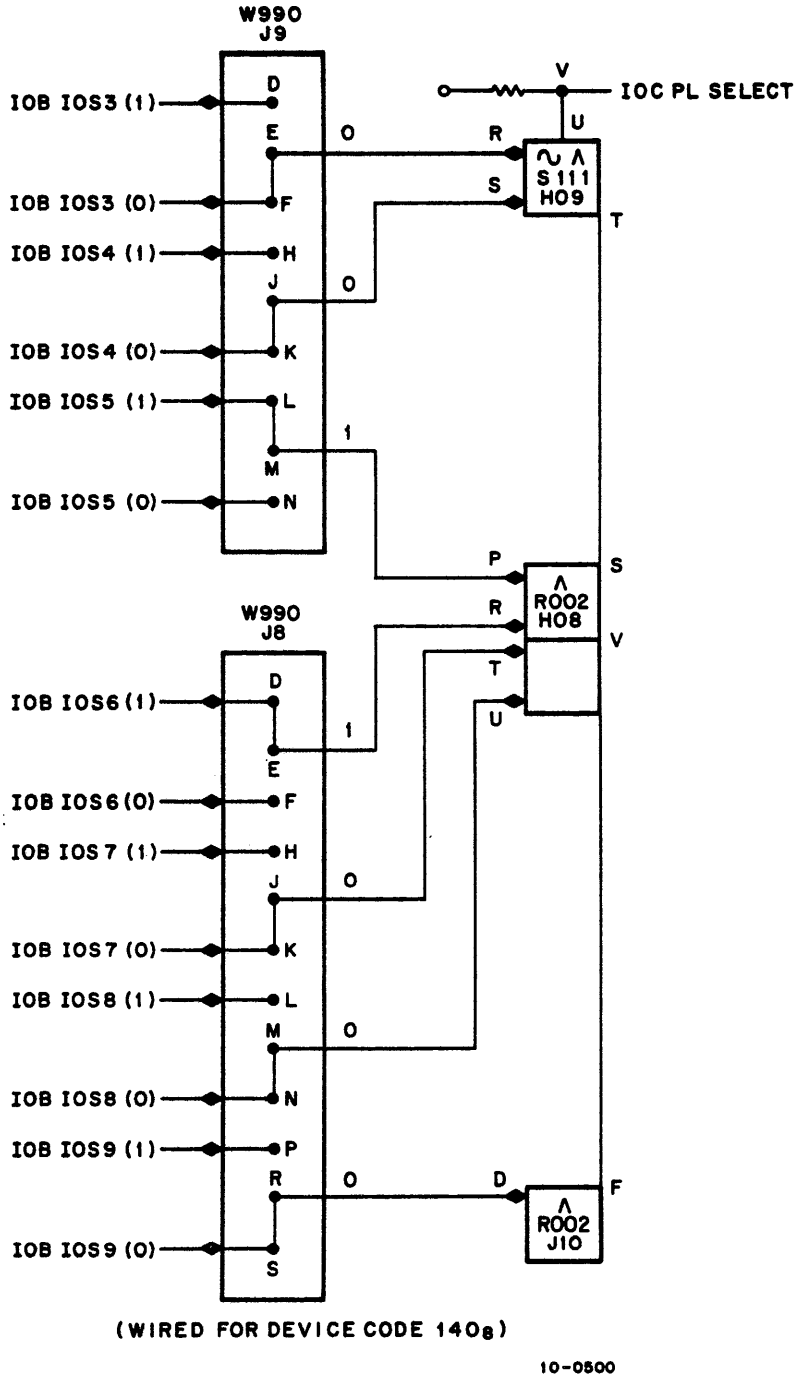


Figure 3-2 Device Selection

Step	Procedure
3	Install a jumper from pin C to pin E of the W990 Module.
4	Reinsert the W990 Module into its original location.

Table 3-2
Standard Device Code Jumpers

Device	Standard Code	W990 Location	Jumper Pins
CP10	110_8	CP10-A14	E to F J to K L to M R to S
		CP10-B14	E to F H to J M to N
CR10	150_8	BA10-H11	E to F J to K L to M
		BA10-H10	D to E J to K L to M R to S
LP10	124_8	BA10-J12	E to F J to K L to M
		BA10-J11	E to F H to J M to N P to R
XY10	140_8	BA10-J9	E to F J to K L to M
		BA10-J8	D to E J to K M to N R to S

3.3 TYPE 844 POWER CONTROL

The Type 844 Power Control (see Figure 3-3) determines the manner in which power is applied to the BA10 Power Supplies (also the card reader and plotters on 50-Hz systems). Table 3-3 provides a description and operation of the Type 844 Power Control.

3.4 BA10 INDICATOR PANEL

The BA10 Indicator Panel (see Figure 3-4) provides a visual display of the control registers, buffers, and status registers associated with the CP10 Card Punch, CR10 Card Reader, LP10 Line Printer, and XY10 Plotter. Refer to Chapters 4 through 7 for a detailed description of the indicators.

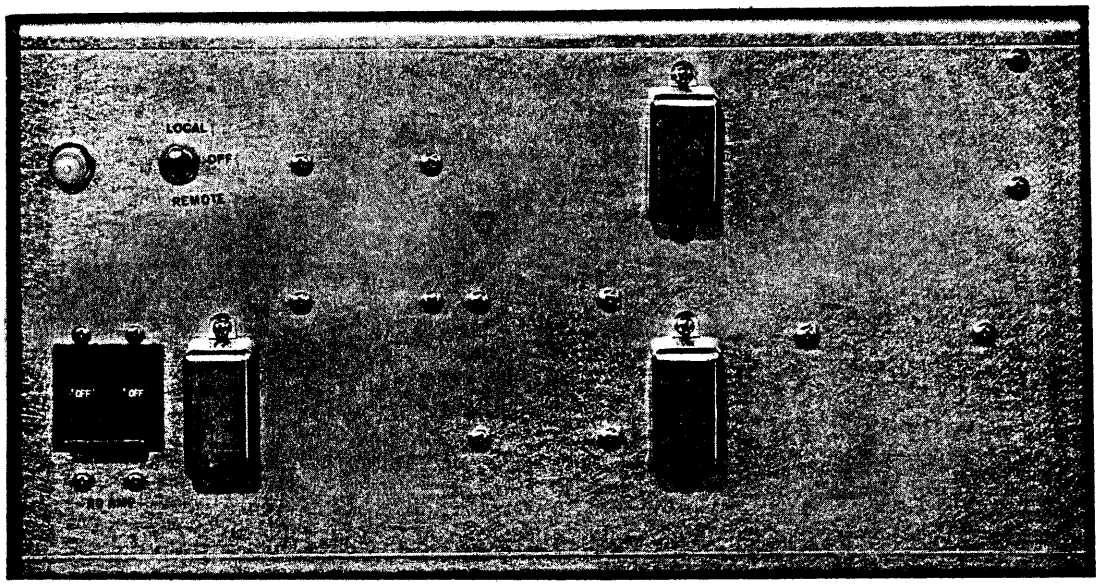


Figure 3-3 Type 844 Power Control

Table 3-3
Type 844 Power Control Panel

Nomenclature	Function
Indicator	When lit: ac power is applied to the Type 844 Power Control.
Circuit Breaker 30A	Protects the ac power source; this circuit breaker should be placed in the OFF position before servicing the BA10.
Toggle Switch REMOTE/OFF/LOCAL	REMOTE – Power is applied to the BA10 upon application of power to the processor. OFF – Power is removed from the BA10 Fans and Power Supplies. LOCAL – Power is applied to the BA10, independent of the processor.

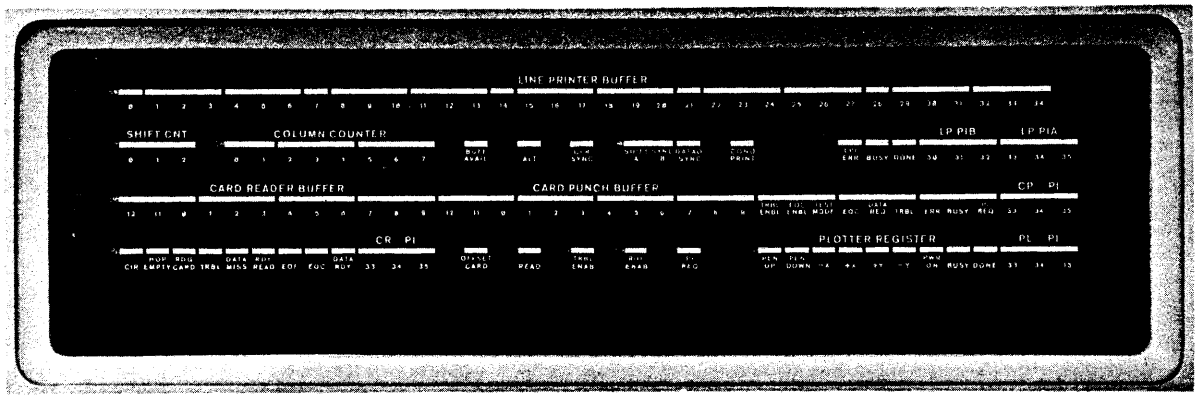


Figure 3-4 BA10 Indicator Control Panel

CHAPTER 4
CP10 CARD PUNCH SYSTEM

This chapter contains programming, theory of operation, and operating information pertinent to the CP10 Card Punch System.

4.1 FUNCTIONAL DESCRIPTION

The CP10 Card Punch System (see Figure 4-1) provides data storage on standard 12-row, 80-column cards. Data are transferred from the processor to the CP10 Card Punch Control one column at a time. After each column of data is transferred to the card punch, the CP10 Card Punch Control requests another column of data from the processor. When the card punch has received four columns of data, it punches them onto the card and then advances the four card columns. This sequence continues until an eject command is issued by the processor.

Figure 4-1 CP10 Card Punch System – Functional Block Diagram

4.2 INDICATORS AND CONTROLS

Table 4-1 describes the functions of the BA10 indicators associated with the CP10 Card Punch System.

The indicator/control panel, located on the CP10A Card Punch, is shown in Figure 4-2. Table 4-2 describes the use and function of these indicators and controls.

Table 4-1
BA10 Indicator Panel – Card Punch Section

Nomenclature	Function
CARD PUNCH BUFFERS 12-09	Display the contents of the 12-bit card punch buffer register.
TRBL ENBL	Indicates the CP10 Control Logic is enabled to interrupt the processor when a card punch trouble condition is detected (see TRBL).
EOC ENBL	Indicates the CP10 Control Logic is enabled to interrupt the processor when the card punch has punched 80 columns of data or an eject command was issued.
TEST MODE	Indicates the card punch is in the off-line test mode.
EOC	Indicates the card punch has punched 80 columns of data or an eject command was issued.
DATA REQ	Indicates the CP10 Card Punch Control is ready to receive new data.
TRBL	Indicates the card punch has detected a stacker full, hopper empty, pick fail, eject fail, stack fail, of full chip box condition.
ERR	Indicates a data punching error was detected by the card punch.
BUSY	Indicates the CP10 Card Punch Control is transferring data to the card punch.
PI REQ	Indicates the CP10 Card Punch Control is requesting a priority interrupt.
CP PI33-35	Indicate the priority interrupt level assignment of the CP10 Card Punch Control.

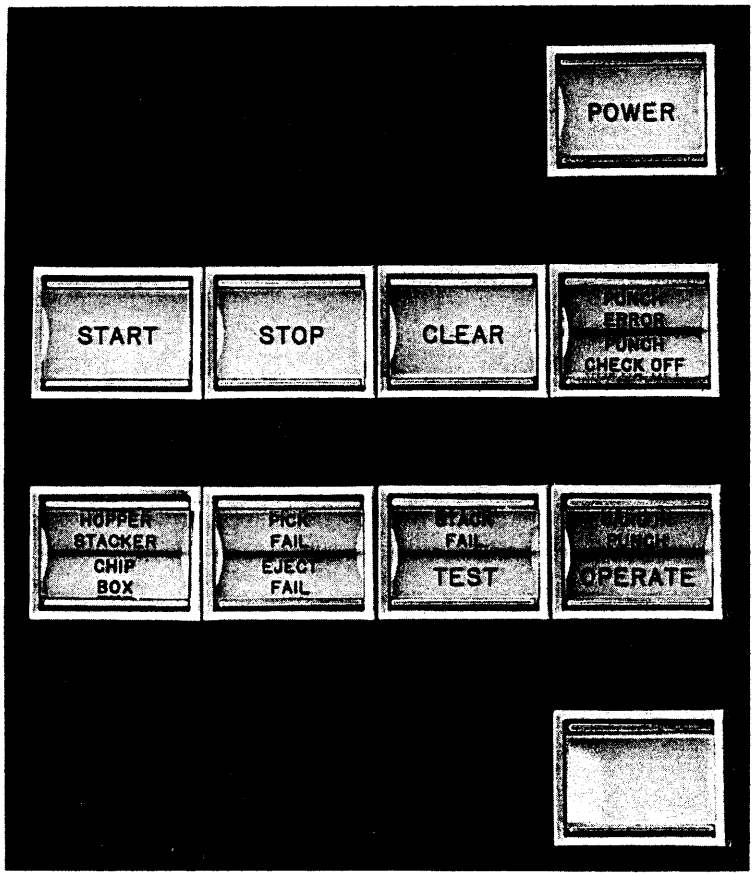


Figure 4-2 CP10A Card Punch Indicator/Control Panel

Table 4-2
CP10A Card Punch Indicator/Control Panel

Nomenclature	Item	Function
POWER	Push ON/Push OFF switch Indicator Status: On — Color: Green Status: Off — Color: Red	Applies ac power to the card punch.
START	Momentary push switch Indicator Status: Start — Color: Green Status: Stop — Color: White	Places the card punch in the START (on-line) condition. In the TEST mode it causes picking and punching of cards for off-line testing.
STOP	Momentary push switch Indicator Status: OFF LINE — Color: Amber Status: ON LINE — Color: White	Places the card punch in the STOP (off-line) condition. In the TEST mode, depressing this switch stops the picking and punching of cards off-line.
CLEAR	Momentary push switch Indicator Status: Trouble — Color: Red Status: No trouble — Color: White	Resets the card punch logic and starts the drive motor if the trouble condition that caused the stop condition has been rectified.
ERROR CHECK	Toggle switch ON/OFF	The switch is located in the lower compartment of the card punch. When in the ON position it allows the punched data to be compared to the contents of the data buffer.
PUNCH CHECK OFF	Indicator Status: Switch on — Color: Orange Status: Switch off — Color: Dark	Indicates the position of the ERROR CHECK switch.
PUNCH ERROR	Indicator Status: Error — Color: Red Status: No error — Color: Dark	Indicates the data punched did not compare to the data in the card punch buffer. ERROR CHECK switch must be ON.
HOPPER/STACKER	Indicator Status: On — Color: Red Status: Off — Color: Dark	Indicates the card punch hopper is empty or the card punch stacker is full.

Table 4-2 (cont)
CP10A Card Punch Indicator/Control Panel

Nomenclature	Item	Function
CHIP BOX	Indicator Status: On / Off Color: Red / Dark	Indicates the card punch chip box is almost full.
PICK FAIL	Indicator Status: On / Off Color: Red / Dark	Indicates a card pick was attempted; however, the card did not reach the punch station in the specified time.
EJECT FAIL	Indicator Status: On / Off Color: Red / Dark	Indicates a card eject was attempted; however, the card did not clear the punch station in the specified time.
STACK FAIL	Indicator Status: On / Off Color: Red / Dark	Indicates a card was not properly accepted by the output stacker.
TEST Switch (not shown in Figure 4-2)	Toggle switch FAST/OFF/NORMAL	Located inside the pedestal door. When in the FAST or NORMAL position it allows self-testing of the card punch in the OFF-line mode.
TEST	Indicator Status: On / Off Color: Red / Dark	Indicates the position of the TEST switch.
CARD IN PUNCH	Indicator Status: On / Off Color: Amber / Dark	Indicates a card is in the card punch station.
OPERATE	Indicator Status: On / Off Color: Green / Dark	When ON, it indicates the card punch is ready to operate on-line.

4.3 OPERATING NOTES

4.3.1 Card Punch Start-Up Procedure

Operational control of the card punch is exercised by the processor, under program control, after system power has been applied and the card punch start-up procedure has been performed as follows:

Step	Procedure
1	Place the TEST switch in the OFF position.
2	Depress the POWER switch.
3	Load the card punch supply hopper (refer to Paragraph 4.3.2).
4	Depress the CLEAR switch.
5	Depress the START switch.

The card punch is now on-line (provided no errors are indicated) and is ready to communicate with the BA10. The card punch is placed off-line by depressing the STOP or CLEAR button.

4.3.2 Card Punch Loading Procedure

To load the hopper, fan the cards and jog them on a flat surface. Hold the first 100 cards (about an inch of the deck) face down, with the 12 edge (top) at the back of the hopper (column 1 to the left). Raise the right end of the card stack and insert the cards into the hopper so that the leading edge of the bottom card rests against the picker throat, then drop the cards into place. Put the remaining cards on top of the first stack. Always stop the punch before removing cards from the stacker.

4.4 CP10 I/O INSTRUCTIONS

The card punch logic responds to three of the four basic I/O instructions, as shown in Table 4-3.

Table 4-3
I/O Instructions

Instruction	Function
CONO (Conditions Out)	Effects a transfer of conditions from the processor to the CP10 Control Logic to perform one or more of the functions shown in Figure 4-3.
CONI (Conditions In)	Transfers the CP10 Control Logic status information (shown in Figure 4-4) into the processor.
DATAO (Data Out)	Clears DATA REQUEST, sets BUSY (Buffer Full), and loads the data word supplied by the processor into the punch control buffer.
DATAI (Data In)	Not used by the card punch control.

4.4.1 CONO Instruction

The format of the conditions word transferred to the card punch logic during a CONO is shown in Figure 4-3.

The CONO bits have the following significance:

Bit 20(1) Initializes the CP10 Card Punch Control Logic.

Bit 21(1) Offsets the card contained in the punch station (compact model) when the card is ejected. Place the card contained in the punch station in the alternate stacker (console model) when the card is ejected.

Bit 23(1) Ejects the card in the punch station after the contents of the card punch buffer are punched. Ejection moves a card through the punch station four times as fast as the normal punch speed.

Bit 24(1) Disables priority interrupt requests from the CP10 Card Punch Control when a card punch trouble condition is detected.

Bit 25(1) Enables priority interrupt requests from the CP10 Card Punch Control when a card punch trouble condition is detected.

Bit 26(1) Clears the punch error flip-flop.

Bit 27(1) Disables priority interrupt requests when 80 columns of data are punched or an eject command is issued.

Bit 28(1) Enables priority interrupt requests when 80 columns of data are punched or an eject command is issued.

Bit 29(1) Clears the end of card flip-flop.

Bit 30(1) Turns on the punch motor.

Bit 31(1) Clears the data request flip-flop.

Bit 32(1) Sets the data request flip-flop.

Bits 33-35 Determine the priority interrupt request level assignment of the CP10.

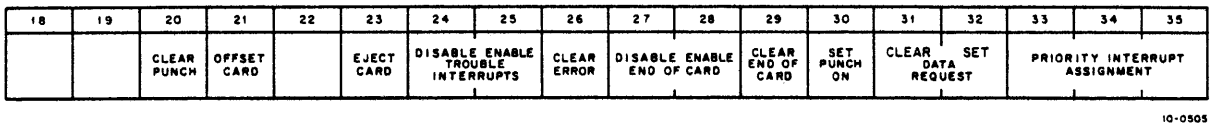


Figure 4-3 CONO Conditions Word

4.4.2 CONI Instruction

The format of the status word read into the processor during a CONI is shown in Figure 4-4.

The CONI bits have the following significance:

Bit 18(1) The card is in the off-line mode.

Bit 20(1) The hopper contains less than 100 cards.

Bit 21(1) The hopper is empty; the stacker is full; the chip box is full.

Bit 22(1) A card pick failure occurred or the card was not accepted properly by the stacker.

Bit 23(1) The card was not ejected properly.

Bit 24(1) The card punch has detected a trouble condition.

Bit 25(1) The control is enabled to request an interrupt after detecting a trouble condition.

Bit 26(1) The data punched does not agree with the contents of the card punch buffer.

Bit 27(1) A card is in the card punch station.

Bit 28(1) The card punch control is enabled to request an interrupt after punching 80 columns of data or issuance of an eject command.

Bit 29(1) 80 columns of data have been punched by the card punch or an eject command was issued.

Bit 30(1) The punch motor is on.

Bit 31(1) A card is being processed.

Bit 32(1) The CP10 Card Punch Control is requesting more data.

Bits 33-35 The priority interrupt level assignment of the CP10.

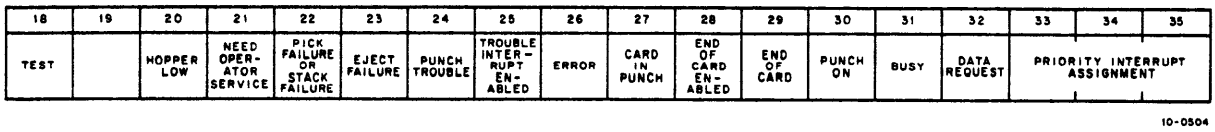


Figure 4-4 CONI Status Word

4.4.3 DATAO Instruction

The format of the data word transmitted to the card punch control logic during a DATAO is shown in Figure 4-5.

BIT	24	25	26	27	28	29	30	31	32	33	34	35
DATA	ROW 12	ROW 11	ROW 0	ROW 1	ROW 2	ROW 3	ROW 4	ROW 5	ROW 6	ROW 7	ROW 8	ROW 9

10-0490

Figure 4-5 DATAO Data Word

When a 1 is present in bits 24 through 35 of the DATAO word, a hole is punched on the card in the corresponding row. Table 4-4 provides a card code chart.

Table 4-4
Card Codes

Rows Punched	026 Data Processing	026 FORTRAN	029	DEC 026	DEC 029	Octal Representation
(None)	(Space)	(Space)	(Space)	(Space)	(Space)	0000
12	&	+	&	+	&	4000
11	–	–	–	–	–	2000
0	0	0	0	0	0	1000
1	1	1	1	1	1	0400
2	2	2	2	2	2	0200
3	3	3	3	3	3	0100
4	4	4	4	4	4	0040
5	5	5	5	5	5	0020
6	6	6	6	6	6	0010
7	7	7	7	7	7	0004
8	8	8	8	8	8	0002
9	9	9	9	9	9	0001

See notes at end of table.

Table 4-4 (cont)
Card Codes

Rows Punched	026 Data Processing	026 FORTRAN	029	DEC 026	DEC 029	Octal Representation
12-0	N/A	N/A	N/A	(See Note 1)	N/A	5000
12-1	A	A	A	A	A	4400
12-2	B	B	B	B	B	4200
12-3	C	C	C	C	C	4100
12-4	D	D	D	D	D	4040
12-5	E	E	E	E	E	4020
12-6	F	F	F	F	F	4010
12-7	G	G	G	G	G	4004
12-8	H	H	H	H	H	4002
12-9	I	I	I	I	I	4001
11-0	N/A	N/A	N/A	(See Note 2)	N/A	3000
11-1	J	J	J	J	J	2400
11-2	K	K	K	K	K	2200
11-3	L	L	L	L	L	2700
11-4	M	M	M	M	M	2040
11-5	N	N	N	N	N	2020
11-6	O	O	O	O	O	2010
11-7	P	P	P	P	P	2004
11-8	Q	Q	Q	Q	Q	2002
11-9	R	R	R	R	R	2001
0-1	/	/	/	/	/	1400
0-2	S	S	S	S	S	1200
0-3	T	T	T	T	T	1100
0-4	U	U	U	U	U	1040
0-5	V	V	V	V	V	1020
0-6	W	W	W	W	W	1010
0-7	X	X	X	X	X	1004
0-8	Y	Y	Y	Y	Y	1002
0-9	Z	Z	Z	Z	Z	1001
8-2	N/A	N/A	:	←	:	0202
8-3	#	=	#	=	#	0102
8-4	@	–	@	@	@	0042
8-5	N/A	N/A	'	↑	'	0022
8-6	N/A	N/A	=	1	=	0012
8-7	N/A	N/A	"	\	"	0006
12-8-2	N/A	N/A	¢	N/A	[	4202
12-8-3	.	.	.	.	.	4102
12-8-4	¤	)	<	)	<	4042
12-8-5	N/A	N/A	(	]	(	4022
12-8-6	N/A	N/A	+	<	+	4012
12-8-7	N/A	N/A	1	!	↑	4006
11-8-2	N/A	N/A	!	N/A	!	2202
11-8-3	$	$	$	$	$	2102
11-8-4	*	*	*	*	*	2042
11-8-5	N/A	N/A	)	[	)	2022
11-8-6	N/A	N/A	;	>	;	2012

See notes at end of table.

Table 4-4 (cont)
Card Codes

Rows Punched	026 Data Processing	026 FORTRAN	029	DEC 026	DEC 029	Octal Representation
11-8-7	N/A	N/A	¬	&	\	2006
0-8-2	N/A	N/A	"0-8-2"	;	]	1202
0-8-3	,	,	,	,	,	1102
0-8-4	%	(	%	(	%	1042
0-8-5	N/A	N/A	–	"	←	1022
0-8-6	N/A	N/A	>	#	>	1012
0-8-7	N/A	N/A	?	%	?	1006
12-11-0-1	N/A	N/A	N/A	End of file	End of file	7400
12-0-2-4-6-8	N/A	N/A	N/A	Mode switch	Mode switch	5252
7-9	N/A	N/A	N/A	Binary	Binary	XX05

1. 12-0 is converted to 12-8-2 internally in DEC 026.
2. 11-0 is converted to 11-8-2 internally in DEC 026.

4.5 GENERAL THEORY

The processor is interfaced with the CP10 Card Punch Control via the PDP-10 I/O Bus. The CP10 Card Punch Control is connected to the card punch via a device cable. (See Figure 4-6.)

To initiate a card punch operation, the program normally executes a CONO instruction with bits 25(1), 28(1), 30(1) and bits 33 through 35 equal to the priority interrupt level assignment of the CP10. The CONO instruction generates ISEL, which turns on the punch motor and conditions the card punch control to interrupt the processor (at the assigned priority interrupt level) when:

a. The card punch control requests data
b. A trouble condition is detected by the card punch
c. 80 columns of data are punched; or
d. An eject command is issued.

When the punch is ready for operation it transmits a ready (IRDY) signal to the card punch control, which generates a priority interrupt request to the processor. The program then determines the cause of the priority interrupt request by executing a CONI instruction. The program detects bit 32(1), which signals the program that the punch is on-line and requesting data.

The program then issues a DATAO instruction, which transfers one column of data to the card punch control and removes the data request and IRDY. The card punch control, in turn, outputs the data to the card punch on lines CL12 through CL09, where it is strobed by IDPS into one of the four-column buffer registers of the card punch (IRDY is also set). When the first column of data is strobed into the card punch, a card is picked from the hopper and transported toward the punch station. While the card is on its way to the punch station, the card punch control performs three additional data requests to obtain three additional columns of data and transfers them to the card punch. The card punch removes the ready signal during each data transfer. When the card is properly positioned within the punch station, all four columns of data are punched and the ready signal is transmitted to the control. At the same time, the card is advanced four columns within the punch station. The card punch control, on receipt of the ready signal, generates additional data requests to obtain each additional

column of data. The preceding operation continues until 80 columns of data are punched (IFUL), an eject command (IEJ) is issued, or a trouble (ITR) condition is detected.

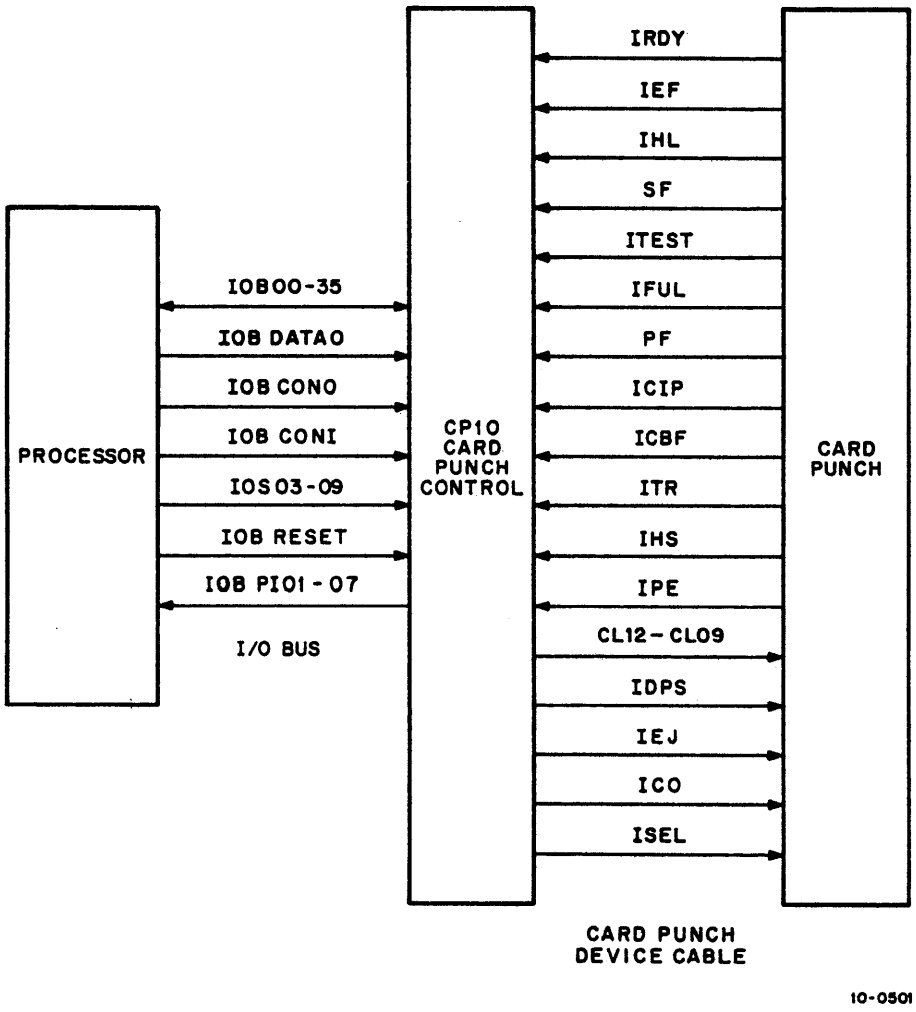


Figure 4-6 CP10 Card Punch System

The program may speed up card punch operations by issuing an eject command at any time. Also, the program must issue an eject command to place the card in the stacker. If an eject command is not issued prior to punching columns 77 through 80, the control makes another data request. The program may then supply the punch with two more columns of data, which will be punched in the card margin.

To effect an eject, the program must issue a CONO instruction with bit 23(1). IEJ is transmitted to the card punch and after punching the contents of the punch buffer, the card punch will eject the card. The card is moved out of the punch station at normal speed until column 16 is reached; then the card is moved at a speed four times as fast as the normal card speed. Issuance of the eject command or the detection of the column 80 of transferred data causes the card punch control to generate a program interrupt to the processor. The program, via a CONI, will detect the end of card condition and supply two more columns of data/issue an eject command. The program may then pick another card and proceed as mentioned above.

4.6 INTERFACE CABLE SIGNALS

Table 4-5 contains a functional description of the I/O bus. Table 4-6 contains a functional description of the CP10 Device Cable.

Table 4-5
I/O Bus Cable
(Partial Listing)

Signal Line	Function
IOB00-IOB35	Transfer status information to the processor during a CONI instruction; transfer control information to the CP10 Card Punch Control during a CONO instruction;transfer data to the CP10 Card Punch Control during a DATAO instruction.
IOB CONO CLR	Transmitted to the CP10 Card Punch Control for initialization.
IOB CONO SET	Transfers control information into the Card Punch Control 1μs after IOB CONO CLEAR.
IOB DATAO	Transfers one column (12-bits) of data to the CP10 Card Punch Control.
IOB CONI	Gates the CP10 Card Punch Control status information into the processor.
IOS03-IOS09	Transfer the device select code to the CP10 Card Punch Control.
IOB RESET	Clears the CP10 Card Punch Control Logic.
IOB PI01-PI07	Transfer the program interrupt signal to the processor.

Table 4-6
Card Punch Device Cable

Signal Line	Function
IRDY	Indicates the card punch is ready to receive data.
IEF (Eject Failure)	Indicates a card was not ejected properly.
IHL (Hopper Low)	Indicates the card punch hopper is low.
SF (Stacker Failure)	Indicates a card did not properly enter the stacker.
ITEST	Indicates the card punch is in the off-line test mode.
IFUL	Indicates the card punch has punched data column 80.
PF (Pick Failure)	Indicates a card was not properly picked.
ICIP (Card-In-Punch)	Indicates a card is in the punch station.
ICBF (Chip Box Full)	Indicates the chip box in the card punch needs to be emptied; actually, there is still enough room to accommodate the punching of one hopperful of cards.
ITR	Indicates a trouble condition has been detected by the card punch.
IHS (Hopper-Stacker)	Indicates the card punch hopper is empty or the card punch stacker is full.

Table 4-6 (cont)
Card Punch Device Cable

Signal Line	Function
IPE (Punch Error)	Indicates the incorrect data was punched.
CL12-CL09	Transfer each column of data to the card punch (in parallel).
IDPS (Data Present Strobe)	Gates the data on the CL12 through CL09 lines into the card punch; the IDPS pulse, coincident with the first column of data, causes a card to be picked and transported to the punch station.
IEJ	Ejects the card in the punch station.
ICO (Card Offset)	Offsets the card in the stacker for identification purposes.
ISEL (Select)	Turns on the punch motor, which remains on for 30s after this signal is removed.

4.7 DETAILED THEORY (See the logic drawings in the BA10 Maintenance Manual, Volume II)

In the following discussions, the operation of the card punch logic is divided into a series of cycles. These cycles have been selected to describe the circuit operation during a normal operating sequence; however, the actual operating sequence is a function of the program.

4.7.1 Punch Motor ON Cycle

The processor normally issues a CONO instruction with bit 30(1). This instruction sets the PC PUNCH ON flip-flop, which generates PC ISEL to the punch. PC ISEL turns on the punch motor.

4.7.2 Pick Cycle

After the card punch control has been conditioned for normal operation, via the CONO instruction, it monitors the ready (IRDY) signal from the card punch. IRDY generates PC BUF RDY, which sets the PC DATA REQ flip-flop. PC DATA REQ(1) causes a program interrupt request to be generated and transmitted to the processor on the priority interrupt level (PI01 through PI07) assigned by the CONO. The program, on detecting the priority interrupt request, performs a CONI instruction to determine the cause of the priority interrupt request. When the program determines that the priority interrupt is a data request (with no errors), the program executes a DATAO instruction. The DATAO CLR signal clears the PC DATA REQ flip-flop and the card punch control buffer register (CB12 through CB09). The DATAO SET signal sets the PC BUFFER FULL flip-flop. If an eject command was issued previously, the PUNCH ON flip-flop is also set. Setting PUNCH ON keeps the punch motor running. The punch motor turns off automatically after 30s with no ISEL.

THE DATAO SET signal gates the data from the I/O bus into the card punch control buffer (CB12 through CB09). The contents of the CB register are transferred to the card punch on lines CL12 through CL09. Approximately 15μs after DATAO SET is generated, PC IDPS is sent to the card punch to strobe the column of data on the CL lines into one of the four column buffers within the card punch. The PC IDPS pulse, for the first column of data, causes a card to be picked and transported to the punch station.

4.7.3 Punch Cycle

When PC IDPS is generated, PC BUFFER FULL is cleared. PC IRDY sets the PC DATA REQ flip-flop which causes another program interrupt request to be sent to the processor. The program executes another CONI

instruction and determines that a data request has been made. The program then issues another DATAO instruction to transfer the second column (12 bits) of data to the card punch as described previously. This sequence continues until the card punch has received four columns of data. The card punch then holds the ready signal false until it has punched all four columns of data onto the card. Next the card is advanced four columns in the punch station. The card punch now generates IRDY to the card punch control. The PC DATA REQ is set and the CP10 Card Punch Control obtains four more columns of data in the manner described previously. This action continues until an eject command is issued by the program.

4.7.4 End of Card Cycle

When the card punch detects column 80 of data, it generates PC IFUL. PC IFUL sets PC END OF CARD [if PC EOC ENB (1)]. PC END OF CARD then generates a priority interrupt. If the program does not issue an eject command, the control makes another data request. The program then issues an eject command or supplies two more columns of data to be punched in card columns 81 and 82 before issuing an eject command. The eject command sets PC END OF CARD, which generates an interrupt. If the program does not issue an eject command, a stack failure is detected.

4.7.5 Eject Cycle

Issuance of the eject command causes the card punch mechanism to rapidly transport the card contained in the punch station into the stacker. The eject command increases card transport speed only after column 16 has been punched.

To execute an eject command, the program must issue a CONO instruction with bit 23(1). Approximately 5μs later, the card punch control logic transmits PC IEJ to the card punch over the device cable. The card punch punches the data stored in its buffer (if any), and advances the card before it acts on the eject command. When the data has been punched, the eject solenoid magnet in the card punch is activated, pressing the eject belt against the card. This action extracts the card from the punch station toward the stacker capstan rollers at four times the normal card motion speed. Operational speeds up to 365 cards per minute can be attained by using the eject command.

4.7.6 Offset Cycle

The card offset command is issued during card processing or concurrent with an eject command. The offset command causes the card being processed to be displaced in the stacker with the edge of the card projecting from the rest of the stack. The operator is thus provided with a visual identification feature. On the console model, the eject command causes the card being processed to be placed in the alternate stacker.

To execute an offset command, the program must issue a CONO instruction with bit 21(1). PC ICO is transmitted 5 μs later to the card punch via the device cable. As the trailing edge of the card leaves the punch station (after 80 columns are punched or an eject command is issued) an offset solenoid magnet in the card punch is activated. The solenoid skews the stacker capstan rollers a few degrees, displacing the card from the rest of the stack.

4.7.7 Error Detection

The card punch control monitors the card punch for error (e.g., pick fail, stacker full, etc.). The card punch detects these errors and transmits the appropriate information to the control, which generates an interrupt to the processor. The program then executes a CONI instruction to determine the cause of the interrupt. The operator

corrects the cause of the error and places the card punch on-line before punching resumes. The types of errors are described in Paragraphs 4.7.7.1 through 4.7.7.5.

4.7.7.1 **Pick Fail** – The card punch attempts to pick a card after receiving the first PC IDPS. If the card does not reach the registration gate within a specified time after the first PC IDPS is received, the card punch makes a second attempt. If the second attempt fails, the card punch transmits PC ITR and PC PF to the card punch control. Data already sent to the punch is lost when the CLEAR button on the punch is pressed; therefore, this data must be retransmitted after the trouble is corrected.

4.7.7.2 **Eject Fail** – If the card-in-punch (ICIP) condition remains for a set time after the card punch attempts to perform an eject function, the card punch transmits PC ITR and PC IEF to the card punch control and removes PC IRDY.

4.7.7.3 **Stack Fail** – If the card punch attempts to eject a card from the read station and the previous card is in the entrance to the card stacker, the card punch transmits PC SF and PC ITR to the CP10 Card Punch and removes PC IRDY. (The previous card should have cleared the stacker entrance.)

4.7.7.4 **Hopper Empty/Stacker Full** – When the supply of cards in the hopper is exhausted, the card punch transmits PI IHS and PC ITR to the card punch control and removes PC IRDY. When the card punch stacker is full, the card punch transmits PC SF and PC ITR to the card punch control and removes PC IRDY.

4.7.7.5 **Chip Box Full** – When the chip box is full, the card punch transmits PC ICBF to the card punch control; however, there is enough room in the chip box to accommodate another stack of cards.

4.8 PUNCH ERROR

During a card punch cycle, the data in the card punch buffer and the activated punch pins are compared. If they do not agree, the card punch transmits PC IPE to the card punch control. This causes the ST PUNCH ERROR flip-flop to be set. When the end of the card (IFUL) is detected or an eject command is issued by the processor, the card punch control generates an interrupt request to the processor. The program performs a CONI instruction and determines that a PUNCH ERROR has occurred. The card punch, however, still holds the PC IRDY line to the card punch control in the true state. The program must then determine the next course of action. (The program may decide to proceed without any corrective action.) The punch check switch in the card punch must be in the ON position to perform the comparison.

4.9 TEST MODE

The card punch, in the off-line test mode, transmits PC ITEST to the CP10 Card Punch Control. PC IRDY is false at this time. The processor determines if PC IRDY is false by executing a CONI instruction. Bit 18(1) during a CONI instruction indicates the off-line test mode.

CHAPTER 5
CR10 CARD READER SYSTEM

This chapter describes programming, theory of operation, and operating information pertinent to the CR10 Card Reader System.

5.1 FUNCTIONAL DESCRIPTION

The CR10 Card Reader System (see Figure 5-1) reads standard 12-row, 80-column punched cards. Data is transferred one column at a time from the card reader to the CR10 Card Reader Control. As each column of data is received by the CR10 Card Reader Control, an interrupt request is generated informing the processor that a word is ready for transfer. The processor then inputs the data word (one column of data). When the second and subsequent columns of data are read by the card reader, the control repeats the above operation until all 80 columns of data are transferred to the processor.

Figure 5-1 CR10 Card Reader System – Functional Block Diagram

5.2 INDICATORS AND CONTROLS

5.2.1 BA10 Indicators

Table 5-1 lists the BA10 Indicators associated with the CR10 Card Reader System. Refer also to Figure 3-4.

5.2.2 Card Reader Indicators and Controls

Figure 5-2 shows the CR10A Indicator/Control Panel. Table 5-2 lists the functions of the indicators and controls for the CR10A. The indicators and controls for the CR10D, CR10E, and CR10F are shown in Figure 5-3 and explained in Table 5-3. (Figure 5-3a shows the Indicator/Control Panel for the CR10D and CR10E models; Figure 5-3b shows the CR10F Indicator Control Panel. Figure 5-3c and Table 5-4 describe the rear control panel which is common to the CR10D, CR10E, and CR10F except where noted.)

Table 5-1
BA10 Indicator Panel - Card Reader Section

Nomenclature	Function
CARD READER BUFFERS 12-09	Display the contents of the 12-bit card reader buffer register.
CIR	Indicates a card is in the card reader read station.
HOP EMPTY	Indicates the card reader hopper is empty or the stacker is full.
RDG CARD	Indicates a card is being read.
TRBL	Indicates a hopper empty, stacker full, feed error, photo error, or card motion error was detected by the card reader.
DATA MISS	Indicates the card reader has attempted to load new data into the reader control buffer before the previous data was transferred to the processor.
RDY READ	Indicates the card reader is ready for on-line operation.
EOF	Indicates the end of file button on the card reader was depressed and a trouble condition was detected by the card reader (normally hopper empty).
EOC	Indicates the card reader has detected the end of the card.
DATA RDY	Indicates the card reader control has new data in its buffer.
CR PI33-35	Indicate the priority interrupt level assignment of the CR10 Card Reader Control.
OFFSET CARD	Indicates the card reader control has received a processor command to offset the card being read by the card reader.
READ	Indicates a read command was received by the card reader control.
TRBL ENAB	Indicates the CR10 Control Logic is enabled to request an interrupt on detection of a card reader trouble condition.
RDY ENAB	Indicates the card reader control is enabled to request an interrupt when the card reader is ready for operation.
PI REQ	Indicates the CR10 Card Reader Control is requesting a priority interrupt.

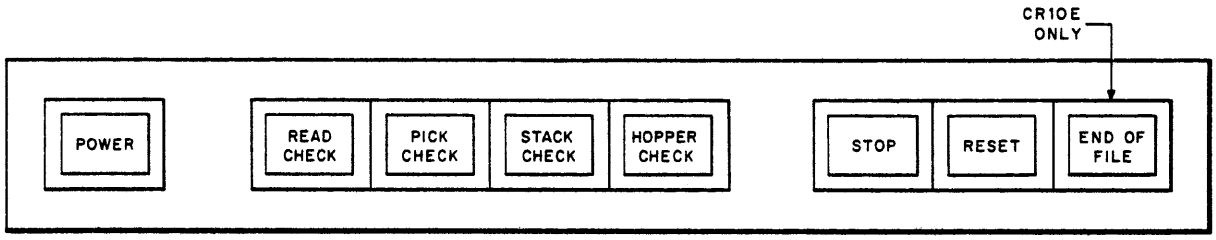
Figure 5-2 CR10A Card Reader Indicator/Control Panel

Table 5-2
CR10A Card Reader Indicator/Control Panel

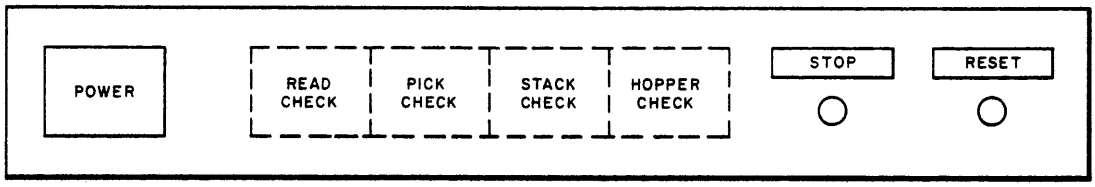
Nomenclature	Item	Function
Circuit Breaker	(Not shown in Figure 5-2)	Located at the rear of the card reader; controls the application of primary power to the card reader and protects the input source.
POWER	Alternate push switch Indicator Status: On — Color: Green Status: Off — Color: Dark	Applies power to the card reader logic and control circuits.
START	Momentary push switch Indicator Status: Start — Color: Green Status: Stop — Color: White	Places the card reader logic in the START condition (on-line); in the TEST mode, causes the picking and reading of cards off-line; operates after release of the push button.
STOP	Momentary push switch Indicator Status: Stop — Color: Yellow Status: Start — Color: White	Places the card reader logic in the STOP (off-line) condition; stops picking and reading of cards during the off-line test mode.
CLEAR	Momentary push switch Indicator Status: Trouble — Color: Red Status: No Trouble — Color: White	Clears the logic in the card reader; must be pushed to clear the logic after any trouble indication.
HOPPER EMPTY	Indicator Status: On — Color: Red Status: Off — Color: White	On (red) when there are no cards in the card reader hopper.
STACKER FULL	Indicator Status: On — Color: Red Status: Off — Color: White	On (red) when the card reader stacker contains approximately 1000 cards (2000 cards on the console version).

Table 5-2 (cont)
CR10A Card Reader Indicator/Control Panel

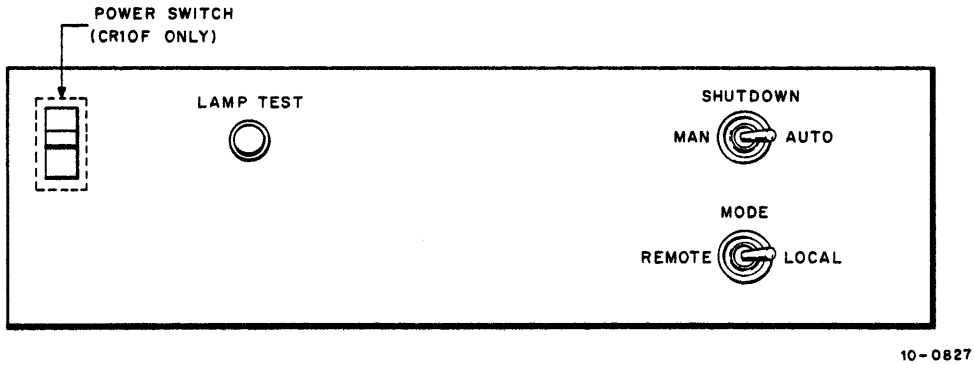
Nomenclature	Item	Function
PICK FAILURE	Indicator Status | Color On | Red Off | White	On (red) when a card does not reach the card read station in the specified time after the picker is energized.
CARD MOTION	Indicator Status | Color On | Red Off | White	On (red) if a card does not complete its pass through the read station in less than 50 ms or if the trailing edge of the card is approximately 1/3 column or more out of synchronization with the timing signals; indicates a jam or card movement error has caused the trouble signal. WARNING **If a jam occurs, depress the POWER switch to place the card reader in the power-off condition. Depressing the CLEAR switch will start the drive motor if power is on; this could cause injury to personnel. Keep clear of belts and pulleys unless power is off.**
LIGHT CURRENT	Indicator Status | Color On | Red Off | White	On (red) if any of the read station phototransistors fail to detect light between the time a card is picked and before the leading edge of the card reaches the read station; indicates a defective light source, phototransistor, or an obstruction by foreign material.
DARK CURRENT	Indicator Status | Color On | Red Off | White	On (red) if any of the read station phototransistors do not detect darkness between the leading edge of the card and column 1; indicates a malfunction in the read station or a torn or perforated leading edge, which caused the trouble signal.
TEST SWITCH	Toggle switch (not shown in Figure 5-2) ON/OFF	Located on the logic circuit assembly; in the ON position, a continuous select and read command is simulated to permit local operation of the card reader.
TEST MODE	Indicator Status | Color On | Red Off | White	On (red) when the card reader TEST switch is in the ON position. Card reader control signals have no effect when the reader is in the test mode.
END OF FILE	Momentary push switch	Generates an end of file signal.



a. Front Control Panel (CR10D, CR10E)



b. Front Control Panel (CR10F)



c. Rear Control Panel

Figure 5-3 CR10D, CR10E, and CR10F Controls and Indicators

Table 5-3
Front Panel Controls and Indicators

Control or Indicator	Type	Function
POWER	For CR10D and CR10E: alternate-action, pushbutton/indicator switch	Controls application of all power to the card reader. When indicator is off, depressing switch applies power to reader and causes associated indicator to light. When indicator is lit, depressing switch removes all power from reader and causes indicator to go out.
	For CR10F: indicator	Indicates the Power switch on the rear of the CR10F is ON.
READ CHECK indicator	white light	When lit, this light indicates that the card just read may be torn on the leading or trailing edges, or that the card may have punches in the 0 or 81st column positions. Because READ CHECK indicates an error condition whenever this indicator is lit, it causes the card reader to stop operation and extinguishes the RESET indicator.
PICK CHECK indicator	white light	When lit, this light indicates that the card reader failed to move a card into the read station after it received a READ COMMAND from the controller. Stops card reader operation and extinguishes RESET indicator.
STACK CHECK indicator	white light	When lit, this light indicates that the previous card was not properly seated in the output stacker and therefore may be mutilated. Stops card reader operation and extinguishes RESET indicator.
HOPPER CHECK indicator	white light	When lit, this light indicates that either the input hopper is empty or that the output stacker is full. In either case, the operator must manually correct the condition before card reader operation can continue.
STOP	Momentary Pushbutton/indicator switch (red light)	When depressed, immediately lights and drops the READY line, thereby extinguishing the RESET indicator. Card reader operation then stops as soon as the card currently in the read station has been read. This switch has no effect on system power; it only stops the current operation.
RESET switch	Momentary Pushbutton/indicator switch (green light)	When depressed and released, clears all error flip-flops and initializes card reader logic. Associated RESET indicator lights to indicate that the READY signal is applied to the controller. The RESET indicator goes out whenever the STOP switch is depressed or whenever an error indicator lights (READ CHECK, PICK CHECK, STACK CHECK, or HOPPER CHECK).
END OF FILE switch (CR10E only)	Momentary Pushbutton/indicator switch	Generates an end-of-file signal.

Table 5-4
Rear Panel Controls

Control	Type	Function
LAMP TEST switch	Pushbutton	When depressed, illuminates all indicators on the front control panel to determine if any of the indicator lamps are faulty.
SHUTDOWN switch	2-position toggle	Controls automatic operation of the input hopper blower. *MAN position* – blower operates continuously whether or not cards are in the input hopper. *AUTO position* – causes the blower to shut down automatically whenever the input hopper is emptied. Blower automatically restarts when cards are loaded into the hopper and the RESET switch is depressed. Blower activates approximately three seconds after RESET is depressed.
MODE switch	2-position toggle	Permits selection of either on-line or off-line operation. *LOCAL position* – removes the READ COMMAND input from the controller to allow the operator to run the reader off-line by using the RESET and STOP switches on the front control panel. Inhibits the sending of READY to controller. *REMOTE position* – enables the READ COMMAND input from the controller to allow normal on-line operation under program control once RESET is depressed.
AC Power switch (CR10F only)	2-position toggle	This circuit breaker controls all power to the reader. When the switch is in the up position, power is supplied to the entire ac distribution system and the POWER indicator on the front panel is illuminated.

5.3 OPERATING NOTES

5.3.1 CR10A Operating Procedures

Operational control of the card reader is exercised by the processor under program control after system power has been applied and the card reader start-up procedure has been performed as follows:

Step	Procedure
1	Place the TEST switch in the OFF position.
2	Depress the POWER switch to turn on power.
3	Load the card reader supply hopper.
4	Depress the CLEAR switch.
5	Depress the START switch

The card reader is now on-line (provided no errors are indicated) and ready to communicate with the BA10. The card reader is placed off-line by depressing the STOP or CLEAR button.

Loading Procedure – To load the hopper, fan the cards and jog them on a flat surface. Hold the first 100 cards (about an inch of the deck) face down, with the 12 edge (top) toward the rear of the machine, column 1 on the left. Place the deck in the hopper with the leading edge of the bottom card resting against the picker throat, then drop the cards into place. Put the remaining cards on top of the first stack. Cards may be added to the hopper while the card reader is running; however, always stop the reader before removing cards from the stacker.

5.3.2 CR10D, E, F Operating Procedures

The following paragraphs present the recommended procedures for loading the input hopper, unloading the output stacker, and correcting error conditions.

5.3.2.1 **Loading Cards** – The following procedure is used when loading the input hopper with punched cards to be read:

Step	Procedure
1	Pull the hopper follower back with one hand and begin loading card decks into the hopper. Make certain that the first card to be read is placed at the front with the "9" edge down, column 1 to the left.
2	Continue placing cards into the input hopper until it is loosely filled (this is the approximate amount of cards listed as the capacity for a particular card reader model).
	CAUTION **Do not pack the input hopper so full that the air from the blower cannot riffle the cards properly. If the cards are packed too tightly, it impairs proper operation of the vacuum picker.**
3	Cards may continue to be loaded while the reader is operating provided tension is maintained on the front portion of the deck as cards are added to the rear. Additional cards should not be loaded, however, until the hopper is approximately 1/2 to 1/3 full.
	CAUTION **When maintaining tension on the card deck, use just enough pressure to maintain the riffle action to prevent card damage and jamming of the reader.**
4	Normally, all cards are moved through the reader into the stacker. However, if it is necessary to remove cards from the input hopper, simply pull back the follower and remove the card deck.

5.3.2.2 **Unloading Cards** – To unload cards from the output stacker, pull the stacker follower back with one hand and remove the card deck from the stacker, being careful to maintain the order of the deck. The stacker may be unloaded while cards are being read.

5.3.2.3 **Correcting Error Conditions** – The four error alarm indicators on the front control panel of the card reader normally indicate a condition that can be corrected by operator intervention. These alarms, their causes, and the required operator intervention are given in Table 5-5.

Table 5-5
Error Alarm Causes and Remedies

Error Indicator	Possible Cause	Corrective Action
READ CHECK	Card edges torn. Punch in 0 or 81st column.	Remove faulty card and restart reader. If READ CHECK occurs for every card, it indicates a malfunction in the reader read logic.
PICK CHECK	Damage to leading edge. Torn webs. Cards stapled together.	Remove faulty card and restart reader. If there is no evidence of card damage, check for excessive warpage of card deck and/or a buildup of ink glaze on the picker face.
STACK CHECK	Jam in card track. Mutilated card.	Correct jam or remove mutilated card and restart reader.
HOPPER CHECK	Input hopper empty. Output stacker full.	Load input hopper. Unload output stacker.

5.3.2.4 **Operating Modes** – The CR10D, CR10E, and CR10F Card Readers can be used in either a local or remote operating mode. The local (off-line) mode is controlled by switches on the front and rear panels of the card reader. The remote (on-line) mode is controlled by programmed commands from the processor. The following paragraphs present procedures for both off-line and on-line operation of the card reader.

Off-Line Operation

Off-line operation of the card reader is used primarily to set up and check reader operation prior to switching to on-line use; to correct error conditions; and for maintenance tests. When placed off-line, the reader can be operated locally from the control panels. The following procedure is used to energize the reader and check operation off-line prior to switching to on-line operation.

Step	Procedure
1	Ensure that the ac power cord is plugged in and that the circuit breaker on the rear base panel of the reader is in the ON position.
2	Set MODE switch to LOCAL position.
3	Set SHUTDOWN switch to AUTO position.
4	Depress POWER switch to energize reader. Note that POWER indicator lights but blower does not come on.
5	Depress LAMP TEST switch and observe that all front panel indicators are lit.
6	Load a card deck into the input hopper.
7	Depress RESET switch and observe that the associated green indicator comes on. After approximately 3 seconds, cards should start being picked and moved through the read station into the output stacker.
8	When the input hopper is empty, observe that the HOPPER CHECK indicator lights, the green RESET indicator goes out, and the red STOP indicator lights.
9	The card reader may now be operated locally or switched to on-line operation.

On-Line Operation

The following procedure is used to place the card reader on-line. When placed on-line, the system is controlled by programmed commands from the processor.

Step	Procedure
1	Ensure that the card reader is operational by performing the off-line procedure.
2	Ensure the output stacker is empty. Load the input hopper with the cards to be read.
3	Set the MODE switch to REMOTE.
4	Depress the RESET switch and observe that the associated green indicator lights. The system is now on-line.
5	If the system goes off-line because of an error alarm, it can be placed back on-line by correcting the error and then depressing the RESET switch. Any time it is desired to go off-line, depress the STOP switch.

5.4 CR10 I/O INSTRUCTIONS

The card reader logic responds to three of the four basic I/O instructions. I/O instructions and their functions are listed in Table 5-6. Refer to Table 4-4 for the card codes. Refer also to the PDP-10 (DECsystem-10) System Reference Manual for additional programming information on card readers.

Table 5-6
I/O Instructions

Instruction	Function
CONO (Conditions Out)	Transfers conditions from the processor to the card reader control, directing the control to perform one or more of the following: *a.* Clear the control logic *b.* Load the priority interrupt channel number into the priority interrupt register *c.* Pick a card from the card reader hopper *d.* Generate an offset command *e.* Enable reader trouble/ready-to-read priority interrupts.
CONI (Conditions In)	Transfers card reader control status information to the processor.
DATAI (Data In)	Transfers data from the card reader control buffer register to the processor.
DATAO (Data Out)	Not used by the card reader control.

5.4.1 CONO Instructions

The format of the conditions out word transferred to the card reader control logic during a CONO is shown in Figure 5-4.

23	24	25	26	27	28	29	30	31	32	33	34	35
CLEAR READER	OFFSET CARD		READ CARD	ENABLE TROUBLE INTER-RUPTS	CLEAR DATA MISSED	ENABLE READY TO READ INTER-RUPTS	CLEAR END OF FILE	CLEAR END OF CARD	CLEAR DATA READY	PRIORITY INTERRUPT ASSIGNMENT		

10-0503

Figure 5-4 CONO Conditions Word

The CONO bits have the following significance:

Bit 23(1) Clears the card reader control logic.
Bit 24(1) CR10A, CR10B offsets the card when it is loaded into the stacker.
CR10E, CR10D, CR10F, not used.
Bit 26(1) Causes a card to be read.
Bit 27(1) Enables priority interrupt requests when a card reader trouble condition is detected.
Bit 27(0) Disables priority interrupt requests from being generated when a card reader trouble condition is detected.
Bit 28(1) Clears the data missed flag.
Bit 29(1) Enables priority interrupt requests if the card reader is ready for operation.
Bit 29(0) Disables ready for operation interrupts.
Bit 30(1) Clears the end of file flag.
Bit 31(1) Clears the end of card flag.
Bit 32(1) Clears the data ready flag.
Bits 33-35 Set the priority interrupt channel assignment of the CR10 Card Reader.

5.4.2 CONI Instruction

The format of the status word transferred to the central processor during a CONI is shown in Figure 5-5.

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
READER MODEL		TROUBLE INTER-RUPT EN-ABLED	READY TO READ INTER-RUPT ENABLED	PICK FAILURE	PHOTO-CELL ERROR	CARD MOTION ERROR	STOP	CARD IN READER	HOPPER EMPTY-STACKER FULL	READING CARD	TROUBLE	DATA MISSED	READY TO READ	END OF FILE	END OF CARD	DATA READY	PRIORITY INTERRUPT ASSIGNMENT		

10-0506

Figure 5-5 CONI Status Word

The CONI bits indicate the following:

Bits 16, 17 Indicates the type of card readers being used and is decoded as follows:

Bit 16	Bit 17	Reader Model
0	0	CR10A or B
0	1	CR10D
1	0	CR10E
1	1	CR10F

Bit 18(1) The CRCN READER TRBL ENAB flip-flop is set and an interrupt will be generated on detection of a trouble condition.
Bit 19(1) The CRCN READY ENAB flip-flop is set and an interrupt will be generated when a ready condition is detected.
Bit 20(1) The card reader did not pick a card when the command (IRC) was routed to the card reader.
Bit 21(1) The card reader failed the light/dark current test due to a defective light source, foreign material in the read station, or a defective card.
Bit 22(1) A card has slipped or jammed while moving through the card reader.

Bit 23(1) The card reader power is on, but the card reader is off-line due to an error condition or the STOP switch was depressed.

Bit 24(1) The card is actually in the card reader station.

Bit 25(1) The card reader hopper is empty or the stacker is full.

Bit 26(1) The card reader is reading a card.

Bit 27(1) The card reader has detected trouble; this signal is generated by one of the following conditions:

a. STOP button depressed

b. Hopper empty or stacker full

c. Card reader failed the light/dark current test

d. Card motion error – the card is slipping or jammed in the reader or the card reader is off-line.

NOTE

All of the above conditions require operator intervention. The card reader has indicators that allow the operator to determine the source of trouble.

Bit 28(1) The processor failed to read a column of data before the card reader transferred new data into the control. Except for column 80, the data must be read into the processor via a DATAI within approximately 350 μs after the DATA READY program interrupt.

Bit 29(1) The card reader control is ready to receive a read command.

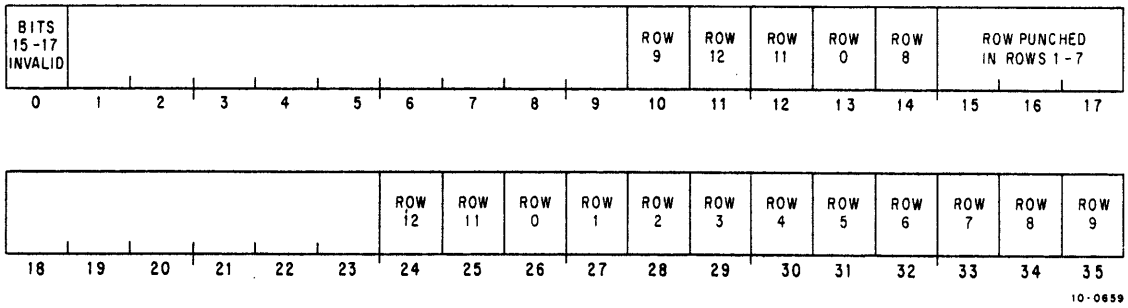
Bit 31(1) The end of the card has been detected.

Bit 32(1) A column of data is ready to be transferred to the processor.

Bits 33-35 The priority interrupt channel register is set.

5.4.3 DATAI Instruction

The format of the data word transferred to the central processor during a DATAI is shown in Figure 5-6. The card codes are listed in Table 4-4.



NOTE

If bit 0 is 0, bits 15–17 hold the octal row number of the single punch in rows 1–7 (zero indicates no punch). However, if bit 0 is 1, there is more than one punch in rows 1–7 and bits 15–17 are meaningless.

Figure 5-6 DATAI Data Word

5.5 GENERAL THEORY

Throughout the remainder of this section on card readers, the signal designations are presented with the Documation reader (CR10D, E, and F) signals listed first followed, in parentheses, by the Mohawk Data Sciences reader signals (CR10A, B).

The processor is interfaced with the CR10 Card Reader Control via the PDP-10 I/O Bus (see Figure 5-7). The CR10 Card Reader Control is interfaced with the card reader via a device cable. After the operator performs the card reader start-up procedure outlined in Paragraphs 5.3.1 and 5.3.2, the program issues a CONO instruction with bits 27(1), 29(1), and bits 33 through 35 set to the priority interrupt level assigned to the CR10. This conditions the card reader control to generate an interrupt, on the assigned level, when the card reader is ready for operation or when a trouble condition is detected.

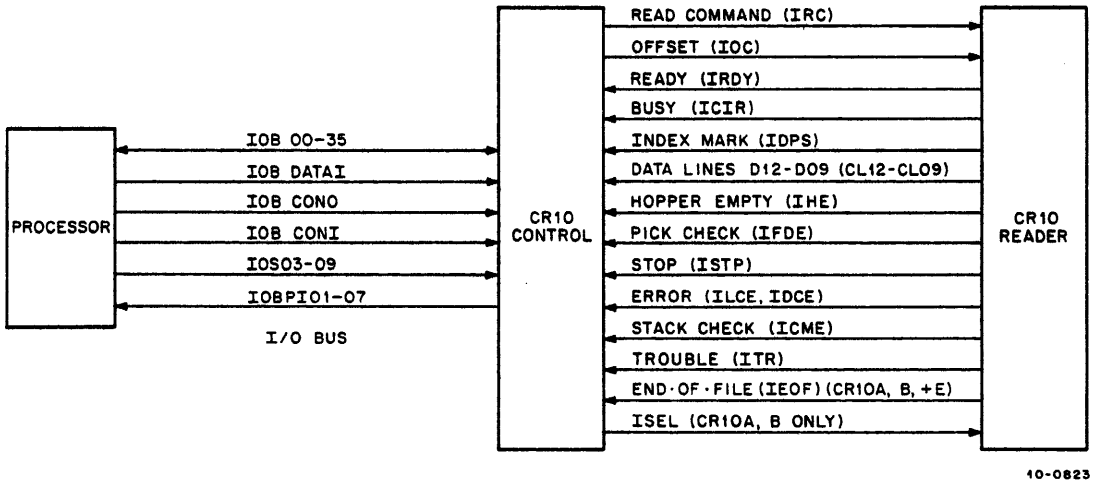


Figure 5-7 CR10 Card Reader System

When the READY (IRDY) signal from the card reader is detected, the card reader control logic generates a priority interrupt request to the processor on the assigned priority interrupt line of the I/O bus. The program then performs a CONI instruction to service the priority interrupt and detects the ready-to-read condition.

5.5.1 Pick Cycle

The program performs a CONO instruction, which causes the card reader control logic to generate the read command (IRC). The card reader responds to the read command by removing a card from its hopper and transporting the card toward the read station. The BUSY (ICIR) signal goes true when the leading edge of the card enters the read station. Before the first card column reaches the read station, the card reader performs a light/dark current test to ensure normal read station operation.

5.5.2 Read Data Cycle

The first card column is read photoelectrically and the data is placed on data lines D12 through D09 (CL12 through CL09) of the card reader device cable. The IM Index Mark (data strobe (IDPS)) signal is then generated by the card reader and is sent to the card reader control logic. IM (IDPS) gates the data into a buffer register where it is temporarily stored. A priority interrupt request is then generated and sent to the processor on the assigned priority interrupt line.

To service the priority interrupt request, the program performs a CONI instruction, which transfers the contents of the status register into the processor via data lines IOB00 through IOB35 of the I/O bus. Bit 32(1) indicates the presence of data in the card reader control buffer register.

5.5.3 Data Transfer Cycle

The program executes a DATAI instruction to fetch the data stored in the buffer register. Since the card continuously moves through the read station, the processor has approximately the time listed in Table 5-7 to complete each data transfer cycle without missing data. After the specified time, data in the next card column are placed on the data lines of the card reader device cable and are strobed into the buffer register. The read data and data transfer cycles are performed as explained above to transfer the next column of data. This action is repeated until all 80 card columns have been read. The card is then transported out of the read station and is loaded into the card reader stacker.

Table 5-7
Data Transfer Cycle Periods

Card Reader	Time-μs
CR10A	350
CR10D	478
CR10E	405
CR10F	2000

After the last card column leaves the read station, the BUSY (ICIR) signal from the card reader goes false. BUSY (ICIR) false clears the reading card flip-flop, and sets the end of card flip-flop, which causes a priority interrupt request. The program performs a CONI instruction to service the priority interrupt request and examines the contents of the status register. The status information informs the program that the end of card has been detected. A CONO instruction is then performed to clear the end of card flip-flop, thereby clearing the priority interrupt request.

The program then issues a CONO instruction to set the read flip-flop, which conditions the control logic to pick the next card. After the card leaves the read station, the READY (IRDY) signal from the card reader becomes true and a read command (IRC) is generated (assuming there is no trouble and that more cards are in the hopper). When the read command (IRC) is sent to the card reader, the next card is picked from the card reader hopper.

Additional status information is generated in the card reader control logic and routed to the processor during a CONI instruction to inform the processor of a change in status. Status changes indicate the following:

a. Missed data indicates the data transfer cycle was not completed before the next card column was read (the original data is overwritten in the card reader control).
b. Card reader trouble indicates a hopper empty, stacker full, pick error, light/dark current error, card motion error, or card reader off-line.
c. End of file (EOF) indicates the operator has depressed the card reader EOF switch to signify that the last card of a file has been read (models CR10A, B, and E only).

5.6 INTERFACE CABLE SIGNALS

Table 5-8 lists the functions of the I/O bus cable. Table 5-9 lists the functions of the CR10 Device Cable.

Table 5-8
I/O Bus Cable (Partial Listing)

Signal Line	Function
IOB00-IOB35	Transfer data and status information to the processor and control signals to the card reader control logic; in the CR10, only IOB18 through IOB35 are used.
IOB DATAI	Gates data into the processor and clears the data ready flag.
IOB CONO CLEAR	Clears the card reader control logic and sets the read, trouble enable/ready enable flip-flops (when requested).
IOB CONO SET	Gates the assigned priority interrupt channel number into the priority interrupt register, clears the card reader control logic/generates an offset command, 1 μs after IOB CONO CLEAR.
IOB CONI	Gates the card reader status into the processor.
IOB03(0)-IOB09(1)	Transfer the device number to the card reader control logic.
IOB RESET	Clears the card reader control logic.
IOB PI01-IOB PI17	Transfer the priority interrupt signal to the processor.

Table 5-9
Card Reader Device Cable

Signal Line	Function
Pick Check (IFDE)	Indicates that the card reader failed to pick a card.
IM (IDPS)	Generates a load buffer pulse after the data has settled on the data lines; causes a priority interrupt.
ISEL	Selects the card reader (always true). For CR10A and CR10B only.
Ready (IRDY)	Indicates the card reader is ready to accept a read command.
Trouble (ITR)	Indicates a card reader trouble condition is detected.
Hopper Empty (IHE)	Indicates the card reader hopper is empty.
IOSF (Output Stacker Full)	Indicates the stacker is full.
Busy (ICIR)	Indicates a card is in the read station.
End of File (IEOF)	Represents pressing of the EOF switch.
Read Command (IRC)	Starts the pick cycle.
Offset (IOC)	Causes a card in the stacker to be offset for identification.
Error (ILCE, IDCE)	Indicates a light or dark current error.
Stack Check (ICME)	Indicates a card has jammed or slipped.
Stop (ISTP)	Indicates card reader power is on, but the card reader is off-line.
D12–D09 (CL12–CL09)	Transfer the 12 bits of data from the card reader to the buffer register in the card reader control logic; the order of bits from the most significant bit to the least significant bit is: CL12, CL11, CL00 through CL09.

5.7 DETAILED THEORY (Refer to BA10 Maintenance Manual, Volume II)

In the following discussions, the operation of the card reader logic has been divided into a series of cycles. Although the actual operating sequence is a function of the program, these cycles have been selected to describe the circuit operation during a normal operating sequence.

5.7.1 Pick Cycle

After the card reader control logic has been conditioned for normal operation, it monitors the READY (IRDY) signal from the card reader. To generate READY (IRDY) the card reader must be on-line as described in Paragraphs 5.3.1 and 5.3.2. IRDY generates CRCN READY. The card reader system is now conditioned for operation by the program.

To initiate a pick cycle, the processor issues a CONO instruction to the card reader control. When the CONO CLEAR pulse is sent to the control, the following functions are performed:

IOB26(1)	CRCN READ flip-flop is set; a card is picked from the card reader hopper and transported toward the read station.
IOB27(1)	CRCN READER TRBL ENAB flip-flop is set; priority interrupt request is generated if a trouble condition is detected in the card reader.
IOB27(0)	CRCN READER TRBL ENAB flip-flop is cleared.
IOB28(1)	CRST DATA MISSED flip-flop is cleared.
IOB29(1)	CRCN READY ENAB flip-flop is set; priority interrupt request is generated when an IRDY signal is received from the card reader.
IOB29(1)	CRCN READY ENAB flip-flop is cleared.
IOB30(1)	CRST END OF FILE flip-flop is cleared.
IOB31(1)	CRST END OF CARD flip-flop is cleared.
IOB32(1)	CRST DATA READY flip-flop is cleared.

Assume that IOB26 through IOB32 are equal to 177_8. When CRCN READ is set, it is ANDed with CRCN READY and triggers a 25-μs pulse (CRCN READ CARD) that is sent to the card reader on line Read command (IRC). This signal causes a card to be picked and transported toward the card reader read station. When the card is picked, READY (IRDY) becomes false. The CRCN READ CARD pulse also sets the CRST READING CARD flip-flop. At the end of CRCN READ CARD, the CRCN READ flip-flop is cleared. When the CONO SET pulse occurs, the following functions are performed:

IOB23(1)	The card reader control logic is cleared.
IOB24(1)	A card offset command is generated.
IOB33-IOB35	The priority interrupt channel is assigned.

If IOB33 through IOB35 are equal to 7_8, CRST PI33 through CRST PI35 are set to 7_8.

5.7.2 Read Data Cycle

When the card has been picked, it is moved continuously through the read station and is deposited in the stacker. The read station contains a beginning-of-card phototransistor and light source, 12 data phototransistors and 12 light sources aligned to match the 12 data rows on the card, and an end-of-card phototransistor and light source. The card reader performs a light current check before the card enters the read station to ensure that the phototransistors detect light. The card reader also performs a dark current check after the card reaches the beginning of card phototransistor, but before the first data column reaches the 12 data phototransistors. In this way, the ability of the data phototransistors to detect light and dark current conditions is ensured prior to reading data. If the phototransistors are not operating properly, the light or dark current error lines are held true.

The card reader generates the BUSY (ICIR) signal before the first column of data is read and removes BUSY (ICIR) after the last column of data is read. BUSY (ICIR) generates CRCN CARD IN READER.

When a column of data passes between the 12 data phototransistors and their associated light sources, any hole punched in that row admits light and activates the associated phototransistor. The resultant signals are gated onto the card reader device cable on lines D12 through D09 (CL12 through CL09).

As a column of data passes between the 12 data phototransistors and light sources, a series of timing pulses are generated for that column by a reluctance pickup head, which is synchronized with the card drive mechanism. These timing pulses generate an index mark pulse IM (IDPS) for that column of data after the data has been placed on lines D12 through D09 (CL12 through CL09). The IM (IDPS) signal is sent over the device cable to the card reader control. This pulse generates CRCN LOAD BUFFER, which gates the data on lines D12 through D09 (CL12 through CL09) into the buffer register CRBF12 through CRBF09. CRCN LOAD BUFFER also sets the CRST DATA READY flip-flop to generate a priority interrupt request to the processor on line PI07.

The program services the interrupt request by performing a CONI instruction. During the CONI instruction the IOC CR CONI level gates the outputs of the status gates onto the I/O bus. The program, after examining the status information, will determine the following:

a. A card is in the reader, IOB26(1)
b. Data is ready to be transferred, IOB32(1)
c. The priority interrupt level assignment is 7_8 (IOB33-IOB35 = 7_8).

The read data cycle is now complete and the card reader control is conditioned for a data transfer cycle. After the data transfer cycle is completed, another read data cycle is performed to obtain the next column of data. The read data and data transfer cycles are repeated alternately until the end of card is reached, a card reader trouble condition is detected, the end of file is reached, or a column of data is missed.

5.7.3 Data Transfer Cycle

To review the sequence up to this point, one column of data has been read from a punched card and stored in the card reader control buffer register. A priority interrupt request caused the program to perform a CONI instruction to determine that the card reader control has a column of data ready to be transferred. The program then performs a DATAI instruction to fetch the data in the buffer register. The processor sends the IOB DATAI signal to the card reader control, which generates IOC CR DATAI. IOC CR DATAI gates the data onto I/O bus lines IOB24 through IOB35, which connect to the processor. The trailing edge of the IOC CR DATAI signal clears the CRST DATA READY flip-flop. When CRST DATA READY becomes false, the priority interrupt request is cleared and the card reader control logic is ready for the next read data cycle. A data transfer cycle is performed after each read data cycle until 80 columns have been read and the end of a card is reached. At this time the end of card cycle begins.

5.7.4 End of Card Cycle

When the end of card is reached, the BUSY (ICIR) signal from the card reader becomes false after the last card column of data is read. When BUSY (ICIR) becomes false, CRCN CARD IN READY becomes false, setting the CRST END OF CARD flip-flop.

END OF CARD(1) generates a priority interrupt request to the processor via the assigned priority interrupt line. The program services the priority interrupt request by performing a CONI instruction. The IOC CR CONI signal reads the following status information into the processor:

IOB24(0)	Indicates a card is not present in the reader
IOB26(0)	Indicates a card is not being read
IOB31(1)	Indicates the end of a card has been reached.

The program then performs a CONO instruction with IOB31(1) to clear the END OF CARD flip-flop, thereby removing the interrupt request.

If there are additional cards to be read and no trouble is indicated, the program performs a CONO instruction with IOB26(1) to set the CRCN READ flip-flop. Approximately 8 ms after the last card column is read, the READY (IRDY) signal from the card reader becomes true, generating CRCN READY. The CRCN READY signal is ANDed with CRCN READ to enable the CRCN READ CARD signal. The CRCN READ CARD signal, a 25-μs pulse, generates a Read Command (IRC) signal to initiate another pick cycle as described in Paragraph 5.7.1.

If the CRCN READ flip-flop has not been set before the CRCN READY signal is generated, the CRCN READ CARD signal is not enabled by CRCN READY. To indicate the presence of the READY (IRDY) signal under these conditions, the CRCN READY TO READ signal is generated and ANDed with CRCN READY ENAB. If CRCN READY ENAB is set, CRCN RDY TO READ PI signal is generated. The priority interrupt decoder is enabled and a priority interrupt request is sent to the processor. The program services the priority interrupt request by performing a CONI instruction to fetch the status information. During the transfer, IOB29(1) indicates the card reader is in the ready condition.

5.7.5 Data Missed Cycle

The program has approximately the time listed in Table 5-7 to perform a CONI instruction, to discover the data is ready, and to execute a DATAI instruction to fetch the data stored in the buffer register.

The performance of these instructions requires only a few microseconds; however, the processor might be engaged in higher priority transfers and the next column of data might be transferred into the buffer register before the processor has fetched the previous data.

When the processor fails to fetch a column of data before the next column of data is read, the DATA MISSED flip-flop is set, and a priority interrupt request is sent to the processor via the I/O bus. In this instance, the CRST DATA READY(1) signal conditions the set gate of the CRST DATA MISSED flip-flop. CRST DATA READY(1) signal remains true until the data in the buffer register is transferred into the processor. When the CRCN LOAD BUFFER pulse is generated, the CRST DATA MISSED flip-flop is set.

To service the priority interrupt, the program performs a CONI instruction to fetch the status information. IOB28(1) indicates the loss of data. Under these circumstances, the program must perform a CONO instruction with IOB28(1) to clear the CRST DATA MISSED flip-flop and remove the priority interrupt request. The program must also take appropriate action to indicate the occurrence of this error to the user.

5.7.6 Fault Location Cycle

The card reader logic constantly checks for malfunctions during normal read operations. If a malfunction is detected, a trouble signal is routed to the card reader control logic; a card reader indicator that identifies the malfunction is illuminated; and the card reader drive motor is stopped after the read station is cleared.

When a trouble condition is detected in the card reader, the trouble (ITR) signal is sent to the card reader control to generate the CRCN READER TROUBLE signal. The CRCN READER TROUBLE signal is ANDed with CRCN TRBL ENAB to generate the CRCN READER TROUBLE PI signal. A priority interrupt request is then routed to the processor via the assigned priority interrupt line.

The program services the priority interrupt request by performing a CONI instruction. During the CONI instruction, the processor discovers IOB27(1), indicating a card reader trouble. The ITR signal remains in the true condition and the program interrupt remains on the I/O bus until the trouble is corrected and the card reader CLEAR and START switches are depressed; or the priority interrupt channel is set to a 0_8; or the trouble enable flip-flop is cleared.

5.7.7 End of File Cycle

The card reader control logic provides the program with an end of file (IEOF) indication. The end of file circuit remains disabled until the operator has depressed the card reader EOF switch and the last card in the hopper has been read (generating a hopper empty). The CRCN HOPPER EMPTY and IEOF signals are ANDed to set the CRST END OF FILE flip-flop. When a priority interrupt request is sent to the processor, the program performs a CONI instruction to service the priority interrupt request and fetch the status information that indicates the following:

IOB24(0)	A card is not present in the read station
IOB25(1)	The hopper is empty
IOB26(0)	A card is not being read
IOB27(1)	A reader trouble condition has been detected
IOB30(1)	The end of file button has been activated
IOB31(1)	The end of a card has been reached.

To remove the EOF program interrupt request, the processor performs a CONO instruction with IOB30(1).

5.7.8 Hopper Empty/Stacker Full (IHE/IOSF) Cycle

During normal operation, the hopper may become empty. When this condition occurs, the card reader drive motor is stopped and the card reader HOPPER CHECK indicator is illuminated. The trouble (ITR) signal and hopper empty (IHE) (or IOSF) signals are generated by the card reader and sent to the card reader control logic.

The trouble (ITR) signal causes the CRCN READER TROUBLE signal to be generated. Meanwhile, the hopper empty (IHE) (or IOSF) signal causes the CRCN HOPPER EMPTY signal to be generated. The CRCN READER TROUBLE signal is ANDed with CRCN READER TRBL ENAB. The resultant signal, CRCN READER TROUBLE PI, causes a priority interrupt request to be sent to the processor. The program services the priority interrupt request via a CONI instruction. During the CONI instruction, the following status information is routed to the processor:

IOB25(1)	Indicates the hopper is empty
IOB27(1)	Indicates the card reader trouble
IOB33-35	Denotes the priority interrupt channel assignment number.

To restart the card reader, the operator must load the hopper or clear the stacker and depress the card reader CLEAR and START switches.

5.7.9 Card Offset Cycle (applicable to CR10A and CR10B only)

The card offset cycle provides the operator with a visual indication of a program selected card by offsetting the card as it enters the stacker. To offset the card, the program performs a CONO instruction with IOB24(1) while the CRCN CARD IN READER signal is true. The CRCN CARD IN READER signal triggers a 25-μs one-shot (CRCN OFFSET CARD). CRCN OFFSET CARD generates an offset card (IOC) signal, which is sent to the card reader via the card reader device cable.

In the card reader, the IOC signal energizes the offset solenoid located at the stacker capstan. When the solenoid is energized, the card in the capstan is offset and deposited on the deck in the stacker with its edge protruding about 0.25 in. (In the console model card reader, the card is deposited in the alternate stacker.)

When IOC becomes false, the offset solenoid is de-energized. The next card can be picked and the read data and data transfer cycles can be started before the offset cycle is completed.

5.7.10 Clear Cycle

The processor clears the reader control logic by two methods. The first method involves the execution of a CONO instruction with bit 23(1). After input buffering, the resultant signal, IOB23B, is applied to the input gate of the 1-μs one-shot IOC CR CONO RESET DLY. When the IOC CR CONO SET pulse occurs, the one-shot is triggered. The trailing edge of IOC CR CONO RESET DLY generates IOC CR CLEAR. The IOC CR CLEAR signal generates IOC CR CONO CLEAR. The occurrence of these signals clears the card reader control logic flip-flops, buffers, and priority interrupt registers.

Using the second method, the processor generates the IOB RESET signal in one of several ways and routes the IOB RESET signal to the card reader control logic. IOB RESET generates the IOC CLEAR signal. The IOC CLEAR signal conditions the reset circuits in the manner explained in the preceding paragraph.

CHAPTER 6
LP10 LINE PRINTER SYSTEM

This chapter describes programming, theory of operation, and operating information pertinent to the LP10 Line Printer System.

6.1 FUNCTIONAL DESCRIPTION

The LP10 Line Printer System (see Figure 6-1) provides the user with a hard copy printed output. Under program control, the LP10 Line Printer Control Logic accepts data from, or transmits status information to, the processor. Each data word includes characters to be printed, control characters that cause printing/spacing, or illegal characters (codes ignored by the line printer). The rate of transfer is determined by the type of line printer. Five characters at a time are transferred from the processor to the line printer control where they are decoded and transmitted to the printer without further program intervention. The line printer, via the priority interrupt system, informs the program that the line printer requires attention. Status indications are DONE (ready for data), BUSY (line printer is busy performing some function), and PRINTER ERROR (line printer off-line, interface cable disconnected, printer out of paper, etc.).

Figure 6-1 LP10 Line Printer System – Functional Block Diagram

6.2 INDICATORS AND CONTROLS

Table 6-1 lists the BA10 Indicators associated with the LP10 Line Printer System (refer to Figure 3-4). Table 6-2 lists the functions of the LP10A, B, C, D, and E Indicator/Control Panel. Table 6-3 lists the functions of the LP10F and LP10H Indicator Control Panel shown in Figure 6-2. Table 6-4 describes the LP10F and LP10H Test Panel (Figure 6-3). Table 6-5 describes the various maintenance and adjustment controls.

Table 6-1
BA10 Indicator Panel – Line Printer Section

Nomenclature	Function
LINE PRINTER BUFFERS 0-34	Display the contents of the line printer buffer register.
SHIFT CNT 0-12	Keep track of the number of times the buffer register is shifted when outputting data to the line printer.
COLUMN COUNTERS 0-7	Display the number of printable characters sent to the line printer since the last PRINT or PRINT AND SPACE command.
BUFFER AVAIL	Indicates the line printer is ready to accept data.
ALT	Indicates the line printer control has detected a delete character; applicable only to LP10D and LP10E Line Printers.
CLR SYNC	Indicates the line printer control is being initialized.
SHIFT SYNC A SHIFT SYNC B	Indicate two flip-flops, which control the shifting of the data buffer while outputting data to the line printer.
DATO SYNC	Indicates the processor is loading the LP10 Control Buffer with new data.
CONO PRINT	Set as the result of a line overflow error; a line overflow error indicates the program has attempted to exceed the column capacity of the line printer.
LPI ERR	Indicates a malfunction was detected in the line printer.
BUSY	Indicates the line printer control is performing an operation.
DONE	Indicates the line printer control has completed a successful operation and is awaiting more data.
LP PIB30-32	Indicate the priority interrupt level at which the line printer control will interrupt the processor on detecting an LPI error.
LP PIA33-35	Indicate the priority interrupt level at which the line printer control will interrupt the processor on detecting the DONE flag.

6.3 OPERATING NOTES (Line Printer Start-Up Procedure)

The processor operationally controls the line printer, under program control, after system power has been applied, and after the line printer start-up procedure has been performed as follows:

Step	Procedure
1	Install paper or forms into the line printer (refer to the line printer maintenance manual).
2	Depress ON switch on the LP10A, B, C, D, and E line printer; put POWER circuit
3	breaker to ON position on models LP10F and LP10H. Depress START switch on LP10A, B, C, D, or E Line Printer; press and release ON LINE switch for models LP10F and LP10H.

The line printer is now on-line (provided no errors are indicated) and is ready to communicate with the LP10 Line Printer Control.

Table 6-2
LP10A, B, C, D, and E Line Printer Indicator/Control Panel

Nomenclature	Item	Function
OFF	Momentary push switch Indicator	Removes power from the line printer.
ON	Momentary push switch and Indicator	Applies power to the line printer.
TEST PRINT	Momentary push switch and Indicator	Causes the character determined by the internal switches b1 through b7 to be continuously printed on all columns (when the line printer is off-line); the hammer enable (internal switch) must be in the HAMMER ENABLE position.
START	Momentary push switch and Indicator	Places the line printer on-line.
STOP	Momentary push switch and Indicator	Places the line printer off-line.
TOP OF FORM	Momentary push switch and Indicator	Advances paper to the top of form when the line printer is off-line.
NO PAPER	Indicator	Indicates the line printer is out of paper.
PAPER LOW ALERT	Indicator	Indicates the last available page is being printed.
YOKE OPEN	Indicator	Indicates the line printer yoke is open.
MANUAL PRINT	Momentary push switch and Indicator	Prints out the characters in the line printer buffer, which have not been printed when the line printer goes off-line.
ALARM STATUS	Indicator	Indicates the line printer has detected a blown fuse, bad lamp, or some other malfunction.
REMOTE/CONTROL	Toggle switch	In the REMOTE position it allows power to be turned on only if power is applied to the BA10; in the LOCAL position it allows power to be applied independent of the BA10.

Table 6-3
LP10F and LP10H Line Printer Indicator/Control Panel

Nomenclature	Item	Function
DRUM SPEED	Switch	Selects high or low speed as indicated. **CAUTION** **Switch power off or unlatch the drum gate latch before changing the drum speed. The drum motor must not be operating when making this speed adjustment.**
POWER	Circuit breaker	Applies ac power to printer. When ON, POWER indicator illuminates if primary power is applied to printer.
PHASE	Vernier control	The PHASE control synchronizes the initiation of hammer motion with the precise position of the drum character to ensure optimum print quality. The PHASE control adjustment is only used to maintain equal printing density at top and bottom of the characters.
PENETRATION	Vernier control	The PENETRATION control allows the user to change the print density. By adjusting the PENETRATION potentiometer, a change in the hammer penetration force of approximately 20% from its normal setting is obtainable. Typical uses of the PENETRATION control include: a. Compensating for the difference in print density between a new ribbon and an old ribbon. b. Matching the print density of a pre-printed form, and improving the quality of a multi-form copy.
DRUM GATE	Indicator	Lights when the drum gate is unlatched.
PAPER FAULT	Indicator	Lights when one or more of the following conditions occurs: a. TOP PAPER BREAK switch is open. b. Ribbon counter alarm. c. Tape reader gate is open. d. Paper runaway fault. The PAPER FAULT indicator will go off when the PRINT INHIBIT indicator is on.
PRINT INHIBIT	Indicator	Lights when PRINT INHIBIT switch is on (UP position). **NOTE** **When PRINT INHIBIT lamp is illuminated, the READY lamp, ON LINE lamp and PAPER FAULT lamp will go off.**

Table 6-3 (Cont.)
LP10F and LP10H Line Printer Indicator/Control Panel

Nomenclature	Item	Function
MASTER CLEAR	Switch	Initializes the printer to ensure that logic elements are in proper state. In addition, when the MASTER CLEAR switch is pressed, the following functions take place: a. READY indicator goes off. b. ON LINE indicator goes off. c. Operation of TOP OF FORM switch is inhibited. d. Operation of TEST MODE switch is inhibited. e. Operation of ON/OFF LINE switch is inhibited. f. Operation of runaway fault is inhibited.
POWER	Indicator	Lights when power is applied to printer.
READY	Indicator	Lights approximately 5 seconds after initial power on. When ON, indicates the following: a. TOP PAPER BREAK switch is closed. b. BOTTOM PAPER OUT switch is closed. c. Tape reader gate is closed. d. No runaway fault. e. No hammer protect fault. f. No Print Inhibit.
ON LINE	Indicator	Lights when READY indicator is on and only after release of ON/OFF LINE switch. **NOTE** **ON LINE indicator will go off when PRINT INHIBIT indicator is on.**
TOP OF FORM	Switch	When pressed and released, allows paper tractors to be advanced 1 line (with no tape installed in tape reader). When tape is installed in tape reader, this switch allows paper tractors to be advanced at slew rate for approximately 1 second. This advance is controlled via channel 0 in the tape reader and will effectively advance the tractors to the top of form position.
TEST MODE	Switch	When pressed and released, allows the decode switches (1-7) on the test panel to be used for entering data. During the test mode, the TEST MODE indicator is lit and a continuous line of each character selected is printed.
ON/OFF LINE	Switch	When pressed and released, enables printer to enter on-line mode. If printer was on-line (ON LINE indicator lit), enables printer to exit on line mode after switch is released.

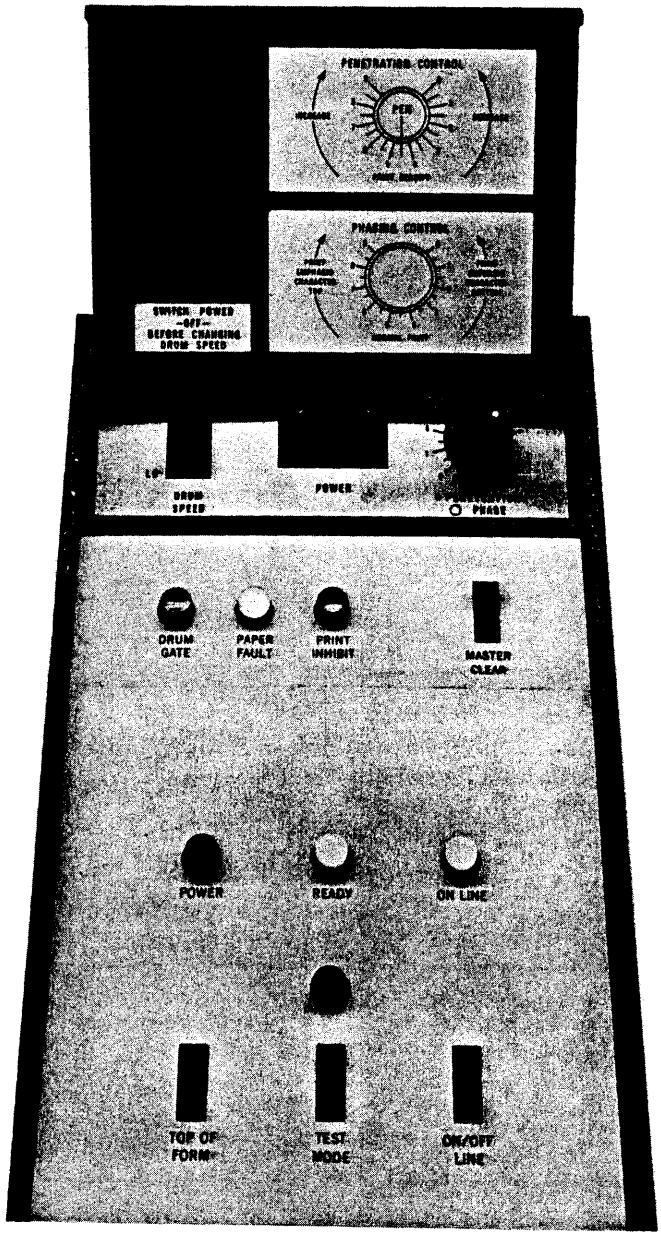


Figure 6-2 LP10F, H Indicator/Control Panel

Table 6-4
LP10F and LP10H Test Panel Switches

Nomenclature	Item	Function
Data Switches 1 through 7	Toggle switches	Used to decode any characters on the drum or VFU channel in off-line mode.
FORM NOT-FORM	Toggle switch	In the FORM position, when TEST MODE is pressed, the data switches on the test panel select any of the eight VFU channels and paper is slewed accordingly. In the NOT-FORM position, when TEST MODE is pressed, the VFU is not selected and printing occurs on every line.

Table 6-4 (Cont.)
LP10F and LP10H Test Panel Switches

Nomenclature	Item	Function
NORMAL SLOW	Toggle switch	In the NORMAL position, when TEST MODE is pressed, the printer prints at the rate specified by the DRUM SPEED switch. In the SLOW position, when TEST MODE is pressed, the printer prints at a very slow set speed to allow the hammer bank to be adjusted.
REMOTE LOCAL	Toggle switch	In the REMOTE position, it allows power to be turned on only if power is applied to the BA10. In LOCAL position, it allows power to be applied independent of the BA10.

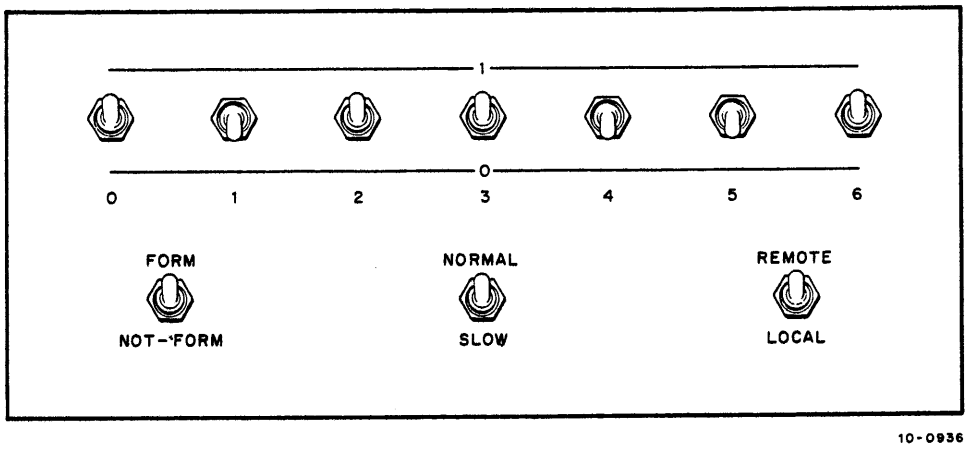


Figure 6-3 LP10F and LP10H Test Panel

Table 6-5
LP10F and LP10H Maintenance/Adjustment Controls

Nomenclature	Item	Function
PRINT INHIBIT	Switch (located on back of logic cage)	With PRINT INHIBIT switch in the UP or on position, the following actions take place: a. The print hammers are inhibited. b. The PRINT INHIBIT indicator illuminates. c. The READY indicator extinguishes. d. The ON LINE indicator extinguishes. e. The TOP PAPER BREAK switch is inhibited. f. The BOTTOM PAPER OUT switch is inhibited. g. The tape reader sprocket error detect circuit is inhibited.

Table 6-5 (Cont.)
LP10F and LP10H Maintenance/Adjustment Controls

Nomenclature	Item	Function
FORMS ALIGNMENT SCALE	Interlock	With FORMS ALIGNMENT SCALE in position and latched in the right-hand position, drum motor operation is inhibited thereby preventing damage to the form alignment scale.
RUN/ADJUST	Lever	The RUN/ADJUST lever, when in the ADJUST position, enables the following: a. Free movement of the paper feed drive tractors. b. VFU timing drive belt disengagement from the paper drive mechanism. c. Microswitch activation. **NOTE** **The activation of the microswitch ("c" above) initiates a master clear mode and causes voltage to be removed from the paper drive motor. This allows easy alignment of forms in the paper feed tractors by rotating PAPER DRIVE adjustment knob in either direction.**
VERTICAL PAPER POSITIONER	Knob	This adjustment allows minor corrections in the vertical form positioning. The control can be adjusted while printing to achieve precise alignment of printed characters with pre-printed forms.
PAPER TENSION CONTROL	Knob	This adjustment allows for proper paper tensioning in a vertical plane to obtain maximum print quality.
6/8 line per inch adjustment	Selection of two pulleys	This adjustment allows data to be printed at either 6 lines per inch or 8 lines per inch depending on the placement of the VFU timing drive belt. The belt may be placed on a large or small drive gear in the area of the paper tape reader. Placing the VFU timing drive belt on the smaller of the gears corresponds to 8 lines per inch. This can be accomplished by tilting the paper tape reader forward.
COPIES CONTROL	Lever	This adjustment positions the hammer bank the correct distance from the character drum, thereby allowing multi-copy forms to pass through the print area.
HORIZONTAL PAPER POSITIONER	Knob	This adjustment allows horizontal positioning in order to select proper margin spacing on printed forms.

6.4 LP10 I/O INSTRUCTIONS

The LP10 Line Printer Control responds to three of the four standard PDP-10 I/O instructions described in Table 6-6.

Table 6-6
PDP-10 I/O Instructions

Instruction	Function
CONO (Conditions Out)	Controls the line printer by: *a.* Setting or clearing the BUSY flag *b.* Setting or clearing the DONE flag *c.* Assigning priority interrupt levels for done and printer-error interrupts *d.* Clearing the LPT buffer.
CONI (Conditions In)	Transfers line printer status information to the processor.
DATAO (Data Out)	Sets the BUSY flag, clears the DONE flag, and loads five 7-bit characters into the control buffer register.
DATAI (Data In)	Not used by the line printer control.

6.4.1 CONO Instruction

The format of the conditions out word transferred to the line printer control logic is shown in Figure 6-4.

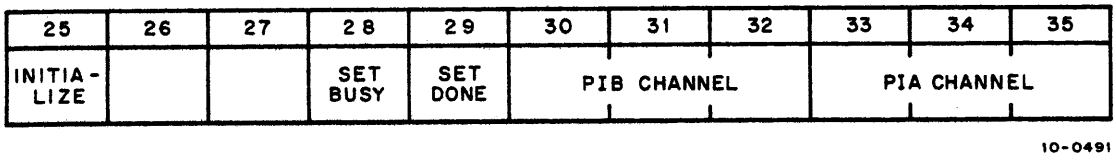


Figure 6-4 CONO Conditions Word

The CONO bits have the following significance:

Bit 25(1) Initializes the line printer system
Bit 28(1) Sets the BUSY flag
Bit 29(1) Sets the DONE flag
Bits 30-32 Set the level at which the line printer control will request an interrupt due to an error
Bits 33-35 Set the level at which the line printer control will request an interrupt due to a successful operation.

6.4.2 CONI Instruction

The format of the status word read into the central processor during a CONI is shown in Figure 6-5.

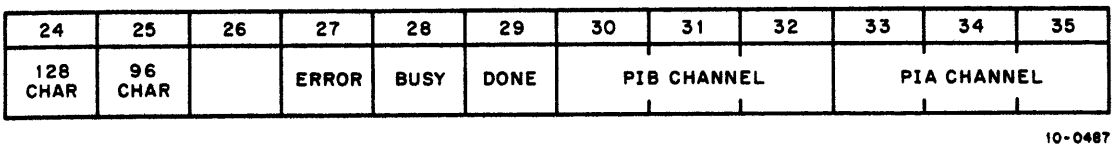


Figure 6-5 CONI Status Word

The CONI bits indicate the following:

Bit 24(1)	The line printer has a 128-character set
Bit 25(1)	The line printer has a 95-character set (or larger)
Bit 27(1)	The line printer control has detected an error in the line printer
Bit 28(1)	The BUSY flag is set
Bit 29(1)	The DONE flag is set
Bits 30-32	The priority interrupt level assignment of the line printer control for errors
Bits 33-35	The priority level assignment of the line printer control for successful operations.

6.4.3 DATAO Instruction

The format of the data word sent to the line printer control logic is shown in Figure 6-6. Table 6-7 lists all ASCII (modified) characters used in the LP10A, B, C, D, and E Line Printer System. The LP10F (64 characters) offers a selection of either a scientific or EDP character set; similarly, the LP10H (96 characters) offers both scientific and EDP character sets. These character codes are listed in Tables 6-8 through 6-11. When a lower case character code is sent to the printer control, in a system using a line printer that does not print lower case, the corresponding upper case character is printed.

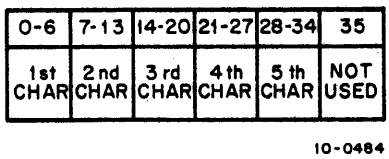
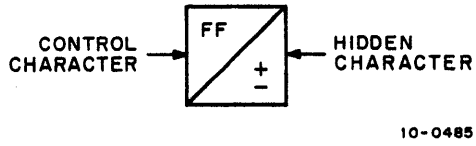


Figure 6-6 DATAO Data Word

The following rules apply when using Table 6-7:

a. To obtain the octal, decimal, or hexadecimal value of an ASCII character, add the row value and the column value. Example: *m* is 155 octal, 109 decimal, and 6D hexadecimal.

b. Hidden characters are indicated as follows:



To print hidden characters (e.g., ±) the octal code (in this case 014_8) must be preceded by 177_8.

6.5 GENERAL THEORY

The processor is interfaced with the LP10 Line Printer Control via the PDP-10 I/O Bus (see Figure 6-7). The LP10 Line Printer Control is connected to the Line Printer via a device cable. The precise manner in which the processor controls a line printer system is a function of the program in use.

A CONO instruction, addressing the line printer, loads control information into the control logic status register, conditioning the line printer system to receive input data from the processor. If the line printer is powered-up and on-line, the line printer control generates a priority interrupt on lines PI01 through 07 to the processor.

In response to the interrupt, the processor examines the line printer status with a CONI instruction. If the processor determines that the system is ready, a DATAO instruction loads five 7-bit characters into the control logic buffer register. The control logic then examines the characters, one at a time, and processes each according to its code (refer to Tables 6-7 through 6-11).

If a character is decoded as a printable character, the control logic transfers it on lines LPI DATA00 through 06 to the line printer memory for storage. If a character is decoded as a control character, the control logic generates a control pulse that forces the appropriate action within the printer. All control characters (except the horizontal tab character) cause the printer to print out the contents of its memory and then vertically space the paper (possibly a distance of zero lines) according to the specific character code. Like a printable character, the horizontal tab character causes data to be stored in the line printer memory. In this case, however, the data consists of a series of space characters, each of which causes the printer to skip one horizontal space during a memory printout.

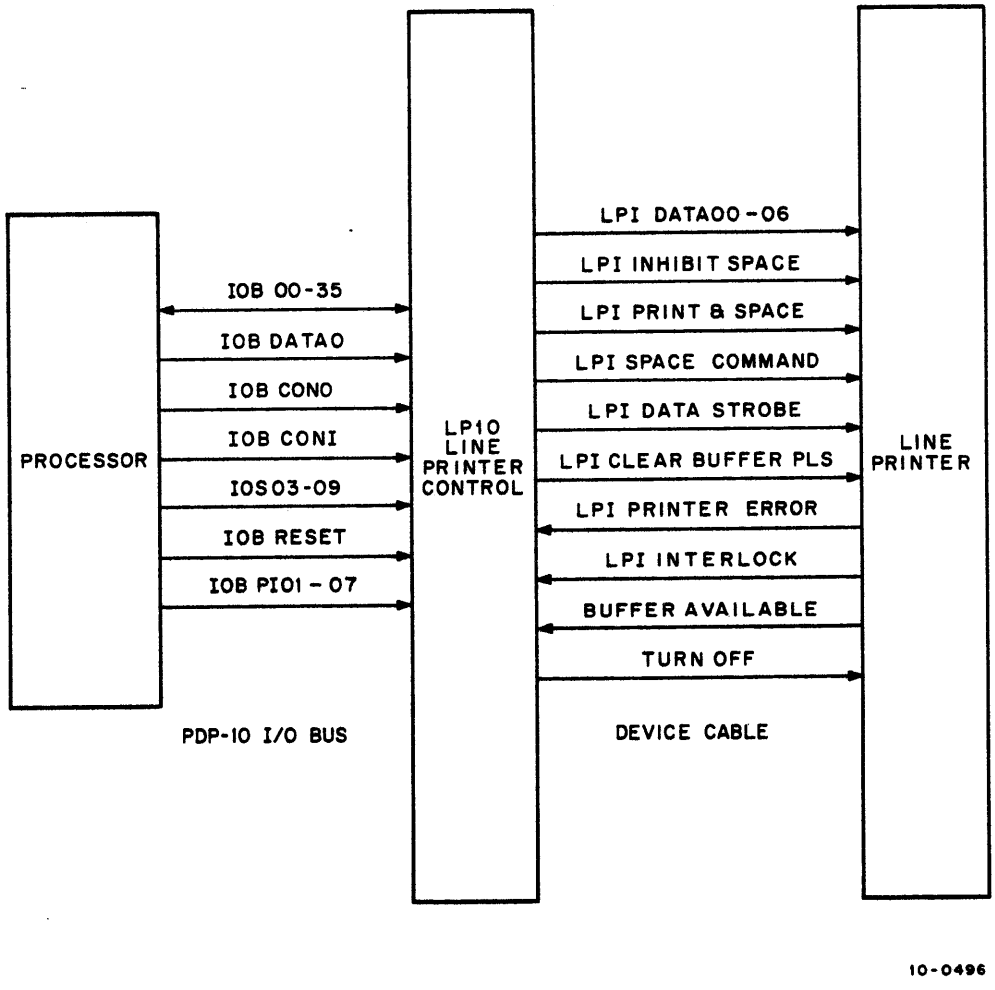


Figure 6-7 Line Printer System

As each character is processed, it is shifted out of the buffer register, and the next character is prepared for processing. A character cannot be processed until the line printer completes its response to the preceding character and enables the BUFFER AVAILABLE signal. When all five characters have been processed, the control logic generates a priority interrupt, and the processor initiates the transfer of five additional 7-bit characters.

Table 6-7
LP10A, B, C, D, and E Line Printer Modified ASCII Code

Row Value (Hexadecimal)	Row Value (Decimal)	Row Value (Octal)	Row Number	Control		Figures		Upper Case		Lower Case	
Hexadecimal →				00	10	20	30	40	50	60	70
	Decimal →			000	016	032	048	064	080	096	012
		Octal →		000	020	040	060	100	120	140	160
				0	1	2	3	4	5	6	7
0	00	00	0	NUL	DC0	Space	0	@	P	`	p
1	01	01	1	↓	DC1	!	1	A	Q	a	q
2	02	02	2	∝	DC2	"	2	B	R	b	r
3	03	03	3	β	DC3	#	3	C	S	c	s
4	04	04	4	Λ	DC4	$	4	D	T	d	t
5	05	05	5	¬	∃	%	5	E	U	e	u
6	06	06	6	∈	⊕	&	6	F	V	f	v
7	07	07	7	π	↔	'	7	G	W	g	w
8	08	10	8	λ	⌢	(	8'	H	X	h	x
9	09	11	9	HT	→	)	9	I	Y	i	y
A	10	12	10	LF	–	*	:	J	Z	j	z
B	11	13	11	VT	≠	+	;	K	[	k	{
C	12	14	12	FF	≤	,	<	L	\	l	¦
D	13	15	13	CR	≥	–	=	M	]	m	}
E	14	16	14	∞	≡	.	>	N	↑	m	~
F	15	17	15	∂	ˇ	/	?	O	←	o	DEL

Column Value

Column Number

Table 6-8 le 6-9

LP10 FE 64 Character EDP Quick entific Quick Change Drum

Line Printer Modified ASCI lified ASCII Code

Hexadecimal	Decimal	Octal		00	10		20	30	40	50	Column Value
				000	016	0	032	048	064	080	
				000	020	0	040	060	100	120	
				0	1		2	3	4	5	Column Number
0	00	00	0	NUL	DLE	S	Space	Ø	@	P	
1	01	01	1		DC1	!	!	1	A	Q	
2	02	02	2		DC2	"	"	2	B	R	
3	03	03	3		DC3	#	#	3	C	S	
4	04	04	4		DC4	$	$	4	D	T	
5	05	05	5			%	%	5	E	U	
6	06	06	6			&	&	6	F	V	
7	07	07	7			'	'	7	G	W	
8	08	10	8			(	(	8	H	X	
9	09	11	9	HT		)	)	9	I	Y	
A	10	12	10	LF		*	*	:	J	Z	
B	11	13	11	VT		+	+	;	K	[	
C	12	14	12	FF		,	,	<	L	\	
D	13	15	13	CR		-	-	=	M	]	
E	14	16	14			.	.	>	N	^	
F	15	17	15			/	/	?	O	—	

Row Value | Row Number | Control | Figures | Upper Case

Table 6-11

LP10 HF 96 Character Scientific Quick Change Drum

Line Printer Modified ASCII Code

Row Value	Row Number	Octal	Decimal	Hexadecimal	Control	Figures	Upper Case	Lower Case
					00	10	20	30	40	50	60	70
					000	016	032	048	064	080	096	012
					000	020	040	060	100	120	140	160
					0	1	2	3	4	5	6	7
0	0	00	00	0	NUL	DLE	Space	Ø	@	P	`	p
1	1	01	01	1		DC1	!	1	A	Q	a	q
2	2	02	02	2		DC2	”	2	B	R	b	r
3	3	03	03	3		DC3	#	3	C	S	c	s
4	4	04	04	4		DC4	$	4	D	T	d	t
5	5	05	05	5			%	5	E	U	e	u
6	6	06	06	6			&	6	F	V	f	v
7	7	07	07	7			′	7	G	W	g	w
8	8	08	10	8			(	8	H	X	h	x
9	9	09	11	9	HT		)	9	I	Y	i	y
A	10	10	12	10	LF		*	:	J	Z	j	z
B	11	11	13	11	VT		+	;	K	[	k	{
C	12	12	14	12	FF		,	<	L	\	l	|
D	13	13	15	13	CR		–	=	M	]	m	}
E	14	14	16	14			.	>	N	^	n	~
F	15	15	17	15			/	?	O	—	o	DEL

Column Value

Column Number

6.6 INTERFACE CABLE SIGNALS

Table 6-12 lists the functions of the I/O bus cable. Table 6-13 lists the functions of the LP10 Device Cable.

Table 6-12
I/O Bus Cable (Partial Listing)

Signal Line	Function
IOB00-35	Transfer status information to the processor during a CONI instruction; transfer control information to the LP10 Line Printer Control during a CONO instruction; transfer data to the LP10 Line Printer Control during a DATAO instruction.
IOB CONO CLEAR	Transmitted to the LP10 Line Printer Control for initialization.
IOB CONO SET	Sets up the LP10 Line Printer Control for operation 1 μs after IOB CONO CLEAR.
IOB DATAO	Transfers five 7-bit characters to the LP10 Line Printer Control.
IOB CONI	Gates LP10 Line Printer Control status information onto the I/O bus.
IOS03-09	Transfer the device select code to the LP10 Line Printer Control.
IOB PI01-07	Transfer the program interrupt signal to the processor.

Table 6-13
Line Printer Device Cable

Signal Line	Function
LPI DATA00-06	Transmit printable characters to the line printer; select the vertical format unit (VFU) channel when spacing paper.
LPI INHIBIT SPACE	Inhibits vertical movement of paper during a print and space command.
LPI PRINT & SPACE	Causes the contents of the line printer memory to be printed and then spaces the paper. If LPI INHIBIT space is true, the contents of memory are printed; however, the paper is not advanced and the next line of characters will be printed over the line printed unless a paper spacing character appears before the next printable character (e.g., a carriage return is simulated).
LPI SPACE COMMAND	Causes the paper to be advanced according to the VFU channel selected by the information on the DATA00-06 lines.
LPI DATA STROBE	Strobes the data on the DATA00-06 lines into the line printer memory.
LPI CLEAR BUFFER PLS	Clears the line printer memory without printing by performing a dummy print cycle.
LINE PRINTER ERROR	Informs the LP10 Line Printer Control that the line printer has detected an error (such as a blown fuse, etc.) that will affect its operation.
LPI INTERLOCK	Informs the LP10 Line Printer Control that the device cable is connected.
BUFFER AVAILABLE	Informs the LP10 Line Printer Control that the line printer is ready to receive data.
TURN OFF	Removes power from the line printer when the line printer is in the remote turn-on mode and power is removed from the BA10.

6.7 DETAILED THEORY (Refer to BA10 Maintenance Manual, Volume II)

A detailed theory of operation for the line printer system is presented in the following paragraphs.

6.7.1 Initialization

During a CONO, the program places control information and the line printer device code on the I/O bus and sends the IOB CONO CLEAR and IOB CONO SET pulses. These CONO pulses, in conjunction with the device

number, are converted to IOC LP CONO CLEAR and IOC LP CONO SET, respectively. IOC LP CONO CLEAR clears the LPST ERROR ENAB, LPST BUSY, LPST DONE, LPST PIB30-32, and LPST PIA33-35 flip-flops; IOC LP CONO SET, which occurs 1 μs later, loads the control information into the status register. The contents of the PIA and PIB flip-flops of the register define the channel over which interrupts are sent to the processor at the successful completion of certain data transfers or detection of line printer errors, respectively.

With IOB25(1), an LPCN SHT CNT INITIALIZE pulse is generated. This pulse forces the shift counter LPBF SHT CNT 0-2, to 4_8. LPCN SHT CNT INITIALIZE also clears LPCN ALT, CLR SYNC, SHIFT SYNC A, SHIFT SYNC B, DATAO SYNC, and CONO PRINT flip-flops. The LPCN CLEAR pulse is generated 1 μs after LPCN SHT CNT INITIALIZE. LPCN CLEAR sets the LPST BUSY flip-flop, clears the LPST DONE flip-flop, sets the control register LPCN CLR SYNC flip-flop, and clears the column counter LPCC 0-7. LPCN SHT CNT INITIALIZE generates the LPCN CLR PRINTER BUF pulse, which is sent to the line printer as LPI CLEAR BUFFER PLS to clear the line printer memory.

When the line printer has cleared its memory, it sends the BUFFER AVAILABLE level to the control to generate LPI BUFFER AVAILABLE. The combination of LPI BUFFER AVAILABLE and LPCN CLR SYNC(1) generates an LPCN DONE pulse, thus clearing the control register LPCN CLR SYNC flip flop. LPCN DONE also clears LPST BUSY flip-flop and sets the LPST DONE flip-flop. Setting the LPST DONE flip-flop generates an interrupt to the processor, signaling the completion of the initialization operation. When these conditions are established, the control logic waits for further input from the processor.

6.7.2 Character Handling

Following initialization, a DATAO instruction places five 7-bit characters on the I/O bus. IOC LP DATAO CLEAR clears the LPCN DATAO SYNC flip-flops, sets the LPST BUSY flip-flop, and clears the LPST DONE flip-flop. In addition, LPBF DATAO CLR A and B pulses are generated to clear the shift counter and buffer register.

IOC LP DATAO SET generates the LPBF DATAO A and B pulses. These pulses load the 7-bit characters on the I/O bus into the buffer register and set the LPCN SHIFT SYNC A and B flip-flops. The IOC LP DATAO SET pulse is delayed 2.2 μs to generate the IOC LP DATAO SET DELAY signal, which sets the LPCN DATAO SYNC flip-flop. With the LPCN DATAO SYNC and LPCN SHIFT SYNC A and B flip-flops set, and the LPI BUFFER AVAILABLE level at -3 Vdc, a synchronizer pulse (LPCN GO) is generated. Control logic operation from this point is controlled by the 7-bit character in flip-flops LPBF00 through 06 of the buffer register. This character is decoded by the logic shown on print LPDA (refer to Volume II).

The decoding function is detailed in subsequent paragraphs. In essence, the decoder defines the character as one of four types: printing character, vertical control character, horizontal control character, or illegal character.

6.7.3 Printing Character

If the seven bits in buffer flip-flops LPB00 through 06 are decoded as a printing character, the LPCN GO pulse is converted to the LPCN DATA STROBE pulse. LPCN DATA STROBE becomes the 2.5-μs LPI DATA STROBE pulse, which transfers the contents of the first seven buffer register flip-flops to the line printer, provided LPDA NORMAL CODE (which is enabled by the decoder for a printable character) is true. During the transfer, the line printer disables the BUFFER AVAILABLE level, preventing the generation of further LPCN GO pulses. The BUFFER AVAILABLE level becomes true after the cycle time of the line printer memory. The LPCN DATA STROBE pulse also generates an LPCN CC ADD ONE pulse, which steps the column counter LPCC00 through 07. The column counter keeps track of the number of characters transferred to the line printer memory.

The same LPCN GO pulse that initiated the data strobe operation clears the LPCN SHIFT SYNC A and B

flip-flops. In addition, LPCN GO is delayed 4 μs and becomes the LPCN CYCLE pulse. LPCN CYCLE generates the LPCN SHIFT pulse.

The LPCN SHIFT pulse generates the LPBF SHIFT A and B pulses. These pulses step the shift counter to 001, and shift the contents of the buffer register. The shift is such that the contents of LPBF00 through 06 are lost; the contents of LPBF07 through 13 move into LPBF00 through 06; the contents of LPBF14 through 20 move into LPBF07 through 13, etc. Although the contents of LPBF28 through 34 shift into LPBF21 through 27, no new data is shifted into LPBF28 through 34; consequently, the contents of flip-flops LPB28 through 34 remain unchanged. In addition to initiating the shift operation, LPCN SHIFT sets the control register LPCN SHIFT SYNC B flip-flop. LPCN SHIFT also generates LPCN SHIFT DLY, which sets the LPCN SHIFT SYNC A flip-flop. When the LPCN SHIFT SYNC A and B flip-flops have been set and the line printer again transmits the BUFFER AVAILABLE level, another LPCN GO pulse is generated. Assume that the buffer register has been filled with printable characters; then, the next LPCN GO pulse initiates the same operations as the first LPCN GO pulse. This essentially means that the character in buffer flip-flops LPBF00 through 06 is strobed into the line printer, the column and shift counters are incremented, and the contents of the buffer register are shifted. This same cycle occurs twice more, transferring four of the five printable characters into the line printer, and stepping the shift counter to 4_8.

When the fifth LPCN GO pulse is generated, it causes the fifth character to be strobed into the line printer. The fifth LPCN GO pulse also produces another LPCN CYCLE pulse. The count 4_8 in the shift counter, however, prevents the generation of another LPCN SHIFT pulse; instead, the count 4_8 generates an LPCN DONE pulse. LPCN DONE clears the LPST BUSY flip-flop and sets the LPST DONE flip-flop. Setting the LPST DONE flip-flop generates a priority interrupt request to processor. The program then samples the status of the PST DONE flip-flop by issuing a CONI instruction.

6.7.4 Vertical Control Characters

Up to and including the generation of LPCN GO, vertical control characters cause essentially the same control logic operations as printable characters. A major difference is that vertical characters produce the LPDA SPACE ONLY or LPDA PRINT AND SPACE commands. For the space only and print and space operation, the contents of the buffer register are shifted similar to a printing character transfer. The BUFFER AVAILABLE level from the printer indicates the readiness of the printer to handle additional characters.

6.7.4.1 **Space Only** – When an LPDA SPACE ONLY command is decoded, the LPCN GO pulse generates the LPCN SPACE COMMAND, which generates the 2.5-μs pulse LPI SPACE COMMAND sent to the line printer. On receiving the LPI SPACE COMMAND pulse, the printer vertically spaces the paper according to the three least-significant bits of the control character. These bits are sent to the line printer via lines LPI DATA04 through 06. The significance of the various codes is discussed in detail in Paragraph 6.7.9.

6.7.4.2 **Print and Space** – Operations initiated by a print and space character are nearly identical to those produced by a space only character. The major difference is that the LPCN GO pulse generates the LPCN PRINT AND SPACE pulse. LPCN PRINT AND SPACE generates the 2.5-μs LPI PRINT AND SPACE B signal that is sent to the line printer. In response to LPI PRINT AND SPACE B, the line printer prints out the contents of its memory When the printout is complete, the printer vertically spaces the paper, in the manner described in Paragraph 6.7.4.1. The LPCN PRINT AND SPACE pulse also generates the LPCN CLR CC pulse to clear the column counter.

6.7.5 Horizontal Control Character

The horizontal tab operation is similar to the printable character operation in that LPI DATA STROBE B is generated to strobe the 7-bit character into the printer. In this case, the 7-bit code is a space character.

When the horizontal tab operation occurs, the space character is repeatedly sent to the printer until the column counter reaches a multiple of 8_{10}. When the column counter equals 7_8, the LPCC TAB STOP level is true. This generates the LPDA DO H TAB level. During a horizontal tab cycle, the LPDA TAB CYCLE level is generated, provided LPCC05 through 07 does not contain 7_8. When the LPDA TAB CYCLE level is true, it prevents the LPCN GO pulse from initiating the LPCN CYCLE pulse and the ensuing shift cycle. LPCN GO produces the LPCN DATA STROBE pulse that eventually strobes bits LPI DATA00 through 06 into the printer.

The decoder does not generate LPDA NORMAL during a horizontal tab operation, thereby disabling gates LPI DATA00 and LPI DATA02 through 06. LPDA DO H TAB generates LPI DATA01, resulting in code 040_8, which is the space character. During a printing cycle, the space character inhibits activation of the corresponding hammer. When the printer has accepted the space character, it re-enables the BUFFER AVAILABLE level.

In the absence of a shift cycle, the shift counter is not stepped and the buffer register data is not shifted; therefore, the horizontal tab code remains in the final stage (LPBF00 through 06) of the buffer register until the tab stop is reached. Each time the printer re-enables BUFFER AVAILABLE after reading in a horizontal space character, the cycle is repeated. With the generation of each data strobe pulse, the horizontal space character is read into the printer and the character counter is stepped. This procedure is repeated until the data strobe pulse increments LPCC05 through 07 to 7_8 and transfers the last horizontal space character to the line printer. The count of 7_8 in LPCC05 through 07 generates the LPCC TAB STOP level. When the LPCC TAB STOP level goes true, the LPDA TAB CYCLE level goes false, enabling a shift cycle. This time, as the horizontal space character is transferred to the printer, LPCC05 through 07 is stepped to 000 and the contents of the buffer register are shifted. The next cycle processes the character following the horizontal tab character.

6.7.6 Illegal Character

When the character contained in line printer buffer LPBF00 through 06 is not decoded as a printing, vertical-control, or horizontal character, it is treated as an illegal character. In this case, the LPCN GO pulse does not produce any of the control pulses that normally initiate line printer action; instead, LPCN GO initiates an LPCN CYCLE pulse and the ensuing shift cycle. As a result, the character is simply shifted out of the buffer register and lost, and the line printer is not affected.

6.7.7 Printing-Character Overflow

Transferring 132 consecutive printing characters to the printer fills the memory to capacity. If character 133 initiates a printing operation, the memory is emptied and the printer is ready to receive additional printing characters; however, if character 133 is a printing character, the control logic must force a printing operation. The operation is such that printing character 133 is not lost; instead, character 133 becomes the first character sent to the line printer for the next print cycle and appears at the left margin of the next line.

The control cycle that transfers the consecutive printing character 132 to the printer, steps the column counter to 133_{10}. From this count, the decoder generates the LPCC LINE OVER ERROR level. When character 133 is a printing character, the control logic initiates another data strobe cycle. As for every cycle of this type, LPCN GO is converted to the LPCN DATA STROBE pulse, which, in turn, produces the 2.2-μs LPI DATA STROBE level that initiates the strobing of the character into the line printer. The line printer, however, does not accept the character because its memory is full.

When the LPCC LINE OVER ERROR level is true, the trailing edge of LPI DATA STROBE performs three operations:

1. It sets the LPCN CONO PRINT flip-flop, inhibiting the generation of an LPCN CYCLE pulse and the resultant LPCN SHIFT pulse. (As a result, the shift counter is not incremented, and the content of the buffer register is not shifted.)

2. LPI DATA STROBE clears the LPCN SHIFT SYNC A and B flip-flops, inhibiting the start of further transfers. (This is a precaution to ensure that these flip-flops are cleared in case the character being decoded is a horizontal tab character.)
3. LPI DATA STROBE triggers a 4-μs delay.

At the end of the 4-μs delay, the logic generates LPCN CONO PRINT PLS and LPCN CONO PRINT DLY pulses. (CONO PRINT is not related in any way to a CONO instruction.)

The LPCN CONO PRINT PLS sets the LPCN SHIFT SYNC B flip-flop in preparation for another character transfer. LPCN CONO PRINT PLS also generates the LPCN PRINT AND SPACE pulse that causes the printer to print the contents of its memory and space the paper according to the code on output lines LPI DATA00 through 06. LPCN CONO PRINT(1) forces lines LPI DATA04 and 05 to a 1, producing a single-space paper advance when the standard vertical format tape is used. As usual, the LPCN PRINT AND SPACE pulse also produces the LPCN CLEAR CC pulse, which clears the column counter in preparation for subsequent character transfers.

Approximately 4 μs after the LPCN PRINT AND SPACE pulse, the LPCN OVERFL DATA DLY level becomes positive. The positive transition clears the LPCN CONO PRINT flip-flop and sets the LPCN SHIFT SYNC A flip-flop. When the printer completes the printout and generates a BUFFER AVAILABLE level, the control logic begins another transfer cycle. Since LPBF00 through 06 still contains the printing character that initiated the printout, that character is now transferred to the printer.

6.7.8 Printer Types

Tables 6-7 through 6-11 show the ASCII code modified for use in the DECsystem-10. Codes 011_8 through 015_8 and 020_8 through 024_8 define control characters unless they are preceded by code 177_8; however, the character printed varies with the type of line printer used. Printers with 64- and 95-character sets define codes 040_8 through 177_8 as printing characters; however, when the 64-character printer receives codes 140_8 through 176_8 it converts them to print characters represented by octal codes 100_8 through 136_8, respectively. All 128-character printers recognize codes 000_8 through 177_8 as printing characters; however, to print the character hidden under the ten control characters and the delete character, the code must be preceded by a delete character.

Jumper wires on the W990 Module at location A03 adapt the control logic for use with the various printers. No jumpers are required for 64-character printers. For 96-character printers that do not print a symbol for the delete code (177_8), a jumper is inserted between terminals C and D of the W990 Module, location A03, enabling the LPDA 96 CHAR level. Essentially, these are 95-character printers. For full 96-character machines (i.e., printers that print a symbol for the delete code) terminal C is jumpered to D and terminal H is jumpered to J. Jumper J enables LPDA FULL 96 CHAR. For 128-character printers, jumpers are inserted between C and D, E and F, and H and J. The jumper between H and J enables LPDA 128 CHAR. These levels are used throughout the character decoding logic to enable functions relevant to different printer types.

6.7.9 Character Decoder

The line printer character decoder is described in the following paragraphs.

6.7.9.1 LPDA – The LPDA PRINTING CHAR level enables the LPI DATA STROBE B level that gates printable characters to the line printer. The LPDA PRINTING CHAR level is always generated by the codes 040_8 through 176_8 (printing characters) and is enabled by the DO H TAB level to transfer a series of space characters to the line printer during a horizontal tab operation.

Two other groups of gates also enable LPDA PRINTING CHAR. The first group prints a character for the delete code on full 96-character line printers. This operation requires that the processor send two delete codes. The first delete code sets the LPCN ALT flip-flop; the second is transferred to the line printer as a printable character.

The second group, used with 128-character printers, enables the use of control character codes and the codes for null (000_8) and delete (177_8) as printing characters. Critical to this operation is the use of the LPDA CONTROL level, which is enabled when a control character, delete, or null is decoded. The LPDA CONTROL signal, in conjunction with the LPCN ALT flip-flop, generates an LPDA PRINTING CHAR level for delete, null, and the control characters. The LPCN ALT flip-flop is set by preceding the code to be printed with a delete character. The false condition of the LPDA CONTROL generates an LPDA PRINTING CHAR level.

6.7.9.2 **LPDA PRINT AND SPACE** – The LPDA PRINT AND SPACE level is generated when a print operation is required; when LPCC = 0 is false; and when LPDA FORM ADVANCE is true. LPPCC = 0 is false when a printable character is sent to the printer after the last LPDA PRINT AND SPACE level is generated. The LPDA FORM ADVANCE level is generated for all vertical control codes except LPDA CAR RET, providing the LPCN ALT flip-flop is not set. If the LPCN ALT flip-flop is set, it initiates a conversion from a control to a printable character function for a 128-character printer.

The LPDA PRINT AND SPACE command is converted to the LPI PRINT AND SPACE B pulse that directs the printer to print the contents of its memory. When the printout is complete, the printer vertically spaces the paper, according to the configuration of bits LPI DATA04 through 06.

The LPDA PRINT AND SPACE level is also enabled for a carriage return operation. When the LPDA CAR RET character is decoded and the LPCN ALT flip-flop is not set, the LPI INHIBIT SPACE B level is generated. This level is sent to the printer to inhibit a spacing operation. At the same time, LPI INHIBIT SPACE B causes the generation of the LPDA PRINT AND SPACE level. This level is also sent to the printer as the LPI PRINT AND SPACE B pulse. In response to LPI INHIBIT SPACE B and LPI PRINT AND SPACE B the printer prints a line, but does not vertically space the paper; consequently, the next print command can cause an overprint.

6.7.9.3 **LPDA SPACE ONLY** – The LPDA FORM ADVANCE level is ANDed with the LPCC = 0 level to generate LPDA SPACE ONLY. LPDA SPACE ONLY is consequently produced by any vertical control code, provided the LPCN ALT flip-flop is not set and no printable characters have been sent to the printer.

As during a print and space operation, paper spacing is accomplished as a function of the data on lines LPI DATA04 through 06.

6.7.9.4 **LPDA CASE SHIFT** – When a lower-case character is decoded (codes 140_8 through 176_8) and the printer is equipped with only 64 characters, the LPDA CASE SHIFT signal is true. This signal prevents the enabling of the LPI DATA 01 line to the printer; consequently, the printer reads a code between 100_8 and 136_8 and prints the uppercase equivalent of the lower case character. The LPI DATA00 line is ignored by 64-character printers.

6.7.9.5 **LPDA NORMAL CODE** – The LPDA NORMAL CODE level gates the contents of buffer register flip-flops LPBF00 through 06 to the line printer. LPDA NORMAL CODE is true when a printing character or vertical control character codes 020_8 through 027_8 are decoded and a CONO PRINT or horizontal tab operation (LPDA DO H TAB) is not performed. These restrictions are imposed because CONO PRINT and horizontal tab operations require specific codes to be sent to the line printer.

If the false condition of the LPDA DO H TAB level were not included, LPDA NORMAL CODE would be enabled during a horizontal tab operation; therefore, the line printer would see the entire horizontal tab character rather than a 1 only on bit LPI DATA01. The LPCN CONO PRINT(0) level is included in the gating structure for essentially the same reason. In this case, of course, the printer is forced to see 1s on bits LPI DATA04 and 05.

6.8 CONTROL CHARACTERS

The control characters used in the line printer system are described in the following paragraphs. Valid printable character codes are also described.

a. *Horizontal Tab (ASCII 011_8)* – A horizontal tab of eight columns is simulated by feeding the necessary spaces to the line printer. The character following the horizontal tab character is printed in the column corresponding to the tab stop (i.e., columns 9, 17, 25, etc.). At least one space always exists between the characters before and after the horizontal tab.

b. *Carriage Return (ASCII 015_8)* – A teleprinter-type carriage return is simulated, (i.e., the contents of the line printer memory are printed, but paper spacing is inhibited). The next print cycle overprints the line printed by the carriage return, unless a paper-spacing character appears before the next printable character. A printing character that appears immediately after a carriage return is printed in column 1.

c. *Line Feed (ASCII 012_8)* – A teleprinter-style carriage return is simulated followed by a teleprinter-style line feed. The line printer memory is printed, then the paper is spaced until a hole is seen in channel 8 of the vertical format tape, ordinarily one vertical space. The next character is printed in column 1.

d. *Vertical Tab (ASCII 013_8)* – A teleprinter-style carriage return is simulated followed by a vertical tab. The line printer memory is printed and the paper is spaced until a hole is sensed in channel 7 of the vertical format tape, ordinarily 20 vertical spaces. The next character is printed in column 1.

e. *Form Feed (ASCII 014_8)* – A teleprinter-style carriage return and form feed is simulated. The line printer memory is printed and the paper is spaced until a hole is sensed in channel 1 of the vertical format tape, ordinarily at the top of the page. The next character is printed in column 1.

f. *DC_0 through DC_4 (ASCII 020_8 through 024_8)* – A teleprinter-style carriage return is simulated followed by vertical paper motion. The line printer memory is printed and the paper is spaced until a hole is sensed in the channel of the vertical format tape, which is determined by the command.

The printable characters employed by a line printer system depend on the printer drum. Printable character codes 040_8 through 137_8 are used for 64-character printers; 040_8 through 176_8 for 96-character printers. If a lower case character (140_8 through 176_8) is sent to a 64-character printer, the corresponding upper case character (100_8 through 136_8) is printed as noted in Paragraph 6.9.

For 128-character printers, printing characters are hidden under control codes HT (011_8), CR (015_8), LF (012_8), VT (013_9), NULL (000_8), FF (014_8), DC_0 through DC_4 (020_8 to 024_8), and DELETE (177_8). The hidden characters are printed by prefixing each character with the delete character. Thus, DELETE, LF loads the printer buffer with the character hidden under LF.

On special "full 96-character" printers a character is hidden under the delete character. This character is printed by sending the string "delete delete" to the printer. The first delete indicates that a hidden character follows, and the second delete is stored in the printer memory to be printed.

6.9 VERTICAL FORMAT TAPE

Eight of the characters sent to the line printer direct the printer to vertically space the paper. On detecting one of these characters, the printer performs the required spacing via one of eight columns on the vertical-format tape, each column corresponding to one of the vertical control characters. The printer vertically spaces the paper until it encounters a hole in the tape column specified by the character being executed. Any vertical format tape may be used, but the tape format shown in Table 6-14 is supplied as a general-purpose tape for 11-in. fan-fold paper.

Table 6-14
Vertical Spacing Characters

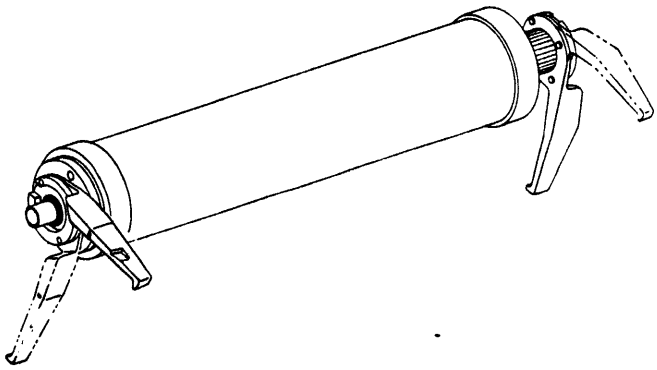
Control Character (ASCII)	Printer Code Specification	Tape Column	Number of Vertical Spaces
Line Feed (012_8)	$XX6_8$	8	1
Vertical Tab (013_8)	$XX5_8$	7	20
Form Feed (014_8)	$XX7_8$	1	*Top-of-form
DC_0 (020_8)	$XX0_8$	2	30
DC_1 (021_8)	$XX1_8$	3	2
DC_2 (022_8)	$XX2_8$	4	3
DC_3 (023_8)	$XX3_8$	5	1 punched every space
DC_4 (024_8)	$XX4_8$	6	10

*This channel is the only one used by the TOP-OF-FORM button.

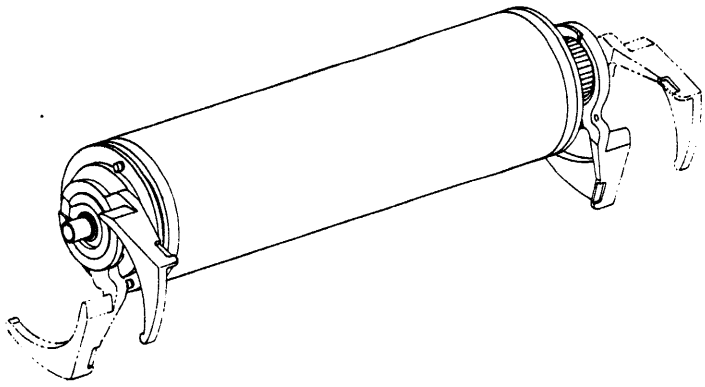
Six blank lines are left on the control tape before the top-of-form position except in the DC_3 case. In column 5 of the vertical format control tape, holes are punched continuously to allow printing across the fold, thereby facilitating photo-reproduction. Usual operation allows 60 printing lines per form, with 66 printing lines in the case of DC_3 spacing.

6.10 LP10F and LP10H CHARACTER DRUMS

The LP10F and LP10H line printers offer a quick-change character drum assembly option. This feature allows the easy interchanging of the 64-character scientific with the 64-character EDP drums and the 96-character scientific with the 96-character EDP drums. Refer to the Data Products Model 2470 technical manual for complete information on the quick-change drums. Figure 6-8 illustrates the 64- and 96-character drum assemblies.



64 CHARACTER QUICK-CHANGE DRUM



96 CHARACTER QUICK-CHANGE DRUM

Figure 6-8 LP10F, H Character Drum Assemblies

CHAPTER 7
XY10 PLOTTER SYSTEM

This chapter describes programming, theory of operation, and operating information relevant to the XY10 Plotter System.

7.1 FUNCTIONAL DESCRIPTION

The XY10 Plotter Control interfaces the processor with a CalComp Digital Incremental Plotter, Model 502, 518, 563, or 565, or to a similar incremental X-Y plotter, which uses the same type of data and control information (see Figure 7-1). The associated plotter allows data to be graphically displayed on paper.

Figure 7-1 XY10 Plotter System – Functional Block Diagram

All plotter operations, except setting the coordinates at which the plotting operation begins, are controlled by the plotter control logic and the processor. The program in the processor addresses the plotter with a CONI instruction to fetch status information from the plotter. This information is transferred to the processor, via the I/O bus, to indicate when the plotter is ready to accept data from the processor. When the status information indicates that the plotter is ready to accept data, the program performs a CONO instruction to assign a priority interrupt channel. A DATAO instruction is then performed to specify one or more of the following functions: raise or lower the plotter pen; move the pen carriage to the left or right; move the paper drum up or down. These functions are accomplished by setting associated flip-flops in the plotter control logic.

7.2 INDICATORS AND CONTROLS

Table 7-1 lists the BA10 Indicators associated with the XY10 Plotter System. The TD10 Indicator Panel displays the contents and status of the plotter control, when the plotter control is mounted in the TD10.

Several models of plotter indicator/control panels can be used with the XY10 Control Logic. Refer to the appropriate plotter instruction manual for control and indicator operation.

Table 7-1
BA10 Indicator Panel - Plotter Section

Nomenclature	Function
PEN UP	Indicates the plotter control has received a command to lift the pen off the paper.
PEN DOWN	Indicates the plotter control has received a command to lower the pen to the paper.
-X, +X, +Y, -Y	Indicates the direction of plotter movement.
PWR ON	Indicates power is applied to the plotter (not present on all plotter models).
BUSY	Indicates the plotter control is performing an operation.
DONE	Indicates the plotter control has completed an operation.
PL PI33-35	Indicate the priority interrupt levels at which the plotter control will interrupt the processor on detection of the DONE flag.

7.3 OPERATING NOTES

To prepare the plotter for operation, proceed as follows:

Step	Procedure
1	Turn on plotter power.
2	Install paper.
3	Position pen to the desired starting point.

7.4 XY10 I/O INSTRUCTIONS

The XY10 Plotters respond to three of the four basic I/O instructions described in Table 7-2.

Table 7-2
I/O Instructions

Instruction	Function
CONO (Conditions Out)	Transfers control conditions from the processor to the plotter control logic to perform one or both of the following: *a.* Load the priority interrupt channel number into the priority interrupt register *b.* Clear or set the BUSY or DONE flip-flops.
CONI (Conditions In)	Reads the plotter status register.
DATAO (Data Out)	Transfers data from the processor into the plotter control data buffer.
DATAI (Data In)	Not used by the plotter control.

7.4.1 CONO Instruction

The configuration of the control word that is transferred to the plotter control logic during a CONO instruction is shown in Figure 7-2.

The CONO bits have the following significance:

Bit 31(1)	Sets the PLST PLOT BUSY flip-flop
Bit 32(1)	Sets the PLST PLOT DONE flip-flop, thereby clearing the PLST PLOT BUSY flip-flop
Bits 33-35	Load the priority interrupt assignment register.

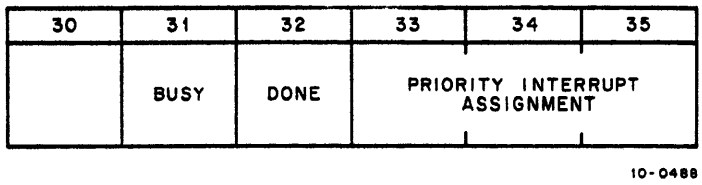


Figure 7-2 CONO Conditions Word

7.4.2 CONI Instruction

The configuration of the status word that is read by a CONI is shown in Figure 7-3.

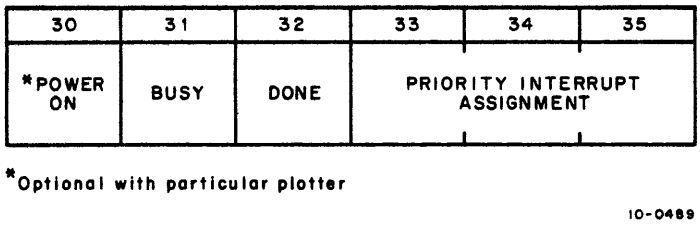


Figure 7-3 CONI Status Word

The CONI bits have the following significance:

Bit 30(1)	Indicates power is applied to the plotter
Bit 31(1)	Indicates the plotter is presently performing a command
Bit 32(1)	Indicates the plotter has finished the last command and will accept another; the DONE flag causes a priority interrupt request; it is cleared by either a CONO or DATAO instruction
Bits 33-35	Contain the present setting of the priority interrupt channel register.

7.4.3 DATAO Instruction

The configuration of the data word that is sent to the plotter control logic from the processor during a DATAO is shown in Figure 7-4.

The DATAO bits indicate the following:

Bit 30(1)	The pen is raised from the paper
Bit 31(1)	The pen is lowered to the paper
Bit 32(1)	The plot is moved in the -X direction
Bit 33(1)	The plot is moved in the +X direction
Bit 34(1)	The plot is moved in the +Y direction
Bit 35(1)	The plot is moved in the -Y direction.

NOTE

If conflicting directions are called for, the plotter motion cannot be determined (being a function of the plotter model).

In addition, the DATAO instruction clears the PLST PLOT DONE flip-flop and sets the PLST PLOT BUSY flip-flop. After the plotter has finished the specified operation, PLST PLOT BUSY is cleared and the PLST PLOT DONE flip-flop is set, causing a priority interrupt request.

30	31	32	33	34	35
RAISE PEN (UP)	LOWER PEN (DOWN)	PLOT -X	PLOT +X	PLOT +Y	PLOT -Y

10-0486

Figure 7-4 DATAO Data Word

7.5 GENERAL THEORY

The XY10 Plotter Control provides the control logic and interface for operating a plotter with the PDP-10 Processor. A series of functions controlled by I/O instructions initialize the plotter control logic, generate priority interrupt requests to indicate a change in status, and initiate a plotting operation. See Figure 7-5 for the functional descriptions.

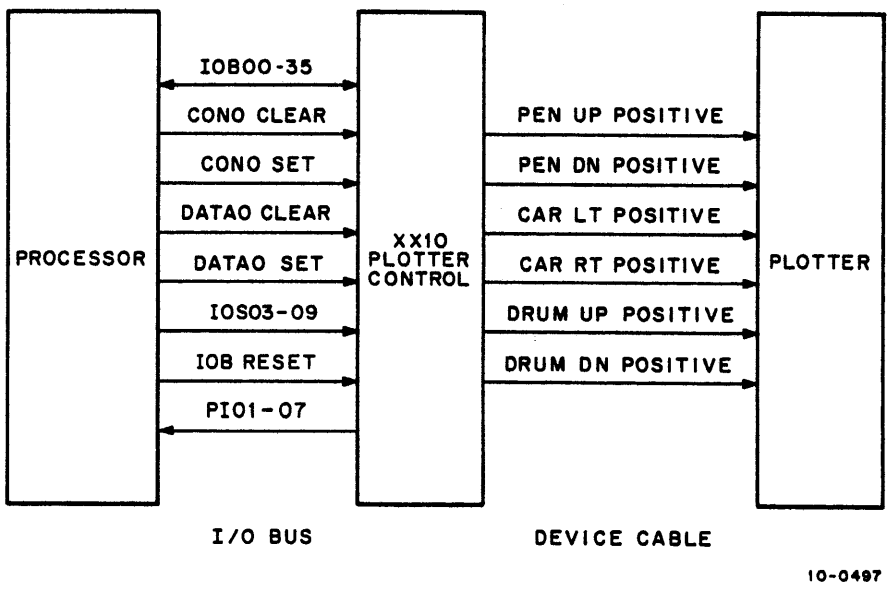


Figure 7-5 XY10 Plotter System

When power is first applied to the XY10 Plotter Control, the BUSY and DONE flags and the priority interrupt register in the plotter control logic are cleared. A CONO instruction is performed to clear the BUSY and DONE flags and to set up the priority interrupt level assignment for the plotter. Next, a DATAO instruction is sent to the plotter control logic to perform the operation defined by the DATAO word. A CONI instruction is then executed to determine if the plotter has completed the operation and is ready for another operation.

7.6 INTERFACE CABLE SIGNALS

Table 7-3 lists functions of the I/O bus cable; Table 7-4 lists functions of the XY10 Device Cable.

Table 7-3
I/O Bus Interface Cable
(Partial Listing)

Signal Line	Function
IOB00-IOB35	Transfer status information into the processor and control signals into the plotter control logic; in the XY10, only IOB30 through IOB35 are used.
IOB CONO CLEAR	Clears the BUSY and DONE flags and the priority interrupt register.
IOB CONO SET	Gates the priority interrupt channel number into the priority interrupt register and sets the DONE/BUSY flags 1 μs after IOB CONO CLEAR.
IOB CONI	Gates plotter status information to the processor.
IOB DATAO CLEAR	Clears the DONE flag, sets the BUSY flag, and triggers internal delays.
IOB DATAO SET	Gates operational data into the plotter control register 1 μs after IOB DATAO CLEAR.
IOS03(1)-IOS09(0)	Identify the device number to the plotter control logic.
IOB RESET	Clears the plotter control logic.
IOB PI01-PI07	Transfer the program interrupt signal to the processor; only one line is assigned to the plotter at a time.

Table 7-4
Plotter Interface Cable

Signal Line	Function
PEN UP POSITIVE	Raises the plotter pen.
PEN DOWN POSITIVE	Lowers the plotter pen.
CAR LT POSITIVE	Moves the pen carriage one increment to the left.
CAR RT POSITIVE	Moves the pen carriage one increment to the right.
DRUM UP POSITIVE	Causes the paper drum to move up one increment.
DRUM DN POSITIVE	Causes the paper drum to move down one increment.
-24V	When present, indicates that power is applied to the plotter.

7.7 DETAILED THEORY (Refer to BA10 Maintenance Manual, Volume II)

The operation of the plotter control logic during the CONO, DATAO, and CONI instructions and the methods used to clear the XY10 Plotter Control Logic are discussed in the following paragraphs.

7.7.1 CONO Instruction

The CONO instructions establishes initial conditions in the plotter control logic. During a CONO instruction, the processor transmits an IOB CONO CLEAR signal and the plotter device selection number (140_8). These signals are routed to the BA10 via the I/O bus. IOC PL CONO CLEAR is then generated and clears the PLST PLOT DONE flip-flop, the PLST BUSY flip-flop, and the 3-bit priority interrupt register. The processor sends an IOB CONO SET signal 1 μs later.

The IOB CONO SET signal generates IOC PL CONO SET. This pulse loads the priority interrupt channel assignment into the priority interrupt register; sets the PLST PLOT DONE flip-flop, and clears the PLST BUSY flip-flop, if IOB32 is a 1; and/or sets the PLST PLOT BUSY flip-flop, if IOB31 is a 1. To read the plotter status register, the processor must perform a CONI instruction.

7.7.2 CONI Instruction

The CONI instruction is performed after a program interrupt to read the plotter status register. To perform the CONI instruction, the processor transmits an IOB CONI signal and the plotter device selection number to the BA10. IOC PL CONI is generated to enable the plotter control logic status gates. A CONI reads the following information into the processor:

a. If the plotter power is turned on, IOB30(1)
b. If the PLST PLOT BUSY flip-flop is set, IOB31(1)
c. If the PLST PLOT DONE flip-flop is set, IOB32(1).

CONI also causes the priority interrupt channel assignment number to be placed on lines IOB33 through IOB35.

The program determines the status of the plotter system from this information. When the plotter power is on, the PLST PLOT BUSY flip-flop is cleared, and the PLST PLOT DONE flip-flop is set, the plotter is ready for operation.

7.7.3 DATAO Instruction

During the DATAO instruction to the plotter control, various control signals are generated by the plotter control logic and transmitted to the plotter to initiate plotter operations. Due to differences in plotter timing requirements, the raise pen and lower pen operations are discussed separately. The other plotter operations are performed in a similar fashion and are explained as a group.

During a DATAO instruction IOC PL DATAO CLEAR is generated to clear the PLST PLOT DONE flip-flop, to set the PLST PLOT BUSY flip-flop, and to trigger the PLCN REG CLEAR one-shot.

7.7.3.1 **Move Pen or Drum** – The four motions that cause the pen carriage to be moved left or right and the paper drum to be moved up or down (or the carriage rail back and forth on a flat-bed plotter) are similar in nature. The required operation is determined by IOB32 through IOB35. In the following discussion it will be assumed that the pen carriage is to be moved an increment to the right.

When the IOC PL DATAO SET pulse is generated and IOB35 is a 1, the PLCN -Y flip-flop is set. The carriage right positive going pulse (CAR RT POSITIVE) is generated and sent to the plotter via the plotter device cable to move the plotter pen carriage an increment to the right. When the PLCN REG CLEAR one-shot times out, the PLCN -Y flip-flop is cleared and PLCN MOVE DONE is triggered. The trailing edge of the one-shot sets the PLST PLOT DONE flip-flop, which clears the PLST PLOT BUSY flip-flop. A priority interrupt is also generated and routed to the processor via the I/O bus. At this time, the plotter is ready to receive the next control signal.

7.7.3.2 **Raise Pen** – When the IOC PL DATAO SET pulse is generated and IOB30 is a 1, the PLCN RAISE PEN flip-flop is set generating PEN UP POSITIVE, which is applied to the plotter mechanism via the device cable. This causes the pen to be lifted from the paper.

At the completion of the PLCN REG CLEAR delay, which was triggered by IOC PL DATAO CLR, the PLCN REG CLEAR pulse is generated. PLCN REG CLEAR triggers the PLST RAISE DONE one-shot delay and clears the PLCN RAISE PEN flip-flop. When the PLST RAISE DONE delay is completed, it sets the PLST PLOT DONE flip-flop, which clears the PLST PLOT BUSY flip-flop. A priority interrupt request is then sent to the processor via the I/O bus. The plotter control and mechanism are now ready for the next instruction.

7.7.3.3 **Lower Pen** – With this instruction, the conditioning levels described above apply with the exception that IOB31 is a 1. When the IOC PL DATAO SET signal is generated, the PLCN LOWER PEN flip-flop is set, thus generating PEN DOWN POSITIVE. This pulse is routed to the plotter via the device cable to lower the pen.

When the PLCN REG CLEAR one-shot times out, it triggers a 30-ms delay and clears the PLCN LOWER PEN flip-flop. After the 30-ms delay, a second delay, PLCN PEN DONE, is triggered. The completion of this delay produces PLCN PEN DONE, which sets the PLST PLOT DONE flip-flop. PLST PLOT DONE, in turn, clears the PLST PLOT BUSY flip-flop. A priority interrupt is then generated and routed to the processor via the I/O bus. At this time the plotter is ready to receive the next control signal.

7.7.4 Logic Clear

The plotter logic may be cleared by an IOB CONO CLEAR instruction or an IOB RESET pulse sent from the processor to the plotter control via the I/O bus. IOB RESET pulse is inverted to produce IOC RESET, which generates IOC CLEAR. IOC CLEAR generates a 100-ns IOC PL CONO CLEAR pulse, which clears the plotter control logic.

7.8 DECTAPE LOGIC

The XY10 Plotter Contol can be installed in the TD10 Logic Rack. The logic involved is shown on the CONT drawings (refer to Volume II).

When the plotter control is installed in the TD10, the signal designations are slightly different from those used with the BA10. Also, module locations are different.

CHAPTER 8
MAINTENANCE

Maintenance of the BA10 Hard Copy System consists of periodic preventive maintenance procedures, troubleshooting procedures (performed in the event of equipment malfunction), and corrective maintenance procedures (performed to repair equipment malfunctions). It is assumed that maintenance personnel are familiar with the theory of operation of the BA10 Hard Copy System and PDP-10 input/output programming as described in the DECsystem-10 Systems Reference Manual (DEC-10-HGAC-D).

8.1 EQUIPMENT REQUIRED

The BA10 Hard Copy System does not require any special test equipment. Standard test equipment, cleaners, test cables, and probes are considered part of every well-equipped installation and are not listed.

8.2 PREVENTIVE MAINTENANCE

Generally, preventive maintenance consists of periodic checks of the BA10 Hard Copy System to ensure that it is operating satisfactorily. Performance of these checks reduces the possibility of future failure by correcting any inceptive damage or deterioration. The rate of component deterioration is ascertained by examining the maintenance log, which contains previous performance data.

The frequency of all preventive maintenance checks (except for card punch and card reader oil supply and the line printer clutch container checks) should be determined by site conditions, usage, and downtime limitations. For a typical application, a schedule of every four months or 1000-equipment-operating hours (whichever occurs first) is suggested.

8.3 MECHANICAL CHECKS

The following steps should be performed during a mechanical check; the indicated corrective action should be performed if a substandard condition is noted.

Step	Procedure
1	Clean the exterior and the interior of each equipment cabinet with a vacuum cleaner or clean cloths moistened in a nonflammable-nonconductive solvent (be sure the solvent is not harmful to paint).
2	Clean the fan assemblies (be careful not to damage cable assemblies or modules).
3	Visually inspect the equipment and repaint any scratched or chipped areas.
4	Inspect all wiring and cabling for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring.
5	Ensure that each module and cable is securely seated in its connector.
6	Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any defective capacitors.
7	Clean any lint or dust on the exposed surfaces of the card punch, card reader, line printer, and plotter. Clean the plotter pen carriage rods with alcohol.

8.4 POWER SUPPLY CHECK

Check the output voltage and ripple content of the power supplies and ensure that they are within tolerances. Use a multimeter to check the output voltage without disconnecting the load. Use an oscilloscope to measure the peak-to-peak ripple content on the dc output.

Check the two output voltages from the DEC 728 (or 728A) Power Supply at the logic end. These voltages are not adjustable; therefore, if the output voltage or ripple content is not within the tolerance specified, the supply is considered defective and troubleshooting procedures should be performed.

Check the +10V output between the red (+) and black (-) wires to ensure that the output is between +9.5 to +11.0V with less than 800 mV rms ripple. Check the -15V output between the blue (-) and black (+) wires to ensure that the output is between -14.5 and -16.0V with less than 100 mV rms ripple. Check that the black wires are connected to the cabinet frame.

8.5 MARGIN CHECKS

Margin checks are performed to aggravate borderline conditions within the logic circuits, thereby revealing observable faults. In this way, marginal conditions can be corrected to forestall equipment downtime. Margin checks can also be used as a troubleshooting aid for locating marginal or intermittent components. Margin checks are performed by manually varying the logic voltages at the margin control panel of the processor, while performing a diagnostic procedure under program control.

8.5.1 CP10 Margin Checks

Margins are taken using the card punch diagnostic program, MAINDEC-10-DCCPA. The margin voltage must be set prior to running the test program. Approximately 100 cards should be punched for each rack margined. The CP10 margin specifications are listed in Table 8-1.

Table 8-1
CP10 Margin Specifications

Panel	+10 Vdc		-15 Vdc	
	Lower Limit	Upper Limit	Upper Limit	Lower Limit
A	+6.5V	+17.5V	-12V	-18V
B	+6.5V	+17.5V	-12V	-18V
C	+2.5V	+15.0V	-12V	-18V
D	+2.5V	+17.5V	-12V	-18V

8.5.2 CR10 Margin Checks

Margins are taken using the card reader diagnostic program, MAINDEC-10-DCCRA. Set all the switches to zero, except 2 and 4 which are set to one. The CR10 margin specifications are listed in Table 8-2.

8.5.3 LP10 Margin Checks

Margins are taken using the line printer diagnostic program, MAINDEC-10-DCLPA. When making ripple-printout tests, the printer output must be carefully inspected for errors. The LP10 margin specifications are listed in Table 8-3.

Table 8-2
CR10 Margin Specifications

Panel	+10 Vdc		-15 Vdc	
	Lower Limit	Upper Limit	Upper Limit	Lower Limit
C	+7V	+14V	-12V	-18V
D	+7V	+17.5V	-12V	-18V
E	+2.5V	+17.5V	-12V	-18V
F	+2.5V	+17.5V	-12V	-18V
H	+2.5V	+17.5V	-12V	-18V
J	+2.5V	+17.5V	-12V	-18V

Table 8-3
LP10 Margin Specifications

Panel	+10 Vdc		-15 Vdc	
	Lower Limit	Upper Limit	Upper Limit	Lower Limit
A	+2.5V	+17.5V	-12V	-18V
B	+4V	+17.5V	-12V	-18V
C	+2.5V	+17.5V	-12V	-18V
D	+2.5V	+17.5V	-12V	-18V
E	+2.5V	+17.5V	-12V	-18V
F	+2.5V	+17.5V	-12V	-18V
H	+2.5V	+17.5V	-12V	-18V
J	+2.5V	+17.5V	-12V	-18V

8.5.4 XY10 Margin Checks

Margins are taken using the plotter diagnostic program, MAINDEC-10-DCXYA. Margin checks are performed in two parts: one using only the static test of the plotter, and the second using the small-box pattern. The second portion requires visual verification that no pattern deterioration occurs. The XY10 margin specifications are listed in Table 8-4.

Table 8-4
XY10 Margin Specifications

Panel	+10 Vdc		-15 Vdc	
	Lower Limit	Upper Limit	Upper Limit	Lower Limit
E	+4V	+17.5V	-12V	-18V
F	+4V	+17.5V	-12V	-18V
H	+2.5V	+17.5V	-12V	-18V
J	+4V	+17.5V	-12V	-18V
Visual Test				
F	+4V	+17.5V	-12V	-18V
J	-4V	+17.5V	-12V	-18V

8.6 CARD PUNCH LUBRICATION

The card punch should be oiled every 500 hours. Check the time meter located in the lower chassis of the card punch table. Refer to the Soroban Compact Card Punch technical manual for oiling procedures.

8.7 CARD READER OIL SUPPLY

When an oil-lubricated vacuum pump is used, oil vapor is fed to the vacuum pump mounted on the drive motor by a carburetor system in the head of the oil supply system. Oil, which is stored in a reserve container, is automatically fed into a plastic container when the oil level drops below 0.75 oz. Any oil accumulation in the collector is drained at the outlet of the pump.

If the oil level in the reserve container is low, the reserve container should be removed and refilled with one of the lubricants listed below. A valve rod permits the reserve container to be removed and replaced without oil spillage. To fill the reserve container, pull it up and out of the adjusting sleeve and invert. Slowly add oil to the reserve container while depressing the valve stem. Replace the reserve container by quickly inserting it against the stop. To adjust the oil level in the bottom container, loosen the lock nut, and move the adjusting sleeve until the desired oil level is reached.

The recommended lubricant for the card reader is Pneumatic Lubrication Oil, SAE No. 10, Gast Mfg. Corp., P/N AD 220. Acceptable substitutes are American SI No. 10, Citgo C-310, Gulf Gulflube HD-10, Humble Encolube HDX-10, Mobile Delva 1110, Shell Rotalla No. 10, Sinclair Super TBT No. 10, Sun Sunvis 610, or Texaco URSA S-I No. 10.

8.8 XY10 ONE-SHOT ADJUSTMENTS

Table 8-5 lists the increment times for some of the plotter models that can be used with the XY10 Plotter Control Logic. The Time per Step column lists the time required for the paper to move one increment from an initial coordinate for given step size. PLCN REG CLEAR and PLCN MOVE DONE one-shot delays are adjusted to the time per step for the plotter mechanism used. Adjustments are performed in conjunction with the diagnostic program, which yields a typeout of the delay setting. Adjust the appropriate delay until the desired typeout is obtained.

Table 8-5
Increment Times

CalComp Model	Step Size	Steps/Second	Time per Step (ms)
502	All	300	3.3
518	0.005 in.	200	5.0
	0.002 in.	450	2.2
	0.1 mm	200	5.0
	0.05 mm	400	2.5
563	0.010 in.	200	5.0
	0.005 in.	300	3.3
	0.1 mm	300	3.3
565	All	300	3.3
602*	All	450/900	2.2/1.1
618*	0.005/0.0025 in.	200/400	5.0/2.5
	0.002/0.001 in.	450/900	2.2/1.1
	0.1/0.05 mm	200/400	5.0/2.5
	0.05/0.025 mm	450/900	2.2/1.1

*600 Series plotters have a switch that determines the step size.

Table 8-5 (cont)
Increment Times

CalComp Model	Step Size	Steps/Second	Time per Step (ms)
663*	0.010/0.005 in.	350/700	2.9/1.4
	0.005/0.0025 in.	450/900	2.2/1.1
	0.0025/0.00125 in.	450/900	2.2/1.1
665*	All	450/900	2.2/1.1
*600 series plotters have a switch that determines the step size.			

8.9 CORRECTIVE MAINTENANCE

Corrective maintenance procedures for the BA10 Control Logic are detailed in this section. Corrective maintenance procedures for the four options are discussed in separate technical manuals and are not repeated in this section.

The BA10 Control Logic is constructed of highly reliable transistorized modules and standard circuits. Preventive maintenance checks reduce equipment downtime due to failure. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the system. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures.

Diagnosis and remedial action for a malfunction are performed in the following manner:

Step	Procedure
1	Preliminary investigation to gather all information and to determine the mechanical and electrical integrity of the equipment and control logic.
2	System troubleshooting to isolate the malfunction to a module or subassembly through the use of diagnostic programs. If the malfunction is not located via the diagnostic program, signal tracing/aggravation techniques may be used.
3	Repairs to correct the cause of the malfunction. Depending on the availability of spare parts, the module or subassembly may be replaced or, when possible, repaired locally.
4	Validation tests to ensure that the malfunction has been corrected.
5	Log entry to record pertinent data.

8.9.1 Preliminary Investigation

It is virtually impossible to outline any specific procedure for locating malfunctions within the card punch, card reader, line printer, and plotter control logic. Before initiating troubleshooting procedures, explore every possible source of information; ascertain all possible information concerning any unusual function of the system prior to the malfunction and all possible program information (e.g., the routine in progress, the condition of the indicators, etc.). Examine the maintenance log to determine if a particular malfunction has previously occurred and if there is any cyclic history. When the entire control logic fails, perform a visual inspection to determine the mechanical and electrical integrity of all power sources, cables, and connectors. Ensure that the power supplies are operational by performing the power supply checks described in Paragraph 8.2.

8.9.2 System Troubleshooting

Do not attempt to troubleshoot the BA10 Control Logic without gathering all information concerning the malfunction, as outlined in Paragraph 8.9.1.

Commence troubleshooting by repeating the operation during which the malfunction was initially observed, using the same conditions. Eliminate portions of the sequence leading to the malfunction, one at a time, until a manageable, small sequence is obtained that allows the malfunction to be generated at will. Examine the operating conditions for proper control settings and note the operation of all indicators before and at the time of malfunction. Check carefully to ensure that the system is actually at fault before continuing the corrective maintenance procedures. Loose or faulty cable connections often give indications similar to those caused by internal malfunctions.

If the malfunction is located within the control logic, but cannot be localized to a specific logic function, perform the diagnostic program procedure. When the malfunction has been isolated to a specific logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the malfunction is intermittent, a form of aggravation testing may be helpful in locating the malfunction.

The equipment flow charts in Volume II are very useful in system troubleshooting. These charts illustrate the normal sequence of events. When an event does not occur at the proper moment, all possible conditions leading up to its scheduled occurrence can be located on the flow chart and checked for normal operation. All such information can be related in individual logic elements on the block schematics by cross references on the flow diagram.

8.9.3 Diagnostic Programs

8.9.3.1 **CP10 Diagnostic Program** – MAINDEC-10-DCCPA Diagnostic Program represents the most efficient means of troubleshooting the card punch system. These routines provide a complete test of the card punch and control logic under operational conditions.

8.9.3.2 **CR10 Diagnostic Program** – The MAINDEC-10-DCCRA Diagnostic Program, representing the most efficient means of troubleshooting the card reader system, provides a complete test of the card reader and control logic under operational conditions. The diagnostic tests include checks on essentially every circuit in the control logic, with and without card motion. During the diagnostic program, a special deck of cards that contains known data is read by the card reader and the data is transferred into the processor where it is checked under program control. A malfunction during this test will provide an indication of the possible fault.

8.9.3.3 **LP10 Diagnostic Program** – The MAINDEC-10-DCLPA Diagnostic Program provides the most efficient means of troubleshooting the line printer system. This program provides a complete test of the line printer and control logic under dynamic conditions. Ideally, indications that occur in the event of a failure isolate the trouble to the functional component of a single module; however, the indications sometime isolate the malfunction to a relatively large circuit cluster, portions of which are contained on a number of modules. In the latter case, the technician should employ good troubleshooting techniques while continuously repeating the failing diagnostic routine.

8.9.3.4 **XY10 Diagnostic Program** – The MAINDEC-10-DCXYA Diagnostic Program represents the most efficient means of troubleshooting the plotter system. Many plotters, which vary in operational speed, can be used in a plotter system; therefore, various delays are incorporated into the plotter control logic to compensate for the differences. When running the diagnostic program, the user specifies the plotter model being used by setting the console data switches. The program then checks certain gates and delays in the control logic. In addition, a regular pattern is plotted to detect any irregularities.

8.9.4 Signal Tracing

If a malfunction is isolated to a specific logic element, program the processor to repeat instructions so that all functions of that logic element are used. Use an oscilloscope to trace signal flow through the suspected logic

element. The control signals are synchronized with the oscilloscope sweep by connecting the trigger input of the oscilloscope to the appropriate module terminal. The output signals are then traced from the connector to its final destination.

Examine the signals to determine the quality of pulse amplitude, duration, rise time, and the correct timing sequence. If an intermittent malfunction occurs, signal tracing should be combined with an appropriate form of aggravation testing.

8.9.5 Intermittent Malfunctions

Intermittent malfunctions are often detected by tapping the modules while simultaneously running a repetitive routine, such as a diagnostic program. By repeatedly starting the program and tapping fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules and the module connector for wear, misalignment, and malfunction.

CAUTION
The primary ac power is present in the BA10 Power Control when the logic power is turned off.

8.9.6 Module Troubleshooting

The procedure followed for troubleshooting and correcting the cause of the malfunction within modules and power supplies is contingent upon downtime limitations. When downtime must be kept at a minimum, it is suggested that a replacement part be installed and the system tested and returned to normal use. The faulty component should be sent back to Digital Equipment Corporation for repair or repaired off-line.

8.9.7 On-Line Dynamic Tests

When downtime is not critical, signal tracing techniques can be used to troubleshoot modules. Signal tracing techniques are performed as follows:

Step	Procedure
1	Remove the suspected module.
2	Insert a module extender into the module connector.
3	Insert the suspected module into the module extender.
4	Perform a signal tracing procedure with an oscilloscope while the equipment is operated in a routine that uses the module circuits.

8.9.8 Repair

To ensure minimum system downtime, replace defective modules/system components located during system troubleshooting procedures. Remove defective components from the module by cutting the component leads and removing the leads from the printed board. When soldering semiconductor devices, use a heat sink and the smallest soldering iron adequate for the work. Perform all soldering operations in the shortest possible time to prevent damage to components. Replace defective components with components of equal or greater quality.

8.9.9 Validation Test

Following the replacement of any electrical component, a test should be performed to ensure the correction of the malfunction and to make any necessary adjustments. A validation test should include the preventive

maintenance procedure most applicable to the portion of the system in which the malfunction was located. Normally, the diagnostic program serves this purpose. When time permits, it is suggested that the entire preventive maintenance check be performed as a validation test.

8.9.10 Log Entry

Corrective maintenance procedures are not complete until they are recorded in the maintenance log. Record all data indicating the malfunction symptoms, the method of locating the malfunction, and any other information that would be helpful in future maintenance.

8.10 ENGINEERING DRAWINGS

Volume II of the BA10 Maintenance Manual contains engineering drawings including block (logic) schematics, module utilization diagrams, and flow diagrams.

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