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decsystem10

MF10 CORE MEMORY MAINTENANCE MANUAL

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CHAPTER 1
GENERAL INFORMATION

This chapter contains a general functional description of the MF10 Core Memory. It includes an operational overview of the logic, a physical description, and general design specifications.

1.1 GENERAL DESCRIPTION

The MF10 (Figure 1-1) is a coincident current, ferrite core, 3D, 3-wire memory, storing up to 65,536 37-bit words (36 data bits plus 1 parity bit), with a cycle time of 950 ns. The MF10-A is the basic system and is capable of storing 32K word locations (32,768 actual locations). The MF10-E option is a 32K expansion unit, which, installed in a basic MF10-A, yields a 64K MF10-G. As many as 16 memory units may be physically connected to the memory bus; however, memory systems of greater than 262,144 total addressable word locations must be approved by the DECsystem-10 product line.

1.2 SYSTEM DESCRIPTION

The operation of the MF10 within the PDP-10 system is asynchronous; that is, access to memory units is governed by a "request/response" system wherein the processor makes a memory cycle request and waits for a response from a memory unit. Communication between processor and memory unit takes place over the memory bus. Each processor in the system has an associated memory bus which is connected to an active port in each memory unit.

A memory unit may contain up to four MC10-F Access Ports; each port is associated with one particular processor, data channel, multiplexer, etc. (Figure 1-2). If an MX10 Memory Data Multiplexer is included in the system, as many as eight DF10 Data Channels may be associated with one memory port. Priority logic contained in each memory unit designates the sequence in which the processors are granted access in the event of simultaneous requests.

MF10s are compatible with all DECsystem-10 memories and processors. Systems containing multiples of 2 or 4 MF10s may be 2-way or 4-way interleaved, respectively, by setting the interleave switches on the memory unit switch panels. The units must, however, contain equal amounts of storage. Interleaving rotates successive memory cycles between the interleaved memory units if the addressing is sequential. Operation in this mode effectively decreases cycle time which, in turn, reduces processor idle time.

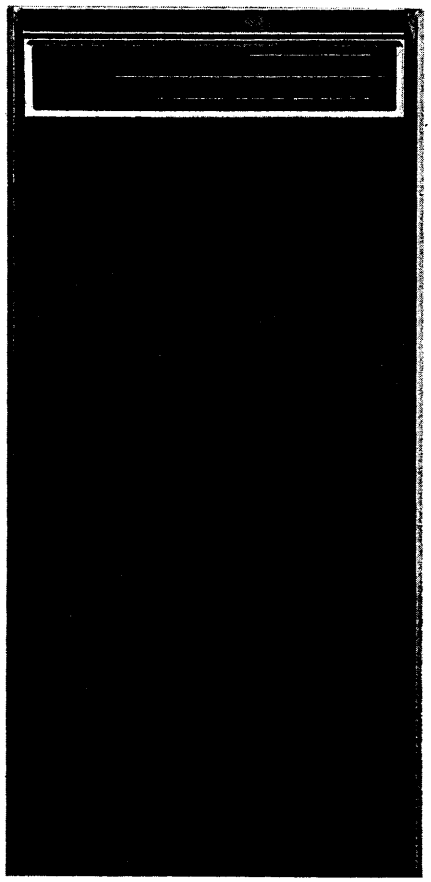


Figure 1-1 MF10 Core Memory

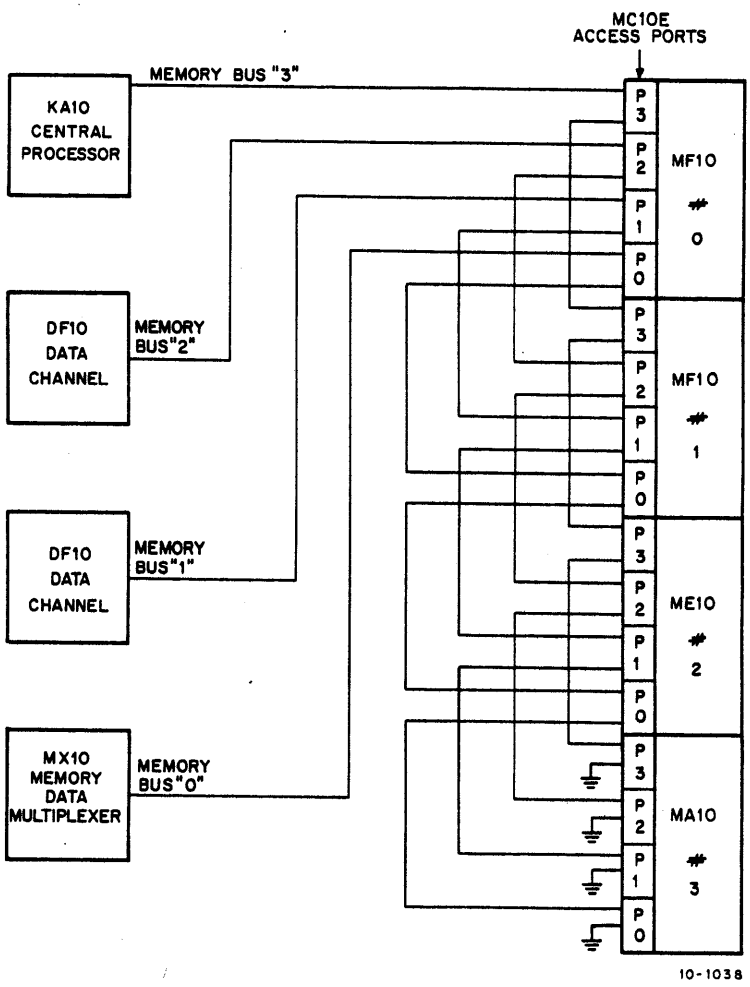


Figure 1-2 System Diagram

1.3 PHYSICAL DESCRIPTION

The MF10 is housed in a standard PDP-10 cabinet (Figure 1-1). The major physical differences in the MF10 and the earlier DECsystem-10 memories are:

a. Higher storage capacity
b. Quick Latch bus connectors (Figure 1-3)
c. Etched back panel boards (Figure 1-4)
d. Maintenance Panel (Figure 1-4).

The Quick Latch bus connectors provide low maintenance, and fast, simple attachment of the bus cable to the four access ports (P0–P3) located at the lower rear of the logic frame. There are two physical connectors (in/out) associated with each port, which are in parallel, allowing Pn of one unit to be daisy chained to the respective Pn of the next unit. These ports are the electrical inputs from the memory bus to the MF10.

The MF10 is divided into two major logic sections: the Core Memory and Control (CMC) section, and the Port Control and Core Interface (PCCI) section. These two sections are connected by six M9170 Core Interface Cables as shown in Figure 1-5.

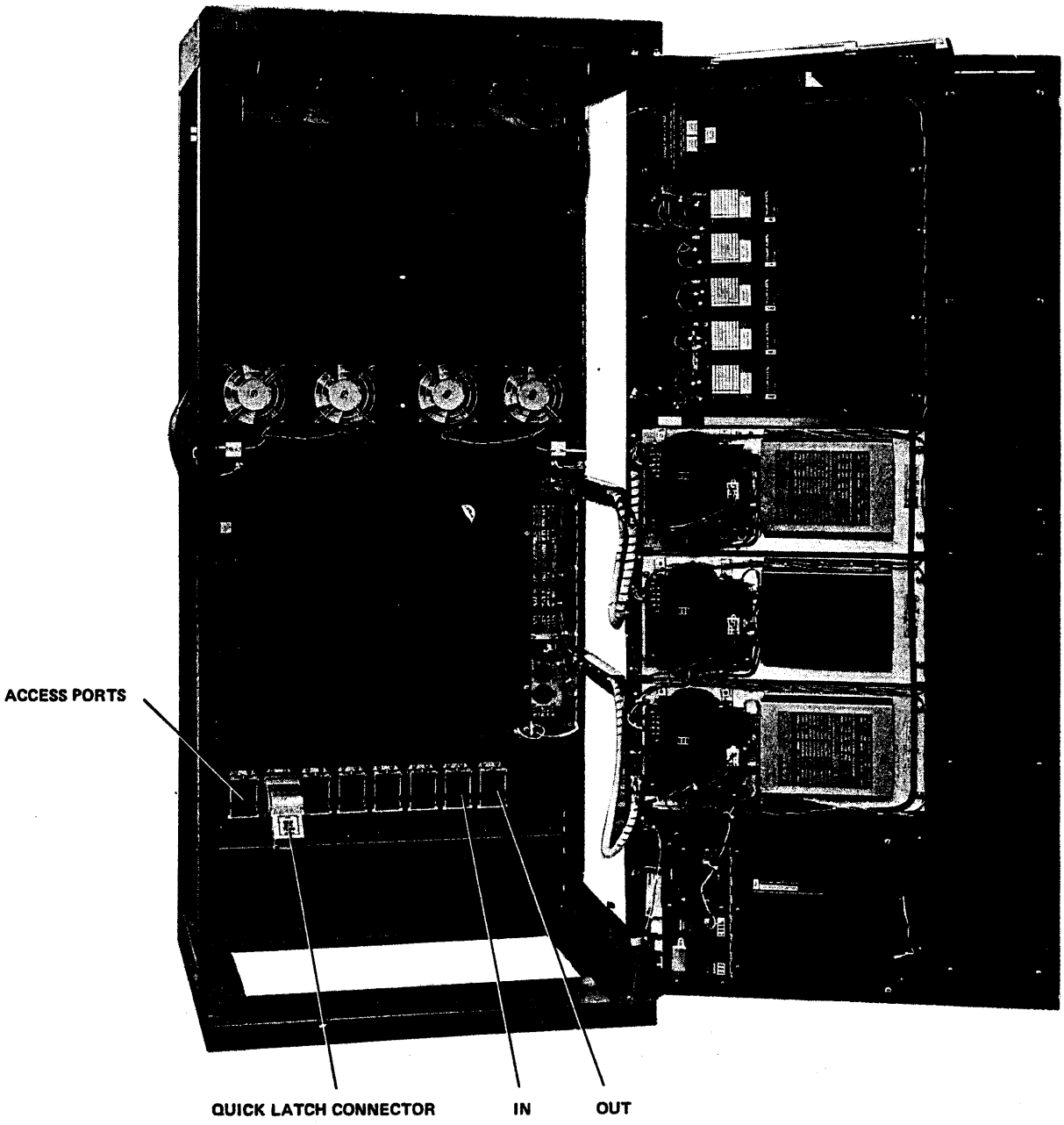


Figure 1-3 MF10 Rear View (Access Ports)

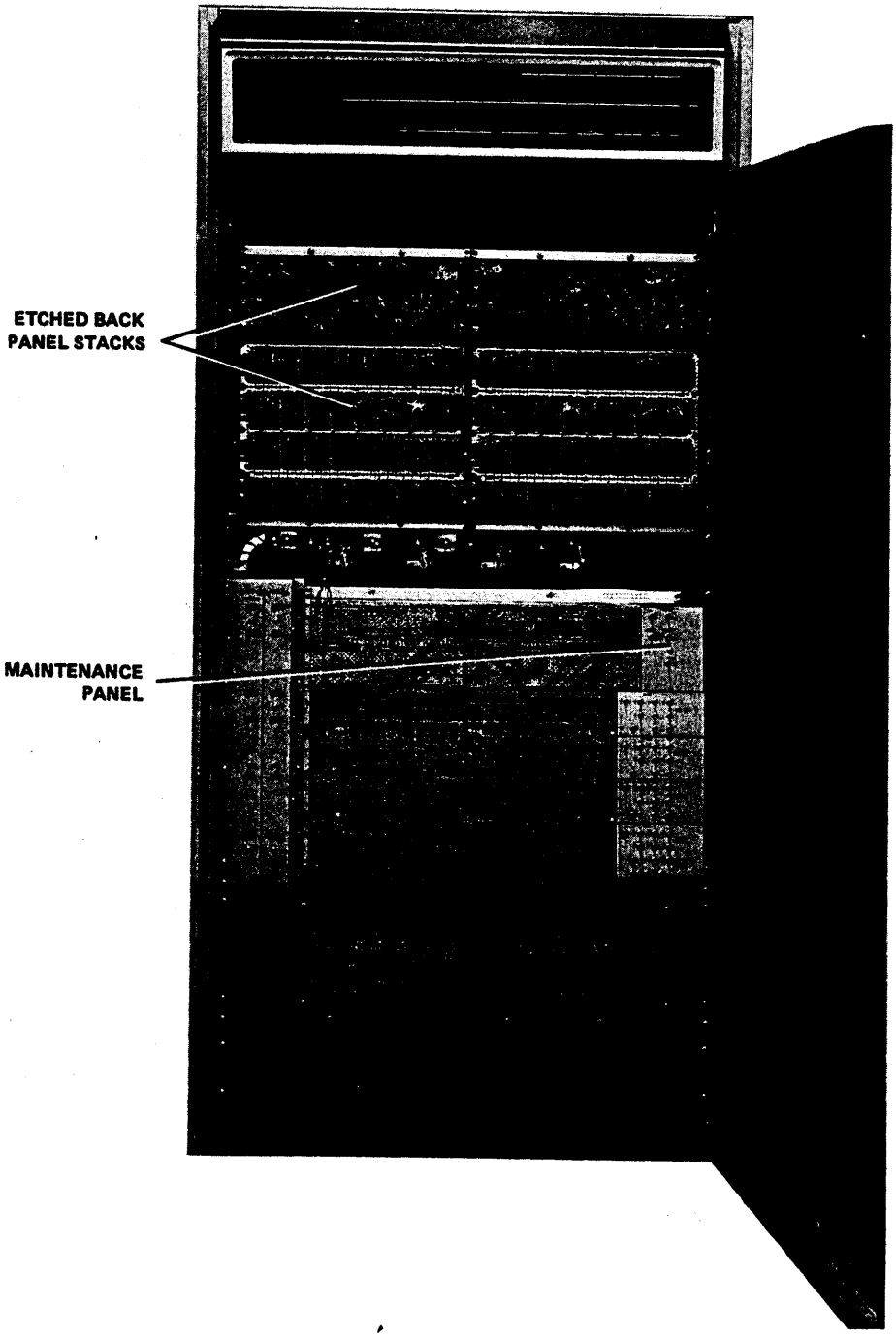


Figure 1-4 MF10 Core Memory Front View (Door Open)

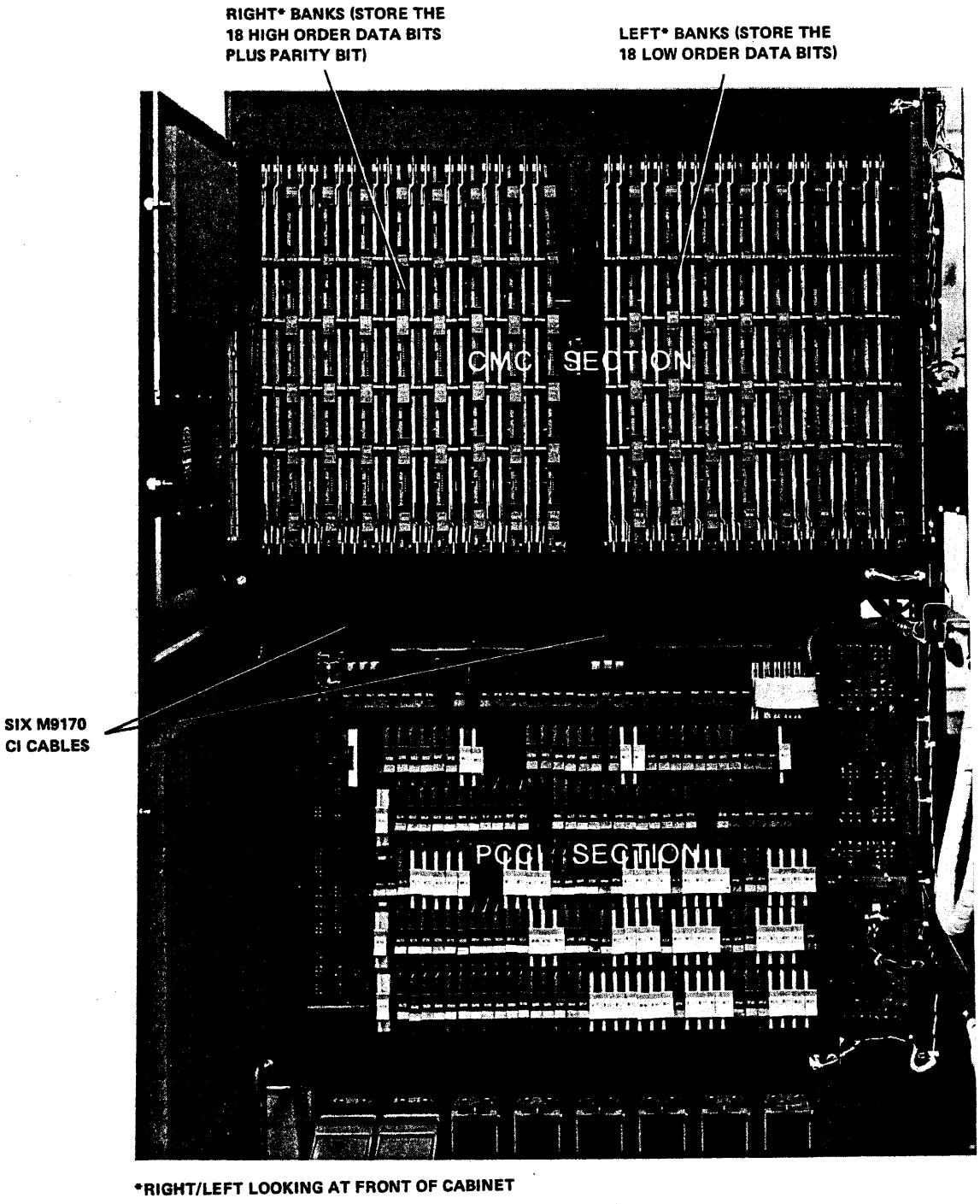


Figure 1-5 MF10 Core Memory Rear View (Logic Sections)

1.4 SPECIFICATIONS

The MF10 Core Memory general specifications are listed in Table 1-1.

Table 1-1
Specifications

Characteristic	Specification
Power Requirements	115 Vac ± 10%, 60 Hz ± 2% 230 Vac ± 10%, 50 Hz ± 2%
Line Current – 60 Hz	14 A
Line Current – 50 Hz	7 A
Power Dissipation	1500 W
Internal Logic Potentials	Positive Logic: 0 V to +3 V Negative Logic: -3 V to 0 V Stack Voltage: -15 V and +5 V
Power Interrupt	Up to 20 ms with no effect on operation. No loss of stored data at power ON/OFF.
Cycle Time	950 ns
Read Access Time	610 ns maximum
Address Acknowledge Time	200 ns maximum
Word Length	36 bits plus parity bit
Memory Size	
MF10-A	32,768 words
MF10-G	65,536 words
Access Ports	4 maximum
Interleaving	2- or 4-way
Dimensions	
Height	72 in. (1.83 m)
Width	33 in. (0.84 m)
Depth	30 in. (0.76 m)
Weight	850 lb (386 kg)
Operating Temperature	60° F to 95° F 15° C to 35° C
Storage Temperature	40° F to 110° F 5° C to 45° C
Relative Humidity	20% to 80%
Heat Dissipation	5100 Btu/hr

1.5 OPERATION OVERVIEW

To begin operation, a processor requests access to a memory unit by placing the memory address on the memory bus along with the type of cycle requested (Figure 1-6). The cycle type is established by the Read Request (Pn MADR RD RQ) and Write Request (Pn MADR WR RQ) signals as follows:

a. Read/Restore Cycle = Pn MADR RD RQ (1) AND Pn MADR WR RQ (0)
b. Clear/Write Cycle = Pn MADR RD RQ (0) AND Pn MADR WR RQ (1)
c. Read/Modify/Write Cycle = Pn MADR RD RQ (1) AND Pn MADR WR RQ (1)

Memory address bits 14–20 are decoded in the Port Address Selection (PAS) logic by ANDing them with the memory address switches. In the event of simultaneous requests, the memory port priority logic determines the highest priority port request; then, the ADR ACK (Address Acknowledge) pulse is sent to the corresponding processor, signifying acceptance of the request.

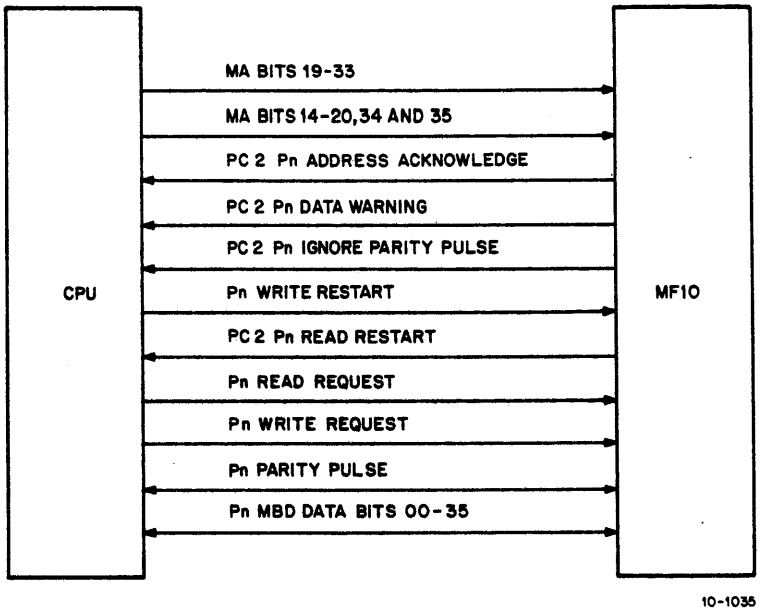


Figure 1-6 Memory/Processor Interface

1.5.1 Read/Restore Cycle

The read/restore cycle transfers data from a selected memory location to a requesting processor. During the read portion of this cycle, the memory reads data from the addressed memory location and loads it into the memory data latches (registers). From there the data, accompanied by a parity pulse, is placed on the bus to the requesting processor. If the parity bit is not operational, the IGN PARITY (Ignore Parity) pulse is sent to the processor. Concurrent with the IGN PARITY pulse, the RD RS (Read Restart) pulse is sent to the processor, indicating that the data requested has been sent. During the restore portion of the cycle, the memory disconnects from the bus and writes the data in the memory data latches back into the addressed memory location. This last step is necessary because the MF10 is a destructive readout memory.

1.5.2 Clear/Write Cycle

The clear/write cycle transfers data from a processor to a selected memory location. During the clear portion of the cycle, the memory reads data from the addressed memory location, discards it, and loads the data from the processor into the memory data latches. During the write portion of the cycle, the processor sends the parity bit and raises the WR RS (Write Restart) signal to the memory which then writes the new data and parity bit contained in the memory data latches into the addressed memory location.

1.5.3 Read/Modify/Write Cycle

The read/modify/write cycle transfers data from a selected memory location to a processor for modification and then transfers the modified data back to the selected memory location. During the read portion of the cycle, the memory reads the data from the addressed memory location, loads it into the memory data latches, places the data on the bus to the processor, clears the memory data latches, and pauses. While the memory pauses, the processor modifies the data (modify portion) and initiates the write portion of the cycle by placing the modified data on the bus and raising the WR RS signal. The memory then loads the modified data into the memory data latches and writes it into the same selected memory location.

1.6 MAJOR LOGIC SECTIONS

A brief description of the two major logic sections is presented in the following paragraphs. The PCCI section comprises the Request-Acknowledge and Port Priority Selection logic, as well as logic that initiates and controls the interfacing between the two sections. The CMC section comprises the core memory stack, and the addressing and timing control logic for reading and writing the data words. Figure 1-7 shows major control signals and data flow, and the logic subsection interconnections.

1.6.1 Port Control and Core Interface Section (PCCI)

The PCCI consists of the following logic sections and is illustrated on Engineering Drawings:

a. Port Address Selection (PAS) – consists of memory address switches and logic for selecting the proper MF10 module (unit).

b. Port Control (PC) – consists of the logic that performs the following:

   1. port priority selection in the event of simultaneous requests
   2. generates strobe to load the Memory Address Register
   3. generates signals that control the entrance and exit of data and other interface signals.

c. Memory Control (MC) – consists of status logic (e.g., run, stop, cycle done, etc.) and conditioning logic (e.g., restart, error stop, start, single step, reset, clear, etc.).

d. Memory Address (MA) – contains the Memory Address Register with associated input/output gating, and the Read and Write Request flip-flops.

e. Memory Buffer (MB) – contains the Memory Data Buffer with associated input/output gating, and the data transmitters/receivers.

f. Core Interface (CI) – consists of logic levels generated for transmission to the Core Memory and Control Section over the core interface cable (CIC) for initiation and control of the read/write timing sequence. Core memory status signals are received from the CMC section over the CIC in this section.

1.6.2 Core Memory and Control Section (CMC)

The CMC is divided into sections or banks, each bank providing 8K, 19-bit words of memory. The banks are organized in two groups: the left banks which store the low order bits (00–17), and the right banks which store the high order bits (18–35) plus the parity bit. Thus, the left banks and the right banks combine to form a 37-bit word memory.

For addressing purposes, the banks are considered in pairs with each pair consisting of one left bank and one right bank. The MF10 may have four bank pairs or eight bank pairs, depending on the memory size desired (32K or 64K). The bank pairs of a memory are addressed as bank pairs 0 through 3 (32K) or 0 through 7 (64K). A memory address is decoded to determine the bank pair number as well as the particular word address in that bank pair. Bank pair number 0 contains the lowest 8K memory addresses, bank pair number 1 contains the next to the lowest 8K memory addresses, and so on.

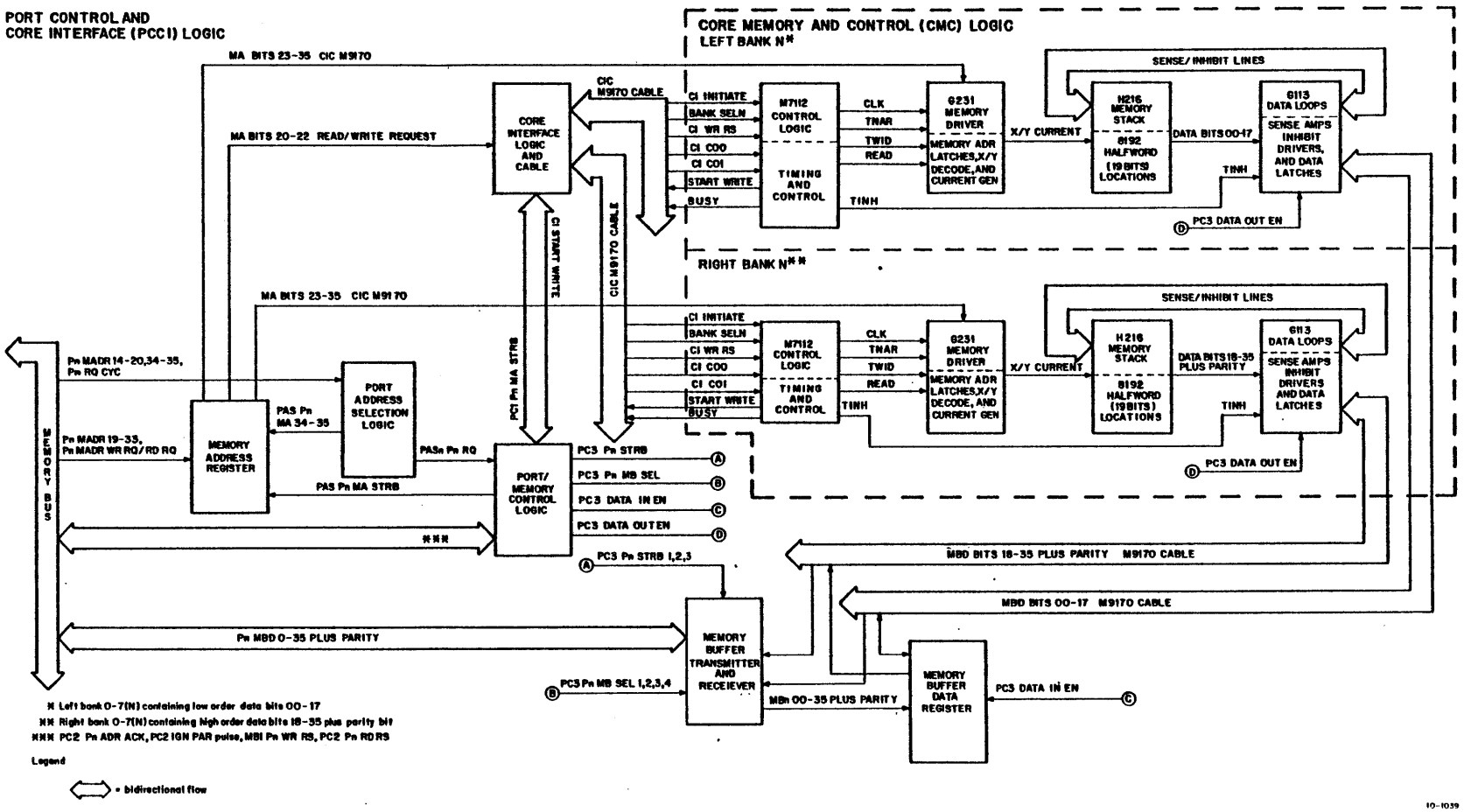


Figure 1-7 Logic Subsection Interconnection Block Diagram

The MF10 shown in Figure 1-5 is a 64K unit and contains sixteen 8K, 19-bit word memory banks. Each memory bank consists of four modules:

a. M7112 Control Logic
b. G231 Memory Driver
c. G113 Data loop
d. H216 Stack.

1.6.2.1 **M7112 Control Logic** – This module contains the logic which generates the timing and other signals that control addressing and reading/writing of the data.

1.6.2.2 **G231 Memory Driver** – This module contains the address selection logic, switches and drivers, current generator, stack discharge circuit, and DC LO protection circuit.

1.6.2.3 **G113 Data Loops** – This module contains the sense amplifiers, inhibit drivers, data latches, strobe circuit, and -5 V supply.

1.6.2.4 **H216 Stack** – This module contains the ferrite core array and the X/Y diode matrices. The core array consists of 19 mats, each wired in a 128 X 64 matrix. The stack also contains the resistor-thermistor combination to control the X/Y current generator temperature compensation.

1.7 INTERLEAVING

Interleaving logic allows 32K and 64K MF10 memory units to be addressed in a manner that allows consecutive memory addresses to alternate between two memories or rotate through four memories.

Only memories of the same size and having consecutive port addresses with an even port address first may be interleaved. For example, 2-way interleaving can exist between memories 0 and 1 but not between 1 and 2; 4-way interleaving can exist between memories 0, 1, 2, 3 but not between 1, 2, 3, 4.

Interleaving is accomplished by swapping port address bits with word address bits. Functionally the memory address can be divided into three segments:

		Segments	
Memory Size	Port Address Bits	Bank Select Bits	Word Address Bits
32K	14 – 20	21, 22	23 – 35
64K	14 – 19	20 – 22	23 – 35

When 2-way interleaving is selected, the least significant port address bit (bit 20 for 32K and bit 19 for 64K) is swapped with the least significant word address bit (bit 35). In this configuration, should the processor generate consecutive addresses starting at address 0 of MF10 number 0, the subsequent memory cycles would alternate between MF10 memories 0 and 1, addressing only the even word locations (0, 2, 4. 6, etc.) until all the even locations were addressed, and then addressing all the odd locations (1, 3, 5, 7, etc.) until all locations were addressed. This sequence would be continuously repeated until the processor ceased generating consecutive addresses.

When 4-way interleaving is selected, the two least significant port address bits are swapped with the two least significant word address bits. In this configuration, should the processor generate consecutive addresses starting at address 0 of MF10 number 0, the subsequent memory cycles would rotate between MF10 memories 0, 1, 2, and 3, starting at address 0. Memory locations would be addressed in the following sequence at each of the four MF10 memories:

a. 0, 4, 10, 14, 20, 24, etc.
b. 1, 5, 11, 15, 21, 25, etc.
c. 2, 6, 12, 16, 22, 26, etc.
d. 3, 7, 13, 17, 23, 27, etc.

This addressing sequence would be continuously repeated until the processor ceased generating consecutive addresses.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter, in conjunction with the *PDP-10 Site Preparation Guide* and the Engineering Drawings provided with each unit, contains the information required for installation of the MF10.

2.2 SITE PREPARATION

There are no special site requirements other than those dictated by environmental conditions (Table 1-1) and service clearances (Figure 2-1). Subflooring is not normally required. The units are free standing; up to four units may be bolted together. The memory unit installed closest to the CPU should not be separated from it by more than 3 feet* or less than 1/4 inch.

2.3 INSTALLATION PROCEDURE

After removing the equipment packing material, visually inspect the exterior and interior of the equipment; ensure that all modules are properly seated.

CAUTION

Check to ensure that logic pins are not shorted together before applying power to equipment.

2.3.1 Cabling

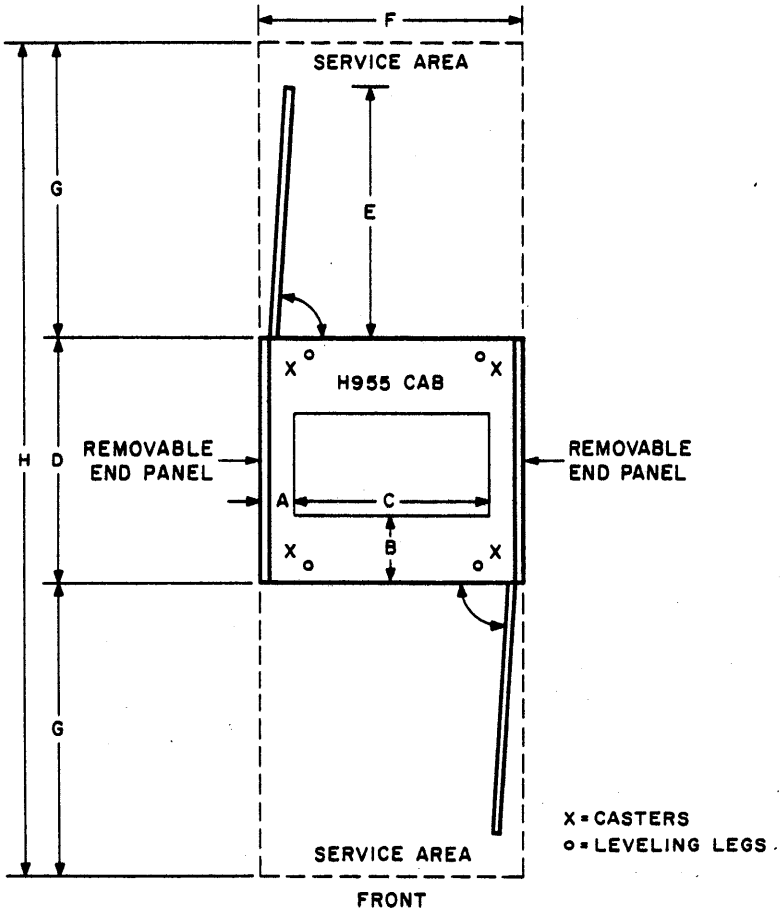
All cables enter or leave the memory unit through access cutouts under the bottom right and left sides. Figure 2-2 shows an example of a system configuration with cabling data.

2.3.1.1 Memory Bus – One memory bus cable is required for connection of the unit to a processor, or to another memory unit if more than one unit is included in the system. One memory bus cable is included for each MC10-F Access Port option (all access ports are optional), with a maximum of four ports per unit. The maximum allowable physical length of the memory bus is 100 feet, including wire runs through each memory unit. The memory bus must be terminated in the last memory unit in the system using one H866 type terminator per access port.

CAUTION

Do not force connection when installing memory bus cable with Quick Latch cable connector.

*Speedy, the processor timing program, is written for the standard 10 foot memory bus cable connection between the CPU and the first memory unit. If lengths in excess of 10 feet are used, Speedy timing printouts will not agree with the timing specifications.



DIMENSIONS	A	B	C	D	E	F	G	H
INCHES	3.7	7.5	24	30	31	31.5	36	102
METERS	0.09	0.19	0.61	0.76	0.79	0.8	0.91	2.6

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Figure 2-1 MF10 Core Memory Service Clearances

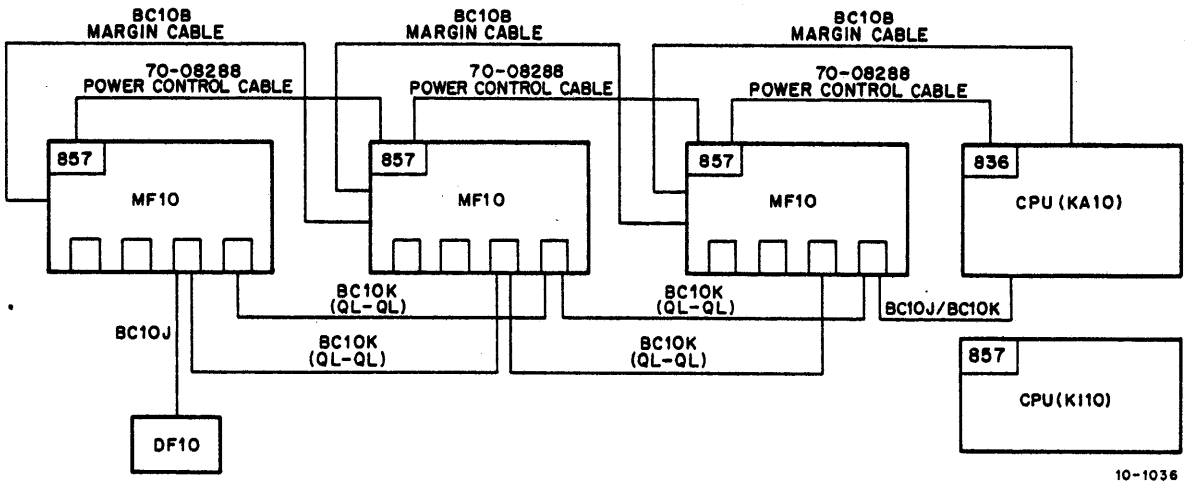

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Figure 2-2 MF10 Cabling

2.3.1.2 **AC Power** – Each 60-Hz MF10 unit is furnished with a 3-wire ac power cable with the Hubbell 2611 Twist-Lok plug to be mated with a Hubbell 2610 receptacle. For 50-Hz users, a Hubbell 2321 Twist-Lok plug is mated with a Hubbell 2320 receptacle. Ensure that the power supplies are jumpered for the appropriate line voltage (115 or 230 Vac). Appropriate jumper configurations are shown on the power supply label.

2.3.1.3 **Power Control** – The 857 Power Controls in all cabinets must be interconnected to enable central control of power ON/OFF from the PDP-10 console power switch.

There are three Mate-N-Lok connectors on each 857 Power Control for interconnection via a 3-wire bus (Figure 2-3). One 3-wire bus cable is supplied with each cabinet to connect the 857 Power Control to the 857 Power Control in the next cabinet. Since each power control must connect to the power controls in the preceding and following cabinets, two Mate-N-Lok connectors are reserved for the intercabinet bus. A third connector is provided for connection to the cabinet-mounted thermal switches and to the PDP-10 console power switch.

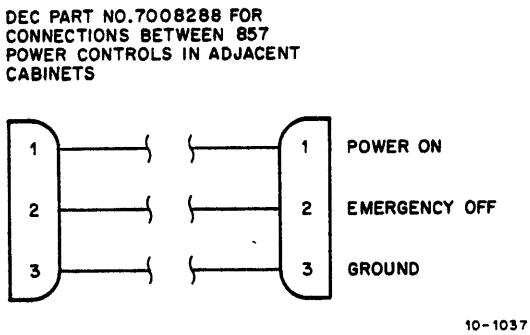


Figure 2-3 Remote Power Control Cable

Ensure that the REMOTE/LOCAL toggle switch on the 857 Power Control is in the REMOTE position before operating the MF10 on-line with the processor, if remote control is desired. Also ensure that the ac line voltage select switch on the 857 Power Control selects the proper ac line voltage level (115 Vac or 240 Vac position).

2.3.1.4 **Ground Mesh Cable** – Connect a No. 4 gauge wire from the copper bolt on the bottom of the MF10 cabinet to the adjacent cabinet(s).

2.3.2 W974 Module Size Jumpers

The W974 size jumper module (drawing D-BS-MF10-0-PAS1/2) selects the two high order address bits which are interchanged with bits 34 and 35 when interleaving. Bits 19 and 20 are used for the MF10-A, and bits 18 and 19 are used for the MF10-G. Table 2-1 shows the jumper connections for the 32K and 64K memory sizes. Ensure that the maintenance panel SIZE switch (Figure 3-4) is in the correct position (32K or 64K) for memory unit installed.

Table 2-1
W974 Module Size Jumpers

32K Jumpers		64K Jumpers	
From	To	From	To
H1	K1	F1	K1
F1	J1	E1	J1
H2	K2	F2	K2
F2	J2	E2	J2
P1	S1	N1	S1
N1	R1	M1	R1
P2	S2	N2	S2
N2	R2	M2	R2

2.3.3 G726-YA Module Jumpers

Ensure that the G726-YA module (drawing D-BS-MF10-0-PAS1/2) for each port is jumpered correctly for the corresponding KA10 or KI10 type memory bus used in that port.

2.3.4 Memory Address Switch Settings

The MF10 port address must be established prior to memory operation. The port address is established via toggle switches on the memory address switch panel. There is one switch panel for each of four memory ports and all four panels must be set to the same address. Table 2-2 lists address switch settings for a typical system having eight 32K MF10-A memories connected to one KA10 or KI10 processor memory bus.

Note that KA10 based memory systems are limited in size. If a KA10 processor is used, the number of 32K MF10 memories connected to its bus must not exceed eight. This limitation is dictated by the memory addressing capability of the KA10 (256K word locations).

Table 2-2
MF10-A (32K) Memory Address Switch Settings

Memory Addresses	MF10 No.	MADR Switches*						
		14	15	16	17	18	19	20
000000–077777	0	0	0	0	0	0	0	0
100000–177777	1	0	0	0	0	0	0	1
200000–277777	2	0	0	0	0	0	1	0
300000–377777	3	0	0	0	0	0	1	1
400000–477777	4	0	0	0	0	1	0	0
500000–577777	5	0	0	0	0	1	0	1
600000–677777	6	0	0	0	0	1	1	0
700000–777777	7	0	0	0	0	1	1	1

*If processor KA10 is used, switches 14 through 17 must be set to IGN (Ignore).

Note: If the KA10 processor is used, only eight 32K MF10-A memories can be connected to the memory bus.

MF10 memories connected to a KA10 memory bus must have consecutive addresses. For example, if only five 32K MF10-A memories are connected to a KA10 memory bus, they must be addressed 0 through 4. If this addressing procedure is not followed, holes are created in the memory address space and the KA10 will attempt to address memory that does not exist.

When 64K MF10-G memories are connected to the memory bus, the memory address switch panel toggle switches are set a little differently. Only four MF10-G memories can be connected to the KA10 processor memory bus due to the memory size limitation of the KA10. The toggle switches representing bit 18 in the 32K port address must now be set to IGN (Ignore) and toggle switches previously identified as 19 and 20 become 18 and 19. This effectively reduces the port address capability by a factor of 2 but does not affect addressing capability of the processor. Table 2-3 lists address switch settings for a typical system having four 64K MF10-G memories connected to one KA10 memory bus or eight MF10-G memories connected to one KI10 memory bus.

Table 2-3
MF10-G (64K) Memory Address Switch Settings

Memory Addresses	MF10 No.	MADR Switches*						
		14	15	16	17	IGN	18	19
000000–177777	0	0	0	0	0	IGN	0	0
200000–377777	1	0	0	0	0	IGN	0	1
400000–577777	2	0	0	0	0	IGN	1	0
600000–777777	3	0	0	0	0	IGN	1	1
1000000–1177777	4	0	0	0	1	IGN	0	0
1200000–1377777	5	0	0	0	1	IGN	0	1
1400000–1577777	6	0	0	0	1	IGN	1	0
1600000–1777777	7	0	0	0	1	IGN	1	1

*If processor KA10 is used, switches 14 through 17 must be set to IGN (Ignore).

Note: If processor KA10 is used, only four 64K MF10-G memories can be connected to the memory bus.

2.3.5 Interleave Switch Settings

Interleaving of MF10 memories is controlled by two toggle switches located on the memory address switch panel. These switches are used to select normal (non-interleaved) operation, 2-way interleaved operation, and 4-way interleaved operation. Table 2-4 lists switch settings for the different interleaved situations.

NOTE

Only memory units with the same number of memory locations can be interleaved; i.e., a 32K memory cannot be interleaved with a 64K memory (Paragraph 1.7).

Table 2-4
Interleave Switch Settings

Mode	MADR Switches	
	34	35
Normal	NORM	NORM
2-way	NORM	INTL
4-way	INTL	INTL

Note: Only memory units with the same number of word locations can be interleaved.

CHAPTER 3
OPERATION

3.1 INTRODUCTION

The MF10 controls and indicators are grouped on five separate panels: memory address switch panel, maintenance panel, margin switch panel, indicator panel, and the 857 Power Control panel. The following paragraphs state the purpose of each panel and describe each control and indicator. Figure 3-1 shows all the panels except the 857 Power Control (Figure 3-2) which is mounted to the rear door of the cabinet.

3.2 PANEL OPERATION

Generally, the panels can be described as follows:

a. The 857 Power Control panel controls input power to the MF10.

b. The memory address switch panels control access port operation.

c. The maintenance panel, the margin switch panel, and the indicator panel provide fault detection, checkout, and troubleshooting controls and indicators.

3.2.1 857 Power Control Panel

The 857 Power Control panel (Figure 3-2) performs the following functions:

a. adapts the MF10 to different ac line voltage inputs

b. enables central control of power turn ON/OFF from the PDP-10 console power switch

c. initiates power shut-down if any of the memory logic door interlocks or the air flow sense switches are activated (Paragraphs 4.6.1.4 and 4.6.1.5)

d. enables memory logic door interlocks and air flow sense switch to be overridden for maintenance purposes

e. provides circuit breaker protection against overloading.

Tables 3-1 and 3-2 describe the 857 Power Control panel switches and indicators.

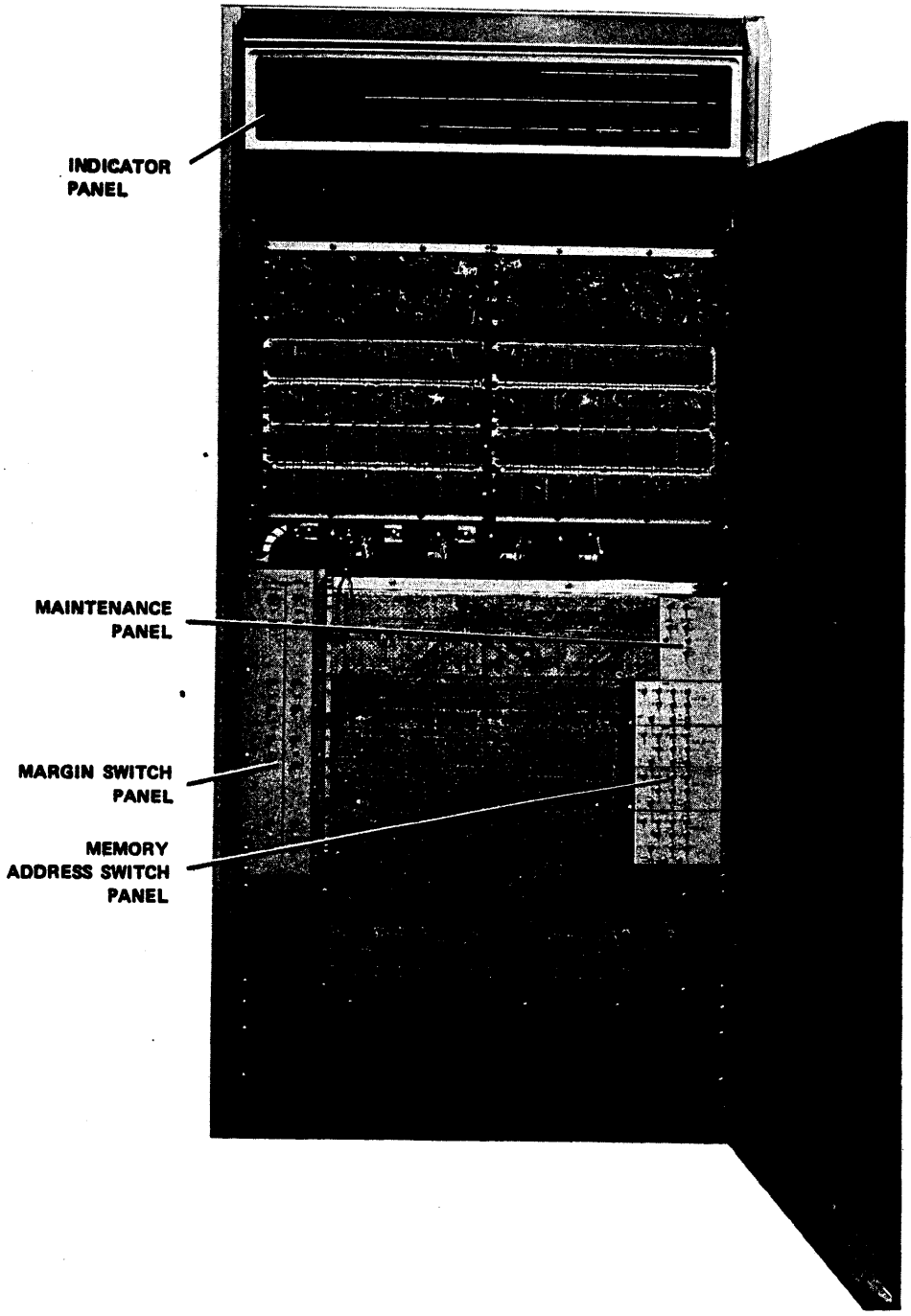


Figure 3-1 MF10 Switch Panel Locations

Figure 3-2 857 Power Control Panel

Table 3-1
Power Control Switches

Switch	Function
LOCAL/OFF/REMOTE	Allows power turn ON/OFF from the CPU (REMOTE) or from the MF10 unit (LOCAL).
OVERRIDE	Overrides the temperature sense switches and door interlock switches.
AC Line Select Voltage	This switch is set for the ac line voltage that is supplied.
Power ON/OFF	This is the ac input line voltage circuit breaker.

Table 3-2
Power Control Indicators

Indicator	Function
PWR SW ON	Lights when ac power is applied to all power supplies in the memory unit. A flashing light means that the OVERRIDE switch is on.
DOORS OPEN	Lights when either or both of the logic cabinet doors are open.
CKT BRK TRP'D	Not Used.
OVERTEMP	Lights when an overtemperature condition occurs.
AC Line Lamp	Lights when ac line voltage is present.

3.2.2 Memory Address Switch Panel

Each of the memory address switch panels (Figure 3-3) performs the following functions:

a. enables or disables the access port circuitry

b. establishes the access port address

c. selects 32K or 64K access port operation

d. selects interleaved or non-interleaved memory operation.

The P3 Memory Address Switch panel contains additional switches which aid in the detection and location of errors occurring in the memory control logic. Refer to Table 3-3 for a description of memory address switch panel switches.

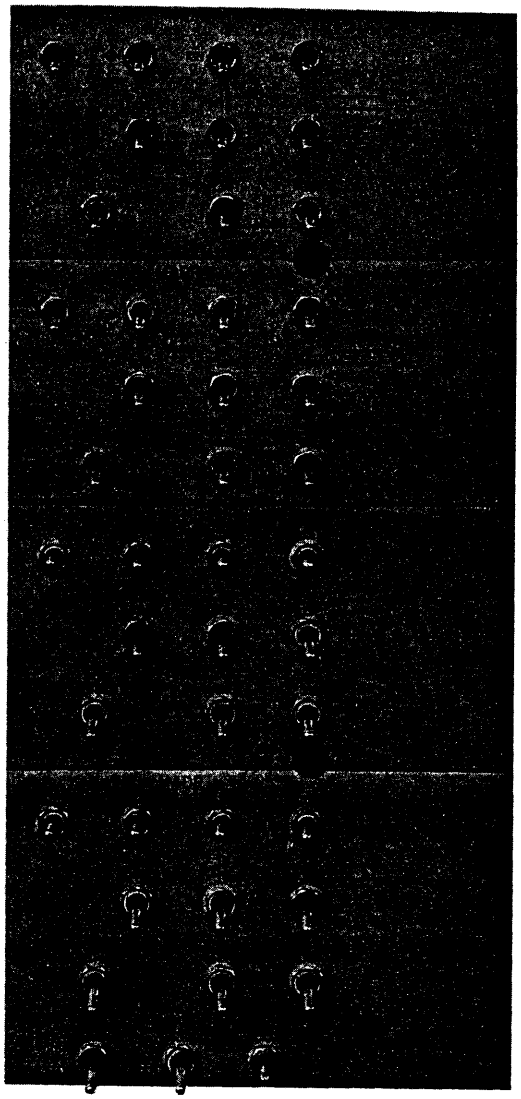


Figure 3-3 Memory Address Switch Panel

Table 3-3
Memory Address Switch Panel

Switch	Function	Engineering Drawing No.
MADR 14–20*	Three-position toggle switches which are set to establish the address of the memory unit, allowing memory address bits 14–20 to select a particular unit (Paragraph 2.3.4).	MF10-0-PAS1/2
SEL/DES*	The Select/Deselect two-position toggle switch is the master port selection switch, which allows the memory port to be switched on/off-line.	MF10-0-PAS1/2
INTL/NORM 34,35*	Two-position toggle switches which select 2- or 4-way interleave or normal mode operation. (See Table 2-4 for interleave switch settings.)	MF10-0-PAS1/2
ERROR STOP	When in the up position, causes the STOP indicator to light and prevents further memory cycles when a memory control logic error is detected. The STOP condition is cleared with the RESET switch.	MF10-0-MC1
SINGLE STEP**	When in the up position, prevents the completion of the memory cycle but allows the completion of one memory cycle each time the RESET switch is activated. (The request and acknowledge portion of the cycle is allowed, but the read/write portion is inhibited.)	MF10-0-MC1 and MF10-0-CI2
RESET	Spring-loaded momentary switch which clears and initializes the memory when placed in the up position.	MF10-0-MC1 and MF10-0-CI2

*These switches are duplicated for each of the four ports and all four ports should be set to the same address.
**All 0s are written into memory when SINGLE STEP is used on a clear/write cycle.

3.2.3 Maintenance Panel

The maintenance panel (Figure 3-4) assists in maintaining the MF10. The only switch on the panel which does not perform a maintenance function is the SIZE switch. Refer to Table 3-4 for maintenance panel switch description. The circuitry for each switch is shown on the engineering drawing listed to the right of the switch description.

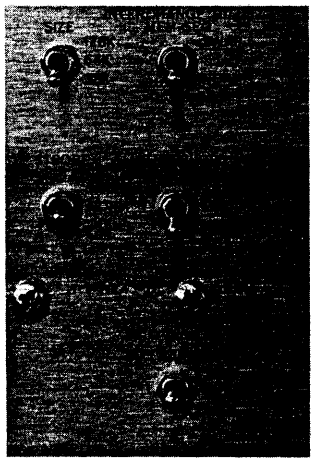


Figure 3-4 Maintenance Panel

Table 3-4
Maintenance Panel Switches

Switch	Function	Engineering Drawing No.
SIZE*	Three-position switch which enables the memory unit to decode the memory address to select the proper banks for 32K or 64K word locations.	MF10-0-CI1
MEM SEG (Memory Segment)	Two-position switch which enables the lower 32K (banks 0–3) of a 64K memory unit to be interchanged with the upper 32K (banks 4–7).	MF10-0-CI1
STROBE POSITION	Three-position switch which varies sense amplifier STROBE by ±15 ns to check for marginal CMC conditions.	
THRESHOLD VOLTAGE	Two-position switch which allows sense amplifier threshold amplitude to be varied from +4 V to +6 V via the margin check vernier on the CPU maintenance panel, with the MARGIN CHECK selection switch in the +10 L/R position. The THRESHOLD switch, located on the margin switch panel, must be in the VAR (variable) position to permit threshold amplitude variation. The NORM position of the THRESHOLD VOLTAGE switch applies a fixed +5 V to the sense amplifiers.	MF10-0-CI2
X/Y CURRENT	This two-position switch increases or decreases X/Y core selection currents by ±5% of 440 mA to check for marginal CMC conditions.	MF10-0-CI2

*A switch position is provided for 128K size selection for future systems.

3.2.4 Margin Switch Panel

The margin switch panel (Figure 3-5) also assists in the maintenance of the MF10. The panel is used to perform monthly preventive maintenance checks to locate marginal operational modules; i.e., modules that are deteriorating (due to age or other factors) and will probably fail in the near future. The panel may also be used to cause intermittent failures to become constant, and thereby facilitate troubleshooting.

The margin switches (H-N) are used to perform marginal operation checks on logic module rows in the PCCI logic section. By placing the margin switches in the VAR (variable) position, the fixed voltages (+10 V and −15 V) normally applied to the modules are replaced by variable voltage via the margin cables. These variable voltages are controlled by the margin check vernier located on the CPU. The module must operate without errors in the voltage range specified in Table 3-5 to pass the maintenance check.

The THRESHOLD switch is used in conjunction with the maintenance panel THRESHOLD VOLTAGE switch (Table 3-4) to provide a variable threshold voltage (+4 V to +6 V) to the sense amplifiers. Placing the THRESHOLD switch in the VAR position applies +10 V ± 7.5 V to the G024 Slice Control module (drawing D-BS-MF10-0-CI2) via the margin cable. This voltage is variable via the CPU margin check vernier. The slice control module is adjusted for +5 V output with a +10 V input. The input voltage may then be varied from +2.5 V to +17.5 V to provide the +4 V to +6 V output.

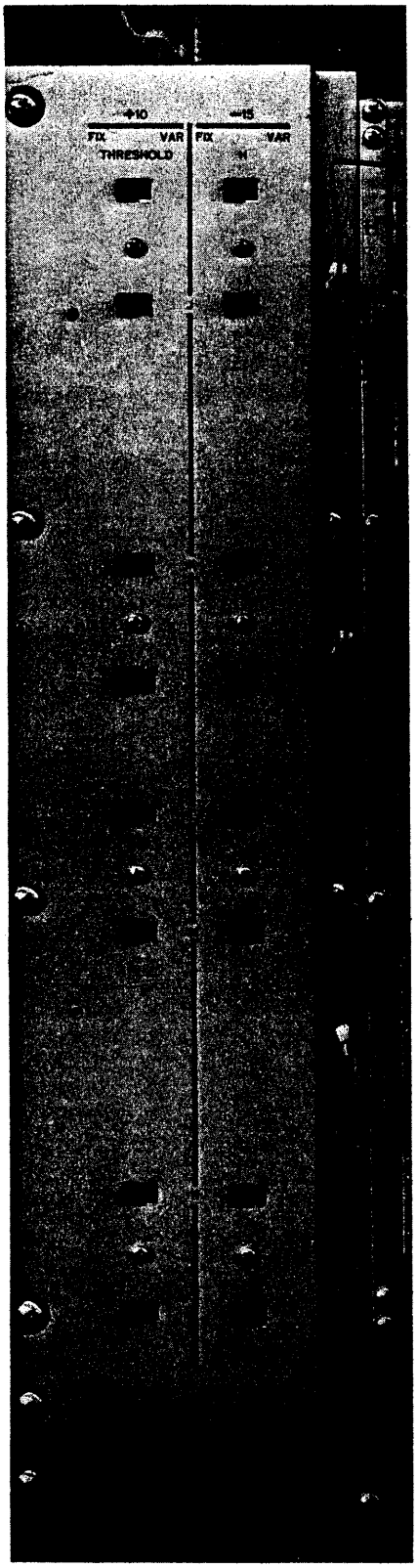


Figure 3-5 Margin Switch Panel

Table 3-5
Margin Specifications

Row	+10 V Margins	-15 V Margins
H	Threshold +2.5 V to +17.5 V	-12 V to -18 V
J	+2.5 V to +17.5 V	-12 V to -18 V
K	+2.5 V to +17.5 V	-12 V to -18 V
L	+6.0 V to +17.5 V	-12 V to -18 V
M	+5.0 V to +16.0 V	-12 V to -18 V
N	+6.0 V to +16.0 V	-12 V to -18 V

3.2.5 Indicator Panel

The indicator panel (Figure 3-6) provides memory operation status indicators to aid in the maintenance of the MF10. Visual displays indicate memory operation and the contents of the Address and Buffer Registers. When an operation indicator lights, the function identified is active or true; when a register indicator lights, the particular bit position identified contains a binary 1. The register indicators (Table 3-6) are grouped in octal format to facilitate translation of the binary word segments.

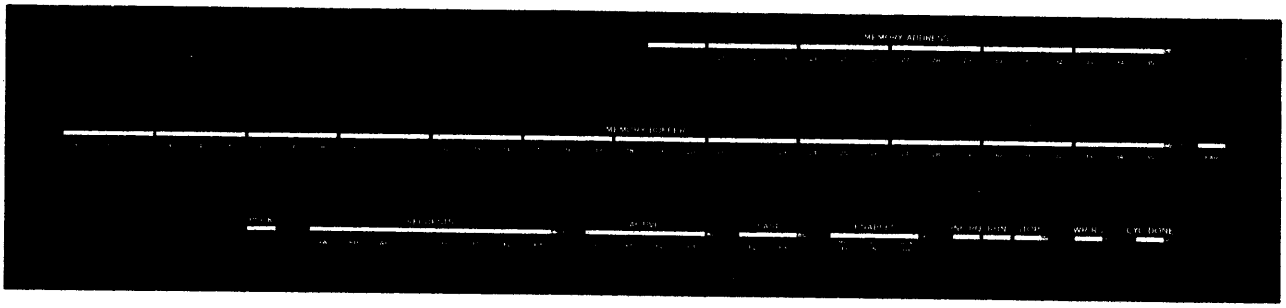


Figure 3-6 Indicator Panel

Table 3-6
Indicator Panel Lamp Functions

Indicator	Function
MEMORY ADDRESS 19–35	Indicates the contents of the Memory Address Register.
MEMORY BUFFER 0–35 and PAR (parity)	Indicates the contents of the Memory Buffer Register.
PSOK	Indicates power is applied to the unit, and regulated voltages are within tolerances.
REQUESTS	
AW	Indicates memory unit is awaiting a processor request for access.
RD	Indicates a read request is being processed, or was the last memory cycle processed.
WR	Indicates a write request is being processed, or was the last memory cycle processed.
P0–P3	Indicates which processor port(s) is requesting access.
ACTIVE P0–P3	Indicates which port request is being processed.
LAST P2–P3	Indicates which port (considering only P2 and P3) was last granted access.
ENABLES	
MB SEL	Indicates the active port memory bus receivers are enabled to receive data from the processor.
DATA IN	Indicates the data transfer from the Memory Buffer to the data latches is enabled.
DATA OUT	Indicates the bus DR (drivers on G113 module) are enabled to transmit the data from the data latches to the bus transmitters.
INC RQ	Indicates the write operation failed to start in a time frame of 20 μs from the start of the memory cycle.
RUN	The memory unit is performing a memory cycle.
STOP	Indicates the detection of an error while in the error stop mode.
WR RS	Indicates the Write Restart signal was received from the processor.
CYC DONE	Indicates the completion of the memory cycle.

CHAPTER 4
PRINCIPLES OF OPERATION

4.1 INTRODUCTION

A block diagram of the MF10 is shown in Figure 1-7, and circuit and timing diagrams are interspersed throughout the chapter. Engineering drawings are also referenced where applicable.

Note that the mnemonic prefix portion of signal names shown on the illustrations indicate the signal source. For example, the MC1 CYC DONE (1) signal is generated by the Memory Control 1 logic, drawing D-BS-MF10-0-MC1.

4.2 INITIAL CONDITIONS

Applying power to the MF10 initializes the system and places it in the idle state, ready to respond to access requests from a processor (refer to drawing D-FD-MF10-0-PDF for a flow diagram of the power up/down and initialize sequences). When power is applied, the CI PSOK signal is asserted, which enables the memory buffers and a 200 ms one-shot multivibrator. Approximately 200 ms later, MC1 START is asserted, which clears the MC1 STOP and PC1 INC RQ flip-flops and generates MC1 RESET. MC1 RESET generates MC1 STATE CLR and CI INITIALIZE. The MC1 STATE CLR signal clears the Port Address Select, Port Control, and Memory Control flip-flops; CI INITIALIZE clears the M7112 Control Logic flip-flops. Approximately 140 ns later, the MC1 STOP flip-flop is examined. If it remains cleared (indicating conditions are go), PC1 SET CYC DONE is asserted; this sets the PC1 AW RQ (Port Control 1 Await Request) flip-flops, and after a variable delay, sets the MC1 CYC DONE flip-flop. The memory is now ready to accept access requests.

4.3 REQUEST/ACKNOWLEDGE

Basic request/acknowledge circuitry must be capable of recognizing an access request from a processor and acknowledging that request when the memory is free to service it. However, the MF10 request/acknowledge circuitry is required to perform tasks in addition to the basic request/acknowledge tasks. Because the MF10 is required to service four separate processors on a timesharing basis, the request/acknowledge circuitry must include a priority network to handle simultaneous access requests. In the event two or more simultaneous requests occur, the priority network allows access to the processor having highest priority. The Request and Port Flow Diagram (drawing D-FD-MF10-0-RPP) illustrates the priority scheme and the sequential operation of the request/acknowledge circuitry. The following paragraphs explain the request/acknowledge sequence with reference to the flow diagram.

4.3.1 Single Access Request

Assuming the memory is in the idle state as explained in Paragraph 4.2, the sequence is initiated when a processor generates a memory address which matches the address of the port to which it is connected. (The port address is established by the memory address switch panel toggle switches.) When this happens, one of the Pn RQ CYC signals goes true and is ANDed with the PC1 AW RQ (1) to set a PAS (Port Address Select) flip-flop. The PAS flip-flop output is ANDed with MC1 CYC DONE (1) to reset the PC1 AW REQ flip-flop and generate the PC1 MA CLR (Port Core 1 Memory Address Clear) pulse. As long as the PC1 AW RQ flip-flop is reset, subsequent processor requests are ignored. The PC1 MA CLR pulse clears the Memory Address and Memory Buffer Registers and the CI WR RS DISPLAY (Core Interface Write Restart Display) flip-flop. The registers are now ready to receive the current memory address and data. After a time delay of 60 ns, PC1 ACT STRB (Port Control 1 Acknowledge Strobe) clears the MC1 CYC DONE flip-flop and is ANDed with the PAS flip-flop outputs (PC1 Pn RQ) in the priority network to generate the Port 0, 1, 2, or 3 Memory Address Strobe (PC1 Pn MA STRB) which loads the address into the Memory Address Register and initiates the memory operation. The priority network also sets the proper Port Acknowledge flip-flop (PC1 Pn ACT). The Port Acknowledge flip-flop output is used to generate the Port Control 2 Port 0, 1, 2, or 3 Address Acknowledge Signal (PC2 Pn ADR ACK) which notifies the processor that its request is granted.

NOTE

The G726-YA Address Acknowledge, Data Warning, and Request Cycle jumper module configurations are determined by the relative speeds of the memories on the bus. Refer to Paragraph 6.5 (Memory Control) in the *KI10 Central Processor Maintenance Manual* for an explanation of memory cycle overlapping.

Finally, 60 ns later, the PC1 LAST STRB is ANDed with PC1 P2 ACT (1) or PC1 P3 ACT (1) (if either is true) to set or reset the PC1 P2/P3 LAST flip-flop, thus completing the request/acknowledge sequence. The P2/P3 LAST flip-flop determines which port has third priority (P2 or P3) during subsequent memory cycles.

4.3.2 Simultaneous Access Requests

Simultaneous access requests dictate the need for a priority scheme. If two or more requests are received by the MF10 simultaneously, the priority network enables the port having the highest priority. The priority scheme is as defined by the logic expressions on the flow diagram:

Priority	Port
First	P0
Second	P1
Third	P2 and P3 (shared)

Third priority is shared between ports P2 and P3 such that if P2 were serviced last in the previous memory cycles, then P3 would be given priority over P2 should simultaneous requests occur on those ports.

4.4 MEMORY CYCLE TIMING

As previously stated (Paragraph 1.5), data may be read from memory and sent to a processor (read/restore cycle); data may be transferred from a processor and written into memory (clear/write cycle); or data may be read from memory, sent to a processor, modified by the processor, returned to the memory and written into the memory at the same location from which it was originally read (read/modify/write). The following paragraphs discuss memory cycle timing.

The basic operations of memory cycle timing, the read operation and the write operation, are common to the three memory cycles. Figure 4-1 illustrates the data path of information written into and read from memory (drawing D-FD-MF10-0-MCF). Note that times stated in the following paragraphs are approximate.

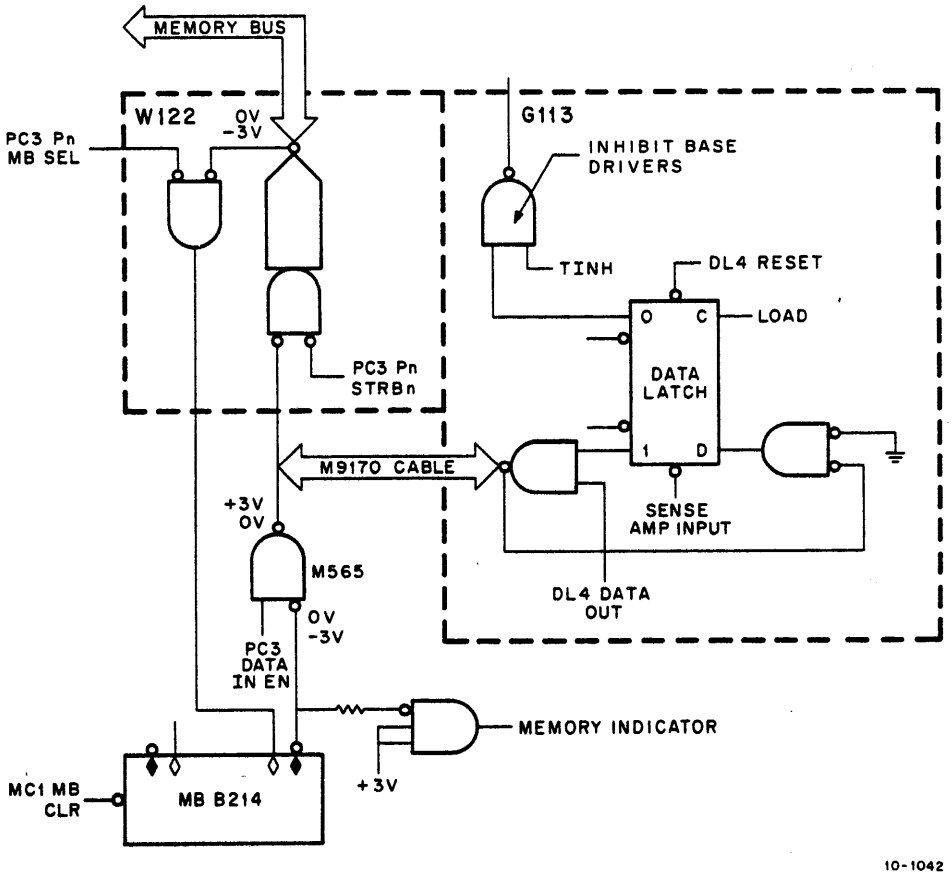


Figure 4-1 Data Path Diagram

4.4.1 Read Timing

Read timing begins when CI INITIATE is true, 60 ns after PC1 Pn MA STRB (drawings D-FD-MF10-0-MCF and D-CS-M7112-0-1). The M7112 Control Logic module associated with the selected memory bank (Paragraph 4.5.3.1) generates the read timing sequence for that specific bank.

CI INITIATE, CI BANK SELECT nR/L, CIC DC LO, and MEM BUSY (0) L are ANDed to generate RESET, which clears the data latches, sets the Read and Delay flip-flops, generates CLK (Clock Pulse) to load the memory address into the memory address latches, and initiates the DL1 multi-tapped delay line timing by sending a high-to-low transition down the delay line. CLK also loads the C00 and C01 flip-flops which determines the type of memory cycle to be performed (Table 4-1). The high DL1, pin 8 output, ANDed with DELAY (1) H, latches the DL1, pin 8 output back to the DL1, pin 1 input, holding the input low for a total of 195 ns. DL1, pin 2 goes low 25 ns after the input, initiating the generation of TNAR (Time Narrow) and TWID (Time Wide). These timing signals cause the proper read drivers/switches and current generators to turn on. Also, TNAR sets the MEM BUSY flip-flop which prevents the regeneration of CLK during the cycle, locks out further requests while the current cycle is in progress, and enables an AND gate which generates BUSY (Busy is the same as CIC BUSY L/R). Pin 6 of DL1 remains low for 125 ns after the input pin 1 goes high; this extends TNAR to 290 ns. In the same manner, pin 8 of DL1 remains low for 175 ns after input pin 1 goes high, extending TWID to 340 ns. Also, DL1, pin 8 going low clears the Delay flip-flop, which prevents DL1 pin 1 from going low when the 175 ns tap times out.

Table 4-1
Memory Cycle Type Coding

Memory Cycle Type	State of C00	State of C01
Read/Restore	0	0
Clear/Write	0	1
Read/Modify/Write	1	0

The data is sensed during TWID/TNAR times and strobed into the data latches at strobe time. (The exception is during a clear/write cycle. Strobe Enable is not generated because C01 (0) H is false, disabling the STRB EN AND gate. The data will not be strobed from the sense amplifiers.) TNAR is delayed 35 ns and ANDed with STRB EN to trigger the 74121 Monostable Multivibrator (drawing D-CS-G113-0-1) and a negative-going pulse is generated on pin 1. The trailing edge of the pulse occurs approximately 300 ns after CI INITIATE. When the trailing edge occurs, the DL4 STROBE AND gates (E11) are enabled for 30 ns, thus generating the 30 ns DL4 STROBE 1 H/0 H. STROBE 1 H/0 H samples the amplified core output and causes the corresponding Data Latch flip-flop to be set. PC3 DATA OUT EN (1) H becomes true 200 ns after CI INITIATE to enable the bus drivers (BUS DRS) on the G113 board. Each bus driver activates immediately with a 1 bit in the respective data latch, allowing the data to pass from the memory bank, through the core interface cable to the memory bus transmitters. TWID going low is inverted to clock the Read flip-flop to the 0 state (the data input pin 12 is tied to ground), ending the read portion of the cycle.

PC3 STRB (L) becomes true 315 ns after CI INITIATE to set PC3 MB SEL. PC3 STRB is ANDed with PC1 Pn ACT (1) to generate PC3 Pn STRB 1, 2, 3, which strobes the proper port to send the data to the processor. Also, PC3 MB SEL (1) L is ANDed with PC1 Pn ACT (1) to generate PC3 Pn MB SEL 1, 2, 3, 4, which gates the proper memory bus data transmitter output into the Memory Buffer to display the contents on the indicator panel.

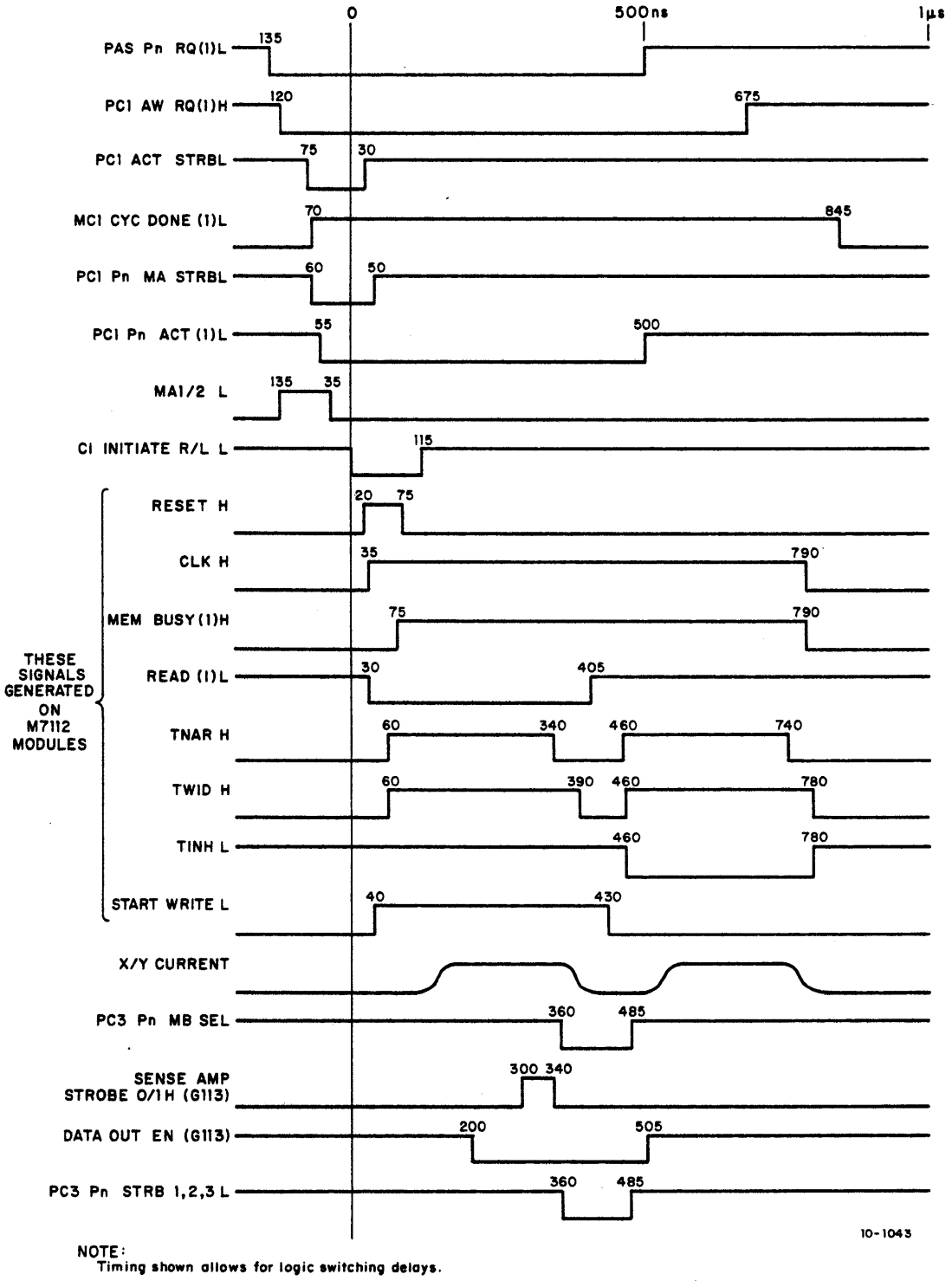
4.4.2 Write Timing

A read operation is always performed before a write operation. At the end of a read operation, READ (1) H becomes false to AND with WR STRB (1) L (if a clear/write or a read/modify/write is being performed), or READ/RESTORE CYCLE (if a read/restore is being performed). The WR STRB flip-flop is set by the WR RS signal generated by the processor to initiate the write portion of a clear/write or clear/modify/write memory cycle. The output of the AND gate clocks the DELAY flip-flop to the 1 state [the data input pin 2 is tied to DELAY (1) L] and causes the generation of START WRITE (START WRITE is the same as CIC START OF WRITE L/R). DELAY (1) H, becoming true, is ANDed with the DL1 output pin 8, which is high, to restart the DL1 timing. TNAR and TWID are generated in the same manner as in a read operation. TWID, RESET (L) inverted, and READ (0) H (READ=WRITE) are ANDed to generate TINH (L), allowing the proper inhibit drivers to operate.

In the CI logic, CIC START OF WRITE goes low and is ANDed with CIC BUSY L/R to complete the CI START OF WRITE input gating. This pulse causes the generation of MC1 STATE CLR which sets PC1 AW RQ after a delay of 140 ns. The MF10 may now accept the next request.

4.4.3 Read/Restore Cycle Timing

During a read/restore cycle (Figure 4-2), the data sensed from the cores are strobed into the data latches and gated by DL4 DATA OUT to the memory bus transmitters. PC3 Pn STRBn enables the data to be transmitted through the proper port to the processor. At the same time, the PC3 Pn MB SELn transfers the data into the Memory Buffer for display. The data still retained in the data latches is then rewritten into the same memory location.



NOTE:
Timing shown allows for logic switching delays.

Figure 4-2 Read/Restore Timing Chart

4.4.4 Clear/Write Timing

During a clear/write cycle (Figure 4-3), a read operation is first performed; however, the data is lost because C01 (0) is false disabling the STRB EN gate and the data is not strobed from the sense amplifiers. CI INITIATE ANDed with MA2 RD RQ (0) sets PC3 DATA IN EN and PC3 MB SEL. PC3 Pn MB SELn enables the Memory Buffer receivers for the proper ports to receive the data from the processor.

The data is received from the processor (along with WR RS) and loaded into the Memory Buffer for display on the indicator panel. PC3 DATA IN EN allows the data to be transferred from the Memory Buffer through the M9170 Core Interface Cables to the data latches in the CMC section. CI WR RS causes WR STRB to start the write operation, and generates DL4 LOAD 0 H/1 H to clock the data into the latches. The data word is then written into the addressed memory location.

4.4.5 Read/Modify/Write Timing

During a read/modify/write cycle (Figure 4-4), the read operation is first performed. The data read is then sent to the processor for modification and the Memory Buffer is cleared. The memory then pauses (20 μs maximum) to await the return of the modified data.

During the read operation, PC3 STRB sets PC3 MB SEL (remains set until MC1 STATE CLR), and the AND of MA2 WR RQ (1) and PC3 DATA OUT EN CLR sets PC3 DATA IN EN (also remains set until MC1 STATE CLR). When the modified data is sent from the processor along with WR RS, a write operation is performed as in a clear/write cycle.

4.5 DETAILED MEMORY DESCRIPTION

4.5.1 Core Array

The 8K, ferrite core, memory module consists of 19 memory mats arranged in a planar configuration. Each mat contains 8192 ferrite cores arranged in a 128 X 64 array. Each mat represents a single bit position of a word. This planar configuration provides a total of 8192 19-bit half-word locations. Each ferrite core can assume a stable magnetic state corresponding to either a binary 1 or binary 0. When power is removed from the core, the core retains its state until changed by appropriate control signals. The outside diameter of each core is 18 mil; the inside diameter is approximately 11 mil. Each core is 4.5 mil thick.

The memory uses a 3-wire core selection technique (Figure 4-5). An X axis read/write line passes through all cores in each horizontal row for all 19 mats. A Y axis read/write line passes through all cores in each vertical row for all 19 mats. Through the use of selection circuits, which control the current applied to a specific X-Y line, any one of the 8192 word locations can be addressed for writing data into memory or reading data out of memory. A third line passes through each core on a mat to provide the sense inhibit functions. There is one sense inhibit line per mat. This single sense inhibit line, as well as the selection circuits, are discussed in subsequent paragraphs.

4.5.2 Memory Operation

The H216 Memory Stack is a standard 3D, 3-wire, coincident current, core array (Figure 4-5). The current passing through any one line (X or Y) is one-half that required to change the magnetic state of the core. X1 and Y1 intersect once on each of the 19 mats, thereby producing full current at 19 cores. If the cores are being read, the current direction is such that the 19 cores are forced to the 0 magnetic state (destructive readout); the other 8191 cores on each mat are not affected. When an addressed core containing a 1 is switched to the 0 magnetic state, the resultant flux change is detected by the sense/inhibit line and a logical 1 is generated at the output of the sense amplifier on the G113 module.

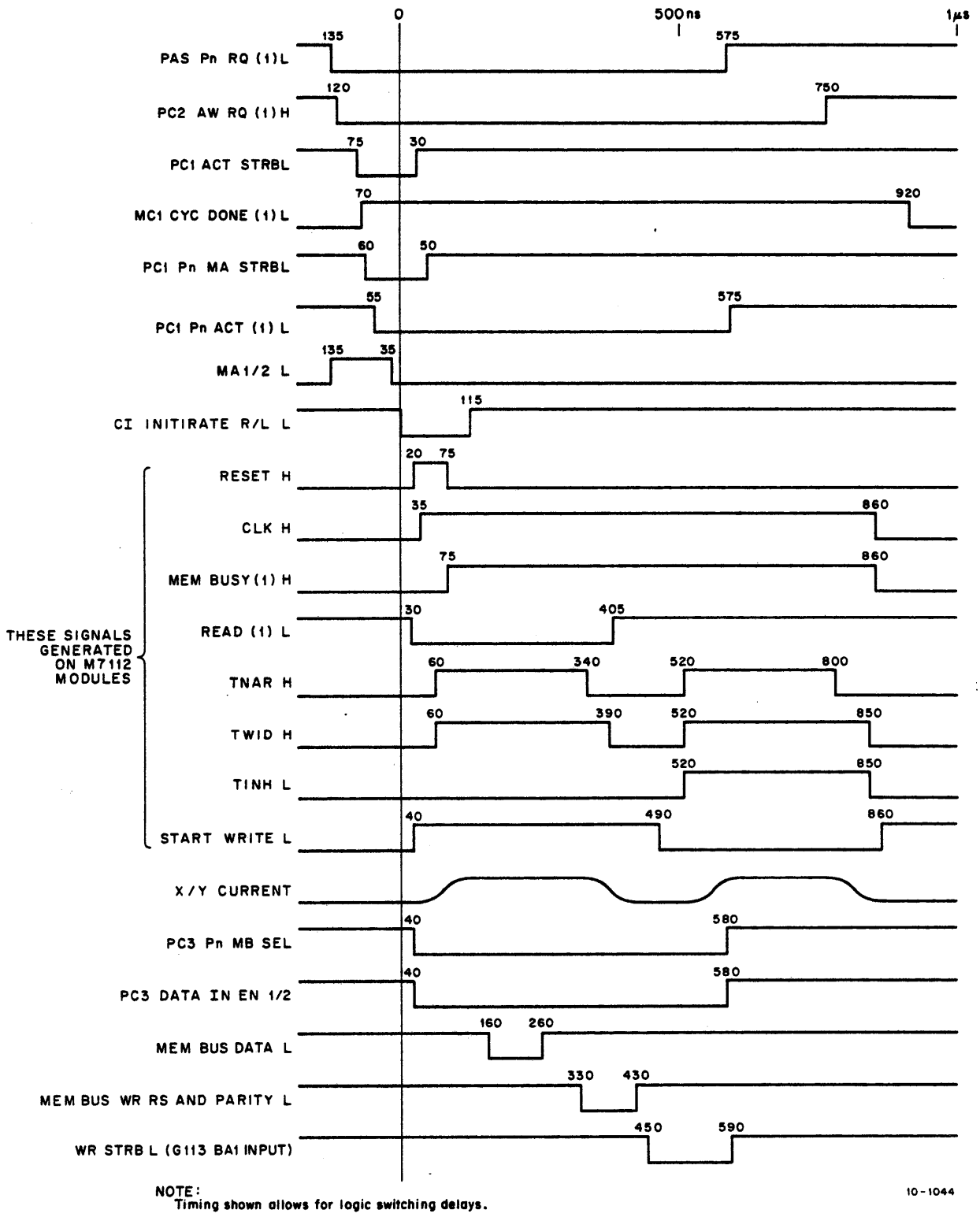
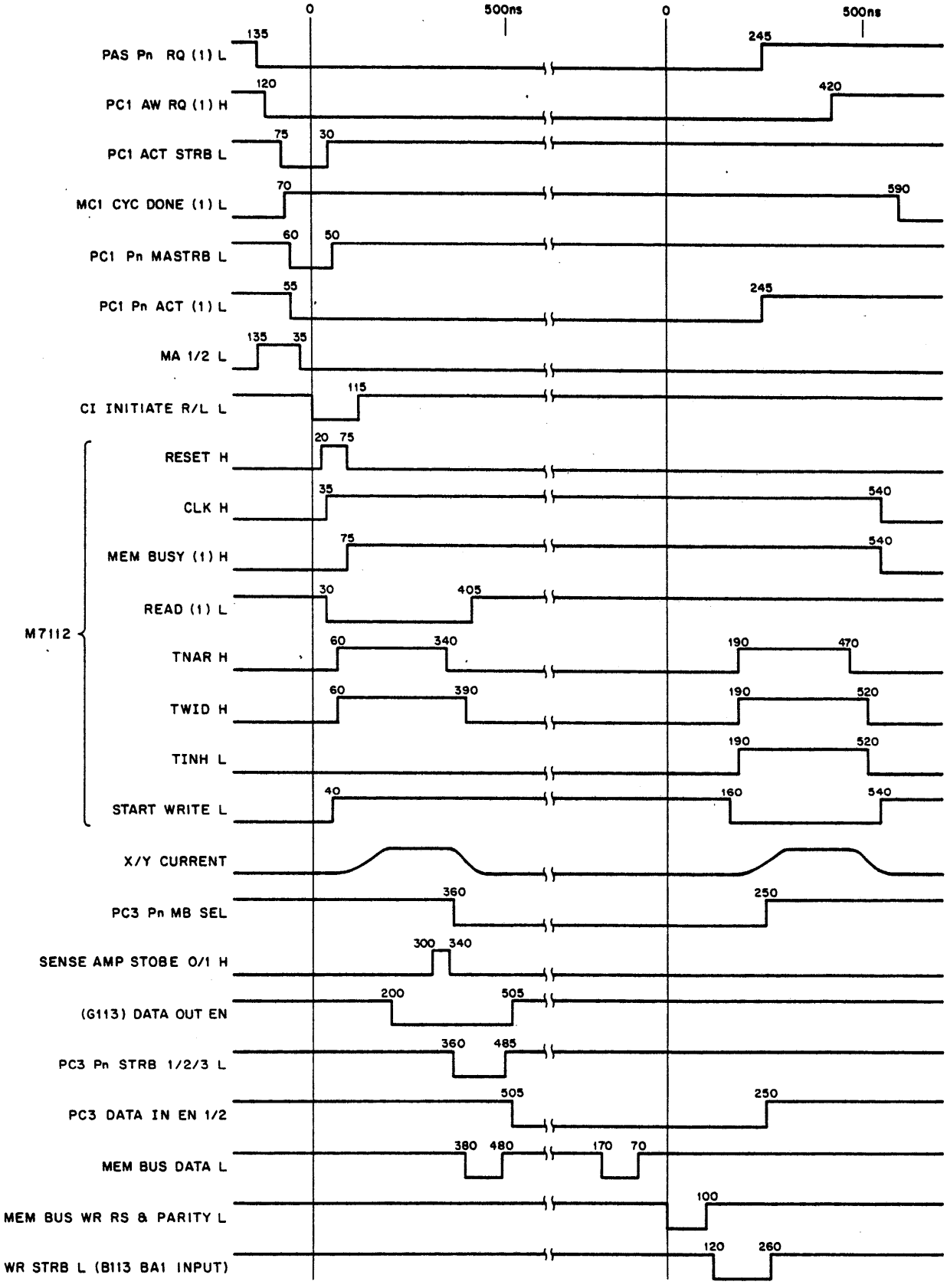


Figure 4-3 Clear/Write Timing Chart



NOTE:
Timing shown allows for logic switching delays.

Figure 4-4 Read/Modify/Write Timing Chart

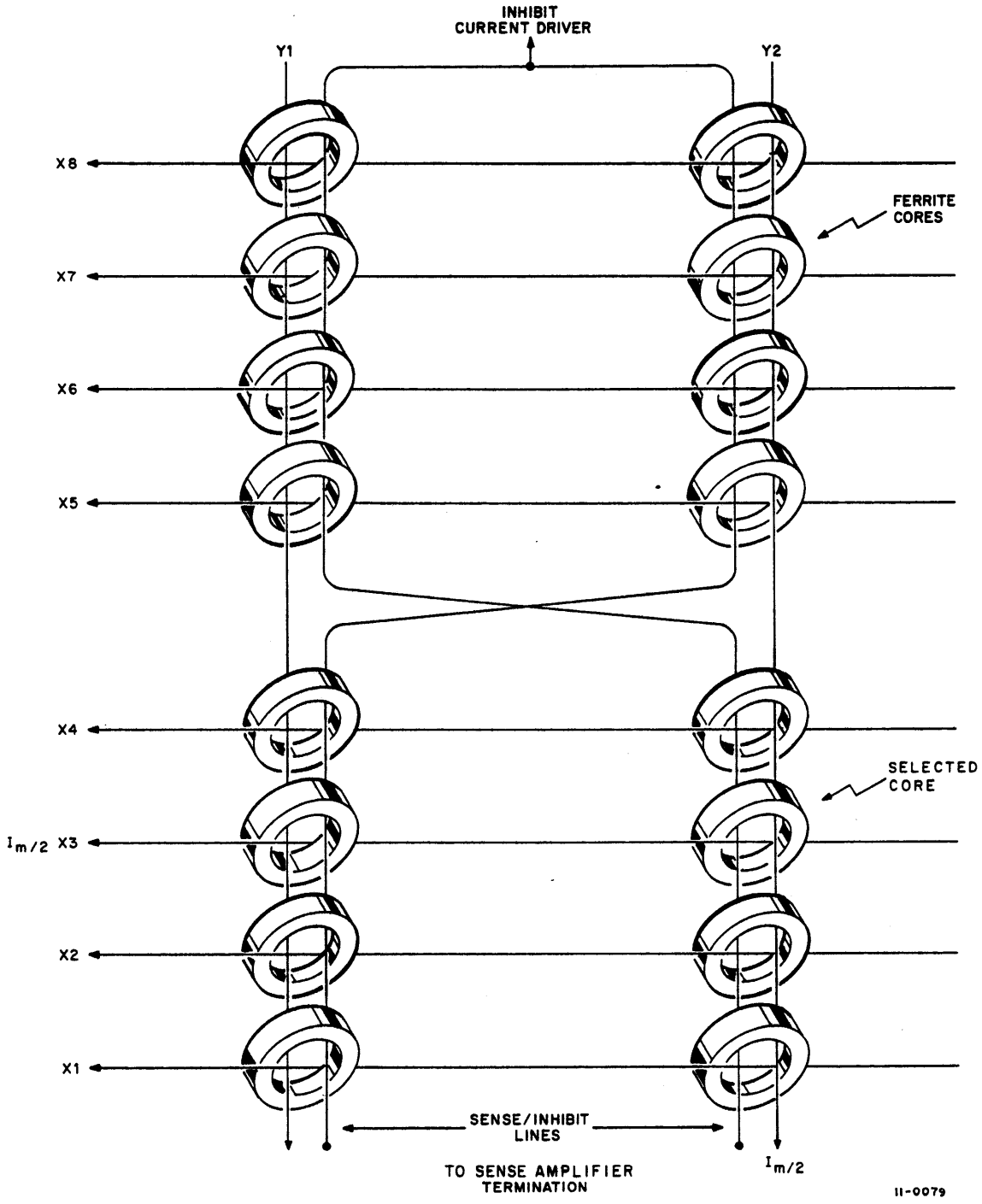


Figure 4-5 Three-Wire Memory Configuration

The memory is accessed in a similar fashion during a write operation except that the current through the X and Y lines is in the opposite direction. All 19 cores are switched to the 1 magnetic state except on those cores having current applied to their sense/inhibit line. This current cancels out the affect of the half-current in the Y line (inhibit current is in the opposite direction of Y write current) and the addressed core remains in the 0 state. For example, when a write operation is performed to complete a read/restore cycle, only those cores containing 1s originally will be forced to the 1 state. All cores containing 0s originally will have current applied to their sense/inhibit line during the restore portion of the cycle. Figure 4-6 shows a 16-word by 4-bit planar memory. The 8K H216 Memory Stack is configured in the same manner, except that it has 128 X lines, 64 Y lines, and 19 core mats. The core stringing is identical, and each of the 19 sense lines are laced through 8192 cores with the interchange between X63 and X64 instead of between X1 and X2.

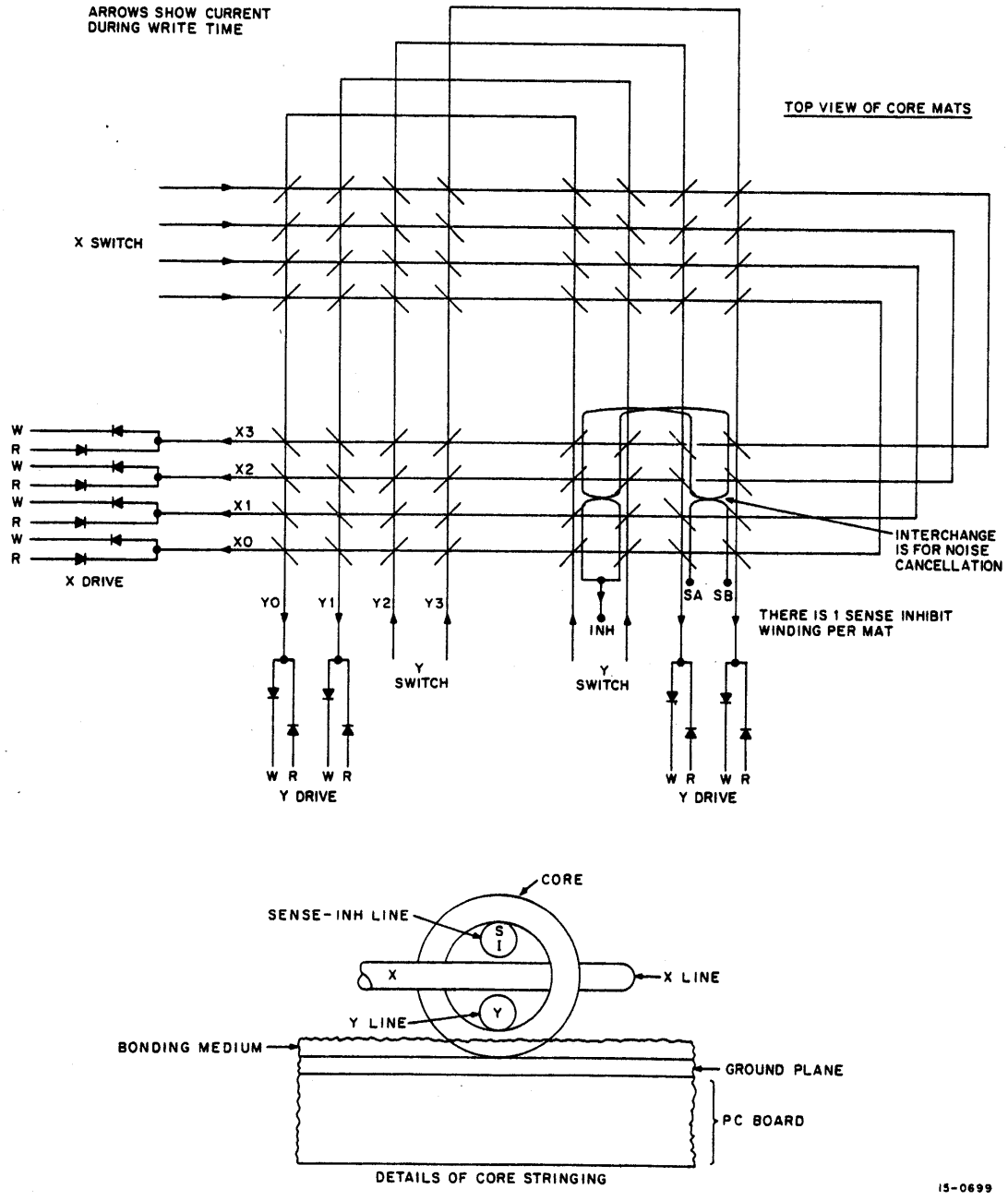


Figure 4-6 Three-Wire 3D, 16-Word by 4-Bit Memory

4.5.3 Memory Addressing

The memory locations of the MF10 are addressed by bits 20–35 of the memory address (Figure 4-7) generated by the processor. These bits are capable of addressing 64K (65,536) locations. One H216 Memory Stack module contains 8K (8192) half-word locations (19 bits). For each 8K full words, two H216 modules are used to store 36 data bits plus one parity bit.

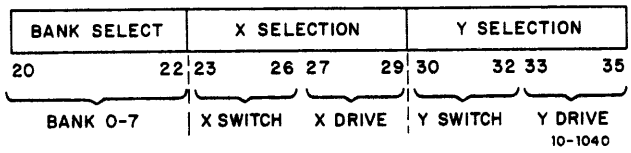


Figure 4-7 Memory Address

4.5.3.1 Memory Bank Selection – The CMC logic section is divided into banks (Figure 1-7). The left banks (looking at the MF10 from the front) store bits 00–17, and the right banks store bits 18–35 plus the parity bit. There may be either 4 or 8 bank pairs or 32K/64K addressable word locations. Although the left and right banks are selected and initialized simultaneously by the same memory address bits (20–22) for each memory cycle, they operate independently of each other to determine the data word location, both using the same memory address bits (23–35). Memory address bits 20–22 are decoded in the Core Interface logic to select the proper 8K data word bank pair (0–7). Memory bank decoding is shown in Table 4-2.

Table 4-2
Memory Bank Selection Decoding

Decimal Addresses	Bank Pair	Addresses Contained (Octal)	Memory Address Bits		
			20	21	22
0–8K	0	000000 – 017777	0	0	0
8–16K	1	020000 – 037777	0	0	1
16–24K	2	040000 – 057777	0	1	0
24–32K	3	060000 – 077777	0	1	1
32–40K	4	100000 – 117777	1	0	0
40–48K	5	120000 – 137777	1	0	1
48–56K	6	140000 – 157777	1	1	0
56–64K	7	160000 – 177777	1	1	1

4.5.3.2 Data Word Selection – Data word selection requires two levels of decoding. Memory address bits 23–35 are placed in the memory address latches (MAL) A13–A01, respectively. MAL outputs are combined in a gating network. The gating network outputs, and outputs directly from the MAL are used as inputs to a group of decoders. The outputs of the decoders select the proper X and Y read/write switches and drivers.

4.5.3.2.1 Memory Address Latches and Gating Logic – The latches and gating logic are contained on the G231 Memory Driver module (drawing D-CS-231-0-1, sheet 2). The MAL consists of 13 dual 74H74 D-type edge-triggered flip-flops identified as E11, E12, E13, E14, E18, E19, and E20. Gate E9 provides high signals to the preset and reset inputs of each flip-flop which prevents direct presetting or clearing. Since the latches cannot be directly cleared or preset, their outputs are affected only by the signal at the data (D) input.

The MAL flip-flops are clocked synchronously. Clocking occurs on the positive-going edge of CLK (1) H input from the M7112 Control Logic. When the MAL is clocked, the outputs of flip-flops A01, A02, A04, A05, A07, A08, A10, and A11 are sent to the type 8251 X/Y line decoders on the driver module (drawing G231-0-1, sheets 3 and 4). The outputs of flip-flops A06, A12, and A13 are combined in a group of six type 74H10 NAND gates which are enabled by signal TSS H. Table 4-3 lists the states of flip-flops A06, A12, and A13 that are required to enable these gates. The outputs of flip-flops A03 and A09 are gated with TDR H in high speed, 2-input NAND gates and then applied to the decoders associated with the drivers. The six signals listed in Table 4-3 are also sent to the X/Y line decoders on the driver module.

Table 4-3
Enabling Signals for Word Register Gating

MAL Gate	Enabling Inputs			Asserted Output
	FFA06	FFA12	FFA13	
E22 pin 12	1	X	X	MD2YS1L
E22 pin 8	0	X	X	MD2YS0L
E22 pin 6	X	1	1	MD2XS3L
E25 pin 12	X	0	1	MD2XS2L
E25 pin 8	X	1	0	MD2XS1L
E25 pin 6	X	0	0	MD2XS0L

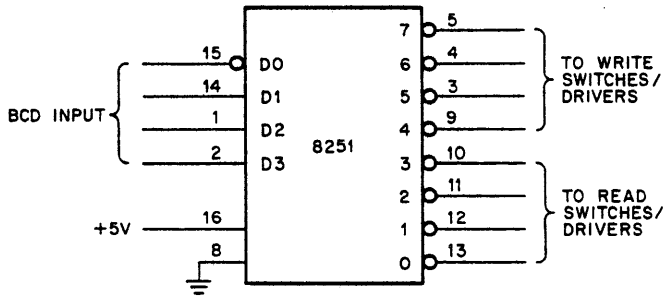
X = Irrelevant

Signal TSS H (drawing D-CS-G231-0-1) is generated during a read or write operation. During a read operation, the enabling signal is produced by ANDing READ H and TNAR H. During a write operation, the enabling signal is produced by ANDing WRITE H and TWID H. READ, TNAR, and TWID are generated by the control logic on the M7112 module. WRITE is the complement of READ (produced by inverter E6).

4.5.3.2.2 **X and Y Line Decoding** – The basic decoding unit is a type 8251 BCD-to-Decimal Decoder. It converts a 4-bit BCD input code to a one-of-ten output; however, only eight outputs are used. Figure 4-8 shows an 8251 and associated truth table. The inputs are D0, D1, D2, and D3; they are weighted 1, 2, 4, and 8, with D0 being the least significant bit. The outputs are 0–7 and are mutually exclusive. The selected output is low and all others are high.

The decoders are required for each 8K memory bank (drawing D-CS-G231-0-1, sheets 3 and 4). There are six X axis decoders and four Y axis decoders. Each decoder controls four read/write switch pairs or four read/write driver pairs. This switch/driver matrix is combined with the stack X/Y diode matrix to allow selection of any location out of the total 8192 locations (drawing D-CS-H216-0-1). The X and Y line switches are first differentiated as switches and drivers: the drivers are connected to the diode end of the stack. Drivers and switches are further differentiated by function: either read or write. Another differentiation is made by polarity: negative or positive, depending on the physical connection. Read drivers and write switches are connected to the current generator outputs and are considered positive; write drivers and read switches are connected to -15 V and are considered negative.

Figure 4-9 shows the decoders associated with Y line read and write switches 4–7 and Y line read and write drivers 4–7. In both decoders (E28 for switches and E8 for drivers), the signal to input D3 must be low for any output to be selected. The signal to input D2, which is READ L for all decoders, controls the selection of read or write switches/drivers. When READ L is low, outputs 0–3 are selected; these are read switches and read drivers. When READ L is high, outputs 4–7 are selected; these are write switches and write drivers. The four combinations of the states of inputs D0 and D1 select the particular switch/driver.



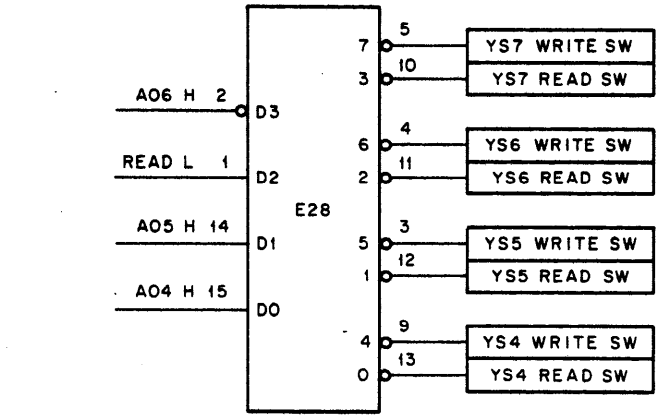
TRUTH TABLE

INPUTS				OUTPUTS							
D3	D2	D1	DO	0	1	2	3	4	5	6	7
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	X	X	X	1	1	1	1	1	1	1	1

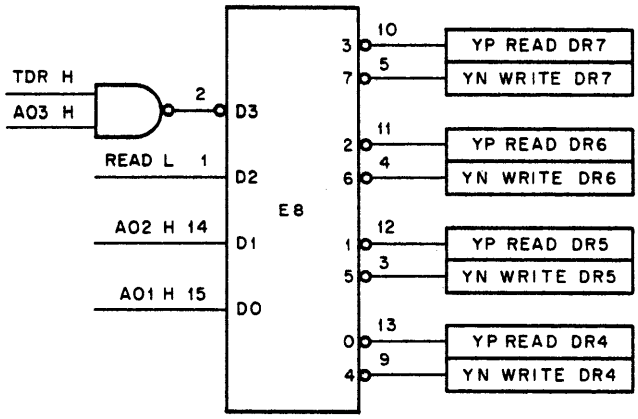
X = IRRELEVANT

11-1095

Figure 4-8 Type 8251 Decoder, Pin Designation and Truth Table



DECODER FOR READ AND WRITE SWITCHES YS4 - YS7



DECODER FOR READ AND WRITE DRIVERS Y4 - Y7

11-1096

Figure 4-9 Decoding of Read/Write Switches and Drivers Y4–Y7

The four driver decoders, E3, E8, E43, and E46 (drawing D-CS-G231-0-1, sheets 3 and 4), have a NAND gate connected to input D3. Signal TDR H is an input to each gate; therefore, the driver decoders cannot be enabled unless TDR H is high. This signal is generated on the driver module (drawing D-CS-G231-0-1, sheet 2, coordinates A-8) by ANDing TWID H and READ H, or TNAR H and WRITE H.

Each switch/driver is connected to the decoder output by a transformer-coupled base drive circuit. When the decoder output is at ground (low), the switch/driver is turned on; it is turned off when the decoder output is at +3.5 V (high). See Table 4-4 for memory address to driver/switch decoding.

NOTE

When referring to Table 4-4, note that memory address bit 23 is registered in address latch A13, bit 24 in A12, etc.

Table 4-4
Memory Address to Driver/Switch Decoding

MA_8 Bits 23–35	Address Latches A13 – A01 (G231 Board)	G231 Decoder	Driver Switch (G231 Board)
XXXX0	XXXX7	E8	YNWD/YPRD 7
XXXX1	XXXX6		YNWD/YPRD 6
XXXX2	XXXX5		YNWD/YDRD 5
XXXX3	XXXX4	E8	YNWD/YDRD 4
XXXX4	XXXX3	E3	YNWD/YDRD 3
XXXX5	XXXX2		YNWD/YDRD 2
XXXX6	XXXX1		YNWD/YDRD 1
XXXX7	XXXX0	E3	YNWD/YDRD 0
XXX0X	XXX7X	E28	YS07
XXX1X	XXX6X		YS06
XXX2X	XXX5X		YS05
XXX3X	XXX4X	E28	YS04
XXX4X	XXX3X	E23	YS03
XXX5X	XXX2X		YS02
XXX6X	XXX1X		YS01
XXX7X	XXX0X	E23	YS00
XX0XX	XX7XX	E46	XNWD/XPRD 7
XX1XX	XX6XX		YNWD/XPRD 6
XX2XX	XX5XX		XNWD/XPRD 5
XX3XX	XX4XX	E46	XNWD/XPRD 4
XX4XX	XX3XX	E43	XNWD/XPRD 3
XX5XX	XX2XX		XNWD/XPRD 2
XX6XX	XX1XX		XNWD/XPRD 1
XX7XX	XX0XX	E43	XNWD/XPRD 0

Table 4-4 (Cont)
Memory Address to Driver/Switch Decoding

MA_8 Bits 23–35	Address Latches A13 – A01 (G231 Board)	G231 Decoder	Driver Switch (G231 Board)
00XXX	17XXX	E40	XS15
01XXX	16XXX		XS14
02XXX	15XXX		XS13
03XXX	14XXX	E40	XS12
04XXX	13XXX	E37	XS11
05XXX	12XXX		XS10
06XXX	11XXX		XS09
07XXX	10XXX	E37	XS08
10XXX	07XXX	E34	XS07
11XXX	06XXX		XS06
12XXX	05XXX		XS05
13XXX	04XXX	E34	XS04
14XXX	03XXX	E31	XS03
15XXX	02XXX		XS02
16XXX	01XXX		XS01
17XXX	00XXX	E31	XS00

A typical base drive circuit for write switch YS7 is shown in Figure 4-10. The decoder inputs have selected output 7, which is at ground. Current i_1 flows into this decoder output circuit from the +5 V supply via resistor R11 and the primary winding (terminals 4 and 3) of transformer T8. The value of i_1 is determined by the value of R11 and the voltage reflected into the transformer primary (approximately 1.0 V). An equal current i_2 is induced in the base-emitter circuit of write switch E29, which is connected to the transformer secondary winding (terminals 13 and 14). This current turns on E29. All the base current for E29 is provided by the base-emitter circuit; i_3 is the collector current. When the decoder is turned off, its output pull-up transistor tries to drive the turn-off current i_4 in the opposite direction. This reverse current removes the forward bias from the base of E29 and turns it off. Capacitor C30 allows the decoder to pump reverse current i_4 into the transformer primary; it also speeds up turn-on current i_1. Diode D1 prevents reverse breakdown of the base-emitter junction of E29 and also protects the decoder output.

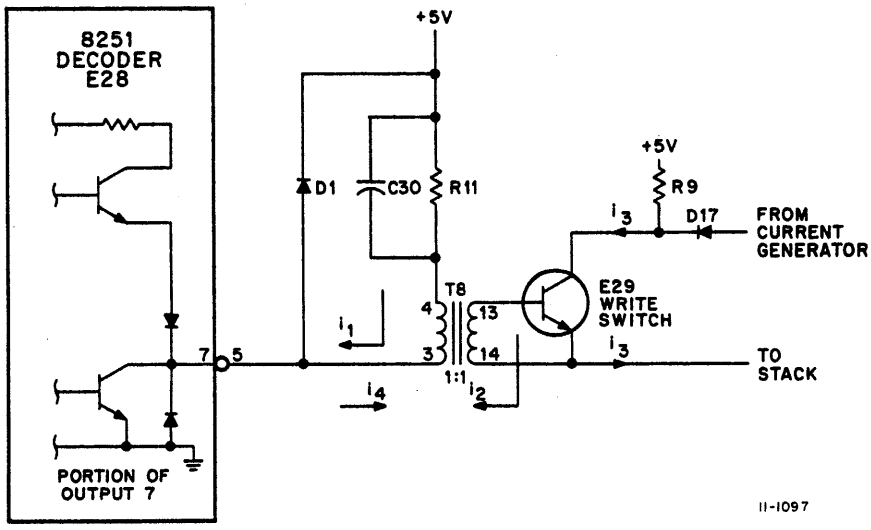


Figure 4-10 Switch or Driver Base Drive Circuit

4.5.3.2.3 Drivers and Switches – Drivers and switches direct the current through the X and Y lines in the proper direction as selected by read and write operations. For each 8K memory bank in the MF10, 16 pairs of read/write switches and 8 pairs of read/write drivers are provided in the X axis; 8 pairs of read/write switches and 8 pairs of read/write drivers are provided in the Y axis. With the stack diode matrix (drawing H216-0-1, sheet 2), 128 lines can be selected in the X axis and 64 lines in the Y axis. Thus, a 128 X 64 matrix is provided that can select any one of 8192 locations.

Figure 4-11 illustrates one-fourth of the Y selection matrix and shows the interconnection of the diodes and the lines from the switches and drivers. Four pairs of drivers and four pairs of switches are shown for the Y axis only; polarities are shown for convenience. The diodes are identified to assist in associating them with the drivers and switches. Each line from a twin diode interconnection to a read/write switch pair passes through 128 cores and represents one line on each bit mat. Assume that a write operation is to be performed and the word address decoders have selected write switch WYS00 and write driver YNWD1. Write switch WYS00 is turned on, resulting in a positive voltage on the anodes of diodes 03W, 02W, 01W, and 00W. The non-selected write drivers (YNWD3, YNWD2, and YNWD0) provide a positive voltage on the cathodes of their associated diodes (03W, 02W, and 00W, respectively) which reverse-biases them and prevents conduction. Write driver YNWD1, which has been selected, turns on and makes the cathode of diode 01W negative with respect to the anode which forward biases it. The diode conducts and allows current to flow from WYS00, through the forward-biased diode and the cores, to YNWD1. A half-select current now flows through this line, linking 128 cores on each bit mat (2432 total for 19 mats).

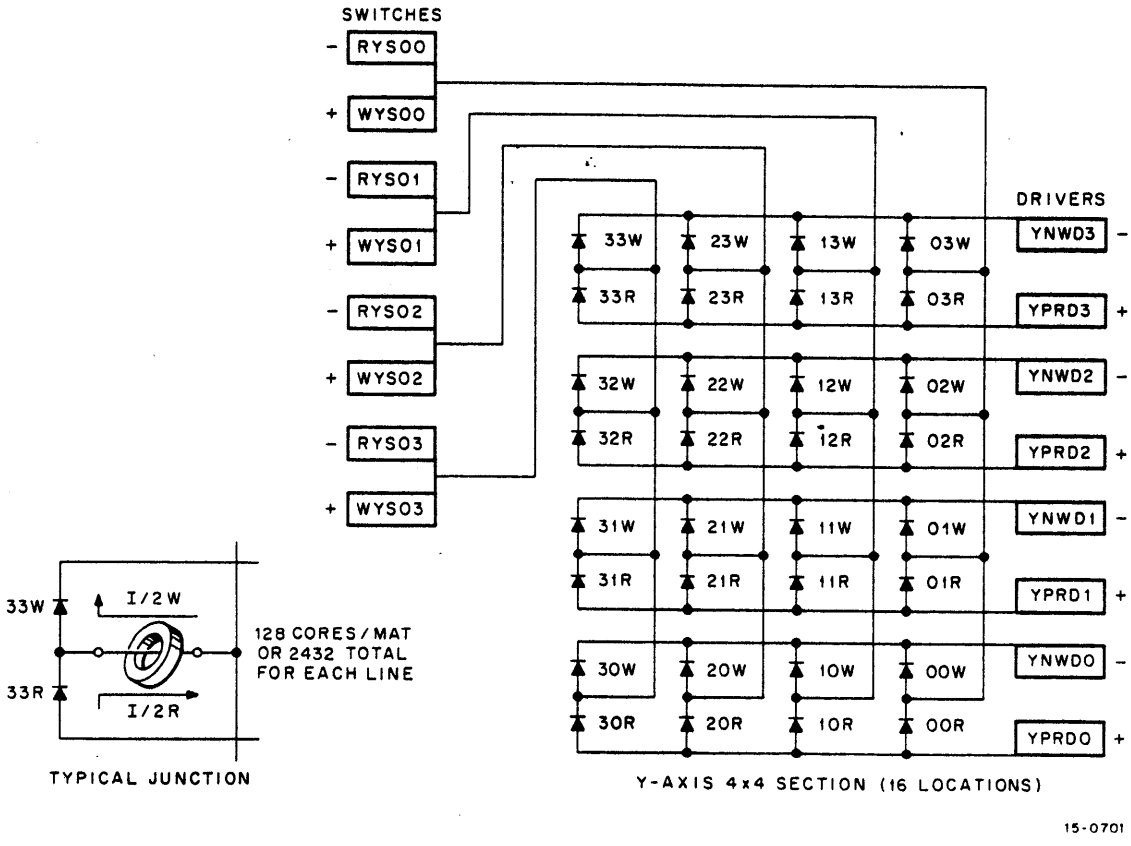


Figure 4-11 Y Line Selection Stack Diode Matrix

Figure 4-12 is a simplified schematic of two pairs of switches and drivers interconnected with the core stack and current generator. Read/write switches YS07 and read/write drivers YD7 are chosen for convenience. For a read or write operation, there are 64 switch/driver combinations available for Y axis and 128 switch/driver combinations for X axis. For a read operation, decoder E8 selects positive read driver E7, and decoder E28 selects negative read switch E26. Both E7 and E26 are turned on when they are selected and current flows as indicated by the solid line. For a write operation, the current flows in the opposite direction. Decoder E28 selects positive write switch E29, and decoder E8 selects negative write driver E10. Both E29 and E10 are turned on and current flows as indicated by the broken line.

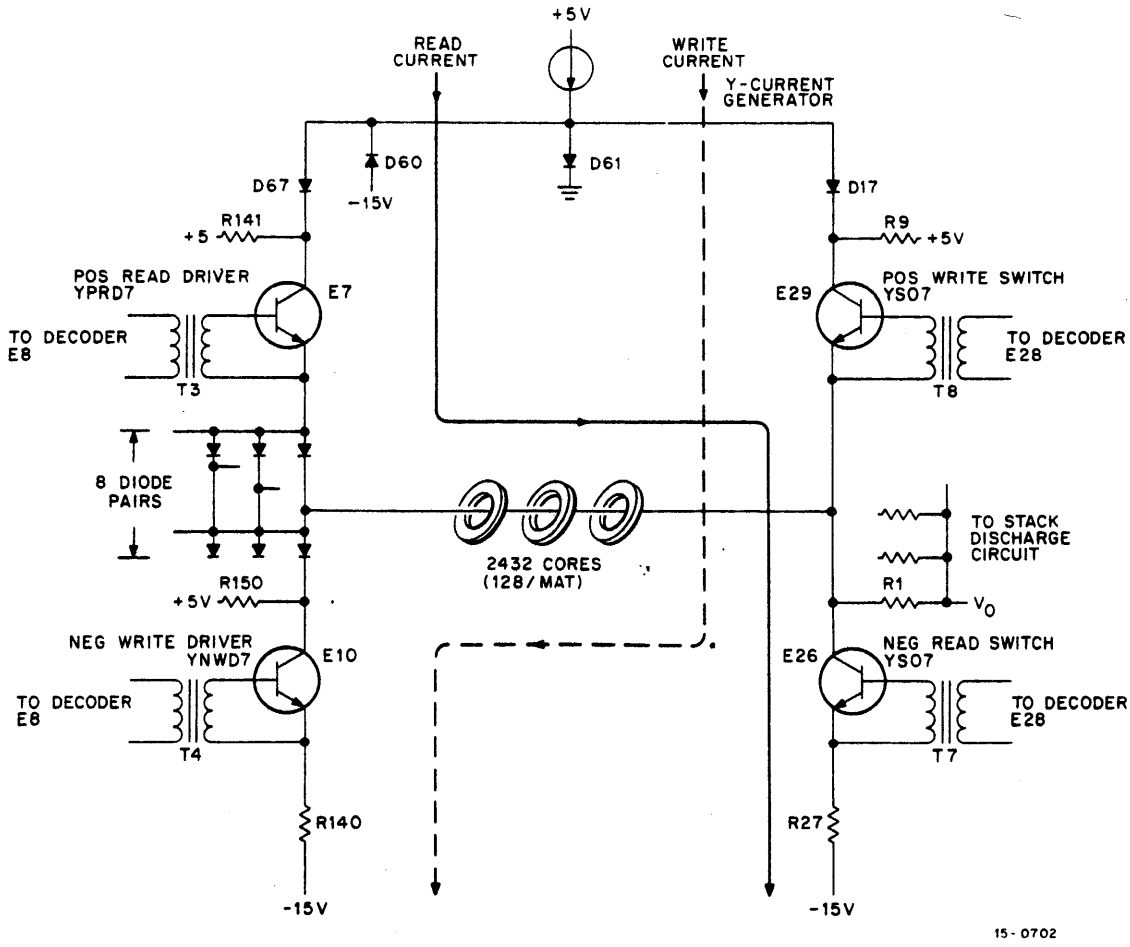


Figure 4-12 Typical Y Line Read/Write Switches and Drivers

4.5.4 Read/Write Current Generation and Sensing

Four functional units are involved in generating current to switch the cores and detect their state. The X and Y line current generators supply the drive current (via switches and drivers); the inhibit drivers allow 0s to be stored during a write operation; the sense amplifiers detect 1s during a read operation; and the memory data latches (MDL) temporarily store data being transferred to and from memory.

During a read operation (Figure 4-13), half-select currents flow in the X and Y lines for the selected core in each bit mat. These currents flow opposite to the write currents; therefore, cores in the 1 state are switched to the 0 state and cores in the 0 state remain unchanged. Assuming bit 7 is a 1 in core, switching the core from the 1 state to the 0 state induces a voltage pulse in the sense winding. This pulse is detected by sense amplifier E36 as a differential voltage on input pins 6 and 7 that exceeds the threshold reference voltage. This pulse is amplified, and when STROBE 0 H is generated at pin 11, the output of sense amplifier E36 goes high. At the beginning of every cycle, the control logic generates RESET 0 which clears flip-flop E38. The sense amplifier output is inverted by E40 and sent to the set input (pin 10) of MDL flip-flop E38. A low on the set input sets the flip-flop; its 1 output (pin 9) is a high and its 0 output (pin 8) is a low. The high from pin 9 of the flip-flop is sent to the input pin 1 of bus driver E4. The other input to this gate is the DATA OUT signal. When the control logic generates DATA OUT H, the output of E4 is low, a logical 1. Timing diagrams for the sense operation are shown in Figure 4-14.

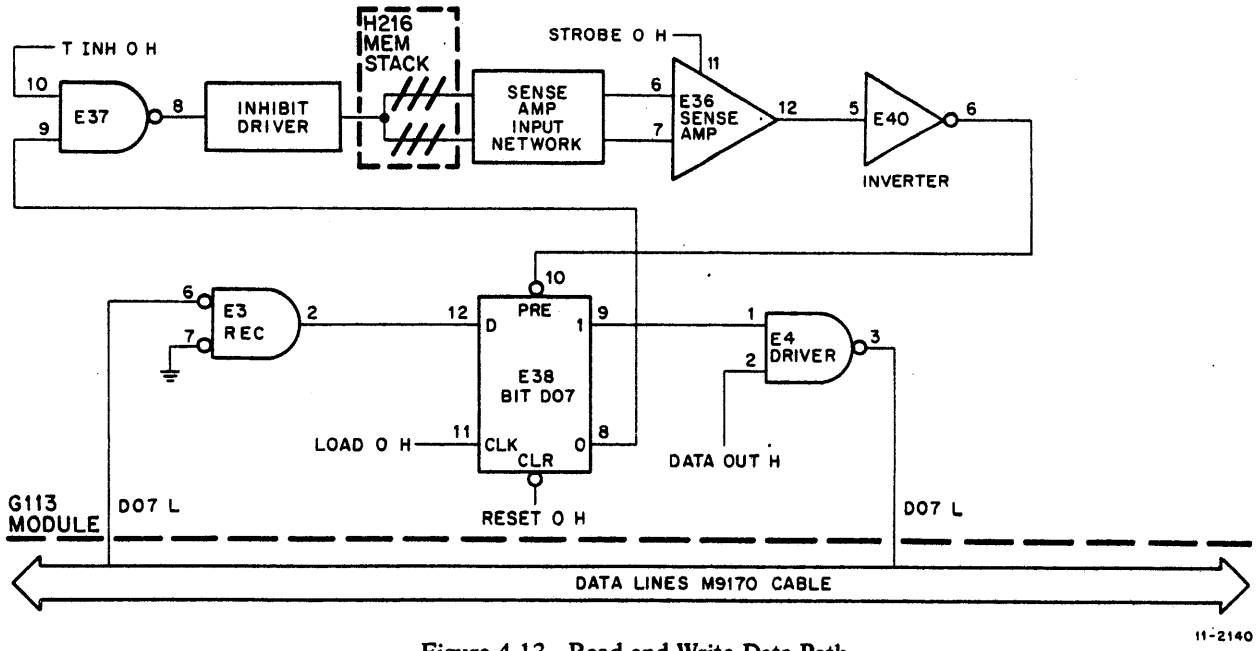


Figure 4-13 Read and Write Data Path

The read operation is destructive; i.e., all cores at the specified location are switched to 0. The 1 bit that was read during the read operation must be restored by a write operation immediately following the read operation. Flip-flop E38 is still in the set state; therefore, its 0 output (pin 8), which is low, is sent to input pin 9 of NAND gate E37. The gate is not asserted (pin 8 is high) and the inhibit driver is not turned on. With no inhibit current in the inhibit line to oppose the half-select Y line current, a 1 is written back into the appropriate core.

However, if bit D07 is 0 in core, it does not switch during the read operation and the output of sense amplifier E36 does not go high. Flip-flop E38 remains cleared; its 1 output (pin 9) is low and its 0 output (pin 8) is high. When the control logic generates DATA OUT H, the output of bus driver E4 is high, a logical 0. The 0 output of flip-flop E38, which is high, is sent to NAND gate E37. During the subsequent write operation, TINH 0 H is generated which produces a low output signal at E37, pin 8. This activates the inhibit driver which produces a current that opposes the Y line current and prevents a 1 from being written into the appropriate core.

The memory operation just described is actually a read/restore operation. The requesting device wants to read a word from memory and, as an internal requirement, the memory must restore the word by writing it back in core. During a read/restore operation, the MDL flip-flops are set by the sense amplifier outputs when 1s are read from core. The flip-flop outputs are then used in the subsequent restore operation to control the inhibit drivers.

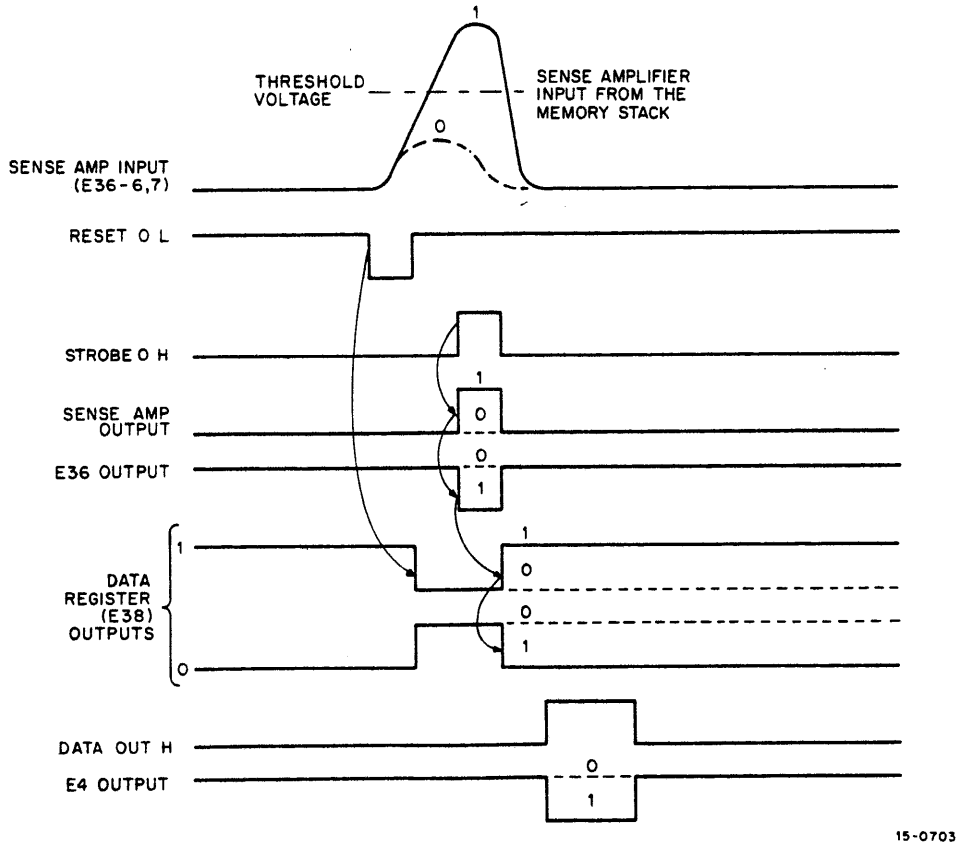


Figure 4-14 Timing Diagram for the Sense Portion of a Read Operation

If the requesting device wants to write a word into memory (clear/write operation), it must load the data into the MDL flip-flops through receiver E3. The bit is inverted by receiver E3 and sent to the D input (pin 12) of flip-flop E38. During the write operation, the control logic generates LOAD 0 H which clocks the flip-flop. If the D input is high, E38 is set, its 0 output goes low, control gate E37 is not asserted by TINH 0 H, the inhibit driver is not turned on, and a 1 is written into the selected core. If the D input is low, E38 is not set, its 0 output is high, control gate E37 is asserted by TINH 0 H, the inhibit driver is turned on, and the selected core remains in the 0 state.

4.5.4.1 X and Y Current Generators – Two identical current generators are provided, one each for the X and Y drive lines. They generate the current pulses that are used during read and write operations to switch the cores. The current generators and associated reference voltage supply are shown in drawing D-CS-G231-0-1, sheet 2. Figure 4-15 shows the Y current generator and reference voltage supply.

Optimum core switching requires repeatable current pulses of constant amplitude with a linear rise time. The current generator and reference voltage circuit provide current pulses that meet these requirements. The amplitude of the output current pulse is determined by the reference voltage circuit; the rise time is determined by an RC circuit in the current generator; and pulse duration is determined by the length of the triggering pulse, TWID H. The amplitude of the current generator output pulse is factory set to approximately 440 mA at 25° C. It should not be adjusted in the field. Temperature compensation is effected by a circuit consisting of a thermistor and a resistor mounted on the stack. This ensures that the amplitude of the current generator output pulse remains within the specified tolerances of 0° C to 50° C. The temperature compensation is approximately -0.8 mA/° C.

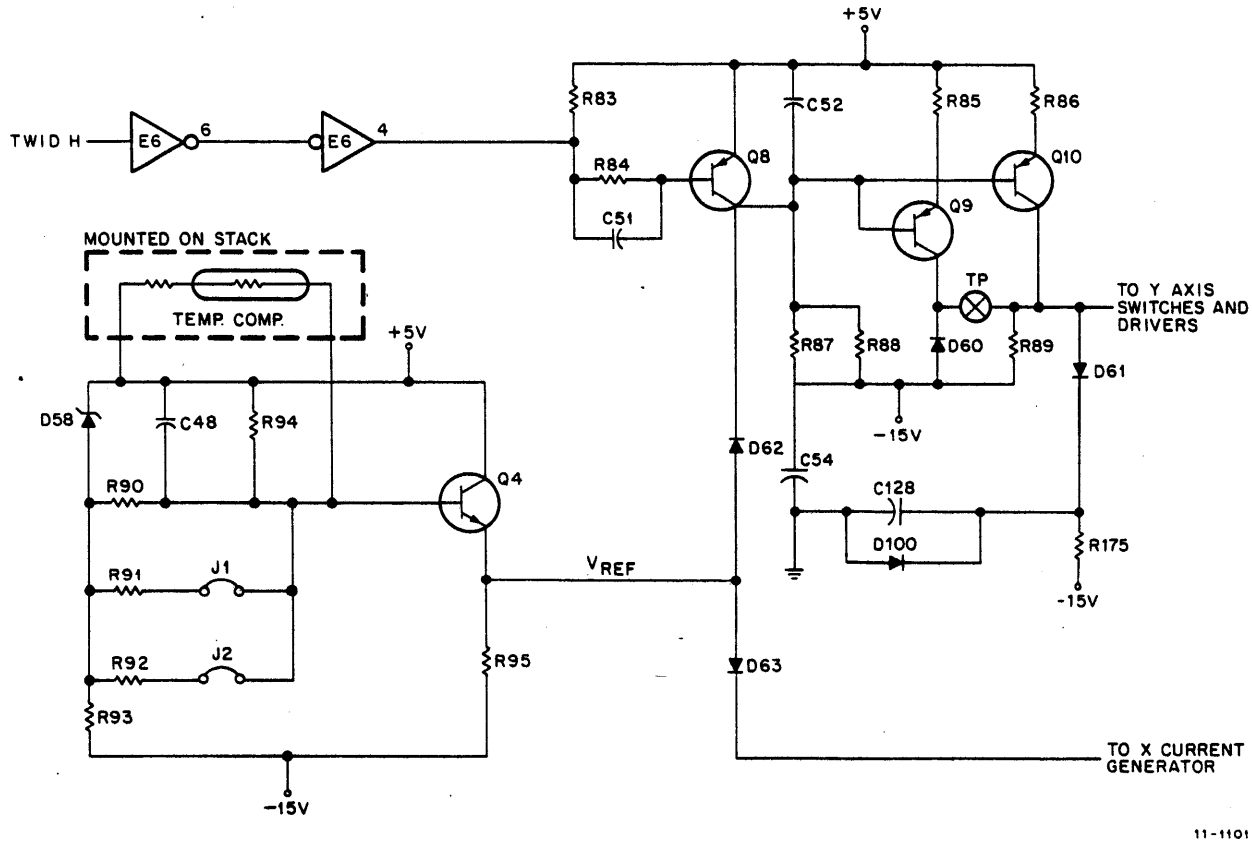


Figure 4-15 Y Current Generator and Reference Voltage Supply

4.5.4.2 **Inhibit Driver** – As previously stated, the state of D07 in core determines the operation of the inhibit circuitry (Figure 4-16). If D07 is represented by a 0 in the Data Register, the write current must be inhibited. This is accomplished by having inhibit current flow in opposition (parallel) to the write current in the Y drive winding on the D07 bit mat. With D07 = 0, E37 is enabled and Q7 is turned on as a result of the voltage induced at the secondary of T8 (base of Q7). Because the inhibit current is carried by two physical wires, each leg sees half of the current (370 mA in each leg). Inhibit driver Q7 is not turned on when D07 = 1, disabling E37. Current does not flow in this sense inhibit winding during the write operation, the core is switched from 0 to 1, and a 1 is written in this bit position.

4.5.4.3 **Sense Amplifier** – The sense amplifier circuit (Figure 4-16) consists of the sense amplifier, a terminating network for the sense inhibit winding, and a threshold voltage network. The sense amplifier input (E36, pins 6 and 7) is across the sense inhibit winding (points 07SB and 07SA). Resistors R46 and R47 are matched to terminate the sense inhibit winding in the desired impedance. Because Q7 is turned off during the sense (read) operation, the affect of the inhibit driver circuit, Balun transformer T7, and isolation diodes D33 and D34 can be ignored. Sense amplifier circuit E36 consists of a preamplifier and sense amplifier, both of which share a reference (threshold) voltage amplifier at pins 4 and 5. Sense amplifier operation is discussed in Paragraph 4.5.4.

4.5.4.4 **Memory Data Latches** – The memory data latches (MDL) consist of 37 flip-flop registers which temporarily store data read from memory or data to be written into memory from the bus (drawing D-CS-G113-0-1).

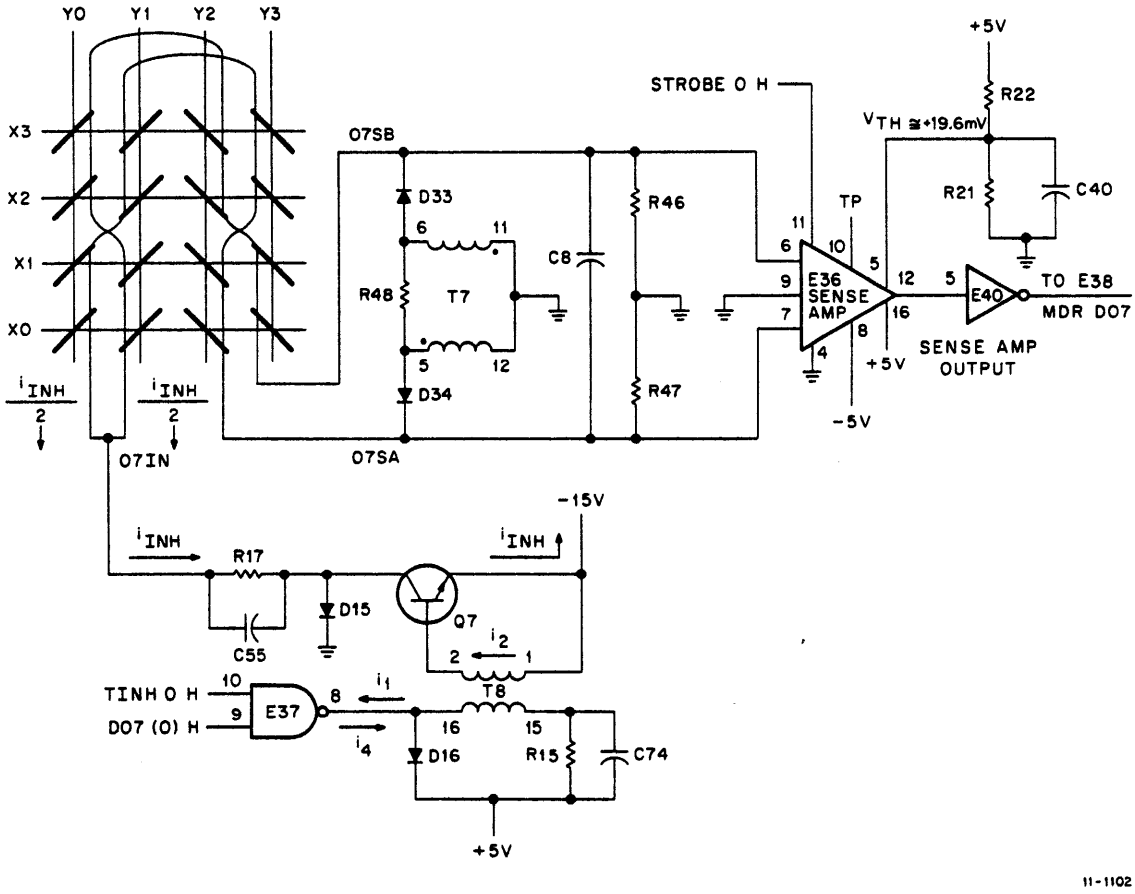


Figure 4-16 Sense Amplifier and Inhibit Driver

4.5.5 Stack Discharge Circuit

The stack discharge circuit (drawing D-CS-G231-0-1, sheet 2 of 4) assists the stack capacitance in recovering and shortens the rise time of the stack current. It also reduces unwanted currents in the seven unselected lines associated with the selected driver.

Figure 4-17 shows the stack discharge circuit. Its output, taken from the emitter of transistor Q2, goes to the junction of each X and Y read/write switch pair via a resistor. This common interconnection is labeled V_0. It is desired that $V_0 = 0$ V (ground) during a read operation, and V = -15 V during a write operation. The effective stack capacitance associated with each line is shown as C_{stack}.

To see how the stack discharge circuit reduces unwanted currents on the seven unselected lines associated with the selected driver, note the application of this circuit in the read/write switch and driver circuit shown in Figure 4-12.

During a read operation, the stack discharge circuit is off and $V_0 = 0$ V. The current generator drives the read driver node of the stack towards ground; the current generator output is clamped to ground by diode D61. The anodes of the eight read diodes are at ground. The stack discharge circuit is on and the cathodes of the seven unselected diodes are also at ground, which back biases them. The read switch pulls the cathode of the selected line towards -15 V, which forward biases it and allows conduction through the diode. Current flows only through the selected line. Reverse biasing of the diodes in the unselected lines prevents current from flowing between the unselected nodes and the selected read driver.

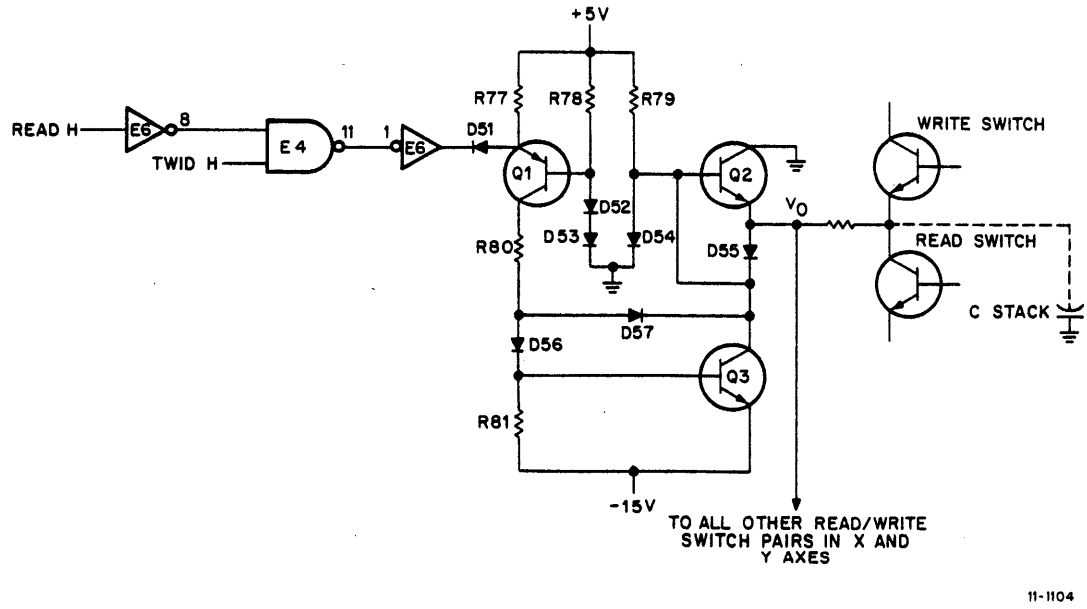


Figure 4-17 Stack Discharge Circuit

4.5.6 DC LO Circuit

The 20–30 Vac secondary tap in the H742 Memory Power Supply is constantly monitored to detect any decrease in line voltage. If the line voltage to the power supply drops to about 80–86 Vac, DC LO L is asserted (Paragraph 4.6.4.1). This signal, distributed to the M7112, M664 (drawing MF10-0-CI2), and G231 modules, terminates the operation underway, thereby preserving the integrity of the core memory and inhibiting any further memory accessing. When power is interrupted, the +5 V supply is lost and the operation of all logic is indeterminate. In this state, it is necessary to cut off the -15 V supply to the X and Y line current generators to prevent them from destroying stored data.

The DC LO circuit performs the -15 V cut off (drawing D-CS-G231-0-1). When DC LO L is asserted at the base of Q5, the transistor is reverse biased and turned off. With Q5 off, Q6 is turned off. Q7 is now turned off to open the -15 Vdc line to the current generators.

4.6 POWER SYSTEM

The MF10 power system includes the following major components:

a. an 857 Power Control
b. three 783C Power Supplies
c. an H742A Power Supply that includes three H744 +5 V Regulators and two H745 -15V Regulators.

These components are interconnected as shown on drawing D-IC-MF10-0-PW, AC-DC Power Wiring. Sheet 1 shows the ac power connections between these components and the various cooling fans that are included in the MF10 cabinet. Sheet 2 shows the dc power distribution and control connections. Sheet 3 shows the additional wiring that allows margin checks of the dc voltages distributed to the logic assembly.

4.6.1 857 Power Control

The complete circuit schematic of the 857 Power Control is shown on three separate drawings:

a. D-CS-857-0-ACL shows ac line connection and control circuits.
b. D-CS-857-0-TMP shows temperature sensor and control circuits.
c. D-CS-857-0-RC shows remote control logic.

In the following descriptions, these drawings are referenced as ACL, RC, and TMP.

4.6.1.1 System Power On – The MF10 power system is remote controlled by the DEC power control bus, which interconnects all cabinets in the system. The 3-wire DEC power control bus cable connects to J5 on the 857 Power Control. Connectors J6 and J7 are parallel with J5 to allow bus interconnection to adjacent cabinets. The DEC power control bus is defined as follows:

Pin	Signal
J5-1	SYSTEM POWER ON L
J5-2	EMERGENCY SHUTDOWN L
J5-3	GROUND

To summarize the DEC power control bus operations:

a. Any connection between line 3 and line 1 energizes all cabinets on the bus.

b. Any connection of a ground to line 2 causes all cabinet power systems on the bus to shut down.

c. If no connection exists between lines 3 and 1, and no ground is connected to line 2, all components on the bus remain in the power OFF state.

The following paragraphs describe the operating sequences of the 857 Power Control functions. The timing for these functions is shown on the 857 Power Control flow diagrams listed in the following chart.

Drawing	Operating Sequence or Case
D-FD-858-0-FL1	Normal power on, Case 1
	Normal power off, Case 2
	Solid power failure, Case 3
D-FD-858-0-FL2	Solid power return, Case 4
	Short power on-off-on cycle, Case 5
	Long power dip, Case 6
D-FD-858-0-FL3	Short power dip, Case 7
	Short pulse in power, Case 8
	Longer pulse in power, Case 9

4.6.1.2 Normal Power On – Connector pins J1-1 and 2 are jumpered to provide POWER SW ON, as shown on drawing TMP. POWER SW ON (1) causes the PWR SWD ON indicator lamp to light after 220 ms. Another jumper is connected between connector pins J3-5 and 12 so that when the SYSTEM POWER ON line on the DEC power control bus is switched to GROUND, BUS POWER REQUEST and POWER SW ON assert POWER REQUEST, as shown on drawing RC. Since no LOW VOLTAGE input connection is made to the MF10 857 connector pin J3-4, POWER REQUEST asserts POWER ALLOW as long as EMERGENCY SHUTDOWN is not grounded. Refer to drawing ACL. POWER DOWN LATCH (1) and POWER ALLOW produce POWER ON COMMAND. As ~ POWER ALLOW goes high, the POWER DOWN LATCH flip-flop latches in the 0 state.

With normal ac input voltage applied to the 857 Power Control, the +5 V POWER OKAY signal is available, as shown on drawing ACL and POWER ON COMMAND asserts POWER ON DRIVE. POWER OK and POWER ON DRIVE are applied to separate sections of the K614 AC Switch module. When these signals are applied, the K614 AC Switch module completes the ac circuit to the coil of contactor relay K1. When K1 energizes, SWITCHED POWER is applied to the MF10 power supplies.

4.6.1.3 Normal Power Off – The MF10 power system is normally turned off by remotely removing the ground signal applied to DEC power control bus pin 1. When pin 1 goes high, POWER ALLOW goes low, as shown on drawing RC. Approximately 400 ms after POWER ALLOW goes low, POWER ON DRIVE goes low to de-energize contactor relay K1, as shown on drawing ACL.

The Crowbar Control logic provided by the W519 module in the 857 is not used for MF10 power system control applications. The purpose of the RECYCLE DELAY logic is to prevent the MF10 normal power ON sequence from occurring less than four seconds after power OFF has been initiated.

4.6.1.4 Air-Flow Power Control – There are four air-flow sense switches located in the MF10 cabinet. If the flow of cooling air is interrupted at any of these locations, an air-flow sense line is grounded. The air-flow sense line from all switches is connected to the 857 Power Control REG STACKS OK H line, as shown on drawing TMP. Any air-flow malfunction will cause the OVERTEMP LATCH flip-flop to be set, as shown on drawing ACL.

When OVERTEMP LATCH sets, it causes POWER ALLOW to go low and initiate the same power OFF sequence described for normal shutdown.

NOTE

When OVERRIDE switch S2 is ON, the power OFF sequence will not be initiated by OVERTEMP LATCH, however, the OVERTEMP indicator lamp will light.

4.6.1.5 Door-Panel Power Control – The memory stack door panels and the control logic door panel are both equipped with interlock switches. If either of these panels are opened while power is applied, the power OFF sequence is initiated to prevent the equipment from operating under abnormal cooling air flow conditions. This protection circuit can be overridden, for maintenance purposes, by setting the 857 OVERRIDE switch S2 to ON.

NOTE

If the OVERRIDE switch is ON, the PWR SWD ON indicator lamp on the 857 flashes intermittently, as a warning to the technician servicing the equipment.

4.6.2 AC Power Distribution

Refer to sheet 1 of the AC-DC Power Wiring interconnection diagram, drawing D-IC-MF10-0-PW. Single-phase 115 V or 230 Vac power is connected to TB1 on the 857 Power Control. A screwdriver adjustable rotary switch, S1 (located on the 857 Power Control panel), is used to adjust the 857 for five ac input voltages: 100, 115, 200, 220, 240.

When the 857 Power Control is sequenced through the normal power ON function, the ac input is switched to the 783C Power Supplies and the H742A Power Supply.

Cooling fans at the top of the MF10 cabinet receive ac input voltage directly from the 857 Power Control and are jumper-connected for 115 V or 230 V operation. Other fans in the cabinet receive ac input voltage from the H742A Power Supply, which is prewired at the factory to provide 115 Vac outputs for cooling fans.

The 857 unswitched ac power outputs are not used for MF10 applications, but are available as convenience outlets to provide test equipment power.

4.6.3 783C Power Supplies

Sheet 1 of drawing D-IC-MF10-0-PW shows how the three 783C Power Supplies are interconnected in the MF10 power system. The 783C Power Supply circuit schematic is drawing C-CS-783C-0-1. Internal connections required at the transformer primary to accommodate various ac line voltages are charted on the drawing. Two half-wave rectifiers are connected across the secondary windings to provide +10 V and -15 Vdc outputs.

4.6.4 H742A Power Supply

The H742A Power Supply is a multi-purpose power supply which can be implemented with several voltage regulator configurations, depending upon system requirements. For MF10 applications, it is used with three H744 +5 V Regulators and two H745 -15 V Regulators.

Interconnections between the H742A, the voltage regulators, the associated power supply, and the cabinet cooling fans are shown on sheet 1 of drawing D-IC-MF10-0-PW. Because the H742A is designed for multi-purpose use, it provides several outputs that are used for other applications. Only those circuits that provide outputs used in the MF10 power system are described in the following paragraphs. The H742A circuit schematic is D-CS-H742-0-1. Jumper connections for 115 V or 230 V operation are shown on the schematic. Input voltage across the primary of transformer T1 is also applied to the power supply cooling fan and three voltage regulator cooling fans. The secondary windings provide 20–30 Vac to each of the voltage regulator inputs.

4.6.4.1 DC LO Sensing – The MF10 DC LO sensing circuit is located on the power control board of the H742A Power Supply. The power control board circuit schematic is C-CS-5409730-0-1. The H742A secondary provides 20–30 Vac to the DC LO sensing circuit. The 20–30 Vac input is rectified and stored by capacitor C3, which charges and discharges at a known rate whenever the ac power is switched on and off. Thus, the voltage applied to the emitters of differential amplifier Q6/Q7, across R17, is a rising or falling waveform of known value. For example, when ac input power drops, through shutdown or failure, the dc voltage decays at a known rate, as determined by the RC time constant. If the voltage decreases to the point where the base of Q6 becomes negative with respect to the base of Q7, the increased forward bias on Q6 causes it to conduct more current, and the resultant decrease in Q7 causes it to cut off. This removal of voltage across R16 causes Darlingtons Q16/Q17 to conduct. This, in effect, connects the DC LO output at J4-12 to the DC LO RET at J4-7. As a result, DC LO goes low when the ac power input voltage drops below a minimum level required for MF10 operation. DC LO is a natural result of the normal power OFF sequence, as well as an indication of primary power failure. The DC LO signal is used to inhibit memory timing and prevent further memory requests from being accepted. When ac input power is restored, the DC LO goes high, the RESET signal is generated by the cycle initiate logic.

4.6.4.2 +15 V Output – The power control board of the H742A Power Supply also contains a +15 V/+8 Vdc supply which receives 15–24 Vac from the secondary of transformer T1. This ac input is full-wave rectified by diode bridge D1. The resultant dc is applied to Darlington power amplifier Q1, through fuse F1. The bias on Q1 is controlled to provide +15 Vdc at output pins 2 and 3 with respect to output pins 4, 5, and 6 (ground). If the Q1 collector voltage starts to increase, the bias at the base of Q2 increases, and Q2 conducts slightly more current to maintain a constant output voltage. Zener diode D7 provides approximately +8 Vdc at output pin 1. The +8 V output is not used in the MF10. When DC LO is grounded at output pin 9, Q2 conducts hard to cut off Q1 completely, thus removing the +15 V output. The +15 V output is used by the H745 -15 V Regulator.

4.6.5 H744 +5 V Regulators

Three H744 +5 V Regulators are used in the MF10 power system. Drawing D-IC-MF10-0-PW shows where the H744 is used in the power system. The H744 circuit schematic is D-CS-H744-0-1.

4.6.5.1 **Regulator Circuit** – The 20–30 Vac input is full-wave rectified by bridge D1 to provide a dc voltage (24–40 Vdc, depending on line voltage) across filter capacitor C1 and bleeder resistor R1. Operation centers on voltage regulator E1, which is configured as a positive switching regulator. A simplified schematic of E1 is shown in Figure 4-18. E1 is a monolithic integrated circuit that is used as a voltage regulator. It consists of a temperature-compensated reference amplifier, error amplifier, series pass power transistor, and the output circuit required to drive the external transistors. In addition to E1, the regulator circuit includes pass transistor Q2, predrivers Q3 and Q4, and level shifter Q5. Zener diode D2 is used with Q5 and R2 to provide +15 V for E1. Q5 is used as a level shifter; most of the input voltage is absorbed across the collector-emitter of Q5. This is necessary because the raw input voltage is well above that required for E1 operation. This +15 V input is supplied while still retaining the ability to switch pass transistor Q2 on or off by drawing current down through the emitter of Q5.

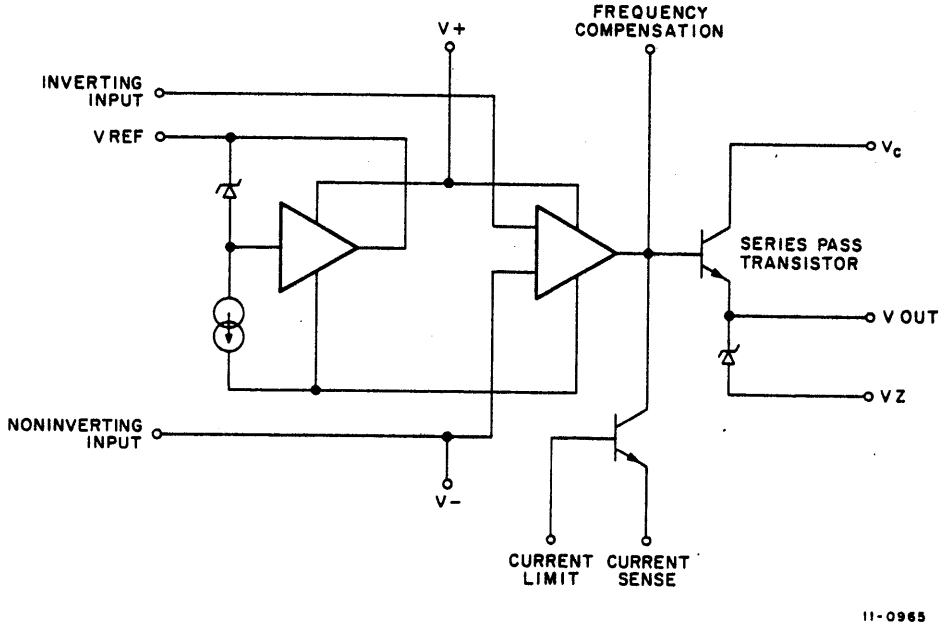


Figure 4-18 Voltage Regulator E1, Simplified Diagram

The output circuit is standard for most switching regulators and consists of "free-wheeling" diode D5, choke coil L1, and output capacitors C8 and C9. These components make up the regulator output filter. Free-wheeling diode D5 is used to clamp the emitter of Q2 to ground when Q2 shuts off, thus providing a discharge path for L1.

In operation, Q2 is turned on and off, generating a square wave of voltage that is applied across D5 at the input of the LC filter (L1, C8, and C9). Basically, this filter is only an averaging device, and the square wave of voltage appears as an average voltage at the output terminal. By varying the period of conduction of Q2, the output (average) voltage may be varied or controlled, thus supplying regulation. The output voltage is sensed and fed back to E1 where it is compared with a fixed reference voltage. E1 turns pass transistor Q2 on and off, according to whether the output voltage level decreases or increases. Defined upper and lower limits for the output are approximately +5.05 V and +4.95 V.

During one full cycle of operation, the regulator operates as follows: Q2 is turned on and a high voltage (approximately +30 V) is applied across L1. If the output is already at a +5 V level, a constant +25 V would be present across L1. This constant dc voltage causes a linear ramp of current to build up through L1. At the same time, output capacitors C8 and C9 absorb this changing current, causing the output level (+5 V at this point) to increase. When the output, which is monitored by E1, reaches approximately +5.05 V, E1 shuts off, turning Q2 off; the emitter of Q2 is then clamped to ground. L1 discharges into capacitors C8, C9, and the load. Predrivers Q3 and Q4 are used to increase the effective gain of Q2, thus ensuring that Q2 can be turned on and off in a relatively short period of time.

Conversely, once Q2 is turned off and the output voltage begins to decrease, a predetermined value of approximately +4.95 V will be reached, causing E1 to turn on. E1 in turn causes Q2 to conduct, beginning another cycle of operation. Thus, a ripple voltage is superimposed on the output and is detected as predetermined maximum (+5.05 V) and minimum (+4.95 V) values by E1. When +5.05 V is reached, E1 turns Q2 off; when +4.95 V is reached, E1 turns Q2 on. This type of circuit action is also called a "ripple regulator."

4.6.5.2 +5 V Overcurrent Sensing Circuit – The overcurrent sensing circuit consists of: Q1, R3 through R6, R25, R26, Q7, and C4. Transistor Q1 is normally not conducting, however, if the output exceeds 30 A, the forward voltage across R4 is sufficient to turn Q1 on, causing C4 to begin charging. When C4 reaches a value equal to the voltage on the anode gate of Q7, Q7 turns on and E1 is biased off, turning the pass transistor off. Thus, the output voltage is decreased as required to ensure that the output current is maintained below 35 A (approximately) and that the regulator is short circuit protected. The regulator continues to oscillate in this new mode until the overload condition is removed. C4 then discharges until E1 is again allowed to turn on and the cycle repeats.

4.6.5.3 +5 V Overvoltage Crowbar Circuit – The following components comprise the overvoltage crowbar circuit: Zener diode D3, silicon-controlled rectifier (SCR) D7, D8, R22, R23, C7, and Q6. Under normal output voltage conditions, the trigger input to SCR D7 is at ground because the voltage across Zener diode D3 is less than 5.1 V. If the output voltage becomes dangerously high (above 6.0 V), diode D3 conducts and the voltage drop across R23 draws gate current and triggers the SCR. The SCR fires and short circuits the +5 V output to ground. The SCR remains on until the capacitors discharge.

4.6.6 H745 -15 V Regulators

Two H745 -15 V Regulators are included in the MF10 power system. Operation of the H745 is basically the same as that of the +5 V regulator (drawing D-CS-H745-0-1). Input power (20 to 30 Vac) is taken from the transformer secondary and input to full-wave bridge D1, whose output is a variable 24–40 Vdc input across capacitor C1 and resistor R1.

4.6.6.1 -15 V Regulator Circuit – Regulator operation is identical to that of the +5 V regulator, except that the +15 V input that is required for E1 operation is derived externally from the H742A Power Control Board and is input across capacitor C2 to E1. In addition, the inverting and noninverting inputs to E1 are reversed and the polarities of the various components are reversed. For example, Q5, which is used as a level shifter, is an NPN transistor on the +5 V regulator; a PNP is required on the -15 V regulator, thus allowing the regulator to operate below ground (at -15 V).

Under normal operating conditions, regulator operation centers around linear regulator E1 and pass transistor Q2, which is controlled by E1. Predetermined output voltage limits are -14.85 V minimum and -15.15 V maximum. When the output reaches -15.15 V, E1 shuts off, turning Q2 off, and L1 discharges into C8 and C9. When the output reaches -14.85 V, E1 conducts, causing Q2 to turn on, thereby increasing the output voltage.

4.6.6.2 -15 V Overcurrent Sensing Circuit – The -15 V regulator overcurrent sensing circuit comprises the same components used in the +5 V regulator except that Q1 is an NPN transistor in the -15 V regulator. Q1 is normally not conducting; however, once the output exceeds 15 A, Q1 turns on and C3 charges. When C3 reaches the same value as the anode gate of Q7, E1 is biased off, which turns Q2 off, thereby stopping current flow and turning the -15 V regulator off. The regulator is, therefore, short circuit protected.

4.6.6.3 -15 V Overvoltage Crowbar Circuit – When SCR D5 is fired, the -15 V output is pulled up to ground and latched at ground until input power or the +15 V input is removed. A negative slope on the +15 V line can be used to trip the crowbar for power-down sequencing, if desired.

CHAPTER 5
MAINTENANCE

5.1 GENERAL INFORMATION

This chapter contains preventive and corrective maintenance procedures applicable to the MF10 Core Memory. Maintenance documents applicable to the processor(s) must also be available for use in conjunction with this chapter.

5.2 TOOLS AND TEST EQUIPMENT

Table 5-1 lists test equipment required for performing maintenance tasks and Table 5-2 lists diagnostic and test programs.

5.3 PREVENTIVE MAINTENANCE

Preventive maintenance is the performance of specific tasks at intervals determined by the usage of the system. The benefit to be realized from good preventive maintenance is the timely discovery of conditions which, if not detected, might result in future failure of the system. All action taken during the performance of either preventive or corrective maintenance procedures should be entered in the maintenance log book.

5.3.1 Daily Tasks

Visually inspect the equipment. Correct obvious failures such as burned out indicator lamps and improperly seated connectors. Determine that the fans are running freely and that the air filters are not clogged (Figures 5-1 and 5-2).

5.3.2 Monthly Tasks

Run MAINDEC-10-DCMMD, MF10 worst case pattern, using maintenance panel STROBE POSITION, THRESHOLD VOLTAGE, and X/Y CURRENT margin switches (Figure 3-4). At least one error-free pass for each switch setting should be run.

NOTE

The STROBE POSITION or X/Y CURRENT switch setting may be utilized simultaneously on all units of the system to minimize preventive maintenance down time. The threshold margin switch settings (THRESHOLD VOLTAGE switch in VAR position and THRESHOLD switch in VAR position) may also be utilized in more than one MF10 unit.

Also run MAINDEC-10-DCQCB (INTACT) using maintenance panel STROBE POSITION, THRESHOLD VOLTAGE, and X/Y CURRENT switches. At least one error-free hour should be run for each margin switch setting.

Table 5-1
Tools and Test Equipment

Test Equipment	Specification	Model or Type*
Multimeter	Range: capable of measuring 0 to ±70 Vdc. Sensitivity: 20 kΩ/V	Triplett 310 or Simpson 360
DVM	0.5% accuracy	Honeywell 33R
Oscilloscope	Frequency Response: 0 to 50 MHz Calibrated deflection ranges: 5 mV to 10 V/div Horizontal sweep speed: 0.1 μs/div Dual trace; delayed sweep feature	Tektronix 453
Oscilloscope Probes	Attenuation X10. Response characteristics matched to oscilloscope.	Tektronix P6010
Current	2 mA/mV or 10 mA/mV Clip-on with passive terminator	Tektronix P6020 or P6022
Unwrapping Tool (30-Gauge)		DEC H812A (No. 29-18387)
Wire-wrap Tool (Pistol Grip)		DEC H810A (No. 29-18388) or Gardner-Denver (No. 14H-1C)
30-Gauge Bit		(No. 29-10247)
30-Gauge Sleeve		(No. 29-15940)
Module Extender Boards		DEC W982
Jumper Wires	Various lengths with 30-gauge termi-point connectors on each end	
Jumper module	Wired for 32K (Table 2-1)	W974

*Equivalent types may be substituted.

Table 5-2
Diagnostic and Test Programs

DEC Number	Name
MAINDEC-10-DCZA	Memory Programs
MAINDEC-10-DCMMA	Simple Memory Data Test
MAINDEC-10-DCMMB	Simple Memory Address Test
MAINDEC-10-DCMMC	Fast AC Diagnostic
MAINDEC-10-DCMMD	Memory Diagnostic
MAINDEC-10-DCMME	BLT/Memory Exerciser Test
MAINDEC-10-DCMMF	Floating Zero/One Memory Diagnostic
MAINDEC-10-DAKFA	Instruction Timing Test
MAINDEC-10-DBKFD	Instruction Timing Test
MAINDEC-10-DCQCB	INTACT

5.3.3 Quarterly Tasks

Change the air filter (DEC Part No. 12-10757) located in the cooling fan assembly above the CMC logic section cabinet (Figure 5-1). Perform monthly preventive maintenance tasks. Clean and inspect interior and exterior of equipment.

5.3.4 Semiannual Tasks

Perform monthly and quarterly preventive maintenance tasks. Check all power supply voltages and correct all faulty power supply indications. Perform +10 V and -15 V margin checks, running MAINDEC-10-DCMMD MF10 worst case pattern, one error-free pass for each margin switch setting.

5.4 CORRECTIVE MAINTENANCE

The following paragraphs contain specific corrective maintenance information concerning tests, adjustments, and replacement procedures that apply to both preventive maintenance and troubleshooting of the MF10 Core Memory.

5.4.1 Maintenance Practices

When troubleshooting the MF10, the following CAUTION must be observed:

CAUTION

Do not ground any positive logic signal.

Do not insert or remove any module while power to the MF10 is ON and for a period of at least 30 seconds following powering down.

The PCCI and CMC logic section cabinet doors should be kept closed when operating. Only open doors when necessary for a maximum of 60 seconds.

5.4.2 Power Supply Measurements

The H744 and H745 Power Supplies shown in Figures 5-2 and 5-3 are the two adjustable supplies. Potentials should first be measured at the load. Table 5-3 lists the power supply output specifications. Figures 5-2 and 5-4 show the 783C Power Supplies.

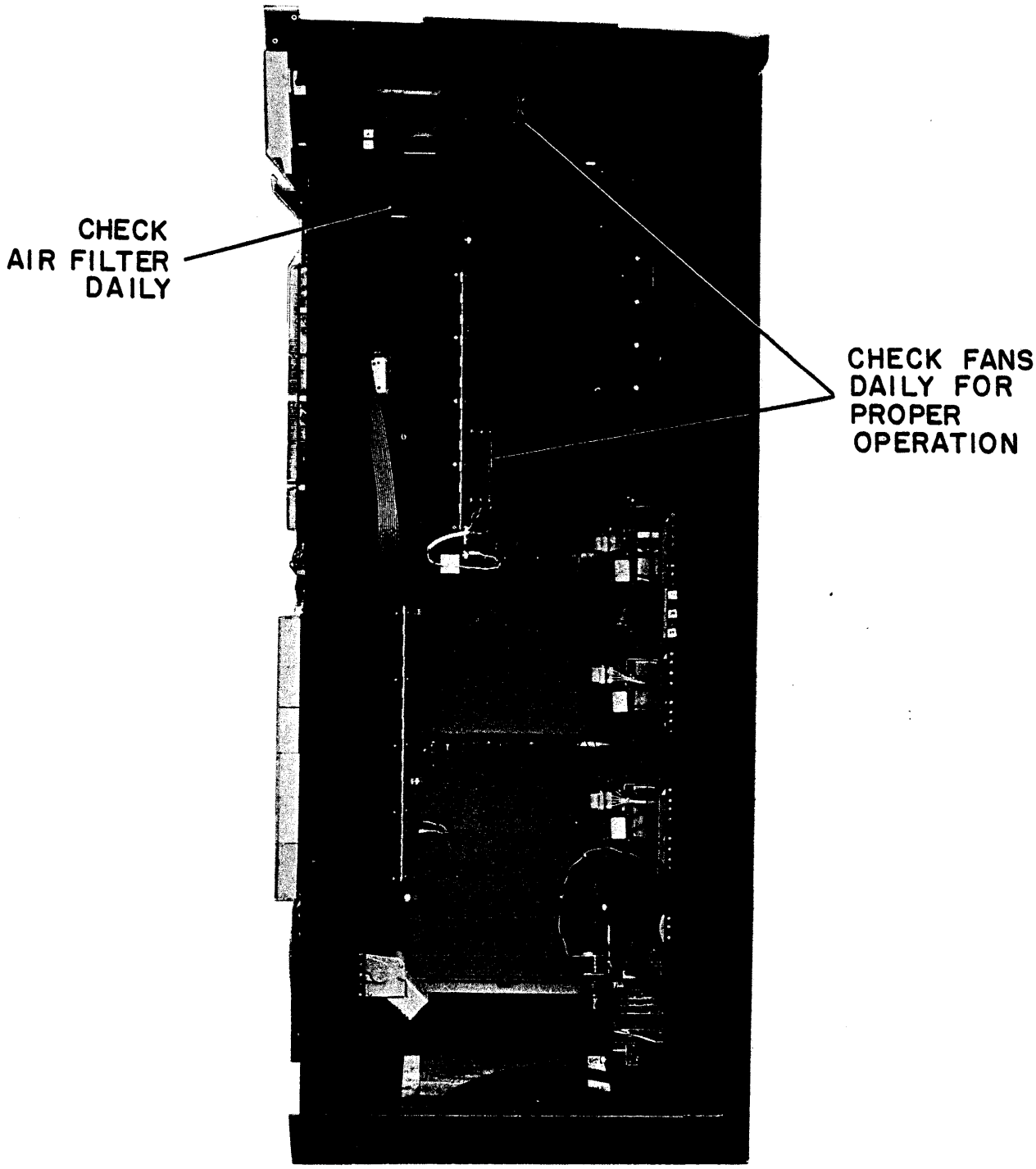


Figure 5-1 MF10 Right Side View

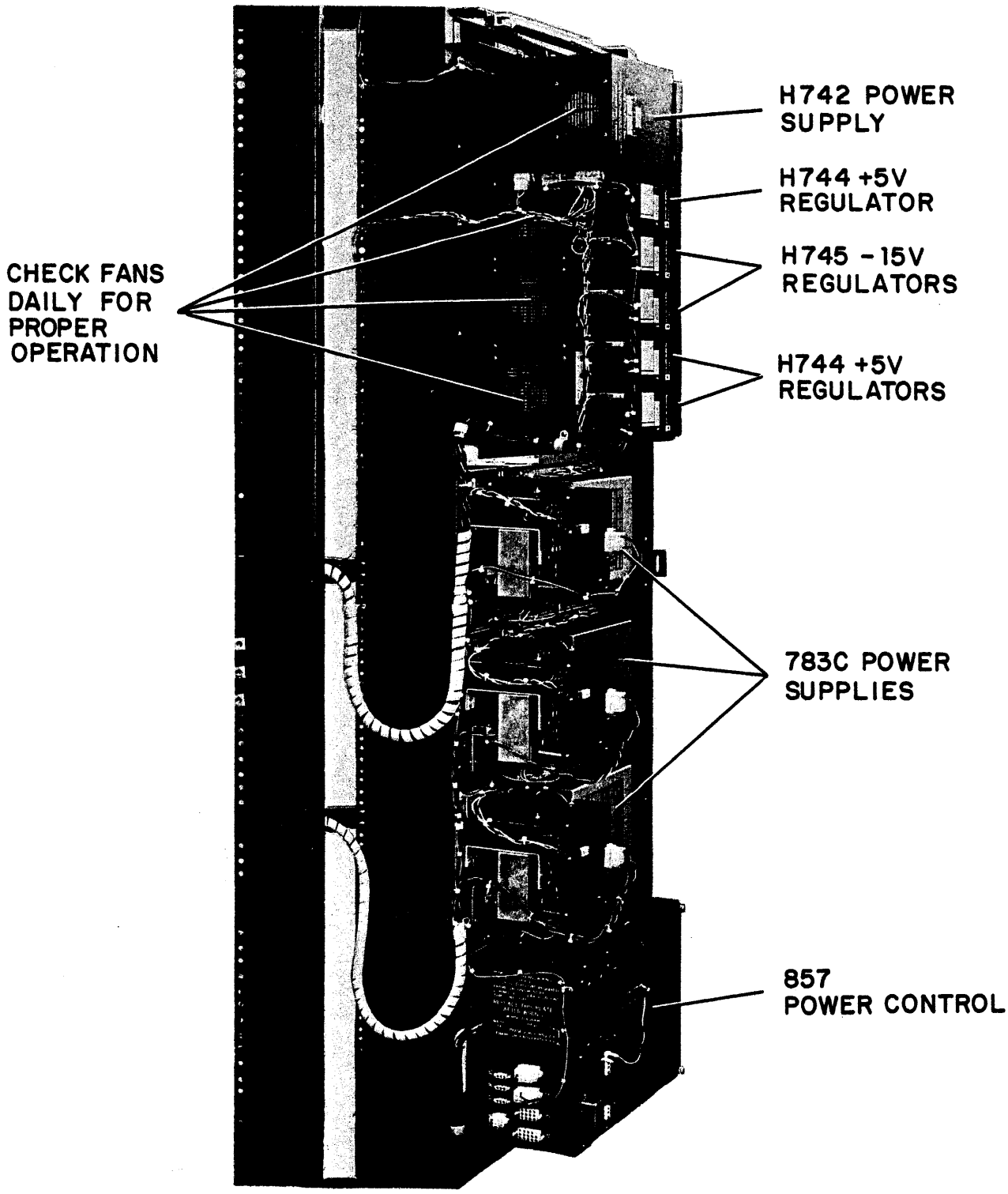


Figure 5-2 MF10 Power Supplies

Table 5-3
Power Supply Specifications

Power Supply	Voltage	Tolerance	Ripple
H742	25 Vac	20 to 30 V	N/A
	15 V (floating)	±1.5 V	N/A
	+3 V (DCLO)	⩾3.5 V	N/A
H744	+5 V	±50 mV	150 mV p-p maximum
H745	-15 V	±50 mV	450 mV p-p maximum
783C	+10 V	9.5 to 11 V	300 mV maximum
	-15 V	-14.5 V to -16 V	700 mV maximum

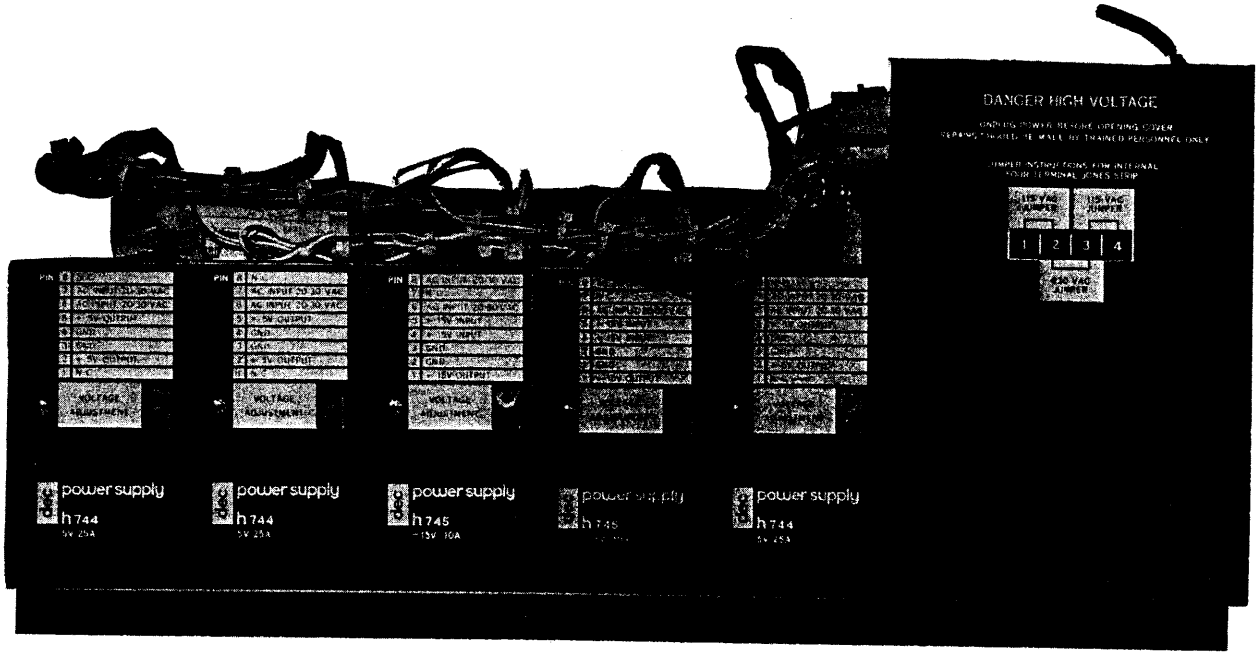


Figure 5-3 H744 and H745 Regulators/H742 Power Supply

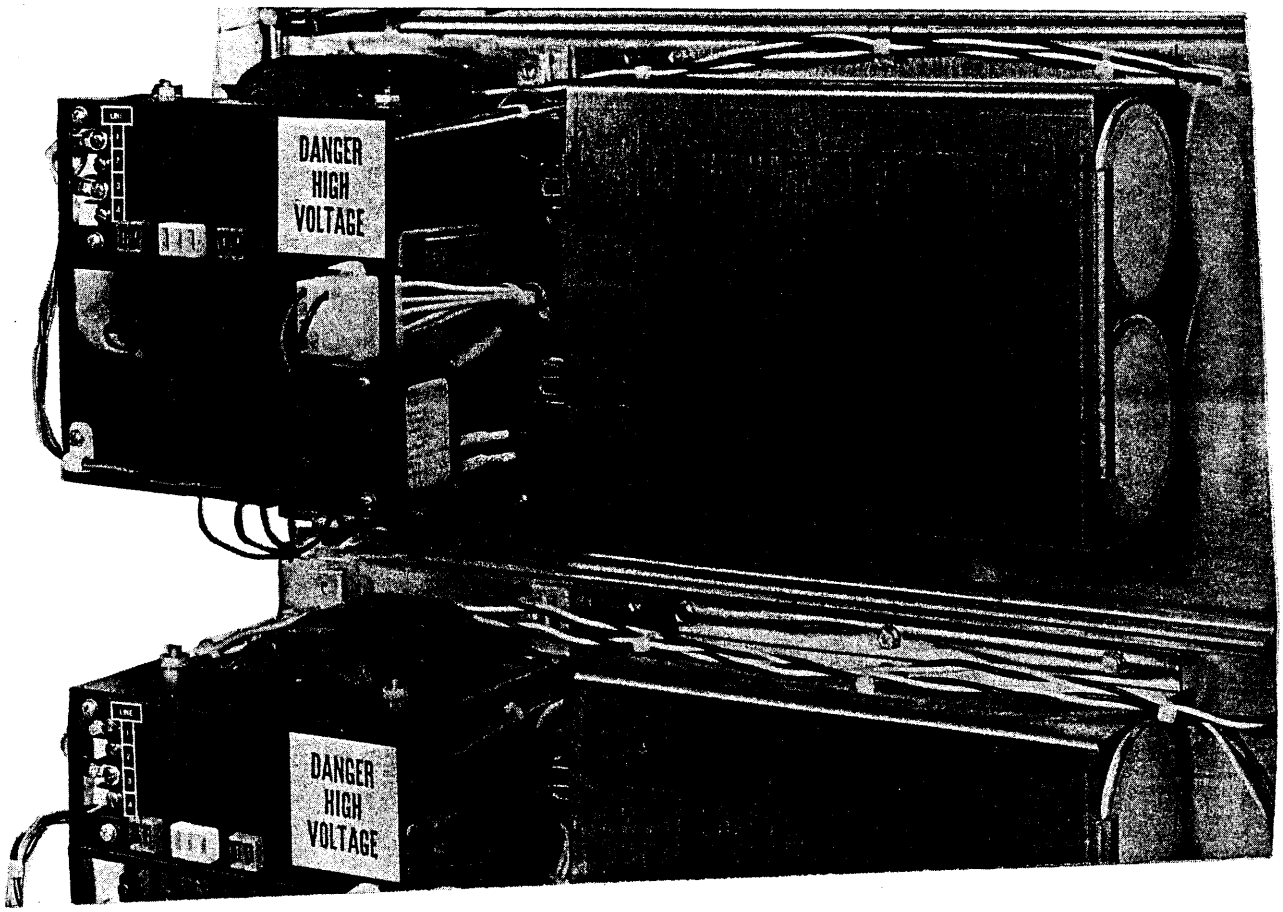


Figure 5-4 783C Power Supply

5.4.3 MF10-M Replacement and Checkout

The MF10-M is an 8K half-word (19 bits) memory bank module set consisting of one each of the following modules: G113, G231, H216, M7112.

If a memory failure is isolated to any of these four modules in a particular bank, the entire MF10-M (all four modules) must be replaced. These four modules are adjusted at the factory as a set. Each MF10-M module set is assigned a serial number which is stamped on each module of the set.

NOTE

The strobe time and X/Y current adjustments are made at the factory for all MF10-M module sets; no adjustments are to be made to these modules in the field.

After replacing an MF10-M module set, perform the following checkout procedure on the new MF10-M set.

1. Perform a repeat-examine operation and log currents of the three operating banks.

2. Synchronize the oscilloscope on MA2 RDRQ(1) (location N34-D2). Table 5-4 lists the X/Y current loop locations.

3. Check the X/Y current readings of the newly installed MF10-M. Because the X/Y currents are factory adjusted within a 15 mA range (435 to 450 mA at 25° C), a quick check on the X/Y current of a newly installed G231 module is to compare it with one or more G231 modules operating in the system. The current amplitude of the new G231 should be within 15 mA of the operating G231 modules. Allow approximately a five minute warm-up for temperature stabilization before taking current measurements.

4. Verify the operation of the X/Y current margin circuit. Change the X/Y CURRENT switch on the maintenance panel (Figure 3-4) to the +5% and -5% positions, while monitoring X/Y current for a change in amplitude.

5. While performing a repeat-examine operation, check the STROBE pulse (synchronize oscilloscope on MA2 RDRQ(1)).

6. Verify the operation of the STROBE POSITION circuit. Change the STROBE POSITION switch on the maintenance panel (Figure 3-4) to the +15NS and -15NS positions, while monitoring STROBE for a change in position.

7. Perform the monthly maintenance tasks.

Table 5-4
X/Y Current and Strobe Locations

Bank	Low Order		High Order	
	Current (G231)	Strobe (G113)	Current (G231)	Strobe (G113)
0	AF03	B04-H2	AF29	B30-H2
1	AF06	B07-H2	AF32	B33-H2
2	AF09	B10-H2	AF35	B36-H2
3	AF12	B13-H2	AF38	B39-H2
4	AF15	B16-H2	AF41	B42-H2
5	AF18	B19-H2	AF44	B45-H2
6	AF21	B22-H2	AF47	B48-H2
7	AF24	B25-H2	AF50	B51-H2

After replacing and checking an MF10-M module set perform the following:

1. Update the MF10 OPTION label located on the CMC logic section cabinet door as follows:

   a. Delete the serial number of the MF10-M replaced.
   b. Add the serial number and date of the MF10-M installed.

2. Complete a Memory Stack Return Data Sheet. Submit as much information as possible under Detailed Description of Fault heading.

3. Enclose the Memory Stack Return Data Sheet with the defective MF10-M (all four modules) and return under separate RA (Return Authorization) number to:

   Digital Equipment Corporation
   146 Main Street
   Maynard, Massachusetts 01754
   Attn: Field Service Logistics, Bldg. 21-2

4. If no stack data sheet was sent with the spare MF10-M, copy Tech Tip LOG-TT-1.

5. Order a replacement MF10-M spare through normal channels immediately.

5.4.4 Margin Checks

Refer to Paragraphs 3.2.3 and 3.2.4 for maintenance panel and margin switch operation and usage.

5.4.4.1 G024 Slice Control Check Adjustment – The G024 module must be adjusted properly before the threshold margins are checked. Proceed as follows:

1. With the THRESHOLD VOLTAGE switch (Figure 3-4) in the VAR position and the THRESHOLD switch (Figure 3-5) in the VAR position, adjust the G024 Slice Control +10 V variable input pin A2 for +10 V by varying the margin check vernier on the CPU maintenance panel.

2. Check G024 output pin P2 for a reading of +5 V. If a correct reading is obtained, proceed to step 4 of this procedure. If not, perform steps 3, 4, etc.

3. Adjust G024 output for a reading of +5 V at pin P2.

4. Check the input range of G024 by varying the CPU margin check vernier from +2.5 V to +17.5 V (monitored at G024 input pin A2).

5. Check tracking of G024 output pin P2 over a range of +4 V to +6 V. The extremes of this range should coincide with the extremes of the input voltage range (+2.5 V to +17.5 V) in step 4.

5.4.4.2 Threshold Voltage Margin Check –

NOTE

Threshold margins may be performed simultaneously on all units of the system.

The threshold voltage margin check is performed using MAINDEC-10-DCMMD, MF10 worst case pattern, and CPU console data switches 8, 9, 18, 20, 22, 25, and 26. Proceed as follows:

1. Perform G024 Slice Control check and adjust if necessary.

2. With the THRESHOLD VOLTAGE switch (Figure 3-4) in the VAR position, and the THRESHOLD switch (Figure 3-5) in the VAR position adjust margin check vernier on the CPU maintenance panel to provide +2.5 V at G024 +10 V variable input pin (location J39-A2). This will provide +4 V at the output pin P2.

3. Run MAINDEC-10-DCMMD. The diagnostic should run with no errors.

4. Adjust the CPU margin check vernier to the opposite end of the margin range to provide +17.5 V at the G024 +10 V variable input pin A2. This will cause the output pin P2 to go to +6 V.

5. Run MAINDEC-10-DCMMD. The diagnostic should run with no errors.

5.4.4.3 X/Y Current Margin Check – The X/Y current margin check is performed using MAINDEC-10-DCMMD, MF10 worst case pattern, and CPU console data switches 8, 9, 18, 20, 22, 25, and 26.

NOTE

The X/Y current margins may be performed simultaneously on all units of the system.

Proceed as follows:

1. Ensure that margin circuits are operating properly by randomly selecting a current loop in each MF10 unit of the system to be margined, and monitor the current with an oscilloscope and current probe (Table 5-4).

   a. Perform a repeat-examine operation, and proceed to monitor the current in the selected loop.

   b. While monitoring the current, change the X/Y CURRENT switch to the +5% position, then the -5% position. Ensure that the current amplitude changes properly for each switch position.

   c. Check the current amplitude change in all units of the system in turn.

2. Run MAINDEC-10-DCMMD for each switch position (+5% and -5%); the diagnostic should run with no errors.

5.4.4.4 Strobe Position Margin Check – The strobe position margin check is performed using MAINDEC-10-DCMMD, MF10 worst case pattern, and CPU console data switches 8, 9, 18, 20, 22, 25, and 26. The procedure is the same for this check as for the X/Y current margin check. The only difference is that the STROBE POSITION switch is used in this procedure.

5.4.4.5 +10 V and -15 V Margin Checks – The +10 V and -15 V margin checks are performed using MAINDEC-10-DCMMD, MF10 worst case pattern, and CPU console data switches 8, 9, 18, 20, 22, 25, and 26. Refer to Table 3-5 for margin specifications.

CAUTION

The +10 V and -15 V margins are checked in one MF10 unit at a time. If an attempt is made to margin units simultaneously, the margin circuits can overload.

Power down MF10 while removing or inserting modules or jumpers.

5.4.5 Timing Measurements and Delay Adjustments

The following timings are measured from the 1.5 V point of negative logic signals (0 V to -3 V), or from the 1.5 V point of positive logic signals (0 V to +3 V).

5.4.5.1 PSOK (W505 Module) Adjustment – To adjust PSOK, refer to drawing MF10-0-CI2 and proceed as follows:

1. Remove the W505 module from location J01 and insert in location J27. This allows the W505 to be adjusted without causing the MF10 to power down.

2. Insert jumper from W505 output pin J27F2 to the unused -3 V clamp on the G706 module, J21J2.

3. Place the J row +10 V margin switch in the VAR Position.

4. Monitor the +10 V margin voltage on pin J27A2, and decrease to +8 V by turning the margin check vernier on the CPU maintenance panel.

5. Connect Channel A of oscilloscope to W505 output pin J27F2 and Sync Negative.

6. Adjust the W505 output pin J27F2 for a low voltage indication of -3 V.

7. Adjust the potentiometer in the opposite direction until J27F2 goes to 0 V.

8. Return the J row +10 V margin switch to FIX (fixed) position, remove the jumper, and return the W505 module to location J01.

5.4.5.2 MC1 AW RQ CLR (R303 Module) One-Shot Adjustments – To adjust the MC1 AW RQ CLR one-shot locations J04 and J05, refer to drawing MF10-0-MC1 and proceed as follows:

1. Ensure that the PSOK module is adjusted and functioning properly.

2. Install jumper from R303 input pin J04V2 to MC1 AW RQ CLR (1) L pin J04D2. This will cause the one-shot to cycle.

3. Connect Channel A oscilloscope probe to J05D2, Sync Negative, and Trigger NORM, Channel A ONLY.

4. Adjust the R303 module in location J05 for a 100 μs pulse width as illustrated on drawing MF10-0-MC1.

5. Adjust the R303 module in location J04 for 200 ms between pulses as illustrated on drawing MF10-0-MC1.

6. Remove jumper.

5.4.5.3 MC1 WR RS TIMEOUT (R303 Module) One-Shot Adjustment – Refer to drawing MF10-0-MC1 and proceed as follows:

1. Remove B214 MC1 RUN module from location J17.

2. Install jumper from R303 input pin J06V2 to MC1 WR RS TIMEOUT (1) L pin J06D2.

3. Connect Channel A oscilloscope probe on J06D2, Sync Negative, and Trigger NORM, Channel A ONLY.

4. Adjust R303 module in location J06 for 20 μs between pulses as shown on drawing MF10-0-MC1.

5. Remove jumper and return B214 module to location J17.

5.4.5.4 PC1 ACT STRB (B312 Module) Delay Adjustment – To adjust PC1 ACT STRB refer to drawing MF10-0-PC1 and proceed as follows:

1. Perform a repeat-examine operation.

2. Connect Channel A oscilloscope probe to PC1 ACT STRB delay input pin K26L2, Sync Negative, and Trigger NORM, Channel A ONLY.

3. Connect Channel B oscilloscope probe to output pin K26N2.

4. Adjust the B312 module in location K26 to cause Channel B to go negative 60 ns after Channel A.

5.4.5.5 CI INITIATE R/L (M363 Module) Delay Adjustment – To perform this adjustment refer to drawing MF10-0-CI2 and proceed as follows:

1. Perform a repeat-examine operation.

2. Connect Channel A oscilloscope probe to PC1 Pn MA STRB for the port being used. The pin numbers of PC1 Pn MA STRB are:

   PC1 P0 MA STRB – N25F2
   PC1 P1 MA STRB – N25K2
   PC1 P2 MA STRB – N25P2
   PC1 P3 MA STRB – N25T2

   Set oscilloscope to Sync Negative, and Trigger NORM, Channel A ONLY.

3. Connect Channel B oscilloscope probe to CI INITIATE L/R pin H33K2/L2.

   NOTE
   PC1 Pn MA STRB is negative logic and CI INITIATE L/R is positive logic.

4. Adjust the M363 module in location H33 to cause Channel B to go negative 60 ns after Channel A as shown on drawing MF10-0-CI2.

5.4.5.6 PC3 STRB (B312 Module) Delay Adjust – Refer to drawing MF10-0-PC3 and proceed as follows:

1. Perform a repeat-examine operation.

2. Connect Channel A oscilloscope probe to H33K2 or L2 (CI INITIATE L/R), Sync Negative, and Trigger NORM, Channel A ONLY.

3. Connect Channel B oscilloscope probe to PC3 Pn STRBn of the port being used. The pin numbers are as follows:

   PC3 P0 STRB 1 – K05D2
   2 – K06D2
   3 – K06U2
   PC3 P1 STRB 1 – K04D2
   2 – K05U2
   3 – K04U2
   PC3 P2 STRB 1 – K03D2
   2 – K02D2
   3 – K03U2
   PC3 P3 STRB 1 – K01D2
   2 – K02U2
   3 – K01U2

4. Adjust the B312 module in location K14 to cause Channel B to go negative 360 ns after Channel A as shown on drawing MF10-0-PC3.

   NOTE
   CI INITIATE L/R and PC3 Pn STRBn are positive logic signals.

5.4.5.7 **MC1 CYC DONE (B312 Module) Delay Adjustment** – Refer to drawing MF10-0-MC1 and proceed as follows:

1. To operate the MF10 at full speed, perform the following steps:

   a. Disconnect the memory bus cables (in and out) for port 0. This causes the memory bus inputs to the unit to float. Among the asserted floating inputs are signal levels PAS1 P0 RQ CYC, P0 MADR RD RQ, and P0 MADR WR RQ.

   b. Install jumper from the Quick Latch connector pin J5 (P0 MADR WR RQ (1) L) to pin H6 (ground) of port 0 (drawing MF10-0-MBI). This inhibits Write Request, leaving Read Request (P0 MADR RD RQ) asserted to cause successive read/restore cycles.

2. Connect Channel A oscilloscope probe to J17S2 (MC1 CYC DONE), Sync Negative, and Trigger NORM, Channel A ONLY.

3. Adjust the B312 module in location J19 for 950 ns between negative-going transition of signals as shown on drawing MF10-0-MC1.

5.5 TROUBLESHOOTING

5.5.1 Procedural Aids

The following paragraphs contain procedures for performing the operations in the troubleshooting flowcharts (Figures 5-5 through 5-7). These paragraphs are referenced on the flowcharts in a block connected to the operation by a dotted line.

5.5.1.1 **Read/Modify/Write Instruction** – This operation is performed to check those circuits peculiar to the read/write/modify cycle. Proceed as follows:

1. Clear memory to all 0s.

2. Deposit 000000, 000001 in AC1.

3. Set console data switches to 272040, E* (ADDM 1,E).

4. Press XCT switch. MF10 MB (indicator) should increment by 1 each time XCT switch is pressed.

5.5.1.2 **Loading Diagnostic Into Failing Memory** – Load DCMMD, using the following procedures:

1. Load diagnostic into a good memory (if more than one memory is in the system) and operate the following maintenance switches:

   a. MF10 SWAP switch (only if memory is 64K)
   b. ±15NS STROBE POSITION switch
   c. THRESHOLD MARGIN switch (Paragraph 5.4.4.2, steps 2 and 4)
   d. ±5% X/Y CURRENT switch

2. Inhibit read/modify/write cycles [CPU SPLIT SYNC (1)] using the following switches:

   a. KA10 – Set FM ENB switch to off.
   b. KI10 – Set STOP PAR switch to on.

*E = an address within the failing memory.

5.5.1.3 **Forcing Failure** – If an error does not occur when running a diagnostic, use the following procedures:

1. The following program writes all memory addresses into both the low and high order halves of the respective memory locations; i.e., the data contained in a location is the address of that location. For example: location 000020 contains 000020 as data in both halves of bank 0, and location 020020 contains 020020 as data in both halves of bank 1. The program then executes continuous read/restore cycles, checking each location for errors (CAME instruction). If an error occurs, the program halts at location 000016. To continue the program, press the CONT (Continue) button on the CPU. Deposit the following program and START at location 000003.

Location (Octal)	Assembled Instruction (Octal)	Instruction Code
000000/	000017, 000017	
000001/	000000, 000000	
000002/	000000, 000000	
000003/	200100, 000000	MOVE 2,0
000004/	252100, 000000	AOBJP 2,5
000005/	550040, 000002	HRRZ 1,2
000006/	202120, 000001	MOVEM 2,@1
000007/	306040, *E	CAIN 1,E
000010/	254000, 000012	JRST ,12
000011/	254000, 000004	JRST ,4
000012/	505300, 254000	HRLI 6,254000
000013/	541300, 000015	HRRI 6,15
000014/	254000, 000003	JRST ,3
000015/	312120, 000001	CAME 2,@1
000016/	254200, 000017	JRST4 ,17
000017/	254000, 000007	JRST ,7

NOTE

To restart program after an Error Halt has occurred, deposit 202120, 000001 in location 000006 and start program at location 000003. This will rewrite each location.

2. Vary the CPU SPEED CONTROL while performing:

   a. a repeat-deposit (1s and 0s)
   b. a repeat-examine (1s and 0s)
   c. a repeat-execute of a MOVEM instruction (1s and 0s).

3. Margin rows L, M, and N while performing a, b, and c of step 2 above. (Refer to Table 3-5 for margin specifications.)

5.5.1.4 **Performing Repeat-Examine Operation With KI10 Hung** – If only one MF10 is in the system, alternately press KI10 RESET and EXAMINE THIS switches.

*E = Memory Size: 017777 (8K), 037777 (16K), 077777 (32K), 177777 (64K), 377777 (128K), 777777 (256K).

For a KI10 with more than one memory, perform the following procedures:

1. Deposit 700200, 440000 in AC1.

2. Deposit 200200, E* in AC2.

3. Deposit 254000, 000001 in AC3.

4. Deposit 254000, 000001 in location 000070 of good memory.

5. Start program at location 000001. The memory cycle will initialize approximately every 1.2 second.

5.5.1.5 **Checking Power-Up Sequence** – The following MF10 indicators should display:

1. PSOK
2. CYC DONE (1)
3. ACTIVE; P0–P3 (0)
4. REQUESTS; P0–P3 (0), AW(1)
5. ENABLES: MB SEL (0), DATA IN (0), and DATA OUT (0)
6. INC RQ (0)
7. RUN (0)
8. STOP (0)

5.5.1.6 **Interpretation of Diagnostic Error Indications** – At this point in the MF10 troubleshooting flow, the diagnostic error indications must be carefully interpreted to determine if the failure is a data error or an addressing error. The type of diagnostic test being performed is usually a good indication of the type of failure, i.e., addressing or data diagnostic. However, addressing failures can cause parity error indications with no data error existing, or data failures can occur without parity error indications (e.g., dropping or picking up an even number of bits). If data tests produce errors, run address tests and compile sufficient error data before making a decision on the type of failure.

When interpreting a diagnostic address test, the data contained in a location is the address of that particular location. The data formats are as follows:

a. DCMMB – 000000, ADR

b. DCMMD – $\overline{\text{ADR}}$, ADR. The 1s complement of the address is written into the low order bits of the data word (bits 00 – 17).

c. Address test in Paragraph 5.5.1.3, step 1 – ADR, ADR.

*E = an address within the failing memory.

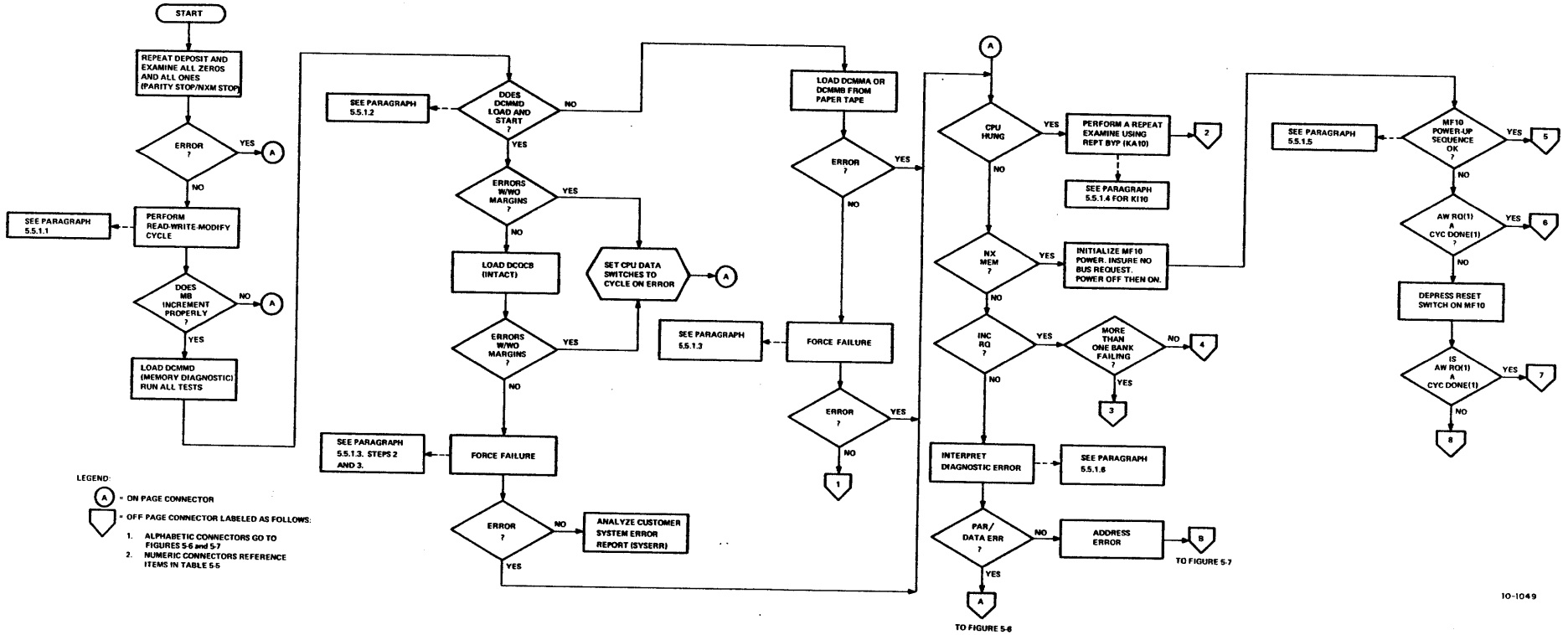

START
REPEAT DEPOSIT AND EXAMINE ALL ZEROS AND ALL ONES (PARITY STOP/NXM STOP)
ERROR ?
YES
A
NO
SEE PARAGRAPH 5.5.1.1
PERFORM READ-WRITE-MODIFY CYCLE
DOES MB INCREMENT PROPERLY ?
NO
A
YES
LOAD DCMMD (MEMORY DIAGNOSTIC) RUN ALL TESTS
SEE PARAGRAPH 5.5.1.2
DOES DCMMD LOAD AND START ?
NO
YES
ERRORS W/WO MARGINS ?
YES
NO
LOAD DCOCB (INTACT)
SET CPU DATA SWITCHES TO CYCLE ON ERROR
A
ERRORS W/WO MARGINS ?
YES
NO
SEE PARAGRAPH 5.5.1.3. STEPS 2 AND 3.
FORCE FAILURE
ERROR ?
NO
ANALYZE CUSTOMER SYSTEM ERROR REPORT (SYSERR)
YES
LOAD DCMMA OR DCMMB FROM PAPER TAPE
ERROR ?
YES
NO
SEE PARAGRAPH 5.5.1.3
FORCE FAILURE
ERROR ?
YES
NO
1
A
CPU HUNG
YES
PERFORM A REPEAT EXAMINE USING REPT BYP (KA10)
2
NO
SEE PARAGRAPH 5.5.1.4 FOR KI10
NX MEM ?
YES
INITIALIZE MF10 POWER. INSURE NO BUS REQUEST. POWER OFF THEN ON.
NO
INC RQ ?
YES
MORE THAN ONE BANK FAILING ?
NO
4
YES
3
NO
INTERPRET DIAGNOSTIC ERROR
SEE PARAGRAPH 5.5.1.6
PAR/ DATA ERR ?
NO
ADDRESS ERROR
B
TO FIGURE 5-7
YES
A
TO FIGURE 5-6
SEE PARAGRAPH 5.5.1.5
MF10 POWER-UP SEQUENCE OK ?
YES
5
NO
AW RQ(1) A CYC DONE(1) ?
YES
6
NO
DEPRESS RESET SWITCH ON MF10
IS AW RQ(1) A CYC DONE(1)
YES
7
NO
8
LEGEND:
A = ON PAGE CONNECTOR
= OFF PAGE CONNECTOR LABELED AS FOLLOWS:
1. ALPHABETIC CONNECTORS GO TO FIGURES 5-6 and 5-7
2. NUMERIC CONNECTORS REFERENCE ITEMS IN TABLE 5-5

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Table 5-5
CPU Hung, NX MEM, and INC RQ, Probable Cause of Failure

Item	Symptom	Probable Cause
1	No error indication	Bus Enable signals or bus receivers/ transmitters (W122s and B685s). (Refer to drawings D-BS-MF10-0-MB1/2/3 and D-BS-MF10-0-PC3.)
2	CPU hung	PC2 Pn RD RS, PC3 Pn STRB1, PC2 Pn MA STRB, or MC1 STATE CLR incorrect.
3	INC RQ with more than one bank failing	CI WR RS L/R, CI C00 L/R, CI C01 L/R, or MC1 STATE CLR at CI START OF WRITE time
4	INC RQ with only one bank failing	START WRITE L/R (M7112 of failing bank), or CI Bank SEL L/R (M7112 of failing bank).
5	NX MEM but MF10 power-up sequence OK (Paragraph 5.5.1.5)	Restart CPU and check PC2 Pn ADR ACK, PC1 Pn ACT, PC1 ACT STROBE, MC1 STATE CLR, and PASn Pn RQ.
6	NX MEM, MF10 power-up sequence not OK, AW RQ (1), and CYC DONE (1)	Flip-flop associated with incorrect indicator state. Paragraph 5.5.1.5 lists correct indicator states.
7	Press RESET switch and the symptoms of item 6 remain.	MC1 START or CI PSOK incorrect.
8	Same as item 7 except AW RQ (1) and CYC DONE (1) incorrect.	MC1 STATE CLR, PC1 AW RQ, or MC1 CYC DONE incorrect.

Figure 5-5 CPU Hung, NX MEM, and INC RQ
Troubleshooting Flowchart

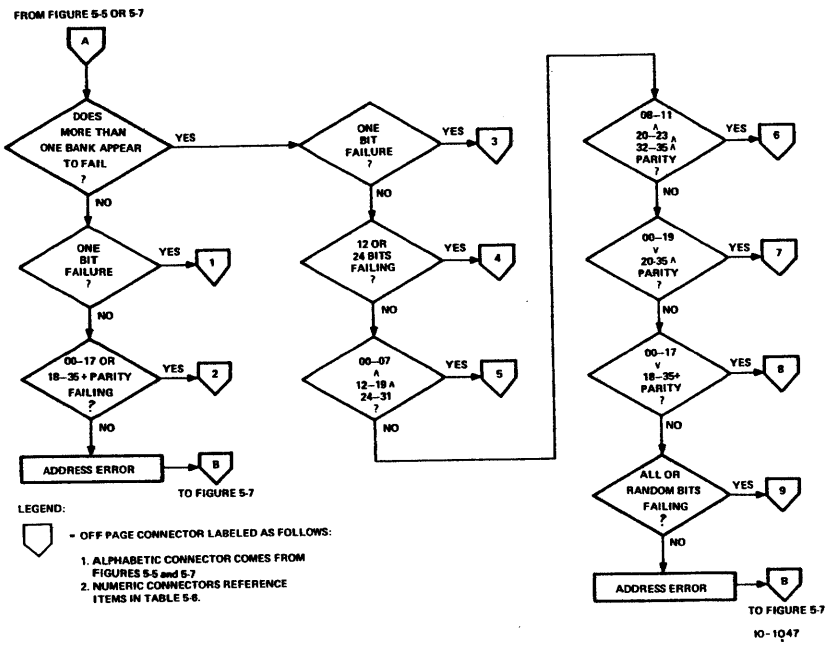


Table 5-6
Memory Parity Error, Probable Cause of Failure

Item	Symptom	Probable Cause
1	One bank, one data failure	Sense line inputs (XXSA/XXSB), inhibit line (XXIN), or DATA LATCH input/output (DXX) (drawings D-CS-G113-0-1 and D-MU-MF10-0-MUAF).
2	One bank, low or high order data bits plus parity failure (00–17 or 18–35 plus parity)	X/Y driver/switch (G231), X/Y current (G231), STROBE (G113), RESET (G113), TNAR (M7112), TWID (M7112), or TINH (M7112)
3	More than one bank, one data bit failure	W122 receiver/transmitter module (MB) of failing bit, M565 module (MB) of failing bit, or CIC CABLE
4	12 or 24 data bits failing	PC3 Pn STRB 1, 2, 3, or PC3 Pn MB SEL 1, 2, 3
5	Data bits 00–17, 12–19, and 24–31 failing in more than one bank	PC3 DATE IN EN 1
6	Data bits 08–11, 20–23, 32–35 plus parity failing in more than one bank	PC3 DATA IN EN 2
7	Data bits 00–19, or 20–35 plus parity failing in more than one bank	MC1 MB CLR 1, or MC1 MB CLR 2, respectively
8	Data bits 00–17, or 18–35 plus parity failing in more than one bank	CI DATA OUT EN L, or CI DATA OUT ENR, respectively
9	All or random bits failing in more than one bank	Check the following: PC3 DATA IN EN PC3 DATA OUT EN PC3 MB SEL CI STROBE CI THRESHOLD (+5 V FIXED) MC1 MB CLR 1/2 Delay Adjustments: a. CI INITIATE b. MC1 CYC DONE c. PC3 STRB d. Ensure PC3 Pn STRB 1, 2, 3 are not occurring at the same time as the sense amplifier STROBE (G113) Ensure that the sense amplifier STROBE is not generated during a clear/write cycle (check CI C01) MC1 STATE CLR All voltages

Figure 5-6 Memory Parity/Data Error Troubleshooting Flowchart

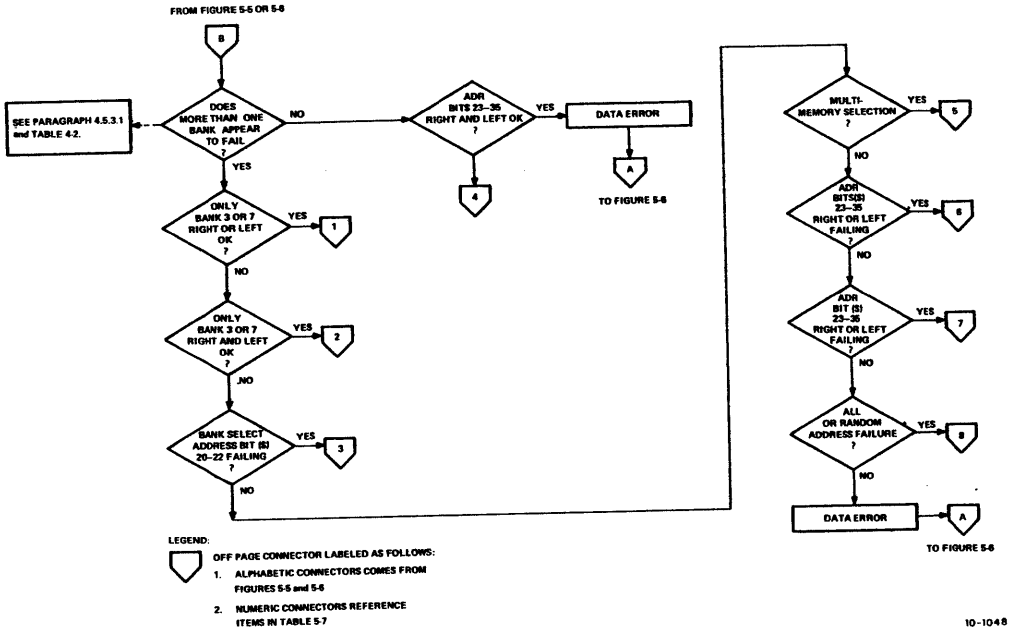


Table 5-7
Memory Addressing Error, Probable Cause of Failure

Item	Symptom	Probable Cause
1	MB bits 02–04 or 20–22 indicate that only the left or right bank of bank 3 or 7 (32K or 64K) has no errors	Multi-banks selected due to faulty CIC CABLE (CIC and MUAF Engineering Drawings) CI BANK SELECT N L/R signals
2	MB bits 02–04 and 20–22 indicate that only the left or right bank of bank 3 or 7 (32K or 64K) has no errors	Multi-banks selected due to failing CI BANK SELECT N L/R
3	MB bits 02–04 and 20–22, when compared with correct address bits 20–22, indicate BANK SELECT address bit(s) 20–22 incorrect; therefore, the wrong bank is selected	Wrong bank selected due to failing CI 20–22
4	One bank, MB bits 05–17 or 23–35 incorrect	Bus AXX (G231), or X/Y drivers/ switches
5	More than one bank failing with multi-memory selection	Pn MADR 14–20, or PAS 1/2 Pn RQ
6	More than one bank failing, with bit(s) in right or left bank (MB bits 05–17 or 23–35) incorrect	MA 1/2 XX, or Pn MADR 23–35
7	More than one bank failing, with bit(s) in right bank and left bank (MB bits 05–17 and 23–35) incorrect	MA1/2 XXL (M565), MA1/2 XXR (M565), or CIC CABLE (MA bits 23–35)
8	All or random address failure	PC1 Pn MA STRB, PC1 MA CLR, or PC1 ACT STRB delay adjustment. Check all voltages.

Figure 5-7 Addressing Error Troubleshooting Flowchart

5.5.2 MF10 Power System Maintenance

WARNING

Dangerous voltages (115 or 230 Vac) are present in the power system. Be careful when servicing these circuits.

Familiarize yourself with Chapter 4 which describes the MF10 power system and contains circuit descriptions of each component and assembly. Drawings depicting the circuits are:

H742 Power Control Board	C-CS-5409730-0-1
H744 +5 V Regulator	D-CD-H744-0-1
H745 -15 V Regulator	D-CS-H745-0-1

These drawings show all power control switches, circuit breakers, fuses, thermal cut-out switches, and power indicator lamps in the power system. A thorough knowledge of the location and operation of these components is essential for troubleshooting.

If a power system fault is suspected, visually inspect the components for obvious fault indications. For example, each of the voltage regulator modules is provided with an output indicator lamp that lights when the output voltage is within range. If a single indicator lamp is off, the fault is probably within that voltage regulator module. In the case of the H744 +5 V Regulator, this can be verified by swapping H744 modules. Once the fault has been isolated to a voltage regulator module, refer to the voltage regulator checkout procedures described in subsequent paragraphs.

CAUTION

Refer to Engineering Drawing D-IC-MF10-PW and Figure 5-3 when swapping H744 or H745 modules. Either of these regulator modules in the wrong slot can burn up the power supply.

NOTE

When replacing a faulty voltage regulator, the new voltage regulator may need adjustment to compensate for the load. In some instances, if the new regulator is initially adjusted too high, it may activate the crowbar circuit and therefore provide no output when installed. If this happens, turn power off and rotate the adjustment potentiometer counterclockwise. Then reapply power (regulator should not crowbar) and adjust the regulator output.

If none of the voltage regulator output indicator lamps are lighted, the fault is probably in the associated H742 Power Supply or 857 Power Control. Visually inspect the power indicator lamps and circuit breakers provided with these components to determine whether the fault can be isolated to either the H742 or the 857.

5.5.2.1 Recommended Test Bench Source – Figure 5-8 shows a recommended test bench source that can be fabricated from standard parts used for voltage regulator bench tests. Figure 5-8 also shows the test bench loads used to test the voltage regulator outputs under various load conditions. No additional test equipment or special tools are required other than those listed in Table 5-1.

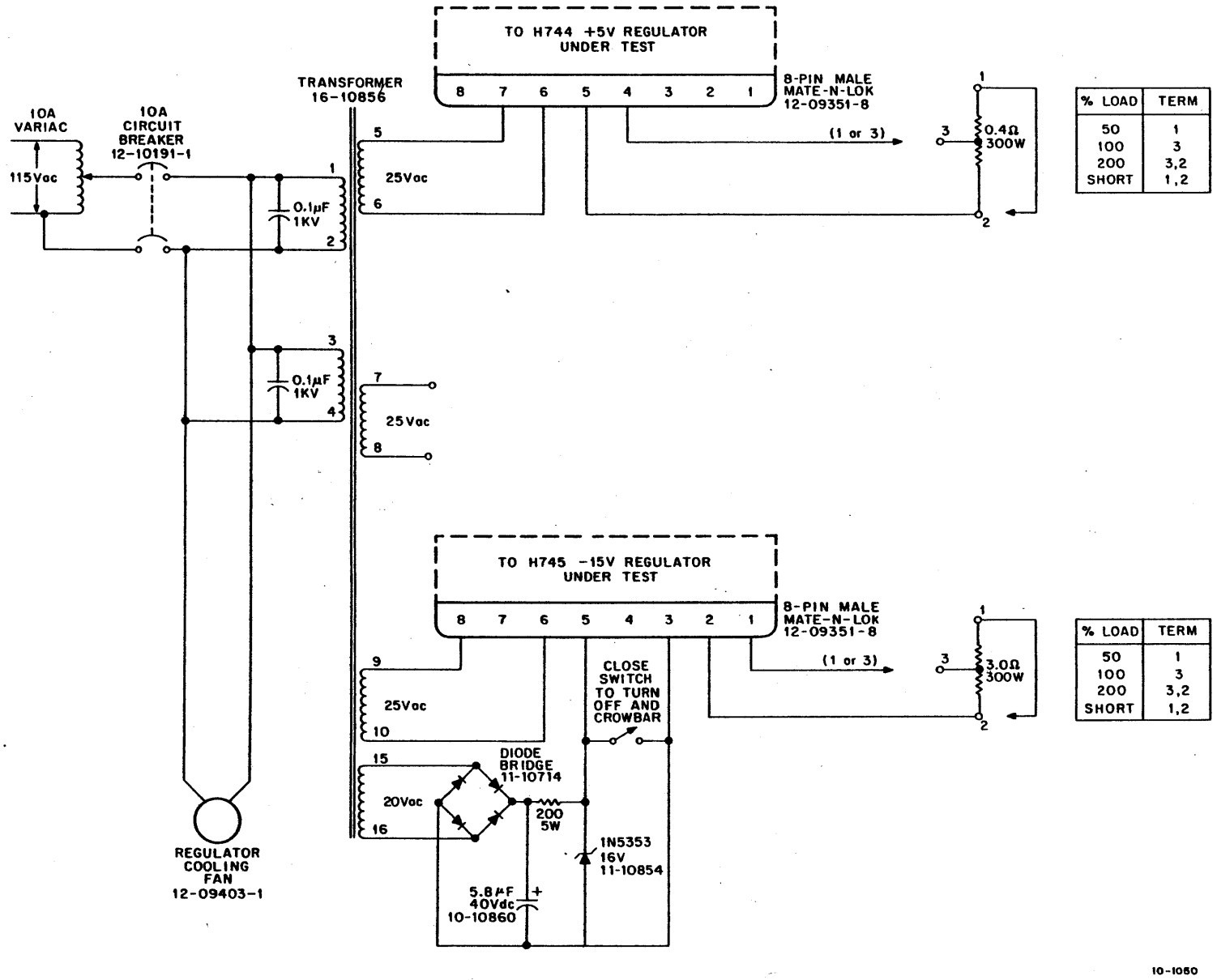


Figure 5-8 Voltage Regulator Test Bench Source and Loads

5.5.2.2 **Initial Tests** – When a power system fault has been isolated to a voltage regulator, examine internal fuse F1. A blown fuse usually indicates that the main pass transistor Q2 and/or one of its drivers Q3 and Q4 has short-circuited.

1. Check for damage to base-emitter bleeder resistors and scorching of the etched board in the area of Q3 and Q4.

2. If the pass transistor and drivers check OK on a VOM, the fault may be caused by continuous base drive to the first driver Q4. Check level shifter Q5 for a short-circuit.

3. Check the resistance to ground at the input to the precision voltage regulator integrated circuit E1 (pins 4 and 5) to determine if an external short-circuit is holding the IC in conduction. The approximate resistance to ground is listed for each voltage regulator in the following chart:

Type of Voltage Regulator	Inverting (-) Input Pin 4	Non-Inverting (+) Input Pin 5
H744	20K	1.5K
H745	1.5K	5K

4. Use the VOM to check for a short-circuit between the fuse terminals and ground. Possible short-circuits involving mounting TO-3 components to the heat sink may be located by connecting VOM leads between TO-3 cases and a regulator bracket mounting screw on the end of the heat sink.

5.5.2.3 **Output Short-Circuit Tests** – A voltage regulator that provides no output, or low output, without causing fuse F1 to blow is probably working into a short-circuited output.

NOTE

An activated crowbar or a short-circuited output in an otherwise properly operating voltage regulator will not cause F1 to blow.

1. If fuse F1 is not blown, and the area of etched circuit around the ac input to the bridge circuit is not damaged, it is safe to apply an ac input to the voltage regulator to determine if the regulator is overloaded by a short-circuit across the output.

2. Connect the voltage regulator to the test bench source and advance the Variac to about 90 V. If the output is near 0 V, turn the voltage adjustment fully counterclockwise and repeat the test.

3. If the regulator appears overloaded, check for short-circuit across the output and for a component failure in the crowbar circuit.

5.5.2.4 **Testing a "Dead" Regulator** – Use the following procedure to test a faulty voltage regulator which can not be fault isolated via the initial tests described in Paragraph 5.5.2.2.

1. Apply 115 Vac to the test bench source (25 Vac at the voltage regulator input), with no load on the regulator output.

2. Check for 30 Vdc across filter capacitor C1.

3. Check for +15 Vdc at pin 12 of precision voltage regulator E1. No voltage at this point could mean Zener diode D2 (H744) has failed.

4. Check for 6.8 Vdc to 7.5 Vdc at pin 7 of E1 with respect to ground, pin 6.

5. If all voltage measurements in steps 2, 3, and 4 check out and there is no output voltage, pin 5 of E1 should be positive with respect to pin 4.

6. E1, pin 2 should be +0.6 V with respect to pin 3. If it is not, connect emitter and base of Q5 together. If 0.6 V indication is then obtained, precision voltage regulator E1 is OK and the fault probably is caused by Q5 or Q4.

5.5.2.5 Testing a Voltage Regulator After Repairs – Before returning a repaired voltage regulator to service, check it on the test bench source, using the recommended test bench loads.

1. Connect the repaired voltage regulator to the appropriate source connector.

2. Set the voltage adjustment fully counterclockwise and set the load to zero.

3. Close the input circuit breaker and advance the Variac until output voltage is indicated (at approximately 60–80 Vac input). No noise should be audible under no-load conditions.

4. Advance the Variac to 130 Vac and return to 115 Vac.

5. Be sure Q2 is connected and soldered before loading the regulator.

6. Apply a 30 to 50 percent load. The output voltage should remain nearly constant. A clean whistle may be heard. A buzz or a harsh hissing sound indicates possible instability. Check waveforms as indicated in Figure 5-9.

7. Apply 100 percent load and set the voltage adjustment for nominal output:

H744	+5.10 Vdc
H745	-15.10 Vdc

8. Apply 200 percent load and check for a decrease in the frequency and the output voltage.

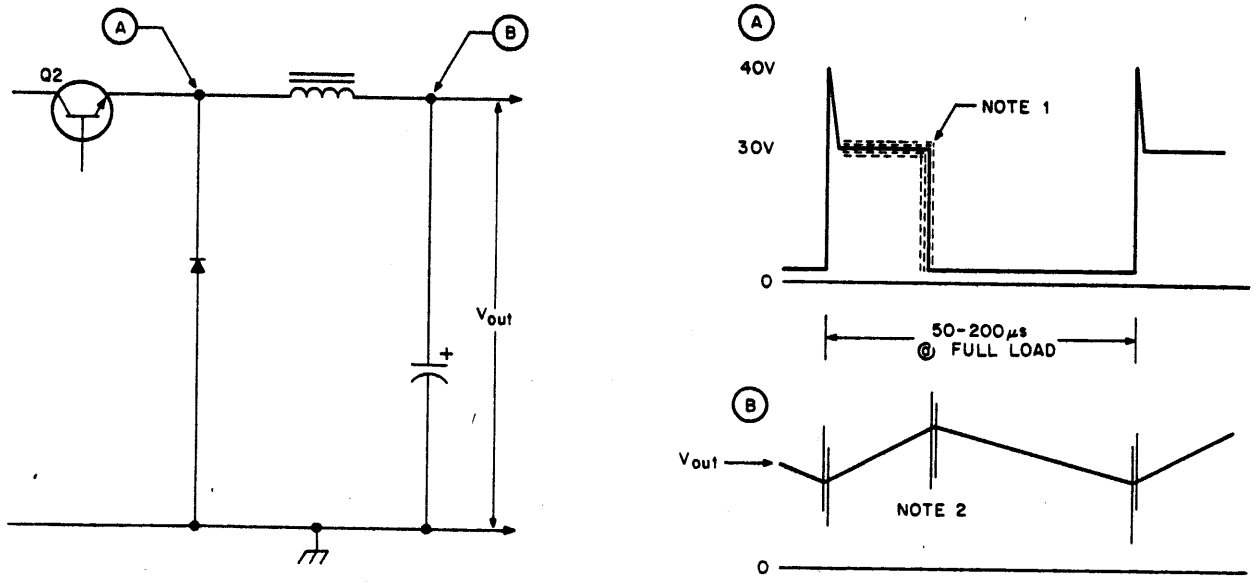
CAUTION

If the output voltage does not decrease noticeably (approximately 1 V on H744, or 1 V to 5 V on the H745), do not attempt the following short-circuit test.

9. Short-circuit the output. The regulator should continue to operate at a low frequency with a clean, smooth whistle and stable waveforms.

10. Increase the voltage adjustment and observe the output voltage when the crowbar circuit fires. The output voltage should be within the following ranges:

H744	6.00–6.65 V
H745	16.8–20.5 V



NOTE 1: 30 volt level shifts with AC input voltage. Small 120Hz jitter is normal.

NOTE 2: Output ripple and noise as follows:

	H744	H745
RIPPLE (P to P)	3% max.	3% max.
	2% typ.	2% typ.
NOISE (PEAK)	1%	1%

Measure noise with a short 100Ω terminated piece of foil coax. Normal 10:1 scope probe will not give an accurate noise measurement.

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Figure 5-9 Typical Voltage Regulator Output Waveforms