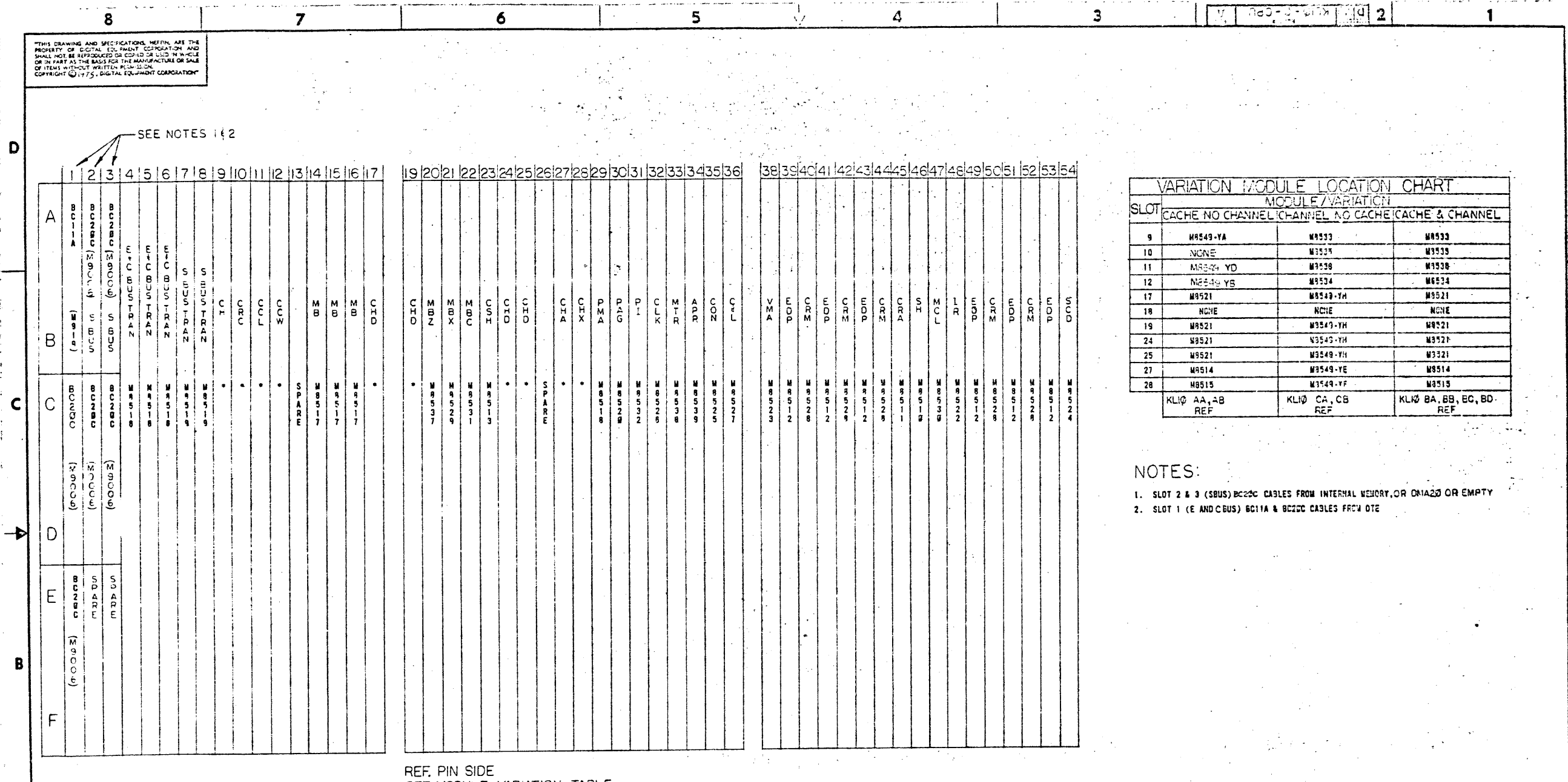


DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			QUANTITY VARIATION																
PARTS LIST																			
MADE BY M. PASCARELLI		CHECKED <i>J. G. Lee</i>	SECTION																
DATE 1 NOVEMBER 1976		DATE 4 1330 76																	
ENG <i>S. M. ...</i>		PROD <i>W. ...</i>	ISSUED SECT.																
DATE 12/28/76		DATE 12/28/76																	
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION																	
1	D-UA-M8521-0-0	CACHE DATA		4															
2	D-UA-M8515-0-0	CACHE EXTENSION		1															
3	D-UA-M8514-0-0	CACHE DIRECTORY		1															
TITLE CACHE UPGRADE KIT (KL10-C)			ASSY NO. B-DD-MCA20-0		SIZE CODE A PL		NUMBER MCA20-0-0				REV.		ECO NO						
			SHEET 1 OF 1		DIST.														

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REF. PIN SIDE
* SEE MODULE VARIATION TABLE

VARIATION MODULE LOCATION CHART

SLOT	CACHE NO	CHANNEL	CHANNEL NO	CACHE	CACHE & CHANNEL
9	M9549-VA			M9533	M9533
10	NGNE			M9533	M9533
11	M9549-YD			M9538	M9538
12	M9549-YS			M9534	M9534
17	M9521			M9549-YH	M9521
18	NGNE			NGNE	NGNE
19	M9521			M9549-YH	M9521
24	M9521			M9549-YH	M9521
25	M9521			M9549-YH	M9521
27	M9514			M9549-YE	M9514
28	M9515			M9549-YF	M9515

KL10 AA, AB REF KL10 CA, CB REF KL10 BA, BB, BC, BD REF

NOTES:

- SLOT 2 & 3 (SBUS) BC22C CABLES FROM INTERNAL MEMORY, OR DMA23 OR EMPTY
- SLOT 1 (E AND CBUS) BC11A & BC22C CABLES FROM DTE

REV.	
CHARGE NO.	A
CHK	KLI0-2-CPU

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

DESCRIPTION	DWG./PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		
QUANTITY & VARIATION		
TITLE: MODULE UTILIZATION (CPU)		
MATERIAL	0-1A-KLI0-0-0	SIZE CODE: D
SCALE		NUMBER: KL10-2-CPU
FINISH		REV: 1

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

The following are the procedural steps in upgrading a non-cache 20 system to a cached 20 system. It is necessary to follow these steps in order.

Test equipment required:

- 1) Digital Voltmeter accuracy $\pm 0.05\%$ or better DC voltages.
 - 2) Oscilloscope (Teletronic type 465, 475, 7000 series, or equivalent).
 - 3) 3 Probes of equal length.
- 1) Run all system diagnostics at CR0, CS0 (25 MHz) and CR0, CS1 (28 MHz). Follow Appendix A. If any failures occur in this step, problems must be resolved before continuing the upgrade procedure.

2) Power system down and remove the following modules:

M8549YH	Slot 17
M8549YH	Slot 19
M8549YH	Slot 24
M8549YH	Slot 25
M8549YV	Slot 27
M8549YF	Slot 28

3) Install the following modules:

M8521	Slot 17
M8521	Slot 19
M8521	Slot 24
M8521	Slot 25
M8514	Slot 27
M8515	Slot 28

Reference documentation for Steps 2 and 3.

KL10 - C/VOL. 2
Print KL10-0-CPU
Module Utilization (CPU)

4) Add C backpanel wire from 4E43A1 to 4D44E1 (cache available).

5) Power up system and check all DC power in entire system at this point with digital voltmeter.

DC (TTL) voltage tolerance (Measured at module power) (pins.)	$+5.0 + \text{or} -0.025 \text{ volts}$ $-5.0 + \text{or} -0.025 \text{ volts}$ $-15.0 + \text{or} -0.075 \text{ volts}$ $+20.0 + \text{or} -0.100 \text{ volts}$	$\pm 5\%$
DC (ECL) Voltage tolerance (Measure at sense tabs on) (CPU Backplane.)	$-5.2 + \text{or} -.050 \text{ volts}$ $-2.7 + \text{or} -.050 \text{ volts}$	$\pm 1\%$

SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

- 6) Check timing following the MA20/MB20/RH20 adjustment procedure accompanying this document: Appendix B. If any timing is not within $\pm 1.0 \text{ Nsec}$ of 50% points on the waveform, readjust to within $\pm 1.0 \text{ Nsec}$ before continuing with upgrade procedure.
- 7) Rerun all CPU, memory and system diagnostics as listed in Appendix A.
- 8) Run DFKPB (instruction timing test) at CR0, CS0 (25 MHz) and compare the output with the accompanying document Appendix C. The times should differ only in the least significant digit.

SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

Appendix A

CPU Tests

- 1) DGKAA - E BOX test #1
- 2) DGKAB - E BOX test #2
- 3) DGKAB - M BOX test #1
- 4) DGKBB - Memory Control Test
- 5) DGABC - Paging Logic Test
- 6) DGMCA - Cache Option Test
- 7) DGMCB - Ram Banger test
- 8) DGKBD - Channel Logic test
- 9) DGKBE - Channel Loopback test
- 10) DGKCA - Meter Board Test
- 11) DFKR - Cache Reliability
- 12) DFKAA - Basic instruction test #1
- 13) DFKAB - Basic instruction test #2
- 14) DFKAC - Basic instruction test #3
- 15) DFKBA - Basic Instruction Reliability
- 16) DFKCA - Advanced Instructions
- 17) DFKDA - CPU/PI/Memory Reliability
- 18) DFKEA - Paging Hardware
- 19) DFKEB - MUUO and User Mode Test
- 20) DFKAD - Basic instruction test #4

INT: 20 Tests

- 1) DGDTE - Basic DTE test
- 2) DFDTE - DTE Reliability test

DMA20/MA20/MB20 Tests

- 1) DDMMD - Memory Exerciser
- 2) DDMNE - BLT test
- 3) DDMNF - Floating Ones & Zeros test
- 4) DDMNG - Memory Exerciser (Over 256K)
- 5) MARGN.CMD - Auto Memory Margins

LP20 Test

- 1) DZLPL - LP20 Logic & Printer Test

RH20 Tests

- 1) DFRHB - Tests RH20's - does not use any mass bus devices.
- 2) DFSXA - System 20 exerciser - tests RH20's with or without mass bus devices.

TU45/TN02 Tests

- 1) DFRHP - RH20 Fault Isolator
- 2) DFTUE - TU45 Device test
- 3) DFTUF - TU45 Multi-Device test

SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

Appendix A (Continued)

RP04/RP05/RP06 Tests

- 1) DFRPH - RP04 Device Test
- 2) DFRPJ - RP05 Device Test
- 3) DFRPK - RP06 Device Test
- 4) DDRPI - RP04/RP05/RP06 Reliability Test

SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

ENGINEERING SPECIFICATION **000000** CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

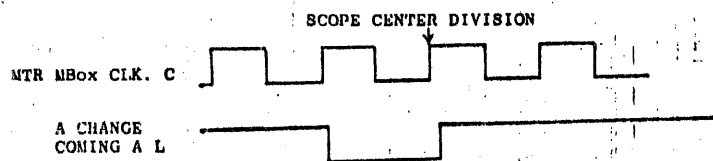
APPENDIX B

MA20 DESKEW PROCEDURE

- Notes:
1. Use equal length probes with short ground clips.
 2. Select CS0, CR0, (25MHz) on KL10.
 3. The M8562 delay lines are arranged so that (A) clock is the top pot and (B) clock is the bottom pot.
 4. A 7000 series or equivalent scope should be used when deskewing the MA20.
 5. The scope sweep rate should be 5ns or less per CM.

MA20 DESKEW PROCEDURE (ON LINE)

1. Attach Channel A probe to Pin 4D33P1. The signal name is: MTR MBox Clk. C.
2. Attach Channel B to 4E22F2. The signal name is: A Change Coming A L. Set the scope to alternate trace.
3. Observe on the scope the relationship of the MTR MBox Clk. C to A Change Coming A L.
4. See the figure below. Set the signal position accordingly.
5. Now move Channel B probe to Pin 5D26A1. Adjust the upper delay line on the M8562 in EF0 of the MA20 so that the leading edge 50 percent point crosses the previously set center division on the scope screen.
6. Now move Channel B probe to 5D29A1. Adjust the delay line on the M8562 in slot EF54 as in Step 5.
7. Next, move Channel B probe to Pin 5D26K1. Adjust the lower M8562 delay line in EF01 so that the leading edge aligns with the third MTR MBox Clk. C from which the clocks were previously aligned. Center the clock on a scope division line. Now align leading edges.
8. Now move Channel B Probe to 5D29K1. Adjust Clocks as in Step 7 for the M8562 in Slot EF54.



SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

ENGINEERING SPECIFICATION **000000** CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

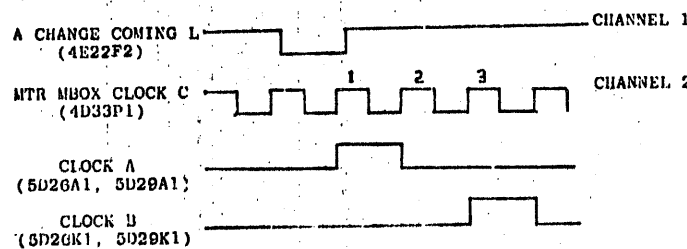
APPENDIX B

MU20 DESKEW PROCEDURE

- Notes:
1. Use equal length probes with short ground clips.
 2. Select clock rate 0 on KL10 (for on line deskew procedure).
 3. The M8565 delay lines are arranged so that (A) clock is the top pot and (B) clock is the bottom pot.
 4. A 7000 series or equivalent scope should be used when deskewing the MU20.
 5. The scope sweep rate should be 5ns or less per CM.

MU20 DESKEW PROCEDURE (ON LINE)

1. Set clock rate to "CR0", clock "source" to "CS0", Type "FX1" to turn the clock on.
2. Place channel 1 probe on Pin 4E22F2 "A Change Coming A L", sync on channel 1.
3. Place channel 2 probe on Pin 4D33P1 "MTR MBox clock C".
4. Align the rising edge of the pulse designated as 1, so that the 50% point crosses the second vertical division of the scope screen. Note this position.
5. Place channel 2 probe on Pin 5D26A1. Adjust the top delay on the M8565, slot 5EF01 so that the leading edge 50% point crosses the second vertical division of the scope screen.
6. Place channel 2 probe on Pin 5D29A1. Adjust the top delay on the M8565, slot 5EF01 so that the leading edge 50% point crosses the second vertical division of the scope screen.
7. Replace channel 2 probe on Pin 4D33P1 "MTR MBox Clock C".
8. Align the leading edge of the pulse designated as 3, so that the 50% point crosses the nearest vertical division mark of the scope screen. Note this position.
9. Place Channel 2 probe on Pin 5D26K1. Adjust the bottom delay on the M8565, Slot 5EF01 so that the leading edge 50% point crosses the vertical division. Mark note in Step 8.
10. Place Channel 2 probe on Pin 5D29K1. Adjust the bottom delay on the M8565, Slot 5EF54 so that the leading edge 50% point crosses the vertical division. Mark Note in Step 8.



SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

ENGINEERING SPECIFICATION **000000** CONTINUATION SHEET

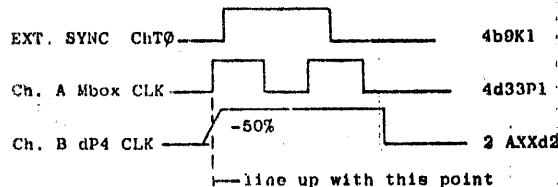
TITLE CACHE UPGRADE PROCEDURE

APPENDIX B

RII20 DESKEW PROCEDURE

Use a 475 or a 4 trace scope. All the RII20's are deskewed to MBOX CLK that produces CHT0 in the channel. Recheck skew whenever the CBUS cable or M8566 board is replaced. The pots to be adjusted are on the M8569 board. The top pot is for RII20 #0, second pot for RII20 #1 etc.

- 1) Load Micro Code. Set CS0-CR0, FX1.
- 2) Sync Positive - External sync on 4B0K1 --- Ch T0 H -- (Ch C1).
- 3) Ch A on 4D33P1 - MBOX CLK H - (MTR 2).
- 4) Ch B on 2 AXXD2 - DP1 CLK H - (DP4).
- 5) Align 1 AXXD2 with the 50% point of the MBOX CLK that happens approximately 10 ns before the CHT0 CLK.



RII20	PIN #
0	2 A30D2
1	2 A33D2
2	2 A30D2
3	2 A27D2
4	2 A24D2
5	2 A21D2
6	2 A18D2
7	2 A15D2

SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

ENGINEERING SPECIFICATION **000000** CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

APPENDIX C

Appendix C
PDP-10 ALIO INSTRUCTION TIMING TEST (DFKFB)
VERSION 0.1, SV=0.11, CPU#0, MCV=126, MCO=0, MO=30, 60HZ
SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE + FULL, AC BLK 0, CACHE: 0 1 2 3

- 1 - BASIC CLOCK CYCLE IS 40 NSEC.
- 2 - INDEXING TAKES 40 NSEC.
- 3 - INDIRECT TAKES 280 NSEC.
- 4 - INDEXING AND INDIRECT TAKES 320 NSEC.
- 5 - MOVEI TAKES 320 NSEC.
- 6 - MOVE FROM AC TAKES 440 NSEC.
- 7 - MOVE FROM MEMORY TAKES 480 NSEC.
- 8 - HRR FROM MEMORY TAKES 520 NSEC.
- 9 - SETOM 0 TAKES 560 NSEC.
- 10 - JHST TAKES 360 NSEC.
- 11 - JSR TAKES 680 NSEC.
- 12 - PUSHJ TAKES 840 NSEC.
- 13 - ADD FROM MEMORY TAKES 520 NSEC.
- 14 - MUL (8 ADD/SUB - 18 SHIFTS) TAKES 2.52 USEC.
- 15 - DIV TAKES 5.58 USEC.
- 16 - FIX A FLOATING POINT ONE TAKES 1.04 USEC.
- 17 - FITR AN INTERGER ONE TAKES 1.84 USEC.
- 18 - FAD (1 RIGHT SHIFT) TAKES 1.88 USEC.
- 19 - FAD (8 SHIFT RIGHT - 3 LEFT) TAKES 2.16 USEC.
- 20 - FMP (7 ADD/SUB - 14 SHIFTS) TAKES 2.40 USEC.
- 21 - FDV TAKES 5.72 USEC.
- 22 - DMOVE FROM MEMORY TAKES 880 NSEC.
- 23 - DFAD (1 RIGHT SHIFT) TAKES 2.44 USEC.
- 24 - DFAD (8 SHIFT RIGHT - 1 LEFT) TAKES 2.44 USEC.
- 25 - DFMP (7 ADD/SUB - 32 SHIFTS) TAKES 4.92 USEC.
- 26 - DFV TAKES 10.32 USEC.
- 27 - CONO PI TAKES 1.92 USEC.
- 28 - CONI PI TAKES 3.36 USEC.
- 29 - DATAO APR TAKES 1.56 USEC.
- 30 - DATAI APR TAKES 1.76 USEC.
- 31 - MOVE TO MEMORY TAKES 680 NSEC.
- 32 - LOGICAL SHIFT (35 PLACES LEFT) TAKES 640 NSEC.
- 33 - LOGICAL SHIFT (35 PLACES RIGHT) TAKES 760 NSEC.
- 34 - LOGICAL SHIFT COMBINED (71 PLACES LEFT) TAKES 1.12 USEC.
- 35 - LOGICAL SHIFT COMBINED (71 PLACES RIGHT) TAKES 1.16 USEC.
- 36 - INCREMENT BYTE POINTER TAKES 1.00 USEC.
- 37 - INCREMENT AND LOAD BYTE TAKES 1.44 USEC.
- 38 - INCREMENT AND DEPOSIT BYTE TAKES 1.80 USEC.
- 39 - JFCL TAKES 880 NSEC.
- 40 - CAI TAKES 480 NSEC.
- 41 - JUMP TAKES 480 NSEC.
- 42 - CAM TAKES 600 NSEC.
- 43 - EQV AC TO AC TAKES 480 NSEC.
- 44 - EQV MEMORY TO AC TAKES 520 NSEC.
- 45 - SETOD TAKES 680 NSEC.
- 46 - AOS TO MEMORY TAKES 840 NSEC.

SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

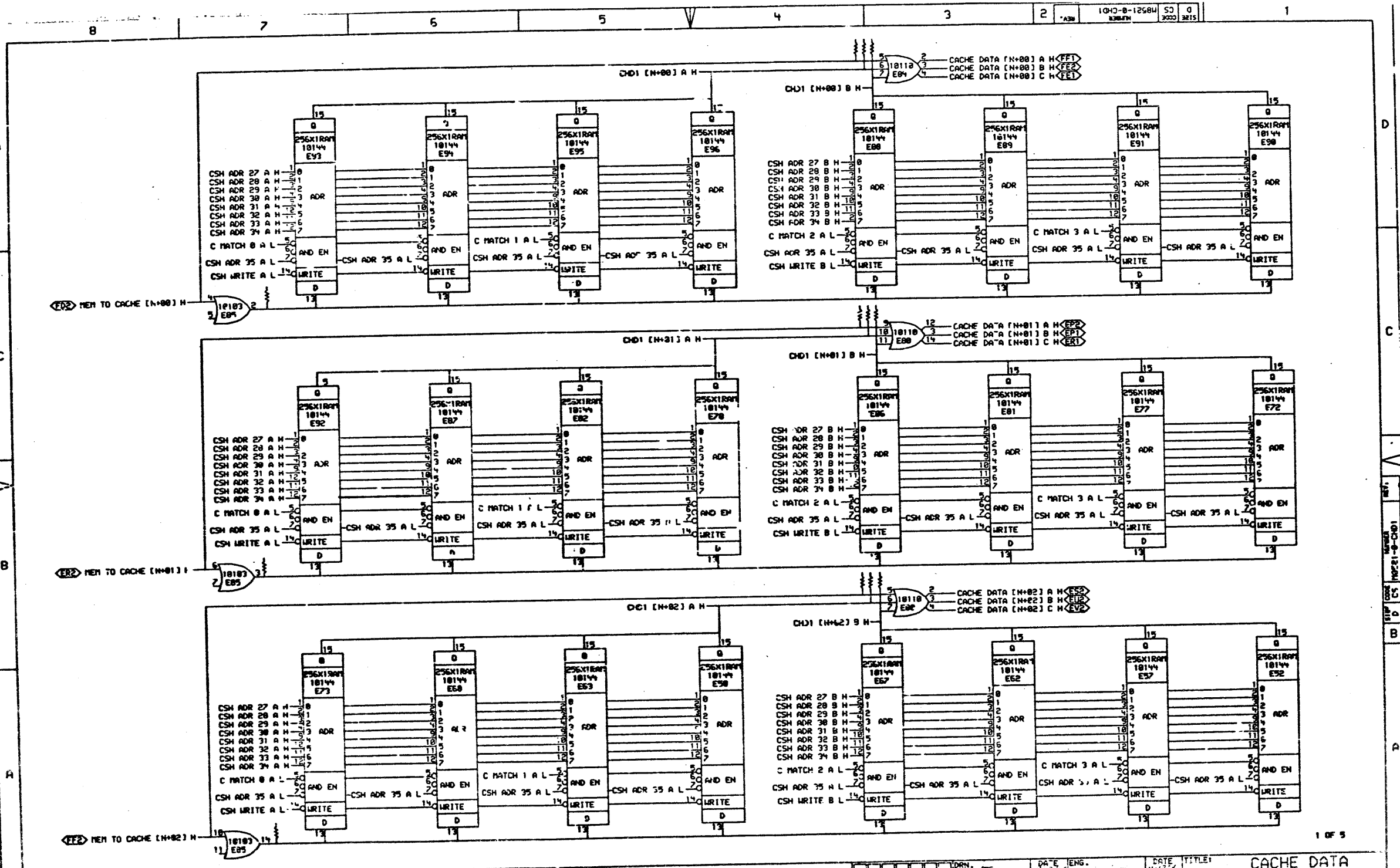
TITLE CACHE UPGRADE PROCEDURE

APPENDIX C (Continued)

- 47 - EXCHANGE AN AC WITH AN AC TAKES 640 NSEC.
- 48 - EXCHANGE AN AC WITH MEMORY TAKES 840 NSEC.
- 49 - EXECUTE TAKES 640 NSEC.
- 50 - BLT MEMORY TO MEMORY TAKES 1.92 USEC.
- 51 - BLT AC TO MEMORY TAKES 1.88 USEC.
- 52 - DATAI TAKES 10.00 USEC.
- 53 - DATAO TAKES 10.00 USEC.

TEST COMPLETED

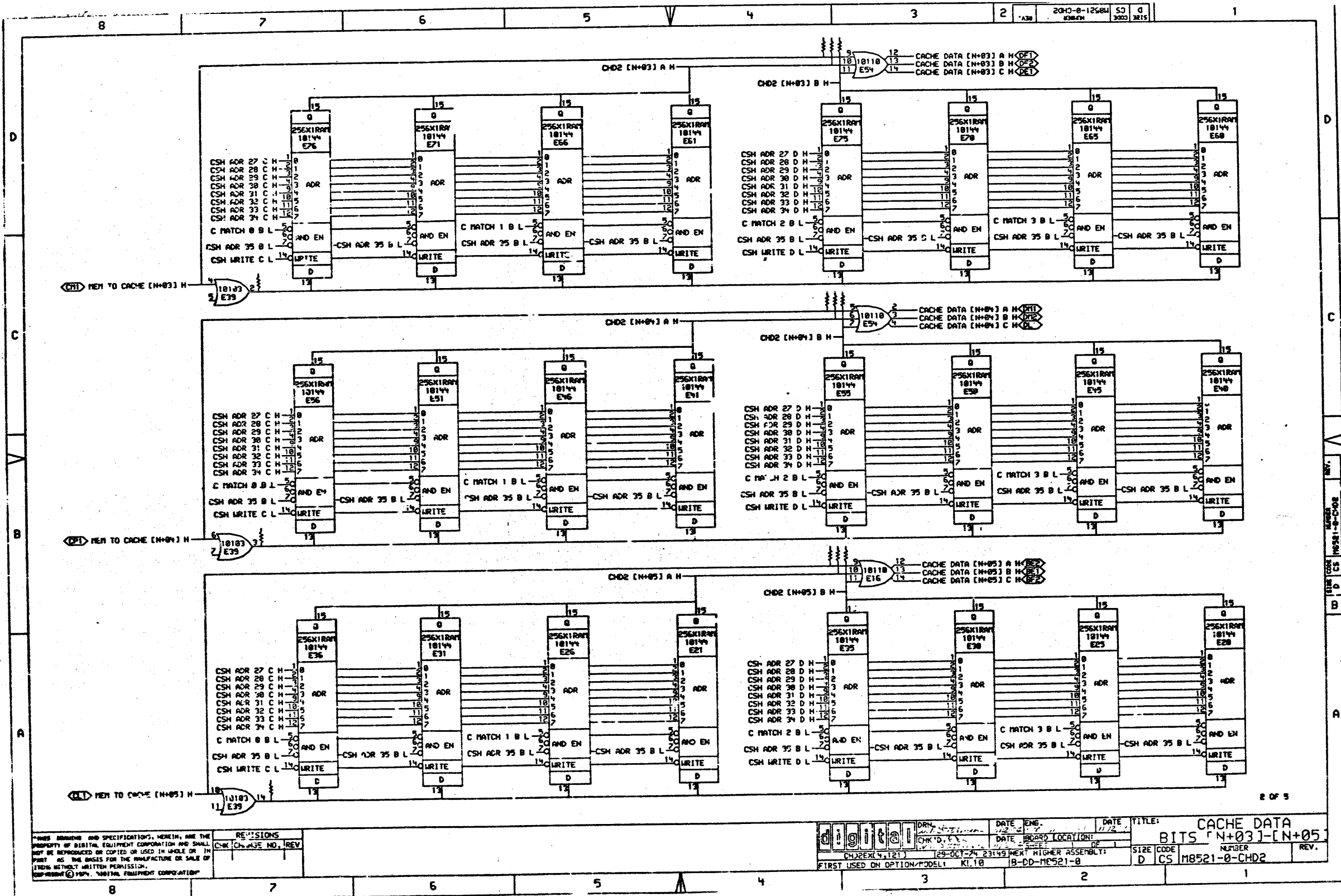
SIZE	CODE	NUMBER	REV
A	SF	MCA20-0-2	



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REVISIONS	
CHK	CHANGE NO. REV.

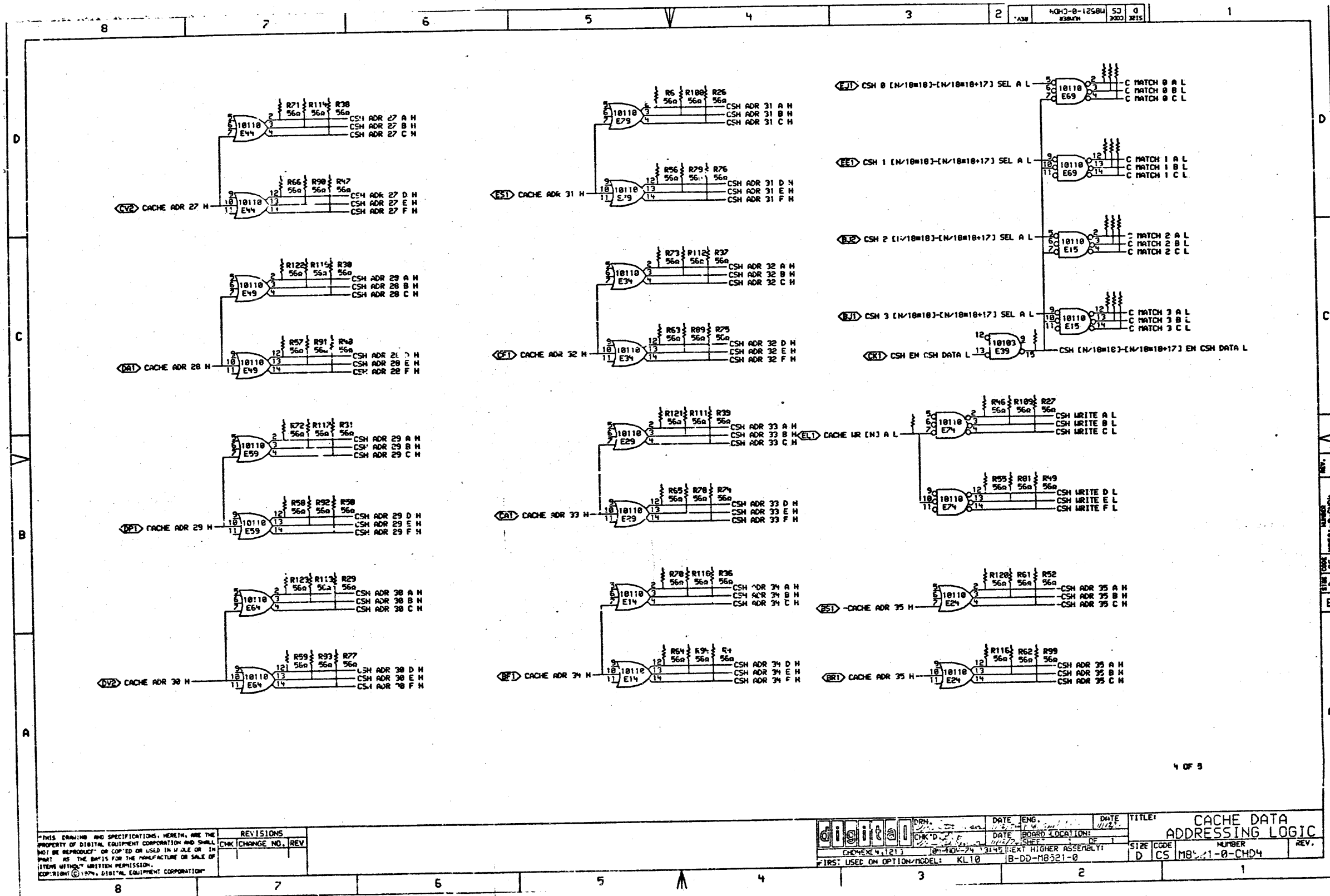
digital DRN. _____ DATE _____ ENG. _____ DATE _____ BOARD LOCATION _____ DATE _____ SPEED _____ OF _____ CH01EV4.1311 12-04-74 23146 NEXT HIGHER ASSEMBLY 1	TITLE: CACHE DATA BITS [N]-[N+02]	
	SIZE (CODE) _____ NUMBER _____ REV. _____	D ICS 118521-0-CHD1



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REV.	DESCRIPTION	CHK.	DATE
1	CH 435 NO. 1		

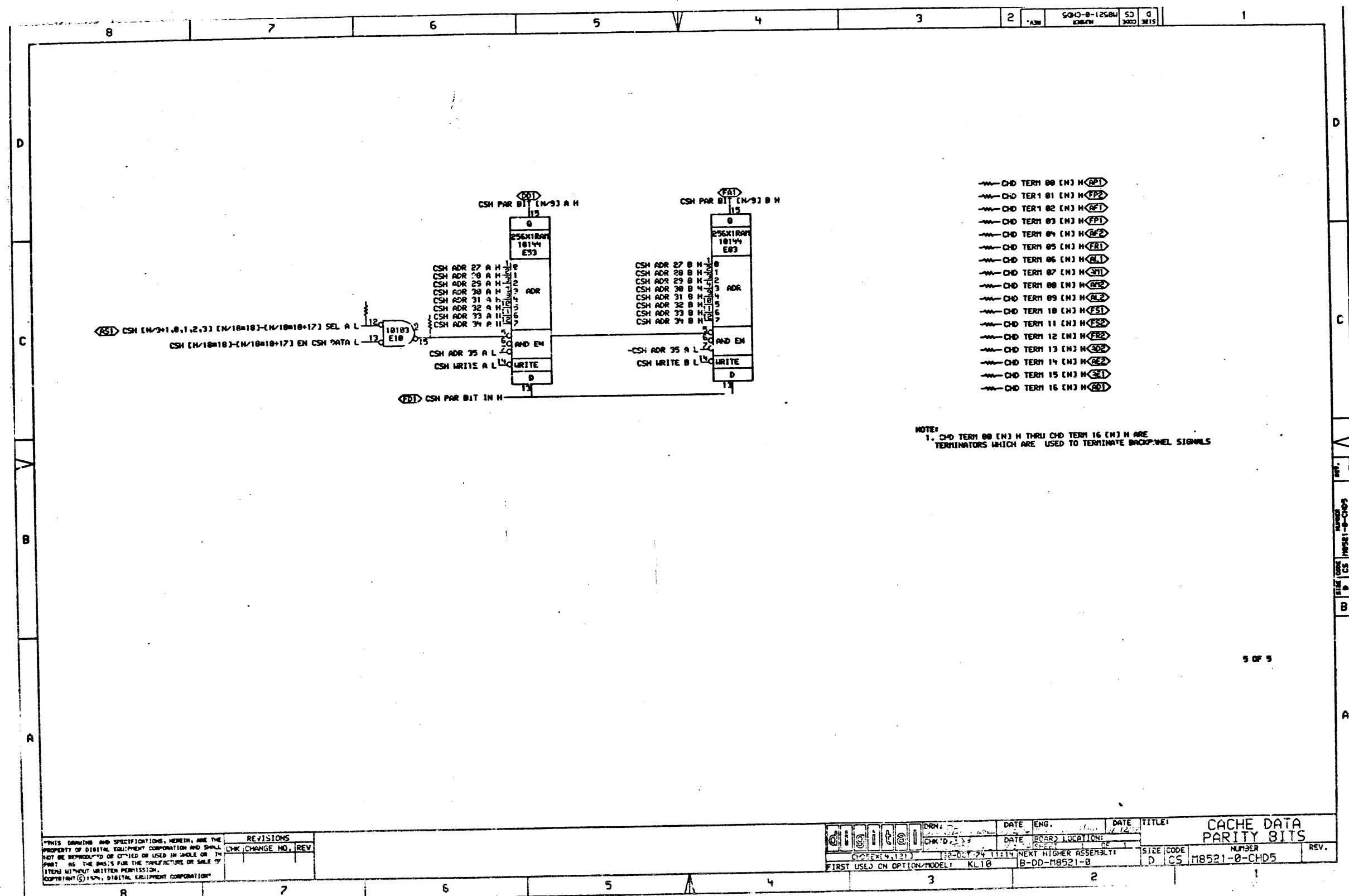
DRN.	DATE ENG.	DATE	TITLE:
CHK'D.	DATE	11/72	CACHE DATA BITS [N+03]-[N+05]
CH 202 (4, 12)	129-OCT-74 23149		NUMBER
FIRST USED ON OPTION/MODEL	KI.10	18-DD-ME521-0	REV.
			D CS M8521-0-CHD2



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REVISIONS	
CHK	CHANGE NO. REV

	DRN.	DATE	ENG.	DATE	TITLE
	CHK'D	DATE	BOARD LOCATION	SHEET	OF
CHECKED 4, 12, 73		10-14-74	13145	REX	HIGHER ASSEMBLY:
FIRST USE ON OPTION/MODEL: KL10		B-DD-MB321-0		SIZE CODE	NUMBER
				D CS MB321-0-CHD4	REV.



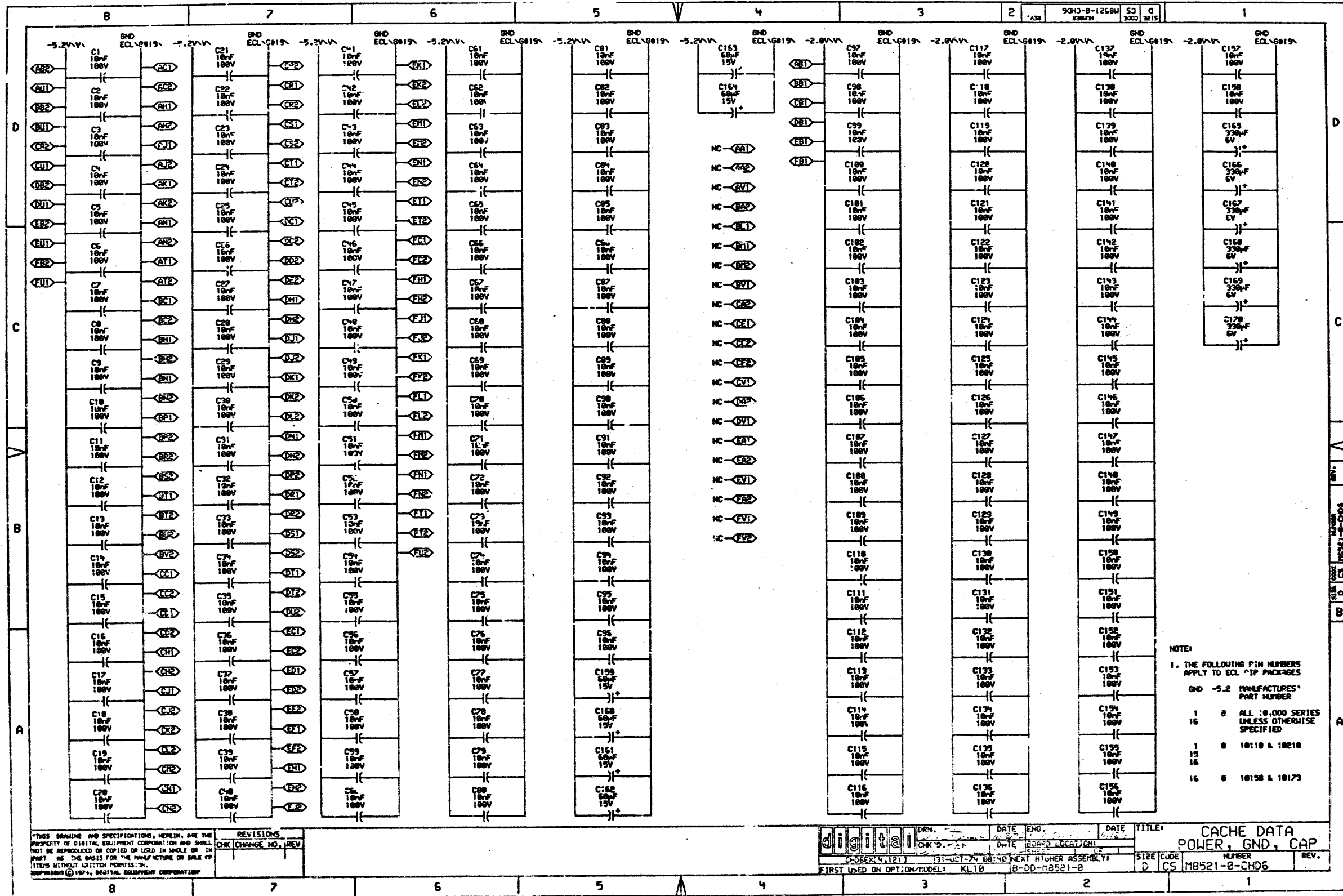
5 OF 5

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REVISIONS	
CHK	CHANGE NO. REV

DATE	ENG.	DATE	TITLE
12-02-74		12-12-74	CACHE DATA PARITY BITS
DATE	ISSUED	LOCATION	
12-02-74	1114	NEXT HIGHER ASSEMBLY	
FIRST USED ON OPTION/MODEL		KL10	B-DD-M8521-0
SIZE	CODE	NUMBER	REV.
D	CS	M8521-0-CHD5	

FILE NO. CS M8521-0-005
 REV. B



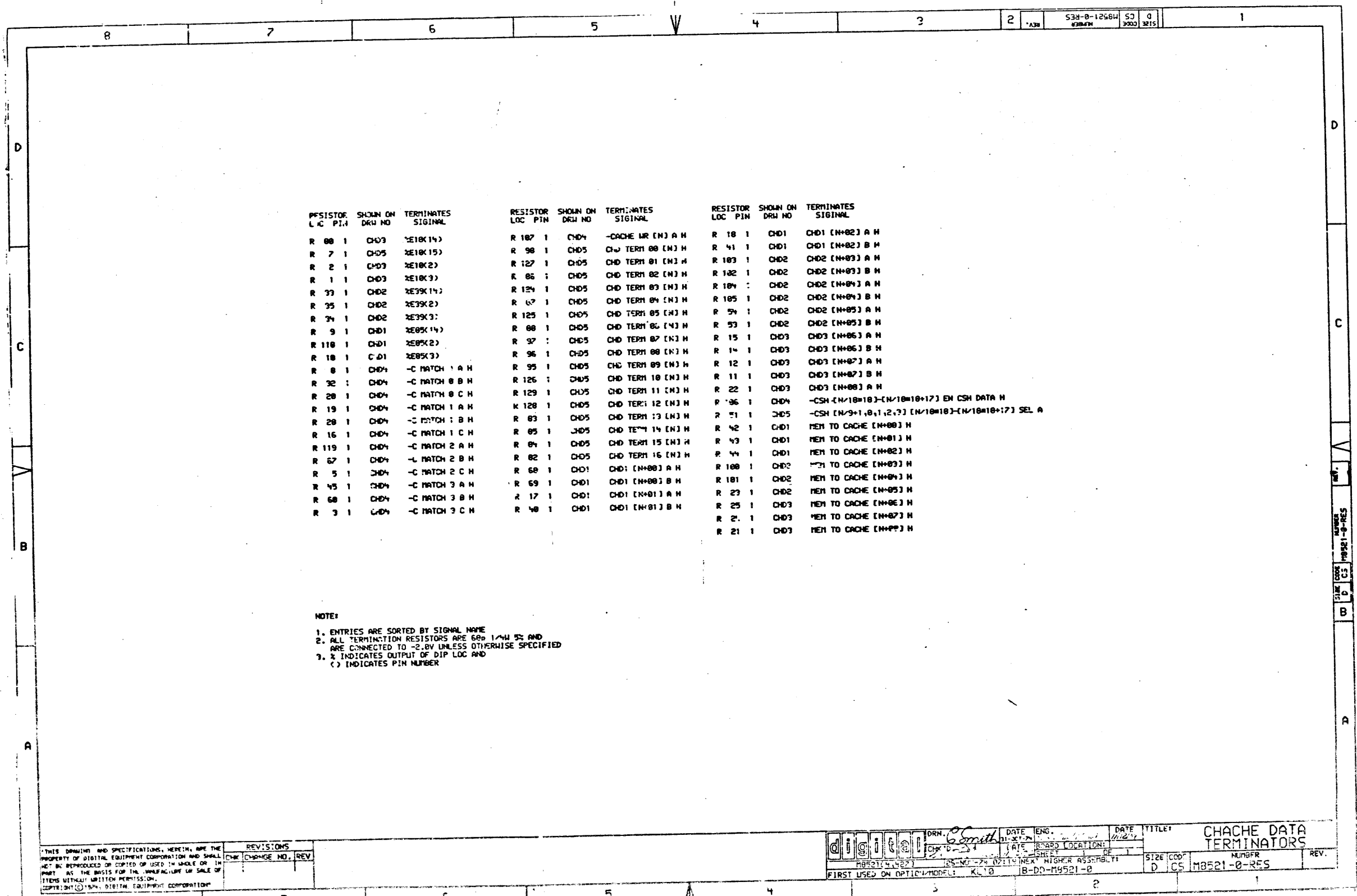
NOTE:
 1. THE FOLLOWING PIN NUMBERS APPLY TO ECL CHIP PACKAGES

GND	-5.2	MANUFACTURER'S PART NUMBER
1	8	ALL 10,000 SERIES UNLESS OTHERWISE SPECIFIED
15	8	10110 & 10210
16	8	10150 & 10173

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REVISIONS	
CHK	CHANGE NO. / REV

digital	DRN	DATE	ENG.	DATE	TITLE
	CHK'D	DATE	BOARD LOCATION		CACHE DATA POWER, GND, CAP
CHGGR: 4.121	131-027-27	08:10	NEAT HIGHER ASSEMBLY	SIZE	CODE
FIRST USED ON OPT. ON MODEL: KL10	8-DD-M8521-0			D	CS
				NUMBER	REV.
				M8521-0-CHD6	



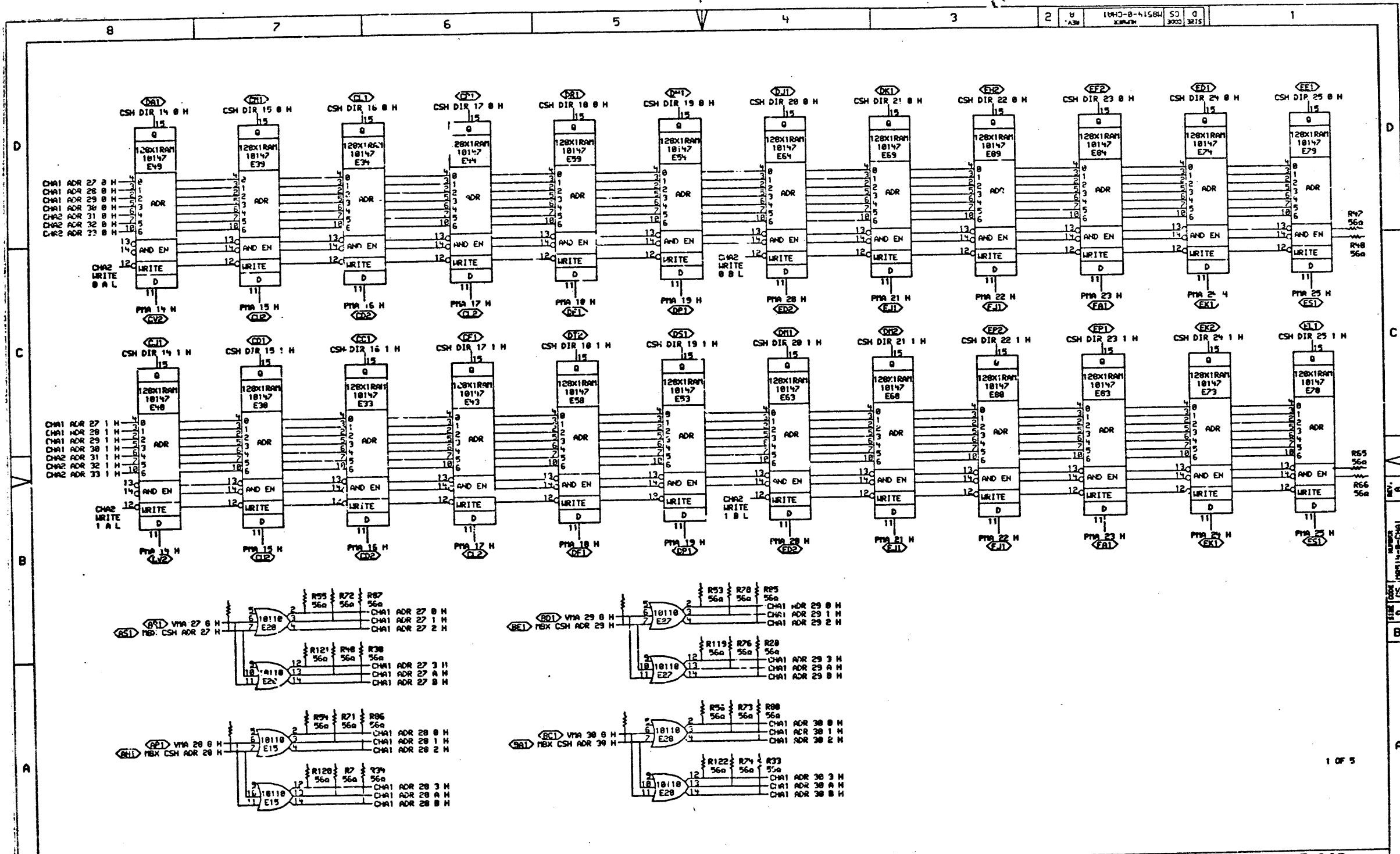
RESISTOR LOC PIN	SHOWN ON DRW NO	TERMINATES SIGNAL	RESISTOR LOC PIN	SHOWN ON DRW NO	TERMINATES SIGNAL	RESISTOR LOC PIN	SHOWN ON DRW NO	TERMINATES SIGNAL			
R 00	1	CH3	XE10K14	R 107	1	CH4	-CACHE LR (N) A H	R 18	1	CH1	CH1 (N+02) A H
R 7	1	CH5	XE10K15	R 98	1	CH5	CH TERM 00 (N) H	R 41	1	CH1	CH1 (N+02) B H
R 2	1	CH3	XE10K2	R 127	1	CH5	CHD TERM 01 (N) H	R 103	1	CH2	CH2 (N+03) A H
R 1	1	CH3	XE10K3	R 85	1	CH5	CHD TERM 02 (N) H	R 102	1	CH2	CH2 (N+03) B H
R 33	1	CH2	XE39K14	R 124	1	CH5	CHD TERM 03 (N) H	R 104	1	CH2	CH2 (N+04) A H
R 35	1	CH2	XE39K2	R 67	1	CH5	CHD TERM 04 (N) H	R 105	1	CH2	CH2 (N+04) B H
R 24	1	CH2	XE39K3	R 125	1	CH5	CHD TERM 05 (N) H	R 54	1	CH2	CH2 (N+05) A H
R 9	1	CH1	XE85K14	R 00	1	CH5	CHD TERM 06 (N) H	R 53	1	CH2	CH2 (N+05) B H
R 110	1	CH1	XE85K2	R 37	1	CH5	CHD TERM 07 (N) H	R 15	1	CH3	CH3 (N+06) A H
R 10	1	CH1	XE85K3	R 96	1	CH5	CHD TERM 08 (N) H	R 14	1	CH3	CH3 (N+06) B H
R 0	1	CH4	-C MATCH 1 A H	R 95	1	CH5	CHD TERM 09 (N) H	R 12	1	CH3	CH3 (N+07) A H
R 32	1	CH4	-C MATCH 0 B H	R 126	1	CH5	CHD TERM 10 (N) H	R 11	1	CH3	CH3 (N+07) B H
R 20	1	CH4	-C MATCH 0 C H	R 129	1	CH5	CHD TERM 11 (N) H	R 22	1	CH3	CH3 (N+08) A H
R 19	1	CH4	-C MATCH 1 A H	K 128	1	CH5	CHD TERM 12 (N) H	R 36	1	CH4	-CSH (N/18+18)-(N/18+17) EN CSH DATA H
R 20	1	CH4	-C MATCH 1 B H	R 83	1	CH5	CHD TERM 13 (N) H	R 51	1	CH5	-CSH (N/9+1,8,1,2,3) (N/18+18)-(N/18+17) SEL A
R 16	1	CH4	-C MATCH 1 C H	R 85	1	CH5	CHD TERM 14 (N) H	R 42	1	CH1	MEM TO CACHE (N+00) H
R 119	1	CH4	-C MATCH 2 A H	R 84	1	CH5	CHD TERM 15 (N) H	R 43	1	CH1	MEM TO CACHE (N+01) H
R 67	1	CH4	-L MATCH 2 B H	R 82	1	CH5	CHD TERM 16 (N) H	R 44	1	CH1	MEM TO CACHE (N+02) H
R 5	1	CH4	-C MATCH 2 C H	R 60	1	CH1	CH1 (N+00) A H	R 100	1	CH2	MEM TO CACHE (N+03) H
R 45	1	CH4	-C MATCH 3 A H	R 69	1	CH1	CH1 (N+00) B H	R 101	1	CH2	MEM TO CACHE (N+04) H
R 60	1	CH4	-C MATCH 3 B H	R 17	1	CH1	CH1 (N+01) A H	R 23	1	CH2	MEM TO CACHE (N+05) H
R 3	1	CH4	-C MATCH 3 C H	R 40	1	CH1	CH1 (N+01) B H	R 25	1	CH3	MEM TO CACHE (N+06) H
								R 2	1	CH3	MEM TO CACHE (N+07) H
								R 21	1	CH3	MEM TO CACHE (N+08) H

NOTE:
 1. ENTRIES ARE SORTED BY SIGNAL NAME
 2. ALL TERMINATION RESISTORS ARE 600 1/4W 5% AND ARE CONNECTED TO -2, BV UNLESS OTHERWISE SPECIFIED
 3. % INDICATES OUTPUT OF DIP LOC AND () INDICATES PIN NUMBER

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REVISIONS		
CHK	CHANGE NO.	REV

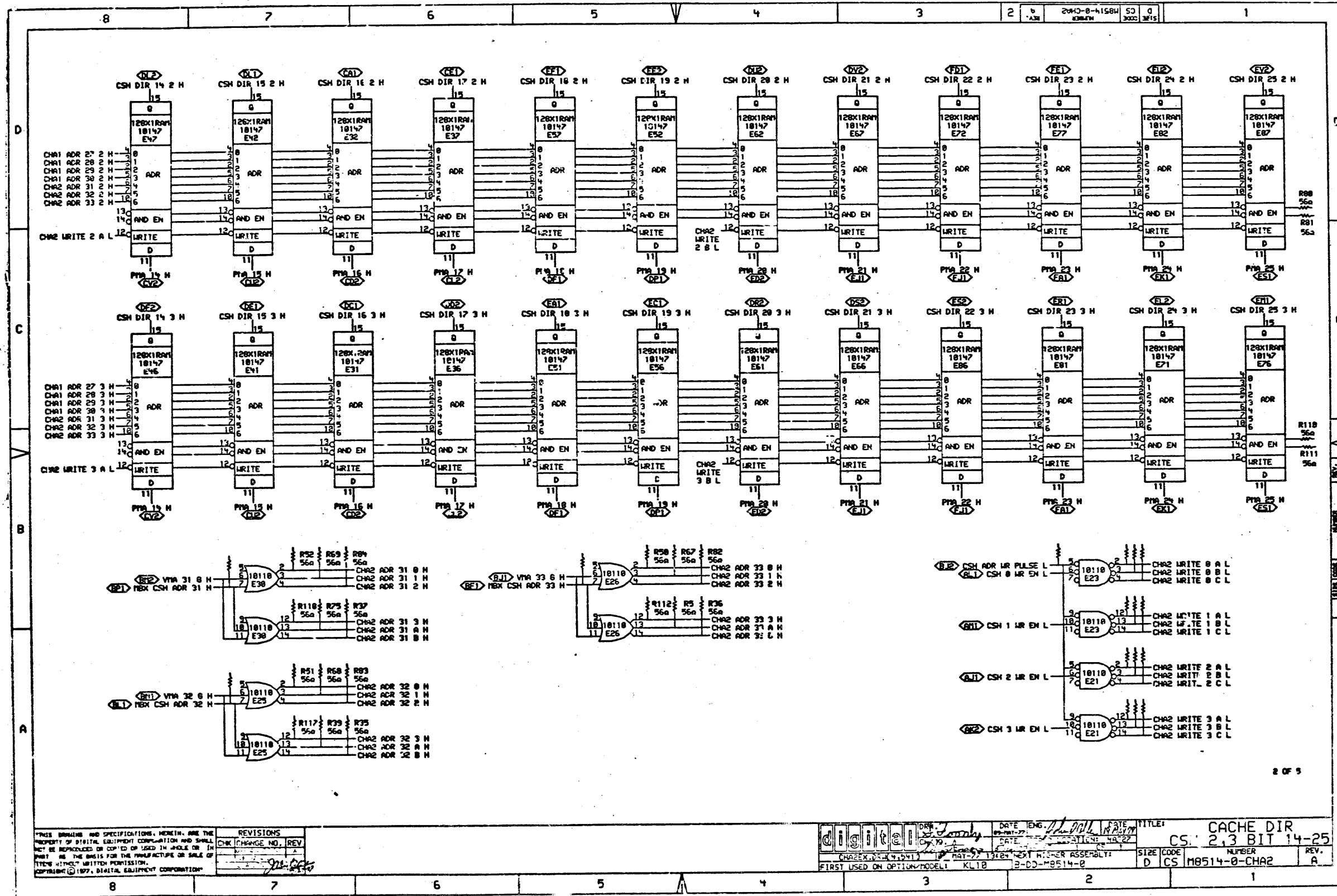
digital	DRN.	DATE	ENG.	DATE	TITLE
	6 Smith	11/15/74		11/15/74	CHACHE DATA TERMINATORS
FIRST USED ON OPTIC-MODEL: KL-10		B-D-D-M9521-0		SIZE	CODE
				D	CS
				NUMBER	REV.
				M9521-0-RES	



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REV. NO.	DESCRIPTION	DATE
1	INITIAL DESIGN	10/11/77
2	REVISED FOR MANUFACTURE	11/15/77
3	REVISED FOR MANUFACTURE	12/15/77
4	REVISED FOR MANUFACTURE	1/15/78
5	REVISED FOR MANUFACTURE	2/15/78
6	REVISED FOR MANUFACTURE	3/15/78
7	REVISED FOR MANUFACTURE	4/15/78
8	REVISED FOR MANUFACTURE	5/15/78

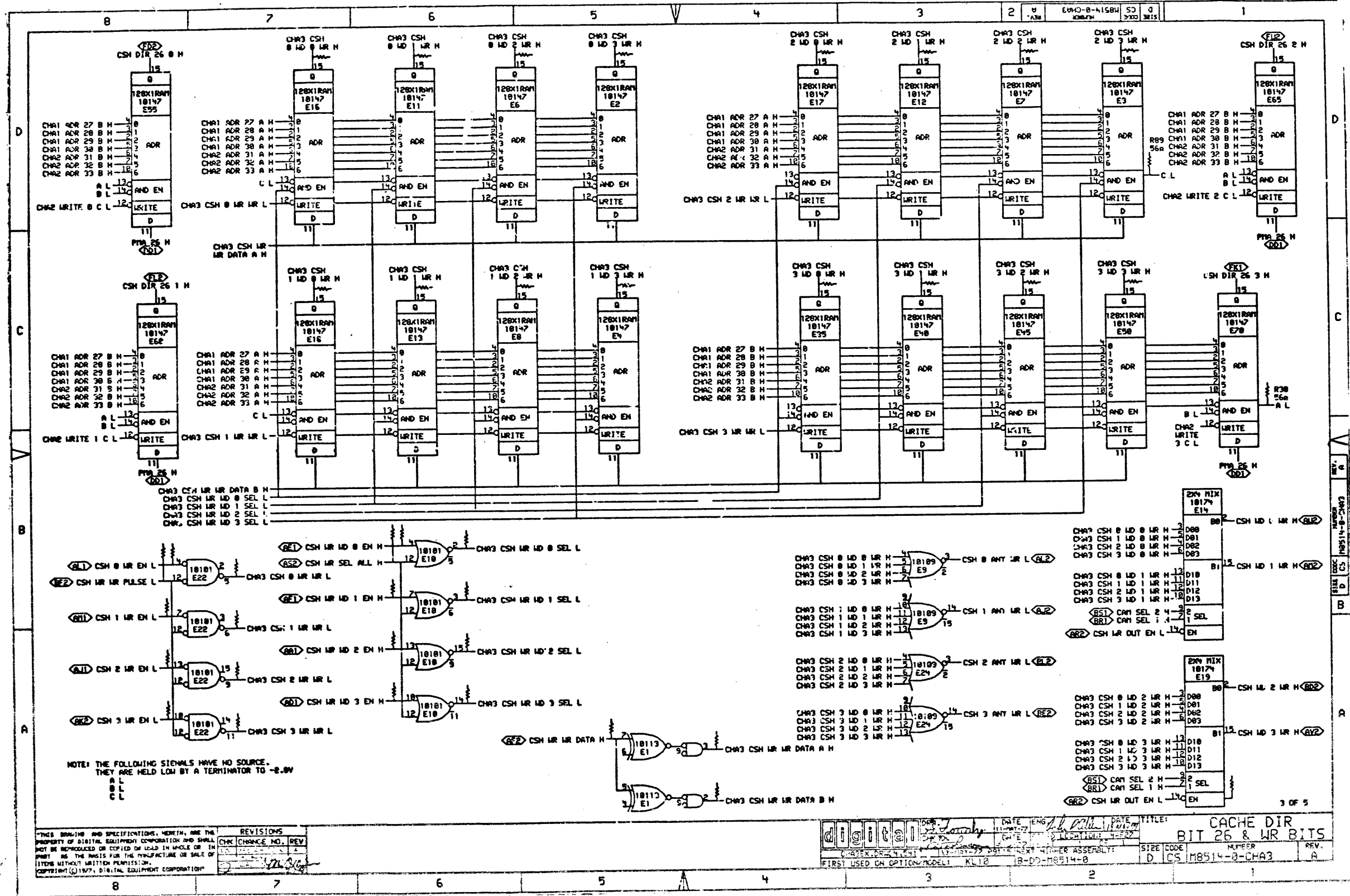
	DATE: 10/11/77 ENG: J. J. O'Neil DESIGNED BY: J. J. O'Neil CHECKED BY: J. J. O'Neil DATE: 11/15/77 DATE: 12/15/77 DATE: 1/15/78 DATE: 2/15/78 DATE: 3/15/78 DATE: 4/15/78 DATE: 5/15/78	TITLE: CACHE DIR CSH 0, 1 BIT 14-25
FIRST USED ON OPTION MODEL: KL18	SIZE CODE: D	NUMBER: M8514-0-CHA1



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REVISIONS	
CHK	CHANGE NO. REV

DATE ENG. <i>Jan 21 1972</i>	DATE <i>1/21/72</i>	FILE # <i>14-25</i>	TITLE CACHE DIR
DATE <i>1/21/72</i>	DATE <i>1/21/72</i>	DATE <i>1/21/72</i>	CS: 2,3 BIT 14-25
DATE <i>1/21/72</i>	DATE <i>1/21/72</i>	DATE <i>1/21/72</i>	SIZE CODE D
DATE <i>1/21/72</i>	DATE <i>1/21/72</i>	DATE <i>1/21/72</i>	NUMBER M0514-0-CHA2
DATE <i>1/21/72</i>	DATE <i>1/21/72</i>	DATE <i>1/21/72</i>	REV. A

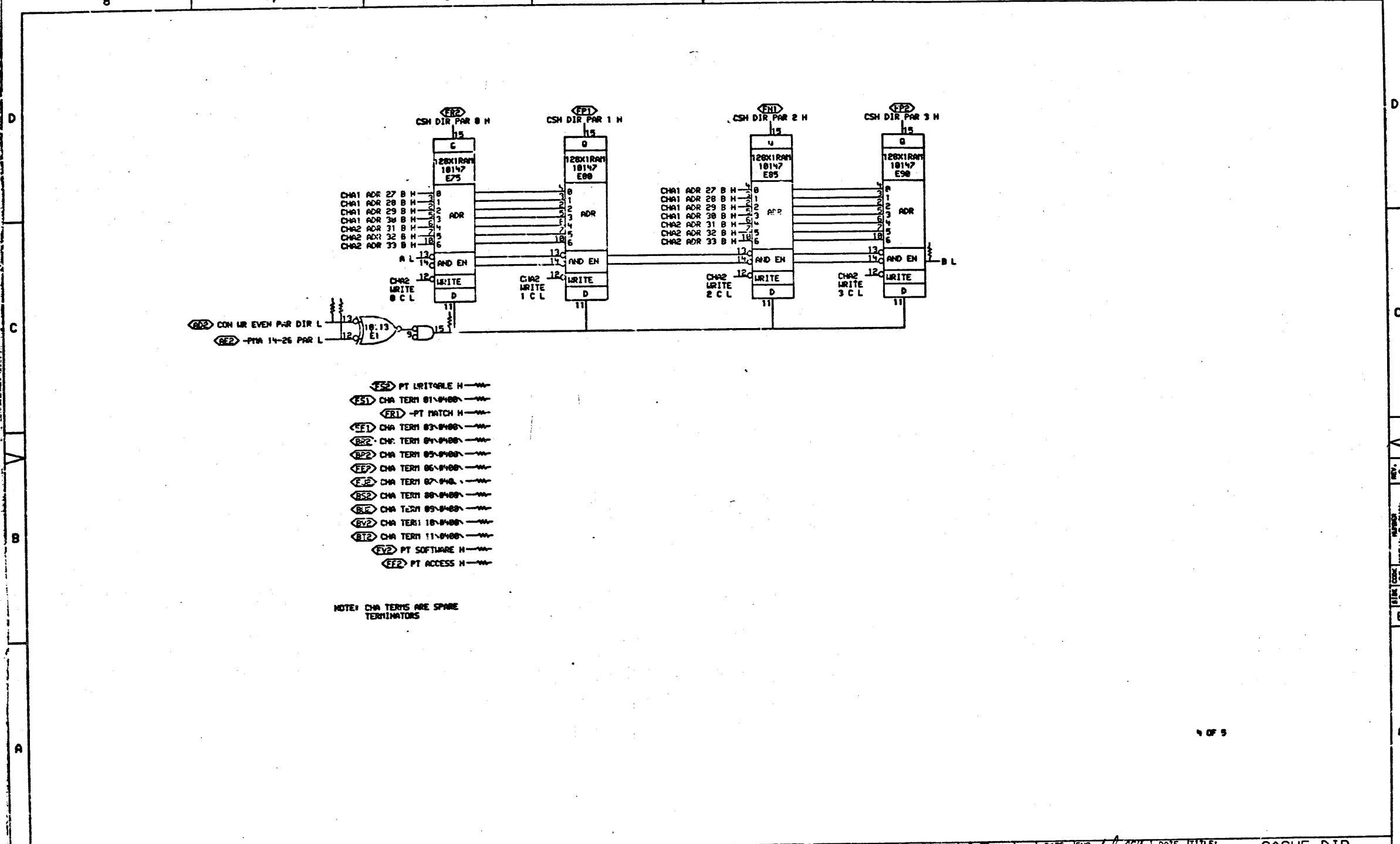


NOTE: THE FOLLOWING SIGNALS HAVE NO SOURCE.
THEY ARE HELD LOW BY A TERMINATOR TO -0.8V

A L
B L
C L

REV.	DESCRIPTION
1	...
2	...

DATE	11-27-77	TITLE	CACHE DIR BIT 26 & WR BITS
DESIGNED BY	J. J. ...	CHECKED BY	...
DATE	...	REV.	A
NUMBER	M8514-0-CHA3	SIZE	D
FIRST USED ON OPTION/MODEL	KL18	PART NUMBER	18-00-M8514-0



NOTE: CHA TERMS ARE SPARE TERMINATORS

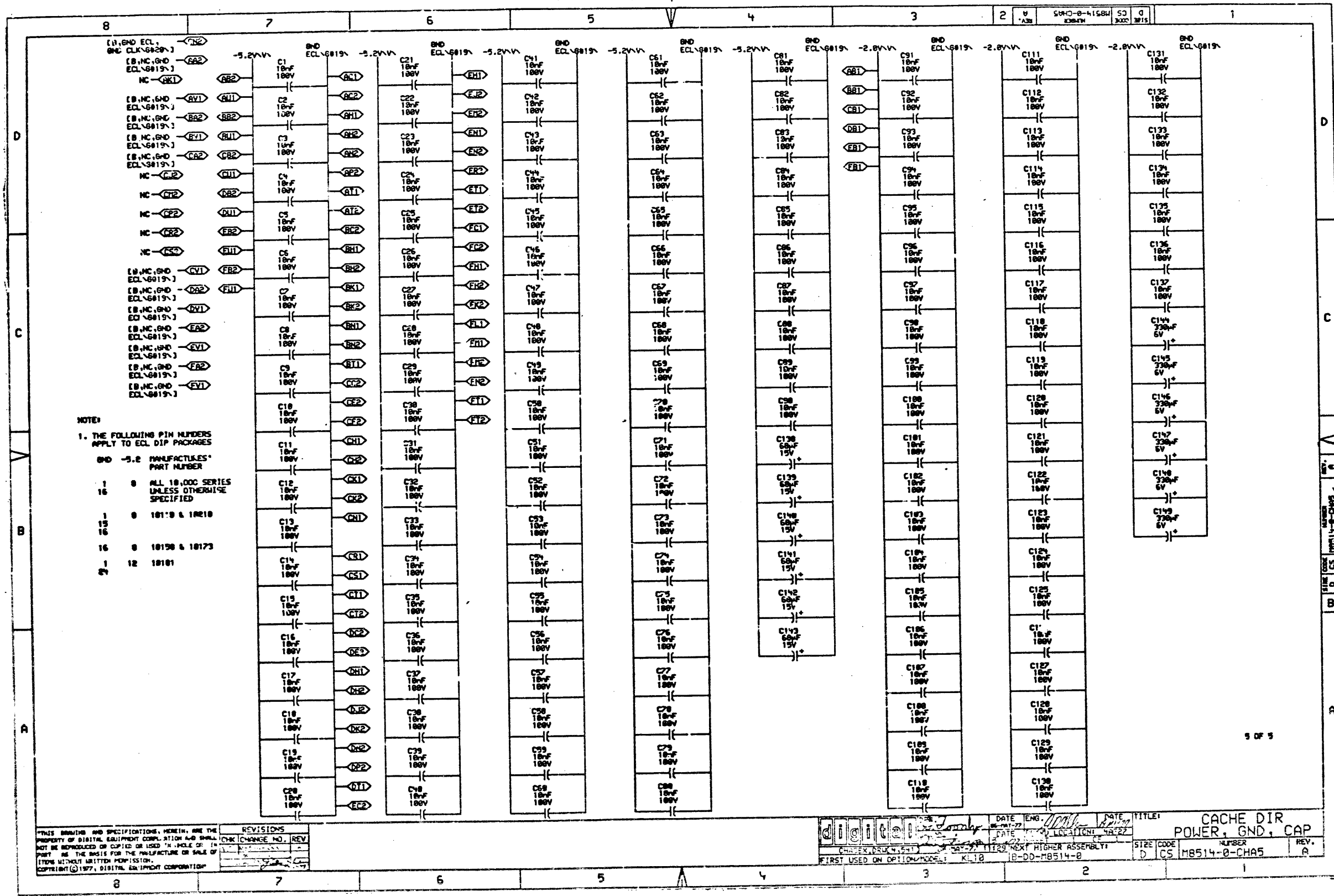
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REVISIONS		
CHK	CHANGE NO.	REV.

digital
DRAWN: [Signature]
DATE: 11-MAY-77
CHK'D: [Signature]
DATE: 11-MAY-77
FIRST USED ON OPTION/MODEL: KL10

ENG. [Signature]
DATE: 11-MAY-77
LOCATION: [Signature]
NEXT HIGHER ASSEMBLY: B-DD-M8514-0

TITLE: CACHE DIR PARITY BITS		SIZE CODE: D CS	NUMBER: M8514-0-CHA4	REV.: A
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- NOTE:
- THE FOLLOWING PIN NUMBERS APPLY TO ECL DIP PACKAGES
- | NO | MANUFACTURER'S PART NUMBER |
|----|--|
| 1 | ALL 10,000 SERIES UNLESS OTHERWISE SPECIFIED |
| 15 | 10170 & 10110 |
| 16 | 10150 & 10173 |
| 21 | 10101 |

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REVISIONS	
CHK	CHANGE NO. REV.

DATE ENG. <i>10/11/77</i>	DATE <i>10/11/77</i>	TITLE
DATE <i>10/11/77</i>	LOCATION <i>4022</i>	CACHE DIR POWER, GND, CAP
SIZE	CODE	NUMBER
D	CS	M8514-0-CHA5
REV.	A	
FIRST USED ON OPTION MODEL: KL10		
NEXT HIGHER ASSEMBLY: 18-DD-M8514-0		

RESISTOR LOC(PIN)	SHOWN DRAW	ON REF	VALUE	TERMINATES SIGNAL
R28K(1)	CH4	C6	50a	XE1(15)
R110K(1)	CH2	B1	50a	XE31(13)
R111K(1)	CH2	B1	50a	XE31(14)
R80K(1)	CH2	D1	50a	XE32(13)
R81K(1)	CH2	D1	50a	XE32(14)
R55K(1)	CH1	B1	50a	XE33(13)
R56K(1)	CH1	B1	50a	XE33(14)
R77K(1)	CH1	D1	50a	XE34(13)
R78K(1)	CH1	C1	50a	XE34(14)
R29K(1)	CH3	C1	50a	-A H
R29K(1)	CH4	C3	50a	-B H
R29K(1)	CH3	D2	50a	-C H
R127K(1)	CH4	C6	50a	CHA TERM 01
R115K(1)	CH4	B6	50a	CHA TERM 03
R105K(1)	CH4	B6	50a	CHA TERM 04
R107K(1)	CH4	B6	50a	CHA TERM 05
R116K(1)	CH4	B6	50a	CHA TERM 06
R113K(1)	CH4	B6	50a	CHA TERM 07
R106K(1)	CH4	B6	50a	CHA TERM 08
R102K(1)	CH4	P5	50a	CHA TERM 09
R103K(1)	CH4	B6	50a	CHA TERM 10
R107K(1)	CH4	B6	50a	CHA TERM 11
R29K(1)	CH1	B7	50a	CH1 ADR 27 0 H
R28K(1)	CH1	B7	50a	CH1 ADR 27 1 H
R67K(1)	CH1	B7	50a	CH1 ADR 27 2 H
R121K(1)	CH1	A7	50a	CH1 ADR 27 3 H
R48K(1)	CH1	A7	50a	CH1 ADR 27 4 H
R38K(1)	CH1	A7	50a	CH1 ADR 27 5 H
R29K(1)	CH1	A7	50a	CH1 ADR 28 0 H
R71K(1)	CH1	A7	50a	CH1 ADR 28 1 H
R85K(1)	CH1	A7	50a	CH1 ADR 28 2 H
R120K(1)	CH1	A7	50a	CH1 ADR 28 3 H
R7K(1)	CH1	A7	50a	CH1 ADR 28 4 H
R3K(1)	CH1	A7	50a	CH1 ADR 28 5 H
R53K(1)	CH1	35	50a	CH1 ADR 29 0 H
R78K(1)	CH1	B4	50a	CH1 ADR 29 1 H
R95K(1)	CH1	B4	50a	CH1 ADR 29 2 H
R119K(1)	CH1	A5	50a	CH1 ADR 29 3 H
R76K(1)	CH1	A4	50a	CH1 ADR 29 4 H
R86K(1)	CH1	A4	50a	CH1 ADR 29 5 H

RESISTOR LOC(PIN)	SHOWN DRAW	ON REF	VALUE	TERMINATES SIGNAL
R55K(1)	CH1	A5	50a	CH1 ADR 30 0 H
R73K(1)	CH1	A4	50a	CH1 ADR 30 1 H
R88K(1)	CH1	A4	50a	CH1 ADR 30 2 H
R122K(1)	CH1	A5	50a	CH1 ADR 30 3 H
R74K(1)	CH1	A4	50a	CH1 ADR 30 4 H
R23K(1)	CH1	A4	50a	CH1 ADR 30 5 H
R55K(1)	CH2	B7	50a	CH2 ADR 31 0 H
R55K(1)	CH2	B7	50a	CH2 ADR 31 1 H
R84K(1)	CH2	B6	50a	CH2 ADR 31 2 H
R110K(1)	CH2	B7	50a	CH2 ADR 31 3 H
R75K(1)	CH2	B7	50a	CH2 ADR 31 4 H
R37K(1)	CH2	B6	50a	CH2 ADR 31 5 H
R51K(1)	CH2	A7	50a	CH2 ADR 32 0 H
R68K(1)	CH2	A7	50a	CH2 ADR 32 1 H
R83K(1)	CH2	A6	50a	CH2 ADR 32 2 H
R117K(1)	CH2	A7	50a	CH2 ADR 32 3 H
R72K(1)	CH2	A7	50a	CH2 ADR 32 4 H
R29K(1)	CH2	A6	50a	CH2 ADR 32 5 H
R58K(1)	CH2	B5	50a	CH2 ADR 33 0 H
R57K(1)	CH2	B4	50a	CH2 ADR 33 1 H
R82K(1)	CH2	B4	50a	CH2 ADR 33 2 H
R112K(1)	CH2	B5	50a	CH2 ADR 33 3 H
R5K(1)	CH2	B4	50a	CH2 ADR 33 4 H
R36K(1)	CH2	B4	50a	CH2 ADR 33 5 H
R46K(1)	CH2	B2	50a	-CH2 WRITE 0 A H
R49K(1)	CH2	B2	50a	-CH2 WRITE 0 B H
R27K(1)	CH2	B2	50a	-CH2 WRITE 0 C H
R53K(1)	CH2	B2	50a	-CH2 WRITE 1 A H
R54K(1)	CH2	B2	50a	-CH2 WRITE 1 B H
R127K(1)	CH2	B2	50a	-CH2 WRITE 1 C H
R70K(1)	CH2	A2	50a	-CH2 WRITE 2 A H
R79K(1)	CH2	A2	50a	-CH2 WRITE 2 B H
R128K(1)	CH2	A2	50a	-CH2 WRITE 2 C H
R108K(1)	CH2	A2	50a	-CH2 WRITE 3 A H
R109K(1)	CH2	A2	50a	-CH2 WRITE 3 B H
R31K(1)	CH2	A2	50a	-CH2 WRITE 3 C H
R3K(1)	CH3	D7	50a	CH3 CSH 0 LD 0 MR H
R4K(1)	CH3	D6	50a	CH3 CSH 0 LD 1 MR H
R13K(1)	CH3	D5	50a	CH3 CSH 0 LD 2 MR H
R15K(1)	CH3	D5	50a	CH3 CSH 0 LD 3 MR H

RESISTOR LOC(PIN)	SHOWN DRAW	ON REF	VALUE	TERMINATES SIGNAL
R90K(1)	CH3	B7	50a	-CH3 CSH 0 MR MR H
R2K(1)	CH3	C7	50a	CH3 CSH 1 LD 0 MR H
R1K(1)	CH3	C6	50a	CH3 CSH 1 LD 1 MR H
R14K(1)	CH3	C5	50a	CH3 CSH 1 LD 2 MR H
R18K(1)	CH3	C5	50a	CH3 CSH 1 LD 3 MR H
R5K(1)	CH3	A7	50a	-CH3 CSH 1 MR MR H
R16K(1)	CH3	D4	50a	CH3 CSH 2 LD 0 MR H
R17K(1)	CH3	D3	50a	CH3 CSH 2 LD 1 MR H
R19K(1)	CH3	D2	50a	CH3 CSH 2 LD 2 MR H
R10K(1)	CH3	D2	50a	CH3 CSH 2 LD 3 MR H
R57K(1)	CH3	A7	50a	-CH3 CSH 2 MR MR H
R8K(1)	CH3	C4	50a	CH3 CSH 3 LD 0 MR H
R3K(1)	CH3	C3	50a	CH3 CSH 3 LD 1 MR H
R42K(1)	CH3	C2	50a	CH3 CSH 3 LD 2 MR H
R11K(1)	CH3	C2	50a	CH3 CSH 3 LD 3 MR H
R26K(1)	CH3	A7	50a	-CH3 CSH 3 MR MR H
R20K(1)	CH3	B6	50a	-CH3 CSH MR LD 0 SEL H
R22K(1)	CH3	B6	50a	-CH3 CSH MR LD 1 SEL H
R23K(1)	CH3	A6	50a	-CH3 CSH MR LD 2 SEL H
R44K(1)	CH3	A6	50a	-CH3 CSH MR LD 3 SEL H
R56K(1)	CH3	A4	50a	CH3 CSH MR MR DATA A H
R25K(1)	CH2	A4	50a	CH3 CSH MR MR DATA B H
R91K(1)	CH4	C7	50a	-CON MR EVEN PAR DIR H
R45K(1)	CH3	B8	50a	-CSH 0 MR EN H
R41K(1)	CH3	B8	50a	-CSH 1 MR EN H
R50K(1)	CH3	A8	50a	-CSH 2 MR EN H
R61K(1)	CH3	A8	50a	-CSH 3 MR EN H
R43K(1)	CH2	B2	50a	-CSH ADR MR PULSE H
R12K(1)	CH3	A1	50a	-CSH MR OUT EN H
R30K(1)	CH3	B6	50a	CSH MR SEL ALL H
R52K(1)	CH3	B6	50a	CSH MR LD 0 EN H
R57K(1)	CH3	B6	50a	CSH MR LD 1 EN H
R59K(1)	CH3	A6	50a	CSH MR LD 2 EN H
R94K(1)	CH3	A6	50a	CSH MR LD 3 EN H
R93K(1)	CH3	A5	50a	CSH MR MR DATA H
R92K(1)	CH3	B8	50a	-CSH MR MR PULSE H
R99K(1)	CH1	E7	50a	MRX CSH ADR 27 H
R100K(1)	CH1	A7	50a	MRX CSH ADR 28 H
R52K(1)	CH1	B5	50a	MRX CSH ADR 29 H
R45K(1)	CH1	A5	50a	MRX CSH ADR 30 H

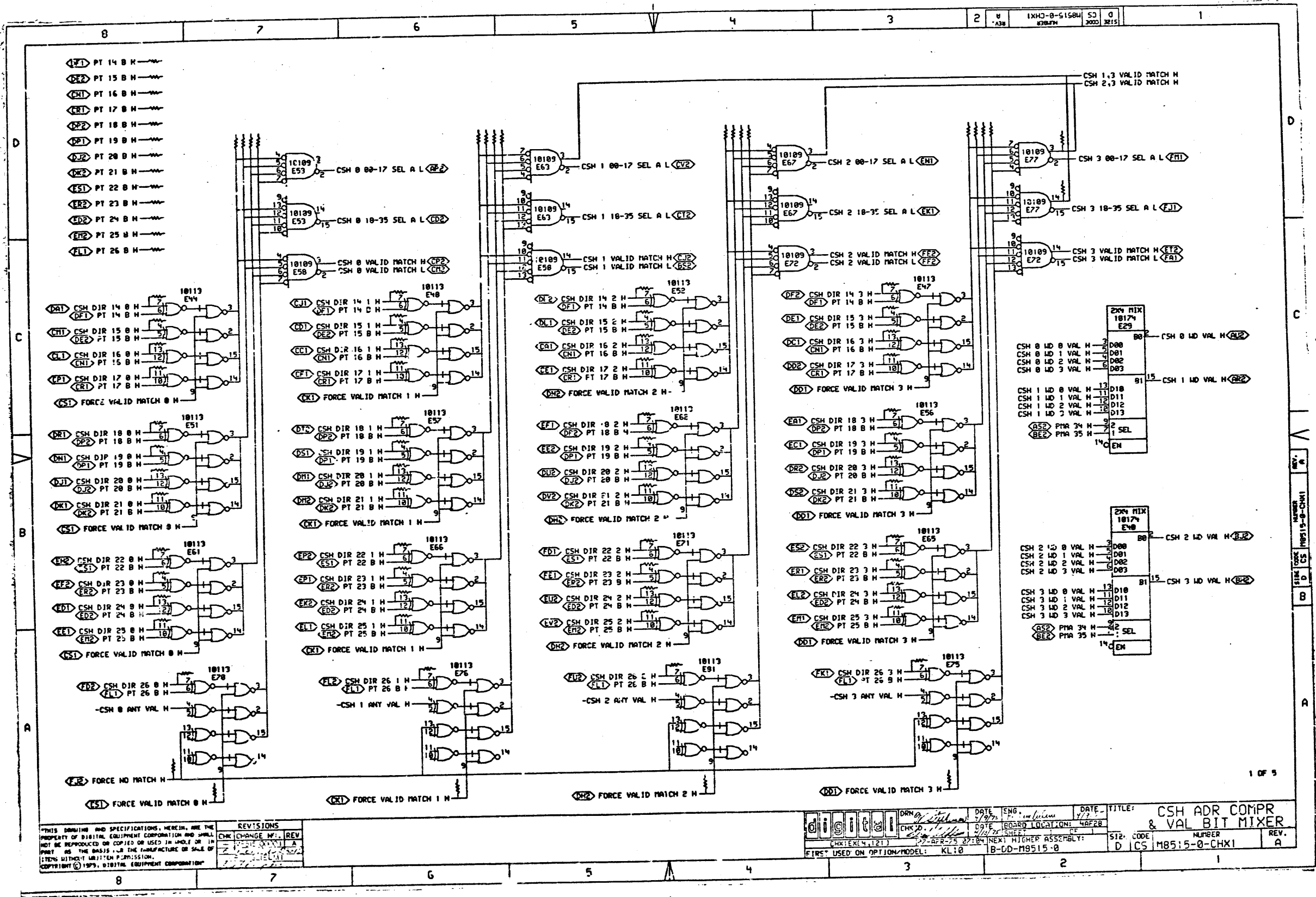
RESISTOR LOC(PIN)	SHOWN DRAW	ON REF	VALUE	TERMINATES SIGNAL
R21K(1)	CH2	B7	50a	MRX CSH ADR 31 H
R101K(1)	CH2	A7	50a	MRX CSH ADR 32 H
R77K(1)	CH2	B5	50a	MRX CSH ADR 33 H
R92K(1)	CH4	C7	50a	PTA 14-25 PAR H
R114K(1)	CH4	B6	50a	PT ACCESS H
R124K(1)	CH4	C6	50a	-PT MATCH H
R126K(1)	CH4	B6	50a	PT SOFTWARE H
R125K(1)	CH4	C6	50a	PT WRITABLE H

NOTES:
 1. ALL TERMINATORS HAVE PIN TWO CONNECTED TO -2.0V AND ARE 5% TOLERANCE UNLESS OTHERWISE SPECIFIED
 2. ENTRIES ARE SORTED BY SIGNAL NAME
 3. % INDICATES OUTPUT OF DIP LOC AND
 () INDICATES PIN NUMBER

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REVISIONS
CHK CHANGE NO. REV

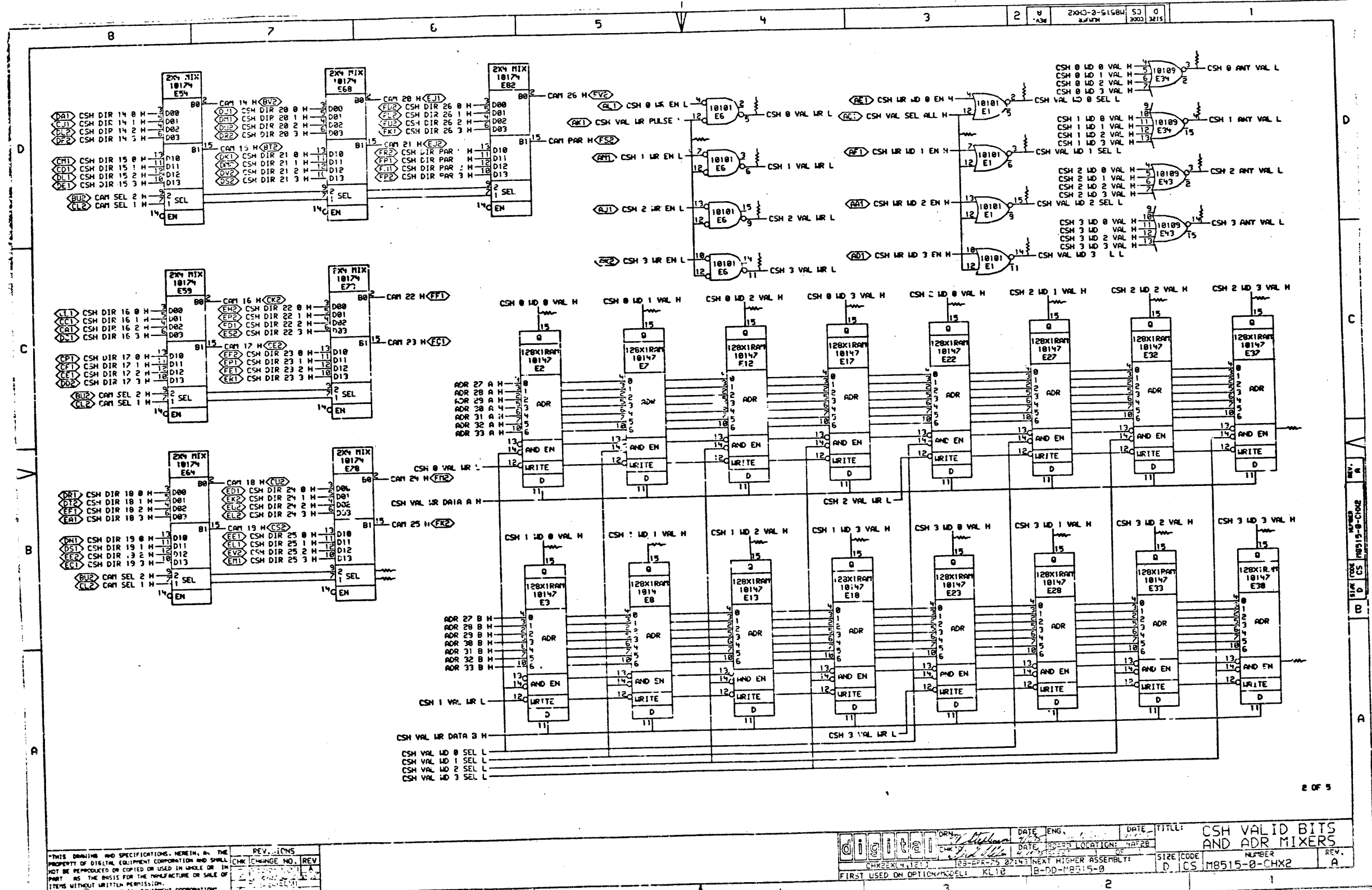
DATE ENG *Smith* DATE *10/11/77* TITLE **CACHE DIR TERMINATORS**
 DATE *10/11/77* DATE *10/11/77* DATE *10/11/77*
 FIRST USED ON OPTION MODEL KL10 B-DD-M8514-2
 SIZE CODE NUMBER REV.
 D CS M8514-2-RES A



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REV	CHANGE	DATE
1	INITIAL	10/1/75
2	REVISED	10/1/75

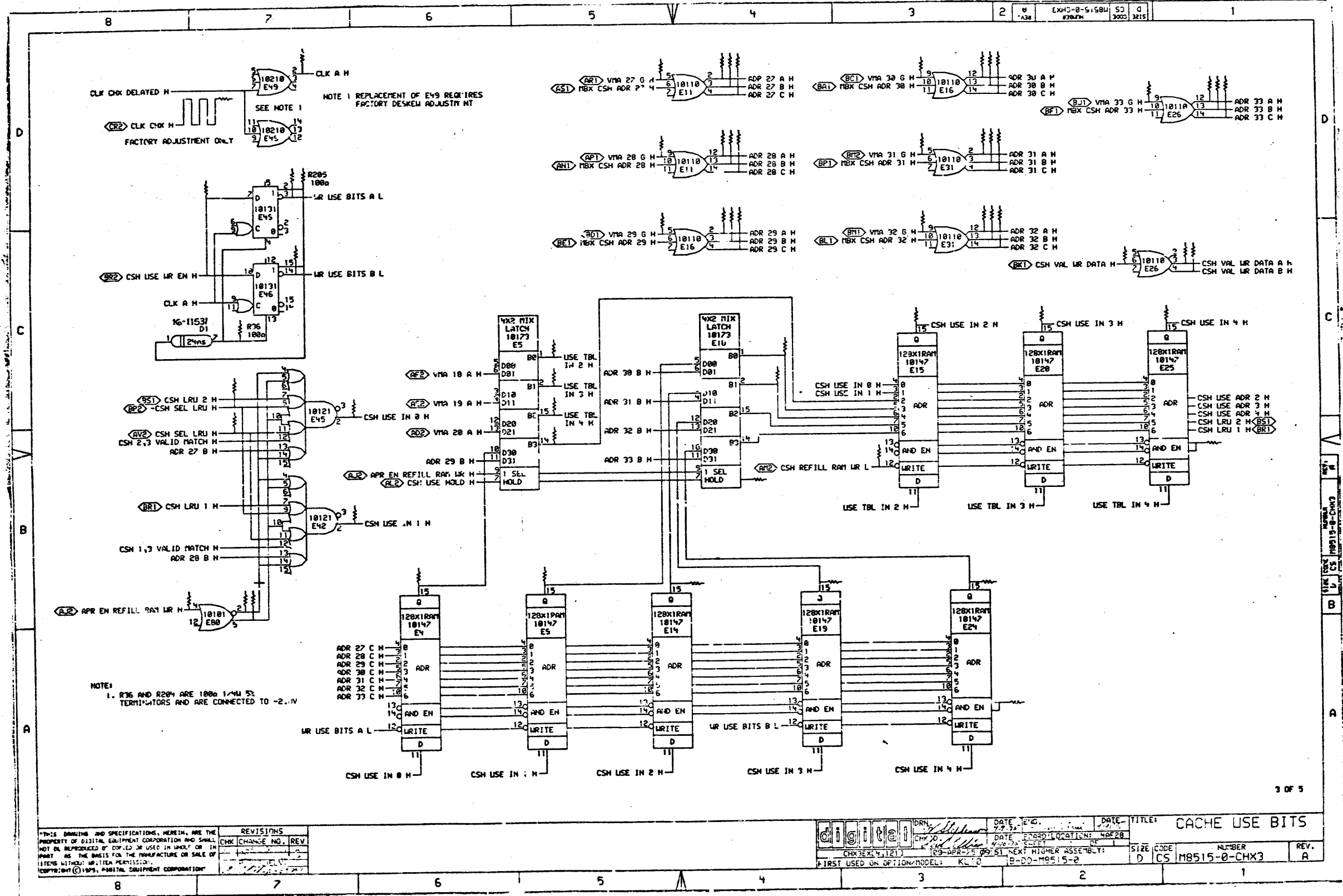
DATE: 10/1/75	DATE: 10/1/75	TITLE: CSH ADR COMP & VAL BIT MIXER
CHK'D: [Signature]	DATE: 10/1/75	BOARD LOCATION: 4AF28
DRN: [Signature]	DATE: 10/1/75	REV: A
DATE: 10/1/75	DATE: 10/1/75	NUMBER: M8515-0-CHK1
DATE: 10/1/75	DATE: 10/1/75	REV: A

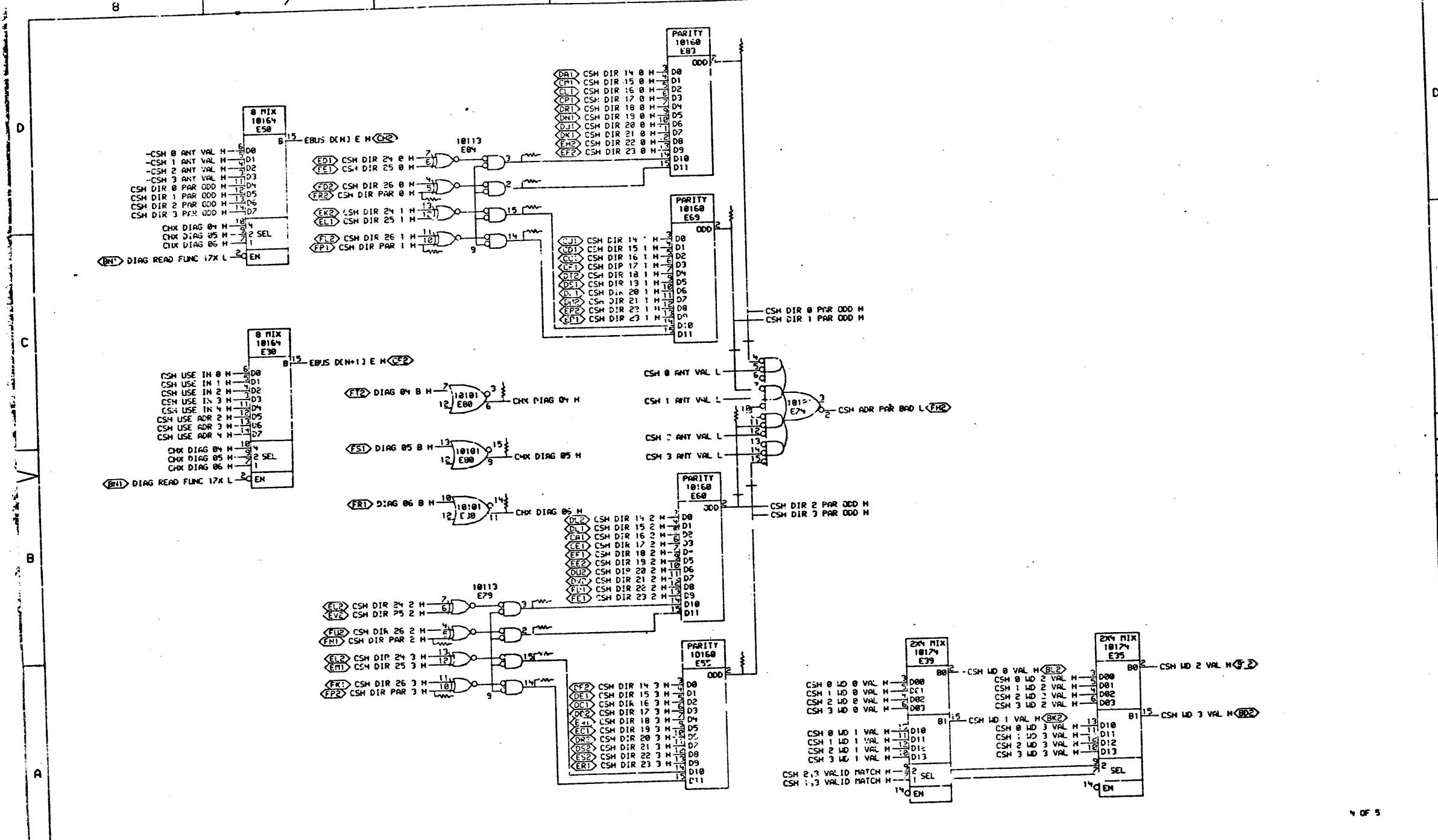


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REV.	CHG.	DESCRIPTION
A		

	DATE: 11/15/75	ENG: [Signature]	DATE: 11/15/75	TITLE: CSH VALID BITS AND ADDR MIXERS
	DATE: 11/15/75	DATE: 11/15/75	DATE: 11/15/75	DATE: 11/15/75
CHX2K4.1217	18-24K-75 02:43	NEXT HIGHER ASSEMBLY: B-DD-M8515-0	SIZE: CODE D	NUMBER: M8515-0-CHX2
FIRST USED ON OPTION MODEL: KL10				REV: A

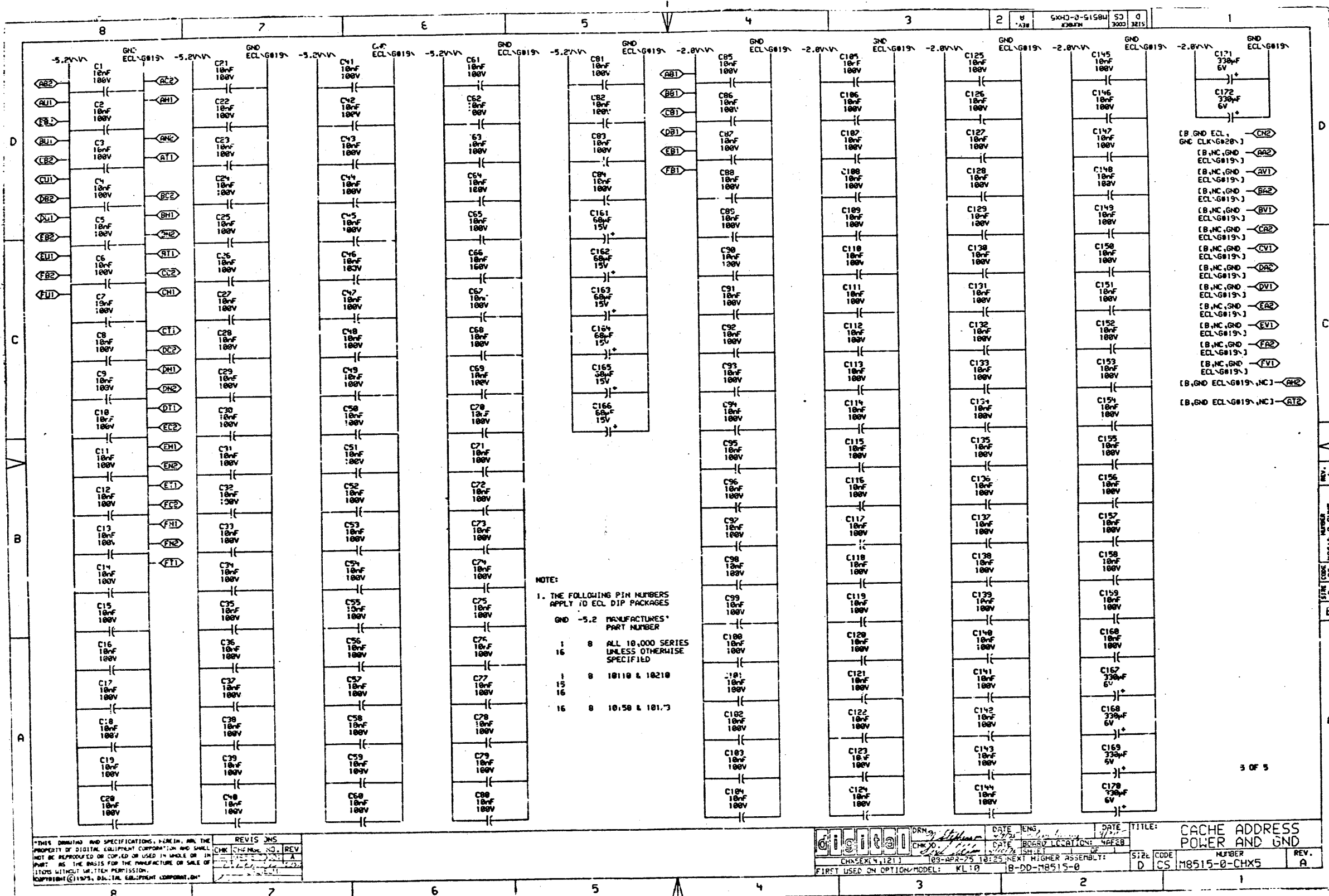




4 OF 5

REV.	CHG.	REASON
1		
2		
3		
4		
5		
6		
7		
8		

DATE ENG: 11/27/71
 DATE DES: 11/27/71
 DATE TEST: 11/27/71
 DATE ASSEMBLY: 11/27/71
 TITLE: CSH DIR PAR NET AND DIAG MIXERS
 SIZE CODE: D CS
 NUMBER: M8515-0-CHX4
 REV. A
 FIRST USED ON OPTION/MODEL: KL18 B-CU-M8515-0



NOTE:
 1. THE FOLLOWING PIN NUMBERS APPLY TO ECL DIP PACKAGES

1	8	MANUFACTURER'S PART NUMBER
1	16	ALL 10,000 SERIES UNLESS OTHERWISE SPECIFIED
1	15	10110 & 10210
16	16	10150 & 10173

REV	DATE	BY	CHK	APP
1				

DRN: <i>103-APR-75</i>	DATE: <i>4/27/75</i>	ENG: <i>W. J. ...</i>	DATE: <i>4/27/75</i>	TITLE: CACHE ADDRESS POWER AND GND
CHK'D: <i>W. J. ...</i>	DATE: <i>4/27/75</i>	BOARD LOCATION: <i>4F2B</i>	DATE: <i>4/27/75</i>	NUMBER: <i>1</i>
CHK'ER: <i>W. J. ...</i>	103-APR-75 10:25	NEXT HIGHER ASSEMBLY:	SIZE: <i>D</i>	CODE: <i>CS</i>
FIRST USED ON OPTION/MODEL: <i>KL10</i>	<i>18-DD-M8515-0</i>		NUMBER: <i>M8515-0-CHX5</i>	REV: <i>A</i>

RESISTOR LOC(PIN)	SHOWN ON DATA REF	VALUE	TERMINATES SIGNAL
R9K(1)	CHKEX B4	68a	XE1K(15)
R3K(1)	CHKEX B4	68a	XE1K(15)
R166(1)	CHKEX B1	68a	XE2K(12)
R57(1)	CHKEX A2	68a	XE2K(13)
R8K(1)	CHKEX B3	68a	XE2K(15)
R14(1)	CHKEX B1	68a	XE25K(13)
R133(1)	CHKEX A1	68a	XE30K(13)
R2(1)	CHKEX B6	68a	XE4K(15)
R141(1)	CHKEX D7	68a	XE4K(14)
R36(1)	CHKEX C7	100a	XE4K(13)
R285(1)	CHKEX D7	100a	XE4K(15)
R153(1)	CHKEX D2	68a	XE47K(14)
R145(1)	CHKEX D6	68a	XE4K(14)
R140(1)	CHKEX D7	68a	XE51(13)
R148(1)	CHKEX D4	68a	XE52K(14)
R154(1)	CHKEX D2	68a	XE56K(14)
R144(1)	CHKEX D6	68a	XE57K(3)
R130(1)	CHKEX D7	68a	XE51(13)
R146(1)	CHKEX D4	68a	XE62K(14)
R152(1)	CHKEX D2	68a	XE65K(14)
R143(1)	CHKEX D5	68a	XE66K(3)
R139(1)	CHKEX D7	68a	XE7K(15)
R150(1)	CHKEX D4	68a	XE71(14)
R147(1)	CHKEX D2	68a	XE73K(15)
R142(1)	CHKEX D5	68a	XE7K(15)
R42(1)	CHKEX A6	68a	XE7K(14)
R43(1)	CHKEX A6	68a	XE7K(15)
R51(1)	CHKEX B6	68a	XE7K(2)
R53(1)	CHKEX B6	68a	XE7K(3)
R189(1)	CHKEX B7	68a	XE8K(2)
R112(1)	CHKEX B7	68a	XE8K(5)
R149(1)	CHKEX D4	68a	XE81(15)
R62(1)	CHKEX C6	68a	XE4K(14)
R51(1)	CHKEX D6	68a	XE8K(15)
R123(1)	CHKEX D6	68a	XE8K(2)
R127(1)	CHKEX D6	68a	XE8K(3)
R18K(1)	CHKEX B5	68a	XE9K(15)
R163(1)	CHKEX D4	68a	ADR 27 A H
R113(1)	CHKEX D4	68a	ADR 27 B H
R181(1)	CHKEX D4	68a	ADR 27 C H

RESISTOR LOC(PIN)	SHOWN ON DATA REF	VALUE	TERMINATES SIGNAL
R160(1)	CHKEX D4	68a	ADR 28 A H
R111(1)	CHKEX D4	68a	ADR 28 B H
R140(1)	CHKEX D4	68a	ADR 28 C H
R167(1)	CHKEX C4	68a	ADR 29 A H
R1C(1)	CHKEX C4	68a	ADR 29 B H
R182(1)	CHKEX C4	68a	ADR 29 C H
R170(1)	CHKEX D3	68a	ADR 30 A H
R11(1)	CHKEX D2	68a	ADR 30 B H
R95(1)	CHKEX D2	68a	ADR 30 C H
R158(1)	CHKEX D3	68a	ADR 31 A H
R5(1)	CHKEX D2	68a	ADR 31 B H
R91(1)	CHKEX D2	68a	ADR 31 C H
R159(1)	CHKEX C3	68a	ADR 32 A H
R6(1)	CHKEX C2	68a	ADR 32 B H
R93(1)	CHKEX C2	68a	ADR 32 C H
R161(1)	CHKEX D1	68a	ADR 33 A H
R4(1)	CHKEX D1	68a	ADR 33 B H
R94(1)	CHKEX D1	68a	ADR 33 C H
R22(1)	CHKEX B7	68a	ADR EN REFILL RAY LR H
R157(1)	CHKEX B6	68a	CAN SEL 1 H
R155(1)	CHKEX B6	68a	CAN SEL 2 H
R20(1)	CHKEX C6	68a	CHK DIAG 04 H
R92(1)	CHKEX B6	68a	CHK DIAG 05 H
R23(1)	CHKEX B5	68a	CHK DIAG 06 H
R35(1)	CHKEX D7	68a	CLK A H
R137(1)	CHKEX D7	68a	CLK CLK H
R202(1)	CHKEX D1	68a	-CSH 0 ANY VAL H
R162(1)	CHKEX D4	68a	-CSH 0 VAL LR H
R110(1)	CHKEX C5	68a	CSH 0 LD 0 VAL H
R185(1)	CHKEX C5	68a	CSH 0 LD 1 VAL H
R24(1)	CHKEX C4	68a	CSH 0 LD 2 VAL H
R186(1)	CHKEX C4	68a	CSH 0 LD 3 VAL H
R183(1)	CHKEX D1	68a	-CSH 1 ANY VAL H
R132(1)	CHKEX D4	68a	-CSH 1 VAL LR H
R180(1)	CHKEX B5	68a	CSH 1 LD 0 VAL H
R187(1)	CHKEX B5	68a	CSH 1 LD 1 VAL H
R22(1)	CHKEX B4	68a	CSH 1 LD 2 VAL H
R184(1)	CHKEX B4	68a	CSH 1 LD 3 VAL H
R27(1)	CHKEX D2	68a	CSH 1,3 VALID RPTCH H
R188(1)	CHKEX D1	68a	-CSH 2 ANY VAL H

RESISTOR LOC(PIN)	SHOWN ON DATA REF	VALUE	TERMINATES SIGNAL
R165(1)	CHKEX D4	68a	-CSH 2 VAL LR H
R33(1)	CHKEX C3	68a	CSH 2 LD 0 VAL H
R74(1)	CHKEX C2	68a	CSH 2 LD 1 VAL H
R31(1)	CHKEX C2	68a	CSH 2 LD 2 VAL H
R21(1)	CHKEX C1	68a	CSH 2 LD 3 VAL H
R20(1)	CHKEX D2	68a	CSH 2,3 VALID MATCH H
R203(1)	CHKEX C1	68a	-CSH 3 ANY VAL H
R135(1)	CHKEX C4	68a	-CSH 3 VAL LR H
R25(1)	CHKEX B3	68a	CSH 3 LD 0 VAL H
R32(1)	CHKEX B2	68a	CSH 3 LD 1 VAL H
R29(1)	CHKEX B2	68a	CSH 3 LD 2 VAL H
R30(1)	CHKEX B1	68a	CSH 3 LD 3 VAL H
R40(1)	CHKEX D4	68a	CSH DIR 0 PAR ODD H
R37(1)	CHKEX C4	68a	CSH DIR 1 PAR ODD H
R122(1)	CHKEX C8	68a	CSH DIR 14 0 H
R67(1)	CHKEX C6	68a	CSH DIR 14 1 H
R52(1)	CHKEX C5	68a	CSH DIR 14 2 H
R49(1)	CHKEX C3	68a	CSH DIR 14 3 H
R130(1)	CHKEX C8	68a	CSH DIR 15 0 H
R68(1)	CHKEX C6	68a	CSH DIR 15 1 H
R53(1)	CHKEX C5	68a	CSH DIR 15 2 H
R46(1)	CHKEX C3	68a	CSH DIR 15 3 H
R120(1)	CHKEX C9	68a	CSH DIR 16 0 H
R69(1)	CHKEX C6	68a	CSH DIR 16 1 H
R54(1)	CHKEX C5	68a	CSH DIR 16 2 H
R47(1)	CHKEX C3	68a	CSH DIR 16 3 H
R156(1)	CHKEX C8	68a	CSH DIR 17 0 H
R71(1)	CHKEX C6	68a	CSH DIR 17 1 H
R56(1)	CHKEX C5	68a	CSH DIR 17 2 H
R50(1)	CHKEX C3	68a	CSH DIR 17 3 H
R129(1)	CHKEX C8	68a	CSH DIR 18 0 H
R70(1)	CHKEX C6	68a	CSH DIR 18 1 H
R55(1)	CHKEX C5	68a	CSH DIR 18 2 H
R48(1)	CHKEX C3	68a	CSH DIR 18 3 H
R151(1)	CHKEX B8	68a	CSH DIR 19 0 H
R55(1)	CHKEX B6	68a	CSH DIR 19 1 H
R58(1)	CHKEX B5	68a	CSH DIR 19 2 H
R116(1)	CHKEX B3	68a	CSH DIR 19 3 H
R30(1)	CHKEX C4	68a	CSH DIR 2 PAR ODD H
R126(1)	CHKEX B8	68a	CSH DIR 20 0 H

RESISTOR LOC(PIN)	SHOWN ON DATA REF	VALUE	TERMINATES SIGNAL
R66(1)	CHKEX B6	68a	CSH DIR 20 1 H
R110(1)	CHKEX B5	68a	CSH DIR 20 2 H
R119(1)	CHKEX B3	68a	CSH DIR 20 3 H
R125(1)	CHKEX B8	68a	CSH DIR 21 0 H
R64(1)	CHKEX B6	68a	CSH DIR 21 1 H
R57(1)	CHKEX B5	68a	CSH DIR 21 2 H
R120(1)	CHKEX B3	68a	CSH DIR 21 3 H
R124(1)	CHKEX B8	68a	CSH DIR 22 0 H
R59(1)	CHKEX B6	68a	CSH DIR 22 1 H
R45(1)	CHKEX B5	68a	CSH DIR 22 2 H
R41(1)	CHKEX B3	68a	CSH DIR 22 3 H
R121(1)	CHKEX B8	68a	CSH DIR 23 0 H
R60(1)	CHKEX B6	68a	CSH DIR 23 1 H
R117(1)	CHKEX B5	68a	CSH DIR 23 2 H
R44(1)	CHKEX B3	68a	CSH DIR 23 3 H
R67(1)	CHKEX B8	68a	CSH DIR 24 0 H
R81(1)	CHKEX B6	68a	CSH DIR 24 1 H
R82(1)	CHKEX B5	68a	CSH DIR 24 2 H
R74(1)	CHKEX B3	68a	CSH DIR 24 3 H
R80(1)	CHKEX B8	68a	CSH DIR 25 0 H
R79(1)	CHKEX B6	68a	CSH DIR 25 1 H
R78(1)	CHKEX B5	68a	CSH DIR 25 2 H
R73(1)	CHKEX B3	68a	CSH DIR 25 3 H
R85(1)	CHKEX A8	68a	CSH DIR 26 0 H
R83(1)	CHKEX A6	68a	CSH DIR 26 1 H
R75(1)	CHKEX A4	68a	CSH DIR 26 2 H
R76(1)	CHKEX A3	68a	CSH DIR 26 3 H
R72(1)	CHKEX A4	68a	CSH DIR 3 PAR ODD H
R86(1)	CHKEX D6	68a	CSH DIR PAR 0 H
R84(1)	CHKEX C6	68a	CSH DIR PAR 1 H
R80(1)	CHKEX B6	68a	CSH DIR PAR 2 H
R70(1)	CHKEX A6	68a	CSH DIR PAR 3 H
R15(1)	CHKEX B3	68a	-CSH REFILL RAY LR H
R114(1)	CHKEX B7	68a	CSH SEL LRU H
R115(1)	CHKEX C7	68a	-CSH SEL LRU H
R17(1)	CHKEX B5	68a	CSH USE ADR 2 H
R10(1)	CHKEX C4	68a	CSH USE ADR 3 H
R19(1)	CHKEX C4	68a	CSH USE ADR 4 H
R7(1)	CHKEX B4	68a	CSH USE HOLD H
R92(1)	CHKEX C6	68a	CSH USE IN 0 H

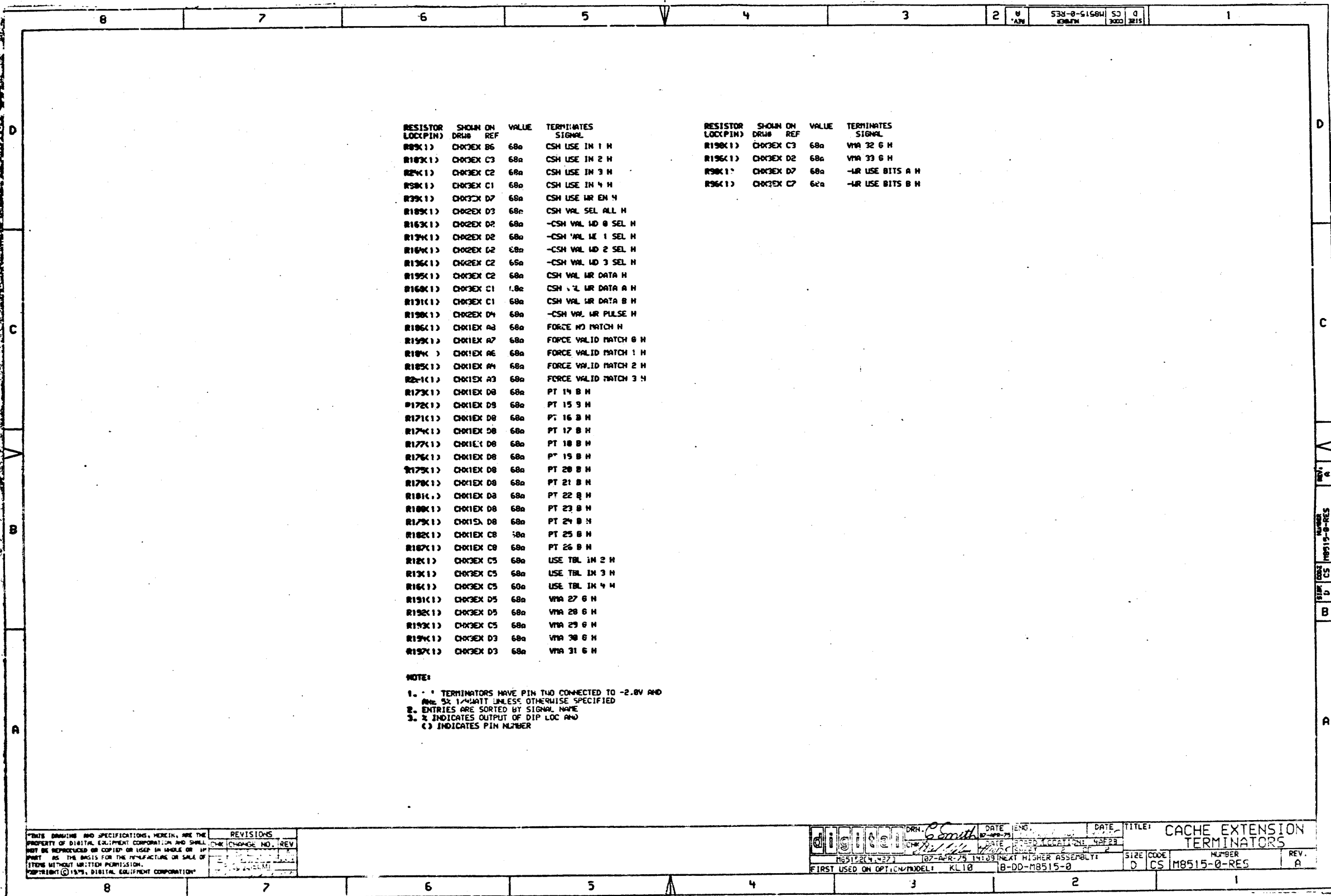
NOTE:
1. ALL TERMINATORS HAVE PIN TWO CONNECTED TO -2.0V AND ARE 5% TOLERANCE UNLESS OTHERWISE SPECIFIED
2. ENTRIES ARE SORTED BY SIGNAL NAME
3. X INDICATES OUTPUT OF DIP LOC AND () INDICATES PIN NUMBER

REVISIONS	
CHG	CHANGE NO. REV
1	1

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	DATE: 11/28/75	ENG: Smith	DATE: 11/28/75	TITLE: CACHE EXTENSION TERMINATORS
18515(4,427)	CHK'D: [Signature]	DATE: 12/1/75	LOCATION: 4428	REV. A
FIRST USED ON OPTION/MODEL: KL10	DATE: 10/27/75	INSTRUMENT: NEXT HIGHER ASSEMBLY	SIZE CODE: D CS	NUMBER: M8515-0-RES
				REV. A

D
C
A
B
18515-0-RES



RESISTOR LOC(PIN)	SHOWN ON DRW#	REF	VALUE	TERMINATES SIGNAL
R09K(1)	CHK3EX	B6	68Ω	CSH USE IN 1 H
R10K(1)	CHK3EX	C3	68Ω	CSH USE IN 2 H
R24K(1)	CHK3EX	C2	68Ω	CSH USE IN 3 H
R58K(1)	CHK3EX	C1	68Ω	CSH USE IN 4 H
R39K(1)	CHK3EX	D7	68Ω	CSH USE MR EN 4
R10K(1)	CHK2EX	D3	68Ω	CSH VAL SEL ALL H
R16K(1)	CHK2EX	D2	68Ω	-CSH VAL LD 0 SEL H
R17K(1)	CHK2EX	D2	68Ω	-CSH VAL LE 1 SEL H
R16K(1)	CHK2EX	D2	68Ω	-CSH VAL LD 2 SEL H
R13K(1)	CHK2EX	C2	68Ω	-CSH VAL LD 3 SEL H
R19K(1)	CHK3EX	C2	68Ω	CSH VAL MR DATA H
R16K(1)	CHK3EX	C1	1.0Ω	CSH VAL MR DATA A H
R13K(1)	CHK3EX	C1	68Ω	CSH VAL MR DATA B H
R19K(1)	CHK2EX	D4	68Ω	-CSH VAL MR PULSE H
R10K(1)	CHK1EX	A3	68Ω	FORCE NO MATCH H
R19K(1)	CHK1EX	A7	68Ω	FORCE VALID MATCH 0 H
R10K(1)	CHK1EX	A6	68Ω	FORCE VALID MATCH 1 H
R10K(1)	CHK1EX	A4	68Ω	FORCE VALID MATCH 2 H
R24K(1)	CHK1EX	A3	68Ω	FORCE VALID MATCH 3 H
R17K(1)	CHK1EX	D8	68Ω	PT 14 B H
R17K(1)	CHK1EX	D8	68Ω	PT 15 B H
R17K(1)	CHK1EX	D8	68Ω	PT 16 B H
R17K(1)	CHK1EX	D8	68Ω	PT 17 B H
R17K(1)	CHK1EX	D8	68Ω	PT 18 B H
R17K(1)	CHK1EX	D8	68Ω	PT 19 B H
R17K(1)	CHK1EX	D8	68Ω	PT 20 B H
R17K(1)	CHK1EX	D8	68Ω	PT 21 B H
R18K(1)	CHK1EX	D8	68Ω	PT 22 B H
R18K(1)	CHK1EX	D8	68Ω	PT 23 B H
R17K(1)	CHK1EX	D8	68Ω	PT 24 B H
R18K(1)	CHK1EX	C8	68Ω	PT 25 B H
R18K(1)	CHK1EX	C9	68Ω	PT 26 B H
R18K(1)	CHK3EX	C5	68Ω	USE TBL IN 2 H
R13K(1)	CHK3EX	C5	68Ω	USE TBL IN 3 H
R16K(1)	CHK3EX	C5	68Ω	USE TBL IN 4 H
R19K(1)	CHK3EX	D5	68Ω	VIA 27 G H
R19K(1)	CHK3EX	D5	68Ω	VIA 28 G H
R19K(1)	CHK3EX	C5	68Ω	VIA 29 G H
R19K(1)	CHK3EX	D3	68Ω	VIA 30 G H
R19K(1)	CHK3EX	D3	68Ω	VIA 31 G H

NOTE:
 1. * TERMINATORS HAVE PIN TWO CONNECTED TO -2.0V AND ARE 5% 1/4WATT UNLESS OTHERWISE SPECIFIED
 2. ENTRIES ARE SORTED BY SIGNAL NAME
 3. * INDICATES OUTPUT OF DIP LOC AND () INDICATES PIN NUMBER

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REVISIONS	
CHK	CHANGE NO. REV

DIGITAL	DRW. <i>C. Smith</i>	DATE <i>10-APR-75</i>	ENG. <i> </i>	DATE <i> </i>	TITLE: CACHE EXTENSION TERMINATORS
	CHK. <i> </i>	DATE <i> </i>	DATE <i> </i>	DATE <i> </i>	
M8515-0-RES			187-APR-75	14109	NEAT HIGHER ASSEMBLY
FIRST USED ON OPTIC/PRODEL			KL10	18-DD-M8515-0	
SIZE	CODE	NUMBER	REV.		
D	CS	M8515-0-RES	A		