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BOOTSTRAP ROMS

BM873YH

First Used On - DECsystem-10XX console front end.

Current Usability - DECsystem-10XX console front end,  
DECSYSTEM-20XX console front end.

Summary of Features

- 1 Switch register
- 2 RP04/05/06 disk bootstrap
- 3 RX11 floppy disk bootstrap
- 4 TC11 DECTape bootstrap
- 5 Error retry
- 6 Bootstrap parameters
- 7 Parameter entry

Button Addresses

- 1 773000 Switch register
- 2 773030 Disk
- 3 773020 Floppy/DECTape
- 4 773554 DTE20

Other Entry Locations

773300 TC11 DECTape bootstrap. Used if DECTape bootstrap (unit  
0) desired and RX11 floppy exists in configuration.

BM873YJ

First Used On - DECSYSTEM-20XX communications front end.

Current Usability - DECsystem-10XX console front end,  
DECSYSTEM-20XX console front end, DECsystem-10XX communications  
front end, DECSYSTEM-20XX communications front end.

Summary of Features

- 1 Switch register
- 2 RP04/05/06 disk bootstrap
- 3 RX11 floppy disk bootstrap
- 4 TC11 DECTape bootstrap
- 5 DTE20 bootstrap and dump
- 6 DL11 asynchronous line bootstrap
- 7 Error retry
- 8 Bootstrap parameters
- 9 Parameter entry
- 10 PDP11/34 support

Button Addresses

- 1 773220 Switch register (halts)
- 1 773000 Switch register (does not halt)
- 2 773030 Disk
- 3 773020 Floppy/DECTape/DL11
- 4 773230 DTE20

Other Entry Locations

773214 TC11 DECTape bootstrap. Used if DECTape bootstrap (unit  
0) desired and RX11 floppy disk exists in configuration.

773530 DL11 asynchronous line bootstrap. Used if DL11 bootstrap  
desired and either RX11 floppy disk on TC11 DECTape exists in  
configuration.

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VECTOR AND ADDRESS ASSIGNMENTS FOR FRONT END OPTIONS

Unit No.	DN11	DQ11	DM11BB	DR11	DTE20	LP20	CD20	CTY DL11-C	KLINIK DL11-E
01	775200 660	760230 520	770500 320	760020 330	774400 774	775400 754	777160 230	777560 60	775610 300
02	775210 664	760240 530	770510 340	760040 350	774440 770	775420 750			
03	775220 670	760250 540	770520 360	760060 370	774500 764				
04	775230 674	760260 550	770530 400	760100 410	774540 760				
05	775240 700	760270 560	770540 420	760120 430					
06	775250 704	760300 570	770550 440	760140 450					
07	775260 710	760310 600	770560 460	760160 470					
08	775270 714	760320 610	770570 500	760200 510					
09	775300 720	760330 620							
10	775310 724	760340 630							
11	775320 730	760350 640							
12	775330 734	760360 650							
13	775340 740								
14	775350 744								
15	775360 750								
16	775370 754								

UNIBUS PIN ASSIGNMENTS (BY PIN NUMBERS)		UNIBUS PIN ASSIGNMENTS (BY SIGNAL NAME)	
AA1	INIT L	AO0 L	BH2
AA2	POWER (+5 V)	AO1 L	BH1
AB1	INTR L	AO2 L	BJ2
AB2	GROUND	AO3 L	BJ1
AC1	DOO L	AO4 L	BK2
AC2	GROUND	AO5 L	BK1
AD1	DO2 L	AO6 L	BL2
AD2	DO1 L	AO7 L	BL1
AE1	DO4 L	AO8 L	BM2
AE2	DO3 L	AO9 L	BM1
AF1	DO6 L	A10 L	BN2
AF2	DO5 L	A11 L	BN1
AH1	DO8 L	A12 L	BP2
AH2	DO7 L	A13 L	BP1
AJ1	D10 L	A14 L	BR2
AJ2	DO9 L	A15 L	BR1
AK1	D12 L	A16 L	BS2
AK2	D11 L	A17 L	BS1
AL1	D14 L	ACLO L	BF1
AL2	D13 L	BBSY L	AP2
AM1	PA L (D16 L)	BG4 H	BE2
AM2	D15 L	BG5 H	BB1
AN1	GROUND	BG6 H	BA1
AN2	PB L (D17 L)	BG7 H	AV1
AP1	GROUND	BR4 L	BD2
AP2	BBSY L	BR5 L	BC1
AR1	GROUND	BR6 L	AU2
AR2	SACK L	BR7 L	AT2
AS1	GROUND	CO L	BU2
AS2	NPR L	C1 L	BT2
AT1	GROUND	DOO L	AC1
AT2	BR 7 L	DO1 L	AD2
AU1	NPG H	DO2 L	AD1
AU2	BR 6 L	DO3 L	AE2
AV1	BG 7 H	DO4 L	AE1
AV2	GROUND	DO5 L	AF2
BA1	BG6 H	DO6 L	AF1
BA2	POWER (+5 V)	DO7 L	AH2
BB1	BG 5 H	DO8 L	AH1
BB2	GROUND	DO9 L	AJ2
BC1	BR 5 L	D10 L	AJ1
BC2	GROUND	D11 L	AK2
BD1	GROUND	D12 L	AK1
BD2	BR 4 L	D13 L	AL2
BE1	GROUND	D14 L	AL1
BE2	BG 4 H	D15 L	AM2
BF1	ACLO L	GROUND	AB2
BF2	DCLO L	GROUND	AC2
BH1	AO1 L	GROUND	AN1
BH2	AO0 L	GROUND	AP1
BJ1	AO3 L	GROUND	AR1
BJ2	AO2 L	GROUND	AS1
BK1	AO5 L	GROUND	AT1
BK2	AO4 L	GROUND	AV2
BL1	AO7 L	GROUND	BB2
BL2	AO6 L	GROUND	BC2
BM1	AO9 L	GROUND	BD1
BM2	AO8 L	GROUND	BE1
BN1	A11 L	GROUND	BT1
BN2	A10 L	GROUND	BV2
BP1	A13 L	INIT L	AA1
BP2	A12 L	INTR L	AB1
BR1	A15 L	MSYN L	BV1
BR2	A14 L	NPG H	AU1
BS1	A17 L	NPR L	AS2
BS2	A16 L	PA L (D16 L)	AM1
BT1	GROUND	PB L (D17 L)	AN2
BT2	C1 L	+5 V*	AA2
BU1	SSYN L	+5 V*	BA2
BU2	CO L	SACK L	AR2
BV1	MSYN L	DCLO L	BF2
BV2	GROUND	SSYN L	BU1

NOTES

- +5 V is wired to these pins to supply power to the bus terminator only.
- +5 V should never be connected via the Unibus between system units.

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GENERAL POWER SUPPLY SPECIFICATIONS

The following voltage measurements are to be made from the backplane of the option.

POWER SUPPLY TYPE	OUTPUT	TOLERANCE		MAXIMUM RIPPLE IN MILLIVOLTS
		MAXIMUM	MINIMUM	
702		VARIABLE		600
703	+10	+11.0	+9.4	300
	+1.8	+1.9	+1.7	N/A
	-3.0	-3.15	-2.85	N/A
705	+10	+11.0	+9.4	300
	-15	-16.5	-14.5	700
706	+50	+54.0	+49.0	1500
723	+8	+9.5	+7.8	600
725	-15	-18.0	-14.7	900
728	+10	+11.0	+9.5	700
	-15	-16.0	-14.5	700
732		VARIABLE		600
739	+53	+55	+52	250
	+65	+65	+63	250
742/7420	+25 V	+30	+20	N/A
	-15	-16.5	-13.5	N/A
	+3	+3.5	+2.5	N/A
744	+5	+5.05	+4.95	150
745	-15	-15.05	-14.95	450
754	+20	+20.2	+19.8	450
	-5	-5.05	-4.95	150
761	-2	NONE		
	-5.2	NONE		
770	+15	+15.05	+14.95	450
778	-15	-16.5	-14.5	700
7131	+5	+5.07	+4.93	50
	+12	+12.18	+11.82	100
	-2	-2.03	-1.97	50
	-5.2	-5.28	-5.12	50

KL10-BASED SYSTEM AND PROCESSOR DESIGNATIONS

The following tables summarize the differences between the various KL10-based DECSYSTEM-10, DECSYSTEM-20, and KL10 processors. Consult the Option/Module List for a complete list of the differences.

KL10 System Designations

Designation	Description
1080	KL10-A(PA) running TOPS-10
1088	Dual processor (1080) system
1090	KL10-B(PA) or KL10-D(PV) running TOPS-10
1090T	KL10-BC(PA) running TOPS-20 (ARPANET system only)
1091	KL10-E(PV) with cache running TOPS-20 *
1092	KL10-E(PV) with cache and MOS memory running TOPS-10
1099	Dual processor (1090) system
2040	KL10-C(PA) or KL10-E(PV) running TOPS-20
2050	KL10-C(PA) or KL10-E(PV) with cache running TOPS-20
2060	KL10-E(PV) with MOS memory

\* A KL10-E(PV) on a DECSYSTEM-1091 has a DIB20 I/O Bus adapter.

KL10 Processor Designations

Designation	PV	FE TYPE	CACHE	INT CHAN	MAX NO. OF		DIA	DMA
					DTEs	RH20s		
KL10-A	NO	10	YES	NO	1	0	YES	YES
KL10-B	NO	10	YES	YES	4	8	YES	YES
KL10-BC	NO	20	YES	YES	4	8	YES	YES
KL10-C	NO	20	OPTIONAL	YES	4	8	NO	NO
KL10-D	YES	10	YES	YES	4	8	YES	YES
KL10-E	YES	20	OPTIONAL	YES	4	8	*	NO

NOTES

1. KL10-PA (Model A) A basic ECL processor with slots for cache and internal channels. Unofficially, this processor is referred to as the Model A machine.
2. KL10-PV (Model B) A KL10-PA which has been modified to include extended addressing, more extensive microcode, and a faster clock. Unofficially, this processor variation is referred to as the Model B machine.

KL10A, B, or C MODEL A(PV) SYSTEM REVISION  
VRS MODULE REVISION COMPATIBILITY

MODULE TYPE	CPU-PA MODULE REVISION COMPATIBILITY			
	10	10A	10B	11
M8510	A	A	A	A
M8511	B,C	B,C	B,C	B,C
M8512	A,B,C	A,B,C	A,B,C	A,B,C
M8513	D1,F	D1,F	D1,F	D1,F
M8516	D,E	D,E	D,E	D,E
M8517	B	B	B	B
M8518	B	B	B	B
M8519	A,B,C	A,B,C	A,B,C	A,B,C
M8520	D	D	D	D
M8522	A	A	A	A
M8523	B,C	B,C	B,C	B,C
M8524	D,E	D,E	D,E	D,E
M8525	E,F,H	E,F,H	E,F,H	E,F,H
M8526	F<H	F<H	F<H	F<H
M8527	E	E	E	E
M8528	B	B	B	B
M8529	C,C1,D	C,C1,D	C,C1,D	C,C1,D
M8530	D	D	D	D
M8531	B,C	B,C	B,C	B,C
M8532	D,E	D,E	D,E	D,E
M8537	C,D	C,D	C,D	C,D
M8538	C,D	C,D	C,D	C,D
M8539	B	B	B	B
MODULE TYPE	CACHE MODULE REVISION COMPATIBILITY			
	10	10A	10B	11
M8514	A	A	A	A
M8515	B	B	B	B
M8521	A	A	A	A
MODULE TYPE	CACHE SUBSTITUTE MODULE REVISION			
	10	10A	10B	11
M8549YE	A	A	A	A
M8549YF	A	A	A	A
M8549YH	B	B	B	B
MODULE TYPE	CHANNEL MODULE REVISION COMPATIBILITY			
	10	10A	10B	11
M8533	C	C	C	C
M8534	C,D	C,D	C,D	C,D
M8535	C,D	C,D	C,D	C,D
M8536	D,E	D,E	D,E	D,E
MODULE TYPE	CHANNEL SUBSTITUTE MODULE REVISION			
	10	10A	10B	11
M8549YA	A	A	A	A
M8549YC	A	A	A	A
M8549YD	B	B	B	B
MODULE TYPE	RB20/DTE MODULE REVISION COMPATIBILITY			
	10	10A	10B	11
M8552	E,F	E,F	E,F	E,F
M8553	H,J,K,L	H,J,K,L	H,J,K,L	H,J,K,L
M8554	D,F	D,F	D,F	F
M8555	C,D,E	C,D,E	C,D,E	D,E
M8556	C,D<E<F	C,D<E<F	C,D<E<F	D<E<F
M8557	C	C	C	D
M8559	A	A	A	A
MODULE TYPE	DMADIA MODULE REVISION COMPATIBILITY			
	10	10A	10B	10B
M8550	B,C	B,C	B,C	B,C
M8551	C	C	C	C
M8558	B,C,D	B,C,D	B,C,D	B,C,D
M8560	B,C	B,C	B,C	B,C
M8563	D,D1	D,D1	D,D1	D,D1
	E,F	E,F	E,F	E,F



KD10D OR E MODEL B(PV) SYSTEM REVISION VRS  
MODULE REVISION COMPATIBILITY

MODULE TYPE	CPU-PV MODULE REVISION COMPATIBILITY		
	2	2A	3
M8512	B,C	B,C	B,C
M8513YA	B	B	B
M8514	A	A	A
M8515	B	B	B
M8516	D,E	D,E	D,E
M8517	B	B	B
M8518YA	A	A	A
M8519	C	C	C
M8520YA	A	A	A
M8521	A	A	A
M8522	A	A	A
M8524	D,E	D,E	D,E
M8525	H	H	H
M8526YA	B	B	B
M8529YA	A	A	A
M8531YA	A	A	A
M8532	D,E	D,E	D,E
M8533	C	C	C
M8534	C,D	C,D	C,D
M8535	D	D	D
M8536	E	E	E
M8537	D	D	D
M8538	C,D	C,D	C,D
M8540	A	A	A
M8541	A	A	A
M8542	A	A	A
M8543	A	A	A
M8544	A	A	A
M8545	A	A	A
M8548	A	A	A
MODULE TYPE	CACHE SUBSTITUTION		MODULE REVISION
	10A	10B	11
M8549YA	A	A	A
M8549YC	A	A	A
M8549YD	B	B	B
M8549YE	A	A	A
M8549YF	A	A	A
M8549YH	B	B	B
MODULE TYPE	RH20/DTE MODULE REVISION COMPATIBILITY		
	10A	10B	11
M8552	E,F	E,F	E,F
M8553	J,K,L	J,K,L	J,K,L
M8554	F	F	F
M8555	C,D,E	C,D,E	D,E
M8556	C<D<E<F	C,D<E<F	D<E<F
M8557	C	C	D
M8559	A	A	A
MODULE TYPE	DMADIA MODULE REVISION COMPATIBILITY		
	10A	10B	11
M8550	B,C	B,C	B,C
M8551	C	C	C
M8558	C,D	C,D	C,D
M8560	C	C	C
M8563	D1,F	D1,F	D1,F

NOTE  
Refer to LCCOMP (purple microfiche) for future revision level changes.

GEN. INFO.

KL10-PA DRAWING INDEX

Module Type	Index Name	Module Description
M8563	AI1 AI2 AI3 AI4 AI5	ADAPTER INTERFACE DM20 BOARD 2 ADDRESS BUFFERS DM20 BOARD 2 BUSSE SELECTION DM20 REQUEST LOGIC DM20 BOARD 3 TIMING LOGIC DM20 BOARD 2
M8539	APR1-6	APR BOARD
M8559	APR7	APR POWER, GND, CAPS
M8514	CDS3	I/O BOX CLOCK DISTRIBUTION
	CHA1	CACHE DIRECTORY 0, 1 BITS 14-25
	CHA2	CACHE DIRECTORY 2, 3 BITS 14-25
M8521	CHA3 CHA4 CHA5 CHA6 CHD1	CACHE DIRECTORY BIT 26 AND WRITTEN 1 CACHE DIRECTORY PARITY BITS CACHE DIRECTORY POWER, GND, CAPS CACHE DIRECTORY TERMINATORS CACHE DATA BITS [N] - [N+02]
	CHD2	CACHE DATA BITS [N+03] - [N+05]
	CHD3	CACHE DATA BITS [N+06] - [N+08]
	CHD4	CACHE DATA ADDRESSING LOGIC
	CHD5	CACHE DATA PARITY BITS
	CHD6	CACHE DATA POWER, GND, CAP
M8515	CHD7 CHX1 CHX2 CHX3 CHX4	CACHE DATA TERMINATORS CSH ADR COMPARITORS AND VAL BIT MIXERS CHS VAL BITS AND ADR MIXERS CACHE USE BITS CSH DIR PAR CHECKERS AND DIAG MIXERS
M8551	CHX5	CACHE DIRECTORY POWER AND GND
	CHX6	CACHE EXTENSION TERMINATORS
	CL1-3	IBUS ADAPTER INTERFACE
M8526	CL4 CLK1	I/O BUS ADAPTER INTERFACE CLK CONTROL CLOCK CONTROL
M8553	CLK2, 4 CLK3 CLK5 CLK6 CNT0-7	CLK CONTROL DIAGNOSTIC CONTROL CLK CONTROL EBOX CLK CONTROL CLOCK CONTROL DIAGNOSTICS EMBOX CLOCK TERMINATORS DTE20 CONTROL LOGIC
M8525	CON1-5	EBOX CONTROL #2
M8511	CON6 CRA2 CRA3, 4 CRA5	CON POWER, GND, CAPS CONTROL RAM ADR CRADR 07-10 CONTROL RAM ADR EBUS, SBR CONTROL RAM ADR RAM
M8528	CRA6 CRM1 CRM2 CRM3 CRM4	CONTROL RAM ADR POWER, GND, CAPS CONTROL RAM INPUT SIGNALS CONTROL RAM CRAM 00-19 CONTROL RAM CRAM 20-39 CONTROL RAM CRAM 40-59
M8513	CRM5 CRM6	CONTROL RAM OUTPUT SIGNALS CONTROL RAM POWER, GND, CAPS
M8527	CSH1-7 CSH8 CTL1-3	CACHE CONTROL MBOX CONTROL - CSH POWER, GND, CAP EBOX CONTROL #1
M8550	CTL4	CTL POWER, GND, CAPS
M8552	DLH1-4	IBUS ADAPTER DATA PATH
M8512	DLH5 DPS1-7 EPD1	IBUS ADAPTER DATA PATH LEFT DTE20 DATA PATH AND STATUS DATA PATH AR REGISTERS
M8554	EDP2 EDP3 EDP4 EDP5 INT1, 2	DATA PATH ARX, MQ REGISTERS DATA PATH AD, ADX, ADDER DATA PATH EBUS, FM, BR, BRX REGISTERS EBOX DATA PATH POWER, GND, CAPS DTE20 UNIBUS INTERRUPT CONTROL
M8522	IR1 IR2 IR3 IR4 IR5	IR, DRAM & CARRY IR REG, DRAM BUFF IR, DRAM & CARRY DRAM IR, DRAM & CARRY DIAG REG & MISC IR, DRAM & CARRY ADD CARRY NETOWKR IR, DRAM & CARRY POWER, GND, CAPS
M8558	KI81-5	KI MEMORY BUS ADAPTER

KL10-PA DRAWING INDEX (Cont)

Module Type	Index Name	Module Description
M8561 M8562 M8517	MAC1-6 MAT1-2 MB1-5 MB6	MA20 CONTROL BOARD MA20 TIMING BOARD MB BOARD MEMORY BUFFER POWER, GND, CAPS
M8531 M8529 M8537	MBC1-5 MBC6 MBX1-6 MBX7 MBZ1-6	MBOX CONTROL #5 MBC POWER, GND, CAPS MBOX CONTROL LOGIC MBX TERMINATORS MBOX CONTROL #4
M8530 M8519 M8538	MBZ7 MCL1-6 MCL7 MEM1-6 MTR1	MBOX CONTROL - MBZ POWER, GND, CAPS MEMORY CONTROL MCL POWER, GND, CAPS INTERNAL MEMORY BUS TRANSLATOR METER COUNTERS
	MTR2 MTR3 MTR4 MTR5 MTR6	ACCOUNTING ENABLES AND 1 MHZ CLOCKS INTERVAL TIMER PERFORMANCE ANALYSIS EBUS MIXERS AND BUFFERS METERS POWER, GND, CAPS
M8520	PAG1 PAG2 PAG3 PAG4 PAG5	PAGE TABLE DATA PT ACCESS-PT-17 PAGE TABLE DATA PT 16-PT-26 PAGE TABLE DIRECTORY PAGE TABLE CONTROL LOGIC PAGE TABLE PARITY LOGIC
M8532	PAG6 PI1 PI2 PI3 PI4	PAGING BOARD POWER, GND, CAPS PRIORITY INTERRUPT REGISTERS PRIORITY INTERRUPT DEVICE SELECTION PRIORITY INTERRUPT CHANNELS PRIORITY INTERRUPT EBUS INTERFACE
M8518	PI5 PI6 PMA1 PMA2 PMA3	PRIORITY INTERRUPT CONTROL PI POWER, GND, CAPS PHYSICAL MEM ADR EBR, UBP, UEBR & VMA PHYSICAL MEM ADR CACHE CLR ADR PHYSICAL MEM ADR PA 14-31
M8524	PMA4 PMA5 PMA6 SCD1 SCD2	PHYSICAL MEM ADR ERA, PA 32-35 & PMA PHYSICAL MEM ADR SELECTION LOGIC PHYSICAL MEM ADR POWER, GND, CAPS SCAD, PC FLAGS SCADD, SCADA, SCADB SCAD, PC FLAGS SC, SCM, FE
M8510	SCD3 SCD4, 5 SH1 SH2 SH3	SCAD, PC FLAGS ARM DIAG MIXER SCAD, PC FLAGS PC FLAGS SHIFT MATRIX CONTROL SHIFT MATRIX SHIFT 16, 32 SHIFT MATRIX SHIFT 4, 8
M8560	SH4 SH5 SH6 SIC1 SIC2	SHIFT MATRIX SHIFT 1, 2 SHIFT MATRIX POWER, GND, CAPS SHIFT REGISTER TERMINATORS SBUS INTERFACE CONTROL BOARD ERROR AND DIAGNOSTIC DMA 20 BOARD
M8516 M8523	SIC3 SIC4 TRM2-5 VMA1 VMA2	CLOCK LOGIC DMA20 BOARD 1 (2 OF 3) TIMING LOGIC DMA20 BOARD 2 E AND C BUS TRANSLATOR VIRTUAL MEM ADR ADDER & CONTROL VIRTUAL MEM ADR VMA REGISTER
	VMA3 VMA4 VMA5 VMA6	VIRTUAL MEM ADR PC & ADR BRK REG VIRTUAL MEM ADR VMA - HELD REGISTER VIRTUAL MEM ADR DIAGNOSTICS VIRTUAL MEM ADR POWER, GND, CAPS

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NOTE

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for future inclusion of KL10-PV Drawing  
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NOTE

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GEN. INFO.

GRAM BIT LOCATIONS

GRAM BITS SORTED BY LOCATION

LOCATION	FUNCTION	PHYSICAL BIT	LOCATION	FUNCTION	PHYSICAL BIT
A40R2	FM ADR SEL 1	58	D44R2	ARXM SEL 2	68
A40V2	COND 05	59	D44V2	J 04	69
B40F1	# 09	39	E44D2	J 03	68
B40F2	COND 02	19	E44P2	# 00	29
C40F2	TIME 01	78	E44S2	ADB SEL 2	28
C40J2	# 07	38	F44K2	MEM 01	49
C40K2	COND 01	18	F44P2	MEM 00	48
D40R2	TIME 00	76	D45M2	DISP00	81
D40V2	COND 00	17	D45T2	DISP01	82
E40D2	MQ SEL	16	E45F1	DISP02	83
E40P2	# 06	37	E45M2	DISP03	84
E40S2	ARXM SEL 4	36	E45S2	DISP04	85
E40K2	FM ADR SEL 2	57	A50R2	SH-ARMM SEL 2	46
E40P2	FM ADR SEL 4	56	A50V2	SH-ARMM SEL 1	47
A42P1	BRX LOAD	54	B50A1	ADA SEL 1	27
A42V2	COND 04	55	B50P2	J 02	07
B42F1	# 05	35	C50F2	ARM SEL 1	96
B42P2	J 10	15	C50J2	ADA SEL 2	26
C42F2	AD CRY	74	C50K2	J 01	06
C42J2	# 04	34	D50R2	ARM SEL 2	64
C42K2	J 09	14	D50V2	J 00	05
D42R2	VMA SEL 1	72	E50D2	FE LOAD	04
D42V2	J 08	13	ES0L1	ADA DISABLE	25
E42D2	J 07	12	ES0S1	AD BOOLE	24
E42P2	# 03	33	E50K2	ARM SEL 4	45
E42S2	ADB SEL 1	32	E50P2	VMA SEL 2	44
F42K2	COND 03	53			
F42P1	BR LOAD	52	A52R2	SCADB SEL 2	42
			AS2V2	MARK BIT	43
A44R2	MEM 02	50	B52F1	AD SEL 1	23
A44V2	MEM 03	51	B52P2	SCAD 1	03
B44F1	# 02	31	C52F2	SCM SEL 2	62
B44P2	J 06	11	C52J2	AD SEL 2	22
C44F2	ARXM SEL 1	70	C52K2	SCAD 2	02
C44J2	# 01	30	D52R2	SCADB SEL 1	60
C44K2	J 05	10	D52V2	SCAD 4	01
			E52D2	SCADA EN L	00
			E52P2	AD SEL 4	21
			E52S1	AD SEL 8	20
			F52K2	SCADA SEL 1	41
			F52P2	SCADA SEL 2	40

GRAM BITS SORTED BY FUNCTION

FUNCTION	PHYSICAL BIT	LOCATION	FUNCTION	PHYSICAL BIT	LOCATION
AD SEL 1	23	B62F1	AD SEL 2	22	C52J2
AD SEL 4	21	E52P2	AD SEL 8	20	E52S1
AD BOOLE	24	E50S1	AD CRY	74	C42F2
ADA SEL 1	27	B50A1	ADA SEL 2	26	C50J2
ADA DISABLE	25	E50L1	ADB SEL 1	32	E42S2
ADB SEL 2	28	E44S2	ARM SEL 1	66	C50F2
ARM SEL 2	64	D50R2	ARM SEL 4	45	F50K2
ARXM SEL 1	70	C44F2	ARXM SEL 2	68	D44R2
ARXM SEL 4	36	E40S2	BR LOAD	52	F42P1
BRX LOAD	54	A42P1	COND 00	17	D40V2
CALL	80	*	COND 02	19	B40P2
COND 01	18	C40K2	COND 04	55	A42V2
COND 03	53	F42K2	FE LOAD	04	E50D2
COND 05	59	A40V2	FM ADR SEL 2	57	F40K2
DISP00	81	D45M2	J 00	05	D60V2
DISP01	82	D45T2	J 02	07	B60P2
DISP02	83	E45F1	J 04	09	D44V2
DISP03	84	E45M2	J 06	11	B44P2
DISP04	86	E45S2	J 08	13	D42V2
FM ADR SEL 1	58	A40R2	J 10	15	B42P2
FM ADR SEL 4	56	F40P2	MEM 01	49	F44K2
J 01	06	C50K2	MEM 03	51	A44V2
J 03	08	E44D2	# 00	29	E44P2
J 05	10	C44K2	# 02	31	B44F1
J 07	12	E42D2	# 04	34	C42J2
J 09	14	C42K2	# 05	37	E40P2
MEM 00	48	F44P2	# 08	38	B40F1
MEM 02	50	A44R2	SCAD 2	02	C52K2
MQ SEL	16	E40D2	SCADA EN L	00	E52D2
# 01	30	C44J2	SCADA SEL 2	40	F52P2
# 03	33	E42P2	SCADB SEL 2	42	A52R2
# 05	35	B42F1	SH-ARMM SEL 2	46	A50R2
# 07	38	C40J2	TIME 00	76	D40R2
SCAD 1	03	B52P2	VMA SEL 1	72	D42R2
SCAD 4	01	D52V2	MARK BIT	43	A52V2
SCADA SEL 1	41	F52K2			
SCADA SEL 2	40	D52R2			
SH-ARMM SEL 1	47	A50V2			
SCM SEL 2	62	C52F2			
TIME 01	78	C40F2			
VMA SEL 2	44	F50P2			

CRAM SORTED BY BITS

PHYSICAL BIT	FUNCTION	LOCATION	PHYSICAL BIT	FUNCTION	LOCATION
00	SCADA EN L	E50D2	36	# 05	B42F1
01	SCAD 4	D52V2	36	ARMX SEL 4	E40S2
02	SCAD 2	C52K2	37	# 06	E40P2
03	SCAD 1	B52P2	38	# 07	C40J2
04	FE LOAD	E50D2	39	# 08	B40F1
05	J 00	D50V2	40	SCADA SEL 2	F52P2
06	J 01	C50K2	41	SCADA SEL 1	F52K2
07	J 02	B50P2	42	SCADB SEL 2	A52R2
08	J 03	E44D2	43	MARK BIT	A52V2
09	J 04	D44V2	44	VMA SEL 2	F50P2
10	J 05	C44K2	45	ARM SEL 4	F50K2
11	J 06	B44P2	46	SH ARMM SEL 2	A50R2
12	J 07	E42D2	47	SH ARMM SEL 1	A50V2
13	J 08	D42V2	48	MEM 00	F44P2
14	J 09	C42K2	49	MEM 01	F44K2
15	J 10	B42P2	50	MEM 02	A44R2
16	MG SEL	E40D2	51	MEM 03	A44V2
17	COND 00	D40V2	52	BR LOAD	F42P1
18	COND 01	C40K2	53	COND 03	F42K2
19	COND 02	B40P2	54	BRX LOAD	A42P1
20	AD SEL 8	E52S1	55	COND 04	A42V2
21	AD SEL 4	E52P2	56	FM ADR SEL 4	F40P2
22	AD SEL 2	C52J2	57	FM ADR SEL 2	F40K2
23	AD SEL 1	B52F1	58	FM ADR SEL 1	A40R2
24	AD BOOLE	E50S1	59	COND 05	A40V2
25	ADA DISABLE	E50L1	60	SCADB SEL 1	D52R2
26	ADA SEL 2	C50J2	62	SCM SEL 2	C52F2
27	ADA SEL 1	B50A1	64	ARM SEL 2	D50R2
28	ADB SEL 2	E44S2	66	ARM SEL 1	C50F2
29	# 00	E44D2	68	ARMX SEL 2	D44R2
30	# 01	C44J2	70	ARMX SEL 1	C44F2
31	# 02	D44F1	72	VMA SEL 1	D42R2
32	ADB SEL 1	E42S2	74	AD CRY	C42F2
33	# 03	E42P2	76	TIME 00	D40R2
34	# 04	C42J2	78	TIME 01	C40F2
			80	CALL	#
			81	DISP00	D45M2
			82	DISP01	D45T2
			83	DISP02	E45F1
			84	DISP03	E45M2
			85	DISP04	E45S2

\*CALL BIT IS USED IN KL10(PV) ONLY. THERE IS NO LOGIC FOR IT IN THE MODEL PA. THE CALL BIT IS NOT ACCESSIBLE ON THE BACKPLANE, IT MUST BE READ VIA A DIAGNOSTIC READ FUNCTION 141 BIT 00.

C RAM BIT MAP

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
SCADA DIS	SCADA DIS	SCAD 02	FE LOAD	FE LOAD	00	01	02	03	04	J FIELD	05	06	07	08	09
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
NO SEL	CONDITIONS	AD SELECT	AD BOOLE	AD BOOLE	AD A DIS	AD A DIS	AD A SEL	AD A SEL	AD A SEL	AD B SEL	AD B SEL	AD B SEL	AD B SEL	#	#
00	01	02	08	08	04	02	01	01	01	02	01	01	00	01	02
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
AD B SEL	#	#	ARXM	ARXM	SCADA SEL	#	SCADA SEL	SCADA SEL	SCADA SEL	SCAD B SEL	MARK	VMA	ARM	SH/ARMM	SEL 1
03	04	05	SEL4	SEL4	06	07	08	02	01	SEL2	SEL2	SEL2	SEL4	SEL2	SEL1

COMPANY CONFIDENTIAL

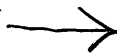
BITS	<06:03>	<04:07>	<08:11>	<12:15>	<16:19>	<20:23>	<24:27>	<28:31>	<32:35>	<36:39>	<40:43>	<44:47>	<48:51>	<52:55>	<56:59>	<60:62>	<64:66>	<68:70>	<72:74>	<76:78>	<80:85>
SLOT	52	50	44	42	40	52	50	44	42	40	52	50	44	42	40	52	50	44	42	40	45

MR-2212



48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
00	MEMORY 01 02 03	BR LOAD	COND 03	BRX LOAD	COND 04	FM ADR 02 01	COND 06	SCADB SEL1	SCM SEL2						
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
ARM SEL2	ARM SEL1	ARM SEL1	ARXM SEL2	ARXM SEL1	COND 04	BRX LOAD	COND 04	VMA SEL1	AD CRY	TIME 00	TIME 01				
80	81	82	83	84	85										
CALL	00	01	02	03	04										

M8548



M8541

KLDCP EC AND DC COMMAND DATA FORMAT

ADR/J	T	AR	AD	BR	MQ	FM	SCAD	SC	FE	SH	#	VMA	MEM	COND	SPEC	M	
3777	3	77	3777	3	1	7	377	1	1	3	777	3	17	77	77	1	
SEE NOTE																	
00	A+C	ARITH	10-17	AR/ARX	00-07	BOOLE	10-17	COND	00-07	COND	10-17	COND	30-37	COND	40-47	COND	50-57
01	A-B-1+C	ORCB+C	A-B-1+C	AR/ARX	SETCA	ANDCA	XOR	LD AR0-8	PCF-#	FM WRITE	DIAG FUNC	VMA-#	VMA-#*TRP	EVEN PAR	SCAD0	SCAD0	SCAD0
02	A#2+C	A-B-1+C	A-B-1+C	CACHE	ORC	XOR	B	LD AR9-17	FE SHRT	PCF-#	EBOX STATE	VMA-##MODE BRD	VMA-##MODE BRD	ARX0	ADXR0	ADXR0	ADXR0
03	A#2+C	-1+C	-1+C	AD	ORCA	OR	OR	LD ARR	AD FLAGS	AD FLAGS	MBOX CTL	VMA-##PI*2	VMA-##PI*2	AR18	AD CRY0	AD CRY0	AD CRY0
04	A+B+C	AND-1+C	AND-1+C	EBUS/MQ	1S	ANDC	ANDCB	ARX CLR	LOAD IR	LOAD IR	SPEC INSTR	VMA INC	VMA INC	AC#0	AD#0	AD#0	AD#0
05	A+B+C	AND-1+C	AND-1+C	SH	SETCB	AND	AND	ARL IND	SR-#	SR-#	LD VMA HLD	LD VMA HLD	LD VMA HLD	SC0	AD#0	AD#0	AD#0
06	A+B+C	A-1+C	A-1+C	AD*2	EOV	ORCB	A	REG CTL	SEL VMA	SEL VMA							
07	A+B+C	A-1+C	A-1+C	AD*25	ORCB	ORCB	A										

NOTE: AR FIELD INCLUDES AR AND ARX  
 AD FIELD INCLUDES ADA AND ADB  
 SCAN FIELD INCLUDES SCADA AND SCADB.

MR-2210

COND 60-67	COND 70-77	FMADR 00-07	MEM 00-07	MEM 10-17	SCAD 00-07	SPEC 00-07	SPEC 10-17	SPEC 20-27	SPEC 30-37
00 FETCH	INTRPT	AC0	ARL IND	A INDRCT	A	DIAG	INH CRY18	SEC HOLD	MUL
01 KERNEL	-START	AC1	MB WAIT	BYTE INDRCT	A-B-1	DRAM J	MQ SHIFT	CALL	DIV
02 USER	RUN	XR	SEC 0	LOAD AR	A-B	A READ	SCM ALT	ARL IND	SIGNS
03 PUBLIC	IO LEGAL	VMA	A READ	LOAD ARX	A-1	RETURN	CLR FPD	MTR CTL	DRAM B
04 RPW CYCLE	PIS XCT	AC2	B WRITE	AD FUNC	A-1	PF DISP	LOAD PC	FLG CTL	BYTE
05 P1 CYCLE	AC REF	AC3	FETCH	BYTE READ	A-B	SR	XCRY ARO	SV FLGS	NORM
06 -EBUS GRNT	-MTR REQ	AC+#	REG FUNC	WRITE	OR	NICOND	GEN CRY18	SP MEM	EA MOD
07 -EBUS XFER		#8#		RPW	AND	SH 0-3		AD LONG	EA TYPE
ADA	ADB	SCADB	SH	ARMM	VMA				
0	FM	SC	SHIFT	#	VMA				
1	BR*2	AR0-5	AR	AR SIGN	PC				
2	BR	AR0-8	ARX	EXP	PC+1				
3	AR*4	#	AR SWAP	POS	AD				

MR-2211

BASIC INSTRUCTION (KA10, KI10 AND KL10)

00	08	09	12	13	14	17	18	35
INSTRUCTION CODE (INCLUDING MODE)			A	F	I	X		Y

MR-3953

IN-OUT INSTRUCTION (KA10, KI10 and KL10)

00	01	02	03	09	10	12	13	14	17	18	35
1	1	1		DEVICE CODE		INSTRUC. TION CODE	I	X		Y	

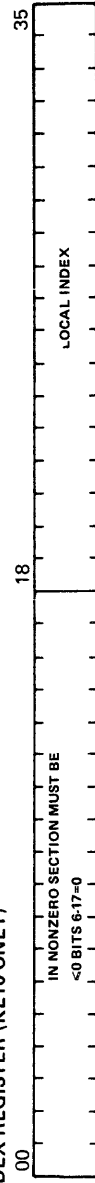
MR-3954

INSTRUCTIONS EXECUTED UNDER EXTEND (KL10 ONLY)

00	08	09	12	13	14	17	18	35
INSTRUCTION CODE			0	0	0	I	X	Y

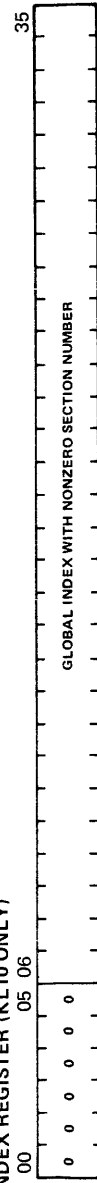
MR-3955

LOCAL INDEX REGISTER (KL10 ONLY)



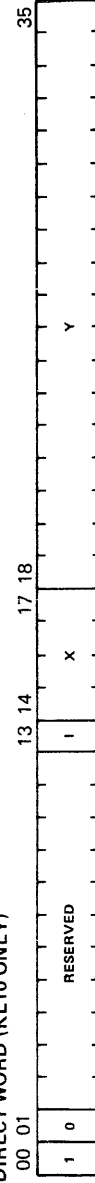
MR-3956

GLOBAL INDEX REGISTER (KL10 ONLY)



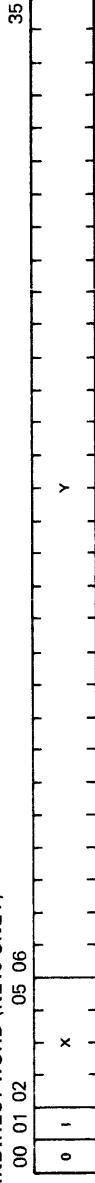
MR-3957

LOCAL INDIRECT WORD (KL10 ONLY)



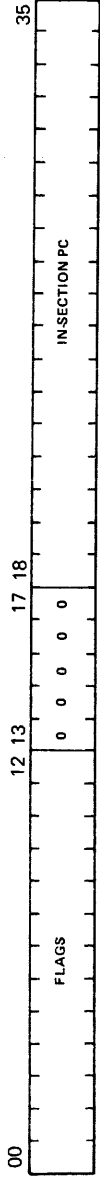
MR-3958

GLOBAL INDIRECT WORD (KL10 ONLY)



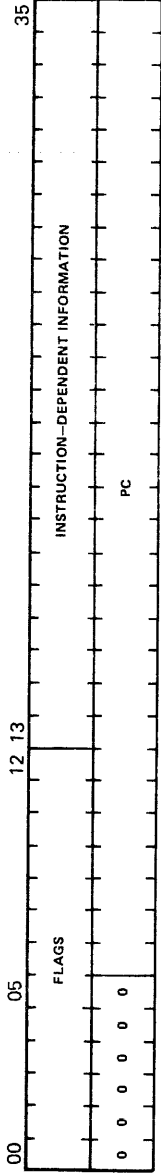
MR-3959

PC WORD (KA10, KI10 AND KL10)



MR-3960

PC DOUBLEWORD (KL10 ONLY)



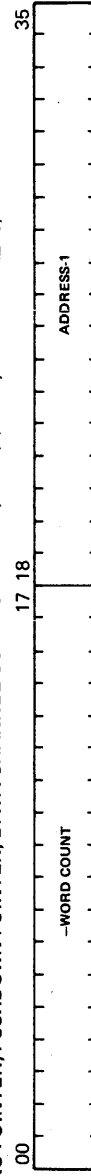
MR-3961

PC FLAGS (KI10 AND KL10 ONLY)

00	01	02	03	04	05	06	07	08	09	10	11	12
OVER FLOW	CARRY 0 1	FLOAT OV/FLO	FPD	USER	USER IOT	PUB	ADDR INH	TRAP 2 1	FLOAT UNFLO	NO DIV		

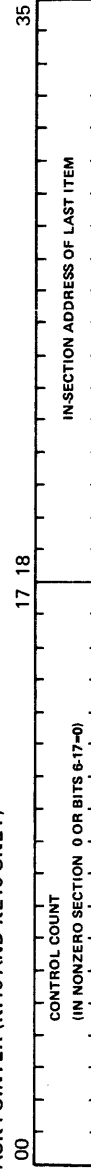
MR-3962

BLKI/BLKO POINTER, PUSHDOWN POINTER, DATA CHANNEL CONTROL WORD (IOWD) (KA10, KI10 AND KL10)



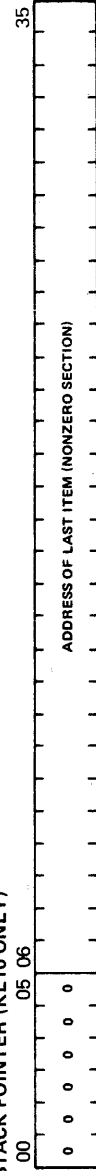
MR-3965

LOCAL STACK POINTER (KI10 AND KL10 ONLY)

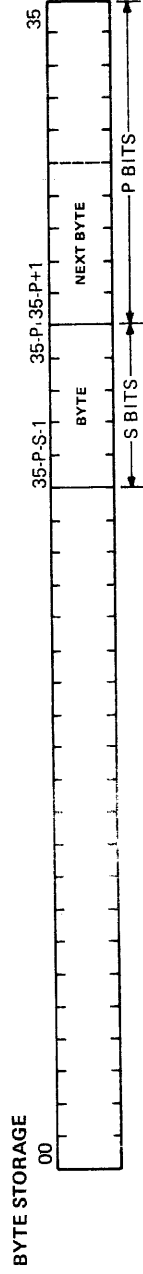
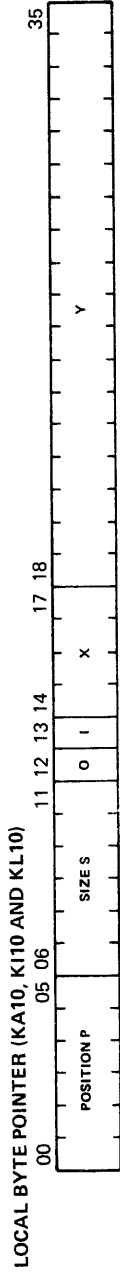


MR-3963

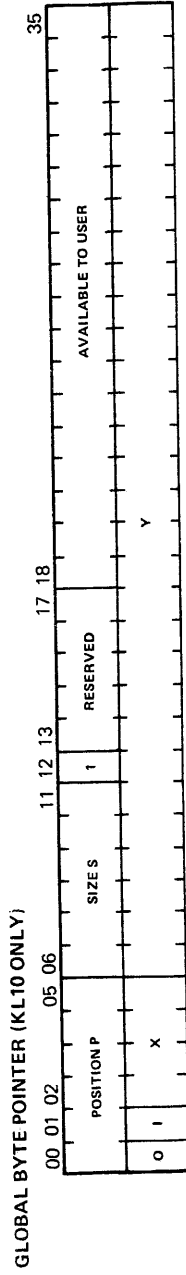
GLOBAL STACK POINTER (KL10 ONLY)



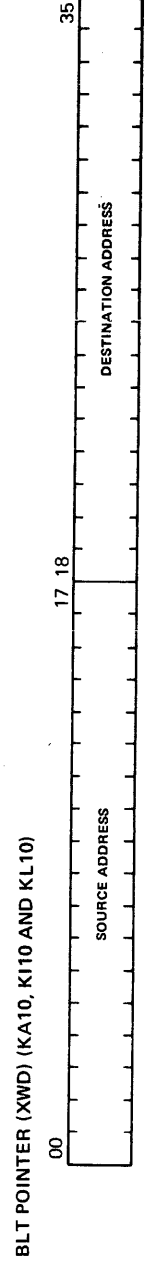
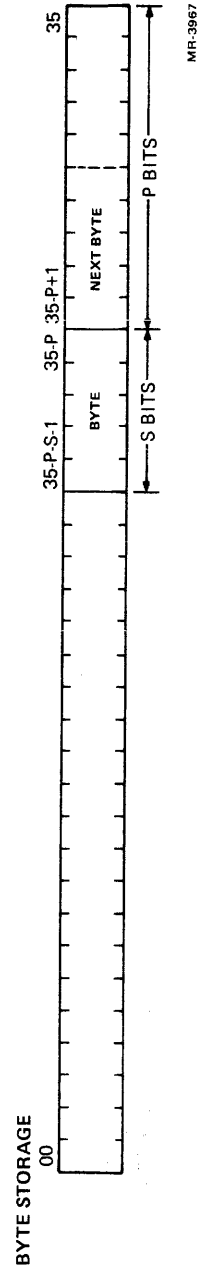
MR-3964



MR-3966





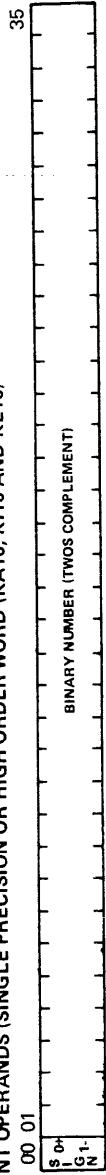


XBLT POINTER (KL10 ONLY)

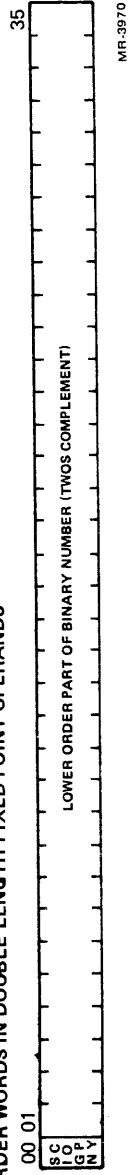
00	05 06	35
AC	NUMBER OF WORDS IN BLOCK	
AC*1	0 0	LOCATION OF SOURCE BLOCK
AC*2	0 0	LOCATION OF DESTINATION BLOCK

MR-3969

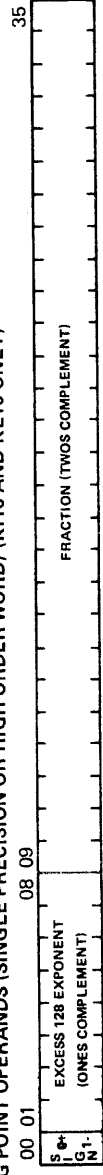
FIXED POINT OPERANDS (SINGLE PRECISION OR HIGH ORDER WORD (KA10, K110 AND KL10))



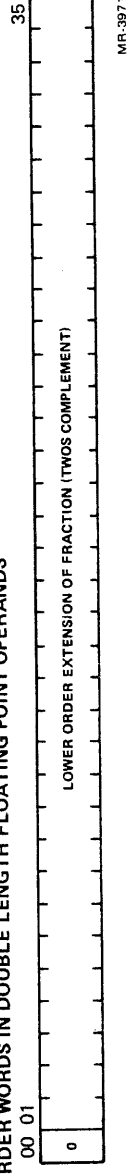
LOWER ORDER WORDS IN DOUBLE LENGTH FIXED POINT OPERANDS



FLOATING POINT OPERANDS (SINGLE PRECISION OR HIGH ORDER WORD) (K110 AND KL10 ONLY)



LOWER ORDER WORDS IN DOUBLE LENGTH FLOATING POINT OPERANDS



DEVICE CODE AND MNEMONICS

SECOND AND THIRD OCTAL DIGITS  
FIRST OCTAL DIGIT

0	04	10	14	20	24	30	34	40	44	50	54	60	64	70	74
APR CPA CENTRAL PROCESSOR	PI PRIORITY INTERRUPT	PAG K110 PAGING	CCA CACHE	TTM K110 TELETYPE LOGIC	MTR ACCOUNTING LOGIC	ADC2 ANALOG DIGITAL CONVERTER	PDC3 MAGNETIC TAPE	XY10 PLOTTER	XY10 PLT PLOTTER	XY10 PLT2 PLOTTER	CR10 CARD READER	DLB PDP-11 DATA LINK	DL10 DLC DATA LINK	CLK TIME CLOCK	DK10 CLK TIME CLOCK
PTP PAPER PUNCH READER	PTR PAPER READER	CDP CARD PUNCH		626 CONSOLE TELETYPE	LPT LINE PRINTER	VP10 DISPLAY	DIS2 DISPLAY	VP10 DISPLAY	CR CARD READER	CR2 CARD READER	CR10 CARD READER	DLB2 PDP-11 DATA LINK	DL10 DLC2 DATA LINK	DSK DISK	DSK2 DISK/DRUM
DTE20 10/11 INTERFACE	DTE20 DTE2 10/11 INTERFACE	DTE3 10/11 INTERFACE	DTE20 DTE4 10/11 INTERFACE	DX10 PDC MAGNETIC TAPE	DX10 PDC2 MAGNETIC TAPE	LF10 LPT2 LINE PRINTER	LF10 LPT2 LINE PRINTER	DC10 DLS DATA LINE SCANNER	DC10 DLS2 DATA LINE SCANNER	DC10 DPC DISK PACK SYSTEM	RP10 DPC2 DISK PACK SYSTEM	RP10 DPC3 DISK PACK SYSTEM	RP10 DPC4 DISK PACK SYSTEM	RC10 RMC DISK CONTROL	RC10 RMC2 DISK CONTROL
	DTE 10/11 INTERFACE	DTE 10/11 INTERFACE		DTC DECTAPE	DTS DECTAPE	TD10 DTC2 DECTAPE	TD10 DTS2 DECTAPE	TMC MAGNETIC TAPE	TMS MAGNETIC TAPE	TMC2 MAGNETIC TAPE	TM10 TMS2 MAGNETIC TAPE	RM10 RMC3 DATA CONTROL	RM10 RMC4 DATA CONTROL	RM10 RMC5 DATA CONTROL	RM10 RMC6 DATA CONTROL
												DSS SINGLE SYNCHRONOUS LINE UNIT	DSI SINGLE SYNCHRONOUS LINE UNIT	DS10 DSS2 SINGLE SYNCHRONOUS LINE UNIT	DS10 DS12 SINGLE SYNCHRONOUS LINE UNIT
								RH20 MBC MASSBUS CONTROL	RH20 MBC2 MASSBUS CONTROL	RH20 MBC3 MASSBUS CONTROL	RH20 MBC4 MASSBUS CONTROL	RH20 MBC5 MASSBUS CONTROL	RH20 MBC6 MASSBUS CONTROL	RH20 MBC7 MASSBUS CONTROL	RH20 MBC8 MASSBUS CONTROL

CODES IN THIS SECTION RESERVED FOR USER SPECIAL DEVICES

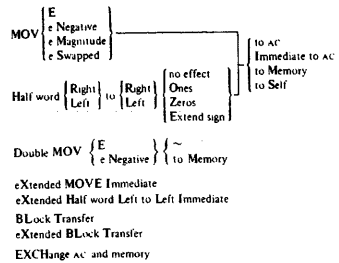
K110 UNRESTRICTED CODES RESERVED FOR DEC

K110 UNRESTRICTED CODES RESERVED FOR DEC

GEN. INFO.

MACHINE LANGUAGE INSTRUCTION SET

Full and Half Word Transmission



Full Word Data Transmission

EXCH	250	(AC) $\leftrightarrow$ (E)			
MOVE	200	(E) $\rightarrow$ (AC)	MOVS	204	(E) <sub>S</sub> $\rightarrow$ (AC)
MOVEI	201	0,E $\rightarrow$ (AC)	MOVSI	205	E,0 $\rightarrow$ (AC)
MOVEM	202	(AC) $\rightarrow$ (E)	MOVSM	206	(AC) <sub>S</sub> $\rightarrow$ (E)
MOVES	203	If AC $\neq$ 0: (E) $\rightarrow$ (AC)	MOVSS	207	(E) <sub>S</sub> $\rightarrow$ (E) If AC $\neq$ 0: (E) $\rightarrow$ (AC)
MOVN	210	- (E) $\rightarrow$ (AC)	MOVMM	214	(E) $\rightarrow$ (AC)
MOVNI	211	- [0,E] $\rightarrow$ (AC)	MOVMI	215	0,E $\rightarrow$ (AC)
MOVNM	212	- (AC) $\rightarrow$ (E)	MOVMM	216	(AC) $\rightarrow$ (E)
MOVNS	213	- (E) $\rightarrow$ (E) If AC $\neq$ 0: (E) $\rightarrow$ (AC)	MOVMS	217	(E) $\rightarrow$ (E) If AC $\neq$ 0: (E) $\rightarrow$ (AC)
XMOVEI	415	If not local AC reference: E $\rightarrow$ (AC) If local AC reference: 1,E $\rightarrow$ (AC)			
DMOVE	120	(E,E+1) $\rightarrow$ (AC,AC+1)	DMOVEM	124	(AC,AC+1) $\rightarrow$ (E,E+1)
DMOVN	121	-(E,E+1) $\rightarrow$ (AC,AC+1)	DMOVNM	125	-(AC,AC+1) $\rightarrow$ (E,E+1)
BLT	251	Move E <sub>R</sub> - (AC) <sub>R</sub> + 1 words starting with ((AC) <sub>L</sub> ) $\rightarrow$ ((AC) <sub>R</sub> )			
XBLT	020	Move  (AC)  words If (AC) > 0: start with ((AC+1)) $\rightarrow$ ((AC+2)) and go up If (AC) < 0: start with ((AC+1) - 1) $\rightarrow$ ((AC+2) - 1) and go down			

Half Word Data Transmission

HLL	500	(E) <sub>L</sub> $\rightarrow$ (AC) <sub>L</sub>	HLLZ	510	(E) <sub>L</sub> ,0 $\rightarrow$ (AC)
HLLI	501	0 $\rightarrow$ (AC) <sub>L</sub>	HLLZI	511	0 $\rightarrow$ (AC)
HLLM	502	(AC) <sub>L</sub> $\rightarrow$ (E) <sub>L</sub>	HLLZM	512	(AC) <sub>L</sub> ,0 $\rightarrow$ (E)
HLLS	503	If AC $\neq$ 0: (E) $\rightarrow$ (AC)	HLLZS	513	0 $\rightarrow$ (E) <sub>R</sub> If AC $\neq$ 0: (E) $\rightarrow$ (AC)
HLLO	520	(E) <sub>L</sub> ,777777 $\rightarrow$ (AC)	HLLE	530	(E) <sub>L</sub> ,[(E) <sub>b</sub> $\times$ 777777] $\rightarrow$ (AC)
HLLOI	521	0,777777 $\rightarrow$ (AC)	HLLEI	531	0 $\rightarrow$ (AC)
HLLOM	522	(AC) <sub>L</sub> ,777777 $\rightarrow$ (E)	HLLEM	532	(AC) <sub>L</sub> ,[(E) <sub>b</sub> $\times$ 777777] $\rightarrow$ (E)
HLLOS	523	777777 $\rightarrow$ (E) <sub>R</sub> If AC $\neq$ 0: (E) $\rightarrow$ (AC)	HLLES	533	(E) <sub>b</sub> $\times$ 777777 $\rightarrow$ (E) <sub>R</sub> If AC $\neq$ 0: (E) $\rightarrow$ (AC)
HLR	544	(E) <sub>L</sub> $\rightarrow$ (AC) <sub>R</sub>	HLRZ	554	0,(E) <sub>L</sub> $\rightarrow$ (AC)
HLRI	545	0 $\rightarrow$ (AC) <sub>R</sub>	HLRZI	555	0 $\rightarrow$ (AC)
HLRM	546	(AC) <sub>L</sub> $\rightarrow$ (E) <sub>R</sub>	HLRZM	556	0,(AC) <sub>L</sub> $\rightarrow$ (E)
HLRS	547	(E) <sub>L</sub> $\rightarrow$ (E) <sub>R</sub> If AC $\neq$ 0: (E) $\rightarrow$ (AC)	HLRZS	557	0,(E) <sub>L</sub> $\rightarrow$ (E) If AC $\neq$ 0: (E) $\rightarrow$ (AC)

HLRO	564	777777,(E) <sub>L</sub> → (AC)	HLRE	574	[(E) <sub>8</sub> × 777777],(E) <sub>L</sub> → (AC)
HLROI	565	777777,0 → (AC)	HLREI	575	0 → (AC)
HLROM	566	777777,(AC) <sub>L</sub> → (E)	HLREM	576	[(AC) <sub>8</sub> × 777777],(AC) <sub>L</sub> → (E)
HLROS	567	777777,(E) <sub>L</sub> → (E) If AC ≠ 0: (E) → (AC)	HLRES	577	[(E) <sub>8</sub> × 777777],(E) <sub>L</sub> → (E) If AC ≠ 0: (E) → (AC)
HRR	540	(E) <sub>R</sub> → (AC) <sub>R</sub>	HRRZ	550	0,(E) <sub>R</sub> → (AC)
HRR1	541	E → (AC) <sub>R</sub>	HRRZI	551	0,E → (AC)
HRRM	542	(AC) <sub>R</sub> → (E) <sub>R</sub>	HRRZM	552	0,(AC) <sub>R</sub> → (E)
HRRS	543	If AC ≠ 0: (E) → (AC)	HRRZS	553	0 → (E) <sub>L</sub> If AC ≠ 0: (E) → (AC)
HRRO	560	777777,(E) <sub>R</sub> → (AC)	HRRE	570	[(E) <sub>16</sub> × 777777],(E) <sub>R</sub> → (AC)
HRROI	561	777777,E → (AC)	HRREI	571	[E] <sub>16</sub> × 777777, E → (AC)
HRROM	562	777777,(AC) <sub>R</sub> → (E)	HRREM	572	[(AC) <sub>16</sub> × 777777],(AC) <sub>R</sub> → (E)
HRROS	563	777777 → (E) <sub>L</sub> If AC ≠ 0: (E) → (AC)	HRRES	573	(E) <sub>16</sub> × 777777 → (E) <sub>L</sub> If AC ≠ 0: (E) → (AC)
HRL	504	(E) <sub>R</sub> → (AC) <sub>L</sub>	HRLZ	514	(E) <sub>R</sub> ,0 → (AC)
HRL1	505	E → (AC) <sub>L</sub>	HRLZI	515	E,0 → (AC)
HRLM	506	(AC) <sub>R</sub> → (E) <sub>L</sub>	HRLZM	516	(AC) <sub>R</sub> ,0 → (E)
HRLS	507	(E) <sub>R</sub> → (E) <sub>L</sub> If AC ≠ 0: (E) → (AC)	HRLZS	517	(E) <sub>R</sub> ,0 → (E) If AC ≠ 0: (E) → (AC)
HRLO	524	(E) <sub>R</sub> ,777777 → (AC)	HRLE	534	(E) <sub>R</sub> ,[(E) <sub>8</sub> × 777777] → (AC)
HRLOI	525	E,777777 → (AC)	HRLEI	535	E,[E] <sub>8</sub> × 777777 → (AC)
HRLOM	526	(AC) <sub>R</sub> ,777777 → (E)	HRLEM	536	(AC) <sub>R</sub> ,[(AC) <sub>8</sub> × 777777] → (E)
HRLOS	527	(E) <sub>R</sub> ,777777 → (E) If AC ≠ 0: (E) → (AC)	HRLES	537	(E) <sub>R</sub> ,[(E) <sub>8</sub> × 777777] → (E) If AC ≠ 0: (E) → (AC)
XHL1	501	E <sub>L</sub> → (AC) <sub>L</sub>			

Byte Manipulation

use present pointer | and | Load Byte into AC  
Increment pointer | and | DePosit Byte in memory  
Increment | Byte Pointer  
ADJust |

IBP 133 Linear operations on pointer in E or E.E+1  
AC = 0 If P - S ≥ 0: P - S → P  
If P - S < 0: Y + 1 → Y 36 - S → P

ADJBP 133 Array operations on pointer in E or E.E+1  
AC ≠ 0  
Let A = REMAINDER  $\frac{36 - P}{S}$   
If S > 36 - A: 1 → NO DIVIDE  
If S = 0: (E) → (AC) or (E.E+1) → (AC,AC+1)  
If 0 < S < 36 - A: make copy C of (E) or (E.E+1)

Compute (AC) +  $\left\lceil \frac{36 - P}{S} \right\rceil = Q \times \text{BYTES/WORD} + R$

$1 \leq R \leq \text{BYTES/WORD} = \left\lceil \frac{36 - P}{S} \right\rceil + \left\lceil \frac{P}{S} \right\rceil$

Y{C} + Q → Y{C}

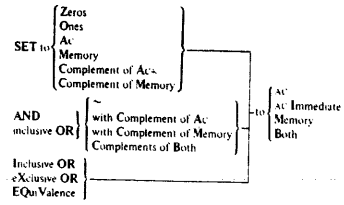
36 - R × S - A → P{C}

C → (AC) or (AC,AC+1)

LDB 135 BYTE IN ((E)) → (AC)  
DPB 137 BYTE IN (AC) → BYTE IN ((E))  
ILDDB 134 IBP and LDB  
IDPB 136 IBP and DPB

GEN. INFO.

Boolean



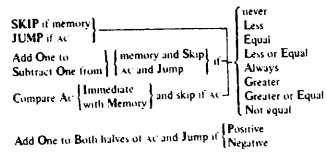
SETZ	400	0 → (AC)	SETO	474	7777777777777777 → (AC)
SETZI	401	0 → (AC)	SETOI	475	7777777777777777 → (AC)
SETZM	402	0 → (E)	SETOM	476	7777777777777777 → (E)
SETZB	403	0 → (AC) (E)	SETOB	477	7777777777777777 → (AC) (E)
SETA	424	(AC) → (AC) [no-op]	SETCA	450	~ (AC) → (AC)
SETAI	425	(AC) → (AC) [no-op]	SETCAI	451	~ (AC) → (AC)
SETAM	426	(AC) → (E)	SETCAM	452	~ (AC) → (E)
SETAB	427	(AC) → (E)	SETCAB	453	~ (AC) → (AC) (E)
SETM	414	(E) → (AC)	SETCM	460	~ (E) → (AC)
SETMI	415	0,E → (AC)	SETCMI	461	~ [0,E] → (AC)
SETMM	416	(E) → (E) [no-op]	SETCMM	462	~ (E) → (E)
SETMB	417	(E) → (AC) (E)	SETCMB	463	~ (E) → (AC) (E)
AND	404	(AC) ∧ (E) → (AC)	ANDCA	410	~ (AC) ∧ (E) → (AC)
ANDI	405	(AC) ∧ 0,E → (AC)	ANDCAI	411	~ (AC) ∧ 0,E → (AC)
ANDM	406	(AC) ∧ (E) → (E)	ANDCAM	412	~ (AC) ∧ (E) → (E)
ANDB	407	(AC) ∧ (E) → (AC) (E)	ANDCAB	413	~ (AC) ∧ (E) → (AC) (E)
ANDCM	420	(AC) ∧ ~ (E) → (AC)	ANDCB	440	~ (AC) ∧ ~ (E) → (AC)
ANDCMI	421	(AC) ∧ ~ [0,E] → (AC)	ANDCBI	441	~ (AC) ∧ ~ [0,E] → (AC)
ANDCMM	422	(AC) ∧ ~ (E) → (E)	ANDCBM	442	~ (AC) ∧ ~ (E) → (E)
ANDCMB	423	(AC) ∧ ~ (E) → (AC) (E)	ANDCBB	443	~ (AC) ∧ ~ (E) → (AC) (E)
IOR	434	(AC) ∨ (E) → (AC)	ORCA	454	~ (AC) ∨ (E) → (AC)
IORI	435	(AC) ∨ 0,E → (AC)	ORCAI	455	~ (AC) ∨ 0,E → (AC)
IORM	436	(AC) ∨ (E) → (E)	ORCAM	456	~ (AC) ∨ (E) → (E)
IORB	437	(AC) ∨ (E) → (AC) (E)	ORCAB	457	~ (AC) ∨ (E) → (AC) (E)
ORCM	464	(AC) ∨ ~ (E) → (AC)	ORCB	470	~ (AC) ∨ ~ (E) → (AC)
ORCMI	465	(AC) ∨ ~ [0,E] → (AC)	ORCBI	471	~ (AC) ∨ ~ [0,E] → (AC)
ORCMM	466	(AC) ∨ ~ (E) → (E)	ORCBM	472	~ (AC) ∨ ~ (E) → (E)
ORCMB	467	(AC) ∨ ~ (E) → (AC) (E)	ORCBB	473	~ (AC) ∨ ~ (E) → (AC) (E)
XOR	430	(AC) ⊕ (E) → (AC)	EQV	444	~ [(AC) ∨ (E)] → (AC)
XORI	431	(AC) ⊕ 0,E → (AC)	EQVI	445	~ [(AC) ∨ 0,E] → (AC)
XORM	432	(AC) ⊕ (E) → (E)	EQVM	446	~ [(AC) ∨ (E)] → (E)
XORB	433	(AC) ⊕ (E) → (AC) (E)	EQVB	447	~ [(AC) ∨ (E)] → (AC) (E)

Logical Testing and Modification

Test AC	$\left\{ \begin{array}{l} \text{with Direct mask} \\ \text{with Swapped mask} \\ \text{Right with } \bar{z} \\ \text{Left with } z \end{array} \right\}$	$\left\{ \begin{array}{l} \text{No modification} \\ \text{set masked bits to Zeros} \\ \text{set masked bits to Ones} \\ \text{Complement masked bits} \end{array} \right\}$	and skip	$\left\{ \begin{array}{l} \text{never} \\ \text{if all masked bits Equal 0} \\ \text{if Not all masked bits equal 0} \\ \text{Always} \end{array} \right\}$
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TLN	601	No-op	TRN	600	No-op
TLNE	603	If (AC) <sub>L</sub> ∧ E = 0: skip	TRNE	602	If (AC) <sub>R</sub> ∧ E = 0: skip
TLNA	605	Skip	TRNA	604	Skip
TLNN	607	If (AC) <sub>L</sub> ∧ E ≠ 0: skip	TRNN	606	If (AC) <sub>R</sub> ∧ E ≠ 0: skip
TLZ	621	(AC) <sub>L</sub> ∧ ~E → (AC) <sub>L</sub>	TRZ	620	(AC) <sub>R</sub> ∧ ~E → (AC) <sub>R</sub>
TLZE	623	If (AC) <sub>L</sub> ∧ E = 0: skip (AC) <sub>L</sub> ∧ ~E → (AC) <sub>L</sub>	TRZE	622	If (AC) <sub>R</sub> ∧ E = 0: skip (AC) <sub>R</sub> ∧ ~E → (AC) <sub>R</sub>
TLZA	625	(AC) <sub>L</sub> ∧ ~E → (AC) <sub>L</sub> skip	TRZA	624	(AC) <sub>R</sub> ∧ ~E → (AC) <sub>R</sub> skip
TLZN	627	If (AC) <sub>L</sub> ∧ E ≠ 0: skip (AC) <sub>L</sub> ∧ ~E → (AC) <sub>L</sub>	TRZN	626	If (AC) <sub>R</sub> ∧ E ≠ 0: skip (AC) <sub>R</sub> ∧ ~E → (AC) <sub>R</sub>
TLC	641	(AC) <sub>L</sub> ∨ E → (AC) <sub>L</sub>	TRC	640	(AC) <sub>R</sub> ∨ E → (AC) <sub>R</sub>
TLCE	643	If (AC) <sub>L</sub> ∧ E = 0: skip (AC) <sub>L</sub> ∨ E → (AC) <sub>L</sub>	TRCE	642	If (AC) <sub>R</sub> ∧ E = 0: skip (AC) <sub>R</sub> ∨ E → (AC) <sub>R</sub>
TLCA	645	(AC) <sub>L</sub> ∨ E → (AC) <sub>L</sub> skip	TRCA	644	(AC) <sub>R</sub> ∨ E → (AC) <sub>R</sub> skip
TLCN	647	If (AC) <sub>L</sub> ∧ E ≠ 0: skip (AC) <sub>L</sub> ∨ E → (AC) <sub>L</sub>	TRCN	646	If (AC) <sub>R</sub> ∧ E ≠ 0: skip (AC) <sub>R</sub> ∨ E → (AC) <sub>R</sub>
TLO	661	(AC) <sub>L</sub> ∨ E → (AC) <sub>L</sub>	TRO	660	(AC) <sub>R</sub> ∨ E → (AC) <sub>R</sub>
TLOE	663	If (AC) <sub>L</sub> ∧ E = 0: skip (AC) <sub>L</sub> ∨ E → (AC) <sub>L</sub>	TROE	662	If (AC) <sub>R</sub> ∧ E = 0: skip (AC) <sub>R</sub> ∨ E → (AC) <sub>R</sub>
TLOA	665	(AC) <sub>L</sub> ∨ E → (AC) <sub>L</sub> skip	TROA	664	(AC) <sub>R</sub> ∨ E → (AC) <sub>R</sub> skip
TLON	667	If (AC) <sub>L</sub> ∧ E ≠ 0: skip (AC) <sub>L</sub> ∨ E → (AC) <sub>L</sub>	TRON	666	If (AC) <sub>R</sub> ∧ E ≠ 0: skip (AC) <sub>R</sub> ∨ E → (AC) <sub>R</sub>
TDN	610	No-op	TSN	611	No-op
TDNE	612	If (AC) ∧ (E) = 0: skip	TSNE	613	If (AC) ∧ (E) <sub>S</sub> = 0: skip
TDNA	614	Skip	TSNA	615	Skip
TDNN	616	If (AC) ∧ (E) ≠ 0: skip	TSNN	617	If (AC) ∧ (E) <sub>S</sub> ≠ 0: skip
TDZ	630	(AC) ∧ ~E → (AC)	TSZ	631	(AC) ∧ ~E) <sub>S</sub> → (AC)
TDZE	632	If (AC) ∧ E = 0: skip (AC) ∧ ~E → (AC)	TSZE	633	If (AC) ∧ E) <sub>S</sub> = 0: skip (AC) ∧ ~E) <sub>S</sub> → (AC)
TDZA	634	(AC) ∧ ~E → (AC) skip	TSZA	635	(AC) ∧ ~E) <sub>S</sub> → (AC) skip
TDZN	636	If (AC) ∧ E ≠ 0: skip (AC) ∧ ~E → (AC)	TSZN	637	If (AC) ∧ E) <sub>S</sub> ≠ 0: skip (AC) ∧ ~E) <sub>S</sub> → (AC)
TDC	650	(AC) ∨ E → (AC)	TSC	651	(AC) ∨ E) <sub>S</sub> → (AC)
TDCE	652	If (AC) ∧ E = 0: skip (AC) ∨ E → (AC)	TSCE	653	If (AC) ∧ E) <sub>S</sub> = 0: skip (AC) ∨ E) <sub>S</sub> → (AC)
TDCA	654	(AC) ∨ E → (AC) skip	TSCA	655	(AC) ∨ E) <sub>S</sub> → (AC) skip
TD CN	656	If (AC) ∧ E ≠ 0: skip (AC) ∨ E → (AC)	TS CN	657	If (AC) ∧ E) <sub>S</sub> ≠ 0: skip (AC) ∨ E) <sub>S</sub> → (AC)
TDO	670	(AC) ∨ E → (AC)	TSO	671	(AC) ∨ E) <sub>S</sub> → (AC)
TDOE	672	If (AC) ∧ E = 0: skip (AC) ∨ E → (AC)	TSOE	673	If (AC) ∧ E) <sub>S</sub> = 0: skip (AC) ∨ E) <sub>S</sub> → (AC)
TDOA	674	(AC) ∨ E → (AC) skip	TSOA	675	(AC) ∨ E) <sub>S</sub> → (AC) skip
TDON	676	If (AC) ∧ E ≠ 0: skip (AC) ∨ E → (AC)	TS ON	677	If (AC) ∧ E) <sub>S</sub> ≠ 0: skip (AC) ∨ E) <sub>S</sub> → (AC)

Arithmetic Testing

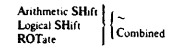


AOBJP	252	(AC) + 1, 1 → (AC)	If (AC) ≥ 0: E → (PC)				
AOBJN	253	(AC) + 1, 1 → (AC)	If (AC) < 0: E → (PC)				
CAI	300	No-op		CAM	310	No-op	
CAIL	301	If (AC) < E: skip		CAML	311	If (AC) < (E): skip	
CAIE	302	If (AC) = E: skip		CAME	312	If (AC) = (E): skip	
CAILE	303	If (AC) ≤ E: skip		CAMLE	313	If (AC) ≤ (E): skip	
CAIA	304	Skip		CAMA	314	Skip	
CAIGE	305	If (AC) ≥ E: skip		CAMGE	315	If (AC) ≥ (E): skip	
CAIN	306	If (AC) ≠ E: skip		CAMN	316	If (AC) ≠ (E): skip	
CAIG	307	If (AC) > E: skip		CAMG	317	If (AC) > (E): skip	
JUMP	320	No-op		SKIP	330	If AC ≠ 0: (E) → (AC)	
JUMPL	321	If (AC) < 0: E → (PC)		SKIPL	331	If AC ≠ 0: (E) → (AC) If (E) < 0: skip	
JUMPE	322	If (AC) = 0: E → (PC)		SKIPE	332	If AC ≠ 0: (E) → (AC) If (E) = 0: skip	
JUMPLE	323	If (AC) ≤ 0: E → (PC)		SKIPLE	333	If AC ≠ 0: (E) → (AC) If (E) ≤ 0: skip	
JUMPA	324	E → (PC)		SKIPA	334	If AC ≠ 0: (E) → (AC) Skip	
JUMPE	325	If (AC) ≥ 0: E → (PC)		SKIPGE	335	If AC ≠ 0: (E) → (AC) If (E) ≥ 0: skip	
JUMPN	326	If (AC) ≠ 0: E → (PC)		SKIPN	336	If AC ≠ 0: (E) → (AC) If (E) ≠ 0: skip	
JUMPG	327	If (AC) > 0: E → (PC)		SKIPG	337	If AC ≠ 0: (E) → (AC) If (E) > 0: skip	
AOJ	340	(AC) + 1 → (AC)		SOJ	360	(AC) - 1 → (AC)	
AOJL	341	(AC) + 1 → (AC) If (AC) < 0: E → (PC)		SOJL	361	(AC) - 1 → (AC) If (AC) < 0: E → (PC)	
AOJE	342	(AC) + 1 → (AC) If (AC) = 0: E → (PC)		SOJE	362	(AC) - 1 → (AC) If (AC) = 0: E → (PC)	
AOJLE	343	(AC) + 1 → (AC) If (AC) ≤ 0: E → (PC)		SOJLE	363	(AC) - 1 → (AC) If (AC) ≤ 0: E → (PC)	
AOJA	344	(AC) + 1 → (AC) E → (PC)		SOJA	364	(AC) - 1 → (AC) E → (PC)	
AOJGE	345	(AC) + 1 → (AC) If (AC) ≥ 0: E → (PC)		SOJGE	365	(AC) - 1 → (AC) If (AC) ≥ 0: E → (PC)	
AOJN	346	(AC) + 1 → (AC) If (AC) ≠ 0: E → (PC)		SOJN	366	(AC) - 1 → (AC) If (AC) ≠ 0: E → (PC)	
AOJG	347	(AC) + 1 → (AC) If (AC) > 0: E → (PC)		SOJG	367	(AC) - 1 → (AC) If (AC) > 0: E → (PC)	
AOS	350	(E) + 1 → (E) If (AC) ≠ 0: (E) → (AC)		SOS	370	(E) - 1 → (E) If AC ≠ 0: (E) → (AC)	
AOSL	351	(E) + 1 → (E) If AC ≠ 0: (E) → (AC) If (E) < 0: skip		SOSL	371	(E) - 1 → (E) If AC ≠ 0: (E) → (AC) If (E) < 0: skip	
AOSE	352	(E) + 1 → (E) If AC ≠ 0: (E) → (AC) If (E) = 0: skip		SOSE	372	(E) - 1 → (E) If AC ≠ 0: (E) → (AC) If (E) = 0: skip	
AOSLE	353	(E) + 1 → (E) If AC ≠ 0: (E) → (AC) If (E) ≤ 0: skip		SOSLE	373	(E) - 1 → (E) If AC ≠ 0: (E) → (AC) If (E) ≤ 0: skip	



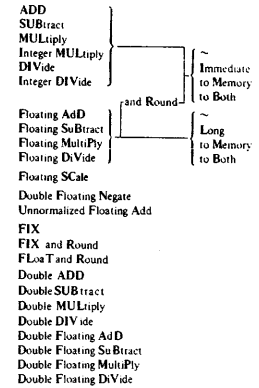
AOSA	354	(E) + 1 → (E) If AC ≠ 0: (E) → (AC) Skip	SOSA	374	(E) - 1 → (E) If AC ≠ 0: (E) → (AC) Skip
AOSGE	355	(E) + 1 → (E) If AC ≠ 0: (E) → (AC) If (E) ≥ 0: skip	SOSGE	375	(E) - 1 → (E) If AC ≠ 0: (E) → (AC) If (E) ≥ 0: skip
AOSN	356	(E) + 1 → (E) If AC ≠ 0: (E) → (AC) If (E) ≠ 0: skip	SOSN	376	(E) - 1 → (E) If AC ≠ 0: (E) → (AC) If (E) ≠ 0: skip
AOSG	357	(E) + 1 → (E) If AC ≠ 0: (E) → (AC) If (E) > 0: skip	SOSG	377	(E) - 1 → (E) If AC ≠ 0: (E) → (AC) If (E) > 0: skip

Shift and Rotate



ASH	240	(AC) × 2 <sup>E</sup> → (AC)	ASHC	244	(AC, AC+1) × 2 <sup>E</sup> → (AC, AC+1)
ROT	241	Rotate (AC) E places	ROTC	245	Rotate (AC, AC+1) E places
LSH	242	Shift (AC) E places	LSHC	246	Shift (AC, AC+1) E places

FIXED AND FLOATING POINT ARITHMETIC



Fixed Point Arithmetic

ADD	270	(AC) + (E) → (AC)	SUB	274	(AC) - (E) → (AC)
ADDI	271	(AC) + 0, E → (AC)	SUBI	275	(AC) - 0, E → (AC)
ADDM	272	(AC) + (E) → (E)	SUBM	276	(AC) - (E) → (E)
ADDB	273	(AC) + (E) → (AC) (E)	SUBB	277	(AC) - (E) → (AC) (E)
IMUL	220	(AC) × (E) → (AC)*	MUL	224	(AC) × (E) → (AC, AC+1)
IMULI	221	(AC) × 0, E → (AC)*	MULI	225	(AC) × 0, E → (AC, AC+1)
IMULM	222	(AC) × (E) → (E)*	MULM	226	(AC) × (E) → (E)*
IMULB	223	(AC) × (E) → (AC) (E)*	MULB	227	(AC) × (E) → (AC, AC+1) (E)
IDIV	230	(AC) ÷ (E) → (AC) REMAINDER → (AC+1)	DIV	234	(AC, AC+1) ÷ (E) → (AC) REMAINDER → (AC+1)
IDIVI	231	(AC) ÷ 0, E → (AC) REMAINDER → (AC+1)	DIVI	235	(AC, AC+1) ÷ 0, E → (AC) REMAINDER → (AC+1)
IDIVM	232	(AC) ÷ (E) → (E)	DIVM	236	(AC, AC+1) ÷ (E) → (E)
IDIVB	233	(AC) ÷ (E) → (AC) (E) REMAINDER → (AC+1)	DIVB	237	(AC, AC+1) ÷ (E) → (AC) (E) REMAINDER → (AC+1)

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DADD	114	(AC,AC+1) + (E,E+1) → (AC,AC+1)
DSUB	115	(AC,AC+1) - (E,E+1) → (AC,AC+1)
DMUL	116	(AC,AC+1) × (E,E+1) → (AC-AC+3)
DDIV	117	(AC-AC+3) ÷ (E,E+1) → (AC,AC+1)
		REMAINDER → (AC+2,AC+3)

\*The high order word of the product is discarded.  
 †The low order word of the product is discarded.

Floating Point Arithmetic

FAD	140	(AC) + (E) → (AC)	FADR	144	(AC) + (E) → (AC)
FADL	141	(AC) + (E) → (AC,AC+1)	FADRI	145	(AC) + E,0 → (AC)
FADM	142	(AC) + (E) → (E)	FADRM	146	(AC) + (E) → (E)
FADB	143	(AC) + (E) → (AC)(E)	FADRB	147	(AC) + (E) → (AC)(E)
FSB	150	(AC) - (E) → (AC)	FSBR	154	(AC) - (E) → (AC)
FSBL	151	(AC) - (E) → (AC,AC+1)	FSBRI	155	(AC) - E,0 → (AC)
FSBM	152	(AC) - (E) → (E)	FSBRM	156	(AC) - (E) → (E)
FSBB	153	(AC) - (E) → (AC)(E)	FSBRB	157	(AC) - (E) → (AC)(E)
FMP	160	(AC) × (E) → (AC)	FMPR	164	(AC) × (E) → (AC)
FMPL	161	(AC) × (E) → (AC,AC+1)	FMPRI	165	(AC) × E,0 → (AC)
FMPM	162	(AC) × (E) → (E)	FMPRM	166	(AC) × (E) → (E)
FMPB	163	(AC) × (E) → (AC)(E)	FMPRB	167	(AC) × (E) → (AC)(E)
FDV	170	(AC) ÷ (E) → (AC)	FDVR	174	(AC) ÷ (E) → (AC)
FDVL	171	(AC) ÷ (E) → (AC)	FDVRI	175	(AC) ÷ E,0 → (AC)
		REMAINDER → (AC+1)			
FDVM	172	(AC) ÷ (E) → (E)	FDVRM	176	(AC) ÷ (E) → (E)
FDVB	173	(AC) ÷ (E) → (AC)(E)	FDVRB	177	(AC) ÷ (E) → (AC)(E)
UFA	130	(AC) + (E) → (AC+1) without normalization			
DFN	131	- (AC,E) → (AC,E)			
FSC	132	(AC) × 2 <sup>E</sup> → (AC)			
FLTR	127	(E) float, rounded → (AC)			
FIX	122	(E) fixed → (AC)	FIXR	126	(E) fixed, rounded → (AC)
DFAD	110	(AC,AC+1) + (E,E+1) → (AC,AC+1)			
DFSB	111	(AC,AC+1) - (E,E+1) → (AC,AC+1)			
DFMP	112	(AC,AC+1) × (E,E+1) → (AC,AC+1)			
DFDV	113	(AC,AC+1) ÷ (E,E+1) → (AC,AC+1)			

STACK

PUSH } | ~  
 POP } | and Jump  
 ADJUST Stack Pointer

PUSH	261	If PC <sub>L</sub> = 0 or (AC) <sub>0,6,17</sub> < 0: (AC) + 1,1 → (AC) (E) → ((AC) <sub>R</sub> ) If PC <sub>L</sub> ≠ 0 and (AC) <sub>0,6,17</sub> < 0: (AC) + 1 → (AC) (E) → ((AC))
POP	262	If PC <sub>L</sub> = 0 or (AC) <sub>0,6,17</sub> < 0: ((AC) <sub>R</sub> ) → (E) (AC) - 1,1 → (AC) If PC <sub>L</sub> ≠ 0 and (AC) <sub>0,6,17</sub> > 0: ((AC)) → (E) (AC) - 1 → (AC)
PUSHJ	260	If PC <sub>L</sub> = 0: (AC) + 1,1 → (AC) FLAGS, PC+1 → ((AC) <sub>R</sub> ) If PC <sub>L</sub> ≠ 0 and (AC) <sub>0,6,17</sub> < 0: (AC) + 1,1 → (AC) PC+1 → ((AC) <sub>R</sub> ) If PC <sub>L</sub> ≠ 0 and (AC) <sub>0,6,17</sub> > 0: (AC) + 1 → (AC) PC+1 → ((AC)) E → (PC)
POPJ	263	If PC <sub>L</sub> = 0: ((AC) <sub>R</sub> ) <sub>R</sub> → (PC) (AC) - 1,1 → (AC) If PC <sub>L</sub> ≠ 0 and (AC) <sub>0,6,17</sub> < 0: ((AC) <sub>R</sub> ) → (PC) (AC) - 1,1 → (AC) If PC <sub>L</sub> ≠ 0 and (AC) <sub>0,6,17</sub> > 0: ((AC)) → (PC) (AC) - 1 → (AC)
ADJSP	105	If PC <sub>L</sub> = 0 or (AC) <sub>0,6,17</sub> < 0: (AC) + [±] E <sub>R</sub> , E <sub>R</sub> → (AC) If PC <sub>L</sub> ≠ 0 and (AC) <sub>0,6,17</sub> > 0: (AC) + [±] E <sub>R</sub> → (AC)

Program Control

(to SubRoutine  
 and Save Pc  
 and Save Ac  
 and Restore Ac  
 if Find First One  
 on Flag and CLear it  
 on Overflow (JFCL 10.)  
 on C<sub>0</sub>R<sub>0</sub>Y 0 (JFCL 4.)  
 on C<sub>0</sub>R<sub>0</sub>Y 1 (JFCL 2.)  
 on C<sub>0</sub>R<sub>0</sub>Y (JFCL 6.)  
 on Floating Overflow (JFCL 1.)  
 and ReSTore  
 and ReSTore Flags (JRST 2.)  
 and ENable  $\pi$  level (JRST 12.)  
 HALT (JRST 4.)  
 PORTAL (JRST 1.)  
 eXtended Jump and ReSTore Flags (JRST 5.)  
 eXtended Jump and ENable  $\pi$  level (JRST 6.)  
 eXtended PC Word (JRST 7.)  
 Save Flags in Memory (JRST 14.)  
 eX-CuTe  
 MAP

XCT	256	Execute (E)		
JFFO	243	If (AC) = 0: 0 → (AC + 1)		
		If (AC) ≠ 0: E → (PC) (see page 2-63)		
JFCL	255	If AC ∧ FLAGS ≠ 0: E → (PC)	~ AC ∧ FLAGS → FLAGS	
JRST	25400	E → (PC)		
PORTAL	25404	0 → PUBLIC E → (PC)		
JRSTF	25410	(X) <sub>L</sub> or (Y) <sub>L</sub> → FLAGS E → (PC)		
HALT	25420	E → (PC) stop		
XJRSTF	25424	(E) <sub>L</sub> → FLAGS (E+1) → (PC)		
XJEN	25430	Dismiss $\pi$ (E) <sub>L</sub> → FLAGS (E+1) → (PC)		
XPCW	25434	FLAGS, 0 → (E) PC+1 → (E+1) (E+2) <sub>L</sub> → FLAGS (E+3) → (PC)		
JEN	25450	Dismiss $\pi$ (X) <sub>L</sub> or (Y) <sub>L</sub> → FLAGS E → (PC)		
SFM	25460	FLAGS, 0 → (E)		
JSR	264	If PC <sub>L</sub> = 0: FLAGS, PC <sub>R</sub> + 1 → (E) E+1 → (PC)		
		If PC <sub>L</sub> ≠ 0: PC+1 → (E) E+1 → (PC)		
JSP	265	If PC <sub>L</sub> = 0: FLAGS, PC <sub>R</sub> + 1 → (AC) E → (PC)		
		If PC <sub>L</sub> ≠ 0: PC+1 → (AC) E → (PC)		
JSA	266	(AC) → (E) E <sub>R</sub> , PC <sub>R</sub> + 1 → (AC) E+1 → (PC)		
JRA	267	((AC) <sub>L</sub> ) → (AC) E → (PC)		
MAP	257	PHYSICAL MAP DATA → (AC)		

Extended Instructions

MOVe String	Left Justified Right Justified Offset Translated
CoMPare Strings and skip if	Less Equal Less or Equal Greater Greater or Equal Not equal
ConVert	Decimal to Binary   Offset Binary to Decimal   Translated
EDIT string	
CMPSL 001	CVTDBO 010
CMPSL 002	CVTDBT 011
CMPSLE 003	CVTDBO 012
EDIT 004	CVTDBT 013
CMPSGE 005	MOVSO 014
CMPSN 006	MOVST 015
CMPSG 007	MOVSLJ 016
	MOVSRJ 017

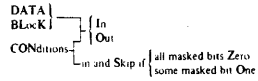
NOTE  
Refer to the DECSYSTEM-10/DECSYSTEM-20  
Hardware Reference Manual, Volume 1, for a  
description of the Extended Instructions.

Cache CCA 014

All sweeps initially set Sweep Busy, and at termination they clear Sweep Busy and set Sweep Done.

SWPIA	70144	Invalidate all pages	SWPIO	70164	Invalidate page E
SWPVA	70150	Validate all pages	SWPVO	70170	Validate page E
SWPUA	70154	Unload all pages	SWPUO	70174	Unload page E

In-out



CONO	70020	E → COMMAND	CONSZ	70030	If STATUS <sub>R</sub> ∧ E = 0: skip
CONI	70024	STATUS → (E)	CONSO	70034	If STATUS <sub>R</sub> ∧ E ≠ 0: skip
DATAO	70014	(E) → DATA	DATAL	70004	DATA → (E)
BLKO	70010	(E) + 1,1 → (E) ((E) <sub>R</sub> ) → DATA If (E) <sub>L</sub> ≠ 0: skip			
BLKI	70000	(E) + 1,1 → (E) DATA → ((E) <sub>R</sub> ) If (E) <sub>L</sub> ≠ 0: skip			

ALGEBRAIC REPRESENTATION

- AC The accumulator address in bits 9-12 of the instruction word
- AC+N The address N greater than AC, except that accumulator addresses wrap around from 17, e.g., AC+3 is 1 if AC is 16.
- E The result of the effective address calculation. When E is an address it has the number of bits appropriate to such use – depending on the type of processor, whether local or global, etc. E is eighteen bits unsigned when used as a half word operand, mask or output conditions; nine bits signed when used as a scale factor or shift number; and eighteen bits signed when used as an offset. For any signed quantity, the sign is always bit 18.
- E<sub>R</sub> The in-section part of E (the right eighteen bits).
- E<sub>L</sub> The section-number part of E (those bits, if any, at the left of bit 18).
- E+N The address N greater than E, with a wraparound, where appropriate, from an in-section value of 777777 without changing the section number.
- PC The 30-bit or 18-bit program counter; the symbol also represents the contents of PC when used as the source of an address.
- PC+1 The address produced by adding 1 to the in-section part of PC with a wraparound from 777777 (the section number does not change).
- (X) The word contained in register X.
- (X)<sub>L</sub> The left half of (X).
- (X)<sub>R</sub> The right half of (X).
- (X)<sub>S</sub> The word contained in X with its left and right halves swapped.
- A<sub>n</sub> The value of bit n of the quantity A.
- A.B A 36-bit word with the 18-bit quantity A in its left half and the 18-bit quantity B in its right half (either A or B may be 0).
- (X.Y) The contents of registers X and Y concatenated into a double word operand.
- (X-Y) The contents of registers X to Y concatenated into a multiword operand.
- ((X)) The word contained in the register addressed by (X), i.e., addressed by the word in register X.

$A \rightarrow B$  The quantity  $A$  replaces the quantity  $B$  ( $A$  and  $B$  may be half words, full words or double words). For example,

$$(AC) + (E) \rightarrow (AC)$$

means the word in accumulator AC plus the word in memory location E replaces the word in AC.

$(AC) (E)$  The word in AC and the word in E.

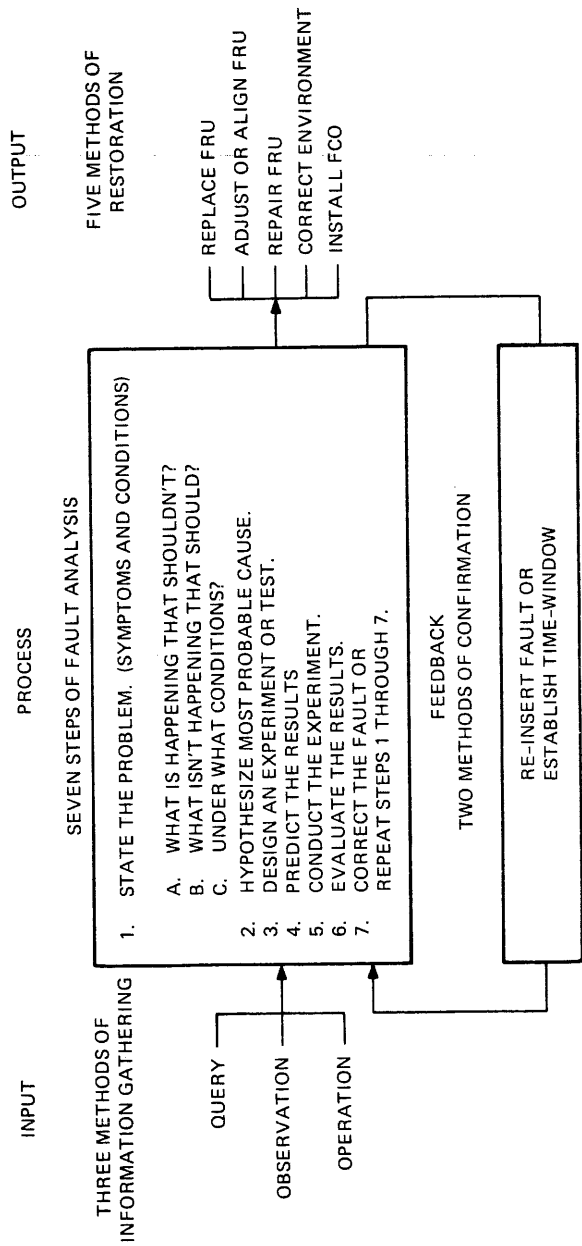
$\wedge \vee \neg \sim$  The Boolean operators AND, inclusive OR, exclusive OR, and complement (logical negation).

$+ - \times \div \parallel$  The arithmetic operators for addition, negation or subtraction, multiplication, division, and absolute value (magnitude).

Square brackets are used occasionally for grouping, but when they enclose an arithmetic computation they represent the "largest integer contained in" the enclosed quantity. With respect to the values of their terms, the equations for a given instruction are in chronological order; e.g., in the pair of equations

$$\begin{aligned} & (AC) + 1 \rightarrow (AC) \\ & \text{If } (AC) = 0: E \rightarrow (PC) \end{aligned}$$

the quantity tested in the second equation is the word in AC after it has been incremented by one.



MR-2502

EK-OKL10-02  
SEPT 1979

GEN. INFO.

-33B-

NOTES

COMPANY CONFIDENTIAL

GATHERING KL10 SYSTEM ERROR INFORMATION

Prior to gathering KL10 system error information, the auto-reload feature must be disabled.

Procedure 1 lists the steps necessary to disable auto-reload for TOPS-20 and TOPS-10 (release 603 or later).

Procedure 2 lists additional steps necessary to disable auto-reload for all TOPS-10 operating systems.

Procedure 3 lists the steps necessary to gather essential KL10 system error information.

Procedure 1 Disabling Auto-Reload (TOPS-20 and TOPS-10/603 and Later)

Step	Command Response	Comments
1	↑\	Enter PARSEr command mode
2	PAR>SET CONSOLE PROGRAMER<CR>	Request PROGRAMMER mode privileges
	CONSOLE MODE: PROGRAMMER	PARSER response
3	PAR>SET NO RELOAD<CR>	Disable auto-reload
	RELOAD ENABLE: OFF	PARSER response
4	PAR>QUIT<CR>	Exit PARSEr. Return to command mode.

Procedure 2 Disabling Auto-Reload (TOPS-10 Only)

Step	Command Response	Comments
1	↑C	Control C - Enter TOPS-20 command mode.
2	.R WHEEL<CR> Setting Wheel Capability if the CTY is used.	Request 1,2 privileges. This step is not necessary
3	.R FILDDT<CR>	Run FILDDT
4	FILE: SYSTEM/S<CR>	Load the operating system's symbol table.
5	FILE:/M/P<CR>	Enable, examining and patching the operating system.
6	*\$H<CR>	Set DDT printout mode to half-word.
7	*DEBUGF/YXXXXX,,XXXXXX	Bit 03 of this word must be set to disable auto-reload. That is, the second octal digit (Y) must be either a 4, 5, 6, or 7. If it is, type a carriage return. If it is not, retype the line changing the second octal digit.  From To 0 4 1 5 2 6 3 7  For example, 127413,,371520 would become: 167413,,371520<CR>
8	↑Z	Control-Z Exit FILDDT and return to TOPS-10 command mode.



Procedure 3 Gathering System Error Status

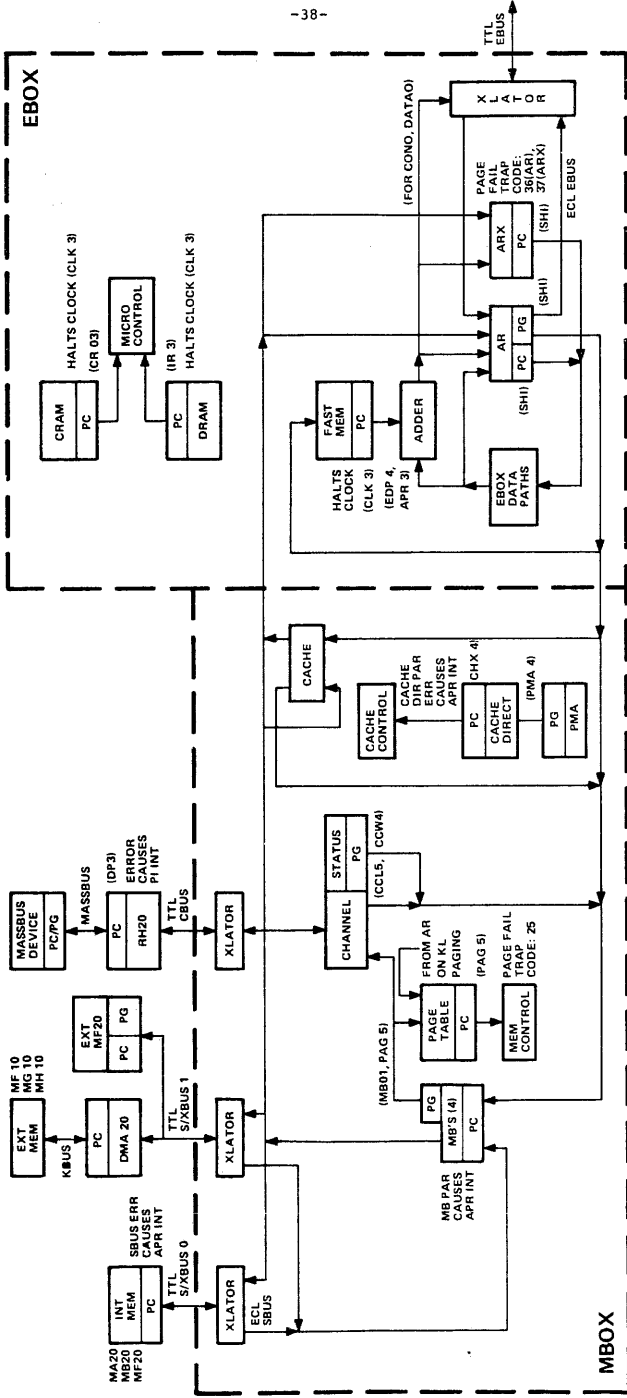
Step	PARSER Command	Comments
1	↑\	Enter PARSER.
2	SET CON MAINT<CR>	Request Maintenance Mode privileges.
3	EXAMINE DTE-20<CR>	Get current DTE20 status.
4	MCR BOO<CR>	Load BOO.TSK file.
5	DBOOT<CR>	Direct BOO to load and start KLDCP.
Step	KLDCP Command	Comments
6	EE 174434<CR>	Examine DTE STATUS register.
7	EE 174430<CR>	Examine DTE DIAG 1 register.
8	DE 174432:100<CR>	Reset the DTE.
9	FX 0<CR>	Turn off the clock.
10	ALL<CR>	Print all CRAM and registers
11	PR 110<CR>	Read APR.
12	PR 100,177<CR>	Read all diagnostic functions.
13	EC 0<CR>	Set the microcode address to 0 and reset the KL10.
14	FX 1<CR>	Turn on the clock.
15	FX 0<CR>	Turn off the clock.
16	FX 1,FX 10,PC<CR>	Start the clock, stop the clock, get the PC.
17	FX 12,PC,FX 12,PC<CR>	Continue (momentarily) and get PC, continue (momentarily) and get the PC again.
18	EC<CR>	Examine the current CRAM location. Determine if the location is the halt loop location for the version of microcode in use by the system. If it is, proceed to step 19. If it is not, stop. The KL10 is hung in an unknown state and the remainder of the procedure cannot be executed.
19	FX 1<CR>	Turn on the clock.
20	EM 16,17<CR>	Examine ACs 16 and 17. If the examine works, proceed to step 21. If the examine fails, stop. The KL10 is hung in an unknown state and the remainder of the procedure cannot be executed.
21	EX 700000 17,EM 17<CR>	BLKI APR(APRID) and print.
22	EX 700240 17,EM 17<CR>	CONI APR and print.
23	EX 701240 17,EM 17<CR>	CONI PAG and print.
24	EX 701040 17,EM 17<CR>	DATAI PAG and print.
25	EX 700400 17,EM 17<CR>	BLKI PI (RDERA) and print.
26	EX 720240 17,EM 17<CR>	CONI DTE (STATUS) and print.
27	EM xxxxx500,xxxxx502<CR>	Examine PAGE FAIL location. Where xxxxx equals bits <23:35> of the DATAI PAG (UBR) refer to step 16.  xxxxx500 = PAGE FAIL WORD xxxxx501 = PAGE FAIL PC and FLAGS xxxxx502 = PAGE FAIL PC

Procedure 3 Gathering System Error Status (Cont)

Step	KLDCP Command (Cont)	Comments (Cont)
28	AC BLK 7<CR>	Select microcode AC block 7.
29	EM 0,2<CR>	Examine the AC block.  AC0 = AR data for PAGE FAIL AC1 = ARX data for PAGE FAIL AC2 = I/O PAGE FAIL word
30	AC BLK 0<CR>	Select AC block 0.
<b>INTERNAL MEMORY STATUS</b>		
31	DM 16:0<CR>	Set up for BLKO PI (SBDIAG 0, controller 0)
32	EX 700500 16,EM 17<CR>	Execute SBDIAG0 and print E+1.
33	DM 16:1<CR>	Set up for BLKO PI (SBDIAG1, controller 0)
34	EX 700500 16,EM 17<CR>	Execute SBDIAG1 and print E+1.
35		Repeat steps 24 through 27 for each controller on the system by incrementing bits <00:04> of the BLKO PI word deposited in AC 16.
<b>EXTERNAL MEMORY (DMA) STATUS</b>		
36	DM 16:100000 0<CR>	Set up BLKO PI (SBDIAG 0, controller 4).
37	EX 700500 16,EM 17<CR>	Execute SBDIAG 0 and print E+1.
<b>MASSBUS CONTROLLER (RH20) STATUS</b>		
38	EX 754240 17,EM 17<CR>	CONI RH and print
39		Repeat step 31 for each RH20 on the system by changing the I/O device select code.  RH20    CONI 1        754640 2        755240 3        755640 4        756240 5        756640 6        757240 7        757640
<b>INTERNAL CHANNEL STATUS IF EBR IS EQUAL TO 0 (Step 15 bits &lt;23:35&gt;</b>		
40	DM 600:540001 540000<CR>	Set up page table
41	EX 701200 20000<CR>	Turn paging on
42	EX 200740 1000,EM 17<CR>	Move CHAN 0 (INIT CMD) to AC17 and print.
43	EX 200740 1001,EM 17<CR>	Move CHAN 0 (ERROR STATUS) to AC17 and print.
44	EX 200740 1002,EM 17<CR>	Move CHAN 0 (STATUS) to AC17 and print.
45		Repeat steps 35 through 37 for each channel on the system.  CHAN 1 (1004-1006) CHAN 2 (1010-1012) CHAN 3 (1014-1016) CHAN 4 (1020-1022) CHAN 5 (1024-1026) CHAN 6 (1030-1032) CHAN 7 (1034-1036)

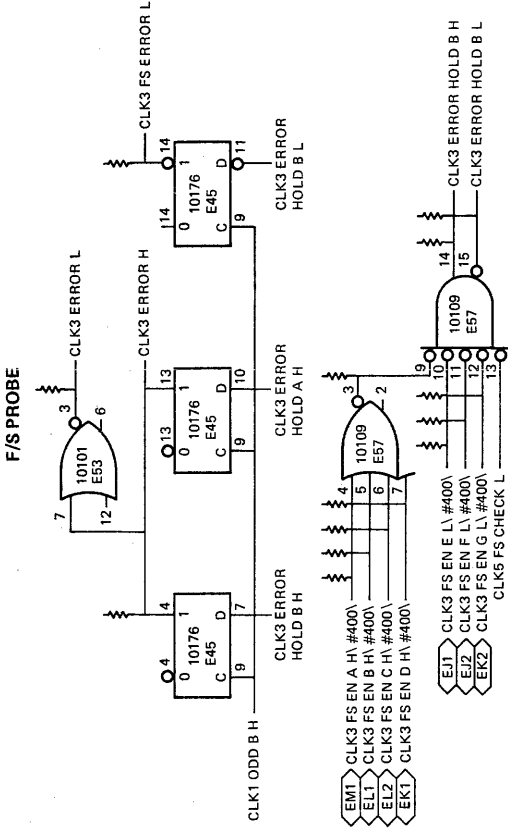
Procedure 3 Gathering System Error Status (Cont)

Step	KLDCP Command (Cont)	Comments (Cont)
INTERNAL CHANNEL STATUS IF EBR IS GREATER THAN 0 (step 15 bits <23:35>)		
46	EM xxxxx000,xxxxx037	Examine channel locations. Where xxxxx equals bits <23:35> of the CONI PAG (EBR) refer to step 15.  xxxxx000 = CHAN 0 INIT CMD xxxxx001 = CHAN 0 ERROR STATUS xxxxx002 = CHAN 0 STATUS  xxxxx004 through xxxxx006 CHAN 1 xxxxx010 through xxxxx012 CHAN 2 xxxxx014 through xxxxx016 CHAN 3 xxxxx020 through xxxxx022 CHAN 4 xxxxx024 through xxxxx026 CHAN 5 xxxxx030 through xxxxx032 CHAN 6 xxxxx034 through xxxxx036 CHAN 7
RH20 DEVICE STATUS		
47	DM 16:000400 0<CR>	Set up DATAO RH to select reg 0 (DRCR).
48	EX 754140 16<CR>	DATAO RH select reg 0.
49	EX 754040 17,EM 17<CR>	DATAI RH print reg 0.
50	DM 16:010400 0<CR>	Set up DATAO RH to select reg 1 (DRSR).
51	EX 754140 16<CR>	DATAO RH select reg 1.
52	EX 754040 17,EM 17<CR>	DATAI RH print reg 1.
53	DM 16:020400 0<CR>	Set up DATAO RH to select reg 2 (DRER1).
54	EX 754140 16<CR>	DATAO RH select reg 2.
55	EX 754040 17,EM 17<CR>	DATAI RH print reg 2.
56	DM 16:140400 0<CR>	Set up DATAO RH to select reg 14 (DRER2).
57	EX 754140 16<CR>	DATAO RH select reg 14.
58	EX 754040 17,EM 17<CR>	DATAI RH print reg 14.
59	DM 16:150400 0<CR>	Set up DATAO RH to select reg 15 (DRER3).
60	EX 754140 16<CR>	DATAO RH select reg 15.
61	EX 754040 17,EM 17<CR>	DATAI RH print reg 15.
62		Repeat steps 40 through 54 for each device on the controller by incrementing bits <15:17> of the DATAO RH word deposited in AC 16. Repeat steps 40 through 55 for each controller on the system by changing the I/O device select code.  RH20    DATAO    DATAI 1        754540    754440 2        755140    755040 3        755540    755440 4        756140    756040 5        756540    756440 6        757140    757040 7        757540    757440



MR-241B

NOTES: PG-PARITY GENERATOR PC-PARITY CHECKER



MR2301

KL10 PAGE FAIL TRAPS (INT. MEM.)

CACHE	DATA SOURCE	WRITE REF	OPERATION	COMMENTS	SBSUS ERR	MB PAR ERR	WHERE DETECTED				PF CODE 25	PF CODE 36 OR 37	FAILING DATA PATH OR COMPONENT
							MEMORY	MB	AR/ARX	PT			
1	1	0	PAGE REFILL	MEMORY READ OR RPW	1	1	X	X	X	X	X	X	MEMORY
0	0	0	READ		0	0	X	X	X	X	X	X	MEMORY TO MB
1	1	0			1	1	X	X	X	X	X	X	MB TO PT OR THE PT
0	0	0			0	1	X	X	X	X	X	X	MEMORY
1	1	0			0	0	X	X	X	X	X	X	MEMORY TO MB
0	0	0			0	0	X	X	X	X	X	X	MB TO AR/ARX
1	1	0			0	0	X	X	X	X	X	X	CACHE TO AR, THE CACHE OR MB TO AR/ARX

MR-2423

KL10 HARDWARE FAULTS (INT. MEM.)

CACHE	SWEEP REF	CHAN REF	DATA SOURCE	WRITE REF	OPERATION	COMMENTS	SBUS ERR	MB PAR ERR	WHERE DETECTED	PF CODE 25	PF CODE 36 OR 37	FAILING DATA PATH OR COMPONENT
1	1	1	0	0	PAGE REFILL	MEMORY READ OR RPW	0	1	MB	X	X	MEMORY TO MB
1	1	0	0	0			1	1	MB	X	X	MEMORY
1	1	0	0	0	READ		0	1	MB	X	X	MEMORY TO MB
1	1	0	0	0			1	1	MB	X	X	MEMORY
1	1	0	0	0			0	1	MB	X	X	MEMORY TO MB
1	1	0	0	0			0	1	MB	X	X	MEMORY TO MB
ON	0	1	1	0		CHAN DATA	0	1	MB	X	X	MB OR AR TO CACHE TO MB
1	0	1	0	1			0	1	MB	X	X	MASSBUS DEVICE TO RH TO CACHE TO MB
1	0	0	0	1	WRITE	CHAN STATUS	0	1	MB	X	X	CHAN TO MB
1	1	1	0	1		EBOX STORE	0	1	MB	X	X	AR TO MB
1	1	1	1	1		RPW	1	0	MB	X		MB TO MEMORY
ON	1	1	1	1	SWEEP	WRITEBACK	0	1	MB	X	X	CACHE TO MB OR THE CACHE
ON	1	1	1	1			0	1	MB	X	X	CACHE TO MB OR THE CACHE

MR-2422

KL10 PAGE FAIL TRAPS (EXT. MEM.)

CACHE	DATA SOURCE	WRITE REF	OPERATION	COMMENTS	SBUS ERR	MB PAR ERR	WHERE DETECTED			PF CODE 25	PF CODE 36 OR 37	FAILING DATA PATH OR COMPONENT
							DMA	MB	AR/ARX	PT		
1	1	0	PAGE REFILL	MEMORY READ OR RPW	1	1	X	X	X	X	X	MEMORY TO DMA
1	0	0			0	1	X	X	X	X	X	DMA TO MB
1	0	0	READ		0	0	X	X	X	X	X	MB TO PT OR THE PT
1	0	0			1	1	X	X	X	X	X	MEMORY TO DMA
1	0	0			0	0	X	X	X	X	X	DMA TO MB
1	0	0			0	0	X	X	X	X	X	MB TO AR/ARX
1	1	0			0	0	X	X	X	X	X	CACHE TO AR, THE CACHE OR MB TO AR/ARX

MR-2419



KL10 HARDWARE FAULTS (EXT. MEM.)

CACHE	SWEEP REF	CHAN REF	DATA SOURCE	WRITE REF	OPERATION	COMMENTS	SBUS ERR	MB PAR ERR	WHERE DETECTED	PF CODE 25	PF CODE 36 OR 37	FAILING DATA PATH OR COMPONENT
ON	1	1	1	1	PAGE REFILL	MEMORY READ OR RPW	0	1	DMA	X	X	DMA TO MB
ON	1	1	1	1	READ	CHAN DATA	0	1	MB	X	X	MEMORY TO DMA
ON	1	1	1	1	WRITE	CHAN STATUS	0	1	MB	X	X	MEMORY TO DMA
ON	1	1	1	1	WRITE	EBOX STORE	0	1	MB	X	X	DMA TO MB
ON	1	1	1	1	WRITE	RPW	0	1	MB	X	X	MEMORY TO DMA
ON	1	1	1	1	WRITE	WRITEBACK	0	1	MB	X	X	MEMORY TO DMA
ON	1	1	1	1	SWEEP		0	1	DMA	X	X	DMA TO MB
ON	1	1	1	1			0	1	PT	X	X	AR OR MB TO CACHE TO MB
ON	1	1	1	1			0	1	AR/RX	X	X	MASSBUS DEVICE TO RH TO CHAN TO MB
ON	1	1	1	1			0	1	MB	X	X	CHAN TO MB
ON	1	1	1	1			0	1	MB	X	X	AR TO MB
ON	1	1	1	1			0	1	MB	X	X	MB TO DMA
ON	1	1	1	1			0	1	MB	X	X	CACHE TO MB OR THE CACHE
ON	1	1	1	1			0	1	MB	X	X	CACHE TO MB OR THE CACHE

GEN. INFO.

MEMORY ADDRESS MAP

Double spaced at 16K  
Triple spaced at 64K

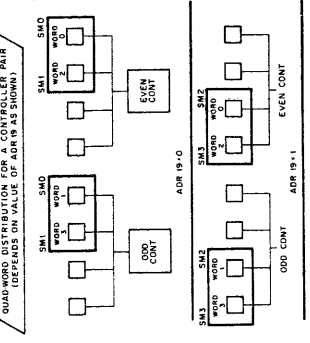
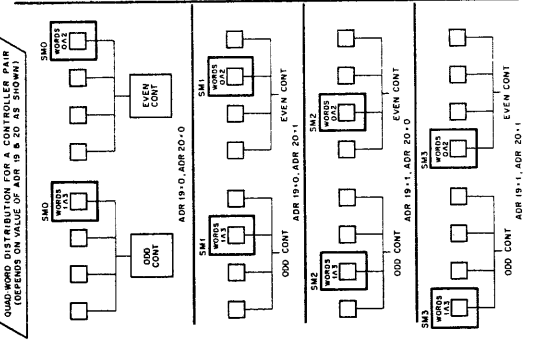
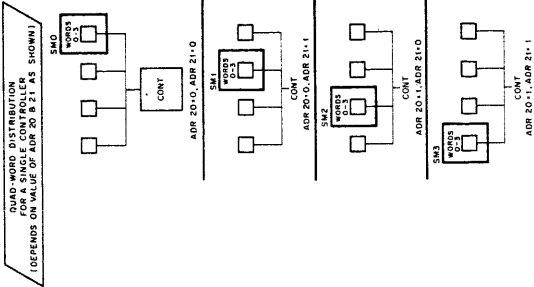
FROM	START	STOP	TO
0K	00	07777	4K
4K	10000	17777	8K
8K	20000	27777	12K
12K	30000	37777	16K
16K	40000	47777	20K
20K	50000	57777	24K
24K	60000	67777	28K
28K	70000	77777	32K
32K	100000	107777	36K
36K	110000	117777	40K
40K	120000	127777	44K
44K	130000	137777	48K
48K	140000	147777	52K
52K	150000	157777	56K
56K	160000	167777	60K
60K	170000	177777	64K
64K	200000	207777	68K
68K	210000	217777	72K
72K	220000	227777	76K
76K	230000	237777	80K
80K	240000	247777	84K
84K	250000	257777	88K
88K	260000	267777	92K
92K	270000	277777	96K
96K	300000	307777	100K
100K	310000	317777	104K
104K	320000	327777	108K
108K	330000	337777	112K
112K	340000	347777	116K
116K	350000	357777	120K
120K	360000	367777	124K
124K	370000	377777	128K
128K	400000	407777	132K
132K	410000	417777	136K
136K	420000	427777	140K
140K	430000	437777	144K
144K	440000	447777	148K
148K	450000	457777	152K
152K	460000	467777	156K
156K	470000	477777	160K
160K	500000	507777	164K
164K	510000	517777	168K
168K	520000	527777	172K
172K	530000	537777	176K
176K	540000	547777	180K
180K	550000	557777	184K
184K	560000	567777	188K
188K	570000	577777	192K

GEN. INFO.

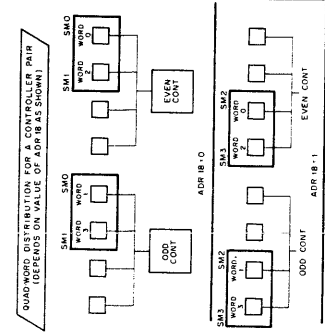
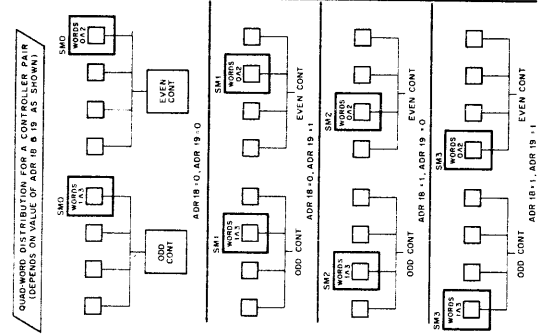
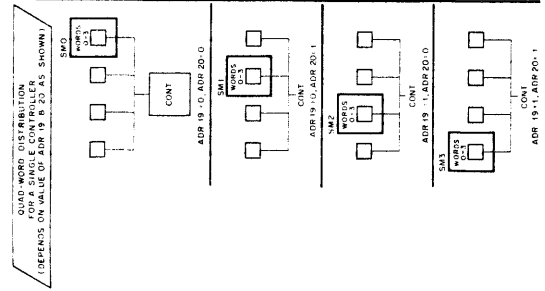
-45-

192K	600000	607777	196K
196K	610000	617777	200K
200K	620000	627777	204K
204K	630000	637777	208K
208K	640000	647777	212K
212K	650000	657777	216K
216K	660000	667777	220K
220K	670000	677777	224K
224K	700000	707777	228K
228K	710000	717777	232K
232K	720000	727777	236K
236K	730000	737777	240K
240K	740000	747777	244K
244K	750000	757777	248K
248K	760000	767777	252K
252K	770000	777777	256K

MA20 1, 2 AND 4-WAY INTERLEAVING



MB20 1, 2 AND 4-WAY INTERLEAVING



GEN. INFO.

-48-

MAGTAPE FORMATS

7 TRACK

TRACK 7	P	P	P	P	P	P	/	C
TRACK 6	0	6	12	18	24	30	/	B
TRACK 5	1	7	13	19	25	31	L	A
TRACK 4	2	8	14	20	26	32	P	8
TRACK 3	3	9	15	21	27	33	C	4
TRACK 2	4	10	16	22	28	34	C	2
TRACK 1	5	11	17	23	29	35	/	1
	REFERENCE EDGE							

9 TRACK (INDUSTRY COMPATIBILITY MODE)

TRACK 9	4	12	20	28	/	/	/	4
TRACK 8	6	14	22	30	/	/	/	6
TRACK 7	0	8	16	24	/	/	/	0
TRACK 6	1	9	17	25	C	L	L	1
TRACK 5	2	10	18	26	R	P	P	2
TRACK 4	P	P	P	P	C	C	C	C
TRACK 3	3	11	19	27	/	/	/	3
TRACK 2	7	15	23	31	/	/	/	7
TRACK 1	5	13	21	29	/	/	/	5
	REFERENCE EDGE							

9 TRACK (CORE DUMP MODE)

TRACK 9	4	12	20	28	32	/	/	/	4
TRACK 8	6	14	22	30	34	/	/	/	6
TRACK 7	0	8	16	24	/	/	/	/	0
TRACK 6	1	9	17	25	C	L	L	L	1
TRACK 5	2	10	18	26	30	R	P	P	2
TRACK 4	P	P	P	P	P	C	C	C	C
TRACK 3	3	11	19	27	31	/	/	/	3
TRACK 2	7	15	23	31	35	/	/	/	7
TRACK 1	5	13	21	29	33	/	/	/	5
	REFERENCE EDGE								

RELATIONSHIP BETWEEN TRACK NO. AND CRC REGISTER BIT POSITIONS:

TRACK NO	1	2	3	4	5	6	7	8	9
CRC REG. BIT	7	9	5	1	4	3	2	8	6

MR-2209

GEN. INFO.

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NOTES

COMPANY CONFIDENTIAL

TX0x/TU7x SENSE BYTES

BYTE 1 T	0 (8)	1 (4)	2 (2)	3 (1)	4 (8)	5 (4)	6 (2)	7 (1)	BYTE I T
0	COMMAND REJECT	INTERVENTION REQUIRED	BUS OUT CHECK	EQUIPMENT CHECK	DATA CHECK	OVERRUN	WORD COUNT ZERO	DATA CONVERT CHECK	0
1	NOISE	TU STATUS A	TU STATUS B	7-TRK	LOAD POINT	SELECTED & WR STAT	FILE PROTECTED	NOT CAPABLE	1
2		TRACK		IN		ERROR			2
3	R/W VRC	MTE/LRC	SKREW ERROR	END DATA CK /CRC	ENV CK/ SKREW VRC	1600 BPI SET IN TU	BACKWARD	C/P COMP.	3
4		REJECT TU	TI	WRITE TRG VRC		LWR	TU CHECK	RPQ	4
5		NEW SUBSYSTEM	WTM CHECK	ID BURST CK	* START READ CHECK	* PARTIAL RECORD	** POSTAMBLE**	RPQ	5
6	7-TRK TU	** WRITE CURRENT FAIL	** DUAL DENSITY TU	NOT 1600	**	TAPE UNIT MODEL IDENTIFICATION			6
7	COLUMN TOP OR BTM	*** LEFT COL. FAIL	RIGHT COL. FAIL	RESET KEY	DSE FAILURE	ERASE HD FAILURE		LOAD FAILURE	7
8	IBG DETECTED	**	CHANNEL	CRC III	**				8
9	6250 CORRECTION	*** VELOCITY CHANGE	BUFFER CK	RECORD NOT DETECTED	6250	TACH START FAIL		TCU RESERVED VELOCITY CHECK	9
10	CMND STAT REJECT	**							10
11									11

\* TX01 ONLY \*\* TX02 ONLY \*\*\* TU72 ONLY

MR-2309





GEN. INFO.

DIAGNOSTIC FUNCTIONS

KL10(PA and PV) Diagnostic Execute (Control) Functions

Function	Mnemonic	Operation
CLOCK CONTROL		
00	STPCLK	STOP THE KL10 CLOCK
01	STRCLK	START THE KL10 CLOCK
02	SSCLK	SINGLE STEP THE MBOX CLOCK
03	SECLK	SINGLE STEP THE EBOX CLOCK. LEAVES THE EBOX CLOCK FALSE AND EBOX SYNC TRUE. CAUSES (2,3) MBOX CLOCKS DEPENDING ON EBOX CLOCK INITIALLY (FALSE,TRUE). DOES NOT DEPEND ON 'T' FIELD OR MB WAIT.
04	CECLK	CONDITIONALLY ISSUE AN MBOX CLOCK IF THE EBOX CLOCK IS TRUE. MAKES EBOX CLOCK FALSE. IF ISSUED IN THE MASTER RESET STATE, LEAVES EBOX SYNC TRUE.
05	BRCLK	ISSUE A BURST OF CLOCKS. THE NUMBER OF MBOX CLOCKS DESIRED (1-255) HAS BEEN LOADED PREVIOUSLY BY FUNCTIONS 42,43.
06	CLRMR	CLEAR MASTER RESET STATE.
07	SETMR	SET MASTER RESET STATE. RUNNING THE CLOCK WHILE IN THIS STATE 'CLEARS' THE KL10.
EBOX CONTROL		
10	CLRRUN	CLEAR THE RUN FLOP. MAKE THE MICRO-CODE GO TO THE "HALT LOOP".
11	SETRUN	SET THE RUN FLOP. ALLOW REPEATED INSTRUCTION EXECUTION.
12	CONBUT	SET THE CONTINUE FLOP (MOMENTARY). ALLOW THE MICROCODE TO LEAVE THE HALT LOOP.
14	IRLTCH	UNLATCH THE IR AND LOAD IT FROM THE AD.
15	DRLTCH	UNLATCH THE DRAM REGISTER AND ALLOW IT TO LOAD FROM THE RAMS.

KL10(PA and PV) Diagnostic Write Functions

CLOCK 'LOAD' FUNCTIONS.

42	LDBRR	LOAD THE RIGHTHAND 4 BITS OF THE 8-BIT BURST COUNTER FROM EBUS BITS 32-35																														
43	LDBRL	LOAD THE LEFTHAND 4 BITS OF THE BURST CTR.																														
44	LDSEL	LOAD THE CLOCK SOURCE AND RATE SELECT REGISTER:																														
		<table border="1"> <thead> <tr> <th>32</th> <th>33</th> <th>SOURCE</th> <th>34</th> <th>35</th> <th>RATE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>NORM XTAL</td> <td>0</td> <td>0</td> <td>NORMAL</td> </tr> <tr> <td>0</td> <td>1</td> <td>FAST XTAL</td> <td>0</td> <td>1</td> <td>DIVIDE BY 2</td> </tr> <tr> <td>1</td> <td>0</td> <td>EXTERN</td> <td>1</td> <td>0</td> <td>DIVIDE BY 4</td> </tr> <tr> <td>1</td> <td>1</td> <td>FAST XTAL</td> <td>1</td> <td>1</td> <td>DIVIDE BY 8</td> </tr> </tbody> </table>	32	33	SOURCE	34	35	RATE	0	0	NORM XTAL	0	0	NORMAL	0	1	FAST XTAL	0	1	DIVIDE BY 2	1	0	EXTERN	1	0	DIVIDE BY 4	1	1	FAST XTAL	1	1	DIVIDE BY 8
32	33	SOURCE	34	35	RATE																											
0	0	NORM XTAL	0	0	NORMAL																											
0	1	FAST XTAL	0	1	DIVIDE BY 2																											
1	0	EXTERN	1	0	DIVIDE BY 4																											
1	1	FAST XTAL	1	1	DIVIDE BY 8																											
45	LDDIS	LOAD THE REGISTER WHICH CONTROLS THE EBOX CLOCK DISTRIBUTION.																														
		<table border="1"> <thead> <tr> <th>BIT</th> <th>ACTION</th> </tr> </thead> <tbody> <tr> <td>33</td> <td>DISABLE CONTROL RAM CLOCK</td> </tr> <tr> <td>34</td> <td>DISABLE DATA PATHS CLOCK</td> </tr> <tr> <td>35</td> <td>DISABLE CONTROL LOGIC CLOCK</td> </tr> </tbody> </table>	BIT	ACTION	33	DISABLE CONTROL RAM CLOCK	34	DISABLE DATA PATHS CLOCK	35	DISABLE CONTROL LOGIC CLOCK																						
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35	DISABLE CONTROL LOGIC CLOCK																															
46	LDCHK1	LOAD THE CONDITION-CHECKING ENABLE REGISTER: THESE ALL ENABLE THE CLOCK TO STOP AND SHOULD BE USED IN CONJUNCTION WITH BIT 35 OF FUNCTION 47.																														
		<table border="1"> <thead> <tr> <th>BIT</th> <th>FUNCTION</th> </tr> </thead> <tbody> <tr> <td>32</td> <td>CHECK FM PARITY</td> </tr> <tr> <td>33</td> <td>CHECK CRAM PARITY</td> </tr> <tr> <td>34</td> <td>CHECK DRAM PARITY</td> </tr> <tr> <td>35</td> <td>CHECK FIELD SERVICE 'PROBE'</td> </tr> </tbody> </table>	BIT	FUNCTION	32	CHECK FM PARITY	33	CHECK CRAM PARITY	34	CHECK DRAM PARITY	35	CHECK FIELD SERVICE 'PROBE'																				
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47 LDCHK2 LOAD THE ENABLE/DISABLE FUNCTION REGISTER:  
 BIT FUNCTION  
 32 DISABLE EBOX REQUESTS TO MBOX  
 33 SIMULATE AN MB RESP FOR EACH MB WAIT.  
 34 CHECK AR AND ARX PARITY AND CAUSE A 'PAGE FAIL' UCODE TRAP IF ERROR.  
 35 MUST BE SET TO PERFORM DESIRED ACTION OF FUNCTION 46 (ABOVE). STOPS ALL CLOCKS IF AN ERROR IS DETECTED.

CONTROL RAM LOAD FUNCTIONS

51 LCRDAR 00-05 CRAM DIAG ADR 05-10  
 52 LCRDAL 01-05 CRAM DIAG ADR 00-04  
 53 LCRAM5 00-05 EA CALL & DISP 00-04

		BITS		
		EBUS	CRAM	
54	LCRAM4	08	60	
		10	62	
		14	64	
		16	66	NOTE
		20	68	ODD NUMBERED BITS ABOVE 60 ARE NONEXISTENT.
		22	70	
		26	72	
		28	74	
		32	76	
		34	78	
55	LCRAM3	08-11	40-43	
		14-17	44-47	
		20-23	48-51	
		26-29	52-55	
		32-35	56-59	
56	LCRAM2	08-11	20-23	
		14-17	24-27	
		20-23	28-31	
		26-29	32-35	
		32-35	36-39	
57	LCRAM1	08-11	00-03	
		14-17	04-07	
		20-23	08-11	
		26-29	12-15	
		32-35	16-19	

LOAD DRAM FUNCTIONS

		BITS		
60	LDRAM1	12-14	DRAM A00-02, EVEN ADDRESSES	
		15-17	DRAM B00-02, EVEN ADDRESSES	
61	LDRAM2	12-14	DRAM A00-02, ODD ADDRESSES	
		15-17	DRAM B00-02, ODD ADDRESSES	
62	LDRAM3	14-17	COMMON J01-04	
63	LDRJEV	15-17	J08-10, EVEN ADDRESSES	
		12	PARITY BIT, EVEN ADDRESSES	
64	LDRJOD	14	COMMON J07 (NOTE: J05 AND J06 DO NOT EXIST.)	
		15-17	J08-10, ODD ADDRESSES	
		12	PARITY BIT, ODD ADDRESSES	

IR, DRAM CONTROL FUNCTIONS

65 DISIOJ DISABLE SPECIAL DECODE OF OP CODES 254, 7XX.  
 66 DISACF DISABLE IR AC OUTPUTS.  
 67 ENIOJA ENABLE KL10 STYLE DECODING OF OP CODES AND AC'S.

CHANNEL CONTROL FUNCTIONS

70 THIS FUNCTION IS USED TO ESTABLISH CERTAIN CONDITIONS WITHIN THE CHANNEL NEEDED FOR DEVICELESS TESTING. THIS FUNCTION SHOULD NOT BE USED WITHOUT PROPER TIMING SYNCHRONIZATION.

EBUS BIT	OPERATION
06	SIMULATE CBUS RESET
07	SIMULATE CBUS START
09	SIMULATE CBUS DONE
10	SIMULATE CBUS CTOM
11	SIMULATE CBUS STORE
12	SET DIAG SLOW REQ
13	SET DIAG FAST REQ

GEN. INFO.

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MBOX CONTROL FUNCTIONS

71 LDMBXA CONTROL OF THE MEMORY TO CACHE SELECTOR (MEM TO C SEL 1,2) IS GIVEN THROUGH THE FUNCTION LDMBXA (071) USING SIX EBUS BITS TO LOAD A CONTROL REGISTER. THIS REGISTER IS NOT INITIALIZED BY MR RESET AND THEREFORE MUST BE LOADED BEFORE NORMAL USE OF THE KL10.

BITS	FUNCTION
34 35	CONTROL MEM TO CACHE MIXER ENABLE
0 0	UNDEFINED
0 1	FORCE MIXER ENABLE
1 0	ALLOW NORMAL OPERATION. MR RESET STATE
1 1	UNDEFINED
32 33	SELECT THE SOURCE OF SEL 2 AND SEL 1
0 0	INCLUSIVE OR BITS 30 AND 31 WITH THE NORMAL SOURCE OF SEL 2 AND SEL 1, RESPECTIVELY.
0 1	REPLACE NORMAL SOURCE WITH BITS 30, 31.
1 0	ALLOW ONLY THE NORMAL INPUTS. THIS IS WHAT THE CONSOLE SHOULD SUPPLY FOR NORMAL OPERATION.
1 1	FORCE SEL 2 AND SEL 1 FALSE. SELECT AR
30 31	(INVERTED) INPUTS TO SEL 2, SEL 1
1 1	SELECT AR
1 0	SELECT MB
0 1	SELECT MEM

NOTE THE FOLLOWING FUNCTION (76) MUST BE INITIALIZED BY THE CONSOLE MASTER RESET SOFTWARE.

76 SBUS CONTROLLER RESET  
 24=1 WILL SET THE MEM RESET FLIP-FLOP  
 24=0 WILL CLEAR THE MEM RESET FLIP-FLOP

TO CLEAR ALL MEMORY CONTROLLERS, SET THE MEM RESET FLIP-FLOP, RUN THE CLOK, THEN CLEAR THE MEM REST FLIP-FLOP.

CHANNEL CLOCK CONTROL

25=1 INHIBIT MBOX CLOCK DISTRIBUTION TO THE CHANNEL LOGIC.  
 25=0 ENABLE MBOX CLOCK DISTRIBUTION TO THE CHANNEL LOGIC

EBUS REGISTER LOAD ENABLE

26=1 ENABLE EBUS REGISTER LOADING ON EVERY CLOCK TICK  
 26=0 DISABLE EBUS REGISTER LOADING ON EVERY CLOCK TICK

FORCE EXTENDED ADDRESSING (KL10(PV) ONLY)

27=1 CAUSES THE EFFECTIVE ADDRESS CALCULATIONS TO OCCUR AD IF THE VMA, PC & PCS SECTIONS WERE NONZERO IN ANY SECTION. TRUE UNTIL A FUNCTION WRITE 76 WITH BIT 27=0 IS EXPECTED.

AR LOAD FUNCTION

77 LDAR 0-35 LOAD THE AR FROM EBUS 0-35.

KL10 (PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	100	03	PIC1 M8532	PIC1 PIH1 H
**	100	04	PIC1 M8532	PIC1 PIH2 H
**	100	05	PIC1 M8532	PIC1 PIH3 H
**	100	06	PIC1 M8532	PIC1 PIH4 H
**	100	07	PIC1 M8532	PIC1 PIH5 H
**	100	08	PIC1 M8532	PIC1 PIH6 H
**	100	09	PIC1 M8532	PIC1 PIH7 H
**	100	10	PIC1 M8532	PIC1 ACTIVE H
**	100	11	PIC1 M8532	PIC1 ON 1 H
**	100	12	PIC1 M8532	PIC1 ON 2 H
**	100	13	PIC1 M8532	PIC1 ON 3 H
**	100	14	PIC1 M8532	PIC1 ON 4 H
**	100	15	PIC1 M8532	PIC1 ON 5 H
**	100	16	PIC1 M8532	PIC1 ON 6 H
**	100	17	PIC1 M8532	PIC1 ON 7 H
**	100	18	MCL3 M8530	VMA HELD OR PC 01 H
**	100	19	MCL3 M8530	VMA HELD OR PC 02 H
**	100	20	MCL3 M8530	VMA HELD OR PC 03 H
**	100	21	MCL3 M8530	VMA HELD OR PC 04 H
**	100	22	MCL3 M8530	VMA HELD OR PC 05 H
**	100	23	MCL3 M8530	VMA HELD OR PC 06 H
**	100	24	CTL1 M8527	CTL SPEC/SCM ALT H
**	100	25	CTL1 M8527	CTL SPEC/SAVE FLAGS L
**	100	26	CTL2 M8527	CTL ARL SEL 2 H
**	100	27	CTL2 M8527	CTL ARR LOAD A L
**	100	28	CTL2 M8527	CTL AR 00-08 LOAD L
**	100	30	CLK1 M8526	CLK EBUS CLK H
**	100	31	CLK1 M8526	CLK SBUS CLK H
**	100	33	CLK5 M8526	CLK BURST CNT=0 H
**	100	34	CLK5 M8526	CLK BURST 128 H
**	100	35	CLK5 M8526	CLK BURST 64 H
**	101	11	PIC1 M8532	PIC1 GEN 1 H
**	101	12	PIC1 M8532	PIC1 GEN 2 H
**	101	13	PIC1 M8532	PIC1 GEN 3 H
**	101	14	PIC1 M8532	PIC1 GEN 4 H
**	101	15	PIC1 M8532	PIC1 GEN 5 H
**	101	16	PIC1 M8532	PIC1 GEN 6 H
**	101	17	PIC1 M8532	PIC1 GEN 7 H
**	101	18	MCL3 M8530	VMA HELD OR PC 07 H
**	101	19	MCL3 M8530	VMA HELD OR PC 08 H
**	101	20	MCL3 M8530	VMA HELD OR PC 09 H
**	101	21	MCL3 M8530	VMA HELD OR PC 10 H
**	101	22	MCL3 M8530	VMA HELD OR PC 11 H
**	101	23	MCL3 M8530	VMA HELD OR PC 12 H
**	101	24	CTL1 M8527	CTL SPEC/CLR FPD H
**	101	25	CTL1 M8527	CTL SPEC MTR CTL L
**	101	26	CTL2 M8527	CTL ARL SEL 1 H
**	101	27	CTL2 M8527	CTL ARR LOAD B L
**	101	28	CTL2 M8527	CTL AR 09-17 LOAD L
**	101	30	CLK5 M8526	CLK BURST 32 H
**	101	31	CLK5 M8526	CLK BURST 16 H
**	101	32	CLK5 M8526	CLK BURST 08 H
**	101	33	CLK5 M8526	CLK BURST 04 H
**	101	34	CLK5 M8526	CLK BURST 02 H
**	101	35	CLK5 M8526	CLK BURST 01 H
**	102	11	PIC4 M8532	EBUS CS05 E H
**	102	12	PIC4 M8532	EBUS CS06 E H
**	102	13	PIC2 M8532	EBUS DEMAND E H
**	102	14	PIC4 M8532	EBUS CS00 E H
**	102	15	PIC4 M8532	EBUS CS01 E H
**	102	16	PIC4 M8532	EBUS CS02 E H
**	102	17	PIC4 M8532	EBUS CS03 E H
**	102	18	MCL2 M8530	MCL VMA READ H
**	102	19	MCL1 M8530	MCL MEM/ARL IND H
**	102	20	MCL2 M8530	MCL PAGE TEST PRIVATE H
**	102	21	MCL4 M8530	MCL XR PREVIOUS H
**	102	22	MCL4 M8530	MCL VMA GETS AD H
**	102	23	MCL5 M8530	ARM 12 H
**	102	24	CTL1 M8527	CTL SPEC/GEN CRY 18 H
**	102	25	CTL1 M8527	CTL COND/AR GETS EXP H
**	102	26	CTL2 M8527	CTL ARR SEL 2 H
**	102	27	CTL2 M8527	CTL MQM SEL 2 H
**	102	28	CTL2 M8527	CTL ARX LOAD H
**	102	30	CLK1 M8526	CLK ERROR STOP H
**	102	31	CLK2 M8526	CLK GO L
**	102	32	CLK4 M8526	CLK EBOX REQ H
**	102	33	CLK3 M8526	CLK SYNC H
**	102	34	CLK4 M8526	CLK PAGE FAIL EN L
**	102	35	CLK4 M8526	CLK FORCE 1777 H

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KL10 (PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH	
103	11	PIC2	M8532	PIC2 TIMER DONE H	
103	12	PIC5	M8532	PIC5 EBUS PI GRANT H	
103	13	PIC2	M8532	PIC2 STATE HOLD H	
**	103	14	PIC4	M8532	EBUS CS04 E H
103	15	PIC2	M8532	PIC2 HONOR INTERNAL H	
103	16	PIC2	M8532	PIC2 READY H	
103	17	PIC5	M8532	PIC5 EBUS REQ H	
103	18	MCL2	M8530	MCL VMA PAUSE H	
103	19	MCL1	M8530	MCL REQ EN L	
103	20	MCL3	M8530	MCL VMA UPT H	
103	21	MCL4	M8530	MCL PREV COND L	
103	22	MCL4	M8530	MCL VMA INC H	
103	23	MCL5	M8530	MCL PREV SEC TO ARMM H	
103	24	CTL1	M8527	CTL SPEC/SECTION HOLD H	
103	25	CTL1	M8527	CTL DISP RET L	
103	26	CTL2	M8527	CTL ARR SEL 1 H	
103	27	CTL2	M8527	CTL MQM SEL 1 H	
103	28	CTL2	M8527	CTL ARL SEL 4 H	
103	30	CLK3	M8526	CLK DRAM PAR ERR H	
103	31	CLK2	M8526	CLK BURST L	
103	32	CLK4	M8526	CLK MB XFER H	
103	33	CLK4	M8526	CLK EBOX CLK L	
103	34	CLK4	M8526	CLK INSTR 1777 H	
103	35	CLK4	M8526	CLK 1777 EN H	
104	18	MCL2	M8530	MCL VMA WRITE H	
104	19	MCL2	M8530	MCL VMA USER H	
104	20	MCL3	M8530	MCL PAGE UEBR REF H	
104	21	MCL4	M8530	MCL VMAX EN L	
104	22	MCL4	M8530	MCL LOAD VMA CONTEXT L	
104	23	MCL6	M8530	MCL EBOX CACHE L	
104	24	CTL1	M8527	CTL SPEC/FLAG CTL H	
104	25	CTL1	M8527	CTL LOAD PC L	
104	26	CTL2	M8527	CTL ARXL SEL 2 H	
104	27	CTL2	M8527	CTL MQ SEL 2 H	
104	28	CTL2	M8527	CTL AR 00-11 CLR H	
104	30	CLK3	M8526	CLK CRAM PAR ERR H	
104	31	CLK2	M8526	CLK EBOX SS L	
104	32	CLK5	M8526	CLK SOURCE SEL 2 H	
104	33	CLK3	M8526	CLK EBOX SOURCE H	
104	34	CLK5	M8526	CLK FM PAR CHECK L	
104	35	CLK5	M8526	CLK MBOX CYCLE DIS H	
105	18	MCL2	M8530	MCL LOAD AR H	
105	19	MCL2	M8530	MCL VMA PUBLIC H	
105	20	MCL3	M8530	MCL PAGE ADDRESS COND H	
105	21	MCL4	M8530	MCL VMAX SEL 2 H	
105	22	MCL4	M8530	MCL 23 BIT EA H	
105	23	MCL6	M8530	MCL EBOX MAY BE PAGED L	
105	24	CTL1	M8527	CTL SPEC/SP MEM CYCLE H	
105	25	CTL1	M8527	CTL ADX CRY 36 H	
105	26	CTL2	M8527	CTL ARXL SEL 1 H	
105	27	CTL2	M8527	CTL MQ SEL 1 H	
105	28	CTL2	M8527	CTL AR 12-17 CLR H	
105	30	CLK3	M8526	CLK FM PAR ERR H	
105	31	SHD1	M8526	SH AR PAR ODD H	
105	32	CLK5	M8526	CLK SOURCE SEL 1 H	
105	33	CLK5	M8526	CLK EBOX CRM DIS H	
105	34	CLK5	M8526	CLK CRAM PAR CHECK L	
105	35	CLK5	M8526	CLK MBOX RESP SIM L	
106	18	MCL2	M8530	MCL LOAD ARX H	
106	19	MCL2	M8530	MCL VMA PREVIOUS L	
106	20	MCL3	M8530	MCL PAGE ILL ENTRY H	
106	21	MCL4	M8530	MCL VMAX SEL 1 H	
106	22	MCL4	M8530	MCL 18 BIT EA H	
106	23	MCL6	M8530	MCL REG FUNC H	
106	24	CTL1	M8527	CTL AD LONG H	
106	25	CTL1	M8527	CTL ADX CRY 36 A H	
106	26	CTL2	M8527	CTL ARXR SEL 2 H	
106	27	CTL2	M8527	CTL MQM EN H	
106	28	CTL2	M8527	CTL ARR CLR H	
106	30	CLK3	M8526	CLK FS ERROR H	
106	31	SHD1	M8526	SH ARX PAR ODD H	
106	32	CLK5	M8526	CLK RATE SEL 2 H	
106	33	CLK5	M8526	CLK EBOX EDP DIS H	
106	34	CLK5	M8526	CLK DRAM PAR CHECK L	
106	35	CLK5	M8526	CLK AR/ARX PAR CHECK L	
107	18	MCL2	M8530	MCL STORE AR L	
107	19	MCL2	M8530	MCL VMA EXTENDED L	
107	20	MCL4	M8530	MCL EA TYPE 10 H	
107	21	MCL4	M8530	MCL EA TYPE 09 H	

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH	
107	22	MCL5	M8530	MCL MBOX CYC REQ H	
107	23	MCL6	M8530	MCL EBOX MAP L	
107	24	CTL1	M8527	CTL INH CRY 18 L	
107	25	CTL3	M8527	DIAG MEM RESET H	
107	26	CTL2	M8527	CTL ARXR SEL 1 H	
107	27	CTL3	M8527	DIAG LOAD EBUS REG L	
107	28	CTL2	M8527	CTL SPEC CALL L	
107	30	CLK3	M8526	CLK ERROR L	
107	31	CLK4	M8526	CLK PAGE FAIL H	
107	32	CLK5	M8526	CLK RATE SEL 1 H	
107	33	CLK5	M8526	CLK EBOX CTL DIS H	
107	34	CLK5	M8526	CLK FS CHECK L	
107	35	CLK5	M8526	CLK ERR STOP EN L	
110	01	APR2	M8539	APR SWEEP BUSY EN H	
110	06	APR1	M8539	APR SBUS ERR IN H	
110	07	APR1	M8539	APR NXM ERR IN H	
110	08	APR1	M8539	APR I/O PF ERR IN H	
110	09	APR1	M8539	APR MB PAR ERR IN H	
110	10	APR2	M8539	APR C DIR P ERR IN H	
110	11	APR2	M8539	APR S ADR P ERR IN H	
110	12	APR2	M8539	APR PWR FAIL IN H	
110	13	APR2	M8539	APR SWEEP DONE IN H	
110	14	APR2	M8539	APR APR INTERRUPT H	
110	15	PIC3	M8539	PT3 APR PIA 04 H	
110	16	PIC3	M8539	PT3 APR PIA 02 H	
110	17	PIC3	M8539	PT3 APR PIA 01 H	
*	110	20-35	MTR1	M8538	MTR TIME 02-17 H
	111	06	APR5	M8539	APR CURRENT BLOCK 4 H
	111	07	APR5	M8539	APR CURRENT BLOCK 2 H
	111	08	APR5	M8539	APR CURRENT BLOCK 1 H
	111	09	APR5	M8539	APR PREV BLOCK 4 H
	111	10	APR5	M8539	APR PREV BLOCK 2 H
	111	11	APR5	M8539	APR PREV BLOCK 1 H
	111	12	APR3	M8539	APR CWSX H
	111	13	APR3	M8539	APR PREV SEC 13 H
	111	14	APR3	M8539	APR PREV SEC 14 H
	111	15	APR3	M8539	APR PREV SEC 15 H
	111	16	APR3	M8539	APR PREV SEC 16 H
	111	17	APR3	M8539	APR PREV SEC 17 H
*	111	20-35	MTR1	M8538	MTR PERF COUNT 02-17 H
	112	06	APR1	M8539	APR SBUS ERR EN IN H
	112	07	APR1	M8539	APR NXM ERR EN IN H
	112	08	APR1	M8539	APR I/O PF ERR EN IN H
	112	09	APR1	M8539	APR MB PAR ERR EN IN H
	112	10	APR2	M8539	APR C DIR P ERR EN IN H
	112	11	APR2	M8539	APR S ADR P ERR EN IN H
	112	12	APR2	M8539	APR PWR FAIL EN IN H
	112	13	APR2	M8539	APR SWEEP DONE EN IN H
*	112	20-35	MTR1	M8538	MTR EBOX COUNT 02-17 H
	113	09	APR3	M8539	APR FETCH COMP H
	113	10	APR3	M8539	APR READ COMP H
	113	11	APR3	M8539	APR WRITE COMP H
	113	12	APR3	M8539	APR USER COMP H
*	113	20-35	MTR1	M8538	MTR CACHE COUNT 02-17 H
	114	07	APR5	M8539	APR MBOX CTL 03 H
**	114	08	APR5	M8539	APR FM BLOCK 4 H
**	114	09	APR5	M8539	APR FM BLOCK 2 H
**	114	10	APR5	M8539	APR FM BLOCK 1 H
**	114	11	APR4	M8539	APR FM ADR 10 H
**	114	12	APR4	M8539	APR FM ADR 4 H
**	114	13	APR4	M8539	APR FM ADR 2 H
**	114	14	APR4	M8539	APR FM ADR 1 H
	114	15	APR4	M8539	APR F02 EN H
	114	16	APR3	M8539	APR FM 36 H
	114	17	APR3	M8539	APR FM ODD PARITY H
*	114	24-35	MTR1	M8538	MTR INTERVAL 06-17 H
	115	07	APR5	M8539	APR MBOX CTL 06 H
	115	08	APR5	M8539	APR SET PAGE FAIL L
	115	09	APR3	M8539	APR EBUS RETURN H
	115	10	APR3	M8539	APR EBOX DISABLE CS H
	115	11	APR2	M8539	APR WR BAD ADR PAR L
	115	12	APR6	M8539	APR EBOX CCA H
	115	13	APR6	M8539	APR EBOX ERA H
	115	14	APR6	M8539	APR EBOX SBUS DIAG H
	115	15	APR6	M8539	MCL MEM/REG FUNC L
	115	16	APR6	M8539	APR EBOX LOAD REG L
	115	17	APR6	M8539	APR EBOX READ REG L
	115	21	MTR3	M8538	MTR3 INTERVAL ON H
	115	22	MTR3	M8538	MTR3 INTERVAL DONE H
	115	23	MTR3	M8538	MTR3 INTERVAL OVRFLO H
*	115	24-35	MTR3	M8538	MTR PERIOD 06-17 H

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KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
116	07	APR5	M8539	APR WR PT SEL 0 H
116	08	APR5	M8539	APR PT DIR WR L
116	09	APR3	M8539	APR EBUS REQ L
116	10	APR3	M8539	APR EBUS F01 E H
116	11	APR2	M8539	APR ANY EBOX ERR FLG H
116	12	APR6	M8539	APR EBOX UBR H
116	13	APR6	M8539	APR EN REFILL RAM WR H
116	21	MTR2	M8538	MTR2 PI ACCT EN H
116	22	MTR2	M8538	MTR2 EXEC ACCT EN H
116	23	MTR2	M8538	MTR2 ACCT ON H
116	25	MTR2	M8538	MTR2 TIME ON H
**	116	33	PIC3	PI3 MTR PIA 04 H
**	116	34	PIC3	PI3 MTR PIA 02 H
**	116	35	PIC3	PI3 MTR PIA 01 H
117	07	APR5	M8539	APR WR PT SEL 1 H
117	08	APR5	M8539	APR PT WR L
117	09	APR3	M8539	APR EBUS DEMAND H
117	10	APR3	M8539	APR EBOX SEND F02 H
117	11	CON5	M8539	CON FM WRITE PAR L
117	12	APR6	M8539	APR EBOX EBR H
117	13	APR6	M8539	APR EBOX SPARE H
117	20	MTR5	M8538	MTR5 VECTOR REQ H
117	21	MTR5	M8538	MTR5 INCR SEL 2 H
117	22	MTR5	M8538	MTR5 INCR SEL 1 H
117	25	MTR3	M8538	MTR CONO MTR, L
**	120	00	EDP1	EDP AR 00 H
**	120	01	EDP1	EDP AR 01 H
**	120	02	EDP1	EDP AR 02 H
**	120	03	EDP1	EDP AR 03 H
**	120	04	EDP1	EDP AR 04 H
**	120	05	EDP1	EDP AR 05 H
**	120	06	EDP1	EDP AR 06 H
**	120	07	EDP1	EDP AR 07 H
**	120	08	EDP1	EDP AR 08 H
**	120	09	EDP1	EDP AR 09 H
**	120	10	EDP1	EDP AR 10 H
**	120	11	EDP1	EDP AR 11 H
*	120	12-35	EDP1	AR 12 TO 35 H
*	121	0-35	EDP4	BR 0 TO 35 H
*	122	0-35	EDP2	MQ 0 TO 35 H
*	123	0-35	EDP4	FM 0 TO 35 H
*	124	0-35	EDP4	BRX 0 TO 35 H
*	125	0-35	EDP2	ARX 0 TO 35 H
*	126	0-35	EDP3	ADX 0 TO 35 H
*	127	0-35	EDP3	AD 0 TO 35 H
130	02	SCD4	M8524	SCD TRAP REQ 2 H
130	03	SCD4	M8524	SCD TRAP CYC 2 H
130	04	SCD4	M8524	SCD TRAP CYC 1 H
130	05	SCD4	M8524	SCD TRAP REQ 1 H
130	06	SCD4	M8524	SCD FPD H
**	130	07	SCD2	SC 05 H
**	130	08	SCD2	SC 06 H
**	130	09	SCD2	SC 07 H
**	130	10	SCD2	SC 08 H
**	130	11	SCD2	SC 09 H
130	12	IRD3	M8522	IR NORM 08 H
130	13	IRD3	M8522	IR NORM 09 H
130	14	IRD3	M8522	IR NORM 10 H
**	130	15	IRD1	DR ADR 00 A H
**	130	16	IRD1	DR ADR 01 A H
**	130	17	IRD1	DR ADR 02 A H
130	18	CON3	M8525	CON WR EVEN PAR ADR H
130	19	CON3	M8525	CON3 WR EVEN PAR DATA H
130	20	CON3	M8525	CON3 WR EVEN PAR DIR H
131	02	SCD4	M8524	SCD OV H
131	03	SCD4	M8524	SCD CRY0 H
131	04	SCD4	M8524	SCD CRY1 H
131	05	EDP3	M8524	AD CRY 01 L
131	06	SCD4	M8524	SCD DIV CHK H
**	131	07	SCD2	SC 00 H
**	131	08	SCD2	SC 01 H
**	131	09	SCD2	SC 02 H
**	131	10	SCD2	SC 03 H
**	131	11	SCD2	SC 04 H
**	131	12	IRD1	DR ADR 03 A H
**	131	13	IRD1	DR ADR 04 A H
**	131	14	IRD1	DR ADR 05 A H
**	131	15	IRD1	DR ADR 06 A H
**	131	16	IRD1	DR ADR 07 A H
**	131	17	IRD1	DR ADR 08 A H
131	18	CON3	M8525	CON3 CACHE LOOK EN H



KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	131	19	CON3 M8525	CON CACHE LOAD EN H
	131	21	CON3 M8525	CON K110 PAGING MODE L
	131	22	CON3 M8525	CON TRAP EN H
	132	02	SCD4 M8524	VMA HELD OR PC 00 H
	132	03	SCD4 M8524	SCD FOV H
	132	04	SCD4 M8524	SCD FXU H
	132	05	EDP3 M8524	AD OVERFLOW 00 L
	132	06	IRD4 M8524	AD CRY -02 A L
**	132	07	SCD2 M8524	FE 05 H
**	132	08	SCD2 M8524	FE 06 H
**	132	09	SCD2 M8524	FE 07 H
**	132	10	SCD2 M8524	FE 08 H
**	132	11	SCD2 M8524	FE 09 H
	132	12	IRD3 M8522	IR EN I/O, JRST H
	132	13	IRD3 M8522	IR EN AC H
**	132	14	IRD1 M8522	IR AC 09 H
**	132	15	IRD1 M8522	IR AC 10 H
**	132	16	IRD1 M8522	IR AC 11 H
**	132	17	IRD1 M8522	IR AC 12 H
	132	18	CON1 M8525	CON COND EN 00-07 L
	132	19	CON1 M8525	CON COND/SEL VMA L
	132	20	CON1 M8525	CON COND/MBOX CTL L
	132	22	CON2 M8525	CON LOAD IR L
	132	23	CON4 M8525	CON4 AR LOADED H
	132	24	CON5 M8525	CON5 PI CYCLE H
	133	02	SCD4 M8524	SCD PCP H
	133	03	SCD5 M8524	SCD LOAD FLAGS A H
	133	04	SCD1 M8524	SCAD=0 L
	133	05	CON2 M8524	CON CLR PRIVATE INSTR H
**	133	06	SCD4 M8524	SCD NICOND 10 H
**	133	07	SCD2 M8524	FE 00 H
**	133	08	SCD2 M8524	FE 01 H
**	133	09	SCD2 M8524	FE 02 H
**	133	10	SCD2 M8524	FE 03 H
**	133	11	SCD2 M8524	FE 04 H
**	133	12	IRD1 M8522	DRAM A 00 H
**	133	13	IRD1 M8522	DRAM A 01 H
**	133	14	IRD1 M8522	DRAM A 02 H
**	133	15	IRD1 M8522	DRAM B 00 H
**	133	16	IRD1 M8522	DRAM B 01 H
**	133	17	IRD1 M8522	DRAM B 02 H
	133	18	CON1 M8525	CON SKIP EN 40-47 L
	133	19	CON1 M8525	CON COND/VMA GETS # H
	133	20	CON3 M8525	CON EBUS REL H
	133	21	CON4 M8525	CON PC+1 INH L
	133	22	CON2 M8525	CON COND INSTR ABORT H
	133	23	CON4 M8525	CON ARX LOADED L
	133	24	CON5 M8525	CON5 MEM CYCLE L
	134	02	SCD5 M8524	SCD USER A L
	134	03	SCD5 M8524	SCD LEAVE USER H
	134	04	CON5 M8524	CON PI CYCLE A L
	134	05	SCD5 M8524	SCD USER EN L
	134	06	SCD5 M8524	SCD PUBLIC PAGE H
	134	07	SCD2 M8524	SC SIGN H
	134	12	IRD3 M8522	TEST SATISFIED H
	134	13	IRD3 M8522	IR JRST 0, L
**	134	14	IRD1 M8522	DRAM J 01 H
**	134	15	IRD1 M8522	DRAM J 02 H
**	134	16	IRD1 M8522	DRAM J 03 H
**	134	17	IRD1 M8522	DRAM J 04 H
	134	18	CON1 M8525	CON SKIP EN 50-57 L
	134	19	CON1 M8525	CON COND/LOAD VMA HELD H
	134	20	CON3 M8525	CON SR 00 H
	134	21	CON2 M8525	CON NICOND TRAP EN H
	134	22	CON2 M8525	CON LOAD ACCESS COND H
	134	23	CON4 M8525	CON UCODE STATE 01 H
	134	24	CON5 M8525	CON FM WRITE PAR L
	135	02	SCD5 M8524	SCD PUBLIC EN L
	135	03	SCD5 M8524	SCD PUBLIC A H
	135	04	SCD5 M8524	SCD KERNEL MODE H
	135	05	SCD5 M8524	SCD PRIVATE INSTR L
	135	06	SCD5 M8524	SCD PRIVATE INSTR EN L
	135	07	SCD2 M8524	FE SIGN H
**	135	12	IRD1 M8522	DRAM PAR H
	135	13	IRD3 M8522	DRAM ODD PARITY H
**	135	14	IRD1 M8522	DRAM J 07 H
**	135	15	IRD1 M8522	DRAM J 08 H
**	135	16	IRD1 M8522	DRAM J 09 H
**	135	17	IRD1 M8522	DRAM J 10 H
	135	18	CON3 M8525	CON DELAY REQ H

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KL10 (PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
135	19	CON1	M8525	CON LOAD SPEC INSTR L
135	20	CON3	M8525	CON SR 01 H
135	21	CON2	M8525	CON NICOND 07 H
135	22	CON2	M8525	CON2 INSTR GO L
135	23	CON4	M8525	CON UCODE STATE 03 H
135	24	CON5	M8525	CON MBOX WAIT L
136	02	SCD5	M8524	SCD KERNEL OR USER IOT H
**	136	03	SCD3	SCD TRAP MIX 32 H
**	136	04	SCD3	SCD TRAP MIX 33 H
136	05	SCD5	M8524	SCD USER IOT A H
136	06	SCD5	M8524	SCD USER IOT EN L
136	07	SCD2	M8524	SC .GE. 36 H
136	12	IRD3	M8522	AD=0 L
136	13	IRD1	M8522	IR I/O LEGAL H
136	14	CTL1	M8522	CTL INH CRY 18 L
136	15	CTL1	M8522	CTL SPEC/GEN CRY 18 H
136	16	IRD4	M8522	GEN CRY 36 H
136	17	IRD4	M8522	AD CRY -02 A H
136	18	CON4	M8525	CON AR 36 H
136	19	CON1	M8525	CON VMA SEL 2 L
136	20	CON3	M8525	CON SR 02 H
136	21	CON2	M8525	CON NICOND 08 H
136	22	CON2	M8525	CON LOAD DRAM H
136	23	CON4	M8525	CON UCODE STATE 05 H
136	24	CON5	M8525	CON FM XFER L
137	02	SCD5	M8524	SCD ADR BRK INH H
137	03	SCD3	M8524	SCD TRAP MIX 34 H
**	137	04	SCD3	SCD TRAP MIX 35 H
**	137	05	SCD5	SCD ADR BRK CYC H
137	06	SCD5	M8524	SCD ADR BREAK PREVENT H
137	07	SCD4	M8524	SCD TRAP CLEAR L
137	12	IRD4	M8522	AD CRY 12 H
137	13	IRD4	M8522	AD CRY 18 H
137	14	IRD4	M8522	AD CRY 24 H
137	15	IRD4	M8522	AD CRY 36 H
137	16	IRD4	M8522	ADX CRY 12 H
137	17	IRD4	M8522	ADX CRY 24 H
137	18	CON4	M8525	CON ARX 36 H
137	19	CON1	M8525	CON VMA SEL 1 L
137	20	CON3	M8525	CON SR 03 H
137	21	CON2	M8525	CON NICOND 09 H
137	22	CON2	M8525	CON COND ADR 10 H
137	23	CON4	M8525	CON UCODE STATE 07 H
137	24	CON5	M8525	CON PI DISMISS L
140	00	CRA3	M8511	DISP EN 00-07 L
140	01	CRA3	M8511	DISP EN 00-03 L
140	02	CRA3	M8511	DISP EN 30-37 L
140	03	CRA3	M8511	DISP 02 A H
140	04	CRA3	M8511	DISP 03 A H
140	05	CRA3	M8511	DISP 04 A H
**	141	00	CRA3	CRA DISP PARITY H
**	141	01	CRA3	CRA DISP 00 H
**	141	02	CRA3	CRA DISP 01 H
**	141	03	CRA3	CRA DISP 02 H
**	141	04	CRA3	CRA DISP 03 H
**	141	05	CRA3	CRA DISP 04 H
**	142	00	CRA4	SBR RET 05 H
**	142	01	CRA4	SBR RET 06 H
**	142	02	CRA4	SBR RET 07 H
**	142	03	CRA4	SBR RET 08 H
**	142	04	CRA4	SBR RET 09 H
**	142	05	CRA4	SBR RET 10 H
**	143	01	CRA4	SBR RET 00 H
**	143	02	CRA4	SBR RET 01 H
**	143	03	CRA4	SBR RET 02 H
**	143	04	CRA4	SBR RET 03 H
**	143	05	CRA4	SBR RET 04 H
**	144	00	CRA2	CR ADR 05 F H
**	144	01	CRA2	CR ADR 06 F H
**	144	02	CRA2	CR ADR 07 F H
**	144	03	CRA2	CR ADR 08 F H
**	144	04	CRA2	CR ADR 09 F H
**	144	05	CRA2	CR ADR 10 F H
**	144	08	CRM5	CRAM 60 H
**	144	09	CRM5	CRAM PAR 1ST 00 H
**	144	10	CRM5	CRAM 62 H
**	144	11	CRM5	CRAM PAR 00 H
**	144	14	CRM5	CRAM 64 H
**	144	15	CRM5	CRAM PAR 1ST 04 H
**	144	16	CRM5	CRAM 66 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
**	144	17 CRM5	M8528 CRAM PAR 04 H
**	144	20 CRM5	M8528 CRAM 68 H
**	144	21 CRM5	M8528 CRAM PAR 1ST 08 H
**	144	22 CRM5	M8528 CRAM 70 H
**	144	23 CRM5	M8528 CRAM PAR 08 H
**	144	26 CRM5	M8528 CRAM 72 H
**	144	27 CRM5	M8528 CRAM PAR 1ST 12 H
**	144	28 CRM5	M8528 CRAM 74 H
**	144	29 CRM5	M8528 CRAM PAR 12 H
**	144	32 CRM5	M8528 CRAM 76 H
**	144	33 CRM5	M8528 CRAM PAR 1ST 16 H
**	144	34 CRM5	M8528 CRAM 78 H
**	144	35 CRM5	M8528 CRAM PAR 16 H
**	145	01 CRA1	M8511 CR ADR 00 F H
**	145	02 CRA1	M8511 CR ADR 01 F H
**	145	03 CRA1	M8511 CR ADR 02 F H
**	145	04 CRA1	M8511 CR ADR 03 F H
**	145	05 CRA1	M8511 CR ADR 04 F H
*	145	08-11 CRM5	M8528 CRAM 40-43 H
*	145	14-17 CRM5	M8528 CRAM 44-47 H
*	145	20-23 CRM5	M8528 CRAM 48-51 H
*	145	26-29 CRM5	M8528 CRAM 52-55 H
*	145	32-35 CRM5	M8528 CRAM 56-59 H
**	146	00 CRA3	M8511 CRA LOC 05 H
**	146	01 CRA3	M8511 CRA LOC 06 H
**	146	02 CRA3	M8511 CRA LOC 07 H
**	146	03 CRA3	M8511 CRA LOC 08 H
**	146	04 CRA3	M8511 CRA LOC 09 H
**	146	05 CRA3	M8511 CRA LOC 10 H
*	146	08-11 CRM5	M8528 CRAM 20-23 H
*	146	14-17 CRM5	M8528 CRAM 24-27 H
*	146	20-23 CRM5	M8528 CRAM 28-31 H
*	146	26-29 CRM5	M8528 CRAM 32-35 H
*	146	32-35 CRM5	M8528 CRAM 36-39 H
**	147	01 CRA3	M8511 CRA LOC 00 H
**	147	02 CRA3	M8511 CRA LOC 01 H
**	147	03 CRA3	M8511 CRA LOC 02 H
**	147	04 CRA3	M8511 CRA LOC 03 H
**	147	05 CRA3	M8511 CRA LOC 04 H
*	147	08-11 CRM5	M8528 CRAM 00-03 H
*	147	14-17 CRM5	M8528 CRAM 04-07 H
*	147	20-23 CRM5	M8528 CRAM 08-11 H
*	147	26-29 CRM5	M8528 CRAM 12-15 H
*	147	32-35 CRM5	M8528 CRAM 16-19 H

NOTE ABOUT READING VMA BOARD REGISTERS  
 THESE FORMULAS TERSELY DESCRIBE THE DIAGNOSTIC FUNCTION (150-157)  
 AND EBUS BIT NUMBER (13-35, ODD) CORRESPONDING TO A REGISTER  
 BIT 'B'.

[ ] MEANS "THE INTEGER PART OF THE QUOTIENT"

REM() MEANS "THE REMAINDER OF"

REGISTER	DIAG FUNC	EBUS BIT	FORMULA FOR:
ADR BRK	153-REM(B/4)	4*	[B/4]+3
PC	DITTO	4*	[B/4]+1
VMA	157-REM(B/4)	4*	[B/4]+3
VMA HELD	DITTO	4*	[B/4]+1

BETTER YET--SEE THE PRINTS!

153	13	VMA1	M8523	VMA 18-31=0 H
157	13	VMA1	M8523	VMA AC REP H
157	15	VMA3	M8523	VMA MATCH 13-35 H
*	15X	13-35	VMA3	M8523 ADR BRK 13-35 H **NOTE
*	15X	13-35	VMA4	M8523 VMA HELD 13-35 H **NOTE
*	15X	13-35	VMA2	M8523 VMA 13-35 H **NOTE
*	15X	13-35	VMA3	M8523 PC 13-35 H **NOTE
160	15	MBZ1	M8537	CORE BUSY H
160	16	MBZ4	M8537	CHAN PAR ERR L
160	17	SHD1	M8537	SH AR PAR ODD A H
160	18	MBZ5	M8537	MB PAR BIT IN H
160	19	MBZ1	M8537	CSH EN CSH DATA L
160	20	MBZ1	M8537	MB IN SEL 1 H
160	21	MBZ3	M8537	NXM ACKN H
160	22	MBZ1	M8537	MBZ1 CHAN CORE BUSY H
160	23	MBZ3	M8537	NXM ANY L
160	24	MBZ4	M8537	MBZ4 NXM T6,7 L
160	25	MBZ3	M8537	CHAN NXM ERR L
160	26	PAG5	M8537	PAG MB 18-35 PAR H
160	27	MBC5	M8531	FORCE VALID MATCH 0 H

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KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH	
160	28	MBC5 M8531	FORCE VALID MATCH 1 H	
160	29	MBC5 M8531	FORCE VALID MATCH 2 H	
160	30	MBC5 M8531	FORCE VALID MATCH 3 H	
160	31	MBC1 M8531	WRITE OK H	
160	32	MBC2 M8531	MBC2 CSH ADR WR PULSE H	
160	33	MBC2 M8531	CSH DATA CLR DONE IN L	
161	15	MBZ4 M8537	MBOX ADR PAR ERR L	
161	16	MBZ5 M8537	CBUS PAR LEFT TE H	
161	17	MEM5 M8537	MEM PAR IN H	
161	18	MBZ6 M8537	MBZ6 CSH PAR BIT H	
161	19	MBZ1 M8537	MEM TO C DIAG EN L	
161	20	MBZ1 M8537	MB IN SEL 2 H	
161	21	MBZ1 M8537	MBZ1 RD-PSE-WR REF L	
161	22	MBZ3 M8537	MBOX NXM ERR L	
161	23	MBZ3 M8537	MBZ3 CHAN MEM REF L	
161	24	MBZ4 M8537	MBOX SBUS ERR L	
161	25	MBZ3 M8537	NXM DATA VAL L	
161	26	MBZ6 M8537	CSH PAR BIT A H	
161	27	MBC2 M8531	CSH DATA CLR T1 L	
161	28	MBC2 M8531	CSH DATA CLR T2 L	
161	29	MBC2 M8531	CSH DATA CLR T3 L	
161	30	MBC2 M8531	CSH SEL LRU H	
161	31	MBC2 M8531	MBC2 CSH VAL WR PULSE H	
161	32	MBC2 M8531	MBC2 CSH WR WR PULSE H	
161	33	MBC2 M8531	RQ HOLD PF H	
162	15	MBZ4 M8537	CHAN ADR PAR ERR L	
162	16	MBZ5 M8537	CBUS PAR RIGHT TE H	
162	17	MBZ5 M8537	CSH PAR BIT IN H	
162	18	MBZ3 M8537	MBZ3 SEQUENTIAL RQ H	
162	19	MBZ1 M8537	CHAN READ L	
162	20	MBZ1 M8537	MB IN SEL 4 H	
162	21	MBZ1 M8537	MEM BUSY H	
162	22	MBZ3 M8537	MBZ3 HOLD ERA L	
162	23	MBZ4 M8537	MBZ4 NXM T2 H	
162	24	MBZ4 M8537	MBOX MB PAR ERR L	
162	25	PAG5 M8537	PAG MB 00-17 PAR H	
162	26	MBZ6 M8537	CSH PAR BIT B H	
162	27	MBC2 M8531	MBC2 CACHE WR 00 A H	
162	28	MBC2 M8531	MBC2 CACHE WR 09 A H	
162	29	MBC2 M8531	MBC2 CACHE WR 18 A H	
162	30	MBC2 M8531	MBC2 CACHE WR 27 A H	
162	31	MBC2 M8531	SBUS ADR HOLD H	
162	32	MBC3 M8531	A CHANGE COMING A L	
162	33	MBC3 M8531	MBC3 ANY SBUS RQ IN L	
163	27	MBC3 M8531	MBC3 B CHANGE COMING L	
163	28	MBC5 M8531	CORE BUSY B H	
163	29	MBC3 M8531	CSH VAL SEL ALL H	
163	30	MBC3 M8531	CSH VAL WR DATA H	
163	31	MBC3 M8531	CSH WR SEL ALL H	
163	32	MBC3 M8531	CSH WR WR DATA H	
163	33	MBC3 M8531	DATA VALID A OUT H	
164	27	MBC3 M8531	DATA VALID B OUT H	
164	28	MBC3 M8531	MBC INH 1ST MB REQ H	
164	29	MBC3 M8531	MEM TO C EN L	
164	30	MBC3 M8531	PHASE CHANGE COMING L	
164	31	MBC4 M8531	ACKN PULSE L	
164	32	MBC4 M8531	CORE ADR 34 H	
164	33	MBC4 M8531	CORE ADR 35 H	
165	27	MBC1 M8531	CAM SEL 1 H	
165	28	MBC1 M8531	CAM SEL 2 H	
165	29	MBC4 M8531	CORE DATA VALID -1 L	
165	30	MBC4 M8531	MBC4 CORE DATA VALID -2 L	
165	31	MBC4 M8531	CORE DATA VALID L	
165	32	MBC4 M8531	MBC4 CORE RD IN PROG H	
165	33	MBC4 M8531	MEM ADR PAR H	
166	27	MBC4 M8531	MEM RD RQ B H	
166	28	MBC4 M8531	MEM RQ 0 H	
166	29	MBC4 M8531	MEM RQ 1 H	
166	30	MBC4 M8531	MEM RQ 2 H	
166	31	MBC4 M8531	MEM RQ 3 H	
166	32	MBC4 M8531	MEM START L	
166	33	MBC4 M8531	MEM WR RQ L	
167	00-08	MBZ2 M8537	EBUS REG 00-08 H	
*	167	14-26	MBZ2 M8537	EBUS REG 14-26 H
*	167	27-33	MBC1 M8531	EBUS REG 27-33 H
*	167	34,35	MBZ2 M8537	EBUS REG 34,35 H
**	170	00	CRC6 M8535	CRC CH BUP ADR 0 H
	170	01	CRC4 M8535	CRC4 RESET IN L
	170	02	CRC4 M8535	CRC MEM STORE ENA L
	170	03	CRC4 M8535	CRC4 DONE IN H

KL10 (PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH	
170	04	CRC4 M8535	CRC4 STORE IN H	
170	05	CCW4 M8534	CCW WD READY H	
170	06	CCW6 M8534	CCW CCWF REQ ENA H	
170	07	CCW6 M8534	CCW MEM STORE ENA H	
170	08	CCW5 M8534	CCW ACT FLAG REQ ENA H	
170	09	CCW3 M8534	CCW ALU C8 OUT H	
170	10	CCW3 M8534	CCW ALU C2 OUT H	
170	11	CHC1 M8533	CH T0 H	
170	12	CHC5 M8533	CBUS SEL 0 E H	
170	13	CHC1 M8533	CHX RESET H	
170	14	CHC2 M8533	CH RESET INTR H	
170	16	CCL5 M8536	CCL ODD WC PAR H	
170	18	CCL5 M8536	CCL5 WC GE4 H	
170	19	CCL5 M8536	CCL WC=0 L	
170	20	CHX2 M8515	CSH 0 ANY VAL L	
170	21	CHX3 M8515	CSH USE IN 0 H	
170	22	CSH5 M8513	CSH5 PAGE REFILL COMP L	
170	23	CSH6 M8513	CACHE WR IN H	
170	24	CSH6 M8513	MBOX PT DIR WR L	
170	25	CSH2 M8513	CSH2 WR TEST L	
170	26	CSH3 M8513	ANY VAL HOLD H	
170	27	CSH4 M8513	CSH DATA CLR DONE L	
170	28	CSH4 M8513	CSH REFILL RAM WR L	
170	29	CSH4 M8513	CSH EBOX T3 L	
170	30	MBX1 M8529	CACHE BIT H	
170	31	MBX1 M8529	CCA REQ L	
170	32	MBX4 M8529	CSH WR WD 2 EN H	
170	33	MBX5 M8529	MB REQ IN H	
170	34	MBX5 M8529	MBX MEM TO C EN L	
170	35	MBX5 M8529	RQ 1 IN H	
**	171	00	CRC6 M8535	CRC CH BUF ADR 1 H
171	01	CRC4 M8535	CRC RH20 ERR IN H	
171	02	CRC4 M8535	CRC OVN ERR IN H	
171	03	CRC4 M8535	CRC SHORT WC ERR H	
171	04	CRC4 M8535	CRC LONG WC ERR H	
171	05	CCW4 M8534	CCW WD0 REQ H	
171	06	CCW4 M8534	CCW WD1 REQ H	
171	07	CCW4 M8534	CCW WD2 REQ H	
171	08	CCW4 M8534	CCW WD3 REQ H	
171	09	CCW1 M8534	CCW MEM ADR=0 H	
171	10	CCW6 M8534	CCW CCWF WAITING H	
171	11	CHC1 M8533	CH T1 H	
171	12	CHC5 M8533	CBUS SEL 1 E H	
171	13	CHC1 M8533	CHX START H	
171	14	CHC2 M8533	CH START INTR H	
171	16	CCL3 M8536	CCL3 MB RIP A H	
171	18	CCL3 M8536	CCL ALU MINUS L	
171	19	CCL4 M8536	CCL CH TEST MB PAR L	
171	20	CHX2 M8515	CSH 1 ANY VAL L	
171	21	CHX3 M8515	CSH USE IN 1 H	
171	22	CSH5 M8513	CHAN RD T5 L	
171	23	CSH6 M8513	CSH6 WR DATA RDY L	
171	24	CSH4 M8513	PAGE FAIL T2 L	
171	25	CSH6 M8513	CSH EBOX LOAD REG H	
171	26	CSH7 M8513	CSH FILL CACHE RD L	
171	27	CSH5 M8513	CSH5 CHAN WR T5 L	
171	28	CSH3 M8513	MB WR RQ CLR NXT L	
171	29	CSH4 M8513	CSH4 EBOX T1 L	
171	30	MBX2 M8529	CACHE TO MB 34 H	
171	31	MBX1 M8529	CCA SEL 1 H	
171	32	MBX4 M8529	CSH WR WD 3 EN H	
171	33	MBX2 M8529	MB SEL 1 H	
171	34	MBX3 M8529	MEM DIAG L	
171	35	MBX5 M8529	RQ 2 IN H	
**	172	00	CRC6 M8535	CRC CH BUF ADR 2 H
172	01	CRC3 M8535	CRC READY IN H	
172	02	CRC3 M8535	CRC LAST WORD IN H	
172	03	CRC3 M8535	CRC ERR IN H	
172	04	CRC3 M8535	CRC REVERSE IN H	
172	05	CCW3 M8534	CCW ACT CTR 0 EN H	
172	06	CCW3 M8534	CCW ACT CTR 1 EN H	
172	07	CCW3 M8534	CCW ACT CTR 2 EN H	
172	08	CCW1 M8534	CCW BUF ADR 0 L	
172	09	CCW1 M8534	CCW BUF ADR 1 L	
172	10	CCW1 M8534	CCW BUF ADR 2 L	
172	11	CHC1 M8533	CH T2 H	
172	12	CHC5 M8533	CBUS SEL 2 E H	
172	13	CHC1 M8533	CHX DONE H	
172	14	CHC2 M8533	CH DONE INTR H	
172	16	CCL3 M8536	CCL3 CCWF T2 H	

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KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
172	18	CCL3	M8536	CCL3 MB REQ T2 H
172	19	CCL4	M8536	CCL4 REVERSE H
172	20	CHX2	M8515	CSH 2 ANY VAL L
172	21	CHX3	M8515	CSH USE IN 2 H
172	22	CSH6	M8513	CHAN WR CACHE L
172	23	CSH6	M8513	CCA CYC DONE L
172	24	CSH5	M8513	CHAN T4 L
172	25	CHX3	M8513	CSH LRU 2 H
172	26	CSH1	M8513	CSH1 READY TO GO A H
172	27	CSH6	M8513	CSH USE HOLD H
172	28	CSH1	M8513	CSH CCA CYC L
172	29	CSH2	M8513	CSH2 EBOX REQ EN L
172	30	MBX2	M8529	CACHE TO MB 35 H
172	31	MBX1	M8529	CCA SEL 2 H
172	32	MBX1	M8529	FORCE NO MATCH H
172	33	MBX2	M8529	MB SEL 2 H
172	34	MBX5	M8529	MEM RD RQ IN H
172	35	MBX5	M8529	RQ 3 IN H
**	173	00	CRC6	M8535 CRC CH BUF ADR 3 H
173	01	CRC2	M8535	CRC2 ACT CTR 0R H
173	02	CRC2	M8535	CRC2 ACT CTR 1R H
173	03	CRC2	M8535	CRC2 ACT CTR 2R H
173	04	CRC2	M8535	CRC2 RAM CYC H
**	173	05	CCW2	M8534 CCW CHA 30 H
**	173	06	CCW2	M8534 CCW CHA 31 H
**	173	07	CCW2	M8534 CCW CHA 32 H
**	173	08	CCW2	M8534 CCW CHA 33 H
**	173	09	CCW2	M8534 CCW CHA 34 H
**	173	10	CCW2	M8534 CCW CHA 35 H
173	11	CHC1	M8533	CH T3 H
173	12	CHC5	M8533	CBUS SEL 3 E H
173	13	CHC1	M8533	CHX STORE H
173	14	CHC2	M8533	CH STORE H
173	16	CCL4	M8536	CCL CH MB SEL 2 H
173	18	CCL4	M8536	CCL CH MB SEL 1 H
173	19	CCL3	M8536	CCL AF T2 L
173	20	CHX2	M8515	CSH 3 ANY VAL L
173	21	CHX3	M8515	CSH USE IN 3 H
173	22	CSH2	M8513	CSH2 ONE WORD RD A L
173	23	CSH2	M8513	CSH2 MBOX RESP L
173	24	CSH2	M8513	CSH2 RD PSE 2ND REQ EN L
173	25	CHX3	M8513	CSH LRU 1 H
173	26	CSH5	M8513	CSH5 T1 L
173	27	CSH4	M8513	CSH4 WRITEBACK T1 A H
173	28	CSH7	M8513	CSH CCA WRITEBACK L
173	29	CSH4	M8513	CSH4 EBOX T2 L
173	30	MBX4	M8529	MBX4 CACHE TO MB DONE H
173	31	MBX2	M8529	CHAN WR CYC L
173	32	MBX3	M8529	MEM DATA TO MEM H
173	33	MBX2	M8529	MB SEL HOLD H
173	34	MBX3	M8529	MEM TO C SEL 1 H
173	35	MBX2	M8529	SBUS ADR 34 H
**	174	00	CRC6	M8535 CRC CH BUF ADR 4 H
174	01	CRC1	M8535	CRC1 ACT FLAG ENA H
174	02	CRC5	M8535	CRC WR RAM L
174	03	CRC3	M8535	CRC3 OP CODE 00 H
174	04	CRC3	M8535	CRC3 OP CODE 01 H
*	174	05-10	CCW2	M8534 CCW CHA 24-29 H
174	11	CHC1	M8533	CBUS READY E H
174	12	CHC5	M8533	CBUS SEL 4 E H
174	13	CHC1	M8533	CHX CTOM H
174	14	CHC3	M8533	CH CTOM H
174	16	CCL3	M8536	CCL CHAN REQ H
174	18	CCL3	M8536	CCL CHAN EPT H
174	19	CCL4	M8536	CCL CHAN TO MEM H
174	20	CHX4	M8515	CSH DIR 0 PAR ODD H
174	21	CHX3	M8515	CSH USE IN 4 H
174	22	CSH2	M8513	CSH2 E CORE RD RQ A L
174	23	CSH6	M8513	PAGE FAIL HOLD L
174	24	CSH5	M8513	CSH5 PAGE REFILL T9,12 L
174	25	CHA3	M8513	CSH 3 ANY WR L
174	26	CSH5	M8513	CSH TO L
174	27	CSH3	M8513	CSH ADR PMA EN H
174	28	CSH1	M8513	CSH1 EBOX CYC B L
174	29	CSH1	M8513	CSH1 CACHE IDLE L
174	30	MBX4	M8529	CACHE TO MB T2 L
174	31	MBX1	M8529	CSH CCA INVAL CSH H
174	32	MBX3	M8529	MB DATA CODE 1 H
174	33	MBX6	M8529	MB0 HOLD IN H
174	34	MBX3	M8529	MEM TO C SEL 2 H
174	35	MBX2	M8529	SBUS ADR 35 H

COMPANY CONFIDENTIAL

K110(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
**	175	00	CRC6 M8535 CRC CH BUF ADR 5 H
	175	01	CRC6 M8535 CRC SEL 1D L
	175	02	CRC6 M8535 CRC SEL 2D L
	175	03	CRC6 M8535 CRC SEL 4D L
	175	04	CRC1 M8535 CRC1 AF REQ ENA L
*	175	05-10	CCW2 M8534 CCW CHA 18-23 H
	175	11	CHC1 M8533 CBUS LAST WORD E H
	175	12	CHC5 M8533 CBUS SEL 5 E H
	175	13	CHC5 M8533 CH SEL 8A H
	175	14	CHC2 M8533 CH CONTR REQ H
	175	16	CCL2 M8536 CCL CCWF REQ H
	175	18	CCL2 M8536 CCL2 ACT FLAG REQ H
	175	19	CCL2 M8536 CCL MEM STORE REQ H
	175	20	CHX4 M8515 CSH DIR 1 PAR ODD H
	175	21	CHX3 M8515 CSH USE ADR 2 H
	175	22	CSH2 M8513 CSH EBOX RETRY REQ L
	175	23	CSH6 M8513 CSH USE WR EN H
	175	24	CSH3 M8513 MB TEST PAR A IN L
	175	25	CHA3 M8513 CSH 1 ANY WR L
	175	26	CSH5 M8513 CSH5 T3 L
	175	27	CSH3 M8513 MBOX GATE VMA 27-33 H
	175	28	CSH1 M8513 CSH MB CYC L
	175	29	CSH4 M8513 ONE WORD WR TO L
	175	30	MBX4 M8529 MBX4 CACHE TO MB T3 L
	175	31	MBX1 M8529 CSH CCA VAL CORE H
	175	32	MBX3 M8529 MB DATA CODE 2 H
	175	33	MBX6 M8529 MB1 HOLD IN H
	175	34	MBX5 M8529 MEM WR RQ IN H
	175	35	MBX3 M8529 SBUS DIAG 3 L
**	176	00	CRC6 M8535 CRC CH BUF ADR 6 H
	176	01	CRC1 M8535 CRC1 MEM PTR0 H
	176	02	CRC1 M8535 CRC1 MEM PTR1 H
	176	03	CRC1 M8535 CRC1 MEM PTR2 H
	176	04	CRC1 M8535 CRC1 MEM PTR3 H
	176	05	CCW3 M8534 CCL WC=3 H
	176	06	CCW4 M8534 CCL CCW REG LOAD H
*	176	07-10	CCW2 M8534 CCW CHA 14-17 H
	176	11	CHC1 M8533 CBUS ERROR E H
	176	12	CHC5 M8533 CBUS SEL 6 E H
	176	13	CHC1 M8533 CH MB REQ INH H
	176	14	CHC1 M8533 CH REVERSE H
	176	16	CCL4 M8536 CCL4 STORE CCW H
	176	18	CCL2 M8536 CCL BUF ADR 3 H
	176	19	CCL4 M8536 CCL START MEM L
	176	20	CHX4 M8515 CSH DIR 2 PAR ODD H
	176	21	CHX3 M8515 CSH USE ADR 3 H
	176	22	CSH6 M8513 CCA INVAL T4 L
	176	23	CSH5 M8513 PAGE REFILL T8 L
	176	24	CSH4 M8513 CSH4 EBOX TO L
	176	25	CHA3 M8513 CSH 2 ANY WR L
	176	26	CSH5 M8513 CSH T2 L
	176	27	CSH2 M8513 E CACHE WR CYC H
	176	28	CSH7 M8513 CSH E WRITEBACK L
	176	29	CSH5 M8513 PAGE REFILL T4 L
	176	30	MBX4 M8529 CACHE TO MB T4 A L
	176	31	MBX4 M8529 CSH WR WD 0 EN H
	176	32	MBX3 M8529 MB PAR H
	176	33	MBX6 M8529 MB2 HOLD IN H
	176	34	MBX3 M8529 REFILL HOLD H
	176	35	MBX3 M8529 MBX3 SBUS DIAG CYC L
	177	00	CRC1 M8535 CRC1 PTR DIF=0 H
	177	01	CRC6 M8535 CRC6 CH ADR 0C L
	177	02	CRC6 M8535 CRC6 CH ADR 1C L
	177	03	CRC6 M8535 CRC6 CH ADR 2C L
	177	04	CRC6 M8535 CRC6 CH ADR 3C L
	177	05	CCW6 M8534 CCW RAM ADR 1 H
	177	06	CCW6 M8534 CCW RAM ADR 2 H
	177	07	CCW6 M8534 CCW RAM ADR 4 H
	177	08	CCW3 M8534 CCL WC=1 H
	177	09	CCW3 M8534 CCL WC=2 H
	177	10	CCW4 M8534 CCW ODD ADR PAR H
	177	11	CHC1 M8533 CH CBUS REQ H
	177	12	CHC5 M8533 CBUS SEL 7 E H
	177	13	CHC2 M8533 CH CONTR CYC H
	177	14	CHC2 M8533 CH START H
	177	16	CCL1 M8536 CCL1 ERR REQ H
	177	18	CCL6 M8536 CCL6 CSH CHAN CYC L
	177	19	CCL3 M8536 CCL3 MEM PTR EN H
	177	20	CHX4 M8515 CSH DIR 3 PAR ODD H
	177	21	CHX3 M8515 CSH USE ADR 4 H

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KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
177	22	CSH6	M8513	PAGE REFILL ERROR L
177	23	CSH6	M8513	CSH6 DATA DLY 1 L
177	24	CSH4	M8513	CSH4 PAGE FAIL DLY H
177	25	CHA3	M8513	CSH 0 ANY WR L
177	26	CSH5	M8513	CSH5 PAGE REFILL T10 L
177	28	CSH2	M8513	RD PAUSE 2ND HALF L
177	29	CSH4	M8513	CSH4 EBOX WR T4 L
177	30	MBX1	M8529	CCA ALL PAGES CYC H
177	31	MBX4	M8529	CSH WR WD 1 EN H
177	32	MBX2	M8529	MB REQ HOLD H
177	33	MBX6	M8529	MB3 HOLD IN H
177	34	MBX5	M8529	RQ 0 IN H
177	35	MBX4	M8529	WRITEBACK T2 L

NOTE

TRACON and the 11-based 10 diagnostic programs interpret all diagnostic read functions which are not preceded with either a single or double asterisk [(\*) or (\*\*)] as single bits; as such, they are printed out by bit position and/or name. Diagnostic read functions preceded by a single asterisk (\*) are interpreted as registers and are printed out as such. Diagnostic read functions which are preceded by a double asterisk (\*\*) may be interpreted and printed as either single bits or as a register depending on the program doing the interpretation.



KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED ALPHABETICALLY

DF	BIT	DRAWING	BOARD	NAME AND TRUTH	
162	32	MBC2	M8531	A CHANGE COMING A L	
164	31	MBC4	M8531	ACKN PULSE L	
127	0-35	EDP3	M8512	AD 0 TO 35 H	
136	17	IRD4	M8522	AD CRY -02 A H	
132	06	IRD4	M8524	AD CRY -02 A L	
131	05	EDP3	M8524	AD CRY 01 L	
137	12	IRD4	M8522	AD CRY 12 H	
137	13	IRD4	M8522	AD CRY 18 H	
137	14	IRD4	M8522	AD CRY 24 H	
137	15	IRD4	M8522	AD CRY 36 H	
132	05	EDP3	M8524	AD OVERFLOW 00 L	
136	12	IRD3	M8522	AD=0 L	
15X	13-35	VMA3	M8523	ADR BRK 13-35 H **NOTE	
126	0-35	EDP3	M8512	ADX 0 TO 35 H	
137	16	IRD4	M8522	ADX CRY 12 H	
137	17	IRD4	M8522	ADX CRY 24 H	
170	26	CSH3	M8513	ANY VAL HOLD H	
116	11	APR2	M8539	APR ANY EBOX ERR FLG H	
110	14	APR2	M8539	APR APR INTERRUPT H	
112	10	APR2	M8539	APR C DIR P ERR EN IN H	
110	10	APR2	M8539	APR C DIR P ERR IN H	
111	08	APR5	M8539	APR CURRENT BLOCK 1 H	
111	07	APR5	M8539	APR CURRENT BLOCK 2 H	
111	06	APR5	M8539	APR CURRENT BLOCK 4 H	
111	12	APR3	M8539	APR CWSX H	
115	12	APR6	M8539	APR EBOX CCA H	
115	10	APR3	M8539	APR EBOX DISABLE CS H	
117	12	APR6	M8539	APR EBOX EBR H	
115	13	APR6	M8539	APR EBOX ERA H	
115	16	APR6	M8539	APR EBOX LOAD REG L	
115	17	APR6	M8539	APR EBOX READ REG L	
115	14	APR6	M8539	APR EBOX SBUS DIAG H	
117	10	APR3	M8539	APR EBOX SEND F02 H	
117	13	APR6	M8539	APR EBOX SPARE H	
116	12	APR6	M8539	APR EBOX UBR H	
117	09	APR3	M8539	APR EBUS DEMAND H	
116	10	APR3	M8539	APR EBUS F01 E H	
116	09	APR3	M8539	APR EBUS REQ L	
115	09	APR3	M8539	APR EBUS RETURN H	
116	13	APR6	M8539	APR EN REFILL RAM WR H	
114	15	APR4	M8539	APR F02 EN H	
113	09	APR3	M8539	APR FETCH COMP H	
114	16	APR3	M8539	APR FM 36 H	
**	114	14	APR4	M8539	APR FM ADR 1 H
**	114	11	APR4	M8539	APR FM ADR 10 H
**	114	13	APR4	M8539	APR FM ADR 2 H
**	114	12	APR4	M8539	APR FM ADR 4 H
**	114	10	APR5	M8539	APR FM BLOCK 1 H
**	114	09	APR5	M8539	APR FM BLOCK 2 H
**	114	08	APR5	M8539	APR FM BLOCK 4 H
**	114	17	APR3	M8539	APR FM ODD PARITY H
112	08	APR1	M8539	APR I/O PF ERR EN IN H	
110	08	APR1	M8539	APR I/O PF ERR IN H	
112	09	APR1	M8539	APR MB PAR ERR EN IN H	
110	09	APR1	M8539	APR MB PAR ERR IN H	
114	07	APR5	M8539	APR MBOX CTL 03 H	
115	07	APR5	M8539	APR MBOX CTL 06 H	
112	07	APR1	M8539	APR NXM ERR EN IN H	
110	07	APR1	M8539	APR NXM ERR IN H	
111	11	APR5	M8539	APR PREV BLOCK 1 H	
111	10	APR5	M8539	APR PREV BLOCK 2 H	
111	09	APR5	M8539	APR PREV BLOCK 4 H	
111	13	APR3	M8539	APR PREV SEC 13 H	
111	14	APR3	M8539	APR PREV SEC 14 H	
111	15	APR3	M8539	APR PREV SEC 15 H	
111	16	APR3	M8539	APR PREV SEC 16 H	
111	17	APR3	M8539	APR PREV SEC 17 H	
116	08	APR5	M8539	APR PT DIR WR L	
117	08	APR5	M8539	APR PT WR L	
112	12	APR2	M8539	APR PWR FAIL EN IN H	
110	12	APR2	M8539	APR PWR FAIL IN H	
113	10	APR3	M8539	APR READ COMP H	
112	11	APR2	M8539	APR S ADR P ERR EN IN H	
110	11	APR2	M8539	APR S ADR P ERR IN H	
112	06	APR1	M8539	APR SBUS ERR EN IN H	
110	06	APR1	M8539	APR SBUS ERR IN H	
115	08	APR5	M8539	APR SET PAGE FAIL L	
110	01	APR2	M8539	APR SWEEP BUSY EN H	
112	13	APR2	M8539	APR SWEEP DONE EN IN H	

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KL10 (PA) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
110	13	APR2	M8539	APR SWEEP DONE IN H
113	12	APR3	M8539	APR USER COMP H
115	11	APR2	M8539	APR WR BAD ADR PAR L
116	07	APR5	M8539	APR WR PT SEL 0 H
117	07	APR5	M8539	APR WR PT SEL 1 H
113	11	APR3	M8539	APR WRITE COMP H
*	120	12-35	EDP1	M8512 AR 12 TO 35 H
	102	23	MCL5	M8530 ARMM 12 H
*	125	0-35	EDP2	M8512 ARX 0 TO 35 H
*	121	0-35	EDP4	M8512 BR 0 TO 35 H
*	124	0-35	EDP4	M8512 BRX 0 TO 35 H
	170	30	MBX1	M8529 CACHE BIT H
	171	30	MBX2	M8529 CACHE TO MB 34 H
	172	30	MBX2	M8529 CACHE TO MB 35 H
	174	30	MBX4	M8529 CACHE TO MB T2 L
	176	30	MBX4	M8529 CACHE TO MB T4 A L
	170	23	CSH6	M8513 CACHE WR IN H
	165	27	MBC1	M8531 CAM SEL 1 H
	165	28	MBC1	M8531 CAM SEL 2 H
	176	11	CHC1	M8533 CBUS ERROR E H
	175	11	CHC1	M8533 CBUS LAST WORD E H
	161	16	MBZ5	M8537 CBUS PAR LEFT TE H
	162	16	MBZ5	M8537 CBUS PAR RIGHT TE H
	174	11	CHC1	M8533 CBUS READY E H
	170	12	CHC5	M8533 CBUS SEL 0 E H
	171	12	CHC5	M8533 CBUS SEL 1 E H
	172	12	CHC5	M8533 CBUS SEL 2 E H
	173	12	CHC5	M8533 CBUS SEL 3 E H
	174	12	CHC5	M8533 CBUS SEL 4 E H
	175	12	CHC5	M8533 CBUS SEL 5 E H
	176	12	CHC5	M8533 CBUS SEL 6 E H
	177	12	CHC5	M8533 CBUS SEL 7 E H
	177	30	MBX1	M8529 CCA ALL PAGES CYC H
	172	23	CSH6	M8513 CCA CYC DONE L
	176	22	CSH6	M8513 CCA INVAL T4 L
	170	31	MBX1	M8529 CCA REQ L
	171	31	MBX1	M8529 CCA SEL 1 H
	172	31	MBX1	M8529 CCA SEL 2 H
	173	19	CCL3	M8536 CCL AP T2 L
	171	18	CCL3	M8536 CCL ALU MINUS L
	176	18	CCL2	M8536 CCL BUF ADR 3 H
	176	06	CCW4	M8534 CCL CCW REG LOAD H
	175	16	CCL2	M8536 CCL CCWF REQ H
	173	18	CCL4	M8536 CCL CH MB SEL 1 H
	173	16	CCL4	M8536 CCL CH MB SEL 2 H
	171	19	CCL4	M8536 CCL CH TEST MB PAR L
	174	18	CCL3	M8536 CCL CHAN EPT H
	174	16	CCL3	M8536 CCL CHAN REQ H
	174	19	CCL4	M8536 CCL CHAN TO MEM H
	175	19	CCL2	M8536 CCL MEM STORE REQ H
	170	16	CCL5	M8536 CCL ODD WC PAR H
	176	19	CCL4	M8536 CCL START MEM L
	170	19	CCL5	M8536 CCL WC=0 L
	177	08	CCW3	M8534 CCL WC=1 H
	177	09	CCW3	M8534 CCL WC=2 H
	176	05	CCW3	M8534 CCL WC=3 H
	177	16	CCL1	M8536 CCL1 ERR REQ H
	175	18	CCL2	M8536 CCL2 ACT FLAG REQ H
	172	16	CCL3	M8536 CCL3 CCWF T2 H
	172	18	CCL3	M8536 CCL3 MB REQ T2 H
	171	16	CCL3	M8536 CCL3 MB RIP A H
	177	19	CCL3	M8536 CCL3 MEM PTR EN H
	172	19	CCL4	M8536 CCL4 REVERSE H
	176	16	CCL4	M8536 CCL4 STORE CCW H
	170	18	CCL5	M8536 CCL5 WC GE4 H
	177	18	CCL6	M8536 CCL6 CSH CHAN CYC L
	172	05	CCW3	M8534 CCW ACT CTR 0 EN H
	172	06	CCW3	M8534 CCW ACT CTR 1 EN H
	172	07	CCW3	M8534 CCW ACT CTR 2 EN H
	170	08	CCW5	M8534 CCW ACT FLAG REQ ENA H
	170	10	CCW3	M8534 CCW ALU C2 OUT H
	170	09	CCW3	M8534 CCW ALU C8 OUT H
	172	08	CCW1	M8534 CCW BUF ADR 0 L
	172	09	CCW1	M8534 CCW BUF ADR 1 L
	172	10	CCW1	M8534 CCW BUF ADR 2 L
	170	06	CCW6	M8534 CCW CCWF REQ ENA H
	171	10	CCW6	M8534 CCW CCWF WAITING H
*	176	07-10	CCW2	M8534 CCW CHA 14-17 H
*	175	05-10	CCW2	M8534 CCW CHA 18-23 H

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KL10 (PA) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
*	174	05-10	CCW2 M8534 CCW CHA 24-29 H
**	173	05	CCW2 M8534 CCW CHA 30 H
**	173	06	CCW2 M8534 CCW CHA 31 H
**	173	07	CCW2 M8534 CCW CHA 32 H
**	173	08	CCW2 M8534 CCW CHA 33 H
**	173	09	CCW2 M8534 CCW CHA 34 H
**	173	10	CCW2 M8534 CCW CHA 35 H
	171	09	CCW1 M8534 CCW MEM ADR=0 H
	170	07	CCW6 M8534 CCW MEM STORE ENA H
	177	10	CCW4 M8534 CCW ODD ADR PAR H
	177	05	CCW6 M8534 CCW RAM ADR 1 H
	177	06	CCW6 M8534 CCW RAM ADR 2 H
	177	07	CCW6 M8534 CCW RAM ADR 4 H
	170	05	CCW4 M8534 CCW WD READY H
	171	05	CCW4 M8534 CCW WD0 REQ H
	171	06	CCW4 M8534 CCW WD1 REQ H
	171	07	CCW4 M8534 CCW WD2 REQ H
	171	08	CCW4 M8534 CCW WD3 REQ H
	177	11	CHC1 M8533 CH CBUS REQ H
	177	13	CHC2 M8533 CH CONTR CYC H
	175	14	CHC2 M8533 CH CONTR REQ H
	174	14	CHC3 M8533 CH CTOM H
	172	14	CHC2 M8533 CH DONE INTR H
	176	13	CHC1 M8533 CH MB REQ INH H
	170	14	CHC2 M8533 CH RESET INTR H
	176	14	CHC1 M8533 CH REVERSE H
	175	13	CHC5 M8533 CH SEL 8A H
	177	14	CHC2 M8533 CH START H
	171	14	CHC2 M8533 CH START INTR H
	173	14	CHC2 M8533 CH STORE H
	170	11	CHC1 M8533 CH T0 H
	171	11	CHC1 M8533 CH T1 H
	172	11	CHC1 M8533 CH T2 H
	173	11	CHC1 M8533 CH T3 H
	162	15	MB24 M8537 CHAN ADR PAR ERR L
	160	25	MB23 M8537 CHAN NXM ERR L
	160	16	MB24 M8537 CHAN PAR ERR L
	171	22	CSH5 M8513 CHAN RD T5 L
	162	19	MB21 M8537 CHAN READ L
	172	24	CSH5 M8513 CHAN T4 L
	172	22	CSH6 M8513 CHAN WR CACHE L
	173	31	MBX2 M8529 CHAN WR CYC L
	174	13	CHC1 M8533 CHX CTOM H
	172	13	CHC1 M8533 CHX DONE H
	170	13	CHC1 M8533 CHX RESET H
	171	13	CHC1 M8533 CHX START H
	173	13	CHC1 M8533 CHX STORE H
	103	35	CLK4 M8526 CLK 1777 EN H
**	106	35	CLK5 M8526 CLK AR/ARX PAR CHECK L
**	101	35	CLK5 M8526 CLK BURST 01 H
**	101	34	CLK5 M8526 CLK BURST 02 H
**	101	33	CLK5 M8526 CLK BURST 04 H
**	101	32	CLK5 M8526 CLK BURST 08 H
**	100	34	CLK5 M8526 CLK BURST 128 H
**	101	31	CLK5 M8526 CLK BURST 16 H
**	101	30	CLK5 M8526 CLK BURST 32 H
**	100	35	CLK5 M8526 CLK BURST 64 H
	100	33	CLK5 M8526 CLK BURST CNT=0 H
	103	31	CLK2 M8526 CLK BURST L
	105	34	CLK5 M8526 CLK CRAM PAR CHECK L
	104	30	CLK3 M8526 CLK CRAM PAR ERR H
	106	34	CLK5 M8526 CLK DRAM PAR CHECK L
	103	30	CLK3 M8526 CLK DRAM PAR ERR H
	103	33	CLK4 M8526 CLK EBOX CLK L
	105	33	CLK5 M8526 CLK EBOX CRM DIS H
	107	33	CLK5 M8526 CLK EBOX CTL DIS H
	106	33	CLK5 M8526 CLK EBOX BDP DIS H
	102	32	CLK4 M8526 CLK EBOX REQ H
	104	33	CLK3 M8526 CLK EBOX SOURCE H
	104	31	CLK2 M8526 CLK EBOX SS L
	100	30	CLK1 M8526 CLK EBUS CLK H
	107	35	CLK5 M8526 CLK ERR STOP EN L
	107	30	CLK3 M8526 CLK ERROR L
	102	30	CLK1 M8526 CLK ERROR STOP H
	104	34	CLK5 M8526 CLK FM PAR CHECK L
	105	30	CLK3 M8526 CLK FM PAR ERR H
	102	35	CLK4 M8526 CLK FORCE 1777 H
	107	34	CLK5 M8526 CLK FS CHECK L
	106	30	CLK3 M8526 CLK FS ERROR H

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KL10 (PA) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
102	31	CLK2	M8526	CLK GO L
103	34	CLK4	M8526	CLK INSTR 1777 H
103	32	CLK4	M8526	CLK MB XFER H
104	35	CLK5	M8526	CLK MBOX CYCLE DIS H
105	35	CLK5	M8526	CLK MBOX RESP SIM L
102	34	CLK4	M8526	CLK PAGE FAIL EN L
107	31	CLK4	M8526	CLK PAGE FAIL H
107	32	CLK5	M8526	CLK RATE SEL 1 H
106	32	CLK5	M8526	CLK RATE SEL 2 H
100	31	CLK1	M8526	CLK SBUS CLK H
105	32	CLK5	M8526	CLK SOURCE SEL 1 H
104	32	CLK5	M8526	CLK SOURCE SEL 2 H
102	33	CLK3	M8526	CLK SYNC H
136	18	CON4	M8525	CON AR 36 H
137	18	CON4	M8525	CON ARX 36 H
133	23	CON4	M8525	CON ARX LOADED L
131	19	CON3	M8525	CON CACHE LOAD EN H
133	05	CON2	M8524	CON CLR PRIVATE INSTR H
137	22	CON2	M8525	CON COND ADR 10 H
132	18	CON1	M8525	CON COND EN 00-07 L
133	22	CON2	M8525	CON COND INSTR ABORT H
134	19	CON1	M8525	CON COND/LOAD VMA HELD H
132	20	CON1	M8525	CON COND/MBOX CTL L
132	19	CON1	M8525	CON COND/SEL VMA L
133	19	CON1	M8525	CON COND/VMA GETS # H
135	18	CON3	M8525	CON DELAY REQ H
133	20	CON3	M8525	CON EBUS REL H
117	11	CON5	M8539	CON FM WRITE PAR L
134	24	CON5	M8525	CON FM WRITE PAR L
136	24	CON5	M8525	CON FM XFER L
131	21	CON3	M8525	CON KI10 PAGING MODE L
134	22	CON2	M8525	CON LOAD ACCESS COND H
136	22	CON2	M8525	CON LOAD DRAM H
132	22	CON2	M8525	CON LOAD IR L
135	19	CON1	M8525	CON LOAD SPEC INSTR L
135	24	CON5	M8525	CON MBOX WAIT L
135	21	CON2	M8525	CON NICOND 07 H
136	21	CON2	M8525	CON NICOND 08 H
137	21	CON2	M8525	CON NICOND 09 H
134	21	CON2	M8525	CON NICOND TRAP EN H
133	21	CON4	M8525	CON PC+1 INH L
134	04	CON5	M8524	CON PI CYCLE A L
137	24	CON5	M8525	CON PI DISMISS L
133	18	CON1	M8525	CON SKIP EN 40-47 L
134	18	CON1	M8525	CON SKIP EN 50-57 L
134	20	CON3	M8525	CON SR 00 H
135	20	CON3	M8525	CON SR 01 H
136	20	CON3	M8525	CON SR 02 H
137	20	CON3	M8525	CON SR 03 H
131	22	CON3	M8525	CON TRAP EN H
134	23	CON4	M8525	CON UCODE STATE 01 H
135	23	CON4	M8525	CON UCODE STATE 03 H
136	23	CON4	M8525	CON UCODE STATE 05 H
137	23	CON4	M8525	CON UCODE STATE 07 H
137	19	CON1	M8525	CON VMA SEL 1 L
136	19	CON1	M8525	CON VMA SEL 2 L
130	18	CON3	M8525	CON WR EVEN PAR ADR H
135	22	CON2	M8525	CON2 INSTR GO L
131	18	CON3	M8525	CON3 CACHE LOOK EN H
130	19	CON3	M8525	CON3 WR EVEN PAR DATA H
130	20	CON3	M8525	CON3 WR EVEN PAR DIR H
132	23	CON4	M8525	CON4 AR LOADED H
133	24	CON5	M8525	CON5 MEM CYCLE L
132	24	CON5	M8525	CON5 PI CYCLE H
164	32	MBC4	M8531	CORE ADR 34 H
164	33	MBC4	M8531	CORE ADR 35 H
163	28	MBC5	M8531	CORE BUSY B H
160	15	MBZ1	M8537	CORE BUSY H
165	29	MBC4	M8531	CORE DATA VALID -1 L
165	31	MBC4	M8531	CORE DATA VALID L
**	145	01	CRA1	CR ADR 00 F H
**	145	02	CRA1	CR ADR 01 F H
**	145	03	CRA1	CR ADR 02 F H
**	145	04	CRA1	CR ADR 03 F H
**	145	05	CRA1	CR ADR 04 F H
**	144	00	CRA2	CR ADR 05 F H
**	144	01	CRA2	CR ADR 06 F H
**	144	02	CRA2	CR ADR 07 F H
**	144	03	CRA2	CR ADR 08 F H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
**	144	04 CRA2	M8511 CR ADR 09 F H
**	144	05 CRA2	M8511 CR ADR 10 F H
**	141	01 CRA3	M8511 CRA DISP 00 H
**	141	02 CRA3	M8511 CRA DISP 01 H
**	141	03 CRA3	M8511 CRA DISP 02 H
**	141	04 CRA3	M8511 CRA DISP 03 H
**	141	05 CRA3	M8511 CRA DISP 04 H
**	141	00 CRA3	M8511 CRA DISP PARITY H
**	147	01 CRA3	M8511 CRA LOC 00 H
**	147	02 CRA3	M8511 CRA LOC 01 H
**	147	03 CRA3	M8511 CRA LOC 02 H
**	147	04 CRA3	M8511 CRA LOC 03 H
**	147	05 CRA3	M8511 CRA LOC 04 H
**	146	00 CRA3	M8511 CRA LOC 05 H
**	146	01 CRA3	M8511 CRA LOC 06 H
**	146	02 CRA3	M8511 CRA LOC 07 H
**	146	03 CRA3	M8511 CRA LOC 08 H
**	146	04 CRA3	M8511 CRA LOC 09 H
**	146	05 CRA3	M8511 CRA LOC 10 H
*	147	08-11 CRM5	M8528 CRAM 00-03 H
*	147	14-17 CRM5	M8528 CRAM 04-07 H
*	147	20-23 CRM5	M8528 CRAM 08-11 H
*	147	26-29 CRM5	M8528 CRAM 12-15 H
*	147	32-35 CRM5	M8528 CRAM 16-19 H
*	146	08-11 CRM5	M8528 CRAM 20-23 H
*	146	14-17 CRM5	M8528 CRAM 24-27 H
*	146	20-23 CRM5	M8528 CRAM 28-31 H
*	146	26-29 CRM5	M8528 CRAM 32-35 H
*	146	32-35 CRM5	M8528 CRAM 36-39 H
*	145	08-11 CRM5	M8528 CRAM 40-43 H
*	145	14-17 CRM5	M8528 CRAM 44-47 H
*	145	20-23 CRM5	M8528 CRAM 48-51 H
*	145	26-29 CRM5	M8528 CRAM 52-55 H
*	145	32-35 CRM5	M8528 CRAM 56-59 H
**	144	08 CRM5	M8528 CRAM 60 H
**	144	10 CRM5	M8528 CRAM 62 H
**	144	14 CRM5	M8528 CRAM 64 H
**	144	16 CRM5	M8528 CRAM 66 H
**	144	20 CRM5	M8528 CRAM 68 H
**	144	22 CRM5	M8528 CRAM 70 H
**	144	26 CRM5	M8528 CRAM 72 H
**	144	28 CRM5	M8528 CRAM 74 H
**	144	32 CRM5	M8528 CRAM 76 H
**	144	34 CRM5	M8528 CRAM 78 H
**	144	11 CRM5	M8528 CRAM PAR 00 H
**	144	17 CRM5	M8528 CRAM PAR 04 H
**	144	23 CRM5	M8528 CRAM PAR 08 H
**	144	29 CRM5	M8528 CRAM PAR 12 H
**	144	35 CRM5	M8528 CRAM PAR 16 H
**	144	09 CRM5	M8528 CRAM PAR 1ST 00 H
**	144	15 CRM5	M8528 CRAM PAR 1ST 04 H
**	144	21 CRM5	M8528 CRAM PAR 1ST 08 H
**	144	27 CRM5	M8528 CRAM PAR 1ST 12 H
**	144	33 CRM5	M8528 CRAM PAR 1ST 16 H
**	170	00 CRC6	M8535 CRC CH BUF ADR 0 H
**	171	00 CRC6	M8535 CRC CH BUF ADR 1 H
**	172	00 CRC6	M8535 CRC CH BUF ADR 2 H
**	173	00 CRC6	M8535 CRC CH BUF ADR 3 H
**	174	00 CRC6	M8535 CRC CH BUF ADR 4 H
**	175	00 CRC6	M8535 CRC CH BUF ADR 5 H
**	176	00 CRC6	M8535 CRC CH BUF ADR 6 H
	172	03 CRC3	M8535 CRC ERR IN H
	172	02 CRC3	M8535 CRC LAST WORD IN H
	171	04 CRC4	M8535 CRC LONG WC ERR H
	170	02 CRC4	M8535 CRC MEM STORE ENA L
	171	02 CRC4	M8535 CRC OVN ERR IN H
	172	01 CRC3	M8535 CRC READY IN H
	172	04 CRC3	M8535 CRC REVERSE IN H
	171	01 CRC4	M8535 CRC RH20 ERR IN H
	175	01 CRC6	M8535 CRC SEL 1D L
	175	02 CRC6	M8535 CRC SEL 2D L
	175	03 CRC6	M8535 CRC SEL 4D L
	171	03 CRC4	M8535 CRC SHORT WC ERR H
	174	02 CRC5	M8535 CRC WR RAM L
	174	01 CRC1	M8535 CRCL ACT FLAG ENA H
	175	04 CRC1	M8535 CRCL AF REQ ENA L
	176	01 CRC1	M8535 CRCL MEM PTR0 H
	176	02 CRC1	M8535 CRCL MEM PTR1 H
	176	03 CRC1	M8535 CRCL MEM PTR2 H

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KL10(PA) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
176	04	CRC1 M8535	CRC1 MEM PTR3 H
177	00	CRC1 M8535	CRC1 PTR DIF=0 H
173	01	CRC2 M8535	CRC2 ACT CTR 0R H
173	02	CRC2 M8535	CRC2 ACT CTR 1R H
173	03	CRC2 M8535	CRC2 ACT CTR 2R H
173	04	CRC2 M8535	CRC2 RAM CYC H
174	03	CRC3 M8535	CRC3 OP CODE 00 H
174	04	CRC3 M8535	CRC3 OP CODE 01 H
170	03	CRC4 M8535	CRC4 DONE IN H
170	01	CRC4 M8535	CRC4 RESET IN L
170	04	CRC4 M8535	CRC4 STORE IN H
177	01	CRC6 M8535	CRC6 CH ADR 0C L
177	02	CRC6 M8535	CRC6 CH ADR 1C L
177	03	CRC6 M8535	CRC6 CH ADR 2C L
177	04	CRC6 M8535	CRC6 CH ADR 3C L
170	20	CHX2 M8515	CSH 0 ANY VAL L
177	25	CHA3 M8513	CSH 0 ANY WR L
171	20	CHX2 M8515	CSH 1 ANY VAL L
175	25	CHA3 M8513	CSH 1 ANY WR L
172	20	CHX2 M8515	CSH 2 ANY VAL L
176	25	CHA3 M8513	CSH 2 ANY WR L
173	20	CHX2 M8515	CSH 3 ANY VAL L
174	25	CHA3 M8513	CSH 3 ANY WR L
174	27	CSH3 M8513	CSH ADR PMA EN H
172	28	CSH1 M8513	CSH CCA CYC L
174	31	MBX1 M8529	CSH CCA INVAL CSH H
175	31	MBX1 M8529	CSH CCA VAL CORE H
173	28	CSH7 M8513	CSH CCA WRITEBACK L
160	33	MBC2 M8531	CSH DATA CLR DONE IN L
170	27	CSH4 M8513	CSH DATA CLR DONE L
161	27	MBC2 M8531	CSH DATA CLR T1 L
161	28	MBC2 M8531	CSH DATA CLR T2 L
161	29	MBC2 M8531	CSH DATA CLR T3 L
174	20	CHX4 M8515	CSH DIR 0 PAR ODD H
175	20	CHX4 M8515	CSH DIR 1 PAR ODD H
176	20	CHX4 M8515	CSH DIR 2 PAR ODD H
177	20	CHX4 M8515	CSH DIR 3 PAR ODD H
176	28	CSH7 M8513	CSH E WRITEBACK L
171	25	CSH6 M8513	CSH EBOX LOAD REG H
175	22	CSH2 M8513	CSH EBOX RETRY REQ L
170	29	CSH4 M8513	CSH EBOX T3 L
160	19	MBZ1 M8537	CSH EN CSH DATA L
171	26	CSH7 M8513	CSH FILL CACHE RD L
173	25	CHX3 M8513	CSH LRU 1 H
172	25	CHX3 M8513	CSH LRU 2 H
175	28	CSH1 M8513	CSH MB CYC L
161	26	MBZ6 M8537	CSH PAR BIT A H
162	26	MBZ6 M8537	CSH PAR BIT B H
162	17	MBZ5 M8537	CSH PAR BIT IN H
170	28	CSH4 M8513	CSH REFILL RAM WR L
161	30	MBC2 M8531	CSH SEL LRU H
174	26	CSH5 M8513	CSH T0 L
176	26	CSH5 M8513	CSH T2 L
175	21	CHX3 M8515	CSH USE ADR 2 H
176	21	CHX3 M8515	CSH USE ADR 3 H
177	21	CHX3 M8515	CSH USE ADR 4 H
172	27	CSH6 M8513	CSH USE HOLD H
170	21	CHX3 M8515	CSH USE IN 0 H
171	21	CHX3 M8515	CSH USE IN 1 H
172	21	CHX3 M8515	CSH USE IN 2 H
173	21	CHX3 M8515	CSH USE IN 3 H
174	21	CHX3 M8515	CSH USE IN 4 H
175	23	CSH6 M8513	CSH USE WR EN H
163	29	MBC3 M8531	CSH VAL SEL ALL H
163	30	MBC3 M8531	CSH VAL WR DATA H
163	31	MBC3 M8531	CSH WR SEL ALL H
176	31	MBX4 M8529	CSH WR WD 0 EN H
177	31	MBX4 M8529	CSH WR WD 1 EN H
170	32	MBX4 M8529	CSH WR WD 2 EN H
171	32	MBX4 M8529	CSH WR WD 3 EN H
163	32	MBC3 M8531	CSH WR WR DATA H
174	29	CSH1 M8513	CSH1 CACHE IDLE L
174	28	CSH1 M8513	CSH1 EBOX CYC B L
172	26	CSH1 M8513	CSH1 READY TO GO A H
174	22	CSH2 M8513	CSH2 E CORE RD RQ A L
172	29	CSH2 M8513	CSH2 EBOX REQ EN L
173	23	CSH2 M8513	CSH2 MBOX RESP L
173	22	CSH2 M8513	CSH2 ONE WORD RD A L
173	24	CSH2 M8513	CSH2 RD PSE 2ND REQ EN L

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KL10 (PA) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
170	25	CSH2	M8513 CSH2 WR TEST L
176	24	CSH4	M8513 CSH4 EBOX T0 L
171	29	CSH4	M8513 CSH4 EBOX T1 L
173	29	CSH4	M8513 CSH4 EBOX T2 L
177	29	CSH4	M8513 CSH4 EBOX WR T4 L
177	24	CSH4	M8513 CSH4 PAGE FAIL DLY H
173	27	CSH4	M8513 CSH4 WRITEBACK T1 A H
171	27	CSH5	M8513 CSH5 CHAN WR T5 L
170	22	CSH5	M8513 CSH5 PAGE REFILL COMP L
177	26	CSH5	M8513 CSH5 PAGE REFILL T10 L
174	24	CSH5	M8513 CSH5 PAGE REFILL T9,12 L
173	26	CSH5	M8513 CSH5 T1 L
175	26	CSH5	M8513 CSH5 T3 L
177	23	CSH6	M8513 CSH6 DATA DLY 1 L
171	23	CSH6	M8513 CSH6 WR DATA RDY L
106	24	CTL1	M8527 CTL AD LONG H
106	25	CTL1	M8527 CTL ADX CRY 36 A H
105	25	CTL1	M8527 CTL ADX CRY 36 H
100	28	CTL2	M8527 CTL AR 00-08 LOAD L
104	28	CTL2	M8527 CTL AR 00-11 CLR H
101	28	CTL2	M8527 CTL AR 09-17 LOAD L
105	28	CTL2	M8527 CTL AR 12-17 CLR H
101	26	CTL2	M8527 CTL ARL SEL 1 H
100	26	CTL2	M8527 CTL ARL SEL 2 H
103	28	CTL2	M8527 CTL ARL SEL 4 H
106	28	CTL2	M8527 CTL ARR CLR H
100	27	CTL2	M8527 CTL ARR LOAD A L
101	27	CTL2	M8527 CTL ARR LOAD B L
103	26	CTL2	M8527 CTL ARR SEL 1 H
102	26	CTL2	M8527 CTL ARR SEL 2 H
102	28	CTL2	M8527 CTL ARX LOAD H
105	26	CTL2	M8527 CTL ARXL SEL 1 H
104	26	CTL2	M8527 CTL ARXL SEL 2 H
107	26	CTL2	M8527 CTL ARXR SEL 1 H
106	26	CTL2	M8527 CTL ARXR SEL 2 H
102	25	CTL1	M8527 CTL COND/AR GETS EXP H
103	25	CTL1	M8527 CTL DISP RET L
107	24	CTL1	M8527 CTL INH CRY 18 L
136	14	CTL1	M8522 CTL INH CRY 18 L
104	25	CTL1	M8527 CTL LOAD PC L
105	27	CTL2	M8527 CTL MQ SEL 1 H
104	27	CTL2	M8527 CTL MQ SEL 2 H
106	27	CTL2	M8527 CTL MOM EN H
103	27	CTL2	M8527 CTL MOM SEL 1 H
102	27	CTL2	M8527 CTL MOM SEL 2 H
107	28	CTL2	M8527 CTL SPEC CALL L
101	25	CTL1	M8527 CTL SPEC MTR CTL L
101	24	CTL1	M8527 CTL SPEC/CLR FPD H
104	24	CTL1	M8527 CTL SPEC/FLAG CTL H
102	24	CTL1	M8527 CTL SPEC/GEN CRY 18 H
136	15	CTL1	M8522 CTL SPEC/GEN CRY 18 H
100	25	CTL1	M8527 CTL SPEC/SAVE FLAGS L
100	24	CTL1	M8527 CTL SPEC/SCM ALT H
103	24	CTL1	M8527 CTL SPEC/SECTION HOLD H
105	24	CTL1	M8527 CTL SPEC/SP MEM CYCLE H
163	33	MBC3	M8531 DATA VALID A OUT H
164	27	MBC3	M8531 DATA VALID B OUT H
107	27	CTL3	M8527 DIAG LOAD EBUS REG L
107	25	CTL3	M8527 DIAG MEM RESET H
140	03	CRA3	M8511 DISP 02 A H
140	04	CRA3	M8511 DISP 03 A H
140	05	CRA3	M8511 DISP 04 A H
140	01	CRA3	M8511 DISP EN 00-03 L
140	00	CRA3	M8511 DISP EN 00-07 L
140	02	CRA3	M8511 DISP EN 30-37 L
**	130	15	IRD1 M8522 DR ADR 00 A H
**	130	16	IRD1 M8522 DR ADR 01 A H
**	130	17	IRD1 M8522 DR ADR 02 A H
**	131	12	IRD1 M8522 DR ADR 03 A H
**	131	13	IRD1 M8522 DR ADR 04 A H
**	131	14	IRD1 M8522 DR ADR 05 A H
**	131	15	IRD1 M8522 DR ADR 06 A H
**	131	16	IRD1 M8522 DR ADR 07 A H
**	131	17	IRD1 M8522 DR ADR 08 A H
**	133	12	IRD1 M8522 DRAM A 00 H
**	133	13	IRD1 M8522 DRAM A 01 H
**	133	14	IRD1 M8522 DRAM A 02 H
**	133	15	IRD1 M8522 DRAM B 00 H
**	133	16	IRD1 M8522 DRAM B 01 H

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KL10 (PA) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	133	17	IRD1 M8522	DRAM B 02 H
**	134	14	IRD1 M8522	DRAM J 01 H
**	134	15	IRD1 M8522	DRAM J 02 H
**	134	16	IRD1 M8522	DRAM J 03 H
**	134	17	IRD1 M8522	DRAM J 04 H
**	135	14	IRD1 M8522	DRAM J 07 H
**	135	15	IRD1 M8522	DRAM J 08 H
**	135	16	IRD1 M8522	DRAM J 09 H
**	135	17	IRD1 M8522	DRAM J 10 H
**	135	13	IRD3 M8522	DRAM ODD PARITY H
**	135	12	IRD1 M8522	DRAM PAR H
**	176	27	CSH2 M8513	E CACHE WR CYC H
**	102	14	PIC4 M8532	EBUS CS00 E H
**	102	15	PIC4 M8532	EBUS CS01 E H
**	102	16	PIC4 M8532	EBUS CS02 E H
**	102	17	PIC4 M8532	EBUS CS03 E H
**	103	14	PIC4 M8532	EBUS CS04 E H
**	102	11	PIC4 M8532	EBUS CS05 E H
**	102	12	PIC4 M8532	EBUS CS06 E H
**	102	13	PIC2 M8532	EBUS DEMAND E H
*	167	00-08	MBZ2 M8537	EBUS REG 00-08 H
*	167	14-26	MBZ2 M8537	EBUS REG 14-26 H
*	167	27-33	MBZ1 M8531	EBUS REG 27-33 H
*	167	34,35	MBZ2 M8537	EBUS REG 34,35 H
**	120	00	EDP1 M8512	EDP AR 00 H
**	120	01	EDP1 M8512	EDP AR 01 H
**	120	02	EDP1 M8512	EDP AR 02 H
**	120	03	EDP1 M8512	EDP AR 03 H
**	120	04	EDP1 M8512	EDP AR 04 H
**	120	05	EDP1 M8512	EDP AR 05 H
**	120	06	EDP1 M8512	EDP AR 06 H
**	120	07	EDP1 M8512	EDP AR 07 H
**	120	08	EDP1 M8512	EDP AR 08 H
**	120	09	EDP1 M8512	EDP AR 09 H
**	120	10	EDP1 M8512	EDP AR 10 H
**	120	11	EDP1 M8512	EDP AR 11 H
**	133	07	SCD2 M8524	FE 00 H
**	133	08	SCD2 M8524	FE 01 H
**	133	09	SCD2 M8524	FE 02 H
**	133	10	SCD2 M8524	FE 03 H
**	133	11	SCD2 M8524	FE 04 H
**	132	07	SCD2 M8524	FE 05 H
**	132	08	SCD2 M8524	FE 06 H
**	132	09	SCD2 M8524	FE 07 H
**	132	10	SCD2 M8524	FE 08 H
**	132	11	SCD2 M8524	FE 09 H
**	135	07	SCD2 M8524	FE SIGN H
*	123	0-35	EDF4 M8512	FM 0 TO 35 H
**	172	32	MBX1 M8529	FORCE NO MATCH H
**	160	27	MBC5 M8531	FORCE VALID MATCH 0 H
**	160	28	MBC5 M8531	FORCE VALID MATCH 1 H
**	160	29	MBC5 M8531	FORCE VALID MATCH 2 H
**	160	30	MBC5 M8531	FORCE VALID MATCH 3 H
**	136	16	IRD4 M8522	GEN CRY 36 H
**	132	14	IRD1 M8522	IR AC 09 H
**	132	15	IRD1 M8522	IR AC 10 H
**	132	16	IRD1 M8522	IR AC 11 H
**	132	17	IRD1 M8522	IR AC 12 H
**	132	13	IRD3 M8522	IR EN AC H
**	132	12	IRD3 M8522	IR EN I/O, JRST H
**	136	13	IRD1 M8522	IR I/O LEGAL H
**	134	13	IRD3 M8522	IR JRST 0, L
**	130	12	IRD3 M8522	IR NORM 08 H
**	130	13	IRD3 M8522	IR NORM 09 H
**	130	14	IRD3 M8522	IR NORM 10 H
**	174	32	MBX3 M8529	MB DATA CODE 1 H
**	175	32	MBX3 M8529	MB DATA CODE 2 H
**	160	20	MBZ1 M8537	MB IN SEL 1 H
**	161	20	MBZ1 M8537	MB IN SEL 2 H
**	162	20	MBZ1 M8537	MB IN SEL 4 H
**	160	18	MBZ5 M8537	MB PAR BIT IN H
**	176	32	MBX3 M8529	MB PAR H
**	177	32	MBX2 M8529	MB REQ HOLD H
**	170	33	MBX5 M8529	MB REQ IN H
**	171	33	MBX2 M8529	MB SEL 1 H
**	172	33	MBX2 M8529	MB SEL 2 H
**	173	33	MBX2 M8529	MB SEL HOLD H
**	175	24	CSH3 M8513	MB TEST PAR A IN L
**	171	28	CSH3 M8513	MB WR RQ CLR NXT L



KL10 (PA) DIAGNOSTIC READ FUNCTION CODES  
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DF	BIT	DRAWING	BOARD	NAME AND TRUTH
174	33	MBX6	M8529	MB0 HOLD IN H
175	33	MBX6	M8529	MB1 HOLD IN H
176	33	MBX6	M8529	MB2 HOLD IN H
177	33	MBX6	M8529	MB3 HOLD IN H
164	28	MBC3	M8531	MBC INH 1ST MB REQ H
162	27	MBC2	M8531	MBC2 CACHE WR 00 A H
162	28	MBC2	M8531	MBC2 CACHE WR 09 A H
162	29	MBC2	M8531	MBC2 CACHE WR 18 A H
162	30	MBC2	M8531	MBC2 CACHE WR 27 A H
160	32	MBC2	M8531	MBC2 CSH ADR WR PULSE H
161	31	MBC2	M8531	MBC2 CSH VAL WR PULSE H
161	32	MBC2	M8531	MBC2 CSH WR WR PULSE H
162	33	MBC3	M8531	MBC3 ANY SBUS RQ IN L
163	27	MBC3	M8531	MBC3 B CHANGE COMING L
165	30	MBC4	M8531	MBC4 CORE DATA VALID -2 L
165	32	MBC4	M8531	MBC4 CORE RD IN PROG H
161	15	MBZ4	M8537	MBOX ADR PAR ERR L
175	27	CSH3	M8513	MBOX GATE VMA 27-33 H
162	24	MBZ4	M8537	MBOX MB PAR ERR L
161	22	MBZ3	M8537	MBOX NXM ERR L
170	24	CSH6	M8513	MBOX PT DIR WR L
161	24	MBZ4	M8537	MBOX SBUS ERR L
170	34	MBX5	M8529	MBX MEM TO C EN L
176	35	MBX3	M8529	MBX3 SBUS DIAG CYC L
173	30	MBX4	M8529	MBX4 CACHE TO MB DONE H
175	30	MBX4	M8529	MBX4 CACHE TO MB T3 L
160	22	MBZ1	M8537	MBZ1 CHAN CORE BUSY H
161	21	MBZ1	M8537	MBZ1 RD-PSE-WR REF L
161	23	MBZ3	M8537	MBZ3 CHAN MEM REF L
162	22	MBZ3	M8537	MBZ3 HOLD ERA L
162	18	MBZ3	M8537	MBZ3 SEQUENTIAL RQ H
162	23	MBZ4	M8537	MBZ4 NXM T2 H
160	24	MBZ4	M8537	MBZ4 NXM T6,7 L
161	18	MBZ6	M8537	MBZ6 CSH PAR BIT H
106	22	MCL4	M8530	MCL 18 BIT EA H
105	22	MCL4	M8530	MCL 23 BIT EA H
107	21	MCL4	M8530	MCL EA TYPE 09 H
107	20	MCL4	M8530	MCL EA TYPE 10 H
104	23	MCL6	M8530	MCL EBOX CACHE L
107	23	MCL6	M8530	MCL EBOX MAP L
105	23	MCL6	M8530	MCL EBOX MAY BE PAGED L
105	18	MCL2	M8530	MCL LOAD AR H
106	18	MCL2	M8530	MCL LOAD ARX H
104	22	MCL4	M8530	MCL LOAD VMA CONTEXT L
107	22	MCL5	M8530	MCL MBOX CYC REQ H
102	19	MCL1	M8530	MCL MEM/ARL IND H
115	15	APR6	M8539	MCL MEM/REG FUNC L
105	20	MCL3	M8530	MCL PAGE ADDRESS COND H
106	20	MCL3	M8530	MCL PAGE ILL ENTRY H
102	20	MCL2	M8530	MCL PAGE TEST PRIVATE H
104	20	MCL3	M8530	MCL PAGE UEBR REF H
103	21	MCL4	M8530	MCL PREV COND L
103	23	MCL5	M8530	MCL PREV SEC TO ARMM H
106	23	MCL6	M8530	MCL REG FUNC H
103	19	MCL1	M8530	MCL REQ EN L
107	18	MCL2	M8530	MCL STORE AR L
107	19	MCL2	M8530	MCL VMA EXTENDED L
102	22	MCL4	M8530	MCL VMA GETS AD H
103	22	MCL4	M8530	MCL VMA INC H
103	18	MCL2	M8530	MCL VMA PAUSE H
106	19	MCL2	M8530	MCL VMA PREVIOUS L
105	19	MCL2	M8530	MCL VMA PUBLIC H
102	18	MCL2	M8530	MCL VMA READ H
103	20	MCL3	M8530	MCL VMA UPT H
104	19	MCL2	M8530	MCL VMA USER H
104	18	MCL2	M8530	MCL VMA WRITE H
104	21	MCL4	M8530	MCL VMAX EN L
106	21	MCL4	M8530	MCL VMAX SEL 1 H
105	21	MCL4	M8530	MCL VMAX SEL 2 H
102	21	MCL4	M8530	MCL XR PREVIOUS H
165	33	MBC4	M8531	MEM ADR PAR H
162	21	MBZ1	M8537	MEM BUSY H
173	32	MBX3	M8529	MEM DATA TO MEM H
171	34	MBX3	M8529	MEM DIAG L
161	17	MBW5	M8537	MEM PAR IN H
166	27	MBC4	M8531	MEM RD RQ B H
172	34	MBX5	M8529	MEM RD RQ IN H
166	28	MBC4	M8531	MEM RQ 0 H
166	29	MBC4	M8531	MEM RQ 1 H

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KL10 (PA) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
166	30	MBC4	M8531	MEM RQ 2 H
166	31	MBC4	M8531	MEM RQ 3 H
166	32	MBC4	M8531	MEM START L
161	19	MBZ1	M8537	MEM TO C DIAG EN L
164	29	MBC3	M8531	MEM TO C EN L
173	34	MBX3	M8529	MEM TO C SEL 1 H
174	34	MBX3	M8529	MEM TO C SEL 2 H
175	34	MBX5	M8529	MEM WR RQ IN H
166	33	MBC4	M8531	MEM WR RQ L
*	122	0-35	EDP2	M8512 MQ 0 TO 35 H
*	113	20-35	MTR1	M8538 MTR CACHE COUNT 02-17 H
	117	25	MTR3	M8538 MTR CONO MTR, L
*	112	20-35	MTR1	M8538 MTR EBOX COUNT 02-17 H
*	114	24-35	MTR1	M8538 MTR INTERVAL 06-17 H
*	111	20-35	MTR1	M8538 MTR PERF COUNT 02-17 H
*	115	24-35	MTR3	M8538 MTR PERIOD 06-17 H
*	110	20-35	MTR1	M8538 MTR TIME 02-17 H
	116	23	MTR2	M8538 MTR2 ACCT ON H
	116	22	MTR2	M8538 MTR2 EXEC ACCT EN H
	116	21	MTR2	M8538 MTR2 PI ACCT EN H
	116	25	MTR2	M8538 MTR2 TIME ON H
	115	22	MTR3	M8538 MTR3 INTERVAL DONE H
	115	21	MTR3	M8538 MTR3 INTERVAL ON H
	115	23	MTR3	M8538 MTR3 INTERVAL OVRFLO H
	117	22	MTR5	M8538 MTR5 INCR SEL 1 H
	117	21	MTR5	M8538 MTR5 INCR SEL 2 H
	117	20	MTR5	M8538 MTR5 VECTOR REQ H
	160	21	MBZ3	M8537 NXM ACKN H
	160	23	MBZ3	M8537 NXM ANY L
	161	25	MBZ3	M8537 NXM DATA VAL L
	175	29	CSH4	M8513 ONE WORD WR T0 L
	162	25	PAG5	M8537 PAG MB 00-17 PAR H
	160	26	PAG5	M8537 PAG MB 18-35 PAR H
	174	23	CSH6	M8513 PAGE FAIL HOLD L
	171	24	CSH4	M8513 PAGE FAIL T2 L
	177	22	CSH6	M8513 PAGE REFILL ERROR L
	176	29	CSH5	M8513 PAGE REFILL T4 L
	176	23	CSH5	M8513 PAGE REFILL T8 L
*	15X	13-35	VMA3	M8523 PC 13-35 H **NOTE
	164	30	MBC3	M8531 PHASE CHANGE COMING L
	110	17	PIC3	M8539 PI3 APR PIA 01 H
	110	16	PIC3	M8539 PI3 APR PIA 02 H
	110	15	PIC3	M8539 PI3 APR PIA 04 H
**	116	35	PIC3	M8538 PI3 MTR PIA 01 H
**	116	34	PIC3	M8538 PI3 MTR PIA 02 H
**	116	33	PIC3	M8538 PI3 MTR PIA 04 H
	100	10	PIC1	M8532 PIC1 ACTIVE H
**	101	11	PIC1	M8532 PIC1 GEN 1 H
**	101	12	PIC1	M8532 PIC1 GEN 2 H
**	101	13	PIC1	M8532 PIC1 GEN 3 H
**	101	14	PIC1	M8532 PIC1 GEN 4 H
**	101	15	PIC1	M8532 PIC1 GEN 5 H
**	101	16	PIC1	M8532 PIC1 GEN 6 H
**	101	17	PIC1	M8532 PIC1 GEN 7 H
**	100	11	PIC1	M8532 PIC1 ON 1 H
**	100	12	PIC1	M8532 PIC1 ON 2 H
**	100	13	PIC1	M8532 PIC1 ON 3 H
**	100	14	PIC1	M8532 PIC1 ON 4 H
**	100	15	PIC1	M8532 PIC1 ON 5 H
**	100	16	PIC1	M8532 PIC1 ON 6 H
**	100	17	PIC1	M8532 PIC1 ON 7 H
**	100	03	PIC1	M8532 PIC1 PIH1 H
**	100	04	PIC1	M8532 PIC1 PIH2 H
**	100	05	PIC1	M8532 PIC1 PIH3 H
**	100	06	PIC1	M8532 PIC1 PIH4 H
**	100	07	PIC1	M8532 PIC1 PIH5 H
**	100	08	PIC1	M8532 PIC1 PIH6 H
**	100	09	PIC1	M8532 PIC1 PIH7 H
	103	15	PIC2	M8532 PIC2 HONOR INTERNAL H
	103	16	PIC2	M8532 PIC2 READY H
	103	13	PIC2	M8532 PIC2 STATE HOLD H
	103	11	PIC2	M8532 PIC2 TIMER DONE H
	103	12	PIC5	M8532 PIC5 EBUS PI GRANT H
	103	17	PIC5	M8532 PIC5 EBUS REQ H
	177	28	CSH2	M8513 RD PAUSE 2ND HALF L
	176	34	MBX3	M8529 REFILL HOLD H
	177	34	MBX5	M8529 RQ 0 IN H
	170	35	MBX5	M8529 RQ 1 IN H
	171	35	MBX5	M8529 RQ 2 IN H

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KL10 (PA) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
	172	35 MBX5 M8529	RQ 3 IN H
	161	33 MBC2 M8531	RQ HOLD FF H
**	143	01 CRA4 M8511	SBR RET 00 H
**	143	02 CRA4 M8511	SBR RET 01 H
**	143	03 CRA4 M8511	SBR RET 02 H
**	143	04 CRA4 M8511	SBR RET 03 H
**	143	05 CRA4 M8511	SBR RET 04 H
**	142	00 CRA4 M8511	SBR RET 05 H
**	142	01 CRA4 M8511	SBR RET 06 H
**	142	02 CRA4 M8511	SBR RET 07 H
**	142	03 CRA4 M8511	SBR RET 08 H
**	142	04 CRA4 M8511	SBR RET 09 H
**	142	05 CRA4 M8511	SBR RET 10 H
	173	35 MBX2 M8529	SBUS ADR 34 H
	174	35 MBX2 M8529	SBUS ADR 35 H
	162	31 MBC2 M8531	SBUS ADR HOLD H
	175	35 MBX3 M8529	SBUS DIAG 3 L
	136	07 SCD2 M8524	SC .GE. 36 H
**	131	07 SCD2 M8524	SC 00 H
**	131	08 SCD2 M8524	SC 01 H
**	131	09 SCD2 M8524	SC 02 H
**	131	10 SCD2 M8524	SC 03 H
**	131	11 SCD2 M8524	SC 04 H
**	130	07 SCD2 M8524	SC 05 H
**	130	08 SCD2 M8524	SC 06 H
**	130	09 SCD2 M8524	SC 07 H
**	130	10 SCD2 M8524	SC 08 H
**	130	11 SCD2 M8524	SC 09 H
	134	07 SCD2 M8524	SC SIGN H
	133	04 SCD1 M8524	SCAD=0 L
	137	06 SCD5 M8524	SCD ADR BREAK PREVENT H
	137	05 SCD5 M8524	SCD ADR BRK CYC H
	137	02 SCD5 M8524	SCD ADR BRK INH H
	131	03 SCD4 M8524	SCD CRYO H
	131	04 SCD4 M8524	SCD CRY1 H
	131	06 SCD4 M8524	SCD DIV CHK H
	132	03 SCD4 M8524	SCD FOV H
	130	06 SCD4 M8524	SCD FPD H
	132	04 SCD4 M8524	SCD FXU H
	135	04 SCD5 M8524	SCD KERNEL MODE H
	136	02 SCD5 M8524	SCD KERNEL OR USER IOT H
	134	03 SCD5 M8524	SCD LEAVE USER H
	133	03 SCD5 M8524	SCD LOAD FLAGS A H
	133	06 SCD4 M8524	SCD NICOND 10 H
	131	02 SCD4 M8524	SCD OV H
	133	02 SCD4 M8524	SCD PCP H
	135	06 SCD5 M8524	SCD PRIVATE INSTR EN L
	135	05 SCD5 M8524	SCD PRIVATE INSTR L
	135	03 SCD5 M8524	SCD PUBLIC A H
	135	02 SCD5 M8524	SCD PUBLIC EN L
	134	06 SCD5 M8524	SCD PUBLIC PAGE H
	137	07 SCD4 M8524	SCD TRAP CLEAR L
	130	04 SCD4 M8524	SCD TRAP CYC 1 H
	130	03 SCD4 M8524	SCD TRAP CYC 2 H
**	136	03 SCD3 M8524	SCD TRAP MIX 32 H
**	136	04 SCD3 M8524	SCD TRAP MIX 33 H
**	137	03 SCD3 M8524	SCD TRAP MIX 34 H
**	137	04 SCD3 M8524	SCD TRAP MIX 35 H
	130	05 SCD4 M8524	SCD TRAP REQ 1 H
	130	02 SCD4 M8524	SCD TRAP REQ 2 H
	134	02 SCD5 M8524	SCD USER A L
	134	05 SCD5 M8524	SCD USER EN L
	136	05 SCD5 M8524	SCD USER IOT A H
	136	06 SCD5 M8524	SCD USER IOT EN L
	160	17 SHD1 M8537	SH AR PAR ODD A H
	105	31 SHD1 M8526	SH AR PAR ODD H
	106	31 SHD1 M8526	SH ARX PAR ODD H
	134	12 IRD3 M8522	TEST SATISFIED H
*	15X	13-35 VMA2 M8523	VMA 13-35 H **NOTE
	153	13 VMA1 M8523	VMA 18-31=0 H
	157	13 VMA1 M8523	VMA AC REF H
*	15X	13-35 VMA4 M8523	VMA HELD 13-35 H **NOTE
	132	02 SCD4 M8524	VMA HELD OR PC 00 H
**	100	18 MCL3 M8530	VMA HELD OR PC 01 H
**	100	19 MCL3 M8530	VMA HELD OR PC 02 H
**	100	20 MCL3 M8530	VMA HELD OR PC 03 H
**	100	21 MCL3 M8530	VMA HELD OR PC 04 H
**	100	22 MCL3 M8530	VMA HELD OR PC 05 H
**	100	23 MCL3 M8530	VMA HELD OR PC 06 H

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## KL10 (PA) DIAGNOSTIC READ FUNCTION CODES SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
**	101	18 MCL3 M8530	VMA HELD OR PC 07 d
**	101	19 MCL3 M8530	VMA HELD OR PC 08 H
**	101	20 MCL3 M8530	VMA HELD OR PC 09 H
**	101	21 MCL3 M8530	VMA HELD OR PC 10 H
**	101	22 MCL3 M8530	VMA HELD OR PC 11 H
**	101	23 MCL3 M8530	VMA HELD OR PC 12 H
	157	15 VMA3 M8523	VMA MATCH 13-35 H
	160	31 MBC1 M8531	WRITE OK H
	177	35 MBX4 M8529	WRITEBACK T2 L

### NOTE

TRACON and the 11-based 10 diagnostic programs interpret all diagnostic read functions which are not preceded with either a single or double asterisk [(\*) or (\*\*)] as single bits; as such, they are printed out by bit position and/or name. Diagnostic read functions preceded by a single asterisk (\*) are interpreted as registers and are printed out as such. Diagnostic read functions which are preceded by a double asterisk (\*\*) may be interpreted and printed as either single bits or as a register depending on the program doing the interpretation.

KL10 (PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	100	03	PIC1 M8532	PIC1 PIH1 H
**	100	04	PIC1 M8532	PIC1 PIH2 H
**	100	05	PIC1 M8532	PIC1 PIH3 H
**	100	06	PIC1 M8532	PIC1 PIH4 H
**	100	07	PIC1 M8532	PIC1 PIH5 H
**	100	08	PIC1 M8532	PIC1 PIH6 H
**	100	09	PIC1 M8532	PIC1 PIH7 H
**	100	10	PIC1 M8532	PIC1 ACTIVE H
**	100	11	PIC1 M8532	PIC1 ON 1 H
**	100	12	PIC1 M8532	PIC1 ON 2 H
**	100	13	PIC1 M8532	PIC1 ON 3 H
**	100	14	PIC1 M8532	PIC1 ON 4 H
**	100	15	PIC1 M8532	PIC1 ON 5 H
**	100	16	PIC1 M8532	PIC1 ON 6 H
**	100	17	PIC1 M8532	PIC1 ON 7 H
**	100	18	MCL3 M8544	VMA HELD OR PC 01 H
**	100	19	MCL3 M8544	VMA HELD OR PC 02 H
**	100	20	MCL3 M8544	VMA HELD OR PC 03 H
**	100	21	MCL3 M8544	VMA HELD OR PC 04 H
**	100	22	MCL3 M8544	VMA HELD OR PC 05 H
**	100	23	MCL3 M8544	VMA HELD OR PC 06 H
**	100	24	CTL1 M8543	CTL SPEC/SCM ALT H
**	100	25	CTL1 M8543	CTL SPEC/SAVE FLAGS L
**	100	26	CTL2 M8543	CTL ARL SEL 2 H
**	100	27	CTL2 M8543	CTL ARR LOAD A L
**	100	28	CTL2 M8543	CTL AR 00-08 LOAD L
**	100	30	CLK1 M8526YA	CLK EBUS CLK H
**	100	31	CLK1 M8526YA	CLK SBUS CLK H
**	100	32	CLK4 M8526YA	CLK INSTR 1777 H
**	100	33	CLK5 M8526YA	CLK5 BURST CNT=0 H
**	100	34	CLK5 M8526YA	CLK5 BURST 128 H
**	100	35	CLK5 M8526YA	CLK5 BURST 64 H
**	101	11	PIC1 M8532	PIC1 GEN 1 H
**	101	12	PIC1 M8532	PIC1 GEN 2 H
**	101	13	PIC1 M8532	PIC1 GEN 3 H
**	101	14	PIC1 M8532	PIC1 GEN 4 H
**	101	15	PIC1 M8532	PIC1 GEN 5 H
**	101	16	PIC1 M8532	PIC1 GEN 6 H
**	101	17	PIC1 M8532	PIC1 GEN 7 H
**	101	18	MCL3 M8544	VMA HELD OR PC 07 H
**	101	19	MCL3 M8544	VMA HELD OR PC 08 H
**	101	20	MCL3 M8544	VMA HELD OR PC 09 H
**	101	21	MCL3 M8544	VMA HELD OR PC 10 H
**	101	22	MCL3 M8544	VMA HELD OR PC 11 H
**	101	23	MCL3 M8544	VMA HELD OR PC 12 H
**	101	24	CTL1 M8543	CTL SPEC/CLR PFD H
**	101	25	CTL1 M8543	CTL SPEC MTR CTL L
**	101	26	CTL2 M8543	CTL ARL SEL 1 H
**	101	27	CTL2 M8543	CTL ARR LOAD B L
**	101	28	CTL2 M8543	CTL AR 09-17 LOAD L
**	101	30	CLK5 M8526YA	CLK5 BURST 32 H
**	101	31	CLK5 M8526YA	CLK5 BURST 16 H
**	101	32	CLK5 M8526YA	CLK5 BURST 08 H
**	101	33	CLK5 M8526YA	CLK5 BURST 04 H
**	101	34	CLK5 M8526YA	CLK5 BURST 02 H
**	101	35	CLK5 M8526YA	CLK5 BURST 01 H
**	102	11	PIC4 M8532	EBUS CS05 E H
**	102	12	PIC4 M8532	EBUS CS06 E H
**	102	13	PIC2 M8532	EBUS DEMAND E H
**	102	14	PIC4 M8532	EBUS CS00 E H
**	102	15	PIC4 M8532	EBUS CS01 E H
**	102	16	PIC4 M8532	EBUS CS02 E H
**	102	17	PIC4 M8532	EBUS CS03 E H
**	102	18	MCL2 M8544	MCL2 VMA READ H
**	102	19	MCL1 M8544	MCL1 MEM/ARL IND H
**	102	20	MCL3 M8544	MCL3 PAGE TEST PRIVATE H
**	102	21	MCL4 M8544	MCL4 XR PREVIOUS H
**	102	22	MCL4 M8544	MCL4 VMA GETS AD H
**	102	23	MCL4 M8544	MCL4 XR SHORT H
**	102	24	CTL1 M8543	CTL SPEC/GEN CRY 18 H
**	102	25	CTL1 M8543	CTL COND/AR GETS EXP H
**	102	26	CTL2 M8543	CTL ARR SEL 2 H
**	102	27	CTL2 M8543	CTL MQM SEL 2 H
**	102	28	CTL2 M8543	CTL ARX LOAD H
**	102	30	CLK1 M8526YA	CLK ERROR STOP H
**	102	31	CLK2 M8526YA	CLK2 GO L
**	102	32	CLK4 M8526YA	CLK EBOX REQ H
**	102	33	CLK3 M8526YA	CLK3 SYNC H
**	102	34	CLK4 M8526YA	CLK4 PAGE FAIL EN L

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KL10 (PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
102	35	CLK4 M8526YA	CLK PORCE 1777 H
103	11	PIC2 M8532	PIC2 TIMER DONE H
103	12	PIC5 M8532	PIC5 EBUS PI GRANT H
103	13	PIC2 M8532	PIC2 STATE HOLD H
**	103	14	PIC4 M8532 EBUS CS04 E H
103	15	PIC2 M8532	PIC2 HONOR INTERNAL H
103	16	PIC2 M8532	PIC2 READY H
103	17	PIC5 M8532	PIC5 EBUS REQ H
103	18	MCL2 M8544	MCL2 VMA PAUSE H
103	19	MCL1 M8544	MCL1 REQ EN L
103	20	MCL6 M8544	MCL6 VMA UPT H
103	21	MCL5 M8544	MCL5 VMA ADR ERR H
103	22	MCL4 M8544	MCL4 VMA INC H
103	23	MCL4 M8544	MCL4 SHORT STACK H
103	24	CTL1 M8543	CTL SPEC/STACK UPDATE H
103	25	CTL1 M8543	CTL DISP RET L
103	26	CTL2 M8543	CTL ARR SEL 1 H
103	27	CTL2 M8543	CTL MQM SEL 1 H
103	28	CTL2 M8543	CTL ARL SEL 4 H
103	30	CLK3 M8526YA	CLK3 DRAM PAR ERR H
103	31	CLK2 M8526YA	CLK2 BURST L
103	32	CLK4 M8526YA	CLK MB XPER H
103	33	CLK4 M8526YA	CLK4 EBOX CLK L
103	34	CLK4 M8526YA	CLK PAGE ERROR H
103	35	CLK4 M8526YA	CLK4 1777 EN H
104	18	MCL2 M8544	MCL2 VMA WRITE H
104	19	MCL2 M8544	MCL VMA USER H
104	20	MCL6 M8544	MCL6 PAGE UEBR REF H
104	21	MCL5 M8544	MCL5 VMAX EN L
104	22	MCL4 M8544	MCL4 LOAD VMA CONTEXT L
104	23	MCL6 M8544	MCL6 EBOX CACHE L
104	24	CTL1 M8543	CTL SPEC/FLAG CTL H
104	25	CTL1 M8543	CTL LOAD PC L
104	26	CTL2 M8543	CTL ARXL SEL 2 H
104	27	CTL2 M8543	CTL MQ SEL 2 H
104	28	CTL2 M8543	CTL AR 00-11 CLR H
104	30	CLK3 M8526YA	CLK3 CRAM PAR ERR H
104	31	CLK2 M8526YA	CLK2 EBOX SS L
104	32	CLK5 M8526YA	CLK5 SOURCE SEL 2 H
104	33	CLK3 M8526YA	CLK3 EBOX SOURCE H
104	34	CLK5 M8526YA	CLK5 FM PAR CHECK L
104	35	CLK5 M8526YA	CLK5 MBOX CYCLE DIS H
105	18	MCL2 M8544	MCL LOAD AR H
105	19	MCL2 M8544	MCL2 VMA PUBLIC H
105	20	MCL3 M8544	MCL3 PAGE ADDRESS COND H
105	21	MCL4 M8544	MCL4 VMAX SEL 2 H
105	22	MCL5 M8544	MCL5 23 BIT EA H
105	23	MCL6 M8544	MCL6 EBOX MAY BE PAGED L
105	24	CTL1 M8543	CTL SPEC/SP MEM CYCLE H
105	25	CTL1 M8543	CTL ADX CRY 36 H
105	26	CTL2 M8543	CTL ARXL SEL 1 L
105	27	CTL2 M8543	CTL MQ SEL 1 H
105	28	CTL2 M8543	CTL AR 12-17 CLR H
105	30	CLK3 M8526YA	CLK3 FM PAR ERR H
105	31	SHD1 M8526YA	SH AR PAR ODD H
105	32	CLK5 M8526YA	CLK5 SOURCE SEL 1 H
105	33	CLK5 M8526YA	CLK5 EBOX CRM DIS H
105	34	CLK5 M8526YA	CLK5 CRAM PAR CHECK L
105	35	CLK5 M8526YA	CLK5 MBOX RESP SIM L
106	18	MCL2 M8544	MCL LOAD ARX H
106	19	MCL2 M8544	MCL2 VMA PREVIOUS L
106	20	MCL3 M8544	MCL3 PAGE ILL ENTRY H
106	21	MCL4 M8544	MCL4 VMAX SEL 1 H
106	22	MCL5 M8544	MCL5 18 BIT EA H
106	23	MCL6 M8544	MCL6 REG FUNC H
106	24	CTL1 M8543	CTL AD LONG H
106	25	CTL1 M8543	CTL ADX CRY 36 A H
106	26	CTL2 M8543	CTL ARXR SEL 2 H
106	27	CTL2 M8543	CTL NOM EN H
106	28	CTL2 M8543	CTL ARR CLR H
106	30	CLK3 M8526YA	CLK3 FS ERROR H
106	31	SHD1 M8526YA	SH ARX PAR ODD H
106	32	CLK5 M8526YA	CLK5 RATE SEL 2 H
106	33	CLK5 M8526YA	CLK5 EBOX EDP DIS H
106	34	CLK5 M8526YA	CLK5 DRAM PAR CHECK L
106	35	CLK5 M8526YA	CLK5 AR/ARX PAR CHECK L
107	18	MCL2 M8544	MCL STORE AR L
107	19	MCL2 M8544	MCL2 VMA EXTENDED L
107	20	MCL6 M8544	MCL6 VMA FETCH H

KL10 (PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
107	21	MCL6	M8544	MCL6 PAGED PUTCA L
107	22	MCL5	M8544	MCL MBOX CYC REQ H
107	23	MCL6	M8544	MCL6 EBOX MAP L
107	24	CTL1	M8543	CTL INH CRV 18 L
107	25	CTL3	M8543	DIAG MEM RESET H
107	26	CTL2	M8543	CTL ARXR SEL 1 H
107	27	CTL3	M8543	DIAG LOAD EBUS REG L
107	28	CTL2	M8543	CTL SPEC CALL L
107	30	CLK3	M8526YA	CLK3 ERROR L
107	31	CLK4	M8526YA	CLK4 PAGE FAIL H
107	32	CLK5	M8526YA	CLK5 RATE SEL 1 H
107	33	CLK5	M8526YA	CLK5 EBOX CTL DIS H
107	34	CLK5	M8526YA	CLK5 FS CHECK L
107	35	CLK5	M8526YA	CLK5 ERR STOP EN L
110	01	APR1	M8545	APR1 SWEEP BUSY EN H
110	06	APR1	M8545	APR1 SBUS ERR IN H
110	07	APR1	M8545	APR1 NXM ERR IN H
110	08	APR1	M8545	APR1 I/O PF ERR IN H
110	09	APR1	M8545	APR1 MB PAR ERR IN H
110	10	APR2	M8545	APR2 C DIR P ERR IN H
110	11	APR2	M8545	APR2 S ADR P ERR IN H
110	12	APR2	M8545	APR2 PWR FAIL IN H
110	13	APR2	M8545	APR2 SWEEP DONE IN H
110	14	APR2	M8545	APR2 APR INTERRUPT H
110	15	PIC3	M8545	PI3 APR PIA 04 H
110	16	PIC3	M8545	PI3 APR PIA 02 H
110	17	PIC3	M8545	PI3 APR PIA 01 H
110	20-35	MTR1	M8538	MTR TIME 02-17 H
111	06	APR5	M8545	APR5 CURRENT BLOCK 4 H
111	07	APR5	M8545	APR5 CURRENT BLOCK 2 H
111	08	APR5	M8545	APR5 CURRENT BLOCK 1 H
111	09	APR5	M8545	APR5 PREV BLOCK 4 H
111	10	APR5	M8545	APR5 PREV BLOCK 2 H
111	11	APR5	M8545	APR5 PREV BLOCK 1 H
111	12	SHM1	M8540	SHM1 AR EXTENDED H
111	13	APR3	M8545	APR3 FM EXTENDED H
111	14	APR4	M8545	APR4 AC+# 09 H
111	15	APR4	M8545	APR4 AC+# 10 H
111	16	APR4	M8545	APR4 AC+# 11 H
111	17	APR4	M8545	APR4 AC+# 12 H
111	20-35	MTR1	M8538	MTR PERF COUNT 02-17 H
112	06	APR1	M8545	APR1 SBUS ERR EN IN H
112	07	APR1	M8545	APR1 NXM ERR EN IN H
112	08	APR1	M8545	APR1 I/O PF ERR EN IN H
112	09	APR1	M8545	APR1 MB PAR ERR EN IN H
112	10	APR2	M8545	APR2 C DIR P ERR EN IN H
112	11	APR2	M8545	APR2 S ADR P ERR EN IN H
112	12	APR2	M8545	APR2 PWR FAIL EN IN H
112	13	APR2	M8545	APR2 SWEEP DONE EN IN H
112	20-35	MTR1	M8538	MTR EBOX COUNT 02-17 H
113	09	APR3	M8545	APR3 FETCH COMP H
113	10	APR3	M8545	APR3 READ COMP H
113	11	APR3	M8545	APR3 WRITE COMP H
113	12	APR3	M8545	APR3 USER COMP H
113	20-35	MTR1	M8538	MTR CACHE COUNT 02-17 H
114	07	APR5	M8545	APR MBOX CTL 03 H
114	08	APR5	M8545	APR FM BLOCK 4 H
114	09	APR5	M8545	APR FM BLOCK 2 H
114	10	APR5	M8545	APR FM BLOCK 1 H
114	11	APR4	M8545	APR FM ADR 10 H
114	12	APR4	M8545	APR FM ADR 4 H
114	13	APR4	M8545	APR FM ADR 2 H
114	14	APR4	M8545	APR FM ADR 1 H
114	15	APR4	M8545	APR4 FO2 EN H
114	16	APR3	M8545	APR FM 36 H
114	17	APR3	M8545	APR3 FM ODD PARITY H
114	24-35	MTR1	M8538	MTR INTERVAL 06-17 H
115	07	APR5	M8545	APR MBOX CTL 06 H
115	08	APR5	M8545	APR5 SET PAGE FAIL L
115	09	APR3	M8545	APR EBUS RETURN H
115	10	APR3	M8545	APR EBOX DISABLE CS H
115	11	APR2	M8545	APR2 WR BAD ADR PAR L
115	12	APR6	M8545	APR6 EBOX CCA H
115	13	APR6	M8545	APR EBOX ERA H
115	14	APR6	M8545	APR6 EBOX SBUS DIAG H
115	15	MCL1	M8545	MCL1 MEM/REG FUNC L
115	16	APR6	M8545	APR6 EBOX LOAD REG L
115	17	APR6	M8545	APR6 EBOX READ REG L
115	21	MTR3	M8538	MTR3 INTERVAL ON H
115	22	MTR3	M8538	MTR3 INTERVAL DONE H

GEN. INFO.

KL10(PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DP	BIT	DRAWING	BOARD	NAME AND TRUTH
	115	23	MTR3 M8538	MTR3 INTERVAL OVRFL0 H
*	115	24-35	MTR3 M8538	MTR PERIOD 06-17 H
	116	07	APR5 M8545	APR5 WR PT SEL 0 H
	116	08	APR5 M8545	APR5 PT DIR WR L
	116	09	APR3 M8545	APR EBUS REQ L
	116	10	APR3 M8545	APR EBUS F01 E H
	116	11	APR2 M8545	APR ANY EBOX ERR FLG H
	116	12	APR6 M8545	APR6 EBOX UBR H
	116	13	APR6 M8545	APR EN REFILL RAM WR H
	116	21	MTR2 M8538	MTR2 PI ACCT EN H
	116	22	MTR2 M8538	MTR2 EXEC ACCT EN H
	116	23	MTR2 M8538	MTR2 ACCT ON H
	116	25	MTR2 M8538	MTR2 TIME ON H
**	116	33	PIC3 M8538	PI3 MTR PIA 04 H
**	116	34	PIC3 M8538	PI3 MTR PIA 02 H
**	116	35	PIC3 M8538	PI3 MTR PIA 01 H
	117	07	APR5 M8545	APR5 WR PT SEL 1 H
	117	08	APR5 M8545	APR5 PT WR L
	117	09	APR3 M8545	APR3 EBUS DEMAND H
	117	10	APR3 M8545	APR3 EBOX SEND F02 H
	117	11	CON5 M8545	CON FM WRITE PAR L
	117	12	APR6 M8545	APR6 EBOX EBR H
	117	13	APR6 M8545	APR6 EBOX SPARE H
	117	20	MTR5 M8538	MTR5 VECTOR REQ H
	117	21	MTR5 M8538	MTR5 INCR SEL 2 H
	117	22	MTR5 M8538	MTR5 INCR SEL 1 H
	117	25	MTR3 M8538	MTR CONO MTR, L
**	120	00	EDP1 M8512	EDP AR 00 H
**	120	01	EDP1 M8512	EDP AR 01 H
**	120	02	EDP1 M8512	EDP AR 02 H
**	120	03	EDP1 M8512	EDP AR 03 H
**	120	04	EDP1 M8512	EDP AR 04 H
**	120	05	EDP1 M8512	EDP AR 05 H
**	120	06	EDP1 M8512	EDP AR 06 H
**	120	07	EDP1 M8512	EDP AR 07 H
**	120	08	EDP1 M8512	EDP AR 08 H
**	120	09	EDP1 M8512	EDP AR 09 H
**	120	10	EDP1 M8512	EDP AR 10 H
**	120	11	EDP1 M8512	EDP AR 11 H
*	120	12-35	EDP1 M8512	AR 12 TO 35 H
*	121	0-35	EDP4 M8512	BR 0 TO 35 H
*	122	0-35	EDP2 M8512	MQ 0 TO 35 H
*	123	0-35	EDP4 M8512	FM 0 TO 35 H
*	124	0-35	EDP4 M8512	BRX 0 TO 35 H
*	125	0-35	EDP2 M8512	ARX 0 TO 35 H
*	126	0-35	EDP3 M8512	ADX 0 TO 35 H
*	127	0-35	EDP3 M8512	AD 0 TO 35 H
	130	02	SCD4 M8524	SCD TRAP REQ 2 H
	130	03	SCD4 M8524	SCD TRAP CYC 2 H
	130	04	SCD4 M8524	SCD TRAP CYC 1 H
	130	05	SCD4 M8524	SCD TRAP REQ 1 H
	130	06	SCD4 M8524	SCD FPD H
**	130	07	SCD2 M8524	SC 05 H
**	130	08	SCD2 M8524	SC 06 H
**	130	09	SCD2 M8524	SC 07 H
**	130	10	SCD2 M8524	SC 08 H
**	130	11	SCD2 M8524	SC 09 H
	130	12	IRD3 M8522	IR NORM 08 H
	130	13	IRD3 M8522	IR NORM 09 H
	130	14	IRD3 M8522	IR NORM 10 H
**	130	15	IRD1 M8522	DR ADR 00 A H
**	130	16	IRD1 M8522	DR ADR 01 A H
**	130	17	IRD1 M8522	DR ADR 02 A H
	130	18	CON3 M8525	CON WR EVEN PAR ADR H
	130	19	CON3 M8525	CON3 WR EVEN PAR DATA H
	130	20	CON3 M8525	CON3 WR EVEN PAR DIR H
	131	02	SCD4 M8524	SCD OV H
	131	03	SCD4 M8524	SCD CRY0 H
	131	04	SCD4 M8524	SCD CRY1 H
	131	05	EDP3 M8524	AD CRY1 01 L
	131	06	SCD4 M8524	SCD DIV CHK H
**	131	07	SCD2 M8524	SC 00 H
**	131	08	SCD2 M8524	SC 01 H
**	131	09	SCD2 M8524	SC 02 H
**	131	10	SCD2 M8524	SC 03 H
**	131	11	SCD2 M8524	SC 04 H
**	131	12	IRD1 M8522	DR ADR 03 A H
**	131	13	IRD1 M8522	DR ADR 04 A H
**	131	14	IRD1 M8522	DR ADR 05 A H
**	131	15	IRD1 M8522	DR ADR 06 A H



KL10(PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING BOARD	NAME AND TRUTH
**	131	16	IRD1 M8522	DR ADR 07 A H
**	131	17	IRD1 M8522	DR ADR 08 A H
	131	18	CON3 M8525	CON3 CACHE LOOK EN H
	131	19	CON3 M8525	CON CACHE LOAD EN H
	131	21	CON3 M8525	CON K110 PAGING MODE L
	131	22	CON3 M8525	CON TRAP EN H
	132	02	SCD4 M8524	VMA HELD OR PC 00 H
	132	03	SCD4 M8524	SCD FOV H
	132	04	SCD4 M8524	SCD FXU H
	132	05	EDP3 M8524	AD OVERFLOW 00 L
	132	06	IRD4 M8524	AD CRY -02 A L
**	132	07	SCD2 M8524	FE 05 H
**	132	08	SCD2 M8524	FE 06 H
**	132	09	SCD2 M8524	FE 07 H
**	132	10	SCD2 M8524	FE 08 H
**	132	11	SCD2 M8524	FE 09 H
	132	12	IRD3 M8522	IR EN I/O, JRST H
	132	13	IRD3 M8522	IR EN AC H
**	132	14	IRD1 M8522	IR AC 09 H
**	132	15	IRD1 M8522	IR AC 10 H
**	132	16	IRD1 M8522	IR AC 11 H
**	132	17	IRD1 M8522	IR AC 12 H
	132	18	CON1 M8525	CON COND EN 00-07 L
	132	19	CON1 M8525	CON COND/SEL VMA L
	132	20	CON1 M8525	CON COND/MBOX CTL L
	132	21	CON2 M8525	CON LONG EN L
	132	22	CON2 M8525	CON LOAD IR L
	132	23	CON4 M8525	CON4 AR LOADED H
	132	24	CON5 M8525	CON5 PI CYCLE H
	133	02	SCD4 M8524	SCD PCP H
	133	03	SCD5 M8524	SCD LOAD FLAGS A H
	133	04	SCD1 M8524	SCAD=0 L
	133	05	CON2 M8524	CON CLR PRIVATE INSTR H
	133	06	SCD4 M8524	SCD NICOND 10 H
**	133	07	SCD2 M8524	FE 00 H
**	133	08	SCD2 M8524	FE 01 H
**	133	09	SCD2 M8524	FE 02 H
**	133	10	SCD2 M8524	FE 03 H
**	133	11	SCD2 M8524	FE 04 H
**	133	12	IRD1 M8522	DRAM A 00 H
**	133	13	IRD1 M8522	DRAM A 01 H
**	133	14	IRD1 M8522	DRAM A 02 H
**	133	15	IRD1 M8522	DRAM B 00 H
**	133	16	IRD1 M8522	DRAM B 01 H
**	133	17	IRD1 M8522	DRAM B 02 H
	133	18	CON1 M8525	CON SKIP EN 40-47 L
	133	19	CON1 M8525	CON COND/VMA GETS # H
	133	20	CON3 M8525	CON EBUS REL H
	133	21	CON4 M8525	CON PC+1 INH L
	133	22	CON2 M8525	CON COND INSTR ABORT H
	133	23	CON4 M8525	CON ARX LOADED L
	133	24	CON5 M8525	CON5 MEM CYCLE L
	134	02	SCD5 M8524	SCD USER A L
	134	03	SCD5 M8524	SCD LEAVE USER H
	134	04	CON5 M8524	CON PI CYCLE A L
	134	05	SCD5 M8524	SCD USER EN L
	134	06	SCD5 M8524	SCD PUBLIC PAGE H
	134	07	SCD2 M8524	SC SIGN H
	134	12	IRD3 M8522	TEST SATISFIED H
	134	13	IRD3 M8522	IR JRST 0, L
**	134	14	IRD1 M8522	DRAM J 01 H
**	134	15	IRD1 M8522	DRAM J 02 H
**	134	16	IRD1 M8522	DRAM J 03 H
**	134	17	IRD1 M8522	DRAM J 04 H
	134	18	CON1 M8525	CON SKIP EN 50-57 L
	134	19	CON1 M8525	CON COND/LOAD VMA HELD H
	134	20	CON3 M8525	CON SR 00 H
	134	21	CON2 M8525	CON NICOND TRAP EN H
	134	22	CON2 M8525	CON LOAD ACCESS COND H
	134	23	CON4 M8525	CON UCODE STATE 01 H
	134	24	CON5 M8525	CON FM WRITE PAR L
	135	02	SCD5 M8524	SCD PUBLIC EN L
	135	03	SCD5 M8524	SCD PUBLIC A H
	135	04	SCD5 M8524	SCD KERNEL MODE H
	135	05	SCD5 M8524	SCD PRIVATE INSTR L
	135	06	SCD5 M8524	SCD PRIVATE INSTR EN L
	135	07	SCD2 M8524	FE SIGN H
**	135	12	IRD1 M8522	DRAM PAR H
**	135	13	IRD3 M8522	DRAM ODD PARITY H
**	135	14	IRD1 M8522	DRAM J 07 H

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KL10(PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	135	15	IRD1	M8522	DRAM J 08 H
**	135	16	IRD1	M8522	DRAM J 09 H
**	135	17	IRD1	M8522	DRAM J 10 H
	135	18	CON3	M8525	CON DELAY REQ H
	135	19	CON1	M8525	CON LOAD SPEC INSTR L
	135	20	CON3	M8525	CON SR 01 H
	135	21	CON2	M8525	CON NICOND 07 H
	135	22	CON2	M8525	CON2 INSTR GO L
	135	23	CON4	M8525	CON UCODE STATE 03 H
	135	24	CON5	M8525	CON MBOX WAIT L
	136	02	SCD5	M8524	SCD KERNEL OR USER IOT H
**	136	03	SCD3	M8524	SCD TRAP MIX 32 H
**	136	04	SCD3	M8524	SCD TRAP MIX 33 H
	136	05	SCD5	M8524	SCD USER IOT A H
	136	06	SCD5	M8524	SCD USER IOT EN L
	136	07	SCD2	M8524	SC .GE. 36 H
	136	12	IRD3	M8522	AD=0 L
	136	13	IRD1	M8522	IR I/O LEGAL H
	136	14	CTL1	M8522	CTL INH CRY 18 L
	136	15	CTL1	M8522	CTL SPEC/GEN CRY 18 H
	136	16	IRD4	M8522	GEN CRY 36 H
	136	17	IRD4	M8522	AD CRY -02 A H
	136	18	CON4	M8525	CON AR 36 H
	136	19	CON1	M8525	CON VMA SEL 2 L
	136	20	CON3	M8525	CON SR 02 H
	136	21	CON2	M8525	CON NICOND 08 H
	136	22	CON2	M8525	CON LOAD DRAM H
	136	23	CON4	M8525	CON UCODE STATE 05 H
	136	24	CON5	M8525	CON FM XFER L
	137	02	SCD5	M8524	SCD ADR BRK INH H
**	137	03	SCD3	M8524	SCD TRAP MIX 34 H
**	137	04	SCD3	M8524	SCD TRAP MIX 35 H
	137	05	SCD5	M8524	SCD ADR BRK CYC H
	137	06	SCD5	M8524	SCD ADR BREAK PREVENT H
	137	07	SCD4	M8524	SCD TRAP CLEAR L
	137	12	IRD4	M8522	AD CRY 12 H
	137	13	IRD4	M8522	AD CRY 18 H
	137	14	IRD4	M8522	AD CRY 24 H
	137	15	IRD4	M8522	AD CRY 36 H
	137	16	IRD4	M8522	ADX CRY 12 H
	137	17	IRD4	M8522	ADX CRY 24 H
	137	18	CON4	M8525	CON ARX 36 H
	137	19	CON1	M8525	CON VMA SEL 1 L
	137	20	CON3	M8525	CON SR 03 H
	137	21	CON2	M8525	CON NICOND 09 H
	137	22	CON2	M8525	CON COND ADR 10 H
	137	23	CON4	M8525	CON UCODE STATE 07 H
	137	24	CON5	M8525	CON PI DISMISS L
	140	00	CRA3	M8541	CRA DISP EN 00-07 L
	140	01	CRA3	M8541	CRA DISP EN 00-03 L
**	140	02	CRA4	M8541	CRA STACK ADR 10 H
**	140	03	CRA4	M8541	CRA STACK ADR 04 H
**	140	04	CRA4	M8541	CRA STACK ADR 02 H
**	140	05	CRA4	M8541	CRA STACK ADR 01 H
**	141	00	CRA4	M8541	CRA CALL, RESET H
**	141	01	CRA3	M8541	CRA DISP 00 H
**	141	02	CRA3	M8541	CRA DISP 01 H
**	141	03	CRA3	M8541	CRA DISP 02 H
**	141	04	CRA3	M8541	CRA DISP 03 H
**	141	05	CRA3	M8541	CRA DISP 04 H
**	142	00	CRA4	M8541	CRA SBR RET 05 H
**	142	01	CRA4	M8541	CRA SBR RET 06 H
**	142	02	CRA4	M8541	CRA SBR RET 07 H
**	142	03	CRA4	M8541	CRA SBR RET 08 H
**	142	04	CRA4	M8541	CRA SBR RET 09 H
**	142	05	CRA4	M8541	CRA SBR RET 10 H
	143	00	CRA3	M8541	CRA DISP EN 30-37 L
**	143	01	CRA4	M8541	CRA SBR RET 00 H
**	143	02	CRA4	M8541	CRA SBR RET 01 H
**	143	03	CRA4	M8541	CRA SBR RET 02 H
**	143	04	CRA4	M8541	CRA SBR RET 03 H
**	143	05	CRA4	M8541	CRA SBR RET 04 H
**	144	00	CRA1	M8541	CR ADR 05 F H
**	144	01	CRA1	M8541	CR ADR 06 F H
**	144	02	CRA2	M8541	CR ADR 07 F H
**	144	03	CRA2	M8541	CR ADR 08 F H
**	144	04	CRA2	M8541	CR ADR 09 F H
**	144	05	CRA2	M8541	CR ADR 10 F H
**	144	08	CRM5	M8548	CRAM 60 H
**	144	09	CRM5	M8548	CRAM PAR 1ST 00 H

KL10 (PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DP	BIT	DRAWING BOARD	NAME AND TRUTH
**	144	10	CRM5 M8548	CRAM 62 H
**	144	11	CRM5 M8548	CRAM PAR 00 H
**	144	14	CRM5 M8548	CRAM 64 H
**	144	15	CRM5 M8548	CRAM PAR 1ST 04 H
**	144	16	CRM5 M8548	CRAM 66 H
**	144	17	CRM5 M8548	CRAM PAR 04 H
**	144	20	CRM5 M8548	CRAM 68 H
**	144	21	CRM5 M8548	CRAM PAR 1ST 08 H
**	144	22	CRM5 M8548	CRAM 70 H
**	144	23	CRM5 M8548	CRAM PAR 08 H
**	144	26	CRM5 M8548	CRAM 72 H
**	144	27	CRM5 M8548	CRAM PAR 1ST 12 H
**	144	28	CRM5 M8548	CRAM 74 H
**	144	29	CRM5 M8548	CRAM PAR 12 H
**	144	32	CRM5 M8548	CRAM 76 H
**	144	33	CRM5 M8548	CRAM PAR 1ST 16 H
**	144	34	CRM5 M8548	CRAM 78 H
**	144	35	CRM5 M8548	CRAM PAR 16 H
**	145	00	CRA3 M8541	CRA DISP PARITY H
**	145	01	CRA1 M8541	CR ADR 00 F H
**	145	02	CRA1 M8541	CR ADR 01 F H
**	145	03	CRA1 M8541	CR ADR 02 F H
**	145	04	CRA1 M8541	CR ADR 03 F H
**	145	05	CRA1 M8541	CR ADR 04 F H
*	145	08-11	CRM5 M8548	CRAM 40-43 H
*	145	14-17	CRM5 M8548	CRAM 44-47 H
*	145	20-23	CRM5 M8548	CRAM 48-51 H
*	145	26-29	CRM5 M8548	CRAM 52-55 H
*	145	32-35	CRM5 M8548	CRAM 56-59 H
**	146	00	CRA3 M8541	CRA LOC 05 H
**	146	01	CRA3 M8541	CRA LOC 06 H
**	146	02	CRA3 M8541	CRA LOC 07 H
**	146	03	CRA3 M8541	CRA LOC 08 H
**	146	04	CRA3 M8541	CRA LOC 09 H
**	146	05	CRA3 M8541	CRA LOC 10 H
*	146	08-11	CRM5 M8548	CRAM 20-23 H
*	146	14-17	CRM5 M8548	CRAM 24-27 H
*	146	20-23	CRM5 M8548	CRAM 28-31 H
*	146	26-29	CRM5 M8548	CRAM 32-35 H
*	146	32-35	CRM5 M8548	CRAM 36-39 H
**	147	01	CRA3 M8541	CRA LOC 00 H
**	147	02	CRA3 M8541	CRA LOC 01 H
**	147	03	CRA3 M8541	CRA LOC 02 H
**	147	04	CRA3 M8541	CRA LOC 03 H
**	147	05	CRA3 M8541	CRA LOC 04 H
*	147	08-11	CRM5 M8548	CRAM 00-03 H
*	147	14-17	CRM5 M8548	CRAM 04-07 H
*	147	20-23	CRM5 M8548	CRAM 08-11 H
*	147	26-29	CRM5 M8548	CRAM 12-15 H
*	147	32-35	CRM5 M8548	CRAM 16-19 H

NOTE ABOUT READING VMA BOARD REGISTERS

THESE FORMULAS TERSELY DESCRIBE THE DIAGNOSTIC FUNCTION (150-157) AND EBUS BIT NUMBER (13-35, ODD) CORRESPONDING TO A REGISTER BIT 'B'.

[ ] MEANS "THE INTSEGER PART OF THE QUOTIENT"

REM ( ) MEANS "THE REMAINDER OF"

REGISTER	DIAG FUNC	FORMULA	FOR:
ADR BRK	153-REM(B/4)	4*[B/4]+3	EBUS BIT
PC	DITTO	4*[B/4]+1	
VMA	157-REM(B/4)	4*[B/4]+3	
VMA HELD	DITTO	4*[B/4]+1	

BETTER YET--SEE THE PRINTS!

150	11	VMA1	M8542	VMA1 VMA SECTION 0 L
151	11	VMA3	M8542	VMA3 PC SECTION 0 L
152	11	VMA4	M8542	VMA4 PCS SECTION 0 L
**	153	11	VMA4	M8542 VMA PREV SEC 17 H
153	13	VMA1	M8542	VMA1 MISC=0 L
**	153	15	VMA1	M8542 VMA1 LOCAL AC ADDRESS L
**	154	11	VMA4	M8542 VMA PREV SEC 16 H
**	155	11	VMA4	M8542 VMA PREV SEC 15 H
**	156	11	VMA4	M8542 VMA PREV SEC 14 H
**	157	11	VMA4	M8542 VMA PREV SEC 13 H
157	13	VMA1	M8542	VMA1 AC REF A L
157	15	VMA3	M8542	VMA3 MATCH 13-35 H

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KL10(PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
*	15X	13-35	VMA3	M8542 ADR BRK 13-35 H **NOTE
*	15X	13-35	VMA4	M8542 VMA HELD 13-35 H **NOTE
*	15X	13-35	VMA2	M8542 VMA 13-35 H **NOTE
*	15X	13-35	VMA3	M8542 PC 13-35 H **NOTE
	160	15	MB21	M8537 CORE BUSY H
	160	16	MB24	M8537 CHAN PAR ERR L
	160	17	SHD1	M8537 SH AR PAR ODD A H
	160	18	MB25	M8537 MB PAR BIT IN H
	160	19	MB21	M8537 CSH EN CSH DATA L
	160	20	MB21	M8537 MB IN SEL 1 H
	160	21	MB23	M8537 NXM ACKN H
	160	22	MB21	M8537 MB21 CHAN CORE BUSY H
	160	23	MB23	M8537 NXM ANY L
	160	24	MB24	M8537 MB24 NXM T6,7 L
	160	25	MB23	M8537 CHAN NXM ERR L
	160	26	PAG5	M8537 PAG MB 18-35 PAR H
	160	27	MBC5	M8531YA FORCE VALID MATCH 0 H
	160	28	MBC5	M8531YA FORCE VALID MATCH 1 H
	160	29	MBC5	M8531YA FORCE VALID MATCH 2 H
	160	30	MBC5	M8531YA FORCE VALID MATCH 3 H
	160	31	MBC1	M8531YA MBC1 WRITE OK H
	160	32	MBC2	M8531YA MBC2 CSH ADR WR PULSE H
	160	33	MBC2	M8531YA MBC2 CSH DATA CLR DONE IN L
	161	15	MB24	M8537 MBOX ADR PAR ERR L
	161	16	MB25	M8537 CBUS PAR LEFT TE H
	161	17	MEM5	M8537 MEM PAR IN H
	161	18	MB26	M8537 MB26 CSH PAR BIT H
	161	19	MB21	M8537 MEM TO C DIAG EN L
	161	20	MB21	M8537 MB IN SEL 2 H
	161	21	MB21	M8537 MB21 RD-FSE-WR REF L
	161	22	MB23	M8537 MBOX NXM ERR L
	161	23	MB23	M8537 MB23 CHAN MEM REF L
	161	24	MB24	M8537 MBOX SBUS ERR L
	161	25	MB23	M8537 NXM DATA VAL L
	161	26	MB26	M8537 CSH PAR BIT A H
	161	27	MBC2	M8531YA MBC2 CSH DATA CLR T1 L
	161	28	MBC2	M8531YA MBC2 CSH DATA CLR T2 L
	161	29	MBC2	M8531YA MBC2 CSH DATA CLR T3 L
	161	30	MBC2	M8531YA CSH SEL LRU H
	161	31	MBC2	M8531YA MBC2 CSH VAL WR PULSE H
	161	32	MBC2	M8531YA MBC2 CSH WR WR PULSE H
	161	33	MBC2	M8531YA RQ HOLD FF H
	162	15	MB24	M8537 CHAN ADR PAR ERR L
	162	16	MB25	M8537 CBUS PAR RIGHT TE H
	162	17	MB25	M8537 CSH PAR BIT IN H
	162	18	MB23	M8537 MB23 SEQUENTIAL RQ H
	162	19	MB21	M8537 CHAN READ L
	162	20	MB21	M8537 MB IN SEL 4 H
	162	21	MB21	M8537 MEM BUSY H
	162	22	MB23	M8537 MB23 HOLD ERA L
	162	23	MB24	M8537 MB24 NXM T2 H
	162	24	MB24	M8537 MBOX MB PAR ERR L
	162	25	PAG5	M8537 PAG MB 00-17 PAR H
	162	26	MB26	M8537 CSH PAR BIT B H
	162	27	MBC2	M8531YA MBC2 CACHE WR 00 A H
	162	28	MBC2	M8531YA MBC2 CACHE WR 09 A H
	162	29	MBC2	M8531YA MBC2 CACHE WR 18 A H
	162	30	MBC2	M8531YA MBC2 CACHE WR 27 A H
	162	31	MBC2	M8531YA SBUS ADR HOLD H
	162	32	MBC3	M8531YA MBC3 A CHANGE COMING A L
	162	33	MBC3	M8531YA MBC3 ANY SBUS RQ IN L
	163	27	MBC3	M8531YA MBC3 B CHANGE COMING L
	163	28	MBC5	M8531YA MBC5 CORE BUSY B H
	163	29	MBC3	M8531YA CSH VAL SEL ALL H
	163	30	MBC3	M8531YA CSH VAL WR DATA H
	163	31	MBC3	M8531YA CSH WR SEL ALL H
	163	32	MBC3	M8531YA CSH WR WR DATA H
	163	33	MBC3	M8531YA DATA VALID A OUT H
	164	27	MBC3	M8531YA DATA VALID B OUT H
	164	28	MBC3	M8531YA MBC3 INH 1ST MB REQ H
	164	29	MBC3	M8531YA MEM TO C EN L
	164	30	MBC3	M8531YA PHASE CHANGE COMING L
	164	31	MBC4	M8531YA ACKN PULSE L
	164	32	MBC4	M8531YA MBC4 CORE ADR 34 H
	164	33	MBC4	M8531YA MBC4 CORE ADR 35 H
	165	27	MBC1	M8531YA CAM SEL 1 H
	165	28	MBC1	M8531YA CAM SEL 2 H
	165	29	MBC4	M8531YA MBC4 CORE DATA VAL -1 L
	165	30	MBC4	M8531YA MBC4 CORE DATA VALID -2 L

KL10(PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
165	31	MBC4	M8531YA MBC4 CORE DATA VALID L
165	32	MBC4	M8531YA MBC4 CORE RD IN PROG A H
165	33	MBC4	M8531YA MEM ADR PAR H
166	27	MBC4	M8531YA MEM RD RQ 3 H
166	28	MBC4	M8531YA MEM RQ 0 H
166	29	MBC4	M8531YA MEM RQ 1 H
166	30	MBC4	M8531YA MEM RQ 2 H
166	31	MBC4	M8531YA MEM RQ 3 H
166	32	MBC4	M8531YA MBC4 MEM START L
166	33	MBC4	M8531YA MEM WR RQ L
*	00-08	MBZ2	M8537 EBUS REG 00-08 H
*	14-26	MBZ2	M8537 EBUS REG 14-26 H
*	27-33	MBC1	M8531YA EBUS REG 27-33 H
*	34,35	MBZ2	M8537 EBUS REG 34,35 H
**	00	CRC6	M8535 CRC CH BUF ADR 0 H
170	01	CRC4	M8535 CRC4 RESET IN L
170	02	CRC4	M8535 CRC MEM STORE ENA L
170	03	CRC4	M8535 CRC4 DONE IN H
170	04	CRC4	M8535 CRC4 STORE IN H
170	05	CCW4	M8534 CCW WD READY H
170	06	CCW6	M8534 CCW CCWF REQ ENA H
170	07	CCW6	M8534 CCW MEM STORE ENA H
170	08	CCW5	M8534 CCW ACT FLAG REQ ENA H
170	09	CCW3	M8534 CCW ALU C8 OUT H
170	10	CCW3	M8534 CCW ALU C2 OUT H
170	11	CHC1	M8533 CH TO H
170	12	CHC5	M8533 CBUS SEL 0 E H
170	13	CHC1	M8533 CHX RESET H
170	14	CHC2	M8533 CH RESET INTR H
170	16	CCL5	M8536 CCL ODD WC PAR H
170	18	CCL5	M8536 CCL5 WC GE4 H
170	19	CCL5	M8536 CCL WC=0 L
170	20	CHX2	M8515 CSH 0 ANY VAL L
170	21	CHX3	M8515 CSH USE IN 0 H
170	22	CSH5	M8513YA CSH5 PAGE REFILL COMP L
170	23	CSH6	M8513YA CSH6 CACHE WR IN H
170	24	CSH6	M8513YA CSH6 MBOX PT DIR WR L
170	25	CSH2	M8513YA CSH2 WR TEST L
170	26	CSH3	M8513YA CSH3 ANY VAL HOLD H
170	27	CSH4	M8513YA CSH4 DATA CLR DONE L
170	28	CSH4	M8513YA CSH REPILL RAM WR L
170	29	CSH4	M8513YA CSH4 EBOX T3 L
170	30	MBX1	M8529YA MBX1 CACHE BIT H
170	31	MBX1	M8529YA MBX1 CCA REQ L
170	32	MBX4	M8529YA CSH WR WD 2 EN H
170	33	MBX5	M8529YA MBX5 MB REQ IN H
170	34	MBX5	M8529YA MBX5 MEM TO C EN L
170	35	MBX5	M8529YA MBX5 RQ 1 IN H
**	00	CRC6	M8535 CRC CH BUF ADR 1 H
171	01	CRC4	M8535 CRC RH20 ERR IN H
171	02	CRC4	M8535 CRC OVN ERR IN H
171	03	CRC4	M8535 CRC SHORT WC ERR H
171	04	CRC4	M8535 CRC LONG WC ERR H
171	05	CCW4	M8534 CCW WD0 REQ H
171	06	CCW4	M8534 CCW WD1 REQ H
171	07	CCW4	M8534 CCW WD2 REQ H
171	08	CCW4	M8534 CCW WD3 REQ H
171	09	CCW1	M8534 CCW MEM ADR=0 H
171	10	CCW6	M8534 CCW CCWF WAITING H
171	11	CHC1	M8533 CH T1 H
171	12	CHC5	M8533 CBUS SEL 1 E H
171	13	CHC1	M8533 CHX START H
171	14	CHC2	M8533 CH START INTR H
171	16	CCL3	M8536 CCL3 MB RIP A H
171	18	CCL3	M8536 CCL ALU MINUS L
171	19	CCL4	M8536 CCL CH TEST MB PAR L
171	20	CHX2	M8515 CSH 1 ANY VAL L
171	21	CHX3	M8515 CSH USE IN 1 H
171	22	CSH5	M8513YA CSH5 CHAN RD T5 L
171	23	CSH6	M8513YA CSH6 WR DATA RDY L
171	24	CSH4	M8513YA CSH4 PAGE FAIL T2 L
171	25	CSH6	M8513YA CSH6 EBOX LOAD REG H
171	26	CSH7	M8513YA CSH7 FILL CACHE RD L
171	27	CSH5	M8513YA CSH5 CHAN WR T5 L
171	28	CSH3	M8513YA CSH3 MB WR RQ CLR NXT L
171	29	CSH4	M8513YA CSH4 EBOX T1 L
171	30	MBX2	M8529YA MBX2 CACHE TO MB 34 H
171	31	MBX1	M8529YA MBX1 CCA SEL 1 H
171	32	MBX4	M8529YA CSH WR WD 3 EN H
171	33	MBX2	M8529YA MB SEL 1 H

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KL10(PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	171	34	MBX3	M8529YA MEM DIAG L
	171	35	MBX5	M8529YA MBX5 RQ 2 IN H
**	172	00	CRC6	M8535 CRC CH BUF ADR 2 H
	172	01	CRC3	M8535 CRC READY IN H
	172	02	CRC3	M8535 CRC LAST WORD IN H
	172	03	CRC3	M8535 CRC ERR IN H
	172	04	CRC3	M8535 CRC REVERSE IN H
	172	05	CCW3	M8534 CCW ACT CTR 0 EN H
	172	06	CCW3	M8534 CCW ACT CTR 1 EN H
	172	07	CCW3	M8534 CCW ACT CTR 2 EN H
	172	08	CCW1	M8534 CCW BUF ADR 0 L
	172	09	CCW1	M8534 CCW BUF ADR 1 L
	172	10	CCW1	M8534 CCW BUF ADR 2 L
	172	11	CHC1	M8533 CH T2 H
	172	12	CHC5	M8533 CBUS SEL 2 E H
	172	13	CHC1	M8533 CHX DONE H
	172	14	CHC2	M8533 CH DONE INTR H
	172	16	CCL3	M8536 CCL3 CCWF T2 H
	172	18	CCL3	M8536 CCL3 MB REQ T2 H
	172	19	CCL4	M8536 CCL4 REVERSE H
	172	20	CHX2	M8515 CSH 2 ANY VAL L
	172	21	CHX3	M8515 CSH USE IN 2 H
	172	22	CSH6	M8513YA CSH6 CHAN WR CACHE L
	172	23	CSH6	M8513YA CSH6 CCA CYC DONE L
	172	24	CSH5	M8513YA CSH5 CHAN T4 L
	172	25	CHX3	M8513YA CSH LRU 2 H
	172	26	CSH1	M8513YA CSH1 READY TO GO A H
	172	27	CSH6	M8513YA CSH USE HOLD H
	172	28	CSH1	M8513YA CSH1 CCA CYC L
	172	29	CSH2	M8513YA CSH2 EBOX REQ EN L
	172	30	MBX2	M8529YA MBX2 CACHE TO MB 35 H
	172	31	MBX1	M8529YA MBX1 CCA SEL 2 H
	172	32	MBX1	M8529YA FORCE NO MATCH H
	172	33	MBX2	M8529YA MB SEL 2 H
	172	34	MBX5	M8529YA MBX5 MEM RD RQ IN H
	172	35	MBX5	M8529YA MBX5 RQ 3 IN H
**	173	00	CRC6	M8535 CRC CH BUF ADR 3 H
	173	01	CRC2	M8535 CRC2 ACT CTR 0R H
	173	02	CRC2	M8535 CRC2 ACT CTR 1R H
	173	03	CRC2	M8535 CRC2 ACT CTR 2R H
	173	04	CRC2	M8535 CRC2 RAM CYC H
**	173	05	CCW2	M8534 CCW CHA 30 H
**	173	06	CCW2	M8534 CCW CHA 31 H
**	173	07	CCW2	M8534 CCW CHA 32 H
**	173	08	CCW2	M8534 CCW CHA 33 H
**	173	09	CCW2	M8534 CCW CHA 34 H
**	173	10	CCW2	M8534 CCW CHA 35 H
	173	11	CHC1	M8533 CH T3 H
	173	12	CHC5	M8533 CBUS SEL 3 E H
	173	13	CHC1	M8533 CHX STORE H
	173	14	CHC2	M8533 CH STORE H
	173	16	CCL4	M8536 CCL CH MB SEL 2 H
	173	18	CCL4	M8536 CCL CH MB SEL 1 H
	173	19	CCL3	M8536 CCL AF T2 L
	173	20	CHX2	M8515 CSH 3 ANY VAL L
	173	21	CHX3	M8515 CSH USE IN 3 H
	173	22	CSH2	M8513YA CSH2 ONE WORD RD A L
	173	23	CSH2	M8513YA CSH2 MBOX RESP L
	173	24	CSH2	M8513YA CSH2 RD PSE 2ND REQ EN L
	173	25	CHX3	M8513YA CSH LRU 1 H
	173	26	CSH5	M8513YA CSH5 T1 L
	173	27	CSH4	M8513YA CSH4 WRITEBACK T1 A H
	173	28	CSH7	M8513YA CSH7 CCA WRITEBACK L
	173	29	CSH4	M8513YA CSH4 EBOX T2 L
	173	30	MBX4	M8529YA MBX4 CACHE TO MB DONE H
	173	31	MBX2	M8529YA MBX2 CHAN WR CYC L
	173	32	MBX3	M8529YA MEM DATA TO MEM H
	173	33	MBX2	M8529YA MB SEL HOLD H
	173	34	MBX3	M8529YA MEM TO C SEL 1 H
	173	35	MBX2	M8529YA SBUS ADR 34 H
**	174	00	CRC6	M8535 CRC CH BUF ADR 4 H
	174	01	CRC1	M8535 CRC1 ACT FLAG ENA H
	174	02	CRC5	M8535 CRC WR RAM L
	174	03	CRC3	M8535 CRC3 OP CODE 00 H
	174	04	CRC3	M8535 CRC3 OP CODE 01 H
*	174	05-10	CCW2	M8534 CCW CHA 24-29 H
	174	11	CHC1	M8533 CBUS READY E H
	174	12	CHC5	M8533 CBUS SEL 4 E H
	174	13	CHC1	M8533 CHX CTOM H
	174	14	CHC3	M8533 CH CTOM H

KL10 (PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
174	16	CCL3	M8536	CCL CHAN REQ H
174	18	CCL3	M8536	CCL CHAN EPT H
174	19	CCL4	M8536	CCL CHAN TO MEM H
174	20	CHX4	M8515	CSH DIR 0 PAR ODD H
174	21	CHX3	M8515	CSH USE IN 4 H
174	22	CSH2	M8513YA	CSH2 E CORE RD RQ A L
174	23	CSH6	M8513YA	CSH6 PAGE FAIL HOLD L
174	24	CSH5	M8513YA	CSH5 PAGE REFILL T9,12 L
174	25	CHA3	M8513YA	CSH 3 ANY WR L
174	26	CSH5	M8513YA	CSH5 CSH TO L
174	27	CSH3	M8513YA	CSH3 ADR PMA EN H
174	28	CSH1	M8513YA	CSH1 EBOX CYC B L
174	29	CSH1	M8513YA	CSH1 CACHE IDLE L
174	30	MBX4	M8529YA	MBX4 CACHE TO MB T2 L
174	31	MBX1	M8529YA	MBX1 CSH CCA INVAL CSH H
174	32	MBX3	M8529YA	MB DATA CODE 1 H
174	33	MBX6	M8529YA	MB0 HOLD IN H
174	34	MBX3	M8529YA	MEM TO C SEL 2 H
174	35	MBX2	M8529YA	SBUS ADR 35 H
**	175	00	CRC6	M8535 CRC CH BUF ADR 5 H
175	01	CRC6	M8535	CRC SEL 1D L
175	02	CRC6	M8535	CRC SEL 2D L
175	03	CRC6	M8535	CRC SEL 4D L
175	04	CRC1	M8535	CRC1 AP REQ ENA L
*	175	05-10	CCW2	M8534 CCW CHA 18-23 H
175	11	CHC1	M8533	CBUS LAST WORD E H
175	12	CHC5	M8533	CBUS SEL 5 E H
175	13	CHC5	M8533	CH SEL 8A H
175	14	CHC2	M8533	CH CONTR REQ H
175	16	CCL2	M8536	CCL CCWF REQ H
175	18	CCL2	M8536	CCL2 ACT FLAG REQ H
175	19	CCL2	M8536	CCL MEM STORE REQ H
175	20	CHX4	M8515	CSH DIR 1 PAR ODD H
175	21	CHX3	M8515	CSH USE ADR 2 H
175	22	CSH2	M8513YA	CSH2 EBOX RETRY REQ L
175	23	CSH6	M8513YA	CSH USE WR EN H
175	24	CSH3	M8513YA	MB TEST PAR A IN L
175	25	CHA3	M8513YA	CSH 1 ANY WR L
175	26	CSH5	M8513YA	CSH5 T3 L
175	27	CSH3	M8513YA	CSH3 GATE VMA 27-33 H
175	28	CSH1	M8513YA	CSH1 MB CYC L
175	29	CSH4	M8513YA	CSH4 ONE WORD WR TO L
175	30	MBX4	M8529YA	MBX4 CACHE TO MB T3 L
175	31	MBX1	M8529YA	MBX1 CSH CCA VAL CORE H
175	32	MBX3	M8529YA	MB DATA CODE 2 H
175	33	MBX6	M8529YA	MB1 HOLD IN H
175	34	MBX5	M8529YA	MBX5 MEM WR RQ IN H
175	35	MBX3	M8529YA	MBX3 SBUS DIAG 3 L
**	176	00	CRC6	M8535 CRC CH BUF ADR 6 H
176	01	CRC1	M8535	CRC1 MEM PTR0 H
176	02	CRC1	M8535	CRC1 MEM PTR1 H
176	03	CRC1	M8535	CRC1 MEM PTR2 H
176	04	CRC1	M8535	CRC1 MEM PTR3 H
176	05	CCW3	M8534	CCL WC=3 H
176	06	CCW4	M8534	CCL CCW REG LOAD H
176	07-10	CCW2	M8534	CCW CHA 14-17 H
176	11	CHC1	M8533	CBUS ERROR E H
176	12	CHC5	M8533	CBUS SEL 6 E H
176	13	CHC1	M8533	CH MB REQ INH H
176	14	CHC1	M8533	CH REVERSE H
176	16	CCL4	M8536	CCL4 STORE CCW H
176	18	CCL2	M8536	CCL BUF ADR 3 H
176	19	CCL4	M8536	CCL START MEM L
176	20	CHX4	M8515	CSH DIR 2 PAR ODD H
176	21	CHX3	M8515	CSH USE ADR 3 H
176	22	CSH6	M8513YA	CSH6 CCA INVAL T4 L
176	23	CSH5	M8513YA	CSH5 PAGE REFILL T8 L
176	24	CSH4	M8513YA	CSH4 EBOX TO L
176	25	CHA3	M8513YA	CSH 2 ANY WR L
176	26	CSH5	M8513YA	CSH5 T2 L
176	27	CSH2	M8513YA	CSH2 E CACHE WR CYC H
176	28	CSH7	M8513YA	CSH7 E WRITEBACK L
176	29	CSH5	M8513YA	CSH5 PAGE REFILL T4 L
176	30	MBX4	M8529YA	MBX4 CACHE TO MB T4 A L
176	31	MBX4	M8529YA	CSH WR WD 0 EN H
176	32	MBX3	M8529YA	MB PAR H
176	33	MBX6	M8529YA	MB2 HOLD IN H
176	34	MBX3	M8529YA	MBX3 REFILL HOLD H
176	35	MBX3	M8529YA	MBX3 SBUS DIAG CYC L
177	00	CRC1	M8535	CRC1 PTR DIP=0 H

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KL10(PV) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
177	01	CRC6 M8535	CRC6 CH ADR 0C L
177	02	CRC6 M8535	CRC6 CH ADR 1C L
177	03	CRC6 M8535	CRC6 CH ADR 2C L
177	04	CRC6 M8535	CRC6 CH ADR 3C L
177	05	CCW6 M8534	CCW RAM ADR 1 H
177	06	CCW6 M8534	CCW RAM ADR 2 H
177	07	CCW6 M8534	CCW RAM ADR 4 H
177	08	CCW3 M8534	CCL WC=1 H
177	09	CCW3 M8534	CCL WC=2 H
177	10	CCW4 M8534	CCW ODD ADR PAR H
177	11	CHC1 M8533	CH CBUS REQ H
177	12	CHC5 M8533	CBUS SEL 7 E H
177	13	CHC2 M8533	CH CONTR CYC H
177	14	CHC2 M8533	CH START H
177	16	CCL1 M8536	CCL1 ERR REQ H
177	18	CCL6 M8536	CCL6 CSH CHAN CYC L
177	19	CCL3 M8536	CCL3 MEM PTR EN H
177	20	CHX4 M8515	CSH DIR 3 PAR ODD H
177	21	CHX3 M8515	CSH USE ADR 4 H
177	22	CSH6 M8513YA	CSH6 PAGE REFILL ERROR L
177	23	CSH6 M8513YA	CSH6 DATA DLY 1 L
177	24	CSH4 M8513YA	CSH4 PAGE FAIL DLY H
177	25	CHA3 M8513YA	CSH 0 ANY WR L
177	26	CSH5 M8513YA	CSH5 PAGE REFILL T10 L
177	27	CSH1 M8513YA	CSH1 CYC TYPE HOLD H
177	28	CSH2 M8513YA	CSH2 RD PAUSE 2ND HALF L
177	29	CSH4 M8513YA	CSH4 EBOX WR T4 L
177	30	MBX1 M8529YA	MBX1 CCA ALL PAGES CYC H
177	31	MBX4 M8529YA	CSH WR WD 1 EN H
177	32	MBX2 M8529YA	MB REQ HOLD H
177	33	MBX6 M8529YA	MB3 HOLD IN H
177	34	MBX5 M8529YA	MBX5 RQ 0 IN H
177	35	MBX4 M8529YA	MBX4 WRITEBACK T2 L

NOTE

TRACON and the 11-based 10 diagnostic programs interpret all diagnostic read functions which are not preceded with either a single or double asterisk [(\*) or (\*\*)] as single bits; as such, they are printed out by bit position and/or name. Diagnostic read functions preceded by a single asterisk (\*) are interpreted as registers and are printed out as such. Diagnostic read functions which are preceded by a double asterisk (\*\*) may be interpreted and printed as either single bits or as a register depending on the program doing the interpretation.



KL10(PV) DIAGNOSTIC READ FUNCTION CODES SORTED ALPHABETICALLY

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	164	31	MBC4	M8531YA ACKN PULSE L
*	127	0-35	EDP3	M8512 AD 0 TO 35 H
	136	17	IRD4	M8522 AD CRY -02 A H
	132	06	IRD4	M8524 AD CRY -02 A L
	131	05	EDP3	M8524 AD CRY 01 L
	137	12	IRD4	M8522 AD CRY 12 H
	137	13	IRD4	M8522 AD CRY 18 H
	137	14	IRD4	M8522 AD CRY 24 H
	137	15	IRD4	M8522 AD CRY 36 H
	132	05	EDP3	M8524 AD OVERFLOW 00 L
	136	12	IRD3	M8522 AD=0 L
*	15X	13-35	VMA3	M8542 ADR BRK 13-35 H **NOTE
	126	0-35	EDP3	M8512 ADX 0 TO 35 H
	137	16	IRD4	M8522 ADX CRY 12 H
	137	17	IRD4	M8522 ADX CRY 24 H
	116	11	APR2	M8545 APR ANY EBOX ERR FLG H
	115	10	APR3	M8545 APR EBOX DISABLE CS H
	115	13	APR6	M8545 APR EBOX ERA H
	116	10	APR3	M8545 APR EBUS F01 E H
	116	09	APR3	M8545 APR EBUS REQ L
	115	09	APR3	M8545 APR EBUS RETURN H
	116	13	APR6	M8545 APR EN REFILL RAM WR H
	114	16	APR3	M8545 APR FM 36 H
**	114	14	APR4	M8545 APR FM ADR 1 H
**	114	11	APR4	M8545 APR FM ADR 10 H
**	114	13	APR4	M8545 APR FM ADR 2 H
**	114	12	APR4	M8545 APR FM ADR 4 H
**	114	10	APR5	M8545 APR FM BLOCK 1 H
**	114	09	APR5	M8545 APR FM BLOCK 2 H
**	114	08	APR5	M8545 APR FM BLOCK 4 H
	114	07	APR5	M8545 APR MBOX CTL 03 H
	115	07	APR5	M8545 APR MBOX CTL 06 H
	112	08	APR1	M8545 APR1 I/O PF ERR EN IN H
	110	08	APR1	M8545 APR1 I/O PF ERR IN H
	112	09	APR1	M8545 APR1 MB PAR ERR EN IN H
	110	09	APR1	M8545 APR1 MB PAR ERR IN H
	112	07	APR1	M8545 APR1 NXM ERR EN IN H
	110	07	APR1	M8545 APR1 NXM ERR IN H
	112	06	APR1	M8545 APR1 SBUS ERR EN IN H
	110	06	APR1	M8545 APR1 SBUS ERR IN H
	110	01	APR1	M8545 APR1 SWEEP BUSY EN H
	110	14	APR2	M8545 APR2 APR INTERRUPT H
	112	10	APR2	M8545 APR2 C DIR P ERR EN IN H
	110	10	APR2	M8545 APR2 C DIR P ERR IN H
	112	12	APR2	M8545 APR2 PWR FAIL EN IN H
	110	12	APR2	M8545 APR2 PWR FAIL IN H
	112	11	APR2	M8545 APR2 S ADR P ERR EN IN H
	110	11	APR2	M8545 APR2 S ADR P ERR IN H
	112	13	APR2	M8545 APR2 SWEEP DONE EN IN H
	110	13	APR2	M8545 APR2 SWEEP DONE IN H
	115	11	APR2	M8545 APR2 WR BAD ADR PAR L
	117	10	APR3	M8545 APR3 EBOX SEND F02 H
	117	09	APR3	M8545 APR3 EBUS DEMAND H
	113	09	APR3	M8545 APR3 FETCH COMP H
	111	13	APR3	M8545 APR3 FM EXTENDED H
	114	17	APR3	M8545 APR3 FM ODD PARITY H
	113	10	APR3	M8545 APR3 READ COMP H
	113	12	APR3	M8545 APR3 USER COMP H
	113	11	APR3	M8545 APR3 WRITE COMP H
	111	14	APR4	M8545 APR4 AC+# 09 H
	111	15	APR4	M8545 APR4 AC+# 10 H
	111	16	APR4	M8545 APR4 AC+# 11 H
	111	17	APR4	M8545 APR4 AC+# 12 H
	114	15	APR4	M8545 APR4 F02 EN H
	111	08	APR5	M8545 APR5 CURRENT BLOCK 1 H
	111	07	APR5	M8545 APR5 CURRENT BLOCK 2 H
	111	06	APR5	M8545 APR5 CURRENT BLOCK 4 H
	111	11	APR5	M8545 APR5 PREV BLOCK 1 H
	111	10	APR5	M8545 APR5 PREV BLOCK 2 H
	111	09	APR5	M8545 APR5 PREV BLOCK 4 H
	116	08	APR5	M8545 APR5 PT DIR WR L
	117	08	APR5	M8545 APR5 PT WR L
	115	08	APR5	M8545 APR5 SET PAGE FAIL L
	116	07	APR5	M8545 APR5 WR PT SEL 0 H
	117	07	APR5	M8545 APR5 WR PT SEL 1 H
	115	12	APR6	M8545 APR6 EBOX CCA H
	117	12	APR6	M8545 APR6 EBOX EBR H
	115	16	APR6	M8545 APR6 EBOX LOAD REG L
	115	17	APR6	M8545 APR6 EBOX READ REG L

KL10 (PV) DIAGNOSTIC READ FUNCTION CODES  
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DP	BIT	DRAWING BOARD	NAME AND TRUTH
115	14	APR6 M8545	APR6 EBOX SBUS DIAG H
117	13	APR6 M8545	APR6 EBOX SPARE H
116	12	APR6 M8545	APR6 EBOX UBR H
*	120	12-35 EDP1 M8512	AR 12 TO 35 H
*	125	0-35 EDP2 M8512	ARX 0 TO 35 H
*	121	0-35 EDP4 M8512	BR 0 TO 35 H
*	124	0-35 EDP4 M8512	BRX 0 TO 35 H
165	27	MBCL M8531YA	CAM SEL 1 H
165	28	MBCL M8531YA	CAM SEL 2 H
176	11	CHC1 M8533	CBUS ERROR E H
175	11	CHC1 M8533	CBUS LAST WORD E H
161	16	MBZ5 M8537	CBUS PAR LEFT TE H
162	16	MBZ5 M8537	CBUS PAR RIGHT TE H
174	11	CHC1 M8533	CBUS READY E H
170	12	CHC5 M8533	CBUS SEL 0 E H
171	12	CHC5 M8533	CBUS SEL 1 E H
172	12	CHC5 M8533	CBUS SEL 2 E H
173	12	CHC5 M8533	CBUS SEL 3 E H
174	12	CHC5 M8533	CBUS SEL 4 E H
175	12	CHC5 M8533	CBUS SEL 5 E H
176	12	CHC5 M8533	CBUS SEL 6 E H
177	12	CHC5 M8533	CBUS SEL 7 E H
173	19	CCL3 M8536	CCL AP T2 L
171	18	CCL3 M8536	CCL ALU MINUS L
176	18	CCL2 M8536	CCL BUF ADR 3 H
176	06	CCW4 M8534	CCL CCW REG LOAD H
175	16	CCL2 M8536	CCL CCWP REQ H
173	18	CCL4 M8536	CCL CH MB SEL 1 H
173	16	CCL4 M8536	CCL CH MB SEL 2 H
171	19	CCL4 M8536	CCL CH TEST MB PAR L
174	18	CCL3 M8536	CCL CHAN EPT H
174	16	CCL3 M8536	CCL CHAN REQ H
174	19	CCL4 M8536	CCL CHAN TO MEM H
175	19	CCL2 M8536	CCL MEM STORE REQ H
170	16	CCL5 M8536	CCL ODD WC PAR H
176	19	CCL4 M8536	CCL START MEM L
170	19	CCL5 M8536	CCL WC=0 L
177	08	CCW3 M8534	CCL WC=1 H
177	09	CCW3 M8534	CCL WC=2 H
176	05	CCW3 M8534	CCL WC=3 H
177	16	CCL1 M8536	CCL1 ERR REQ H
175	18	CCL2 M8536	CCL2 ACT FLAG REQ H
172	16	CCL3 M8536	CCL3 CCWF T2 H
172	18	CCL3 M8536	CCL3 MB REQ T2 H
171	16	CCL3 M8536	CCL3 MB RIP A H
177	19	CCL3 M8536	CCL3 MEM PTR EN H
172	19	CCL4 M8536	CCL4 REVERSE H
176	16	CCL4 M8536	CCL4 STORE CCW H
170	18	CCL5 M8536	CCL5 WC GE4 H
177	18	CCL6 M8536	CCL6 CSH CHAN CYC L
172	05	CCW3 M8534	CCW ACT CTR 0 EN H
172	06	CCW3 M8534	CCW ACT CTR 1 EN H
172	07	CCW3 M8534	CCW ACT CTR 2 EN H
170	08	CCW5 M8534	CCW ACT FLAG REQ ENA H
170	10	CCW3 M8534	CCW ALU C2 OUT H
170	09	CCW3 M8534	CCW ALU C8 OUT H
172	08	CCW1 M8534	CCW BUF ADR 0 L
172	09	CCW1 M8534	CCW BUF ADR 1 L
172	10	CCW1 M8534	CCW BUF ADR 2 L
170	06	CCW6 M8534	CCW CCWF REQ ENA H
171	10	CCW6 M8534	CCW CCWF WAITING H
*	176	07-10 CCW2 M8534	CCW CHA 14-17 H
*	175	05-10 CCW2 M8534	CCW CHA 18-23 H
*	174	05-10 CCW2 M8534	CCW CHA 24-29 H
**	173	05 CCW2 M8534	CCW CHA 30 H
**	173	06 CCW2 M8534	CCW CHA 31 H
**	173	07 CCW2 M8534	CCW CHA 32 H
**	173	08 CCW2 M8534	CCW CHA 33 H
**	173	09 CCW2 M8534	CCW CHA 34 H
**	173	10 CCW2 M8534	CCW CHA 35 H
171	09	CCW1 M8534	CCW MEM ADR=0 H
170	07	CCW6 M8534	CCW MEM STORE ENA H
177	10	CCW4 M8534	CCW ODD ADR PAR H
177	05	CCW6 M8534	CCW RAM ADR 1 H
177	06	CCW6 M8534	CCW RAM ADR 2 H
177	07	CCW6 M8534	CCW RAM ADR 4 H
170	05	CCW4 M8534	CCW WD READY H
171	05	CCW4 M8534	CCW WDO REQ H
171	06	CCW4 M8534	CCW WDI REQ H

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DF	BIT	DRAWING	BOARD	NAME AND TRUTH	
171	07	CCW4	M8534	CCW WD2 REQ H	
171	08	CCW4	M8534	CCW WD3 REQ H	
177	11	CHC1	M8533	CH CBUS REQ H	
177	13	CHC2	M8533	CH CONTR CYC H	
175	14	CHC2	M8533	CH CONTR REQ H	
174	14	CHC3	M8533	CH CTOM H	
172	14	CHC2	M8533	CH DONE INTR H	
176	13	CHC1	M8533	CH MB REQ INH H	
170	14	CHC2	M8533	CH RESET INTR H	
176	14	CHC1	M8533	CH REVERSE H	
175	13	CHC5	M8533	CH SEL 8A H	
177	14	CHC2	M8533	CH START H	
171	14	CHC2	M8533	CH START INTR H	
173	14	CHC2	M8533	CH STORE H	
170	11	CHC1	M8533	CH T0 H	
171	11	CHC1	M8533	CH T1 H	
172	11	CHC1	M8533	CH T2 H	
173	11	CHC1	M8533	CH T3 H	
162	15	MB24	M8537	CHAN ADR PAR ERR L	
160	25	MB23	M8537	CHAN NXM ERR L	
160	16	MB24	M8537	CHAN PAR ERR L	
162	19	MB21	M8537	CHAN READ L	
174	13	CHC1	M8533	CHX CTOM H	
172	13	CHC1	M8533	CHX DONE H	
170	13	CHC1	M8533	CHX RESET H	
171	13	CHC1	M8533	CHX START H	
173	13	CHC1	M8533	CHX STORE H	
102	32	CLK4	M8526YA	CLK EBOX REQ H	
100	30	CLK1	M8526YA	CLK EBUS CLK H	
102	30	CLK1	M8526YA	CLK ERROR STOP H	
102	35	CLK4	M8526YA	CLK PORCE 1777 H	
100	32	CLK4	M8526YA	CLK INSTR 1777 H	
103	32	CLK4	M8526YA	CLK MB XFER H	
103	34	CLK4	M8526YA	CLK PAGE ERROR H	
100	31	CLK1	M8526YA	CLK SBUS CLK H	
103	31	CLK2	M8526YA	CLK2 BURST L	
104	31	CLK2	M8526YA	CLK2 EBOX SS L	
102	31	CLK2	M8526YA	CLK2 GO L	
104	30	CLK3	M8526YA	CLK3 CRAM PAR ERR H	
103	30	CLK3	M8526YA	CLK3 DRAM PAR ERR H	
104	33	CLK3	M8526YA	CLK3 EBOX SOURCE H	
107	30	CLK3	M8526YA	CLK3 ERROR L	
105	30	CLK3	M8526YA	CLK3 FM PAR ERR H	
106	30	CLK3	M8526YA	CLK3 FS ERROR H	
102	33	CLK3	M8526YA	CLK3 SYNC H	
103	35	CLK4	M8526YA	CLK4 1777 EN H	
103	33	CLK4	M8526YA	CLK4 EBOX CLK L	
102	34	CLK4	M8526YA	CLK4 PAGE FAIL EN L	
107	31	CLK4	M8526YA	CLK4 PAGE FAIL H	
106	35	CLK5	M8526YA	CLK5 AR/ARX PAR CHECK L	
**	101	35	CLK5	M8526YA	CLK5 BURST 01 H
**	101	34	CLK5	M8526YA	CLK5 BURST 02 H
**	101	33	CLK5	M8526YA	CLK5 BURST 04 H
**	101	32	CLK5	M8526YA	CLK5 BURST 08 H
**	100	34	CLK5	M8526YA	CLK5 BURST 128 H
**	101	31	CLK5	M8526YA	CLK5 BURST 16 H
**	101	30	CLK5	M8526YA	CLK5 BURST 32 H
**	100	35	CLK5	M8526YA	CLK5 BURST 64 H
100	33	CLK5	M8526YA	CLK5 BURST CNT=0 H	
105	34	CLK5	M8526YA	CLK5 CRAM PAR CHECK L	
106	34	CLK5	M8526YA	CLK5 DRAM PAR CHECK L	
105	33	CLK5	M8526YA	CLK5 EBOX CRM DIS H	
107	33	CLK5	M8526YA	CLK5 EBOX CTL DIS H	
106	33	CLK5	M8526YA	CLK5 EBOX EDP DIS H	
107	35	CLK5	M8526YA	CLK5 ERR STOP EN L	
104	34	CLK5	M8526YA	CLK5 FM PAR CHECK L	
107	34	CLK5	M8526YA	CLK5 FS CHECK L	
104	35	CLK5	M8526YA	CLK5 MBOX CYCLE DIS H	
105	35	CLK5	M8526YA	CLK5 MBOX RESP SIM L	
107	32	CLK5	M8526YA	CLK5 RATE SEL 1 H	
106	32	CLK5	M8526YA	CLK5 RATE SEL 2 H	
105	32	CLK5	M8526YA	CLK5 SOURCE SEL 1 H	
104	32	CLK5	M8526YA	CLK5 SOURCE SEL 2 H	
136	18	CON4	M8525	CON AR 36 H	
137	18	CON4	M8525	CON ARX 36 H	
133	23	CON4	M8525	CON ARX LOADED L	
131	19	CON3	M8525	CON CACHE LOAD EN H	
133	05	CON2	M8524	CON CLR PRIVATE INSTR H	
137	22	CON2	M8525	CON COND ADR 10 H	

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KL10(PV) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
132	18	CON1	M8525 CON COND EN 00-07 L
133	22	CON2	M8525 CON COND INSTR ABORT H
134	19	CON1	M8525 CON COND/LOAD VMA HELD H
132	20	CON1	M8525 CON COND/MBOX CTL L
132	19	CON1	M8525 CON COND/SEL VMA L
133	19	CON1	M8525 CON COND/VMA GETS # H
135	18	CON3	M8525 CON DELAY REQ H
133	20	CON3	M8525 CON EBUS REL H
117	11	CON5	M8545 CON FM WRITE PAR L
134	24	CON5	M8525 CON FM WRITE PAR L
136	24	CON5	M8525 CON FM XFER L
131	21	CON3	M8525 CON KI10 PAGING MODE L
134	22	CON2	M8525 CON LOAD ACCESS COND H
136	22	CON2	M8525 CON LOAD DRAM H
132	22	CON2	M8525 CON LOAD IR L
135	19	CON1	M8525 CON LOAD SPEC INSTR L
132	21	CON2	M8525 CON LONG EN L
135	24	CON5	M8525 CON MBOX WAIT L
135	21	CON2	M8525 CON NICOND 07 H
136	21	CON2	M8525 CON NICOND 08 H
137	21	CON2	M8525 CON NICOND 09 H
134	21	CON2	M8525 CON NICOND TRAP EN H
133	21	CON4	M8525 CON PC+1 INH L
134	04	CON5	M8524 CON PI CYCLE A L
137	24	CON5	M8525 CON PI DISMISS L
133	18	CON1	M8525 CON SKIP EN 40-47 L
134	18	CON1	M8525 CON SKIP EN 50-57 L
134	20	CON3	M8525 CON SR 00 H
135	20	CON3	M8525 CON SR 01 H
136	20	CON3	M8525 CON SR 02 H
137	20	CON3	M8525 CON SR 03 H
131	22	CON3	M8525 CON TRAP EN H
134	23	CON4	M8525 CON UCODE STATE 01 H
135	23	CON4	M8525 CON UCODE STATE 03 H
136	23	CON4	M8525 CON UCODE STATE 05 H
137	23	CON4	M8525 CON UCODE STATE 07 H
137	19	CON1	M8525 CON VMA SEL 1 L
136	19	CON1	M8525 CON VMA SEL 2 L
130	18	CON3	M8525 CON WR EVEN PAR ADR H
135	22	CON2	M8525 CON2 INSTR GO L
131	18	CON3	M8525 CON3 CACHE LOOK EN H
130	19	CON3	M8525 CON3 WR EVEN PAR DATA H
130	20	CON3	M8525 CON3 WR EVEN PAR DIR H
132	23	CON4	M8525 CON4 AR LOADED H
133	24	CON5	M8525 CON5 MEM CYCLE L
132	24	CON5	M8525 CON5 PI CYCLE H
**	160	MBZ1	M8537 CORE BUSY H
**	145	01	CRA1 M8541 CR ADR 00 F H
**	145	02	CRA1 M8541 CR ADR 01 F H
**	145	03	CRA1 M8541 CR ADR 02 F H
**	145	04	CRA1 M8541 CR ADR 03 F H
**	145	05	CRA1 M8541 CR ADR 04 F H
**	144	00	CRA1 M8541 CR ADR 05 F H
**	144	01	CRA1 M8541 CR ADR 06 F H
**	144	02	CRA2 M8541 CR ADR 07 F H
**	144	03	CRA2 M8541 CR ADR 08 F H
**	144	04	CRA2 M8541 CR ADR 09 F H
**	144	05	CRA2 M8541 CR ADR 10 F H
**	141	00	CRA4 M8541 CRA CALL, RESET H
**	141	01	CRA3 M8541 CRA DISP 00 H
**	141	02	CRA3 M8541 CRA DISP 01 H
**	141	03	CRA3 M8541 CRA DISP 02 H
**	141	04	CRA3 M8541 CRA DISP 03 H
**	141	05	CRA3 M8541 CRA DISP 04 H
**	140	01	CRA3 M8541 CRA DISP EN 00-03 L
**	140	00	CRA3 M8541 CRA DISP EN 00-07 L
**	143	00	CRA3 M8541 CRA DISP EN 30-37 L
**	145	00	CRA3 M8541 CRA DISP PARITY H
**	147	01	CRA3 M8541 CRA LOC 00 H
**	147	02	CRA3 M8541 CRA LOC 01 H
**	147	03	CRA3 M8541 CRA LOC 02 H
**	147	04	CRA3 M8541 CRA LOC 03 H
**	147	05	CRA3 M8541 CRA LOC 04 H
**	146	00	CRA3 M8541 CRA LOC 05 H
**	146	01	CRA3 M8541 CRA LOC 06 H
**	146	02	CRA3 M8541 CRA LOC 07 H
**	146	03	CRA3 M8541 CRA LOC 08 H
**	146	04	CRA3 M8541 CRA LOC 09 H
**	146	05	CRA3 M8541 CRA LOC 10 H

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DF	BIT	DRAWING BOARD	NAME AND TRUTH
**	143	01 CRA4 M8541	CRA SBR RET 00 H
**	143	02 CRA4 M8541	CRA SBR RET 01 H
**	143	03 CRA4 M8541	CRA SBR RET 02 H
**	143	04 CRA4 M8541	CRA SBR RET 03 H
**	143	05 CRA4 M8541	CRA SBR RET 04 H
**	142	00 CRA4 M8541	CRA SBR RET 05 H
**	142	01 CRA4 M8541	CRA SBR RET 06 H
**	142	02 CRA4 M8541	CRA SBR RET 07 H
**	142	03 CRA4 M8541	CRA SBR RET 08 H
**	142	04 CRA4 M8541	CRA SBR RET 09 H
**	142	05 CRA4 M8541	CRA SBR RET 10 H
**	140	05 CRA4 M8541	CRA STACK ADR 01 H
**	140	04 CRA4 M8541	CRA STACK ADR 02 H
**	140	03 CRA4 M8541	CRA STACK ADR 04 H
**	140	02 CRA4 M8541	CRA STACK ADR 10 H
*	147	08-11 CRM5 M8548	CRAM 00-03 H
*	147	14-17 CRM5 M8548	CRAM 04-07 H
*	147	20-23 CRM5 M8548	CRAM 08-11 H
*	147	26-29 CRM5 M8548	CRAM 12-15 H
*	147	32-35 CRM5 M8548	CRAM 16-19 H
*	146	08-11 CRM5 M8548	CRAM 20-23 H
*	146	14-17 CRM5 M8548	CRAM 24-27 H
*	146	20-23 CRM5 M8548	CRAM 28-31 H
*	146	26-29 CRM5 M8548	CRAM 32-35 H
*	146	32-35 CRM5 M8548	CRAM 36-39 H
*	145	08-11 CRM5 M8548	CRAM 40-43 H
*	145	14-17 CRM5 M8548	CRAM 44-47 H
*	145	20-23 CRM5 M8548	CRAM 48-51 H
*	145	26-29 CRM5 M8548	CRAM 52-55 H
*	145	32-35 CRM5 M8548	CRAM 56-59 H
**	144	08 CRM5 M8548	CRAM 60 H
**	144	10 CRM5 M8548	CRAM 62 H
**	144	14 CRM5 M8548	CRAM 64 H
**	144	16 CRM5 M8548	CRAM 66 H
**	144	20 CRM5 M8548	CRAM 68 H
**	144	22 CRM5 M8548	CRAM 70 H
**	144	26 CRM5 M8548	CRAM 72 H
**	144	28 CRM5 M8548	CRAM 74 H
**	144	32 CRM5 M8548	CRAM 76 H
**	144	34 CRM5 M8548	CRAM 78 H
**	144	11 CRM5 M8548	CRAM PAR 00 H
**	144	17 CRM5 M8548	CRAM PAR 04 H
**	144	23 CRM5 M8548	CRAM PAR 08 H
**	144	29 CRM5 M8548	CRAM PAR 12 H
**	144	35 CRM5 M8548	CRAM PAR 16 H
**	144	09 CRM5 M8548	CRAM PAR 1ST 00 H
**	144	15 CRM5 M8548	CRAM PAR 1ST 04 H
**	144	21 CRM5 M8548	CRAM PAR 1ST 08 H
**	144	27 CRM5 M8548	CRAM PAR 1ST 12 H
**	144	33 CRM5 M8548	CRAM PAR 1ST 16 H
**	170	00 CRC6 M8535	CRC CH BUF ADR 0 H
**	171	00 CRC6 M8535	CRC CH BUF ADR 1 H
**	172	00 CRC6 M8535	CRC CH BUF ADR 2 H
**	173	00 CRC6 M8535	CRC CH BUF ADR 3 H
**	174	00 CRC6 M8535	CRC CH BUF ADR 4 H
**	175	00 CRC6 M8535	CRC CH BUF ADR 5 H
**	176	00 CRC6 M8535	CRC CH BUF ADR 6 H
	172	03 CRC3 M8535	CRC ERR IN H
	172	02 CRC3 M8535	CRC LAST WORD IN H
	171	04 CRC4 M8535	CRC LONG WC ERR H
	170	02 CRC4 M8535	CRC MEM STORE ENA L
	171	02 CRC4 M8535	CRC OVN ERR IN H
	172	01 CRC3 M8535	CRC READY IN H
	172	04 CRC3 M8535	CRC REVERSE IN H
	171	01 CRC4 M8535	CRC RH20 ERR IN H
	175	01 CRC6 M8535	CRC SEL 1D L
	175	02 CRC6 M8535	CRC SEL 2D L
	175	03 CRC6 M8535	CRC SEL 4D L
	171	03 CRC4 M8535	CRC SHORT WC ERR H
	174	02 CRC5 M8535	CRC WR RAM L
	174	01 CRC1 M8535	CRC1 ACT FLAG ENA H
	175	04 CRC1 M8535	CRC1 AP REQ ENA L
	176	01 CRC1 M8535	CRC1 MEM PTR0 H
	176	02 CRC1 M8535	CRC1 MEM PTR1 H
	176	03 CRC1 M8535	CRC1 MEM PTR2 H
	176	04 CRC1 M8535	CRC1 MEM PTR3 H
	177	00 CRC1 M8535	CRC1 PTR DIF=0 H
	173	01 CRC2 M8535	CRC2 ACT CTR 0R H
	173	02 CRC2 M8535	CRC2 ACT CTR 1R H

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DF	BIT	DRAWING	BOARD	NAME AND TRUTH
173	03	CRC2	M8535	CRC2 ACT CTR 2R H
173	04	CRC2	M8535	CRC2 RAM CYC H
174	03	CRC3	M8535	CRC3 OP CODE 00 H
174	04	CRC3	M8535	CRC3 OP CODE 01 H
170	03	CRC4	M8535	CRC4 DONE IN H
170	01	CRC4	M8535	CRC4 RESET IN L
170	04	CRC4	M8535	CRC4 STORE IN H
177	01	CRC6	M8535	CRC6 CH ADR 0C L
177	02	CRC6	M8535	CRC6 CH ADR 1C L
177	03	CRC6	M8535	CRC6 CH ADR 2C L
177	04	CRC6	M8535	CRC6 CH ADR 3C L
170	20	CHX2	M8515	CSH 0 ANY VAL L
177	25	CHA3	M8513YA	CSH 0 ANY WR L
171	20	CHX2	M8515	CSH 1 ANY VAL L
175	25	CHA3	M8513YA	CSH 1 ANY WR L
172	20	CHX2	M8515	CSH 2 ANY VAL L
176	25	CHA3	M8513YA	CSH 2 ANY WR L
173	20	CHX2	M8515	CSH 3 ANY VAL L
174	25	CHA3	M8513YA	CSH 3 ANY WR L
174	20	CHX4	M8515	CSH DIR 0 PAR ODD H
175	20	CHX4	M8515	CSH DIR 1 PAR ODD H
176	20	CHX4	M8515	CSH DIR 2 PAR ODD H
177	20	CHX4	M8515	CSH DIR 3 PAR ODD H
160	19	MBZ1	M8537	CSH EN CSH DATA L
173	25	CHX3	M8513YA	CSH LRU 1 H
172	25	CHX3	M8513YA	CSH LRU 2 H
161	26	MBZ6	M8537	CSH PAR BIT A H
162	26	MBZ6	M8537	CSH PAR BIT B H
162	17	MBZ5	M8537	CSH PAR BIT IN H
170	28	CSH4	M8513YA	CSH REFILL RAM WR L
161	30	MBC2	M8531YA	CSH SEL LRU H
175	21	CHX3	M8515	CSH USE ADR 2 H
176	21	CHX3	M8515	CSH USE ADR 3 H
177	21	CHX3	M8515	CSH USE ADR 4 H
172	27	CSH6	M8513YA	CSH USE HOLD H
170	21	CHX3	M8515	CSH USE IN 0 H
171	21	CHX3	M8515	CSH USE IN 1 H
172	21	CHX3	M8515	CSH USE IN 2 H
173	21	CHX3	M8515	CSH USE IN 3 H
174	21	CHX3	M8515	CSH USE IN 4 H
175	23	CSH6	M8513YA	CSH USE WR EN H
163	29	MBC3	M8531YA	CSH VAL SEL ALL H
163	30	MBC3	M8531YA	CSH VAL WR DATA H
163	31	MBC3	M8531YA	CSH WR SEL ALL H
176	31	MBX4	M8529YA	CSH WR WD 0 EN H
177	31	MBX4	M8529YA	CSH WR WD 1 EN H
170	32	MBX4	M8529YA	CSH WR WD 2 EN H
171	32	MBX4	M8529YA	CSH WR WD 3 EN H
163	32	MBC3	M8531YA	CSH WR WR DATA H
174	29	CSH1	M8513YA	CSH1 CACHE IDLE L
172	28	CSH1	M8513YA	CSH1 CCA CYC L
177	27	CSH1	M8513YA	CSH1 CYC TYPE HOLD H
174	28	CSH1	M8513YA	CSH1 EBOX CYC B L
175	28	CSH1	M8513YA	CSH1 MB CYC L
172	26	CSH1	M8513YA	CSH1 READY TO GO A H
176	27	CSH2	M8513YA	CSH2 E CACHE WR CYC H
174	22	CSH2	M8513YA	CSH2 E CORE RD RQ A L
172	29	CSH2	M8513YA	CSH2 EBOX REQ EN L
175	22	CSH2	M8513YA	CSH2 EBOX RETRY REQ L
173	23	CSH2	M8513YA	CSH2 NBOX RESP L
173	22	CSH2	M8513YA	CSH2 ONE WORD RD A L
177	28	CSH2	M8513YA	CSH2 RD PAUSE 2ND HALF L
173	24	CSH2	M8513YA	CSH2 RD PSE 2ND REQ EN L
170	25	CSH2	M8513YA	CSH2 WR TEST L
174	27	CSH3	M8513YA	CSH3 ADR PMA EN H
170	26	CSH3	M8513YA	CSH3 ANY VAL HOLD H
175	27	CSH3	M8513YA	CSH3 GATE VMA 27-33 H
171	28	CSH3	M8513YA	CSH3 MB WR RQ CLR NXT L
170	27	CSH4	M8513YA	CSH4 DATA CLR DONE L
176	24	CSH4	M8513YA	CSH4 EBOX T0 L
171	29	CSH4	M8513YA	CSH4 EBOX T1 L
173	29	CSH4	M8513YA	CSH4 EBOX T2 L
170	29	CSH4	M8513YA	CSH4 EBOX T3 L
177	29	CSH4	M8513YA	CSH4 EBOX WR T4 L
175	29	CSH4	M8513YA	CSH4 ONE WORD WR TO L
177	24	CSH4	M8513YA	CSH4 PAGE FAIL DLY H
171	24	CSH4	M8513YA	CSH4 PAGE FAIL T2 L
173	27	CSH4	M8513YA	CSH4 WRITBACK T1 A H
171	22	CSH5	M8513YA	CSH5 CHAN RD T5 L

KL10 (PV) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
172	24	CSH5	M8513YA	CSH5 CHAN T4 L
171	27	CSH5	M8513YA	CSH5 CHAN WR T5 L
174	26	CSH5	M8513YA	CSH5 CSH T0 L
170	22	CSH5	M8513YA	CSH5 PAGE REFILL COMP L
177	26	CSH5	M8513YA	CSH5 PAGE REFILL T10 L
176	29	CSH5	M8513YA	CSH5 PAGE REFILL T4 L
176	23	CSH5	M8513YA	CSH5 PAGE REFILL T8 L
174	24	CSH5	M8513YA	CSH5 PAGE REFILL T9,12 L
173	26	CSH5	M8513YA	CSH5 T1 L
176	26	CSH5	M8513YA	CSH5 T2 L
175	26	CSH5	M8513YA	CSH5 T3 L
170	23	CSH6	M8513YA	CSH6 CACHE WR IN H
172	23	CSH6	M8513YA	CSH6 CCA CYC DONE L
176	22	CSH6	M8513YA	CSH6 CCA INVAL T4 L
172	22	CSH6	M8513YA	CSH6 CHAN WR CACHE L
177	23	CSH6	M8513YA	CSH6 DATA DLY 1 L
171	25	CSH6	M8513YA	CSH6 EBOX LOAD REG H
170	24	CSH6	M8513YA	CSH6 MBOX PT DIR WR L
174	23	CSH6	M8513YA	CSH6 PAGE FAIL HOLD L
177	22	CSH6	M8513YA	CSH6 PAGE REFILL ERROR L
171	23	CSH6	M8513YA	CSH6 WR DATA RDY L
173	28	CSH7	M8513YA	CSH7 CCA WRITEBACK L
176	28	CSH7	M8513YA	CSH7 E WRITEBACK L
171	26	CSH7	M8513YA	CSH7 FILL CACHE RD L
106	24	CTL1	M8543	CTL AD LONG H
106	25	CTL1	M8543	CTL ADX CRY 36 A H
105	25	CTL1	M8543	CTL ADX CRY 36 H
100	28	CTL2	M8543	CTL AR 00-08 LOAD L
104	28	CTL2	M8543	CTL AR 00-11 CLR H
101	28	CTL2	M8543	CTL AR 09-17 LOAD L
105	28	CTL2	M8543	CTL AR 12-17 CLR H
101	26	CTL2	M8543	CTL ARL SEL 1 H
100	26	CTL2	M8543	CTL ARL SEL 2 H
103	28	CTL2	M8543	CTL ARL SEL 4 H
106	28	CTL2	M8543	CTL ARR CLR H
100	27	CTL2	M8543	CTL ARR LOAD A L
101	27	CTL2	M8543	CTL ARR LOAD B L
103	26	CTL2	M8543	CTL ARR SEL 1 H
102	26	CTL2	M8543	CTL ARR SEL 2 H
102	28	CTL2	M8543	CTL ARX LOAD H
105	26	CTL2	M8543	CTL ARXL SEL 1 L
104	26	CTL2	M8543	CTL ARXL SEL 2 H
107	26	CTL2	M8543	CTL ARXR SEL 1 H
106	26	CTL2	M8543	CTL ARXR SEL 2 H
102	25	CTL1	M8543	CTL COND/AR GETS EXP H
103	25	CTL1	M8543	CTL DISP RET L
107	24	CTL1	M8543	CTL INH CRY 18 L
136	14	CTL1	M8522	CTL INH CRY 18 L
104	25	CTL1	M8543	CTL LOAD PC L
105	27	CTL2	M8543	CTL MQ SEL 1 H
104	27	CTL2	M8543	CTL MQ SEL 2 H
106	27	CTL2	M8543	CTL MQM EN H
103	27	CTL2	M8543	CTL MQM SEL 1 H
102	27	CTL2	M8543	CTL MQM SEL 2 H
107	28	CTL2	M8543	CTL SPEC CALL L
101	25	CTL1	M8543	CTL SPEC MTR CTL L
101	24	CTL1	M8543	CTL SPEC/CLR FPD H
104	24	CTL1	M8543	CTL SPEC/FLAG CTL H
102	24	CTL1	M8543	CTL SPEC/GEN CRY 18 H
136	15	CTL1	M8522	CTL SPEC/GEN CRY 18 H
100	25	CTL1	M8543	CTL SPEC/SAVE FLAGS L
100	24	CTL1	M8543	CTL SPEC/SCM ALT H
105	24	CTL1	M8543	CTL SPEC/SP MEM CYCLE H
103	24	CTL1	M8543	CTL SPEC/STACK UPDATE H
163	33	MBC3	M8531YA	DATA VALID A OUT H
164	27	MBC3	M8531YA	DATA VALID B OUT H
107	27	CTL3	M8543	DIAG LOAD EBUS REG L
107	25	CTL3	M8543	DIAG MEM RESET H
**	130	IRD1	M8522	DR ADR 00 A H
**	130	IRD1	M8522	DR ADR 01 A H
**	130	IRD1	M8522	DR ADR 02 A H
**	131	IRD1	M8522	DR ADR 03 A H
**	131	IRD1	M8522	DR ADR 04 A H
**	131	IRD1	M8522	DR ADR 05 A H
**	131	IRD1	M8522	DR ADR 06 A H
**	131	IRD1	M8522	DR ADR 07 A H
**	131	IRD1	M8522	DR ADR 08 A H
**	133	IRD1	M8522	DRAM A 00 H
**	133	IRD1	M8522	DRAM A 01 H

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KL10(PV) DIAGNOSTIC READ FUNCTION CODES  
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DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	133	14	IRD1	M8522 DRAM A 02 H
**	133	15	IRD1	M8522 DRAM B 00 H
**	133	16	IRD1	M8522 DRAM B 01 H
**	133	17	IRD1	M8522 DRAM B 02 H
**	134	14	IRD1	M8522 DRAM J 01 H
**	134	15	IRD1	M8522 DRAM J 02 H
**	134	16	IRD1	M8522 DRAM J 03 H
**	134	17	IRD1	M8522 DRAM J 04 H
**	135	14	IRD1	M8522 DRAM J 07 H
**	135	15	IRD1	M8522 DRAM J 08 H
**	135	16	IRD1	M8522 DRAM J 09 H
**	135	17	IRD1	M8522 DRAM J 10 H
**	135	13	IRD3	M8522 DRAM ODD PARITY H
**	135	12	IRD1	M8522 DRAM PAR H
**	102	14	PIC4	M8532 EBUS CS00 E H
**	102	15	PIC4	M8532 EBUS CS01 E H
**	102	16	PIC4	M8532 EBUS CS02 E H
**	102	17	PIC4	M8532 EBUS CS03 E H
**	103	14	PIC4	M8532 EBUS CS04 E H
**	102	11	PIC4	M8532 EBUS CS05 E H
**	102	12	PIC4	M8532 EBUS CS06 E H
*	102	13	PIC2	M8532 EBUS DEMAND E H
*	167	00-08	MBZ2	M8537 EBUS REG 00-08 H
*	167	14-26	MBZ2	M8537 EBUS REG 14-26 H
*	167	27-33	MBC1	M8531YA EBUS REG 27-33 H
*	167	34,35	MBZ2	M8537 EBUS REG 34,35 H
**	120	00	EDP1	M8512 EDP AR 00 H
**	120	01	EDP1	M8512 EDP AR 01 H
**	120	02	EDP1	M8512 EDP AR 02 H
**	120	03	EDP1	M8512 EDP AR 03 H
**	120	04	EDP1	M8512 EDP AR 04 H
**	120	05	EDP1	M8512 EDP AR 05 H
**	120	06	EDP1	M8512 EDP AR 06 H
**	120	07	EDP1	M8512 EDP AR 07 H
**	120	08	EDP1	M8512 EDP AR 08 H
**	120	09	EDP1	M8512 EDP AR 09 H
**	120	10	EDP1	M8512 EDP AR 10 H
**	120	11	EDP1	M8512 EDP AR 11 H
**	133	07	SCD2	M8524 FE 00 H
**	133	08	SCD2	M8524 FE 01 H
**	133	09	SCD2	M8524 FE 02 H
**	133	10	SCD2	M8524 FE 03 H
**	133	11	SCD2	M8524 FE 04 H
**	132	07	SCD2	M8524 FE 05 H
**	132	08	SCD2	M8524 FE 06 H
**	132	09	SCD2	M8524 FE 07 H
**	132	10	SCD2	M8524 FE 08 H
**	132	11	SCD2	M8524 FE 09 H
*	135	07	SCD2	M8524 FE SIGN H
*	123	0-35	EDP4	M8512 FM 0 TO 35 H
	172	32	MBX1	M8529YA FORCE NO MATCH H
	160	27	MBC5	M8531YA FORCE VALID MATCH 0 H
	160	28	MBC5	M8531YA FORCE VALID MATCH 1 H
	160	29	MBC5	M8531YA FORCE VALID MATCH 2 H
	160	30	MBC5	M8531YA FORCE VALID MATCH 3 H
**	136	16	IRD4	M8522 GEN CRY 36 H
**	132	14	IRD1	M8522 IR AC 09 H
**	132	15	IRD1	M8522 IR AC 10 H
**	132	16	IRD1	M8522 IR AC 11 H
**	132	17	IRD1	M8522 IR AC 12 H
	132	13	IRD3	M8522 IR EN AC H
	132	12	IRD3	M8522 IR EN I/O, JRST H
	136	13	IRD1	M8522 IR I/O LEGAL H
	134	13	IRD3	M8522 IR JRST 0, L
	130	12	IRD3	M8522 IR NORM 08 H
	130	13	IRD3	M8522 IR NORM 09 H
	130	14	IRD3	M8522 IR NORM 10 H
	174	32	MBX3	M8529YA MB DATA CODE 1 H
	175	32	MBX3	M8529YA MB DATA CODE 2 H
	160	20	MBZ1	M8537 MB IN SEL 1 H
	161	20	MBZ1	M8537 MB IN SEL 2 H
	162	20	MBZ1	M8537 MB IN SEL 4 H
	160	18	MBZ5	M8537 MB PAR BIT IN H
	176	32	MBX3	M8529YA MB PAR H
	177	32	MBX2	M8529YA MB REQ HOLD H
	171	33	MBX2	M8529YA MB SEL 1 H
	172	33	MBX2	M8529YA MB SEL 2 H
	173	33	MBX2	M8529YA MB SEL HOLD H
	175	24	CSH3	M8513YA MB TEST PAR A IN L

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KL10 (PV) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
174	33	MBX6	M8529YA	MB0 HOLD IN H
175	33	MBX6	M8529YA	MB1 HOLD IN H
176	33	MBX6	M8529YA	MB2 HOLD IN H
177	33	MBX6	M8529YA	MB3 HOLD IN H
160	31	MBC1	M8531YA	MBC1 WRITE OK H
162	27	MBC2	M8531YA	MBC2 CACHE WR 00 A H
162	28	MBC2	M8531YA	MBC2 CACHE WR 09 A H
162	29	MBC2	M8531YA	MBC2 CACHE WR 18 A H
162	30	MBC2	M8531YA	MBC2 CACHE WR 27 A H
160	32	MBC2	M8531YA	MBC2 CSH ADR WR PULSE H
160	33	MBC2	M8531YA	MBC2 CSH DATA CLR DONE IN L
161	27	MBC2	M8531YA	MBC2 CSH DATA CLR T1 L
161	28	MBC2	M8531YA	MBC2 CSH DATA CLR T2 L
161	29	MBC2	M8531YA	MBC2 CSH DATA CLR T3 L
161	31	MBC2	M8531YA	MBC2 CSH VAL WR PULSE H
161	32	MBC2	M8531YA	MBC2 CSH WR WR PULSE H
162	32	MBC3	M8531YA	MBC3 A CHANGE COMING A L
162	33	MBC3	M8531YA	MBC3 ANY SBUS RQ IN L
163	27	MBC3	M8531YA	MBC3 B CHANGE COMING L
164	28	MBC3	M8531YA	MBC3 INH 1ST MB REQ H
164	32	MBC4	M8531YA	MBC4 CORE ADR 34 H
164	33	MBC4	M8531YA	MBC4 CORE ADR 35 H
165	29	MBC4	M8531YA	MBC4 CORE DATA VAL -1 L
165	30	MBC4	M8531YA	MBC4 CORE DATA VALID -2 L
165	31	MBC4	M8531YA	MBC4 CORE DATA VALID L
165	32	MBC4	M8531YA	MBC4 CORE RD IN PROG A H
166	32	MBC4	M8531YA	MBC4 MEM START L
163	28	MBC5	M8531YA	MBC5 CORE BUSY B H
161	15	MB24	M8537	MBOX ADR PAR ERR L
162	24	MB24	M8537	MBOX MB PAR ERR L
161	22	MB23	M8537	MBOX NXM ERR L
161	24	MB24	M8537	MBOX SBUS ERR L
170	30	MBX1	M8529YA	MBX1 CACHE BIT H
177	30	MBX1	M8529YA	MBX1 CCA ALL PAGES CYC H
170	31	MBX1	M8529YA	MBX1 CCA REQ L
171	31	MBX1	M8529YA	MBX1 CCA SEL 1 H
172	31	MBX1	M8529YA	MBX1 CCA SEL 2 H
174	31	MBX1	M8529YA	MBX1 CSH CCA INVAL CSH H
175	31	MBX1	M8529YA	MBX1 CSH CCA VAL CORE H
171	30	MBX2	M8529YA	MBX2 CACHE TO MB 34 H
172	30	MBX2	M8529YA	MBX2 CACHE TO MB 35 H
173	31	MBX2	M8529YA	MBX2 CHAN WR CYC L
176	34	MBX3	M8529YA	MBX3 REFILL HOLD H
175	35	MBX3	M8529YA	MBX3 SBUS DIAG 3 L
176	35	MBX3	M8529YA	MBX3 SBUS DIAG CYC L
173	30	MBX4	M8529YA	MBX4 CACHE TO MB DONE H
174	30	MBX4	M8529YA	MBX4 CACHE TO MB T2 L
175	30	MBX4	M8529YA	MBX4 CACHE TO MB T3 L
176	30	MBX4	M8529YA	MBX4 CACHE TO MB T4 A L
177	35	MBX4	M8529YA	MBX4 WRITEBACK T2 L
170	33	MBX5	M8529YA	MBX5 MB REQ IN H
172	34	MBX5	M8529YA	MBX5 MEM RD RQ IN H
170	34	MBX5	M8529YA	MBX5 MEM TO C EN L
175	34	MBX5	M8529YA	MBX5 MEM WR RQ IN H
177	34	MBX5	M8529YA	MBX5 RQ 0 IN H
170	35	MBX5	M8529YA	MBX5 RQ 1 IN H
171	35	MBX5	M8529YA	MBX5 RQ 2 IN H
172	35	MBX5	M8529YA	MBX5 RQ 3 IN H
160	22	MBZ1	M8537	MBZ1 CHAN CORE BUSY H
161	21	MBZ1	M8537	MBZ1 RD-PSE-WR REF L
161	23	MBZ3	M8537	MBZ3 CHAN MEM REF L
162	22	MBZ3	M8537	MBZ3 HOLD ERA L
162	18	MBZ3	M8537	MBZ3 SEQUENTIAL RQ H
162	23	MBZ4	M8537	MBZ4 NXM T2 H
160	24	MBZ4	M8537	MBZ4 NXM T6,7 L
161	18	MBZ6	M8537	MBZ6 CSH PAR BIT H
105	18	MCL2	M8544	MCL LOAD AR H
106	18	MCL2	M8544	MCL LOAD ARX H
107	22	MCL5	M8544	MCL MBOX CYC REQ H
107	18	MCL2	M8544	MCL STORE AR L
104	19	MCL2	M8544	MCL VMA USER H
102	19	MCL1	M8544	MCL1 MEM/ARL IND H
115	15	MCL1	M8545	MCL1 MEM/REG FUNC L
103	19	MCL1	M8544	MCL1 REQ EN L
107	19	MCL2	M8544	MCL2 VMA EXTENDED L
103	18	MCL2	M8544	MCL2 VMA PAUSE H
106	19	MCL2	M8544	MCL2 VMA PREVIOUS L
105	19	MCL2	M8544	MCL2 VMA PUBLIC H

KL10(PV) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
102	18	MCL2	M8544	MCL2 VMA READ H
104	18	MCL2	M8544	MCL2 VMA WRITE H
105	20	MCL3	M8544	MCL3 PAGE ADDRESS COND H
106	20	MCL3	M8544	MCL3 PAGE ILL ENTRY H
102	20	MCL3	M8544	MCL3 PAGE TEST PRIVATE H
104	22	MCL4	M8544	MCL4 LOAD VMA CONTEXT L
103	23	MCL4	M8544	MCL4 SHORT STACK H
102	22	MCL4	M8544	MCL4 VMA GETS AD H
103	22	MCL4	M8544	MCL4 VMA INC H
106	21	MCL4	M8544	MCL4 VMAX SEL 1 H
105	21	MCL4	M8544	MCL4 VMAX SEL 2 H
102	21	MCL4	M8544	MCL4 XR PREVIOUS H
102	23	MCL4	M8544	MCL4 XR SHORT H
106	22	MCL5	M8544	MCL5 18 BIT EA H
105	22	MCL5	M8544	MCL5 23 BIT EA H
103	21	MCL5	M8544	MCL5 VMA ADR ERR H
104	21	MCL5	M8544	MCL5 VMAX EN L
104	23	MCL6	M8544	MCL6 EBOX CACHE L
107	23	MCL6	M8544	MCL6 EBOX MAP L
105	23	MCL6	M8544	MCL6 EBOX MAY BE PAGED L
104	20	MCL6	M8544	MCL6 PAGE UEER REF H
107	21	MCL6	M8544	MCL6 PAGED FETCH L
106	23	MCL6	M8544	MCL6 REG FUNC H
107	20	MCL6	M8544	MCL6 VMA FETCH H
103	20	MCL6	M8544	MCL6 VMA UPT H
165	33	MBC4	M8531YA	MEM ADR PAR H
162	21	MBZ1	M8537	MEM BUSY H
173	32	MBX3	M8529YA	MEM DATA TO MEM H
171	34	MBX3	M8529YA	MEM DIAG L
161	17	MEM5	M8537	MEM PAR IN H
166	27	MBC4	M8531YA	MEM RD RQ B H
166	28	MBC4	M8531YA	MEM RQ 0 H
166	29	MBC4	M8531YA	MEM RQ 1 H
166	30	MBC4	M8531YA	MEM RQ 2 H
166	31	MBC4	M8531YA	MEM RQ 3 H
161	19	MBZ1	M8537	MEM TO C DIAG EN L
164	29	MBC3	M8531YA	MEM TO C EN L
173	34	MBX3	M8529YA	MEM TO C SEL 1 H
174	34	MBX3	M8529YA	MEM TO C SEL 2 H
166	33	MBC4	M8531YA	MEM WR RQ L
*	122	0-35	EDP2	M8512 MQ 0 TO 35 H
*	113	20-35	MTR1	M8538 MTR CACHE COUNT 02-17 H
	117	25	MTR3	M8538 MTR CONO MTR, L
*	112	20-35	MTR1	M8538 MTR EBOX COUNT 02-17 H
*	114	24-35	MTR1	M8538 MTR INTERVAL 06-17 H
*	111	20-35	MTR1	M8538 MTR PERF COUNT 02-17 H
*	115	24-35	MTR3	M8538 MTR PERIOD 06-17 H
*	110	20-35	MTR1	M8538 MTR TIME 02-17 H
	116	23	MTR2	M8538 MTR2 ACCT ON H
	116	22	MTR2	M8538 MTR2 EXEC ACCT EN H
	116	21	MTR2	M8538 MTR2 PI ACCT EN H
	116	25	MTR2	M8538 MTR2 TIME ON H
	115	22	MTR3	M8538 MTR3 INTERVAL DONE H
	115	21	MTR3	M8538 MTR3 INTERVAL ON H
	115	23	MTR3	M8538 MTR3 INTERVAL OVRFLO H
	117	22	MTR5	M8538 MTR5 INCR SEL 1 H
	117	21	MTR5	M8538 MTR5 INCR SEL 2 H
	117	20	MTR5	M8538 MTR5 VECTOR REQ H
	160	21	MBZ3	M8537 NXM ACKN H
	160	23	MBZ3	M8537 NXM ANY L
	161	25	MBZ3	M8537 NXM DATA VAL L
	162	25	PAG5	M8537 PAG MB 00-17 PAR H
	160	26	PAG5	M8537 PAG MB 18-35 PAR H
*	15X	13-35	VMA3	M8542 PC 13-35 H **NOTE
	164	30	MBC3	M8531YA PHASE CHANGE COMING L
	110	17	PIC3	M8545 PI3 APR PIA 01 H
	110	16	PIC3	M8545 PI3 APR PIA 02 H
	110	15	PIC3	M8545 PI3 APR PIA 04 H
**	116	35	PIC3	M8538 PI3 MTR PIA 01 H
**	116	34	PIC3	M8538 PI3 MTR PIA 02 H
**	116	33	PIC3	M8538 PI3 MTR PIA 04 H
	100	10	PIC1	M8532 PIC1 ACTIVE H
**	101	11	PIC1	M8532 PIC1 GEN 1 H
**	101	12	PIC1	M8532 PIC1 GEN 2 H
**	101	13	PIC1	M8532 PIC1 GEN 3 H
**	101	14	PIC1	M8532 PIC1 GEN 4 H
**	101	15	PIC1	M8532 PIC1 GEN 5 H
**	101	16	PIC1	M8532 PIC1 GEN 6 H
**	101	17	PIC1	M8532 PIC1 GEN 7 H

KL10(PV) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
**	100	11 PIC1 M8532	PIC1 ON 1 H
**	100	12 PIC1 M8532	PIC1 ON 2 H
**	100	13 PIC1 M8532	PIC1 ON 3 H
**	100	14 PIC1 M8532	PIC1 ON 4 H
**	100	15 PIC1 M8532	PIC1 ON 5 H
**	100	16 PIC1 M8532	PIC1 ON 6 H
**	100	17 PIC1 M8532	PIC1 ON 7 H
**	100	03 PIC1 M8532	PIC1 PIH1 H
**	100	04 PIC1 M8532	PIC1 PIH2 H
**	100	05 PIC1 M8532	PIC1 PIH3 H
**	100	06 PIC1 M8532	PIC1 PIH4 H
**	100	07 PIC1 M8532	PIC1 PIH5 H
**	100	08 PIC1 M8532	PIC1 PIH6 H
**	100	09 PIC1 M8532	PIC1 PIH7 H
	103	15 PIC2 M8532	PIC2 HONOR INTERNAL H
	103	16 PIC2 M8532	PIC2 READY H
	103	13 PIC2 M8532	PIC2 STATE HOLD H
	103	11 PIC2 M8532	PIC2 TIMER DONE H
	103	12 PIC5 M8532	PIC5 EBUS PI GRANT H
	103	17 PIC5 M8532	PIC5 EBUS REQ H
	161	33 MBC2 M8531YA	RQ HOLD FF H
	173	35 MBX2 M8529YA	SBUS ADR 34 H
	174	35 MBX2 M8529YA	SBUS ADR 35 H
	162	31 MBC2 M8531YA	SBUS ADR HOLD H
	136	07 SCD2 M8524	SC .GE. 36 H
**	131	07 SCD2 M8524	SC 00 H
**	131	08 SCD2 M8524	SC 01 H
**	131	09 SCD2 M8524	SC 02 H
**	131	10 SCD2 M8524	SC 03 H
**	131	11 SCD2 M8524	SC 04 H
**	130	07 SCD2 M8524	SC 05 H
**	130	08 SCD2 M8524	SC 06 H
**	130	09 SCD2 M8524	SC 07 H
**	130	10 SCD2 M8524	SC 08 H
**	130	11 SCD2 M8524	SC 09 H
	134	07 SCD2 M8524	SC SIGN H
	133	04 SCD1 M8524	SCAD=0 L
	137	06 SCD5 M8524	SCD ADR BREAK PREVENT H
	137	05 SCD5 M8524	SCD ADR BRK CYC H
	137	02 SCD5 M8524	SCD ADR BRK INH H
	131	03 SCD4 M8524	SCD CRY0 H
	131	04 SCD4 M8524	SCD CRY1 H
	131	06 SCD4 M8524	SCD DIV CHK H
	132	03 SCD4 M8524	SCD FOV H
	130	06 SCD4 M8524	SCD FPD H
	132	04 SCD4 M8524	SCD FXU H
	135	04 SCD5 M8524	SCD KERNEL MODE H
	136	02 SCD5 M8524	SCD KERNEL OR USER IOT H
	134	03 SCD5 M8524	SCD LEAVE USER H
	133	03 SCD5 M8524	SCD LOAD FLAGS A H
	133	06 SCD4 M8524	SCD NICOND 10 H
	131	02 SCD4 M8524	SCD OV H
	133	02 SCD4 M8524	SCD PCP H
	135	06 SCD5 M8524	SCD PRIVATE INSTR EN L
	135	05 SCD5 M8524	SCD PRIVATE INSTR L
	135	03 SCD5 M8524	SCD PUBLIC A H
	134	02 SCD5 M8524	SCD PUBLIC EN L
	134	06 SCD5 M8524	SCD PUBLIC PAGE H
	137	07 SCD4 M8524	SCD TRAP CLEAR L
	130	04 SCD4 M8524	SCD TRAP CYC 1 H
**	130	03 SCD4 M8524	SCD TRAP CYC 2 H
**	136	03 SCD3 M8524	SCD TRAP MIX 32 H
**	136	04 SCD3 M8524	SCD TRAP MIX 33 H
**	137	03 SCD3 M8524	SCD TRAP MIX 34 H
**	137	04 SCD3 M8524	SCD TRAP MIX 35 H
	130	05 SCD4 M8524	SCD TRAP REQ 1 H
	130	02 SCD4 M8524	SCD TRAP REQ 2 H
	134	02 SCD5 M8524	SCD USER A L
	134	05 SCD5 M8524	SCD USER EN L
	136	05 SCD5 M8524	SCD USER IOT A H
	136	06 SCD5 M8524	SCD USER IOT EN L
	160	17 SHD1 M8537	SH AR PAR ODD A H
	105	31 SHD1 M8526YA	SH AR PAR ODD H
	106	31 SHD1 M8526YA	SH ARX PAR ODD H
	111	12 SHM1 M8540	SHM1 AR EXTENDED H
	134	12 IRD3 M8522	TEST SATISFIED H
*	15X	13-35 VMA2 M8542	VMA 13-35 H **NOTE
*	15X	13-35 VMA4 M8542	VMA HELD 13-35 H **NOTE
	132	02 SCD4 M8524	VMA HELD OR PC 00 H
**	100	18 MCL3 M8544	VMA HELD OR PC 01 H

GEN. INFO.

-102-

KL10 (PV) DIAGNOSTIC READ FUNCTION CODES  
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING BOARD	NAME AND TRUTH
**	100	19	MCL3 M8544 VMA HELD OR PC 02 H
**	100	20	MCL3 M8544 VMA HELD OR PC 03 H
**	100	21	MCL3 M8544 VMA HELD OR PC 04 H
**	100	22	MCL3 M8544 VMA HELD OR PC 05 H
**	100	23	MCL3 M8544 VMA HELD OR PC 06 H
**	101	18	MCL3 M8544 VMA HELD OR PC 07 H
**	101	19	MCL3 M8544 VMA HELD OR PC 08 H
**	101	20	MCL3 M8544 VMA HELD OR PC 09 H
**	101	21	MCL3 M8544 VMA HELD OR PC 10 H
**	101	22	MCL3 M8544 VMA HELD OR PC 11 H
**	101	23	MCL3 M8544 VMA HELD OR PC 12 H
**	157	11	VMA4 M8542 VMA PREV SEC 13 H
**	156	11	VMA4 M8542 VMA PREV SEC 14 H
**	155	11	VMA4 M8542 VMA PREV SEC 15 H
**	154	11	VMA4 M8542 VMA PREV SEC 16 H
**	153	11	VMA4 M8542 VMA PREV SEC 17 H
	157	13	VMA1 M8542 VMA1 AC REF A L
	153	15	VMA1 M8542 VMA1 LOCAL AC ADDRESS L
	153	13	VMA1 M8542 VMA1 MISC=0 L
	150	11	VMA1 M8542 VMA1 VMA SECTION 0 L
	157	15	VMA3 M8542 VMA3 MATCH 13-35 H
	151	11	VMA3 M8542 VMA3 PC SECTION 0 L
	152	11	VMA4 M8542 VMA4 PCS SECTION 0 L

NOTE

TRACON and the 11-based 10 diagnostic programs interpret all diagnostic read functions which are not preceded with either a single or double asterisk [(\*) or (\*\*)] as single bits; as such, they are printed out by bit position and/or name. Diagnostic read functions preceded by a single asterisk (\*) are interpreted as registers and are printed out as such. Diagnostic read functions which are preceded by a double asterisk (\*\*) may be interpreted and printed as either single bits or as a register depending on the program doing the interpretation.

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# SW./JMPS.

-2-

## LP20 SWITCHES AND JUMPERS

### Switches

M8586 (Rev. E) uses a switch pack in place of jumpers.

775400 (address unit 0) set switches 5, 6, 8, 9, and 10 OFF.

754 (vector unit 0) set switch 3 OFF

775420 (address unit 1) set switches 1, 5, 6, 8, 9, and 10 OFF.

750 (vector, unit 1) set switches 1 and 3 OFF.

### Jumpers

I indicates that the jumper should be installed.

R indicates that the jumper should be removed.

M8586 Control Loc: ABCDEF02

W1-W9 corresponds to base address 775400 (for unit 0) or 775420 (for unit 1).

Jumper	Adr	List	775400	775420
--------	-----	------	--------	--------

W1	4	I	R
W2	5	I	I
W3	6	I	I
W4	7	I	I
W5	8	R	R
W6	9	R	R
W7	10	I	I
W8	11	R	R
W9	12	R	R

W10-W16 correspond to vector 754 (for unit 0) or 750 (for unit 1)

Jumper	Vec	bit	754	750
--------	-----	-----	-----	-----

W10	2	I	R
W11	3	I	I
W12	4	R	R
W13	5	I	I
W14	6	I	I
W15	7	I	I
W16	8	I	I

### M8587 Data Paths

Jumper	Function
--------	----------

W1	Install to enable parity
W2	Install for DAVFU

## KL10 MODEL (PA and PV) OPTION JUMPERS

OPTION BITS--SOURCE-----4D44E1=CRM 08 H

CACHE AVAILABLE-----4E43A1  
 CHANNELS AVAILABLE-----4E43E1  
 50 HRZ-----4E43M2

KL10-PV-CPU 4D43D2

SERIAL NUMBER BITS--SOURCE--4D42E1

2048--4E41M2  
 1024--4E41A1  
 512---4E41E1  
 256---4D41D2  
 128---4E41E1  
 64----4E41F2

SERIAL NUMBER BITS--SOURCE--4D40E1

32----4E39M2  
 16----4E39A1  
 08----4E39E1  
 04----4D39D2  
 02----4D39E1  
 01----4E39F2

## MA20 JUMPERS

CONT # JUMPER PINS(S) TO GROUND

0 EE1 AND EF2  
 1 EE1 (ONLY)  
 2 EF2  
 3 NONE

NOTE: Jumpers are external on the backplane.

## MG10/MH10 JUMPERS

DEV	REQCYC (M ROW)		ADRACK (N ROW)	
	From	To	From	To
DAS33	T7	A5*	T7	C7
DF10	T7	A4	T7	A1
DF10C	T7	A5*	T7	C7
DL10	T7	A5*	T7	C7
DT05	T7	A4	T7	A1
DX10	T7	A5**	T7	C7
KA10	T7	A4	T7	A1
KI10	T7	A5*	T7	C7
KL10	T7	A5*	T7	A1
MX10	T7	A4	T7	A1
MX10C	T7	A5*	T7	C7

## NOTES:

\* Use pin A5 if MG10 is the fastest memory on that bus, otherwise,  
 use pin B5.  
 \*\*Never use pin B5 (RQ Cyc Slow).

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**NOTES**



LPBCTR — DMA Byte Count Register

(775406)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
					11	10	09	08	07	06	05	04	03	02	01	00
					(BYTE COUNT — TWO'S COMPLEMENT OF NUMBER OF BYTE TO XFER)											

NOTE: ALL BITS READ/WRITE.

MR-2015

LPBSAD — DMA Bus Address Register

(775404)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
					11	10	09	08	07	06	05	04	03	02	01	00
					(ADDRESS OF NEXT BYTE IN BUFFER)											

NOTE: ALL BITS READ/WRITE

MR-2014

LPCCTR — Column Count Register (High Byte)  
LPCBUF — Character Buffer Register (Low Byte)

(775414)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
					07	06	05	04	03	02	01	00				
					(CHARACTER COLUMN)				(CHARACTER BUFFER)							

NOTE: BITS <15:08> READ/WRITE

MR-2018

LPCSKM — Checksum Register  
LPTDAT — Printer Data Register

(775416)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
				CHECKSUM									DATA				
													04	02	01	00	

NOTE: ALL BITS READ ONLY

MR-2013

LPCSRA — Control and Status Register "A"

(775400)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	R	R	R	R	R	R/W	W	W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	ERROR	PAGE = 0	ILL CHAR	VFU RDY	ON LINE	DEL CHAR	INIT	RESET ERROR	DONE	INIT ENAB	(EXT ADR) 17	(EXT ADR) 16	(MODE) 00	PAR ENAB	GO	

- 15 LOGICAL "OR" OF ALL ERRORS
  - 14 PAGE COUNTER INCREMENTED TO ZERO
  - 13 ILLEGAL CHARACTER
  - 12 DAVFU READY (SET IF OPTICAL VFU)
  - 11 PRINTER READY AND ON LINE
  - 10 DELIMITER CHAR HELD
  - 09 INITIALIZE - RESET FLAGS SET DONE
  - 08 RESET ERROR, SET DONE, RESET GO
- 06 INTERRUPT ENABLE
  - <06:04> EXTENDED UNIBUS ADDRESS BITS 17 AND 16
  - <03:02> MODE BITS
  - 00 = NORMAL
  - 01 = TEST MODE (INHIBIT PRINTING)
  - 10 = VFU LOAD (DMA TO VFU)
  - 11 = RAM LOAD (DMA MODE ONLY)
  - 01 PARITY ENABLE (RAM AND MEMORY)

MR-2012

LPCSRB - Control and Status Register "B"

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALID DATA	LA180	NOT RDY	PAR BIT	OP VFU	02	(TEST) 01	00	OFF LINE	VFU ERROR	PAR ERROR	MEM ERROR	RAM ERROR	SYNC TO	DEM TO	GO ERROR
R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

14	SET IF LA180 TYPE PRINTER	FORCE ERROR CONDITIONS
13	NOT READY (OTHER THAN TAPE FAULT)	02 01 00
12	DATA PARITY BIT (AS SENT TO PRINTER)	0 0 0
11	OPTICAL VFU (ZERO IF DAVFU)	0 0 1
06	PARITY ERROR AT PRINTER	0 0 1
04	MEMORY PARITY ERROR	0 1 1
03	RAM PARITY ERROR DURING DMA XFER	1 0 0
02	MASTER SYNC TIME OUT (NO SYNC)	1 0 1
01	DEMAND TIME OUT	1 1 0
00	GO SET AND "ERROR" OR "DEMAND	1 1 1

MR-2016

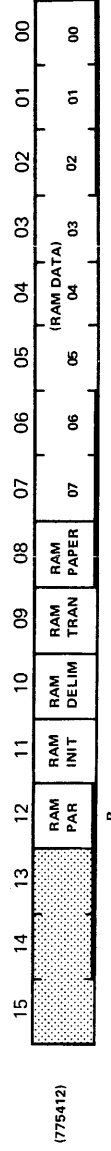
LPPCTR - Page Count Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(PAGE COUNT)															
(775410)															

NOTE: ALL USED BITS READ/WRITE

MR-2017

LPRAMD - RAM Data Register



NOTE: ALL USED BITS EXCEPT 12 READ/WRITE

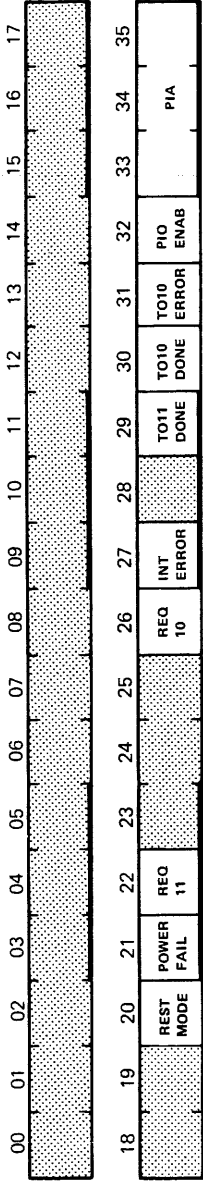
- 12 RAM PARITY BIT
- 11 INTERRUPT BIT - GEN A BR
- 10 DELIMITER - TAKE DATA FROM RAM
- 09 TRANSLATION BIT - RDAT TO PRINTER
- 08 PAPER INSTRUCTION RDAT TO DAVFU
- <07:00> RAM DATA - ADDRESS IS IN LPCBUF

MR-2019

174434

CONI DTE

(7x240)



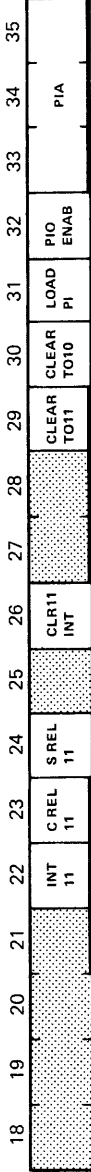
20 RESTRICTED MODE  
 22 10 REQUESTING 11  
 26 11 REQUESTING 10

27 INTERRUPT TO11 ERROR  
 32 PIO ENABLE

MR-2100

CONO DTE

(7x200)



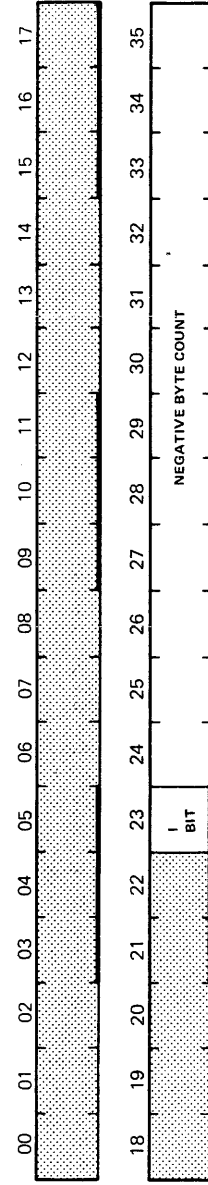
22 10 REQUESTING 11 INTERRUPT  
 23 CLEAR RELOAD 11  
 24 SET RELOAD 11  
 26 CLEAR 11 REQUESTING 10 INTERRUPT

29 CLEAR TO 11 DONE AND TO 11 ERROR  
 30 CLEAR TO 10 DONE AND TO 11 ERROR  
 31 LOAD PI CHAN NUMBER INTO BITS <33:35>  
 32 PIO ENABLE

MR-2099

DATAO DTE

(7xx140)

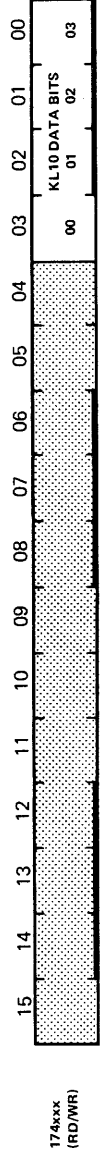


23  
0 - INTERRUPT KL10 (ONLY) AT END OF TRANSFER  
1 - INTERRUPT BOTH 10 AND 11 AT END OF TRANSFER

MR-2106



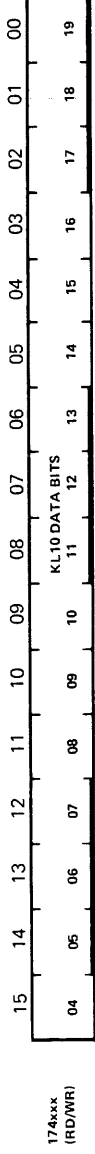
DEXWD1 - Deposit or Examine Word 1



MR-2107

NOTE: xxx = (406 - DTE NO. 0) (446 - DTE NO. 1) (506 - DTE NO. 2) (546 - DTE NO. 3)

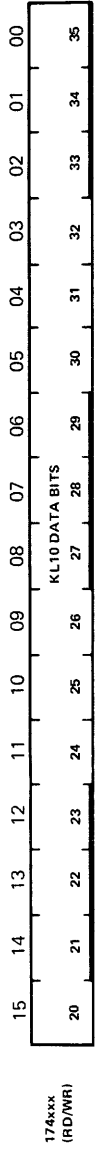
DEXWD2 - Deposit or Examine Word 2



MR-2108

NOTE: xxx = (404 - DTE NO. 0) (444 - DTE NO. 1) (504 - DTE NO. 2) (544 - DTE NO. 3)

DEXWD3 - Deposit or Examine Word 3



MR-2109

NOTE: xxx = (402 - DTE NO. 0) (442 - DTE NO. 1) (502 - DTE NO. 2) (542 - DTE NO. 3)

DIAG1 - Diagnostic Word 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
174xxx (READ)				ERROR STOP	KL10 RUN	HALT LOOP	DEP EX	TO10 XFER	TO11 XFER	DIAG 10/11	VEC INT ADR 04 03 02				DIAG CMDST

NOTE: xxx = (430 - DTE NO. 0) (470 - DTE NO. 1) (530 - DTE NO. 2) (570 - DTE NO. 3)

- 11 CRAM, DRAM, FM PARERR OR FS PROBE COND
- 10 RUN FLOP SET, CONTROLLED BY 11
- 09 MICROCODE IN HALT LOOP
- 08 DEPOSIT OR EXAMINE
- 07 TO10 TRANSFER
- 06 TO11 TRANSFER
- 05 DIAGNOSE 10/11 INTERFACE
- 04 VECTOR INTERRUPT ADDRESS
- 03 DIAGNOSTIC COMMAND START

MR-2118

DIAG1 - Diagnostic Word 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
174xxx (WRITE)	00	01	02	03	04	05	06	DIAG FUNC	DIAG 10/11	SING PULSE	KL10 DIAG	DSEND DREC			DIAG CMDST

NOTE: xxx = (430 - DTE NO. 0) (470 - DTE NO. 1) (530 - DTE NO. 2) (570 - DTE NO. 3)

- 07 REMOVE STATUS FROM DS LINES
- 06 DIAGNOSE 10/11 INTERFACE
- 05 SINGLE CLOCK CYCLE
- 04 KL10 DIAGNOSTIC TRANSFER MODE
- 03 SEND/RECEIVE DURING DIAGNOSTIC BUS TRANSFER
- 02 DIAG COMMAND START (DCOMST)
- 01
- 00

MR-2102

DIAG2 - Diagnostic Word 2

174xxx  
(READ)

15	00
14	RAM FILE MIXER
13	01 02 03
12	
11	
10	
09	
08	
07	
06	
05	
04	
03	
02	
01	
00	

NOTE: xxx = (432 - DTE NO. 0) (472 - DTE NO. 1) (532 - DTE NO. 2) (572 DTE NO. 3)

<15:12> RAM FILE MIXER ADDRESS

MR-2119

DIAG2 - Diagnostic Word 2

174xxx  
(WRITE)

15	
14	EBUS DONE
13	
12	
11	
10	
09	
08	
07	
06	DTE RESET
05	
04	
03	
02	
01	
00	

NOTE: xxx = (432 - DTE NO. 0) (472 - DTE NO. 1) (532 - DTE NO. 2) (572 - DTE NO. 3)

MR-2103

DIAG3 - Diagnostic Word 3 % Y

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SWSEL LEFT	PAR FLOP	UNIBUS PARITY INFO								UBUS DPE	WRITE EP	UBUS ERROR	NPR ERROR		

NOTE: xxx = (436 - DTE NO. 0) (476 - DTE NO. 1) (536 - DTE NO. 2) (576 - DTE NO. 3)

- 15 SWAP SELECT LEFT 03 EVEN PARITY WRITE SET
- 14 DPS4 (N) PARITY FLOP 02 UNIBUS RECEIVER ERROR
- <13.09> UNIBUS PARITY ERROR CAPTURED DATA 01 UNIBUS (NPR - BYTE) PARITY ERROR
- 04 DATO UNIBUS PARITY ERROR

MR-2120

DIAG3 - Diagnostic Word 3

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
					SHIFT C DATA	CLEAR PE RE	WRITE EP	CLEAR NPR E	TO10 BYTE						

NOTE: xxx = (436 - DTE NO. 0) (476 - DTE NO. 1) (536 - DTE NO. 2) (576 - DTE NO. 3)

- 05 SHIFT CAPTURED DATA 01 CLEAR NPR PARITY ERROR
- 04 CLEAR UNIBUS PARITY AND RECEIVE ERROR 00 TO10 BYTE MODE
- 03 WRITE EVEN PARITY

MR-2104

DLYCNT DELAY COUNT

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
17Axxx (RD/WR)	UA	17	MSD	DELAY COUNT											LSD
16															

MR-2101

NOTE: xxx = (400 - DTE NO. 0) (440 - DTE NO. 1) (500 - DTE NO. 2) (540 - DTE NO. 3)  
DELAY COUNT 37777 = NO DELAY

<15:14> UNIBUS ADDRESS BITS 16 AND 17

STATUS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
174xxx (READ)	TO10 DONE	TO10 ERROR	RAM = 0	TO11 BELL	DEX WD1	11MEM PE	TO10 BELL	TO11 DONE	EBUF SEL	NULL STOP	EBUS PE	REST MODE	DEPEX COMP	TO11 ERROR	INT ON

NOTE: xxx = (434 - DTE NO. 0) (474 - DTE NO. 1) (534 - DTE NO. 2) (574 - DTE NO. 3)

- 15 TO10 BYTE COUNT = 0 OR PDP-11 SET TO10 DONE
- 13 NPR UNIBUS OR - 11 MEM PE OR UNIBUS TIMEOUT
- 12 DURING TO10 BYTE XFER
- 11 RAM DATA = 0
- 10 11 DOORBELL INT REQ BY 10
- 09 DIAGNOSTIC USE ONLY
- 08 PDP-11 MEMPARITY ERROR
- 07 TO11 BYTE COUNT = 0, XFER STOP ON MU11 CHAR OR PDP-11 SET TO11 DONE
- 06 E BUFFER SELECT
- 04 EBUSPARITY ERROR DURING TO11 BYTE OR EXAM XFER
- 03 1 = RESTRICTED MODE, 0 = PRIVILEGED MODE
- 02 LAST DEPEXAM COMPLETED
- 01 TO11 BYTE XFER ERROR
- 30 INTERRUPT ON

MR-2105

STATUS

174xxx (WRITE)	15	CLEAR TERM	TO10 ERROR	14	CLEAR TO10 ERROR	TO10 ERROR	13	CLEAR TO10 ERROR	TO10 ERROR	12	CLEAR TO10 ERROR	TO10 ERROR	11	SETT1 BELL	CLRT1 BELL	10	CLRT1 BELL	CLRT1 PE	09	CLRT1 PE	SETT10 BELL	08	SETT10 BELL	SETT1 DONE	07	CLR11 DONE	11INT REQ	06	CEBUS PE	INT OFF	05	SET EBPE	04	SET EBPE	03	SET TO11E	02	01	00	CLEAR TO11E
-------------------	----	---------------	---------------	----	------------------------	---------------	----	------------------------	---------------	----	------------------------	---------------	----	---------------	---------------	----	---------------	-------------	----	-------------	----------------	----	----------------	---------------	----	---------------	--------------	----	-------------	------------	----	-------------	----	-------------	----	--------------	----	----	----	----------------

NOTE: xxx = (434 - DTE NO. 0) (474 - DTE NO. 1) (534 - DTE NO. 2) (574 - DTE NO. 3)

- 15 TO10 NORMAL TERMINATION
- 14 CLEAR TO10 NORMAL TERMINATION
- 13 SET TO10 ERROR
- 12 CLEAR TO10 ERROR
- 11 SET TO11 DOORBELL
- 10 CLEAR TO11 DOOR BELL
- 09 CLEAR PDP-11 MEMORY PARITY ERROR
- 08 SET T10DB
- 07 SET TO11 DONE
- 06 CLEAR TO11 DONE
- 05 GEN PDP-11 BR REQ
- 04 CLEAR ERBUS PARITY ERROR
- 03 DISABLE DTE FROM GENERATING BR REQ
- 02 SET ERBUS PARITY ERROR
- 01 SET TO11 ERROR
- 00 CLEAR TO11 ERROR

MR-2121

TENAD1 - Ten Address 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
174xxx (RD/WR)	ADDRESS SPACE	EX DER	PROT	KL10 ADDRESS			13	14	15	16	17	18	19		

NOTE: xxx = (410 - DTE NO. 0) (450 - DTE NO. 1) (510 - DTE NO. 2) (550 - DTE NO. 3)

<16:13> 0 = EPT, 1 = EXEC VIRTUAL,  
2-3 = RES, 4 = PHYS, 5-7 = RES

0 = EXAMINE 1 = DEPOSIT  
0 = PROTECT OFF, 1 = PROTECT ON

MR-2110

TENAD2 - Ten Address 2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
174xxx (RD/WR)	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
	KL10 ADDRESS															

NOTE: xxx = (412 - DTE NO. 0) (452 - DTE NO. 1) (512 - DTE NO. 2) (552 - DTE NO. 3)

MR-2111

TO10AD - TO10 Address

174xxx	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	BYTE ADDRESS OF SOURCE STRING (PDP-11)															

NOTE: xxx = (420 - DTE NO. 0) (460 - DTE NO. 1) (520 - DTE NO. 2) (560 - DTE NO. 3)

MR-2115

TO10BC - TO10 Byte Count

174xxx	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	NEGATIVE BYTE COUNT															

NOTE: xxx = (414 - DTE NO. 0) (454 - DTE NO. 1) (514 - DTE NO. 2) (554 - DTE NO. 3)

MR-2117

TO10DT - TO10 Data

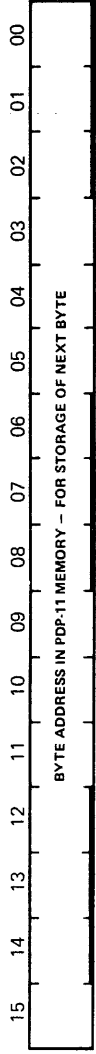
174xxx	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	BYTE MODE: <16:08> = 0 WORD MODE: KL10 BITS <20:27> BYTE MODE: KL10 BITS <28:35> WORD MODE: KL10 BITS <28:35>															

NOTE: xxx = (424 - DTE NO. 0) (464 - DTE NO. 1) (524 - DTE NO. 2) (564 - DTE NO. 3)

MR-2113



TO11AD - TO11 Address

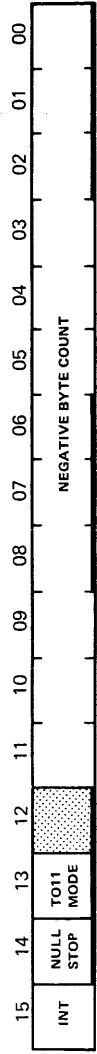


174xxx

NOTE: xxx = (422 - DTE NO. 0) (462 - DTE NO. 1) (522 - DTE NO. 2) (562 - DTE NO. 3)

MR-2114

TO11BC - TO11 Byte Count



174xxx

NOTE: xxx = (416 - DTE NO. 0) (456 - DTE NO. 2) (516 - DTE NO. 2) (556 - DTE NO. 3)

15 INT BIT: 0 = INT 11 NORM TERM,  
: 1 = INT 10 AND 11

14 STOP ON NULL CHAR FROM EBOX  
13 0 = WORD MODE IN DTE  
1 1 = BYTE MODE IN DTE

MR-2116

TO11DT - TO11 Data

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BYTE MODE: KL10 BITS <20:27> OR <28:35> WORD MODE: KL10 BITS <20:27>															
BYTE MODE: KL10 BITS <20:27> OR <28:35> WORD MODE: KL10 BITS <28:35>															

174xxx

NOTE: xxx = (426 - DTE NO. 0) (466 - DTE NO. 1) (526 - DTE NO. 2) (666 - DTE NO. 3)

MR-2112

EXECUTIVE PROCESS TABLE

(ADDRESSED FROM EBR)

0	EIGHT CHANNEL LOGOUT AREAS	
	EACH: 0 INITIAL CHANNEL COMMAND	
	1 GETS CHANNEL STATUS WORD	
	2 GETS LAST UPDATED COMMAND	
	3 RESERVED	
37	RESERVED	
40	RESERVED	
41	RESERVED	
42	STANDARD PRIORITY INTERRUPT INSTRUCTIONS	
57	RESERVED	
60	FOUR CHANNEL BLOCK FILL WORDS	
63	RESERVED	
64	RESERVED	
137	RESERVED	
140	FOUR DTE20 CONTROL BLOCKS	
	EACH: 0 TO11 BYTE POINTER	
	1 TO10 BYTE POINTER	
	2 DTE INTERRUPT INSTRUCTION	
	3 RESERVED	
	4 EXAMINE PROTECT	
	5 EXAMINE RELOCATION	
	6 DEPOSIT PROTECT	
	7 DEPOSIT RELOCATION	
177	EXECUTIVE PAGE 400	
200	EXECUTIVE PAGE 401	EXECUTIVE PAGE 401
377	EXECUTIVE PAGE 776	EXECUTIVE PAGE 777
400	RESERVED	
420	RESERVED	
421	EXECUTIVE ARITHMETIC OVERFLOW TRAP INSTRUCTION	
422	EXECUTIVE STACK OVERFLOW TRAP INSTRUCTION	
423	EXECUTIVE TRAP 3 TRAP INSTRUCTION	
424	RESERVED	
507	RESERVED	
510	TIME BASE	
511	RESERVED	
512	PERFORMANCE ANALYSIS COUNT	
513	RESERVED	
514	INTERVAL COUNTER INTERRUPT INSTRUCTION	
515	RESERVED	
577	RESERVED	
600	EXECUTIVE PAGE 0	EXECUTIVE PAGE 1
757	EXECUTIVE PAGE 336	EXECUTIVE PAGE 337
760	RESERVED	
777	RESERVED	

TOPS - 10 PROCESS TABLE  
CONFIGURATION

MR-3699

-21-

USER PROCESS TABLE  
 (ADDRESSED FROM UBR)

0	USER PAGE 0	USER PAGE 1
377	USER PAGE 776	USER PAGE 777
400	EXECUTIVE PAGE 340	EXECUTIVE PAGE 341
417	EXECUTIVE PAGE 376	EXECUTIVE PAGE 377
420	RESERVED	
421	USER ARITHMETIC OVERFLOW TRAP INSTRUCTION	
422	USER STACK OVERFLOW TRAP INSTRUCTION	
423	USER TRAP 3 TRAP INSTRUCTION	
424	MUJO STORED HERE	
425	MUJO OLD PC WORD	
426	MUJO PROCESS CONTEXT WORD	
427	RESERVED	
430	KERNEL NO TRAP MUJO NEW PC WORD	
431	KERNEL TRAP MUJO NEW PC WORD	
432	SUPERVISOR NO TRAP MUJO NEW PC WORD	
433	SUPERVISOR TRAP MUJO NEW PC WORD	
434	CONCEALED NO TRAP MUJO NEW PC WORD	
435	CONCEALED TRAP MUJO NEW PC WORD	
436	PUBLIC NO TRAP MUJO NEW PC WORD	
437	PUBLIC TRAP MUJO NEW PC WORD	
440	RESERVED	
477	PAGE FAIL WORD	
500	PAGE FAIL OLD PC WORD	
501	PAGE FAIL NEW PC WORD	
502	PAGE FAIL NEW PC WORD	
503	RESERVED	
504	USER PROCESS EXECUTION TIME	
505	USER PROCESS EXECUTION TIME	
506	USER MEMORY REFERENCE COUNT	
507	USER MEMORY REFERENCE COUNT	
510	RESERVED	
777	RESERVED	

TOPS - 10 PROCESS TABLE CONFIGURATION

MR-3698

Page Map Entry (TOPS-10 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
ACC	PUB	WRITE	SOFT	CACHE	14	15	16	17	18	19	20	21	22	23	24	25	26
PHYSICAL PAGE NUMBER (ODD VIRTUAL PAGE)																	
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
ACC	PUB	WRITE	SOFT	CACHE	14	16	16	17	18	19	20	21	22	23	24	25	26
PHYSICAL PAGE NUMBER (EVEN VIRTUAL PAGE)																	

00 & 18 0 = NO ACCESS ALLOWED  
 1 = ACCESS ALLOWED  
 01 & 19 0 = PRIVATE  
 1 = PUBLIC

02 & 20 0 = WRITE-PROTECTED  
 1 = WRITABLE  
 03 & 21 SOFTWARE (NOT INTERPERTED BY HARDWARE)  
 04 & 22 0 = CACHE-LOOK BUT DO NOT LOAD  
 1 = CACHEABLE

MR-2194

Map (TOPS-10 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
MODE	0	ACC	WRITE	SOFT	0	PUB	CACHE	1	0	0	0	0	0	14	15	16	17
PHYSICAL ADDRESS																	
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
PHYSICAL ADDRESS																	

257000

NOTE: THIS REPRESENTS THE CONTENTS OF AC IF NO ERRORS OCCURRED.

00	0 = EXEC MODE	04	SOFTWARE (NOT INTERPERTED BY HARDWARE)
	1 = USER MODE	06	0 = PRIVATE
02	0 = NO ACCESS ALLOWED		1 = PUBLIC
	1 = ACCESS ALLOWED	07	0 = CACHE LOOK BUT DO NOT LOAD
03	0 = WRITE PROTECTED		1 = CACHEABLE
	1 = WRITABLE		

MR-3824

Map (TOPS-10 Only)

257000

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	
MODE	1		FAILURE TYPE		PUB	CACHE	1	0	0	0	0	0	0	0	14	15	16	17
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	

NOTE: THIS REPRESENTS THE CONTENTS OF AC IF A MAP ERROR IS DETECTED.  
REFER TO OTHER MAP WORD FOR BIT DEFINITIONS.

<01:05> FAILURE TYPE  
21 = PROPRIETARY ERROR  
25 = PAGE TABLE PARITY ERROR

MR-3825

Page Fail Word (TOPS-10 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17				
MODE	0	ACC	WRT	SOFT	REF TYPE	PUB	CACHE	VIRT													
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35				
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35				

00 0 = EXEC MODE  
1 = USER MODE

02 0 = NO ACCESS ALLOWED  
1 = ACCESS ALLOWED

03 0 = WRITE PROTECTED  
1 = WRITABLE

04 SOFTWARE (NOT INTERPERTED BY HARDWARE)

05 0 = READ-ONLY REFERENCE  
1 = REFERENCE INVOLVED A WRITE

06 0 = PRIVATE  
1 = PUBLIC

07 0 = CACHE LOOK BUT DO NOT LOAD  
1 = CACHEABLE

08 A 1 INDICATES A VIRTUAL ADDRESS WAS GIVEN FOR THE REFERENCE

MR-2193

*Handwritten notes:*  
8M W4  
VIRT MODE ONLY  
800 900 205 2  
A 205 2  
M 205 2

Page Fail Word (TOPS-10 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
MODE	PAGE FAIL CODE							VIRT									
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

NOTE: REFER TO OTHER PAGE FAIL WORD FOR BIT DEFINITIONS.

<01:05>  
 PAGE FAIL CODES  
 21 PROPRIETARY VIOLATION  
 22 REFILL ERROR  
 23 ADDRESS FAILURE

<01:06>  
 CONT

PAGE TABLE PARITY ERROR  
 EXEC MODE AR DATA PARITY ERROR  
 EXEC MODE ARX DATA PARITY ERROR  
 USER MODE AR DATA PARITY ERROR  
 USER MODE ARX DATA PARITY ERROR

26  
 36  
 37  
 76  
 77

MR-3823



EXECUTIVE PROCESS TABLE  
(ADDRESSED FROM EBR)

0	EIGHT CHANNEL LOGOUT AREAS EACH: 0 INITIAL CHANNEL COMMAND 1 GETS CHANNEL STATUS WORD 2 GETS LAST UPDATED COMMAND 3 RESERVED
37	
40	RESERVED
41	
42	STANDARD PRIORITY INTERRUPT INSTRUCTIONS
57	
60	FOUR CHANNEL BLOCK FILL WORDS
63	
64	RESERVED
137	
140	FOUR DTE20 CONTROL BLOCKS EACH: 0 TO11 BYTE POINTER 1 TO10 BYTE POINTER 2 DTE INTERRUPT INSTRUCTION 3 RESERVED 4 EXAMINE PROTECT 5 EXAMINE RELOCATION 6 DEPOSIT PROTECT 7 DEPOSIT RELOCATION
177	
200	RESERVED
420	
421	EXECUTIVE ARITHMETIC OVERFLOW TRAP INSTRUCTION
422	EXECUTIVE STACK OVERFLOW TRAP INSTRUCTION
423	EXECUTIVE TRAP 3 TRAP INSTRUCTION
424	
	RESERVED
507	
510	TIME BASE
511	
512	PERFORMANCE ANALYSIS COUNT
513	
514	INTERVAL COUNTER INTERRUPT INSTRUCTION
515	
	RESERVED
537	
540	EXECUTIVE SECTION 0
577	EXECUTIVE SECTION 37
600	
	RESERVED
777	

SINGLE-SECTION TOPS-20 PROCESS  
TABLE CONFIGURATION

MR-3702

USER PROCESS TABLE  
 (ADDRESSED FROM UBR)

0	RESERVED	NOTE: ASTERISKS INDICATE LOCATIONS WHOSE USE DIFFERS FROM THOSE IN THE EXTENDED PROCESS TABLE LISTED ON THE PRECEDING PAGE.	
420			
421			USER ARITHMETIC OVERFLOW TRAP INSTRUCTION *
422			USER STACK OVERFLOW TRAP INSTRUCTION *
423			USER TRAP 3 TRAP INSTRUCTION *
424			RESERVED *
425			MUJO STORED HERE *
426			MUJO OLD PC WORD *
427			MUJO PROCESS CONTEXT WORD *
430			KERNEL NO TRAP MUJO NEW PC WORD *
431			KERNEL TRAP MUJO NEW PC WORD *
432			SUPERVISOR NO TRAP MUJO NEW PC WORD *
433			SUPERVISOR TRAP MUJO NEW PC WORD *
434			CONCEALED NO TRAP MUJO NEW PC WORD *
435			CONCEALED TRAP MUJO NEW PC WORD *
436			PUBLIC NO TRAP MUJO NEW PC WORD *
437			PUBLIC TRAP MUJO NEW PC WORD *
440			RESERVED
477			PAGE FAIL WORD *
500			PAGE FAIL FLAGS *
501			PAGE FAIL OLD PC WORD *
502			PAGE FAIL NEW PC WORD *
503			USER PROCESS EXECUTION TIME
504			USER MEMORY REFERENCE COUNT
505			RESERVED
506			RESERVED
507			RESERVED
510			RESERVED
537			USER SECTION 0
540			USER SECTION 37
577			RESERVED
600			RESERVED
777			RESERVED

SINGLE-SECTION TOPS-20 PROCESS  
 TABLE CONFIGURATION (CONT)

MR-3703

EXECUTIVE PROCESS TABLE  
(ADDRESSED FROM EBR)

0	EIGHT CHANNEL LOGOUT AREAS EACH: 0 INITIAL CHANNEL COMMAND 1 GETS CHANNEL STATUS WORD 2 GETS LAST UPDATED COMMAND 3 RESERVED
37	
40	RESERVED
41	
42	STANDARD PRIORITY INTERRUPT INSTRUCTIONS
57	
60	FOUR CHANNEL BLOCK FILL WORDS
63	
64	RESERVED
137	
140	FOUR DTE20 CONTROL BLOCKS EACH: 0 TO11 BYTE POINTER 1 TO10 BYTE POINTER 2 DTE INTERRUPT INSTRUCTION 3 RESERVED 4 EXAMINE PROTECT 5 EXAMINE RELOCATION 6 DEPOSIT PROTECT 7 DEPOSIT RELOCATION
177	
200	RESERVED
420	
421	EXECUTIVE ARITHMETIC OVERFLOW TRAP INSTRUCTION
422	EXECUTIVE STACK OVERFLOW TRAP INSTRUCTION
423	EXECUTIVE TRAP 3 TRAP INSTRUCTION
424	
	RESERVED
507	
510	TIME BASE
511	
512	PERFORMANCE ANALYSIS COUNT
513	
514	INTERVAL COUNTER INTERRUPT INSTRUCTION
515	
	RESERVED
537	
540	EXECUTIVE SECTION 0
577	EXECUTIVE SECTION 37
600	
	RESERVED
777	

EXTENDED TOPS - 20 PROCESS TABLE  
CONFIGURATION

MR-3700

USER PROCESS TABLE  
 (ADDRESSED FROM UBR)

0		
		NOTE: * ASTERISKS INDICATE * LOCATIONS WHOSE * USE DIFFERS FROM * THOSE IN THE * SINGLE SECTION * PROCESS TABLE * LISTED ON THE * NEXT PAGE.
	RESERVED	
417		
420	ADDRESS OF LUUO BLOCK	*
421	USER ARITHMETIC OVERFLOW TRAP INSTRUCTION	
422	USER STACK OVERFLOW TRAP INSTRUCTION	
423	USER TRAP 3 TRAP INSTRUCTION	
424	MUJO FLAGS	MUJO OP CODE, A *
425	MUJO OLD PC	*
426	E OF MUJO	*
427	MUJO PROCESS CONTEXT WORD	
430	KERNEL NO TRAP MUJO NEW PC	*
431	KERNEL TRAP MUJO NEW PC	*
432	SUPERVISOR NO TRAP MUJO NEW PC	*
433	SUPERVISOR TRAP MUJO NEW PC	*
434	CONCEALED NO TRAP MUJO NEW PC	*
435	CONCEALED TRAP MUJO NEW PC	*
436	PUBLIC NO TRAP MUJO NEW PC	*
437	PUBLIC TRAP MUJO NEW PC	*
440		
	RESERVED	
477		
500	PAGE FAIL WORD	*
501	PAGE FAIL FLAGS	*
502	PAGE FAIL OLD PC	*
503	PAGE FAIL NEW PC	*
504	USER PROCESS EXECUTION TIME	
505		
506	USER MEMORY REFERENCE COUNT	
507		
510		
	RESERVED	
537		
540	USER SECTION 0	
577	USER SECTION 37	
600		
	RESERVED	
777		

EXTENDED TOPS - 20 PROCESS TABLE  
 CONFIGURATION (CONT)

CST ENTRY

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
					PAGE AGE												
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

NOTE: AGE TRAP OCCURS IF BITS <00:05> EQUAL ZERO.

MR-2162

Page Map Entry (TOPS-20 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
ACC	PUB	MOD	WRT	CACHE	14	15	16	17	18	19	20	21	22	23	24	25	26
PHYSICAL PAGE ADDRESS BITS																	

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
ACC	PUB	MOD	WRT	CACHE	14	15	16	17	18	19	20	21	22	23	24	25	26
PHYSICAL PAGE ADDRESS BITS																	

00:18 0 = REFILL REQUIRED TO DETERMINE PAGE ACCESSIBILITY 02 & 20 0 = PAGE NOT MODIFIED  
 1 = ACCESSIBLE 1 = PAGE MODIFIED  
 01 & 19 0 = PRIVATE 03 & 21 0 = WRITE-PROTECTED  
 1 = PUBLIC 1 = WRITABLE  
 04 & 22 0 = CACHE-LOOK BUT DO NOT LOAD  
 1 = CACHEABLE

MR-3828

MAP POINTER — No Access (TOPS-20 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
POINTER TYPE																	
0	0																
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
[Hatched area]																	

MR-3831

MAP POINTER — Immediate (TOPS-20 Only)

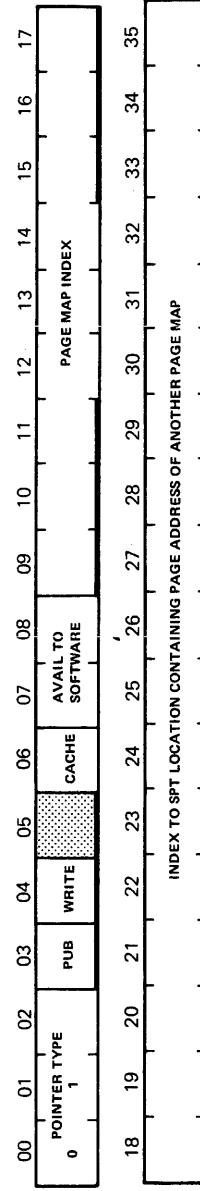
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	
POINTER TYPE		PUB		WRITE		CACHE		AVAILABLE TO SOFTWARE				STORAGE MEDIUM						
0	0	1																
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	
AVAILABLE TO SOFTWARE				PAGE NUMBER FOR MAPPING														
				14	15	16	17	18	19	20	21	22	23	24	25	26		

03 0 = PRIVATE  
1 = PUBLIC  
04 0 = WRITE PROTECTED  
1 = WRITABLE

06 0 = CACHE-LOOK BUT DO NOT LOAD  
1 = CACHEABLE  
<12:17> NON-ZERO INDICATES PAGE NOT IN MEMORY

MR-2149

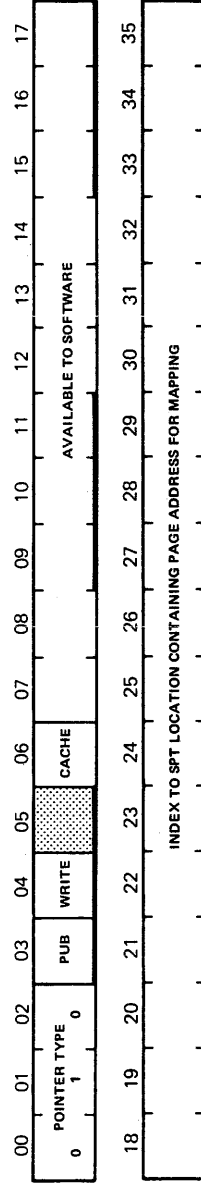
MAP POINTER -- Indirect (TOPS-20 Only)



NOTE: REFER TO IMMEDIATE POINTER FOR BIT DEFINITIONS.

MR-2151

MAP POINTER -- Shared (TOPS-20 Only)



NOTE: REFER TO IMMEDIATE POINTER FOR BIT DEFINITIONS.

MR-2150



SECTION POINTER - No Access (TOPS-20 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
POINTER TYPE																	
0	0	0															

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
MR-3832																	

SECTION POINTER - Immediate (TOPS-20 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
POINTER TYPE		PUB		WRITE		CACHE		AVAILABLE TO SOFTWARE				STORAGE MEDIUM					
0	0	1															

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
AVAILABLE TO SOFTWARE				14	15	16	17	18	19	20	21	22	23	24	25	26	
PAGE NUMBER OF PAGE MAP																	

03	06
04	<12:17>

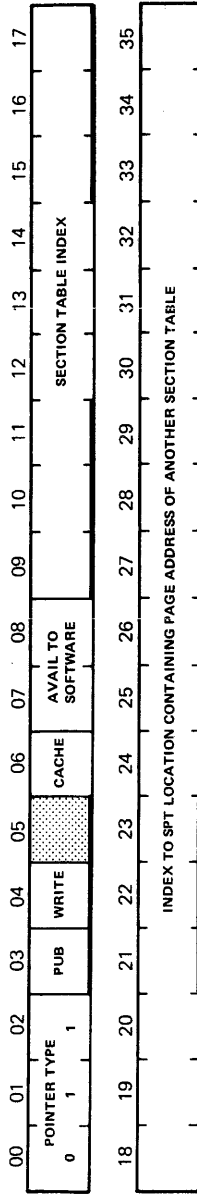
  

0 = PRIVATE  
1 = PUBLIC  
0 = WRITE-PROTECTED  
1 = WRITABLE

0 = CACHE-LOOK BUT DO NOT LOAD  
1 = CACHE/ABLE  
NON-ZERO INDICATES PAGE MAP IS NOT IN MEMORY

MR-3833

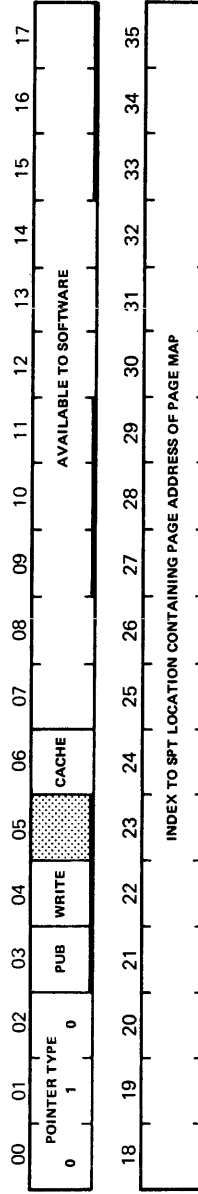
SECTION POINTER -- Indirect (TOPS-20 Only)



MR-3834

NOTE: REFER TO IMMEDIATE POINTER FOR BIT DEFINITIONS.

SECTION POINTER -- Shared (TOPS-20 Only)



MR-3835

NOTE: REFER TO IMMEDIATE POINTER FOR BIT DEFINITIONS.

Map (TOPS-20 Only)

267000

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
MODE	0	1	MOD	WRT	0	PUB	CACHE	1	0	0	0	0	0	14	15	16	17
PHYSICAL ADDRESS																	
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

NOTE: THIS REPRESENTS THE CONTENTS OF AC IF NO ERRORS OCCURRED.

- 00 0 = EXEC MODE 06 0 = PRIVATE
- 1 = USER MODE 1 = PUBLIC
- 03 0 = PAGE NOT MODIFIED 07 0 = CACHE-LOOK BUT DO NOT LOAD
- 1 = PAGE MODIFIED 1 = CACHEABLE
- 04 0 = WRITE PROTECTED
- 1 = WRITABLE

MR-3829

Map (TOPS-20 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
MODE			FAILURE TYPE			UNDEFINED			0	0	0	0	0			UNDEFINED	
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
								UNDEFINED									

NOTE: THIS REPRESENTS THE CONTENTS OF AC IF A MAP ERROR IS DETECTED.

00 0 = EXEC MODE  
 1 = USER MODE

FAILURE TYPE

00 = AGE, NO ACCESS OR NOT-IN-MEMORY IN A REFILL  
 21 = PROPRIETARY VIOLATION  
 25 = PAGE TABLE PARITY ERROR

<01:05>  
 CONT

27 = ILLEGAL ADDRESS - SECTION > 37  
 36 = AR DATA PARITY ERROR

Page Fail Word (TOPS-20 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
MODE	0	ACC	MOD	WRT	REF TYPE	PUB	CACHE	VIRT					13	14	15	16	17

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
VIRTUAL ADDRESS (PHYSICAL FOR MAP)																	
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

- 00 0 = EXEC MODE
- 1 = USER MODE
- 02 0 = REFILL REQUIRED TO DETERMINE PAGE ACCESSIBILITY
- 1 = ACCESSIBLE
- 03 0 = PAGE NOT MODIFIED
- 1 = PAGE MODIFIED
- 04 0 = WRITE-PROTECTED
- 1 = WRITABLE
- 05 0 = READ-ONLY REFERENCE
- 1 = REFERENCE INVOLVED A WRITE
- 06 0 = PRIVATE
- 1 = PUBLIC
- 07 0 = CACHE-LOOK BUT DO NOT LOAD
- 1 = CACHEABLE
- 08 A 1 INDICATES A VIRTUAL ADDRESS WAS GIVEN FOR THE REFERENCE

MR-3826

Page Fail Word (TOPS-20 Only)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
MODE	1	PAGE FAIL CODE				VIRT											
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

VIRTUAL ADDRESS (PHYSICAL FOR MAP)

NOTE: REFER TO OTHER PAGE FAIL WORD FOR BIT DEFINITIONS.

<01:05>	PAGE FAIL CODES	<01:05>	25	PAGE TABLE PARITY ERROR
21	PROPRIETARY VIOLATION	27	27	ILLEGAL ADDRESS - SECTION > 37
23	ADDRESS FAILURE	36	36	EXEC MODE ARX DATA PARITY ERROR
24	ILLEGAL INDIRECT	37	37	EXEC MODE ARX DATA PARITY ERROR
		76	76	USER MODE ARX DATA PARITY ERROR
		77	77	USER MODE ARX DATA PARITY ERROR

MR-3827

PC - Program Counter

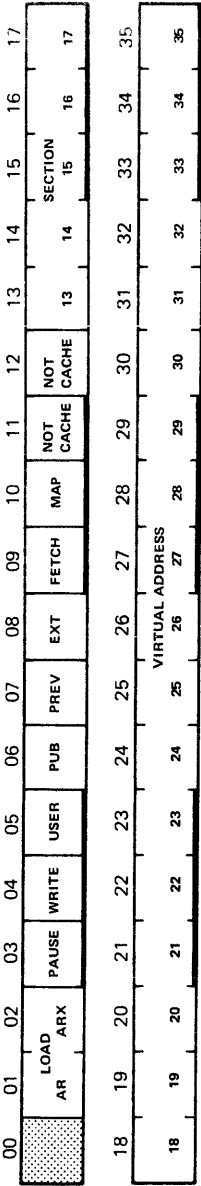
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
OVER FLOW	CARRY 0	FLOAT OVFL0	FPD	USER	USER IOT	PUB	ADDR INH	TRAP 2	TRAP 1	FLOAT UNFLO	NO DIV	CURRENT SECTION 13	CURRENT SECTION 14	CURRENT SECTION 15	CURRENT SECTION 16	CURRENT SECTION 17	
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

04 FIRST PART DONE

08 ADDRESS FAILURE INHIBIT

MR-2192

VMA - FORMAT

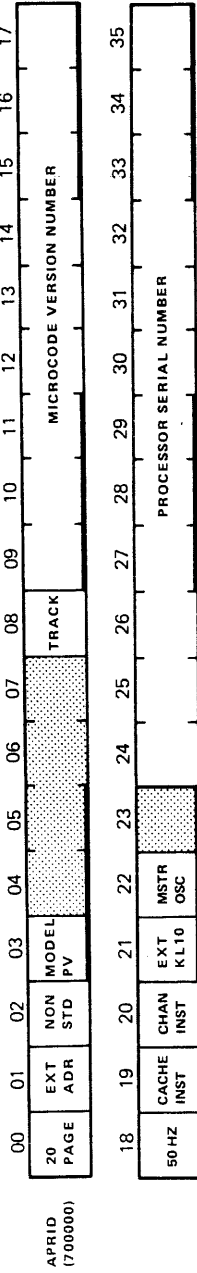


NOTE: THIS IS THE INTERMEDIATE WORD STORED BY THE MICROCODE AT LOCATION SV. VMA DURING A PAGE TABLE REFILL.  
THE STATUS BITS MAY BE READ VIA DIAGNOSTIC FUNCTIONS.

- |    |                  |    |                               |
|----|------------------|----|-------------------------------|
| 01 | FR 106 BIT 18(1) | 07 | FR 106 BIT 19(0)              |
| 02 | FR 106 BIT 18(1) | 08 | FR 107 BIT 19(0)              |
| 03 | FR 103 BIT 18(1) | 09 | FR 107 BIT 20(1) KL10 PV ONLY |
| 04 | FR 104 BIT 18(1) | 10 | FR 107 BIT 23(0)              |
| 05 | FR 104 BIT 19(1) | 11 | FR 104 BIT 23(1)              |
| 06 | FR 105 BIT 19(1) | 12 | FR 105 BIT 23(1)              |



BLKI APP,



NOTE: BITS <00:08> ARE MICROCODE OPTIONS  
 BITS <18:23> ARE HARDWARE OPTIONS

00	MICROCODE IS FOR TOPS-20 PAGING	08	MICROCODE VERSION SUPPORTS TRACKING
01	MICROCODE HANDLES EXTENDED ADDRESSES	19	CACHE INSTALLED
02	NON-STANDARD MICROCODE	20	CHANNELS INSTALLED
03	MODEL PV TYPE PROCESSOR	21	CPU IS AN EXTENDED KL10
		22	MASTER OSCILLATOR (KW20 OPTION)

MR-2067

CONI APR,

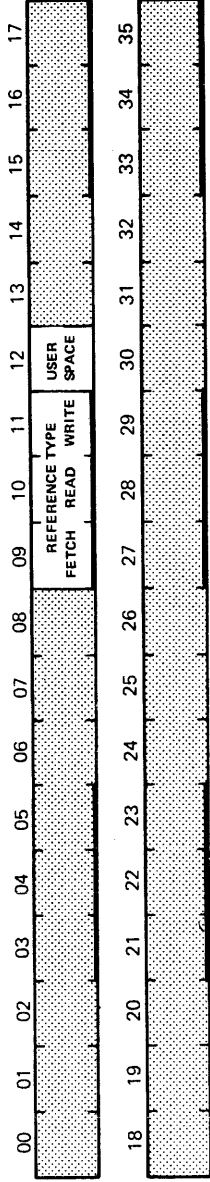
APR  
(700240)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
						SBUS ERROR	NXM	I/O PGF	MB PE	CACHE DIR	ADR PE	POWER FAIL	SWEEP DONE				
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
	SWEEP BUSY		MSTR OSC			SBUS ERROR	NXM	I/O PGF	MBUS PE	CACHE DIR	ADR PE	POWER FAIL	SWEEP DONE	INT REQ			PI LEVEL

06 INTERRUPT ON: SBUS ERROR  
 07 : NONEXISTENT MEMORY  
 08 : I/O PAGE FAIL  
 09 : MB PARITY ERROR  
 10 : CACHE DIR PARITY ERROR  
 11 : ADDRESS PARITY ERROR  
 12 : POWER FAILURE  
 13 : CACHE SWEEP DONE  
 19 CACHE SWEEP IN PROGRESS  
 22 MASTER OSCILLATOR (KW20 OPTION)

24 SBUS ERROR  
 25 NONEXISTENT MEMORY  
 26 I/O PAGE FAILURE  
 27 MB PARITY ERROR  
 28 CACHE DIRECTORY PARITY ERROR  
 29 ADDRESS PARITY ERROR  
 30 POWER FAILURE  
 31 CACHE SWEEP DONE  
 32 INTERRUPT REQUEST

DATAI APR,

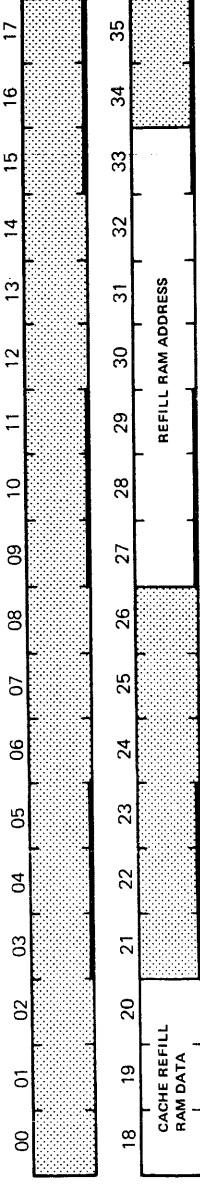


APR  
(700040)

NOTE: REFER TO DATAQ APR FOR BIT DEFINITIONS

MR-2068

BLKO APR, (WRFIL)



APR  
(700100)

MR-2066

CONO APR,

APR (700200)	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
	I/O RESET	EN ABLE	DIS ABLE	CLEAR SET	SBUS ERROR	NXM	I/O PGF	MB PE	CACHE DIR	ADR PE	POWER FAIL	SWEEP DONE					PIA	

20	ENABLE	SELECTED FLAGS <24:31>	24	SELECT FLAG:	SBUS ERROR
21	DISABLE	SELECTED FLAGS <24:31>	25	:	NON-EX-MEMORY
22	CLEAR	SELECTED FLAGS <24:31>	26	:	I/O PAGE FAIL
23	SET	SELECTED FLAGS <24:31>	27	:	MB PARITY ERROR
			28	:	CACHE DIR PARITY ERROR
			29	:	ADDRESS PARITY ERROR
			30	:	POWER FAIL
			31	:	CACHE SWEEP DONE

MR-2063

DATA ADDRESS

APR (700140)	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
											REFERENCE TYPE	USER						
											FETCH	READ						

	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
	ADDRESS																	

<09:12> ADDRESS BREAK ENABLES

MR-2065

BLKI MTR,

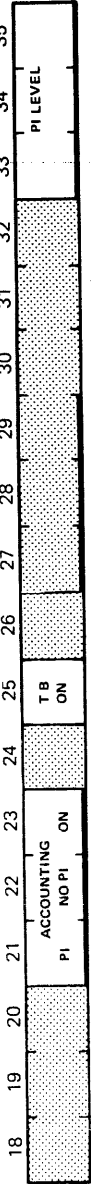
ROMACT  
(702400)

READ MBOX ACCOUNT DOUBLEWORD

MR-2081

CONI MTR,

702640



25 TIME BASE ON

MR-2089

DATAI MTR,

RDEACT  
(702440)

READ EBOX ACCOUNT DOUBLEWORD

MR-2080

CONO MTR,

702600

18	LOAD ACCT
19	
20	
21	ACCOUNTING PI NO PI ON
22	
23	
24	TIME BASE OFF ON CLEAR
25	
26	
27	
28	
29	
30	
31	
32	
33	
34	PI LEVEL
35	

MR-2089

CONI PAG,

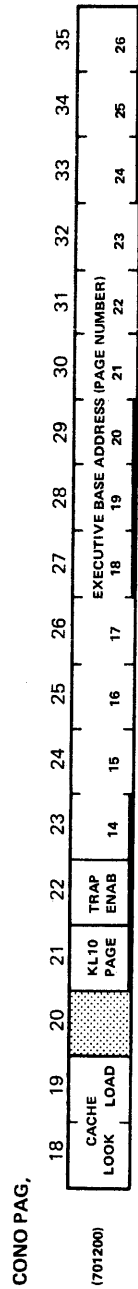
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
PAG (701240)	CACHE LOOK LOAD		KL10 PAGE	TRAP ENAB	14	15	16	17	18	19	20	21	22	23	24	25	26
	EXECUTIVE BASE ADDRESS (PAGE NUMBER)																
	22      ENABLE PAGER AND PAGE TRAPS																
21	0 - TOPS-10 PAGING 1 - TOPS-20 PAGING																

MR-2145

DATAI PAG,

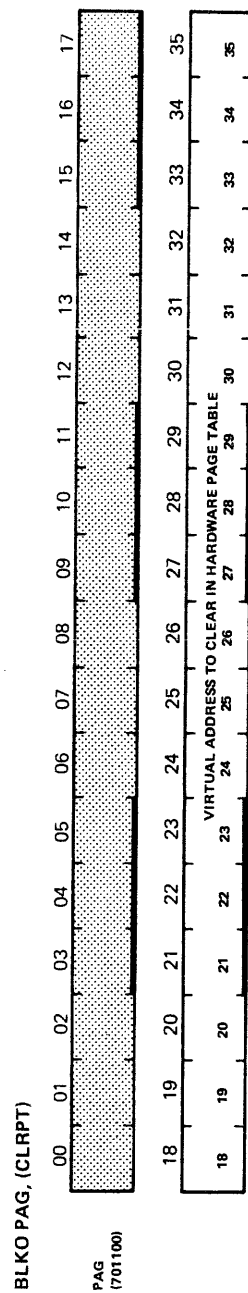
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
PAG (701040)	1	1	1			CURRENT AC BLK 04 02 01			PREVIOUS AC BLK					PREVIOUS CONTEXT SECTION 13 14 15 16 17			
	18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35																
	USER BASE ADDRESS (PAGE NUMBER)																
	14 15 16 17 18 19 20 21 22 23 24 25 26																

MR-2147



NOTE: REFER TO CONI/PAG FOR BIT DEFINITIONS.

MR-2144



MR-2148



DATA0 PAG,

PAG  
(701140)

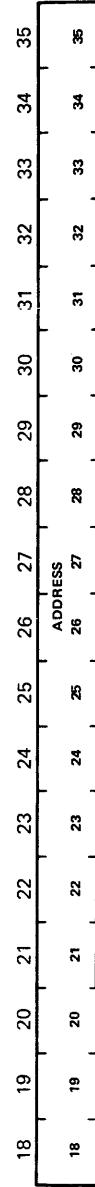
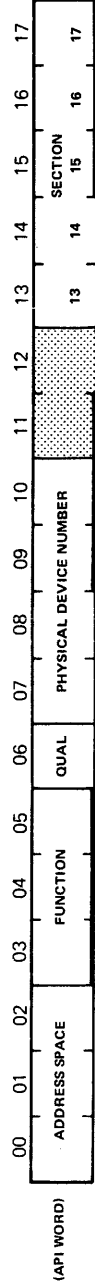
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
SEL AC	SEL PCS	LOAD UBA	[Patterned]		CURRENT AC BLK 04 02 01		PREVIOUS AC BLK 04 02 01		PREVIOUS AC BLK 04 02 01		[Patterned]		PREVIOUS CONTEXT SECTION 13 14 15 16 17				
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
USER ACCT	[Patterned]		[Patterned]		14	15	16	17	USER BASE ADDRESS (PAGE NUMBER) 18 19 20 21 * 22								

00 SELECT AC BLOCKS <06:08>  
01 SELECT PREVIOUS CONTEXT SECTION <09:11>

02 LOAD USER BASE ADDRESS  
18 1 = DO NOT UPDATE USER ACCOUNTS

MR-2146

IOP FUNCTION WORD

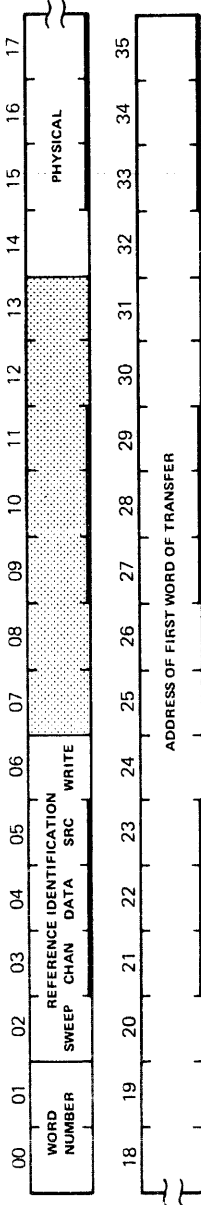


- <00:02> 0 = EPT 1 = EXECUTE VIRTUAL
  - 4 = PHYSICAL
  - 0 = STANDARD (40 + 2N) INTERRUPT
  - 1 = STANDARD INTERRUPT (40 + 2N)
  - 2 = VECTOR INTERRUPT (XCT (13-35))
  - 3 = INCREMENT [QUAL = > DECREMENT]
  - 4 = DATAO (EXAMINE) [QUAL = > PROTECTED]
- 5 = DATAI (DEPOSIT) [QUAL = > PROTECTED]
  - 6 = BYTE [QUAL = > TO -10]
  - 7 = STANDARD (40 + 2n) INTERRUPT
  - n = DTE NUMBER
  - 0-7 = RH20
  - 10-13 = DTE20
  - 17 = DIA 20

MR-2195

BLK1PI,

PI  
(700400)  
(RDERA)



02 REF MADE FOR CACHE SWEEP  
03 REF MADE FOR CHANNEL XFER  
04 DATA

05 SOURCE  
06 WRITE

BIT <04:06> COMBINATIONS

04	05	06 (WRITE = 0)	06 (WRITE = 1)
0	0	MEMORY (RD OR RPW)	CHAN STORE STATUS
0	1		CHAN STORE DATA
1	0	READ FROM CACHE (PAGE REFILL OR CHAN READ)	EBOX STORE FROM AR
1	1		CACHE WRITEBACK

MR-2162

CONI PI,

PI (700640)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
PI										PROGRAM REQUEST LEVELS							
PI										01	02	03	04	05	06	07	

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
WR EVEN PAR		PI IN PROGRESS		PI		PI CHANNELS ON		PI		PI		PI		PI		PI	
ADR DATA DIR		01	02	03	04	05	06	07	ON	01	02	03	04	05	06	07	

MR-2185

DATAI PI,

PI (700440)

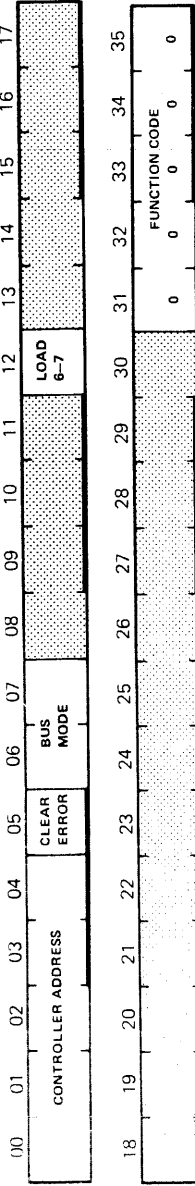
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
PI																	

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
PHYSICAL ADDRESS OF LAST PC STORED IN BUFFER																	

NOTE: TRACKS ONLY

MR-2187

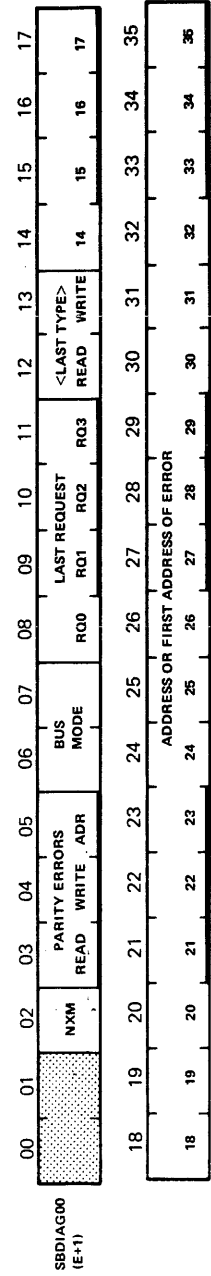
BLKO PI, (SBus Diagnostic Function Code 00) DMA



SBDIAG 00  
(700500)

NOTE: THIS BIT MAP APPLIES TO DMA20S ONLY.

- <00:04> CONTROLLER ADDRESS
  - 04 = DMA20
- 05 CLEAR ERROR - CLEARS CONTROLLER'S ERROR
  - FLAGS NXM, RD PE, WR PE AND ADR PE
- <06:07> BUS MODE
  - 0 = OFF LINE
  - 1 = 1 BUS MODE
  - 2 = 2 BUS MODE
  - 3 = 4 BUS MODE
- 12 LOAD ENABLE - ENABLES LOADING OF BITS 6-7.
  - 0 = READ ONLY
  - 1 = LOAD AND READ BACK



NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO P1, (FUNCT 00). THIS BIT MAP APPLIES TO DMAZ05 ONLY.

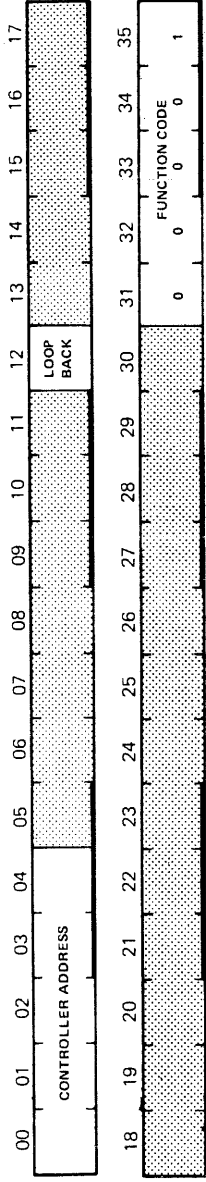
<06:07>  
 BUS MODE  
 0 - OFF LINE  
 1 - 1 BUS MODE  
 2 - 2 BUS MODE  
 3 - 4 BUS MODE

MR-3815

-50F-

BLKO PI, (SBus Diagnostic Function Code 01) DMA

SBDIAG01  
(700500)

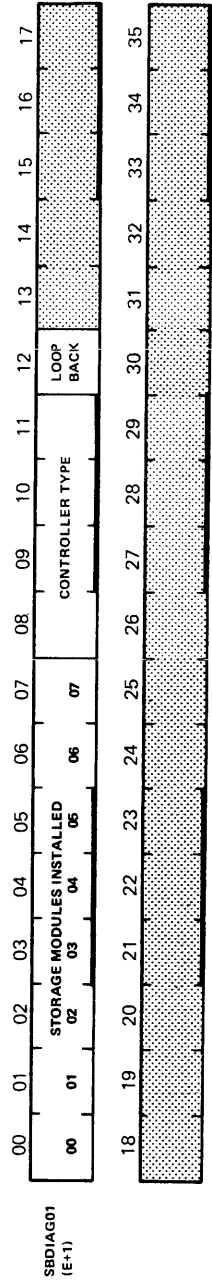


NOTE: THIS BIT MAP APPLIES TO DMA20S ONLY.

<00:04>  
12

REFER TO SBDIAG FUNCTION 00  
SET LOOP-AROUND MODE-INHIBITS READ/WRITE  
CURRENTS IN STORAGE MODULES. A DIAGNOSTIC  
FEATURE FOR CHECKING DATA PATH INDEPENDENT  
OF CORE ACTIVITY

MR-3816



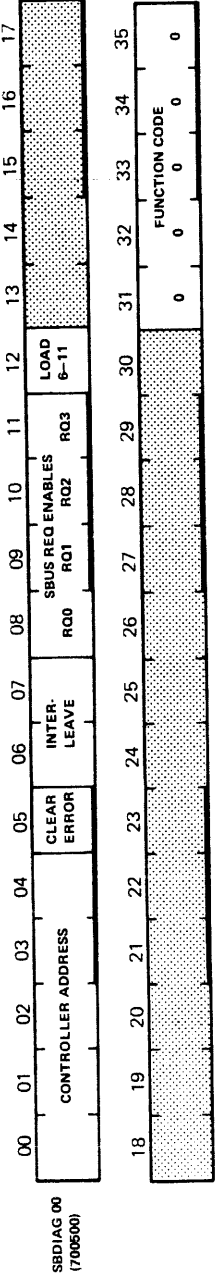
NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI (FUNCT 01). THIS BIT MAP APPLIES TO DMA20S ONLY.

- <00:07> DMA ALWAYS RETURNS 0.
- <08:11> MEMORY ID-THESE HARDWIRED BITS IDENTIFY MEMORY TYPE.
  - 00 - CUSTOMER UNIT
  - 01 - MA20
  - 02 - DMA20
  - 03 - MB20
- 12 LOOP-AROUND MODE - INDICATES CONTROLLER IN LOOP-AROUND MODE.

MR-3817



BLKO P1, (SBus Diagnostic Function Code 00) MA/MB



NOTE: THIS BIT MAP APPLIES TO MA20 AND MB20 MEMORIES ONLY.

<00:04>

CONTROLLER ADDRESS-EACH MA20 CONTROLLER HAS A HARDWIRED ADDRESS 0-3. MC0 AND MC1 CONNECT TO SBUS 0; MC2 AND MC3 TO SBUS 1  
 00 - MC0 FIRST 128K (MA20) OR  
 01 - MC1 FIRST 256K (MB20)  
 02 - MC2 SECOND 128K (MA20) OR  
 03 - MC3 SECOND 256K (MB20)  
 04 = DMA20 (NOT AN MA20 OR MB20 ADDRESS)

05 CLEAR ERROR-CLEARs CONTROLLER'S INTERNAL ERROR FLAGS INCOMPLETE REQUEST AND ADR PAR ERR.

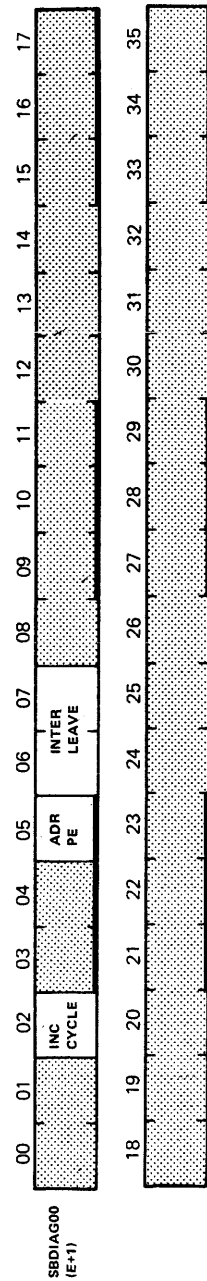
<06:07>

INTERLEAVE  
 0 = OFF LINE FOR DMA20 (NOT AN MA20 OR MB20 OPERATING MODE)  
 1 = NO INTERLEAVE  
 2 = TWO WAY INTERLEAVING  
 3 = FOUR WAY INTERLEAVING

<08:11>

SBUS REG ENABLES  
 RQ0 RQ1 RQ2 RQ3  
 LOAD 6-11  
 SET REQUEST ENABLES-ASSIGNS CONTROLLER ODD-EVEN STATUS  
 00 - CONTROLLER OFF-LINE  
 05 - CONTROLLER ODD (2 WAY AND 4 WAY INTERLEAVE MODES)  
 12 - CONTROLLER EVEN (2 AND 4 WAY INTERLEAVE MODES)  
 17 - CONTROLLER ODD AND EVEN (NO INTERLEAVE MODES)  
 LOAD ENABLE-ENABLES LOADING OF BITS 6-11.  
 0 = READ ONLY  
 1 = LOAD AND READ BACK

12



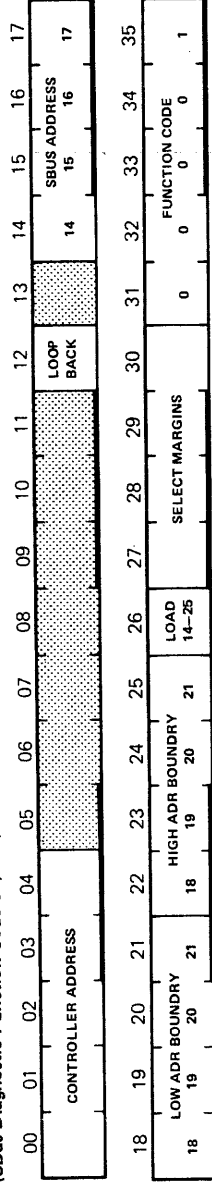
NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKOP1, (FUNCT 00). THIS BIT MAP APPLIES TO MA20 AND MB20 MEMORIES ONLY.

- 02 INCOMPLETE REQUEST INDICATES CONTROLLER ACTIVE
- 05 FOR 10.2 MICROSECONDS: HUNG CONTROLLER.
- ADDRESS PARITY ERROR-INDICATES BAD PARITY DETECTED FOR INFORMATION ON SBUS ADR, RDn, RD RQ, AND WR RQ LINES.
- <06:07> INTERLEAVE MODE-INDICATES INTERLEAVE MODE LOADED IN FIRST HALF OF FUNCTION 0.

MR-2159

BLKO PI, (SBus Diagnostic Function Code 01) MA/MB

SBDIAG01  
(7006500)



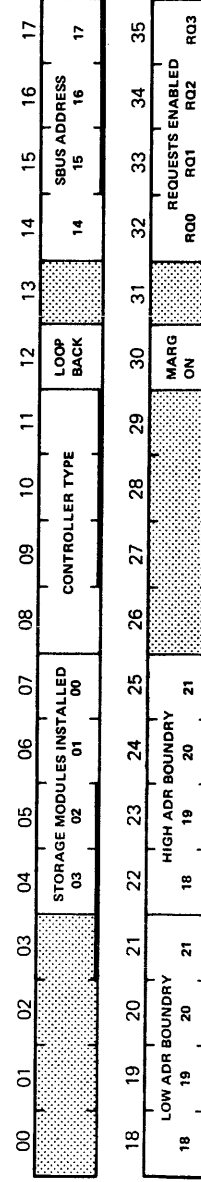
NOTE: THIS BIT MAP APPLIES TO MA20 AND MB20 MEMORIES ONLY.

- <00:04>  
12 REFER TO SBDIAG FUNCTION 00  
SET LOOP AROUND MODE INHIBITS READ/WRITE CURRENTS IN STORAGE MODULES. A DIAGNOSTIC FEATURE FOR CHECKING DATA PATH INDEPENDENT OF CORE ACTIVITY
- <14:17>  
14-17 SET MEMORY ADDRESS-CORRESPOND TO SBUS ADR 14-17. MUST MATCH THE SBUS ADDRESS LINES IF A CONTROLLER IS TO RESPOND TO A MEMORY REFERENCE
- <18:21>  
18-21 SET LOWER ADDRESS BOUNDARY-CORRESPOND TO SBUS ADR 18-21. ACT IN CONJUNCTION WITH MEMORY ADDRESS (BITS 14-17) TO SPECIFY LOWER ADDRESS LIMIT
- <22:25>  
22-25 SET UPPER ADDRESS BOUNDARY-CORRESPOND TO SBUS ADR 18-21. ACT IN CONJUNCTION WITH MEMORY ADDRESS (BITS 14-17) TO SPECIFY UPPER ADDRESS LIMIT
- 26 LOAD ENABLE - ENABLE LOADING BITS <14:25>  
0 = READ ONLY  
1 = LOAD AND READ BACK  
<27:35>  
27-35 SET MARGIN CONTROL-TURN ON MARGIN CONTROL AS SPECIFIED BELOW. ONLY ONE MARGIN SHOULD BE TURNED ON AT ANY ONE TIME

27	28	29	30	31	32	33	34	35
0	0	0	0	0	0	0	0	1
0	0	0	0	1	1	1	1	1
0	0	0	1	X	X	X	X	X
0	1	0	0	X	X	X	X	X
1	0	0	0	X	X	X	X	X

MR-2160

SBD/AG01  
 (E+1)



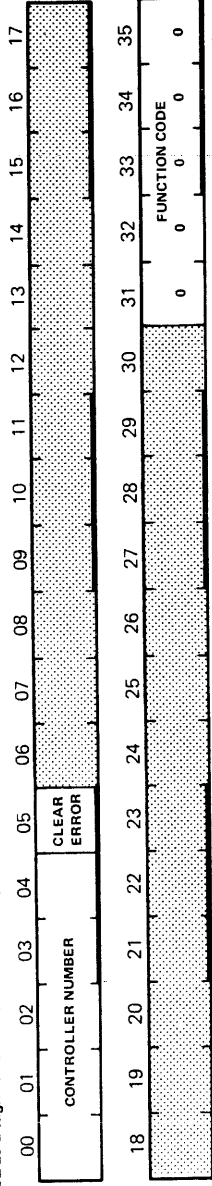
NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BK0 P1 (FUNCT 01). THIS BIT MAP APPLIES TO MA20 AND MB20 MEMORIES ONLY.

- <04:07> STORAGE MODULES CONNECTED - THESE HARDWIRED BITS INDICATE THE NUMBER OF STORAGE MODULES CONNECTED TO A CONTROLLER.
  - 1 = SM CONNECTED
  - 0 = SM NOT CONNECTED
- <08:11> MEMORY ID - THESE HARDWIRED BITS IDENTIFY MEMORY TYPE.
  - 00 = CUSTOMER UNIT
  - 01 = MA20
  - 02 = DNMA20
  - 03 = MB20
- 12 LOOP-AROUND MODE - INDICATES CONTROLLER IN LOOP-AROUND MODE.
  - <14:25> ADDRESS BOUNDARIES - INDICATES ADDRESS BOUNDARIES LOCATED IN FIRST HALF OF FUNCTION 1.
  - 30 MARGINS SELECTED - INDICATES THAT CURRENT STROBE, OR THRESHOLD MARGIN CONTROL IS ON.

MR-2161

BLKO PI (SBus Diagnostic Function Code 00)

SBDIAG00  
(706500)



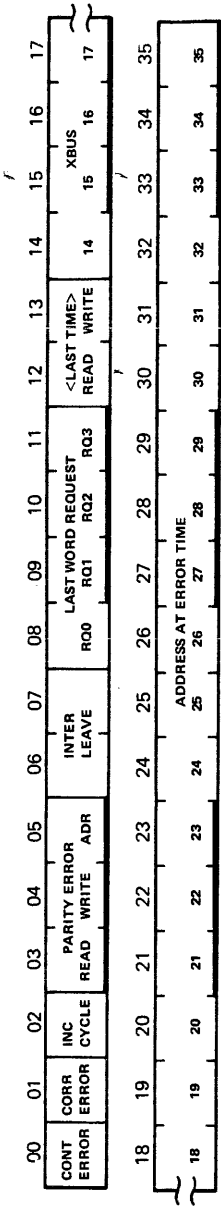
NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY

05 CLEAR ERRORS - REFER TO FUNCT 0  
(E+1) BITS <00:05>

DM 6: 200000 0  
 DM 7: -1  
 EX 700500 6  
 EM 7

MR-2163

SBDIAG00  
(E+1)

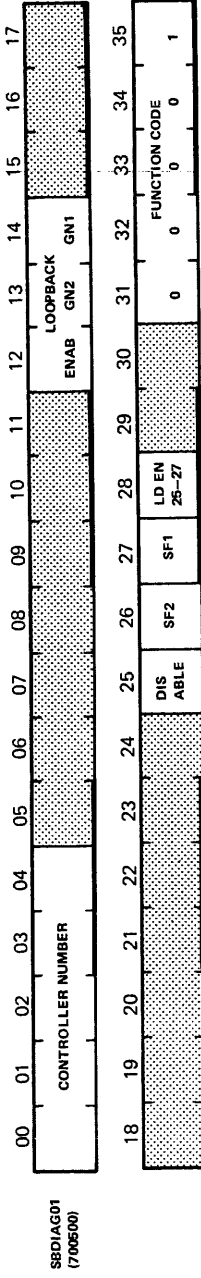


NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO P1, (FUNCT 00). THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY.

- 00 CONTROLLER ERROR - REFER TO FUNCT 2 (E+1)
- 01 CORRECTABLE READ PARITY ERROR
- 02 INCOMPLETE MEMORY CYCLE

MR-2164

BLKO PI (SBus Diagnostic Function Code 01)



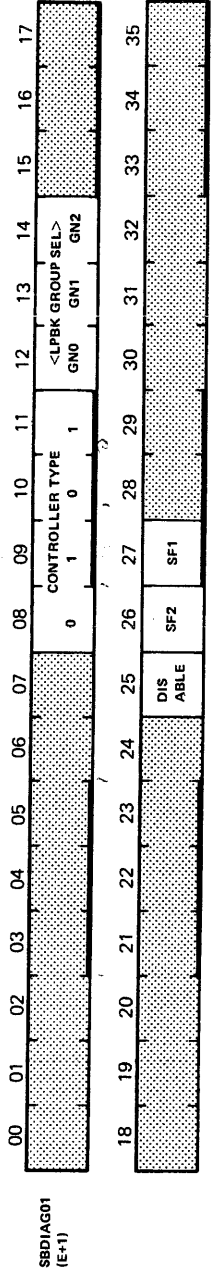
SBDIAG01  
(700600)

NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY. BITS <26:27> ARE SOFTWARE FLAGS. THEY DO NOT EFFECT THE HARDWARE, NOR DOES THE HARDWARE EFFECT THEM.

12 ENABLE LOOPBACK  
<13:14> GROUP NUMBER TO LOOPBACK  
25 DISABLE MF20 (PLACE OFF-LINE)

<26:27>  
00 - MF20 JUST POWER UP  
01 - ALL RAMS EXCEPT ADDRESS RESPONSE RAM LOADED  
10 - ALL RAMS LOADED  
11 - ALL RAMS LOADED AND TGHA HAS BEEN RUN

MR-2165



NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 01)

<08:11> CONTROLLER TYPE (S = MF20)

<12:14> LOOPBACK GROUP SELECTED

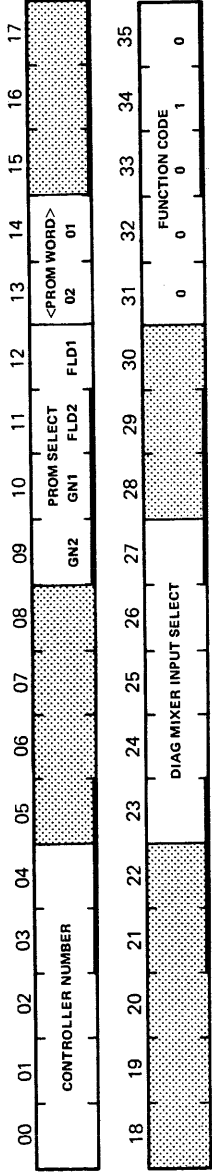
<25:27> REFER TO FUNCT 01 (E) BITS <25:27>

MR-2166



BLKO PI (SBus Diagnostic Function Code 02)

SBDIAG02  
(706500)



NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY.

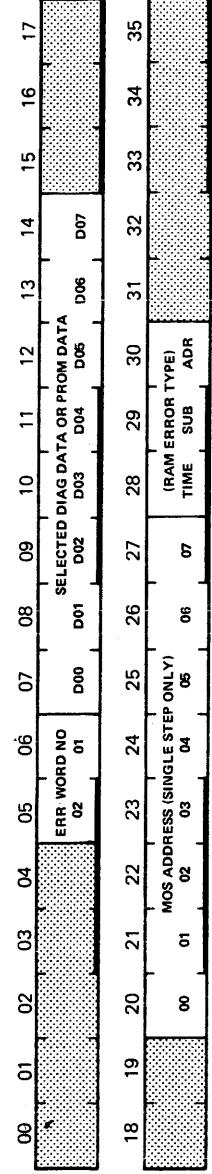
<23:27> WHEN ALL ZEROS, THIS FIELD INDICATES THAT THE CONTENTS OF BITS <07:14> DURING THE SECOND HALF OF THE DIAGNOSTIC CYCLE WILL BE PROM DATA.

<23:27>

WHEN NOT ALL ZEROS, THE BITS ARE USED TO SELECT WHICH MF20 CONTROL SIGNALS WILL APPEAR IN <07:14> DURING THE SECOND HALF OF THE DIAGNOSTIC CYCLE (DIAGNOSTIC DATA).

MR-2167

SBDIAG02  
(E+1)



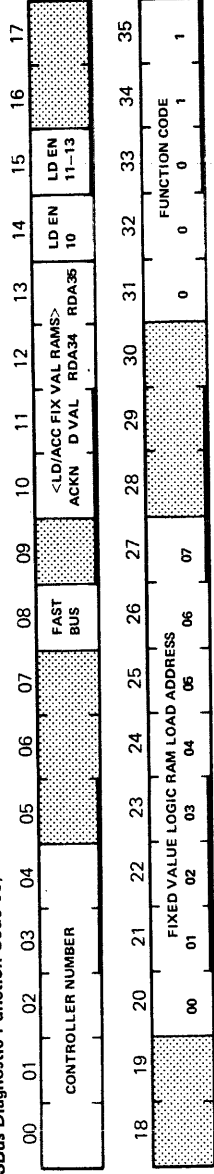
NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 02)

- <06:06> SPECIFY WHICH WORD IN QUAD WORD GROUP CAUSED ERROR
- <07:14> REFER TO FUNCT 02 (E) BITS <23:27>
- 28 RAM TIMING ERROR
- 29 RAM SUBSTITUTION BIT ERROR
- 30 RAM ADDRESS RESPONSE ERROR

MR-2168

BLKO PI (SBus Diagnostic Function Code 03)

SBDIAG03  
(7006500)

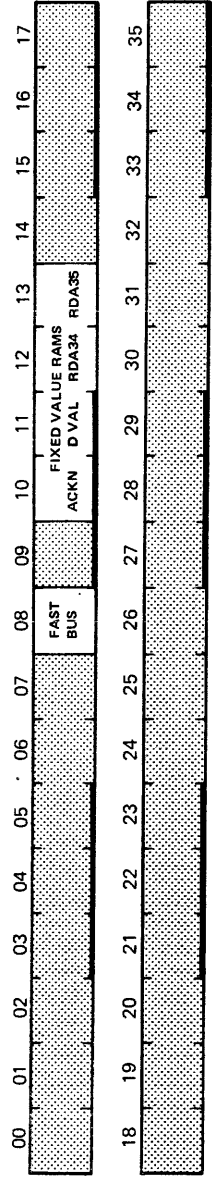


NOTE: THIS BIT MAP APPLIES TO ME20 MEMORIES ONLY.  
THE FAST-BUS (BIT 08) IS DISCONNECTED INTERNALLY. IT IS LEFT IN ONLY FOR DIAGNOSTIC COMPATIBILITY.  
THE ACKN RAM (BIT 10) USES ADDRESS BITS <21:27> ONLY.

10 P ACKN EN BIT  
<10:13> LOAD OR ACCESS FIXED VALUE RAMS

11 SET DATA VALID BIT  
<12:13> P RD ADR 34-35 BITS

MR-2169

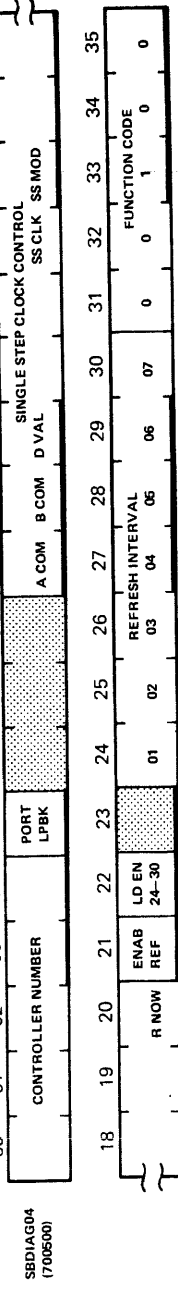


SBDIAG03 (E+1)

NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI. (FUNCT 03). REFER TO FUNCT 03 (E) FOR BIT DEFINITIONS.

MR-2170

BLKO P1, (SBus Diagnostic Function Code 04)



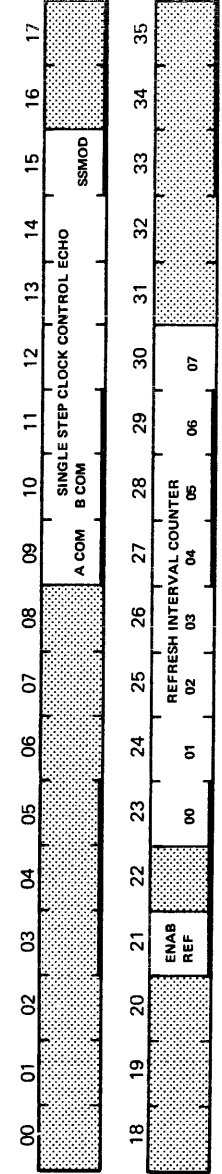
NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY.  
 IF 5 = 1 THE CONTROLLER WILL ONLY ECHO INFORMATION SENT OUT BY AN SBUS DIAG AS LONG AS THE PROPER  
 CONTROLLER NUMBER IS GIVEN. ONLY A SBUS RESET CAN CLEAR THIS CONDITION

06 PORT LOOPBACK  
 09 SIM A PHASE COMING  
 10 SIM B PHASE COMING

11 P DATA VALID IN  
 20 REFRESH NOW  
 21 ENABLE REFRESH

MR-2171

SBDIAG04  
(E\*1)

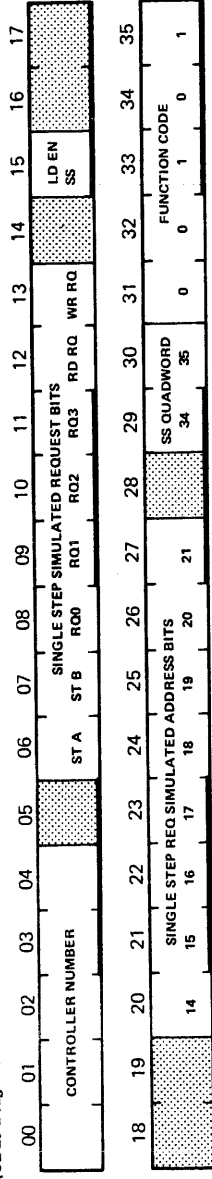


NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY. E\*1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF A BLK0 PI, (FUNCT 04)  
REFER TO FUNCT 4 (E) FOR BIT DEFINITIONS

MR-2172

BLKO P1, (SBus Diagnostic Function Code 05)

SBDIAG05  
(700600)



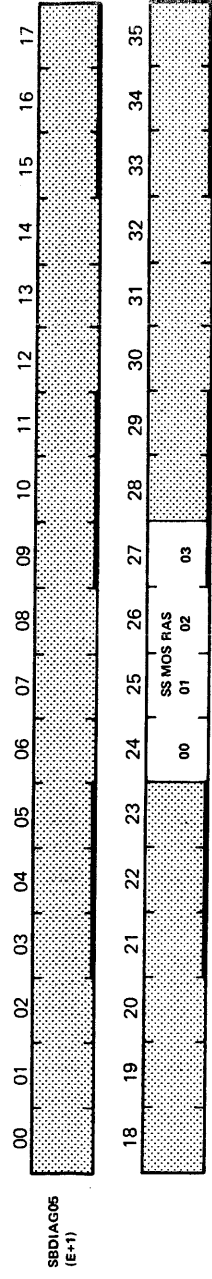
NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY.

- 06 DIAGNOSTIC START A
- 07 DIAGNOSTIC START B

<28-30>

SELECTS QUADWORD FOR DIAGNOSTIC SINGLE STEP OPERATION

MR-2173



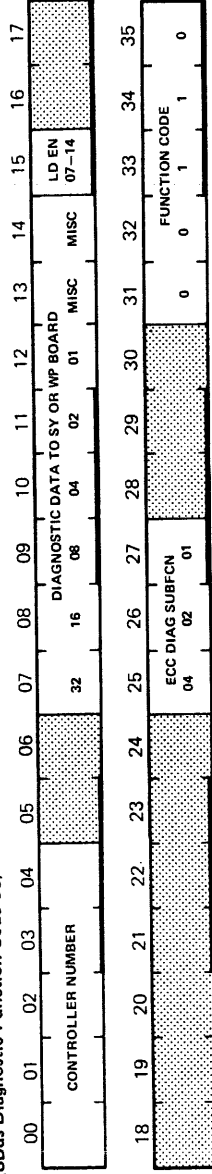
NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLK0 PI, (FUNCT 06)  
 <24:27> ROW ADDRESS STROBE (RAS) BITS

MR-2174



BLKO P1, (SBus Diagnostic Function Code 06)

SBDIAG06  
(700500)



NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY.

<07:14> AN 8-BIT FIELD USED TO SET UP THE DIAGNOSTIC DATA USED TO CONTROL SYN2.M TO CHK ECC.32, 16, 8, 4, 2, 1. PAR TO BE USED AS SPECIFIED BY THE DIAGNOSTIC SUBFUNCTION SPECIFIED IN <25:27>

<25:27> SPECIFIES ONE OF EIGHT SUBFUNCTIONS PERFORMED BY A DIAGNOSTIC FUNCTION CODE 6.

= 0 READ THE ECC REGISTER ON WRP7.

= 1 READ THE SYNDROME BUFFER REGISTER ON THE SYN BOARD.

= 2 SELECT DIAGNOSTIC BITS <07:13> IN PLACE OF MOS BITS <36:42>, FORCE 05 ON <00:35>, RUN A CORRECTION PASS, AND RETURN <00:35>.

<25:27> CONT

= 3 NOT USED

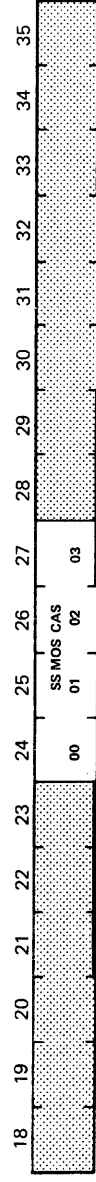
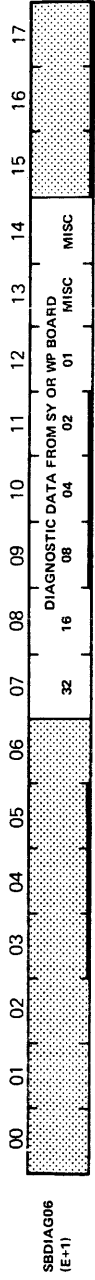
= 4 WRITE THE ECC COMPLEMENT REGISTER IF 15 = 1, THEN READ IT BACK.

= 5 WRITE THE ECC COMPLEMENT REGISTER, THEN ENABLE IT TO BE SENT TO MEMORY IN PLACE OF <36:42> ON THE NEXT WRITE CYCLE.

= 6 READ THE OUTPUT OF THE <36:42> MIXER.

= 7 ENABLE LATCHING OF <36:42> MIXER AFTER NEXT WRITE.

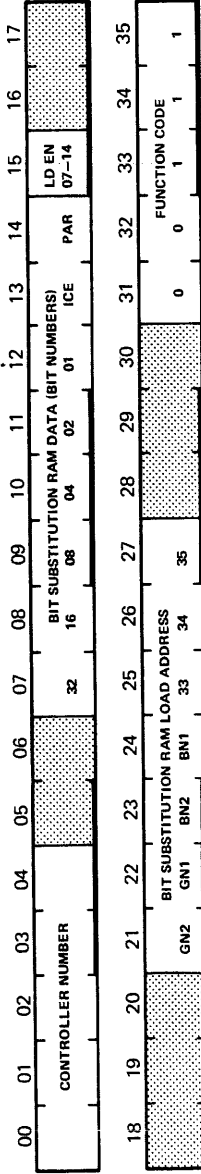
MR-2175



NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO P1, (FUNCT 06).  
 <07:14> REFER TO FUNCT 06 E <07:14>      <24:27> A 4-BIT FIELD THAT DISPLAYS THE STATE OF THE COLUMN ADDRESS STROBE (CAS) SIGNALS ADT5 MOS CAS 0-3.

MR-2176

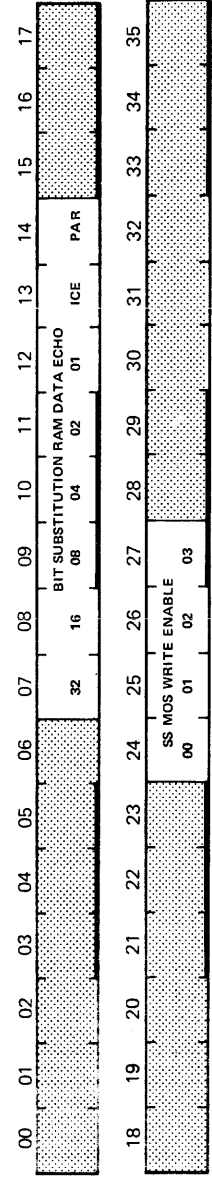
BLKO PI (SBus Diagnostic Function Code 07)



SSDIAG07  
(700500)

NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY.  
"ICE" MEANS IGNORE CORRECTABLE ERROR (I.E., DON'T SET CORR ERR FLAG)

MR-2177



SBDIAG07  
(E+1)

NOTE: THIS BIT MAP APPLIES TO ME20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLK0 PI, (FUNCT 07).  
"ICE" MEANS IGNORE CORRECTABLE ERROR (I.E., DON'T SET CORR ERR FLAG).

MR-2176

BLKO PI, (SBus Diagnostic Function Code 10)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
CONTROLLER NUMBER				VOLTAGE MARGINS +12V +5V -2V -5.2V		MARGIN ENABLES +12V +5V -2V -5.2V		LD EN 07-14									

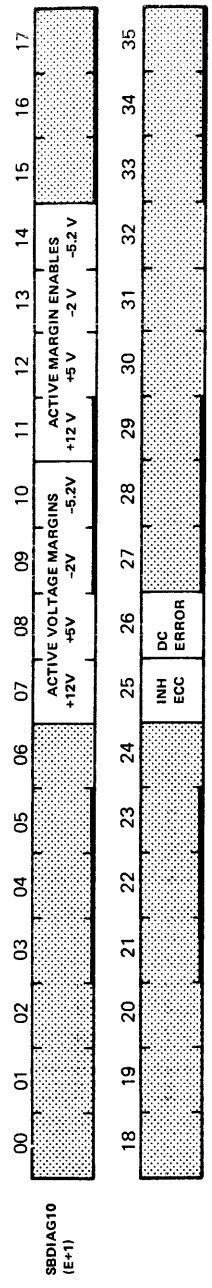
SBDIAG10  
(700500)

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
INH ECC				CLEAR DCBAD		FUNCTION CODE 0 1 0 0 0 0 0 0											

NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY.  
MORE THAN ONE VOLTAGE MARGIN MAY BE SET CONCURRENTLY.

- 07 0 = 11.40, 1 = 12.60
- 08 0 = 4.75, 1 = 5.25
- 09 0 = -1.90, 1 = 2.10
- 10 0 = -4.94, 1 = -5.46

MR-2179

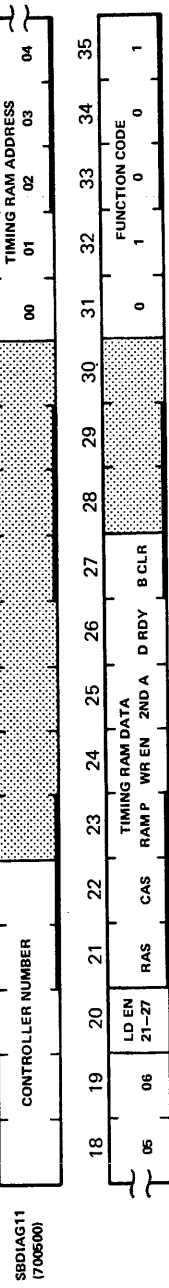


SBDIAG10 (E+1)

NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI. (FUNCT 10). <07:10> REFER TO FUNCT 10 (EI) FOR MARGINS

MR-2180

BLKO P1 (SBus Diagnostic Function Code 11)

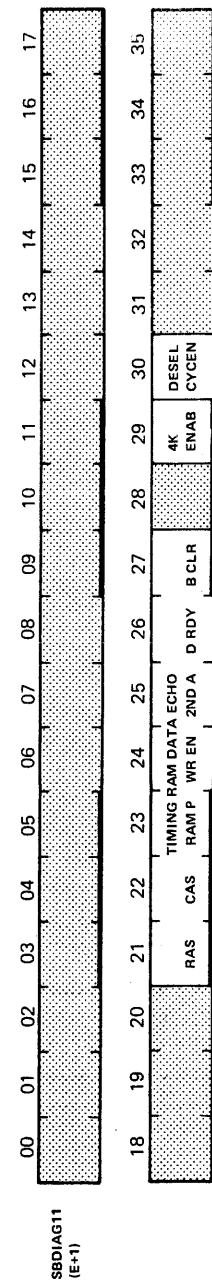


NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY.

- 21 ROW ADDRESS STROBE
- 22 COLUMN ADDRESS STROBE
- 23 RAM PARITY
- 24 WRITE ENABLE

- 25 ADDRESS 2ND HALF
- 26 DATA READY
- 27 RAM BUSY CLEAR

MR-2181



NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKOP I, (FUNCT 11).

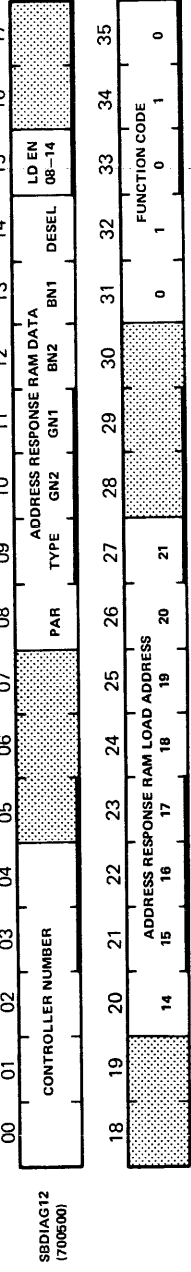
<21:27> REFER TO FUNCT 11 (E) BITS <21:27>  
 28 SPECIFY MOS CHIP SIZE

30 DESELECT CYCLE ENABLE

MR-2162



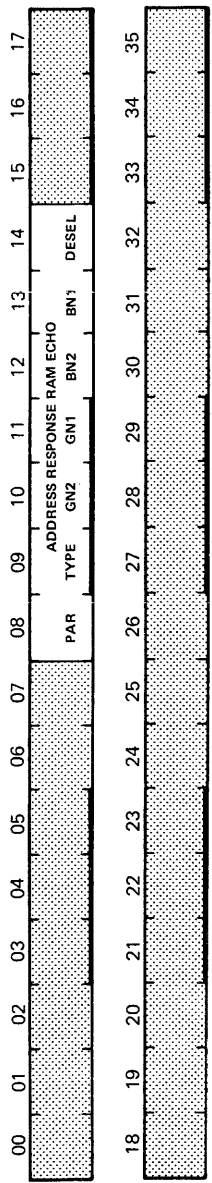
BLKO PI, (SBus Diagnostic Function Code 12)



NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY.

14 1 - BOX DESELECTED ON A 1

MR-2183



SBDIAG12  
(E+1)

NOTE: THIS BIT MAP APPLIES TO MF20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 12).

MR-2184

CONO PI,

PI (700600)	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
	WR ADR	EVEN DATA	PAR DIR	DROP INT		CLEAR SYS	REQ INT	PI CHAN ON OFF	PI SYSTEM OFF ON	REQUEST INTERRUPT		01	02	03	04	06	06	07

22 DROP INTERRUPT  
23 CLEAR PI SYSTEM

24 REQUEST INTERRUPT

MR-2154

DATAO PI,

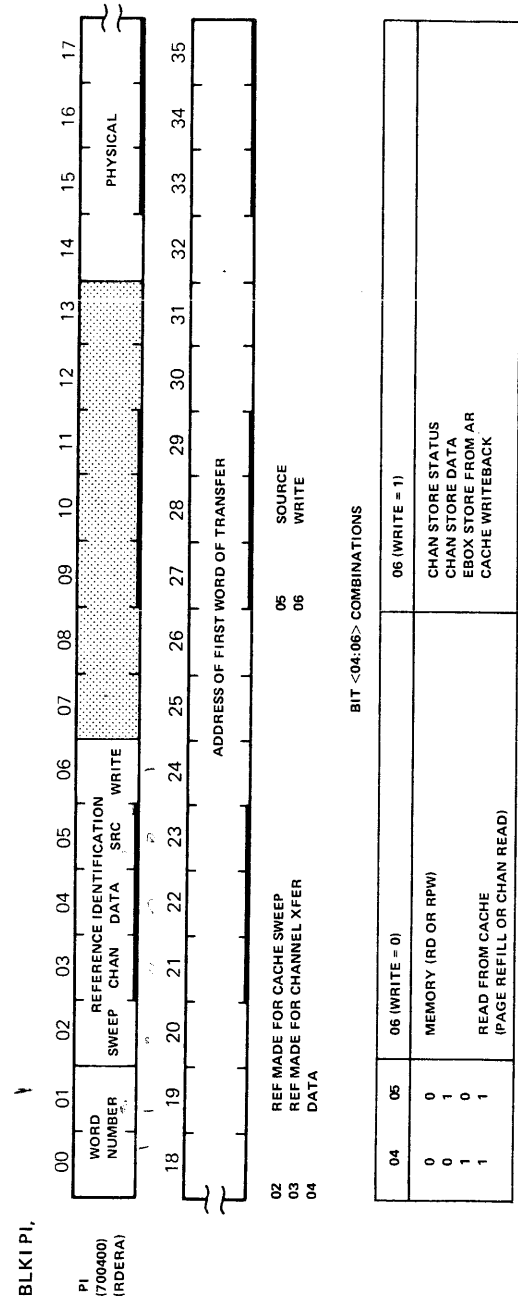
PI (700540)	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
	TRACK ENAB	TWO'S COMPLEMENT OF LENGTH OF BUFFER IN WORDS																

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35		
				14		15	16	17	PHYSICAL PAGE NUMBER OF BUFFER		18	19	20	21	22	23	24	25	26

NOTE: TRACKS ONLY

00 ENABLE MICROCODE TRACKING

MR-2156



MR-2162

BLKI TIM

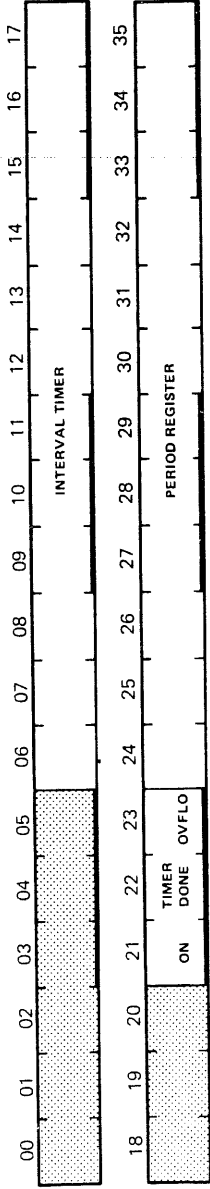
RDPERF  
(702000)



MR-2086

CONI TIM (TOPS-10 TAG: TIMSTS)

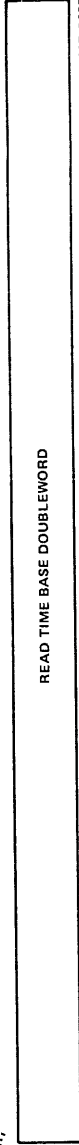
702240



MR-2084

DATAI TIM,

RDTIM  
(702040)



MR-2085

BLKO TIM,

WRPAE  
(702100)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
00	01	02	03	04	05	06	07	IGNOR	IGNOR	PROBE LOW	IGNOR	REF	CACHE FILL	PERFORMANCE WRITE	ENABLES SWEEP	IGNOR	
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
00	01	02	03	04	05	06	07	NO PI	PC MODE USER	IGNOR	EVENT MODE	CLEAR PA					

MR-2087

CONO TIM

702200

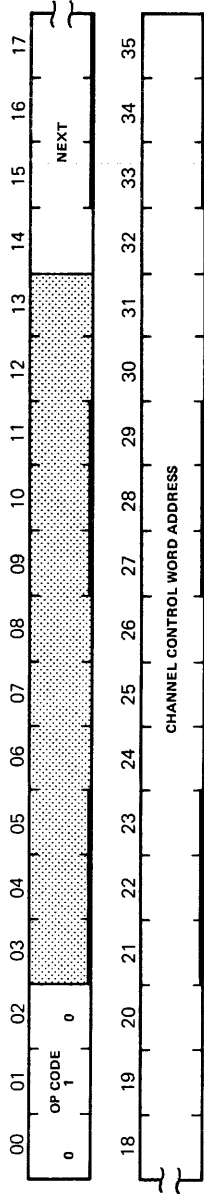
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
CLEAR TIMER			TIMER DONE	CLEAR DONE													
PERIOD REGISTER																	

MR-2083

CHANNEL COMMAND CODES

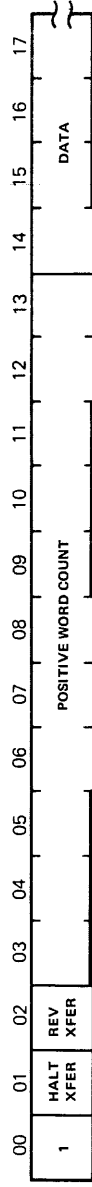
Code	Operation	Code	Operation
000	HALT	100	FORWARD DATA TRANSFER (DO NOT HALT)
001	NOT USED	101	REVERSE DATA TRANSFER (DO NOT HALT)
010	JUMP	110	FORWARD DATA TRANSFER (HALT)
011	NOT USED	111	REVERSE DATA TRANSFER (HALT)

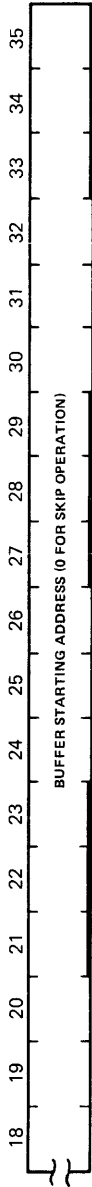
CCW JUMP



MR-2186

CCW DATA TRANSFER





NOTE: WORD COUNT FIELD = POSITIVE WORD COUNT STORED IN CHAN AND DECREMENTED, IF BIT 1 = 1 HALT WHEN WC = 0  
 ADDRESS = 22 BIT PHYSICAL ADDRESS:

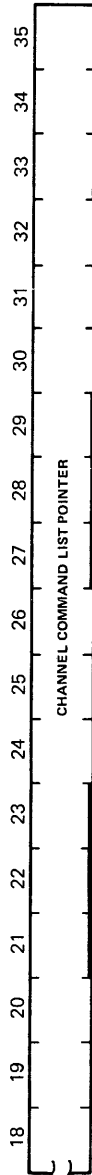
IF = 0: SKIP  
 IF DEVICE READ: DON'T MOVE DATA TO MEMORY  
 IF DEVICE WRITE: CHANNEL SUPPLIES FILL DATA FROM EXEC PROCESS TABLE LOCATIONS 60-63 TO WRITE REMAINDER OF DRIVES DATA BLOCK

01 HALT AFTER LAST TRANSFER

02 REVERSE DATA TRANSFER

MR-21B7

CCW HALT



MR-21B5



WORD 0 JUMP

JUMP TO CHANNEL COMMAND LIST

NOTE: EXECUTED AS A RESULT OF RH20 ASSERTING CBUS RESET.

MR-2188

WORD 1 STATUS

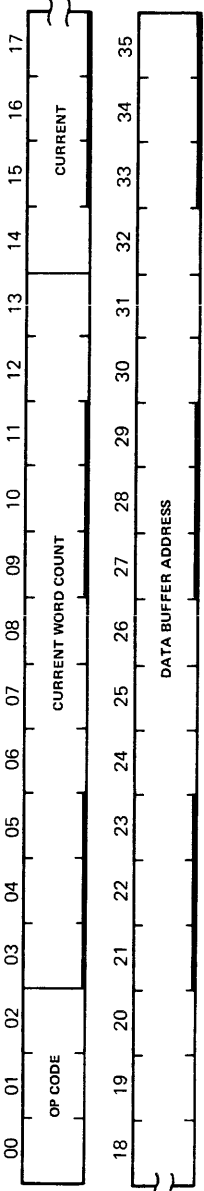
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
1	MEM PE	-ADR PE	-WC =0	NXM					LXE	RH20 ERROR	LONG WC	SHORT WC	OVER RUN	COMMAND			
18																	

LIST POINTER (ADDRESS OF CURRENT CCW + 1)

- 01 MEMORY PARITY ERROR
- 02 NOT ADDRESS PARITY ERROR
- 03 CHAN WORD COUNT DID NOT = 0 WHEN CHAN DID STORE TO EPT
- 04 CHAN REF NON EXIST MEM
- 09 ERROR DETECTED AFTER RH20 TERM XFER, CHAN ABORTS NEXT XFER
- 10 RH20 TRIED TO START CHAN WHEN CHAN WAS NOT READY
- 11 RH20 COMP XFER, BUT WORD COUNT IN CCW NOT REACHED
- 12 CHAN XFERRED DATA SPEC BY CCW, BUT RH20 STILL HAS DATA
- 13 IF DEV READ, RH20 SENT DATA BUT CHAN BUFF WERE FULL
- IF DEV WRITE, RH20 REQ DATA BUT CHAN BUFF WERE EMPTY

MR-2189

WORD 2 STATUS



<00:01> CURRENT FUNCTION CODE IN CCW  
 00 = HALT  
 01 = NOT IMPLEMENTED  
 02 = JUMP  
 03 = NOT IMPLEMENTED  
 04 = FWD DATA XFER  
 05 = REV DATA XFER  
 06 = FWD DATA XFER (HALT LAST XFER)  
 07 = REV DATA XFER (HALT LAST XFER)

<03:13> NORMALLY 0 AT END OF TRANSFER  
 <14:35> ADDRESS OF LAST DATA TRANSFERRED TO/FROM MEMORY

MR-2190

WORD 3 STATUS

NOTE: WORD 3 OF THE CHANNEL LOGOUT AREA IS NOT CURRENTLY USED BUT THE PROGRAM MAY USE IT AS THE VECTOR INTERRUPT ADDRESS FOR THE ASSOCIATED CHANNEL.

MR-2191

# FUNCT. CODES

## RH/DISK Function Codes

Nondata Transfer Codes		Data Transfer Codes	
Code	Fixed Head	Moving Head	Code
01	NO-OP	NO-OP	51*
03	UNLOAD	UNLOAD	53*
05	SEEK	SEEK	61
07	RECAL	RECAL	63
11	DRIVE CLEAR	DRIVE CLEAR	71
13	RELEASE	RELEASE	73
15	OFFSET	OFFSET	
17	RET TO C.L.	RET TO C.L.	
21	RD-IN PRESET	RD-IN PRESET	
23	PACK ACK	PACK ACK	
31	SEARCH	SEARCH	

\*Implemented in RH11 controllers only.

## RH/TAPE Function Codes

Nondata Transfer Codes		Data Transfer Codes	
Code	Magnetic Tape	Code	Magnetic Tape
01	NO-OP	51*	WR CHECK FORWARD
03	REWIND - OFF LINE	57*	WR CHECK REVERSE
07	REWIND	61	WR FORWARD
11	DRIVE CLEAR	71	RD FORWARD
21	RD-IN PRESET	77	RD REVERSE
25	ERASE		
27	WR FILE MARK		
31	SPACE FORWARD		
33	BACKSPACE		

\*Implemented in RH11 controllers only.



CON1 RHn

(7XX240)

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17
AR FULL	CB FULL	CC INH	CHAN INH ACT	CHAN PLS ACT	CHAN PLS	DF22	ILL FUNCT	ILL FUNCT	SELDR ADRE	SELDR ADRE	SELDR ADRE	SELDR ADRE	SELDR ADRE	SELDR ADRE	SELDR ADRE	SELDR ADRE	SELDR ADRE
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
DBUS PE	DREXC ERROR	CHAN ERROR	CW WRITE	OVER RUN	DR RE ERROR	ILL CMD	POWER FAIL	POWER FAIL	POWER FAIL	CBUS OVRUN	CBUS OVRUN	RAE	ATTN	BUSY	DONE	P/A	P/A

- 00 ASSEMBLY REGISTER FULL
- 01 CHANNEL BUFFER FULL
- 03 CHANNEL CONTROL INHIBIT
- 04 CHANNEL CONTROL CHANNEL ACTIVE
- 05 CHANNEL CONTROL CHANNEL PULSE
- 06 CHANNEL IS IN 22 BIT ADDRESS MODE
- 09 ILLEGAL FUNCTION CODE
- 10 SELECTED DRIVE REGISTER ADDRESS ERROR
- 15 CHANNEL DATA PARITY ERROR
- 16 CONTROL WORD PARITY ERROR
- 17 NONEXISTENT MEMORY
  
- 18 DATA BUS PARITY ERROR
- 19 EXCEPTION ERROR
- 20 CHANNEL ERROR
- 21 CONTROL WORD WRITTEN
- 22 DATA CHANNEL OVERRUN
- 23 DRIVE RESPONSE ERROR
- 24 ILLEGAL COMMAND
- 28 CONTROL BUS OVERRUN
- 29 REGISTER ACCESS ERROR
- 30 ATTENTION

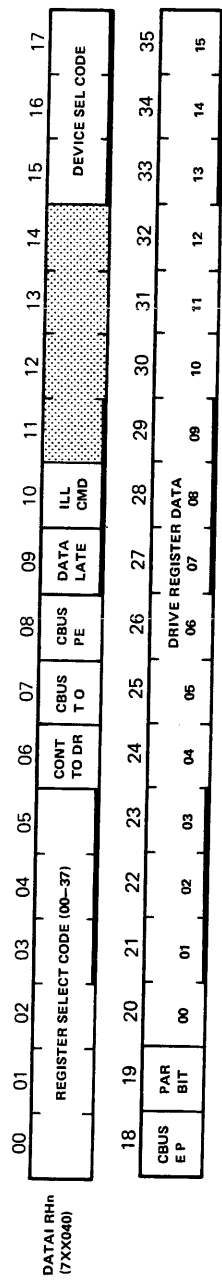
MR-2198

RH10 Register Addresses

Reg Adr	R/W	Name
40	R W	CR - Control Register
44	R W	IA - Interrupt Address
50	R W	DB - Data Buffer
54	R W	AE = Access Error

Reg Adr	R/W	Name
---------	-----	------

DIB - Drive Interface Buffer

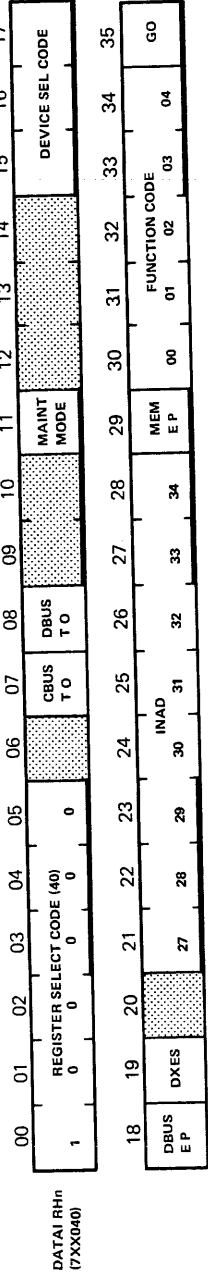


NOTE: REFER TO DATA0 DIB FOR A DEFINITION OF BITS <00:05>, <06, <15:17> AND 18.

07 CONTROL BUS TIME OUT  
08 CONTROL BUS PARITY ERROR

10 ILLEGAL COMMAND

CR — Control Register



NOTE: REFER TO DATA0 CR FOR A DEFINITION OF BITS <08:05>, 15, 18, 19, AND 29.

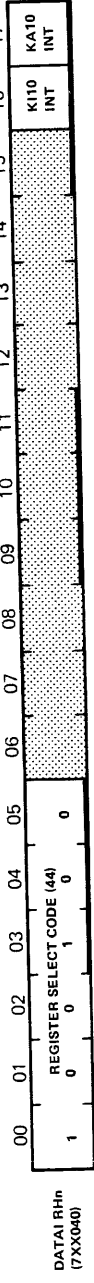
Refer to the function code tables which precede the RH10 I/O bit maps.

07 CONTROL BUS TIME OUT

08 DATA BUS TIME OUT

MR-2202

IA — Interrupt Address





NOTE: REFER TO DATA CR FOR A DEFINITION OF BITS <00:05>.

16 K110 INTERRUPT BIT

17 KA10 INTERRUPT BIT

MR-2204

DB - Data Buffer



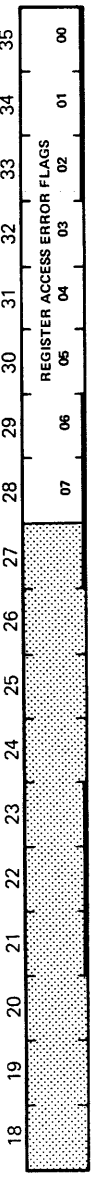
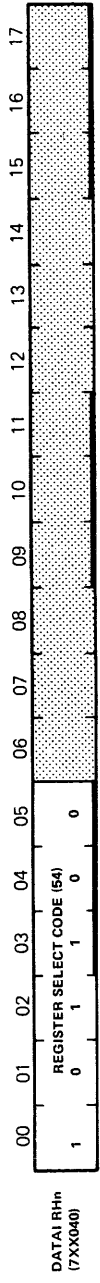
NOTE: REFER TO DATA CR FOR A DEFINITION OF BITS <00:05>.

14 DATA BUS ODD PARITY

MR-2206



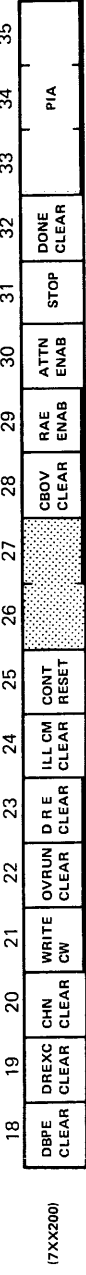
AE - Access Error



NOTE: REFER TO DATA0 CR FOR A DEFINITION OF BITS <00:06>.

MR-2208

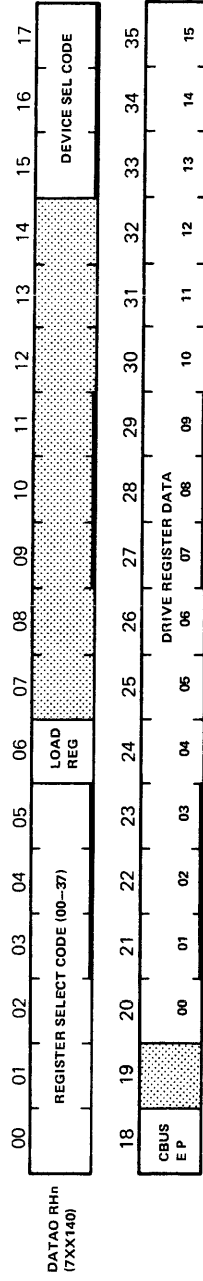
CONO RHn



- 18 DATA BUS PARITY ERROR CLEAR
- 19 CLEAR DRIVE EXCEPTION ERROR
- 20 CHANNEL ERROR CLEAR
- 21 WRITE CONTROL WORD
- 22 OVERRUN CLEAR
- 23 DRIVE RESPONSE ERROR CLEAR
- 24 ILLEGAL COMMAND CLEAR
- 25 CONTROLLER RESET
- 28 CONTROL BUS OVERRUN CLEAR
- 29 REGISTER ACCESS ERROR ENABLE
- 30 ATTENTION ENABLE

MR-2197

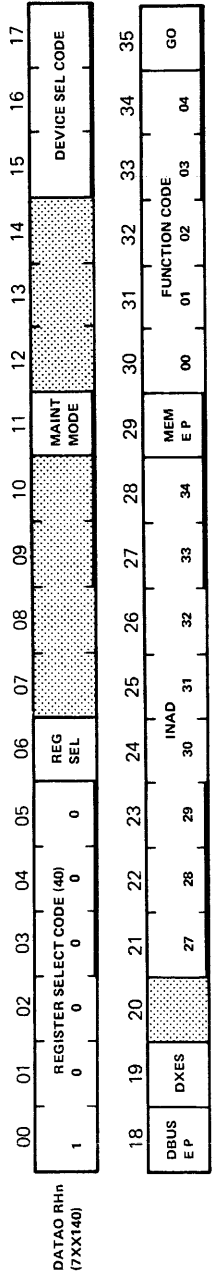
DIB — Drive Interface Buffer



<00:05> SELECTS ONE OF 32 DRIVE REGISTERS FOR INPUT OR OUTPUT  
 06 IF = 0 DATA (FROM THE DRIVE REGISTER AND DRIVE REGISTER ON BIT 6  
 SPECIFIED BY BITS <00:05> AND <15:17>) WILL BE TRANSFERRED TO THE RH. IF = 1 DATA WILL BE TRANSFERRED TO THE DRIVE AND REGISTER SPECIFIED

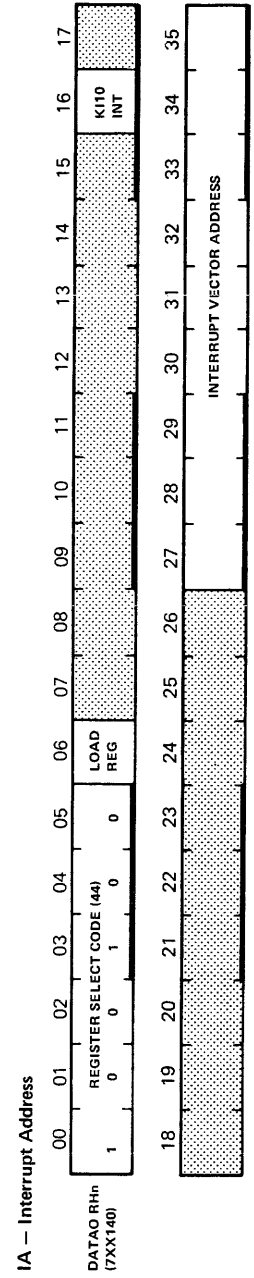
<15:17> DEVICE SELECT CODE SPECIFIES WHICH DEVICE (0-7) IS TO BE USED IN THE OPERATION  
 18 CONTROL BUS EVEN PARITY

CR - Control Register



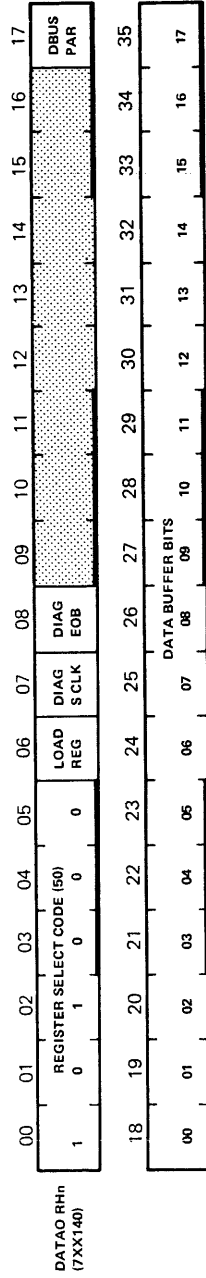
NOTE: Refer to the function code tables which precede the RH10 I/O bit maps.

- <00:05> REGISTER SELECT CODE - SPECIFIES WHICH REGISTER IS TO BE LOADED IF BIT 06 IS SET. THIS APPLIES TO REGISTER ADDRESS 40-77 ONLY. REFER TO DIB REGISTER FOR ADDRESS 00-37
- 06 LOAD REGISTER - IF = 0 LOAD CONTROL REGISTER. IF = 1 LOAD THE REGISTER SPECIFIED BY BIT <00:05>
- <15:17> DEVICE SELECT CODE - SPECIFIES WHICH DEVICE (0-7) IS TO BE USED IN THE OPERATION
- 18 DATA BUS EVEN PARITY
- 19 DISABLE TRANSFER ERROR STOP
- 29 WRITE EVEN MEMORY PARITY



MR-2203

DB - Data Buffer



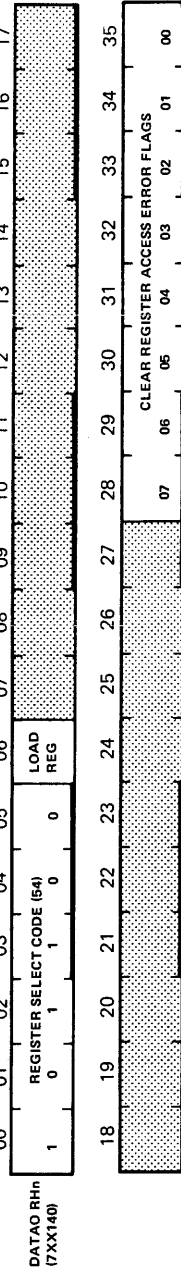
NOTE: REFER TO DATA0 CR FOR A DEFINITION OF BITS <00:05> AND 06.

07 DIAGNOSTIC SYNC CLOCK  
08 DIAGNOSTIC END OF BLOCK

17 DATA BUS PARITY

MR-2205

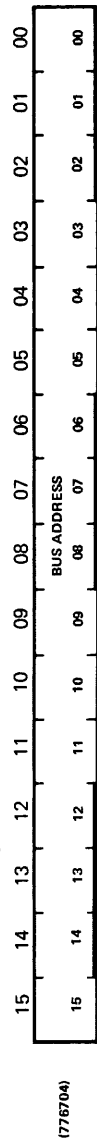
AE - Access Error



NOTE: REFER TO DATA0 CR FOR A DEFINITION OF BITS <00:06> AND 06.

MR-2207

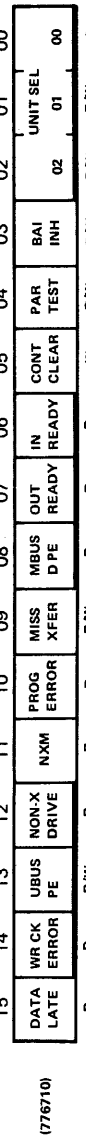
RH11 - RPBA - Bus Address Register



NOTE: ALL BITS READ/WRITE

MR-2215

RH11 - RPCS2 - Control and Status Register 2



15 DATA LATE  
 14 WRITE CHECK  
 13 UNIBUS PARITY ERROR  
 12 NON-EXISTENT DRIVE  
 11 NON-EXISTENT MEMORY  
 10 PROGRAM ERROR - RH BUSY  
 09 MISSED TRANSFER

08 MASSBUS DATA PARITY ERROR  
 07 OUTPUT READY  
 06 INPUT READY  
 05 CONTROLLER CLEAR  
 04 PARITY TEST  
 03 BUS ADDRESS INCREMENT INHIBIT  
 <02:00> UNIT SELECT

MR-2216

RH11 — RPDB — Data Buffer Register

(776722)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

DATA BUFFER

NOTE: ALL BITS READ/WRITE

MR-2217

RH11 — RPWC — Word Count Register

(776702)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

WORD COUNT REGISTER

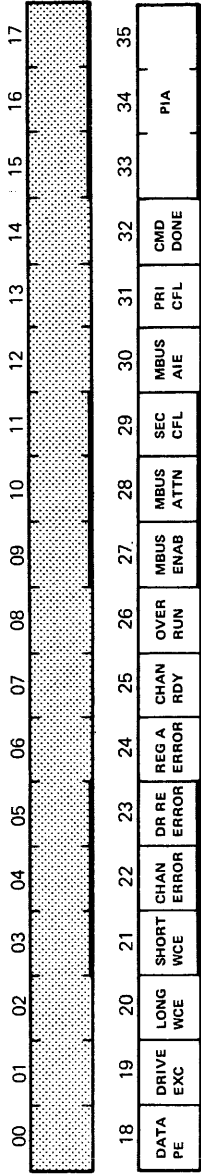
NOTE: ALL BITS READ/WRITE

MR-2218



CONI RHh

(7XX 240)

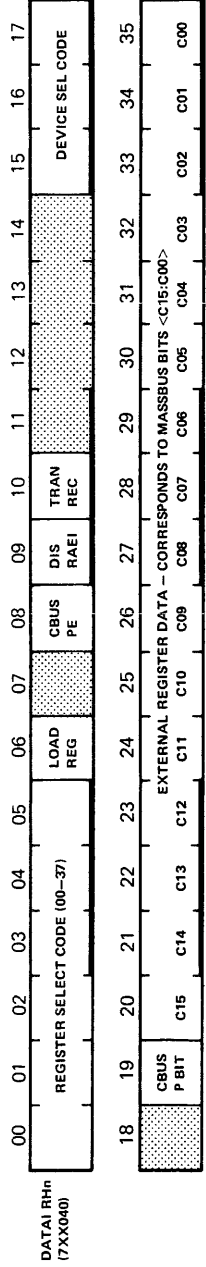


NOTE: BITS 24, 28 AND 32 WILL CAUSE AN INTERRUPT.

- 18 DATA BUS PARITY ERROR
- 19 DRIVE EXCEPTION ERROR
- 20 LONG WORD COUNT ERROR
- 21 SHORT WORD COUNT ERROR
- 22 CHANNEL ERROR
- 23 DRIVE RESPONSE ERROR
- 24 REGISTER ACCESS ERROR (CBTO OR CBPE)
- 25 CHANNEL READY TO BEGIN TRANSFER
- 26 DATA OVERRUN ERROR
- 27 MASSBUS ENABLE
- 28 MASSBUS ATTENTION
- 29 SECONDARY COMMAND FILE LOADED
- 30 MASSBUS ATTENTION INTERRUPT ENABLED
- 31 PRIMARY COMMAND FILE LOADED
- 32 COMMAND DONE
- <33:36> PRIORITY INTERRUPT CHANNEL

Reg Adr	R/W	Name
--	R W	PREP - Preparation Register (not addressed directly)
7 0	R W	SBAR - Secondary Block Address Register
7 1	R W	STCR - Secondary Transfer Control Register
7 2	R -	PBAR - Primary Block Address Register
7 3	R -	PTCR - Primary Transfer Control Register
7 4	R W	IVIR - Interrupt Vector Index Register
7 5	R -	RR - Read Register (Diagnostic Use)
7 6	W	WR - Write Register (Diagnostic Use)
7 7	W	DCR - Diagnostic Control Register (Diagnostic Use)

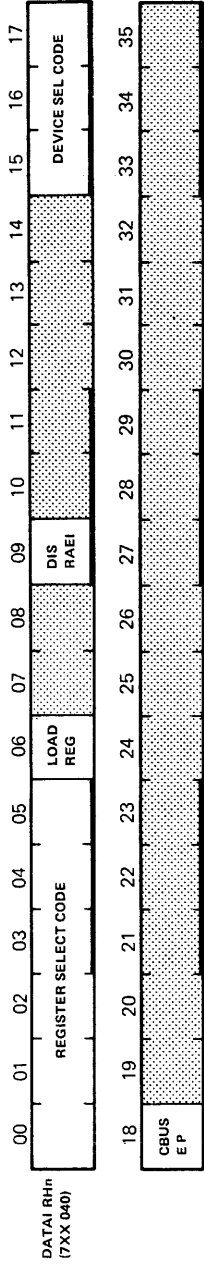
EXT -- External Registers (00--37)



NOTE: REFER TO PREP REG FOR DEFINITION OF BITS <00:06>, 8, AND <15:17>.

- 08 CONTROL BUS PARITY ERROR 10 TRANSFER RECEIVED (DEVICE RESPONDED)
- 09 DISABLE REG ACCESS ERROR, INTERRUPTS AND SUBSEQUENT REG WRITES 19 CONTROL BUS PARITY BIT

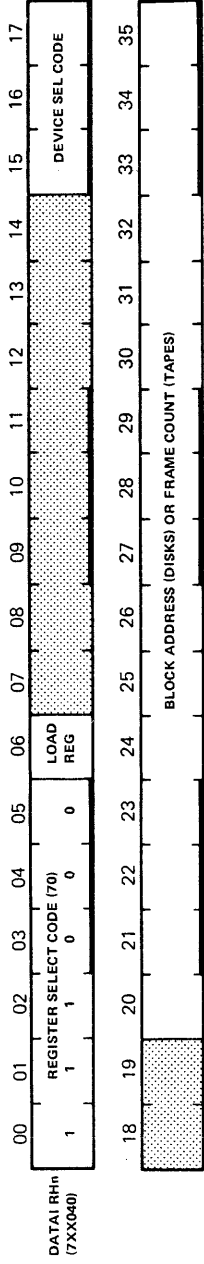
PREP — Preparation Register (Not Addressed Directly)



NOTE: REFER TO DATA0 PREP REG FOR DEFINITIONS OF BITS.

MR-2048

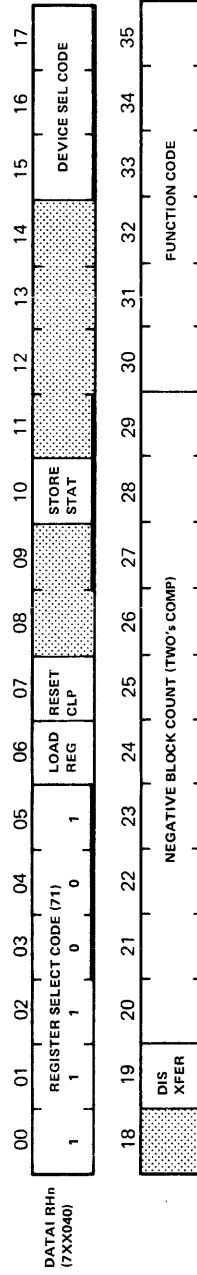
SBAR — Secondary Block Address Register (70)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF <00:05>, 06 AND <16:17>.

MR-2062

STCR - Secondary Transfer Control Register (71)

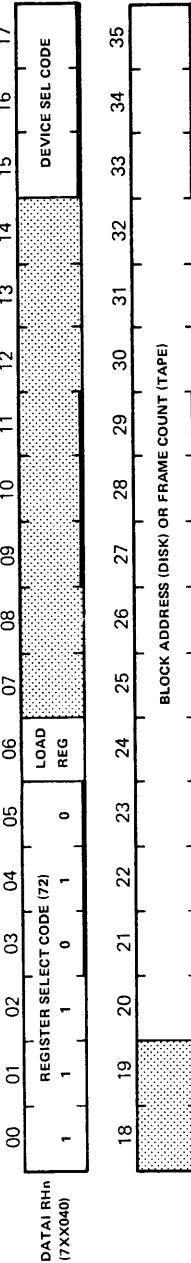


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.  
Refer to the function code tables which precede the RH10 I/O bit maps.

- 07 RESET COMMAND LIST POINTER
- 10 STORE CHANNEL STATUS CONTROL BIT
- 19 DISABLE TRANSFER ERROR STOP BIT

MR-2054

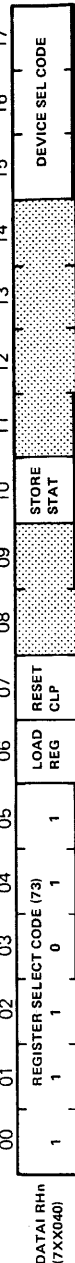
PBAR — Primary Block Address Register (72)

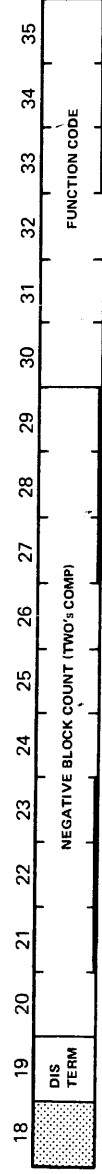


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:06>, 06, AND <15:17>.  
REFER TO SBAR REG FOR DEFINITIONS OF BITS <20:35>.

MR-2055

PTCR — Primary Transfer Control Register (73)

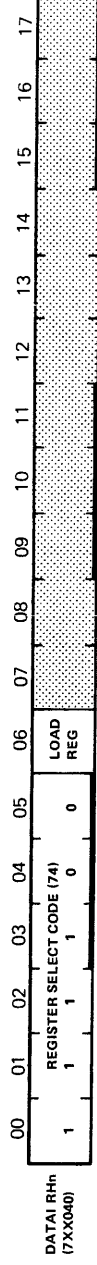




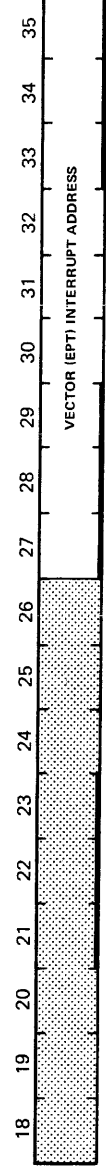
NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.  
 Refer to the function code tables which precede the RH10 I/O bit maps.  
 REFER TO STCR REG FOR DEFINITION OF BITS 07, 10, AND 19.

MR-2056

IVIR - Interrupt Vector Index Register (74)



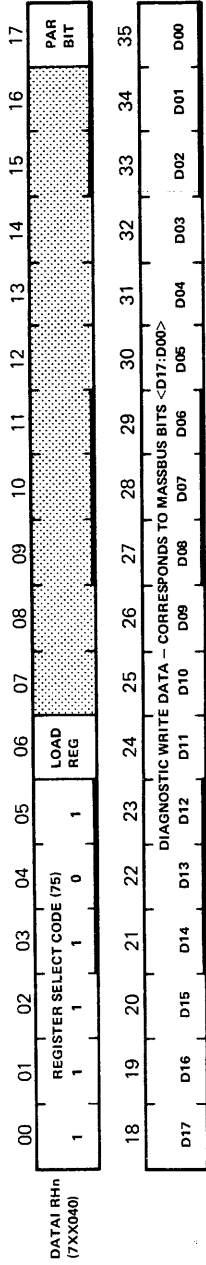
DATA1 RHn  
 (7XX040)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

MR-2058

RR -- Read Register (75) Diagnostic Use

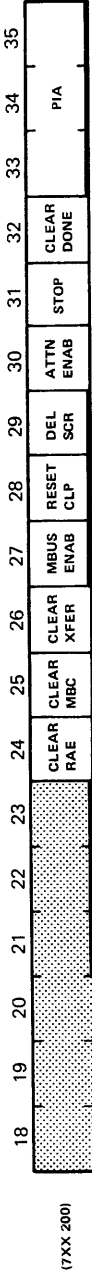


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:06> AND 06.

17 PARITY BIT  
 <18:35> WRITE DATA AND PARITY (17) LOOPED BACK VIA MASSBUS  
 XCVRS DURING DIAG WRITE

MR-2069

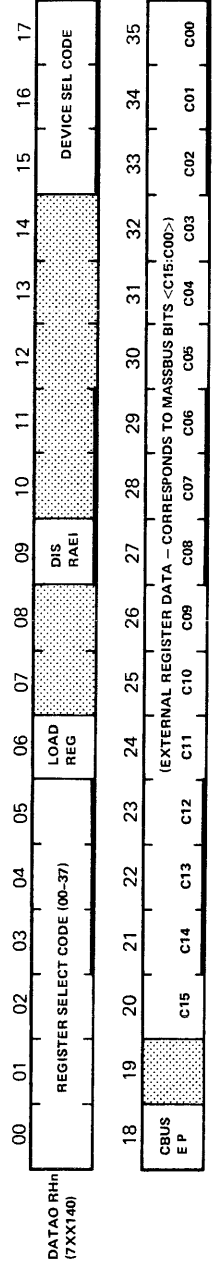
CONO RHn



- 24 CLEAR REGISTER ACCESS ERROR
- 25 CLEAR MASSBUS CONTROLLER
- 26 CLEAR TRANSFER ERRORS
- 27 MASSBUS ENABLE
- 28 RESET COMMAND LIST POINTER
  
- 29 DELETE SECONDARY CONTROL REGISTER
- 30 ATTENTION INTERRUPT ENABLE
- 31 STOP TRANSFER (STATUS BITS NOT CLEARED)
- <39:35> PRIORITY INTERRUPT CHANNEL

MR-2045

EXT — External Registers (00—37)



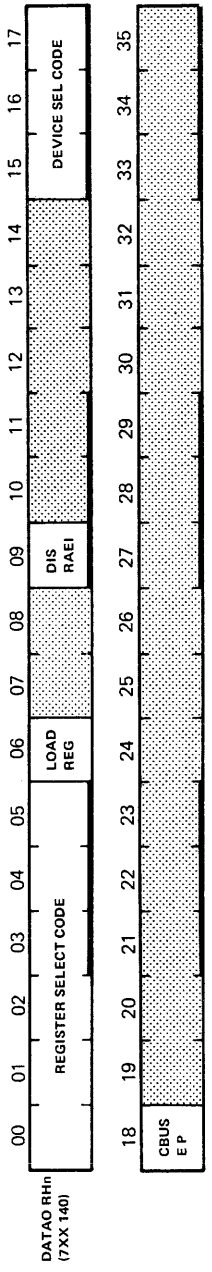
NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:18>.

09 DISABLE REG ACCESS ERROR, INTERRUPTS AND SUBSEQUENT REG WRITES.

MR-2049



PREP - Preparation Register (Not Addressed Directly)

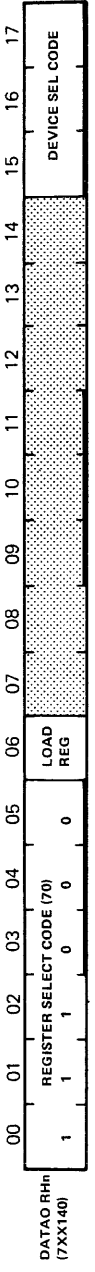


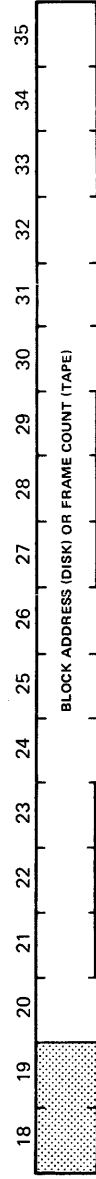
NOTE: BITS <00:06>, 06 AND <15:17> HAVE A COMMON DEFINITION FOR MANY RH REGISTERS, TO ELIMINATE REDUNDENCY THEY ARE DESCRIBED ONCE HERE.

- <00:06> REGISTER SELECT CODE. SPECIFIES WHICH REGISTER IS TO BE LOADED IF BIT 06 IS SET.
- 06 LOAD REGISTER. IF 0 LOAD PREP REG. IF 1 LOAD REG SPECIFIED BY BITS <00:06>
- 09 DISABLE REG ACCESS ERROR INTERRUPTS AND SUBSEQUENT REG WRITES
- <15:17> DEVICE SELECT CODE. SPECIFIES WHICH DEVICE (0-7) IS TO BE USED IN THE OPERATION. CONTROL BUS EVEN PARITY

MR-2047

SBAR - Secondary Block Address Register (70)



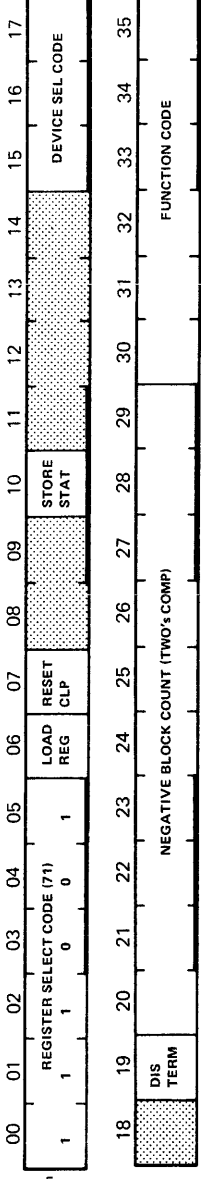


BLOCK ADDRESS (DISK) OR FRAME COUNT (TAPE)

NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, <15:17>.  
 <20:35> TAPE - FRAME COUNT 20 = MSD 35 = LSD  
 <23:27> DISK - TRACK ADDRESS  
 <31:35> DISK - SECTOR ADDRESS

MR-2051

STCR - Secondary Transfer Control Register (71)



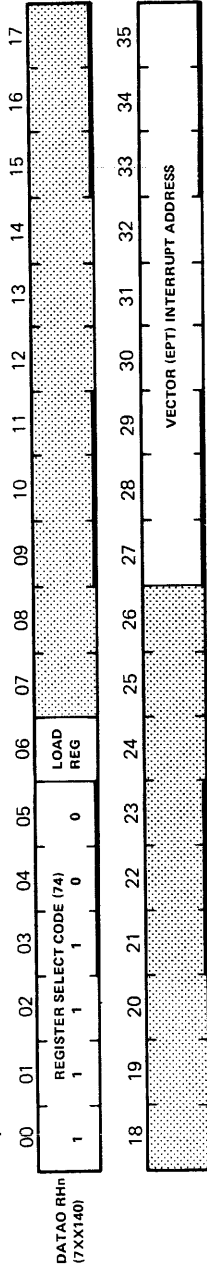
DATA0 RH<sub>n</sub>  
(7XX140)

NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.  
 Refer to the function code tables which precede the RH10 I/O bit maps.

- 07 RESET COMMAND LIST POINTER
- 10 STORE CHANNEL STATUS CONTROL BIT
- 19 DISABLE TERMINATION OF TRANSFERS DUE TO DATA BUS PARITY ERRORS OR DRIVE EXCEPTION ERRORS.

MR-2053

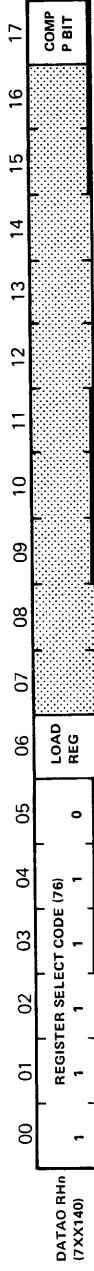
IVIR – Interrupt Vector Index Register (74)

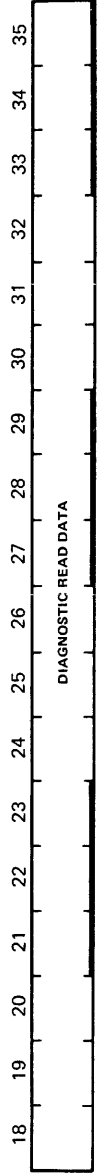


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:06> AND 06.

MR-2057

WR – Write Register (76) Diagnostic Use





NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

17 COMPUTED PARITY BIT (BY PROG) FOR DIAG READ DATA

MR-2060

DCR — Diagnostic Control Register (77) Diagnostic Use

DATA0 RH <sup>h</sup> (7XX140)	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	
	REGISTER SELECT CODE (77)							LOAD REG											
	1	1	1	1	1	1	1												
	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	
								XFER SIG	DATA LOOP	TEST SBAR	EVEN PCK	READ WRITE	SIM D EXC	SIM EOB	SIM ATTN	SIM S CLK			

NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

- 26 TRANSFER SIGNAL (SIMULATED)
- 27 DATA LOOPBACK (VIA MASSBUS XCVRS)
- 28 TEST SBAR
- 29 EVEN PARITY CHECK
- 30 READ/WRITE-SET ON DIAG READ (LOOPS RD DATA VIA MASSBUS XCVRS)
- 31 SIMULATES DRIVE EXCEPTION
- 32 DATA LOOPBACK (VIA MASSBUS XCVRS)
- 33 SIMULATES END OF BLOCK
- 34 TEST SBAR
- 35 EVEN PARITY CHECK
- 36 READ/WRITE-SET ON DIAG READ (LOOPS RD DATA VIA MASSBUS XCVRS)

MR-2061

RH11 – RPCS1 – Control and Status Register 1  
RH20 – DRCR – Control Register

(776700) (MB-00)	15	R	XFER COND ERROR	14	R	MBUS C PE	13	R	DRIVE AVAIL	12	R	DRIVE AVAIL	11	R	PORT SEL	10	R/W	ADDRESS 17 16	09	R/W	READY	08	R	INIT ENAB	07	R/W	06	R/W	05	R/W	04	R/W	03	R/W	02	R/W	01	R/W	00	R/W	GO
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NOTE: SHARED REGISTER BITS <15:13> AND <10:06> ARE IN RH.  
REFER TO DCL PRINT RG3 AND RG6.

Refer to the function code tables which precede the RH10 I/O bit maps.

- 15 SPECIAL CONDITION
- 14 TRANSFER ERROR
- 13 MASSBUS CONTROL PARITY ERROR
- 11 DRIVE AVAILABLE

- 10 PORT SELECT
- <09:06> UNIBUS ADDRESS EXTENSION BITS 17 AND 16
- 06 INTERRUPT ENABLE

RH11 – RPDS – Drive Status  
RH20 – DRSR – Status Register

MR-2219

(776712) (MB-01)	15	R	ATTN ACT	14	R	ERROR	13	R	PIP	12	R	MOL	11	R	WRITE LOCK	10	R/W	LAST SECT	09	R/W	PROG ABLE	08	R/W	DRIVE PRES	07	R	DRIVE READY	06	R/W	VALID VOL	05	R/W	D=1	04	R/W	D>64	03	R/W	GOREV	02	R/W	DIGB	01	R/W	DF20	00	R/W	DF06
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NOTE: ALL BITS READ ONLY.  
REFER TO DCL PRINT RG6.

- 15 DATA CHECK
- 14 UN SAFE
- 13 OPER INC
- 12 DIR T ERROR
- 11 WR LK ERROR
- 10 I ADR ERROR
- 09 A OV ERROR
- 08 H CRC ERROR
- 07 H COM ERROR
- 06 ECC ERROR
- 05 WR CK FAIL
- 04 FMT ERROR
- 03 PAR ERROR
- 02 RMR
- 01 ILL REG
- 00 ILL FUNC

- 15 ATTENTION ACTIVE
- 13 POSITIONING IN PROGRESS
- 12 MEDIUM ON LINE
- 10 LAST SECTOR TRANSFERRED
- 09 PROGRAMMABLE
- 08 DRIVE PRESENT
- 06 VALID VOLUME

- 06 RP04 - DIFFERENCE EQUALS ONE
- 04 RP04 - DIFFERENCE LESS THAN 64
- 03 RP04 - GO REVERSE
- 02 RP04 - DRIVE TO INNER GUARD BAND
- 01 RP04 - DRIVE FORWARD 20 INCH/SEC
- 00 RP04 - DRIVE FORWARD 5 INCH/SEC
- <06:00> RP06 UNUSED

MR-2220

RH11 - RPER1 - Error Register 1  
 RH20 - DRER1 - Error Register 1

(776714)  
 (MB-02)

15	DATA CHECK	14	UN SAFE	13	OPER INC	12	DIR T ERROR	11	WR LK ERROR	10	I ADR ERROR	09	A OV ERROR	08	H CRC ERROR	07	H COM ERROR	06	ECC ERROR	05	WR CK FAIL	04	FMT ERROR	03	PAR ERROR	02	RMR	01	ILL REG	00	ILL FUNC
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NOTE: ALL BITS READ/WRITE.  
 REFER TO DCL PRINT RGO.

- 13 OPERATION INCOMPLETE
- 12 DRIVE TIMING ERROR
- 11 WRITE LOCK ERROR
- 10 INVALID ADDRESS ERROR
- 09 ADDRESS OVERFLOW ERROR
- 08 HEADER CRC ERROR
- 07 HEADER COMPARE ERROR

- 06 ECC HARD ERROR
- 05 WRITE CLOCK FAIL
- 04 FORMAT ERROR
- 03 PARITY ERROR
- 02 REGISTER MODIFICATION REFUSED
- 01 ILLEGAL REGISTER
- 00 ILLEGAL FUNCTION

MR-2221

RH11 – RPMR – Maintenance Register  
RH20 – DRMR – Maintenance Register

(776724)  
(MB-03)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
					HI CT DET	S BYTE DET	ZERO DET	DATA ENV	ECC ENV	MANT WRITE	MANT READ	MANT S CLK	MANT INDEX	MANT CLOCK	DIAG MODE

NOTE: ALL BITS READ/WRITE.  
REFER TO DCL PRINT EC1 AND RG3.

- 10 HIGH COUNT DETECT
- 09 SYNC BYTE DETECTED
- 08 ZERO DETECT
- 07 DATA ENVELOPE

- 06 ECC ENVELOPE
- 03 MAINTENANCE SECTOR CLOCK
- 00 DIAGNOSTIC MODE

MR-2222

RH11 – RPAS – Attention Summary  
RH20 – DRAS – Attention Summary

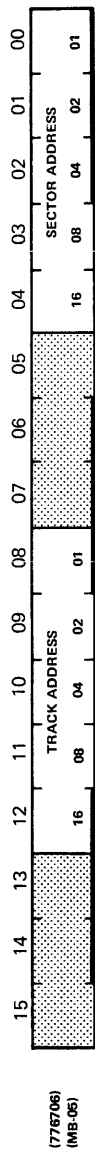
(776716)  
(MB-04)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
								DRIVE ATTENTION SUMMARY							

NOTE: ALL BITS READ/WRITE.  
REFER TO DCL PRINT DP.

MR-2223

RH11 - RPDA - Desired Track/Sector Address  
 RH20 - DRDA - Desired Track/Sector Address

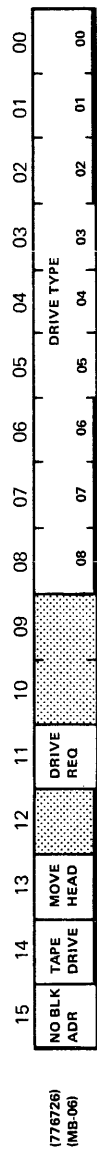


(776706)  
 (MB-06)

NOTE: ALL BITS READ/WRITE.  
 REFER TO DCL PRINT SS3 AND SS6.

MR-2224

RH11 - RPDT - Drive Type  
 RH20 - DRTR - Type Register



(776726)  
 (MB-06)

NOTE: ALL BITS READ ONLY.  
 REFER TO DCL PRINT ECR.

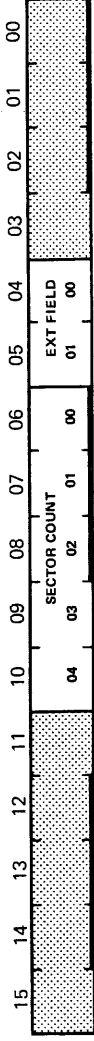
15 NOT BLOCK ADDRESSED  
 14 TAPE DRIVE

13 MOVING HEAD  
 11 DRIVE REQUEST REQUIRED

MR-2225



RH11 - RPLA - Look Ahead  
RH20 - DRLP



NOTE: ALL BITS READ ONLY.  
REFER TO DCL PRINT DP6.

<06:04> EXTENSION FIELD

06 04 HEAD LOCATION

0 0 = <20% (IN FIRST 20% OF SECTOR)

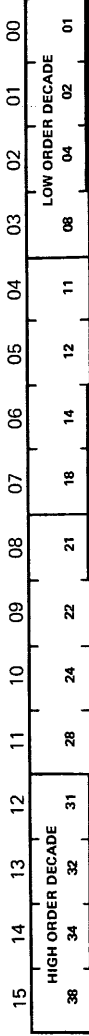
0 1 = 20 - 40%

1 0 = 40 - 80%

1 1 = >80% (IN LAST 20% OF SECTOR)

MR-2226

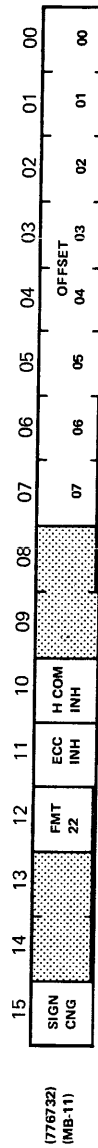
RH11 - RPSN - Serial Number  
RH20 - DRSN - Serial Number



NOTE: ALL BITS READ ONLY.  
REFER TO DCL PRINT EC8.

MR-2227

RH11 - DPOF - Offset  
 RH20 - DROF - Offset



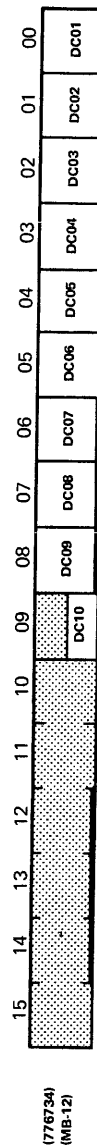
NOTE: ALL BITS READ/WRITE.  
 REFER TO DCL PRINT RG1.

15 SIGN CHANGE  
 12 FORMAT 22 SECTORS

11 ECC INHIBIT  
 10 HEADER COMPARE INHIBIT

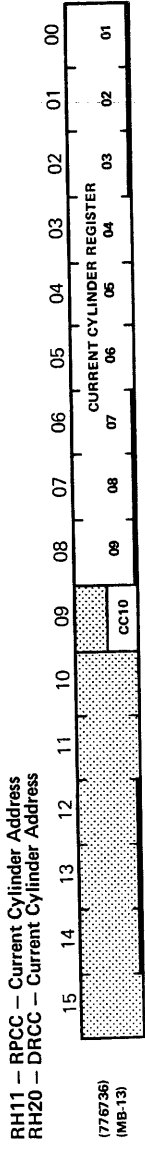
MR-2228

RH11 - RPDC - Desired Cylinder  
 RH20 - DRDC - Desired Cylinder



NOTE: ALL BITS READ WRITE.  
 REFER TO DCL PRINT SS1.

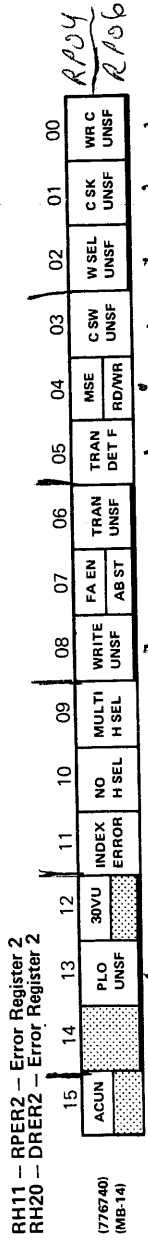
MR-2229



NOTE: ALL BITS READ ONLY.  
 REFER TO DCL PRINT SST.

09 RP04 - UNUSED  
 RP06 - CURRENT CYLINDER BIT 10

MFR-2230



NOTE: ALL BITS READ/WRITE  
 REFER TO DCL PRINT EC6.

- 15 RP04 - AC UNSAFE
- 13 RP06 - UNUSED
- 12 PHASE LOCKED OSCILLATOR UNSAFE
- 11 RP04 - 30 VOLTS UNSAFE
- 10 RP06 - UNUSED
- 09 INDEX ERROR
- 08 NO HEAD SELECT
- 07 MULTIPLE HEAD SELECT
- 06 WRITE READY UNSAFE
- 05 RP04 - FAILSAFE ENABLED
- 04 RP06 - ABNORMAL STOP
- 03 TRANSITION UNSAFE
- 02 TRANSITION DETECTOR FAILURE
- 01 RP04 - MOTOR SEQUENCE ERROR
- 00 RP06 - READ AND WRITE
- 00 CURRENT SWITCH UNSAFE
- 01 WRITE SELECT UNSAFE
- 00 CURRENT SINK FAILURE
- 00 WRITE CURRENT UNSAFE

MR-2231

RH11 - RPER3 - Error Register 3  
RH20 - DRER3 - Error Register 3

(778742)  
(MB-15)

15	OFF CYL	14	SEEK INC	13	OPER	12		11		10		09		08		07	AC LOW	06	DC LOW	05	35 VF	04	UNSF	03	UNSF	02		01	VE US	PS UN	00	DC UN
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NOTE: ALL BITS READ/WRITE REFER TO DCL PRINT EC7.

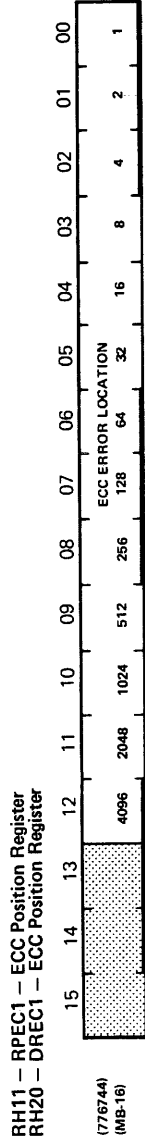
- 15 OFF CYLINDER
- 14 SEEK INCOMPLETE
- 13 RP04 - UNUSED
- 06 RP06 - OPERATOR PLUG ERROR
- 05 AC VOLTAGE UNSAFE
- 04 DC VOLTAGE UNSAFE
- 00 RP04 - UNUSED
- 00 RP06 - 35 VOLTS UNSAFE

- 03 RP04 - ANY UNSAFE EXCEPT READ/WRITE
- 00 RP06 - UNUSED
- 01 RP04 - VELOCITY UNSAFE
- 00 RP06 - WRITE AND OFFSET
- 00 RP04 - PACK SPEED UNSAFE
- 00 RP06 - DC VOLTAGE UNSAFE

MR-2232

*RP04*  
*RP06*

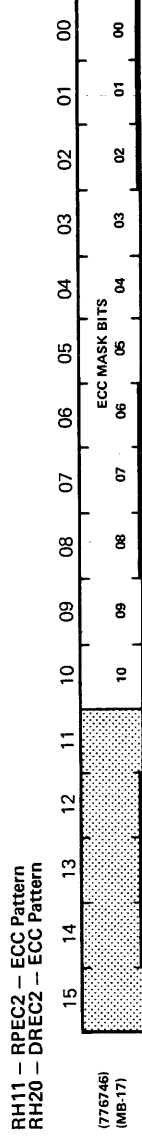
*DCL*



NOTE: ALL BITS READ ONLY.  
 REFER TO DCL PRINT EC1.

<12:00> BURST LOCATION CODE FOR ECC

MR-2233



NOTE: ALL BITS READ ONLY.  
 REFER TO DCL PRINT EC1.

<10:00> ERROR BURST AT COMPLETION OF ECC

MR-2234



CS1 - Control Register 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(MB-00)				DRIVE AVAIL						05	FUNCTION CODE			01	GO
										R/W	R/W	R/W	R/W	R/W	R/W

NOTE: Refer to the function code tables which precede the RH10 I/O bit maps.

11 DRIVE AVAILABLE (HARDWIRED)

MR-2072

DS - Status Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(MB-01)	ATTN ACT	ERROR	PIP	MOL	WRITE LOCK	EOT		DRIVE PRES	DRIVE RDY	SLAVE STAT	PE STAT	SET DOWN	IDB DECT	TAPE MARK	SLAVE ATTN

NOTE: ALL BITS READ ONLY.

- 15 ATTENTION ACTIVE
- 14 COMPOSITE ERROR
- 13 POSITIONING IN PROGRESS
- 12 MEDIUM ON LINE
- 10 END OF TAPE
- 08 DRIVE PRESENT
- 07 DRIVE READY
- 06 SLAVE STATUS CHANGE
- 06 PHASE ENCODED STATUS
- 04 SETTLE DOWN
- 03 IDENTIFICATION BURST DETECTED
- 02 TAPE MARK DETECTED
- 01 BEGINNING OF TAPE
- 00 SLAVE ATTENTION

MR-2073

ER -- Error Register

15	CORR CRC	14	UN SAFE	13	OPER INC	12	DR T ERROR	11	NXF	10	CS TTM	09	F C ERR	08	N STD GAP	07	PFE LRC	06	NDE VPE	05	DBUS PE	04	FMT ERROR	03	CBUS PE	02	REG MOD	01	ILL REG	00	ILL FUNC
----	-------------	----	------------	----	-------------	----	---------------	----	-----	----	-----------	----	------------	----	--------------	----	------------	----	------------	----	------------	----	--------------	----	------------	----	------------	----	------------	----	-------------

(MB-02)

NOTE: ALL BITS READ ONLY  
SPLIT BITS PE NRZI

- 15 PE -- CORRECTABLE DATA ERROR NRZI -- CRC DOES NOT MATCH COMPUTED CRC
- 14 UNSAFE
- 13 OPERATION INCOMPLETE
- 12 DRIVE TIMING ERROR
- 11 NONEXECUTABLE FUNCTION
- 10 PE CORRECTABLE SKEW
- 09 NRZI -- ILLEGAL TAPE MARK
- 08 FRAME COUNT ERROR
- 07 PE -- FORMAT ERROR
- 06 NRZI -- CHECK CHAR ERROR
- 05 PE -- NONCORRECTABLE DATA ERROR
- 04 NRZI -- VERTICAL PARITY ERROR
- 03 DATA BUS PARITY ERROR
- 02 FORMAT ERROR
- 01 CONTROL BUS PARITY REGISTER MODIFICATION REFUSED
- 00 ILLEGAL REGISTER ILLEGAL FUNCTION

MR-2074



MR - Maintenance Register

(MB-03)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
08	07	06	05	04	03	02	01	00	SEL S CLK	MANT CLK	03	02	01	00	MANT MODE

NOTE: ALL BITS READ/WRITE

<15:7> MAINT DATA FIELD: BUFFER DATA ON WRAP OP, LRC AT  
 END OF MRZ1 TRANSFERS  
 06 SELECTED SLAVE CLOCK: WRT CLOCK SIG GEN BY SEL  
 SLAVE

05 MAINTENANCE CLOCK  
 MAINT OPERATION CODE  
 00

MR-2075

AS - Attention Summary

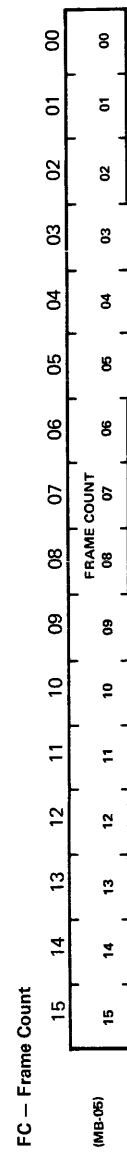
(MB-04)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
								07	06	05	04	03	02	01	00

NOTE: ALL BITS READ/WRITE

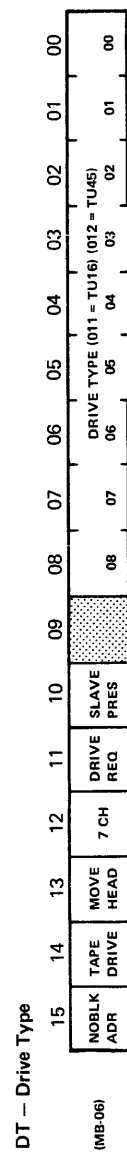
ATTENTION SUMMARY

MR-2076



NOTE: ALL BITS: READ/WRITE

MR-2082



NOTE: ALL BITS READ ONLY  
BITS <08:00> HARDWIRED

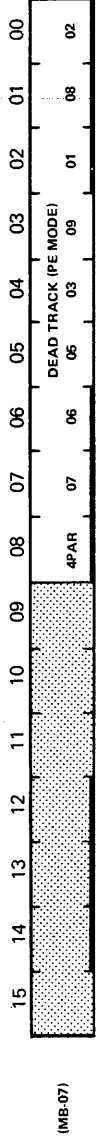
15 NOT BLOCK ADDRESSED  
14 TAPE DRIVE  
13 MOVING HEAD UNIT  
12 7 CHANNEL UNIT-NEGATED ON 9 CH DRIVE OR POWER LOSS  
11 DRIVE REQUEST REQUIRED  
10 SLAVE PRESENT

<08:00>

DRIVE TYPE  
X5X = TM03  
X1X = TM02  
XX1 = 45 IPS SLAVE  
XX2 = 75 IPS  
XX4 = 125 IPS

MR-2077

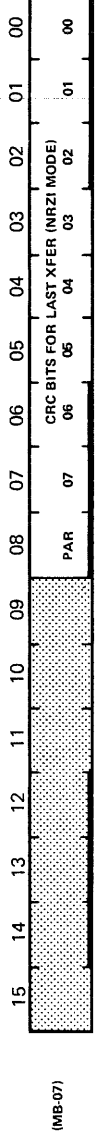
CK — Check Character



MR-2078

NOTE: ALL BITS READ ONLY  
USE THIS BIT MAP FOR PHASE ENCODED DRIVES

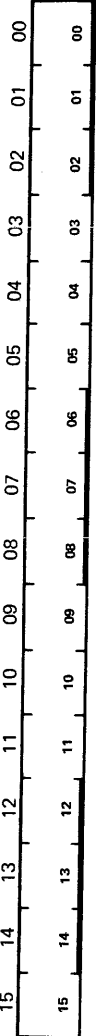
CK — Check Character



MR-2079

NOTE: ALL BITS READ ONLY  
USE THIS BIT MAP FOR NRZI DRIVES

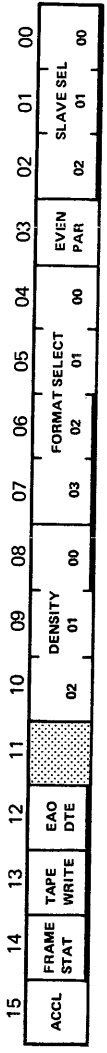
SN - Serial Number



NOTE: ALL BITS READ ONLY

MR-2080

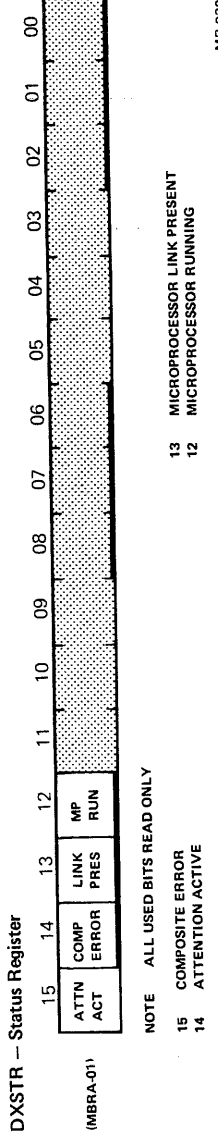
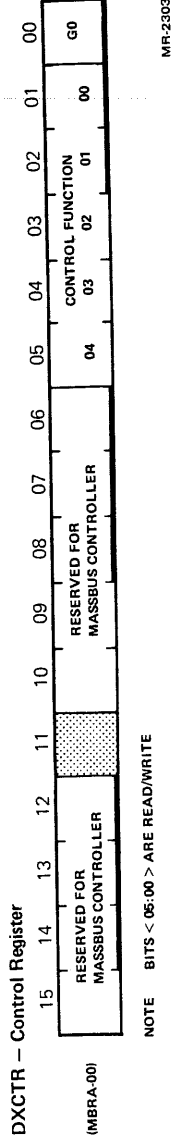
TC - Tape Control



NOTE: ALL BITS READ/WRITE

- 15 ACCELERATION
- 14 FRAME COUNT STATUS
- 13 TAPE CONTROL WRITE
- 12 ENABLE ABORT ON DATA TRANS ERROR
- 3 EVEN PARITY
- <02:00> SLAVE SELECT BITS

MR-2081



DXERR - Error Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
07	06	05	04	03	02	01	00	MP ERROR	MP STOP	UBUS PE	DBUF PE	CBUS PE	REG MOD	ILL REG	ILL FUNCT

NOTE ALL BITS READ/WRITE EXCEPT <15:08> WHICH ARE READ ONLY

- 07 MICROPROCESSOR ERROR
- 06 MICROPROCESSOR STOPPED
- 05 MICRO BUS PARITY ERROR
- 04 DATA BUFFER PARITY ERROR
- 03 CONTROL BUS PARITY ERROR
- 02 REGISTER MODIFICATION REFUSED
- 01 ILLEGAL REGISTER
- 00 ILLEGAL FUNCTIONS

MR-2305

DXMTR - Maintenance Register

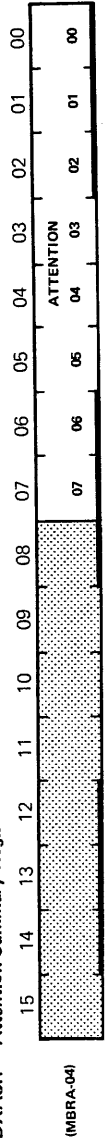
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(MBRA-03)											SING CYC	WRITE EP	MP START	DX20 RESET	

NOTE ALL USED BITS ARE READ/WRITE

- 04 SINGLE CYCLE
- 03 WRITE EVEN PARITY
- 02 MICROPROCESSOR START

MR-2306

DXASR – Attention Summary Register

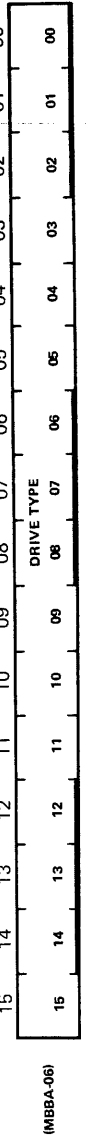


(MBRA-04)

NOTE: ALL USED BITS ARE READ/WRITE

MR-2307

DXDTR – Drive Type Register

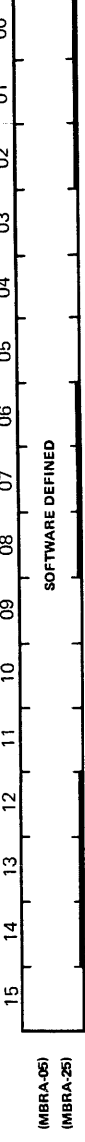


(MBBA-06)

NOTE: ALL BITS READ ONLY

MR-2317

DXGP5 – General Purpose Register



(MBRA-05)  
(MBRA-25)

MR-2308

NOTES



BYTE I T	0 (B)	1 (4)	2 (2)	3 (1)	4 (8)	5 (4)	6 (2)	7 (1)	BYTE I T	
0	COMMAND REJECT	INTERVENTION REQUIRED	BUS OUT CHECK	EQUIPMENT CHECK	DATA CHECK	OVERRUN	WORD COUNT ZERO	DATA CONVERT CHECK	0	
1	NOISE	TU STATUS A	TU STATUS B	7-TRK	LOAD POINT	SELECTED & WR STAT	FILE PROTECTED	NOT CAPABLE	1	
2		TRACK		IN		ERROR			2	
3	R/W VRC	MTE/LRC	SKEW ERROR	END DATA CK /CRC	ENV CK/ SKEW VRC	1600 BPI SET IN TU	BACKWARD	C/P COMP.	3	
4		REJECT TU	T1	WRITE TRG VRC	LWR	TU CHECK	RPQ	RPQ	4	
5		NEW SUBSYSTEM	WTM CHECK	ID BURST CK	* START READ CHECK	* PARTIAL RECORD	* POSTAMBLE** ERROR	RPQ	5	
6	7-TRK TU	** WRITE CURRENT FAIL	DUAL DENSITY TU	NOT 1600	TAPE UNIT MODEL IDENTIFICATION					6
7	COLUMN *** TOP OR BTM	LEFT. COL. FAIL ***	RIGHT COL. FAIL ***	RESET KEY	DSE FAILURE	ERASE HD *** FAILURE	LOAD FAILURE	LOAD FAILURE	7	
8	IBG DETECTED **								8	
9	6250 *** CORRECTION	VELOCITY CHANGE	CHANNEL ** BUFFER CK	CRC III	6250	**	TCU RESERVED	TCU RESERVED	9	
10	CMND STAT REJECT **			RECORD NOT DETECTED		TACH START FAIL **	VELOCITY ** CHECK	VELOCITY ** CHECK	10	
11									11	

MR-2309

12													12
13	CU FEATURES				CONTROL UNIT UNIQUE IDENTIFICATION (HI-ORDER PART S/N)	2048	1024	512	256				13
14	128	64	32	CONTROL UNIT UNIQUE IDENTIFICATION (LO-ORDER PART S/N)	4096	8	4	2	1				14
15			8192	TAPE UNIT UNIQUE IDENTIFICATION (HI-ORDER PART S/N)	4096	2048	1024	512	256				15
16	128	64	32	TAPE UNIT UNIQUE IDENTIFICATION (LO-ORDER PART S/N)	16	8	4	2	1				16
17	2 CH SW FEATURE	SWITCH FEATURES								REFLECTS TCU DIAGNOSTIC RELEASE LEVEL			17
18		SAME	TU	I.D.	TU			E.C. LEVEL					18
19	TU 7	TU 6	TU 5	BUSY STATUS, LO-ORDER TAPE UNITS	TU 4	TU 3	TU 2	TU 1	TU 0				19
20	TU F	TU E	TU D	BUSY STATUS, HI-ORDER TAPE UNITS	TU C	TU B	TU A	TU 9	TU 8				20
21													21
22				"REFER TO MICROPROGRAM PAGE QAO25"			**						22
23	MOD IV TCU	**		"REFER TO MICROPROGRAM PAGE AO025"			**						23
BYTE I T	0 (8)	1 (4)	2 (2)	3 (1)	4 (8)	5 (4)	6 (2)	7 (1)					BYTE I T

\* TX01 ONLY \*\* TX02 ONLY \*\*\* TU72 ONLY

**NOTES**

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1 - DMA / DIA Backplane  
2 - DTE / RH20  
4 - CPU Backplane

CHECKS/ADJ

-2-

RH20 MASS FAIL ADJ

- 1 Attach channel 1 probe to appropriate pin for RH20 being adjusted.

RH20 #	PIN #
0	2F34T2
1	2F31T2
2	2F28T2
3	2F25T2
4	2F22T2
5	2F19T2
6	2F16T2
7	2F13T2

- 2 Adjust MASS FAIL potentiometer on appropriate M8555 one turn beyond the point at which it goes low.

WHEN TO DESKEW

LOGIC ASSY.	MODULE REPLACED	DESKEW
CPU Bay	M8526 - CLK CPU Clock Module	DMA20, All MA20s, All MB20s, All RH20s
	M8519 - MEM (Slot 07) SBus Translator	DMA20, All MA20s, All MB20s
	M8516 - TRN (Slot 06) E & C Bus Translator	All RH20s
MA20	M8562 - MA20 Timing Module	MA20
	M8561 - MA20 Control Module	MA20
	SBus Cable	MA20
DMA20	M8563 - DMC Adapter Interface DMA20 Board Two	DMA20
	M8560 - DTR DMA Timing and S Bus Transceivers	DMA20
	SBus Cable	MB20
MB20	M8565 MB20 Timing Module	MB20
	M8568 MB20 Control Module	MB20
	SBus Cable	MB20
I/O BAY	M8559 - CDS I/O Bay Clock Distribution Module	All RH20s
	M8556-DP RH20 Data Path	RH20

## RH20 DESKEW PROCEDURE

**EQUIPMENT REQUIRED**  
Tektronics 475 or equivalent (100 MHz) scope with identical probes and short ground clips.

**OBJECTIVE**  
ALL RH20s are deskewed to the MBox clock that produces channel time zero, CHT0.

**NOTES**  
Recheck skew whenever the CBus cable or the M8556 module is replaced.

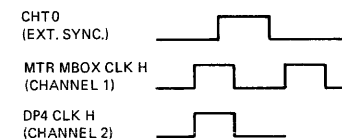
The adjustments are made on the M8559 module. The top potentiometer is for RH20 #0, the second potentiometer is for RH20 #1, etc.

**ADJUSTMENT PROCEDURE**  
Attach a probe (either ext, sync or channel 3) to CHT0 H, 4B09K1.

Sync positive external.

Attach channel 1 probe to MTR MBOX CLK H, 4D33P1.

Push TRIGGER VIEW and verify that the MBOX CLK that occurs just prior to CHT0 can be seen on the scope. See diagram below.



MR-2256

Attach channel 2 probe to appropriate clock pin for RH20 being deskewed. See chart below.

RH20	PIN
0	2A36D2
1	2A33D2
2	2A30D2
3	2A27D2
4	2A24D2
5	2A21D2
6	2A18D2
7	2A15D2

Align clock pulse on channel 2 with the MBox clock that occurs approximately 10 nanoseconds before CHT0. Do this for all RH20s that are installed.

# CHECKS/ADJ.

-4-

## MA20/MB20 DESKEW PROCEDURE

### EQUIPMENT REQUIRED

Tektronics 475 or equivalent (100 MHz) scope with identical probes and short ground clips.

### OBJECTIVE

To assure proper clock alignment between KL10 and MA20/MB20 controller.

### NOTES

Select CR0 on the KL10. Type a MR and then a FX1 to turn on the clock.

The M8562 delay lines are arranged so that A clock is the top potentiometer and B clock is the bottom potentiometer.

### ADJUSTMENT PROCEDURE

Attach a probe (either external sync or channel 3) to A CHANGE COMING L, 4E22F2. Set scope for external trigger and negative edge.

Attach channel 1 probe to MTR MBOX CLK C, 4D33P1. Use 0.5 V/CM and set scope such that the ground reference is 1.3 V above the centerline.

Press TRIGGER VIEW and observe that the relationship of MTR MBOX CLK C to A CHANGE COMING L corresponds to diagram below.

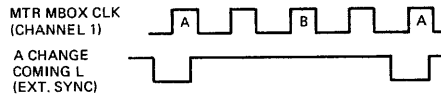


DIAGRAM OF CLOCK "A" AND "B" PHASES

MR-2285

Set the leading edge of the first A phase clock on the first division on the scope screen.

Attach channel 2 probe to pin 5D26A1 in memory to be aligned.

Adjust the top potentiometer on the M8562 or M8565 in slot 1 of the memory so that the leading edge 50% point crosses the leading edge 50% point of MBox A phase clock.

Connect channel 2 probe to pin 5D26K1 in the memory to be aligned.

Adjust the bottom potentiometer on the M8562 or M8565 in slot 1 of the memory so that the leading edge 50% point crosses the leading edge 50% point of MBox B phase clock.

Connect channel 2 probe to pin 5D29A1 in the memory to be aligned.

Perform the A phase alignment described above. Adjust the top potentiometer of the M8562 or M8565 in slot 54.

Connect channel 2 probe to pin 5D29K1 in the memory to be aligned.

Perform the B phase alignment described above. Adjust the bottom potentiometer of the M8562 or M8565 in slot 54. This completes the adjustments for one MA20 or MB20 unit.

For additional memory boxes the procedure is identical.

DMA20 CLOCK DESKEW PROCEDURE

EQUIPMENT REQUIRED  
Tektronics 475 or equivalent (100 MHz) scope with identical probes and short ground clips.

OBJECTIVE  
To assure performing clock deskew procedure type MR and then type FX1 to turn on the clock. Do not check deskew under a running program.

NOTES  
Before performing clock deskew procedure type MR and then type FX1 to turn on the clock. Do not check deskew under a running program

ADJUSTMENT PROCEDURE  
Attach a probe (either external sync or channel 3) to A CHANGE COMING L, 4E22F2. Set sync for negative edge.

Attach channel 1 probe to MTR MBOX CLOCK, 4D33P1. Use 0.5 V/CM and set scope such that the ground reference is 1.3 V above the centerline.

Attach channel 2 probe to DMC2 CLK DESKEW POINT, 1A02R2. Use 0.5 V/CM and adjust scope such that the ground reference is 1.5 V below the centerline.

The positive MBox clock pulse which occurs after A CHANGE COMING L goes low is the A phase clock. The second clock tick after the A phase clock tick is the B phase clock tick. The second clock tick after the B phase clock tick is another A phase clock tick, etc.

Adjust DL2 on the M8560 in slot 1AF03 (it is the 4th delay from the top) until the leading edge of the clock on channel 2 which is affected by this adjustment crosses the centerline at the same time as the leading edge of A phase MBox clock on channel 1.

Adjust DL3 on the M8560 in slot 1AF03 (it is the top delay) until the leading edge of the clock which is affected by this adjustment crosses the centerline at the same time as the leading edge of B phase MBox clock on channel 1.

Connect channel 2 to DTR3 CLK 125 NS A H, 1D03F1.

Adjust DL1 on the M8560 in slot 1AF03 (it is the bottom delay) until the leading edge of the clock on channel 2 which is affected by this adjustment crosses the centerline at the same time as the leading edge of A phase MBox clock on channel 1.

Connect channel 2 to DTR3 CLK 62 NS A H, 1D03L2.

Adjust DL4 on the M8560 in slot 1AF03 (it is the 2nd delay from the top) until the leading edge of the clock which is affected by this delay crosses the centerline at the same time as the leading edge of A phase MBox clock on channel 1.

Adjust DL5 on the M8560 in slot 1AF03 (it is the 3rd delay from the top) until the leading edge of the clock which is affected by this delay crosses the centerline at the same time as the leading edge of B phase MBox clock on channel 1.

This completes the adjustment of the DMA20 clock.

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M<sup>6</sup>G-SMH

## DMA20 DATA WARNING ADJ

## EQUIPMENT REQUIRED

Tektronics 475 or equivalent (100 MHz) scope with identical probes and short ground clips.

## OBJECTIVE

The KL10 use DATA WARN as well as READ RESTART for memory reads. This procedure assures correct alignment of these pulses.

## NOTES

This procedure should be done in 4-Bus Mode, assuming the system has multiples of 4 memories. This general procedure will, however, work in any bus mode.

The memory must be set up to return DATA WARNING SLOW and ADDRESS ACK (NT) only. No other combination is legal!

## ADJUSTMENT PROCEDURE

Set up the DMA20 in 4-Bus Mode doing a small loop which reads from only one memory on a given bus, such as:

```

10/ MOVE 0, 100 (200000 100)
11/ MOVE 0, 101 (200000 101)
12/ MOVE 0, 102 (200000 102)
13/ MOVE 0, 103 (200000 103)
14/ JRST 10 (254000 10)

```

Put channel 1 probe on KBus n DATA WARNING.

```

KBus 0 1C05D1
KBus 1 1C07D1
KBus 2 1C09D1
KBus 3 1C11D1

```

Put channel 2 probe on KBus n RD RS.

```

KBus 0 1C05J1
KBus 1 1C07J1
KBus 2 1C09J1
KBus 3 1C11J1

```

Sync on channel 1 going negative.

Adjust each memory such that DATA WARNING (on channel 1) occurs (MG10s 260 ±5) MH10s 295 ±5) nanoseconds prior to RD RS (on channel 2). This adjustment is done in the memory. Refer to the memory print set for delay locations for the specific type of memory being adjusted.

If more than four memory controllers are to be adjusted, deselect the memories just adjusted and select the next boxes as low core. Rerun the program and adjust the next memories.

Adjust the appropriate M8591 for the port - top delay potentiometer.

## MG10/MH10

Port	Loc
0	KL39
1	KL32
2	KL38
3	KL31
4	KL37
5	KL30
6	KL36
7	KL29

## PNEUMATIC ADJUSTMENTS

## THREAD MODE

## ALL MODELS

ITEM	V/P	TUBE COLOR	EASY LOAD
LOWER RESTRAINT	P	10 RED	10" - 12"
UPPER RESTRAINT	P	10 BLUE	16" - 20"
RT THD CHAN	P	10 YELLOW	30"
RT THD CHAN	V	10 PURPLE	5" - 6"
LT THD CHAN	P	6 YELLOW	30"
AIR JET	P	6 BLUE	15" - 17"
VACUUM REEL	V	6 RED	19" - 21"

## RUN MODE TU70

ITEM	V/P	TUBE COLOR	TU70
COLUMNS	V	6 PURPLE	34" - 35"
RT UPPER AIR BEARING	P	10 PINK	48" - 53"
RT GUIDE	P	10 GREEN	44" - 48"
LT GUIDE	P	10 BROWN	40" - 60"
RT LOWER AIR BEARING	P	10 CLEAR	48" - 53"
LT LOWER AIR BEARING	P	6 GREEN	40" - 42"
TAPE CLEANER BLOCK	V	10 BLACK	5" - 8" - ADJUST SO THAT TAPE SEALS TO CLEANER BLOCK WITH MINIMUM VACUUM.

## RUN MODE TU72

ITEM	V/P	TUBE COLOR	TU72
COLUMNS	V	6 PURPLE	33" - 35"
RT UPPER AIR BRNG	P	10 PINK	48" - 53"
RT LOWER AIR BRNG	P	10 CLEAR	48" - 53"
RT GUIDE	P	10 GREEN	60" - 70"
LT GUIDE	P	10 BROWN	0
LT LOWER AIR BRNG	P	6 GREEN	40" - 42"
CAPSTAN	V	6 PINK	15" - 19"
TAPE CLEANER BLOCK	V	10 BLACK	5" - 6" - ADJUST FOR TAPE SEAL AT MINIMUM VACUUM

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## Notes for KL10 CPU Power Layout

1. PTn - U represents upper power tabs on CPU backplane.
2. PTn - L represents lower power tabs on CPU backplane.
3. PT tabs 5-U, 5-L, 6-U and 6-L are connected to the H7420 No. 2 in the I/O cabinet for +5 volt power.
4. The following power tabs are jumpered together.  
PT9U to PT11U... PT9L to PT11L PT10U to PT12U PT10L to PT12L  
PT19U to PT21U PT19L to PT21L PT20U to PT22U PT20L to PT22L
5. STn represents sense tabs for remote sensing. Connections are from J2 and J3 of the H761 to the sense tabs, and from the sense tabs (via an etch) to the remote sensing pins on the backplane as indicated below.

## TWISTED PAIR FROM H761 (J2 AND J3) TO SENSE TABS

-5.2A -SENSE - J2-2 TO ST17  
+SENSE - J2-1 TO ST16  
-5.2B -SENSE - J2-4 TO ST19  
+SENSE - J2-3 TO ST18  
-5.2C -SENSE - J2-6 TO ST1  
+SENSE - J2-5 TO PT15-U  
-5.2D -SENSE - J2-8 TO ST2  
+SENSE - J2-7 TO PT17-U  
-5.2E -SENSE - J2-10 TO ST13  
+SENSE - J2-9 TO PT17-L  
-5.2F -SENSE - J2-12 TO ST7  
+SENSE - J2-11 TO ST6  
-5.2H -SENSE - J2-14 TO ST5  
+SENSE - J2-13 TO ST4  
-5.2J -SENSE - J3-2 TO ST3  
+SENSE - J3-1 TO ST4  
-5.2K -SENSE - J3-4 TO ST10  
+SENSE - J3-3 TO ST11  
-SENSE - J3-8 TO ST15  
-2A +SENSE - J3-7 TO ST16  
-SENSE - J3-10 TO ST14  
-2B +SENSE - J3-9 TO PT15-L  
-SENSE - J3-12 TO ST12  
-2C +SENSE - J3-11 TO ST11  
-SENSE - J3-14 TO ST8  
-2D +SENSE - J3-13 TO ST9

## ETCH FROM SENSE TABS TO REMOTE SENSE PIN

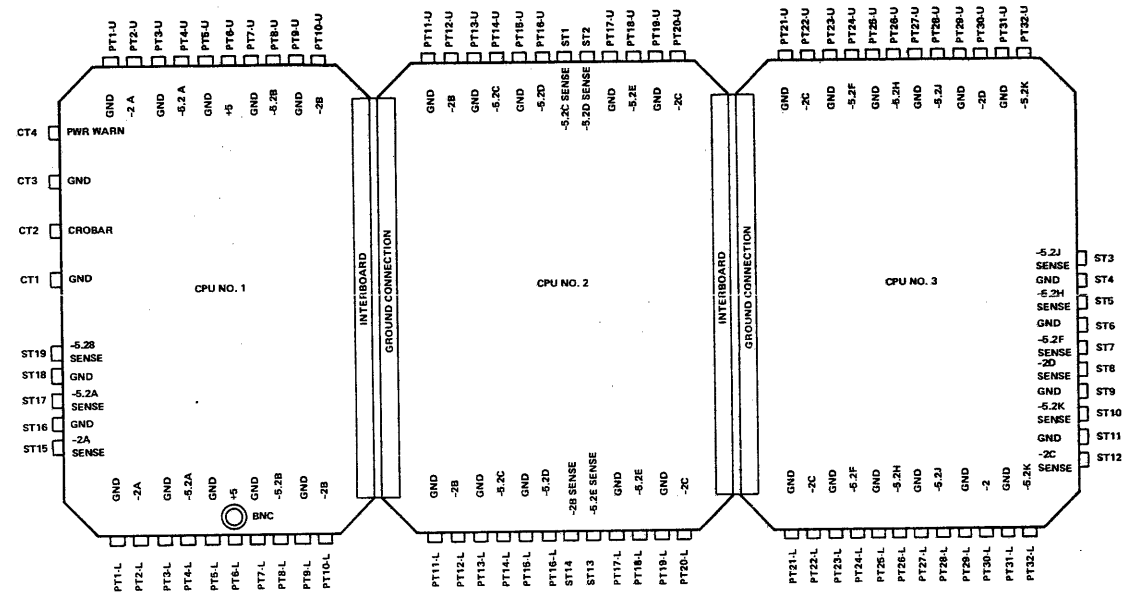
-5.2A ST17 TO F8B2  
-5.2B ST19 TO F14B2  
-5.2C ST1 TO A21U1  
-5.2D ST2 TO A27U1  
-5.2E ST13 TO F33B2  
-5.2F ST7 TO A48U1  
-5.2H ST5 TO A45U1  
-5.2J ST3 TO A49U1  
-5.2K ST10 TO F53B2  
-2A ST15 TO F9B1  
-2B ST14 TO F21B1  
-2C ST12 TO F38B1  
-2D ST8 TO F48B1

6. The sense lines use the following color code.

BLACK = GND RED = +5 GREEN = -2.0 BLUE = -5.2

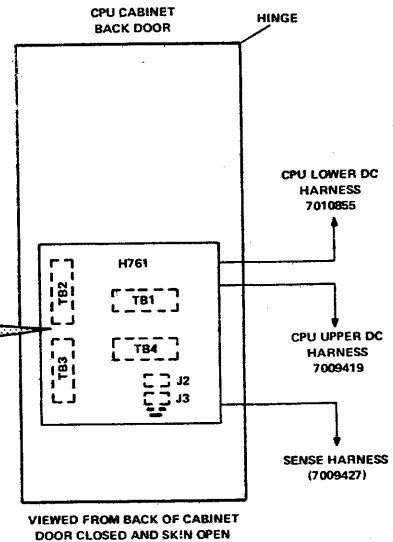
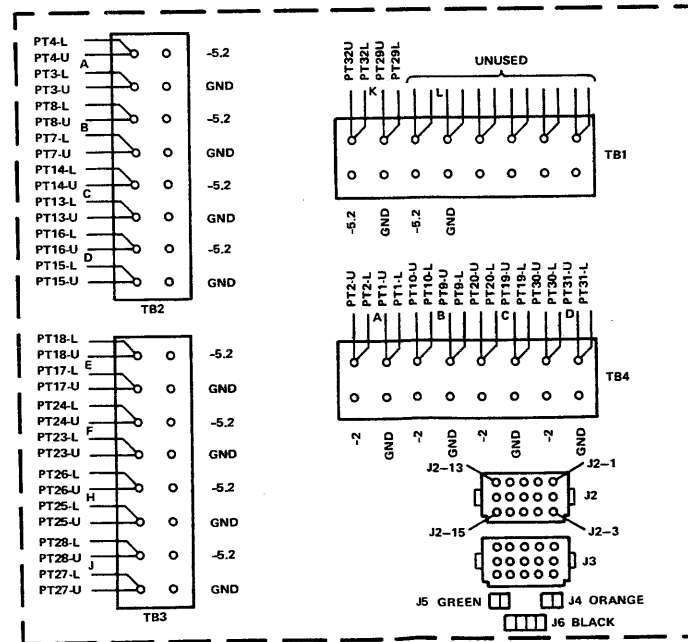
7. CTn represents control tabs. Connections are from the 863 power control to the control tabs, and from the control tabs (via an etch) to the following pins.

POWER WARN CT4 to A04J1  
CROWAR CT2 to A06J2, B06S1, C02S1, C03S1, and F01U2.



MR-2236

KL10 CPU DC POWER (BACKPLANE)



MR-2237

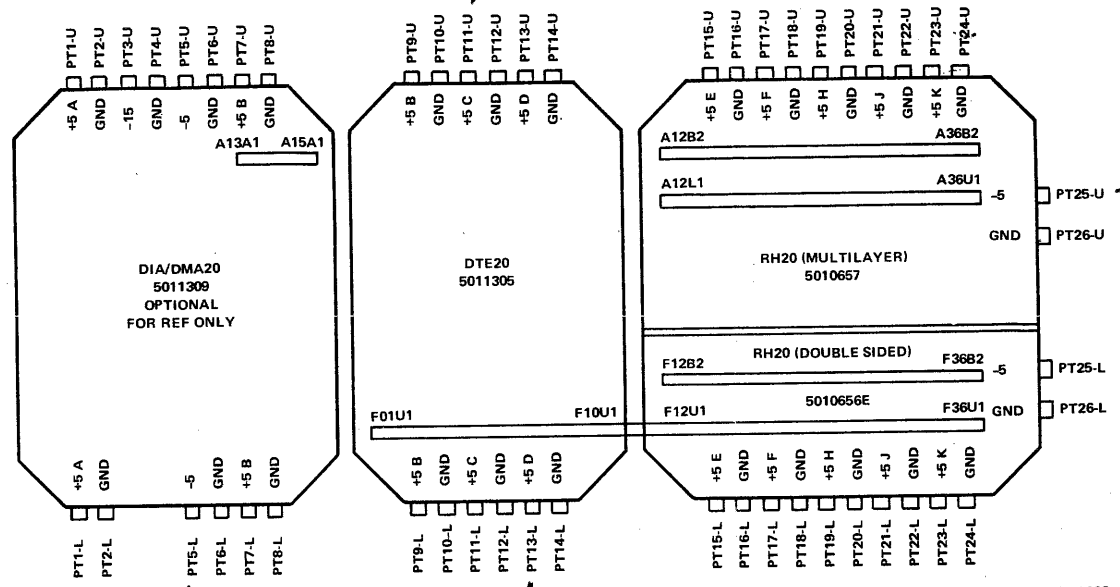
KL10 CPU DC POWER (DISTRIBUTION)

## I/O PWR

-4-

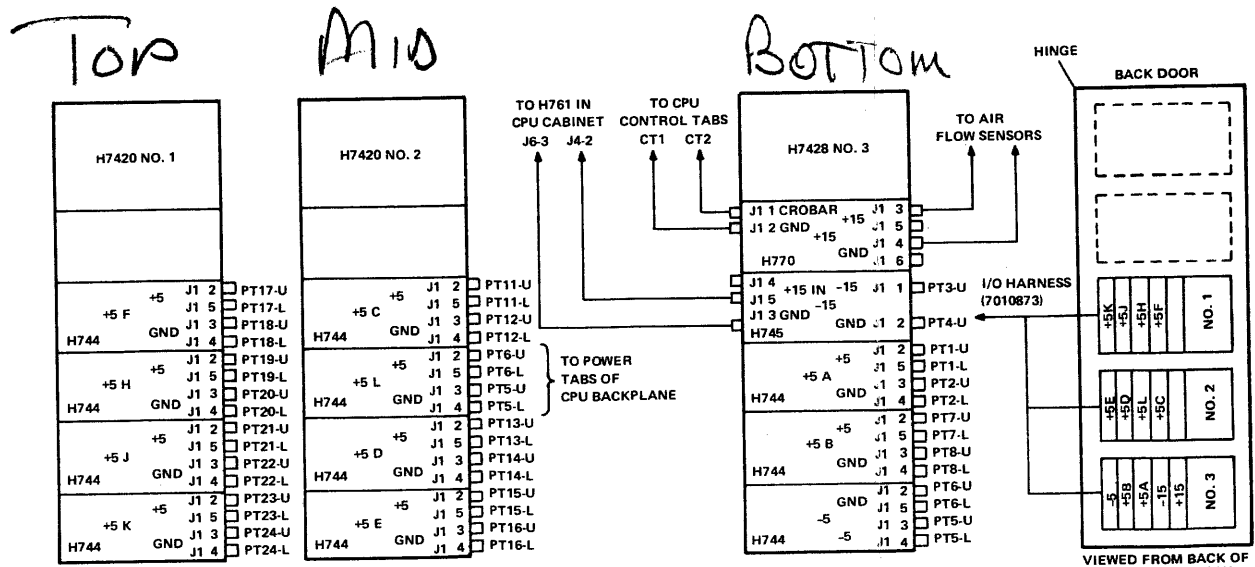
### Notes for KL10 I/O DC Power Layout

1. PTn - U represents upper power tabs on I/O backplane.
2. PTn - L represents lower power tabs on I/O backplane.
3. The following power tabs are jumpered together.  
PT7U to PT9U   PT8U to PT10U   PT7L to PT9L   PT8L to PT10L  
PT5U to PT25U   PT5L to PT25L   PT6U to PT26U   PT6L to PT26L
4. Pin block bus bars are used in the RH20 and DTE20 to distribute -5.0 V and in the DIA/DMA20 to distribute -15 V.
6. H7420 No. 2 (+5.0 L) supplies power tabs 5-U, 5L, 6U and 6L of the CPU backplane.
7. The +15 V regulator (H770) supplies the air flow sensors in the KL10 system.
8. The following color code is applicable.  
BLACK = GND   GREEN = -5   ORANGE = +15  
RED = +5   BLUE = -15



MR-2238

KL10 I/O DC POWER (BACKPLANE)



MR-2239

KL10 I/O DC POWER (DISTRIBUTION)

# ECL PWR

-6-

## KL10 ECL POWER ZONES

### -5.2 VOLTS

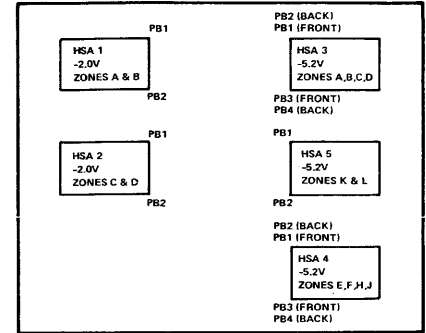
ZONE	POWER REG	PB #	CIRCUIT BRKR	SENSE MODULE	BACKPLANE MOD
A	HSA-3	1	CB1	SLOT 1 G8010	SLOTS 4-12
B	HSA-3	2	CB2	SLOT 1 G8010	SLOTS 13-17
C	HSA-3	3	CB3	SLOT 1 G8010	SLOTS 19-24
D	HSA-3	4	CB4	SLOT 2 G8010	SLOTS 25-29
E	HSA-4	1	CB5	SLOT 2 G8010	SLOTS 30-36
F	HSA-4	2	CB6	SLOT 2 G8010	SLOTS 38-41
H	HSA-4	3	CB7	SLOT 3 G8010	SLOTS 42-45
J	HSA-4	4	CB8	SLOT 3 G8010	SLOTS 46-50
K	HSA-5	1	CB9	SLOT 3 G8010	SLOTS 51-54
L	HSA-5	2	CB10		

### -2.0 VOLTS

ZONE	POWER REG	PB #	CIRCUIT BRKR	SENSE MODULE	BACKPLANE MOD
A	HSA-1	1	CB11	SLOT 5 G8011	SLOTS 4-14
B	HSA-1	2	CB12	SLOT 5 G8011	SLOTS 15-28
C	HSA-2	1	CB13	SLOT 5 G8011	SLOTS 29-41
D	HSA-2	2	CB14	SLOT 6 G8011	SLOTS 42-54



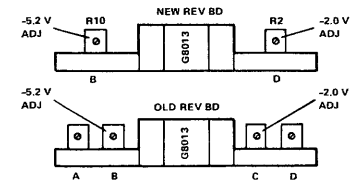
KL10 ECL POWER



SLOTS

1	2	3	4	5	6	7	8
G8010 -5.2V ZONES A,B,C	G8010 -5.2V ZONES D,E,F	G8010 -5.2V ZONES H,J,K	SPARE	G8011 -2.0V ZONES A,B,C	G8011 -2.0V ZONE D	G8013 +10V REF.	G8014 DC LOW DETECT.

G8013 +10 VOLT REF  
SLOT A07



MR-2235

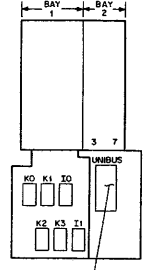


APR 34  
APR 35

MODULES (TYPE/DESCRIPTION/PRINTS)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
M9008	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200
BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED

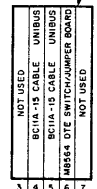
MODULE SLOT (FRONT VIEW - WIRE SIDE)



MODULES (TYPE/DESCRIPTION/PRINTS)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
M9008	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200	M9200
BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE	BC11A-18 CABLE
NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED

MODULE SLOT (FRONT VIEW - WIRE SIDE)





MODEL 'A'

SEE NOTES 1, 2 & 3

Slot	Type/Description/Prints	Module Slot (Front View - Wire Side)
1	M9008 BC20C-3C CABLE E AND C BUS	CPU1
2	M9008 BC20C-6C CABLE SBUS 0	CPU1
3	M9008 BC20C-6C CABLE SBUS 1	CPU1
4	M9008 BC20C-6C CABLE SBUS 0	CPU1
5	M9008 BC20C-6C CABLE SBUS 1	CPU1
6	M9008 BC20C-6C CABLE SBUS 0	CPU1
7	M9008 BC20C-6C CABLE SBUS 1	CPU1
8	M9008 BC20C-6C CABLE SBUS 0	CPU1
9	M9008 BC20C-6C CABLE SBUS 1	CPU1
10	M9008 BC20C-6C CABLE SBUS 0	CPU1
11	M9008 BC20C-6C CABLE SBUS 1	CPU1
12	M9008 BC20C-6C CABLE SBUS 0	CPU1
13	M9008 BC20C-6C CABLE SBUS 1	CPU1
14	M9008 BC20C-6C CABLE SBUS 0	CPU1
15	M9008 BC20C-6C CABLE SBUS 1	CPU1
16	M9008 BC20C-6C CABLE SBUS 0	CPU1
17	M9008 BC20C-6C CABLE SBUS 1	CPU1
18	M9008 BC20C-6C CABLE SBUS 0	CPU1
19	M9008 BC20C-6C CABLE SBUS 1	CPU1
20	M9008 BC20C-6C CABLE SBUS 0	CPU1
21	M9008 BC20C-6C CABLE SBUS 1	CPU1
22	M9008 BC20C-6C CABLE SBUS 0	CPU1
23	M9008 BC20C-6C CABLE SBUS 1	CPU1
24	M9008 BC20C-6C CABLE SBUS 0	CPU1
25	M9008 BC20C-6C CABLE SBUS 1	CPU1
26	M9008 BC20C-6C CABLE SBUS 0	CPU1
27	M9008 BC20C-6C CABLE SBUS 1	CPU1
28	M9008 BC20C-6C CABLE SBUS 0	CPU1
29	M9008 BC20C-6C CABLE SBUS 1	CPU1
30	M9008 BC20C-6C CABLE SBUS 0	CPU1
31	M9008 BC20C-6C CABLE SBUS 1	CPU1
32	M9008 BC20C-6C CABLE SBUS 0	CPU1
33	M9008 BC20C-6C CABLE SBUS 1	CPU1
34	M9008 BC20C-6C CABLE SBUS 0	CPU1
35	M9008 BC20C-6C CABLE SBUS 1	CPU1
36	M9008 BC20C-6C CABLE SBUS 0	CPU1
37	M9008 BC20C-6C CABLE SBUS 1	CPU1
38	M9008 BC20C-6C CABLE SBUS 0	CPU1
39	M9008 BC20C-6C CABLE SBUS 1	CPU1
40	M9008 BC20C-6C CABLE SBUS 0	CPU1
41	M9008 BC20C-6C CABLE SBUS 1	CPU1
42	M9008 BC20C-6C CABLE SBUS 0	CPU1
43	M9008 BC20C-6C CABLE SBUS 1	CPU1
44	M9008 BC20C-6C CABLE SBUS 0	CPU1
45	M9008 BC20C-6C CABLE SBUS 1	CPU1
46	M9008 BC20C-6C CABLE SBUS 0	CPU1
47	M9008 BC20C-6C CABLE SBUS 1	CPU1
48	M9008 BC20C-6C CABLE SBUS 0	CPU1
49	M9008 BC20C-6C CABLE SBUS 1	CPU1
50	M9008 BC20C-6C CABLE SBUS 0	CPU1
51	M9008 BC20C-6C CABLE SBUS 1	CPU1
52	M9008 BC20C-6C CABLE SBUS 0	CPU1
53	M9008 BC20C-6C CABLE SBUS 1	CPU1
54	M9008 BC20C-6C CABLE SBUS 0	CPU1

MODULE VARIATION CHART

Slot	NO CACHE	CACHE
17	M8549-YH	M8551
19	M8549-YH	M8551
24	M8549-YH	M8551
25	M8549-YH	M8551
27	M8549-YH	M8551
28	M8549-YH	M8551

NOTES:  
1. See notes 2 & 3. (BUS) BC20C cables from internal memory.  
2. Slot 1 (E/C BUS) BC20C cables from DTECO.  
3. DMS20 SBUS connection to slot 3 only.  
\*See module variation chart.

MODEL 'B'

SEE NOTES 1, 2 & 3

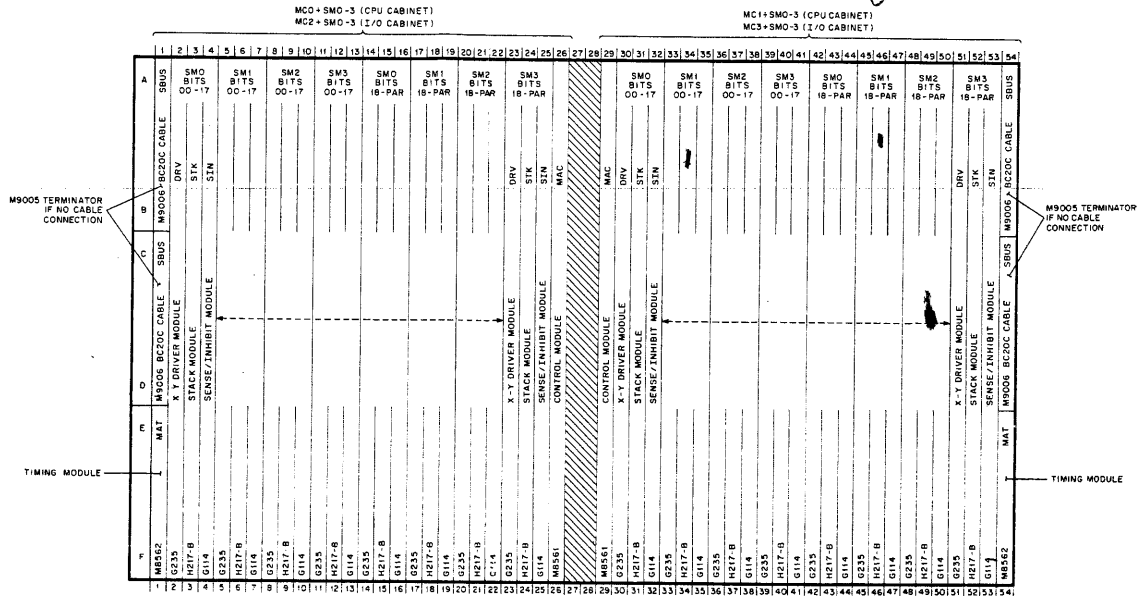
Slot	Type/Description/Prints	Module Slot (Front View - Wire Side)
1	M9008 BC20C-3C CABLE E AND C BUS	CPU1
2	M9008 BC20C-6C CABLE SBUS 0	CPU1
3	M9008 BC20C-6C CABLE SBUS 1	CPU1
4	M9008 BC20C-6C CABLE SBUS 0	CPU1
5	M9008 BC20C-6C CABLE SBUS 1	CPU1
6	M9008 BC20C-6C CABLE SBUS 0	CPU1
7	M9008 BC20C-6C CABLE SBUS 1	CPU1
8	M9008 BC20C-6C CABLE SBUS 0	CPU1
9	M9008 BC20C-6C CABLE SBUS 1	CPU1
10	M9008 BC20C-6C CABLE SBUS 0	CPU1
11	M9008 BC20C-6C CABLE SBUS 1	CPU1
12	M9008 BC20C-6C CABLE SBUS 0	CPU1
13	M9008 BC20C-6C CABLE SBUS 1	CPU1
14	M9008 BC20C-6C CABLE SBUS 0	CPU1
15	M9008 BC20C-6C CABLE SBUS 1	CPU1
16	M9008 BC20C-6C CABLE SBUS 0	CPU1
17	M9008 BC20C-6C CABLE SBUS 1	CPU1
18	M9008 BC20C-6C CABLE SBUS 0	CPU1
19	M9008 BC20C-6C CABLE SBUS 1	CPU1
20	M9008 BC20C-6C CABLE SBUS 0	CPU1
21	M9008 BC20C-6C CABLE SBUS 1	CPU1
22	M9008 BC20C-6C CABLE SBUS 0	CPU1
23	M9008 BC20C-6C CABLE SBUS 1	CPU1
24	M9008 BC20C-6C CABLE SBUS 0	CPU1
25	M9008 BC20C-6C CABLE SBUS 1	CPU1
26	M9008 BC20C-6C CABLE SBUS 0	CPU1
27	M9008 BC20C-6C CABLE SBUS 1	CPU1
28	M9008 BC20C-6C CABLE SBUS 0	CPU1
29	M9008 BC20C-6C CABLE SBUS 1	CPU1
30	M9008 BC20C-6C CABLE SBUS 0	CPU1
31	M9008 BC20C-6C CABLE SBUS 1	CPU1
32	M9008 BC20C-6C CABLE SBUS 0	CPU1
33	M9008 BC20C-6C CABLE SBUS 1	CPU1
34	M9008 BC20C-6C CABLE SBUS 0	CPU1
35	M9008 BC20C-6C CABLE SBUS 1	CPU1
36	M9008 BC20C-6C CABLE SBUS 0	CPU1
37	M9008 BC20C-6C CABLE SBUS 1	CPU1
38	M9008 BC20C-6C CABLE SBUS 0	CPU1
39	M9008 BC20C-6C CABLE SBUS 1	CPU1
40	M9008 BC20C-6C CABLE SBUS 0	CPU1
41	M9008 BC20C-6C CABLE SBUS 1	CPU1
42	M9008 BC20C-6C CABLE SBUS 0	CPU1
43	M9008 BC20C-6C CABLE SBUS 1	CPU1
44	M9008 BC20C-6C CABLE SBUS 0	CPU1
45	M9008 BC20C-6C CABLE SBUS 1	CPU1
46	M9008 BC20C-6C CABLE SBUS 0	CPU1
47	M9008 BC20C-6C CABLE SBUS 1	CPU1
48	M9008 BC20C-6C CABLE SBUS 0	CPU1
49	M9008 BC20C-6C CABLE SBUS 1	CPU1
50	M9008 BC20C-6C CABLE SBUS 0	CPU1
51	M9008 BC20C-6C CABLE SBUS 1	CPU1
52	M9008 BC20C-6C CABLE SBUS 0	CPU1
53	M9008 BC20C-6C CABLE SBUS 1	CPU1
54	M9008 BC20C-6C CABLE SBUS 0	CPU1

MODULE VARIATION CHART

Slot	NO CACHE	CACHE
17	M8549-YH	M8551
19	M8549-YH	M8551
24	M8549-YH	M8551
25	M8549-YH	M8551
27	M8549-YH	M8551
28	M8549-YH	M8551

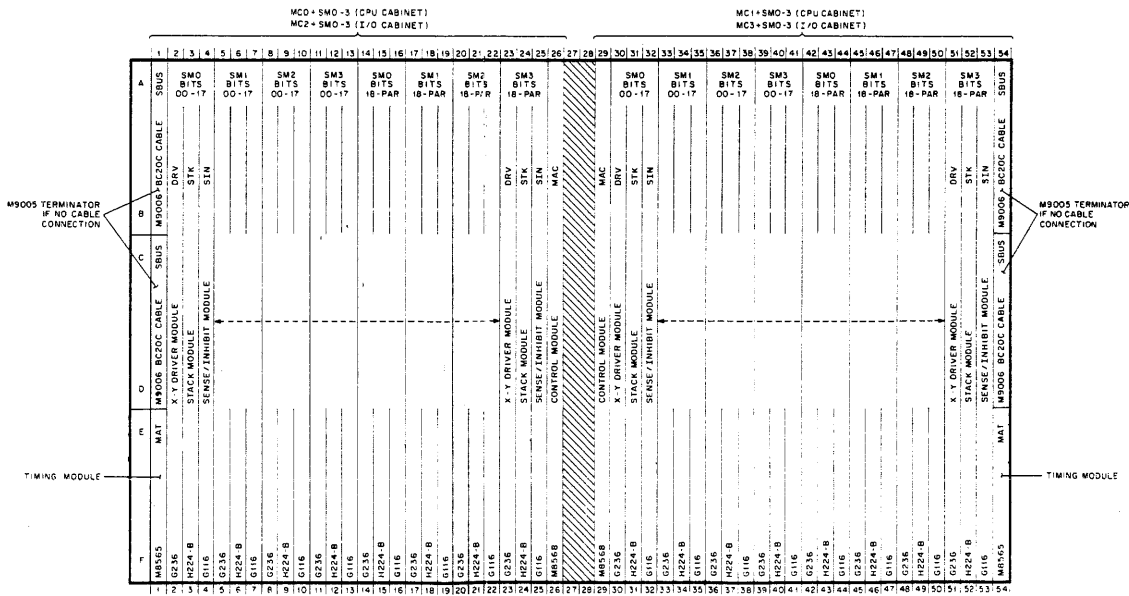
NOTES:  
1. See notes 2 & 3. (BUS) BC20C cables from internal memory & entry.  
2. Slot 1 (E/C BUS) BC20C cables from DTECO.  
3. DMS20 SBUS connection to slot 3 only.  
\*See module variation chart.

Cont 1



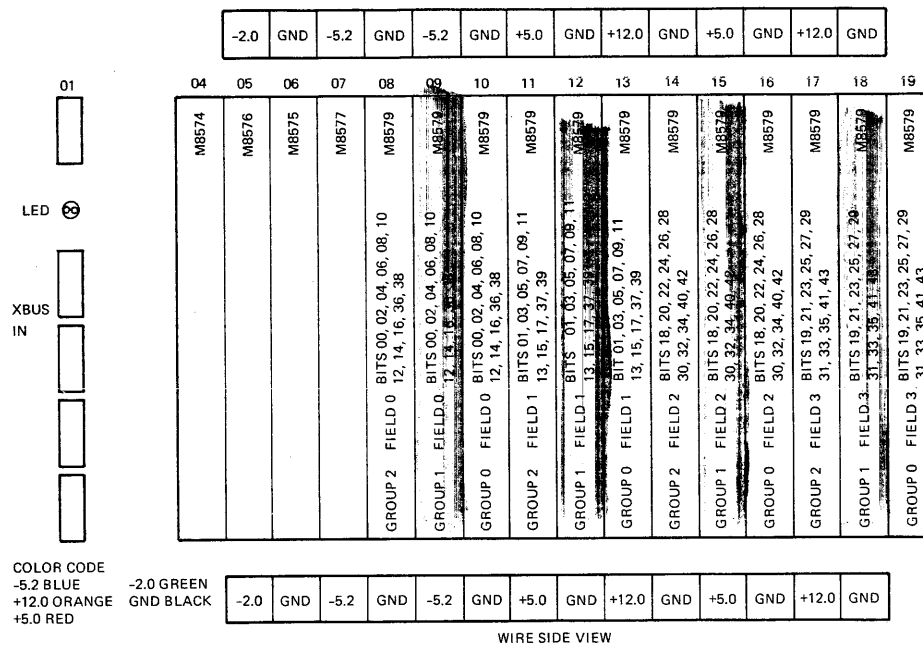
- NOTES:  
1. Viewed from wire side  
2. MU same for CPU and I/O cabinets

MA20 MUL

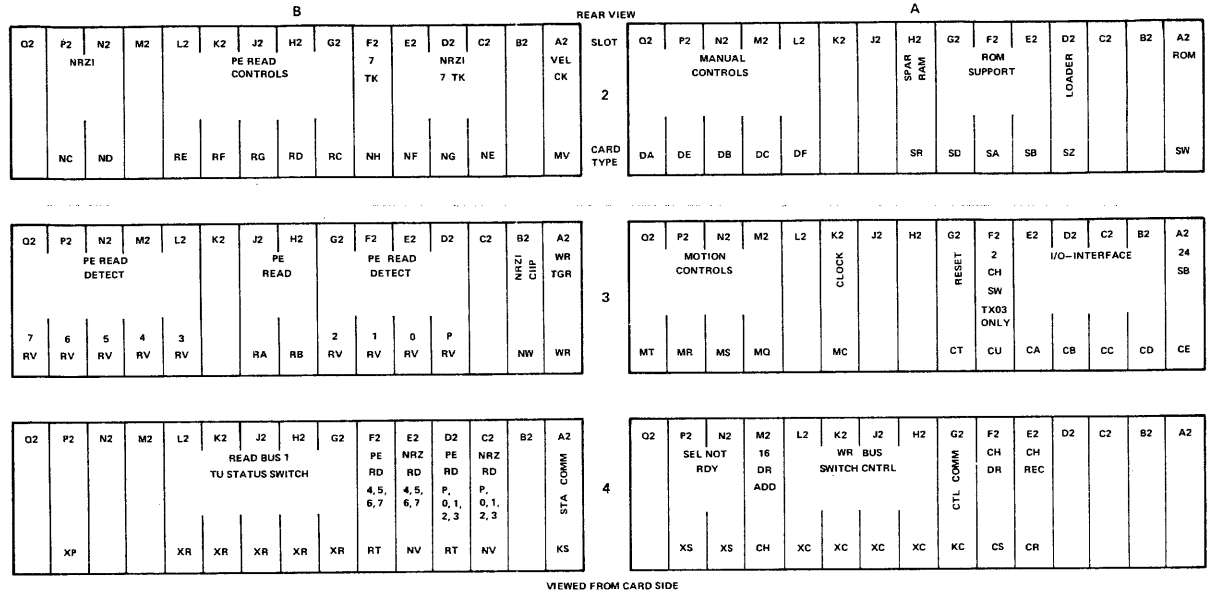


- NOTES:  
1. Viewed from wire side  
2. MU same for CPU and I/O cabinets

MB20 MUL

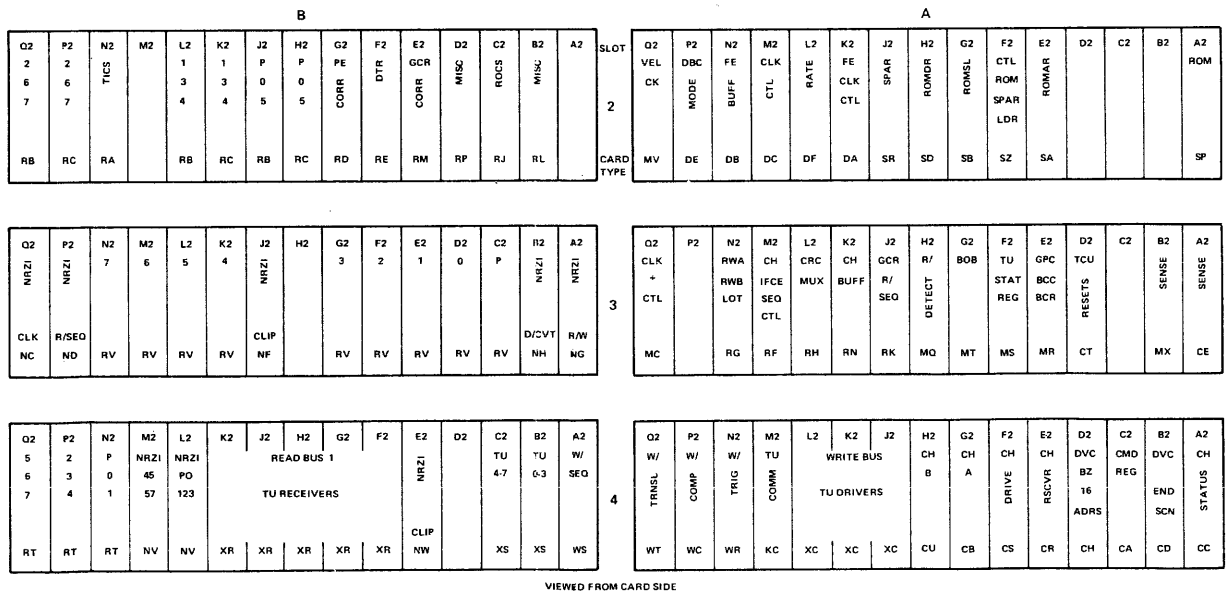


# TX01/TX02



MR-2311

## TX01 MUL



MR 2312

## TX02 MUL



	1	2	3	4	5	6
2A		THREAD LOAD LOGIC		COUNTER LOGIC		TESTER CONN
2B		GO/ REW/ UNLOAD LOGIC		REEL CONTROL LOGIC		AC CONTROL LOGIC
2C	EOT/BOT LOGIC	PADDLE TO R/W GATE (1A2)		I/O LOGIC		CONFIG LOGIC

FRONT VIEW

MR-2313

TU70 MUL

	1	2	3	4	5	6	7
1A	R/W TERM	PADDLE TO LOGIC GATE (2C2)	WRITE STATUS	WRITE DRIVER 5 P 0	WRITE DRIVER 7 2 5	WRITE DRIVER 3 1 4	LOAD CARD
1B	DAC	PE READ PRE AM 5, 7, 3, P, 2	PE READ PRE AM 1, 0, 6, 4	PADDLE TO HEAD AMP	NRZI READ PRE AM 0, 6, 4	NRZI READ PRE AM P, 2, 1	NRZI READ PRE AM 5, 7, 3

# WITS END...

*Pity the Corporate newcomers.  
Eyes glazed, damp hands  
trembling, they must master  
a wide vocabulary of company  
abbreviations and "DECronyms."  
It's enough to dismay the most  
technically sophisticated  
Ph.D.*

*But now they can take heart.  
Here's a list of the most  
commonly used abbreviations  
within Field Service for  
those who worry that a fatal  
slip of the tongue will send  
them to be Finally Assembled  
and Tested (FA&T) on their  
way to Finance and Admin-  
istration (F&A).*

JWYAN

HOPE THIS BOOKLET COMES IN HANDY.

IF YOU HAVE ANY "DECRONYMS" + MEANINGS  
NOT INCLUDED IN THIS BOOKLET SEND THEM  
TO:

NANCIE MITCHELL  
MR1-1/S35

ALSO, SEND US ANY "DECRONYM" YOU'VE  
SEEN AND YOU DON'T KNOW WHAT IT MEANS.

YOU'RE PROBABLY NOT ALONE

## A

A BUS - I/O Adaptor Bus  
 ACK - Affirmative Acknowledgement  
 ACP - Ancillary Control Process  
 ACU - Automatic Calling Unit  
 ADC (A/D) - Analog to Digital Converter  
 ADR - Address Data Register  
 - Address  
 AIDS - Automated Information and Diagnostic System  
 ALM - Area Logistics Manager  
 ALU - Arithmetic and Logic Unit  
 AND - Logic Function (both)  
 ANSI - American National Standards Institute  
 APA - Arithmetic Processing Accelerator  
 APL - Advanced Programming Language  
 AQL - Acceptable Quality Level  
 AR - Arithmetic Register  
 ARL - Authorized Returns List  
 ARO - After Receipt of Order

ARPA(NET) - Advanced Research Projects Administration (Network)  
 ASCII - American Standard Code for Information Interchange  
 ASM - Advanced Systems Manufacturing  
 ASR - Automatic Send/Receive Set  
 AST - Asynchronous System Trap  
 ASTLVL - Asynchronous System Trap Level  
 ASYNC - Asynchronous  
 AV - Audio Visual  
 AWB # - Air Waybill Number  
 AWT - Automatic Wire List

## B

BAS - Basic  
 BAUD - Speed = Events/Sec.  
 BBL - Bug Back List  
 BBU - Battery Backup Unit  
 BCC - Block Check Character  
 BCD - Binary Coded Decimal  
 BDA - BI Disk Adaptor

B		C	
BFSM	- Branch Field Service Manager	CAD	- Computer Aided Design
BFSS	- Branch Field Service Supervisor	CAI	- Computer Aided Instruction
BI	- Backplane Interconnect	CALDEC	- A CAD Tool used for PC Layout
BIMS	- Branch Inventory Management System	CB	- Circuit Breaker
BISYNC	- Binary Synchronous Communications	CC	- Cost Center
BIT	- Binary Digit	CCB	- Channel Control Block
BLA	- Branch Logistics Administrator	CCITT	- International Communications Standard
BLC	- Branch Logistics Coordinator	CCW	- Channel Control Word
BMC	- Basic Monthly Charge	CD	- Controlled Distribution (of warranty spares)
B/O	- Back Order	CER	- Central European Region
BOM	- Bill Of Material	CI	- Computer Interconnect
BOT	- Beginning of Tape	CIA	- Computer Interconnect Adaptors
BPG	- Business Products Group	CIS	- Corporate Information Services
bpi	- bytes per inch (magtape)	CLD	- Central Log Desk
bps	- bits per second	CM	- Corrective Maintenance - Compatibility mode bit in the hardware PSL
BR	- Buffer Register	COD	- Central Order Desk
BS	- Block Schematic	COS	- Commercial Operating System
BTA	- BI Tape Adaptor		
BYTE	- Binary Element String		

WITS

END

C		D	
CPG	- Commercial Products Group	DA	- Design Aids - Device Adaptor
CPL	- Cross Product Line	DAA	- Data Access Arrangement
CPM	- Cards/Minute	DAP	- Data Access Protocol
CPU	- Central Processing Unit	DAVFU	- Direct Access Vertical Format Unit
CR	- Central Region	db	- Decibel
CRB	- Channel Request Block	DBMS	- Data Base Management System
CRC	- Cyclic Redundancy Code	DC	- Data Communications (e.g.: DC10,DC76)
CRT	- Cathode Ray Tube	DCE	- Data Communications Equipment (modems,etc.)
CS	- Circuit Schematic (revision or documentation)	DCG	- Digital Components Group
CSG	- Commercial Systems Group	DCL	- Digital Control Logic
CSI	- Commercial Services Industrial Group	DCON	- Diagnostic CONsole Program
CSMC	- Customer Services Management Committee (Jack Shield's Staff)	DCP	- Device Control Program
CSS	- Computer Special Systems	DDB	- Device Data Block
CUSP	- Commonly Used Systems Programs	DDC	- Digital Diagnosis Center
CYC-0	- Cycle Ordering	DDCMP	- A Digital Designed Communications Protocol
		DDP	- Distributed Data Processing

D		E	
DDT	- Device Data Table - Dynamic Debugging Technique	DPSS	- District Product Support Supervisor
DEC	- Digital Equipment Corporation	DS	- Datasystems
DECnet	- Digital Networks	DSPL	- DEC Standard Price List
DECO	- Diagnostic Engineering Change Order	DTE	- DEC Ten/Eleven Interface - Data Terminal Equipment (source/sink)
DECUS	- Digital Equipment Computer Users Society		
DEPO	- Diagnostic Engineering Patch Order		
DFSM	- District Field Service Manager	E-1	- Emergency One (parts must be sent out within 7-days)
DI	- Device Interconnect	E BOX	- Logic Part of CPU (instruction execution unit)
DIAMON	- DIAGnostic MONitor	EBR	- Exec Base Register
DIBOL	- Digital Business Oriented Language	EC	- Etch Cut
DL	- Delay Line	ECB	- Exit Control Block
DM	- Defered Maintenance - District Manager	ECC	- Error Correcting Code
DMA	- Direct Memory Access	ECO	- Engineering Change Order
DMT	- Design Maturity Testing	ECL	- Emitter Coupled Logic
DOA	- Dead on Arrival	ECP	- Engineering Computation Products
DOS	- Disk Operating System	ECS	- Education Computer Systems
DPSM	- District Product Support Manager	EDP	- Electronic Data Processing

WITS END

**E**

EDU - Education Computer Group  
 EHQ - European Headquarters or Geneva  
 EIA - Electronic Industries Association  
 EMI - Electro Magnetic Interference  
 EMS - Engineering Model Shop  
 EOF - End of File  
 EOT - End of Tape  
 - End of Transmission  
 EPG - Education Products Group  
 EPMP - Exec Page Map Page  
 EPROH - Erasable Prom  
 EPT - Exec Page Table  
 EQ - FCO Parts + Documentation Kit  
 ESG - Engineering Systems Group  
 ESP - Execution Mode Stack Pointer  
 ESR - Exception Service Routine  
 EUR - Europe

**F**

F11ACP - Files-11 Ancillary Control Process  
 FA - FCO Documentation Kit  
 FAB - File Access Block  
 FA&T - Final Assembly and Test  
 F BOX - Logic Part of CPU (floating point)  
 FCA - Fixed Control Area  
 FCB - File Control Block  
 FCO - Field Change Order  
 FCS - First Customer Ship  
 FDT - Function Decision Table  
 FDX - Full Duplex  
 FE - Front End  
 FIFO - First In First Out (Buffer)  
 FLA - Field Logistics Administrator  
 FOB - Freight on Board  
 FP - Frame Pointer  
 FPA - Floating Point Accelerator  
 FPD - First Part Done  
 FPP - Floating Point Processor

<p><b>F</b></p> <p>FRU - Field Replaceable Unit</p> <p>FS - Field Service</p> <p>FSAR - Field Service Activity Report</p> <p>FSE - Field Service Engineer</p> <p>FSG - Federal Systems Group</p> <p>FSL - Field Service Logistics</p> <p>FU - Floating Underflow Trap enable bit in the PSW.</p> <p>FVS - First Volume Ship</p> <p>*F.Y. - Fiscal Year</p>	<p><b>H</b></p> <p>HDX - Half Duplex</p> <p>HOSS - Home Office Software Support</p> <p>HSC - Hierarchical Storage Controller</p> <p>HZ - Hertz - Cycles (frequency)</p>
<p><b>G</b></p> <p>GCR - Group Coded Recording (magtape 6250 bpi)</p> <p>GIA - General International Area</p> <p>GIS - Government Information Systems</p> <p>GPR - General Purpose Register</p> <p>GSD - Global Section Descriptor</p> <p>GSG - Government Systems Group</p> <p>GST - Global Symbol Table</p> <p>GT - Graphics Terminal</p>	<p><b>I</b></p> <p>I - (generally means instruction)</p> <p>IAS - Interactive Applications System</p> <p>I BOX - Logic Part of CPU (instruction address area)</p> <p>IC - Integrated Circuit</p> <p>I.C. - Inventory Control</p> <p>ICCS - InterComputer Communication Switch (same as CI)</p> <p>IDB - Interrupt Dispatch Block</p> <p>IDEA - Interactive Design &amp; Engineering Automation</p> <p>IEG - Internal Equipment Group</p> <p>IHFS - In House Field Service</p> <p>IMP - Interface Message Processor (ARFAnet)</p>



WITS

END

I			
INH	- In-House	ISR	- Interrupt Service Routine
I/O	- Input/Output	IV	- Integer Overflow Trap Enable bit in the PSW
IORB	- I/O Request Block	I+W	- Installation + Warranty
IOF	- Internal Order Form		
IPA	- ICCS Port Adaptor		
IPB	- Illustrated Parts Breakdown	<b>K</b>	
IPC	- Information Process Center	K\$	- A Thousand Dollars
IPG	- Industrial Products Group	K SYSTEMS	- Contract Systems
IPL	- Interrupt Priority Level	KA	- Kanata (Canada) Backplane Manufacturing
IPS	- Information Processing Services	KLAD	- KL Acceptance Diagnostic
IQ	- Installation Quality	KL COMP	- KL10 Compatibility
IR	- Instruction Register	KLDCP	- KL10 Diagnostic Console Program
IRP	- I/O Request Packet	KLDDT	- KL10 Dynamic Debugging Technique
IS	- Interrupt Stack bit in PSL	KLINIK	- KL Integrated Network for Investigation and Korrection
ISD	- Image Section Descriptor	KL REV	- KL10 Revision Control
ISECT	- Image Section	KSP	- Kernel Mode Stack Pointer
ISG	- Information Systems Group	KS COMP	- KS10 Compatibility
ISP	- Interrupt Stack Pointer	KS REV	- KS10 Revision Control

L	M
LAB - Laboratory	M72XX - Module - PDP11 System
LARS - Labor Activity Reporting System	M85XX - Module - KL System
LCEG - Large Computer Engineering Group	M86XX - Module - KS System
LCG - Large Computer Group	MAR - Mid Atlantic Region
LDP - Laboratory Data Products	MARK - Presence of Signal = Binary 1
LF - Line Feed	Mb - Megabyte
LIF - Line Item Forecasting	MBA - Mass Bus Adaptor
LOS - Level Of Service	MBI - Mass Bus Interface
LP - Line Printer	MBZ - Must be Zero
LPXX - Line Printer	M BOX - Logic Part of CPU (cache + paging)
LPC - Longitudinal Redundancy Check	MCA - Macro Cell Array
LPM - Lines/Minute	MCH - Monthly Cost of Maintenance
LSD - Large Systems Diagnostics	MCP - Macrocode Control Program
LSI - Large Scale Integration	MCR - Monitor Console Routine
LSG - Large Systems Group	MD - Memory Data - Micro Diagnostic Dispatcher
LUB - Line Unit Bus	MDC - Manufacturing, Distribution and Control Product Group
	MDG - Market Development Group

M			
MEG	- Maintainability Engineering Group	MTP	- Maynard Transfer Price
MFD	- Master File Directory	MTPR	- Move to Process Register Instruction
MFPR	- Move from Process Register Instruction	MTD	- Mean Time to Diagnose
MI	- Memory/Interconnect	MTR	- Mean Time to Repair
MIC	- Macro Interpretive Commands	MULTIDROP	- Line Accessible at a number of points
MLP	- Maynard List Price	MUTEX	- Mutual Exclusion Semaphore
MM	- Maintenance Manual	MUX	- Multiplexer
MME	- Memory Mapping Enable		
MODEM	- Modulator-Demodulator	N	
MOF	- Master Order Form	NAK	- Negative Acknowledgement
MOS	- Metallic Oxide Semiconductor	NER	- Northeast Region
MP	- Maintenance Print Set	NERU	- Non Field Replaceable Unit
MPS	- Micro Processing Systems	NI	- Network Interconnect
MRC	- Module Repair Center	NIBBLE	- Half 8 bit byte
MRL	- Model Revision Level	NPG	- New Products Group (Logistics)
MSE	- Maintenance Service Expense	NRZI	- Non Return to Zero Inverted (magtape)
MSI	- Maintenance Service Income - Medium Scale Integration	NSP	- Network Services Protocol
MTBF	- Mean Time Between Failures		

<b>O</b> OEM      - Original Equipment Manufacturer OP        - Order Processing OPCOM    - Operator Communication Manager OPSUM    - Option Summary OR        - Logic Function (either) OS        - Operating System		PAL       - Programming Assembly Language PC        - Printed Circuit - Program Counter PCB       - Process Control Block (SW/HW) - Printed Circuit Board PCBB     - Process Control Block Base Register PCM       - Plug Compatible Manufacturer PDL       - Program Design Language - Push Down List PDP       - Programmed Data Processor PE        - Phase Encoded (magtape) PERT     - Program Evaluation and Review Technique PFN       - Page Frame Number PIC       - Parts Information Catalog - Position Independent Code PID       - Process Identifier Number P/L       - Product Line PLM       - Product Line Manager	
<b>P</b> POBR     - Program Region Base Register POLR     - Program Region Length Register POPT     - Program Region Page Table PIBR     - Control Region Base Register P1LR     - Control Region Limit Register P1PT     - Control Region Page Table P-1      - Priority One Order (a machine is "down" and a F.S. part must be sent out in 48-hours) PACKET   - Group of Bits (Data, Control, Error Handling)			

WITS

END

<b>P</b>			
P/L REP	- Product Line Representative	PSW	- Processor Status Word
PM	- Preventive Maintenance	PT	- Page Table
PMC	- Pre Molded Carrier	PTE	- Page Table Entry
PME	- Performance Monitor Enable bit in PCB	PTT	- Post, Telephone and Telegraph Authority
PMT	- Process Maturity Testing		
PN	- Part Number	<b>Q</b>	
PO	- Purchase Order	QA	- Quality Assurance
POG	- Parts Ordering Guide	QC	- Quality Control
POTS	- Plain Old Telephone Service	QIO	- Queue Input/Output Request System Service
PRC	- Product Repair Center	<b>R</b>	
PROM	- Programmable Read Only Memory	RA	- Return Authorization
PROTOCOL	- Format/Timing Conventions	RAB	- Record Access Block
PS	- Programming Systems Product Support	RAM	- Random Access Memory
PSE	- Product Support Engineer	RAMP	- Reliability and Maintainability Program
PSECT	- Program Section	RC	- Rev Con (FA+T min. shippable level)
PSL	- Processor Status Longword	RCOF	- Regional Customer Obligation File
		RD	- Remote Diagnosis
		R&D	- Research and Development
		RED	- Reliability Exercise Diagnostic
		REV CON	- Revision Control

R	S
REV LEVEL - Revision Level	SBA - Shipping/Billing Authorization
RFA -- Request for Action - Record's File Access	SBI - Synchronous Backplane Interconnect (vax unibus)
RFI - Radio Frequency Interference	SBR - System Base Register
RFSM - Regional Field Service Manager	SCB - System Control Block
RIL - Restricted Items List	SCBB - System Control Block Base Register
RLM - Regional Logistics Manager	SDC - Software Distribution Center
RMS - Record Management Services	SDI - Standard Drive Interface
RMXX - Rotating Memory - Drive	SDLC - Synchronous Data Link Control
ROM - Read-Only Memory	SDS - Software Distribution Services
RPXX - Rotating Pack - Controller/Drive	SE - Systems Engineer
RPSM - Regional Product Support Manager	SHF CNT - Shift Counter
RSL - Recommended Spares List	SI - Storage Interconnect
RSTS - Resource Sharing Timesharing System	SIL0 - Hardware Buffer (first in/first out)
RTF - Return to Factory	SIRC - Signal Integrity Reference Conductor
RTL - Register Transfer Level	SLR - System Length Register
RTS - Real Time System	SMG - Site Management Guide
RWED - Read, Write, Execute, Delete	

S		T	
SMP	- Symmetrical Multi-Processing	T&C	- Terms and Conditions
SNR	- Signal-to-noise Ratio	TBD	- To Be Determined
SP	- Stack Pointer	TDXX	- Tape Deck - Controller
SPACE	- Opposite to MARK	TDR	- Time Domain Reflectometer
SPEC	- Specifications	TELCO	- Telephone Industry (Product Line)
SPR	- Software Performance Report	TFM	- Test Equipment Manufacturing
SPT	- System Page Table	TGHA	- The Great Heuristic Algorithm
SR	- Stockroom	TIP	- Terminal Interface Processor (Arpanet)
SRM	- System Reference Manual	TMXX	- Tape Magnetic - Controller
SSI	- Small Scale Integration	TOPS	- Time-Shared Operating Systems
SSP	- Supervisor Mode Stack Pointer	TP	- Trace Trap Pending bit in PSL
STR	- Structure (disk)	TPL	- Traditional Product Line
SUDS	- Stanford University Drawing System	TTL	- Transistor - Transistor Logic
SVA	- System Virtual Address	TU	- Tape Unit
SWS	- Software Services	TUMS	- Register Transfer Level Simulator
SYNC	- Synchronous	TWX	- Teletypewriter Exchange Service

<b>U</b>			
UBA	- UNIBUS Adapter	VMA	- Virtual Memory Address
UCB	- Unit Control Block	VMS	- Virtual Memory System (VAX Operating System)
UCODE	- Micro-Code	VMQ	- Virtual Address Multiplexer Quotient Register (generally means write)
UDA	- UNIBUS Disk Adaptor	VPN	- Virtual Page Number - Vendor Part Number
UDB	- Unit Data Block	VRC	- Vertical Redundancy Check
UETP	- User Environment Test Package	VT	- Video Terminal
UFD	- User File Directory		
UIC	- User Identification Code	<b>W</b>	
UOF	- Unusual Order Form	W	- (generally means write)
UPMP	- User Page Map Page	WATS	- Wide Area Telephone Service
UPT	- User Page Table	W BUS	- Write Bus
USP	- User Mode Stack Pointer	W SYSTEMS	- Warranty Systems
		WCB	- Window Control Block
<b>V</b>		WCP	- Worst Case Patterns
VA	- Virtual Address	WCS	- Writeable Control Store
VAX	- Virtual Address Extended	WDCS	- Writeable Diagnostic Control Store
VCB	- Volume Control Block	WO	- Woburn Logistics Headquarters
VFU	- Vertical Format Unit	WP	- Word Processing
VIBA	- Virtual Instruction Buffer Address		
VLSI	- Very Large Scale Integration		



WITS END

**W**  
WR - Western Region  
WS - Word Station  
WT - Word Terminal

**X**  
XOR - Logic Function  
(exclusive or)

" W I T S E N D "  
- - - - -  
WE INVENTED THE SOLUTION.  
EXPLAINED NIFTY DECRONYMS.

SEPTEMBER '79

# WITS END...

*Pity the Corporate newcomers. Eyes glazed, damp hands trembling, they must master a wide vocabulary of company abbreviations and "DECronyms." It's enough to dismay the most technically sophisticated Ph.D.*

*But now they can take heart. Here's a list of the most commonly used abbreviations within Field Service for those who worry that a fatal slip of the tongue will send them to be Finally Assembled and Tested (FA&T) on their way to Finance and Administration (F&A).*

JWYAN

HOPE THIS BOOKLET COMES IN HANDY,

IF YOU HAVE ANY "DECRONYMS" + MEANINGS  
NOT INCLUDED IN THIS BOOKLET SEND THEM  
TO:

NANCIE MITCHELL  
MRI-1/S35

ALSO, SEND US ANY "DECRONYM" YOU'VE  
SEEN AND YOU DON'T KNOW WHAT IT MEANS.

YOU'RE PROBABLY NOT ALONE

WITS END

<b>A</b>	ADC	- Analog to Digital Converter	<b>B</b>	BAS	- Basic
	AIDS	- Automated Information and Diagnostic System		BFSM	- Branch Field Service Manager
	ALU	- Arithmetic and Logic Unit		BFSS	- Branch Field Service Supervisor
	ANSI	- American National Standards Institute		BIMS	- Branch Inventory Management System
	APL	- Advanced Programming Language		BLC	- Branch Logistics Coordinator
	AQL	- Acceptable Quality Level		BMC	- Basic Monthly Charge
	ARL	- Authorized Returns List		B/O	- Back Order
	ARO	- After Receipt of Order		BOM	- Bill Of Material
	ASC11	- American Standard Code for Information Interchange		BOT	- Beginning of Tape
	ASM	- Advanced Systems Manufacturing		BPG	- Business Products Group
	ASR	- Automatic Send/Receive Set		bpi	- bytes per inch
	AWB #	- Air Waybill Number			

SEPTEMBER '79

WITS END

**C** CAD - Computer Aided Design  
 CAI - Computer Aided Instruction  
 CC - Cost Center  
 CD - Controlled Distribution (of warranty spares)  
 CIS - Corporate Information Services  
 CLD - Central Log Desk  
 CM - Corrective Maintenance  
 COD - Central Order Desk  
 CPG - Commercial Products Group  
 CPL - Cross Product Line  
 CPU - Central Processing Unit  
 CR - Central Region  
 CRT - Cathode Ray Tube  
 CSI - Commercial Services Industrial Group  
 CSMC - Customer Services Management Committee (Jack Shield's Staff)  
 CSS - Computer Special Systems  
 CUSP - Commonly Used Systems Programs

**D** DBMS - Data Base Management System  
 DCG - Digital Components Group  
 DCL - Digital Control Logic  
 DDC - Digital Diagnosis Center  
 DDP - Distributed Data Processing  
 DEC - Digital Equipment Corporation  
 DECnet - Digital Networks  
 DECUS - Digital Equipment Computer Users Society  
 DFSM - District Field Service Manager  
 DIBOL - Digital Business Oriented Language  
 DM - Deferred Maintenance - District Manager  
 DMA - Direct Memory Access  
 DMT - Design Maturity Testing  
 DOA - Dead on Arrival  
 DOS - Disk Operating System  
 DPSM - District Product Support Manager  
 DPSS - District Product Support Supervisor  
 DS - Datasystems

SEPTEMBER '79

WITS END

<b>E</b>	ECO - Engineering Change Order	<b>F</b>	FA&T - Final Assembly and Test
	ECL - Emitter Coupled Logic		FCO - Field Change Order
	ECP - Engineering Computation Products		FCS - First Customer Ship
	ECS - Education Computer Systems		FLA - Field Logistics Administrator
	EDP - Electronic Data Processing		FOB - Freight on Board
	EDU - Education Computer Group		FPP - Floating Point Processor
	EHQ - European Headquarters		FRU - Field Replaceable Unit
	EHS - Engineering Model Shop		FS - Field Service
	EOF - End of File		FSAR - Field Service Activity Report
	EOT - End of Tape		FSE - Field Service Engineer
	EPG - Education Products Group		FSG - Federal Systems Group
	ESG - Engineering Systems Group		FSL - Field Service Logistics
	EUR - Europe		
		<b>G</b>	GIA - General International Area
			GIS - Government Information Systems
			GSG - Government Systems Group
			GT - Graphics Terminal
		<b>H</b>	HOSS - Home Office Software Support

SEPTEMBER '79

WITS END

I	IAS	- Interactive Applications System	L	LAB	- Laboratory
	IC	- Integrated Circuit		LARS	- Labor Activity Reporting System
	I.C.	- Inventory Control		LCEG	- Large Computer Engineering Group
	IDEA	- Interactive Design & Engineering Automation		LCG	- Large Computer Group
	IEG	- Internal Equipment Group		LDP	- Laboratory Data Products
	IHFS	- In House Field Service		LF	- Line Feed
	INH	- In-House		LIF	- Line Item Forecasting
	IOF	- Internal Order Form		LOS	- Level Of Service
	IPB	- Illustrated Parts Breakdown		LP	- Line Printer
	IPG	- Industrial Products Group		LPXX	- Line Printer
	IPS	- Information Processing Services		LSI	- Large Scale Integration
	IQ	- Installation Quality		LSG	- Large Systems Group
	ISG	- Information Systems Group			
K	KLAD	- KL Acceptance Diagnostic			
	KL COMP	- KL10 Compatibility			
	KLINIK	- KL Integrated Network for Investigation and Korrection			
	KL REV	- KL10 Revision Control			
	KS COMP	- KS10 Compatibility			
	KS REV	- KS10 Revision Control			

SEPTEMBER '79

WITS END

<b>M</b>	M72XX	- Module - PDP11 System	<b>O</b>	OEM	- Original Equipment Manufacturer
	M85XX	- Module - KI System		OP	- Order Processing
	M86XX	- Module - KS System		OS	- Operating System
	MAR	- Mid Atlantic Region	<b>P</b>	P-1	- Priority One Order
	MCM	- Monthly Cost of Maintenance		PAL	- Programming Assembly Language
	MDC	- Manufacturing, Distribution and Control Product Group		PC	- Printed Circuit
	MDG	- Market Development Group		PDP	- Programmed Data Processor
	MEG	- Maintainability Engineering Group		PERT	- Program Evaluation and Review Technique
	MM	- Maintenance Manual		PIC	- Parts Information Catalog
	MOF	- Master Order Form		P/L	- Product Line
	MOS	- Metallic Oxide Semiconductor		PLM	- Product Line Manage
	MPS	- Micro Processing Systems		P/L REP	- Product Line Representative
	MRC	- Module Repair Center		PM	- Preventive Maintenance
	MRL	- Model Revision Level		PMT	- Process Maturity Testing
	MSE	- Maintenance Service Expense		PO	- Purchase Order
	MSI	- Maintenance Service Income		POG	- Parts Ordering Guide
	MTBF	- Mean Time Between Failures		PRC	- Product Repair Center
	MTTR	- Mean Time to Repair		PROM	- Programmable Read Only Memory
<b>N</b>	NER	- Northeast Region		PS	- Programming Systems - Product Support
				PSE	- Product Support Engineer

SEPTEMBER '79

WITS END

<b>Q</b>	QC	- Quality Control	<b>S</b>	SBA	- Shipping/Billing Authorization
<b>R</b>	RAM	- Random Access Memory		SDC	- Software Distribution Center
	RAMP	- Reliability and Maintainability Program		SDS	- Software Distribution Services
	RD	- Remote Diagnosis		SE	- Systems Engineer
	R&D	- Research and Development		SIRC	- Signal Integrity Reference Conductor
	RED	- Reliability Exercise Diagnostic		SPR	- Software Performance Report
	REV LEVEL	- Revision Level			
	RFA	- Request for Action	<b>T</b>	T&C	- Terms and Conditions
	RFI	- Radio Frequency Interference		TDXX	- Tape Deck - Controller
	RFSM	- Regional Field Service Manager		TDW	- Time Domain Reflectometer
	RIL	- Restricted Items List		TELCO	- Telephone Industry (Product Line)
	ROM	- Read-Only Memory		TEM	- Test Equipment Manufacturing
	RMXX	- Rotating Memory - Drive		TMXX	- Tape Magnetic - Controller
	RPXX	- Rotating Pack - Controller/Drive		TOPS	- Time-Shared Operating Systems
	RPSM	- Regional Product Support Manager		TPL	- Traditional Product Line
	RSL	- Recommended Spares List		TTL	- Transistor - Transistor Logic
	RSTS	- Resource Sharing Timesharing System		TU	- Tape Unit
	RTF	- Return to Factory			
	RTS	- Real Time System			

SEPTEMBER '79

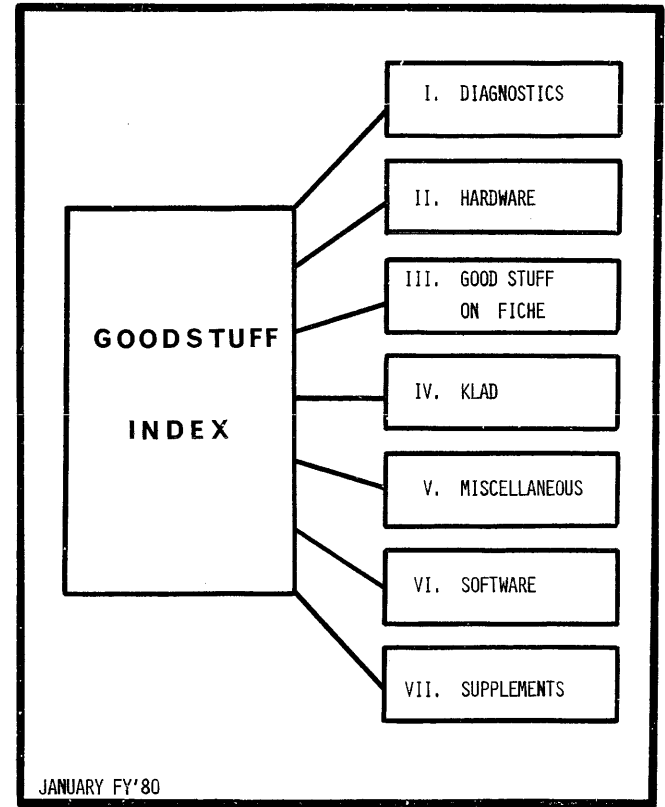


WITS END

<b>U</b>	UOF	- Unusual Order Form
<b>V</b>	VAX	- Virtual Address Extended
	VT	- Video Terminal
<b>W</b>	WP	- Word Processing
	WR	- Western Region
	WS	- Word Station
	WT	- Word Terminal

BY THE WAY... "W I T S E N D"  
STANDS FOR:  
WE INVENTED THE SOLUTION. EXPLAINED  
NIFTY DECRONYMS.

SEPTEMBER '79



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### DIAGNOSTICS

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### DIAGNOSTICS

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HARDWARE

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## HARDWARE

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