MAGNETIC TAPE EQUIPMENT TYPES 50/51/52

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CHAPTER 1

INTRODUCTION

1-1 PURPOSE AND SCOPE

The purpose of this instruction manual is to aid personnel in the installation, operation and maintenance of two magnetic tape systems used with the DEC Programmed Data Processor-1. This manual, a supplement to the basic PDP-1 Maintenance Manual, describes the Automatic Tape Control Unit, Type 52; the Programmed Tape Control Unit, Type 51; and the DEC-designed Local Tape Control, which is mounted in each Type 50 Tape Transport Unit. A separate manufacturer's manual for the tape transport is furnished with the tape system.

Throughout this manual an automatic tape system comprising a Type 52 Automatic Tape Control and one or more Type 50 Tape Units is referred to as a Type 52 System. A programmed tape system comprising a Type 51 Programmed Tape Control and one or more Type 50 Tape Units is referred to as a Type 51 System.

1-2 CHAPTER SUBJECTS

A brief summary of system use and application is presented in Chapter 2, General Description. This chapter also lists system specifications and physical characteristics.

Chapter 3, Installation, provides instructions for initial installation and setup of the system.

Chapter 4, System Function, provides a full general description of all system operations. At block diagram level, Chapter 4 explains what the system does rather than describing the specific hardware and connections involved in the various functions. Also included in this chapter are descriptions of tape format, write and read signal flow and all magnetic tape instructions.

Chapter 5, Operating Procedures, explains the use of all controls and indicators on the tape system control panels, as well as the basic operating procedures for normal functions.

Chapter 6, Tape System Logic, presents a complete and detailed description of the logic in both tape control units and of the DEC-designed logic in the tape transport unit. This chapter also includes flow charts of all system operations.

Chapter 7, Circuit Description, describes the function, specifications and circuit theory of all DEC System Modules not described in the basic PDP-1 manual.

Chapter 8, Maintenance, contains information useful in adjustment, calibration, troubleshooting and repair of the tape equipment. This chapter also describes the function and use of the DEC Tape Unit Calibrator.

1-3 FIGURES

This manual includes three general classes of figures: logic diagrams, circuit schematics, and miscellaneous figures such as photographs, flow charts, block diagrams and layout drawings. Complete system logic is shown in logic drawings for Chapter 6. This chapter also includes the flow charts. Circuit schematics accompany Chapter 7. Block diagrams, photographs and layout drawings illustrate the other chapters. Chapters 7 and 8 also include various cable and wiring diagrams.

All figures are assembled in numerical order at the back of the manual. References to all figures except circuit schematics are of the form "Figure 5-1" (i.e. the first figure of Chapter 5.) Circuit schematics are arranged in order by circuit type designation.

CHAPTER 2

GENERAL DESCRIPTION

2-1 PURPOSE OF SYSTEM

One of the many PDP-1 options is the magnetic tape system. This system provides computer input-output at a much faster rate than other peripheral devices, and may also be used as high capacity, slow access storage to augment core memory. Two kinds of tape option are available: automatic systems and programmed system. This manual describes one system of each kind.

The Type 52 Automatic Tape System transfers blocks of characters between computer memory and tape. By using the high speed channels it allows computation to continue while the transfer is in process. Special features include scatter read and gather write automatic bit-by-bit read-compare with core memory automatic lateral parity error detection while reading and writing and rapid tape search by skipping a preselected number of records. Tape format is standard IBM with choice of odd or even parity. Each automatic tape control can handle up to eight tape units. A maximum of three tape controls (for capability of 24 tape units) can be added to the PDP-1.

The Type 51 Programmed Tape System transfers information between computer and tape one character at a time. All transfer operations including error checking and assembly of characters into computer words must be performed by subroutines. Some choice of tape format is allowed including standard IBM. The programmed tape control can handle up to three tape units.

All tape system components are housed in standard DEC equipment frames and run on ordinary 60 cycle, 117 volt current. The control unit of the automatic system contains built-in marginal checking to facilitate preventive maintenance. No special wiring, subflooring or air conditioning is required.

2-2 SYSTEM COMPONENTS

Equipment comprising two of the PDP-1 tape systems is shown in Figure 2-1. Both systems include a tape control, the Programmed Tape Control Type 51, or the Automatic Tape Control Type 52.

Each Type 50 Tape Transport Unit includes the DEC-designed Local Tape Control (read-write electronics) and two components designed by Potter Instrument Company: the M906II-1 Tape Transport, and the M3323 Drive Electronics Unit. The Type 51 or 52 Tape Control governs the tape unit through the local control. All motion and status signals between local control and the transport pass through the Potter drive electronics. Data signals, however, go directly between the read-write electronics and the read and write heads.

Both tape systems are governed from the in-out transfer control section of PDP-1. For the Type 52 Automatic System, six iot instructions are added to the computer repertoire. These instructions specify a tape unit, initial and final addresses, and a tape command. The Type 52 Control then selects the specified tape unit and executes the command automatically. This process is independent of further computer operations, so the computer may continue with the program. All required tape operations are executed by the Type 52 hardware. Each time the Type 52 Control has finished writing a word on tape or reading a word from tape, it gains direct access to memory through a high speed channel. Data transfers are made to or from consecutive memory locations, starting with the initial address and ending with the final address. Since the high speed channel control includes three channels, up to three Type 52 Controls (and hence 24 tape units) may be added to the computer.

The Type 51 Programmed Tape System, like the Type 52 System, is governed from iot control. However, all data transfers are made through the in-out register one character at a time. The five iot instructions added to the computer repertoire select the tape unit and its operating mode (read or write, odd or even parity, etc.) and initiate the individual character transfers. The write instruction transfers a character from the in-out register to the tape control to be written on tape; each character read from tape must be detected by the program and transferred to the in-out register by a read instruction. The program must also assemble the characters into words and deposit them in memory.

A typical automatic tape system including a Type 52 Tape Control and three tape units is shown in Figure 2-2. The tape control requires an entire bay and each tape unit, including a tape transport, is mounted in an additional bay. In a programmed system the tape units also require one bay each, but the Type 51 Control is mounted in the bottom of one of the tape unit bays.

2-3 SYSTEM OPERATING SPECIFICATIONS

SYSTEM PARAMETERS

Characters	7 bits: 6 data, 1 parity
Parity	
Lateral	Odd or even
Longitudinal	Even
Transfer rate	15,000 characters/second
Density	200 characters/inch
Minimum record length (excluding longitudinal parity character)	
Type 52 System	3 characters
Type 51 System	1 character
Load point gap	6"
Longitudinal parity character spacing	0.020" 0.023" (4 character spaces)
Inter-record gap	3/4"
Recording	NRZ
Errors detected	
Type 52 System	Parity, skipped character, read-compare, illegal command, late HSC access
Type 51 System	Parity

TRANSPORT PARAMETERS

Tape	1.5 mil polyester, 2400' long, 1/2" wide
Speed	75 ips
Start time	3 ms
Start distance	0.15"
Stop distance	0.10"
Single unit stop-start interval	10 ms
Read-write heads	7 channel
Data protection	Write enable ring
Detected conditions	

Load point	10' from physical beginning of tape
Full reel	<100' of tape on takeup reel
Low reel	<100' of tape on supply reel
End point	14' from physical end of tape
Load point and end point detection	Photoelectric
Rewind speed	300 ips
Rewind time	1 3/4 minutes, full reel
Reel diameter	10 1/2"

2-4 PHYSICAL CHARACTERISTICS

CONSTRUCTION

All magnetic tape equipment is housed in Standard DEC Bays (all steel construction). Control panels are aluminum.

MODULES

Standard DEC System Plug-in units, series 1000 and series 4000.

POWER EQUIPMENT

Power supplies series 700; power controls series 800.

LOGIC

Solid state. Transistors and crystal diodes operating on static logic levels (0 vdc and -3vdc).

DIMENSIONS

Each DEC bay has the following dimensions:

Height 69 1/2 inches
Width 22 inches
Depth 26 inches

Usually, however, several units are bolted together — the overall length then being 20" per unit plus 2" for the end panels. For example, if a Tape Control Type 52 and three tape units are bolted together, total length is 82".

UNIT WEIGHTS

Tape Unit Type 50 (including transport and logic) 600 pounds

Tape Control Type 51 65 pounds

Tape Control Type 52 500 pounds

Each pair of unused end panels reduces system weight by 90 pounds.

2-5 POWER REQUIREMENTS

LINE VOLTAGE INPUT

105 to 125 volts, 60 cycle, single phase

CURRENT CONSUMPTION

Tape Unit Type 50	7.5 amperes average, 740 watts. However, under heavy operating conditions, the tape unit may draw 20-ampere peaks.
Tape Control Type 51	0.5 ampere, 60 watts
Tape Control Type 52	4 amperes (6-ampere peaks), 410 watts

2-6 EQUIPMENT LIST

All PDP-1 tape equipment is housed in Standard DEC Bays. The front of each bay can accommodate up to 12 horizontal 19-inch mounting panels (DEC Type 1914). Each panel can hold 25 Standard DEC Plug-in Logic Modules. Inside the double doors at the back of each bay is an inner plenum door supporting the required power supplies and power controls.

A typical automatic tape installation is shown in Figure 2-2. The Type 52 Tape Control (left) is bay 1. All tape units of a system are designated bay 2 for purposes of module location. The tape transport is behind the glass door on the front of the tape unit. The transport and the manual control panel together take up the upper half of the unit. Behind the double doors in the lower half are the logic, the drive electronics, a test panel and a bus socket panel.

a LOGIC PANELS AND POWER EQUIPMENT - Complete front and back layouts of tape system bays 1 and 2 are shown in Figures 2-3 and 2-4. The front of bay 1 (Type 52 includes an indicator panel and seven mounting panels of logic. In general each mounting

panel contains a complete subsection of logic and is shown in a single logic drawing in Chapter 6. The figure number is at the lower left of each panel. On the back of bay 1 are a power control, the logic power supplies and a variable power supply for marginal checking.

The upper half of bay 2 (tape unit) contains the tape transport and the manual control panel. The components listed in the layout drawing (Figure 2-4) are also shown in Figure 2-5, a photograph of the tape unit with the double doors open. Below the transport is the drive electronics: test points and fuses on the left, plug-in modules on the right. The DEC tape unit equipment, below the drive electronics, includes the gain, slice and test ponit panel, the logic for local tape control and the bus socket and taper pin panel for cable connections between tape control and tape unit. The unit shown in Figure 2-5 is unit 1 of a programmed tape system. Below the bus socket panel is the logic for the Programmed Tape Control Type 51. In all units of a Type 52 System and in units 2 and 3 of a Type 51 System, this logic is replaced by a blank panel.

The back of the tape unit (Figure 2-4) includes an isolating transformer, a power control and a power supply for the Type 50 Logic. However, in unit 1 of the Type 51 System, an additional power control and power supply for the Type 51 Logic are mounted at the top of the plenum door.

The following table lists the mounting panel and power equipment requirements for the three tape system components described in this manual.

Tape Transport Unit Type 50 (Figure 2-4)

Space requirement	1 bay
Logic	1 mounting panel (2G)
Power equipment	1 power supply 728
	1 power control 822 (811B)
	1 isolation transformer

Programmed Tape Control Type 51 (Figure 2-4)

Logic	1 mounting panel (2H)
Power equipment	1 power supply 728
	1 power control 811

Automatic Tape Control Type 52 (Figure 2-3)

Space requirement	1 bay
Logic	7 mounting panels (1A to 1H)
Power equipment	3 power supplies 728
	1 variable power supply 734
	1 power control 811

b MODULE LIST - The following list includes all plug-in modules required by local tape control in the Type 50, Programmed Tape Control Type 51 and Automatic Tape Control Type 52. Circuits indicated by an asterisk (*) are described in Chapter 7 of this manual. All other circuits are described in Chapter 10 of the basic PDP-1 manual.

Local Tape Control

Type	Quantity
Differential Amplifier 1536* or 1549*	4
Rectifying Slicer 1542*	3
Indicator Driver 1669	1
Inverter 4105	5
Inverter 4106R	1
Diode 4112R	3
Diode 4113	2
Delay 4301	1
NRZ Writer 4514*	4

Programmed Tape Control Type 51 and Automatic Tape Control Type 52 - Numbers in parentheses indicate modules that must be added to PDP-1 iot control to govern the tape system.

Type	Quantity	
	Type 51	Type 52
Delay 1304		1
Peak Detector and Slicer 1539*	4	4
Indicator Driver 1669		5
Bus Driver 1685		8 (1)

Type	Quantity Type 51	Type 52
Inverter 4105	2 (1)	14
Inverter 4106		2
Inverter 4106R	1	9
Diode 4111	1	4
Diode 4112		2
Diode 4112R		1
Diode 4113	2	13
Diode 4113R	2	3
Capacitor-Diode 4126		6
Capacitor-Diode 4127	2	5
Capacitor-Diode 4127R		4
Capacitor-Diode 4128	2	14
Binary-to-Octal Decoder 4151*		1
Dual Flip-Flop 4202*		9
Dual Flip-Flop 4209		2
Quadruple Flip-Flop 4213		5
Quadruple Flip-Flop 4214	4	11
4-Bit Counter 4215*	2	2
Delay 4301	2	17
Integrating Delay 4303*		3
Clock 4401		1
Clock 4407*		1
Pulse Amplifier 4603	1 (4)	15 (4)

CHAPTER 3

INSTALLATION

3-1 SITE SELECTION

Before installing a magnetic tape system, select a suitable location near the PDP-1 computer. The Tape Control Type 52 must be installed within 25 feet of the computer. Furthermore, the tape units must be within 25 feet of the tape control. In the programmed system the Type 51 Tape Control is mounted in tape unit 1 so the entire system must be within 25 feet of the computer.

All system equipment frames are 69 1/2" high. The floor area occupied by the system depends upon the number of tape units that are included (equipment dimensions are given in paragraph 2-4). Usually the equipment frames are bolted together in groups. At least 3 feet of clearance should be allowed on all sides of the equipment for access during maintenance.

A level floor is required because the equipment frames are mounted on casters. The floor should be capable of supporting 150 psf.

The system is designed to operate efficiently from 50° to 100°F. The plug-in modules are cooled by blowing air out the front of the bays. Intake fans are factory-installed in the floor of all DEC bays, and in the top of each tape unit bay as well. No additional cooling equipment is required.

All units run on ordinary 115 volt, 60 cycle current. Since each bay has its own ac line, a separate outlet must be provided for every unit. Tape units should each be connected to a 20 ampere line. A 10 ampere line is sufficient for the Type 52 Tape Control. All cables are equipped with Miller Electric Type 034-2 Connectors.

3-2 INSTALLATION

The bays containing the tape control and the tape units are usually bolted together into one or two large equipment frames. However, the drive electronics and the isolation transformer for each tape unit are packed separately and must be installed before the system is ready for use. All cabling within a single equipment frame is installed at the factory. All cables necessary

to connect the different frames are packed in a single separate container. Thus a tape system including one Type 52 Control and three tape units would be shipped as a single large equipment frame and seven additional containers: three contain drive electronics units, three contain isolation transformers, and one contains the necessary cables.

a UNPACKING - Each equipment frame is shipped on a skid. The frame is wrapped in plastic, a wooden cover is placed on the top, and the entire package is held on the skid with metal straps. The tape unit subassemblies and cables are shipped separately in ordinary packing containers.

(1) Carefully remove the metal straps, wooden cover and plastic from the equipment frame. Remove the frame from the skid and place as desired near the PDP-1.

(2) The plenum doors at the rear of the bays have spring catches. To reinforce these doors during shipment two screws are used to hold each door shut. Remove these screws and store them in the plastic loops provided.

(3) Remove any packing material, shipping blocks, etc., from the inside of the frame.

(4) The plug-in modules are taped into the logic panels to prevent damage in shipment. Remove the tape.

(5) Unpack the cables, transformers and drive electronics units.

> NOTE: If the user plans to reship the equipment (or move it more than a short distance) in the near future, special packing materials should be saved for reuse. The containers for drive electronics units and transformers, in particular, are designed especially to accommodate the equipment and are the safest means of packing it for reshipment.

b INSTALLATION OF SUBASSEMBLIES - The user must install a drive electronics unit and an isolation transformer in each tape unit. Mount the drive electronics just below the tape transport with the fuses at the left end of the unit (see Figure 2-4). The mounting bolts are already in place at the sides of the bay front, behind the double doors. Correct mounting of the unit is shown in Figure 2-4 of the Potter Handbook.

Two cables connect the drive electronics to the rest of the tape unit. The cable from the Type 50 Logic is coiled and taped to the bay floor. Remove the tape and plug this cable

into the smaller receptacle at the back of the drive electronics. The cable from the tape transport is coiled and taped around the transport motors. Remove the tape and plug this cable into the larger receptacle at the back of the drive electronics.

The isolation transformer must be mounted on the second panel from the bottom on the inside of the plenum door at the rear of the bay (see Figure 2-4). The mounting bolts and connecting cables for the transformer are already in place. Each cable is marked by a numbered tag. On the front of the transformer are two sets of terminals covered with plastic plates. On the plastic are strips of tape bearing corresponding terminal numbers. Connect the cables to the matching transformer terminals.

c BUS CONNECTIONS - At the bottom of each tape unit is a bus socket and taper pin panel (Figure 3-1). The socket in the upper right provides connection to the manual control panel at the top of the unit. The other two sockets are for the tape control bus (TC bus).

All tape units are connected to a single bus from the tape control. The TC bus enters each tape unit at the left of the socket panel and leaves at the lower right. Connections between the two sockets are made through the taper pins in the center of the panel. There are three taper pin blocks, each containing three horizontal rows of pins. In all three blocks, connections from the in-bus are made to the center row, while connections to the out-bus are made from the bottom row. Connections to the Type 50 Logic and to the socket for the control panel connector are made from the top row.

All cables within a single equipment frame are installed at the factory. However, bus connections between the tape system and the computer, and between separate equipment frames within the system, must be made at the site.

Bus connections for the Type 52 Tape System are shown in Figure 3-2. A panel containing four bus sockets is located at the bottom of the Type 52 Control. Three cables connect the tape system to the in-out transfer control section of the PDP-1. The in-out plugs at the computer are labelled to correspond to the bus sockets at the tape control: J52-1, -2 and -3. The TC bus socket, J52-4, is equivalent to J50-4A and J50-4B in all tape units. If the system is divided between two equipment frames, J50-4B in the last unit of the first frame must be connected to J50-4A in the first unit of the second frame.

The bus connections for the Type 51 Tape System are shown in Figure 3-3. Since the Programmed Tape Control Type 51 is mounted in tape unit 1, and all three units are bolted into a single frame, only one bus need be installed. This connects the computer to J51-4 at the left of the unit 1 socket panel. Connections to the Type 51 Control are made directly from J51-4. Connections between the Type 51 and the rest of the tape system are then made through the taper pins. Note, however, that the bus connections in tape units 2 and 3 are just the opposite of those in the units of the Type 52 System. The bus connections are reversed in order that all tape units except unit 1 of the Type 51 System will have the same taper pin wiring. The unit that contains the Type 51 Logic must provide voltage to the unit calibrator through the out-bus. Reversing the bus connections prevents the mixing of logic voltages between two adjacent units.

3-3 INSPECTION AND CHECKOUT

The tape system is thoroughly tested and checked before it leaves the factory. However, it should be inspected and checked again after installation to make sure that no damage has occurred during shipment.

a INSPECTION - After the tape equipment has been unpacked and installed, the system should be inspected visually. Check the following:

(1) Have a drive electronics unit and an isolation transformer been installed in every tape unit?

(2) Have all bus connections between computer and tape system been made properly?

(3) Have all shipping blocks, packing materials, tape, etc. been removed? A coiled ac power line is taped to the fan at the bottom of each bay. Remove the tape but do not plug in the power lines.

(4) Are all plug-in units inserted firmly in position?

(5) Are there any loose nuts or bolts?

(6) Are there any loose or broken wires?

b PREOPERATIONAL CHECKOUT - Before using the tape system make sure that the entire system turns on and off properly and that the tape transport functions correctly. The checkout

procedure makes use of the following switches:

The POWER switch and indicator located at the lower right of the Type 52 Indicator Panel;

The TRANSPORT POWER switch and indicator located at the left end of the tape unit manual control panel;

The circuit breakers and LOCAL/REMOTE switch on each Type 811 and 822 (811B) Power Control.

All switches and indicators in the tape system are described in detail in paragraphs 5-2 and 5-3. The following checkout procedure is complete for both the Type 52 and Type 51 Tape Systems. For either system merely ignore those steps that refer only to the other. All steps that refer to the tape unit should be performed on all tape units.

(1) Make sure computer power is off.

(2) Turn OFF the TRANSPORT POWER switch on the manual control panel. Turn off (down) the Type 52 POWER switch.

(3) Load a tape into the tape unit. Complete tape loading procedure is described in paragraph 5-4.

(4) Switch the 811 and 822 power controls to REMOTE.

(5) Plug in the ac lines and make sure all 811 and 822 circuit breakers are closed. All units should remain off.

(6) Switch the 822 power control to LOCAL. This applies power to the Type 50 Logic.

(7) Set TRANSPORT POWER to REMOTE. Nothing should happen.

(8) Push TRANSPORT POWER to the momentary contact ON position. The transport should go on, lighting the associated indicator. When the switch is returned to REMOTE, power remains on.

(9) Switch the 882 power control to REMOTE. All tape unit power including the transport goes off.

(10) Turn on (up) the Type 52 POWER switch.

(11) Switch the 811 power control into LOCAL. With Type 52 this turns on the power indicator and applies power to the entire tape system. With the Type 51, both the 811 and the unit 1 822 power controls must be switched to LOCAL. This turns on only the Type 51 Logic and unit 1. (To turn on the entire system, switch all power controls to LOCAL.)

(12) Switch the 811 power control to REMOTE. With the Type 52, the entire tape system should go off. With the Type 51 all power controls must be returned to REMOTE to turn off the entire system.

(13) Turn on the computer. The entire tape system should go on with the computer.

(14) Turn off the computer. The entire tape system should go off.

(15) Check the operation of the tape transport as described in paragraph 5-5.

CHAPTER 4

SYSTEM FUNCTION

4-1 LOGICAL ORGANIZATION

The logical configuration of the PDP-1 Type 52 Automatic Magnetic Tape System is shown in Figure 4-1. The Tape Control Type 52 functions as an automatic buffer between the computer and the tape units. Program iot instructions govern the entire tape system by providing addresses and commands to the tape control. The tape control then goes into automatic operation, regulating both its own operations and those of the addressed tape unit. All data transfers between tape system and computer are made directly to memory through a high speed channel.

To place the tape system in operation the program must provide three types of information:

1. It must select a tape unit by providing a unit address.
2. It must specify the quantity of data to be processed by providing a pair of memory addresses. These addresses define a range of memory locations for retrieval or storage of data through a high speed channel.
3. It must tell the system what to do with the data by providing a tape command.

The program performs the first two functions through the address logic, the third through the command logic.

The address logic contains three registers and an equality net. The program provides these three registers with tape unit, initial and final addresses. For each tape operation the tape control selects a tape unit according to the unit address (UA). The first HSC access to memory is made according to the initial address. Subsequently, the initial address becomes the current address (CA). The tape control keeps count of data transfers by incrementing this current address by 1 on each HSC access. When the current address becomes equal to the final address (FA),the equality net indicates that the operation is complete. This equal address condition produces a sequence break in the computer. If the program then resets the initial and final addresses before termination takes place, the operation continues.

Besides providing addresses to the tape control, the program must also provide a tape command to the command register (CR). The command is decoded to govern the operation of both the tape control and the selected tape unit. The control portion of the Type 52 contains two parts: in-out control and format control. Basically, in-out control governs the transfer of information between computer and tape control, while format control governs transfers between tape control and tape unit. In-out control governs program initiation of all tape operations, transfers of data through a high speed channel and requesting of sequence breaks. All status levels for both tape control and tape unit are also provided to the computer by in-out control.

Format control includes logic for the sequences of operations that produce the correct tape format in writing and that respond properly to the same format in reading. Format control also generates high speed channel requests whenever a full computer word has been read or written; it provides timing for the termination of a tape operation in order to produce the correct record gap; it positions the tape properly with respect to the read and write heads.

Data is transferred between computer memory and tape through a set of three data transfer registers. All transfers between computer and tape system are full-word transfers between the memory buffer and the 18-bit data word buffer (DWB). In writing, format control divides the word in DWB into three characters which are made available to the tape through the single-character write buffer (WB). In reading, format control assembles three consecutive characters from the single-character read buffer (RB) into a full word in DWB.

In the programmed tape system, the Type 52 Control is replaced by a Type 51 and no use is made of high speed channels or sequence break system. All command information and data are transferred through the in-out register and most control and address functions must be provided by the computer. The Type 51 Control includes only a pair of single-character buffers for data transfer and a command register which includes bits for tape unit selection. All data transfers are single-character transfers, made completely under program control. In writing, the program must transfer each character to the character buffer (CB); it is then made available to the tape through the write buffer (WB). In reading, the character buffer doubles as a read buffer, and the program must transfer each character to the in-out register. The command register specifies the tape unit operating mode but governs no functions in the tape control except parity mode.

4-2 TAPE FORMAT

PDP-1 magnetic tape units use 1/2" wide tape containing 7 information channels. The tape format produced by the Type 52 Automatic Tape Control is shown in Figure 4-2. With the Type 51 Programmed Tape Control the computer may provide the necessary timing to duplicate this format or may write the tape in some other format if desired.

The left part of Figure 4-2 shows the tape in relation to the read and write heads. The tape moves by the heads vertically — forward direction being downward. The tape is composed of a mylar base coated on one side with an iron oxide composition. The oxide or dull side of the tape faces the heads, with the left edge toward the transport drive plate. The recording rate of 15,000 characters/second means that one character is written every 66.67 microseconds. Since the tape moves at 75 ips, there are 200 characters/inch,and the characters are spaced 0.005 inches apart.

The method of recording used is nonreturn-to-zero (NRZ). Although the tape has two basic states of remanent magnetization, the remanent magnetic state of the tape at a given bit position does not determine the value of that bit. A logical 1 is represented by a change from one state of magnetization to the other, in either direction. A logical 0 is represented by a constant state of magnetization. Thus, writing a character containing all 0s is equivalent to producing blank tape. Each time a character is transferred into the write buffer, the NRZ writers produce an equivalent character on the tape. Because of the NRZ type of recording however, a transfer into the buffer is not a normal 1 transfer. Instead, whenever a 1 is to be written in a given tape channel,the corresponding bit of the buffer is complemented, producing a change in tape magnetization.

The structure and spacing of the individual tape characters are shown at the right in Figure 4-2. Each 18-bit computer word is divided into three 6-bit characters in DWB. The write buffer, however, contains seven flip-flops corresponding to the seven tape channels. A parity bit is transferred into the buffer with each 6-bit data character, producing a tape character of six data bits and a lateral parity bit. Channel 1 contains the least significant data bit; channel 6, the most significant. The parity of the character may be either odd or even, as specified by the program.

In reading the tape, only 1s are detected. If odd parity is used, there must be a 1 in at least

one channel of every character so that all characters will be detected. However, if six 0 data bits are written with even parity, a character containing all 0s is produced. This is equivalent to a character space and is interpreted by the system as a missing character error. After the first 1 bit of a character is detected, the tape control waits 25 microseconds for the read buffer to receive all the bits in the character. This procedure allows a tape skew of up to 0.0018" without loss of information.

The smallest unit of information that can be written on the tape is a record. Since each word is divided into three characters, a record contains 3n data characters, where n is the number of words provided by the computer for a given write operation. After the last data character is written, the tape control writes 0.020" of blank tape (270 microseconds at 75 ips), and then clears the write buffer to produce an end-of-record character (EOR). A complete record therefore contains 3n+1 characters, that is, 3n data characters and the EOR character. Since the write buffer flip-flops always begin a record in the 0 state, returning the buffer to its initial state at the end of the record produces even longitudinal parity in all tape channels.

The smallest unit of information that can be read by the tape control is also an entire record. This does not mean, however, that the entire record must be deposited in computer memory. In a read operation, the program specifies initial and final addresses for transfer of information to memory. If, when the addresses become equal, they are reset within 100 microseconds, the operation continues. If the addresses remain equal for longer than the allowed time, all high speed channel transfers to memory cease, but the tape control continues reading until the end of record is reached. If the address range specified by the program is greater than the number of words in the record, the tape stops at the end of the record even though the addresses have not become equal.

In all normal tape operations, therefore, the tape always stops so that both the read head and the write head are within the record gap. The distance that the EOR character moves beyond the read head, in combination with the delay before writing is allowed, always produces at least 3/4" of blank tape between records. Since only 1s are written on the tape (the failure to detect a 1 during the reading of a character is interpreted as a 0) the absence of write signals during a write operation erases the tape, i.e. produces blank tape. The actual position of the heads within the gap depends upon the type of operation just completed. The EOR character always moves slightly further beyond the heads in writing than in reading. This prevents

generation of inter-record trash, which can be produced by failing to erase the entire record gap when writing on a previously recorded tape.

Since the spacing between the read and write heads is 0.30", every character passes the read head 4 milliseconds after it is written. Thus in a write operation the characters are read in order to check for parity or missing character errors, but no transfers beyond the read buffer occur.

Besides detecting changes in magnetization through the read head, the tape unit also includes a photoelectric system for sensing beginning and end of tape and a mechanical system for detecting low tape supply. The low reel condition (less than 100 feet of tape on the supply reel) is provided to the tape control as a status condition but is not used within the tape unit. In the rewind operation, the full reel condition (less than 100 feet of tape on the takeup reel) returns the tape unit to normal speed for the remainder of the rewind and the tape finally halts at load point. The load point and end point of the tape are marked by reflective strips mounted on the side of the tape away from the heads. These strips are detected by photodiodes which sense light reflected from them. In writing on a newly mounted or rewound tape, a gap of 6" is left from the load point before writing can begin. If the tape should run to the end point in any operation the tape unit stops automatically.

4-3 TAPE WRITE AND READ SIGNAL FLOW

Figure 4-3 is a block diagram of the tape system write and read paths for a single channel. The write path begins at the write buffer in the tape control and ends at the tape, while the read path begins at the tape and ends at the tape control read buffer. Most of the equipment shown in the figure is located physically in the read-write electronics of the tape unit.

In the write path, both outputs of a WB flip-flop are connected to an NRZ writer whose three outputs are in turn connected to the two ends and centertap of a write head inductor. The NRZ writer contains a pair of semiconductor switches. If the write enable level is not asserted, both switches are off and no current flows in the inductor. However, if write enable is asserted, one (and only one) switch must be on because the two switches are controlled by complementary outputs of a WB flip-flop. If the upper switch is closed, current flows through the upper coil in the direction shown by the arrow. If the lower switch closes, current flows through the lower coil.

The tape control writes information on the tape by complementing the WB bit. So long as a given WB bit remains in the same state, the corresponding writer switch remains closed, and current still flows through the same half of the write head coil. This is equivalent to writing 0s on the tape every 66.7 microseconds. Whenever a 1 is to be written on the tape, the WB bit is complemented; this reverses the states of the two writer switches, causing current to flow in the other half of the coil. This, in turn, changes the direction of magnetization in the tape channel. Current flow through the two halves of the coil for writing a typical tape message is shown by the graphs above and below the current lines. A similar graph represents the direction of tape magnetization for the same message as shown at the right.

A tape passes the read head 4 milliseconds after passing the write head. So long as the direction of tape magnetization remains the same, no current flows in the read head coil. However, when the read head encounters a change in the direction of magnetization, current flows through the coil. Each change causes current flow in the opposite direction from the preceding change. Typical current flow for two consecutive tape 1s is shown by the waveforms above the connecting lines from the coil to the differential amplifier.

The differential amplifier provides considerable amplification for difference signals but only fractional amplification for common mode signals. Amplifier waveforms are shown to the left. The amplifier also includes a balance potentiometer to assure that the output signals are the same amplitude regardless of polarity.

The output of the differential amplifier is applied to a rectifying slicer. No slicer output can be generated unless the read enable level is asserted. This prevents the sending of read signals to the tape control when tape is in motion but is not being read as, for example, in the rewind operation. The rectifying slicer generates a negative output pulse for an input pulse of either polarity from the differential amplifier. However, no slicer output is generated unless the input exceeds a threshold level. Thus a low level noise input cannot generate an output pulse.

The rectifying slicer output feeds a peak detector and slicer in the tape control. The pulse produced through the read path from the read head is long compared to the duration of most logic levels within the tape control. Therefore, for the time during which the input pulse exceeds a preset threshold level, the slicer portion of the peak detector and slicer produces a logic level output. Further, the peak detector produces a logic pulse output at the peak of the input pulse. The two outputs — a logic level and a pulse — are applied to a capacitor-diode gate to set a flip-flop in the read buffer.

4-4 TYPE 52 TAPE INSTRUCTIONS

With the installation of a Type 52 Automatic Tape System, eight in-out transfer instructions are added to the PDP-1 repertoire. Each of these instructions is executed in a single computer memory cycle of 5 microseconds. In order to place the tape system in operation, the program must execute the two initiating instructions. These provide the necessary addresses and tape commands. The tape system then executes the command automatically. When the address-equal condition occurs during a tape operation, the program may provide new initial and final addresses through the two reset instructions without stopping the tape operation in process. The automatic tape instructions also include a pair of examine instructions (through which the program may check the condition of the tape system) and a pair of maintenance instructions. The entire set of eight instructions uses the iot primary operation code and six of the secondary operation codes (both maintenance instructions use the same second code as one of the reset instructions). Furthermore, one of the initiating instructions has a third 4-bit operation code. This third code is the tape command which is executed by the tape control.

In all magnetic tape instructions, bits 6 and 7 of the instruction word (denoted by 'ab' in the instruction code) select the tape control. The three tape controls are addressed at 00, 01 and 10. If there is only one tape control these bits are ignored. In the following list the instruction codes are given in octal with capital letters representing variable octal digits. Whenever binary digits are necessary, they are given as 1s and 0s in parentheses or are represented by lower case letters. For convenience, the tape control is often referred to as the TC, while the tape unit is referred to as the TU. In some instructions, reference is made to various status bits. These correspond to the tape status conditions and are described under the instruction mes. Each status bit number corresponds to its position in the in-out register when tape status is examined by mes.

Initiating Instructions:

Magnetic Tape Unit and Final Address .....

.....muf Instruction Code 72abxC76

The $C(AC_{15-17})$ replace C(UA); $C(IO_{2-17})$ replace C(FA). The unit address transferred to UA selects that TU whose unit selector is set to the same address. If the program is about to initiate a read or write command, the memory address transferred to FA must be 1

greater than the desired final address to which high speed channel access is to be made during execution of the command. However, if the program is about to initiate a space command, the number transferred to FA must be 1 less than the total number of records to be spaced over.

If the selected TC is not busy, muf is properly executed and the computer skips the next instruction in sequence. If TC is busy, muf is performed as a nop and the computer goes on to the next instruction in sequence. In either event, C(IO) and C(AC) remain unchanged.

Bits 5, 8 and 9 of the instruction are ignored. Bits 10 and 11 (octal digit C) adjust the states of the continue flip-flops in order to select one of three possible end-of-record actions. When the end of a record is reached, the tape control clears the busy flip-flop (status bit 3) and returns a completion pulse to the computer. If the sequence break system is on, the TC requests a break. The three end-of-record actions are as follows:

(1) Normal Completion and Stop, C=0. Upon reaching the end-of-record, the tape stops with the head at the appropriate distance past the EOR character. The tape control waits 10 milliseconds to allow the pinch rollers to settle down and then returns the completion pulse.

(2) Early Completion and Stop, C=1. Upon reaching the end-of-record, TC returns the completion pulse immediately. Thus the programmer can use the same TC to initiate a tape command on a different TU while the previously selected TU is stopping. This saves 10 milliseconds of program time.

(3) Early Completion and Continue, C=3. Upon reaching the end-of-record, TC returns the completion pulse immediately, and the previously selected TU continues in operation. During a 2 millisecond interval following the completion pulse, the program must provide new initiating instructions. In this manner many records can be processed without stopping the tape. If new instructions are not given within the allotted time, TC repeats the previous command with Early Completion and Stop, producing the following results:

(a) If the previous command was Write, the tape control writes a complete record gap and then stops with the heads at the appropriate distance in a second gap.

(b) If the previous command was Read or Readcheck, the tape control processes

the next record. HSC transfers continue until the addresses become equal, but the tape control reads to the end-of-record in the normal manner. Since the completion pulse at the end of the first record clears the busy flip-flop, the processing of the second record can be interrupted by a new muf instruction. Use of this procedure to read two records with a single pair of initiating instructions is therefore not recommended.

(c) If the previous command was Forward Space or Backspace, the tape control spaces the tape to the end of the reel. Since any number of records can be spaced with a single tape command, Early Completion and Continue should not be specified with a space command unless the command is definitely intended to be changed.

Magnetic Tape Initial Address and Command .....

.....mic Instruction Code 72abnN75

Bits 8 through 11 of the mic instruction (MB_{8-11}) replace C(CR); C(IO_{2-17}) replace C(CA). This instruction also sets the TC busy flip-flop, clears the HSC request flip-flop and clears the status flip-flops which indicate tape system errors. The mic instruction contains a third operation code nN which specifies the tape command that the system is to perform. As soon as nN is transferred into the command register, the tape control begins automatic operations and places in operation the tape unit selected by the previous muf. The memory address for initial high speed channel access is provided from IO to the current address register. As each word is processed the current address is incremented by 1 so that the next HSC access will be made to the next consecutive memory location. For space commands, IO should contain zero.

Bit 5 of mic is ignored. If the selected TC is not busy and the TU selected by the previous muf is ready, mic is properly executed, and the computer skips the next instruction in sequence. If either TC or TU are not available, mic is performed as a nop and the computer goes on to the next instruction in sequence. In either event, C(IO) remain unchanged.

The following table lists the tape commands with their mnemonic codes and octal codes. The octal code is given as the center pair of octal digits in the instruction word when tape control 0 is selected. That is, the code represents abnN with a and b both 0. To provide a tape command to TC 1, add 20 to the code as given; to provide a command to TC 2, add 40. All

commands that generate or check parity have two codes: even code for even parity, odd for odd parity.

Command	Mnemonic Code	Octal Code
Stop	mst	00
Rewind	mrw	01
Backspace	mbs	02, 03
Forward Space Check Even Parity	mfe	10
Forward Space Check Odd Parity	mfo	11
Write Even Parity	mwe	12
Write Odd Parity	mwo	13
Read and Compare Even Parity	mce	14
Read and Compare Odd Parity	mco	15
Read Even Parity	mre	16
Read Odd Parity	mro	17

Stop - This command should only be used immediately after the return of a completion pulse following a muf instruction that called for early completion and continue with same unit. Stop clears the command register, halting the tape.

Rewind - This command merely initiates the rewind operation — the tape unit then completes it automatically. The tape control returns the completion pulse 10 microseconds after Rewind is given. The program may then use the same tape control to operate another unit while the previously selected unit is rewinding.

Space - For Backspace and Forward Space commands, the number of records spaced (i.e. skipped over) is equal to C(FA) - C(CA) + 1. To space five records, for example, load 4 into FA and 0 into CA. Besides spacing, Forward Space checks for parity errors and missing characters. Any errors discovered are indicated by status bits 1 and 2 respectively.

Write - Normally the tape control writes the first word of the record 6 milliseconds after tape motion begins. However, if the tape is at load point, TC waits 78 milliseconds to produce the load point gap before starting the first

record. Writing then continues at the rate of one word every 200 microseconds until the current and final addresses become equal. When the address-equal condition occurs, status bit 7 is set, and a sequence break is requested if the sequence break system in on. The address of the last word taken from memory is C(FA) - 1.

The tape continues in motion in order to write the three characters of the final word. If the addresses are changed by reset instructions within 100 microseconds after the address-equal condition occurs, the write operation continues. This process is called "gather write." That is, information contained in scattered areas of memory can be gathered and written on tape as a single continuous record. If the address-equal condition still exists when the third character of the final word is written, the tape control automatically writes 0.020" of blank tape and an EOR character.

If Write is executed with the addresses equal initially, one record gap is written and one of the end-of-record actions is taken. Controlled lengths of blank tape can be written in this manner by using Early Completion and Continue.

Since the tape passes the read head after passing the write,head every character is read and checked 4 milliseconds after it is written. If a parity error or missing character error occurs,it is indicated by the appropriate status bit. Writing a character composed of seven 0s is equivalent to writing blank tape; it produces a missing character error. In PDP-1 Concise Code, such a 0 character can be generated by writing a space or tape feed character with even parity.

Read - Normally the tape control retrieves the first word of a record approximately 10 milliseconds after tape motion begins. However, if the read operation begins at load point,TC must wait approximately 82 milliseconds while the load point gap passes by the read head. After the first character is detected the record is processed at the rate of one word every 200 microseconds. As soon as the third character of each word is read, the system requests high speed channel access to memory in order to deposit the word. HSC access must be granted before the next character is encountered or an HSC Late error occurs. Reading continues until the addresses beoome equal or the end-of-record is encountered.

When the address-equal condition occurs, status bit 7 is set and a sequence break is requested if the sequence break system is on. At this time the address of the last word stored in memory is C(FA) - 1. Tape motion continues and the tape control retrieves the next word from the record. If the program resets the addresses within 100 microseconds after address-equal occurs (i.e. before the system finishes retrieving the next complete word),the normal read operation continues. This process is called "scatter read." That is, information read from a single continuous record can be stored in scattered areas of memory.

If the addresses are not reset, HSC transfers to memory cease,but the tape continues to the end-of-record. If the address reset is delayed beyond the allotted time, the normal read operation restarts,but information retrieved from the tape during the delay is lost. In any event, whether or not the addresses become equal beforehand, Read terminates at the end of the record.

When the end-of-record is encountered,the system returns a completion pulse either at the normal time or earlier, depending upon the previously selected end-of-record action. The completion pulse clears status bit 3 (indicating that the TC is no longer busy) and requests a sequence break if the sequence break system is on. If the end-of-record action specifies that system operation will continue with the same tape unit, tape motion continues at normal speed into the next record. The address of the last word stored in memory is C(CA) - 1. Note that if the total range of memory locations specified by the initiating and reset instructions is greater than the number of words in the record, CA and FA will not be equal when Read ends.

Parity errors or missing character errors detected while reading a record are indicated by the appropriate status bits. The read operation is not affected by the discovery of errors. However, if a character is skipped,all subsequent words transferred to memory are offset by one character, i.e. all characters retrieved from the tape are packed sequentially in memory. If the system is not at the third character of a word when the end-of-record is encountered, HSC access is requested,and the final partial word is deposited in memory, left justified.

Read and Compare (Readcheck) - This operation retrieves information from tape in exactly the same manner as Read. All timing, address reset operations, termination by address-equal or end-of-record conditions, end-of-record actions taken, etc. are exactly the same as for Read. However, in readchecking, each time a complete word is assembled in the data word buffer it is not transferred to the computer. Instead the HSC access is used to retrieve a word from the currently addressed memory location. The two words are then compared bit by bit by producing their exclusive OR function in DWB. If DWB does not contain zero after the comparison, a readcheck error is indicated.

When a readcheck error occurs, status bit 4 is set and the Readcheck ceases, but tape motion continues until the end-of-record is encountered. The address of the last word taken from memory which correctly compared with the corresponding word retrieved from tape is C(CA) - 1.

Reset Instructions:

Magnetic Tape Reset Final Address.....

.....mrf Instruction Code 72ab(0)067

The $C(IO_{2-17})$ replace C(FA); C(IO) remain unchanged. This instruction resets the final address to allow HSC transfers to proceed for gather write, scatter read or gather readcheck. In all other respects the operation specified by the initiating instructions continues. To be effective, mrf must be given within 100 microseconds after the address-equal condition occurs. Usually both reset instructions are used together, in which case both must be given within the 100-microsecond interval.

Bits 5, 9 and 11 of mrf are ignored. However, bits 8 and 10 must be 0. If either of these bits is 1, a maintenance instruction results.

Magnetic Tape Reset Initial Address.....

.....mri Instruction Code 72abxxcx66

The $C(IO_{2-17})$ replace C(CA); C(IO) remain unchanged. Furthermore, bit 10 of the mri instruction (represented by 'c' in the instruction code) replaces $C(CR_{10})$ in the command register. This instruction provides a new initial address to allow further HSC transfers for gather write,

scatter read and gather readcheck. Moreover, by adjusting the state of CR_{10}, the instruction alsoallows the programmer to change the current command from Read to Readcheck, or vice versa.

Since mri clears CR_{10} before transferring bit 10 into it, the program must also provide the appropriate bit if continuation of the original operation is desired. To read or write after the address reset, bit 10 must be 1; to readcheck, it must be 0.

The mri instruction must be given within 100 microseconds after the address-equal condition occurs. Usually both reset instructions are used, in which case both must be given within the 100-microsecond interval.

Examine Instructions:

Magnetic Tape Examine Status...mes Instruction Code 72abxX35

The various status bits replace C(IO). The status bits are unaffected by the instruction. Bits 5 and 8 to 11 of mes are ignored. Following transfer of status information to IO, the program can determine the status of the selected TC and selected TU by checking the states of the 18 IO bits.

The 18 status bits are listed and described in Table 4-1. The left column lists the IO bits; the center column lists the status condition that causes the corresponding IO bit to be set by mes. The status condition may be either a flip-flop or a logic level; flip-flops are indicated by an 'f' in parentheses. The last column lists the meaning of the status condition. Conditions examined are those for the TC selected by mes and the TU specified by the unit address provided by the last muf.

Magnetic Tape Examine Location...mel Instruction Code 72abxX36

The C(CA) replace $C(IO_{2-17})$; $IO_{0,1}$ are cleared. The address of the last HSC access to memory is 1 less than the address transferred into IO by this instruction.

Bits 5 and 8 to 11 of mel are ignored. To examine the current address while a record is being processed, execute two mel instructions and accept the results only if they are identical. This procedure prevents the program from accepting an erroneous address should the transfer occur while CA is in a dynamic state.

Maintenance Instructions:

Two special instructions are available for maintenance and diagnostic operations. These instructions bypass all interlocks in the tape control. Both instructions use the same second op

code (67) as mrf,and they therefore reset the final address according to C(IO) at the same time that they perform their maintenance functions.

Initiate HSC Request.....inr Instruction Code 72ab(0)267

This instruction sets flip-flop HSC REQ,causing TC to request high speed channel access. Use made of such access depends upon the tape operation currently being performed.

Clear Command Register.....ccr Instruction Code 72ab(1)067

This instruction halts the tape by clearing the command register. This procedure is the only way, under program control, to halt tape motion while a record is being processed. The ccr instruction is particularly useful for adjusting the transport start-stop characteristics.

4-5 TYPE 52 SYSTEM LOGIC

Figure 4-4 is a detailed block diagram of the Type 52 Automatic Tape Control. This figure shows the registers and many of the logic nets in the Type 52 as well as the connections from the tape control to the computer and the tape units. The number of physical lines required for each connection is indicated by a number written on the line in the figure. For example, transfer of information from data word buffer to memory buffer requires 18 lines. A pulse that gates information into a register (usually an iot command pulse) is shown as an arrow drawn across the transfer line into the register. The name of the pulse, or pulses, is written at the base of the arrow. Solid lines represent data transfers; dotted lines represent control.

Connections to the computer are shown at the left. Information is provided to the tape system from MB, IO and AC. The transfer pulses for such information are provided by in-out control in the Type 52. The computer, however, provides gating pulses for information transferred from the Type 52. High speed channel control governs transfer of addresses and data to MA and MB; in-out transfer control governs transfer of status or location data into IO in the two examine instructions. Other connections between computer and tape system are for high speed channel access and sequence break request signals, and for iot command pulses.

Connections from the tape control to a single tape unit are shown at the top of Figure 4-4. All tape units are actually connected in parallel across a single TC bus. A block diagram of the tape unit is shown in Figure 4-5. Paragraphs a to e below describe the five major portions of the tape control shown in Figure 4-4; paragraph f describes the tape unit as shown in Figure 4-5.

TABLE 4-1 TYPE 52 TAPE SYSTEM STATUS

IO Bit	Status Condition	Meaning
0	ERROR	OR function of those conditions marked with an asterisk (*).
1*	PARITY ERROR (f)	At least one parity error has occurred since the last mic.
2*	CHAR SKPD (f)	At least one missing character error has occurred since the last mic.
3*	TC BUSY (f)	Tape control is in operation. When the TC is busy no initiating instructions are accepted. To synchronize the completion of tape operations with computer timing, any state change in TC BUSY is transferred to TC BUSY SYNC at TP_4. Command pulses for initiating instructions muf and mic are gated by $\overline{\text{TC BUSY SYNC}}$. When a tape operation is initiated, mic sets TC BUSY. When the end-of-record is encountered during the operation, the completion pulse (RECORD DONE) clears TC BUSY. If the computer includes the multi-channel sequence break system, the completion pulse also requests a break. However, for use with the single channel sequence break system, the assertion of $\overline{\text{TC BUSY}}$ requests the break.
4*	RCK ERROR (f)	A readcheck error has occurred since the last mic.
5*	ILLEGAL (f)	The last mic specified an illegal command. An illegal command is a write command that occurs when there is no write enable ring in the reel, or any command code that does not correspond to a command.
6*	HSC LATE (f)	The computer failed to respond to a high speed channel request before the next character transfer was ready.
7	ADDRESS EQUAL	C(CA) = C(FA), i.e. the current address has been counted up to the final address. With a single channel sequence break system this condition requests a break; with a multi-

TABLE 4-1 TYPE 52 TAPE SYSTEM STATUS (continued)

IO Bit	Status Condition	Meaning
		channel system the level is used to develop a pulse which requests a break only if there has been no readcheck error.
8	READY	TU is ready for on-line operation.
9	AUTO	TU is on-line and transport power is on.
10	REWIND	TU is rewinding.
11	WRITE INHIBIT	TU is in "file protect," i.e. there is no write enable ring in the reel.
12	LOAD POINT	Beginning-of-tape reflective strip is at beginning-of-tape sensor.
13	FULL REEL	Takeup reel contains less than 100 feet of tape.
14	LOW REEL	Supply reel contains less than 100 feet of tape.
15*	END POINT	End-of-tape reflective strip is at or beyond end-of-tape sensor.
16	WILL CONT (f)	When the end-of-record is encountered an early completion pulse will be returned.
17	WILL CONT SAME (f)	The previous muf specified that when the end-of-record is encountered operations will continue on the same tape unit. Note: This flip-flop is cleared by the 1/2 UP SPEED pulse 2 milliseconds after mic and it does not therefore usually give meaningful status information. However, if both WILL CONT and WILL CONT SAME are set by muf, 1/2 UP SPEED sets the SAME UNIT flip-flop. When the end-of-record is encountered an early completion pulse is returned; SAME UNIT causes tape motion to continue into the next record and prevents the following muf from selecting a new TU.

a COMMAND LOGIC - The command logic includes a 4-bit command register CR and a pair of decoders (center, Figure 4-4). Two instructions affect CR. At the initiation of tape operations, mic provides a tape command from bits 8 to 11 of the instruction word (MB_{8-11}). Furthermore, mri may change CR_{10} to switch from reading to readchecking or vice versa at the same time that it resets the initial address. CR_{8-10} are decoded to provide command signals both to TU and to in-out and format control. The state of CR_{11} defines the parity mode, i.e. whether the current tape operation shall use even or odd parity.

b ADDRESS LOGIC - Instruction muf provides the tape control with a tape unit address and a final memory address. The 3-bit unit address is transferred from AC_{15-17} to UA (upper left, Figure 4-4). From UA the TC decodes the address to select one out of eight tape units. The 16-bit final address is transferred from IO to FA (bottom). This address is 1 greater than the address of the final location to which HSC access will be made during the coming tape operation. The four most significant bits of FA specify a memory module while the twelve least significant bits address a memory location within that module.

After muf provides a final address, mic places the tape system in operation and provides an initial memory address. When tape operation begins, this initial address becomes the current address. At the beginning of each HSC cycle, the contents of CA are transferred through the HSC address mixer to the memory address register. Following the transfer, CA is incremented by 1 so that the next HSC access is made to the next consecutive memory location. The computer may examine the location of current tape operations at any time by transferring CA into IO.

The outputs of CA and FA are applied to an equality net. When CA is counted up to FA, the equality net generates an ADDRESS EQUAL signal which terminates HSC transfers and requests a sequence break. If the program uses mri and mrf to reset the addresses within the allotted time (100 microseconds), further HSC access may be requested and the operation continues. By using this procedure the program can cause information to be gathered from or scattered to noncontiguous areas of memory.

c DATA TRANSFER REGISTERS - The three data transfer registers are shown in the upper right of Figure 4-4. In writing, each HSC transfer provides a full 18-bit word from MB to DWB. For transfer to tape, the word is divided into three 6-bit characters, each of which is

provided to the write buffer from DWB_{0-5}. Although the character provided to DWB is six bits, the character transferred into WB is seven bits. Outputs of DWB_{0-5} are applied to a parity net which generates an appropriate parity bit according to the parity mode specified by CR_{11}. The WRITE signal from format control then transfers the parity bit into WB_p at the same time that it transfers the six data bits into WB_{0-5}. This transfer is a complement transfer; that is, if a given DWB bit is 1, WRITE complements the corresponding WB bit. This causes the tape unit write head to change the direction of magnetization in the corresponding tape channel.

As each character is encountered on the tape in reading, the transfer of the first bit into the 7-bit read buffer is detected by an OR gate. After the first character is detected format control compensates for tape skew by allowing 25 microseconds for RB to receive the entire character. During this time a parity net also checks the parity of the character in RB against the parity mode specified by CR_{11}. At the end of the 25 microsecond interval, format control generates the READ STROBE, which transfers the six data bits of the character into the appropriate section of DWB. If the parity of the character is incorrect, the strobe also sets the parity error status flip-flop in in-out control. After a complete word is assembled in DWB from three consecutive characters, it is transferred to memory through a high speed channel.

The readcheck operation uses RB and DWB exactly as in reading. However, after a complete word is assembled in DWB, instead of transferring the word to memory, in-out control compares the word with the contents of the currently addressed memory location by using the HSC access to produce the exclusive OR function of the two words in DWB. If, after the comparison, DWB does not contain zero, the readcheck error status flip-flop is set.

The read buffer and its parity net are also used in Write and Forward Space to check for parity errors and missing characters. In either case, however, there are no transfers into DWB.

d IN-OUT CONTROL - In-out control handles all signal and data transfers between computer and tape control. The computer supplies eight iot command pulses (two for each of four instructions) to in-out control. Initiating pulses are gated within TC so that the program cannot interrupt the system when it is in operation. Command pulses for muf are gated by the 0 state of TC BUSY while those of mic are gated by the 1 state of TU OK. The latter flip-flop is set when the tape control is not busy and the tape unit selected by the previous

muf is ready for operation. Reset command pulses are, of course, not gated because these must occur while the system is in operation.

In-out control also includes the two continue flip-flops (shown separately in Figure 4-4). These two flip-flops are regulated by bits 10 and 11 of muf to specify the end-of-record action. For early completion and stop, in-out control returns the completion pulse 10 milliseconds early. If early completion and continue is specified, the in-out control flip-flop SAME UNIT is set following the mic instruction. When the end-of-record is encountered, the 1 state of SAME UNIT prevents the next muf from selecting a new unit,and it also replaces the TU READY condition in TU OK in order to gate the mic command pulses into the system.

Whenever format control has read or is ready to write another word, in-out control sends an HSC request to the computer. When the request is granted the computer returns an HSC transfer pulse causing in-out control to develop the necessary transfer pulses within the TC. If TC is performing a Read Command,the READING signal causes the computer to accept information from the tape system during HSC access.

In-out control requests sequence breaks whenever the addresses become equal or the end-of-record is encountered. With the multichannel sequence break system,the request signals are pulses: the completion pulse RECORD DONE, and the ADDRESS EQUAL pulse (which in-out control develops from the ADDRESS EQUAL level). With the single channel system, requests are made by levels: the ADDRESS EQUAL status level and $\overline{\text{TC BUSY}}$ (this flip-flop is cleared by the completion pulse). In-out control also provides tape system status information which the computer can examine at any time by transferring the status bits into the in-out register. Status levels for the tape control are provided by flip-flops included in in-out control. Tape unit status levels are transmitted from the selected TU to the computer through in-out control.

e FORMAT CONTROL - This section of TC includes the logic that governs the writing of information on the tape in correct format and responds properly to the same format in retrieving information from the tape. A 2-bit character counter (flip-flops A and B) continually cycles through a 3 count to control the conversion of words into characters and the assembly of characters into complete words.

Each time DWB receives a word from the computer, format control divides the word into three characters and produces the WRITE signals that transfer the characters to tape at the correct rate of 15,000 characters per second. All characters are made available to WB from DWB_{0-5} by successive 6-place left shifts in DWB. When the third character has been written, format control clears DWB and signals in-out control to request HSC access to memory for another word. When the addresses become equal and are not reset within the allotted time, format control writes 0.020 inches of blank tape and then writes the EOR character.

When reading the tape, format control responds to the detection of each character and sets up the time intervals that compensate for tape skew and detect missing characters and the end-of-record. When the tape is read as part of a Read or Readcheck command, format control generates a strobe that is gated by levels from the character counter to assemble three consecutive characters into a full word. The successive character counter states gate each character into the appropriate section of DWB. After retrieving an entire word, HSC access to memory is requested to deposit the word or retrieve a word to be compared with it. In space commands no information is transferred to DWB, but format control detects EOR gaps and counts the spaced records by incrementing the current address register.

When the tape operation is completed, format control waits until the correct spot on the tape is at the read head — the time delay depends upon the direction of tape motion and whether the system is reading or writing — and then clears the command register, stopping the tape.

f TAPE UNIT CONTROL - Figure 4-5 is a block diagram of a typical tape unit connected to the TC bus. The hardware included in the tape transport and drive electronics is represented by the vertical column of blocks at the right of the unit. The rest of the equipment is included in the DEC-designed Type 50 Local Control and Manual Control Panel.

The TC bus includes five types of signal lines. In those instances where the number of lines of a given type is different for the Type 52 System than for the Type 51 System, the automatic system requirements are indicated by "52" in parentheses. The tape control selects the TU by enabling one of the eight selection lines. Even though all eight selection lines are connected to all eight tape units only, that unit (or units) whose unit selector is set to the appropriate address goes into operation. The output of the selector places the unit in operation by enabling the other sections of the Type 50 Logic.

Signals from the command register govern operation of the tape transport through the motion logic. The selection and command lines are shown going to TU through the manual control panel. To operate the unit off-line, the operator provides duplicate selection and command signals from the panel. The remaining control signals are status levels provided to TC from the tape transport. The status conditions are also displayed in indicators on the tape unit.

The remaining lines of the TC bus carry data signals. The outputs of the write buffer are applied to write drivers which in turn provide current to the write head. The write drivers are enabled only when the unit is on-line and the system is performing a Write command. Signals detected by the read head are transmitted to the read buffer through read amplifiers and rectifying slicers. The read circuits of the selected unit are enabled at all times except when the tape is rewinding.

4-6 TYPE 51 TAPE INSTRUCTIONS

With the installation of a Type 51 Programmed Tape System, five in-out transfer instructions are added to the PDP-1 repertoire. All of these instructions are executed in a single computer memory cycle of 5 microseconds. With these instructions the program can place the tape unit into appropriate operation but cannot begin any automatic sequence of operations within the tape control. The only automatic events in the tape control involve parity operations or data transfers between tape control and tape unit.

The Type 51 Control includes a parity net which generates a parity bit in writing and checks parity in reading; a 6-microsecond delay which allows time for parity bit generation before writing a character transferred to the character buffer and a set of detectors that respond to any signals from the tape so long as the read circuits are enabled. All transfers of data between computer and tape control and all timing to provide the correct transfer rates, produce appropriate gaps on the tape and check for missing characters must be provided by the program. Furthermore the in-out register must provide information to the tape system one character at a time and must accept information one character at a time from the character buffer.

Magnetic Tape Select Mode.....msm Instruction Code 72XX73

The $C(IO_{10-17})$ replace the contents of the tape control command register. The tape control selects tape unit 1, 2 or 3 according to the 2-bit number contained in IO bits 16 and 17 (00 is no selection). The other six bits determine the operating mode of the selected unit as follows:

IO bit	If 0	If 1
10	Do not operate	Operate
11	Do not rewind	Rewind if IO_{12} is 1
12	Forward	Reverse
13	Read	Write
14	Odd parity	Even parity
15	Low speed	High speed

The speed control (bit 15) is not at present used but is included to make the system capable of controlling a two-speed tape transport. Note that a 1 in bit 11 is not sufficient to rewind tape. In order to rewind, the program must specify both rewind and reverse.

Magnetic Tape Clear Buffers.....mcb Instruction Code 72XX70

Clears both character buffer and write buffer. To read or write tape, the program must execute mcb immediately after executing an msm instruction. The mcb clears the write buffer in order to establish a known initial state before writing, and clears the character buffer to prepare it for receiving information when reading. The mcb instruction may also be used to produce an even longitudinal parity end-of-record character when writing IBM format.

Magnetic Tape Write Character.....mwc Instruction Code 72XX71

The $C(IO_{0-5})$ replace $C(CB_{0-5})$. Following the transfer the parity net generates a parity bit according to the configuration of the six data bits in CB and the parity mode specified by the previous msm. After a delay of 6 microseconds TC writes the 7-bit character on tape.

Magnetic Tape Read Character.....mrc Instruction Code 72XX72

This instruction transfers $C(CB_{0-5})$ to IO_{12-17}, sets PF_4 if the character contained in CB has incorrect parity, and clears both CB and PF_2. This instruction does not include a prior clear of IO before the 1 transfer of C(CB) into it. Therefore the program must assure that the six least significant bits of the in-out register are clear before reading a character.

When the first bit of a tape character is detected, the tape control sets program flag 2. Upon recognizing that PF_2 has been set, the program must compensate for tape skew by waiting an appropriate time for all bits in the character to be received by CB. During this time the parity net also checks the parity of the 7-bit character against the parity mode specified by the previous msm. Then at the same time that mrc transfers the six data bits from CB to IO_{12-17}, it

also sets PF_4 if the parity of the character is in error. Following the transfer, mrc clears both CB and PF_2 to prepare them for detection and retrieval of the next tape character.

Figure 4-6 is a timing diagram for programmed read operations. Note that the time between character detections may vary considerably, depending on tape skew. If the first 1 bit in a character is in the last bit position encountered, and the earliest bit position in the next character contains a 1, then the inter-character gap is only 15 microseconds. Since the program waits 25 microseconds after character detection to ensure that the entire character is retrieved, the program has only 15 microseconds to transfer the character to IO and sense PF_2 for the next character.

Magnetic Tape Check Status.....mcs Instruction Code 72XX34

Tape unit status information replaces $C(IO_{0-7})$. The status conditions represented by the IO bits are as follows:

IO bit	If 0
0	Ready
1	Rewind
2	Write Inhibit
3	Load Point
4	Full Reel
5	Low Reel
6	End Point
7	Auto

The above status levels have the same meaning as the tape unit status levels listed in Table 4-1 for the Type 52 System. Note, however, that the existence of a given condition is implied by a 0 in the corresponding IO bit. This is because the status signals from TU are available to the input mixer in the opposite polarities from those in the Type 52 System. Thus the existence of a given status condition is represented by a 1 IO bit when using the Type 52 Control, but by a 0 when using the Type 51. The setting of an IO bit by mcs implies that the corresponding status condition is negated.

4-7 TYPE 51 SYSTEM LOGIC

Figure 4-7 shows the hardware included in the Programmed Tape Control Type 51. The iot control section of PDP-1 is at the left. A typical tape unit connected to the control through the TC

bus is at the top. Up to three tape units may be connected in parallel to the TC bus. The number of physical lines required for each connection is indicated by a number written on the line in the figure. The iot instructions that gate system transfers are shown beside arrows drawn across the transfer lines.

The iot command pulses are applied directly to the input gating of the various registers and program flags used in operating the programmed tape system. This is necessary because the Type 51 contains no central control portion. The instruction msm selects the tape unit and its operating mode by transferring eight control bits from IO_{10-17} to the command register. In most cases the command signals to TU are provided directly from the first five bits of this register. The only control element external to the register is a simple AND gate which assures that TU will rewind only if the program specifies both rewind and reverse. The last two bits of the command register serve as a unit address register. These two bits are decoded to select a tape unit for operation by the tape control. The remaining command register bit specifies the parity mode for use within the tape control.

In write operations, instruction mwc transfers single characters from IO_{0-5} to the 6-bit data portion of the 7-bit character buffer. Following the transfer, the parity net generates a parity bit for the character according to the configuration of CB_{0-5} and the parity mode specified by the command register. Six microseconds after the transfer into CB, the 7-bit character is written on tape by complementing any write buffer bit that corresponds to a 1 in the character. Bits CB_{0-5} condition WB_{0-5}; the parity bit conditions WB_p.

In a read operation, a change in magnetization in any tape channel sets the corresponding CB bit. The outputs of the character buffer are applied to an OR gate which recognizes detection of the first 1 bit in a character and signals the computer by setting PF_2. The program must then compensate for tape skew by allowing sufficient time for CB to receive all bits of the character. After the entire character is received, mrc transfers the six data bits from CB_{0-5} to IO_{12-17}. At the same time mrc also sets PF_4 if the parity net error output indicates that the parity of the 7-bit character does not correspond to the specified parity mode. Instruction mrc also clears PF_2 and CB to prepare the system to receive the next tape character.

The Type 51 Tape Control does not generate any status information for examination by the program. However, the program may examine the status of the selected tape unit. The eight TU status bits are transferred into IO_{0-7} by mcs.

The logical organization of the tape unit itself is identical to that for units in the Type 52 System. Figure 4-5 is a block diagram of the tape unit and is described in paragraph 4-5f. The only differences between units in the two systems are in the number of selection and command lines provided from the tape control. Since the Type 51 System includes only three units, only three selection lines are necessary instead of eight. However, two additional command lines help to achieve the hardware economy provided by the Type 51. Since the character buffer doubles as a read buffer, the system cannot read as it writes. Therefore, the TU read circuits respond to tape signals only when enabled by the command register. Further, since the tape command is not decoded, the command register specifies certain tape operations even when clear (for example, the data mode flip-flop in the command register must specify either read or write). The command register therefore includes an operate flip-flop which must be set in order to place the selected tape unit in operation. This arrangement allows the program to select a tape unit to examine status without placing it in operation.

CHAPTER 5

OPERATING PROCEDURES

5-1 GENERAL

This chapter provides the operator with information needed to operate the PDP-1 Magnetic Tape System. Descriptions of all controls and indicators are included as well as instructions for tape loading and manual control of the tape transport. An operator's checklist is also provided for operating the system under normal conditions.

5-2 TAPE UNIT SWITCHES AND INDICATORS

All switches and indicators necessary for operation of the tape unit are located on the manual control panel. The unit also includes a gain, slice and test point panel and several miscellaneous controls. These, however, are used primarily for maintenance.

a MANUAL CONTROL PANEL - This panel (Figure 5-1) includes four switches with three associated indicators and eight independent lights that indicate various tape unit conditions when lit.

Switches:

TRANSPORT POWER

This switch has two stable positions, OFF and REMOTE, and a momentary contact position, ON. When OFF, power cannot be applied to the transport. In REMOTE, transport turn-on is governed through the 822 power control (c below). Pushing the switch to the momentary ON position turns on the transport; it then stays on even if the switch is returned to REMOTE. However, under no circumstances can power be applied to the transport (by either the TRANSPORT POWER switch or the 822 power control) unless the transport interlock is closed (paragraph 5-5).

The indicator above TRANSPORT POWER does not indicate a switch position, but instead lights whenever power is actually applied to the transport.

Mode

Two-position switch with associated AUTO and MAN indicators. In AUTO the tape unit is on line and all operations are initiated from the tape control. In MAN the unit is off line; reading and writing are disabled and transport motion signals are generated from the rewind and direction switches on the control panel.

UNIT

Eight-position thumbwheel which determines the address of the tape unit. For example, if the tape control addresses unit 5, only that unit whose UNIT thumbwheel is set to 5 responds. If desired, the operator can cause the tape control to write on two tapes simultaneously by giving both units the same address.

Manual Rewind

Three-position momentary contact switch with a stable center off position. Pushing this switch to START RWD sets the rewind flip-flop, causing the tape to run in reverse at high speed. Pushing the switch to STOP RWD clears the rewind flip-flop, halting the tape.

Manual Direction

Three-position momentary contact switch with a center off position. Forward tape motion is produced while this switch is held in FORWARD; reverse motion while held in REVERSE.

Indicators:

SELECTED

With the Type 52 Control, this light indicates that the tape unit has been selected. However, with the Type 51 Control, the light indicates that the tape unit has been selected and commanded to operate.

READY

Indicates that the unit is ready for on-line operation. This requires that the unit be in AUTO mode, that transport power be on and that the tape be stationary.

WRITE LOCK

Indicates that the supply reel does not contain a write enable ring. Leaving the ring out of the reel protects the information contained on the tape.

REWIND

Indicates that the tape is rewinding.

LOAD POINT

Indicates that the beginning-of-tape reflective strip is at the photosensor.

FULL REEL

Indicates that less than 100 feet of tape are on the takeup reel.

LOW REEL

Indicates that less than 100 feet are left on the supply reel.

END POINT

Indicates that the end-of-tape reflective strip is at or has passed the photosensor.

b GAIN, SLICE AND TEST POINT PANEL - The controls and test points on this panel (Figure 5-2) are for the convenience of maintenance personnel.

Switches

HIGH GAIN

Two-position toggle switch which controls the gain of the Type 1549 Differential Amplifiers. Up position selects high gain and lights the associated indicator. If the tape unit is equipped with Type 1536 Differential Amplifiers in place of the Type 1549s, this switch is not used.

SLICE CONTROL

Potentiometer and associated volt meter. This control varies the threshold of the Type 1542 Rectifying Slicers for marginal check purposes. Normal setting is 5 volts; range is 0 to 10 volts.

Test Points:

SELECTED

Signal to the Type 50 Logic through the UNIT selector.

FORWARD

Forward motion signal to the drive electronics.

REVERSE

Reverse motion signal to the drive electronics.

CLEAR

AUTO CLEAR signal in the transport logic. In AUTO, this is CLEAR TU from the tape control; in MAN, this is STOP RWD.

WRITE SIGNALS: WR ENABLE, 1, 2, 3, 4, 5, 6, PARITY

Signals associated with the NRZ writers. WR ENABLE is the enabling signal to the writers. The others are the writer outputs.

READ SIGNALS: READ ENABLE, 1, 2, 3, 4, 5, 6, PARITY

Signals associated with the tape sensing circuits. READ ENABLE is the enabling signal to the rectifying slicers. The others are the read outputs from the differential amplifiers.

c MISCELLANEOUS CONTROLS - Located in the lower left of the bus socket panel is a tape control selector (Figure 3-1). This two-position toggle switch allows the operator to use the tape unit with either TAPE CONTROL 51 or TAPE CONTROL 52. However, in unit 1 of the Type 51 System (containing the Type 51 Logic) the switch is absent and the Type 51 Connections are wired in.

Located on the 822 (811B) power control at the rear of the bay (Figure 2-4), are a pair of ganged ac circuit breakers and a power mode switch. This switch affects the transport only if TRANSPORT POWER is in REMOTE and the transport interlock is closed. When the 822 is in REMOTE mode, the tape unit (including the Type 50 Logic and the transport) goes on and off with the Tape Control (Type 52) or the Computer (Type 51). If the remote input is off, switching the 822 to LOCAL provides power to the entire unit. However, if the transport is turned off while the tape unit is on, only the TRANSPORT POWER switch can restore power (a above).

5-3 TAPE CONTROL SWITCHES AND INDICATORS

The Type 52 Control includes an indicator panel located on the front of the bay and several marginal check and power controls located on the plenum door (Figure 2-3). The Type 51 Tape Control, on the other hand, includes only those switches associated with its 811 power control located on the unit 1 plenum door (Figure 2-4).

a INDICATOR PANEL - The Type 52 Indicator Panel (Figure 5-3) includes a single switch, POWER. This two-position toggle switch functions in conjunction with the 822 power control (b below). AC voltage can be applied through the power control to the power supplies only if the POWER switch is on (up). The associated indicator is lit when the Type 52 Logic is on.

The lights on the indicator panel may be divided into three groups. The tape control registers occupy the left half and the upper right corner of the panel. Between the two sections of register lights are two columns of status indicators; tape unit indicators in the right columns; tape control indicators in the left. The latter group also includes the set of three CONTINUE lights located directly above the POWER switch. The tape unit indicators are equivalent to the status indicators on the manual control panel of the selected tape unit. WRITE INHIBIT is equivalent to WRITE LOCK. The other tape unit indicators have the same names on both panels.

Registers:

DATA WORD BUFFER (DWB)

In writing, this 18-bit register receives full words from computer memory over a high speed channel. Two 6-place left shifts render the data available sequentially from DWB_{0-5} to the write buffer as three 6-bit characters. In reading, three consecutive characters received from the tape by the read buffer are assembled into an 18-bit word in DWB. The word is then transferred to memory through a high speed channel. In readchecking, the word assembled in DWB from the tape is compared with a word from memory by first generating the exclusive OR function of the two words in DWB, then sensing for zero contents.

FINAL FIELD & ADDRESS (FA)

This 16-bit register specifies a memory address 1 greater than the final address to which access will be made for the current tape operation. The first 4 bits specify the field (module); the last 12 bits address a single memory location within the specified field. In spacing operations, FA does not contain an address but instead contains a number that is 1 less than the number of records to be spaced.

CURRENT FIELD & ADDRESS (CA)

This 16-bit register specifies the memory address to which the next access will be made

during the current tape operation. The first 4 bits specify the field (module); the last 12 bits address a location within the specified field. Initially, CA receives from the computer the address for the first memory access. After each HSC request is granted, C(CA) are incremented by 1. When C(CA) become equal to C(FA), the tape operation is terminated unless the program provides reset instructions. In spacing operations, CA is initially 0 and is used to count the records spaced.

UNIT (UA)

This 3-bit register holds the address of the selected tape unit.

COMMAND (CR)

This 4-bit register holds the tape command provided by the mic instruction.

Status Indicators:

TC BUSY

Indicates that the tape control has been placed in operation by an mic instruction and has not yet reached the end of the record.

PARITY

Indicates that a parity error has been detected on the tape since the last mic.

CHAR SKIP

Indicates that at least once since the last mic the system has failed to retrieve a character from the tape when one was expected.

READ CHECK

Indicates that since the last mic at least one word retrieved from tape has failed to compare correctly with the contents of the specified memory location.

ILLEGAL

Indicates that the preceding mic specified an illegal command.

HSC LATE

Indicates that since the last mic the computer has failed at least once to respond to an HSC request within the allotted time.

HSC REQ

Indicates that high speed channel access to memory has been requested but not yet granted.

CONTINUE (WILL CONT, WILL CONT SAME, SAME UNIT)

From left to right, these three indicators correspond to the will continue, will continue same, and same unit flip-flops. The left light indicates that the last muf instruction specified that tape operations will continue after completion of the current operation. In this case the tape control returns an early completion pulse. The center light indicates that the last muf specified that tape operations will continue on the same unit after the current operation is completed. After WILL CONT SAME is set, it is usually cleared too quickly to turn on the light. However, if both WILL CONT and WILL CONT SAME are set by muf, an initiating signal generated by the subsequent mic clears WILL CONT SAME at the same time that SAME UNIT is set. Thus the right light indicates that the last muf specified that tape operations will continue on the same unit after the current operation is completed. In this case the unit does not stop at the end of the current operation and the next muf cannot select a new unit.

b POWER CONTROLS - Both the Type 52 and the Type 51 include an 811 power control. For the Type 52, the 811 is located at the bottom of the bay 1 plenum door (Figure 2-3). For the Type 51, it is located at the top of the unit 1 plenum door (Figure 2-4). The 811 control includes a ganged pair of AC circuit breakers and a power mode switch. These are the only switches governing Type 51 power. In the Type 52, however, power can be provided to the system through the 811 only if the indicator panel POWER switch is on. If the 811 is in REMOTE mode, the tape control goes on and off with the computer. Switching to LOCAL turns on the Type 52 Tape Control independently of the computer. For Type 51 off-line operation, however, the tape control cannot be turned on independently of tape unit 1. Both the 811 and the unit 1 822 must be switched to LOCAL. Both the Type 51 Logic and the tape unit then receive power.

The Type 52 Tape Control also includes a variable Power Supply Type 734 which furnishes marginal check voltages to the logic circuits. This supply, located at the top of the plenum door, provides voltages that can vary from 0 to +20 vdc. To marginal check the +10 A and B lines to the logic mounting panels, output values between 0 and 20 volts are controlled by the MARGINAL CHECK variac and monitored on an associated voltmeter (Figure 5-4). Line

voltage for the Type 734 is supplied directly from the 811 with no intervening switch. Therefore the marginal check power supply is on whenever the tape control is on.

Plug-in pins to which marginal check voltage is applied are selected by the toggle switches at the left of each mounting panel. Marginal voltage is applied to the A line of any panel by pushing up the top toggle switch on that panel, and to the B line by pushing up the center switch. The bottom switch is not used. Note that all lines not being marginal checked receive their normal voltages automatically.

5-4 TAPE LOADING

The front view of the tape transport is shown in Figure 1-1 of the Potter Handbook. In the PDP-1 system, the upper tape reel is the supply reel; the lower is the takeup reel. Potter Figure 1-5 shows a more detailed view of the drive plate assembly — the vacuum chamber, the EOT sensor and the read-write head. In the figure the smaller cover at the right is the head cover; the larger, at the left, is the buffer cover. All terminology used in the following instructions is listed with these two figures.

1. Turn TRANSPORT POWER switch to OFF.
2. Take the unit off line by turning the mode switch to MAN.
3. Rotate tape load handle 180° clockwise. This brings the tension arms inside the bridge rollers.
4. Lock low tape sensors by pushing them against the stop blocks.
5. Mount an empty reel on the lower hub.
6. Mount a full reel of tape on the upper hub so that the free end of the tape hangs down from the right side of the reel, shiny side out. The groove for the write enable lockout ring should be on the back of the reel. If the tape contains data that must be protected, make certain there is no write enable ring in the reel.
7. Unwind about 6 feet of tape from the reel.
8. Open buffer cover and head cover.
9. Thread tape as shown in Figure 5-5.

10. Close buffer cover but not head cover.

11. Wind one turn of tape around the takeup reel in a clockwise direction.

CAUTION

Do not slip free end of tape into slot in reel core and do not secure the free end to the reel in any manner.

12. Hold free end of tape to core of takeup reel with finger.

13. Turn supply reel until tape slack is taken up.

14. Wind about four turns of tape on takeup reel by rotating both reels manually. Make sure the tape is not slipping on the takeup reel.

15. Unwind about 2 feet of tape from each reel to provide slack for the tension arms.

16. Release tape load handle by rotating 180° counterclockwise. The tension arms swing toward normal position, taking up tape slack.

17. Inspect to see that tape is properly positioned within all guiding rollers and the guide trough.

18. Close head cover.

19. Release low tape sensors.

20. Make sure the tape is seated properly by running the transport from the manual control panel (paragraph 5-5).

5-5 MANUAL CONTROL

After loading a tape, the operator should check out the tape unit from the manual control panel to make sure that the tape is seated correctly and that the transport is running properly. Apply power to the transport by turning ON the TRANSPORT POWER switch. It is not necessary to put the 822 power control into LOCAL. It can be left in REMOTE provided the tape unit is off line (i.e. the mode switch is in MAN). However, transport power cannot go on unless the transport interlock is closed.

The interlock opens whenever the tape load handle is turned to the load position bringing the tension arms inside the bridge rollers. It also opens whenever the tension arms swing all the way

out to the tension arm bumpers. The former condition prevents the transport from being turned on while tape is being loaded; the latter turns off the transport if the tape should break or run off the reel.

With power on and the unit off line, check the effect of the direction and rewind switches at the right of the control panel. These switches function only when the unit is off line. Check the forward motion of the tape by holding the direction switch in FORWARD. Wind enough tape on the takeup reel so that both reverse and rewind can be checked. Run the tape in reverse for a short distance. Then push the rewind switch to START RWD and let the rewind go to the beginning of the tape. The tape should halt when the LOAD POINT indicator goes on.

5-6 OPERATOR'S CHECKLIST

After loading a tape and checking tape motion, the unit should be readied for on-line operation. Check the following:

1. If computer power is off, turn TRANSPORT POWER to REMOTE.
2. If computer power is on, is the transport also on? If not, push TRANSPORT POWER to ON, then return it to REMOTE. The indicator at the upper left should light.
3. Is the tape unit on-line? The AUTO indicator should be lit.
4. Is the READY indicator lit? The LOAD POINT and FULL REEL indicators should also be on.
5. If the tape contains data that must not be destroyed, make sure the write enable ring is not in the reel. The WRITE LOCK indicator should be lit.
6. Is the UNIT selector set to the correct address? If the computer is to read the tape, make sure no other unit is set to the same address.

CHAPTER 6

TAPE SYSTEM LOGIC

6-1 GENERAL

This chapter provides a detailed logical description of the Type 51 and 52 Magnetic Tape Systems. Included are descriptions of in-out transfer control for magnetic tape, the control units in the Automatic and Programmed Systems Types 52 and 51 respectively and the local tape control or read-write electronics which is provided in each Type 50 Tape Unit.

The tape system logic is shown in six flow charts (Figures 6-1 to 6-6) and thirteen logic drawings (Figures 6-7 to 6-19). The organization of the flow charts and the system operations depicted by them are described in paragraph 6-2. For information on the symbology, use and organization of the logic drawings, see paragraphs 3-3c, d, and 3-16 in the basic PDP-1 Maintenance Manual.

Figures 6-7 and 6-8 show equipment that must be added to the in-out transfer control section of the computer in order to operate the two types of magnetic tape control units. Figure 6-9 shows the signal connections between computer and tape control units. The equipment shown in these three figures is described in paragraph 6-3.

Figures 6-10 to 6-19 show system equipment that is external to the computer. This includes the logic in the tape control units and in the tape units. The Automatic Control Unit Type 52 is shown in Figures 6-10 to 6-16 and described in paragraphs 6-4 to 6-10. Usually, each section of the logic is contained completely within a single mounting panel. Thus, except for lack of space for an extra module or two, each figure shows the logic for one mounting panel (the panel letter is written in the upper right corner of the drawing). Each figure also includes the indicator drivers associated with the logic, a module layout of the mounting panel and a block diagram of the logic.

The Programmed Tape Control Unit Type 51 is shown in Figure 6-17 and described in paragraph 6-11. The local control (read-write electronics) which is included within each Type 50 Tape Unit, is shown in Figures 6-18 and 6-19 and described in paragraph 6-12.

6-2 SYSTEM OPERATIONS

All operations that can be performed by the tape system are shown in a series of flow charts, Figures 6-1 to 6-6, and timing charts, Tables 6-1 to 6-5 (the tables are grouped at the end of this chapter). For general information on flow chart conventions, see paragraph 3-8 in the PDP-1 manual. The flow charts for the tape system, however, are not organized like memory cycle flow charts. Instead, time intervals between events in a sequence are produced by delays, or by the time required to wait for the receipt of information or to wait for a synchronizing clock. Delays between events are shown by breaks in the line of flow with the length of the delay written in the break.

a TYPE 52 SYSTEM - Table 6-1 lists the general functions that clear the automatic tape system and synchronize the Type 52 Control to the computer. Table 6-2 lists those operations performed directly by the iot command pulses. Operations in the examine instructions take place within the computer; all other operations occur within the tape control. Each instruction includes a pair of command pulses. The operations produced by all instructions except mic are complete in the table. Instruction mic initiates tape control operation which then continues automatically. The automatic operations are shown in the flow chart for the initiation and termination of tape commands (Figure 6-1).

In all flow charts, the pulse that produces a given set of events is written at the left, while the events themselves are written in rectangles in the line of flow. Beside each pulse name the terminal at which the pulse first appears is written in parentheses. In some cases terminal designations are also given for logic levels and pulse events that occur in the rectangles. The flow charts provide a sequential formulation of the events that are produced by in-out control and format control.

The logic for initiation of tape commands is part of in-out control (refer to the logic drawing, Figure 6-15). The system enters the sequence shown in Figure 6-1 through the instruction mic. For convenience, the command pulse operations listed in Table 6-2 are also included at the top of Figure 6-1. The command provided by mic is transferred to the command register. From this register, it is decoded to govern operation of tape control and tape unit.

After a delay for tape motion to begin, the actual execution of the command is started by the pulse 1/2 UP SPEED. The particular sequences of operations for the different types of

commands are shown in separate flow charts, Figures 6-2 to -5. Most of the logic for the operations in these flow charts is part of format control (logic drawing, Figure 6-16), but the logic nets that control individual registers are part of in-out control (Figure 6-15). The tape commands Write, Forward Space, and Backspace are shown in individual flow charts (Figures 6-2, 6-4 and 6-5 respectively); but since Read and Readcheck are similar, they are shown together (Figure 6-3). Read and Readcheck differ only in mode of HSC access, which is shown as a separate flow chart.

During execution of Write, Read and Readcheck commands, data transfers between computer and tape control are made through a high speed channel. In the command flow charts, each time HSC REQ is set, a reference is made to the flow chart for HSC access (Figure 6-6). This flow chart shows both the HSC cycle within the computer and the access operations required in the tape control. The HSC memory cycle is shown at the left; at the right are the tape control events, spaced so that the timing is related to the memory cycle events.

When any command is completed, the line of flow returns to the terminatation portion (bottom) of Figure 6-1. The termination logic is also part of format control. At the very end of the operation, the tape control returns the completion pulse RECORD DONE to the computer. If operations are to continue on the same tape unit, the line of flow returns to the initiating sequence (upper part) of the flow chart, through a 2-millisecond delay during which the program must provide new initiating instructions. In this case, the instruction mic causes the tape control to enter the initiating sequence, but the signal $\overline{\text{SAME UNIT}}$ terminates normal flow at the pulse GO. Continuation of the sequence is produced by the delayed entrance from RECORD DONE.

Throughout the flow charts, various events are gated by logic levels which are not defined in the flow charts themselves. These logic levels are listed in Table 6-3. No flow chart is provided for tape unit operations because the only automatic time-sequenced events are information transfers through the read and write circuits. However, all logic functions governing tape motion and status are listed in Table 6-4.

b TYPE 51 SYSTEM - All programmed tape system operations are listed in Table 6-5. These include clear functions and events produced by iot command pulses. No flow chart is necessary because the only automatic operation is transfer of a character from CB to WB 6 microseconds after the mwc instruction. Tape unit logic functions are listed

in Table 6-4. Wherever programmed system tape unit functions differ from those in the automatic system, appropriate functions are indicated as "Type 52" or "Type 51."

6-3 PDP-1 CONTROL

A magnetic tape system may be attached to the computer by adding a small number of plug-in modules to in-out transfer control and connecting the appropriate in-out plugs and cables. Additions to iot control for the Type 52 and Type 51 Systems are shown in Figures 6-7 and 6-8, respectively. These figures show logic and module types but do not give unit locations or pin connections. For locations and wiring connections, see Figures D9-1 and D9-7 in the basic PDP-1 manual. For information on iot decoding and general organization of iot control, refer to paragraph 9-2 in that manual.

a TYPE 52 SYSTEM - Decoding of the iot instructions governing the automatic magnetic tape system is shown in Figure 6-7. The two initiating instructions (muf, mic) and the two reset instructions (mrf, mri) each generate command pulses at both TP_7 and TP_{10}. All eight command pulses are applied to the tape control unit. Furthermore, various other signals such as TP_{4-4}, STOP-4, POWER CLEAR and SC-4 are also applied. However, transmission of noninstruction signals outside of the computer requires no additional equipment in iot control unless a given signal is to be used by more than one external device. In this case each signal line must be driven by a separate 4603 Pulse Amplifier.

Besides initiating and resetting instructions, the tape system requires two examine instructions - mes and mel. Each of these develops a single command pulse which is not transmitted to the control unit; instead, the pulse is applied to the input mixer in order to transfer appropriate information into the in-out register. These two instructions require only a single command pulse at TP_{10} because all iot instructions in class 30 automatically clear IO at TP_7.

If more than one tape control unit is added to the computer, the equipment shown in Figure 6-7 must be duplicated for each additional unit. Further, a simple network must be added to decode bits 6 and 7 of each instruction word, so that command pulses are generated only for the addressed TC.

b TYPE 51 SYSTEM - The equipment that must be added to iot control to govern the

programmed magnetic tape system is shown in Figure 6-8. In each of the four instructions actually governing operations in the tape control, command pulses are generated at both TP_7 and TP_{10}. However, only in the mode-selecting instruction (msm) are the pulses transmitted to the control unit on lines unique to a single instruction. In the other three instructions (mcb, mrc, mwc) only one pulse for each instruction is transmitted over a unique line. The other three pulses are ORed to clear the TC character buffer.

In addition to being transmitted to the control unit, the first pulse in the read instruction (MRC_7) clears program flag 2 so that it can signal the detection of the character. MRC_7 also sets program flag 4 if a parity error has occurred during the previous read instruction. The status-checking instruction (mcs) produces only one command pulse at TP_{10}; this pulse is applied to the input mixer rather than the TC. However, as in the case of all class 30 iot instructions, iot control automatically clears the in-out register before transfer of status information into it. Besides the command pulses transmitted to the control unit, a clear pulse is also provided. This pulse is generated when power is first applied to the computer system, and also when the console stop switch is turned on.

c SIGNAL CONNECTIONS BETWEEN PDP-1 AND TAPE SYSTEM - The signal layout of in-out plugs for the PDP-1 Magnetic Tape System is shown in Figure 6-9. The Type 52 System requires three IO plugs; the Type 51 System requires only one. In the figure, each plug is shown by two columns. For each plug, the left column gives the signal connection to the PDP-1; the right column gives the signal connection, or signal meaning, in the tape control. For each plug, the type, direction and polarity of the signal are shown by diamonds and arrows drawn between the two columns.

6-4 COMMAND LOGIC

Each PDP-1 in-out transfer instruction contains two operation codes. The primary code (indicating an iot instruction) is decoded by the instruction register. The second code (indicating a specific operation for a device control unit) is decoded into command pulses by iot control. However, the instruction Magnetic Tape Initial Address and Command (mic) contains a third operation code. This 4-bit code (bits 8 to 11 of the instruction word) specifies the particular tape control unit operation for governing the tape transport.

During the mic instruction, this third operation code is transferred from the memory buffer to the command register in the TC. From the contents of CR, two sets of decoders develop the necessary control levels. One set provides control levels for TU; the other provides levels for TC.

a COMMAND REGISTER - The 4-bit command register (CR_{8-11}) is shown at the lower right of Figure 6-10. In normal operation, this register is cleared by a pulse from register control (paragraph 6-9e). Conditions that generate the clear include the first command pulse in mic. The second command pulse in mic loads the 4-bit tape command code into CR from bits 8 to 11 of the iot instruction word. The 12 legal commands and their 4-bit codes are as follows:

Command	Code (Bits 8-11)	
mst	0000	
mrw	0001	
mbs	0010	(fast)
mbs	0011	(slow)
mfe	1000	(fast)
mfo	1001	(slow)
mwe	1010	
mwo	1011	
mce	1100	
mco	1101	
mre	1110	
mro	1111	

The four possible 4-bit codes not listed here are illegal codes. The normal codes are as listed, with the exception of mst and mrw.

If the initial and final addresses become equal but are reset, the first command pulse in mri clears CR_{10}. The second command pulse then sets CR_{10} if bit 10 of the instruction word is 1. Thus, the TC may continue in operation, but the program, by manipulating the third bit of the command code, can change the operation from readchecking to reading or vice versa (see table above).

The command register is also cleared by ccr, which is equivalent to mrf but with a 1 in bit 8. In this case, command pulse MRF_7 also frees the control unit by clearing flip-flop TC BUSY (paragraph 6-9a).

b COMMAND DECODERS - Command decoders that develop control levels for the TU are shown above the command register in Figure 6-10. Those that develop control levels for the TC are shown to the left of the register.

In control of the tape transport, a single bit of the command register sometimes determines a property common to several commands, while in other cases the entire command code must be decoded. For example, the 1 state of CR_8 causes the tape to move forward because all command codes beginning with 1 require forward motion (refer to the command codes listed in a above). Reverse motion is produced by either of the Backspace commands (codes 001X); writing is enabled by either of the Write commands (codes 101X). On the other hand, the rewind level to the tape transport is asserted only for the Rewind command (codes 0001).

All normal commands are executed at a single speed; however, two-speed logic is included in case the equipment is used with a two-speed tape transport. In the spacing instructions (codes 001X and 100X), the fourth bit (CR_{11}) determines the speed. On commands 0010 and 1000, the transport runs at the higher speed (SPEED #2). Whenever neither SPEED #2 nor REWIND is asserted, the transport runs at the lower speed. The various control signals discussed above are applied to the TU through the bus drivers shown in the center of Figure 6-12.

Command codes are decoded in greater detail for the control unit because the TC must control information transfers and many other operations rather than just tape motion. Again, the 1 state of CR_8 specifies a forward command while in all Write, Read and Readcheck commands, the state of the fourth bit (CR_{11}) determines the parity (Figure 6-10C7). The outputs of CR_{11} are applied to the parity nets for the write buffer and the read buffer. Among the control levels shown at the left of CR are levels specific to each normal command (disregarding parity) and to pairs of commands requiring common operations. The level causing reverse tape motion also indicates that TC is controlling backspacing. Command code 100X indicates forward spacing. In either case, the spacing level causes TC to count records rather than the usual words. Similarly, the level that allows writing in the tape transport indicates that TC is controlling writing, while codes 110X and 111X indicate readchecking and reading, respectively. Further, readchecking is combined with both of the other operations. Data transfers between TU and TC are the same for reading and readchecking; data transfer between computer and TC are the same for writing as for readchecking.

The normality and legality of commands are determined by decoding nets shown in C3. Commands that are not normal are those whose codes are of the form 01XX or 000X. However, Write also fails to be normal if the write enable ring is not in place in the tape transport. Among commands that are not normal, all are illegal except Stop and Rewind (codes 0000 and 0001, respectively).

6-5 ADDRESS LOGIC

To begin operation of the automatic magnetic tape system, the program must provide not only a tape command but also three addresses. Two of these are memory locations specifying the initial address and the final address for access to memory through a high speed channel. The third address is that of the tape unit to be controlled by the tape control unit.

The initial address is the first current address. As each word is transferred between the computer and the tape, the current address is incremented by 1. When the current address is the same as the final address, TC signals the computer that the desired number of words has been transferred. The program may then cause further data transfers by resetting the initial and final addresses.

a CURRENT ADDRESS - The 16-bit current address register specifies a memory field (module) and a memory location within the specified field (Figure 6-11). The initial address is made available to CA from the in-out register. Flip-flops in CA are connected in a carry configuration through the capacitor diode gates shown immediately below the register. A change in state of a given bit from 1 to 0 complements the next more significant bit.

Outputs of all flip-flops in the register are applied to the address-equal net for comparison with the contents of the final address register (d below). The 1 outputs of CA are also made available to the high speed channel address mixer and the input mixer in the computer. The current address is transmitted through HSAM to the memory address register for each high speed channel memroy access. The current location may be examined by the instruction mel, which transfers the contents of CA through IM to IO.

Clear and transfer pulse inputs into CA are shown in Figure 6-11, B2 and C2. The positive-going pulse that clears the register is produced through a 2-microsecond delay. This extra pulse is required in order to prevent the clearing of a flip-flop in the register from setting the next more significant flip-flop through the carry chain. In normal operation, the current

address register is cleared from register control (paragraph 6-9e). The pulse $\lfloor 0 \rightarrow$ CA includes the first command pulse in the initiating instruction mic. Following the clear, the second gated command pulse MIC_{10} OK transfers the initial address from IO into CA.

As each word is transferred to or from the TC through a high speed channel, the address in CA is incremented by 1. The pulse $\lfloor +1 \rightarrow$ CA is generated by register control. When the current address equals the final address, TC sends the address-equal signal to the computer. The program may then continue tape operations within the same record by resetting the initial and final addresses. The initial address is reset by the instruction mri. The first command pulse in mri clears CA; the second pulse transfers in a new address from IO. The two command pulses are also applied to the command register to adjust the state of CR_{10} according to bit 10 of the instruction word (paragraph 6-4a). This allows the program to switch from reading to readchecking, or vice versa, while resetting the initial address.

b UNIT ADDRESS - A single Type 52 Control Unit can handle up to eight magnetic tape units. The particular tape unit to be used during any given operation is selected by the 3-bit unit address register UA (lower left, Figure 6-12).

The instruction muf transfers both unit address and final address from the computer simultaneously. The clear pulse for UA is provided by register control (paragraph 6-9e). The pulse $\lfloor 0 \rightarrow$ UA includes the first command pulse of muf. The second command pulse then transfers the unit address into UA from the three least significant bits of the accumulator. However, during muf, the clear and transfer are performed only if a new unit is being selected. The two command pulses of muf are gated so that if the TC is to continue into another record with the same tape unit, UA is not cleared and no new address is transferred into it. The gating for the first command pulse (MUF_7OK) is performed in the net that generates $\lfloor 0 \rightarrow$ UA. The gating of the second command pulse is performed by the level SELECT UNIT at the inputs to UA. The gating in both cases is developed by the continue logic (paragraph 6-9c).

The address provided by the accumulator is decoded from UA by a standard binary-to-octal decoder. For each 3-bit address in UA, a single output of the decoder is enabled. All eight decoder outputs are applied to the tape units through the local tape bus. The TU that goes into operation is that one whose address switch has previously been set to the same address as that contained in UA. The program may, of course, write on two tape units simultaneously by setting the address switches of both units to the same selected address.

c FINAL ADDRESS - At the beginning of each tape operation, the program must provide a 16-bit final address to the final address register, FA (Figure 6-12). The final address is provided from the in-out register through the same in-out plug connections that provide the current address to CA. The outputs of FA are used only by the address-equal logic (d below).

When power is supplied to the tape control unit, all registers (including FA) are cleared. The clear is developed through register control (paragraph 6-9e), which generates $\underset{\text{IO}}{\longrightarrow}$ FA and the clear pulses for the other registers. However, when a computer operation is initiated from the console, the associated clear does not include FA. The start clear pulse SC clears all other registers in TC but instead of clearing FA, it sets FA_3. In normal tape operations, a sequence break is requested when the current address becomes equal to the final address. Setting FA_3 (by SC) prevents a spurious sequence break request by assuring that the contents of FA and CA are not both zero.

When tape operations are initiated, the first command pulse (muf) clears FA by generating $\underset{\text{IO}}{\longrightarrow}$FA. The second command pulse then transfers the final address from IO to FA. After CA is counted up to FA, a sequence break is requested. The program may then continue operations within the same tape record by resetting the initial and final addresses. In resetting the final address, the first command pulse in mrf clears FA; the second loads a new final address from IO into FA.

d ADDRESS EQUAL LOGIC - The net that develops the level ADDRESS EQUAL is shown above the final address register in Figure 6-12. The inputs to the net are the 0 and 1 outputs of both FA and CA. Outputs of each bit of FA are paired up with the opposite outputs of the corresponding bit of CA through negative OR gates. Thus, all transistors in the net are cut off only if all flip-flops in CA are in exactly the same configuration as those in FA. Therefore, ADDRESS EQUAL is asserted only when the current address is equal to the final address. When the address has become equal, indicating that the desired number of words has been transferred between computer and tape, a sequence break is requested. With the single-channel sequence break system, the address-equal level is used directly. With the Type 20 Sequence Break System, a pulse is developed from ADDRESS EQUAL by in-out control (paragraph 6-9d).

6-6 DATA WORD BUFFER

All data transfers between memory and tape control unit are made as full-word transfers through a high speed channel. However, all data is transferred between the control unit and the tape as 6-bit characters. Of course, each character on the tape actually includes a seventh bit for parity in addition to the six data bits. Transition from 18-bit words to 6-bit characters, and vice versa, is carried out in the data word buffer.

The 18-bit data word buffer DWB is shown in Figure 6-13. In writing, computer words are made available from the memory buffer through a high speed channel and one of the in-out plugs. After an 18-bit word has been transferred into DWB, the six bits in DWB_{0-5} are transferred to the write buffer (paragraph 6-12). After the character has been written on tape, the contents of DWB are shifted left six places, and the second character is transferred into the write buffer from DWB_{0-5}. After the second character is written, another 6-place shift occurs and the third character is written.

In reading, characters are transferred from the tape in the same order in which they are written. However, no shifting is performed to assemble a full word in DWB. Instead, DWB input gating for transfers from the read buffer is divided into three sections. The first character is transferred from RB directly into DWB_{0-5}. Similarly, the second and third characters are transferred from RB directly into DWB_{6-11} and DWB_{12-17}, respectively. After the full word is assembled and a high speed channel request has been granted to the TC, the word is transferred from DWB to memory through an in-out plug and the HSC buffer mixer.

Pulses governing information transfers for DWB are shown at the left of the register. Clearing of the data word buffer is performed by register control (paragraph 6-9e). In writing, DWB is cleared after the third character is written. The register is then free to accept the next word from MB. In reading, DWB is cleared after a word is transferred to MB; the register is then free to accept new information from tape.

Transfer of information from MB into DWB is performed by an exclusive OR pulse. In writing, MB XOR DWB is preceded by a clear; the exclusive OR is, therefore, equivalent to a 1 transfer. In readchecking, however, the exclusive OR occurs immediately after DWB is filled from tape. If the contents of DWB and MB are identical, the exclusive OR clears each flip-flop in DWB. The data word buffer is checked for zero contents by diode nets (A1). If any bit of DWB is in the 1 state after the exclusive OR, a readcheck error is indicated.

As characters are written onto tape, the contents of DWB are shifted left six places by a shift pulse from format control (paragraph 6-10b). SHIFT DWB produces a 3-place shift directly. It also triggers the 2-microsecond delay in 1F2 which in turn produces a second 3-place shift. As each character is read from tape into the read buffer, the read strobe transfers the character into the word buffer. The character counter in format control (paragraph 6-10a) determines which character is being read and generates the corresponding character level. These three character levels gate the read strobe so that the character is sent to the appropriate section of the buffer.

6-7 WRITE BUFFER

Information is written on tape by adjusting the states of flip-flops in the write buffer according to the states of corresponding bits in the data word buffer (upper left, Figure 6-10). In NRZ recording, a 1 is represented in a channel on the tape by a change in magnetization. Magnetization is changed by changing the state of the corresponding write buffer flip-flop. Thus the write signal from format control (paragraph 6-10b) does not transfer information into WB from DWB but instead complements a WB bit if the corresponding DWB bit is 1.

The write buffer is cleared when tape operations are initiated, but never during a record. Instead, a sequence of write signals writes consecutive characters on the tape by adjusting the state of the buffer. After the record is complete, the buffer is cleared to produce an end-of-record character whose bits represent longitudinal parity. Since a 1 is written in a given channel each time the corresponding WB flip-flop changes state, the final state at the end of the record depends upon the number of 1s in the channel. A flip-flop contains a 1 if an odd number of 1s have been written; it contains a 0 if an even number of 1s have been written. Clearing WB writes a 1 in only those channels corresponding to WB flip-flops that were in the 1 state before the clear. Thus, the configuration of the end-of-record character produces an even longitudinal parity; i.e. if the parity character is included in the record, each tape channel contains an even number of 1s.

The write buffer contains seven flip-flops: six data bits (WB_{0-5}) and a parity bit (WB_p). The WB data bits correspond to channels on the tape. This is in the opposite order from the data bits received from DWB. The input from DWB_0 is at the left, but it conditions WB_0 at the right. Outputs of WB_0 are applied to the write driver for channel 6. Similarly, WB_5 (on the

left) is conditioned by DWB_5, but it provides information to channel 1. The WB outputs are applied to NRZ drivers (paragraph 6-12b) through bus drivers shown in Figure 6-12, C3 to C5.

The exclusive OR nets shown below the WB input gates develop the parity bit for each character. When data bits are made available to the WB input gates from DWB, the parity bit is also made available at the input gate to WB_p by means of level changes through exclusive OR nets. Diode nets in 1D7 provide the first level of parity generation by producing exclusive OR functions of each of the three pairs of contiguous bits in DWB. The second and third parity net levels are pairs of cross-connected transistors shown below the diode nets. Two of the first level outputs are XORed in 1D9 (B3). At the right in 1D10 (B4, B5), the remaining first level output is XORed with the 0 output of command register parity flip-flop CR_{11}. The two outputs of the second level are then XORed by the transistor pair at the left of 1D10. The ground-asserted output of the third level at 1D9M represents a parity bit of 1. Assertion of this level depends upon the number of 1s in the six data bits and upon the state of parity flip-flop CR_{11}. The parity bit is 1 if DWB_{0-5} contains an odd number of 1s when even parity is specified or if DWB_{0-5} contains an even number of 1s when odd parity is specified.

The parity level is inverted at 1D9R and applied to the input gate of WB_p. Thus WRITE adjusts the state of WB_p according to the output of the parity nets at the same time that it adjusts the states of WB_{0-5}.

6-8 READ BUFFER

The read buffer and its associated logic are shown in the upper two thirds of Figure 6-14. As each character is encountered on the tape, it is transferred into the 7-bit read buffer. RB_p receives the parity bit, while RB_{0-5} receives the six data bits. The channel connections to the RB bits are the same as those to the WB bits (paragraph 6-7). That is, information from channel 1 goes into RB_5, and so on to information from channel 6 which is sent to RB_0. Thus, a character read from tape has the same configuration in the read buffer that it had before in the write buffer; a full 18-bit computer word assembled in DWB looks exactly as it did in DWB before being written on tape.

Below each buffer bit is a Type 1539 Peak Detector and Slicer. Each detector produces two outputs--a level and a pulse. Both of these are applied to the capacitor-diode input gate at the corresponding bit of the buffer. Whenever a 1 is encountered in any tape channel, the

signal output through the differential amplifier and rectifying slicer in the tape unit (paragraph 6-12b) is applied to the peak detector. During the tape signal, the gating level output of the detector is asserted. At the peak signal return the detector produces a pulse which is gated through the capacitor-diode input gate by the level to set the corresponding flip-flop in the buffer. A detailed description of the Type 1539 circuit is given in paragraph 7-3d.

After each character is sent from RB to DWB, register control clears the read buffer by generating $\boxed{0} \rightarrow$ RB (paragraph 6-9e). Then as bits of the next character are encountered on tape, they are transferred individually into the RB flip-flops. Because of tape skew, bits of a single character do not necessarily arrive simultaneously at RB. For this reason a period of 25 microseconds is allowed between arrival of the first bit in RB and generation of the read strobe which transfers the contents of RB to DWB. It is assumed that tape skew can never be great enough to require more than 25 microseconds between arrival of the first and last bits.

Arrival in RB of the first bit from the tape is detected by diode nets (Figure 6-14A2). When RB is cleared, a ground level is produced at 1E5E. As soon as any bit of RB is set, the level at 1E5E is asserted, producing the character-detected level at 1E3J. There are times when reading of information from the tape is inhibited. The inhibit, however, is supplied directly to the detection circuit rather than to the input gating of the read buffer. If any inhibit level is asserted (B2), the detection level at 1E5E is grounded and thus remains unaffected by changes in state of the RB flip-flops.

Reading of information from tape is prevented by the initial read delay when the tape is first put in motion, by the read inhibit as the record gap moves past the read head, and by the load point read inhibit when the tape is put in motion from the load point. These inhibits are described in greater detail as part of the execution of tape instructions (paragraph 6-9c). Reading is also inhibited if the command register specifies an abnormal instruction. This prevents reading tape while rewinding.

As character bits are loaded into the buffer, level changes through the logic nets shown above RB check the parity of the character against the parity required by CR_{11}. The parity function is generated by a three-level set of exclusive-OR nets in the same way that the parity bit is generated for the write buffer (paragraph 6-7). However, the read parity nets are symmetrical; there are eight inputs as against seven inputs in the write parity nets. In writing, a parity bit is generated according to the six data bits and CR_{11}. In reading, a parity function is generated

from the seven bits of the character and CR_{11}. There are thus eight inputs to the first level, four inputs to the second level and two to the third level in the nets. Wrong parity is indicated if the character has odd parity when CR_{11} specifies even parity, or if the character has even parity when CR_{11} specifies odd parity.

6-9 IN-OUT CONTROL

This paragraph describes hardware linking computer and magnetic tape system. In-out control includes equipment which prepares the tape system for operation, determines and indicates the status of the system and controls transfer of information between computer and tape control. The paragraph also includes the logic through which computer initiating instructions govern tape operations. The hardware that performs these various functions is shown in Figure 6-15. The logic that governs the actual process of writing and reading tape is described in paragraph 6-10.

a CLEAR LOGIC - When power is first applied to the TC, the circuit connected to pin Y of the power clear clock (Figure 6-15B4) grounds Y until the capacitor connected to W charges. Thus, for a short time at power turn-on (and turn-off) the power clock generates clear pulses. These pulses directly clear the final address register (A5) and the tape unit (A8). The clear pulse for the TU is stretched to 4 microseconds by a 4301 Delay and applied to the unit through a bus driver.

Besides clearing FA and TU, the power clock clears all registers and flip-flops in TC through the pulse amplifier in B4. Whenever any operation is initiated from the computer console, the start clear pulse also clears TC through the same pulse amplifier. Note, however, that SC does not clear FA or TU; instead, the start clear pulse sets FA_3 so that the contents of FA and CA cannot be equal (i.e. both zero) and thus generate a spurious sequence break request. Whenever computer operations are halted from the console,the pulse from the stop switch (A8) clears both command register and tape unit.

b SYSTEM STATUS - The program can examine the status of the magnetic tape system through the instruction mes. It does this by adjusting the states of in-out register bits according to status levels provided by the tape system. Status of the tape unit and the tape itself is provided by status levels directly from the tape transport. Status of the tape control is indicated by the row of flip-flops shown below the center of Figure 6-15 and the

single flip-flop TC BUSY shown at the left in the same figure. All these flip-flops are cleared when TC is cleared.

Flip-flop TC BUSY indicates whether or not the tape control is currently in use. It is set when an initial address and command are sent to TC; it then remains in the 1 state until cleared by the completion pulse, indicating that the tape operation has been completed. However, TC BUSY is also cleared by the maintenance instruction Clear Command Register ($MB_8^1 \cdot MRF_7$) which bypasses all interlocks to halt tape operations.

When TC BUSY is set at the beginning of tape operations, the error flip-flops are cleared. The first two flip-flops on the left (C4) indicate errors in normal retrieval of information from the tape. One flip-flop indicates a parity error in the character read; the other shows that a character has been skipped. An error flip-flop is set if the corresponding error level is asserted at the time of the read strobe, provided the tape is moving forward. Tape information is not checked for errors during back-spacing. The level indicating incorrect parity is provided by the read buffer parity checking nets (paragraph 6-8), while the level indicating a missing character is provided by format control (paragraph 6-10c).

The readcheck error flip-flop is controlled by the high speed channel transfer logic (b below), while the flip-flop indicating failure of the computer to respond in time to an HSC request is governed by format control (paragraph 6-10d). The next flip-flop in the row (HSC REQ) is cleared along with the error flip-flops at the beginning of tape operations but is not a status flip-flop (d below). The flip-flop at the right end of the row is the last error flip-flop. Ten microseconds after mic has loaded the command register, the illegal command flip-flop is set if CR contains an illegal command code.

The two flip-flops between HSC REQ and ILLEGAL are the continue flip-flops; they indicate the status of TC with respect to continuation of tape operations into a new record after operations on the current record are completed. These two flip-flops are not cleared by mic along with the error flip-flops; their states are governed by muf, which must precede mic. The first command pulse in muf clears both continue flip-flops; the second command pulse then adjusts their states according to bits 10 and 11 of the instruction word. If MB_{11} is 1, WILL CONT is set indicating that, at the completion of the current operation, the computer will continue into a new record with the same TC (but not necessarily on the same TU). Furthermore, if MB_{10} is 1, WILL CONT SAME is set, indicating that at the

completion of the current operation the computer will continue into the next record on the same tape unit. Following execution of the mic instruction, the one-half-up-to-speed pulse sets the same unit flip-flop if both continue flip-flops are in the 1 state (c below). WILL CONT SAME is cleared simultaneously. Note, however, that WILL CONT is not cleared because this flip-flop governs the generation of the completion pulse by format control at the end of the operation (paragraph 6-10e). No inhibit is included to prevent the program from setting WILL CONT SAME without setting WILL CONT, but this configuration is ignored by the system.

Tape system status levels are available to the computer through the in-out plug shown in the lower part of Figure 6-14. There are 17 individual status levels from the TC flip-flops and from the TU. Each line is connected through the input mixer to a single bit of the in-out register. The OR function of the seven error conditions (six TC error flip-flops plus the transport end point condition) is applied to IO bit 0. All status levels are inverted so that assertion is at -3 volts. Thus, after transferring status information into IO with a mes instruction, the program can check the appropriate bit in IO_{1-17} to determine the existence of a specific condition, or it can check IO_0 to determine the existence of any error condition.

In addition to providing status information, flip-flop TC BUSY provides an interrupt level for the single-channel sequence break system. Upon completion of a tape operation, TC BUSY is cleared, and the resultant assertion of $\overline{\text{TC BUSY}}$ causes a sequence break request.

c INSTRUCTION EXECUTION - Figure 6-15 shows the logic through which the PDP-1 in-out transfer instructions control the automatic magnetic tape system. Some PDP-1 control functions, such as the command pulses that reset initial and final addresses, are shown in the appropriate Type 52 Drawings. However, most control signals between computer and TC are shown at the left of Figure 6-15.

All tape operations are initiated by the PDP-1 instructions muf and mic. Command pulses for these instructions are gated so that the computer cannot attempt to initiate operations in a TC or a TU which is not available. Gating for these command pulses is provided by a pair of flip-flops, TC BUSY and TU OK. Since conditions governing these flip-flops may be fulfilled at any time (e.g. the completion pulse clears TC BUSY), synchronization to computer timing is provided by TP_4. This time pulse adjusts the state of TU OK directly but transfers state changes of TC BUSY to a second flip-flop, TC BUSY SYNC.

Assume that a specific tape unit is being selected for the first time - that is, the operation being initiated is not to continue into the next record on the previously addressed tape and, therefore, flip-flop SAME UNIT is 0 (B6). The first initiating instruction from the computer provides the unit address and final address. The two gated command pulses (MUF_7 OK and MUF_{10} OK) are produced from the muf command pulses only if the tape control is not already in operation (B2). The first command pulse increments the program counter (C2) to indicate to the computer that the attempt to call the TC was successful. This pulse also clears the unit and final address registers (A5) and clears the two continue flip-flops (C6). The second command pulse then loads FA from IO_{2-17} (paragraph 6-5c) and adjusts the states of the continue flip-flops according to bits 10 and 11 of the instruction word. Since SAME UNIT is 0, asserting the level SELECT UNIT (B8), MUF_{10} OK also loads UA from AC_{15-17} (paragraph 6-5b).

After the computer provides unit and final addresses, the second initiating instruction provides the initial address and command, placing the tape system in operation. The two mic command pulses are gated by flip-flop TU OK. This flip-flop is 1 if TC is not busy, and if the TU addressed by the previous muf is ready. The first command pulse, MIC_7 OK (besides incrementing PC) clears the error flip-flops (C3), the current address register (A5), the read buffer and the command register (A7). The second pulse then loads CR and CA from MB_{8-11} and IO_{2-17}, respectively (paragraphs 6-4a and 6-5a), and clears the write buffer (A6). Immediately after a command is loaded into CR, the levels asserted by the command decoders put the transport in operation. As the tape begins to move, TC also generates a sequence of timing functions which prepares the system for the first reading or writing of information.

The second command pulse (MIC_{10} OK) initiates this sequence by triggering the 10-microsecond delay in B5. This delay inhibits reading while tape motion begins and then, at termination, produces the GO pulse. If mic has loaded an illegal command into CR, GO sets the appropriate status flip-flop (C7). Furthermore, if the command is not normal, GO clears the command register (A7) and produces the completion pulse (paragraph 6-10e). Thus, operation of the tape control ceases immediately, not only for an illegal command but also for Stop or Rewind. Once Rewind is initiated, TU completes the operation automatically, freeing TC for further use by the computer.

Since SAME UNIT is clear, GO generates GO NEW (B6), indicating that the computer is addressing a unit whose tape is not already in motion. The effect of GO NEW depends on the position of the tape in the supply reel. If the tape is not at load point, GO NEW triggers a 2-millisecond delay during which reading is inhibited. At the end of the delay, the tape is one-half up to speed and the pulse 1/2 UP SPEED is generated (B8). This pulse initiates operations within format control to begin reading or writing. It also clears RB and DWB (A7, A4) and adjusts the state of the same unit flip-flop. If both WILL CONT and WILL CONT SAME were set by the previous muf, SAME UNIT is set indicating that, at completion of the current operation, TC will continue into a new record with the same tape unit. At the same time 1/2 UP SPEED also clears WILL CONT SAME.

If the tape is at load point in the supply reel, GO NEW triggers a different initiating sequence. Instead of triggering a 2-millisecond delay, it triggers a 24-millisecond delay (B7). Reading is inhibited during the delay, and the terminating pulse clears RB and triggers another 50-millisecond delay. The output of this delay then produces 1/2 UP SPEED. The tape has actually been running at full speed during most of the delay; this provides the six inches of blank tape required at the beginning of the reel.

With the generation of 1/2 UP SPEED, functions governing information transfers begin. Transfer of information in single characters between tape and TC is governed by format control (paragraph 6-10). Transfer of full 18-bit words between computer and TC is governed by the high speed channel transfer logic (d below). Each time the current and final addresses become equal in a Write, Read or Readcheck command, TC requests a sequence break. The computer may then provide new initial and final addresses with the reset instructions, and tape operation continues in the same record. When the end of the record is reached (or the end of the final record in spacing), format control generates the completion pulse RECORD DONE. This pulse clears TC BUSY (C2), indicating that TC is again free for operation from the computer. RECORD DONE also requests a sequence break if the computer includes the Type 20 Break System; otherwise the status level from TC BUSY requests a break through the single-channel sequence break system.

If the previous muf instruction has specified that use of the TC will continue into another record, the completion pulse is generated 3 milliseconds early and the computer must then provide new initial instructions. These begin tape operations in the normal manner.

However, if the previous muf has specified that tape operations will continue with the same tape unit, then flip-flop SAME UNIT is in the 1 state. This prevents the stop pulse from clearing the command register (A7) and then causes the completion pulse to trigger 1/2 UP SPEED through a 2-millisecond delay (B8). During this delay, the computer must provide new initiating instructions. In muf, SAME UNIT prevents clearing of UA and selection of a new unit (A5, B8). The instruction does, however, provide a new final address and new continue information. Then, SAME UNIT gates in mic command pulses by replacing the ready condition in TU OK (D3), but inhibits the normal starting procedure by preventing GO from generating GO NEW (B6). Finally, 1/2 UP SPEED again starts operations in format control and readjusts the state of SAME UNIT according to the newly provided continue information (B6).

d HSC TRANSFER LOGIC - Transfer of data between computer and tape control is governed by in-out control through the high speed channel transfer logic (Figure 6-15). Each time TC is ready to receive information from the computer or send information to it, format control requests an HSC transfer by setting flip-flop HSC REQ. This flip-flop may also be set by the maintenance instruction Initiate HSC Request ($MB^{1}_{10} \cdot MRF_{7}$). If TC is reading, all HSC transfers send information into the computer (B1). When the channel request is granted by PDP-1, the same pulse that sends the current address to the memory address register also triggers HSC operations in TC. The entire transfer operation uses a sequence of three pulses: the original HSC XFER (HSC X1) plus two pulses (HSC X2 and HSC X3) that are delayed by 4.5 and 8.5 microseconds respectively (B3). The initial pulse increments the current address register (provided there has been no previous readcheck error) and clears HSC REQ (A3, C5). Then, 4.5 microseconds later when the computer is in the write portion of the memory cycle, the second HSC pulse terminates the transfer. In reading, the computer HSC control sends the word from DWB to MB at TP_7, so HSC X2 merely clears DWB (A4). In writing or readchecking, a word is available from MB after TP_4 so HSC X2 pulses MB XOR DWB (A3). In writing, DWB is clear, so the exclusive OR produces a normal 1 transfer. In readchecking, the exclusive OR provides a comparison function between the word read from tape and the word read from memory. After the computer has completed the HSC cycle, two additional functions required for the TC logic are provided by the third HSC pulse. If the system is readchecking and DWB is not clear after the comparison function, HSC X3 sets the readcheck error flip-flop (D3, D4). If the HSC

transfer just completed has incremented the current address to the final address, and either the system is not readchecking or DWBis clear, then HSC X3 requests a sequence break in the Type 20 System (A2). For the single-channel sequence break system, the address-equal status level makes the request directly, with no further conditions.

e REGISTER CONTROL - Many control inputs for the registers, particularly those governing information transfers, are pulsed directly, either by command pulses or by pulses from format control. However, many register functions, particularly the clear pulses, require additional gating or are pulsed by a variety of input conditions. Generating nets for these pulses are shown at the top of Figure 6-15.

All system elements except FA and TU are cleared by CLEAR TC. These exceptions are cleared by the power clear. However, CR and TU are also cleared whenever the stop switch on the computer console is turned on. Most of the other pulse input conditions are developed from in-out control and are described in detail as part of the process of instruction execution and high speed channel transfers (c and d above). The other inputs to the nets are developed by format control; these are as follows.

Format control clears the read buffer after each character is transferred into DWB (A7), and clears DWB after each full word is shifted out to the write buffer (A4). Besides counting words when reading or writing, the current address register counts records when spacing. Thus, $\xrightarrow{+1}$ CA is pulsed each time the end-of-record is encountered while the system is spacing tape (A4). When writing has been completed, the end-of-record character is written on tape by clearing WB (A6). Upon completion of any tape operation, the stop pulse clears the command register unless the operation is to be continued with the same tape unit (A7).

6-10 FORMAT CONTROL

The logic that determines and reacts to the format of information on tape is shown in Figure 6-16. The two main portions of format control govern sequences of events by which characters are written on, and read from, the tape. Common to both portions are the character counter, the HSC request logic and the terminating logic.

a CHARACTER COUNTING - Two flip-flops, A and B, make up the character counter (Figure 6-16C1). At the beginning of each tape operation, 1/2 UP SPEED clears the

counter; then, as each character is written or read, the counter is incremented. Three character levels are developed from A and B outputs. Each level corresponds to a particular state of the counter and specifies the particular character within the current word. These character levels control transfer of characters from RB into the appropriate section of DWB, the shifting of characters out of DWB into WB and the requesting of HSC transfers.

Initially the counter contains 00, and the asserted level CHAR 3 enables the set input gate to B. The first count pulse thus sets B, and the configuration 01 asserts CHAR 1. With B set and CHAR 3 negated, the next count clears B and sets A; the configuration 10 asserts CHAR 2. With B again clear and CHAR 3 still negated, the next count clears A, returns the counter to its initial configuration and asserts CHAR 3.

b WRITE SEQUENCE - Logic governing the write sequence is shown in the upper left of Figure 6-16. Writing is synchronized to a clock which is independent of computer timing, in order to assure continuous writing at the proper frequency, independent of information transfers between computer and tape control. The clock is set at 15 kilocycles to produce a writing speed of 15,000 characters per second.

To begin writing, the clock is synchronized by a pair of flip-flops, WRITE and WRITE SYNC (B1, A1). Both of these flip-flops are cleared whenever the entire TC is cleared. The sequence of events that controls writing is triggered by 1/2 UP SPEED. If the command decoder specifies writing, 1/2 UP SPEED triggers a 4.2-millisecond delay (B1). This delay allows enough tape to move by the heads to complete a record gap. If the current and final addresses are not equal, the pulse output of the delay sets WRITE and generates the first HSC request. If the addresses are already equal, the delayed 1/2 UP SPEED instead triggers a 4.6-millisecond delay (A5) whose output initiates the terminating sequence (e below). Thus, if the addresses are equal at the beginning of a write operation, TC merely writes a second consecutive record gap on the tape.

As soon as WRITE is set, the first pulse from the write clock sets WRITE SYNC; every succeeding clock pulse produces PREWRITE. This pulse increments the character counter (C2) and also sets the error flip-flop HSC LATE if the preceding HSC request has not yet been granted. PREWRITE also triggers a 4-microsecond delay, generating WRITE (A2). This pulse writes the character on tape by complementing those WB flip-flops that correspond to 1s in the character presented by DWB_{0-5} and the parity generating nets (see paragraph 6-7,.

If the first or second character of a word is being written, WRITE also shifts the contents of DWB six places to the left. However, the shift is inhibited when the third character is being written, and WRITE instead clears DWB. At the same time, WRITE also generates an HSC request, provided the addresses are not yet equal.

This sequence of events is then repeated over and over. Each word brought in from memory is divided into three characters. As the third character is written, WRITE requests and HSC transfer for the next word. If the request is not granted before the next pulse from the write clock, HSC LATE is set. When the current and final addresses become equal during an HSC transfer, a sequence break is requested. The program then has 100 microseconds in which to reset the initial and final addresses. If the addresses are still equal when the third character is written, WRITE ends the record by triggering the 270-microsecond delay in A4. Even if the addresses are not equal, WRITE terminates the record if the computer has failed to grant an HSC request in time to write the next character.

As soon as the A4 delay is triggered, the level output stops further writing by clearing both WRITE and WRITE SYNC (B1). Then, during this 270-microsecond delay, TC writes 0.02 inch of blank tape. The output pulse at the end of the delay writes the end-of-record character by clearing WB, and also triggers the 4.6-millisecond delay in A5. The output pulse from this delay, in turn, initiates the terminating sequence (e below).

c READ SEQUENCE - The sequence of events that retrieves information from tape is governed by logic shown in the lower center of Figure 6-16. Each time the first bit of a character is detected, the READ DETECT pulse is produced through a 20-microsecond delay (D3). This pulse increments the character counter, provided the system is reading or readchecking. Characters are not counted when the system is merely spacing tape. READ DETECT also triggers a second delay of 5 microseconds which gives the character counter time to stabilize. The pulse output of this delay clears RB and produces the read strobe. The total delay of 25 microseconds between initial detection of the character and generation of the strobe which transfers the character to DWB is large enough to compensate for maximum allowable tape skew.

The pulse which clears RB is ungated; every time information is detected on the tape, RB is cleared 25 microseconds later. The read strobe is gated. In backspacing, every character detection produces a strobe. The strobe is gated in such a way, however, that it is

never produced by detection of the end-of-record character during forward tape motion. The read strobe triggers the three delay circuits shown in C5 and, if the system is reading or readchecking, it also triggers the pulse amplifier shown above the delay circuits. It is this strobe (at 1B15E) that transfers information from RB to DWB when the system must actually retrieve information from tape. The read-readcheck strobe is gated by levels from the character counter to send each character from RB into the appropriate part of DWB (paragraph 6-8). Reading of the third character in a word (i.e. the asserting of CHAR 3 at strobe time) generates an HSC request (A6), provided the addresses are not equal.

Thus the system repeats the read cycle over and over, retrieving an entire 18-bit word from tape each time. Each set of three characters is counted by the character counter and, when the third character is strobed into DWB, high speed channel access is requested. When the addresses become equal during an HSC cycle, the program has 100 microseconds in which to reset CA and FA. If the addresses are still equal when the third character is read, the HSC request is prevented and no further data is transferred between TC and computer.

Note that this does not stop the tape as in the case of the write sequence. When all desired information has been written, TC writes a record gap and the tape stops. In reading, only the data transfers cease, and the tape continues in motion until the record gap is encountered. Thus the tape stops only within a record gap. The same situation holds for failure of the computer to respond in time to an HSC request. If HSC LATE is set during writing, a record gap is written and the tape stops. In reading, if HSC REQ is still set 20 microseconds after another character is detected, READ DETECT sets HSC LATE. The status bit does, therefore, indicate an error but the system continues to read tape even though one or two words may have been lost.

The rest of the read sequence logic detects certain characteristics of tape spacing. The three delays triggered by the read strobe (C5) are 100, 230 and 480 microseconds. These are the time intervals that correspond to the space required for 1 1/2, 3 1/2 and 7 characters. If no strobe occurs for 100 microseconds, the > 1 1/2 CHAR level is asserted at 1B13E. On the other hand, the < 3 1/2 CHAR level at 1D25W remains asserted so long as no two consecutive strobes are more than 230 microseconds apart. These two output levels are ANDed to generate the character-missing level. If the tape is moving forward and a strobe occurs while this level is asserted, the character-skipped error flip-flop is set

(paragraph 6-9b). It is thus assumed that if no character is encountered for 100 microseconds, but a character is encountered within 230 microseconds, a character has been skipped.

If there is no strobe for more than 230 microseconds, the one-shot in 1D25 switches state, indicating that the record gap has been encountered. It is assumed that a space of more than 3 1/2 characters is the gap between record and end-of-record character. Assertion of > 3 1/2 CHAR produces a pulse at 1D22J. This pulse indicates to the HSC request logic that the read head is at the record gap (d below).

The third one-shot delay (1C25) produces the level > 7 CHAR whenever there is no strobe for longer than 480 microseconds. However, this does not mean that no character is encountered for 480 microseconds. The delay outputs < 3 1/2 CHAR and > 7 CHAR are applied to the read strobe gate. Whenever a space of 3 1/2 characters is encountered, the read head is presumably at the end of the record, and the strobe is disabled until the tape has moved a distance of 7 characters past the final data character. This prevents the system from strobing the end-of-record character into DWB and consequently prevents the possible detection of an irrelevant parity error.

Assertion of >7 CHAR reenables the strobe and also produces the end-of-record pulse EOR (C6). On reading or readchecking, this pulse triggers the terminating sequence. In spacing, EOR increments CA to count the record that has just been spaced over. But if the addresses are equal, indicating that the tape has been spaced the required number of records, EOR then initiates the terminating sequence.

d HSC REQUEST LOGIC - Each time TC is ready to receive or send a full word, high speed channel access to memory is requested. If access is not granted before the next character transfer between tape and TC is ready, an HSC LATE error is indicated. The logic governing this is shown in the upper right of Figure 6-16.

There are four sets of conditions that request an HSC transfer - two each for writing and reading. In all cases, the conditions require current and final addresses to be unequal. If the addresses become equal during an HSC cycle but are reset before timing conditions are fulfilled, further HSC access can be requested.

During writing, the first word is requested by the delayed 1/2 UP SPEED pulse (B2). All subsequent requests are made as the third character of each word is being written . Conditions

governing requests for reading and readchecking are combined. However, during readchecking, no further requests can be made after a readcheck error occurs. In normal operation, HSC REQ is set every time the third character of a word is strobed from RB into DWB. But if DWB contains only one or two characters when the record gap is encountered, an HSC transfer is also requested. This condition implies that at least one character has been skipped. All information retrieved after the skipped character is packed sequentially in the specified memory locations and the final partial word is deposited in memory left-justified.

If HSC REQ is still asserted when the next character transfer is ready, HSC LATE is set (A8). During writing, the time condition is provided by PREWRITE; during reading or readchecking, the time condition is provided by READ DETECT.

e TERMINATING SEQUENCE - The logic that governs termination of tape operations is shown in the lower right of Figure 6-16. The terminating sequence is triggered by an end-of- record pulse whose source depends upon the type of operation. In writing, the EOR pulse is produced 4.6 milliseconds after the EOR character is written (A5). Since the EOR character follows the final character in the record by 270 microseconds, total time delay between the end of record and the EOR pulse is 4.9 milliseconds. During reading, readchecking or spacing, the EOR pulse is produced 0.4 milliseconds after the final character in the record (D5). Since the distance between the read head and the write head is equivalent to 4 milliseconds, the tape stops 0.5 millisecond sooner in reading than in writing. This prevents occurrence of inter-record trash caused by variation in stop time on reading a tape that has been written more than once.

The terminating sequence is started by triggering a 700-microsecond delay which produces the STOP pulse (C7). This delay is triggered directly by the EOR pulse from the write sequence logic; if the system is reading or readchecking, it is triggered by the EOR pulse from the read sequence logic. In spacing, the read EOR pulse initiates the terminating sequence only if the addresses are equal, indicating that the desired number of records has been spaced. In forward spacing, the stop delay is triggered directly; in backspacing, it is triggered through another 4-millisecond delay. This compensates for the distance between the heads.

STOP indicates that the read head is at the correct spot in the record gap, and it stops the tape by clearing the command register. It also generates the completion pulse, RECORD

DONE. If the previous muf instruction has specified that TC will not continue in operation, the completion pulse is delayed 10 milliseconds to allow the tape to stop and the pinch rollers to settle (C7). If operations will continue, the completion pulse is returned immediately. If operations are to continue into the next record on the same tape unit, the 1 state of the SAME UNIT flip-flop prevents STOP from clearing CR. It also causes the early completion pulse to initiate further tape operations by producing 1/2 UP SPEED through a 2-millisecond delay (paragraph 6-9c). During this delay, the computer must provide new muf and mic instructions to specify the new addresses and command. If no new initiating instructions are provided, the effect depends upon the type of operation previously performed.

In writing, a second record gap is written and the tape stops. In reading or readchecking, TC reads the next record and requests HSC access to memory for each word until the addresses become equal or the end-of-record is encountered, whichever occurs first. Since any number or records can be spaced with a single command, a space command should not specify continuation with the same unit unless new initiating instructions are definitely to be provided. Failure to change a space command results in tape spacing to the end of the reel.

In addition to the normal generation of RECORD DONE by STOP, the completion pulse is also produced by GO 10 microseconds after completion of a mic instruction, if that instruction specifies an abnormal command. This means that for illegal commands no operations are performed, and both TU and TC are available to the computer immediately. For Rewind, however, TC is available immediately while TU completes the operation automatically. In Stop, of course, the tape is halted and both units are available.

6-11 PROGRAMMED TAPE CONTROL TYPE 51

With the programmed magnetic tape system, the PDP-1 computer can handle up to three tape units with a minimum of peripheral hardware. The hardware that provides the necessary operations in the Type 52 Automatic System is replaced by programming that must be executed by the computer directly. Instead of merely specifying initial and final addresses for high speed channel access to memory, the program must initiate each character transfer through the in-out register. The program must provide all information to the tape as single characters, and must assemble the characters retrieved from tape into full words to be stored in memory. The Type 51 hardware is quite simple, but in order to understand the complicated timing of information

transfers, the reader should be familiar with the corresponding hardware in the Type 52 System (i.e. primarily format control, paragraph 6-10).

The complete Type 51 Tape Control is shown in a single logic drawing Figure 6-17. Control inputs to the system from the computer are shown at the left. These control inputs, including magnetic tape command pulses, are described in detail in paragraph 6-3b. All information transfers between computer and tape are made as single-character transfers through the character buffer (center, Figure 6-17). The TC includes two other registers: the write buffer at the top of the figure and the command register at the bottom. The command register governs the mode of operation of the tape unit. Finally, the control unit includes parity nets which are shown at the upper right. The figure also shows the status level connections from tape unit to computer. In the Type 51 System, these signals are opposite in polarity from the same signals in the Type 52 System. Thus in status examination, a 1 in an IO bit means the negation of the corresponding status level.

Of the control signals provided by the computer, two are clear pulses. Whenever computer power is turned on or operations are halted from the console, both command register and TU are cleared (D2, C2). The clear for TU is 3 microseconds wide and is produced through a 4301 Delay. Whenever any operation other than Continue is initiated from the computer console, the start clear pulse (A2) clears TU and all three registers in TC.

a COMMAND LOGIC - In the Type 51 Magnetic Tape System, tape unit operations are governed by an 8-bit command register (bottom, Figure 6-17). Instead of specifying command codes that must be decoded by the TC, the program controls each operational characteristic of the TU through an individual bit of the command register. The two flip-flops at the left (D3) specify on/off events. The program places the addressed tape unit in operation by setting the operate flip-flop. The programmer may wish to address a TU without placing it in operation (for example, to check its status). In order to rewind tape, the programmer must set the rewind flip-flop. However, the 1 output of this flip-flop is ANDed with the R output of the direction flip-flop so that the tape rewinds only if the programmer also specifies that it shall move in reverse.

The four flip-flops in the center of the command register specify binary functions which are not on/off events. That is, each specifies one or the other of two mutually exclusive operations, rather than specifying whether a single operation shall or shall not be performed. The direction flip-flop specifies either forward or reverse. The data mode must

be either read or write; the parity must be odd or even, and the speed, high or low. The last flip-flop is not used, but is included to enable the system to control a two-speed tape transport.

The final two flip-flops, A and B, function together to provide a tape unit address. The program addresses a specific TU by loading a 2-bit address into these flip-flops. The address is decoded by the diode net in D7, and the specific unit is addressed by a ground level on the corresponding unit line. Address 00 is no selection; the other three 2-bit numbers address units 1, 2 and 3.

The outputs of the address decoder and several of the flip-flops in the command register are applied to the TU. REWIND is used only as an input to the diode gate which ANDs the rewind function with the reverse direction. The tape transport receives the output of the AND gate. Since parity generation and checking are performed entirely in TC, the outputs of the parity flip-flop are applied only to the parity nets and not to TU.

The instruction msm selects a specific TU and its mode of operation by loading information into the command register from the in-out register. The first command pulse in msm clears the register; the second loads the contents of IO_{10-17} into it.

b WRITE LOGIC - The instruction mwc causes TC to write a single character on tape. The sequence of operations governing writing requires two buffers; the character buffer, CB, and the write buffer, WB (upper half, Figure 6-17). Both buffers are shown with bit 5 at the left, because this bit corresponds to channel 1 on the tape. Similarly bit 0, at the right, corresponds to channel 6.

The program must provide each character that is to be written from the six most significant bits of the in-out register. The first command pulse in the mwc clears CB. The second pulse then transfers the character from IO_{0-5} into the data portion of the buffer, CB_{0-5}. The parity bit, CB_p, is not used in writing. The same command pulse that loads the buffer also triggers a 6-microsecond delay (A2). During this interval, the parity nets generate a parity bit for the character (d below).

After 6 microseconds, the output pulse of the delay adjusts the states of the write buffer flip-flops according to the contents of CB and the output of the parity nets. In NRZ recording, a 1 is written in a tape channel by changing the direction of magnetization. This change

in direction is produced by changing the state of the WB flip-flop corresponding to that channel. Thus the character is written in by complementing each WB flip-flop for which the corresponding CB flip-flop contains a 1. At the same time the parity flip-flop WB_p is complemented if the parity net output indicates a parity bit of 1.

The program may also clear WB with the first command pulse in the clear buffers instruction mcb. Since clearing WB writes a 1 in each channel of the tape that corresponds to a WB bit already in the 1 state, the clear buffers instruction allows the program to write an even-longitudinal-parity end-of-record character on tape.

c READ LOGIC - As each character is encountered on tape, it is loaded into the character buffer (center, Figure 6-17). Bit CB_p receives the parity bit, while CB_{0-5} receives the six data bits. Channel connections to the CB bits are the same as those to the WB bits (b above). That is, information from channel 1 is transferred into CB_5 and so on to information from channel 6, which is put into CB_0.

Below each buffer bit is a Type 1539 Peak Detector and Slicer. Each detector produces two outputs - a level and a pulse. Both outputs are applied to the capacitor-diode input gate at the corresponding bit of the buffer. Whenever a 1 is encountered in any channel on the tape, the signal output through the differential amplifier and rectifying slicer in the tape unit (paragraph 6-12b) is applied to the peak detector. During the tape signal, the gating level output of the detector is asserted. At peak signal return the detector produces a pulse which is gated through the capacitor-diode input gate by the level to set the corresponding flip-flop in the buffer. A detailed description of the Type 1539 circuit is given in paragraph 7-3d.

The presence of a character in CB is detected by the diode net in B2. When CB is clear, a ground level is present at 2H6J. As soon as any CB bit is set (indicating that a 1 bit has been encountered on tape) the level at 2H6J falls to -3 volts, setting program flag 2. This indicates to the computer that the first bit of a character has been encountered. The program must then compensate for tape skew by allowing enough time for the entire character to be loaded into CB. As character bits are loaded into the buffer, level changes through the parity nets (d below) check the parity of the character against that required by the parity flip-flop in the command register.

After the entire character has been loaded, the program must transfer the character to the in-out register with the read character instruction mrc. For this purpose the outputs of the CB data bits are connected to the input mixer. The first command pulse in mrc (also applied to the mixer) loads the contents of CB_{0-5} into IO_{12-17}. The second pulse then clears CB so that it is ready to receive the next character from tape.

d PARITY LOGIC - In the programmed system, reading and writing both use the same set of parity-generating nets (upper right, Figure 6-17). The bottom row of elements in the nets produces three outputs, each of which is the exclusive OR function of a pair of contiguous CB data bits. At the second level, a pair of cross-connected transistors XORs two of the first-level outputs. A third-level transistor pair XORs the second-level output with the remaining first-level output.

The third-level output and its negation are then ANDed with the ODD and EVEN outputs of the parity flip-flop. The level that appears at 2H8H is the correct parity of the character contained in CB: -3 volts for 1, ground for 0. In writing, the parity bit is generated during the 6-microsecond delay between the loading of CB and the writing of the character. The output at 2H8H provides the input to WB_p. When even parity is specified, the parity bit is 1 if the six CB data bits contain an odd number of 1s. Odd parity, however, requires that the parity bit be 1 when the data bits contain an even number of 1s.

The same output (2H8H) is used to check the parity of a character that is being read. The AND gates at the top of the parity logic compare this output with the actual state of CB_p. If the correct parity for the character differs from CB_p, the parity error level is asserted (A1). In the computer, this level gates the first command pulse in mrc. When the program transfers the character from CB to IO, the simultaneous assertion of PARITY ERROR causes MRC_7 to set program flag 4 (paragraph 6-3b).

6-12 LOCAL TAPE CONTROL TYPE 50

In addition to a tape transport and associated drive electronics, the Type 50 Tape Unit includes the DEC-designed local tape control, which comprises the read-write electronics. This unit is shown in two logic drawings, Figures 6-18 and 6-19. Figure 6-18 shows the TU status logic and the control logic both for the transport and for the read-write circuits. The read-write circuits themselves are shown in Figure 6-19.

a TRANSPORT LOGIC - Figure 6-18 shows the manual control panel at the left. The Type 50 Logic is in the center, and connections to the transport drive electronics are at the far right. Control inputs to TU from TC are at the far left. Most of these control functions are applied to TU through switching in the manual control panel. Tape motion is controlled by the circuits in the upper half of the figure: inputs at the left, logic at the lower right. Tape status levels provided from the drive electronics are sent to TC through the TU status logic. Figure 6-18 also shows the generation of read and write enable levels. These, however, are described with the read-write circuits (b below).

TC supplies control signals to all tape units through the TC bus. Signals are gated into the logic of the selected TU by the diode gates shown in A3 and B3. The gating level is derived from deck F of the auto/manual switch on the manual control panel (C2). When this switch is in manual (i.e. the unit is off line) the operation enable level is asserted automatically and control signals for the unit are generated from the other switches on the panel. For on-line operation, the switch must be set to automatic. Signals from the TC bus are then gated into the unit when the AUTO SELECT level is asserted through deck F. AUTO SELECT is derived from the address provided by TC. In the Type 52, this address is contained in the 3-bit unit address register (paragraph 6-5b), while in the Type 51 the address is contained in bits A and B of the command register (paragraph 6-11a). TC enables only one address line and selects the unit (or units) at which the unit selection thumbwheel setting matches the address (D2).

Further conditions on the selection depend upon the type of TC. The TC type is selected by the switch in D4, normally located on the bus socket panel at the bottom of the tape unit. However, in unit 1 of a programmed system, the Type 51 logic is mounted in the TU bay, and permanent wiring connections replace the switch. For Type 52 operation, deck B of the switch provides ground at 2G10E so AUTO SELECT at 2G6L is logically equivalent to the unit selection level at 2G10F. No further conditioning is necessary to enable the operation gates because no Type 52 Command Signals are generated unless the program loads a code into the command register.

For the Type 51, deck B switches the operate level to 2G10E so that AUTO SELECT enables operations only if the unit is selected and programmed to operate. This is necessary because only the mode of an operating characteristic, and not the presence of a command,

is determined by the Type 51 Command Register. For example, if forward is not asserted then reverse must be. Thus the deck B condition in AUTO SELECT allows the program to select a TU to examine status without putting it in operation.

The two speed lines to TU are not switched at the manual control panel (top, Figure 6-18). The speed logic is not normally used but is included in case a two-speed transport is available. Selection of speed 1 clears the speed flip-flop (A6); selection of speed 2 sets it. The flip-flop outputs supply speed signals to the drive electronics.

All other TC signals to the transport logic go through the auto/manual switch on the control panel. The signals through switch decks B and C (B2) control direction of tape motion. For manual control, these signals are duplicated from the manual direction switch (shown in the normal center-off position). Holding the switch up makes the forward contact; holding it down makes the reverse contact. Direction is selected within the logic if OPERATION ENABLE is asserted (B4). From the selection levels, a preforward and a prereverse level are generated. Note that prereverse is produced both by reverse selection and by the rewind function, since the tape must move in reverse while rewinding. Between the preforward and prereverse signal lines is a diode gate that ORs the negations of the two levels to detect a command conflict. Should both forward and reverse be selected simultaneously, no directional signal at all is sent to the drive electronics.

A further condition gates the forward motion signal: if writing is selected when the write enable ring is not in position, forward motion is inhibited. This prevents tape motion if the program attempts to write on a file-protected tape. Forward and reverse motion signals are supplied to the end point logic, as well as to the drive electronics.

The TC rewind signal is routed into the transport logic through deck D (B2) of the auto/manual switch. This signal is duplicated manually by a momentary ground from the rewind switch start contact. The rewind selection level is gated by OPERATION ENABLE and by the negation of the load point switch level from the transport. Thus the program (or the operator) can rewind tape only if it is not already at load point.

The rewind selection level sets the rewind flip-flop. In the 1 state this flip-flop produces the speed 6 signal for the dirve electronics (B5) and also selects reverse motion (B4). The high speed rewind continues until only 100 feet of tape are left on the takeup reel. Then

the full-reel signal disables speed 6 (B5) but reverse tape motion continues, returning to low speed. Finally, when the tape reaches load point, the rewind flip-flop is cleared, halting tape motion (C5).

In automatic operation rewind is terminated before completion if the computer is halted from the console. Operating the computer stop switch generates CLEAR TU, which produces AUTO CLEAR in all tape units. This clear returns all control flip-flops to the 0 state (speed, rewind and end point). In manual operation, rewind may be terminated by pressing the rewind switch down, thus generating AUTO CLEAR. In addition, whenever transport power is turned on or off at the control panel, all control flip-flops are cleared by the manual clear (D3). Under remote control, however, only AUTO CLEAR is available.

In addition to providing control signals to the drive electronics, the transport logic also provides status signals to the tape control. Some status levels are provided by the transport itself, as shown at the lower portion of the transport connector. These levels indicate whether or not the write enable ring is installed, and they provide information on tape position: load point, full reel, low reel and end point. Except for end point, the status logic uses all of these signals directly. If the tape is moving forward, the closure of the end point switch sets the end point flip-flop, which provides the end point condition even if the reflective strip moves beyond the end-of-tape sensor. Motion in the opposite direction through or from the end point then clears the flip-flop. The remaining transport status condition, rewind is provided by the rewind flip-flop because rewind is still in progress even after speed 6 is disabled.

In addition to the six transport status levels, two tape unit status levels are provided. The unit is ready for operations (D6, D7) if transport power is on and neither forward nor reverse motion has been selected. In a two-speed unit, TU is also unavailable for a specified period after a change from high to low speed to allow the capstans to slow down.

In order to prevent signal conflicts, the status levels are gated onto the TC bus only if the unit is in automatic and is selected (this also provides the additional condition that the unit is ready only if it is in automatic). Auto status is generated by the AND gate in C4. The auto condition for this gate is provided by deck G of the auto/manual switch, provided transport power is on (C3, C4). The selection condition is provided by the unit selection logic (D2). The signal from the unit selector passes through deck A of the TC selector. However, the position of the latter switch changes only the electrical configuration of the circuit - - the signals through both poles are logically equivalent.

The auto status level is applied directly to the TC bus (since it is asserted only for the selected TU) and is also ANDed with the other status levels to gate them onto the bus.

b TAPE WRITING AND SENSING - The levels controlling the read and write circuits are shown in Figure 6-18; Figure 6-19 shows the circuits themselves.

The write enable signal from TC is applied to TU through the manual control panel. If TU is in automatic and OPERATION ENABLE is asserted, the TC write enable signal produces the write selection level (B3). This level produces WRITE ENABLE (B8) provided the tape reel contains a write enable ring. The selection level is also ORed with a 10-millisecond delay level (B7). This delay is tirggered when the selection level is negated; thus WRITE ENABLE continues for 10 milliseconds after TC terminates the write operation. This assures that the tape will be erased as long as it continues to move (format control requires 10 milliseconds between the end of one operation and the beginning of another, paragraph 6-10e).

WRITE ENABLE is applied to two of the four inputs to each NRZ writer (upper half, Figure 6-19). The other two inputs to each writer are 1 and 0 outputs of the corresponding write buffer bit. While writing is enabled, tape magnetization in a given channel changes polarity each time the associated WB bit changes state. A circuit description of the Type 4514 NRZ Writer is given in paragraph 7-2.

The level that enables tape reading is generated by nets at the bottom center of Figure 6-18. Conditions included in the net depend upon whether the TU is included in a programmed or automatic tape system. In the Type 52 a TU can be selected without asserting any command signals. In the Type 51, command signals are necessarily asserted when a unit is selected; therefore the unit selection level is ORed with the operate level through deck B of the TC selector. To produce READ ENABLE, the output of this OR gate is then ANDed with another level that also depends upon the type of tape system. In the programmed system the tape cannot be read (to check parity) during the writing operation; reading is enabled only when the read signal from the command register is asserted. In the automatic system, reading is prohibited only when TU is rewinding.

READ ENABLE is applied to the rectifying slicers in the tape sensing circuits (lower half, Figure 6-19). Signals from tape are sensed by Type 1536 or 1549 Differential Amplifiers.

If READ ENABLE is asserted, signals from the amplifiers are passed through Type 1542 Rectifying Slicers to peak detectors associated with the read buffer. Besides the logic inputs there are two switch control inputs to the read circuits. Amplifier gain and slicer threshold level are both controlled from the gain, slice and test point panel. Paragraph 7-3 gives descriptions of the slicer and amplifier circuits.

TABLE 6-1

TYPE 52 TAPE SYSTEM, GENERAL FUNCTIONS

Clear Logic	
POWER TURN ON:	$\lfloor 0 \rightarrow$ FA, CLEAR TC, CLEAR TU
SC:	$\lfloor 1 \rightarrow$ FA_3, CLEAR TC
STOP:	CLEAR TC, CLEAR TU
CLEAR TC =	$\lfloor 0 \rightarrow$ TC BUSY, TC BUSY SYNC, TU OK, PARITY ERROR, CHAR SKPD, RCK ERROR, HSC LATE, HSC REQ, ILLEGAL, SAME UNIT, WRITE, WRITE SYNC, A, B, DWB, CA, UA, WB, RB, CR
Synchronization	
TP_4:	TC BUSY: $\lfloor 1 \rightarrow$ TC BUSY SYNC
	$\overline{\text{TC BUSY}}$: $\lfloor 0 \rightarrow$ TC BUSY SYNC
	$\overline{\text{TC BUSY SYNC}}$ (READY + SAME UNIT): $\lfloor 1 \rightarrow$ TU OK
	TC BUSY SYNC + $\overline{\text{(READY + SAME UNIT)}}$: $\lfloor 0 \rightarrow$ TU OK

TABLE 6-2

TYPE 52 TAPE SYSTEM,

IOT COMMAND PULSE OPERATIONS

2^{nd} Op Code	Operations
muf 76	$MUF_7 \cdot \overline{\text{TC BUSY SYNC}}$:
	$\xrightarrow{+1}$ PC
	$\xrightarrow{0}$ FA
	$\overline{\text{SAME UNIT}}$: $\xrightarrow{0}$ UA
	$\xrightarrow{0}$ WILL CONT, WILL CONT SAME
	$MUF_{10} \cdot \overline{\text{TC BUSY SYNC}}$:
	IO $\xrightarrow{1}$ FA
	SAME UNIT: $AC_{15-17} \xrightarrow{1}$ UA
	MB^{1}_{11}: $\xrightarrow{1}$ WILL CONT
	MB^{1}_{10}: $\xrightarrow{1}$ WILL CONT SAME
mic 75	$MIC_7 \cdot$ TU OK:
	$\xrightarrow{+1}$ PC
	$\xrightarrow{0}$ PARITY ERROR, CHAR SKPD, RCK ERROR, HSC LATE, HSC REQ, ILLEGAL
	$\xrightarrow{0}$ CA, RB, CR
	$MIC_{10} \cdot$ TU OK:
	IO $\xrightarrow{1}$ CA

Table 6-2, Type 52 Tape System, IOT Command Pulse Operations (cont'd)

2nd Op Code	Operations
	$MB \xrightarrow[8-11]{1} CR$ $\lfloor 1 \rightarrow$ TC BUSY $\lfloor 0 \rightarrow$ WB (see Figure 6-1)
mri 66	MRI_7: $\lfloor 0 \rightarrow CA$, $\lfloor 0 \rightarrow CR_{10}$ MRI_{10}: $IO \xrightarrow{1} CA$ MB^1_{10}: $\lfloor 1 \rightarrow CR_{10}$
mrf 67	Note: Both MB_8 and MB_{10} must be 0 or a maintenance instruction results, i.e. mrf = 72ab(0)067. MRF_7: $\lfloor 0 \rightarrow FA$ MRF_{10}: $IO \xrightarrow{1} FA$ Maintenance Instructions inr 72ab(0)267 $MRF_7 \cdot MB^1_{10}$: $\lfloor 1 \rightarrow$ HSC REQ ccr 72ab(1)067 $MRF_7 \cdot MB^1_8$: $\lfloor 0 \rightarrow CR$, $\lfloor 0 \rightarrow$ TC BUSY
mes 35	$3X \cdot TP_7$: $\lfloor 0 \rightarrow IO$ MES(TP_{10}): STATUS $\xrightarrow{1} IO$ For status bits refer to Table 4-1.

Table 6-2, Type 52 Tape System, IOT Command Pulse Operations (cont'd)

2^{nd} Op Code	Operations
mel 36	$3X \cdot TP_7$: $\overset{0}{\longrightarrow}$ IO
	MEL(TP_{10}): CA $\overset{1}{\longrightarrow}$ IO

TABLE 6-3

TYPE 52 TAPE CONTROL LOGIC LEVELS

$\overline{\text{NORMAL COMMAND}} = 0X0X + 01XX + 101X \cdot \text{WRITE LOCKOUT}$

$\text{ILLEGAL COMMAND} = \overline{\text{NORMAL COMMAND}} \cdot (101X + CR_9^1)$

$= 01XX + 101X \cdot \text{WRITE LOCKOUT}$

$\text{CHAR 3} = A^0B^0$

$\text{CHAR 1} = A^0B^1$

$\text{CHAR 2} = A^1B^0$

$\text{PARITY BIT} = DWB_0 \oplus DWB_1 \oplus DWB_2 \oplus DWB_3 \oplus DWB_4 \oplus DWB_5 \oplus CR_{11}$

$(\text{ADD} =) = \overline{\prod_{i=2}^{17} (CA_i \oplus FA_i)}$

$\text{WRONG PARITY} = RB_0 \oplus RB_1 \oplus RB_2 \oplus RB_3 \oplus RB_4 \oplus RB_5 \oplus RB_p \oplus CR_{11}$

CHAR MISSING = (>1 1/2 CHAR) (<3 1/2 CHAR)

INHIBIT = INITIAL READ DELAY + READ INHIBIT + LOAD POINT READ

INHIBIT + $\overline{\text{NORMAL COMMAND}}$

TABLE 6-4

TAPE UNIT LOGIC FUNCTIONS

Unit is on line in AUTO; off line in MAN.

Clear Logic

MANUAL CLEAR = ($\lfloor$ON$\rightarrow$ + $\lfloor$OFF$\rightarrow$) TRANSPORT POWER

MANUAL CLEAR: $\lfloor$0$\rightarrow$ SPEED, REWIND, END POINT

AUTO CLEAR = CLEAR TU + STOP MANUAL REWIND

AUTO CLEAR: $\lfloor$0$\rightarrow$ SPEED, REWIND, END POINT

Selection

(Unit n) SELECTED = [C (UA) = n] + [C(A,B) = n]
Type 52 Type 51

AUTO SELECT (Type 52) = SELECTED · AUTO

AUTO SELECT (Type 51) = SELECTED · AUTO · OPERATE

OPERATION ENABLE = AUTO SELECT + MAN

Read-Write

SEL WRITE = OPERATION ENABLE · TC WRITE ENABLE · AUTO

WRITE ENABLE = SEL WRITE · $\overline{\text{WRITE LOCKOUT}}$

(WRITE ENABLE continues for 10 ms after
SEL WRITE is negated)

READ ENABLE (Type 52) = AUTO SELECT · $\overline{\text{RWD SET REV}}$

READ ENABLE (Type 51) = AUTO SELECT · TC READ ENABLE

Table 6-4, Tape Unit Logic Functions (cont'd)

Speed

SEL SPEED 1 = OPERATION ENABLE · TC SPEED 1: $\xrightarrow{0}$ SPEED

SEL SPEED 2 = OPERATION ENABLE · TC SPEED 2: $\xrightarrow{1}$ SPEED

SEL RWD = OPERATION ENABLE (REWIND · AUTO + START MANUAL REWIND · MAN)

SEL RWD · $\overline{\text{LOAD POINT SW}}$: $\xrightarrow{1}$ REWIND

LOAD POINT SW: $\xrightarrow{0}$ REWIND

RWD SET REV = REWIND^1

SPEED 1 = SPEED^0

SPEED 2 = SPEED^1

SPEED 6 = REWIND^1 · $\overline{\text{FULL REEL SW}}$

Direction

SEL FWD = PREFORWARD

= OPERATION ENABLE (FORWARD · AUTO + MANUAL FWD · MAN)

SEL REV = OPERATION ENABLE (REVERSE · AUTO + MANUAL REV · MAN)

PREREVERSE = SEL REV + RWD SET REV

COMMAND CONFLICT = PREFORWARD · PREREVERSE

MOVE FORWARD = PREFORWARD · $\overline{\text{COMMAND CONFLICT}}$ ($\overline{\text{SEL WRITE}}$ + $\overline{\text{WRITE LOCKOUT}}$)

MOVE REVERSE = PREREVERSE · $\overline{\text{COMMAND CONFLICT}}$

Table 6-4, Tape Unit Logic Functions (cont'd)

Status

MOVE FORWARD·END POINT SW: $\xrightarrow{1}$ END POINT

MOVE REVERSE·END POINT SW: $\xrightarrow{0}$ END POINT

AUTO STATUS = SELECTED·AUTO·TRANSPORT POWER ON

READY STATUS = AUTO STATUS $\overline{(\text{PREFORWARD} + \text{PREREVERSE})}$

LOW REEL STATUS = AUTO STATUS·LOW REEL SW

FULL REEL STATUS = AUTO STATUS·FULL REEL SW

LOAD POINT STATUS = AUTO STATUS·LOAD POINT SW

END POINT STATUS = AUTO STATUS·END POINT[1]

WRITE INHIBIT STATUS = AUTO STATUS·WRITE LOCKOUT

REWIND STATUS = AUTO STATUS·RWD SET REV

TABLE 6-5

TYPE 51 SYSTEM OPERATIONS

General Functions

POWER CLEAR + STOP: $\lfloor 0 \rightarrow$ Command Register, CLEAR TU

SC: $\lfloor 0 \rightarrow$ CB, WB, Command Register

IOT Command Pulse Operations

2nd Op Code	Operations
mcb 70	MCB_7: $\lfloor 0 \rightarrow$ WB
	MCB_{10}: $\lfloor 0 \rightarrow$ CB
msm 73	MSM_7: $\lfloor 0 \rightarrow$ Command Register
	MSM_{10}: IO^1_{10}: $\lfloor 1 \rightarrow$ OPERATE = OPERATE
	IO^1_{11}: $\lfloor 1 \rightarrow$ REWIND
	IO^1_{12}: $\lfloor R \rightarrow$ DIRECTION = REVERSE (otherwise FORWARD)
	$REWIND^1 \cdot REVERSE = REWIND$
	IO^1_{13}: $\lfloor W \rightarrow$ DATA MODE = WRITE ENABLE (Otherwise READ ENABLE)
	IO^1_{14}: $\lfloor E \rightarrow$ PARITY = EVEN (otherwise ODD)
	IO^1_{15}: $\lfloor LO \rightarrow$ SPEED = SPEED #1 (otherwise SPEED #2)
	IO^1_{16}: $\lfloor 1 \rightarrow$ A
	IO^1_{17}: $\lfloor 1 \rightarrow$ B
	A^0B^1 = UNIT 1
	A^1B^0 = UNIT 2
	A^1B^1 = UNIT 3

Table 6-5, Type 51 System Operations (cont'd)

mwc 71	MWC_7: $\lfloor 0 \rightarrow CB$ MWC_{10}: $IO \xrightarrow[0-5]{1} CB$ After 6μsec. delay to generate parity bit CB_i^1: $\lfloor C \rightarrow WB_i$ $ODD \cdot \overline{\sum \oplus CB_{0-5}} + EVEN \cdot \sum \oplus CB_{0-5}$: $\lfloor C \rightarrow WB_p$
mrc 72	On detection of first bit of character: $\lfloor 1 \rightarrow PF_2$ PARITY ERROR = $ODD \cdot \overline{\sum \oplus CB_{0-5,p}} + EVEN \cdot \sum \oplus CB_{0-5,p}$ MRC_7: $CB_{0-5} \xrightarrow{1} IO_{12-17}$ PARITY ERROR: $\lfloor 1 \rightarrow PF_4$ MRC_{10}: $\lfloor 0 \rightarrow CB$, $\lfloor 0 \rightarrow PF_2$
mcs 34	$3X \cdot TP_7$: $\lfloor 0 \rightarrow IO$ MCS (TP_{10}): $\overline{STATUS} \xrightarrow{1} IO_{0-7}$ For status bits refer to mcs instruction (paragraph 4-6)

CHAPTER 7

CIRCUIT DESCRIPTION

7-1 GENERAL

This chapter includes descriptions of twelve tape system circuits not used in the computer. Descriptions of those circuits common to the tape system and the computer may be found in Chapter 10 of the basic PDP-1 Manual. Schematic diagrams of the twelve circuits described here are grouped at the rear of this manual, in order by type number. No figure reference is made in individual unit descriptions, but references to the applicable schematics are implied.

7-2 NRZ WRITER 4514

The NRZ writer contains four identical circuits which control write head current. These four circuits have dual inputs at terminals P-R, U-V, E-F and K-L; the respective outputs are at S, W, H and M. Each of the circuits constitutes an electronic switch. That is, the switch output current path forms part of the load circuit, and the input levels to each switch determine whether the load circuit is open or closed.

A load circuit is closed only when both inputs to the switch are at ground. If either or both of the inputs are at -3 vdc, the load circuit is open. The closed circuit load current is approximately 75 milliamperes. The four circuits are used in pairs, one pair with each center tapped write head inductor of a tape channel. The outputs of the paired circuits connect to opposite ends of the write inductor. The current return is made at the center tap. By using a pair of switch circuits and a center tapped inductor, the write current is made essentially bipolar. Specifically, the current that flows in one half of the write inductor is opposite in direction to the current that flows in the other half. Consequently, the tape can be magnetized in either of two directions, depending on which one of the pair of switches is closed.

The signals to one set of input terminals (R and V, for example) of a switch pair are complementary logic levels. Thus either one switch or the other is closed but not both. The tape is then magnetized in the appropriate direction. However, in the NRZ method of recording, the direction of magnetization has no logical significance. A change in direction of magnetization indicates a logical 1, whereas a constant direction of magnetization indicates a logical 0. The

remaining set of inputs (P and U, for example) are connected in parallel and used to gate the complementary inputs, enabling the write current for a legal write operation and inhibiting the write current at all other times.

Because the four switch circuits contained in the 4514 module are identical, the following description of the circuit with inputs P and R, and output S, adequately describes all four. The circuit is completed by connecting one end of a write head inductor to S and the inductor center tap to Z.

Normally, the write current flows through the emitter-collector path of Q4, through the write inductor across terminals S and Z, and through R15 and R16 to the -15 volt bus. This circuit opens when -3 vdc is applied to either or both input terminals P and R. Diodes D3-D4 and resistors R4-R5-R6 comprise a negative diode OR gate. Thus, whenever -3 vdc is applied to P or R, the output of the gate is -3 volts also. Resistor R4 and capacitor C2 couple the negative input to the base of transistor Q2, turning it on. At the turn-on of Q2, its collector rises to ground. R10 and D10 shift this ground level slightly positive at the base of Q4, cutting this transistor off. This opens the write current circuit. D8 clamps the Q4 collector to -15 volts during the collapse of current in the inductor.

The write circuit closes when ground inputs are applied to both inputs P and R. The D3-D4 diode gate output is then at ground, cutting off Q2. The Q2 collector falls to -7.5 volts. R10, D10, and C5-C6 couple this negative level to the Q4 base. Q4 turns on, completing the load circuit, causing current to flow in the write head inductor. R15 and R16 limit this current to 75 milliamperes. Although Q4 turns on, it is prevented from saturating by silicon diode D10 and germanium diode D9, since the lower forward voltage drop of the germanium diode keeps the Q4 collector slightly more negative than its base. This anti-saturation circuit allows faster turn-off of Q4 when the switch input falls to -3 volts.

7-3 TAPE SENSING CIRCUITS

This paragraph describes four circuits used in reading information from the tape. Differential amplifiers 1536 and 1549 and rectifying slicer 1542 are part of the Type 50 Read-Write electronics. However, Types 1536 and 1549 perform similar operations, and a tape unit includes only one or the other of these types. Peak detector and slicer 1539 is part of the tape control, either Type 51 or Type 52.

a DIFFERENTIAL AMPLIFIER 1536 - This module contains two identical differential amplifiers, the first consisting of transistors Q1 through Q6, the second of Q7 through Q12. Each amplifier provides high gain for balanced signals from a read head channel while discriminating against common mode noise. Negative DC feedback stabilizes circuit operation. The 1536 amplifiers are used in place of the 1549 amplifiers (b below) in some tape units.

Whenever the magnetic tape flux changes direction, indicating a logical 1, a 10 millivolt pulse appears across the signal inputs (H and K, for example). The input is balanced with respect to ground through a connection at the common input terminal (J, for example). Thus, when a 1 is read from the tape, a +5 volt pulse appears at one input, while a -5 volt pulse appears at the other. The duration of the pulse is about 66 microseconds. The balanced input gain of each 1536 amplifier is variable from 180 to 350 by potentiometer adjustment. Common mode gain is less than 1. The amplifiers overload when driven beyond 3 volts output (at either output terminal). A balance potentiometer varies one output up to 250 millivolts.

Since the two differential amplifier circuits contained in the Type 1536 Module are identical, the following description of the circuit with inputs H-J-K and outputs M-N adequately describes both.

Capacitors C1 and C2 AC couple the balanced input to the bases of transistors Q1 and Q2. The input is amplified at the collectors of Q1 and Q2. The stage generates a voltage gain for the out-of-phase input since R4 provides the principal emitter-to-emitter resistance of the stage and this resistance is lower than the collector-to-collector load. The stage common mode gain is less than 1 since R5 and R9 alone form the emitter resistance for the common mode signal and this resistance is higher than the collector load.

The collector outputs of Q1 and Q3 are amplified by two more differential stages, Q3-Q4 and Q5-Q6. The collector outputs of the final stage appear at M and N. A portion of the Q5-Q6 differential emitter load (potentiometer R23) is variable; decreasing this resistance increases the differential gain of the stage, increasing it decreases gain. Potentiometer R19, part of the Q6 collector load, varies the input K-to-output N gain and serves to balance the M and N outputs.

R6-R15 and R7-R16 close the output-input feedback loop. C4 and C5 remove any AC component in the feedback path. Because the voltage variation at any transistor base is reversed at the collector and the number of stages is odd, the feedback is negative.

b DIFFERENTIAL AMPLIFIER 1549 - The 1549 module contains two identical differential amplifiers. Each amplifier is similar in function and use to those of the 1536 module (a above) which replaces the Type 1549 in some tape units. Unlike the 1536 amplifiers, the 1549 amplifiers have fixed gain in all three cascaded stages. The gain of each stage is extremely high, and overall gain is reduced by employing negative AC feedback as well as DC feedback. A logic-level actuated relay switches two alternative configurations in the feedback loop, providing dual gain.

The first amplifier circuit includes transistors Q1 through Q7, and has inputs at terminals H and K, balanced about the common ground connection at J. Terminals M and N are the outputs. The second circuit includes Q8 through Q14, and has inputs U-V-W and outputs S and R.

A 10 millivolt, 66 microsecond pulse is applied to the differential amplifiers whenever a logical 1 is read from the associated tape channel. Amplifier gain is 400 when a ground level is applied to the gain selection input (E and Z for amplifiers 1 and 2). When -3 vdc is applied to these inputs, amplifier gain is 480.

Since the two differential amplifier circuits contained in the Type 1549 Module are identical, the following description of the circuit with inputs H-J-K and outputs M-N adequately describes both.

Capacitors C1 and C2 couple the balanced input to the bases of Q1 and Q2. The input is amplified at the collectors of these transistors. The balanced input gain is that of a grounded emitter stage. However, common mode gain is less than 1 since R8 makes the emitter impedance higher than the collector load when amplifying a common mode input. The second and third stages, composed of Q3-Q4 and Q5-Q6, respectively, similarly amplify the signal. C6 and R14, in the Q3-Q4 collector load, reduce the high frequency collector load of the second stage, thereby decreasing the high frequency gain. This attenuation provides stability to the amplifier circuit, which has a large amount of AC feedback.

The AC feedback circuit of the input H, output N channel consists of R18 in series with the parallel combination of R10 and C15. A similar combination of R12, R20 and C16 provide feedback in the input K, output M channel. Because the signal at any transistor base is reversed in polarity at the collector, and there is an odd number of stages, the feedback is negative. C15 and C16 increase the high frequency feedback, but contribute to amplifier stability by keeping the feedback negative.

The amplifier may be operated at either of two gains. Selecting the amount of feedback determines the gain. For low gain, a ground level is applied to input E, cutting Q7 off. Relay K1 de-energizes, opening the relay contact. Resistor R21, which shunts the feedback current, is thus removed from the circuit. Feedback is maximum, and consequently gain is at the low level. For high gain, -3 vdc is applied to E, saturating Q7. K1 energizes, closing the relay contact and thus inserting R21 in the feedback circuit. Feedback is minimum, and gain is at the high level. Diode D1 keeps the collector of Q7 from going more negative than -5 volts at the collapse of current in the relay coil.

The DC feedback circuit, consisting of R9-R11-R17-R19 and C4-C5, is similar to the feedback circuit of the Type 1536 Differential Amplifier (a above).

c RECTIFYING SLICER 1542 - The Type 1542 Module contains three identical rectifying slicers. One slicer is used in each tape channel read circuit, following the differential amplifier (either Type 1536 or 1549). The 1542 circuit rectifies the bipolar output of the differential amplifier, generating a negative output pulse for an input pulse of either polarity. However, no slicer output is generated unless the input exceeds a preset level. Thus a low level noise input cannot generate an output pulse.

The circuits are labeled A, B and C on the schematic. Since all three circuits are identical, only circuit A is described.

The balanced input is applied to the bases of transistors Q1 and Q2 at terminals E and F. The common emitter junction of Q1-Q2-Q3 follows the negative-going input once the input drives the base of Q1 and Q2 more negative than the base of Q3. The negative signal at the emitter junction drives the Q4 collector and is gated through to the Q4 emitter if -3 vdc is applied to the enable input Z. A ground level at Z prevents the signal from appearing at the Q4 emitter.

The Q4 gating circuit is not complete within the module but requires an emitter connection to +10 vdc through a 10K resistor. The next link in the tape read circuit, the Type 1539 Peak Detector and Slicer, furnishes the required gate termination. Consequently, noise induced on the connecting line between the 1542 output (in the tape unit) to the 1539 input (in the tape control) is shunted by the low emitter impedance of Q4.

Potentiometer R6 determines the slice level in conjunction with the margin input, W. This input is normally at +5 vdc, but may be varied ±5 vdc for marginal checking. With a +5 vdc input a W, R6 varies the slice level from approximately -0.1 to -0.5 vdc. The slice voltage is usually set at 10% of the rectified input signal, which is of the order of -3 volts peak.

In the quiescent state voltage divider R7-R4-R1 determines the voltate at the bases of Q1 and Q7. The negative end of the divider is tha arm of potentiometer R6; this varies the negative end voltage from -0.75 to -0.3 vdc. The positive end of the divider is the margin input W. Since Q1 and Q2 do not conduct until their bases are more negative than the base of Q3, the difference between the quiescent Q1-Q2 and Q3 base voltages is the slice level. Silicon diode D3 clamps the base of Q3 to -0.75 vdc, so the slice level is determined only by the margin input and the setting of R6.

Assume that the margin input and the setting of R6 make the bases of Q1 and Q2 0.5 volts negative. An input pulse, when applied to E and F, is AC-coupled to the bases of Q1 and Q2 by C2 and C1. If the polarity of the pulse is such that the Q1 base is driven positive and the Q2 base is driven negative, Q1 reamins cut off, but Q2 conducts when the negative input exceeds -0.25 volts. Consequently, the common emitter connection of Q1-Q2-Q3 follows the Q2 base. If the polarity of the input were reversed, Q1 would conduct, so that a negative signal is developed from either input signal polarity. Capacitor C3 de-couples the signal from the inputs to the other two circuits in the module.

When input Z is at ground (inhibit), D1 clamps the base of gate transistor Q4 to the ground input, holding the no-signal operating point of Q4 just out of saturation. The negative-going signal at the Q4 collector drives the transistor further out of saturation. Collector impedance is high, and there is no change in emitter current, so the gate voltage gain is 0. However, if the Z input is -3 vdc (enable), D1 disconnects the Q4 base from the -3 vdc input, and the R10 current holds Q4 solidly in saturation at the no-signal operating point. For any negative collector input up to -3 volts, the gate transistor operates in saturation, and the collector input impedance is approximately the emitter load resistance. Voltage

gain is unity, coupling the signal to output L. D1 clamps the base of Q4 so that it can go no more negative than -3 volts; collector voltages more negative than -3 volts; collector voltages more negative than this take Q4 out of saturation and are clipped at the Q4 emitter.

Silicon diodes D3 through D9, and resistors R18, R20 and R21 form a negative DC supply. The D3 cathode furnishes -0.75 vdc to the slice control potentiometers and the bases of the slice transistors. The D4 cathode furnishes -3.75 vdc to the collectors of the rectifying transistors.

d PEAK DETECTOR AND SLICER 1539 - The Type 1539 Module contains two identical circuits, the first including transistors Q1 through Q6 and the second Q7 through Q12. When pulsed by a 1542 output, each circuit generates two outputs, a level and a pulse. The level and pulse combine in a Type 4127 Negative Capacitor-Diode Gate to generate a gate output pulse which sets a read buffer flip-flop, indicating that a 1 has been read in the corresponding tape channel.

A Schmitt trigger circuit generates the pulse from the differentiated input. Thus as the input goes positive, the Schmitt circuit flips to its alternate state and its output rises to ground. When the input peaks, the differentiated signal begins to go negative, driving the Schmitt trigger back to its original state, with output at -3 vdc. The negative-going transition marks the input peak and sets the associated read buffer flip-flop through the 4127 capacitor-diode gate. However, the pulse output is susceptible to noise, so a slicer is included in the 1539 circuit. This slicer generates a -3 vdc enable level for the 4127 gate provided the driving pulse is above a minimal amplitude. If the input does not exceed the slice level, the level output remains at ground, inhibiting the gate. The following description refers to the circuit with input F, level output J and pulse output R.

The slicer consists of transistors Q2 and Q3, the Schmitt circuit of Q5 and Q6. Q1 amplifies and inverts the input; its output drives both the slicer and pulse generator (Schmitt circuit). Q4 is a grounded base amplifier. Its emitter input impedance combines with C5 to differentiate the Q1 output. The differentiated signal at the Q4 collector is AC-coupled by C6 to the pulse generator.

In the quiescent state, R38 and D1 bias the Q1 base at 0.3 vdc so that the Q1 collector current is about 1 ma and the collector voltage is about -14 vdc. R5 supplies current to

saturate Q2. D3 clamps level output J at the collector of Q2, to ground. The saturation of Q2 holds the Q3 emitter at ground. A +0.75 vdc from supply R37-D15 makes the Q3 base more positive than the emitter so Q3 is cut off. R12 and R14 limit the collector current of the grounded-base amplifier Q4 to 2 ma. R11 furnishes another 1/3 ma to collector load resistor R10 so that the Q4 collector is at -8 vdc. When potentiometer R13 is set full CCW, Schmitt trigger Q5-Q6 free runs. In normal operation however, R13 is rotated clockwise so that Q5 is on and Q6 is off. The pulse output, at the collector of Q6, is then clamped to -3 vdc (from supply R36, D11 through D14).

A negative pulse from a Type 1542 Rectifying Slicer is applied to input F (K is tied to F in order to provide the dc return for the 1542 output gate, c above). C2 couples the inverted positive-going pulse to the base of Q2. When the base of Q2 becomes more positive than 0.75 volts, Q3 turns on, cutting Q2 off. D3 clamps output J at -3 vdc. When the input signal falls off so that the Q2 base again becomes more negative than the Q3 base, J rises to ground, ending the gate.

During the gate interval, the rising Q1 collector output is differentiated by C5 and applied to the emitter of Q4. Conduction through Q4 increases, making its collector more positive. C6 couples the rise to the base of Q5. Conduction through Q5 decreases and Q6 turns on. D5 clamps the pulse output at ground. Positive feedback through R11, C6 and Q5 continues to hold Q6 off even though the differentiated signal is falling off. However, when the input signal peaks, the Q4 emitter goes negative, cutting Q4 off. Its collector goes negative, turning on Q5. The Schmitt circuit flips to its original state, with Q6 cut off. The pulse output at R drops from ground to -3 vdc.

When the level output rises to ground, the peak detector and slicer completes its return to the quiescent state. Outputs H and P are used only as test points.

7-4 LOGIC CIRCUITS

The logic circuits described here are used in the tape controls but not in the tape unit. Of the three circuits, only 4-bit counter 4215 is used in the Type 51 Control. All three are used in the Type 52 Control.

a BINARY-TO-OCTAL DECODER 4151 - Both outputs of each of three flip-flops are applied to the input terminals of the binary-to-octal decoder. The decoder has eight output

terminals numbered 0 through 7. For any given combination of flip-flop states, only one corresponding output of the decoder is a ground level. The remaining seven outputs are -3 vdc.

The decoder circuit is composed of eight identical parts, one for each octal character. Each part is a three-diode negative AND gate (logically equivalent to a positive OR gate), and a logical inverter. For example, in the octal 0 part, diodes D1-D2-D3 and resistor R9 make up the AND gate. If the anode of any gate diode is ground (positive), the gate output is ground also. Silicon diodes D33 and D45 shift the gate output ground level sufficiently positive to cut off transistor Q1. D25 then clamps the decoder 0 output at R to -3 vdc. When the anodes of all three gate diodes are at -3 vdc (negative), the gate output disconnects from the gate input, and the current in R9 biases Q1 on. The 0 output is then grounded.

The eight gates are each connected to a different set of input lines (bottom, 4151 schematic). These connections are arranged so that each gate responds to only one of the eight possible combinations of 0s and 1s that can be generated by three flip-flops. That is, for any given combination of states of the three input flip-flops, only one gate receives -3 vdc levels at all three input diodes, thus turning on the associated transistor. Every remaining gate has at least one ground input. Consequently, the seven associated transistors remain cut off, producing -3 vdc levels at all but one of the eight decoder outputs.

The 1 and 0 outputs of the flip-flop representing the least significant of the three bits being decoded are connected to inputs L and K, respectively. Flip-flop outputs for the next more significant bit are connected to J and H, those for the most significant to F and E. The input connections for each gate represent the 3-bit number being decoded. For example, the gate which decodes octal 7 (= binary 111) is connected to the 1 outputs of all three flip-flops. With all three diodes at -3 vdc, the gate transistor is turned on, decoder output 7 rises to ground.

b DUAL FLIP-FLOP 4202 - The Type 4202 Flip-Flop Module contains two buffered flip-flops (A and B), two pulse inverters, twelve positive capacitor-diode gates, two negative AND gates, and a -3 vdc supply. Flip-flop A consists of transistors Q3 and Q4, with output buffers Q2 and Q5. Q1 inverts a negative pulse applied to its base; the resulting

positive pulse at the Q1 collector sets A. Flip-flop B contains Q8 and Q9, with output buffers Q7 and Q10. Pulse inverter Q6 permits a negative pulse to set B.

The combination C2-R4-D4, located at the shift right 0 input M, forms a typical capacitor-diode gate. D1-D2-R1 forms one of the AND gates; D16-D17-R22 forms the other. The -3 vdc supply is D29-D30-D31-D32-R43.

The two flip-flops contained in the 4202 module have individual complement and direct set inputs, and a common clear input. A gated set to each flip-flop is also provided for the individual read-in of 1s. Gated shift right and shift left inputs permit the use of the flip-flops as stages in a shift register. Internal connections for both types of shift between flip-flops A and B are made within the module. Module 4202 flip-flops are used in the data word buffer in the Type 52 Tape Control. This application requires only the complement, direct set, clear and shift left inputs.

A positive-going pulse from a Type 4127R Capacitor-Diode Gate applied to N or T complements flip-flop A or B, respectively. A positive pulse from a Type 4128 Capacitor-Diode Gate at E or Y sets flip-flop A or B. Both flip-flops are cleared by a Standard DEC 0.4-microsecond Positive Pulse at S. The gated shift left input R is driven by a similar pulse. The 0 and 1 inputs at U and X, which gate the shift pulse, are complementary levels (ground and -3 vdc). Ground assertion enables the gate. Because FFA is similar to FFB, the following description of FFB describes both.

Flip-flop B may be stable in either the 1 or 0 state. Assume that it is in the1 state, so that Q8 is on and Q9 is off. With Q8 on, its collector is grounded, and voltage dividers R36-R37 and R41-R42 bias the bases of Q9 and Q10 positive, holding both transistors off. Q7 and Q8 are held on by base currents flowing from the Q9 collector resistor, R32, through input resistors R28 and R33. The Q9 collector is held at approximately -4 volts. Since Q7 is saturated, the 0 output W is ground. With Q10 off, the 1 output V is clamped at -3 vdc by D28. C19 and C29 synchronize level changes of the 0 and 1 outputs. The flip-flop state changes to 0 when a positive pulse drives the Q8 base positive, cutting it off. Because the flip-flop is symmetric, it remains stable in the 0 state with Q7-Q8 off and Q9-Q10 on. In the 0 state, W is at -3 volts and V is at ground. A positive pulse at the base of Q9 returns the flip-flop to the 1 state.

Flip-flop B is complemented when a positive-going pulse from a Type 4127R Gate is applied to T. Internal gates C18-R26-D21 and C28-R39-D27 direct the input pulse to the base of the on flip-flop transistor, either Q8 or Q9. As a result the on transistor turns off, and the flip-flop assumes the complementary state. For instance, if the flip-flop is initially in the 1 state, C28-R39-D27 blocks the pulse from the base of Q9, while C18-R26-D21 gates the pulse to the base of Q8. As a result the input pulse complements the flip-flop to the 0 state. The gating is done in the following manner.

Assume that flip-flop B is in the 1 state and a pulse is applied to T. C18 differentiates the leading edge of the pulse, generating a positive pulse referenced to the Q7 collector level (0 output) at the anode of D21. Since this level is ground, the positive pulse forward-biases both D21 and D22. Consequently Q8 is cut off and flip-flop B changes to the 0 state. Silicon diode D22 raises the voltage level necessary to forward-bias the base of Q8, thus preventing small noise pulses from clearing the flip-flop. Although C28 couples the input pulse to the anode of D27, this pulse is referenced to the -3 volts at the flip-flop 1 output. D27 is not driven sufficiently positive to become forward biased, so the pulse is blocked from the base of Q9. If the flip-flop is in the 0 state prior to the application of a pulse to T, the reference levels of the two diode gates are reversed so that the complementing pulse is passed to the base of Q9, placing the flip-flop in the 1 state.

The shift left input R operates like the complement input in that capacitor-diode gates direct the input pulse to one or the other of the flip-flop transistors. However, the gate reference levels are taken from the appropriate bit to the right in the data word buffer. Therefore, FFB assumes the state of this bit when the shift left input is pulsed, rather than complementing itself. Furthermore, the shift left pulse is also applied to FFA, being directed to one of the FFA transistor bases so that A assumes the state of B.

Assume that the register bit whose contents are to be shifted into FFB contains a 1, and that B contains a 0. The 1 state of the register bit is asserted by a ground input at X and a -3 vdc input at U. When the positive shift left pulse appears at R, gate C27-R38-D26 passes the pulse to the Q9 base, but gate C21-R30-D19 blocks the pulse from the Q8 base. Consequently, B assumes the 1 state. While FFB is changing state, gate C6-D7-R3 passes the pulse to the base of FFA transistor Q3 (the gate reference level derived from the 1 output of B, is ground, since B is in the 0 state when the shift pulse occurs). Gate C12-R17-D8

blocks the pulse from the Q4 base because the gate reference level is -3 volts, derived from the 0 output of B. Flip-flop A thus assumes the 0 state of B. The delay in change of reference level of each gate is long enough so that there is no ambiguity in sensing the state of a flip-flop at the same time that its shift input is pulsed.

Flip-flop B is set by applying a positive pulse from a Type 4128 Capacitor-Diode Gate to input Y. D25 and D24 couple the pulse to the base of Q9. D25 isolates Y from the other inputs to the base of Q9, while the forward-bias threshold of silicon diode D24 prevents small noise pulses from setting the flip-flop. D14-D7 and D15-D22 couple a pulse at input S to A and B, clearing both flip-flops.

c FOUR-BIT COUNTER 4215 - This module contains four flip-flops for use as counter bits. The four flip-flops, A, B, C and D, are logically independent. They may therefore be connected in any logical configuration. When connected as a counter, the significance of each flip-flop as a counter bit is determined entirely by the external connections. The module also contains 12 positive capacitor-diode gates (C14-R30-D1 and C1-R7-D5 are two examples) and a negative DC supply. The supply, consisting of diodes D21 to D24 and resistor R29, provides -0.75 vdc at the cathode of D21 and -3.0 vdc at the cathode of D24.

Flip-flops B, C and D, have complement inputs at terminals R, K and E, respectively. Flip-flop A has separate set and clear inputs, but this flip-flop may be complemented by applying a signal to both inputs simultaneously. Flip-flop C has an inhibit level input at M. When the inhibit is applied, C cannot be complemented from 0 to 1, although it may still be complemented from 1 to 0.

A positive pulse (such as a Standard 0.4-microsecond DEC Pulse or the positive-going output of a pulse inverter) or a positive 3-volt step (such as the change in the 1 output of a less significant counter bit when it goes from 1 to 0) drives the complement and clear inputs. A -3 vdc level at M enables the inhibit to FFC. Carry propagate time per bit is 50 nanoseconds. The following description of flip-flop A also applies to the other three flip-flops.

A positive pulse applied to the 1 input W (set one) or the 0 input (set zero) reaches the base of the associated flip-flop transistor only if the transistor is on. The pulse changes the flip-flop state by turning the on transistor off. When A is 1, a pulse at V passes through capacitor-diode gate C15-R31-D4 to the base of Q2, turning Q2 off. This switches the flip-flop

to the 0 state. Pulses at V now have no further effect, since gate C15-R31-D4 is disabled when A is 0. However, gate C14-R30-D1 is enabled when A contains 0, so a positive pulse at W passes to the base of Q1, turning Q1 off and switching A back to the 1 state.

If W is jumpered to V, the combination is a complement input. When this input is pulsed, gates C14-R30-D1 and C15-R31-D4 steer the pulse to the base of the on transistor, turning it off, so the flip-flop switches state. Gate C1-R7-D5, associated with terminal X, is permanently enabled because R7 is returned to -0.75 vdc. Thus a positive pulse at X clears FFA directly.

R7 is returned to -0.75 vdc rather than to ground in order to prevent spurious noise from affecting the flip-flop. Since signal voltages are greater than -0.75 vdc, they pass through D5, but small noise signals are blocked. The gate time constant (R7 x C1) is longer than that of the other two capacitor-diode input gates because a 1.0-microsecond pulse is used to clear the counter. This allows carries to die out before the pulse ends.

Terminal R (add FFB) is the complement input to B. A positive pulse at R is applied simultaneously to two capacitor-diode gates. These gates, C16-R32-D6 and C17-R33-D9, steer the pulse to the base of the on transistor, turning it off. When B is 1, gate C17-R33-D9 is enabled, and a positive pulse at R clears the flip-flop. Conversely, when B is 0, gate C16-R32-D6 is enabled, and a positive pulse at R sets it. The complement input to flip-flop D, terminal E (add FFD), operates similarly.

Terminal K (add FFC) is the complement input to FFC. Pulses at K are gated by two capacitor-diode gates, like the two input gates of flip-flop B, described above. One of the two FFC input gates is returned to the Q6 collector. This gate, C19-R35-D14, is enabled when FFC is 1. Then a positive pulse at K is gated to the base of Q6, turning it off and clearing the flip-flop. The other gate, C18-R34-D11, is returned to the output of a negative OR gate, of which the Q5 collector is one input, rather than directly to the Q5 collector.

This OR gate, composed of D25, D26 and puller resistor R38, functions similarly to the gates in diode 1110 (paragraph 10-3a, PDP-1 Manual). The anode of D11 is at the more negative level of either the Q5 collector voltage or the inhibit level at M. When the M input is ground, flip-flop C functions like the others in the module, and is complemented by each

positive pulse at K. However, if the input at M is -3 vdc, the pulse at K cannot reach the Q5 base, even though the Q5 collector is ground (the flip-flop is in the 0 state). On the other hand, the path to the Q6 base is not affected by the input at M, so the flip-flop may be complemented from 1 to 0 regardless of the inhibit level.

7-5 INTEGRATING DELAY 4303

This module contains two monostable multivibrators, two difference amplifiers (slicers), three inverters, a positive capacitor-diode gate and a negative DC supply. These components form a single circuit. The Type 4303 has flip-flop type logic level outputs. When the circuit is in the 1 state, the 1 output is at -3 vdc and the 0 output is at ground. In the 0 state, the output polarities are reversed. When an input (there are three) is pulsed, the circuit assumes the 1 state, having previously been in the 0 state. The circuit returns to the 0 state after a selected delay, which begins with the termination of the input signal.

The two multivibrators include transistors Q2-Q3 and Q10-Q11. Q5-Q6 form one slicer, Q7-Q8, the other. The three inverters are Q1, Q4 and Q9; the capacitor-diode gate is C1-R1-D1. The negative DC supply contains diodes D9 through D16 and resistor R28. Voltage levels of -0.75 vdc, -1.5 vdc, -3 vdc, -4.5 vdc, -5.25 vdc and -6 vdc are tapped from the supply at the cathodes of D16, D15, D13, D11, D10 and D9 respectively.

Three inputs are provided at terminals K, S and R. The signal input at K may be either a DEC Standard 0.4-microsecond Negative Pulse or a negative level. The input at S may be either a DEC Standard 0.4-microsecond Positive Pulse or positive-going level change; this pulse is gated through to the base of Q2 by a ground level at terminal T. Input R requires a positive pulse such as the output of a positive capacitor-diode gate similar to C1-R1-D1. The 1 and 0 outputs are W and U.

The delay is variable from 3.4 microseconds to 0.9 seconds in five overlapping ranges. Connection of one of five internally contained capacitors into the circuit determines the delay range. C7 is connected internally to give the shortest range. Connecting C6, C8, C9 or C10 (E, F, H or J) to ground (D) increases the range by successive factors of approximately 10. Potentiometer R10 determines the delay within each range if Y is jumpered to X. Alternatively, the delay may be determined by an external potentiometer connected between Z and X.

In the quiescent state, Q1, Q3, Q4, Q5, Q8, Q9, and Q10 are off. Q2, Q6, Q7 and Q11 are on. Voltage divider R2-R3 shifts the ground level at input K positive, biasing Q1 off. Multivibrator Q2-Q3 is in its stable state with Q2 held on by base current flowing through R5, and with Q3 held off by voltage divider R8-R9. With the Q2 collector at ground, voltage divider R11-R12 biases Q4 off.

In slicer Q5-Q6, Q5 is off and Q6 is conducting. D6 clamps the Q6 collector at -0.75 volts, holding Q6 out of saturation. The common emitter connection of NPN transistors Q5 and Q6 follows the voltage (-1.5 volts) at the base of Q6. Consequently Q5 is cut off.

The other slicer transistors, Q7 and Q8, are on and off, respectively. The series combination of potentiometer R10 and resistors R13 and R14 draws sufficient current from the base of Q7 to saturate that transistor, even if the potentiometer is set at its maximum resistance. The saturation of Q7 holds the common emitter connection of Q7 and Q8 at -5.25 volts, the Q7 collector voltage. The more positive voltage (-4.5 volts) at the Q8 base holds Q8 at cut-off. With Q8 cut off, Q9 is back-biased through R19 so Q9 is cut off also. Since Q9 is cut off, the voltage divider composed of R23 and the parallel combination of R21 and R24 holds Q10 off. Consequently, multivibrator Q10-Q11 is in its stable state, with Q10 off and Q11 on.

The circuit is triggered from the quiescent state when an appropriate input at K, R or S drives the Q2 base positive. Multivibrator Q2-Q3 flips to the temporary state with Q2 off and Q3 on. D4 clamps the Q2 collector at -3 volts. R11 and C5 couple this -3 volt level to the base of Q4. The saturation of Q4 grounds its collector.

The grounded Q4 collector drives the bases of Q5 and Q7 positive. The signal divides at the two bases in order to perform two functions. The signal at the Q7 base goes to output multivibrator Q10-Q11, driving this multivibrator to its temporary state. The Q5 base forms part of the feedback loop that returns the signal to input multivibrator Q2-Q3, returning this multivibrator to its quiescent, or stable, state.

As the Q7 base goes positive, Q7 turns off and Q8 turns on. The common emitter connection of the two transistors rises to the Q8 base voltage. Q8 turns on but does not saturate because its rising collector voltage is clamped at -5.25 volts by the turn-on of Q9. Transistor Q9 does saturate, and its collector drops to -5.25 volts. R20 couples this voltage to the Q10 base, turning Q10 on. Multivibrator Q10-Q11 flips to the temporary state, with Q10 on and Q11 off. The output is now in the 1 state, with W at -3 volts and U at ground.

In the feedback loop to input multivibrator Q2-Q3, R14 drives C7 (and any other capacitor that may be in parallel with it) toward ground. This is the charge mode. When this voltage reaches approximately -1.5 volts, Q5 saturates heavily, forward-biasing both its base-emitter and base-collector junctions. The larger part of the base current flows to the collector so that the Q5 collector is more negative than its emitter. Consequently, Q6 is cut off. The Q6 collector goes positive, forward-biasing D5 and cutting off Q3. Q2 turns on, provided that it is not held off by a continuing negative level at K.

The turn-on of Q2 grounds the Q4 base, cutting Q4 off and beginning the discharge mode. Before the Q7 collector can return to its quiescent state, C7 (and any additional capacitor in parallel with C7) must discharge through resistor R13 and potentiometer R10. As C7 begins to discharge, Q5 turns off and Q6 turns on. D5 becomes back-biased, disconnecting R16 and R17 from the base circuit of Q3. However, the grounded collector of Q2 continues to hold Q3 off.

When the base of Q7 becomes more negative than -4.5 volts, Q7 turns on and Q8 turns off. The -6 volts from the negative supply back-biases Q9 through R19, turning Q9 off. The rise in voltage at the Q9 collector cuts off Q10, returning the output multivibrator to its stable state. The outputs at W and U return to the 0 state (W at ground and U at -3 volts), indicating the end of the delay.

If the input to Q1 is held at -3 vdc, C7 charges up to -1.5 volts and stays there. Thus the output remains in the 1 state. The output returns to the 0 state after a fixed interval following the removal of the negative Q1 input. When input pulses arrive at shorter intervals than the delay period, the output similarly remains in the 1 state, returning to the 0 state after a fixed interval following the last pulse.

7-6 CRYSTAL CLOCK 4407

This module contains a crystal oscillator, an oscillator output amplifier, a Schmitt trigger circuit and an output pulse amplifier. The crystal oscillator includes transistors Q1, Q2 and Q3; Q4 is the oscillator amplifier. The Schmitt circuit includes Q5 and Q6. Transistor Q7 is part of the output pulse amplifier.

The 4407 module generates DEC Standard 0.4-microsecond Pulses, either positive or negative, at a frequency determined by the series resonance of the oscillator crystal. In the Type 52 Tape Control, Clock 4407 has a crystal with a series resonance of 15 kc.

Terminal E is the negative output, and F is the positive output. If F is jumpered to ground, a 15 kc train of negative pulses appears atE. Conversely, with E grounded, a train of positive pulses appears at F.

Positive feedback from the collector to the emitter of Q1 sustains oscillations in the crystal oscillator. The feedback path goes from the collector of Q1 through crystal CR-1, the two emitter followers Q2 and Q3, to the emitter of Q1. The oscillator output is taken from the collector of Q3.

The circuit oscillates (unity gain around the feedback loop) at a frequency such that the highest proportion of signal voltage is fed back to the Q1 emitter. Crystal CR-1 has minimum resistance at series resonance. Thus the positive feedback is maximum at the CR-1 series-resonant frequency. Gain around the feedback loop is less than unity for other frequencies. Oscillation is therefore sustained only at the series-resonant frequency, i.e. 15 kc.

The parallel resonant circuit C1-C2-L1 is tuned in the vicinity of 15 kc. The increased impedance of this tuned circuit at resonance compensates for the loss of Q1 collector load impedance at the series resonance of CR-1. This compensation near resonance helps to stabilize the Q1 gain, and assists in tuning the oscillator to the desired frequency. Zener diodes D1 and D2 make the operating voltages of the oscillator circuit independent of supply variations.

The oscillator output to the Q4 base is amplified at the Q4 collector and applied to the Q5 base. The Schmitt circuit, Q5 and Q6, converts the 15 kc sine wave into a 15 kc square wave. The output pulse amplifier, Q7, then converts the square wave into a 15 kc train of DEC Standard 0.4-microsecond Pulses.

The Schmitt circuit and output pulse amplifier are similar to the circuit contained in module 4410 (paragraph 10-9e, PDP-1 Manual). Each time the sinusoidal output from the Q4 collector drives the Q5 base more negative than -2 volts, Q5 turns on and Q6 turns off. The Q6 turn-off generates a pulse at output E-F. Since Q6 turns off and on once for each cycle of the oscillator, the pulses are produced at the oscillator frequency.

7-7 POWER CONTROLS

The power controls are relay units that provide for remote turn-on of ac power to the magnetic tape equipment from the PDP-1 computer, as well as local turn-on independent of the computer. Circuit breakers are included in the controls to protect against overload.

Two types of power control are described, the Type 811 and the Type 822. The 811, with minor modifications, serves as the power control for either the Type 51 or Type 52 Magnetic Tape Control. One of the modifications is the omission of relay K3, which is not used in either application. The 822 is the Type 50 Tape Unit Power Control. The latter is a more extensive modification of the 811, and in some tape units is designated on the control itself as the 811B.

a POWER CONTROL 811 - As a power control for the Type 51 and Type 52 Tape Controls, the 811 includes line filters FL1 to FL4, a 20-ampere circuit breaker CB1, a two-position single-pole switch S1 and two relays K1 and K2. The contacts of both relays are normally open. K1 is energized by 115 vac while K2 is energized by -15 vdc. S1 is the 811 power mode switch (local/remote).

Provided that the circuit breaker is closed, line power applied to the control input is coupled to the output if contacts A and B of K1 are closed. Thus the application of power to the output depends on K1 being energized. The way this is done depends on the type of tape control with which the 811 is used.

For use with the Type 51 (upper half, Figure 7-1), Cinch Jones terminal 6 is connected to 9, so that the K1 energizing current must flow through contacts C of K2. Terminal 3 is connected to 5, placing S1 in series with the K2 coil. Depending on the power mode, the input at terminal 1 or 2 energizes K2 and in turn K1, applying power to the control output. The input at 1 is -15 vdc from the computer, and the input at 2 is -15 vdc from the 728 power supply of tape unit 1 (i.e. the unit located in the same bay as the Type 51 Control). Thus when S1 is in remote, the tape control turns on and off with the computer. In local, however, the tape control turns on and off with the unit 1 read-write electronics (b below).

When the 811 is used with the Type 52 (Figure 7-2), terminal 3 is connected to 8, 6 to 7, and 1 to 7 placing S1 in parallel with contacts K2C. The parallel combination is placed in series with the K1 coil by connecting 7 to 9 through the power switch on the Type 52 Indicator Panel. Thus the power switch must be closed or the tape control cannot be on.

When the power switch is on, the method of applying power to the system depends on the 811 power mode. The local position of S1 shorts terminal 3 to 1, bypassing the K2C contacts and turning on the tape control. When S1 is in remote, the direct path between 1 and 3 is open, and K2 must be energized in order to apply power. K2 is energized by -15 vdc

from the computer, applied to terminal 5. Thus the tape control goes on and off with the computer.

b POWER CONTROL 822 - The 822 includes line filters FL1 to FL4, a 20-ampere circuit breaker CB1, a three-pole power mode switch S1 (local/remote) and five relays K1 to K5. Figure 7-3 shows the power control wiring for use with the Type 50. For convenience, the 822 is also shown in the lower half of Figure 7-1; this figure shows both power controls that are mounted in unit 1 of the Type 51 System.

The contacts of all relays are normally open. K1 and K5 are energized by 115 vac while K2, K3 and K4 are energized by -15 vdc. The Potter isolation transformer, transport interlock, and manual control panel transport power switch (off/remote/on) complete the power control circuitry. The switch is momentary contact in the on position and has two contact forms, A and B. The form A contacts are closed only in on while the form B contacts are closed in remote as well as on.

The 822 switches the 115 vac line input to two outputs, one to the tape transport and the other to the fan and 728 power supply for the Type 50 Logic. Input power flows through CB1 and the Potter transformer to contacts A and B of K1 and K5. When K1 is energized, its contacts supply power to the transport through pins 33 and 34 of the Potter connector. When K5 is energized, its contacts supply power to the Type 50.

The interlock, transport power switch S4, relays K2 and K3, in conjunction with K1 itself determine whether K1 is energized and power is supplied to the transport. K4 governs the energization of K5. The power mode switch S1 determines the -15 vdc source for the K2 and K3 coils. In local, voltage comes from the tape unit 728 supply; in remote, voltage comes from the Tape Control (Type 52) or the Computer (Type 51). The latter also provide -15 vdc to K4 in remote mode. In local, the switch bypasses K4 so that K5 is energized directly, turning on the Type 50 provided only that the circuit breaker is closed.

Assume that S1 is in remote, connecting -15 vdc from the remote input at terminal 1 to the K2 and K3 coils through the lower set of contacts and to the K4 coil through the upper set of contacts. Assume also that S4 is in remote so that the form A contacts are open but the form B contacts are closed. When the remote input turns on, -15 vdc appears at terminal 1. Relay K4 energizes, closing the K4 contacts, and placing 115 vac across the K5 coil.

K5 energizes, turning on power to the Type 50. The K2 coil is ac-coupled to the -15 vdc input by C1 and momentarily energizes, closing the K2 contact in series with the form B contacts of S4, the interlock and the K1 coil. If the interlock is closed, K1 energizes, providing power to the transport.

The C contact of K1 together with the K3 contact (closed since K3 is energized by the -15 vdc input) bypasses the K2 contact so that transport power continues after K2 opens. The dual path is provided as a safety feature. If the interlock is open, as it is when tape is being loaded or if it breaks, completing the tape loading procedure cannot start the transport. S4 must first be placed in its momentary contact on position closing the form B contacts that bypass the relay contacts. A consequence of this arrangement is that if transport power is interrupted by turning S4 off, returning to remote does not allow the transport to turn on without a transient at terminal 1. As in the case of the open interlock, S4 must be turned on.

When S1 is in local, the upper section of the switch disconnects the K4 coil from any input, but the middle section closes, bypassing the K4 contact so that K5 is energized directly. With the turn-on of the power supply, -15 vdc appears at terminal 2. The lower section of S1 couples the input to the K2 and K3 coils. The conditions for supplying power to the transport are the same as before.

CHAPTER 8

MAINTENANCE

8-1 SPECIAL TOOLS AND TEST EQUIPMENT

Paragraph 11-1 of the basic PDP-1 manual lists the special tools and test equipment recommended for efficient maintenance of DEC digital logic systems such as the Types 51 and 52 Magnetic Tape Controls for the Type 50 Magnetic Tape Unit (transport and read/write electronics). The following special tools and test equipment are recommended in addition to the basic list.

10 ampere variable transformer	General Radio Variac or equivalent
0-16 ounce spring scale	Chatillon No. 516-500 or equivalent
0 to 2 pound spring scale*	Chatillon No. 516-1000 or equivalent
0-20 pound spring scale*	Chatillon No. 719-20 or equivalent
Set of feeler gauges*	Range 1-20 for 1-20 mils, 1/8" leaf width
Set of extension frames	Potter Nos. M3323-801 and M3323-802
Head cleaning fluid*	"Vithene D" or duPont Freon TF or Ampex Head Cleaner
Allen wrench set*	Must include 0.050" size: Craftsman No. 46681 or equivalent
1-1/2" machinist's square*	Starrett No. 20 or equivalent
Offset screwdriver	Any medium-blade, short-offset type
Toothpicks	The round, sharply pointed kind (for probing airholes)
Vacuum cleaner	Any canister type with a narrow suction nozzle
Two spare bulbs for the tape unit panel*	...
Magnetic tape unit calibrator	A suitcase-size substitute for the tape control, developed by DEC for use in calibration and maintenance of Type 50 tape units

*These items included with the DEC magnetic tape unit calibrator.

The DEC magnetic tape unit calibrator (Figure 8-1) replaces the Type 51 or Type 52 magnetic tape control for off-line calibration of the Type 50 tape unit. The calibrator simulates the 51 or the 52. To use the calibrator, disconnect the 50-conductor cables from J50-4B and J50-4A. If the tape unit bay does not contain a Type 51 control, connect the 50-conductor cable from the calibrator to J50-4A, forming an independent calibrator-tape unit system. For a tape unit containing the Type 51 control, connect the calibrator cable instead to J50-4 (this plug is in the same position as J50-4B in other tape units).

The tape unit connected to the calibrator is off-line and may therefore be tested or calibrated independently. The remaining tape units are still on-line so the calibration of any given tape unit does not involve downtime for the whole magnetic tape facility.

Since the calibrator is generally used with an oscilloscope, it is provided with straps to hang it from thebar on a scope cart. Oscilloscope test points are available on the calibrator front panel for observation of the rectified and sliced read signal from each of the seven tape channels. The write density clock output, the write density output and the start/stop frequency output are also available.

The calibrator includes an instruction sheet for operation of the calibrator with the Type 50 transport. The sheet includes information on preliminary connections and the function of all calibrator controls and indicators, and gives a procedure for setting the Type 50 start/stop time using the calibrator.

Figure 8-1 shows the calibrator front panel. The calibrator logic (Figure 8-2) includes four DEC logic modules and an indicator driver board. For writing on tape, the clock (D2) may be set, using the coarse and fine speed controls, to a pulse repetition frequency between 5 and 50 kc. The clock pulse output complements the WRT flip-flop through an inverter. This flip-flop, with the seven write channel switches (1,2,4,8,A, B and C), simulates the TC write buffer. If a given write channel switch is turned off, one side of the pair for the channel is returned to -15V through a 10K resistor (A1 to A6). When the switch is turned on, however, the pair for that channel receives the 1 and 0 outputs of the WRT flip-flop. Thus, turning <u>all</u> switches on is equivalent to writing all ones in every line on the tape. The write density may be varied, using the coarse and fine speed controls, from 20 microseconds to 200 microseconds per line. Normally the density is set to 66 microseconds by observing, with an oscilloscope, the CLK pulse train output (available at the jack, lower right, calibrator panel). The interval between clock pulses is the same as the interval between lines written on the tape.

To provide forward and reverse pulses for measuring stop and start times, the function selector is set to start/stop so that the WRT 1 output complements the SS flip-flop. The SS 1 and 0 outputs, however, can be asserted through the inverters (C3) only while WRT is 1. The inverter outputs 2F3P and 2F3L provide short alternating ground pulses to the forward and reverse command lines, as shown on the calibrator timing chart (Figure 8-3). In the start/stop position, the speed range deck of the function selector provides a 5 to 50 cps adjustment range for the clock output frequency. The coarse and fine speed controls may therefore select a forward/reverse tape movement frequency from 1.25 to 12.5 cps.

8-2 EQUIPMENT LAYOUT AND WIRING

The complete module layout for tape controls 51 and 52, and for the Type 50 transport logic, is shown in Figure 8-4. The five mounting panels at the left and the top two at the right show all module locations for the Type 52 automatic tape control. Panels 2G and 2H (bottom right) show the module locations for the Type 50 logic and for the Type 51 programmed tape control. The appropriate block schematics are referenced both by figure number and by DEC drawing number in the box shown at the left of each mounting panel.

Figures 8-5 and 8-6 show the name and origin or destination of the signal on each connection through the three taper pin blocks at the bottom of a tape unit bay. Figure 8-5 shows the taper pin layout of the Type 50 tape unit alone; Figure 8-6 shows the layout for a 50-51 combination in a single bay. The three blocks (numbered 1 to 3 from bottom to top) are each divided into twenty columns lettered A to W. The three pins of each column are bused together to form a permanent connection.

Figure 8-5 shows the TC bus from the preceding TU connected from J50-4A to the middle row of each taper pin block. The TC bus to the following TU on line is connected from the bottom rows to J50-4B. The TC bus thus runs continuously through every tape unit from J50-4A through the taper pin blocks to J50-4B. Connections to the tape unit logic in each bay are made from the top rows. Block 1 connections include tape unit status signals; operate and read enable levels from the Type 51 control (when it is used); the auto turn-on level; and, at columns N and R, the +10 and -15 volt power levels required by the unit calibrator. Block 2 connections include the seven read channels, tape movement command levels, and write enable and unit selection levels. Block 3 connects 1 and 0 outputs of the write buffer bits, speed selection levels, and ground bus.

Connections to the taper pins in unit 1 of a Type 51 system differ somewhat because many of the levels and signals must originate or terminate in the Type 51 control which is mounted in the same bay (Figure 8-6). As in the standard Type 50 taper pin configuration, the top rows provide connections to the tape unit logic, the manual control panel and the power controls. Similarly, the middle rows provide connections to the TC bus for the following TU. Note, however, that block 2 has only three connections for unit selection levels because three tape units are the maximum which may be controlled by the Type 51. Connections from the tape units to the PDP-1 and from the TC bus to the TC are made at the bottom rows. Block 1 provides TU status levels directly to PDP-1 through J51-4; connects the auto turn-on level from PDP-1 to both power controls; and connects the operate and read enable levels from the TC logic to the TC bus. Connections at taper pin blocks 2 and 3 have the same function as those in the standard tape unit, but the bottom rows provide connections directly to the TC instead of the TC bus.

In all tape units of a Type 51 system, the middle rows provide TC bus connections to the following TU, while the bottom rows provide connections from the previous TU (or from TC and PDP-1). This results from the reversed cable connections (see Figure 3-3) and contrasts with the configuration shown in Figure 8-5 (see also Figure 3-2) where the middle rows are the TC bus in from previous units, and the bottom rows are the TC bus out to following units.

Figure 8-7 is the wiring diagram for the manual control panel at the top of each tape unit. The figure shows the panel as seen from the rear, with each component shown in its approximate location. The figure also gives the wire color and pin number of all connections made to the panel, and includes a cable schedule for P50-13, which connects the panel to the tape unit logic and the TC bus.

8-3 RECOMMENDED SPARE PARTS

The most economical quantity of spare parts to be stocked depends on the requirements of the individual user. If the tape system is used only one shift a day, spare stocks need not be as large as would be necessary for a tape system used two or three shifts a day. If minimizing downtime is a financial consideration, the stock of critical module spares should be enlarged over that necessary in more relaxed installations. Paragraphs a and b discuss recommended spare allowances for DEC modules and for the Potter Tape Transport. Paragraph c lists recommended mechanical spares.

a MODULE SPARES - For single shift applications one spare module of each type usually constitutes a sufficient stock of spares. Many modules used in either Type 51 or Type 52 tape systems are also used in the standard PDP-1. The following table lists recommended additional spares by module type for tape systems used with the PDP-1. The modules listed are recommended in addition to the minimum stock of spares listed in Table 11-2 of the basic PDP-1 manual. Type 51 system users should stock the additional spares listed under Types 50 and 51 of the table. Type 52 system users should stock the additional spares listed under Types 50 and 52.

TAPE SYSTEM SPARE MODULE LIST

TYPES 50 AND 51

1536 or 1549	1542	1539	4215	4514

TYPES 50 AND 52

1536 or 1549	1539	1542	4127R	4151
4202	4213	4215 4514	4303	4407

For tape system applications in which downtime must be minimized and for installations used more than one shift a day, additional stocks of the more complex modules are desirable. Since the more complex modules may require considerable time for diagnosis and repair, insurance (in the form of additional spares) may be provided against the possibility of two failures within the time required for repair of a single module. The following table gives additional spares recommended for applications requiring minimal downtime or multiple shift operation. To ensure minimum downtime the spares listed below should be stocked in addition to those listed above. The following list applies to either type of tape system.

RECOMMENDED ADDITIONAL SPARES

1539	1549*	1542	4603

*If used. In systems using the Type 1536, no additional spares are recommended.

b TAPE TRANSPORT SPARES - The Potter Instrument M9061I-1 Tape Transport is a particularly complex piece of equipment. Removal and replacement of any part requires a high degree of technical skill as well as complete familiarity with the peculiarities of the transport. The following table lists transport spares recommended for installations in which down-time of any transport must be kept to an absolute minimum. Transport parts and assemblies not listed in this table should not be removed or installed except by DEC or Potter personnel.

Potter Part No.	Part	Recommended Quantity
A415884	Low tape sensor shoe	2 per unit
B416146	IBM end-of-tape sensor bulb and tube ass'y	2 per unit
S235-3	Rubber expansion ring for IBM reel hub	2 per installation

For installations including more than two Type 50 tape units, stock the following spare modules for the Potter electronics:

Potter Part No.	Part	Recommended Quantity
M3323-202-Y/Z	Solenoid driver for FWD and REV pinch-rollers	1
M3323-301-Y/Z	Capstan speed-change relay	1
M3323-101	Servo-Motor control	1
M3323-601	Servo-modulator amp reference supply	1
M3323-701	IBM photoelectric end-of-tape sensor amplifier	1

c MECHANICAL SPARES - The following table lists mechanical spares recommended for a Type 51 or Type 52 system.

Part		Recommended Quantity
Rotron Venturi:	Muffin fan with muffin clips	1

10" x 10" x 2" EZ Kleen Filters	1 per bay
Type 418 Super Filter Coat	2 pints

8-4 ADJUSTMENT AND CALIBRATION

The procedures described in this section should be performed as corrective maintenance only and are not intended as routine periodic checks.

Adjustments for the Type 51 programed tape system involve the tape sensing circuits, described in a below, and a 4301 delay. Type 52 automatic tape system adjustments involve the tape sensing circuits and three adjustable delays - modules 1304, 4301 and 4303. Adjustment of the 4301 is described in the PDP-1 manual; the same procedure applies to the 1304. Adjustment of the 4303 delay is described in b below.

a TAPE SENSING CIRCUITS - The sensing circuits for each channel are adjusted separately while all ones are being read from the tape. Each system includes four differential amplifier modules which may be either Type 1536 or Type 1549; three gatable rectifying slicers Type 1542; and four peak detector and slicer modules Type 1539. All differential amplifiers in a given system are of one type (1539 or 1549), but since a given system may use either, procedures are described below for adjusting both.

The differential amplifiers are in locations 2G21 to 2G24; the rectifying slicers are in 2G20 to 2G18 of every tape unit bay (bay 2). In the 51 control, the peak detector and slicer modules are in 2H21 to 2H17 of tape unit 1. These slot listings are in order from channel 1 to channel 7. In the 52 control, the peak detector and slicer modules are in 1E16 to 1E19 (i.e. in bay 1, the tape control bay). All of these modules contain circuitry for more than one channel. Adjustments are made by means of screwdriver trimpots; access holes in the aluminum frame are provided at the rear of each module. Within each module adjustment holes for the lower numbered channel are at the top; those for higher numbered channels, below.

The Type 1536 differential amplifier has two pairs of access holes. In each pair the top trimpot is the gain adjustment; the bottom, the balance adjustment for a given channel. The 1542 module contains three gatable rectifying slicers. The three holes at the rear of the module provide access to the three slice potentiometers.

When making adjustments to Types 1536, 1549 and 1542, signal from tape is observed at a test point provided on the Type 1539 peak detector and slicer. Each 1539 contains two circuits. The test point for the lower numbered channel is pin H; for the next channel in sequence, pin Y. The adjustment procedures are as follows:

Systems Using Type 1536

1. Locate the slice trimpot on the 1542 module corresponding to the channel to be adjusted; check that it is fully counterclockwise. This provides minimum slice level.
2. Connect the vertical input of a calibrated oscilloscope to the corresponding test point (pin H or Y of a 1539). Sync the scope internally and sweep so that three positive-going pulses are displayed.
3. Read a tape with all ones.
4. Locate the gain control on the 1536 differential amplifier corresponding to the desired channel. Adjust the trimpot so the signal is approximately 7.5 volts peak-to-peak. (Gain adjustments are made through the upper access hole in each pair.)
5. Adjust the balance potentiometer so that the three scope pulses are of equal amplitude (balance through the lower access hole in each pair).
6. Readjust the gain so that the scope pulses are 7.5 volts peak-to-peak. The pulses should have a well-defined peak and should not be clipped.

   This completes the adjustment.

Systems Using Type 1549

1. At the upper left of the gain, slice and test point panel, switch to low gain (down).
2. Connect the signal lead of a calibrated oscilloscope to the test point (pin H or Y of a 1539) corresponding to the channel being adjusted. Sync the scope internally and sweep so that three positive-going pulses are displayed.
3. Read a tape with all ones.
4. Locate the slice trimpot on the corresponding 1542 module. Adjust the trimpot so that the scope pulses are as close to 7.5 volts peak-to-peak as possible. Turning the trimpot counterclockwise increases pulse height.

5. If the gain on all channels is substantially low, repeat the procedure with the gain switch in high gain position. The pulses should have a well-defined peak and should not be clipped.

   This completes the adjustment.

Type 1539 Adjustments

The Type 1539 is adjusted for proper operation when the tape system leaves the factory. It is strongly recommended that the 1539 be adjusted only by DEC personnel.

There are two peak detector and slicer circuits on each 1539 module. Each circuit includes a Schmitt trigger which produces a level output (at pin R or pin T) indicating presence of a signal from the tape. The threshold levels for the two triggers are adjustable through access holes at the rear of the module.

The following procedure should be followed, preferably by DEC, only if troubleshooting indicates that the fault must lie in the 1539.

1. Remove the 1539 module corresponding to the channel to be tested.
2. Using clip leads, ground pin D and provide power to the module at the +10 volt A and B lines and the -15 volt C line.
3. Drive the 1539 input (pin F for the upper circuit, Z for the lower) with a 2-volt peak-to-peak sine wave input of 27.5 kilocycles.
4. Display the input and pulse output (R or T) on a dual channel scope.
5. Adjust the trimpot so that the negative-going transition of the pulse output occurs about 0.5 microsecond after the negative input peak. Rotating the trimpot clockwise increases the lag.
6. Remove the input, leaving the oscilloscope connected to the output at pin R or T. Make certain that the Schmitt trigger is not free-running. When proper adjustment is made, the trigger should not run free.
7. If the trigger runs free in the absence of an input signal, turn the trimpot clockwise one turn. If this does not prevent free-running, the module must be shipped to DEC for adjustment or repair; a spare module should be placed in the control.

8. If this slight clockwise rotation (step 7) stops free-running or if the module is stable after completing step 5, remove all test leads and replace the module in its proper location.

This completes the adjustment.

b INTEGRATING DELAY 4303 - Three integrating delays are used in the 52 control. Locations of these delays are 1B13, 1C25 and 1D25. All three delays are shown in Figure 6-16C5. Normally, the delay provides a -3 volt logic level at pin U and ground at pin W. When triggered, a delay changes state and the levels at U and W are transposed. If trigger pulses arrive at intervals shorter than the delay time, the delay remains in the ONE state, i.e. ground at U and -3 volts at W.

During normal read and readcheck operations, the read strobe triggers all three delays at intervals of 66 microseconds. This interval is shorter than the delay period for any of the three; thus, while reading a record with no missing characters, all delays remain in the ONE state. Since the function of these delays in format control is to signal the absence of characters on the tape (paragraph 6-10c), these delays must be adjusted while reading a special test tape containing one-word records each followed by the characteristic 3/4" end-of-record gap. Directions for preparing such a tape are given in section 8-6.

Normally the Type 4303 does not need frequent adjustment. Adjustments should be performed as part of corrective maintenance and not as routine periodic checks. The following adjustment must be made, however, whenever a spare module replaces one in the machine and whenever a 4303 is used in a mounting panel location different from that for which it was adjusted.

The 4303 delay range is determined by selecting one of five capacitance values. Pin D is the capacitor selection terminal. The shortest delay range is determined by making no connection to D; jumpering D to E, F, H or J selects four successively longer delay ranges. Fine adjustment of the delay is made at the screwdriver trimpot behind the access hole at the rear of the module. In all three locations, D is jumpered to E on the module connector. The proper delay range is therefore determined automatically when the module is plugged in. After the module is inserted, use the following procedure to make the fine adjustment at the screwdriver trimpot.

1. Connect the A trace vertical input of an oscilloscope having a dual-trace preamp to 0 output pin U of the 4303 to be adjusted. Adjust the A trace vertical controls to display a 3-volt positive pulse.

2. Connect the B trace vertical input to input pin K. Adjust the B trace vertical controls to display 2.5-volt negative pulses.

3. Read a tape with continuous sequences of single three-character words, each followed by an EOR gap.

4. If the dual trace preamp chop frequency is fast enough, set it to chop between the A and B inputs; if not, use alternate sweeps.

5. Sync the scope on the first negative pulse at the 4303 input (pin K), to display a single positive level on the A trace. The A trace signal should rise from -3 volts to ground just after the first of the three pulses shown by the B trace. The level should remain at ground during the second and third B trace pulses, and for a period following the third pulse determined by the delay interval.

6. Adjust the sweep to display conveniently the interval starting at the third pulse of the B trace and ending at the fall in level of the A trace. This time interval is the delay period.

7. If the time interval between the last input pulse (B trace) and the fall in level at the delay output (A trace) is within ± 5 microseconds of the delay interval given in Figure 6-16 for the corresponding location, the delay does not need adjustment. If the delay is incorrect by more than this tolerance, rotate the trimpot at the rear of the module frame to adjust the delay period. Counterclockwise rotation increases the delay.

   This completes the adjustment.

8-5 PREVENTIVE MAINTENANCE

This section lists recommended preventive maintenance procedures for the standard Type 50 tape unit, including the Potter transport, and for the Type 51 or 52 tape control. These procedures should be performed according to a regular schedule determined approximately as in the following paragraphs, which are based on a normal eight-hour shift. At installations where the tape system is used overtime or for more than one shift a day, the following procedures

should be followed at appropriately more frequent intervals. Each schedule below presents procedures first for the Type 50 and Potter transport, then for the 51 control and, finally, for the 52 control.

Every Day (Operator's Maintenance)

1. Clean the entire front panel and all surfaces contacted by the tape, such as guide rulers, pinch rollers, trough guides, capstans, and the inside surface and cover of the vacuum buffer, with "Vithene D" or duPont Freon TF.
2. Using a cotton swab such as a Q-tip or equivalent, clean the record/playback head surface making absolutely sure that no red oxide residue remains to prevent good tape contact with the head.
3. Clean drag pads with brush or compressed air.
4. Clean the bleedholes in the vacuum buffer with a toothpick or similar instrument.

NOTE

It is impossible to place too much emphasis on cleanliness of all tape handling surfaces. A large proportion of read and readcheck malfunctions can be traced to a fouled transport.

5. Check that all cooling fans (bottom of each bay) are operating properly and check for free flow of air.
6. For systems using the 51 control, run a simple write and readcheck program using techniques given in section 8-6. Log all malfunctions (the typeout is sufficient.)
7. For systems using the 52 control, run an appropriate write and read check routine. Log all malfunctions so that a malfunction history exists if troubleshooting becomes necessary.

Every Week

1. Repeat the daily procedure if not already performed.
2. Vacuum clean the back of the transport.

THE FOLLOWING PROCEDURES SHOULD BE PERFORMED ONLY BE QUALIFIED TECHNICIANS OR BY DEC PERSONNEL:

Every Two Weeks

1. Repeat the daily and weekly procedures if not already performed.

2. In the process of cleaning, examine the drag pads for excessive fouling or wear. If either drag pad is badly worn, replace both and perform the complete start/stop adjustment procedure (see Every Month, step 13, below).

Every Month

While performing any of the following procedures, listen for abnormal bearing noise. Bearing replacement should be performed only by Potter or DEC personnel.

1. Repeat all procedures listed in previous schedules if they have not already been performed.

2. Inspect the drive belts (back of transport) for evidence of wear. Replacement of drive belts should be done only by DEC or Potter personnel.

3. Check all supply voltages to the Potter electronics using procedures given in paragraph 6-6-12 of the Potter Manual.

4. At the manual control panel turn the TRANSPORT POWER switch OFF. Remove fuses F9 and F10 in the Potter electronics. Switch the 822 power mode switch to REMOTE. At the manual control panel, switch control to AUTO. Connect the unit calibrator cable to J50-4A at the tape unit bus socket panel. Do not turn tape unit power on with the calibrator.

5. With the upper tension arm fully extended, attach a 0 to 2 pound scale and pull the arm into the roller bridge. Measure the force required to keep the arm in the center of its swing. The force should measure 8 ounces.

6. Release the tension arm abruptly; it should come to rest against its stop immediately. If it bounces, adjust the tension arm dashpot according to the procedure given in paragraph 6-6-3 of the Potter Manual.

7. Using the procedure of Potter Manual paragraph 6-8-3-2B, check the reel brake tension.

8. With a 0 to 20 pound spring scale, push down on each pinch roller. The force required to engage the pinch roller should be 2 to 3 pounds.

9. Turn TRANSPORT POWER to REMOTE. Push calibrator REMOTE POWER switch to ON and direction switch to FWD. The lower pinch roller should engage the capstan. With the 0 to

20 pound spring scale, measure the force required to lift the pinch roller from the capstan. A 6 to 8 pound force should be required. Switch direction to REV and repeat the measurement on the upper pinch roller.

10. If necessary, adjust the pinch roller driving force according to paragraph 6-6-4D and adjust the return force according to paragraph 6-6-4C of the Potter Manual. The following steps should be performed only if the pinch roller drive force and return force are within tolerance.

11. Check the transport reel servo systems as follows:
Turn TRANSPORT POWER to OFF. Replace fuses F9 and F10 in the Potter electronics. Thread a full reel of tape in the normal manner (paragraph 5-4) and restore transport power. Run about 50 feet onto the takeup reel. Set the calibrator clock to its slowest pulse rate and switch to STOP-START. Slowly increase the clock rate up to a 10-cycle forward-reverse frequency. If the tension arms swing to within 3/8" of their stops or to within 3/8" of the roller bridge, the transport servo system is defective and must be adjusted according to paragraph 6-8-3-2 of the Potter Manual.

12. Check the end-of-tape sense amplifier adjustment (part of the Potter electronics) according to Potter Manual paragraph 10-7-4. The top trimpot on the amplifier module is the load point adjustment; the bottom trimpot, the end point adjustment.

13. Using the calibrator, rewind the tape and write ones for the length of the reel (or use a test tape prewritten with all ones).

14. Run about 50 feet of tape onto the takeup reel. Set the calibrator direction switch to the neutral position and switch to STOP-START.

15. With an oscilloscope, observe the start/stop signal at the calibrator jack and set the clock to a pulse width of 100 milliseconds.

16. Sync the scope on the calibrator forward signal at the test jack on the gain, slice and test point panel. The scope trace should present one of the patterns shown in Potter Manual Figure 6-2. By changing the triggering polarity on the oscilloscope fine trigger adjustment, either of the two patterns of Figure 6-2 can be presented.

17. In Figure 6-2 (Potter Manual) the upper photograph shows the start velocity profile; the lower photograph, the stop profile. Start time is measured from the beginning of the

observed read signals. Stop time is measured from the beginning of the trace to the end of the observed read signals. The start time should be 1.8 ± .1 milliseconds. The stop time should be 1.2 ± .1 milliseconds.

18. If the forward start time is incorrect, the gap between the pinch roller and the capstan head must be adjusted. Switch the calibrator from STOP-START to NORMAL. Loosen the Allen screw on the bracket directly under the pinch roller. Adjust the screw located in the center of this bracket (the one locked by the Allen screw). Retighten the Allen screw and again check the start and stop times.

19. The stop time is adjusted by increasing or decreasing the pressure of the drag pads. The drag pad pressure is adjusted (with a screwdriver) by turning the shaft in which the drag pad springs are mounted. Loosen the Allen set screw that locks the shaft, and turn the slotted shaft very slightly to adjust the drag pad force. Counterclockwise rotation increases the force. Do not forget to retighten the Allen setscrew.

20 Trigger the oscilloscope from the REVERSE test point. Again measure start and stop times; if necessary adjust the top pinch roller clearance and the lower drag pad pressure.

21. Perform step 3 of paragraph 11-5c in the basic PDP-1 manual. This completes the monthly preventive maintenance procedure.

8-6 MAINTENANCE PROGRAMS

This section discusses available programs both for the Type 51 and Type 52 tape systems, and describes two maintenance programs. Paragraph a discusses general programming considerations; paragraph b describes a simple but very useful routine for the Type 52 system, as well as suggested examples for preventive maintenance checkouts and for console troubleshooting. For the Type 51 system a considerably more involved program (paragraph c) allows generation of complex iterative loops using a repertoire of 30 pseudo instructions. Paragraph c also gives some examples of the use of this Type 51 test program to construct short maintenance routines.

For the Type 52 system the fully comprehensive maintenance and checkout program is Maindec 21. This program allows a complete testing of all Type 52 logic and contains routines enabling a thorough checkout of all Potter transport mechanical functions. Program tapes and documentation for Maindec 21 are available from DEC on request.

Readers are assumed familiar with the contents of Chapters 4, 5 and 6 of this manual as well as Chapters 3 and 5 of the basic PDP-1 manual. There is no substitute for thorough knowledge of the logic. For example, consider the following short routine for the Type 51 system:

Load AC from TW Set program flag 2	lat u stf 2	76 2212
Rotate AC and IO left 9 places	swap	66 3777
Rotate AC and IO left 9 places		66 3777
Magnetic tape write character	mwc	72 0071
Magnetic tape read character	mrc	72 0072
Skip on zero program flag 2	szf 2	64 0002
Halt	hlt	76 0400
Jump (to beginning)	jmp.-7	60 *

*address of the load AC instruction

This routine may be placed in any eight consecutive memory locations to test continuity of all cabling between the PDP-1 and the Type 51 logic. It depends on the fact that the write instruction loads the character buffer from IO_{0-5}, allowing the subsequent read to transfer the same 6-bit character back into IO_{12-17}. Thus during the time the loop is in operation, the IO indicators show the character code in bits 0 to 6 and 12 to 17. Familiarity with only the instruction list would not be sufficient background for generating this loop. Note also that if the MRC_7 pulse fails, the computer halts with program flag 2 set.

a GENERAL PROGRAMMING CONSIDERATIONS - Paragraph 11-8d(1) of the basic PDP-1 manual (p. 11-43) presents the basic concepts involved in construction of diagnostic and exercise loops for use in troubleshooting and signal tracing logic systems. When making up such loops for either tape system, it is most important to consider the PDP-1 and the magnetic tape equipment together as an integrated data handling system. The magnetic tape equipment should never be regarded merely as a piece of in-out gear incidentally attached to the PDP-1. Diagnostic and exercise loops of the type described in

the basic PDP-1 manual are very useful in troubleshooting intermittent malfunctions because, using such loops, a given subsection of logic can be repetitively pulsed for an indefinite length of time. During repetitive performance of a loop, various troubleshooting procedures (e.g. aggravation or signal tracing) may be used to isolate a malfunction. The particular instructions used in the loop must bear some relation to the section of logic suspected.

The following considerations affect programming of magnetic tape operations:

1. The Potter transport has a speed tolerance of ±3%. Writing a record containing a given number of words therefore requires a length of tape which varies by as much as 6%. Accordingly, it is impossible to replace a record on the tape by another record containing the same number of words and still be assured that end-of-record gaps are within tolerance. Each write command is therefore assumed to be writing the last record on tape.
2. When programming the Type 52 system, a write command with equal initial and final addresses writes 3/4" blank tape.
3. If the selected end-of-record action is Early Completion and Continue (bits 10 and 11 of the muf instruction contain 3), a write command with equal initial and final addresses writes two blank 3/4" gaps.
4. Characters containing all zeros must not be written in even parity. The read sequence interprets the resulting blank space as a missing character. Arbitrary lengths of blank tape may be generated by specifying appropriate initial and final addresses and writing all zeros in even parity.
5. With the Type 52 system, if it is desired to read through the end of one record and into the next, muf must specify Early Completion and Continue. At the end of the first record the tape control continues through the gap to process the next record, requesting HSC transfers until the addresses become equal. Since an inadvertent muf or mic instruction can interrupt processing of the second record, a new muf and mic should be given during the 2-millisecond interval following the first completion pulse.
6. Using given initial and final address settings, any number of small blocks may be read from the tape by repeating the original muf instruction followed by mel and

the original mic instruction. After mel, IO contains the current address; mic then resets CA to this address. The tape stops at the end of the first record following that in which the current and final addresses become equal.

7. If Early Completion and Continue is specified with a space command, do not fail to provide new initiating instructions within the allotted 2 milliseconds. Such failure causes spacing to the end of the reel.
8. The hardware provides no interlock to prevent reversing tape motion after an early completion pulse. If the programmer desires to reverse the tape after Early Completion and Continue, he must program both the stop command and a 3- millisecond wait before programming the mic instruction specifying reverse motion. On Early Completion and Stop, only the wait is required. The early completion option is included to allow the program to continue into the next record on a tape without waiting for stop-start time, or to switch to another unit without waiting for the first to stop. Under no circumstances should the mic following an early completion pulse be used to reverse the motion of a tape that is already moving.
9. The reset instructions (mri and mrf) must not be used following an early completion pulse.
10. If practical, normal Type 52 system programming should not use the stop command. If Stop is used, it must be followed by a 3-millisecond delay before reversing tape motion.
11. If Stop is used after an early completion Read, which is to be followed by Write, then Stop must be given within 100 microseconds of the early completion pulse. If the 100-microsecond time is exceeded, the tape must be repositioned by backspacing one record and forward spacing one record before writing.
12. If Stop is used after an early completion Read, which is to be followed by Read, Readcheck, or Forward Space, then Stop must be given within 1.5 milliseconds of the early completion pulse. If Stop is delayed longer than 1.5 milliseconds, the tape will probably have proceeded into the next record. The tape must then be repositioned by backspacing two records and determining tape position by additional programming.

Sample Routines, Type 52 System

Any of the following routines may be deposited in memory manually, using the Deposit operation and the address and test word switches. Alternatively, a paper tape may be prepared for Read In mode. A Read In tape should end with a Jump to the start location of the routine. Except for Continuous Write below, all routines start in location 1000; other start locations may be used by adding an appropriate octal number to, or subtracting it from, the locations shown.

Each routine includes a location for a unit address. This location may be left clear by the Read In tape and the desired address deposited from the TW switches. However, the operator may leave the location clear and set the thumbwheel of the selected tape unit to 0.

Continuous Write - This routine writes a test word on tape in a single record of any desired length. It uses the sequence break system to reset the initial address after writing each word, so the test word need be available in only one memory location. Since the tape runs continuously after starting the program, the operator must stop it by clearing sense switch 1 when the tape supply runs low.

All sequence break locations appear in the program. The Jump to the break routine occupies the fourth location of each sequence-break channel; the address of the deferred Jump from the break back to the main program is in the second. The program uses whatever channel corresponds to the ADDRESS EQUAL break. These sequence break addresses must not be changed when moving the entire program to a different start location.

The program uses sense switch 1 as a stop/go switch. While SS1 is set, the program cycles continuously, resetting the initial address every time a word is written on tape. Clearing SS1 interrupts the loop and returns control to the program start location. SS1 does not halt the computer, however; instead, the program samples SS1 continuously. Thus setting SS1 restarts tape operations immediately. If desired, a new word may be placed in TW during the pause on SS1. When SS1 is again set, the program deposits the new test word before starting tape operations.

TYPE 52 CONTINUOUS WRITE PROGRAM

Location	Contents	Mnemonic Code		Remarks
0003	620137	0003/	jsp sns	set-up to insure return regardless of wiring of break system
0007	620137	0007/	jsp sns	
0013	620137	0013/	jsp sns	
0017	620137	0017/	jsp sns	
0023	620137	0023/	jsp sns	
0027	620137	0027/	jsp sns	
0033	620137	0033/	jsp sns	
0037	620137	0037/	jsp sns	
0043	620137	0043/	jsp sns	
0047	620137	0047/	jsp sns	
0053	620137	0053/	jsp sns	
0057	620137	0057/	jsp sns	
0063	620137	0063/	jsp sns	
0067	620137	0067/	jsp sns	
0073	620137	0073/	jsp sns	
0077	620137	0077/	jsp sns	
0100	720051	on,	iot 0051	turn on all channels
0101	720151		iot 0151	
0102	720251		iot 0251	
0103	720351		iot 0351	
0104	720451		iot 0451	
0105	720551		iot 0551	
0106	720651		iot 0651	
0107	720751		iot 0751	

TYPE 52 CONTINUOUS WRITE PROGRAM (continued)

Location	Contents	Mnemonic Code		Remarks
0110	721051		iot 1051	turn on all channels
0111	721151		iot 1151	
0112	721251		iot 1251	
0113	721351		iot 1351	
0114	721451		iot 1451	
0115	721551		iot 1551	
0116	721651		iot 1651	
0117	721751		iot 1751	
0120	720056	beg,	iot 0056	clear break system enter SBM
0121	720055		iot 0055	
0122	650010		szs i 10	wait
0123	600122		jmp .-1	
0124	762200		lat	load address
0125	240145		dac tw	
0126	220147		lio fa	initialize tape to write forward
0127	200150		lac ua	
0130	720376		iot 0376	
0131	600130		jmp .-1	
0132	220146		lio ca	
0133	721375		iot 1375	
0134	600133		jmp .-1	
0135	600135		jmp .+0	wait for break
0136	600135		jmp .-1	
0137	420151	sns,	sub (3	

TYPE 52 CONTINUOUS WRITE PROGRAM (continued)

Location	Contents	Mnemonic Code		Remarks
0140	260144		dap exc	initialize break return
0141	650010		szs 1 10	return if SSW1=1
0142	600120		jmp beg	
0143	720266		iot 0266	reset initial address
0144	610000	exc,	jmp i 0000	debreak
0145	0	tw,	000000	program constants
0146	145	ca,	.-1	
0147	146	fa,	.-1	
0150	0	ua,	000000	
0151	3	constants		

Write One-word Records - The following program writes a continuous series of one-word records, each followed by the characteristic 3/4" end-of-record gap. The program iterates as a loop as long as SS1 is set. Clearing SS1 stops the tape. The single, three-character word comprising each record written on tape is taken from TW. The program requires 17 consecutive memory locations.

If the routine is prepared on paper tape, clear all sense switches before pressing READ IN. The program then pauses between locations 1000 and 1001. During this pause, set the desired three characters into TW; then set SS1 to begin tape operations. The endless sequence of one-word records produced by this program is useful in adjusting the 4303 integrating delay (paragraph 8-4b).

TYPE 52 WRITE ONE-WORD RECORDS

Location	Contents	Mnemonic Code	Remarks
1000	650010	1000/beg,szs i 10	wait
1001	601000	jmp .-1	
1002	762200	lat	load address
1003	241014	dac tw	
1004	201015	lac un	write forward-odd
1005	221017	lio fa	
1006	720376	iot 0376	
1007	601006	jmp .-1	
1010	221016	lio ca	
1011	721375	iot 1375	
1012	601011	jmp .-1	
1013	601000	jmp beg	return
1014	0	tw, 000000	program constants
1015	0	un, 000000	
1016	1014	ca, .-2	
1017	1015	fa, .-2	

Read One-Word Record Tape

Either of the following two routines may be used to read the tape generated by the one-word record program. The first requires 14 consecutive memory locations, and performs the complete Read Tape operation including HSC transfers into core. The second routine, requiring only ten locations, "reads" the tape only as far as the read buffer. Parity is checked in RB but DWB remains clear.

The first routine uses the Read Odd Parity command in the mic instruction. SS1 functions as a stop/go switch. When SS1 is clear, the program pauses between locations 1000 and 1001.

TYPE 52 READ ONE-WORD RECORDS

Location	Contents	Mnemonic Code	Remarks
1000	650010	1000/beg,szs i 10	initialize tape control
1001	601000	jmp .-1	
1002	201012	lac ua	
1003	221013	lio fa	
1004	720376	iot 0376	begin reading
1005	601004	jmp .-1	
1006	221014	lio ca	
1007	721775	iot 1775	
1010	601007	jmp .-1	
1011	601000	jmp beg	return
1012	0	ua, 000000	program constants
1013	1016	fa, .+3	
1014	1015	ca, .+1	
1015	0	wd, 000000	

Setting SS1 allows the program to proceed. If a paper program tape is prepared, clear all sense switches before pressing READ IN; set SS1 to begin tape operations.

The second routine for reading one-word records uses the Forward Space Odd Parity command in the mic instruction instead of the Read Odd Parity command. During forward spacing, each character on the tape is loaded into the read buffer where parity is checked, and the 4303 integrating delays operate just as in read commands. The data word buffer remains clear, however, and no HSC access is requested. The constants in this routine are selected in order to space through 3000 one-word records. This number of records comes very close to filling an entire 2400-foot reel of tape. Thus if the tape is not started at load point or if it contains less than this number of records, the program must be stopped before tape runs off the supply reel. In the interests of simplicity the routine uses no sense switches; instead, the address switches are set permanently to the start location and the START and STOP switches are used to begin and end tape operations.

TYPE 52 READ ONE-WORD RECORDS (ALTERNATE PROGRAM)

Location	Contents	Mnemonic Code	Remarks
1000	201010	1000/beg,lac ua	initialize tape control to space forward
1001	221011	lio fa	
1002	720076	iot 0076	
1003	601002	jmp .-1	
1004	764000	cli	
1005	721175	iot 1175	
1006	601005	jmp .-1	
1007	601007	jmp .+0	wait
1010	0	ua, 000000	program constants
1011	5670	fa, 005670	

A routine such as this is probably simple enough to deposit using the test word switches. Reset the address switches to 1000 before pressing START. Note that once tape operations have begun the tape will space out to the end of the reel. If there is any danger of running off the reel, press STOP to halt the tape.

If desired, instructions mes (iot 0035), rir 4S, spi and jmp . -3 may be substituted for the jmp . +0 in location 1007. This substitution automatically stops the tape on the Low Reel condition. This program, with or without the Examine Status variation, is also useful in adjusting the 4303 integrating delays.

Start-Stop Program - The following routine essentially duplicates the action of the unit calibrator when checking start and stop times (see Every Month, section 8-5). The program is intended for use with a single continuous record of all ones from beginning to end of the tape. The Type 52 end-of-record detection logic is frustrated by the use of Forward Space and Backspace commands with a final address so large as to prevent assertion of ADDRESS EQUAL. No HSC transfers are made; DWB remains clear; characters are "read" from tape only as far as the read buffer. SS1 is used as a stop/go switch; clearing it stops the tape; setting it allows the program to proceed.

The normal order of tape operations is as follows:

1. The muf instruction.
2. Examine SS1: if set, proceed.
3. The mic instruction for forward spacing with odd parity.
4. Delay sequence for timing forward tape movement.
5. Clear command register to stop tape.
6. Delay sequence to establish length of stop time.
7. The mic instruction for backspacing.
8. Delay sequence for timing backward tape movement.
9. Clear command register to stop tape.
10. Delay sequence to establish duration of stop time.
11. Repeat steps 2 to 11 continuously.

Sense switch 1 may be used to halt tape after either forward spacing or backspacing. In Forward Space, the program sets PF_1; then, in the subsequent Backspace, the program clears it. The stop time duration in steps 6 and 10 above is determined by bits 0 to 8 of the test word switches. The least significant bit (TW_8) represents 0.5 milliseconds. The program adds a constant representing 3 milliseconds to the time selected in TW_{0-8}; thus, the stop time may be varied from 3 milliseconds to approximately 1/4 second.

Tape movement time is determined by the last nine bits of TW. The least significant bit (TW_{17}) represents 4 milliseconds. A constant representing 60 milliseconds is added to the time represented by TW_{9-17}, thus tape movement time may be varied from 60 milliseconds to approximately 2 seconds.

Since this routine requires 48 locations for instructions and constants, it makes little sense to waste time depositing the routine from the console. Clear all sense switches before pressing READ IN. Once started, the program pauses between locations 1005 and 1006 until SS1 is set. If a specific unit address is to be deposited at this time, first push STOP; then set the TA switches to 1050 and deposit the unit address from TW. Reposition TA to 1000 and press START. Again, the program pauses between locations 1005 and 1006. Before setting SS1, the desired stop time and tape movement time should be set into TW_{0-8} and TW_{9-17}. Setting SS1 now starts the tape.

TYPE 52 START-STOP ROUTINE

Location	Contents	Mnemonic Code	Remarks
1000	760001	1000/beg, clf 1	initialize tape control
1001	201050	on, lac ua	
1002	221051	lio fa	
1003	720076	iot 0076	
1004	601003	jmp .-1	
1005	650010	szs i 10	wait for SSW1=1
1006	601005	jmp .-1	
1007	640001	szf 1	test for backspace
1010	601031	jmp bs	
1011	221052	fwd, lio ca	space forward
1012	721175	iot 1175	
1013	601012	jmp .-1	
1014	760011	stf 1	
1015	763200	stp, 763200	set-up and delay
1016	41053	ior tmm	
1017	661007	ral 3s	
1020	421054	sub co1	
1021	171036	jda ms	
1022	721067	iot 1067	clear command register
1023	763200	763200	set-up and delay
1024	41055	ior stm	
1025	671777	rar 9s	
1026	421056	sub co2	
1027	171036	jda ms	

TYPE 52 START-STOP ROUTINE (continued)

Location	Contents	Mnemonic Code		Remarks
1030	601001		jmp on	return
1031	221052	bs,	lio ca	return to stop routine
1032	720275		iot 0275	
1033	601032		jmp .-1	
1034	760001		clf 1	
1035	601015		jmp stp	backspace routine
1036	0	ms,	000000	millisecond delay routine
1037	261047		dap gb	
1040	201057		lac mst	
1041	241060		dac ct	
1042	760000		nop	
1043	461060		isp ct	
1044	601042		jmp .-2	
1045	461036		isp ms	
1046	601040		jmp .-6	
1047	600000	gb,	jmp 0000	program constants
1050	0	ua,	000000	
1051	77777	fa,	077777	
1052	0	ca,	000000	
1053	777000	tmm,	777000	
1054	170	col,	000170	
1055	777	stm,	000777	
1056	6	co2,	000006	
1057	777750	mst,	777750	
1060	0	ct,	000000	

Sample Routines, Type 51 System

Since all timing for tape operations in the Type 51 system must be supplied by the program, writing tape in standard IBM format requires routines far too complex to be useful in maintenance procedures. In the interests of simplicity, the routines presented below do not use IBM format for writing or reading. The program listings show all routines starting in location 1000. Other start locations may be used by subtracting or adding an appropriate octal constant to the address of each memory reference instruction. All routines specify a 0 unit address; the desired tape may be selected by setting its unit thumbwheel to 0.

Read Tape - The following routine of eleven instructions reads every character on tape. The routine does not sense missing characters or end-of-record gaps. If EOR characters are present, they may cause a parity error to set PF_4. Three nop instructions allow 25 microseconds for tape skew.

TYPE 51 READ ONE-WORD RECORD TAPE

Location	Contents	Mnemonic Code		Remarks
1000	221013		lio fro	initialize tape to read
1001	720073		iot 0073	
1002	720070		iot 0070	
1003	650002	sns,	szf i 2	wait for character
1004	601003		jmp .-1	
1005	760000		nop	delay and read character
1006	760000		nop	
1007	760000		nop	
1010	764000		cli	
1011	720072		iot 0072	
1012	601003		jmp sns	return
1013	201	fro,	000201	program constant

No sense switch control is included in this routine; to start, set the start location in the address switches and press START. Tape operations begin immediately and continue until STOP is pressed. Since the routine ignores record gaps and simply reads tape continuously, be sure to press STOP before the tape supply runs low.

Write Tape - The following routine writes 6-bit characters from the test word switches continuously. It uses a total of 23 instructions including eight nop's that provide the 65-microsecond interval between tape characters. The operator specifies the character in TW_{11-17} and he may change it at any time while the routine is running. Also included is a 10.6 millisecond delay between starting the tape and writing the first character, to provide a 3/4" record gap. However, the routine does not provide the EOR mark (longitudinal parity) used in IBM format.

To start tape operations set the desired character in TW_{11-17}. Set the address switches to the start location and press START. To stop tape movement, press STOP. When the tape comes to rest, the write head is approximately 0.13" past the end of the string of characters written. The read head, however, lies within the string, and if a read instruction were now given, between 30 and 40 characters would be read before coming to blank tape.

TYPE 51 WRITE TAPE ROUTINE

Location	Contents	Mnemonic Code		Remarks
1000	221026	beg,	lio fwo	initialize tape control
1001	720073		720073	
1002	720070		720070	
1003	201024		lac tml	delay
1004	241025		dac ct	
1005	461025		isp ct	
1006	601005		jmp .-1	
1007	762200	wrt,	lat	load character and write
1010	673077		rcr 6s	
1011	720071		720071	

TYPE 51 WRITE TAPE ROUTINE (continued)

Location	Contents	Mnemonic Code	Remarks
1012	760000	nop	delay 65 μsec
1013	760000	nop	
1014	760000	nop	
1015	760000	nop	
1016	760000	nop	
1017	760000	nop	
1020	760000	nop	
1021	760000	nop	
1022	760000	nop	
1023	601007	jmp wrt	return
1024	776474	tml, 776474	program constants
1025	0	ct, 000000	
1026	221	fwo, 000221	

Start-Stop Routine

This routine is adapted from the start-stop routine for the Type 52 listed above. Although all tape instructions are changed to fit the Type 51, the description and procedures given for the Type 52 start-stop routine apply to the following as well.

All routines described above both for the Type 51 and Type 52 tape systems are given only to illustrate form and organization. With a well grounded familiarity with both tape logic and programming, a technician should be able to generate applicable loops to troubleshoot any section of the system. Comparison of these routines with Tables 11-10 and 11-11 of the basic PDP-1 Manual illustrates the complexity characterized by tape routines as contrasted with routines that test small sections of logic. Although the examples given are typical, many simplifications can be made in the loops given above. For example, sense switch control need not be used. If tape control logic is suspect, whereas the transport itself seems healthy, many simple routines may be generated that test logic functions with transport power off.

TYPE 51 START-STOP ROUTINE

Location	Contents	Mnemonic Code	Remarks
1000	760001	1000/beg, clf 1	clear tape buffers and wait
1001	720070	on, 720070	
1002	650010	szs 1 10	
1003	601002	jmp .-1	
1004	640001	szf 1	test for backspace
1005	601026	jmp bs	
1006	221044	fwd, lio fro	move tape forward
1007	720073	720073	
1010	760011	stf 1	
1011	763200	stp, 763200	set-up and delay
1012	41046	ior tmm	
1013	661007	ral 3s	
1014	421047	sub col	
1015	171032	jda ms	
1016	764000	cli	clear command register set-up and delay
1017	720073	720073	
1020	763200	763200	
1021	41050	ior stm	
1022	671777	rar 9s	
1023	421051	sub co2	
1024	171032	jda ms	
1025	601001	jmp on	return
1026	221045	bs, lio rro	backspace
1027	720073	720073	

TYPE 52 START-STOP ROUTINE (continued)

Location	Contents	Mnemonic Code		Remarks
1030	760001		clf 1	return to stop routine
1031	601011		jmp stp	
1032	0	ms,	000000	millisecond delay routine
1033	261043		dap gb	
1034	201052		lac mst	
1035	241053		dac ct	
1036	760000		nop	
1037	461053		isp ct	
1040	601036		jmp .-2	
1041	461032		isp ms	
1042	601034		jmp .-6	
1043	600000	gb,	jmp 0000	
1044	201	fro,	000201	program constants
1045	241	rro,	000241	
1046	777000	tmm,	777000	
1047	170	col,	000170	
1050	777	stm,	000777	
1051	6	co2,	000006	
1052	777750	mst,	777750	
1053	0	ct,	000000	

The routines listed above are designed for specific applications (e.g. calibration of the 4303 delays in the Type 52). These examples should not be considered as limiting the scope or application of exercise routines developed by the technician in the course of troubleshooting procedures. Ingenuity, common sense and familiarity with the instruction list enable an alert

technician to develop diagnostic or exercise loops to suit any specific troubleshooting problem.

b TYPE 52 TEST WORD PROGRAM - This program is a short routine designed to supplement diagnostic routines for maintenance purposes. Using the test word switches, the operator deposits unit address, initial address, final address, two pattern words and three commands. PDP-1 then causes the Type 52 system to perform the three-command sequence repetitively. Under sense switch control, the first two commands alone may be performed as a repetitive sequence.

Additional program functions selected by sense switches include single-record backspacing after any command, error checking after each command, and halting after each command (single command mode). Two pattern words are included to allow alternating characters of all zeros and all ones, or to provide a six-character pattern. The two pattern words are placed in alternating memory locations between selected initial and final addresses.

Console Operating Procedures

The only tapes required are the 52 TEST WORD program on paper tape and one or more reels of blank magnetic tape. The load sequence is as follows:

1. Clear all sense switches.
2. Set the desired unit address into TW_{15-17}.
3. Load the program tape into the reader and press READ IN at the console. The program halts at location 104.
4. Set the desired 16-bit initial address into TW_{2-17}. Press CONTINUE. The program stops at location 111.
5. Set the desired 16-bit final address into TW_{2-17}. This final address should equal precisely the final core address to which HSC access is desired. The program provides the necessary indexing (see paragraph 4-4). Again press CONTINUE. The program stops at 117.
6. Set the three characters comprising the first desired pattern word into the test word switches. Again press CONTINUE. The program stops at 122.
7. Set the three characters comprising the second desired pattern word into the test word switches and press CONTINUE. After a length of time depending on the size of record desired (i.e., the difference between initial and final addresses), the program stops at 126.

8. Into TW_{2-5}, set the first of the three desired commands (see the command list under the mic instruction, paragraph 4-4). Similarly, set the second command into TW_{8-11} and the third command into TW_{14-17}. Press CONTINUE. The program halts at 160, and can now proceed with tape operations. Do not press CONTINUE again until making the desired sense switch settings as described below.

During normal operation, the program provides the unit address in AC, the final address in IO, and gives a muf instruction. The initial address is then loaded into IO and the program gives a mic instruction. Both mic and muf are given repeatedly until accepted by the TC. This sequence is repeated three times, once for each of the commands set into TW in step 8 above. Bits 8 to 11 of the first mic contain the command set into TW_{2-5}. Similarly, TW_{8-11} provides the command for the second mic and TW_{14-17} provides it for the third. Normally the third command is followed again by the first so that the three-command sequence is repeated indefinitely. The sense switches make the following modifications to the sequence:

Sense switch 1 backspaces the tape one record after execution of the first command.

Sense switch 2 backspaces one record after the second command.

Sense switch 3 backspaces one record after the third command.

Sense switch 4 performs an error check routine after each command.

Sense switch 5 halts the computer after each command.

Sense switch 6 causes the program to execute the first command after the second.

The third command (TW_{14-17} in step 8) can be performed only when SS6 is off.

Two simple error check routines are provided: one for tape error, the other for data error. When SS4 is on, both routines are performed. The tape error routine gives the mes instruction (examine status) and halts on IO_0^1, setting pf5. The data error routine normally performed after a read instruction checks the contents of core from the initial to final addresses against the two pattern words deposited in load sequence steps 6 and 7 above. A data-error halt lights pf6. These routines cause the following error halts:

Location 260: tape error; IO contains the status word.

Location 267: data error; the contents of core differ from the first pattern word. The AC

lights show the erroneous bits; IO contains the pattern word.

Location 277: data error; the contents of core differ from the second pattern word. The AC lights show the erroneous bits; IO contains the pattern word.

The following list gives procedures for continuing the program after a program halt. When the program halts, first look at the address indicators, then consult the following list for the restart procedure corresponding to the halt in that location. The listing does not include halts encountered as part of the load sequence described above.

Halt location 176: SS5 stop after first command. To proceed to second command press CONTINUE.

Halt location 215: SS5 stop after second command. To proceed to third command, press CONTINUE. Note that if SS6 is on, the program does not perform the third command but instead returns to the first.

Halt location 236: SS5 stop after third command. To return to first command, press CONTINUE.

Halt location 260: tape error halt. To proceed with data error check routine press CONTINUE.

Halt location 267: pattern 1 data error halt. To proceed with the pattern 2 error check, press CONTINUE.

Halt location 277: pattern 2 data error halt. As long as SS4 is on, repeatedly pressing CONTINUE displays each data error in core until the final address is reached. If SS4 is turned off, CONTINUE returns the computer to the current command. The program then performs the backspace routine if specified, and halts if SS5 is on.

After any of the foregoing program halts, or after pressing STOP, command parameters may be changed individually or in groups. The program accepts parameters from the test word switches in the following order: unit address, initial address, final address, pattern word 1, pattern word 2 and command word. Any of the procedures described below may be executed after a program halt. If the program is performing the command sequence, the computer must be STOPped before changing parameters.

If SS5 is off, the program halts to allow changing the next parameter in order. If SS5 is on, the program jumps to the halt just before the command sequence (location 160). Sense switches may then be adjusted for desired command sequence.

TYPE 52 TEST WORD TO TAPE

Location	Contents	Mnemonic Code		Remarks
0100	762207	beg,	opr 2207	initialization
0101	240331		dac un	
0102	640050		szs 50	
0103	600160		jmp hup	
0104	760400		hlt	
0105	762207	gca,	opr 2207	
0106	240332		dac ca	
0107	640050		szs 50	
0110	620306		jsp cha	
0111	760400		hlt	
0112	762207	gfa,	opr 2207	
0113	240336		dac fa	
0114	440336		idx fa	
0115	640050		szs 50	
0116	620306		jsp cha	
0117	760400		hlt	
0120	762207	gp,	opr 2207	
0121	240337		dac pal	
0122	760400		hlt	
0123	762207		opr 2207	
0124	240340		dac pa2	
0125	620306		jsp cha	
0126	760400		hlt	
0127	340333	gc,	dzm cl	

TYPE 52 TEST WORD TO TAPE (continued)

Location	Contents	Mnemonic Code	Remarks
0130	340334	dzm c2	initialize
0131	340335	dzm c3	
0132	200343	lac col	
0133	240170	dac fc	
0134	240207	dac sc	
0135	240230	dac tc	
0136	762200	lat	
0137	300333	dip c1	
0140	661077	ral 6s	
0141	300334	dip c2	
0142	661077	ral 6s	
0143	300335	dip c3	
0144	200333	lac c1	
0145	671077	rar 6s	
0146	60170	xor fc	
0147	240170	dac fc	
0150	200334	lac c2	
0151	671077	rar 6s	
0152	60207	xor sc	
0153	240207	dac sc	
0154	200335	lac c3	
0155	671077	rar 6s	
0156	60230	xor tc	
0157	240230	dac tc	

TYPE 52 TEST WORD TO TAPE (continued)

Location	Contents	Mnemonic Code		Remarks
0160	760400	hup,	hlt	
0161	760007	il,	760007	enter first command
0162	760011		760011	
0163	200331		lac un	
0164	220336		lio fa	
0165	720076	mul,	iot 0076	
0166	600165		jmp .-1	
0167	220332		lio ca	
0170	720075	fc,	iot 0075	
0171	600170		jmp .-1	
0172	640040		szs 40	
0173	620251		jsp ecr	
0174	640010		szs 10	
0175	620241		jsp bsr	
0176	640050		szs 50	
0177	600176		jmp .-1	
0200	760007	i2.	760007	enter second command
0201	760012		760012	
0202	200331		lac un	
0203	220336		lio fa	
0204	720076	mu2.	iot 0076	
0205	600204		jmp .-1	
0206	220332		lio ca	
0207	720075	fc.	iot 0075	

TYPE 52 TEST WORD TO TAPE (continued)

Location	Contents	Mnemonic Code		Remarks
0210	600207		jmp .-1	
0211	640040		szs 40	
0212	620251		jsp ecr	
0213	640020		szs 20	
0214	620241		jsp bsr	
0215	640050		szs 50	
0216	600215		jmp .-1	
0217	640060		szs 60	
0220	600161		jmp i1	
0221	760007	i3,	760007	enter third command
0222	760013		760013	
0223	200331		lac un	
0224	220336		lio fa	
0225	720076	mu3,	iot 0076	
0226	600225		jmp .-1	
0227	220332		lio ca	
0230	720075	tc,	iot 0075	
0231	600230		jmp .-1	
0232	640040		szs 40	
0233	620251		jsp ecr	
0234	640030		szs 30	
0235	620241		jsp bsr	
0236	640050		szs 50	
0237	600236		jmp .-1	

TYPE 52 TEST WORD TO TAPE (continued)

Location	Contents	Mnemonic Code		Remarks
0240	600161		jmp il	
0241	260250	bsr,	dap lve	
0242	200331		lac un	
0243	764000		cli	
0244	720076		iot 0076	
0245	600244		jmp .-1	
0246	720375		iot 0375	
0247	600246		jmp .-1	
0250	600000	lve,	jmp 0000	return
0251	260330	ecr,	dap gb	error tests if halt occurs set proper PF
0252	760014		760014	
0253	200331		lac un	
0254	720076		iot 0076	
0255	600254		jmp .-1	
0256	720035		iot 0035	
0257	642000		spi	
0260	760415	ert,	760415	
0261	200332		lac ca	
0262	240342		dac wbc	
0263	210342	cp,	lac i wbc	
0264	60337		xor pal	
0265	220337		lio pal	
0266	640100		sza	
0267	760416	erl,	opr 0416	

TYPE 52 TEST WORD TO TAPE (continued)

Location	Contents	Mnemonic Code		Remarks
0270	440342		idx wbc	continue error testing
0271	500336		sad fa	
0272	600307		jmp chk	
0273	210342		lac i wbc	
0274	60340		xor pa2	
0275	220340		lio pa2	
0276	640100		sza	
0277	760416	er2,	opr 0416	
0300	650040		szs i 40	
0301	600307		jmp chk	
0302	440342		idx wbc	
0303	520336		sas fa	
0304	600263		jmp cp	
0305	600307		jmp chk	
0306	260330	cha,	dap gb	
0307	200332	chk,	lac ca	
0310	240341		dac pp	
0311	724074		iot 4074	
0312	200337	wp,	lac pal	
0313	250341		dac i pp	
0314	440341		idx pp	
0315	500336		sad fa	
0316	600324		jmp dc	
0317	200340		lac pa2	

TYPE 52 TEST WORD TO TAPE (continued)

Location	Contents	Mnemonic Code		Remarks
0320	250341		dac i pp	continue error testing
0321	440341		idx pp	
0322	520336		sas fa	
0323	600312		jmp wp	
0324	640004	dc,	szf 4	
0325	610330		jmp i gb	
0326	640050		szs 50	
0327	600160		jmp hup	
0330	600330	gb,	jmp .	
0331	0	un,	000000	Program constants
0332	0	ca,	000000	
0333	0	c1,	000000	
0334	0	c2,	000000	
0335	0	c3,	000000	
0336	0	fa,	000000	
0337	0	pal,	000000	
0340	0	pa2,	000000	
0341	0	pp,	000000	
0342	0	wbc,	000000	
0343	720075	col,	iot 0075	

TYPE 52 TEST WORD TO TAPE (continued)

Location	Contents	Mnemonic Code	Remarks
000	762212	beg, opr 2212	load AC from test word set PF2=1
1001	663777	rcl 9s	test connections error halt if no MRC 7
1002	663777	rcl 9s	
1003	720071	iot 0071	
1004	720072	iot 0072	
1005	640002	szf 2	
1006	760400	hlt	
1007	601000	jmp beg	return

To change unit address: set address switches to location 100. Set TW_{15-17} to the new unit address. If the initial address is also to be changed, clear SS5. To return to the command sequence, set SS5. Press START.

To change initial address: set TA to location 105. Set TW_{2-17} to the new current address. Clear SS5 if the final address is also to be changed; set it to return to the command sequence. Press START.

To change final address: set TA to location 112. Set the new final address into TW_{2-17}. Clear SS5 if pattern words are also to be changed; set it to return to the command sequence. Press START.

To change pattern words: set TA to location 120. Set test word switches to the first 18-bit pattern word. Press START. The program halts at location 122. Set TW to the second 18-bit pattern word. Set SS5 to return to the command sequence; clear it to allow depositions a new command word. Press CONTINUE (not START.)

To change command word: set TA to location 127. Set the three new commands into TW_{2-5}, TW_{8-11} and TW_{14-17}. Press START. The program halts at location 160, and can now proceed with the command sequence. The sense switches may be adjusted to provide the desired configuration of backspacing, error checking, program halts, and sequence of commands.

c MAINDEC 20 FOR TYPE 51 SYSTEM - MAINDEC 20 is a program designed to test operation of the Type 51 Tape System. This program can perform all tape operations. Reading and writing (even or odd parity) are in standard low-density IBM format (200 characters per inch). The program provides a data buffer of 3000 words (octal).

MAINDEC 20 includes a pattern generating routine which may be used to load the entire data buffer or any portion with one of six data patterns. These patterns include all zeros, all ones, alternate ones, and zeros, random numbers, and the concise code for any character. Alternatively, every memory location in the buffer may receive its own address. In read and write operations the operator specifies initial and final addresses, encompassing any portion of the buffer.

The program accepts and decodes thirty pseudo instructions. Twelve of these control the pattern generating routine; six generate the six patterns; the remaining six are normally used after reading from tape. The latter check the data buffer against the pattern generator and type out any discrepancies. Eight pseudo instructions are provided for tape operations: these include read and write instructions in both even and odd parity, spacing instructions, and instructions for rewind and read compare.

The pseudo instruction list also includes four arithmetic instructions for address modification, four utility instructions that perform functions internal to the program, and two transfer instructions. MAINDEC 20 can execute programs of up to 128 pseudo instructions.

All communication between program and operator is via the typewriter. The program accepts pseudo instructions from the keyboard and all error halts are typed out forming a permanent record for maintenance logs. A complete description of this maintenance program for the Type 51 system is given in MAINDEC 20.

8-7 POTTER TRANSPORT

The handbook of operation and maintenance for the M90611-1 Tape Transport System is relatively complete for troubleshooting and maintenance procedures. The adjustment procedures of Section VI are complete and exhaustive; adequate reference information is provided for curing malfunctions. However, three of the procedures given in Section VI of the Potter manual are not recommended by DEC. All three are part of the performance test procedures,

and all apply to the pinch-roller solenoid drive system. On page 6-12 (of the manual dated June 1962), paragraph 6-8-4-2a, step 3 is a procedure for measuring pinch roller return force by pushing the roller down onto the capstan with a 0 to 16 ounce spring scale. This method of measurement must not be used. Instead, use the technique given in paragraph 6-6-4c, step 2, page 6-5.

In paragraph 6-8-4-2g, a procedure is given for measuring the pinch roller drive force by hooking a 0 to 20 pound spring scale over the lower leaf spring on the forward pinch roller drive assembly (or the upper spring on the reverse assembly). Do not use this procedure. Instead use the measurement procedure given in step 1, paragraph 6-6-4d, page 6-5.

In paragraph 6-8-4-3h, start time is given as the interval between the leading edge of the forward command signal and the point at which the playback envelope stablizes - a maximum of 3 milliseconds, as shown in Potter Figure 6-2. This criterion may be used if the envelope begins no later than 2 milliseconds after the forward command signal leading edge (Potter Figure 6-2 shows 1.5 milliseconds). The preferred method of measuring start time, however, is detailed in step 17 of paragraph 8-5 above. The sum of the start and stop times must not exceed 3 milliseconds.

There are two important test and adjustment procedures not covered by the Potter manual. These are the pinch roller bounce test and the check and adjustment procedure for write signal coupling, described below.

a PINCH ROLLER BOUNCE - This effect may be observed when measuring the stop time according to steps 16 and 17 of paragraph 8-5 above, using a prepared tape containing all ones. The stop time velocity profile of a machine having pinch roller bounce is illustrated in Figure 8-8 as the random pips occurring some time after the fall of the tape signal envelope. These pips are ones picked up by the read head during slight movement of the tape caused by a pinch roller rebound briefly engaging the tape to the capstan.

The waveform of Figure 8-8 may be caused by a number of transport maladjustments, the most severe of which is jitter in the takeup or supply reel. Jitter severe enough to cause this waveform has progressed to a point where it will be noted even before attempting to measure start and stop times. The more probable causes include the following:

Improper dash pot adjustment
Insufficient drag pad tension
Insufficient vacuum
Leaky vacuum chamber buffer plate
Insufficient pinch roller return force
Insufficient pinch roller clearance
Pinch roller and capstan not parallel
Pinch roller and return springs mechanically resonant

The vacuum buffer system should first be checked for proper operation. If the blower seems to be laboring without providing adequate vacuum, the only reasonable remedy at the site is replacement. The defective unit should be returned to DEC. The vacuum buffer plate, part 7 in Potter Figure 3-4, sometimes becomes loose and should be checked for leaks. The plate seldom becomes sloppy enough to destroy operation of the buffer, but this malfunction is not unknown.

If the spurious tape motion implied by the waveform in Figure 8-8 is not due to any of the above causes, the entire adjustment procedure for the drag pads and pinch roller return force, clearance and parallelism should be performed again with particular care. Pinch roller bounce rarely survives a proper adjustment of the drive system. If the malfunction does not respond to the adjustment procedures given in paragraph 6-4 of the Potter manual, then DEC field service personnel should be called.

If service is not available or if the transport is absolutely necessary and cannot be replaced, there are interim techniques which can eliminate pinch roller bounce until arrival of the DEC field service representative.

1. Check for swayback of either pinch roller return spring. The two springs are shown as parts 16 and 40 in Potter manual Figure 3-20. Normally these springs appear flat and resist firmly any attempt to buckle them. The most common cause of bowed springs is the attempt to measure pinch roller drive force according to paragraph 6-8-4-2g of the Potter manual. This technique is not recommended (see above). If either spring is substantially curved, the pinch roller bounce is most probably due to mechanical resonance in the return spring system. The two springs are selected to resonate at different frequencies, similar to the two springs

per value used in modern high-speed engines. If a spring is substantially deformed, resonance is possible at one or more frequencies and the only remedy is spring replacement.

2. When spring resonance is absent, pinch roller bounce can sometimes be cured either by increasing return spring tension above 45 ounces or by decreasing it below 35. An increase eliminates the bounce-back by providing still more force in the direction of return; lowering the force decreases the kinetic energy picked up by the roller during its return. The decision to increase or decrease tension depends on the characteristics of the collision between the roller bracket and its stop.
3. As a last resort, the pinch roller can be made to bounce against the capstan at the end nearest the observer (i.e. farthest away from the transport panel), thus preventing the bounce from affecting the tape. This is accomplished by very slightly disturbing the parallelism between the roller and the capstan so the clearance is less at the outer end of the capstan than at the inner end. The bouncing pinch roller then hits the capstan only at the outer end and thus does not engage the tape to the capstan.

These are interim measures. Under no circumstances are these methods to be used to eliminate pinch roller bounce on a permanent basis. If the waveforms shown in Figure 8-8 cannot be improved by a proper adjustment of the drive system according to paragraph 6-6-4 of the Potter manual, DEC field service representatives must be called to diagnose and remedy the malfunction

b WRITE-READ COUPLING - Excessive magnetic coupling from the write to read head results in a write signal superimposed upon a read signal, causing distortion, misinterpretation and excessive parity error. Write signal coupling can be detected by examing the read signal during a normal write operation either with or without tape in the machine. Figure 8-8 (middle-left) shows mild write signal coupling causing slight loss of oscilloscope sync; severe coupling (bottom-left) causes sharp pucks in the waveforms, resulting in picking up ones and consistent loss of scope sync. In the Type 52 system, excessive write signal coupling most often appears during write operations as parity error that is not substantiated by a follow-up readcheck of the same record. For comparison, Figure 8-8 (top-right) shows a normal read waveform.

During all normal tape operations, the read head is magnetically shielded from the write head by a piece of black ferrite, part 31 in the Potter manual, Figure 1-7. On transports of recent design, the ferrite pad is not as large as that shown in Figure 1-7, but the figure accurately shows the position of the pad and configuration of the mounting hardware. Clearance between the pad and the read-write head is determined by the vertical position of the plate assembly (part 30) with respect to the head pad bracket (part 29); by the relative adjustments of the tripod rest created by the three setscrews (part 26 - these screws are arranged in a triangle); and by the setting of the clearance adjustment screw (28). Since the clearance adjustment sits against the cover plate tab (3) when the head cover is closed, any movement of the plate disturbs the rest position of the cover and thus alters the clearance between the head and the ferrite slab. Consequently the clearance and position adjustments must be made whenever the read-write head is moved or replaced, whenever the through guides are replaced or adjusted, and in general after any movement of the cover plate or its hardware.

The pad position must also be adjusted whenever the head cover sustains any physical damage. The most common cause of damage results from failure to close the cover after threading the tape and then subsequently slamming the heavy glass front door on it. In general this merely bends the head cover, but occasionally it also chips the ferrite pad. The only cure for such damage is replacement.

The adjustment procedure is as follows:

1. Remove tape from the transport.
2. Block the tension arms at the null point by hooking rubber bands around the rollers of both tension arms and roller bridge.
3. Using either the Calibrator or an appropriate maintenance routine, write all ones continuously in odd parity.
4. Obtain a display from the channel 1 read preamp output (at the gain, slice and test point panel). Compare this waveform with Figures 8-12 and 8-13.

Figure 8-8 shows the static (tapeless) write coupling signal when there is heavy magnetic coupling between read and write heads. The signal as shown is about 1 volt peak-to-peak (0.5 volt per division). The ideal is less than 100 millivolts signal coupled through (Figure 8-8 bottom right), but often this cannot be realized. Less than 200 mv may be achieved as follows:

5. Insert two thicknesses of standard blank paper tape between the read-write head and the ferrite pad. The tape interposes a minimum clearance of 9 mils.
6. Loosen the two screws (Potter manual Figure 1-7, part 27) and very carefully move the plate up or down vertically while watching the scope. Adjust the vertical position of the coupling plate assembly for minimum read signal amplitude. Only very slight movements are necessary. When a minimum is achieved, gently tighten the two mounting screws.
7. If the minimum coupled signal is still greater than 200 mv, rotate the clearance adjustment (28) counterclockwise to just barely pinch the paper tape between the ferrite pad and the head. If the clearance is already this close, proceed to the next step.
8. Check each of the seven channels and leave the oscilloscope probe on the channel that shows the least coupling. Generally this will be an end channel, i.e. channel 1 or the parity channel.
9. If this minimum coupled signal is not less than 200 mv, remove one strip of paper tape and continue to reduce clearance by rotating the adjustment (28) counterclockwise. Under no circumstances bring the clearance close enough to pinch the remaining single thickness of paper tape. If it is still impossible to bring write signal coupling on at least one channel lower than 200 mv, something else is wrong and you must call the DEC field service representative. Normally at least one channel will attenuate below 200 mv coupling without difficulty.
10. When minimum write coupling has been achieved on a single channel (Figure 8-8 bottom-right), coupling on the remaining channel can be minimized without further decreasing the clearance by adjusting for parallelism between the head and the pad. The adjustment is a cut-and-try technique; each change in the adjustment must be made by first loosening both mounting screws (27), altering the relative adjustment of the three tripod rest setscrews (26), and retightening the mounting screws. Following this adjustment, all seven channels should be examined for coupling.
11. If the write coupling signal cannot be reduced below 200 mv peak, remove the pad and coupling plate assembly, turn it up-side-down, and reinstall. The pad may be in either the upper or the lower position on the plate, whichever provides minimum coupling.

12. As a final check on the adjustment, place the tape in the machine and remove the bands from the tension arms. Using an alligator-clip jumper with a banana jack, short the forward tape movement command level to ground at the FWD jack on the gain, slice, and test point panel. Program the system (or use the calibrator) to write ones continuously and again examine the read waveform. With tape in the machine, the waveform may be slightly altered but the write coupling signal should still be below 200 mv peak-to-peak.
13. When a satisfactory parallelism adjustment is obtained, touch up the vertical position of the pad and plate assembly once more before finally tightening the mounting screws (27).

This completes the adjustment.

Figure 2-1

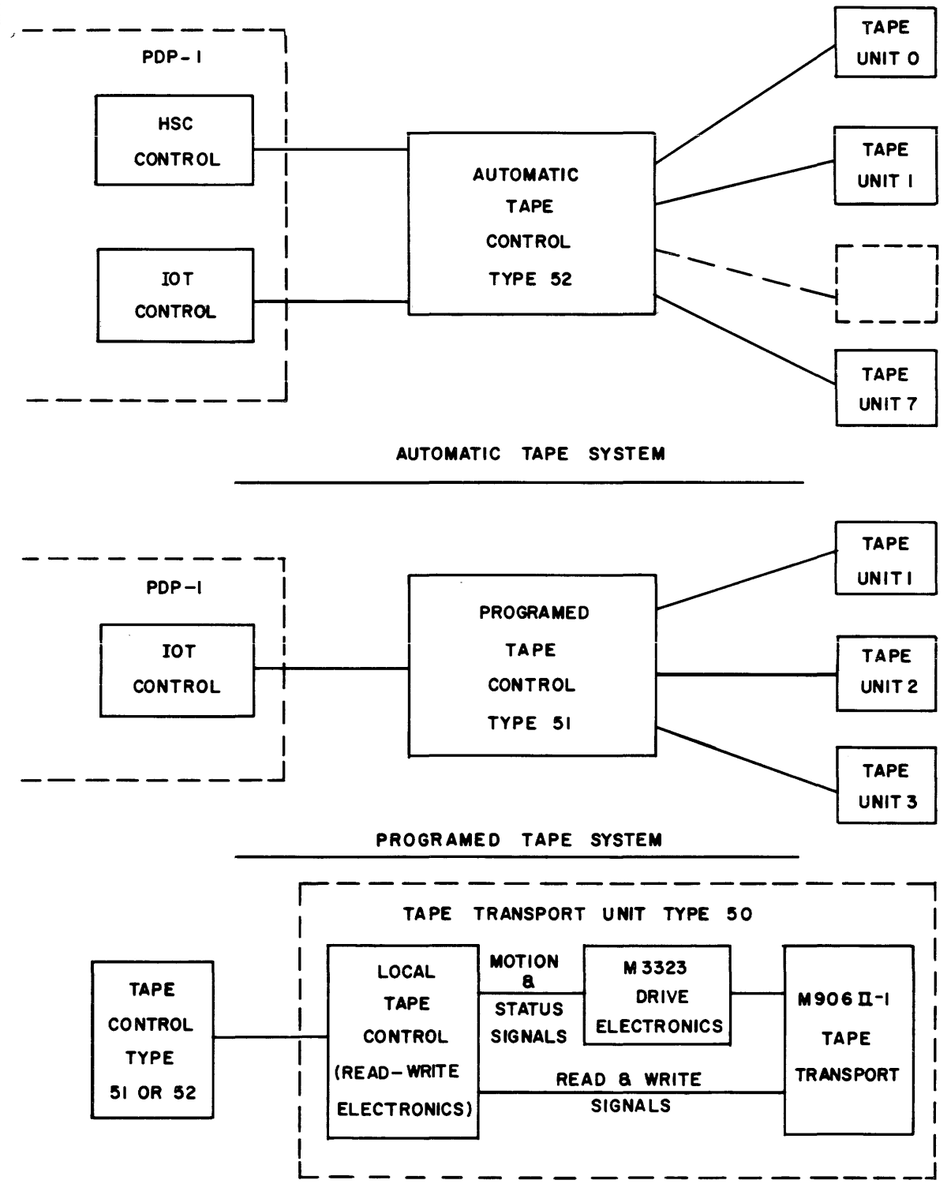


Figure 2-1 Tape System Configuration Diagram

Figure 2-2

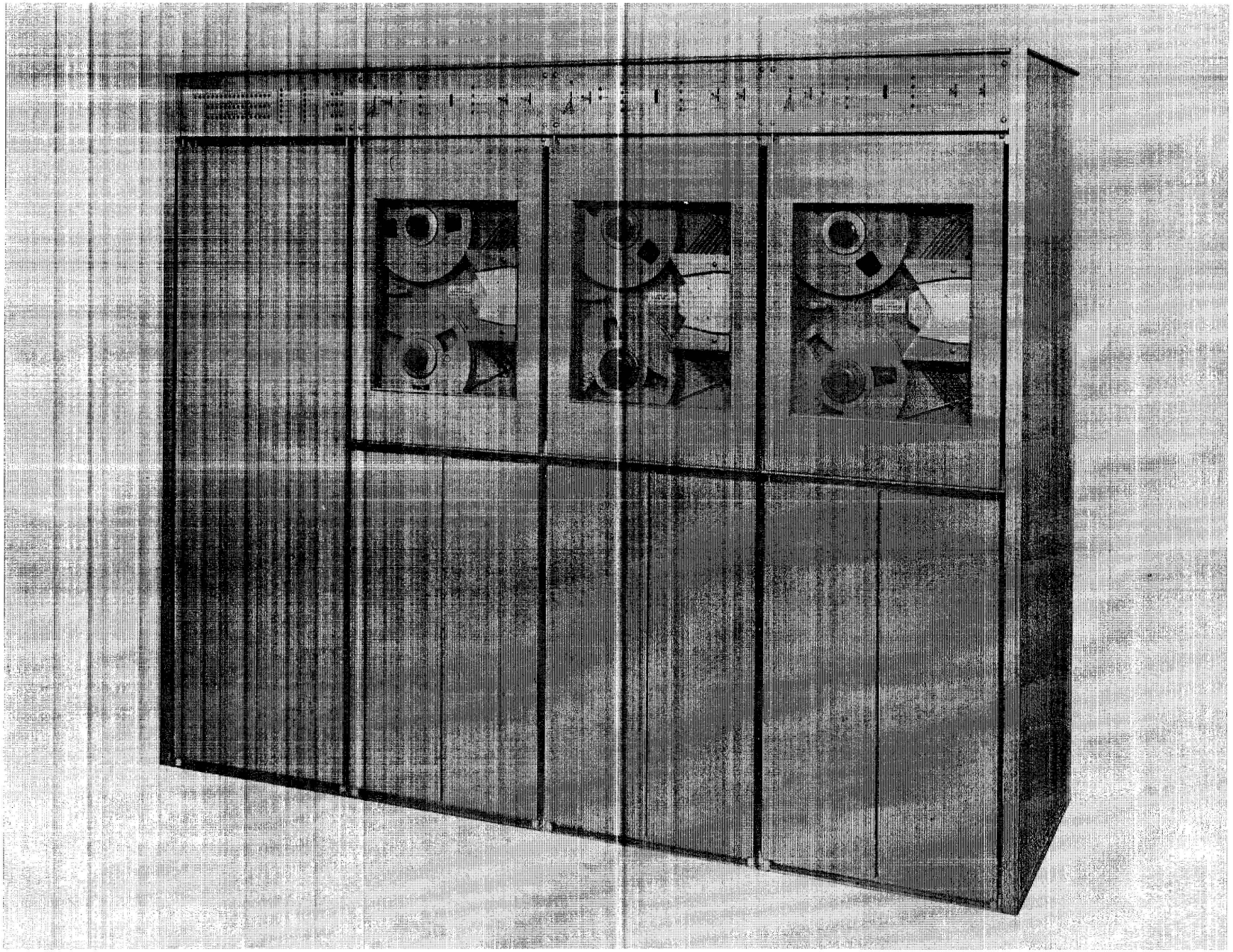


Figure 2-2 Typical Installation, Type 52 Automatic Tape System

BAY I FRONT

INDICATOR PANEL

FIG 5-3

BLANK

1B

FORMAT CONTROL

FIG 6-16

1C

IN-OUT CONTROL

FIG 6-15

1D

WRITE BUFFER
COMMAND REGISTER

FIG 6-10

1E

READ BUFFER

FIG 6-14

1F

DATA WORD BUFFER

FIG 6-13

1G

UNIT ADDRESS
FINAL ADDRESS

FIG 6-12

1H

CURRENT ADDRESS

FIG 6-11

BUS SOCKET PANEL

FIG 3-2

BLANK

BLANK

LOGIC LAYOUT

BAY I REAR

BLANK

MARGINAL CHECK
POWER SUPPLY
734

FIG 5-4

POWER SUPPLY
728

POWER SUPPLY
728

POWER SUPPLY
728

POWER CONTROL
811

BLANK

PLENUM DOOR LAYOUT

Figure 2-3 Layout Diagram, Tape Control 52

BAY 2 FRONT

MANUAL CONTROL PANEL

FIG 5-1

BLANK

TRANSPORT

READ – WRITE HEAD

POTTER DWG D-414075T FIG 5-5

DOOR MOUNT

TRANSPORT DRIVE ELECTRONICS

POTTER DWG X-416189T

GAIN, SLICE AND TEST POINT PANEL

FIG 5-2

2 G

LOCAL CONTROL TYPE 50

FIG 6-18,19

BUS SOCKET AND TAPER PIN PANEL

FIG 3-1,2,3

2 H

TAPE CONTROL TYPE 51*

FIG 6-17

LOGIC LAYOUT

BAY 2 REAR

POWER SUPPLY 728 (51)*

POWER CONTROL 811 (51)*

POWER SUPPLY 728

POWER CONTROL 822 (811B)

BLANK

ISOLATION TRANSFORMER

BLANK

PLENUM DOOR LAYOUT

* In unit 1 of type 51 system only

Figure 2-4 Layout Diagram, Tape Unit 50

Figure 2-5

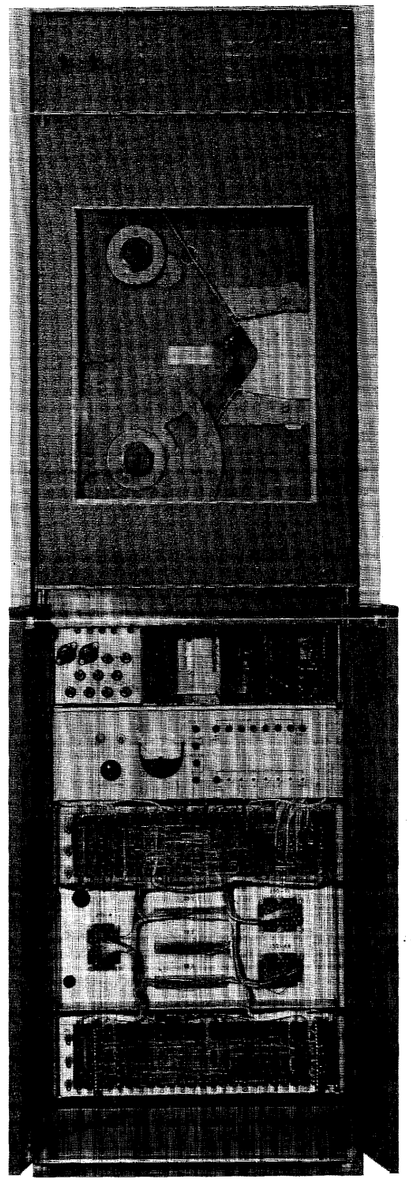


Figure 2-5 Tape Unit

Figure 3-1

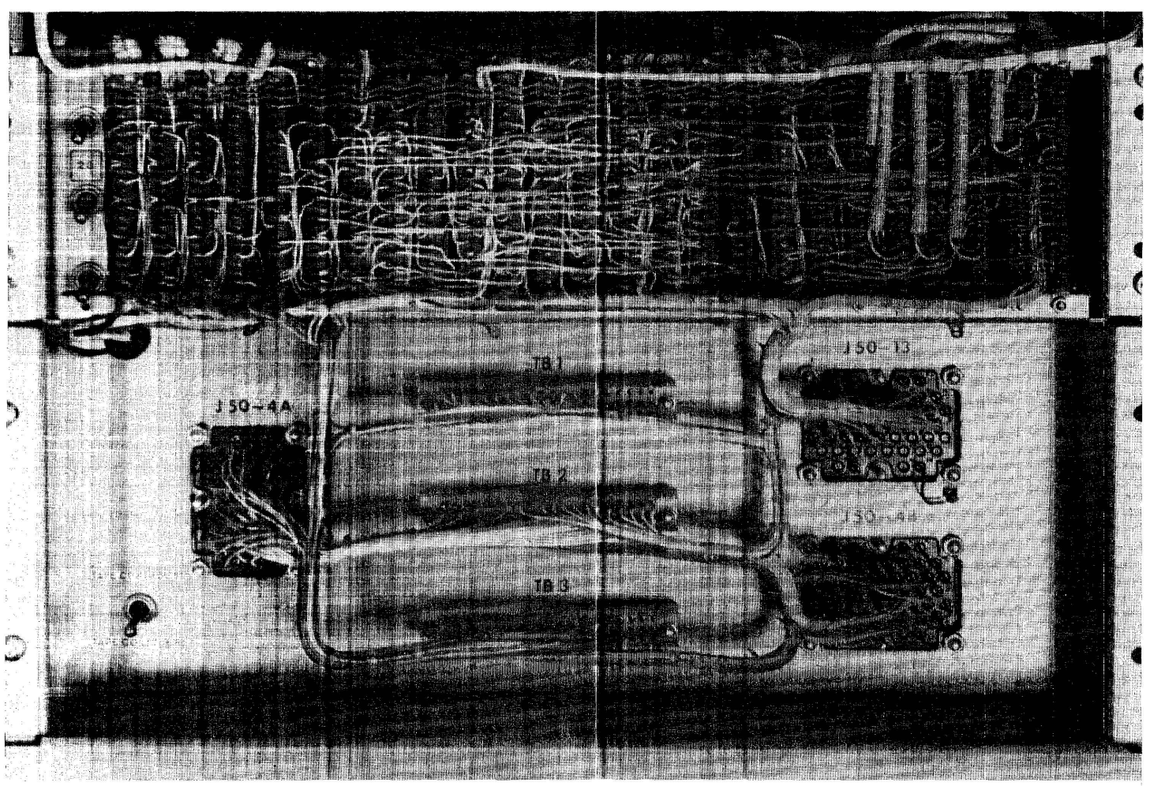


Figure 3-1 Tape Unit Bus Socket and Taper Pin Panel

Figure 3-2

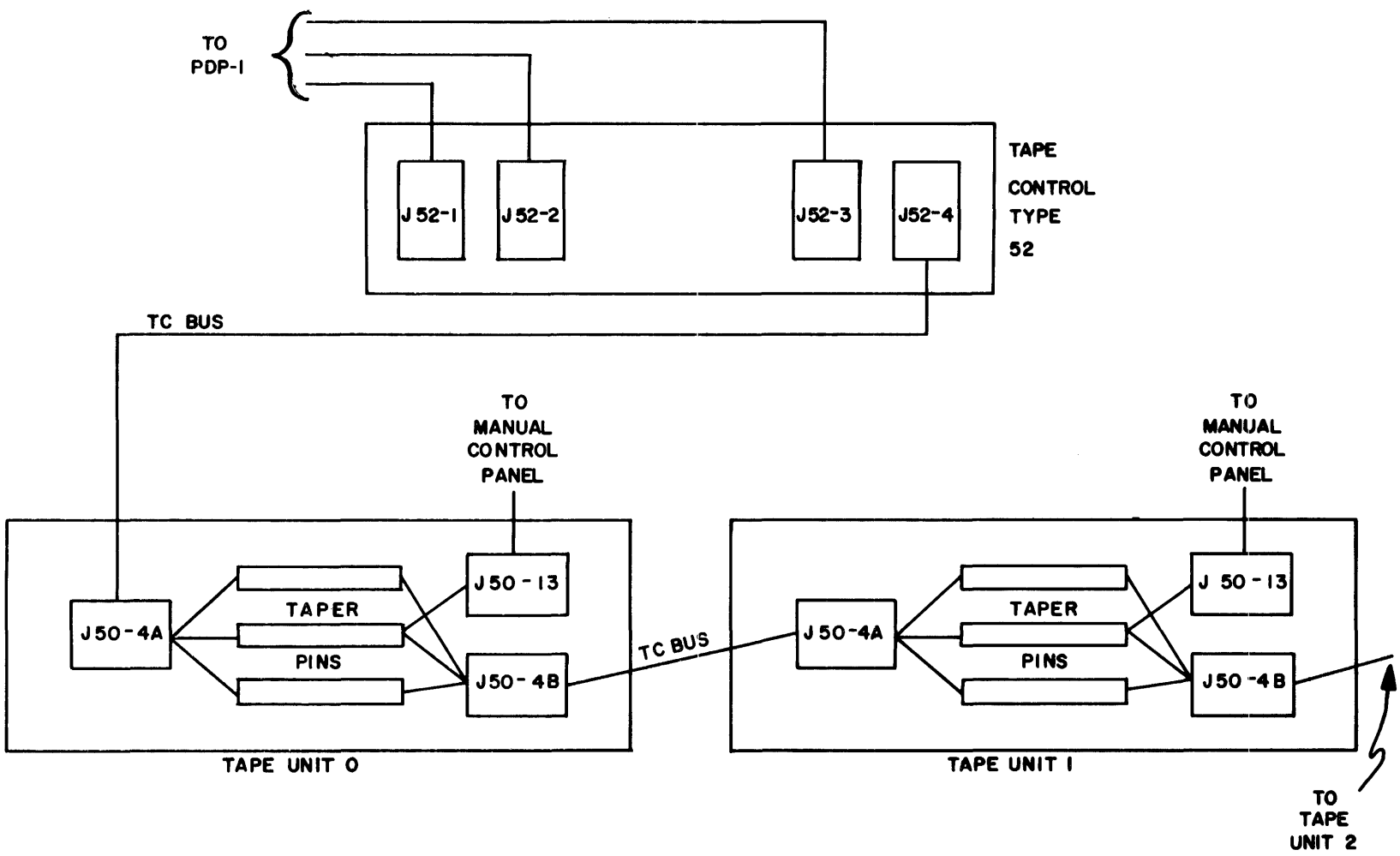


Figure 3-2 Type 52 System Bus Connections

Figure 3-3

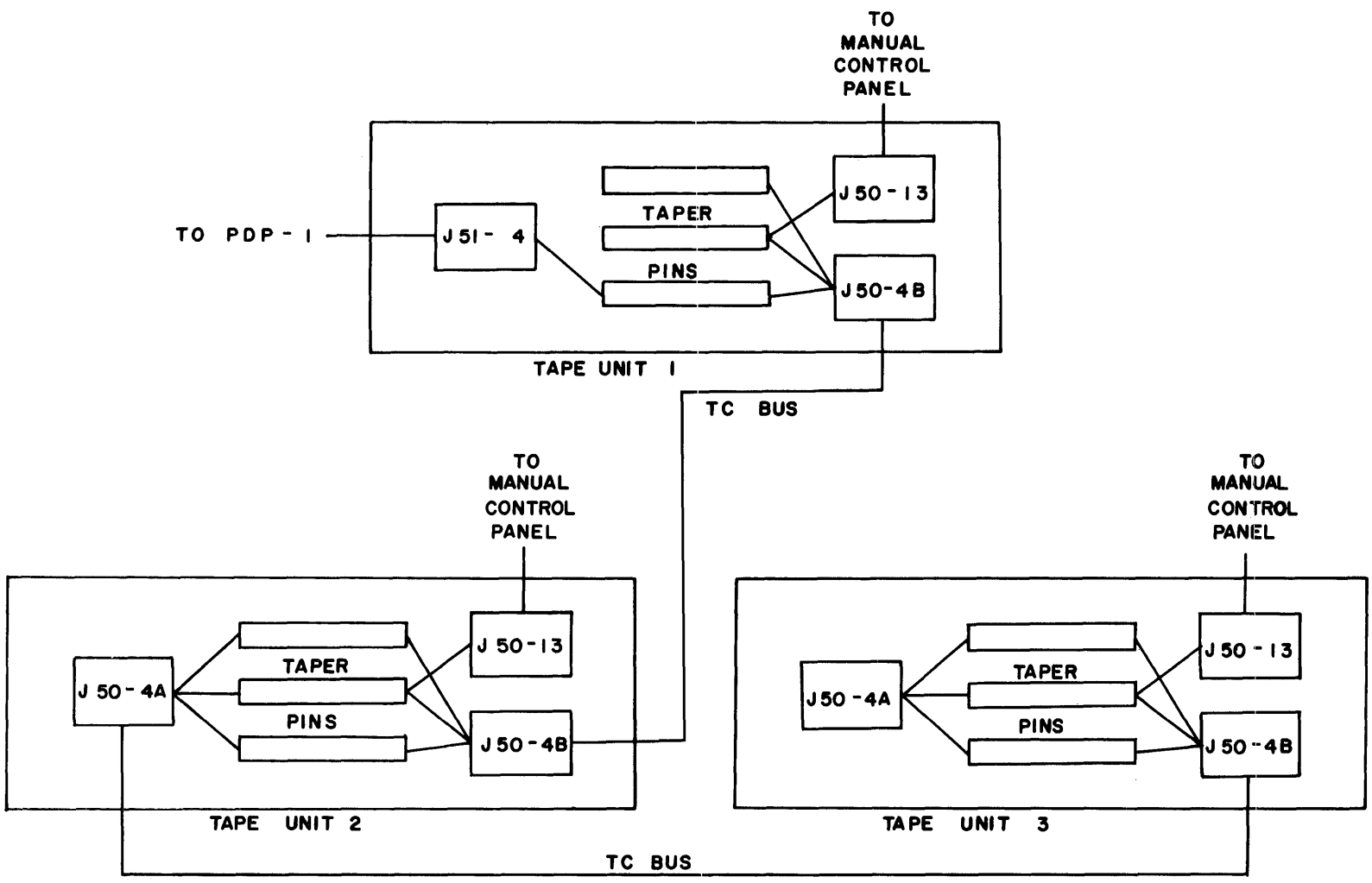


Figure 3-3 Type 51 System Bus Connections

Figure 4-1

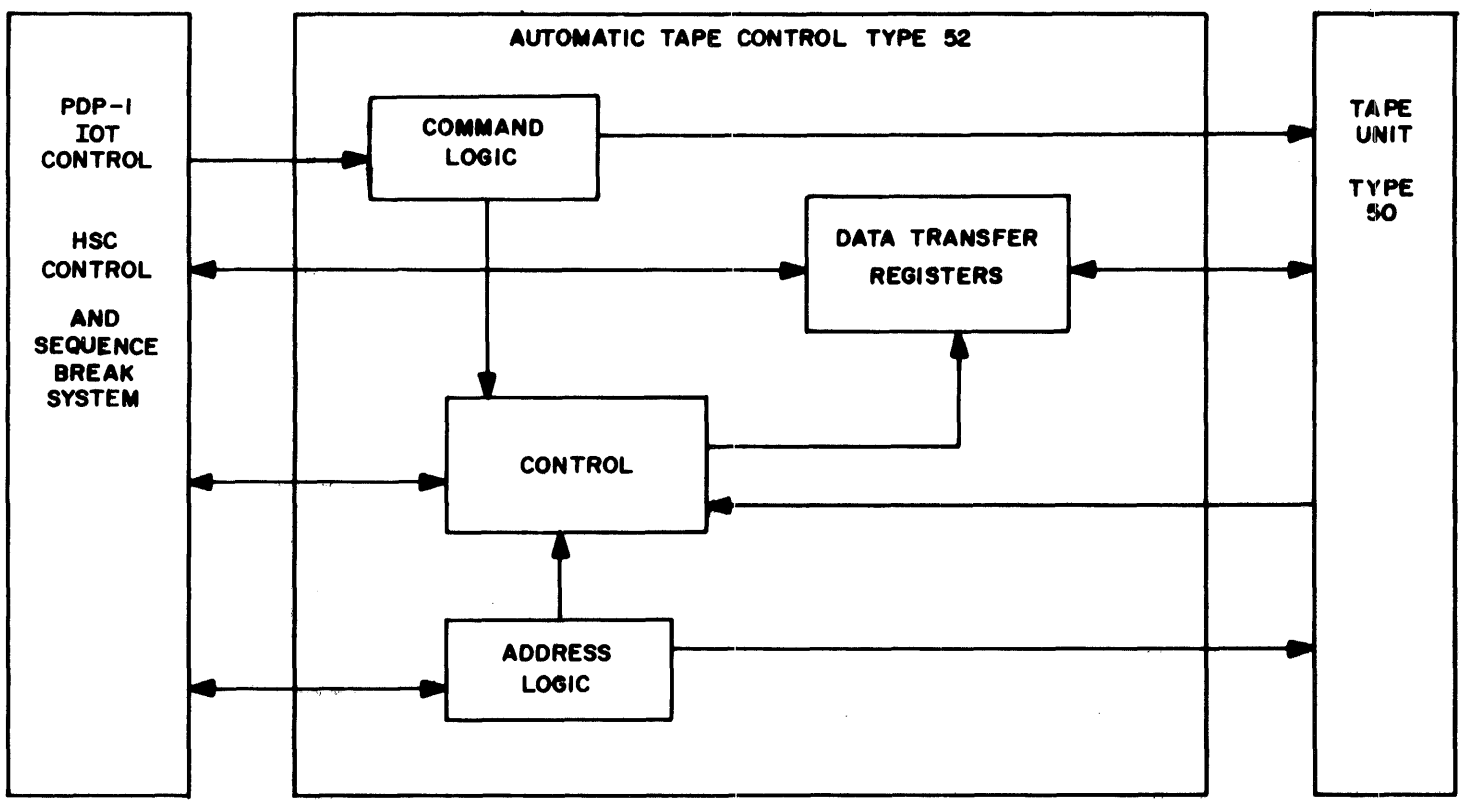


Figure 4-1 Automatic Tape System Block Diagram

Figure 4-2

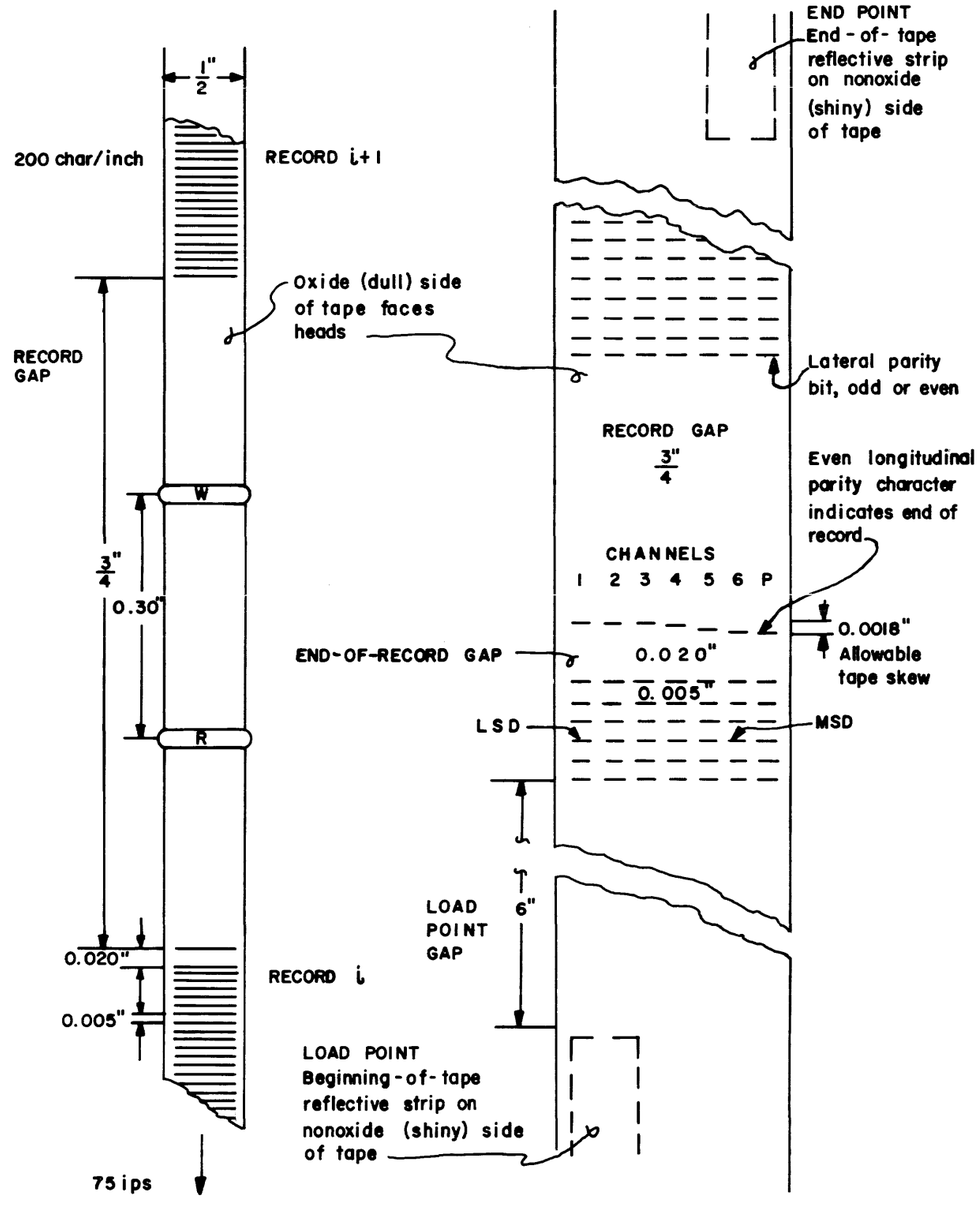


Figure 4-2 Tape Format

Figure 4-3

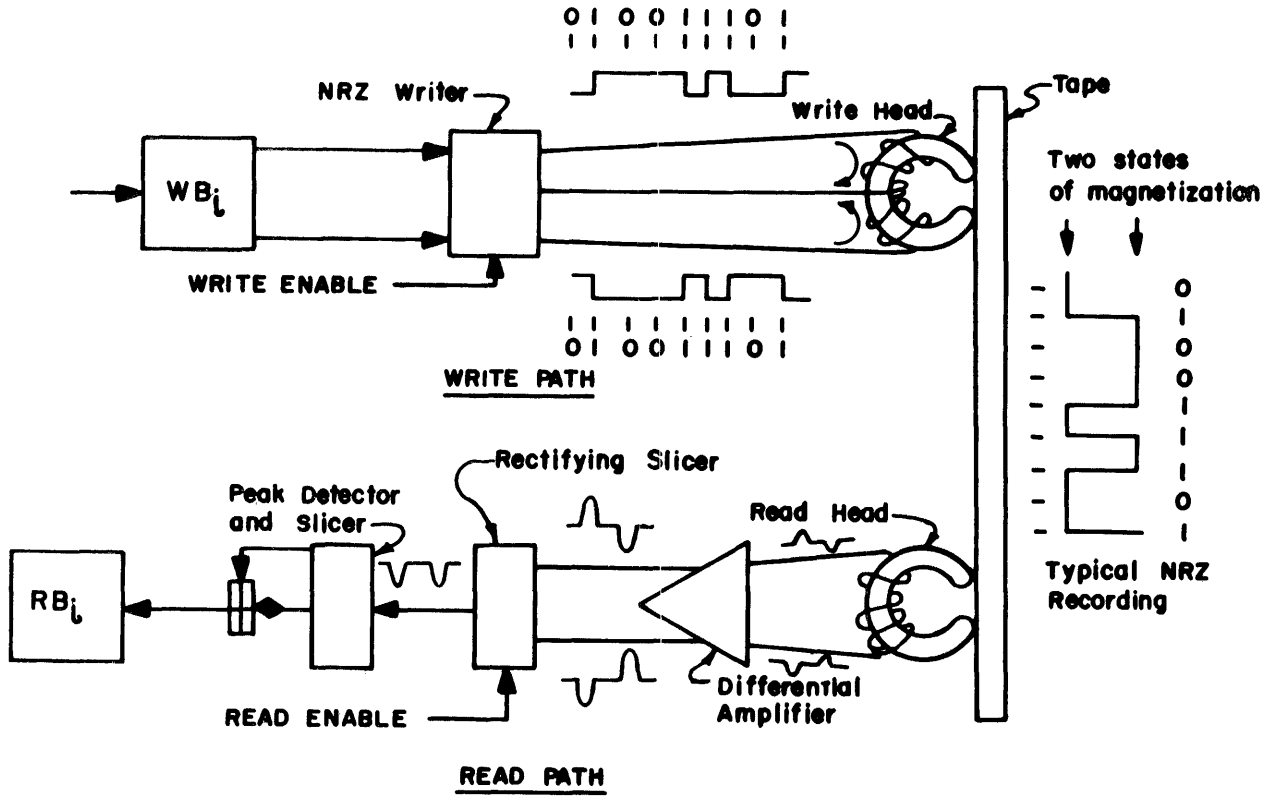


Figure 4-3 Tape Write and Read Signal Flow

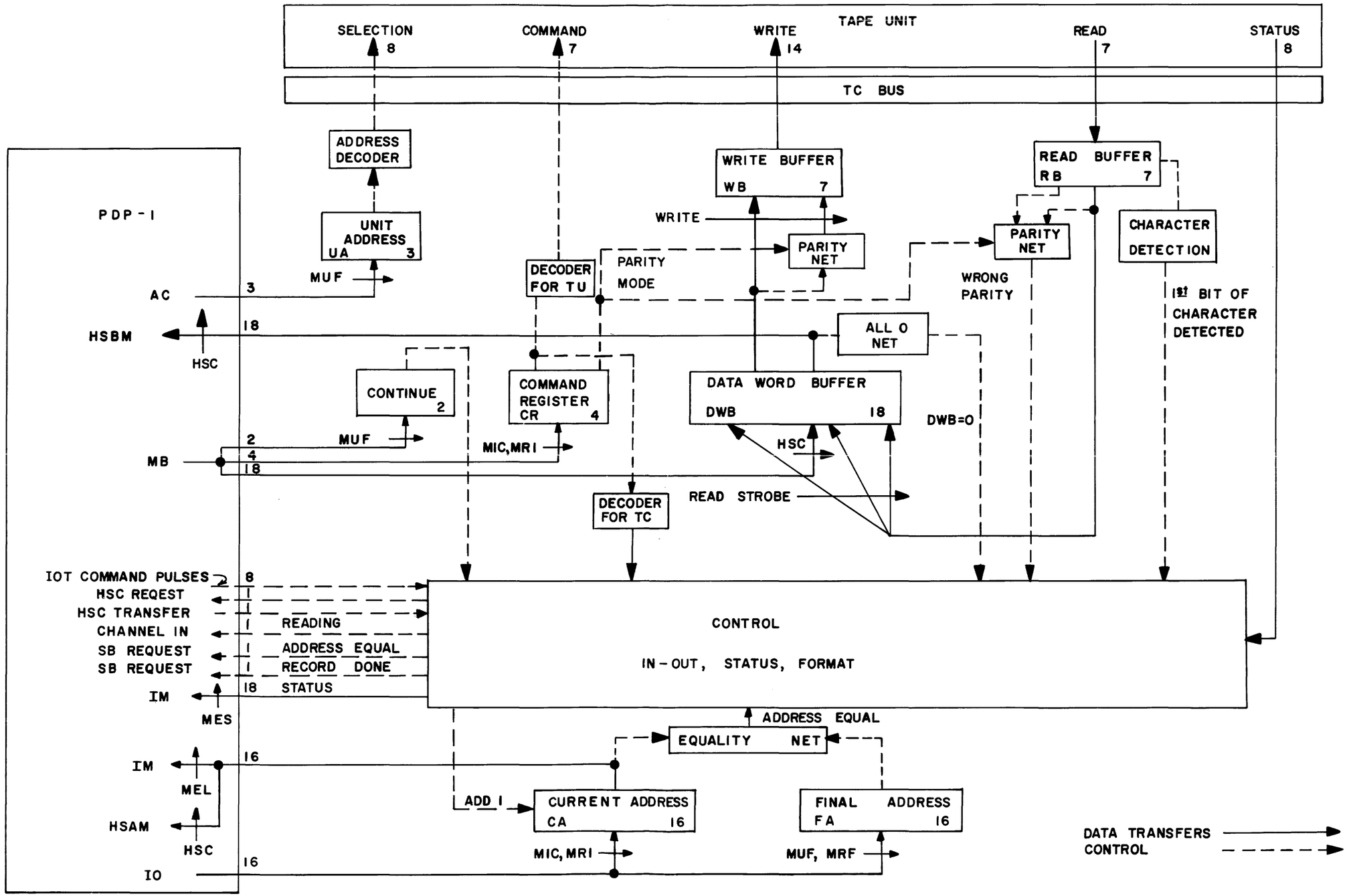


Figure 4-4 Automatic Tape Control 52 Block Diagram

Figure 4-5

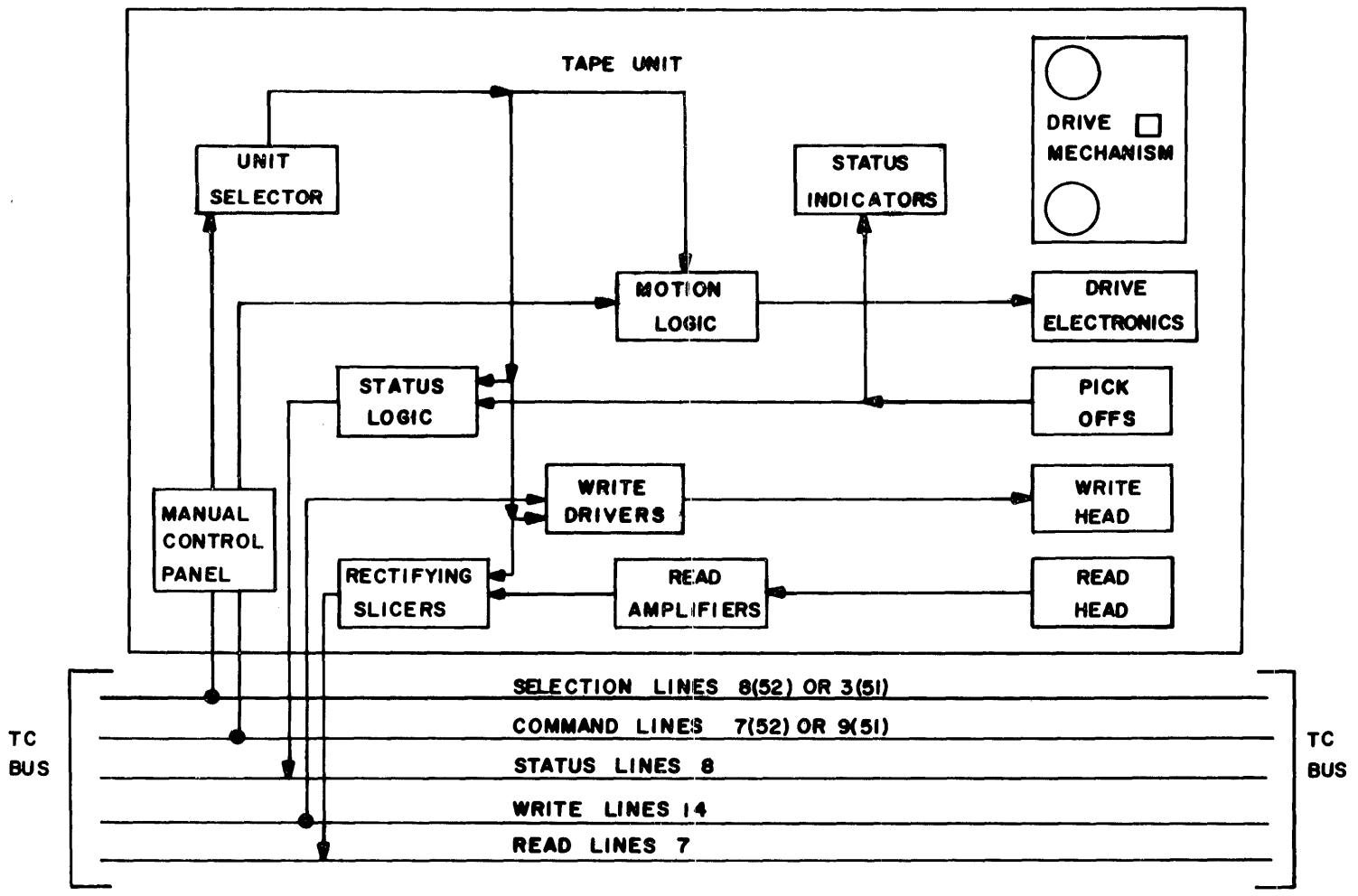


Figure 4-5 Tape Unit 50 Block Diagram

Figure 4-6

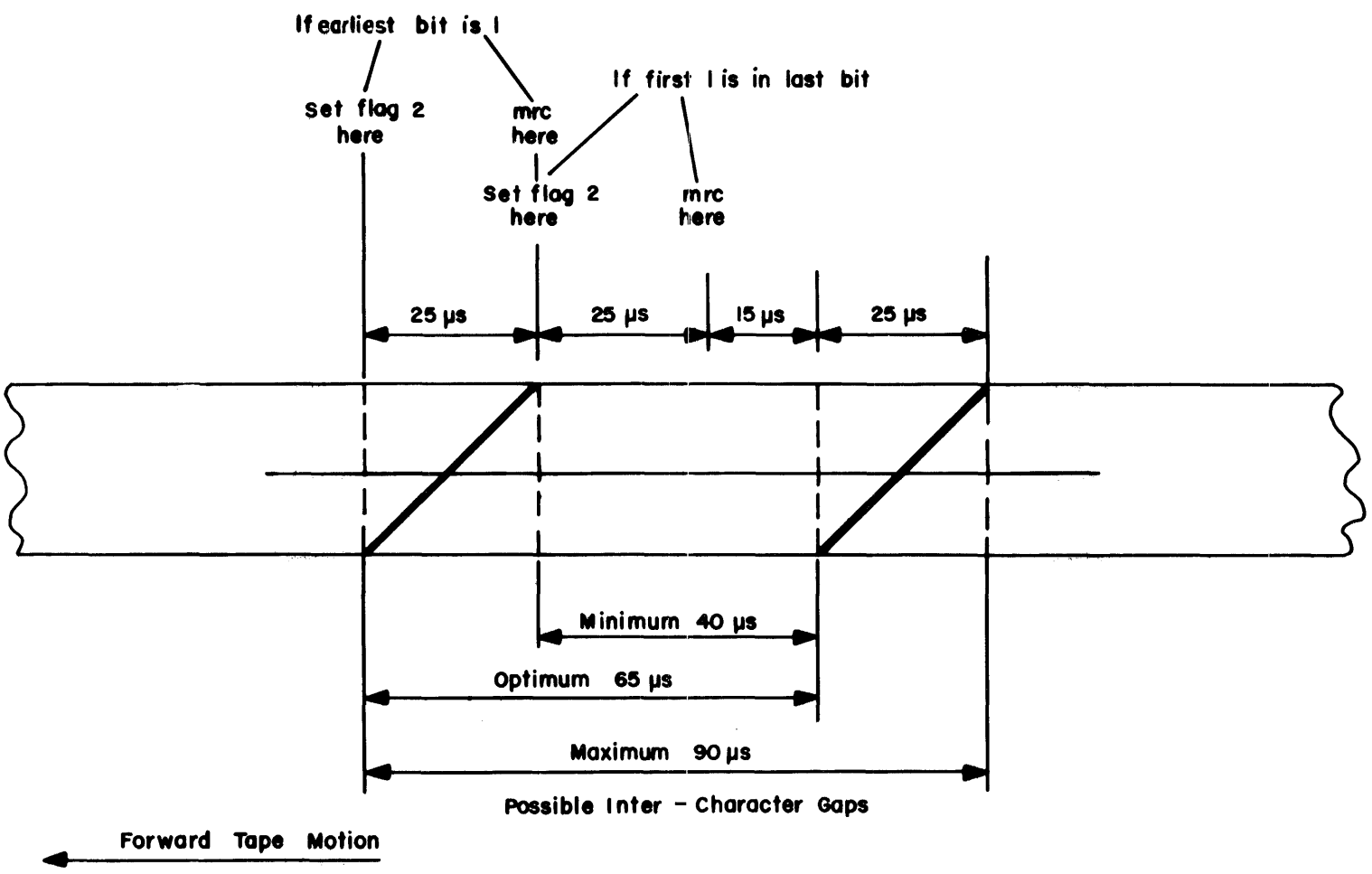


Figure 4-6 Read Timing for Type 51 Programmed Tape System

Figure 4-7

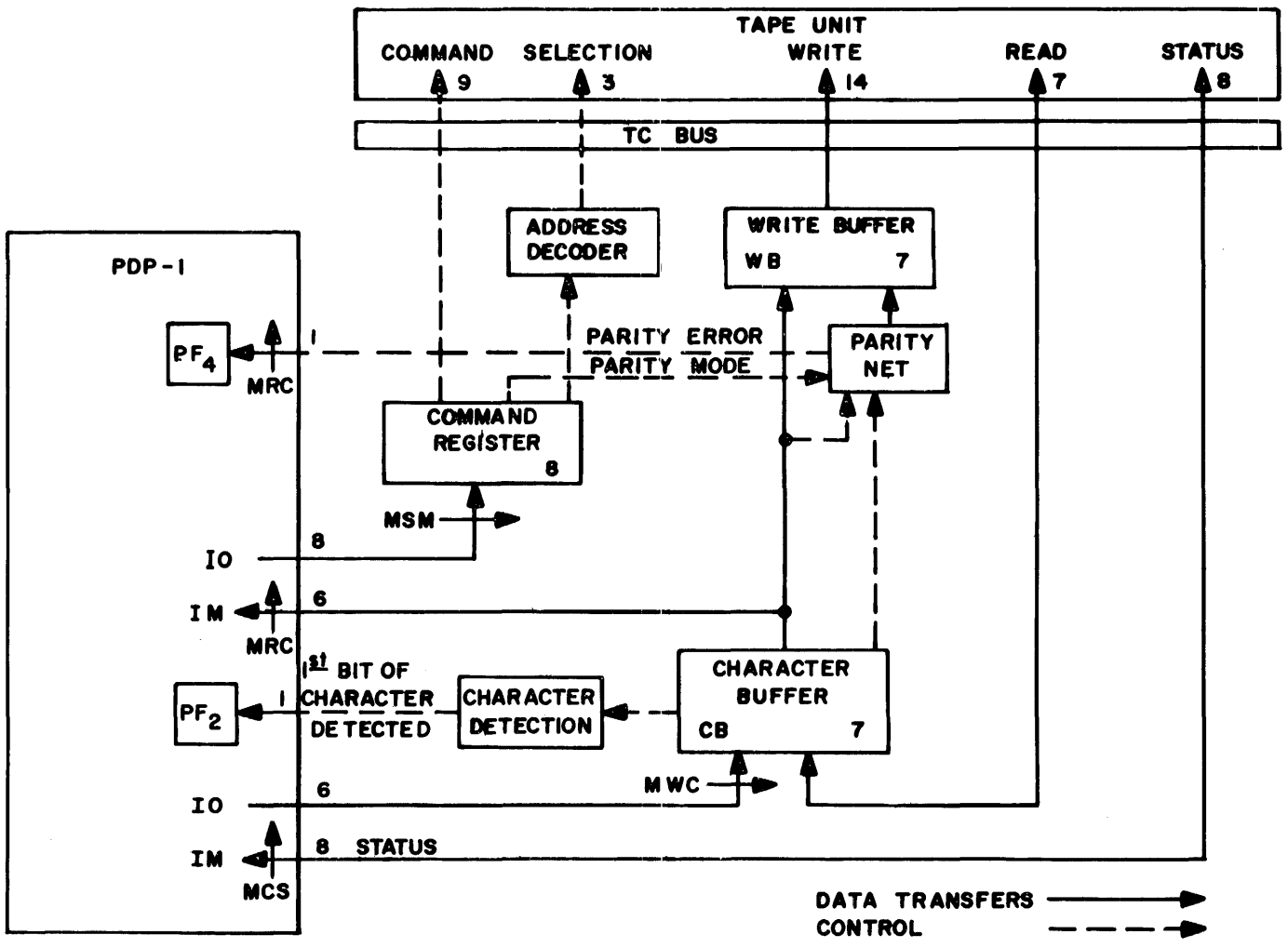


Figure 4-7 Programmed Tape Control 51 Block Diagram

Figure 5-1

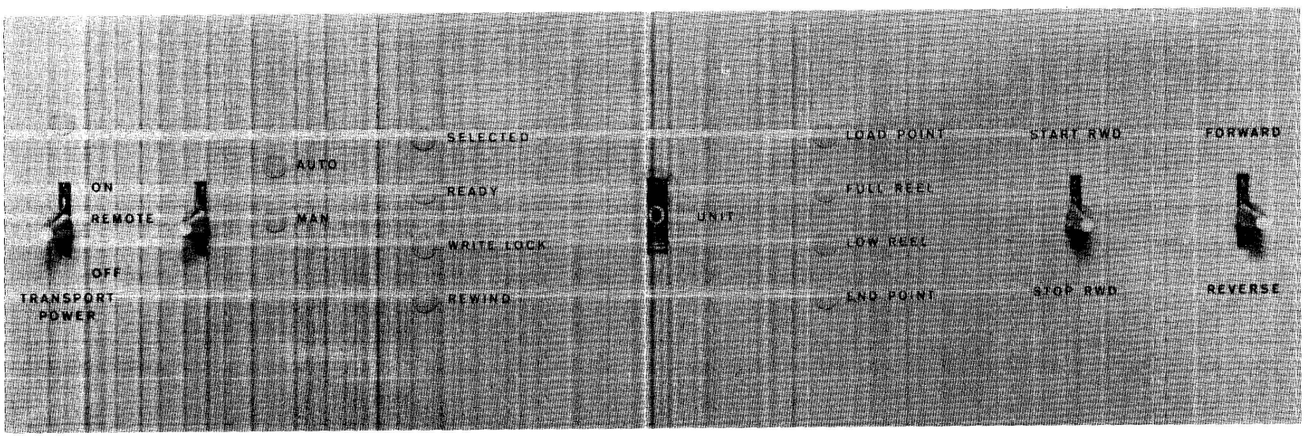


Figure 5-1 Manual Control Panel

Figure 5-2

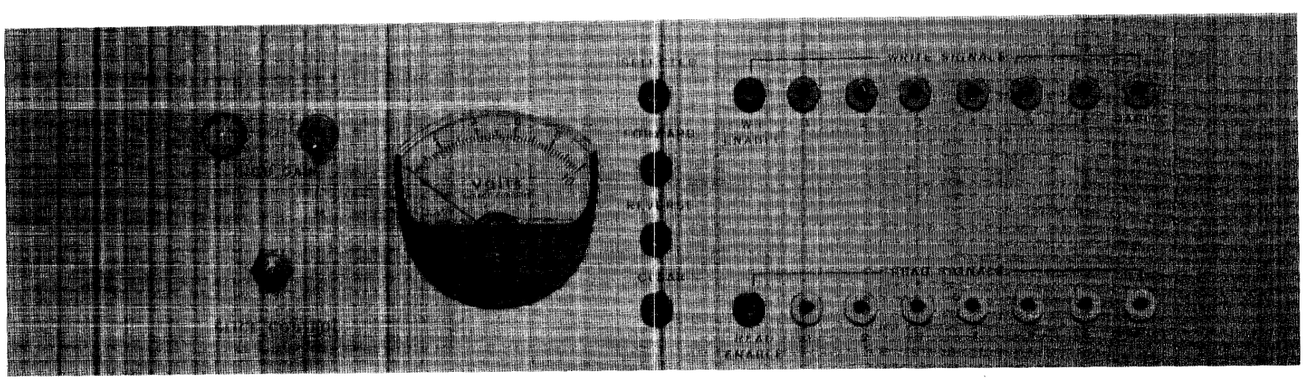


Figure 5-2 Gain, Slice and Test Point Panel

Figure 5-3

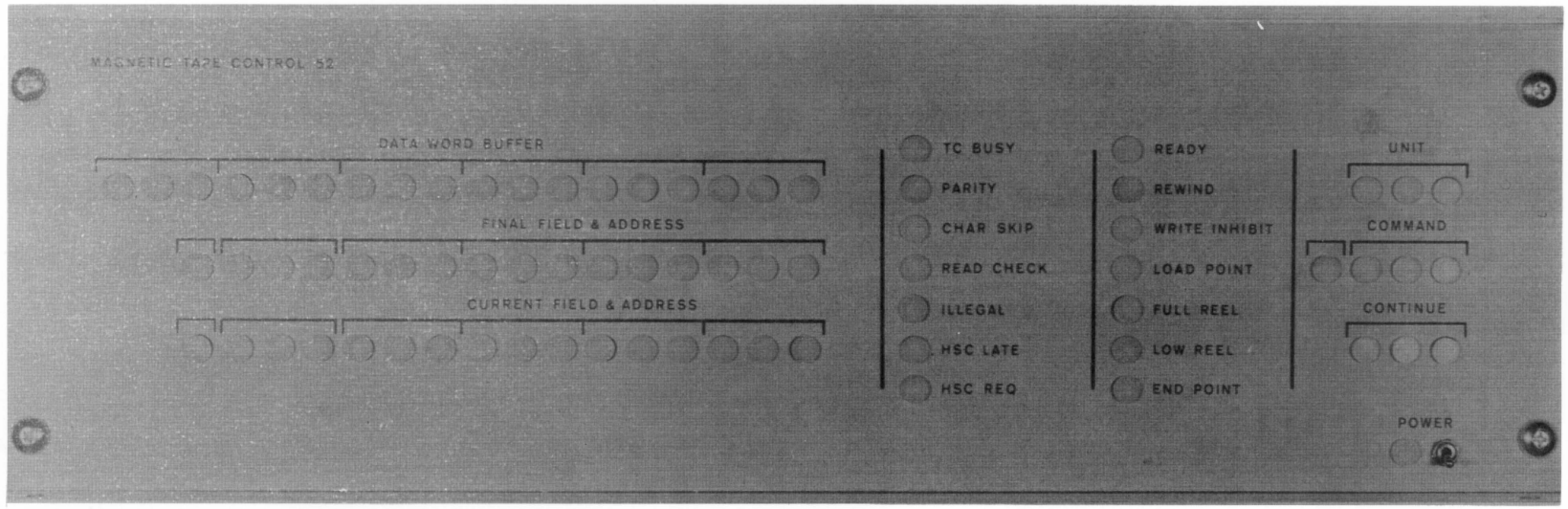


Figure 5-3 Indicator Panel

Figure 5-4

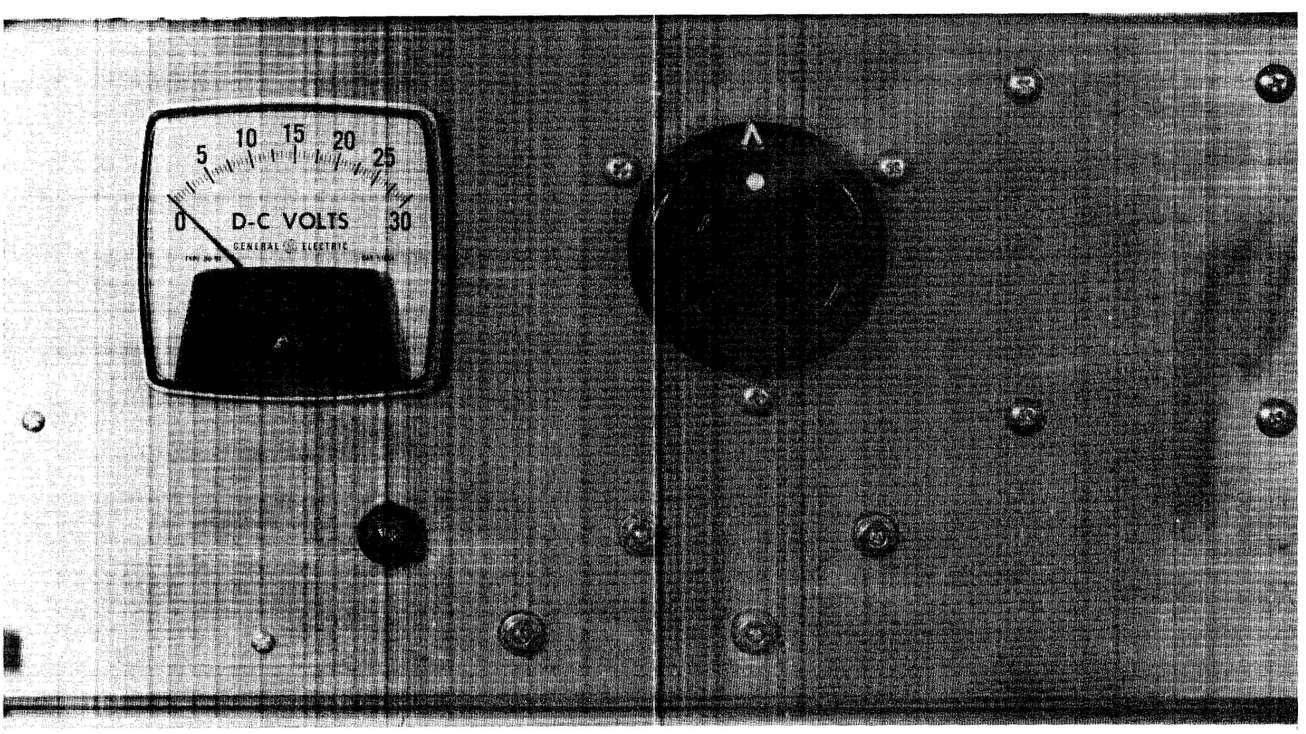


Figure 5-4 Variable Power Supply 734

Figure 5-5

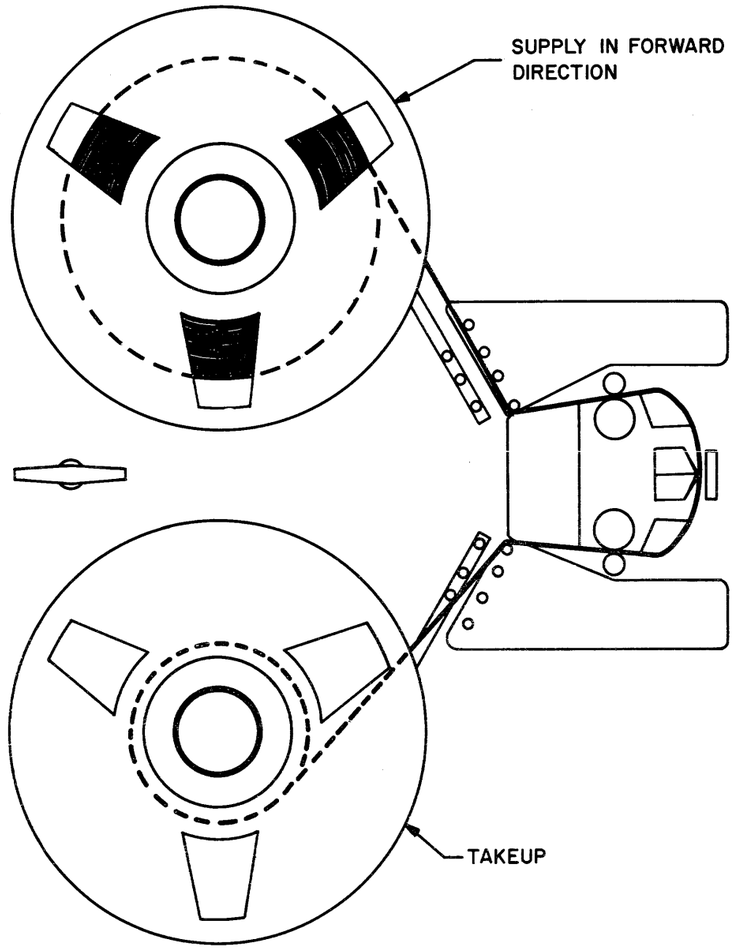


Figure 5-5 Tape Threading

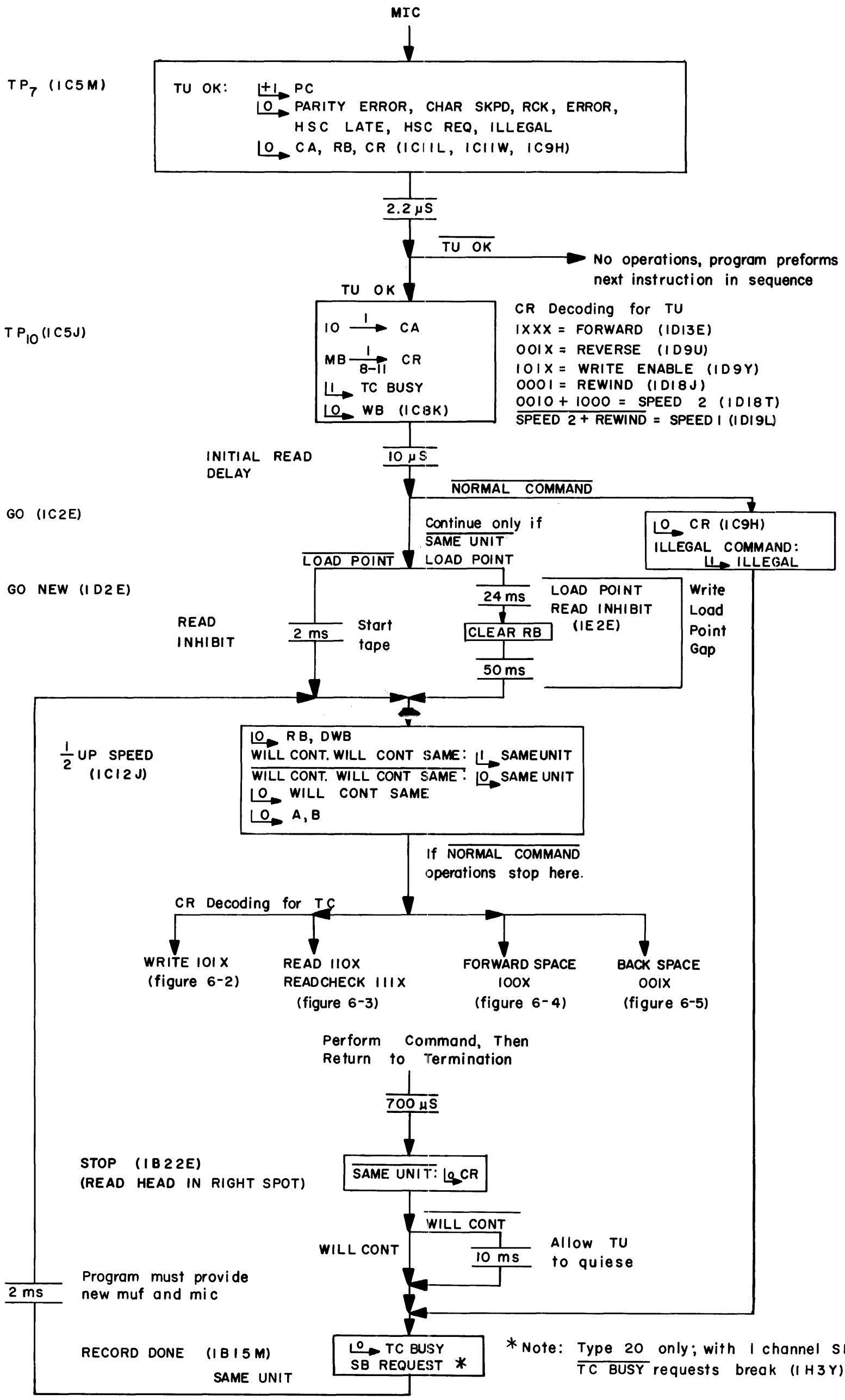


Figure 6-1 Flow Chart: Initiation and Termination of Tape Commands

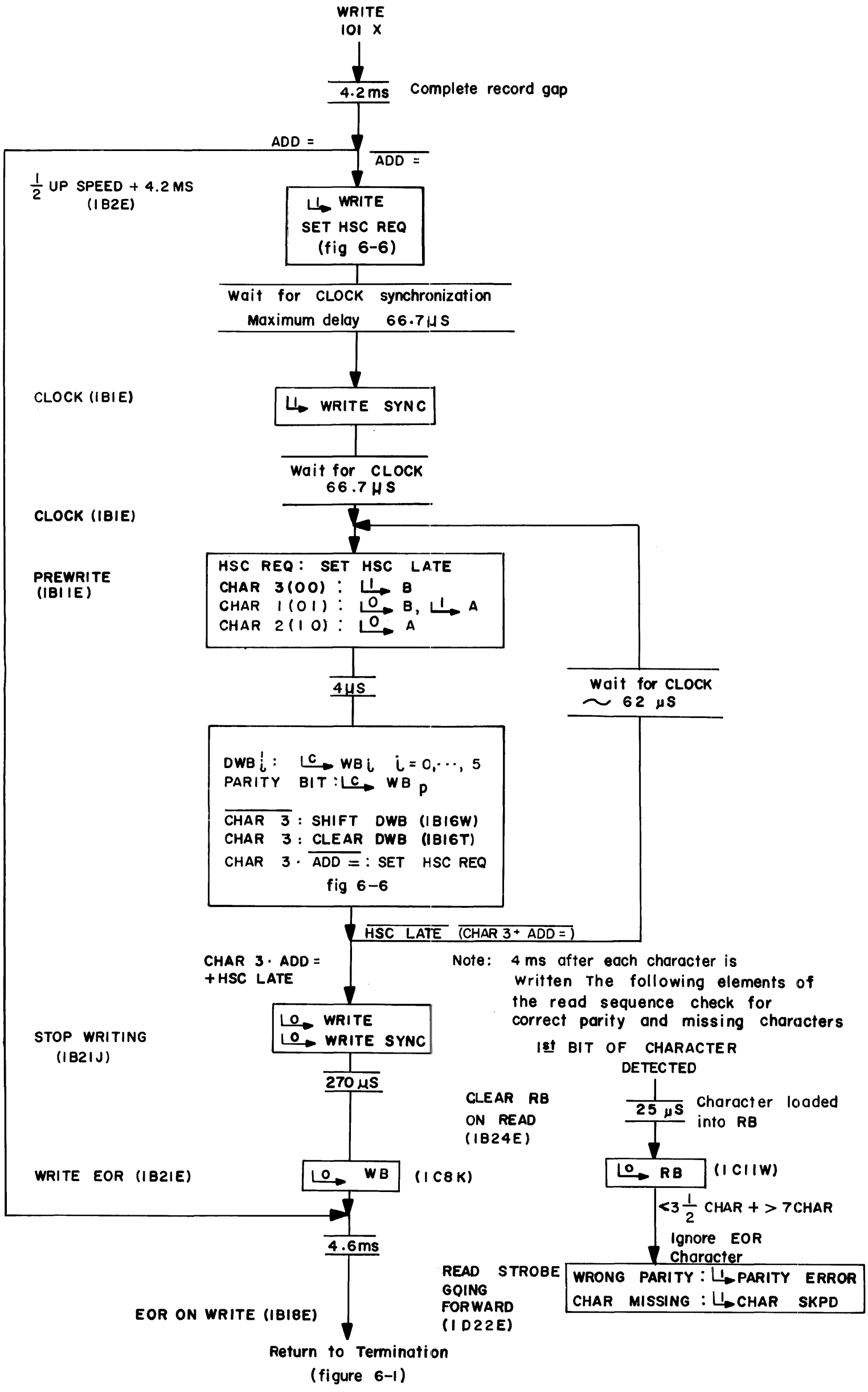


Figure 6-2 Flow Chart: Write

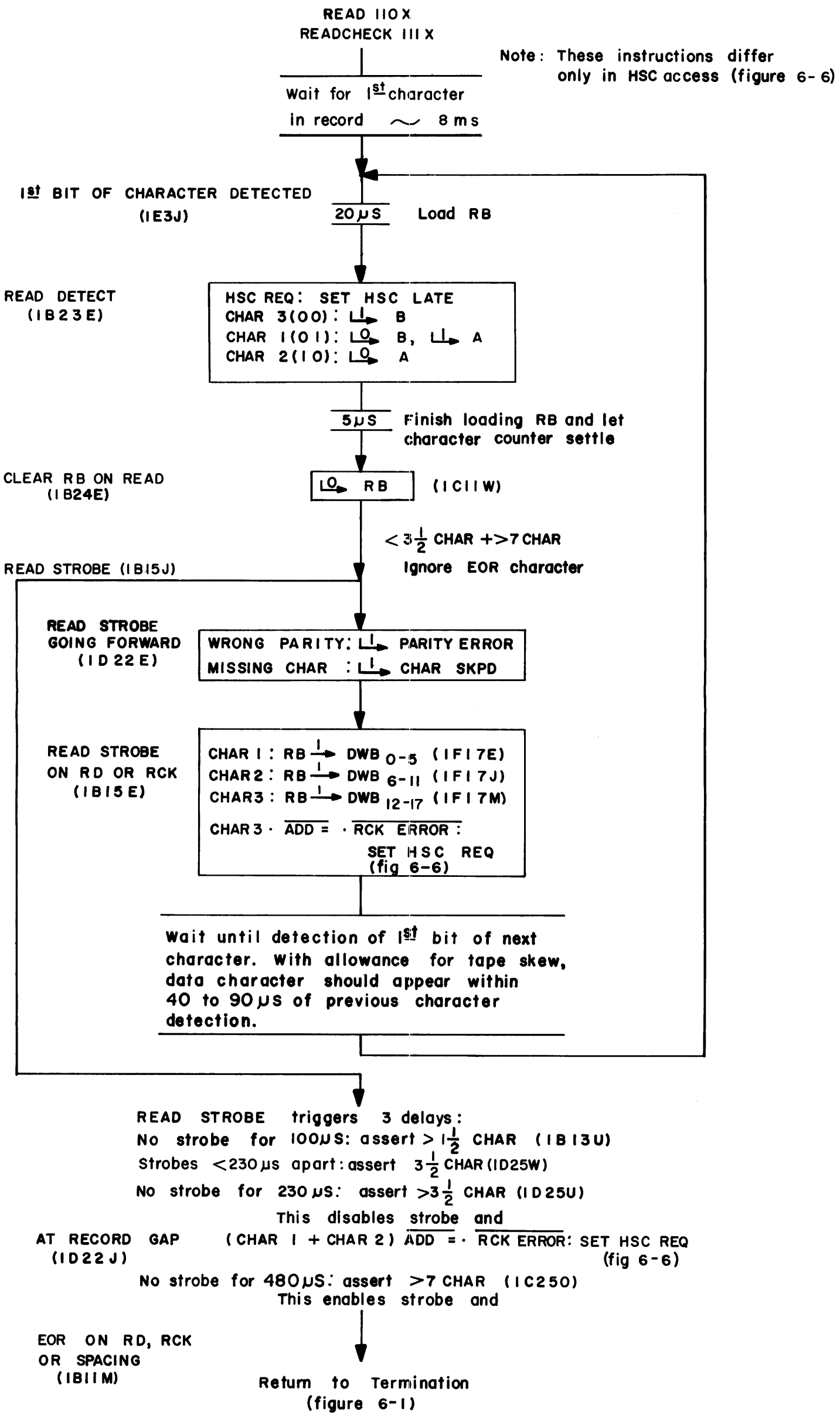


Figure 6-3 Flow Chart: Read and Readcheck

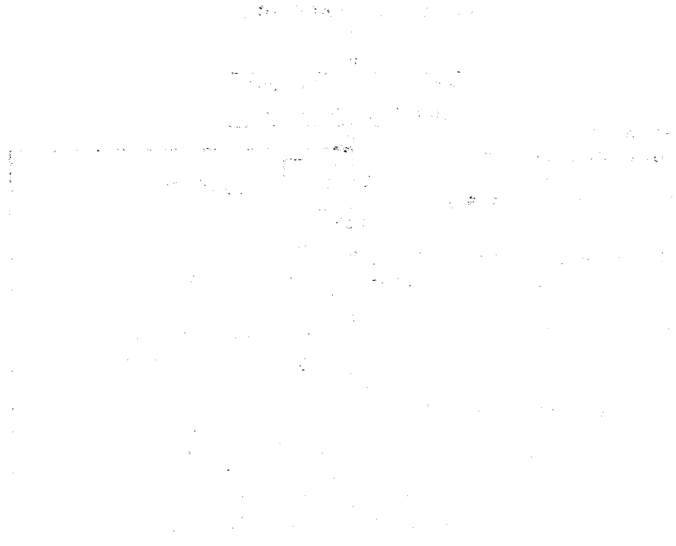


Figure 6-4

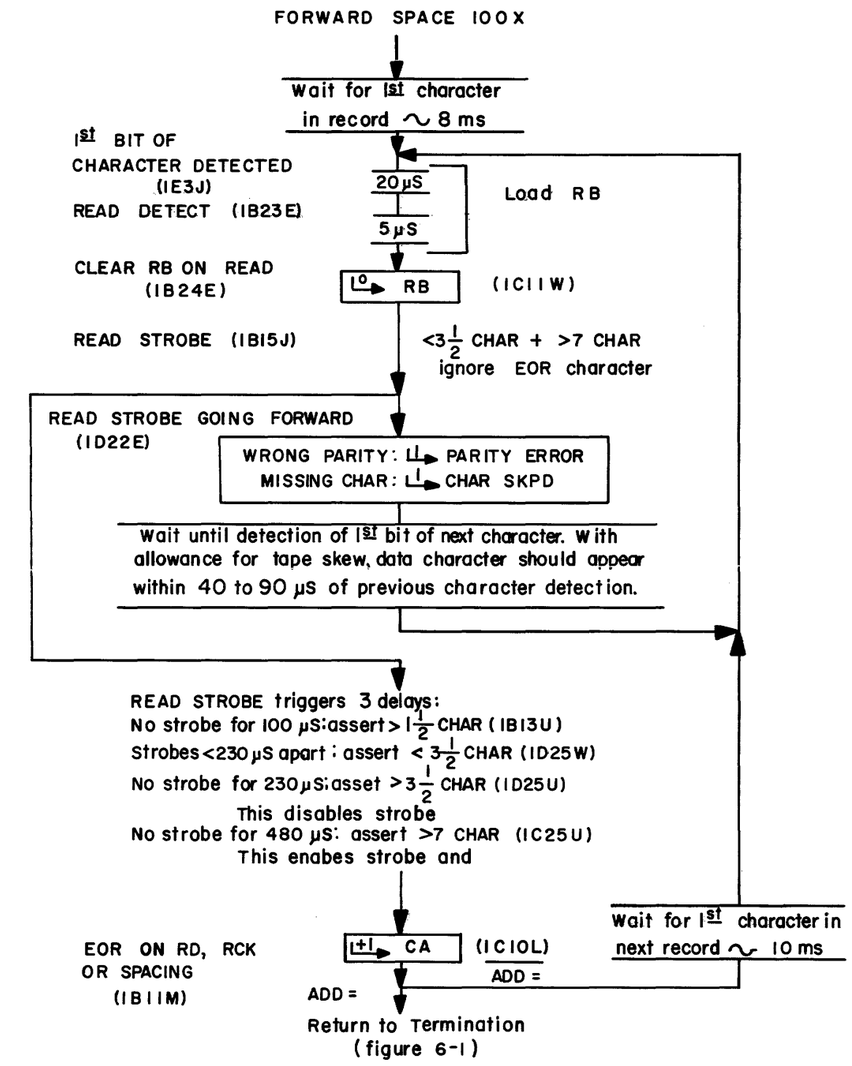


Figure 6-4 Flow Chart: Forward Space

Figure 6-5

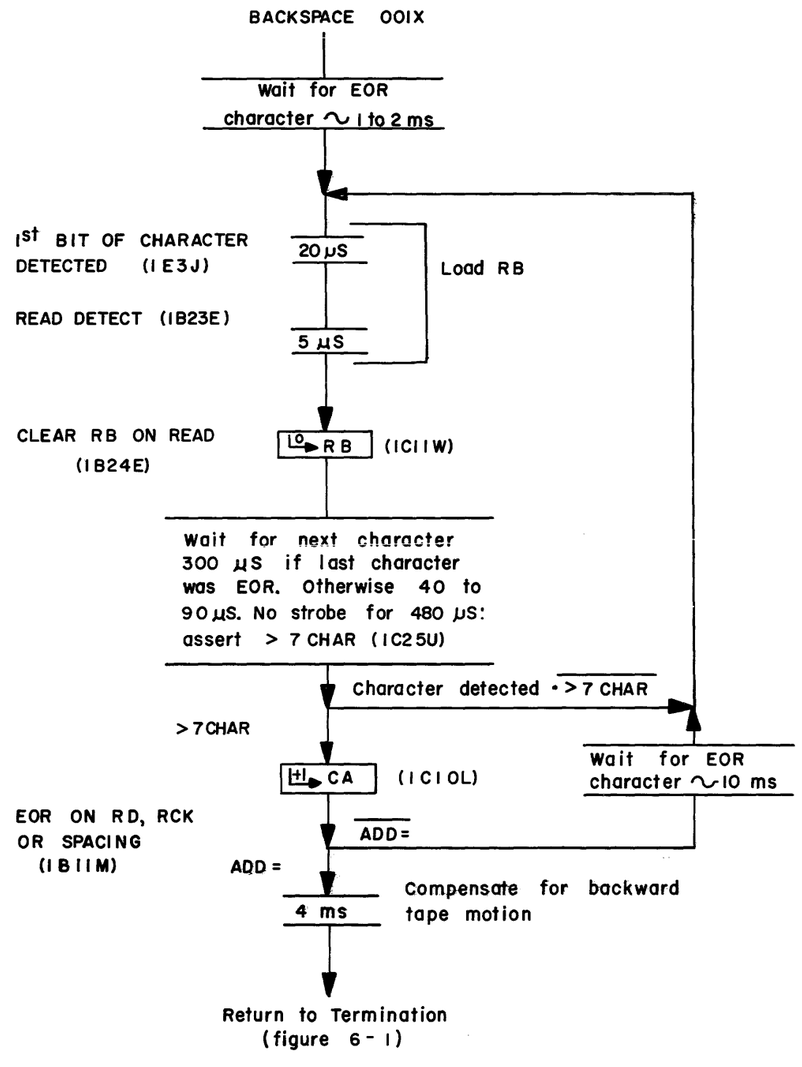


Figure 6-5 Flow Chart: Backspace

Figure 6-6

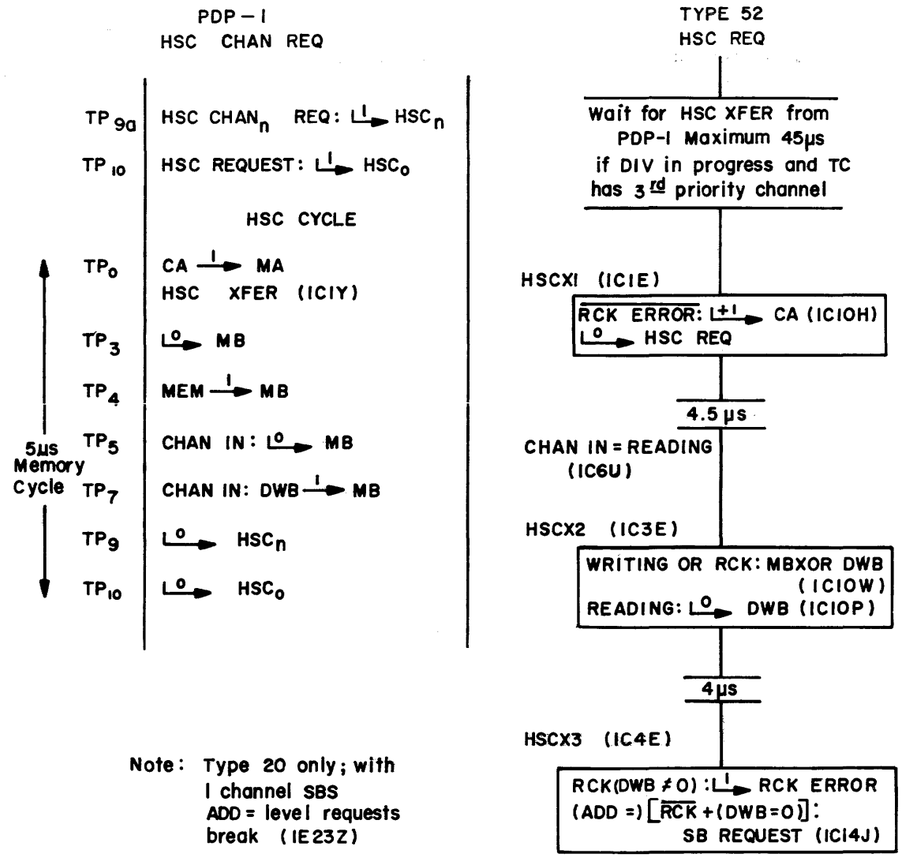


Figure 6-6 Flow Chart: High Speed Channel Access

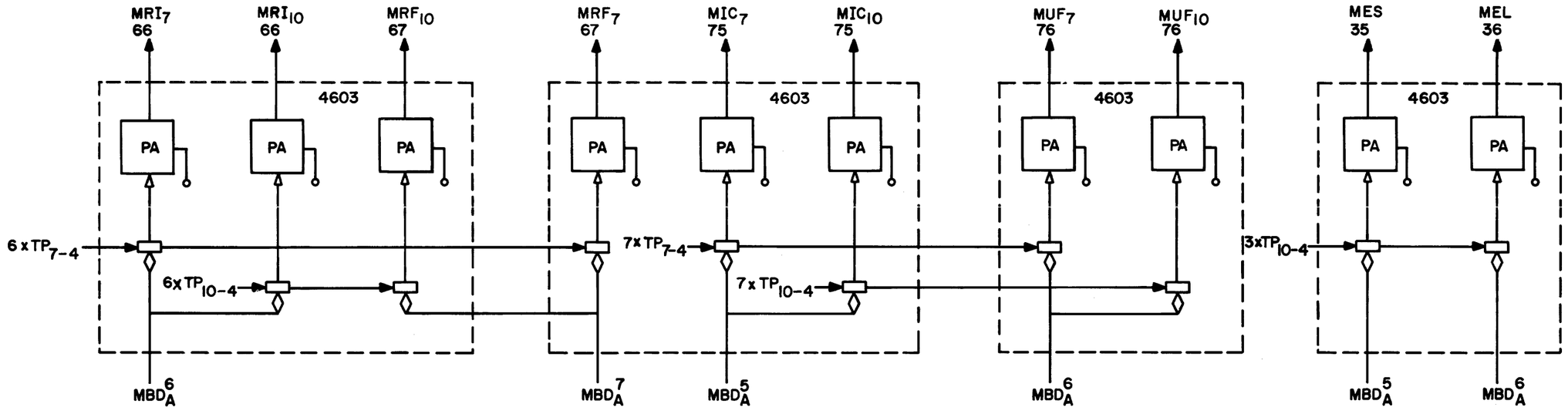


Figure 6-7 IOT Control for Type 52 Tape System

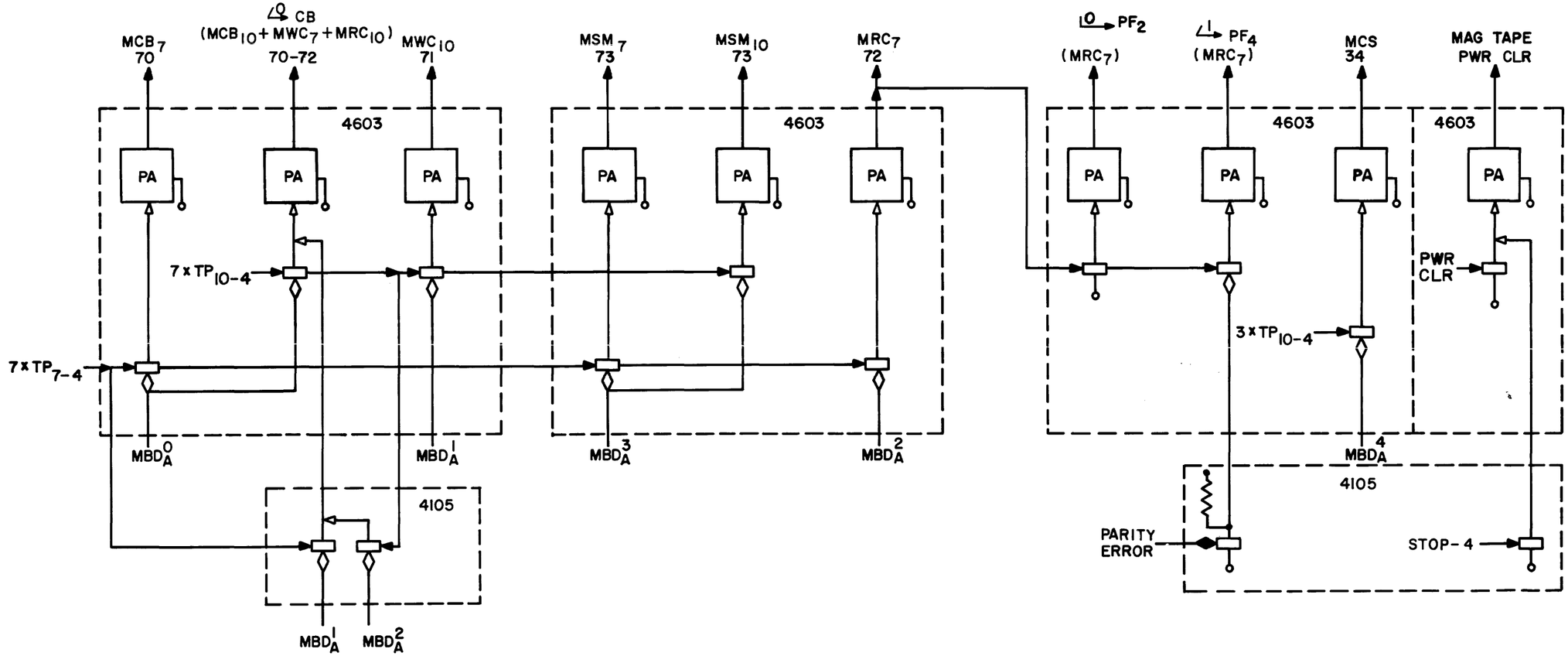


Figure 6-8 IOT Control for Type 51 Tape System

AUTOMATIC SYSTEM

J52-1

	PDP-1		TYPE 52
1			
2			
3	IO^1_2 OUT		$CA_2 FA_2$ IN
4	IO^1_3 OUT		$CA_3 FA_3$ IN
5	IO^1_4 OUT		$CA_4 FA_4$ IN
6	IO^1_5 OUT		$CA_5 FA_5$ IN
7	IO^1_6 OUT		$CA_6 FA_6$ IN
8	IO^1_7 OUT		$CA_7 FA_7$ IN
9	IO^1_8 OUT		$CA_8 FA_8$ IN
10	IO^1_9 OUT		$CA_9 FA_9$ IN
11	IO^1_{10} OUT		$CA_{10} FA_{10}$ IN
12	IO^1_{11} OUT		$CA_{11} FA_{11}$ IN
13	IO^1_{12} OUT		$CA_{12} FA_{12}$ IN
14	IO^1_{13} OUT		$CA_{13} FA_{13}$ IN
15	IO^1_{14} OUT		$CA_{14} FA_{14}$ IN
16	IO^1_{15} OUT		$CA_{15} FA_{15}$ IN
17	IO^1_{16} OUT		$CA_{16} FA_{16}$ IN
18	IO^1_{17} OUT		$CA_{17} FA_{17}$ IN
19	$IM_6 HSAM_6$		CA^1_6 OUT
20	$IM_7 HSAM_7$		CA^1_7 OUT
21	$IM_8 HSAM_8$		CA^1_8 OUT
22	$IM_9 HSAM_9$		CA^1_9 OUT
23	$IM_{10} HSAM_{10}$		CA^1_{10} OUT
24	$IM_{11} HSAM_{11}$		CA^1_{11} OUT
25	$IM_{12} HSAM_{12}$		CA^1_{12} OUT
26	$IM_{13} HSAM_{13}$		CA^1_{13} OUT
27	$IM_{14} HSAM_{14}$		CA^1_{14} OUT
28	$IM_{15} HSAM_{15}$		CA^1_{15} OUT
29	$IM_{16} HSAM_{16}$		CA^1_{16} OUT
30	$IM_{17} HSAM_{17}$		CA^1_{17} OUT
31	IM_0		ERROR
32	IM_1		PARITY ERROR
33	IM_2		CHAR SKPD
34	IM_3		TC BUSY
35	IM_4		RCK ERROR
36	IM_6		HSC LATE
37	IM_{15}		END POINT
38	IM_{10}		REWIND
39	IM_8		READY
40	IM_9		AUTO
41	IM_{11}		WRITE LOCKOUT
42	IM_{13}		FULL REEL
43	IM_{14}		LOW REEL
44	IM_{12}		LOAD POINT
45	IM_7 1 CH SBS		ADDRESS EQUAL
46	IM_{16}		WILL CONT
47	IM_{17}		WILL CONT SAME
48	IM_5		ILLEGAL
49			
50	GND		GND

J52-2

	PDP-1		TYPE 52
1	$HSBM_0$		DWB^1_0 OUT
2	$HSBM_1$		DWB^1_1 OUT
3	$HSBM_2$		DWB^1_2 OUT
4	$HSBM_3$		DWB^1_3 OUT
5	$HSBM_4$		DWB^1_4 OUT
6	$HSBM_5$		DWB^1_5 OUT
7	$HSBM_6$		DWB^1_6 OUT
8	$HSBM_7$		DWB^1_7 OUT
9	$HSBM_8$		DWB^1_8 OUT
10	$HSBM_9$		DWB^1_9 OUT
11	$HSBM_{10}$		DWB^1_{10} OUT
12	$HSBM_{11}$		DWB^1_{11} OUT
13	$HSBM_{12}$		DWB^1_{12} OUT
14	$HSBM_{13}$		DWB^1_{13} OUT
15	$HSBM_{14}$		DWB^1_{14} OUT
16	$HSBM_{15}$		DWB^1_{15} OUT
17	$HSBM_{16}$		DWB^1_{16} OUT
18	$HSBM_{17}$		DWB^1_{17} OUT
19	MB^1_0 OUT		DWB_0 IN
20	MB^1_1 OUT		DWB_1 IN
21	MB^1_2 OUT		DWB_2 IN
22	MB^1_3 OUT		DWB_3 IN
23	MB^1_4 OUT		DWB_4 IN
24	MB^1_5 OUT		DWB_5 IN
25	MB^1_6 OUT		DWB_6 IN
26	MB^1_7 OUT		DWB_7 IN
27	MB^1_8 OUT		DWB_8 IN
28	MB^1_9 OUT		DWB_9 IN
29	MB^1_{10} OUT		DWB_{10} IN
30	MB^1_{11} OUT		DWB_{11} IN
31	MB^1_{12} OUT		DWB_{12} IN
32	MB^1_{13} OUT		DWB_{13} IN
33	MB^1_{14} OUT		DWB_{14} IN
34	MB^1_{15} OUT		DWB_{15} IN
35	MB^1_{16} OUT		DWB_{16} IN
36	MB^1_{17} OUT		DWB_{17} IN
37	MB^1_8 OUT		CR_8 IN
38	MB^1_9 OUT		CR_9 IN
39	MB^1_{10} OUT		CR_{10} IN
40	MB^1_{11} OUT		CR_{11} IN
41			
42			
43	$IM_2 HSAM_2$		CA^1_2 OUT
44	$IM_3 HSAM_3$		CA^1_3 OUT
45	$IM_4 HSAM_4$		CA^1_4 OUT
46	$IM_5 HSAM_5$		CA^1_5 OUT
47	AC^1_{15} OUT		UA_4 IN
48	AC^1_{16} OUT		UA_2 IN
49	AC^1_{17} OUT		UA_1 IN
50	GND		GND

J52-3

	PDP-1		TYPE 52
1	GND		GND
2	HSC WORD XFER		HSC XFER
3	HSC CHAN IN		HREADING
4	1 CHAN SBS		TC BUSY
5	HSC CHAN REQ		HSC REQ
6	GND		GND
7	MUP_{10} 76		$IO^1 \rightarrow PA, AC^1 \rightarrow UA$
8			
9	GND		GND
10	GND		GND
11	+1 → PC		MUP+MIC OK
12	GND		GND
13	$TP_4 \rightarrow 4$		TF_4 SYNC
14			
15	SB REQUEST		RECORD DONE
16	GND		GND
17			
18	GND		GND
19	MIC_{10} 75		$IO^1 \rightarrow CA, MB^1 \rightarrow CR$
20	GND		GND
21	MIC_7 75		$\rightarrow CA, CR, RB, SR$
22	GND		GND
23	STOP-4		$\rightarrow CR, TU$
24			
25			
26			
27	GND		GND
28	MUP_7 76		$\rightarrow PA, UA$
29			
30	SC-4		CLEAR TC
31	GND		GND
32	MB^1_{11} OUT		WILL CONT SAME
33	MB^1_{10} OUT		WILL CONT
34	GND		GND
35	MRP_7 67		$IO \rightarrow PA$
36	GND		GND
37	MRP_{10} 67		$IO^1 \rightarrow PA$
38			
39	MRI_7 66		$IO \rightarrow CA$
40	GND		GND
41			
42			
43	GND		GND
44	MRI_{10} 66		$IO^1 \rightarrow CA$
45	GND		GND
46	SB REQUEST		ADDRESS EQUAL
47			
48			
49	POWER -15V TURN ON		TO 811
50	GND		GND

PROGRAMMED SYSTEM

J51-4

	PDP-1		TYPE 51
1	IO^1_0 OUT		CB_5 IN
2	IO^1_1 OUT		CB_4 IN
3	IO^1_2 OUT		CB_3 IN
4	IO^1_3 OUT		CB_2 IN
5	IO^1_4 OUT		CB_1 IN
6	IO^1_5 OUT		CB_0 IN
7	IO^1_{11} OUT		REWIND
8	IO^1_{12} OUT		REVERSE
9	IO^1_{13} OUT		WRITE
10	IO^1_{14} OUT		EVEN PARITY
11	IO^1_{15} OUT		LO SPEED
12	IO^1_{16} OUT		A IN
13	IO^1_{17} OUT		B IN
14	IM_{12}		CB^1_0 OUT
15	IM_{13}		CB^1_1 OUT
16	IM_{14}		CB^1_2 OUT
17	IM_{15}		CB^1_3 OUT
18	IM_{16}		CB^1_4 OUT
19	IM_{17}		CB^1_5 OUT
20	IO^1_{10} OUT		OPERATE
21	IM_0		READY
22	IM_1		REWIND
23	IM_2		WRITE LOCKOUT
24	IM_3		LOAD POINT
25	IM_4		FULL REEL
26	IM_5		LOW REEL
27	IM_6		END POINT
28	IM_7		AUTO
29	TEST PURPOSES ONLY		
30	$\rightarrow PP_2$		1st BIT OF CHAR
31	TEST PURPOSES ONLY		
32	SC-4		CLEAR
33	GND		GND
34	GND		GND
35	POWER CLEAR + STOP		$\rightarrow$ TU & COMMAND
36	GND		GND
37	$MBC_{10} \cdot MWC_7 \cdot MRC_{10}$		$\rightarrow CB$
38	GND		GND
39	MSM_7 73		$\rightarrow$ COMMAND
40	GND		GND
41	MCB_7 70		$\rightarrow WB$
42	GND		GND
43	MWC_{10} 72		LOAD CB
44	GND		GND
45	MSM_{10} 73		LOAD COMMAND
46	-15V POWER TURN ON		TO 811 & 822
47	PARITY ERROR		PARITY ERROR
48	GND		GND
49			
50	GND		GND

Figure 6-9 Signal Connections: PDP-1 to Magnetic Tape System

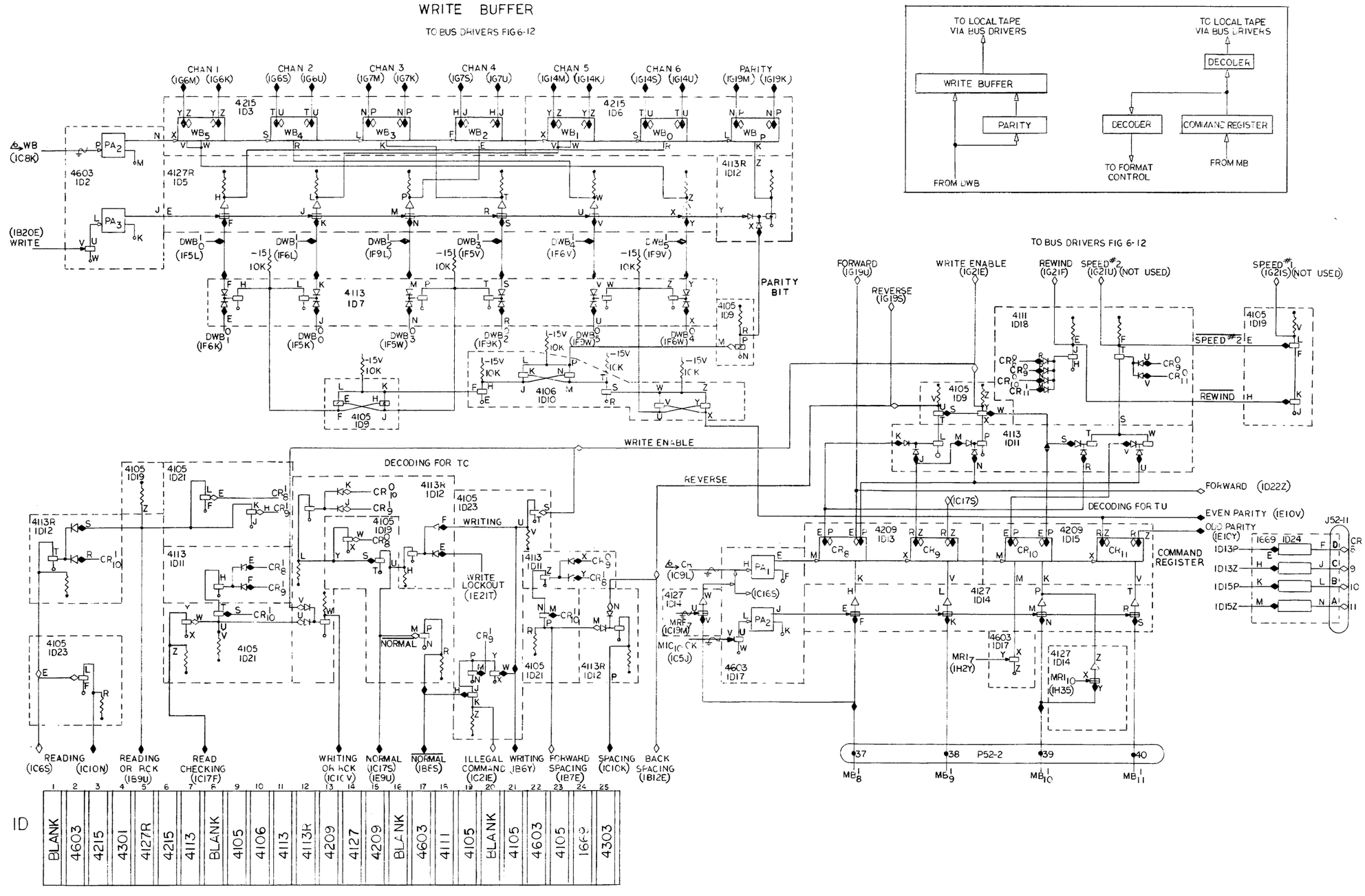
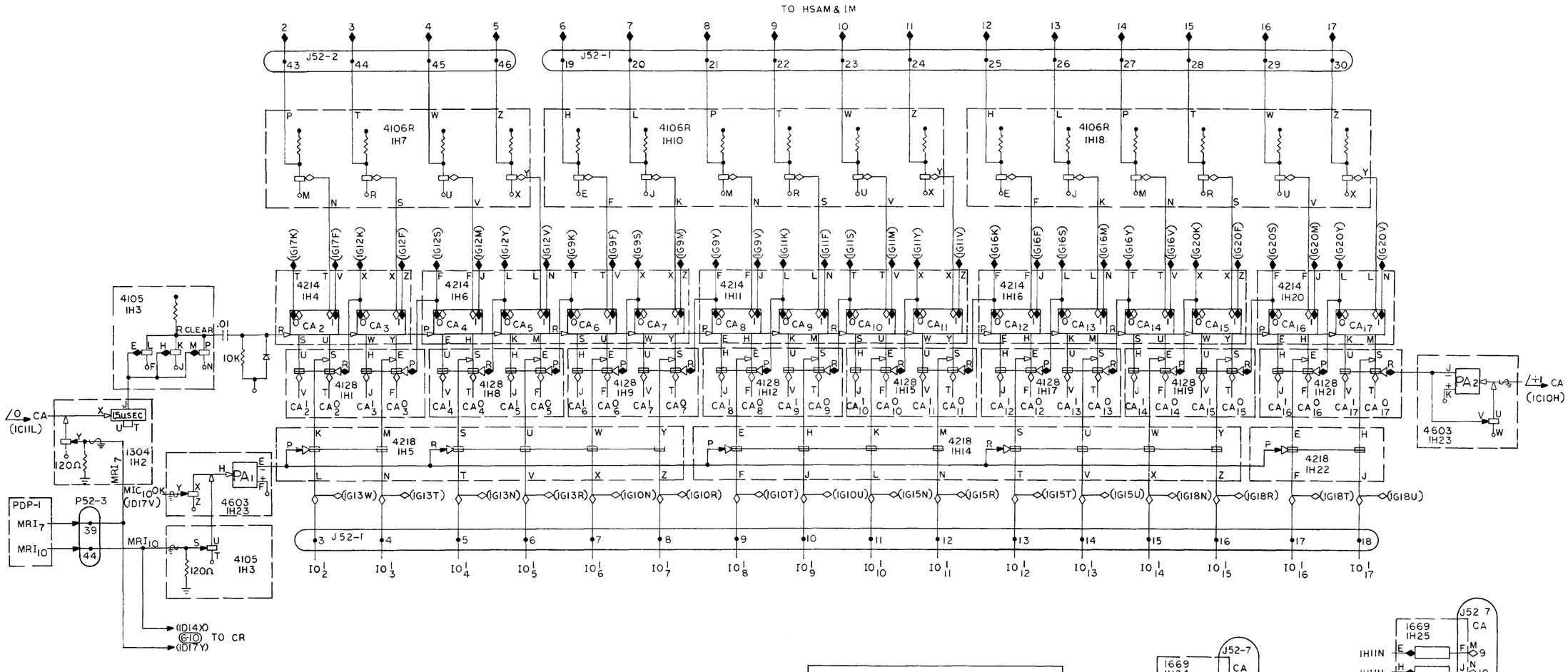
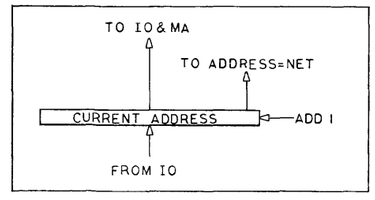


Figure 6-10 Command Register, Command Decoders, Write Buffer





IH

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
4128	1304	4105	4214	4218	4214	4106R	4128	4128	4106R	4214	4128	BLANK	4218	4128	4214	4128	4106R	4128	4214	4128	4218	4603	1669	1669

Figure 6-11 Current Address

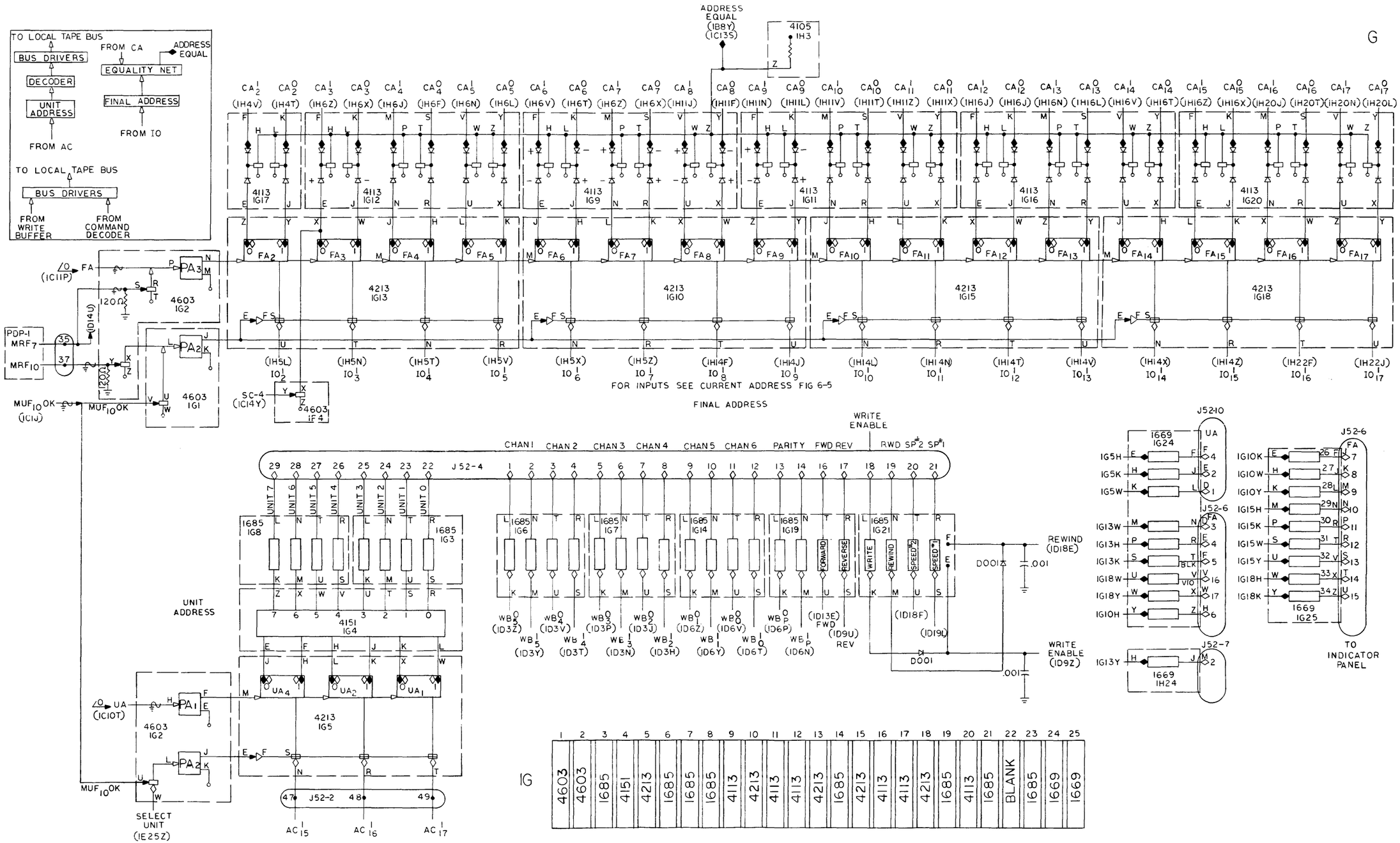


Figure 6-12 Unit, Final Address, Address Equal

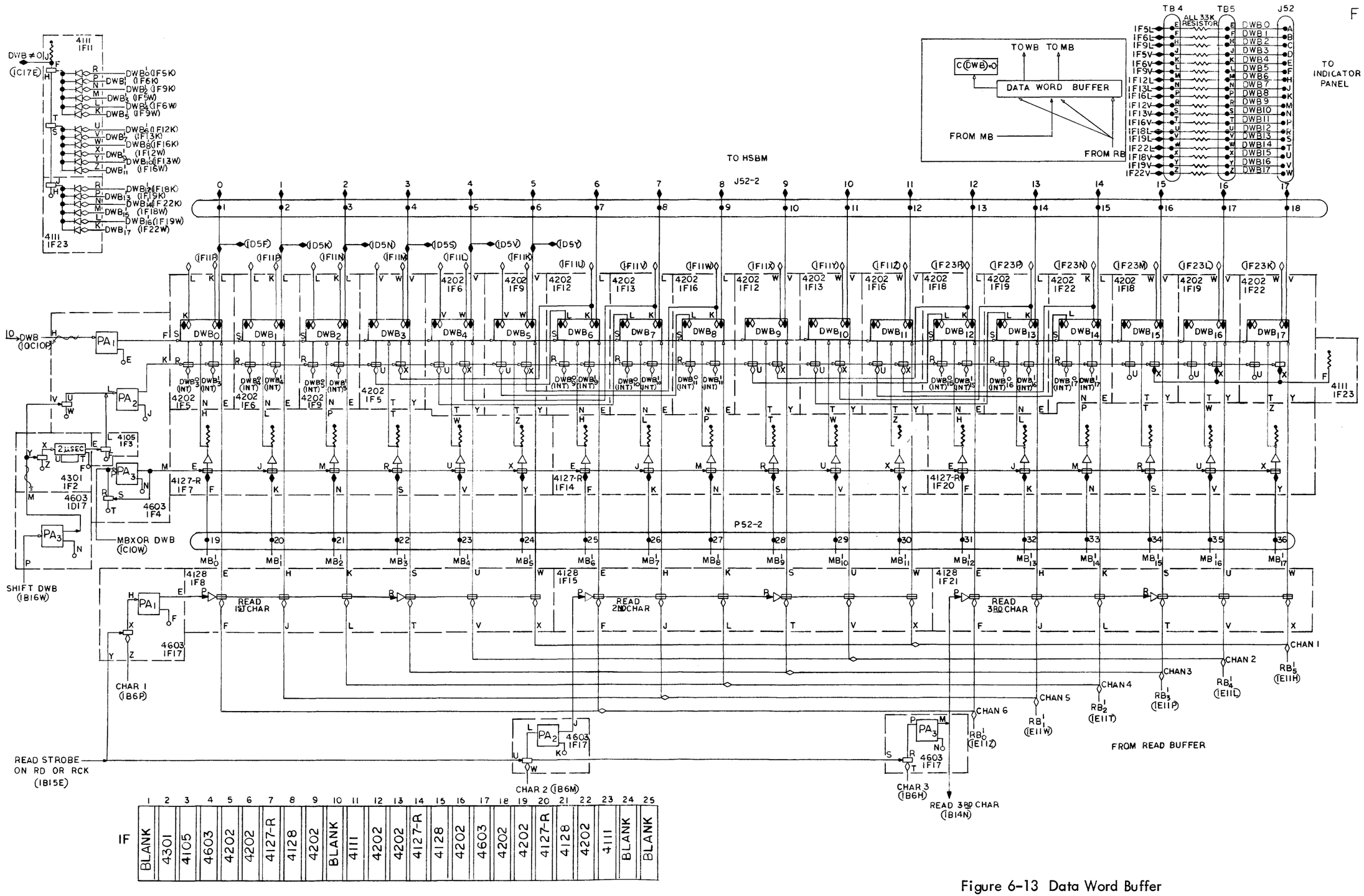
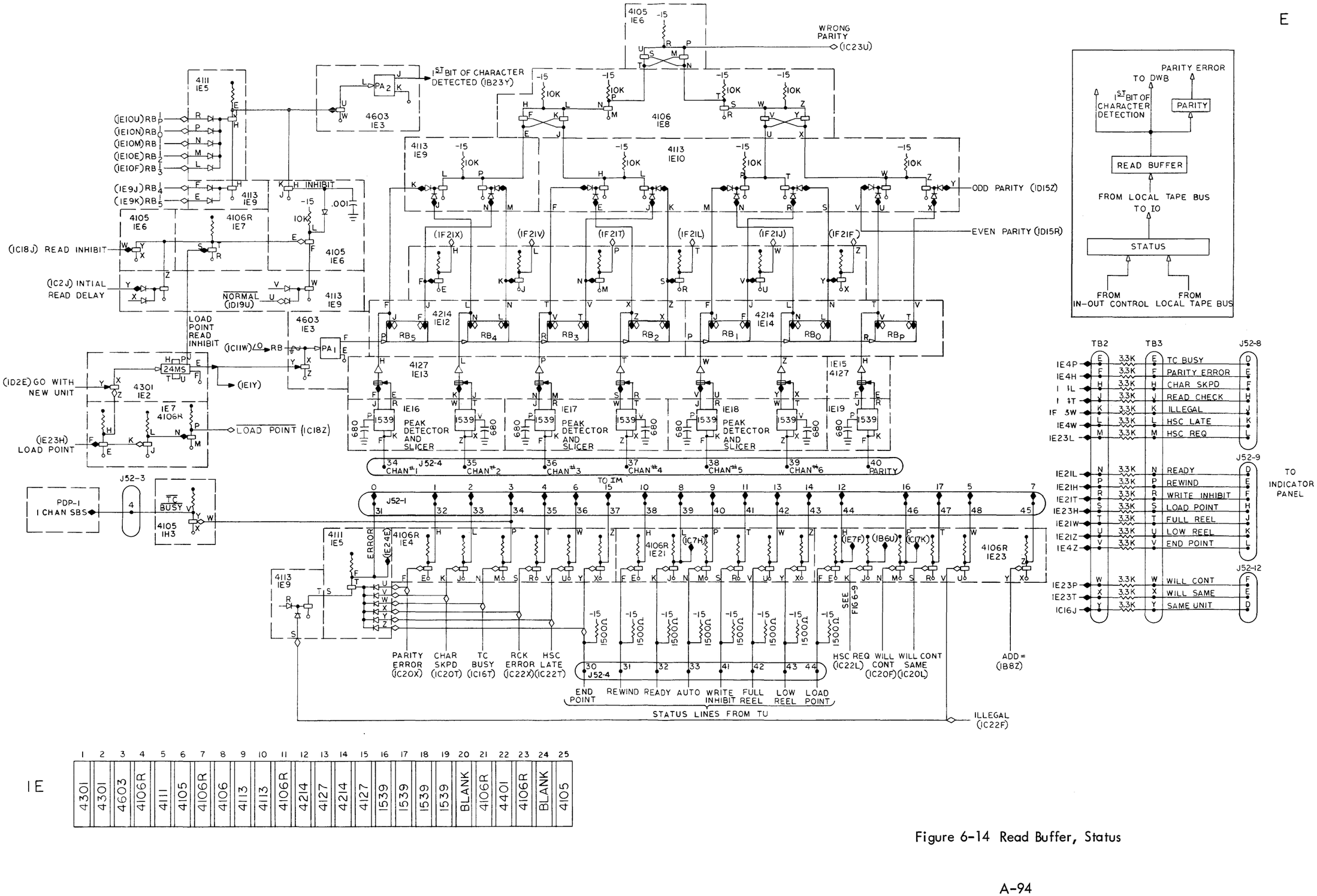


Figure 6-13 Data Word Buffer



IE

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
4301	4301	4603	4106R	4111	4105	4106R	4106	4113	4113	4106R	4214	4127	4214	4127	1539	1539	1539	1539	BLANK	4106R	4401	4106R	BLANK	4105

Figure 6-14 Read Buffer, Status

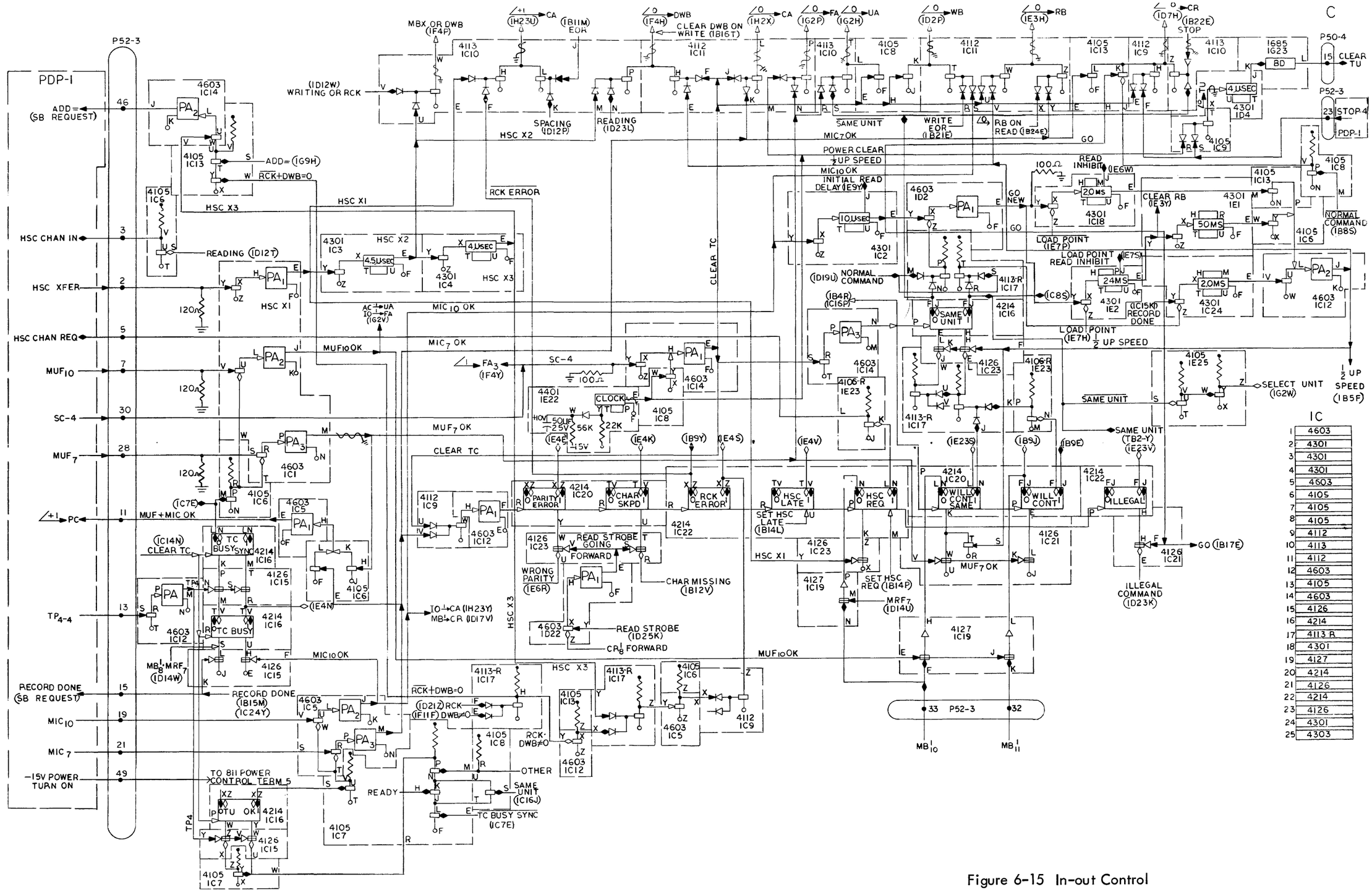


Figure 6-15 In-out Control

B

WRITE (ID2V)

WRITE EOR (ID3W) (IC11R)

1/2 UP TO SPEED + 4.2MS

4603 1B11 PA1

4127 1B16

4124 1B4 WRITE SYNC

(IC14N) CLEAR TC

4126 1B3

4214 1B4 WRITE

4407 1B1 CLOCK

4301 1B2 4.2MS

4113R 1B8

WRITING

4214 1B4

CHARACTER COUNTER

4126 1B5

4105 1B12

1/2 UP SPEED (IC12J)

COUNT

4301 1B20 4 μSEC

PREWRITE

4603 1B11 PA2

4105 1E25

ASK FOR FIRST WORD

STOP WRITING

4126 1B3

4113R 1B6

CLEAR DWB (IC11H)

SHIFT DWB (ID17P)

4127 1B16

4106R 1B8

CHAR 3

PREWRITE

CHAR 1 (IF17Z)

CHAR 2 (IF17W)

CHAR 3 (IF17T)

READ DETECT

RD OR RCK

4113 1B25

STOP WRITING

4127 1B16

4301 1B21 270 μSEC

4112R 1B7

HSC LATE (IE4W)

CHAR3

WRITE LOGIC

4106R 1B8

ADD=

ADD= (IG20Z)

ADD= (IE23Y)

4301 1B24 5 μSEC

4301 1B23 20 μSEC

CLEAR RB ON READ (IC11X)

4603 1B15 PA2

BACK SPACE 4105 1B12

1ST BIT OF CHARACTER DETECTED (IE3J)

4410 1E25

4301 1B18 4.6MS

EOR ON WRITE

4106R 1B8

ADD=

4112R 1B7

CHAR 3

WRITING

4105 1B17

4113 1B25

READING OR RCK

RCK ERROR (IC22X)

CHAR 2

READING OR RCK

CHAR 1 READ DETECT

WRITING (ID23V)

SET HSC REQ. (IC22M)

READ 3rd CHAR (IF17M)

HSC REQUEST LOGIC

WRITE

4126 1B14

AT RECORD GAP

4105 1B17

4603 1B15

SET HSC LATE (IC22U)

PREWRITE

4126 1B14

4113R 1B6

HSC REQ. (IE23L)

READ LOGIC

4603 1B15

READ STROBE ON READING OR RCK (IF17S)

READING OR RCK (ID21L)

4113 1B25

4105 1B12

>1 1/2 CHAR

4303 1B13 100 μSEC

4303 1D25 230 μSEC

4303 1C25 480 μSEC

READ STROBE (ID22Y)

>3 1/2 CHAR

<3 1/2 CHAR

>7 CHAR

>7 CHAR

< 3 1/2 CHAR

4112R 1B7

FORWARD SPACING (ID21R)

BACKWARD SPACING

BACKSPACING (ID12N)

WILL CONTINUE (IC20F)

CHAR MISSING IC23R

WILL CONTINUE (IC20J)

4603 1D22 PA2

EOR ON WRITE

EOR (IC10J)

4603 1B11 PA2

EOR ON RD RCK OR SPACING

4112R 1B7

.001

.001

ADD=

4113 1B9

4603 1B15

RECORD DONE (IC15K)

4301 1B19 10 MS

GO (IC21F)

4106R 1B8

NORMAL COMMAND (ID23H) (IC8M)

READ HEAD IN RIGHT SPOT

4105 1B17

4113 1B9

4105 1B17

STOP (IC10X)

4301 1B22 700 μS

4105 1B17

4301 1B10 4 MS

TERMINATING LOGIC

1B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
4407	4301	4126	4214	4126	4113R	4112R	4106R	4113	4301	4603	4105	4303	4126	4603	4127	4105	4301	4301	4301	4301	4301	4301	4301	4113

Figure 6-16 Format Control

Figure 6-17 Programmed Tape Control Type 51

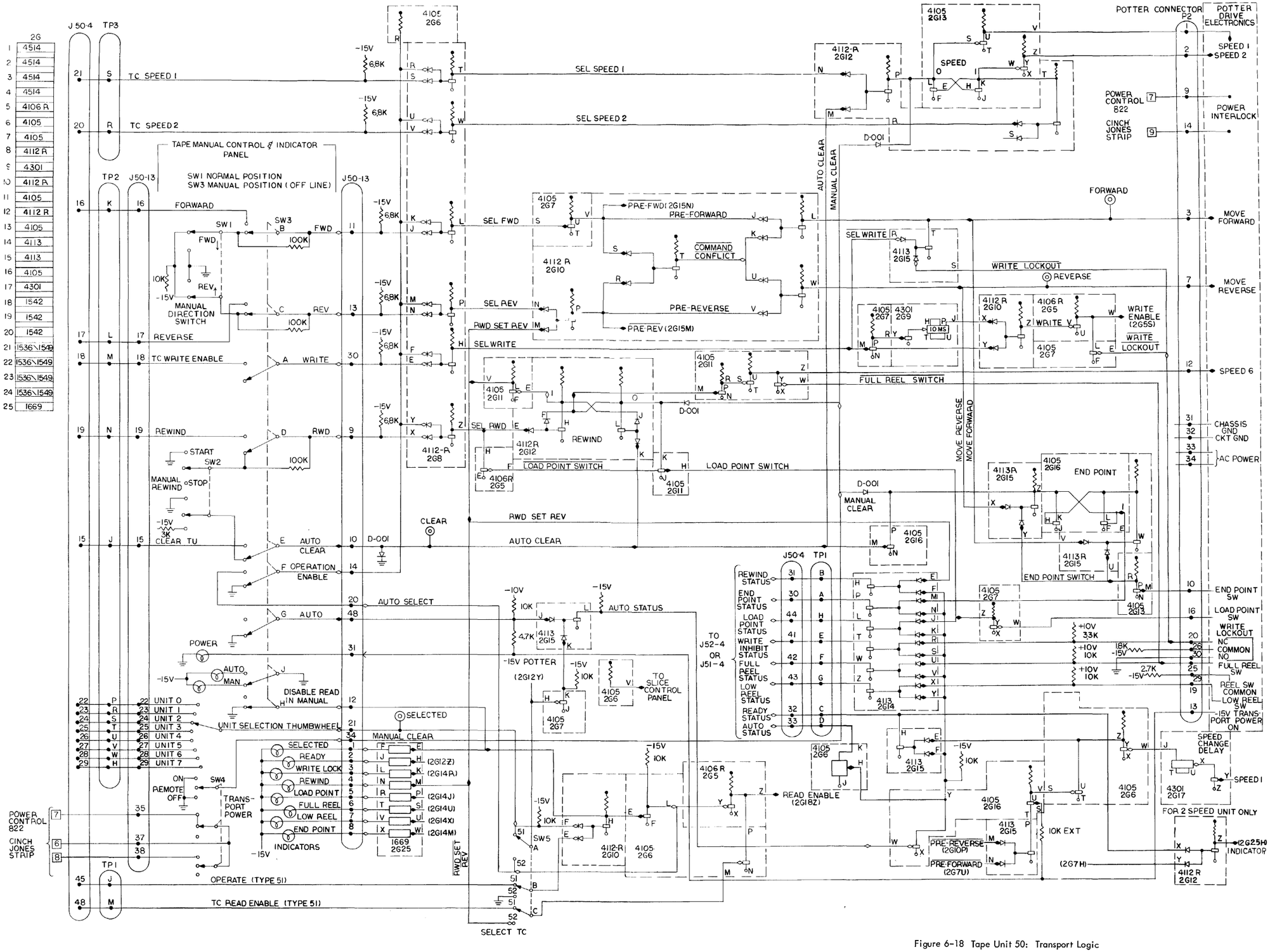


Figure 6-18 Tape Unit 50: Transport Logic

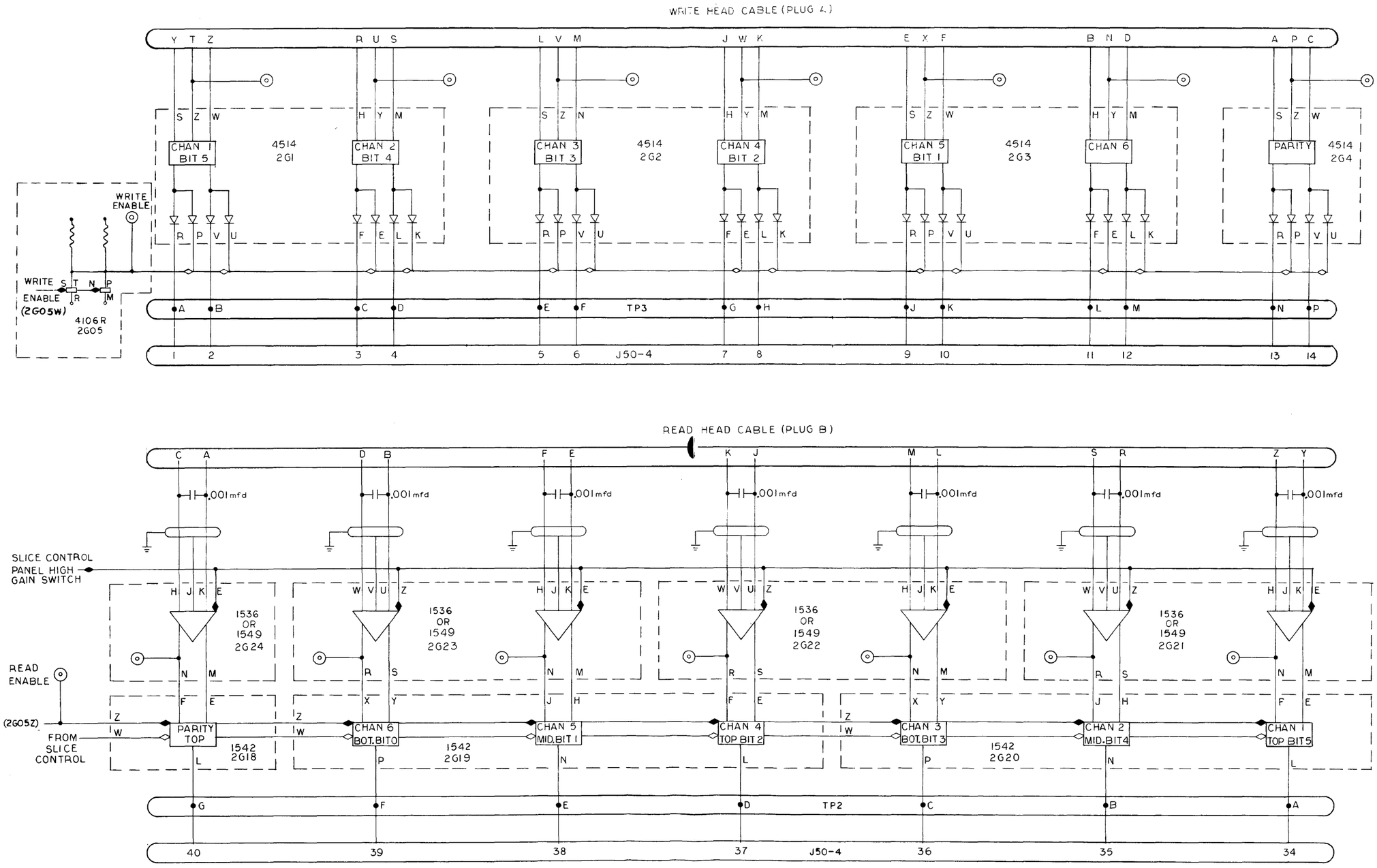


Figure 6-19 Tape Unit 50: Read-Write Circuits

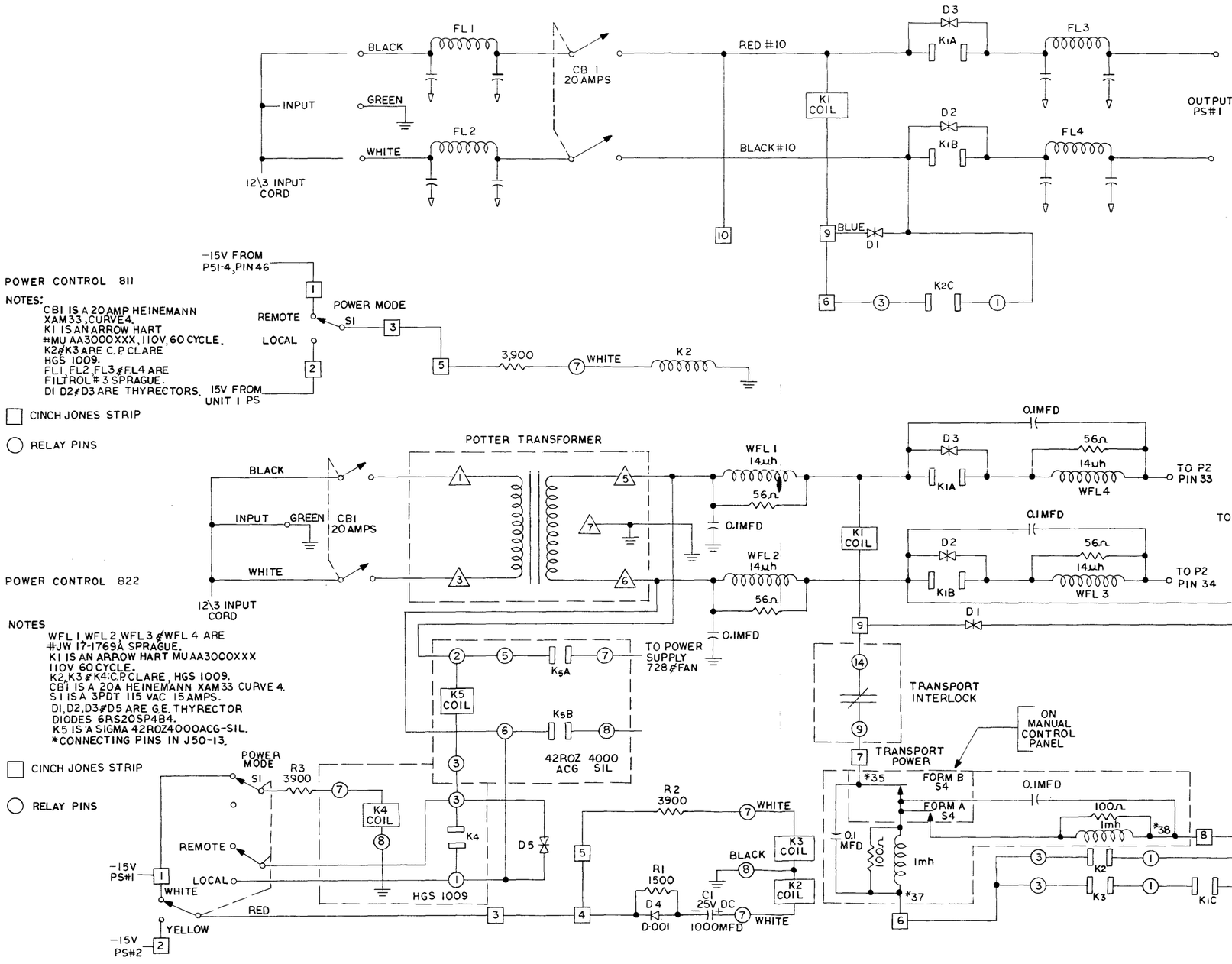
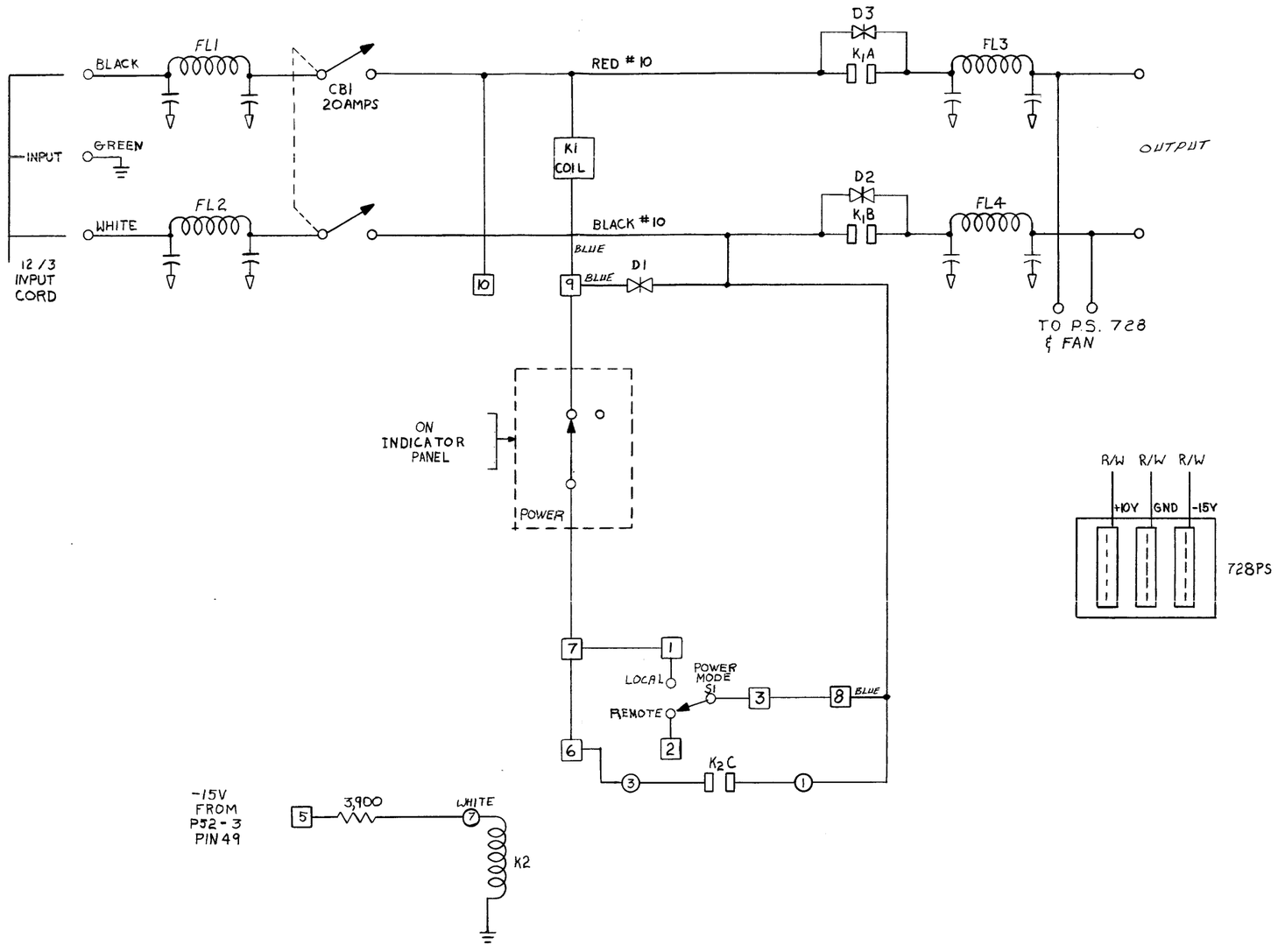


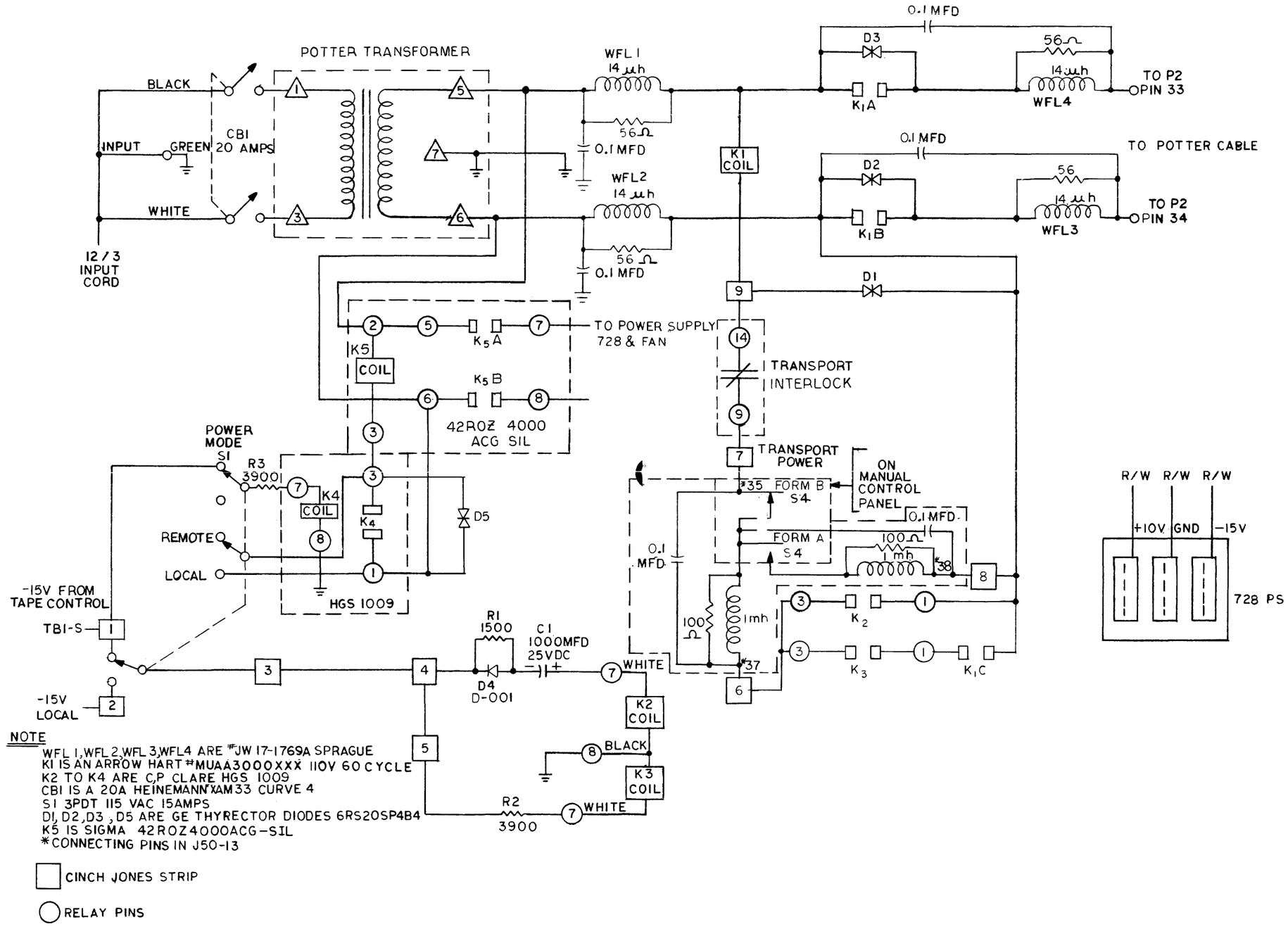
Figure 7-1 Power Control Wiring for Types 50 and 51 Combination



NOTE:
K1 IS AN ARROW HART* MUAA3000XXX, 110V 60 CYCLE
K2 K3 C.P. CLARE HGS 1009
FL1, FL2 FL3, FL4 ARE FILTROL #3 SPRAGUE
D1, D2, D3 THYRECTORS

□ CINCH JONES STRIP
○ RELAY PINS

Figure 7-2 Power Control Wiring for Tape Control 52



NOTE

WFL 1, WFL 2, WFL 3, WFL4 ARE #JW 17-1769A SPRAGUE
K1 IS AN ARROW HART #MUAA3000XXX 110V 60 CYCLE
K2 TO K4 ARE C,P CLARE HGS 1009
CB1 IS A 20A HEINEMANN #AM33 CURVE 4
S1 3PDT 115 VAC 15AMPS
D1, D2, D3, D5 ARE GE THYRECTOR DIODES 6RS20SP4B4
K5 IS SIGMA 42ROZ4000ACG-SIL
*CONNECTING PINS IN J50-13

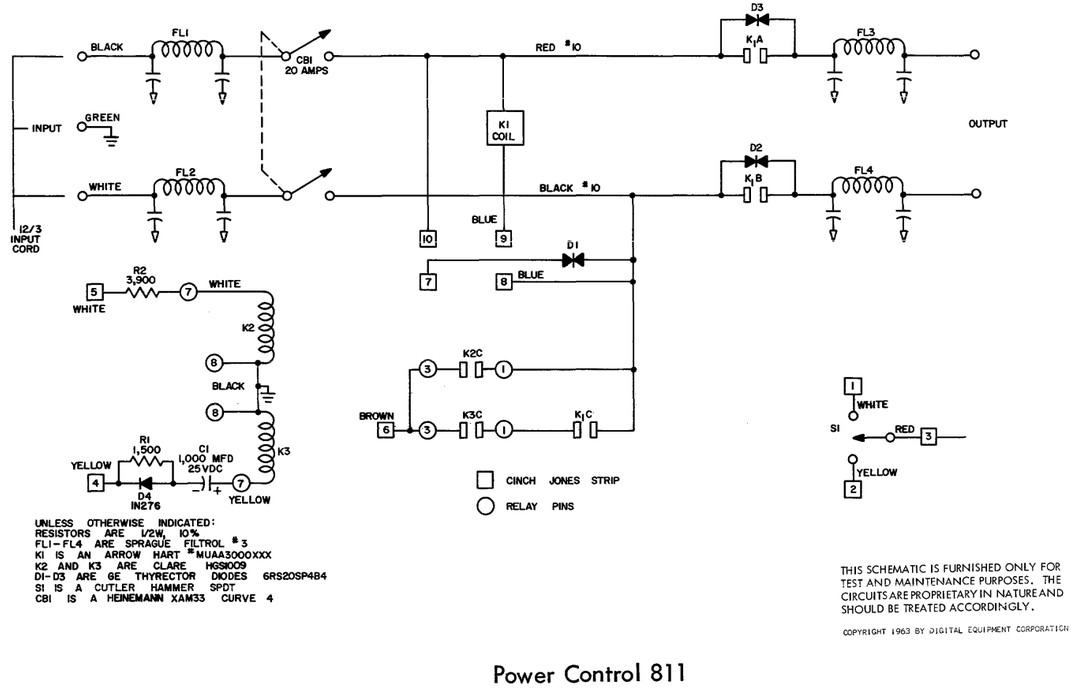
CINCH JONES STRIP

RELAY PINS

Figure 7-3 Power Control Wiring for Tape Unit 50

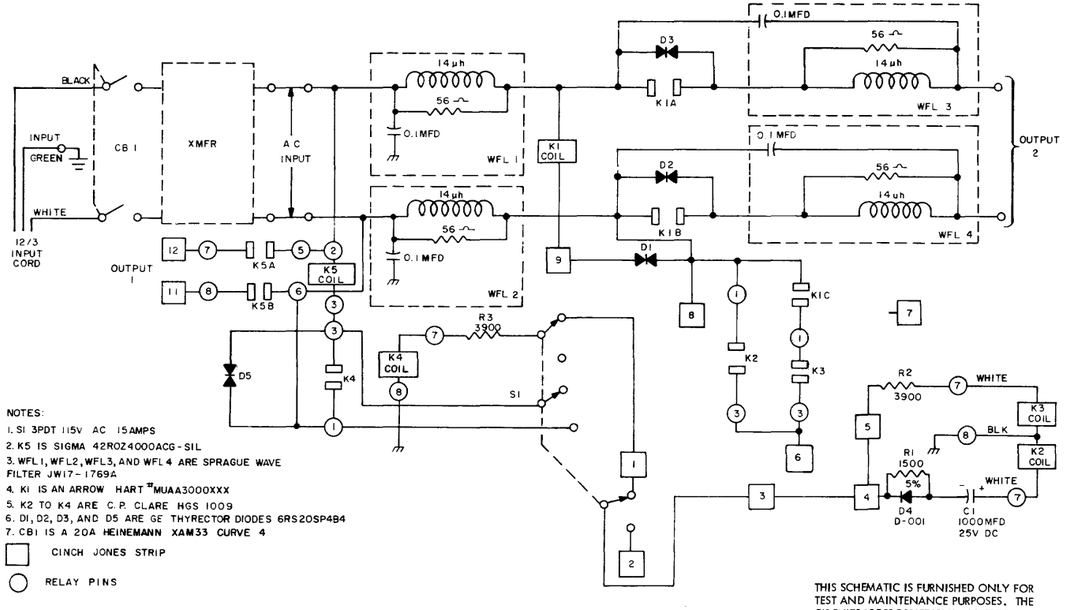
Power Control 811

Power Control 822



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
FL1 - FL4 ARE SPRAGUE FILTROL #3
K1 IS AN ARROW HART #MUAA3000XXX
K2 AND K3 ARE CLARE HGS1009
D1-D3 ARE GE THYRECTOR DIODES 6RS20SP4B4
S1 IS A CUTLER HAMMER SPDT
CB1 IS A HEINEMANN XAM33 CURVE 4

Power Control 811

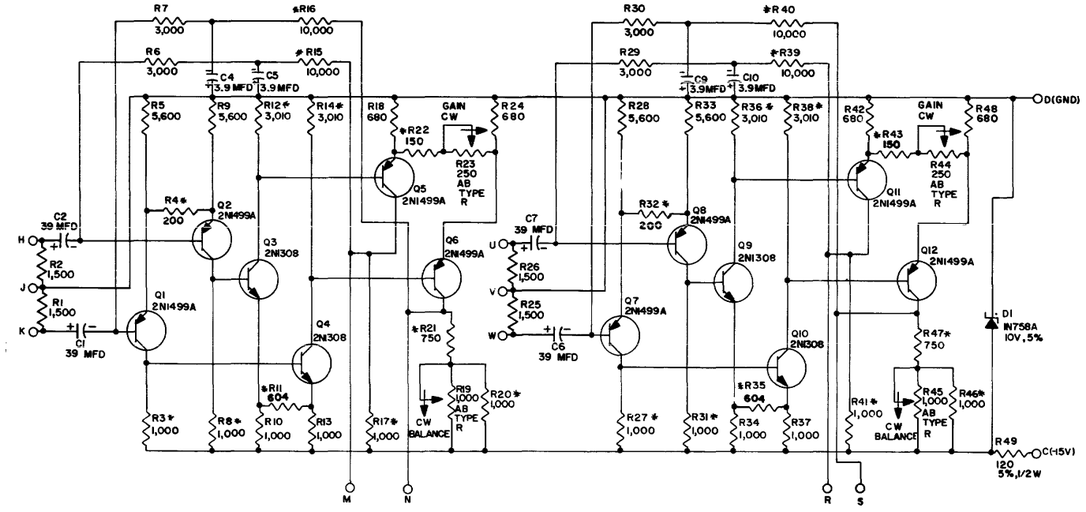


NOTES:
1. S1 3PDT 115V AC 15AMPS
2. K5 IS SIGMA 42ROZ4000ACG-SIL
3. WFL1, WFL2, WFL3, AND WFL4 ARE SPRAGUE WAVE FILTER JW17-1769A
4. K1 IS AN ARROW HART #MUAA3000XXX
5. K2 TO K4 ARE C.P. CLARE HGS 1009
6. D1, D2, D3, AND D5 ARE GE THYRECTOR DIODES 6RS20SP4B4
7. CB1 IS A 20A HEINEMANN XAM33 CURVE 4

CINCH JONES STRIP
RELAY PINS

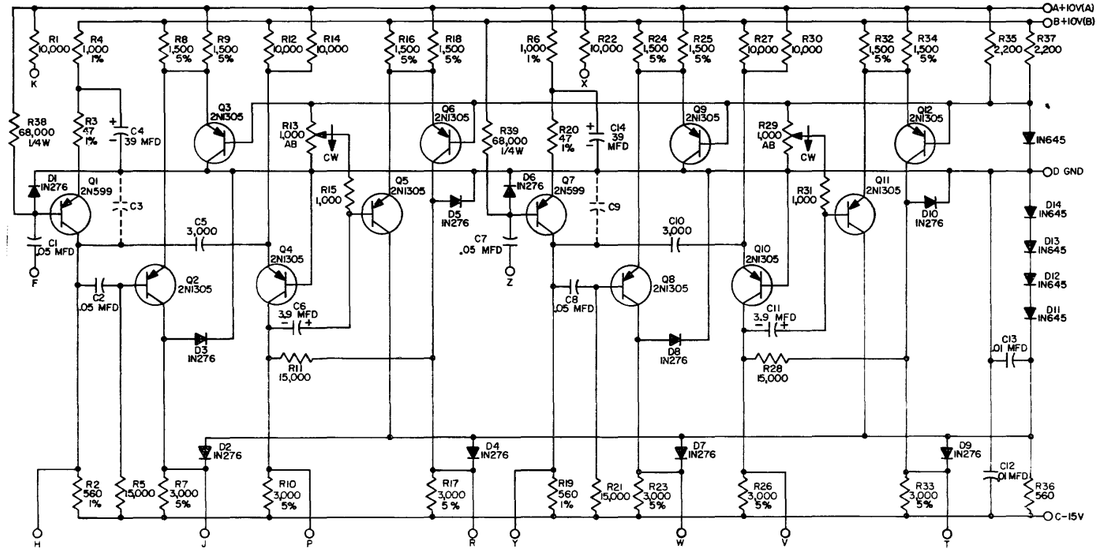
Power Control 822

Differential Amplifier 1536
Peak Detector and Slicer 1539



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD
*DC 1/2 ARN 20X (ELECTRA) 1% RESISTORS

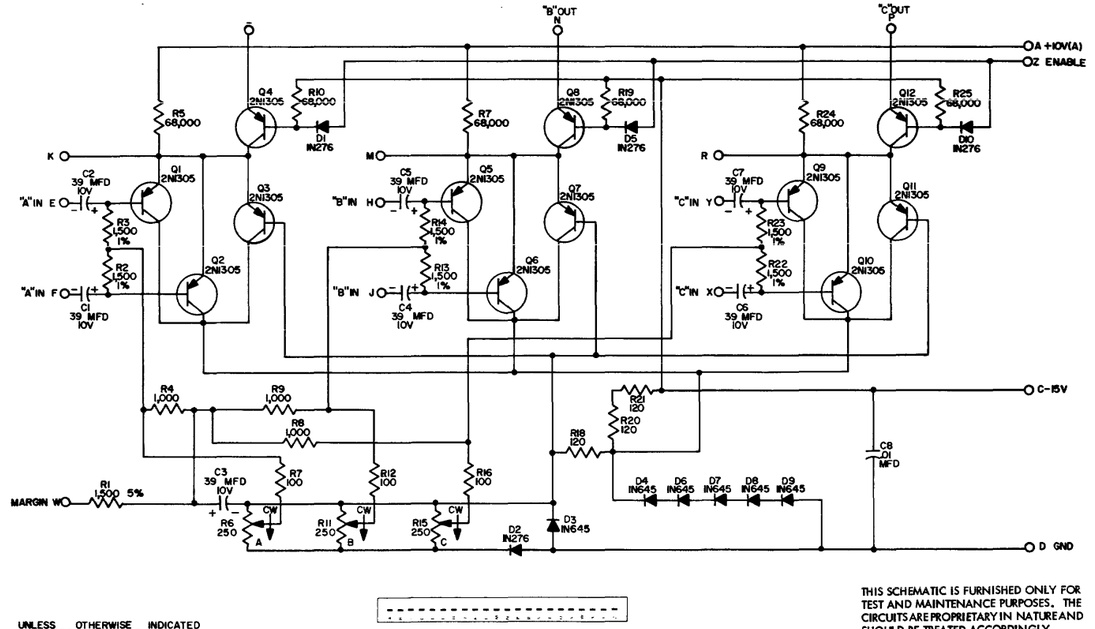
Differential Amplifier 1536



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD.

Peak Detector and Slicer 1539

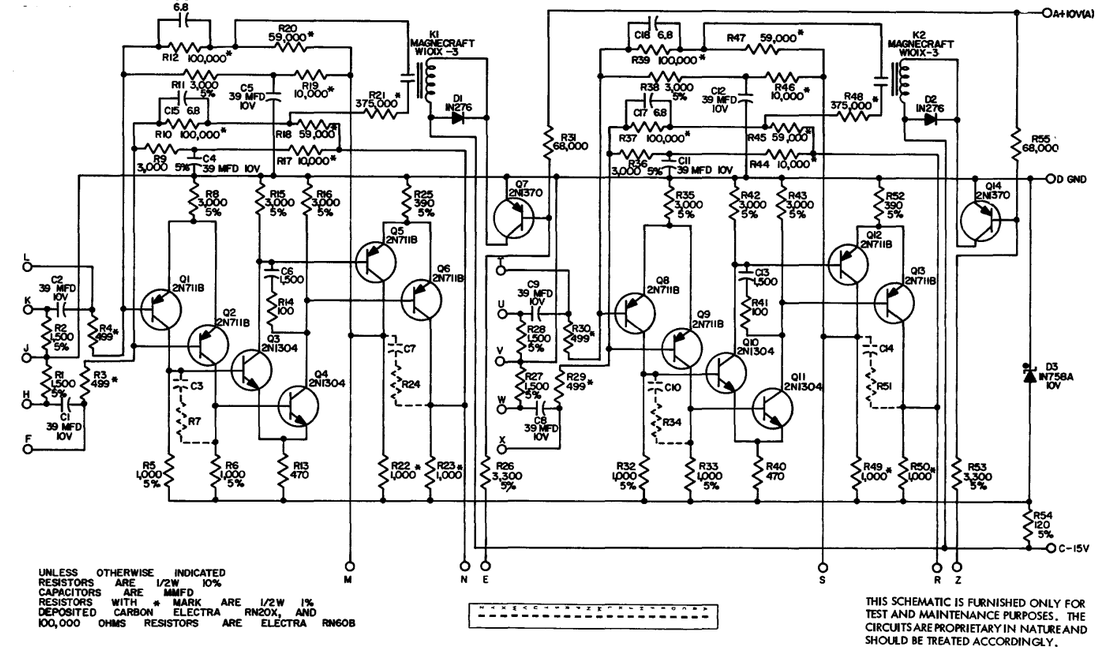
Rectifying Slicer 1542
Differential Amplifier 1549



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD.

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

Differential Amplifier 1549



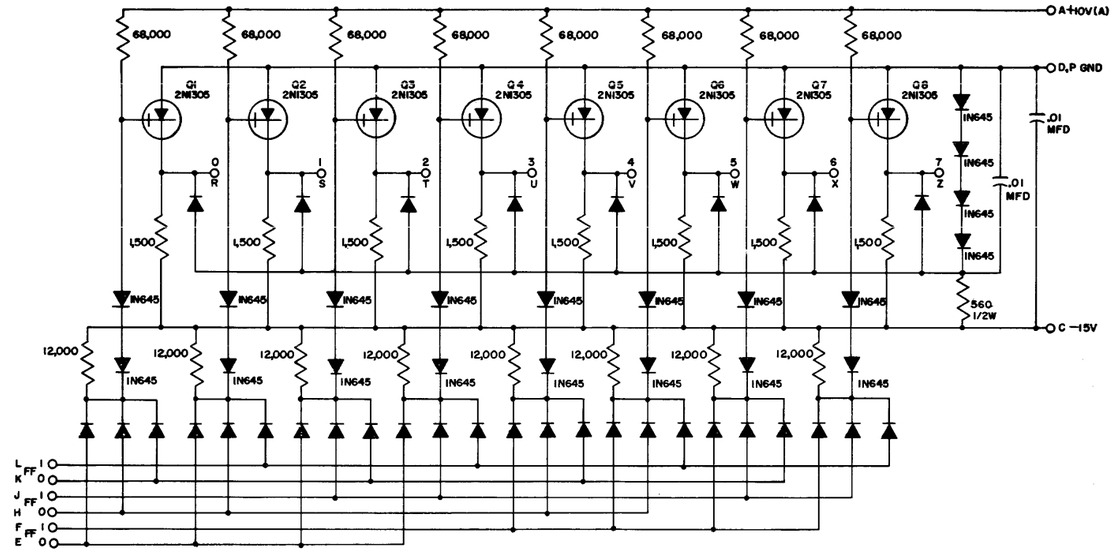
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2W 10%
CAPACITORS ARE MMFD
RESISTORS WITH * MARK ARE 1/2W 1%
DEPOSITED CARBON ELECTRA RN20X, AND
100,000 OHMS RESISTORS ARE ELECTRA RN60B

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

Rectifying Slicer 1542

Binary-to-Octal Decoder 4151

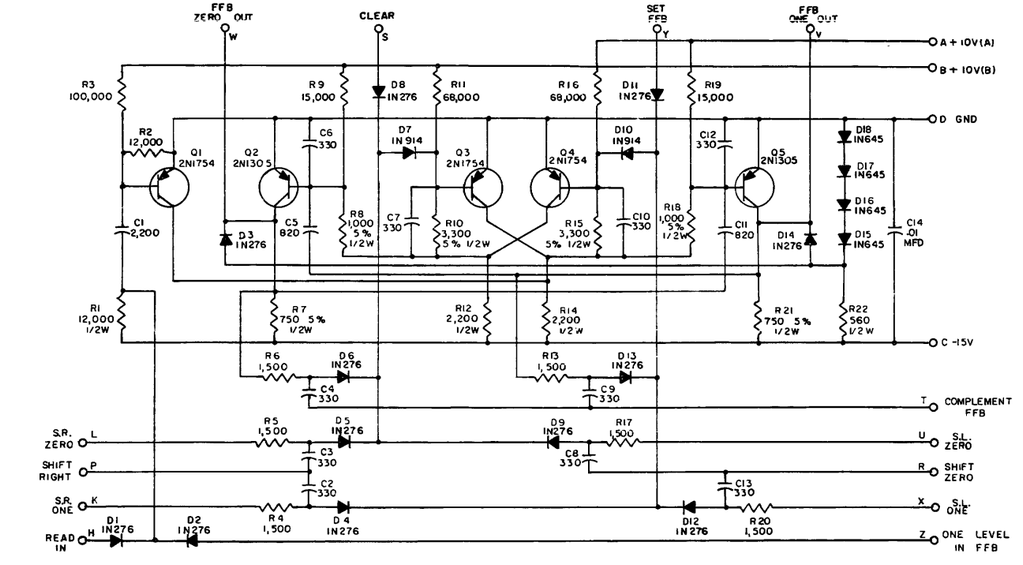
Dual Flip-Flop 4202



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
DIODES ARE IN276

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

Binary-to-Octal Decoder 4151



UNLESS OTHERWISE INDICATED,
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD.

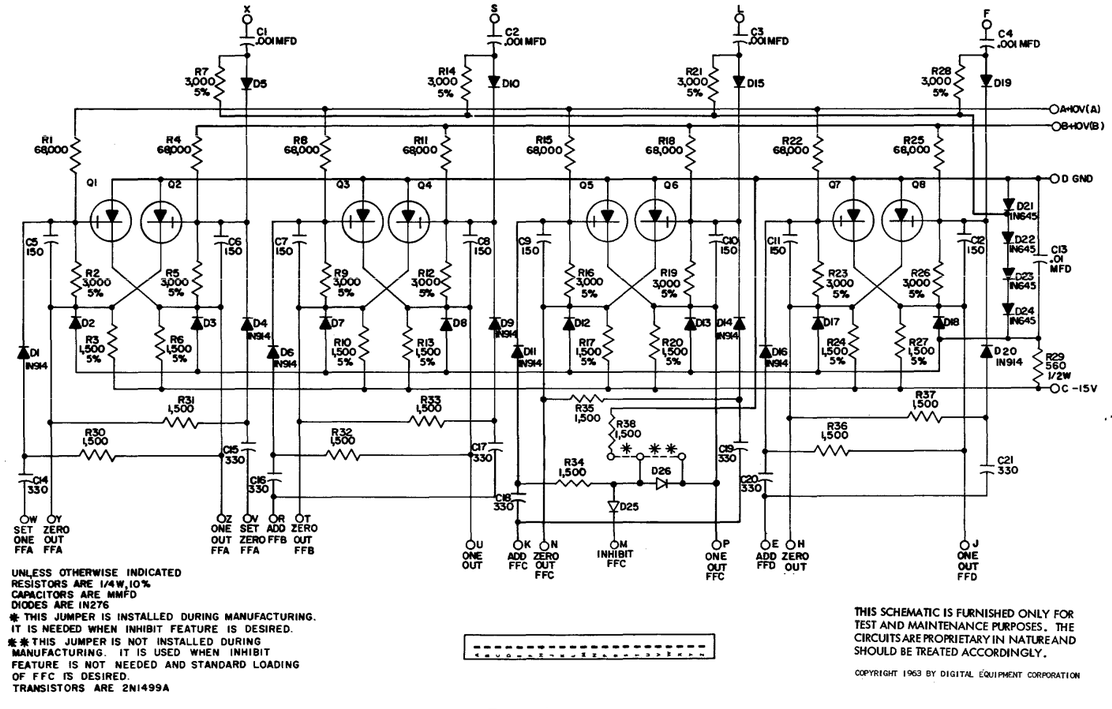
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

Dual Flip-Flop 4202

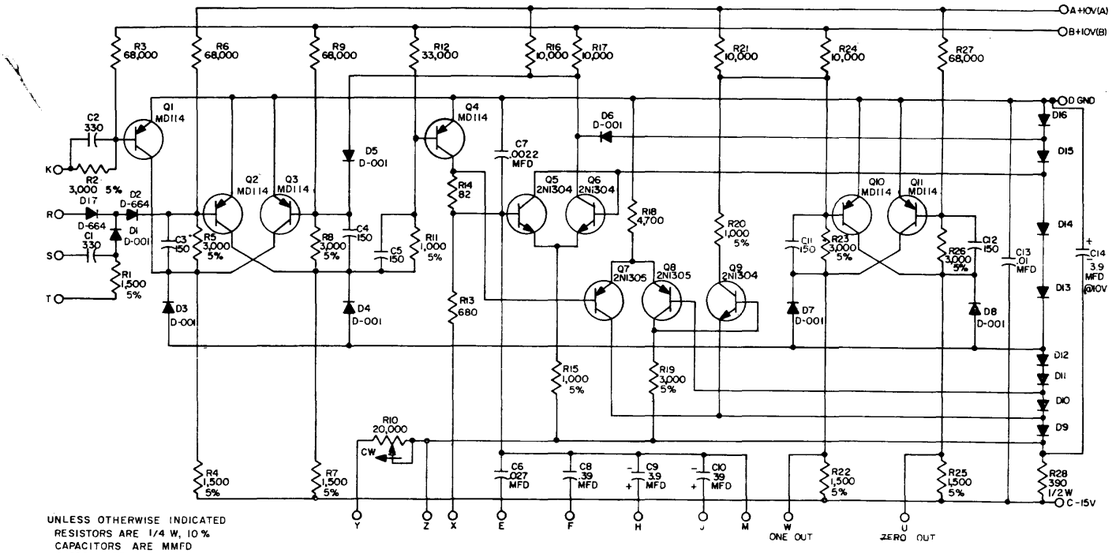
Four-bit Counter 4215

Integrating Delay 4303

A-140



Four-bit Counter 4215



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N1499A	D-664	IN914
2N1304	2N1304		
2N1305	2N1305		
D-001	IN276		
D-662	IN645		

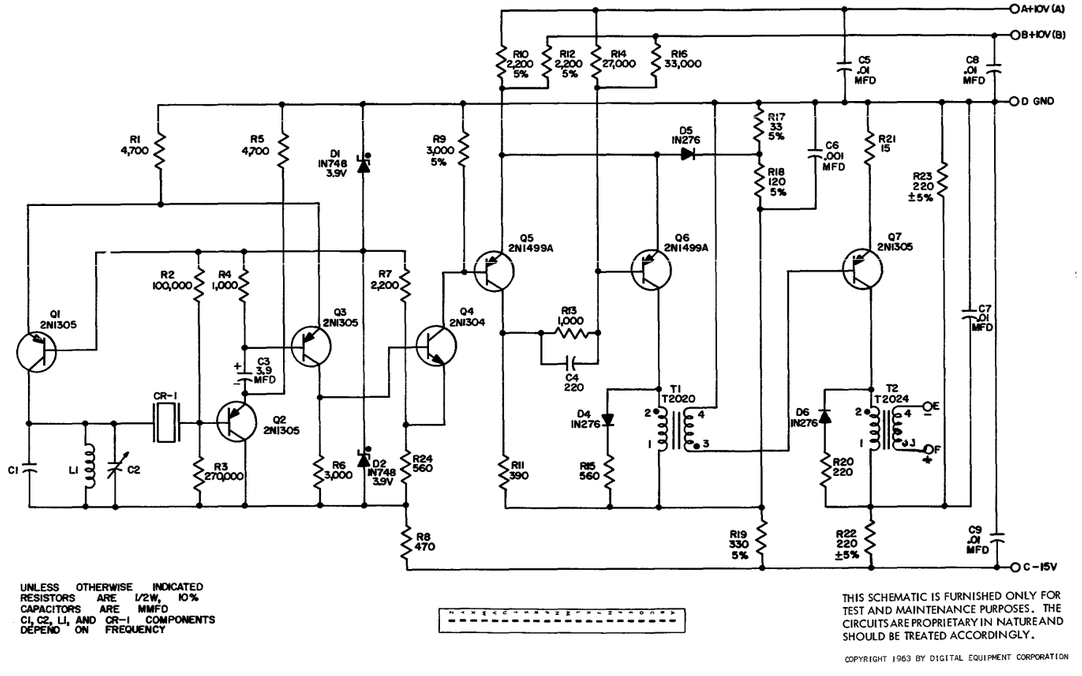
NOTES

H	RS-4303-9
INTEGRATING ONE-SHOT 4303	

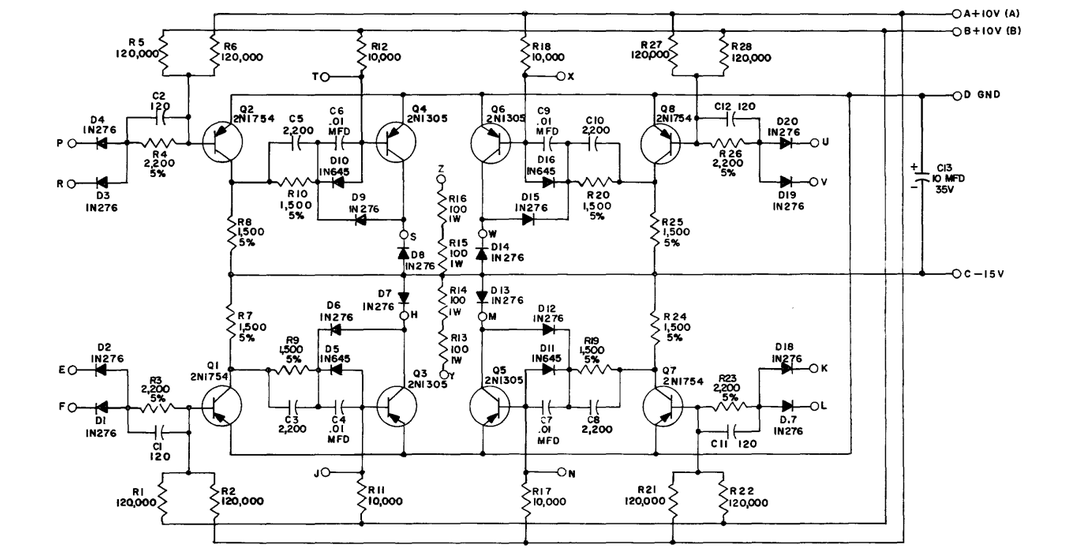
Integrating Delay 4303

Crystal Clock 4407

NRZ Writer 4514



Crystal Clock 4407



NRZ Writer 4514

Figure 8-1

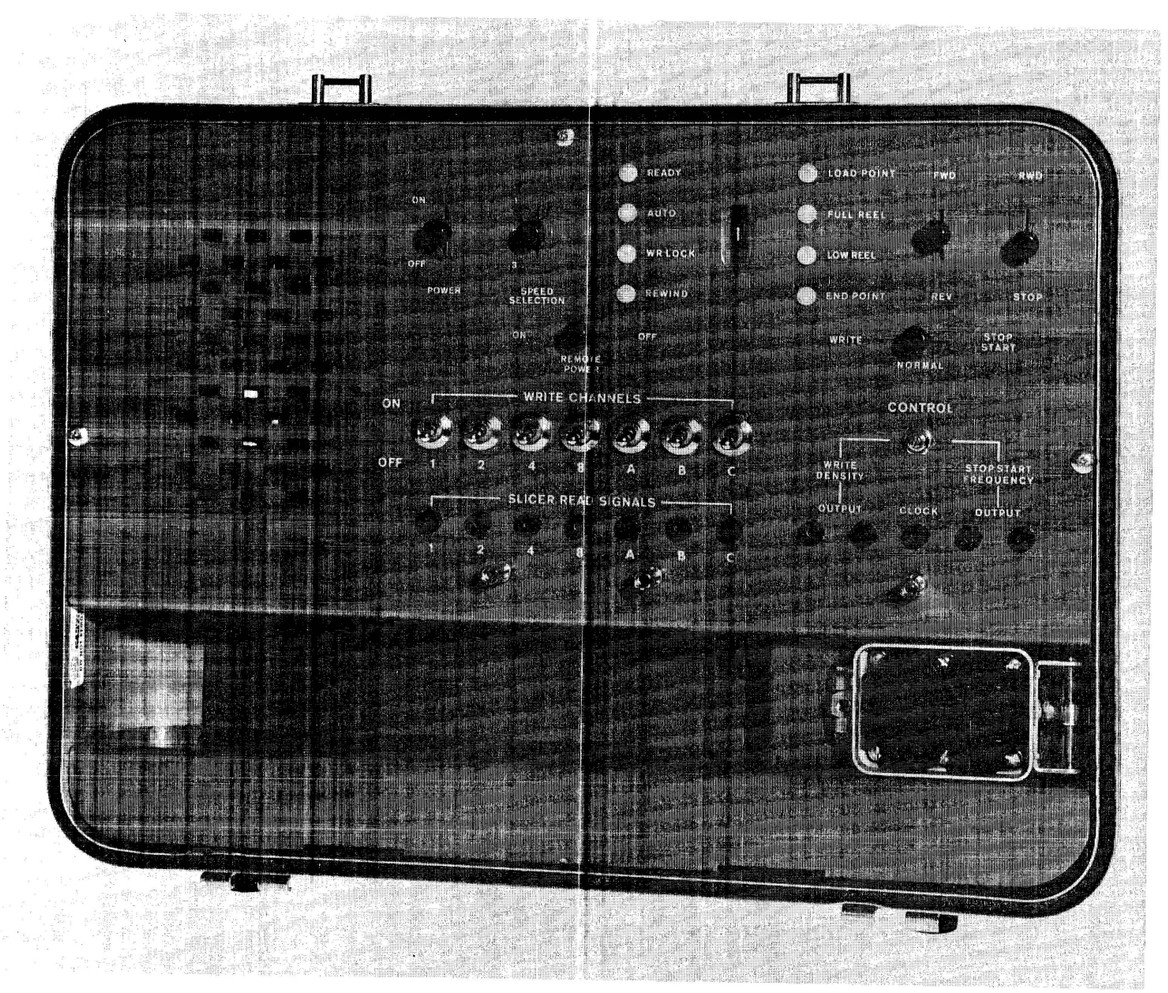


Figure 8-1 Magnetic Tape Unit Calibrator

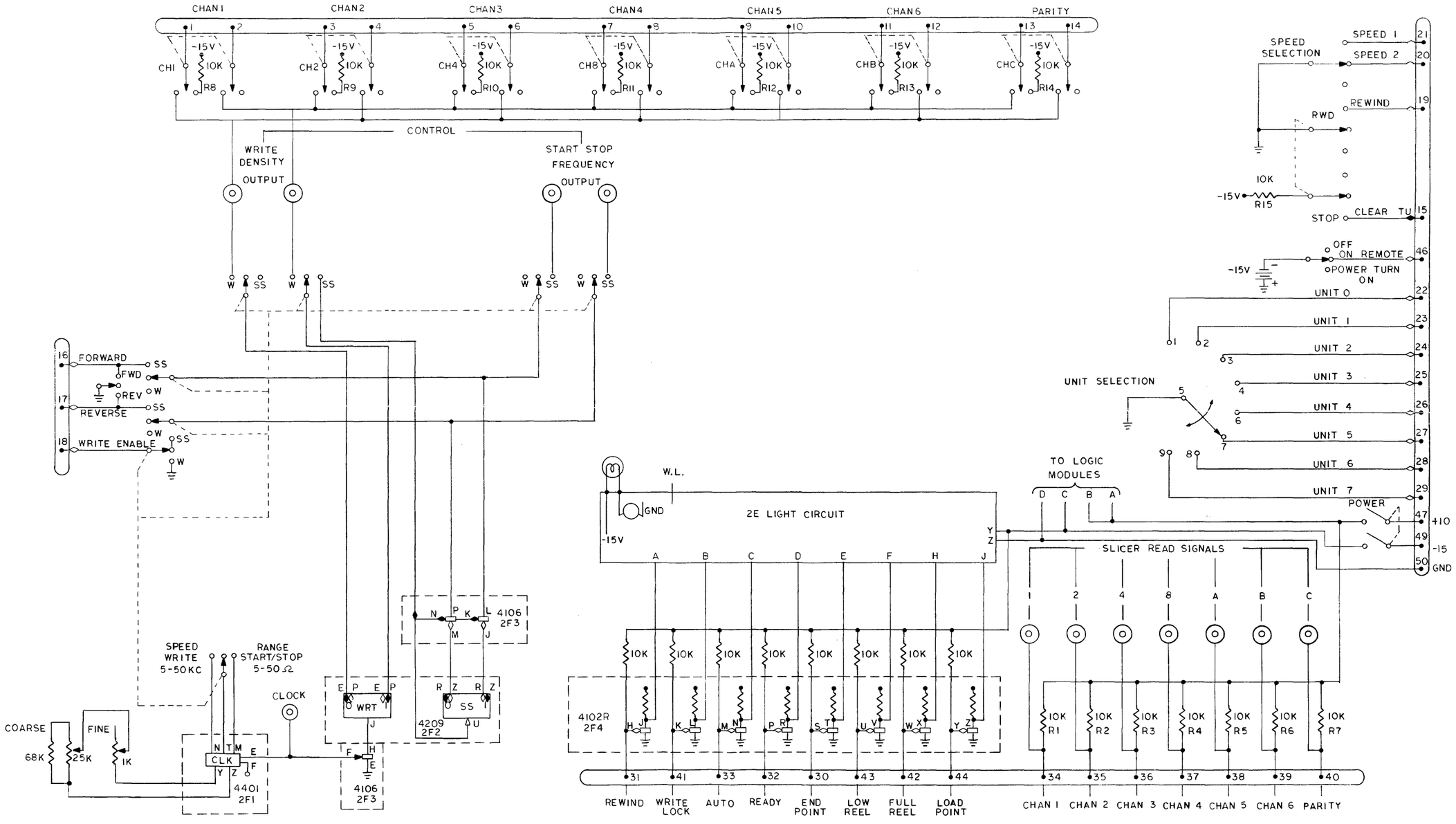


Figure 8-2 Unit Calibrator Logic

Figure 8-3

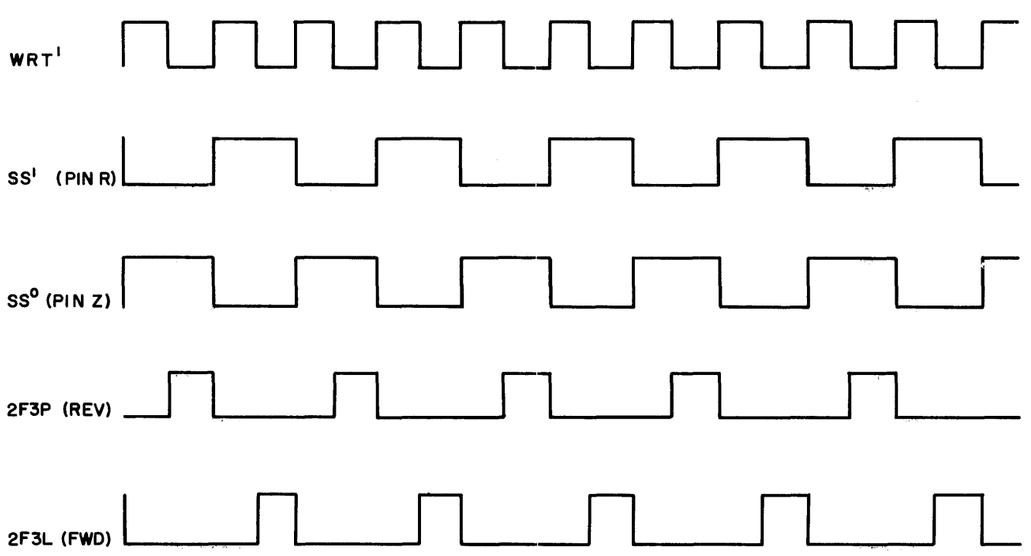


Figure 8-3 Calibrator Timing Chart

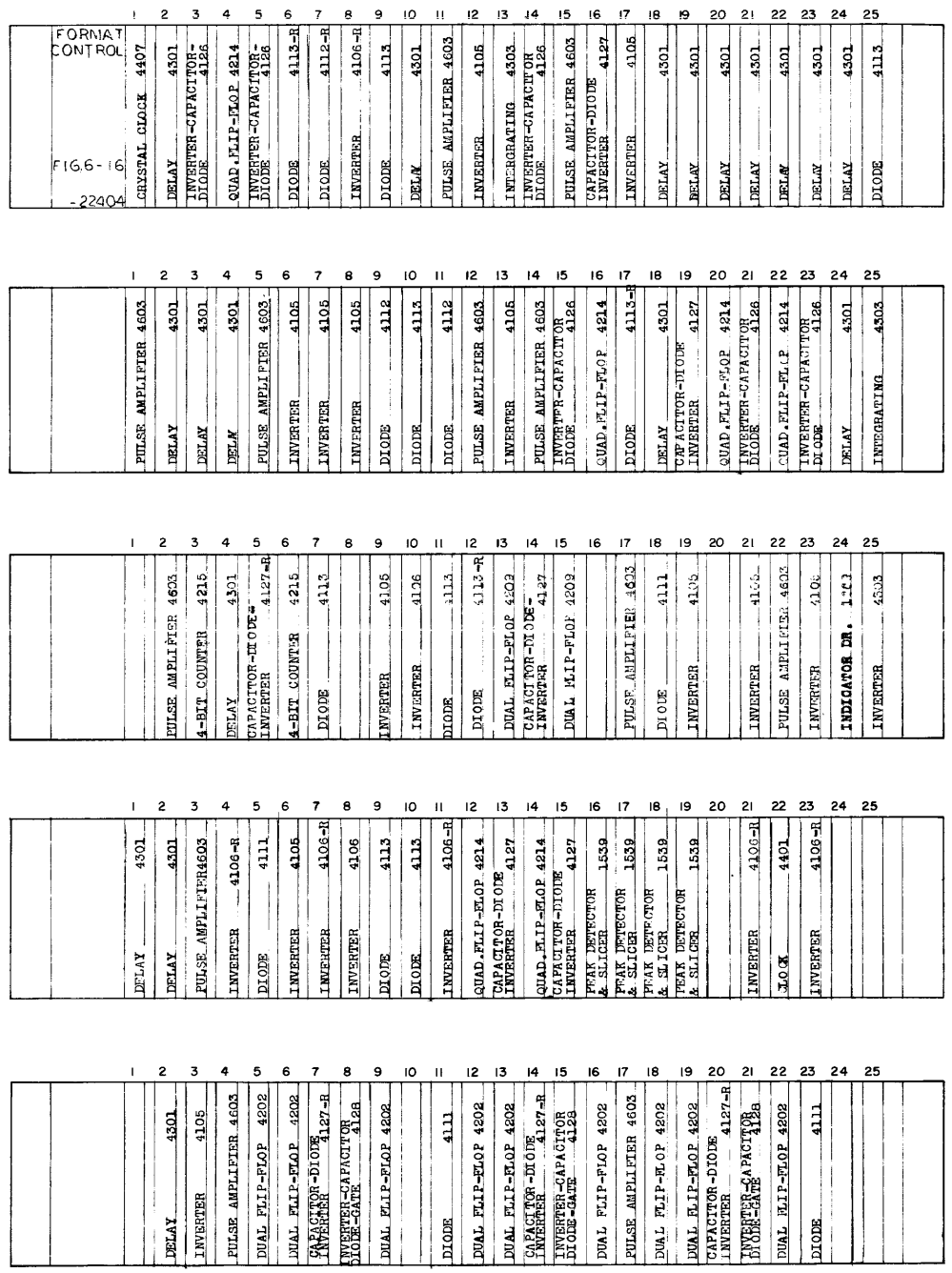


Figure 8-4 Tape System Module Layout, Types 50, 51 and 52

TAPER PIN BLOCK #3

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V	W
1	YELLOW 2G1R ○ WB 0 BIT 5	BLUE 2G1V ○ WB 0 BIT 5	YELLOW 2G1F ○ WB 0 BIT 4	BLUE 2G1L ○ WB 1 BIT 4	YELLOW 2G2R ○ WB 2 BIT 3	BLUE 2G2V ○ WB 2 BIT 3	YELLOW 2G2F ○ WB 3 BIT 2	BLUE 2G2L ○ WB 3 BIT 2	YELLOW 2G3R ○ WB 4 BIT 1	BLUE 2G3V ○ WB 4 BIT 1	YELLOW 2G3F ○ WB 5 BIT 0	BLUE 2G3L ○ WB 5 BIT 0	YELLOW 2G4R ○ WB 6 PARITY	BLUE 2G4V ○ WB 6 PARITY	WHITE 2G8V ○ SPEED 2	WHITE 2G8S ○ SPEED 1	BLACK 26 GND ○ GND	○	○	○
2	J50-4A PIN 1 ○ WB 0 BIT 5	J50-4A PIN 2 ○ WB 0 BIT 5	J50-4A PIN 3 ○ WB 0 BIT 4	J50-4A PIN 4 ○ WB 1 BIT 4	J50-4A PIN 5 ○ WB 2 BIT 3	J50-4A PIN 6 ○ WB 2 BIT 3	J50-4A PIN 7 ○ WB 3 BIT 2	J50-4A PIN 8 ○ WB 3 BIT 2	J50-4A PIN 9 ○ WB 4 BIT 1	J50-4A PIN 10 ○ WB 4 BIT 1	J50-4A PIN 11 ○ WB 5 BIT 0	J50-4A PIN 12 ○ WB 5 BIT 0	J50-4A PIN 13 ○ WB 6 PARITY	J50-4A PIN 14 ○ WB 6 PARITY	J50-4A PIN 20 ○ SPEED 2	J50-4A PIN 21 ○ SPEED 1	J50-4A PIN 50 ○ GND	○	○	○
3	J50-4B PIN 1 ○ WB 0 BIT 5	J50-4B PIN 2 ○ WB 0 BIT 5	J50-4B PIN 3 ○ WB 0 BIT 4	J50-4B PIN 4 ○ WB 1 BIT 4	J50-4B PIN 5 ○ WB 2 BIT 3	J50-4B PIN 6 ○ WB 2 BIT 3	J50-4B PIN 7 ○ WB 3 BIT 2	J50-4B PIN 8 ○ WB 3 BIT 2	J50-4B PIN 9 ○ WB 3 BIT 2	J50-4B PIN 10 ○ WB 4 BIT 1	J50-4B PIN 11 ○ WB 5 BIT 0	J50-4B PIN 12 ○ WB 5 BIT 0	J50-4B PIN 13 ○ WB 6 PARITY	J50-4B PIN 14 ○ WB 6 PARITY	J50-4B PIN 20 ○ SPEED 2	J50-4B PIN 21 ○ SPEED 1	J50-4B PIN 50 ○ GND	○	○	○

TAPER PIN BLOCK #2

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V	W
1	GRY 2G20L ○ READ CH1 BIT 5	GRY 2G20N ○ READ CH2 BIT 4	GRY 2G20P ○ READ CH3 BIT 3	GRY 2G19L ○ READ CH4 BIT 2	GRY 2G19N ○ READ CH5 BIT 1	GRY 2G19P ○ READ CH6 BIT 0	GRY 2G18L ○ PARITY	WHITE J50-13 ○ PIN 29 UNIT 7	GRY J50-13 ○ PIN 15 CLEAR	WHITE J50-13 ○ PIN 16 FWD	WHITE J50-13 ○ PIN 17 REV	WHITE J50-13 ○ PIN 18 WR ENABLE	WHITE J50-13 ○ PIN 19 REWIND	WHITE J50-13 ○ PIN 22 UNIT 0	WHITE J50-13 ○ PIN 23 UNIT 1	WHITE J50-13 ○ PIN 24 UNIT 2	WHITE J50-13 ○ PIN 25 UNIT 3	WHITE J50-13 ○ PIN 26 UNIT 4	WHITE J50-13 ○ PIN 27 UNIT 5	WHITE J50-13 ○ PIN 28 UNIT 6
2	J50-4A PIN 34 ○ READ CH1 BIT 5	J50-4A PIN 35 ○ READ CH2 BIT 4	J50-4A PIN 36 ○ READ CH3 BIT 3	J50-4A PIN 37 ○ READ CH4 BIT 2	J50-4A PIN 38 ○ READ CH5 BIT 1	J50-4A PIN 39 ○ READ CH6 BIT 0	J50-4A PIN 40 ○ PARITY	J50-4A PIN 29 ○ UNIT 7	J50-4A PIN 15 ○ CLEAR	J50-4A PIN 16 ○ FWD	J50-4A PIN 17 ○ REV	J50-4A PIN 18 ○ WR ENABLE	J50-4A PIN 19 ○ REWIND	J50-4A PIN 22 ○ UNIT 0	J50-4A PIN 23 ○ UNIT 1	J50-4A PIN 24 ○ UNIT 2	J50-4A PIN 25 ○ UNIT 3	J50-4A PIN 26 ○ UNIT 4	J50-4A PIN 27 ○ UNIT 5	J50-4A PIN 28 ○ UNIT 6
3	J50-4B PIN 34 ○ READ CH1 BIT 5	J50-4B PIN 35 ○ READ CH2 BIT 4	J50-4B PIN 36 ○ READ CH3 BIT 3	J50-4B PIN 37 ○ READ CH4 BIT 2	J50-4B PIN 38 ○ READ CH5 BIT 1	J50-4B PIN 39 ○ READ CH6 BIT 0	J50-4B PIN 40 ○ PARITY	J50-4B PIN 29 ○ UNIT 7	J50-4B PIN 15 ○ CLEAR	J50-4B PIN 16 ○ FWD	J50-4B PIN 17 ○ REV	J50-4B PIN 18 ○ WR ENABLE	J50-4B PIN 19 ○ REWIND	J50-4B PIN 22 ○ UNIT 0	J50-4B PIN 23 ○ UNIT 1	J50-4B PIN 24 ○ UNIT 2	J50-4B PIN 25 ○ UNIT 3	J50-4B PIN 26 ○ UNIT 4	J50-4B PIN 27 ○ UNIT 5	J50-4B PIN 28 ○ UNIT 6

TAPER PIN BLOCK #1

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V	W
1	WHITE 2G14P ○ END POINT	WHITE 2G14H ○ REWIND	WHITE 2G15H ○ READY	WHITE 2G15L ○ AUTO	WHITE 2G14T ○ WR LOCK	WHITE 2G14W ○ FULL REEL	WHITE 2G14Z ○ LOW REEL	WHITE 2G14L ○ LOAD POINT	5 LUG DKB TC SWITCH ○ OPERATE	○	○	5 LUG DKC TC SWITCH ○ READ ENABLE	2G1A +10A ○	○	2G1C -15 ○	POWER CONTROL ○ 822 TERM 1	○	○	○	○
2	J50-4A PIN 30 ○ END POINT	J50-4A PIN 31 ○ REWIND	J50-4A PIN 32 ○ READY	J50-4A PIN 33 ○ AUTO	J50-4A PIN 41 ○ WR LOCK	J50-4A PIN 42 ○ FULL REEL	J50-4A PIN 43 ○ LOW REEL	J50-4A PIN 44 ○ LOAD POINT	J50-4A PIN 45 ○ OPERATE	○	○	J50-4A PIN 48 ○ READ ENABLE	J50-4A PIN 47 ○	○	J50-4A PIN 49 ○	J50-4A PIN 46 ○ AUTO TURN ON	○	○	○	○
3	J50-4B PIN 30 ○ END POINT	J50-4B PIN 31 ○ REWIND	J50-4B PIN 32 ○ READY	J50-4B PIN 33 ○ AUTO	J50-4B PIN 41 ○ WR LOCK	J50-4B PIN 42 ○ FULL REEL	J50-4B PIN 43 ○ LOW REEL	J50-4B PIN 44 ○ LOAD POINT	J50-4B PIN 45 ○ OPERATE	○	○	J50-4B PIN 48 ○ READ ENABLE	○	○	○	J50-4B PIN 46 ○	○	○	○	○

Figure 8-5 Bus Panel Taper Pin Layout for Type 50 Alone

TAPER PIN BLOCK #3

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V	W
1	YELLOW 2G1R ○ WB 0 BIT 5	BLUE 2G1V ○ WB 0 BIT 5	YELLOW 2G1F ○ WB 1 BIT 4	BLUE 2G1L ○ WB 1 BIT 4	YELLOW 2G2R ○ WB 2 BIT 3	BLUE 2G2V ○ WB 2 BIT 3	YELLOW 2G2F ○ WB 3 BIT 2	BLUE 2G2L ○ WB 3 BIT 2	YELLOW 2G3R ○ WB 4 BIT 1	BLUE 2G3V ○ WB 4 BIT 1	YELLOW 2G3F ○ WB 5 BIT 0	BLUE 2G3L ○ WB 5 BIT 0	YELLOW 2G4R ○ WB 6 PARITY	BLUE 2G4V ○ WB 6 PARITY	WHITE 2G8V ○ SPEED 2	WHITE 2G8S ○ SPEED 1	BLACK 2G GND ○ GND	○	○	○
2	J50-4 PIN 1 ○ WB 0 BIT 5	J50-4 PIN 2 ○ WB 0 BIT 5	J50-4 PIN 3 ○ WB 1 BIT 4	J50-4 PIN 4 ○ WB 1 BIT 4	J50-4 PIN 5 ○ WB 2 BIT 3	J50-4 PIN 6 ○ WB 2 BIT 3	J50-4 PIN 7 ○ WB 3 BIT 2	J50-4 PIN 8 ○ WB 3 BIT 2	J50-4 PIN 9 ○ WB 4 BIT 1	J50-4 PIN 10 ○ WB 4 BIT 1	J50-4 PIN 11 ○ WB 5 BIT 0	J50-4 PIN 12 ○ WB 5 BIT 0	J50-4 PIN 13 ○ WB 6 PARITY	J50-4 PIN 14 ○ WB 6 PARITY	J50-4 PIN 20 ○ SPEED 2	J50-4 PIN 21 ○ SPEED 1	J50-4 PIN 50 ○ GND	○	○	○
3	2H1Y ○ WB 0 BIT 5	2H1Z ○ WB 0 BIT 5	2H1T ○ WB 1 BIT 4	2H1U ○ WB 1 BIT 4	2H1N ○ WB 2 BIT 3	2H1P ○ WB 2 BIT 3	2H1H ○ WB 3 BIT 2	2H1J ○ WB 3 BIT 2	2H3Y ○ WB 4 BIT 1	2H3Z ○ WB 4 BIT 1	2H3T ○ WB 5 BIT 0	2H3W ○ WB 5 BIT 0	2H3N ○ WB 6 PARITY	2H3P ○ WB 6 PARITY	TIE POINT ○ SPEED 2	TIE POINT ○ SPEED 1	2H GND ○	○	○	○

100Ω → 2H23J; 100Ω → 2H23F

TAPER PIN BLOCK #2

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V	W
1	GRAY 2G20L ○ READ CH1 BIT 5	GRAY 2G20N ○ READ CH2 BIT 4	GRAY 2G20P ○ READ CH3 BIT 3	GRAY 2G19L ○ READ CH4 BIT 2	GRAY 2G19N ○ READ CH5 BIT 1	GRAY 2G19P ○ READ CH6 BIT 0	GRAY 2G18L ○ PARITY	○	GRAY J50-13 ○ PIN 15 CLEAR	WHITE J50-13 ○ PIN 16 FWD	WHITE J50-13 ○ PIN 17 REV	WHITE J50-13 ○ PIN 18 WR ENABLE	WHITE J50-13 ○ PIN 19 REWIND	○	WHITE J50-13 ○ PIN 23 UNIT 1	WHITE J50-13 ○ PIN 24 UNIT 2	WHITE J50-13 ○ PIN 25 UNIT 3	○	○	○
2	J50-4 PIN 34 ○ READ CH1 BIT 5	J50-4 PIN 35 ○ READ CH2 BIT 4	J50-4 PIN 36 ○ READ CH3 BIT 3	J50-4 PIN 37 ○ READ CH4 BIT 2	J50-4 PIN 38 ○ READ CH5 BIT 1	J50-4 PIN 39 ○ READ CH6 BIT 0	J50-4 PIN 40 ○ PARITY	○	J50-4 PIN 15 ○ CLEAR	J50-4 PIN 16 ○ FWD	J50-4 PIN 17 ○ REV	J50-4 PIN 18 ○ WR ENABLE	J50-4 PIN 19 ○ REWIND	○	J50-4 PIN 23 ○ UNIT 1	J50-4 PIN 24 ○ UNIT 2	J50-4 PIN 25 ○ UNIT 3	○	○	○
3	2H21F ○ READ CH1 BIT 5	2H21Z ○ READ CH2 BIT 4	2H20F ○ READ CH3 BIT 3	2H20Z ○ READ CH4 BIT 2	2H18F ○ READ CH5 BIT 1	2H18Z ○ READ CH6 BIT 0	2H17F ○ PARITY	○	2H 7J ○ CLEAR	TIE POINT ○ FWD	TIE POINT ○ REV	TIE POINT ○ WR ENABLE	TIE POINT ○ REWIND	○	2H22H ○ UNIT 1	2H22L ○ UNIT 2	2H22P ○ UNIT 3	○	○	○

100Ω → 2H25N; 100Ω → 2H25L; 100Ω → 2H25T; 100Ω → 2H22T

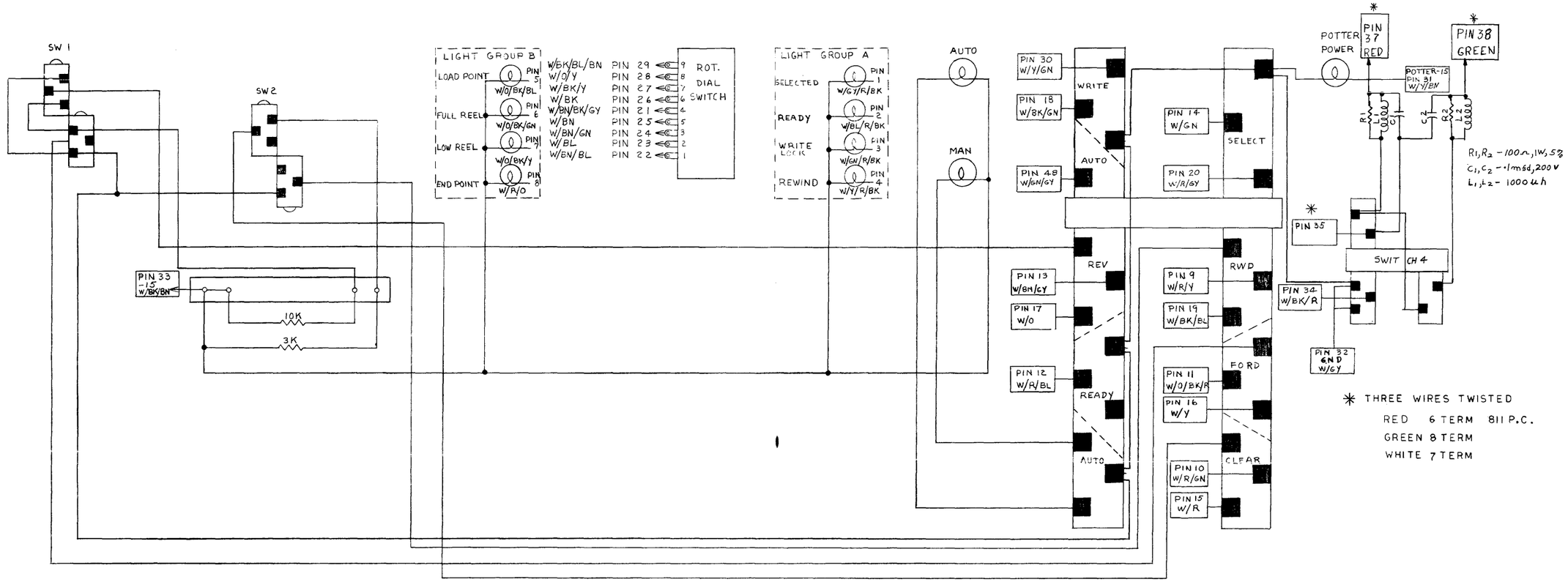
TAPER PIN BLOCK #1

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	V	W
1	WHITE 2G14P ○ END POINT	WHITE 2G14H ○ REWIND	WHITE 2G15H ○ READY	WHITE 2G15L ○ AUTO	WHITE 2G14T ○ WR LOCK	WHITE 2G14W ○ FULL REEL	WHITE 2G14Z ○ LOW REEL	WHITE 2G14L ○ LOAD POINT	WHITE 2G10E ○ OPERATE	○	○	WHITE 2G6M ○ READ ENABLE	RED 2 G1A ○ + 10A	RED 2 G1C ○ -15	○	POWER CONTROL #2 ○ 811 & 822 TERM #1	○	○	○	○
2	J50-4 PIN 30 ○ END POINT	J50-4 PIN 31 ○ REWIND	J50-4 PIN 32 ○ READY	J50-4 PIN 33 ○ AUTO	J50-4 PIN 41 ○ WR LOCK	J50-4 PIN 42 ○ FULL REEL	J50-4 PIN 43 ○ LOW REEL	J50-4 PIN 44 ○ LOAD POINT	J50-4 PIN 45 ○ OPERATE	○	○	J50-4 PIN 48 ○ READ ENABLE	○	○	○	J50-4 PIN 46 ○ AUTO TURN ON	○	○	○	○
3	J51-4 PIN 27 ○ END POINT	J51-4 PIN 22 ○ REWIND	J51-4 PIN 21 ○ READY	J51-4 PIN 28 ○ AUTO	J51-4 PIN 23 ○ WR LOCK	J51-4 PIN 25 ○ FULL REEL	J51-4 PIN 26 ○ LOW REEL	J51-4 PIN 24 ○ LOAD POINT	TIE POINT ○ OPERATE	○	○	TIE POINT ○ READ ENABLE	J50-4 PIN 47 ○	J50-4 PIN 49 ○	○	J51-4 PIN 46 ○ AUTO TURN ON	○	○	○	○

1500Ω → -15V; 100Ω → 2H23X; 100Ω → 2H25V

NOTE: ALL RESISTORS ARE LOCATED ON TERMINAL BOARDS ON FACE OF CONTROL 51 LOGIC

Figure 8-6 Bus Panel Taper Pin Layout for Types 50 and 51 Combination

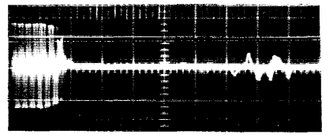


CABLE SCHEDULE FOR 50 PIN AMPHENOL CONNECTOR

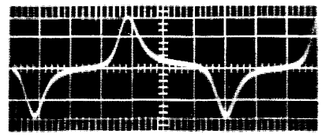
PIN NO.	COLOR	PIN NO.	COLOR	PIN NO.	COLOR	PIN NO.	COLOR
1	W/GY/R/BK	14	W/GN	27	W/BK/Y	39	W/Y/BL
2	W/BL/R/BK	15	W/R	28	W/O/Y	40	W/Y/GY
3	W/GN/R/BK	16	W/Y	29	W/BK/BL/BN	41	W/BN/O
4	W/Y/R/BK	17	W/O	30	W/Y/GN	42	W/BN/R
5	W/O/BK/BL	18	W/BK/GN	31	W/Y/BN	43	W/BK/GY
6	W/O/BK/GN	19	W/BK/BL	32	W/GY	44	W/O/GY
7	W/O/BK/Y	20	W/R/GY	33	W/BK/BN	45	W/O/BN/BK
8	W/R/O	21	W/BN/BK/GY	34	W/BK/R	46	W/Y/BN/BK
9	W/R/Y	22	W/BN/BL	35	W/BK/O	47	W/GN/BL
10	W/R/GN	23	W/BL	36	W/O/BL	48	W/GN/GY
11	W/O/BK/R	24	W/BN/GN	37	W/O/GN	49	W/BL/GY
12	W/R/BL	25	W/BN	38	W/GN/BN/BK	50	W/R/BN/BK
13	W/BN/GY	26	W/BK				

Figure 8-7 Manual Control Panel Wiring

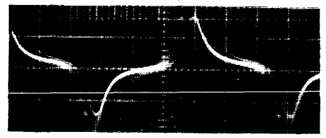
Figure 8-8



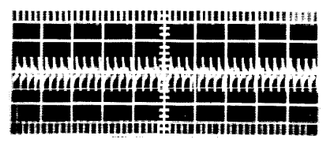
Pinch Roller Bounce



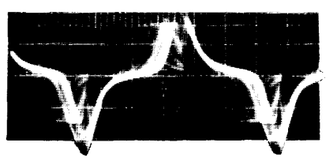
Normal Read Waveform



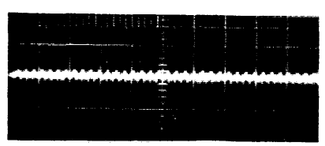
Mild Write Coupling



Write Coupling - Tape Absent



Severe Write Coupling



Ideal Minimum

Figure 8-8 Typical Waveforms