PDP-X Technical Memorandum # 21

Title: Processor/Memory Timing Relations

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Timing

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The timing relations between the central processor hardware (registers, gates, adders) and the main memory system are examined. The results indicate the speed requirements for the central processor and for the control memory.

In order to arrive at speed goals for the central processor hardware, several constraints were placed on the processor organization. These constraints logically lead to further constraints from which operating speeds and requirements may be determined. A 20% safety factor is normally applied after worst-case analysis to accommodate changes in component specifications.

The basic assumptions are:

1. The main memory cycles at less than 1 usec and has short access time. The arithmetic processor designed for this memory system will, of course, work with slower memories. Details of the choice of memory system are given in Technical Memorandum #22.

2. Two of the processor time states are initiated by signals from the memory system. The two signals are:

a.	ADDR ACK	address acknowledge; indicates that the memory has received the address and control information sent to it.
b.	RD RST	read restart; indicates that the memory data has been placed on the data lines.

3. The memory system is kept running at full speed; i.e., the new address is calculated and sent to the memory before the memory has completed its current cycle.

4. The cable delay between the central processor and the memory (and conversely) is 50 NS including receivers and transmitters. This represents approximately ten feet.

5. Each main memory cycle will contain three processor cycles. There will be one cycle before memory data has reached the processor (between ADDR ACK and RD RST) and two processor cycles after memory strobe time. The address for the next main memory cycle must be calculated during the first processor cycle after memory strobe time (RD RST) and may not be changed by the second processor cycle after RD RST.

6. The RD RST signal is received (by the processor) 300 NS after the receipt of the ADDR ACK signal.

These assumptions are used to develop constraints based upon various main memory cycle times. The fastest memory cycle time realizable with proposed technology (20 mil cores, 3D, common sense/digit) is 750 NS. Lengthening the cycle time corresponds to allowing larger dead times and longer address set-up times. Some of the constraints on the central processor and central memory timing may also be relaxed.

Figure 1 shows the main memory timing for a cycle time of 750 NS. An increase in cycle time corresponds to an increase in the dead-time.

These assumptions lead to the following constraints which are expressed as inequalities: (in the following, M stands for Main memory cycle time, A stands for control memory Access time, C stands for processor Cycle time. All times are expressed in nanoseconds.)

1. $A + C \leq M - 400$

   The address for the next memory reference must be calculated by time M - 100 (RQ, ADDRESS at CP). Since this address may depend on the data received by the processor at time 300 (RD RST at CP) and since a control memory word has to be read as a function of this data, $A + C \leq (M - 100) - 300$ yielding the stated relation.

2. $A + 2C \leq M - 100$

   From time 0 (ADDR ACK at CP) to time M - 100 (RQ, ADDRESS at CP) two cycles and one access, must be completed. The control memory access occurs starting at time 0. After this access, 2 processor cycles must be completed by time M - 100. (Note: the first cycle may overlap the access starting at time 300. This leads to the following constraint.)

3. $A \leq C$

   This must be true for the above assumptions to be valid.

4. $C \leq (M - 300)/2$

   After time 300 (RD RST at CP) one control memory access and two processor cycles must be completed before the access starting at time 0 (or time M, ADDR ACK at CP) has completed. This leads to $A + 2C \leq M - 300$ which yields the stated relation.

These four (constraints) inequalities are plotted (dotted lines) in Figure 2 for M = 750 NS. The solid lines reflect these constraints with a 20% safety factor. The allowable region for the parameters A, C is in the lower left-hand region. A point was chosen within the 20% area which yields

Main memory cycle time	= 750 NS
Control memory access time	= 100 NS
Processor cycle time	= 180 NS

Using these values, the processor/memory timing for a 750 NS memory is redrawn in Figure 3.

The timing relations for this system during a read-modify-write operation are illustrated in Figure 4. If the cable delay decreases, the total time for this operation decreases. This is not true, however, for the normal read operation.

Since M = 750 NS represents the fastest achievable memory system, these constraints are examined with different values of M to determine the effect upon control memory access time and upon the central processor cycle time. The results (with a 20% safety factor) are indicated in Figure 5. Again, the allowable region for A and C is the region in the lower left-hand corner. As M is increased, the constraints on A and C are relaxed until M = 1 usec at which point the assumption of RD RST at 300 NS limits further improvement in processor cycle.

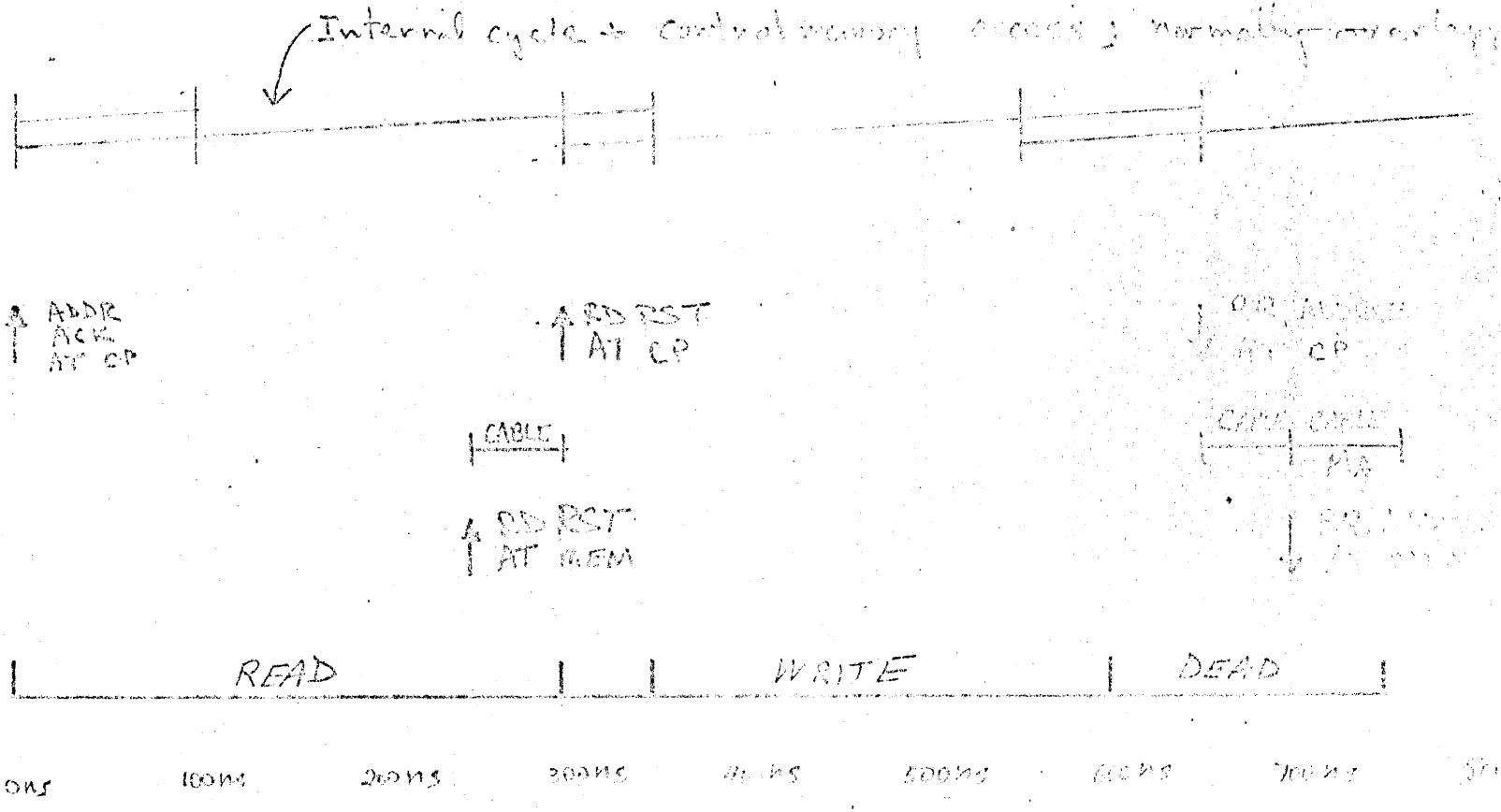
In conclusion, the fastest achievable memory system (M = 750 NS) leads to a control memory access time of 100 NS and a central processor cycle time of 180 NS. Preliminary design of the central processor data paths indicate that such a processor internal cycle time is not easily achievable. Similarly, in light of experience with the PDP-9 control memory, a 100 NS access time appears difficult to achieve. It, therefore, appears that a slower memory would be more cost-effective. While final specifications for main memory cycle, control memory access, and processor internal cycle will be set after further development clarifies the cost/performance trade-offs, the following will serve as guidelines:

800 NS main memory (read-restore) cycle

200 NS processor internal cycle

120 NS control memory access time

Figures 6 and 7 show processor/memory timing based upon these guidelines.



MAIN MEMORY

MAW MEMORY
CONTROL MEMORY
TIMING RELATIONS
Figure 1.

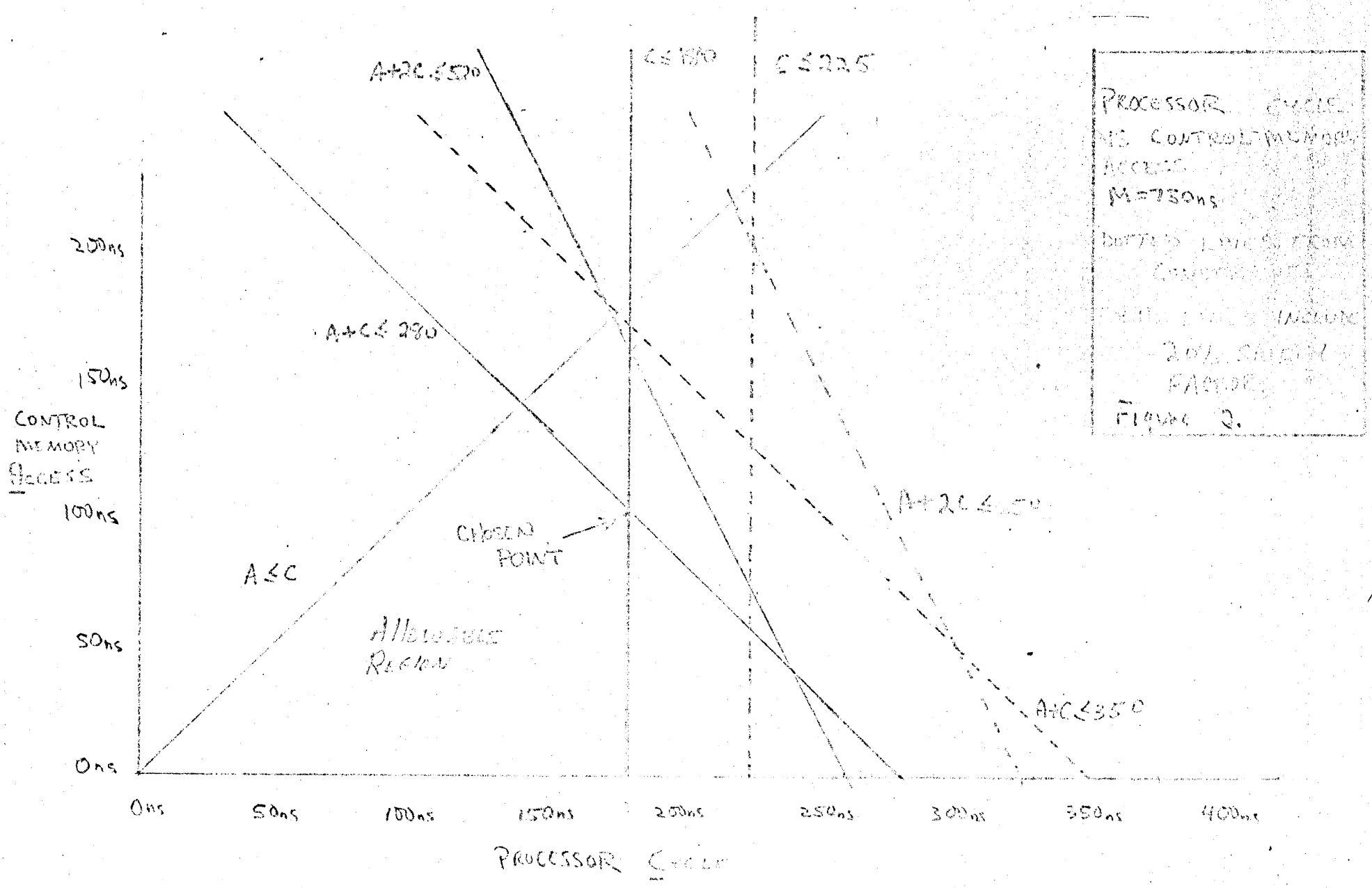
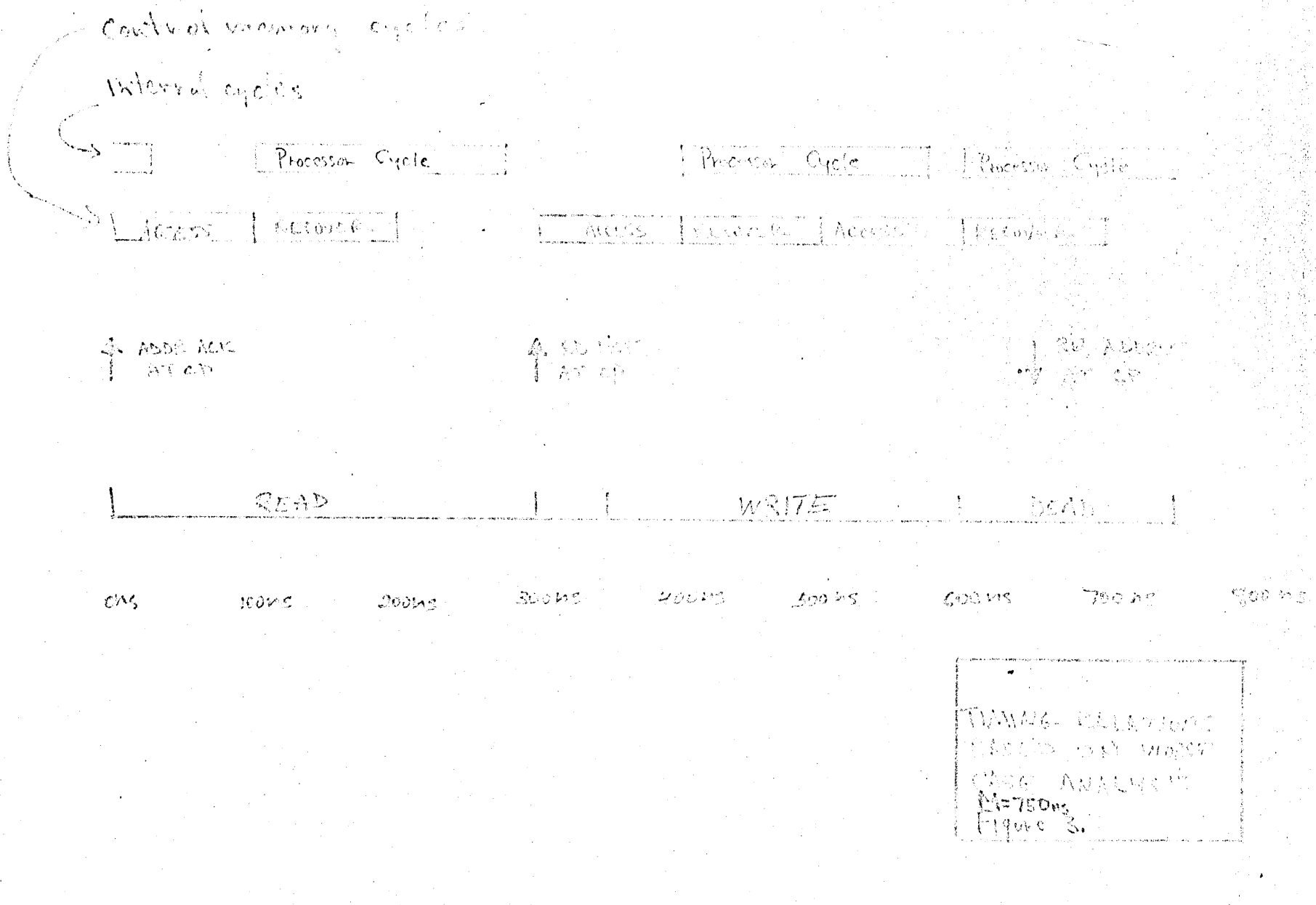
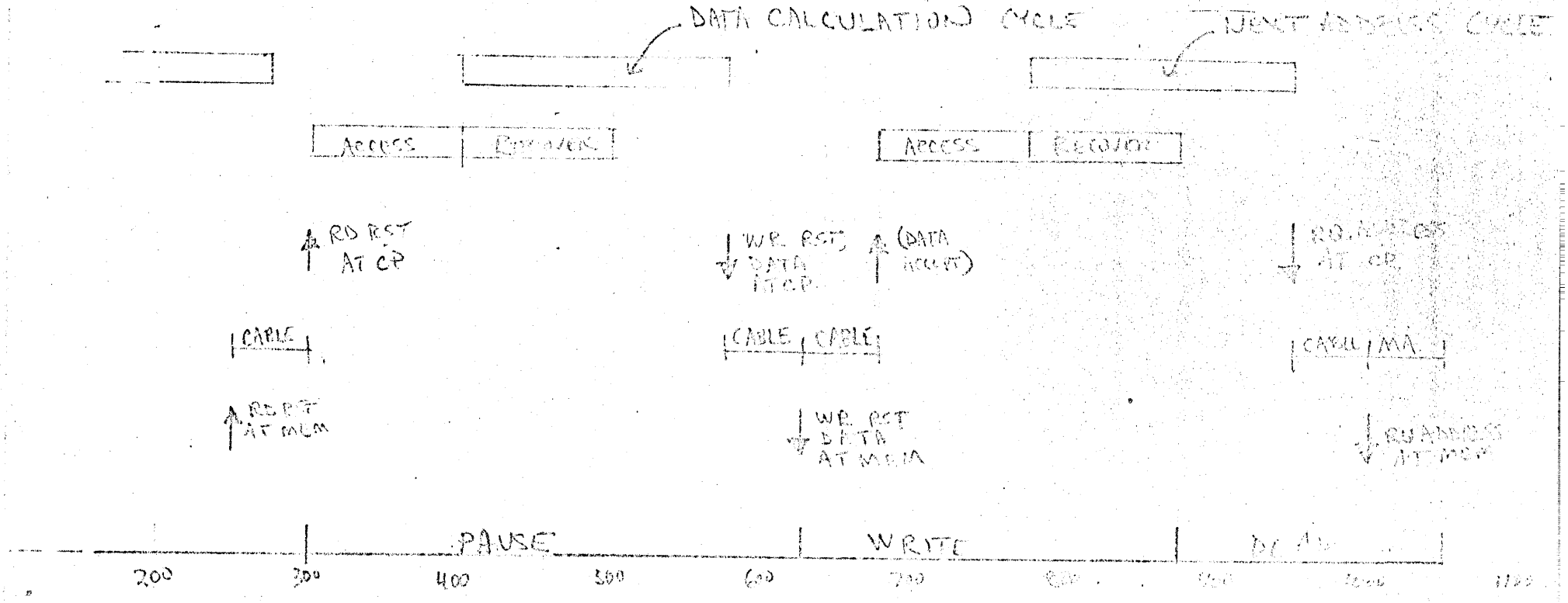

A+2C≤500
C≤150
C≤225
A+C≤280
A+2C≤450
A+C≤350
A≤C
CHOSEN POINT
Allowable Region
200ns
150ns
100ns
50ns
0ns
CONTROL MEMORY ACCESS
0ns
50ns
100ns
150ns
200ns
250ns
300ns
350ns
400ns
PROCESSOR CYCLE
PROCESSOR CYCLE
MS CONTROL MEMORY ACCESS
M=150ns
20% SAFETY FACTOR

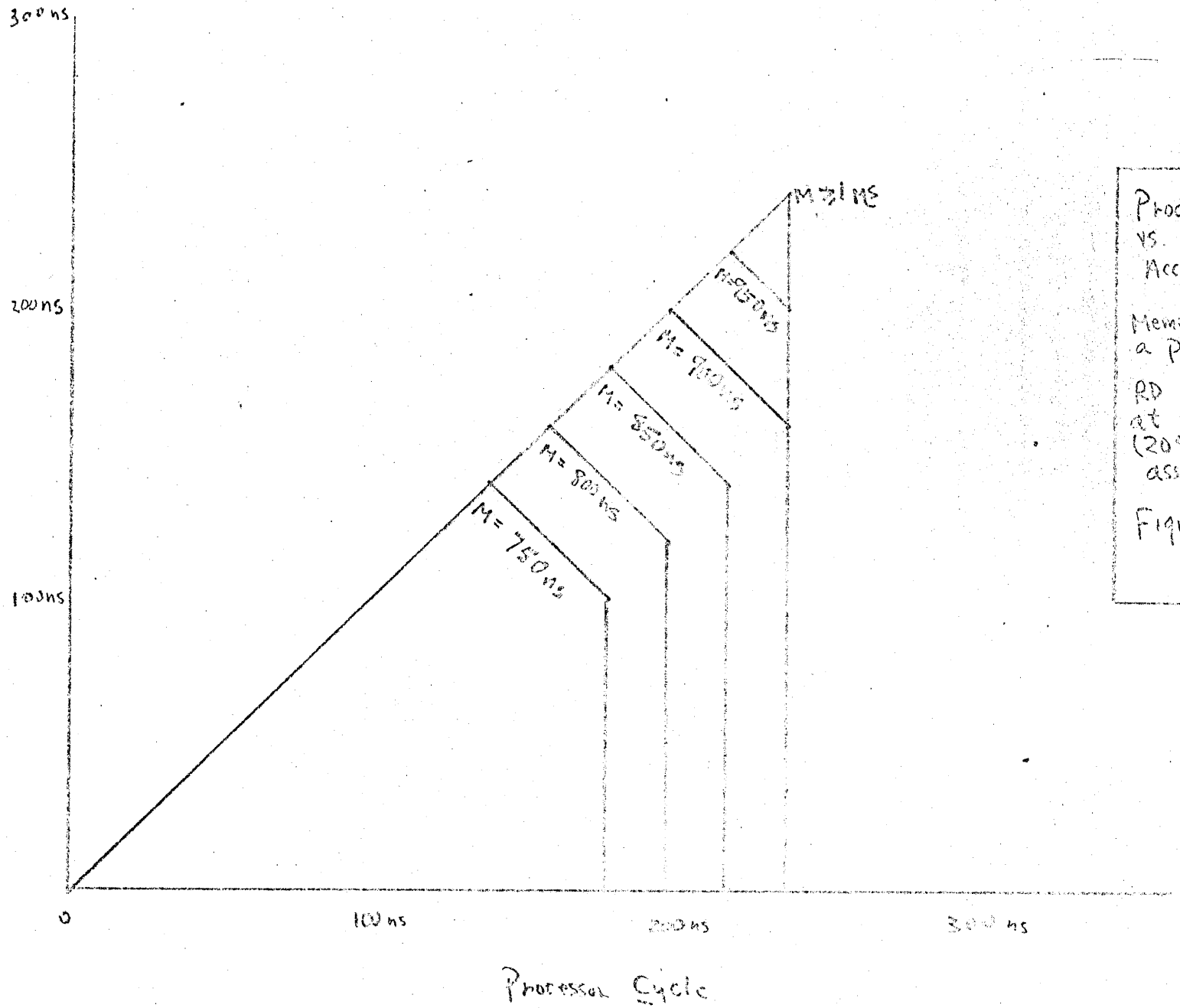
Figure 2.



TIMING RELATIONSHIP BETWEEN MEMORY CYCLE ANALYSIS
Δt=750ns
Figure 3.



TIMING RELATIONS DURING READ/ MODIFY/WRITE M=750 Figure 4.

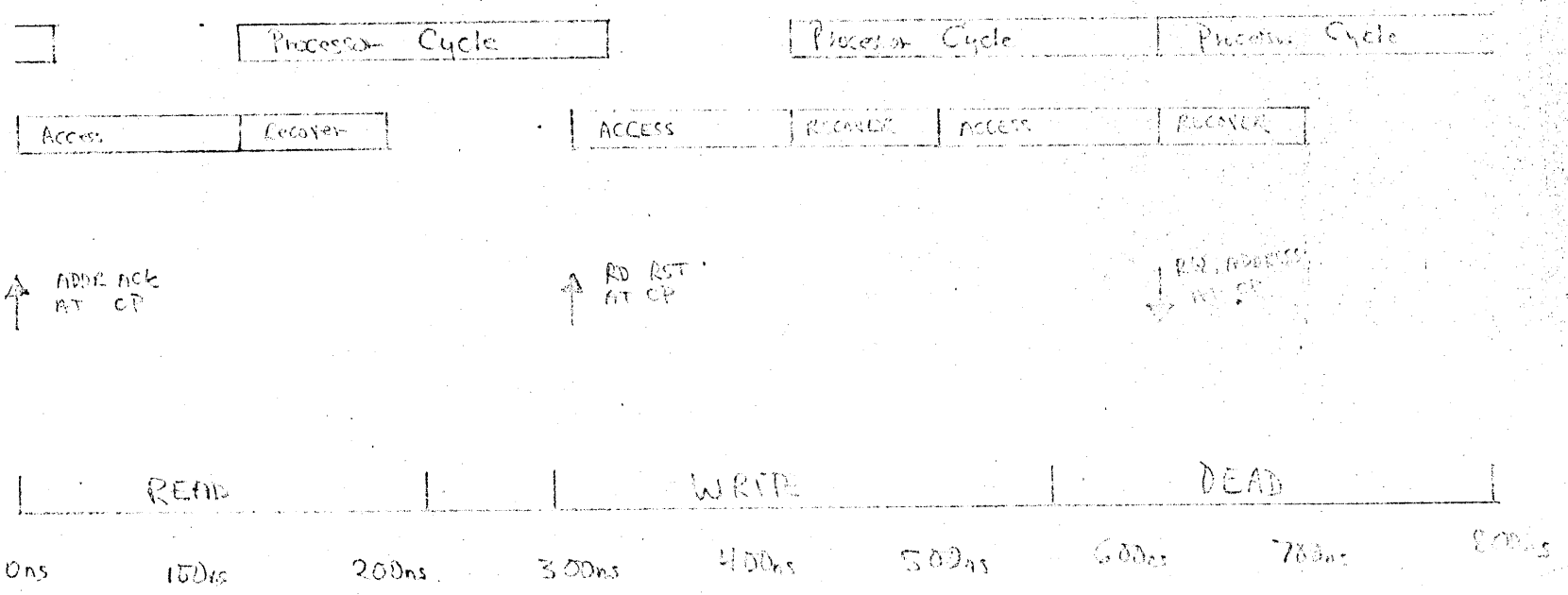


Processor Cycle vs. Control Memory Access

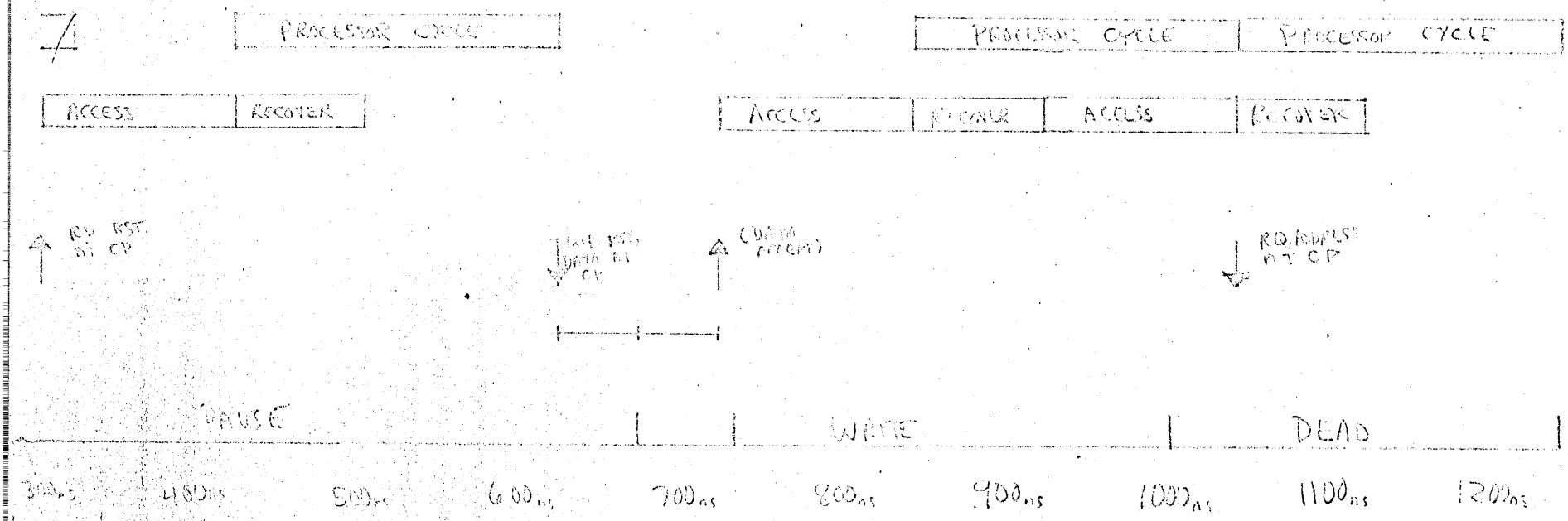
Memory Cycle as a parameter

RD RST Time fixed at time 300 (20% Safety Factors assumed).

Figure 5.



Timing Relations
Based on Worst
Case Analysis
Memory Cycle = 800ns
Figure 6



Timing Relations
During Read/Modify/
WRITE
Memory Cycle = 800ns
Figure 7