MPS MICROPROCESSOR DEVELOPMENT SYSTEM

OPERATING GUIDE

Prepared by

Logic Products Group

Digital Equipment Corporation

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FOREWORD

This operating guide provides general and detailed descriptions of the basic MPS Microprocessor Development System, its hardware and software systems, and the optional modules and equipment available. Also included is the information necessary for the user to install, program, and operate the system. References are made throughout this guide to detailed supporting software and hardware documentation. For specific applications information not contained within this guide, contact your local DIGITAL sales representative.

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CHAPTER 1

INTRODUCTION

1.1 GENERAL

The Microprocessor Series (MPS) Development System is composed of a general purpose, programmable processor module and standard and optional plug-in modules with associated mounting hardware and accessories. The MPS Development System can be assembled and programmed by the user to perform a wide range of process monitor and control, data acquisition, or decision-making functions. The microprocessor module performs the data manipulation and controls the input/output and memory modules. The modular construction allows a basic system developed for a specific application to be easily expanded to meet future requirements. Operating programs for the MPS can be developed using the basic MPS components and additional modules and hardware, or using most existing PDP-8 processor systems.

Each MPS Development System is capable of receiving a maximum of five 8-bit parallel data words from external sources and providing a maximum of six 8-bit parallel data words for the control of external devices. The input interfaces accept TTL-compatible signals, and the output interfaces provide open collector output drivers for TTL loads or indicators and relays.

Serial data, in ASCII format, can be transferred between the processor and a teletypewriter or similar device over a 20 mA current loop line.

The memory can be expanded from 2K words to a total capacity of 16K words using available read/write memory (RAM) modules or programmable read-only memory (PROM) modules.

A monitor/control panel is available as an option to provide on-line control and program diagnostic capability. The panel contains switches to load address and data information into the system and indicators to display machine states and register contents.

A complete line of mounting boxes and panels, cable assemblies, and accessories are made available with the system to facilitate installation.

Power to the system can be provided from a DIGITAL power supply or by a recommended power supply purchased by the user.

1.2 APPLICATIONS

Systems assembled from the MPS elements can serve as communication controllers, central processors in intelligent terminals, machine and process controllers, laboratory instrument control, and data acquisition devices. Figure 1-1 shows a typical configuration operating with input sense signals and output control signals.

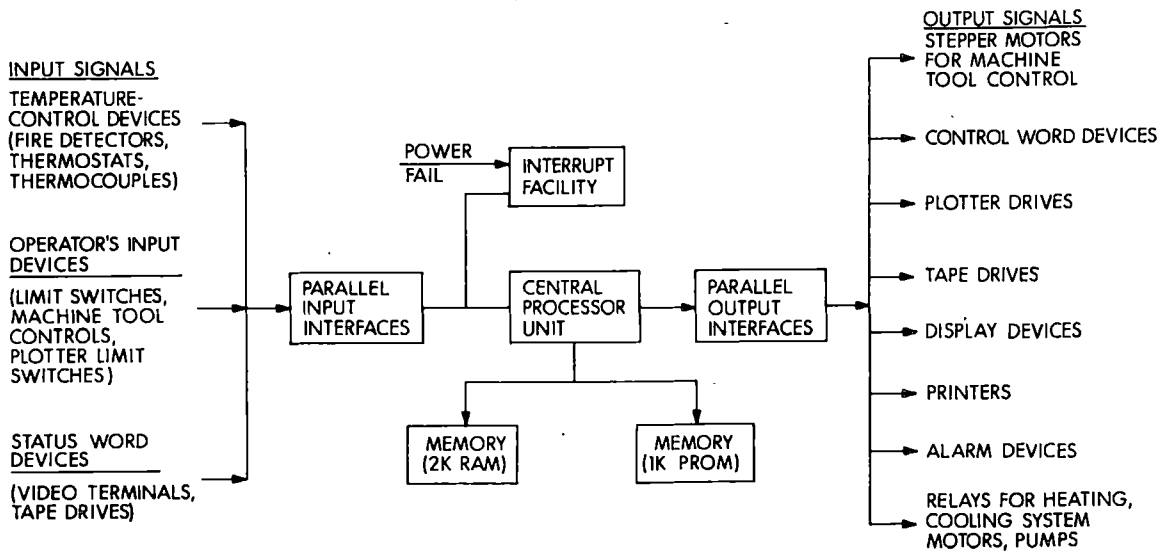


Figure 1-1. Typical MPS Development System Applications

1.3 REFERENCED DOCUMENTS

The publications listed in Table 1-1 provide additional detailed information related to the operation and interfacing of MPS Development System modules, options, and hardware. The documents referenced, but not supplied with the MPS system, may be ordered through a local DIGITAL Sales Office or by contacting:

Digital Equipment Corporation
Components Group
One Iron Way
Marlborough, Massachusetts 01752

Attn: Program Manager - Microprocessors

Table 1-1

MPS Referenced Documents

*M7341 Processor Module Data Sheet
*M7344-YA, -YB, -YC Read/Write Memory Module Data Sheet
*M7345 Programmable Read-Only Memory Module Data Sheet
*M7346 External Event Detection Module Data Sheet
*M7347 Paper Tape Reader-Run Module Data Sheet
*M7328 Evoke Decoder Module Data Sheet
*M1501 Bus Input Interface Module Data Sheet
*M1502 Bus Output Interface Module Data Sheet
MR873 Microprocessor ROM Programmer Product Bulletin
General Interfacing Techniques for the M7341 Microprocessor Module Application Note
Interfacing the TU60 to the MPS M7341 Microprocessor Application Note
*MPS Microprocessor Series User's Handbook
*MPS User's Handbook Change Notice
*Communicating with DIGITAL's MPS Microprocessor
*MPS Microprocessor Series Pocket Reference Card
**MPS Resident Software Checkout Procedure
*MPS Development System Logic Prints
1975-76 DIGITAL Logic Handbook
Hardware/Accessories Catalog

*Supplied with Development System.

**Supplied with QY500-AB Software Package.

1.4 EQUIPMENT LIST

Table 1-2 lists and describes the basic hardware and software items which comprise the MPS Development System and the optional hardware and equipment available from DIGITAL. This list can be used to check the items received by the customer or to order additional items when required.

1.5 EQUIPMENT SPECIFICATIONS

The general mechanical, electrical, and environmental specifications for the MPS Development System are listed on page 1-5. Detailed data on specific items available or supplied is provided in the related documents listed in Table 1-1.

Table 1-2

MPS Equipment List

Item	Part	Description
1	M7341	Processor Module
2	M7345	4K x 8 Read-Only (PROM) Memory Module (with MDP preprogrammed and installed in 1K)
3	M7345	4K x 8 Read-Only (PROM) Memory Module (user programmed)
4	M7344-YA	1K x 8 Read/Write (RAM) Memory Module
5	M7344-YB	2K x 8 Read/Write (RAM) Memory Module
6	M7344-YC	4K x 8 Read/Write (RAM) Memory Module
7	M1501	Bus Input Interface Module
8	M1502	Bus Output Interface Module
9	M7328	Evoke Decoder Module
10	M7347	Paper Tape Reader-Run Module
11	M7346	External Event Detection Module
12	M111	Inverter Module
13	G772	Power Connector Module
14	G720	Bus Terminator Module
15	KMP02	System Unit, Prewired
16	BC07A	Device Cable Assembly; H856 Connector to open end, 20-conductor twisted pair
17	BC07D	Device Cable Assembly; H856 Connector to open end, two 20-conductor ribbon
18	BC05Y	Power Cable Assembly used on KC341-B; G772 Connector to Faston tabs
19	BC05W	Signal Cable Assembly used on KC341-B
20	H909-A	Mounting Enclosure (KMP02 and power supply mounting)
21	H909-BA	Mounting Enclosure (includes H755 Power Supply and BC05H Line Set)
22	KC341-B	Monitor/Control Panel
23	2S-140T	Adapter Plate with mounting screws
24	H014	19" Rack Mounting Panel
25	12-11041	Pushbutton switch, momentary contact
26	BC05H	Line Set, 115 Vac with 7 A circuit breaker
27	BC05J	Line Set, 230 Vac with 3 A circuit breaker
28	QY500-AB	Resident Software Package for MPS Programming System
29	QF500-AB	Resident Software Package for MPS using PDP-8 Processor (except PDP-8/S)
30	BC08R-1	I/O Test Cable Assembly

Environmental

Temperature:	
Storage	-40°C to 66°C (-40°F to 150°F)
Operating	5°C to 50°C (41°F to 122°F)
Relative Humidity	10% to 95% non-condensing

Word Size

Data	8 bit word
Peripheral Data	8 bits
Power Fail/Stop	8 bits multiplexed
I/O Interrupt/Start	8 bits

Communication Lines

Serial I/O	Two 20 mA current loops--one for receive, one for transmit; active or passive
Baud Rate (with internal clock)	110 baud (1.76 KHz)
Baud Rate (with external clock)	9600 baud (153.6 KHz) maximum (TTL) 4800 baud (76.8 KHz) maximum (20 mA current loop)

Mounting Area

Panel Mounted*	5.19 in. (13.18 cm) H x 19.00 in. (48.26 cm) W x 11.25 in. (28.57 cm) D
H909-A, H909-BA Enclosure	5.25 in. (13.34 cm) H x 17.38 in. (26.38 cm) W x 20 in. (50.80 cm) D
Monitor/Control Panel	10 in. (25.4 cm) H x 16.5 in. (41.9 cm) W x 4.75 in. (11.06 cm) D

*Power supply not included in dimensions.

CHAPTER 2

GENERAL DESCRIPTION

The MPS Development System consists of a processor configuration used to perform the data acquisition and process control functions and a programming configuration used to develop the operating programs. The programming system can be composed of modules and hardware from the processor system, together with additional modules and input/output devices. A special software package consisting of paper tapes, operating instructions, and forms are also available for use with the programming system.

Operating programs can also be developed on existing PDP-8 processor systems (except for the PDP-8/S), using a separate software package available from DIGITAL.

2.1 PROCESSOR SYSTEM COMPONENTS

The basic processor is supplied with eleven system modules, two power connector modules, and a bus terminator module as listed in Table 2-1. The modules plug into the KMP02 System Unit, and the customer input and output devices connect to the modules via BC07D I/O data cables.

The M7345 module supplied with the basic processor system contains four PROM circuits which are preprogrammed with the Microprocessor Debugging Program (MDP). This program enables the user to read, modify, and write processor programs through the LT33-DC Teletypewriter or equivalent terminal.

The memory capacity of the processor system can be expanded to 16K words by the addition of M7345 and/or M7344 modules. The system will accept a total of four memory modules in any RAM or PROM combinations.

The basic input and output capability can be expanded by wiring the blank slots in the KMP02 and by including two additional M1501 modules and one additional M1502 module.

Table 2-1

Processor System Components

Basic System	
Modules	Hardware/Accessories (supplied with basic system)
1 - M7341 Processor Module 1 - M7344-YA RAM Memory Module (1K) 1 - M7345 PROM Memory Module (with 1K MDP supplied) 1 - M7346 External Event Detection Module *3 - M1501 Bus Input Interface Modules *2 - M1502 Bus Output Interface Modules 1 - M7328 Evoke Decoder Module 1 - M111 Inverter Module 2 - G772 Power Connector Modules 1 - G720 Terminator Module	1 - KMP02 System Unit

Options Available	
Modules	Hardware/Accessories
M7345 PROM Memory Module (4K) M7344-YA RAM Memory Module (1K) M7344-YB RAM Memory Module (2K) M7344-YC RAM Memory Module (4K) M1501 Bus Input Interface Module M1502 Bus Output Interface Module	BC07D-10 Cable (two 20-conductor flat ribbon cables) H909-A System Unit Drawer H909-BA System Unit Drawer (includes H755 Power Supply and BC05H Line Set) H014 19" Rack Mounting Panel 12-11040 Start Switch BC08R-1 Test Cable Mounting Plate for 2S-140T Power Supply

*System prewired to accept total of five M1501 and three M1502 modules.

2.2 PROGRAMMING SYSTEM COMPONENTS

Table 2-2 lists the modules and hardware necessary for program development and the items included in each of the resident software packages. Refer to Table 2-1 for optional hardware and accessory items available.

Programs can be developed using the same M7341 Processor Module and KMP02 Backplane supplied with the processor system. Two M7344-YC 4K memory modules, an M7347 Paper Tape Reader-Run Module, the KC341-B Monitor/Control Panel, and an LT33-DC Teletypewriter are also required.

2.3 SOFTWARE PACKAGES

Two software packages are available with the MPS Development System, as listed in Table 2-2 and described below. The QY500-AB provides the paper tapes and supporting

Table 2-2

Programming System Components

Modules	Hardware/Accessories	Software Package
1 - M7341 Processor Module 2 - M7344-YC RAM Memory Modules (4K) 1 - M7347 Paper Tape Reader-Run Module 1 - G772 Power Connector Module	1 - KMP02 System Unit *1 - LT33-DC Teletypewriter 1 - KC341-B Monitor/Control Panel with a BC05W Signal Cable and BC05Y Power Cable *1 - Power Supply and Mounting Accessories	QY500-AB: 1 - MLA Paper Tape 1 - MLE Paper Tape 1 - MDP Paper Tape Checkout Procedures Software Reporting Form Software Registration Form MPS Microprocessor Series User's Handbook and Errata Sheets
PDP-8 computer system (with Teletype facility including paper tape punch and reader)		QF500-AB: 1 - MLA Paper Tape 1 - MLE Paper Tape 1 - MDP Paper Tape 1 - MRP Paper Tape 1 - MHL Paper Tape 1 - MTD Paper Tape

*Optional

forms and documents for developing programs on the MPS Programming System. The QF500-AB allows MPS operating programs to be developed using an existing PDP-8 Processor System except for the PDP-8/S. Refer to the MPS Microprocessor Series User's Handbook for detailed information on the paper tape programs.

Software Package QY500-AB contains:

1 - Microprocessor Language Assembler (MLA) Paper Tape

1 - Microprocessor Language Editor (MLE) Paper Tape

1 - Microprocessor Debugging Program (MDP) Paper Tape

Checkout Procedures

Software Reporting Form

Software Registration Form

MPS Microprocessor Series User's Handbook and Errata Sheets

Software Package QF500-AB contains:

1 - Microprocessor Language Assembler (MLA) Paper Tape
(Runs on PDP-8*)

1 - Microprocessor Language Editor (MLE) Paper Tape
(Runs on PDP-8*)

1 - Microprocessor Debugging Program (MDP) Paper Tape
(Runs on MPS)

1 - Microprocessor ROM Programmer (MRP) Paper Tape
(Runs on PDP-8*)

1 - Microprocessor Host Loader Program (MHL) Paper Tape
(Runs on PDP-8*)

1 - Master Tape Duplicator Program (MTD) Paper Tape
(Runs on PDP-8*)

*Except PDP-8/S.

Additional programs are currently available through DECUS (DEC Users Society) and include floating point packages, trigonometric function packages, and exponential function packages. Contact the nearest DIGITAL Sales Office or DECUS (at the address below) for a list of the latest MPS programs available.

Digital Equipment Computer Users Society (DECUS)
146 Main Street, PK3-1/E55
Maynard, Massachusetts 01754

2.4 MODULES AND HARDWARE FUNCTIONS

The function of each of the modules, cables, and hardware is described in the following paragraphs. Refer to Table 1-1 for documents supplied or available which provide more detailed information.

2.4.1 M7341 Processor Module

The M7341 Processor Module operates as an 8-bit parallel processor in the MPS Development System. The M7341 occupies four slots of the KMP02 System Unit and contains an MOS/LSI microprocessor chip, together with the I/O control and memory addressing logic that performs the memory addressing and input/output operations. The processor includes a serial, asynchronous transmitter/receiver and optical couplers to enable the M7341 to be connected to an LT33-DC Teletypewriter, VT50 DECscope Video Display, LA36 DECwriter II Data Terminal, or any compatible DIGITAL device. When the KC341-B Monitor/Control Panel is used with the system, a cable from the panel attaches to a 50-pin connector mounted on the edge of the processor module.

For detailed operating information and specifications on the M7341 Processor Module, refer to the 1975-76 DIGITAL Logic Handbook, the MPS Microprocessor Series User's Handbook, and the M7341 Processor Module data sheet.

2.4.2 M7345 Programmable Read-Only (PROM) Module

The M7345 PROM module supplied with the MPS processor configuration contains four preprogrammed 1702A PROMs and mounting sockets for 12 additional PROMs. The module occupies four slots of the KMP02 System Unit. Each PROM socket provides mounting for a 256 x 8-bit word MOS semiconductor memory for a total memory capacity of 4096 8-bit words in the 16 sockets included with the M7345 module. Extra PROM circuits are available from DIGITAL and can be electrically programmed at DIGITAL or by a user with a PDP-8 computer system and an MR873-A Microprocessor ROM Programmer.

In addition to memory storage, the module contains an address buffer, address and control decoding logic, and an output gating network. Specific memory locations are selected by the 16 address bits from the M7341 Processor Module.

The four preprogrammed PROM circuits occupy 1K x 8-bit word locations and are used when operating the Microprocessor Debugging Program (MDP).

Refer to the 1975-76 DIGITAL Logic Handbook, the M7345 Programmable Read-Only Memory Module data sheet, or the MPS Microprocessor Series User's Handbook for detailed operating information and specifications.

2.4.3 M7344-YA, -YB, -YC Read/Write Memory (RAM) Module

The M7344 Random Access Memory is available in three memory capacity configurations:

M7344-YA. . . . . 1K x 8-bit words
M7344-YB. . . . . 2K x 8-bit words
M7344-YC. . . . . 4K x 8-bit words

One M7344-YC module is supplied with each MPS Development System and occupies four slots of the KMP02 System Unit. Additional modules can be added to the system for a total RAM or PROM memory configuration of 16K x 8-bit words.

In addition to the memory circuits, each read/write memory module has a buffer register, decoding logic, input data register, output data gates, and timing and control logic. Specific memory locations are selected by the 14 address bits from the M7341 Processor Module.

For detailed data on the M7344 series modules, refer to the 1975-76 DIGITAL Logic Handbook, the M7344-YA, -YB, -YC Read/Write Memory Module data sheet, and the MPS Microprocessor Series User's Handbook.

2.4.4 M7346 External Event Detection Module

The M7346 module is capable of monitoring up to six individual interrupt request signals, an ac and dc power fail signal produced by a low ac or dc system voltage, and a Halt and Auto Restart signal. The arbitration logic on the M7346 assigns priority to the detected signals and provides an encoded output to the processor to initiate a subroutine in honor of the specified request.

The processor Halt function has the highest priority, and the ac or dc power fail has the highest arbitrated priority. Each of the six interrupt request signals, generated when an external device requests an input data transfer, is assigned a priority level dependent upon the location of the M1501 module in the KMP02 System Unit.

Two Faston(TM) terminals, mounted near the edge of the module, facilitate the connection of leads from a 6.3 Vac source. The input ac voltage is used by the ac power fail detection logic and to generate an ac sync signal used for real-time processor applications. All other input and output signals and voltages are through the KMP02 backplane wiring. The M7346 occupies one slot in the KMP02 backplane.

For detailed information on the M7346 module, refer to the MPS Microprocessor Series User's Handbook, the 1975-76 DIGITAL Logic Handbook, and the M7346 External Event Detection Module data sheet.

2.4.5 M7328 Evoke Decoder Module

The M7328 module functions as a device selector and decodes the five address bits on the M7341 Processor Module data/address bus to select one of eight input devices or one of 24 output devices for data transfer. The module contains a 5-line to 32-line decoder and an input gating logic configuration to enable the decoding logic. Each of the 32 outputs from the decoder enables a specific input/output interface to perform a data transfer to or from an external device. The M7328 module occupies two slots in the KMP02 System Unit.

For detailed information on the M7328 module, refer to the 1975-76 DIGITAL Logic Handbook, the M7328 Evoke Decoder Module data sheet, and the General Interfacing Techniques for the M7341 Processor Module application note.

2.4.6 M1501 Bus Input Interface Module

Each M1501 module transfers one 8-bit parallel data input from an external device to the M7341 processor input bus when enabled by a device address from the processor. The MPS Development System has facilities for mounting up to five M1501 modules. The M1501 module includes the logic for generating control signals between the device and interface and for initiating an interrupt request signal to the processor. A 40-pin connector, mounted near the edge of the module, allows data and control signals to be transferred through a BC07D ribbon cable or BC04Z flat shielded cable. The input interface module occupies one slot in the KMP02 System Unit.

For detailed information on the M1501 module, refer to the 1975-76 DIGITAL Logic Handbook and the M1501 Bus Input Interface Module data sheet.

2.4.7 M1502 Bus Output Interface Module

The M1502 module is a buffered output interface which transfers two 8-bit parallel data words from the data/address bus of the MPS system to the external device. Up to three M1502 modules can be mounted on the KMP02 System Unit, providing a total of six data output words. The M1502 module includes control logic for sequencing the data transfers and interrupt request logic to enable the external device to initiate a data transfer. The M1502 module occupies two slots in the KMP02 System Unit.

A 40-pin connector, mounted near the edge of the module, allows the data and control signals to be transferred through a BC07D ribbon cable or BC04Z flat ribbon cable.

For detailed information on the M1502 module, refer to the 1975-76 DIGITAL Logic Handbook and the M1502 Bus Output Interface Module data sheet.

2.4.8 M111 Logic Inverter Module

The M111 module provides necessary circuits to invert the TTL logic levels within the MPS Development System. The M111 inverts the device selector output levels from the M7328 Evoke Decoder Module and the interrupt request signals from an input device through the bus interfaces. The module occupies one slot in the KMP02 System Unit.

The 16 inverter circuits on the M111 module will allow the MPS system expansion to five M1501 Bus Input Interface Modules and three M1502 Bus Output Interface Modules.

For detailed information on the M111 module, refer to the 1975-76 DIGITAL Logic Handbook.

2.4.9 M7347 Paper Tape Reader-Run Module

The M7347 module controls the operation of the paper tape reader on the teletypewriter when used with the MPS programming system. The M7347 transfers the serial data between the M7341 Processor Module and the LT33-DC Teletypewriter or an equivalent

terminal. The module provides four control lines to activate or disable the reader before and after data transfers. The module connects to the M7341 module by an attached cable and mating connector. The teletypewriter cable mates with the connector mounted on the edge of the M7347. The module occupies one slot in the KMP02 System Unit.

For detailed information, refer to the M7347 Paper Tape Reader-Run Module data sheet.

2.4.10 G720 Bus Terminator Module

The G720 module consists of fifteen 470-ohm pull-up resistors which connect to the +5 Vdc system power. The G720 is an impedance matching device and connects to each of the memory/device address and data lines in the processor system. The module is required when more than two M1502 Bus Output Interface Modules are included in the system. Each G720 can match impedance for up to 30 M1502 modules.

Refer to the General Interfacing Techniques for M7341 Processor Module application note for additional information.

2.4.11 G772 Power Connector Module

The G772 module is used to connect the dc power from a power supply to the KMP02 System Unit. Three solder terminals are mounted on the module to connect the leads from the power supply. The G772 module occupies one slot in the KMP02 System Unit, and the dc power to the system modules is distributed by the KMP02 backplane.

Refer to the Installation Section of this manual for additional information on the G772 module connections.

2.4.12 KC341-B Monitor/Control Panel

The KC341-B panel is used with the programming system to enter address information and data into the processor and to monitor the processor status and register contents. The control panel connects to the M7341 Processor Module by a cable and receives power from the G772 Power Connector Module.

Refer to the MPS Microprocessor Series User's Handbook for detailed control panel functions.

2.4.13 KMP02 System Unit

The KMP02 System Unit provides mounting for the MPS Development System modules and consists of six H803 Connector Blocks and three H8030 Connector Blocks mounted onto an H034 Double System Unit Mounting Frame. The KMP02 provides 54 slots for the MPS plug-in logic modules, cable connectors, bus terminators, and user-specified modules. The KMP02 has a prewired backplane capable of accepting all modules for the basic processor system and recommended expansion. Fourteen spare slots are available for the

user to mount additional plug-in modules. These slots are bused for M Series modules power and ground connections and can be wire wrapped for signal distribution by the user. The KMP02 is provided with four standoff posts for mounting to a panel and with pre-tapped holes in the mounting frame for installation in the H909-A or H909-BA enclosure.

For detailed information on the KMP02 connector blocks and mounting frame, refer to the DIGITAL Hardware/Accessories Catalog.

2.4.14 H909-A and H909-BA Mounting Box Enclosures

The H909-A and H909-BA are enclosures designed to provide mounting for the KMP02 System Unit and power supply. These enclosures can be installed in a standard 19-inch (48.26 cm) rack or cabinet or positioned as a free-standing table-top unit. Chassis slides are available for mounting to the H909-A or H909-BA.

The H909-A also includes space for mounting the DIGITAL recommended 2S-140T Powertec power supply and associated mounting plate or other suitable power supplies selected by the customer. The H909-BA includes a DIGITAL H755 Power Supply and an ac power cord with a BC05H (115 Vac) or BC05J (230 Vac) Line Set.

Refer to the 1975-76 DIGITAL Logic Handbook and the DIGITAL Hardware/Accessories Catalog for detailed descriptions of the H909-A and H909-BA and items included with these enclosures.

2.4.15 BC05W, BC05Y, and BC07D Cables

The BC05W and BC05Y cable assemblies transfer signals and power, respectively, to the KC341-B Monitor/Control Panel from the programming system. The BC05W is a 4-foot, 50-conductor, shielded cable with identical 50-pin connectors attached on each end. The BC05Y cable consists of three leads terminating at a G772 Power Connector Module. The opposite end has three Faston(TM) female terminals that mate with the power terminals on the KC341-B control panel.

The BC07D cables transfer control signals and data between the customer devices and the interface modules. The BC07D consists of two 20-conductor, flat ribbon cables with H856 Connector mounted on one end. The opposite cable end is not terminated. Other types of interfacing cables available from DIGITAL include the following:

Cable*	Description
BC04Z-XX	40-Conductor, flat cable (H856 to open end)
BC07A-XX	20-Conductor twisted pair (H856 to open end)

*-XX indicates desired cable length in feet.

2.5 PROCESSOR SYSTEM OPERATION

General operation of an MPS Processor System involves receiving input data from a user's device, performing specified programmed operations on the data, and providing appropriate outputs to external devices as a result of the processor decisions. Figure 2-1 shows the data, address, and control signal paths between the modules of a basic and expanded MPS Processor System.

2.5.1 Input Data Transfers

Input data transfers from an external device to the processor system are controlled by interrupts initiated by a device or by input instructions from the processor program.

During interrupt controlled transfers, the device should place an 8-bit word and a Data Ready control signal on the interface cable to the M1501 Bus Input Interface Module. The Data Ready signal produces an interrupt request signal from the M1501 module. The interrupt signal, inverted by the M111 module, is applied to the M7346 External Event Detection Module where the interrupt priority is determined. When the interrupt request is recognized, the M7346 produces an 8-bit octal code that interrupts the current processor program and jumps to one of eight dedicated memory locations. The processor then initiates a service routine stored at the address specified by the selected memory location. Under program control, when an INP instruction is executed, the address of the device requesting service is transferred from memory to memory/device address and data bus. The M7328 decodes the device address and produces a Data In signal to the appropriate M1501 module. The Data In signal gates the input data into the M7341 Processor Module and to the accumulator through the Data In bus, and clears the Data Ready flag in the M1501 module.

During a noninterrupt data transfer, the address of the specified device from memory is decoded by the M7328 module to produce a Data In signal. Any existing data from a device at the M1501 input interface will be transferred to the M7341 Processor Module and will appear in the accumulator.

2.5.2 Input Interface Timing

Figure 2-2 shows the relationship of the input data and control signals used to transfer the 8-bit parallel data into the processor. The input data must be stable on the lines a minimum of 50 ns prior to the Data Ready signal generated by the external device. The Data Ready signal is a positive transition and must remain high for a minimum of 50 ns. This signal sets the Interrupt Request flag in the M1501, which is reset when the data is transferred by the decoded Data In signal from the processor.

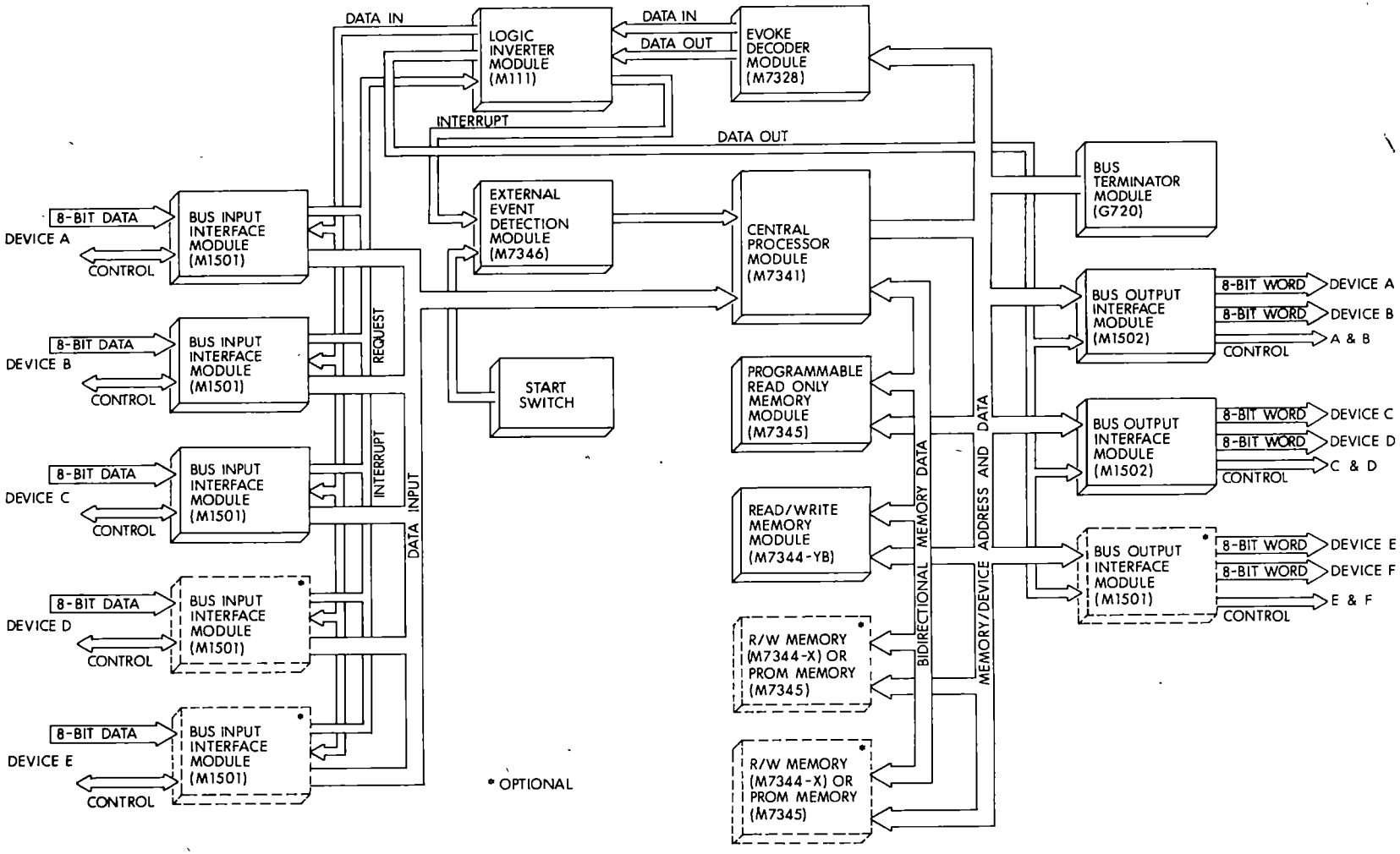


Figure 2-1. Processor System Block and Signal Flow Diagram

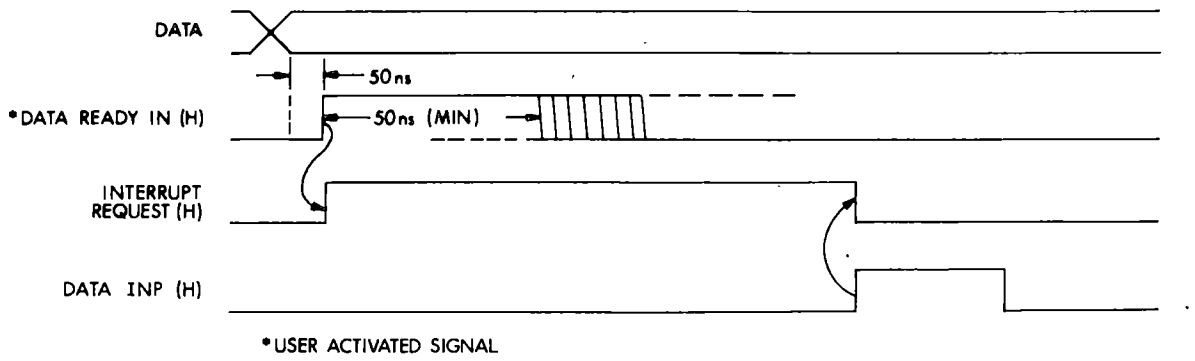


Figure 2-2. Input Data and Control Signal Timing

2.5.3 Output Data Transfers

Data transfers from the processor system to a peripheral device are controlled by the M7341 Processor Module during output instructions. During an output instruction, the address of the device to which the data will be transferred is placed on the memory/device address and data bus from memory. The M7328 module decodes the address and produces a Data Out signal on one of the six assigned Data Out lines. The signal is inverted by the M111 module and applied to the proper M1502 Bus Output Interface Module to enable the output data transfer and to generate a Data Ready signal to the device. The output data from memory is transferred to the buffer register in the selected M1502 module. When the output device accepts the data stored in the M1502 module, it resets the Data Ready control line to inform the processor that the output data has been received.

During serial output data transfers from the M7341 to current loop devices, the serial data is transferred through a special line from the asynchronous transmitter/receiver on the M7341 module. The address information for serial data is not decoded by the M7328 module.

2.5.4 Output Interface Timing

The relationship of the output interface timing and control signals is shown on Figure 2-3. The 8-bit parallel output data is stable 50 ns before the positive transition of the decoded Data Out pulse from the processor. The Data Ready signal to the device occurs at the trailing edge of the Data Out signal. The Data Accepted signal, generated by the device when data is received, must be a positive transition for a minimum of 50 ns.

2.5.5 Serial I/O Data Transfer

The M7341 Processor Module contains a universal asynchronous receiver/transmitter (UART) to interface with serial I/O devices requiring a 20 mA current loop or with TTL

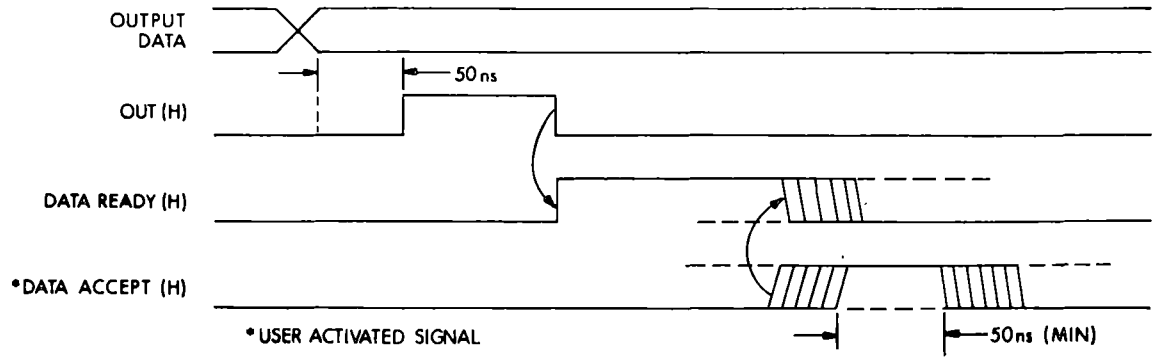


Figure 2-3. Output Data and Control Signal Timing

devices. The maximum data transfer rate is 9600 baud for TTL lines and 4800 baud for current loop lines. Data transfers to and from the UART are controlled by input/output instructions.

Refer to the MPS Microprocessor Series User's Handbook for a complete description of UART operations and instructions.

2.6 PROGRAMMING SYSTEM OPERATION

Figure 2-4 shows the data and control signal paths between the modules. The programming system of the MPS Development System is designed to produce operating programs for the processor system. The programming system enables the user to assemble and edit the source programs that are used to efficiently perform the functions required. The source programs on paper tape are entered into the processor memory through the paper tape reader under control of the teletypewriter keyboard.

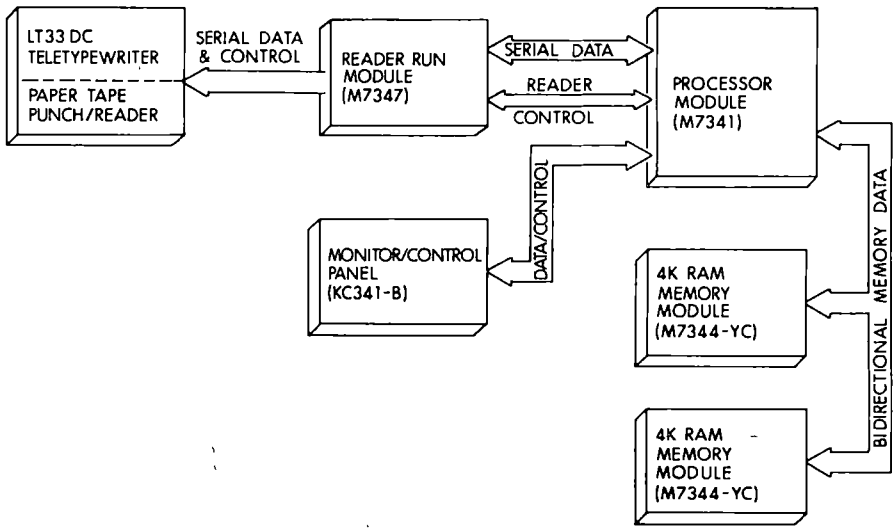


Figure 2-4. Programming System Block and Signal Flow Diagram

CHAPTER 3

ASSEMBLY AND INSTALLATION

The MPS Development System components are easily assembled and can be conveniently installed within existing or recommended enclosures or on mounting panels. Power for the system can be provided from a DIGITAL supply, from a DIGITAL recommended power supply, or from a customer system supply.

3.1 UNPACKING/INSPECTION

Carefully inspect all components shipped as part of the Development System to check for conformance to the items ordered and to insure that no damage has been incurred during shipment. Notify the nearest DIGITAL sales office immediately if items are missing, or the carrier if damage to the items is evident.

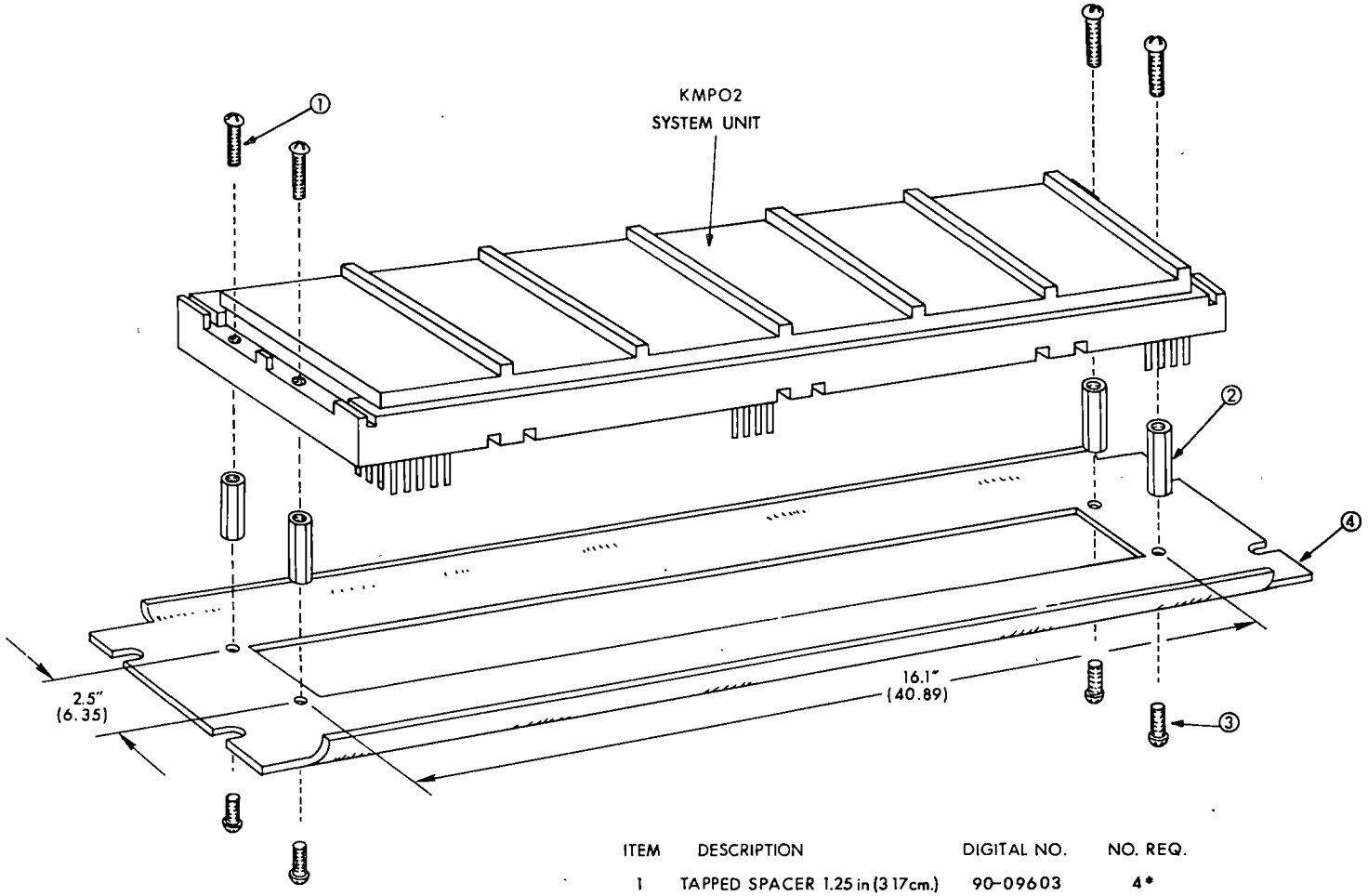
3.2 KMP02 SYSTEM UNIT MOUNTING

The KMP02 System Unit is supplied with four standoff posts to facilitate attachment to a chassis or panel. Three tapped holes in the H034 Mounting Frame of the KMP02 allow the system unit to be secured in the DIGITAL H909-A or H909-BA enclosure or other suitable customer-supplied enclosure. The H034 Mounting Frame also contains a series of tapped and nontapped holes to allow the user to mount the KMP02 in any suitable unit.

Refer to the DIGITAL Hardware/Accessories Catalog for detailed hole sizes and dimensions.

3.2.1 Panel Installation

The KMP02 System Unit can be mounted to any H014 panel or to a similar panel or chassis by drilling four holes in alignment with the standoff post provided with the KMP02. Refer to Figure 3-1 for the mounting hole dimensions. The H014 panel permits the unit to be installed in a 19-inch (48.26 cm) rack or cabinet.



ITEM	DESCRIPTION	DIGITAL NO.	NO. REQ.
1	TAPPED SPACER 1.25 in (3 17cm.)	90-09603	4*
2	SCREW 8-32×1 (2 54 cm)	90-6043-1	4*
3	SCREW 8-32×1/4 (.635 cm.)	90-6035-1	4
4	PANEL	HO14	1**
*	SUPPLIED WITH KMPO2		
**	OPTIONAL FOR 19.0 in. RACK MOUNTING		

Figure 3-1. KMP02 Panel Mounting and Hole Dimensions

3.2.2 H909-A and H909-BA Enclosure Installation

The KMP02 System Unit is designed for mounting within the H909-A or H909-BA enclosure. The metal frame (H034) of the KMP02 is provided with three tapped holes that align with three predrilled holes in the base of the H909-A or H909-BA enclosure and two tapped holes on the edge of the frame that align with the two mounting brackets in the enclosure. Refer to Figure 3-2 for the position of the KMP02 within the enclosure and for the hardware required. Prior to mounting the KMP02 System Unit in the H909-A or H909-BA, remove the four standoff posts mounted in the KMP02 metal frame.

3.3 POWER SUPPLY INSTALLATION

Two power supplies are recommended for use with the MPS Development System. The H909-BA enclosure, available from DIGITAL, is equipped with an H755 Power Supply which provides the required voltages and current for the complete MPS system configuration. The 2S-140T power supply can be purchased by the customer from Powertec, Inc. or a Powertec distributor, and mounted within an H909-A enclosure or on a suitable panel or chassis. When the 2S-140T is mounted within the H909-A enclosure, a special mounting plate adapter is available from DIGITAL to compensate for the mounting hole locations on the supply and enclosure.

In addition to these power supplies, the customer may use dc power available from an existing system or from other purchased supplies, provided the specified current capacity and voltage regulations are maintained.

3.3.1 Power Supply Selection

The following power supply specifications are required for the dc power to the MPS system:

Voltage/Current:	+5 Vdc @ 15.0 A, -15 Vdc @ 1.5 A
Regulation:	+5 Vdc (±5%), -15 Vdc (±2%)
Ripple:	+5 Vdc (50 mV P-P), -15 Vdc (5 mV P-P)
Overvoltage Protection:	+5 Vdc

The current requirements of the basic and expanded processor system are listed in Table 3-1. The H909-BA enclosure with the H755 Power Supply is recommended for expanded systems using all available I/O interface modules and more than a total of 8K words of PROM or RAM memory.

When using the Powertec 2S-140T supply, the Powertec OVP-1 overvoltage protection module must be wired to the +5 Vdc output.

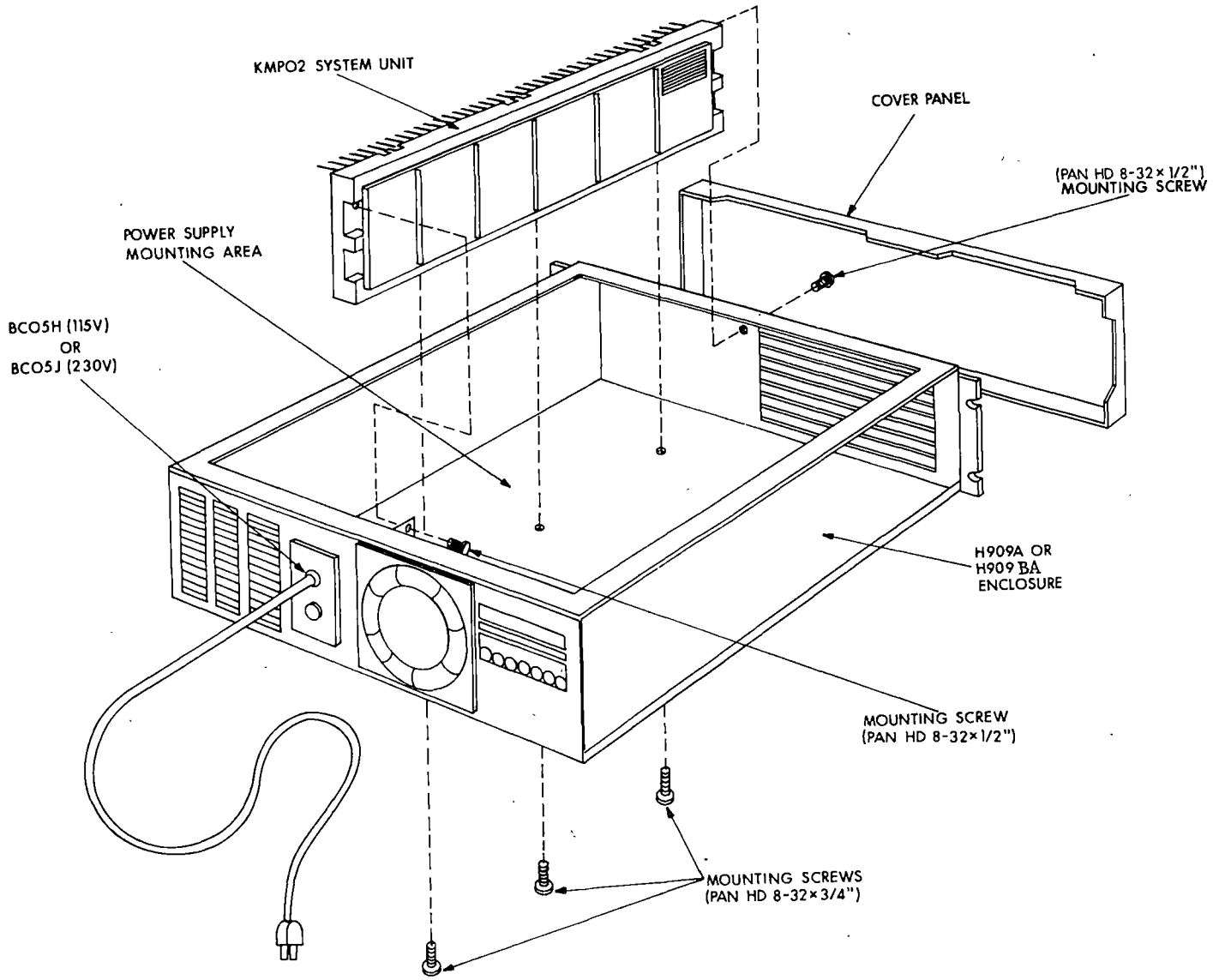


Figure 3-2. KMP02 Mounting in H909-A or H909-BA Enclosure

Table 3-1

System Module Power Requirements

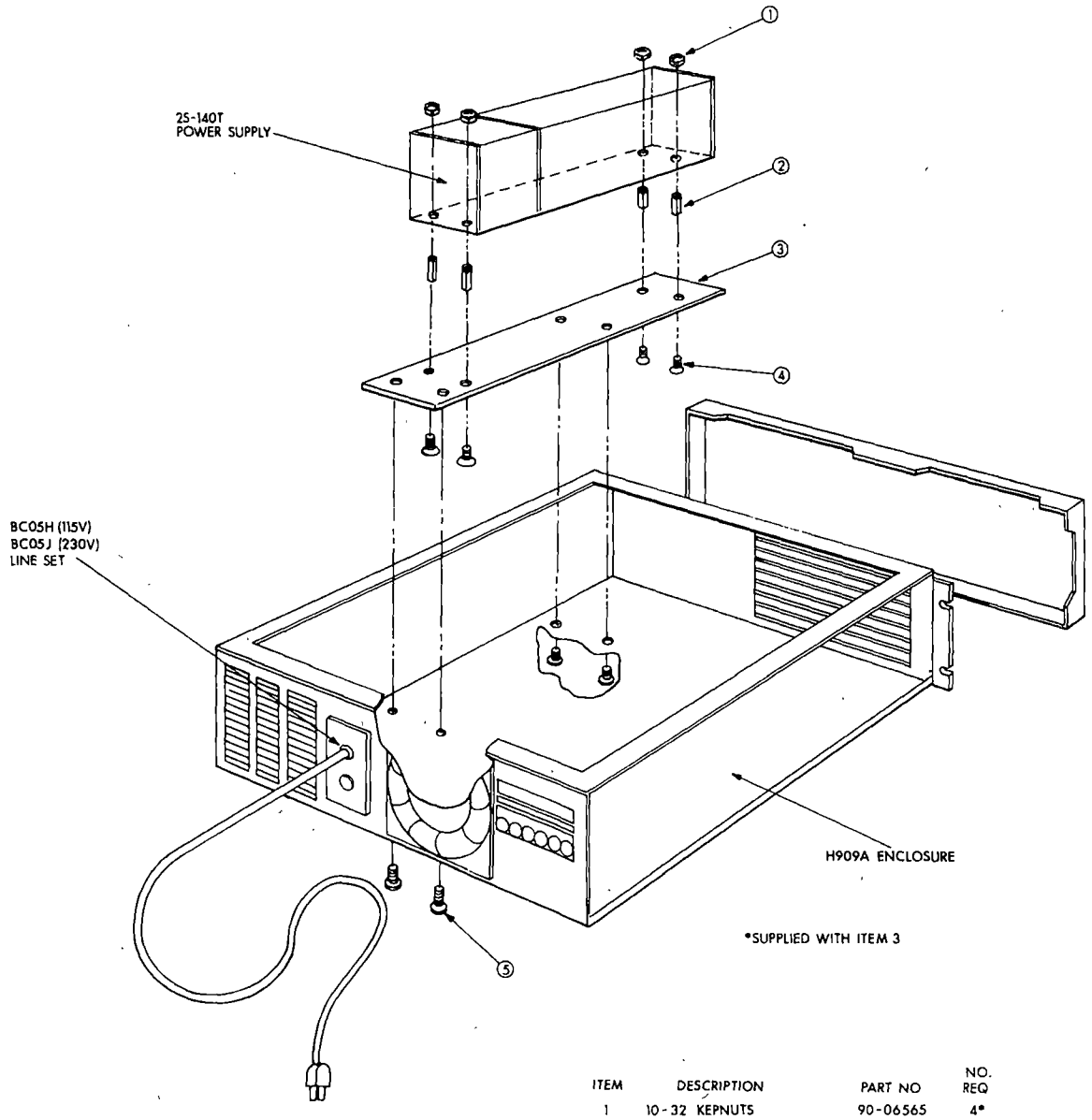
Module Type	+5 Vdc	-15 Vdc	6.3 Vac
Basic Processor System			
M7341	1.6 A	150 mA	
M7345 (1K PROM)	.49 A	300 mA	
M7344-YB	1.5 A		
M7346	.25 A		50 mA
M7328	.30 A		
M111	.08 A		
M1501 (3)	.90 A		
M1502 (2)	1.5 A		
G720	.15 A		
Total	6.77 A	450 mA	50 mA
Expansion Modules			
Additional 3K on M7345	.51 A	700 mA	
Full complement of M7344-YC	6.6 A		
M1501 (2)	.6 A		
M1502 (1)	.75 A		
Total	8.46 A	700 mA	-
Total Power (Basic and Expansion)	15.23 A	1145 mA	50 mA
M7347 (used with programming system only)	140 A	13 mA	

3.3.2 Power Supply Mounting

When the MPS Development System is not installed within the H909-A or H909-BA, the power supply can be attached to any one of several mounting panels or frames available from DIGITAL. Refer to the DIGITAL Hardware/Accessories Catalog for the hardware available.

3.3.2.1 2S-140T Power Supply Mounting in H909-A

The 2S-140T Powertec power supply can be installed in the H909-A enclosure using the mounting plate adapter and screws supplied by DIGITAL. The mounting plate is secured to the enclosure in the position shown on Figure 3-3, using the specified hardware.



ITEM	DESCRIPTION	PART NO	NO. REQ
1	10-32 KEPNUTS	90-06565	4*
2	SPACER, HEX	90-06822	4*
3	MOUNTING PLATE		1
4	FLT HD SCREW 10-32 × 7/8	90-09422-2	4*
5	PAN HD SCREW 8-32 × 1	90-06043-1	4*

Figure 3-3. 2S-140T Power Supply Mounting in H909-A Enclosure

3.3.3 AC Power Wiring

The input ac power can be supplied from an existing system power controller or from an external ac outlet. In addition to supplying voltage to the power supply, ac is also required for the power supply cooling fans and for the ac power fail detection circuit of the M7346 External Event Detection Module. When the Powertec 2S-140T power supply is used, a 115 Vac cord and fused terminal board must be supplied by the customer. If the 2S-140T is to be mounted within the H909-A enclosure, the BC05H (115 Vac) Line Set is available from DIGITAL and includes an external six-foot, 115 Vac cord with a three-prong male plug and a 7 A circuit breaker. The BC05H Line Set mounts in the opening provided in the rear of the H909-A enclosure. The H909-BA enclosure includes either a BC05H (115 Vac) or BC05J (230 Vac) Line Set, as required by the user. Figure 3-4 is a typical ac wiring schematic for the MPS Development System using the H909-A.

When the ac power fail function of the M7346 module is desired, a 6.3 Vac transformer is required. The input ac to the 6.3 Vac transformer can be supplied from the fused output of the BC05H Line Set or from a separate 115 V line input.

3.3.4 DC Power Wiring

The dc power from the power supply is distributed to the KMP02 System Unit through a power cable and G772 Power Connector Module. The G772 module plugs into one of the two designated slots in the KMP02, and power is distributed to the modules through busing strips presoldered to the pins of the KMP02 backplane. The cable from the power supply is attached to the G772 by soldering the leads to the lugs, as shown on Figure 3-5. Use the wire size specified for each of the dc connections:

+5 V. . . . . #12 gauge (red)
-15 V. . . . . #16 gauge (blue)
GND . . . . . #10 gauge (black)

Figure 3-5 also lists the voltage distributed by each pin on the G772 connector module.

3.4 KC341-B MONITOR/CONTROL PANEL MOUNTING

The KC341-B unit has rubber bumpers attached to the back of the panel to allow the unit to be positioned horizontally on a table. When the bumpers are removed, the panel can be easily mounted to a panel for vertical installation into a cabinet or rack. Figure 3-6 shows the dimensions and hole locations for panel mounting. The four 6-32 screws that secure the rubber bumpers to the KC341-B can also be used to attach the unit to a mounting panel.

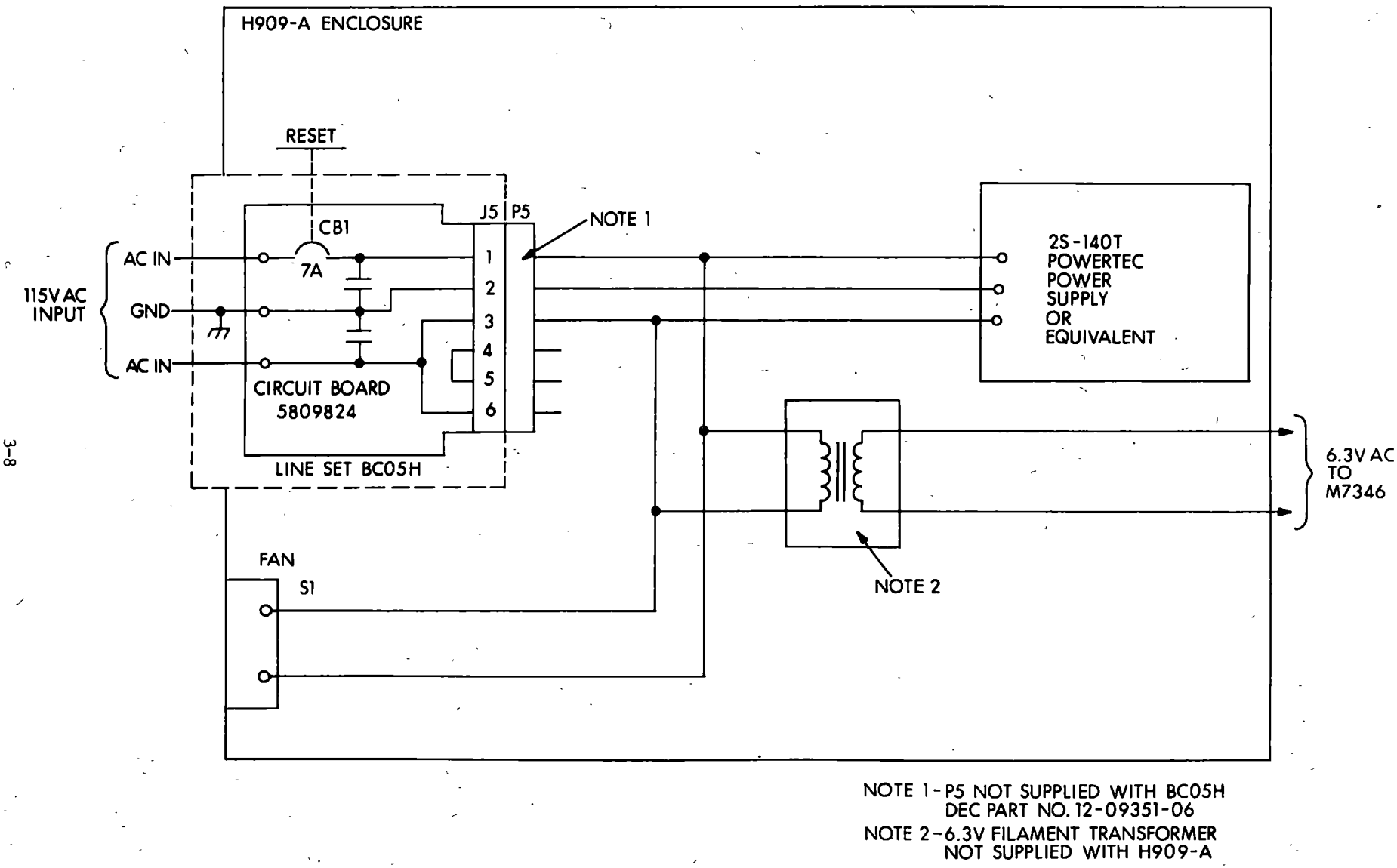
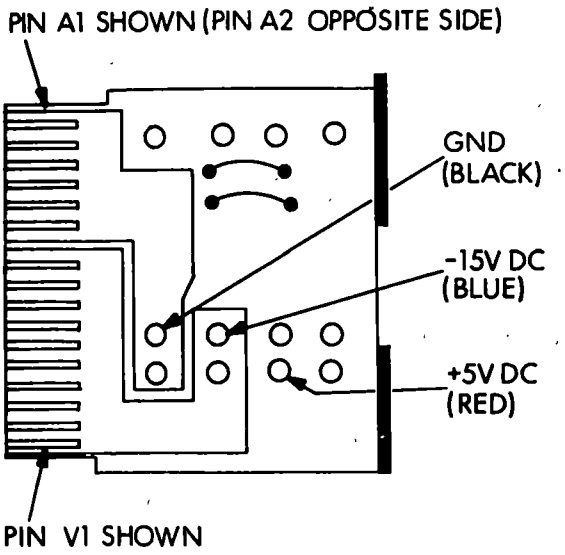


Figure 3-4. H909-A Enclosure Typical AC Wiring Diagram



PIN	POWER	PIN	POWER
A1	- 15 V	L 1	- 15 V
A2	+ 5 V	L 2	+ 5 V
B 1	- 15 V	M1	- 15 V
B 2	- 15 V	M2	+ 5 V
C 1	- 15 V	N1	GND
C2	GND	P 1	GND
D1	- 15 V	R 1	GND
D2	GND	S 1	GND
E 1	-15 V	T 1	GND
E2	GND	U 1	GND
F 1	- 15 V	V 1	GND
F2	GND		
H1	- 15 V		
H2	+ 5 V		
J 1	- 15 V		
J 2	+ 5 V		
K 1	- 15 V		
K2	+ 5 V		

Figure 3-5. G772 Module Power Lead Connections

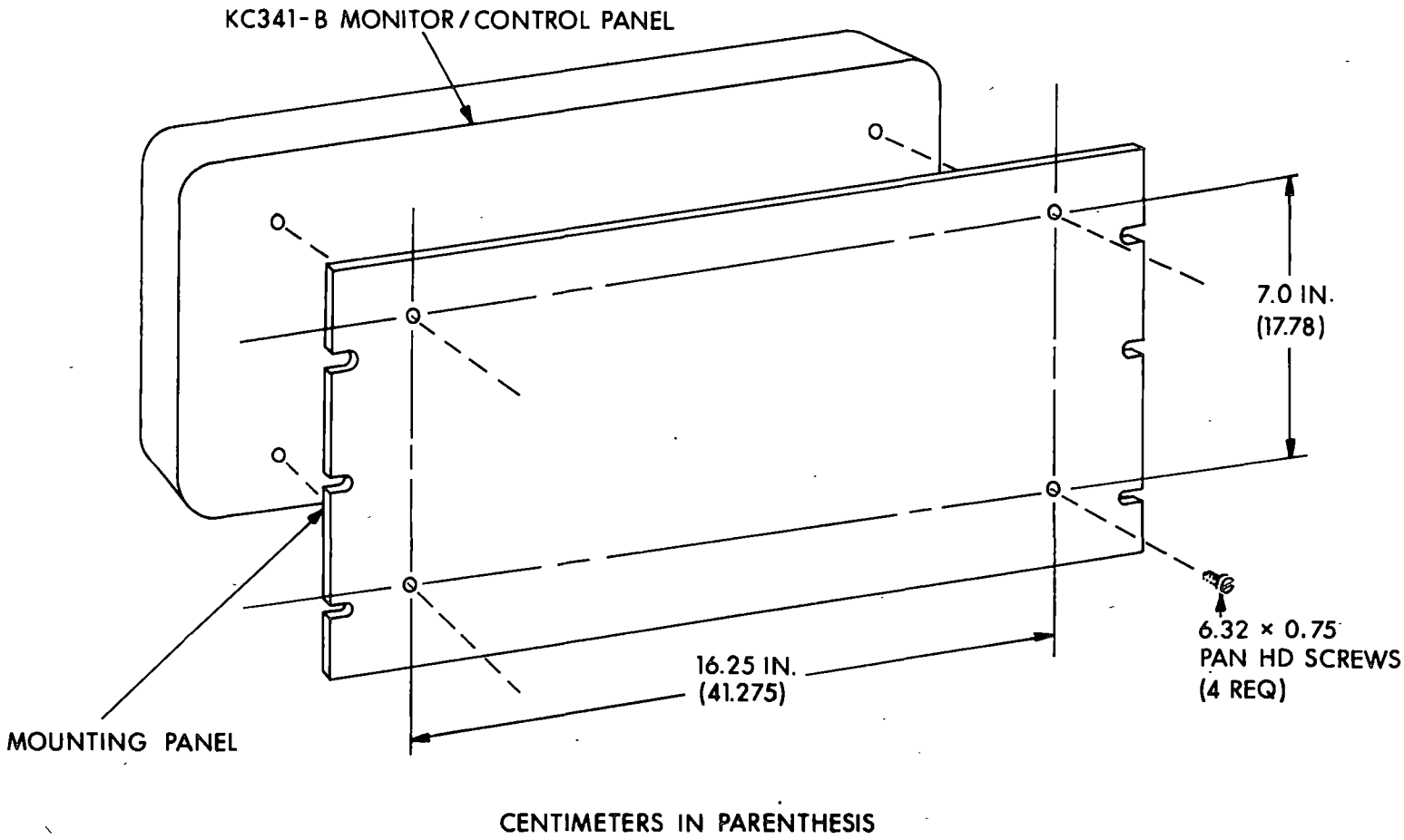


Figure 3-6. KC341-B Mounting Panel Hole Dimensions

3.5 MODULE AND CONNECTOR INSTALLATION

The modules and connectors provided with the programming or processor system insert into specific slots of the KMP02 System Unit. After the KMP02 is properly mounted in the H909-A or H909-BA enclosure or on a mounting chassis or panel, perform the following adjustments and insert the modules into the appropriate slots.

3.5.1 KMP02 Slot Designations

Each location within the KMP02 is assigned a row and slot designation. Figure 3-7 shows the position of the modules and connectors in a fully configured KMP02 System Unit.

Each of the connector blocks mounted to the H034 frame has a module keying ridge in the center and on one end of the block. To properly orient the KMP02 System Unit for module insertion, the connector block ridge closest to the H034 mounting frame is designated the F row, as shown on Figure 3-7. The opposite end, without a connector block ridge close to the frame, is designated row A, as shown. After the KMP02 is properly oriented, the slot designations from 1 to 9 are assigned as indicated.

3.5.2 Connector Pin Assignments

The wire wrap connector pins on the backplane of the KMP02 are marked and identified as shown on Figure 3-8. Each connector slot has 36 wire wrap pins that are assigned a row, slot, and pin designation. Once the row and slot have been determined, the pin is specified by an alphanumeric character (S2, B1, etc.).

3.5.3 Start Switch Wiring

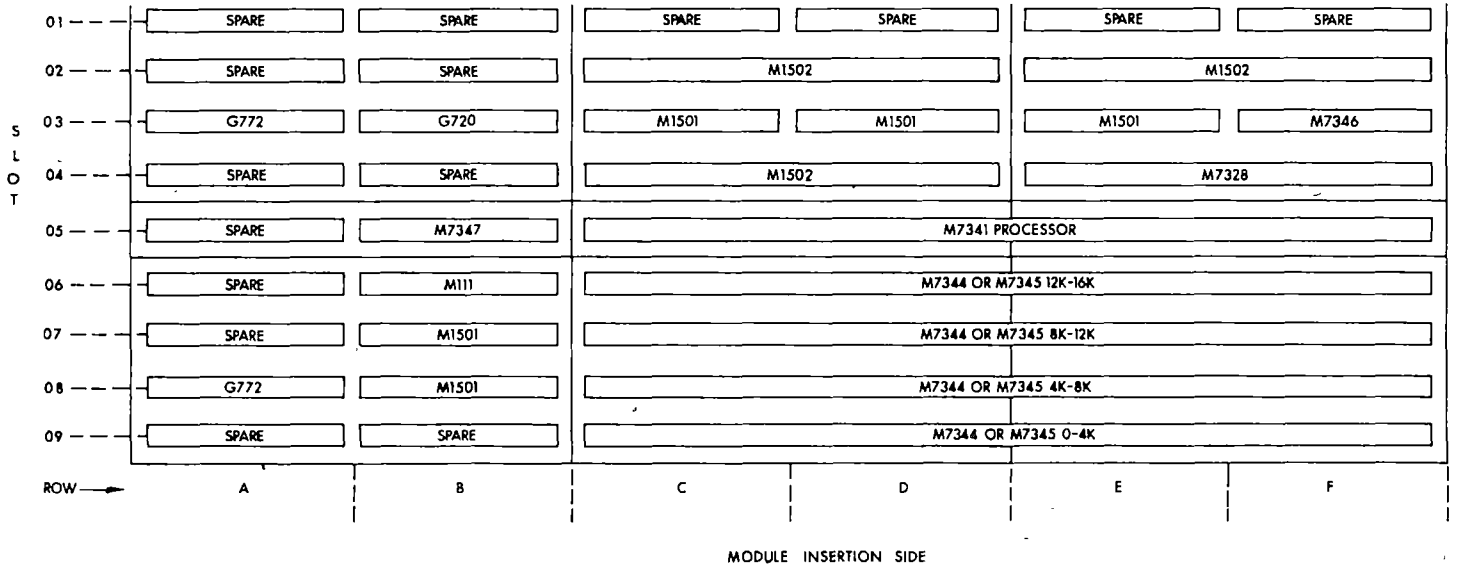
The external start switch can be installed on the same panel used to mount the MPS Development System or at any convenient location. A 5/16-inch clearance hole is required to install the switch. The associated wires are soldered at the switch and can be wire wrapped or soldered to slip on terminals which connect to the designated pins on the backplane of the KMP02 System Unit. One of the wires from the switch connects to wire wrap pin F03 D2. The remaining wire connects to pin D05 C2 or any equivalent signal ground on the backplane.

3.5.4 DC Power Checkout Procedure

After the ac wiring to the power supply has been implemented and the dc cable is connected to the G772 module, perform the following procedures to insure the proper distribution of power to the KMP02.

NOTE

Do not insert any modules in KMP02 before the checkout procedures have been performed. A VTVM or digital voltmeter is required.



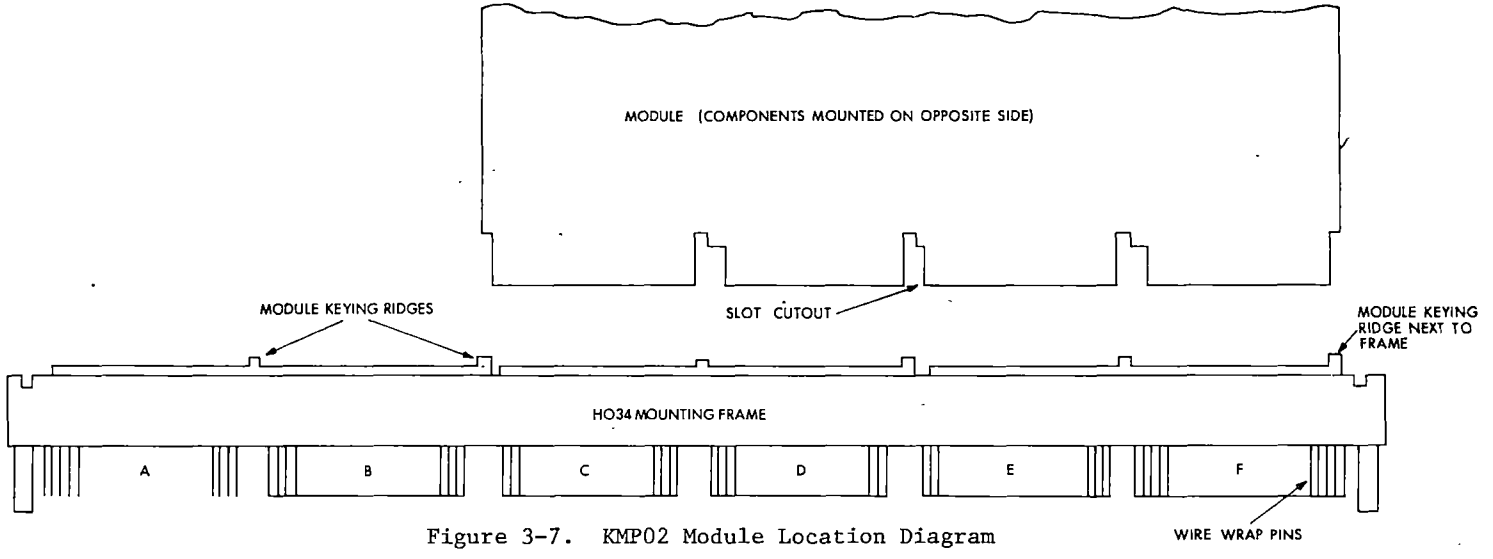


Figure 3-7. KMP02 Module Location Diagram

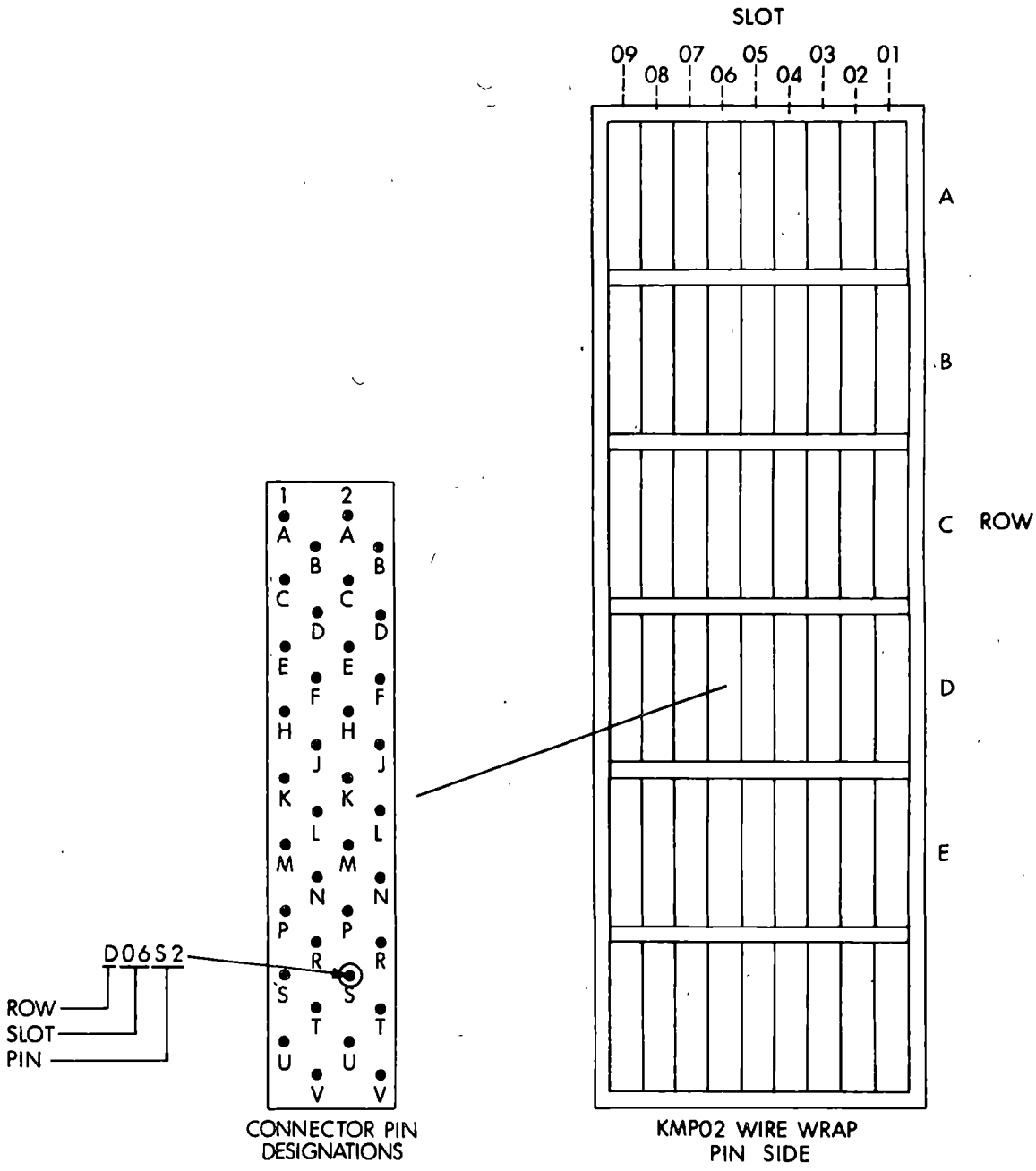


Figure 3-8. KMP02 Wire Wrap Pin Designations

a. Apply ac power to the power supply.

b. Measure the dc output voltages of the power supply at the appropriate terminals.

c. Measure the dc output voltages at the appropriate terminals of the G772 connector. Refer to Figure 3-5 for pin designations and voltage values. Reference all voltages to the ground connections on the G772 connector module.

d. Remove the ac voltage from the input to the power supply.

e. Insert the G772 connector module into slot A03 of the KMP02.

f. Apply the input ac voltage to the power supply and monitor the voltage present on the following pins of all slots in the KMP02 (Table 3-2).

Table 3-2
DC Voltage/Pin Designation

Voltage	Module Height		
	Single	Double	Quad
+5 V	A2	A2	AA2, BA2, CA2, DA2
-15 V			AB2
GND	C2, T1	C2, T1	AC2, AC1, BC2, BC1, CC2, CC1, DC2, DC1

3.5.5 Module Installation

Table 3-3 lists the modules that are available with the MPS system and identifies the location of the module in the KMP02 System Unit. Fifteen of the 54 slots are available for customer-supplied modules. These slots are prebused for power and ground, but must be wire wrapped for signal transfer. When modules are installed in spare slots of the KMP02, the total current capacity of the power supply must not be exceeded.

Figure 3-7 shows the orientation of a quad-height module for insertion into the KMP02. With the KMP02 in the position shown, the components on the module will be located on the opposite side.

CAUTION

Before inserting any module in the KMP02, be sure that the ridges on the connector blocks are properly aligned with the deepest section of the cutout slots in the module. Do not use excessive force to insert the modules. When properly aligned, the modules can be inserted with nominal pressure.

Table 3-3

KMP02 Module Locations

Module Type	Slots/Module	Slot Designations
G720	1	B03
G772	1	A03
G772	1	A08
M111	1	B06
M1501	1	B07
M1501	1	B08
M1501	1	E03
*M1501	1	C03
*M1501	1	D03
M1502	2	C02, D02
M1502	2	C04, D04
*M1502	2	E02, F02
M7328	2	E04, F04
M7341	4	C05, D05, E05, F05
M7344 or M7345 (12-16K)	4	C09, D09, E09, F09
*M7344 or M7345 (8-12K)	4	C08, D08, E08, F08
*M7344 or M7345 (4-8K)	4	C07, D07, E07, F07
M7344 (0-4K)	4	C06, D06, E06, F06
Spare		A01, B01, C01, D01, E01, F01, A02, B02, A04, B04, A05, A06, A07, A09, B09

*Optional modules.

Before inserting the M7341 Processor Module and the M7346 External Event Detection Module, insure that the following specified adjustments have been made to conform to the operating system.

3.5.5.1 M7341 Processor Module Switch Selection

The M7341 module is equipped with a switch bank consisting of eight dual-in-line (DIP) rocker switches used to select the characteristic serial I/O interface. The switch bank occupies one IC socket and is located in either of the two positions shown on Figure 3-9, depending on the module revision. When shipped, the DIP switches are preset for the serial I/O configuration listed in Table 3-4.

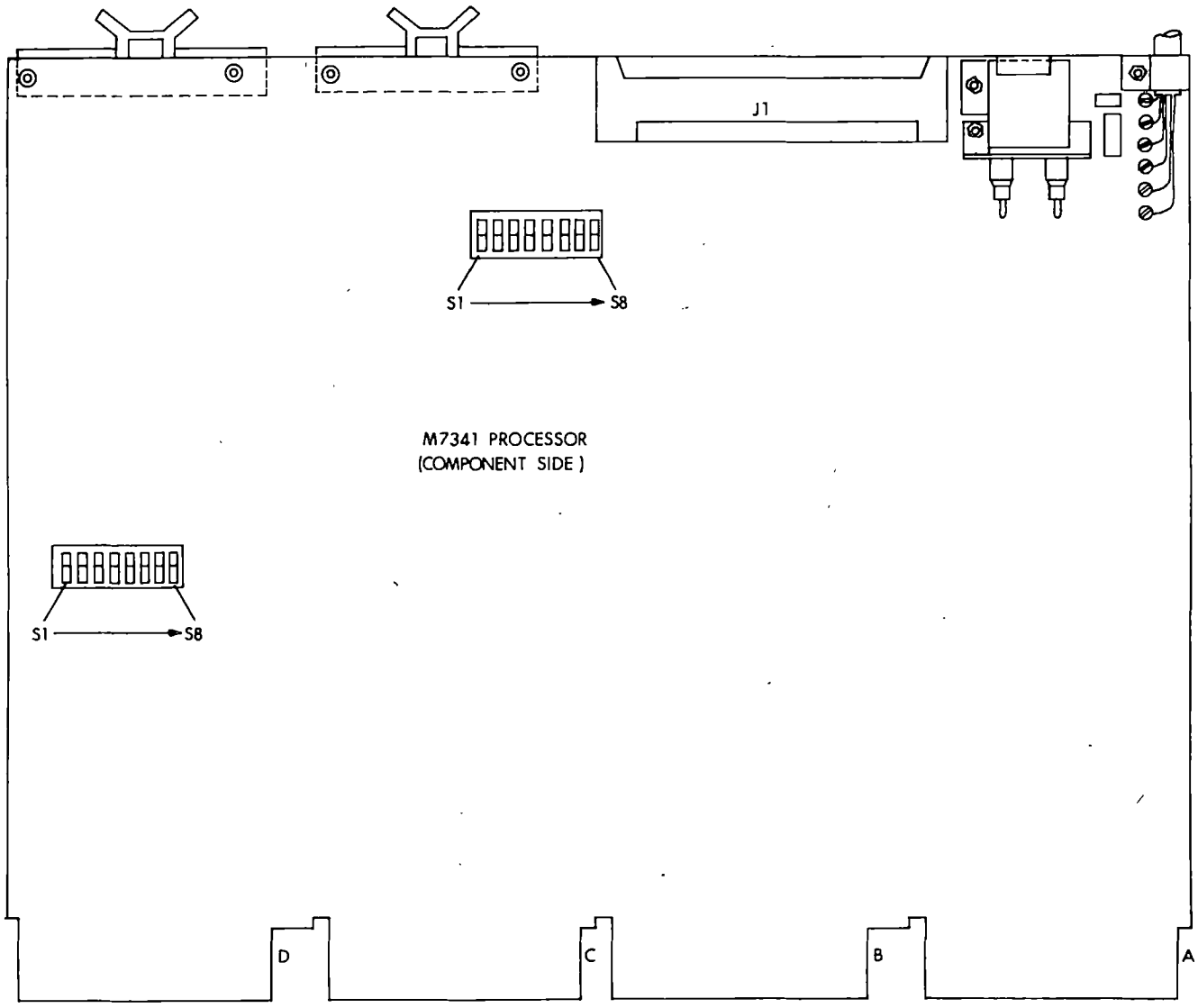


Figure 3-9. M7341 Serial I/O Switch Locations

Table 3-4

M7341 Serial I/O Switch Settings

Switch/Position	Function	Selected
S1/ON	Receiver clock	Internal, 110 baud
S2/ON	Transmitter clock	Internal, 110 baud
S3/OFF	Stop bits	Two stop bits for each data transmission word
S4/OFF S5/OFF	Mode	Active mode for receive and transmit
S6/ON	Receiver/transmitter select logic	Enabled
S7/ON	Test	Normal operation
S8	Not Used	

The MPS Development System is designed to operate with the switches set to the indicated positions. Operation of the system with other functions selected is not specified. Refer to the M7341 Processor Module data sheet for additional I/O configurations available.

CAUTION

If serial I/O communications problems are evident with the MPS system, visually check the switches to insure proper settings. To change switch positions, remove the clear plastic cover over switches and set switches S1 through S7. Switch S8 is not used. Replace plastic cover over switches after adjustment.

3.5.5.2 M7346 Power Fail Detector Timing

The ac power fail detection circuit on the M7346 module generates a 5 ms pulse, 35 ms after a low ac voltage condition is detected. Both the 35 ms delay and the 5 ms output pulse width are produced by one-shots mounted on the module.

Timing can be varied by changing the value of capacitance controlling the one-shot circuits. Capacitor C12 (Figure 3-10) on the M7346 board is the timing capacitor for the 35 ms one-shot, and C11 times the 5 ms one-shot. To change the timing, remove C11 and/or C12 and solder the replacement capacitors across the appropriate split lug pairs, noting that the positive (+) side of the capacitors are to be soldered to the plus (+) lugs. The value of the replacement timing capacitor to produce a given pulse width is determined by the following formula. For detailed information on the M7346, refer to the 1975-76 DIGITAL Logic Handbook listed in Table 1-1.

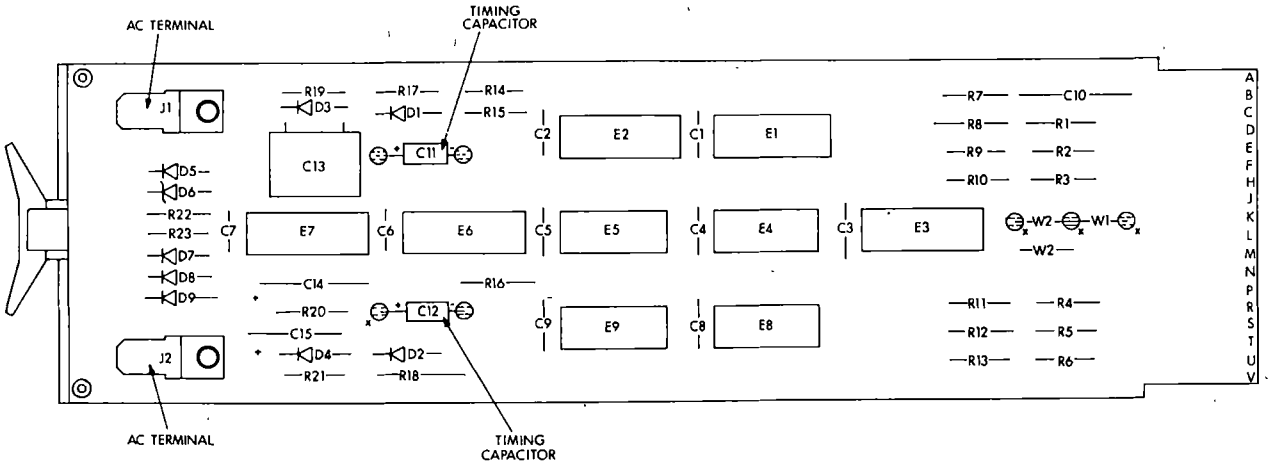


Figure 3-10. M7346 Timing Capacitor Locations

$$Tpw = 0.32\ R_T C_{EXT}\left(1 + \frac{0.7}{R_T}\right)$$

Where: Tpw = selected pulse width in nanoseconds

R_T = resistance in kilohms (R_T = 20K when computing C11 value. R_T = 33K when computing C12 value).

C_{EXT} = required capacitance in picofarads (pF)

3.5.5.3 Memory Configuration

The M7344 and M7345 memory modules are inserted into adjacent slot locations on the KMP02 System Unit. The slot locations are indicated on Figure 3-7 and are assigned as follows:

1st 4K	Slot 9, Row C - F
2nd 4K	Slot 8, Row C - F
3rd 4K	Slot 7, Row C - F
4th 4K	Slot 6, Row C - F

All memory modules included with a system are inserted into the KMP02 starting with the lowest position indicated (0 - 4K) and proceeding to the next highest (4K - 6K), etc. When a memory module contains less than 4K and another memory module is also used, the vacant memory address locations must be considered in the programming operation.

3.5.5.4 M1501 Interrupt Priority Assignment

Each of the designated slots in the KMP02 System Unit for the M1501 Bus Input Interface Modules has an associated interrupt request priority level assignment. When a peripheral device is cabled to the module, the priority of the interrupt request will be granted as follows. Refer to Figure 3-7 for the M1501 slot locations.

KMP02 Slot Designation	Priority Assignment
	1 (not wired)
D03	2 (highest)
C03	3
E03	4
B07	5
B08	6 (lowest)

3.6 SIGNAL DISTRIBUTION

All signal transfers within the processor system or programming system are implemented by the prewired backplane of the KMP02 System Unit. Signal transfers between the input and output devices, KC341-B Monitor/Control Panel, and LT33-DC Teletypewriter are through cables supplied with the MPS Development System or available from DIGITAL.

Figure 3-11 is a cabling diagram which locates and identifies all the necessary cables used with the system. Additional cable assemblies are available from DIGITAL in lengths specified by the customer. Refer to the 1975-76 DIGITAL Logic Handbook or the DIGITAL Hardware/Accessories Catalog listed in Table 1-1 for cable types available.

3.6.1 Processor System Cables

The basic processor system requires five BC07D-04 cables that are used to connect three input devices to the M1501 modules and two output devices to the M1502 modules. One cable end mates with the 40-pin connector mounted on the module edge and the other end can be terminated at the customer's device. Tables 3-5 and 3-6 list the signals and pin designations associated with the M1501 and M1502 interface modules. Figure 3-12 is a pin layout diagram for the cable and module input/output connectors.

3.6.2 Programming System Cables

The cables required with the programming system are supplied with the associated I/O devices. Refer to Figure 3-12 for the cable designations and connections.

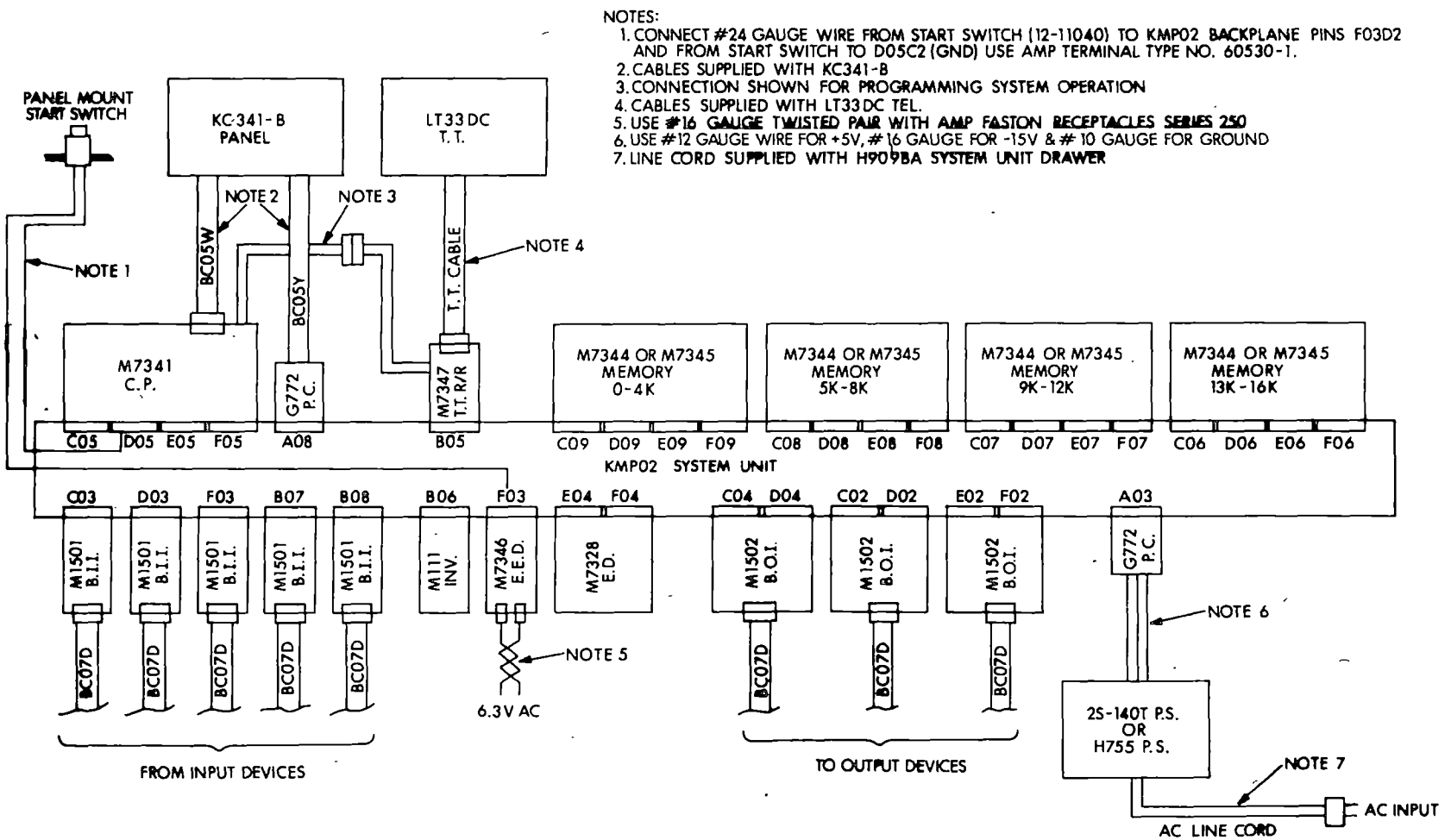


Figure 3-11. MPS Development System Cable Location Diagram

Table 3-5

M1501 Input Connector Pin Assignments

Pin*	Signal	Loading (TTL Unit Loads)
Y	GROUND	
Z	DATA ACC H OUT**	8**
W	GROUND	
X	DATA RDY H IN	1
CC	GROUND	
DD	BIT 7 MSB IN	1
EE	GROUND	
FF	BIT 6 IN	1
HH	GROUND	
JJ	BIT 5 IN	1
KK	GROUND	
LL	BIT 4 IN	1
MM	GROUND	
NN	BIT 3 IN	1
PP	GROUND	
RR	BIT 2 IN	1
SS	GROUND	
TT	BIT 1 IN	1
UU	GROUND	
VV	BIT 0 LSB IN	1

*Pins A through V, Y, Z, and pins AA and BB are not used.

**Drive capability of output signal to device.

Table 3-6

M1502 Output Connector Pin Assignments

Pin	Signal	Drive Capability (TTL Unit Loads)
A	GROUND	
B	BIT 7 MSB OUT	20
C	GROUND	
D	BIT 6 OUT	20
E	GROUND	
F	BIT 5 OUT	20
H	GROUND	
J	BIT 4 OUT	20
K	GROUND	
L	BIT 3 OUT	20
M	GROUND	
N	BIT 2 OUT	20
P	GROUND	
R	BIT 1 OUT	20
S	GROUND	
T	BIT 0 LSB OUT	20
U	GROUND	
V	NOT USED	
W	GROUND	
X	DATA RDY OUT	30
Y	GROUND	
Z	DATA ACC IN*	1*
AA	GROUND	
BB	NOT USED	
CC	GROUND	
DD	BIT 7 MSB OUT	20

*Input signal from device to processor.

(Continued)

Table 3-6 (Continued)

M1502 Output Connector Pin Assignments

Pin	Signal	Drive Capability (TTL Unit Loads)
EE	GROUND	
FF	BIT 6 OUT	20
HH	GROUND	
JJ	BIT 5 OUT	20
KK	GROUND	
LL	BIT 4 OUT	20
MM	GROUND	
NN	BIT 3 OUT	20
PP	GROUND	
RR	BIT 2 OUT	20
SS	GROUND	
TT	BIT 1 OUT	20
UU	GROUND	
VV	BIT 0 LSB OUT	20

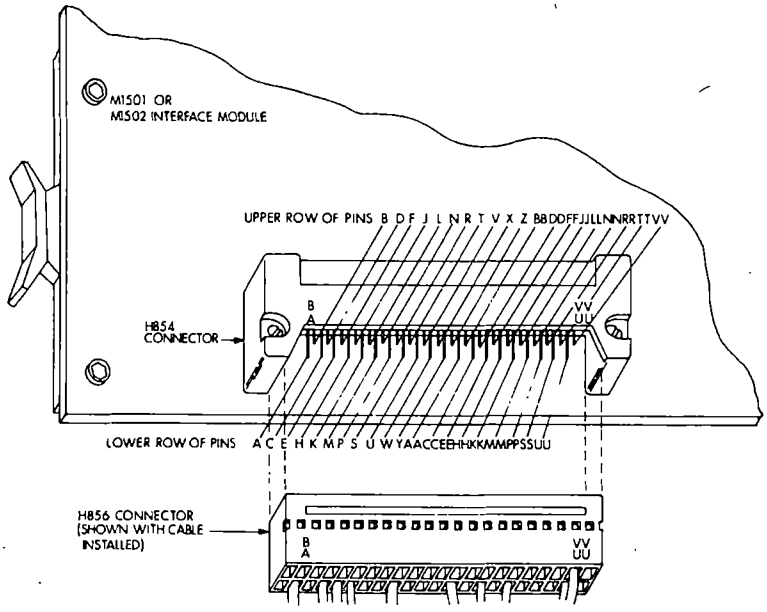


Figure 3-12. Input/Output Connector Pin Layout

3.6.3 KC341-B Control Panel Cables

Data and control signals are transferred between the KC341-B control panel and the M7341 Processor Module through the BC05W, 50-conductor, flat ribbon cable. The cable is supplied with the panel and has mating 50-pin connectors on each end.

The dc power and ground to the KC341-B is supplied by a BC05Y cable. Power is derived from the KMP02 System Unit through the G772 power connector.

3.6.4 LT33-DC Teletypewriter Connections

The LT33-DC signal cable attaches to the mating connector mounted on the M7347 Paper Tape Reader-Run Module. The M7347 is provided with an attached cable and connector which mates with the serial I/O cable on the M7341 Processor Module.

When an ASR33 Teletype terminal (or equivalent) is used with the MPS system, an ASR Teletype Conversion Kit is available from DIGITAL to interface the unit to the M7347 module. Refer to Appendix for interfacing information.

CHAPTER 4

OPERATION AND PROGRAMMING

Operating programs for the processor system are developed using the programming system and the QY500-AB Software Package or with a PDP-8 computer system and the QF500-AB Software Package. This section contains the information necessary to test the operation and functions of both the processor and programming systems and to produce basic data storage and control programs for customer applications. References to detailed programming information contained in other MPS documents are also included.

4.1 KC341-B MONITOR/CONTROL PANEL OPERATION

The KC341-B Monitor/Control Panel provides on-line control and program diagnostic capability for the programming system. The KC341-B performs the following functions:

- Enter Address Data
- Enter Operating Data
- Display Address Data
- Display Operating Data
- Display Processor Status
- Control Processor Status

4.1.1 Control Panel Switches and Indicators

Figure 4-1 shows the switches and indicators on the front panel of the unit. The vertical row of indicators displays the machine states and status of the processor. The upper horizontal row of switches and indicators is used to enter memory addresses or data bytes and to display the contents of the specified address. The lower row of switches provides control of the processor operations. Table 4-1 lists the function of the switches and indicators on the panel.

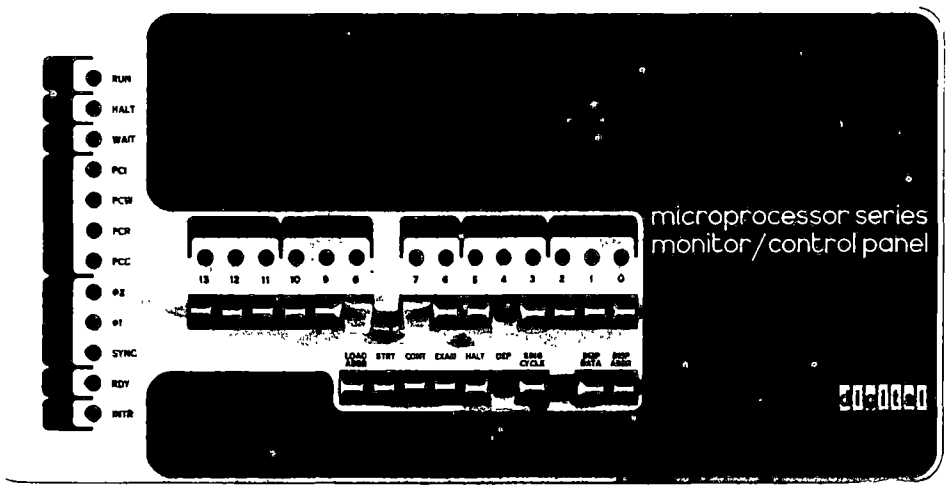


Figure 4-1. KC341-B Panel, Switches, and Indicators

Table 4-1

KC341-B Switches and Indicators

Switch/Indicator	Function
0 - 13 (Data/Address Switches)	Two position switches of the panel switch register used to enter data and address information when the processor is in the HALT state. Offset Address: Switches 0 - 7 enter three address octal digits $000 - 377_8$ (0 = low order, 7 = high order) Block Address: Switches 8 - 13 enter two address octal digits $00 - 77_8$ (8 = low order, 13 = high order) Data: Switches 0 - 7 enter data (0 = low order, 7 = high order)
0 - 13 (Data/Address Indicators)	Displays the current 14-bit octal address when the processor module is in the RUN state, or displays 8-bit memory data when using the EXAM or DISP DATA switches. Logical one's are indicated when LED's are lighted. Offset Address: Indicators 0 - 7 display offset address $000 - 377_8$. Block Address: Indicators 8 - 13 display block address $00 - 77_8$. Data: Indicators 0 - 7 display data.

Table 4-1 (Continued)

KC341-B Switches and Indicators

Switch/Indicator	Function
LOAD ADDR (Load Address Switch)	A momentary-action switch which loads the 14-bit address entered by the Data/Address switches 0 - 13 into the processor memory address buffer register. The next operation, initiated by the processor, will be executed using the memory address selected.
STRT (Start Switch)	A momentary-action switch which starts normal processor operation when the HALT switch is in the run-enable (down) position. Program execution starts at the current memory address. The HALT indicator turns off and the RUN indicator is lighted, indicating the Run mode. The Run mode continues until the HALT switch is again raised or until a HLT instruction is executed.
SING CYCLE (Single Cycle Switch) CONT (Continue Switch)	The SING CYCLE and CONT switches enable program execution on the processor module's memory address bus on a cycle-by-cycle basis. The SING CYCLE switch must be in the down (single cycle) position and the HALT switch must be in the down (run-enable) position. Each cycle is then initiated by pressing the momentary-action CONT switch, causing processor time state TS3 to be entered. The processor then executes the cycle and stops, as indicated by lighting the WAIT indicator. The 14-bit address of the next memory byte is displayed and the PCI, PCW, PCR, or PCC indicator displays the identity of the next machine cycle to be executed. The 8-bit contents of the addressed location may be displayed by pressing the DISP DATA switch. The up position of the SING CYCLE switch selects normal operation.
DEP (Deposit Switch)	A momentary-action switch which is raised to load switch register data into the memory location currently addressed by the processor memory address buffer. Sequential memory locations may be loaded by entering new data into the switch register for the next location to be loaded and raising the DEP switch. The memory address is automatically incremented to the next address for successive DEP switch operations. (See the DISP DATA and DISP ADDR switch descriptions.)

Table 4-1 (Continued)

KC341-B Switches and Indicators

Switch/Indicator	Function
EXAM (Examine Switch)	A momentary-action switch which is pressed to examine (read) the contents of the location currently addressed by the processor memory address buffer. The memory data obtained is displayed on the Data/Address indicators 0 - 7. The memory address is automatically incremented to the next address for successive EXAM switch operations. Currently displayed data may be altered by entering the desired data into the Data/Address switches and by raising the DEP switch. The new data is loaded into the same memory location where the altered data was obtained. Pressing EXAM will then cause the new data (at the same location) to be displayed. The next location is then examined by simply pressing EXAM. (See the DISP ADDR switch description.)
HALT (Switch)	Selects the run-enable Halt mode of the processor. In the up position, the processor is in the Halt mode, and the HALT indicator is lighted. When in this position, the switch enables the LOAD ADDR, EXAM, DEP, and switch register functions. In the down position, the processor is in the run-enable mode. The HALT indicator is turned off when the program execution is started until the processor is halted by the HALT switch or by executing a HLT instruction. When in the run-enable position, the switch enables the STRT, SING CYCLE, and CONT switches, and the Address/Data indicators display the current memory address.
DISP DATA (Display Data Switch)	A momentary-action switch which is pressed to examine the contents of the current location when using the DEP or SING CYCLE switch functions.
DISP ADDR (Display Address Switch)	A momentary-action switch which is pressed to display the current address when using the DEP or EXAM switch functions.
RUN (Indicator)	Lights to indicate a program is being executed in the processor. (Refer to STRT switch function.)

Table 4-1 (Continued)
KC341-B Switches and Indicators

Switch/Indicator	Function
HALT (Indicator)	Lights to indicate that the processor is in the Halt mode. (Refer to HALT switch function.)
WAIT (Indicator)	Lights to indicate that the processor is in a Wait condition between machine cycles TS2 and TS3. (Refer to SING CYCLE and CONT switch functions.)
PCI (Indicator)	Lights during the first cycle of each instruction.
PCW (Indicator)	Lights during the processor cycle when memory is addressed and data is written into the addressed location.
PCR (Indicator)	Lights during the retrieval of data from memory.
PCC (Indicator)	Lights during an I/O instruction when a device is addressed and data is transferred.
$\phi 1$, $\phi 2'$ (Phase Indicators)	Light to indicate the presence of two-phase clock signals in the processor module.
SYNC (Indicator)	Lights to indicate the processor SYNC signal is being generated.
RDY (Ready Indicator)	Lights to indicate the RDY H signal is true, enabling processor module operation. When the RDY H signal is false, the processor module remains in the Wait state until the signal is again asserted.
INTR (Interrupt Indicator)	Lights to indicate that the INTR H signal is in the true state during an interrupt request at the processor. If interrupts are enabled, the processor will service the request.

4.1.2 Address Notation and Operating Data Selection

Both address notation and operating data entered or monitored by the Data/Address switches and indicators on the KC341-B Monitor/Control Panel are represented in octal notation. Figure 4-2 shows the octal assignments for address information and data.

Switches 0 - 7 select the desired offset for the address information and also the complete 8-bit data byte from $000 - 377_8$. Switches 8 - 13 are used to select the desired block number of the address. Block numbers may range from $00 - 77_8$.

4.1.3 Control Panel Functions

Load Address - The load address function permits the manual insertion of a 14-bit memory address through the switch register to deposit data in the location accessed or examine its contents. Once an address has been loaded, it is displayed automatically.

Deposit - The deposit function permits an 8-bit data byte to be written into the memory location by setting switches 0 - 7 and raising the deposit switch. The data is automatically displayed in indicators 0 - 7.

Examine - The examine function permits the examination of the contents of that location accessed by the MPS address bus. The contents of this location are displayed in the Address/Data display by pressing the EXAM switch.

Start - The start function permits the execution of a program at any location within that program by inserting the address of the desired memory location in the switch register and pressing the STRT switch. This address may be, for example, the starting location of the bootstrap routine contained in the front panel PROM resident memory.

Single Cycle and Continue - These functions permit the examination, on a cycle-by-cycle basis, of the MPS memory address bus and the bidirectional data port contents. Pressing the SING CYCLE switch grounds the RDY (ready) line to the MPS, causing the processor to enter the Wait state and the WAIT indicator to light.

Halt - The halt function permits a user to halt operations of the processor module by a single-switch action. The HALT switch must be operated to perform such panel functions as load, address, examine, or deposit.

Display Data - The display data function is used while operating the MPS in the Single Cycle mode. Each pressing of the CONT switch steps the program in a cycle-by-cycle manner. At the end of each cycle, the control panel lights display the memory location currently being addressed.

Display Address - The address currently being examined under an examine function can be displayed by pressing the DISP ADDR switch. The address location is displayed on panel indicator lights 0 - 13, where the switch is held down.

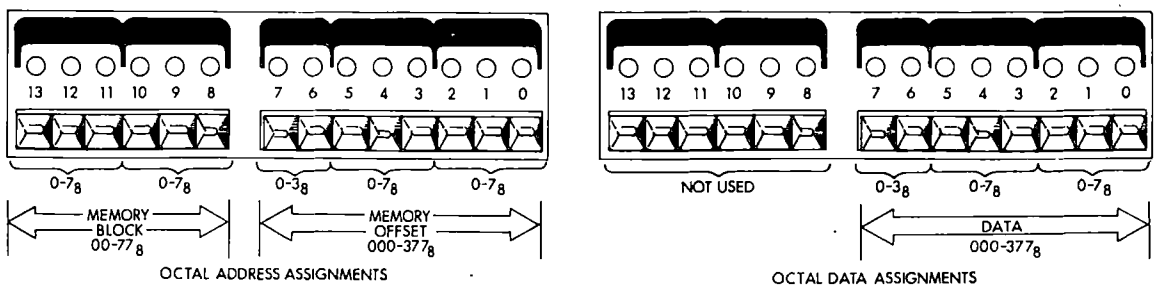


Figure 4-2. KC341-B Data/Address Switch Selections

4.2 LT33-DC TELETYPEWRITER OPERATION

The LT33-DC terminal contains a paper tape reader and punch used to read the assembler and editor programs on paper tape in the QY500-AB Software Package into the MPS programming system. The user programs are punched on paper tape for loading into the processor system. Detailed information on the LT33-DC operation is contained in the MPS Microprocessor Series User's Handbook. The LT33-DC is interfaced to the programming system through the M7347 Paper Tape Reader-Run Module.

4.3 PROM PROGRAMMING

The M7345 Programmable Read-Only Memory Module is supplied with PROM circuits to be programmed by the user. Each PROM circuit is equipped with a sealed, transparent quartz lid which permits erasure, using an ultraviolet light source, prior to reprogramming. PROM programming is accomplished through the use of a ROM (read-only memory) programmer which is run on a PDP-8 processor. The user interested in PROM programming should consult the MPS Microprocessor Series User's Handbook supplied with the system.

4.4 PROCESSOR SYSTEM CHECKOUT

Prior to entering the user programs into the processor system, the following checks will ensure the proper operation of the hardware and modules. An LT33-DC Teletypewriter or an equivalent terminal must be connected to the serial line input on the M7341 Processor Module. Refer to the terminal interconnection information in the Appendix of this guide for proper interfacing of the teletypewriter to the processor system.

4.4.1 Teletypewriter Check

1. Apply power to the processor system.
2. Set the teletypewriter switch to LINE (refer to MPS Microprocessor Series User's Handbook).

3. Check the RUN light on the M7341 module for an "ON" condition.

4. To verify the Run condition, press the STRT switch on the mounting panel or press the "C" key on the teletypewriter keyboard.

5. If the system is running, an asterisk (*) will be printed by the teletypewriter.

The system is now under control of the MDP program permanently written into the M7345 Programmable Read-Only Memory Module. MDP will allow the following actions to be performed:

1. Open specified memory locations so that the contents may be examined, verified, and modified, if necessary. The previous, current, and next locations may be opened, displayed, and closed.

2. Allow a program segment to execute for test purposes.

3. Specify breakpoint locations for test program execution.

4. Load specified memory locations with a constant value.

5. Display the contents of program addresses, status flip-flops, and index registers via the terminal.

6. Read and punch paper tape on the terminal.

The most basic application of MDP is in loading a basic sample program. Complete details on MDP are defined in Chapter 8 of the MPS Microprocessor Series User's Handbook.

4.4.2 2K Read/Write Memory Test

This test is performed after the teletypewriter check and is capable of detecting faults which may occur during system operation as a result of a hardware error. Additional checks on peripheral devices may be required for a more complete system test. The program is entered by the Microprocessor Debugging Program (MDP) stored in the M7345 4K PROM module.

The program runs in block 20, starting at address 20#0. When started, the program loads zeros (000) in memory locations 116 through 377 of block 20. We then recycle through the block just written and compare each location to zero to check that the data was written correctly. If no errors are detected, the process is repeated in the next block. After all blocks ($20 - 27_8$) have been written with zeros, the program is repeated with all ones (377_8) being written in each location. At the end of the second pass or on an error, control returns to MDP. If the test was successful, register C should contain 0. If register C contains 376 or 377, it indicates that an error occurred during pass one or pass two, respectively. Registers H, L will contain the address of the location in error.

Proceed as directed below:

1. Apply system power.
2. Turn terminal on. (Set teletype switch to LINE.)
3. System should be in a Run condition as indicated by the RUN light on the M7341 CPU module being lit.
4. Verify Run condition by:
   a. pressing switch button on H014 Mounting Panel; or
   b. pressing the CTRL and C keys simultaneously on the terminal keyboard.

   If the system is running, an asterisk will be printed or displayed by the terminal.
5. Enter the program as follows:
   a. Type 20#0/.
   b. MDP will respond with 3 digits indicating the current contents of location 20#0 and a space.
   c. Type 026 <LF>.
   d. MDP will respond by typing a carriage return, line feed, and 20 001/xxx.
   e. Type 376 <LF>.
   f. MDP will respond with a carriage return, line feed, and 20 002/xxx.
   g. Continue in this manner until you get to the last location, 20 071.
   h. Type 020 <CR>.
   i. MDP responds with carriage return, line feed, and an asterisk (*).
   j. The program may be listed by typing the following command:

      D 20#0; 20#71 <CR>

   k. MDP will list the contents of each location and finish with a <CR>, <LF>, *.
   l. When the program has been verified, type the following command:

      G 20#0 <CR>

   m. The program will begin execution and return control to MDP (indicated by a <CR>, <LF>, *) on completion of the test or an error condition.
   n. Type X <CR>.

o. MDP will respond with 20 111/xxx (contents of register A).

p. Type <LF>.

q. MDP will respond with 20 112/xxx (contents of register B).

r. Type <LF>.

s. MDP will respond with 20 113/xxx (contents of register C).

t. The contents of 20 113 should be 0 if the test was a success. If xxx is equal to 376 or 377, it means that an error was detected. Type <LF> twice to get the address of the location in error. MDP will respond with:

20 114/xxx (block)
20 115/xxx (offset)

The contents of 20 114 is the block number and 20 115 is the offset number.

Block 20 Offset	Machine Instruction or Data	Symbolic Instruction or Data	Remarks
0	026	BEG, LCI 376	/initial pass switch
1	376		
2	036	LDI A	/initial offset
3	116		
4	056	I, LHI A↑	/initial block number
5	020		
6	364	LLD	/set initial offset
7	016	G, LBI 0	/initial data
10	000		
11	371	B, LMB	/load memory
12	060	INL	/increment offset
13	110	JFZ B	/loop till end of current block
14	011		
15	020		
16	364	LLD	/reset offset
17	301	LAB	/load accumulator with data
20	277	C, CPM	/compare with memory
21	110	JFZ MDP	/exit to MDP on error
22	077		
23	000		
24	060	INL	/increment offset
25	110	JFZ C	/loop till end of current block
26	020		

Block 20 Offset	Machine Instruction or Data	Symbolic Instruction or Data		Remarks
27	020			
30	056		LHI I+1↑	/end of memory?
31	020			
32	066		LLI I+1	/set block number address in H, L
33	005			
34	006		LAI 27	/load accumulator with last block #
35	027			
36	277		CPM	/compare with current block #
37	110		JFZ D	/not equal, continue pass
40	062			
41	020			
42	076		LMI 20	/pass complete, reset block #
43	020			
44	066		LLI BEG+3	/reset offset
45	003			
46	076		LMI A	/to protect scratch area
47	116			
50	066		LLI G+1	/reset data
51	010			
52	020		INC	/end of second pass?
53	372		LMC	
54	150		JTZ MDP	/yes, exit to MDP
55	077			
56	000			
57	104		JMP I-2	/no, do pass two
60	002			
61	020			
62	347	D,	LEM	/increment block #
63	040		INE	
64	374		LME	
65	036		LDI 0	/reset offset
66	000			
67	104		JMP I	/continue pass
70	004			
71	020			

4.4.3 Sample I/O Program

Eight input interface instructions and ten output interface instructions are available to control the transfer of serial and parallel data to and from the processor system. Two sample programs are included for checking the I/O operations. The programs can be entered into memory by the LT33-DC Teletypewriter keyboard.

Input Interface Instructions - The following list shows the address, instruction, and function of each input instruction. When the processor receives an instruction, the data on the selected input is read into the processor accumulator.

Device Address	Instruction	Function
INO 0	INP 0	Read serial data (from UART)
INO 1	INP 1	Read status (from UART)
INO 2	INP 2	Read data from M1501 slot D03
INO 3	INP 3	Read data from M1501 slot C03
INO 4	INP 4	Read data from M1501 slot E03
INO 5*	INP 5	Read data from M1501 slot B07
INO 6*	INP 6	Read data from M1501 slot B08

*Optional M1501.

Example Input Program - The following program will input a ten-word block of data to memory. The starting address of the memory location for the block is 20 230.

Memory Block	Word Address	Instruction or Data	Instruction	Label	Comments
			*20#200		
20	200	056 020	LHI	BLK↑	/load address of /block to H and /L regs
20	202	066 230	LLI	BLK	
20	204	016 012	LBI	12	/set count to 10
20	206	105	AGIN, INP 2		/read A data word
20	207	370	LMA		/store it in block
20	210	060	INL		/increment pointer
20	211	011	DCB		/decrement pointer
20	212	110 206 020	JFZ	AGIN	/if not done, go back
20	215	000	HLT		

Memory Block	Word Address	Instruction or Data	Instruction	Label	Comments
			*20#230		
20	230	000	BLK	BLOCK 12	
		000			
		000			
		000			
		000			
		000			
		000			
		000			
		000			
		000			

Output Interface Instructions - The following list shows the address, instruction, and function of each output instruction. When the processor receives the instruction, data is transferred from the processor accumulator.

Device Address	Instruction	Function
OUT 00	OUT 0	Load data out to UART
OUT 01	ION	Enable interrupts
OUT 02	IOF	Disable interrupts
OUT 03	OUT 3	Load M1502 slot EF02 (low byte)
OUT 04	OUT 4	Load M1502 slot EF02 (high byte)
OUT 05	OUT 5	Load M1502 slot CD02 (low byte)
OUT 06	OUT 6	Load M1502 slot CD02 (high byte)
OUT 07*	OUT 7	Load M1502 slot CD04 (low byte)
OUT 10*	OUT 10	Load M1502 slot CD04 (high byte)

*Optional M1502.

Example Output Program - The following program will output a ten-word block of data from memory location 20 230 to 20 241.

Memory Block	Word Address	Instruction or Data	Instruction	Label	Comments
			*20#300		
20	300	056	LHI	BLK↑	/load address of
		020			/block to H and /L regs
20	302	066	LLI	BLK	
		230			
20	304	016	LBI	12	/set count to 10_{10}
		012			
20	306	307	NEXT, LAM		/load register from /memory

Memory Block	Word Address	Instruction or Data	Instruction	Label	Comments
20	307	131	OUT 5		/load output register
20	310	060	INL		/increment pointer
20	311	011	DCB		/decrement counter
20	312	110	JFZ NEXT		/if not done, go back
20	313	306			
20	314	020			
20	315	104	JMP 20#300		/load block again
20	316	300			
20	317	020			

4.4.4 Input/Output Interface Test

The following program tests the operation of the input (M1501) and output (M1502) interface modules by cycling data stored in memory through an output interface and into an input interface. The binary value of the data returned is compared with the data initially loaded into memory, and any errors are indicated by a teletypewriter printout. To execute the test, perform the following procedure:

1. Connect the test cable BC08R-1 between the output connector of the M1502 module in slots C02, D02 and the input connector of the M1501 module in slot D03.
2. Using the teletypewriter, preload the following program into memory starting at block 20#200. Enter a ten-word block of test data in the desired configuration starting at block 20#230.
3. Type "G" 20#200 on the keyboard to execute the program. When program stops, type D 20#242; 20#253 <CR>. The input data received by the system and stored in memory will be printed on the teletypewriter. The value of the printed data should equal the value of the ten-word block of data stored in location 20#230 through location 20#241.

Block 20 Offset	Machine Instruction or Data	Symbolic Instruction or Data	Remarks
		*20#200	/initialize origin
200	056	LHI OBLK†	/initial H register
201	020		
202	026	LCI OBLK	/initial C register to OUT data
203	230		
204	036	LDI IBLK	/initial D register to IN data
205	242		

Block 20 Offset	Machine Instruction or Data	Symbolic Instruction or Data	Remarks
206	016	LBI 12	/set counter for ten words
207	012		
210	362	NEXT, LLC	/set pointer to OUT data
211	307	LAM	/load data into accumulator
212	131	OUT5	/output data to M1502
213	363	LLD	/set pointer to IN data
214	105	INP2	/read data from M1502
215	370	LMA	/store in IN data block
216	020	INC	/increment pointers
217	030	IND	
220	011	DCB	/decrement counter
221	110	JFZ NEXT	/if not zero, get next word
222	210		
223	020		
224	104	JMP 100	/if zero, return to MDP
225	100		
226	000		
227	000	HLT	/dummy statement
230	XXX	OBLK, BLOCK 12	/ten-word block for output data
231	XXX		/to be entered at run time
232	XXX		
233	XXX		
234	XXX		
235	XXX		
236	XXX		
237	XXX		
240	XXX		
241	XXX		
242	XXX	IBLK, BLOCK 12	/ten-word block for input data
243	XXX		/should equal data entered
244	XXX		/in OBLK after execution
245	XXX		
246	XXX		
247	XXX		
250	XXX		
251	XXX		
252	XXX		
253	XXX		
254		$	/end-of-program indicator

4.4.5 Sample Arithmetic Program

This program performs a multiplication of two binary numbers from specified memory locations and stores the result in a separate memory location. The two numbers are loaded into general registers B and C, and register D is used to temporarily store results during the computation. Register E performs a count operation. The binary numbers are multiplied by a series of additions and shift operations.

The program is loaded into read/write memory starting at location 10000 (block 20 offset 0) using MDP (refer to the following listing). The first location is opened to enter the assembled code followed by a line feed. MDP will automatically open the next location. After the last location (block 20 offset 40) is entered, a carriage return is typed to return control to MDP. To run this program for different values, enter the multiplicand and the multiplier in locations block 20, offset 41 and 42. Program execution may be initiated by typing the GO command, G 20 0 <CR>. When the asterisk appears in the left margin, the operation is complete and the result will be found in location block 20 offset 43.

Block 20 Offset	Machine Instruction or Data	Symbolic Instruction or Data	Remarks
0	056	LHI ABLE↑	/get data in registers
1	020		
2	066	LLI ABLE	/for ease of operation
3	041		
4	317	LBM	/store 1st number in B
5	060	INL	
6	327	LCM	/store 2nd number in C
7	250	XRA	/clear accumulator and carry
10	330	LDA	/clear product
11	046	LEI -10	/set counter to -8_{10}
12	370		
13	301	M01, LAB	/load 1st number into accumulator
14	032	RAR	/rotate accumulator one bit right
15	310	LBA	/save rotated number in B
16	303	LAD	/load product into accumulator
17	100	JFC M02	/carry set?
20	024		
21	020		
22	240	NDA	/yes, clear carry
23	202	ADC	/add 2nd number
24	032	M02, RAR	/rotate product right one bit
25	330	LDA	/save product in D

Block 20 Offset	Machine Instruction or Data	Symbolic Instruction or Data	Remarks
26	040	INE	/increment counter
27	110	JFZ M01	/are we done?
30	013		
31	020		
32	301	LAB	/yes, get register B
33	032	RAR	/rotate if one bit to the right
34	060	INL	/increment memory pointer
35	370	LMA	/save result
36	104	JMP MDP	/return to MDP
37	077		
40	000		

4.5 PROGRAMMING SYSTEM CHECKOUT

After the KC341-B has been properly connected to the programming system, perform the following checkout procedures.

4.5.1 Control Panel Operation Test

This test verifies the correct operation of the 32-word, 8-bit read/write memory and the 256-word, 8-bit read-only memory located in the control panel (containing the Microprocessor Loader Program) have been verified.

1. Ensure that switches labeled 0 - 13 are off (down) and all function switches are up except DEP, which is normally down.
2. Observe that indicators ϕ1, ϕ2, SYNC and PCI are on (ϕ1, ϕ2, and SYNC remain on).
3. Set switches 0, 2, 4, 6, 8, 10, and 12 up.
4. Press the LOAD ADDR switch.
5. Observe that the corresponding switch indicators are lit (0, 2, 4, 6, 8, 10, 12).
6. Set switches 0, 2, 4, 6, 8, 10, and 12 down.
7. Repeat steps 4 and 5, substituting switches and indicators 1, 3, 5, 7, 9, 11, and 13.
8. Set switches 1, 3, 5, 7, 9, 11, and 13 down.
9. Set switches 8 - 13 up (address 77 000).
10. Press the LOAD ADDR switch.

11. Press the EXAM switch.

12. The switch indicator lights should display 00 125_8. Actuate the DISP ADDR switch to observe the address 77 000.

13. Repeat 11 and 12 above except observe 00 106_8 and address 77 001.

14. Repeat 11 and 12 above except observe 00 142_8 and address 77 002.

15. Repeat 11 and 12 above except observe 00 077_8 and address 77 003.

16. Repeat 11 and 12 above except observe 00 054_8 and address 77 004.

17. Set switches 8 through 13 down.

18. Set switches 9 through 13 and 5 through 7 up (address 76 340).

19. Press the LOAD ADDR switch.

20. Set switches 9 through 13 and 5 through 7 down.

21. Set switches 1 through 5 up (00 076).

22. Actuate the DEP switch.

23. Set switches 1 through 5 down.

24. Repeat 21 and 22 above except set switches 7, 5, 3, and 1 up (00 252).

25. Set switches 1, 3, 5, and 7 down.

26. Repeat 21 and 22 above except set switches 0 through 3 and 6 up (00 117).

27. Set switches 0, 1, 2, 3, and 6 down.

28. Repeat 18 and 19 above (load address 76 340).

29. Set HALT then SING CYCLE switches down.

30. Actuate STRT switch.

31. Observe that the INTR, RDY, WAIT, and PCI indicators are on. (ϕ1, ϕ2, and SYNC remain on continuously.)

32. Actuate the CONT switch.

33. Observe that the INTR and PCI indicators go off.

34. Observe that the PCR indicator is on.

35. Actuate the CONT switch six more times and observe the following (also actuate DISP DATA switch each time to observe the data):

    (a) PCR ON
    (b) PCI ON, PCR OFF
    (c) PCR ON, PCI OFF
    (d) PCW ON, PCR OFF
    (e) PCI ON, PCW OFF
    (f) PCC ON, PCI OFF

36. Set HALT and SING CYCLE switches up.

37. Repeat 9 and 10 (load address 77 000).

38. Set HALT switch down.

39. Actuate STRT switch.

40. Observe that the RUN indicator is on.

41. Set HALT switch up.

42. RUN indicator goes out.

43. End of test.

4.5.2 8K Read/Write Memory Test

This test will establish the ability of the control panel to properly address and deposit data in all blocks of the 8K x 8-bit read/write memory module. The program is entered through the KC341-B Control Panel.

The program runs in block 0, starting at address 014. When started, the program loads zeros (000) in memory locations 110 through 377. The program is then recycled through the block just written and compares each location to zero to check that the data was written correctly. If no errors are detected, the process is repeated for the next block. After all blocks ($0 - 37_8$) have been written with zeros, the program is repeated with all ones (377) being written in each location. If no errors are detected in this pass, the program halts at location 0#110. When an error is detected, the program halts at location 0#013. The address of the location that failed is contained in the following locations: the block number (N) is in location 0#021 and the offset is in location N#012. Location 0#024 contains the correct data, either 000 or 377. Location 0#046 contains the highest block number to be tested. Proceed as directed below:

1. Apply system power.

2. Set the HALT switch to the down position.

3. Set the switch register to all zeros (down). Press LOAD ADDRess.

4. Load the system checkout program by setting the switch register to an instruction or data value for each location as specified in the following listing, and momentarily raising the DEPosit switch. Repeat this operation for each data value or instruction in the program. The memory address is automatically incremented each time the DEP switch is raised. If desired, the program may be examined after it has been loaded by first repeating step 3 and then pressing EXAMine; each time EXAM is pressed, the memory address is automatically incremented. The contents of the memory locations are displayed in indicators 0 to 7 located above the switch register. A symbolic listing is included, enabling a better understanding of the program operation.

5. Run the program by starting the program at location 014, as follows:

   a. Set the switch register to 0#014. Press LOAD ADDR.

   b. Return the HALT switch to the run (up) position.

   c. Press STRT. The program will immediately start and then halt at a location, as displayed on the panel indicators. The displayed address should be 00 110, an indication of normal operation. If any fault occurs, the program halts at location 00 012. The address where the error occurred may be obtained by examining the contents of location 00 021 to determine the block number. Location 013 of that block will contain the offset of the address in memory that caused the failure.

The system checkout program should not be considered a system diagnostic program, although it is capable of detecting faults which could occur during system operation if the MPS had a persistent hardware error. Generally, if the MPS system is properly installed and this program is run without errors, the MPS portion of the system is fully operational. Additional checks on peripheral devices may be required for a more complete assurance test.

Block 20 Offset	Machine Instruction or Data	Symbolic Instruction or Data	Remarks
0	277	CPM	/compare memory to accumulator
1	110	JFZ E	/error if not zero
2	006		
3	000		
4	060	INL	/increment offset
5	007	RET	/return to location after RST
6	336	E, LDL	/error, save offset
7	066	LLI F	/get F offset into L
10	013		
11	373	LMD	/store offset of location in error
12	000	HLT	/program halts here on error
13	000	F, HLT	/stores offset of offending location
14	026	BEG, LCI 376	/initial pass switch
15	376		
16	036	LDI A	/initial starting offset
17	110		
20	056	I, LHI A↑	/initial starting block number
21	000		

Block 20 Offset	Machine Instruction or Data	Symbolic Instruction or Data	Remarks
22	363	LLD	/load offset
23	016	G, LBI 0	/initialize data
24	000		
25	371	B, LMB	/load memory
26	060	INL	/increment offset
27	110	JFZ B	/loop till end of current block
30	025		
31	000		
32	363	LLD	/reset offset for comparison
33	300	LAA	
34	301	C, LAB	/load accumulator with data
35	005	RST	/call compare memory subroutine
36	110	JFZ C	/loop till end of current block
37	034		
40	000		
41	056	LHI I+1+	/test for end of memory
42	000		
43	066	LLI I+1	/set block number address in H, L
44	021		
45	006	LAI 37	/load accumulator with last block
46	037		
47	277	CPM	/compare with current block #
50	110	JFZ D	/not equal, go to D
51	070		
52	000		
53	076	LMI 0	/pass complete, reset block #
54	000		
55	106	CAL H	/reset starting offset
56	100		
57	000		
60	020	INC	/end of first pass
61	150	JTZ K	/no
62	107		
63	000		
64	372	LMC	/yes, set data to all ones
65	104	JMP I-2	/do pass two
66	016		
67	000		

Block 20 Offset	Machine Instruction or Data	Symbolic Instruction or Data	Remarks
70	347	D, LEM	/increment block #
71	040	INE	
72	374	LME	/store new block #
73	036	LDI 0	/reset starting offset to zero
74	000		
75	104	JMP I	
76	020		
77	000		
100	066	H, LLI BEG+3	/reset starting offset to A
101	017		
102	076	LMI A	/to protect program
103	110		
104	066	LLI G+1	/set memory pointer to G+1
105	024		
106	007	RET	/return to instruction after CAL
107	372	K, LMC	/reset data to all zeros
110	000	A, HLT	/halt, end of test

APPENDIX A

SERIAL I/O TERMINAL CONNECTIONS

The M7341 Processor Module is equipped with a 20 mA current loop, full-duplex serial communication line operating at a rate of 110 baud. Data is transmitted to and from a terminal over this line. Digital Equipment Corporation terminals using serial communication lines are listed below:

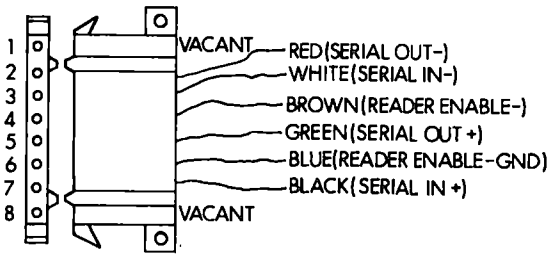
LT33-DC	Teletype Terminal	LA36	DECwriter II Terminal
VT05	Video Terminal	RT01	Data Entry Terminal
VT50	DECscope Video Terminal	RT02	Data Entry Terminal

LA30 DECwriter Terminal

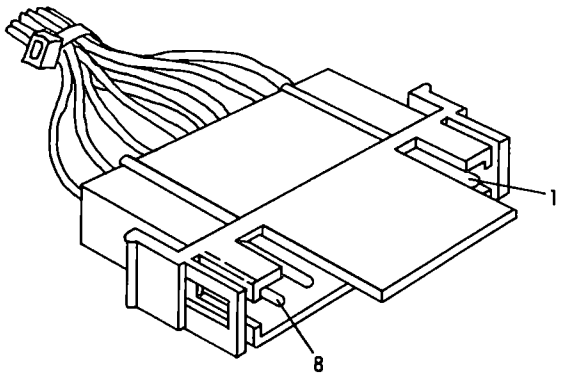
When an ASR-33 Teletype(TM) Console is used, a conversion kit is available to interface the terminal to the M7341 Processor Module: ASR-33 Teletype Kit, Part No. LT33-MB.

The communication line on the M7341 Processor Module is terminated in a female Mate-N-Lok connector carrying the following signals:

Pin 1 - Vacant
Pin 2 - Serial out, negative (red wire)
Pin 3 - Serial in, negative (white wire)
Pin 4 - Reader enable, negative (brown wire)
Pin 5 - Serial out, positive (green wire)
Pin 6 - Reader enable, ground (blue wire)
Pin 7 - Serial in, positive (black wire)
Pin 8 - Vacant



FEMALE MATE-N-LOK CONNECTOR



MALE MATE-N-LOK CONNECTOR

The terminal communicating with the M7341 Processor Module must be equipped with a corresponding male Mate-N-Lok connector and must supply at least the signals identified by the asterisk on the connector signal list.

APPENDIX B

BLOCK-OFFSET TO OCTAL CONVERSION

This appendix can be used to convert the block-offset notation in assembly language programs and output to octal notation. Only the first and last conversions are given for each block. To convert an offset within a given block, add the offset to the starting octal location in the block. For example:

Block	Offset	Octal
11	0	4400
.	.	.
.	.	.
.	.	.
11	377	4777

To convert block 11 offset 227 to octal, add 227 to 4400. The correct octal equivalent is 4627.

Block	Offset	Octal
0	000	0000
.	.	.
.	.	.
.	.	.
0	377	0377
1	0	0400
.	.	.
.	.	.
.	.	.
1	377	0777
2	0	1000
.	.	.
.	.	.
.	.	.
2	377	1377
3	0	1400
.	.	.
.	.	.
.	.	.
3	377	1777
4	0	2000
.	.	.
.	.	.
.	.	.
4	377	2377

Block	Offset	Octal
5	0	2400
.	.	.
.	.	.
.	.	.
5	377	2777
6	0	3000
.	.	.
.	.	.
.	.	.
6	377	3377
7	0	3400
.	.	.
.	.	.
.	.	.
7	377	3777
10	0	4000
.	.	.
.	.	.
.	.	.
10	377	4377

Block	Offset	Octal	Block	Offset	Octal
11	0	4400	23	0	11400
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
11	377	4777	23	377	11777
12	0	5000	24	0	12000
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
12	377	5377	24	377	12377
13	0	5400	25	0	12400
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
13	377	5777	25	377	12777
14	0	6000	26	0	13000
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
14	377	6377	26	377	13377
15	0	6400	27	0	13400
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
15	377	6777	27	377	13777
16	0	7000	30	0	14000
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
16	377	7377	30	377	14377
17	0	7400	31	0	14400
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
17	377	7777	31	377	14777
20	0	10000	32	0	15000
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
20	377	10377	32	377	15377
21	0	10400	33	0	15400
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
21	377	10777	33	377	15777
22	0	11000	34	0	16000
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
22	377	11377	34	377	16377

Block	Offset	Octal
35	0	16400
.	.	.
.	.	.
.	.	.
35	377	16777
36	0	17000
.	.	.
.	.	.
.	.	.
36	377	17377
37	0	17400
.	.	.
.	.	.
.	.	.
37	377	17777
40	0	20000
.	.	.
.	.	.
.	.	.
40	377	20377
41	0	20400
.	.	.
.	.	.
.	.	.
41	377	20777
42	0	21000
.	.	.
.	.	.
.	.	.
42	377	21377
43	0	21400
.	.	.
.	.	.
.	.	.
43	377	21777
44	0	22000
.	.	.
.	.	.
.	.	.
44	377	22377
45	0	22400
.	.	.
.	.	.
.	.	.
45	377	22777
46	0	23000
.	.	.
.	.	.
.	.	.
46	377	23377

Block	Offset	Octal
47	0	23400
.	.	.
.	.	.
.	.	.
47	377	23777
50	0	24000
.	.	.
.	.	.
.	.	.
50	377	24377
51	0	24400
.	.	.
.	.	.
.	.	.
51	377	24777
52	0	25000
.	.	.
.	.	.
.	.	.
52	377	25377
53	0	25400
.	.	.
.	.	.
.	.	.
53	377	25777
54	0	26000
.	.	.
.	.	.
.	.	.
54	377	26377
55	0	26400
.	.	.
.	.	.
.	.	.
55	377	26777
56	0	27000
.	.	.
.	.	.
.	.	.
56	377	27377
57	0	27400
.	.	.
.	.	.
.	.	.
57	377	27777
60	0	30000
.	.	.
.	.	.
.	.	.
60	377	30377

Block	Offset	Octal	Block	Offset	Octal
61	0	30400	71	0	34400
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
61	377	30777	71	377	34777
62	0	31000	72	0	35000
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
62	377	31377	72	377	35377
63	0	31400	73	0	35400
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
63	377	31777	73	377	35777
64	0	32000	74	0	36000
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
64	377	32377	74	377	36377
65	0	32400	75	0	36400
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
65	377	32777	75	377	36777
66	0	33000	76	0	37000
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
66	377	33377	76	377	37377
67	0	33400	77	0	37400
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
67	377	33777	77	377	37777
70	0	34000			
.	.	.			
.	.	.			
.	.	.			
70	377	34377			

APPENDIX C

7-BIT ASCII CODE

Octal Code	Char.	Octal Code	Char.	Octal Code	Char.	Octal Code	Char.
000	NUL	040	SP	100	@	140	
001	SOH	041	!	101	A	141	a
002	STX	042	"	102	B	142	b
003	ETX	043	#	103	C	143	c
004	EOT	044	$	104	D	144	d
005	ENQ	045	%	105	E	145	e
006	ACK	046	&	106	F	146	f
007	BEL	047	'	107	G	147	g
010	BS	050	(	110	H	150	h
011	HT	051	)	111	I	151	i
012	LF	052	*	112	J	152	j
013	VT	053	+	113	K	153	k
014	FF	054	,	114	L	154	l
015	CR	055	-	115	M	155	m
016	SO	056	.	116	N	156	n
017	SI	057	/	117	O	157	o
020	DLE	060	0	120	P	160	p
021	DC1	061	1	121	Q	161	q
022	DC2	062	2	122	R	162	r
023	DC3	063	3	123	S	163	s
024	DC4	064	4	124	T	164	t
025	NAK	065	5	125	U	165	u
026	SYN	066	6	126	V	166	v
027	ETB	067	7	127	W	167	w
030	CAN	070	8	130	X	170	x
031	EM	071	9	131	Y	171	y
032	SUB	072	:	132	Z	172	z
033	ESC	073	;	133	[	173	{
034	FS	074	<	134	\	174	|
035	GS	075	=	135	]	175	}
036	RS	076	>	136	↑	176	~
037	US	077	?	137	←	177	DEL