digital

Computer Special Systems

MAGTAPE TRANSPORT ADAPTER

OPTION DESCRIPTION

COMPUTER TYPE PDP-11	DRAWING SET NO. B-DD-M8921-0
PROGRAM NO. DECSPEC-11-AYVAD DECSPEC-11-AYVBD DECSPEC-11-AYVCD DECSPEC-11-AYVDD DECSPEC-11-AYVED DECSPEC-11-AYVFD	DOCUMENT NO. CSS-MO-F-5.2-23
DATE February 1977	

1st Printing July 1976
2nd Printing February 1977

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SECTION 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The Magtape Transport Adapter (MTA), designed and manufactured by Digital, interfaces the TM02 Magnetic Tape Controller to the TU45 Tape Transport. The MTA in essence is a buffer capable of handling and converting logic signals to and from the TM02 and to and from the TU45 Tape Transport. Capable of both phase-encoded (PE) (1600 bpi dual-density) and NRZI (800 bpi) recording, the MTA is designed for a tape speed of 75 inches per second (IPS). The MTA logic is fully contained on one module (M8921) and consists of the following functional sections:

a. Basic crystal and selectable clock frequencies for the TM02
b. Motion logic
c. Write logic
d. Read logic
e. Delay logic
f. Serial number registers
g. Miscellaneous circuits

1.2 SPECIFICATIONS

a. Mechanical:

Logic Housing	One printed circuit board (M8921)
Dimensions	12.1 in. X 15.688 in.
Interconnections	TM02 Slave Bus (daisy-chain) Transport Bus (one only)

b. Electrical:

Logic Power	+5 Vdc @ 1.5 A
Logic Levels	TTL (0 to 3 V)
Power Supply	H716-B (115 Vac) or H716-D (230 Vac)
Depth	12.00 in. (.305 m)
Width	5.25 in. (.133 m)
Height	5.14 in. (.105 m)
Weight	7 lb. (3.18 kg)

c. Operational:

Packing Density	800 and 1600 bpi; Program Selectable
Tape Speed	
Forward/Reverse	75 IPS
Rewind	250 IPS
Maximum Transfer Rate	120,000 cps

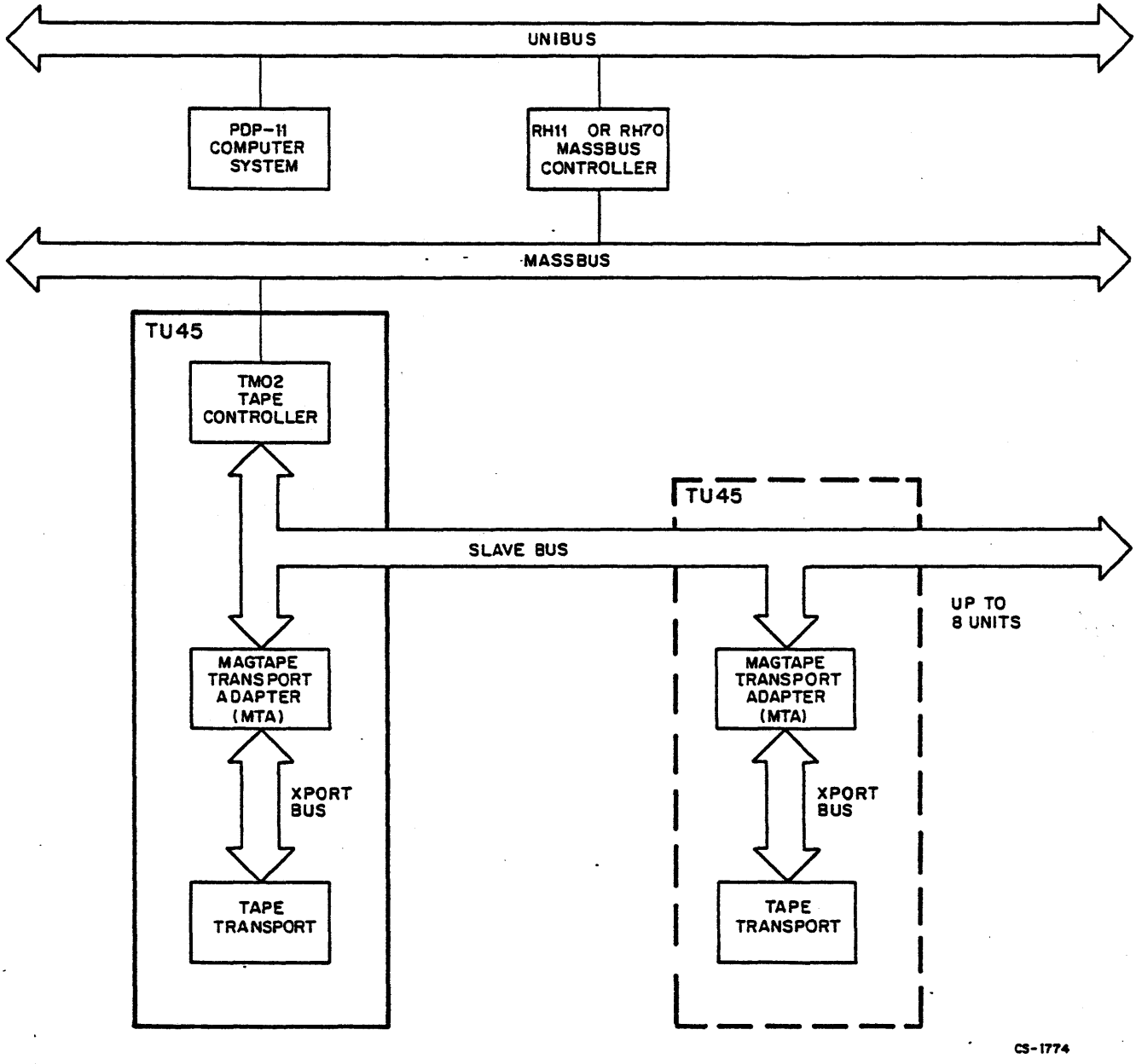

Figure 1-1 MTA Simplified System Diagram

SECTION 2
INSTALLATION

2.1 SITE CONSIDERATIONS

All logic comprising the MTA is on one printed circuit board (M8921) that is located at the rear of the cabinet which houses the tape transport. Power is provided by an H716-B (115 Vac) or H716-D (230 Vac) power supply.

All general environmental requirements specified for the PDP-11 computer system also apply to the MTA.

2.2 CABLES

Connections between the TM02, MTA, and TU45 transport are made via the Slave Bus (BC06R-XX) and XPORT Bus (BC08R-05).

2.2.1 Slave Bus

Slave bus cable connections between the TM02 and the TU45 (and between daisy-chained TU45s) are shown in Figure 2-1. A half-twist in the slave bus cable is not required between the TM02 and the first (or single) TU45, but if multiple TU45s are installed, a half-twist of the slave cable must be used. Refer to Paragraph 2.2.3 for cable identification marks. Tables 2-1 through 2-3 list the slave bus signals as they are referenced at their associated connectors (refer to Engineering Drawing B-DD-M8921-0).

NOTE
The slave bus should not exceed 80 ft. in length.

Table 2-1
Slave Bus 1 (Connector J6/J7)

Pin	SB1 Signal	Pin	SB1 Signal
A	WD 00 (SB) L	AA	WD 05 (SB) L
C	WD P (SB) L	CC	WD 04 (SB) L
E	WD 01 (SB) L	EE	WD 03 (SB) L
H	WD 07 (SB) L	HH	SS 00 (SB) L
K	WD 02 (SB) L	KK	DRV SET PLS (SB) L
M	WD 06 (SB) L	MM	EMD (SB) L
P	REC (SB) L	PP	INIT PLS (SB) L
S	ACCL (SB) L	SS	DRV CLR PLS (SB) L
U	SS 01 (SB) L	UU	STOP (SB) L
W	LRC STRB (SB) L	VV	+5 V from TM02
Y	SS 02 (SB) L		

Table 2-2
Slave Bus 2 (Connector J8/J9)

Pin	SB2 Signal	Pin	SB2 Signal
A	MRD 0 (SB) L	AA	END PT (SB) L
C	MRD P (SB) L	CC	SET SSC (SB) L
E	MRD 1 (SB) L	EE	RWND (SB) L
H	MRD 7 (SB) L	HH	NOT USED
K	MRD 2 (SB) L	KK	TUR (SB) L
M	MRD 6 (SB) L	MM	WRT CLK (SB) L
P	MRD 3 (SB) L	PP	FWD (SB) L
S	MRD 5 (SB) L	RR	CLOCK (SB) L
U	MRD 4 (SB) L	SS	WRITE (SB) L
W	RSD 0 (SB) L	UU	REV (SB) L
Y	BOT (SB) L	VV	+5 V from TM02

Table 2-3
Slave Bus 3 (Connector J10/J11)

Pin	SB3 Signal	Pin	SB3 Signal
A	MOL (SB) L	U	SN 14 (SB) L
B	PESB (SB) L	V	SN 15 (SB) L
C	7 CH (SB) L	W	SN 03 (SB) L
D	SN 00 (SB) L	X	DT 02 (SB) L
E	SN 02 (SB) L	Y	RWS (SB) L
F	SN 05 (SB) L	AA	DT 01 (SB) L
H	SN 04 (SB) L	CC	WRL (SB) L
J	SN 06 (SB) L	EE	DEN 00 (SB) H
K	SN 01 (SB) L	HH	DT 00 (SB) L
L	SN 07 (SB) L	KK	SDWN (SB) L
M	SN 08 (SB) L	MM	SLA (SB) L
N	SN 09 (SB) L	PP	IRD (SB) L
P	SN 10 (SB) L	RR	SPR (SB) L
R	SN 11 (SB) L	SS	DEN 02 (SB) H
S	SN 12 (SB) L	UU	DEN 01 (SB) H
T	SN 13 (SB) L	VV	+5 V from TM02

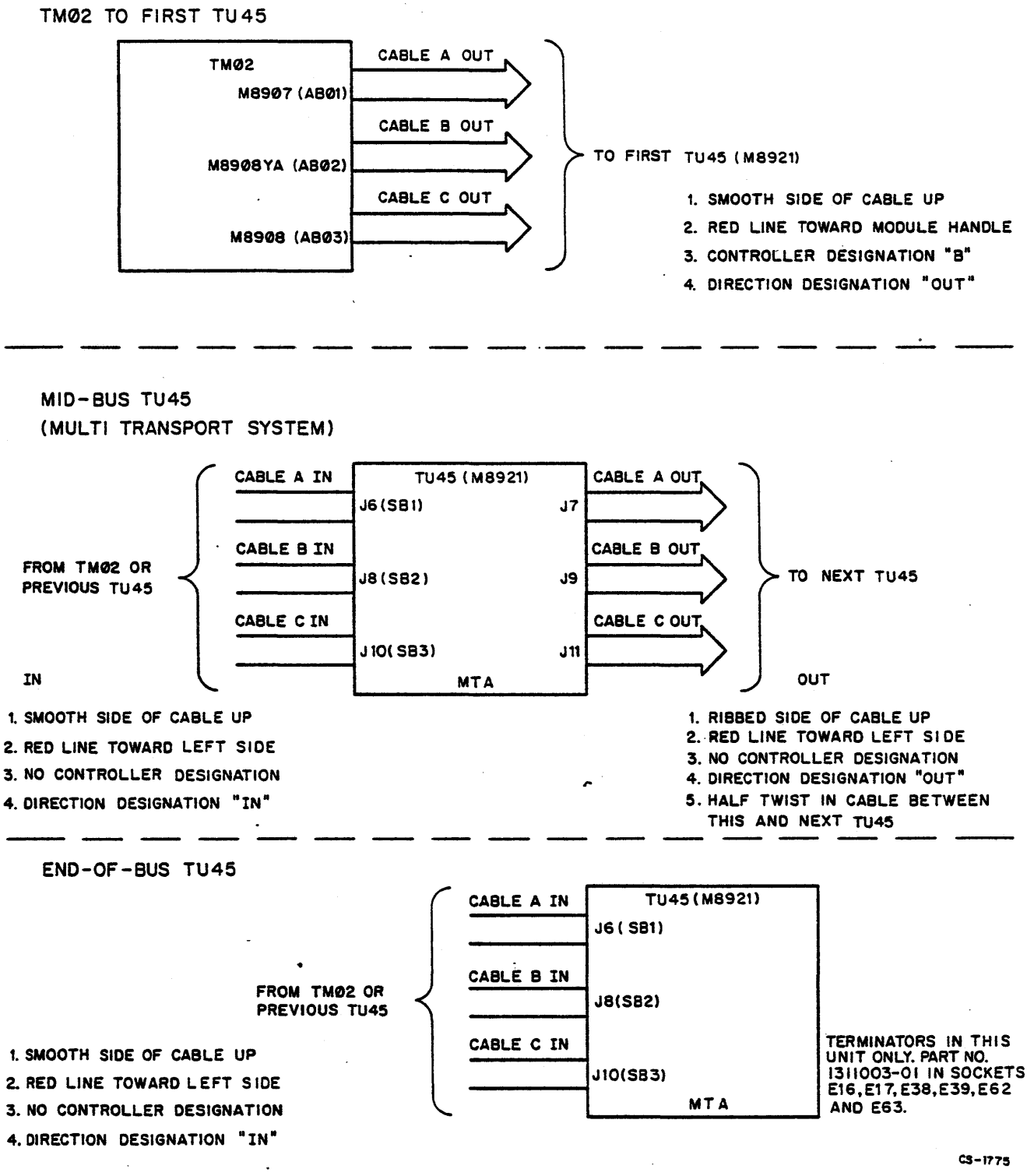

Figure 2-1 TM02/TU45 Slave Bus Cabling

2.2.2 XPORT Bus

XPORT Bus connections between the MTA and the TU45 Tape Transport (Figure 2-2) are made via three 40-conductor ribbon cables and one 9-conductor wiring harness. The ribbon cables handle the control, write, and read signals and the 9-conductor wiring harness handles the address signals to the UNIT SELECT switch. The XPORT Bus should not exceed 20 feet in length. Tables 2-4 through 2-7 list the XPORT Bus signals as they are referenced at their associated connectors.

NOTE

Connectors on the XPORT Bus consist of Berg for the MTA end and Cinch for Tape Transport end. To establish proper continuity, a special adapter connector (DEC #5411692) is included that fits over the Cinch connector allowing proper contact by the Berg connector. Table 2-8 provides a cross reference depicting pin assignments for these two connectors.

Table 2-4
Transport Bus (Connector J1-Control)

Pin	Signal	Pin	Signal
F	IFSC (PEC) L	BB	IRWD (PEC) L
J	IDDS (PEC) L	DD	IFPT (PEC) L
L	ISRC (PEC) L	FF	ILDP (PEC) L
N	IDDI (PEC) L	JJ	+5 V from (PEC)
R	IRWC (PEC) L	LL	IRDY (PEC) L
T	ISLT 0 (PEC) L	MM	IEOT (PEC) L
V	ISWS (PEC) L	SS	
X	IOFC (PEC) L	TT	
Z	I ON-LINE (PEC) L	UU	+5 V From (PEC)
		VV	

Table 2-5
Transport Bus (Connector J2 - Write)

Pin	Signal	Pin	Signal
B	IWDS (PEC) L	DD	IWD2 (PEC) L
F	IWARS (PEC) L	FF	IWD3 (PEC) L
X	IWDP (PEC) L	JJ	IWD4 (PEC) L
Z	IWD0 (PEC) L	LL	IWD5 (PEC) L
BB	IWD1 (PEC) L	NN	IWD6 (PEC) L
		RR	IWD7 (PEC) L

Table 2-6
Transport Bus (Connector J3 - Read)

Pin	Signal	Pin	Signal
A	IRDP (PEC) L	W	INRZ (PEC) L
C	IRDS (PEC) L	EE	IRD4 (PEC) L
E	IRD0 (PEC) L	HH	IRD5 (PEC) L
H	IRD1 (PEC) L	MM	IRD6 (PEC) L
S	IRD2 (PEC) L	PP	IRD7 (PEC) L
U	IRD3 (PEC) L		

Table 2-7
Transport Unit Select (Connector J4 - Address)

Pin	Signal	Pin	Signal
1	SLT (P) H	6	SLT 1 (P) H
2	SLT 3 (P) H	7	SLT 6 (P) H
3	SLT 0 (P) H	8	SLT 7 (P) H
4	SLT 4 (P) H	9	SLT 2 (P) H
5	SLT 5 (P) H		

Table 2-8
Connector Adapter

Berg	Cinch	Berg	Cinch
A	1	Y	11
B	A	Z	M
C	2	AA	12
D	B	BB	N
E	3	CC	13
F	C	DD	P
H	4	EE	14
J	D	FF	R
K	5	HH	15
L	E	JJ	S
M	6	KK	16
N	F	LL	T
P	7	MM	17
R	H	NN	U
S	8	PP	18
T	J	RR	V
U	9	SS	S
V	K	TT	S
W	10	UU	S
X	L	VV	S

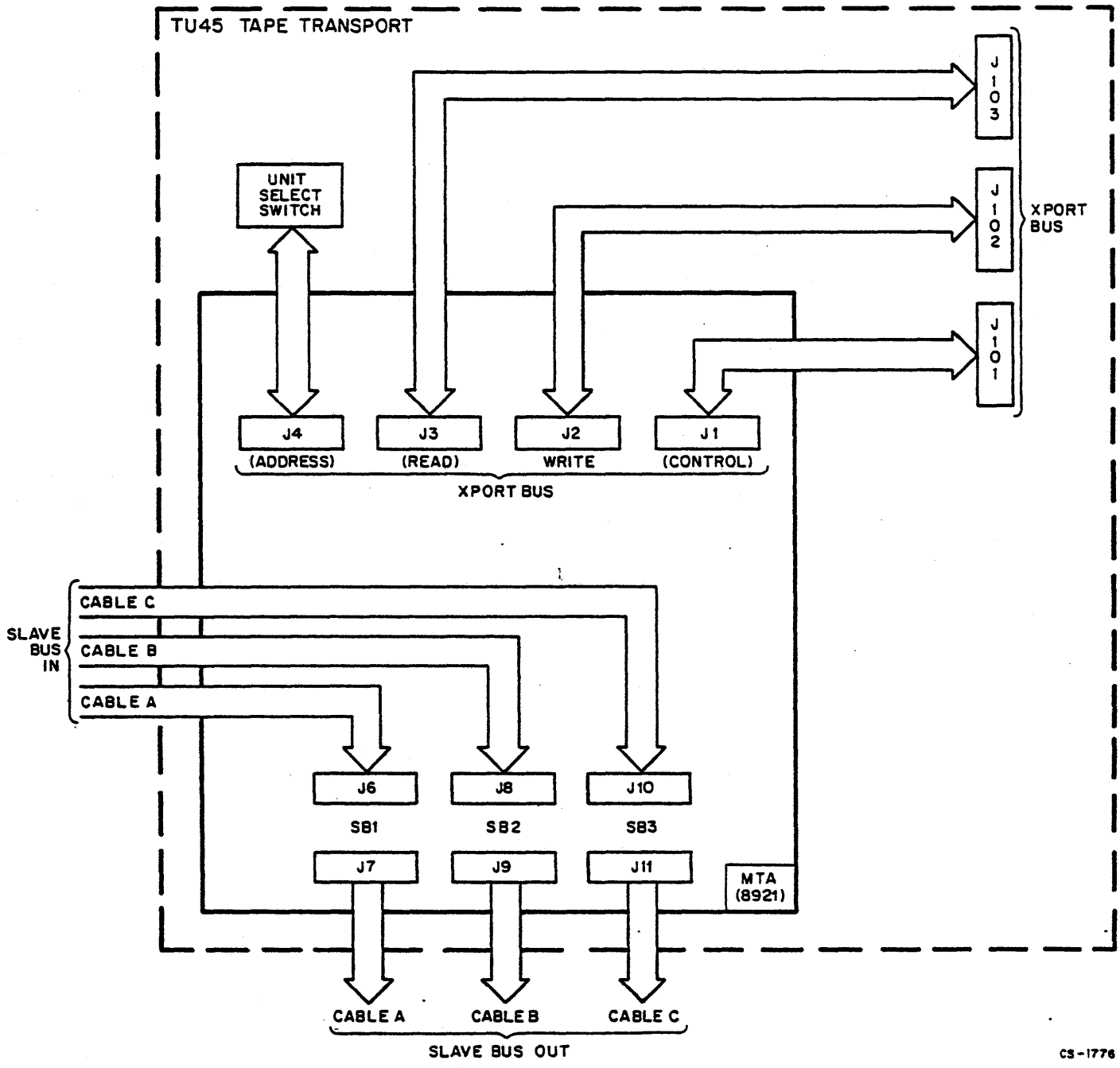

Figure 2-2 MTA/TU45 XPORT Bus Cabling

2.2.3 Markup of Massbus and Slave Bus Cables

Both surfaces of each end of the Massbus and Slave bus cables are stamped as shown in Figure 2-3. The stamps are marked up to indicate cable designations at the time the cables are installed. Mark the BC06R Massbus cables as follows when installing them:

1. Cross out the designation THIS SIDE UP on the under side of the cable.
2. Cross out the CONTROLLER designation that does not apply. Cross out B when plugging into the RH11/RH70 and cross out A when plugging into the TM02.
3. Cross out the CONNECTOR MODULE designations that do not match the cable letter being used.
4. Cross out IN for the output cables and cross out OUT for the input cables.

Figure 2-4 shows an example of a cable that is marked up to be plugged into the M5903YA module in slot A/B06 of an end-of-bus TM02.

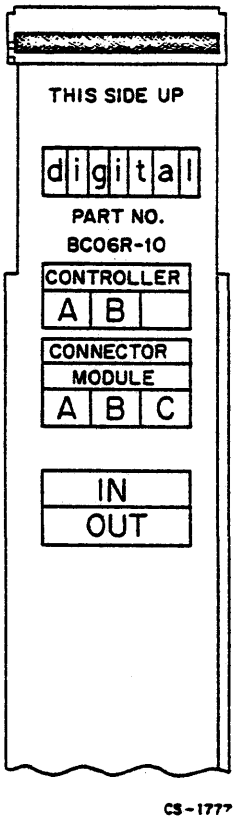

Figure 2-3 Massbus Cable Stamp

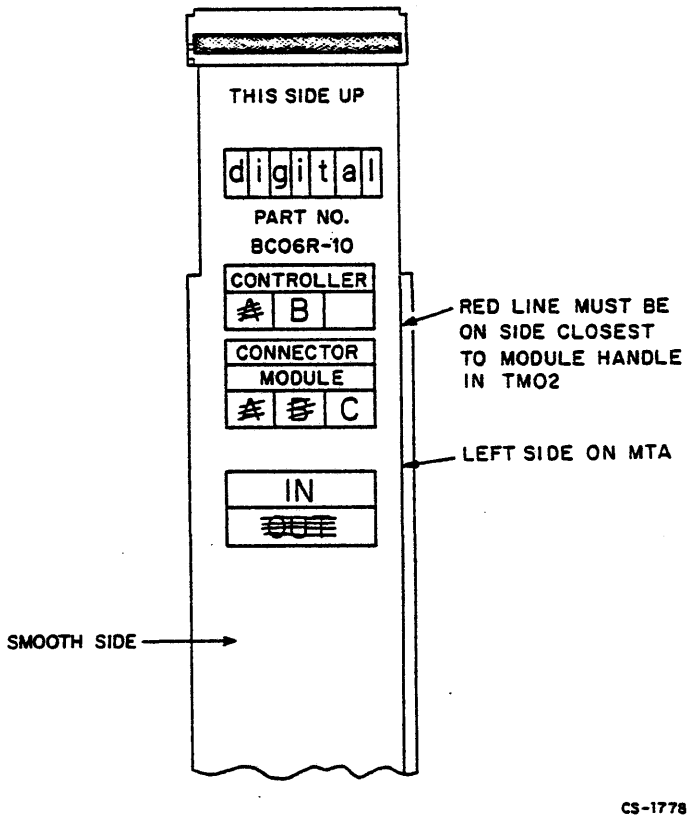

Figure 2-4 Marked-UP Massbus Cable

2.3 GROUNDING

All grounding requirements are satisfied by the standard cable connections. (See the Installation Section of the appropriate TU45 Systems Manual).

2.4 INITIAL OPERATION

Refer to the Checkout and Acceptance procedures in the appropriate TU45 System Manual.

2.5 TU45 RELATED LITERATURE

TJU45 Magtape System Manual, CSS-MO-F-5.2-21
TWU45 Magtape System Manual, CSS-MO-F-5.2-25
TM02-FE/FF Magnetic Tape Controller Manual, CSS-MO-5.2-22
RH11/Special Massbus Controller, CSS-MO-F-5.2-26
RH70/Special Massbus Controller, CSS-MO-F-5.2-27
TU45 Tape Transport Manual (Pertec #104597)
DEC System 20 Manual, EK-KL10-TD-002

SECTION 3
OPERATION AND PROGRAMMING

3.1 INDICATORS

Two light emitting diodes (LEDs) are mounted on the M8921 MTA module. The top LED (D5) lights when +5 V is present on the MTA. The bottom LED (D4) indicates that the transport is selected and moving tape or was the last address selected if the system halted.

3.2 INPUT/OUTPUT CODING

Drive Type (DT) is selected by three jumpers (W37, W38, and W39). For the TU45, jumper W38 is always in and jumpers W37 and W39 are out designating the TU45 as always drive type two.

The following are the MTA jumpers, as they are configured to provide specific functions.

Jumper	Condition		Function
	IN	OUT	
W1		X	MTA5 +5 V (PEC)
W2	X		MTA2 EXT +5 V (J5)
W3		X	MTA2 7CH SEL
W4	X		MTA3 Basic Clock
W5		X	
W7	X		
W9		X	
W11		X	MTA3 Set IWDS flip-flop
W13		X	
W15		X	
W17		X	
W19		X	
W6		X	
W8		X	
W10		X	
W12		X	MTA3 - Reset IWDS flip-flop
W14		X	
W16	X		
W18		X	
W20		X	
W21			
W22			
W23			
W24			
W25			
W26			
W27			Serial Number register. Appropriate
W28			jumpers will be in to identify the
W29			serial number of the transport
W30			register to be read.
W31			
W32			
W33			
W34			
W35			
W36			

Jumper	Condition IN	Condition OUT	Function
W37		X	MTA4 DTS0 L
W38	X		MTA4 DTS1 L
W39		X	MTA4 DTS2 L
W40		X	
W41	X		MTA7 PESB L
W42	X		MTA7 WRL L
W43		X	
W44	X		MTA2 ISWS (PEC) L

3.3 SERIAL NUMBER REGISTER

The Serial Number register (Figure 3-1) is simply 16 jumpers, the combination of which are inserted at the factory to identify the serial number of the TU45.

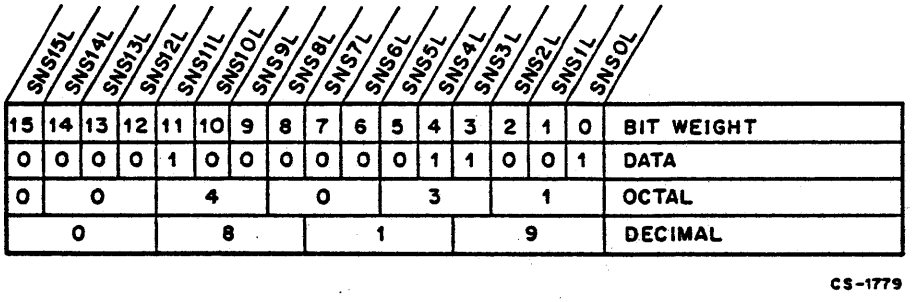

Figure 3-1 Example of Serial Number Register

In the above example, the serial number is 0819 (decimal) or 004031 (octal).

NOTE

The Serial Number Register will be typed in octal when using diagnostic programs.

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

This section presents a functional description of the events that occur within the Magtape Adapter logic during all basic operations. The M8921 and M8903 Engineering Drawing Sets should be available to the reader.

4.2 MTA CLOCK CIRCUIT (MTA3)

The MTA Clock circuit primarily consists of the following circuit components.

a. One 3.84 MHz crystal (Y1)
b. Schmitt trigger gates (E70)
c. Three type 74161 4-Bit synchronous counters (E58, E59, and E69) to divide and select appropriate frequencies.

The basic clock frequency is controlled by a 3.84 MHz crystal, and produces all free-running system clock waveforms used in the TM02. The 3.84 MHz clock is divided down to 240 kHz, and is transmitted to the TM02 via the SLAVE BUS clock (SB) by an on-line, selected transport loaded with tape. This clock is further divided on the M8903 (TCCM) module in the TM02 to provide the following frequencies:

DATA HALF	120 KHz
800 BPI CLK	60 KHz
200 BPI CLK	15 KHz

These clocks perform various housekeeping functions in the TM02. For example, 800 BPI CLK clocks the Motion Delay Counter (M8903, sheet 3); 200 BPI CLK clocks the IDB counter, Write End Counter, and Shutdown Counter.

DATA HALF is essentially a 1600 bpi clock and is used in functions pertaining to PE mode. For instance, it clocks the Character Counter on the Tape Control – PE module (M9802, sheet 4).

The TM02 is capable of reading and writing data at several bit densities. To do this a separate clock signal (WRT CLK), whose frequency depends on the tape data density, must be developed.

WRT CLK is a basic data rate clock used by the TM02 to send or receive data during transfers. E58 and E59, two 4-bit 74161 synchronous counters, are connected in series to count up a 960 Hz clock to the desired frequency according to the preset data contained in the density select PROM (DEC-23141A1-XX)* (E54). The PROM is addressed in the on-line mode by the DENSITY SELECT bits 00:02 issued by the TM02 (in the off-line mode TEST PE and TEST DEN determine the address of the PROM). The content of the PROM is shown in the ROM map (Table 4-1).

The preset of the 74161 counters (E58-E59) are determined by various signals and conditions. These are listed in Table 4-2 along with the resulting Counter Presets, WRT CLK frequency and density. Note that WRT CLK frequency for 1600 bpi is four (4) times that at 800 bpi. This is because 1600 bpi is used only in PE mode which requires a double frequency WRT CLK.

Obviously, the frequency of the cycle will vary with the magnitude of the preset. Figure 4-1 shows timing diagrams for presets of -1 (-n =2's complement of n), -2, and -3. Note that for a preset of -n, the frequency of WRT CLK, is equal to [960/(n+1)] KHz.

*See latest revisions of drawings (B-DD-M8921-0) for appropriate value of -XX.

Table 4-1
Write Clock ROM Map

ROM ADDRESS (OCTAL)	DEN 0 14 E	DEN 1 13 D	DEN 2 12 C	TEST DEN 11 B	TEST PE 10 A	9	7	6	5	4	3	2	1	PIN OCTAL	DENS	FREQ	USE
00	0	0	0	0	0	0	1	0	1	0	0	1	1	123	238		TEST
01	0	0	0	0	1	1	0	0	0	1	1	1	1	217	800	60K	TEST
02	0	0	0	1	0	0	0	1	1	1	1	1	1	077	1277	192K	TEST
03	0	0	0	1	1	1	0	0	0	0	0	1	1	203	200	15K	
04	0	0	1	0	0	0	1	0	1	0	0	1	1	123	N/A		
05	0	0	1	0	1	1	0	0	0	1	1	1	1	217	N/A		
06	0	0	1	1	0	0	1	0	1	1	1	1	1	137	N/A		
07	0	0	1	1	1	1	0	1	1	1	1	1	1	277	1600	240K	
10	0	1	0	0	0	0	1	0	1	0	0	1	1	123	N/A		
11	0	1	0	0	1	1	0	0	0	1	1	1	1	217	N/A		
12	0	1	0	1	0	0	0	1	1	1	1	1	1	077	N/A		
13	0	1	0	1	1	1	0	0	0	1	1	1	1	217	800	60K	
14	0	1	1	0	0	0	1	0	1	0	0	1	1	123	N/A		
15	0	1	1	0	1	1	0	0	0	1	1	1	1	217	N/A		
16	0	1	1	1	0	0	0	1	1	1	1	1	1	077	N/A		
17	0	1	1	1	1	1	0	0	0	1	1	1	1	217	800	60K	
20	1	0	0	0	0	0	1	0	1	0	0	1	1	123	N/A		
21	1	0	0	0	1	1	0	0	0	1	1	1	1	217	N/A		
22	1	0	0	1	0	0	0	1	1	1	1	1	1	077	N/A		
23	1	0	0	1	1	0	1	0	1	0	1	1	1	127	556	41.7K	
24	1	0	1	0	0	0	1	0	1	0	0	1	1	123	N/A		
25	1	0	1	0	1	1	0	0	0	1	1	1	1	217	N/A		
26	1	0	1	1	0	0	0	1	1	1	1	1	1	077	N/A		
27	1	0	1	1	1	0	0	1	1	1	1	1	1	077	1277	192K	
30	1	1	0	0	0	0	1	0	1	0	0	1	1	123	N/A		
31	1	1	0	0	1	1	0	0	0	1	1	1	1	217	N/A		
32	1	1	0	1	0	0	0	1	1	1	1	1	1	077	N/A		
33	1	1	0	1	1	1	0	0	0	1	1	1	1	217	800	60K	
34	1	1	1	0	0	0	1	0	1	0	0	1	1	123	N/A		
35	1	1	1	0	1	1	0	0	0	1	1	1	1	217	N/A		
36	1	1	1	1	0	0	0	1	1	1	1	1	1	077	N/A		
37	1	1	1	1	1	1	0	1	1	1	1	1	1	277	1600	240K	

Table 4-2
Write Clock Frequencies

	DEN 2	DEN 1	DEN 0	Test PE	Test DEN	WRT CLK Counter Presets LSB MSB	Frequency KHz (bpi)
On-Line	0	0	0	1	1	10000011	15 (200)
	0	0	1	1	1	01010111	41.7 (556)
	0	1	0	1	1	10001111	60 (800)
	0	1	1	1	1	10001111	60 (800)
	1	0	0	1	1	10111111	240 (1600)
	1	0	1	1	1	00111111	192 (1277)
	1	1	0	1	1	10001111	60 (800)
	1	1	1	1	1	10111111	240 (1600)
Off-Line	x	x	x	0	0	01010011	17.5 (233)
	x	x	x	0	1	10001111	60 (800)
	x	x	x	1	0	00111111	192 (1277)
	x	x	x	1	1	10000011	15 (200)

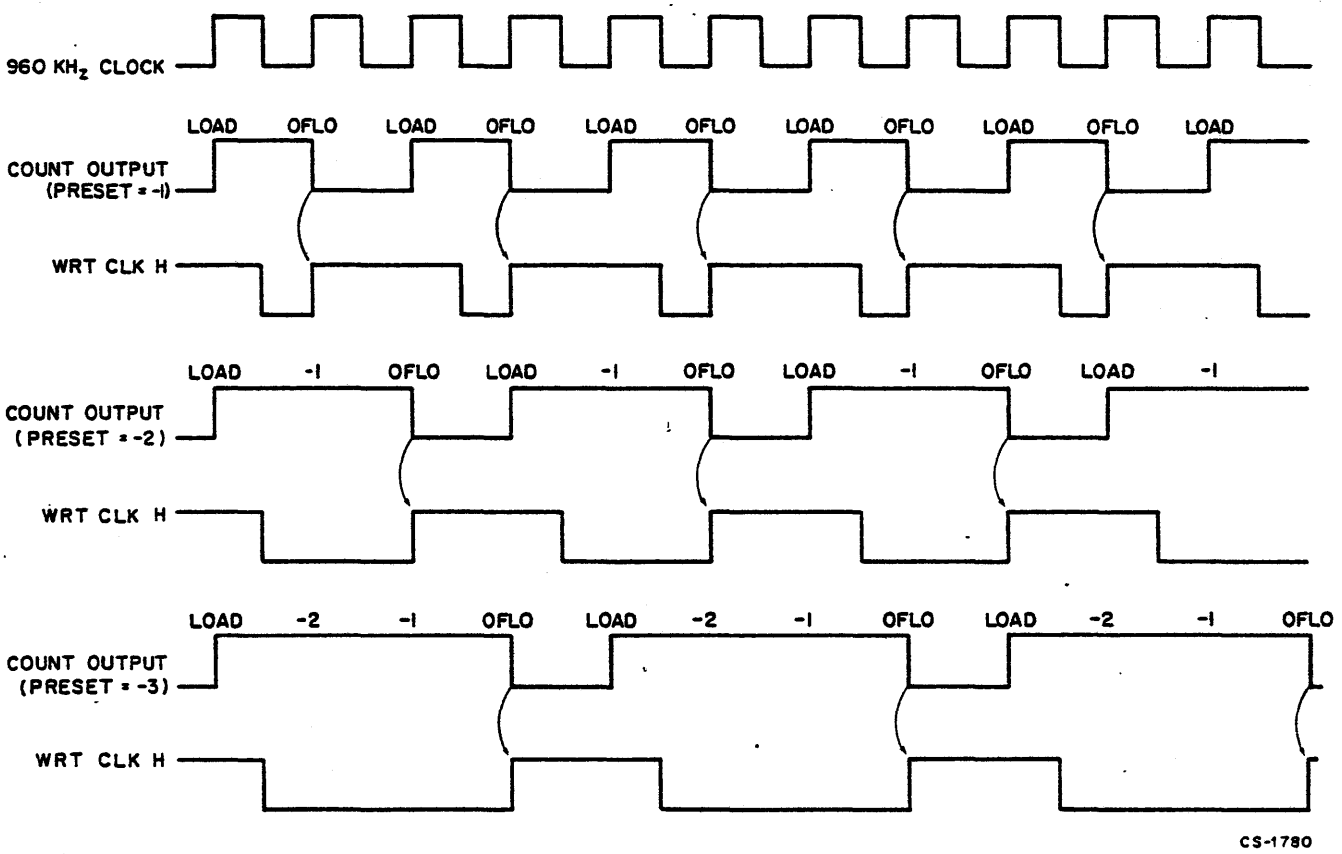

Figure 4-1 WRT CLK Generation Timing

4.3 WRITE DATA STROBE GENERATION (MTA3)

The Write Data Strobe (IWDS) logic is developed via E53, E74, E66, E67, E40, and E47 (upper right corner of Engineering Drawing (MTA3).

Signal MTA6 REC (SB) is received by the MTA from the TM02 coincident with the data to be written on tape. The leading edge of REC L sets a flip-flop (E74 PIN 8) to a low. The 3.84 MHz CLK will clock this low input through the Shift Register (E66) on successive clock pulses. When E66 PIN 3 goes low, the E74 flip-flop is reset. The odd numbered jumpers (W5-W19) are used to delay the leading edge of the Write Data Strobe. The even numbered jumpers (W6-W20) are used to determine the Write Data Strobe pulse width. For the TU45, jumpers W7 and W16 are in, all others are cut. These jumpers provide a delay of 260 ns and a pulse width of 1.04 μs with a period corresponding to the selected density. See Figure 4-2 for the timing at 1600 bpi.

4.4 SELECT LOGIC (MTA2)

The Slave Select bits SS0-SS2 are received from the slave bus and inverted with 7404s (E52, upper left corner of Engineering Drawing MTA2). The Slave Select bits are decoded with a decoder (E61) and inverted by E65 and E52 to be sent to the transport as SLT0 to SLT7 (Engineering Drawings MTA2 and MTA5).

If the transport thumbwheel SELECT switch is set to the decoded SELECT BITS signal, MTA5 SLT (p) H becomes true. If the transport is placed on-line and is selected the SELECT LED is illuminated.

To quickly verify operation of the select logic, load via the switch register the following programs.

Location	Content	Mneumonic
30000	013737	MOV SR MTTC
30002	777570	
30004	772472	
30006	000240	NOP
30010	000240	NOP
30012	000137	JMP 30000
30014	030000	

Load START at Location 30000

Switch register bits 00 to 02 correspond to SS0 to SS2 respectively. Set the transport on-line, select a number via the thumbwheel, issue the appropriate select code via the switch register and observe the SELECT LED.

NOTE

The output of the DENSITY PROM (MTA2) can be examined using the same routine as shown above via switch register bits 8, 9, and 10 which correspond to DEN 00 to DEN 02 respectively.

4.5 PEC POWER OK, CROBAR, P CLEAR (MTA2)

Two redundant circuits monitor the state of the +5 V power. The 2nd circuit is required if an external +5 V power source is used. For the TU45, jumper W2 is in (coordinates D2 on MTA2).

Signals MTA2 CROBAR L, MTA2 P CLR L, and NOT PEC PWR OK will be asserted until the +5 V power rises to approximately 4.5 volts. At this time, transistors Q1 and Q3 will turn on. As long as the power remains above 4.5 V, MTA2 CROBAR, MTA2 P CLR, and MTA2 PWR OK will be high.

4.6 MTA2 SET SSC L AND MTA2 SLA (1)

The logic in the center of Engineering Drawing MTA2 including E13, E14, E21, E26, E27, and E31 are used to develop two signals (MTA2 SET SSC L and MTA SLA (1)) to the TM02 controller. MTA2 SET SSC indicates a slave status change. The following conditions require this signal.

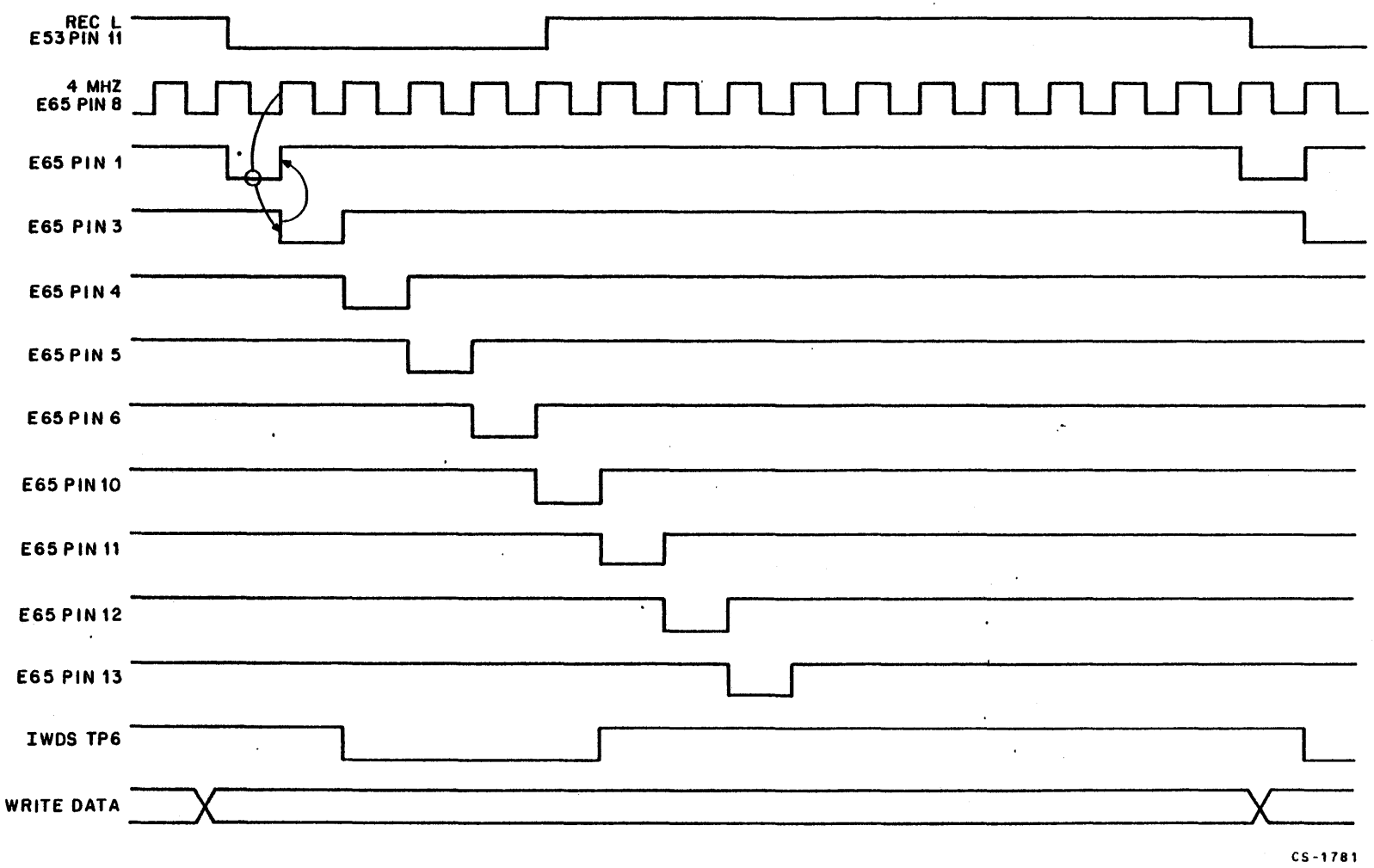

Figure 4-2 Write Strobe Delay and Pulse Width (1600 bpi)

a. ON LINE AND CROBAR (a change in either direction)
b. MTA RWD STATUS (transport starting a rewind)
c. MTA2 PEC PWR OK (transport power going off)
d. MTA2 REWIND (1) L AND LOAD POINT (illegal)

Pulses of 2.08 μs are generated at the output of E13 (74174 D-Type flip-flop) by the 480 KHz CLK setting the status true and then setting the status complement true on the next clock pulse.

The outputs of E13 are ORed at E14 and E21 to develop the 2.08 μs pulse SET SSC L.

Signal MTA2 SLA (1) L indicates slave attention to the TM02 controller. This signal is set by ON LINE and NOT CROBAR becoming true, i.e., when the transport is placed on-line and the power is above 4.5 volts.

NOTE

The signal to the TM02 slave bus is gated by the signal MTA2 ON LINE. MTA2 ON LINE requires that the transport also is selected. Thus, turning a drive on or off line has no affect on the TM02 unless the drive is selected.

4.7 MTA2 SDWN AND MTA2 TUR LOGIC

The logic for these functions is located in the upper center of Engineering Drawing MTA2 coordinates D3–D5. Any of the commands FWD, REV or RWD being asserted will cause E47 pin 5 to go low. This causes the integrating one-shot E31 pin 13 to go high and E31 pin 4 to go low. When the command is removed, E47 pin 5 goes open allowing the timing capacitor to charge to +5 V. The one-shot times out in approximately 6 ms, thus MTA2 SDWN L is a 6 ms low-going pulse occurring at the removal of the motion command (trailing edge) so that the tape transport can decelerate. MTA2 TUR L is a low-level which is true when the transport does not have a motion command, the shut down period has expired, and the transport is in the ready state (loaded, on-line, and not rewinding).

4.8 MOTION DELAY CIRCUITS (MTA4)

The motion delay logic is located on Engineering Drawing MTA4 and is comprised of the Motion Delay ROM E2 and the Read Data Multiplexors E7 and E8.

For each operation of the transport there is a specific delay count contained in the ROM. The purpose of these delay counts is to allow for the acceleration of the tape to speed and for gap spacing between records.

The sequence is initiated by MTA6 DRV SET PLS (SB) L loading the selected command into the Command register E48 (74174) on print MTA2. The commands FWD (1) H and WRITE (1) H together with MTA2 7 CH H, MTA3 ACCL ON LINE H and MTA5 ILDP (PEC) L are used to select an address in the motion delay ROM. The content of the selected address is gated onto the Read Data lines MTA4 MRD 0 - MRD 7, MRD P by the MTA6 EMD (SB) L signal (Enable Motion Delay). The EMD signal strobes the delay count into the delay counter of the TM02 (Engineering Drawing TCCM3) and up counts to 2^{14} counts at the clock rate of the 800 BPI CLK (16.67 μs for the TU45). This Stop Delay is used to terminate a function and is initiated by MTA6 EMD (SB) L being asserted for a second time to gate the Stop Delay from the Motion Delay ROM to the delay counter in the TM02.

Figure 4-3 shows the sequence of starting and stopping and the interrelations of the required signals. Modification of the preset data occurs for the WRITE TAPE MARK AND ERASE functions in the TM02. An additional 3072 counts are added to the START DELAY if the tape is not at LOAD POINT.

4.9 READ DATA LOGIC (MTA4)

The data from the tape is gated onto the MTA board with ENABLE READ L (generated in the lower left hand corner of MTA4). ENABLE READ L is asserted when either ~ACCL (SB) H is asserted or PIN 5 of the one-shot (E5A) is high. ~ACCL (SB) H is high when the tape is at speed or slowing down (normal conditions for data to be read). The one-shot is used so that the ID Burst, which occurs while the tape is accelerating from BOT, can be read. The one-shot is triggered by ~ILDP (PEC) H which is asserted only when the BOT marker is under the photosensor. ~ILDP (PEC) H has a rising edge, which triggers the one-shot when the tape starts accelerating from BOT. The one-shot then provides a pulse of approximately 7 ms duration during which the controller can look for the ID Burst.

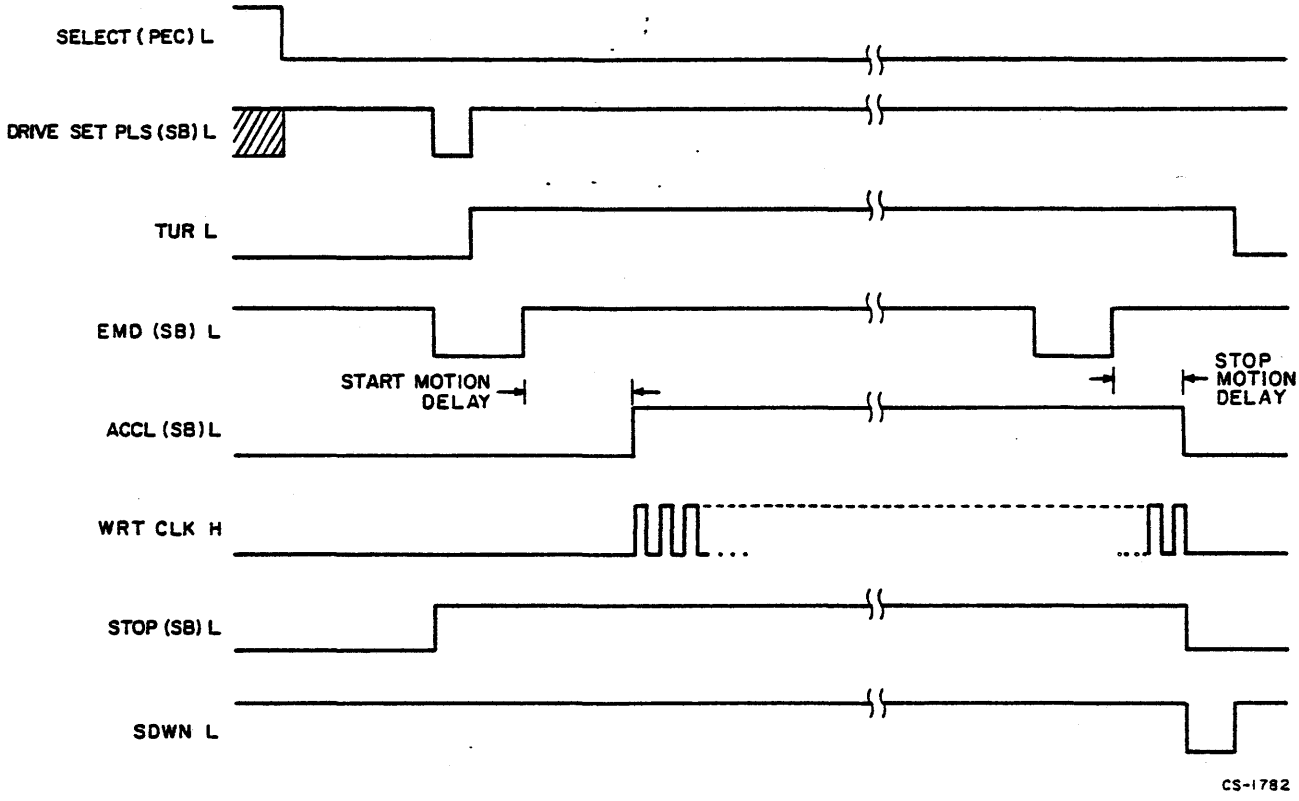

Figure 4-3 Starting and Stopping Interrelationships

Table 4-3 shows the delays necessary to operate the TU45.

Table 4-3
Required Delays for TU45 Operation

DEC	OCTAL	7 Track* E	Write D	FWD C	ACCL On-Line B	LD Point A	MRD P 9	MRD 0 7	MRD 1 6	MRD 2 5	MRD 3 4	MRD 4 3	MRD 5 2	MRD 6 1	Pin	
00	00	0	0	0	0	0	1	1	1	1	1	0	1	1	373	Read Rev Stop
01	01	0	0	0	0	1	1	1	1	1	1	1	1	1	377	Illegal
02	02	0	0	0	1	0	1	1	1	1	1	0	0	1	371	Read Rev Start
03	03	0	0	0	1	1	1	1	1	1	1	1	1	1	377	Illegal
04	04	0	0	1	0	0	1	1	1	1	1	1	1	1	377	Read Fwd Stop
05	05	0	0	1	0	1	1	1	1	1	1	1	1	1	377	Illegal
06	06	0	0	1	1	0	1	1	1	1	1	0	0	1	371	Read Fwd Start
07	07	0	0	1	1	1	1	1	0	1	1	1	1	1	337	Read Fwd Start at LD Point
08	10	0	1	0	0	0	1	1	1	1	1	1	1	1	377	Illegal
09	11	0	1	0	0	1	1	1	1	1	1	1	1	1	377	Illegal
10	12	0	1	0	1	0	1	1	1	1	1	1	1	1	377	Illegal
11	13	0	1	0	1	1	1	1	1	1	1	1	1	1	377	Illegal
12	14	0	1	1	0	0	1	1	1	1	1	1	0	1	375	Write Fwd Stop
13	15	0	1	1	0	1	1	1	1	1	1	1	1	1	377	Illegal
14	16	0	1	1	1	0	1	1	1	0	1	1	0	1	355	Write Fwd Start
15	17	0	1	1	1	1	1	1	1	0	1	1	1	0	356	Write Fwd Start at LD Point
16	20	1	0	0	0	0	1	1	1	1	1	1	1	1	377	
17	21	1	0	0	0	1	1	1	1	1	1	1	1	1	377	
18	22	1	0	0	1	0	1	1	1	1	1	1	0	1	377	
19	23	1	0	0	1	1	1	1	1	1	1	1	1	1	377	
20	24	1	0	1	0	0	1	1	1	1	1	1	1	1	377	
21	25	1	0	1	0	1	1	1	1	1	1	1	1	1	377	
22	26	1	0	1	1	0	1	1	1	1	1	1	1	1	377	
23	27	1	0	1	1	1	1	1	1	1	1	1	1	1	377	
24	30	1	1	0	0	0	1	1	1	1	1	1	1	1	377	
25	31	1	1	0	0	1	1	1	1	1	1	1	1	1	377	
26	32	1	1	0	1	0	1	1	1	1	1	1	1	1	377	
27	33	1	1	0	1	1	1	1	1	1	1	1	1	1	377	
28	34	1	1	1	0	0	1	1	1	1	1	1	1	1	377	
29	35	1	1	1	0	1	1	1	1	1	1	1	1	1	377	
30	36	1	1	1	1	0	1	1	1	1	1	1	1	1	377	
31	37	1	1	1	1	1	1	1	1	1	1	1	1	1	377	

NOTE 1: Spacing delays are the same as for read operations

NOTE 2: ROM = 23140A1-XX**
Inputs: 1 = +3 V
0 = 0 V
Outputs: 1 = +3 V
0 = 0 V

*7 Track Operation not used on TU45

**See latest revision of drawings for appropriate value of -XX.

SECTION 5
MAINTENANCE

5.1 GENERAL

No special tools or test equipment are required for maintaining the Magtape Transport Adapter.

5.2 PREVENTIVE AND CORRECTIVE MAINTENANCE

No preventive maintenance is necessary, all corrective maintenance can be performed utilizing the following system diagnostics, as outlined in the acceptance and checkout procedures which are located in the accompanying Systems Manual.

DECSPEC-11-AYVAD
DECSPEC-11-AYVBD
DECSPEC-11-AYVCD
DECSPEC-11-AYVDD
DECSPEC-11-AYVED
DECSPEC-11-AYVFD

SECTION 6
MODULES

6.1 GENERAL

The MTA consists of one M8921 Module.