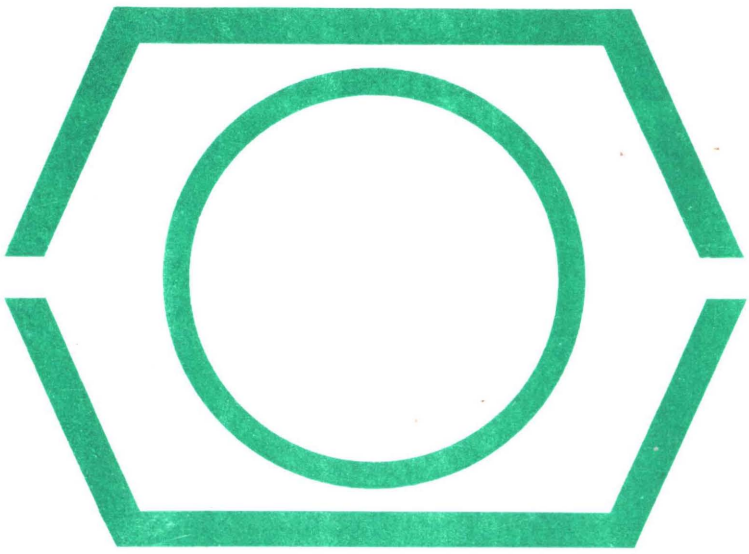
PRECISION CRT DISPLAY / TYPE 30E



PRECISION CRT DISPLAY / TYPE 30E

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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PREFACE

This manual is intended for use with the Type 30A, Type 30E, and Type 30M Precision CRT Displays. These three types of displays are identical in operation and circuitry, and only differ in slight degree with respect to their use. The Type 30A does not contain the five BNC connectors which allow an external oscilloscope to be used for monitoring purposes. The Type 30M contains a reversing switch that allows the horizontal and vertical axes of the display to be interchanged.

Engineering drawings and schematics may become outdated over a period of time. If the equipment does not resemble the printed drawing or schematic, request a print for your particular equipment listing all model and/or serial numbers.

Figure 1-1 Type 30 Precision CRT Display

SECTION 1

GENERAL DESCRIPTION

The Type 30E Precision CRT Displcy shown in Figure 1-1 is an ancillary equipment designed to be used with digital computers. It is a random-position, point-plotting cathode ray tube with a control unit and power supplies mounted in a table. The equipment receives X and Y coordinate information in two ten-bit words and, on command, displays a spot of light on the screen of a cathode ray tube at this translated position. Discrete points may be plotted in any sequence at a 20 kilocycle rate (one point every 50 microseconds). Provision is made for a Light Pen to be used for identification and selection of any specific display area, and for an external monitoring oscilloscope to repeat the display.

The Type 30E Precision CRT Display consists of a 16-inch cathode ray tube in an adjustable mounting and a table with all the electronic equipment mounted beneath it. Figure 1-2 shows the outline of the equipment and the location of various panels.

TABLE 1-1 PHYSICAL SPECIFICATIONS

Dimensions	50 inches wide, 34 inches deep, 24 inch table height, 49 inches overall height.
Color	Blue and Gray Tweed unless specified.
Weight	360 pounds.
Mounting	All circuits and power supplies are mounted on or under a table. The table legs have adjustable feet for leveling, and normally support 75-100 pounds each when properly adjusted.
Clearance	Access room for maintenance requires 3 feet in the rear and 2 feet above.
Display Tube	The CRT housing can be tilted approximately 5° forward, 20° backward, and 60° sideways. Full 360° rotation is possible by removing the stop bolts. A 1/8" thick sheet of form-fitted plexiglass protects the face of the CRT.
Controls	The only operating control is a Light Pen Gain control located under the right front corner of the CRT housing.

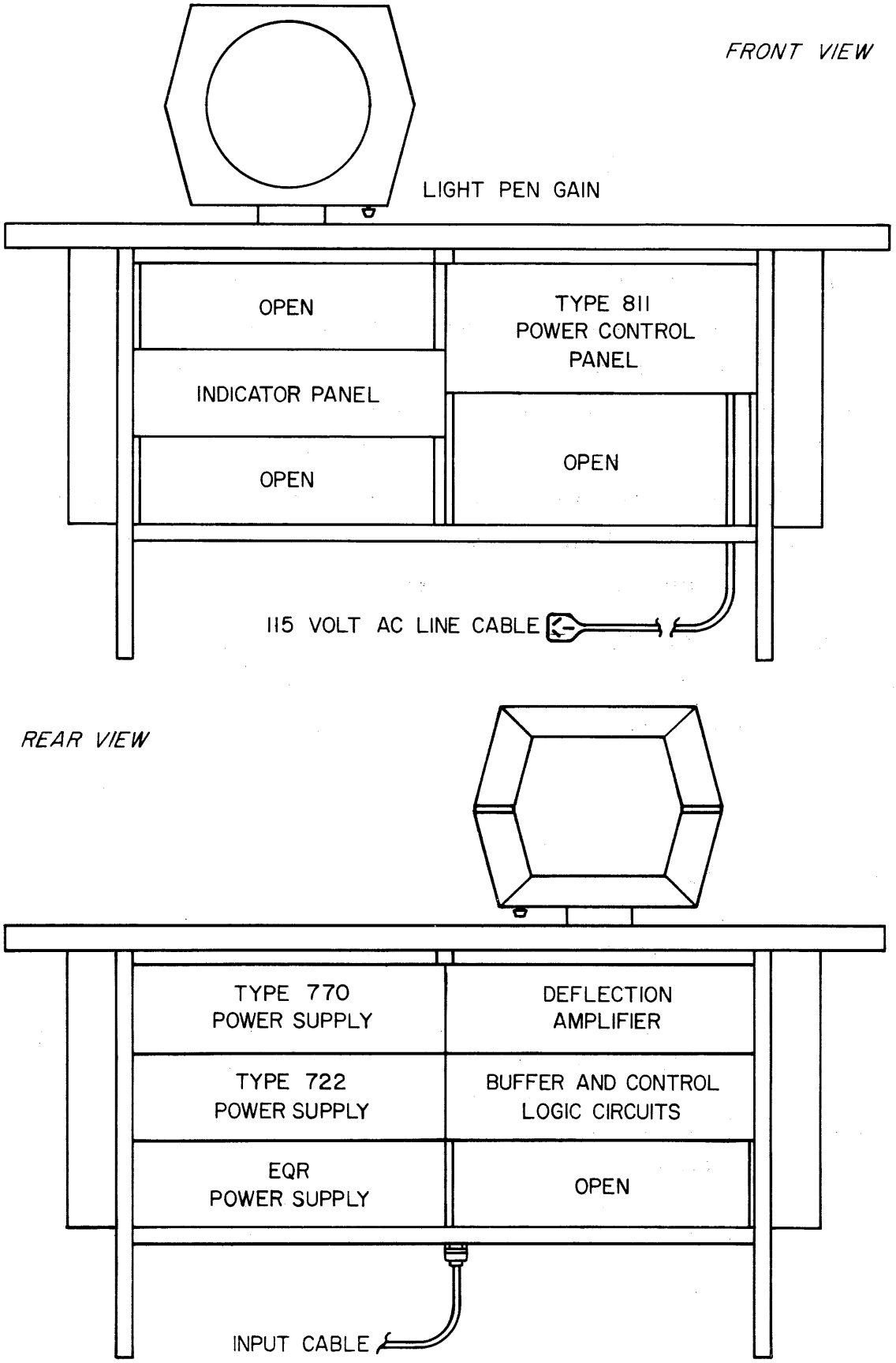


Figure 1-2 Type 30E Logic Panel and Power Supply Locations

Viewed from the front, the CRT housing is mounted on the left-hand side of the table (See Figure 1-2). The indicator panel is mounted directly beneath it under the table top. The right hand mounting area contains a Type 811 Power Control. Both the indicator panel and the power control panel are covered with easily removable trim panels.

Viewed from the rear, the mounting area contains the following equipment behind removable trim panels: On the left, a Type 770 Power Supply which supplies +10,000 volts, +250 volts, -150 volts and 6.3 volts ac to the cathode ray tube; a Type 722 Power Supply which supplies +10 volts and -15 volts to the logic circuits; and an NJE regulated 50-volt power supply* for the deflection circuits. The right hand mounting area contains a special panel in level A which holds two pluggable resistor stack assemblies and a heat sink assembly. These assemblies comprise the output stages of the two deflection amplifiers. Directly beneath in level B is the logic circuit mounting panel. The third mounting panel (level C) is left blank. Between the two lower mounting panels is the deflection reversing switch. The BNC connectors for use with an external oscilloscope are located inside the center mounting strip with the input cable socket.

The logic circuit panel and the deflection output amplifier are mounted on slides, and are connected together so they slide out as a single unit for easy access to adjustment points. The left hand side contains the horizontal coordinate channel and the right hand side contains the vertical coordinate channel.

The three switches on the left of the logic circuit panel are used with the marginal checking circuit. The two mounting boards are the compensation networks. The two capacitors are the -10 volt reference filters. The center fan cools the deflection output amplifier transistors, and has a sail (airflow actuated) switch inside the housing.

The housing on top of the table contains the CRT with its deflection yoke and focus coil and some circuitry associated with these two coils. It also contains a Type 1705 Biasing Module to provide biasing voltages for the CRT, a Type 4688 Intensification Amplifier, a socket for a Type 1559 Light Pen Amplifier, and one spare module socket.

*The NJE instruction manual for the EQR Transistorized Regulated Power Supply is a separate publication supplied with this manual. Additional copies may be procured from the NJE Corporation, 20 Boright Ave., Kenilworth, N.J.

TABLE 1-2 OPERATING SPECIFICATIONS

Input Power	115 ± 10 volts, 60 cycles, single phase, at 7 amps
Ambient Temperature	50° F (10° C) to 110° F (43° C)
Cathode Ray Tube	16ADP7A
Focus	Magnetic
Spot Size	Approximately 0.030 inch, 0.015 inch at the half light output points
Deflection	Magnetic. The electron beam is deflected by the earth's magnetic field, therefore the CRT housing should not be moved while spot position measurements are being made. External signals available
Deflection Sensitivity	0.009 inch change for change of least significant digit in address
Stability of (0,0) Point	±0.5% of raster size
Stability of Deflection System	±0.5% of raster size
Overall Accuracy	±3% of raster size overall, ±1% of raster size not including distortion due to geometry of the deflecting system and yoke
Repeatability	±0.05 inch regardless of the location of the preceding point
Addressing Scheme	1's complement, with +0 = -0 at the center of the raster for each axis. May be adjusted for 2's complement
Raster Size	9 3/8 inches by 9 3/8 inches, containing 1024 by 1024 points
Pincushion Distortion	Less than 3/16 inch per side
Timing Sequence	2.5 microseconds for address transfer, 35 microseconds for deflection setup, and 10 microseconds for spot intensification
Intensification	Normally preset. Circuits exist to allow the intensity to be controlled by the computer, with eight levels available. External signal available
Indicators	Current state of the coordinate address is shown on two rows of ten lights. A row of four lights indicates the status of the Light Pen and Intensification circuits. A single light indicates the existence of a Need-A-Completion command

CAUTION

An airflow-actuated sail switch controls the application of the 115-volt power to the equipment. Loss of cooling air will shut off the main power. Never operate the equipment without cooling air, as the deflection amplifier transistors will overheat. Replacement cost is approximately $600.

WARNING

Lethal voltages are present in this equipment. Never touch the black ring around the CRT near the front bezel (exposed on early models). Turn off all power before removing any modules.

SECTION 2

INTERFACE SIGNALS

SIGNAL DESCRIPTION

All logic signals between the computer and the display are either Standard DEC Logic Levels or Standard DEC Pulses. A Standard DEC Logic Level is either a ground (0 to -0.3 volts), indicated by an open diamond, or -3 volts (-2.5 to -3.5 volts), indicated by a solid diamond. All logic levels applied to the conditioning level inputs of capacitor-diode gates must be present for at least 3 microseconds before an input pulse is applied to the gate. The Standard DEC Pulse is either a positive-going pulse from ground (0 to -0.3 volts) to + 2.5 volts (+ 2.3 to + 3.0 volts), indicated by an open triangle, or a negative-going pulse from ground to -2.5 volts (same tolerances), indicated by a solid triangle; with a pulse width of either 1.0, 0.4, or 0.07 microsecond.

INPUT SIGNALS

Each coordinate address requires a 10-bit binary word composed of Standard DEC Logic Levels. These levels are -3 volts for logic O and ground for logic 1, except for the most-significent bits which are ground for logic O and -3 volts for logic 1. A 0.4-microsecond pulse is required to clear the two Coordinate Buffers in the Type 30, and another 0.4-microsecond pulse is required to load the coordinant addresses into the two Buffers. The load pulse must follow the clear pulse by at least 1 microsecond, and must follow the digital address words by at least 3 microseconds. Three positive Standard DEC Logic Levels or Pulses are required if the intensity level is to be controlled by the computer. These must be received within 33 microseconds after the load pulse occurs. The computer also supplies a -15 volt level to light the Need-A-Completion (NAC) indicator.

OUTPUT SIGNALS

Each Coordinate Channel of the Type 30 produces an analog output voltage that varies from -10 volts to ground directly with the numerical value of the coordinate address word. Thirty-five microseconds after the load pulse is received a -20 to -40 volt intensification level is

produced for 10 microseconds. Forty-five microseconds after the load pulse is received a 0.4-microsecond negative display completed pulse is generated.

If the Light Pen is used and if it has seen a spot during the display period, a pulse similar to the display completed pulse will be produced. This pulse will occur at the same time as the display completed pulse. In addition, a -3 volt level is produced starting at this time and lasting until the next clear pulse is received.

SECTION 3

LOGICAL OPERATION

The overall operation of the Type 30 Precision CRT Display can best be understood by reference to the block diagram, Figure 3-1. The Type 30 uses two channels for horizontal (X-axis) and vertical (Y-axis) deflection and special control circuitry for timing and intensifying the spot. The Horizontal and Vertical Coordinate Channels are similar, therefore only one channel will be described in the discussion to follow. An explanation of the drawing symbology is given in Section 5 and in the DEC Module Catalog.

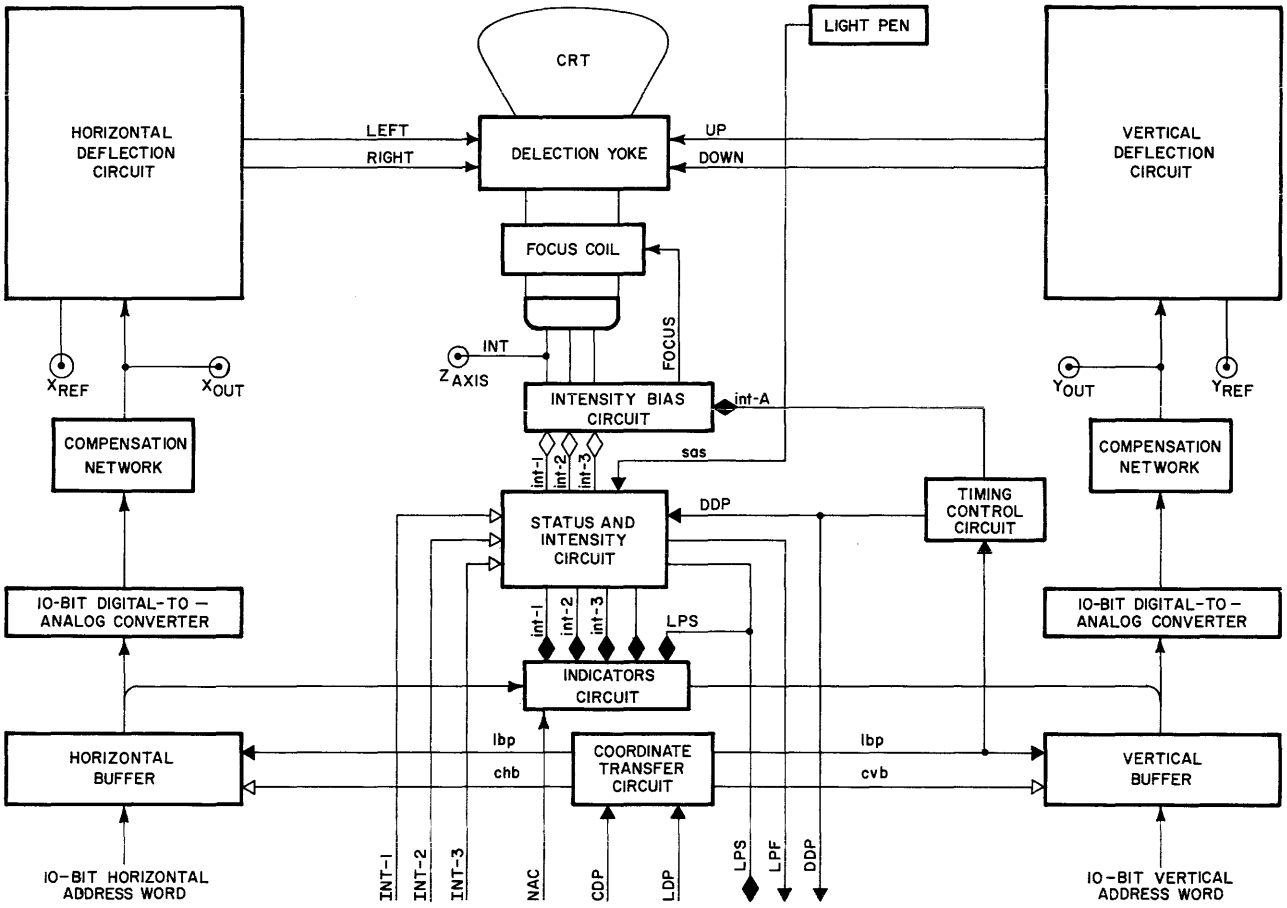


Figure 3-1 Type 30E Block Diagram

The coordinate location (address) information for the displayed spot is determined by the contents of two 10-bit binary words, one for the horizontal coordinate and one for the vertical coordinate. Each word uses the 1's complement, in which 1000000000 is -511 or the smallest number, and 0111111111 is the maximum number, +511. The bits are applied as gating levels to the two Buffers. When the Type 30 is controlled by DEC's PDP-1 computer, the two address words are applied in succession by two pairs of memory cycles.

In the next (fifth) memory cycle the computer supplies an IOT instruction which causes the clear and load pulses to be applied to the Coordinate Transfer Circuit, and usually the three intensity level bits to the Status and Intensity Circuit. The load pulse causes the two coordinate words to be transferred into the Buffers and starts the display cycle.

During the first 35 microseconds of the display cycle the output of the Buffers is converted into equivalent analog voltages and applied to separate Deflection Amplifiers through Compensation Networks. At the end of this time the CRT is unblanked for 10 microseconds and a spot of light appears on the screen at the location specified by the two coordinate address words. The intensity of the spot is controlled by the Intensity Bias Circuit.

At the end of the display cycle the Status Circuit generates a negative pulse which is returned to the computer. A second pulse and a negative level will also be generated if a Light Pen has seen the displayed spot.

COORDINATE CHANNELS

Both the Horizontal and Vertical Coordinate Channels are identical, therefore only the horizontal channel will be discussed in detail. Figure 3-2 shows a logic block diagram of both Coordinate Channels.

The information to be displayed occurs as two sets of ten bits, in which ground is a logic 1 and -3 volts is a logic O, except for the most-significant bits which are the reverse. These bits are applied to the conditioning level inputs of 10 capacitor-diode gates in each Buffer.

Clearing The Buffers - Following the computer instruction that deposits the second coordinate address word in either the Accumulator or the In/Out Register, an IOT instruction occurs in the next memory cycle. This IOT instruction causes a negative Clear Display Pulse (CDP) to occur at tp7. The CDP pulse is amplified and standardized by two pulse amplifiers in the

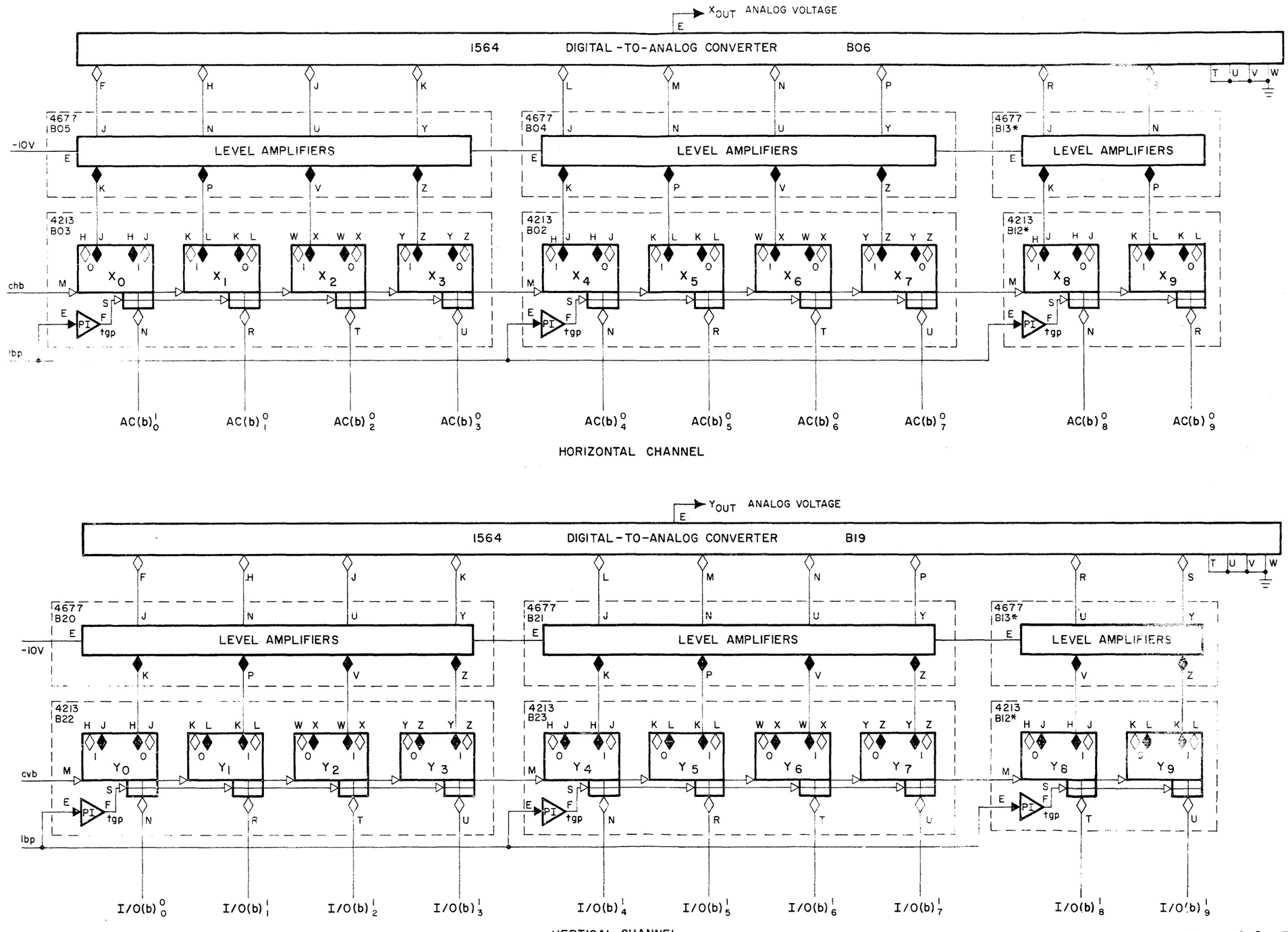


Figure 3-2 Type 30E Coordinate Channels Logic Block Diagrams

Coordinate Transfer Circuit, becoming the positive clear horizontal buffer (chb) and clear vertical buffer (cvb) pulses. These pulses are applied to the direct clear inputs of all the flip-flops in the Buffers and the Status and Intensity Circuit, setting them to their ZERO (or ONE) states. The Horizontal Buffer now holds 0111111111 (+ 511) and the Vertical Buffer now holds 1000000000 (-511). However, each flip-flop in the Horizontal Buffer produces a -3 volt output while each flip-flop in the Vertical Buffer produces a ground output, due to the reversal of the most-significant bits definition.

Loading the Buffers - In either the same or next succeeding IOT instructions, a negative Load Display Pulse (LDP) occurs at tp10. This pulse is also amplified and standardized by a pulse amplifier in the Coordinate Transfer Circuit, and becomes the negative load buffer pulse (lbp). The lbp pulse is applied to five pulse inverters, producing positive trigger gate pulses (tgp) that are applied to the trigger inputs of the 10 capacitor-diode gates in each Buffer.

Each bit in the horizontal address word which is a logic 0 (except the most-significant bit which would be a logic 1) and each bit in the vertical address word that is a logic 1 (except the most-significant bit which would be a logic 0) will apply a ground potential to the conditioning level input of its capacitor-diode gate for at least three microseconds before the LDP pulse occurs. This enables the gate and causes it to differentiate the tgp pulses. The positive signals which result are applied to the associated flip-flops, complementing them to their opposite states.

Those bits of the address words which are -3 volts disable the capacitor-diode gates and prevent the flip-flops from being complemented by the tgp pulses. Therefore at the completion of the LDP pulse each flip-flop in the Horizontal and Vertical Buffer has been set to the same state as the corresponding flip-flop in the computer's AC and I/O Registers.

Digital-to-Analog Conversion - Each 10-bit coordinate address word is converted into an analog voltage by a resistive-ladder network in a Type 1564 module. This analog voltage varies its upper and lower limits in 1024 discrete intervals, and is directly proportional to the numerical value of the 10-bit binary word from the Buffer. The upper and lower voltage limits are set by the two voltage levels of the ten input bits to the D-A Converter. The lower voltage is set at -10 volts, and is determined by a stable Type 1562 Reference Voltage Supply module. This voltage is applied to the ten Level Amplifiers, each of which apply it to the D-A Converter when the amplifier is cut off. The upper voltage is ground (approximately),

obtained by saturating the Level Amplifier. This makes each discrete interval equal to approximately 10 millivolts.

The output of each Buffer is ten bits, each at -3 volts when the Buffer holds 0111111111 (+ 511, Horizontal Buffer cleared and Vertical Buffer complemented) and at ground when the Buffer holds 1000000000 (-511, Horizontal Buffer complemented and Vertical Buffer cleared). This is a 10-bit binary word in which ground is logic O and -3 volts is a logic 1.

Each Level Amplifier is cut off when its input is at ground and is saturated when its input is at -3 volts. Therefore the analog voltage is ground, its most positive value, when the Buffer holds + 511 and is -10 volts, its most negative value, when the Buffer holds -511. This represents deflection to the extreme top or right-hand side, and to the extreme bottom or left-hand side, respectively. Table 3-1 shows the relationships between the coordinate address words, flip-flop states, D-A conversion, and deflection.

TABLE 3-1 COORDINATE CHANNEL LOGIC CONVERSION TABLE

Digital Address and Flip-Flop States	Buffer Output and Level Amplifier Input	Level Amplifier Output and D-A Converter Input	Digital-to-Analog Converter Output
O111111111	xxxxxxxxxx	0000000000	most positive (ground)
O111111110	xxxxxxxxx0	000000000X	
⋮	⋮	⋮	⋮
OOOOOOOO01	x00000000x	0XXXXXXXX0	
OOOOOOOOOO	x0000000000	0XXXXXXXXX	
1111111111	0xxxxxxxxx	X000000000	
1111111110	0xxxxxxxx0	X00000000X	
⋮	⋮	⋮	⋮
1OOOOOOOO1	000000000x	XXXXXXXXX0	
1OOOOOOOOO	0000000000	XXXXXXXXXX	most negative (-10 volts)
O = logic zero = ZERO state 1 = logic one = ONE state	0 = ground x = -3 volts	0 = ground X = -10 volts	Positive = up = right Negative = down = left

side, respectively. Table 3-1 shows the relationships between the coordinate address words, flip-flop states, D-A conversion, and deflection.

The accuracy, or linearity, of the analog address voltage with the coordinate address is determined by the D-A Converter adjustment, and is approximately ±1 millivolt per bit. This adjustment is necessary to correct for the slight resistance differences of the resistive ladder network and the saturation resistance of each Level Amplifier. If any part of a resistive ladder network or a Level Amplifier is changed, the D-A Converter must be readjusted as described in Section 4.

The value of the analog address voltage will not reach its final value for approximately 2 microseconds after the LDP pulse occurs. This is due to the delays in the pulse amplifiers, the flip-flops, the Level Amplifiers, and the ladder networks. This time is part of the deflection setup delay, which also includes the compensation time. The analog address voltage is available at a BNC connector for external use, along with the reference voltage for preamplifier.

DEFLECTION CIRCUITS

Both the Horizontal and Vertical Deflection Circuits are identical, therefore the description that follows applies equally to both circuits. Figure 3-3 shows the logic diagram for these circuits.

Basically, the Deflection Circuit consists of a Compensation Network, a Deflection Preamplifier, a Deflection Output Amplifier with a stack of associated Precision Resistors, a Reversing Switch (in the Type 30M only), and a pair of Deflection Coils. The electron beam is deflected by a magnetic field produced by the dc currents flowing in the two opposing Deflection Coils. This circuit acts as a stable and linear operational amplifier, permitting the compensation needed for correction of the yoke's undershoot to be introduced at the inputs.

Compensating - When the coordinate address is changed, a voltage step is produced in the analog address voltage. Since abrupt changes of the current in the Deflection Coils would produce ringing and the spot would oscillate, the Deflection Coils are damped. The amount of damping used is slightly less than critical in order to minimize the deflection setup delay time.

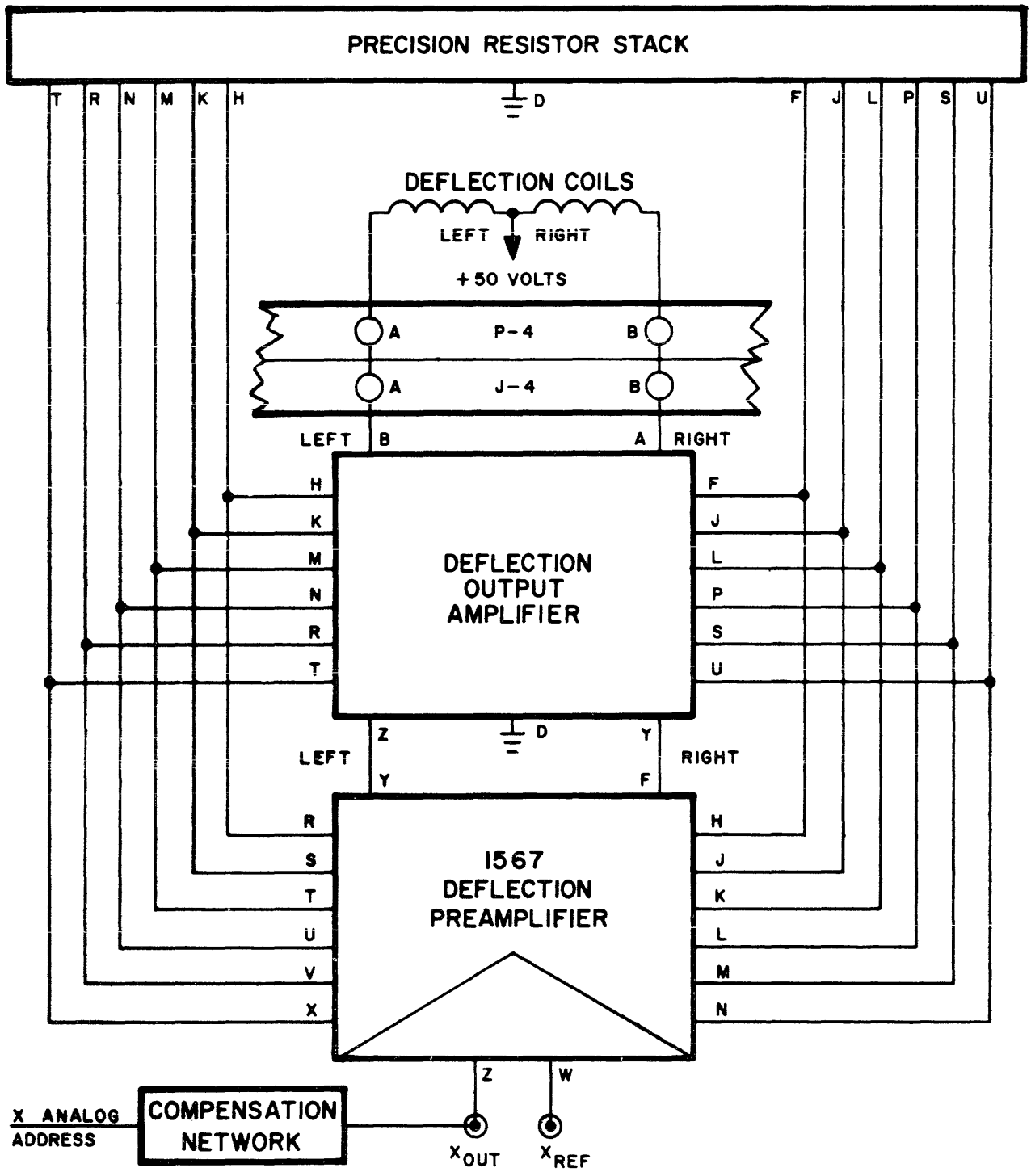


Figure 3-3 Deflection Circuit Block Diagram

An abrupt voltage change to the Deflection Preamplifier does not cause an abrupt change in the deflection current due to the large inductance of the Deflection Coils. Instead, the current changes semilinearly from its previous value to a value close to that desired, as shown in

Figure 3-4. Because of the coupling between the Focus Coil and Deflection Coils and the hysteresis of the paramagnetic items in close proximity to the coils, the magnetic field does not completely stabilize at its final value. For about 150 microseconds after the change of address, a slightly uncertain undershoot value exists that is a little less than the required value. Therefore a Compensation Network is used to introduce some initial overshoot into the coordinate address change.

The Compensation Network is a simple RC circuit with a time constant of about 0.1 millisecond that applies a signal to the preamplifier which is initially much greater than required and which decreases exponentially toward that value. This overshoot causes the magnetic field to approximately reach its required value by the end of the 35-microsecond deflection setup delay. The overshoot is a fixed percentage, while the undershoot varies somewhat depending upon the previous address; therefore the compensation is not exactly complete. However, with proper adjustment of the Compensation Network, the resulting spot movement will be negligible for most applications.

Amplifying - The compensated analog address voltage is applied to terminal Z of the Deflection Preamplifier, and a stable -10 volts is applied to terminal P. This latter potential is divided in half to produce a -5 volt reference voltage, available as X_{REF} at terminal W. These two voltages are the inputs to a differential amplifier.

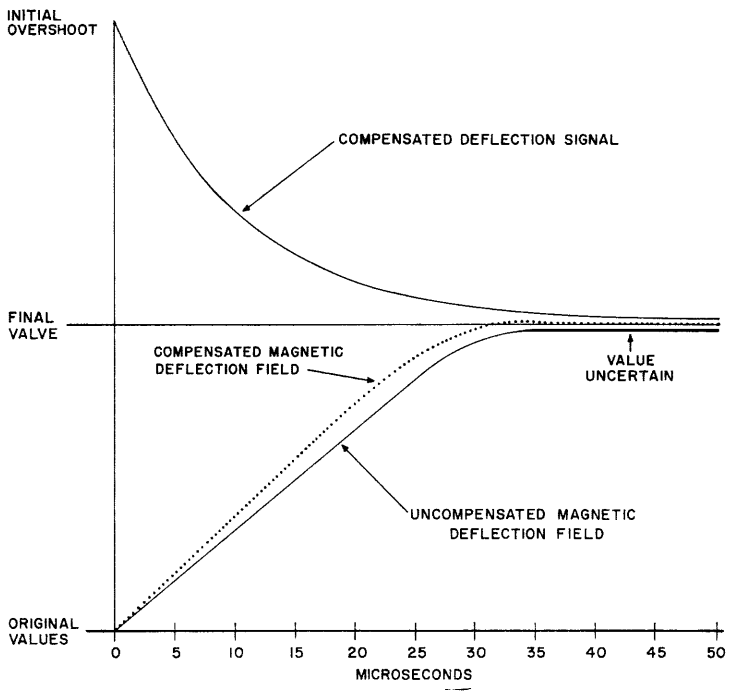


Figure 3-4 Deflection Compensation Characteristics

The differential amplifier compares the analog voltage with the reference voltage and produces two outputs which are proportional to the difference between the two inputs. Both of these outputs vary from a common reference potential (approximately +4 volts) by the same amount but in different directions, one going positive while the other goes negative.

The two outputs of the Preamplifier are applied to the Deflection Output Amplifier; each signal controlling the conduction through a separate amplifier channel. The deflection current flows through a stack of Precision Resistors, the amplifier channel, and Deflection Coil. The Precision Resistors develop a negative feedback voltage that is applied to the Preamplifier to increase the stability of the circuit. The Deflection Output Amplifier and Precision Resistor Stack utilize forced air for cooling. Zener diodes across the Deflection Coils prevent the back emf developed by changing an address from burning out a Deflection Output Amplifier.

> NOTE: Loss of cooling air will result in burning up an expensive assembly. Never operate the equipment if the fans or sail switch fail.

CONTROL AND TIMING CIRCUIT

The Control and Timing Circuit consists of the Coordinate Transfer Circuit and the Timing Control Circuit, shown in Figure 3-5. The Coordinate Transfer Circuit generates the pulses which clear and load the Buffers and the Status and Intensity Circuit, as well as initiating the Timing Control Circuit's operation.

Coordinate Transfer Circuit

Clear Pulses - When the computer wants to clear the Buffer, it applies a Clear Display Pulse (CDP) at tp7 to two inverters in a Type 4603 Pulse Amplifier module. The inverters then conduct and activate two pulse amplifiers, producing positive clear horizontal buffer (chb) and clear vertical buffer (cvb) pulses which are applied to the flip-flops in the Horizontal and Vertical Buffers. The cvb pulse is also applied to the flip-flops in the Status and Intensity Circuit. The clear pulses are divided in order to provide the required driving power for the large number of flip-flops. Each pulse clears 12 flip-flops, the chb pulse also clearing the two less-significant flip-flops in the Vertical Buffer.

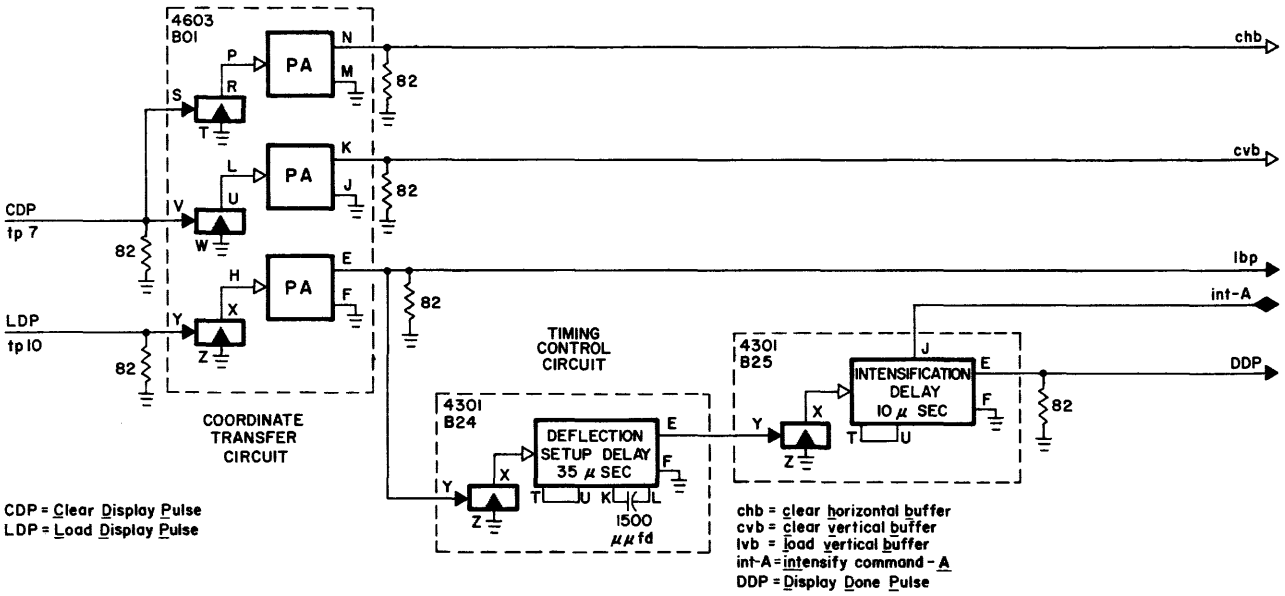


Figure 3-5 Control and Timing Circuit Logic Block Diagram

Load Pulse - Approximately 2.2 microseconds after the CDP pulse, the computer supplies a Load Display Pulse (LDP) at tp10. This pulse is also applied to an inverter in the Type 4603 Pulse Amplifier module, causing the inverter to conduct and activate a pulse amplifier which produces a negative load buffer pulse (lbp). This pulse is applied to the pulse inverters in both Buffers (causing the coordinate address words to be loaded into the Buffers) and to the Timing Control Circuit (initiating the display cycle).

Timing Control Circuit

The lbp pulse is applied to an inverter in a Type 4301 Delay module, producing a positive pulse that initiates the 35-microsecond deflection setup delay period. While the Deflection Setup Delay is timing out the coordinate address words are loaded into the Buffers, converted into equivalent analog voltages, and develop currents to deflect the electron beam. The length of time is determined by the transfer time of the Buffers, D-A conversion time, response time of the amplifiers, and primarily the characteristic time of the Deflection Coils and Compensation Networks.

At the end of the 35-microsecond period the Deflection Setup Delay produces a negative pulse that is applied to an inverter in another Type 4301 Delay module. Again, the inverter conducts and initiates a 10-microsecond intensify delay. While the Intensification Delay is timing out a -3 volt intensify-A (int-A) level is produced which causes the Intensity Bias Circuit to unblank the CRT. At the end of the 10-microsecond period a negative Display Done Pulse (DDP) is produced and returned to the computer. The DDP pulse is also used by the Status and Intensity Circuit to produce a pulse and light an indicator if the Light Pen saw the pulse.

STATUS AND INTENSITY CIRCUIT

The Status and Intensity Circuit shown in Figure 3-6 generates a negative pulse and level and lights an indicator when the Light Pen sees the displayed spot. The circuit also contains the Intensity Buffer that selects the intensity level of the displayed spot. Because the four flip-flops are cleared by the cvb pulse each time a CDP command occurs, the Intensity Buffer must be reloaded before the end of the deflection setup delay.

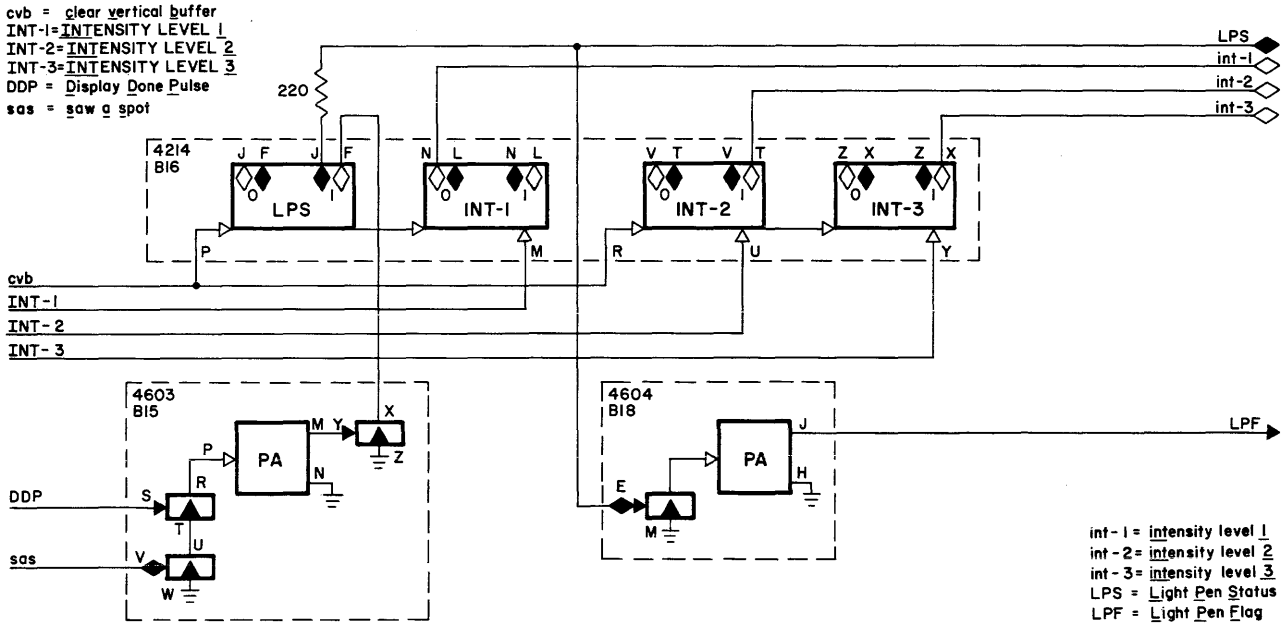


Figure 3-6 Status and Intensity Circuit Logic Block Diagram

Light Pen Status - At the end of each display cycle a negative Display Done Pulse (DDP) is applied to an inverter gate in a Type 4603 Pulse Amplifier module. This inverter gate is controlled by another inverter which receives the light pen gate signal. When a Type 32 Light Pen is used and the pen sees the displayed spot, it produces a -3 volt saw a spot (sas) level

during and slightly after the spot's display period. This turns on the inverter, enabling the inverter gate and allowing the DDP pulse to activate the pulse amplifier. The pulse amplifier turns on a third inverter which complements the Light Pen Status Flip-Flop, thereby producing a negative Light Pen Status (LPS) level that is returned to the computer.

The LPS level is also applied to another inverter in a Type 4604 module which conducts and activates a pulse amplifier. This pulse amplifier produces the positive Light Pen Flag (LPF) which is returned to the computer.

Intensity Buffer - Eight different levels of intensity are possible with the Type 30. These levels correspond with the numerical value of a 3-bit 1's complement binary word supplied by the computer. The Intensity Buffer stores this word from its application til the next CDP command occurs. The intensity word must be applied within 33 microseconds after the LDP command occurs to allow the intensity bias to be set before the deflection setup delay ends. Table 3-2 shows the correlation between the intensity word, flip-flop states and outputs, and relative intensity levels.

The flip-flops are changed from their ZERO state to their ONE state by the application of a +2.5 volt pulse (or level). Since the most-significant bit in the intensity word is reversed, the output of the flip-flop is also reversed. This allows the intensity to automatically be set just above the median level if no input signal is received.

TABLE 3-2 INTENSITY CORRELATIONS

Octal Number and Relative Intensity	Input Signal			Flip-Flop States			Output Signal		
	bit 1	bit 2	bit 3	bit 1	bit 2	bit 3	bit 1	bit 2	bit 3
0	+	0	0	1	0	0	-	-	-
1	+	0	+	1	0	1	-	-	0
2	+	+	0	1	1	0	-	0	-
3	+	+	+	1	1	1	-	0	0
4	0	0	0	0	0	0	0	-	-
5	0	0	+	0	0	1	0	-	0
6	0	+	0	0	1	0	0	0	-
7	0	+	+	0	1	1	0	0	0
0 = dimmest	0 = ground			0 = logic 0			0 = ground		
7 = brightest	+ = +2.5 volts			1 = logic 1			- = -3 volts		

INTENSITY BIAS CIRCUIT

The Intensity Bias Circuit, Figure 3-7, is located in the CRT housing. It includes a Type 1705 Bias and Focus module and a Type 4688 Variable Amplitude Intensifier module. These modules, along with a Type 1559 Light Pen Amplifier and any other that may be in the spare socket, constitute level D for location purposes.

Intensifying - While the Intensification Delay is timing out, the negative int-A signal is applied to a negative NOR gate in a Type 4688 Variable Amplitude Intensifier module. This turns on a variable intensity bias circuit, whose output, the INTensity (INT) command is ac coupled to the cathode of the CRT. Normally the INT signal is at ground, but during the 10-microsecond intensification delay period it goes to some value between -20 and -35 volts, depending on the intensity level inputs. This reduces the bias and unblanks the CRT, allowing a spot of light to appear on the screen at the coordinate location specified by the two address words.

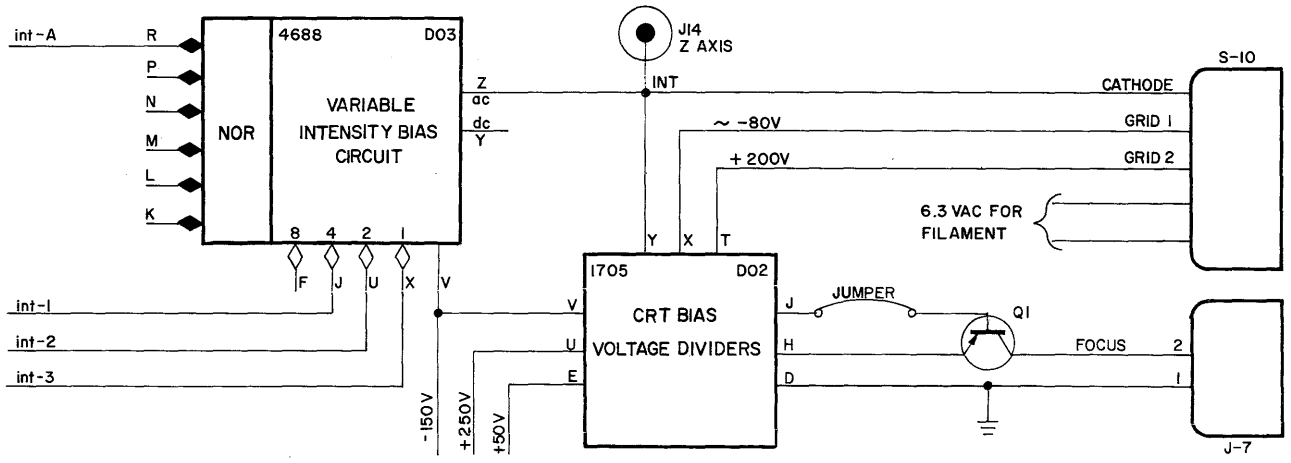


Figure 3-7 Intensity Bias Circuit Logic Block Diagram

Intensity Levels - The dc bias potentials for the CRT grids are developed in the Bias and Focus module by Zener diode voltage dividers. Grid 2 is kept at +200 volts, while grid 1 is normally kept at approximately -80 volts. The latter potential can be adjusted from 0 to -120 volts to adjust the intensity level. Two diodes connect the cathode to the grid so that the cathode can never go more negative than the grid.

CAUTION

Repeated and/or intensely bright intensifications can burn a hole in the screen of the CRT, ruining an expensive tube.

When the CRT is blanked the cathode is at ground. In order to unblank the CRT and produce a spot of light, it is necessary to apply a -3 volt enabling potential to any one of the six NOR inputs. This potential turns on an inverter which enables the variable intensity bias circuit. The INT signal is capacitively coupled to avoid ruining the CRT in the event of a malfunction. A Z axis BNC connector makes the INT signal available for external use.

The intensity bias circuit is capable of providing 16 different potentials for the cathode, depending on the binary number present on terminals F, J, U, and X. The Type 30 uses only the three less-significant bits of this number, providing eight intensity levels. When the number is 7 (all grounds), the cathode potential is -35 volts and a bright spot is displayed. When the number is 0 (all -3 volts) the cathode potential is about -20 volts, giving a dim spot.

Focus - The CRT is focused magnetically by a constant current through a Focus Coil. This current is controlled by a focus transistor, Q1, which in turn is controlled by a fixed voltage from the Type 1705 Bias and Focus module's focus voltage divider. A potentiometer allows the current in the focus transistor to be adjusted if necessary.

INDICATORS CIRCUIT

Twenty-five incandescent lamps are used in the indicator panel. All but one of these indicate the state of various flip-flops in the equipment, glowing when the flip-flop holds a ONE and dark when the flip-flop holds a ZERO. The exception is the Need A Completion (NAC) indicator which is lighted when the computer requests a signal at the end of the display process. This lamp is energized directly by -15 volts from the computer.

All the other lamps are energized by -15 volts from an indicator driver. Nine of these are contained in each driver module, and each one is actuated by a -3 volt signal from the 1 output of a flip-flop when the flip-flop is in the ONE state.

ELECTRICAL POWER

The primary power for the equipment is 115 volts, 60 cycles, single phase. This is applied to a 20 amp, 2 pole circuit breaker located on the Type 811 Power Control panel. From the circuit breaker the 115 volt power goes to the ac power control circuit, to the cooling fans, and through the contacts of relay K1 to the dc power supplies.

One side of the ac line from the circuit breaker goes to the coil of K1 and to the cooling fan motors. The other side of the ac line goes to the normally-open contact of an airflow-actuated sail switch (operated by the central cooling fan) and to contacts on relay K2. When K2 is energized, the cooling fans are energized. When the fans come to speed, the sail switch will close and relay K1 will be energized, thereby applying the ac power to the dc power supplies.

The ac power from relay K1 is applied to the Type 722 Power Supply. An outlet on the Type 722 supplies the ac power to the Type 770 Power Supply. Similarly, the Type 770 supplies the ac power to the NJE EQR 60-6 Power Supply.

> NOTE: Some equipments may use a Type 721 Power Supply instead of a Type 722.

The Type 722 (or Type 721) Power Supply provides the +10 volts and -15 volts DC for the logic circuits. Refer to the DEC Module Catalog for complete specifications.

The Type 770 Power Supply provides the high voltage and filament power for the CRT. Its outputs include + 10,000 volts DC, +250 volts DC, -150 volts DC, and 6.3 volts AC.

WARNING

> Lethal voltages are present when the Type 770 Power Supply is energized. Exercise extreme caution working inside the equipment when it is turned on. The black ring around the CRT near the front bezel (exposed on early models) must never be touched or closely approached with power on.

The Model EQR 60-6 Power Supply provides the 50 volt deflection power for the CRT yoke. It must normally be adjusted for 50 volts output and 80% maximum current. Refer to the NJE manual for complete specifications.

NOTE: If the individual power supplies are turned on and off separately, be sure that the EQR 60-6 Power Supply is not turned on when the Type 722 is turned off. If the EQR 60-6 is used without the Type 722, it will overconduct and to into its current-limiting mode.

SECTION 4

MAINTENANCE

SPECIAL TOOLS AND TEST EQUIPMENT

The following special tools and test equipment are recommended for efficient maintenance and realignment of the Type 30. If the specified item is not available, an equivalent substitute may be used.

TABLE 4-1 SPECIAL TOOLS AND TEST EQUIPMENT

Multimeter	Simpson Model 260A or Triplett Model 630NA
Oscilloscope	Tektronix 540 series
Preamplifiers	Type L Preamplifier of 5 mv/cm sensitivity
Oscilloscope Probes	Tektronix P-6002 Shielded cable direct probe with subminiature alligator clips
Module Extractor	DEC Type 1960
Module Extender	DEC Type 1954
Soldering Iron	General Electric V6 W25 YT, cat. 6A210
Screwdriver	Xcelite R-3324

ASSEMBLY AND DISASSEMBLY

Logic Modules - All logic modules may be easily removed by unplugging them from their racks. Access to the modules is gained by opening the rear door of bay 2. A Type 1960 Module Extractor should be used when removing any logic module.

> NOTE: When removing or replacing a module, be sure all power is turned off.

Deflection Output Amplifier - The resistor stacks and the deflection output amplifier heat sink assembly may be unplugged after the 110-volt power to the fans has been removed. Two mounting screws on the wiring side of the panel must be loosened before the resistor stacks and the

heat sink can be removed. The resistor stacks must be removed before the heat sink module can be removed.

Cathode Ray Tube - The front bezel and the CRT mounting assembly that holds the yoke and focus coil must be removed from the bottom of the shroud by unscrewing the four underneath hold-down screws (two at the bezel and two at the rear of the assembly) and the two screws that hold the mounting assembly to the sides of the shroud. Once removed, the assembly should be set up on blocks with the CRT face down and the four bolts that hold the CRT mounting assembly to the bezel removed. The yoke and focus coil assembly is removed by unscrewing the three bolts that spring-load it on the CRT mounting assembly. The CRT is removed by loosening the screws which hold the clamps that secure the tube to the front bezel. The CRT mounting assembly can then be removed from the front bezel.

To replace the tube, place it face down on the plexiglass shield in the bezel. Place the CRT mounting assembly over the tube and bolt it down. Place the yoke assembly very carefully over the tube and bolt it down. Place the yoke assembly very carefully over the neck of the tube, and at the same time align the tube with the yoke. When the tube has been aligned, it should be possible to move the yoke back and forth without scraping the neck of the tube. Next, tighten down the tube clamps. Then install the hold-down screws for the yoke and focus coil assembly.

ADJUSTMENTS

Light Pen Gain - Located underneath the right front of the CRT housing. Clockwise rotation increases gain.

Electrical Adjustment

Digital-to-Analog Converters - If any level amplifiers in either the Horizontal or Vertical Deflection Channels have their output transistors replaced, or if the module itself is replaced, the Digital-to-Analog Converters associated with that channel will have to be adjusted. The procedure for adjusting these D-A Converters is as follows:

(a) Turn off the main ac power to the Type 30.

(b) Remove the affected module with a Type 1960 Module Extractor. Insert a

1954 Module Extender into the space in the rack, and then replace the D-A Converter in the extender.

(c) Remove the Type 1567 Deflection Preamplifier associated with the D-A Converter being adjusted.

(d) Individually turn off the Deflection and Ultor Voltage Power Supplies (EQR and Type 770). The main ac power may now be turned on.

(e) Program the computer to alternately display the most negative number (0000000000) and the next less negative number (0000000001). This will alternately switch the least significant digit (bit 9) between its two states. Refer to Tables 3-1 and 4-2 for computer and converter states.

TABLE 4-2 10-BIT DIGITAL-TO-ANALOG CONVERTER ADJUSTMENT

DIGITAL INPUT TO BUFFER										OUTPUT CHANGE (millivolts)
bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8	bit 9	
0	0	0	0	0	0	0	0	0	1	} Δ1 _____
0	0	0	0	0	0	0	0	0	0	
0	0	0	0	0	0	0	0	1	0	} Δ2 _____
0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	1	0	0	} Δ3 _____
0	0	0	0	0	0	0	0	1	1	
0	C	0	0	0	0	1	0	0	0	} Δ4 _____
0	0	0	0	0	0	0	1	1	1	
0	0	0	0	0	1	0	0	0	0	} Δ5 _____
0	0	0	0	0	0	1	1	1	1	
0	0	0	0	1	0	0	0	0	0	} Δ6 _____
0	0	0	0	0	1	1	1	1	1	
0	0	0	1	0	0	0	0	0	0	} Δ7 _____
0	0	0	0	1	1	1	1	1	1	
0	0	1	0	0	0	0	0	0	0	} Δ8 _____
0	0	0	1	1	1	1	1	1	1	
0	1	0	0	0	0	0	0	0	0	} Δ9 _____
0	0	1	1	1	1	1	1	1	1	
0	0	0	0	0	0	0	0	0	0	} Δ10 _____
1	1	1	1	1	1	1	1	1	1	

$\frac{\Delta 1 + \Delta 2}{2}$ = _____ = _____ millivolts
2

(f) Connect the direct probe from the horizontal input of the oscilloscope to terminal E of the module being adjusted. Set the oscilloscope for 5 mv/cm vertical dc sensitivity and internal sync.

(g) Adjust the oscilloscope time base so that two horizontal lines appear on the screen. Measure the voltage difference of these two lines as well as possible and record this value as Δ 1 (see Table 4-2). This voltage should be approximately 10 millivolts.

(h) Program the computer to alternately switch the next less significant digit (bit 8). Measure the difference of the two horizontal lines and record this value as Δ 2.

(i) Add the values of Δ 1 and Δ 2, and divide by 2 to obtain the average change per bit. Record this value. These bits are not adjustable, and the differences

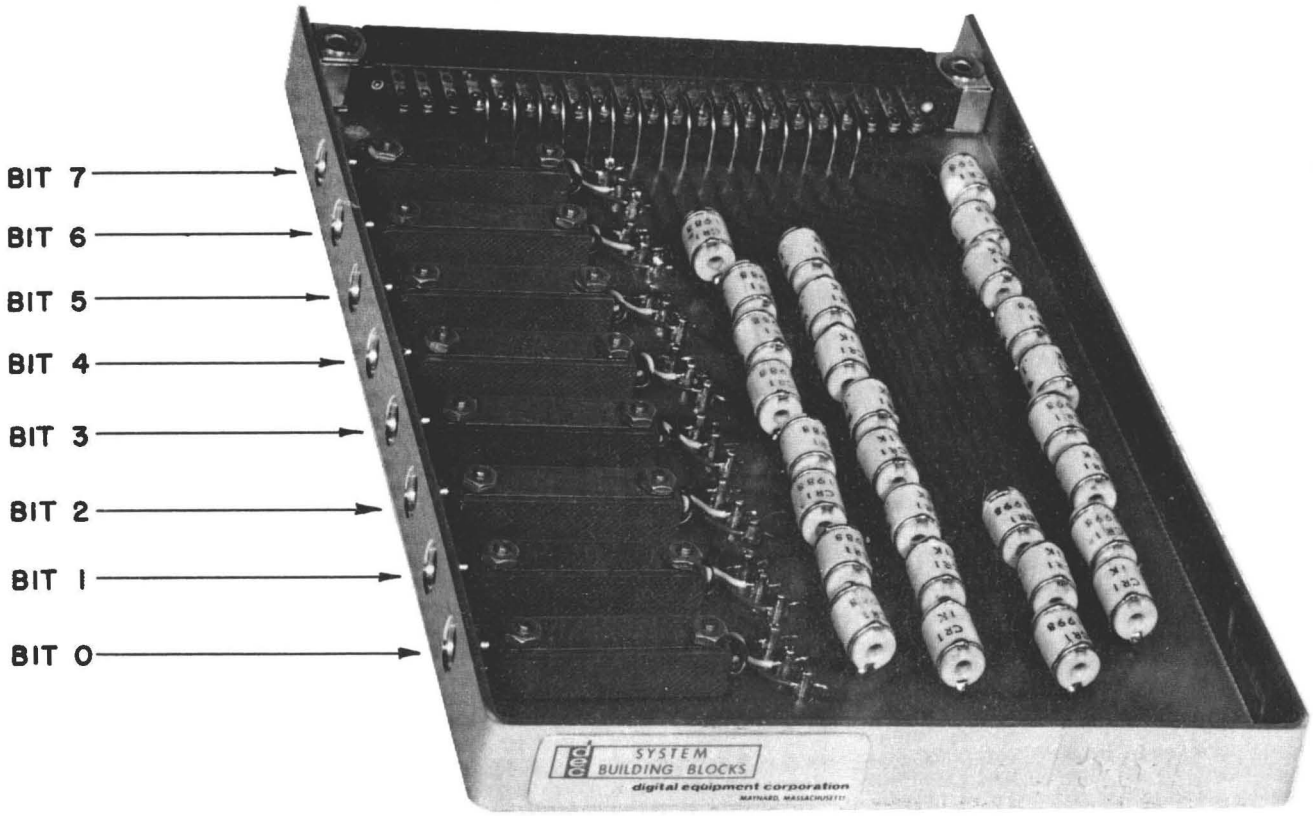


Figure 4-1 Type 1564 Adjustment Locations

between them are caused by the slight differences in tolerances in both the D-A converter and the level amplifier output transistors. If these two values are not close (±1 millivolt), check both circuits for a malfunction.

(j) Program the computer to alternately switch bit 7 and bits 8 and 9, and note the voltage difference of the two lines. If this voltage is different from the average value of the unadjustable bits, adjust the potentiometer behind the hole nearest the plug end of the module. See Figure 4-1 for the adjustment locations.

(k) Repeat step (j) for each bit in turn. Each bit must be adjusted for the same value.

NOTE: If any bit cannot be adjusted, especially the more significant bits, it is necessary to assume a slightly different value for the average of $\Delta 1 + \Delta 2$; then readjust all the adjustable bits in turn for this value.

Raster Position - The raster should be located in the center of the CRT screen. If it is not, it may be moved by the following procedure:

(a) Program the computer to display vertical and horizontal lines along each edge of the raster.

(b) Adjust potentiometer R2 (center hole, Figure 4-2, in the Type 1567 module located in B17) to center the vertical lines.

(c) Adjust potentiometer R2 in the Type 1567 module in location B08 to center the horizontal lines.

Raster Size - The size of the raster on the face of the CRT should be nine and three-eighths inches per side. It may only be adjusted after the raster is centered. The raster size is adjusted in the following manner:

(a) Program the computer to alternately display the most positive and most negative horizontal lines (see Table 3-1). Measure the distance between these lines at their center.

(b) Adjust potentiometer R16 (lower hole, Figure 4-2) in the Type 1567 module located in B17 for nine and three-eighths inches between the midpoints of the two horizontal lines.

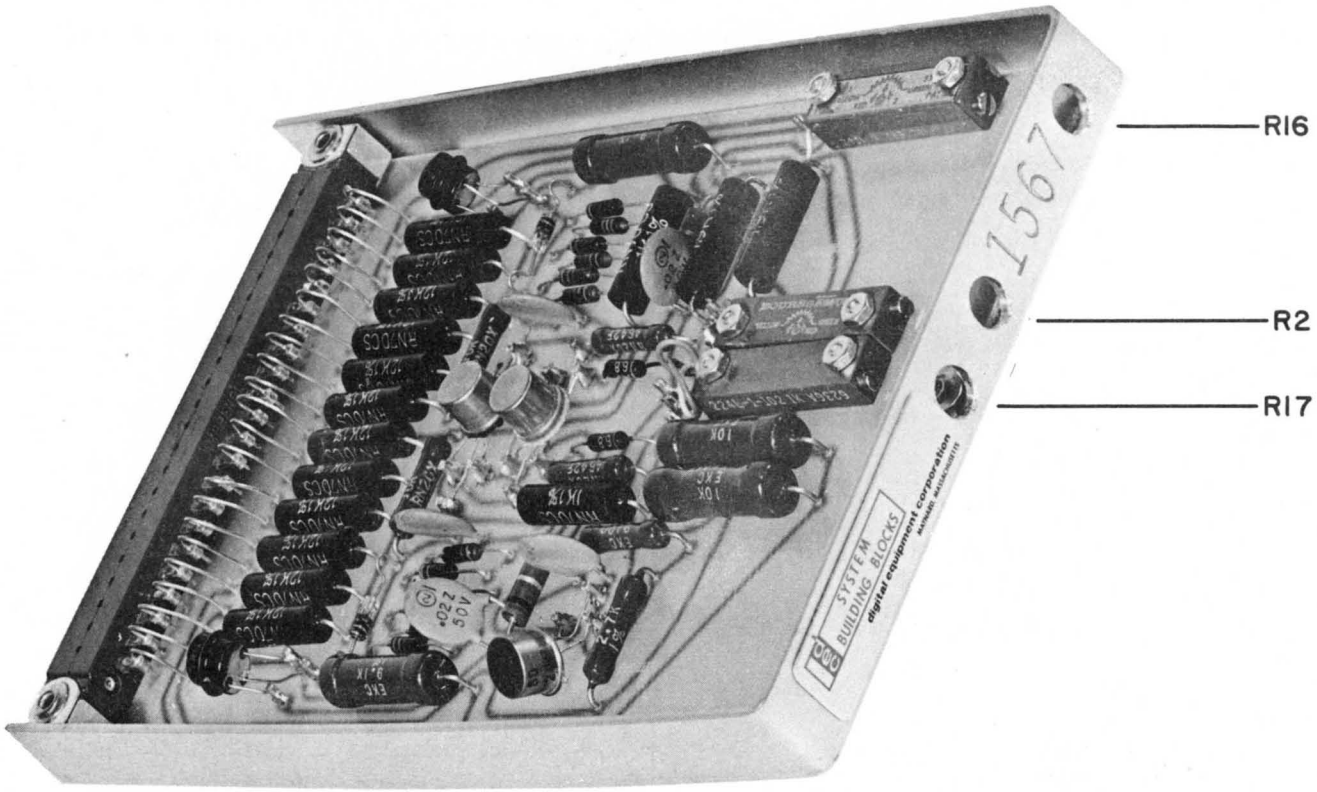


Figure 4-2 Type 1567 Adjustment Locations

(c) Program the computer to alternately display the most positive and most negative vertical lines. Measure the distance between these lines at their center.

(d) Adjust potentiometer R16 in the Type 1567 module located in B08 for nine and three-eighths inches spacing between the midpoints of the two vertical lines.

Common Mode - If a Type 1567 Deflection Preamplifier module is replaced, it may be necessary to adjust its common mode current. This may be done by the following procedure:

(a) Program the computer to alternately display the most positive and most negative addresses in both the horizontal and vertical positions at the dimmest intensity level.

(b) Connect an oscilloscope to terminals F or Y on the Type 1567 module. The two voltage levels present should be approximately +0.5 volts and +6 volts.

(c) If the voltage range is greater than this, adjust potentiometer R17 (upper hole, Figure 4-2) so that the lower voltage is 0.5 volts minimum.

CAUTION

If the higher voltage range is too great (approximately +7 volts), the deflection amplifiers may be burned up.

Brightness - The relative brightness of all displayed intensity levels is controlled by the cathode-to-grid 1 bias. To vary the relative brightness, the following procedure is used:

(a) Program the computer to display eight separate lines on the CRT, each line at a different intensity level.

(b) Adjust the bias control potentiometer R3 (lowest control) on the Type 1705 module in D02 for the best levels of intensity.

CAUTION

Reducing the grid bias by too great an amount will produce an extremely bright spot on the screen of the CRT, which can burn a hole in the screen.

Delay Time - The variable delay of the Type 4301 modules may be adjusted as follows:

(a) Connect an oscilloscope (set for dc input and negative internal sync) to terminal J of the module to be adjusted.

(b) Trigger the delay with the program or by connecting a 0.01 microfarad capacitor (which has previously been shorted) between terminal X and ground. A -3 volt level should be observed for the required duration.

(c) To change the duration of the delay, adjust potentiometer R7 through the access hole in the back of the module.

(d) With the oscilloscope adjusted to be triggered with the delay trigger, connect the probe to terminal E and check for a -3 volt pulse starting at the end of the delay period.

Focus - The focus of the spot may be adjusted by changing the current through the Focus Coil as follows:

(a) Program the computer to display the two alternate diagonals on the screen of the CRT. Observe the focus along each line, especially at the corners and the center.

(b) Adjust potentiometer R5 (bottom rear) in the Type 1705 module in D02 for the best focus over the entire tube face. If astigmatism is present, adjust the alignment of the Focus Coil.

Mechanical Adjustments

Focus Coil - The focus coil may be moved in any direction by the adjusting screws provided. It can move in or out, tilt in either direction, and move sideways. It should require adjustment only when a CRT has been replaced. In order to align the focus coil correctly, the short brown jumper on the mounting plate in the bottom of the CRT housing should be removed and a sinusoidal signal (such as that obtained from an audio oscillator) connected in its place. This will cause the focus current to vary rapidly, focusing and defocusing the spot so that the concentricity of the focused and defocused spot can be observed. When the coil is perfectly aligned, the focused and defocused spots should be perfectly concentric. There should be no circular motion as the spot changes from its unfocused to focused condition. The coil need not be perfectly aligned for most applications.

Deflection Yoke - The deflection yoke adjustment affects only the angular position of the display on the tube face. The three aluminum clamps holding the yoke may be loosened to rotate the display. It should only require adjustment when the CRT has been removed.

PERIODIC MAINTENANCE

Clean the Rotron fan filters in the deflection and focus output amplifiers once a month with soapy water. Spray with Filter-Kote (Research Products Corporation, Madison, Wisconsin) or equivalent.

Clean dust from the Deflection Output Amplifier Heat Sink and Resistor Stacks once every six months.

Check accuracy of ladder decoder alignment as desired. These should require readjustment only when a level amplifier module is replaced, or once every six months. See decoder adjustment procedure, page 4-4.

Refer to the NJE manual for maintenance requirements of the EQR 60-6 power supply.

TROUBLESHOOTING

An understanding of operation of the equipment as described in Section 2 should allow many malfunctions to be isolated to a particular circuit or component. Further isolation may then be accomplished with the schematic diagrams in Section 5. When troubles do occur, it is most advantageous to trace each signal path from input to output and compare the signals observed with the Standard DEC Signal for both shape and timing.

Some of the possible malfunctions do not lie in the logic circuitry and cannot be found by the standard deductive process. Those peculiar malfunctions which affect the beam are listed in Table 4-3 below.

TABLE 4-3 POSSIBLE CRT BEAM MALFUNCTIONS

Symptom	Probable Cause
Beam deflects over one half axis only.	Possible shorted Deflection Output Amplifier transistor (2N1719) or open lead in deflection yoke cable.
Some locations on tube face cannot be addressed, i.e., missing spots in a line.	Check Buffer Register, Level Amplifiers and Decoder adjustments for the axis involved.
Ripple, jitter, or other size changes that occur at edges of screen but not in center.	Defective high voltage power supplies.
Spots appear elongated. Trouble is most apparent when two successive points are widely separated.	Deflection setup delay is shorter than the required 35 microseconds, or yoke damping resistor open.

If any malfunction ever occurs, enter both the symptoms and remedy in Table 4-4. Be explicit and write clearly so that someone else may later read and understand the history.

TABLE 4-4 SPECIFIC MALFUNCTIONS

Symptoms of Abnormal Operation	Remedy

SECTION 5

DIAGRAMS

This section contains the necessary information to locate and identify all the components and signal paths in the Type 30E Precision CRT Display. This information is in the form of logic diagrams, schematic diagrams, wiring diagrams, wiring tables, and cable schedules. An explanation of logic symbols is also included. These diagrams should be consulted for all signal tracing and troubleshooting. If any difficulty occurs in understanding the diagrams, the equivalent DEC engineering drawings listed in Table 5-1 should be consulted.

TABLE 5-1 LIST OF DIAGRAMS

Figure	Title	Equivalent DEC No.
5-1	DEC Logic Symbols	-------
5-2	Type 30E Logic Diagram	D-30908
5-3	Type 30 Display Housing Schematic	C-30909
5-4	Type 30E Logic Circuits Panel Wiring Diagram	D-30914
5-5	Type 30 Display Housing Wiring Diagram	C-30916
5-6	Type 30E Cable and Wiring Diagram	B-22117
5-7	Type 811 Power Control Panel Wiring Diagram	C-22101
5-8	Logic Circuits Power End Panel Schematic	B-10801
5-9	Deflection Amplifier Heat Sink Wiring Diagram	B-22106
5-10	Deflection Amplifier Resistor Stack Wiring Diagram	C-22106
5-11	Deflection Amplifier Printed Circuit Layout	B-22116
5-12	Deflection Amplifier Module Schematic	B-22100
5-13	Type 722 Power Supply Schematic	RS-722
5-14	Type 770 Power Supply Schematic	RS-770
5-15	Type 1559 Light Pen Amplifier Schematic	RS-1559
5-16	Type 1562 Reference Supply Schematic	RS-1562
5-17	Type 1564 Digital-to-Analog Converter Schematic	RS-1564
5-18	Type 1567 Display Preamplifier Schematic	RS-1567

TABLE 5-1 LIST OF DIAGRAMS (continued)

Figure	Title	Equivalent DEC No.
5-19	Type 1669 Indicator Driver Schematic	RS-1669
5-20	Type 1705 Bias and Focus Schematic	RS-1705
5-21	Type 4213 Quadruple Flip-Flop Schematic	RS-4213
5-22	Type 4214 Quadruple Flip-Flop Schematic	RS-4214
5-23	Type 4301 One-Shot Multivibrator Delay Schematic	RS-4301
5-24	Type 4603 Pulse Amplifier Schematic	RS-4603
5-25	Type 4604 Pulse Amplifier Schematic	RS-4604
5-26	Type 4677 Level Amplifier Module Schematic	RS-4677
5-27	Type 4688 Intensifier Module Schematic	RS-4688

CABLE SCHEDULE

J-1 to Logic Panel
Display Control Signals

Amphenol
115-115S

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
w/blk	B03N	1	AC-0	w/red	gnd	33	CDP ret
w/brn	B03R	2	AC-1	w/orn	B01S	34	CDP
w/red	B03T	3	AC-2	w/yel	gnd	35	LDP ret
w/orn	B03U	4	AC-3	w/grn	B01Y	36	LDP
w/yel	B02N	5	AC-4	w/blu	gnd	37	DDP ret
w/grn	B02R	6	AC-5	w/vio	B25E	38	DDP
w/blu	B02T	7	AC-6	w/gry	gnd	39	LPF ret
w/vio	B02U	8	AC-7	wht	B15M	40	LPF
w/gry	B12N	9	AC-8	w/blk	B16M	41	INT-1
wht	B12R	10	AC-9	w/brn	B16U	42	INT-2
w/blk	B22N	21	I/O-0	w/red	B16Y	43	INT-3
w/brn	B22R	22	I/O-1	w/yel	ST-B15	45	LPS
w/red	B22T	23	I/O-2	w/grn	ST-B11	46	NAC
w/orn	B22U	24	I/O-3	w/blu	+10MC term.	47	+10 MC
w/yel	B23N	25	I/O-4	w/vio	811-5	48	-15 volts
w/grn	B23R	26	I/O-5	wht	gnd	50	ground
w/blu	B23T	27	I/O-6				
w/vio	B23U	28	I/O-7				
w/gry	B12T	29	I/O-8				
wht	B12U	30	I/O-9				

CABLE SCHEDULE (continued)

J-2 from Logic Panel
Indicator Signals

Amphenol
143-022-04

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
w/blk	B09F	A	H-0	w/blu	B09V	H	H-6
w/brn	B09J	B	H-1	w/vio	B09X	J	H-7
w/red	B09L	C	H-2	w/gry	B11F	K	H-8
w/orn	B09N	D	H-3	w/blk	B11J	M	H-9
w/yel	B09R	E	H-4	w/gry	J-1, 46	W	NAC
w/orn	B09T	F	H-5	w/blk	-15V	Y	-15 volts
				w/brn	gnd	Z	ground

J-3 from Logic Panel
Indicator Signals

Amphenol
143-022-04

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
w/blk	B10F	A	V-0	w/gry	B11L	K	V-8
w/brn	B10J	B	V-1	w/blk	B11N	M	V-9
w/red	B10L	C	V-2	w/grn	B11R	T	int-1
w/orn	B10N	D	V-3	w/blu	B11T	U	int-2
w/yel	B10R	E	V-4	w/vio	B11V	V	int-3
w/grn	B10T	F	V-5	w/gry	B11X	W	LPS
w/blu	B10V	H	V-6	w/blk	-15V	Y	-15 volts
w/vio	B10X	J	V-7	w/brn	gnd	Z	ground

P-4 from CRT Housing
Deflection Signals

Amphenol
126-195

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
microdot teflon	A08B	A	left	microdot teflon	A17A	E	up
microdot teflon	A08A	B	right	blu	+50V ST	F	+50 volts
orn	+10 V	C	+10 volts	blk	gnd	H	ground
microdot	A17B	D	down				

CABLE SCHEDULE (continued)

J-5 from Logic Panel
Intensity and Light Pen Signals

Amphenol
126-221

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
w/brn	B16N	B	int-1	brn	Z-BNC	F	INT
w/red	B16T	C	int-2	w/blu	B15V	H	LP gate
w/orn	B16X	D	int-3	w/vio	-15V	J	-15 volts
w/yel	B25J	E	int-A	w/gry	gnd	K	ground

P-6 from Deflection Yoke
Deflection Currents

Cinch-Jones
P-308-FH

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
blk	P-4,F	1	+50V	orn	P-4,A	6	left
wht	P-4,F	2	+50V	yel	P-4,B	7	right
red	P-4,E	5	up	brn	P-4,D	8	down

J-7 from CRT Housing
Focus Current

Cinch-Jones
S-302-AB

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
yel	P-5,K	1	ground	grn	2N457A-C	2	focus

P-8 from Type 770 Power Supply
CRT Bias and Heater Voltage

Amphenol
26-4404-8S

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
red	770-1	1	+265V	blu	770-5	5	-150V
blk	770-3	3	ground	blk	770-8	8	6.3 vac
wht	770-4	4	6.3 vac				

P-9 from CRT Tube
CRT Ultor Voltage

Winchester
456

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
wht	770-A	A	+10KV	shield	770-B	B	ground

CABLE SCHEDULE (continued)

S-10 from CRT Housing — 12-pin Tube Socket
CRT Socket Connections

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
brn	6.3 V ST	1	6.3 vac	orn	D02T	10	+200V
grn	D02X	2	bias	yel	D02Y	11	INT
				brn	resistor ST	12	6.3 vac

P-11 from Logic Panel — Cinch-Jones
+10 and -15 volt Logic Power — P-308-FP

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
grn	MC +10	1 and 2	+10 volts	blk	MC gnd	7 and 8	ground
red	MC -15	3 and 4	-15 volts				

J-12 from Logic Panel — BNC
X Analog Voltage — Microdot 50-3920

J-13 from Logic Panel — BNC
Y Analog Voltage — Microdot 50-3920

J-14 from J-5 — BNC
Z Intensifying Voltage — Microdot 50-3920

P-16 to 811 Power Control Panel — Miller Electric
Primary 115 Volt 60 CPS Power — 034-2

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
blk	FL1	1	115VAC	grn	chassis	3	ground
wht	FL2	2	115VAC				

P-17 from NJE Power Supply — Amphenol
Main AC Power — 160-5

Wire Color	Socket Pin	Cable Pin	Line Name	Wire Color	Socket Pin	Cable Pin	Line Name
blk	tb 1-1	1	115 vac	grn	chassis	3	ground
wht	tb 1-2	2	115 vac				

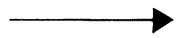
CABLE SCHEDULE (continued)

P-18 to J-19 115 Volt 60 CPS Power for Type 770 Power Supply	Amphenol 160-5 and 160-4
P-20 from 811 Power Control Panel 115 Volt 60 CPS Power for Power Supplies	Amphenol 160-5
J-21 from B08W Horizontal Reference	BNC Microdot 50-3920
J-22 from B17W Vertical Reference	BNC Microdot 50-3920

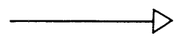
WIRING SCHEDULE

Wire Color	From	To
wht	811-2	811-8
wht	811-3	811-6
blk	811-6	cooling fans
blk	811-8	sail switch
brn	811-9	sail switch
red	811-10	cooling fans
blk	EQR 60-6B, tb 1-1	P-11, 1
wht	EQR 60-6B, tb 1-2	P-11, 2
jumper	EQR 60-6B, tb 1-3	EQR 60-6B, tb 1-4
jumper	EQR 60-6B, tb 1-4	EQR 60-6B, tb 1-3
jumper	EQR 60-6B, tb 1-5	EQR 60-6B, tb 1-6
jumper	EQR 60-6B, tb 1-6	EQR 60-6B, tb 1-5
jumper	EQR 60-6B, tb 1-7	EQR 60-6B, tb 1-8
jumper	EQR 60-6B, tb 1-8	EQR 60-6B, tb 1-9
jumper	EQR 60-6B, tb 1-9	EQR 60-6B, tb 1-8
jumper	EQR 60-6B, tb 1-10	EQR 60-6B, tb 1-11
jumper	EQR 60-6B, tb 1-11	EQR 60-6B, tb 1-12
grn	EQR 60-6B, tb 1-12	P-11, 3; chassis gnd
red	EQR 60-6B 50V pos.	+50V standoff on deflectiom amp.
blk	EQR 60-6B 50V neg.	gnd on deflection amp. panel

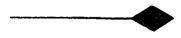
Miscellaneous signal. Indicates direction only. No voltage levels or timing considerations implied.



DEC negative-going 3 volt pulse, usually from ground to -2.5 volts. Pulse widths of 70, 400, and 1000 nanoseconds.

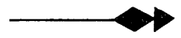


DEC positive-going 3 volt pulse, usually from -3 volts to ground. Pulse widths of 70, 400, and 1000 nanoseconds.

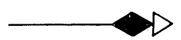


Negative level, -3 volts. Greater than one microsecond.

Positive level, ground. Greater than one microsecond.

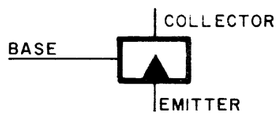


Negative-going level which triggers on its leading edge, or differentiates. Open diamond and arrow for positive-going levels.

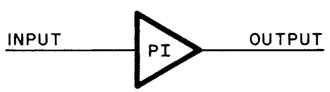


Negative-going level which triggers on its trailing edge. Open diamond and solid arrow for positive-going levels. Also applicable to pulses.

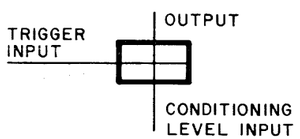
Clamped load resistor. Normally goes to -15 volts, with the output clamped to -3 volts. Gives ground and -3 volts output pulses or levels.



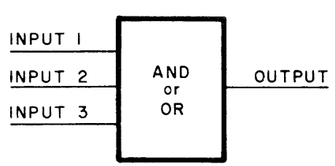
Inverter. A transistor in common-emitter configuration, with biased input on its base. Emitter must be at ground to conduct. Ground input cuts it off and -3 volt input saturates it. Delay = 20 nanoseconds.



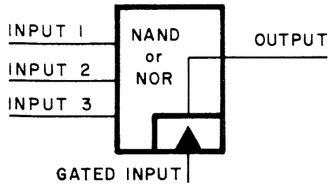
Pulse Inverter. Similar to standard inverter but with lower driving power. Used only with Capacitor-Diode Gates.



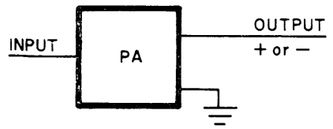
Capacitor-Diode Gate. Differentiates the input if the conditioning level has had the proper voltage for approximately three microseconds.



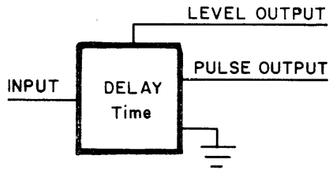
Logic Gate. May be either AND or inclusive OR, depending on polarity of inputs and output. Number of inputs unlimited.



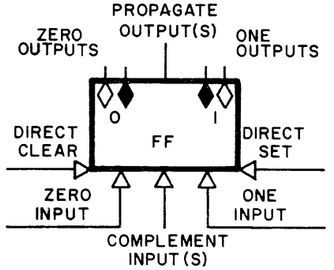
NAND or NOR Logic Gate. Same as an AND or OR Logic Gate with an inverter which may be gated. Output polarity opposite to input polarities.



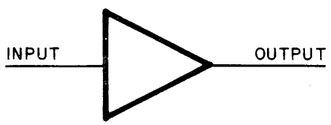
Pulse Amplifier. Amplifies and standardizes DEC pulses. Output is from a pulse transformer, giving either positive or negative pulses depending on which side is grounded.



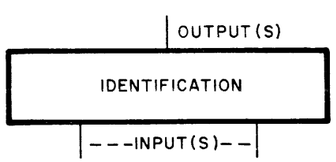
Delay. A monostable multivibrator which produces one or two level outputs while it is timing out, and then may trigger a Pulse Amplifier. Operating time adjustable.



Flip-Flop. A bistable multivibrator with numerous inputs and two outputs, which may be buffered. Outputs shown twice, with diamonds indicating voltage levels in each state. Positive pulses from ground to +2.5 volts required to set or clear on inputs. A complement input changes the state regardless of the previous state, and may generate a propogate pulse output.



Analog Amplifier. Any amplifier that operates over a continuous voltage range. May have single or multiple inputs and/or outputs. Generally requires different voltages.



Other types of circuits, such as Digital-to-Analog Converters, Electronic Switches, Switch Filters, Level Amplifiers, etc. Shown in any shape or orientation.

Figure 5-1 DEC Logic Symbols

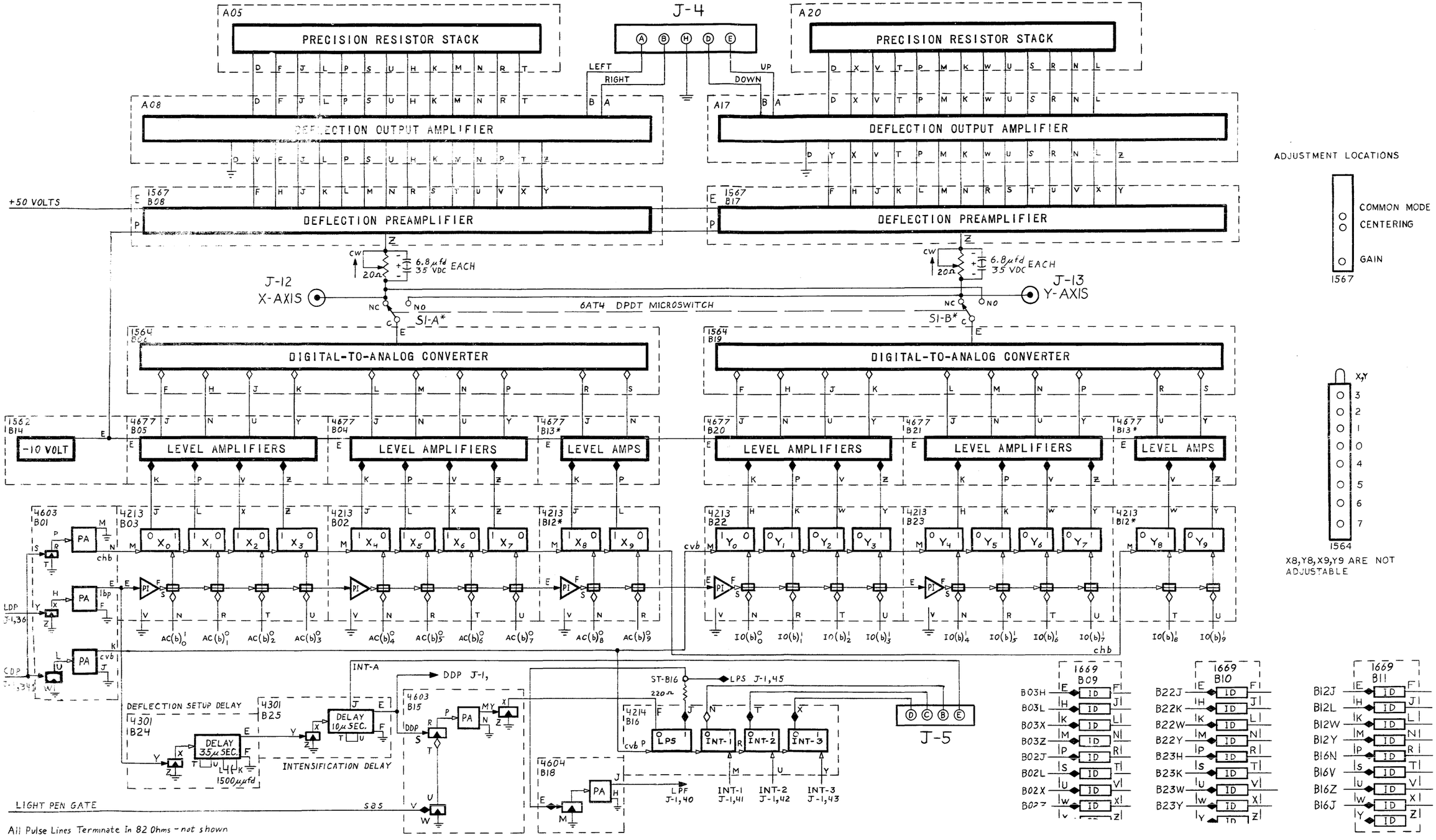


Figure 5-2 Type 30E Logic Diagram

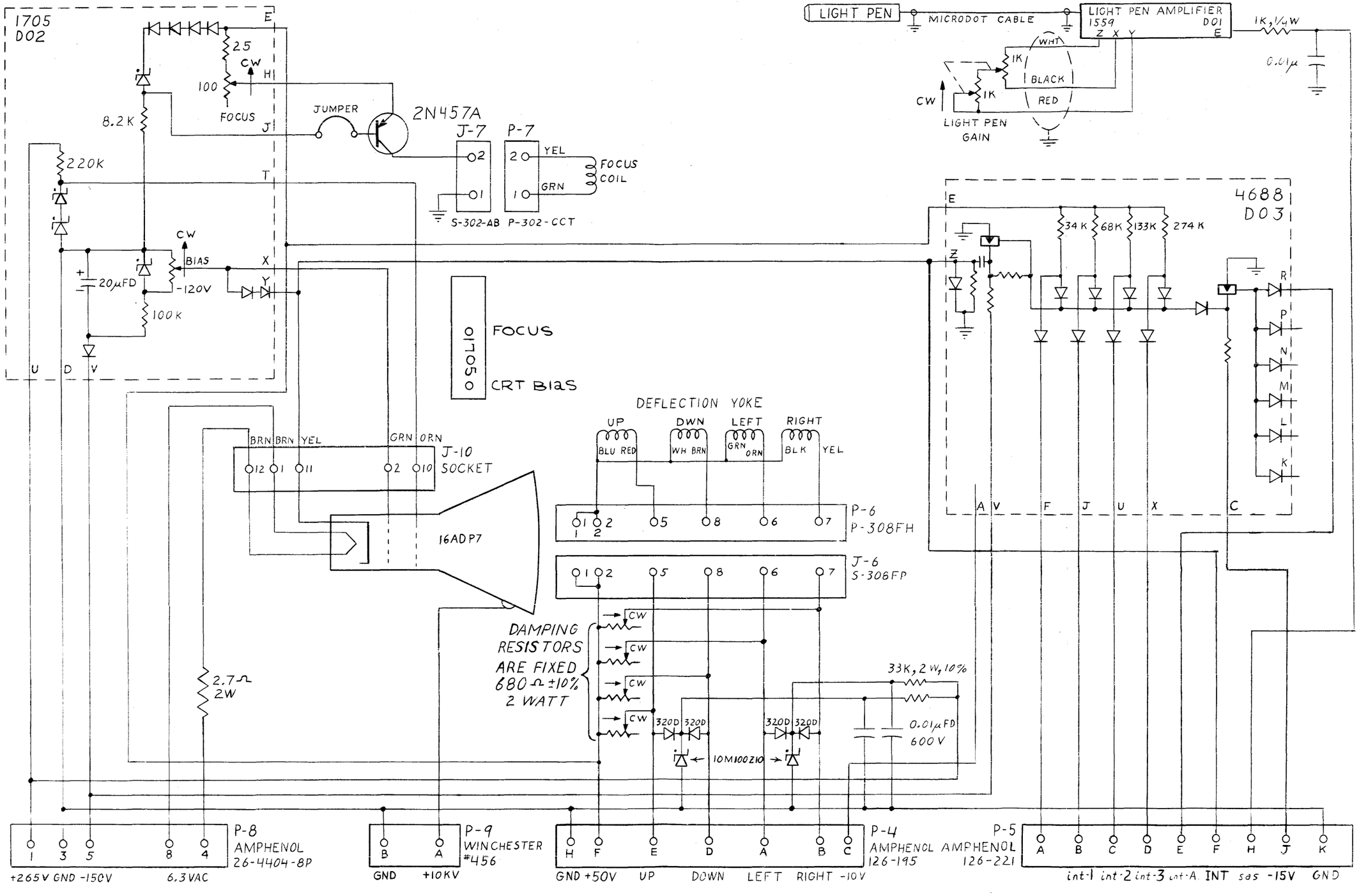


Figure 5-3 Type 30 Display Housing Schematic

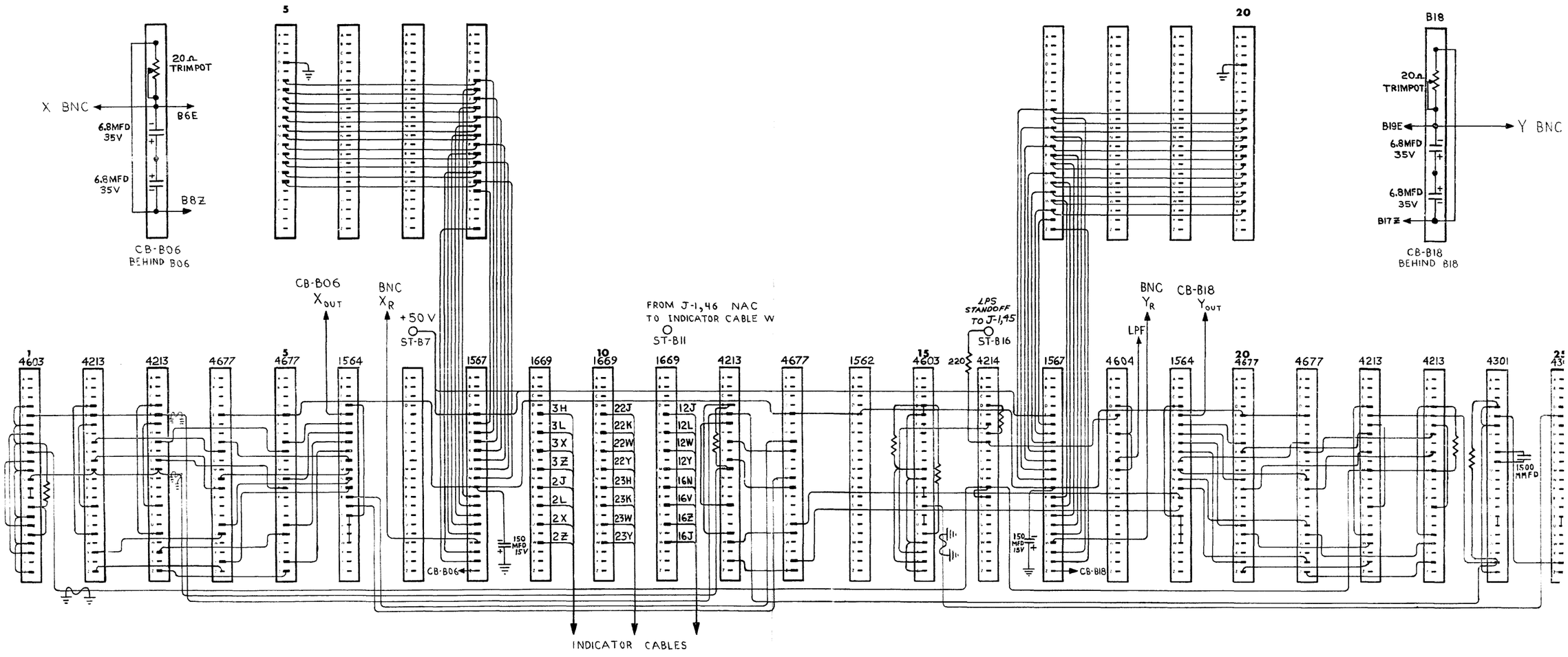


Figure 5-4 Type 30E Logic Circuits
Panel Wiring Diagram

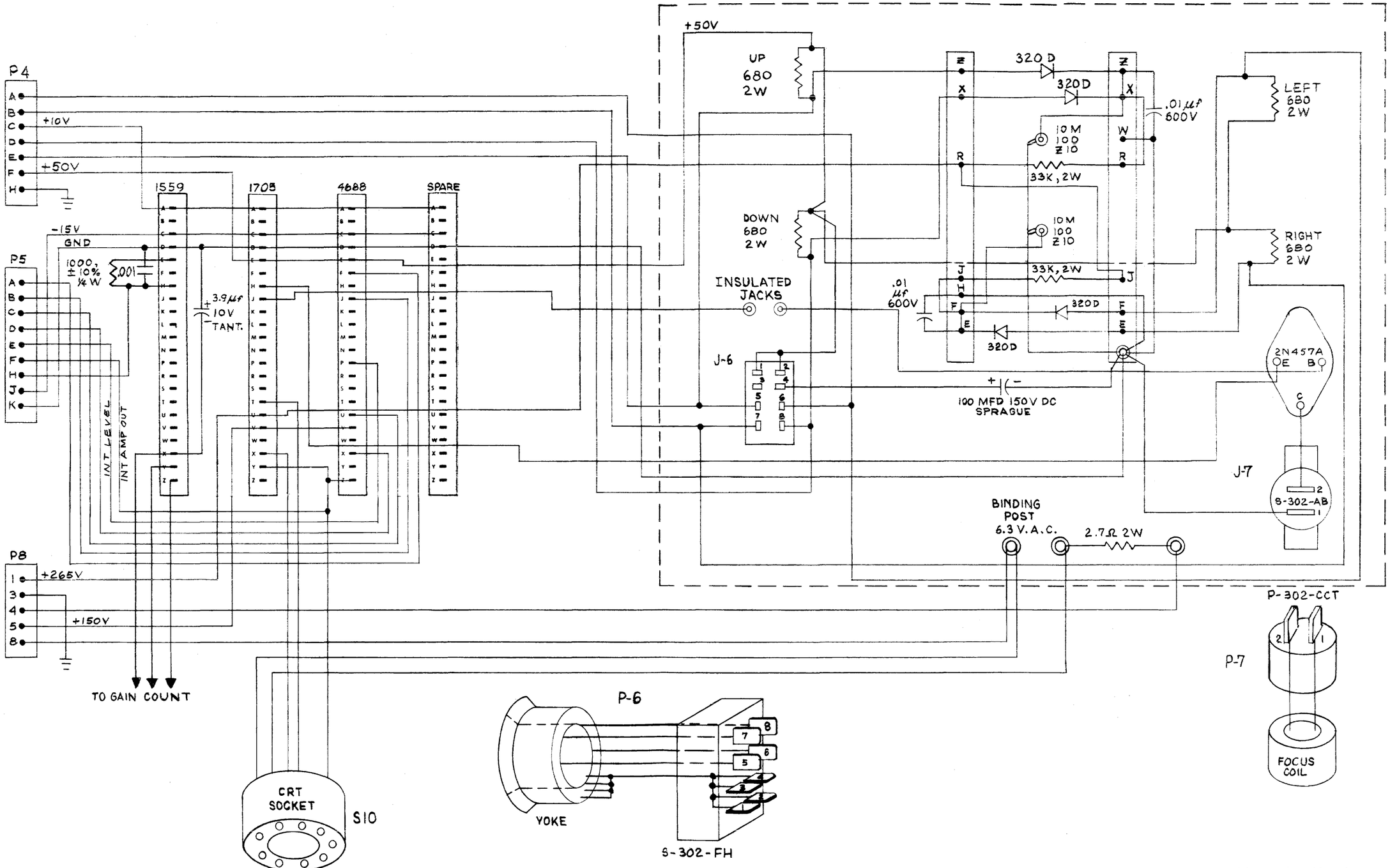


Figure 5-5 Type 30 Display Housing Wiring Diagram

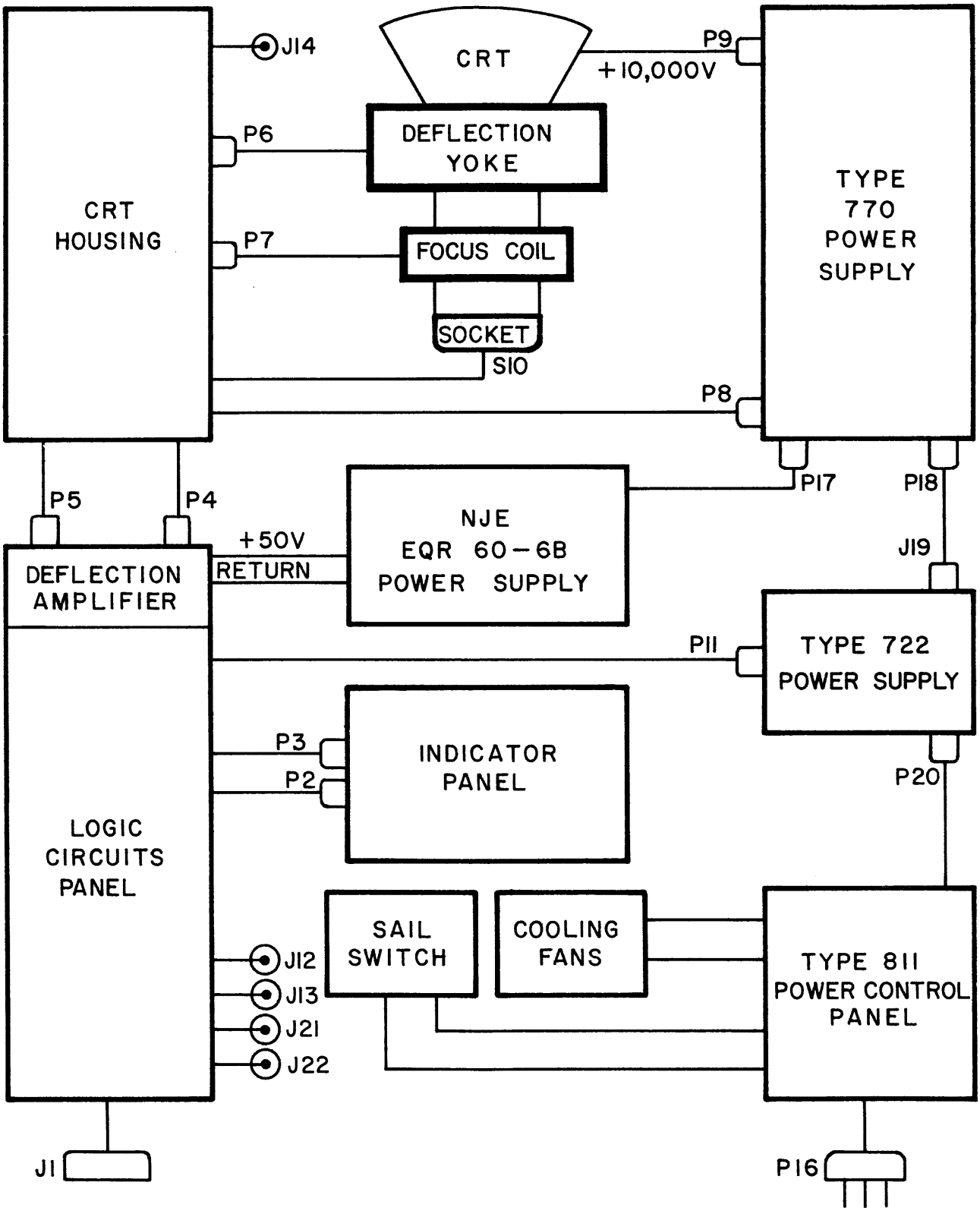
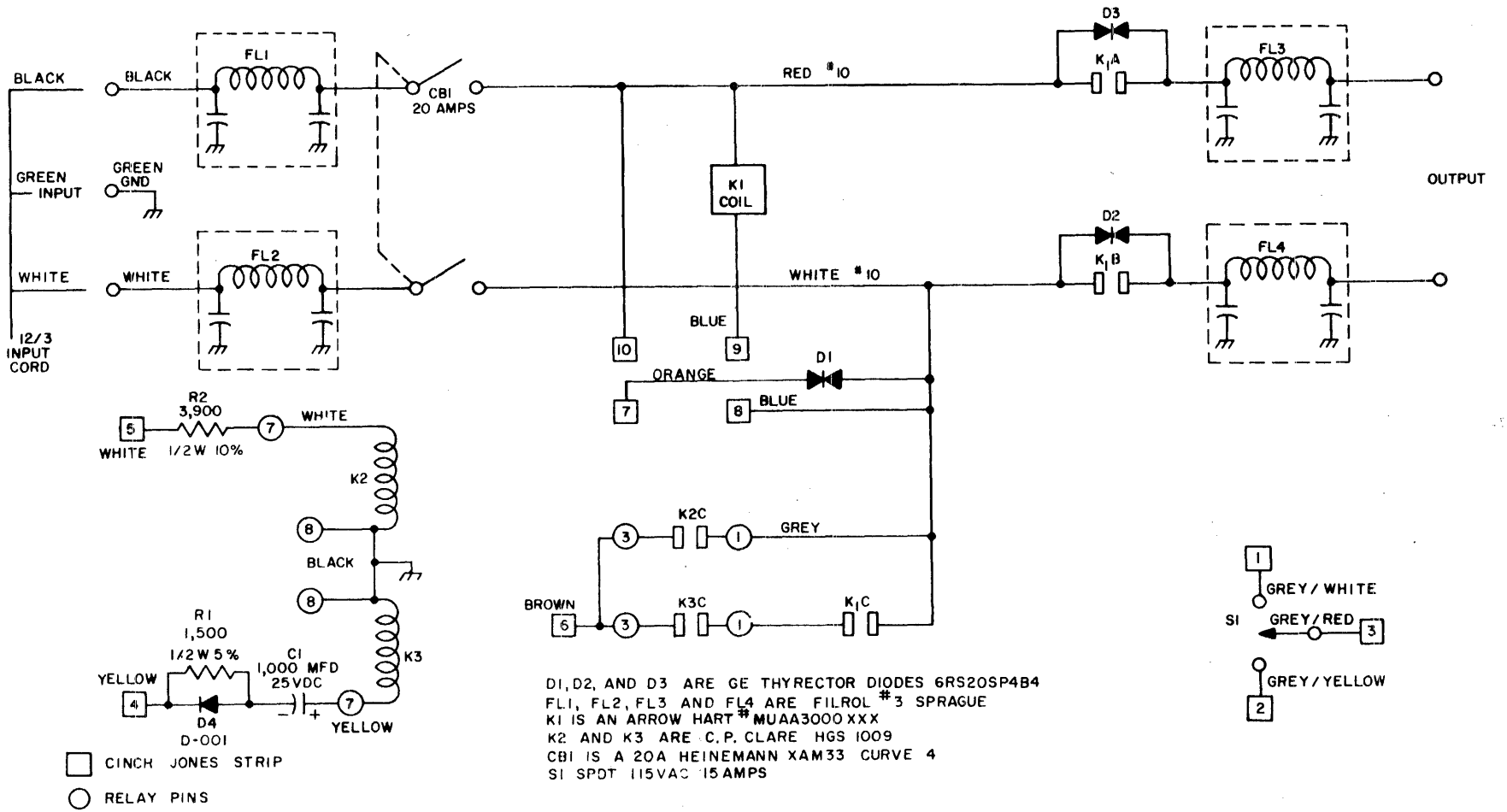


FIGURE 5-6 TYPE 30E CABLE AND WIRING DIAGRAM



D1, D2, AND D3 ARE GE THYRECTOR DIODES 6RS20SP4B4
FL1, FL2, FL3 AND FL4 ARE FILROL #3 SPRAGUE
K1 IS AN ARROW HART # MUAA3000XXX
K2 AND K3 ARE C.P. CLARE HGS 1009
CB1 IS A 20A HEINEMANN XAM33 CURVE 4
S1 SPDT 115VAC 15AMPS

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D-001	IN276		

NOTES

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY

RS-811 | 7

POWER CONTROL 811

Figure 5-7 Type 811 Power Control Panel Wiring Diagram

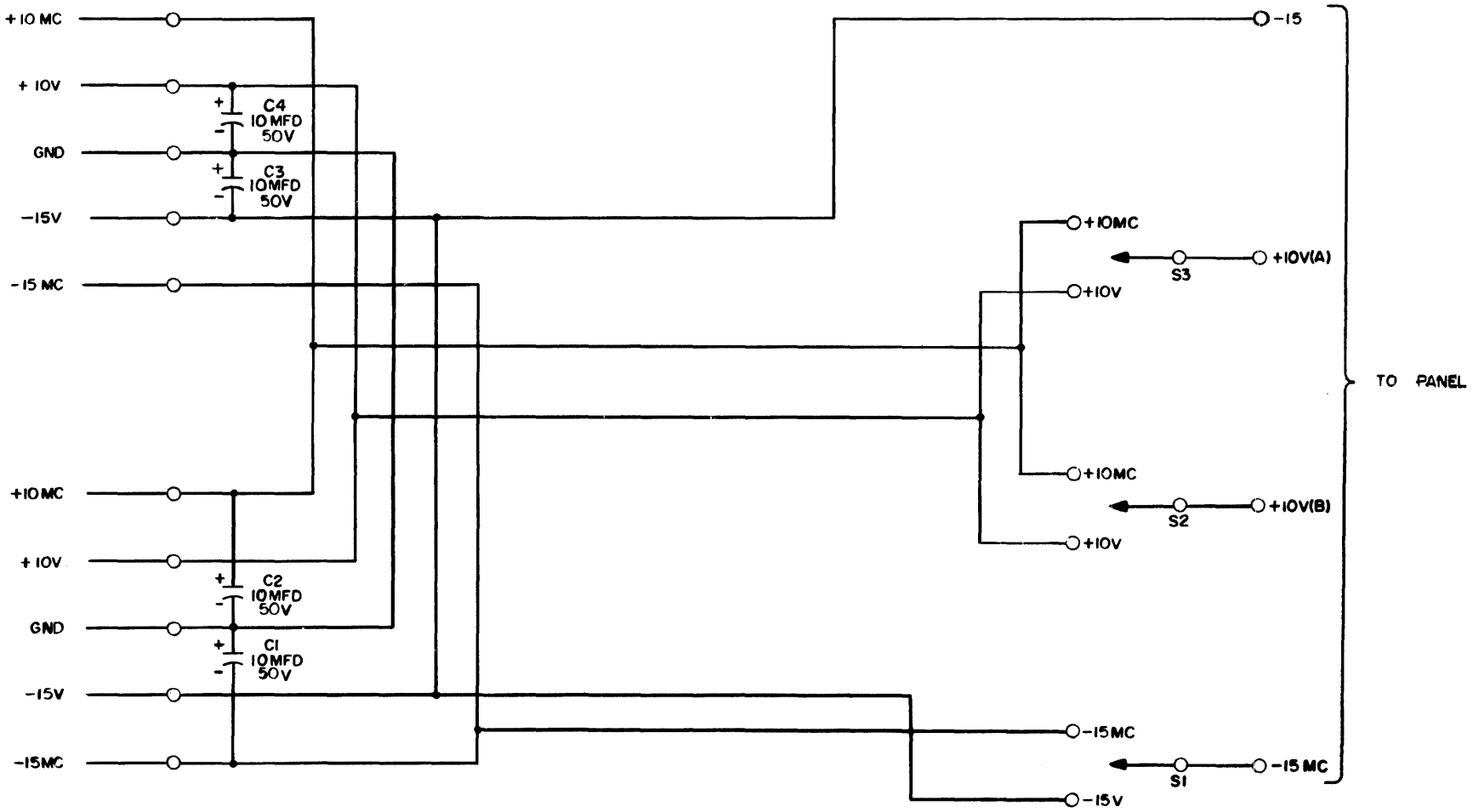


Figure 5-8 Logic Circuits Power End Panel Schematic

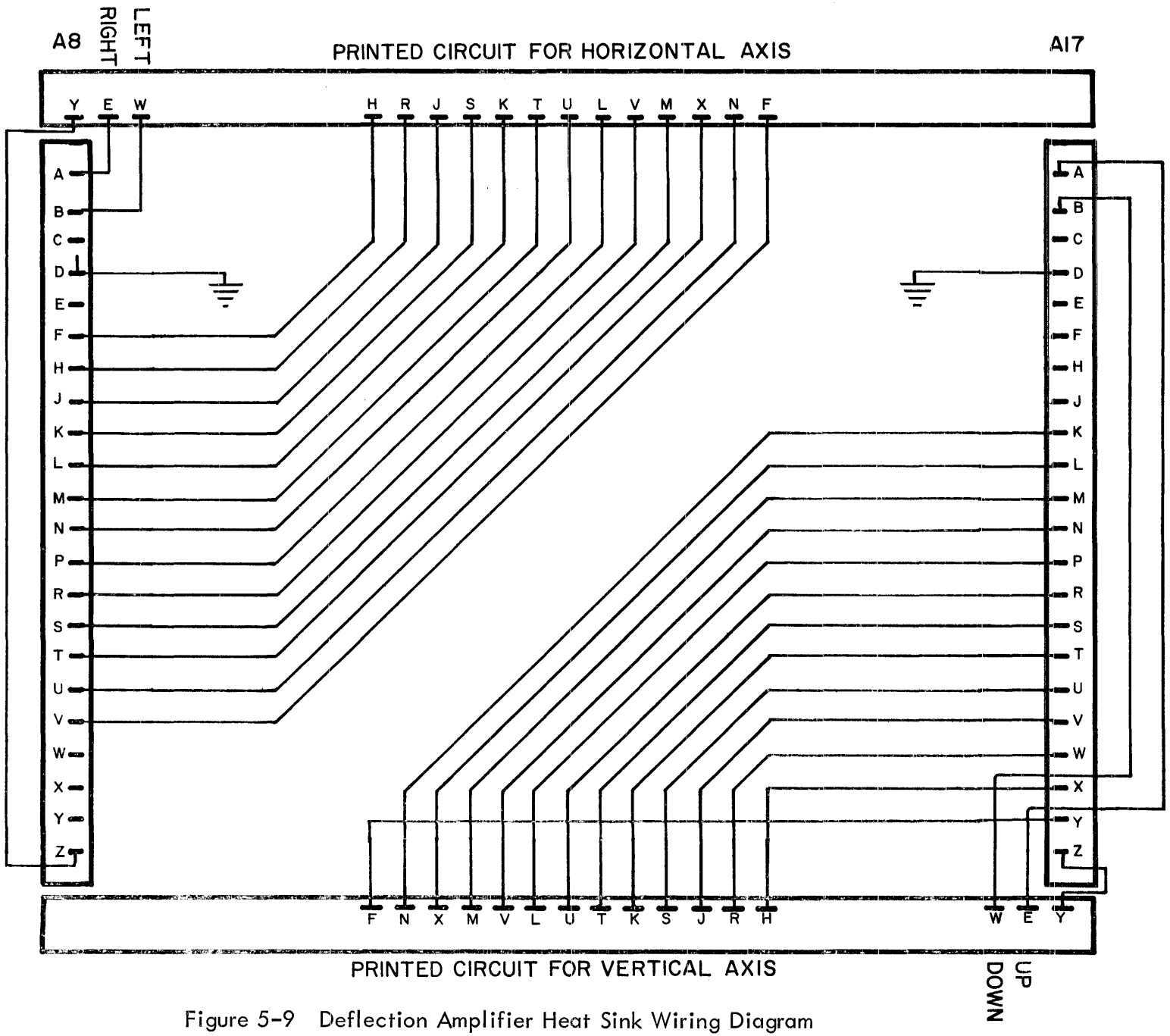
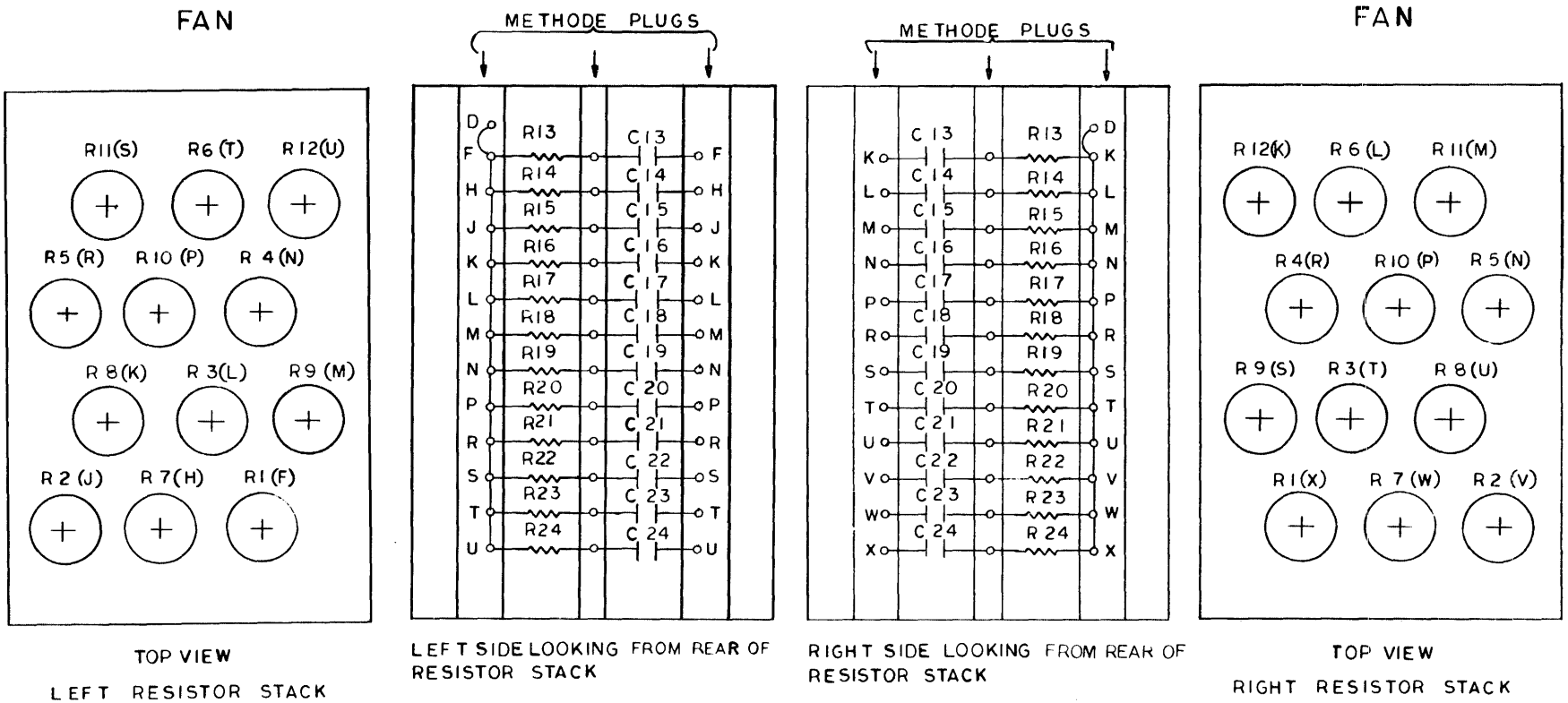


Figure 5-9 Deflection Amplifier Heat Sink Wiring Diagram

DEFLECTION AMPLIFIER HEAT SINK WIRING DIAGRAM



NOTE:

1. ON METHODE (22P) PLUG THE FOLLOWING NUMBERS CORRESPOND TO THE FOLLOWING LETTERS

   1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

   A B C D E F H J K L M N P R S T U V W X Y Z

2. C 13 - C 24 GOODALL .05 ufd, ±10% 100 VOLTS
3. R 13 - R 24 ½ WATT, 10 % 20Ω COMPOSITION RESISTOR

Figure 5-10 Deflection Amplifier Resistor Stack Wiring Diagram

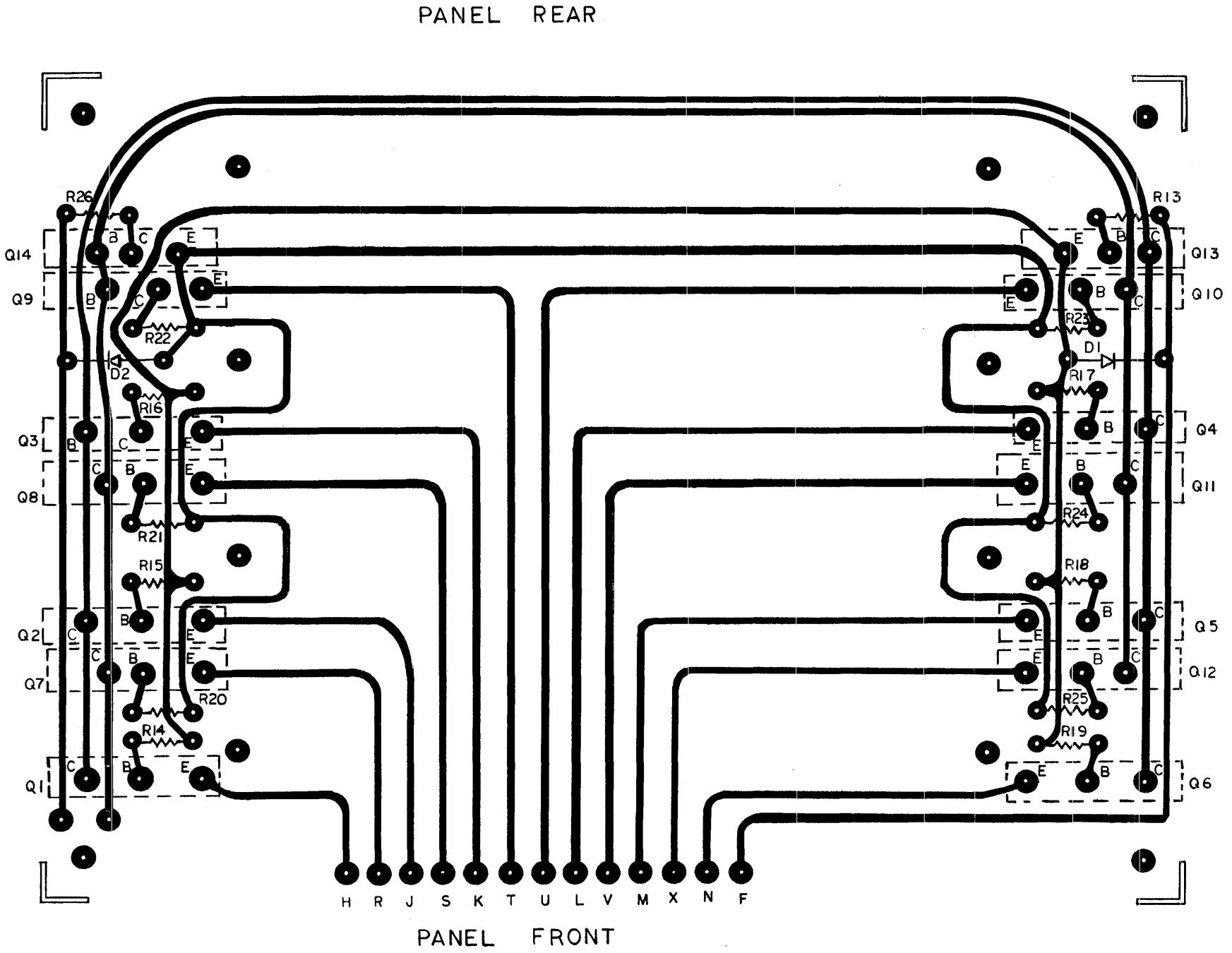
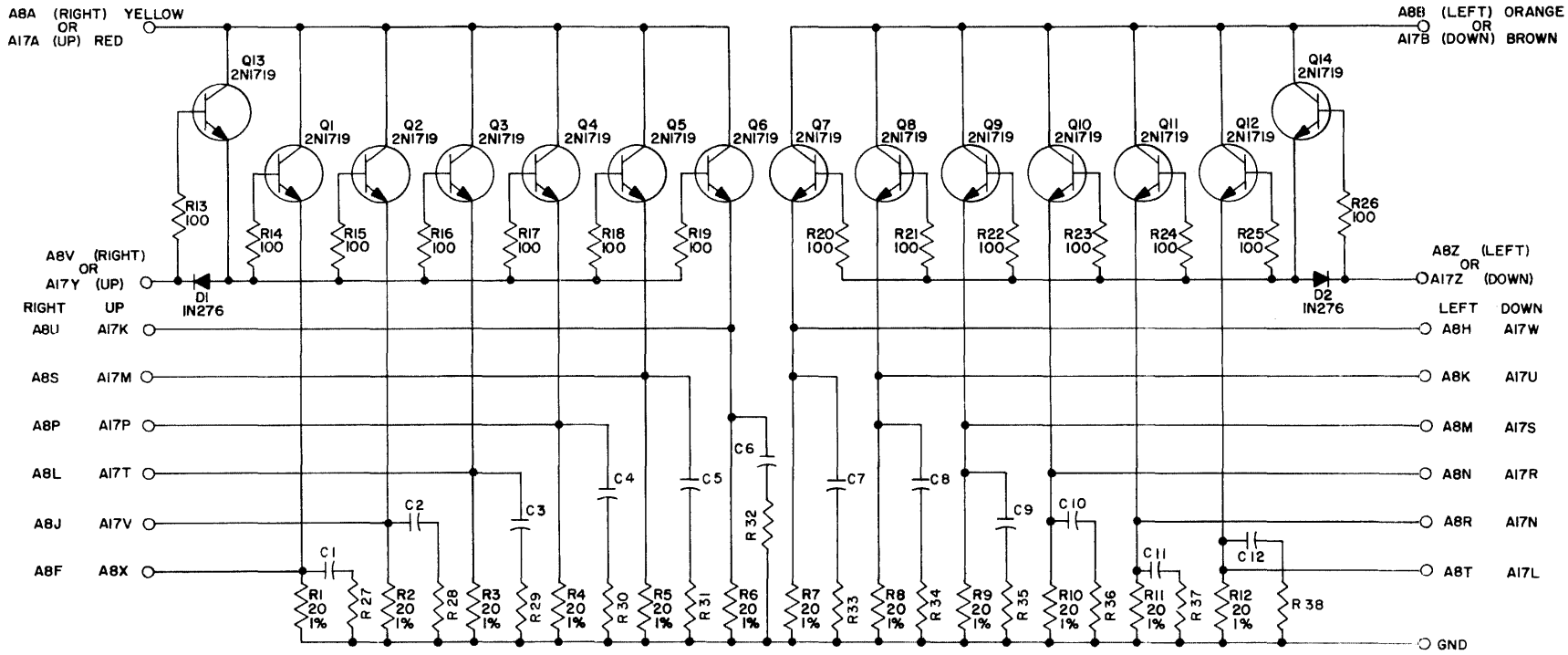


Figure 5-11 Deflection Amplifier Printed Circuit Layout

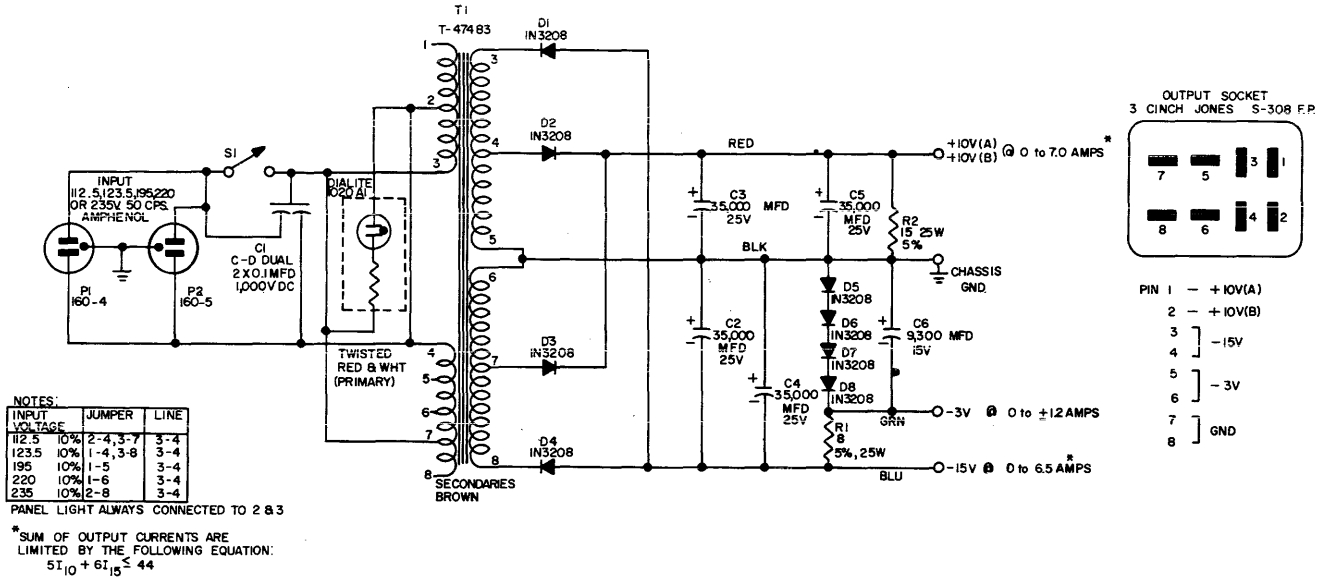


UNLESS OTHERWISE INDICATED
R1 THRU R11 ARE TEL-LABS NON INDUCTIVE WIREWOUND TYPE TL-12
R13 THRU R26 ARE ± 10%, 1/4 W CARBON
R27 THRU R38 ARE 20 OHM ± 10%, 1/2W CARBON
CAPACITORS ARE GOODALL 0.05 MFD 100V ± 10% MYLAR FILM

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

Figure 5-12 Deflection Output Amplifier Schematic

RS-722A



NOTES:

INPUT VOLTAGE		JUMPER	LINE
112.5	10%	2-4, 3-7	3-4
123.5	10%	1-4, 3-8	3-4
195	10%	1-5	3-4
220	10%	1-6	3-4
235	10%	2-8	3-4

PANEL LIGHT ALWAYS CONNECTED TO 2 & 3

*SUM OF OUTPUT CURRENTS ARE LIMITED BY THE FOLLOWING EQUATION:
$5I_{10} + 6I_{15} \leq 44$

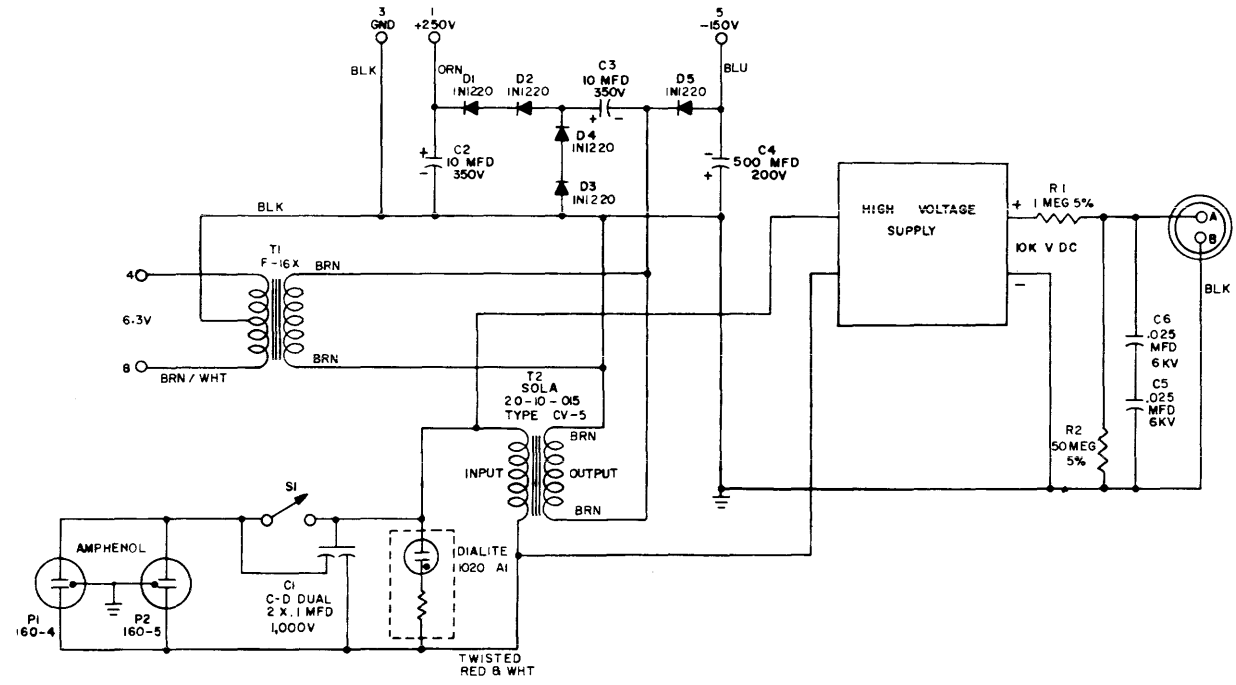
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
IN3208	IN3208		

NOTES

RS-722A
POWER SUPPLY 722A

Figure 5-13 Type 722 Power Supply Schematic

RS-770-5

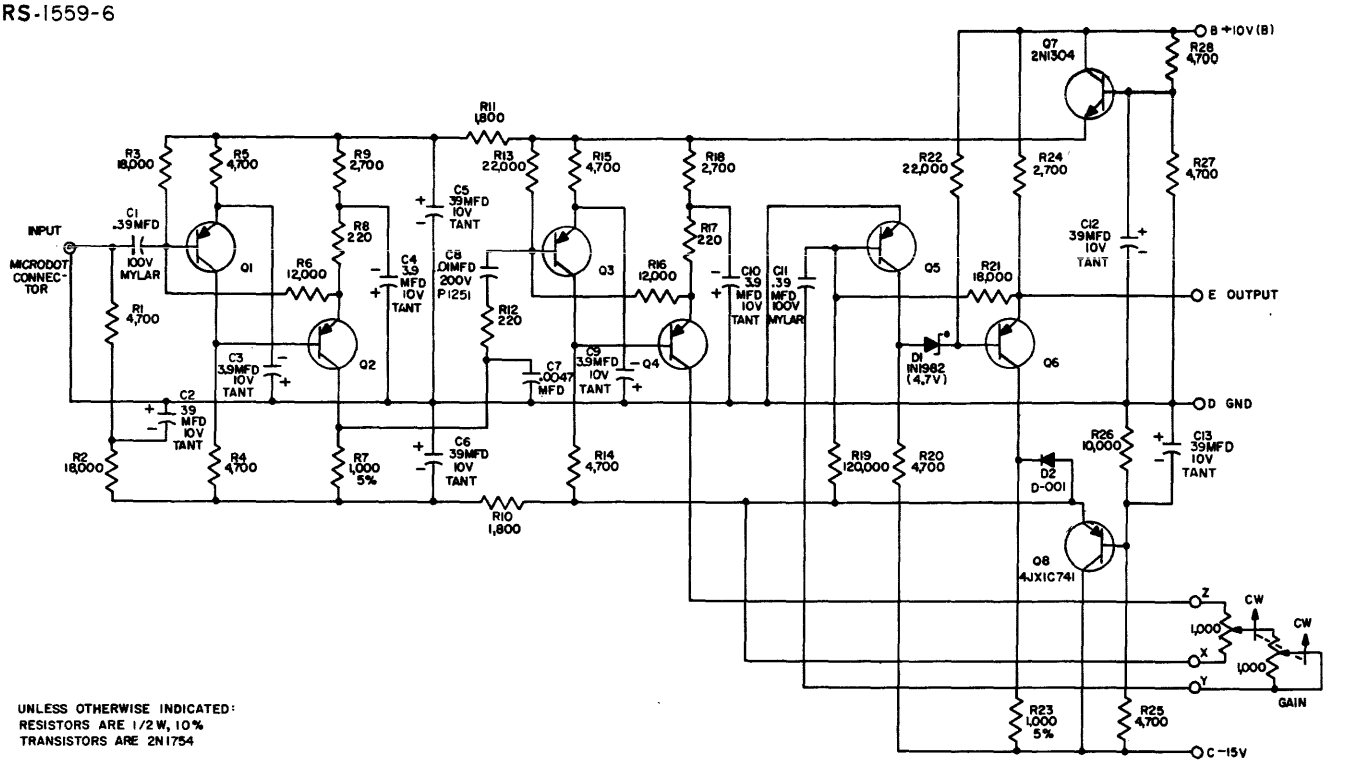


TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
IN1220	IN1220		

NOTES

RS-770 5
POWER SUPPLY 770

Figure 5-14 Type 770 Power Supply Schematic



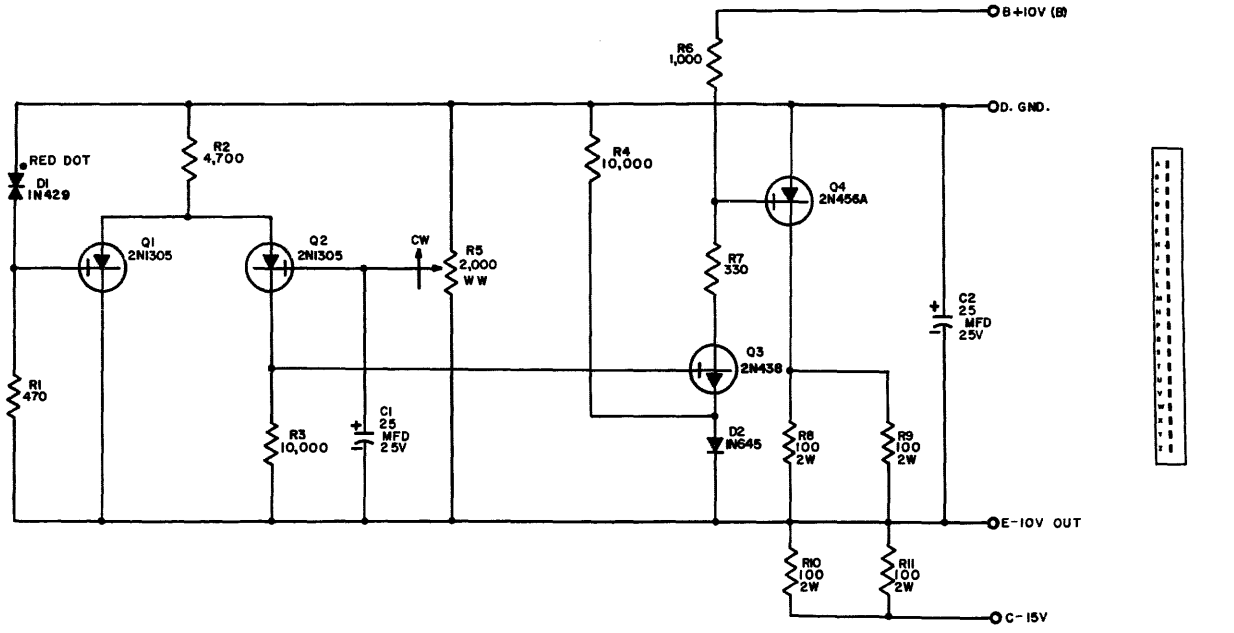
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N1754	2N1754		
2N1304	2N1304		
4JX1C741	2N527		
D-001	IN276		
IN1982(4.7V)	IN1982(4.7V)		

NOTES

B	RS-1559	6
LIGHT PEN AMPLIFIER 1559		

RS-1562-3

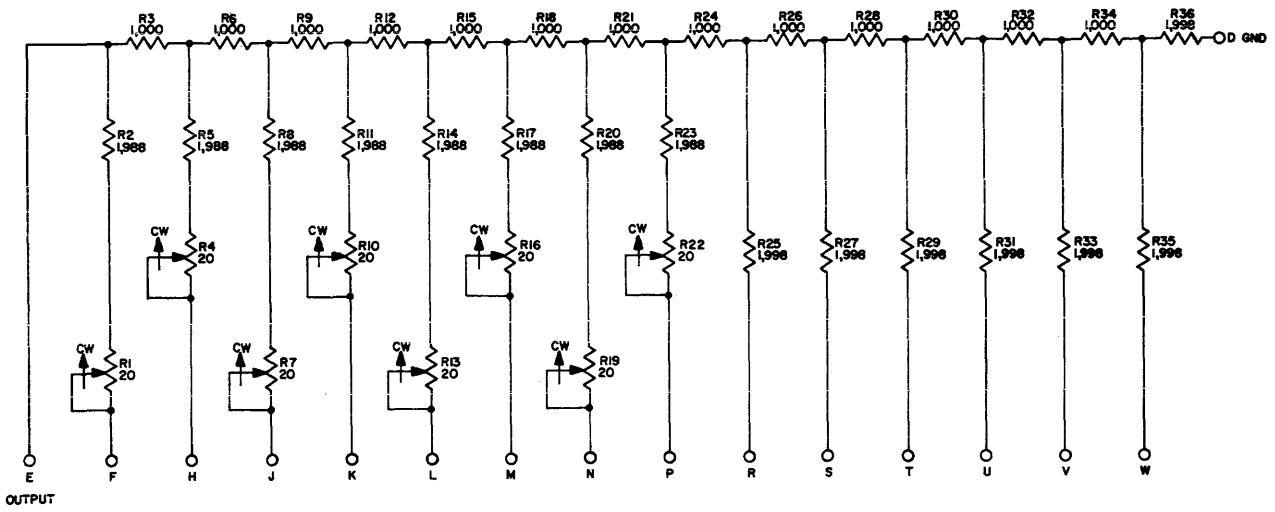
Figure 5-15 Type 1559 Light Pen Amplifier Schematic



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2 W, 10%
CAPACITORS ARE MMFD.

Figure 5-16 Type 1562 Reference Supply Schematic

RS-1564

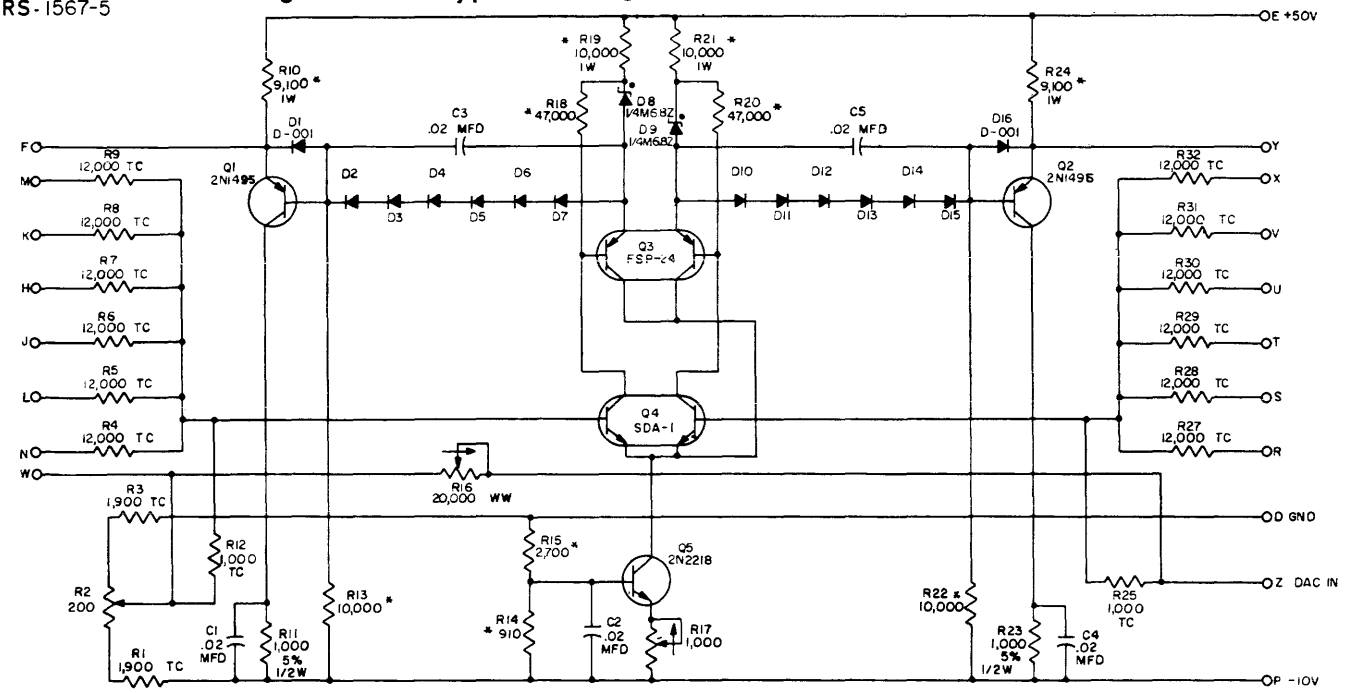


UNLESS OTHERWISE INDICATED:
FIXED RESISTORS ARE 1/10% TEL-LABS AMI
ALL POTS ARE BOURNS TYPE 200 OR 271

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

Figure 5-17 Type 1564 Digital-to-Analog Converter Schematic

RS-1567-5



UNLESS OTHERWISE INDICATED:
TC-LOW TEMP. COEF., METALLIC FILM, ±1%, 1/2W
* RESISTOR DEPOSITED CARBON, ±1%
POTS ARE BOURNS
DIODES ARE D-662

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N1495	2N1495	D-001	1N276
FSP-24	FSP-24	1/4M6.8Z	1/4 6.8Z
SDA-1	2N2060		
2N2218	2N2218		
D-662	1N645		

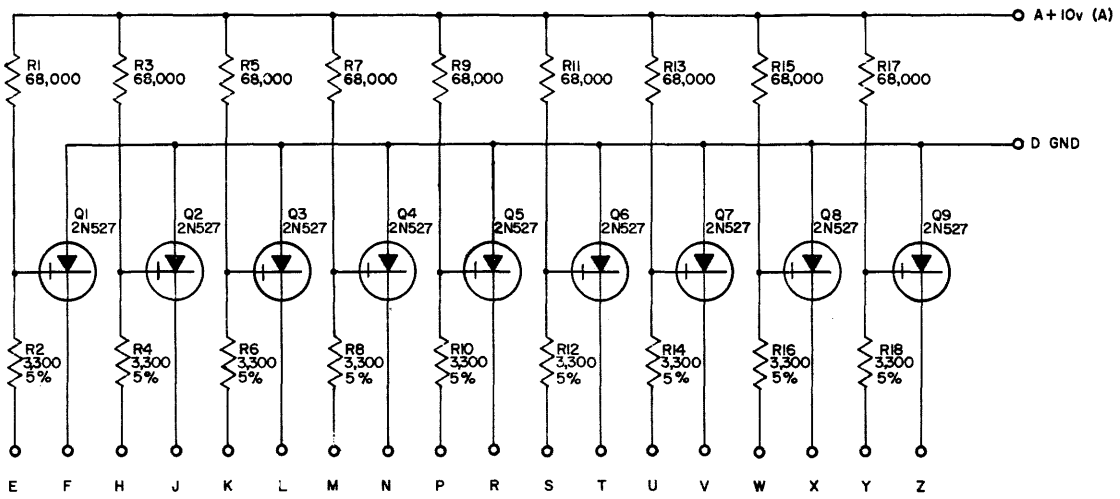
NOTES

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

B	RS-1567	5
DISPLAY PREAMPLIFIER 1567		

Figure 5-18 Type 1567 Display Preamplifier Schematic

RS-1669-4

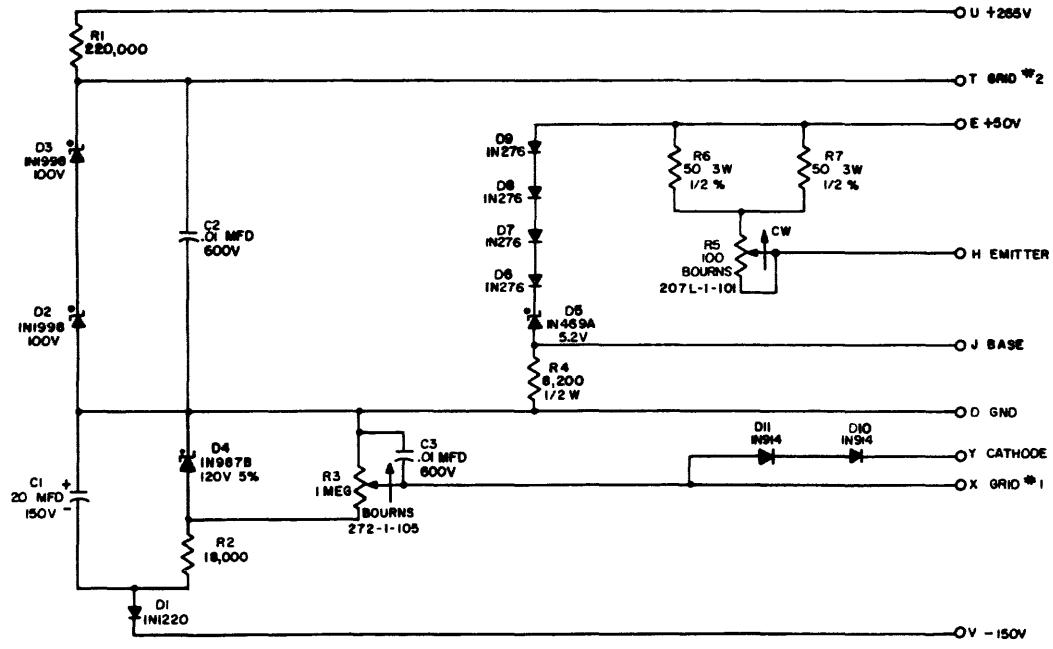


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

RS-1705-3

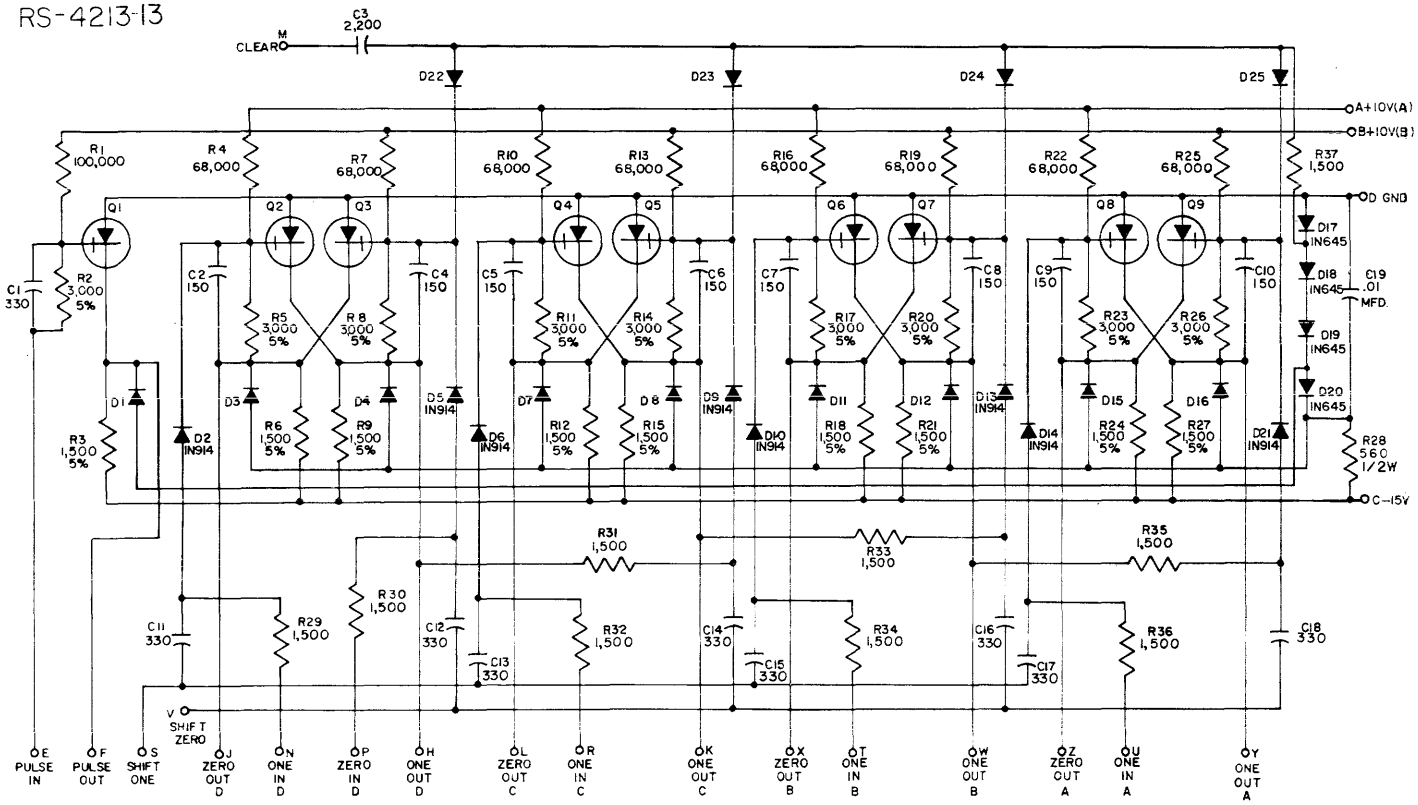
Figure 5-19 Type 1669 Indicator Driver Schematic



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%

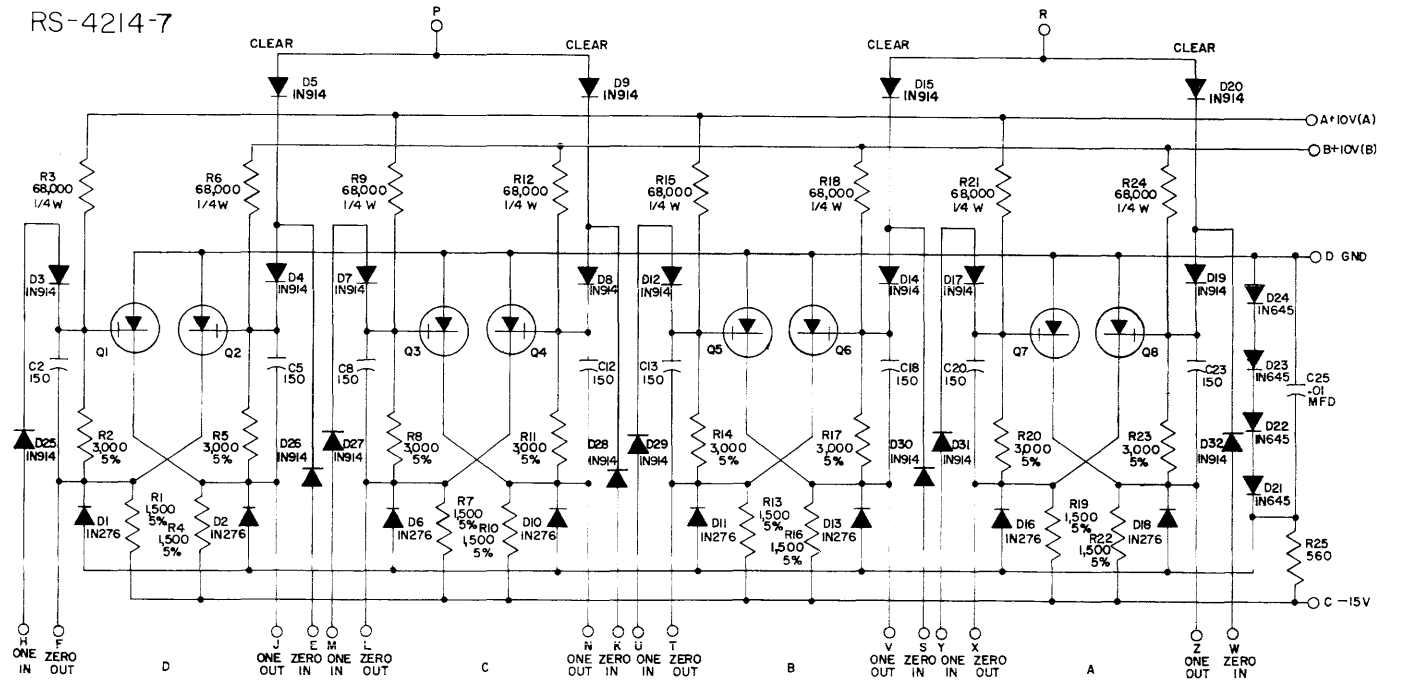
Figure 5-20 Type 1705 Bias and Focus Schematic

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD.
TRANSISTORS ARE 2N1499A
DIODES ARE IN276

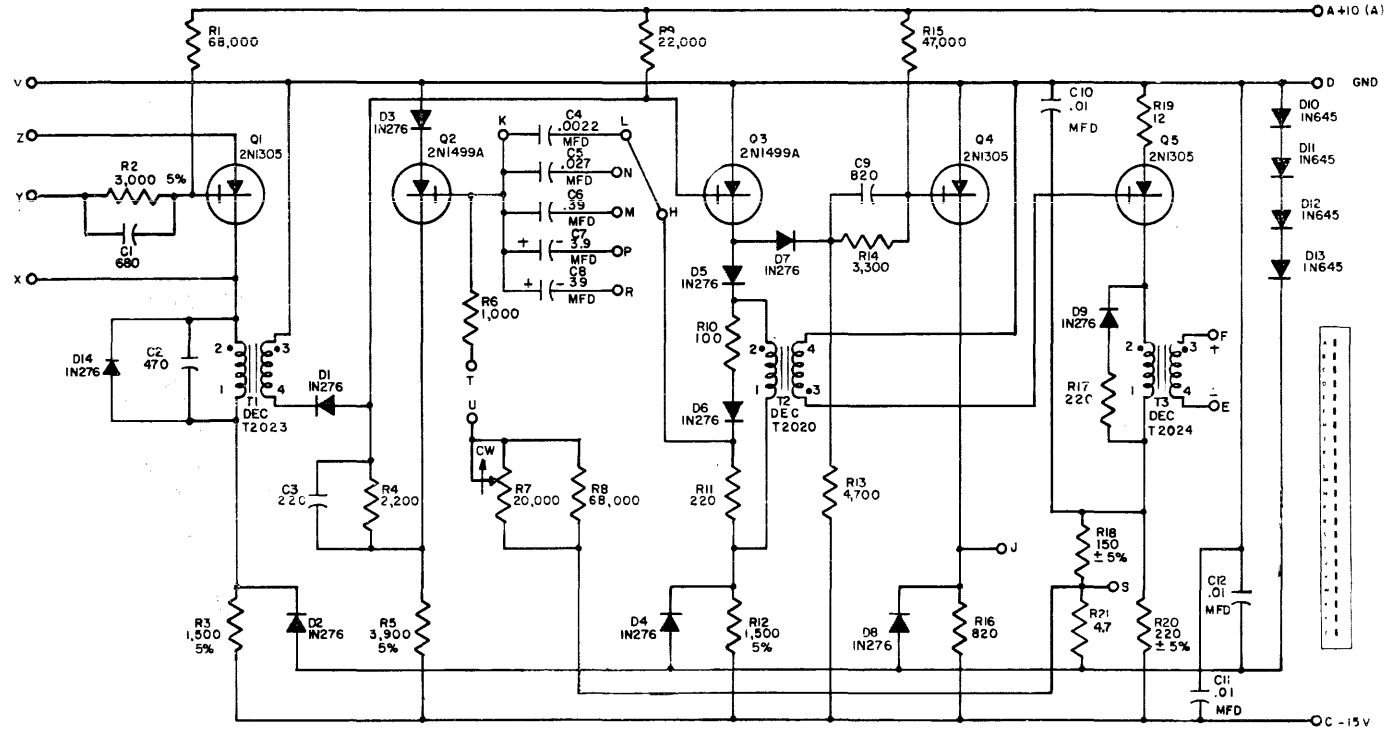
Figure 5-21 Type 4213 Quadruple Flip-Flop Schematic



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2 W, 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE 2N1499A

Figure 5-22 Type 4214 Quadruple Flip-Flop Schematic

RS-4301-13

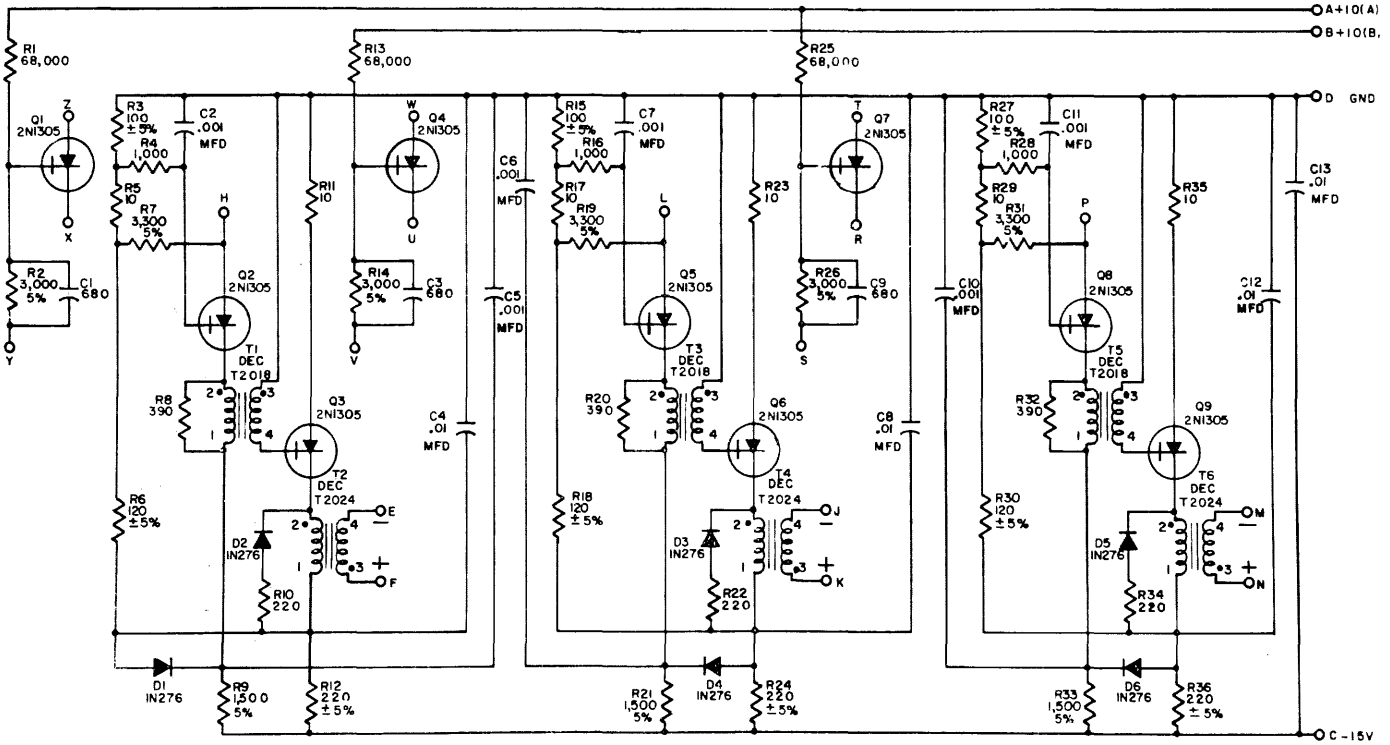


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

Figure 5-23 Type 4301 One-Shot Multivibrator Delay Schematic

RS-4603-7

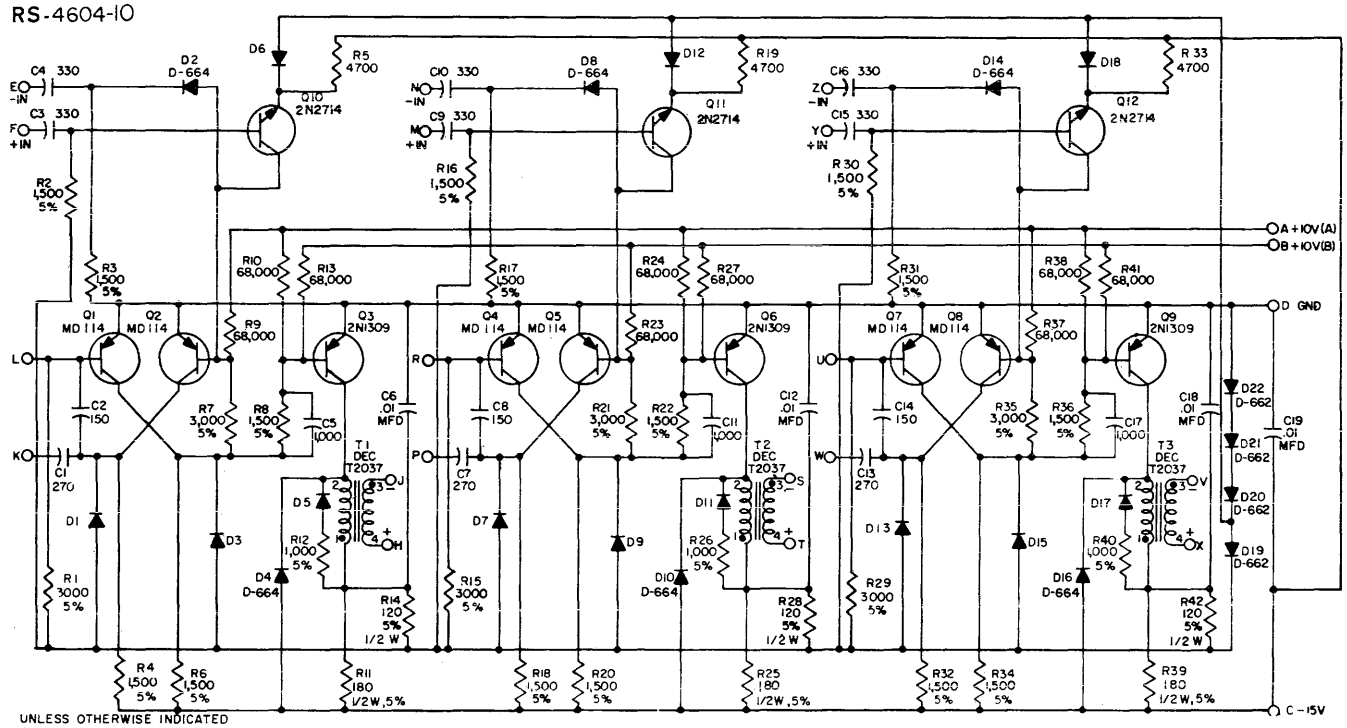


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD.

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

Figure 5-24 Type 4603 Pulse Amplifier Schematic

RS-4604-10



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-001

Figure 5-25 Type 4604 Pulse Amplifier Schematic

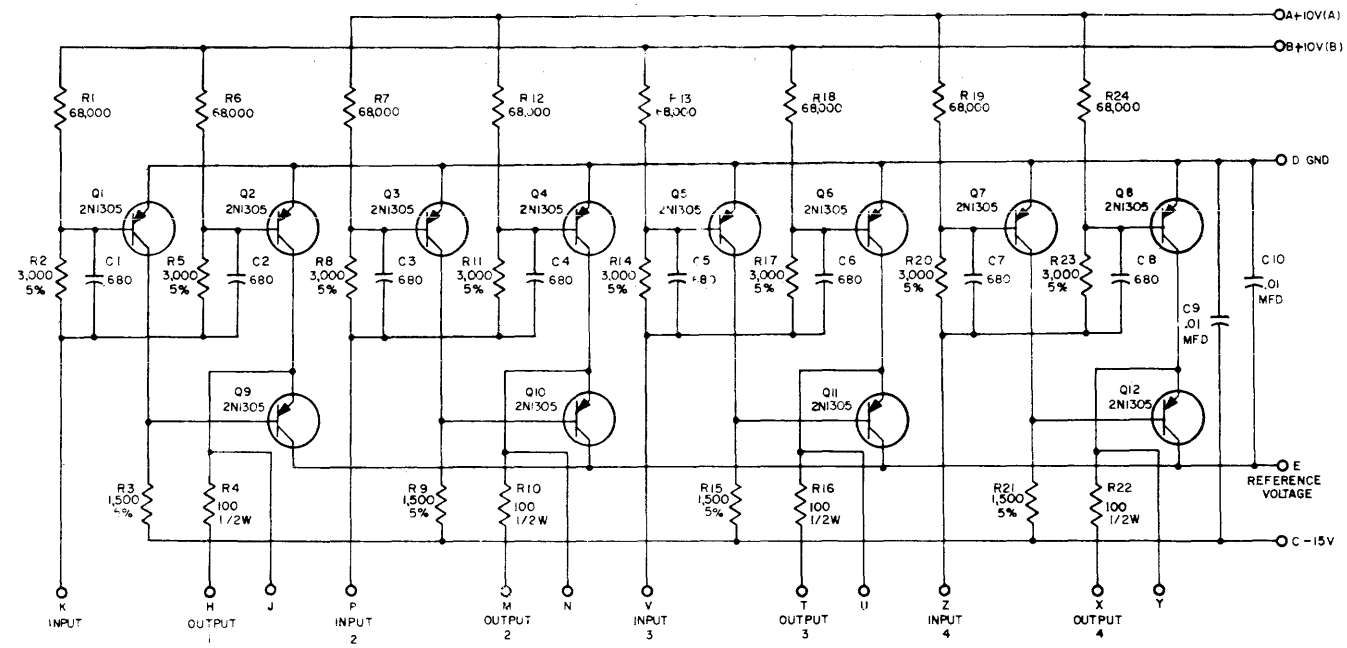
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N2714	2N2714	D-664	IN914
MDII4	2N1499A		
2N1309	2N1309		
D-001	IN276		
D-662	IN645		

NOTES

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

C	RS-4604	10
PULSE AMPLIFIER 4604		

RS-4677-4



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD

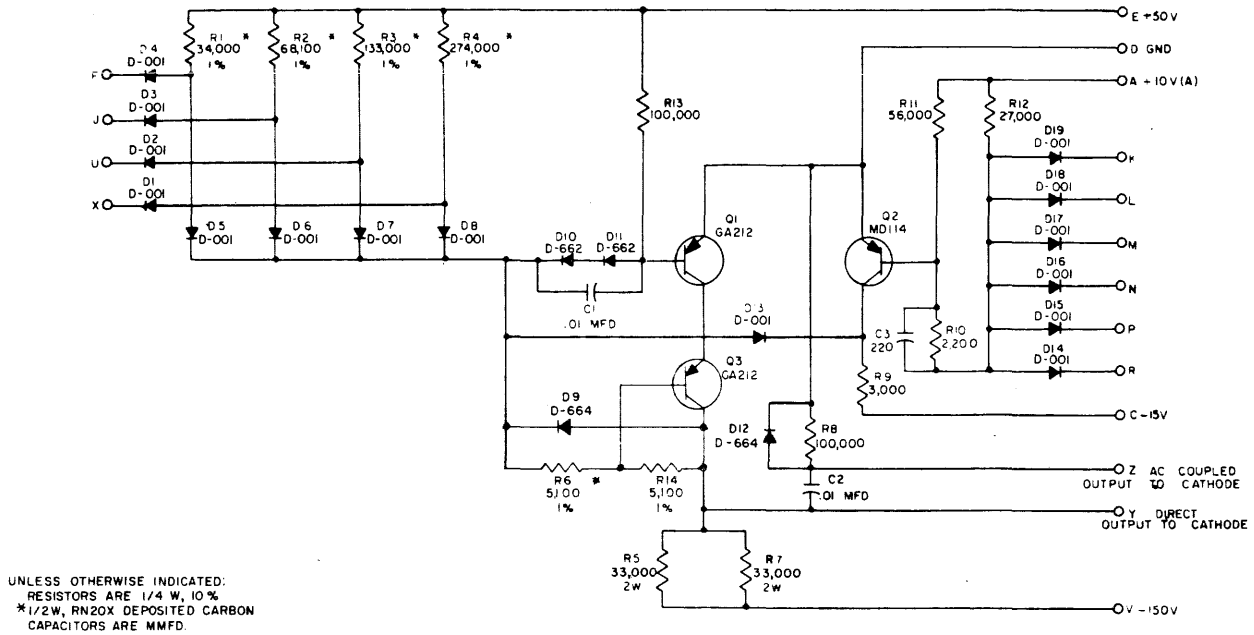
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N1305	2N1305		

NOTES

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

A,B,C,D	RS-4677	4
LEVEL AMPLIFIER 4677		

Figure 5-26 Type 4677 Level Amplifier Module Schematic



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
*1/2W, RN20X DEPOSITED CARBON
CAPACITORS ARE MMFD.

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
GA212	2N599		
MD114	2N1499A		
D-001	IN276		
D-662	IN645		
D-664	IN914		

NOTES

D	RS-4688	7
VARIABLE AMPLITUDE NEGATIVE INTENSIFIER 4688		

Figure 5-27 Type 4688 Variable Intensifier Module Schematic