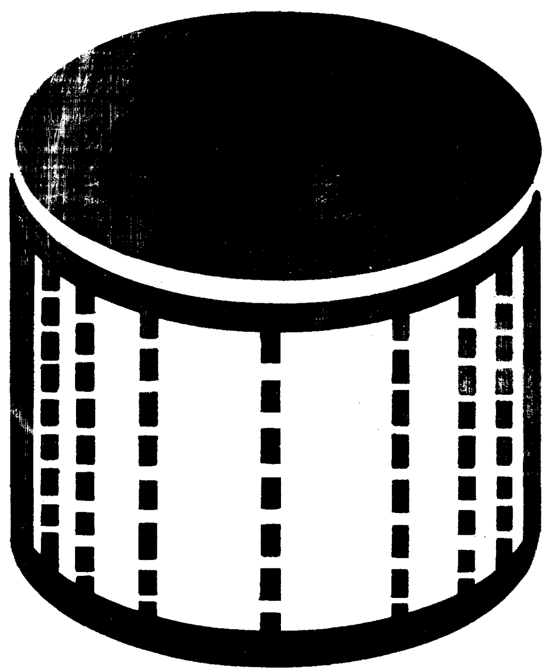
SERIAL DRUM / TYPE 24



SERIAL DRUM / TYPE 24

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

PREFACE

This manual contains information on the principles of operation, installation, operation, programming, and maintenance of the Digital Equipment Corporation Type 24 Serial Drum. The Serial Drum is designed for use as a data storage device to augment the main memory of a computing system. Section 1 of this manual presents information of a general nature which is applicable to the entire machine. Section 2 explains the principles of operation of the Serial Drum as a system and of each functional element of the system. Sections 3 through 6 present information and procedures which allow personnel to install, operate, program, and maintain the equipment. Reference material pertaining to the engineering drawings of the machine is contained in Section 7.

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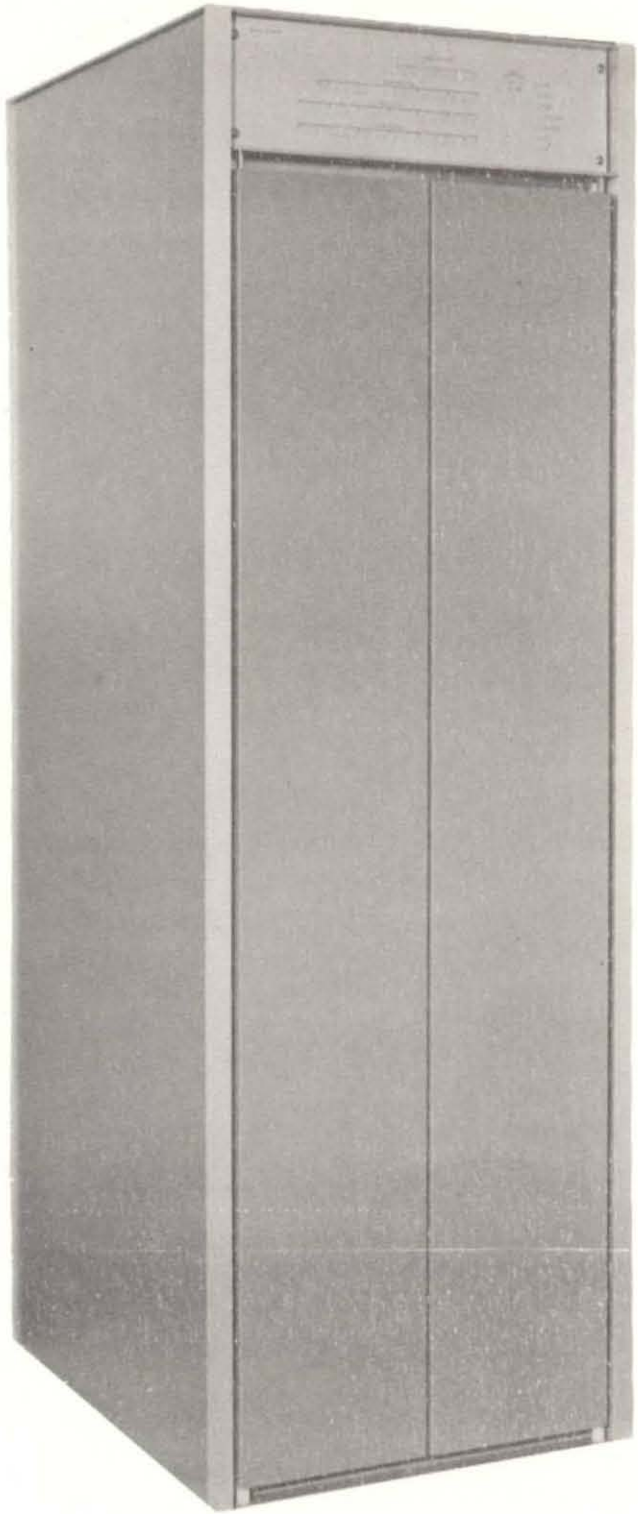


Figure 1-1 Typical Type 24 Serial Drum

SECTION 1

INTRODUCTION

The Digital Equipment Corporation (DEC) Type 24 Serial Drum system serves as an auxillary data storage device for either of the Programmed Data Processors PDP-1 or PDP-4. Information in the computer can be stored (written) in the Serial Drum and retrieved (read) in the blocks of 256 computer words. After programmed initialization, 256-word blocks of data are transferred between the computer and the Serial Drum automatically; transfer of each word being interleaved with the running computer program. Serial Drums are equipped to store either 64, 128, or 256 data blocks, providing a memory capability of 16384, 32768, or 65536 computer words. Each word is transferred between the computer and the Serial Drum in parallel (18 bits at a time) and is written or read on the drum surface in series (one bit at a time).

Since application of the Serial Drum is more common in a PDP-4 computing system than in a PDP-1 system, this manual and the engineering drawings assume the machine is connected to a PDP-4. When the Series Drum is connected to another computer, all references in this manual to signal origins and destinations and to data interrupt functions in the PDP-4 can be interpreted to refer to circuits performing similar functions.

FUNCTIONAL DESCRIPTION

The basic functions of the Type 24 Serial Drum are data storage and retrieval, core memory address control, track selection, data request and transfer control, error checking, and power supply and distribution. Functional operation of the machine is initiated by receipt of IOT pulses from the computer. Two computer instructions produce all of the IOT pulses required to enact a 256-word transfer between the computer and the Serial Drum.

A power supply and distribution network within the Serial Drum produces and controls the operating voltages required by all circuits of the machine. One source of external ac power is required to energize the machine; control of this source within the machine can be exercised locally or remotely.

In response to an IOT pulse the Serial Drum requests that the computer enter a data break to transfer a block of information. Eighteen-bit computer words are transferred to the Type 24 one word at a time and are written around the drum one bit at a time when the IOT pulse indicates a $\overline{\text{data in}}$ direction. Information bits are sensed on the drum one bit at a time, and transferred to the computer one word at a time when the IOT pulses indicate a data in direction of transfer. During a write cycle a parity bit is generated for each word received from the computer; so that 19-bit words are written on the drum surface. In reading data from the drum the parity of the word is checked to assure proper transmission. Error circuits in the machine check for parity error during read cycles and check data transmission timing during both read and write cycles. If bits are picked up or dropped out, if data received from the computer is late during a write cycle, or if data is late in being stored in the core memory during a write cycle, an error signal is sent to the computer.

Before transfers occur, the initial computer core memory address to send or receive data is set into a register in the Serial Drum. This register is automatically incremented by one at the end of each word transfer. Transfers of each block of 256 words is performed at one track, or address, in the drum. The track address is also transferred to the Serial Drum from the computer before transfer of the first word. At the completion of the transfer of the last word in a block this register is automatically incremented by one to simplify the programming of continuous block transfers on consecutive tracks.

Control circuits within the Serial Drum request the computer break cycle for each word transferred, indicate the completion of a block transfer by means of a flag, signal the detection or an error and the direction of the block transfer, in addition to performing the normal internal control operations.

PHYSICAL DESCRIPTION

The machine is constructed of a DEC computer cabinet 21 5/8 inches wide, 25 3/4 inches deep, and 67 7/16 inches high. All indicators are located on a panel at the front of the machine. Maintenance controls are located on the plenum door inside the double rear doors. Power and signal cables enter the cabinet through a port in the bottom. The power cable is permanently wired to the equipment and the two signal cables mate with connectors which are mounted on the front of the cabinet, facing the center of the machine. Four casters allow mobility of the machine which weighs 500 pounds with a 16384 or 32768-word memory, and 550 pounds with a 65536-word memory.

The cabinet is constructed of a welded steel frame covered with sheet steel. Double front and rear doors are held closed by magnetic latches. A full-width plenum door provides mounting for the power control, power supply, and switch panel inside the double rear doors. The plenum door is latched by a spring-loaded pin at the top. The indicator panel, racks of logic, and cable connector panel is attached to the front of a cabinet. Module racks are mounted on the front of the cabinet with the wiring side outwards, so that modules are accessible by opening the plenum door. A fan mounted at the bottom of the cabinet draws cooling air through a dust filter in the bottom, passes it over the electronic components, and exhausts it through openings in the cabinet. The memory drum housing is permanently mounted on braces above the fan assembly.

A coordinant system is used to locate racks, modules and cable connectors, and terminals. Each 5 1/4 inch position on the front of the cabinet is assigned a capital letter, beginning with A at the top, as indicated on Figure 1-2. Modules are numbered from 1 through 25 from left to right in a rack, as viewed from the wiring side. Connectors are numbered from 1 through 6, from left to right as viewed from the front of the machine. Blank module and connector locations are numbered. Terminals on a module connector are designated by capital letters from top to bottom. Therefore, D09E is in the fourth location from the top(D), the ninth module from the left (09), and the fifth (E) terminal from the top of the module. Components mounted on the plenum door are not identified by location. Engineering drawing E-10208 shows the system for locating terminal blocks and standoffs mounted on the logic racks. The location of printed-wiring boards in the memory drum housing is indicated on engineering drawing D-24619.

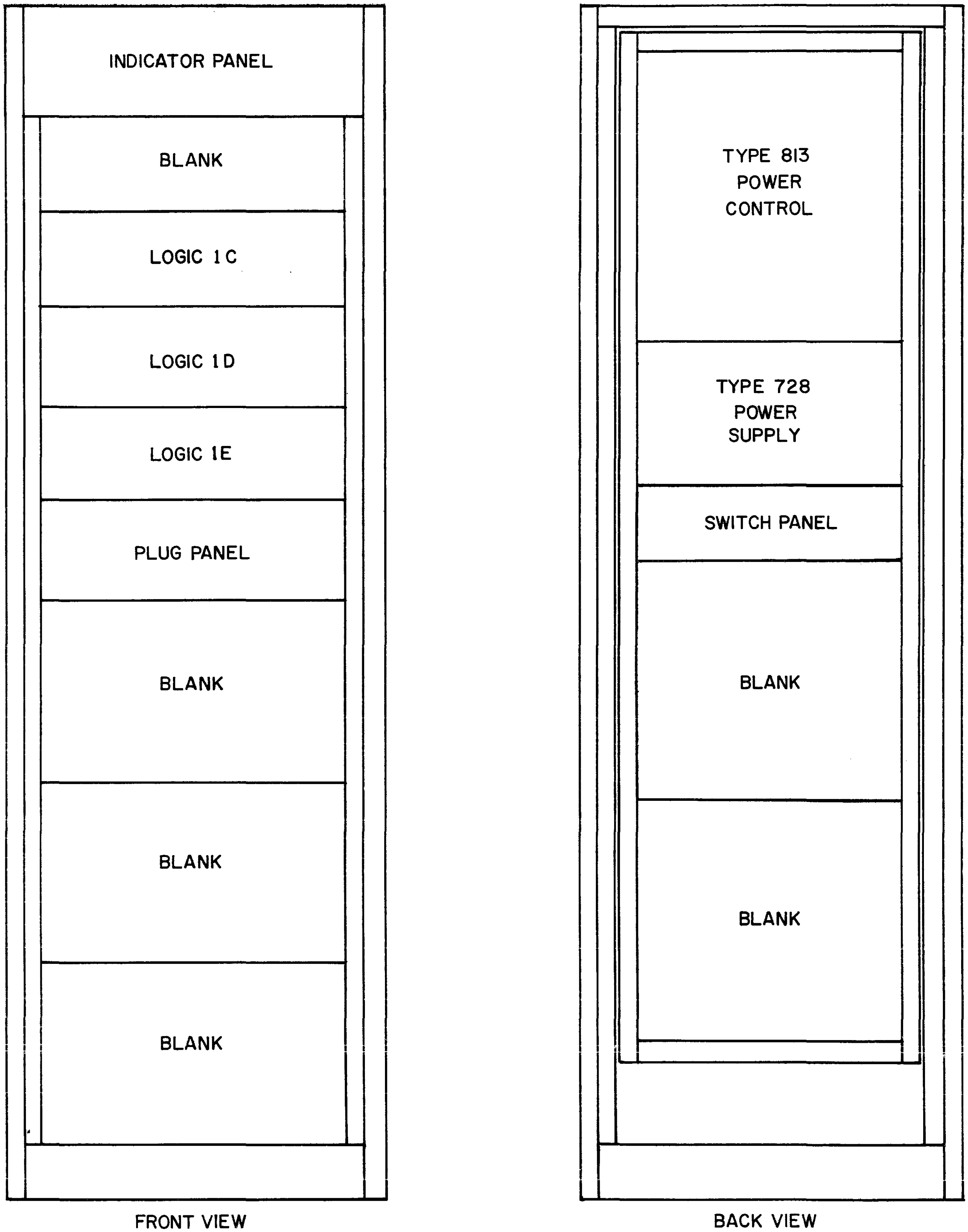


Figure 1-2 Component Locations

SPECIFICATIONS

Dimensions:	23 1/2 inches wide, 27 1/16 inches deep, 69 1/8 inches high
Service Clearances:	8 3/4 inches in front 14 7/8 inches in back
Weight:	500 pounds for 16,384- and 32,768-word memory 550 pounds for 65,536-word memory
Power Required:	115 volts, 60 cycles, single phase, 8-ampere starting current, 5-amperes running current
Power Dissipation:	450 watts
Power Control Point:	Local or remote (computer)
Initial Starting Delay:	10 minutes
Signal Cables:	Two, 50 wire, shielded
Temperature:	32 to 105 degrees F operating range 4 degrees F/minute maximum rate of change 20 degrees F maximum allowable instantaneous change
Drum Motor:	115 volts, single phase, 2 pole, induction, capacitor start and run
Magnetic Head Interference:	Maximum interchannel read cross talk at least 25 db below nominal signal level. Maximum noise in any channel at least 25 db below nominal signal level.
Write Current:	80 milliamperes
Pulse Repetition Rate:	3.5 microseconds
Word Transfer Time:	66.5 microseconds
Block Transfer Cycle: (1 drum revolution)	17.3 millisecond

ABBREVIATIONS

The following abbreviations are used throughout this manual and on engineering drawings.

AC	Accumulator in computer
ACB	Buffered outputs of Accumulator in computer

ABREVIATIONS (continued)

ACT	Active
AMP	Amplifier
AMPH	Amphenol connector
ANS	Answered
B	Break (computer state)
COMP	Complement
COND	Conditioned or enabled
DCL	Drum Core Location Counter in Serial Drum
DCT	Drum Control element in Serial Drum
DDC	Drum Data Channel in Serial Drum
DE	Data error
DF and DFB	Drum Final Buffer in Serial Drum
DIC	Data Interrupt Control in computer
DNG	Data No Good flip-flop
DS	Device Selector in computer
DSB	Drum Serial Buffer in Serial Drum
DT and DTR	Drum Track Address Register in Serial Drum
DTD	Drum Track Address Decoder in Serial Drum
EXT	External
F	As a subscript means final or last bit of information; the bit after the least significant data word bit.
IOS	Input Output Skip facility in computer
IOT	Input Output Transfer
MA and MAR	Memory Address Register in computer
MB	Memory Buffer Register in computer
PA	Pulse amplifier
PAR	Parity
PC	Power Control (Type 813)

ABREVIATIONS (continued)

PE	Parity error
PG	Pulse generator
PIC	Program Interrupt Control in computer
R	Read
RD/WR	Read/Write flip-flop
RQ	Request flip-flop
R/WP	Read/Write Parity element in Serial Drum
S	As a subscript means the first or initial bit of information; the bit preceding the most significant data word bit.
SA	Sense amplifier
TRA	Transfer
WD	Write Data flip-flop
XA	Most significant octal digit of X address
XB	Least significant octal digit of X address
YA	Most significant octal digit of Y address
YB	Least significant octal digit of Y address

SECTION 2

PRINCIPLES OF OPERATION

RECORDING AND PLAYBACK TECHNIQUE

The Type 24 Serial Drum utilizes Manchester non-return-to-zero (NRZ) or phase modulation recording to enhance the operating margins at the high densities used. This recording technique produces playback head voltages which are either fully positive or fully negative at read strobe time. Therefore the effective playback signal is twice the amplitude of that produced by other recording methods in which the sense amplifier must discriminate between the presence or absence of uni-directional flux. Data and signal patterns produced in recording and playback of information in the Serial Drum are indicated in Figure 2-1.

BLOCK DIAGRAM DISCUSSION

Major functional elements of the Serial Drum are shown in Figure 2-2. Complete information transfer flow and timing of operations in the Serial Drum are indicated in engineering drawings D-24611 and C-24612.

Drum Core Location Counter (DCL)

The DCL is shown on engineering drawing D-24604 to be a 16-bit flip-flop register which contains the computer core memory address to or from which the next word is to be transferred. Before transfer of the initial word in a block, the address of the first word is set into the DCL from the computer accumulator. As each word is transferred the DCL is automatically incremented by one.

Drum Track Address Register (DTR)

The DTR is an 8-bit flip-flop register which contains the address of the drum track selected for transfer of a data block. The drum track (which may be considered as the data block address in the drum or as the address of the selected drum head) is set into the Serial Drum, during program initialization, from the accumulator of the computer. At the completion of a successful block transfer (if the $DE^0 \cdot PE^0$ flag is a 0) the DTR is incremented by one to simplify

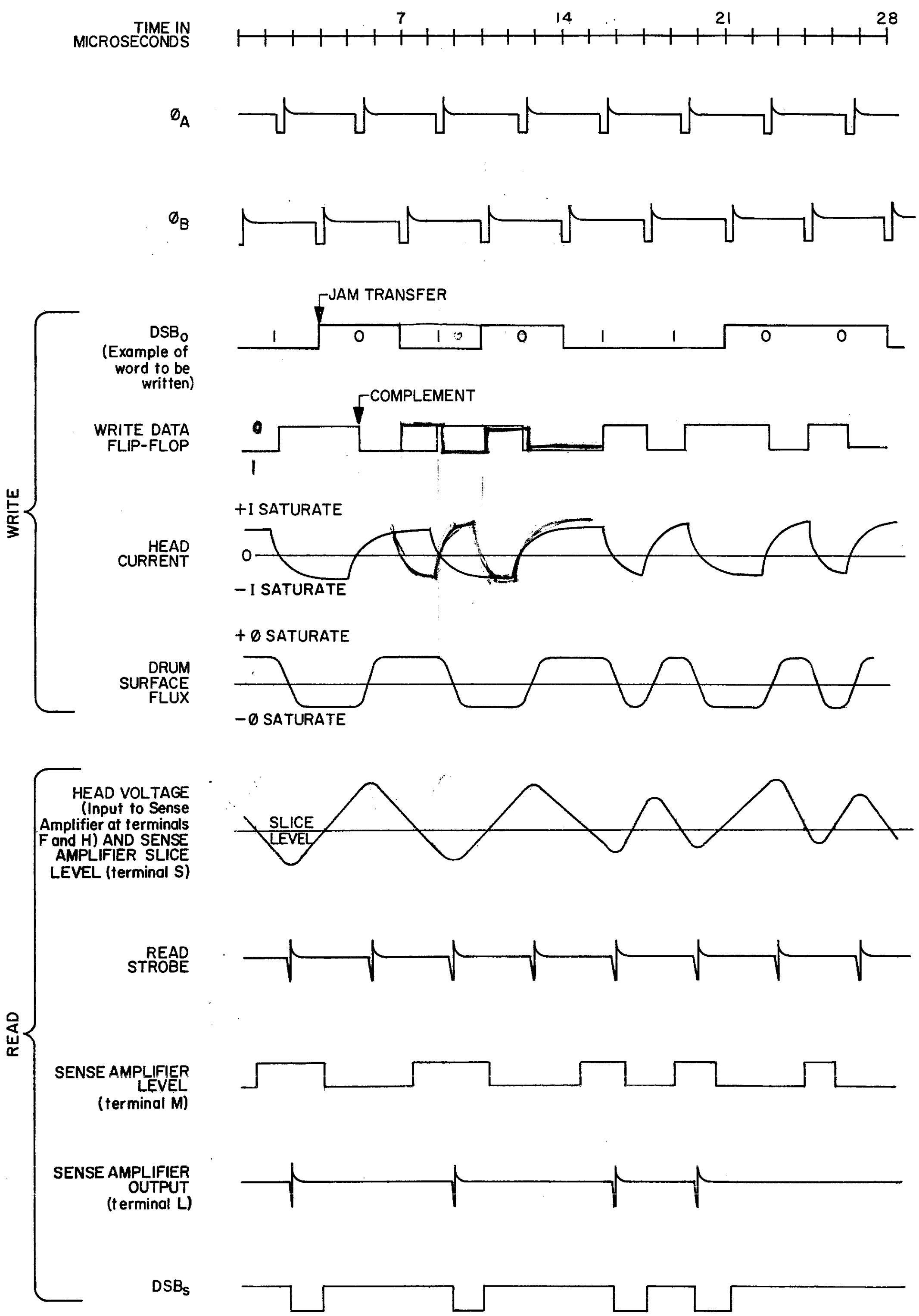


Figure 2-1 Typical Recording and Playback Timing

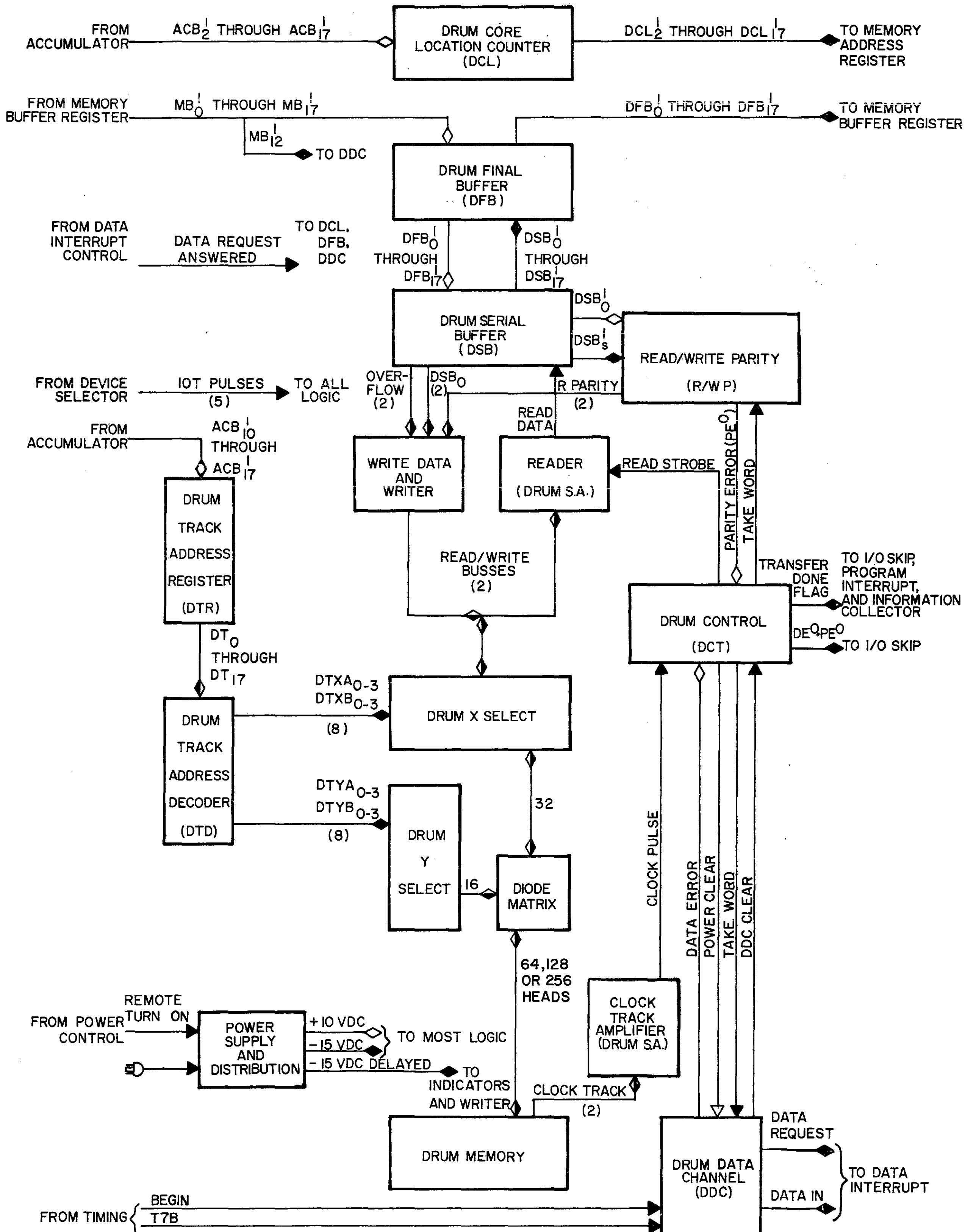


Figure 2-2 Type 24 Serial Drum Block Diagram

programming of continuous transfers at successive drum tracks. Engineering drawing D-24607 shows the DTR.

Drum Track Address Decoder (DTD)

Half of the drum track selection is performed by decoding of the DTR flip-flop outputs in the DTD. As shown on engineering drawing D-24607, the DTD consists of two groups of eight 2-input diode gates, one group for the X address and one for the Y address. The eight X address outputs function as a two-digit octal address which is further decoded in the Drum X Select logic. The eight Y address outputs serve a similar function.

Drum Head Selection

Final selection of a drum head is performed in the Drum X and Y Select circuits shown on engineering drawing E-24608 and in the diode matrix within the drum housing. The 16 FIELD LOCKOUT switches each inhibit a Type 4521 Drum X Select Module when closed and so prevent accidental writing in 16 addresses.

Drum Sense Amplifiers

Two Type 1537 Drum Sense Amplifier modules convert information sensed by the magnetic heads of the drum into digital pulse data. Information recorded on a clock track is sensed by the clock head and supplied to the sense amplifier shown on drawing D-24603 as the Clock Track Amplifier. The output from this sense amplifier is applied to the Drum Control (DCT) to establesh the basic clock rate of all drum operations. The sense amplifier shown on drawing D-24602 as the Reader samples the signals picked up by the selected data head and produces a pulse to set a 1 into the Drum Serial Buffer (DSB) when the read strobe signal occurs during the maximum negative excursion of the head signal.

Drum Control (DCT)

The basic timing pulses for the machine are generated in the DCT from pulses received from the Clock Track Amplifier. The DCT also contains a 4-state device consisting of four negative diode gates. Each state of this device corresponds with and initiates one of the four machine control states: idle, transfer, active, or transfer done. This logic is shown on engineering drawing D-24603.

Drum Data Control (DDC)

Engineering drawing D-24605 shows the DDC. Circuits within the DDC control the transfer of each word between the computer and the Drum Serial Buffer. The DDC establishes the read/write status of the machine, makes the data break request for a computer break cycle, indicates the detection of an error, and designates the direction of the ensuing data transfer.

Drum Final Buffer (DFB)

The DFB is an 18-bit register which serves as a buffer between the computer Memory Buffer Register and the Drum Serial Buffer. Words are transferred in parallel (18 bits at a time) under control of the computer Data Interrupt Control. During the drum writing, DFB holds the <u>next</u> word. During drum reading, DFB is empty and is prepared to accept information read from the DSB and place it into core memory under control of the Data Interrupt Control. The logic circuits which compose the DFB are shown on engineering drawing D-24606.

Drum Serial Buffer (DSB)

As shown on the top and left side of engineering drawing D-24602, the DSB is an 18-bit shift register which is a serial-to-parallel-converter during drum reading, and a parallel-to-serial-converter during drum writing. Information is read from the drum into DSB serially and transferred to DFB in parallel. During drum writing, a word is read from DFB into DSB and written serially around the drum.

Read/Write Parity (R/WP)

As each bit of a word is written on the surface of the drum, the R Parity flip-flop counts the number of binary 1s and produces a 19 bit to provide an odd parity. When data is read from the drum this flip-flop counts the 1s again and sets the Parity Error flip-flop if an even number is detected in any one word. The condition of the Parity Error flip-flop is indicated in the DCT as one of the two possible causes of an error condition. These circuits are shown in area C4 and C5 of engineering drawing D-24602.

Write Data and Writer

Druing a write cycle data is presented on the read/write busses for recording on a selected drum track by the Type 4518 Drum NRZ Writer module. The data is written as a function of the

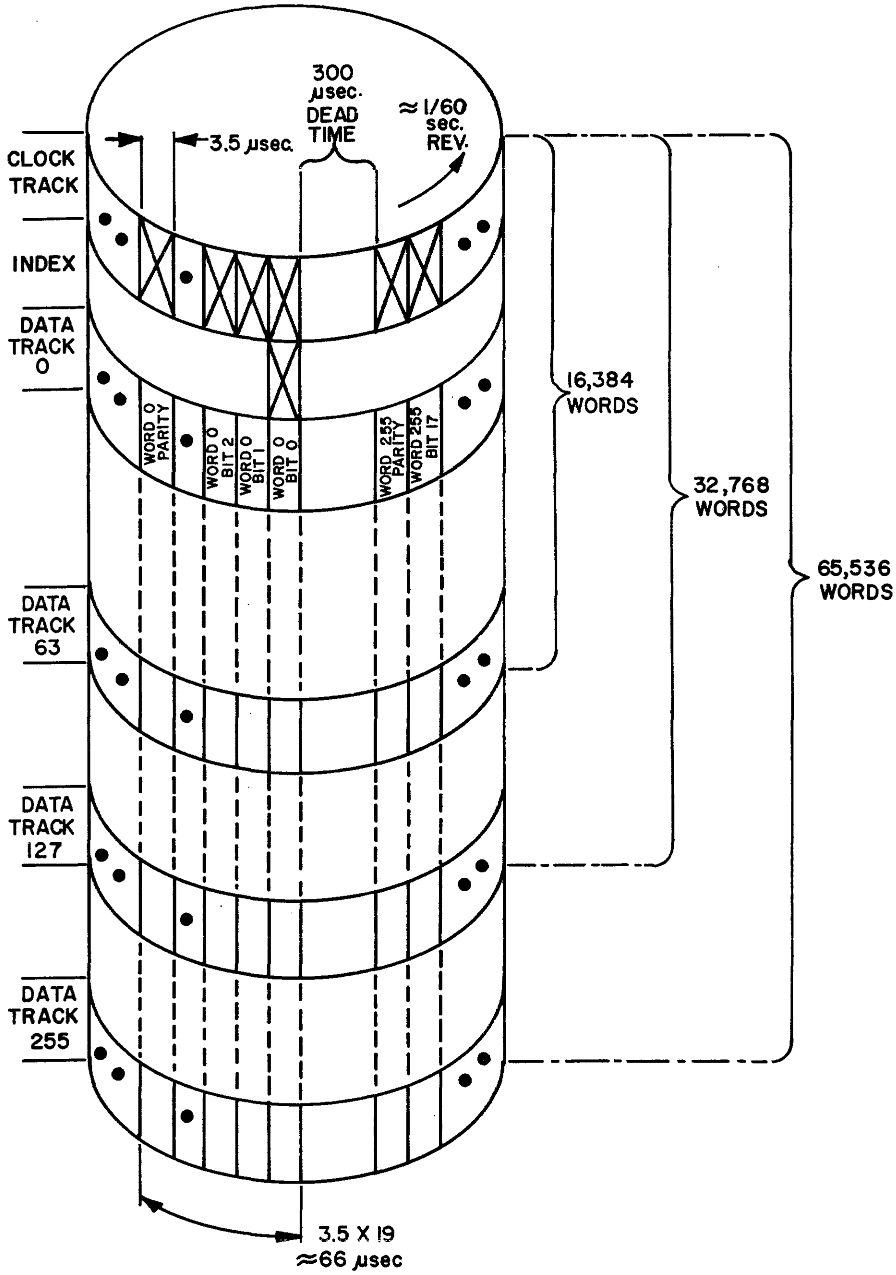


Figure 2-3 Drum Surface Information

contents of the most significant bit of the DSB. This logic is shown in the lower right corner of engineering drawing D-24602.

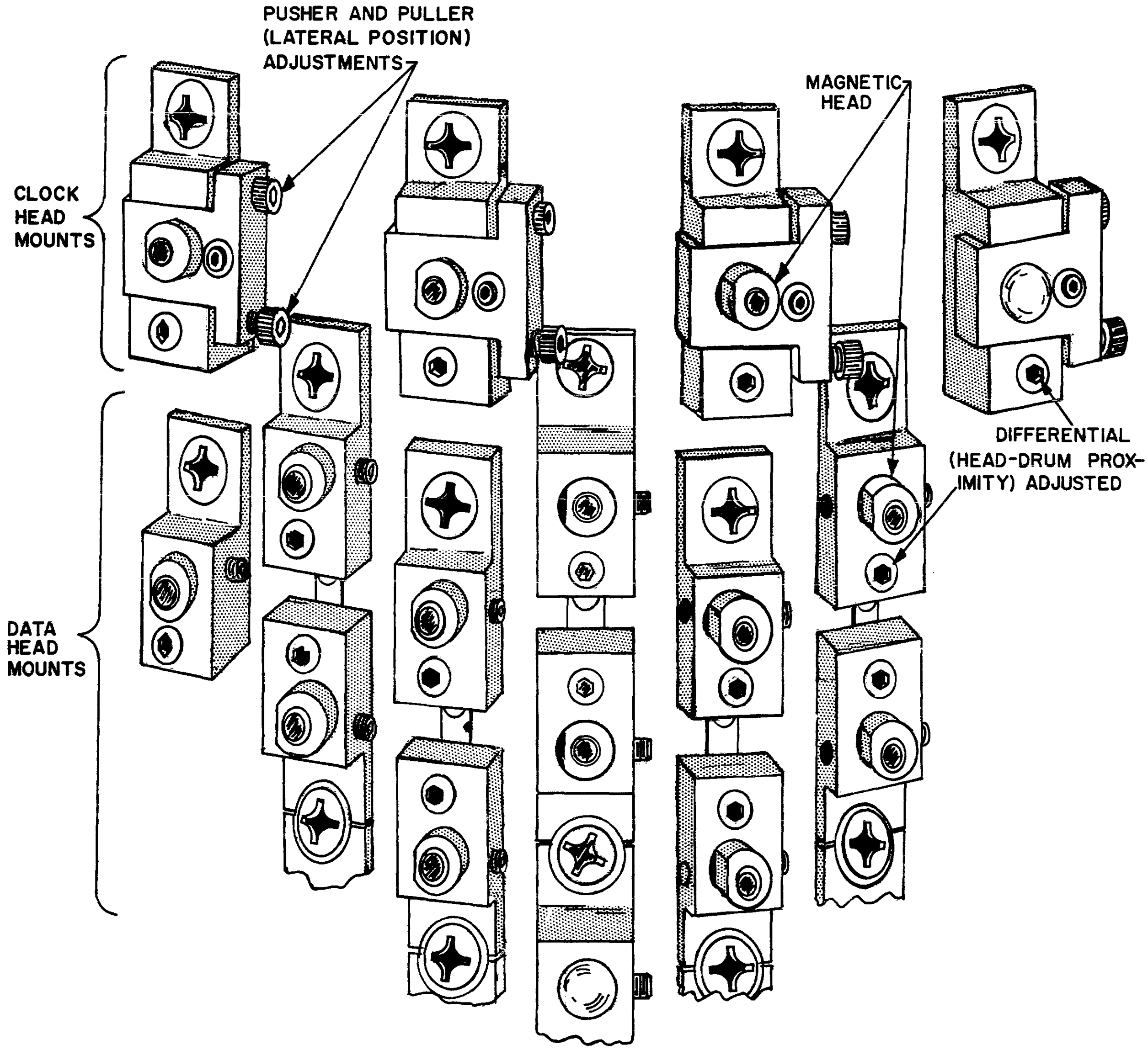


Figure 2-4 Drum Head Configuration

Drum Memory

The rotating drum assembly is designed with minimum cross-section for proper heat transfer and dissipation. It is mounted on separable inner-ring angular-contact bearings which are pre-lubricated for life. Preloading is accomplished by springs at the top end of the unit.

The magnetic coating on the surface of the drum is "GRIMACO" # 6037-X high density dispersion, heat-cured and lapped to its final finish. Dynamic runout is less than 0.0001 inch total indicator reading.

The motor which turns the drum is of special design to provide the fastest starting time compatible with minimum power input and losses at synchronous speed. The fan for this single-phase, two-pole, induction, capacitor-start and run motor is fastened to the bottom of the spindle. Ambient air is drawn through a shroud and over the finned motor housing. This air current takes away heat from the motor preventing localized temperature rise.

Four panels allow ready access to the drum without disassembly of signal or power connectors. Thus, adjustments of spacing or clock bit alignment can be made under operating conditions. The drum housing is designed so that the fan action of the drum circulates air around the drum and head mounts so that the temperature differential is kept to a minimum within the housing. This internal circulation, together with the external discharge from the motor fan, also tends to maintain a minimum differential from inside to outside so that repeated stops and starts can be made without endangering head contact. Actual limits of ambient temperatures should be maintained to 55° Fahrenheit and 115° Fahrenheit with a rate of change not to exceed 15° Fahrenheit per hour.

The location of tracks and words on the drum are indicated schematically in Figure 2-3 and the relative position of head mounts and the major components of the mounts are shown in Figure 2-4.

Power Supply and Distribution

The Serial Drum operates fron a single source of 115-volt, 60-cycle, single-phase power. Control and overload protection of this power within the machine is exercised by a Type 813 Power Control. Operation of the power control can be controlled by the MAINT ON/OFF switch on the switch panel or by means of a contact closure provided by the computer. The ac output of the power control operates the drum motor, fan motor, and the Type 728 Power Supply. The -15 volt output of this supply which operates the indicator panel is controlled by a 10 minute time delay relay in the power control. Therefore the indicators do not light until ten minutes after the drum motor has been energized, at which time the drum has reached synchronous speed and is ready to transfer data.

The Type 728 Power Supply produces the normal module operating voltages of +10 vdc and -15 vdc. These outputs are connected to each rack of logic through a color-coded connector and a toggle switch at the right side of each rack, as seen from the module side. Marginal-check terminals are provided on these connectors which are connected in common to all racks, so that an external power supply can be connected to any connector to marginal check all racks. The color coding of these connectors is as follows, from top to bottom:

a. Green, + 10 vdc marginal-check supply
b. Red, + 10 vdc internal supply
c. Black, ground
d. Blue, -15 vdc internal supply
e. Yellow, -15 vdc marginal-check supply

Three single-pole double-throw switches at the end of each rack of logic allow selection of either the normal internal power supply or the external marginal-check power supply for distribution to the logic. The top switch selects the +10 volt supply routed to terminal A of all modules in that rack. In the down position the fixed internal +10 volt supply connected to the red terminal is supplied to the modules, and in the up position the marginal-check voltage supplied to the green terminal is supplied to terminal A of the modules. The center switch performs the same selection as the top switch for connection of a nominal +10 volt level to terminal B of all modules. The bottom switch selects the -15 volt supply to be routed to terminal C of all modules. In the down position the fixed -15-volt output of the internal power supply, received at the blue terminal, is supplied to the modules while in the up position the marginal-check voltage, connected to the yellow terminal, is supplied to terminal C of all modules.

WRITE CYCLE

Two IOT commands write a block of 256-words on a drum track. IOT 706046 clears the Drum Core Location Counter and clears the Drum Final Buffer. It then loads the Drum Core Location Counter with the contents of AC_{2-17}, the computer Information Distributor. This information
? indicates the core memory address of the first word to be transferred. The Read-Write flip-flop is set to write and a level (data request) is sent to the computer. When the break cycle is executed in the computer, the Memory Address Register is set to the core memory location specified by the Drum Core Location Counter, the Drum Core Location Counter is incremented by one, and information is read from core memory to the Memory Buffer Register. At the end of the break cycle a Data Request Answered pulse is sent to the drum and the word in the Memory

data request answered

Buffer Register is transferred to the Drum Final Buffer. When the request is made the Data No Good (DNG) flip-flop is set to a 1 and the Data Request Answered signal clears this flip-flop. If another request is initiated before the DNG flip-flop is cleared, signifying that incorrect information is in the Drum Final Buffer, a Data Error (DE) results.

The second IOT 706106 clears the Drum Track Address Register and the error flip-flops at time pulse 7, and then loads the track address into the DTR at time pulse 1 of the next cycle. A computer break cycle is initiated to bring the first word to be written from the DFB to the DSB and loads DSB_S unconditionally with a binary 1 and brings the second word to be written from core memory into the DFB. After a delay of 200 microseconds the transfer request (TRA) state is set. This delay allows the track selection capacitor-diode gates to set up. After a period of 0 to 17 milliseconds (up to one drum revolution time) the clock track initiates the first timing pulse and the system timing passes to the drum. At the $\emptyset_B$ clock time the DSB is shifted, bringing the next bit to be written into the DSB_0 flip-flop and bringing a 0 into the DSB_S. At this time the bit arriving in the DSB_0 is jammed into the Write Data flip-flop. At the $\emptyset_A$ time the Write Data flip-flop is complimented, creating the proper flux transition on the drum surface. After 18 bits have been written all zeros will exist in the DSB and a 17-input AND gate will detect this condition and create an overflow. As each of the 18 bits is written the R Parity flip-flop is complimented for each 1 recorded. Since this flip-flop was originally set to 1, after the 18th bit is written it contains the proper odd parity bit. When the overflow occurs the state of this flip-flop is jammed into the Write Data flip-flop and is recorded as the odd parity bit.

After the parity bit is recorded a data request is made to the computer. The present contents of the DFB are read into the DSB and the next word to be written is brought into the DFB via a request to the computer. After 256 words are written, a flag is sensed in the Program Interrupt and the decision to continue writing the next block, or to initialize a new core memory location and track address, or to halt, is made by the program. A continue instruction writes the next block of 256 words. This instruction may be given any time during the 300 microsecond gap which exists in the timing track. At the completion of each block transfer the Drum Track Address Register is incremented, addressing the next track.

READ CYCLE

Two IOT commands read a block of 256 words. IOT 706006 clears the Drum Core Location Counter, clears the Drum Final Buffer and loads the Drum Core Location Counter from the Information Distributor (AC_{2-17}) with the core memory address into which the first word will be read from the drum. The Read/Write flip-flop is set to the read status and produces the Data In signal which is supplied to the computer. This signal inhibits generation of the core read strobe pulse so that the Memory Buffer Register remains cleared and allows insertion of new data. IOT 706106 clears the Drum Track Address Register at T7 time and loads the new track address, from which information is to be read, at the next cycle. A binary 1 is unconditionally loaded into DSB_{17} and 200 microseconds later a transfer request state (TRA) is set. When the first timing mark on the drum occurs the transfer commences. Bit one is read into DSB_S. For each 1 that is read the R Parity flip-flop, which was originally set to 1, is complimented. After reading nineteen bits and shifting the information through the DSB, DSB_{17} arrives at DSB_F and an overflow condition is created. This overflow initiates a Take Word signal which transfers the assembled word in the DSB into the DFB. It creates a data request condition in the computer so that the Memory Buffer Register takes the word in DFB and inserts it in core memory at the address specified by the DCL. This Take Word signal tests the state of the R Parity flip-flop. Since R Parity was originally set to 1, and each 1 that was read into DSB compliments R Parity, then at the end of 19 bits (18 bits plus the parity bit) the R Parity flip-flop must contain a 0 if the parity was correct during writing and the correct number of 1s and 0s were read. If R Parity is a 1 at Take Word time a parity error will result. The computer has 66 microseconds in which to take the word which exists in the DFB and insert it in core memory, so that the DFB may be cleared and ready to receive the next word from DSB. At the end of a 256-word transfer the drum transfer done flag is set to 1 and creates a program interrupt. The programmer now has the option of giving a continue instruction to bring the next successive block of 256 words into core memory, initializing a new core memory location and track address, or terminating the transmission.

SECTION 3

INTERFACE

All logic signals which pass between the computer and the Serial Drum are standard DEC levels or standard DEC pulses. A standard DEC level is either ground potential (0.0 to -0.3 volts) or -3 volts (-3.0 to -4.0 volts). Standard DEC pulses are 2.5 volts in amplitude (2.3 to 3.0 volts) and are 0.4 microsecond in duration. Positive pulses are referenced to the standard negative level and negative pulses are referenced to ground potential.

Throughout the manual standard DEC ground-potential signals are symbolized by an open diamond and standard DEC negative levels are indicated by a solid diamond. Open and solid arrow heads are used to symbolize standard DEC positive and negative pulses, respectively.

In addition to the logic signal inputs a contact closure in the computer power control circuit provides the remote turn on signal to the power supply and distribution network in the Serial Drum. This signal is used to energize or de-energize the Serial Drum from the computer in normal operation. The effect of this signal can be disabled during maintenance operations to control power application and removal via a switch on the Serial Drum.

Input signals to the Serial Drum are listed in Table 3-1 and output signals are listed in Table 3-2. Numbers in the Serial Drum Drawing column of these tables indicate the engineering drawing number when prefixed by D-246. The letter and number following the colon indicates the horizontal and vertical coordinates on the engineering drawing where the signal can be found. Signal origins in Table 3-1 and signal destinations in Table 3-2 are given for interface with a PDP-4 computer. When planning interface between the Serial Drum and another computer these tables can be used as a guide for connection to circuit elements performing similar functions.

Note that input signal levels to the DCL, DFB, DTR, and DDC must be present for at least 3 microseconds before receipt of the IOT pulse or T7B pulse which strobes the data contents into the flip-flops. This delay is required to allow settling of the capacitor-diode gate at the input of each flip-flop.

TABLE 3-1 INPUTS TO 24 FROM PDP-4

Signal Name	Symbol	From PDP-4		To Serial Drum		Function
		Logic	Drawing	Logic	Drawing	
ACB^1_{10} thru ACB^1_{17}	—◇	AC (ID)	D-4-00-01-04 D-40004-3	DTR	07:C	Provides track address to be strobed into DTR by IOT 6104 pulse.
ACB^1_2 thru ACB^1_{17}	—◇	AC (ID)	D-4-00-01-03 D-4-00-01-04 D-40004-3	DCL	04:B	Provides initial address of data transfer into DCL.
Begin	—▷	Keys	D-4-00-C1-01	DDC	05:B1	Produces "DDC CLEAR" signal.
Data Request Answered (equals Data•B•T1) (Data Address ⇒MA)	—▶	DIC	D-40004-1	DCL DDC DFB	04:C2 05:B2 06:D1	Produces "DCL + 1" signal which increments DCL. Clears REQUEST (RQ) flip-flop. Produces "DF CLEAR" signal in Write mode.
IOT 6002	—▶	DS	D-40004-4	DCL DDC DFB	04:C1 05:B1 06:D1	Produces "DCL CLEAR" signal. Produces "DDC CLEAR" signal. Produces "DF CLEAR" signal.
IOT 6004	—▶	DS	D-40004-4	DCL DDC DSB	04:B1 05:B2 02:C1	Strobes ACB_{2-17} information into DCL. Strobes MB^1_{12} into RD/WT, RQ, and DNG flip-flops. Produces "TAKE WORD" signal if MB_{12} is a 1.

TABLE 3-1 INPUTS TO 24 FROM PDP-4 (continued)

Signal Name	Symbol	From PDP-4		To Serial Drum		Function
		Logic	Drawing	Logic	Drawing	
IOT 6102	——▶	DS	D-40004-4	R/WP DCT DTR DDC	02:C5 03:B1 07:C1 05:B3	OR to clear PAR ERROR flip-flop. OR to set IDLE to 1. Produces "DT CLEAR" signal. OR to clear DATA ERROR (DE) flip-flop.
IOT 6104	——▶	DS	D-40004-4	DCT DCT DCT DTR	02:C1 02:D3 03:C1 07:C2	Produces "TAKE WORD" signal in Write mode. Produces "DSB INITIAL CONDITION" signal in Read mode. Sets TRANSFER REQUEST (TRA) to a 1 after 200 nsec delay. Strobes ACB_{10-17} information into DTR.
IOT 6204	——▶	DS	D-40004-4	R/WP DDC DCT	02:C5 05:B3 03:B2	OR to clear PAR ERROR flip-flop. OR to clear DATA ERROR (DE) flip-flop. OR to set TRA to a 1.
MB^1_0 thru MB^1_{17}	——◇	MB	D-4-00-01-06	DFB	06:C	Provides data read from core memory to be written on the drum.
MB^1_{12}	——◇	MB	D-4-00-01-06	DDC	05:B2	Controls setting of RD/WR^1, RQ, and DNG flip-flops by IOT 6004 pulse.
Remote Turn On	Contact Closure	Power Control		PSD	None	Energizes drum from computer START key.

TABLE 3-1 INPUTS TO 24 FROM PDP-4 (continued)

Signal Name	Symbol	From PDP-4		To Serial Drum		Function
		Logic	Drawing	Logic	Drawing	
T7B	⟶	Timing	D-4-00-01-01	DDC	05:D3	Produces a "T7C" pulse after 1 nsec which clears the DFB in the Read mode, increments the DFB in the Write mode, and clears the DATA NO GOOD (DNG) flip-flop in the DDC.

TABLE 3-2 OUTPUTS FROM 24 TO PDP-4

Signal Name	Symbol	From Serial Drum		To PDP-4		Function
		Logic	Drawing	Logic	Drawing	
Data In	—◆	DDC	05:C2	DIC	D-40004-1	Indicates the direction of data transfers. Data passes into the computer from the drum when this signal is at -3 volts.
Data Request	—◆	DDC	05:C2	DIC	D-40004-1	Indicates the Serial Drum is ready for data transfer.
DCL_2^1 through DCL_{17}^1	—◆	DCL	04:B	MAR(DIC)	D-4-00-01-05	Holds the core memory address for the next word to be transferred.
$DE^0 \cdot PE^0$	—◆	DCT	03:D3	IOS	D-40004-1	Indicates that no data errors and no parity errors have occurred when at the -3 volt level.

TABLE 3-2 OUTPUTS FROM 24 TO PDP-4 (continued)

Signal Name	Symbol	From Serial Drum		To PDP-4		Function
		Logic	Drawing	Logic	Drawing	
DFB^1_0 through DFB^1_{17}		DFB	02:B	MB (DIC)	D-4-00-01-06	Provides data read from drum which is to be written in core memory.
Transfer Done Flag		DCT	03:A4	IOS PIC	D-4004-1	Signals completion of a block transfer when reverting to -3 volts (Nominally ground level).

SECTION 4

INSTALLATION AND OPERATION

SITE REQUIREMENTS

The installation site must provide floor space at least 14 inches wide and 28 inches deep to accomodate the Serial Drum. At least 9 inches must be provided in front of the cabinet and 15 inches at the back of the cabinet to allow opening of the doors for maintenance.

A source of 115-volts (±17 volts), 60 cycle, single-phase power must be supplied by the site. This source must be capable of supplying the 8.0-ampere starting surge current and 5.0-ampere running current required by the Serial Drum.

Ambient temperature at the installation site can vary between 32 and 105 degrees Fahrenheit (0 to 41 degrees Centigrade) without deleterious affect upon equipment operation. For normal operation an ambient temperature range from 70 to 85 degrees Fahrenheit is recommended. Note that rapid changes in temperature adversely affect the operation of the drum memory only when the covers are removed. Therefore, the installation site should be capable of maintaining a relatively stable temperature during drum maintenance, such as during the drum head spacing checks.

SIGNAL AND POWER CONNECTIONS

All signal connections to the Type 24 Serial Drum are made at connectors F1 and F2 on the plug panel at the front of the machine. To mate with these connectors, a cable should contain an Amphenol connector of the 115-114P series with a housing 1391 and wire clamp 3057. Maximum signal cable length should not exceed 25 feet. The input and output signals are defined in Tables 3-1 and 3-2 and their wiring connections are given on sheets 1 and 2 of the engineering drawing A-24614.

A grounded, three-wire power cable is permanently attached to the machine. A standard three-prong male power plug at the end of this cable allows connection to a power source at least 18 feet from the cabinet.

CONTROLS AND INDICATORS

All manual control of the Serial Drum is exercised by means of toggle switches on the switch panel at the rear of the machine. The function of these switches is as follows:

MAINT ON / OFF	Allows maintenance personnel to select the normal or stop-on-error mode of operation. In the OFF position the equipment functions normally and data errors or parity errors can be detected via the error flag only at the end of a 256-word block. In the ON position detection of data error or parity error by the machine inhibits generation of clock signals ($\emptyset_A$, Read Strobe, and $\emptyset_B$) so that all data transfer stops and the contents of all registers can be observed to locate the cause of the error.
REMOTE ON/OFF/LOCAL ON	Allows local or remote control of machine energization. In the REMOTE ON position the machine is energized by a contact closure in the computer. The OFF and LOCAL ON positions function as a normal power switch.
FIELD LOCKOUT (0 through 7 and 10 through 17)	Each switch allows a group of 16 consecutive tracks (4096 words) to be inhibited during writing so that the information stored on those tracks cannot be accidentally destroyed.

Visual indication of the machine status and register contents is given on the indicator panel. The functions denoted by these lamps are as follows:

TRACK ADDRESS (8)	Light to indicate ONEs in the Drum Track Address Register.
CORE LOCATION (16)	Light to indicate ONEs in the Drum Core Location Counter.
FINAL BUFFER (18)	Light to indicate ONEs in the Drum Final Buffer.
SERIAL BUFFER (18)	Light to indicate ONEs in the Drum Serial Buffer.

READY (RD and WR) (2)	Indicate the machine is in either the read or write mode. Either of these lamps light to indicate that the initial delay following energization of the power control has elapsed and the machine is ready for use.
TRA	Lights to acknowledge receipt of IOT pulses and indicate that the machine has been taken out of the idle state and is waiting for clock pulses to be read from the drum to assure that the drum is in the correct position before initiating a transfer.
ACT	Lights to indicate that the machine has been taken out of the transfer state and is actively engaged in a data transfer.
FLAG	Lights to indicate that a block transfer has been completed and the machine has been taken out of the active state. The machine remains in this state until the flag is cleared when the machine is set to either the idle or the transfer state.
OVERFLOW	Lights to indicate that a 19-bit word has been assembled in the DSB and is ready for transfer to the DFB in the read mode, or that a 19- bit word has been transferred from the DSB to the drum in the write mode.
REQUEST	Lights to indicate that a data request signal has been sent to the computer to request a data break to transfer a word.
PE	Lights to indicate that the machine has detected a parity error after read-in from drum to core. If the MAINT ON/OFF switch is OFF when a parity error occurs, the drum error flag is set to 1; if the switch is ON, the flag is set to 1 and the transfer is terminated.
DE	Lights to indicate that the machine has detected a data error, in that the data request signal from the drum was not answered within the 66 microsecond period required (when reading a data word is therefore incorrect in the computer core memory

DE (continued)

or when writing the next word to be written has not been received by the DFB). If the MAINT ON/OFF switch is OFF when a data error occurs, the drum error flag is set to 1; if the switch is ON, the flag is set to 1 and the transfer is terminated. This condition occurs either because devices with higher priority are connected to the Data Interrupt Control, or because the instruction being executed at the time of the data request takes longer than 66 microseconds for completion.

EQUIPMENT TURN-ON AND TURN-OFF

Operation of the Type 24 can be controlled locally by operation of a switch, or remotely from a signal received from the computer. Control point is selected at the REMOTE ON/OFF/ LOCAL ON switch on the switch panel. In normal use this switch is left in the REMOTE ON position with the circuit breaker in the ON position. For maintenance operations this switch is set to the LOCAL ON position to apply power and to the OFF position to remove power. Power is not controlled by manual operation of the circuit breaker. Note that the circuit breaker must be in the ON position to allow either local or remote control of primary power in the Serial Drum by means of the switch; setting the switch to the REMOTE ON position alone is not sufficient for remote operation.

SECTION 5

PROGRAMMING

INSTRUCTION CODES

The functions performed by IOT pulses in the Serial Drum are listed in Table 3-1. Combining these pulses and adding the skip group yields the instruction list given in Table 5-1.

TABLE 5-1 TYPE 24 SERIAL DRUM INSTRUCTION LIST

Octal Code	Mnemonic Code	Operation
706006	drlcrd	Load the Drum Core Location Counter with the core memory location information in Accumulator bits 2 through 17. Prepare to read one block of information from the drum into the specified core location.*
706046	drlcwr	Load the Drum Core Location Counter with the core memory location information in Accumulator bits 2 through 17. Prepare to write one block of information into the drum from the specified core location.*
706101	drsf	Skip next instruction if the drum transfer done flag is a 1. (The block transfer is complete.)
706102	drcf	Clear the drum transfer done flag and the $DE^0 \cdot PE^0$ error flag.
706106	drlblk	Load the Drum Track Address Register with the contents of Accumulator bits 10 through 17. Clear the drum transfer done flag, clear the $DE^0 \cdot PE^0$ error flag, and begin a transfer (reading or writing).*
706201	drsok	Skip next instruction if the drum transfer done flag is not a 1.
706204	drcont	Clear the drum transfer done flag, clear the $DE^0 \cdot PE^0$ error flag and begin a transfer.

*The Drum Core Location Counter is incremented after each word transfer and the Drum Track Address Register is advanced to the next position at the end of each block transfer if the drum error flag is not set to a 1 and the MAINT ON/OFF switch is in the OFF position.

PROGRAM TIMING

Two instructions cause the transfer of a 256-word block. The first (drlcrd or drlcwr) specifies the core memory location of the block and the direction of transfer (drum-to-core or core-to-drum). The second instruction (drlblk) specifies the block or track number and initiates the transfer. Transfer of each word is performed during a data break, under control of the computer Data Interrupt Control, and is interleaved with the running program.

The timing of a block transfer is shown in Figure 5-1. A transfer begins when the continuously rotating drum reaches the index mark, 3.5 microseconds before the beginning of the data track (word 0, bit 0). A 300-microsecond interval separates the end of a block from its beginning. Because the selection of a read-write head requires 200 microseconds stabilization time, a new track must be specified during the first 100 microseconds of the 300 microsecond interval for continuous transferring. If selected tracks are consecutive, uninterrupted transferring may be programmed merely by specifying continuation, since the block number is automatically incremented at the end of each successful block transfer and core memory location is automatically incremented at the completion of each word transfer. The continuation instruction (drcont) can be given at any time during the 300-microsecond interval.

The drum transfer done flag is set to 1 upon completion of a block transfer, causing a program interrupt. The flag is cleared when a drcf instruction is issued specifically for that purpose, or automatically when either tha drblk or drcont transfer instruction is given. The drum transfer done flag is associated with bit 17 of the computer in-out read status instruction.

The $DE^0 \cdot PE^0$ error flag should be checked at completion of a block transfer. If this flag is a 1 it indicates either of the following conditions:

(a) A parity error has been detected after read-in from drum to core memory. If the MAINT ON/OFF switch is in the OFF position when a parity error occurs, the error flag in the computer is set to 1; if this switch is in the ON position, the error flag is set to 1 and the transfer is terminated.

(b) The data request signal from the drum was not answered by the computer within the 66-microsecond period. The data transmission is terminated and the error flag in the computer is set to 1. This condition occurs either because other devices with higher priority are connected to the computer Data Interrupt

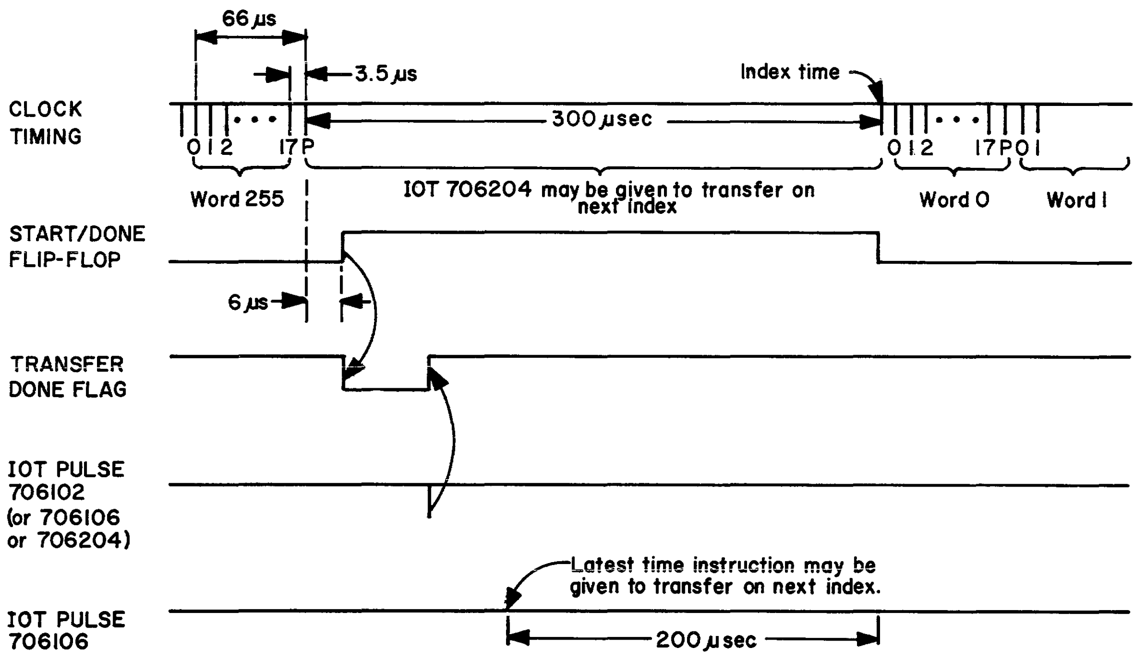


Figure 5-1 Program Timing

Control, or because an instruction requiring longer than 66 microseconds for completion was in progress at the time the data request was made.

The programmer should be aware of the settings of the FIELD LOCKOUT switches to avoid attempting to write at track addresses which are inhibited by switches being in the up position. The octal addresses inhibited by each switch are as follows:

Switch	Addresses	Switch	Addresses
0	0000 to 0017	10	0200 to 0217
1	0020 to 0037	11	0220 to 0237
2	0040 to 0057	12	0240 to 0257
3	0060 to 0077	13	0260 to 0277
4	0100 to 0117	14	0300 to 0317
5	0120 to 0137	15	0320 to 0337
6	0140 to 0157	16	0340 to 0357
7	0160 to 0177	17	0360 to 0377

Note that a Serial Drum containing 16384 words uses only addresses 0000 through 0077, containing 32768 words uses addresses 0000 through 0177, and containing the maximum of 65536 words uses all octal track addresses from 0000 through 0377.

PROGRAM SEQUENCE

The following programs are examples of Serial Drum subroutines for the PDP-4 computer. Example A is a simple routine which allows reading or writing. Example B is a more sophisticated routine in which frequent error checks are made.

Program Sequence Example A

```
/Subroutine to read or write n blocks.
/Core location a, drum block location b.
/Calling sequence:
/                 law a
/                 jms drumrd        /or drumwr
/                 law b
/                 lam -n+1
drumrd,           0                 /read entry
                  drlcrd            /give read command
                  lac drumrd        /setup to use common
                  dac drumwr
                  jmp common
drumwr,           0                 /write entry
                  drlcwr
common,           xct i drumwr      /fetch block number
                  drlblk            /begin first block transfer
                  isz drumwr
                  xct i drumwr      /get number of blocks
                  dac temp
drcon,            drsf              /wait till transfer is done
                  jmp drcon
                  drsok             /check for valid transfer
```

Program Sequence Example A (continued)

```
                        hlt                     /stop if not good
                        isz                     /index block number
                        jmp .+2
                        jmp drdone
                        drcont                  /give continue for more blocks
                        jmp drcon
drdone,                 drcf
                        isz drumwr              /advance return
                        jmp i drumwr
/end of drum read or write subroutine
```

Program Sequence Example B

```
/drum subroutines
/a = initial core memory address, b = initial drum address
/calling sequence:      lac (a)                 /or law (a)
/                       jms drumrd or drumwr
/                       law b                   /or lac (b)
/                       lam -n+1                /n = no. of blocks to write
/                       jmp subr                /return to drsub + 1, for
                                                /multiprogramming
/                       jmp err
drlcrd = 706006
drlcwr = 706046
drlblk = 706106
drcont = 706204
drsf = 706101
drsok = 706201
drcf = 706102
drumwr,                 0
                        drlcwr                  /drum wr
                        dac drumt1
```

Program Sequence Example B (continued)

```
                lac drumwr
                dac drumrd
                jmp drumcm
drumrd,         0
                drlcrd              /drum rd
                dac drumt1
drumcm,         xct i drumrd
                dac drumt2
                drlblk              /start transfer
                isz drumrd
                xct i drumrd        /block counter
                dac drumt3
                isz drumdr
                lac i drumdr
                dac drsub
                isz drumrd          /points to error return
                jmp drsub
drcon,          drcont
                isz drumt2
                lac drumt1
                add decimal (256) octal
                dac drumt1
drsub,          0
                drsf
                jmp .-1
                drsok
                jmp drexit
                isz drumt3
                jmp drcon
                isz drumrd
drexit,         drcf
```

Program Sequence Example B (continued)

```
                    jmp i drumrd
drumt1,             0               /current core address
drumt2,             0               /drum address
drumt3,             0               /counter
start
```

SECTION 6

MAINTENANCE

Maintenance of the Type 24 Serial Drum consists of procedures repeated periodically as preventive maintenance, and tasks performed in the event of equipment malfunction as corrective maintenance. Maintenance activities require use of the equipment listed in Table 6-1, or equivalent, as well as the use of standard hand tools, cleansers, and test cables and probes.

TABLE 6-1 MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Model
Multimeter	Triplett Simpson	630-NA 260
Oscilloscope	Tektronix	540 Series
Variable Power Supply	DEC	734
System Module Extender*	DEC	1954
System Module Puller*	DEC	1960

*One supplied with the equipment

If it is necessary to remove the modules during either preventive or corrective maintenance, the Type 1960 System Module Puller should be used. Turn off all power before extracting or inserting modules. Carefully hook the small flange of the module puller over the center of the module rim, and gently pull the module from the rack. Use a straight even pull to avoid damage to plug connections or twisting of the printed-wiring board. Since the puller does not fasten to the module, grasp the rim of the module to prevent it from falling. Access to controls on the module for use in adjustment, or access to points used in signal tracing can be gained by removing the module, connecting a Type 1954 System Module Extender into the rack, and then inserting the module into the extender.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the equipment and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks will forestall possible future failure by correcting minor damage and discovering progressive deterioration at an early stage. A log book used to record data found during the performance of each preventive maintenance task will indicate the rate of circuit operations deterioration and provide information to determine when components should be replaced to prevent failure of the equipment. These tasks consist of mechanical checks which include cleaning and visual inspections; checks of specific circuit elements such as the power supply, clock timing, sense amplifiers, and magnetic heads; and marginal checks which aggravate border line conditions or intermittent failures so that they can be detected and corrected. All preventive maintenance tasks should be performed every six months or 1,000 equipment operating hours, whichever occurs first.

Mechanical Checks

Assure good mechanical operation of the equipment by performing the following steps and the indicated corrective action for any substandard conditions found:

1. Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in non-flammable solvent.

2. Clean the air filter at the bottom of the cabinet. Remove the filter by removing the fan and housing, which are held in place by two knurled and slotted captive screws. Wash the filter in soapy water, dry in an oven or by spraying with compressed gas, and spray with Filter-Kote (Research Products Corporation, Madison, Wisconsin).

3. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

4. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC blue enamel number 3277-1S65 or DEC gray enamel number 3277-1R44.

5. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring.

6. Inspect the following for security: switches, knobs, jacks, connectors, transformers, fan, capacitors, lamp assemblies, etc. Tighten or replace as required.

7. Inspect all racks of logic to assure that each module is securely seated in its connector.

8. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors giving these signs of malfunction.

Power Supply Checks

Check the output voltage and ripple content of the Type 728 Power Supply, and assure that it is within tolerance. Use multimeter to make the output voltage measurements without disconnecting the load. Use the oscilloscope to measure the peak-to-peak ripple content on dc outputs of the supplies. These supplies are not adjustable, so if the output voltage or ripple content is not within the tolerance specified, the supply is considered defective and troubleshooting procedures should be undertaken.

Check the +10 volt output between the black (-) and red (+) terminals to assure that it is between 9.5 and 11.0 volts with less than 800 millivolts ripple. Check the -15 volt output to assure that it is between 14.5 and 16.0 volts with less than 400 millivolts ripple.

Timing Checks

Using the oscilloscope and referring to engineering drawing D-24603, check the timing of the Type 4410 Variable Clock at location C13, the Type 4303 Integrating Single Shot at location C09, and the Type 1304 Delay at location D24. If necessary the timing of these modules can be adjusted by turning the potentiometer screw which is accessible through a hole in the handle.

Check the timing at the variable clock to assure that standard DEC pulses occur at terminal C13F every 2 to 4 microseconds when the module is uninhibited. The clock can be made free-running for this check by disconnecting the wire from the green Heyman Tab Terminal at the top of the Type 813 Power Control. Be sure to restore this connection at the completion of this check or subsequent data transfers may be invalid.

Check the single shot by observing the ONE output at C09W while triggering the oscilloscope on C09K. During each revolution of the drum the single shot is triggered every 3.5 microseconds for approximately 17 milliseconds (4865 pulses x 3.5 μsec) during data reading and receives no pulses during the 300-microsecond gap. The output at terminal C09W should be at ground level during the gap, drop to -3 volts at the first triggering pulse, and remain at -3 volts for 6 microseconds after the last triggering pulse is received before reverting to ground potential.

Check the timing of the delay module by observing the negative Read Strobe pulse at terminal D24E while triggering the oscilloscope on the $\emptyset_A$ pulse at D24Y. Read Strobe pulses should succeed $\emptyset_A$ pulses by approximately 0.8 microseconds. Observe the Read Strobe pulses and the amplified output of a magnetic head by connecting the second input of the dual-trace oscilloscope to terminal E24S. It is more important that the Read Strobe pulses occur at the negative peak of the sinusoidal signal read from the drum than that they occur 0.8 microseconds after the $\emptyset_A$ pulses. Measurements should be made with several different heads selected and the Read Strobe pulse should be adjusted for an average of the measurements to eliminate large differences in peak playback time.

Drum Sense Amplifier Checks

The Type 1537 Drum Sense Amplifier modules at locations E25 (clock track) and E24 (data track) are checked for proper slice or threshold level at terminal S. This measurement can be made with the oscilloscope by measuring the amount the base line shifts above ground when the signal is connected to the input. The clock track sense amplifier slice level should be -100 millivolts. The data tracks sense amplifier slice level should be -150 millivolts. Adjustment of the slice level can be achieved by turning the potentiometer screw which is accessible through a hole in the module handle.

Drum Clock Head Spacing Checks

Check the spacing of the clock track head by measuring the preamplifier output of the Drum Sense Amplifier at terminal E25S. This output should be approximately one volt peak-to-peak, as measured on an oscilloscope. Adjustment of the head should be undertaken only if the preamplifier output is less than 750 millivolts, if the head has been replaced, or when operational tests clearly indicate that it is required.

Clock heads are mounted in a "T" saddle attached to a mounting block on the shroud. This assembly is shown in Figure 6-1. The distance between the pickup end of the head and the surface of the drum can be adjusted by means of the differential screw. Turning this screw 360 degrees causes the mounting block to move 0.006 inch at the screw, resulting in approximately 0.003 inch travel of the head. Therefore approximately 9 degrees of differential screw rotation moves the head 75 microinches. A safety shim prevents the head from being drawn down against the drum surface by rotation of the differential screw, providing that the drum is at thermal equilibrium and the head and shim have been properly installed. The clock head mounts also have provision for slight horizontal adjustment to allow accurate timing coincidence on the bits recorded on the drum surface. This adjustment is effected by turning the puller or pusher screws in a "T" saddle which is set into the mounting block. Since the Series Drum requires only one clock head this feature of the drum memory is not utilized and so need not be adjusted.

To locate the clock head which is being used trace the wiring from module E25 to connector J1. As shipped from DEC the module is connected to terminals J1-18 through J1-21, signifying use of clock head C4. Clock head C3 is connected to J1-26 through J1-29, C2 to J1-35 through J1-38, and C1 to J1-43 through J1-46.

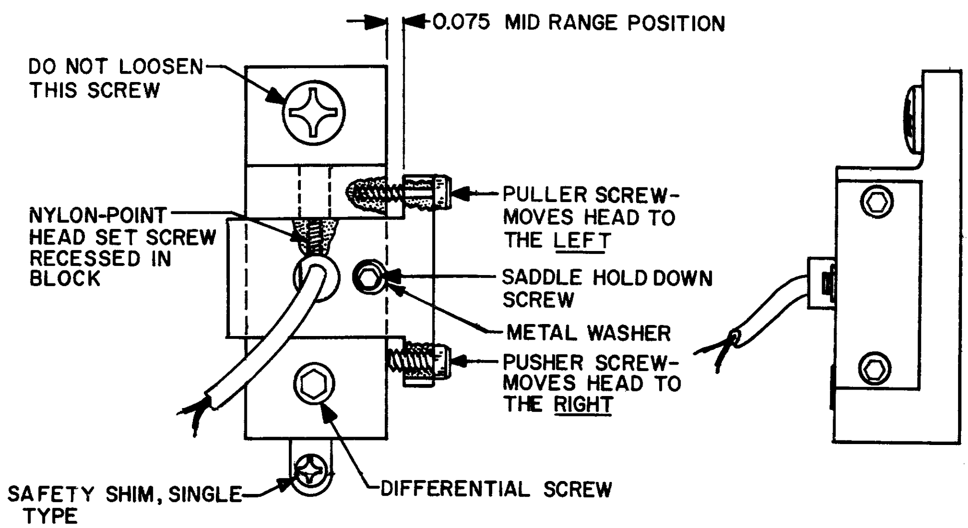


Figure 6-1 Drum Clock Head Assembly

CAUTIONS

1. A short circuit between any of the three clock heads leads and ground destroys the information recorded on the clock track. Do not remove the tape from the connector terminals of the spare clock heads and never check continuity of the clock head with a multimeter.

2. The drum must remain at the thermal equilibrium when the covers are removed from the housing. Before commencing head adjustment procedures, check the immediate area to assure that no drafts or other causes of temperature transients will occur during the procedure.

3. When the covers of the drum are removed use extreme care to maintain the clean condition of the drum. Do not permit dust, smoke, or other foreign matter to enter the drum housing.

To adjust the head:

1. Connect the oscilloscope to module location E25S to observe the preamplifier output.

2. Ascertain the location of the head to be adjusted by tracing the wiring from module E25 to connector J1 and by referring to engineering drawing D-24619. In this manner the covers on the drum housing can be removed for a minimum time.

3. If necessary, remove the end panels from the cabinet by lifting them above the hooks on the frame. Remove the cover from the drum housing adjacent to head to be adjusted by turning the six captive screws.

4. Turn the differential screw to obtain a one-volt peak-to-peak signal on the oscilloscope. No other screws should be turned to adjust the output amplitude.

5. Replace the drum housing cover and the panels, if removed.

Drum Data Head Spacing Checks

Check the spacing of each data head by measuring the output of the Drum Sense Amplifier at terminal E24S, with the head selected by the Drum Track Address Register, and with the machine in the read status. The best method of making this check is to run a program in which patterns of all ZEROs, all ONEs or alternate ONEs and ZEROs are written on the selected track, then continuously read the data and monitor the output on an oscilloscope. Patterns of all ONEs or all ZEROs should produce an output of one volt peak-to-peak and patterns of alternate bits should produce an output of two volts peak-to-peak. If test data patterns are to be written during this check, and if the data on the drum is to be retained it should be read into the computer core memory, the check of a head performed, and the data rewritten on the drum for each track. If the check is to be performed without the use of the computer, test data patterns should not be produced manually if the data recorded on the drum must be retained. Data, track address, and read/write status can be set into the machine without use of the computer by manually grounding appropriate flip-flop terminals in the Drum Final Buffer, Drum Track

Address Register, and Drum Data Channel. Adjustment of the head should be undertaken only if the preamplifier output differs substantially from the one and the two volt limits as stated previously, if the head has been replaced, or when operational tests clearly indicate that it is required.

Data heads are set into a mounting block which is permanently attached to the shroud. This assembly is shown in Figure 6-2. The distance between the pickup end of the head and the surface of the drum can be adjusted by means of the differential screw. Turning this screw 360 degrees causes the mounting block to move 0.006 inch at the screw, resulting in approximately 0.003 inch travel of the head. Therefore approximately 9 degrees of differential screw rotation moves the head 75 microinches. A safety shim prevents the head from being drawn down against the drum surface by rotation of the differential screw, providing that the drum is at thermal equilibrium and the head and shim have been properly installed. One such shim is used for two head mounts, one above the other, so that replacement of either head requires adjustment of the other.

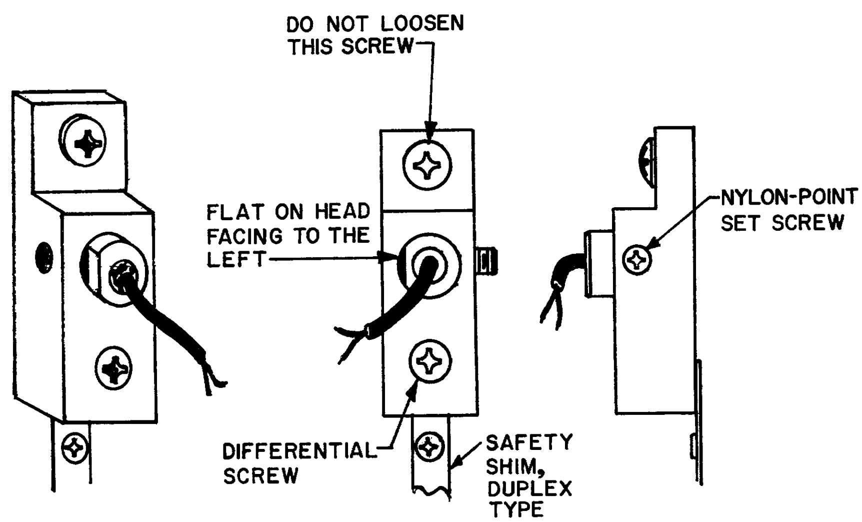


Figure 6-2 Drum Data Head Assembly

CAUTIONS

1. The drum must remain at thermal equilibrium when the covers are removed from the housing. Before commencing head adjustment procedures, check the immediate area to assure that no drafts or other causes of temperature transients will occur during the procedure.

2. When the covers of the drum are removed use extreme care to maintain the clean condition of the drum. Do not permit dust, smoke, or other foreigh matter to enter the drum housing.

To adjust the head:

1. Connect the oscilloscope to module location E24S to observe the preamplifier output.

2. Ascertain the location of the head to be adjusted by referring to engineering drawing D-24619. This drawing indicates the diode matrix board location for each head by X-Y address coordinates. From the matrix board location the wiring can be traced to a head. The heads are also located on the drum shroud address coordinates, X being horizontal and Y being the vertical axis. In this manner the covers on the drum housing can be removed for a minimum of time.

3. If necessary remove the end panels from the cabinet by lifting them above the hooks on the frame. Remove the cover from the drum housing adjacent to head to be adjusted by turning the six captive screws.

4. Turn the differential screw to obtain the correct peak-to-peak output signal on the oscilloscope for the data pattern being read. When adjusting, turn the differential screws to increase or decrease the signal by approximately 50% of the desired correction factor, then rewrite and read the data again. Repeat this step until a proper output is achieved. Do not turn any screws except the differential screws to adjust the output amplitude.

5. Repeat step 4 for each track to be adjusted.

6. Replace the drum housing cover and the end panels, if removed.

Marginal Checks

Marginal checks are performed to aggravate borderline conditions within the logic to reveal observable faults. Therefore, these conditions can be corrected during scheduled preventive maintenance to forestall possible future equipment failure. These checks can also be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors. The checks are performed by operating the equipment logic circuits from an external, adjustable power source, such as the DEC Type 734 Variable Power Supply. The Marginal Check Panel of the PDP-4 has facilities for providing this power to the Serial Drum. Raising the bias voltage above +10 is equivalent to lowering the amount of base drive on a particular transistor. This in turn simulates a lower gain driving transistor. Raising the bias voltage thus tends to indicate low gain transistors. Lowering the bias voltage below +10 volts simulates a condition where the voltage drop across the previous driving transistor (V_{CE}) has increased, thus tends to indicate high V_{CE} drop (leakage) transistors or low gain driving transistors. The -15 volt supply margins are not checked in the Series Drum because raising or lowering the -15 volts does not affect the majority of control logic, since it is the collector load voltage and is usually clamped to -3 volts. The +10 volt margin should be about ±5 volts. By recording the level of bias voltage at which circuits fail, progressive deterioration can be plotted and expected failure dates predicted. Therefore, these checks provide a means of planned replacement.

Marginal checks of the +10 (A) supply (top switch of the left of the rack) to rack E varies the slice level on the drum sense amplifier modules and so is a valuable tool in verifying the capability of the machine to read and write on the drum surface. Normally increasing the +10 (A) supply by 3 or 4 volts also increases the slice level and causes bits to be dropped out (i.e. 1s to become 0s). Decreasing the +10 (A) source by 3 or 4 volts usually lowers the slice level and causes bits to be picked up (i.e. 0s to become 1s).

Refer to the Power Supply and Distribution discussion in Section 2 for an explanation of the connection of the color-coded connector at the right side of each rack of modules and for the function of the marginal-check switches at the end of each rack.

To perform the checks:

1. Supply the marginal check voltage to the Serial Drum from the PDP-4 Marginal Check Panel or connect the external marginal-check power supply to the colored connector on any rack between the green (+) and the black (ground) terminal.

2. Energize the marginal-check power supply and adjust the outputs to supply the nominal +10 vdc.

3. Start equipment operation in a repetitive program or in a routine which fully utilizes the circuits in the rack to be tested. The diagnostic program described in the System Troubleshooting procedure is excellent for this check.

4. Set the top switch on the rack to be checked to the up position.

5. Lower the +10 volt marginal-check power supply until normal system operation is interrupted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced, if desired.

6. Start equipment operation. Then decrease the +10 volt marginal-check supply until normal operation is interrupted, at which point record the marginal-check voltage. Transistors can again be located and replaced.

7. Return the top switch to the down position.

8. Repeat steps 2 through 7 for the center switch on the logic rack being checked.

9. Repeat steps 2 through 8 for each rack or logic to be checked.

10. De-energize and/or disconnect the external marginal-check power supply.

CORRECTIVE MAINTENANCE

The equipment is constructed of highly reliable transistorized modules. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment down time due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. No special tools or test equipment are required for corrective maintenance other than a broad bandwidth oscilloscope and a standard multimeter. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept and the operation of specific circuits as described in Section 2, program techniques described in Section 5, the engineering drawings presented in Section 7, and the location of mechanical and electrical components.

Diagnosis and remedial action for a fault condition is performed in the following phases:

a. Preliminary investigation to gather all information and to determine the physical and electrical security of the system.

b. System troubleshooting to locate the fault to within a module through the use of diagnostic programming, signal tracing, or aggravation techniques.

c. Circuit troubleshooting to locate defective parts within a module.

d. Repairs to replace or correct the cause of the malfunction.

e. Validation tests to assure that the fault has been corrected.

f. Log entry to record pertinent data.

Preliminary Investigation

It is virtually impossible to outline any specific procedures for locating faults within complex digital systems such as the Serial Drum. Before commencing troubleshooting procedures, explore every possible source of information. Ascertain all possible information concerning any unusual function of the machine prior to the fault and all possible program information such as routine in progress, condition of control panel indicators, etc. Search the maintenance log to determine if this type of fault has occurred before or if there is any cyclec history of this kind of fault, and determine how this condition was previously corrected. When the entire machine fails, perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Assure that the power supply is working properly and that there are no power short circuits, by performing the power supply checks as described under Preventive Maintenance.

System Troubleshooting

Do not attempt to troubleshoot the drum system without first gathering all information possible concerning the fault, as outlined in the Preliminary Investigation.

Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings. Careful checks should be made to assure that either the Series Drum is actually at fault before continuing with corrective maintenance procedures. Faults in equipment transmitting or receiving information or improper connections of the system frequently give indications very similar to those caused by drum malfunction. From that portion of the program being performed and the general condition of the indicators, the logical section of the machine at fault can usually be determined.

If the fault has been determined to be within the Type 24 Serial Drum but cannot be localized to a specific logic function, perform the diagnostic program procedure. When the location of a fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent a form of aggravation test should be employed to locate the source of the fault.

Diagnostic Program - This test procedure is designed to check the basic control functions performed by the machine and to determine the reliability of recording on various tracks. Specifically the program performs the following:

a. Writing and checking of any desired pattern on the entire drum, writing one track at a time.

b. Writing and checking of specific patterns on the entire drum, writing one track at a time.

c. Writing and checking of randon numbers over the entire drum, writing four tracks at a time.

Prepare a perforated tape or other vehicle for loading the following program into the computer.

```
24/
wra = 2000
rda = 4000
begin,          lac dlngth
                cma
                add (1)
                dac dloop1+3
                dac dwrite+1
                add (3)
                dac d3a
d0,             las
                sma
                jmp d1
                hlt
```

```
                las
                jms dloop1
                jmp d0
d1,             lam tb-tbe
                dac t2
                law tb-1
                dac 17
d2,             lac i 17
                jms dloop1
                isz t2
                jmp d2
d3              lac (736425)      /test random 2000 wd patterns
                dac rnk
                lac (nop)
                dac drsub+4
d3a,            lam               /modified, -dlngth+4
                dac t1
                dzm dk1
d4,             lam -1777
                dac t2
                law wra-1
                dac 10
d5,             jms rn
                dac i 10
                isz t2
                jmp d5
d6,             lac (wra)
                jms drumwr
                lac dk1
                lam -3
                jmp drsub+1
                jmp wze
```

```
d7,     jms dcmp
        lam -3
        lam -1777
        isz dk1
        isz t1
        jmp d4
        jmp d3a
dcmp,   0               /compare read area against write area
        lac (rda)
        jms drumrd
        lac dk1
        xct i dcmp
        jmp drsub+1
        jmp .+1
        isz dcmp
        xct i dcmp
        dac dct1
        lac (lac wra-1)
        dac 10
        lac (lac rda-1)
        dac 11
dcmp2,  lac i 10
        sad i 11
        jmp .+2
        jms dcmpe
        isz dct1
        jmp dcmp2
        isz dcmp
        jmp i dcmp
dct1,   0
dk1,    0
dk2,    0
```

```
dk3,        0
dcmpe,      0                       /type out drum error
            tin
            lac dk1
            dac dk2                 /channel no.
            lac (lac rda)
            cma
            add 11
dcmpe1,     add (decimal -255 octal)
            spa
            jmp dcmpe2
            add (-1)
            isz dk2
            jmp dcmpe1
dcmpe2,     add (decimal 255 octal)
            spa
            cma
            dac dk3                 /word no.
            lac dk2                 /track number
            twordz
            6
            tab
            lac dk3                 /word number
            twordz
            6
            tab
            xct 10                  /word written
            tword
            6
            tsp
            xct 11                  /word read
            tword
```

```
                6
                jmp i dcmpe
dloop1,         0                   /do writing and checking
                jms dsprd
                jms dwrite
                lam                 /modified, -dlength+1
                dac t1
                dzm wra
                dzm dk1
dloop2,         jms dcmp
                lam
                lam decimal -255 octal
                isz dk1
                isz wra
                isz t1
                jmp dloop2
                jmp i dloop1
t1,             0
t2,             0
dsprd,          0                   /spreads 256 words in wra
                dac dsprda
                lam decimal -255 octal
                dac dsprdc
                law wra-1
                dac 10
                lac dsprda
                dac i 10
                isz dsprdc
                jmp .-2
                dzm wra
                dzm dk1
                jmp i dsprd
```

```
dsprdc,     0
dsprda,     0                   /writes all channels
dwrite,     0
            lam                 /modified, -dlngth+1
            dac dwc
            lac (jmp drexit)
            dac drsub+4
dw1,        lac (wra)
            jms drumwr
            lac dk1
            lam
            jmp drsub+1
            jms wze
            isz wra
            isz dk1
            isz dwc
            jmp dw1
            jmp i dwrite
dwc,        0
rn,         0                   /random number generator
            lac rnk
            cllVrar
            szl
            xor (400000)
            xor (335671)
            add (335671)
            dac rnk
            jmp i rn
rnk,        0                   /working number
wze,        0
            tin
            lac dk1
```

```
                    twordz
                    6
                    tsp
                    lac (flex wre)
                    ty3
                    jmp i wze
tb,                 0
                    777777
                    525252
                    252525
                    666666
tbe,                111111
dlngth,             400             /256 tracks decimal
start
```

This program assumes that DEC Read-In Mode Loader program and standard teleprinter subroutines are stored in core memory. If the subroutines are not in the computer prepare routines as listed in Appendix A1, or equivalent, and load them into the computer.

To use this program set the ADDRESS switches to 7770, load the tape in the reader, and depress the START key. When the program is in the computer press the STOP key, set the ADDRESS switches to 24, then press the START key.

a. If bit 0 of the ACCUMULATOR switches is a 1 the program will halt. Put the pattern desired to be written on the drum in the ACCUMULATOR switches and press CONTINUE. The pattern will be written on all tracks and checked. Note that during this phase and during phase b below, the first word written on each track is the track number.

After the entire drum (tracks $0\text{-}127_{10}$ or $0\text{-}255_{10}$) have been checked, the program will continue with phase b unless bit 0 of the ACCUMULATOR switches is a 1, in which case the machine will halt again and the entire process can be repeated. The switches can be changed any time after CONTINUE is pressed.

If bit 0 of the ACCUMULATOR switches is a 0 when starting the program phase b will begin immediately.

b. During this phase the following patterns are written and checked over the entire drum, writing one track at a time:

000000

777777

525252

666666

111111

(The first word on each track will be the track number)

c. When phase b is completed the program will generate pseudo-random numbers and write and check the entire drum writing and reading, four tracks at a time (i.e. 0-3, 1-4, 2-5, 3-6 etc. through $124-127_{10}$ or $252-255_{10}$). This phase will continue indefinitely until the machine is stopped.

If information is misread from the drum, the following typical message will be typed, and the program will continue checking the next channel:

000100	000236	525252	525250

Where: word one = the track number (octal 0-255)

word two = word number (octal 0-377)

word three = the word written on the drum

word four = the word read from the drum (in this example bit 16 was dropped)

If an error occurs during writing, the message 000100 WRE will be typed, indicating a write error on track 100 (octal). The program will continue, however, if this error occurs during phace c, start the program over manually. Normally this error cannot occur, as parity is not checked during writing, and no timing problems are imposed by the programming.

The program has been assembled for a 256_{10} track drum. To use the same program for a 128_{10} track drum, change register DLNGTH to 200_8.

Signal Tracing - If the fault has been located within a functional logic element, program the equipment to repeat some operation in which all functions of that element are utilized. Use the oscilloscope to trace a signal flow through the suspect logic element. Oscilloscope sweep may be synchronized by control signals or clock pulses available at individual module terminals. Trace the signal from the output back to its origin. The signal tracing method determines with absolute certainty the quality of pulse amplitude, duration, and rise time and the correct timing sequence. In the event an intermittent malfunction occurs, signal tracing must be combined with an appropriate form of aggravation test.

Aggravation Tests - Intermittent faults should be traced through the use of aggravation techniques. Intermittent logic malfunctions are located by the performance of marginal-check procedures as described under Preventive Maintenance. Intermittent failures caused by poor wiring connections can often be revealed by vibrating the modules while running a repetitive test cycle. Often, wiping the handle of a screw-driver across the back of a suspect row of modules is a useful technique. By repeatedly starting the equipment and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector, check the module connector for wear or misalignment, and check the module wiring for cold solder joints or wiring kinks.

Circuit Troubleshooting

The procedure followed for troubleshooting and correcting the cause of faults within specific circuits depends upon the down time limitations of equipment use. Where down time must be kept at a minimum it is suggested that a provisioning parts program be adopted to maintain one spare module or standard component which can be inserted into the cabinet when systems troubleshooting procedures have located the fault to a particular component. Bench troubleshooting procedures can be performed to correct the defective components. Where down time is not as critical, the spare parts list can be reduced and signal tracing techniques can be utilized to troubleshoot modules within the equipment. This practice involves module removal by means of a Type 1960 System Module Puller, insertion of a Type 1954 System Module Extender into the logic rack, insertion of the suspect module in the module extender, and oscilloscope signal tracing of the module with the equipment energized and operating.

Static and dynamic circuit troubleshooting procedures may be performed at a bench. Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble, or confirm a fault condition observed, use the multimeter to measure resistances.

CAUTIONS

1. Do not use the lowest or highest resistance ranges of the multimeter when checking semi-conductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

2. Do not attempt to measure resistance of any clock head. The voltage applied to the test probes is sufficient to erase information from the drum surface and possibly cause damage to the head and the selection circuits.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same, and no parallel paths exist, replace the diodes.

Measure the emitter-collector and emitter-base resistance of transistors. Most catastrophic failures are due to short circuits between the collector and the emitter or due to an open circuit in the base-emitter path. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and the base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse directions. To determine forward and reverse directions a transistor can be considered as two diodes connected back-to-back. In this analogy PNP transistors are considered to have both cathodes connected together to form the base and both the emitter and collector assume the function of an anode. In NPN transistors the base is assumed to be common-anode connection and both the emitter and collector are assumed to be cathode. Multimeter polarity must be checked before measuring resistances, since many meters (including the Triplett 630) apply a positive voltage to the common lead when in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. More reliable indication of diode or transistor malfunction is obtained through the use of one of the many inexpensive in-circuit testers commercially available.

Damage or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at the wires or components around the connection, or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by intermittent connections. Current interruptions of very short duration, caused by an intermittent connection, can be detected by connecting a 1.5-volt flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope while probing the connection.

Dynamic bench testing of modules can be performed through the use of special equipment. A Type 922 Test Power Cable and either a Type 722 or Type 756 power supply can be used to energize a systems module. These supplies provide both the +10 vdc and -15 vdc operating supply for the module as well as ground and -3 volt sources which may be used as signal inputs. The signal inputs can be connected to any terminal normally supplied by logic level by means of eyelets provided on a Jones plug on the power cable. Type 911 Patch Cords may be used to make these connections on the Jones plug. In this manner logic operations and voltage measurements can be made. When using the Type 765 Bench Power Supply, marginal checks of an individual module can also be obtained.

Repair

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placement of excessive solder or flux on adjacent parts or service lines. When soldering semi-conductor devices (transistors, crystal diodes, and metallic rectifiers) which may be damaged by heat, the following special precautions should be taken:

a. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

b. Use a 6-volt soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

c. Perform the soldering operation in the shortest possible time, to prevent damage to the component and delamination of the module etched wiring.

When any part of the equipment is removed for repair and replacement make sure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals.

Replace defective components only with parts of equal or greater quality and tolerance.

The following procedure should be followed in the removal and replacement of a drum head:

CAUTIONS

1. With the system energized, a short circuit between any of the three clock head leads and ground erases the information recorded on the clock track of the drum surface. A short circuit between any of the three data head leads and ground causes either an open circuit in the head winding or destroys the Type 4522 module which selects the head. Similar faults are caused by attempting to check the continuity of head wiring with a multimeter. Use extreme caution to prevent accidental contact between leads, directly or through a screwdriver or soldering iron at connectors.

2. When soldering head leads use only a tool which is well isolated and grounded. Most electronic soldering irons produce a potential (in the millivolt range) at the tip which would be destructive to the magnetic heads.

3. The drum must remain at thermal equilibrium when the covers are removed from the housing. Before the covers are removed, check the immediate area to assure that no drafts or other causes of temperature transient will occur during the replacement and adjustment procedure.

4. When the covers are removed from the drum housing, use extreme care to maintain the clean condition of the drum. Do not permit dust, smoke, or other foreign matter to enter the drum housing.

1. Ascertain the physical location of the head to be replaced. Refer to engineering drawing D-24619 for the location of the head on the shroud. Visually trace the wiring from the Drum Sense Amplifier module (E24 for data heads, and E25 for clock heads) to terminals of J1 and J2. By becoming familiar with these connections the replacement and adjustment can be performed in a minimum of time.

2. Set the circuit breakers on the power control panel to the OFF position.

3. If necessary, remove the end panels from the cabinet by lifting them above the frame support on which they are hung. Remove the appropriate cover from the drum housing by turning the six captive screws.

4. Turn the differential screw several turns counterclockwise to back the mounting block away from the shroud. Refer to Figures 6-1 and 6-2 for the name and location of parts.

5. Loosen the nylon-point set screw which holds the head in the mounting block and withdraw the head from the block.

6. Loosen the screw holding the safety shim, turn the shim 90 degrees (horizontally) so that it is not under the mounting block, then tighten the screw to hold the shim in this position temporarily.

7. Turn the differential screw clockwise to draw the mounting block firmly against the shroud.

8. Insert the new head into the mounting block so that it is in static contact with the drum surface and making sure that the flat surface is horizontal on the left side. Assure that the head is making contact with the drum surface by applying a slight amount of pressure to the drum surface with one finger. If the drum does not move, indicating drum-to-head contact, maintain the finger pressure and tighten the nylon-point set screw to hold the head in position.

9. Turn the differential screw several revolutions counterclockwise to raise the mounting block away from the shroud.

10. Loosen the set screw holding the safety shim, turn the shim 90 degrees to the vertical position so that it is under the mounting block(s), then permanently tighten the set screw.

11. Turn the differential screw clockwise until a slight resistance is noted, indicating that the mounting block has made contact with the safety shim. Then turn the differential screw approximately 120 degrees counterclockwise.

12. Disconnect the defective head from the printed-wiring board or connector, and connect the leads of the replacement head.

13. When replacing a clock head, loosen the saddle hold-down screw, and adjust the pusher and puller screws so that the "T" saddle is parallel with and 0.075 inch away from the right side of the mounting block. This adjustment can be made very coarsely since this feature of the clock head mount is not used.

14. Set the circuit breakers on the power control panel to the ON position.

15. Proceed to the Preventive Maintenance portion of this section and adjust the head as instructed under the appropriate drum head spacing check.

Validation Test

Following the replacement of any electrical component of the equipment, a test should be performed to assure the correction of the fault condition and to make any adjustments of timing or signal levels caused by the replacement. This test should be taken from the Preventive Maintenance procedure most applicable to the portion of the system in which the error was found. For example, if a filter capacitor was replaced in the power supply the ripple check for that power supply should be repeated as specified under Power Supply Checks. If repairs or replacement are made in an area which is not checked during preventive maintenance, the diagnostic program should be run or an appropriate operational test should be devised. For example, if a flip-flop is repaired or replaced the register on control function performed by the flip-flop should be checked in entirely by manually setting and clearing, by programmed exercise of the function, or by repeating the diagnostic program.

Log Entry

Corrective maintenance activities are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments which would be helpful in maintaining the equipment in the future.

SECTION 7

ENGINEERING DRAWINGS

Engineering drawings in the following list apply to the Type 24 Serial Drum and are supplied in a separately bound schematic book. The logic drawings are included in this manual as an aid to understanding and troubleshooting the system. Should any discrepancy exist between the drawings in this manual and in the schematic book, the schematic book is assumed to be correct.

POWER SUPPLY AND CONTROL

Power Supply	RS-728
Power Control	RS-813

MODULES

Delay	RS-1304
Drum Sense Amplifier	RS-1537
Inverters	RS-4102
Diode Unit	RS-4110
Diode	RS-4112
Diode	RS-4113
Diode	RS-4115
Capacitor-Diode Gates	RS-4127
Quadruple Flip-Flop	RS-4216
Four-Bit Counter	RS-4217
Delay	RS-4301
Integrating Single Shot	RS-4303
Variable Clock	RS-4401
Pulse Generator	RS-4410
Drum NRZ Writer	RS-4518
Drum X Select	RS-4521
Drum Y Select	RS-4522

MODULES (continued)

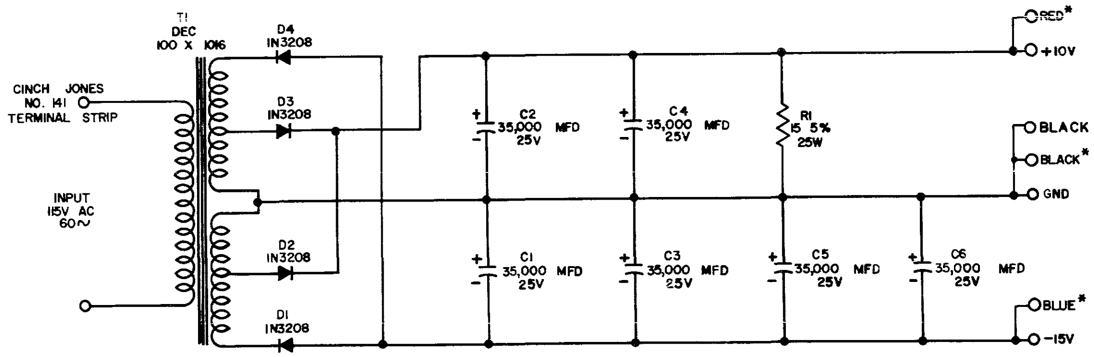
Pulse Amplifier	RS-4604
Pulse Amplifier	RS-4606

LOGIC

DSB, Control & Parity	D-24602
Drum Control	D-24603
Drum Core Location Counter	D-24604
Drum Data Channel	D-24605
Drum Final Buffer & Data Channel	D-24606
Drum Track Address Register & Decoding (X & Y)	D-24607
Drum X & Y Select and Drum Heads	E-24608
Flow Diagram	D-24611
Timing Diagram	C-24612

MISCELLANEOUS

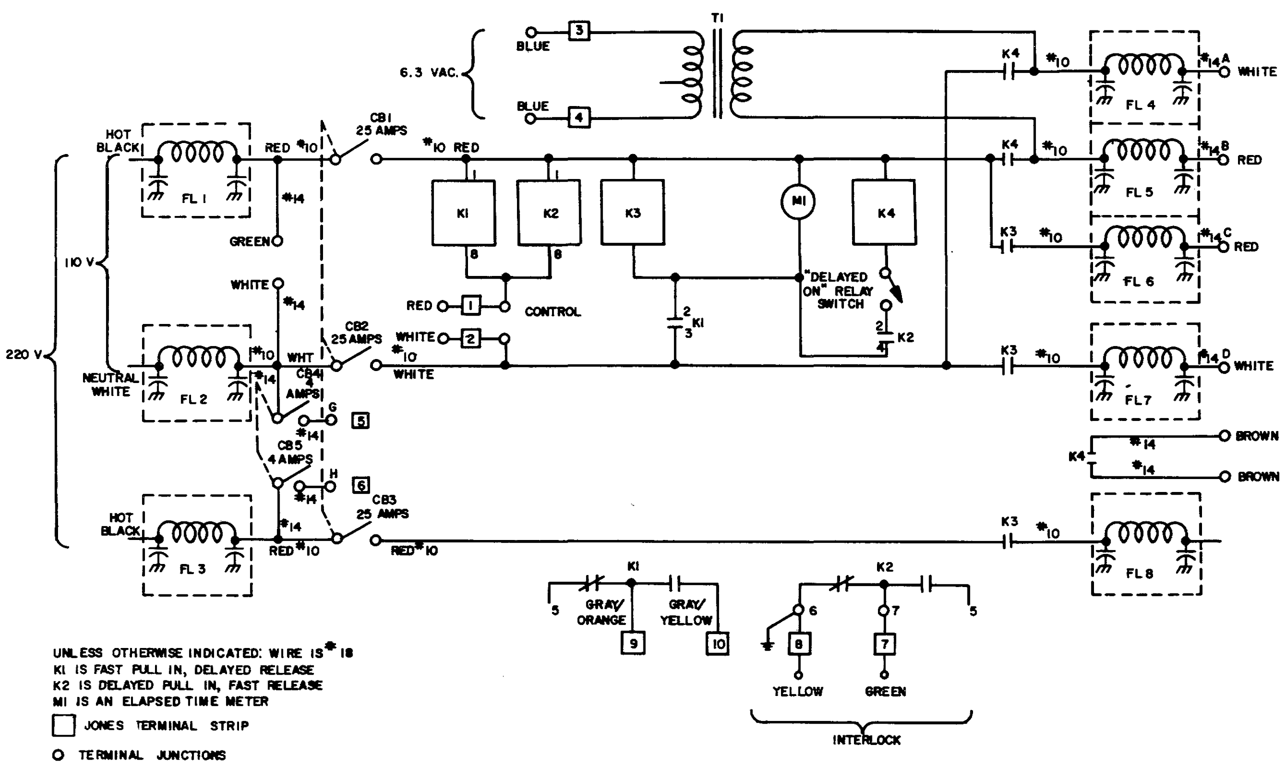
Terminal Designation Layout	E-10208
Utilization Module List	D-24601
Wiring Diagram (Logic) (2 sheets)	D-24609
Wiring Schedule (Drum)	D-24619
Indicator Cable Breakout	D-24613
Wire Run List (Cable connectors to Logic) (5 sheets)	A-24614
Wire Run List (Logic to Indicator Panel) (5 sheets)	A-24617



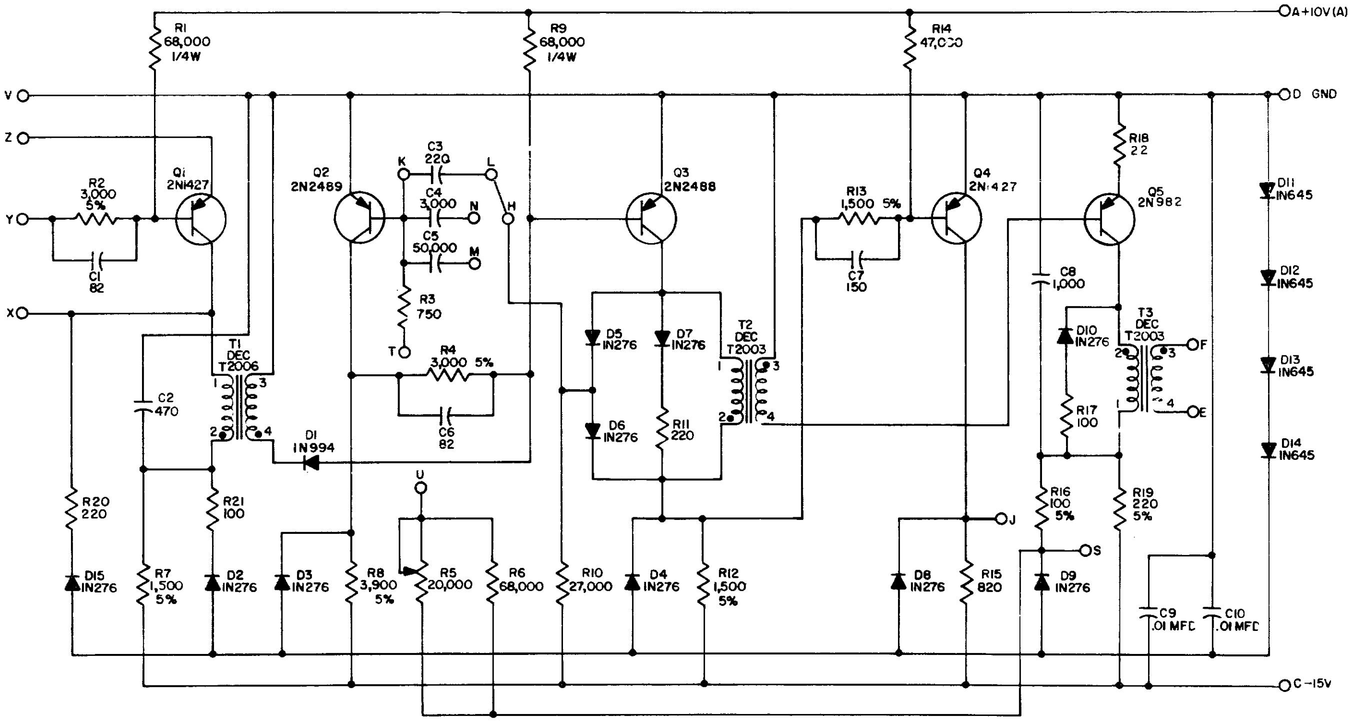
* HEYMAN MFG. CO.
TAB TERMINALS

NOTE
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:
BOTH SIDES LOADED: +10V .0 TO 7.0 AMPS; -15V 1.0 TO 8.0 AMPS
ONE SIDE LOADED: +10V .0 TO 7.5 AMPS; -15V 1.0 TO 8.5 AMPS
SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE FOLLOWING EQUATION $5I_{10} + 6I_{15} \leq 53$

Power Supply 728



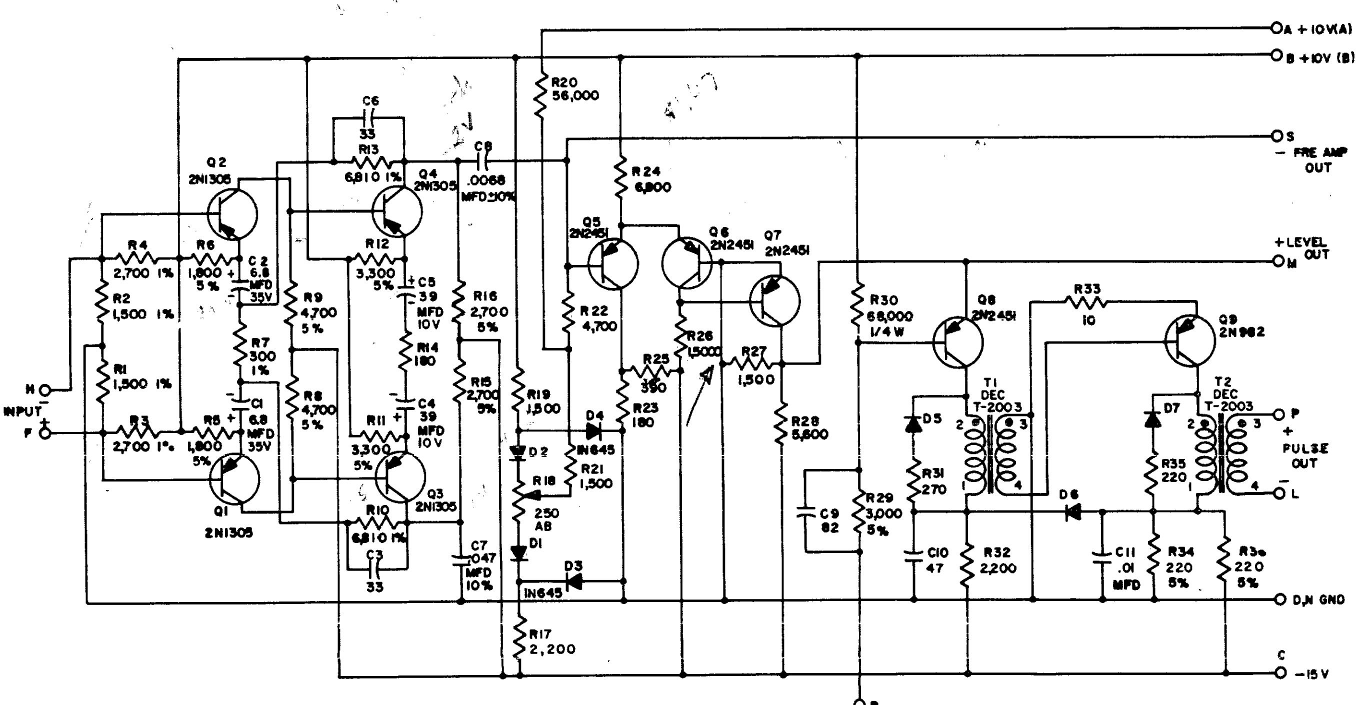
Power Control 813



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD.

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

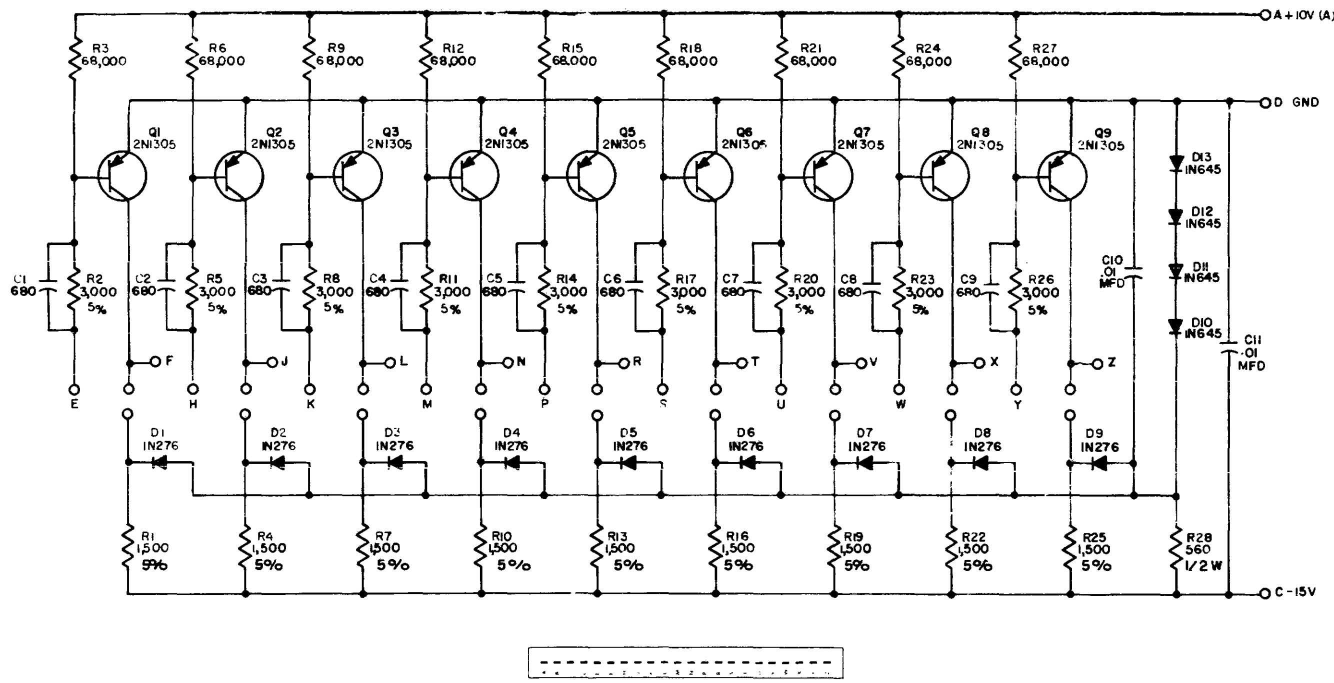
Delay 1304



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4W, 10%
CAPACITORS ARE MMFD
DIODES ARE IN276

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

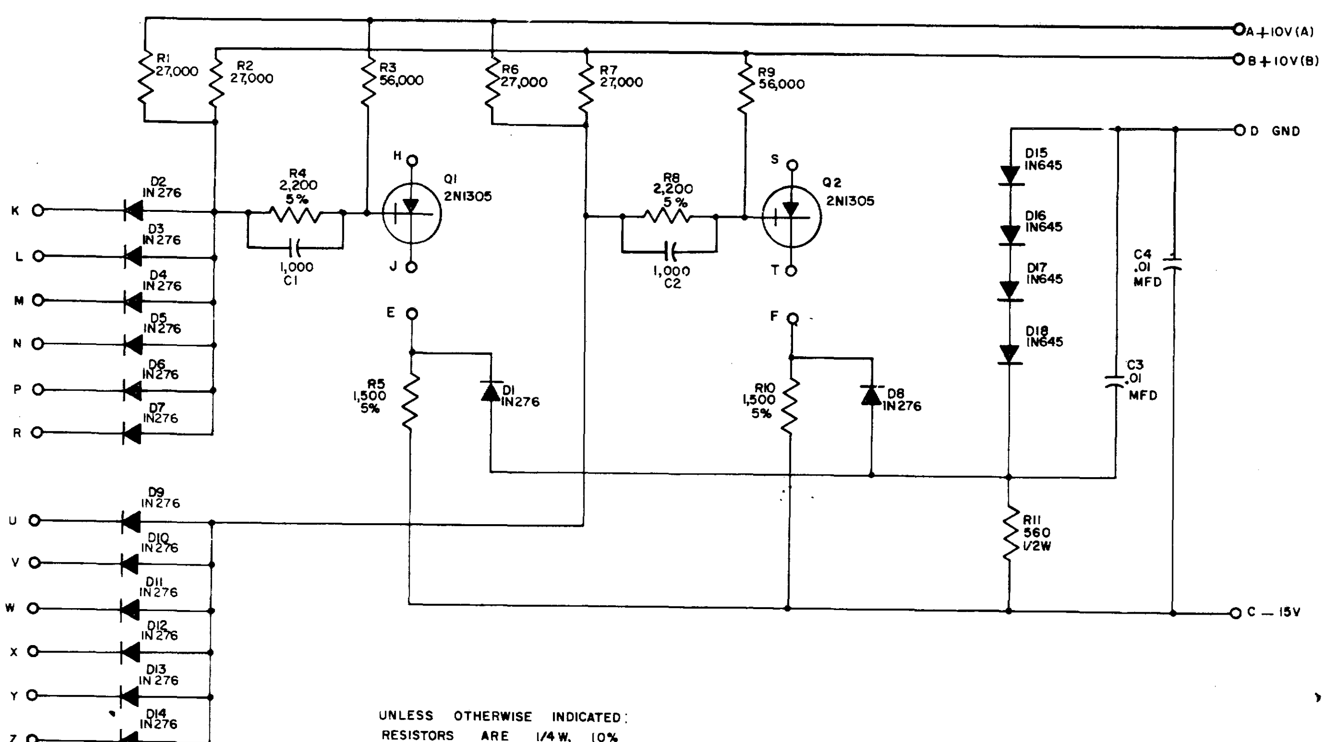
Drum Sense Amplifier 1537



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W 10%
CAPACITORS ARE MMFD

Inverters 4102

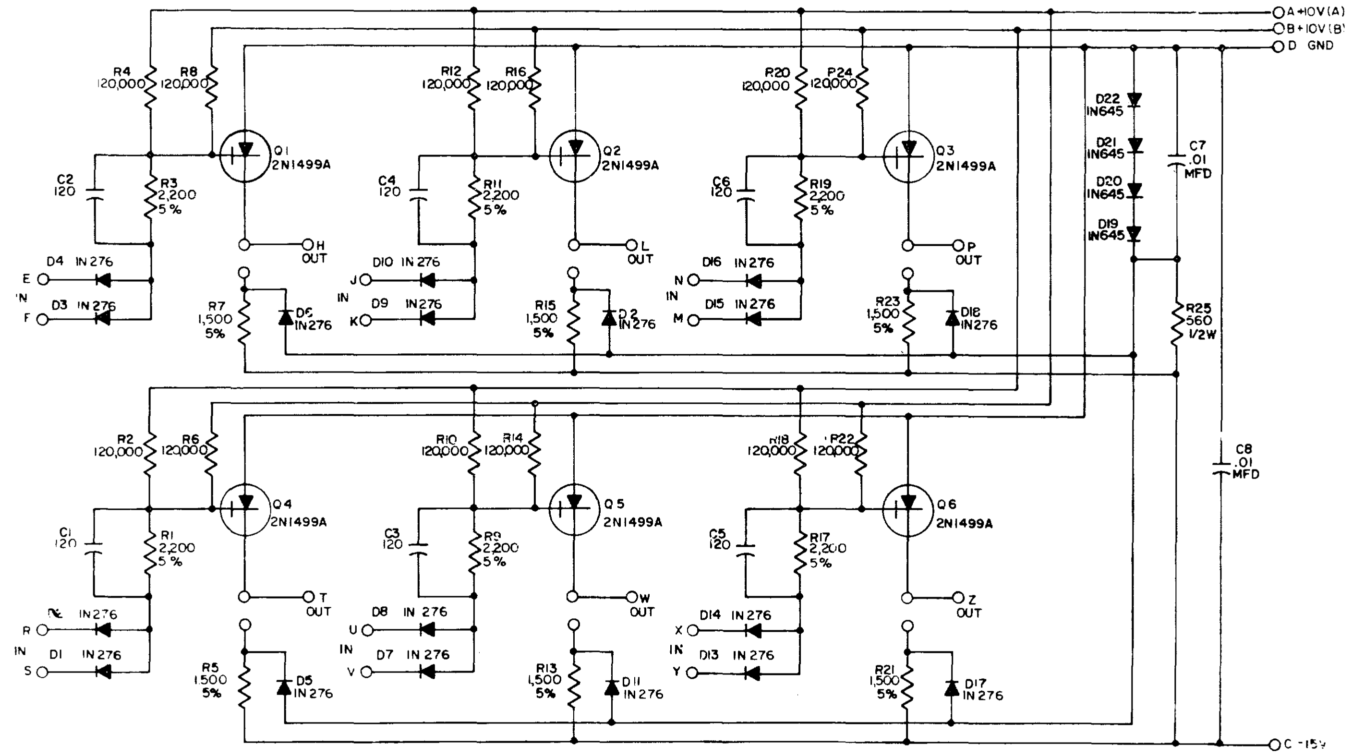
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

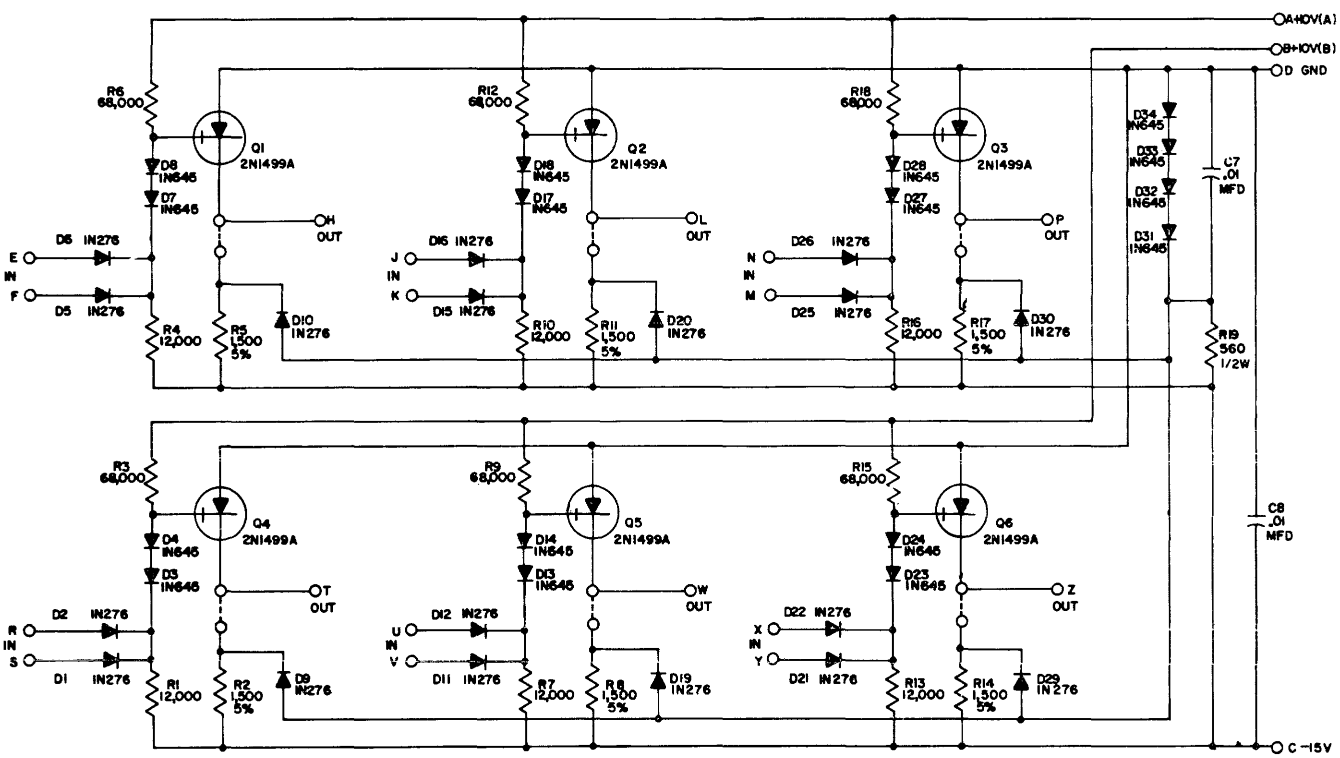
Diode Unit 4110



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W 10%
CAPACITORS ARE MMFD

Diode 4112

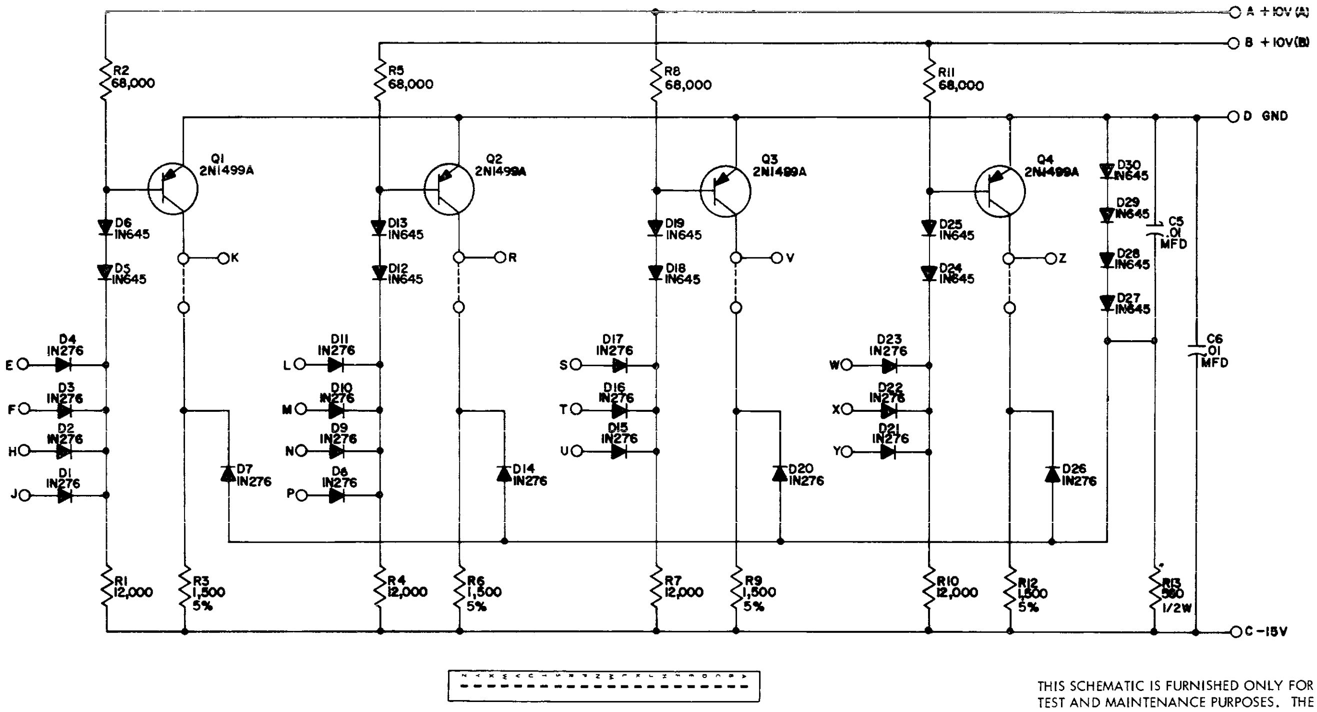
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

Diode 4113

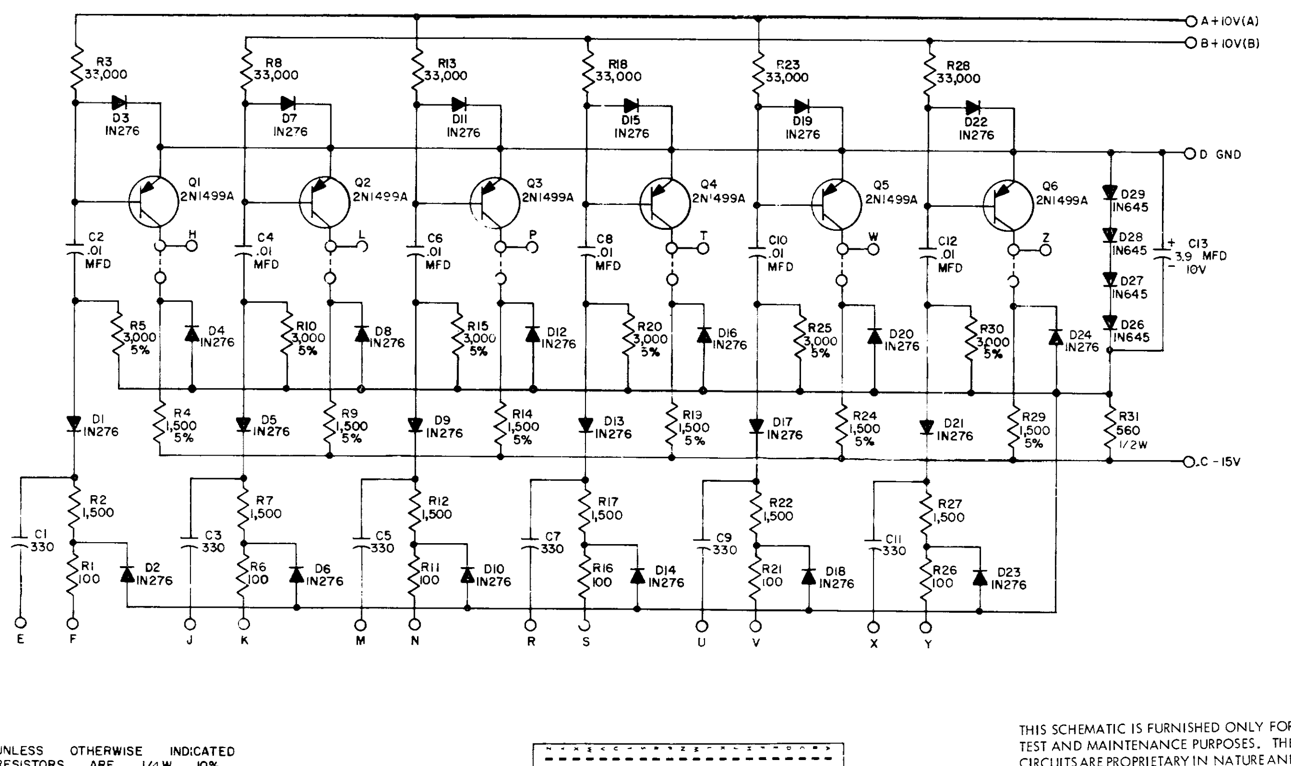
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

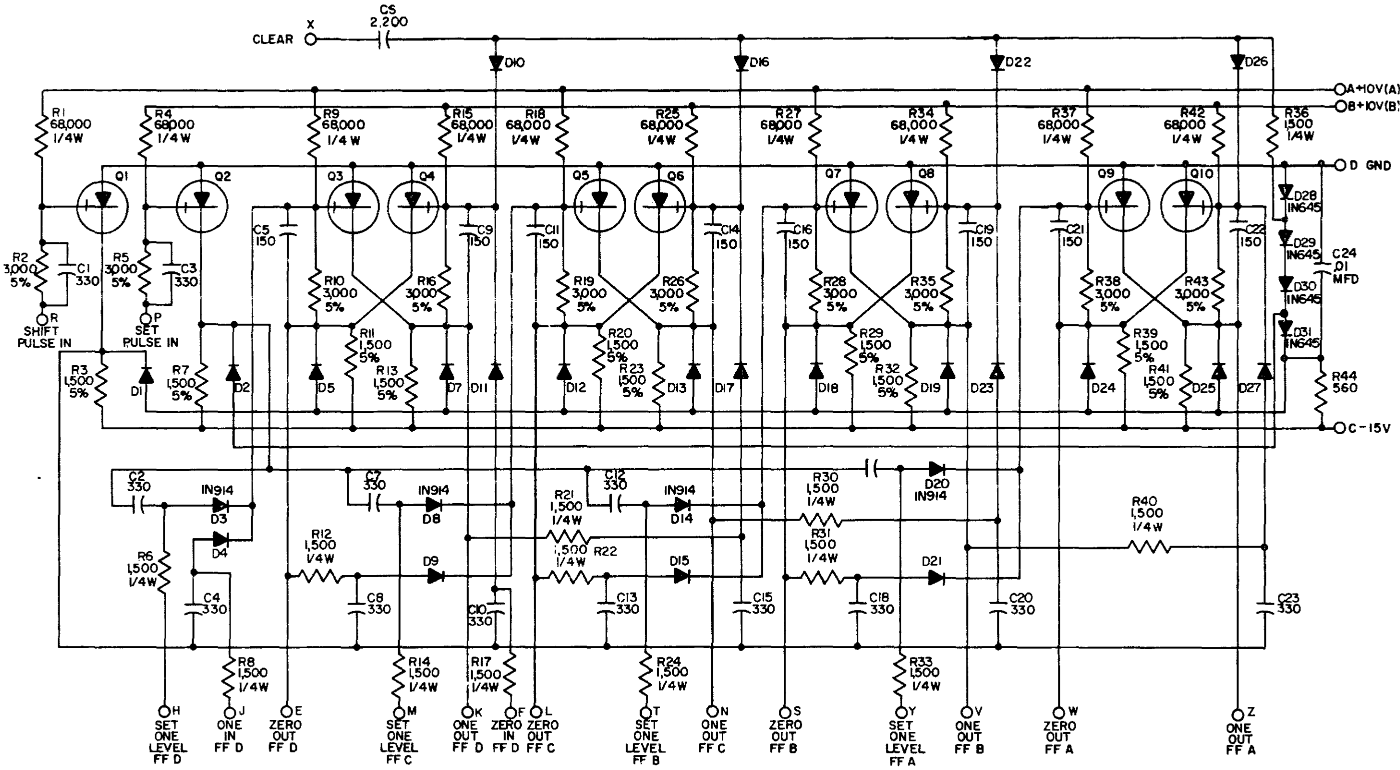
Diode 4115



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD

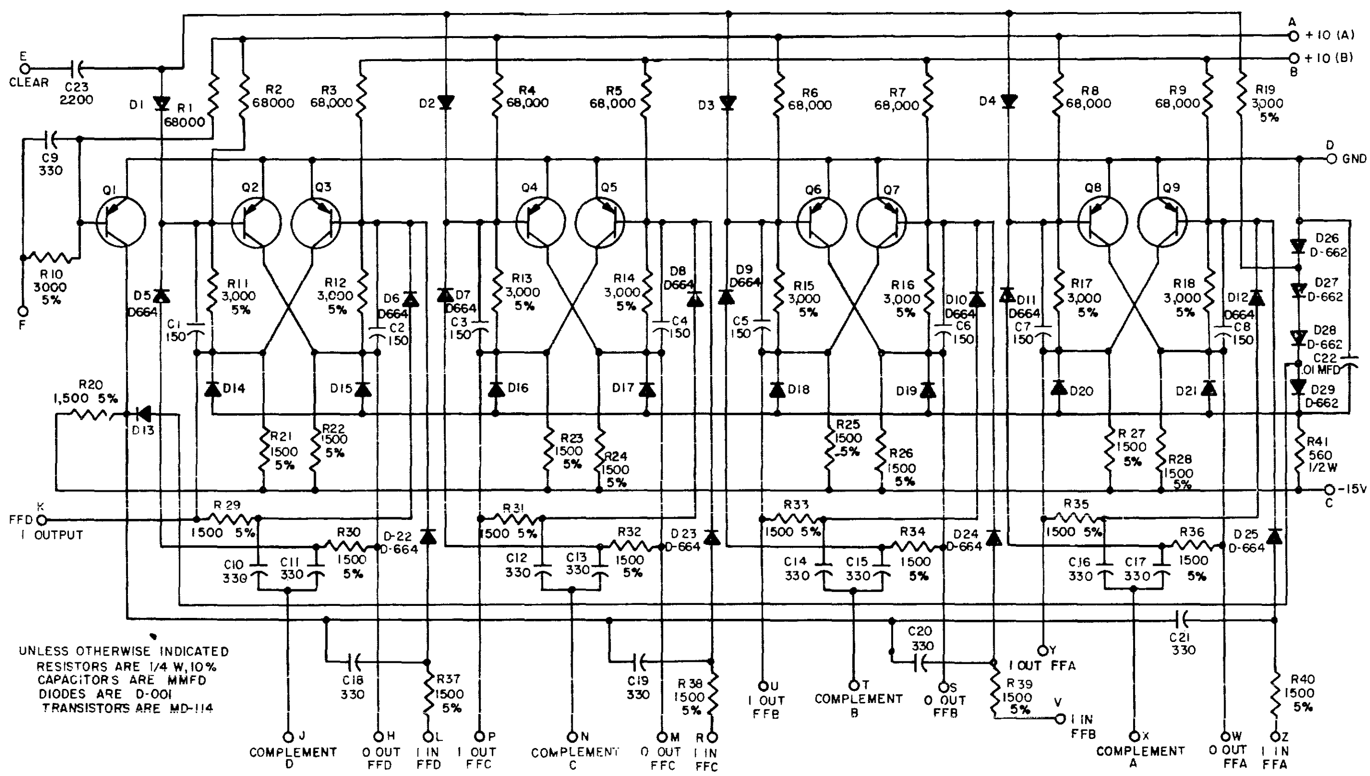
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

Capacitor-Diode Gates 4127



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%.
CAPACITORS ARE MMFD.
DIODES ARE IN276.
TRANSISTORS ARE 2N1499A

Quadruple Flip-Flop 4216



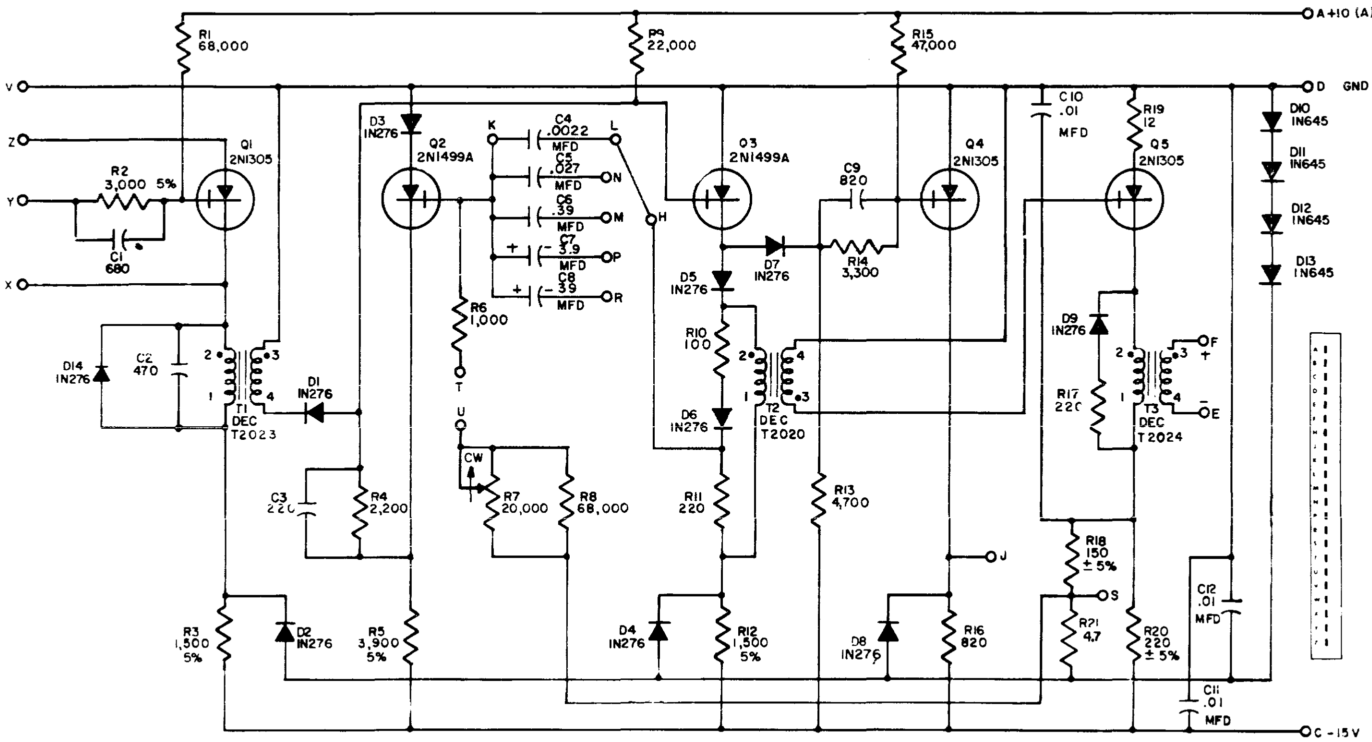
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-001
TRANSISTORS ARE MD-114

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N1499A		
D-001	IN276		
D-662	IN645		
D-664	IN914		

NOTES

B	RS-4217	2

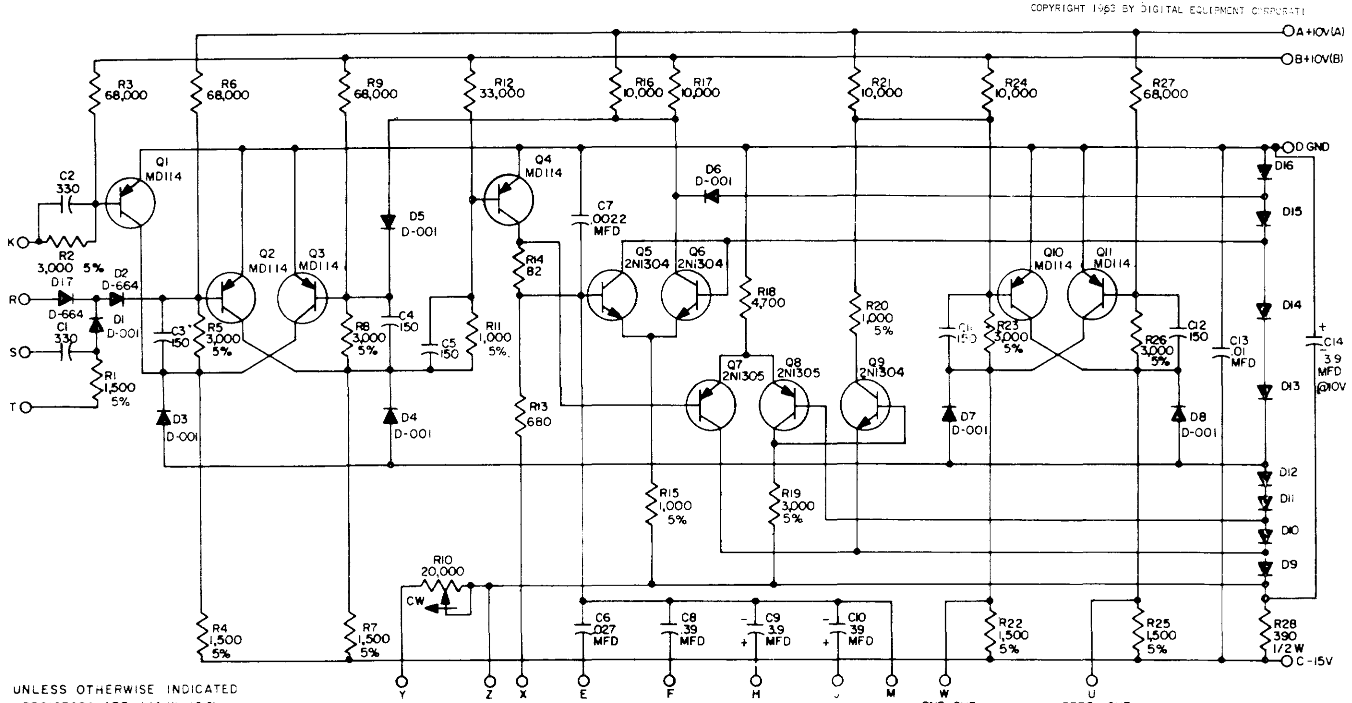
Four-Bit Counter 4217



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD

Delay 4301

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-662

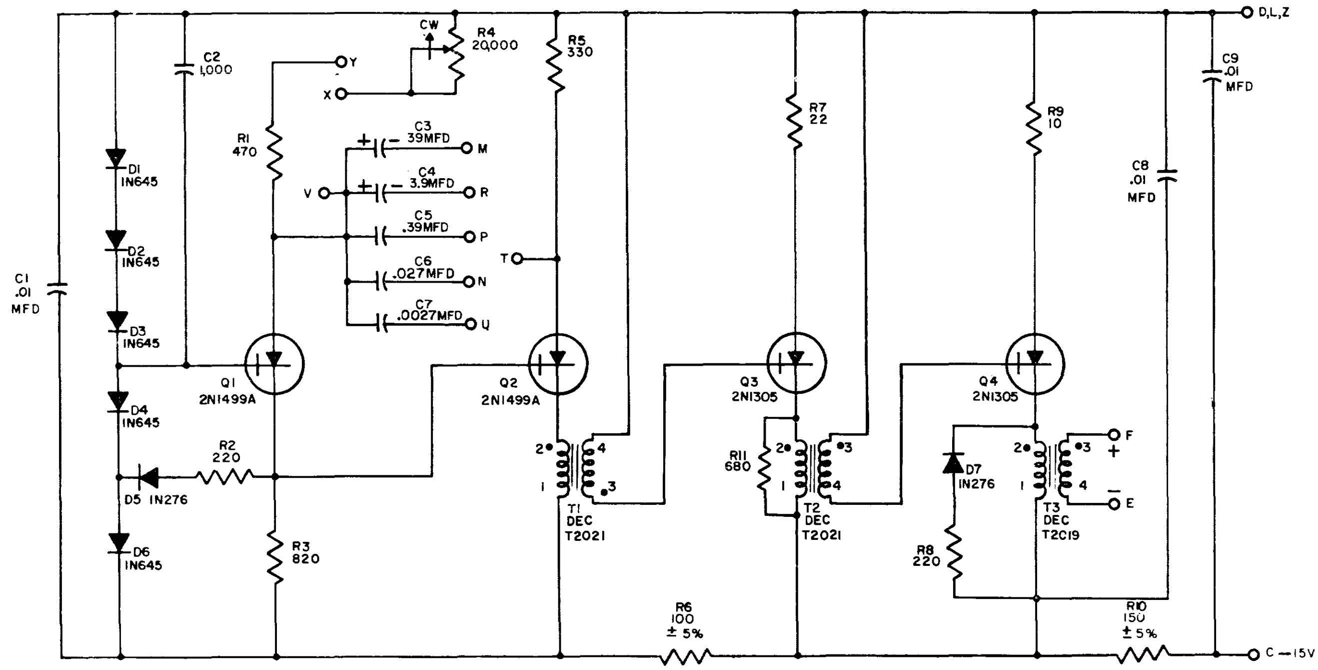
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N1499A	D-664	IN914
2N1304	2N1304		
2N1305	2N1305		
D-001	1N276		
D-662	1N645		

NOTES

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

H | RS 4303-9

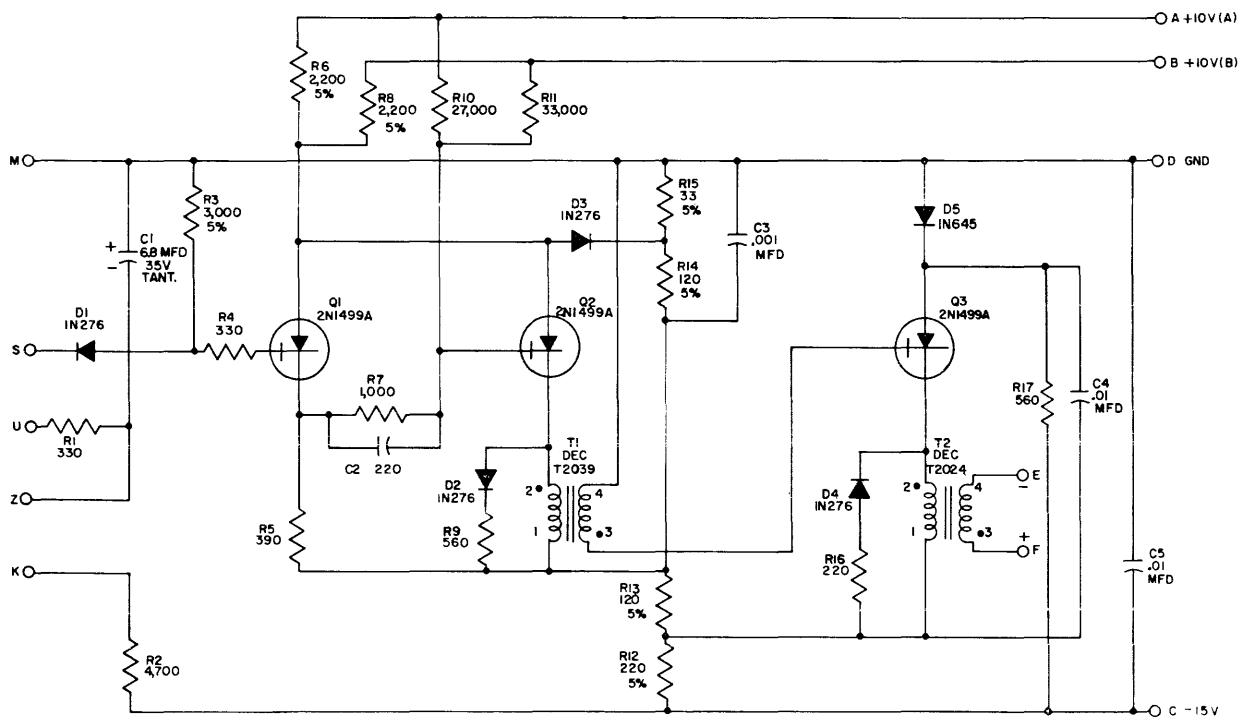
Integrating Single Shot 4303



UNLESS OTHERWISE INDICATED.
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

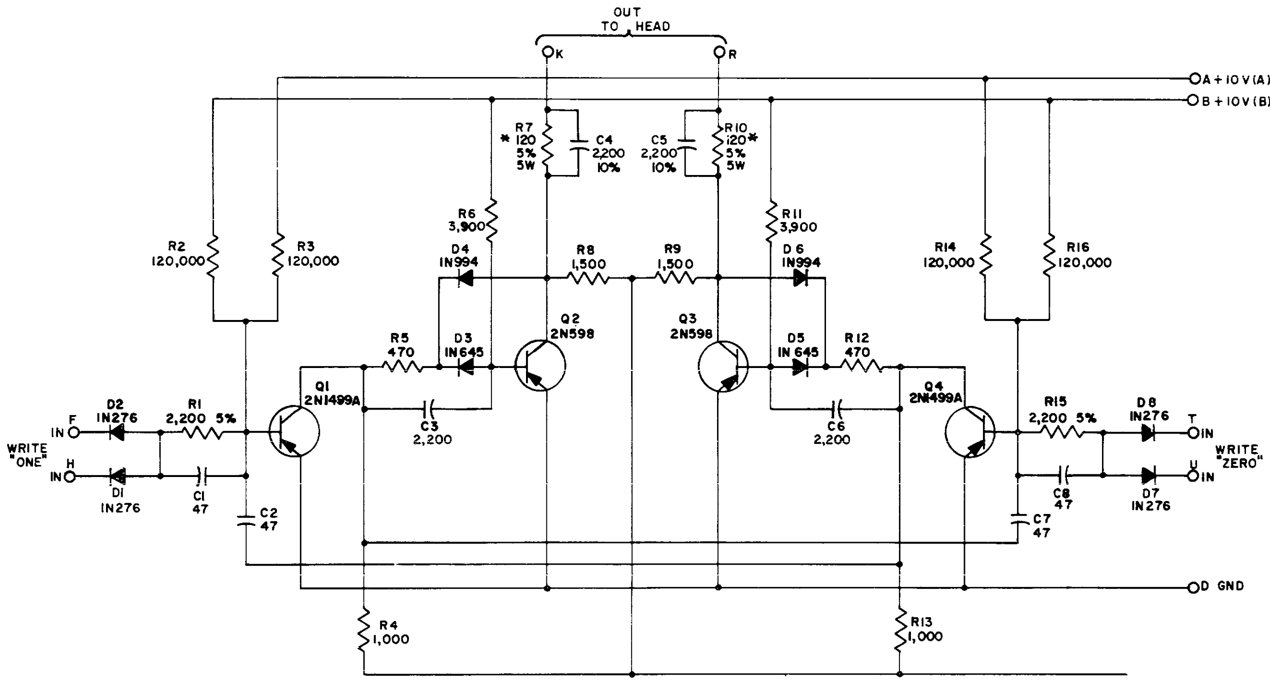
Variable Clock 4401



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W, 10%
CAPACITORS ARE MMFD

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

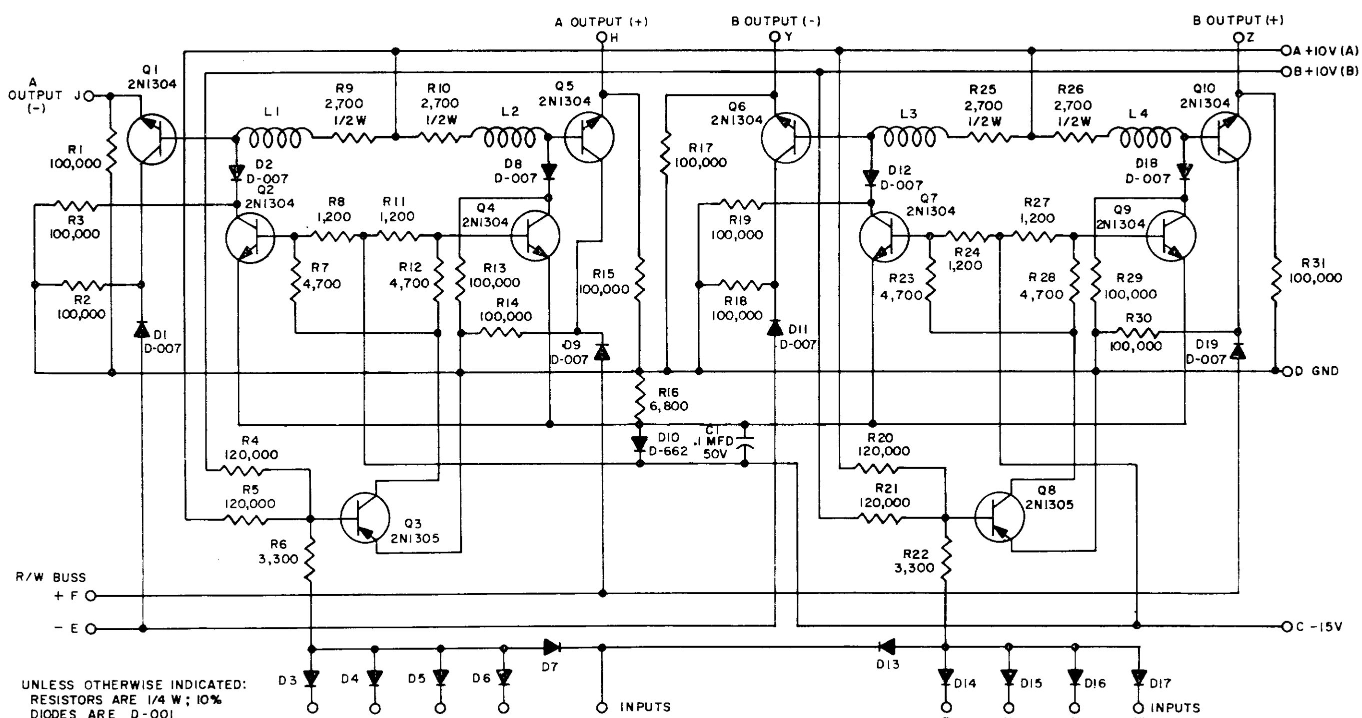
Pulse Generator 4410



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2 W, 10%
CAPACITORS ARE MMFD
*SPRAGUE 453E KOOLOHM

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY.

Drum NRZ Writer 4518



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
DIODES ARE D-001
INDUCTORS ARE ESSEX RFC-L
4700 μh

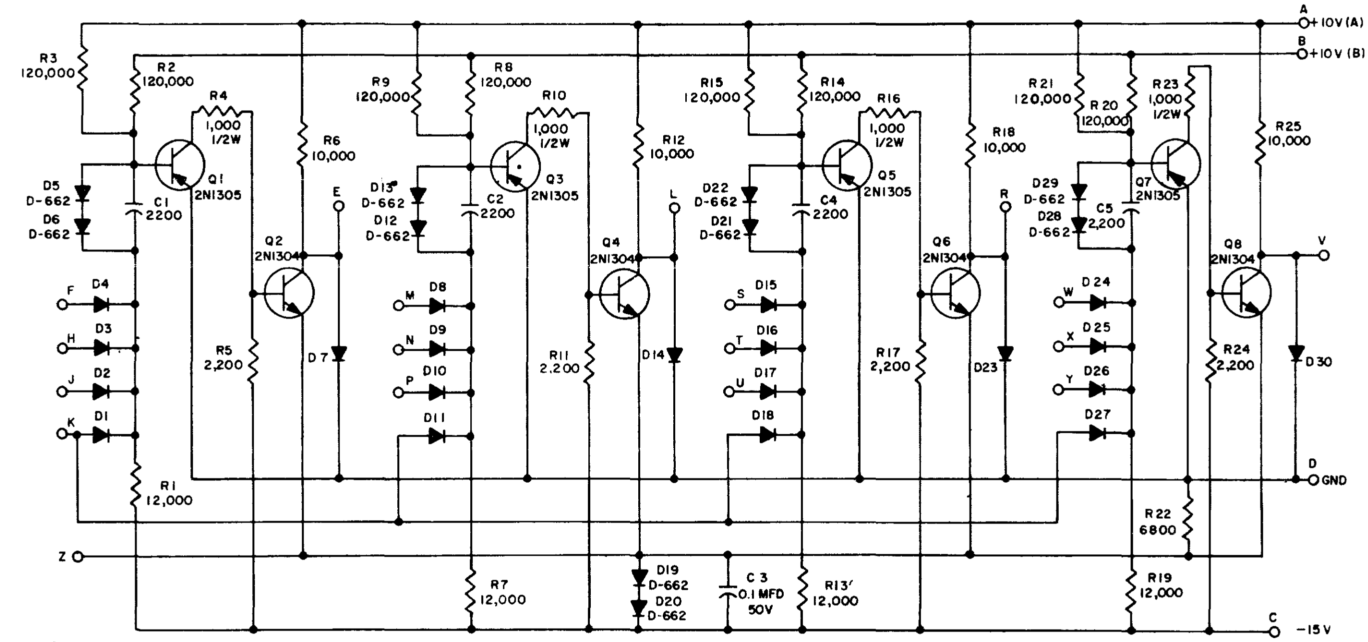
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N1304	2N1304		
2N1305	2N1305		
D-001	IN276		
D-007	IN277		
D-662	IN 645		

NOTES

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY

C | RS-4521

Drum X Select 4521



NOTE:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-001

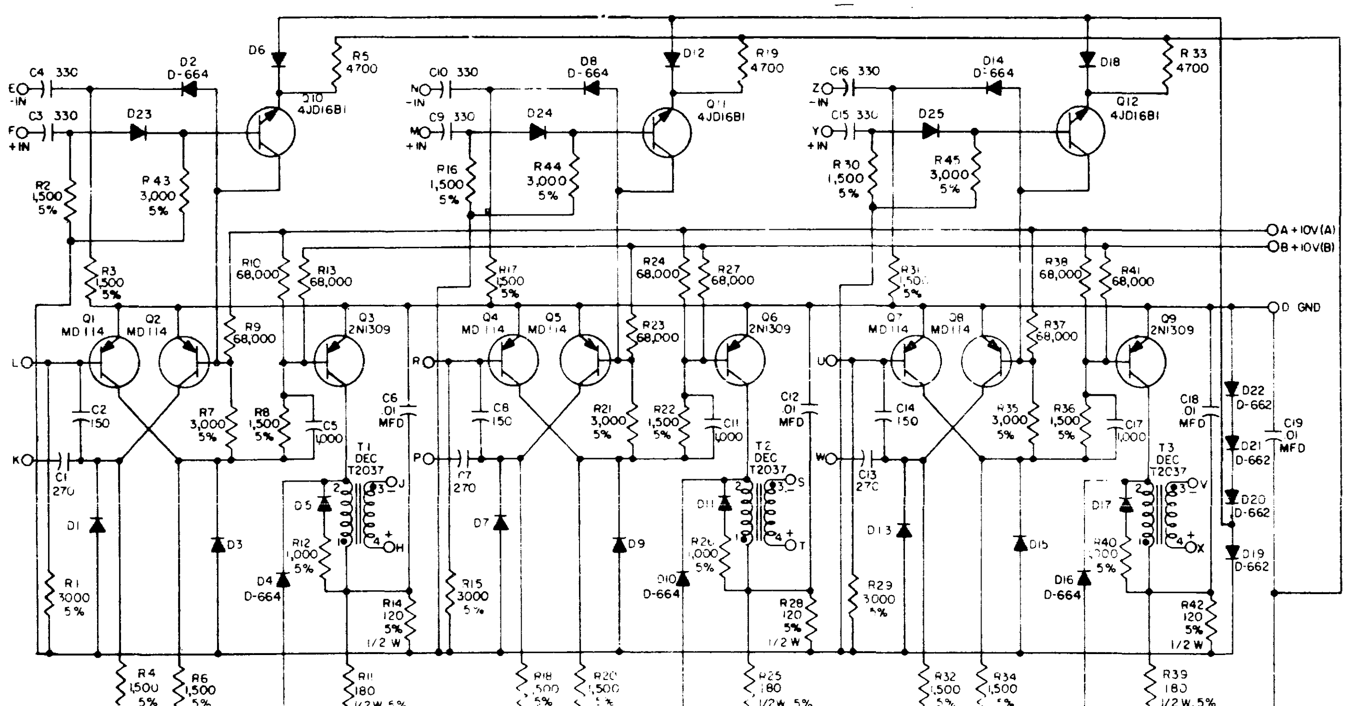
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N1305	2N1305		
2N1304	2N1304		
D-001	IN276		
D-662	IN645		

NOTES

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY

B	RS-4522	1

Drum Y Select 4522



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-001

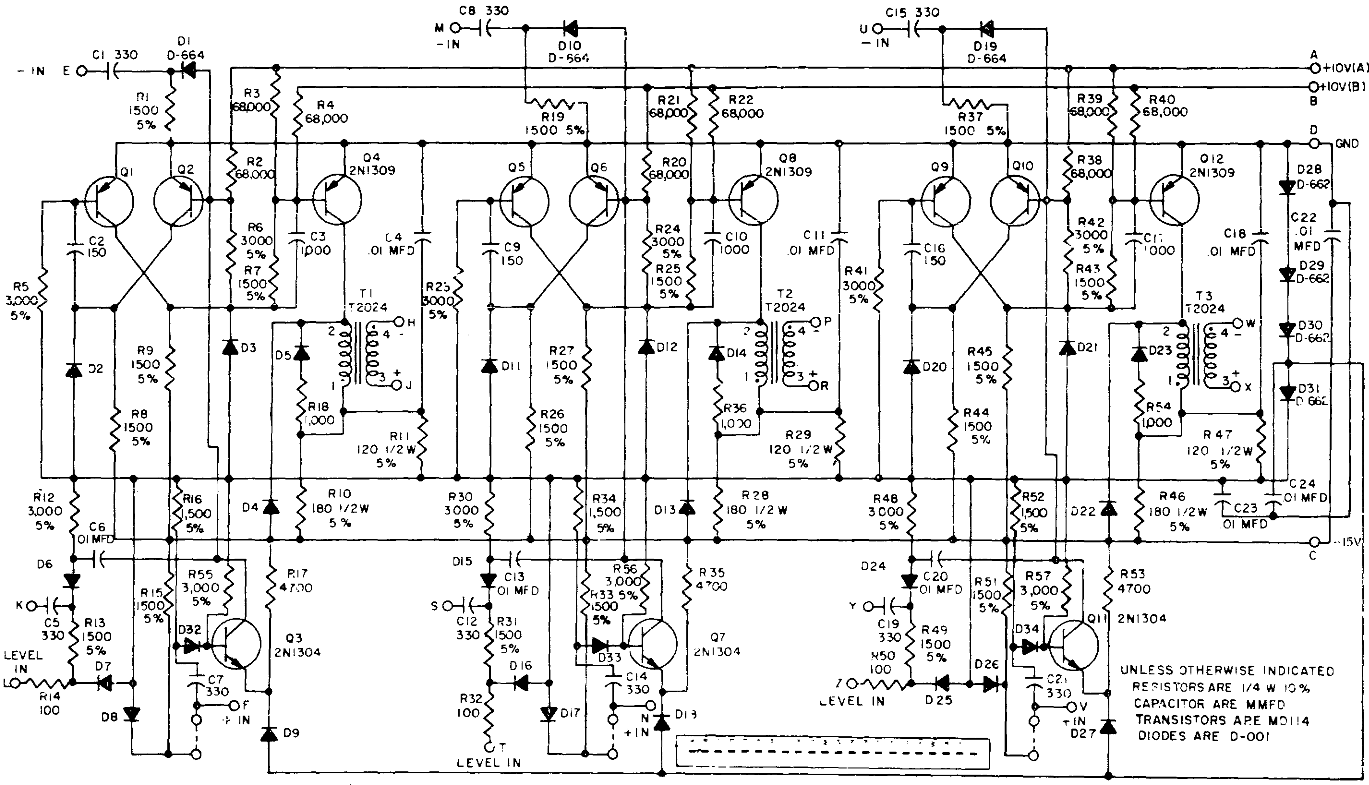
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
4JD16B1	2N2713	D-664	IN914
MD114	2N1499A		
2N1309	2N1309		
D-001	IN276		
D-662	IN645		

NOTES

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY

C	RS-4604	9

Pulse Amplifier 4604



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N1499A	D-664	IN914
2N1304	2N1304		
2N1309	2N1309		
D-001	IN276		
D-662	IN645		

NOTES

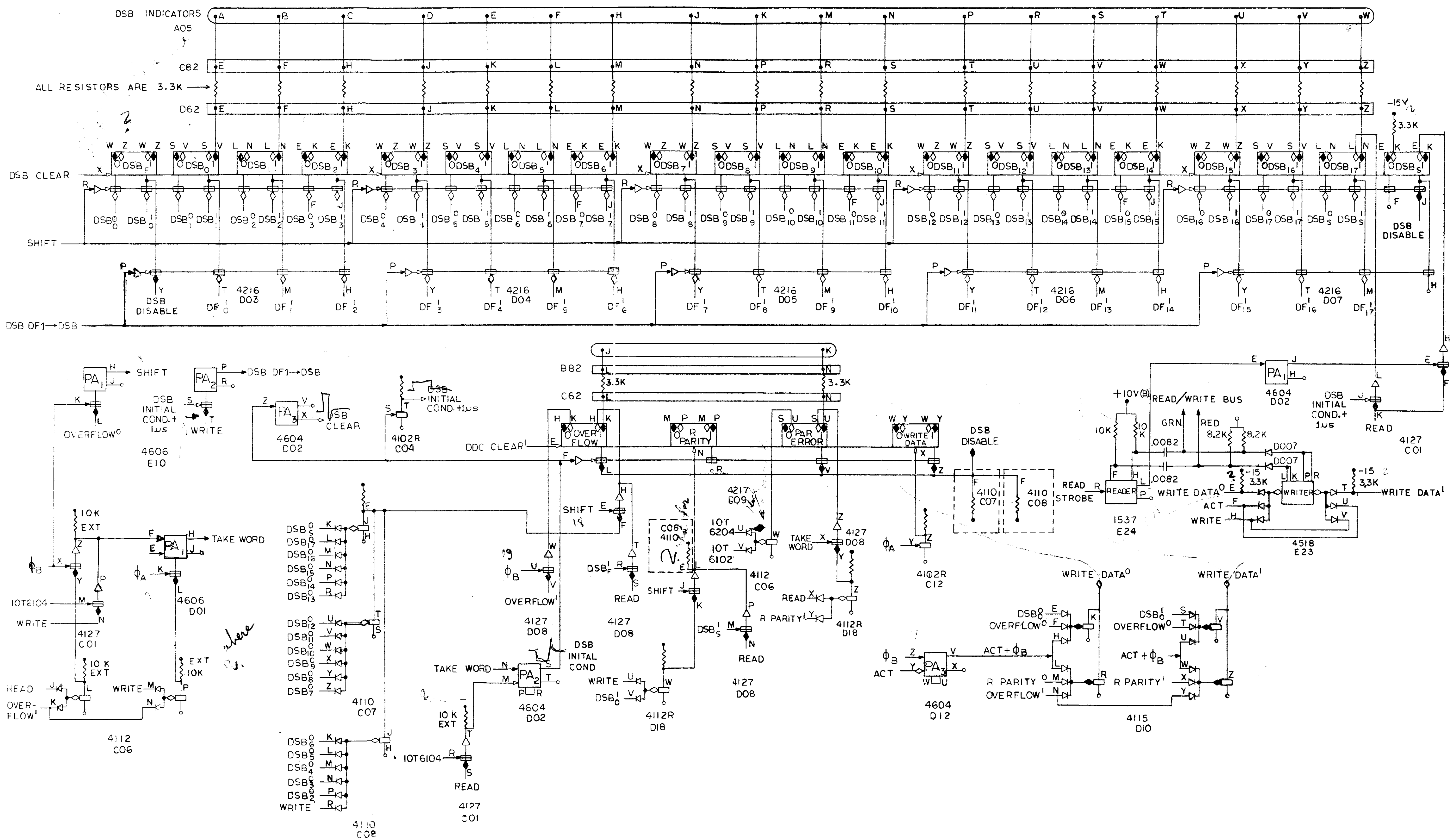
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY

C | RS-4606 | 2

Pulse Amplifier 4606

DSB, Control and Parity

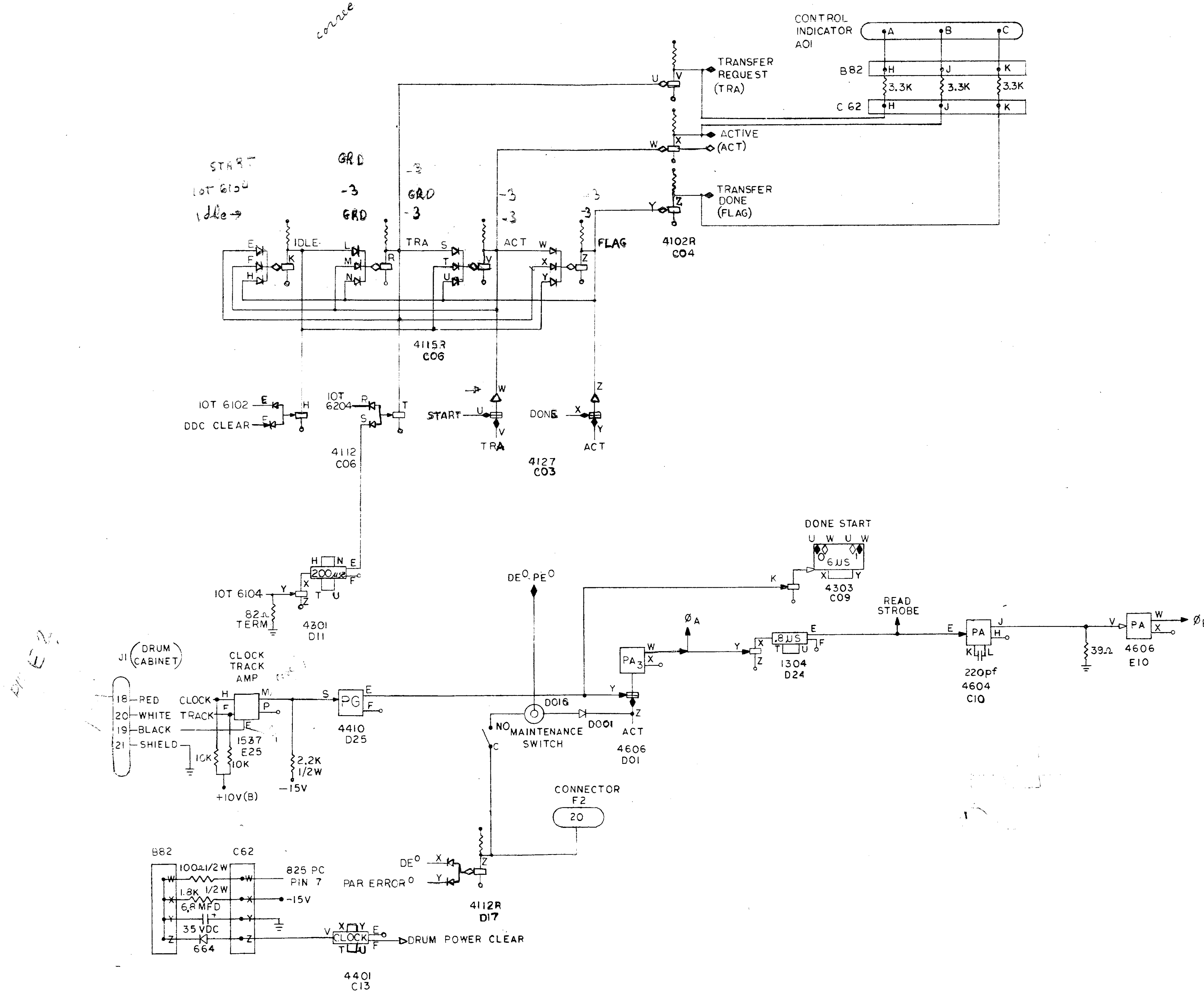
D-24602


DSB INDICATORS
A05
C82
ALL RESISTORS ARE 3.3K
D62
DSB CLEAR
SHIFT
DSB DF1→DSB
DSB DISABLE
4216
D03
4216
D04
4216
D05
4216
D06
4216
D07
PA1
SHIFT
OVERFLOW⁰
PA2
DSB DF1→DSB
DSB INITIAL COND.+ 1μs
WRITE
4606
E10
PA3
DSB CLEAR
4604
D02
DSB INITIAL COND.+1μs
4102R
C04
B82
C62
3.3K
DDC CLEAR¹
OVER FLOW
PARITY
PAR ERROR
WRITE DATA
DSB DISABLE
4110
C07
4110
C08
+10V(B)
READ/WRITE BUS
GRN
RED
8.2K
10K
.0082
D007
READ STROBE
READER
WRITER
WRITE DATA⁰
WRITE DATA¹
ACT
WRITE
1537
E24
4518
E23
PA1
4604
D02
DSB INITIAL COND.+ 1μs
READ
4127
C01
-15V
3.3K
10K EXT
TAKE WORD
IOT6104
WRITE
4127
C01
4606
D01
READ
OVER-FLOW¹
4112
C06
TAKE WORD
PA2
DSB INITAL COND
4604
D02
10K EXT
IOT6104
READ
4127
C01
OVERFLOW¹
4127
D08
SHIFT
READ
4127
D08
WRITE
4112R
D18
IOT 6204
IOT 6102
4217
E09
4112
C06
SHIFT
READ
4127
D08
TAKE WORD
4127
D08
READ
R PARITY¹
4112R
D18
4102R
C12
4110
C07
4110
C08
WRITE DATA⁰
WRITE DATA¹
OVERFLOW⁰
ACT+ΦB
R PARITY
OVERFLOW¹
R PARITY¹
ACT
PA3
4604
D12
4115
D10

Drum Control

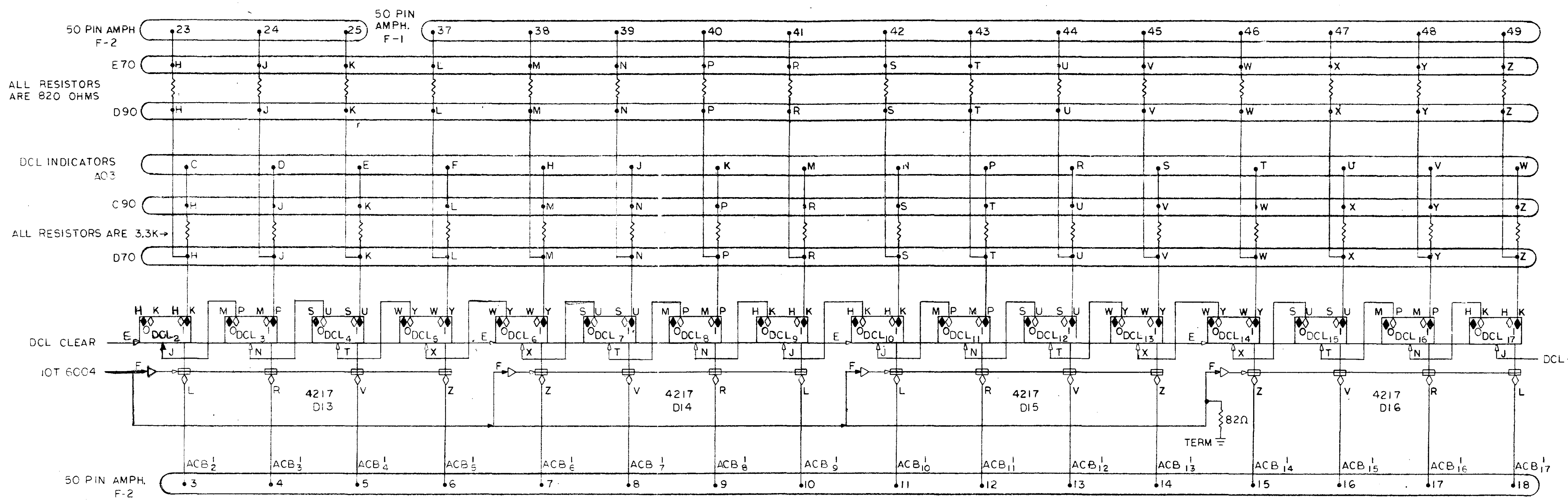
D-24603

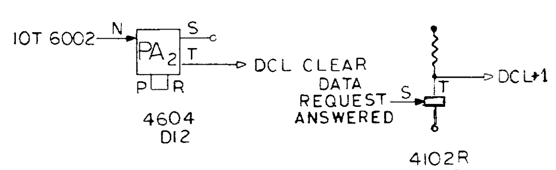
correct symbols !!!



Drum Core Location Counter

D-24604

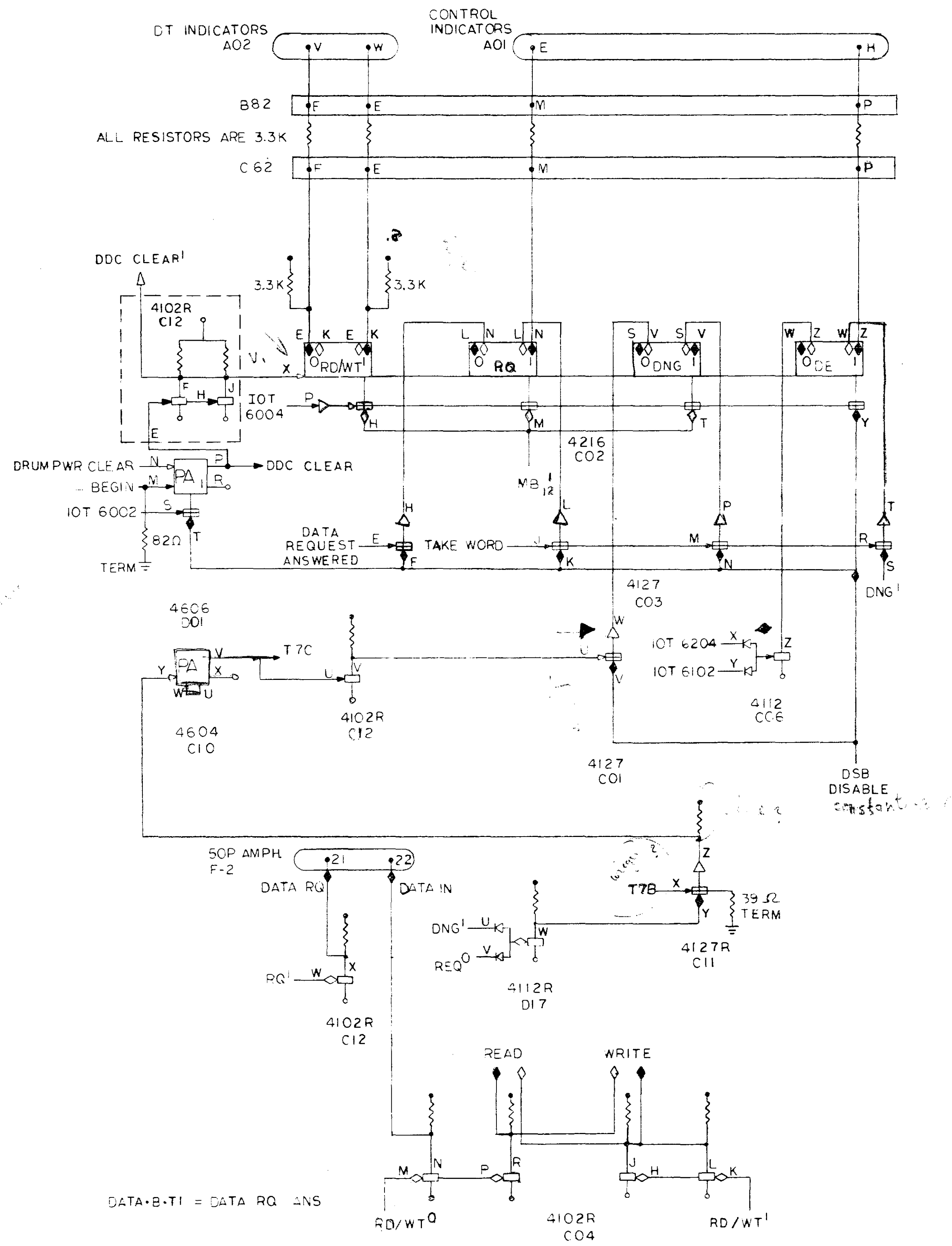

50 PIN AMPH F-2
50 PIN AMPH. F-1
E70
ALL RESISTORS ARE 820 OHMS
D90
DCL INDICATORS A03
C90
ALL RESISTORS ARE 3.3K
D70
DCL CLEAR
IOT 6004
DCL+1
4217 D13
4217 D14
4217 D15
4217 D16
82Ω
TERM
50 PIN AMPH. F-2


IOT 6002
PA2
DCL CLEAR
4604 D12
DATA REQUEST ANSWERED
DCL+1
4102R C12

Drum Data Channel

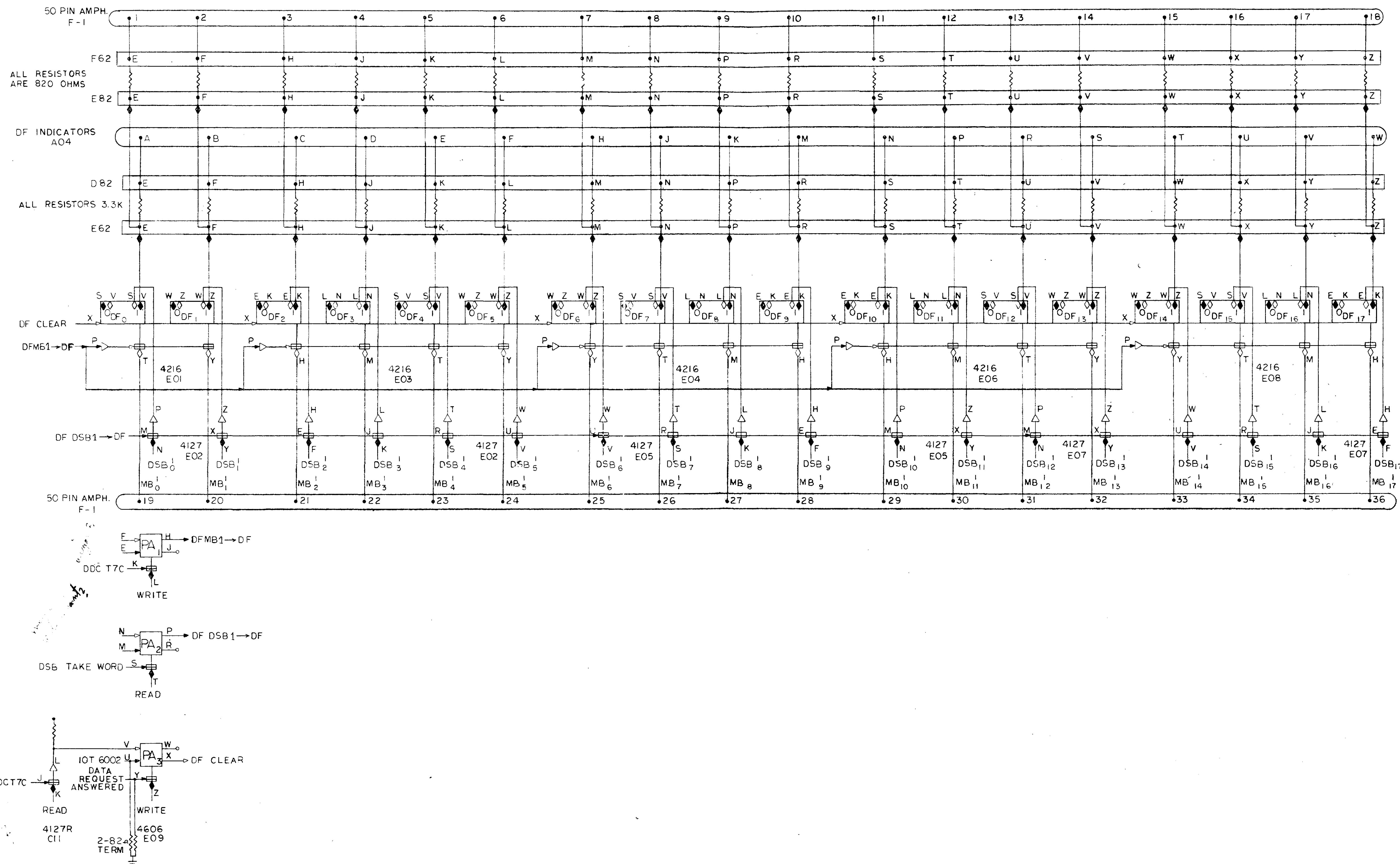
D-24605

7-21


DT INDICATORS
A02
CONTROL
INDICATORS
A01
B82
ALL RESISTORS ARE 3.3K
C62
DDC CLEAR
4102R
C12
3.3K
3.3K
RD/WT
RQ
DNG
DE
IOT
6004
4216
C02
DRUM PWR CLEAR
BEGIN
IOT 6002
82Ω
TERM
DDC CLEAR
DATA
REQUEST
ANSWERED
TAKE WORD
DNG
4127
C03
4606
D01
T7C
IOT 6204
IOT 6102
4112
C06
4102R
C12
4604
C10
4127
C01
DSB
DISABLE
50P AMPH.
F-2
DATA RQ
DATA IN
T7B
39 Ω
TERM
4127R
C11
4112R
D17
4102R
C12
READ
WRITE
4102R
C04
RD/WT
RD/WT
DATA·B·T1 = DATA RQ ANS

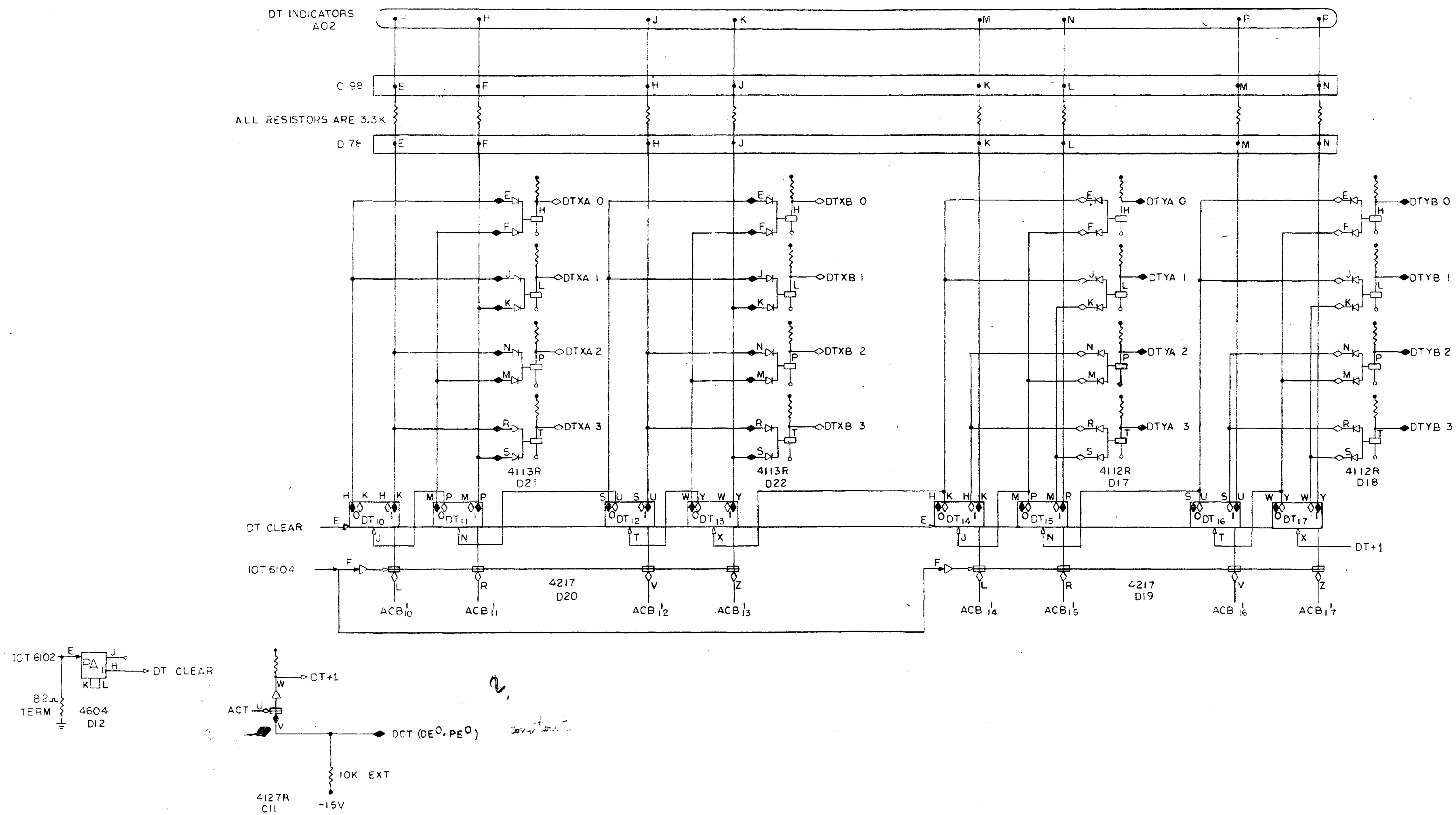
Drum Final Buffer and Data Channel

D-24606


50 PIN AMPH. F-1
F62
ALL RESISTORS ARE 820 OHMS
E82
DF INDICATORS A04
D82
ALL RESISTORS 3.3K
E62
DF CLEAR
DFMB1→DF
4216 E01
4216 E03
4216 E04
4216 E06
4216 E08
DF DSB1→DF
4127 E02
4127 E02
4127 E05
4127 E05
4127 E07
4127 E07
50 PIN AMPH. F-1
DFMB1→DF
DDC T7C
WRITE
DF DSB1→DF
DSB TAKE WORD
READ
IOT 6002
DATA REQUEST ANSWERED
DF CLEAR
DDCT7C
READ
WRITE
4127R C11
4606 E09
2-82 TERM

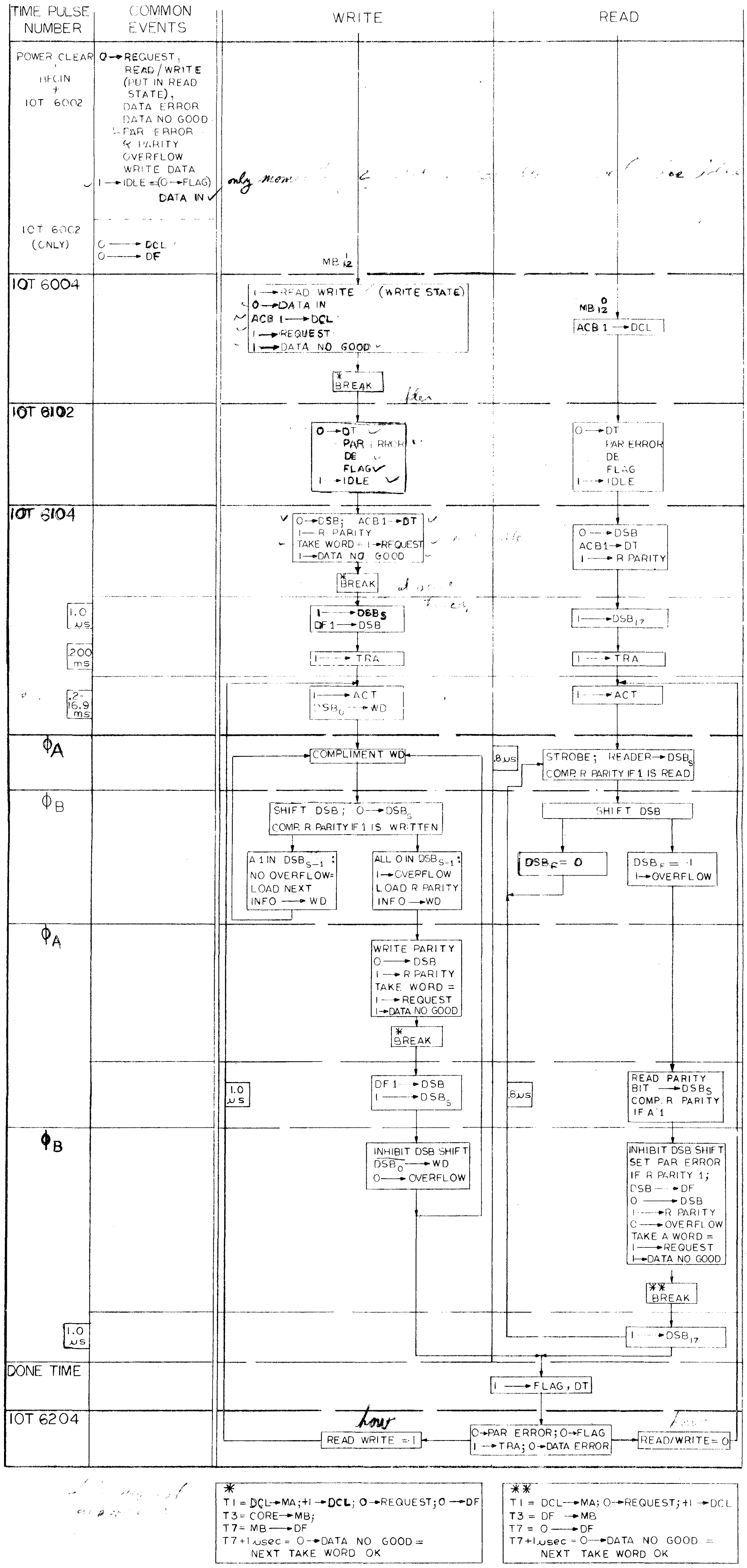
Drum Track Address Register & Decoding (X&Y)

D-24607


DT INDICATORS
A02
C 98
ALL RESISTORS ARE 3.3K
D 78
DTXA 0
DTXA 1
DTXA 2
DTXA 3
DTXB 0
DTXB 1
DTXB 2
DTXB 3
DTYA 0
DTYA 1
DTYA 2
DTYA 3
DTYB 0
DTYB 1
DTYB 2
DTYB 3
4113R
D21
4113R
D22
4112R
D17
4112R
D18
DT CLEAR
IOT 6104
4217
D20
4217
D19
DT+1
ACB 10
ACB 11
ACB 12
ACB 13
ACB 14
ACB 15
ACB 16
ACB 17
IOT 6102
PA
DT CLEAR
82Ω
TERM
4604
D12
DT+1
ACT
DCT (DE0, PE0)
10K EXT
-15V
4127R
C11

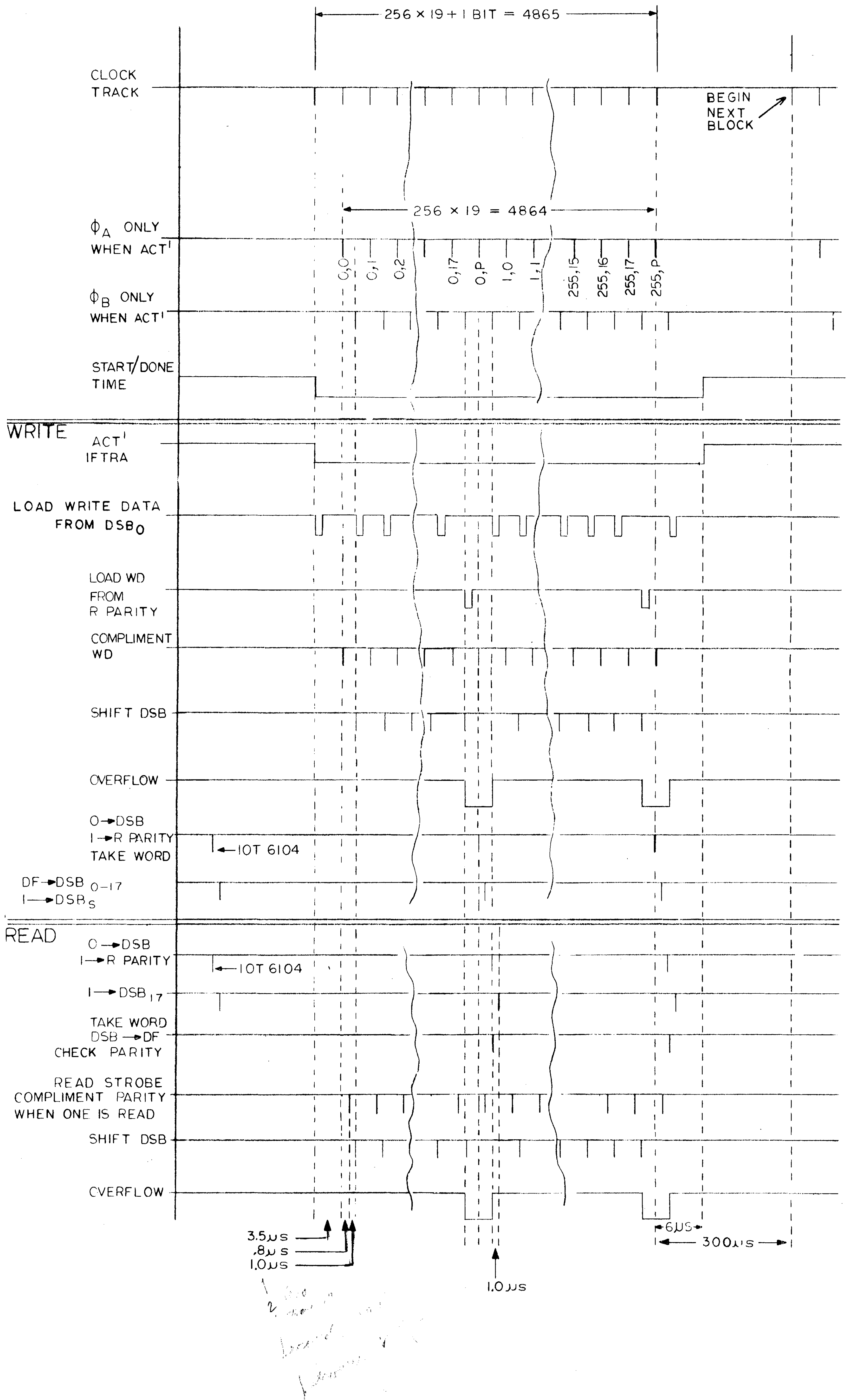
Flow Diagram

D-24611


TIME PULSE NUMBER
COMMON EVENTS
WRITE
READ
POWER CLEAR
BEGIN
IOT 6002
O→REQUEST, READ/WRITE (PUT IN READ STATE), DATA ERROR DATA NO GOOD PAR ERROR R PARITY OVERFLOW WRITE DATA
1→IDLE =(O→FLAG)
DATA IN
only mem
IOT 6002 (ONLY)
O→DCL
O→DF
MB 12
IOT 6004
1→READ WRITE (WRITE STATE)
O→DATA IN
ACB 1→DCL
1→REQUEST
1→DATA NO GOOD
ACB 1→DCL
BREAK
IOT 6102
O→DT
PAR ERROR
DE
FLAG
1→IDLE
IOT 6104
O→DSB; ACB1→DT
1→R PARITY
TAKE WORD = 1→REQUEST
1→DATA NO GOOD
O→DSB
ACB1→DT
1→R PARITY
BREAK
1.0 µs
1→DSB$_S$
DF 1→DSB
1→DSB$_{17}$
200 ms
1→TRA
.2-16.9 ms
1→ACT
DSB$_0$→WD
ΦA
COMPLIMENT WD
.8 µs
STROBE; READER→DSB$_S$
COMP. R PARITY IF 1 IS READ
ΦB
SHIFT DSB; O→DSB$_S$
COMP. R PARITY IF 1 IS WRITTEN
SHIFT DSB
A 1 IN DSB$_{S-1}$: NO OVERFLOW= LOAD NEXT INFO→WD
ALL O IN DSB$_{S-1}$: 1→OVERFLOW LOAD R PARITY INFO→WD
DSB$_F$ = O
DSB$_F$ = 1
1→OVERFLOW
ΦA
WRITE PARITY
O→DSB
1→R PARITY
TAKE WORD =
1→REQUEST
1→DATA NO GOOD
BREAK
1.0 µs
DF 1→DSB
1→DSB$_S$
.8 µs
READ PARITY BIT→DSB$_S$
COMP. R PARITY IF A 1
ΦB
INHIBIT DSB SHIFT
DSB$_0$→WD
O→OVERFLOW
INHIBIT DSB SHIFT
SET PAR ERROR IF R PARITY 1;
DSB→DF
O→DSB
1→R PARITY
O→OVERFLOW
TAKE A WORD =
1→REQUEST
1→DATA NO GOOD
BREAK
1.0 µs
1→DSB$_{17}$
DONE TIME
1→FLAG, DT
IOT 6204
READ WRITE = 1
O→PAR ERROR; O→FLAG
1→TRA; O→DATA ERROR
READ/WRITE = O
*
T1 = DCL→MA; +1→DCL; O→REQUEST; O→DF
T3 = CORE→MB;
T7 = MB→DF
T7+1 µsec = O→DATA NO GOOD = NEXT TAKE WORD OK
**
T1 = DCL→MA; O→REQUEST; +1→DCL
T3 = DF→MB
T7 = O→DF
T7+1 µsec = O→DATA NO GOOD = NEXT TAKE WORD OK

Timing Diagram

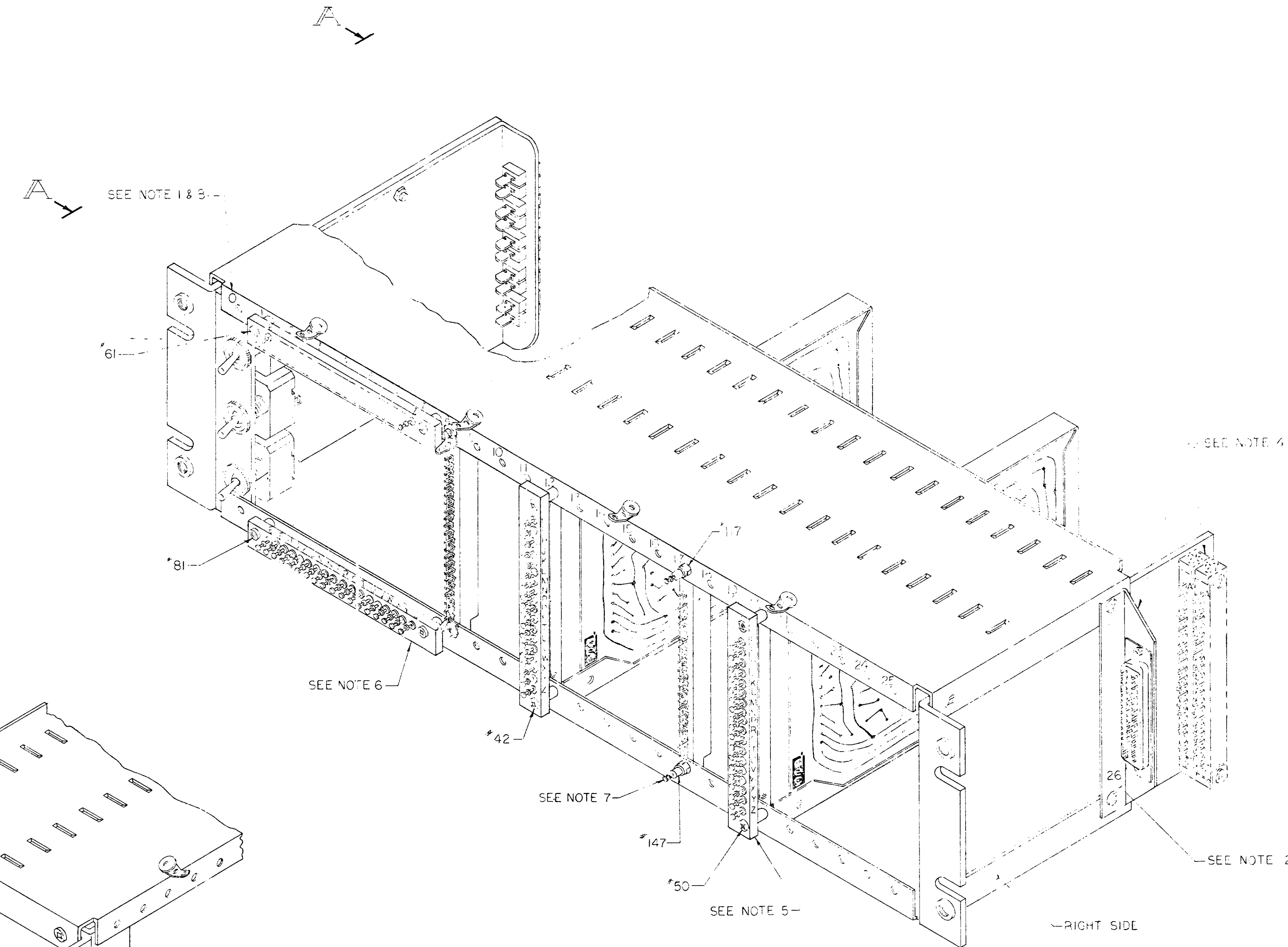
C-24612

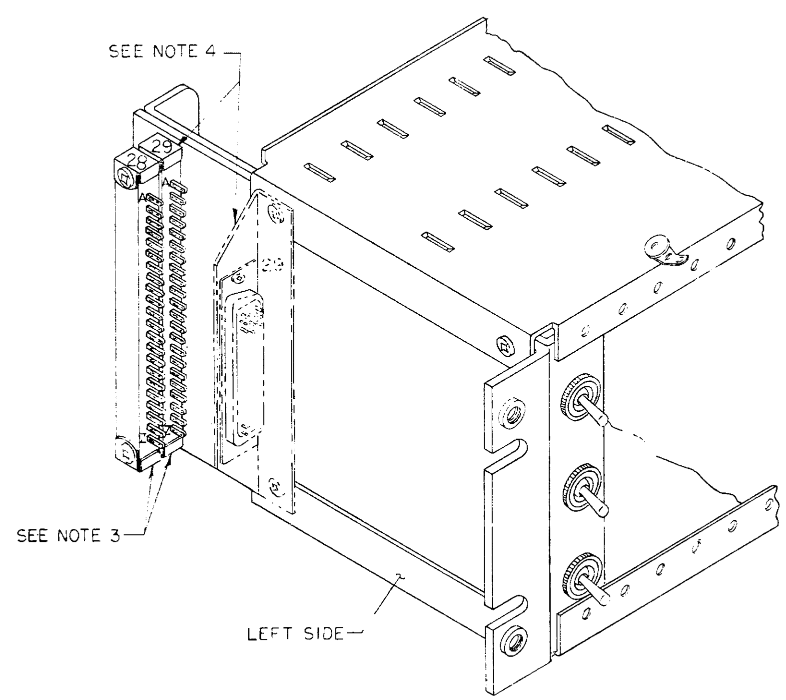


256 × 19 + 1 BIT = 4865
CLOCK TRACK
BEGIN NEXT BLOCK
256 × 19 = 4864
Φ_A ONLY WHEN ACT'
0,0
0,1
0,2
0,17
0,P
1,0
1,1
255,15
255,16
255,17
255,P
Φ_B ONLY WHEN ACT'
START/DONE TIME
WRITE
ACT' IFTRA
LOAD WRITE DATA FROM DSB_0
LOAD WD FROM R PARITY
COMPLIMENT WD
SHIFT DSB
OVERFLOW
0→DSB
1→R PARITY
TAKE WORD
IOT 6104
DF→DSB_{0-17}
1→DSB_S
READ
0→DSB
1→R PARITY
IOT 6104
1→DSB_{17}
TAKE WORD
DSB→DF
CHECK PARITY
READ STROBE
COMPLIMENT PARITY
WHEN ONE IS READ
SHIFT DSB
CVERFLOW
3.5μs
.8μs
1.0μs
1.0μs
6μs
300μs

Terminal Designation Layout

E-10208


A
A
SEE NOTE 1 & 8
61
81
SEE NOTE 6
42
SEE NOTE 7
147
50
SEE NOTE 5
RIGHT SIDE
SEE NOTE 2
SEE NOTE 4
26


SEE NOTE 4
SEE NOTE 3
LEFT SIDE
28
29

VIEW A-A

Utilization Module List

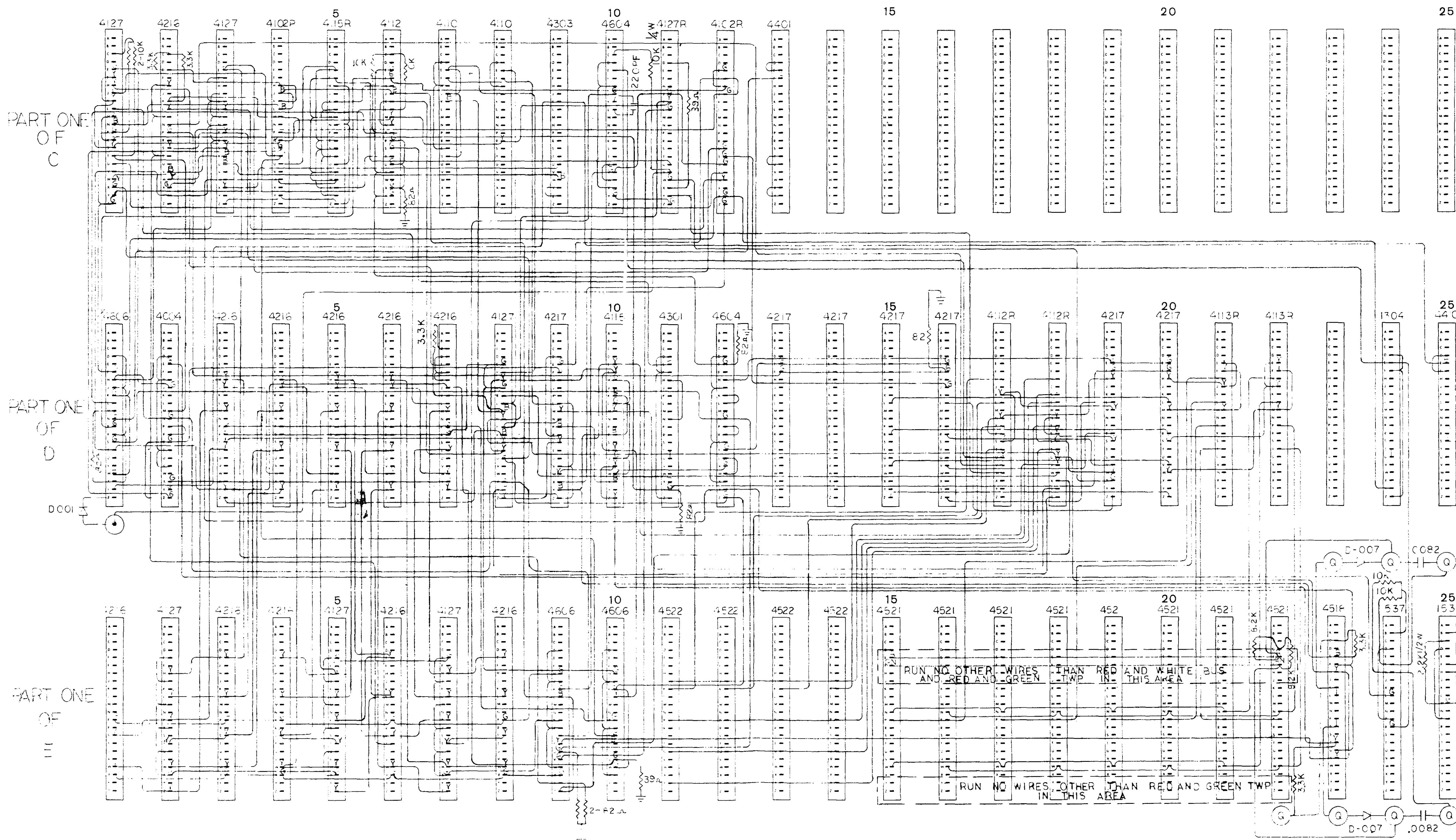
D-24601

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
	4127	4216	4127	4102R	4115R	4112	4110	4110	4303	4604	4127R	4102R	4401												
C	DSB5 DSB 1/2 TAKE WORD DSP DNG TAKE WORD	RD/WT RQ DNG DE	RQ DNG DE ACT FLAG	WRITE RTL IN READ DSP INIT TRA ACT FLAG	IDLE TRA ACT FLAG	IDLE TAKE WORD TRA PAR ERROR DE	DSB DISABLE VER FLOW	OVER-FLOW	DT/ST	PA1 DCT TA→8 PA3 T7C	DF CLR DT +1 T7C	DCC CLEAR DCL +1 DNG DATA RQ WR DATA	POWER CLEAR												
	4606	4604	4216	4216	4216	4216	4216	4127	4217	4115	4301	4604	4217	4217	4217	4217	4112R	4112R	4217	4217	4113R	4113R		1304	4410
D	PA1 TAKE WORD PA DC CLR PA DCT DA	PA DSB5 PA2 DSB PA DSB CLR	DSP	DSB	DSB	DSB	DSB	OVER-FLOW R PARITY OVER FLOW PAR ERROR	OVER FLOW R PARITY PAR ERROR WRITE DATA	WRITE DATA 0 WRITE DATA 1	DELAY IOT 6104	PA1 DT CLR PA2 DCL CLR PA3 ACT·Φ_B	DCL	DCL	DCL	DCL	DTYA T7C DE·PER ERROR	DTYB R PARITY	DT	DT	DTXA	DTXB		READ STROBE	CLOCK TRACK PG
	4216	4127	4216	4216	4127	4216	4127	4216	4606	4606	4522	4522	4522	4522	4521	4521	4521	4521	4521	4521	4521	4521	4518	1537	1537
E	DF	DF	DF	DF	DF	DF	DF	DF	PA DFMB 1→DF PA DF DSB 1→DF PA DF CLR	DSB PA1 SHIFT PA2 DSB DF 1→DSB PA2 DCT CB	'Y' AXES	'Y' AXES	'Y' AXES	'Y' AXES	'X' AXES	'X' AXES	'X' AXES	'X' AXES	'X' AXES	'X' AXES	'X' AXES	'X' AXES	WRITER	READER	CLOCK TRACK AMP

Wiring Diagram (Logic)

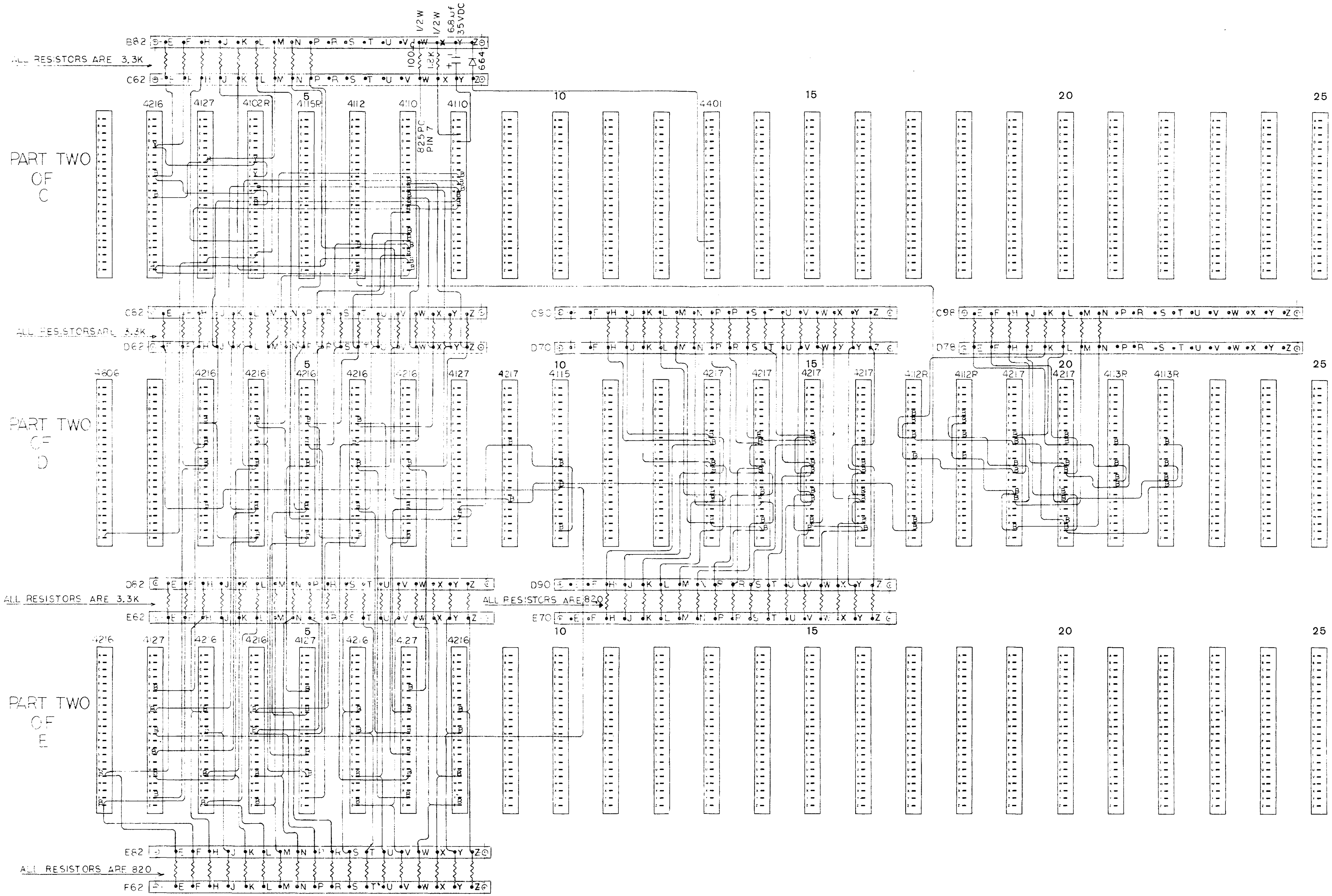
Sheet 1 of 2

D-24609


PART ONE OF C
PART ONE OF D
PART ONE OF E
RUN NO OTHER WIRES THAN RED AND WHITE BUS AND RED AND GREEN TWP IN THIS AREA
RUN NO WIRES OTHER THAN RED AND GREEN TWP IN THIS AREA
D-007
.0082
D001

Wiring Diagram (Logic)
Sheet 2 of 2

D-24609

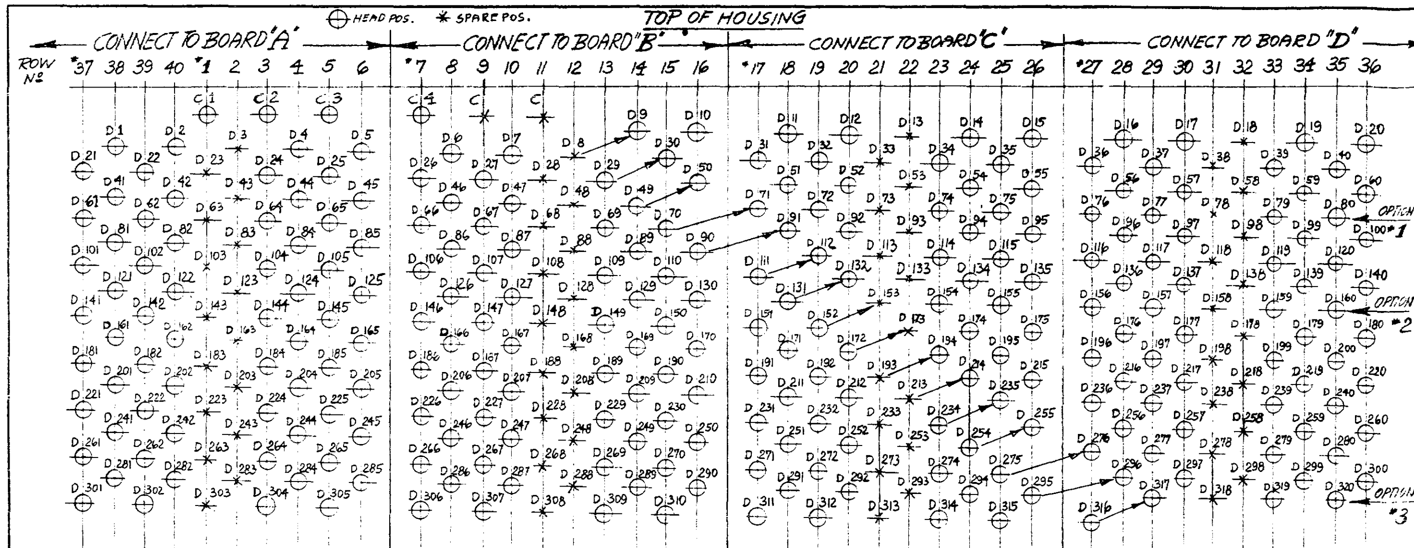

B82
ALL RESISTORS ARE 3.3K
C62
1/2 W
1/2 W
68 uf
35VDC
100
1.2K
664
825PC
PIN 7
4216
4127
4102R
4115R
4112
4110
4110
4401
5
10
15
20
25
PART TWO OF C
C82
ALL RESISTORS ARE 3.3K
D62
C90
D70
C98
D78
4606
4216
4216
4216
4216
4216
4127
4217
4115
4217
4217
4217
4217
4112R
4112R
4217
4217
4113R
4113R
PART TWO OF D
D82
ALL RESISTORS ARE 3.3K
E62
D90
ALL RESISTORS ARE 820
E70
4216
4127
4216
4216
4127
4216
4127
4216
PART TWO OF E
E82
ALL RESISTORS ARE 820
F62

Wiring Schedule (Drum)

D-24619

NUMBER W-46

TOP OF HOUSING

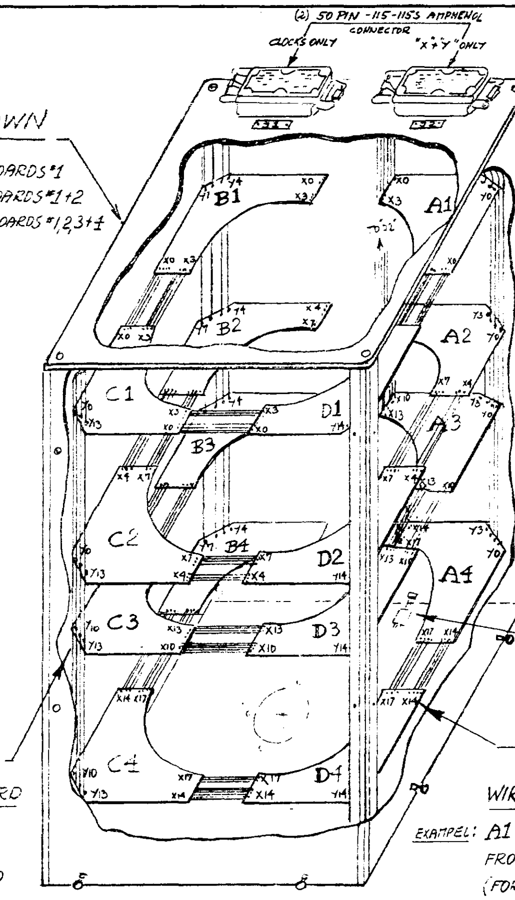


DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP	DATA HEAD	BOARD GROUP
TO DIODE BOARD: A1										TO DIODE BOARD: B1										TO DIODE BOARD: C1										TO DIODE BOARD: D1									
41	Q	42	M	43	I	44	E	45	A	46	Q	47	M	48	I	49	E	50	A	51	Q	52	M	53	I	54	E	55	A	56	Q	57	M	58	I	59	E	60	A
61	S	62	O	63	K	64	G	65	C	66	S	67	O	68	K	69	G	70	C	71	S	72	O	73	K	74	G	75	C	76	S	77	O	78	K	79	G	80	C
1	R	2	N	3	J	4	F	5	B	6	R	7	N	8	J	9	F	10	B	11	R	12	N	13	J	14	F	15	B	16	R	17	N	18	J	19	F	20	B
21	T	22	P	23	L	24	H	25	D	26	T	27	P	28	L	29	H	30	D	31	T	32	P	33	L	34	H	35	D	36	T	37	P	38	L	39	H	40	D
TO DIODE BOARD: A2										TO DIODE BOARD: B2										TO DIODE BOARD: C2										TO DIODE BOARD: D2									
121	Q	122	M	123	I	124	E	125	A	126	Q	127	M	128	I	129	E	130	A	131	Q	132	M	133	I	134	E	135	A	136	Q	137	M	138	I	139	E	140	A
141	S	142	O	143	K	144	G	145	C	146	S	147	O	148	K	149	G	150	C	151	S	152	O	153	K	154	G	155	C	156	S	157	O	158	K	159	G	160	C
81	R	82	N	83	J	84	F	85	B	86	R	87	N	88	J	89	F	90	B	91	R	92	N	93	J	94	F	95	B	96	R	97	N	98	J	99	F	100	B
101	T	102	P	103	L	104	H	105	D	106	T	107	P	108	L	109	H	110	D	111	T	112	P	113	L	114	H	115	D	116	T	117	P	118	L	119	H	120	D
TO DIODE BOARD: A3										TO DIODE BOARD: B3										TO DIODE BOARD: C3										TO DIODE BOARD: D3									
201	Q	202	M	203	I	204	E	205	A	206	Q	207	M	208	I	209	E	210	A	211	Q	212	M	213	I	214	E	215	A	216	Q	217	M	218	I	219	E	220	A
221	S	222	O	223	K	224	G	225	C	226	S	227	O	228	K	229	G	230	C	231	S	232	O	233	K	234	G	235	C	236	S	237	O	238	K	239	G	240	C
161	R	162	N	163	J	164	F	165	B	166	R	167	N	168	J	169	F	170	B	171	R	172	N	173	J	174	F	175	B	176	R	177	N	178	J	179	F	180	B
181	T	182	P	183	L	184	H	185	D	186	T	187	P	188	L	189	H	190	D	191	T	192	P	193	L	194	H	195	D	196	T	197	P	198	L	199	H	200	D
TO DIODE BOARD: A4										TO DIODE BOARD: B4										TO DIODE BOARD: C4										TO DIODE BOARD: D4									
281	Q	282	M	283	I	284	E	285	A	286	Q	287	M	288	I	289	E	290	A	291	Q	292	M	293	I	294	E	295	A	296	Q	297	M	298	I	299	E	300	A
301	S	302	O	303	K	304	G	305	C	306	S	307	O	308	K	309	G	310	C	311	S	312	O	313	K	314	G	315	C	316	S	317	O	318	K	319	G	320	C
241	R	242	N	243	J	244	F	245	B	246	R	247	N	248	J	249	F	250	B	251	R	252	N	253	J	254	F	255	B	256	R	257	N	258	J	259	F	260	B
261	T	262	P	263	L	264	H	265	D	266	T	267	P	268	L	269	H	270	D	271	T	272	P	273	L	274	H	275	D	276	T	277	P	278	L	279	H	280	D

(4) 50 PIN - 115-1155 AMPHENOL CONNECTOR

REF. OPTION #3 SHOWN

OPTION #1 = 86 TRACKS – 4 BOARDS #1
OPTION #2 = 166 " " – 8 BOARDS #1+2
OPTION #3 = 326 " " – 16 BOARDS #1,2,3+4



LOCATION OF "J3" (MOTOR CONNECTOR)

"Y" SELECTOR BOARD WIRING:

WIRE EACH CORNER BOARD AS SHOWN.

EXAMPEL: C4 TO C3, C3 TO C2, C2 TO C1 AND C1 TO CONNECTOR "J2" (FOR PIN # SEE CHART BELOW)

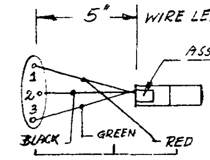
"X" SELECTOR BOARD WIRING:

WIRE EACH BOARD FLOOR AS SHOWN.

EXAMPEL: A1 TO D1, D1 TO C1, C1 TO B1 FROM A1 TO CONNECTOR "J2" (FOR PIN # SEE CHART BELOW)

5" WIRE LENGTH FOR ALL DATA HEADS #12A2

ASSEMBLE HEAD WITH FLAT FACING TO THE LEFT.

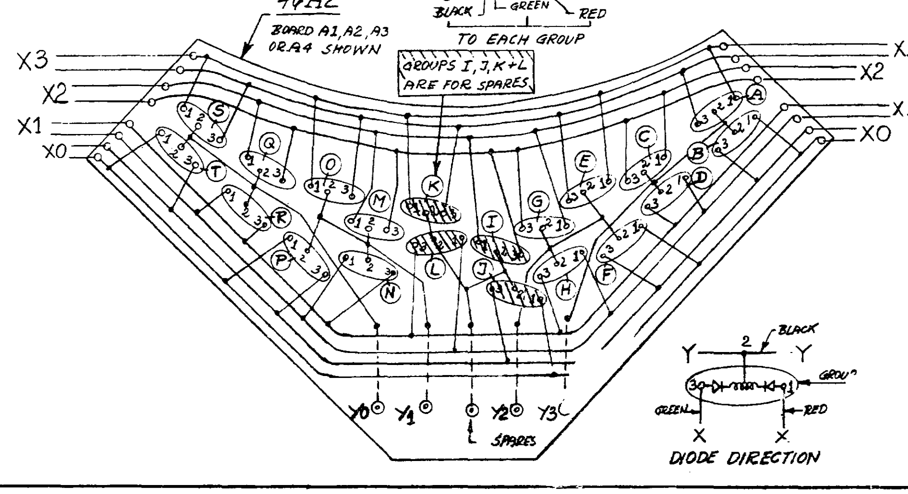


OPTION #1 = 64 DATA
OPTION #2 = 128 "
OPTION #3 = 256 "
SPARES PLUG UP WITH #17M79-2

#46A2

BOARD A1, A2, A3 OR A4 SHOWN

GROUPS I, J, K+L ARE FOR SPARES



DIODE DIRECTION

(OPTION #1, 2+3)

"X" SELECTOR CODE

FOR DIODE BOARDS

A1+B1 C1+D1	A2+B2 C2+D2	A3+B3 C3+D3	A4+B4 C4+D4
X0	X4	X10	X14
X1	X5	X11	X15
X2	X6	X12	X16
X3	X7	X13	X17
OPTION #1			
← OPTION #2 →		OPTION #3 →	

(OPTION 1, 2+3)

"Y" SELECTOR CODE

FOR DIODE BOARDS

A1+A2 A3+A4	Y0	Y1	Y2	Y3
B1+B2 B3+B4	Y4	Y5	Y6	Y7
C1+C2 C3+C4	Y10	Y11	Y12	Y13
D1+D2 D3+D4	Y14	Y15	Y16	Y17
ALL OPTIONS "Y0" THRU "Y17"				

"X" AND "Y" SELECTOR TO CONNECTOR "J2"

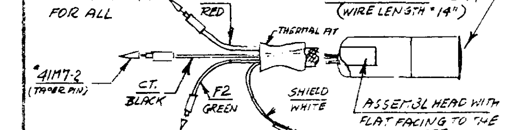
BOARD	CODE	COLOR	PIN		BOARD	CODE	COLOR	PIN	
A1	X0	RED	1	ALL OPTIONS (C)	A2	X4	RED	9	OPTIONS #2 + #3 (C)
A1	X0	GRN.	2		A2	X4	GRN.	10	
A1	X1	RED	3		A2	X5	RED	11	
A1	X1	GRN.	4		A2	X5	GRN.	12	
A1	X2	RED	5		A2	X6	RED	13	
A1	X2	GRN.	6		A2	X6	GRN.	14	
A1	X3	RED	7		A2	X7	RED	15	
A1	X3	GRN.	8		A2	X7	GRN.	16	
"Y" SELECTOR									
A1	Y0	BLACK	34	ALL OPTIONS	A3	X10	RED	17	OPTION #3 ONLY
A1	Y1	"	35		A3	X10	GRN.	18	
A1	Y2	"	36		A3	X11	RED	19	
A1	Y3	"	37		A3	X11	GRN.	20	
B1	Y4	"	38		A3	X12	RED	22	
B1	Y5	"	39		A3	X12	GRN.	23	
B1	Y6	"	40		A3	X13	RED	24	
B1	Y7	"	41		A3	X13	GRN.	25	
C1	Y10	"	42						
C1	Y11	"	43		A4	X14	RED	26	
C1	Y12	"	44		A4	X14	GRN.	27	
C1	Y13	"	45		A4	X15	RED	28	
D1	Y14	"	46		A4	X15	GRN.	29	
D1	Y15	"	47		A4	X16	RED	30	
D1	Y16	"	48		A4	X16	GRN.	31	
D1	Y17	"	49		A4	X17	RED	32	
		"			A4	X17	GRN	33	
GROUND LUG		"	50						

CLOCK HEADS CONNECT TO "J1" (B)

HEAD	CODE	COLOR	PIN	HEAD	CODE	COLOR	PIN	HEAD	CODE	COLOR	PIN
C1	S1	RED	43	C3	S1	RED	26		S1	RED	
"	CT.	BLACK	44	"	CT.	BLACK	27		CT.	BLACK	
"	F2	GREEN	45	"	F2	GREEN	28		F2	GREEN	
"	SHIELD	WHITE	46	"	SHIELD	WHITE	29		SHIELD	WHITE	
C2	S1	RED	35	C4	S1	RED	18		S1	RED	
"	CT.	BLACK	36	"	CT.	BLACK	19		CT.	BLACK	
"	F2	GREEN	37	"	F2	GREEN	20		F2	GREEN	
"	SHIELD	WHITE	38	"	SHIELD	WHITE	21		SHIELD	WHITE	

WIRE LENGTH = 14" FOR ALL

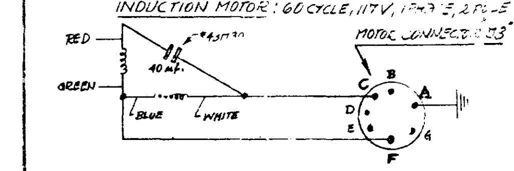
SHIELDED HEAD #12A4 (WIRE LENGTH = 14")



ASSEMBL HEAD WITH FLAT FACING TO THE LEFT.

3600 R.P.M.

INDUCTION MOTOR: 60 CYCLE, 117V, [illegible], 2 POLE



NOTES TO REVERSE ROTATION CHANGE BLUE + WHITE OR GREEN + RED

C	"X" + "Y" SELECTOR CHANGED PER CUSTOMER [illegible] (OPTION [illegible]) BY: H.DE. 4-2 -3
B	CLOCKS "C5" + "C6" TAKEN OUT PER CUSTOMER REQUEST. H.DE. [illegible] 23-63
A	THIS DWG. REPLACES W-45 BY: H.D. [illegible]

CHANGE RECORD
LETTER; DESCRIPTION; DATE; AUTHORIZATION

± .010 ALLOWED ON DIMENSIONS CONTROLLING FINISHED SURFACES UNLESS OTHERWISE SPECIFIED

DET. BY: H. DE[illegible]	DATE 2-21-63
C'K'D' BY: [illegible]	SCALE
MAT'L: —	REF. ASSEMBLY: 2A40 [illegible]

Vermont Research Corporation
SPRINGFIELD, VERMONT

DESC. WIRING SCHEDULE FOR D.E.C. OPTION #1, 2+3

NUMBER W-46 C

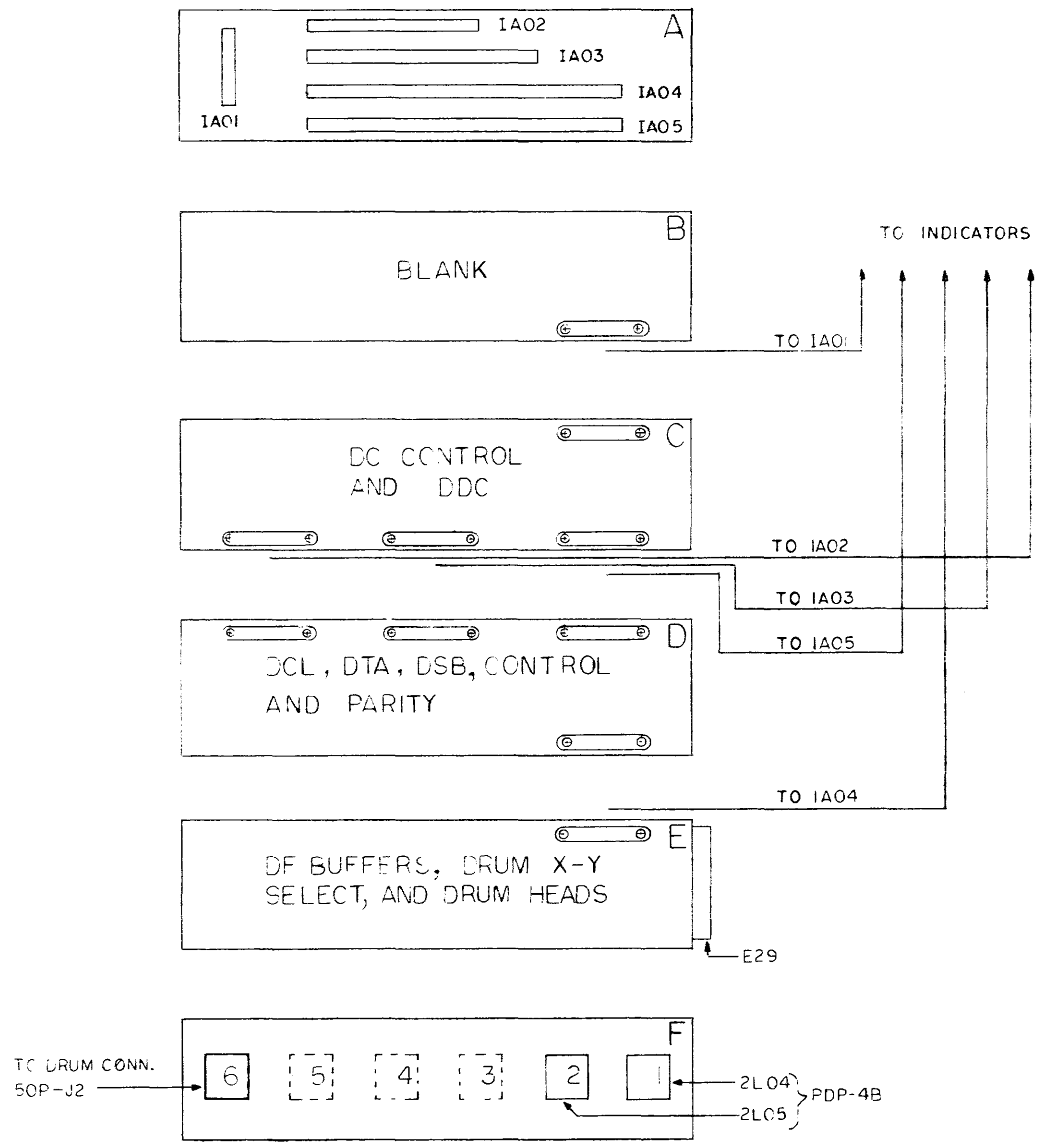
5-60 C-6418

Indicator Cable Breakout

D-24613

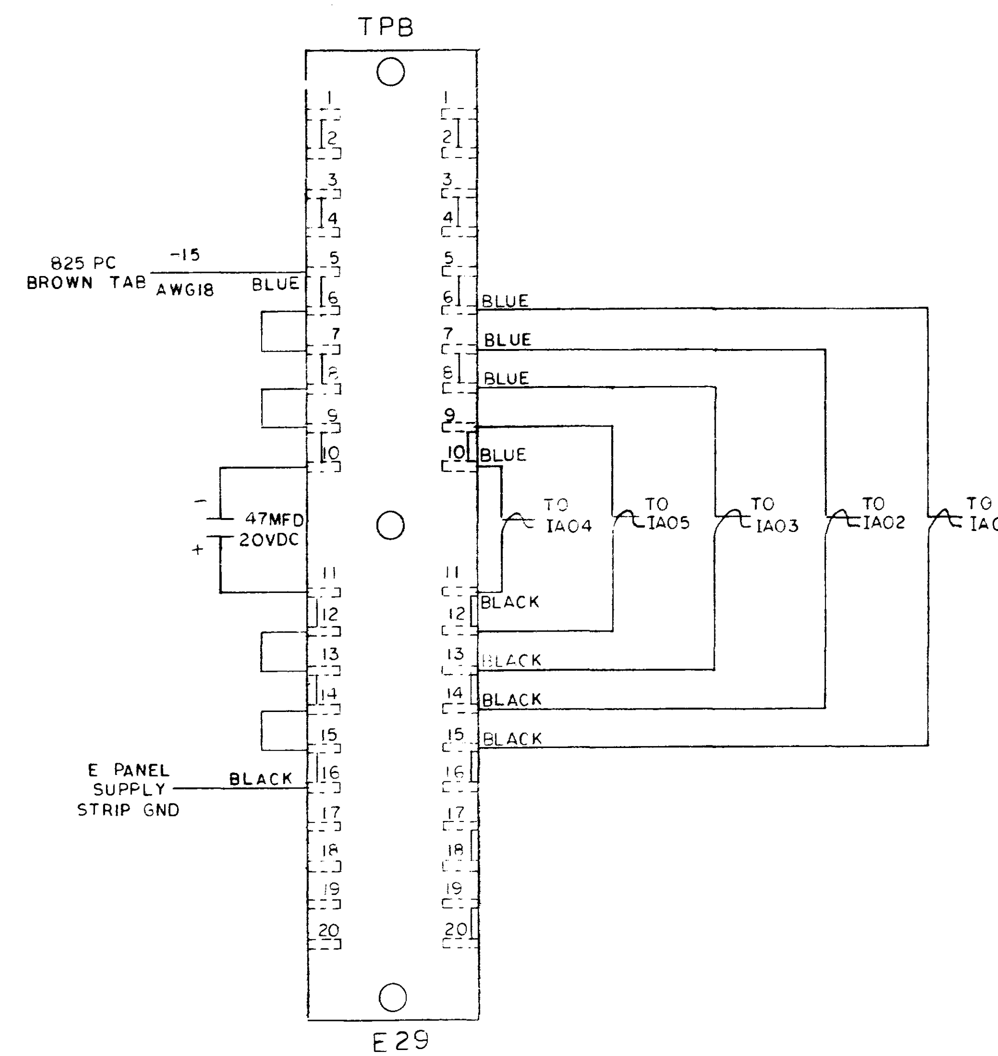
REAR VIEW

INDICATOR CABLE LOCATION



NOTE:

1. #18 CONNECTION TERMINAL STANDOFF BOARD
2. INDICATORS



NOTE:

AMPH TAPER PIN BLOCK E29 IS DEC STOCK 100A-480065-6

JACK	X	PLUG	
FEMALE	X	MALE	

LOCATION, LENGTH, ROUTE
F1

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
WHITE	F62E	1	DF^{0} → MB^{0}	WHITE	E04T	26	MBD7 → DF7
	F	2	1		M	27	8
	H	3	2		H	28	9
	J	4	3		E06H	29	10
	K	5	4		M	30	11
	L	6	5		T	31	12
	M	7	6		Y	32	13
	N	8	7		E08Y	33	14
	P	9	8		T	34	15
	R	10	9		M	35	16
	S	11	10		H	36	MBD17 → DF17
	T	12	11		E70L	37	DCL5 → MA5
	U	13	12		M	38	6
	V	14	13		N	39	7
	W	15	14		P	40	8
	X	16	15		R	41	9
	Y	17	16		S	42	10
	Z	18	DF17 → MB17		T	43	11
	E01T	19	MBD^{0} → DF^{0}		U	44	12
	Y	20	1		V	45	13
	E03H	21	2		W	46	14
	M	22	3		X	47	15
	T	23	4		Y	48	16
	Y	24	5	WHITE	E70Z	49	17
WHITE	E04Y	25	MBD^{0} → DF^{0}	BLACK	GND. LUG	50	GND.

DRAWN Anne Mullen 5-1-63

CHECKED R. Gould 5-3-63

ENG

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

APP'V

ECO. NO. REV. LTR.

50 PIN AMPHENOL

TITLE

SERIAL DRUM 24

F1 TO LOGIC

DRUM SIDE

DWG NO A-24614

REV. LTR.

SHEET 1 OF 5

CODE CL

Wire Run List (Cable connectors to Logic)

Sheet 1 of 5

A-24614

JACK [X] PLUG [ ]

FEMALE [X] MALE [ ]

LOCATION, LENGTH, ROUTE

F2

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
		1				26	
		2				27	
WHITE	D13L	3	ACB2 — DCL2			28	
	R	4	3			29	
	V	5	4			30	
	Z	6	5			31	
	D14Z	7	6			32	
	V	8	7			33	
	R	9	8			34	
	L	10	9	WHT	TA/PIN 1	35	TEMP SW (TA)
	D15L	11	10	BLK TWP	TA/PIN 2	36	TA GND
	R	12	11			37	
	V	13	12	RED	E PANEL +10 MC	38	+10 MC
	Z	14	13	WHT TWP	POWER SW REMOTE SIDE	39	REMOTE TURN ON
	D16Z	15	14	BRN	POWER SW LOCAL SIDE	40	REMOTE TURN ON
	V	16	15			41	
	R	17	16	GRY/BLK/TWP	E09Y	42	DATA REQ ANS
	L	18	ACB17 → DCL17		D01M	43	BEGIN
	C04Z	19	DRUM FLAG		C11X	44	T7B
	D17Z	20	$PE^{0} \cdot DE^{0}$		E09U	45	IOT 6002
	C12X	21	DATA REQ		D13F	46	IOT 6004
	C04N	22	DATA IN		D12E	47	IOT 6102
	E70H	23	DCL 2		D11Y	48	IOT 6104
	E70J	24	DCL 3	GRY/BLK/TWP	C06X	49	IOT 6204
WHITE	E70K	25	DCL4 → MA4	BLACK	GND LUG	50	GND

DRAWN Anne Mullen 5-1-63

CHECKED [illegible] 5-3-63

ENG [illegible]

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

APP'V

ECO. NO. REV. LTR.

50 PIN AMPHENOL

TITLE SERIAL DRUM 24 F2 DRUM SIDE

DWG NO A-24614

REV. LTR.

SHEET 2 OF 5

CODE CL

Wire Run List (Cable connectors to Logic)

Sheet 2 of 5

A-24614

JACK [X]	PLUG [ ]	LOCATION, LENGTH, ROUTE
FEMALE [X]	MALE [ ]	F-6

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
RED	E15 J	1	X0	RED	E21 J	26	X14
GREEN	↑ H	2	X0	GREEN	↑ H	27	X14
RED	↓ Y	3	X1	RED	↓ Y	28	X15
GREEN	E15 Z	4	X1	GREEN	E21 Z	29	X15
RED	E16 J	5	X2	RED	E22 J	30	X16
GREEN	↑ H	6	X2	GREEN	↑ H	31	X16
RED	↓ Y	7	X3	RED	↓ Y	32	X17
GREEN	E16 Z	8	X3	GREEN	E22 Z	33	X17
RED	E17 J	9	X4	BLACK	E11 E	34	Y0
GREEN	↑ H	10	X4	↑	↑ L	35	Y1
RED	↓ Y	11	X5		↓ R	36	Y2
GREEN	E17 Z	12	X5		E11 V	37	Y3
RED	E18 J	13	X6		E12 E	38	Y4
GREEN	↑ H	14	X6		↑ L	39	Y5
RED	↓ Y	15	X7		↓ R	40	Y6
GREEN	E18 Z	16	X7		E12 V	41	Y7
RED	E19 J	17	X10		E13 E	42	Y10
GREEN	↑ H	18	X10		↑ L	43	Y11
RED	↓ Y	19	X11		↓ R	44	Y12
GREEN	E19 Z	20	X11		E13 V	45	Y13
	SPARE	21			E14 E	46	Y14
RED	E20 J	22	X12		↑ L	47	Y15
GREEN	↑ H	23	X12		↓ R	48	Y16
RED	↓ Y	24	X13	↓	E14 V	49	Y17
GREEN	E20 Z	25	X13	BLACK	GND. LUG	50	GND.

DRAWN Anne Mullen 3/13/63

CHECKED [signature] 5-1-63

ENG [signature] 5/1/63

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

50 PIN AMPHENOL

TITLE SERIAL DRUM 24 HEAD SELECTION

NOTE: RED & GREEN ARE TWISTED PAIR.

APP'V

ECO. NO.

REV. LTR.

DWG NO A-24614

REV LTR.

SHEET 3 OF 5

CODE CL

Wire Run List (Cable connectors to Logic)

Sheet 3 of 5

A-24614

JACK [ ]	PLUG [X]	LOCATION, LENGTH, ROUTE
FEMALE [ ]	MALE [X]	J1, Drum Cabinet, To Logic

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
		1		RED	E25H	26	START
NOTE:		2		BLACK	E25E	27	C. TAP
INITALLY WIRE		3		WHITE	E25F	28	FINISH
CLOCK TRACK 1, PINS 18-		4		SHIELD	E25D	29	GND.
21, THEN SPARES AS		5				30	
NEEDED.		6		SPARE CLOCK TRACK		31	
ALWAYS INSULATE E25		7				32	
NOTE:		8				33	
PLUG END OF J1 MUST		9				34	
NOT BE CONNECTED WHILE		10		RED	E25H	35	START
WIRING.		11		BLACK	E25E	36	C. TAP
		12		WHITE	E25F	37	FINISH
		13		SHIELD	E25D	38	GND.
		14				39	
		15		SPARE CLOCK TRACK		40	
		16				41	
		17				42	
RED	E25H	18	START	RED	E25H	43	START
BLACK	E25E	19	C. TAP	BLACK	E25E	44	C. TAP
WHITE	E25F	20	FINISH	WHITE	E25F	45	FINISH
SHIELD	E25D	21	GND.	SHIELD	E25D	46	GND
		22				47	
CLOCK TRACK 1		23		SPARE CLOCK TRACK		48	
		24				49	
		25				50	

DRAWN Anne Mullen 5-1-63	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	50 PIN AMPHENOL
CHECKED H. [illegible] 5-3-63		TITLE SERIAL DRUM 24 CLOCK TRACK
ENG [illegible]	APP'V	
	ECO NO. REV. LTR.	DWG NO A-24614 — REV. LTR.
		SHEET 4 OF 5 — CODE CL

Wire Run List (Cable connectors to Logic)

Sheet 4 of 5

A-24614

COLOR	NAME	PIN	PIN	REMARKS
BLUE	LOCKOUT FIELD 0	E15L	FLO SW 0 NORM.	OPEN
	1	E15U	1	NOTE: Each Switch
	2	E16L	2	locks out (16X Posi-
	3	E16U	3	tions) x (256 Words)
	4	E17L	4	or 4096 Words.
	5	E17U	5	
	6	E18L	6	
	7	E18U	7	
	10	E19L	10	
	11	E19U	11	
	12	E20L	12	
	13	E20U	13	
	14	E21L	14	
	15	E21U	15	
	16	E22L	16	
BLUE	LOCKOUT FIELD 17	E22U	FLO SW 17 NORM.	OPEN
BLU/WHT	WRITE[1]	E10S	ALL FLO SW NORM.	CLOSED
WHITE	DCT $(PE^{o} \cdot DE^{o})$	D01Z	MAINT. SW NORM.	OPEN
WHITE	DCT $(PE^{o} \cdot DE^{o})$	D18Q	MAINT. SW COM.	
RED } TWP	POWER ON	825/TB1-2	POWER SW COM. ON	
WHITE }	POWER ON	825/TB1-1	POWER SW LOCAL ON	

DRAWN Anne Mullen 5-2-63

CHECKED A. Jushta 5-3-63

ENG

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

APP'V

ECO. NO. REV. LTR.

GENERAL WIRING SHEET

TITLE SERIAL DRUM 24 FIELD LOCK OUT SWITCH PANEL

DWG NO A-24614

REV. LTR.

SHEET 5 OF 5

CODE CL

Wire Run List (Cable connectors to Logic)

Sheet 5 of 5

A-24614

JACK [X]	PLUG [ ]	LOCATION, LENGTH, ROUTE	MARK
FEMALE [X]	MALE [ ]	33" LONG	1A01

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	B82H	A	TRA	PLUG USED TO CONNECT
W/BRN (Z)	B82J	B	ACT	THIS CABLE IS A 10
W/RED (R)	B82K	C	FLAG	PIN AMPHENOL.
W/ORN (O)	B82L	D	OVERFLOW	
W/YEL (Y)	B82M	E	REQUEST	
W/GRN (N)	B82N	F	PARITY ERROR	
W/BLU (B)	B82P	H	DATA ERROR	
	E29/6R	K	-15V	BLUE AND BLACK TWP ARE TO BE 53" LONG
	E29/15R	L	GND.	
				NOT USED

DRAWN Anne Mullen 3/12/63

CHECKED [signature] 5-2-63

ENG

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

10 PIN AMPHENOL

TITLE SERIAL DRUM 24

CONTROL LOGIC TO IND PANEL

APP'V

ECO. NO. REV. LTR.

DWG NO A-24617

REV. LTR.

SHEET 1 OF 5

CODE CL

Wire Run List (Logic to Indicator Panel)

Sheet 1 of 5

A-24617

JACK [X]	PLUG [ ]	LOCATION, LENGTH, ROUTE: 50" LONG	MARK: IA02
FEMALE [X]	MALE [ ]		

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)		A		
W/BRN (Z)		B		
W/RED (R)		C		
W/ORN (O)		D		
W/YEL (Y)		E		
W/GRN (N)	C98E	F	DTR 1 0	
W/BLU (B)	C98F	H	DTR 1 1	
W/VIO (V)	C98H	J	DTR 1 2	
W/GRY (G)	C98J	K	DTR 1 3	
WHT (W)		L		
W/BLK (X)	C98K	M	DTR 1 4	
W/BRN (Z)	C98L	N	DTR 1 5	
W/RED (R)	C98M	P	DTR 1 6	
W/ORN (O)	C98N	R	DTR 1 7	
W/YEL (Y)		S		
W/GRN (N)		T		
W/BLU (B)		U		
W/VIO (V)	B82F	V	READ	
W/GRY (G)	B82E	W	WRITE	
WHT (W)		X		
BLUE AND BLK TWP	E29/7R	Y	-15	
	E29/14R	Z	GND	

DRAWN Anne Malley 3-6-64

CHECKED [illegible] 5-3-62

ENG [illegible]

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

22 PIN AMPHENOL

TITLE SERIAL DRUM 24

DRUM TRACK ADDRESS TO 1ND PANEL

APP'V

ECO. NO. REV. LTR.

DWG NO A-24617

REV. LTR.

SHEET 2 OF 5

CODE CL

Wire Run List (Logic to Indicator Panel)

Sheet 2 of 5

A-24617

JACK [X]	PLUG [ ]	LOCATION, LENGTH, ROUTE	
FEMALE [X]	MALE [ ]	44" LONG	

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)		A		
W/BRN (Z)		B		
W/RED (R)	C90H	C	DCL $\overset{1}{2}$	
W/ORN (O)	C90J	D	DCL 3	
W/YEL (Y)	C90K	E	DCL 4	
W/GRN (N)	C90L	F	DCL 5	
W/BLU (B)	C90M	H	DCL 6	
W/VIO (V)	C90N	J	DCL 7	
W/GRY (G)	C90P	K	DCL $\overset{1}{8}$	
WHT (W)		L		
W/BLK (X)	C90R	M	DCL $\overset{1}{9}$	
W/BRN (Z)	C90S	N	DCL 10	
W/RED (R)	C90T	P	DCL 11	
W/ORN (O)	C90U	R	DCL 12	
W/YEL (Y)	C90V	S	DCL 13	
W/GRN (N)	C90W	T	DCL 14	
W/BLU (B)	C90X	U	DCL 15	
W/VIO (V)	C90Y	V	DCL 16	
W/GRY (G)	C90Z	W	DCL $\overset{1}{17}$	
WHT (W)		X		
BLUE AND BLACK TWP	E29/8 R	Y	-15V	
	E29/13 R	Z	GND	

DRAWN A. Mullen, 3-7-63

CHECKED [illegible]

ENG

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

22 PIN AMPHENOL

TITLE SERIAL DRUM TYPE 24

CORE LOCATION REGISTOR TO IND PANEL

APP'V | ECO. NO. | REV. LTR.

DWG NO A-24617 | REV. LTR.

SHEET 3 OF 5 | CODE CL

Wire Run List (Logic to Indicator Panel)

Sheet 3 of 5

A-24617

JACK [X]	PLUG [ ]	LOCATION, LENGTH, ROUTE	MARK
FEMALE [X]	MALE [ ]	38" LONG	1A05

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	C82E	A	DSB 0	
W/BRN (Z)	C82F	B	DSB 1	
W/RED (R)	C82H	C	DSB 2	
W/ORN (O)	C82J	D	DSB 3	
W/YEL (Y)	C82K	E	DSB 4	
W/GRN (N)	C82L	F	DSB 5	
W/BLU (B)	C82M	H	DSB 6	
W/VIO (V)	C82N	J	DSB 7	
W/GRY (G)	C82P	K	DSB 8	
WHT (W)		L		
W/BLK (X)	C82R	M	DSB 9	
W/BRN (Z)	C82S	N	DSB 10	
W/RED (R)	C82T	P	DSB 11	
W/ORN (O)	C82U	R	DSB 12	
W/YEL (Y)	C82V	S	DSB 13	
W/GRN (N)	C82W	T	DSB 14	
W/BLU (B)	C82X	U	DSB 15	
W/VIO (V)	C82Y	V	DSB 16	
W/GRY (G)	C82Z	W	DSB 17	
WHT (W)		X		
BLUE AND BLACK TWP	E29/9R	Y	-15V	
	E29/12R	Z	GND	

DRAWN Anne Mullen 5-6-63

CHECKED H. Yurlow 5-3-63

ENG

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

APP'V

ECO. NO. REV. LTR.

22 PIN AMPHENOL

TITLE SERIAL DRUM 24

SERIAL BUFFER REGISTER TO IND PANEL

DWG NO A-24617

REV. LTR.

SHEET 4 OF 5

CODE CL

Wire Run List (Logic to Indicator Panel)

Sheet 4 of 5

A-24617

JACK ☒	PLUG ☐	LOCATION, LENGTH, ROUTE	MARK
FEMALE ☒	MALE ☐	44" LONG	IA04

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	D82E	A	DFB $\overset{1}{0}$	
W/BRN (Z)	D82F	B	DFB 1	
W/RED (R)	D82H	C	DFB 2	
W/ORN (O)	D82J	D	DFB 3	
W/YEL (Y)	D82K	E	DFB 4	
W/GRN (N)	D82L	F	DFB 5	
W/BLU (B)	D82M	H	DFB 6	
W/VIO (V)	D82N	J	DFB 7	
W/GRY (G)	D82P	K	DFB $\overset{1}{8}$	
WHT (W)		L		
W/BLK (X)	D82R	M	DFB $\overset{1}{9}$	
W/BRN (Z)	D82S	N	DFB $1\overset{1}{0}$	
W/RED (R)	D82T	P	DFB $1\overset{1}{1}$	
W/ORN (O)	D82U	R	DFB 12	
W/YEL (Y)	D82V	S	DFB 13	
W/GRN (N)	D82W	T	DFB 14	
W/BLU (B)	D82X	U	DFB 15	
W/VIO (V)	D82Y	V	DFB 16	
W/GRY (G)	D82Z	W	DFB $1\overset{1}{7}$	
WHT (W)		X		
BLUE AND BLACK TWP	E29/10R	Y	-15	
	E29/11R	Z	GND	

DRAWN Anne Mullen 3-7-63	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	22 PIN AMPHENOL
CHECKED [illegible] 3-5-63		TITLE SERIAL DRUM 24 FINAL BUFFER TO IND PANEL
ENG		
APP'V		
ECO. NO. REV. LTR.		DWG NO A-24617 — REV. LTR.
		SHEET 5 OF 5 — CODE CL

Wire Run List (Logic to Indicator Panel)

Sheet 5 of 5

A-24617

APPENDIX 1

TELEPRINTER SUBROUTINES

The diagnostic test given as a corrective maintenance tool in Section 6 is for use with a PDP-4 computer which has the following standard subroutines stored in core memory. The routines allow automatic printing of test results on the Type 65 Printer-Keyboard. These routines are presented here to allow generation of a binary tape to store them in the PDP-4 if they are not present, or to allow comparison to determine the extent of modifications required in the diagnostic program to allow it to function with existing subroutines.

```
/teletype subroutines, octal and decimal fractional prints.
/turns interrupt off

/octal print, with zero suppression
/format                     lac wd
/                           twordz
/                           n              /n=number of digits to print from
                                           left end of word

octal
twordz=jms .
                            0
                            dac dcpnum
                            lac (sza)
                            dac twordz+17-jms
                            lac i twordz-jms
                            cma
                            dac dcpcnt
                            isz dcpcnt
                            isz twordz-jms
                            lac dcpnum
                            rtl
                            ral
```

```
                        dac dcpnum
                        ral
                        and (7)
                        sza             /modified
                        jmp twordz+25-jms
                        isz dcpcnt
                        jmp twordz+11-jms
                        tdigit
                        jmp i twordz-jms
                        dac dcpdig
                        lac (jmp twordz+31-jms)
                        dac twordz+17-jms
                        lac dcpdig
                        tdigit
                        isz dcpcnt
                        jmp twordz+11-jms
                        jmp i twordz-jms

/octal print, no zero suppression
/format same as twordz

tword=jms .
                        0
                        dac dcpnum
                        lac tword-jms
                        dac twordz-jms
                        lac (jmp twordz+31-jms)
                        jmp twordz+3-jms

/table for octal to decimal conversion
decimal
dcptab,                 100000  10000  1000  100  10  1
octal
/teletype output package 0-1  9-26-62
```

```
ext=jmp i-jms          ttab=10

/type 1 character from AC bits 12-17

ty1=jms   .
                                0
                                rar
                                jms ty1a
                                ext ty1

/type 1 character (5 bit), Link indicates case

ty1a,                           0
                                dac temy
                                and (37
                                sna
                                jmp ty2
                                lac ocl
                                spl
                                lac ocu
                                sad ocs
                                jmp . 3
                                jms oty
                                dac ocs
                                lac temy
                                jms oty
                                isz tbc
ty2,                            lac temy
                                jmp i ty1a

/type 3 characters from AC 0-5, 6-11, 12-17 respectively

ty3=jms   .
                                0
                                jms r16
                                jms ty1a
```

```
                jms r16
                jms ty1a
                jms r16
                jms ty1a
                ext ty3

/type a carriage return, and line feed

tcr=jms   .
                0
                law 2
                jms oty
                law 10
                jms oty
                dzm tbc
                ext tcr

/teletype output package - page 2

/type a space

tsp=jms   .
                0
                law 4
                jms oty
                isz tbc
                ext tsp

/type a tabulation

tyt=jms   .
tab=tyt
                0
                lac tbc
                add (-ttab-1
                sma
                jmp .-2
```

```
        add (1
        sma
        lac (-ttab-1
        add (-1
        dac tem
        tsp
        isz tem
        jmp .-2
        ext tyt

/typewriter initialize

tin=jms   .
        0
        lac ocl
        dac ocs
        jms oty
        tcr
        ext tin

/type the digit in the AC

tdigit=jms   .
        0
        and (17
        add (lac nct
        dac . 1
        xx
        ty1
        ext tdigit

/teletype output package - page 3

/type a string of characters

tsr=jms   .
        0
```

```
        dac temy1
        lac (jmp tsr1
        dac ty1a 4
        lac i temy1
        ty3
        isz temy1
        jmp .-3
tsr1,   lac (jmp ty2
        dac ty1a 4
        lac temy1
        ext tsr
/output one five bit character
oty,    0
        iof
        dac tword-jms     /save
        law               /counter
        dac rl6
        lac tword-jms
        tsf
        skp
        jmp .+3
        isz rl6
        jmp .-4
        tls
        jmp i oty
/rotate left 6
rl6,    0
        rtl
        rtl
        rtl
        jmp i rl6
```

```
/table of digits

nct,                33   73   63   41
                    25   3    53   71
                    31   7

/case storage

ocu,                33
ocl,                37
ocs,                0

/decimal fractional print subroutine
/uses teletype output package
/suppresses unnecessary zeros
/format             lac number
/                   decfr
/                   x                  /number of decimal places (0-6)
decfr=jms   .
                    0
                    smaVccl
                    cmaVcll            /make word negative
                    dac dcpnūm
                    law char r         /space
                    szl
                    law char r-        /minus
                    ty1
                    lac (add dcptab)
                    dac decfr1+2
                    lam -5
                    dac dcpcn̄t
                    lac i decfr-jms
                    isz decfr-jms
                    add .-4            /-5
                    dac dcpcn̄1
```

```
                 sma
                 jmp decfr6          /write initial zero
                 lac (sza)
                 dac decfr2
                 dzm dcpdig          /value counter
                 lac dcpnum
                 jmp .+3
decfr1,          dac dcpnum
                 isz dcpdig
                 add dcptab          /modified
                 spa
                 jmp decfr1
                 isz decfr1+2
                 lac dcpdig
decfr2,          sza                 /modified to jmp decfr3
                 jmp decfr3
                 isz dcpcn1
                 jmp decfr5
                 clc
                 dac dcpcn1
                 cla
decfr3,          tdigit
                 isz dcpcnt
                 skp
                 jmp i decfr-jms
decfr4,          lac decfr2+1
                 isz dcpcn1
                 jmp decfr1-4
                 law char r.         /period
                 ty1
                 jmp decfr4
decfr5,          isz dcpcnt
```

```
                jmp decfr1-2
                tdigit          /should never reach here
                jmp i decfr-jms
decfr6,         cla
                tdigit
                jmp decfr4+3
start
```