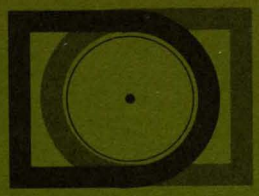


DATA DISC
INCORPORATED

Display Division

FPD Disc-Memory System
INPUT/OUTPUT MANUAL

Section 1
Summary Specifications

DISC SPEED

1800 RPM $^{+1.3\%}_{-3\%}$
Hysteresis-Synchronous Motor

DATA RATE

3.0 Mbps per track

DATA CAPACITY

100,000 bits per track
(Tracks can be added in increments of 8, up to 64.)

INPUT/OUTPUT LEVELS

0 and +5V TTL integrated-circuit interface (+5V Power Supply TI Series 74)

TEMPERATURE

Operating	50^{o}F to 105^{o}F; less than 20^{o}F change per hour
Non-Operating	-20^{o}F to $+130^{o}$F

ATMOSPHERE

Corrosive atmospheres such as those found in steel and chemical plants are not permitted.

VIBRATION

Floor vibration of 0.15 g's max. from 10 to 65 Hz. The disc package shall not be damaged by 5 g's or less of shock in any axis.

A-C POWER

120 volts $\pm$10%, 60 $^{+0.5}_{-1.5}$Hz, single phase, 8.2 amperes starting (10 sec.); 2.6 amperes running

SIZE & WEIGHT

10-1/4 X 19 X 19-3/4 inches; 90 pounds. Shipping weight is 135 pounds.

Section 2
General Description

2.1 ELECTRICAL

The FPD-Series Fixed-Head Parallel-Digital Disc Memory System has a 12-inch disc which can contain as many as 64 data tracks with up to 100,000 bits on each track. This disc rotates at 1,800 RPM to provide a maximum bit rate of 3-million bits per second.

The FPD unit is designed for buffer-storage applications. Because the FPD unit uses synchronous clocking from a clock track, it is recommended only for buffer storage applications. The time stability between tracks cannot be guaranteed for long periods of time. Where Data is to be stored for an indefinite period, the DATA DISC F6 Disc Memory System should be employed.

Each track is complete with a read/write head and all electronics to perform the following functions, as diagrammed in Figures 2-1 and 2-2:

Encode Data	Decode Data
Write Data	Re-Clock Data
Read Data	

Any number of tracks may be written or read in parallel because each has a clocked flip-flop output. The standard write-amplifier power supply will accommodate 10 write amplifiers in parallel. Larger supplies can be provided where it is necessary to write on more than 10 tracks simultaneously. Power and input/output connectors are on the rear of the unit, Figure 2-5.

2.2 MECHANICAL

The cast-aluminum disc-module chassis is shock-mounted within the rackmount tray. The chassis includes the heads, 12-inch disc and read/write electronics.

FPD Series units are 10-1/2 inches high and 19-3/4 inches deep (not including space for cable breakout) and are designed for mounting into standard 19-inch-wide racks or rack cabinets. Power supplies are mounted at the back of the rackmount tray. See Figure 2-5.

2.3 SYSTEM APPLICATION

The FPD unit is designed so that each track on the disc is a complete channel. A high-speed processor can access each track and update the data stored on any track. Where data rates higher than 3-million bits per second are needed, several tracks can be combined to form the data buffer. For example, data read from four channels may be loaded into a four-bit shift register and a 4X clock used to shift the data into the output channel at a 12-million-bit rate. Other bit rates may be achieved by using similar combining techniques. See Figure 2-3.

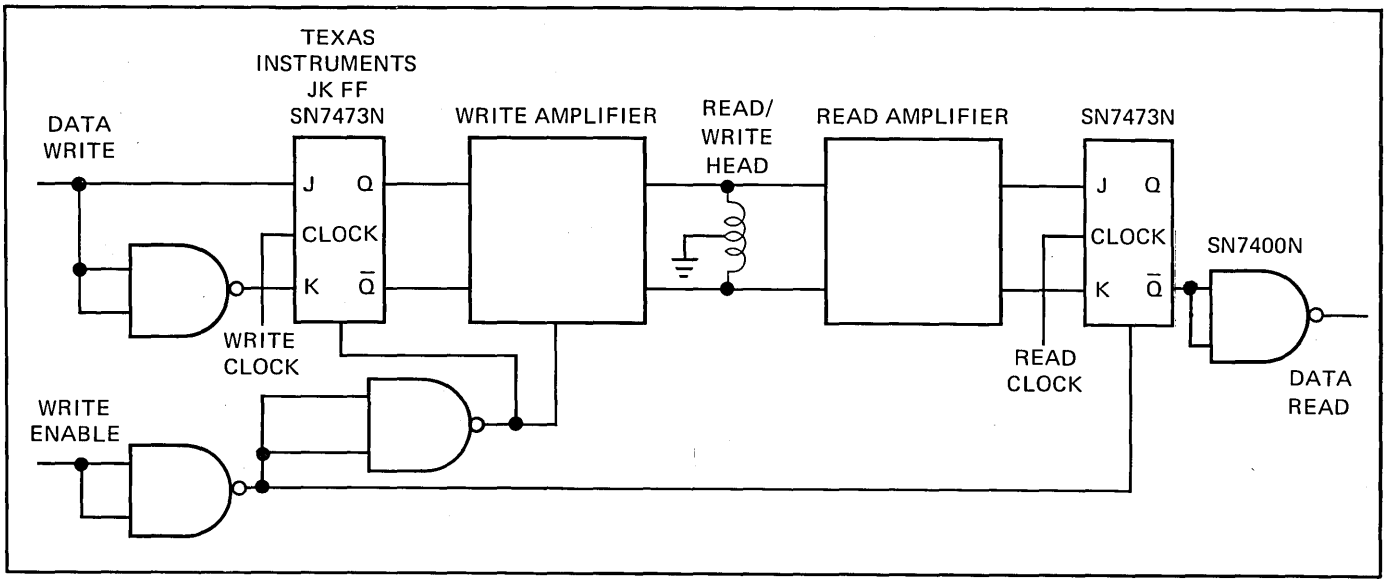


Figure 2-1 Read/Write Module

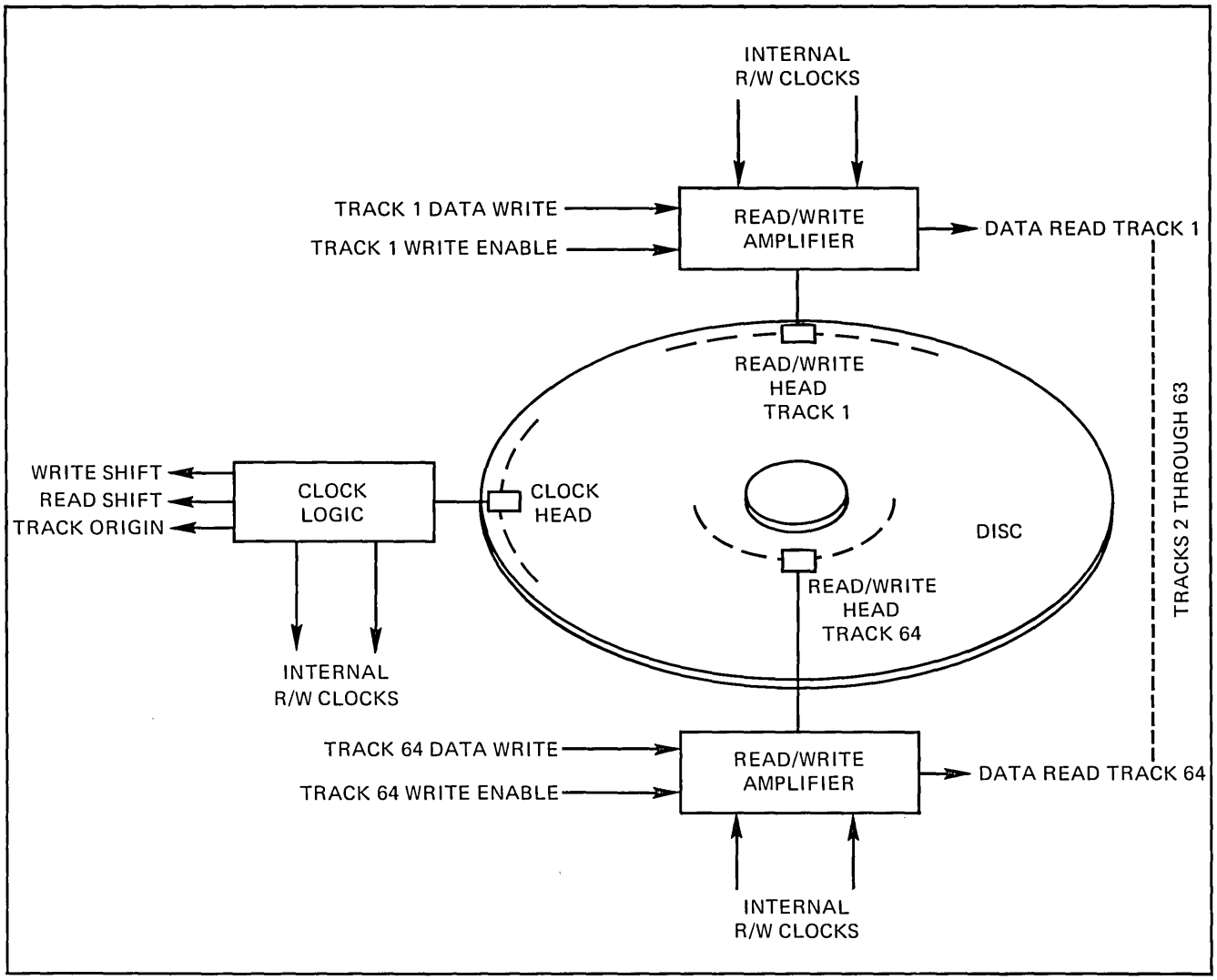


Figure 2-2 FPD Disc Memory System Block Diagram

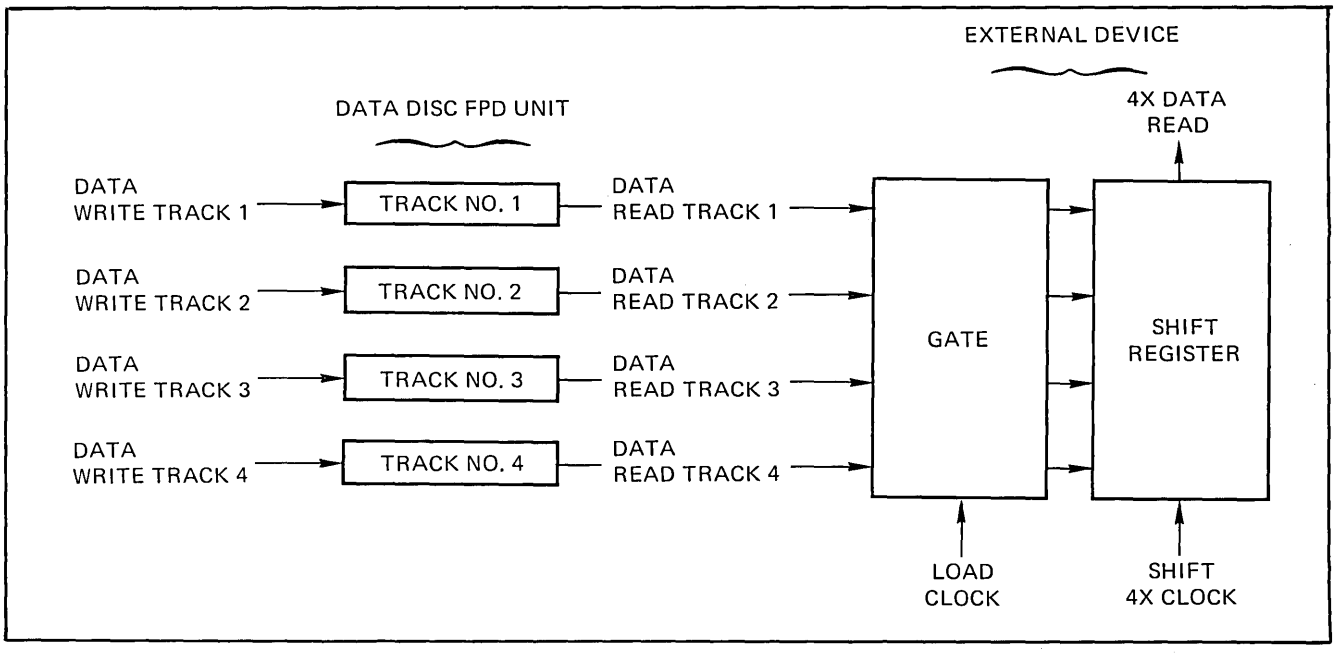


Figure 2-3 Four Tracks Read in Parallel and Serialized at a 4X Rate

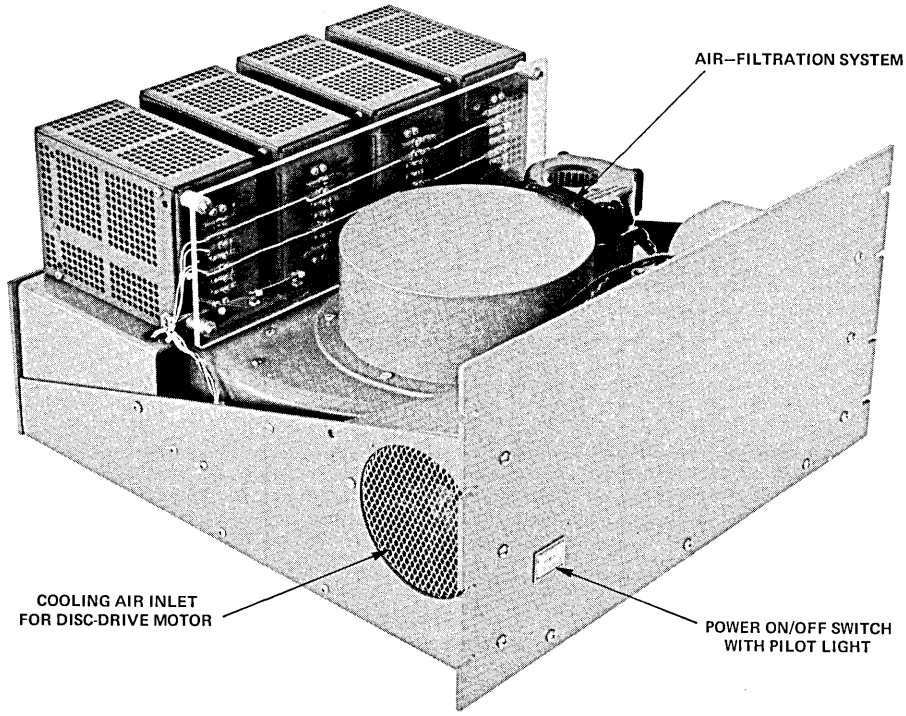


Figure 2-4 FPD Disc Memory System, Front View

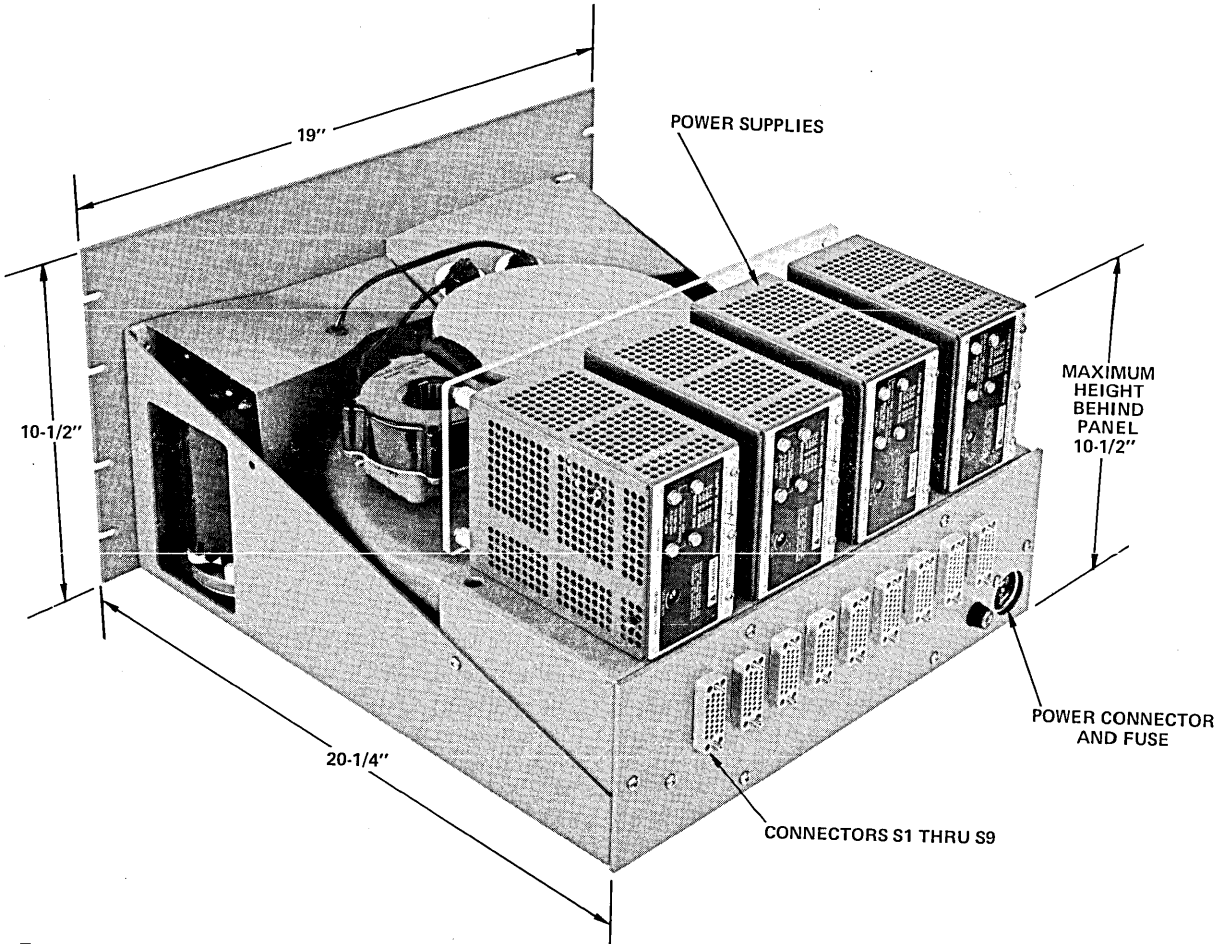


Figure 2-5 FPD Disc Memory System, Rear View

Section 3
Input/Output Details

3.1 INPUT/OUTPUT LINES

Each track has three input/output lines that connect to the external device via an I/O Cable as described in Figure 3-1. The FPD unit uses Texas Instruments Series SN7400N and SN7473N TTL Integrated Circuits.

3.2 INPUT CONNECTORS

Eight 66-pin connectors are provided, each serving eight heads. The use of 16 heads requires two connectors, etc. All eight connectors (S1 through S8) are required when 64 heads are used. See Table 2 which also indicates the function served by each pin on each connector, and the tracks served by each.

3.3 CLOCKS

Five clocks, all derived from one clock track, are available in the standard FPD system. Two are used internally, and the other three are for use at the interface. The three interface clocks are the Track Origin (once per revolution), Write Shift and Read Shift (Figure 3-2 and Table 3).

The Write Shift Clocks are used to change the state of the Data Write line and are counted down to indicate angular position of the disc.

The Track Origin clock is derived from the four-bit gap in the clock track and is used to indicate the zero-degree position of the disc and as a reset for any counters used to identify other angular positions.

A second clock track can be provided as an option.

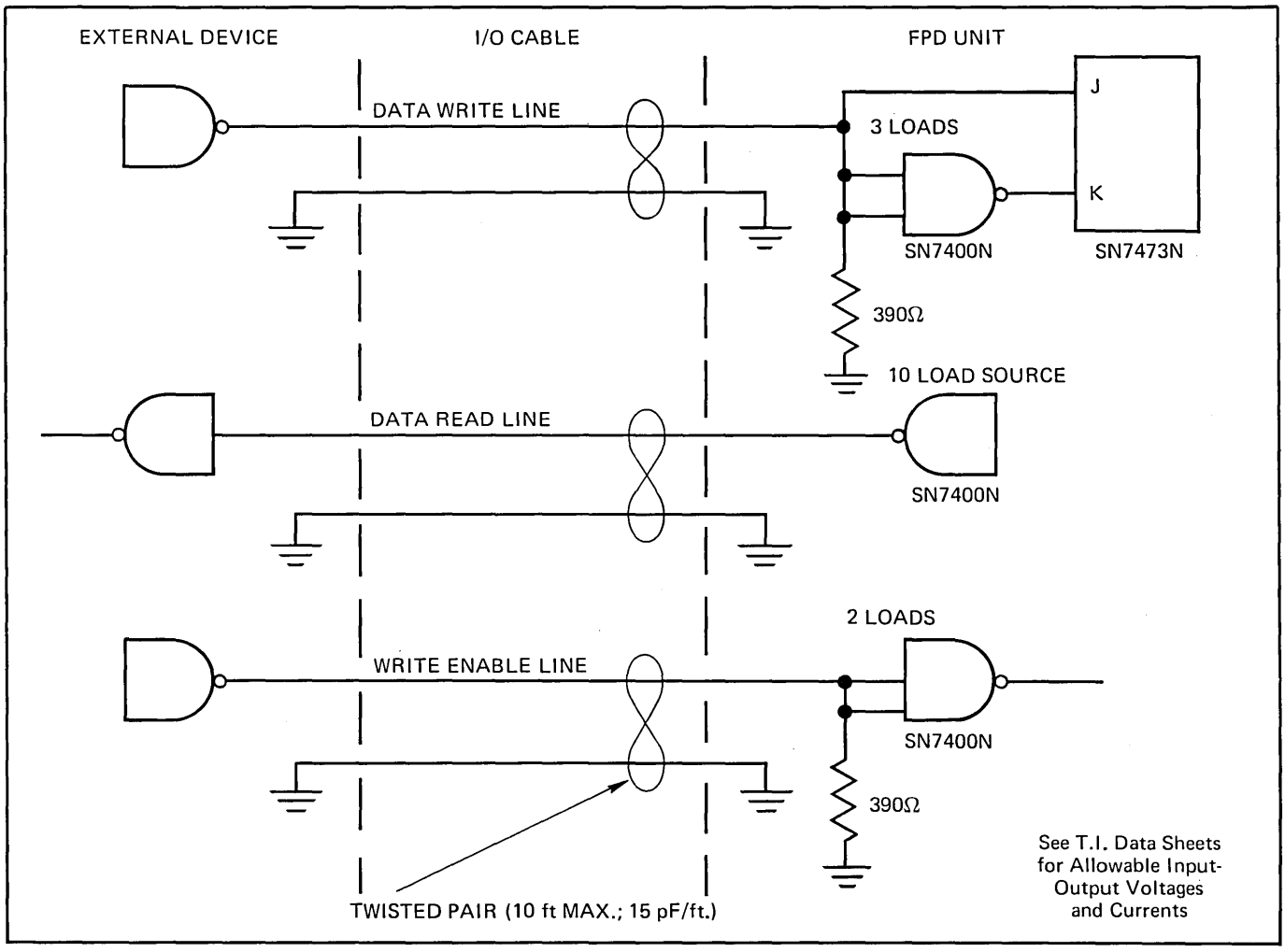


Figure 3-1 Input/Output Circuits

FPD units are supplied with factory-written clocks. However, if new clocks are to be written, the Clock Write Enable lines can be accessed as detailed in Table 4.

3.4 CLOCK CONNECTOR S9

S9 is a 66-pin used only by the clock tracks. See Table 4 for pin assignments.

Table 1
Data Input/Output Lines

Data Write 1 thru 64:

An input line that is driven from the output of an external flip-flop that is clocked by Data Write Shift Clock.

Write Enable 1 thru 64:

The Write Enable line going high will cause the data on the corresponding Data Write line to be written on the track. As long as the Write Enable line is high, writing will continue.

Data Read 1 thru 64:

Each Data Read line is the buffered output of a clocked flip-flop. The Data Read is delayed from Data Write and may be shifted into an external register by using the negative-going edge of the Data Read Shift Clocks or the negative-going edge of the Write Shift Clock may be used. See Timing Diagram Figure 3-2. During Write the output of the Data Read line is held low.

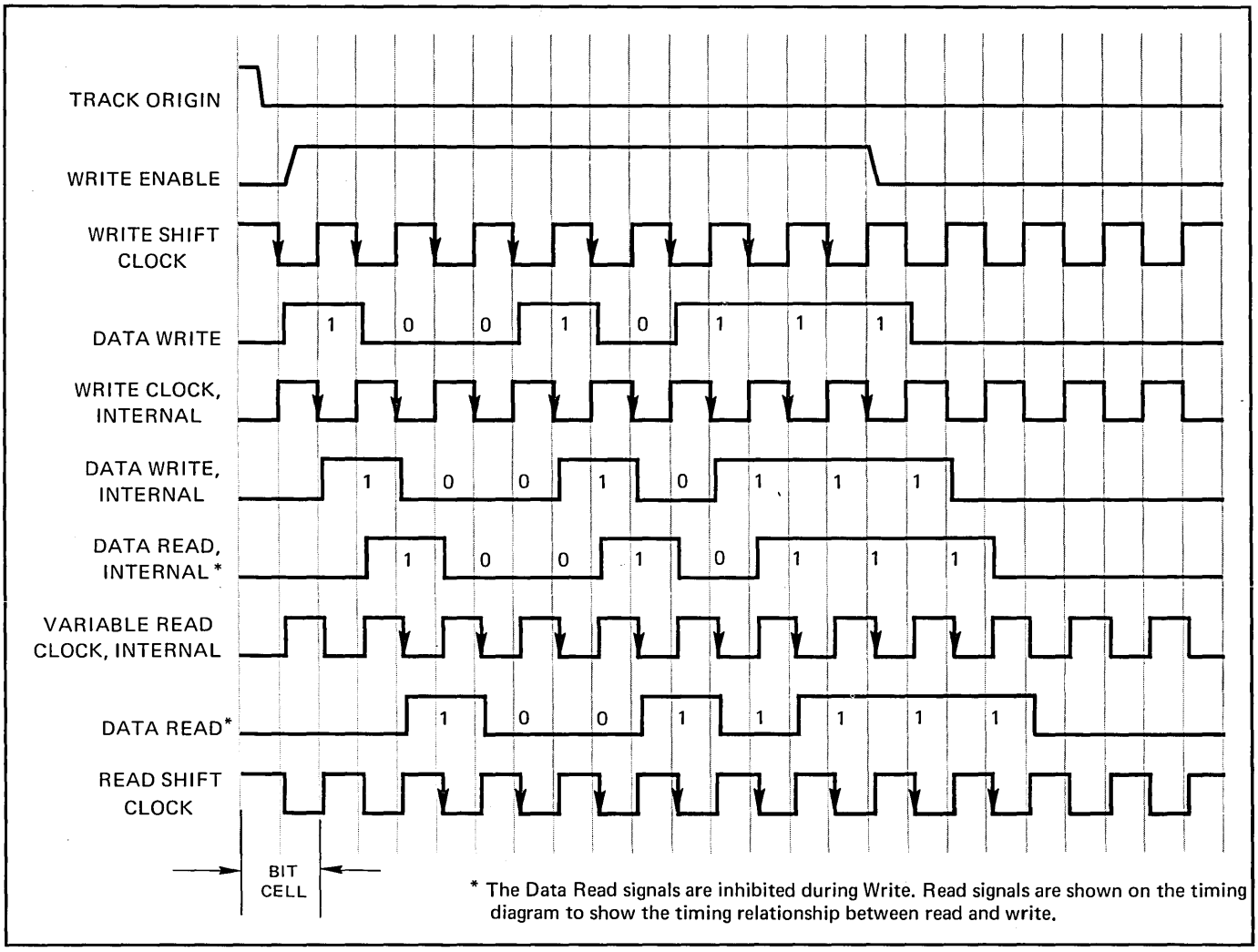


Figure 3-2 Timing Diagram

Table 2
Pin Assignment
66-pin I/O Connectors S1–S8

Pin No.	Function	Connectors S1	S2	S3	S4	S5	S6	S7	S8
		Tracks							
1*	Data Write								
2	Data Write Ground								
3	Write Enable	1	9	17	25	33	41	49	57
4	Write Enable Ground								
5	Data Read								
6	Data Read Ground								
7	Data Write								
8	Data Write Ground								
9	Write Enable	2	10	18	26	34	42	50	58
10	Write Enable Ground								
11	Data Read								
12	Data Read Ground								
13	Data Write								
14	Data Write Ground								
15	Write Enable	3	11	19	27	35	43	51	59
16	Write Enable Ground								
17	Data Read								
18	Data Read Ground								
19	Data Write								
20	Data Write Ground								
21	Write Enable	4	12	20	28	36	44	52	60
22	Write Enable Ground								
23	Data Read								
24	Data Read Ground								
25	Data Write								
26	Data Write Ground								
27	Write Enable	5	13	21	29	37	45	53	61
28	Write Enable Ground								
29	Data Read								
30	Data Read Ground								
31	Data Write								
32	Data Write Ground								
33	Write Enable	6	14	22	30	38	46	54	62
34	Write Enable Ground								
35	Data Read								
36	Data Read Ground								
37	Data Write								
38	Data Write Ground								
39	Write Enable	7	15	23	31	39	47	55	63
40	Write Enable Ground								
41	Data Read								
42	Data Read Ground								
43	Data Write								
44	Data Write Ground								
45	Write Enable	8	16	24	32	40	48	56	64
46	Write Enable Ground								
47	Data Read								
48	Data Read Ground								

*All signal leads twisted with ground.
P1 thru P8: Mating connector supplied with unit.
Winchester MRAC 66PJTC6H.
Each connector serves eight tracks.

Table 3
Clock Output Lines

Data Write Shift Clock:

A 3-million bit per second clock with 4 clocks missing at Track Origin time. The negative-going edge is used for changing state of Data Write lines.

Data Read Shift Clock:

The negative-going edge is used for sampling the center of Data Read. The center of Data Read is delayed 2 bit times from the leading edge of Data Write. The sample caused by Data Read Shift Clocks will be delayed approximately two bit times relative to Data Write.

Track Origin Clock:

A once-per-revolution clock used to reset counters, etc.

Clock No. 1 Write Line:

A data input line for writing clocks. This line should be grounded except when writing a clock track.

Clock No. 1 Write Enable Line:

Taking this line positive will enable writing in the clock track. No connections should be made to this line except when writing clocks. See note on Table 4.

Clock No. 2 Read Line (option):

The output of the second clock track read amp.

Clock No. 2 Write Line (option):

A data input line for writing clocks. This line should be grounded except when writing a clock track.

Clock No. 2 Write Enable (option):

Taking this line positive will enable writing a clock track. No connections should be made to this line except when writing clocks. See note on Table 4.

Table 4
Pin Assignment
66-pin Clock Connector S9*

Pin No.		Function
1	**	Write Shift Clock
2		Ground
3		Read Shift Clock
4		Ground
5		Track Origin Clock
6		Ground
7		Clock #1 Write Line
8		Ground
9	***	Clock #1 Write Enable Line
10		Ground
11		Disc Ready
12		Ground
13		Clock #2 Read Line (option)
14		Ground
15		Clock #2 Write Line (option)
16		Ground
17	***	Clock #2 Write Enable (option)
18		Ground
19 - 66		Unassigned

*Supplied with mating connector, Winchester MRAC 66PJTC6H.

**All signal leads twisted with ground.

***These pins (9 and 17) are not inserted into the connector block. Connector S9 must be pulled away from the rear panel to gain access to these pins for writing clocks.

Section 4
Operation

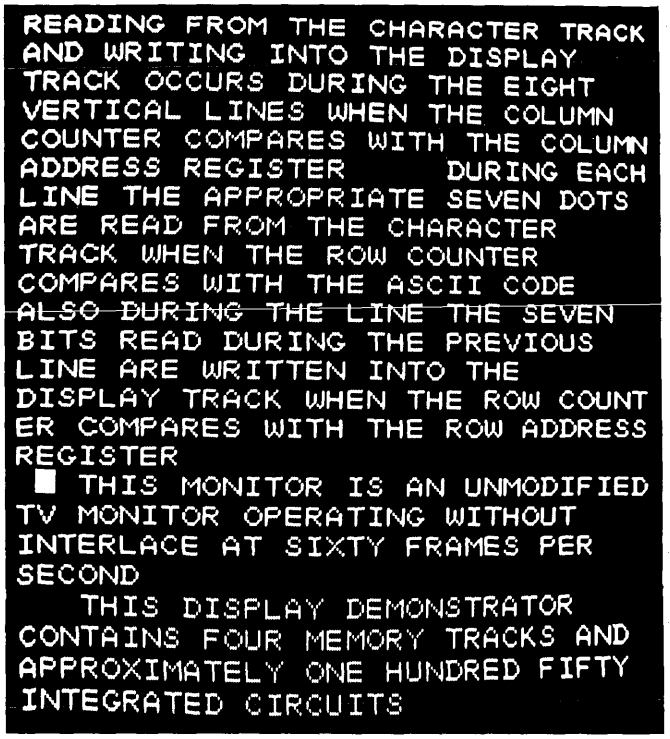
4.1 WRITE

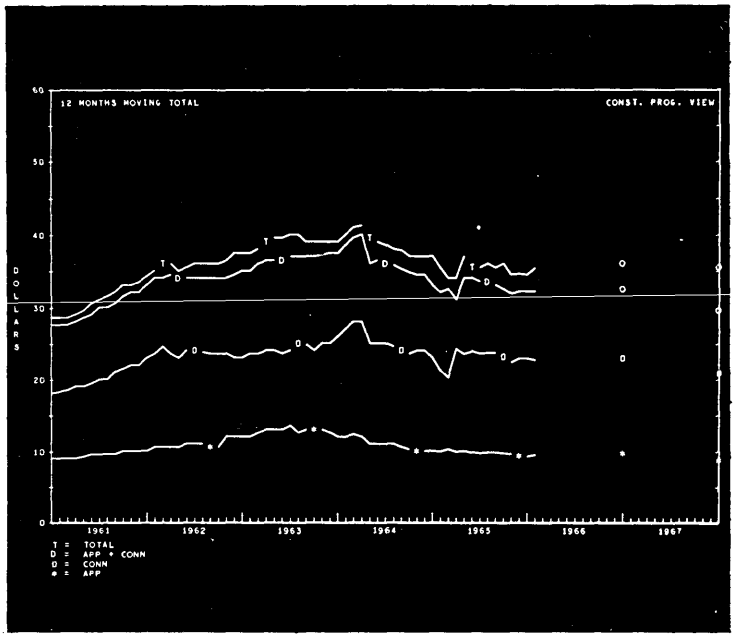
To write, the first bit of data is placed on the Data Write line and at the correct angular position the Write Enable line is raised and writing begins. Each negative-going transition of the Write Shift clock is used by the external device to transfer another data bit onto the Data Write line. The turn on of the Write Enable should occur at no later than 100 nanoseconds from the negative-going edge of a Write Shift clock.

Write Enable should be turned off at the next positive-going clock transition following the last shift clock as shown in the timing diagram, Figure 3-2.

4.2 READ

During Write the Data Read line is held low but at all other times, any data on the track will be clocked out to the Data Read line. The data may be transferred from the Data Read line to an external device at the negative-going edge of the Read Shift Clock.





Left: Photo of TV raster-scan alpha-numeric display where dot pattern is stored on a single FPD track. Above: Photo of X-Y scope being driven from X-Y data stored on one data track.

DATA DISC
INCORPORATED
1275 CALIFORNIA AVENUE
PALO ALTO, CALIFORNIA 94304
TELEPHONE 415 326-7602
Display Division

PRICE SCHEDULE

F-SERIES PARALLEL DIGITAL DISC MEMORY SYSTEM (FPD)

PRODUCT DESCRIPTION

Unit consists of mechanical assembly (including disc), heads (one per track or channel) with read-write-clocking module, standard clock channel, and power supply. The number of channels required will dictate the model number ordered. Channels are added in increments of eight.

PRICING:

	Unit		Unit
FPD-8 -	$ 7,270	FPD-48 -	$19,270
FPD-16 -	9,670	FPD-56 -	21,670
FPD-24 -	12,070	FPD-64 -	24,070
FPD-32 -	14,470	FPD-72 -	26,470
FPD-40 -	16,870		

Double-loop Servo Drive Unit: $ 3,900
(Syncs to external TV signal)

DELIVERY: First unit: 30 days ARO; subsequent units at 2-week intervals thereafter.

TERMS: ½% 10 days, net 30 days, F.O.B. Palo Alto, California.

Prices are subject to change.

FOR FURTHER INFORMATION: Call Bill Stevens: (415) 326-7602

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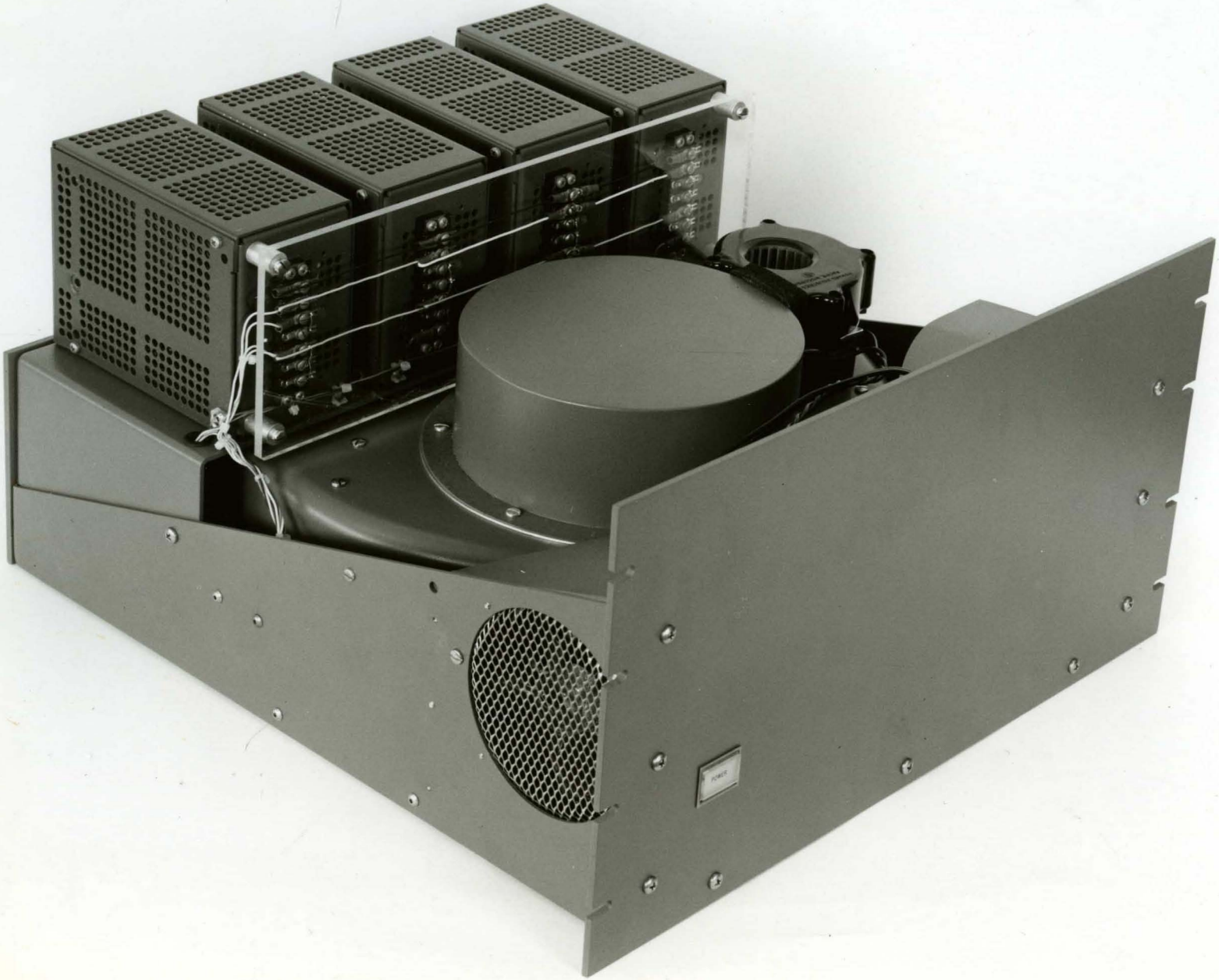
POWER