Workstation Hardware

First Edition Revised, Update Notice 6
A-09-00243-01-A

The attached pages update: (1) edition A-09-00016-01-A and Update Notices A-09-00058-01-A, A-09-00066-01-A, A-09-00091-01-A, A-09-00177-01-A, and A-09-00228-01-A or (2) edition A-09-00016-01-B and Update Notices A-09-00066-01-A, A-09-00091-01-A, A-09-00177-01-A, and A-09-00228-01-A of the Workstation Hardware Manual.

Insert these pages according to the collating instructions on the inside of this cover.

Updated pages are indicated by a date at the bottom of the page.

Throughout this Update Notice, change bars in the margins indicate technical additions and changes. Asterisks indicate deletions. Editorial changes are not identified. All changes will be incorporated into the next editions of this manual.

Insert this page after the title page of your manual to provide a record of this Update Notice.

Convergent Technologies

COLLATING INSTRUCTIONS

VOLUME 1: Sections 1 - 9

Delete	Replace with
iii to xi	iii to xi
1-3, 1-4	1-3, 1-4
1-9	1-9, 1-10
2-25, 2-26	2-25, 2-26
2-109, 2-110	2-109, 2-110
9-5, 9-6	9-5, 9-6

Place the seven foldout pages (schematic) of the 64K I/O-Memory board at the end of Section 5. (Do not delete the existing schematics.)

VOLUME 2: Sections 10 - 14
Glossary
Appendixes A - G

Delete		Replace with
iii to vi		iii to vi
12-7		12-7
D-1, D-2	(Appendix C)	D-1, D-2, D-2.1
D-7		D-7
E-1	(Appendix D)	E-i to E-iii, E-1 to E-101
F-1	(Appendix E)	F-i, F-ii, F-1 to F-72

DESCRIPTION OF CHANGES

Revisions include changes in Chapter 2 and Appendix C for the 64K I/O Memory board. Other revisions include a minor change to Chapter 9 and revised Figures 1-1, 1-4, and 12-2.

Appendix D contains a description of the monitor form of the IWS workstation and includes information about custom Multibus applications.

Appendix E contains a detailed software description of the four bootstrap ROMs available for the IWS workstation.

CONTENTS: Volume 1

LIST OF FIGURES

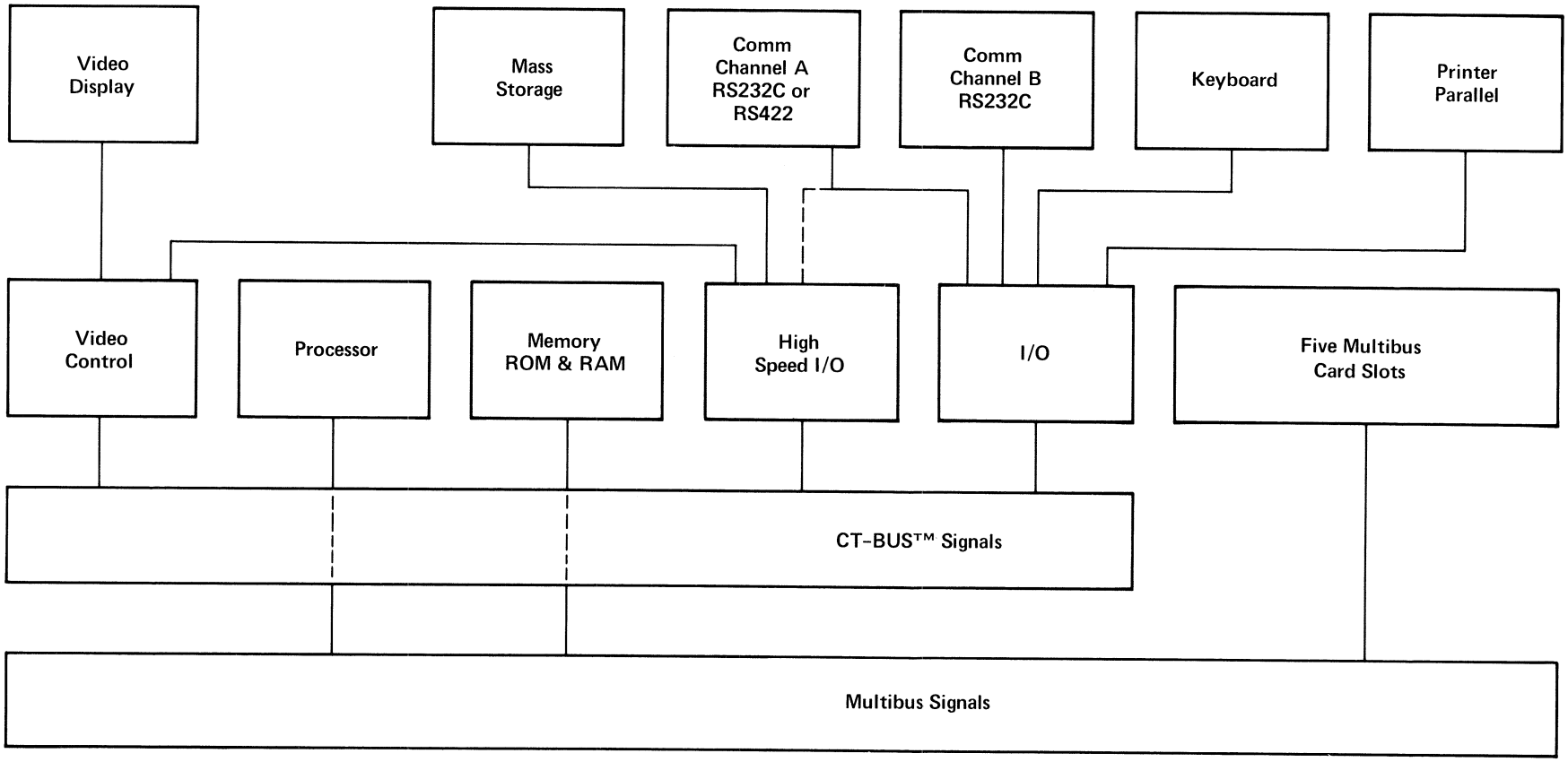
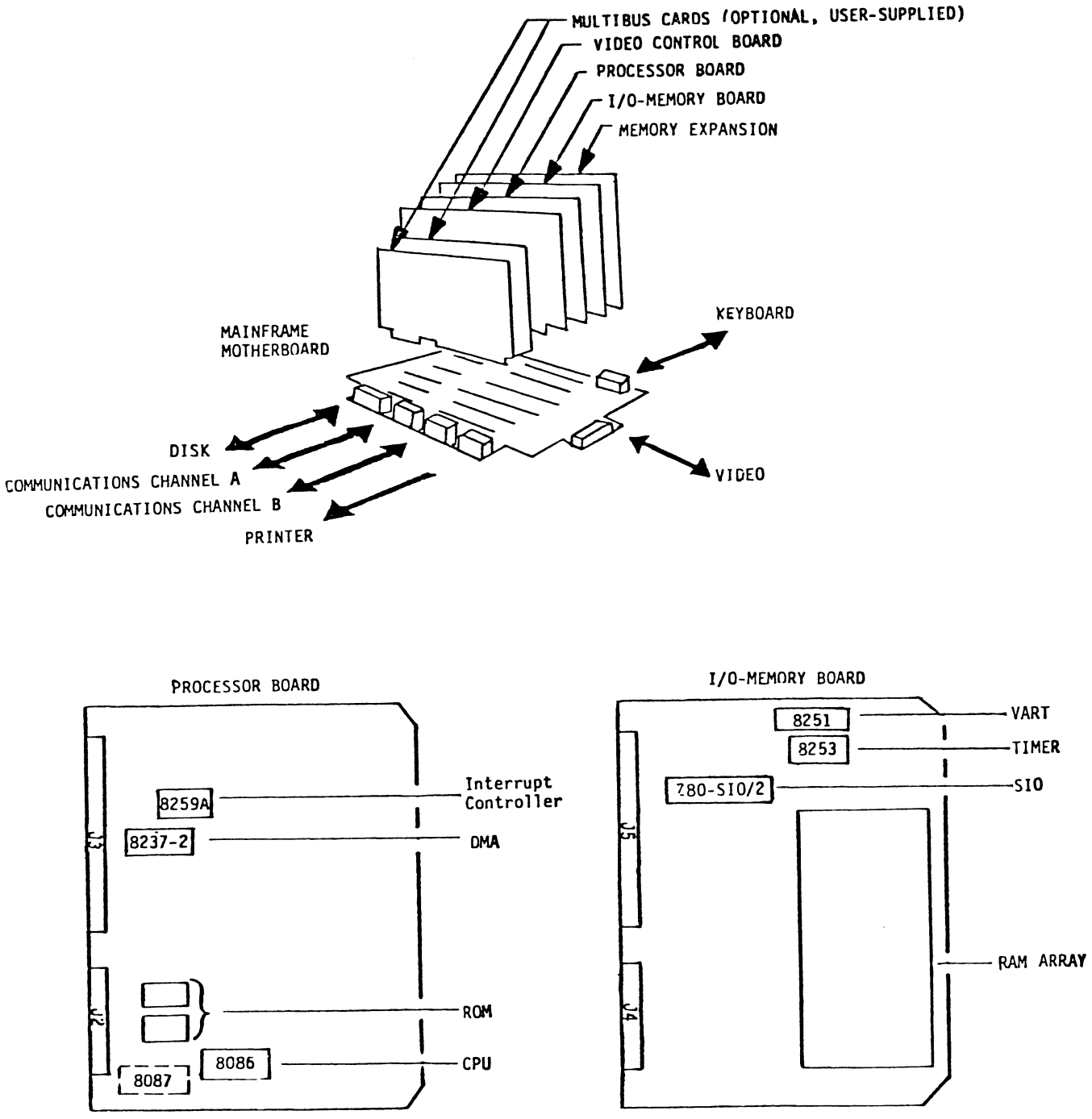


Figure 1-1. Workstation System Overview



Note: Device nomenclature corresponds to Intel device codes with the exception of the SIO which is a Zilog Code. The manufacturer actually used may vary.

Figure 1-2. Workstation Mainframe

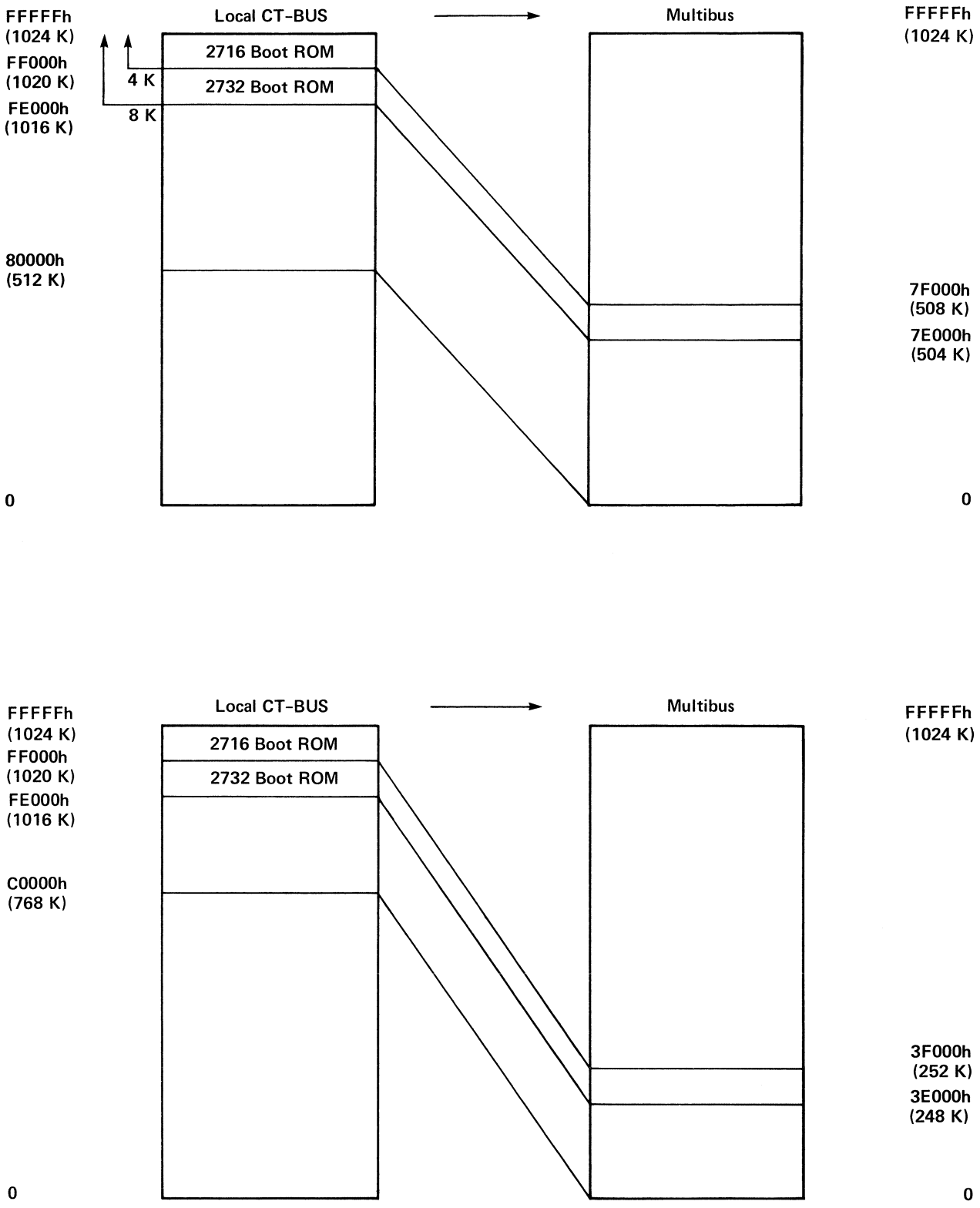


Figure 1-4. Memory-Mapping Between the Local Bus and Multibus

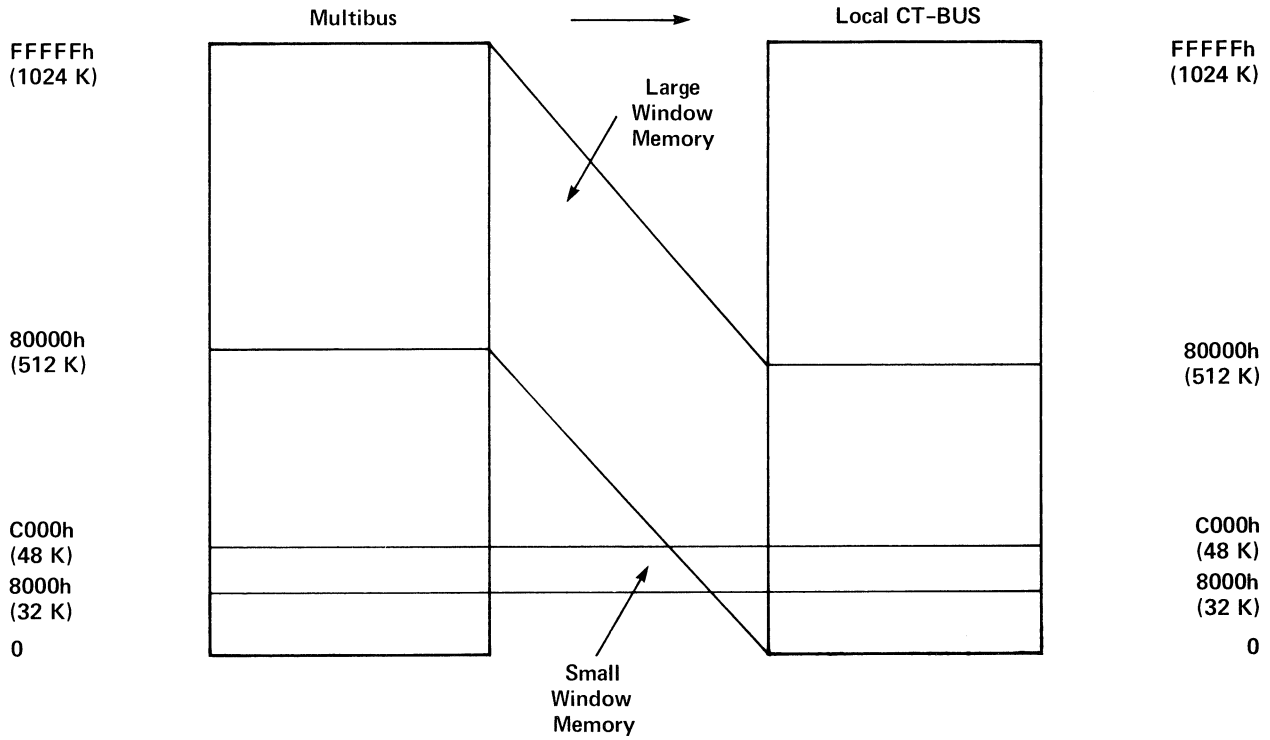


Figure 1-4. Memory-Mapping Between the Local Bus and Multibus (Continued)

For use with CPU boards 60-00002-00 and 60-00036-00 and the 16K I/O Memory board:

Total System Capacity	16K I/O Memory Board	RAM Expansion Board
256K	128K	128K
384K	128K	256K
512K	128K	384K
640K	128K	512K

For use with CPU board 60-00110-00 and the 16K I/O Memory board:

Total System Capacity	16K I/O Memory Board	RAM Expansion Board
384K	128K	256K

For use with the CPU board 60-00110-00:

Total System Capacity	64K I/O Memory Board	RAM Expansion Board
384K	384K	-
512K	384K	128K
512K	512K	-
640K	384K	256K
768K	512K	256K
768K	384K	384K
1 Mb†	512K	512K

† 32 kilobytes of the address space must be reserved for permanent ROM space. Also, 160 kilobytes of the address space must be reserved for ROM space if the optional RAM Expansion board is used. See Appendix C for special S3, S4, and S6 switch settings for 1 Mb of RAM.

Note: For CPU board switch settings, see Appendix C.

Figure 2-9. RAM Configurations (kilobytes).

Typically, the operating system will write the entire contents of memory to disk upon parity-error detection and bootstrap a new version of the operating system.

The bottom 32 kilobytes of RAM, where the operating system typically resides, can be write-protected by setting a bit in the I/O Control Register (IOCR). If a write is attempted into this area, it is prevented and a non-maskable interrupt to the CPU is generated.

Multibus/Local-Bus Memory Mapping

The processor board contains a set of switches which define memory-space windows for local and Multibus masters. The windows determine whether memory resources on the Multibus or on the local bus will be addressed when an address is generated by a master. These windows are illustrated in Figure 1-4 of the prior chapter. Three choices of windows are available for local-bus masters, and four choices are available for Multibus masters.

This scheme of windowing is intended to facilitate communication across the Multibus interface with either 8-bit or 16-bit microprocessor boards on the Multibus. It also tends to minimize the amount of physical memory chips needed for high-address communication. A small and large window are available in both directions.

The small window is generally intended for interprocessor communication. On the Multibus side, this window falls within the 64-kilobyte address space of 8-bit boards without interfering with the board's ability to access its own low-end or high-end operating memory. On the local-bus side, there will always be some RAM at the low end of the memory space where communication message buffers are located and Multibus masters will be able to access these locations.

The large window is generally intended for buffering of large I/O devices, such as tape drives. The method used for shifting the window across the Multibus interface simply involves forcing the high-order address bits one way or another.

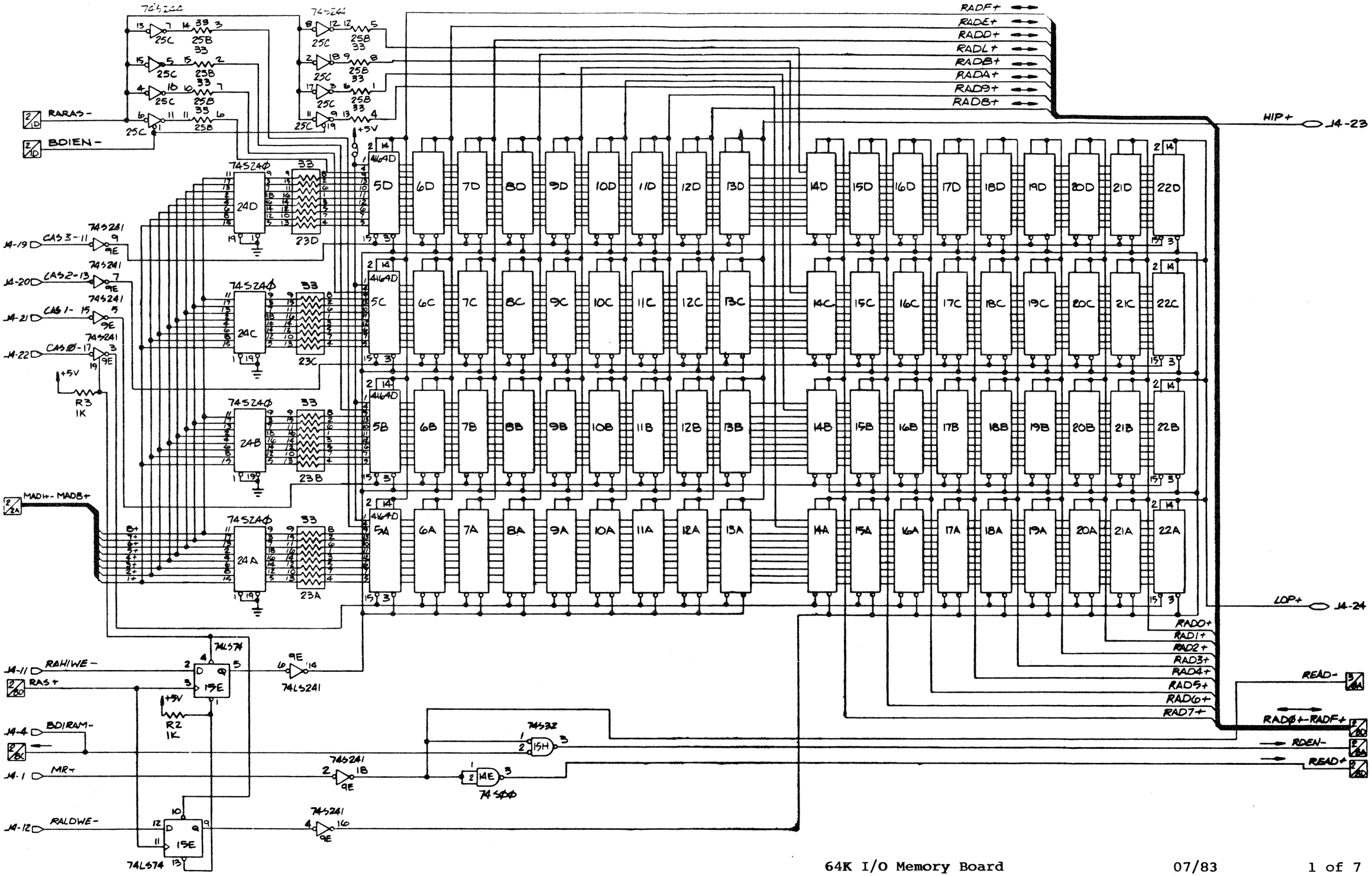
PRINTER INTERFACE

An 8-bit parallel Centronics-type printer interface is provided through a 25-pin D-type male connector on the mainframe enclosure. The interface outputs ASCII data from a memory buffer using the low byte of the MEM bus and I/O port 50 (80). It will accommodate both buffered and non-buffered printers that use the Centronics signaling format. A 4-bit Printer Status Register (PSR) is also available for reading status through port 50 (80).

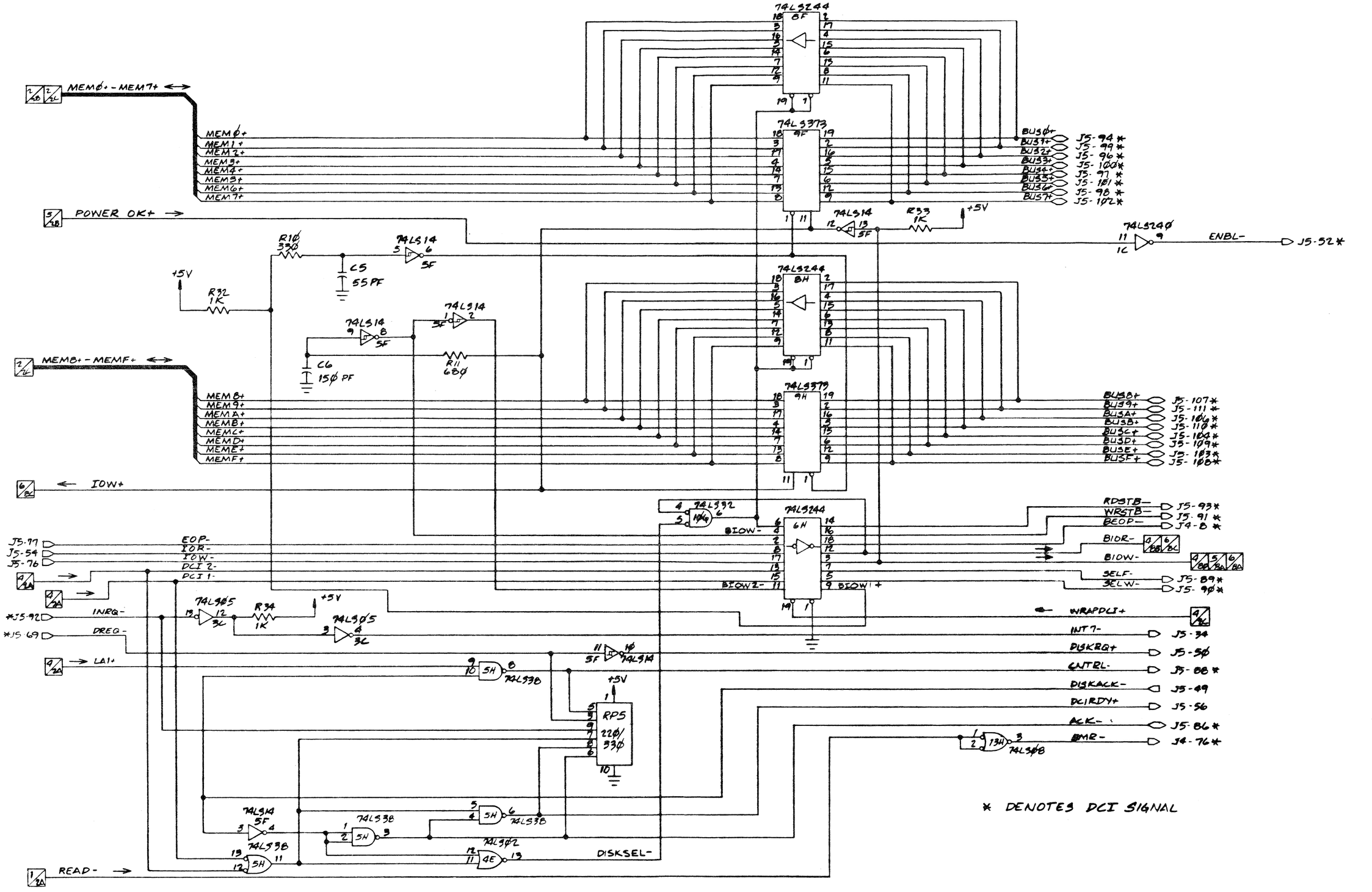
The pinout for the 25-pin connector, which carries signals for both the data output, status input and control signals, is shown in Figure 2-37.

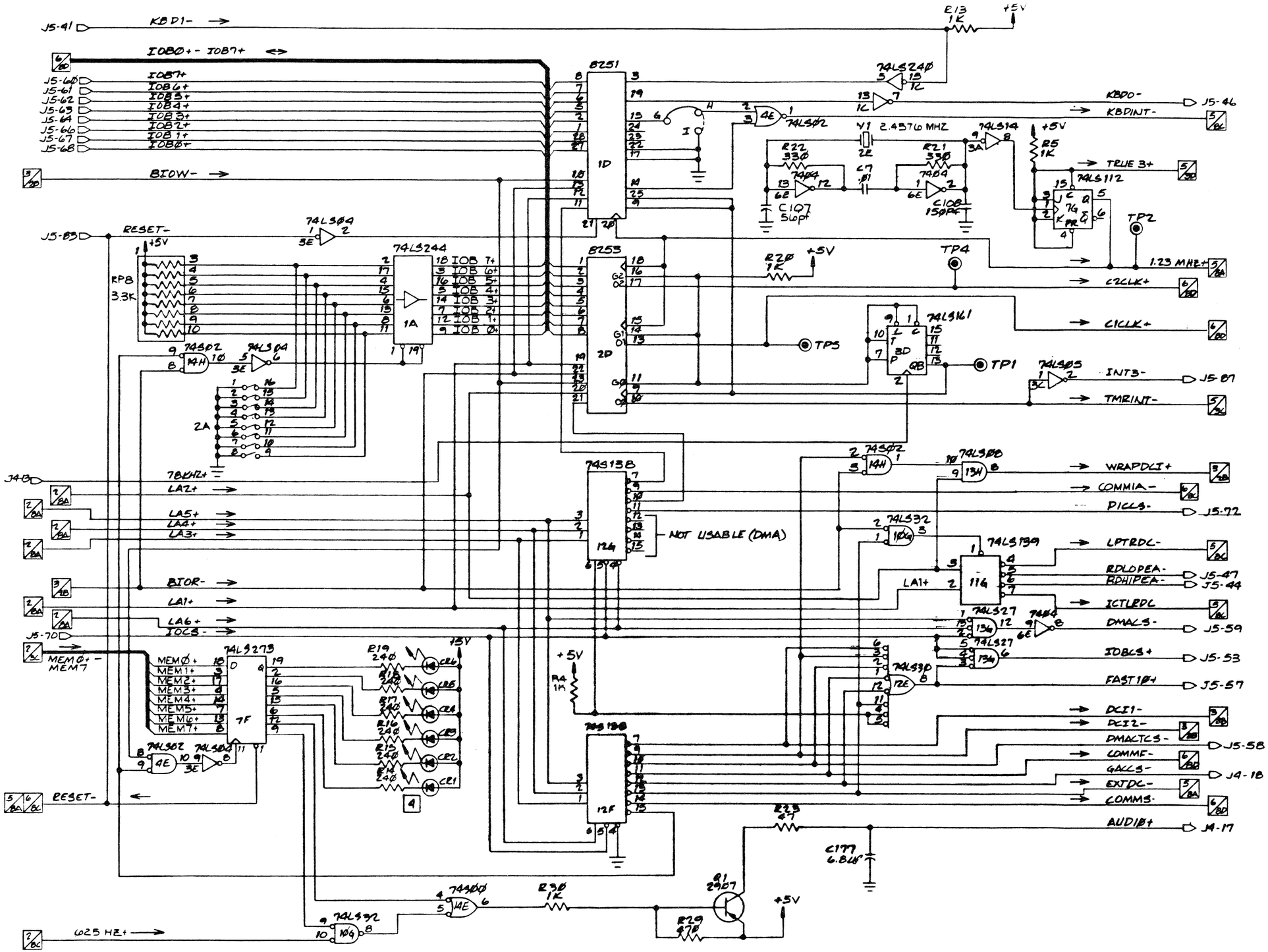
Pin	Signal	Source
1	Data bit 0	Mainframe
2	Data bit 1	Mainframe
3	Data bit 2	Mainframe
4	Data bit 3	Mainframe
5	Data bit 4	Mainframe
6	Data bit 5	Mainframe
7	Data bit 6	Mainframe
8	Data bit 7	Mainframe
9	Ground	
10	Ground	
11	Ground	
12	Ground	
14	Strobe (DATA STROBE/)	Mainframe
15	Ground	
16	Acknowledge (ACKNLG/)	Printer
17	Printer Busy (BUSY)	Printer
21	No Paper (PE)	Printer
22	Select (SLCT)	Printer
25	Ground	

Figure 2-37. Printer Connector Pinout


74S244
74S244
25C
25B
33
RARAS-
BDIEN-
+5V
74S240
24D
23D
24C
23C
24B
23B
24A
23A
74S241
CAS3-11
CAS2-13
CAS1-15
CAS0-17
M-19
M-20
M-21
M-22
R3
1K
MAD1+-MAD8+
4164D
5D
6D
7D
8D
9D
10D
11D
12D
13D
14D
15D
16D
17D
18D
19D
20D
21D
22D
5C
6C
7C
8C
9C
10C
11C
12C
13C
14C
15C
16C
17C
18C
19C
20C
21C
22C
5B
6B
7B
8B
9B
10B
11B
12B
13B
14B
15B
16B
17B
18B
19B
20B
21B
22B
5A
6A
7A
8A
9A
10A
11A
12A
13A
14A
15A
16A
17A
18A
19A
20A
21A
22A
RADF+
RADE+
RADD+
RADL+
RADB+
RADA+
RAD9+
RAD8+
HIP+
J4-23
LOP+
J4-24
RADO+
RAD1+
RAD2+
RAD3+
RAD4+
RAD5+
RAD6+
RAD7+
74LS74
RAHIWE-
RAS+
M-11
M-60
15E
R2
1K
74LS241
BDIRAM-
M-4
M-1
MR+
74S32
15H
74S00
14E
RALDWE-
M-12
READ-
RAD8+-RADF+
RDEN-
READ+

J4-7 RARAS-
READ+
RAS+
74S00 14E
RARAS- 1/8D
BDIEN- 1/8D
RAD0+ - RADF+ 1/1A
625 HZ 4/6A
74LS161
J4-10 RFDONE-
+5V
R1 1K
14F
13F
74LS161
74LS373 15F
BDIRAM- 1/8A
J4-9 RFGO-
74S08 13H
74LS241 9E
LA10+ 5/8B
J4-47 LA10+
J4-49 LAE+
J4-50 LAD+
J4-51 LAC+
J4-60 LA4+
J4-61 LA3+
J4-62 LA2+
J4-63 LA1+
74S258 14G
LA4+
LA3+
74S02 14H
J4-6 COLMPX-
J4-52 LAB+
J4-53 LAA+
J4-54 LA9+
J4-56 LAB+
J4-48 LAF+
J4-57 LA7+
J4-58 LA6+
J4-59 LA5+
74S258 15G
LA6+
LA5+
LAF+ 5/8B
RDEN- 1/2A
RADF+
RADE+
RADD+
RADC+
RADB+
RADA+
RAD9+
RAD8+
74LS240 10F
10E
RP4 3.3K
MEMF+
MEME+
MEMD+
MEMC+
MEMB+
MEMA+
MEM9+
MEM8+
MEMF+ J4-26
MEME+ J4-27
MEMD+ J4-28
MEMC+ J4-29
MEMB+ J4-30
MEMA+ J4-31
MEM9+ J4-32
MEM8+ J4-33
MEM8+ - MEMF+ 3/6C 5/8B 6/8B
RP3 1K
RAD7+
RAD6+
RAD5+
RAD4+
RAD3+
RAD2+
RAD1+
RAD0+
13E
11E
RP2 3.3K
RP1 1K
MEM7+
MEM6+
MEM5+
MEM4+
MEM3+
MEM2+
MEM1+
MEM0+
MEM7+ J4-34
MEM6+ J4-36
MEM5+ J4-37
MEM4+ J4-38
MEM3+ J4-39
MEM2+ J4-40
MEM1+ J4-41
MEM0+ J4-42
MEM4+ - MEM7+ 3/8A 4/8B 5/8D
MEM0+ - MEM3+ 3/8D 4/8B 5/8D 6/8A
MAD8+
MAD7+
MAD6+
MAD5+
MAD4+
MAD3+
MAD2+
MAD1+
MAD1+ - MAD8+ 1/8B
LA3+ - LA6+ 4/8B
LA1+ 3/8B 4/8B 5/8B 6/8D
LA2+
4/8C 5/8D 6/8B


MEM0+ - MEM7+
MEM0+
MEM1+
MEM2+
MEM3+
MEM4+
MEM5+
MEM6+
MEM7+
74LS244
8F
74LS373
8F
BUS0+
BUS1+
BUS2+
BUS3+
BUS4+
BUS5+
BUS6+
BUS7+
J5-94*
J5-99*
J5-96*
J5-100*
J5-97*
J5-101*
J5-98*
J5-102*
POWER OK+
74LS14
5F
R33
1K
+5V
74LS240
1C
ENBL-
J5-52*
R10
330
C5
55 PF
74LS14
5F
+5V
R32
1K
74LS14
5F
74LS14
5F
C6
150 PF
R11
680
MEMB+ - MEMF+
MEMB+
MEM9+
MEMA+
MEMB+
MEMC+
MEMD+
MEME+
MEMF+
74LS244
8H
74LS373
9H
BUSB+
BUS9+
BUSA+
BUSB+
BUSC+
BUSD+
BUSE+
BUSF+
J5-107*
J5-111*
J5-106*
J5-110*
J5-105*
J5-109*
J5-103*
J5-108*
IOW+
74LS32
1/4
74LS244
6H
BIOW-
BIOW2-
RDSTB-
WRSTB-
BEOP-
BIOR-
BIOW-
SELF-SELW-
J5-93*
J5-91*
J4-8*
J5-89*
J5-90*
EOP-
IOR-
IOW-
DCI2-
DCI1-
J5-77
J5-54
J5-76
74LS85
R34
1K
+5V
74LS05
3C
INRQ-
DREQ-
*J5-92
*J5-69
74LS14
5F
WRAPDET+
INT7-
DISKRQ+
CNTRL-
DISKACK-
DCIRDY+
ACK-
BMR-
J5-34
J5-50
J5-88*
J5-49
J5-56
J5-86*
J4-76*
LA1+
74LS38
5H
RP5
220/330
+5V
74LS14
5F
74LS38
5H
74LS38
5H
74LS38
5H
74LS02
4E
74LS08
READ-
DISKSEL-
* DENOTES DCI SIGNAL


J5-41
KBD1-
IOB0+ - IOB7+
IOB7+
IOB6+
IOB5+
IOB4+
IOB3+
IOB2+
IOB1+
IOB0+
J5-60
J5-61
J5-62
J5-63
J5-64
J5-65
J5-67
J5-68
BIOW-
J5-83
RESET-
+5V
RP8
3.3K
74LS244
1A
2A
74LS04
74LS02
74LS00
74LS08
78KHZ+
J4-B
LA2+
LA5+
LA4+
LA3+
BIOR-
LA1+
LA6+
IOCS-
J5-70
MEM0+ - MEM7
74LS273
7F
74LS32
74LS86
RESET-
B251
1D
B253
2D
74LS138
12F
12A
NOT USABLE (DMA)
E13
1K
74LS240
74LS02
Y1 2.4576 MHZ
74LS14
R22
330
R21
330
74LS04
C107
56pf
C108
150PF
R5
1K
74LS112
TRUE 3+
TP2
1.23 MHZ+
C2CLK+
C1CLK+
R20
1K
TP4
TP3
74LS161
TP1
74LS03
INT3-
TMRINT-
KBDO-
KBDINT-
J5-46
R19
240
R18
240
R17
240
R16
240
R15
240
R14
240
CR6
CR5
CR4
CR3
CR2
CR1
4
R4
1M
74LS32
74LS00
R30
1K
R29
47R
Q1
2907
R23
47
C177
6.8uF
74LS00
74LS32
74LS139
74LS27
74LS04
74LS30
WRAPDCI+
COMMIA-
PICCS-
J5-72
LPTRDC-
RDLOPEA-
RDHIPEA-
J5-47
J5-44
ICTLRDC
DMACS-
J5-59
IOBCS+
J5-53
FAST10+
J5-57
DCI1-
DCI2-
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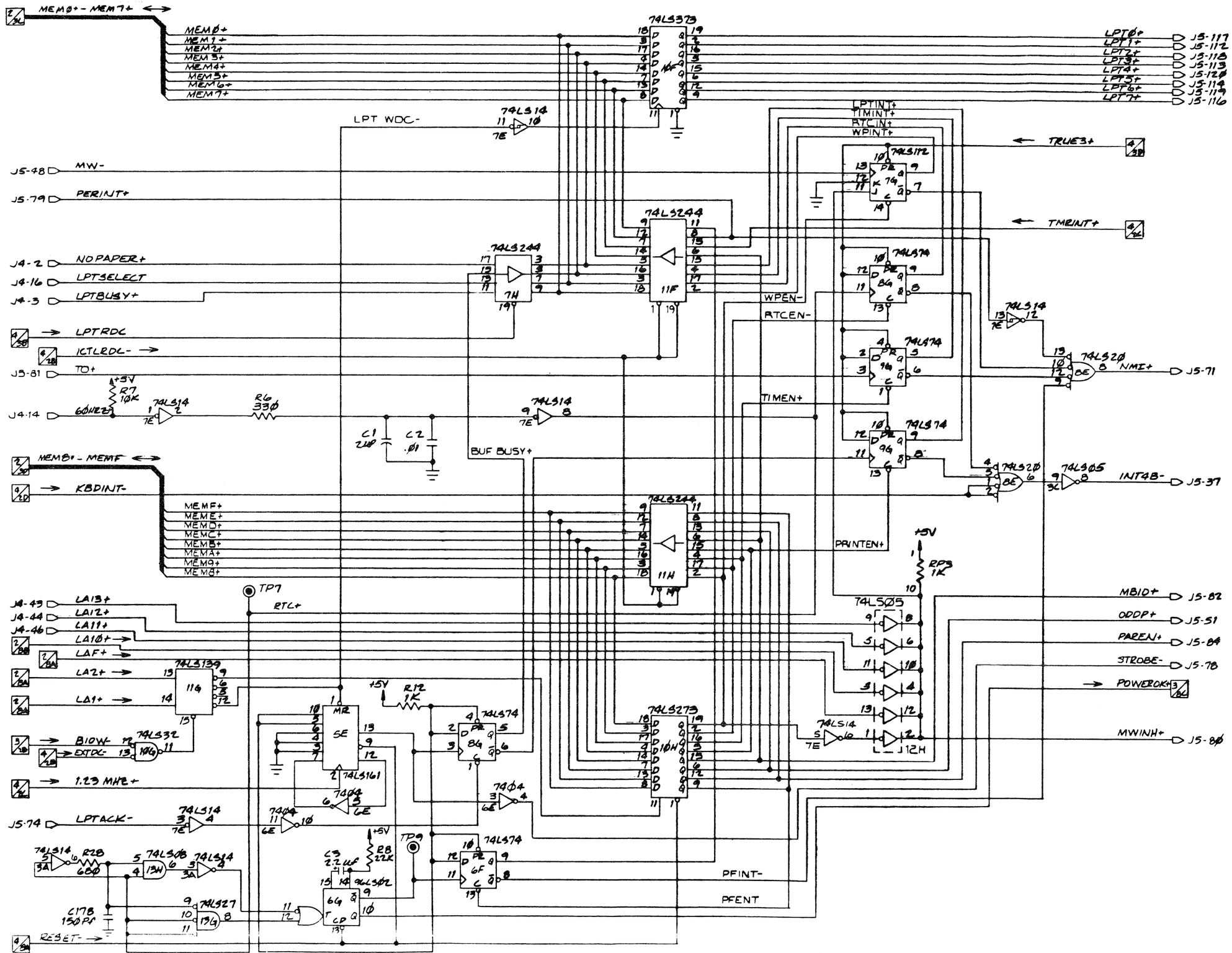
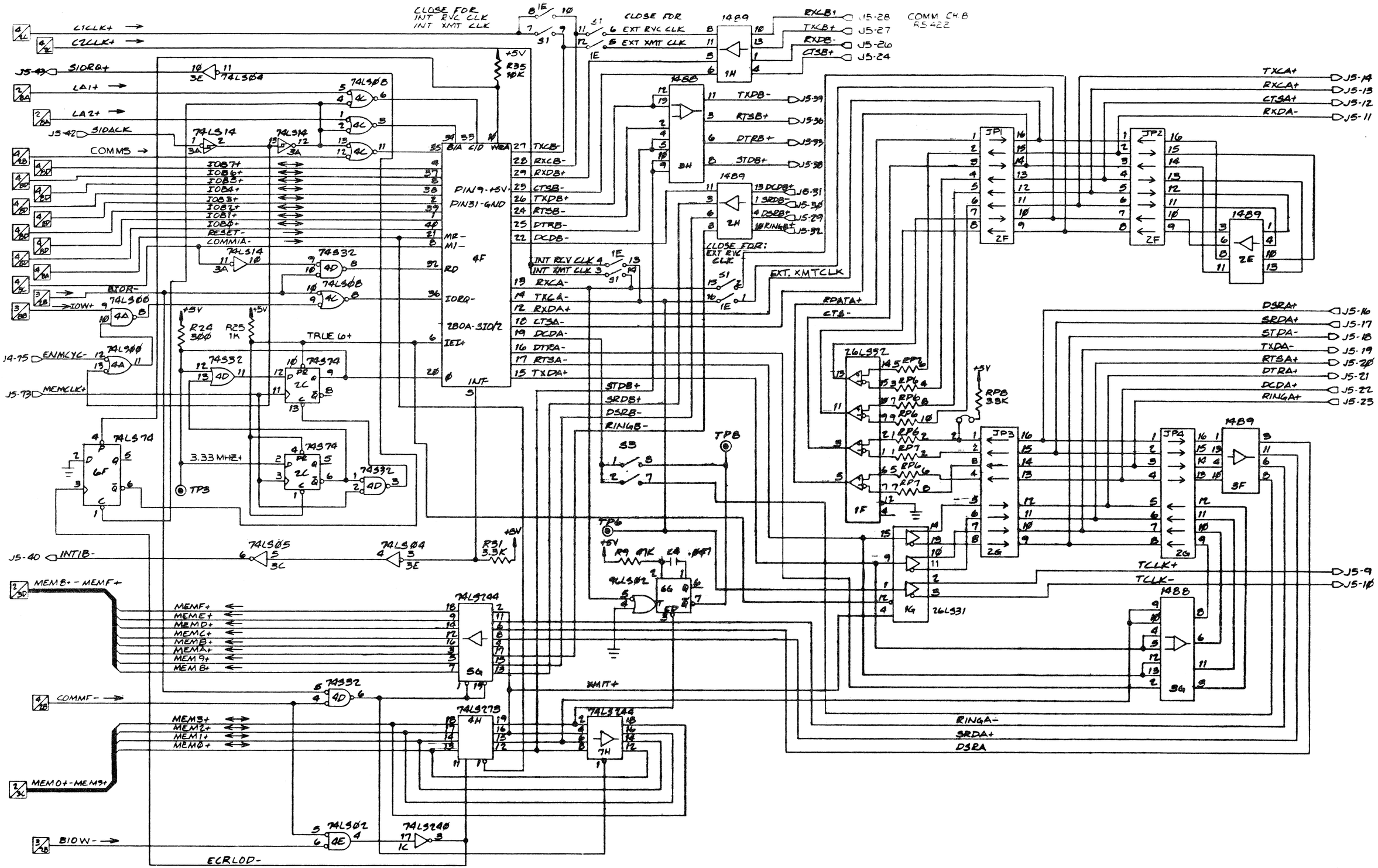
J5-58
COMMF-
GACCS-
J4-18
EXTDC-
COMMS-
AUDIO+
J4-17
625 HZ+


MEM0+ - MEM7+
MEM0+
MEM1+
MEM2+
MEM3+
MEM4+
MEM5+
MEM6+
MEM7+
74LS373
LPT0+
LPT1+
LPT2+
LPT3+
LPT4+
LPT5+
LPT6+
LPT7+
J5-117
J5-112
J5-118
J5-113
J5-120
J5-114
J5-119
J5-116
LPT WDC-
74LS14
7E
LPTINT+
TIMINT+
RTCIN+
WPINT+
74LS112
TRUE3+
TMRINT+
J5-48 MW-
J5-79 PERINT+
74LS244
74H
11F
J4-2 NOPAPER+
J4-16 LPTSELECT
J4-3 LPTBUSY+
74LS74
WPEN-
RTCEN-
LPTRDC
ICTLRDC-
J5-81 TO+
+5V
R7 10K
J4-14 60HZ
R6 330
C1 2UF
C2 .01
BUF BUSY+
TIMEN+
NMI+
J5-71
74LS20
74LS05
INT4B-
J5-37
MEMF+ - MEM8+
KBDINT-
MEMF+
MEME+
MEMD+
MEMC+
MEMB+
MEMA+
MEM9+
MEM8+
11H
PRINTEN+
RP3 1K
TP7
RTC+
J4-43 LA13+
J4-44 LA12+
J4-46 LA11+
LA10+
LAF+
LA2+
LA1+
74LS139
74LS32
BIOW-
EXTDC-
1.23 MHZ+
74LS161
R12 1K
74LS273
10H
MBID+
ODDP+
PAREN+
STROBE-
POWEROK+
MWINH+
J5-82
J5-51
J5-84
J5-78
J5-80
12H
J5-74 LPTACK-
R28 680
C178 150PF
RESET-
TP9
C3 2.2 UF
R8 22K
74LS02
PFINT-
PFENT


CLOSE FOR INT RVC CLK INT XMT CLK
CLOSE FOR EXT RVC CLK
EXT XMT CLK
COMM CH B RS 422
RXCB+ J5-28
TXCB+ J5-27
RXDB- J5-26
CTSB+ J5-24
TXCA+ J5-14
RXCA+ J5-13
CTSA+ J5-12
RXDA- J5-11
DSRA+ J5-16
SRDA+ J5-17
STDA- J5-18
TXDA- J5-19
RTSA+ J5-20
DTRA+ J5-21
DCDA+ J5-22
RINGA+ J5-23
TCLK+ J5-9
TCLK- J5-10
L1CLK+
L2CLK+
J5-43 SIORQ+
LA1+
LA2+
J5-42 SIOACK
COMM5
IOB7+
IOB6+
IOB5+
IOB4+
IOB3+
IOB2+
IOB1+
IOB0+
RESET-
COMMIA-
IORR-
IOW+
J4-75 ENMCYC-
J5-73 MEMCLK+
3.33 MHZ+
TP3
INTIB- J5-40
MEMB+ - MEMF+
MEMF+
MEME+
MEMD+
MEMC+
MEMB+
MEMA+
MEM9+
MEM8+
COMMF-
MEM3+
MEM2+
MEM1+
MEM0+
MEM0+ - MEM3+
BIOW-
ECRLOD-
PIN9 +5V
PIN31 GND
INT RCV CLK 4
INT XMT CLK 3
RXCA-
TXCA-
RXDA+
CTSA-
DCDA-
DTRA-
RTSA-
TXDA+
STDB+
SRDB+
DSRB-
RINGB-
TPB
TPG
EXT. XMTCLK
RDATA+
CTS-
XMIT+
RINGA-
SRDA+
DSRA
RPB 3.3K

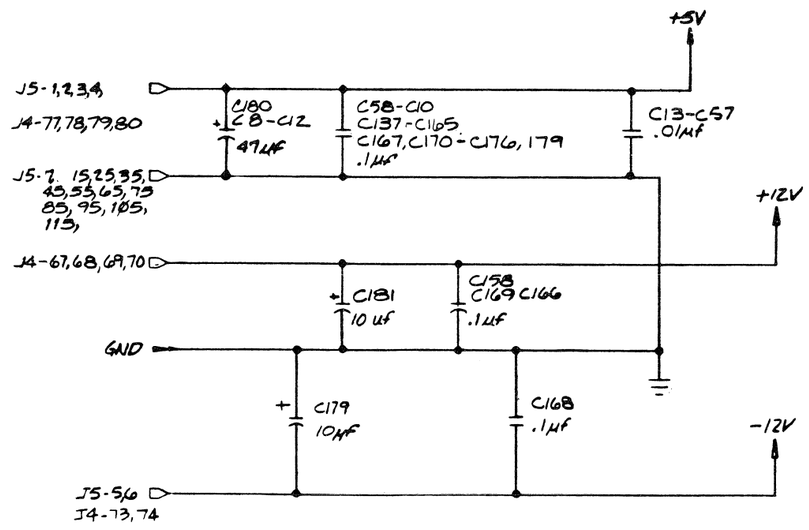
NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES ARE IN OHMS, 1/4W 5%
2. COMPACITANCE VALUES ARE IN PICOFARADS.
3. ALL DEVICES ARE STANDARD 7400, 8T16 AND 10T20 GROUND & POWER CONNECTIONS.
4. ALL DIODES ARE TYPE FLV560.

POWER AND GROUND LOCATOR CHART					
REF DES.	DEVICE TYPE	+5V	GND	+12	-12
5A-22A 5B-22B 5C-22C 5D-22D	4160-4	8	16		
4F	7830A-SIO/2	9	31		
1D	8251	26	4		
3H, 3G	1488		7	14	1

SPARE GATES		
REF DES16.	DEVICE TYPE	NO. OF GATES

REFERENCE DESIGNATION	
LAST USED	NOT USED
RP7	
R34	
C181	C109-C136
JP4	
CR6	
Y1	
J5	J1-J3



COMMAND	HEX CODE
Reset	92 (146)
CheckROM	8C (140)
Echo	9E (158)
LED03	AX (160+X)
LED47	BX (176+X)

"Reset" cancels the Echo mode (if enabled), turns off all the LEDs, waits for any bytes in the keyboard buffer to be sent out and then initiates a new scan.

"CheckROM" computes a checksum of the 8048 ROM and sends it to the processor.

"Echo" causes the 8048 to send back all subsequent 256 input bytes verbatim (excluding the LED commands, which are interpreted as usual but do not cancel the Echo mode) until one of those bytes is 92 (146) or 80 (128), which are interpreted as Reset or CheckROM commands.

"LED03" and "LED47" write the bit pattern specified by 'X' to LEDs 0-3 and 4-7, respectively. 'X' is the bottom nibble of the command byte.

OPERATION

The 8048 scans the keyboard by generating a series of row address (pins 21-24) and monitoring the state of the column lines (pins 27-34). Chip IC6 demultiplexes the row addresses and drives the corresponding row lines in the keyboard array.

Crystal Y36 and the number of program steps involved in the 8048's UART operations determine the baud rate, which is 1221 baud, the same as that of the 8251A USART in the mainframe.

DATA IN is buffered by a Schmitt trigger inverter, whose hysteresis helps ensure good noise immunity. DATA OUT comes from an open-collector TTL gate, which has an external 1K pullup resistor.

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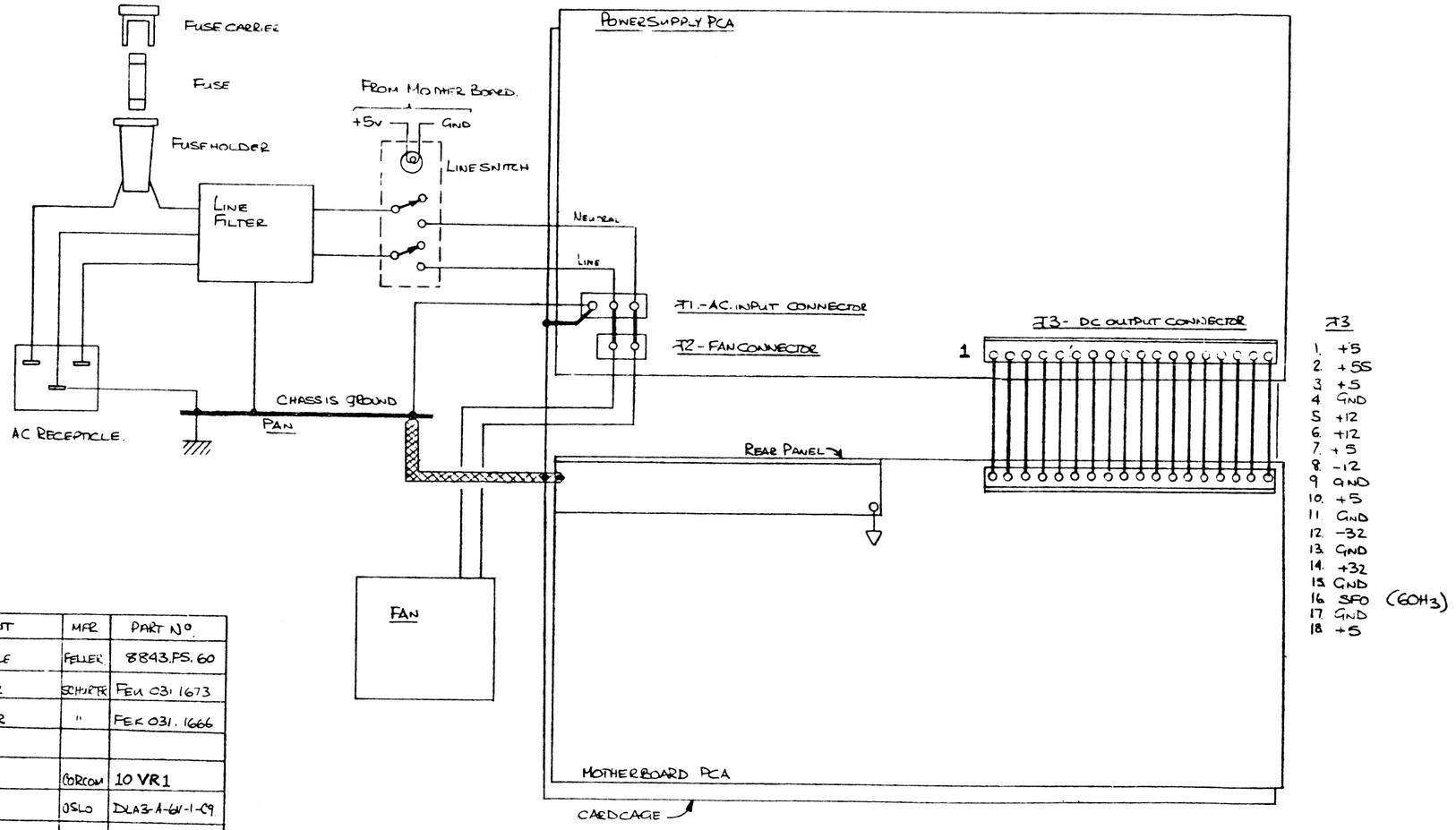

COMPONENT	MFR	PART NO.
AC RECEPTICLE	FELLER	8843.FS.60
FUSE HOLDER	SCHURTER	FEH 031 1673
FUSE CARRIER	"	FEK 031. 1666
FUSE.		
LINE FILTER	CORCOM	10 VR1
LINE SWITCH	OSLO	DLA3-A-6W-1-09
J1 - INPUT CONNECTOR	AMP	640900-1
J2 - FAN CONNECTOR	AMP	350786-1
J3 - DC OUTP. CONN.	AMP	1-640386-8

APPENDIX C

WORKSTATION SWITCH AND JUMPER SETTINGS

CPU BOARD SWITCHES

The functions of each of the switches on the CPU board are listed below.

S1

Bit	On	Off
1	4 MHz DMA	5 MHz DMA
2	no wait states	one wait state
3	not used	not used
4	5 MHz 8086	3.3 MHz 8086

S2

1	Multibus-to-CT window at 512K	no Multibus-to-CT window at 512K
2	not used	not used
3	not used	not used
4	no Multibus-to-CT window at 32K	Multibus-to-CT window at 32K

S3

1	CT-to-Multibus window at 512K	CT-to-Multibus window at 768K
2	CT-to-Multibus window at 768K	CT-to-Multibus window at 512K
3	CT generates CCLK-	external CCLK-generation
4	CT generates BCLK-	external BCLK-generation

S4 (for use with 16K I/O Memory board and CPU board numbers 60-00002-00 or 60-00036-00)

1	640K RAM total	256K RAM total 384K RAM total 512K RAM total
2	-	256K RAM total 384K RAM total 512K RAM total 640K RAM total
3	256K RAM total 512K RAM total	384K RAM total 640K RAM total
4	256K RAM total 384K RAM total	512K RAM total 640K RAM total

S4 (for use with 16K I/O Memeory board and CPU board number 60-00110-00)

1	-	384K RAM total
2	-	384K RAM total
3	-	384K RAM total
4	384K RAM total	-

S4 (for use with 64K I/O Memory board with 384K of RAM and CPU board number 60-00110-00)

1	640K RAM total	384K RAM total
	768K RAM total	512K RAM total
2	384K RAM total	
		768K RAM total
	640K RAM total	
3	384K RAM total	
	768K RAM total	
	512K RAM total	
	640K RAM total	
4	384K RAM total	640K RAM total
		512K RAM total
	768K RAM total	

S4 (for use with 64K I/O Memory board with 512K of RAM and CPU board number 60-00110-00)

1	768K RAM total	512K RAM total
		1 Mb RAM total*
2	512K RAM total	
	768K RAM total	1 Mb RAM total*
3		512K RAM total
		768K RAM total
		1 Mb RAM total*
4	512K RAM total	768K RAM total
		1 Mb RAM total*

* See Figure 2-9 in Section 2.

Note: For 1 Mb of RAM, also set

S3 switch 1 to off	S6 switch 1 to on
S3 switch 2 to on	S6 switch 2 to off
S3 switch 3 to on	S6 switch 3 to on
S3 switch 4 to on	S6 switch 4 to on

S5

1	2732 PROMs	2716 PROMs
2	2716 PROMs	2732 PROMs
3	not used	not used
4	not used	not used

S6

1	no PROM board	PROM board
2	PROM board	no PROM board
3	no CT-to-Multibus access	CT-to-Multibus access enabled
4	CBRQ- always asserted	CBRQ- from Multibus master

CPU BOARD JUMPERS

For workstations without 8087 coprocessors, a jumper from TP6 to ground must be installed. If an 8087 is used, there must be no jumper installed.

FACTORY CONFIGURATION 3

The following configuration constitutes a Channel A cluster RS-422 and Channel B RS-232 workstation with 2732 bootstrap ROMs. It is the Convergent factory setting for workstations with the following serial numbers:

8131B-00400 and up.

	CPU					
bit	S1	S2	S3	S4	S5	S6
1	on	off	on	*	on	off
2	on	off	off	*	off	on
3	off	off	on	*	off	off
4	on	on	on	*	off	on

* See switch S4 on p. D-1 for the settings for different memory boards.

	I/O Memory		
bit	S1	S2	S3
1	off	on	on
2	on	on	off
3	off	on	off
4	on	on	off
5	off	on	
6	off	on	
7	on	on	
8	on	on	

CPU jumper TP6 to ground is installed.

I/O-Memory jumper E-F is installed.

I/O-Memory jumper plugs JP1 and JP3 are installed; JP2 and JP4 are not installed.

RAM expansion jumper A-C is installed.

Bits 1-8 of motherboard switch U3 are On.

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APPENDIX D: MONITOR FORM OF THE IWS WORKSTATION

OVERVIEW

The monitor form of the IWS workstation is a different version of the IWS workstation with a larger capacity for Multibus boards. The monitor form is designed for use with custom applications requiring up to five Multibus board slots, as opposed to the two Multibus slots provided with standard IWS workstations. Because of the monitor form's design, it is useful in a variety of applications where desk-top space is at a minimum and great Multibus versatility is required.

This appendix describes the monitor form components and explains how boards are inserted and removed from the electronics enclosure. It also contains an overview and description of Multibus and provides the user with instructions and information for designing custom Multibus applications for the monitor form.

Differences between the monitor form and the standard IWS workstation are:

- The desktop portion of the IWS consists only of a video monitor and does not have the added "lectern" assembly found on standard IWS workstations. This arrangement allows the monitor form to take up less room on the desk top than the standard IWS workstation.
- The workstation boards and power supply are contained in a floor-standing, instead of a desktop, enclosure.
- The monitor form electronics enclosure contains five Multibus slots, three more slots than contained in a standard IWS workstation.

Figure D-1 shows the video monitor, detachable keyboard, and electronics enclosure for the monitor form of the IWS workstation.

Video Monitor

The video monitor converts video signals into a visible display, controls the workstation speaker circuitry, and buffers signals between the keyboard and video monitor enclosure.

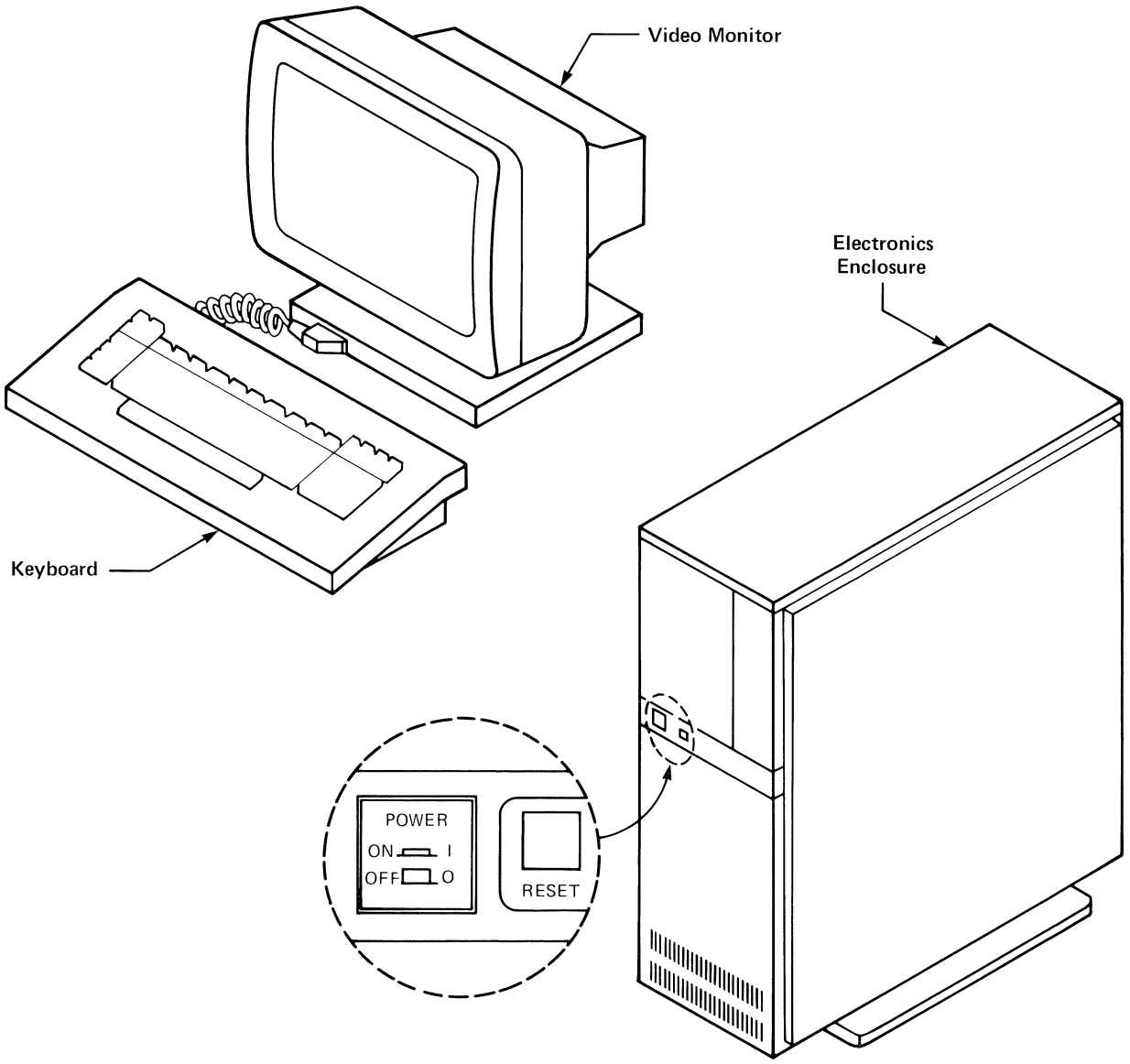


Figure D-1. Monitor Form of the IWS Workstation.

The video monitor case, shown in Figure D-2, contains a 15-inch CRT, the CRT Deflection board, a high-voltage power supply, the Monitor Buffer board, the monitor cable assembly, and a speaker. Figure D-3 contains a block diagram of the video monitor circuitry, which is described below.

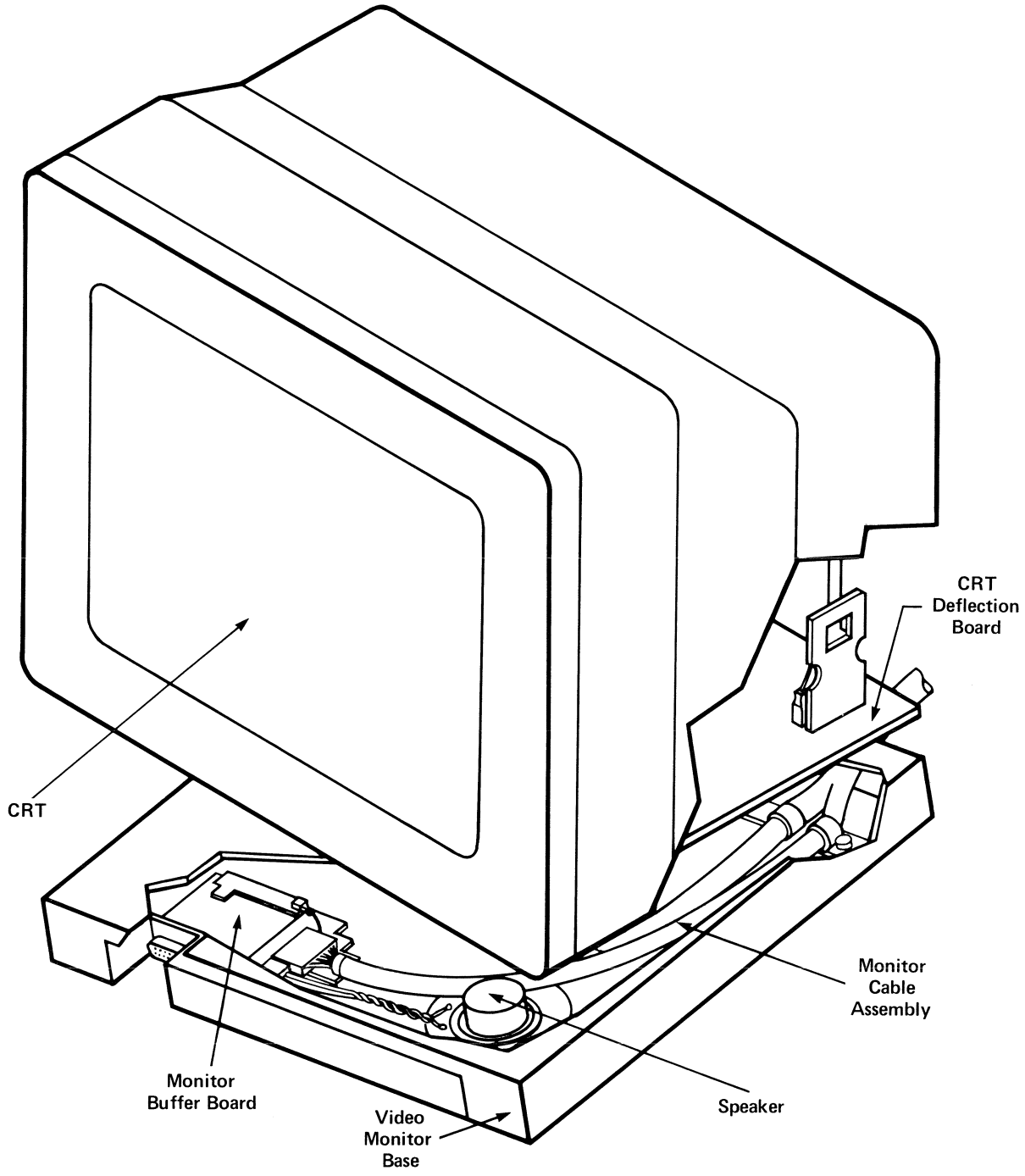


Figure D-2. Video Monitor Case.

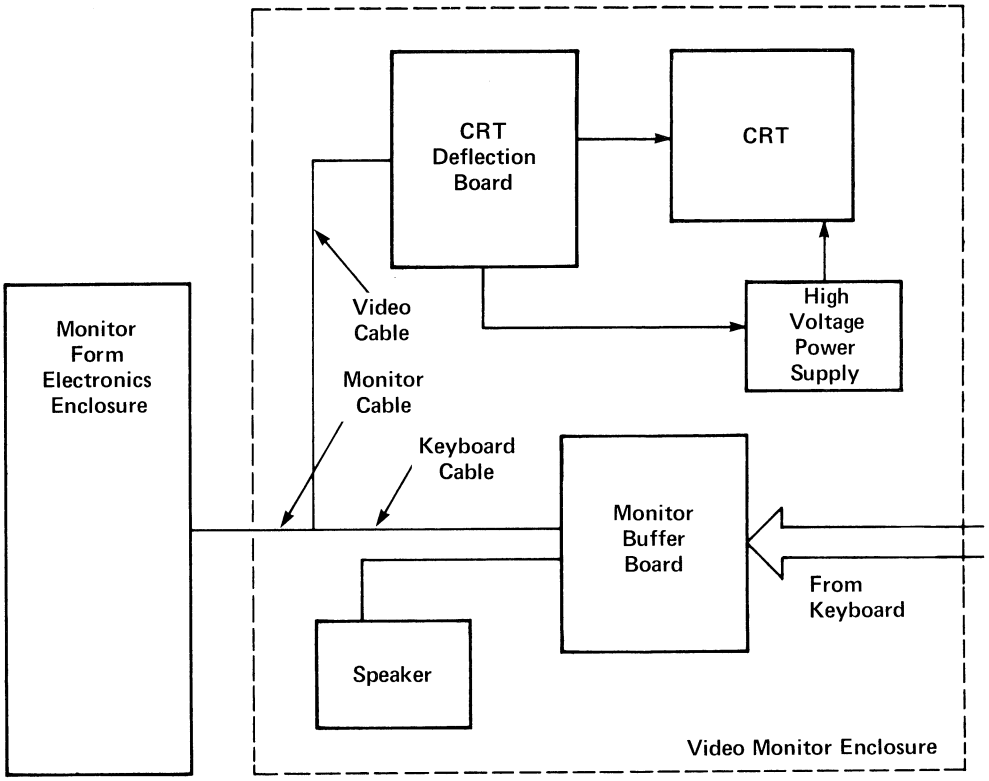


Figure D-3. Video Monitor Block Diagram.

CRT, CRT Deflection Board, and Speaker

The CRT and CRT Deflection board are identical to those found in the standard workstation and explained in Section 10, "Video Monitor (CRT)." The monitor form speaker is also identical to the speaker in the standard workstation, but it is located in the front right-hand section of the monitor base (see Figure D-2) and wired to the Monitor Buffer board instead of the motherboard.

Monitor Buffer Board

The Monitor Buffer board buffers the keyboard signals, connects the remote keyboard and speaker to the electronics box, and generates a regulated +5 V dc from a +12 V-dc input.

A schematic of the Monitor Buffer board is shown in Figure D-4. The schematic shows Q1 as a three-terminal fixed 5-V dc regulator that supplies power to the keyboard via pins 6 and 7 of connector J1. Buffer U1 drives the keyboard

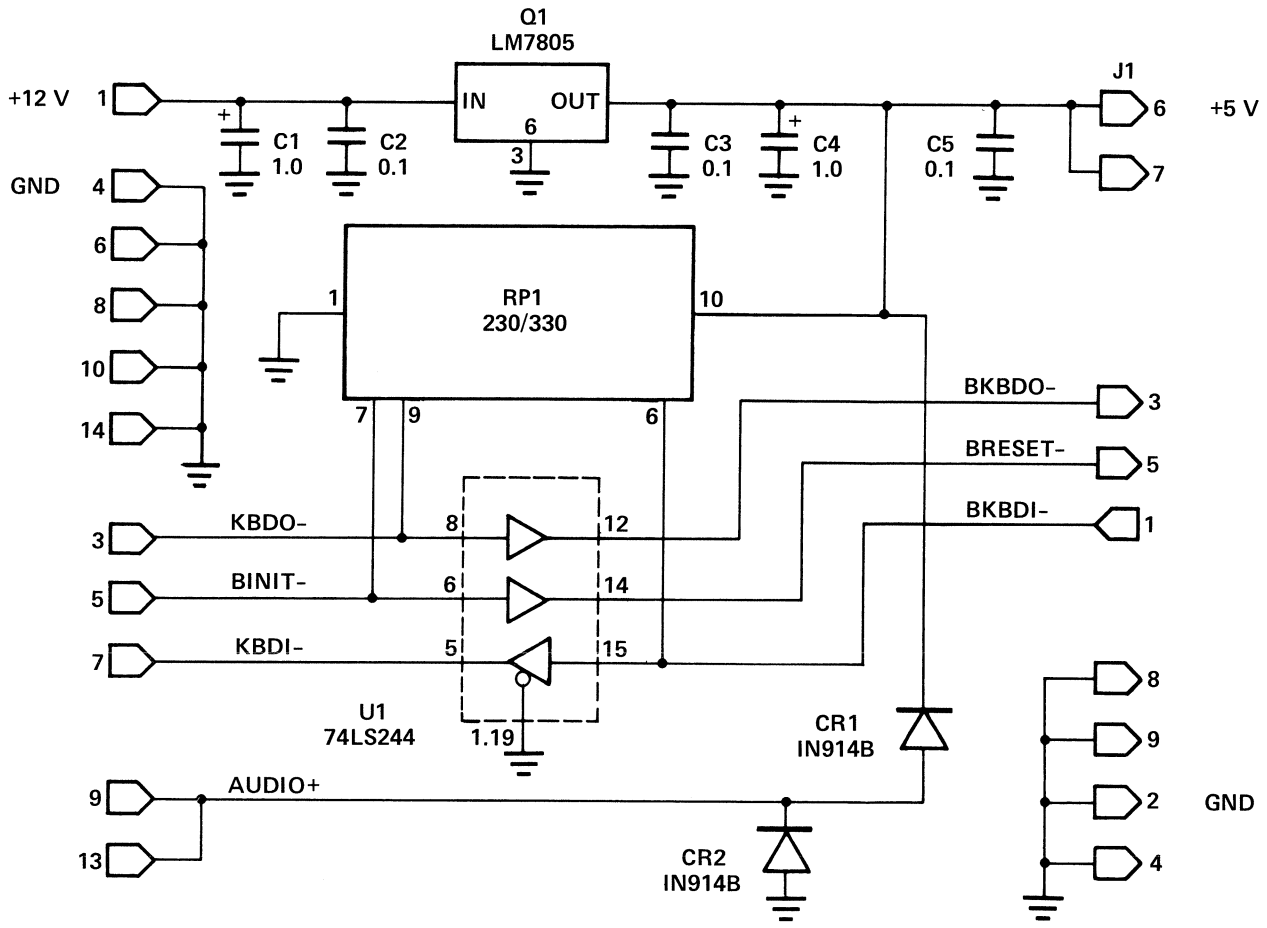


Figure D-4. Monitor Buffer Board Schematic.

signals KBDO-, BINIT- (to the keyboard), and KBDI- (from the keyboard). Resistor pack RP1 provides 230/330 ohm split termination on these lines. The AUDIO+ signal to the speaker is diode terminated with CR1 and CR2 to prevent under- and overvoltage protection.

Monitor Cable Assembly

As shown in Figure D-3, signals from the electronics enclosure are carried through the monitor cable assembly to the video monitor case. The monitor cable assembly, as shown, contains both the video cable and the keyboard cable. The video cable carries video and synchronization information to the monitor; the keyboard cable carries the speaker signals, and signals and power to the keyboard.

Both cables in the monitor cable assembly are enclosed within a single plastic outer sleeve. The monitor cable is 11 ft long and is wired to a single 37-pin D-type connector that plugs into the electronics enclosure monitor socket.

The video cable is wired to a 20-pin D-type connector that plugs into the CRT Deflection board, and the keyboard cable is wired to a 10-pin D-type connector that plugs into the front of theMonitor Buffer board base front. Wire lists for video and keyboard cable connectors are shown in Tables D-1 and D-2. For more information, see Section 10, "Video Monitor (CRT)."

Table D-1. Video Cable Wire List.

37-Pin Monitor Form Connector	Signal Name	Wire Color	20-Pin Electronics Enclosure Connector
1	VIDEOA+	yellow	10
2	VIDEOA-	white/yellow	9
20	VIDEOA (shield)	(return)	8
21	VIDEOB+	black	12
22	VIDEOB-	white/black	13
3	VIDEOB (shield)	(return)	11
6	HORDR+	grey	5
7	HORDR-	white/grey	4
5	HORDR (shield)	(return)	3
25	VERDR+	brown	16
26	VERDR-	white/brown	17
24	VERDR (shield)	(return)	15
9	+32V	red	2
10	-32V	blue	1
29	+12V	orange	20
27	CRTOK	green	18
	polarizing plug		14

Table D-2. Keyboard Cable Wire List.

37-Pin Monitor Form Connector	Signal Name	Wire Color	10-Pin Electronics Enclosure Connector
17	12V	white	1
36	polarizing plug	black	2
16	KBDO-	red	3
35	KBDO RETURN	brown	4
15	RESET+	blue	5
34	RESET RETURN	green	6
14	KBDI-	yellow	7
33	KBDI RETURN	orange	8
13	SPKR+/AUDIO+	violet	9
32	SPKR RETURN	grey	10

Keyboard

The monitor form of the IWS workstation uses the same keyboard as a standard IWS workstation. The keyboard is explained in Section 9, "Keyboard." Signals from the electronics assembly are sent to the video monitor, and then to the keyboard via the monitor cable assembly, described above. The keyboard wire list is given in Table D-2.

Electronics Assembly

The electronics assembly, shown in Figures D-5 and D-6, is 26 in high, 8 in wide, and weighs 55 lb. It contains the workstation's electronics boards, the power supply, five Multibus slots, and two fans.

The control panel on the front of the electronics assembly contains the power switch, the power indicator, and the reset button, as shown in Figure D-1.

The power switch allows the operator to control both the floor-standing electronics enclosure and the video monitor. When the power switch is ON, the power indicator is lit, and the workstation

electronics, video monitor, and keyboard are powered up. The reset button allows an operator to reset the system workstation manually. These two switches, shown in Figure D-1, are explained in Section 11, "Console Switches."

As shown in Figure D-5, the power supply and cooling fans are located in the top half of the assembly. The 262-W power supply has a higher capacity than the power supply in a standard IWS workstation. Twenty watts are available to each board, allowing operation of up to five Multibus boards in any range of user applications. The power supply wiring diagram is shown in Figure D-7 and Table D-3 contains the power supply wire list.

There are three main boards in the electronics assembly: the Multibus motherboard, the I/O Extender board, and the Main motherboard These three boards, their contents, and interfaces are explained in the following subsections.

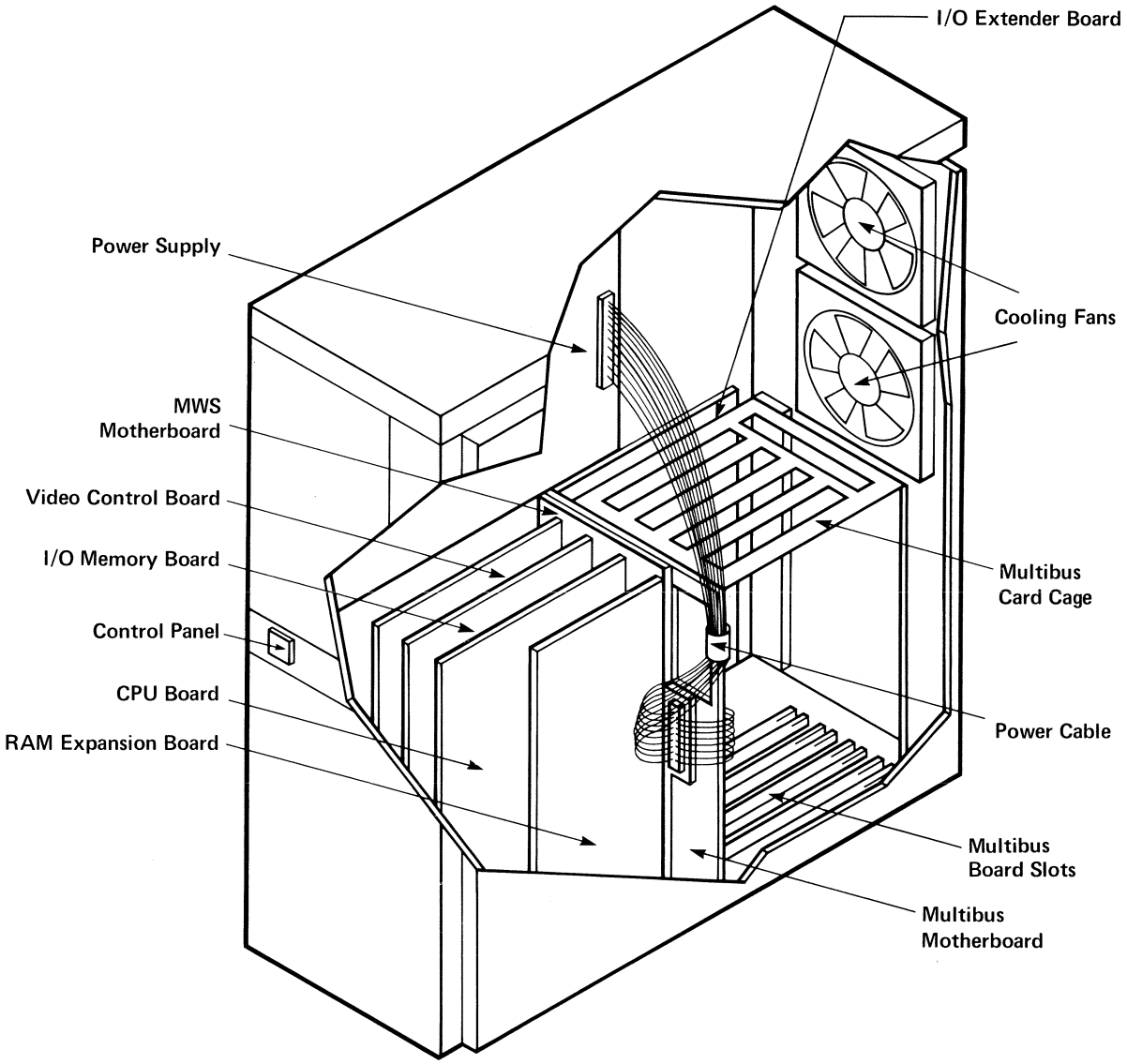


Figure D-5. Electronics Enclosure for the Monitor Form of the IWS Workstation (Front View).

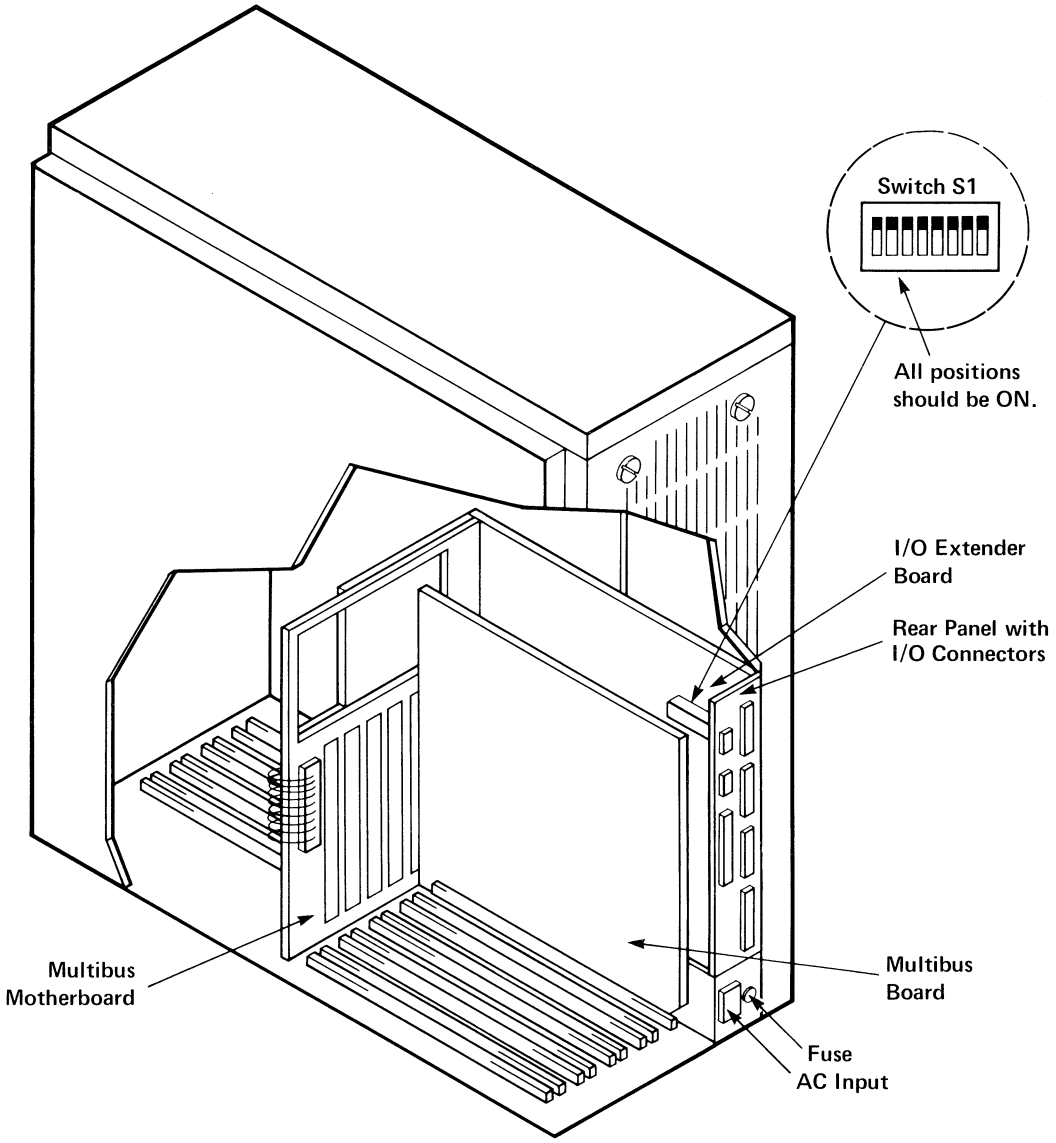


Figure D-6. Electronics Enclosure for the Monitor Form of the IWS Workstation (Rear View).

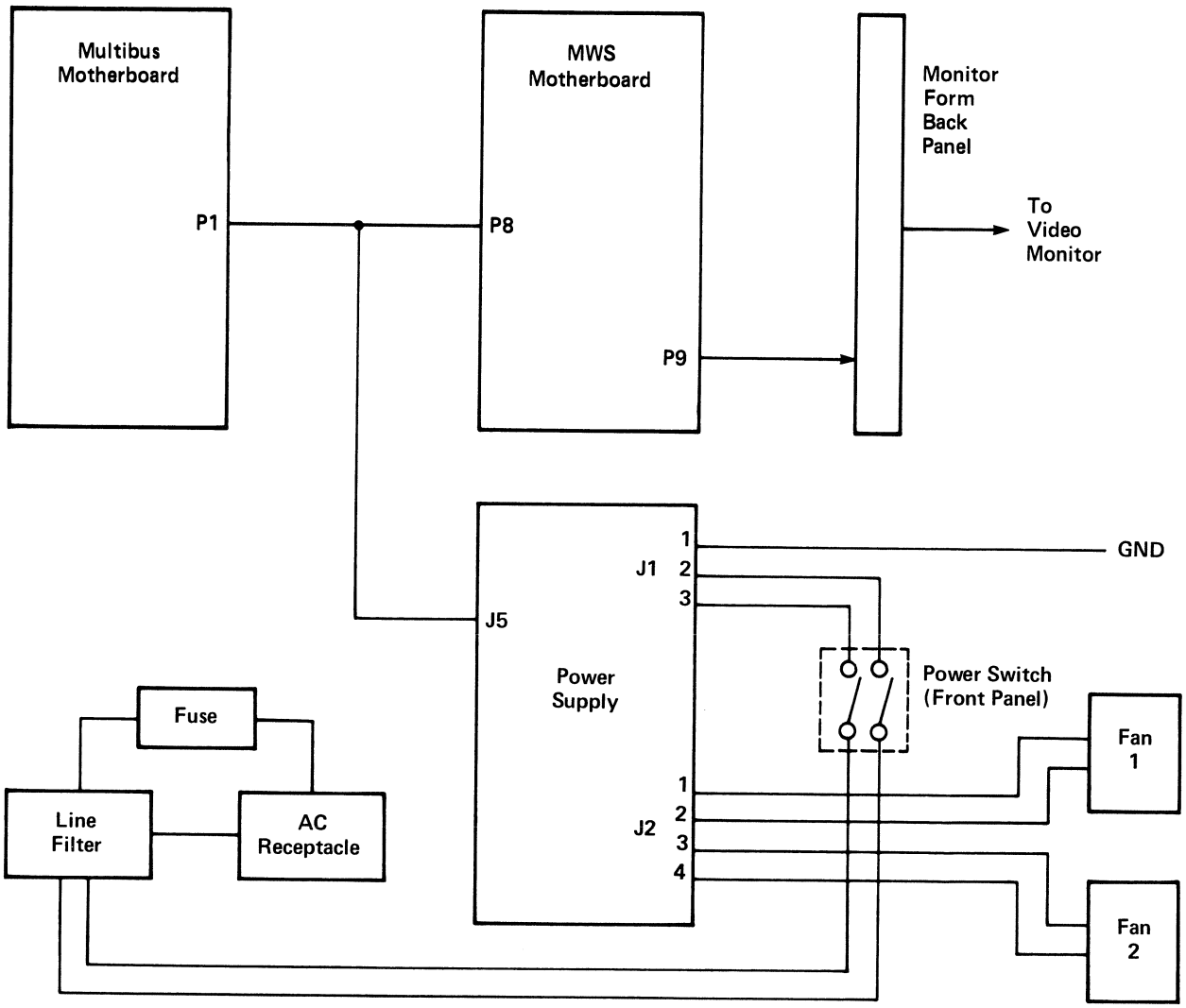


Figure D-7. Power Supply Wiring Diagram.

Table D-3. Power Supply Wire List.

Connector J1		Connector J2	
Pin	Signal	Pin	Signal
1	GND	1	LINE
2	NEUT	2	NEUT
3	LINE	3	LINE
		4	NEUT

Connector J3

Pin	Signal	Pin	Signal
1	+5 V	13	GND
2	+5 S	14	+32 V
3	+5 V	15	GND
4	GND	16	S.F.O.
5	-12 V	17	GND
6	+12 V	18	-5 V
7	+5 V	19	GND
8	-12 V	20	+5 V
9	GND	21	GND
10	+5 V	22	+5 V
11	GND	23	GND
12	-32 V	24	GND

Main Motherboard

The Main motherboard contains terminations for Multibus lines and circuitry for the control panel switches, as shown in Figure D-8. The Main motherboard also accommodates the following standard IWS workstation boards:

- the CPU board
- the I/O Memory board
- the Video Control board
- the RAM Expansion board

These boards are described in Sections 4 through 8 of this manual and can be inserted and removed from the Main motherboard when the front panel of

the electronics assembly is removed, as shown in Figure D-9. One slot is provided for each board.

The Main motherboard also contains connectors for the I/O Extender board and the power supply. The I/O Extender board acts as an interface between the Main motherboard, the Multibus motherboard, and the rear panel (containing peripheral and RS-232-C connectors). Figure D-10 shows connector locations on the Main motherboard.

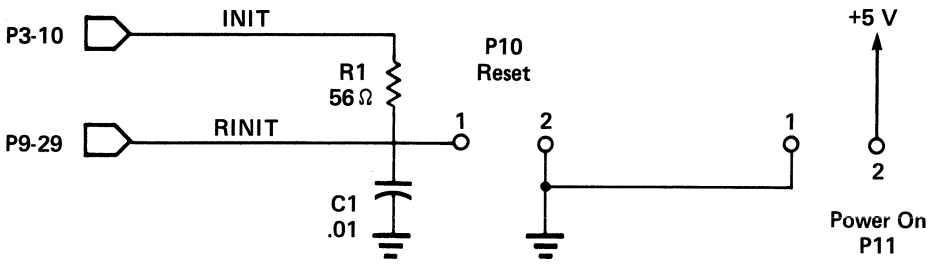


Figure D-8a. Main Motherboard Termination and Console Switch Circuitry.

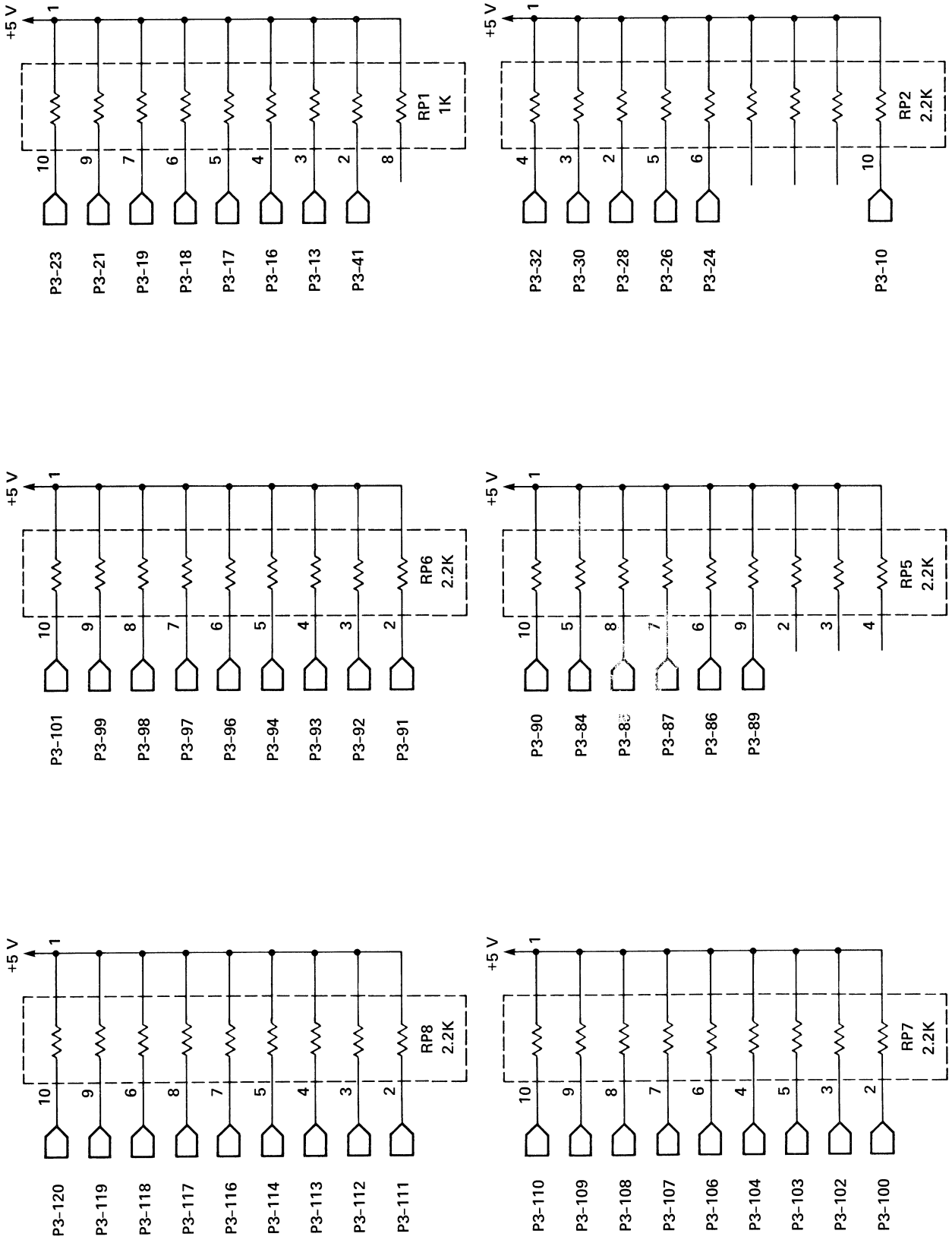


Figure D-8b. Main Motherboard Termination and Console Switch Circuitry.

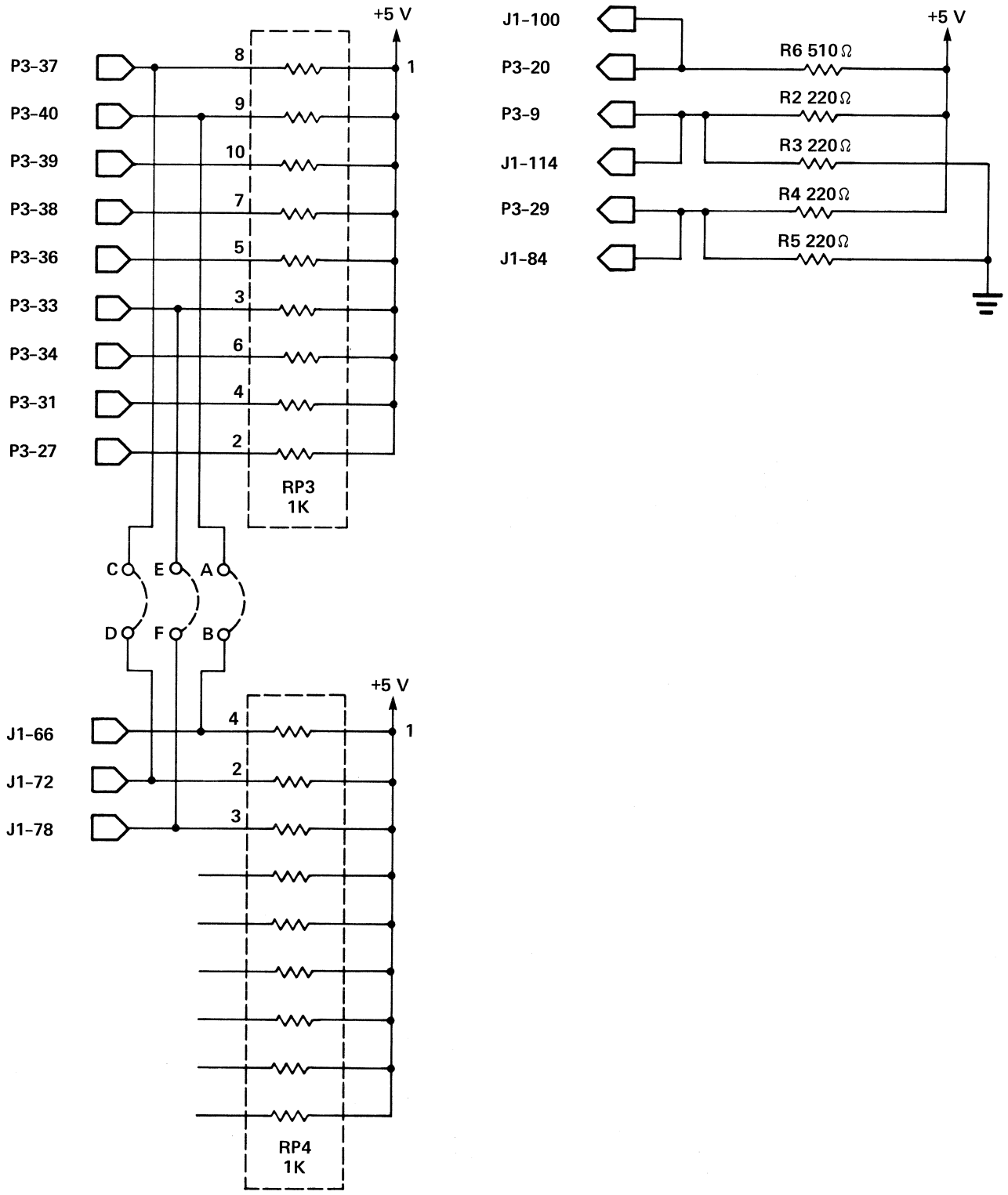


Figure D-8c. Main Motherboard Termination and Console Switch Circuitry.

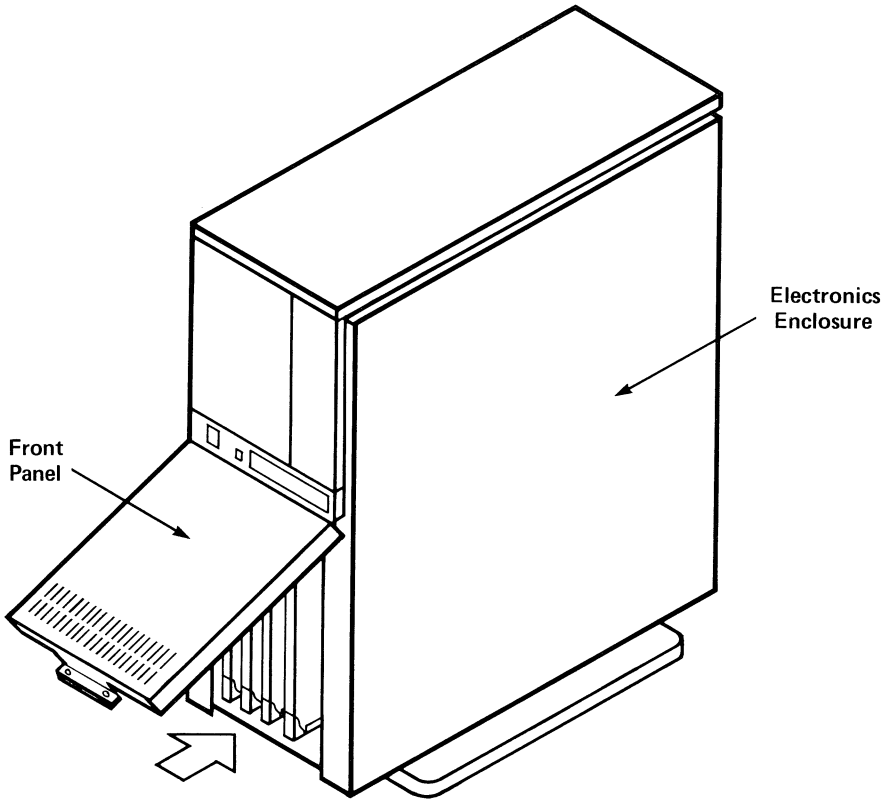
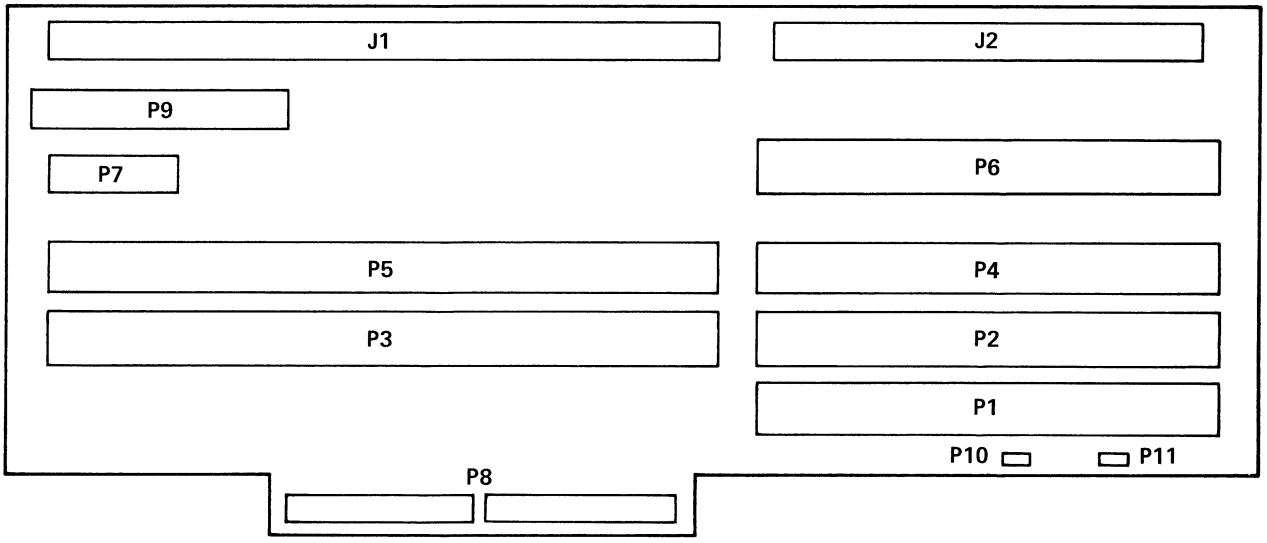


Figure D-9. Front Panel of the Monitor Form Electronics Enclosure Removed, Allowing Access to Boards.



P1 RAM Expansion Board
P2 CPU Board
P3 CPU Board
P4 I/O Memory Board
P5 I/O Memory Board
P6 Video Control Board
P7 Video Control Board
P8 Power Supply
P9 Video Monitor Cable
P10 Reset Button
P11 Power On Switch
J1 I/O Extender Board
J2 I/O Extender Board

Figure D-10. Main Motherboard Connector Locations.

Table D-4 lists Main motherboard connectors, a source or destination for each, and the number of pins for each connector. Table D-5 lists all signals found on the Main motherboard.

Table D-4. Main Motherboard Connectors.

Number	Board	Pins
P1	RAM Expansion board	80
P2	Processor board	80
P3	Processor board	120
P4	I/O Memory board	80
P5	I/O Memory board	120
P6	Video Control board	80
P7	Video Control board	20
P8	Power Cable	24
P9	Video Monitor Cable	68
P10	Reset Button	2
P11	Power On Switch	2
J1	I/O Extender board	120
J2	I/O Extender board	80

Table D-5. Main Motherboard Wire List. (Page 1 of 21)

Ctr*	Signal and Pin Numbers							
	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
P1	1	2	3	4	77	78	79	80
P2					77	78	79	80
P3	1	2	3	4				
P4					77	78	79	80
P5	1	2	3	4				
P6	1	2	3	4	77	78	79	80
P7								
P8	1	2	3	10	18	20	22	7
P9								
P10								
J1								
J2								
J3								
J4								
P11								
P12								
P13								
P14								
P15								
P16								

Ctr	Signal and Pin Numbers						
	+12V	+12V	+12V	+12V	-12V	-12V	-12V
P1	67	68	69	70	5	6	73
P2	67	68	69	70			
P3					5	6	
P4	67	68	69	70			73
P5					5	6	
P6	67	68	69	70	5	6	
P7	34						
P8	5	6			8		
P9	20	33					
P10							
J1							
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

* Ctr = connector

Table D-5. Main Motherboard Wire List. (Page 2 of 21)

Ctr	Signal and Pin Number					
	-12V	+32V	-32V	78 KHZ+	ACK-	AD10-
P1	74					
P2				13		
P3						26
P4	74			13		
P5					86	
P6						
P7						
P8		14	12			
P9		17	19			
P10						
J1						94
J2					53	
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Ctr	Signal and Pin Number					
	AD11-	AD12-	AD13-	ADR0-	ADR1-	ADR2-
P1						
P2						
P3	28	30	32	102	101	100
P4						
P5						
P6						
P7						
P8						
P9						
P10						
J1	90	86	82	32	34	36
J2						
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Table D-5. Main Motherboard Wire List. (Page 3 of 21)

Ctr	Signal and Pin Number					
	ADR3-	ADR4-	ADR5-	ADR6-	ADR7-	ADR8-
P1						
P2						
P3	99	98	97	96	94	93
P4						
P5						
P6						
P7						
P8						
P9						
P10						
J1	38	40	42	44	46	48
J2						
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Ctr	Signal and Pin Number						
	ADR9-	ADRA-	ADRB-	ADRC-	ADRD-	ADRE-	ADRF
P1	92	91	90	89	88	87	86
P2							
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	50	52	54	56	58	60	62
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 4 of 21)

Ctr	Signal and Pin Number						
	AUDIO+	BCLK-	BD1RAM-	BD2RAM-	BEOP-	BHEN-	BMR
P1				9			
P2			4	3			
P3		9				24	
P4	17		4		8		76
P5							
P6							
P7							
P8							
P9	25						
P10							
J1		114				92	
J2					74		80
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number							
	BPRNO	BREQO-	BUS0+	BUS1+	BUS2+	BUS3+	BUS4+	BUS5+
P1								
P2								
P3	11	14						
P4								
P5			94	99	96	100	97	101
P6								
P7								
P8								
P9								
P10								
J1	118	120						
J2			61	67	63	66	62	68
J3								
J4								
P11								
P12								
P13								
P14								
P15								
P16								

Table D-5. Main Motherboard Wire List. (Page 5 of 21)

Ctr	Signal and Pin Number						
	BUS6+	BUS7+	BUS8+	BUS9+	BUSA+	BUSB+	BUSC+
P1							
P2							
P3							
P4							
P5	98	102	107	111	106	110	104
P6							
P7							
P8							
P9							
P10							
J1							
J2	64	70	72	79	73	78	71
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	BUSD+	BUSE+	BUSF+	BUSY-	CAS0-	CAS1-	CAS2-
P1							
P2					22	21	20
P3				13			
P4					22	21	20
P5	109	103	108				
P6							
P7							
P8							
P9							
P10							
J1				112			
J2	77	69	76				
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 6 of 21)

Ctr	Signal and Pin Number						
	CAS3-	CAS4-	CAS5-	CAS6-	CAS7-	CBRQ-	CCLK-
P1		22	21	20	19		
P2	19	18	17	16	14		
P3						27	29
P4	19						
P5							
P6							
P7							
P8							
P9							
P10							
J1						88	84
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number					
	CNTRL-	COLMPX-	COMMTIMING	CRTOR-	CTSA+	CTSB+
P1		12				
P2		6	75			
P3						
P4		6	75			
P5	88				12	24
P6						
P7				16		
P8						
P9				16		
P10						
J1						
J2	54				30	9
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Table D-5. Main Motherboard Wire List. (Page 7 of 21)

Ctr	Signal and Pin Number						
	DAT0-	DAT1-	DAT2-	DAT3-	DAT4-	DAT5-	DAT6-
P1							
P2							
P3	120	119	118	117	116	114	113
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	2	4	7	6	8	10	12
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	DAT7-	DAT8-	DAT9-	DATA-	DATB-	DATC-	DATD-
P1							
P2							
P3	112	111	110	109	108	107	106
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	14	16	18	20	22	24	26
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 8 of 21)

Ctr	Signal and Pin Number					
	DATE-	DATF-	DCDA+	DCDB+	DCIRDY+	DISKACK-
P1						
P2						
P3	104	103			56	49
P4						
P5			22	31	56	49
P6						
P7						
P8						
P9						
P10						
J1	28	30				
J2			22	12		
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Ctr	Signal and Pin Number						
	DISKRQ+	DMACS-	DMACTCS-	DREQ-	DSRA+	DSRB+	DTRA+
P1							
P2							
P3	50	59	58				
P4							
P5	50	59	58	69	16	29	21
P6							
P7							
P8							
P9							
P10							
J1							
J2				51	29	10	28
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 9 of 21)

Ctr	Signal and Pin Number						
	DTRB+	ENBL-	EOP-	FASTIO+	GACCS-	GND	GND
P1						7	8
P2						5	
P3			77	57		7	8
P4					18	5	
P5	33	52	77	57		7	8
P6			11		12	7	8
P7						2	5
P8						4	9
P9						2	5
P10							
J1						1-5	9-119
J2	11	52				5	15
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number								
	GND	GND	GND	GND	GND	GND	GND	GND	GND
P1	15	25	35		45		55	65	66
P2	15	25	35		45		55	65	66
P3	15	25	35		45		55	65	
P4	15	25	35		45		55	65	66
P5	15	25	35		45		55	65	
P6	15	25	35	43	45	47	55	65	66
P7	9	10	15	17	18	19	20	65	
P8	11	13	15	17	19	21	23	24	
P9	10	9	15	18	26	28	30	32	
P10									
J1									
J2	25	35	45	55	65	75			
J3									
J4									
P11									
P12									
P13									
P14									
P15									
P16									

Table D-5. Main Motherboard Wire List. (Page 10 of 21)

Ctr	Signal and Pin Number							
	GND	GND	GND	GND	GND	GND	GND	GND
P1	71	72						
P2	71	72						
P3			75	85	95	105	115	
P4	71	72						
P5			75	85	95	105		
P6	71	72					115	18
P7								
P8								
P9								
P10								
J1								
J2								
J3								
J4								
P11								
P12								
P13								
P14								
P15								
P16								

Ctr	Signal and Pin Number							
	GND	GND	HIP+	HORDR+	HORDR-	INH1-	INH2-	INIT
P1			23					
P2			23					
P3								
P4			23					
P5								
P6	21	24						
P7				11	13			
P8								
P9				11	13			
P10								
J1								
J2								
J3								
J4								
P11								
P12								
P13								
P14								
P15								
P16								

Table D-5. Main Motherboard Wire List. (Page 11 of 21)

Ctr	Signal and Pin Number							
	INRQ-	INT0-	INT1B-	INT2-	INT3-	INT4B-	INT5-	INT6-
P1								
P2								
P3		41	40	39	38	37	36	34
P4								
P5	92		40		87	37		
P6								
P7								
P8								
P9								
P10								
J1		64		68	70		74	76
J2	60							
J3								
J4								
P11								
P12								
P13								
P14								
P15								
P16								

Ctr	Signal and Pin Number						
	INT7B-	INTA-	IOB0+	IOB1+	IOB2+	IOB3+	IOB4+
P1							
P2							
P3	33	31	68	67	66	64	63
P4							
P5	34		68	67	66	64	63
P6							
P7							
P8							
P9							
P10							
J1		80					
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 12 of 21)

Ctr	Signal and Pin Number						
	IOB5+	IOB6+	IOB7+	IOBCS+	IOCS-	IOR-	IORC-
P1							
P2							
P3	62	61	60	53	70	54	18
P4							
P5	62	61	60	53	70	54	
P6						46	
P7							
P8							
P9							
P10							
J1							104
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	IOW-	IOWC-	KBDI-	KBDO-	LA0+	LA1+	LA2+
P1	19				64	63	62
P2					64	63	62
P3	76						
P4	76				64	63	62
P5	14		41	46			
P6					64	63	62
P7							
P8							
P9			27	31			
P10							
J1	106						
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 13 of 21)

Ctr	Signal and Pin Number							
	LA2+	LA3+	LA4+	LA5+	LA6+	LA7+	LA8+	LA9+
P1	62	61	60	59	58	57	56	54
P2	62	61	60	59	58	57	56	54
P3								
P4	62	61	60	59	58	57	56	54
P5								
P6	62	61	60	59	58	57	56	54
P7								
P8								
P9								
P10								
J1								
J2								
J3								
J4								
P11								
P12								
P13								
P14								
P15								
P16								

Ctr	Signal and Pin Number						
	LA10+	LA11+	LA12+	LA13+	LAA+	LAB+	LAC+
P1	47	46	44	43	53	52	51
P2	47	46	44	43	53	52	51
P3							
P4	47	46	44	43	53	52	51
P5							
P6					53	52	51
P7							
P8							
P9							
P10							
J1							
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 14 of 21)

Ctr	Signal and Pin Number						
	LAD+	LAE+	LAF+	LBHEN+	LOP+	LPT SELECT+	
P1	50	49	48		24		
P2	50	49	48		24		
P3				46			
P4	50	49	48		24	16	
P5							
P6	50	49	48				
P7							
P8							
P9							
P10							
J1							
J2						50	
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	LPT0	LPT1+	LPT2+	LPT3+	LPT4+	LPT5+	LPT6+
P1							
P2							
P3							
P4							
P5	117	112	118	113	120	114	119
P6							
P7							
P8							
P9							
P10							
J1							
J2	33	36	39	43	44	46	47
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 15 of 21)

Ctr	Signal and Pin Number					
	LPT7+	LPTACK-	LPTBUSY+	MB10-	MEM0+	MEM1+
P1	116				42	41
P2					42	41
P3				82		
P4			3		42	41
P5		74		82		
P6					42	41
P7						
P8						
P9						
P10						
J1						
J2	48	37	41			
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Ctr	Signal and Pin Number						
	MEM2+	MEM3+	MEM4+	MEM5+	MEM6+	MEM7+	MEM8+
P1	40	39	38	37	36	34	33
P2	40	39	38	37	36	34	33
P3							
P4	40	39	38	37	36	34	33
P5							
P6	40	39	38	37	36	34	33
P7							
P8							
P9							
P10							
J1							
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 16 of 21)

Ctr	Signal and Pin Number						
	MEM9+	MEMA+	MEMB+	MEMC+	MEMCLK+	MEMD+	MEME+
P1	32	31	30	29		28	27
P2	32	31	30	29		28	27
P3					73		
P4	32	31	30	29		28	27
P5					73		
P6	32	31	30	29	9	28	27
P7							
P8							
P9							
P10							
J1							
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	MEMF+	MR-	MRDC-	MW-	MWINH-	MWTC-	NMI+
P1	26	10					
P2	26	1					
P3			16	48	80	17	71
P4	26	1					
P5				48	80	110	71
P6	26	10					
P7							
P8							
P9							
P10							
J1			108				
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 17 of 21)

Ctr	Signal and Pin Number					
	NO PAPER+	ODDP+	PAREN-	PERINT-	PICCS-	PROMEXDC-
P1						11
P2						8
P3		51	84	79	72	
P4	2					
P5		51	84	79	72	
P6						
P7						
P8						
P9						
P10						
J1						
J2	49					
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Ctr	Signal and Pin Number					
	RAHIWE-	RALOWE-	RARAS-	RDHIPEA-	RDLOPEA-	RDSTB-
P1	18	17	14			
P2	11	12	7			
P3				44	47	
P4	11	12	7			
P5				44	47	93
P6						
P7						
P8						
P9						
P10						
J1						
J2						59
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Table D-5. Main Motherboard Wire List. (Page 18 of 21)

Ctr	Signal and Pin Number						
	RESET-	RFDONE-	RFGO-	RINGA+	RINGB+	RTSA+	RTSB+
P1		13	16				
P2		10	9				
P3	83						
P4		10	9				
P5	83			23	32	20	36
P6	13						
P7							
P8							
P9							
P10							
J1							
J2				24	13	26	7
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	RXCA+	RXCB+	RXDA-	RXDB-	SELF-	SELW-	SFO
P1							
P2							
P3							
P4							14
P5	13	28	11	26	89	90	
P6							
P7							
P8							16
P9							
P10							
J1							
J2	18	8	16	4	57	56	
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 19 of 21)

Ctr	Signal and Pin Number						
	SPARE	SPARE	SIOACK-	SIORQ+	SRDA+	SRDB-	STDA+
P1							
P2	76						
P3		22	42	43			
P4							
P5			42	43	17	30	18
P6							
P7							
P8							
P9							
P10							
J1		96					
J2					14	6	17
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	STDB-	STROBE-	TO+	TCLK+	TCLK-	TEST	TXCA+
P1							
P2							
P3			81			74	
P4							
P5	38	38	81	10	9		14
P6							
P7							
P8							
P9							
P10							
J1							
J2	2	31		21	19		20
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-5. Main Motherboard Wire List. (Page 20 of 21)

Ctr	Signal and Pin Number					
	TXCB+	TXDA-	TXDB-	VERT DR+	VERT DR-	VIDA+
P1						
P2						
P3						
P4						
P5	27	19	39			
P6						
P7				12	14	1
P8						
P9				12	14	1
P10						
J1						
J2	1	23	3			
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Ctr	Signal and Pin Number					
	VIDA-	VIDACK-	VIDB+	VIDB-	VIDRQ+	WAIT-
P1						
P2					2	
P3		78				52
P4						
P5						
P6		17			16	44
P7	3		4	6		
P8						
P9	3		4	6		
P10						
J1						
J2						
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Table D-5. Main Motherboard Wire List. (Page 21 of 21)

Ctr	Signal and Pin Number	
	WRSTB-	XACK-
P1		
P2		
P3		20
P4		
P5	91	
P6		
P7		
P8		
P9		
P10		
J1		100
J2	58	
J3		
J4		
P11		
P12		
P13		
P14		
P15		
P16		

The Multibus motherboard, with one installed Multibus board, is shown in Figure D-6. Like the Main motherboard, the Multibus motherboard plugs into the I/O Extender board. It provides a back for the Multibus card cage and is an interface between Multibus boards and the rest of the workstation.

In addition to carrying signals and power for up to five Multibus boards, the Multibus motherboard contains Multibus priority resolution logic. This logic controls bus access priority for up to six Multibus masters, one of which is the workstation itself. Multibus masters are described in Section 2 "Functions and Interfaces." Bus access priority circuitry is shown in Figure D-11 and described below.

Bus Access Priority Logic. As shown in Figure D-11, encoder U1 determines whether one or more of the six Multibus request lines (BREQ0- through BREQ5-) are active, assigns a priority if more than one signal is active, and sends a binary

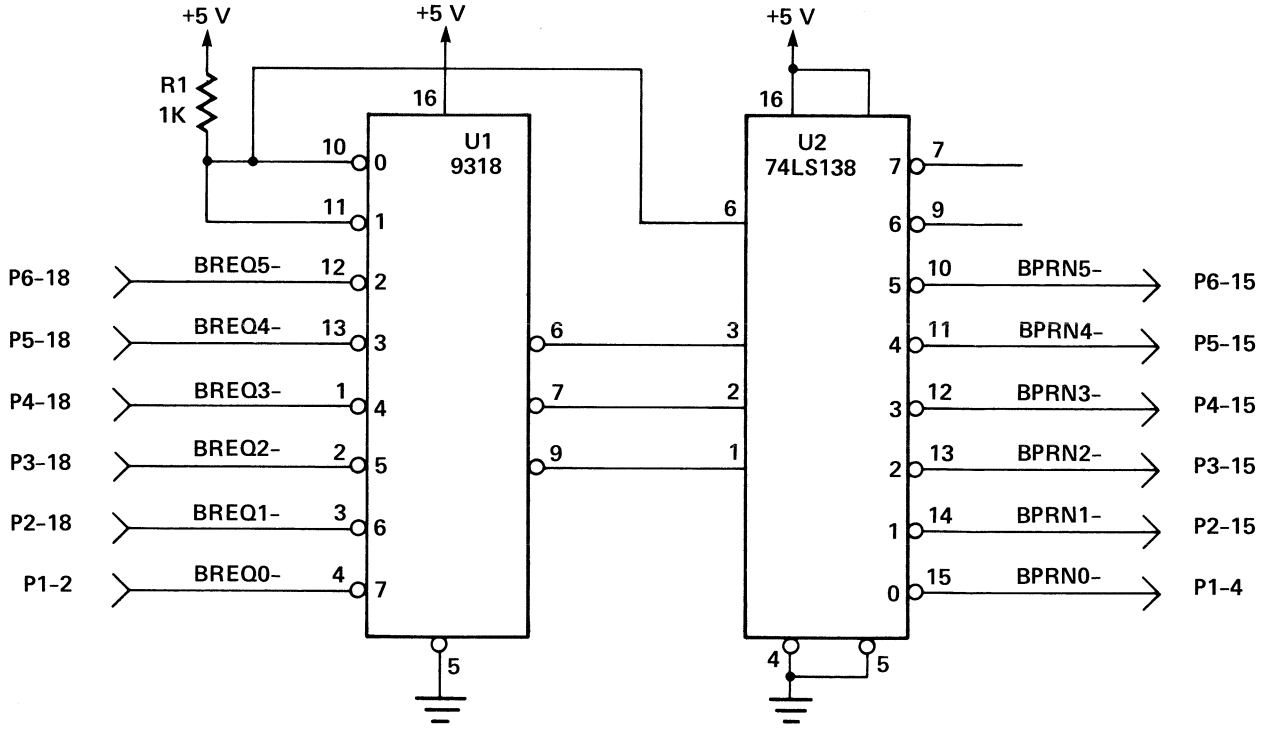


Figure D-11. Multibus Priority Resolution Logic.

code to U2, corresponding to either the active Multibus request line or the Multibus request line with the highest priority. U2 then asserts the corresponding Bus Priority In (BPRN0- through BPRN5-) signal. Bus request prioritization is assigned as follows:

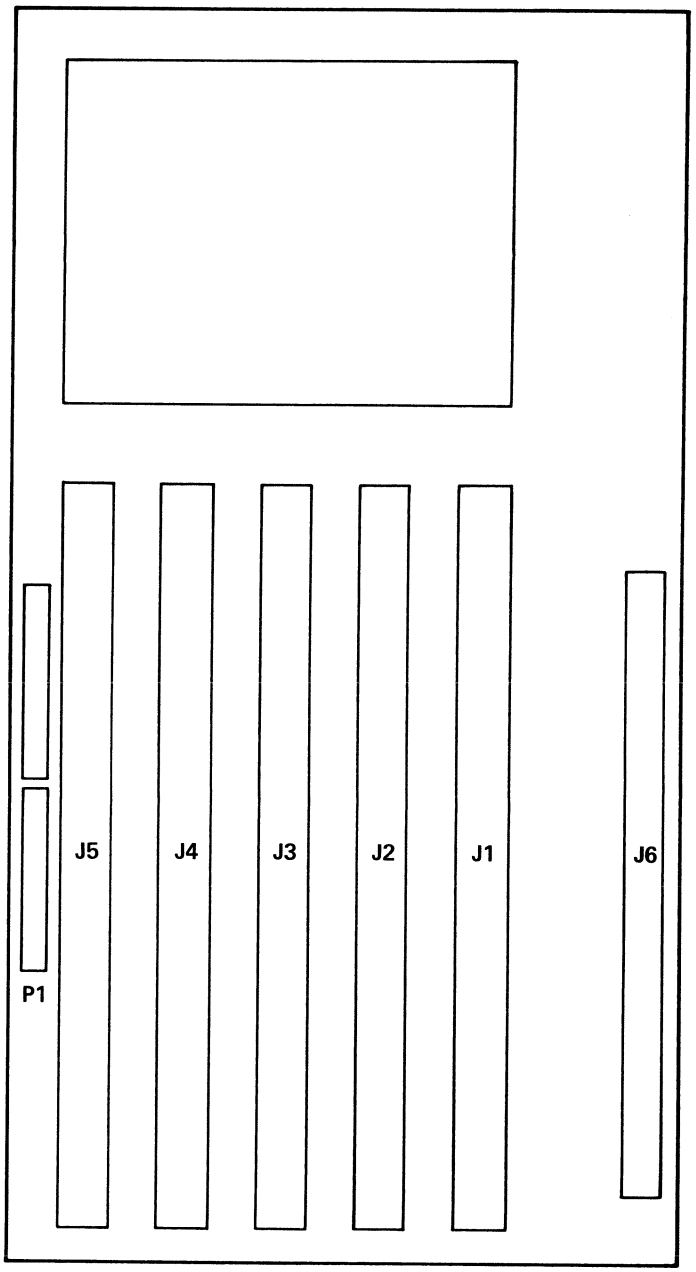
Line	Priority
BREQ0-	highest
BREQ1-	↓
BREQ2-	↓
BREQ3-	↓
BREQ4-	↓
BREQ5-	lowest

Since the monitor form fits into the Multibus request structure, BREQ0- is assigned to the monitor form of the IWS workstation, which is recognized as another Multibus board, while BREQ1- through BREQ5- are assigned to the J1 through J5 Multibus slots.

Multibus Motherboard Wire List. Figure D-12 shows connector locations on the Multibus motherboard. Table D-6 lists connectors, a source or destination for each, and the number of pins for each connector. Table D-7 lists all signals found on the Multibus motherboard. More information on Multibus can be found under "Multibus," below, and in Section 2," Functions and Interfaces."

Table D-6. Multibus Motherboard Connectors.

Number	Board	Pin
P1	Power Supply	24, 24
J1	Multibus Board	84
J2	Multibus Board	84
J3	Multibus Board	84
J4	Multibus Board	84
J5	Multibus Board	84
J6	I/O Extender Board	120



J1, J2, J3, J4, J5 Multibus Board Slots
J6 I/O Extender Board
P1 Power Supply

Figure D-12. Multibus Motherboard Connector Locations.

Table D-7. Multibus Motherboard Wire List. (Page 1 of 11)

Ctr*	Signal and Pin Numbers							
	+5V	+5V	+5V	+5V	-10V	+12V	-12V	AD10-
P1								28
P2								
P3								
P4								
P5								
P6								
P7								
P8								
P9								
P10								
J1	3,4,5	6,81	82,83	84	77,78	7,8	79,80	28
J2	3,4,5	6,81	82,83	84	77,78	7,8	79,80	28
J3	3,4,5	6,81	82,83	84	77,78	7,8	79,80	28
J4	3,4,5	6,81	82,83	84	77,78	7,8	79,80	28
J5	3,4,5	6,81	82,83	84	77,78	7,8	79,80	28
J6	1,3,7	10,81	20,22	2		5,6	8	
P11								
P12								
P13								
P14								
P15								
P16								

* Ctr = connector

Table D-7. Multibus Motherboard Wire List. (Page 2 of 11)

Ctr	Signal and Pin Number						
	AD11-	AD12-	AD13-	ADR0-	ADR1-	ADR2-	ADR3-
P1	32	36	40	90	88	86	84
P2							
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	30	32	34	57	58	55	84
J2	30	32	34	57	58	55	84
J3	30	32	34	57	58	55	84
J4	30	32	34	57	58	55	84
J5	30	32	34	57	58	55	84
J6							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-7. Multibus Motherboard Wire List. (Page 3 of 11)

Ctr	Signal and Pin Number						
	ADR4-	ADR5-	ADR6-	ADR7-	ADR8-	ADR9-	ADRA-
P1	82	80	78	76	74	72	70
P2							
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	53	54	51	52	49	50	47
J2	53	54	51	52	49	50	47
J3	53	54	51	52	49	50	47
J4	53	54	51	52	49	50	47
J5	53	54	51	52	49	50	47
J6							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-7. Multibus Motherboard Wire List. (Page 4 of 11)

Ctr	Signal and Pin Number						
	ADRB-	ADRC-	ADRD-	ADRE-	ADRF-	BCLK-	BHEN-
P1	68	66	61	62	60	8	30
P2							
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	48	45	46	43	44	13	27
J2	48	45	46	43	44	13	27
J3	48	45	46	43	44	13	27
J4	48	45	46	43	44	13	27
J5	48	45	46	43	44	13	27
J6							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-7. Multibus Motherboard Wire List. (Page 5 of 11)

Ctr	Signal and Pin Number						
	BUSY-	CBRQ-	CCLK-	DAT0-	DAT1-	DAT2-	DAT3-
P1	10	34	38	120	118	113	116
P2							
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	17	29	31	73	74	71	72
J2	17	29	31	73	74	71	72
J3	17	29	31	73	74	71	72
J4	17	29	31	73	74	71	72
J5	17	29	31	73	74	71	72
J6							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-7. Multibus Motherboard Wire List. (Page 6 of 11)

Ctr	Signal and Pin Number						
	DAT4-	DAT5-	DAT6-	DAT7-	DAT8-	DAT9-	DATA-
P1	114	112	110	108	106	104	102
P2							
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	69	70	67	68	65	66	63
J2	69	70	67	68	65	66	63
J3	69	70	67	68	65	66	63
J4	69	70	67	68	65	66	63
J5	69	70	67	68	65	66	63
P11							
P12							
P13							
P14							
P15							
P16							

Table D-7. Multibus Motherboard Wire List. (Page 7 of 11)

Ctr	Signal and Pin Number					
	DATB-	DATC-	DATD-	DATE-	DATF-	GND
P1	100	98	96	94	92	1-119
P2						
P3						
P4						
P5						
P6						
P7						
P8						
P9						
P10						
J1	64	61	62	59	60	1,2,11,12,75
J2	64	61	62	59	60	1,2,11,12,75
J3	64	61	62	59	60	1,2,11,12,75
J4	64	61	62	59	60	1,2,11,12,75
J5	64	61	62	59	60	1,2,11,12,75
J6						4,9,11,13,15
P11						
P12						
P13						
P14						
P15						
P16						

Table D-7. Multibus Motherboard Wire List. (Page 8 of 11)

Ctr	Signal and Pin Number						
	GND	GND	GND	INH1-	INH2-	INIT-	INT0-
P1	119			20	24	6	58
P2							
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	76,85	86		24	26	14	41
J2	76,85	86		24	26	14	41
J3	76,85	86		24	26	14	41
J4	76,85	86		24	26	14	41
J5	76,85	86		24	26	14	41
J6	17,19	21,23,24					
P11							
P12							
P13							
P14							
P15							
P16							

Table D-7. Multibus Motherboard Wire List. (Page 9 of 11)

Ctr	Signal and Pin Number					
	INT1B-	INT2-	INT3-	INT4B-	INT5-	INT6-
P1	56	54	52	50	48	46
P2						
P3						
P4						
P5						
P6						
P7						
P8						
P9						
P10						
J1	42	39	40	37	38	35
J2	42	39	40	37	38	35
J3	42	39	40	37	38	35
J4	42	39	40	37	38	35
J5	42	39	40	37	38	35
J6						
P11						
P12						
P13						
P14						
P15						
P16						

Table D-7. Multibus Motherboard Wire List. (Page 10 of 11)

Ctr	Signal and Pin Number					
	INT7B-	INTA-	IORC-	IOWC-	MRDC-	MWTC-
P1	44	42	18	16	14	12
P2						
P3						
P4						
P5						
P6						
P7						
P8						
P9						
P10						
J1	36	33	21	22	19	20
J2	36	33	21	22	19	20
J3	36	33	21	22	19	20
J4	36	33	21	22	19	20
J5	36	33	21	22	19	20
J6						
P11						
P12						
P13						
P14						
P15						
P16						

Table D-7. Multibus Motherboard Wire List. (Page 11 of 11)

Ctr	Signal and Pin Number	
	SPARE	XACK-
P1	26	22
P2		
P3		
P4		
P5		
P6		
P7		
P8		
P9		
P10		
J1	25	23
J2	25	23
J3	25	23
J4	25	23
J5	25	23
J6		
P11		
P12		
P13		
P14		
P15		
P16		

I/O Extender Board

The I/O Extender board provides a connection between the Main and Multibus motherboards, the video monitor, and external connectors, located on the rear panel of the electronics assembly. The I/O Extender board also contains six of the external connectors on the rear panel, as shown in Figure D-7, and an eight-position DIP switch at U1, also shown.

The six external connectors contained by the I/O Extender board are

- Communications Channel A
- Communications Channel B
- Parallel Printer Interface
- Disk Controller Interface
- Cluster Communications (two connectors)

Communications Channels A and B are RS-232-C interfaces, and the Disk Controller Interface is a DCI cable to a mass storage subsystem, or MSS. I/O Extender board connectors are shown in Figure D-13.

The two nine-pin connectors labeled Cluster Communications on the back panel, (connectors P4 and P5 on the I/O Extender board) can be used instead of the Communications Channel A for high-speed communications. To select the RS-422 channel for cluster communications, make sure that all switches on U1, the mode selector switch on the I/O Extender board, are set to ON. Since the monitor form is normally used as a cluster workstation, all switches set to ON is the normal setting. This setting configures Communications Channel A for half-duplex and connects surge protection diodes CR1 through CR9 to the channel. Figure D-14 is a schematic diagram of U1 circuitry.

I/O Extender board connectors are shown in Figure D-13. Table D-8 lists these connectors, their sources and/or destinations, and the number of pins for each connector. Table D-9 is a wire list for all the I/O Extender board connectors.

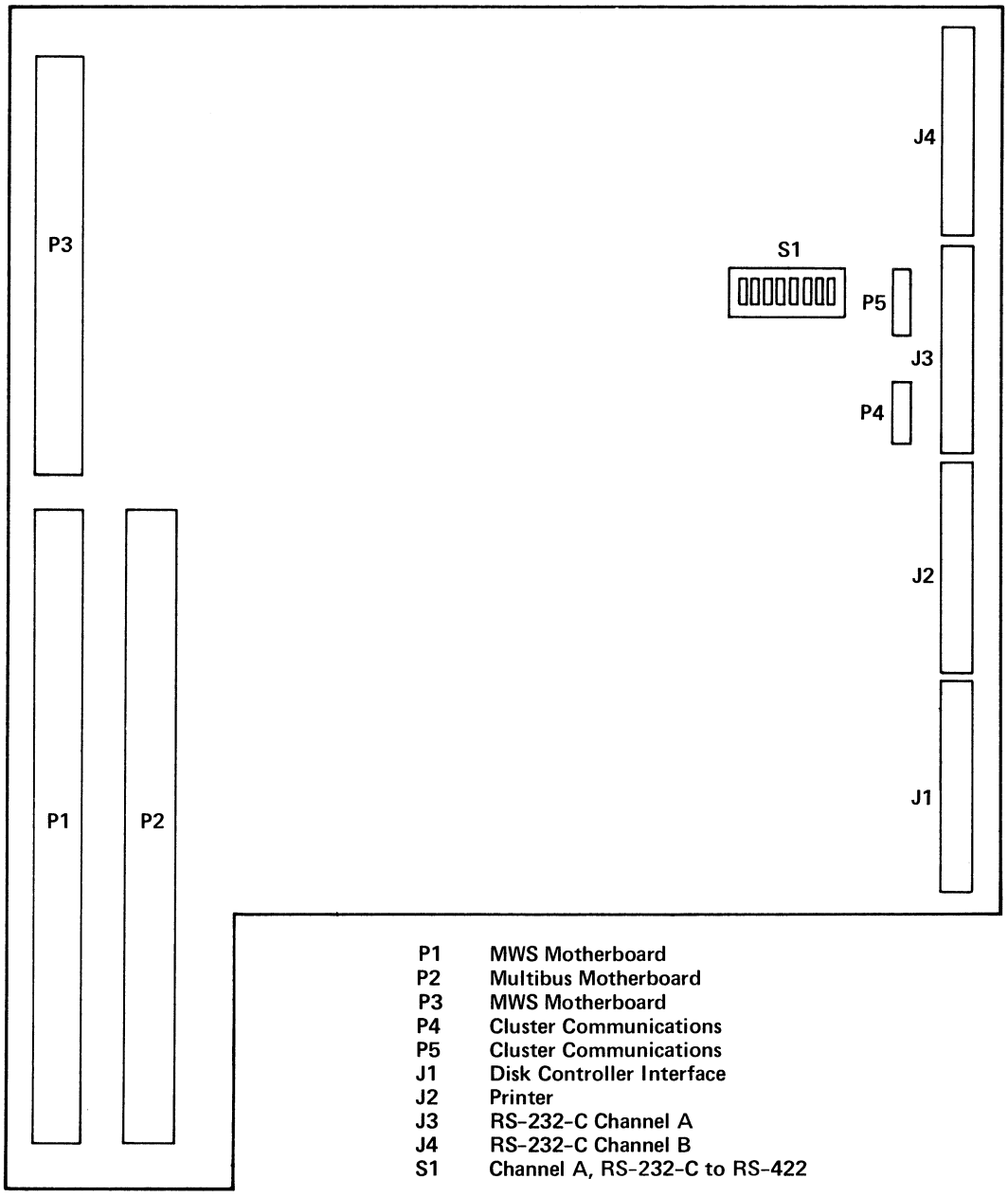


Figure D-13. I/O Extender Board Connector Locations.

Table D-8. I/O Extender Board Connectors.

Number	Board	Pins
P1	Main Motherboard	120
P2	Multibus Motherboard	120
P3	Main Motherboard	80
P4	Cluster Communications	9
P5	Cluster Communications	9
J1	Disk Controller Interface	50
J2	Printer	25
J3	Channel A	25
J4	Channel B	25

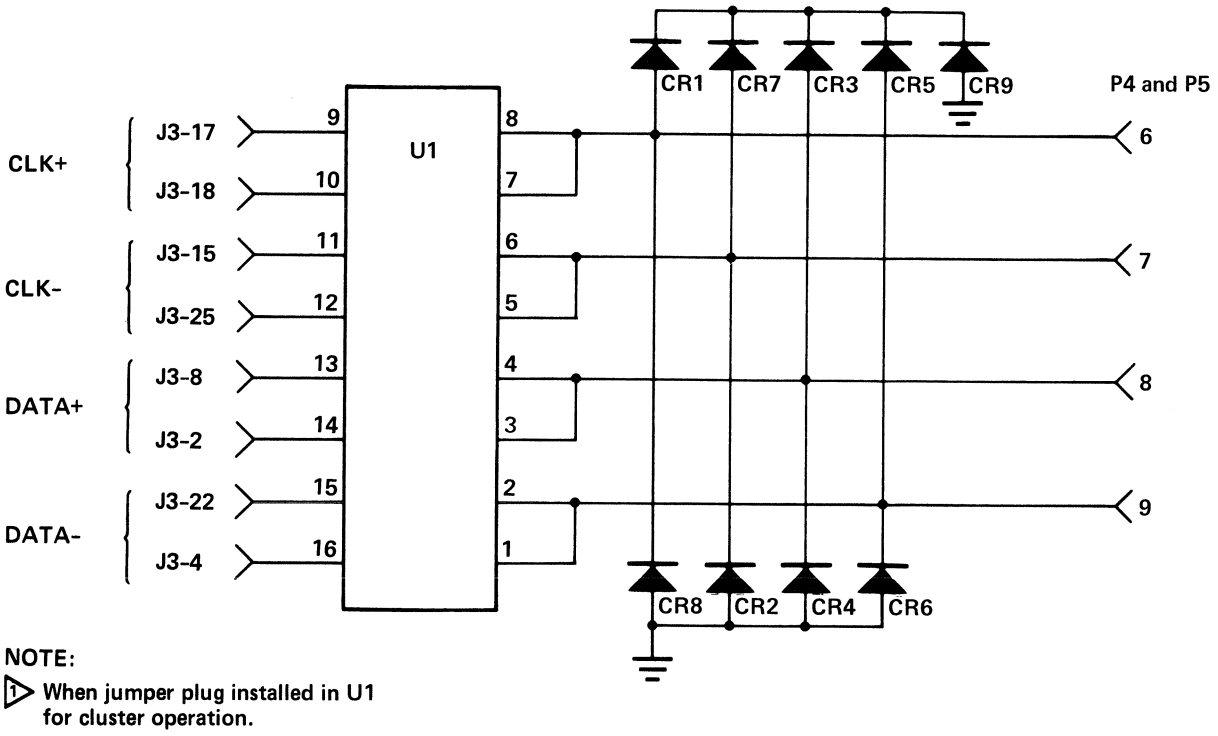


Figure D-14. I/O Extender Board U1 Mode Selector Switch Circuitry.

Table D-9. I/O Extender Board Wire List. (Page 1 of 12)

Ctr*	Signal and Pin Number						
	ACK-	AD10-	AD11-	AD12-	AD13-	ADR0-	ADR1-
P1		94	90	86	82	32	34
P2		28	32	36	40	90	88
P3	53						
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	2						
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	ADR2-	ADR3-	ADR4-	ADR5-	ADR6-	ADR7-	ADR8-
P1	36	38	40	42	44	46	48
P2	86	84	82	80	78	76	74
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1							
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

* Ctr = connector

Table D-9. I/O Extender Board Wire List. (Page 2 of 12)

Ctr	Signal and Pin Number						
	ADR9-	ADRA-	ADRB-	ADRC-	ADRD-	ADRE-	ADRF-
P1	50	52	54	56	58	60	64
P2	72	70	68	66	64	62	58
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1							
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	BCLK-	BEOP-	BHEN-	BMR-	BPRN0-	BREQ0-	BUS0+
P1	114		92		118	120	61
P2	8		30		4	2	
P3		74		80			
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1		48		50			24
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-9. I/O Extender Board Wire List. (Page 3 of 12)

Ctr	Signal and Pin Number						
	BUS1+	BUS2+	BUS3+	BUS4+	BUS5+	BUS6+	BUS7+
P1							
P2							
P3	67	63	66	62	68	64	70
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	10	8	43	41	28	26	12
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	BUS8+	BUS9+	BUSA+	BUSB+	BUSC+	BUSD+	BUSE+
P1							
P2							
P3	72	79	73	78	71	77	69
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	47	33	14	49	30	16	45
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-9. I/O Extender Board Wire List. (Page 4 of 12)

Ctr	Signal and Pin Number						
	BUSF+	BUSY-	CBRQ-	CCLK-	CNTRL-	CTSA+	CTSB+
P1		112	88	84			
P2		10	34	38			
P3	76				54	30	9
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	48				20	5	5
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	DAT0-	DAT1-	DAT2-	DAT3-	DAT4-	DAT5-	DAT6-
P1	2	4	7	6	8	10	12
P2	120	118	113	116	114	112	110
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1							
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-9. I/O Extender Board Wire List. (Page 5 of 12)

Ctr	Signal and Pin Number						
	DAT7-	DAT8-	DAT9-	DATA-	DATB-	DATC-	DATD-
P1	14	16	18	20	22	24	26
P2	108	106	104	120	100	98	96
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1							
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	DATE-	DATF-	DCDB+	DLDA+	DREQ-	DSRA+	DSRB+
P1	28	30					
P2	94	92					
P3			12	22	51	29	10
P4				8			
P5				8			
P6							
P7							
P8							
P9							
P10							
J1					35	6	
J2							
J3				8			
J4			8				6
P11							
P12							
P13							
P14							
P15							
P16							

Table D-9. I/O Extender Board Wire List. (Page 6 of 12)

Ctr	Signal and Pin Number							
	DTRA+	DTRB+	ENBL-	GROUND	GROUND	GROUND	GROUND	GROUND
P1				1,3,5,9	11,13,15	17,19,21	23,25,27	29,31,33
P2				1,3,5,7	9,11,13	15,17,19	21,23,25	27,29,31
P3	28	11	52	5,15	25,35	45,55	65,75	27
P4				1,2	3,4	5		
P5				1,2	3,4	5		
P6								
P7								
P8								
P9								
P10								
J1			18	1,3	5,7	9,11	13,15	17,19
J2				9,10	11,12	15,25		
J3	20			1,7				
J4		20		1,7				
P11								
P12								
P13								
P14								
P15								
P16								

Ctr	Signal and Pin Number						
	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
P1	35,37	39,41,43	45,47	49,51,53	55,57,59	61,63	65,67,69
P2	33,35	37,39,41	43,45,47	49,51,53	55,57,59	61,63	65,67,69
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1	21,23	25,27	29,31	34,36	38,40	42,44	46
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-9. I/O Extender Board Wire List. (Page 7 of 12)

Ctr	Signal and Pin Number					
	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
P1	71,73,75	77,79,81	83,85	87,89	91,93	95,97,99
P2	71,73,75	77,79,81	83,85	87,89	91,93	95,97
P3						
P4						
P5						
P6						
P7						
P8						
P9						
P10						
J1						
J2						
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Ctr	Signal and Pin Number						
	GROUND	GROUND	GROUND	GROUND	GROUND	INH1-	INH2-
P1	101,103	105,107	109,111	113,115	117,119	102	98
P2	99,101	103,105	107,109	111,115	117,119	20	24
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1							
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-9. I/O Extender Board Wire List. (Page 8 of 12)

Ctr	Signal and Pin Number						
	INIT-	INRQ-	INT0-	INT1B-	INT2-	INT3-	INT4B-
P1	116		64	66	68	70	72
P2	6		58	56	54	52	50
P3		60					
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1		6					
J2							
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	INT5-	INT6-	INT7B-	INTA-	IORC-	IOWL-	LPT SELECT+
P1	74	76	78	80	104	106	
P2	48	46	44	42	18	16	
P3							50
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1							
J2							22
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Table D-9. I/O Extender Board Wire List. (Page 9 of 12)

Ctr	Signal and Pin Number						
	LPT0+	LPT1+	LPT2+	LPT3+	LPT4+	LPT5+	LPT6+
P1							
P2							
P3	33	36	39	43	44	46	47
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1							
J2	1	2	3	4	5	6	7
J3							
J4							
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number					
	LPT7+	LPTACK-	LPTBUSY+	MRDC-	MWTC-	NO PAPER+
P1				108	110	
P2				14	12	
P3	48	37	41			49
P4						
P5						
P6						
P7						
P8						
P9						
P10						
J1						
J2	8	16	17			21
J3						
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Table D-9. I/O Extender Board Wire List. (Page 10 of 12)

Ctr	Signal and Pin Number						
	RDSTB-	RESERVED	RINGA+	RINGB+	RTSA+	RTSB+	RXCB+
P1		96					
P2		26					
P3	59		24	13	26	7	8
P4			9		9		
P5			9		9		
P6							
P7							
P8							
P9							
P10							
J1	39						
J2							
J3			22		4		
J4				22		4	17
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number						
	RXDA+	RXDB-	RXDA+	SELF-	SELW-	SPARES	SPARES
P1							
P2							
P3	16	4	18	57	56		
P4			6				
P5			6				
P6							
P7							
P8							
P9							
P10							
J1				4	37		
J2						13,18	19,20
J3	3		17			9,10,11	12,13
J4		3				9,10,11	13,18
P11							
P12							
P13							
P14							
P15							
P16							

Table D-9. I/O Extender Board Wire List. (Page 11 of 12)

Ctr	Signal and Pin Number						
	SPARES	SPARES	SPARES	SRDA+	SRDB-	STDA-	STDB-
P1							
P2							
P3							
P4							
P5							
P6							
P7							
P8							
P9							
P10							
J1							
J2	23,24						
J3	19,21	23,24	25				
J4	19,21	23,24	25				
P11							
P12							
P13							
P14							
P15							
P16							

Ctr	Signal and Pin Number					
	STROBE-	TCLK+	TCLK-	TXCB+	TXDA	TXDB-
P1						
P2						
P3	31	21	19			
P4		7	6			
P5		7	6			
P6						
P7						
P8						
P9						
P10						
J1						
J2	14					
J3		25				
J4						
P11						
P12						
P13						
P14						
P15						
P16						

Table D-9. I/O Extender Board Wire List. (Page 12 of 12)

Ctr	Signal and Pin Number		
	TXDA+	WRSTB-	XACK-
P1			100
P2			22
P3	20	58	
P4	7		
P5	7		
P6			
P7			
P8			
P9			
P10			
J1		22	
J2			
J3	15		
J4			
P11			
P12			
P13			
P14			
P15			
P16			

Multibus

Multibus is a means of interconnecting independently manufactured devices and allowing them to operate as if designed by a single manufacturer for a single system. The monitor form of the IWS workstation, with its five Multibus card slots, is for customers who wish to take full advantage of their Convergent workstation and Multibus applications hardware. This section provides a detailed description of Convergent Technologies' version of Multibus and supplements Section 4, "Processor Board," which contains further information on Multibus and system options.

The IEEE 796 Multibus standard (Appendix A) defines several levels of hardware compliance. The Convergent version of Multibus achieves the highest level of compliance to this standard, with the exception of memory address bits. (Convergent provides 20 instead of 24 bits.) Also, the CT-BUS provides 16 bits for data, 16 bits for I/O, and a V023E level of interrupt attribute compliance to the IEEE standard. For more information, refer to Section 4, "Processor Board."

Dual-Bus Architecture

Figure 1-1 in Section 1, "System Architecture," provides an architectural overview of the monitor form and the IWS workstation. Multibus interacts with the CT-BUS through exchange logic, command signals, and address signals.

Multibus devices, as shown in Figure 1-1, cannot directly access CT-BUS I/O resources; they are limited to accessing local memory. The workstation CPU, however, can access Multibus I/O resources. When a Multibus device accesses workstation local memory, a DMA chip places the workstation CPU in hold state to allow the access. Dual-bus architecture and Multibus accessing are further described in Section 2, "Functions and Interfaces, and in the following subsection.

Multibus Structure

The Multibus structure is designed using a master-slave concept, in which the master device in the system takes control of the bus, and the

slave device acts upon a command provided by the master. This master-slave relationship allows modules of different speeds and manufacturers to interface, using the same bus. The workstation CPU can function as either a master or a slave in Multibus transactions. Figure D-15 is an example of the Multibus master-slave relationship.

A master is any module having the ability to control the bus. The master obtains control by acquiring the bus through bus exchange logic and generating command signals and memory or I/O addresses. A master module is equipped with a CPU or logic dedicated to transferring data to and from the bus.

A slave is another type of module that can interface with the bus. Slave modules decode address lines, act upon command signals sent by the master or masters, and assert XACK (Transfer Acknowledge) when a memory or I/O transfer is completed. Each command (MRDC, IORDC, IOWTC, or INTA) on the Multibus is completed when the XACK signal goes active. It is the responsibility of the slave device in a Multibus transaction to assert XACK at the completion of a bus command. Slave modules are not capable of controlling the bus.

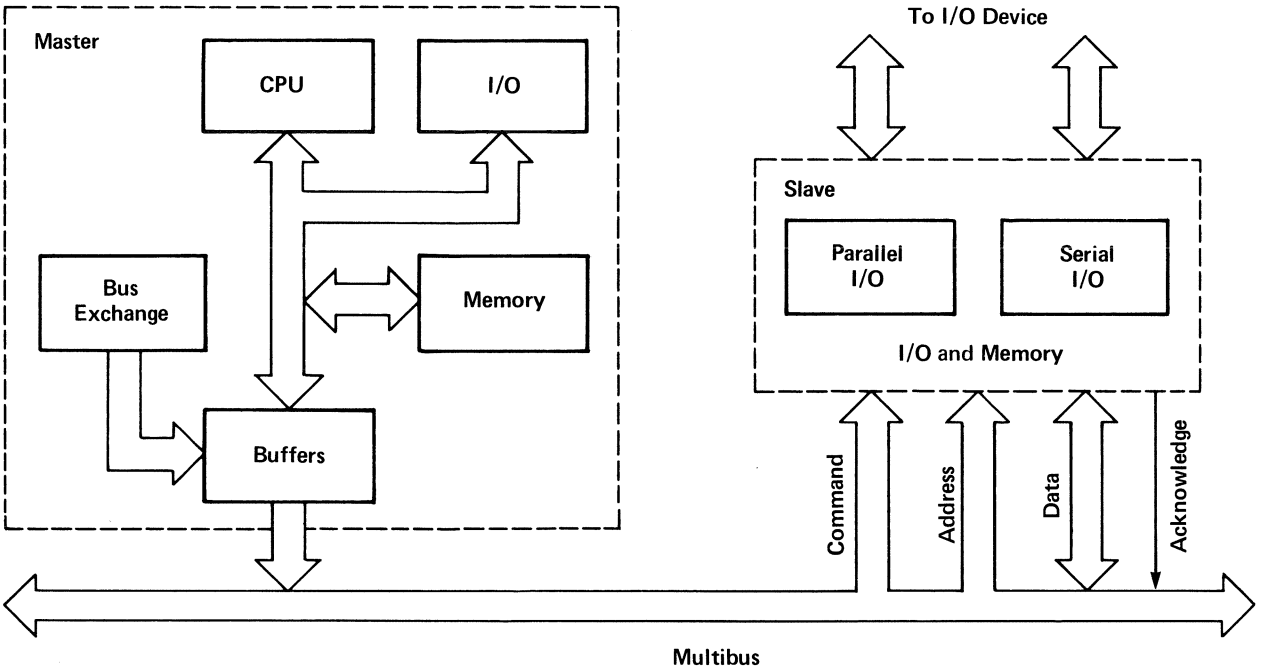


Figure D-15. Multibus Master-Slave Relationship.

Multibus Interface

As described under "Multibus Interface" in Section 4, "Processor Board," the Multibus interface operates in three separate modes:

- o independent mode
- o master mode
- o slave mode

In the independent mode, the Multibus and the CT-BUS are separate. In the master mode, the CT local bus controls Multibus and drives its command and address lines. In the slave mode, another Multibus master controls the CT-BUS and drives its command and address lines.

These three modes constitute three different types of data transfer. These three types of data transfer are implemented by use of signal and timing specifications listed in Section 2 of Appendix A, "IEEE 796 (Multibus) Standard."

In I/O bus cycles, for example, master modules have the option of generating either 8-bit or 16-bit addresses. Therefore, all I/O slaves must be capable of being configured to decode 8 address bits (ADR0 - ADR7) and ignore the upper 8 address bits, or to decode all 16 address bits (ADR0 - ADRF). If a board is specifically designed to decode a 16-bit address bus, it is not necessary to include an option to decode 8-bit addresses.

In summary: when transfers across the Multibus interface are controlled by the CT-BUS, either memory or I/O slave resources on the Multibus can be accessed. When a Multibus master controls the transfers, only memory can be accessed on the CT-BUS.

Multibus Master Access

With proper memory addressing and Processor board switch settings (see "Master Access Memory Mapping and Switch Settings," below), a Multibus user can access either memory and I/O devices on CT-BUS or memory and I/O devices on both CT-BUS and Multibus. If the MB10 bit in the I/O control register (port 56h) is not set, addresses generated from 0 to 7FFFF (high-order address bit

active low) cause access to CT-BUS local memory and I/O devices only.

Multibus Master Mode I/O Addressing. If bit 15 (Fh) is high , the Multibus is allowed master access to Multibus I/O devices

- If jumper option 3-2 is installed and jumper 1-2 is removed.
- If the MB10 bit in the I/O control register (port 56h) is enabled (bit C=1). (In this case, however, the Multibus is acquired for I/O addresses 8000h - FFFFh.)

These two conditions cause the Multibus I/O slave device to appear to the local CPU master as a local I/O device. It is then the responsibility of the slave device to assert XACK when the command is complete. For more information, see "Multibus Interface" in Section 4, "Processor Board."

Master Access Memory Mapping and Switch Settings. Memory window switch settings differ depending on the direction in which the transfer is made. The CPU can be switch-configured to acquire the Multibus at two different address boundaries, 512K or 768K, as shown in Figure D-16. In either case, the address is mapped to address 0 on the accessed Multibus device. Switches S3, S4, and S6 on the Processor board, as described below, control Multibus master access within these ranges.

768K Option

Switch	Position	State	Definition	
S3	1	OFF	Disables boundary	512K
S3	2	ON	Enables boundary	768K
S4	1	ON	Enables boundary	768K
S6	3	OFF	Enables Multibus acquisition.	

512K Option

Switch	Position	State	Definition	
S3	1	ON	Enables boundary	512K
S3	2	OFF	Disables boundary	768K
S4	1	ON	Disables boundary	768K
S6	3	OFF	Enables Multibus acquisition	

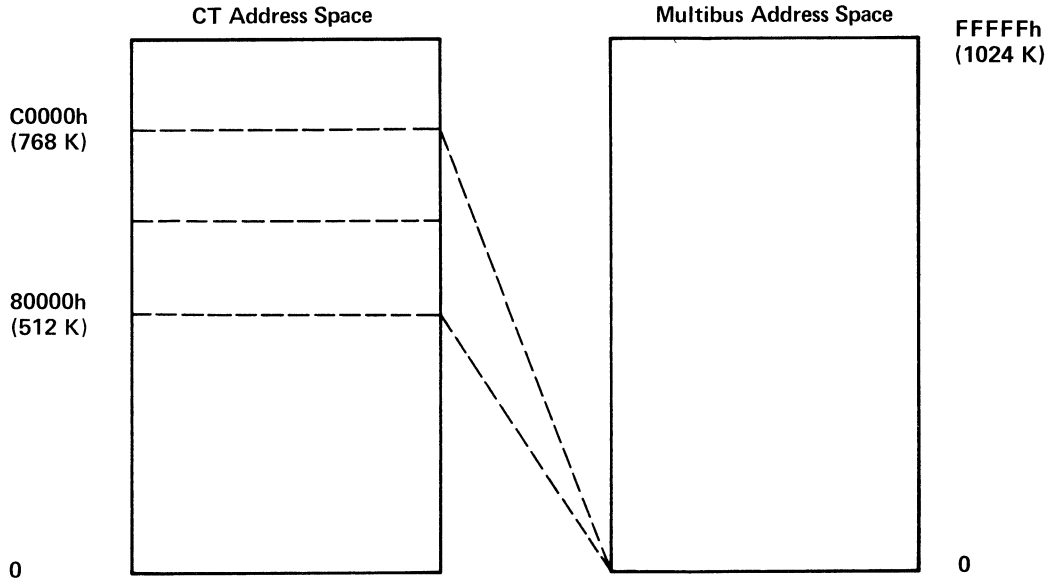


Figure D-16. Memory Mapping.

The upper limit of the Multibus memory space is determined by type of bootstrap ROM used in the workstation. Typically, the monitor form of the workstation uses a 2732 bootstrap ROM, which uses 8K of memory. Address space memory allocation for 1M byte is shown in Figure D-17.

Multibus Slave Access

Multibus slave access occurs when another Multibus master uses the CT-BUS memory. The

Processor board switches S2 and S6 determine specific memory ranges for this access.

The memory-mapping ranges for Multibus slave access to CT-BUS local memory are

1. 32K to 47K bytes,

2. 512K to 1024K bytes,

3. 1 and 2,
or
4. 0K bytes

When the local bus RAM is the slave, the XACK signal must be generated by CT-BUS logic. XACK signal generation is controlled by memory timing. The 8237 DMA Controller provides bus arbitration for the slave mode, in which addresses and commands come from the Multibus master and not from the DMA controller.

Slave mode bus arbitration is therefore assigned to channel 0 of the 8237. Multibus access to the local bus is given the highest-priority channel, because some Multibus devices (real-time, for example) do not have their own storage buffering and require fast access to local RAM. For all other DMA channels, addresses and commands are sent from the DMA controller during DMA transfers.

In slave mode, the Multibus master or masters are granted access to workstation RAM memory when two registers within the 8237-2 DMA controller have been initialized. Initializing the two registers can be done in two ways, either by linking the ASM-86 program to your application program,

```
MOV AL, 58H; DMA 0 MODE
OUT 16H, AL
XOR AL, AL
Enter the Debugger [Action (A)]
OUT 14H, AL; clear channel 0 mask bit
```

or by the Debugger method:

1. Enter the Debugger.

2. Write 58h to port 16h by entering 160 <-58 <RETURN>.

3. Write 00h to port 14h by entering 140 <-0 <RETURN>.

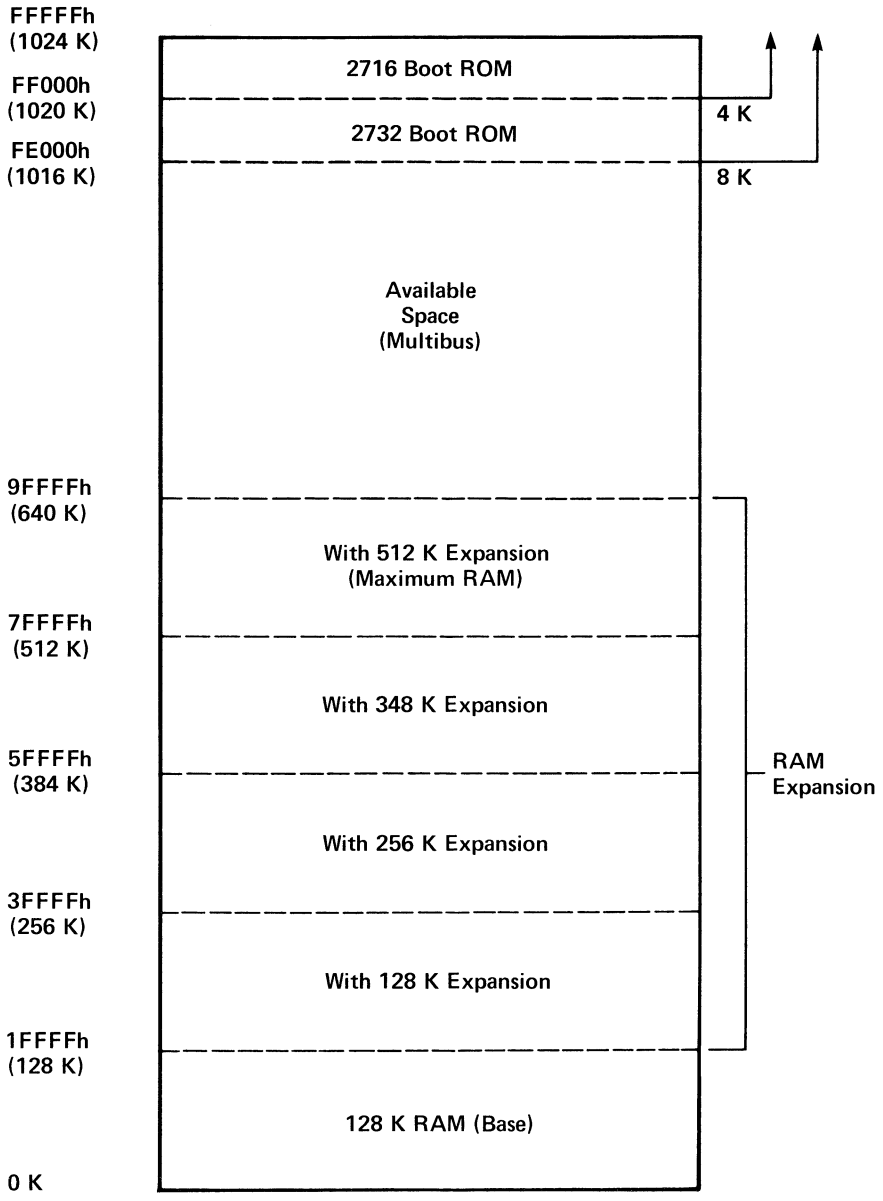


Figure D-17. 1M-byte Address Space Memory Allocation.

Figure 2-16 in Section 2, "Functions and Interfaces," shows 8237-2 register formats and explains bit assignments for ports 14h and 16h.

Slave Access Memory Mapping and Switch Settings. There are four choices of memory windows for another Multibus master to control the bus and use CT-BUS memory.

For Multibus slave access, the bits of S2 and S6 on the Processor board are set as follows:

Switch	Position	State	Definition
S2	1	ON	Multibus slave region at greater than 512K.
S2	4	OFF	32K to 48K Multibus slave region.
S6	4	ON	Always asserts Multibus CBRQ, the signal that indicates to the master in control that another master wants control of the bus.

GUIDELINES FOR CUSTOM HARDWARE APPLICATIONS

Introduction

For the many users of the monitor form of the IWS workstation who will develop or install special applications hardware, this subsection lists specific Convergent Technologies design features, suggests some sources for special parts, and presents an example of how a Multibus slot in the monitor form can be used in a simple application.

The monitor form allows users to take full advantage of its expanded Multibus features. The five Multibus card slots are supported by a connector panel design that allows each card and its external cabling to be handled as a separate module.

Figure D-6 shows the Multibus environment within the monitor form. Applications hardware can be developed, manufactured, and installed easily; and never has to compromise one Multibus application in order to implement another. Multibus P2 connector installation is convenient and wire wrap P2 connectors can be installed in two of the card slots, making development and fabrication of the applications hardware easier.

Multibus Applications for the Monitor Form

The Multibus applications for the monitor form of the IWS workstation have, in accordance with UL and FCC standards, met criteria for the design of safe, electrically quiet business machines with the following features:

- A tool other than a standard slotted screwdriver is required to reach the electrical components of the monitor form.
- Installed cabling has passed a 30 lb (13.6 kg) pull test without exposing the user to unsafe voltages.
- EMI radiated from the electronics is safely contained within the assembly. The interface cable exit is well shielded and grounded.
- Convergent Technologies hardware has high reliability. We realize that in complex systems, such as the monitor form of the IWS workstation, a failure can be difficult to

isolate. This is especially true for cables, which often fail intermittently. Convergent Technologies uses the highest quality cables and electrical hardware available.

- Cable hookups, frequently performed by users, are simple.
- The monitor form of the IWS workstation has a high immunity to ESD (electrostatic discharge).
- Convergent Technologies hardware is easy to install and low in cost.
- Convergent Technologies hardware is easy to fabricate and uses standard assembly methods and parts, which are much less likely to cause problems than are non-industry-tested parts.

Assembling the Monitor Form of the IWS Workstation

This section describes the tools, hardware, and procedures used for assembling the monitor form of the IWS workstation. It is intended to supplement, rather than replace, the Monitor Form Installation Guide.

Bulkhead Hardware

This subsection provides a description of the hardware used in monitor form bulkhead construction and contains part specification drawings and instructions for custom hardware development.

The back panel of the monitor form is covered by a single blank connector panel and referred to as a bulkhead. The bulkhead is fastened at the top with two Phillips screws and can be removed to expose the Multibus card cage and five Multibus card slots. When Multibus cards and their external cabling are installed in the Multibus card cage, smaller sizes of bulkheads can be used to cover the unused portion of the assembly's back panel as shown in Figure D-18.

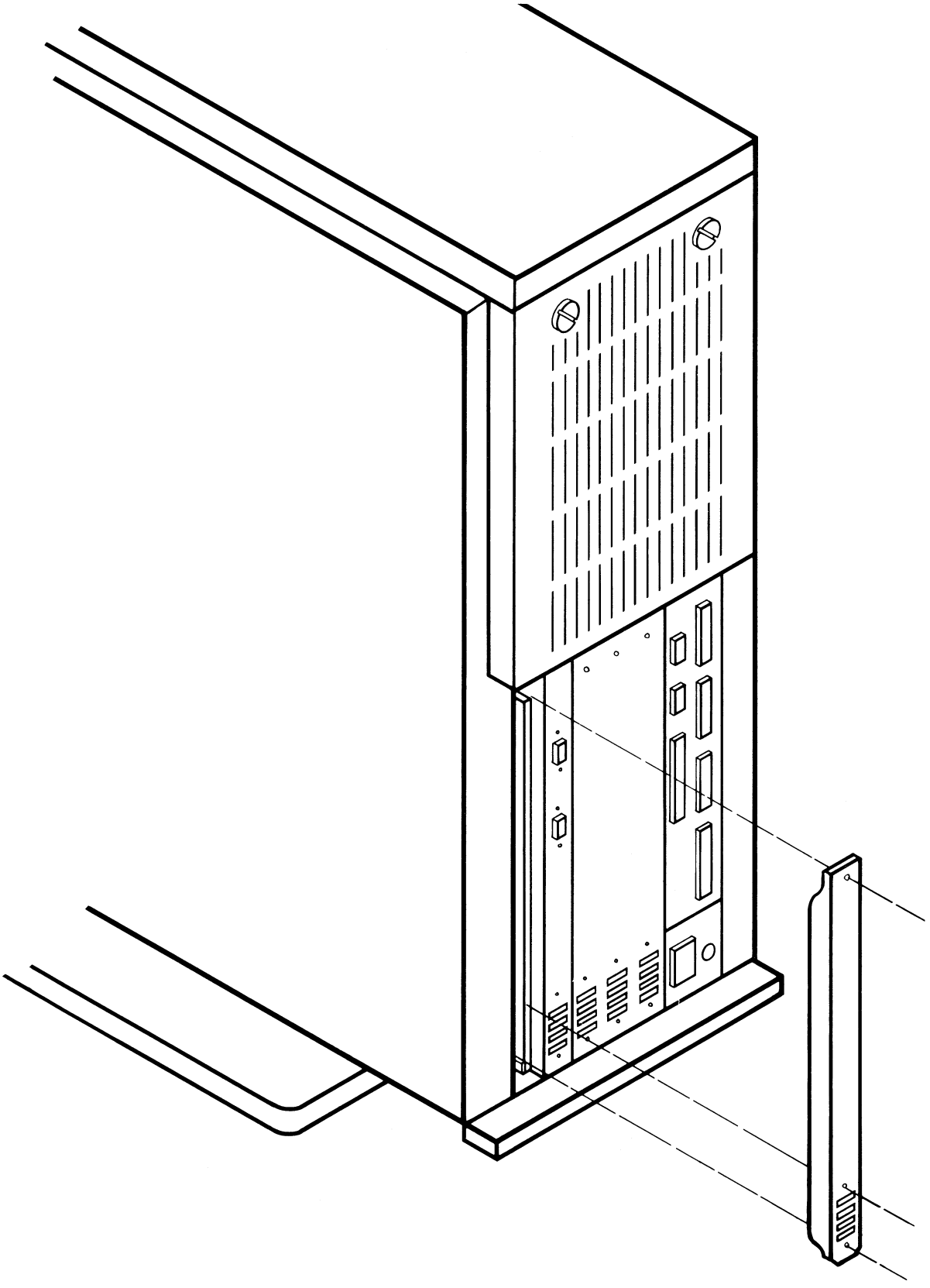


Figure D-18. Back Panel with Bulkheads Installed.

The bulkhead assembly consists of the following parts:

- one five-card-wide bulkhead plate
- five bulkhead grounding clips
- five pop rivets
- two Phillips screws (with washers)
- two screw retainers

Specification drawings for these parts are shown in Figures 19 through 27.

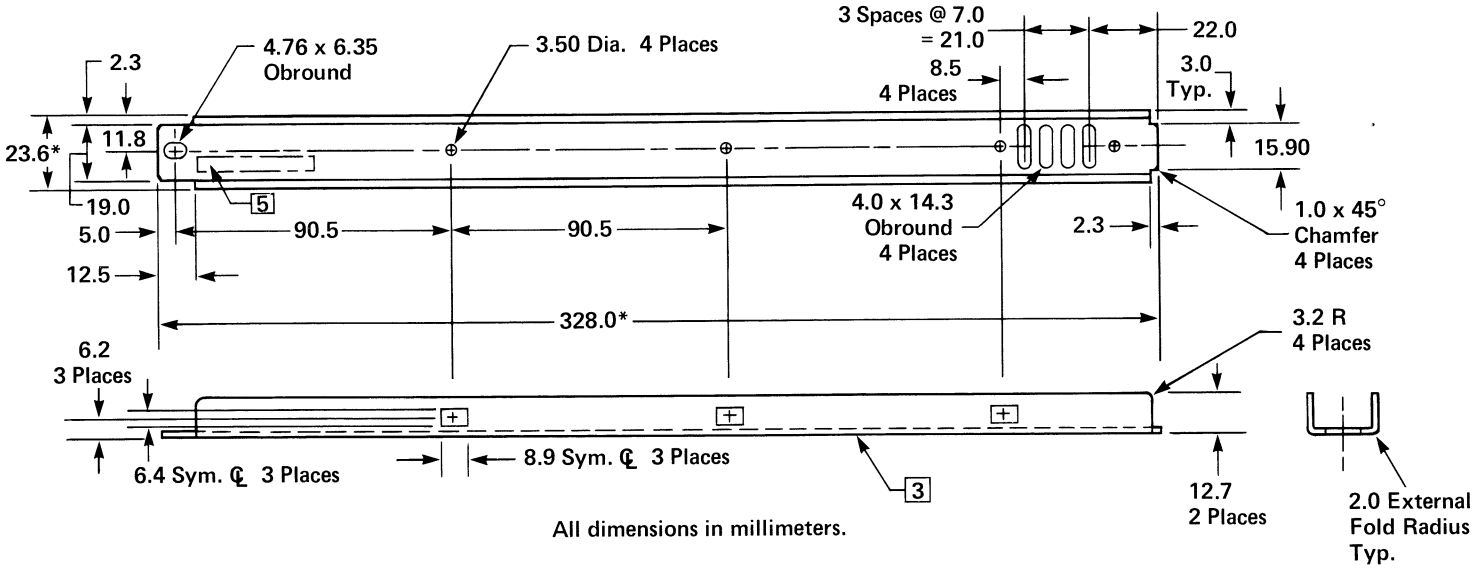
Bulkhead grounding clips are part of the ESD/EMI shield and must be installed to prevent ESD/EMI leakage. These clips, shown in Figure D-27, are available only from

Instrument Specialties Company, Inc.
Delaware Water Gap, PA 18327
Phone: (717) 424-8510

The pop rivets are used to fasten bulkhead grounding clips to the bulkhead assembly; and the two phillips screws, made captive by the screw retainers, are the crucial barrier to the monitor form Multibus electronics as required by UL, which means that their removal requires use of a tool other than a slotted-head screwdriver.

Screws, screw retainers, pop rivets, and tools should be available from hardware stores or distributors in your area. Sheet metal and cables are custom parts that can be built to your specifications by specialty shops.

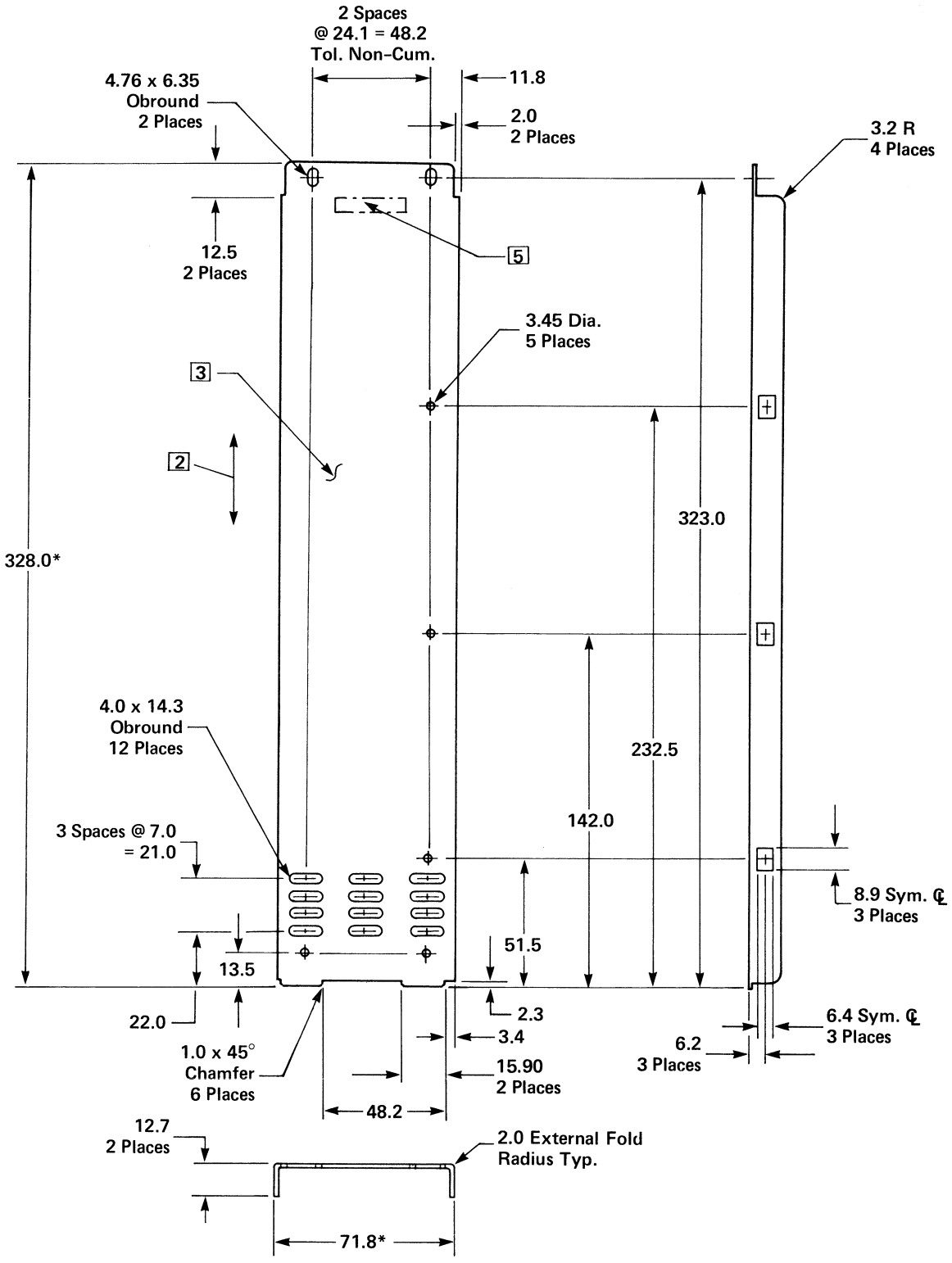
Bulkhead Sheet Metal. Figures D-19 and D-20 are design drawings for one- and three-card-wide bulkheads. Since the cards are spaced 24.1 mm (0.95 in) apart, intermediate bulkhead widths can be determined by adding this increment. Samples of the two types of bulkheads were included with your monitor form of the IWS workstation to aid in prototype experiments.



NOTES:

1. Material: 1.5mm (.059") thick Sheet CRS C-1010.
2. Finish: Deburr all edges, sand lengthwise, then plate clear zinc.
3. Cosmetics per CT Spec. No. 02-00006-00, Class-B.
   All other surfaces Class-C.
4. Process control dimensions denoted by *.
5. Print Part No. 83-00083-00 Rev. A in location shown.

Figure D-19. One-Card Wide Bulkhead Design Drawing (Standard Bulkhead Panel).



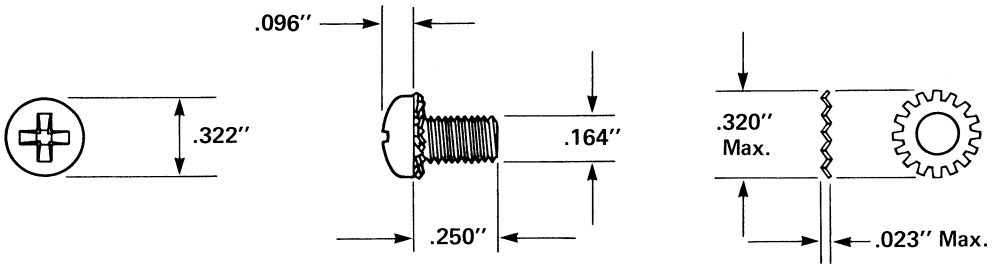
All dimensions in millimeters.

NOTES:

1. Material: 1.5mm (.059") thick Sheet CRS C-1010.
2. Finish: Deburr all edges, sand in direction shown, then plate clear zinc.
3. Cosmetics per CT Spec. No. 02-00006-00, Class B.
   All other surfaces Class C.
4. Process control dimensions denoted by *.
5. Mark Part No. 83-00084-00 and Rev. in area shown, far side.

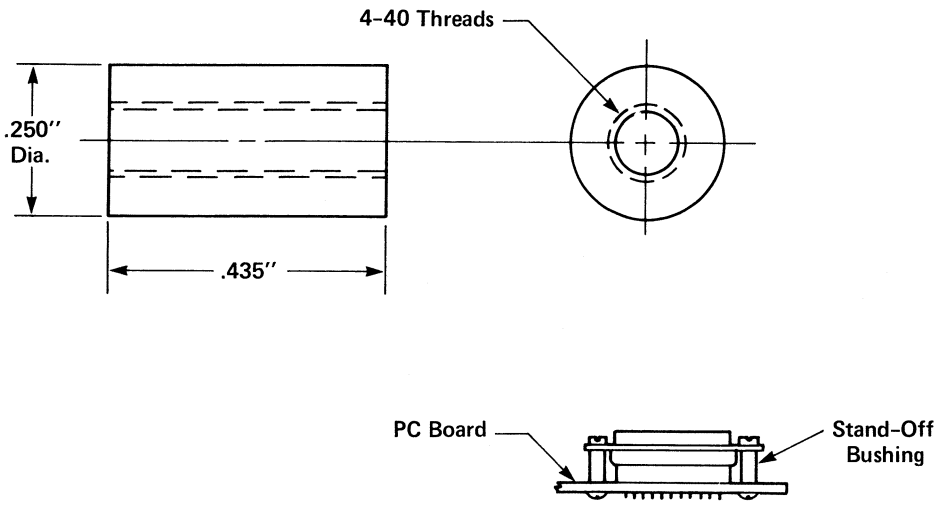
Figure D-20. Three-Card-Wide Bulkhead Design Drawing.

Figures D-21 through D-27 are specification control drawings for bulkhead hardware.



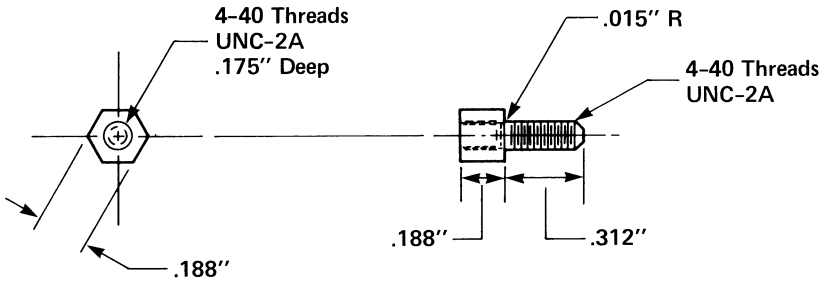
Type:	Machine (SEM)
Thread Size:	8-32
Major Dia.:	.164"
Thread Standard:	UNC-2A
Length:	.250"
Head Style:	Pan Head
Head Dia.:	.322"
Head Height:	.096"
Recess Type:	Phillips
Driver Size:	2
Locking Device:	External Tooth Captive Lock Washer
Washer Outside Dia.:	.320" Max.
Washer Thickness:	.023" Max.
Material:	1018 Mild Carbon Steel
Finish:	Zinc Plate .0002" Thick
Finish Spec.:	QQ Z 325C, Type I, Class 3

Figure D-21. Machine Screw #8-32 X 1/4" SEM. (CT Part Number 58-00024-00)



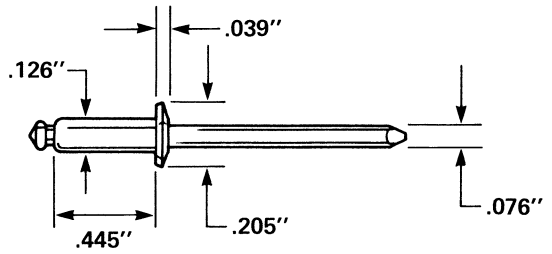
Type:	Stand-Off Bushing
Thread Size:	4-40
Outside Dia.:	.250"
Length:	.435"
Material:	Aluminum
Finish:	Clear Anodized

Figure D-22. Standoff Bushing. (CT Part Number 58-00024-00)



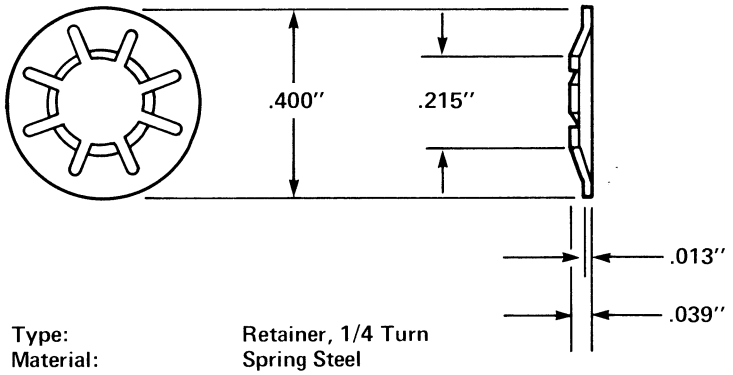
Type:	Screwlock, Male-Female Standoff
Thread Size:	4-40
Thread Standard:	UNC-2A
Material:	Steel
Finish:	Zinc Plate
Finish Spec.:	QQ Z 325B, Type II, Class 2

Figure D-23. Screwlock Assembly. (CT Part Number 41-00064-00)



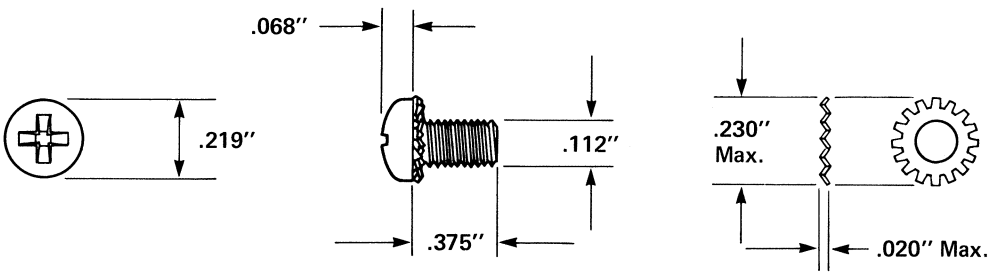
Rivet Type:	Blind, Dome Head
Grip Range:	.125"/.312"
Head Height:	.039"
Head Dia.:	.205"
Max Length Under Head:	.445"
Material:	
Shell:	5052 Aluminum
Stem:	Mild Steel, Finish Phosphate Coated
Recommended Hole Size:	.136"

Figure D-24. 1/8 Rivet. (CT Part Number 59-00016-00)



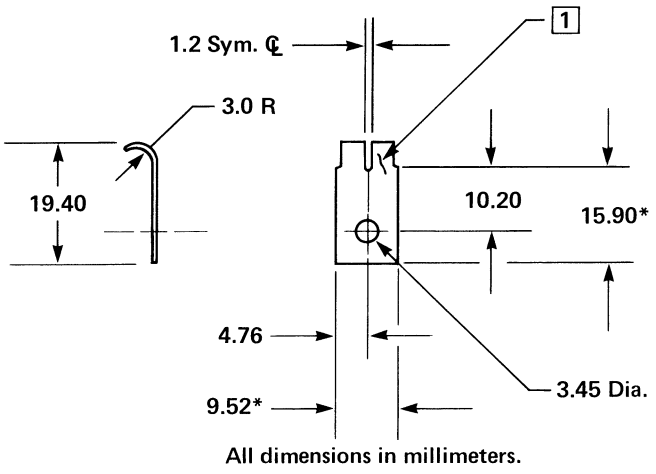
Type:	Retainer, 1/4 Turn
Material:	Spring Steel
Finish:	Zinc Plated

Figure D-25. 1/4 Turn Retainer. (CT Part Number 59-00001-00)



Type:	Machine (SEM)
Thread Size:	4-40
Major Dia.:	.112"
Thread Standard:	UNC-2A
Length:	.375"
Head Style:	Pan Head
Head Dia.:	.219"
Head Height:	.068"
Recess Type:	Phillips
Driver Size:	1
Locking Device:	External Tooth Captive Lock Washer
Washer Outside Dia.:	.230" Max.
Washer Thickness:	.020" Max.
Material:	1018 Mild Carbon Steel
Finish:	Zinc Plate .0002" Thick
Finish Spec.:	Per QQ P 416, Type I

Figure D-26. SEM Screw #4-40 X 3/8". (CT Part Number 58-00035-00)



NOTES:

1. Cosmetics per CT Spec. No. 02-00006-00, Class C.
2. Material: 0.13mm (.005") Beryllium Copper, Alloy 25.
3. Process control dimensions denoted by *.

Figure D-27. Bulkhead Grounding Clip. (Drawing Number A-57-00016-00)

Design Notes. The following notes are important considerations when designing your own bulkheads:

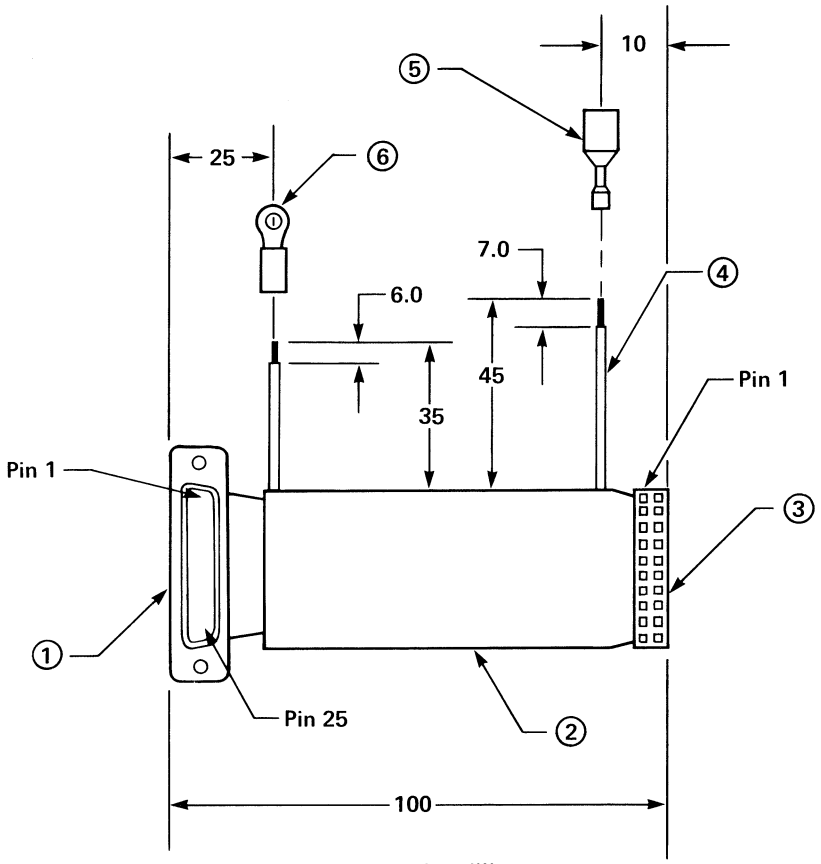
- The four oblong slots near the bottom of the bulkhead are air intake vents. Their location was chosen because it provides the best distribution of cool air over the Multibus card. These vents should therefore be included in each bulkhead design.

- Since the bulkhead is only an inch wide, it runs the risk of acting as an EMI "antenna" and hampering machine performance if the length-to-width ratio becomes greater than 4:1. The bulkhead grounding clips should therefore be placed so that there are no ungrounded sections more than 4 in long.

- If the sheet metal is folded near a punched hole during the fabrication process, the hole may become distorted. As a general rule, it is best to keep holes, namely, connector mounting holes, clear of folds by at least 1.5 times the material thickness, or 2.3 mm for a 1.6-mm-thick bulkhead.

Cabling and Cable Design. A common cabling arrangement at Convergent Technologies is to route a ribbon cable from the Multibus card to the bulkhead. At the bulkhead, a D-type connector is installed. These cable parts are readily available, and specialty shops can assemble the parts at low cost. The D-type connector is used because it is rugged, reliable, well shielded, and provides good strain relief and shield termination via its metal shell and mounting screws.

A design drawing for a ribbon cable using the D-type connector is shown as Figure D-28 and D-29, below. Note that, as shown in Figure D-28, the cable has a ground plane, which is terminated with fasteners at both ends. This ground is necessary to maintain the EMI/ESD integrity of the system.



All dimensions in millimeters.

NOTES:

1. 25 Position "D" Receptacle 3M No. 3483-1000
2. 26 Condr Ground Plane Ribbon 3M No. 3469/26
3. 26 Position Socket Connector 3M No. 3399-7000
4. 18 AWG Green/Yellow Wire, Stranded UL No. 1007
5. Quick Disconnect Amp No. 2-350804-4
6. Ring Tongue Terminal Amp No. 2-32951-1

Figure D-28. Ribbon Cable Assembly with D-Type Connector and Ground Plane.

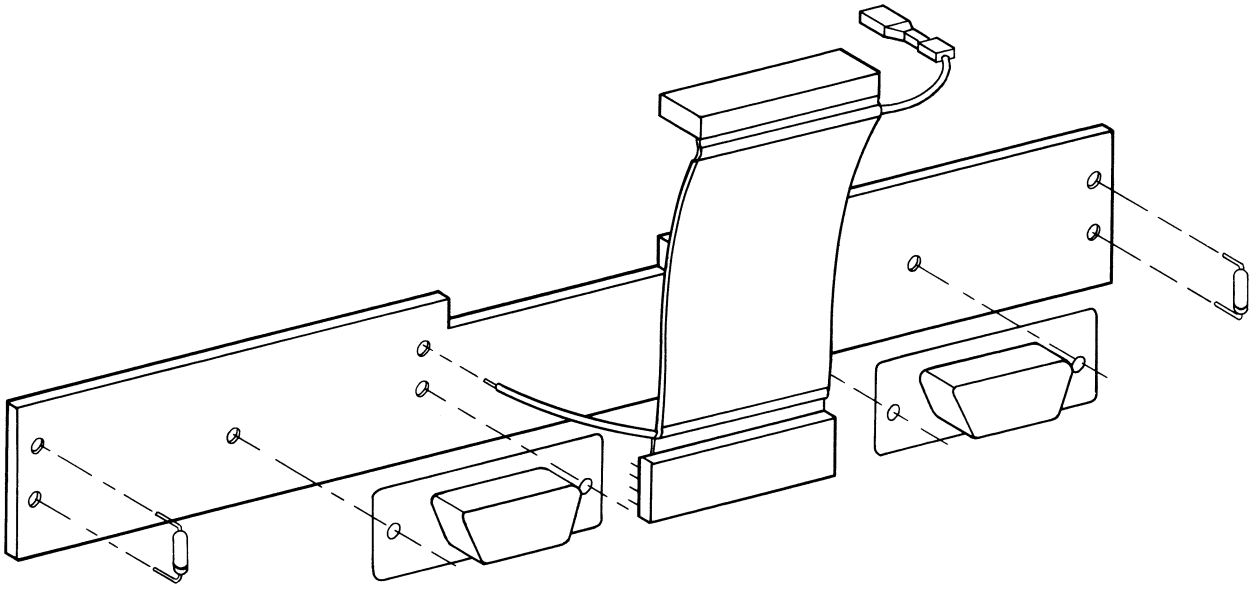


Figure D-29. Ribbon Cable Assembly.

Figures D-30, D-31, and D-32 show monitor form applications using the following cabling schemes and service loops:

- card edge connectors and pin headers at the Multibus card
- discrete wire, jacketed round wire, ribbon cable, and ground-plane ribbon cable from card to bulkhead
- D-type, 3M Delta Ribbon, and Amphenol Micro-Ribbon connectors at the bulkhead

Electrical parameters depend on the application, but the physical parameters for bulkhead cable design are as follows:

- The cable and connectors must fit within the space allotted between the Multibus card and the bulkhead.
- The cable and connectors should not spread into the space reserved for other Multibus cards.
- The cable should be long enough to include a few inches of service loop as required to allow convenient installation and removal.

An excellent way of making a service loop for installation of a ribbon cable is to fold the ribbon cable back on itself a few times as shown in Figure D-31. If round wire or jacketed cable is used in lieu of ribbon cable, locating the bulkhead connector a couple of inches lower than the connector on the Multibus card holds the service loop.

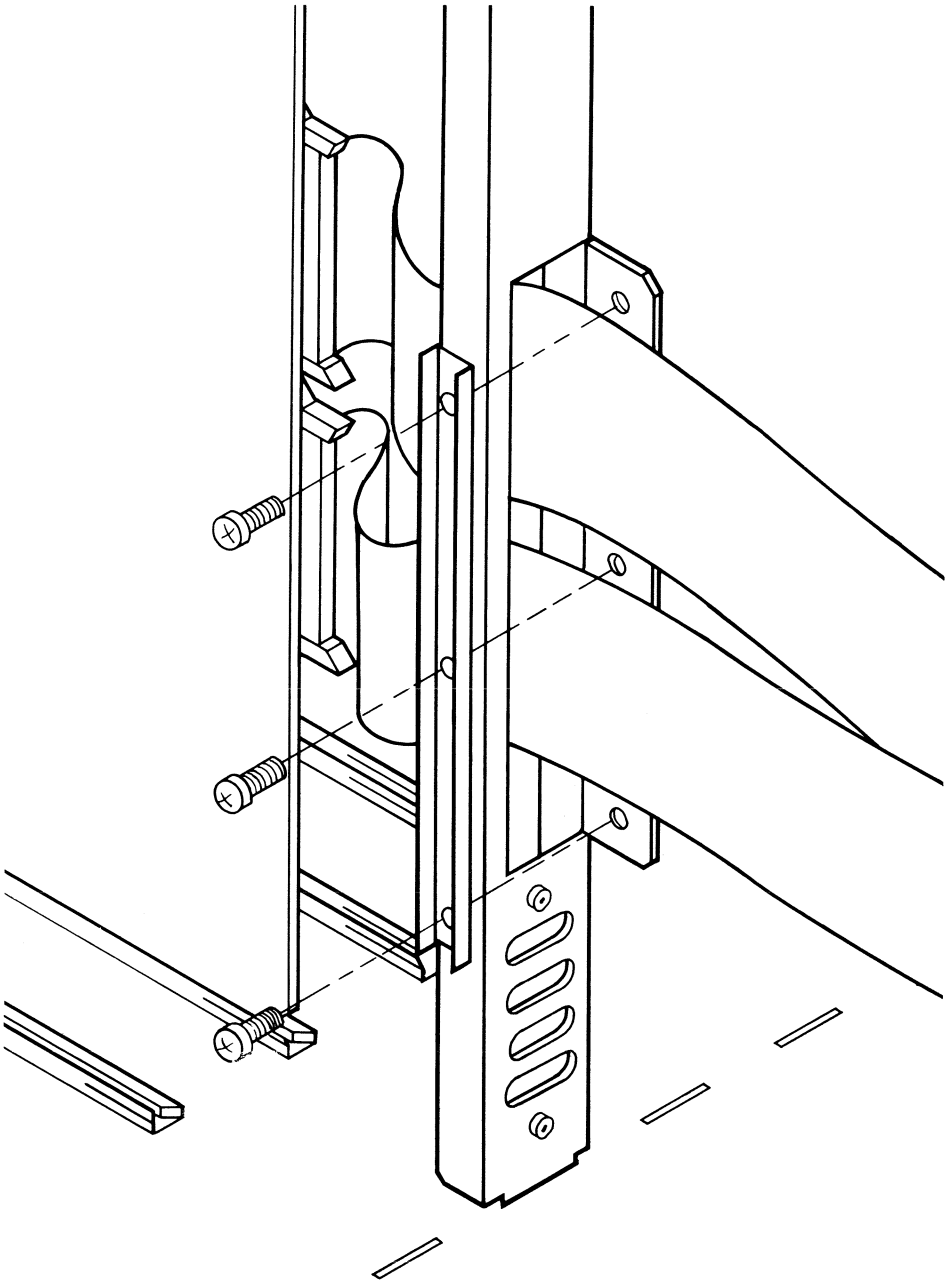


Figure D-30. Multibus Service Loop Example A.

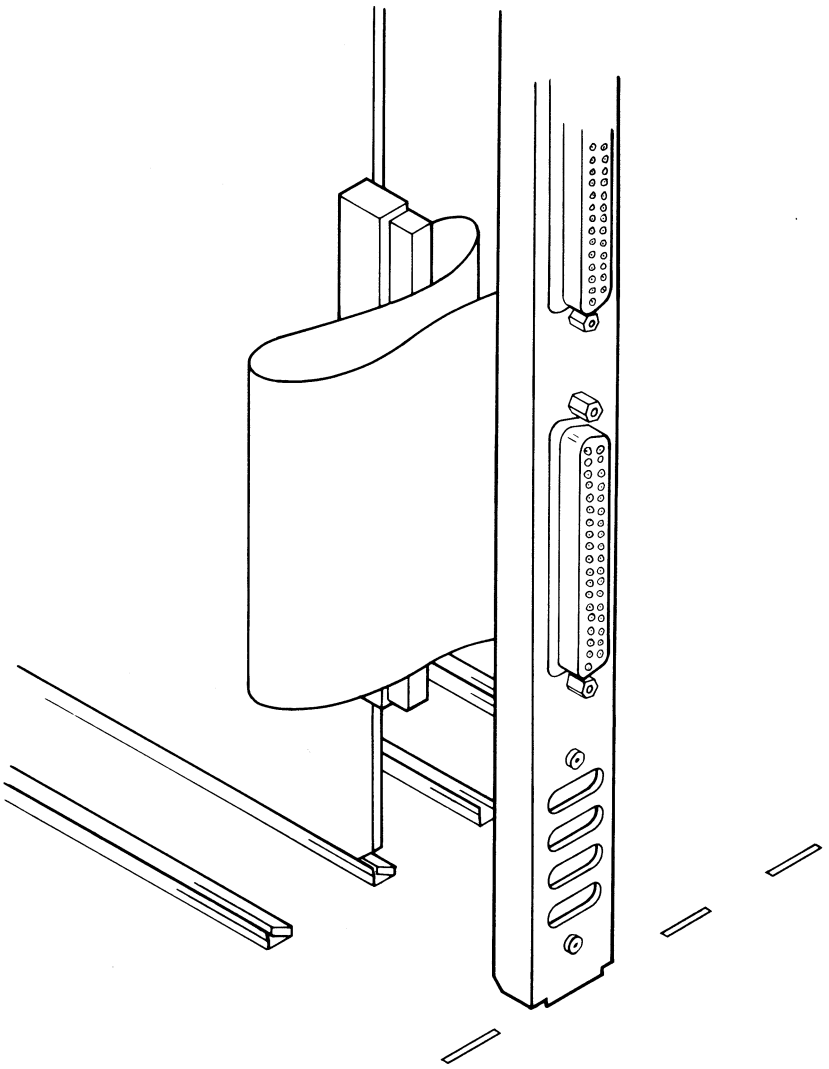


Figure D-31. Multibus Service Loop Example B.

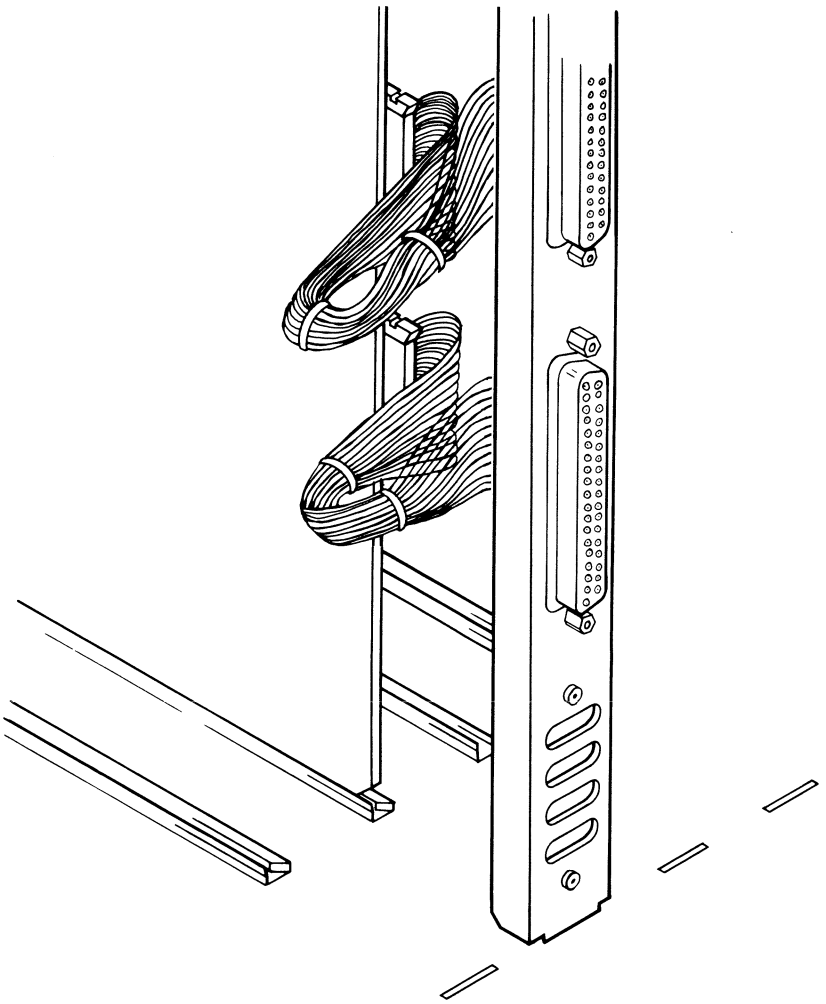
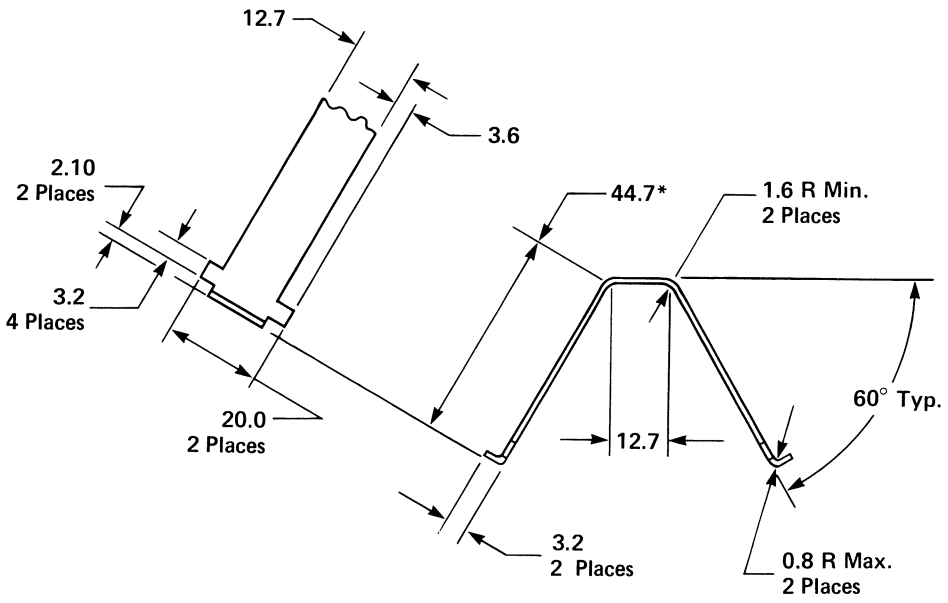


Figure D-32. Multibus Service Loop Example C.

Special Requirements. In some cases it is appropriate to cable directly from the Multibus card to the external device, as shown in D-32. When this happens, remember that the bulkheads and their grounding points are an important part of the ESD/EMI strategy, and that it is especially important to ground the cable shield where it enters the electronics box (at the bulkhead) to avoid interference with the monitor form's own operation.

Under some conditions, such as shipping or high vibration environments, retention of the Multibus cards in their slots might be necessary. A design for a Multibus card retainer device, which is disengaged when the bulkhead is removed, is shown in Figure D-33, below.



All dimensions in millimeters.

NOTES:

1. Tumble deburr
2. Material: 1095 annealed steel, 0.38mm (0.015") thick. Fold, then heat treat.
3. Finish: Zinc plate, clear. Bake parts immediately after plating to eliminate nitrogen embrittlement.
4. Quality Assurance:
   a.) Parts must meet CT Spec. No. 02-00006-00, Class C for cosmetic acceptability.
   b.) Process control dimensions are denoted by *.

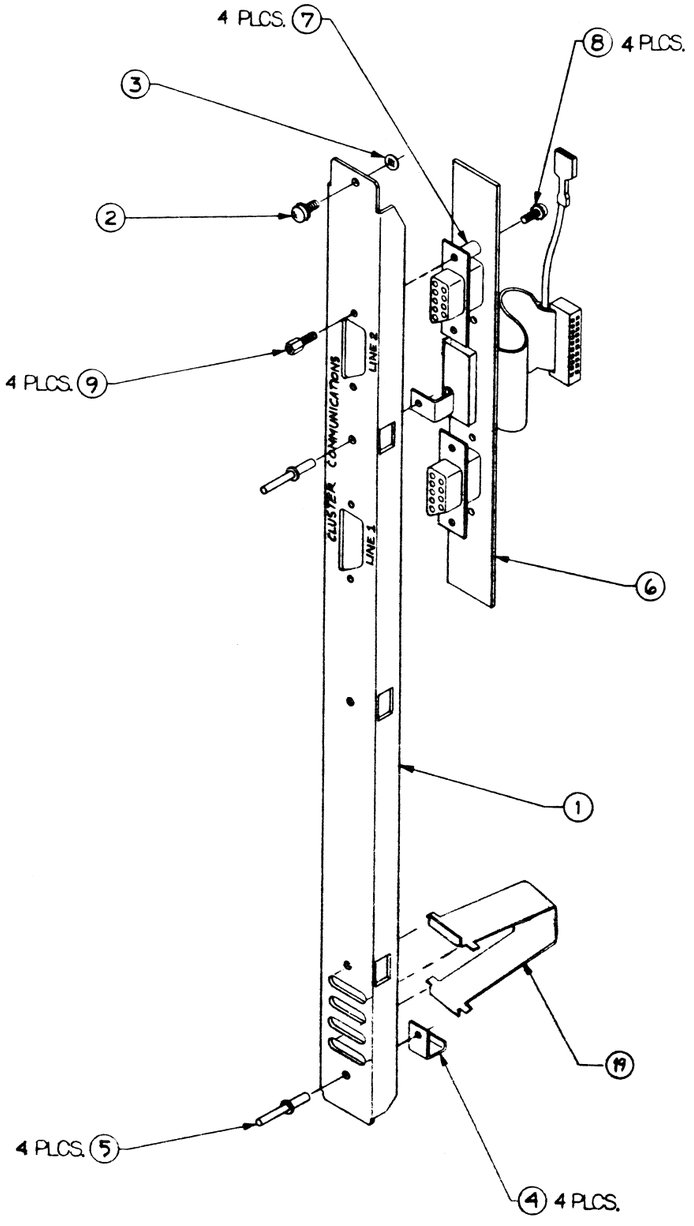
Figure D-33. Multibus Card Retainer.

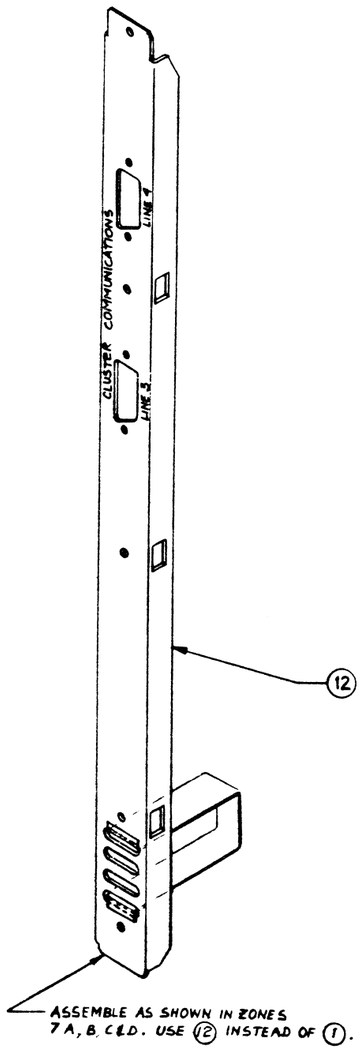
Multibus Applications Example

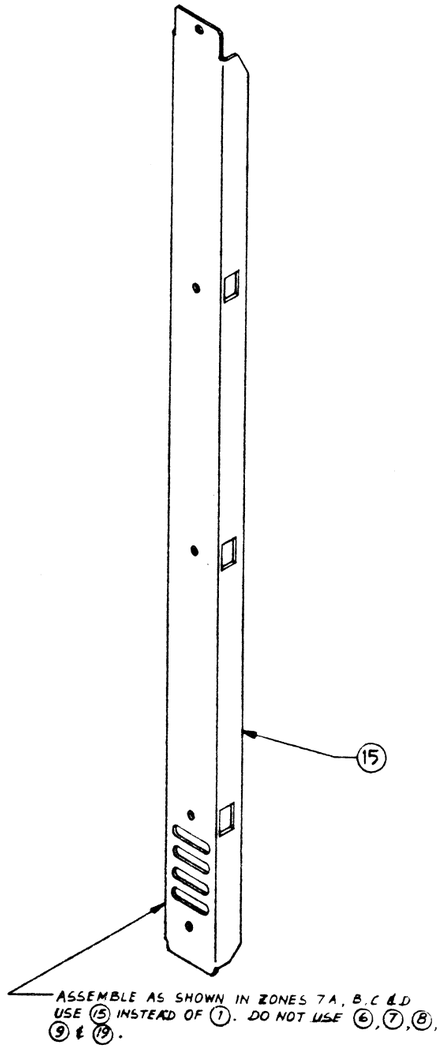
Convergent's CommIOP installation provides a good example of custom design for a monitor form Multibus application. The CommIOP provides an RS-422 communications interface through two 9-pin D-type connectors. A one-card-slot wide bulkhead, with connectors, cabling, and termination electronics attached, can be plugged into a workstation when the CommIOP Multibus card is installed. Installation is fast and easy, and, once complete, it allows the user to connect system cables without entering the machine or disturbing other Multibus card slots and cabling.

In addition to the CommIOP bulkhead, the CommIOP kit includes installation instructions and blank bulkheads for covering remaining Multibus slots. These blank bulkheads are similar to those shown in Figures D-19 and D-20. The CommIOP bulkhead design is unique because, as shown in Figure D-34, bulkhead connectors are mounted on a jumper printed circuit board with a single cable running to the Multibus card, instead of bulkhead-mounted connector cables running straight to the Multibus card. This design has allowed termination electronics to be added without affecting the Multibus card.

A partial set of manufacturing documentation for the CommIOP card is shown in Figures D-21 through D-27, D-33, and D-34.







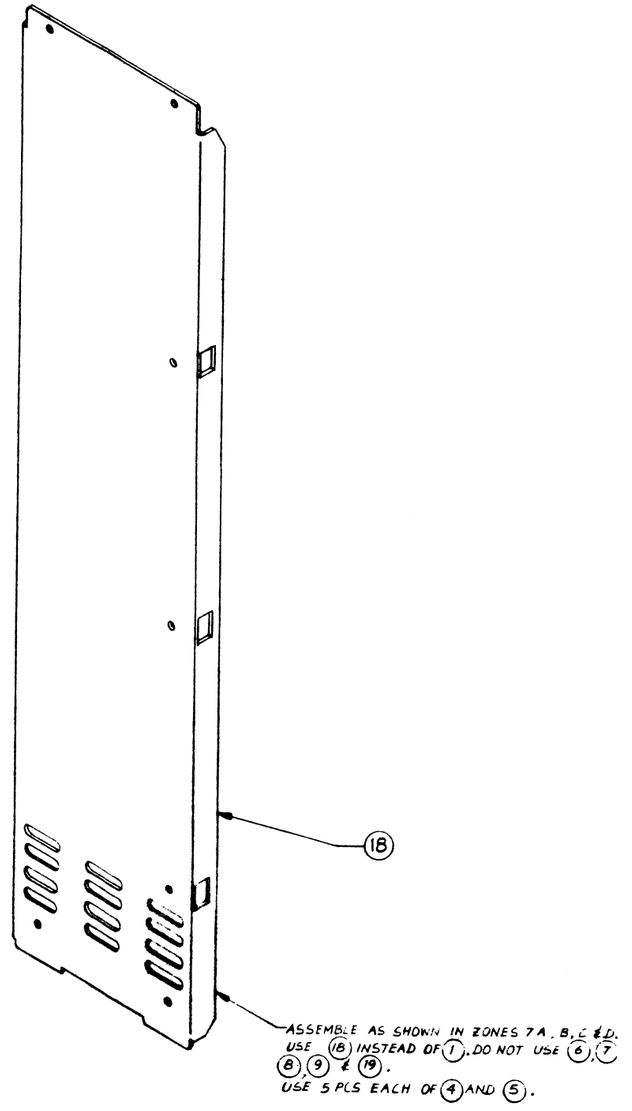
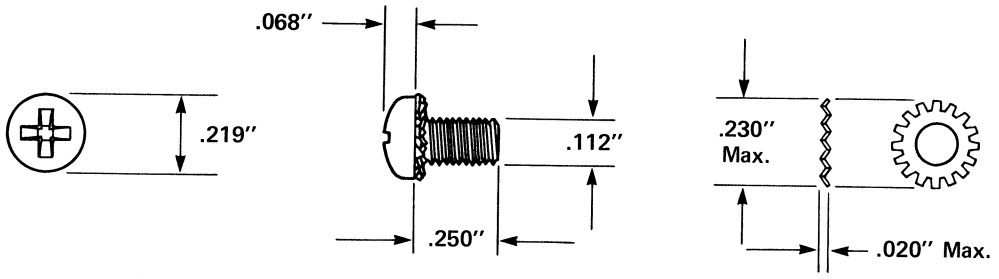


Figure D-34. Comm IOP Board Assembly.



Type:	Machine (SEM)
Thread Size:	4-40
Major Dia.:	.112"
Thread Standard:	UNC-2A
Length:	.250"
Head Style:	Pan Head
Head Dia.:	.219"
Head Height:	.068"
Recess Type:	Phillips
Driver Size:	1
Locking Device:	External Tooth Captive Lock Washer
Washer Outside Dia.:	.230" Max.
Washer Thickness:	.020" Max.
Material:	1018 Mild Carbon Steel
Finish:	Zinc Plate .0002" Thick
Finish Spec.:	Per QQ Z 325 C, Type I, Class 3

Figure D-35. SEM Screw #4-40 X 1/4". (CT Part Number 58-00022-00)

CONTENTS: APPENDIX E

LIST OF FIGURES

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APPENDIX E: IWS WORKSTATION BOOTSTRAP ROMS

This appendix describes the four types of programmable ROMs that are found in the IWS workstation: the standalone ROM, a 2716 used in standalone and cluster master workstations, which can bootstrap from either a floppy or a hard disk; the cluster ROM, a 2716 used only in cluster workstations, which can bootstrap from either a floppy disk or communications channel A (RS-422); and the common ROMs, versions 2 and 4. Common ROMs are 2732s that can be used in any cluster position and can bootstrap from a floppy disk or a hard disk. All new workstations contain common ROMs, although older workstations may contain cluster or standalone ROMs.

Subsection 1 of this appendix is a functional description of the four types of bootstrap ROM, their operation, and their role in cluster protocol. Subsection 2 discusses installation and switch settings for switches controlling ROM program selection. Subsection 3 explains software entry into the ROM program and contains a list of register settings for each type of ROM. Subsection 4 contains a description of the Panel debugger. Subsection 5 contains an explanation of error codes, a list and description of codes and their meanings, and a quick-reference summary of error codes.

1. FUNCTIONAL DESCRIPTION

This subsection contains a description of the ROM program, explains when it is executed, and outlines program flow. It also describes the ANSI protocol used for cluster communications and contains a list of protocol symbols and their meanings.

The bootstrap ROM program is executed

- when the IWS is powered up
- when the reset button on the workstation back panel is pushed
- after a software jump into the bootstrap ROM (that is, when the CTOS operating system detects a nonrecoverable error)

- when a breakpoint (INT 7Ch) instruction causes a jump from RAM to the bootstrap ROM panel program

In all of these cases, except for a breakpoint, the ROM entry address is at FFFF:0h

The 8086's internal ES and DX registers control the bootstrap ROM program flow and can be read to determine how the ROM program was entered. If the ES register is set to 0, for example, it indicates that the bootstrap ROM program was entered through a power-up or reset. If the ES register is set to 1, the bootstrap program was entered through a software jump (for example, a nonrecoverable error) or through a breakpoint embedded in the software code. The bootstrap ROM will not attempt a memory dump if the workstation has just been powered up.

If the bootstrap program is entered through a power-up or reset, the ROM reads the "cold bit" of port 54h, bit 0Dh, to determine which condition caused the entry. (Port 54h is defined in the "Software Interface" subsection of Section 2, "Functional Interfaces.") The bootstrap ROM then reads I/O Memory board switch 2 (SW2) settings at port 44h to determine if the workstation is in a standalone, cluster, or master position. At this time, the bootstrap ROM also transfers the contents of SW2 (port 44h) into internal register DX to specify the bootstrap program sequence. SW2 is factory set, but switch settings may be changed to run memory tests or different bootstrap sequences, to set up the bootstrap ROM to only look at specific devices, or to indicate that a workstation's position has been changed (from a cluster position, for example, to a master position). For more information on switch settings, see Subsection 2, "Bootstrap ROM Installation and Switch Settings," below.

If the bootstrap ROM program is entered through a software jump or a breakpoint, the ROM program assumes that registers ES and DX have already been set up by another program, and does not read port 44h (SW2) to control the program flow. Nor does the ROM program reset the video during hardware initialization or perform the main memory test. (The video is normally reset in hardware initialization just before the video buffer in RAM is overwritten with the new image.) The video is left on to display crash status in case the bootstrap fails.

The normal program flow for all versions of the bootstrap ROM follows:

1. Starts execution at FFFF:0h.

2. Reads port 44h for special instructions.

3. Initializes hardware.

4. Performs a checksum test of ROM.

5. Performs a memory test of the ROM program work area.

6. Copies the CTOS operating system buffer (256K bytes) into the ROM program work area.

7. Copies the first 128K of RAM to a disk or communications line in a memory dump. (Common ROM version 4 dumps all RAM here.)

> NOTE
>
> 4K of RAM (from 124K to 128K) is used by the ROM for a work area and is therefore invalid as RAM.

8. Performs a memory test on the first 124K of RAM. (Common ROM version 4 tests all RAM here.)

9. Bootstraps and performs a checksum test of the CTOS operating system or the selected diagnostic.

10. Jumps to the start of the CTOS operating system or the selected program.

In step 3 of the above program flow, only enough hardware is initialized to boot the CTOS operating system or a diagnostic. Steps 6 and 7 (CTOS operating system buffer copy and RAM dump) occur only at a reset boot. In step 7, RAM is dumped to the floppy disk first, to the hard disk next, and then to the communications line. As referred to in step 5, the work area of the 2716 ROMs (cluster and standalone) is 4K bytes at 1F00:0h. If the workstation uses a 2732, or common bootstrap ROM, the work area is 8K bytes at 1E00:0h.

The bootstrap ROM distinguishes internally between hard and floppy disks because many systems use separate boards for the floppy and hard disk controllers. While the bootstrap ROM program assumes that a floppy disk is a double-density diskette as described in the System Programmer's Guide, no assumption is made as to the type of hard disk. Instead, hard disk units have a time restriction of 10 seconds in which to complete a recalibration or data transfer before an error code is generated.

> NOTE
>
> Because of the 10-sec time restriction, systems with SMD Controller boards fail to boot most operating systems successfully. The file system has been changed for hard disks, solving this problem, but bootable floppy or hard disks must be initialized with IVolume version 8.0 or greater. This procedure creates a Bootest.Sys file. ROM then loads this Bootext.Sys file instead of SysImage.Sys. A program in Bootext.Sys then loads the SysImage.Sys file.

The CTOS operating system examines the ROM version number by reading two identical bytes at locations FFFF:0006h and FFFF:0007h. This version number byte is repeated so that it appears in each of the two ROM chips. Version numbers are

FF standalone

01 cluster

02 common (version 2)

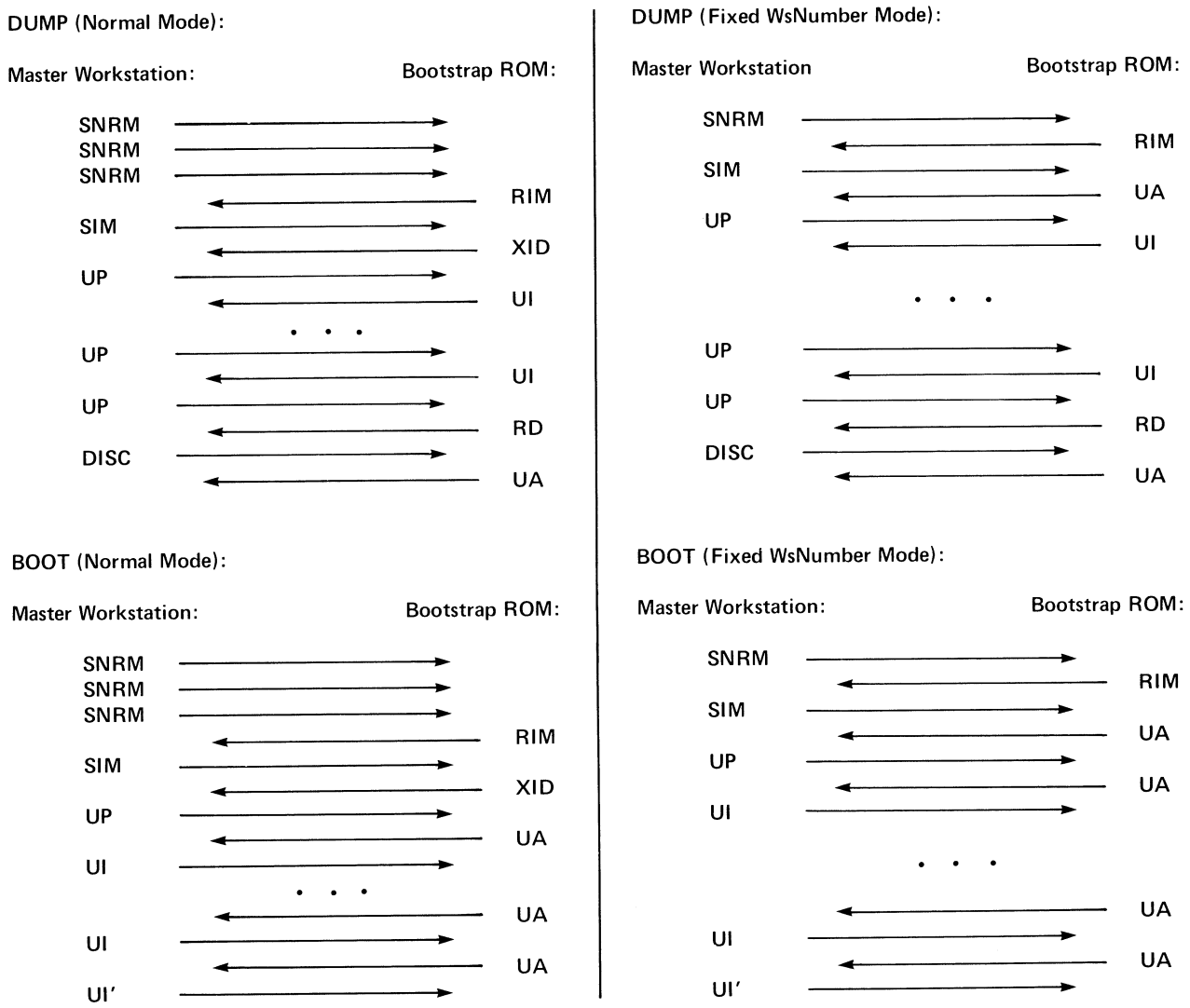
04 common (version 4)

Any application that wants to access the ROM version number must do so with bus timeout and parity disabled; otherwise a nonmaskable error results. The Parity Control register is controlled by port 56h, which is listed in the "I/O Control Register" subsection of Section 2, "Functions and Interfaces."

Cluster Protocol

The actual protocol used for cluster communications is a subset of the American National Standard for Advanced Data Communications Control Procedures (ADCCP), as defined in ANSI, Version 3.66, published by the American National Standards Institute, Inc. The sequence used during the dump and bootstrap routines is illustrated in Figure E-1. The protocol symbols (as described by ANSI) are as follows:

Symbol	Meaning
SNRM	Set Normal Response Mode
RIM	Request Initialization Mode
SIM	Set Initalization Mode
XID	Identification Frame (contains WsType, or workstation type)
UP	Unnumbered Poll
UI	Unnumbered Data Frame
RD	Request Disconnect
DISC	Disconnect
UA	Unnumbered Acknowledge
UI'	Unnumbered Data Frame with termination data



DUMP AND BOOT PROTOCOL SYMBOLS:

SNRM	Set Normal Response Mode
RIM	Request Initialization Mode
SIM	Set Initialization Mode
RD	Request Disconnect
DISC	Disconnect
UP	Unnumbered Poll
UI	Unnumbered Data Frame
UI'	Unnumbered Data Frame with Termination Data
UA	Unnumbered Acknowledge
XID	ID Frame (Contains WsType)

Figure E-1. Communications Dump and Bootstrap Protocol.

2. BOOTSTRAP ROM INSTALLATION AND SWITCH SETTINGS

The bootstrap ROM is installed at the factory. It is located on the CPU board. Switch 5 (S5) on the CPU board controls ROM type. If the workstation serial number, located on a metal plate at the rear of the workstation, is revision A or B, for example, the bootstrap ROM is a 2716; if the workstation ID number is revision C or greater, the bootstrap ROM is a 2732. For a 2716 ROM, bit 1 of S5 is off, and bit 2 is on; for a 2732, bit 1 of S5 is on, and bit 2 is off. (For more information on bootstrap ROM types, see the introduction to this appendix.)

The ROM program flow is controlled by switch 2 (SW2), located on the I/O Memory board. While SW2 is factory installed with a default setting (all bits are 0), cluster bootstrap ROMs (2716, revision A or B workstations) may require special SW2 settings, and SW2 can be set to program special tests or boot sequences for all bootstrap ROMs, as described in this section.

> NOTE
>
> I/O port 44h, when read, indicates the contents of SW2 in negative logic. When written to, port 44h controls the workstation speaker and the six LEDs at the edge of the I/O Memory board.

I/O Memory board LEDs and SW2 are shown in Figure E-2.

As mentioned, the I/O Memory board LEDs and SW2 use negative logic, so if a bit in SW2 is set to ON, it sets the corresponding bit in port 44h to 0, and vice versa. I/O Memory board LEDs are all ON at power-up.

Special Bootstrap Program Configurations

Specific Devices

SW2 bits may be set to cause the bootstrap ROM to look only at specific devices, as shown in the switch setting tables for each ROM, below. The

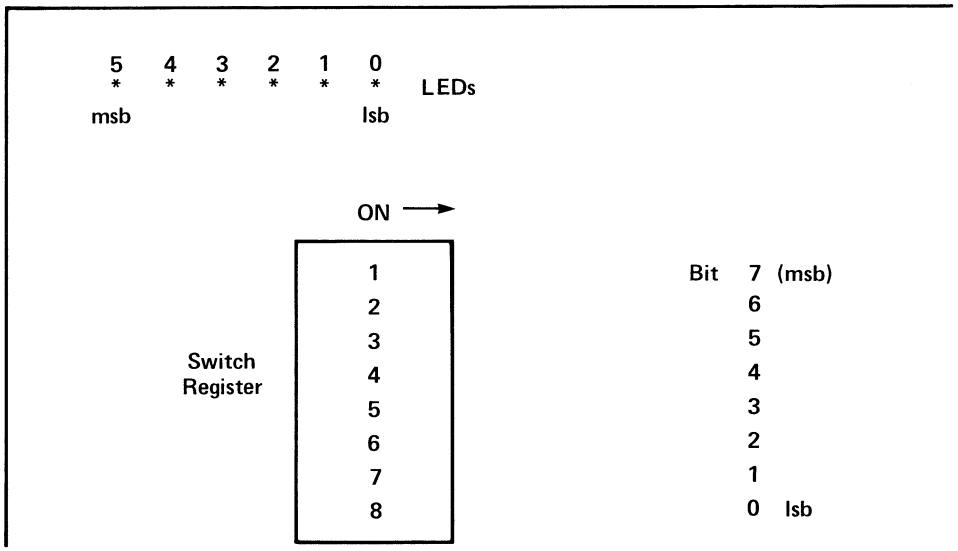


Figure E-2. I/O Memory Board SW2 and LEDs.

settings may specify floppy disk only; a specific disk only; the communications line only; or the floppy and hard disks, but not the communications line.

Memory Diagnostic

The SW2 bits may also be set to cause the bootstrap ROM to run a continuous test memory. A bootstrap ROM with this setting initializes hardware and then repeatedly does a checksum test of ROM followed by a test of RAM.

Switch settings for this option are shown below.

Panel Debugger

Several bit settings, as shown below, cause the Panel debugger program to be entered at two places in the boot sequence. For more information on Panel, see Subsection 4, "Panel (Virtual Console Debugger)."

Standalone Bootstrap ROM Switch Settings

S1	S2	S3	S4	S5	S6	S7	S8	Function
on	on	on	on	on	on	on	on	Normal operation.
on	on	on	off	on	on	on	on	Enter Panel after booting.
on	on	off	on	on	on	on	on	Ignore floppy drive.
on	on	off	off	on	on	on	on	Ignore floppy drive, enter Panel after booting.
on	off	on	on	on	on	on	on	No dump.
on	off	on	off	on	on	on	on	No dump, enter Panel after booting.
on	off	off	on	on	on	on	on	No dump, ignore floppy drive.
on	off	off	off	on	on	on	on	No dump, ignore floppy drive, enter Panel after booting.
off	on	on	on	on	on	on	on	Infinite memory test.
off	on	on	off	on	on	on	on	Enter Panel at start and after booting.
off	on	off	on	on	on	on	on	Jump into expansion ROM (starting at location F7FF:0000h).

Cluster Bootstrap ROM Switch Settings

RS-422 Baud Rate

CT software supports only 307.2 kilobaud.

S1	S2	S3	Baud Rate
on	on	off	307.2 kilobaud

Panel

S4	Function
on	Normal operation.
off	Enter Panel after booting.

Cluster ID Number

The cluster bootstrap ROM operates in fixed ID mode only. Each workstation on a line must have a different ID setting.

S5	S6	S7	S8	Identification Number
on	on	on	off	ID1
on	on	off	on	ID2
on	on	off	off	ID3
on	off	on	on	ID4
on	off	on	off	ID5
on	off	off	on	ID6
on	off	off	off	ID7
off	on	on	on	ID8
off	on	on	off	ID9
off	on	off	on	ID10
off	on	off	off	ID11
off	off	on	on	ID12
off	off	on	off	ID13
off	off	off	on	ID14
off	off	off	off	ID15

Special Cluster ROM Settings

S1	S2	S3	S4	S5	S6	S7	S8	Function
off	on	on	on	on	on	on	on	Infinite memory test.
off	on	on	off	on	on	on	on	Enter Panel at start and after booting (no cluster).
off	on	off	on	on	on	on	on	Jump into expansion ROM, starting at location F7FF:0000h.

Common Bootstrap ROM Switch Settings

Operation Control

S1	S2	S3	S4	Function
on	on	on	on	Normal operation. Device code (see Table E-1, below) is used as workstation type if booting from RS-422 communications line.

S1	S2	S3	S4	Function
on	on	on	off	Boot from a particular disk only. The device code shown in Table E-1, "Disk Device Codes," designates which device is used for booting.
on	on	off	on	Boot from the RS-422 communications line only. The device code is used as the workstation type number.
on	on	off	off	Boot from disks only, using the normal disk search order. If the device code is not zero, enter the Panel debugger after loading the operating system or diagnostic.
off	on	on	on	Execute repeated memory ROM and RAM tests. If the device code is not zero, enter Panel at the start of each test.
off	on	on	off	Normal operation, except that Panel is entered at the start of the booting sequence and after loading an operating system. The device code is used as the workstation type number if booting from the RS-422 communications line.
off	on	off	on	Jump into expansion ROM (starting at location F7FF:0000h).
off	on	off	off	Fixed ID mode. The device code is used as the workstation ID number if booting from the RS-422 communications line.

Device Codes

S5	S6	S7	S8	Device Codes
on	on	on	on	0
on	on	on	off	1
on	on	off	on	2
on	on	off	off	3
on	off	on	on	4
on	off	on	off	5
on	off	off	on	6
on	off	off	off	7
off	on	on	on	8
off	on	on	off	9
off	on	off	on	10
off	on	off	off	11
off	off	on	on	12
off	off	on	off	13
off	off	off	on	14
off	off	off	off	15

Table E-1. Disk Device Codes.

Device code	System with HDC or FDC board*	System with SMD Controller board
0	floppy 0 ([f0])	--
1	disk 0 ([d0])	disk 0 ([f0])
2	disk 1 ([d1])	disk 2 ([d0])
3	disk 2 ([d2])	disk 4 ([d3])
4	--	disk 6 ([d1])
5-15	--	--

* HDC = Hard Disk Controller
FDC = Floppy Disk Controller

3. SOFTWARE ENTRY INTO BOOTSTRAP ROM

If the 8086 register ES is set to 1 when the bootstrap ROM is entered, the ROM program assumes that registers ES and DX have been set up by another program, and SW2 (port 44h) is not used to control program flow. If ES is set to 0, however, the ROM program reads port 44h to control program flow. Registers ES and DX are examined at various times in the bootstrap process, and the specific tests are described here.

In the following table, register DX is shown in binary, with the hex value in parentheses. A 0 (zero) indicates that a bit is OFF, and a 1 indicates that a bit is ON. A hyphen (-) indicates that the bit is ignored.

Software Entry into Standalone Bootstrap ROM

Register ES must be set to 1, and register DX must be set with bits 0 to 15 defined as follows:

Register DX Setting (binary)	Definition
000- 0000 ---- ---1	No dump, no copy of operating system buffer.
000- 0000 ---- --1-	No dump.
000- 0000 ---- -1--	Ignore floppy in dump.
000- 0000 ---- 1---	Jump to start of program after doing memory test.
000- 0000 ---1 ----	Ignore floppy in boot.
000- 0000 --1- ----	Ignore hard disk in dump.
000- 0000 -1-- ----	Ignore hard disk in boot.
000- 0000 1--- ----	Enter Panel at start of program.
0001 0000 ---- ----	Enter Panel after boot.

To dump to a hard disk, for example, and then reboot from the floppy, set register ES to 1 and set register DX to 44h (0000 0000 0100 0100). After setting the registers, jump to location 0FFFF:0000h.

Software Entry into Cluster Bootstrap ROM

Register DX Setting (binary)	Definition
---- ---- ---- ---1	No dump or copy of buffer.
---- ---- ---- --1-	No dump.
---- ---- ---- -1--	Ignore floppy in dump.
---- ---- ---- 1---	Jump to start of program after memory test.
---- ---- ---1 ----	Ignore floppy in boot.
---- ---- 1--- ----	Enter Panel at start of program.
---- 0000 ---- ----	Ignore cluster in dump and boot.
---- 0001 ---- ----	ID 1.
---- 0010 ---- ----	ID 2.
---- 0011 ---- ----	ID 3.
---- 0100 ---- ----	ID 4.
---- 0101 ---- ----	ID 5.
---- 0110 ---- ----	ID 6.
---- 0111 ---- ----	ID 7.
---- 1000 ---- ----	ID 8.
---- 1001 ---- ----	ID 9.
---- 1010 ---- ----	ID 10.
---- 1011 ---- ----	ID 11.
---- 1100 ---- ----	ID 12.
---- 1101 ---- ----	ID 13.
---- 1110 ---- ----	ID 14.
---- 1111 ---- ----	ID 15.
---1 ---- ---- ----	Enter Panel after booting.

Register DX Setting (binary)	Definition
000- ---- ---- ----	614.4 kilobaud.
001- ---- ---- ----	307.2 kilobaud (required by the CTOS operating system).
010- ---- ---- ----	153.6 kilobaud.
011- ---- ---- ----	76.8 kilobaud.
100- ---- ---- ----	38.4 kilobaud.
101- ---- ---- ----	19.2 kilobaud.
110- ---- ---- ----	9.6 kilobaud.
111- ---- ---- ----	4.8 kilobaud.

To dump to the floppy disk, for example, and then to the communications line at 307.2 kilobaud (fixed ID 3), set register ES to 1 and register DX to 2310h (0010 0011 0001 0000). After setting registers, jump to location 0FFFF:0000h.

Software Entry into the Common Bootstrap ROM

Register ES must be nonzero. If register ES is set to 1, no memory RAM test will occur and video will be left running until the boot starts. Register DX must be set by adding values as follows:

Register DX Setting (binary)	Definition
---- ---- ---- ---1	No copy of the operating system bootblock.
---- ---- ---- --1-	No memory dump.
---- ---- 1--- ----	Enter Panel at start of program after loading operating system.
---- ---- ---- 01--	Dump and boot from the communications line only.
---- 0000 ---- 10--	Dump and boot with disk device 0 as shown in Table E-1.
---- 0001 ---- 10--	Dump and boot with disk device 1 only.

Register DX Setting (binary)	Definition
---- 0010 ---- 10--	Dump and boot with disk device 2 only.
---- 0011 ---- 10--	Dump and boot with disk device 3 only.
---- 0100 ---- 10--	Dump and boot with disk device 4 only.
---- ---- -110 00--	Dump and boot with disk device 0 only.
---- ---- -001 00--	Dump to disk devices 0 and 1; boot from disk device 1.
---- ---- -011 00--	Dump to disk devices 0, 1, and 2; boot from disk device 2.
---- ---- -101 00--	Dump to disk devices 0, 1, 2, and 3; boot from disk device 3.
---- ---- -111 00--	Dump to any disk device; boot from disk device 4.
1101 0001 ---- 0--- to 1101 1111 ---- 0---	Use fixed workstation ID modes 1 to 15 when booting from RS-422 communications line.
---- 0000 ---- 0--- to ---- 1111 ---- 0---	Use workstation types 0 to 15 when booting from RS-422 communications line, if not booting from fixed ID mode.
1000 ---- ---- --11	Repeated test of memory ROM and RAM.

For example, on a workstation with the SMD Controller board, to dump to either the [f0] or [d0], and then reboot from [d0], set ES to 1 and DX to 030h (0000 0000 0011 0000 binary).

Bootstrap Interface Block

When a program is loaded, the bootstrap ROM places a 16-byte structure in memory. The structure of this bootstrap interface block is as follows:

Offset	Field	Size	Description
0	pProgramStart	4	Pointer to the first instruction in the operating system or diagnostic that was booted.
4	pCtosBuffer	4	Pointer to the CTOS operating system buffer that was saved by the bootstrap ROM before booting the new operating system.
8	DumpDevice	1	Dump device code, where 0 means no dump occurred, 1 means dump to floppy, 2 means dump to floppy disk (standalone and common), and 3 means dump over RS-422 line to master workstation (cluster or common ROM only).
9	BootDevice	1	Boot device code; follows the same format as the dump device code, above.
10	WsType	1	Workstation type number, as defined by SW2 setting (common bootstrap ROM only).
11	DumpUnit	1	Hard disk unit number if dump device is 2, ID if 3, and error number if 0.
12	BootUnit	1	Same as dump unit.
13	unused	1	
14	WsNumber	1	ID number if common bootstrap ROM.
15	fixedWsNumber	1	True means SW2 settings are for fixed ID mode (common bootstrap ROM only).

For the cluster, standalone, and common (version 2) ROMs, the bootstrap interface block starts at 1F00:0000. The common bootstrap ROM, version 4, has a pointer to the bootstrap interface block at 0:1FC. The bootstrap interface block may be located anywhere in memory as long as it is above the operating system.

CTOS Operating System Buffer

The standalone and cluster bootstrap ROMs save a 64-byte buffer for the CTOS operating system. The common bootstrap ROMs save a 256-byte buffer for the operating system. The CTOS operating system has a pointer to this buffer at location 0000:0240h. The buffer must be within the first 124K bytes of RAM. The bootstrap ROM copies this buffer into its work area and sets the pointer (pCtosBuffer) to this copy in the bootstrap interface block. The CTOS operating system then uses this pointer to recover the buffer after it has been bootstrapped.

4. PANEL (VIRTUAL CONSOLE DEBUGGER)

The bootstrap ROM program contains Panel, a virtual console debugger. While not comprehensive enough for general software debugging, Panel is designed for use when the workstation is unable to run the operating system. The Panel debugger allows the user to perform the following functions:

- o examine or modify RAM
- o examine or modify internal registers
- o input or output to or from a port
- o set haltpoints

Since a workstation is not booted up when Panel is used, the workstation video terminal cannot be used during debugging. To use Panel, connect an interactive ASCII CRT terminal (or another workstation executing the Asynchronous Terminal Emulator utility) to the connector marked "Channel B" located on the rear panel of the workstation. This terminal must be EIA RS-232 compatible. Set the terminal to full duplex and to 9600 baud for standalone and cluster ROMs, or to 300 baud for common ROMs. Since the terminal is DTE, or data terminal equipment, it should be connected using a crossed RS-232-C cable. (Pins 2 and 3, the Receive Data and Transmit Data signals, are crossed for a crossed RS-232-C cable.) The terminal may also be connected via a modem that meets the above specifications.

Panel may be entered in three different ways:

1. from the bootstrap ROM program, if an error is detected or if SW2 switches are set to enter Panel
2. from a haltpoint set while in Panel
3. from execution of the Assembly language instruction INT 7Ch after the bootstrap ROM program has set up interrupt vectors at location 0000:01F0h

The ROM program uses the Assembly language instruction method (3) to enter Panel. Regardless of the type of entry method used, however, any haltpoint is removed when Panel is entered.

All numbers in the Panel debugger are hexadecimal words (never bytes). Addresses must be entered in an SA:RA, hexadecimal format. SA refers to the segment base address, and RA refers to the relative address, or the number of bytes from the beginning of the segment pointed to by SA. The first digit entered must be numeric (for example, the user must enter 0FFFF rather than FFFF), and only the last four digits of any word are used, although more than one word may be entered at a time. Initially, SA is FFF0Oh. Since Panel always remembers SA, it does not have to be keyed in every time a user wishes to specify an address; thus, an address can be specified by entering SA:RA, or just RA. If an input/output port is specified, RA is used by the Panel debugger routine as the port address.

When Panel is entered, the 12 CPU word registers, the instruction pointer, and the flag register are saved on the user stack. The RAM location of each register can be addressed by typing in the register name. Register names, as they are located in memory, are as follows: SP, SS, ES, DS, BP, DI, DX, CX, BX, AX, SI, IP, CS, and FL. Byte registers cannot be addressed in this manner, since Panel does not support byte memory operations. Note that, because of the characteristics of the 8086/8088 family of microprocessors, the AX register is composed of the AL and AH registers, the BX register is composed of the BL and BH registers, and so forth.

When Panel is entered, the address of the instruction that caused the entry is displayed on the video terminal screen. This address is displayed in CS:IP format. (For more information on CS:IP format, see "Register Structure" under "8086 Machine Organization," in The Central Processing Unit.) If the entry was caused by a haltpoint imbedded in the code, IP is decremented by two bytes, so that the instruction where the haltpoint was set can be executed when Panel is exited. After the address display, a + prompt appears on the screen. This prompt indicates that Panel is waiting for a command.

To enter Panel without specially setting the I/O Memory board switches, proceed as follows:

1. Connect a terminal or modem to the workstation as described above.

2. Turn the Mass Storage Subsystem (MSS) off or disconnect the communications cable, and press RESET.

3. Press the space bar on the peripheral terminal's keyboard.

The bootstrap ROM checks for this condition in the Dump and Boot routines just before trying each device. The Panel + prompt is displayed on the screen as soon as the ROM reaches one of these checks. When the + prompt appears, the ES and DX registers can be set as described in Subsection 3 of this appendix.

4. When you have set ES and DX, type 0FFFF:0G to bootstrap with the specified options.

Panel Interface

Panel recognizes the ASCII return key <CR>, the linefeed key <LF>, and the following ASCII characters: :, /, 0 to 9, and A to Z (upper- or lowercase). If other characters or keys are typed, the screen displays

```
BEL
```

(07h error code), and the previously specified command is terminated before execution. In the following examples, Panel displays

```
xxxx,  , =,
```

and the address at the beginning of lines that do not begin with +, that is, lines that require operator input. Note that the ASCII codes for <CR> and <LF> are inverted relative to the Convergent Technologies codes for <CR> and <LF>.

Description of Panel Commands

This subsection describes the following Panel commands:

- Open/Modify RAM
- Open/Modify Register
- Input/Output to or from an I/O port

- Set Haltpoint
- Proceed/Go

The Open/Modify RAM command may be used to

- modify a word of RAM and terminate the command
- modify a word of RAM and open the next (chosen) word of RAM
- examine a word of RAM and open the next (chosen) word of RAM
- examine a word of RAM and terminate the command

To use the Open/Modify RAM command, type the address of the RAM location that you wish to examine, followed by a diagonal (/). This "opens," or displays, the word of RAM at that location.

Example:

To modify the word at RAM location F00:3Ch to be 701h, enter

```
+   0F00:3c/ xxxx 701h <CR>
```

where xxxx denotes the number that is displayed by the Panel program for the old value at the location.

Example:

To change words at 0:0 and 0:4 to 3F0h and 23h respectively, and also to examine words at 0:2 and 0:6 without modifying them, enter

```
+   0:0/ xxxx 3F0 <LF>
0000:0002 xxxx <LF>
0000:0004 xxxx 23 <LF>
0000:0006 xxxx <CR>
```

The Open/Modify Register command may be used to perform the same functions as the Open/Modify RAM command. Typing in a register name at the + prompt is the same as typing in the address of the RAM location where the register contents is stored, followed by a /.

Example:

To change the contents of register DX to A03h, enter

```
+   DX xxxx 0A03 <CR>
```

(Note that it is necessary to type in "0A03" instead of just "A03".)

To use the Input/Output to or from a Port command to input a word to a port, type an address (an entry in RA:SA format will be ignored) followed by the letter I. A word is then input from the port, the word is displayed, and the command is terminated.

To output a word to a port, type an address followed by the letter O. Panel displays = (an equal sign). Type the word to be output to the port, then type <CR>. Note that the Output Port command does not input from the port. This arrangement accommodates I/O controllers that change state when their I/O port is read.

Example:

To input the contents of port 44h, enter

```
+   44I xxxx
+
```

Example:

To output 4400h to port 56h, enter

```
+   5600h=4400h <CR>
+
```

The Set Haltpoint command sets a haltpoint when an internal Panel flag is set up. To use this command, type the RAM address, followed by the letter H. This procedure sets an internal Panel flag, or haltpoint, and stores the address for later use. When Panel is exited (when a G or P is typed), the haltpoint is inserted into RAM at the specified address. Only one haltpoint can be set at a time; if more than one is specified, only the last is used.

Once the haltpoint is executed, the original instruction at that address is restored and can be executed by typing the letter P. The Panel

program remembers the existence and location of a haltpoint by storing information in 16 bytes reserved at 0000:01F0h.

To avoid conflict with the single-byte INT instruction (3h) for the operating system debugger, the Panel haltpoint INT is a two-byte instruction (7Ch). If the haltpoint is set as a single-byte instruction, with a jump to the following instruction, the results cannot be determined.

NOTE
A haltpoint cannot be set in ROM.

Setting a haltpoint at the current CS:IP will cause Panel to be reentered immediately when the letter P is typed. To reestablish a haltpoint at the same address, set a haltpoint at the next instruction, type the letter P, set a haltpoint at the desired address, and type the letter P again. (The letter P is used to exit Panel. For more information on exiting Panel, see the Proceed/Go command description, below.)

Example:

To set a haltpoint at address 1E21:C3h, enter

```
+   1E21:0C3H
+
```

The Proceed/Go command is used to exit the Panel program. Either the letter P is typed, or an address, followed by the letter G, is typed. If the Proceed command is used to exit Panel, the execution is resumed at the current CS:IP, which are saved on the stack. If the GO command is used to exit Panel, the program resumes execution at the address typed prior to the letter G.

Example:

To proceed from the current CS:IP, enter

```
+   P
```

Example:

To resume execution at address 1E43:90h, enter

```
+   1E43:90G
```

5. ROM ERROR CODES

When the IWS workstation is bootstrapped, it goes through diagnostic, memory dump, and bootstrapping routines which are resident in the ROM. These routines light LEDs on the I/O Memory board and on the keyboard. When an error is detected by the ROM program, that error code is displayed on eight keyboard LEDs: OVERTYPE (OT), LOCK (LK), F1, F2, F3, F8, F9, and F10. (OT indicates the most significant bit of the error code; F10, the least.)

This subsection describes each error code and lists corresponding reasons or sources for such a failure. In most cases, a list of possible causes follows each error code. These causes are listed in order from most to least likely.

When an error code is displayed on the workstation keyboard LEDs, the workstation beeper is cycled on and off. This cycling continues indefinitely if the bootstrap ROM program was entered from a CTOS operating system crash, five times if the bootstrap ROM was entered from power-up or a reset, and three times if a boot timeout error (40h) occurs.

Before performing each diagnostic test, the bootstrap ROM program displays which diagnostic test it is about to run on the six I/O Memory board LEDs, CR1 through CR6. If an error occurs during the test, the same LED pattern that is displayed on the keyboard LEDs F1, F2, F3, F8, F9, and F10 is left on the I/O Memory board. (CR1 through CR6 display the lower six bits of an error code.)

The I/O Memory board LEDs should only be examined if the workstation beeper is cycling or if the processor has stopped executing. If the error code shown on the I/O Memory board LEDs is different from the error code shown on the workstation keyboard, the I/O Memory board LEDs are more likely to be correct.

If the workstation beeper does not cycle and there has been no disk activity, the problem is probably with the processor or with power. If the beeper does not cycle and there has been disk activity, the problem could lie within the operating system or diagnostic being loaded, the beeper could be broken, or the I/O Memory board

switches could be set improperly (SW2 on the I/O Memory board has a default setting of all switches ON.)

Using Panel to Diagnose Error

If a peripheral CRT and keyboard are connected to the workstation, the Panel debugger program can be entered by pressing the space bar (20h), the carriage return (0Dh), or the ESCAPE key (1Bh) on a dumb terminal.

> NOTE
>
> If the error code is 40h (boot timeout), the space bar entry to Panel must be performed within five seconds after the error code is displayed, or the ROM program will continue trying to bootstrap.

The 8086 register CX is set up to contain the error code before Panel is entered. If the error is a memory error, information related to the error is contained in registers DS, DI, SI, and BP, as follows:

Register	Contents
CX	error code
DS	Segment base address of memory error
DI	Offset address of memory error
SI	Data written to memory
BP	Data read back from memory

If there is an error in RAM, Panel could be unreliable, as it uses RAM (0:1D0 to 0:1F0) for its stack, and uses its stack for internal argument passing and to save the values of registers. (Panel saves flags and register values when it is entered and restores them when it is exited.) Note that the only valid values of DS when a

memory error occurs are those in which the last three digits are 0, such as 0000h, 1000h, etc. This information can be used to measure the reliability of Panel. In the case of a memory Read/Write error (60h), the only valid values of SI are 0000h, FFFFh, and (DS+DI). In the case of a memory addressing error (80h), SI can only be (DS+DI). Register DI ranges from 0000h to FFFEh and is always even.

Error Code Display

The 2716 ROMs display their error codes on the six LEDs located on the I/O Memory board; 2732s display their error codes on the eight keyboard LEDs described below. Both methods of error display are accompanied by the system speaker; it beeps three times for a boot timeout error, and five times if a hardware error occurs.

You can determine the ROM type by looking at the keyboard LEDs after pressing the RESET button. If the system has a 2732 ROM, it displays a 1 (the F10 key lights), then a 21h (the F1 and F10 keys light), and an A1 (the OVERTYPE, F1, and F10 keys light). All LEDs light at the end of a successful boot. There is no display during a boot if your system has a 2716; only error codes are displayed.

Interpreting Error Codes

The error code displayed on the keyboard LEDs is interpreted as an 8-bit value, with the following bit assignments:

OVERTYPE (OT)	Bit 7 (msb)
LOCK (LK)	Bit 6
F1	Bit 5
F2	Bit 4
F3	Bit 3
F8	Bit 2
F9	Bit 1
F10	Bit 0

Example

If the keyboard displays an error code with keyboard LEDs F1, F8, F9, and F10 on and the rest off, the error code is 00100111 (27h), indicating that the disk (hard disk unit 0) has an invalid volume home block.

Example

If the keyboard displays an error code with the LOCK LED on and the rest off, the error code is 01000000 (40h), which indicates that the bootstrap ROM program could not find a device to boot from after 30 seconds of trying (note that this error code is displayed for 5 seconds, and then the bootstrap ROM continues trying to boot).

The contents of the LEDs on the keyboard and I/O Memory board change as the bootstrap ROM executes. As mentioned, the contents of these LEDs should be examined only if the beeper is cycling or the processor has stopped executing.

Common Bootstrap ROM Error Code List

This is a description of each error code and the possible sources for the failure. The following error code descriptions are listed in hexadecimal format and apply to the common bootstrap ROMs. In most cases, the error code description is followed by a list of possible causes, listed in order from most to least probable.

Following the error code descriptions are quick reference guides for the common, standalone, and cluster bootstrap ROMs. Unlike the error code descriptions, quick reference guides list errors in binary format, followed by a short error summary. The quick reference guide for standalone and cluster bootstrap ROMs also lists a hexadecimal number corresponding to a common bootstrap ROM error. This hexadecimal number can be used to obtain error code descriptions for standalone and cluster bootstrap ROMs.

Error codes for the common bootstrap ROM are listed in the following format:

Code (hex)	Meaning
00	No power or inoperative keyboard. If the beeper is cycling, the keyboard may be inoperative. If the keyboard is inoperative, the lower six bits of the error code are displayed on the I/O Memory board LEDs as described above. If the beeper is not cycling and there is no disk activity, check the power. If there is disk activity, the problem may be with the program that was booted. Note that it can take as long as 5 minutes for a cluster workstation CTOS operating system to initialize if the master workstation is heavily loaded. Check: The workstation power indicator The cable from the keyboard to the workstation The keyboard Software in SysImage.Sys file
01	Starting floppy dump or boot. This is not an error. This code is displayed on the LEDs just before a dump or boot is started, and it is left there until the dump or boot is completed successfully or an error occurs.
02	No floppy disk controller. A timeout occurred when the ROM program tried to access the floppy disk controller port (port 72h). The DCI cable could be disconnected or the floppy disk controller could

Code (hex)	Meaning
02 (cont.)	be stalled, in which case the workstation should be powered down and up again to clear the error. Check: The DCI cable connection (both ends) The I/O Memory board The CPU board
03	Floppy disk controller register did not become ready in 3 seconds. The sequencer in the floppy disk controller was never ready to be used (that is, port 72h was not 80h). There is probably no power to the disk controller or, as mentioned for 02h, the floppy disk controller could be stalled, in which case the workstation should be powered down, and then up again. Check: The power-on indicator The Floppy Disk Controller or SMD Controller board The I/O Memory board The CPU
04	Data-in bit set in command. The floppy disk controller was trying to send information to the processor while the processor was trying to send a new command to the controller. Usually this error code means that the floppy disk controller received an invalid command. However, this error can also result from a defective or poorly connected DCI cable.

Code (hex)	Meaning
04 (cont.)	Check: The DCI cable The Floppy Disk Controller board or the SMD Controller board The I/O Memory board The CPU
05	Data-in bit not set in result. When the processor expected result information, none was available. This error is similar to error 03. Check: The DCI cable The Floppy Disk Controller board or the SMD Controller board The I/O Memory board The CPU
06	DMA not completed. At the end of a disk transfer, the 8237 DMA count register was not 0FFFFh. This condition indicates a DMA problem. The DCI cable and the boards listed below can also cause this error, however. Check: The DCI cable The CPU The Floppy Disk Controller board or the SMD Controller board The I/O Memory board The Video board

Code (hex)	Meaning
07	Volume home block checksum error. The first block of information read from the floppy disk into memory is invalid. This might be because the floppy disk in drive 0 was never processed by the Initialize Volume utility. This error might also occur because the floppy disk is defective, the DMA logic is storing the wrong data in memory, or the floppy disk controller is malfunctioning. Check: The floppy disk The DCI cable The CPU The Floppy Disk Controller board or the SMD Controller board The I/O Memory board
08	No file on floppy disk. The volume home block on the floppy disk in drive 0 has a length of 0 for the file (SysImage.Sys in boot, Crashdump.Sys in dump) that contains the program to be booted. When the Initialize Volume utility processed the floppy, the number of pages for the file was zero. Check: The floppy disk
09	Run file checksum.
0A	File header invalid. This description applies to both 09 and 0A. The system image file on the floppy disk in drive 0 does not contain a valid run file. You must copy a valid system image onto it. The Initialize Volume utility does

Code (hex)	Meaning
0A (cont.)	NOT automatically copy a system image onto the volume it is initializing. Check: The floppy disk
0B	Floppy disk controller register inconsistent. The floppy disk controller register was polled until it became ready (port 72h was 80h), but the next time it was polled it was not ready. Check: The DCI cable The Floppy Disk Controller or SMD Controller board The I/O Memory board The CPU
0C	Floppy disk drive became not ready during seek. The floppy disk drive went not ready while seeking. Usually the operator causes this error by opening the door of the drive. Other causes are a bad floppy disk or a bad cable from the floppy disk controller to the drive. Check: The floppy disk drive The disk drive cable The Floppy Disk Controller or SMD Controller board
0D	Invalid floppy disk command received. This error code occurs when the floppy disk controller receives an undefined command during the seek/recalibrate phase. It is

Code (hex)	Meaning
0D (cont.)	usually caused by a defective DCI cable rather than a defective floppy disk controller. Check: The DCI cable The Floppy Disk Controller or SMD Controller board The I/O Memory board
0E	Floppy disk drive NOT ready. The floppy disk drive was not ready when the Seek or Recalibrate command was issued. Check: The floppy disk is in drive 0 The floppy disk label is on the side opposite the release latch The door is closed properly
0F	Floppy disk drive fault condition during seek/recalibrate. This floppy disk drive failure occurs when the floppy disk does not recalibrate after 77 step pulses or when the drive fault line goes active. Check: The floppy disk drive The disk drive cable
10	Abnormal termination of seek. If the floppy disk did not finish a seek correctly, the drive could be defective or the ready status could have changed.

Code (hex)	Meaning
10 (cont.)	Check: Operator The floppy disk The floppy disk drive The Floppy Disk Controller board or the SMD Controller board
11	Floppy disk drive became not ready. The floppy disk drive went not ready during a data transfer. Usually the operator causes this error by opening the door of the drive. Check: Operator The floppy disk The disk drive The disk drive cable The Floppy Disk Controller board or the SMD Controller board
12	Invalid floppy disk command received. This error occurs if the floppy disk controller receives an undefined command when the ROM requests a data transfer. It is possibly due to a defective DCI cable. Check: The DCI cable The Floppy Disk Controller board or the SMD Controller board The I/O Memory board

Code (hex)	Meaning
13	Floppy disk drive not ready. This error can only occur if the floppy disk was ready during a previous recalibrate and seek. It is caused by the floppy disk drive not being ready when the Read or Write command is issued. The most likely cause for this error is removing the floppy disk after the bootstrap sequence has started. Check: Operator
14	Floppy disk fault condition during data transfer. Floppy disk drive fault line went active. Check: The floppy disk drive The disk drive cable
15	End of cylinder. After a read or write, no EOP signal is received from the DMA logic. This error usually indicates either a DCI problem or a DMA problem. Check: The DCI cable The 8237 CPU The Floppy Disk Controller board or the SMD Controller board The I/O Memory board
16	Data error: data field. The floppy disk controller was unable to read data from the floppy disk correctly. Usually the floppy disk is defective. Other possible causes are the disk cable or the floppy disk controller.

Code (hex)	Meaning
16 (cont.)	Check: The floppy disk The floppy disk drive The disk drive cable The Floppy disk Controller board or the SMD Controller board
17	Data error: ID field. The floppy disk controller was unable to read the ID of the addressed sector. Usually the floppy disk is defective. Other possibilities are the disk drive cable or the floppy disk controller. Check: The floppy disk The floppy disk drive The disk drive cable The Floppy Disk Controller board or the SMD Controller board
18	Data late. The floppy disk controller did not get service from the DMA chip in time for the floppy disk. Check: The 8237 CPU The DCI cable The Floppy Disk Controller board or the SMD Controller board The I/O Memory board The Video board

Code (hex)	Meaning
19	No data: wrong cylinder. During a read or write operation, the floppy disk was on the wrong cylinder. That is, either the floppy disk was initialized incorrectly or a seek went to the wrong place. Check: The floppy disk The floppy disk drive The disk drive cable The Floppy Disk Controller board or the SMD Controller board
1A	No data: bad cylinder. The cylinder accessed is marked as number 255 (0FFh). Check: The floppy disk The Floppy Disk Controller board and the SMD Controller board
1B	No data. The floppy disk controller reported a no data condition. This means that the specified sector could not be found. Most likely, the floppy disk is defective. Check: The floppy disk The floppy disk drive The disk drive cable The Floppy Disk Controller board or the SMD Controller board

Code (hex)	Meaning
1C	Floppy disk write protected. This error is never sent to the keyboard LEDs, because it can only occur in the dump when the floppy is being written to.
1D	Missing address mark: data field. The floppy disk controller was unable to find the data address mark of a sector. Usually this means that the floppy disk is no good. Check: The floppy disk The floppy disk drive The disk drive cable The Floppy Disk Controller board or the SMD Controller board
1E	Missing address mark: ID field. The floppy disk controller was unable to find any ID address mark on a track. Usually this is because the floppy disk has not been initialized by the Initialize Volume utility. Check: The floppy disk The floppy disk drive The disk drive cable The Floppy Disk Controller board or the SMD Controller board
1F	Abnormal termination of command (no specified cause). The floppy disk controller reported abnormal termination of a data command without reporting any cause.

Code (hex)	Meaning
1F (cont.)	Check: The Floppy Disk Controller board or the SMD Controller board
20	ROM checksum error. There is a bad ROM chip on the CPU board (location F14 or F15). Check: CPU board (2716 or 2732 ROMs)
21 to 2B	Same as 01 to 0B. These error codes are for hard disk unit 0; they are the same as those for the floppy disk, except that the controller is the Hard Disk Controller board (or SMD Controller board), and the Control register is port 7Ah.
2C	Invalid hard disk command received. The disk controller thinks that it has received an undefined command from the processor. Usually this is due to a defective DCI cable. Check: DCI cable The Hard Disk Controller board or the SMD Controller board I/O Memory board The 8237 CPU
2D	Drive not ready. The disk drive (unit 0) was not ready when the Seek or Recalibrate command was issued. Check: Power indicator on disk drive

Code (hex)	Meaning
2E	Hard disk fault condition during seek/recalibrate. Hard disk drive (unit 0) failure (did not recalibrate after 77 step pulses or the drive fault line goes active). Check: The hard disk drive The disk drive cable
2F	Abnormal termination of seek. This error indicates that the hard disk did not finish a seek correctly. Either the drive (unit 0) failed or the ready status changed. Check: The hard disk The hard disk drive The disk drive cable The Hard Disk Controller board or the SMD Controller board
30	Unit became not ready. The hard disk drive (unit 0) went not ready during a data transfer. Check: The hard disk drive The hard disk drive cable The Hard Disk Controller board or the SMD Controller board
31	Invalid command: bad head.
32	Invalid command: bad sector.
33	Invalid command: bad cylinder.
34	Invalid hard disk command issued.

Code (hex)	Meaning
31-34 (cont)	The hard disk controller thinks it received an illegal parameter or an undefined command from the processor. This error is usually due to a bad DCI cable. Check: DCI cable The Hard Disk Controller board or the SMD Controller board The I/O Memory board
35	Drive not ready. The disk drive (unit 0) was not ready when the Read or Write command was issued. This error can only occur if the disk was ready during a previous recalibrate and a previous seek, and then went not ready. Check: The DCI cable The Hard Disk Controller board or the SMD Controller board The I/O Memory board
36	Hard disk fault condition during I/O. Hard disk drive (unit 0) failure (drive fault line goes active). Check: The DCI cable The hard disk drive
37	Data late. The hard disk controller did not get service from the DMA chip in time to satisfy the hard disk.

Code (hex)	Meaning
37 (cont.)	Check: The 8237 CPU The DCI cable The Hard Disk Controller board or the SMD Controller board The I/O Memory board
38 39	Data CRC. ID CRC. A Cyclical Redundancy Check (parity error) occurred in a sector read (for a data CRC), or in the address information of the sector (for an ID CRC). This generally means an error on the hard disk (unit 0). Check: The hard disk The data separator (on the Floppy Disk Controller board) The disk drive cable The Hard Disk Controller board or the SMD Controller board
3A	Halt during execution. The hard disk controller received a Halt command during execution of some other command. Usually this is due to a bad DCI cable. Check: The DCI cable The Hard Disk Controller board or the SMD Controller board The I/O Memory board The 8237 CPU

Code (hex)	Meaning
3B	Sector not found. The sector in a read or write command was not found on the track (unit 0). This could be because no sector mark or no matching sector number was found. Check: The hard disk The data separator (on the Floppy Controller board) The disk drive cable The Hard Disk Controller board or the SMD Controller board
3C	Abnormal termination of command (no specified cause). The hard disk reported abnormal termination of a data command without reporting any cause. Check: The Hard Disk Controller board or the SMD Controller board
3D	Invalid disk parameters. The parameters returned by the hard disk controller, for either the number of sectors per cylinder or the number of cylinders per head, were zero. Check: The Hard Disk Controller board or the SMD Controller board
3E	Not used.
3F	Not used.

Code (hex)	Meaning
40	Boot timeout. If the boot program cannot find a floppy or hard disk that is ready and contains a system image, before the communications routine times out (error code 0A2h), the program retries all devices. After four complete cycles, this error code is displayed, and the beeper sounds three times. This error code is displayed for 8 sec. If a video terminal is attached and the correct character is typed on the keyboard, Panel can be entered; otherwise the program recycles. After each subsequent set of four cycles, the error code is displayed for 5 sec, but the beeper does not sound again. The error codes that may be reported as 40h are 02h, 22h, 42h, 62h, 82h (no DCR); 08h, 28h, 48h, 68h, 88h (unit has no system image file); 0Eh, 2Dh, 4Dh, 6Dh, 8Dh (unit not ready); and 0A2h (never polled).
41 to 5F	Same as 21 to 3F. These error codes are for disk unit 1; they are the same as those for disk unit 0.
60	RAM read/write test error. An error occured during the read/write RAM test; all ones, all zeros, and the sum of DS and DI were written and then read and compared. This error code indicates that the comparison failed. Check: I/O Memory board insertion I/O Memory board The 8237 CPU

Code (hex)	Meaning
61 to 7F	Same as 21 to 3F. These error codes are for disk unit 2; they are the same as those for disk unit 0.
80	RAM address test error. An error occurred during the RAM addressing test. After the completion of the RAM read/write test, each RAM word must contain the sum of its own DS and DI. The RAM address test verifies that this is true. This error can result from a short that causes data for different addresses to be written to the same RAM. It can also be caused by memory that picks or drops bits when idle. Check: I/O Memory board insertion The I/O Memory board The 8237 CPU
81 to 9F	Same as 21 to 3F. These error codes are for disk unit 3; they are the same as those for disk unit 0.
A0	Communications data transfer.
A1	Doing dump or boot. This code is displayed at the start of a dump or boot; it is left there until the master protocol is initialized or until an error occurs. Once the protocol is established, the codes 0A0h and 0A1h are shown alternately after every successful data transfer. This does not indicate any problem. This code is cleared at the end of the boot or dump procedure.

Code (hex)	Meaning
A2	Never polled. This indicates a nonfatal error and occurs when a disk waits 10 seconds for an initial poll from the master workstation. This error is reported during the boot initialization routine as part of error code 40h. It is never displayed in the LEDs of the keyboard. Check: The communications cable The I/O Memory board (SIO or RS-422 receivers) Master workstation operating system must be running
A3	SIO error. This error is shown when the SIO initialization routine detects an error in the SIO communications controller IC. Check: The I/O Memory board (SIO port)
A4	8253 error. The Clock Initialization routine detects an error in the programmable counter/timer IC. Check: The I/O Memory board (8253)
A5	No SIM. A RIM was sent to the master workstation, but no answering SIM was received. This can indicate that the workstation is able to receive but not transmit, or that the master workstation is able to transmit but not receive.

Code (hex)	Meaning
A5 (cont.)	Check: The I/O Memory board (SIO or RS-422 receivers/drivers) The master workstation The communications cable The master workstation CTOS operating system (for a crash)
A6	No UP in initialization (SNRM). A UA or XID was sent to acknowledge the SIM sent by the master, but the master sent back an SNRM instead of a UA. This is probably caused by the master timing out while waiting for the UA or XID. Check: The I/O Memory board (SIO or RS-422 receivers/drivers) The master workstation The communications cable The master workstation CTOS operating system (for a crash)
A7	No UP in initialization (DISC). A UA or XID was sent to acknowledge the SIM sent by the master, but the master sent back a DISC instead of a UA. The most likely cause is that switches are set for something other than fixed WsNumber mode, and the master workstation CTOS operating system is version 4.x or earlier, which does not accept the XID as valid protocol.

Code (hex)	Meaning
A7 (cont.)	Check: Switch settings The I/O Memory board (SIO or RS-422 receivers/drivers) The master workstation The communications cable The master workstation CTOS operating system (for a crash)
A8	No UP in initialization. A UA or XID was sent to acknowledge the SIM sent by the master, but the master sent back something else instead of a UA. Check: The I/O Memory board (SIO or RS-422 receivers/drivers) The master workstation The communications cable
A9	No ID available. The initialization routine listened to the communications line but never found a free ID number. This is usually caused by attaching more workstations to a line than the master workstation CTOS operating system can handle. Check: The master workstation CTOS operating system (for a crash)
AA	ID failure. The initialization routine found free ID numbers when it listened to the communications line, but errors were detected every time it tried to use a number. This error is usually

Code (hex)	Meaning
AA (cont.)	due to a failure of the collision recovery algorithm; it can be overcome by pressing the reset button on the stations that have collided.
AB	Read ID timeout. The initialization routine timed out after 10 sec while listening to the communications line for an ID number. This error is generated only after some number of successful reads. Check: The I/O Memory board (SIO or RS-422 receivers/drivers) The master workstation The communications cable The master workstation CTOS operating system (for a crash)
AC	Bad address (dump routine). This error occurs when the workstation ID sent in a frame by the master workstation does not match the one expected. This error never is displayed on keyboard LEDs because the program continues to do a memory test and then boot.
AD	Disconnected (dump routine). The master workstation sends a DISC because of excessive line or protocol errors, because there is no file to which to write the memory dump, or because the file is not large enough for the entire dump. This error is never displayed on keyboard LEDs because the program continues to do a memory test and then boot.

Code (hex)	Meaning
AE	No UP: SNRM
AF	No UP: REJ
B0	No UP
	After the dump block was transmitted, an unexpected response was received from the master workstation. These errors are never displayed on keyboard LEDs because the program continues to do a memory test and then boot.
B1	Read UI error.
	A bootblock (frame type UI) is expected, but another frame type is received.
	Check: The I/O Memory board
	Duplicate workstation ID
B2	Read SNRM error.
	A bootblock (frame type UI) is expected, but an SNRM is received.
	Check: The I/O Memory board (SIO)
B3	Disconnected.
	The master workstation decides to send a DISC due to excessive errors during transmission. This may be caused by having several workstations in the fixed WsNumber mode with the same switch settings.
	Check: The communications cables
	The I/O Memory board (SIO or RS-422 transmitters)
	Workstation IDs in fixed WsNumber mode (duplicate IDs)

Code (hex)	Meaning
B4	Bad checksum of system image. The system image transferred from the master workstation is not a valid run file. Either the file is invalid, or the transmission was faulty or incomplete. Check: Cluster workstation CTOS operating system file validity Duplicate workstation IDs (fixed WsNumber mode) The I/O Memory board (SIO or RS-422 receivers) The communications cables The master workstation CTOS operating system or IOP (for a crash)
B5	Read error. Excessive I/O errors occured while trying to read a bootblock. Check: The I/O Memory board (SIO or RS-422 receivers) The communications cables
B6	Read timeout. During a read operation, no response was received from the master workstation. Check: The master workstation CTOS operating system (for a crash)
B7	Write DMA count bad. This error occurs after completion of a write operation, if the entire block has not been sent.

Code (hex)	Meaning
B7 (cont.)	Check: The I/O Memory board (SIO) The 8237 CPU
B8	Write timeout. A write operation did not properly go to completion. Check: The 8237 CPU The I/O Memory board (SIO or 8253)
B9	Bad bootblock format. An illegal length bootblock was received. Check: The boot file format
BA	DMA error. After initializing the DMA for a read or write, the 8237 DMA controller does not contain the same information as was written to it. Check: The 8237 CPU The I/O Memory board The Video board
BB to FE	Not used.
FF	Successful boot. This is not an error. This code is displayed on the keyboard LEDs for one second just before the bootstrap ROM jumps into the program that it loads.

Common Bootstrap ROM Error Code Quick Reference List

In the following lists, x indicates a lighted LED; o indicates an unlit LED.

Floppy Disk Controller Errors [f0]

Keyboard LEDs					
O	L	123	890	Code	Description
o	o	ooo	ooo	00	Unused (possibly inoperative keyboard)
o	o	ooo	oox	01	Starting floppy dump or boot
o	o	ooo	oxo	02	No floppy disk controller (FDC)
o	o	ooo	oxx	03	FDC did not become ready
o	o	ooo	xoo	04	Data-in bit set in command
o	o	ooo	xox	05	Data-in bit not set in result
o	o	ooo	xxo	06	DMA not completed
o	o	ooo	xxx	07	Volume home block checksum error
o	o	oox	ooo	08	No file on floppy disk
o	o	oox	oox	09	Run file checksum
o	o	oox	oxo	0A	File header invalid
o	o	oox	oxx	0B	FDC inconsistent
o	o	oox	xoo	0C	Floppy disk drive became not ready during a seek
o	o	oox	xox	0D	Invalid floppy disk command received
o	o	oox	xxo	0E	Floppy disk drive not ready
o	o	oox	xxx	0F	Floppy disk drive fault during seek/recalibrate
o	o	oxo	ooo	10	Abnormal termination of seek
o	o	oxo	oox	11	Floppy disk drive became not ready
o	o	oxo	oxo	12	Invalid floppy disk command received
o	o	oxo	oxx	13	Floppy disk drive not ready

Keyboard LEDs					
O	L	123	890	Code	Description
o	o	oxo	xoo	14	Floppy disk fault during data transfer
o	o	oxo	xox	15	End of cylinder
o	o	oxo	xxo	16	Data error: data field
o	o	oxo	xxx	17	Data error: ID field
o	o	oxx	ooo	18	Data late
o	o	oxx	oox	19	No data: wrong cylinder
o	o	oxx	oxo	1A	No data: bad cylinder
o	o	oxx	oxx	1B	No data
o	o	oxx	xoo	1C	Floppy disk is write protected
o	o	oxx	xox	1D	Missing address mark: data field
o	o	oxx	xxo	1E	Missing address mark: ID field
o	o	oxx	xxx	1F	Abnormal termination of command
o	o	xoo	ooo	20	ROM checksum error

Disk Unit 0 Errors [d0] (SMD Controller board [f0])

Keyboard LEDs					
O	L	123	890	Code	Description
o	o	xoo	oox	21	Starting disk dump or boot
o	o	xoo	oxo	22	No hard disk controller (HDC)
o	o	xoo	oxx	23	HDC did not become ready
o	o	xoo	xoo	24	Data-in bit set in command
o	o	xoo	xox	25	Data-in bit not set in result
o	o	xoo	xxo	26	DMA not completed
o	o	xoo	xxx	27	Volume home block checksum error
o	o	xox	ooo	28	No file on disk
o	o	xox	oox	29	Run file checksum
o	o	xox	oxo	2A	File header invalid
o	o	xox	oxx	2B	Disk Control register inconsistent
o	o	xox	xoo	2C	Invalid hard disk command received
o	o	xox	xox	2D	Drive not ready
o	o	xox	xxo	2E	Hard disk fault condition during seek/recalibrate
o	o	xox	xxx	2F	Abnormal termination of seek
o	o	xxo	ooo	30	Unit became not ready
o	o	xxo	oox	31	Invalid command: bad head
o	o	xxo	oxo	32	Invalid command: bad sector
o	o	xxo	oxx	33	Invalid command: bad cylinder
o	o	xxo	xoo	34	Invalid hard disk command issued
o	o	xxo	xox	35	Drive not ready
o	o	xxo	xxo	36	Hard disk fault condition during I/O
o	o	xxo	xxx	37	Data late
o	o	xxx	ooo	38	Data CRC

Keyboard LEDs					
O	L	123	890	Code	Description
o	o	xxx	oox	39	ID CRC
o	o	xxx	oxo	3A	Halt during execution
o	o	xxx	oxx	3B	Sector not found
o	o	xxx	xoo	3C	Abnormal termination of command
o	o	xxx	xox	3D	Invalid disk parameters
o	o	xxx	xxo	3E	(unused)
o	o	xxx	xxx	3F	(unused)
o	x	ooo	ooo	40	Boot timeout

Disk Unit 1 Errors [d1] (SMD Controller board [d0])

Keyboard LEDs					
O	L	123	890	Code	Description
o	x	ooo	oox	41	Starting disk dump or boot
o	x	ooo	oxo	42	No hard disk controller (HDC)
o	x	ooo	oxx	43	HDC did not become ready
o	x	ooo	xoo	44	Data-in bit set in command
o	x	ooo	xox	45	Data-in bit not set in result
o	x	ooo	xxo	46	DMA not completed
o	x	ooo	xxx	47	Volume home block checksum error
o	x	oox	ooo	48	No file on disk
o	x	oox	oox	49	Run file checksum
o	x	oox	oxo	4A	File header invalid
o	x	oox	oxx	4B	HDC inconsistent
o	x	oox	xoo	4C	Invalid hard disk command received
o	x	oox	xox	4D	Drive not ready
o	x	oox	xxo	4E	Hard disk fault condition during seek/recalibrate
o	x	oox	xxx	4F	Abnormal termination of seek
o	x	oxo	ooo	50	Unit became not ready
o	x	oxo	oox	51	Invalid command: bad head
o	x	oxo	oxo	52	Invalid command: bad sector
o	x	oxo	oxx	53	Invalid command: bad cylinder
o	x	oxo	xoo	54	Invalid hard disk command issued
o	x	oxo	xox	55	Drive not ready
o	x	oxo	xxo	56	Hard disk fault condition during I/O
o	x	oxo	xxx	57	Data late
o	x	oxx	ooo	58	Data CRC

Keyboard LEDs O	L	123	890	Code	Description
o	x	oxx	oox	59	ID CRC
o	x	oxx	oxo	5A	Halt during execution
o	x	oxx	oxx	5B	Sector not found
o	x	oxx	xoo	5C	Abnormal termination of command
o	x	oxx	xox	5D	Invalid disk parameters
o	x	oxx	xxo	5E	(unused)
o	x	oxx	xxx	5F	(unused)
o	x	xoo	ooo	60	Memory read/write error

Disk Unit 2 Errors (FDC or HDC board [d2],
SMD Controller board [d3])

Keyboard LEDs					
O	L	123	890	Code	Description
o	x	xoo	oox	61	Starting disk dump or boot
o	x	xoo	oxo	62	No disk controller
o	x	xoo	oxx	63	HDC did not become ready
o	x	xoo	xoo	64	Data-in bit set in command
o	x	xoo	xox	65	Data-in bit not set in result
o	x	xoo	xxo	66	DMA not completed
o	x	xoo	xxx	67	Volume home block checksum error
o	x	xox	ooo	68	No file on disk
o	x	xox	oox	69	Run file checksum
o	x	xox	oxo	6A	File header invalid
o	x	xox	oxx	6B	Disk Controller register inconsistent
o	x	xox	xoo	6C	Invalid hard disk command received
o	x	xox	xox	6D	Drive not ready
o	x	xox	xxo	6E	Hard disk fault condition during seek/recalibrate
o	x	xox	xxx	6F	Abnormal termination of seek
o	x	xxo	ooo	70	Unit became not ready
o	x	xxo	oox	71	Invalid command: bad head
o	x	xxo	oxo	72	Invalid command: bad sector
o	x	xxo	oxx	73	Invalid command: bad cylinder
o	x	xxo	xoo	74	Invalid hard disk command issued
o	x	xxo	xox	75	Drive not ready
o	x	xxo	xxo	76	Hard disk fault condition during I/O
o	x	xxo	xxx	77	Data late

Keyboard LEDs					
O	L	123	890	Code	Description
o	x	xxx	ooo	78	Data CRC
o	x	xxx	oox	79	ID CRC
o	x	xxx	oxo	7A	Halt during execution
o	x	xxx	oxx	7B	Sector not found
o	x	xxx	xoo	7C	Abnormal termination of command
o	x	xxx	xox	7D	Invalid disk parameters
o	x	xxx	xxo	7E	(unused)
o	x	xxx	xxx	7F	(unused)

Disk Unit 3 Errors (SMD Controller board [d1])

Keyboard LEDs					
O	L	123	890	Code	Description
x	o	ooo	oox	81	Starting disk dump or boot
x	o	ooo	oxo	82	No disk controller
x	o	ooo	oxx	83	HDC did not become ready
x	o	ooo	xoo	84	Data-in bit set in command
x	o	ooo	xox	85	Data-in bit not set in result
x	o	ooo	xxo	86	DMA not completed
x	o	ooo	xxx	87	Volume home block checksum error
x	o	oox	ooo	88	No file on disk
x	o	oox	oox	89	Run file checksum
x	o	oox	oxo	8A	File header invalid
x	o	oox	oxx	8B	HDC inconsistent
x	o	oox	xoo	8C	Invalid hard disk command received
x	o	oox	xox	8D	Drive not ready
x	o	oox	xxo	8E	Hard disk fault condition during seek/recalibrate
x	o	oox	xxx	8F	Abnormal termination of seek
x	o	oxo	ooo	90	Unit became not ready
x	o	oxo	oox	91	Invalid command: bad head
x	o	oxo	oxo	92	Invalid command: bad sector
x	o	oxo	oxx	93	Invalid command: bad cylinder
x	o	oxo	xoo	94	Invalid hard disk command issued
x	o	oxo	xox	95	Drive not ready
x	o	oxo	xxo	96	Hard disk fault condition during I/O
x	o	oxo	xxx	97	Data late
x	o	oxx	ooo	98	Data CRC

Keyboard LEDs					
O	L	123	890	Code	Description
x	o	oxx	oox	99	ID CRC
x	o	oxx	oxo	9A	Halt during execution
x	o	oxx	oxx	9B	Sector not found
x	o	oxx	xoo	9C	Abnormal termination of command
x	o	oxx	xox	9D	Invalid disk parameters
x	o	oxx	xxo	9E	(unused)
x	o	oxx	xxx	9F	(unused)

Communications Errors (RS-422 Cluster Line)

Keyboard LEDs					
O	L	123	890	Code	Description
x	o	xoo	ooo	A0	Communications data transfer
x	o	xoo	oox	A1	Doing dump or boot
x	o	xoo	oxo	A2	Never polled
x	o	xoo	oxx	A3	SIO error
x	o	xoo	xoo	A4	8253 error
x	o	xoo	xox	A5	No SIM
x	o	xoo	xxo	A6	No UP in initialization (SNRM)
x	o	xoo	xxx	A7	No UP in initialization (DISC)
x	o	xox	ooo	A8	No UP in initialization
x	o	xox	oox	A9	No ID available
x	o	xox	oxo	AA	ID failure
x	o	xox	oxx	AB	Read ID timeout
x	o	xox	xoo	AC	Bad address (dump routine)
x	o	xox	xox	AD	Disconnected (dump routine)
x	o	xox	xxo	AE	No UP: SNRM (dump routine)
x	o	xox	xxx	AF	No UP: REJ (dump routine)
x	o	xxo	ooo	B0	No UP (dump routine)
x	o	xxo	oox	B1	Read UI error
x	o	xxo	oxo	B2	Read SNRM error
x	o	xxo	oxx	B3	Disconnected
x	o	xxo	xoo	B4	Bad checksum of system image
x	o	xxo	xox	B5	Read error
x	o	xxo	xxo	B6	Read timeout
x	o	xxo	xxx	B7	Write DMA count bad

Keyboard LEDs					
O	L	123	890	Code	Description
x	o	xxx	ooo	B8	Write timeout
x	o	xxx	oox	B9	Bad bootblock format
x	o	xxx	oxo	BA	DMA error
x	o	xxx	oxx	BB to	
x	x	xxx	xxo	FE	(unused, except used by the CTOS operating system after boot is completed)
x	x	xxx	xxx	FF	Successful boot

Standalone Bootstrap ROM Error Code Quick Reference List

The common ROM error codes listed after each error code description can be used to look up a full description of the error in the common ROM error code descriptions at the beginning of this section.

Keyboard LEDs					
O	L	123	890	Code	Description (Common ROM Error Code)
o	o	ooo	ooo	00	(unused) (00)
o	o	ooo	oox	01	No floppy disk controller (02)
o	o	ooo	oxo	02	FDC did not become ready (03)
o	o	ooo	oxx	03	Data-in bit set in command (04)
o	o	ooo	xoo	04	Data-in bit not set in result (05)
o	o	ooo	xox	05	DMA not completed (06)
o	o	ooo	xxo	06	Volume home block checksum error (07)
o	o	ooo	xxx	07	No file on floppy disk (08)
o	o	oox	ooo	08	Run file invalid (09, 0A)
o	o	oox	oox	09	Starting seek (01)
o	o	oox	oxo	0A	Floppy disk drive became not ready during a seek (0C)
o	o	oox	oxx	0B	Invalid floppy disk command received (0D)
o	o	oox	xoo	0C	Floppy disk drive not ready (0E)
o	o	oox	xox	0D	Floppy disk drive fault during seek/recalibrate (0F)
o	o	oox	xxo	0E	Abnormal termination of seek (10)
o	o	oox	xxx	0F	Starting data transfer (01)
o	o	oxo	ooo	10	Floppy disk drive became not ready (11)
o	o	oxo	oox	11	Invalid floppy disk command received (12)

Keyboard LEDs O	L	123	890	Code	Description
o	o	oxo	oxo	12	Floppy disk fault during data transfer (14)
o	o	oxo	oxx	13	Floppy disk fault during data transfer (14)
o	o	oxo	xoo	14	End of cylinder (15)
o	o	oxo	xox	15	Data error: data field (16)
o	o	oxo	xxo	16	Data error: ID field (17)
o	o	oxo	xxx	17	Data late (18)
o	o	oxx	ooo	18	No data: wrong cylinder (19)
o	o	oxx	oox	19	No data: bad cylinder (20)
o	o	oxx	oxo	1A	No data (1B)
o	o	oxx	oxx	1B	Floppy disk is write protected (1C)
o	o	oxx	xoo	1C	Missing address mark: data field (1D)
o	o	oxx	xox	1D	Missing address mark: ID field (1E)
o	o	oxx	xxo	1E	Abnormal termination of command (1F)
o	o	oxx	xxx	1F	ROM checksum error (20)
o	o	xoo	ooo	20	Memory read/write error (60)
o	o	xoo	oox	21	No disk controller (22)
o	o	xoo	oxo	22	HDC did not become ready (23)
o	o	xoo	oxx	23	Data-in bit set in command (24)
o	o	xoo	xoo	24	Data-in bit not set in result (25)
o	o	xoo	xox	25	DMA not completed (26)
o	o	xoo	xxo	26	Volume home block checksum error (27)
o	o	xoo	xxx	27	No file on disk (28)
o	o	xox	ooo	28	Run file invalid (29, 2A)
o	o	xox	oox	29	Starting seek (21)

Keyboard LEDs 0		123	890	Code	Description
o	o	xox	oxo	2A	Disk became not ready during seek (2D)
o	o	xox	oxx	2B	Invalid Seek command: bad cylinder (2C)
o	o	xox	xoo	2C	Invalid Seek command (2C)
o	o	xox	xox	2D	Disk drive not ready during seek (2D)
o	o	xox	xxo	2E	Hard disk fault condition during seek/recalibrate (2E)
o	o	xox	xxx	2F	Abnormal termination of seek (2F)
o	o	xxo	ooo	30	Starting data transfer (21)
o	o	xxo	oox	31	Disk became not ready (35)
o	o	xxo	oxo	32	Invalid command: bad head (31)
o	o	xxo	oxx	33	Invalid command: bad sector (32)
o	o	xxo	xoo	34	Invalid command: bad cylinder (33)
o	o	xxo	xox	35	Invalid hard disk command issued (34)
o	o	xxo	xxo	36	Disk drive not ready (35)
o	o	xxo	xxx	37	Hard disk fault during I/O (36)
o	o	xxx	ooo	38	Data late (37)
o	o	xxx	oox	39	Data CRC (38)
o	o	xxx	oxo	3A	ID CRC (39)
o	o	xxx	oxx	3B	Halt during execution (3A)
o	o	xxx	xoo	3C	Sector not found (3B)
o	o	xxx	xox	3D	Abnormal termination of command (3C)
o	o	xxx	xxo	3E	Memory address error (80)
o	o	xxx	xxx	3F	Successful boot (FF)

Cluster Bootstrap ROM Error Code Quick Reference List

The common ROM error codes listed after each error code description can be used to look up a full description of the error in the common ROM error code descriptions at the beginning of this section.

Keyboard LEDs					
O	L	123	890	Code	Description (Common ROM Error Code)
o	o	ooo	ooo	00	(unused) (00)
o	o	ooo	oox	01	No floppy disk controller (02)
o	o	ooo	oxo	02	FDC did not become ready (03)
o	o	ooo	oxx	03	Data-in bit set in command (04)
o	o	ooo	xoo	04	Data-in bit not set in result (05)
o	o	ooo	xox	05	DMA not completed (06)
o	o	ooo	xxo	06	Volume home block checksum error (07)
o	o	ooo	xxx	07	No file on floppy disk (08)
o	o	oox	ooo	08	Run file invalid (09, 0A)
o	o	oox	oox	09	Starting seek (01)
o	o	oox	oxo	0A	Floppy disk drive became not ready during a seek (0C)
o	o	oox	oxx	0B	Invalid floppy disk command received (0D)
o	o	oox	xoo	0C	Floppy disk drive not ready (0E)
o	o	oox	xox	0D	Floppy disk drive fault during seek/recalibrate (0F)
o	o	oox	xxo	0E	Abnormal termination of seek (10)
o	o	oox	xxx	0F	Starting data transfer (01)
o	o	oxo	ooo	10	Floppy disk drive became not ready (11)
o	o	oxo	oox	11	Invalid floppy disk command received (12)

Keyboard LEDs					
O	L	123	890	Code	Description
o	o	oxo	oxo	12	Floppy disk fault during data transfer (14)
o	o	oxo	oxx	13	Floppy disk fault during data transfer (14)
o	o	oxo	xoo	14	End of cylinder (15)
o	o	oxo	xox	15	Data error: data field (16)
o	o	oxo	xxo	16	Data error: ID field (17)
o	o	oxo	xxx	17	Data late (18)
o	o	oxx	ooo	18	No data: wrong cylinder (19)
o	o	oxx	oox	19	No data: bad cylinder (20)
o	o	oxx	oxo	1A	No data (1B)
o	o	oxx	oxx	1B	Floppy disk is write protected (1C)
o	o	oxx	xoo	1C	Missing address mark: data field (1D)
o	o	oxx	xox	1D	Missing address mark: ID field (1E)
o	o	oxx	xxo	1E	Abnormal termination of command (1F)
o	o	oxx	xxx	1F	ROM checksum error (20)
o	o	xoo	ooo	20	Memory read/write error (60)
o	o	xoo	oox	21	DMA error (BA)
o	o	xoo	oxo	22	Waiting for poll (A1)
o	o	xoo	oxx	23	Never polled (A2)
o	o	xoo	xoo	24	SIO error (A3)
o	o	xoo	xox	25	8253 error (A4)
o	o	xoo	xxo	26	Writing SIM (A1)
o	o	xoo	xxx	27	No SIM (A5)
o	o	xox	ooo	28	No UP in initialization (A6, A7, A8)
o	o	xox	oox	29	Writing UA (A1)

Keyboard LEDs					
O	L	123	890	Code	Description
o	o	xox	oxo	2A	Writing dump (A1)
o	o	xox	oxx	2B	Waiting for UA (A1)
o	o	xox	xoo	2C	Bad address (dump routine) (AC)
o	o	xox	xox	2D	Disconnected (dump routine) (AD)
o	o	xox	xxo	2E	No UP (dump routine) (AE, AF, B0)
o	o	xox	xxx	2F	Dump successful (A1)
o	o	xxo	ooo	30	Reading bootblock (A1)
o	o	xxo	oox	31	Reading ACK (A1)
o	o	xxo	oxo	32	Read UI error (B1)
o	o	xxo	oxx	33	Read SNRM error (B2)
o	o	xxo	xoo	34	Disconnected (B3)
o	o	xxo	xox	35	Bad checksum of system image (B4)
o	o	xxo	xxo	36	Read error (B5)
o	o	xxo	xxx	37	Read timeout (B6)
o	o	xxx	ooo	38	Write DMA count bad (B7)
o	o	xxx	oox	39	Write timeout (B8)
o	o	xxx	oxo	3A	Bad bootblock format (B9)
o	o	xxx	oxx	3B	(unused)
o	o	xxx	xoo	3C	(unused)
o	o	xxx	xox	3D	(unused)
o	o	xxx	xxo	3E	Memory address error (80)
o	o	xxx	xxx	3F	Successful boot (FF)