IWS Peripherals Hardware

SMD Version

Convergent Technologies

IWS PERIPHERALS HARDWARE MANUAL (SMD VERSION)

Specifications Subject to Change.

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GUIDE TO TECHNICAL DOCUMENTATION

This manual is one of a set that documents the Convergent™ Family of Information Processing Systems. The set can be grouped as follows:

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This section outlines the contents of these manuals.

Introductory

The Installation Guide describes the procedure for unpacking, cabling, and powering up a system.

The Operator's Guide addresses the needs of the average user for operating instructions. It describes the workstation switches and controls, keyboard function, and floppy disk handling.

The Executive Manual describes the command interpreter, the program that first interacts with the user when the system is turned on. It specifies commands for managing files and invoking other programs such as the Editor and the programming language compilers.

Hardware

The Workstation Hardware Manual describes the mainframe, keyboard, and video display for the IWS family of workstations. It specifies system architecture, printed circuit boards (Motherboard, Processor, I/O-Memory, Video Control, Graphics Control Board, ROM and RAM Expansions), keyboard, video monitor, Multibus interface, communications interfaces, power supply, and environmental characteristics of the workstation.

The Peripherals Hardware Manual describes the non-SMD single-board Mass Storage Subsystem (MSS) and Mass Storage Expansion (MSX) disk subsystems for the IWS family of workstations. It contains descriptions of the disk controller Motherboard, the two controller boards for floppy and Winchester disks, power supplies, disk drives, and environmental characteristics.

The IWS Peripherals Hardware Manual (SMD Version) describes the SMD MSS and MSX disk subsystems having one controller board.

The AWS-210 Hardware Manual describes the mainframe, keyboard, and video display of the AWS-210 workstation. It specifies architecture, theory of operation of the printed circuit boards (Motherboard, Deflection, and CPU), keyboard, video monitor, expansion interface, cluster communications interface, power supply, and environmental characteristics of the workstation.

The AWS-220, -230, -240 Hardware Manual describes the mainframe, keyboard, disk controllers, and video display of the AWS-220, -230, and -240 workstations. It specifies architecture, theory of operation of the printed circuit boards (Motherboard, Deflection, 8088 CPU, 8086 CPU, Floppy Disk Controller, and Hard Disk Controller), keyboard, video monitor, cluster communications interface, external interfaces, power supply, and environmental characteristics of the workstation.

The AWS Color Workstation Hardware Manual describes the mainframe, keyboard, and color video display of the AWS Color Workstation. This manual reports the architecture and theory of operation of the printed circuit boards (Motherboard, Graphics Control Board, Hard Disk Controller, Color Video, Color Deflection, and CPU), keyboard, color monitor, peripheral interfaces, cluster communications interface, power supply, and environmental characteristics of the workstation. This manual also contains four OEM disk drive manuals and a summary of adjustments for the color monitor.

Operating System

The CTOS™ Operating System Manual describes the Operating System. It specifies services for

managing processes, messages, memory, exchanges, tasks, video, disk, keyboard, printer, timer, communications, and files. In particular, it specifies the standard file access methods: SAM, the sequential access method; RSAM, the record sequential access method; and DAM, the direct access method.

The System Programmer's Guide addresses the needs of the system programmer or system manager for detailed information on Operating System structure and system operation. It describes (1) cluster architecture and operation, (2) procedures for building a customized Operating System, and (3) diagnostics.

The System Utilities Manual describes utilities such as Backup Volume, IVolume, Restore, Change Volume Name, PLog, Maintain File, Dump.

The Batch Manual describes the batch manager, which executes batch jobs under control of job control language (JCL) files.

Programming Languages

The COBOL, FORTRAN, FORTRAN-86, BASIC (Interpreter), BASIC Compiler, PASCAL, and Assembly Language Manuals describe the system's programming languages. Each manual specifies both the language itself and also operating instructions for that language.

The Pascal Manual is supplemented by a popular text, Pascal User Manual and Report.

The Assembly Language Manual is supplemented by a text, the Central Processing Unit, which describes the main processor, the 8086. It specifies the machine architecture, instruction set, and programming at the symbolic instruction level.

Program Development Tools

The COBOL Animator describes the COBOL Animator, a debugger that allows the user to interact directly with the COBOL source code during program execution.

The Editor Manual describes the text editor.

The Debugger Manual describes the Debugger, which is designed for use at the symbolic instruction level. Together with appropriate interlistings, it can be used for debugging FORTRAN, Pascal, and assembly language programs. (COBOL and BASIC, in contrast, are more conveniently debugged using special facilities described in their respective manuals.)

The Linker/Librarian Manual describes the Linker, which links together separately compiled object files, and the Librarian, which builds and manages libraries of object modules.

Data Management Facilities

The CT-DBMS Manual describes Convergent's data base management system (CT-DBMS), which consists of (1) a data manipulation language for accessing and manipulating the data base and (2) utilities for administering the data base activities such as maintenance, backup and recovery, and status reporting.

The ISAM Manual describes both the single- and the multiuser indexed sequential access method. It specifies the procedural interfaces (and how to call them from various languages) and the utilities.

The Forms Manual describes the Forms facility that includes (1) the Forms Editor, which is used to interactively design and edit forms, and (2) the Forms run time, which is called from an application program to display forms and accept user input.

The Sort/Merge Manual describes (1) the Sort and Merge utilities that run as a subsystem invoked at the Executive command level, and (2) the Sort/Merge object modules that can be called from an application program.

Text Management Facilities

The Word Processing User's Guide introduces the Word Processor to the first-time user. It provides step-by-step lessons that describe basic word processing operations. The lessons show how to execute operations and apply them to sample text.

The Word Processing Reference Manual is a reference tool for users already familiar with the Word Processor. It describes the Word Processor keyboard and screen; basic, advanced, and programmer-specific operations; list processing; printer and print wheel configurations; and hardware considerations.

The Word Processing Quick Reference provides a concise summary of all word processing operations and briefly describes the keyboard and commands.

Applications Facilities

Multiplan is a financial modeling package designed for business planning, analysis, budgeting, and forecasting.

The Business Graphics User's Guide introduces Business Graphics to the first-time user. It provides step-by-step lessons that describe basic Business Graphics operations. The lessons show how to execute operations and apply them to sample charts.

The Business Graphics Reference Manual is a reference tool for users already familiar with Business Graphics. It describes the Business Graphics keyboard and screen; box and arrow cursor movement; obtaining information from Multiplan; operations; and plotter configurations.

The Graphics Programmer's Guide is a reference for applications and systems programmers. It describes the graphics library procedures that can be called from application systems to generate graphic representations of data, and it includes a section on accessing Business Graphics from an application system.

The Font Designer Manual describes the interactive utility for designing new fonts (character sets) for the video display.

Communications

The Asynchronous Terminal Emulator Manual describes the asynchronous terminal emulator.

The 3270 Terminal Emulator Manual describes the 3270 emulator package.

The 2780/3780 RJE Terminal Emulator Manual describes the 2780/3780 emulator package.

The SNA Network Gateway Manual describes the SNA Network Gateway, which supports data communications over an SNA network. The SNA Network Gateway comprises the Transport Service and Status Monitor. The Transport Service allows a Convergent workstation to function as cluster controller and forms the foundation for Convergent SNA products.

The SNA 3270 Emulator Manual describes the SNA 3270 emulator package. The SNA 3270 emulator provides CRT and printer subsystems in addition to a Virtual Terminal Interface for use in application programs.

The X.25 Network Gateway Manual describes the X.25 Network Gateway, which supports CCITT Recommendation X.25 communications over a public data network. There are three levels of access to the network: packet, X.25 sequential access method, and the Multimode Terminal Emulator X.25 communications option.

The Multimode Terminal Emulator User's Guide introduces the Multimode Terminal Emulator to the first-time user. It describes the MTE video display, keyboard, display memory, and advanced operations for the X.25 communications option.

The Multimode Terminal Emulator Reference Manual is a reference tool for sophisticated users of the Multimode Terminal Emulator. It describes the MTE escape sequences and field verification program.

CONVENTIONS, REFERENCES, AND ABBREVIATIONS

Conventions

Numbers

All numbering of bits in a word, bits on a bus line, and input/output port addresses is done in hexadecimal notation. For example, the 20 bits in an address are numbered from 0 (least significant bit) to 13h (most significant bit). The signal lines on 16-bit data buses are numbered from 0 to Fh.

Signal Names

Signal names use plus (+) and minus (-) suffixes to distinguish active-high from active-low signals, respectively. For example:

Signal Name	Logical State	Voltage Level
RD-	0 (active)	Low
	1 (inactive)	High
RD+	0 (inactive)	Low
	1 (active)	High

The convention used here corresponds to the Multibus convention as follows:

CT Convention	Multibus Convention
RD-	RD/RD*
RD+	RD RD

In all other respects, the Convergent Technologies convention is the same as the Multibus convention.

References

The IWS Storage Module Drive (SMD) Controller board is heavily dependent upon programmable large scale integrated (LSI) circuits to perform its functions. Since the hardware functions and software interfaces of such circuits are only

briefly detailed in this manual, the reader may want to occasionally refer to the following source literature:

- Signetics 8X300 Reference Manual, Signetics Corporation
- 8X300 Design Guide, Signetics Corporation
- 8X330 Floppy Disk Controller Reference Manual, Signetics Corporation
- ANSII X3.66, American National Standards Institute, Incorporated

Several new terms are introduced in this manual. Generally, they are explained when first used, but the Glossary at the end of the manual contains explanations of terms that may be unfamiliar. Also at the end of this manual, in Appendix E, is the Signals Glossary, which gives the names of signals used on this board and explains their use. Schematic diagrams, as referenced in text, are included within this document.

Abbreviations

Following is a list of standard abbreviations used in Convergent Technologies manuals:

Unit or Term	Symbol or Abbreviation
alternating current	ac
amp	A
amplitude modulation	AM
average	avg
binary coded decimal	BCD
centimeter	cm
cyclic redundancy checking	CRC

Unit or Term	Symbol or Abbreviation
disk controller interface	DCI
degree Celcius	°C
degree Fahrenheit	°F
degree (temperature interval or difference)	deg
direct current	dc
data communications equipment	DCE
data terminal equipment	DTE
error control circuitry	ECC
farad	F
foot	ft
frequency modulation	FM
gigahertz	GHz
henry	H
hertz (cycles per second)	Hz
inch	in
inch per second	in/sec
inductance	L
inductance-capacitance	LC
input/output	I/O
kilobaud	kbaud
kilobyte	K, K byte
kilogram	kgram
kilohertz	kHz

Unit or Term	Symbol or Abbreviation
kilovolt	kV
light-emitting diode	LED
megabyte	M, M byte
meter	m
modified frequency modulation	MFM
Mass Storage Subsystem	MSS
Mass Storage Expansion	MSX
nanosecond	nsec
phase-locked loop	PLL
pound	lb
resistance-capacitance	RC
resistance-inductance-capacitance	RLC
revolutions per minute	RPM
second (time)	sec
Storage Module Drive	SMD
volt	V
voltage controller oscillator	VCO
voltage root mean square	Vrms
watt	W

OVERVIEW

This manual describes the IWS Workstation Mass Storage Subsystem (MSS) and the Mass Storage Expansion (MSX) memory expansion peripherals. It also describes the interface between the IWS workstation and its other peripherals, including printers and plotters. Figure 1-1 shows the IWS and its peripheral components.

Section 2 of this manual, "Mass Storage Subsystem," contains a description of the MSS, including its boards and power supplies. In particular, Section 2 describes the Storage Module Drive (SMD) Controller board, a single controller board, which replaces the Floppy Disk Controller and Hard Disk Controller boards found in the non-SMD version of the MSS.

Section 3, "Mass Storage Expansion," contains a description of the components and operation of the MSX.

Section 4 of this manual, "Additional Peripherals Hardware," contains instructions for the construction and assembly of cables needed to connect additional hardware to the IWS workstation. It also contains directions for setting up some of the printers and plotters supported by the IWS workstation, or attaching an IWS workstation to a cluster network.

Appendix A contains a list of MSS/MSX specifications. Appendix B contains specifications and information on Storage Module Drives. Appendix C contains connector pin lists; Appendix D contains a description of switch settings for the SW1 memory configuration switch on the SMD Controller board; and Appendix E contains a glossary of signals.

The IWS Peripherals Hardware Manual (SMD Version) is for the OEM engineer who writes service or installation manuals for IWS Peripherals hardware, or who tests or services IWS system electronics. This manual is also for the engineer who modifies system software for use with IWS peripherals. It is not intended, however, as documentation for production-level testing, nor does it support hardware modifications. Convergent Technologies does not support modi-

fications to its boards other than those predetermined by design, such as jumper options.

For more information on Convergent Technologies software support of hardware peripherals, consult the reference manual for each specific application, such as word processing or business graphics.

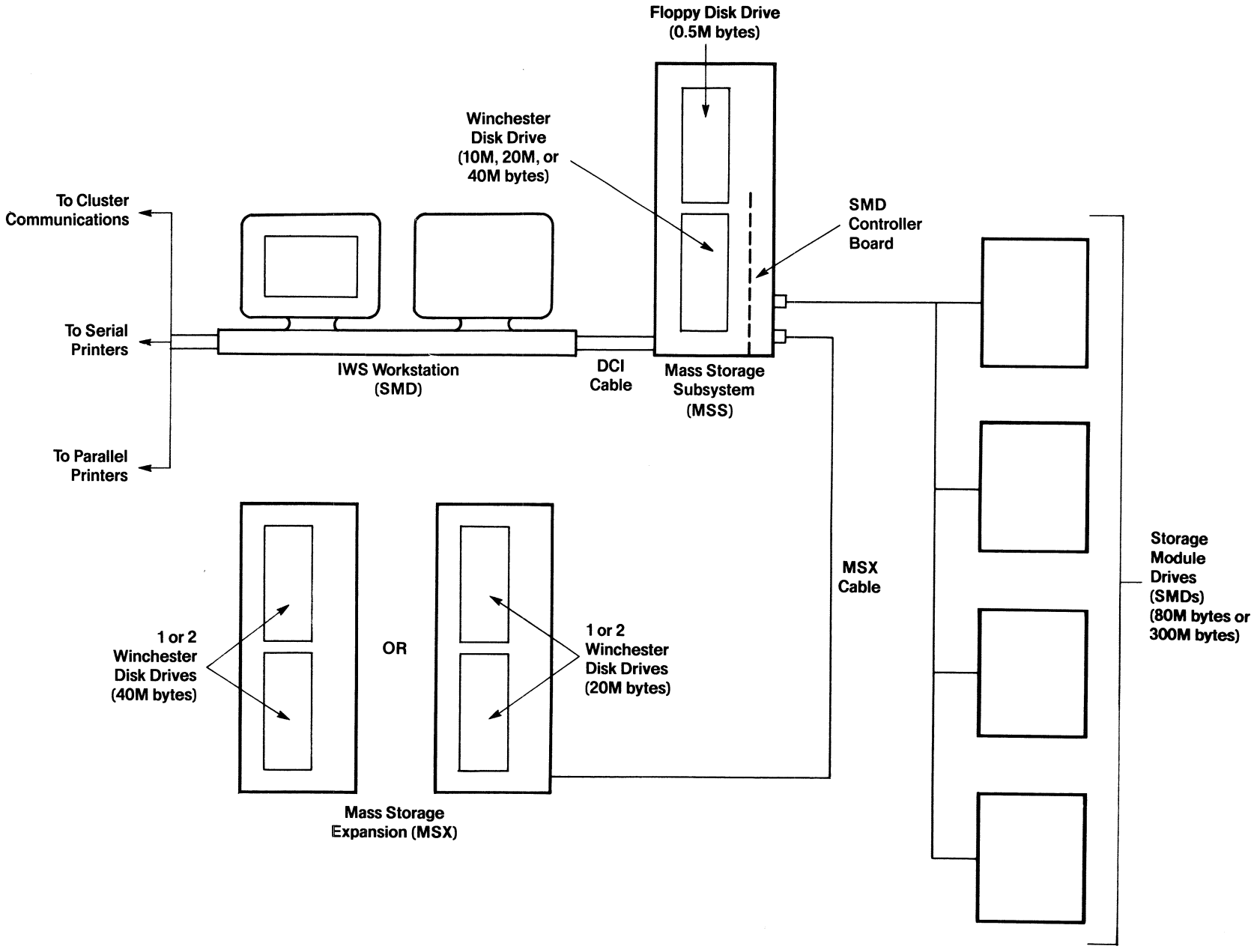


Figure 1-1. IWS Peripherals Hardware.

2 MASS STORAGE SUBSYSTEM

INTRODUCTION

The Mass Storage Subsystem (MSS) contains two disk drives, a Storage Module Drive (SMD) Controller board, an SMD I/O Extender board, a motherboard, and a power supply. Commands from the IWS workstation enter the MSS at the SMD I/O Extender board, and are sent to the SMD Controller board through the motherboard. The SMD Controller board outputs data and control signals, which are sent to a floppy disk and Winchester disk drive in the MSS, SMDs connected to the MSS, and two Winchester disk drives located in the Mass Storage Expansion (MSX) peripheral. Up to four SMDs can be connected to the MSS through the SMD I/O Extender board. Figure 2-1 shows the functional blocks of the MSS.

The MSS accommodates an 8-inch floppy disk, and an 8-inch Winchester hard disk drive, which can be either 10M-, 20M-, or 40M-byte capacity. SMDs connected to the MSS can be either 80M- or 300M-byte capacity, and the Winchester disk drives in the MSX can be either 20M- or 40M-byte capacity.

Disk drive capacity is determined by switch SW1, located on the SMD Controller board. For more information on switch settings, refer to Appendix D, "SMD Controller Board Memory Configuration Switch Settings."

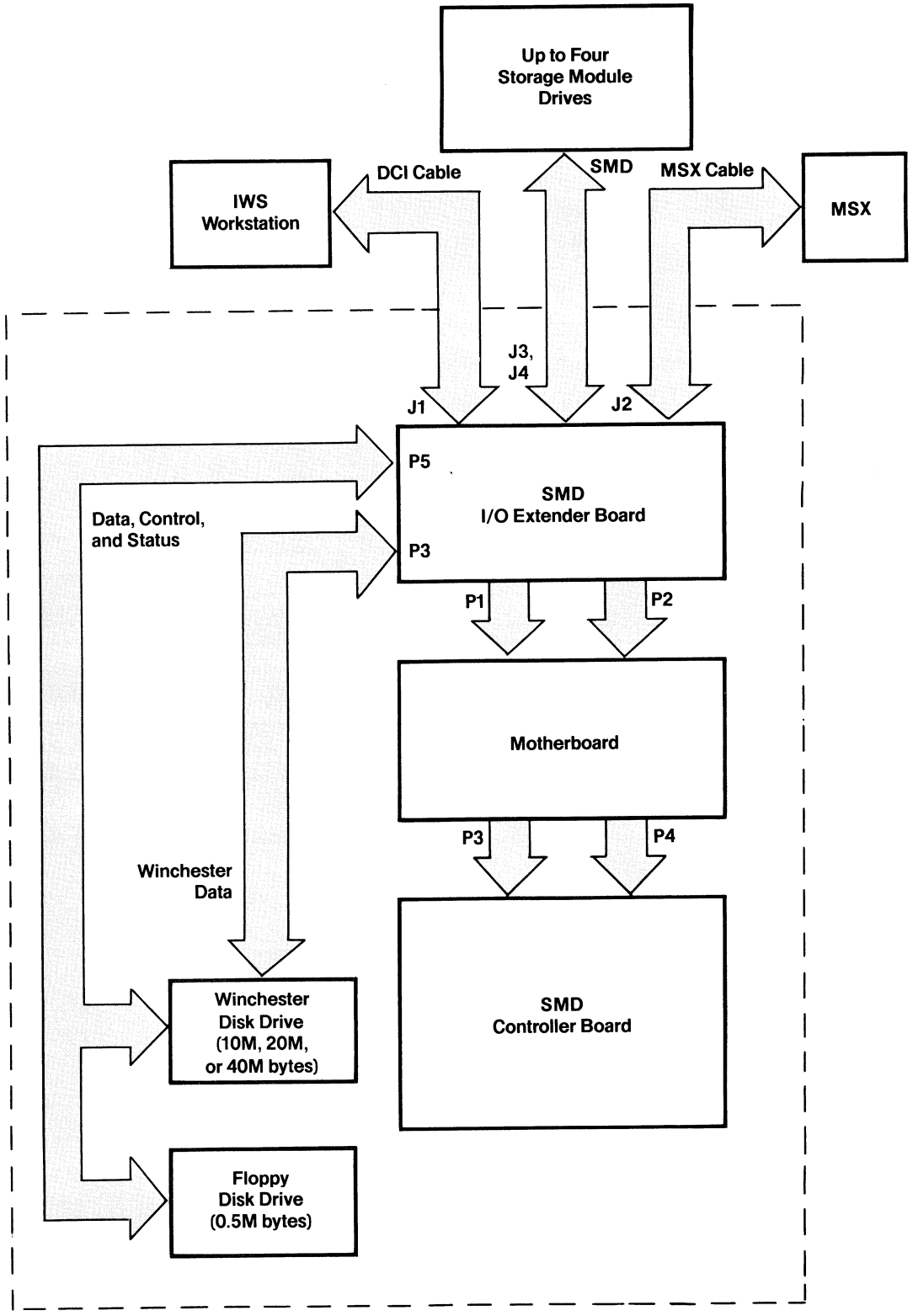


Figure 2-1. Mass Storage Subsystem Block Diagram.

SMD CONTROLLER BOARD

The SMD Controller board controls all disk-related functions for the IWS. Disk drive configuration is selected by switch SW1 on the controller board. An internally used controller logical unit designation of drive 0 (000), as shown in Table 2-1, refers to an 8-inch single-sided floppy disk drive with 77 tracks per inch, located in the MSS as drive 0. Designations D1, D2, and D6 refer to Winchester hard disk drives, located in the MSS and MSX chassis.

For more information on SW1, see Appendix D, "SMD Controller Board Memory Configuration Switch Settings."

Table 2-1. SMD Controller Device Names.

Controller Logical Unit	Unit/Drive Type	Physical Drive Select
0 (000)	MSS/floppy unit 3*	DS4
1 (001)	MSX/Winchester unit 2	DS3
2 (010)	MSS/Winchester unit 0*	DS1
3 (011)	SMD unit 3	SMD3
4 (100)	SMD unit 0*	SMD0
5 (101)	SMD unit 1	SMD1
6 (110)	MSX/Winchester unit 1*	DS2
7 (111)	SMD unit 2	SMD2

*Only even numbered logical units can be bootstrapped.

The SMD Controller board is based on a Signetics 8X300 microcontroller, operating from a micro-program stored in 12K bytes of ROM (Read Only Memory). The 8X300 fetches instructions from ROM with its address and instruction buses, and communicates with external devices through the 8-bit IV (interface vector) bus.

The IV bus accommodates separate right and left banks of input/output devices. Located on the left bank of the IV bus are two 1K-byte buffers, used for local disk storage and disk data buffering. All other disk controller input/output ports are located on the right bank of the IV bus. The architecture of the 8X300 allows it to

receive data on one bank, process the data, and then deposit the data on either bank, all in one machine cycle of 250 nsec. Since the 8X300 fetches ROMs with separate address and instruction lines, it can fetch the next instruction while, at the same time, processing data on the IV bus.

An 8X320 16-bit bus interface register array (BUS0+ through BUSF+) is the interface between the IV bus and the IWS workstation data bus. The 8X320 has 16 eight-bit registers that contain disk data, and command or status information. DMA (Direct Memory Access) Channel 2 in the IWS workstation is used to control data transfers for disk read and write operations, while an interrupt-controlled mode is used for status commands and ready/not-ready status changes.

SMD CONTROLLER BOARD ARCHITECTURE

Command and Status Registers

The SMD Controller board has two eight-bit input/output ports, which provide access to the IWS workstation CPU. They are

Port	Write Information	Read Information
78h	Data register (command bytes)	Data register (status bytes)
7Ah	Control register	Main Status register

Main Status Register (Port 7Ah)

The Main Status register at port 7Ah is an eight-bit register that provides status on the controller logic and disk drives and can be written to or read from at any time, even during a DMA data transfer or other execution phase of a command. The Main Status register plays a central part in the IWS workstation/controller handshake protocol when port 78h is read from or written to. In particular, it must be read from before the IWS workstation attempts to read from or write to port 78h. This is done to determine if the controller logic is ready for an operation at port 78h, and whether the operation should be a read or a write. Table 2-2 shows the contents of the Main Status register.

Control Register (Port 7Ah)

The lower eight bits of port 7Ah comprise the Control register, which is written to only when the IWS workstation halts or resets the SMD Controller board logic. The contents of the Control register are shown in Table 2-3.

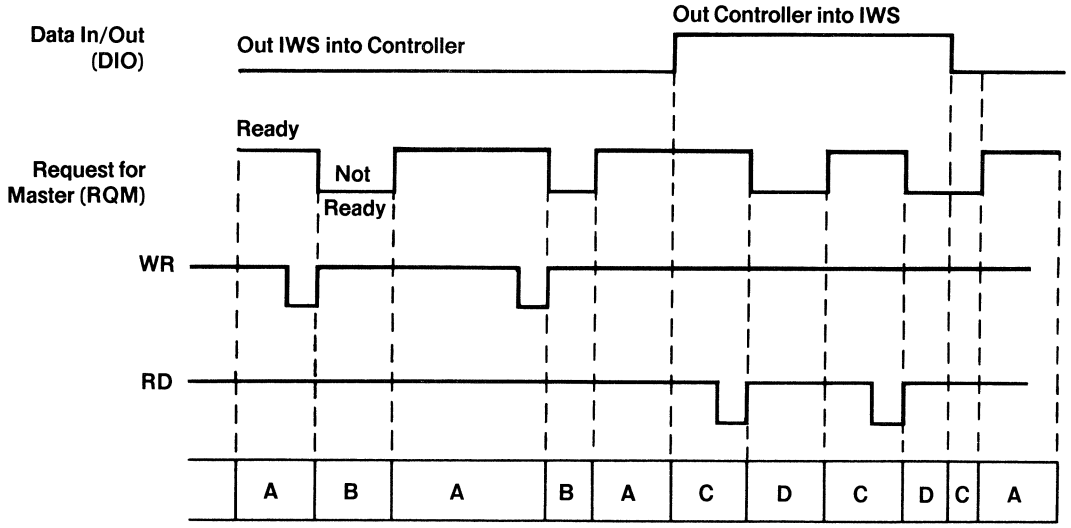
Data Register (Port 78h)

Port 78h is an eight-bit register to which all control and status bytes associated with a specific command function are written and read. Port 78h is only written to before the execution of a command (such as a Data Transfer or Recalibrate), and it is only read from after a command

Table 2-2. Main Status Register (Port 7Ah).

Bit	Name	Read Function
7	Request for Master (RQM)	If RQM is 1, it indicates that data is ready to be transferred to or received from the IWS workstation. Both RQM and DIO are used by the 8X300 to perform a handshake function of ready and direction to the IWS workstation.
6	Data Input/Output (DIO)	DIO indicates the direction of Disk Controller Interface (DCI) bus transactions. If DIO is 1, then the transfer is from the data register to the IWS workstation; if DIO is 0, then the transfer is from the IWS workstation to the controller.
5	Interrupt Request (IR)	IR indicates the state of the Interrupt Request flag.
4	Controller Busy (CB)	If CB is 1, it indicates that a Read/Write command is in progress.
3-0		Unused

has been executed. Control bytes written to this port determine the functions of individual disk drives and, during a Result phase, status bytes are read at this port. Although port 78h is referred to as a Data register, it is used only for writing and reading control/status bytes. Actual data to be transferred to or from disk is handled by the IWS workstation DMA logic. Figure 2-2 illustrates the IWS workstation/controller handshake protocol used when reading or writing a byte at port 78h.



Notes: A Data register ready to be written to by the IWS.
B Data register not ready to be written to by the IWS.
C Data register ready for next data byte to be read by the IWS.
D Data register not ready for next data byte to be read by the IWS.

Figure 2-2. Handshake Protocol Used When Reading from or Writing to Port 78h.

Table 2-3. Control Register (Port 7Ah).

Bit	Name	Write Function
7	Reset	If Reset is 1, it asynchronously initiates a reset to the controller. This bit must remain set for at least 15 microseconds to ensure that the reset has been completed. It can then be cleared in a separate write to port 78h.
4	Inhibit Error Code Checking (INHECC)	When INHECC is 1, it inhibits ECC generation and detection on the SMD Controller board. When it is 0, it indicates that ECC is enabled.
5-0		Unused

Status Registers 0 Through 3 (ST0 Through ST3)

ST0 through ST3 are registers internal to the controller that provide status information to the IWS workstation after a command has been executed. (See Tables 2-4 through 2-7.) A set of these registers is maintained for each drive in the system. The contents of these registers may be read by the IWS workstation through the data port (port 78h) only after a command is executed and only if the register contains information relevant to that command. There is no separate port associated with ST0 through ST3.

Table 2-4. Status Register 0 (ST0)*:

Bit Number	Read Information (if Bit is 1)
6-7	Interrupt code. (See below for code interpretation.)
5	Seek complete
4	Drive fault
3	Drive not ready
2-0	US2 through US0 (drive select numbers). (See Table 2-1 for binary coding.)

Interrupt Code

Bit 7	Bit 6	Code Meaning
0	0	Normal command termination
0	1	Unsuccessful command termination
1	0	Invalid command
1	1	Attention interrupt

*After reset, this register is set to 00.

Table 2-5. Status Register 1 (ST1)*:

Bit Number	Read Information (if Bit is 1)
7	Invalid cylinder number
6	ID CRC (identification field cyclic redundancy check) error
5	Data CRC error
4	Data is late
3	Invalid sector number
2	Read error
1	Write-protect violation
0	Invalid head number

*After reset, this register is set to 00.

Table 2-6. Status Register 2 (ST2)*:

Bit Number	Read Information (if Bit is 1)
7	Controller read/write error
6	Data buffer error
5	Halt during command execution
4	Head compare error
3	Cylinder compare error
2	Sector not found
1	Missing identification field address mark
0	Missing data address mark

*After reset, this register is set to 00.

Table 2-7. Status Register 3 (ST3)*:

Bit Number	Read Information (if Bit is 1)
7	Drive fault
6	Write-protect error
5	Drive ready
4	Disk is at track 000
3	Unused
2-0	US2 through US0 (drive select numbers). (See Table 2-1.)

*After reset, this register is set to 00.

Command Structure

A command is the set of all bytes that must be written to or read from the SMD Controller board input/output ports in order to perform a specific function. Each command to the controller board consists of a multibyte transfer between the IWS workstation and controller via the DCI (disk controller interface) cable. Table 2-8 lists the full set of commands that can be issued to the controller logic, together with the associated number of bytes written to or read from ports 7Ah and 78h. Table 2-9 is a description of SMD Controller board commands. The actual number of bytes transferred is determined by the command.

Table 2-8. Number of Byte Transfers for SMD Controller Board Commands.

Command	Type*	Port 7Ah Write	Port 7Ah Read	Port 78h Write	Port 78h Read
Format a Track	Data	0	7	6	1
Read Data	Data	0	6	5	1
Read Syndrome Bytes	Control	0	5	1	4
Read Full Status	Control	0	7	1	6
Recalibrate**	Control	0	1	1	0
Seek**	Control	0	3	3	0
Read Drive Status	Control	0	4	1	3
Sense Interrupt Status	Control	0	4	1	3
Write Data	Data	0	6	5	1
Set Drive Parameter	Control	0	9	8	1
Read Drive Configuration	Control	0	7	1	6

* Nondata commands do not involve user-data transfers between the IWS workstation and disk drive.

**The Recalibrate and Seek commands must be followed by a Sense Interrupt Status command.

Table 2-9. SMD Controller Board Commands. (Page 1 of 7)

Read Data Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2	US1	US0	0	0	1	1	0
Byte 1	W	head						cylinder	
Byte 2	W	cylinder							
Byte 3	W	first sector							
Byte 4	W	number of sectors							
Execution									
Result	R	ST0							

The controller has an implied-seek capability, which means that no Seek command has to be issued for a command to be implemented and also that the controller will invoke the Seek command as many times as needed to complete a command. The number of sectors must be in twos complement. First sector refers to the number of the first sector to be read.

The Data bus (D7-D0) shown above is defined as follows:

	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Byte 1	head						cylinder	
	H3	H2	H1	H0	H4	C11	C10	C9

H0 is the least significant bit and H4 is the most significant bit. In cylinder, C11 is valid for Winchester and floppy type drives, but should be 0 for SMD drives.

After this command, the CPU reads ST0. If ST0 contains anything other than 00 in the interrupt code, or if there is an abnormal command termination, the CPU executes a Read Full Status command.

Table 2-9. SMD Controller Board Commands. (Page 2 of 7)

Format a Track Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2	US1	US0	0	1	1	0	1
Byte 1	W	head					cylinder		
Byte 2	W	cylinder							
Byte 3	W	offset							
Byte 4	W	spacing							
Byte 5	W	filler byte							
Execution									
Result	R	ST0							

512 bytes per sector are formatted. The filler byte specifies the contents of all 512 bytes. Offset is the gap between Index and first sector, in bytes. Spacing is the number of bytes between sectors.

Write Data Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2	US1	US0	0	0	1	0	1
Byte 1	W	head					cylinder		
Byte 2	W	cylinder							
Byte 3	W	first sector							
Byte 4	W	number of sectors							
Execution									
Result	R	ST0							

The Write Data command has an implied-seek capability, meaning that no Seek command has to be issued for a command to be implemented. The number of sectors must be a twos complement number. First sector refers to the number of the first sector to be written.

Table 2-9. SMD Controller Board Commands. (Page 3 of 7)

Read Full Status Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2*	US1*	US0*	0	0	0	1	1
Result	R	ST0							
Byte 1	R	ST1							
Byte 2	R	ST2							
Byte 3	R	ST3							
Byte 4	R	- - - head-					- -	cylinder-	-
Byte 5	R	- - - - - - - - cylinder-							

*Unit select is ignored.

Reads the full status of the previous drive that performed an input/output operation.

The status registers returned in the Result phase are a subset of the registers returned in the Read Diagnostics command. This command has no Execution phase.

Recalibrate Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2	US1	US0	0	0	1	1	1
Execution									
Result		(execute Sense Interrupt Status command)							

This command positions the heads over TRK0 (track zero).

Table 2-9. SMD Controller Board Commands. (Page 4 of 7)

Seek Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2	US1	US0	0	1	1	1	1
Byte 1	W	|- - - - - - head- - - - - - - -|						- - cylinder- - -|	
Byte 2	W	|- - - - - - cylinder- - - - - - - - - - - - - - -|							

Execution

Result (execute Sense Interrupt Status command)

This command causes a seek to the specified cylinder and head.

Read Syndrome Byte Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2	US1	US0	0	0	0	1	0
Result									
Byte 0	R	|- - - - - - - -Syndrome Byte 1- - - - - - - - -|							
Byte 1	R	|- - - - - - - -Syndrome Byte 2- - - - - - - - -|							
Byte 2	R	|- - - - - - - -Syndrome Byte 3- - - - - - - - -|							
Byte 3	R	|- - - - - - - -Syndrome Byte 6 - - - - - - - - |							

This command reads the syndrome bytes of the data that was last read. Data from these syndrome bytes is used for external data correction in case of a data CRC error. This command is invalid for floppy disk drives.

Table 2-9. SMD Controller Board Commands. (Page 5 of 7)

Sense Interrupt Status Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2	US1	US0	0	1	0	0	0
Result									
Byte 1	R	|- - - - - - - ST0 - - - - - - - - - - - - - - - -|							
Byte 2	R	|- - head- - - - - - - - - - -|- - cylinder- -|							
Byte 3	R	|- - - - cylinder- - - - - - - - - - - - - - - -|							

The interrupt request is cleared immediately after byte 1 is read.

Read Drive Status Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2	US1	US0	0	0	1	0	0
Execution									
Result									
Byte 1	R	|- - - - - - - - - - ST3 - - - - - - - - - - - |							
Byte 2	R	|- - - - - - head - - - - - - -|- - cylinder- -|							
Byte 3	R	|- - - - - - - - - -cylinder - - - - - - - - - |							

Table 2-9. SMD Controller Board Commands. (Page 6 of 7)

Set Drive Parameters Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2	US1	US0	1	0	0	0	0
Byte 1	W	|- - - - - - - -maximum head - - - - - - - - - |							
Byte 2	W	|- - - - - - maximum cylinder (MSB)*- - - - - -|							
Byte 3	W	|- - - - - - maximum cylinder (LSB)* - - - - - |							
Byte 4	W	|- - - - reserved- - - - - |-ECC- |- -MF - |							
Byte 5	W	| - - - - - - - - - - -N - - - - - - - - - - - - |							
Byte 6	W	|- - - - - - - - - - -DTL - - - - - - - - - - - -|							
Byte 7	W	|- - (SC) # of sectors per cylinder- - - - |							

*MSB is the most significant byte;
LSB is the least significant byte.

If MF (bits 0 and 1 of byte 4) equals 00, then FM recording mode is selected. If MF equals 01, then MFM recording mode is selected.

If ECC (error code checking) at bit 2 of byte 4 equals 0, then ECC bytes are checked; if ECC equals 1, ECC bytes are ignored.

When the number of data bytes written in a sector (N) is defined as 00, DTL stands for the data length that users will read out or write into the sector.

After a Reset sequence, these parameters default to the following values for a floppy drive:

MF = 01
N = 02
DTL = 00
SC = OF

SC refers to the number of sectors for cylinder. For Winchester drives, its value is 16; for SMD drives the SC is 32.

MF, N, and DTL have no meaning for SMD and Winchester drives.

Table 2-9. SMD Controller Board Commands. (Page 7 of 7)

Read Drive Configuration Command

Phase	Read/ Write	Data Bus D7	D6	D5	D4	D3	D2	D1	D0
Command	W	US2	US1	US0	0	1	1	0	0
Byte 1	R	|-controller ID#-			|-firmware revision lev.-|				
Byte 2	R	|- - - - -number of cylinders (LSB)* - - - |							
Byte 3	R	|- - - - -number of cylinders (MSB)* - - - |							
Byte 4	R	|- - - number of heads per cylinder- - - - |							
Byte 5	R	|- - - -number of sectors per track- - - - |							
Byte 6	R	|drive type |- - - |-# of drives supported-|							

*MSB is the most significant byte;
LSB is the least significant byte.

If the controller identification number (controller ID#) equals 0001, the firmware revision level is from 0001 to 1111.

If a Shugart 10M-byte, 256-cylinder drive is selected, the least significant byte will equal 0, and the most significant byte will equal 1.

If a Quantum 20M-byte, 512-cylinder drive is selected, the least significant byte will equal 0, and the most significant byte will equal 2.

If a Fujitsu 589 cylinder SMD is selected, the least significant byte will equal 00, and the most significant byte will equal 02.

If bits 7 and 6 of byte 6 equal 00, then the drive is floppy.

If bits 7 and 6 of byte 6 equal 01, then the drive is Winchester.

If bits 7 and 6 of byte 6 equal 10, then the drive is SMD.

Input/Output Transfer Routines

When the SMD Controller board receives the required number of bytes for a command from the IWS workstation, the command is executed. This input/output transfer routine, shown in Figure 2-3, is described as three phases in the following subsections: the Command phase, the Execution phase, and the Result phase.

Command Phase

In the Command phase, all of the required bytes are written to port 78h. Although port 7Ah does not have to be written to before port 78h, whenever port 78h is written to, the handshake with port 7Ah is used. Once a command sequence is initiated, all byte transfers must be completed before the Execution phase can occur.

Execution Phase

This is the functional execution of the command. A Read Data (RDDATA) command, for example, is executed when DMA transfers from controller to IWS workstation occur. During this time, the Controller Busy (CB) bit in the Main Status register indicates that port 78h is busy. The following commands do not have an Execution phase that involves disk-drive activity: Read Syndrome Bytes, Read Disk Configuration, Set Drive Parameters, Read Drive Status, and Sense Interrupt Status. (For more information on these commands, see the "Control Operations" subsection, below).

Result Phase

This phase usually begins with an interrupt of the IWS workstation after a command has been executed, and usually involves reading one or more status bytes from port 78h. Commands with no Execution phase, however, have no interrupt or other clear boundary between their Command and Result phases. The IWS workstation must read all status bytes to remove the interrupt condition, and must also use the Main Status register handshake protocol. The Recalibrate and Seek commands have no associated status bytes, but they must be followed by the Sense Interrupt

Status command. For more information on commands with no Execution phase, see the "Control Operations" subsection, below. A Seek command operation is described following the "Control Operations" subsection.

Data Input/Output Transfer Protocol

The general data input/output transfer routine, illustrated in Figure 2-3, follows:

1. When the IWS workstation wants to issue a command to the controller, it checks the Main Status register to verify that the RQM (Request for Master) bit is high and the DIO (Data Input/Output) bit is low.

2. If they are, the IWS workstation checks that the CB (Controller-Busy) and IF (Interrupt Flag) bits are low.

3. The IWS workstation then issues a command byte to the controller's data port (78h). The format of this command is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
US2	US1	US0	|---------operating code----------|				

Bits US0 through US2 are the device select code.

4. After issuing the command byte, the IWS workstation again reads port 7Ah for RQM and DIO bits (referred to as parameters in Figure 2-3).

5. If no error has occurred, the IWS workstation then outputs from zero to eight additional bytes to port 78h, depending on the command. The number of additional bytes transmitted depends on the opcode field of the first byte. Once the command sequence is initiated, all byte transfers must be completed before the controller can enter the Execution phase.

6. When the command has finished execution, the controller enters the Result phase. In the Result phase, the IWS workstation must read ST0 from the data port. For the data transfer, the controller enables RQM, DIO,

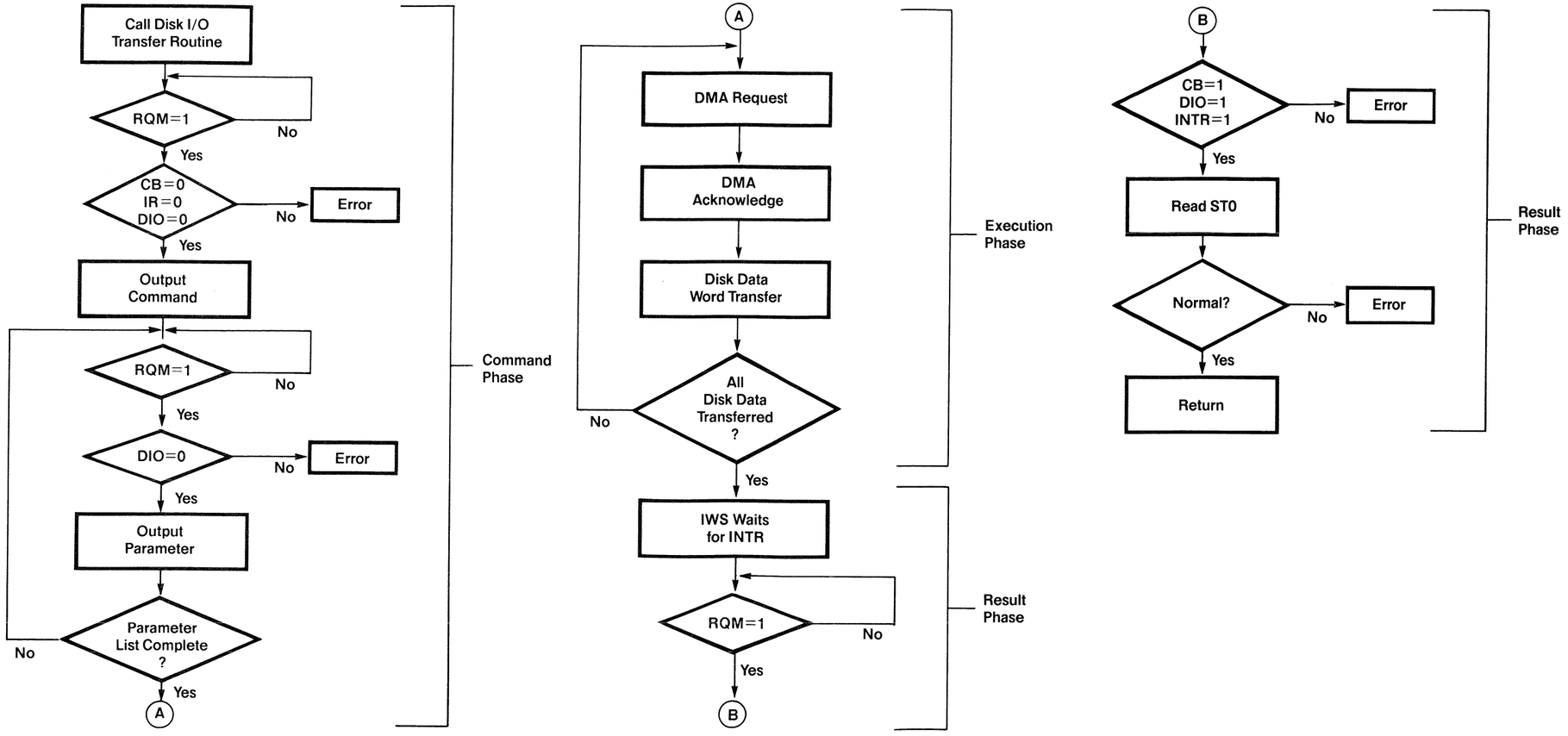


Figure 2-3. Data Input/Output Transfer Routine.

IR (Interrupt Request) and CB bits. When it receives an Interrupt Request signal from the controller, the IWS workstation reads port 7Ah and checks the CB, RQM, and DIO bits. When it detects an enabled CB bit, the IWS workstation reads ST0 from port 78h to determine the cause of the interrupt. Interrupt Request is disabled when the control status has been read. For a status data transfer, the Result phase is indicated by an asserted INTR and deasserted CB bit in the Main Status register. If the IWS workstation does not detect an asserted CB bit, it sends a Sense Interrupt Status command to determine the cause of interrupt from the status bytes read during the Sense Interrupt Status command's Result phase. When the required number of status bytes have been read, the controller can enter the next Command phase.

Read or Write Operation (Execution Phase)

1. The IWS workstation sends a write or read command (seven bytes) to the controller through port 78h. After writing each command byte, the IWS workstation reads the controller's Main Status register at port 7Ah to determine when the controller can accept another byte.

2. When the Main Status register indicates that the Controller Data register at port 78h is full, the read or write operation begins when the controller sends a DREQ- (DMA Request) signal to the IWS workstation.

3. The IWS workstation acknowledges the DMA Request by enabling ACK- (Acknowledge). The DMA control logic then requests the address and data buses, generates the appropriate command strobes (RDSTR-, BMR-), and transfers data as a DMA transfer. For a write operation, WRSTR- (Write Strobe) is asserted and data is transferred from the IWS workstation to the SMD Controller board buffer, and then into a selected disk drive's memory. For a read operation, data is transferred from a selected disk drive to the SMD Controller board buffer, and is then read by the IWS workstation. Fourteen bytes are transferred for every DMA request.

4. When the data transfer is complete, the controller generates an interrupt signal to the IWS workstation.

5. The IWS workstation then reads the data register at port 78h to determine success of the operation.

Nondata Input/Output Transfer Protocol

Control operations (Read Syndrome Bytes, Read Configuration, Set Drive, and Parameter) do not use DMA, since no data is being transferred. Such control operations, as mentioned, consist of only two phases, the Command phase, and the Result phase, and interrupt the IWS workstation when a command is completed. A typical nondata input/output transfer routine is shown in Figure 2-4 and a Seek command is described below, in the "Control Operation" subsection.

1. The IWS workstation sends a control command to the controller through port 78h. After writing each command byte, the IWS workstation reads the controller's Main Status register at port 7Ah to determine when the controller can accept another byte.

2. When the last command byte is written to the Controller Data register at 78h, the IWS workstation waits for an interrupt. After the interrupt is received, the IWS workstation reads port 7Ah, checks that the RQM and DIO bits are set, and then reads status bytes from the Data register until all bytes are read.

Control Operation (Seek Command)

1. The IWS workstation reads port 7Ah for a high RQM signal.

2. The IWS workstation then sends a Seek command (three bytes) to the controller through port 78h. After writing each command byte, the IWS workstation reads the controller's Main Status register at port 7Ah to determine when the controller can accept another byte.

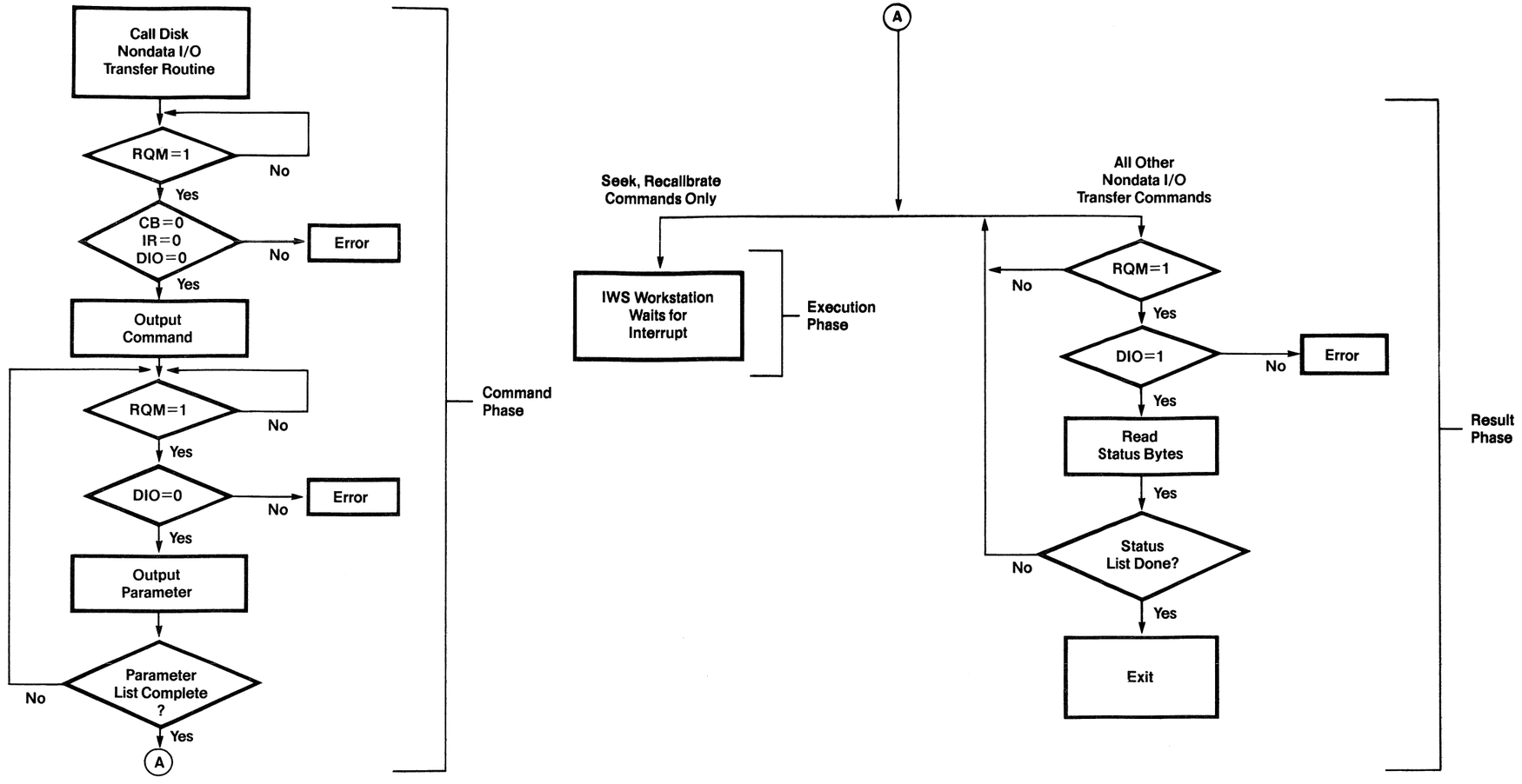


Figure 2-4. Nondata Input/Output Transfer Routine.

4. When the operation is complete, the controller interrupts the IWS workstation by lowering INT-.

5. The IWS workstation then issues a Sense Interrupt Status command to acquire status from the Data register at port 78h. The IWS workstation reads three status bytes to determine the outcome of the command execution.

SMD CONTROLLER BOARD THEORY OF OPERATION

This section is for the engineer or technician who must understand the Storage Module Drive (SMD) Controller board at the component level. The SMD Controller board contains SMD, floppy disk, and Winchester disk drive control circuitry for the IWS workstation, in place of the separate Floppy and Hard Disk Controller boards used in previous IWS workstation MSSs. This section is organized as follows: the SMD, floppy disk, and Winchester disk drive interfaces are described, followed by a listing and explanation of control signals. Control and read/write operations are then described, for SMD, floppy disk, and Winchester disk drives. Subsections within operational descriptions describe specific functional blocks of circuitry used during these operations which may be used by more than one drive, or in both read and write cycles. Appropriate block diagrams and schematic references are included. More information on Storage Module Drives is contained in Appendix D, "Switch Settings for IWS Workstation Memory Configurations."

The circuitry on the SMD Controller board can be separated into six major groups:

- the 8X300 microcontroller
- IWS workstation interface circuitry
- RAM storage
- Winchester disk control, and floppy disk control, read, and write circuitry
- Winchester and SMD read and write circuitry
- SMD control circuitry

Figure 2-5 shows how the major blocks of controller board circuitry are organized.

The microcontroller logic consists, for the most part, of the Signetics 8X300 microcontroller, its 12K-byte microcode ROMs, an interface element with the disk controller interface logic, and input/output ports associated with the control of SMD, floppy disk, and Winchester disk drives.

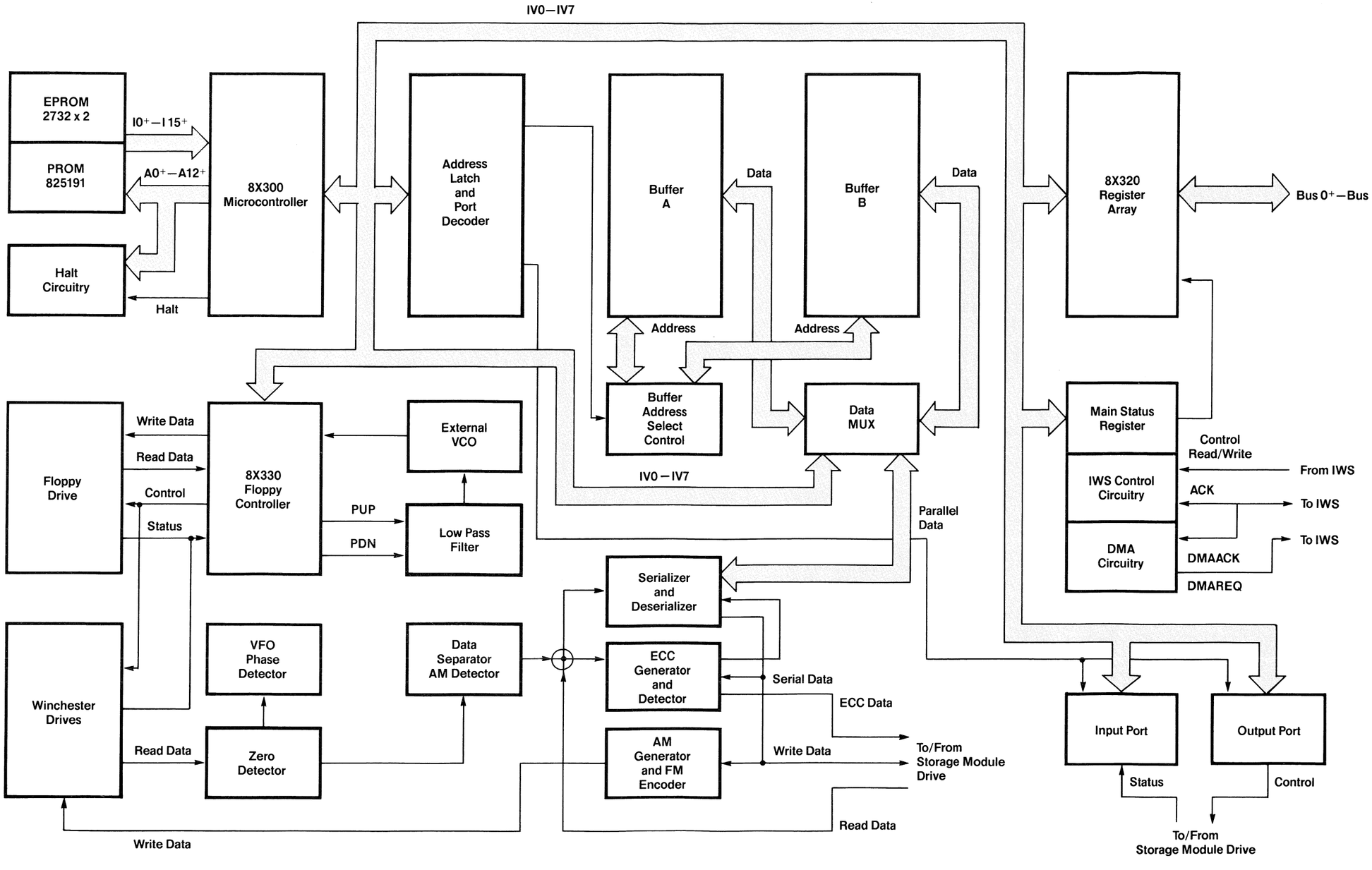


Figure 2-5. SMD Controller Board Block Diagram.

The IWS workstation interface includes IWS workstation control circuitry, the Main Status register, the disk controller interface cable, and DMA read and write channels.

RAM storage consists of four 1K x 4-bit RAMs, which make up buffers A and B, the buffer address select circuitry, and a data multiplexer.

The floppy disk control, read, and write functions, including Winchester hard disk control operations, are handled by the 8X330 floppy disk controller. The 8X330 uses a low pass filter and external VFO (variable frequency oscillator).

Winchester and SMD read and write circuits include a VFO phase detector, a zero detector, a data separator and address mark detector, signal buffering, and ECC (Error Code Checking) and serializing/deserializing circuitry.

SMD control circuitry consists of input/output ports, an address latch and port decoder, and signal buffering.

Figure 2-6, the SMD Controller board schematic, is used as the major reference throughout the following theory of operation discussion.

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NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL DEVICES ARE STANDARD 4+8, 7+14, 8+16, 10+20 GROUND AND POWER CONNECTIONS.

POWER AND GROUND LOCATOR CHART					
REF. DES.	TYPE	GND.	+5V	+12V	-5V
5A, 2A	8T25/91	12	24		
2B	8X300	12	37		
6F	LM358	4	8		
8Q	8X336	1,20	40		
7E	MC4024	3,7,9	1,13,14		
1F	8X320	1,20	40		
16H,16G,14H 9G,9H,15H,17G	MC3450	8	16		12
11H,12H,4H,5H 13H,14G,15G,10H	MC3453	8	16		9

SPARE GATES		
TYPE	REF. DESIGNATOR(S)	QTY.
LM 358	5A	1
7414	4F	3
74LS244	6H	1
74S04	16D, 8A	3,1
		1
74S86	11B	1

REF. DESIGNATORS	
LAST USED	NOT USED
C 81	
RP27	
R65	R1,R7,R5
Q8	
VR2	
CR4	
Y3	

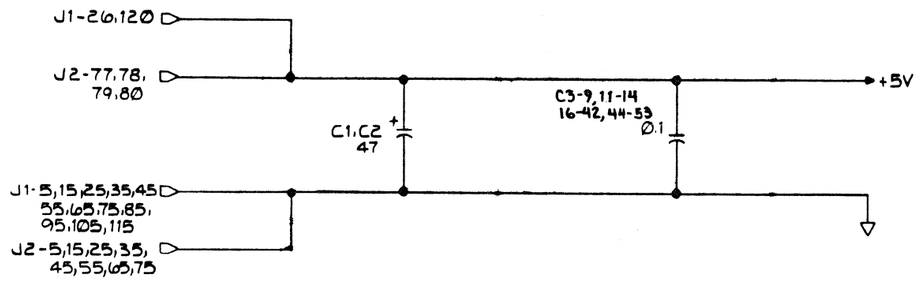


Figure 2-6. SMD Controller Board Schematic. (Page 1 of 11)

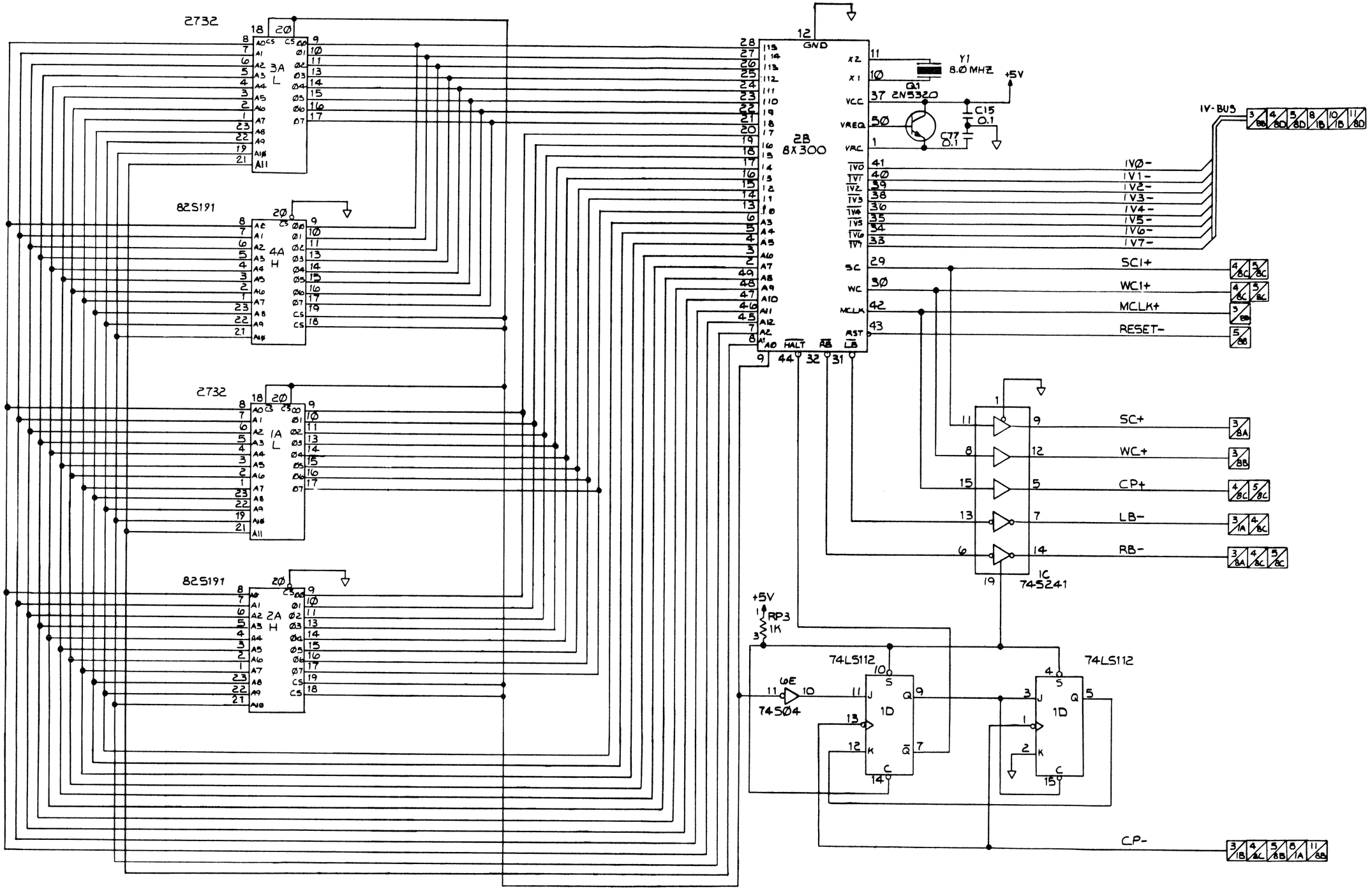


Figure 2-6. SMD Controller Board Schematic. (Page 2 of 11)

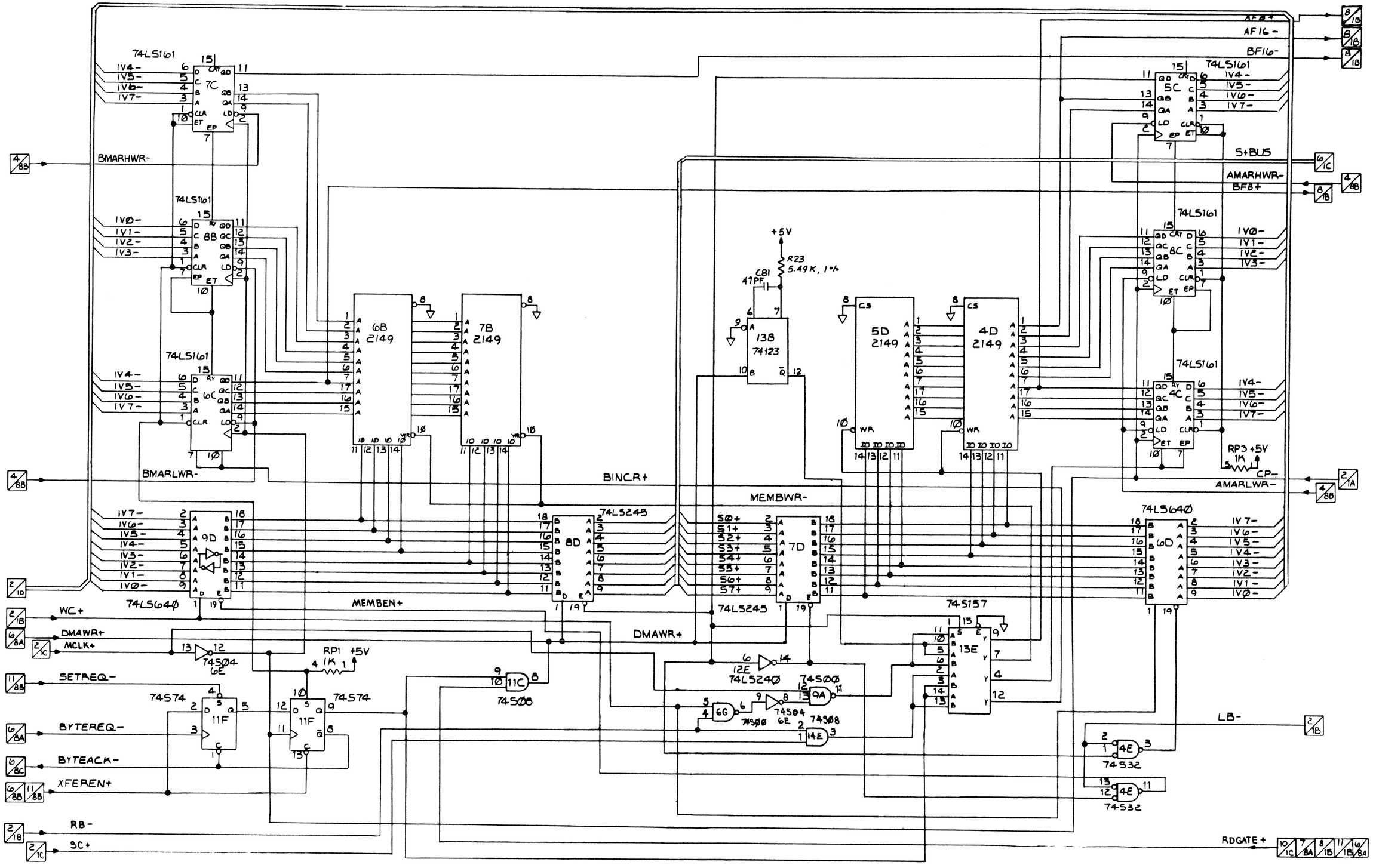


Figure 2-6. SMD Controller Board Schematic. (Page 3 of 11)

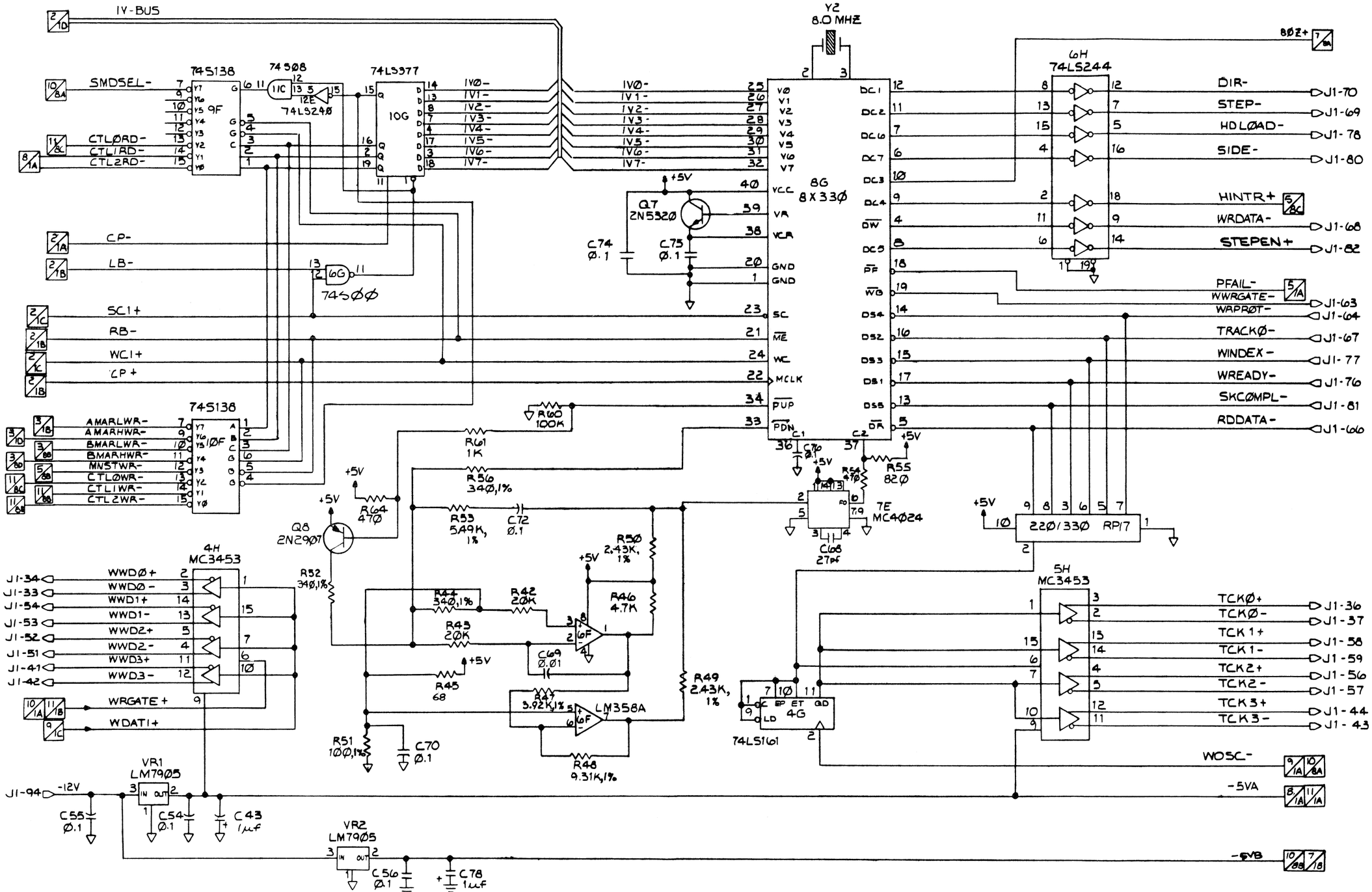


Figure 2-6. SMD Controller Board Schematic. (Page 4 of 11)

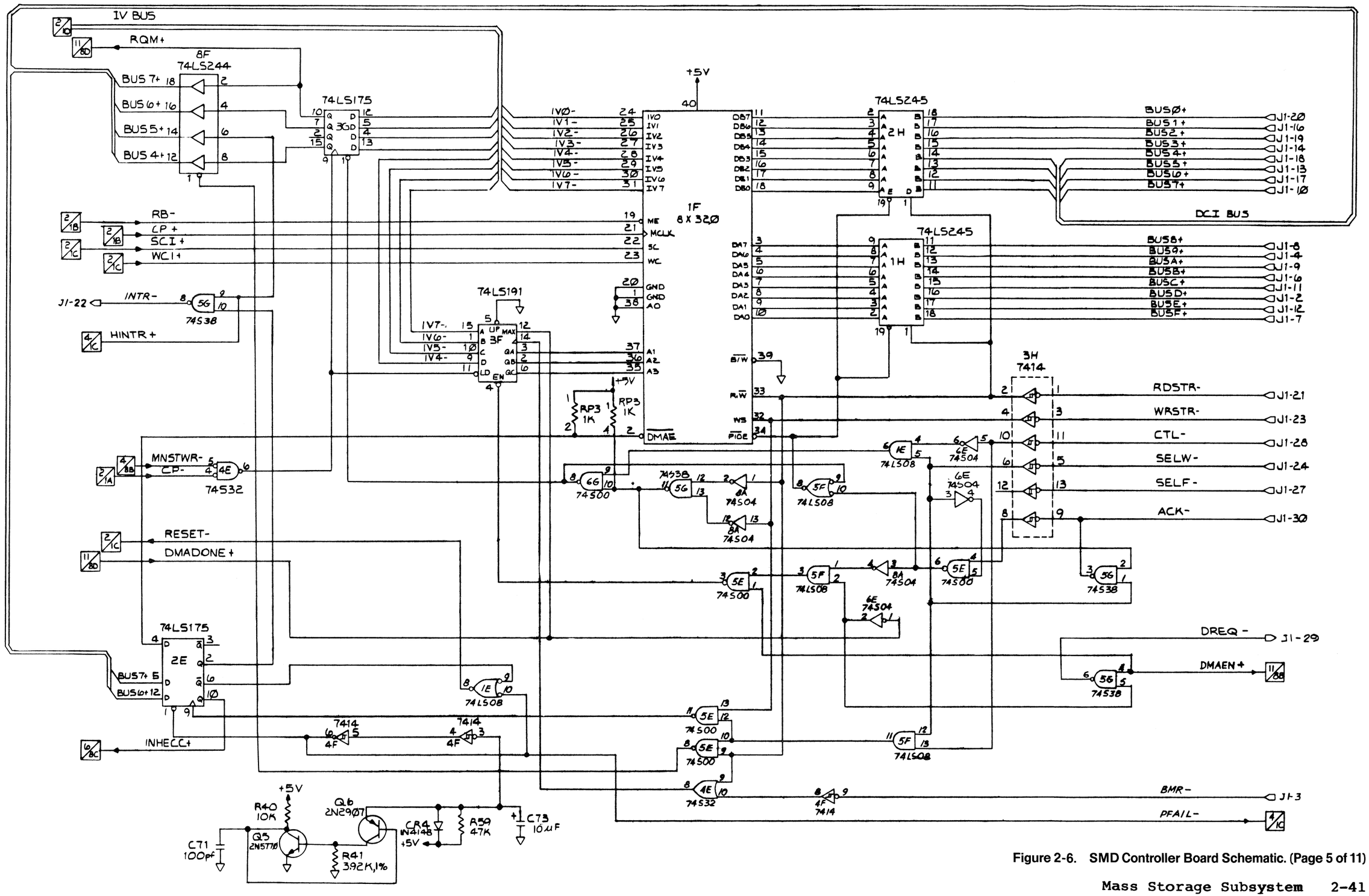


Figure 2-6. SMD Controller Board Schematic. (Page 5 of 11)

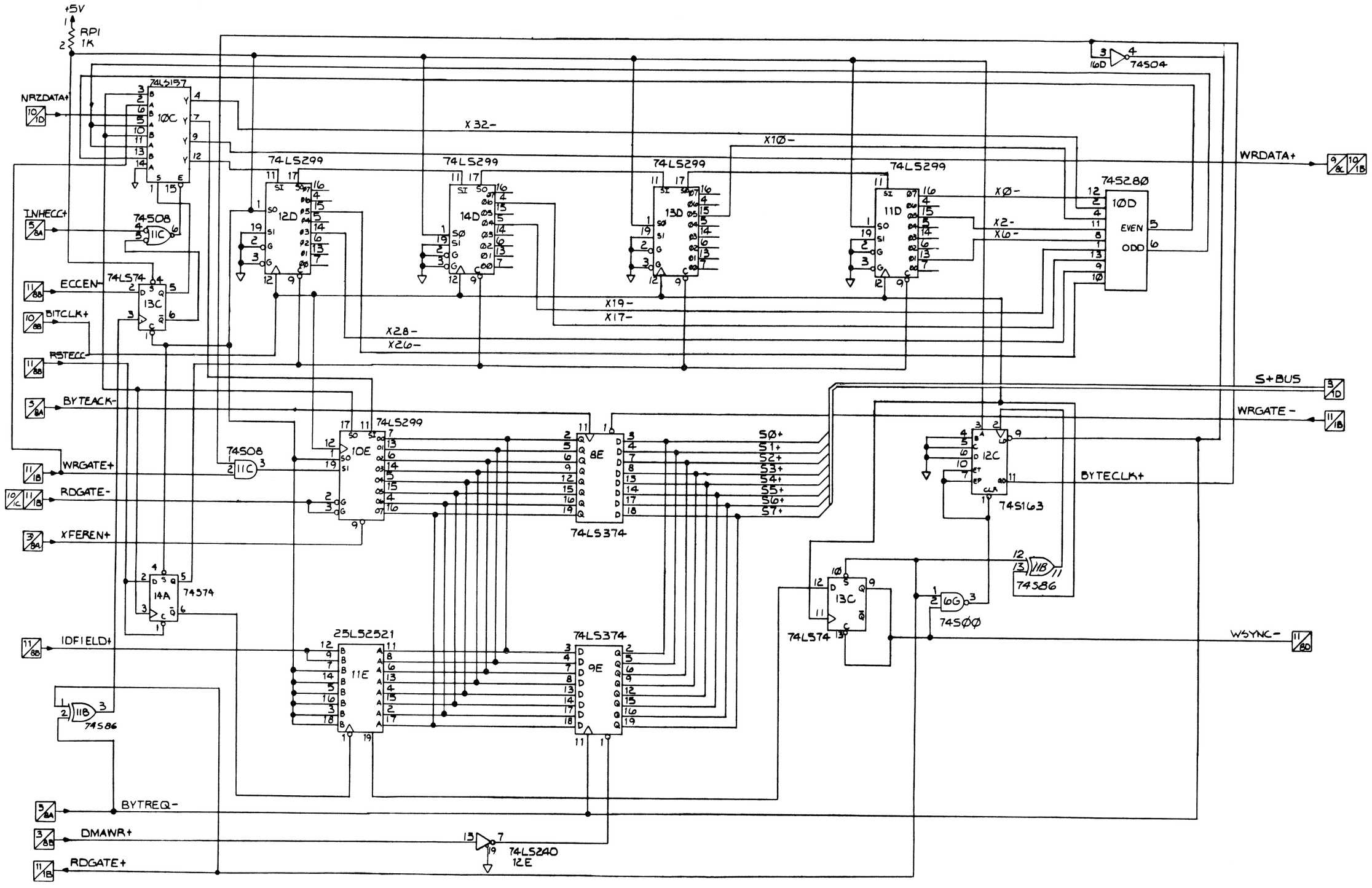


Figure 2-6. SMD Controller Board Schematic. (Page 6 of 11)

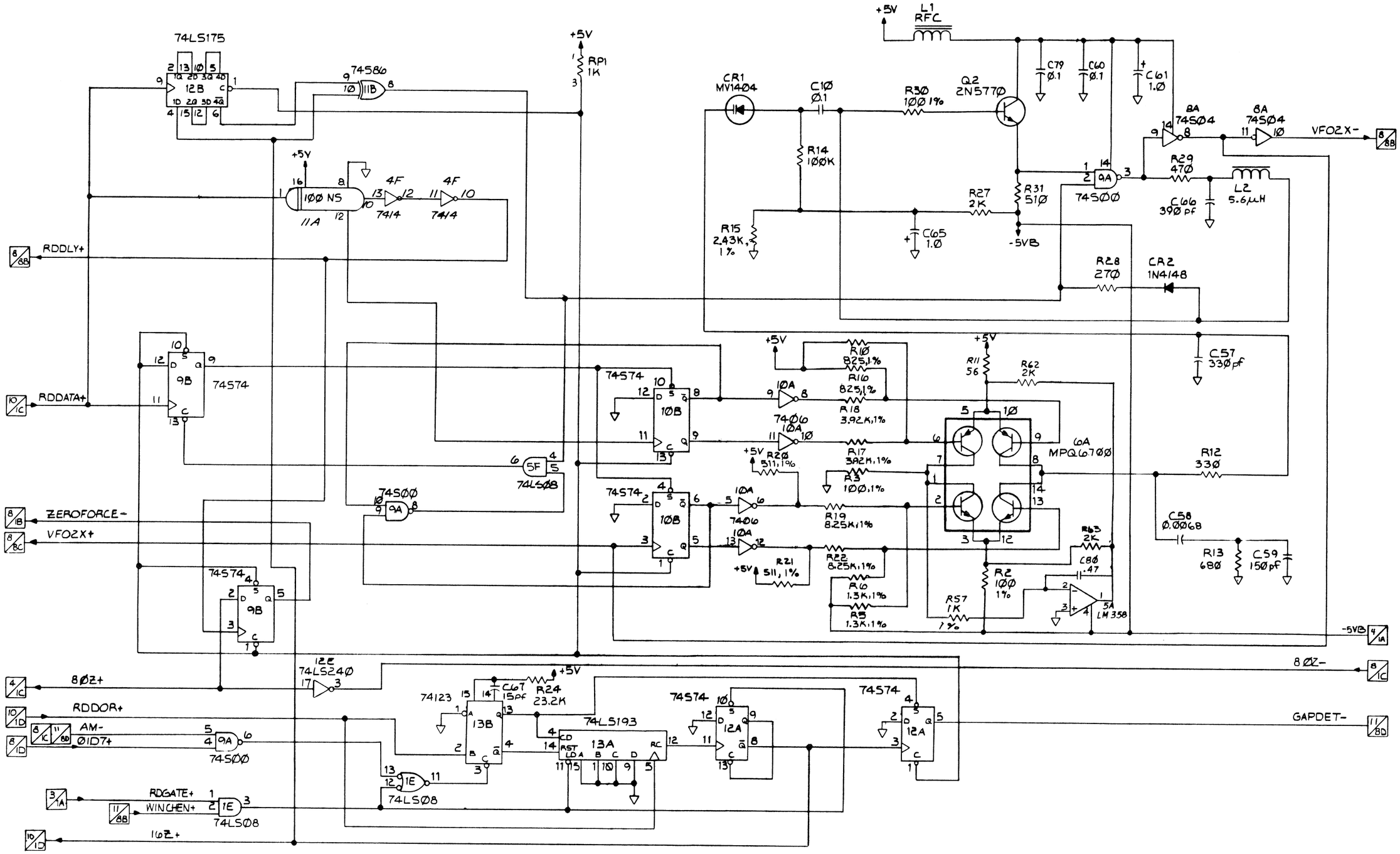


Figure 2-6. SMD Controller Board Schematic. (Page 7 of 11)

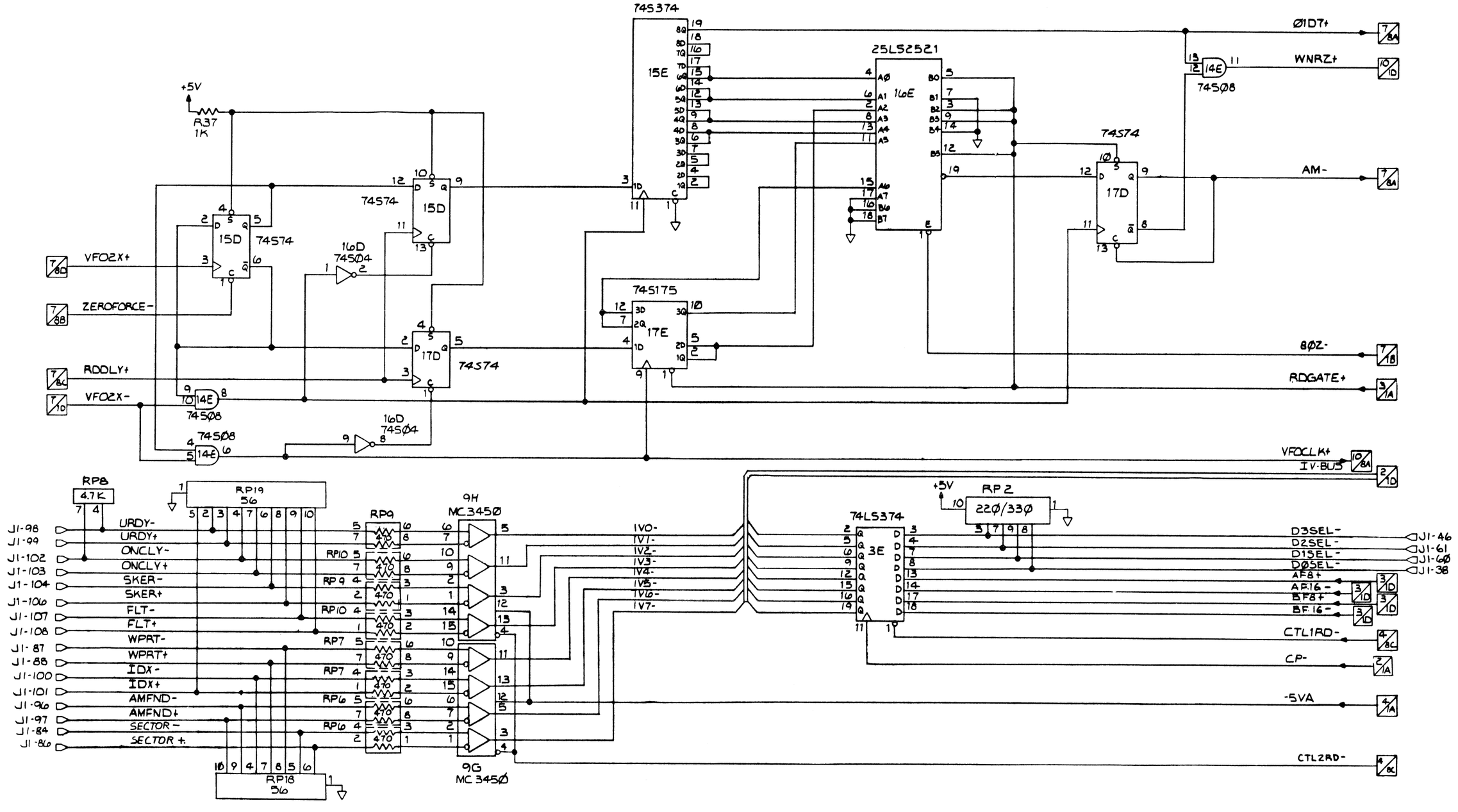


Figure 2-6. SMD Controller Board Schematic. (Page 8 of 11)

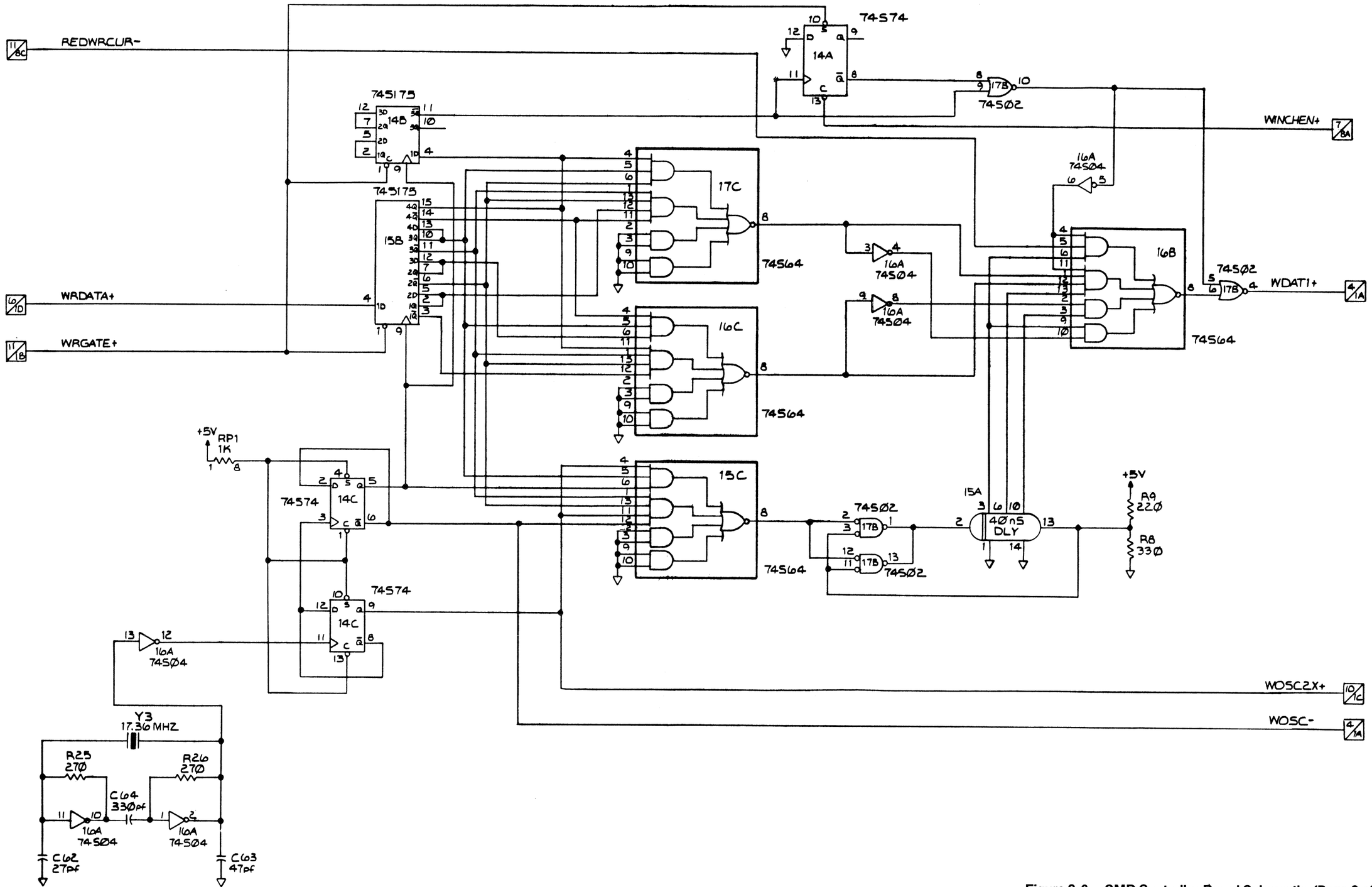


Figure 2-6. SMD Controller Board Schematic. (Page 9 of 11)

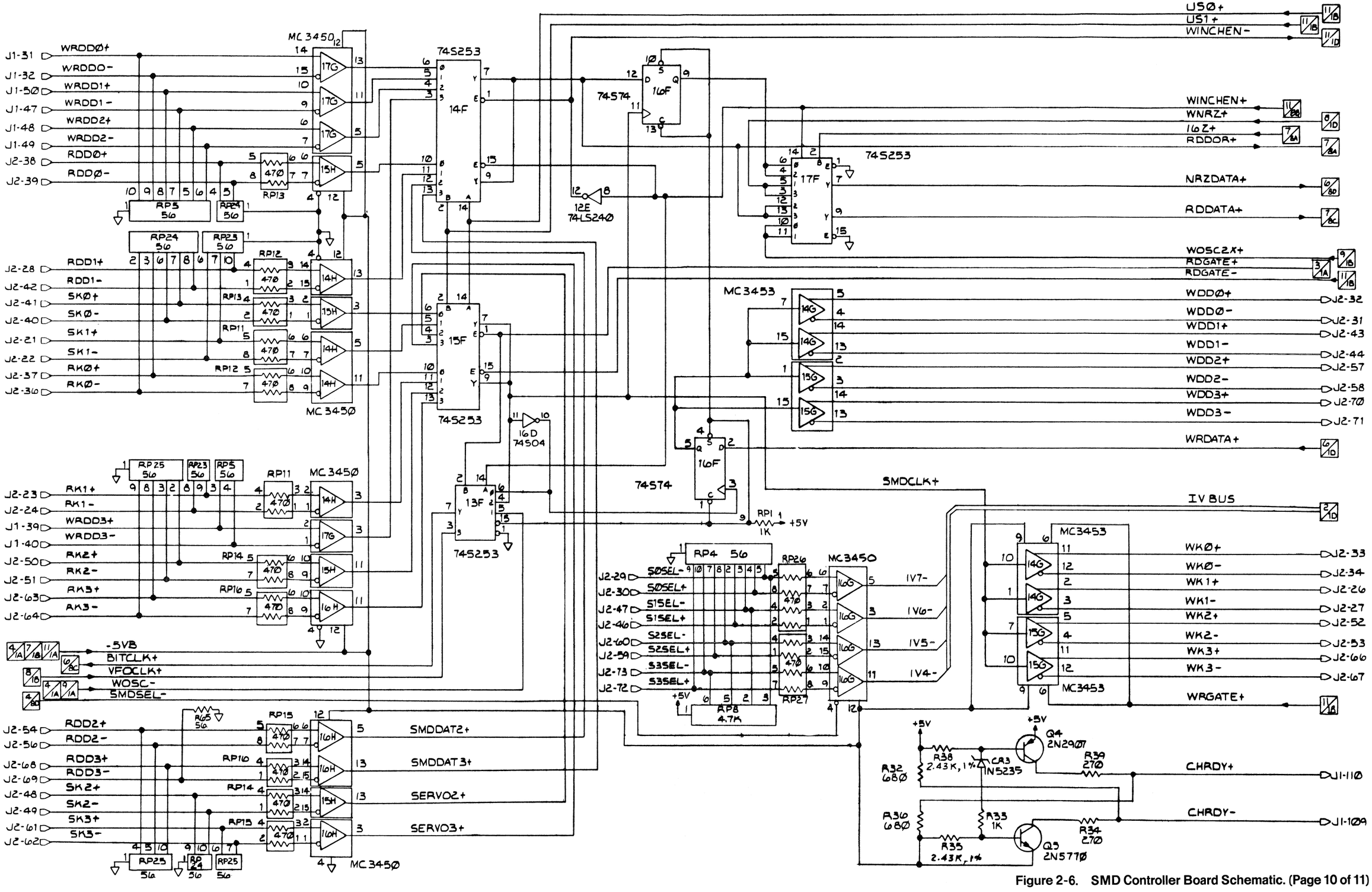


Figure 2-6. SMD Controller Board Schematic. (Page 10 of 11)

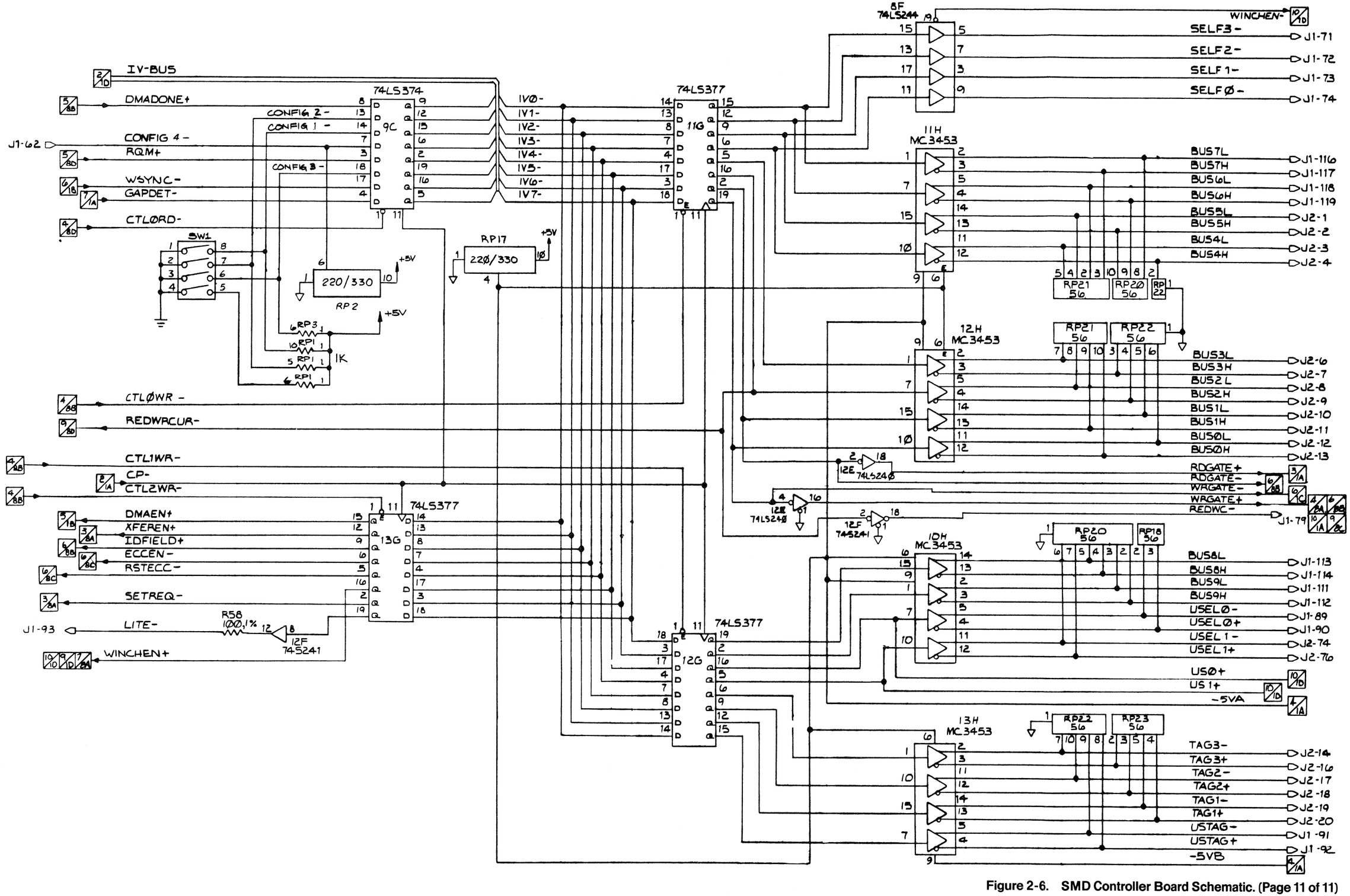


Figure 2-6. SMD Controller Board Schematic. (Page 11 of 11)

8X300 Microcontroller Logic Interface

As shown on page 2 of Figure 2-6, the Signetics 8X300 microcontroller at 2B is the single controlling element for the SMD, floppy disk, and Winchester disk drives. The 8X300 has three separate buses, used for addresses, instructions, and data: A0 through A12, a 13-bit address bus; I0 through I15, a 16-bit instruction bus; and IV0 through IV7, an 8-bit interface vector bus.

The 8X300 operates from a microprogram stored in four PROMs, 1A through 4A. EPROMs 1A and 3A are two 4K-byte 2732s, located at addresses 0 through 0FFF. 2A and 4A are two 2K-byte 82S191s, located at addresses 1000 through 17FF. Each PROM has eight bits, so two PROMS at a time are addressed in parallel by the 8X300's A0-A12 bus, resulting in 16 bits of microcode instruction, which can be read by the 8X300 on its I0-I15 bus.

A0, at pin 9 of the 8X300, is the most significant bit (MSB) of the address bus and determines which set of PROMs is addressed. When A0 is low, the 2732 EPROMs are addressed; when A0 is high, the 82S191 PROMs are addressed.

Since 2732s 1A and 3A have an access time of 450 nsec, which is slower than the program storage access time of 80 nsec required by the 8X300, flip-flop 1D on page 2 of Figure 2-6 acts as a divide-by-three counter, halting the 8X300 for two out of every three instruction cycles when it accesses EPROM data.

When A0 goes low to select 1A and 3A, it sets pin 11 of flip-flop 1D high. CP- (Clock Pulse) at input pins 1 and 13 of 1D is the inverted buffered MCLK+ from the 8X300. At the falling edge of CP-, pin 9 of 1D goes high, sending Q- output pin 7 (HALT-) low and halting the 8X300 in its execution of instructions. At the next Clock Pulse, pin 5 of 1D goes high, setting pins 11 and 12 high so that, on the third Clock Pulse, pin 9 of 1D toggles low, enabling the 8X300. This inserts two wait states in the 8X300's normal instruction cycle time of 250 nsec, causing the 8X300 to run at 750 nsec and providing enough time for the EPROM address to become valid on the I0 through I15 lines.

A high A0 bit selects the 82S191s, which have an access time of 50 nsec. The divide-by-three

circuitry is not used when the 82S191s are selected.

As mentioned above, the 8X300 communicates with the controller board circuitry via the Interface Vector, or IV bus, at IV0-IV7. The IV bus is multiplexed to supply data and address information to two independent banks (right and left) of input/output devices, which are used for controlling drive read and write circuitry and communicating with the IWS workstation.

Buffers A and B, as shown on page 3 of Figure 2-6, are the only input/output devices on the left bank of the IV bus. Each data buffer is made up of two 1K x 4-bit RAMs: 4D and 5D comprise buffer A, and 6B and 7B comprise buffer B. The RAMs are used to store variables and temporarily store and buffer data being transferred between one of the disk drives and the IWS workstation.

The other input/output devices are on the right bank of the IV bus and are explained in the "IWS Workstation/SMD Controller Board Interface" subsection, below. These devices consist of

- An 8X320 register array at 1F (shown on page 5 of Figure 2-6), which provides an interface between the IV bus and the BUS0+ through BUSF+ data lines from the IWS workstation.

- 8G, an 8X330 floppy disk controller (shown on page 4 of Figure 2-6), which transfers read and write data for the floppy disk drive, and control signals for both floppy and Winchester drives.

- Input/output ports, detailed in the "SMD Controller Board Architecture" subsection, which handle drive control signals.

The 8X300 reads from and writes to all of the IV bus input/output devices using five control lines as shown on page 2 of Figure 2-6: LB- (Left Bank) and RB- (Right Bank) at pins 31 and 32 of 2B; WC1+ (Write Command) at pin 30; SC1+ (Select Command) at pin 29; and MCLK- (Master Clock) at pin 42 of 2B. All of these lines are buffered at 1C and then sent to the input/output devices. The 8X300 then selects either a right or left bank device and places an eight-bit address on the IV bus when both SC1+ and MCLK+ are asserted.

Each port or register on the IV bus is selected by address register 10G (page 4 of Figure 2-6). Once the 8X300 selects a port, that port remains selected until the SC1+ (Select Command) line goes high again with a different address. To write data to a port on the IV bus, the 8X300 places eight bits of data on the IV bus, and sets WC1+ high and RB- low (LB- if the disk data buffer is being written to) at the falling edge of MCLK+. To read data from a port, the 8X300 sets WC1+ low and latches data onto the IV bus.

8X320 IWS Workstation-SMD Controller Board Interface

The 8X320 register array at 1F (see page 5 of Figure 2-6) contains 16 eight-bit internal registers. These registers store data, command, and status information for the controller, providing an interface between the 8X300 IV bus, and the IWS Workstation DCI (Disk Controller Interface) bus.

The 8X320 register array is therefore thought of as having a primary (DCI) and a secondary (IV bus) port. The DCI bus cable connects the IWS workstation, through the SMD I/O Extender board, to the SMD Controller board through the primary port, and consists of BUS0+ through BUSF+, and five control signals. The secondary port accommodates the IV bus, as well as an eight-bit control register for command and status signals.

The 8X300 reads from or writes to the secondary port as described in the preceding "8X300 Micro-controller Logic Interface" subsection.

The 8X320 A0+ through A3+ (address) input lines select one of the 16 registers in the 8X320 to be used for a transfer. When a register has been selected, either the RDSTR- (Read Strobe), for a status or data read, or WRSTR- (Write Strobe) line, for a command or data write, is pulsed, causing data to be transferred onto the DCI bus (BD0 through BD7), where it is read by the IWS workstation. A description of the DCI and command signals follows, as well as an explanation of the input/output command sequence and DMA transfers.

Disk Controller Interface Signals

The disk controller interface (DCI) is structured around a 16-bit bidirectional data bus and six control signals: WRSTR- (Write Strobe), RDSTR- (Read Strobe), CTL- (Control), SELW- (Select Winchester), DREQ- (Data Request), and ACK- (Acknowledge). A description of the BUS0+ through BUSF+ lines, and all control signals and their functions follows:

Data Bus. The BUS0+ through BUSF+ data bus is 16 bits wide, bidirectional, and tristated. It is used to transmit control and data from the IWS workstation to the controller, and status and data from the controller to the IWS workstation. Bit F is the most significant bit, and bit 0 is the least significant bit.

Select Winchester (SELW-). The Select Winchester signal indicates a non-DMA input/output operation transfer. When low, SELW- enables non-DMA transfers between the Winchester disk drive and the controller board. When SELW- is high, the controller board responds to DMA transfer requests only.

Write Strobe (WRSTR-). The Write Strobe signal indicates that data is being sent from the IWS workstation and received by the controller. The content of the data bus is strobed into the input buffer on the trailing edge of the WRSTR- pulse. Information transmitted to the controller is data when CTL- is high, and Main Status register information when CTL- is low.

Read Strobe (RDSTR-). A low Read Strobe signal indicates that data is being sent from the controller and received by the IWS workstation. This signal, generated by the IWS workstation, copies the contents of the DCI data bus back into the IWS workstation. RDSTR- does not affect the state of the controller when reading the Main Status register. When user data or status bytes are read from the data register, the Main Status register is cleared.

Control (CTL-). The Control signal is used to define the type of information being transmitted on the DCI data bus. When CTL- is low, the contents of the Main Status register are transmitted. When CTL- is high, the contents of the Data Buffer register are transmitted. Table

2-10 shows specific relationships between the three DCI control signals (0=inactive, 1=active).

Table 2-10. DCI Signal Truth Table.

Control	Read Strobe	Write Strobe	Operation by the IWS Workstation
0	0	0	No operation
0	0	1	Write data or command
0	1	0	Read data or sense
0	1	1	Error condition
1	0	0	No operation
1	0	1	Write to controller
1	1	0	Read controller status
1	1	1	Error condition

Data Request (DREQ-). The controller asserts the Data Request signal to indicate that data is ready to be transferred. DREQ-, ACK-, and RDSTR- are used to transfer data in a read operation. Data transfers are 16 bits wide and 7 words long. DREQ- is used to transmit data in a read or write operation.

Acknowledge (ACK-). The IWS workstation uses a low Acknowledge signal to provide a handshake response to RDSTR- during non-DMA transfers. During such transfers, ACK- is asserted until RDSTR- goes high. The controller also uses ACK- as a response to a low WRSTR- signal. On the trailing edge of WRSTR-, the contents of the bus are copied onto the controller and ACK- goes high.

During DMA transfers, the IWS workstation asserts ACK- when it is ready to transfer data. Transfers under ACK- in the DMA mode are controlled by RDSTR- or WRSTR-, and no handshake with the IWS workstation exists.

Interrupt Request (INTR-). The Interrupt Request signal is asserted at the end of each read or write command. The IWS workstation responds by reading the termination status, which indicates the success or failure of the

command. INTR- is cleared when the IWS workstation reads all status bytes from the Main Status register. If the controller requires further service, INTR- goes low and remains low until the IWS workstation responds.

8X330 Floppy Disk/Winchester Disk Drive-SMD Controller Board Interface

As shown on page 4 of Figure 2-6, the 8X330 at 8G provides control and status line interface between the SMD Controller Board IV bus and the floppy and Winchester disk drives located in the MSS and MSX. The 8X330 also contains the floppy disk drive read and write circuitry.

Data for floppy disk or Winchester disk read and write operations is input and output through port 78h of the 8X320 register (see page 5 of Figure 2-6). After an MSS or MSX floppy or Winchester disk drive is selected for use by the 8X300, before the operation begins, the 8X300 loads internal registers in the 8X330 to set up control line operating characteristics for the selected drive. These operating characteristics, or floppy disk/Winchester disk drive control signals, are then output through motherboard connector J1 to the disk drives.

Floppy Disk/Winchester Disk Drive Control Signals

The 8X330 floppy disk controller, shown on page 4 of Figure 2-6, outputs the STEP- (Step Pulse) line at pin 7 of buffer 6H to increment the drive read/write head carriage one track on the disk surface, either in or out, depending on the state of the DIR- (Direction) signal output at pin 12 of 6H. SIDE-, at pin 16 of 6H, selects which disk side is used, HDLOAD- (Head Load) at pin 5 controls head loading onto disks, and WRDATA- (Write Data) at output pin 9 is the precompensated write data, sent only to the floppy disk drive.

The 8X330 HINTR+ signal is not output to a drive. Instead, it controls on-disk gating of the INTR- signal, which controls the IWS workstation/drive interrupt state. The WWRGATE- (Winchester Write Gate) signal at pin 19 of 8G is the write data enable for the selected disk drive

and is automatically disabled during power-up or a power failure.

Status lines from the disk drives to the 8X330 include: WRPROT- (Write Protect) at pin 14 of 8G to indicate that the selected disk drive is allowing only read operations; TRACK0- (Track 0) at pin 16 to indicate that the selected device's read/write head is positioned over the first readable track on the disk media; WINDEX- (Winchester Index) at pin 15 to indicate that the disk drive is detecting the beginning of the first physical sector on the track; WREADY- (Winchester Ready) at pin 17 to indicate that the selected drive is ready to perform a read, write, or seek operation; SKCOMPL- (Seek Complete) at pin 13 of 8G to indicate whether the Winchester seek operation just performed was successful; and RDDATA- (Floppy Read Data) at pin 5, which indicates that read data is being sent to the 8X330 data separator and phase-locked loop.

The PFAIL- (Power Failure) input to the 8X330 at 8G pin 18 disables WWRGATE- when the +5-V dc power supply falls below +4.5 V dc. When WWRGATE- is disabled, the 8X300 is simultaneously reset by the RESET- signal.

Floppy Disk Read and Write Circuitry

The 8X330 floppy disk controller at 8G, as shown on page 4 of Figure 2-6, contains almost all of the read and write circuitry required to convert data bytes from the IV bus to MFM floppy disk data during a write operation, and back again to data bytes during a read operation. The only components required to make the floppy disk controller complete are: the 8.0-MHz crystal, Y2; the variable frequency oscillator at 7E; a pass transistor, Q7, for the on-chip voltage regulator; and a low-pass filter, the active components of which are two operational amplifiers at 6F.

When a read or write command is sent to the 8X320 Command register at 1F and a drive is specified (for example, F0, the floppy disk drive), the 8X300 configures the 8X330's internal registers to perform the selected operation. Through control lines output from the 8X330, the 8X300 selects the drive, read/write head, and the direction of read/write head travel. Next, the

8X300 performs a seek to the specified track on the floppy disk by pulsing the STEP- line a specified number of times.

Read Operation

Read data for the floppy disk drive is sent to pin 5 of the 8X330 at 8G from pin 66 of mother-board connector J1. The 8X330 performs internal data separation to generate a data window and synchronized data for on-chip data processor and CRC (Cyclic Redundancy Check) use. The external low-pass filter shown on page 4 of Figure 2-6 controls the 8X300's phase-locked variable frequency oscillator (VFO) at 7E during the data separation process. Two output signals from the 8X330's on-chip phase detector, PUP- (Pump Up) at pin 34, and PDN- (Pump Down) at pin 33, are sent to the low-pass filter. PUP- and PDN- indicate that the frequency of the oscillator is either too low or too high, and result in a change in the frequency of pin 37. If no floppy disk read operation is taking place, the VFO is locked to the 8.0-MHz crystal frequency.

After data separation, the 8X330 deserializes floppy disk data, which is then read by the 8X300 on the IV bus. The RAM data buffer on the left bank of the IV bus is not used for floppy disk read and write operations. Instead, the 8X300 transfers floppy disk data it reads from the 8X330, one byte at a time, through the IV bus into the data register (port 78h) at 1F. (See page 5 of Figure 2-6.) When the 8X300 has assembled two bytes in the 8X320 register, it loads counter 3F with the proper address bit to determine A1, A2, and A3 inputs to 1F at pins 37, 36, and 35. (A1, A2, and A3 determine which address the IWS workstation reads from or writes to.)

When it has transferred data into the 8X320, the 8X300 asserts DMAEN+ (DMA Enable), sending pin 4 of gate 5G high. DMAEN+ is gated with an inactive DMADONE+ through 5G, outputting a low DREQ- (DMA Request) signal to the IWS workstation from pin 6 of 5G. This begins a DMA transfer.

DMA Read Data Transfer. The IWS workstation responds to DREQ- by asserting ACK-, CTL-, and RDSTR-, for a read operation. Every time the IWS workstation strobes RDSTR-, it increments counter

3F at A1, A2, and A3, and changes the 8X320 address. The 8X300 then transfers another word to the 8X320 and starts the DMA cycle again until an entire sector has been read. When counter 3F reaches its maximum count, it sets the MAX output pin 12 high, sending pin 1 of 6E low, and enables DMADONE+. Inverter 6E then outputs a high at pin 2, thereby disabling DREQ- at pin 6 of 5G.

Data flow direction is controlled by RDSTR- (Read Strobe). During a read operation, RDSTR- is asserted and passes through inverter 3H to set pin 1 of transceivers 1H and 2H high. When pin 1 is set high, data flow is from A to B. RDSTR- is also sent to 1F pin 32, allowing data to be read from the 8X320 when RDSTR- is strobed by the IWS workstation.

The asserted ACK- signal passes through inverter 3H at output pin 8, and sets pin 5 of 5E high, while (since a floppy disk is being read from) an inactive SELW- (Select Winchester) signal is also inverted and buffered to set pin 4 of 5E high. The output of 5E at pin 6 is low, and the resulting low output at 5F pin 8 enables 1H and 2H at pin 19, and the 8X320 at pin 34 (PIOE-) PIOE- enables the 8X320 to transfer data into transceivers at 1H and 2H. Since, during a read operation, data flow is already from side A to side B, data can now be read by the IWS workstation through the DA and DB data buses when RDSTR- is strobed.

When an entire sector has been read by the IWS workstation through the BUS0 through BUSF lines, the 8X300 interrupts the IWS workstation with a low INTR- command. When the IWS workstation receives the interrupt, it reads ST0 to determine the success of an operation. If there is a disk read error, the data is still transferred from the floppy disk drive to the IWS workstation memory. The error is then detected when the IWS workstation reads status registers after completion of a DMA transfer, as described in the Workstation Hardware Manual and the "SMD Controller Board Architecture" subsection.

Write Operation

Before a write operation occurs, the 8X300 sets up the 8X330 floppy disk controller for a write operation in the manner described above. The

8X300 then sets up register 3F for a one-word transfer, and sets up starting addresses in the 8X320 for data transfers. When this is done, the 8X300 asserts DMAEN+, sending DREQ- to the IWS workstation through pin 6 of 5G as described. This begins a DMA write data transfer.

DMA Write Data Transfer. The IWS workstation, as in a read operation, responds to DREQ- by asserting ACK, CTL-, and WRSTR-, instead of RDSTR-. The low ACK- and high SELW- signals are gated together, as in the read operation, resulting in a low output at pin 8 of 5F, and enabling transceivers 1H and 2H and the 8X320 for a write data transfer.

During a write operation, RDSTR- is high and passes through inverter 3H to set pin 1 of 1H and 2H low. When pin 1 is low, data flow is from B to A, causing data from the IWS workstation bus to flow to the 8X320. An inverted WRSTR- signal enables the 8X320 at pin 32 of 1F, allowing data to be written into the 8X320 when WRSTR- is strobed by the IWS workstation. BMR- (Buffered Memory Read) is also set low by the IWS workstation during an ACK-, and is NORed with a high RDSTR-, sending output pin 8 of 4E high and incrementing counter 3F at pin 14. After data has been strobed into 3F, the MAX output at pin 12 is set high, enabling DMADONE+, which is sent to the 8X300. The 8X300 disables DMAEN+ when it receives DMADONE+ and sends data stored in the the 8X320 register to the 8X330 floppy disk controller. MFM data is then sent to Drive F0 from the 8X330 at pin 4 (WRDATA-).

When the 8X330 floppy disk controller receives a byte of data, it sends an internal byte ready flag signal to the 8X300. The 8X300 then repeats a WRSTR- cycle until an entire sector (512 bytes) has been received from the IWS workstation. When 512 bytes have been received and transferred, the 8X300 issues a command to the floppy disk controller to disable the WWRGATE- (Write Gate) command. The 8X300 then interrupts the IWS workstation by asserting INTR-, and the IWS workstation reads ST0 to determine the success of the write operation.

SMD and Winchester Disk Drive-SMD Controller Board Interface

Signals from the Storage Module Drives (SMDs) are sent to the SMD I/O Extender board through connectors J3 and J4, cables A and B. Cable A contains control and status signals, and Cable B contains data and clock signals. Tables 2-11 and 2-12 list signals from cables A and B, and the Tag/Bus signal definitions are shown in Table 2-13.

Table 2-11. SMD Cable A Signals.

From Controller Board	Pin Numbers
USTAG (Unit Select Tag)	22, 52
S0SEL - S3SEL (Unit Select 0 - 3)	23, 24, 26, 53, 54, 56
TAG1 - TAG3	1, 2, 3, 31, 32, 33
BUS0 - BUS9	4-13, 34-43
CHRDY (Channel Ready)	14, 44
From SMD	**Pin Numbers**
ST0 - ST5 (Status 0 - 5)	15, 16, 17, 19, 20, 28, 45, 46, 47, 49, 50, 58
WINDEX	18, 48
SECTOR	25, 55

SMD data and clock signals enter through the J2 connector as shown on page 10 of Figure 2-6, pass through a transceiver at 14H and 16H, and are multiplexed out through 14F and 15F as determined by WINCHEN+ (Winchester Enable). SMD control, data, and status signals are input through connectors J1 and J2, as shown on page 11 of Figure 2-6, and pass through transceivers 10H through 13H to input/output latches 11G and

12G. Data from differential signal pairs BUS0 - BUS9 is then latched through 11G, depending on the status of CTL0WR- and SMD status signals, and can be either written to or read from the IV bus.

Table 2-12. SMD Cable B Signals.

From Controller Board	Pin Numbers
WDD0 - WDD3 (Write Data)	8, 20
WK0 - WK3 (Write Clock)	6, 19
From SMD	
SK0 - SK3 (Servo-Clock, 1F Write Clock)	2, 14
RDD0 - RDD3 (Read Data)	3, 16
RD0 - RD3 (Read Clock)	5, 17
S0SEL - S3SEL (Unit Select)	9, 22

Table 2-13. Tag/Bus Lines.

Bus	Tag 1 Cylinder Address	Tag 2 Head Address	Tag 3 Control Select	Pin Numbers
0	1	1	Write Gate	4, 34
1	2	2	Read Gate	5, 35
2	4	4		6, 36
3	8			7, 37
4	16		Fault Clear	8, 38
5	32			9, 39
6	64		RTZ	10, 40
7	128			11, 41
8	256			12, 42
9	512			13, 43

SMD Interface Signals

Cable A Control Signals

USTAG (Unit Select Tag). USTAG gates the Unit Select 1 and 2 signals and is sent by the controller board to select the desired SMD drive.

USEL0, USEL1 (Unit Select 1,2). These two signals are binary coded by the controller board to select the desired disk and are validated by the leading edge of Unit Select Tag.

BUS0 through BUS9 (Tag/Bus). This 10-bit bus is sent to drives from the controller port 11G on page 11 of Figure 2-6. The content of this is defined by Tags 1, 2, and 3, described below.

TAG1 (Cylinder Address). The leading edge of TAG1 gates the cylinder address, causing the contents of bus lines (BUS0 - BUS9) to be set into the SMD cylinder address register. The bus lines must be stable prior to, and remain stable throughout, TAG1.

TAG2 (Head Address). The leading edge of TAG2 gates the head address, causing the contents of BUS0 - BUS9 to be set into the SMD head address register. The bus lines must be stable prior to, and remain stable throughout, TAG2.

TAG3 (Control Select). TAG3 enables BUS0 - BUS9. All bus signals are defined as control signals, and each bit has a different meaning.

BUS0 (Write Gate). This bit enables a write operation on a specified track/sector. This signal is validated under the following conditions:

Unit Ready	1
On Cylinder	1
Seek End	1
Seek Error	0
Fault	0
File Protect	0

If Write Gate is asserted in conditions other than the above, a fault occurs and writing is inhibited.

BUS1 (Read Gate). This bit causes a data read from a specified track/sector.

BUS2 and BUS3. Unused.

BUS4 (Fault Clear). This bit clears the fault status. If a seek error fault condition still exists, however, this status cannot be cleared (see RTZ, BUS6).

BUS5. Unused.

BUS6 RTZ (Return to Zero). This bit clears a Seek Error Condition and, no matter where the read/write heads are located on the disk, they are returned to cylinder zero and head zero.

BUS7 - BUS9. Unused.

CHRDY (Channel Ready). CHRDY is sent by the controller to prevent damage to files when control unit power is lost. CHRDY, therefore, is asserted when the controller is available and disasserted if a power failure of the controller occurs. A Unit Select is not possible when the Channel Ready signal is low.

Cable A Status Signals

URDY (Unit Ready). URDY is asserted by the SMD when a drive initial seek is completed and goes inactive when power is turned off.

ONCLY (On Cylinder). ONCLY is asserted with URDY and is cleared by the next seek or RTZ command. ONCLY is asserted again when a Seek or RTZ operation is completed, and deasserted if a Seek Error occurs.

WPRT (Write Protect). An asserted WPRT signal may indicate that all tracks are write-protected. Attempting to write while this signal is asserted will cause a fault.

SKER (Seek Error). SKER is asserted by an SMD if there is an error during a Seek or RTZ operation. If, for example, On Cylinder is not set, but B Cable Seek End is asserted, SKER is active. SKER is cleared by an RTZ instruction. The conditions for such error status are as follows:

- RTZ or Seek was not completed within a specified time.

- An illegal cylinder address was specified.
- The heads were moved to a position outside of the recording area.

FLT (Fault). FLT indicates a drive fault.

IDX (Index). IDX is a two-byte pulse that occurs once per disk revolution, is read by the controller board during a read/write operation, and is used for reference. The index signal is invalid during initial Seek or RTZ operation.

SECTOR (Sector). SECTOR is read by the controller board to signal the beginning of a sector. SECTOR is a 1-bit pulse that occurs 31 times per track, and is derived from the Index signal and Byte Clock.

Cable B Write Data

WDD0 - WDD3 (Write Data). Cable B carries NRZ (Non Return to Zero) data to be written onto SMDs, which must be synchronized with Write Clock signals.

WK0 - WK3 (Write Clock). WK0 - WK3 is a return signal of SK (1F Write Clock) issued from the controller board (shown on page 10 of Figure 6).

Cable B Control and Status Signals, and Read Data

SK0 - SK3 (1F Write Clock). This servo-clock signal is sent from SMDs to synchronize the WK0 - WK3.

RDD0 - RDD3 (Read Data). Read Data lines transmit SMD-recovered data to the controller board in the form of NRZ data synchronized with the 1F Read Clock.

RK0 - RK3 (1F Read Clock). RK0 - RD3 are only valid during a read operation, and are synchronized with RDDATA-.

US1, US2 (Unit Selected). US1 and US2 activate receivers and drivers on the A cable. When the two unit select signals (gated by the Unit Select Tag) and the logical address of the unit are the same, the status signals are issued from the SMD.

SKCOMPL- (Seek Complete). The Seek Complete signal indicates that a Seek, RTZ, or Offset operation has terminated. This signal may be used as an interrupt to the control unit.

SMD Control Circuitry

To perform an SMD control function, the 8X300 first enables the US0+ or US1+ signals (Unit Select). These signals are enabled by the USTAG signals to input control signals from the selected SMD drive through port 12G. (See page 11 of Figure 2-6.) Unit Select signals are buffered through 16G (shown on page 10 of Figure 2-6) onto the IV bus, and SMD control data is read by the 8X300.

SMD and Winchester Disk Drive Read and Write Circuitry

> NOTE
>
> All page references in the following logic description refer to the sheet number of Figure 2-6, the SMD Controller board schematic.

As shown on page 3 of Figure 2-6, there are two buffers on the controller board: buffer A, made up of RAM chips 4D and 5D; and buffer B, comprised of RAMs 6B and 7B. Before any SMD or Winchester read or write cycle starts, the 8X300 selects buffer A or buffer B to store disk data during the operation. In the following discussion, buffer B transfers are described for consistency, although buffer A may be used by the controller as well. When buffer B is selected for a read or write operation, the 8X300 loads starting buffer location addresses into counters, using the BMARHWR- and BMARLWR- (Buffer B Memory Address Register High Byte Write and Buffer B Memory Address Register Low Byte Write) signals from page 4.

As shown on page 3 of Figure 2-6, the most significant bit at pin 11 of counter 5C determines which buffer is selected during a read or write operation, and whether data is read or written.

A low at pin 11 selects buffer B for a disk data transfer, and a high at pin 11 selects buffer A. When buffer B is selected, transceiver 8D is also enabled at pin 19.

While disk data is being transferred into one buffer by the controller board circuitry during a read/write operation, the 8X300 can read or write data from the other buffer, using circuitry described below.

During a read operation, the 8X300 selects SMD or Winchester data to be read through multiplexers 14F and 15F by setting the WINCHEN+ signal high to select data from the Winchester drive, and low when data is selected from an SMD. Once either SMD or Winchester data has been selected, USEL0+ and USEL1+ (Unit Select) signals select the channel that is used to receive data.

Winchester Disk Drive Read Operation

If the the 8X300 selects a Winchester disk drive to read data from, data from the Winchester is output from multiplexer 14F as RDDOR+. Winchester drive data is also output as RDDATA+ through multiplexer 17F when the 8X300 asserts WINCHEN+. RDDATA+ is sent through the phase-locked loop, the address mark detector, and the data separator, resulting in the WNRZ+ (Winchester Non Return to Zero) signal. The WNRZ+ signal is then sent from data separator circuitry (shown on page 8 of Figure 2-6) to pins 5 and 13 of multiplexer 17F.

At the beginning of a Winchester read operation, when, as shown on page 7 of Figure 2-6, RDGATE+ (Read Gate) is low at pin 1 of gate 1E (that is, when no read operation is taking place), pin 3 of 1E is low, clearing pin 11 of one-shot 13B, causing counter 13A at pin 11 to load all 0s, and setting pin 5 of flip-flop 12A. Devices 13B, 9B, counter 13A, and flip-flop 12A form the zero detector, which is explained in the subsection, "Zero Detector Circuitry," below. The 16Z+ (16 zeros) detector flag is disabled at this time. The RDDOR+ signal from the Winchester disk drive triggers 16Z+ when it goes through zero detection circuitry, causing the multiplexer at 17F on page 10 to output Winchester data (or SMD data during an SMD read) through the NRZDATA+ line at pin 7. NRZDATA+, at pin 6 of 10C, is multiplexed

through error control circuitry and sent through deserializer 10E. Parallel data is output at pins 7 through 16 of 10E. At the rising edge of BYTREQ-, latch 9E is enabled, latching the data byte onto S0+ - S7+ (Serializer 0+ - 7+), the internal buffer bus, also called S+BUS. S0+ - S7+ data is sent to buffer circuitry, shown on page 3 of Figure 2-6, where it can be transferred to the 8X320 and read by the IWS workstation.

Buffer Transfer. A buffer transfer is set by the XFEREN+ signal from the 8X300. During a read cycle, as shown on page 3, the 8X300 selects which buffer is used for a particular operation by setting the most significant bit at counter 5C either high, for buffer A, or low, for buffer B use. If pin 11 is low, for example, buffer B, composed of RAM chips 6B and 7B, is selected to be read from or written to, and multiplexer 13E is set at pin 1. When 5C pin 11 is low, it also enables transceiver 8D at pin 19. For clarity, buffer B is described in the following description, although buffer A may be used for a transfer or storage instead.

If the XFEREN+ (Transfer Enable) signal is asserted at 11F pin 2, flip flop 11F is set at the rising edge of BYTEREQ- (Byte Request), sending output pins 5 and 9 high and effectively starting a buffer operation cycle. During a read operation, READGATE+ is asserted at pin 10 of gate 11C, outputting a high DMAWR+ signal at pin 8, and latching transceiver 8D low.

When 8D is latched low, data flows from transceiver side A to side B, or from the S+ bus to the buffer. A low DMAWR+ signal then enables data to be latched onto the S+ bus. When 11F pin 9 goes high at the rising edge of BYTEREQ- to start a read cycle, it sends pins 3 and 14 of 13E high, and triggers one-shot 13B at pin 10. The output from 13B sends pins 5 and 10 of multiplexer 13E low for 170 nsec.

During a read operation, the pin 10 input to buffer B is high. Since 13E has been set low by counter 5C, the 170 nanosecond pulse from 13E pin 10 is transferred out through pin 7, pulsing the MEMBWR- (Memory B Write) line low and writing data from the 8D B outputs to the buffer.

The next BYTEREQ- pulse sends 11F pin 8 low, resetting 11F at pin 1 and sending 11F pin 9 low

at the next clock signal. A low pin 1 of 11F output asserts the BYTEACK- signal, which clocks latch 8E, shown on page 6 of Figure 2-6. During a write cycle, the 8X300 sends a WRGATE- signal to enable latch 8E, when clocked by BYTEACK-, to latch data from the S+ bus onto the serializer/deserializer bus.

When multiplexer 13E on page 3 outputs MEMBWR- (Memory B Write) at pin 7, it also outputs a BINCR+ (Buffer B Increment) pulse at pin 4 to buffer B counters at 6C, 8B, and 7C, setting up the counters to increment the buffer B address being written to.

After data has been written into buffer B, counter 6C is incremented at the falling edge of MCLK+. This increments the address line of the buffer so that the next available data byte can be written to a new location.

At port 3E on page 8 of Figure 2-6, the 8X300 monitors BF16+ and BF8+ (Buffer Full) signals from buffer circuitry on page 3 to set ECCEN- (Error Correction Circuitry Enable) low at the proper time. When the 8X300 issues a low ECCEN- signal from port 13G, it sets flip-flop 13C Q output pin 5 and pin 1 of 10C low (page 6). This causes multiplexer 10C to start multiplexing 32-bit ECC syndrome bytes into deserializer 10E. When syndrome bytes are loaded into the buffer, the 8X300 disables XFEREN+ and RDGATE+ signals and begins to transfer data from the buffer to the IWS workstation. This is done by first setting pin 11 of counter 5C (shown on page 3 of Figure 2-6) high. When pin 11 is set high, it disables, if buffer B has been used, transceiver 8D at pin 19. At the same time, the high input from 5C pin 11 causes gate 14E pin 11 output to go low, enabling transceiver 9D at pin 19 to shift data from buffer B onto the IV data bus.

When the WC1+ (Write Control) signal from the 8X300 goes low, data is transferred from buffer memory onto the IV Bus. Conversely, when the WC1+ signal is high, bus data from the 8X300 is written into RAM.

The 8X300 loads the address of data it wishes to obtain from buffer B into counters 8B, 6C and 7C as shown on page 3. Data is read from buffer B to the 8X320, 14 bytes at a time, until all data bytes from RAM memory have been transferred.

The IWS workstation then reads RAM buffer memory from the 8X320 in a DMA transfer.

DMA Transfer. Before performing a DMA transfer from the SMD Controller board to the IWS workstation, the 8X300 first loads counter 3F with 1000. This causes 3F MAX output pin 12 (DMADONE+) to go low, since 1000 is not the counter maximum load.

The 8X300 then outputs a high DMAEN+ signal at port 13G pin 15 on page 11 to begin a DMA transfer to the IWS workstation. As mentioned, DMADONE+ is low at 6E pin 1. When pin 6 of gate 5G (page 5) goes low to signal the IWS workstation that there is a DREQ- (DMA request), the IWS workstation acknowledges the request by enabling ACK-.

RDSTR- goes low when the IWS workstation is reading. When RDSTR- is low, 3H pin 2 is high, enabling the data contents of the 8X320 to be transferred through 1H and 2H to the IWS workstation. Together with a low ACK- signal, this sends 5E pin 6 low. Since pins 1 and 2 of 5F are high, 5E pins 1 and 2 are also high (DMAEN+ is asserted), resulting in a low at 5E pin 3, which enables counter 3F at the rising edge of 3F pin 14.

Every time the IWS workstation toggles the READSTR- signal, it increments counter 3F at A1, A2, and A3, and changes the 8X320 address. After the IWS workstation has read seven words, the counter reaches its maximum count, sending 3F pin 12 high. A high 3F pin 12 sets 6E pin 1, sending pin 2 of 6E low. When pin 2 of 6E goes low, it sends 5G pin 5 low. Output pin 6 of gate 5G thereby goes high, disabling the DREQ- signal to the IWS workstation.

Also, when MAX output pin 12 of counter 3F goes high, it asserts the DMADONE+ signal. This signal is read by the 8X300 from port 9C (see page 11) and indicates that the IWS workstation has accepted all of the 14 bytes from the serializer/deserializer circuitry.

When the IWS workstation is performing a DMA transfer, it is also reading the Main Status register, port 7Ah at 3G, shown on page 5 of Figure 2-6. When the CTL- signal from the 8X300 is set low, pins 13, 12 and 11 of gate 5F are

high. Pin 9 of gate 5E is also high, because RDSTRB- is active, sending output pin 8 of 5E low and strobing the DCI bus contents into the write register at 2E.

During a write operation, pin 12 of 5E is high because of active SELW- and CTL- signals. Since WRSTR- is also asserted, input pin 13 of 5E is set high as well. The resulting low at pin 11 of 5E clocks the write register, 2E.

Main Status Register Read. When the IWS workstation reads the Main Status register, it sets CTL- and SELW- low. The resulting output of 1E to pin 9 of 6G is high. An asserted RDSTR- is gated through 6G to enable the Main Status register at 3G and output port 7Ah contents onto the DCI bus. Pin 8 of 6G is set low when RDSTR- is disasserted, clearing the Main Status register at pin 1.

Main Status Register Write. During a write operation to the Main Status register, WRSTR- goes low, setting 5G pin 13 high. The RDSTR- signal is inactive, setting pin 2 of 3H low and causing data to be transferred from the DCI bus to the 8X320. Whenever the 8X320 is written to or read from, the Main Status register is cleared. Whenever RDSTR- or WRTSTR- is enabled, pins 11 and 12 of 5G are low. When pin 11 of 5G is low and the SELW- is asserted, the controller is selected to be written to, sending pin 1 of 5G high.

At the end of a read transfer, ECCEN- goes low, setting 13C. When BYTEREQ- is active, 13C pin 5 goes low and selects the A side of multiplexer 10C. To read ECC (Error Checking and Correction) generator content, 10C is switched to A, and 12D pin 11 is set to 10C pin 14. Pin 6 of 10D goes to 10C pin 5 and is output through pin 7, sending the syndrome byte out at pin 7. The syndrome byte is then shifted to 10E.

At the end of a data transfer, after reading 512 data bytes and four ECC bytes, the 8X300 enables ECCEN-, sending pin 6 of 13C high and pin 5 of 13C low. A low pin 5 selects side A. When side A is selected, pin 12 goes low, setting pin 11 of 12D low and disabling the RDGATE- signal. The 8X300 then checks RAM to see if the proper head and cylinder section have been read, and to see

if the syndrome bytes are all zero. An error has occurred if all syndrome bytes are not zero.

SMD Read Operation

In an SMD read operation, the 8X300 first selects a drive and outputs a unit select bit (USEL1 or USEL0) through 12G (shown on page 11 of Figure 2-6). The 8X300 then raises USTAG to gate the USEL signal to the drives. At this time, the 8X300 checks all SMD drive status signals. It does this by asserting the CTL2RD- (Control 2 Read) signal, which enables drivers 9G and 9H, shown on page 8, at pin 4. When these drivers are enabled, status signals, such URDY, FLT, and IDX (Unit Ready, Fault, and Index), can be read by the 8X300 on the IV BUS. After reading unit status, the 8X300 tries to do a seek to the proper cylinder to select the head. It does this by using BUS0 and BUS9 bits to send the cylinder address. Then it strobes TAG1 high. TAG1 is high from one to five microseconds. When the cylinder is found, the 8X300 sets BUS0 and BUS3, and strobes TAG2 to select the proper head. To signal the SMD that a read operation is in progress, the 8X300 sets BUS1 high and strobes TAG3. More information on drive selection and operation is in Table 2-13, "Tag/Bus Lines."

SMD RDDATA is input and multiplexed through 14F and clocked by 16F, at the falling edge of SMDCLK+. NRZDATA+ is then sent through serializing/deserializing circuitry to the data buffer, as described in the "Buffer Transfer" subsection. At the end of the buffer transfer, after the identification field has been read, the 8X300 scans the buffer to make sure that the correct cylinder and head were read. If the operation was successful, the 8X300 asserts BUS1, disables BUS0, and begins a DMA transfer.

SMD and Winchester Disk Drive Write Operation

A write operation to an SMD or Winchester disk drive is generally the same as a read operation, with the exception of data flow. When the IWS workstation wants to write to an SMD or Winchester drive, it first transfers data, eight bytes at a time, into buffer B, in a DMA transfer operation. Then the IWS workstation issues a read command to the controller to obtain the

sector to be written to, and the identification field number. This information is compared by the IWS workstation and, if found to be correct, the 8X330 enables WWRGATE- as shown on page 4 of Figure 2-6, at pin 19 of 8G. At the rising edge of the BYTEREQ-, pin 5 of flip-flop 11F pin 5 goes high (page 3), which, at the falling edge of MCLK, sets pin 9 of 11F high, beginning a buffer transfer. The buffer transfer sequence is identical to that of a read operation, except that pin 10 of 11C (RDGATE+) is low, causing pin 1 of 8D to go low and allowing data to flow from side B to A and onto the S+BUS. Write data is clocked through transceiver 8E by the BYTEACK- signal, and, since WRGATE- enables 8E at pin 1, is deserialized at 10E. The write data is then shifted out of the deserializer at 10E on its pin 17 (Serial Out) line, through pin 9 of multiplexer 10C as WRDATA+, and sent to pin 2 of flip-flop 16F on page 10, for an SMD write, and pin 4 of shift register 15B, on page 9, for a Winchester write.

SMD Write. WRDATA+ sent from the deserializer to flip-flop 16F is sync-clocked at the falling edge of the SMD write clock and output through drivers 14G and 15G to storage module drives as WDD0 through WDD3.

Winchester Write. The AND/OR gate at 15C examines the outputs of shift register 15B and combines them with WOSC- (Write Oscillator) and WOSC2X+. Pin 8 of 15C generates MFM data from these inputs and sends the data to pins 2 and 12 of 17B. The AND/OR gates at 16C and 17C examine a wider pattern of the bits shifted out of 15B; they form a history of bit patterns to determine when write precompensation can be applied. When pin 8 of 17C is low, the data bit is to be written early. If pin 8 is 16C is low, the data bit is to be written late. If pins 8 of both 16C and 17C are high, the data is to be written without write precompensation. The MFM encoded data generated by 15C and applied to gate 17B is sent to pin 2 of delay line 15A. The three outputs of 15A are spaced in time at 12 nsec intervals. Pin 3 of 15A represents a write delay 12 nsec before the nominal, and pin 10 represents a write delay of 12 nsec after the nominal. The three outputs of 15A are applied to the inputs of AND/OR gate 16B, along with inverted and noninverted outputs of AND/OR gates 16C and 17C. Pin 8 of 16B generates the MFM precompen-

sated data bits, the bits propagate through gate 17B pin 4 as WDAT1+, and are sent to the Winchester drive through driver 4H as WWD0 through WWD3.

Additional SMD Controller Board Circuitry Descriptions

Zero Detection Circuitry

As shown on page 10 of Figure 2-6, MFM data from the Winchester disk drive enters through any one of the four WRDD0+-WRDD3- channels and is output from the RS-422 receiver 17G. Input control pins 2 and 14 of multiplexer 14F select the appropriate channel (A or B), and MFM data (RDDOR+) is output through 14F pin 7 to trigger one-shot 13B (pin 2), as shown on page 7. The time constant of 13A, a clock counter, is set by R24 and C67 to time out at an interval slightly longer than the 230 nanosecond bit-cell time of the Winchester disk data. When a series of zeros are read from the SMD or Winchester disk, 13A does not have the opportunity to time out. The pin 13 output of 13B holds the CD (Count Down) input of 13A high, and MFM data from pin 4 of 13B causes 13A to count up until 16 zeros occur. When 13A detects 16 zeros, it triggers output pin 12, resetting flip-flop 12A. When reset, 12A pin 8 goes high, enabling the 16Z+ (16 Zeros Detected) signal, which remains high until the RDGATE- signal is reset. A high 12A pin 8 also resets 12A output pin 5, causing the GAPDET- signal to go low. A low GAPDET- is then read by the 8X300 as a status bit (Gap Detect), to ensure that it is reading a valid gap before a sector and not just a long field of zeros.

Since it takes some time for the VFO to lock onto the MFM data, the presence of 16 MFM zeros is sufficient to start the lockup process. Since 16 bytes of zeros are present in a gap (and two bytes are used to get the 16Z+ flag), another 10-byte interval (about 20.0 nanoseconds) is allowed to ensure that the VFO has enough time to lock onto the incoming data stream. The 8X300 monitors GAPDET-, while a timer in the 8X300 microprogram counts the 10 bytes of zeros that should appear if the gap is valid.

If one-shot 13B detects an MFM one bit in the data stream, it will time out, with its high pin 4 output clearing pin 14 of counter 13A. The low

pin 6 output of 13B will then set GAPDET- high at 12A pin 5 and pin 10 of 15A. If GAPDET+ goes high, the 8X300 takes RDGATE+ low at pin 1 of gate 1E, which reloads counter 13A with all zeros, clears one-shot 13B, and sets the gap detector flip-flop at 12A output pin 5 high. If GAPDET+ remains low for the 10-byte interval count, the 8X300 asserts 80Z+ (80 Zeros Detected) at pin 10 of 8G (page 4).

Serializing/Deserializing Circuitry

When data is read from drives during an SMD or Winchester read cycle, the ECCEN- input at 13C pin 2 is deasserted, Q output pin 5 of 13C is set, and the multiplexer 10C selects side B of the input. When flip-flop 13C is clocked by the BYTEREQ- signal, NRZ data is output through 10C pin 7 to deserializer 10E pin 11.

During a read operation, the RDGATE- (Read Gate) signal is low at pins 2 and 3 of 10E, shifting read data out through output pins 00 through 07. Data is clocked into 10E by the BITCLK- signal from the SMD or Winchester drives.

NRZ data is then shifted right in shift register 10E. The shifted outputs of the 10E are tied to the input of comparator 11E for detection of the ID Sync Byte FEh or Data Sync Byte F8h. In ID Sync Byte detection, pins 9 and 12 of 11E (IDFIELD+) are set by the 8X300 and reset in the case of a Data Field Sync Byte. The detected sync pattern 11111111 or 11111100 enables pin 19 low, and the condition is latched by pin 9 of flip-flop 13C. WSYNC- goes low when a sync pattern is detected, acting as a status bit connected to the input port of 9C pin 17 and read by the 8X300. The sync pattern is 11111111 instead of 11111110 for the ID Sync Byte, because there is a one-bit delay in enabling counter 12C. The pattern is thus formed with the last bit of A1 and the first seven bits of FEh or F8h. When the sync byte is detected, pin 3 of 6G goes high, enabling counter 12C. If WSYNC- does not go low approximately three bytes after GAPDET- goes high, the incoming MFM data is not an address mark. If this is the case, the 8X300 will lower RDGATE+ and start the zero detect operation again.

Phase Detection Circuitry

As shown on page 7 of the SMD Controller board schematic, three flip-flops form the phase-locked loop phase detector: the phase detector enable flip-flop at 9B, and two flip-flops at 10B. An MFM data bit from pin 9 of multiplexer 17F on page 10 clocks pin 3 of flip-flop 9B, which sets it, thus enabling 10B, the two phase detector flip-flops. At 10B, output pins 8 and 9 are the data phase comparison signals. These two signals are compared with the VFO phase comparison signals, at pins 5 and 6.

The leading edge of the MFM data pulse enables the data and phase comparison flip-flops. At the same time, the data pulse is sent to the pin 1 input of delay line 11A, where it is delayed 100 nsec. The delayed data pulse at pin 12 of the delay line is sent to the VFO as RDDAT1+, and also clocks pin 11 of the data phase comparison flip-flop (10B). The VFO phase comparison flip-flop at 10B is clocked at pin 11 by the VFO2X- (VFO Frequency Times 2) line.

The two 10B flip-flops should be clocked at the same time. If an error exists between the frequency of the data and VFO, however, one flip-flop will be set before the other one. Pin 11, for example, when clocked before pin 3, indicates that VFO frequency is too slow.

The two complementary outputs of the 10B flip-flops are sent to a charge pump to change VFO frequency if it is incorrect. Once both flip-flops are set, the high levels at input pins 9 and 10 of gate 9A cause, through pin 13 of gate 9B, phase detector flip-flops to be reset.

Charge Pump and VFO Oscillator

The four phase comparison signals described above at pins 8, 9, 5, and 6 of 10B on page 7 of Figure 2-6 are applied to a four-transistor error amplifier at 6A. In the example given above, if the data phase comparison flip-flop sets before the VFO phase comparison flip-flop, the VFO frequency is too slow to be in phase with incoming data. The output of the data phase comparison flip-flop at 10A pin 8 causes the PNP transistor at 13A pins 8, 9, and 10 to turn on before the the NPN transistor turns on at pins

14, 13, and 12. This increases the voltage on the cathode of varactor diode CR1 before the NPN transistor turns on. Since the PNP transistor is on for a longer time than the NPN transistor, there is a net increase in voltage at CR1. If the VFO frequency is too high, as indicated by the VFO phase comparison flip-flop setting first at 10B, pins 5 and 6, the NPN transistor turns on first, causing a net decrease of voltage at CR1.

To keep the error amplifier 6A balanced, operational amplifier 5A monitors pins 1 and 7 of 6A at its inverting input, pin 2. If the voltage at pins 1 and 7 is slightly positive, the error amplifier is unbalanced in a positive direction, requiring a negative correction. This positive voltage at input pin 2 of 5A causes output pin 1 to go low in proportion to the voltage. This, in turn, causes a lower voltage to appear (through R62 and R63) at pins 5 and 10 (the two PNP transistors). A lower voltage at pins 5 and 10 gives a slight bias to the NPN transistors, lowering the positive voltage at 6A pins 1 and 7. Conversely, if 6A output pins 1 and 7 are more negative than the grounded noninverting input of 5A, the output of 5A at pin 1 will be positive, removing negative bias from the NPN transistors.

Phase-Locked Loop

Also on page 7 of Figure 2-6 is the low-pass filter for the phase-locked loop, comprised of C57, C58, C59, R12, and R13. CR1, as explained above, is a varactor diode, and acts as the main variable frequency control element, changing capacitance as the voltage from the error amplifier 6A varies, and adjusting frequency of the VFO (Q2). Output from the Collpitts oscillator emitter goes to pin 1 of gate 9A. 9A output is sent through a timing network composed of inductor L2, C66, and R29. The timing network provides proper phase shift for the oscillator.

The VFO is synchronized with the incoming MFM data stream as follows: The 16Z+ flag from pin 8 of flip-flop 12A is sent to the 1D input of shift register 12B, and also to pin 10 of exclusive-OR gate 11B. The shift register is clocked by the MFM data stream from pin 9 of 17F, RDDAT+. When the VFO is locked to the 8.68-MHz crystal

oscillator frequency (no gap is detected), pin 8 of 11B stays high at pin 2 of 9A, keeping the VFO turned on. When the 16Z+ flag goes high, pin 8 of 11B goes low for four bit-intervals, sending 9A pin 3 high, and breaking the VFO feedback loop, turning the VFO off. VFO output is sent to the data separator as VFO2X+ from 8A pin 8, and output line 8 from 11B is sent back to pin 4 of 5F to disable the three phase detector flip-flops during the time that the VFO is turned off. If the phase detector were not turned off with the VFO, it would generate a disproportionately large phase detection error.

Once the VFO turns off, since shift register 12B is clocked by the MFM data leading edge, pin 8 of 11B goes high four bit-intervals later, at the leading edge of the MFM data pulse. This causes the VFO to restart in phase with the data stream.

Data Separator and Address Mark Detection Circuitry

The output of the VFO, VFO2X+, is inverted at pin 8 of 8A and sent to the phase detector. The 8A output is also sent to a toggle flip-flop, 15D (shown on page 8 of Figure 2-6), which divides the VFO frequency by two, to equal 4.34 MHz at output pin 5. This 4.34-MHz output signal corresponds to the rate at which data is read from or written to the Winchester disk drive. Figure 2-7, "Winchester Data Separator Timing Diagram," shows the timing relationships used in detecting the address mark.

In the MFM data stream, a 0 arrives at the boundaries of a bit cell and a 1 arrives in the middle of the bit cell. Therefore, the output at pin 5 of 15D is high in the middle of a bit cell and low at the boundaries of a bit cell.

Flip-flop 15D is enabled when the 8X300's software timer counts 80 bit-intervals and sets the 80Z+ flag at pin 10 of input/output port 8G (see page 4 of Figure 2-6). This 80Z+ flag signal is sent to pin 2 of flip-flop 9B on page 7, where it is clocked by the 120-nsec delayed MFM data pulse, RDDLY+ (Read Delay), and sent to 15D on page 8.

When enabled by 80Z-, flip-flop 15D outputs pin 5 to the pin 12 15D input. Pin 11 is clocked by the delayed MFM data pulse RDDLY1+, so that if

pin 12 is high when pin 11 is clocked, a high appears at the pin 9 Q output. A high at pin 9 means that the arriving data bit appeared in the middle of a bit cell and must be a 1.

Another flip-flop, 17D, is clocked by RDDLY+ at pin 3. The D input at pin 2 of 17D is sent to the pin 6 Q output of the toggle flip-flop, 15D, causing the output of 17D pin 5 to always be a complement of 15D pin 9. Although both pin 9 of 15D and pin 5 of 17D outputs are cleared to 0 at the end of a bit cell, 17D pin 5, which receives complementary data from pin 6 of 15D, remains 0, while 15D pin 9 is clocked to a 1. This characteristic is used to detect a unique address mark or data pattern that always directly precedes an MFM ID data field. (See Figure 2-7, Winchester Data Separator Timing Diagram.)

The address mark byte is A1h (10100001 binary), and the unique aspect of this A1h byte is that, when the address mark is written, the second 0 from the right (note the underline under this bit above) is inhibited. The MFM encoding rule states that the three 0s in the last four bits of the address mark byte are written at the beginning of the bit cell, and the 1 bit is written in the middle of the final bit cell for this byte. The address mark has nothing in the bit cell that corresponds to the second 0 in the last four bits of the byte. When the address mark is read back, assuming that both the 15D and 17D flip-flops have been cleared, the 15D flip-flop clocks the first MFM 0 as a low on its pin 9 output. Since 17D's data is the complement of 15D's data, pin 5 of 17D is high. Again, at the end of the bit cell, both flip-flops are cleared. At this point, the second 0 bit in the field of three 0s was never written on the disk so nothing exists to clock flip-flops 15D and 17D. A 0 still appears at pin 9 of 15D, which is valid for this A1h byte even though the 0 never actually appeared. However, since no complementary data bit (that is, no 1) was present to clock flip-flop 17D, a 0 also appears at pin 9 of 17D. Once again, 15D and 17D are cleared at the end of the bit cell. The third MFM 0 that was written in the address mark byte clocks a 0 at pin 9 of 15D and a complement bit 1 at pin 5 of 17D.

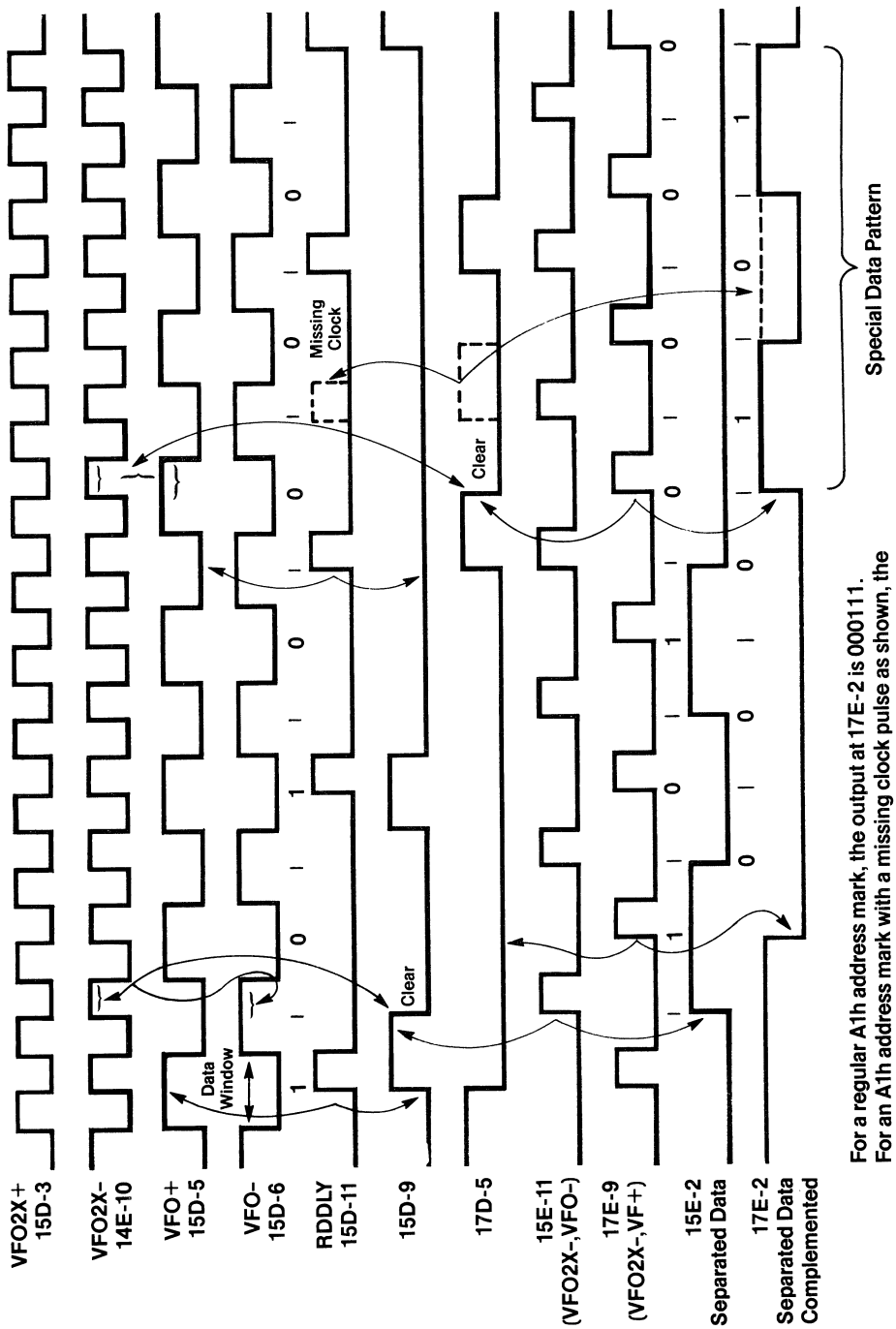


Figure 2-7. Winchester Data Separator Timing Diagram.

For the three bit-intervals above, a unique noncomplementary pattern occurs at the two flip-flop outputs. For any other byte of data read from the Winchester disks, the pattern at pin 5 of 17D is always an exact complement of pin 9 of 15D. The address mark, however, generates 000 at pin 9 of 15D and 101 at pin 5 of 17D. The outputs of both flip-flops are clocked into respective shift registers at 15E and 17E by clocks at pins 8 and 6 of gate 14E. The 000 and 101 patterns are compared at 16E. When 16E finds this special noncomplementary pattern in the data bit stream (according to its externally wired code), it sends pin 19 low, causing output pin 8 of flip-flop 17D to go high and enabling the data from the data separator to be shifted to the serializer/deserializer.

When the 8X300 first sets the 80Z+ flag, it waits for the WSYNC- signal. It is possible, at this point in the read operation, that the 80Z+ and previous 16Z+ flags were both set by a long field of MFM 0s in a data field and not by a valid intersector gap. If so, eventually either an MFM 1 or (if the whole sector is nothing but MFM 0s) an A1h address mark from the next sector will appear. Therefore, the first MFM 1 clocked through shift register 15E to its pin 19 8Q output is coupled to pin 9 of gate 17D. If an address mark is not found, pin 8 of 17D is low, resetting pin 11 of 14E (WNRZ+).

Also when the 8X300 sets the 80Z+ flag, it waits for the GAPDET- to go high, signalling that an MFM data 1 has appeared. If data coming in is address mark A1H, pin 8 of 17D goes high, enabling the MFM data to be transferred to pin 11 of 14E (WNRZ+). If the incoming data is not the address mark, pin 8 of 17D will remain low, and pin 13 of 14E will be reset. When the signal WNRZ+ is output from 14E, it is sent to pins 1 and 3 of multiplexer 17F on page 10, and output through pin 7 as NRZDATA+ when WINCHEN+ (Read Winchester Enable) is set high by the IWS workstation.

SMD I/O EXTENDER BOARD

The SMD I/O Extender board plugs into the MSS motherboard and provides communication channels between the controller board, the MSX Winchester drives, the SMD drives, and the IWS workstation. Connectors on the SMD I/O Extender board are shown in Figure 2-8, while Table 2-14 shows connector signal destinations. Data and control signals from the IWS workstation are transported through the DCI cable and enter the SMD I/O Extender board through connector J1. These signals are sent through the motherboard, via the J5 and J6 connectors, to the controller board, and then back out the motherboard to drives. Connectors P3 and P6 are internal connectors used in this system version, with P5 for Winchester and floppy disk control and status signals, and P3 for Winchester and floppy disk data.

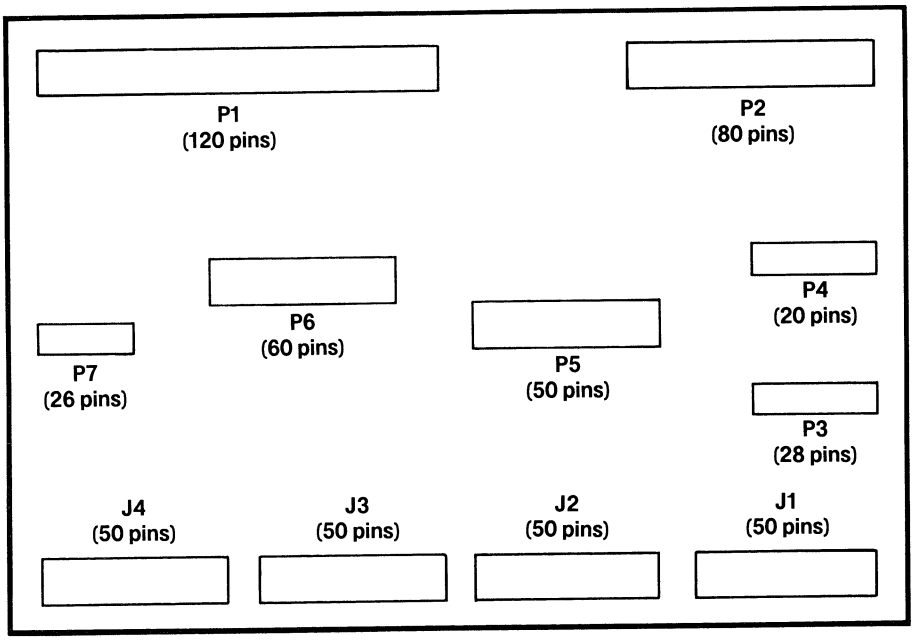


Figure 2-8. SMD I/O Extender Board Connector Locations.

MOTHERBOARD

The motherboard, contained in the MSS chassis, provides an interface between the SMD Controller board and the SMD I/O Extender board. The motherboard also receives power from the power supply, through connector P5.

Table 2-14. SMD I/O Extender Board Connectors.

Connector	To/From	Pins
J1	IWS workstation	50
J2	MSX	50
J3	SMD drives	50
J4	SMD drives	50
P1	Motherboard	120
P2	Motherboard	180
P3	Winchester disk drive	20
P5	Floppy disk drive	50

POWER SUPPLY

The MSS and MSX power supply is a switching supply that generates the following outputs:

Output	Tolerance
+5 V	±1%
-12 V	±10%
+24 V	±10%

The 5 V output is adjustable. A potentiometer is provided inside the power supply for adjustment of the 5 V output. The adjustment range is 10 percent of the full nominal output value.

> NOTE
>
> Although this is an adjustable power supply, it is not recommended that the user attempt to adjust the 5 V potentiometer.

The power supply primary input is jumpered at the factory to the local power supply, either for 110 V ac or 220 V ac. This setting can vary from 100/115 Vrms to 230 Vrms, as shown in Table 2-15. Jumpering should not be changed without contacting Convergent Technologies Field Service.

Overvoltage and overcurrent protection are provided on the +5 V, +12 V and -12 V outputs. The supply is protected to guard against failure by externally applied voltages and protected against excessive loads with an overall power-limit capability of approximately 153 W. The supply also has an overtemperature switch that turns off primary power if the heatsink temperature exceeds 80°C.

Switches

One switch, located on the front panel, controls main power to the subsystem. The switch contains an illuminated indicator, which lights when power is on.

Power Supply Wiring

The power supply is factory wired to operate with a line voltage input of either 115 V ac or 230 V ac. Figure 2-9 shows power supply wiring.

Table 2-15. Alternate AC Input Conditions.

Alternate Inputs	Primary Frequency	Primary Voltage (Vrms)		
		Low Line	Nominal	High Line
Domestic	60 Hz	105	115	130
Foreign 1	60 Hz	85	100	115
Foreign 2	50 Hz	180	230	260

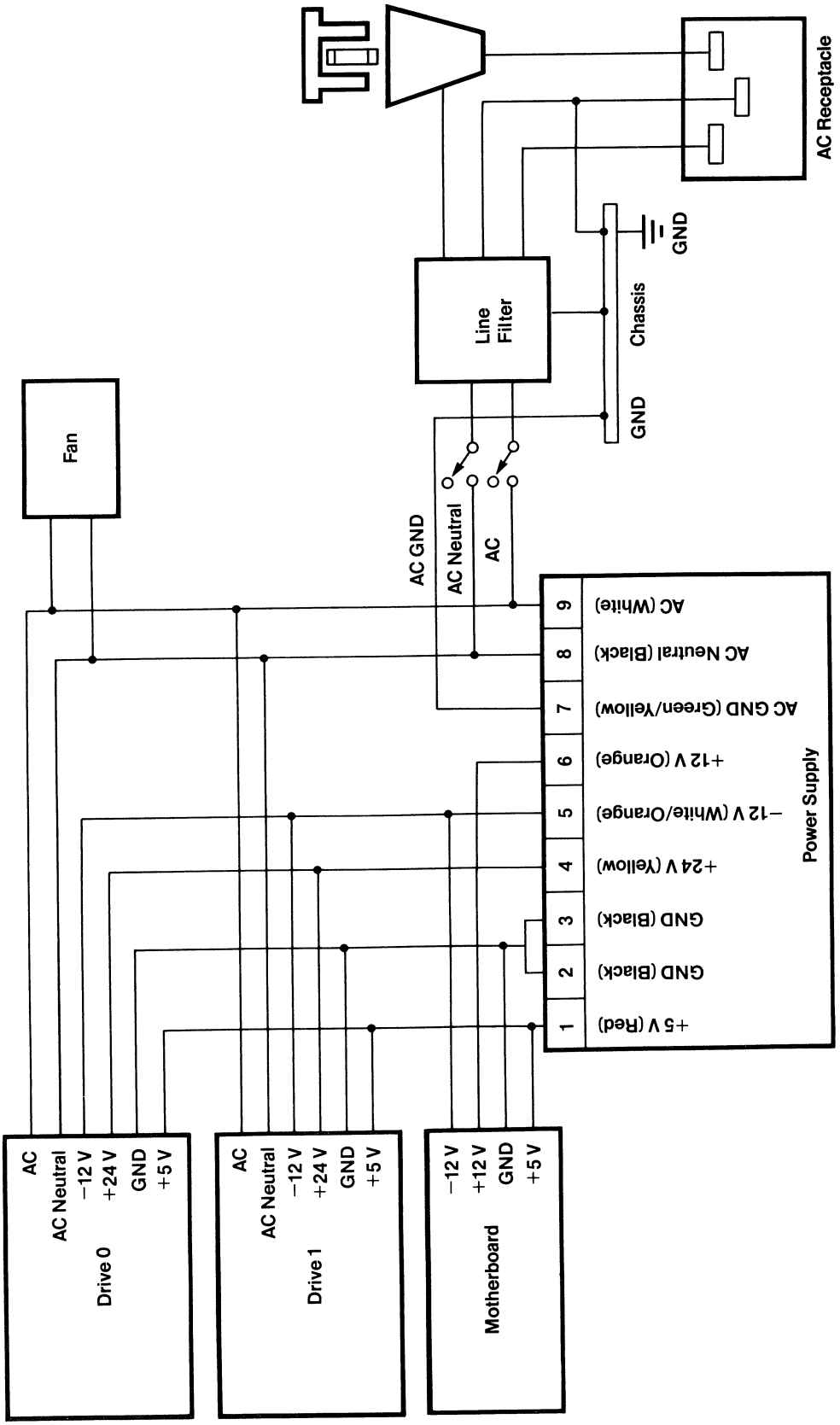


Figure 2-9. Power Supply Wiring.

3 MASS STORAGE EXPANSION

The Mass Storage Expansion (MSX) is a mass memory expansion peripheral capable of operating two Winchester disk drives of either 20M- or 40M-byte capacity. The MSX is used in conjunction with and is connected to the MSS via the MSX cable, which is a multiconductor cable similar to the cable connecting the MSS to the IWS workstation. Unlike the MSS, however, the MSX contains no controller board. Control, status, and data signals from the SMD Controller board in the MSS are sent through the MSX I/O Extender board, which also provides a channel to and from the disk drives. A Write-Protect board mounted on the MSX I/O Extender board buffers drive select signals when power is on, and contains logic to disable the disk drives if power fails. Functional blocks of the MSX are shown in Figure 3-1.

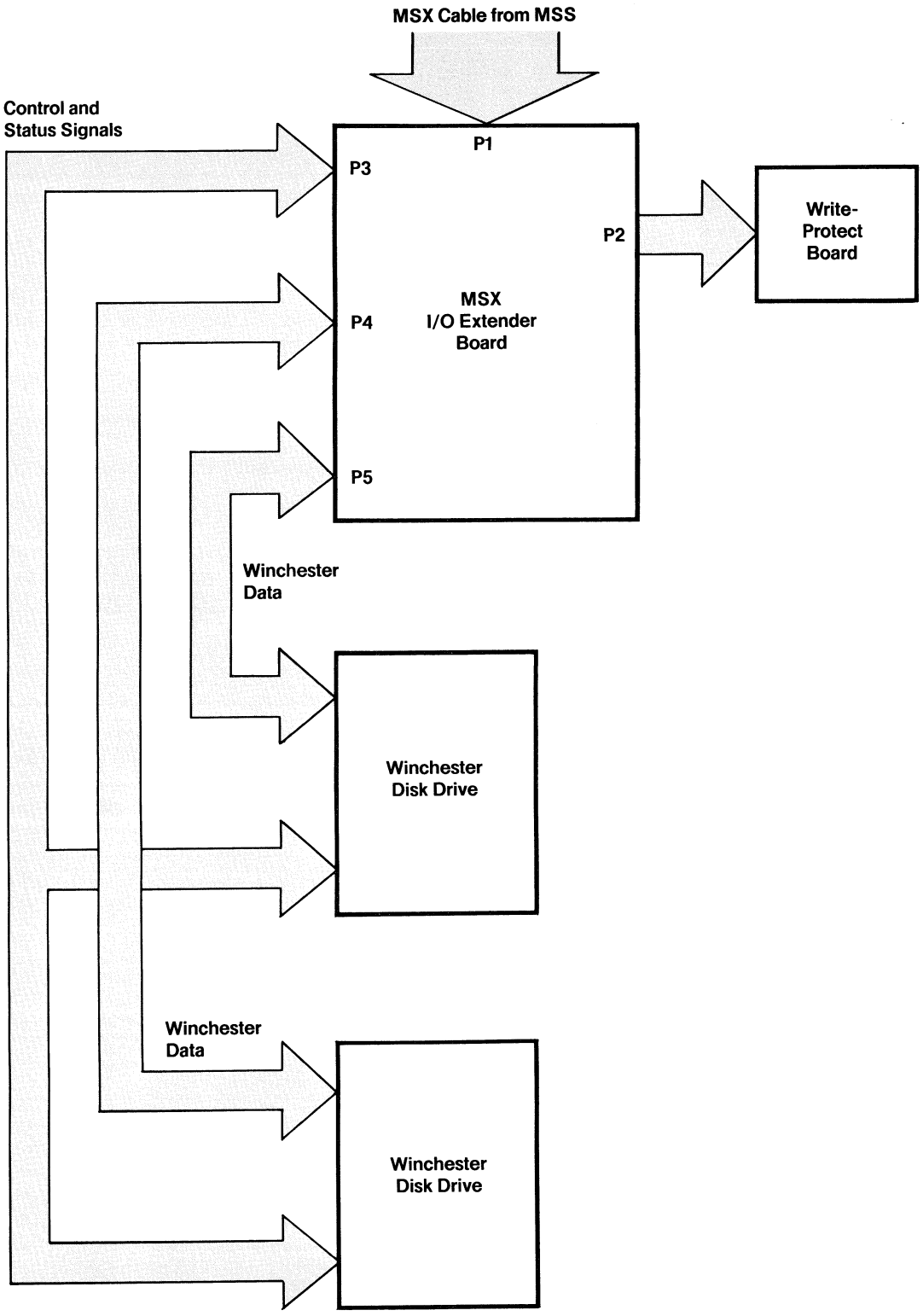


Figure 3-1. Mass Storage Expansion Block Diagram.

MSX I/O EXTENDER BOARD

The MSX I/O Extender board contains five connectors (P1 to P5) and transports signals between the SMD Controller board, located in the MSS, and the disk drives located in the MSX. Signals from the MSS enter the MSX I/O Extender board through P1. Control and status signals are sent to MSX drives through connector P3. P4 and P5 carry data signals to MSX disk drives. The Write-Protect board plugs into connector P2. Figure 3-2 shows MSX I/O Extender board connector locations.

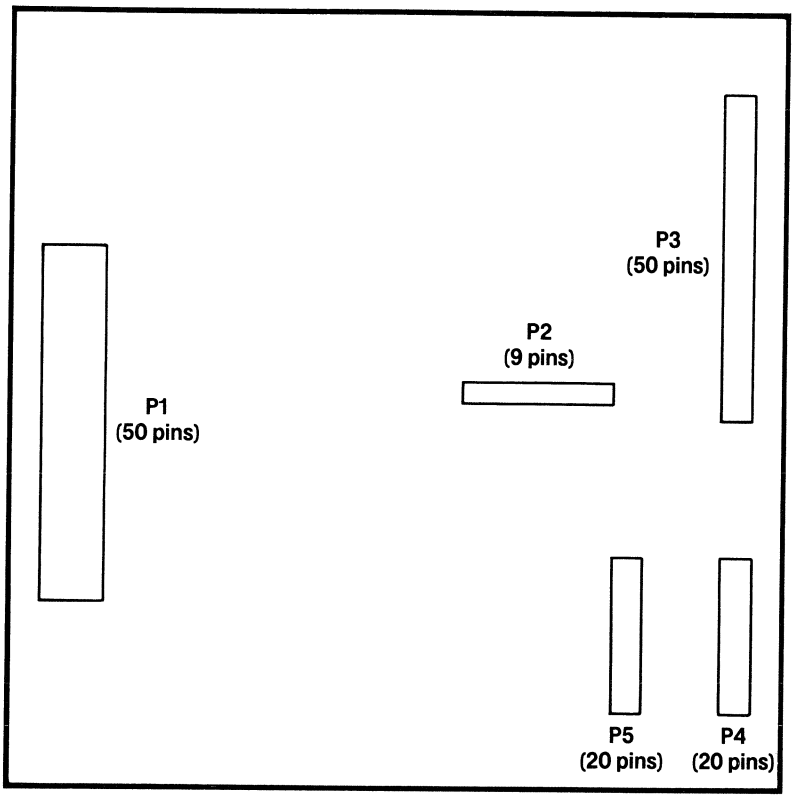


Figure 3-2. MSX I/O Extender Board Connector Locations.

WRITE-PROTECT BOARD

The Write-Protect board disables drive select signals when power drops, and buffers drive select signals from the SMD Controller board when the power is on. Figure 3-3 is the Write-Protect board schematic.

DS1- and DS2- enter the Write-Protect board through connector J5 and are buffered through U1. The DS0- signal is not used. Jumpers W1 and W2 are connected to provide proper signal termination for DS1- and DS2- at terminating resistor RP1. During operation, P6 is also jumpered, sending approximately 3.5 V to pin 9 of voltage comparator U2. U2 pin 8 is set at 2.4 V from Zener diode CR5. A high voltage at pin 9 sets pin 14 to approximately 5 V and causes pin 2 of U2 to drop, enabling the U1 buffer.

Circuitry at U2 and CR4 provides a 4-sec delay when the power is turned on, pulling pin 2 of U2 high and disabling buffer U1 while the disk drives initialize.

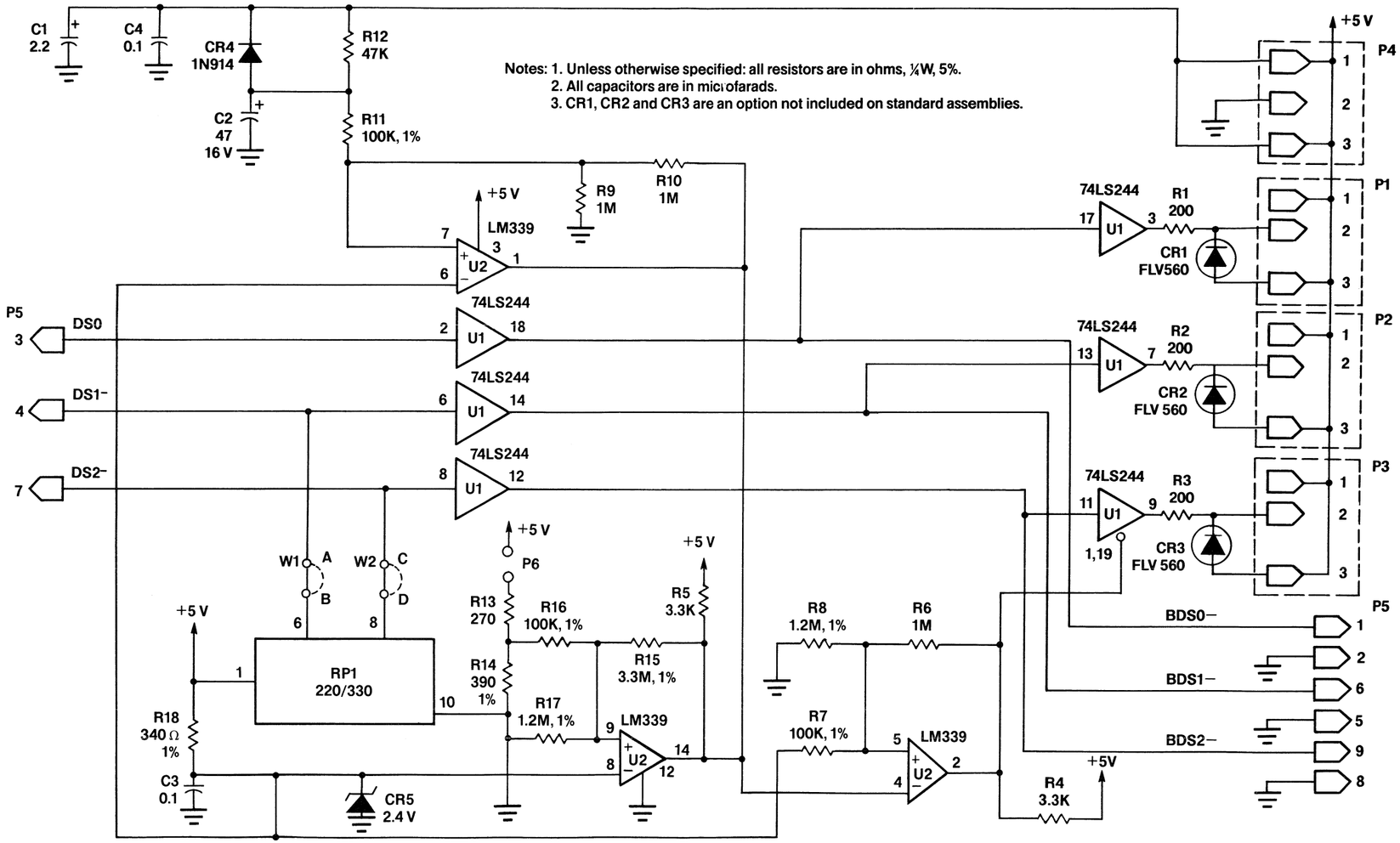


Figure 3-3. Write-Protect Board Schematic.

POWER SUPPLY

The power supply for the MSX is identical to the power supply already described in the MSS section. Refer to the "Power Supply" subsection in Section 2, "Mass Storage Subsystem," for more information.

4 ADDITIONAL IWS PERIPHERALS HARDWARE

This section describes components, and explains how to connect additional peripheral hardware to the IWS. Directions for constructing cables, connector pinouts, and parts lists are included in this section, as are switch settings for printers and plotters supported by Convergent Technologies applications software.

There are five connectors located on the rear panel of the IWS. These connectors, labeled Cluster Communications, Printer, and Channel A and Channel B, are used to link the workstation in a cluster, and are also used to link printers, plotters, and modems to the workstation. If a Communications I/O Processor board has been installed in this workstation, there will be more than five connectors on the workstation's back panel. (See the Communications I/O Processor Board for the IWS Workstation: Installation Instructions for more details.)

RS-422 CLUSTER COMMUNICATIONS INTERFACE

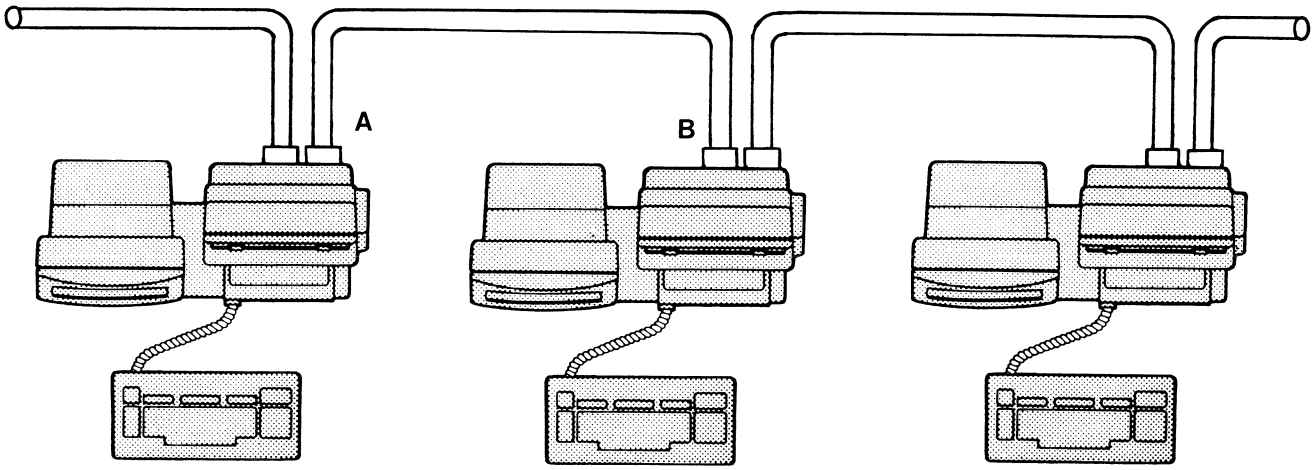
Workstations are connected to the cluster network in a daisy-chain configuration, using RS-422 cluster communications cable assemblies and the two connectors on the rear workstation panel marked "Cluster Communications." Both connectors are used in every workstation in a daisy-chain configuration, except for the two workstations located at the end of a cluster. Since only one connector is used in the end workstations, the unused connector requires a terminator plug.

This subsection contains an assembly parts list, construction directions, and pinouts for the cluster communications cable, the cluster communications terminator, and the cluster communications cable splice.

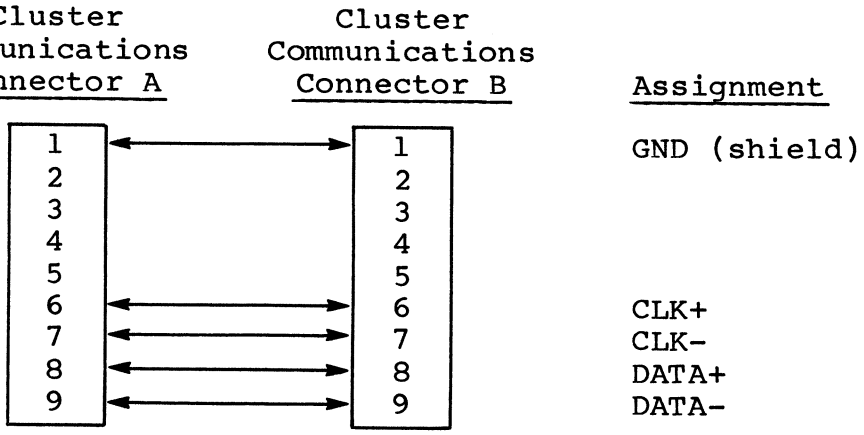
Cluster Communications Cable Assembly
(Convergent Technologies Part Number 61-00027)

This assembly connects workstations to the cluster communications line.

Connection:

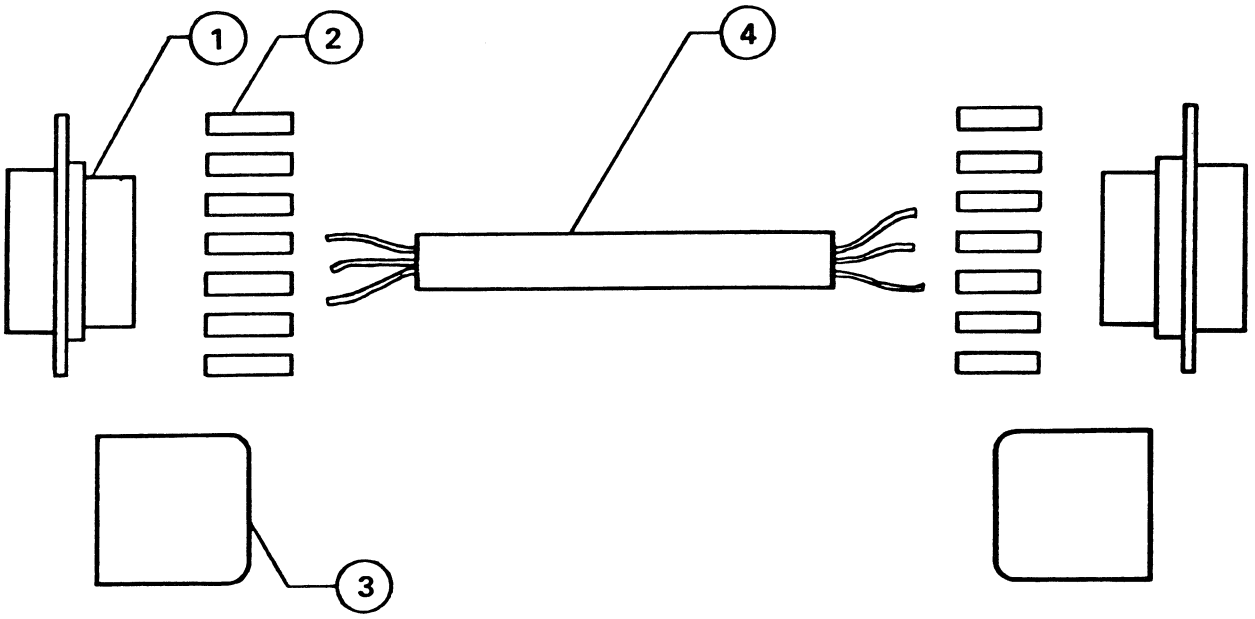


Connector Pinouts:



Cluster Communications Cable Construction

Directions:



Item	Quantity	Description
1.	2	9-pin D-type plug assemblies (male). Use Amp part number 205204-1 or the equivalent.
2.	10	Connector contacts. Use Amp part number 66507-3 or the equivalent.
3.	2	Connector shell/strain reliefs. Use Amp part number 207908-1 or the equivalent.
4.	50 ft (15.2 m)	4-conductor twisted pair shielded cable. Use Belden part number 9502 or the equivalent.

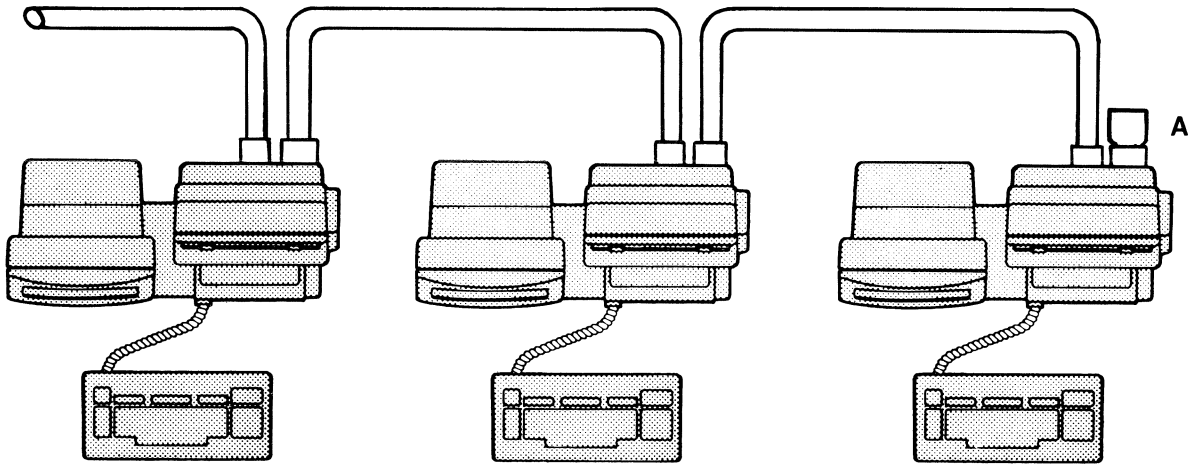
Notes: Pin 1 must be connected to the shield drain wire at both ends. Pins 6 and 7 are a twisted pair; pins 8 and 9 are also a twisted pair.

The maximum total length of a cluster communications line is 1100 ft (345 m). The minimum cable length between workstations is 25 ft (7.62 m).

Cluster Communications Terminator Assembly
(Convergent Technologies Part Number 61-00029)

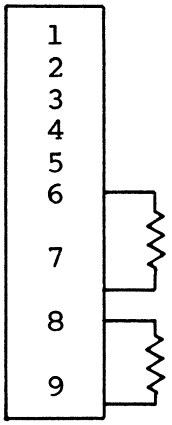
This assembly terminates the cluster communications line and ends a cluster.

Connection:



Connector Pinouts:

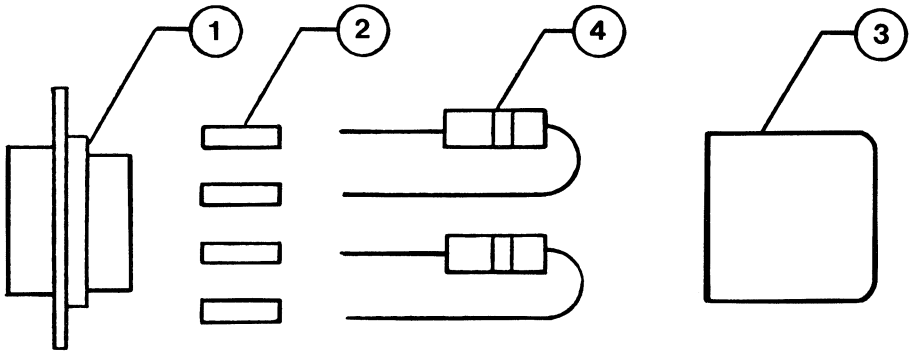
Cluster Communications Connector A



Assignment
CLK+
240-ohm, 1/4-W
CLK-
DATA+
240-ohm, 1/4-W
DATA-

Cluster Communications Terminator Construction

Directions:



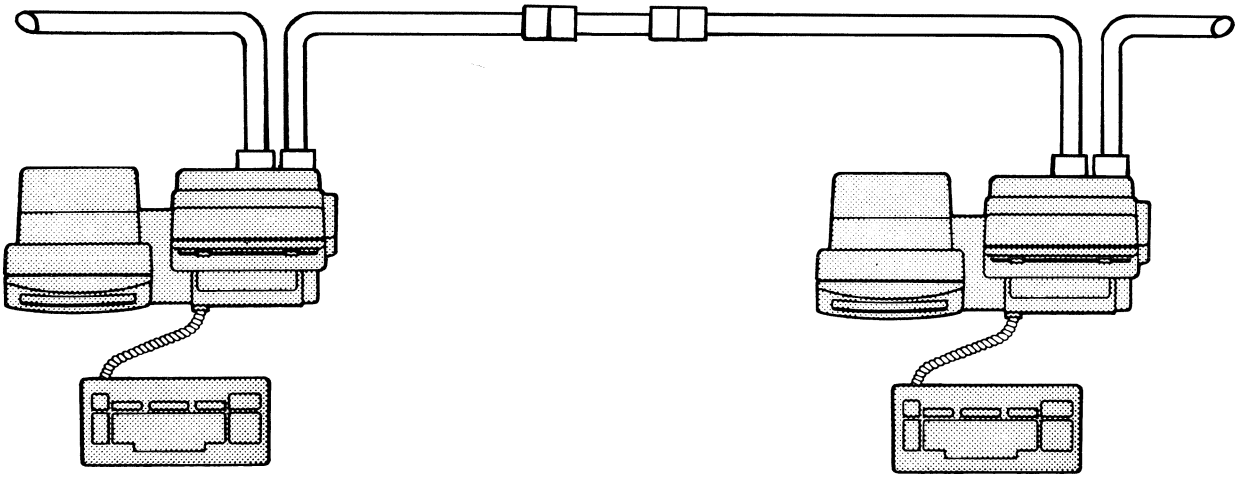
Item	Quantity	Description
1.	1	9-pin D-type plug assembly (male). Use Amp part number 205204-1 or the equivalent.
2.	4	Connector contacts. Use Amp part number 66507-3 or the equivalent.
3.	1	Connector shell. Use Amp part number 207908-1 or the equivalent.
4.	2	240-ohm, 1/4-W resistors

Note: A terminator must be installed at each end of the cluster communications line.

Cluster Communications Cable Splice Assembly

This assembly joins two cluster communications cables.

Connection:

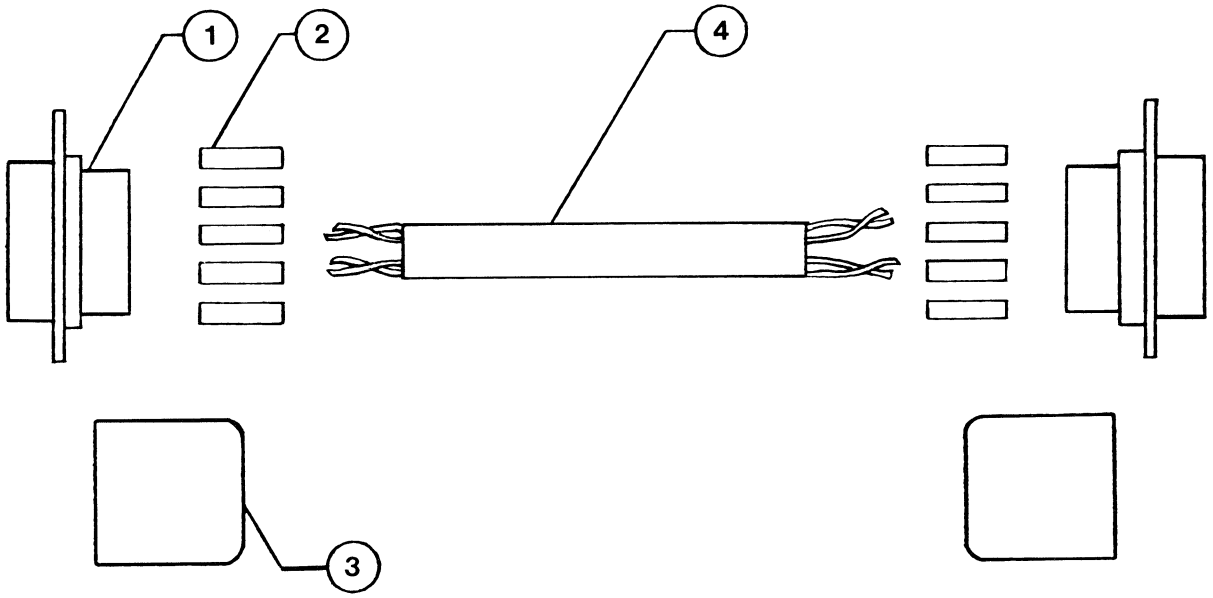


Connector Pinouts:

Cluster Communications Cable	Cluster Communications Cable	Assignment
1	1	GND (shield)
2	2	
3	3	
4	4	
5	5	
6	6	CLK+
7	7	CLK-
8	8	DATA+
9	9	DATA-

Cluster Communications Cable Splice Construction

Directions:



Item	Quantity	Description
1.	2	9-pin D-type receptacle assemblies (female). Use Amp part number 205203 or the equivalent.
2.	10	Connector contacts. Use Amp part number 66505-9 or the equivalent.
3.	2	Connector shell/strain reliefs. Use Amp part number 207908-1 or the equivalent.
4.	0.5 ft (0.15 m)	4-conductor twisted pair shielded cable. Use Belden part number 9502 or the equivalent.

Notes: Pin 1 must be connected to the shield drain wire at both ends. Pins 6 and 7 are a twisted pair; pins 8 and 9 are also a twisted pair.

The maximum total length of a cluster communications line is 600 ft (183 m).

RS-232-C SERIAL INTERFACE

Two types of RS-232-C cables, either "straight" or "crossed," may be connected to either Channel A or Channel B on the rear panel of a workstation. Channel A is configured for RS-422 use as shipped. To reconfigure Channel A, see Appendix C of the Workstation Hardware Manual.

A straight cable is used to connect data terminal equipment (DTE), such as a workstation, to data communications equipment (DCE), such as a modem.

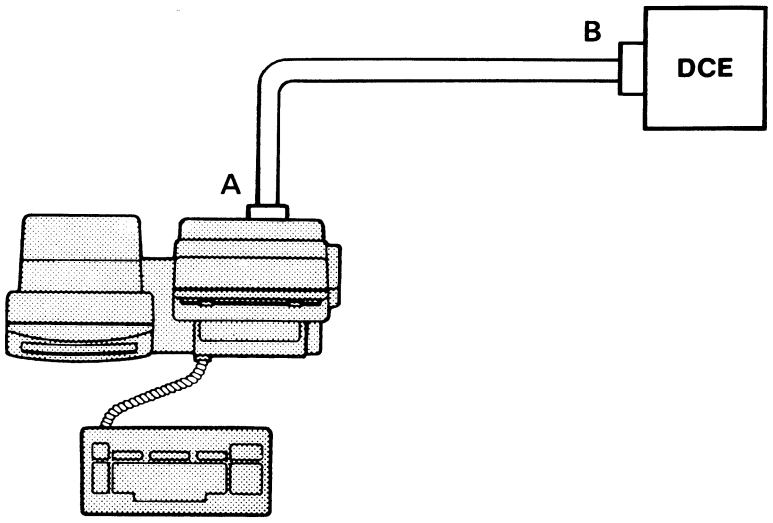
A crossed cable crosses the control and data lines, effectively presenting a "null modem" to each DTE. Such a cable is used to connect two DTEs, for example, a workstation to a terminal. A crossed cable, as described in this section, is also used to connect a workstation to a plotter. Another type of crossed cable, called the Serial Printer Interface cable, is used to connect a workstation to a printer.

This subsection describes connection and construction of the straight RS-232-C and the crossed RS-232-C cables. Connector pinouts are also included in the descriptions. The (also crossed) RS-232-C serial printer interface cable is described in a later section, "RS-232-C Serial Printer Interface." Switch settings and appropriate instructions for plotters and printers that can be connected using each type of cable are listed after the description of each cable assembly.

Straight RS-232-C Cable Assembly

This assembly connects the workstation to data communications equipment (DCE).

Connection:

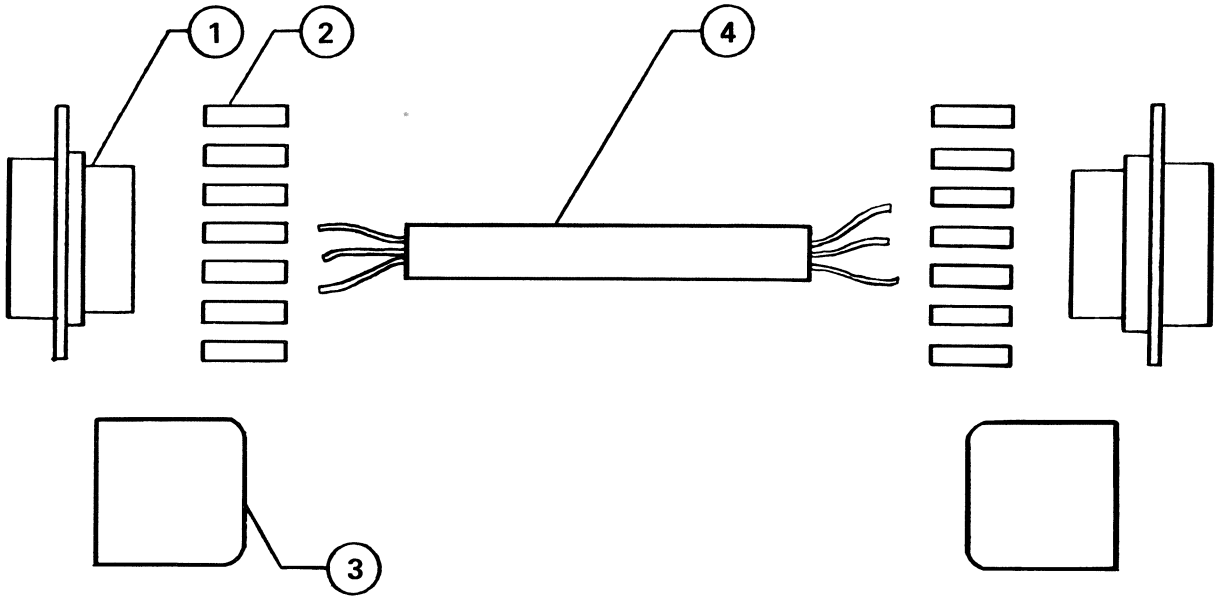


Connector Pinouts:

Workstation Channel A	DCE Channel B	Assignment
1	1	Protective Ground (shield)
2	2	Transmit Data
3	3	Receive Data
4	4	Request to Send
5	5	Clear to Send
6	6	Data Set Ready
7	7	Signal Ground (Spare Conductor)
8	8	Carrier Detect
14	14	Secondary Transmit Data
15	15	Transmit Clock
16	16	Secondary Receive Data
17	17	Receive Clock
20	20	Data Terminal Ready
22	22	Ring Indicator

Straight RS-232-C Cable Construction

Directions:



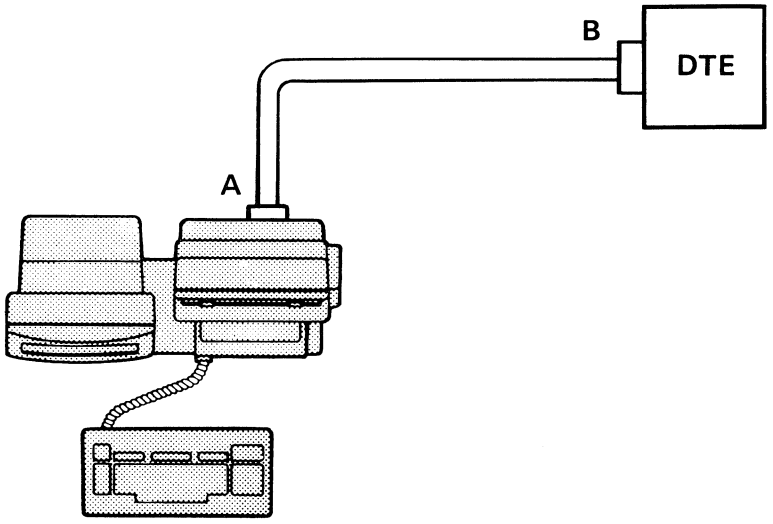
Item	Quantity	Description
1.	2	25-pin D-type plug assemblies (male). Use Amp part number 205208 or the equivalent.
2.	30	Connector contacts. Use Amp part number 66507-3 or the equivalent.
3.	2	Connector shell/strain reliefs. Use Amp part number 207908 or the equivalent.
4.	25 ft (7.62 m)	15-conductor shielded cable. Use Belden part number 9541 or the equivalent.

Notes: Pin 1 must be attached to the shield drain wire at both ends. The additional conductor in this cable must be terminated to signal ground (pin 7) at both ends. The minimum length of this cable is 25 ft (7.62 m).

Crossed RS-232-C Cable Assembly

This assembly connects the workstation to data terminal equipment such as plotters and terminals and is used for RS-232-C communications.

Connection:

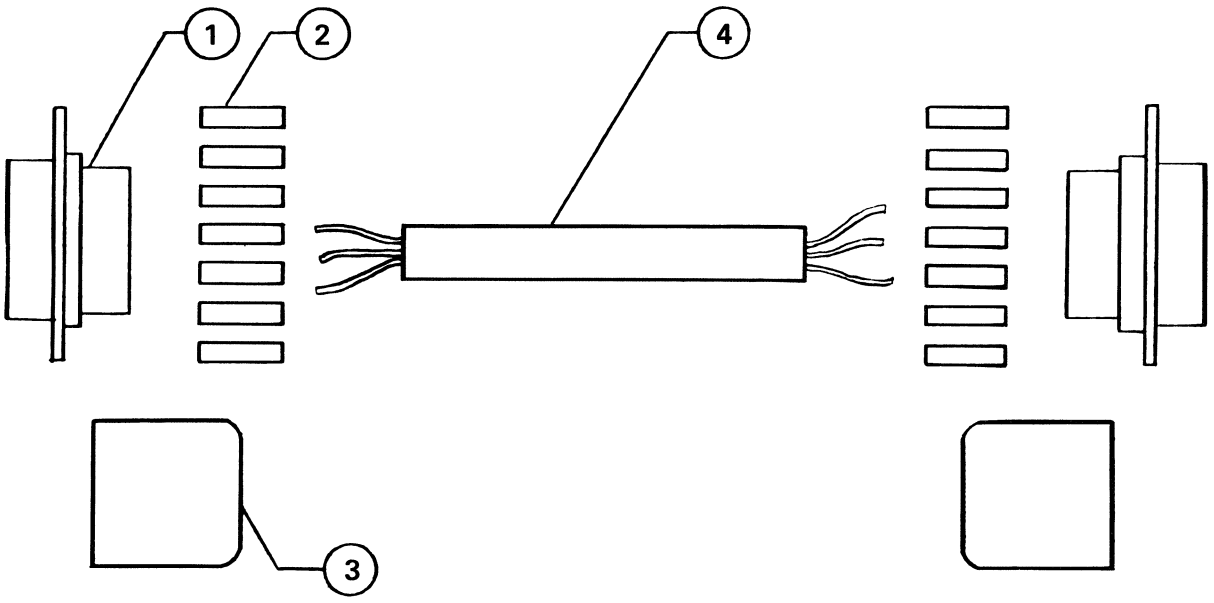


Connector Pinouts:

Assignment	Workstation Channel A	DTE Channel B	Assignment
Protective Ground (shield)	1	1	Protective Ground (shield)
Transmit Data	2	3	Receive Data
Receive Data	3	2	Transmit Data
Request to Send	4	4	Request to Send
Clear to Send	5	5	Clear to Send
Signal Ground	7	7	Signal Ground
Data Set Ready	6	6	Data Set Ready
Carrier Detect	8	8	Carrier Detect
Data Terminal Ready	20	20	Data Terminal Ready

Crossed RS-232-C Cable Construction

Directions:



Item	Quantity	Description
1.	2	25-pin D-type plug assemblies (male). Use Amp part number 205208-1 or the equivalent.
2.	18	Connector contacts. Use Amp part number 66507-3 or the equivalent.
3.	2	Connector shell/strain reliefs. Use Amp part number 207908-7 or the equivalent.
4.	25 ft (7.62 m)	3-conductor shielded cable. Use Belden part number 9533 or the equivalent.

Notes: Pin 1 must be connected to the shield drain wire at both ends. The minimum length of this cable is 25 ft (7.62 m).

PLOTTER CONFIGURATIONS

Three plotters are supported by Convergent Technologies software:

- Hewlett-Packard Model HP7470A
- Hewlett-Packard Model HP7220C
- Strobe Model 100

This subsection contains connections and switch settings required to run each of the following plotters with an IWS. These plotters are connected with the crossed RS-232-C cable described in the preceding subsection.

Plotter Switch Settings

Hewlett-Packard 7470A Plotter

This plotter uses the crossed RS-232-C cable. To use this plotter with an IWS, the switches should be set as follows:

Switch	Setting
Parity	Off (S2) Off (S1)
D/Y (Programmed On/Off)	Y
A4/US	US
Baud rate	On (B4) Off (B3) Off (B2) Off (B1)

Figure 4-1 illustrates the HP7470A plotter switch settings.

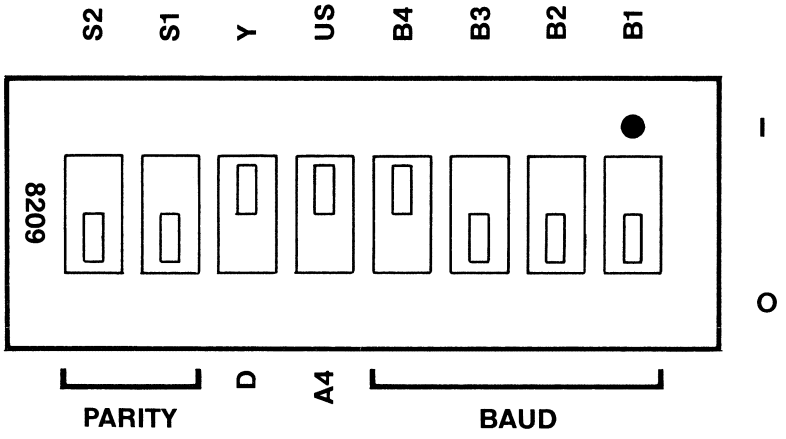


Figure 4-1. HP7470A Plotter Switch Settings.

Hewlett-Packard 7220C Plotter

This plotter uses the crossed RS-232-C cable. The cable should be connected to the MODEM connector, as shown in Figure 4-2, and the Baud rate dial should be set to 2400. The switches should be set as follows:

Switch	Setting
CONF. TEST	Off
DTR Bypass/Norm	Norm
Parity	Off
Hard Wire/Modem	Modem

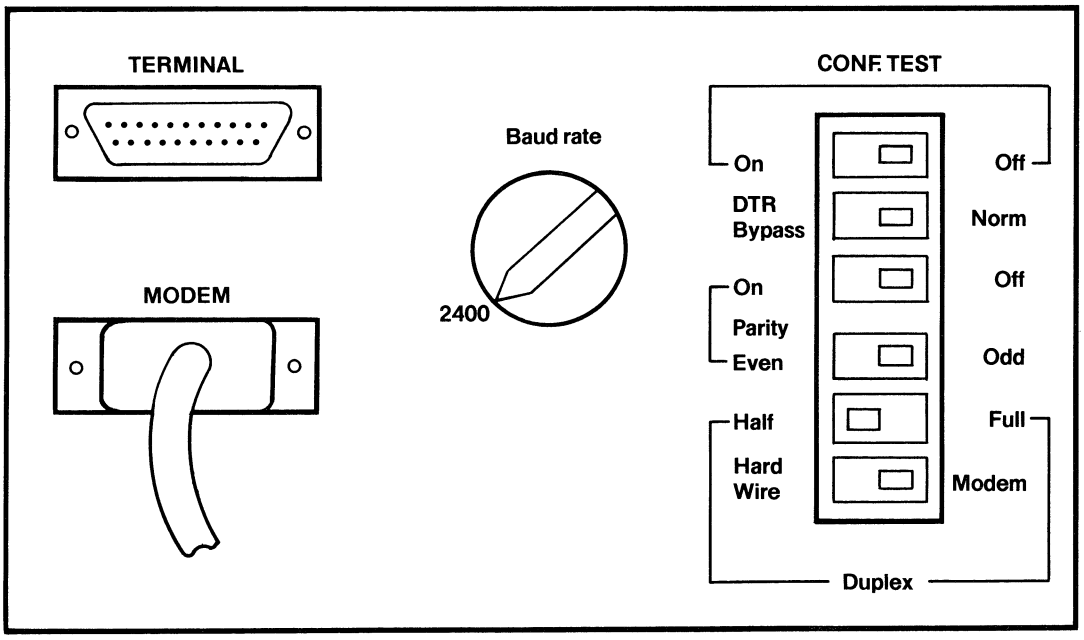


Figure 4-2. HP7220C Plotter Switch Settings.

Strobe Model 100 Plotter

This plotter uses the crossed RS-232-C cable and requires a Strobe Model RS-232-C interface attachment. The switches should be set on the interface attachment as follows:

Switch	Setting
Baud rate dial	2400 (A)
Parity	None

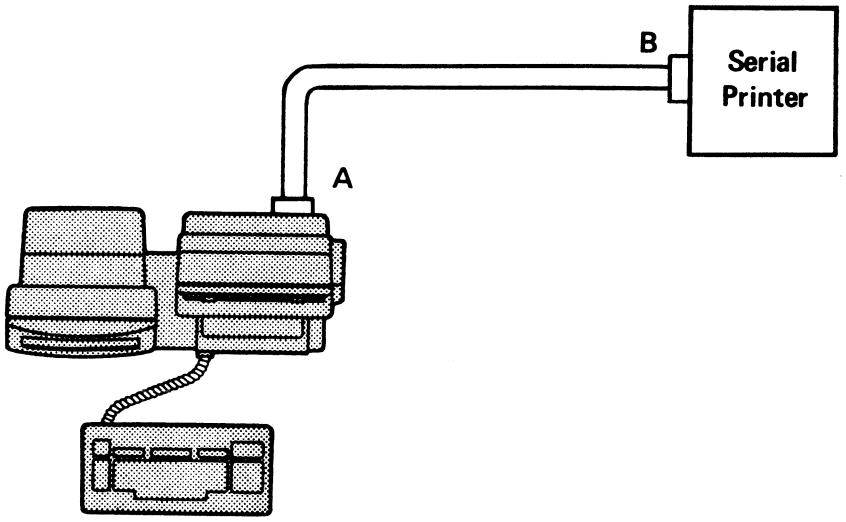
RS-232-C SERIAL PRINTER INTERFACE

A crossed RS-232-C serial printer interface cable, described in this subsection, is used to connect serial printers to the IWS workstation. A crossed cable crosses the control and data lines, effectively presenting a "null modem" to each piece of data terminal equipment (DTE).

Serial Printer Interface Cable Assembly

This assembly connects the workstation to serial printers.

Connection:



Connector Pinouts:

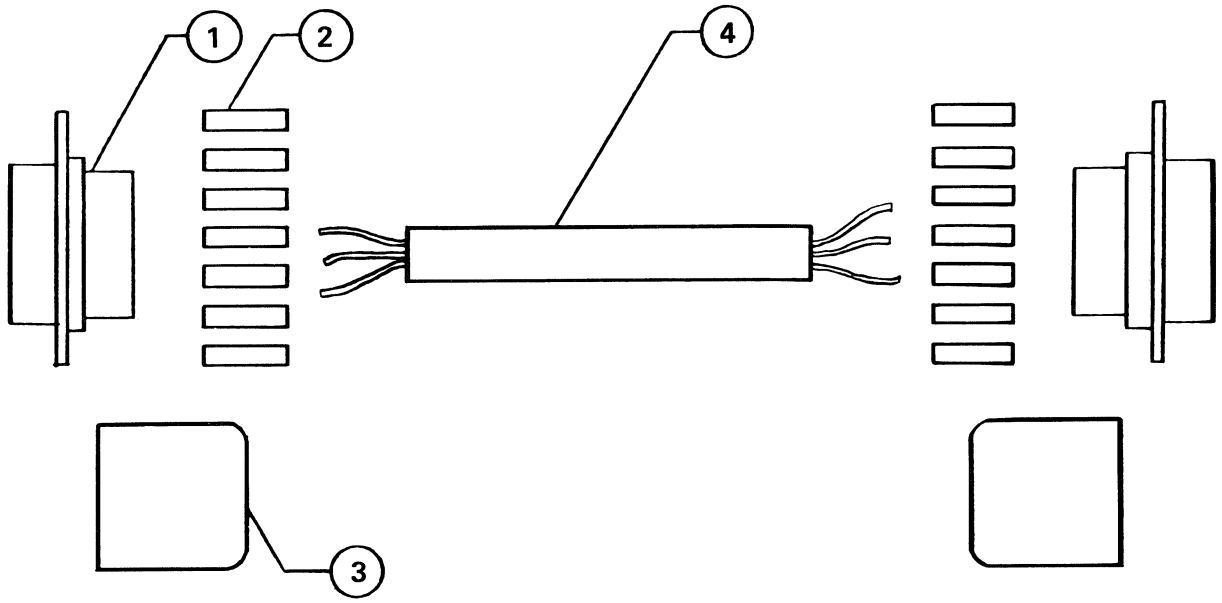
Assignment	Workstation Channel A	DTE Channel B	Assignment
Protective Ground (shield)	1	1	Protective Ground (shield)
Transmit Data	2	3	Receive Data
Receive Data	3	2	Transmit Data
Request to Send	4	4	Request to Send
Clear to Send	5	5	Clear to Send
Signal Ground	7	7	Signal Ground
Data Set Ready	6	6	Data Set Ready
Carrier Detect	8	8	Carrier Detect
Data Terminal Ready	20	20	Data Terminal Ready

CAUTION

An RS-232-C serial printer must only be connected to a workstation channel configured for RS-232-C. Channel A is configured as RS-422 from the factory. A serial printer must not be connected to Channel A unless it is reconfigured. A serial printer must also never be connected to the parallel printer connector on the workstation.

Serial Printer Interface Cable Construction

Directions:



Item	Quantity	Description
1.	2	25-pin D-type plug assemblies (male). Use AMP part number 205208-1 or the equivalent.
2.	18	Connector contacts. Use Amp part number 66507-3 or the equivalent.
3.	2	Connector shell/strain reliefs. Use Amp part number 207908-7 or the equivalent.
4.	25 ft (7.62 m)	3-conductor shielded cable. Use Belden part number 9533 or the equivalent.

Notes: Pin 1 must be connected to the shield drain wire at both ends. The minimum length of this cable is 25 ft (7.62 m); the maximum length is 50 ft.

SERIAL PRINTER CONFIGURATIONS

Qume Sprint 5 Serial Printer Cable Connection

The serial interface option for the Qume Sprint 5 serial printer does not provide the standard female 25-pin D-type cable connector mounted on the back of the printer. (This connection is, however, standard on the Qume Sprint 9 serial printer, the Diablo 630 HPRO5 printer, and the Diablo 630 SPI printer.)

Instead of providing a standard connector, the serial interface for Qume Sprint 5 is a 10-conductor cable that is hard-wired to the printer. Figure 4-3 shows the correct way to connect the wires within the cable to a male 25-pin D-type connector, which can then be plugged into either Channel A or Channel B at the rear of the workstation.

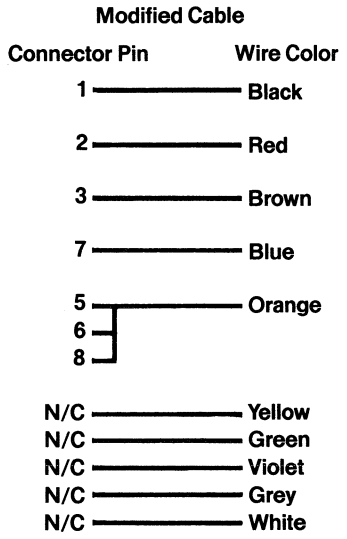


Figure 4-3. Modified Cable Connection for the Qume Sprint 5 Serial Printer.

Serial Printer Switch Settings

Qume Sprint 5 Serial Printer

The switches for a Qume Sprint 5 printer should be set as follows:

Front panel switches

Switch	Setting
Baud	1200
Duplex	Full
Parity	Even
Auto Line Feed	Off
Twintellect	Standard
Character Spacing	10
Form Length	11

Keyboard switches (if applicable)

Switch	Setting
On-line	ON

Inside switches

Switch	Setting
No Modem	HIGH (left)
Baud rate	HIGH (left)

Since the Qume Sprint 5 printer does not support XON/XOFF handshaking, the printer configuration should be set for CTS only, not both CTS and XON/XOFF. This printer must be connected using the serial printer interface cable. Figure 4-4 shows the Sprint 5 printer switches.

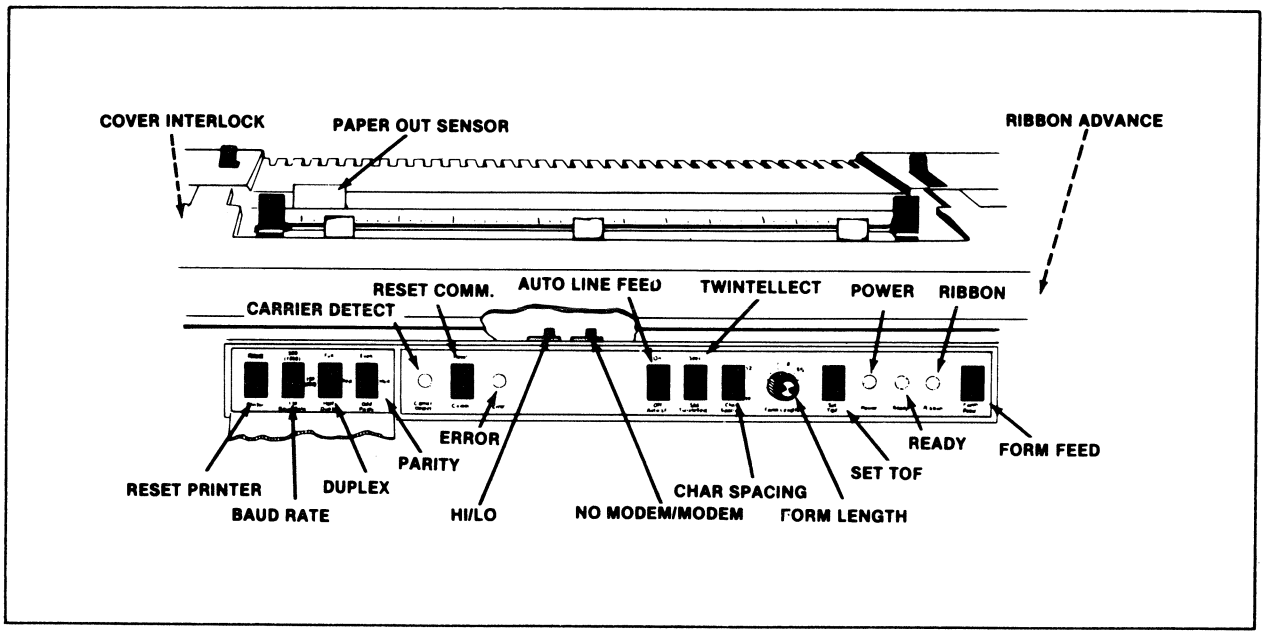


Figure 4-4. Qume Sprint 5 Serial Printer Switches.

Qume Sprint 9 Serial Printer

If a Qume Sprint 9 serial printer is to be used, the switches should be set as follows:

Front panel switches

Switch	Setting
Linespace	Set the number of lines to 3, 6, or 8 lines per inch.
Pitch	Set pitch as 10, 12, or 15 characters per inch.
WPS	Turn WPS off.
TOF	Set top of form as needed.
Form length	Set form length as needed.
Form feed	Turn form feed on.
Pause	Turn pause off.

Internal Front Panel Switches

Switch	Setting
Even parity	Turn off (A8)
Even parity	Turn off (A7)
No modem	Turn on (A6)
Full duplex	Turn off (A5)
1200 baud	Turn on (A3)
1200 baud	Turn off (A2)
1200 baud	Turn off (A1)
XON/XOFF	Turn off (B8)
XON/XOFF	Turn off (B7)
Auto CR/LF	Turn off (B6)
Auto LF	Turn off (B5)
Stop print on paper out	Turn off (B4)
Twintellect	Turn off (B3) (B2 is not used)
Automatic bidirectional printing	Turn off (B1)

Figure 4-5 shows the Qume Sprint 9 serial printer switches.

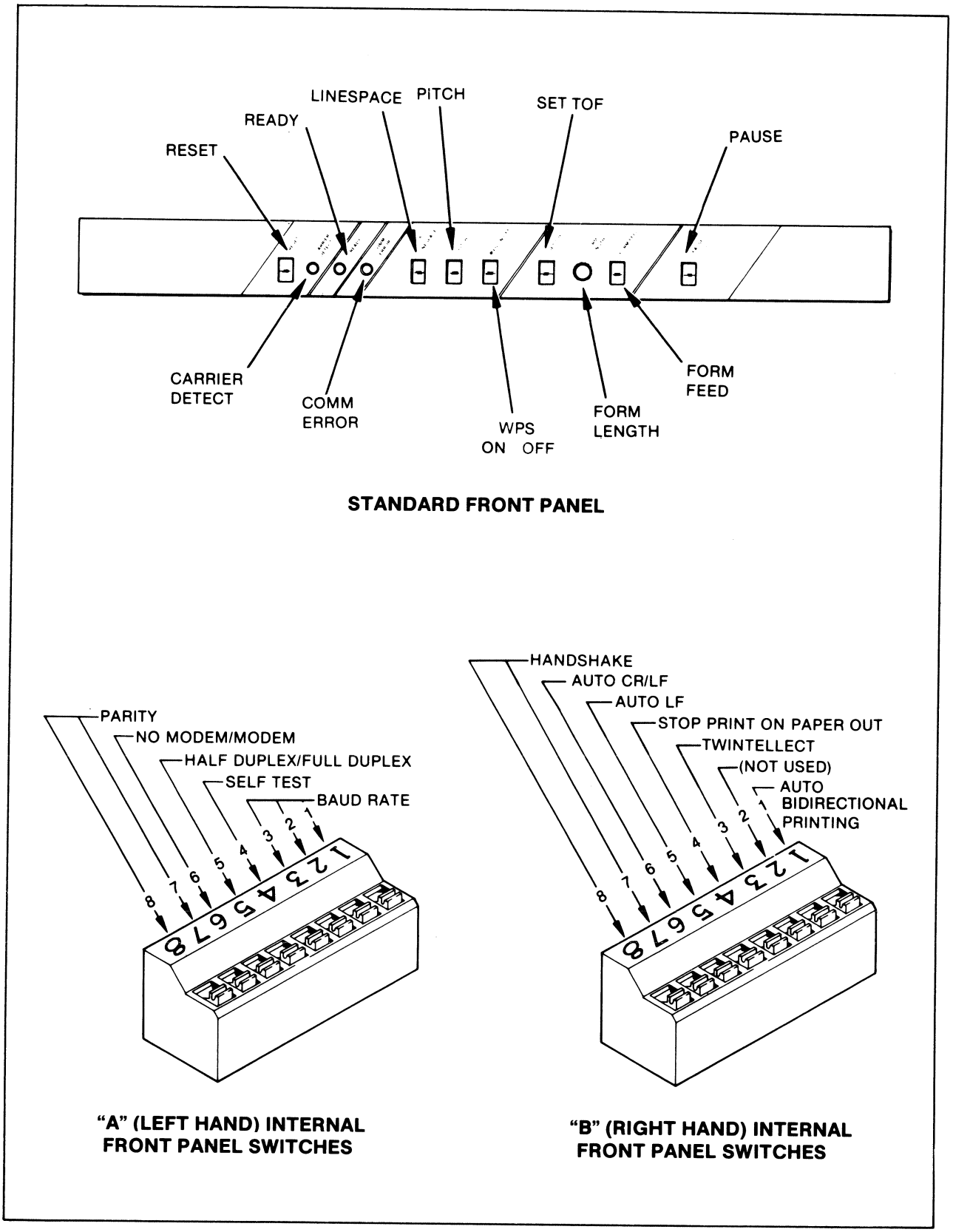


Figure 4-5. Qume Sprint 9 Serial Printer Switches.

Diablo 630 SPI Serial Printer

For a Diablo 630 SPI serial printer, the switches should be set as follows:

Switch	Setting
Print wheel	Turn 1 off (plastic).
Spacing	Turn 2 and 3 off (10-pitch).
Protocol	Turn 4 off (DC1-DC3).
Baud	Turn 5 on (1200 baud).
Parity	Turn 6 and 7 on (even parity).
Self-test	Turn 8 off.

Figure 4-6 shows the switches of the Diablo 630 SPI printer.

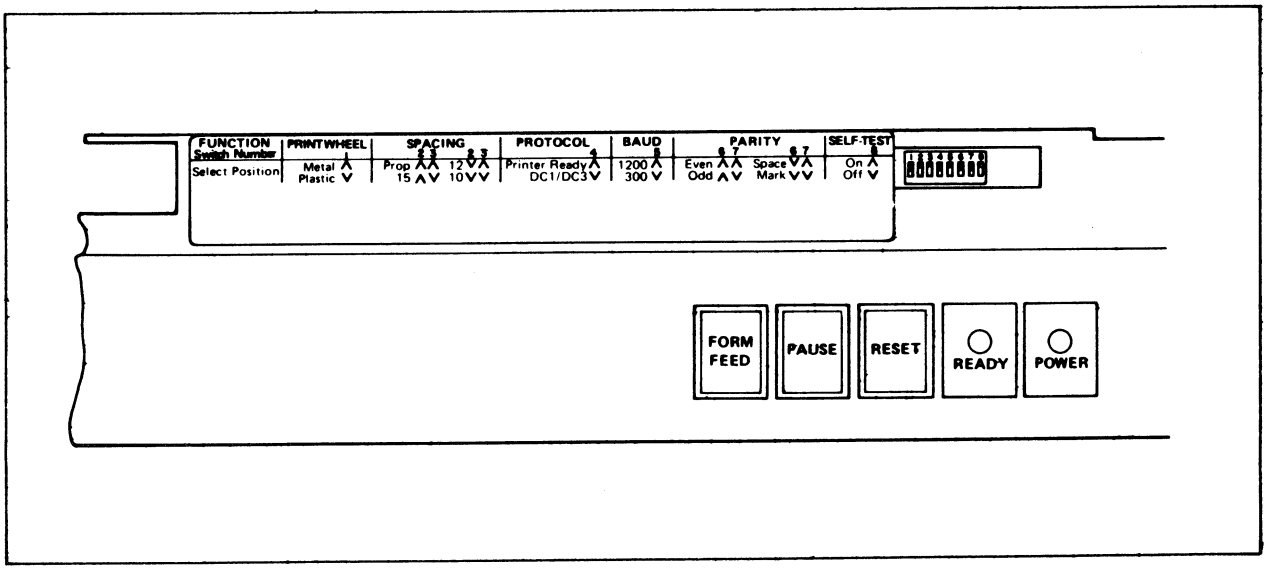


Figure 4-6. Diablo 630 SPI Serial Printer Switches.

Diablo 630 HPRO5 Serial Printer

When this printer is used, the Print Wheel Select should match the type of print wheel on the printer. Switches, as shown in Figure 4-7, should be set as follows (see also Note and Figure 4-8, below):

Switch	Setting
Double line feed	Off
Auto line feed	Off
Uppercase only	Off
Message load	Off
Full duplex	Off
Parity enable	Off
Baud 30	Off
Baud 1200	Off
Parity	Even (turned on)
Paper out	Off

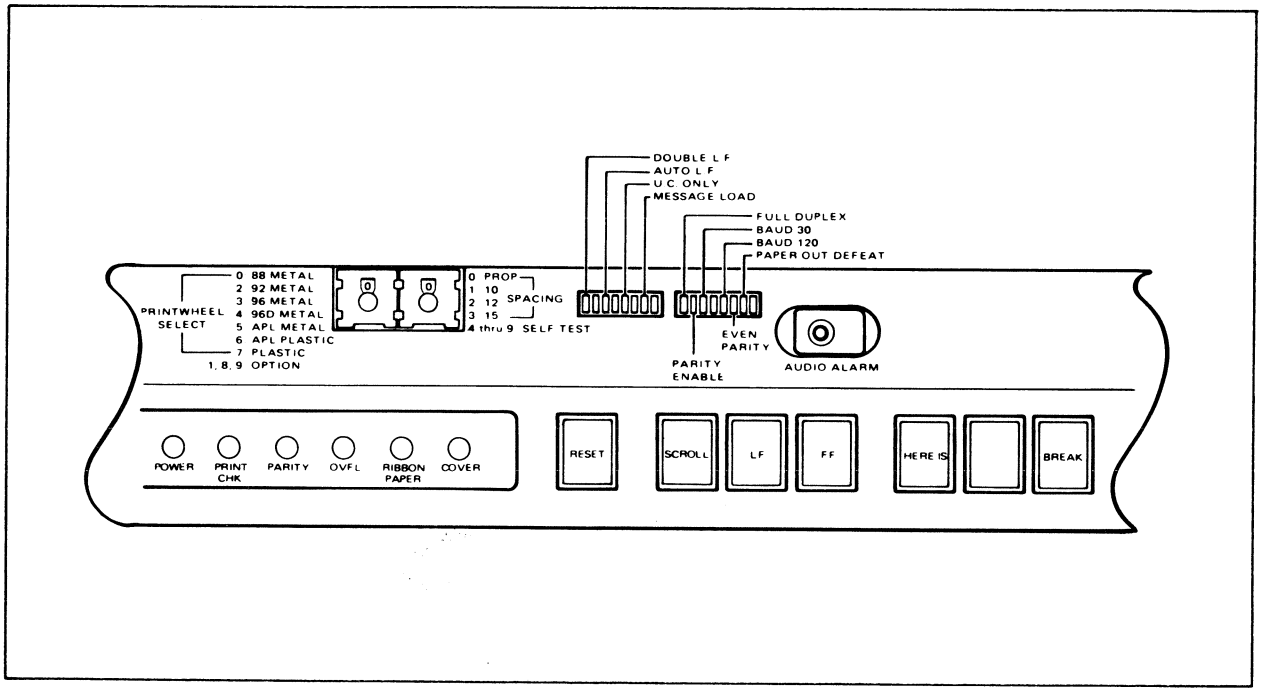


Figure 4-7. Diablo 630 HPRO5 Serial Printer Switches.

NOTE

In certain configurations of the Diablo 630 HPRO5 serial printer, the Printer Ready signal is at pin 11 of the RS-232-C connector, rather than at pin 20. The result of having the Printer Ready signal at pin 11 is that the signal never reaches the system, and data is not transmitted to the printer.

It is possible for the problem to occur in the Diablo 630 HPRO5 depending on the state of an internal jumper on its logic board. Normally, the Printer Ready signal appears at pin 11 of the RS-232-C connector unless a jumper is installed between pins 5 and 6 of plug A60 on the HPRO5 logic board. When the jumper is installed, the Printer Ready signal appears on pin 20 of the RS-232-C connector.

If you encounter the problem of your printer having the Printer Ready signal at pin 11 with no jumper installed, you can modify the printer end of the printer cable. Figure 4-8 shows the original cable connection and the modified cable connection.

Be aware that when you modify the printer cable, it becomes asymmetric and that the proper end must be plugged into the proper device. Also be aware that the modified cable may not work for all printer configurations. Therefore, both types of cables may be needed.

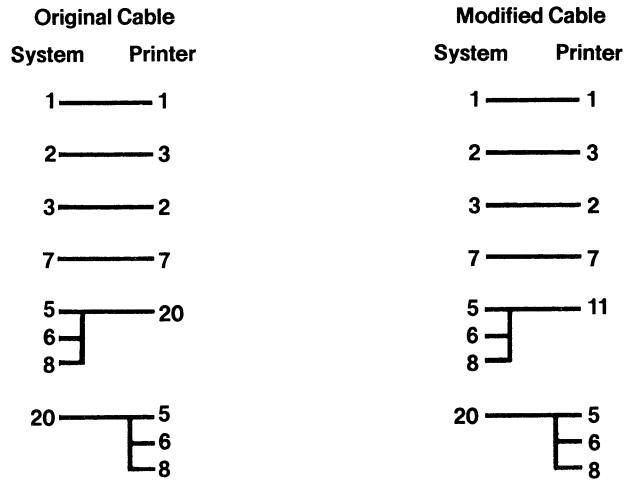


Figure 4-8. Cable Connections for the Diablo 630 HPRO5 Serial Printer.

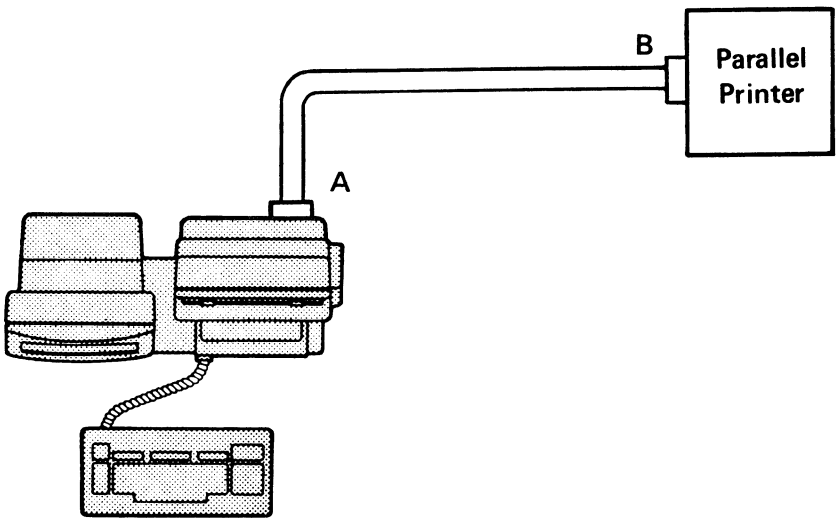
PARALLEL INTERFACE

The following subsection describes the assembly and connection of cables used for connecting a parallel printer to the IWS workstation. Switch settings for parallel printers supported by Convergent Technologies are shown and described in the "Parallel Printer Configurations" subsection, below.

Parallel Printer Interface Cable Assembly

This cable connects the workstation with a Centronics-type parallel interface line printer.

Connection:

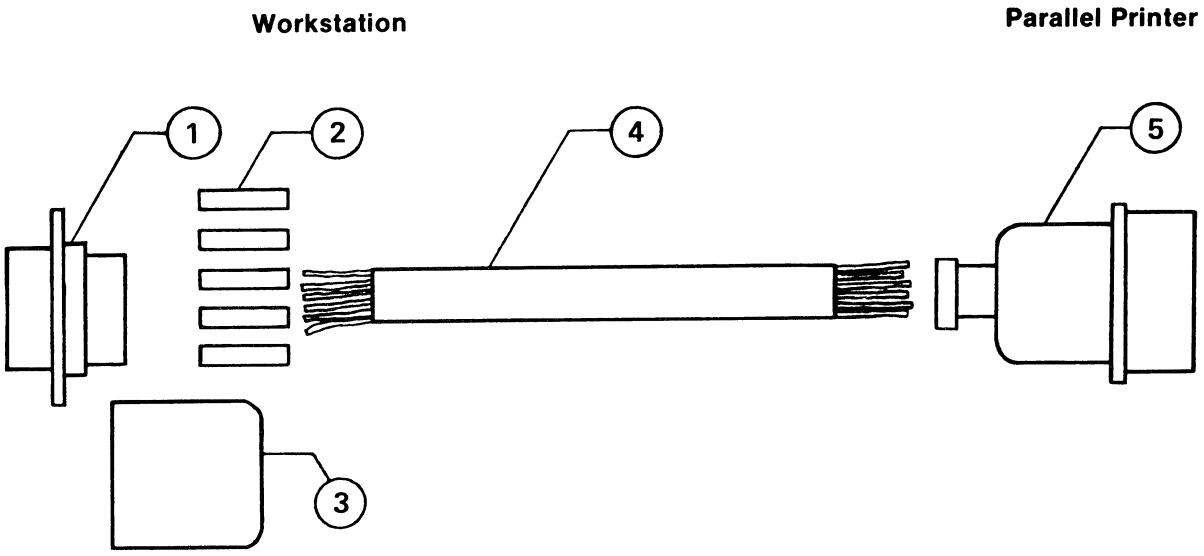


Pinouts:

Workstation Channel A	Line Printer	Assignment
1	2	DATA0+
10	20	GND
2	3	DATA1+
10	21	GND
3	4	DATA2+
10	22	GND
4	5	DATA3+
11	23	GND
5	6	DATA4+
11	24	GND
6	7	DATA5+
11	25	GND
7	8	DATA6+
11	26	GND
8	9	DATA7+
12	27	GND
14	1	STROBE-
15	19	GND
16	10	ACKNLG-
15	28	GND
17	11	BUSY+
15	29	GND
22	13	SLCT+
9	14	GND
21	12	PE+
9	16	GND
25	17	CHASSIS GND (shield)
12	14	GND (spare conductor)
12	14	GND (spare conductor)
9	16	GND (spare conductor)
9	16	GND (spare conductor)

Parallel Printer Interface Cable Construction

Directions:



Item	Quantity	Description
1.	1	25-pin D-type plug assembly (male). Use Amp part number 205208-1 or the equivalent.
2.	25	Connector contacts. Use Amp part number 66507-3 or the equivalent.
3.	1	Connector shell/strain relief. Use Amp part number 207908-7 or the equivalent.
4.	10 ft (3.0 m)	30-conductor shielded cable. Use Belden part number 9515 or the equivalent.
5.	1	36-pin "Blue Ribbon" type connector assembly (male). Use Amp part number 57-30360 or the equivalent.

NOTE

Chassis ground must be connected to the shield drain wire at both ends.

A twisted pair consists of a signal and a ground. That is, DATA0+ (workstation pin 1) and ground (workstation pin 10).

All four unused conductors must be connected to a ground at both ends.

The vinyl insulation must be stripped back at the 36-pin printer connector so that the metal strain relief clamps down on the conducting shield.

This cable must be 10 ft (30 m) minimum length. Longer lengths must be approved by the printer manufacturer.

PARALLEL PRINTER CONFIGURATIONS

The IWS has a Centronix-type interface for parallel printers, which uses the parallel printer interface cable. This subsection contains switch settings for some of the parallel printers supported by Convergent Technologies applications software.

Parallel Printer Switch Settings

Printronix MVP Parallel Printer

To use this printer with Convergent Technologies business graphics software, follow steps 1 through 4. (The printer panel referred to in these steps is shown in Figure 4-9.)

1. Turn the printer on, using the On/Off switch on the back panel.

2. Lift the front cover.

3. Press the 2nd FUNC button once.

4. Press the RDY button four times. The LED indicator to the left of RDY will now read: 001.

This sets up the size of each dot in accordance with Convergent Technologies graphics configuration requirements.

To use this printer as a text printer, push RDY two additional times, or until the LED indicator reads 002.

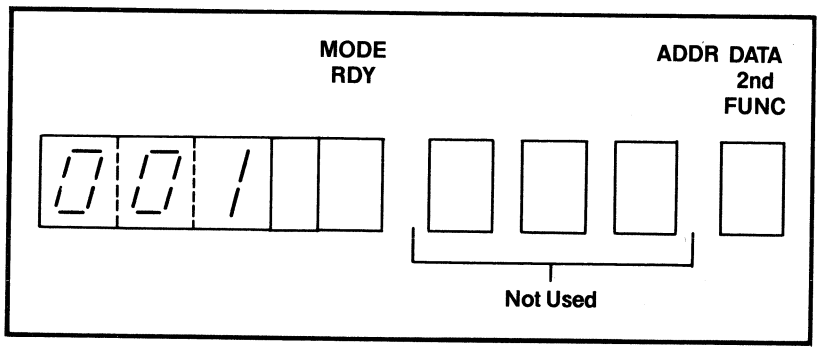


Figure 4-9. Printronix MVP Parallel Printer Switches.

TI 810 Parallel Printer

This printer can be used as either a parallel or a serial printer, depending on switches 1 through 3. Switch settings for using this printer as a parallel printer are listed below. More instructions can be found in the Texas Instruments instruction manual, and on the inside cover of the printer.

Switch number	Setting
1	On
2	On
3	On
4	Off
5	Off
6	On
7	On

RS-232-C COMMUNICATIONS DIAGNOSTIC INTERFACE

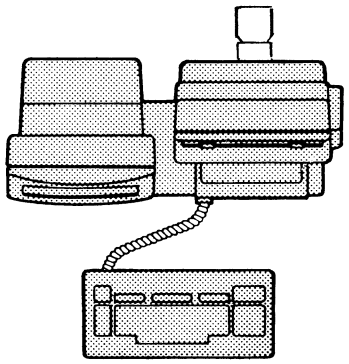
The diagnostic connector described in the following section provides simple loopback for running standalone communications diagnostics for RS-232-C configurations.

RS-232-C Communications Diagnostic Connector Assembly
(Convergent Technologies Part Number 64-00007)

This assembly provides RS-232-C diagnostic loopback capability.

Connection:

A

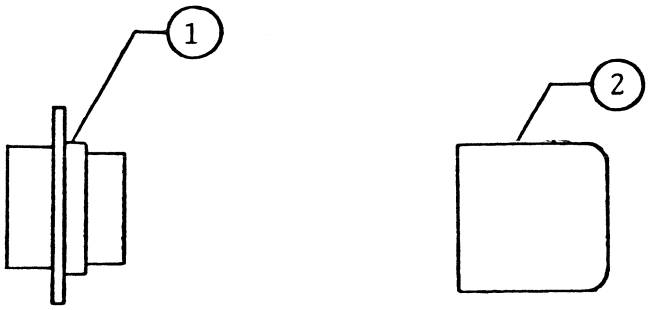


Connector Pinouts:

Workstation Channel A	Assignment
2	Transmit Data
3	Receive Data
4	Request to Send
5	Clear to Send
8	Carrier Detect
14	Secondary Transmit Data
16	Secondary Receive Data
20	Data Terminal Ready
22	Ring Indicator
6	Data Set Ready

RS-232-C Communications Diagnostic Connector Construction

Directions:



Item	Quantity	Description
1.	1	25-pin D-type plug assembly (male). Use Cannon part number 8026-25P or the equivalent.
2.	1	Connector shell. Use Cannon part number D13-110963-3 or the equivalent.

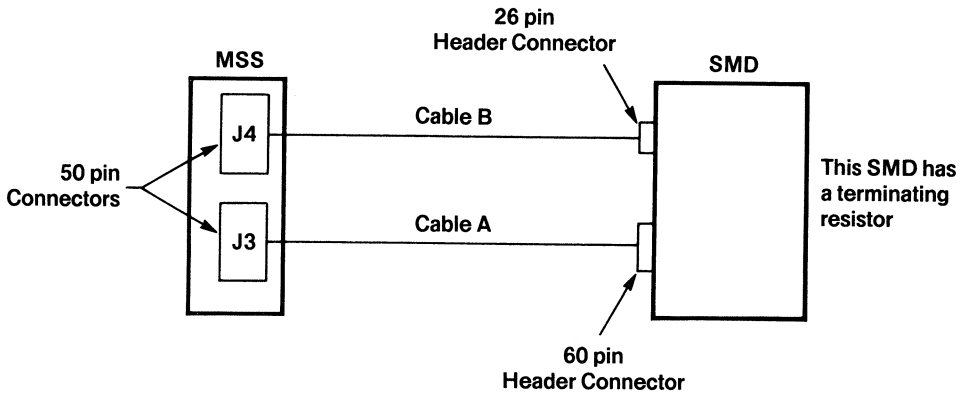
Note: This connector may be connected to communications Channel A or B if they are configured for RS-232-C operation.

SMD CABLE INTERFACE

The following subsection describes the cables used to connect Storage Module Drives to the IWS workstation. Up to four SMDs can be connected to the IWS workstation via two 50-pin connectors located on the SMD I/O Extender board: J3 and J4. Ribbon or twisted pair cables may be used. Proper pin assignments and correct pin correlation for connecting either connector J3 or J4 to a ribbon cable, and SMD drive Cable A or Cable B connectors is shown below, in the "SMD Interface Cable Assembly" subsection. Because the method of pin numbering is different, extreme caution must be used when connecting pins from the SMD I/O Extender board to a ribbon cable.

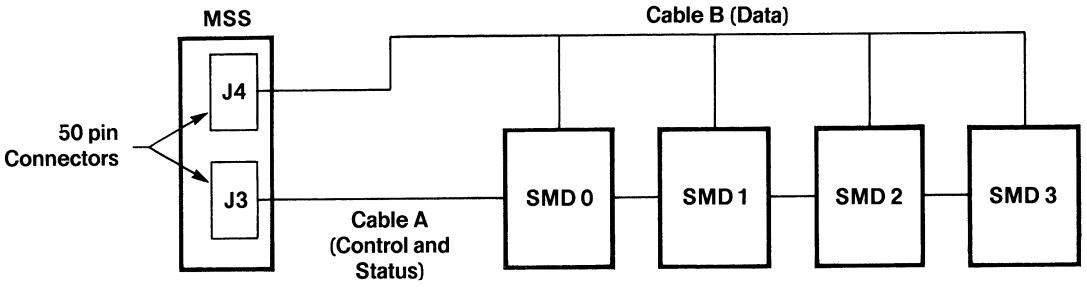
Single SMD Interface Cable Assembly

Function: This cable assembly connects one SMD to the SMD I/O Extender board in the MSS.



Multiple SMD Interface Cable Assembly

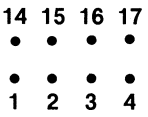
Function: This cable assembly connects four SMDs to the SMD I/O Extender board in the MSS.



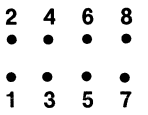
The terminating resistor is in SMD 3.

Notes: Cable A and Cable B pinouts, listed below, are the same when connecting either one SMD or four SMDs to the SMD I/O Extender board, with the following exception: if only one SMD is connected to the SMD I/O Extender board, the Cable B signals for SMD0 only are used. Listings for SMD1-SMD3 are used when connecting four SMDs to the SMD I/O Extender board.

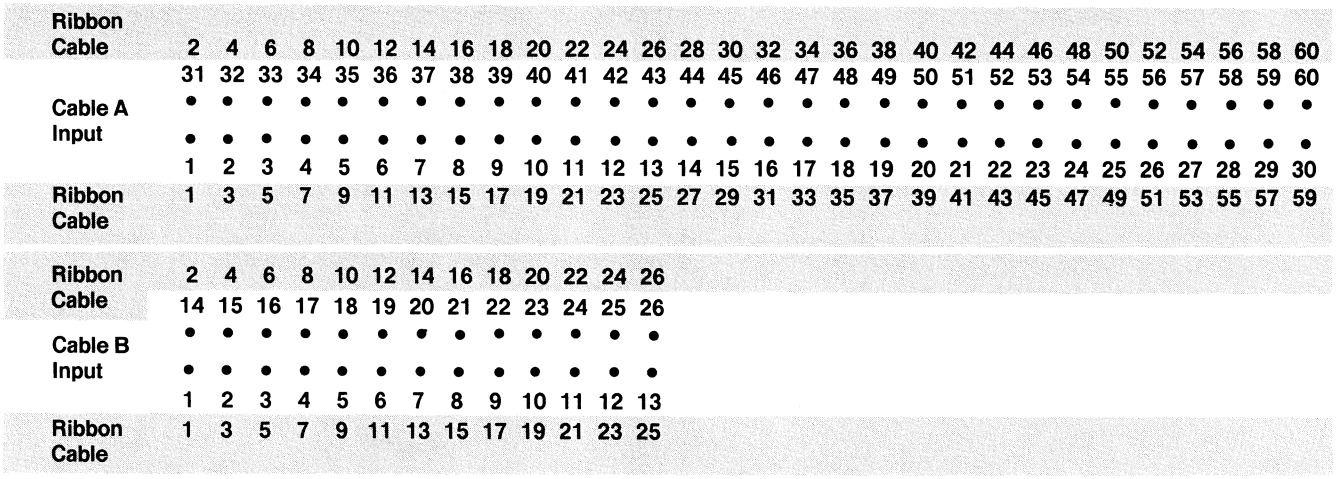
Pins for SMD Cable A and Cable connectors are numbered in the following manner:



But the ribbon cable is numbered in the following manner:



Therefore, if ribbon cables are used to connect SMDs to the IWS workstation, care must be taken to avoid connecting the wrong pins. Following is a diagram showing exactly which ribbon cable pins should be connected to SMD Cable A and Cable B connectors, and a listing of pin assignments.



Pinouts, Cable A

SMD Cable A (60-pin)	SMD Connector J3 (50-pin)	Ribbon Cable (60-pin)	Signal
49	30	38	URDY+
19	48	37	URDY-
47	12	34	ONCYL+
17	46	33	ONCYL-
46	28	32	SKER+
16	45	31	SKER-
45	11	30	FLT+
15	44	29	FLT-
58	14	56	WPRT+
28	13	55	WPRT-
48	29	36	IDX+
18	47	35	IDX-
50	31	40	AMFND+
20	49	39	AMFND-
34	34	8	BUS0H
4	19	7	BUS0L
35	35	10	BUS1H
5	20	9	BUS1L
36	36	12	BUS2H
6	21	11	BUS2L
37	37	14	BUS3H
7	22	13	BUS3L
38	38	16	BUS4H
8	6	15	BUS4L
39	39	18	BUS5H
9	23	17	BUS5L
40	7	20	BUS6H
10	40	19	BUS6L
41	24	22	BUS7H
11	8	21	BUS7L
42	41	24	BUS8H
12	25	23	BUS8L
43	42	26	BUS9H
13	26	25	BUS9L
26, 27, 44	43	51, 53, 28	CHRDY+
14, 56, 57	27	27, 52, 54	CHRDY-
33	1	6	TAG3+
3	18	5	TAG3-
31	5	2	TAG1+
1	4	1	TAG1-
32	3	4	TAG2+
2	2	3	TAG2-
53	16	46	USEL0+
23	15	45	USEL0-

SMD Cable A (60-pin)	SMD Connector J3 (50-pin)	Ribbon Cable (60-pin)	Signal
52	33	44	USTAG+
22	17	43	USTAG-
55	32	50	SECTOR+
25	50	49	SECTOR-
51			BUSY+
21			BUSY-
24	9	47	USEL1-
54	10	48	USEL1+
29			GND

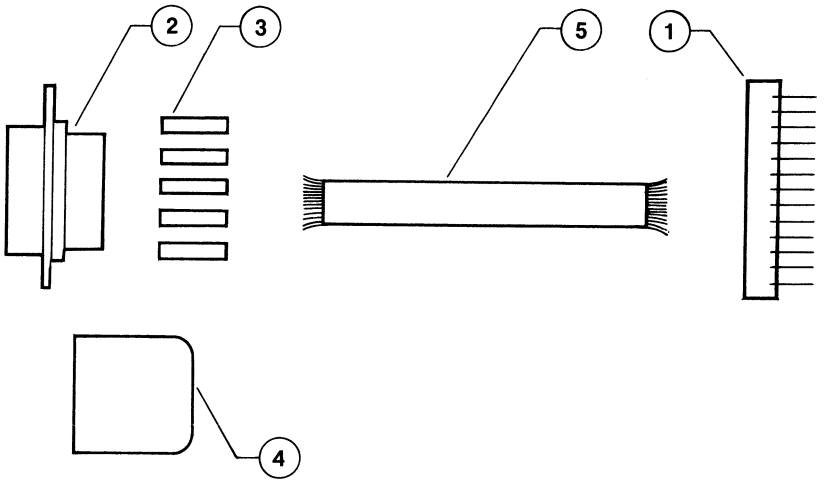
Pinouts, Cable B

SMD Cable B (26-pin)	SMD Connector J4 (50-pin)	Ribbon Cable	Signal
Drive 0			
14	27	2	SK0+
2	44	3	SK0-
17	29	8	RK0+
5	46	9	RK0-
19	47	12	WK0+
6	30	11	WK0-
16	45	6	RDD0+
3	28	5	RDD0-
20	31	14	WDD0+
8	48	15	WDD0-
9	32	17	S0SEL-
22	49	18	S0SEL-
Drive 1			
14	16	2	SK1+
2	17	3	SK1-
17	33	8	RK1+
5	13	9	RK1-
19	14	12	WK1+
6	15	11	WK1-
16	50	6	RDD1+
3	12	5	RDD1-
20	43	14	WDD1+
8	26	15	WDD1-
9	42	17	S1SEL+
22	25	18	S1SEL-

SMD Cable B (26-pin)	SMD Connector J4 (50-pin)	Ribbon Cable	Signal
Drive 2			
14	41	2	SK2+
2	24	3	SK2-
17	40	8	RK2+
5	23	9	RK2-
19	39	12	WK2+
6	22	11	WK2-
16	38	6	RDD2+
3	21	5	RDD2-
20	37	14	WDD2+
8	20	15	WDD2-
9	36	17	S2SEL+
22	19	18	S2SEL-
Drive 3			
14	35	2	SK3+
2	11	3	SK3-
17	10	8	RK3+
5	9	9	RK3-
19	8	12	WK3+
6	7	11	WK3-
16	6	6	RDD3+
3	5	5	RDD3-
20	4	14	WDD3+
8	3	15	WDD3-
9	18	17	S3SEL+
22	34	18	S3SEL-

SMD Interface Cable A Construction

Directions:

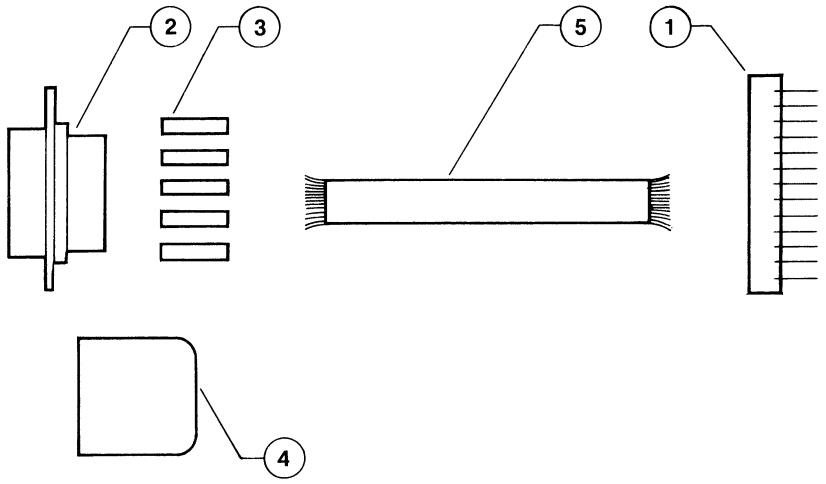


Item	Quantity	Description
1.	1	60-pin socket connector. Use 3M part number 3334-6000.
2.	1	50-pin D-type connector shell. Use Amp part number 205212-1 or the equivalent.
3.	50	Connector contacts. Use Amp part number 66507-3 or the equivalent.
4.	1	Shield and cable clamp assembly kits. Use Amp part number 1-207908-3.
5.		Non-grounded #28 AWG stranded flat cable. Use 3M part number 3365/60. OR Grounded #28 AWG stranded flat cable. Use 3M part number 3469/60. (Grounded cable is recommended for this connection.)

Note: The maximum length for this cable is 15 m (45 ft).

SMD Interface Cable B Construction

Directions:



Item	Quantity	Description
1.	1	26-pin socket connector. Use 3M part number 3399-6000.
2.	1	50-pin D-type connector shell. Use Amp part number 205212-1 or the equivalent.
3.	48	Connector contacts. Use Amp part number 66507-3 or the equivalent.
4.	1	Shield and cable clamp assembly kits. Use Amp part number 1-207908-3.
5.		Non-grounded #28 AWG stranded flat cable. Use 3M part number 3365/26. OR grounded #28 stranded flat cable. Use 3M part number 3469-26. (Grounded cable is recommended for this connection.)

Note: The maximum length for this cable is 15 m (45 ft).

APPENDIX A: IWS PERIPHERALS HARDWARE SPECIFICATIONS

ELECTRONIC

Memory Capacity

	8-inch Floppy Disk Drive (double density)	8-inch Winchester Disk Drive (10M byte)	8-inch Winchester Disk Drive (20M byte)	8-inch Winchester Disk Drive (40M byte)
Unformatted:	800K bytes	10.5M bytes	21.0M bytes	42.0M bytes
Formatted:	591K bytes	8.4M bytes	16.8M bytes	33.6M bytes
Sector size:	512 bytes	512 bytes	512 bytes	512 bytes
Sectors per track:	15	16	16	16

Storage Module Drive (SMD) specifications are listed in Appendix B, "Storage Module Drive Description and Specifications."

Serial Input/Output Rate

RS-422 (Cluster Communications)

Internal clock	50 baud to 615 kbaud (maximum)
External clock	dc to 730 kbaud

RS-232-C Communications

Internal clock	50 baud to 19.2 kbaud (maximum)
External clock	dc to 19.2 kbaud

Parallel Output Rate
(Printer Interface)

19.6K characters/second

Mass Storage Timing

	Floppy Disk Drive	Winchester Disk Drive
Transfer rate	62.5K bytes/sec	543.4K bytes/sec
Access time (average)	260 milliseconds	70 milliseconds (10M byte) 50 milliseconds (20M byte)
Access time (track to track)	8 milliseconds	19 milliseconds
Settling time	8 milliseconds	15 milliseconds
Head load time	35 milliseconds	N/A

Storage Module Drive timing information is listed in Appendix B, "Storage Module Drive Description and Specifications."

SAFETY AND ENVIRONMENTAL

Safety

UL 478 (EDP) and 114 (office equipment)

CSA 154 (EDP) and 143 (office equipment)

VDE 0730, Parts 1 and 2 (available at extra cost)

BSI BS 3861, Parts 1, 2, and 3 (available at extra cost)

Electromagnetic Interference

US FCC Rules and Regulations, Part 15, Subpart J, Class A

VDE 0871, Level A (available at extra cost)

Electrostatic Discharge

5,000 V	no observable effect
15,000 V	no operator-perceived errors
25,000 V	no permanent damage

Altitude

Operating	6,000 ft at sea level
Nonoperating	12,000 ft at sea level

Acoustic Noise Level

NR40

Temperature and Humidity

	System	Media
Temperature		
Operating	32 to 104°F (0 to 40°C)	50 to 104°F (10 to 40°C)
Nonoperating	-40 to 167°F (-40 to 75°C)	-7 to 116.6°F (-22 to 47°C)
Humidity (non-condensing)	5 to 95%	20 to 80%

PHYSICAL

Mass Storage Base Unit

Height	26.00 in (66.0 cm)
Width	8.46 in (21.50 cm)
Depth	20.87 in (53.00 cm)
Weight	85.00 lb (38.64 kg)

Information on Storage Module Drives is listed in Appendix B, "Storage Module Drive Description and Specifications."

Cable Lengths

AC line	10 ft
Workstation to MSS	10 ft
MSS to MSX	5 ft
Maximum cluster length	1100 ft

ELECTRICAL

AC Power Capacity

60 ±0.5 Hz

AC Voltage

85 to 130 Vrms

AC Power Requirements

Maximum	105 Vrms
MSS unit	3.3 A

APPENDIX B: STORAGE MODULE DRIVE DESCRIPTION AND SPECIFICATIONS

Storage Module Drives (SMDs) are high-speed, random access digital data storage devices. Up to four SMDs can be connected to the IWS workstation and controlled by the SMD Controller board at one time. The SMD Controller board has been tested with the Fujitsu 80M-byte and the CDC 80M- and 300M-byte drives.

When an SMD is connected to an IWS workstation (or rather, an MSS), it communicates only with the SMD Controller board. The controller board issues commands to the drive, which decodes the commands and performs the appropriate operation. In addition to the commands, the SMD Controller board sends write data, write clock, and power sequence information to the drive.

The SMD, in turn, sends various status signals to the controller board, including read data, read clock, and servo clock information, which the controller uses to monitor and control SMD operations.

Specifications are listed below for the Fujitsu 80M-byte and the CDC 80M- and 300M-byte drives.

FUJITSU 80M-BYTE STORAGE MODULE DRIVE (MODEL M2312K)

Electronic

Storage Capacity

Unformatted	84,439,040 bytes
Formatted	67,551,232 bytes
Sector size	512 bytes
Sectors per track	32
Number of cylinders	589
Tracks/cylinder	7
Cylinder capacity	143,360 bytes
Track capacity	20,480 bytes
Latency (average)	8.3 milliseconds
Positioning time:	
Track to track	5 milliseconds
Average	20 milliseconds
Maximum	40 milliseconds
Rotational speed	3,600 RPM (±1%)
Transfer rate	1.229M bytes/sec
Encoding method	MFM
Interface data	NRZ
Recording density	9,550 BPI
Track density	720 TPI
Start/stop time	<20/<40 sec
Interface	SMD

Physical

Mechanical

Depth	15.0 in (380 mm)
Width	8.5 in (216 mm)
Height	5.1 in (130 mm)

Mechanical (cont.)

Weight	Approx. 25 lb (11.3 kg)
Mounting axis	Horizontal/vertical

Operating

Temperature	41°F to 104°F (5°C to 40°C)
Temperature variation	<27°F/hr (15°C/hr)
Relative humidity (noncondensing)	20% to 80%
Altitude	10,000 ft (3,000 m)
Vibration	0.2 G max (30 to 60 Hz) Both ways: 2 min x 30 cycle (sine wave)
Shock	<2.0 G, 10 milliseconds

Nonoperating

Temperature	-40°F to 140°F (-40°C to 60°C)
Relative humidity (noncondensing)	5% to 95%
Altitude	40,000 ft (12,000 m)
Vibration	0.4 G max (3 to 60 Hz) Both ways: 2 min (sine wave)
Shock	<5.0 G, 30 milliseconds (during storage or transportation)

Electrical

DC Power Requirements

DC voltage	Load Current (basic)
+5 V ± 5%	3.5 A
-12 V ± 5%	3.0 A
+24 V ± 10%	30 A (effective, typical) 60 A maximum

CDC 80M-BYTE AND 300M-BYTE STORAGE MODULE DRIVES

Electronic

Data Capacity

	80M byte (Model 9762)	300M byte (Model 9766)
bytes/track*	20,160	20,160
bytes/cylinder*	100,800	383,040
bytes/spindle*	81,446,400	309,496,320
Cylinders/spindle*	823	823

*based on 8-bit bytes and not allowing for tolerance gaps for sectoring, etc.

Formatted Capacity

	80M byte (Model 9762)	300M byte (Model 9766)
Per drive	67.4M bytes	256.2M bytes
Sector size	512 bytes	512 bytes
Sectors per track	32	32

Disk Pack

Type	883-91 (one/drive)
Disks/pack	12 (top and bottom disks are for protection only)
Data surfaces	19 (300M byte) 5 (80M byte)
Servo surfaces	1
Usable tracks/surface	823
Tracks/inch	384
Track spacing	0.0026 in (0.066 mm) (center to center)
Coating	Magnetic oxide

Recording Characteristics

Mode	MFM
Density (nominal)	
Outer track	4038 bits/in (1590 bits/cm)
Inner track	6038 bits/in (2377 bits/cm)
Rate (nominal)	9.67 MHz (1 209 600 bytes/sec)

Heads

Read/Write	19 (300M byte) 5 (80M byte)
Servo	1
Read/Write width	0.002 in (0.051 mm)

Seek Characteristics

Mechanism	Voice coil, driven by servo loop
Maximum seek time	55 milliseconds
Maximum track seek time	6 milliseconds
Average seek time	30 milliseconds
Average latency	8.33 milliseconds (at 3600 RPM)
Maximum latency	17.3 milliseconds (at 3474 RPM)
Spindle speed	3600 RPM

Physical

Mechanical

Height	36 in (920 mm)
Width	36 in (914 mm)
Depth	23 in (584 mm)
Weight	550 lb (252 kg)

Operating

Temperature	59°F to 90°F (15.5°C to 32.2°C)
Temperature variation	12°F (6.6°C)/hr
Relative humidity (noncondensing)	20% to 80%
Altitude	-1000 ft to 6500 ft (305 m to 2000 m)

Nonoperating

Temperature (packed for transit)	-40°F to 158°F (-40.4°C to 70.0°C)
Nonoperating change/hr	36°F (20°C)/hr
Relative humidity (noncondensing)	5% to 95%
Altitude	-1000 ft to 15,000 ft (305 m to 4572 m)

APPENDIX C: MSS/MSX CONNECTORS AND SIGNAL LISTS

This appendix contains pin listings for connectors used in the MSS and MSX.

MASS STORAGE SUBSYSTEM CONNECTORS (located on the SMD I/O Extender board)

Connector Designation	Connector Function	Number of Pins
J1	DCI signals from host to controller	50
J2	Signals from controller to host	50
J3	Cable to SMD	50
J4	Cable to SMD	50
P1	To motherboard	120
P2	To motherboard	80

Table C-1. MSS Connector J1 Pin Assignments. (Page 1 of 2)

Pin	Signal
1	GND
2	ACK-
3	GND
4	SELF-
5	GND
6	INTR-
7	GND
8	BUS2+
9	GND
10	BUS1+
11	GND
12	BUS7+
13	GND
14	BUSA+
15	GND
16	BUSD+
17	GND
18	
19	GND
20	WRSTR-
21	GND
22	WRSTR-
23	GND
24	
25	GND

Table C-1. MSS Connector J1 Pin Assignments. (Page 2 of 2)

Pin	Signal
26	BUS6+
27	GND
28	BUS5+
29	GND
30	BUSC+
31	GND
32	BUSF+
33	BUS9+
34	GND
35	DREQ-
36	GND
37	SELW-
38	GND
39	RDSTR-
40	GND
41	BUS4+
42	GND
43	BUS3+
44	GND
45	BUSE+
46	GND
47	BUS8+
48	
49	BUSB+
50	BMR-

Table C-2. MSS Connector J2 Pin Assignments. (Page 1 of 2)

Pin	Signal
1	GND
2	HDLOAD-
3	GND
4	SIDE-
5	GND
6	
7	GND
8	TRACK0-
9	USEL1-
10	USEL2-
11	GND
12	TCK2-
13	STEPEN-
14	WWD1+
15	GND
16	WRDD1-
17	
18	SKCOMPL-
19	GND
20	REDWC-
21	GND
22	WINDEX-
23	GND
24	STEP-
25	GND

Table C-2. MSS Connector J2 Pin Assignments. (Page 2 of 2)

Pin	Signal
26	WRPROT-
27	GND
28	TCK1-
29	GND
30	WWD1+
31	
32	WWD2-
33	WRDD2-
34	GND
35	GND
36	WREADY-
37	SEL1-
38	SEL2-
39	DIR-
40	GND
41	GND
42	WWRGATE-
43	D1SEL-
44	TCK1+
45	TCK2+
46	GND
47	
48	WWD2+
49	WRDD1+
50	WRDD2+

Table C-3. MSS Connector J3 Pin Assignments. (Page 1 of 2)

Pin	Signal
1	TAG3+
2	TAG2-
3	TAG2+
4	TAG1-
5	TAG1+
6	BUS4L
7	BUS6H
8	
9	BUS5L
10	BUS6L
11	BUS7L
12	ONCYL+
14	CHRDY-
15	USEL0-
16	USEL0+
17	USTAG-
18	TAG-
19	BUS0L
20	BUS1L
21	BUS2L
22	BUS3L
23	BUS5L
24	BUS7H
25	BUS8L

Table C-3. MSS Connector J3 Pin Assignments. (Page 2 of 2)

Pin	Signal
26	BUS9L
27	CHRDY-
28	SKER-
29	IDX+
30	URDY+
31	AMFND+
32	SECTOR+
33	USTAG+
34	BUS0H
35	BUS1H
36	BUS2H
37	BUS3H
38	BUS4H
39	BUS5H
40	BUS6L
41	BUS8H
42	BUS9H
43	CHRDY
44	FLT-
45	SKER-
46	ONCYL-
47	IDX-
48	URDY-
49	AMFND-
50	SECTOR-

Table C-4. MSS Connector J4 Pin Assignments. (Page 1 of 2)

Pin	Signal
1	USEL1-
2	USEL1+
3	WDD3-
4	WDD3+
5	RDD3-
6	RDD3+
7	WK3-
8	WK3+
9	RD3-
10	RD3+
11	SK3-
12	RDD1-
13	RK1-
14	WK1+
15	WK1-
16	SK1+
17	SK1-
18	S3SEL+
19	S2SEL-
20	WDD2+
21	RDD2-
22	WK2-
23	RK2-
24	SK2-
25	S1SEL-

Table C-4. MSS Connector J4 Pin Assignments. (Page 2 of 2)

Pin	Signal
26	WDD1-
27	SK0+
28	RDD0-
29	RK0+
30	WK0-
31	WDD0+
32	S0SEL+
33	RK1+
34	S3SEL-
35	SK3+
36	S2SEL+
37	WDD2+
38	RDD2+
39	WK2+
40	RD2+
41	SK2+
42	S1SEL+
43	WDD1+
44	SK0-
45	RDD0+
46	RD0-
47	WK0+
48	WDD0-
49	S0SEL-
50	RDD1+

Table C-5. MSS Connector P1 Pin Assignments. (Page 1 of 3)

Pin	Signal
1	
2	BUSD+
3	
4	BUS9+
5	GND
6	BUSB+
7	BUSF+
8	BUS8+
9	BUSA+
10	BUS7+
11	BUSC+
12	BUSE+
13	BUS5+
14	BUS3+
15	GND
16	BUS1+
17	BUS6+
18	BUS4+
19	BUS2+
20	BUS0+
21	RDSTR-
22	INTR-
23	WRSTR-
24	SELW-
25	GND
26	
27	SELF-
28	CTL-
29	DREQ-
30	ACK-
31	WRDD0-
32	WRDD0-
33	WWD0-
34	WWD0+
35	GND
36	TCK0+
37	TCK0-
38	D0SEL-
39	
40	WRDD3-

Table C-5. MSS Connector P1 Pin Assignments. (Page 2 of 3)

Pin	Signal
41	WWD3+
42	WWD3-
43	TCK3-
44	TCK3+
45	GND
46	D3SEL-
47	WRDD1-
48	WRDD2+
49	WRDD2-
50	WRDD1+
51	WRDD2-
52	WWD2+
53	WWD1-
54	WWD1+
55	GND
56	TCK2+
57	TCK2-
58	TCK1+
59	TCK1-
60	D1SEL-
61	D2SEL-
62	CONFIG-
63	WWRGATE-
64	WRPROT-
65	GND
66	RDDATA-
67	TRACK0-
68	WRDATA-
69	STEP-
70	DIR-
71	SEL3-
72	SEL2-
73	SEL1-
74	SEL0-
75	GND
76	WREADY-
77	WINDEX-
78	HDLOAD-
79	REDWC-
80	SIDE-

Table C-5. MSS Connector P1 Pin Assignments. (Page 3 of 3)

Pin	Signal
81	SKCOMPL-
82	STEPEN+
83	
84	SECTOR-
85	GND
86	
87	WPRT-
88	WPRT+
89	USEL0-
90	USEL0+
91	USTAG+
92	USTAG+
93	
94	
95	GND
96	AMFND-
97	AMFND+
98	URDY-
99	URDY+
100	IDX-
101	IDX+
102	
103	
104	SKER-
105	GND
106	SKER+
107	FLT-
108	FLT+
109	CHRDY-
110	CHRDY+
111	BUS9L
112	BUS9H
113	BUS8L
114	BUS8H
115	GND
116	BUS7L
118	BUS6L
119	BUS6H
120	

Table C-6. MSS Connector P2 Pin Assignments. (Page 1 of 2)

Pin	Signal
1	BUS5L
2	BUS5H
3	BUS4L
4	BUS4H
5	GND
6	BUS3L
7	BUS3H
8	BUS2L
9	BUS2H
10	BUS1L
11	BUS1H
12	BUS0L
13	BUS0H
14	TAG3-
15	GND
16	TAG3+
17	TAG2-
18	TAG2+
19	TAG1-
20	TAG1+
21	SK1+
22	SK1-
23	RD1+
24	RK1-
25	GND
26	WK1+
27	WK1-
28	RDD1+
29	S0SEL-
30	S0SEL+
31	WDD0-
32	WDD0+
33	WK0+
34	WK0-
35	GND
36	RK0-
37	RK0+
38	RDD0+
39	RDD0-
40	SK0-

Table C-6. MSS Connector P2 Pin Assignments. (Page 2 of 2)

Pin	Signal
41	SK0+
42	RDD1-
43	WDD1+
44	WDD1-
45	GND
46	S1SEL+
47	S1SEL-
48	SK2+
49	SK2-
50	RK2+
51	RK2-
52	WK2+
53	WK2-
54	RDD2+
55	GND
56	RDD2-
57	WDD2+
58	WDD2-
59	S2SEL+
60	S2SEL-
61	SK3+
62	SK3-
63	RK3+
64	RK3-
65	GND
66	WK3+
67	WK3-
68	RDD3+
69	RDD3-
70	WDD3+
71	WDD3-
72	S3SEL+
73	S3SEL-
74	USEL1-
75	GND
76	USEL1+
77	
78	
79	
80	

MASS STORAGE EXPANSION CONNECTORS

Connector Designation	Connector Function	Number of Pins
P1	Cable from MSS to MSX	50
P2	Write-Protect Board	9
P3	Control and status to both drives	50
P4	Data to drive	20
P5	Data to drive	20

Table C-7. MSX Connector P1 Pin Assignments. (Page 1 of 2)

Pin	Signal
1	GND
2	HDS1-
3	GND
4	HDSO-
5	GND
6	SEL1-
7	GND
8	TRACK0-
9	GND
10	D2SEL-
11	GND
12	TCK2-
13	HDS2-
14	WWD1-
15	GND
16	WRDD1-
17	GND
18	SKCOMPL-
19	GND
20	REDWC-
21	GND
22	WINDEX-
23	GND
24	STEP-
25	GND
26	WRPROT-
27	GND
28	TCK1-
29	GND
30	WWDH-
31	GND
32	WWD2-
33	WRDD2-
34	GND
35	GND
36	WREADY-
37	SEL2-
38	SEL3-
39	DIR-
40	GND

Table C-7. MSX Connector P1 Pin Assignments. (Page 2 of 2)

Pin	Signal
41	GND
42	WWGATE-
43	DISEL-
44	TCK1+
45	TCK2-
46	GD
47	GND
48	WWD2+
49	MRD1+WRDD1+
50	WRDD2+

Table C-8. MSX Connector P2 Pin Assignments.

Pin	Signal
1	BDSO-
2	GND
3	DSO-
4	DS1-
5	GND
6	BDS1-
7	DS2-
8	GND
9	BDS2-

Table C-9. MSX Connector P3 Pin Assignments. (Page 1 of 2)

Pin	Signal
1	GND
2	REDWC-
3	GND
4	STEPHEN+
5	GND
6	
7	GND
8	SKCOMPL-
9	GND
10	
11	GND
12	
13	GND
14	SIDE-
15	GND
16	
17	GND
18	HSLOAD-
19	GND
20	WINDEX-
21	GND
22	WREADY-
23	GND
24	
25	
26	SELO-
27	GND
28	SEL1-
29	GND
30	SEL2-
31	GND
32	SEL3-
33	GND
34	DIR-
35	GND
36	STEP-
37	GND
38	
39	GND
40	WWGATE-
41	GND

Table C-9. MSX Connector P3 Pin Assignments. (Page 2 of 2)

Pin	Signal
42	TRACK0-
43	
44	WRPROT-
45	GND
46	RDDATA-
47	GND
48	
49	GND
50	CONFIG-

Table C-10. MSX Connector P4 Pin Assignments.

Pin	Signal
1	DOSEL-
2	
3	
4	
5	
6	
7	
8	
9	TCKO+
10	TCKO-
11	GND
12	GND
13	WWDO+
14	WWDO-
15	GND
16	GND
17	WRDDO+
18	WRDDO-
19	GND
20	GND

Table C-11. MSX Connector P5 Pin Assignments.

Pin	Signal
1	D3SEL-
2	
3	
4	
5	
6	
7	
8	
9	TCK3+
10	TCK3-
11	GND
12	GND
13	WWD3+
14	WWD3-
15	GND
16	GND
17	WRDD3+
18	WRDD3-
19	GND
20	GND

APPENDIX D: SWITCH SETTINGS FOR IWS WORKSTATION MEMORY CONFIGURATIONS

Memory configuration for the IWS workstation peripherals (the MSS, MSX, and SMDs) can be controlled by Switch 1 (SW1), located on the controller board and shown below, in Figure D-1. In the following table, an "X" indicates that one side of the switch has been pushed down, either to an "On" or an "Off" position.

Drive	Switch	Setting		Memory Configuration
		On	Off	
MSS	1	X	-	40M bytes
MSS	1	-	X	10M bytes
MSX	2	X	-	40M bytes/40M bytes
MSX	2	-	X	20M bytes/20M bytes
SMD	3	X	-	300M-byte CDC
SMD	3	-	X	80M-byte CDC
	4			Reserved

The IWS workstation automatically recognizes the 20M-byte Winchester disk drive configuration for the MSS, and the 80M-byte Fujitsu SMD drive. No switch settings are necessary.

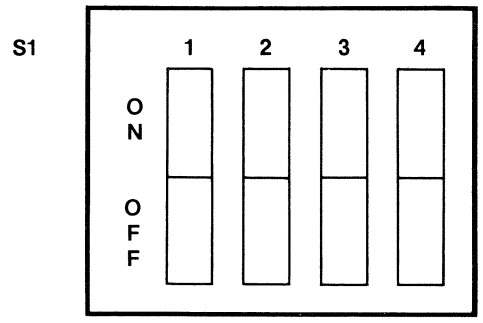


Figure D-1. Controller Board Switch Settings.

APPENDIX E: MOTHERBOARD SIGNAL GLOSSARY

Signal Name	Page Number	Description
A0+-A3+	5/11	Address 0-3. Select one of 16 registers in the 8X320 to be used for a data transfer.
A0+-A12+	2/11	Address 0-12. From the 8X300. Instruction address lines to ROM memory.
ACK-	5/11	Acknowledge signal. Sent from IWS workstation to SMD controller board during a data transfer.
AMFND	8/11	Address Mark Found. Not used on this board.
BUS0-BUSF	5/11	DCI Bus. Read, write, or control data from the 8X320 to the IWS workstation.
BUS0-BUS9	11/11	SMD Control Bus. From the 8X300 to the selected SMD drive. For more information, see the "SMD Interface Signals" subsection.
CONFIG-	11/11	Configuration (4). From the MSS Winchester disk drive to the 8X300. If high, the CONFIG- signal indicates that the MSS Winchester disk drive is a 20M-byte drive. If low, the drive is either 10M- or 40M-bytes, as determined by the SW1 setting on the SMD Controller board. (For more information on SW1, see Appendix D.)
CTL-	5/11	Control signal. From the host. Used to define the type of transfer between the IWS workstation and the SMD Controller board.

Signal Name	Page Number	Description
CHRDY	10/11	Channel Ready. From the 8X320 to the selected drive. Tells the drive that the controller is ready.
D0SEL- to D3SEL-	8/11	Device Select Signals. From the IWS workstation to the SMD Controller board. Used to select the SMD Unit number. (Also see Figure 2-1.)
DIR-	4/11	Direction. From the 8X330 to the floppy disk drive. Determines the direction in which the head carriage is incremented.
DREQ-	5/11	Data Request. Delayed DMA data request.
FLT	8/11	Drive Fault. From the selected drive to the SMD Controller board. Indicates a drive fault.
HDLOAD-	4/11	Head Load. From the 8X330 to the floppy disk drive. Controls head loading.
HINTR+	4/11	Head Interrupt. From the 8X330. Controls on-disk gating of the INTR- signal.
IDX	8/11	Index. From the SMD to the 8X300. A two-byte pulse read by the SMD Controller board during a read/write operation and used for reference.
INTR-	5/11	Interrupt Signal. From the 8X320 to the IWS workstation. Asserted at the end of each data read or write transfer.
LITE-	11/11	Light. From the 8X300 to the IWS workstation.
ONCYL	8/11	On Cylinder. From the SMD to the 8X300. Asserted with URDY or when a Seek or RTZ operation is completed.

Signal Name	Page Number	Description
RDDATA-	4/11	Floppy Read Data. Read data sent from the floppy drive to the 8X330.
RDD0-RDD3	10/11	SMD Read Data. Read data from the SMD B Cable.
RDSTR-	5/11	Read Strobe. From the IWS workstation to the 8X320. Indicates that data is being sent to the SMD Controller board from the IWS workstation.
RK0-RK3	10/11	SMD Read Clock from the SMD B Cable. Also called the 1F Read Clock.
SECTOR-	8/11	Sector. From the selected SMD drive. Read by the SMD Controller board to signify the beginning of a sector.
SELF-	5/11	Select Floppy. From the 8X320 to the IWS workstation. Indicates a non-DMA transfer between the floppy disk drive and the SMD Controller board.
SELW-	5/11	Select Winchester. From the 8X320 to the IWS workstation. Indicates a non-DMA transfer between the Winchester disk drive and the SMD Controller board.
SIDE-	4/11	Side Select. From the 8X330 to the floppy disk drive. Selects which side of a disk is used in a read or write operation.
SKER	8/11	Seek Error. From the SMD to the 8X300. Asserted by an SMD is there is an error during a Seek or RTZ operation.
SKCOMPL-	4/11	Seek Complete. From drive to 8X330. Indicates whether the Winchester or SMD Seek, RTZ, or Offset operation just performed was successful.

Signal Name	Page Number	Description
SK0-SK3	10/11	SMD Servo-clock from the SMD B Cable. Also called the 1F Write Clock.
S0SEL- S3SEL	10/11	Unit Selected from the SMD drive to the 8X300.
STEP-	4/11	Step Signal. From the 8X330 to the floppy disk drive. Increments the floppy disk drive head carriage one track on the disk surface, either in or out, depending on the state of the DIR- signal.
STEPEN+	4/11	Step Enable. From the 8X330 to the floppy disk drive. Enables a one-track increment.
TAG1	11/11	Cylinder Address. From the 8X300 to the selected SMD drive. Causes the contents of BUS0-BUS9 to be set into the SMD cylinder address register.
TAG2	11/11	Head Address. From the 8X300 to the selected SMD drive. Causes the content of BUS0-BUS9 to be set into the SMD head address register.
TAG3	11/11	Control Select. Enables BUS0-BUS9, control bits from the 8X300, to be written into the selected SMD.
TRACK0-	4/11	Track 0. Indicates that the selected disk drive's head is positioned over the first readable track.
URDY	8/11	Unit Ready. From the selected SMD to the 8X300. URDY is asserted when a drive initial seek is completed.
US0-US2	11/11	Unit Selected. When these signals are different, they are sent from the 8X300 to the SMDs. When they are the same, they are sent from the SMD and

Signal Name	Page Number	Description
		indicate that a drive has been selected.
USEL0-USEL3	11/11	Drive Select. From the 8X300 to the SMDs.
USTAG	11/11	Drive Select Enable. Gates the USEL drive select.
WDATA1+		
WDD0-WDD3	10/11	SMD Write Data. Write data from the IWS workstation to the selected SMD drive.
WINDEX-	4/11	Winchester Index. From the selected disk drive. Indicates that the disk drive is detecting the beginning of the first physical sector on the track.
WK0-WK3	10/11	SMD Write Clock. From the SMD Controller board to the selected SMD drive. This signal is the return signal for SK0-SK3.
WPRT	8/11	Write Protect. From the SMD to the 8X300. Indicates that a SMD drive is write-protected.
WRDATA-	4/11	Write Data. From the 8X330. Precompensated write data to the selected disk drive.
WRDD0-WRDD3	10/11	Winchester Control Data. Control data from the Winchester drive.
WRPROT-	4/11	Write Protect. From the selected disk drive to the 8X330. Indicates that the disk drive is allowing only read operations.
WREADY-	4/11	Winchester Ready. From the selected disk drive. Indicates that the disk drive exists and is ready to perform a seek, read, or write operation.

Signal Name	Page Number	Description
WRSTR-	5/11	Write Strobe. From the IWS workstation to the SMD Controller board. Used in a DMA transfer to indicate that data is being sent from the IWS workstation to the SMD Controller board.
WDD0-WDD3	4/11	Winchester Clock. From the 8X330 to the host.
WWRGATE-	4/11	Winchester Write Gate. From the 8X330. A write data enable for the selected disk drive.

APPENDIX F: SHUGART SA800/801 FLOPPY DISK DRIVE MANUAL

SA800/801 Diskette Storage Drive

OEM Manual

Shugart

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

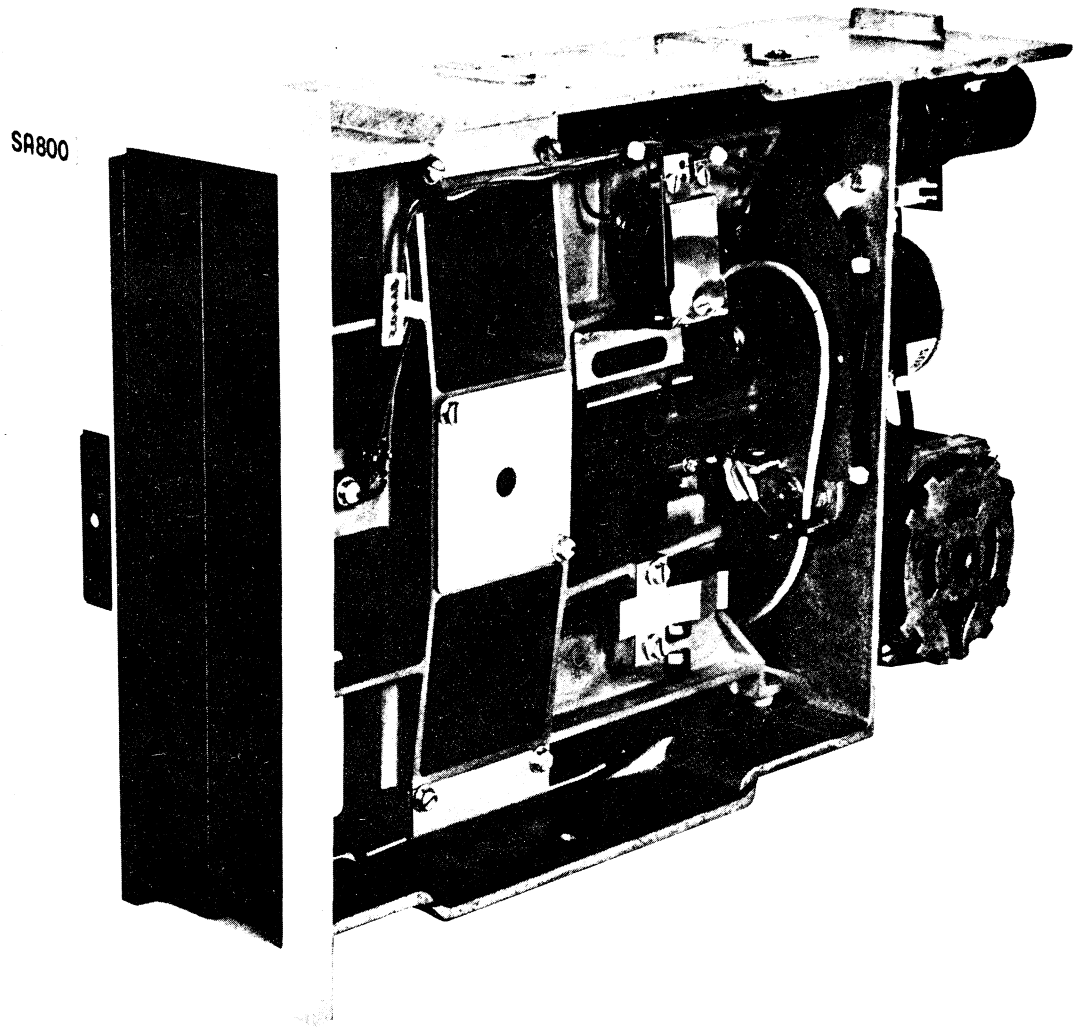


Figure 1. SA800/801 Diskette Storage Drive

1.0 INTRODUCTION

1.1 General Description

The SA800/801 are enhanced versions of the successful SA900/901 Diskette Storage Drive. The SA800/801 provides the customer with a mature and reliable product, manufactured to the same high standard of excellence as the 900/901, but with additional featuress.

The SA800 Diskette Storage Drive can read and write diskettes for interchange with other SA800's, the SA900, IBM 3741, 3742 or 3540 and with the IBM System 32.

The SA801 provides the same features as the SA800 with additional flexibility for those requirements which preclude IBM compatibility.

The SA800/801 Diskette Storage Drives have as standard features: a patented diskette clamping/registration design which eliminates the possibility of damage to the diskette due to misregistration and quarantees over 30,000 interchanges with each diskette; single and double density capability on the same drive for the same price; a proprietary ceramic R/W head designed and manufactured by Shugart Associates to provide media life exceeding 3.5 million passes/track and head life exceeding 15,000 hours; an activity light which indicates drive in use; and ribbon cable or twisted pair connector for ease of packaging. All of these features and more are available with the SA800/801.

SA800/801 Diskette Storage Drive provide the system designer solutions to his applications requirements with greater performance and reliability than cassette or cartridge drives, and lower cost with increased function over I/O and reel-to-reel tape drives.

Applications for the SA800/801 Diskette Storage Drive are key entry systems, point of sale recording systems, batch terminal data storage microprogram load and error logging, minicomputer program and auxiliary data storage, word processing systems and data storage for small business systems.

The SA100 Diskette, IBM Diskette or equivalent, can be read and written interchangeably between any SA800 and IBM 3741/42, 3747 and 3540. The SA101 Diskette can be read or written interchangeably on any SA801. The SA102 and SA103 are used for double density applications.

As a product enhancement, to improve reliability and serviceability, Shugart is incorporating into the SA800 serves drives a PCB Large Scale Integration (LSI) components. These components are:

- *Control Chip*
- *Write Channel*
- *Read Channel*

The LSI Control chip performs the following functions:

- *TRK 00 detector*
- *Index detector*
- *Stepper logic*
- *FM clock/data separator and data window*
- *Sector separator*
- *Write Protect detector*
- *Door open/close detector*
- *Disk change circuit*
- *Ready signal*

The functions listed above are either detected from the drive mechanics or from the Host Interface. As a result, the proper logic generated by the LSI chip either will be used within the drive electronic circuit to perform stepping, read/write operations or will be fed back to the Host Interface.

Also, an internal FM data separator is incorporated inside the chip. A jumper option will allow the user to select the data separator to perform as its predecessor SA800 (jumper FS) or to select the separator to be compatible with the IBM System 3740 data separator (jumper TS). Thus IBM compatibility will allow direct interfacing with LSI single chip floppy disk controllers.

1.2 Specification Summary

1.2.1 Performance Specifications

	Single Density	Double Density
Capacity		
Unformatted		
Per Disk	3.2 megabits	6.4 megabits
Per Track	41.7 kilobits	83.4 kilobits
IBM Format		
Per Disk	2.0 megabits	n/a
Per Track	26.6 kilobits	n/a
Tranfer Rate	250 kilobits/sec.	500 kilobits/sec
Latency (average)	83 ms	83 ms
Access Time		
Track to Track	8 ms	8 ms
Average	260 ms	260 ms
Settling Time	8 ms	8 ms
Head Load Time	35 ms	35 ms

1.2.2 Functional Specifications

	Single Density	Double Density
Rotational Speed	360 rpm	360 rpm
Recording Density		
(inside track)	3200 bpi	6400 bpi
Flux Density	6400 fci	6400 fci
Track Density	48 tpi	48 tpi
Tracks	77	77
Physical Sectors		
SA800	0	0
SA801	32/16/8	32/16/8
Index	1	1
Encoding Method	FM	MFM/M^{2}FM
Media Requirements		
SA800	SA100/IBM Diskette	SA102/IBM Diskette
SA801	SA101	SA103

1.2.3 Physical Specifications

Enviromental Limits	**Operating**	**Shipping**	**Storage**
Ambient Temperature	= 40°F to 115°F (4.4° to 46.1°C)	-40°F to 144°F	-8°F to 117°F
Relative Humidity	= 20% to 80%	1 to 95%	1 to 95%
Maximum Wet Bulb	= 78°F (25°C)	No Condensation	No Condensation

AC Power Requirements
50/60 Hz ± 0.5 Hz
100/115 VAC Installations = 85 to 127V @ .3A typical
200/230 VAC Installations = 170 to 253V @ .18A typical

DC Voltage Requirements
+24 VDC ±5% 1.3A typical
+ 5 VDC ±5% 0.8A typical
-5 VDC ±5%.05A typical (option -7 to -16 VDC)

Mechanical Dimensions (Reference Figures 18 and 20)
Width = 4 5/8 in. (11.75 cm)
Height = 9 1/2 in. (24.13 cm)
Depth = 14 1/4 in. (36.20 cm)
Weight = 13.0 lbs. (5.91 kg)

Heat Dissipation = 271 BTU/hr. typical (80 Watts)

1.2.4 Reliability Specifications

MTBF:	5000 POH under heavy usage 8000 POH under typical usage
PM:	Every 5000 POH under heavy usage Every 15,000 under typical usage
MTTR:	30 minutes
Component Life:	15,000 POH
Error Rates:	
Soft Read Errors:	1 per 10^9 bits read
Hard Read Errors:	1 per 10^{12} bits read
Seek Errors:	1 per 10^6 seeks.
Media Life:	
Passes Per Track	3.5×10^6
Insertions:	30,000 +

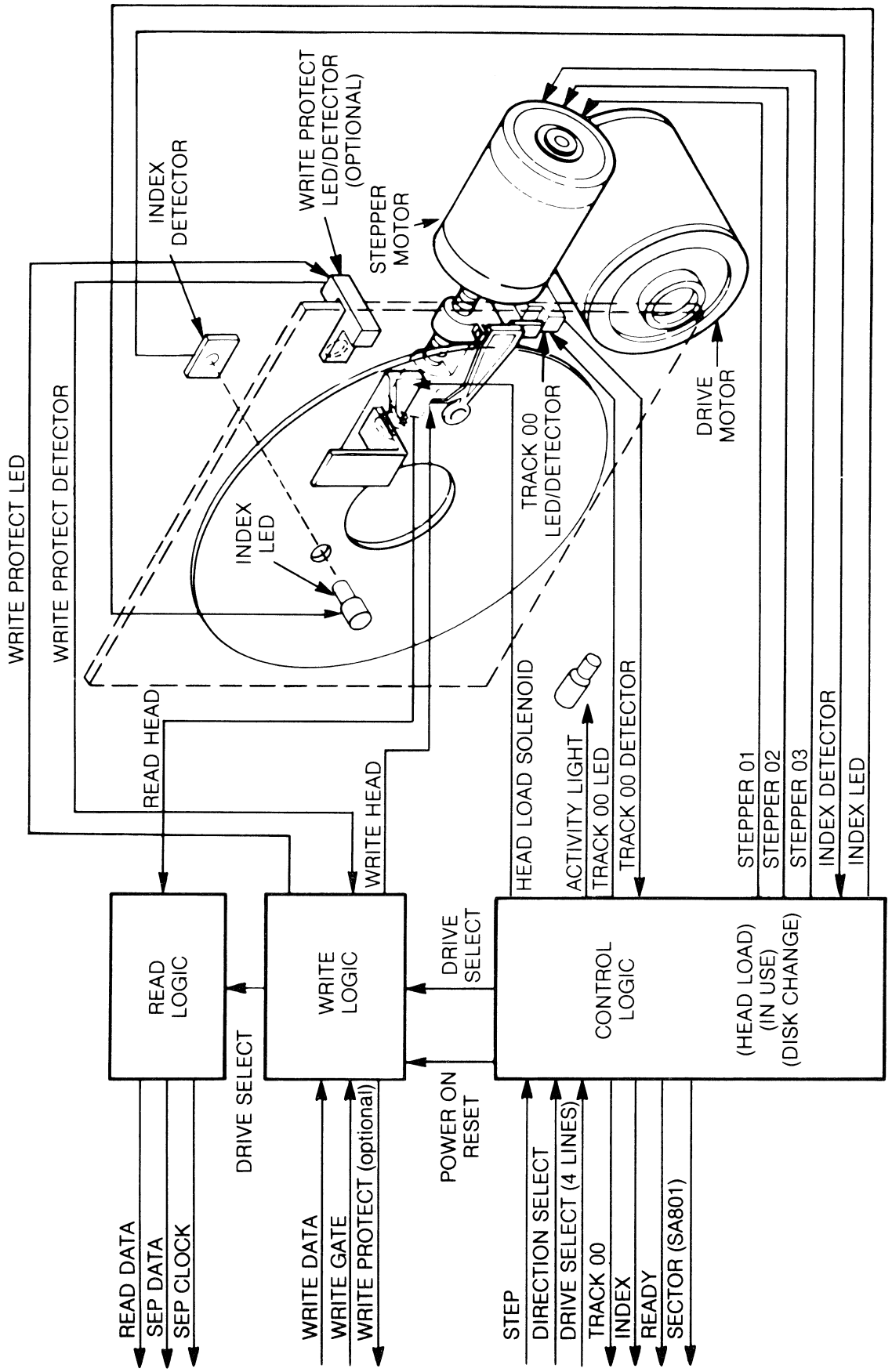


Figure 2. SA800/801 Functional Diagram

2.0 FUNCTIONAL CHARACTERISTICS

2.1 General Operation

The SA800/801 Diskette Storage Drive consists of read/write and controls electronics, drive mechanism, read/write head, track positioning mechanism, and the removable diskette. These components perform the following functions:

Interpret and generate control signals.
Move read/write head to the selected track.
Read and write data.

The relationship and interface signals for the internal functions of the SA800/801 are shown in Figure 2.

The Head Positioning Actuator positions the read/write head to the desired track on the diskette. The Head Load Actuator loads the diskette against the read/write head and data may then be recorded or read from the diskette.

2.2 Read/Write and Control Electronics

The electronics are packaged on one PCB. The PCB contains:

1. Index Detector Circuits. (Sector/Index for 801).
2. Head Position Actuator Driver.
3. Head Load Actuator Driver.
4. Read/Write Amplifier and Transition Detector.
5. Data/Clock Separation Circuits.
6. Write Protect.
7. Drive Ready Detector Circuit.
8. Drive Select Circuits.

2.3 Drive Mechanism

The Diskette drive motor rotates the spindle at 360 rpm through a belt-drive system. 50 or 60 Hz power is accommodated by changing the drive pulley and belt. A registration hub, centered on the face of the spindle, positions the Diskette. A clamp that moves in conjunction with the cartridge guide fixes the Diskette to the registration hub.

2.4 Positioning Mechanism

An electrical stepping motor (Head Position Actuator) and lead screw positions the read/write head. The stepping motor rotates the lead screw clockwise or counterclockwise in 15° increments. A 15° rotation of the lead screw moves the read/write head one track position. The using system increments the stepping motor to the desired track.

2.5 Read/Write Head

The SA800/801 head is a single element ceramic read/write head with straddle erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal to noise ratio and insures Diskette interchangeability.

The read/write head is mounted on a carriage which is located on the Head Position Actuator lead screw. The Diskette is held in a plane perpendicular to the read/write head by a platen located on the base casting. This precise registration assures perfect compliance with the read/write head. The Diskette is loaded against the head with a load pad actuated by the head load solenoid.

The read/write head is in direct contact with the Diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the Diskette with minimum head/Diskette wear.

2.6 Recording Format

The format of the data recorded on the disk is totally a function of the host system, and can be designed around the users application to best take advantage of the total available bits that can be written on any one track.

For a detailed discussion of various recording formats, the systems designer should read one of the following:

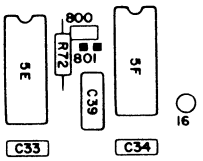
1. IBM Compatibility Manual.
2. Shugart Associates Double Density Design Guide.
3. SA801/901 Track Formats.

2.7 Optional Features

1. -12 to -15 Volt DC to replace -5 Volt DC requirement.
2. Dust Cover, Not available on "R"series.
3. Write Protect for SA800. Standard on SA801.
4. Door Lock. Will lock the door when drive is selected or through alternate I/O pin.
5. Horizontal mounting with door opening up.
6. SA800/801 "R" Series. Allows two drives to be horizontally installed in a standard 19" Retma rack. Reference figure 20.

2.8 Model Differences

800-1 - Soft Sectored with an FM (single density) data separator.
800-2 - Soft Sectored without data separator.
800-4 - Mechanics only (No PCB).
801 - Hard Sectored with an FM (single density) data separator and sector separator.



NOTE:

To convert a 801 to a 800 move the shorting plug from the 801 position to the 800 position. A 800 cannot be converted to a 801.

3.0 FUNCTIONAL OPERATIONS

3.1 Power Sequencing

Applying AC and DC power to the SA800/801 can be done in any sequence, however, once AC power has been applied, a 2 second delay must be introduced before any Read or Write operation is attempted. This delay is for stabilization of the Diskette rotational speed. Also, after application of DC power, a 90 millisecond delay must be introduced before a Read, Write, or Seek opration or before the control output signals are valid. After powering on, initial position of the R/W head with respect to data tracks is indeterminant. In order to assure proper positioning of the R/W head prior to any read/write operation after powering on, a Step Out operation should be performed until the Track 00 indicator becomes active.

3.2 Drive Selection

Drive selection occurs when a drive's Drive Select line is activated. Only the drive with this line active will respond to input lines or gate output lines. Under normal operation, the Drive Select line will load the R/W head, apply power to the stepper motor, enable the input lines, activate the output lines and light the Activity LED on the front of the drive. Optional modes of operation are available. Reference section 7 for these user installable features.

3.3 Track Accessing

Seeking the R/W head from one track to another is accomplished by:

a. Activating Drive Select line.
b. Selecting desired direction utilizing Direction Select line.
c. Write Gate is being inactive.
d. Pulsing the Step line.

Multiple track accessing is accomplished by repeated pulsing of the Step line until the desired track has been reached. Each pulse on the Step line will cause the R/W head to move one track either in or out depending on the Direction Select line. Head movement is initiated on the trailing edge of the Step Pulse.

3.3.1 Step Out

With the Direction Select line at a plus logic level (2.5V to 5.25V) a pulse on the Step line will cause the R/W head to move one track away from the center of the disk. The pulse(s) applied to the Step line and Direction Select line must have the timing characterisitics shown in Figure 3.

3.3.2 Step In

With the Direction Select line at a minus logic level (0V to .4V), a pulse on the Step line will cause the R/W head to move one track closer to the center of the disk. The pulse(s) applied to the Step line must have the timing characterisitics shown in Figure 3.

3.4 Read Operation

Reading data from the SA800/801 Diskette Storage drive is accomplished by:

a. Activating Drive Select line.
b. Write Gate being inactive.

The timing relationships required to initiate a read sequence are shown in Figure 4. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to reading.

The timing of the read signals, Read Data, Separated Data, and Separated Clock are shown in Figure 5.

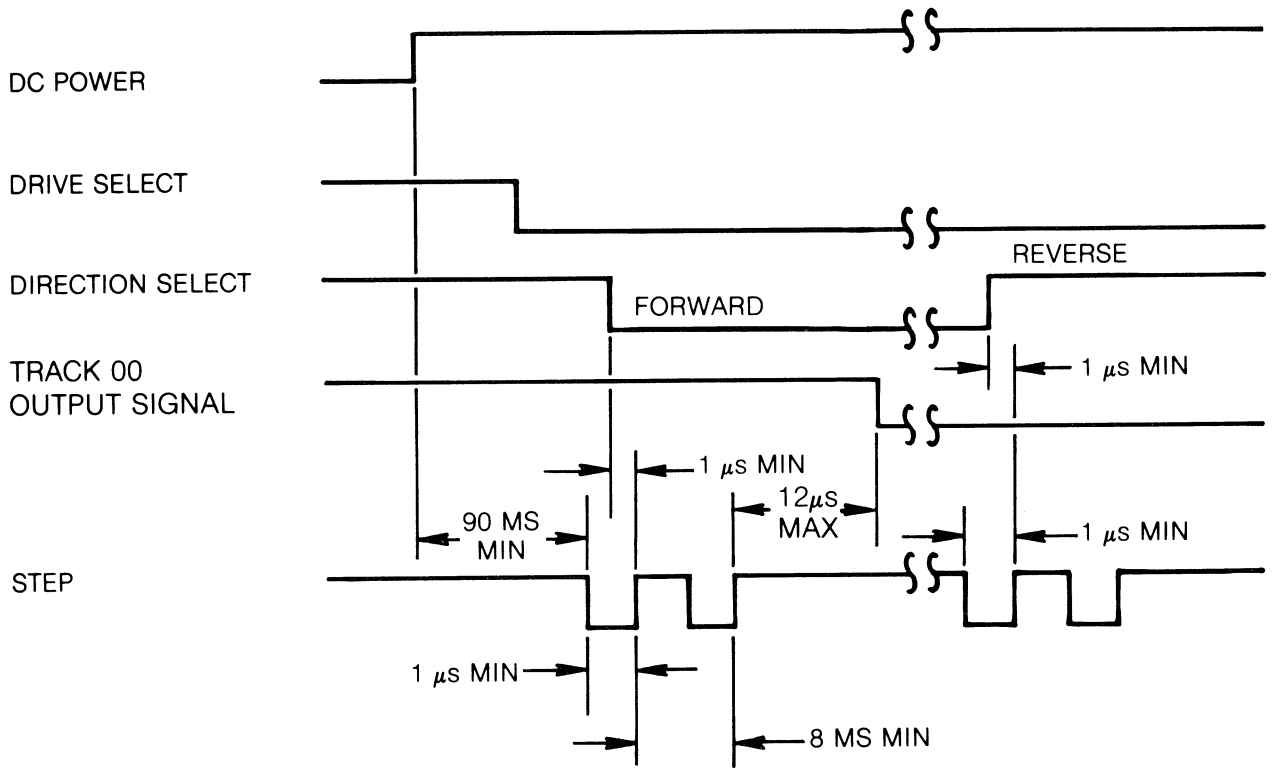
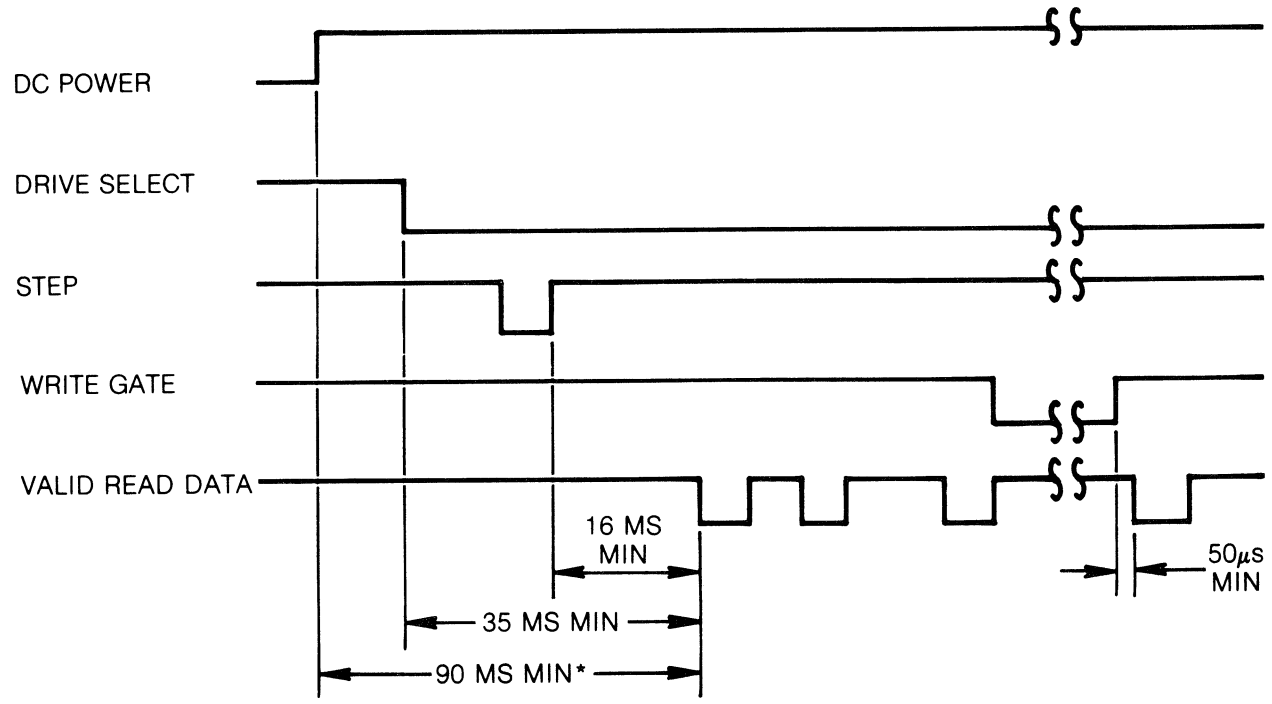
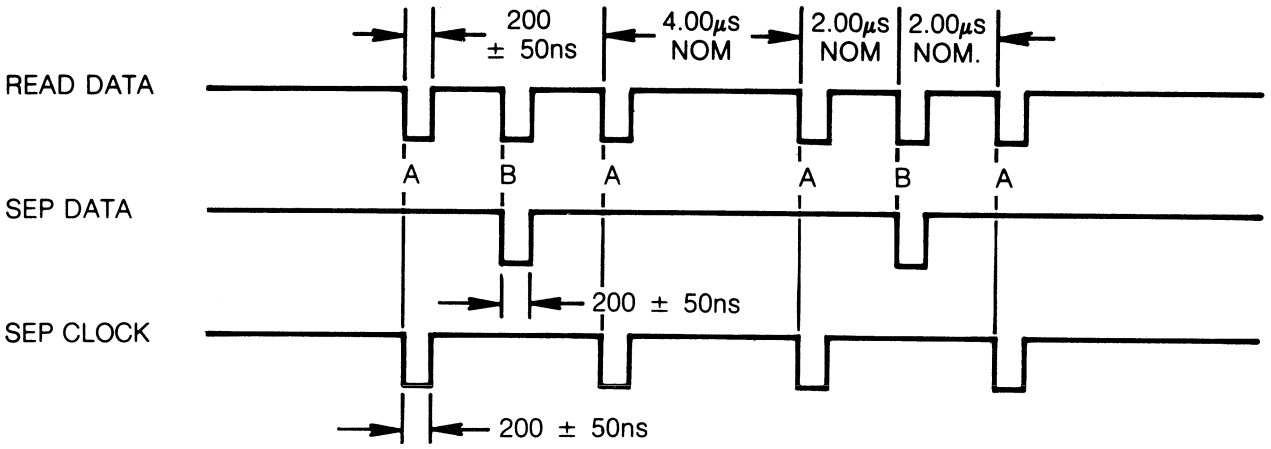


Figure 3. Track Access Timing



* 2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME

Figure 4. Read Initiate Timing



A = LEADING EDGE OF BIT MAY BE ± 400 ns FROM ITS NOMINAL POSITION.
B = LEADING EDGE OF BIT MAY BE ± 200 ns FROM ITS NOMINAL POSITION.

Figure 5. Read Signal Timing

3.5 Write Operation

Writing data to the SA800/801 is accomplished by:

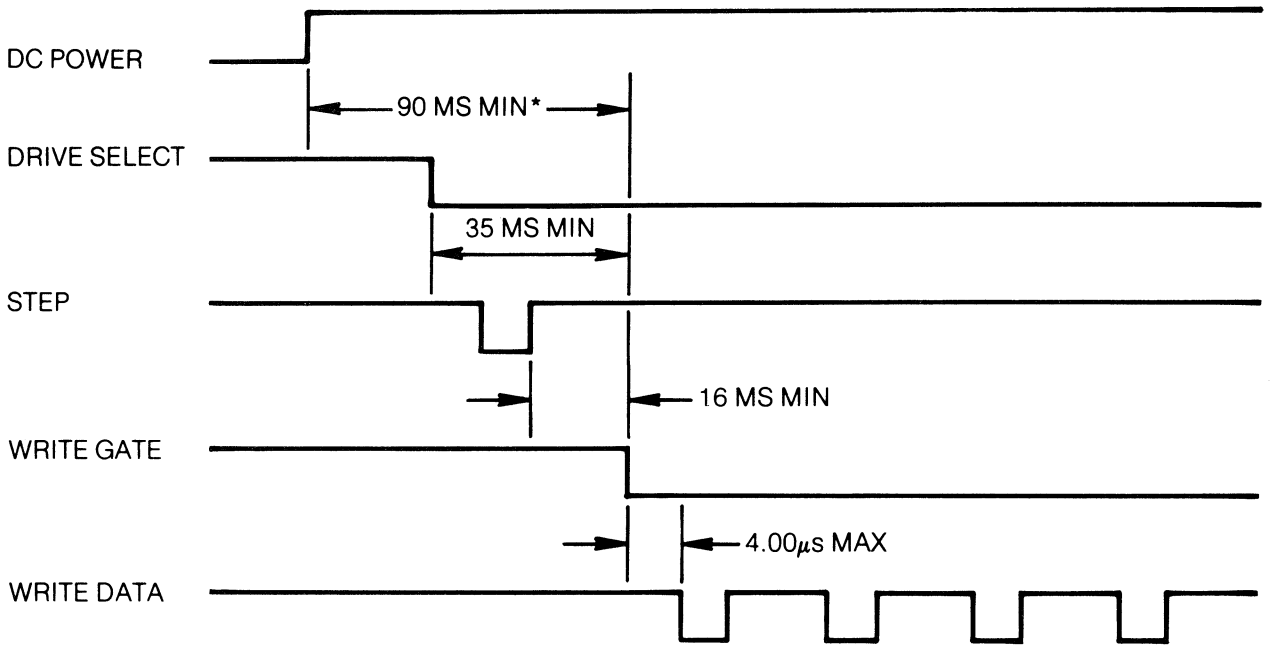
a. Activating the Drive Select line.
b. Activating the Write Gate line.
c. Pulsing the Write Data line with the data to be written.

The timing relationships required to initiate a write data sequence are shown in Figure 6. These timing specifications are required in order to guarantee that the R/W head position has stabilized prior to writing.

The timing specifications for the Write Data pulses are shown in Figure 7.

3.6 Sequence of Events

The timing diagram shown in Figure 8 shows the necessary sequence of events with associated timing restrictions for proper operation.



* 2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME.

Figure 6. Write Initiate Timing

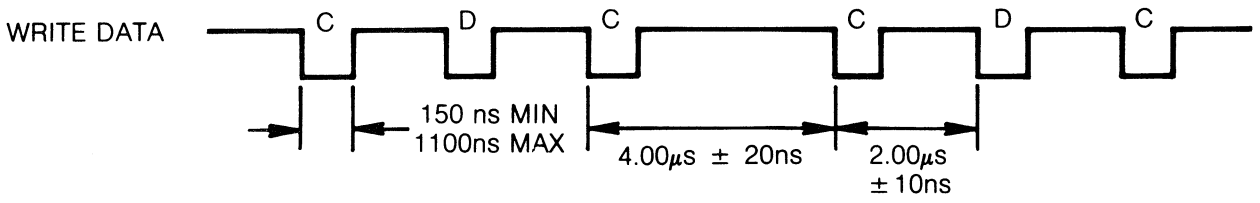
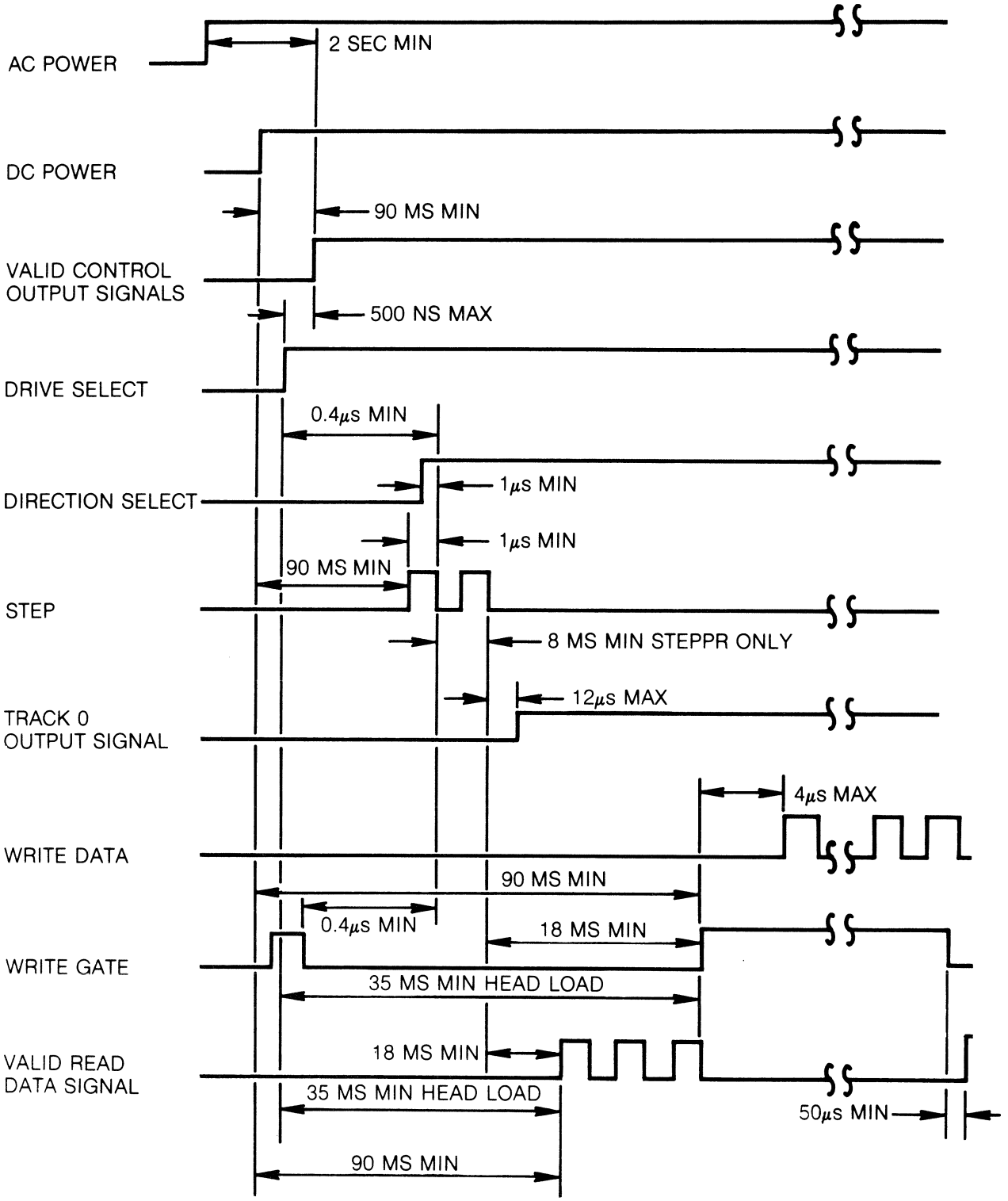


Figure 7. Write Data Timing



NOTE 1: 35ms minimum delay must be introduced after Drive Select to allow for proper head load settling. If stepper power is to be applied independent of Head Load, than and 8ms minimum delay must be introduced to allow for stepper settling.

General Control and Data Timing Requirements

4.0 ELECTRICAL INTERFACE

The interface of the SA800/801 Diskette drive can be divided into two categories:

1. Signal
2. Power

The following sections provide the electrical definition for each line.

Reference Figure 9 for all interface connections.

4.1 Signal Interface

The signal interface consists of two categories:

1. Control
2. Data Transfer

All lines in the signal interface are digital in nature and either provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

4.1.1 Input Lines

There are ten signal input lines, eight are standard and two are user installable options (reference section 7).

The input signals are of two types, those intended to be multiplexed in a multiple drive system and those which will perform the multiplexing. The input signals to be multiplexed are:

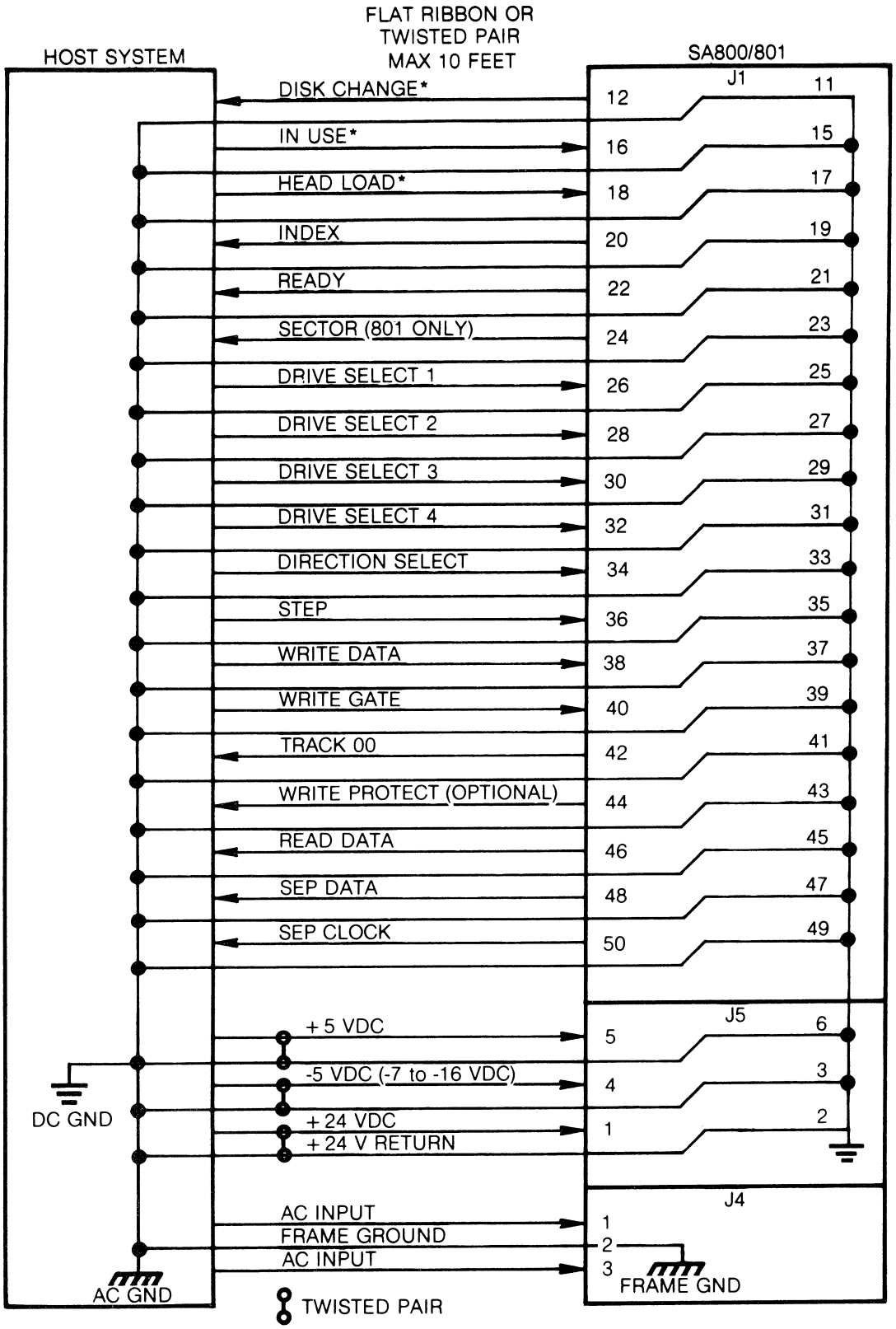
1. Direction Select
2. Step
3. Write Data
4. Write Gate

The input signals which are intended to do the multiplexing are:

1. Drive Select 1
2. Drive Select 2
3. Drive Select 3
4. Drive Select 4

The input lines have the following electrical specifications. Reference Figure 10 for the recommended circuit.

True = Logical zero = Vin ± 0.0V to + 0.4V
@ Iin = 40 ma (max)
False = Logical one = Vin + 2.5V to + 5.25V
@ Iin = 0 ma (open)
Input Impedence = 150 ohms



NOTE: Not shown are 5 of the 9 Alternate I/O connections. The connections for these lines are on pins 2, 4, 6, 8, 10 and 14. Signal return for these lines are on pins 1, 3, 5, 7, 9 and 13 respectively. Reference Section 7 for uses of these lines.

*These lines are alternate input/output lines and they are enabled by jumper plugs. Reference Section 7 for uses of these lines.

Figure 9. Interface Connections

4.1.1 Input Line Termination

The SA800/801 has been provided with the capability of terminating the four input lines, which are meant to be multiplexed, by jumpering traces. The four lines and their respective jumpering traces are:

1. Direction Select ..... Trace "T3"
2. Step ..... Trace "T4"
3. Write Data ..... Trace "T5"
4. Write Gate ..... Trace "T6"

In order for the drive to function properly, the last drive on the interface must have these four lines terminated. Termination of these four lines can be accomplished by either of two methods.

1. As shipped from the factory, jumpers are installed on the terminator posts T3, T4, T5, and T6. Remove these shorting plugs from all drives except the last one on the Interface.

2. External termination may be used provided the terminator is beyond the last drive. Each of the four lines should be terminated by using a 150 ohm, ¼ watt resistor, pulled up to + 5 VDC.

4.1.1.2 Drive Select 1-4

Drive Select when activated to a logical zero level, activates the multiplexed I/O lines and loads the R/W head. In this mode of operation only the drive with this line active will respond to the input lines and gate the output lines.

Four separate input lines, Drive Select 1, Drive Select 2, Drive Select 3, and Drive Select 4, are provided so that up to four drives may be multiplexed together in a system and have separate Drive Select lines. Traces 'DS1', 'DS2', 'DS3', and 'DS4' have been provided to select which Drive Select line will activate the interface signals for a unique drive. As shipped from the factory, a shorting plug is installed on 'DS1'. To select another Drive Select line, this plug should be moved to the appropriate 'DS' pin. For additional methods of selecting drives, see section 7.1.

4.1.1.3 Direction Select

This interface line is a control signal which defines direction of motion the R/W head will take when the Step line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the Step line the R/W head will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero level, the direction
of motion is defined as "in" and if a pulse is applied to the step line, the R/W head will move towards the center of the disk.

4.1.1.4 Step

This interface line is a control signal which causes the R/W head to move with the direction of motion as defined by the Direction Select line.

The access motion is initiated on each logical zero to logical one transition, or the trailing edge of the signal pulse. Any change in the Direction Select line must be made at least 1 μs before the trailing edge of the Step pulse. The read/write head may be prevented from stepping past track 00 by using the "NFO" trace option on LSI PCB. Refer to Figure 3 for these timings. **Note:** When going from a reverse seek to a forward seek or vice versa and additional 8 ms delay must be induced before changing direction.

4.1.1.5 Write Gate

The active state of this signal, or logical zero, enables Write Data to be written on the diskette. The inactive state, or logical one, enables the read data logic (Separated Data, Separated Clock, and Read Data) and stepper logic. Refer to Figure 6 for timings.

4.1.1.6 Write Data

This interface line provides the data to be written on the diskette. Each transition from a logical one level to a logical zero level, will cause the current through the R/W head to be reversed thereby writing a data bit. This line is enabled by Write Gate being active. Refer to Figure 7 for timings.

4.1.1.7 Head Load (Alternate Input)

This customer installable option, when enabled by jumpering Trace 'C' and activated to a logical zero level and the diskette access door is closed, will load the R/W head load against the diskette. Refer to section 7 for uses and method of installation.

4.1.1.8 In Use (Alternate Input)

This customer installable option, when enabled by jumpering Trace 'D' and activated to a logical zero level will turn on the Activity LED in the door push button. This signal is an "OR" function with Drive Select. Refer to section 7.8 for uses and method of installation.

4.1.2 Output Lines

There are six standard and one optional output lines from the SA800, and eight output lines from the SA801. Also, there is one Alternate Output available from the drive. The output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at a logical level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is off and the collector current is a maximum of 250 microamperes.

Refer to Figure 10 for the recommended circuit.

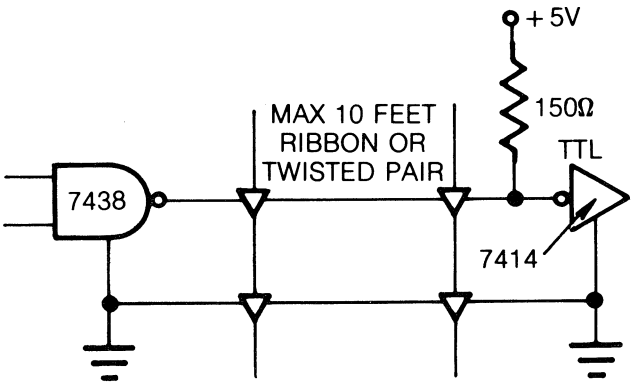


Figure 10. Interface Signal Driver/Receiver

4.1.2.1 Track 00

The active state of this signal, or a logical zero indicates when the drives R/W head is positioned at track zero (the outermost track) and the access circuitry is driving current through phase one of the stepper motor. This signal is at a logical one level, or false state, when the selected drives R/W head is not at track 00.

4.1.2.2 Index

This interface signal is provided by the drive once each revolution of the diskette (166.67 ms) to indicate the beginning of the track. Normally this signal is a logical one and makes the transition to the logical zero level for a period of 1.7 ms (0.4 ms on SA801) once each revolution. The timing for this signal is shown in Figure 11.

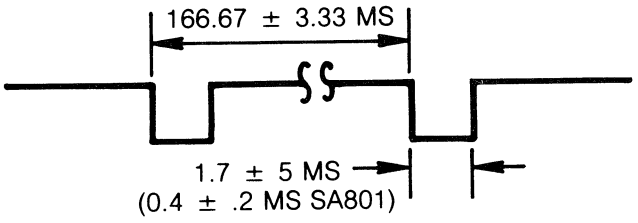


Figure 11. Index Timing

To correctly detect Index at the Host Index should be false at Drive Select time, that is, the Host should see the transition from false to true after the drive has been selected.

For additional methods of detecting Index, refer to section 7.6.

4.1.2.3 Sector (SA801 only)

This interface signal is provided by the drive 32 times each revolution. Normally, this signal is a logical one and makes the transition to a logical zero for a period of 0.4 ms each time a sector hole on the Diskette is detected. Figure 12 shows the timing of this signal and its relationship to the Index pulse.

For additional methods of detecting Sector refer to section 7.7.

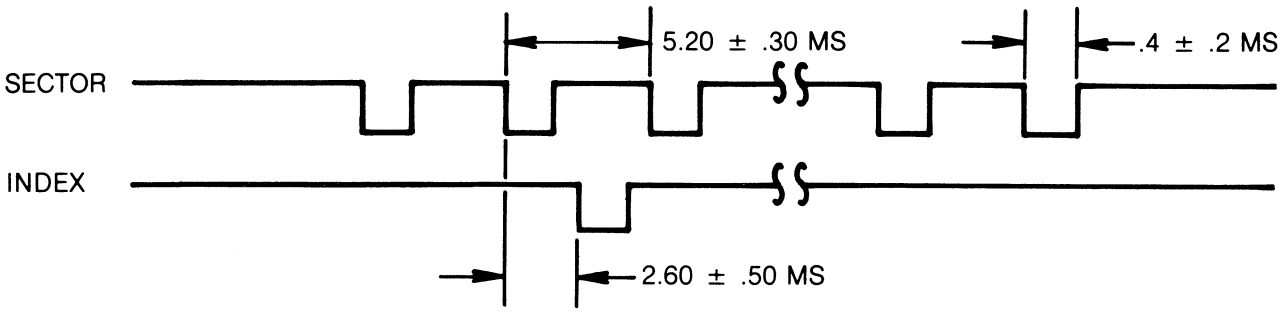


Figure 12. Sector Timing

4.1.2.4 Ready

This interface signal indicates that two index holes have been sensed after properly inserting a diskette and closing the door, or that two index holes have been sensed following the application of +5V power to the drive.

For additional methods of using the Ready line, refer to section 7.5.

4.1.2.5 Read Data

This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing and bit shift tolerance within normal media variations.

4.1.2.6 Sep Data

This interface line furnishes the data bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing. This line is available on the SA801 and 800 Model 1.

4.1.2.7 Sep Clock

This interface line furnishes the clock bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing. This line is available on the SA801 and 800 Model 1 and PCB 25136.

NOTE: True separation internally inserting up to three missing clock bits to maintain synchronization, is available on the LSI PCB by using trace option "TS".

4.1.2.8 Write Protect (Optional on SA800)

This interface signal is provided by the drive to give the user an indication when a Write Protected Diskette is installed. The signal is logical zero level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition of notifying the interface.

For other methods of using Write Protect, refer to section 7.9.

4.1.2.9 Disk Change (Alternate Output)

Reference section 7.10.

4.1.3 Alternate I/O Pins

These interface pins have been provided for use with customer installable options. Refer to section 7 for methods of use.

4.2 Power Interface

The SA800/801 Diskette Storage Drive requires both AC and DC power for operation. The AC power is used for the spindle drive motor and the DC power is used for the electronics and the stepper motor.

4.2.1 AC Power

The AC power to the drive is via the connector P4/J4 located to the rear of the drive and below the AC motor capacitor. The P4/J4 pin designations are outlined below for standard as well as optional AC power.

P4 PIN	60 Hz		50 Hz	
	115 V (Standard)	208/230 V	110V	220V
1	85-127 VAC	170-253 VAC	85-127 VAC	170-253 VAC
2	Frame Gnd	Frame Gnd	Frame Gnd	Frame Gnd
3	85-127 V Rtn	170-253 V Rtn	85-127 V Rtn	170-253 V Rtn
MAX CURRENT	0.35 Amps	0.23 Amps	0.35 Amps	0.23 Amps
FREQ TOLERANCE	± 0.5 Hz		± 0.5 Hz	

4.2.2 DC Power

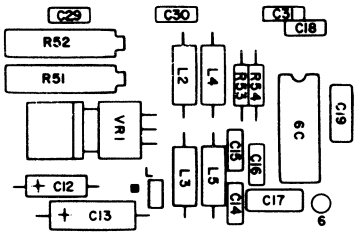
DC power to the drive is via connector P5/J5 located on non-component side of PCB near the P4 connector. The three DC voltages and their specifications along with their P5/J5 pin designators, are outlined below.

P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+ 24 VDC	± 1.2 VDC	1.7 A Max** 1.3 A Typ	100 mv
2	+ 24 V Return*			
3	- 5 V Return			
4	- 5 VDC	± 0.25 VDC	0.07 A Max 0.05 A Typ	50 mv
	Optional -7 to -16 VDC (trace 'L')***	NA	0.10 A Max 0.07 A Typ	NA
5	+ 5 VDC	± 0.25 VDC	1.0 A Max 0.8 A Typ	50 mv
6	+ 5 V Return			

*The + 24 VDC power requires a separate ground return line. It, and all other DC grounds must be connected together at the power supply. One line from this common DC connection must go to one common Frame Ground connection near the power supply.

**If either customer installable option described in sections 7.2 and 7.4 are used, the current requirement for the + 24 VDC is a multiple of the maximum of + 24V current times the number of drives on the line.

***If the shorting plug is in the vertical position the -7 to -16 VDC option can be used. If the shorting plug is in the horizontal position, -5 VDC must be used.



5.0 PHYSICAL INTERFACE

The electrical interface between the SA800/801 and the host system is via three connectors. The first connector, J1, provides the signal interface; the second connector, J5, provides the DC power; and the third conector, J4, provides the AC power and frame ground.

This section describes the physical connectors used on the drive and the recommended connectors to be used with them. Refer to Figure 16 for connector locations.

5.1 J1/P1 Connector

Connection to J1 is through a 50 pin PCB edge card connector. The dimensions for this connector are shown in Figure 13. The pins are numbered 1 through 50 with the even numbered pins on the component side of the PCB and the odd numbered pins on the non-component side. Pin 2 is located on the end of the PCB connector closest to the AC motor capacitor and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying.

The recommended connectors for P1 are tabulated below.

TYPE OF CABLE	MANUFACTURER	CONNECTOR P/N	CONTACT P/N
Twisted Pair, #26 (crimp or solder)	AMP	1-583717-1	583616-5 (crimp) 58354-3 (solder)
Twisted Pair, #26 (solder term.)	VIKING	3VH25/1JN-5	NA
Flat Cable	3M "Scotchflex"	3415-0001	NA

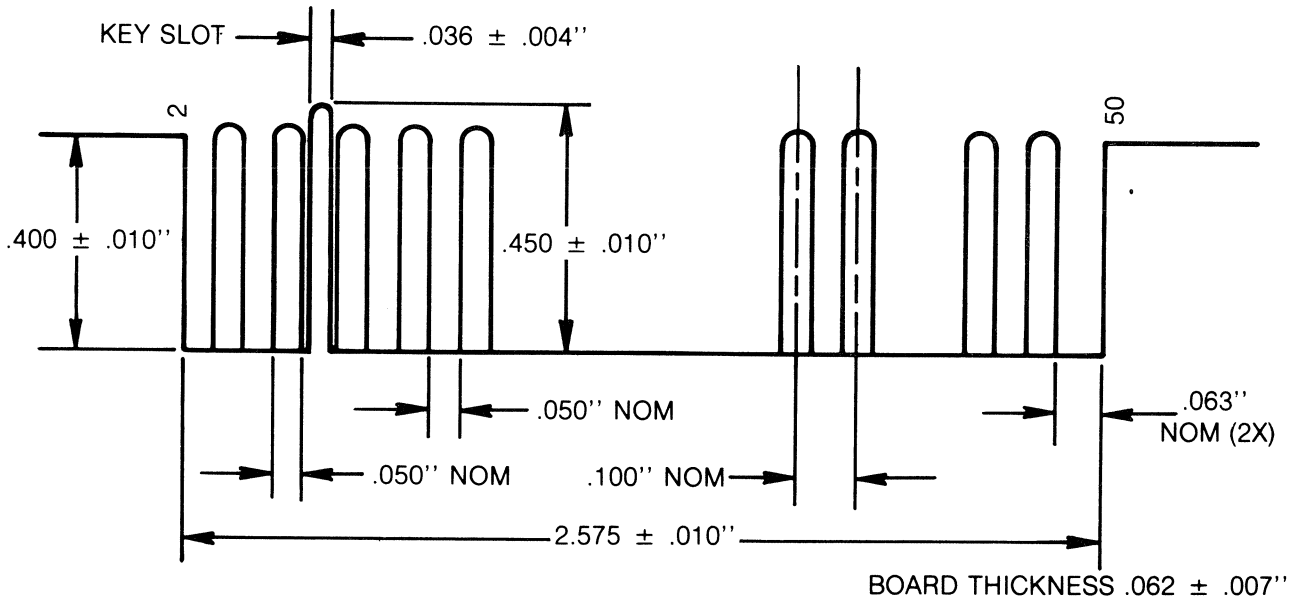


Figure 13. J1 Connector Dimensions

5.2 J5/P5 Connector

The DC power connector, J5, is mounted on the non-component side of the PCB and is located below the AC motor capacitor. J5 is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0. The recommended mating connector (P5) is AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. J5 pins are labeled on the component side of the PCB with pin 5 located nearest J1/P1. Figure 14 illustrates J5 connector as seen on the drive PCB from non-component side.

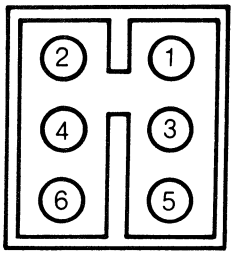


Figure 14. J5 Connector

5.3 J4/P4 Connector

The AC power connector, J4 is mounted on the AC motor capacitor bracket and is located just below the capacitor. J4 connector is a 3 pin connector AMP P/N 1-480305-0 with pins P/N 60620-1. The recommended mating connector (P4) is AMP P/N 1-480303-0 or 1-480304-0 both utilizing pins P/N 60619-1. Figure 15 illustrates J4 connector as seen from the rear of the drive.

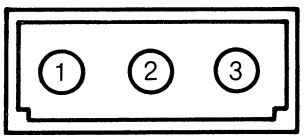


Figure 15. J4 Connector

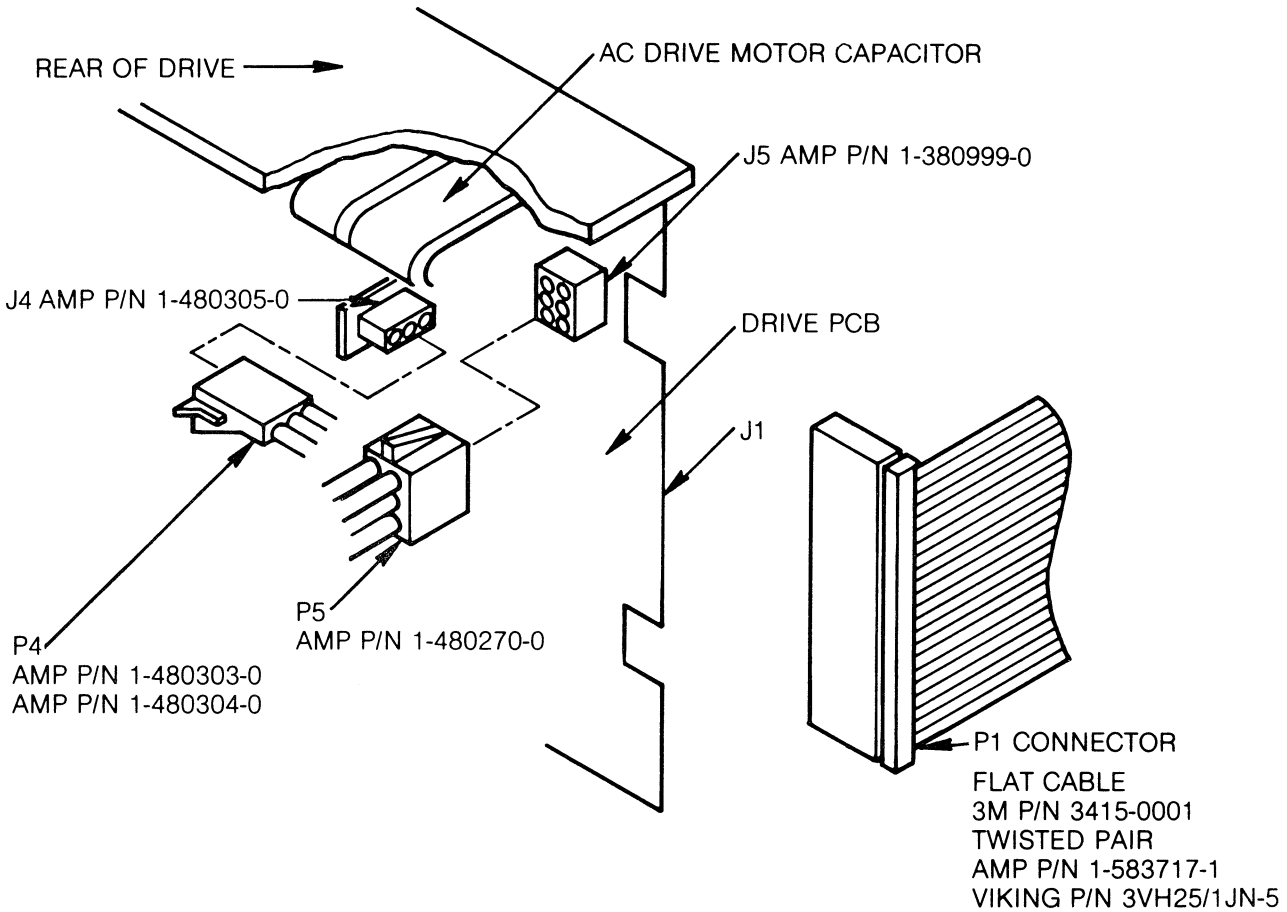


Figure 16. Interface Connectors - Physical Location Diagram

6.0 DRIVE PHYSICAL SPECIFICATIONS

This section describes the mechanical dimensions and mounting recommendations for the SA800/801.

6.1 Drive Dimensions

Reference Figure 18 for dimensions of the SA800/801.

6.2 Mounting Recommendations

The SA800/801 is capable of being mounted in one of the following positions:

1. Vertical-Door opening to the left or right.
2. Horizontal-Door opening up or down.
3. Upright-Door opening towards the front or rear.

6.2.1 Vertical Mounting

The drive, as shipped from the factory, is ready to be mounted in the vertical position, door opening left or right, without any adjustments.

Horizontal Mounting

If the drive is to be mounted horizontally with the door opening down (PCB up), the head load actuator return spring must be repositioned to compensate for gravity. Reference Figure 17 for the proper spring position on the actuator.

If the door is to open up (PCB down), it must be specified when ordering. This feature provides a heavier door opening spring. In addition, the head load actuator return spring will be repositioned to compensate for gravity. Reference Figure 17 for the proper position for the spring on the actuator.

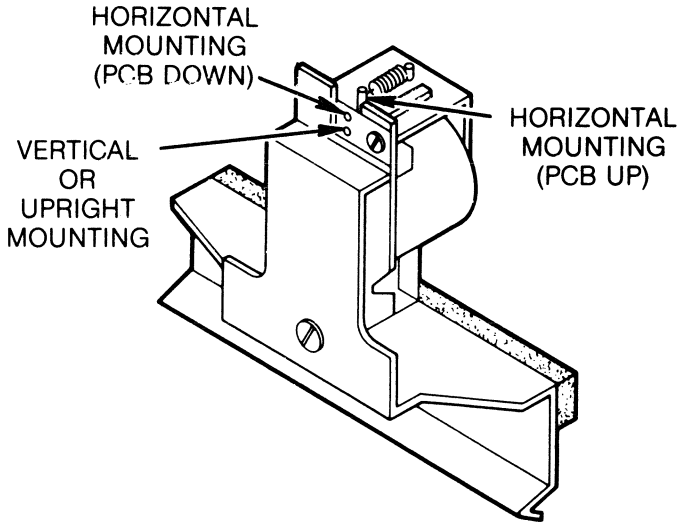


Figure 17. Head Load Actuator Mounting Prerequisites

6.2.3 Upright Mounting

If the Drive is to be mounted in the upright position (IBM 3740 fashion), the spring hook attached to the eject mechanism must be removed and then attach the eject spring to the place the hook was on.

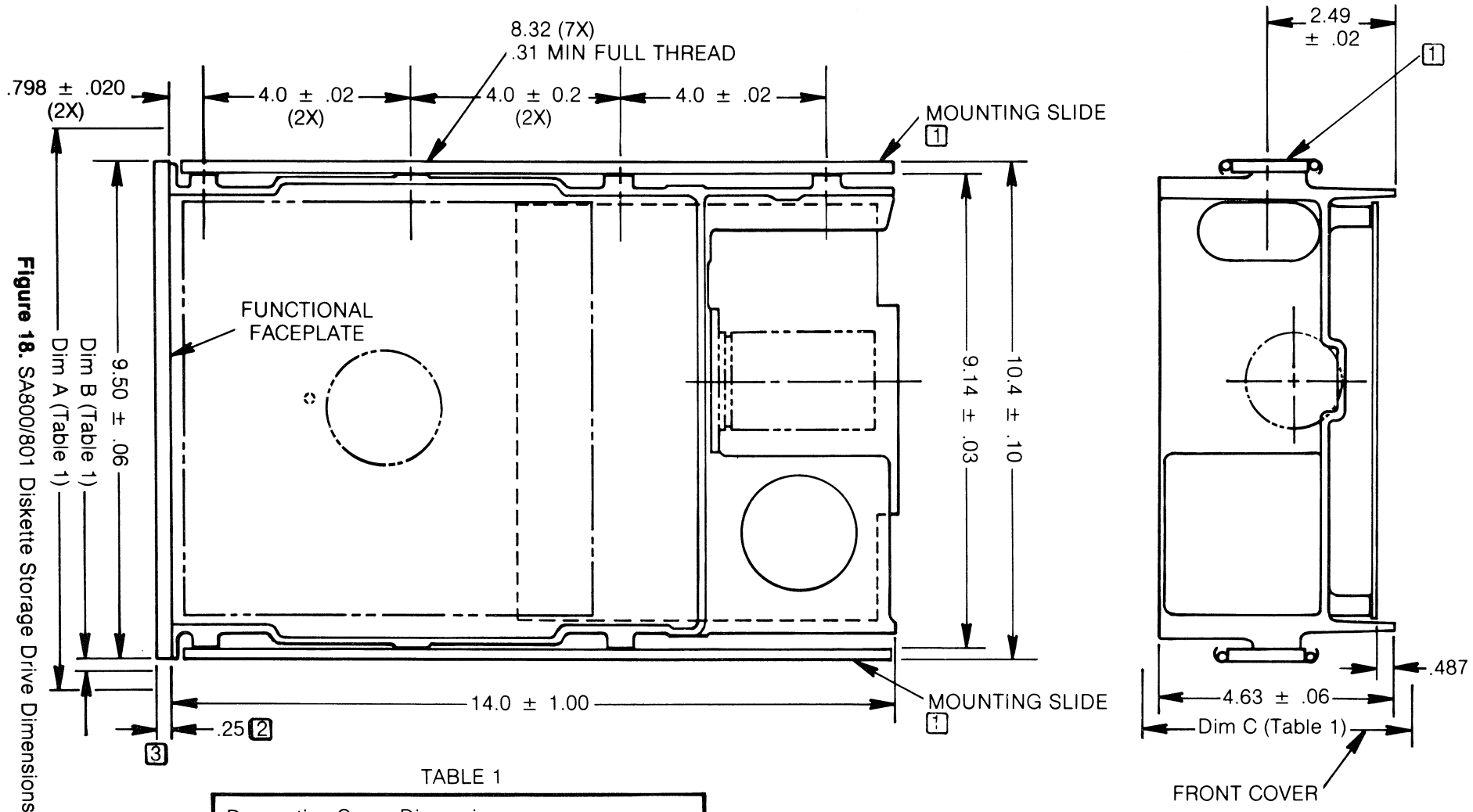


Figure 18. SA800/801 Diskette Storage Drive Dimensions

TABLE 1

Decorative Cover Dimensions			
Cover Size	Dim A	Dim B	Dim C
4-5/8 × 10-1/2	10.50	.240	4.62
5-1/4 × 10	10.00	.240	5.25
5-1/4 × 11	11.00	.740	5.25
Tolerance	± .03	± .030	± .03

[1] If file is mounted on slides, file will extend 14 inches from operating position for servicing.

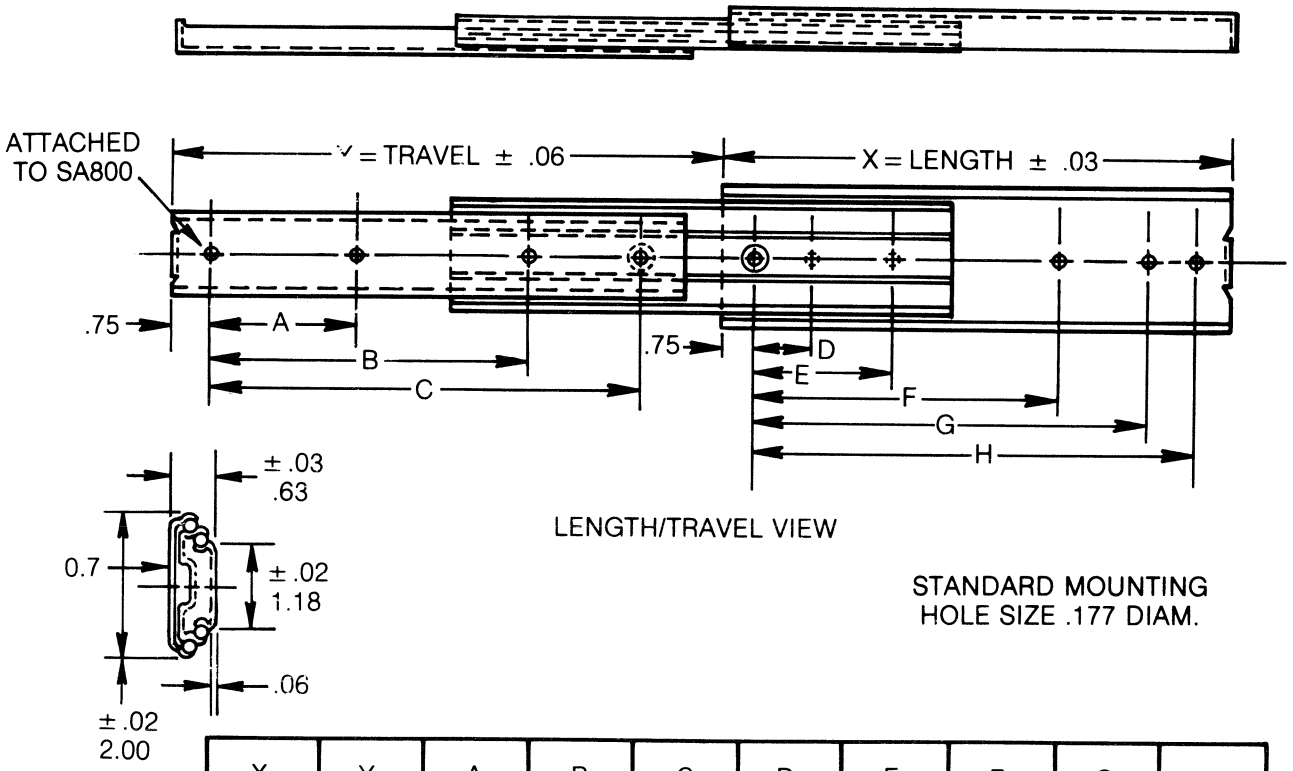
[2] With decorative cover this dimension is .38.

[3] Handle extends .375 beyond faceplate.

[4] All dimensions are in inches.

6.3 Chassis Slide

Available as an optional accessory is a chassis slide kit P/N 50239. This kit contains two slides, one locking and one non-locking, and seven screws. Dimensions of the slide are shown in Figure 19. For use on the standard casting only.



X	Y	A	B	C	D	E	F	G	H
14	15	4.00	8.00	12.00	1.00	3.50	8.50	11.50	12.50

Figure 19. Slide Mounting Dimensions

6.4 Decorative Face Plate

The SA800/801 may be ordered with one of the following decorative face plates:

SIZE	COLOR	PART NO.
4 5/8 × 10 1/2	Tan	50264
4 5/8 × 10 1/2	White	50263
5 1/4 × 10	Tan	50261
5 1/4 × 10	White	50260
5 1/4 × 11	Tan	50258
5 1/4 × 11	White	50257
"R" Series-4 5/8 × 8 11/16	Tan	50675

If another color is required to match the system's color scheme, the face plate may be painted. The following information should be utilized to avoid potential problems in the painting process.

1. The front cover is made from GE's LEXAN. Dimensional stability of LEXAN exists from -60°F + 250°F. If the type paint used requires baking, the temperature should not exceed + 250°F, including any hot spots which can contact the cover.

2. LEXAN is a polycarbonate. Any paint to be used should be investigated to insure that it does not contain chemicals that are solvents to polycarbonates.

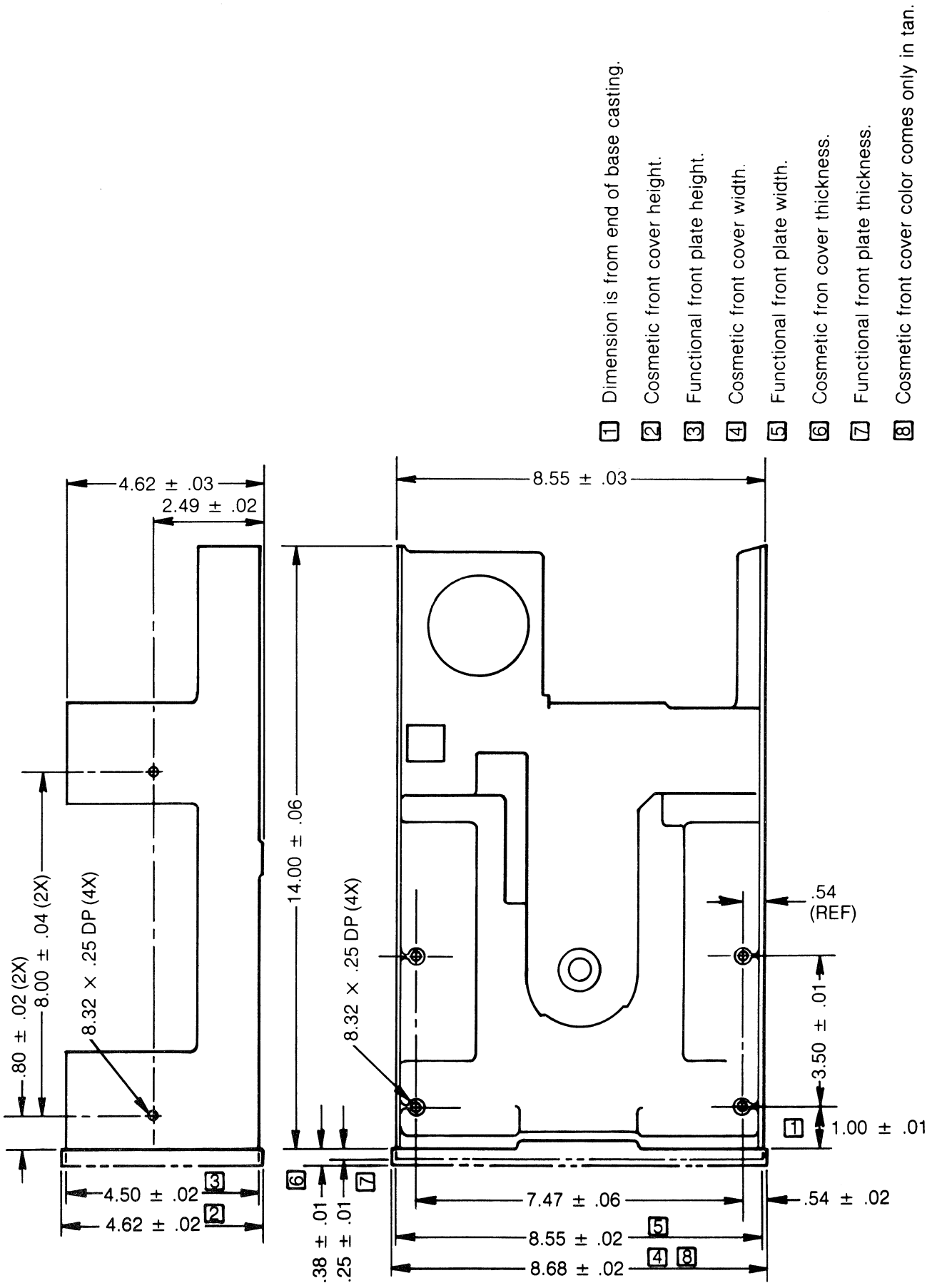


Figure 20. SA800/801R Dimensions

7.0 CUSTOMER INSTALLABLE OPTIONS

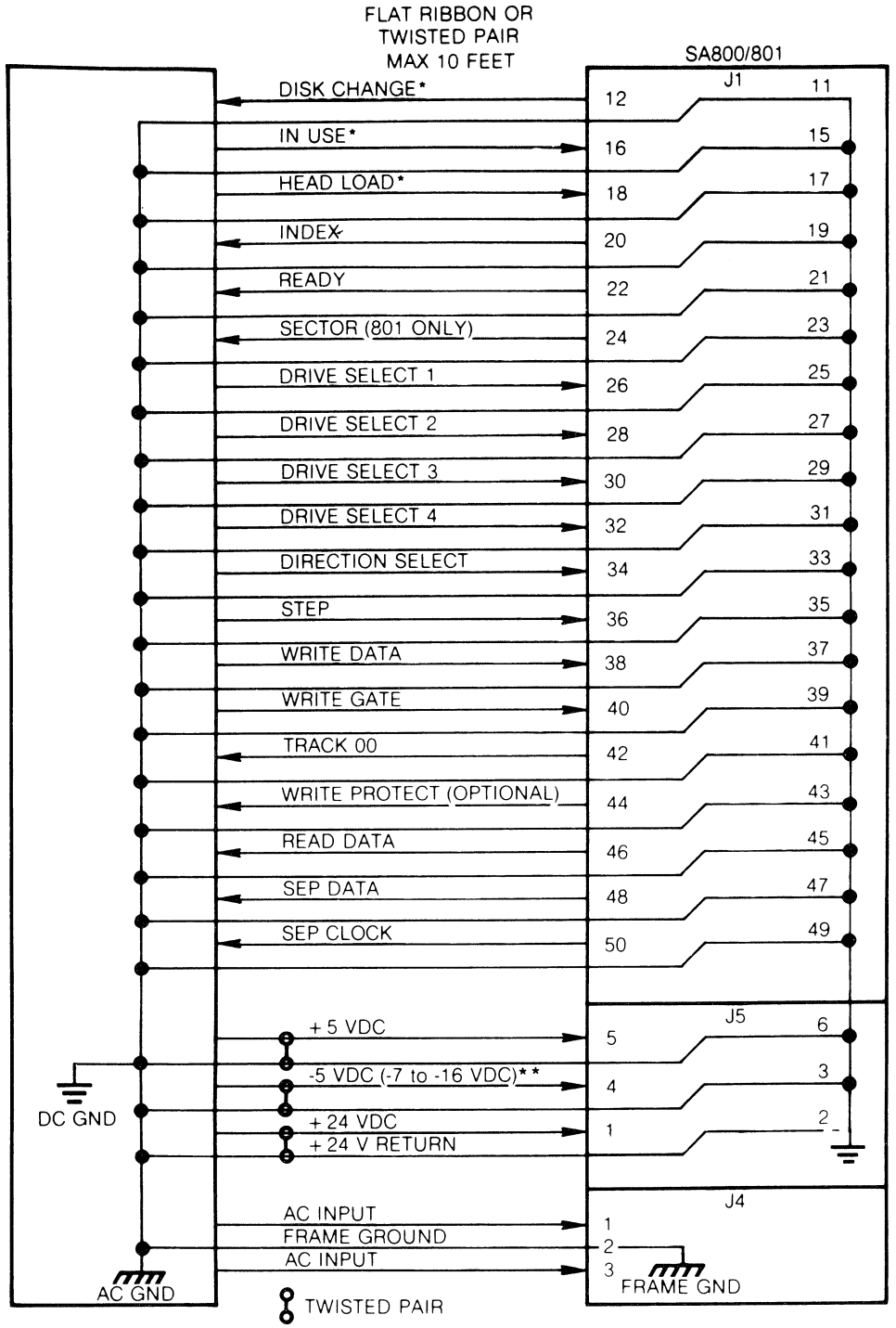
The SA800/801 can be modified by the user to function differently than the standard method as outlined in sections 3 and 4. These modifications can be implemented by adding or deleting traces and by use of the Alternate I/O pins. Some traces are capable of being connected by use of a shorting plug, Shugart P/N 15648 or AMP P/N 530153-2. This section will discuss a few examples of modifications and how to install them. The examples are:

1. Drive Select one to eight drives.
2. Select drive without loading head or enabling stepper.
3. Select drive and enable stepper without loading the head.
4. Load head without selecting drive or enabling stepper.
5. Radial Ready.
6. Radial Index/Sector.
7. Eight, 16, or 32 Sector option.
8. In Use (Activity L.E.D.) optional input.
9. Write Protect options.

Tabulated below are the trace options with the condition of the trace as it is shipped from the factory. Figure 21 shows the location of these traces on the PCB.

CUSTOMER CUT/ADD TRACE OPTIONS

TRACE DESIGNATOR	DESCRIPTION	SHIPPED FROM FACTORY	
		OPEN	SHORT
T3,T4,T5,T6	Terminations for Multiplexed Inputs		Plugged
T1	Terminator for Drive Select		Plugged
T2	Spare Terminator for Radial Head Load	X	
DS1,DS2,DS3,DS4	Drive Select Input Pins	X	DS1 is Plugged
RR	Radial Ready		X
RI	Radial Index and Sector		X
R,I,S	Ready, Index, Sector Alternate Output Pads		X
HL	Stepper Power From Head Load		Plugged
DS	Stepper Power From Drive Select	X	
WP	Inhibit Write When Write Protected		X
NP	Allow Write When Write Protected	X	
8,16,32	8, 16, 32 Sectors (SA801 Only)	8 & 16	32
D	Alternate Input-In Use	X	
2,4,6,8,10,12,14,16,18	Nine Alternate I/O Pins	X	
D1,D2,D4,DDS	Customer Installable Decode Drive Select Option	X	
A,B,X	Radial Head Load		Plugged
C	Alternate Input-Head Load	X	
Z	In Use from Drive Select		Plugged
Y	In Use from HD LD	X	
DC	Alternate Output-Disk Change	X	
NFO	Non Force Out	X	
TS	True FM Data Separation	X	



NOTE: Not shown are 5 of the 9 Alternate I/O connections. The connections for these lines are on pins 2, 4, 6, 8, 10 and 14. Signal return for these lines are on pins 1, 3, 5, 7, 9 and 13 respectively.

*These lines are alternate input/output lines and they are enabled by jumper plugs.

**Not required on LSI PCB's

FIGURE 40. INTERFACE CONNECTIONS

1.9.4 Output Lines

There are seven (7) output lines from the SA800 and eight (8) from the SA801. There also is one (1) optional output line from the SA800/801.

The output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at a logical zero level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is in a logical one or false state the driver is off and the collector current is a maximum of 250 microamperes. The receiver should be a Schmidt trigger type device. Refer to Figure 41.

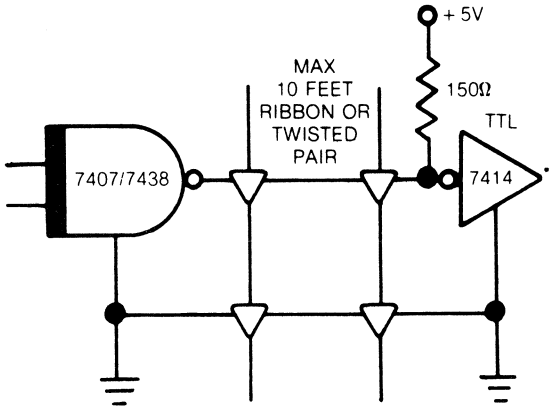


FIGURE 41.

7.1 Drive Select - One to Eight Drives

Customer installed option allows up to eight drives to be multiplexed together. This method of drive selection uses a binary address to select a drive.

To install this feature on a standard drive, the following traces should be added or deleted:

1. Add a 74L85, 4 bit comparator (Motorola P/N MC 14585, National Semiconductor P/N MM 74c85) into position 2B on PCB, (1A on PCB 25136).
2. Connect trace 'DDS'.
3. Insure traces 'DS1' - 'DS4' are plugged.
4. Jumper traces 'D1', 'D2', and 'D4' according to table below for address of each drive.

The four Drive Select lines are to be used for addressing the drives. Pin 26 is used as Drive Select enable and pins 28 (binary 1), 30 (binary 2), and 32 (binary 4), are the address lines. Figure 23 illustrates the circuitry. The table below shows the logical state each line must be at to select each of the drives.

Figure 23 illustrates the circuitry.

ADDRESS	TRACE		
	D1	D2	D4
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

DRIVE	INTERFACE PIN			
	26	28	30	32
0	0	1	1	1
1	0	0	1	1
2	0	1	0	1
3	0	0	0	1
4	0	1	1	0
5	0	0	1	0
6	0	0	1	0
7	0	0	0	0

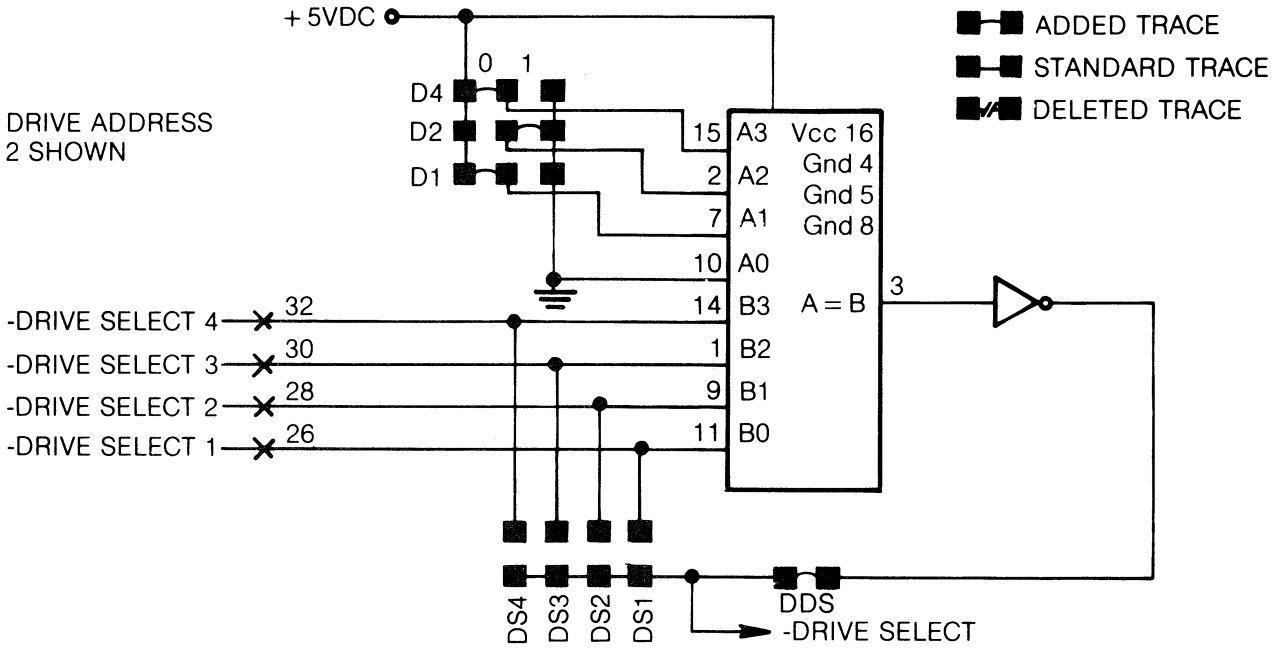


Figure 23. Drive Select Circuitry

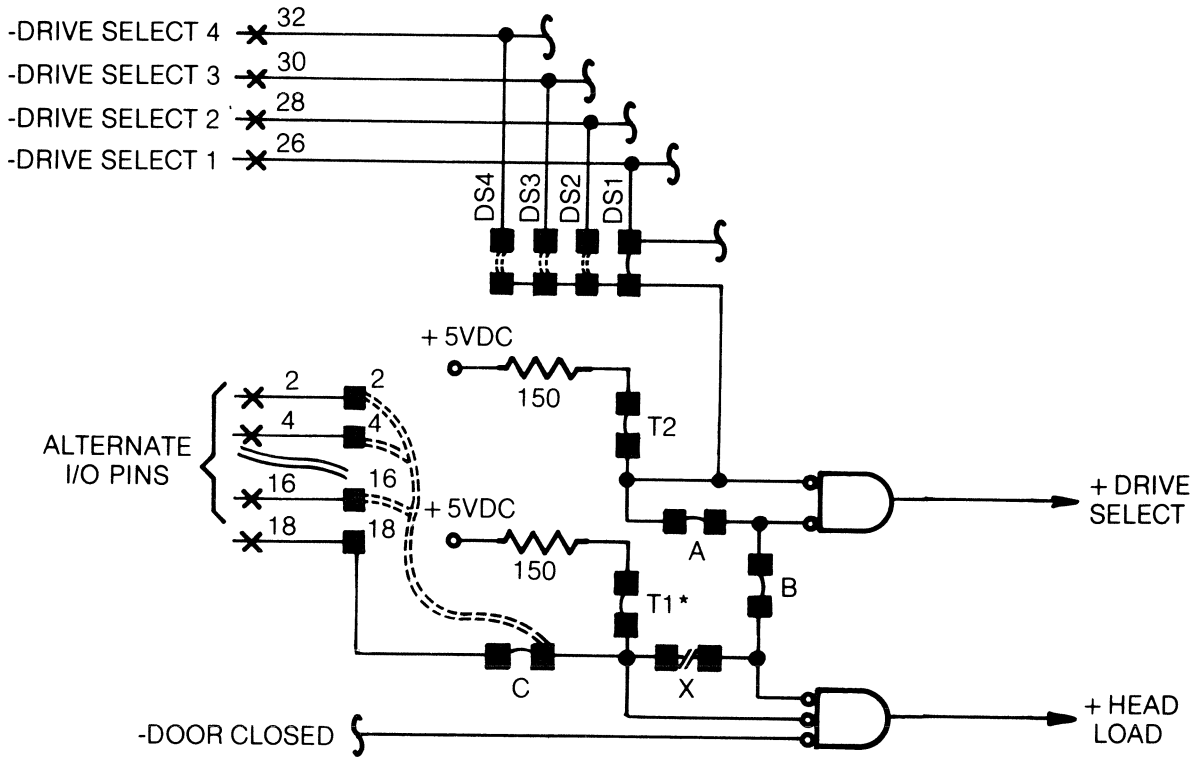
7.2 Select Drive Without Loading Head Or Enabling Stepper Motor

This option would be advantageous to the user who requires a drive to be selected at all times. Normally, when a drive is selected, its head is loaded and the stepper motor is energized. The advantage of this option would be that the output control signals could be monitored (with the exception of Track Zero, which requires the stepper to be energized) while the head was unloaded thereby extending the head and media life. When the system requires the drive to perform a Read, Write, or Seek, the controller would activate the Head Load line (pin 18) which in turn would load the head and energize the stepper motor. After the Head Load line is activated, a 35 ms delay must be introduced before Write Gate and Write Data may be applied or before Read Data is valid.

To install this option on a standard drive, the following traces should be added or deleted:

1. Jumper trace 'T2'.
2. Remove jumper from trace 'X'.
3. Jumper trace 'C'.

Figure 24 iilustrates the circuitry.



*NOTE: If the -Head Load line is multiplexed, terminator 'T1' jumper must be removed from each drive except the last one on the line. Also, the current requirement for the +24 VDC supply should be a multiple of the maximum +24 volt current times the number of drives on the line that have Head Load active.

Figure 24. Select Drive Without Loading Head Circuit

7.3 Select Drive and Enable Stepper Without Loading Head

This option is useful to the user who wishes to select a drive and perform a seek operation without the head being loaded or with door open. An example use of this option is that at power on time, an automatic recalibrate (reverse seek to track zero) operation could be performed with the drive access door open. Normally for a seek to be performed, the door must be closed and the head loaded. Other advantages are those listed in section 7.2 in addition to being able to monitor Track Zero. When a Read or Write operation is to be performed, the head must be loaded (pin 18). After the Head Load line is activated, a 35 ms delay must be introduced before Write Gate and Write Data may be applied or before Read Data is valid.

To install this option on a standard drive, the following traces should be added or deleted:

1. Jumper trace 'T2'.
2. Remove jumper from trace 'B'.
3. Remove jumper from trace 'HL'.
4. Jumper trace 'DS'.
5. Jumper trace 'C'.

Figures 24 and 25 illustrate the circuitry.

7.4 Load Head Without Selecting Drive Or Enabling Stepper

This option is useful in disk to disk copy operations. It allows the user to keep the heads loaded on all drives thereby eliminating the 35 ms head load time. The head is kept loaded on each drive via an Alternate I/O pin. Each drive may have its own Head Load line (Radial or Simplexed) or they may share the same line (Multiplexed). When the drive is selected, an 8 ms delay must be introduced before a Read or Write operation can be performed. This is to allow the R/W head to settle after the stepper motor is energized. With this option installed, a drive can only be selected with both Drive Select and Head Load active.

To install this option on standard drive, the following traces should be added or deleted:

1. Jumper trace 'T2'.
2. Remove jumper from trace 'A'.
3. Remove jumper from trace 'HL'.
4. Jumper trace 'DS'.
*5. Jumper trace 'C'.

*If the -Head Load line is multplexed, terminator 'T1' jumper must be removed from each drive except the last one on the line.

Figures 25 and 26 illustrate the circuitry.

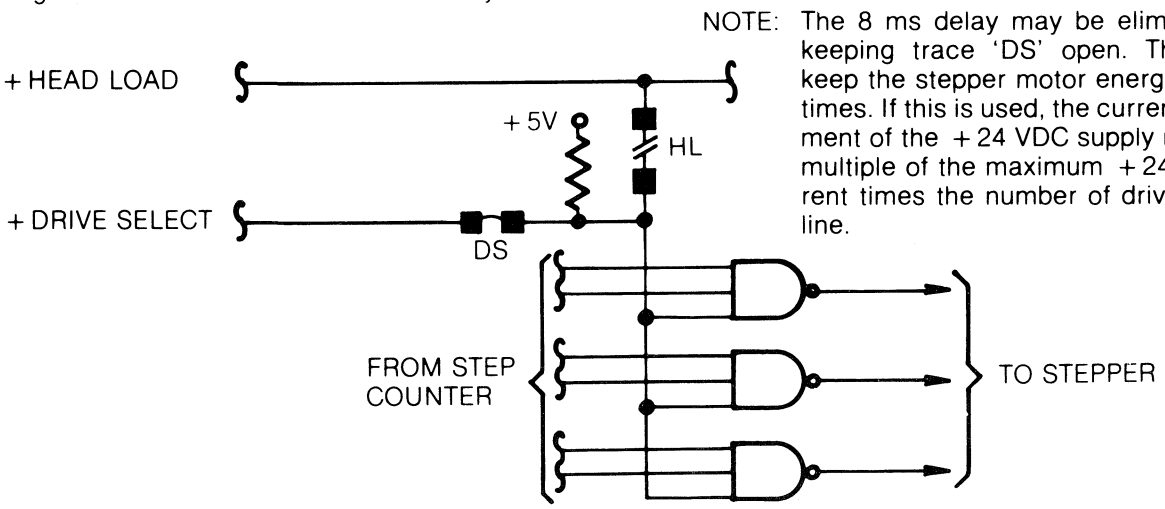


Figure 25. Stepper Motor Enable Circuit

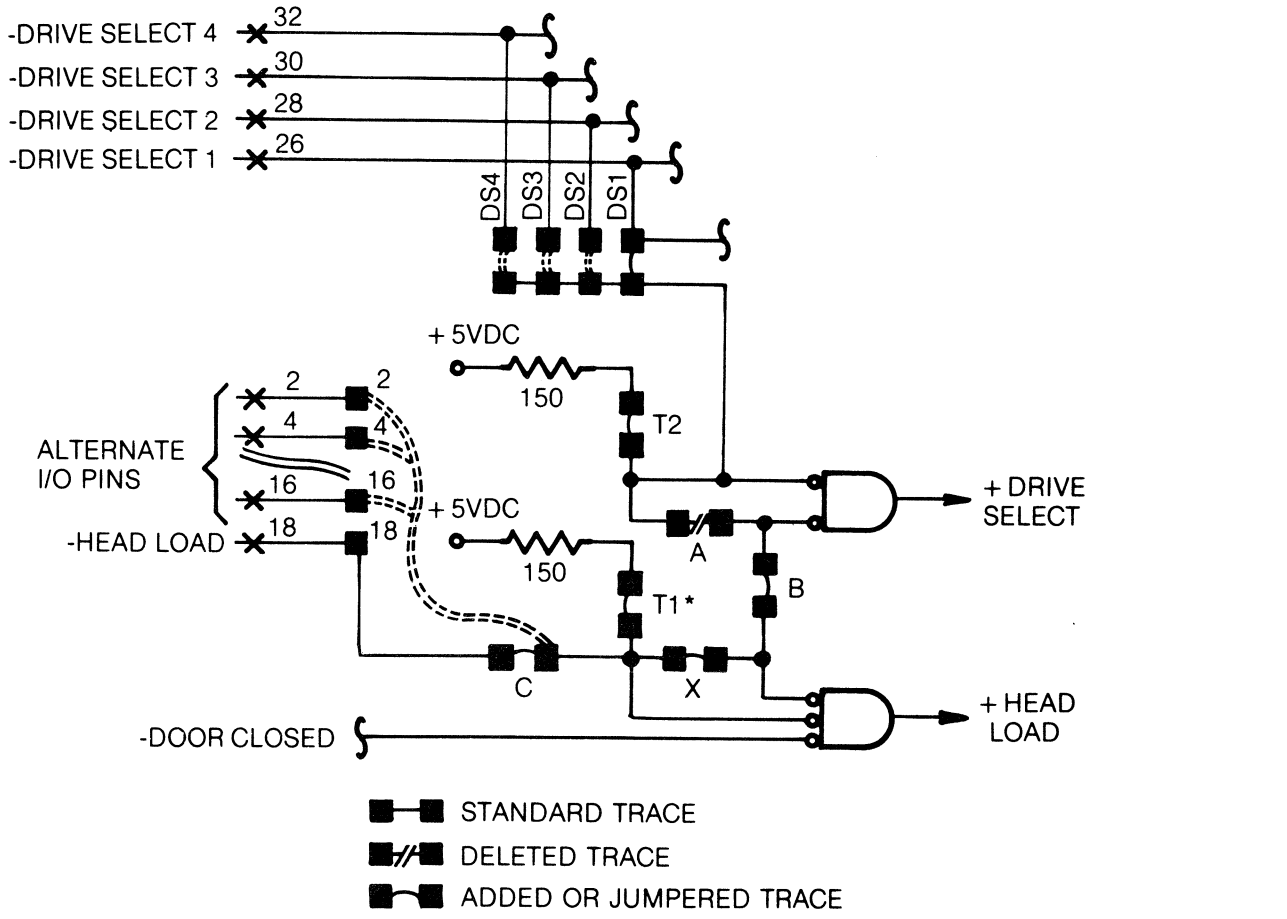


Figure 26. Load Head Without Selecting Drive or Enabling Stepper Circuit

7.5 Radial Ready

This option enables the user to monitor the Ready line of each drive on the interface. This can be useful in detecting when an operator has removed or installed a Diskette in any drive. Normally, the Ready line from a drive is only available to the interface when it is selected.

To install this option on a standard drive, the following traces should be added or deleted:

1. Cut trace 'RR'.
*2. Cut trace 'R'.
*3. Add a wire from pad 'R' to one of the Alternate I/O pins.

*One of the drives on the interface may use pin 22 as its Ready line, therefore, steps 2 and 3 may be eliminated on this drive. All the other drives on the interface must have their own Ready line, therefore steps 2 and 3 must be incorporated.

Figure 27 illustrates the circuitry.

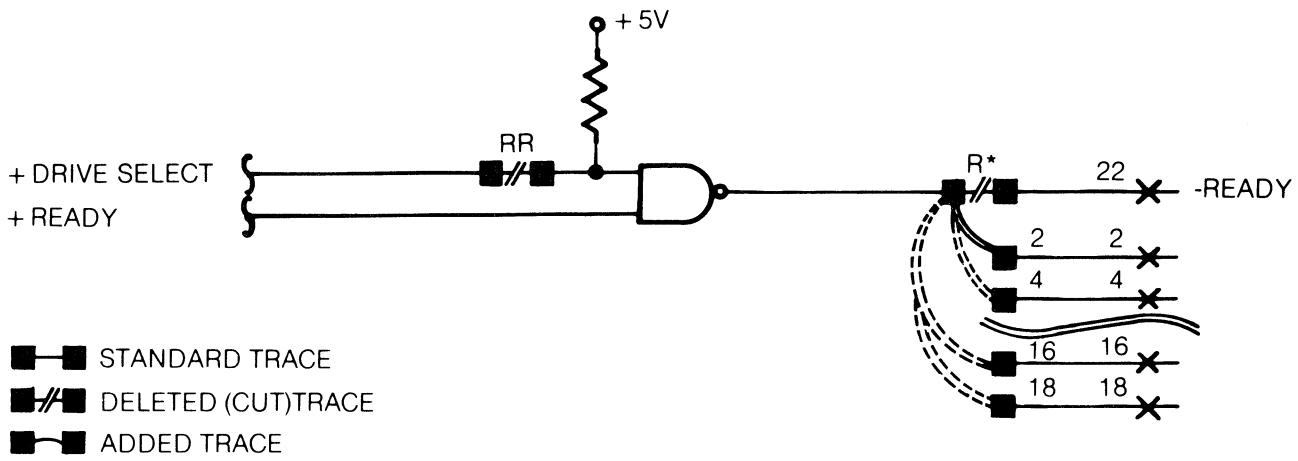


Figure 27. Radial Ready Circuit

7.6 Radial Index/Sector

This option enables the user to monitor the Index and Sector lines at all times so that the drive may be selected just prior to the sector that is to be processed. This option can be used to reduce average latency.

To install this option on a standard drive the following traces should be added or deleted:

1. Cut trace 'RI'.
*2. Cut trace 'I'.
*3. Cut trace 'S'.
*4. Add a wire from trace 'I' to one of the Alternate I/O pins.
*5. Add a wire from trace 'S' to one of the Alternate I/O pins.

*One of the drives on the interface may use pin 20 (-Index) and pin 24 (-Sector) as its Index and Sector lines, therefore, steps 2-5 may be eliminated for this drive. All other drives on the interface must have their own Index and Sector lines, therefore, steps 2-5 must be incorporated.

Figure 28 illustrates the circuitry.

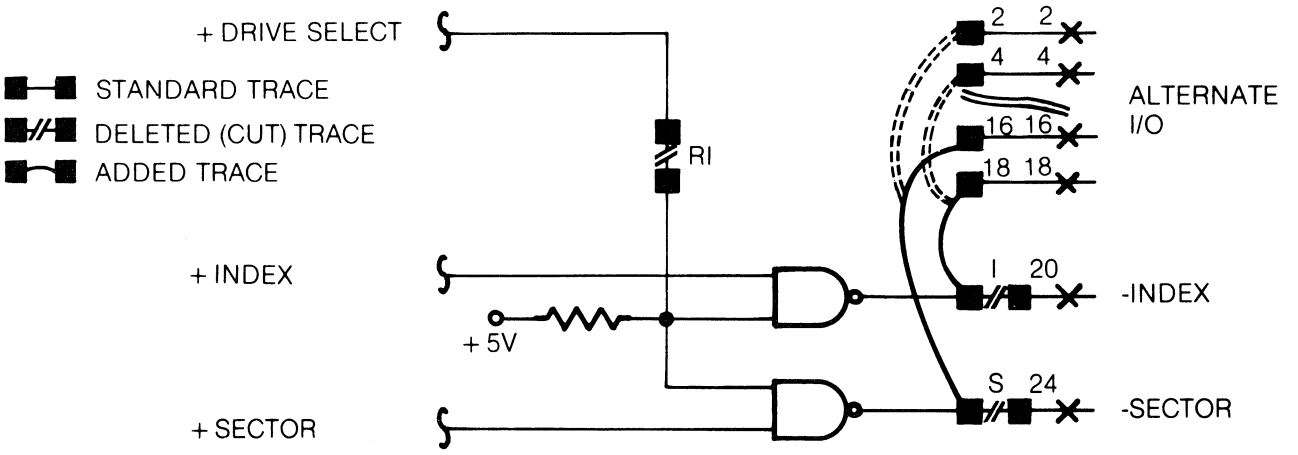


Figure 28. Radial Index/Sector Circuit

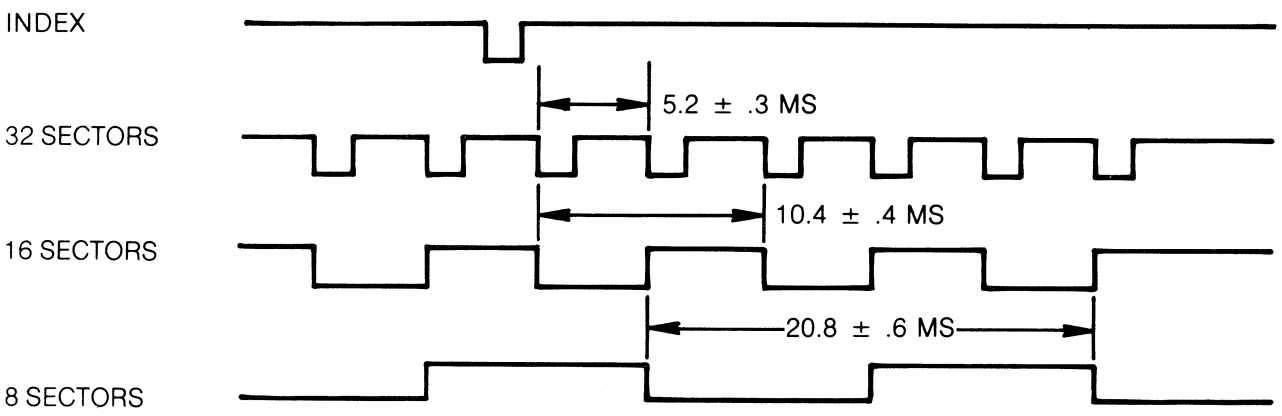
7.7 Eight, 16, Or 32 Sectors

The SA801, as shipped from the factory, is set up to provide 32 Sector pulses per revolution of the Diskette onto the interface. This option is provided for the user who wishes to have eight or 16 Sectors per revolution. The logic divides the Sector pulses by two or four. Reference Figure 29 for the timing relationships.

To install this option on a standard drive (SA801), the following traces should be added or deleted:

1. Cut trace '32'.
2. Connect trace '16' for 16 Sectors or connect trace '8' for eight Sectors.

Figure 30 illustrates the circuitry.



* INDICATES BEGINNING OF SECTOR 1 IN RELATIONSHIP TO INDEX

Figure 29. Sector Timing Relationships

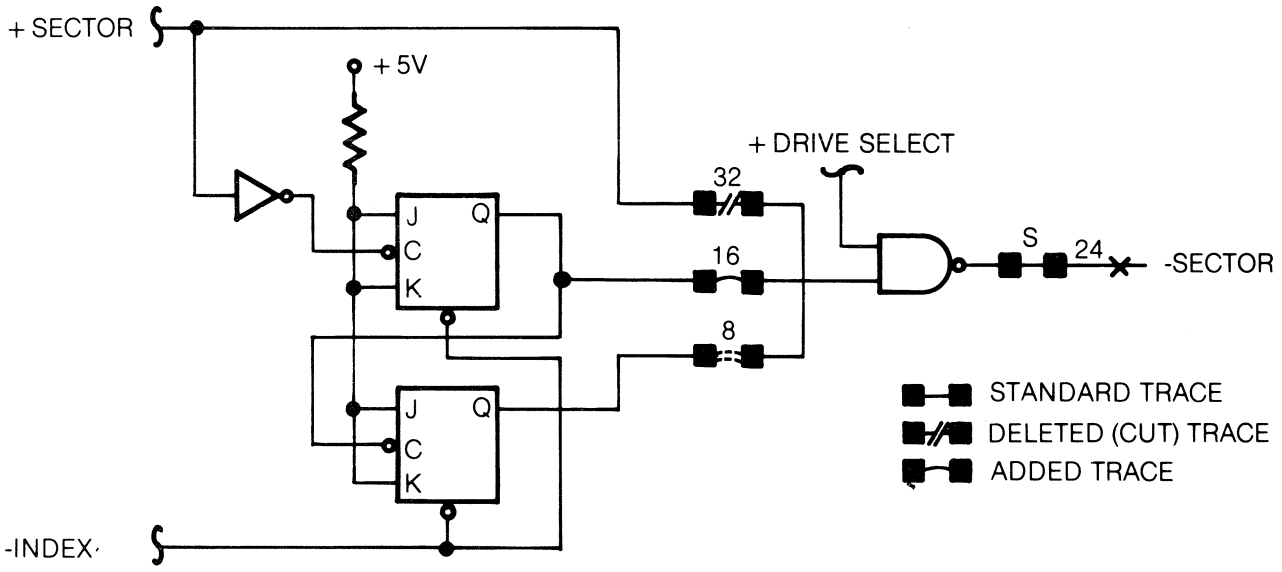


Figure 30. Sector Divide Circuit

7.8 In Use Alternate Input (Activity LED)

This alternate input, when activated to a logical zero level, will turn on the Activity LED mounted in the push bar on the front panel of the drive. It can be used as an indicator to the operator. Examples of some indications are:

1. Write protected Diskette is installed.
2. Drive in which the diskette is to be changed.
3. The operating system drive.
4. Drive with a special configuration.

To install this option on standard drive, jumper trace 'D' and active the interface line pin 16.

This signal is an "OR" function with Drive Select or Head Load. Figure 31 illustrates the circuitry.

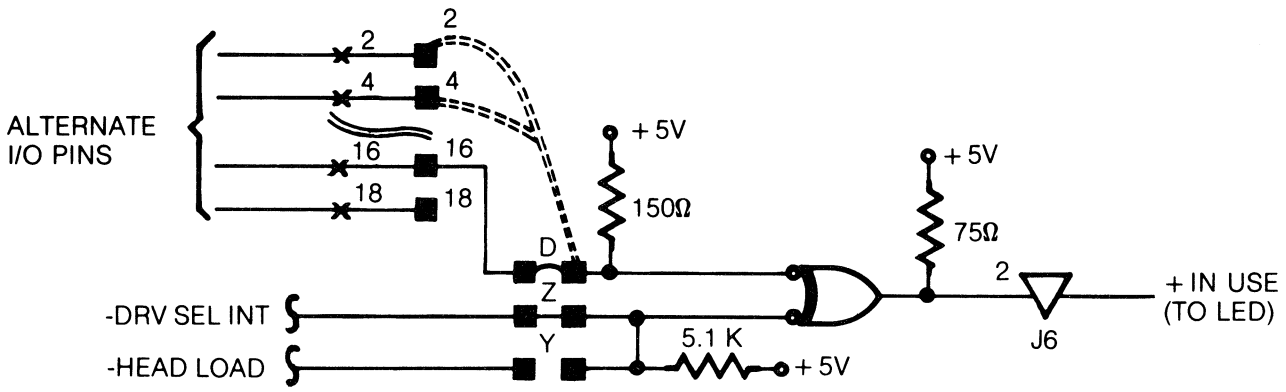


Figure 31. In Use/Activity LED Circuit

7.9 Write Protect Optional Use

As shipped from the factory, the optional Write Protect feature will internally inhibit writing when a Write Protected Diskette is installed. With this option installed, a Write Protected Diskette will not inhibit writing, but it will be reported to the interface. This option may be useful in identifying special use Diskettes.

To install this option on a drive with the Write Protect feature, the following traces should be added or deleted:

1. Cut trace 'WP'.
2. Connect trace 'NP'.

Figure 32 illustrates the circuitry.

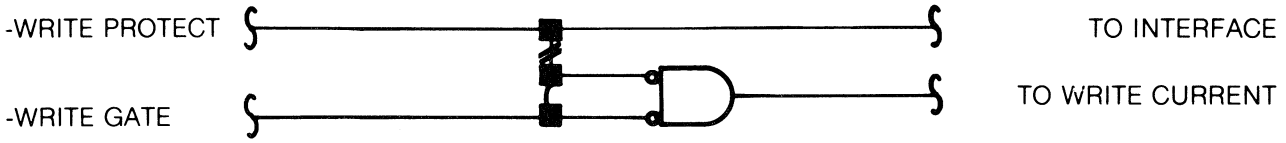


Figure 32. Write Protect Circuit

7.10 Disk Change (Alternate Output)

This customer installable option is enabled by jumpering trace 'DC'. It will provide a true signal (logical zero) onto the interface (pin 12) when Drive Select is activated if while deselected the drive has gone from a Ready to a Not Ready (Door Open) condition. This line is reset on the true to false transition of Drive Select if the drive has gone Ready. Timing of this line is illustrated in Figure 33. The circuitry is illustrated in Figure 34.

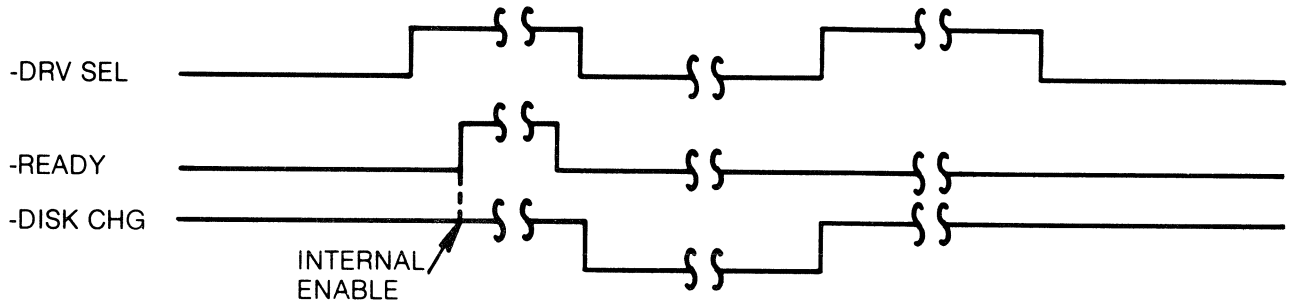


Figure 33. Disk Change Timing

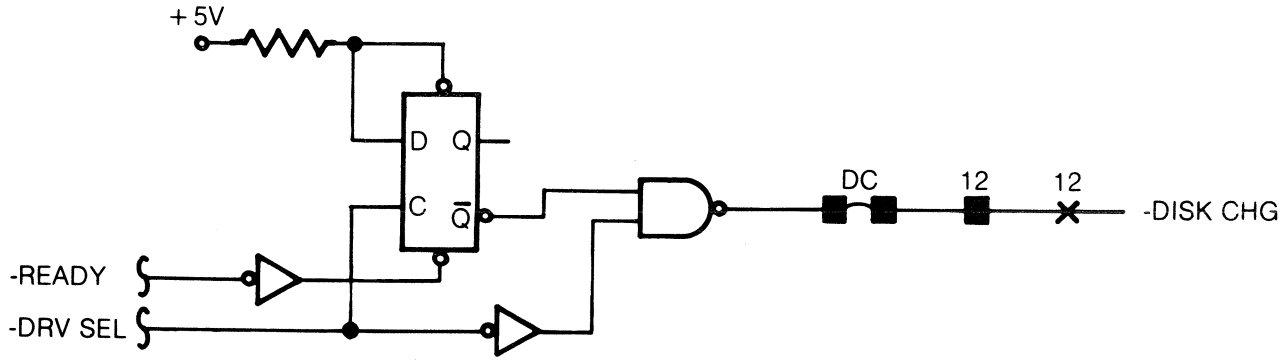


Figure 34. Disk Change Circuit

8.0 OPERATION PROCEDURES

The SA800/801 was designed for ease of operator use to facilitate a wide range of operator oriented applications. The following section is a guide for the handling and error recovery procedures on the diskette and diskette drive.

8.1 Diskette Loading and Handling

The diskette is a flexible disk enclosed in a plastic jacket. The interior of the jacket is lined with a wiping material to clean to disk of foreign material. Figure 35 shows the proper method of loading a diskette in the SA800/801 Diskette Storage Drive. To load the diskette, depress latch, insert the diskette with the label facing out. (See Figure 35). Move the latch handle to the left to lock diskette on drive spindle. The diskette can be loaded or unloaded with all power on and drive spindle rotating.

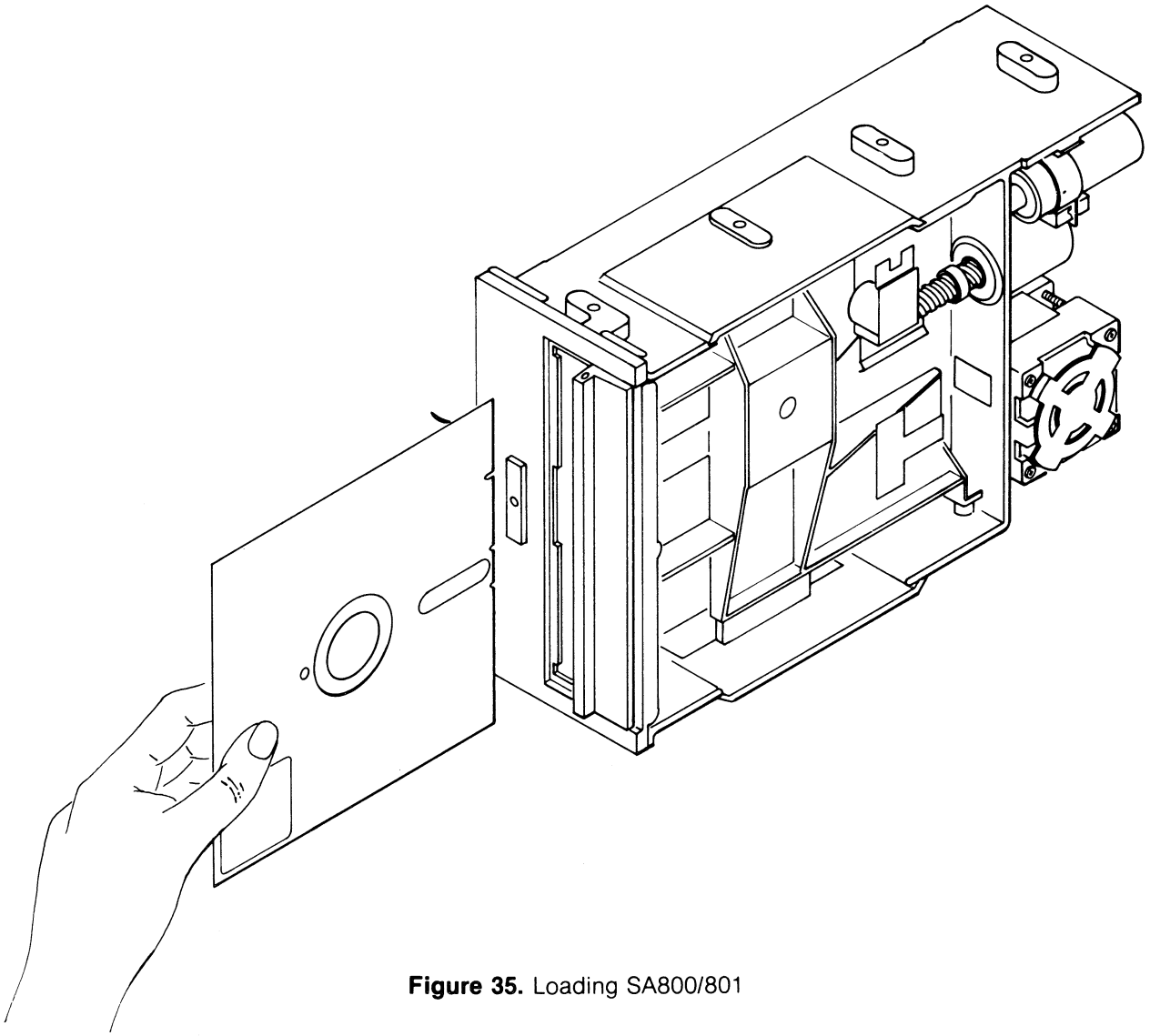


Figure 35. Loading SA800/801

When removed from the drive, the diskette is stored in an envelope. To protect the diskette, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

1. Return the diskette to its storage envelope.
2. Keep cartridges away from magnetic fields and from ferromagnetic materials which might become magnetized. Strong magnetic fields can distort recorded data on the disk.
3. Replace storage envelopes when they become worn, cracked or distorted. Envelopes are designed to protect the disk.
4. Do not write on the plastic jacket with a lead pencil or ball-point pen. Use a felt tip pen.
5. Heat and contamination from a carelessly dropped ash can damage the disk.
6. Do not expose diskette to heat or sunlight.
7. Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.

8.2 Write Protecting a Diskette

Shugart Media has the capability of being write protected. The write protect feature is selected by the notch in the media. When the notch is open it is protected; when covered, writing is allowed. The notch is closed by placing a tab over the front of the notch, and the tab folded over covering the rear of the notch. The Diskette can then be write protected by removing the tab. Refer to Figures 36 and 37.

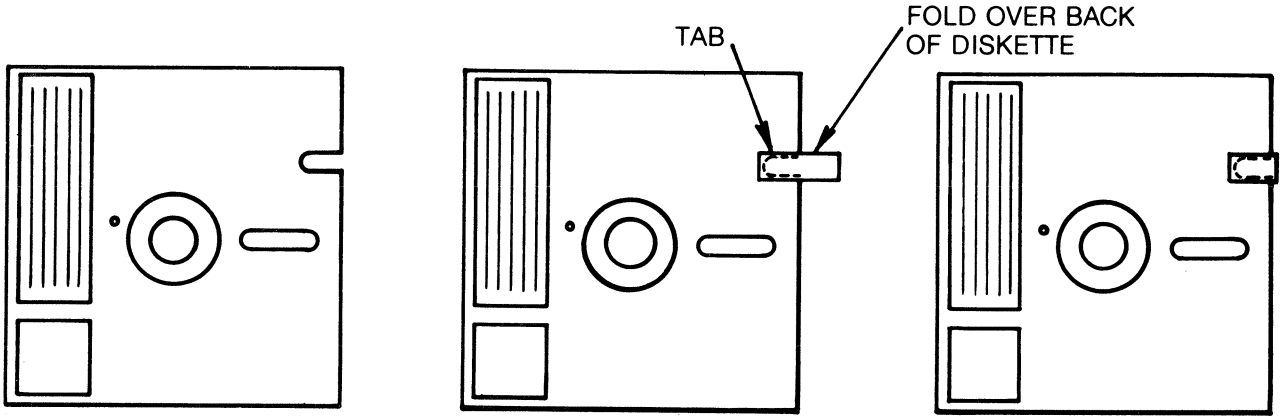


Figure 36. Diskette Write Protected

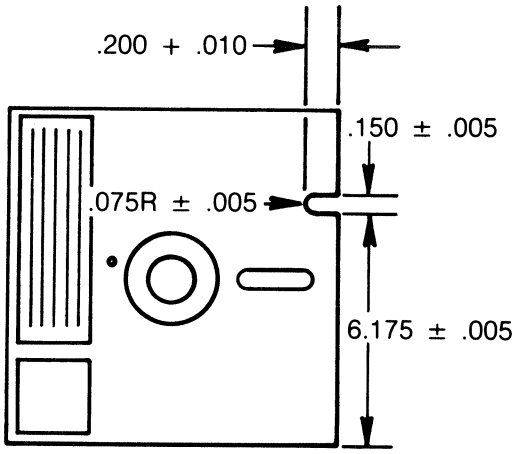


Figure 37. Write Inhibit Notch Specifications

9.0 ERROR DETECTION AND CORRECTION

9.1 Write Error

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check." To correct the error, another write and write check operation must be done. If the write operation is not successful after ten attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error still persists, the disk should be considered defective and discarded.

9.2 Read Error

Most errors that occur will be "soft" errors; that is, by performing an error recovery procedure the data will be recovered.

Soft errors are usually caused by:

1. Airborne contaminants that pass between the read/write head and the disk. These comtaminants will generally be removed by the cartridge self-cleaning wiper.
2. Random electrical noise which usually lasts for a few μsec.
3. Small defects in the written data and/or track not detected during the write operation which may cause a soft error during a read.

The following procedures are recommended to recover from the above mentioned soft errors:

1. Reread the track ten times or until such time as the data is recovered.
2. If data is not recovered after using step 1, access the head to the adjacent track in the same direction previously moved, then return to the desired track.
3. Repeat step 1.
4. If data is not recovered, the error is not recoverable.

APPENDIX G: SHUGART SA1000 8" FIXED DISK DRIVE MANUAL

SA1000
Fixed Disk Drive

OEM Manual

Shugart

SA1000
Fixed Disk Drive

OEM Manual

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LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The Shugart Model 1000 series disk drive is a random access storage device with one or two non-removable 8" disks as storage media. Each disk surface employs one movable head to service 256 data tracks. The two models of the SA1000 series are the 1002 and the 1004 with single and double platters respectively. The SA1002 provides 5 megabytes accessed by 2 movable heads and the SA1004 provides 10 megabytes accessed by 4 movable heads.

Low cost and unit reliability are achieved through the use of a unique band actuator design. The inherent simplicity of mechanical construction and electronic controls allows maintenance free operation throughout the life of the drive.

Mechanical and contamination protection for the head, actuator and disks are provided by an impact resistant plastic and alumimun enclosure. A self contained recirculating system supplies clean air through a .3 micron filter. Another absolute filter allows pressure equalization with ambient air without chance of contamination.

The optional SA1200 Data Separator PCB or equivalent circuitry is necessary to provide MFM encoding/decoding, write precompensation, a crystal write oscillator and address mark writing and detection. These functions are also provided by the optional SA1400 controller.

The SA1000 fixed disk drive's interface is similar to the Shugart 8" family of floppy disk drives. The SA1000 is designed to fit into the same physical space as the 8" floppies.

Key Features:

- Storage Capacity of 5.33 or 10.67megabytes.
- Winchester design reliability.
- Same physical size and identical mounting configuration as the SA800/850 floppies.
- Uses the same D.C. voltages as the SA800/850 floppies.

- Proprietary Fast Flex III band actuator.
- 4.34 Mbits/second transfer rate.
- Simple floppy type interface.

1.2 Specification Summary

1.2.1 Physical Specifications

Environmental Limits

Ambient Temperature =	50° to 115°F (10° to 46°C)
Relative Humidity =	8% to 80%
Maximum Wet Bulb =	78° non-condensing

AC Power Requirements

50/60 Hz ± 0.5Hz

100/115 VAC Installations	= 90-127V at 0.5A typical
200/230 VAC Installations	= 180-253V at 0.25A typical

DC Voltage Requirements

+24VDC ± 10% 2.8A typical during stepping (0.2A typical steady state, non stepping)

+5VDC ± 5% 2.0A typical during stepping (3.6A typical non-stepping)

-5VDC ± 5% (-7 to -16VDC optional) .2A typical

Mechanical Dimensions

	Rack Mount	Standard Mount
Height =	4.62 in. (117.3mm)	4.62 in. (117.3mm)
Width =	8.55 in. (217.2mm)	9.50 in. (241.3mm)
Depth =	14.25 in. (362.0mm)	14.25 in. (362.0mm)
Weight =	17 lbs. (7.7Kg)	17 lbs. (7.7Kg)

Heat Dissipation = 511 BTU/Hr. typical (150 Watts)

1.2.2 Reliability Specifications

MTBF: 8,000 POH typical usage
PM: None Required
MTTR: 30 minutes
Component Life: 5 years

Error Rates:

Soft Read Errors:	1 per 10^{10} bits read
Hard Read Errors:	1 per 10^{12} bits read
Seek Errors:	1 per 10^{6} seeks

1.2.3 Performance Specifications

Capacity	SA1002	SA1004
Unformatted		
Per Drive	5.33 Mbytes	10.67 Mbytes
Per Surface	2.67 Mbytes	2.67 Mbytes
Per Track	10.4 Kbytes	10.4 Kbytes
Formatted		
Per Drive	4.2 Mbytes	8.4 Mbytes
Per Surface	2.1 Mbytes	2.1 Mbytes
Per Track	8.2 Kbytes	8.2 Kbytes
Per Sector	256 bytes	256 bytes
Sectors/Track	32	32
Transfer Rate	4.34 Mbits/sec	4.34 Mbits/sec
Access Time		
Track to Track	19 msec	19 msec
Average	70 msec	70 msec
Maximum	150 msec	150 msec
Average Latency	9.6 msec	9.6 msec

1.2.4 Functional Specifications

Rotational Speed	3125 rpm	3125 rpm
Recording Density	6270 bpi	6270 bpi
Flux Density	6270 fci	6270 fci
Track Density	172 tpi	172 tpi
Cylinders	256	256
Tracks	512	1024
R/W Heads	2	4
Disks	1	2

2.0 FUNCTIONAL CHARACTERISTICS

2.1 GENERAL OPERATION

The SA1000 fixed disk drive consists of read/write and control electronics, read/write heads, track positioning mechanism, media, and air filtration system. These components perform the following functions:

1. Interpret and generate control signals.
2. Position the heads over the selected track.
3. Read and Write data.
4. Provide a contamination free environment.

2.2 READ/WRITE AND CONTROL ELECTRONICS

The standard electronics are packaged on a single printed circuit board containing the following circuits:*

1. Index Detector Circuit
2. Head Position Actuator Drivers
3. Read/Write Amplifiers
4. Drive (Ready) up to Speed Circuit
5. Drive Select Circuit
6. Write Fault Detection Circuit
7. Read/Write Head Select Circuit
8. Step Buffers with Ramped Stepper Circuit
9. Track 000 indicator

*Early units may have two printed circuit boards.

2.3 Drive Mechanism

The AC drive motor rotates the spindle at 3125 RPM through a belt-drive system. Either 50 or 60 Hz power is accommodated by changing the drive pulley and belt.

2.4 Air Filtration System (Figure 1)

The disk(s) and read/write heads are fully enclosed in a module using an integral recirculating air system with an absolute filter which maintains a clean environment. A separate absolute breather filter permits pressure equalization with the ambient air without contamination.

2.5 Positioning Mechanism (Figure 2)

The read/write heads are mounted on a ball bearing supported carriage which is positioned by the Fasflex III™ actuator. A stepper motor is used to precisely position the carriage assembly utilizing a unique metal band/capstan concept.

2.6 Read/Write Heads and Disk(s)

The recording media consists of a lubricated thin magnetic oxide coating on a 200mm diameter aluminum substrate. This coating formulation, together with the low load force/low mass Winchester type flying heads, permit reliable contact start/stop operation.

Data on each disk surface is read by one read/write head, each of which accesses 256 tracks. The drive is available in two basic configurations: one disk with two read/write heads, or two disks with four read/write heads.

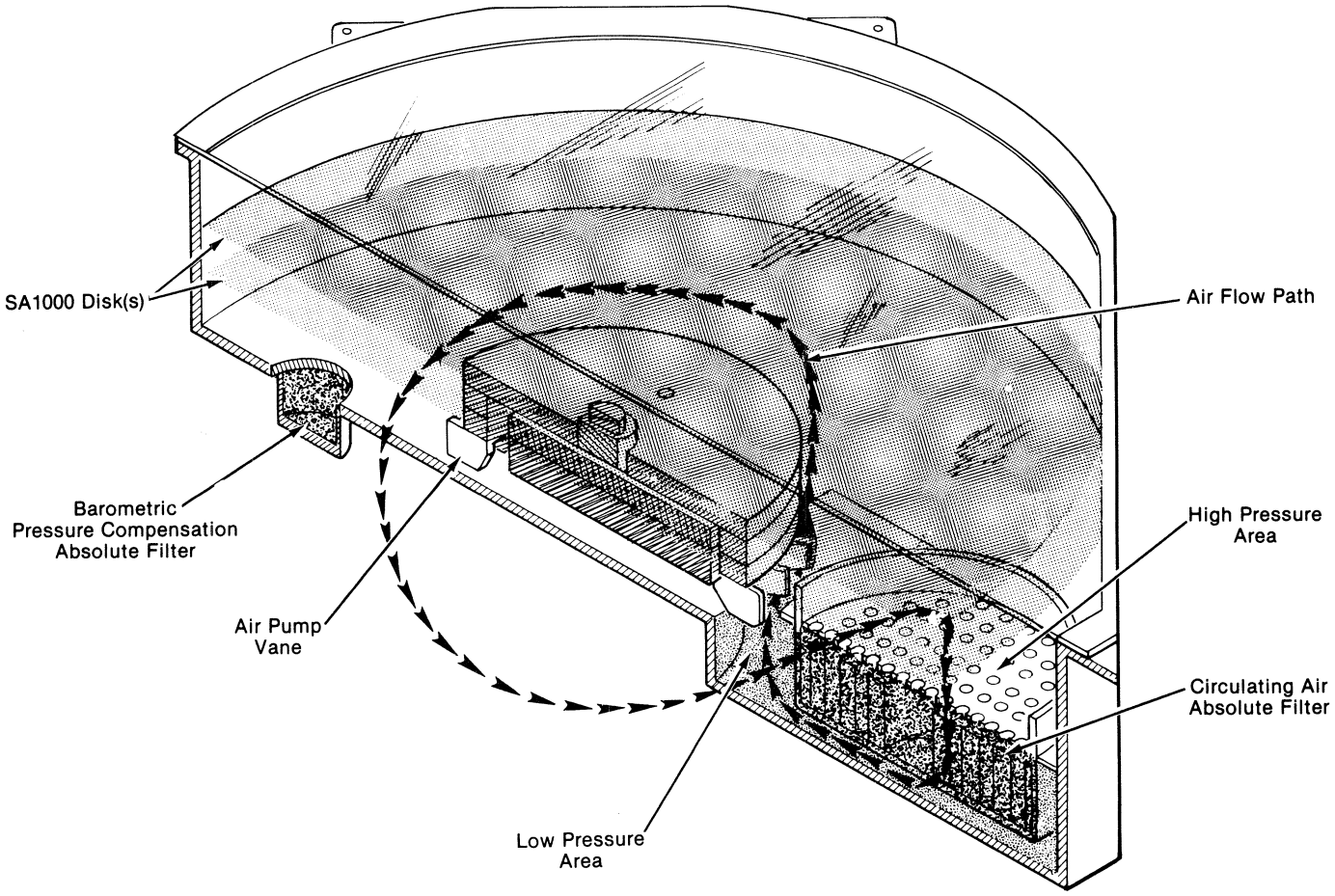


Figure 1 Air Filtration System

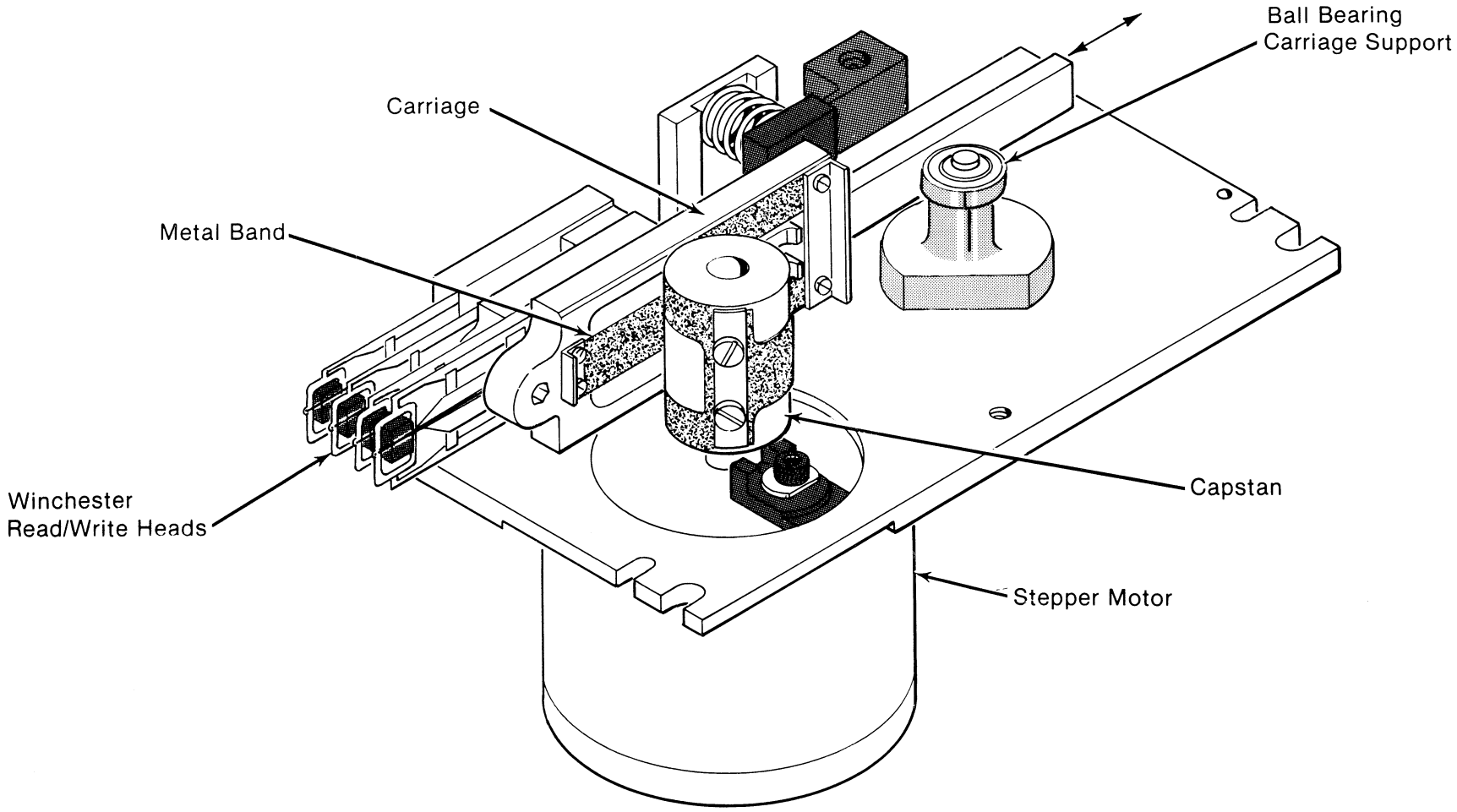


Figure 2 Posiitoning Mechanism

3.0 FUNCTIONAL OPERATIONS

3.1 POWER SEQUENCING

Since the SA1000 has a speed sense circuit that prevents stepping until the disk is rotating at the proper speed, no power on sequence is required. A READY signal will be presented to the controller interface once the disk is up to 95% of its normal rotational speed. At READY time, after an initial power up, the drive will recalibrate itself to TK000. After a 18 msec head settle time, SEEK COMPLETE will go true. Normal seek and read/write functions can now begin. Refer to Figure 3.

3.2 DRIVE SELECTION

Drive selection occurs when one of the Drive Select lines is activated. Only the disk appropriately jumpered will respond to the input signals, and that drive's output signals are then gated to the controller.

3.3 TRACK ACCESSING

Read/Write Head positioning is accomplished by:

a. Deactivating Write Gate.

b. Activating the appropriate Drive Select Line.

c. Being in the READY condition with SEEK COMPLETE true.

d. Selecting the appropriate Direction.

e. Pulsing the Step Line.

Stepping can occur at either the Normal or Buffered rate. During Normal Stepping, the heads are repositioned at the rate of incoming step pulses. In the case of Buffered Stepping, incoming step pulses are received at a high rate and are buffered into counters. When all of the steps have been received, they are issued at a ramped stepping rate, to the stepper drivers.

Each pulse will cause the heads to move either 1 track in or 1 track out, depending on the level of the Direction In line. A true on the Direction In Line will cause an inward seek; a false on the Direction In Line will result in an outward seek toward TK000.

3.4 HEAD SELECTION

Any of the 4 possible heads can be selected by placing that head's binary address on the two Head Select lines.

3.5 READ OPERATION

Reading data from the disk is accomplished by:

a. Deactivating the Write Gate Line.

b. Activating the appropriate Drive Select Line.

c. Assuring that the drive is Ready.

d. Selecting the appropriate head.

3.6 WRITE OPERATION

Writing data onto the disk is accomplished by:

a. Activating the appropriate Drive Select Line.

b. Assuring that the Drive is Ready.

c. Clearing any write fault conditions if they exist, by reselecting the drive.

d. Selecting the proper head.

e. Activating Write Gate and placing data on the Write Data line.

4.0 ELECTRICAL INTERFACE

The interface of the SA1000 can be divided into three categories:

1. Signal

2. DC Power

3. AC Power

The following sections provide the electrical definition for each line.

4.1 SIGNAL INTERFACE

The signal interface consists of three categories:

1. Control Input lines

2. Control Output lines

3. Data Transfer lines

All control lines are digital in nature and either provide signals to the drive (input) or provide signals to the host (output) via the interface connector J1/P1. The data transfer signals are differential in nature, they provide data and clocking, either to or from the drive, via J2/P2.

NOTE: Refer to Figure 3.*Those signal lines marked SPARE are uncommitted. They may be used as alternate lines to carry SA1000 signals if the user prefers to do his own modification.* **Those signal lines marked NA are uncommitted for the SA1000, but are assigned for the SA800/850.** Therefore, these signals should not be used as alternate signals if a controller having an SA800/850 interface is used.

4.1.1 CONTROL INPUT LINES

The control input signals are of two types: those intended to be mutliplexed in a multiple drive system and those intended to control the multiplexing. The control input signals to be mutliplexed are STEP, DIRECTION IN, HEAD SELECT 2^0 and 2^1, WRITE GATE and REDUCED WRITE CURRENT. The signal which is intended to do the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, DRIVE SELECT 4.

The input lines have the following electrical specifications. Refer to Figure 4 for the recommended circuit.

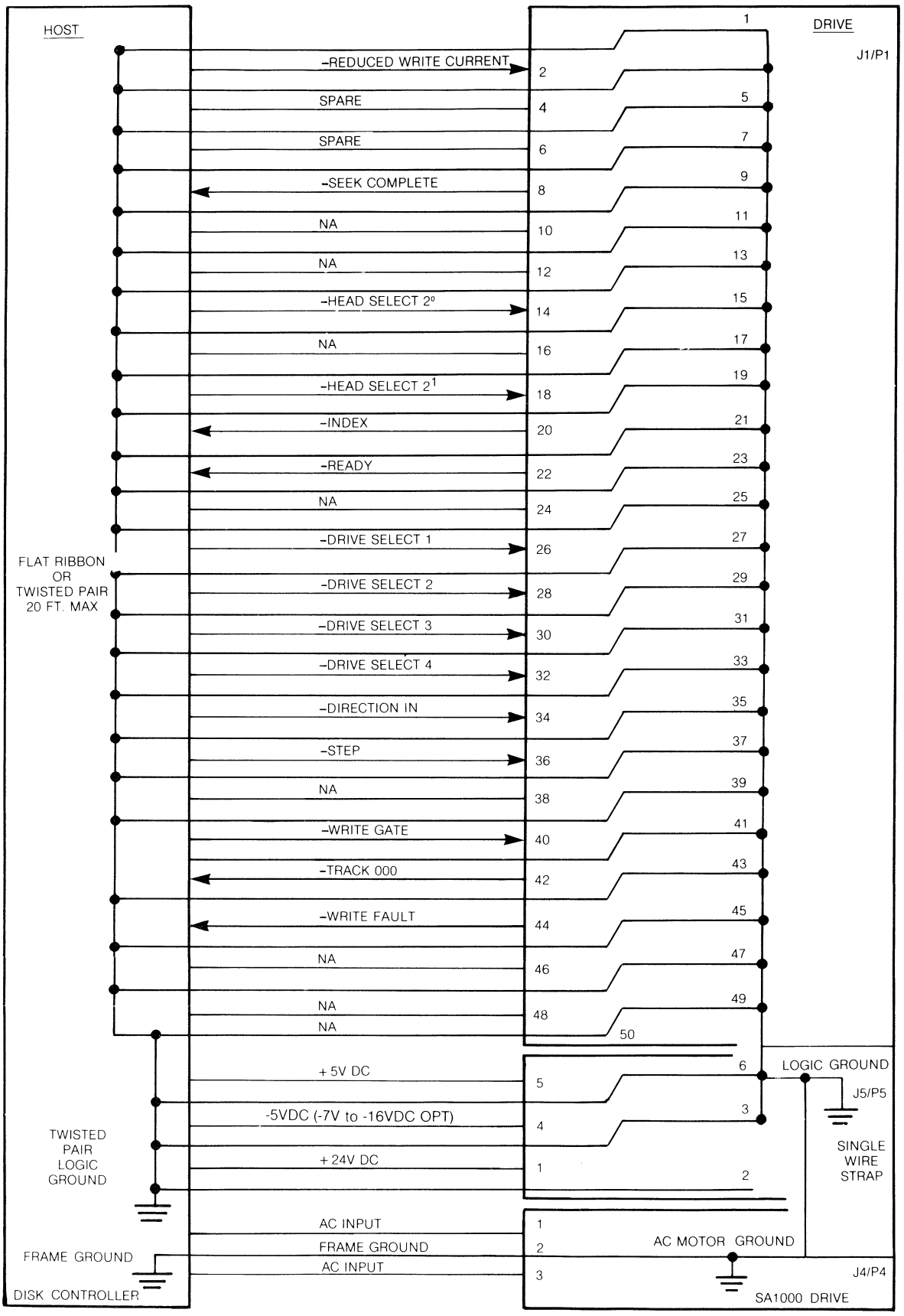


Figure 3 J1 Interface and Power Connection

True = 0.0VDC to 0.4VDC @ Iin = 40 ma(max)
False = 2.5VDC to 5.25 VDC @ Iin = 0 ma (open)

Only 1 drive in the system should be terminated, if floppy disks are daisy chained together with SA1000 drives. A SA1000 should be physically located at the end of the cable and terminated at IC location 8C.

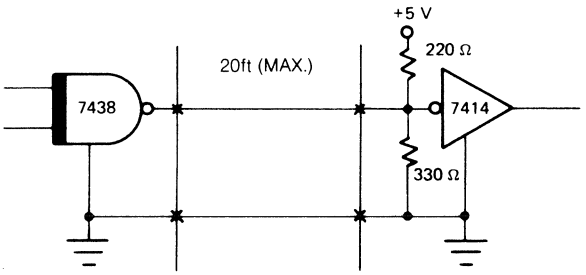


Figure 4 Control Input Driver/Receiver Combination

4.1.1.1 DRIVE SELECT 1-4

DRIVE SELECT, when logically true, connects the drive to the control lines. Only one DRIVE SELECT line may be active at a time.

Jumper options DS1, DS2, DS3, and DS4 are used to select which drive select line will activate the interface for that unique drive.

4.1.1.2 DIRECTION IN

This signal defines the direction of motion of the read/write heads when the STEP line is pulsed. An open circuit or logical false, defines the direction as "out" and if a pulse is applied to the STEP line, the read/write head will move away from the center of the disk. If the input is shorted to ground, or logical true, the direction of motion is defined as "in" and if a pulse is applied to the STEP line, the read/write heads will move towards the center of the disk.

A 220/330Ω resistor pack, located at IC location 8C, provides input line termination.

4.1.1.3 STEP

This line causes the read/write heads to move in the direction as defined by the DIRECTION IN line. The motion is initiated at each logical true to false transition. Any change in the DIRECTION IN line must be made at least 100 ns before the trailing edge of the step pulse. Stepping can be performed in either the Normal or Buffered mode:

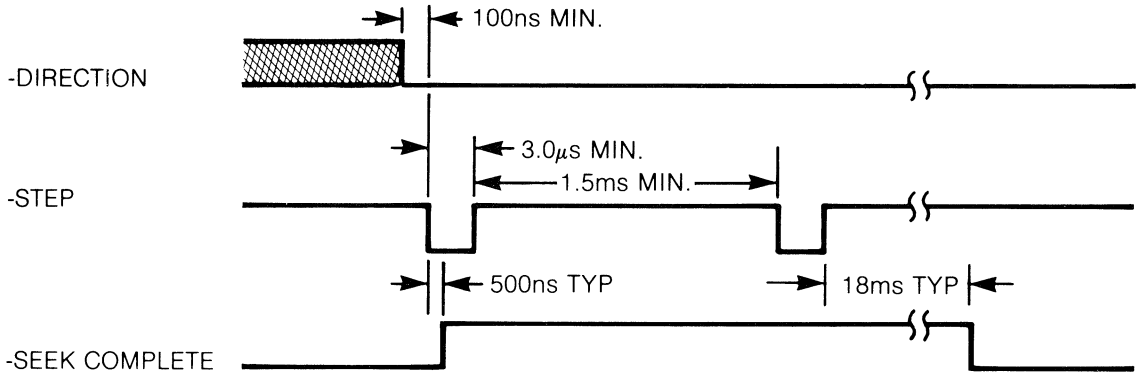


Figure 5 Normal Step Mode

- Normal Step Mode- In this mode, the read/write heads will move at the rate of the incoming step pulses. The minimum time between successive steps is 1.5ms, with a minimum pulse width of 3.0μs. Refer to Figure 5.

- Buffered Step Mode- In this mode, the step pulses are received at a high rate and buffered into a counter. After the last step pulse, the read/write heads will begin stepping the desired number of cylinders and SEEK COMPLETE (Refer to Section 4.1.2.5) will go true after the read/write heads settle on the cylinder. *This mode of operation is automatically selected when the time between step pulses is the less than 200μsec.*

  100 ns after the last step pulse has been sent to the drive, the DRIVE SELECT line may be dropped and a different drive selected.

  The maximum time between steps is 200μs with a minimum pulse width of 3.0μs. (Refer to Figure 6).

NOTE: A high pitched noise may be present if AC and DC power are applied to an SA1000 with the data cable disconnected (no timing clock signal). It's the stepper motor trying to return to track zero with no step pulses present. While this will not damage the drive, this condition should be avoided.

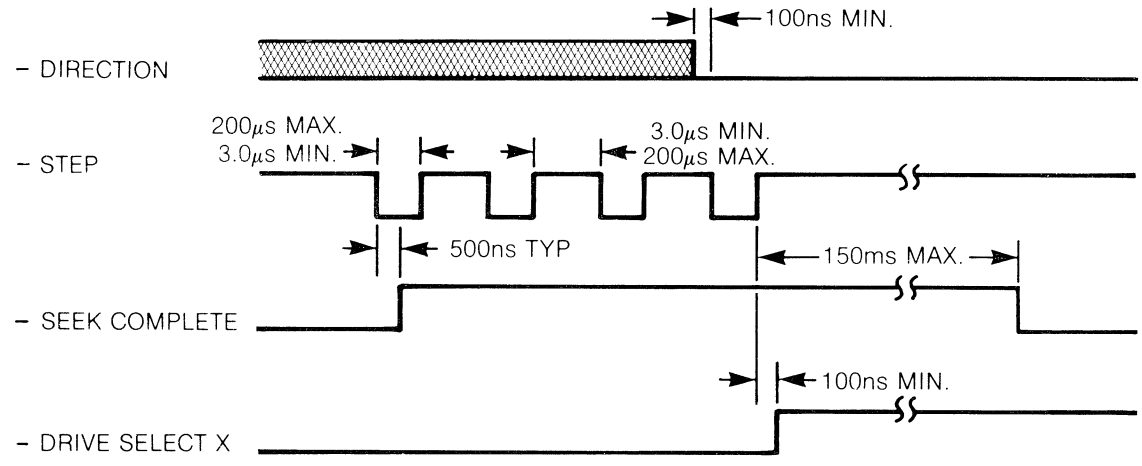


Figure 6 Buffered Step Mode

NOTES: 1. Step pulses with periods between 200μs and 1.5ms are not permitted. Seek accuracy is not guaranteed if this timing requirement is violated.

2. A 220/330Ω resistor pack,located at IC location 8C, allows for Step line termination .

4.1.1.4 HEAD SELECT 2^0 and 2^1

These two lines provide for the selection of each individual read/write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. When all HEAD SELECT lines are false, head 0 will be selected. Table 1 shows the HEAD SELECT SEQUENCE and model variations for the HEAD SELECT lines. (Refer to Figure 7 for the timing sequences).

A 220/330Ω resistor pack, located at IC location 8C, allows for input line termination.

HEAD SELECT LINE 2^0	HEAD SELECT LINE 2^1	HEAD# SELECTED SA1002	HEAD# SELECTED SA1004
1	1	0	0
1	0	1	1
0	1	-	2
0	0	-	3

Table 1 Head Select (1 = False, 0 = True)

4.1.1.5 WRITE GATE

The active state of this signal (logical zero level) enables WRITE DATA to be written onto the disk. The inactive state of this signal (logical one level) enables data to be transferred from the drive and enables STEP pulses to reposition the head arm.

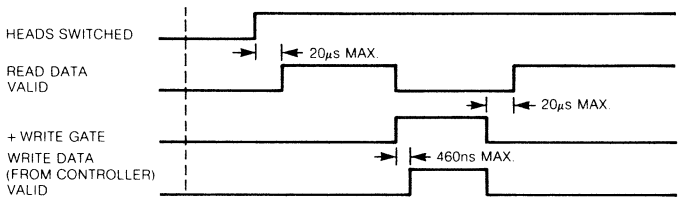


Figure 7 Head Selection Timing

A 220/330Ω resistor pack, located at IC location 8C, allows for termination of this line.

4.1.1.6 REDUCED WRITE CURRENT

When this interface signal is low (true) the lower value of Write Current is selected (for writing on cylinders 128 through 255). When this signal is high (false), the higher value of Write Current is selected (for writing on cylinders 0 through 127). A 220/330Ω resistor pack, located at IC location 8C, allows for line termination.

4.1.2 CONTROL OUTPUT LINES

The control output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at logical zero (true), with a maximum voltage of 0.4V measured at the driver. When the line driver is at logical one (false) the driver transistor is off and the collector cut off current is a maximum of 250 microamperes.

All J1 output lines are enabled by their respective DRIVE SELECT line.

Figure 8 shows the recommended control signal driver/receiver combination.

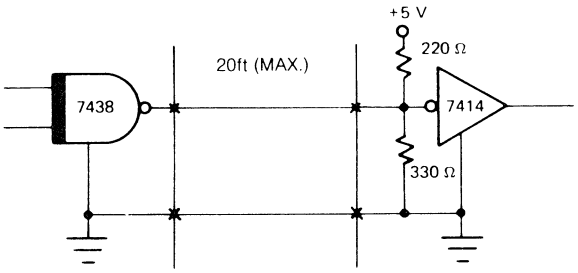


Figure 8 Control Output Driver/Receiver Combination

4.1.2.1 TRACK 000

This interface signal indicates a true state (logical zero) only when the selected drive's read/write heads are at track zero (the outermost data track) and the access circuitry is driving current through phase one of the stepper motor. This signal is false (logical one) when the selected drive's read/write head is not at track zero.

4.1.2.2 INDEX

The drive provides this interface signal once each revolution (19.2ms) to indicate the beginning of the track. Normally, this signal is a logical one and makes the transition to logical zero for a period of approximately 10μs once each revolution. Refer to Figure 9.

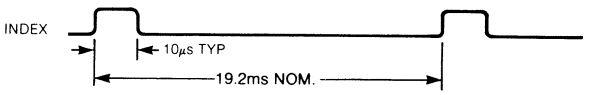


Figure 9 Index Timing

4.1.2.3 READY

This interface signal when true (logical zero), together with SEEK COMPLETE, indicates that the drive is ready to read, write, or seek and that the signals are valid. When this line is false (logical one), all writing to the disk and seeking is inhibited at the drive.

Ready will be true after the drive is 95 ± 2% up to speed. The typical time for READY to become true after power on is 5 seconds.

4.1.2.4 WRITE FAULT

This signal when active (logical zero) is used to indicate that a condition exists at the drive that could cause improper writing on the disk. A WRITE FAULT occurs whenever one of two conditions occur:

- WRITE CURRENT in the head without WRITE GATE active.
- Multiple heads selected.

To reset the WRITE FAULT line, deselect the drive for at least 500 ns.

4.1.2.5 SEEK COMPLETE

SEEK COMPLETE will go true (logical zero) when the read/write heads have settled on the final track at the completion of a seek. Reading or writing should not be attempted until SEEK COMPLETE is true.

SEEK COMPLETE will go false in two cases:

- A recalibration sequence is initiated (by the drive logic) at power on if the read/write heads are not over track zero.
- 500 NS typical, after the leading edge of a STEP pulse (or the first of a series of step pulses).

4.1.3 DATA TRANSFER LINES

All lines associated with the transfer of data between the drive and the host are differential in nature and may not be multiplexed. These three pairs of balanced signals are: MFM WRITE DATA, MFM READ DATA, and TIMING CLOCK and are provided at the J2/P2 connectors on all drives. Figure 10 illustrates the driver/receiver combination.

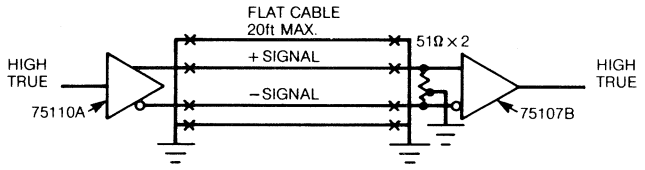


Figure 10 Data Transfer Line Driver/Receiver Combination

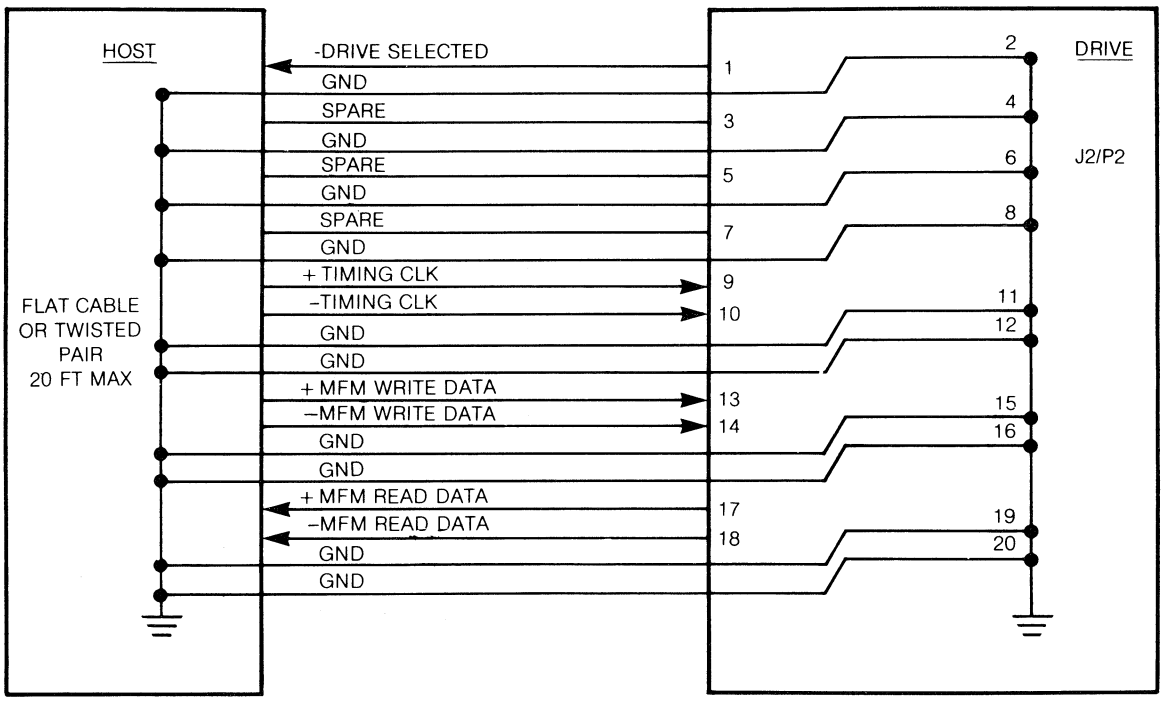


Figure 11 J2 Interface Connection

4.1.3.1 MFM WRITE DATA

This pair of signals defines the transitions (bits) to be written the on disk. + MFM WRITE DATA going more positive than -MFM WRITE DATA will cause a flux reversal on the track under the selected head providing WRITE GATE is active. This signal must be driven to an inactive state (+ MFM WRITE DATA more negative than -MFM WRITE DATA) by the host system when in the read mode. Figure 12 shows the timing for MFM WRITE DATA.

4.1.3.2 MFM READ DATA

The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of MFM READ DATA lines. This transition of the + MFM READ DATA line going more positive than -MFM READ DATA line represents a flux reversal on the track of the selected head while WRITE GATE is inactive. Refer to Figure 12.

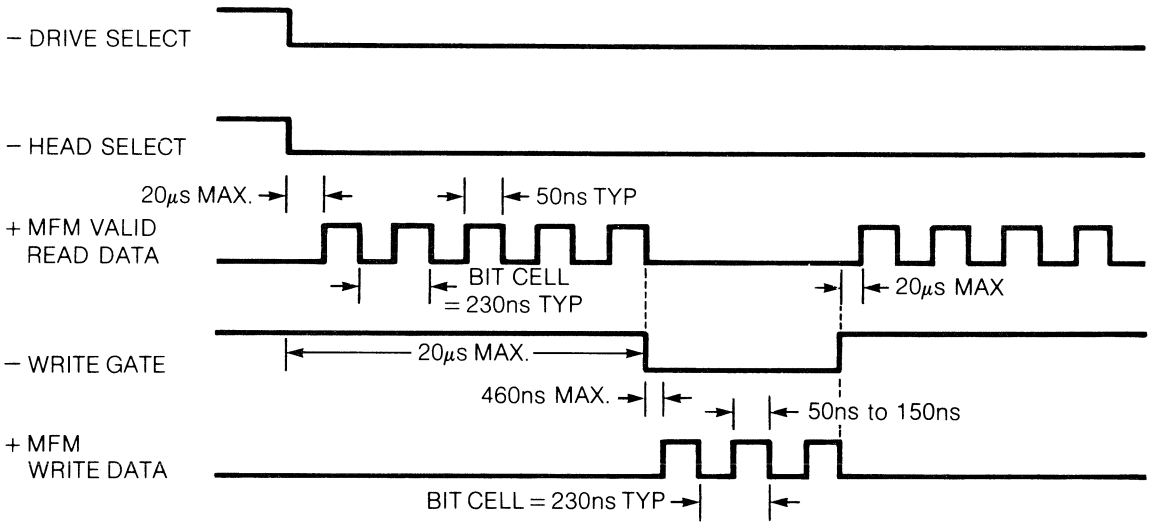


Figure 12 MFM Read/Write Data Timing

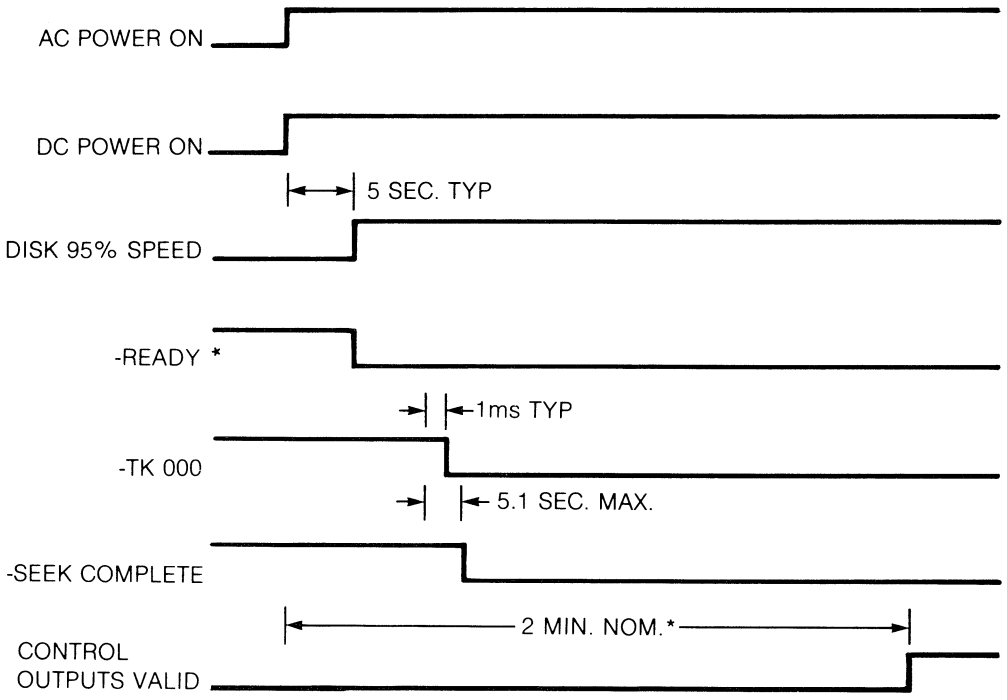
4.1.3.3 TIMING CLOCK

This is a differential pair of clock signals (provided by the host) having a 50% (nominal) duty cycle and a 3.6866 μs ± .1% period. The frequency of this clock is exactly 1/16 the bit frequency for the standarized write data. Phase relationship between TIMING CLOCK and MFM WRITE DATA need not be maintained by the host for the SA1000 interface. The TIMING CLOCK is used by the drive logic for clocking and timing purposes.

4.1.4 SELECT STATUS

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED line is driven by a TTL open collector driven as shown in Figure 8. This signal will go active only when the drive is programmed as drive X (X = 1, 2, 3 and 4) by proper placement of the shorting plug in the vicintiy of J1, and that DRIVE SELECT X line at J1/P1 is activated by the host system.



*The drive will bring Ready active as soon as the disk is rotating at 95% of normal speed. It is now safe to seek the drive but an additional 2 minutes should be allowed for thermal expansion to stabilize.

Figure 13 General Control Timing Requirement

4.1.5 GENERAL TIMING REQUIREMENTS

The timing diagram as shown in Figure 13 shows the necessary sequence of events (with associated timing restrictions) for proper operation of the drive.

Note that a recalibrate to track zero sequence is initiated automatically at every DC power on. For this auto-recal sequence to function, the following conditions must be met:

- TIMING CLOCK is supplied to the drive (via J2/P2).
- STEP Input at J1/P1 is held inactive.
- Spindle is spinning at regular speed (if AC and DC are switched on at the same time, stepping action will not occur until spindle is up to speed).

4.2 POWER INTERFACE

The SA1000 requires both AC and DC power for operation. The AC power is used for the drive motor and the DC power is used for the electronics and the stepper motor.

4.2.1 AC POWER

The AC power is via the connector J4 mounted at the center rear of the drive. Table 2 shows a listing of the AC power requirements.

4.2.2 DC POWER

DC power to the drive is via connector J5/P5 located on the solder side of the PCB. The three DC voltages and their specifications along with their J5/P5 pin designations, are outlined in Table 3.

NOTE: The SA1000 is shipped with DC (base casting) and AC ground (drive motor) connected together with a ground strap located on the drive motor. If the system configuration requires the separation of these grounds, remove the strap.

CONN P4	60HZ		50HZ	
	110V (STANDARD)	203/230V	100V	220V
1 2 3	90-127V FRAME GND 90-127V RTN	180-253V FRAME GND 180-253V	90-127V FRAME GND 90-127V RETURN	180-253V FRAME GND 180-253V
MAX INRUSH CURRENT (3 SEC)	4.0A	TBS	TBS	TBS
MAX RUN CURRENT	1.0A	0.5A	1.1A	0.6A
FREQ TOL	±0.5 HZ		±0.5 HZ	

Table 2 AC Power Requirements

P5 CONNECTOR	CURRENT			
	STEADY STATE		STEPPING	
	MAX.	TYP	MAX.	TYP
+24 ± 2.4V 1V. P-P MAX. Ripple	0.25A	0.20A	3.3A	2.8A
+5 ± 0.25V 50mV P-P MAX. Ripple	4.1A	3.6A	2.5A	2.0A
(-7 TO -16V OPT) -5 ± 0.25V 50mV P-P MAX. Ripple	0.25A	0.20A	0.25A	0.20A

Table 3 DC Requirements

5.0 PHYSICAL INTERFACE

The electrical interface between the SA1000 and the host system is via four connectors. The first connector, J1, provides control signals for the drive; the second connector, J2, provides for the radial connection of the read/write signals; the third connector, J5, provides DC power; and the fourth connector, J4, provides AC power and frame ground. Refer to Figure 14 for the connector locations.

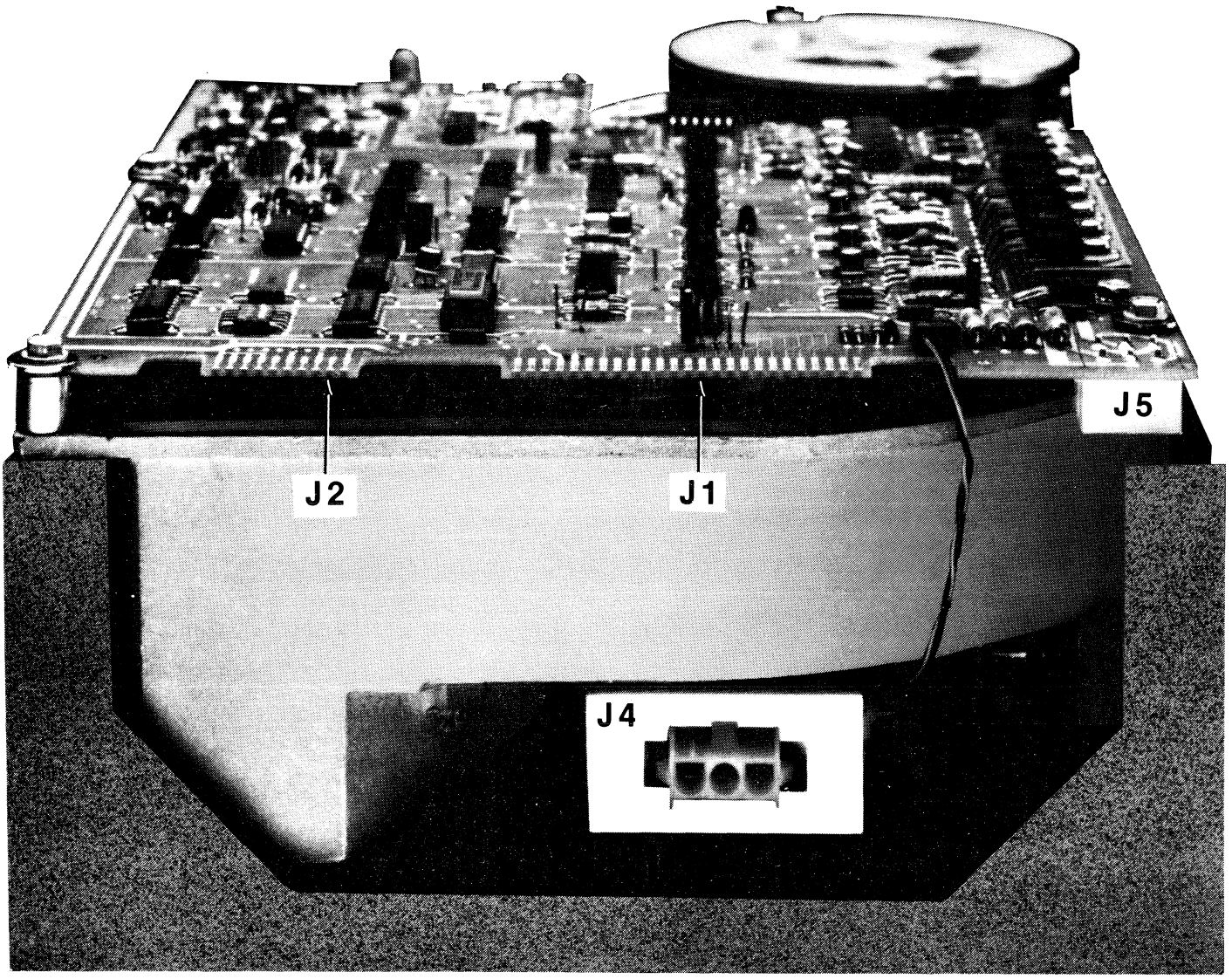


Figure 14 Connector Locations

5.1 J1/P1 CONNECTOR

Connection to J1 is through a 50 pin PCB edge connector. The dimensions for this connector are shown in Figure 15. The pins are numbered 1 through 50 with the even numbered pins located on the component side of the PCB and odd pins located on the non-component side of the PCB. Pin 2 is located on the end of the PCB connector closest to the J2 connector and is labeled. A Key Slot is provided between pins 4 and 6. The *recommended mating connector* for P1 is Scotchflex ribbon connector P/N 3415-0001.

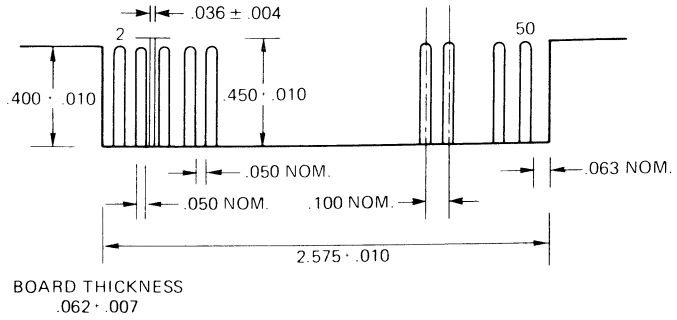


Figure 15 J1 Connector Dimensions

5.2 J2/P2

Connection to J2 is through a 20 pin PCB edge connector. The pins are numbered 1 through 20 with the even numbered pins located on the component side of the PCB. The *recommended mating connector* for P2 is a Scotchflex ribbon connector P/N 3461-0001. A key slot is provided between pins 4 and 6. Figure 16 shows the dimensions for the connector.

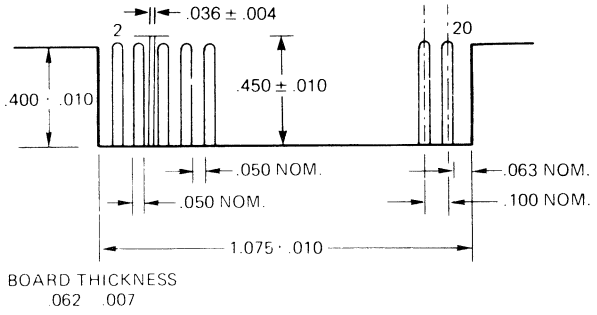


Figure 16 J2 Connector Dimensions

5.3 J5/P5

The DC power connector, J5, is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0, mounted on the non-component side of the Control PCB. The *recommended mating connector,* P5, is an AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. The J5 pins are labeled on the connector. Refer to Figure 17.

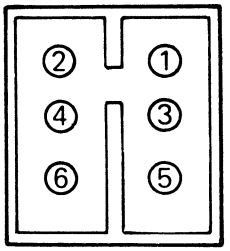


Figure 17 J5 Connector

5.4 J4/P4

AC power and frame ground are interfaced through a 3 pin connector, J4, located on the end of the drive. The AMP part number for J4 is 1-480701-0 with pins AMP P/N 350687-1 and 350654-1 (ground pin), refer to Figure 18. The *recommended mating connector,* P4, is AMP socket P/N 1-480700-0 with AMP pins P/N 350536-1.

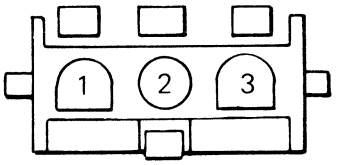


Figure 18 J4 Connector

IMPORTANT NOTE:

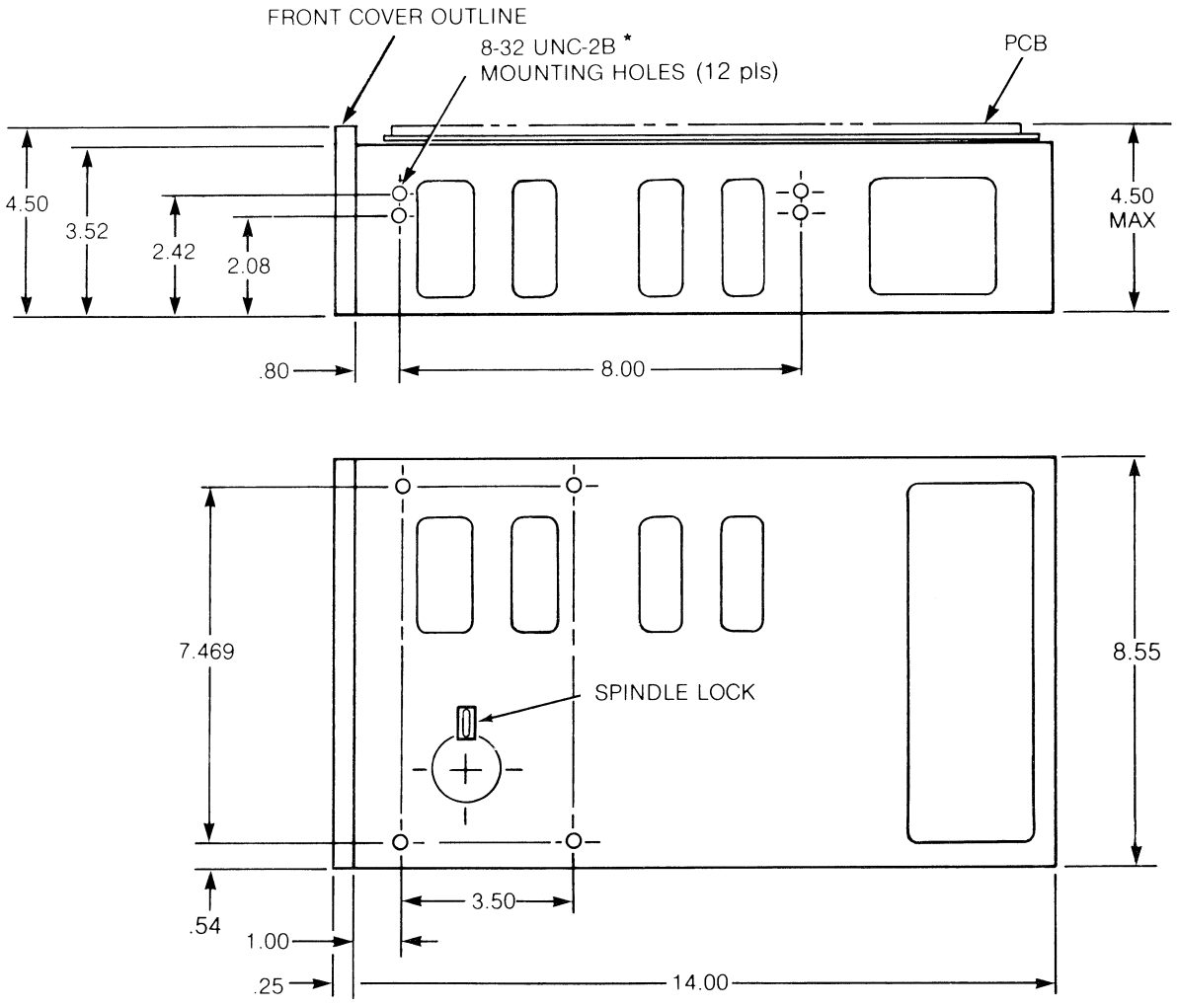
Spindle lock shown in figures 19 & 20 must be installed whenever drive is being transported. Damage to the magnetic heads, disks, or both may occur if spindle is not locked during shipment.

6.0 PHYSICAL SPECIFICATIONS

This section describes the mechanical dimensions and mounting recommendations for the SA1000. Refer to Figures 19 and 20 for the dimensions.

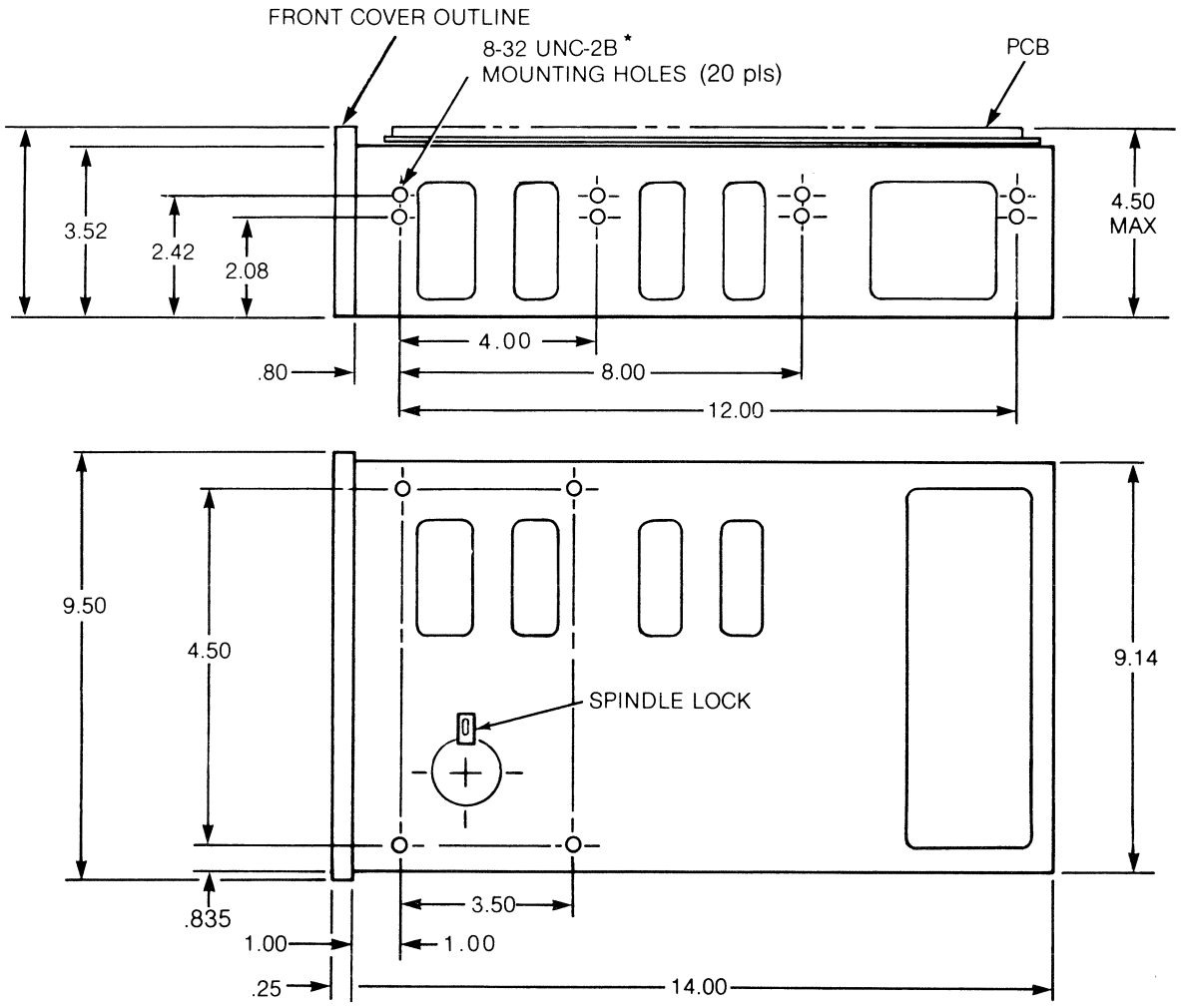
The SA1000 is capable of being mounted in either one of the following positions:

- Vertical - on either side
- Horizontal - PCB Up.



*EARLY UNITS MAY HAVE .146 DIA THRU HOLES

Figure 19 Rack Mount Physical Dimensions



*EARLY UNITS MAY HAVE .146 DIA THRU HOLES

Figure 20 Standard Mount Physical Dimensions

7.0 MEDIA DEFECT & ERRORS

Introduction

In high density digital recording storage systems it is necessary to increase the reliability or improve the operational performance by providing an error detection and correction scheme. For disk storage systems, the predominant error pattern is a burst of errors occurring in one or more tracks which are drop outs (absent bits) or shifted bits from their nominal position more than the data separator can tolerate them to shift. These errors are due to defects in the media as well as signal to noise ratio contributing to probability of error occurrence. The error rate is dependent upon noise and phase characterisitics of media, Read/Write circuits, head and mispositioning of actuator.

What Is The Definition Of An Error?

An error is any discrepancy between recovered data and true correct recorded data. There can be an extra bit or a missing bit, i.e., a "zero" can be transformed into "one" or a "one" can be changed to zero. Errors can be classified into soft or hard errors. Soft errors are generally related to signal to noise ratio of the system and represent marginal conditions of head, media, and Read/Write circuits.

If an error is repeatable with a high probability, it is due to media defect and is termed a hard error.

How Will Shugart Find the Errors?

The errors will be identified prior to shipment and information incorporated in a usable format to enable the user to skip those defective locations per his system capability. Shugart has a unique media test system which exercises the drive in extreme marginal conditions and measures the amplitude and phase distortion of each bit recorded on the disk storage. All drives shipped will be accompanied by an error map reporting any media defects.

Error Reporting

A map will be provided with each drive showing defective bytes as a location from index identified by cylinder and head address. Additionally, cylinder 000 is guaranteed to be error free.

Error Acceptance Criteria

There will be no more than 12 tracks with defects per head of which no more than 4 tracks will contain multiple defects.

A single defect is defined as an error less than 2 bytes long. A multiple defect is defined as an error greater than 2 bytes long, or a single error in several sectors.

8.0 SA1000 TRACK FORMAT

The purpose of a format is to organize a data track into smaller, sequentially numbered, blocks of data called sectors. The SA1000 format is a soft sectored type which means that the beginning of each sector is defined by a prewritten identification (I.D.) field which contains the physical sector address, plus cylinder and head information. The I.D. field is then followed by a user data field.

The soft sectored format is a slightly modified version of the I.B.M. system 34 double density, which is commonly used on 8 inch floppy disk drives. The encoding method used here is modified frequency modulation (MFM).

In the example shown (Figure 21), each track is divided into 32 sectors. Each sector has a data field of 256 bytes in length.

The beginnings of both the I.D. field and the data field are flagged by unique characters called address marks.

An address mark is 2 bytes in length. The first byte is always an "A1" data pattern. This is followed by either an "FE" pattern which is the pattern used to define an I.D. address mark, or an "F8" which is a data address mark pattern.

The "A1" pattern is made unique by violating the encode rules of MFM by omitting one clock bit. This makes the address mark pattern unique to any other serial bit combination.

Each I.D. and data field are followed by a 16 bit cyclic redundancy check (CRC) character used for data verification. Each CRC polynomial is unique for a particular data pattern.

Surrounding The I.D. and data field are gaps called Interrecord gaps.

8.1 GAP LENGHTH CALCULATIONS

8.1.1 GAP 1

Gap 1's purpose is to provide a head switching recovery period so that when switching from one track to another, sequential sectors may be read without waiting the rotational latency time. Gap 1 should be at least 11 bytes long which corresponds to the head switching time of 20 microseconds. Gap 1 is immediately followed by a sync field for the I.D. field of the first sector.

8.1.2 GAP 2

Following the I.D. field, and separating the I.D. field from the data field, is gap 2. Gap 2 provides a known area for the data field write update splice to occur. The remainder of this gap also serves as the sync up area for the data field address mark. The length of gap 2 is determined by the data separator lock up performance.

8.1.3 GAP 3

Gap 3, following the data field, is a speed variation tolerance area. This allows for a situation where a track has been formatted while the disk is running 3% slower than nominal, then write updated with the disk running 3% faster than nominal (power line variations).
Gap 3 should be at least 15 bytes in length.

8.1.4 GAP 4

Gap 4 is a speed tolerance buffer for the entire track. This allows the disk to rotate at least 3% faster than normal without overflowing the track during the format operation. The format operation which writes the I.D. fields, begins with the first encountered index and continues to the next index.

8.2 WRITE PRECOMPENSATION

Whenever two bits are written in close proximity to each other, a phenomenon called pulse superposition occurs, which tends to cause the two bits to move away from each other. This is a large factor of bit shift.

Other phenomenon such as random noise, speed variation, etc., will also cause bit shift, but to a lesser degree.

The effect of bit shift can be reduced by a technique called precompensation which, by detecting which bits will occur early and which bits will occur late, can be done by writing these bits in the opposite direction of the expected shift.

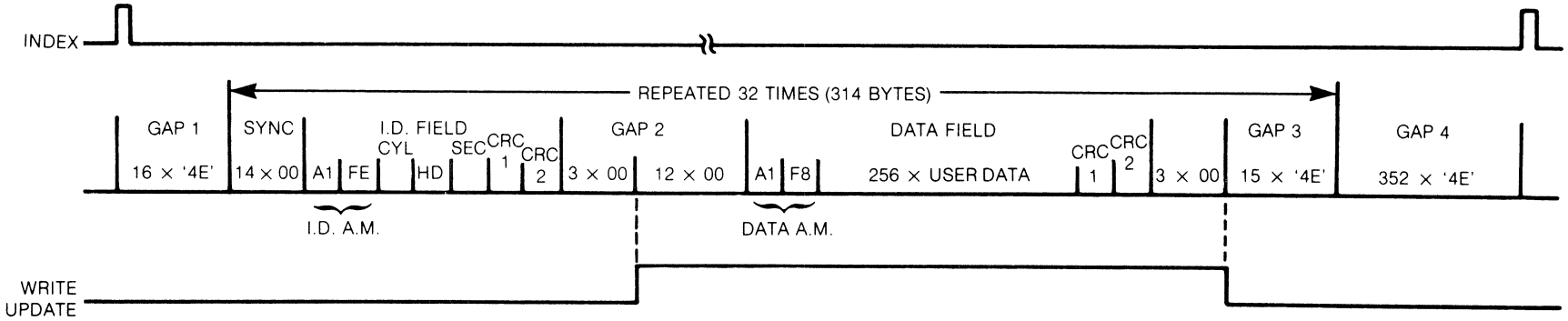
Bit shift is more apparent on the innermost data tracks due to pulse crowding. Therefore, precompensation should only be at track number greater than 128.

The optimum amount of pre-compensation for the SA1000 is 10 nanoseconds for both early and late written bits.
TABLE 4 shows various bit patterns for pre-compensation.

WRITE POSITION	DIRECTION OF SHIFT
0 0 0 0	= On Time Clock
0 0 0 1	= Late Clock
0 0 1 0	= On Time Data
0 0 1 1	= Early Data
0 1 0 0	-----
0 1 0 1	-----
0 1 1 0	= Late Data
0 1 1 1	= On Time Data
1 0 0 0	= Early Clock
1 0 0 1	= On Time Clock
1 0 1 0	= On Time Data
1 1 0 0	-----
1 1 0 1	-----
1 1 1 0	= Late Data
1 1 1 1	= On Time Data

Precompensation Pattern Detection bits are shifted through a 4 bit shift register. Bit is written out of the the third position.

Table 4 Write Precompensation



NOTES:
1. NOMINAL TRACK CAPACITY - 10416 BYTES.
2. MINIMUM TRACK CAPACITY - (NOMINAL - 3% SPEED VARIANCE) 10102 BYTES.
3. WRITE TO READ RECOVERY TIME = 20 MICROSECONDS.
4. HEAD SWITCHING TIME = 20 MICROSECONDS.

Figure 21 Track Format

APPENDIX H: QUANTUM Q2000 8″ FIXED DISK DRIVE MANUAL

QUANTUM

OEM
MANUAL

Q2000
8″ Media Fixed Disk Drive

QUANTUM CORPORATION
2150 Bering Drive
San Jose, CA. 95131
(408) 262-1100

Publication P/N
81-40184

PREFACE

This manual describes the electrical and mechanical characteristics of the Q2000 Series Rigid Disk Drive required by customers who purchase it as an OEM device. It contains timing, electrical and mechanical specifications, and recommended circuitry necessary to interface it to a host controller and data separator.

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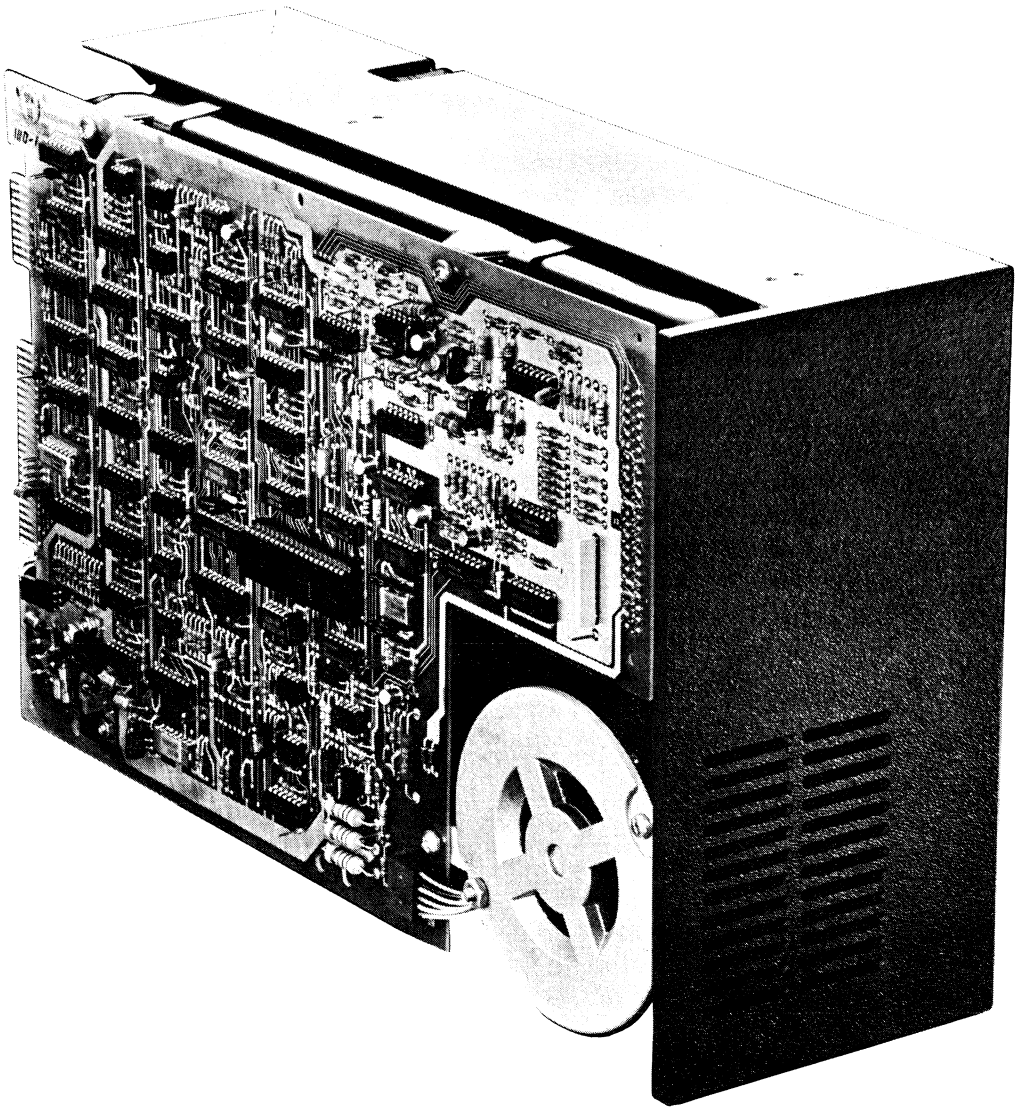


Quantum's new Q2000 8-inch fixed disk drive compatible with industry standard Shugart Associates SA1000.

Figure 1. Q2000 Series Rigid Disk Drive

1.0 INTRODUCTION

1.1 General Description

The Quantum Series 2000 Disk Drive is a random access storage device with one, two, three, or four non-removable 8" rigid disks as storage media. Each disk surface employs one movable head to access the 512 data tracks. The four models of the Q2000 series are Q2010, Q2020. Q2030, and Q2040 with one, two, three, or four disk platters respectively. The Q2010 provides 10.66 megabytes of storage accessed by 2 movable heads. The Q2020 had 21.33 megabyte capacity, the Q2030 has 32.00 megabyte capacity and the Q2040 has 42.67 megabyte capacity with 4, 6 and 8 movable heads respectively. Low cost and drive reliability are achieved through the use of a unique positioning actuator design. The inherent simplicity of mechanical construction and electronic control allows operation with minimal maintenance throughout the life of the drive.

Mechanical and contamination protection for the heads, actuator, and disks is provided by an impact resistant plastic and aluminum enclosure. A self-contained recirculation system supplies clean air through a 0.3 micron filter with another absolute filter allowing pressure equalization with ambient air without contamination.

The Q2000 Series Disk Drive is also supplied with an actuator lock and a spindle lock for shipping protection. In addition, the heads are positioned in a landing and shipping zone on the disk surfaces which is inside track 511. The heads are always positioned in this zone when power is removed so that the heads never rest upon any area of the disk surface where data is written. Upon power up, the heads do not move from this area until the disk is rotating fast enough for the heads to fly.

An external data separator is required to provide MFM encoding/decoding, write precompensation, a crystal controlled write oscillator, and address mark writing and detecting. Quantum's Q2200 data separator may be used for these functions. Most controllers, however, integrate these functions into the controller design. The Q2000 fixed disk drive interface is similar to the Shugart

8" floppy drive and a superset of Shugart's SA1000 series disk drive interface. The Q2000 series disk drive is designed with the same form factor and power supply voltage requirements as 8" floppy drives.

Key Features:

- Storage Capacity of 10, 20, 30, or 40 megabytes
- Winchester design reliability
- Same physical size and mounting as 8" floppy drives
- Uses the same D.C. voltages as 8" floppy and SA1000 drives
- Proprietary, rotary, high resolution, quiet, head position actuator
- 4.34M bits/second transfer rate
- Shugart SA1000 interface compatible
- Microprocessor controlled temperature compensation servo

1.2 SPECIFICATION SUMMARY

1.2.1 Physical Specifications

ENVIRONMENTAL LIMITS

Ambient temperature
= 50° to 115°F (10° to 46°C)
Relative Humidity
= 8% to 80%
Maximum wet bulb
= 78° non-condensing

AC POWER REQUIREMENTS

50/60Hz ±0.5Hz
100/115VAC Installations =
90-127V at 1.0A Typical
200/230VAC Installations =
180-253V at 0.5A Typical

DC VOLTAGE REQUIREMENTS

+24VDC ±10% 1.25A Typical
+5VDC ±5% 1.0[1] Typical
−5VDC ±5% (−7 to −16VDC optional) 0.2A Typical

MECHANICAL DIMENSIONS

Height = 4.50 in.
(114.3mm)
Width = 8.55 in.
(217.2mm)
Depth = 14.25 in.
(362.0mm)
Weight = 17 lbs.
(7.7Kg)

HEAT DISSIPATION
= 235 BTU/HR. TYP (70 Watts)

1.2.2 Reliability Specification

MTBF: 8,000 POH typical usage
PM: not required
MTTR: 30 minutes
Component Life: 5 years

Error Rates

Soft read errors: 1 per 10^{10} bits read
Hard read errors: 1 per 10^{12} bits read
Seek errors: 1 per 10^{6} seeks

1.2.3 Performance specifications

	Q2010	Q2020	Q2030	Q2040
Capacity				
Unformated				
Per drive	10.66Mb	21.33Mb	32.00Mb	42.66Mb
Per surface	5.33Mb	5.33Mb	5.33Mb	5.33Mb
Per track	10.40Kb	10.40Kb	10.40Kb	10.40Mb
Formatted (MFM)				
Per drive	8.40Mb	16.80Mb	25.20Mb	33.60Mb
Per surface	4.20Mb	4.20Mb	4.20Mb	4.20Mb
Per track	8.20Kb	8.20Kb	8.20Kb	8.20Mb
Per sector	256 Bytes	256 Bytes	256 Bytes	256 Bytes
Sectors/TK	32	32	32	32
Transfer Rate	4.34Mbits/sec	4.34Mbits/sec	4.34Mbits/sec	4.34Mbits/sec
Access Time				
TK to TK	15 ms	15 ms	15 ms	15 ms
Average	50 ms	55 ms	60 ms	65 ms
Maximum	100 ms	100 ms	100 ms	100 ms
Avg. Latency	10 ms	10 ms	10 ms	10 ms

1.2.3 Functional Specifications

Rotational speed	3000 RPM	3000 RPM	3000 RPM	3000 RPM
Recording Density	6600 bpi	6600 bpi	6600 bpi	6600 bpi
Flux Density	6600 fci	6600 fci	6600 fci	6600 fci
Track Density	345 tpi	345 tpi	345 tpi	345 tpi
Cylinders	512	512	512	512
Tracks	1024	2048	3072	4096
R/W Heads	2	4	6	8
Disks	1	2	3	4
Index	1	1	1	1

Rotational speed, recording, flux and track densities differ from SA1000 values to accomodate Quantum track position servo and higher disk capacity while retaining Shugart Associates SA1000 and SA1400 format and interface compatibility.

2.0 FUNCTIONAL CHARACTERISTICS

2.1 General Operation

The Series 2000 fixed disk drive consists of read/write and control electronics, read/write heads, head positioning mechanism, media, and air filteration system. These components perform the following functions:

- Interpret and generate control signals
- Position the heads over the selected track with appropriate corrections to compensate for thermal effects on track location
- Read and write data
- Provide a contamination free environment around the media
- Perform diagnostics on the head positioning and servo systems

2.2 Read/Write And Control Electronics

The electronics for the drive are packaged on two printed circuit boards, the control PCB and the Transducer PCB.

2.2.1 Transducer PCB

The Transducer PCB contains the following circuits:

- Coarse servo transducer detector circuit
- Raw track 0 detector circuit
- AGC circuit for servo and track 0 sensors
- Head select diode matrix

2.2.2 Control PCB

The main PCB contains the following circuits:

- Index detector circuit
- Head positioning actuator predrivers
- Microprocessor for diagnostics and fine servo control as well as step buffers.
- Read/write amplifier/drivers
- Head select circuits
- Drive select circuit

- Drive ready circuit
- Write fault detection circuit
- Power on reset circuit
- Track 0 indicator circuit

2.3 Drive Mechanism

The spindle rotates at 3000 rpm through a belt drive from an AC motor. Either 50 or 60Hz power is accomodated by changing the motor drive pulley and belt. 220/230VAC operation can be utilized by a motor change.

2.4 Read/Write Head And Disks

The recording media is a lubricated thin magnetic oxide coated on an 8 inch diameter aluminum substrate. This lubricated coating formulation, together with the low load force/low mass Winchester type flying heads permit reliable contact start/stop operation.

2.5 Head Positioning System

The head positioning system consists of three major elements: rotary torque motor actuator, optical track position encoder, and temperature compensation servo.

2.5.1 Rotary Torque Motor Actuator (Fig. 3)

The read/white heads are mounted on counterbalanced arms attached to the hub of the roatry torque motor. This configuration applies a pure torque to the rotor. The balance system maximizes bearing life and leads to high mechanical stability and maximum vibration resistance.

The motor is of simple construction consisting of a ring magnet, two flat plate pole pieces, a single plane moving coil and two bearings. This system is faster than stepper motors and its performance matches many voice coil actuator systems.

2.5.2 Optical Track Position Encoder

The optical track position encoder is a proven technology utilizing a highly reliable photo etched scale, an LED light source and photodiode sensors. The encoder components are located inside the bubble with the scale attached to the lowermost actuator arm. This system is accurate to over ten times the track density utilized in this product.

2.5.3 Temperature Compensation Servo

The temperature compensation, (fine) servo obtains position feedback directly from the disk surface 50 times each second. This track location coding is embedded between the last inter-record gap and the index pulse. This information is transparent to the controller or host since writing is inhibited by the drive during this servo operation. Compatibility is maintained with like drives by reducing the disk rotational speed by 4%. This servo method places no restrictions on format and allows platter capacities equal to other comparable competitive units.

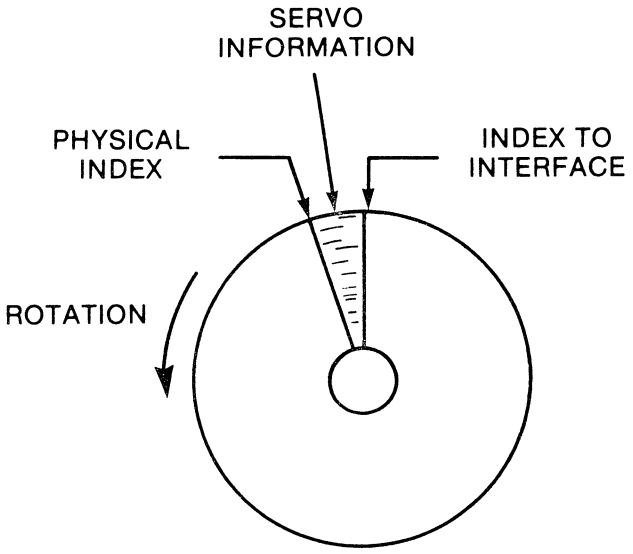


Figure 2. Servo Information Location

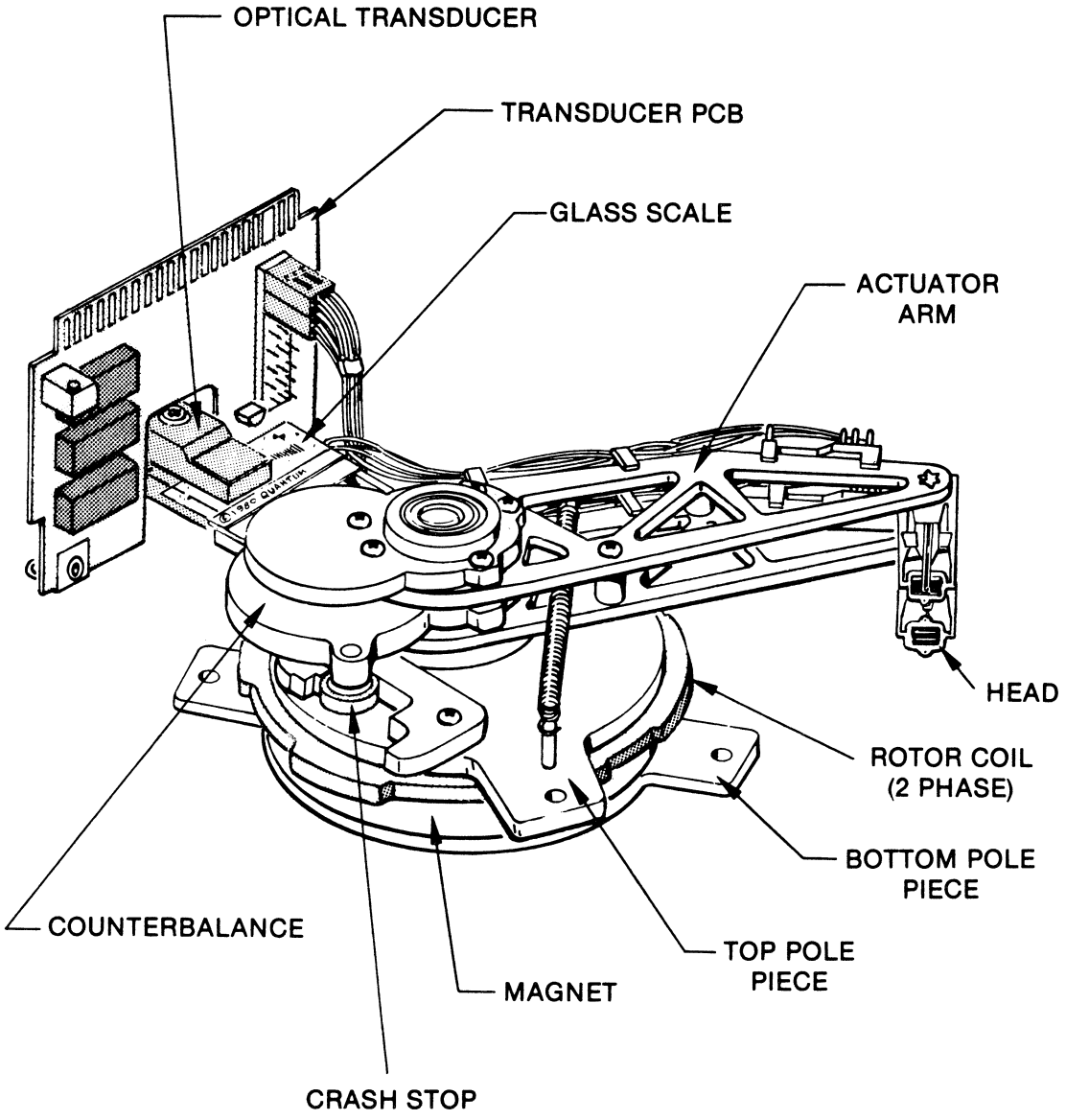


Figure 3. Head Positioning Mechanism

2.6 Air Filtration System (Fig. 4)

The disk(s) and read/write heads are fully enclosed in a module consisting of a casting and a plastic bubble. The module uses an integral recirculatory air system with an absolute (0.3 micron) filter to maintain a clean environment. A separate absolute filter is mounted in the bubble at the lowest pressure area in the system to allow pressure equalization with the ambient air without contamination.

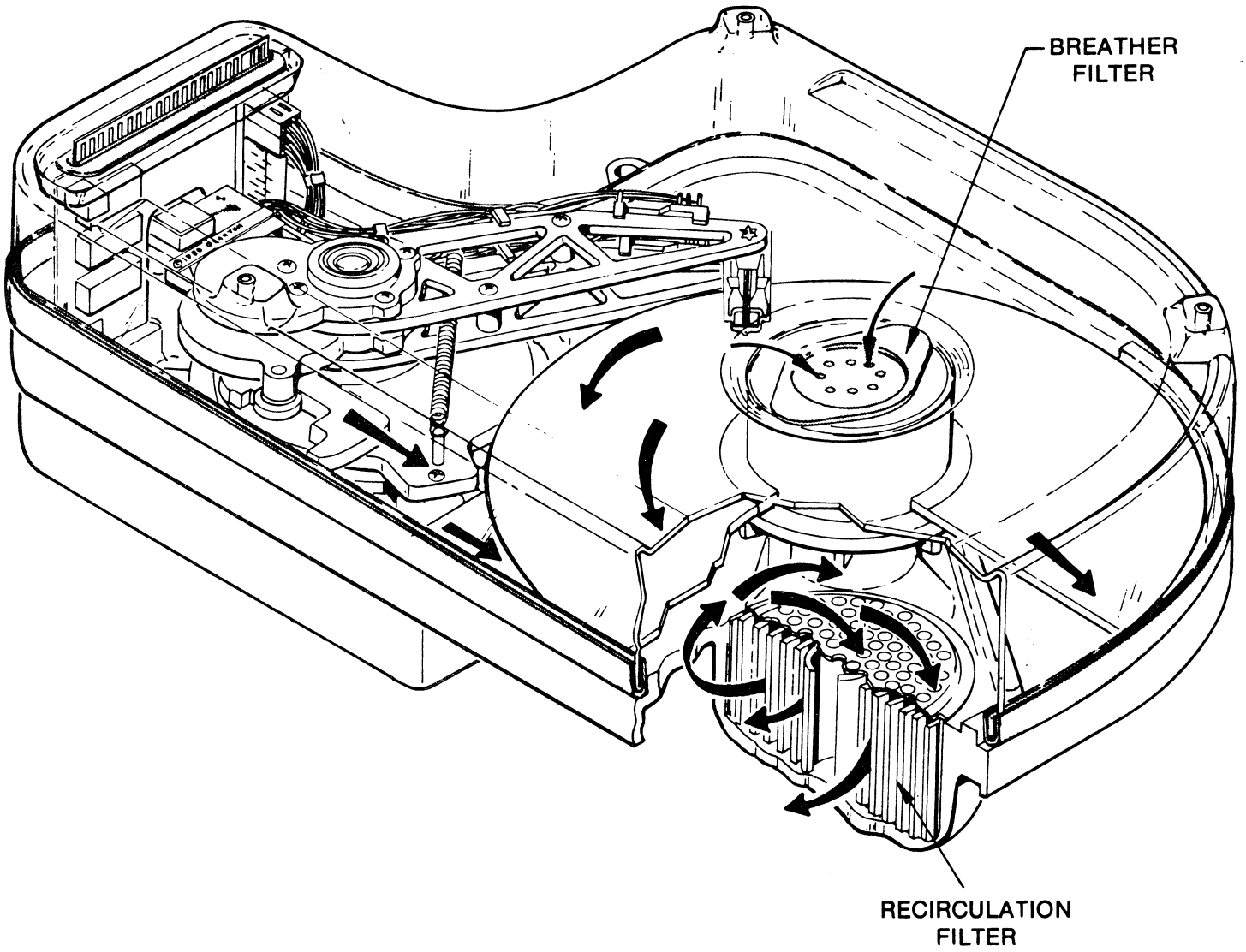


Figure 4. Air Filtration System

3.0 FUNCTIONAL OPERATIONS

3.1 Power Sequencing

No power sequencing is necessary with the Q2000 series drive. Upon power up, seeking is inhibited until the disk is at 90% of its normal rotational speed. Upon attaining 90% of the normal speed the READY signal will be presented to the controller interface and the drive will initiate a recalibrate sequence. The recalibrate sequence is:

1. Seek to track 0.
2. Seek to track 508.
3. Determine the offset value and store it in memory.
4. Repeat steps 2 and 3 for tracks 509, 510, and 511.
5. Seek to track 448.
6. Determine the difference between the offset required and the offset determined for track 508. Store this difference value in memory.
7. Repeat steps 5 and 6 for tracks 384, 320, 256, 192, 128, 64, and 0.

This procedure has established eight zones, each with its own thermal compensation value. These values will be updated with each revolution of the disk thereby providing real time tracking and adjustment for thermal drift. The initial recalibrate sequence takes approximately 3 seconds to complete and "SEEK COMPLETE" will be false during this time.

3.2 Drive Selection

Drive selection occurs when one of the 4 drive select lines is activated. Only the drive appropriately jumpered will respond to input signals and gate output signals to the controller.

3.3 Track Accessing

Read/write head positioning is accomplished by:

a) Deactivating write gate

b) Activating the appropriate drive select line

c) Assuring that the drive is ready and seek complete is true by checking the ready and seek complete lines

d) Select the appropriate direction

e) Pulse the step line

Stepping can occur in either the normal or buffered modes. In the normal stepping mode, the heads are repositioned at the rate of the incoming step pulses. In the buffered step mode, incoming step pulses are buffered in the microprocessor. When all of the steps have been received, they are issued at a ramped stepping rate to the actuator motor.

Each pulse will cause the heads to move one track position in or out depending on the level of the direction in line. A true level on this line will cause steps to be inward while a false level will cause steps outward toward track 0.

3.4 Head Selection

Any of the 8 possible heads may be selected by placing that head's appropriate binary address on the 3 head select lines.

3.5 Read Operation

Reading data from the Q2000 drive is accomplished by:

a) Deactivating the write gate signal

b) Activating the appropriate drive select line

c) Assuring that the drive is ready by checking the ready line

d) Selecting the appropriate head

3.6 Write Operation

Writing data onto the disk is accomplished by:

a) Activating the appropriate drive select line

b) Assuring that the drive is ready by checking the ready line.

c) Clearing any Write Fault conditions if they exist by reselecting the drive

d) Selecting the appropriate head

e) Activating Write Gate and placing MFM data on the Write Data line

4.0 INTERFACE LINES AND PIN ASSIGNMENTS

The interface of the drive is divided into three categories: Signal, DC power, and AC power. Tables I, II and III define the pin assignments for these interface lines. Tables IV and V show the recommended cable types and the grounding configurations at the drive and at the host systems. Signal pins marked SPARE are uncommitted. Those signal pins marked NA should not be used as alternate I/O signal pins if a controller having a floppy disk interface is used. A 4-drive subsystem is shown in Figure 5.

5.0 SIGNAL INTERFACE

The signal interface consists of two categories: Control, and data transfer. All control lines are TTL in nature and either provide signals to the drive (input) or provide signals to the host (output) via interface connector J1/P1. The data transfer signals are differential in nature. They provide data and clocking, either to or from the drive, via the J2/P2 Connector.

5.1 Control Input Lines

The control input signals are of two types: Those intended to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are STEP, DIRECTION, HEAD SELECT 2^0, 2^1 and 2^2, WRITE GATE, REDUCED WRITE CURRENT, and REZERO. The signal which is intended to do the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, or DRIVE SELECT 4.

The input lines have the following electrical specifications. Refer to figure 6 for the recommended circuit.

Logic "0" = True = 0.0V DC to 0.04V DC
@ Iin = 40 MA (max)

Logic "1" = False = 2.5V DC to 5.25V DC
@ Iin = 0 MA (Open)

5.1.1 Drive Select 1 thru 4

DRIVE SELECT when true logically connects the drive to the control lines. Only one DRIVE SELECT line may be active at a time and will allow the drive to respond to input signals and gate outputs.

5.1.2 Direction In

This signal defines direction of motion of the R/W heads when the STEP line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the STEP line the R/W heads will move away from the center of the disk.

Conversely, if this input is shorted to ground or a logical zero level is applied, the direction of motion is defined as "in" and if a pulse is applied to the STEP line, the R/W heads will move toward the center of the disk. A 220/330 ohm resistor pack allows line termination.

5.1.3 Step

This interface line is a control signal which causes the R/W head to move with the direction of motion defined by the DIRECTION IN line.

The access motion is initiated at each logical zero to logical one transition on the trailing edge of this signal pulse. Any change in the DIRECTION IN line must be made at least 100ms before the leading edge of the step pulse.

There are two modes of operaion of stepping the R/W heads, the normal mode and the buffered mode.

5.1.3.1 Normal Step Mode

In this mode of operation the R/W heads will move at the rate of the incoming step pulses. The minimum time between successive steps is 1.0ms. The minimum pulse width is 3.0us. See Figure 6 for normal step mode timing.

5.1.3.2 Buffered Step Mode

In this mode of operation the step pulses are received at a high rate and buffered into a counter. After the last pulse the R/W heads will then begin stepping the appropriate number of cylinders and Seek Complete (see section 4.2.5) will go true after the R/W heads settle at the cylinder.

This mode of operation is automatically selected when the time between step pulses is $\leq$ 200 usec.

100ns after the last step pulse has been sent to the drive, the DRIVE SELECT line many be dropped and a different drive selected.

The minimum time between steps is 3.0us with a pulse witdth of 3.0us minimum. The maximum time between steps is 200us. Refer to Figure 6 for Buffered Step Mode Timing.

Note: 1. Step pulses with periods between 200us and 1.0 ms are not allowed. Seek accuracy is not guaranteed if this restriction is violated.

2. A 220/330 ohm resistor pack allows step line termination.

5.1.4 Head Select 2^0, 2^1, & 2^2

These three lines provide for the selection of each individual read/write heads in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. Heads are numbered 0 thru 7. When all HEAD SELECT lines are false, head 0 will be selected. TAble VI shows the HEAD SELECT decode and model variations for the HEAD SELECT lines. See Figure 11 for timing considerations.

A 220/230 ohm resistor pack allows for termination on each line.

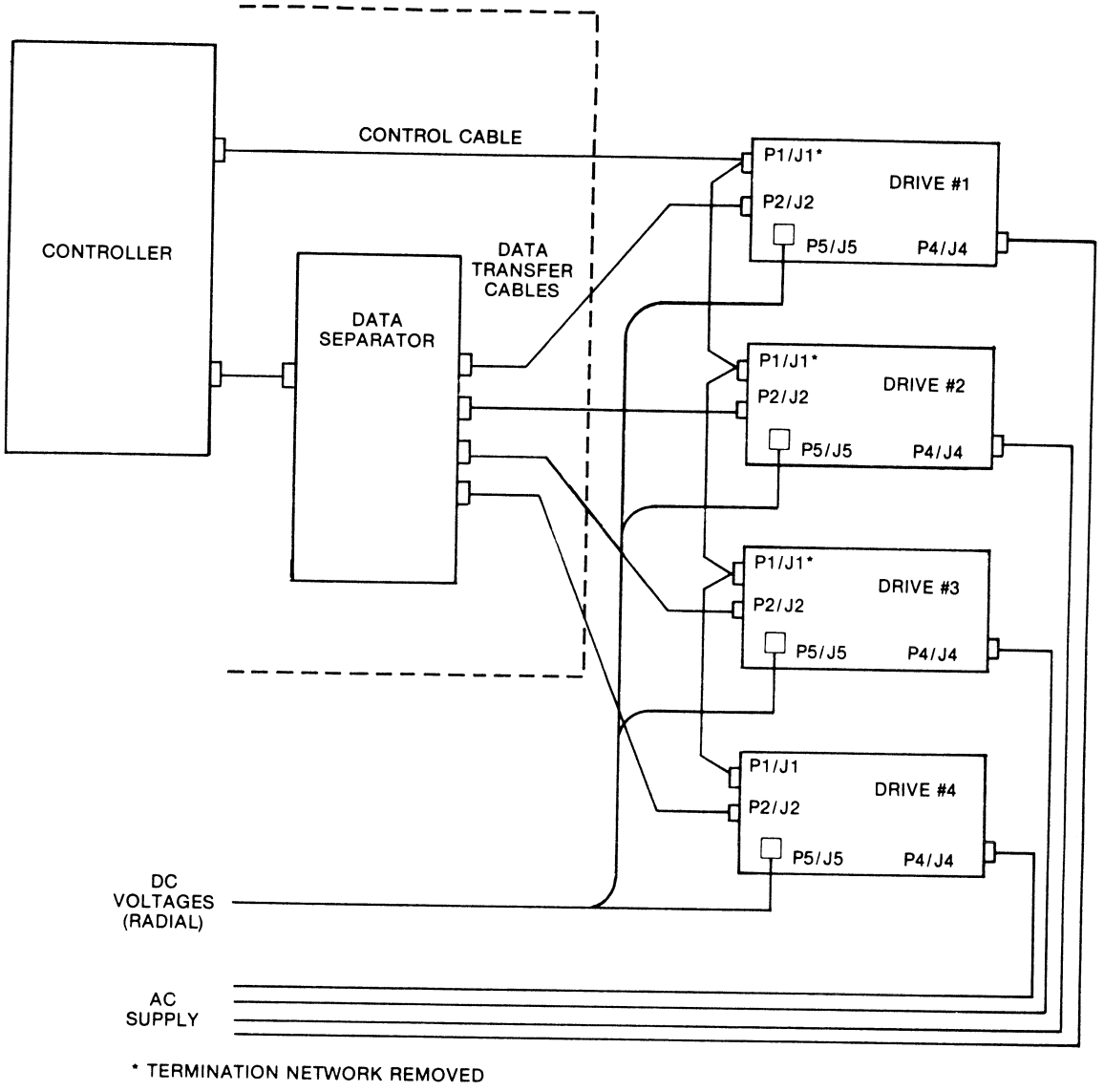


Figure 5. Typical Multiple Drive Connection

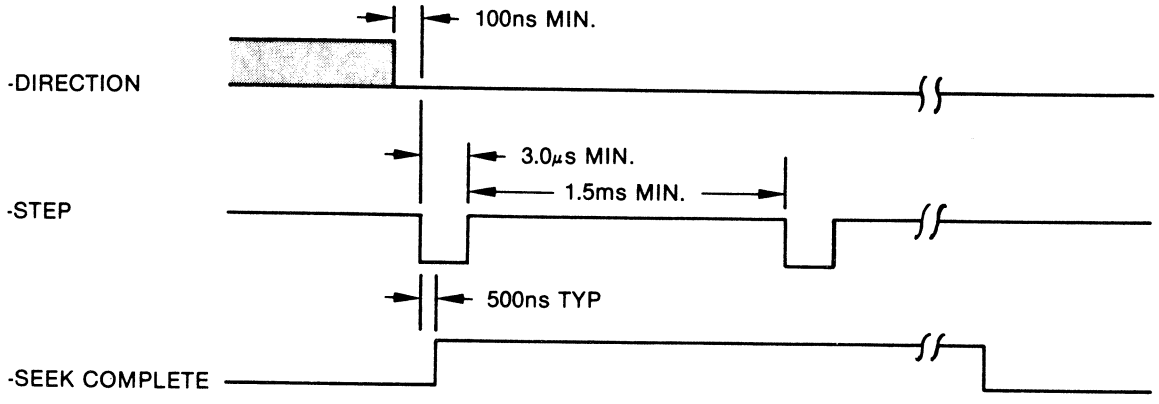


Figure 6. Normal Step Mode Timing

Table IA. J1/P1 Connector Pin Assignment

Ground Return	Signal Pin	Signal Name
1	2	−Reduced Write Current
3	4	−Head Select 2^2
5	6	−Rezero (Jumperable Option)
7	8	−Seek Complete
9	10	−NA
11	12	−NA
13	14	−Head Select 2^0
15	16	−NA
17	18	−Head Select 2^1
19	20	−Index
21	22	−Ready
23	24	−NA
25	26	−Drive Select 1
27	28	−Drive Select 2
29	30	−Drive Select 3
31	32	−Drive Select 4
33	34	−Direction In
35	36	−Step
37	38	−NA
39	40	−Write Gate
41	42	−Track 000
43	44	−Write Fault
45	46	−NA
47	48	−NA
49	50	−NA

Table IB. J2/P2 Connector Pin Assignment

Ground Return	Signal Pin	Signal Name
2	1	−Drive Selected
4	3	Spare
6	5	Spare
	7	Spare
8		GND
	9	+Timing Clk
	10	−Timing Clk
11		GND
12		GND
	13	+MFM Write Data
	14	−MFM Write Data
15		GND
16		GND
	17	+MFM Read Data
	18	−MFM Read Data
19		GND
20		GND

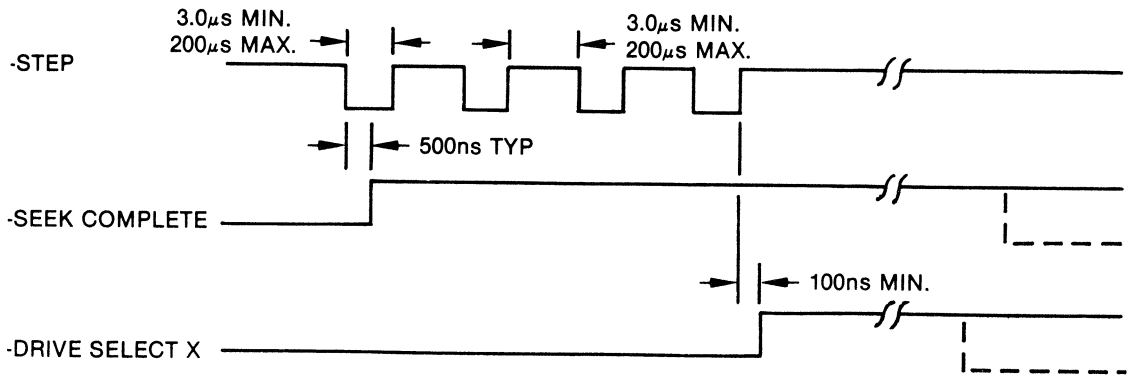


Figure 7. Buffered Step Mode Timing

VOLTAGE		GROUND	
Pin 1	+24 Volts DC	Pin 2	+24 Volt Return
Pin 2	−7 to −16 (−5 OPT) Volts	Pin 3	−7 to −16 (−5 OPT) Volt Return
Pin 5	+5 Volts	Pin 6	+5 Volt Return

Table II. P5 — DC Connector Pin Assignments

Pin 1	Motor Power "A"
Pin 2	Frame Ground
Pin 3	Motor Power "B"

Table III. P4 — AC Connector Pin Assignments

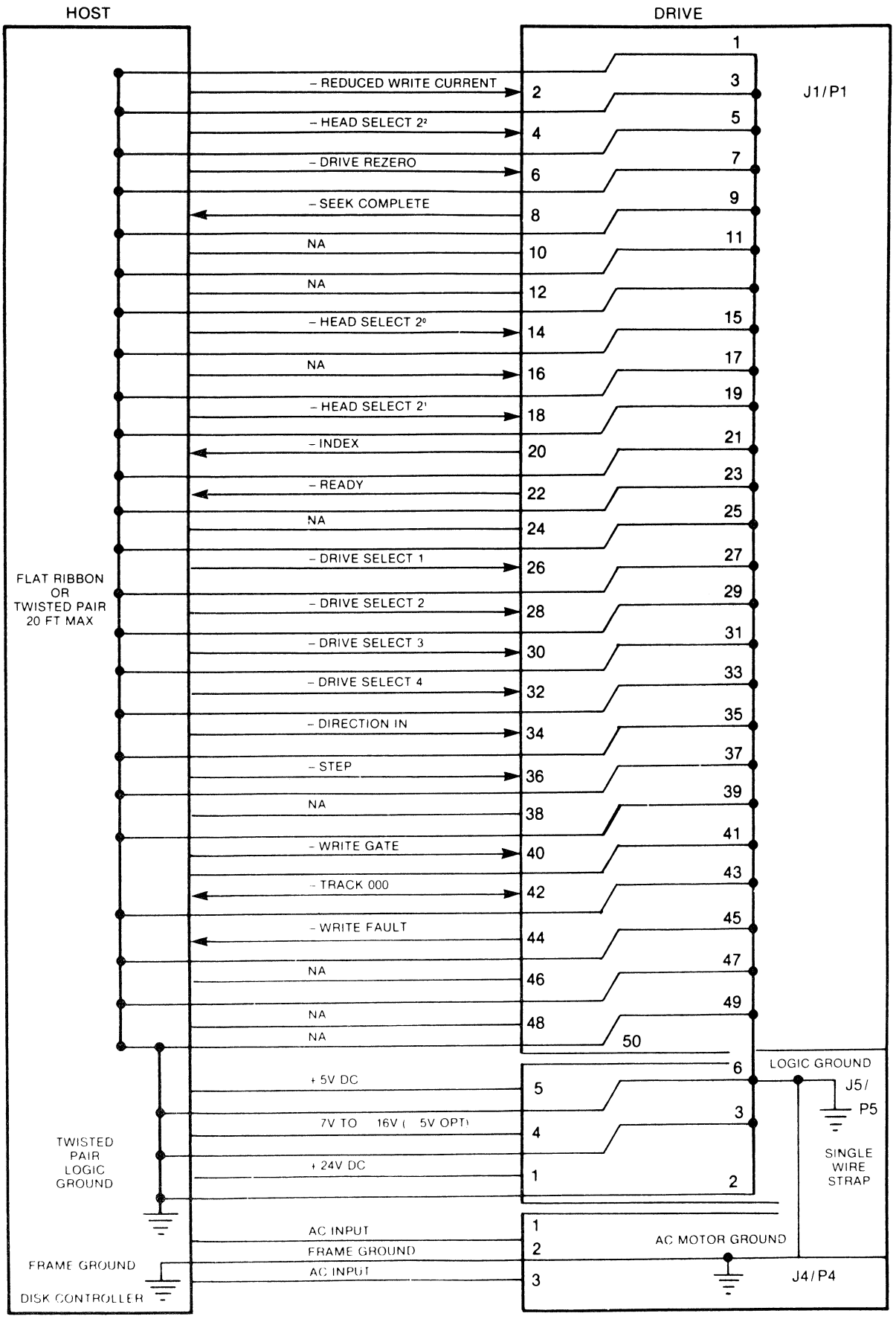


TABLE IV. Interface and Power Connections

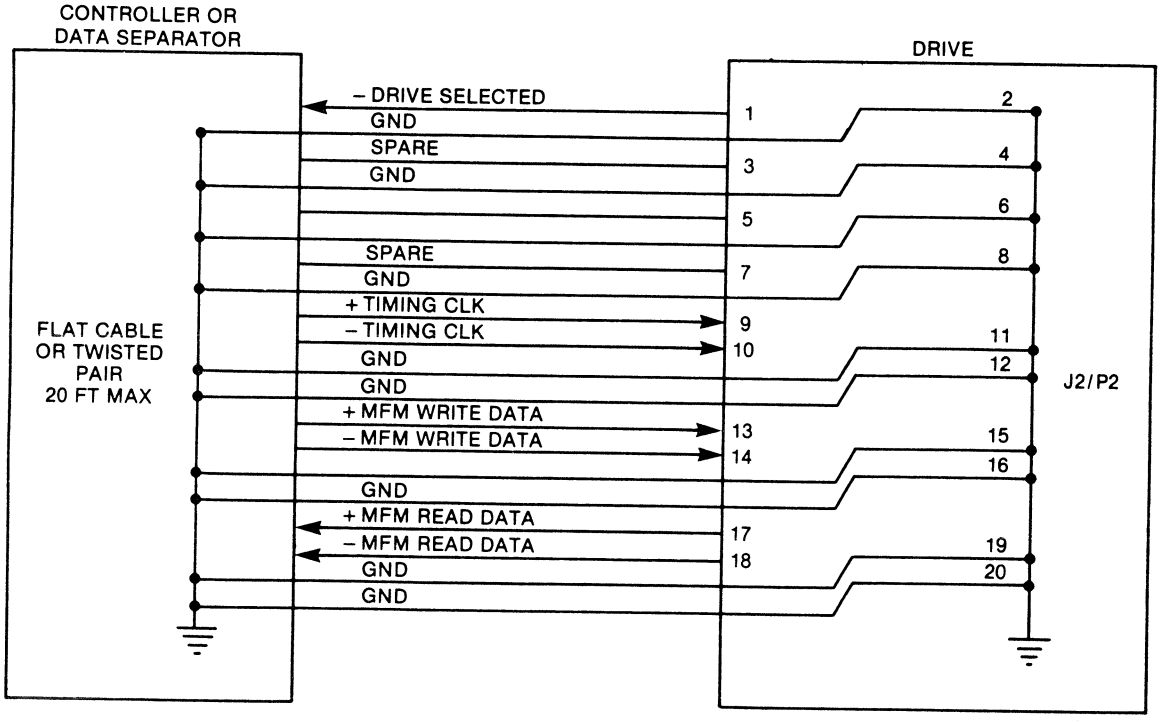


TABLE V. J2 Interface Connection

Head Select Line			Head Selected			
2^2	2^1	2^0	Q2010	Q2020	Q2030	Q2040
0	0	0	0	0	0	0
0	0	1	1	1	1	1
0	1	0	-	2	2	2
0	1	1	-	3	3	3
1	0	0	-	-	4	4
1	0	1	-	-	5	5
1	1	0	-	-	-	6
1	1	1	-	-	-	7

Table VI. Head Select Decode

5.1.5 Write Gate

The active state of this signal, or logical zero, enables write data to be written on the disk. The inactive state of this signal, or logical one level, enables data to be transferred from the drive and enables the STEP pulses to reposition the head arms. A 220/330 resistor pack allows for termination on each line.

5.1.6 Reduced Write Current

When this interface signal is low (true) the lower value of Write Current is selected for writing. It is recommended that the lower value of write current be selected when writing on tracks 256 through 511 and the higher value be selected when writing on tracks 0 through 255. When this signal is high (false), the higher value of Write Current is selected for writing. A 220/330 ohm resistor pack allows for line termination.

5.1.7 Rezero (PCB Option)

When this interface signal is low (true) 50 microseconds minimum, the drive will reset internal microcomputer parameters and will recalibrate to cylinder 0. This feature can be enabled by adding a jumper at the "C" option near connector J1 on the PCB. A 220/330 ohm resistor pack allows for line termination.

5.2 Output Lines

The control output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at logical zero or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in logical one or false state the driver transistor is off and the collector cutoff current is a maximum of 250 microamperes.

All J1 output lines are enabled by the respective DRIVE SELECT LINE.

Figue 8 shows the recommended control signal driver/receiver combination.

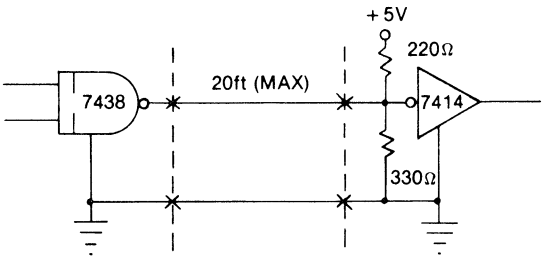


Figure 8. Control Signal Driver/Receiver Combination

5.2.1 Track 000

This interface signal indicates a true state only when drive's R/W heads are positioned at track zero (the outermost data track). This signal is a logical one level, or false state, when the selected drive's R/W head is not at track zero.

5.2.2 Index

The index signal is provided by the drive once each revolution (20.0ms) to indicate the beginning of a track. Normally, this signal is a logical one level and makes the transition to the logical zero level for a period of approximately 10us once each revolution. The leading edge of this pulse must be used for all timing requirements including track format initialization. The 19.2 milliseconds following the leading edge of index are available for read and write during each disk rotation. During the last 800 microseconds before each index pulse, read and write functions are not available to the host (this time is used by internal drive logic for the thermal compensation servo function).

5.2.3 Ready

This interface signal, when true together with SEEK COMPLETE, indicates that the drive is ready to read, write, or seek and that the interface signals are valid. When this line is false, all reading, writing, and seeking are inhibited at the drive, and the R/W heads are automatically positioned at the landing zone (innermost disk radius).

READY will be true after the drive is 90 ± 1% up to speed.

The typical time for READY to become true after power on is 20 seconds.

5.2.4 Write Fault

This signal is provided by the drive and is used to indicate that a condition exists at the drive that caused improper writing on the disk. When this line goes true, further writing is inhibited at the drive until the condition no longer exists AND that the DRIVE SELECT line for that particular drive made inactive for at least 500ns to reset the fault detection circuit. There is one FAULT condition detected and latched. It is:

WRITE CURRENT in the head without WRITE GATE active.

5.2.5 Seek Complete

This line will go true when the R/W heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when SEEK COMPLETE is false.

SEEK COMPLETE will go false in two cases:

(1) A recalibration sequence was initiated (by drive logic) at power on.

(2) 500 ns (typ.) after the leading edge of a step pulse (or the first of a series of step pulses.)
SEEK COMPLETE is gated with DRIVE SELECT. See Figure 7.

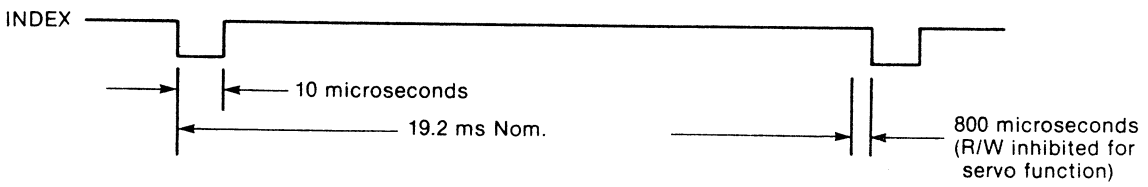


Figure 9. Index Timing

5.3 Data Transfer Lines

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connector on all drives.

The pairs of balanced signals used for data transfer in a standard drive are: MFM WRITE DATA, MFM READ DATA, and TIMING CLK. Figure 10 illustrates the driver/receiver combination used in the Q2000 series drives for data transfer signals.

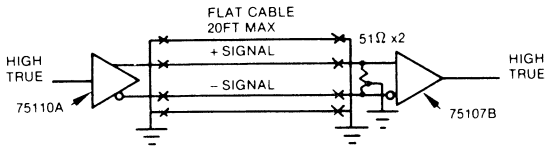


Figure 10. Data Transfer Line Driver/Receiver

5.3.1 MFM Write Data

This is a differential pair that defines the transitions to be written on the track. The transition of + MFM WRITE DATA line more positive then the − MFM WRITE DATA line will cause a flux reversal on the track provided − WRITE GATE is active. This signal pair must be driven to an inactive state (+ MFM WRITE DATA more negative than − MFM WRITE DATA) by the controller when in a read mode. Figure 11 shows the timing for MFM WRITE DATA as required at the interface. The actual occurrence of the flux reversals may differ due to write precompensation.

5.3.2 MFM Read Data

The data recovered by reading a prerecorded track is transmitted to the host system via the differential pair of MFM READ DATA lines. The transition of the + MFM READ DATA line more positive than the − MFM DATA line indicates a flux reversal was detected on the track provided the − WRITE GATE is inactive. Figure 12 shows the timing for MFM READ DATA as required at the interface.

5.4 Select Status

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED line is driven by a TTL open collector driver as shown in Figure 6. This signal will go active only when the drive is selected as drive "X" ("X" = 1,2,3 or 4) by proper placement of the shorting plug at the vicinity of J1, and the corresponding − DRIVE SELECT "X" line at J1/P1 is activated by the host system.

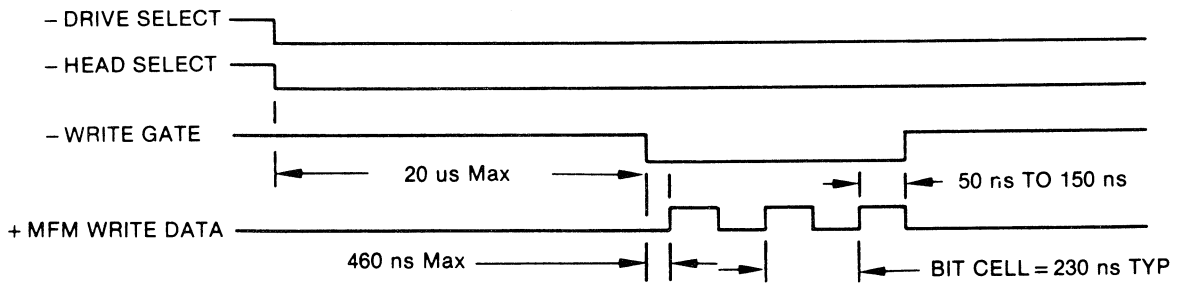


Figure 11. MFM Write Data Timing

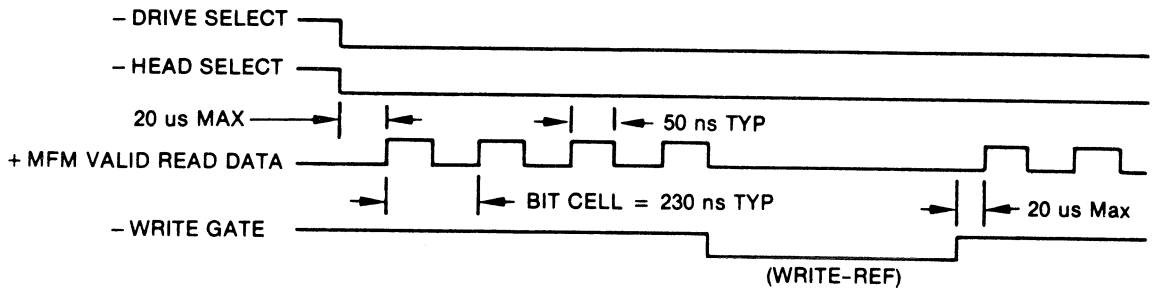


Figure 12. MFM Read Data Timing

6.0 General Timing Requirements

The timing diagram as shown in Figure 13 shows the necessary sequence of events (with associated timing restrictions) for proper operation of the drive.

Note that a recalibrate to track zero sequence is initiated automatically at every DC power on. For this auto-recal sequence to function, the Spindle must be spinning at normal speed (if AC and DC are switched on at the same time, seeking action will not occur until spindle is up to speed).

No AC or DC power sequencing is required.

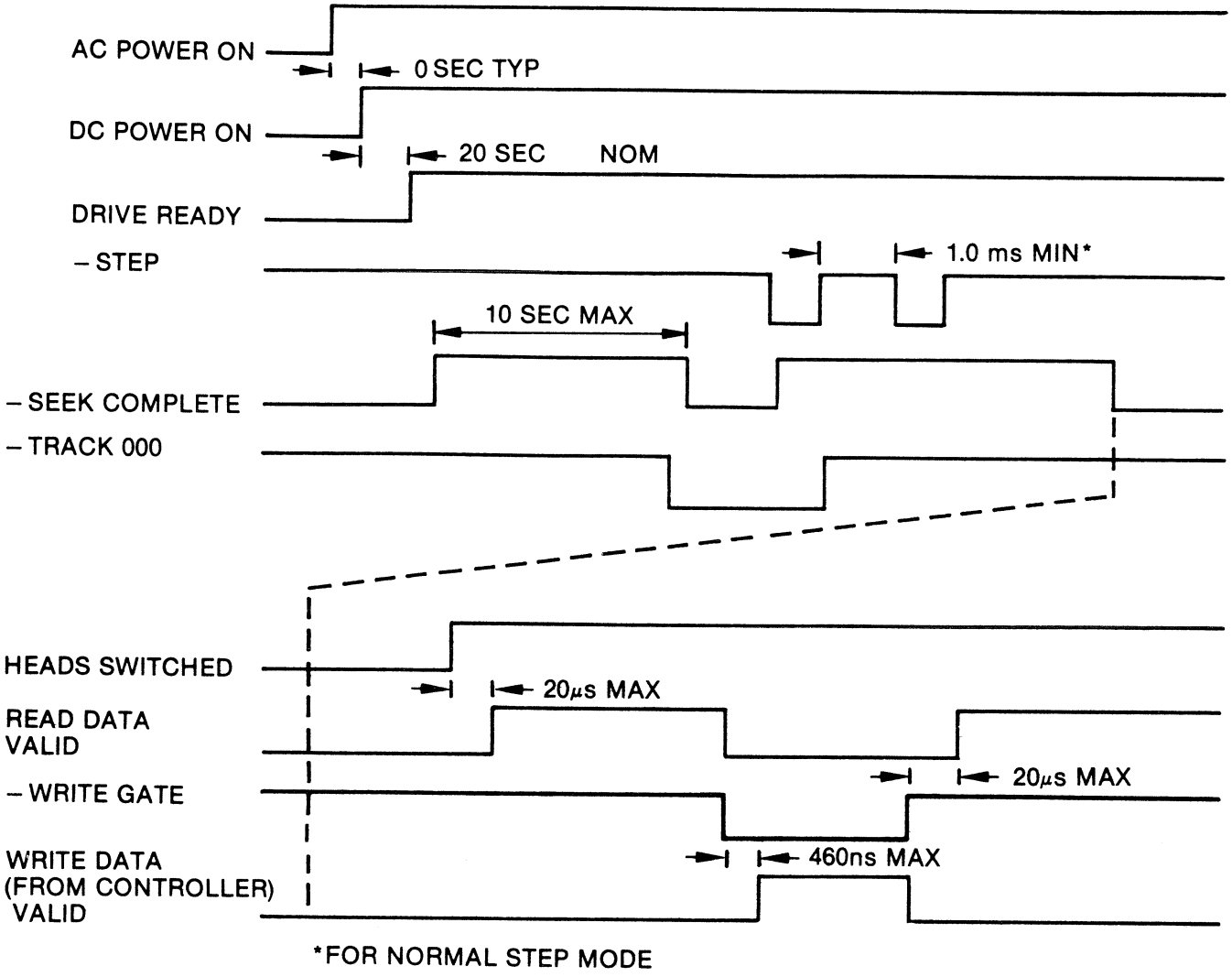


Figure 13. General Control Timing Reqirements

7.0 Power Interface

The drive requires both AC and DC power for operation. The AC power is used for the drive motor and the DC is used for the electronics and actuator.

7.1 AC Power

AC power to the drive is via J4/P4. The voltage, frequency and current requirements are given in Table VII.

	60HZ		50HZ	
CONNECTOR P4	110V (Standard)	208/230V	100V	220V
1 2 3	90-127V FRAME GND 90-127 RTN	180-253V FRAME GND 180-253V	90-127V FRAME GND 90-127 RTN	180-253V FRAME GND 180-253V
MAX INRUSH CURRENT (Duration*)	4.0 Amps	2.0 Amps	TBS	TBS
MAX RUN CURRENT	1.0 Amps	0.5 Amps	TBS	TBS
FREQ TOL	± 0.5 HZ		± 1.0HZ	

Table VII. AC Power Requirements

*1 sec. for Q2010
2 sec. for Q2020
3 sec. for Q2030
4 sec. for Q2040
@ 117V AC

7.2 DC Power

DC power to the drive is via P5/J5. The three required voltages and curent requirements are given in Table VIII.

DC VOLTAGE	CURRENT	
	STEADY OR SEEKING	
	MAX.	TYP.
+24 ± 2.4V 1V P-P MAX RIPPLE	1.5A	1.25A
+5 ± 0.25V 50mV P-P MAX RIPPLE	1.5A	1.0A
17 ± to −16V (−5 ± 0.25V OPT) 50mV P-P MAX RIPPLE	.25A	.20A

Table VIII. DC Power Requirements

8.0 Physical Outline

The mechanical outline of the Q2000 is given in Figure 14.
WARNING: Exercise caution when selecting mounting screws. The screws must be short enough to not contact the bubble when installed and tightened. Failure to observe this warning may result in damage to the bubble

9.0 Physical Interface

Electrical interface between the Q2000 and the host system is through four connectors: the first connector (J1) provides control signals for the drive; the second connector (J2) provides radial connection of read/write

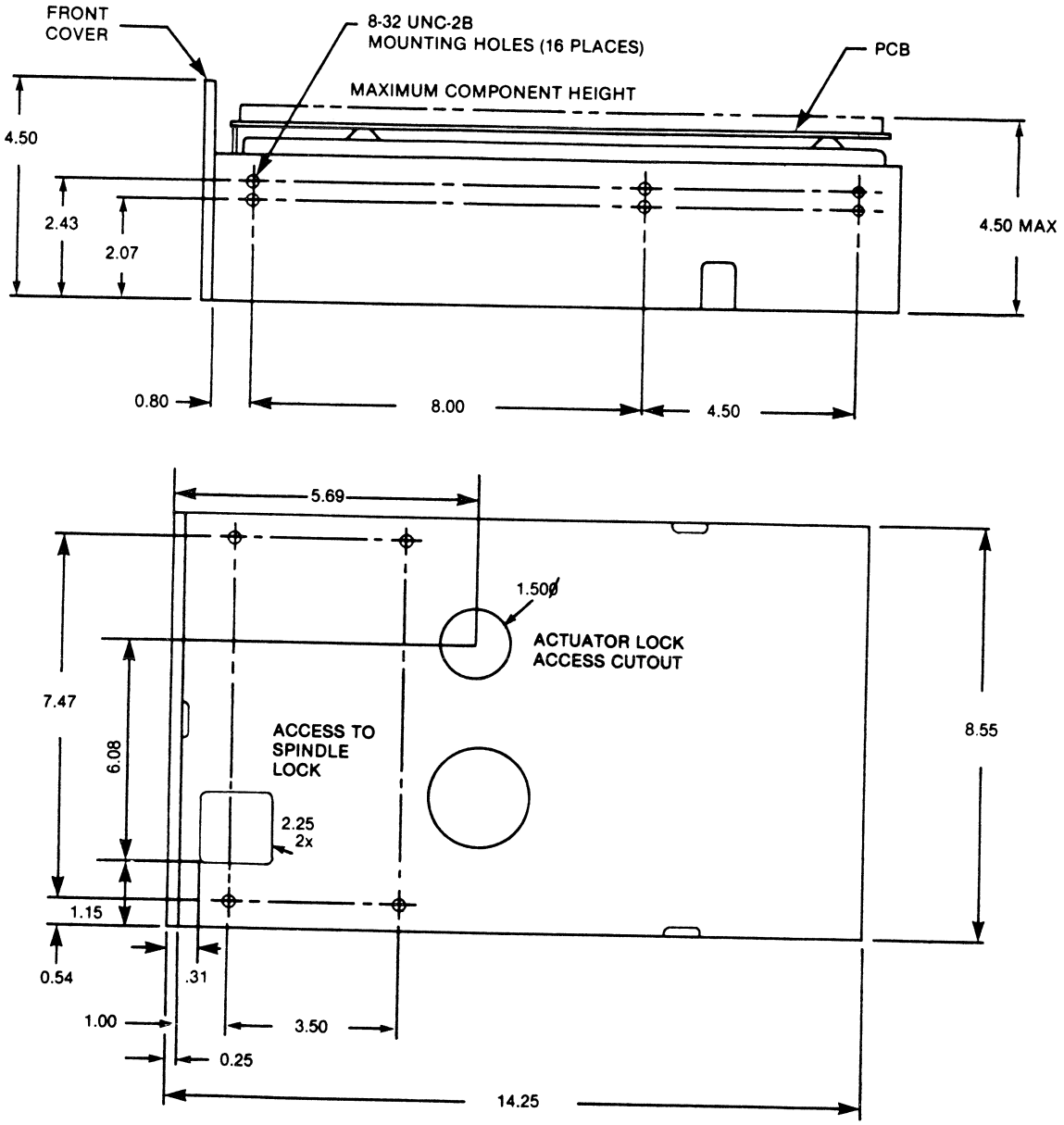
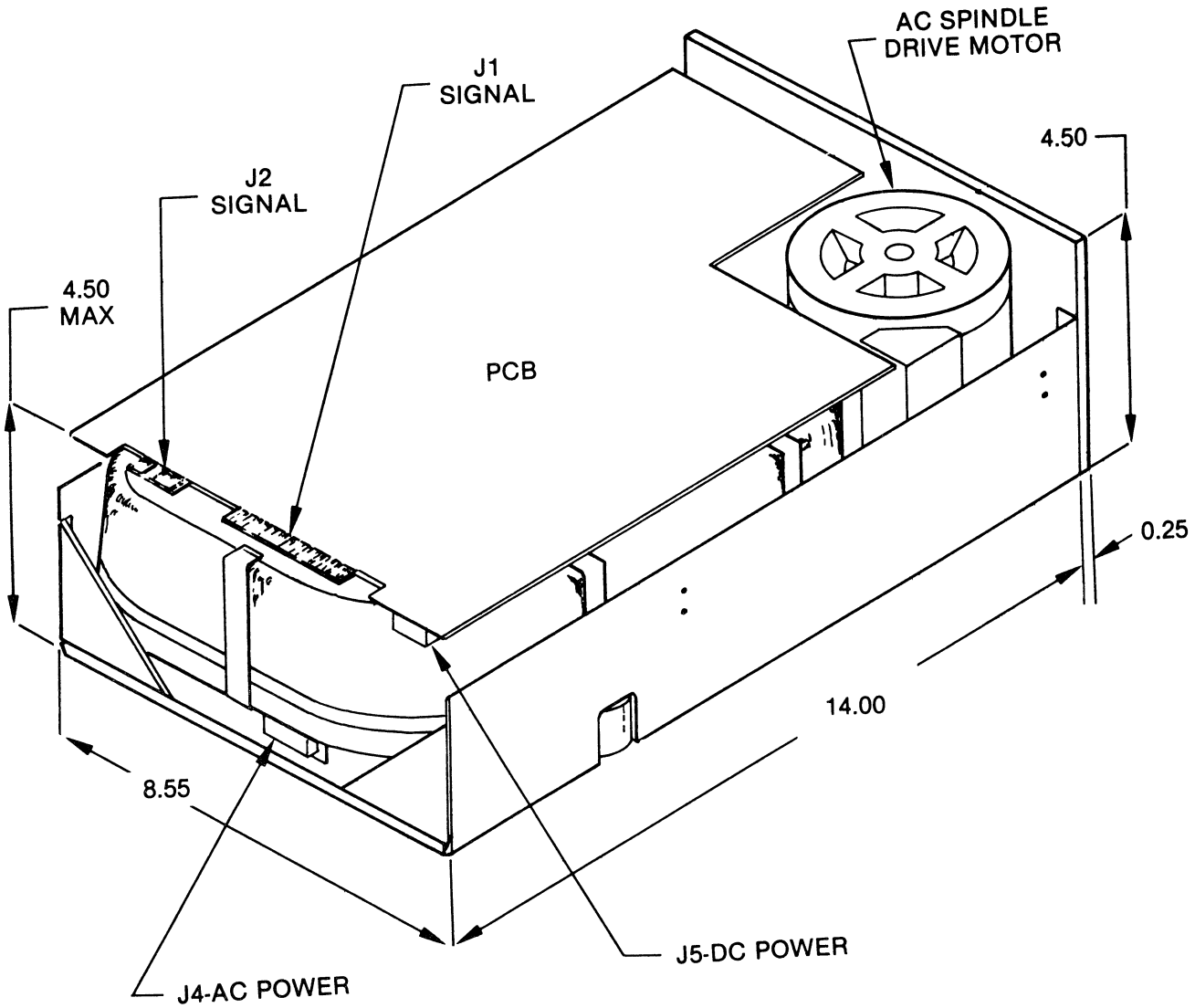


Figure 14. Q2000 Mounting Dimensions

data signals; the third connector (J5) provides for DC power; and the fourth connector (J4) provides for AC power and frame ground. Refer to Figure 15 for connector locations.



All dimensions in inches

Figure 15. Mechanical Dimensions and Connector Locations

9.1 J1/P1 Connector

Connection to J1 is through a 50 pin PCB edge connector. Connector dimensions are shown in Figure 16. The pins are numbered 1 through 50 with the even pins located on the component side of the PCB and odd pins located on the noncomponent side of the PCB. Pin 2 is located on the end of the PCB connector closest to the J2 connector and is labeled. A KEY SLOT is provided between pins 4 and 6. The recommended mating connector for P1 is Scotchflex ribbon connector P/N 3415-0001.

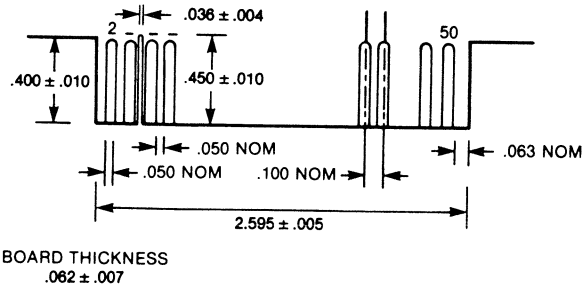


Figure 16. J1 Connector Dimensions

9.2 J2/P2 Connector

Connection to J2 is through a 20 pin PCB edge connector. Connector dimensions are shown in Figure 17. The pins are numbered 1 through 20 with the even pins located on the component side of the PCB. The recommended mating connector for P2 is Scotchflex ribbon connector P/N 3461-0001. A key slot is provided between pins 4 and 6.

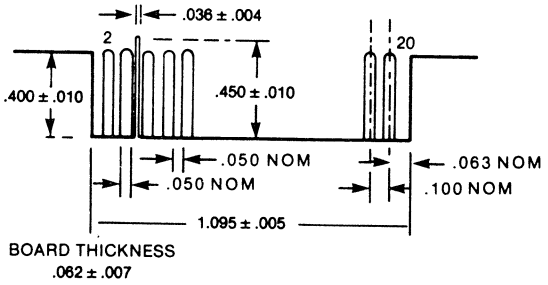


Figure 17. J2 Connector Dimensions

9.3 J5/P5 Connector

DC power connector (J5) is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0 mounted on the solder side of the PCB. The recommended mating connector (P5) is AMP P/N 1-480270 utilizing AMP pins P/N 60619-1. J5 pins are labeled on J5 connector.

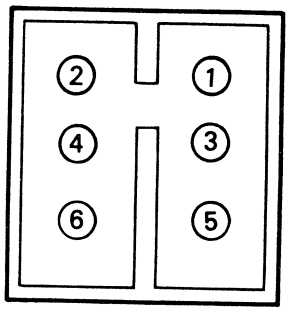


Figure 18. J5 Connector

9.4 J4/P4 Connector

AC power and frame ground are applied through a 3 pin connector. The pin housing (J4) is mounted in the drive and is AMP P/N 1-480701-0 with pins AMP P/N 350687-1 and 350654-1 (gnd pin). The recommended mating connector (P4) is AMP socket P/N 1-480700-0 with AMP pins P/N 350536-1.

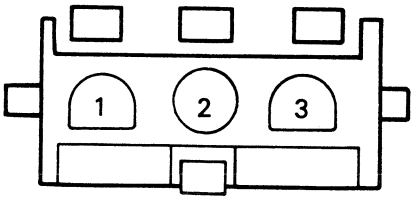


Figure 19. J4 Connector

The disk drive is shipped with DC ground (base casting) and AC ground (drive motor) connected together with a ground strap located on the drive motor and grounding clips. AC and DC grounds may be separated by removing a ground wire attached to the AC motor and the casting.

10.0 Q2000 Recommended Track Format (in Figure 20)

The purpose of a track format is to organize a data track into smaller, sequentially numbered blocks of data called sectors. The Q2000 disk drive is intended to have a soft sectored format. Soft sectored means that the beginning of each sector is identified by a prewritten identification (ID) field. (Hard sectored disks use some type of mechanically fixed method of identifying sector beginnings.) The ID field of a soft sectored drive contains the physical sector address plus cylinder and head information The I.D. field is then followed by a user data field.

The format shown in figure 20 is for illustration only as the Q2000 drive does not dictate the format to be used. The soft sectored format shown is a slightly modified version of the I.B.M. System 34 double density format, which is commonly used on 8 inch floppy disk drives. The encoding method used here is modified frequency modulation (MFM).

In the example shown (Figure 20), each track is divided into 32 sectors. Each sector has a data field of 256 bytes in length.

The beginnings of both the I.D field and the data field are flagged by unique characters called address marks.

An address mark is 2 bytes in length. The first byte is always an "A1" data pattern This is followed by either an "FE" pattern which is the pattern used to define an I D address mark, or an "FB" which is a data address mark pattern.

The "A1" pattern is made unique by violating the encoded rules of MFM by omitting one clock bit. This makes the address mark pattern unique to any other serial bit combination

Each I.D. and data field is followed by 16 bits of cyclic redundancy check (CRC) or 24 or 32 bits of Error Correction Code (ECC) used for data verification and correction Each CRC or ECC polynominal is unique for a particular data pattern.

Surrounding the I.D. and data field are gaps called interrecord gaps.

10.1 GAP LENGTH CALCULATIONS

10.1.1 Gap 1

Gap 1's purpose is to provide a head switching recovery period so that by switching heads from one surface to another, sequential sectors may be read without waiting for the rotational latency time. Gap 1 should be at least 11 bytes long which corresponds to the head switching time of 20 microseconds. Gap 1 is immediately followed by a sync field for the I.D. field of the first sector.

10.1.2 Gap 2

Following the I.D. field, and separating the I.D. field from the data field is gap 2. Gap 2 provides a known area for the data field write update splice to occur. The remainder of this gap also serves as the sync up area for the data field address mark. The length of gap 2 is determined by the data separator lock up performance.

10.1.3 Gap 3

Gap 3, following the data field, is a speed variation tolerance area. This allows for a situation where a track has been formatted while the disk is running 3% slower than nominal, then write updated with the disk running 3% faster than nominal (power line variations). Gap 3 should be at least 15 bytes in length.

10.1.4 Gap 4

Gap 4 is a speed tolerance buffer for the entire track. This allows the disk to rotate at least 3% faster than normal without overflowing the track during the format operation. The format operation, starts with the first encountered index and continues writing a fixed number of ID fields. These fields must be written prior to the next index.

10.2 Write Precompensation

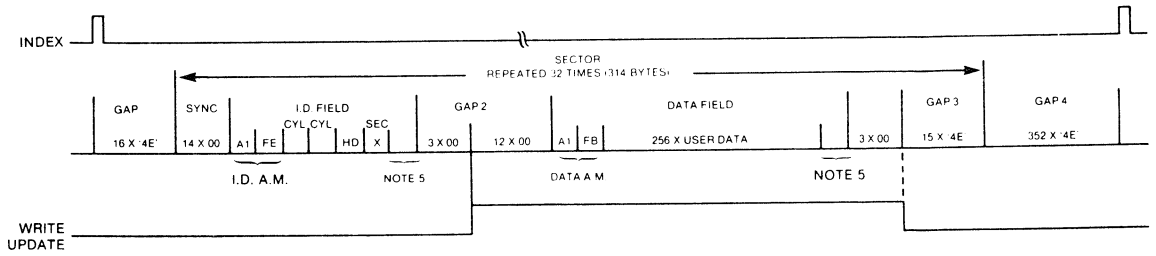
Whenever two bits are written in close proximity to each other, a phenomenon called pulse superposition occurs, which tends to cause the two bits to move away from each other. This is a large factor of bit shift.

Other phenomenon such as random noise, speed variation, etc., will also cause bit shift, but to a lesser degree.

The effect of bit shift can be reduced by a technique called write precompensation. This technique requires detecting those cases where bits will be written in close proximity to each other and alters the write timing of these bits. The bits are then written earlier or later than normal to compensate for the expected shift.

Since bit crowding is greatest on the innermost tracks, the effects of pulse superposition cause the greatest shift on these tracks. Therefore, write precompensation should only be used when writing on track numbers greater than 255.

The optimum amount of pre-compensation for the Q2000 is 12 nanoseconds for both early and late written bits.



NOTES:
1. NOMINAL TRACK CAPACITY - 10416 BYTES.
2. MINIMUM TRACK CAPACITY - (NOMINAL - 3% SPEED VARIANCE) 10102 BYTES.
3. WRITE TO READ RECOVERY TIME = 20 MICROSECONDS.
4. HEAD SWITCHING TIME = 20 MICROSECONDS.
5. CHECK BYTES MAY BE 2 BYTES OF CRC OR 3 OR 4 BYTES OF ECC.

Figure 20. Track Format

Table IX shows data bit patterns, the expected bit shift direction, the write precompensate direction and the type of pulse to write for MFM recording.

DATA PATTERN				EXPECTED SHIFT DIRECTION OF PULSE FOR CELL 2*	PRECOMPENSATE DIRECTION AND PULSE FOR CELL 2*	
4	3	2	1			
0	0	0	0	NONE	ON TIME	CLOCK
0	0	0	1	LATE	EARLY	CLOCK
0	0	1	0	NONE	ON TIME	DATA
0	0	1	1	EARLY	LATE	DATA
0	1	0	0	NONE	NO CLOCK OR DATA WRITTEN	
0	1	0	1	NONE	NO CLOCK OR DATA WRITTEN	
0	1	1	0	LATE	EARLY	DATA
0	1	1	1	NONE	ON TIME	DATA
1	0	0	0	EARLY	LATE	CLOCK
1	0	0	1	NONE	ON TIME	CLOCK
1	0	1	0	NONE	ON TIME	DATA
1	0	1	1	EARLY	LATE	DATA
1	1	0	0	NONE	NO CLOCK OR DATA WRITTEN	
1	1	0	1	NONE	NO CLOCK OR DATA WRITTEN	
1	1	1	0	LATE	EARLY	DATA
1	1	1	1	NONE	ON TIME	DATA

Table IX

The write data bits are shifted through a 4 bit shift register to detect those patterns that require precompensation and to determine what type of pulse to write. Data or clock pulses are written on the disk according to the rules for MFM recording, and are written on time, early or late in the cell period according to the direction of expected shift. Timing is such that the cell period for a pulse starts when the data bit is shifted into position three and ends when the bit is shifted into position four.

*Determination of pulse and precompensation is made in cell 2, however pulse is written from cell 3.

11.0 INSTALLATION INSTRUCTION

11.1 Required Tools:

1. Common Screwdriver
2. 11/32 inch socket or hex nut driver

11.2 Unpacking Instruction:

a) Carefully remove drive from shipping container, inspect for damage. **Do Not Drop!**

b) Do not set drive down on its printed circuit board.

11.3 Motor Locking Clip Disengagement

a) Stand drive on edge to unlock drive motor. (See Figure 21.)

b) Loosen 11/32 inch hex nut.

c) Rotate locking clip away from pulley. Do not rotate pulley.

d) Retighten 11/32 inch hex nut.

Figure 21.

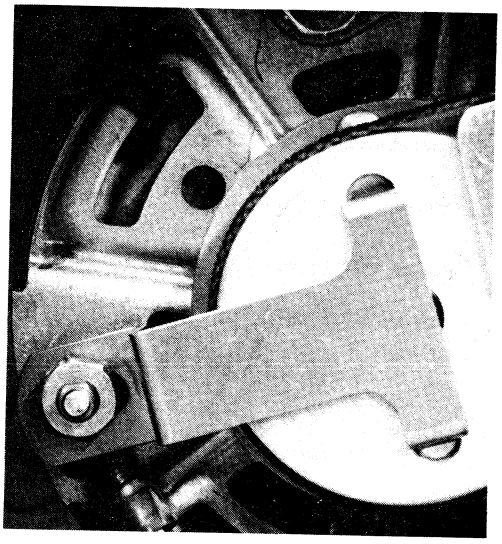
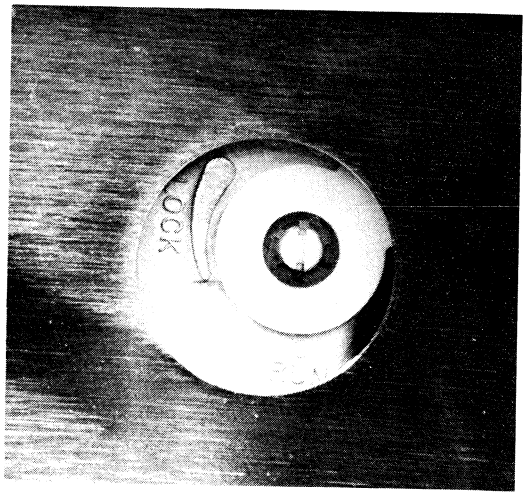


Figure 22.



11.4 Actuator Lock

Unlock actuator by rotating the actuator lock CCW as far as it will go (approx. ½ turn) **Do Not Force.** The actuator lock is located on the bottom of the drive. (See Figure 22.)

11.5 Drive Options

11.5.1 Jumper Options (Fig. 23)

Designator	Description
−5/−15	The drive requires −5V DC (−5V position) but will regulate higher negative voltages from −7 to −16 (−15 position). Drive is normally shipped with the jumper in the −15 position.
DS1,2,3,4	Four drive select jumpers allow logical drive assignment.
A	Causes drive to be selected constantly.
C	When jumpered, allows J1 pin 6 REZERO to be used to cause the drive to recalibrate Use of this option is recommended since it is faster than standard recalibration sequences and the drive goes through an internal recalibration.
E3	When jumpered, disables the fine servo for maintenance purposes.
E4	When jumpered, causes the microprocessor to perform a seek diagnostic routine.

11.5.2 Cut Trace Options

Designator	Description
B	The third head select line (− head select 2^2) is attached to pin 4 of J1. If it is desired to use a pin on J1 other than 4, this trace may be cut and a wire added from "B" to the desired pin.
T1-T5	These options are not for customer use. They are used for factory test only.

11.6 Control Line Termination

If drive is the last drive at the end of the control signal cable, a 220/320 terminator pack must be installed at PCB location 6J. The terminator pack must be removed from location 6J if this drive is not at the end of a string of drives. The Quantum P/N for the terminator pack is 13-12302.

12.0 Shipping Instructions

In the event that the Q2000 drive needs to be repacked for shipment, use the following procedure:

12.1 Actuator Lock

Lock the actuator by rotating the actuator lock CW as far as it will go (approx. ¼ turn). ***Do not force!*** (See Figure 22).

12.2 Motor Locking Clip Engagement

Enagage drive motor locking clip (See Figure 21).

a) Loosen 11/32 inch hex nut.

b) Rotate locking clip until engaged in pulley.

c) Tighten 11/32 inch hex nut.

12.3 Packaging

Carefully place the drive in a padded shipping container and enclose a copy of the packing/unpacking instructions, Quantum P/N 81-40162.

Secure container and ship.

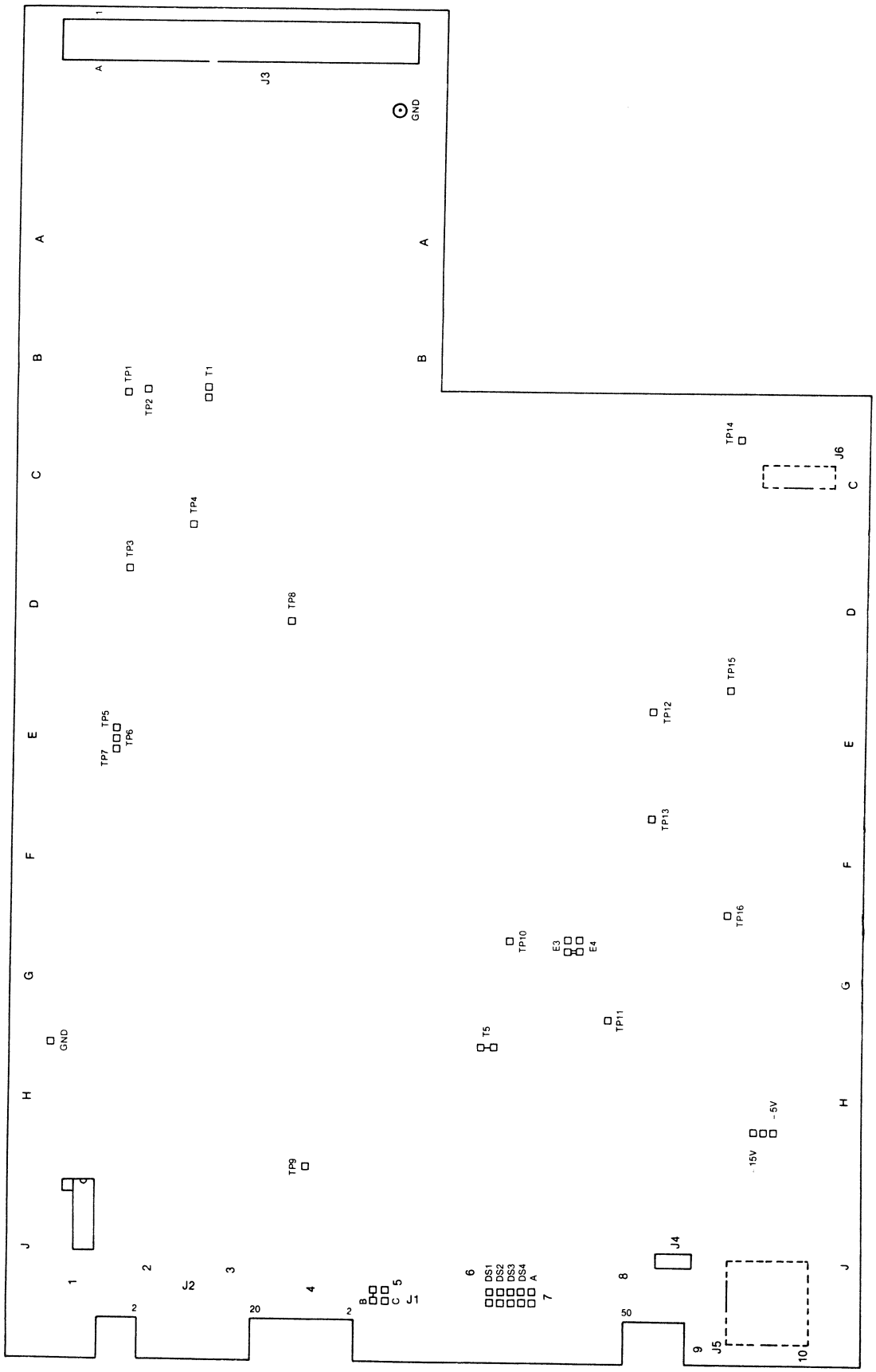


Figure 23. PCB Jumper Locations

APPENDIX A

Definition of Terms

A. Read/write head

The read/write head is a ferrite magnetic transducer element which writes data to or reads data from the magnetic media. The read/write heads for use on "Winchester" technology drives are aerodynamically constructed such that they fly over the surface of the media at a height of 20 microinches. The heads are in contact with the media when the media is not rotating. See Figure 24.

B. Media

The media is a magnetic oxide coated on an aluminum substrate (platter) which is very flat and in the shape of a disk. The media is lubricated to aid in the take off and landing of the heads without damage to either the media or heads. The media is also oriented to give maximum signal output.

C. Surface

A media surface is one side of a disk in the drive. Surface 0 is the area of a disk where read/write head 0 writes and reads data. See Figure 24.

D. Track

A track is a ring of constant radius on the surface of a disk where data is stored. A track is .0023 inches wide and the track spacing is.00285 center to center. Tracks are numbered 000 to 511 on the Quantum drive with track 511 being the innermost. See Figures 24 and 25.

E. Cylinder

A cylinder is a set of tracks on multiple recording surfaces at a given actuator position or location. See Figure 24. The Quantum 2000 series drive has 512 cylinders.

F. Actuator

An actuator positions the read/write heads over the desired track or cylinder The actuator consists of a rotary torque motor and the actuator arms. The actuator arms are attached to the motor. The read/write heads are attached to the other end of the actuator arm. As the motor rotates, the heads are moved over the surface of the disks and can access any track.

G. Shipping and landing zone

The shipping and landing zone is a circular area inside of track 511. The heads are positioned over this area at power off or any time that the disks are not spinning at a minimum of 90% of the nominal speed of 3000 RPM. This area is a designated landing zone for the heads such that the heads do not contact the surface in usable data areas. This adds to the data reliability and integrity on the Quantum drives. See Figure 25.

H. Winchester Technology

The term "Winchester Technology" when used in reference to rigid disk drives means many things. Rigid disk drives utilizing Winchester Technology use continuously loaded, low mass high compliant head assemblies. These heads fly over the surface of the platter at a height of 20 microinches during normal operation but rest on the surface of the media when the platter is not spinning. The media used on the platters is lubricated such that there is no damage to head or media when the two come into contact.

The environment in which the heads and platters reside is sealed and contamination free to allow the 20 microinch head flying height.

I. Disk/Platter

A disk or platter is a very flat circular substate upon which magnetic oxide is deposited or coated. Each disk/platter has two surfaces for recording information.

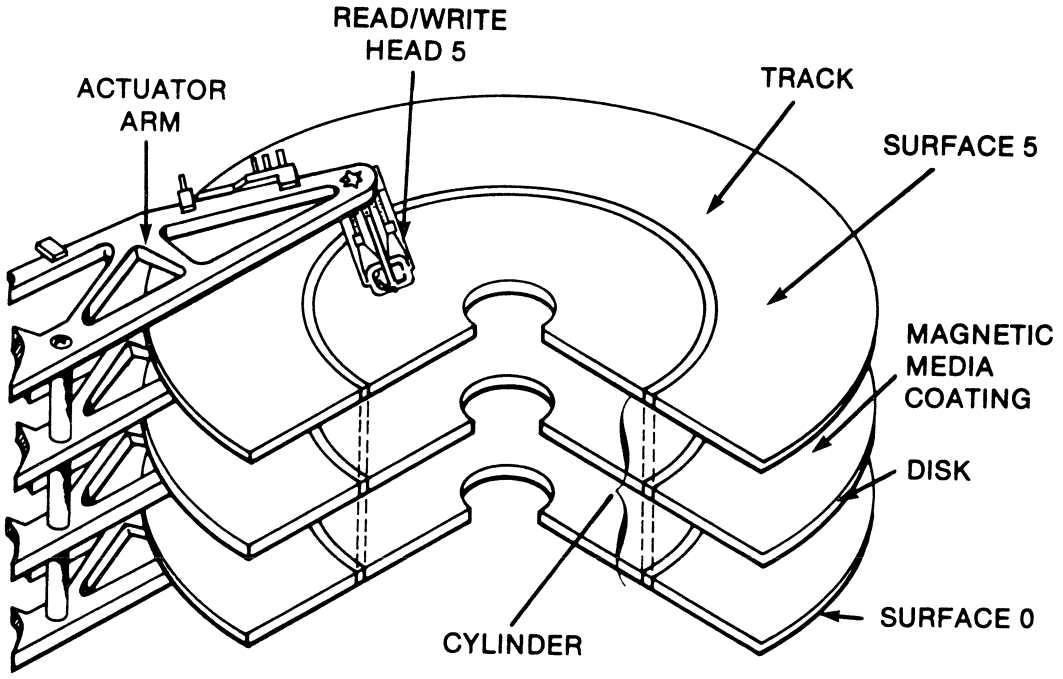


Figure 24. Typical Quantum Disk Drive Organization and Terminology

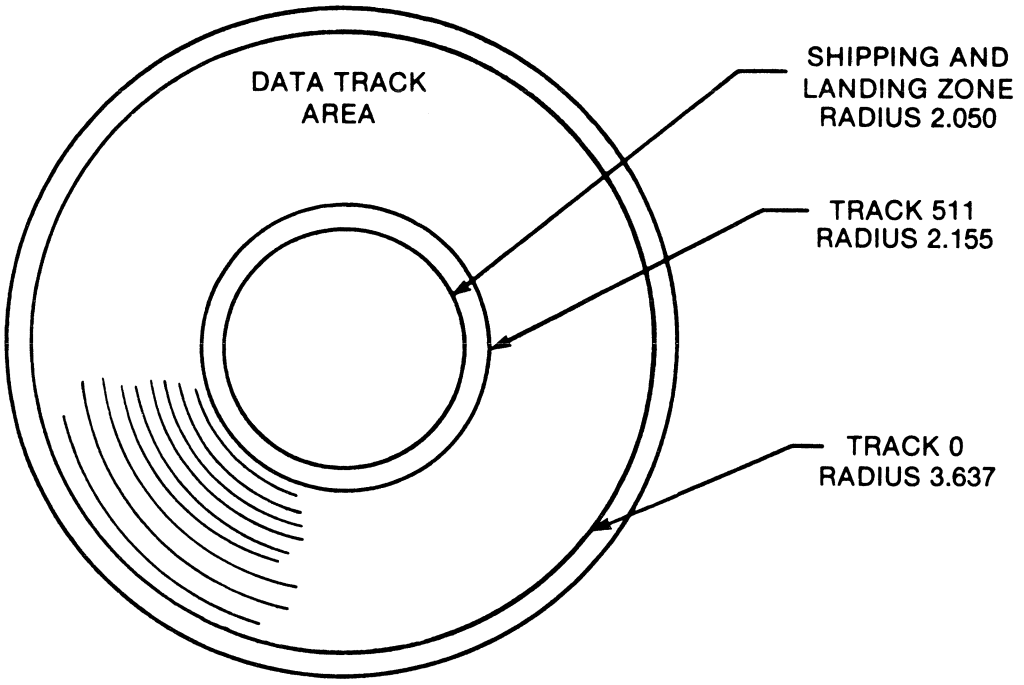


Figure 25. Data Area and Landing Zone

APPENDIX B

MEDIA DEFECTS & ERRORS

Introduction

In a high density digital recording storage system it is necessary to increase the reliability and improve the operational performance by providing an error detection and correction scheme. For disk storage systems, the predominant error pattern is a burst of errors ocurring in one or more tracks. These errors are normally absent bits (dropouts) or additional bits. Errors may occur when bits are shifted further from nominal than can be tolerated by the data separator.
These errors are due to defects in the media as well as a low signal to noise ratio that contributes to probability of error occurrence. The error rate is dependent upon the noise and phase characteristics of the media, Read/Write circuits, and heads and the accuracy of actuator positioning.

What Is The Definition Of An Error?

An error is any discrepancy between recovered data and true, correctly recorded data. There can be an extra bit or a missing bit, i.e., a "zero" can be transformed into "one" or a "one" can be changed to zero. Errors can be classified into soft or hard errors. Soft errors are generally related to the signal to noise ratio of the system and represent marginal conditions of the head, media, and Read/Write circuits.

If an error is repeatable with a high probability, it is due most often to a media defect and is termed a hard error.

How will Quantum Find the Errors?

The errors will be identified prior to shipment and information incorporated in a usable format to enable the user to skip those defective locations per his system capability. Quantum has a unique media test system which exercises the drive in extreme marginal conditions and measures the amplitude and phase distortion of each bit recorded on the disk storage. All drives shipped will be accompanied by an error map reporting any media defects.

Error Reporting

An error map will be provided with each drive showing defective areas. The areas will be identified by cylinder and head address, number of bytes from index, and number of bits in length. Additionally, cylinder 000 is guaranteed to be error free.

Error Acceptance Criteria

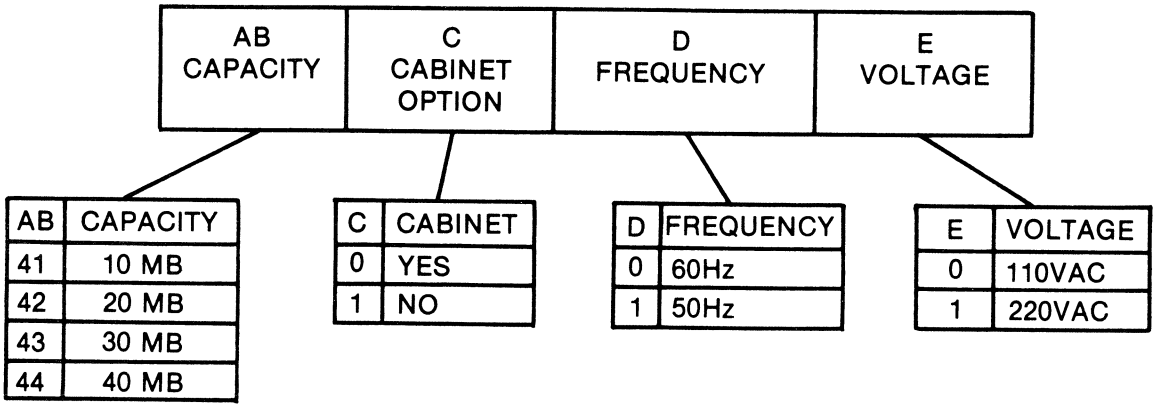
There will be no more than 12 tracks with defects per surface of which no more than 4 tracks will contain multiple defects.

A single defect is defined as an error less than 2 bytes long. A multiple defect is a defined as an error greater than 2 bytes long, or a single error in several sectors.

APPENDIX C

Ordering Information

1. Table X provides the information necessary to construct a unique part number for a Q2000 rigid disk drive.



AB	CAPACITY
41	10 MB
42	20 MB
43	30 MB
44	40 MB

C	CABINET
0	YES
1	NO

D	FREQUENCY
0	60Hz
1	50Hz

E	VOLTAGE
0	110VAC
1	220VAC

Example: 42010 = 20MB, Cabinet, 50 Hz, 110VAC

Table X. Product Selection Index

2. Accessories

   a) Signal Cable Connector Kit P/N 73-40157
   b) DC Power Connector Kit P/N 73-40158
   c) AC Power Connector Kit P/N 73-40159

3. AC voltage or Frequency Conversion. If it is required to change AC power voltage and or frequency, the following table indicates the necessary components.

POWER	PART NUMBERS		
VOLTAGE AND FREQUENCY	MOTOR ASM	PULLEY	BELT
110VAC 60 Hz	74-40109	40-40015	50-40000
110VAC 50 Hz	74-40109	40-40032	50-40001
220VAC 60 Hz	74-40111	40-40015	50-40000
220VAC 50 Hz	74-40111	40-40032	50-40001

Table XI. Voltage and Frequency Conversion Information

GLOSSARY

8X300 Microcontroller. The Signetics 8X300 microcontroller controls all of the floppy disk, Winchester disk, and Storage Module Drive functions on the SMD Controller board. The 8X300 operates from a microprogram stored in four on-board ROMs and communicates with its peripheral devices through the IV bus. Instructions from the CPU board are sent through an 8X320 bus interface register array. See the 8X300 Design Guide, published by the Signetics Corporation.

8X320 Bus Interface Register Array. The Signetics 8X320 bus interface register array contains sixteen 16-bit registers for interfacing the 8X300 microcontroller to the HDC board bus interface. See the 8X300 Design Guide, published by the Signetics Corporation.

8X330 Floppy Disk Controller. The Signetics 8X330 floppy disk controller contains all of the circuitry necessary to control the floppy disk drive and most of the circuitry necessary to control the Winchester disk drive on the IWS workstation. The 8X330 is controlled by the 8X300 microcontroller. See the 8X300 Design Guide, published by the Signetics Corporation.

Actual Sector. Actual sector refers to the physical sector number at which the head is currently located.

Bit Numbering. Bits in an 8-bit byte, 16-bit word, or 20-bit address are numbered from right to left, beginning with zero as the least significant bit and counting in hexadecimal. Thus, bits in a byte are numbered 0h to 7h, bits in a word are numbered from 0h to Fh (bits 8h and Fh are the most significant bits), and bits in a 20-bit address are numbered from 0h to 13h. Also see High Order Byte and Low Order Byte.

Board. One of several types of boards manufactured by Convergent Technologies. This set of boards includes: the Processor board, the I/O Memory board, the Video Control board, the SMD Controller board, the Write-Protect board, and the I/O Extender boards (SMD and MSX). None of these boards has the Multibus form factor.

Buffer. A buffer is an amplifying signal driver, not necessarily with memory capability. Buffers that provide temporary storage for data are called "storage buffers."

Bus. A bus is a collection of signal lines used by more than one device.

Byte. A byte is 8 bits. Also see High Byte and Low Byte.

Clear. A register is cleared when a logical 0 or series of 0s is written to that register. Also see Reset and Set.

Cluster Communications Logic. The cluster communications logic in the host workstation allows the IWS workstation to communicate with a master workstation on an RS-422, half-duplex communications channel at a transmission rate of 307 kbaud. Instructions for installing the cluster communications cable are contained in Section 4, "Additional IWS Peripherals Hardware."

Cluster Configuration. A cluster is a hardware configuration in which cluster workstations are linked in a daisy chain to a master workstation.

Disk Controller Interface (DCI). The DCI is the cable used to link the MSS with the IWS workstation (host). It contains all of the data, control, and status signals necessary to operate all of the peripherals described in this manual.

DIR. DIR is used to indicate the direction that a disk is stepped (to the outside or the center).

Direct Memory Access Logic. See DMA.

DMA (Direct Memory Access). DMA allows the host to transfer data to or from the SMD Controller board without using the 8X300 microcontroller.

DMA Address. When the DMA channel is initialized for a transfer, the DMA address is the initial address in memory of the transfer. If the DMA address is read for status at any time, it is the current memory address of the transfer.

DMA Count. When the DMA channel is initialized for a transfer, the DMA count is the number of bytes to be transferred in the operation. If the

DMA count is read for status at any time, it is the number of bytes remaining to be transferred.

Driver. See Buffer.

Filler Byte. Filler byte refers to the bit pattern for each byte, which is written to an empty disk sector.

First Sector. First sector refers to the first sector number to be read or written during an operation.

High-Order Byte. The high-order byte is the most significant byte in a word (bits 8h to Fh). The high-order byte is also called the odd byte, since it always has an odd address in memory.

Host. Host is generally used to refer to the CPU board in the IWS workstation, or just the IWS workstation.

Instruction Vector Bus (IV Bus). The IV bus is the bus for the 8X300 microcontroller on the SMD Controller board. The 8X300 uses the IV bus to transfer data from and to peripheral devices, such as the 8X320 bus interface register array, the 8X330 floppy disk controller, and the Main Status register.

Low-Order Byte. The low-order byte is the least significant byte in a word (bits 0h to 7h). The low-order byte is also called the even byte, since it always has an even address in memory.

Master Workstation. A master workstation is used in a cluster configuration to control access to shared resources.

MFM (Modified Frequency Modulation). MFM is a data-encoding scheme used on the SMD Controller board to store double-density data on a floppy disk. The basic rules for MFM encoding are as follows: Write data bits to the center of a bit cell. Write clock bits to the beginning of a bit cell if there is no data bit written in the previous bit cell, and there will be no data bit written in the current cell. See 8X330 Floppy Disk Controller, published by the Signetics Corporation.

Nonmaskable Interrupt. A nonmaskable interrupt is caused by a parity error. When it occurs, the

CPU branches to the address contained in locations 8h, 9h, Ah, and Bh, which is the address of a recovery software routine.

Number of Sectors. The number of sectors designation refers to the number of sectors, in twos complement, to be read or written. In the Format a Track command, this designation refers to the number of physical spaces between logical sectors.

Parity Bit. A parity bit is stored along with every data byte in memory as a ninth bit. The IWS controller ECC uses an even parity error checking system. When a byte with an odd number of 1 bits is stored in a memory location, a 1 is stored as the parity bit. Accordingly, when a byte is stored with an even number of 1 bits, a 0 is stored as the parity bit.

Parity Error Register. The parity error register latches the address at which a RAM parity error occurred and indicates whether DMA was active at the time of the error.

Peripheral Device. Peripheral device refers, for the most part, to the MSS and MSX memory expansion peripherals. In a wider sense, peripheral device refers to any electromechanical devices (i.e., a printer, a plotter, or an additional drive) that can be connected to the IWS workstation.

Physical Drive Select. Physical drive select refers to the actual number of drives that are attached to the MSS.

Port. A port is an input/output address, such as port 78h, that allows access to several registers at one time. Also see Register.

RAM (Random Access Memory). Four 1K-byte dynamic RAM chips comprise the two buffers used during SMD Controller board operation.

Register. A register is a temporary memory location for data.

ROM (Read Only Memory). ROM refers to a ROM, PROM (Programmable ROM), or EPROM chip. Four bootstrap PROMs are used on the SMD Controller board: two 4K-byte 2732 EPROMs and two 2K-byte 82S191 ROMs.

Seek Interrupt. Seek interrupt refers to the drive number associated with a seek interrupt.

Set. To set is to write a logical 1 or series of 1s to a register. Also see Clear.

Storage Module Drives (SMDs). Up to four SMDs can be connected to the IWS workstation, via the SMD I/O Extender board located in the MSS. SMDs, which are not manufactured by Convergent Technologies, can be configured to have either an 80M- or a 300M-byte memory capacity.

Storage Buffer. A storage buffer is a buffer with storage, such as a flip-flop, latch, or register.

Wait State. A wait state is a temporary suspension of an input/output or memory cycle. It is used when an input/output or memory device operates at a speed slower than that of the host CPU.

Winchester. Winchester refers to an 8-inch hard-disk drive, containing multiple heads.

Word. A word, 16 bits, consists of a high byte (most significant byte) and a low byte (least significant byte).

INDEX

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