AWS-220, -230, -240 Hardware Manual

Volume 1

Convergent Technologies

AWS-220, -230, -240 HARDWARE MANUAL

Volume 1

Specifications Subject to Change.

First Edition (April, 1982) A-09-00111-01-A

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GUIDE TO TECHNICAL DOCUMENTATION

This Manual is one of a set that documents the Convergent™ Family of Information Processing Systems. The set can be grouped as follows:

Introductory
- Installation Guide
- Operator's Guide
- Executive Manual

Hardware
- Workstation Hardware Manual
- Peripherals Hardware Manual
- AWS-210 Hardware Manual
- AWS-220, -230, -240 Hardware Manual

Operating System
- CTOS™ Operating System Manual
- System Programmer's Guide
- System Utilities Manual
- Batch Manual

Programming Languages
- COBOL Manual
- FORTRAN Manual
- BASIC Manual
- Pascal Manual
- Assembly Language Manual

Program Development Tools
- Editor Manual
- Debugger Manual
- Linker/Librarian Manual

Data Management Facilities
- ISAM Manual
- Forms Manual
- Sort/Merge Manual

Text Management Facilities
- Word Processing Reference Manual
- Word Processing User's Guide
- Word Processing Quick Reference
- Font Designer Manual
- Multiplan

Communications
- Asynchronous Terminal Emulator Manual
- 3270 Terminal Emulator Manual
- 2780/3780 RJE Terminal Emulator Manual
- X.25 Network Gateway Manual

Multimode Terminal Emulator User's Guide
Multimode Terminal Emulator Reference Manual

This section outlines the contents of these manuals.

Introductory

The Installation Guide describes the procedure for unpacking, cabling, and powering up a system.

The Operator's Guide addresses the needs of the average user for operating instructions. It describes the workstation switches and controls, keyboard function, and floppy disk handling.

The Executive Manual describes the command interpreter, the program that first interacts with the user when the system is turned on. It specifies commands for managing files and invoking other programs such as the Editor and the programming language compilers.

Hardware

The Workstation Hardware Manual describes the mainframe, keyboard, and video display. It specifies system architecture, printed circuit boards (Motherboard, Processor, I/O-Memory, Video Control, ROM Expansion, and RAM Expansion), keyboard, video monitor, Multibus interface, communications interfaces, power supply, and environmental characteristics of the workstation.

The Peripherals Hardware Manual describes the disk subsystems. It specifies the disk controller Motherboard, controller boards for the floppy disk and the Winchester disks, power supplies, disk drives, and environmental characteristics.

The AWS-210 Hardware Manual describes the mainframe, keyboard, and video display of the AWS-210 workstation. It specifies architecture, theory of operation of the printed circuit boards (Motherboard, Deflection, and CPU), keyboard, video monitor, expansion interface, cluster communications interface, power supply, and environmental characteristics of the workstation.

The AWS-220, -230, -240 Hardware Manual describes the mainframe, keyboard, disk controllers, and video display of the AWS-220, -230, and -240 workstations. It specifies architecture, theory of operation of the printed circuit boards (Motherboard, Deflection, 8088 CPU, 8086 CPU, Floppy Disk Controller, and Hard Disk Controller), keyboard, video monitor, cluster communications interface, external interfaces, power supply, and environmental characteristics of the workstation.

Operating System

The CTOS™ Operating System Manual describes the Operating System. It specifies services for managing processes, messages, memory, exchanges, tasks, video, disk, keyboard, printer, timer, communications, and files. In particular, it specifies the standard file access methods: SAM, the Sequential Access Method; RSAM, the Record Sequential Access Method; and DAM, the Direct Access Method.

The System Programmer's Guide addresses the needs of the system programmer or system manager for detailed information on Operating System structure and system operation. It describes (1) cluster architecture and operation, (2) procedures for building a customized Operating System, and (3) diagnostics.

The System Utilities Manual describes utilities such as Backup Volume, IVolume, Restore, Change Volume Name, PLog, Maintain File, Dump, etc.

The Batch Manual describes the batch manager, which executes batch jobs under control of job control language (JCL) files.

Programming Languages

The COBOL, FORTRAN, BASIC, Pascal, and Assembly Language Manuals describe the system's programming languages. Each manual specifies both the language itself and also operating instructions for that language.

The Pascal Manual is supplemented by a popular text, Pascal User Manual and Report.

The Assembly Language Manual is supplemented by a text, the Central Processing Unit, which describes the main processor, the 8086. It specifies the machine architecture, instruction set, and programming at the symbolic instruction level.

Program Development Tools

The Editor Manual describes the text editor.

The Debugger Manual describes the Debugger, which is designed for use at the symbolic instruction level. Together with appropriate interlistings, it can be used for debugging FORTRAN, Pascal, and assembly language programs. (COBOL and BASIC, in contrast, are more conveniently debugged using special facilities described in their respective manuals.)

The Linker/Librarian Manual describes the Linker, which links together separately compiled object files, and the Librarian, which builds and manages libraries of object modules.

Data Management Facilities

The ISAM Manual describes the multikey Indexed Sequential Access Method. It specifies the procedural interfaces and shows how these interfaces are called from the various languages.

The Forms Manual describes the Forms facility that includes (1) the Forms Editor, which is used to interactively design and edit forms, and (2) the Forms run time, which is called from an application program to display forms and accept user input.

The Sort/Merge Manual describes (1) the Sort and Merge utilities that run as a subsystem invoked at the Executive command level, and (2) the Sort/Merge object modules that can be called from an application program.

Text Management Facilities

The Word Processing User's Guide introduces the Word Processor to the first-time user. It provides step-by-step lessons that describe basic

word processing operations. The lessons show how to execute operations and apply them to sample text.

The Word Processing Reference Manual is a reference tool for users already familiar with the Word Processor. It describes the Word Processor keyboard and screen; basic, advanced, and programmer-specific operations; printer and print wheel configurations; and hardware considerations.

The Word Processing Quick Reference provides a concise summary of all word processing operations and briefly describes the keyboard and commands.

The Font Designer Manual describes the interactive utility for designing new fonts (character sets) for the video display.

Multiplan is a financial modeling package designed for business planning, analysis, budgeting, and forecasting.

Communications

The Asynchronous Terminal Emulator Manual describes the asynchronous terminal emulator.

The 3270 Terminal Emulator Manual describes the 3270 emulator package.

The 2780/3780 RJE Terminal Emulator Manual describes the 2780/3780 emulator package.

The X.25 Network Gateway Manual describes the X.25 Network Gateway, which supports CCITT Recommendation X.25 communications over a public data network. There are three levels of access to the network: packet, X.25 Sequential Access Method, and the Multimode Terminal Emulator X.25 communications option.

The Multimode Terminal Emulator User's Guide introduces the Multimode Terminal Emulator to the first-time user. It describes the MTE video display, keyboard, extended functions (Find, Substitute, and Print), and preconfigured functions for the X.25 communications option.

The Multimode Terminal Emulator Reference Manual is a reference tool for sophisticated users of

the Multimode Terminal Emulator. It describes the MTE display memory, communication, escape sequences, field verification program, and programmable functions.

CONVENTIONS AND REFERENCES

CONVENTIONS

Numbers

Numbers are decimal except where suffixed with "h" for hexadecimal. Thus, 10h = 16 and 0FFh = 255.

Signal Names

Signal names use plus (+) and minus (-) suffixes to distinguish active-high from active-low, respectively. For example:

Signal Name	Logical State	Voltage Level
RD-	0 (active)	Low
	1 (inactive)	High
RD+	0 (inactive)	Low
	1 (active)	High

REFERENCES

The CPU, FDC, and HDC Boards in the AWS-220, -230, and -240 are heavily dependent upon programmable LSI circuits to perform their functions. Since the hardware functions and software interfaces of the LSI circuits are only briefly summarized in this Manual, users are likely to want occasional reference to the following manufacturers' literature:

The Central Processing Unit Convergent Technologies, Inc.
Intel 8086 Family User's Manual
Intel Component Data Catalog
NEC Microcomputers, Inc., 1981 Catalog
Signetics 8X300 Reference Manual
8X300 Design Guide, Signetics Corporation
8X330 Floppy Disk Controller, Signetics Corporation
ANSI X3.66, American National Standards Institute, Inc.

1 OVERVIEW

This Manual is for the engineer who writes service manuals or tests the AWS-220, -230, or -240 workstation electronics, or who writes or modifies system software for use with the AWS-220, -230, or -240.

It is not, however, documentation to support modifications of the hardware. The only provision for the user to add to the system is the expansion interface connector on the Motherboard.

The AWS-220, -230, and -240 are designed to run application software and operate in a cluster, minicluster, or as standalone workstations. The AWS-220, -230, and -240 have their own local mass storage peripherals, the type and configuration of which is determined by the model number. European model numbers are determined by adding 500 to the domestic number, that is, an AWS-220 domestic model is an AWS-720 in its European form.

- The AWS-220 can support from 128 to 512 kilobytes of RAM (in increments of 64 kilobytes) and has one 5 1/4-in floppy disk drive with a formatted storage capacity of 315 kilobytes.

- The AWS-230 is identical to the AWS-220, but has an additional floppy disk drive. The total formatted storage capacity of the AWS-230 is 630 kilobytes.

- The AWS-240 can support from 256 to 512 kilobytes of RAM, in increments of 128 kilobytes. The AWS-240 uses a different disk controller than the AWS-220 and AWS-230 to support one 5 1/4-in floppy disk drive and one 5 1/4-in Winchester hard disk drive. The total formatted storage capacity of the AWS-240 is 5.3 megabytes.

The AWS-220, -230, and -240 workstations all have two RS-232-C communications channels and a Centronics-compatible parallel printer channel.

The AWS-220, -230, and -240 workstations contain several programmable peripheral ICs and registers. These are either initialized to

default conditions by the CTOS Operating System during a manual or power-up reset, or they are supported with programs that are linked to the user's application programs. In addition, the Operating System's interrupt service programs often reinitialize or modify the operation of this logic. The descriptions in the "Architecture" section document the interface between software and hardware. A separate "External Interfaces" section provides a collection of both hardware and software interface information for the RS-232-C communications and printer ports, and the keyboard interface.

Figure 1-1 shows the functional blocks of the AWS-220, -230, and -240. The electronics are housed in a desktop enclosure. The 98-key keyboard is housed in a separate enclosure and connected to the base of the desktop enclosure through a detachable coiled cord. The CRT display is in another separate enclosure connected to the base of the desktop enclosure by a tilt and swivel mechanism. The rear of the desktop enclosure has five connectors: two provide for the connection of the workstation into a cluster daisy chain, one is for the parallel printer channel, and two are for RS-232-C Channels A and B.

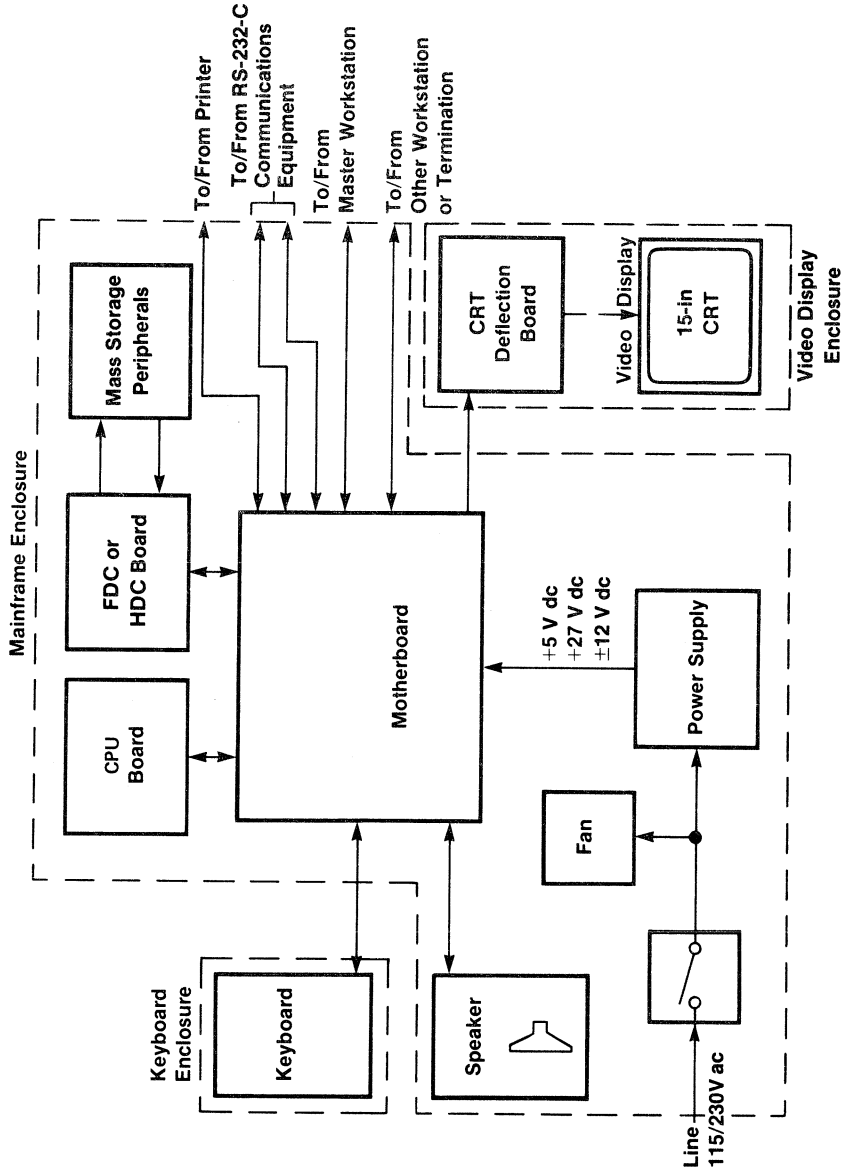


Figure 1-1. AWS-220, -230, and -240 Workstations.

MAJOR COMPONENTS

The major components of the AWS-220, -230, and -240 workstations are:

- a mainframe enclosure that contains everything except the keyboard and video display,
- a keyboard enclosure,
- a 98-station microprocessor-based keyboard with eight LED indicators,
- a single CPU Board that includes an 8088 or 8086 host CPU, up to 512 kilobytes of parity-protected RAM, and input/output logic,
- a single FDC (Floppy Disk Controller) Board for the AWS-220 and AWS-230 or a single HDC (Hard Disk Controller) Board for the AWS-240. The controller boards both include two RS-232-C communications channels, a parallel printer interface channel, and interrupt and bus control logic.
- a Motherboard that connects the CPU Board to the input/output panel at the rear of the mainframe enclosure, the keyboard connector, and the power supply,
- a 137-W switching power supply, and
- a 19.8 MHz etched-faceplate CRT monitor in a tilt-and-swivel enclosure.

CLUSTER ARCHITECTURE

A cluster is a collection of workstations connected by a data communications line. Each workstation includes the memory and processing ability required for the workstation operator. This type of configuration, called distributed processing, allows the processing capabilities of the system to grow uniformly with the number of users.

Cluster workstations are connected by a high-speed (usually 307 kilobaud) RS-422 differential data communications line composed of two twisted pairs of wires: one for data and one for clock. This allows for multidrop, half-duplex operation. A variant of the Advanced Data Communications Control Procedures (ADCCP) protocol is used between workstations for communications.

A cluster is configured to have one master workstation, which polls the other workstations on the cluster. All communications pass between the master workstation and a cluster workstation; communication cannot occur directly between cluster workstations. The cluster workstations share the peripheral devices of the master workstation. The AWS-220 and -230 have their own mass storage peripherals and can either stand alone or share peripherals with the master workstation. Because of its greater mass storage features, the AWS-240 can operate as a master workstation.

Mechanically, the cluster is linked in a daisy-chain configuration. Each cluster workstation has two 9-pin female connectors connected to have parallel electrical lines. Cluster cables consist of two 9-pin male connectors joined by a cable consisting of two twisted pairs of wires and a ground shield.

The daisy chain consists of cluster workstations each having one 9-pin connector with a cable that leads to the master workstation (or to the cluster workstation between it and the master workstation) and one cable that leads away from the master workstation to the next cluster workstation. Cluster workstations at the end of the daisy chain have a special termination connector in place of the cable.

2 ARCHITECTURE

INTRODUCTION

This section addresses the needs of the system programmer who must understand the AWS-220, -230, and -240 workstation hardware at a functional block level and must understand how to program the various LSI devices within it.

Figure 2-1 shows the functional blocks of the logic in the AWS-220, -230, and -240. Each block in Figure 2-1 is discussed in relation to the programmable LSI device or devices performing that function in the workstation. Each subsection describes the nature of the function and how it is implemented. Next, specific status and command registers are examined. Also, several annotated programming examples are provided, which can be used as guides for understanding how certain devices are operated in the workstation. Finally, a summary of all of the input/output ports is given at the end of this section under "Workstation Input/Output Address Summary."

8088 AND 8086 CPU BOARDS

Two CPU Boards are available for the AWS-220, -230, and -240: a standard 8088-based CPU Board, and an optional 8086-based CPU Board.

The 8088 CPU Board for the AWS-220, -230, and -240 uses an Intel 8088 microprocessor operating at 5 MHz with one wait state. The 8088 is a cross between an 8-bit microprocessor, such as the 8085, and a 16-bit one, such as the Intel 8086. Like the 8086, the 8088 has internal operations and registers that are 16 bits in length. Unlike the 8086, which has an external interface that is 16 bits in length, the 8088 has an external interface to the CPU Board logic that is 8 bits in length, which allows simpler data buses and control logic. Strapped to operate in the minimum mode, the 8088's bus control lines are similar to those of an 8085.

The 8086 CPU Board is identical in function to the 8088 CPU Board but uses an 8-MHz Intel 8086 microprocessor. Like the 8088, the 8086 is strapped to operate in the minimum mode. The 8086 inserts one wait state during a RAM write operation and eight during an input/output read operation. The 8086 CPU Board can also accommodate additional boards to enhance its video display capabilities. These advanced video boards are connected to the 8086 CPU Board through the J3 connector.

The only user-noticeable difference between the two boards is that the 8086 CPU Board executes instructions faster than the 8088 CPU Board. The increase in execution speed for the 8086 comes both from its higher clock frequency and also from its ability to read or write 16 bits of data in one memory cycle (the 8088 requires two memory cycles). See Chapters 2 and 4 of The 8086 Family User's Manual (available from the Intel Corporation) for more information on the 8086 and 8088. Throughout this section, when it is unnecessary to distinguish between the 8088 and the 8086, the microprocessor is referred to as "the CPU."

8088 and 8086 Instruction Set

The 8088 and the 8086 are machine-language compatible. The instruction set (see Appendix A)

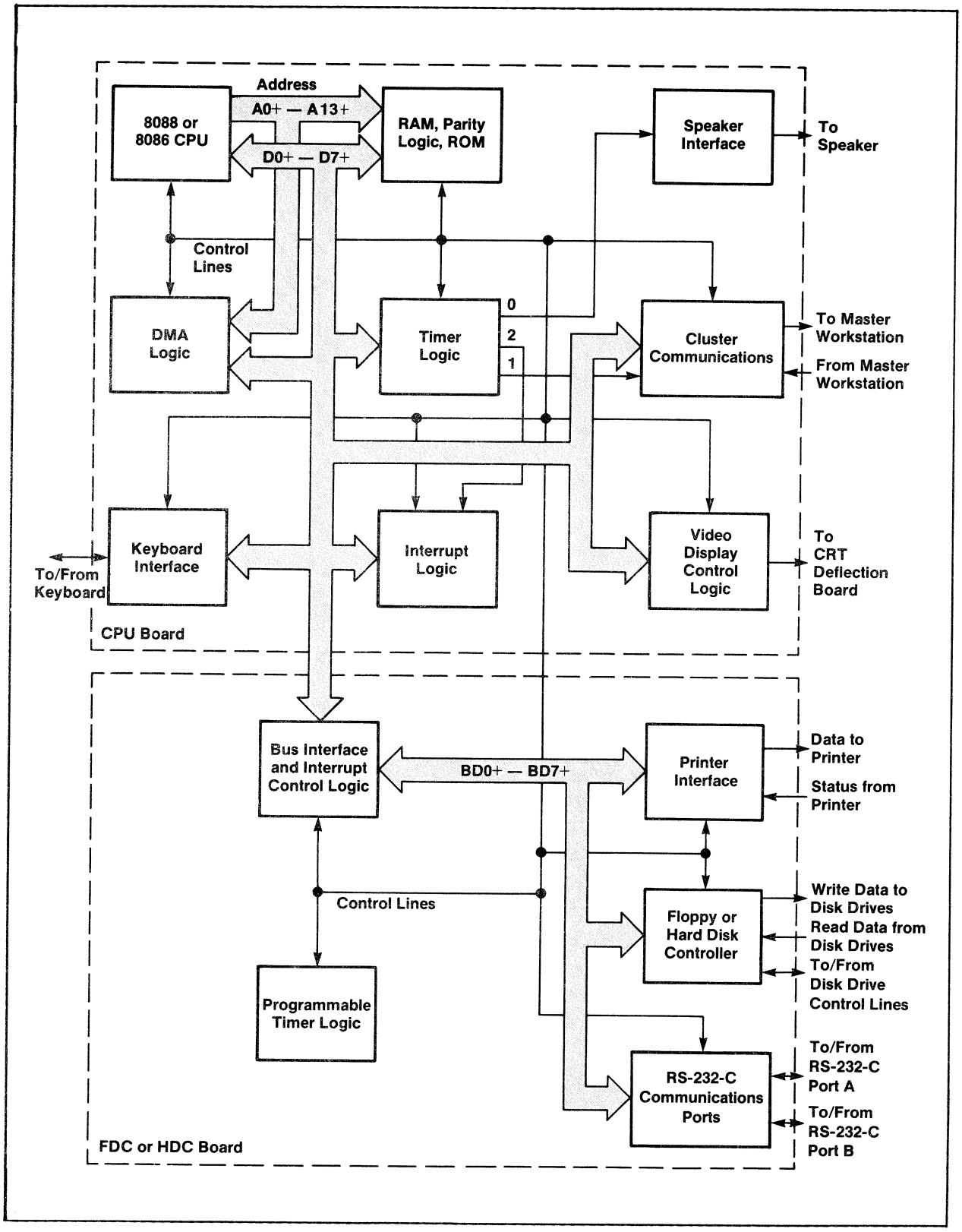


Figure 2-1. Workstation Logic.

is the same for both microprocessors. Two publications available from Convergent Technologies, The Central Processing Unit and the Assembly Language Manual, provide full explanations on programming the 8088.

RAM, PARITY, AND THE BOOTSTRAP ROM

The RAM array on the CPU Board is based on dynamic RAM chips, which are 64 kilobits (kb) by 1 bit. The RAM array is arranged in up to eight rows, with each row containing 64 kilobytes. Physically, each row has nine 64-kb chips: one for each of the eight data bits plus one for a parity bit.

The number of rows of RAM installed on the 8088 or 8086 CPU Boards can vary. In the minimum configuration, the CPU Board in the AWS-220 and -230 has only two rows of RAM, providing a total of 128 kilobytes; the AWS-240 has a minimum of four rows of RAM, providing 256 kilobytes. In the maximum configuration, the CPU Board has all eight rows installed, providing 512 kilobytes.

As shown in Figure 2-2 below, RAM addressing starts at location 0 in the address space and ascends to a maximum address of 7FFFFh when all eight banks are populated. If a program reads a RAM location that does not have RAM chips installed, a value of FFh is returned and a parity error occurs.

The RAM array is accessible by the CPU or an 8257 Direct Memory Access (DMA) controller. When either device performs a write operation to the RAM array, a parity bit is stored along with the eight data bits. If parity detection is enabled by the CPU (by reading Port F0h) and a RAM location is read, the nine bits are checked for proper parity. If an error is detected, the status of the address bus is saved in the input/output registers, and a nonmaskable interrupt to the CPU occurs. The nonmaskable interrupt causes the CPU to branch to the address contained in locations 8, 9, A, and B: the starting address of error-recovery software. This starting address uses the Parity Error Register to determine the error address. The parity error condition is cleared by reading Port F4h, which disables parity detection. Parity detection is also disabled when the AWS-220, -230, and -240 are reset, either by a manual or power-up reset.

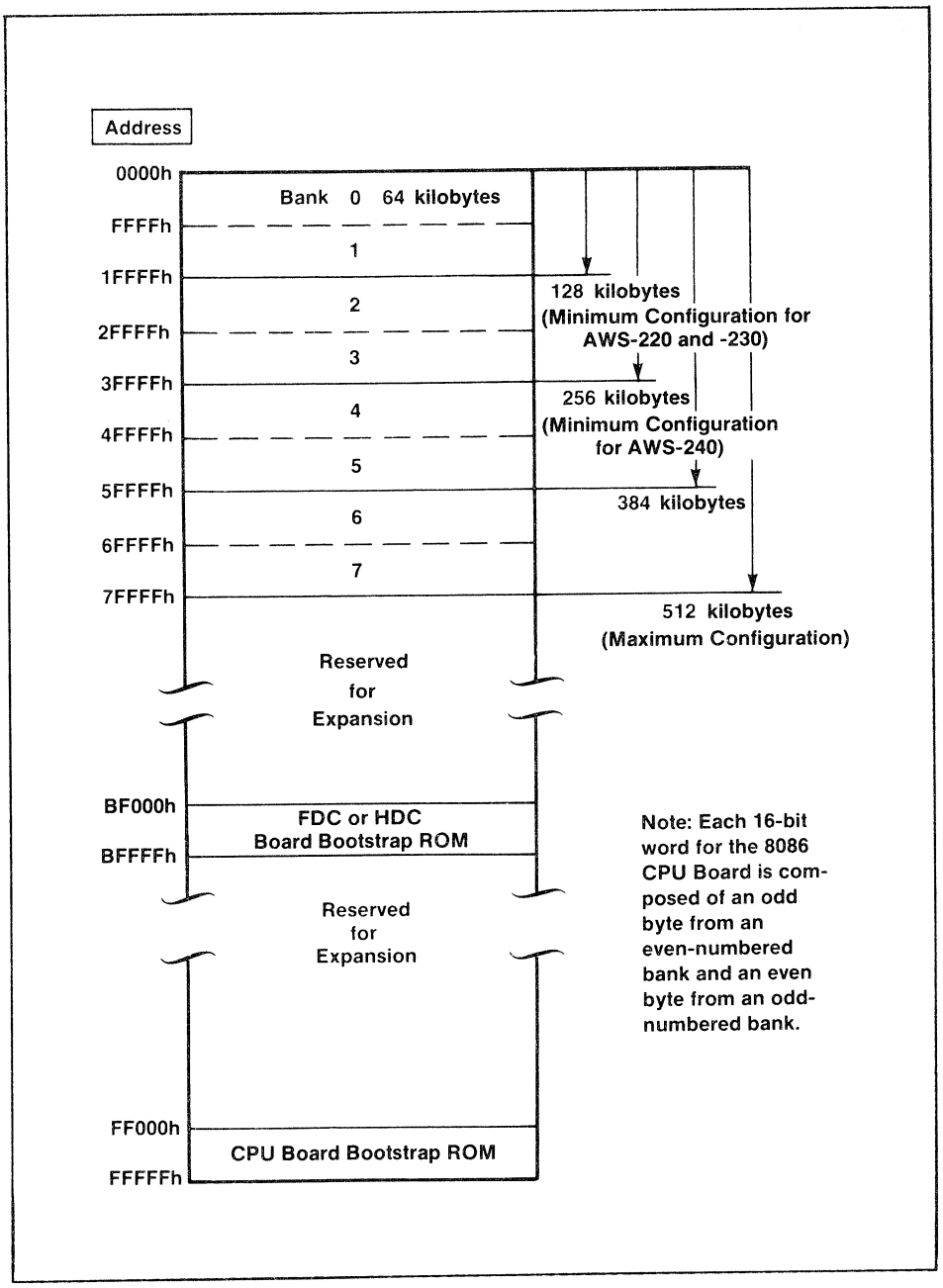


Figure 2-2. RAM and ROM Memory Space.

Parity Control Ports and Parity Status Ports

Port F4h

Reading Port F4h disables parity error detection and clears existing parity error conditions. Once a parity error occurs, it must be cleared before another can be detected. The data read from Port F4h are always FFh.

Port F0h

Reading Port F0h enables parity error detection and nonmaskable interrupts. The data read from Port F0h are always FFh.

Port E0h

Port E0h contains the low-order, 8-bit memory address of the most recent parity error. If no error has occurred since the workstation was powered up, Port E0h is random; it is only updated when a nonmaskable interrupt occurs. For Port E0h to be updated, parity detection must be enabled and previous errors must be cleared.

Register AL Bit (CPU)	Read Information
0-7	0-7

Port E4h

Port E4h is identical to Port E0h except that it contains bits 8h-Fh of the error address.

Register AL Bit (CPU)	Read Information
0-7	8-F

Port E8h

Port E8h is identical to Port E0h except that it contains bits 10h-13h of the error address and a single bit indicating whether DMA was in progress when the error occurred.

Register AL Bit (CPU)	Read Information
0	10
1	11
2	12
3	13
4	If 1, DMA was active when the error occurred.

Bootstrap ROM Firmware

The bootstrap ROM firmware on the CPU Board is executed when the workstation receives a manual or power-up reset, or when the program running in RAM enters it. The firmware features include:

- Automatic self-test of both hardware and memory. Any errors are reported to the user by either an audible alarm and the display of a unique error code on the keyboard LEDs, or the display of a unique error code on the video display.

- Operating System or diagnostic bootstrap from a local disk drive, or from (by explicit selection or if an error occurs) the master workstation.

- Option menu. Options include loading special System Image files (such as diagnostics), dumping the content of RAM to the local disk drive or the master workstation, testing communications or repetitive testing of memory, and running the panel debugger routine.

Upon entry, the bootstrap ROM tests the hardware, and checks and tests the amount of memory, displaying a "*" for every 64 kilobytes tested. Next, the bootstrap ROM loads the System Image from the local disk drive or master workstation, displaying a "." for every sector transferred.

The bootstrap ROM in the AWS-220 or -230 first attempts to load <Sys>SysImage.Sys from the local floppy disk drive 0. If an error occurs or a floppy disk is not inserted, the bootstrap ROM attempts to load [Sys]<Sys>WS254>SysImage.Sys from the master workstation over the cluster communications line.

The bootstrap ROM in the AWS-240 first attempts to load <Sys>SysImage.Sys from the floppy disk drive (drive 0). If not successful, the bootstrap ROM attempts to load <Sys>SysImage.Sys from the hard disk drive (drive 1). If still unsuccessful, the bootstrap ROM attempts to load [Sys]<Sys>WS253>SysImage.Sys from the master workstation over the cluster communications line.

If the bootstrap ROM is unsuccessful at finding a System Image file at the master workstation, error B3h occurs (see "Error Codes" below).

When the System Image is being loaded, the video display shows the message:

```
T
**
L.............. (etc.)
```

If more than 128 kilobytes of RAM are being tested on the CPU Board, more "*" characters are displayed. Similarly, a typical System Image file (CTOS Operating System or diagnostic) displays several lines of "." characters.

If any key is held down while the bootstrap ROM is initializing, the sequence described above does not occur. Instead, the bootstrap ROM enters the menu mode, in which the user can change the type of Operating System, dump the content of RAM to the local disk drive or a master workstation, run diagnostic tests, or use the panel debugger (see "Menu Mode" below).

Since the bootstrap ROM uses a variable identification mode of cluster protocol (described below under "Cluster Protocol") it cannot work properly if IWS cluster workstations on the communications line are using a fixed identification mode.

Menu Mode

The bootstrap ROM enters the menu mode when the user holds down any key while pressing the reset button on the workstation's back panel. The video display is then initialized, and the following message appears:

```
V x.y

B, C, D, L, M, P, T:
```

where

x.y — is the version number of the bootstrap ROM.

An option is selected when the user presses the appropriate character without using the SHIFT or RETURN key. The keyboard input routine of the bootstrap ROM uses the keyboard codes directly (that is, it does not translate them). Thus, keys such as SHIFT, CODE, and those on the numeric keyboard are interpreted as invalid characters and should not be used. Also, in the panel debugger routine, the ";:" key is used without the SHIFT key to get the ":" character.

The menu options are: B for bootstrap, C for communications test, D for dump, L for load, M for memory test, P for panel debugger, and T for the type of Operating System.

B Boot. The bootstrap ROM RAM loads the System Image file. If the T (type of Operating System) option is not selected, the bootstrap ROM attempts to load the System Image file from the following sources, in order, just as if the reset button were pressed:

1. local floppy disk drive 0,
2. local hard disk drive 1 (AWS-240 only),
3. [Sys]<Sys>WSnnn>SysImage.Sys (where nnn equals 254 for the AWS-220 and AWS-230 or 253 for the AWS-240) at the master workstation.
4. [Sys]<Sys>WS>SysImage.Sys, the default System Image file, at the master workstation.

If the bootstrap ROM does not find a System Image file at the master workstation, error B3h occurs (see "Error Codes" below).

Note that if the T option is selected, the local disks are not checked for the presence of a valid System Image file. Instead, the System Image is loaded from the specified System Image at the master workstation (see "T Type of Operating System" below).

C Communications Test. The bootstrap ROM tests the RS-422 communications channel and DMA hardware; error codes appear on the video display. The cluster cables on the workstation must be disconnected before the communications test is run.

D Dump. The content of RAM is dumped to the local disk drive, or, if an error occurs (such as if no disk is present), to the master workstation. The bootstrap ROM will attempt to dump to the following files, in order:

1. <Sys>CrashDump.Sys at the local floppy disk drive 0,

2. <Sys>CrashDump.Sys at the local hard disk drive 1 (AWS-240 only),

3. [Sys]<Sys>WSnnn>CrashDump.Sys (where nnn is the workstation number, not type, between 1 and 15) at the master workstation,

4. [Sys]<Sys>WS>CrashDump.Sys, the default System Image file, at the master workstation.

If neither CrashDump file exists at the master, error ADh occurs (see "Error Codes" below).

L Load. The bootstrap ROM loads the System Image file from the local disk drive or master workstation, as described above under "Boot." However, instead of jumping to the first location of the System Image, the bootstrap ROM enters the panel debugger. As soon as the panel debugger is exited, the System Image executes (see "Panel Debugger Routine," below).

M Memory Test. The bootstrap ROM repeatedly tests the RAM array. The test is terminated when the user presses the reset button on the back panel of the workstation. Any errors cause the memory test to halt and the appropriate error code and message to appear on the video display.

P Panel Debugger. This test is entered and exited as described below in "Panel Debugger Routine."

T Type of Operating System. When the bootstrap ROM prompts with "OS:," the user enters the number of the desired System Image at the master workstation and presses RETURN. The file to be loaded is [Sys]<Sys>WSnnn>SysImage.Sys where nnn is the numeric code entered in response. Only the digit keys on the typewriter pad of the

keyboard should be used, not the keys on the numeric keypad. The T option influences the operation of subsequent B and L options.

Panel Debugger Routine

The bootstrap ROM includes a panel (virtual console). The panel debugger routine is of limited use as a general software debugger, but it is useful when the workstation cannot successfully run the Operating System.

The panel debugger routine is entered when the bootstrap ROM is in the menu mode and the user presses P. When the panel debugger routine is entered, the address of the instruction that caused it to be entered is displayed in CS:IP format (see "Register Structure" in The Central Processing Unit). Next, the panel debugger routine prompts the user with a "+" character and waits for a command to be keyed in (as described below).

All numbers in the panel debugger routine are hexadecimal words (never bytes). Addresses are entered in the format SA:RA, where SA (Segment Base Address) and RA (Relative Address, that is, the number of bytes from the beginning of the segment pointed to by SA) are entered in hexadecimal format. The first digit must be numeric (for example, the user enters 0FFFF rather than FFFF). Only the last four digits of any word are used, although more can be keyed in. Because it is always remembered by the panel debugger routine (initially, the SA is FF00h), the SA does not have to be keyed in every time. Thus, an address can be specified by SA:RA, or just RA. If an input/ output port is specified, RA is used by the panel debugger routine as the port address.

Upon entry to the panel debugger routine, the twelve CPU Word Registers, the Instruction Pointer, and the Flag Register are saved on the user stack. The RAM location of each register can be addressed by keying in the name of the register.

The names of the registers (in the order in which they are located in memory) are: SP, SS, ES, DS, BP, DI, DX, CX, BX, AX, SI, IP, CS, and FL. The Byte Registers cannot be specified explicitly,

since the panel debugger routine does not support byte memory operations. Note that, due to the characteristics of the 8086/8088 family of microprocessors, the AX Register is composed of the AL and AH Registers, the BX Register is composed of BL and BH Registers, etc.

The panel debugger routine recognizes the characters RETURN, NEXT, ";" (printed as ":"), "/", 0 to 9, and A to Z. Typing other characters causes the audible alarm to sound and the current command to terminate without executing. In the examples given below, the panel debugger routine displays "xxxx", "=", and the address at the beginning of those lines that do not begin with "+".

The panel debugger routine has five commands:

- Open/Modify RAM,
- Open/Modify Register,
- Input/Output from or to a Port,
- Set Haltpoint, and
- Proceed/Go.

In the Open/Modify RAM command, an address, followed by a "/" character is keyed in to examine a RAM location. The content of the RAM location can be either modified or left as is (and the next sequential RAM location examined). The Open/Modify command can also be terminated without changing the RAM location.

To modify the word at RAM location F00:3Ch to contain 701h, enter:

```
+0F00:3C/ xxxx 701<RETURN>
+
```

To modify words at 0:0 and 0:4 to contain 3F0h and 23h, respectively, and to examine words at 0:2 and 0:6 without modification, enter:

```
+0:0/ xxxx 3F0<NEXT>
0000:0002 xxxx<NEXT>
0000:0004 xxxx 23<NEXT>
0000:0006 xxxx<RETURN>
+
```

To use the Open/Modify Register command, a register name is keyed in in response to the "+" prompt. A "/" character is not required.

To change the content of the DX Register to contain A03h, enter:

```
+DX xxxx 0A03<RETURN>
+
```

(Note that 0A03h must be keyed in instead of A03h.)

To use the Input/Output from or to a Port command to input a byte from a port, the user keys in the address (in the format SA:RA; SA is ignored), followed by the command I. A byte is input from the port, the byte is displayed, and the command is terminated.

To use the Input/Output from or to a Port command to output a byte to a port, the user keys in the address, followed by the command O. The panel then displays a "=" character. The user then keys in the byte to be output to the port, followed by a RETURN. Note that the output command does not input from the port. This is to accommodate input/output controllers that change state when their input/output port is read. Also note that port operations on the AWS-220, -230, and -240 are byte, not word, operations. The workstation input/output ports are listed in Table 2-1 at the end of the "Architecture" section.

To input the content of Port A0h, enter:

```
+0A0I xx
+
```

To output 7Ah to Port A1h, enter:

```
+0A1O=7A<RETURN>
+
```

The Set Haltpoint command sets a haltpoint when the user keys in the RAM address, followed by the command H. This sets an internal panel debugger routine flag and stores the address for later use. When the panel debugger routine is exited, by pressing G (Go) or P (Proceed), the haltpoint is inserted in RAM at the specified address. Only one haltpoint can be set at a time; if more than one is specified, the one set most recently is used.

When the haltpoint is executed, the original instruction is restored and can be executed using the command P. The panel debugger routine remembers the existence and location of a haltpoint by storing information in the 16 bytes reserved at 0000:01F0h.

To avoid conflict with the the single-byte INT 3 instruction of the Operating System Debugger, the haltpoint is a 2-byte instruction (INT 7Ch). If the haltpoint is set as a single-byte instruction, and there is a jump to the next instruction, the result is unpredictable. A haltpoint cannot be set in ROM.

Setting a haltpoint at the current CS:IP causes the panel debugger routine to be reentered immediately if the user presses the command P. A haltpoint at the same address is reestablished by setting the haltpoint at the next instruction, proceeding, setting the haltpoint at the desired address, and proceeding again.

To set a haltpoint at 1E21:C3H, enter:

```
+1E21:0C3H
+
```

To reestablish the haltpoint at 1E21:C3h after it is encountered, enter:

```
1E21:00C3
+E21:0CxH    (address of next instruction,
              not the next byte)
+P
1E21:00Cx
+1E21:0C3H
+P
```

The panel debugger routine is exited either when the user presses the command P (Proceed), or keys in an address, followed by the command G (Go). In the first case, execution is resumed at the current CS:IP, which is saved on the stack. In the second case, execution is resumed at the specified address.

To proceed from the current CS:IP, enter:

```
+P
```

To go from 1E43:90h, enter:

```
+1E43:90G
```

Firmware Functional Description

Cluster Protocol. Cluster architecture is discussed in detail in the System Programmer's Guide. The general protocol of the Operating System dictates that the master workstation poll the cluster workstations, and the master workstation and the cluster workstations exchange messages. The protocol requires that every workstation on the cluster communications line (or all workstations in a minicluster) have a unique workstation identification number.

The master workstation initiates all communications; a cluster workstation recognizes messages intended for it by the workstation identification number. The cluster workstation picks a workstation identification number by (1) monitoring the cluster communications line to find an unused one, (2) taking an unused number, and then (3) monitoring the cluster communications line again to see if it has collided with another workstation that may have picked the same number. If a collision occurs, both workstations wait a random time interval before restarting the search for another identification number.

The workstation identification number can be between 1 and 15, the largest number of cluster workstations allowed on a single cluster communications line. Identification numbers are not the same as user numbers. User numbers are assigned to cluster workstations by the Operating System of the master workstation and are different for every workstation in a cluster. Identification numbers are determined by the cluster workstations and are duplicated on the different cluster communications lines of a cluster, since a cluster can have up to four separate communications lines.

The actual protocol used for cluster communications is a subset of the American

National Standard for Advanced Data Communications Control Procedures (ADCCP), as defined in ANSI X3.66, published by the American National Standards Institute, Inc. The sequence used during the dump and bootstrap routines is illustrated in Figure 2-3 below. The protocol symbols are:

Symbol	Meaning
SNRM	Set Normal Response Mode
RIM	Request Initialization Mode
SIM	Set Initialization Mode
XID	Identification Frame (contains workstation type)
UP	Unnumbered Poll
UI	Unnumbered Data Frame
RD	Request Disconnect
DISC	Disconnect
UA	Unnumbered Acknowledge
UI'	Unnumbered Data Frame (with termination data)

Bootstrap Interface Block. When a program is loaded, and before execution is transferred to it, the bootstrap ROM places a 16-byte structure in memory with a pointer to it at location 1FCh. The structure of the bootstrap interface block is:

```
BootBlock:      RECORD
                pProgramStart,
                pCtosBuffer: POINTER;
                DumpDevice,
                BootDevice,
                WsType,
                DumpWsNumber/DumpErrorCode,
                BootWsNumber,
                unused,
                unused,
                unused: BYTE;
                END;
```

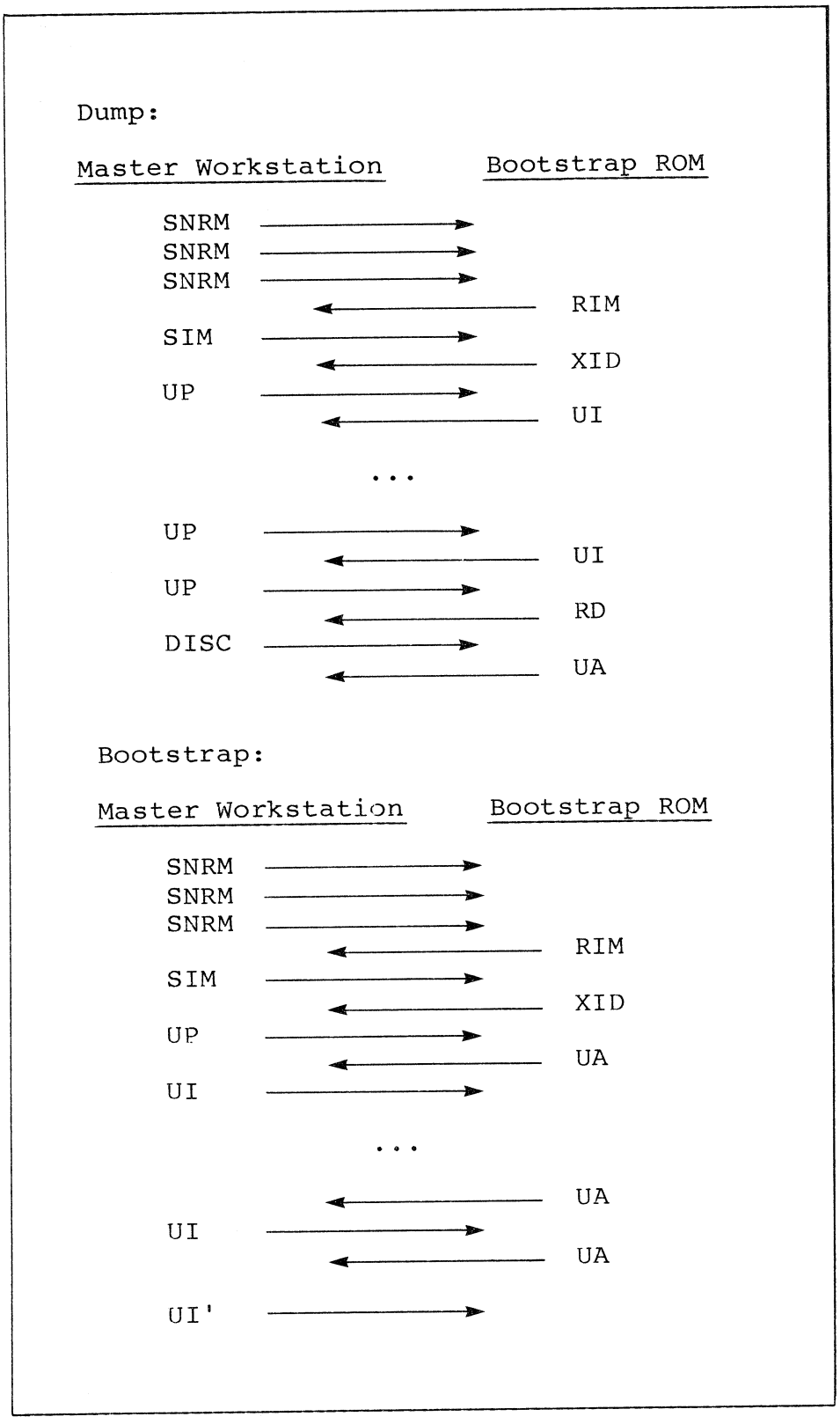


Figure 2-3. Communications Dump and Bootstrap Protocol.

The dump and bootstrap device numbers are either 0 (failed), 1 (floppy disk drive 0), 2 (hard disk drive, on the AWS-240 only) or 3 (communications line). The workstation type (WsType) is either 253, 254, or some other type selected using the T option on the menu (see Menu Mode above). Dump and bootstrap workstation identification numbers (WsNumbers) are those that the bootstrap ROM picked during the dump and/or the bootstrap. If the dump failed, the failing error code is saved in the DumpWsNumber field.

The CTOS Operating System also examines the ROM type number, which is a word (80h for the bootstrap ROM) found at location FFFF:0006h. Any application that wants to access this ROM type number must do so with parity disabled or a parity error results.

CTOS Operating System Buffer. The bootstrap ROM saves a 64-byte buffer for the CTOS Operating System. The CTOS Operating System has a pointer to the buffer at location 0000:0240h. The buffer must lie beyond the first 6 kilobytes of RAM, which are the bootstrap ROM's work area. The bootstrap ROM copies the buffer into its work area and sets the pointer (pCtosBuffer) to this copy in the Bootstrap Interface Block. The CTOS Operating System uses this pointer to recover the buffer after it has been bootstrapped.

Bootstrap Errors

When the workstation is bootstrapped, it goes through diagnostic and bootstrapping routines, which are resident in the ROM of the CPU. When an error is detected by the bootstrap ROM, the error code appears on the video display. For E0 and E1 error codes only, the audible alarm is cycled on and off five times and the error code appears on the keyboard LEDs.

Errors During Bootstrap or Dump. The communications bootstrap or dump routines do not stop to report an error if there is no activity on the RS-422 cluster communications line. This can occur when the cable to the master workstation is disconnected, when the master workstation crashes, or when the master workstation is disabled by the Disable Cluster

utility. When the connection with the master workstation is reestablished, the bootstrap or dump routine automatically starts (indicated on the video display by a "." for every sector transferred).

Interpreting Keyboard Error Codes. The E0h and E1h error codes are displayed on the keyboard LEDs. They are interpreted as follows.

LED	Error E0h	Error E1h
OVERTYPE	on	on
LOCK	on	on
F1	on	on
F2	off	off
F3	off	off
F8	off	off
F9	off	off
F10	off	on

Error Codes. For most of the error codes listed in hexadecimal format below, there is also a list of possible causes for the error (listed with the most likely cause first).

AWS-220 and -230 Floppy Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
00-02	Unused
03	Timeout waiting for an interrupt after a seek command. The floppy disk controller did not interrupt the CPU after being issued a seek command. Check: 1. that the operator did not open the door of the floppy disk drive, or 2. the seating of the FDC and CPU Boards on the Motherboard.

AWS-220 and -230 Floppy Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
04	Data bit set. The data input/output bit of the Floppy Main Status Register (Port 80h bit 6) is continually set to 1. The CPU cannot issue a command to the floppy disk controller. Check: the FDC Board (8272).
05	Data bit not set. The request for master bit of the Floppy Main Status Register (Port 80h bit 7) is never set to 1. The floppy disk controller can neither accept a data byte from the bus master nor send a byte to the bus master. Check: the FDC Board (8272).
06	DMA not done. The Byte Count Register of the 8257 Channel 0 never decremented to 0, which means that the DMA operaton never finished. Check: the CPU Board (8257).
07-08	Unused
09 0A	Run file checksum error. File header invalid. The System Image file on the floppy disk in drive 0 does not contain a valid run file. Since the Initialize Volume utility does not automatically copy a System Image onto the volume it is initializing, the user must copy a valid System Image onto the volume. Check: the floppy disk.

AWS-220 and -230 Floppy Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
0B	Floppy Control Register inconsistent. The Floppy Main Status Register was polled until it became ready (Port 80h was 80h). The Floppy Main Status Register was then polled again and it was not ready. Check: the FDC Board (8272).
0C	Floppy disk drive became not ready during a seek. The floppy disk drive became not ready while performing a Seek command. This error can be caused by opening the door of the floppy disk drive or by a bad cable from the floppy disk drive to the Motherboard. Check: 1. operator intervention, 2. the cable from the floppy disk drive to the Motherboard, 3. the floppy disk drive, or 4. the FDC Board (8272).
0D	Invalid floppy disk drive controller command received. The floppy disk drive controller received an undefined command during a Seek or Recalibrate command. Check: 1. the seating of the FDC Board on the Motherboard, or 2. the FDC Board (8272).
0E	Floppy disk drive not ready. The floppy disk drive was not ready when the Seek or Recalibrate command was issued. Check: 1. that the floppy disk is inserted in drive 0 with the disk label on the opposite side of the release latch, or 2. that the door of the floppy disk drive is properly closed.

AWS-220 and -230 Floppy Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
0F	Floppy disk drive fault condition during a Seek or Recalibrate command. The floppy disk drive did not recalibrate to track 00 after 77 step pulses or the drive fault line went active. Check: 1. the cable between the floppy disk drive and the Motherboard, 2. the floppy disk drive, or 3. the FDC Board (8272).
10	Abnormal termination of Seek command. The floppy disk drive did not complete the Seek command correctly. Either the floppy disk drive failed or the ready status changed. Check: 1. operator intervention, 2. the floppy disk, 3. the cable between the floppy disk drive and the Motherboard, 4. the floppy disk drive, or 5. the FDC Board (8272).
11	Floppy disk drive became not ready. The floppy disk drive became not ready during a data transfer. Usually, this error is caused by opening the door of the floppy disk drive. Check: 1. operator intervention, 2. the floppy disk, 3. the cable between the floppy disk drive and the Motherboard, 4. the floppy disk drive, or 5. the FDC Board (8272).

AWS-220 and -230 Floppy Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
12	Invalid floppy disk drive command received. The floppy disk drive controller reported an undefined command when the bootstrap ROM requested a data transfer. Check: 1. the seating of the FDC Board on the Motherboard, or 2. the FDC Board (8272).
13	Floppy disk drive not ready. The floppy disk drive was not ready when a Read or Write command was issued. This error can only occur if the floppy disk drive was ready during a previous Recalibrate command and a previous Seek command. Check: operator intervention.
14	Floppy disk drive fault condition during a data transfer. The floppy disk drive's fault line went active. Check: 1. the cable between the floppy disk drive and the Motherboard, or 2. the floppy disk drive.
15	End of track. After a Read or Write command, no EOT signal was received from the 8257. Check: 1. the cable between the floppy disk drive and the Motherboard, 2. the CPU Board (8257), or 3. the FDC Board (8272).

AWS-220 and -230 Floppy Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
16	Data error (data field). The floppy disk drive controller cannot read data from the floppy disk drive correctly. Check: 1. the floppy disk, 2. the cable between the floppy disk drive and the Motherboard, 3. the floppy disk drive, or 4. the FDC Board (8272).
17	Data error (identification field). The floppy disk drive controller cannot read the identification field of the addressed sector. Check: 1. the floppy disk, 2. the cable between the floppy disk drive and the Motherboard, 3. the floppy disk drive, or 4. the FDC Board (8272).
18	Data late. The floppy disk drive controller did not get service from the 8257 in time. Check: 1. the seating of the CPU and FDC Boards on the Motherboard, 2. the CPU Board (8257), or 3. the FDC Board (8272).
19	No data (wrong track). During a Read or Write command, the floppy disk drive was on the wrong track. That is, either the floppy disk is incorrectly initialized or a Seek command sent the read/write head to the wrong track. Check: 1. the floppy disk, 2. the cable between the floppy disk drive and the Motherboard, 3. the floppy disk drive, or 4. the FDC Board (8272).

AWS-220 and -230 Floppy Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
1A	No data (bad track). The track accessed was marked as number 255 (0FFh). Check: 1. the floppy disk, or 2. the FDC Board (8272).
1B	No data. The floppy disk drive controller reported a no data condition. The specified sector could not be found. Check: 1. the floppy disk, 2. the cable between the floppy disk drive and the Motherboard, 3. the floppy disk drive, or 4. the FDC Board (8272).
1C	Floppy disk write protected. This error code appears only during the dump operation and indicates that the floppy disk has a write protect tab in place. Check: the floppy disk.
1D	Missing address mark (data field). The floppy disk drive controller cannot find any identification address marks on the track. Usually, this error means that the floppy disk was not initialized by the Initialize Volume Utility. Check: 1. the floppy disk, 2. the cable between the floppy disk drive and the Motherboard, 3. the floppy disk drive, or 4. the FDC Board (8272).
1E	Unused

AWS-220 and -230 Floppy Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
1F	Abnormal termination of command. The floppy disk drive controller reported abnormal termination of a command without reporting the cause. Check: the FDC Board (8272).

AWS-240 Disk Drive Errors

20-22	Unused
23	Timeout waiting for an interrupt after issuing a read or write command. The disk controller did not interrupt the CPU after performing a read or write command. Check: 1. that the operator did not open the door of the floppy disk drive, or 2. the seating of the HDC and CPU Boards on the Motherboard.
24	CMDBUSY always set. Bit 5 of Flag Register 1 (Port 8Eh) is continually set, which means that the disk controller cannot accept a command. Check: the HDC Board.
25	STRDY never set. Bit 1 of Flag Register 0 (Port 8Fh) is never set, which means that the Status Registers cannot be read. Check: the HDC Board.

AWS-240 Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
26	DMA not done. The Byte Count Register of 8257 Channel 0 never decremented to 0, which means that the DMA operaton never finished. Check: the CPU Board (8257).
07-08	Unused
29 2A	Run file checksum error. File header invalid. The System Image file on the floppy disk in drive 0 does not contain a valid run file. Since the Initialize Volume utility does not automatically copy a System Image onto the volume it is initializing, the user must copy a valid System Image onto the volume. Check: the floppy disk.
2B	Unused
2C	Invalid command received. The disk controller received an undefined command from the host processor. Check: the seating of the HDC and CPU Boards on the Motherboard.
2D	Drive not ready. The disk drive was not ready when a Seek or Recalibrate command was issued. Check: the disk drive power connections.

AWS-240 Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
2E	Disk fault condition during Fault or Recalibrate command. The disk drive did not recalibrate, or the drive fault line became active. Check: 1. the disk drive cable to the Motherboard, or 2. the disk drive.
2F	Abnormal termination of Seek command. The disk drive did not sucessfully seek a specified track. Either the drive failed or the ready status changed. Check: 1. the disk drive cable, 2. the disk drive, or 3. the HDC Board.
30	Disk drive became not ready. The disk drive became not ready during a data transfer. Check: 1. the disk drive cable, 2. the disk drive, or 3. the HDC Board.
31 32 33 34	Invalid command (bad head). Invalid command (bad sector). Invalid command (bad track). Invalid disk command issued. The disk controller received an invalid parameter or an undefined command from the CPU. Check: 1. the disk drive cable, 2. the HDC Board, or 3. the CPU Board.

AWS-240 Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
35	Disk drive not ready. The disk drive became not ready when a Read or Write command was issued. This error can occur only if the disk drive was ready during execution of a previous Recalibrate and Seek command. Check: 1. the disk drive cable, 2. the HDC Board, or 3. the CPU Board.
36	Disk drive fault condition during input/output. The disk drive fault line went active. Check: 1. the disk drive cable, or 2. the disk drive.
37	Data late. The drive controller did not receive service from the 8257 DMA channel in time to satisfy the disk drive. This error code can only occur in reference to Drive 0 on the AWS-240. Check: 1. the floppy disk drive cable, 2. the HDC Board, or 3. the CPU Board (8257).
38 39	Data CRC. Identification CRC. A Cyclical Redundancy Check (CRC) error occurred in a sector of data read or in the address information of the sector (identification). This generally indicates an error on the disk media. Check: 1. the disk drive, 2. the disk drive cable, 3. the HDC Board (data separator), or 4. the CPU Board.

AWS-240 Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
3A	Halt during execution. The disk controller received a Halt command during execution of another command. Check: 1. the disk drive cable, 2. the HDC Board, or 3. the CPU Board.
3B	Sector not found. The sector in a Read or Write command was not found on the track. This can occur if neither a sector mark nor a matching sector number were found. Check: 1. the disk drive, 2. the disk drive cable, 3. the HDC Board (data separator), or 4. the CPU Board.
3C	Abnormal termination of command (no specified cause). The disk reported abnormal termination of a command without reporting any cause. Check: the HDC Board.
3D	Invalid hard disk parameters. The parameters returned by the disk controller for either the number of sectors per track or the number of tracks per head was zero. Check: the HDC Board.
3E	Disk write protect. A write operation was attempted to a write protected disk.
3F to 40	Unused

AWS-240 Hard Disk Drive Errors

Error Code	Message/Meaning/Possible Causes
41 to 5E	These codes are for Drive 1 on the AWS-240 and are the same, respectively, as the 21 to 3E error codes listed above.
5F to A2	Unused

Communications Errors

A3 Serial input/output error.

The serial input/output initialization routine detected an error in the serial input/output communications controller chip.

Check: the CPU Board (7201).

A4 8253 error.

The clock initialization routine detected an error in the 8253 programmable counter/timer chip.

Check: the CPU Board (8253).

A5 No SIM.

RIM was sent to the master workstation, but no SIM was received. This indicates that the workstation is able to receive but not transmit, or that the master workstation is able to transmit but not receive.

Check:

1. the CPU Board (7201 and cluster communications logic),
2. the master workstation,
3. the communications cable, or
4. the Operating System of the master workstation, which may have crashed.

Error Code	Message/Meaning/Possible Causes
A6	No UP in initialization (SNRM). A UA or XID was sent to acknowledge the SIM sent by the master workstation, but the master workstation sent back an SNRM instead of a UA. The master workstation probably timed out, while waiting for the UA or XID. Check: 1. the CPU Board (7201 and cluster communications logic), 2. the master workstation, 3. the communications cable, or 4. the Operating System of the master workstation, which may have crashed.
A7	No UP in initialization (DISC). A UA or XID was sent to acknowledge the SIM sent by the master workstation. The master workstation sent back a DISC instead of a UA. Check: 1. the CPU Board (7201 and cluster communications logic), 2. the master workstation, 3. the communications cable, or 4. the Operating System of the master workstation, which may have crashed.
A8	No UP in initialization. A UA or XID was sent to acknowledge the SIM sent by the master workstation. The master workstation sent back something other than a UA. Check: 1. the CPU Board (7201 and cluster communications logic), 2. the master workstation, 3. the communications cable, or 4. the Operating System of the master workstation, which may have crashed.

Communications Errors

Error Code	Message/Meaning/Possible Causes
A9	No identification available. The initialization routine monitored the cluster communications line but never found a free identification number. This is usually caused by attaching more workstations to a cluster communications line than the Operating System of the master workstation is designed to accept. Check: the Operating System of the master workstation, which may have crashed.
AA	Identification failure. The initialization routine found free workstation identification numbers by monitoring the communications line, but errors were detected when it tried to use one. This is usually caused by a failure of the collision recovery algorithm and can be overcome by pressing the reset button on each of the back panels of the workstations that collided.
AB	Read identification timeout. The initialization routine timed out after waiting 10 seconds while monitoring the communications line for a workstation identification number. This error code is only generated after a number of unsuccessful reads. Check: 1. the CPU Board (7201 and cluster communications logic), 2. the master workstation, 3. the communications cable, or 4. the Operating System of the master workstation which may have crashed.

Communications Errors

Error Code	Message/Meaning/Possible Causes
AC	Bad address (dump routine). The workstation identification number sent in a frame by the master workstation did not match the one expected. Check: 1. the communications cable, or 2. the CPU Board.
AD	Disconnected (dump routine). The master workstation sent a DISC because of excessive line or protocol errors or because of a conflict with the crash/dump file at the master workstation. Check: 1. that either the file [Sys]<Sys>WSnnn>CrashDump.Sys or [Sys]<Sys>WS>CrashDump.Sys at the master workstation exists, 2. that the file is not in use by another workstation that is dumping, 3. that the file is large enough, 4. the communications cable, or 5. the CPU Board.
AE	No UP - SNRM.
AF	No UP - REJ.
B0	No UP. After transmitting a dump block, an unexpected response was received from the master workstation. Check: 1. whether an IWS cluster workstation is using the fixed identification mode or 2. the CPU Board (7201).
B1	Read UI error. A bootstrap block (frame type UI) was expected, but another frame type was received.

Error Code	Message/Meaning/Possible Causes
B2	Read SNRM error. A bootstrap block (frame type UI) was expected, but a SNRM was received. Check: the CPU Board (7201).
B3	Disconnected. The master workstation chose to send a DISC because of a conflict with the System Image file, or possibly because of excessive errors during transmission. Check: 1. That there is a [Sys]<Sys>WSnnn>SysImage.Sys file at the master workstation for the workstation type selected nnn. The type defaults to 253 for the AWS-240, to 254 for the AWS-220 and 230, or to whatever was selected with the T option on the menu. If [Sys]<Sys>-WSnnn>SysImage.Sys cannot be found, the default System Image file [Sys]<Sys>WS>SysImage.Sys is loaded. 2. the cluster communications cables or 3. the CPU Board.
B4	Bad checksum of System Image. The System Image transferred from the master workstation is not a valid run file. Either the file is invalid, or the transmission was faulty or incomplete. Check: 1. whether the Operating System of the cluster workstation is invalid, 2. the CPU Board (7201 or cluster communications logic), or 3. whether the communications input/output processor of the master workstation has crashed.

Communications Errors

Error Code	Message/Meaning/Possible Causes
B5	Read error. Excessive input/output errors occurred while the bootstrap interface block was being read. Check: 1. the CPU Board (7201 or cluster communications logic), or 2. the cluster communications cables.
B6	Read timeout. During a read operation, no response was received from the master workstation. Check: the Operating System of the master workstation, which may have crashed.
B7	Write DMA count is bad. After completion of a write operation, the bootstrap ROM determined that the entire block was not sent. Check: the CPU Board (7201 or 8257).
B8	Write timeout. A write operation did not properly complete. Check: the CPU Board (7201, 8257, or 8253).
B9	Bad bootstrap block format. A bootstrap block of an invalid length was received. Check: whether the format of the bootstrap file is correct.

Communications Errors

Error Code	Message/Meaning/Possible Causes
BA	DMA error. After initializing the DMA channel for a Read or Write operation, the 8257 DMA controller did not contain the same information that was written to it. Check: the CPU Board (8257).
BB to CF	Unused

ROM/RAM Hardware Tests

E0	ROM checksum error. There is a bad ROM chip on the CPU Board at device location 3H. This error is displayed on the keyboard LEDs, not the video display (see "Interpreting Keyboard Error Codes," above).
E1	RAM error. An error occurred during initialization of the bootstrap ROM work area. This error is displayed on the keyboard LEDs, not the video display (see "Interpreting Keyboard Error Codes," above). Check: the CPU Board.

Error Code	Message/Meaning/Possible Causes
E2	RAM read and write 0's error.
E3	RAM read and write 1's error.
E4	RAM read and write address error.

An error occurred during the read and write RAM test. All 1's, all 0's, or the sum of DS and DI are written, read, and compared. The comparison showed that the DS and DI were not identical. The error display for E2, E3, E4, and E5 (below) is:

```
E: E2
1000:675C 0000 0002
```

where

E: E2	is the error code,
1000:675C	is the hexadecimal address,
0000	is the expected value, and
0002	is the received value.

Check: that the CPU Board is correctly seated on the Motherboard.

E5 RAM address test error.

An error occurred during the RAM addressing test. After completion of the RAM read/write address test, each RAM word should contain the sum of its own DS and DI. The RAM address test verifies that this is true. This error can be caused by a short or an always low address line allowing different addresses to be written to the same RAM. It may also be caused by memory that picks up or drops bits when idle.

Check: that the CPU Board is correctly seated on the Motherboard.

E6 Keyboard initialization error.

An error occurred while the bootstrap ROM was initializing the hardware.

E7 to EF Unused

The F0-F9 errors are generated by the communications test (menu option C). They indicate problems with the cluster communications and DMA logic or that the cluster cable was still connected to the workstation when the test was started.

Error Code	Message/Meaning/Possible Causes
F0	Underrun transfer ready not set. Status bits transmit underrun and/or transmit buffer empty were not set after a reset.
F1	CTS and/or DCD set. The status bits CTS and DCD were not set after the transmitter was enabled.
F2	Carrier not clear. DCD did not clear after the transmitter was disabled.
F3	DMA write receive not ready. A character was written using DMA to the transmit buffer, but no character was received in the receive buffer.
F4	DMA write data error. A character was written using DMA to the transmit buffer. The character received in the receive buffer does not match the one written.
F5	DMA write data error bits. A frame was written using DMA to the transmit buffer. Though all characters within the frame were received correctly, no end of frame (EOF) character was received in the receive file. This usually indicates a chip failure.

Error Code	Message/Meaning/Possible Causes
F6	Timeout waiting for DMA read ready. A character was written using programmed input/output to the transmit buffer, but no character was received in the receive buffer.
F7	DMA read EOF not set. A frame was written using programmed input/output to the transmit buffer. Though all characters within the frame were received correctly, no end of frame (EOF) character was received in the receive file. This usually indicates a chip failure.
F8	DMA read data error. A character was written using programmed input/ouput to the transmit buffer. The character received in the receive buffer does not match the one written.
F9	Carrier set after DISC. The DCD is still set. The most probable cause of the problem is the cluster communications cable. Check: 1. whether the cluster communications cable is disconnected from the workstation, or 2. the CPU Board.
FA to FF	Unused

DIRECT MEMORY ACCESS

The Direct Memory Access (DMA) channels on the CPU Board ensure high-speed input/output data transfers without relying on the CPU to perform these functions.

An Intel 8257 DMA controller chip provides four high-speed DMA channels, three of which are usable on the AWS workstations. The priority and assignment of the DMA channels on the CPU Board are:

Priority	Channel	Use
High	0	Shared by Disk Controller and advanced video boards
Middle	1	Cluster Communications
Low	2	Video Display Refresh
---	3	Auto-initialization of the Video Display Refresh parameters.

The only purpose of DMA Channel 3 is to auto-initialize DMA Channel 2. That is, when the Channel 2 DMA count is decremented to 0, the address and count registers are reloaded from the Channel 3 registers.

A DMA operation involves the following basic steps:

1. The 8257 is programmed by the CPU to use a particular channel, that of either video display refresh or cluster communications. Programming involves setting registers (described below) for the data buffer address, transfer length, and transfer direction (to or from memory), and starting the appropriate channel.

2. The input/output device requiring a data transfer makes a device DMA request.

3. The 8257 asserts its HOLD+ (Hold Request) output to the CPU to request control of the address and data buses of the CPU.

4. The CPU responds by asserting its HDLA+ (Hold Acknowledge) output when it gives up the bus and tristates (isolates) its address, data, and most control lines.

5. The 8257 simultaneously drives the memory address and sends a device acknowledge strobe to the input/output device.

6. The 8257 generates the appropriate command strobes, either an input/output read and a memory write (if the transfer is from input/output to memory), or a memory read and an input/output write (if the transfer is from memory to the input/output device).

7. When the transfer is complete, the 8257 removes the device acknowledge and command strobes, and the address.

8. Finally, the 8257 drops its HOLD+ signal (which the CPU has continually monitored) and allows the CPU to continue processing.

Control and Status Registers

Port 8h

Port 8h is the Control and Status Register for the 8257. When writing to Port 8h, the user controls the setting of all DMA channels. It is necessary for any programs which enable or disable DMA for one channel to be aware of any activity on any other DMA channel.

Register AL Bit (CPU)	Read Information
0	Channel 0 reached a count of 0
1	Channel 1 reached a count of 0
2	Channel 2 reached a count of 0
3	Not used
4	This bit is 1 if Channel 2 has never auto-initialized but is programmed in the auto-initialize mode.
5	0
6	0
7	0

Register AL Bit (CPU)	Write Information
0	Starts Channel 0
1	Starts Channel 1
2	Starts Channel 2
3	Not used
4	If 1, this bit sets rotating priority between channels.
5	0
6	If 1, this bit stops DMA when the count is 0.
7	If 1, this bit starts the auto-initialize mode.

Address and Count Registers

Port 0

Port 0 contains the address for the disk controller and advanced video DMA channel. Since the address is two bytes, two transfers are required for the CPU to read or write it. The first transfer is the low-order byte of the address; the second is the high-order byte.

Register AL Bit (CPU)	Read or Write Information (1st/2nd Transfer)
0	0/8
1	1/9
2	2/A
3	3/B
4	4/C
5	5/D
6	6/E
7	7/F

Port 1h

Port 1h contains the count and transfer direction for the disk controller and advanced video DMA channel. Since the count and direction data are two bytes, two transfers are required for the CPU to read or write them. The first transfer is the low-order byte of the count; the second is the high-order six bits of the count and the two direction bits.

Register AL Bit (CPU)	Read or Write Information (1st/2nd Transfer)
0	0/8
1	1/9
2	2/A
3	3/B
4	4/C
5	5/D
6	6/Memory Write DMA
7	7/Memory Read DMA

Port 2h

Port 2h contains the address for the cluster communications DMA channel. Since the address is two bytes, two transfers are required for the CPU to read or write it. The first transfer is the low-order byte of the address; the second is the high-order byte.

Register AL Bit (CPU)	Read or Write Information (1st/2nd Transfer)
0	0/8
1	1/9
2	2/A
3	3/B
4	4/C
5	5/D
6	6/E
7	7/F

Port 3h

Port 3h contains the count and transfer direction for the cluster communications' DMA channel. Since the count and direction data are combined into two bytes, two transfers are required for the CPU to read or write them. The first transfer is the low-order byte of the count; the second is the high-order six bits of the count and the two direction bits.

Register AL Bit (CPU)	Read or Write Information (1st/2nd Transfer)
0	0/8
1	1/9
2	2/A
3	3/B
4	4/C
5	5/D
6	6/Memory Write DMA
7	7/Memory Read DMA

Port 4h

Port 4h contains the current address for the video display refresh DMA channel. Since the address is two bytes, two transfers are required for the CPU to read or write it. The first transfer is the low-order byte of the address; the second is the high-order byte.

Register AL Bit (CPU)	Read or Write Information (1st/2nd Transfer)
0	0/8
1	1/9
2	2/A
3	3/B
4	4/C
5	5/D
6	6/E
7	7/F

Port 5h

Port 5h contains the current count and transfer direction for the video display refresh DMA channel. Since the count and direction data are combined into two bytes, two transfers are required for the CPU to read or write them. The first transfer is the low-order byte of the count; the second transfer is the high-order six bits of the count and two direction bits.

Register AL Bit (CPU)	Read or Write Information (1st/2nd Transfer)
0	0/8
1	1/9
2	2/A
3	3/B
4	4/C
5	5/D
6	6/Memory Write DMA
7	7/Memory Read DMA

Port 6h

Port 6h contains the initial address for the video display refresh DMA channel. Since the address is two bytes, two transfers are required for the CPU to read or write it. The first transfer is the low-order byte of the address; the second is the high-order byte.

Register AL Bit (CPU)	Read or Write Information (1st/2nd Transfer)
0	0/8
1	1/9
2	2/A
3	3/B
4	4/C
5	5/D
6	6/E
7	7/F

Port 7h

Port 7h contains the initial count and transfer direction for the video display refresh DMA channel. Since the count and direction data are two bytes, two transfers are required for the CPU to read or write them. The first transfer is the low-order byte of the count; the second is the high-order six bits of the count and two direction bits.

Register AL Bit (CPU)	Read or Write Information (1st/2nd Transfer)
0	0/8
1	1/9
2	2/A
3	3/B
4	4/C
5	5/D
6	6/Memory Write DMA
7	7/Memory Read DMA

CLUSTER COMMUNICATIONS

Cluster communications are handled by an NEC 7201 (or Intel 8274) MPSC (Multi-Protocol Serial Controller) chip. The MPSC contains two serial channels: A and B. Channel A is used only for cluster communications. Channel B is used for communications between the keyboard and the CPU. While Channel B is similar in operation to Channel A, it is programmed in a completely different manner. For a discussion of Channel B and an example of how it is programmed, see "Keyboard and Keyboard Communications" below.

Under control of Channel 1 of the 8257, Channel A of the 7201 transfers data at speeds of up to 410 kilobaud on the half-duplex, multidrop, RS-422 cluster communications line. The communications protocol used by Convergent software is a variant of Advanced Data Communications Control Procedures (ADCCP), much of which is handled directly by the 7201. Since Channel A is multidrop (that is, the same lines can be driven by any one of several transmitting workstations), the Channel A Request to Send signal is used to ensure that only the transmitting workstation drives the communications lines.

Preparing Channel A for operation involves three steps:

1. Several write registers in the 7201 must be programmed to perform the operation (see Figure 2-5, the "7201 Programming Example" below).

2. The baud rate must be selected by programming the 8253 counter/timer.

3. DMA Channel 1 must be programmed to handle cluster communications. DMA programming is discussed above in "Direct Memory Access."

Control and Status Registers

Channel A is programmed using three input/output ports:

Port	Use
60h	Channel A data (cluster data)
62h	Channel A commands/status
66h	Write Register 2 only

Channel A has a set of three status (read) registers and eight command (write) registers. The CPU transfers information to and from these registers by input/output Port 62h. Port 66h is used by both Channels A and B to store the interrupt vector. The Pointer Register in the 7201 selects which read or write register is accessed when Ports 62h and 66h are used. When either a manual or power-up reset occurs, the Pointer Register is set to 0. Any read or write to Ports 62h or 66h then accesses Read Register 0 or Write Register 0, respectively. The Pointer Register is programmed when Write Register 0 is written to. The Pointer Register is reset to 0 after any command or status access is made to a read or write register other than 0.

For example, to access Read Register 2, a 2 is written to Write Register 0. The next read accesses Read Register 2. Figure 2-4 shows the register hierarchy.

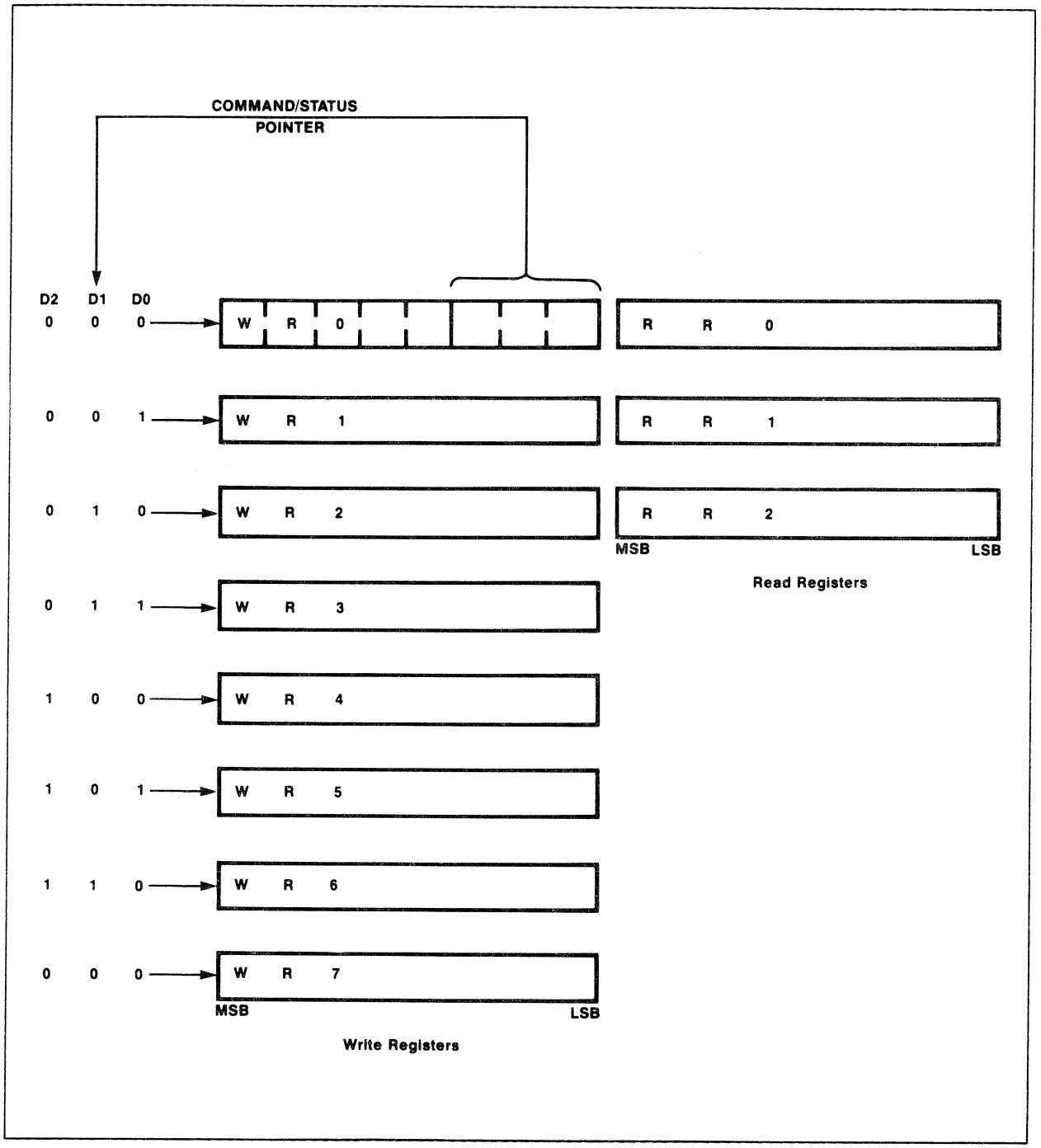


Figure 2-4. 7201 Register Hierarchy.

READ REGISTER 0 (PORT 62h STATUS)

Register AL Bit (CPU)	Read Information
0	Receive character available
1	Interrupt pending
2	Transmit buffer empty
3	Carrier detect
4	Synchronize/Hunt
5	Clear to send
6	Transmit underrun/End of message
7	Break/Terminate

READ REGISTER 1 (PORT 62h STATUS)

Register AL Bit (CPU)	Read Information
0	All sent
1-3	Residue code
4	Parity error
5	Receive overrun
6	CRC/Framing error
7	End of frame

READ REGISTER 2 (PORT 62h STATUS)

Register AL Bit (CPU)	Read Information
0	Present interrupt vector (least significant bit)
1-6	Present interrupt vector
7	Present interrupt vector (most significant bit)

WRITE REGISTER 0 (PORT 62h COMMAND)

Register AL Bit (CPU)	Write Information
0-2	Pointer Register (see below)
3-5	Command code (see below)
6-7	CRC control (see below)

Pointer Register

AL2	AL1	AL0	Register to be Accessed
0	0	0	Read/Write Register 0
0	0	1	Read/Write Register 1
0	1	0	Read/Write Register 2
0	1	1	Write Register 3
1	0	0	Write Register 4
1	0	1	Write Register 5
1	1	0	Write Register 6
1	1	1	Write Register 7

Command Code

AL5	AL4	AL3	Command
0	0	0	Null command
0	0	1	Send terminate
0	1	0	Reset external/status interrupts
0	1	1	Channel reset
1	0	0	Enable interrupt on next receive
1	0	1	Reset transmit interrupt/DMA pending
1	1	0	Error reset
1	1	1	End of interrupt

CRC Control

AL7	AL6	Action
0	0	External interrupt enable
0	1	Reset receive CRC checker
1	0	Reset receive CRC generator
1	1	Reset underrun/EOM latch

WRITE REGISTER 1 (PORT 62h COMMAND)

Register AL Bit (CPU)	Write Information
0	External interrupt enable
1	Transmit interrupt/DMA enable
2	0 = fixed vector (Channel B only)
3-4	Interrupt control (see below)
5	Wait on receive
6	Must be 0
7	Wait enable

Interrupt Control

AL7	AL6	Command
0	0	Receive interrupt/DMA enable
0	1	Receive interrupt on first character or special condition
1	0	Interrupt on all receive characters or special conditions; parity affects vector.
1	1	Interrupt on all receive characters or special conditions; parity does not affect vector.

WRITE REGISTER 2 (PORT 62h COMMAND)

Command affects both channels.

Register AL Bit (CPU)	Write Information
0-1	Configuration code (see below)
2	Priority bit (see below)
3-5	Interrupt code (see below)
6	0
7	0

Configuration Code

AL1	AL0	Action
0	0	DMA not used
0	1	Channel A DMA, Channel B interrupts
1	0	Both channels DMA
1	1	Invalid

Priority Bit

AL2	Interrupt Priorities (in decreasing order)
0	Receive Channel A Transmit Channel A Receive Channel B Transmit Channel B External status Channel A External status Channel B
1	Receive Channel A Receive Channel B Transmit Channel A Transmit Channel B External status Channel A External status Channel B

Interrupt Code

AL5	AL4	AL3	Interrupt Mode
0	X	X	Nonvectored
1	0	0	8085 mode 1
1	0	1	8085 mode 2
1	1	0	8088 mode

WRITE REGISTER 2 (Port 66h COMMAND)

Command affects both channels.

In the status-affects-vector mode, bits 0-2 of the vector are called base vector bits because they depend on the cause of the interrupt.

Register AL Bit (CPU)	Write Information
0	Base vector bit 0 (least significant bit)
1-6	Base vector bit 1-6
2	Base vector bit 7 (most significant bit)

WRITE REGISTER 3 (PORT 62h COMMAND)

Register AL Bit (CPU)	Write Information
0	Receive enable
1	Synchronization character load inhibit
2	Address search mode
3	Receive CRC enable
4	Enter hunt mode
5	Auto-enables
6-7	Length code (see below)

Length Code

AL7	AL6	Receive Character Length (bits)
0	0	5
0	1	7
1	0	6
1	1	8

WRITE REGISTER 4 (PORT 62h COMMAND)

Register AL Bit (CPU)	Write Information
0	Parity enable
1	Even parity
2-3	Synchronous/Asynchronous code (see below)
4-5	Synchronization type (see below)
6-7	Divisor code (see below)

Synchronous/Asynchronous Code

AL3	AL2	Transmission Mode Selected
0	0	Synchronous mode
0	1	1 stop bit
1	0	1 stop bit
1	1	2 stop bits

Synchronization Type

AL5	AL4	Synchronization Character Used
0	0	Character synchronous (1 character) mode
0	1	Character synchronous (2 character) mode
1	0	Bit protocol mode
1	1	External synchronization

Divisor Code		
AL7	AL6	8253 Clock Internal Divisor
0	0	1
0	1	16
1	0	32
1	1	64

WRITE REGISTER 5 (PORT 62h COMMAND)

Register AL Bit (CPU)	Write Information
0	Transmit CRC enable
1	Request to send
2	CRC select
3	Transmit enable
4	Send break
5-6	Length code (see below)
7	Data terminal ready

Length Code

AL6	AL5	Transmit Character Length (bits)
0	0	5
0	1	7
1	0	6
1	1	8

WRITE REGISTER 6 (PORT 62h COMMAND)

Address is in bit protocol mode, and synchronization character is in bit synchronous mode. This register must be programmed with either a secondary address (for a bit-synchronous address mark), or a synchronization character for the character synchronous mode.

WRITE REGISTER 7 (COMMAND)

Flag is in bit protocol mode, and second synchronization character is in bit synchronous mode. This register must be programmed with either a flag (75h) character for bit protocol mode, or a second synchronization character for character synchronous (two character) mode.

7201 Programming Example

Figure 2-5 below is a listing of the initialization sequence used for both Channels A and B of the 7201 on the CPU Board. The listing is annotated to show how registers used in Channels A and B are configured for cluster and keyboard communications, respectively. If more extensive information concerning the NEC 7201 (or Intel 8274) is required, see either the 1981 Catalog published by NEC Microcomputers, Inc., or the Component Data Catalog published by the Intel Corporation.

Baud Rate

The baud rate of data received on the cluster communications channel depends entirely on the rate at which the transmitting workstation is sending data. The limits to the clock speed are established by two factors: the upper limit that the 7201 accepts, and the lower limit that the carrier detector recognizes as a constant clock.

The carrier detector input of the 7201 is connected to a one-shot multivibrator triggered by the receive clock. The one-shot's output is asserted any time the clock has a rising edge. For the carrier detector to remain continuously asserted, the minimum clock rate is 100k baud. The maximum clock rate is 410k baud; this is a limitation of the 7201 when it is running with a 2.5-MHz system clock.

When the request-to-send line for Channel A is asserted, the CPU Board transmit clock is driven onto the clock line of the cluster. The frequency of the transmit clock is determined by the divisor that is programmed into Counter 1 of the 8253. The 8253 should be programmed in Mode 3 (square wave) as follows:

1. write 76h to Port 46h,

2. write the low-order byte of the divisor to Port 42h, and

3. write the high-order byte of the divisor to Port 42h.

```
Location   Object    Line      Source          Comments

                      1
                      2
                      3
                      4
                      5
                      6
                      7        PUBLIC  Init7201
                      8
                      9        InitDevCode  SEGMENT PUBLIC 'COED'
                     10        ASSUME  CS: InitDevCode
0000                 11
                     12        Init7201  PROC FAR
                     13
                     14
                     15
                     16 +1
0000       B01B      17 +1     mov   al, 18h
0002       E662      18 +1     out   62h, al     Channel A reset.
0004       90        19 +1     nop
0005       90        20 +1     nop
0006       90        21 +1     nop
0007       90        22 +1     nop
0008       B018      23 +1     mov   al, 18h
000A       E662      24 +1     out   62h, al     Channel A reset.
000C       90        25 +1     nop
000D       90        26 +1     nop
000E       90        27 +1     nop
000F       90        28 +1     nop
                     29 +1
                     30 +1
0010       B004      31 +2     mov   al, 04h
0012       E662      32 +1     out   62h, al     Select Port 62h,
                                                   Write Register 4.
0014       B020      33 +2     mov   al, 20h
0016       E662      34 +1     out   62h, al     Select bit
                                                   protocol mode.
                                                   All other bits 0.
                     35 +1
                     36 +1
0018       B001      37 +2     mov   al, 01h
001A       E662      38 +1     out   62h, al     Select Port 62h,
                                                   Write Register 1.
001C       B000      39 +2     mov   al, 00h
0016       E662      40 +1     out   62h, al     All bits 0.
                     41 +1
                     42 +1
```

Figure 2-5. 7201 Programming Example. (Page 1 of 3)

```
Location  Object  Line     Source              Comments
0020      B002    43 +2    mov   al, 02h
0022      E662    44 +1    out   62h, al       Select Port 62h,
                                                Write Register 2.
0024      B031    45 +2    mov   al, 31h
0026      E662    46 +1    out   62h, al       Channel A DMA,
                                                Channel B
                                                interrupts; 8088
                                                interrupt mode;
                                                priority Channel A
                                                over Channel B.
                                                All other bits 0.
                  47 +1
                  48 +1
0028      B003    49 +2    mov   al, 03h
002A      E662    50 +1    out   62h, al       Select Port 62h,
                                                Write Register 3.
002C      B000    51 +2    mov   al, 00h
002E      E662    52 +1    out   62h, al       All bits 0.
                  53 +1
                  54 +1
0030      B005    55 +2    mov   al, 05h
0032      E662    56 +1    out   62h, al       Select Port 62h,
                                                Write Register 5.
0034      B000    57 +2    mov   al, 00h
0036      E662    58 +1    out   62h, al       All bits 0.
                  59 +1
                  60 +1
0038      B018    61 +1    mov   al, 18h
003A      E666    62 +1    out   66h, al       Channel B reset.
003C      90      63 +1    nop
003D      90      64 +1    nop
003E      90      65 +1    nop
003F      90      66 +1    nop
0040      B018    67 +1    mov   al, 18h
0042      E666    68 +1    out   66h, al       Channel B reset.
0044      90      69 +1    nop
0045      90      70 +1    nop
0046      90      71 +1    nop
0047      90      72 +1    nop
                  73 +1
                  74 +1
0048      B004    75 +2    mov   al, 04h
004A      E666    76 +1    out   66h, al       Select Port 66h,
                                                Write Register 4.
```

Figure 2-5. 7201 Programming Example. (Page 2 of 3)

```
Location   Object   Line      Source              Comments

004C       B0C4     77 +2     mov   al, C4h
004E       E666     78 +1     out   66h, al       Asynchronous, 1
                                                  stop bit; 8 bits;
                                                  divisor code, 64.
                                                  All other bits 0.
                    80 +1
0050       B003     81 +2     mov   al, 03h
0052       E666     82 +1     out   66h, al       Select Port 66h,
                                                  Write Register 3.
0054       B0C1     83 +2     mov   al, C1h
0056       E666     84 +1     out   66h, al       Length code, 8
                                                  bits; receive
                                                  enable.  All other
                                                  bits 0.
                    85 +1
                    86 +1
0058       B001     87 +2     mov   al, 01h
005A       E666     88 +1     out   66h, al       Select Port 66h,
                                                  Write Register 1.
005C       B015     89 +2     mov   al, 15h
005E       E666     90 +1     out   66h, al       External interrupt
                                                  enable; no fixed
                                                  vector; interrupt
                                                  on all receive
                                                  characters or
                                                  special conditions
                                                  and parity affects
                                                  vector.  All other
                                                  bits 0.
                    91 +1
                    92 +1
0060       B002     93 +2     mov   al, 02h
0062       E666     94 +1     out   66h, al       Select Port 66h,
                                                  Write Register 2.
0064       B008     95 +2     mov   al, 08h
0066       E666     96 +1     out   66h, al       Base vector, 08h.
                    97 +1
                    98 +1
0068       B005     99 +1     mov   al, 05h
006A       E666    100 +1     out   66h, al       Select Port 66h,
                                                  Write Register 5.
006C       B068    101 +2     mov   al, 68h
006E       E666    102 +1     out   66h, al       Length code, 8
                                                  bits; transmit
                                                  enable.  All other
                                                  bits 0.
```

Figure 2-5. 7201 Programming Example. (Page 3 of 3)

The 8253 then generates the clock. The clock frequency input to Counter 1 of the 8253 is 1.23 MHz. For example, to set 307 kilobaud (Convergent's standard cluster frequency), use the following sequence:

1. write 76h to Port 46h,

2. write 4h to Port 42h, and

3. write 0 to Port 42h.

KEYBOARD AND KEYBOARD COMMUNICATIONS

The keyboard is housed in an enclosure separate from the mainframe enclosure. The keyboard enclosure contains the keys, an 8048 single-component microcomputer with related logic, and eight LEDs. The 8048 scans the keyboard, controls the LEDs, and functions as an asynchronous serial port. Channel B of the 7201 on the CPU Board communicates with the keyboard via a bidirectional serial link. Figure 2-6 shows the layout of the 98-key keyboard.

The keyboard communicates using an asynchronous protocol at approximately 1200 baud. Each time a key is pressed or released, the status of the key is sent to Channel B of the 7201 on the CPU Board. Channel B of the 7201 is interrupt-driven, as opposed to Channel A, which operates under DMA control. As shown in Figure 2-7, one 8-bit code is sent to Channel B for each key pressed. If no keys are pressed, the status consists of a special code (C0). The last code of the status sequence sent has the high-order bit set.

Channel B is programmed using three input/output ports:

Port	Use
62h	Write Register 2 only (used for controls common to both 7201 channels)
64h	Channel B data (keyboard data)
66h	Channel B commands/status

An example of an initialization sequence for Channel B of the 7201 is shown in Figure 2-5 in "Cluster Communications," above. For this example to apply to keyboard communications, substitute Port 66h for 62h.

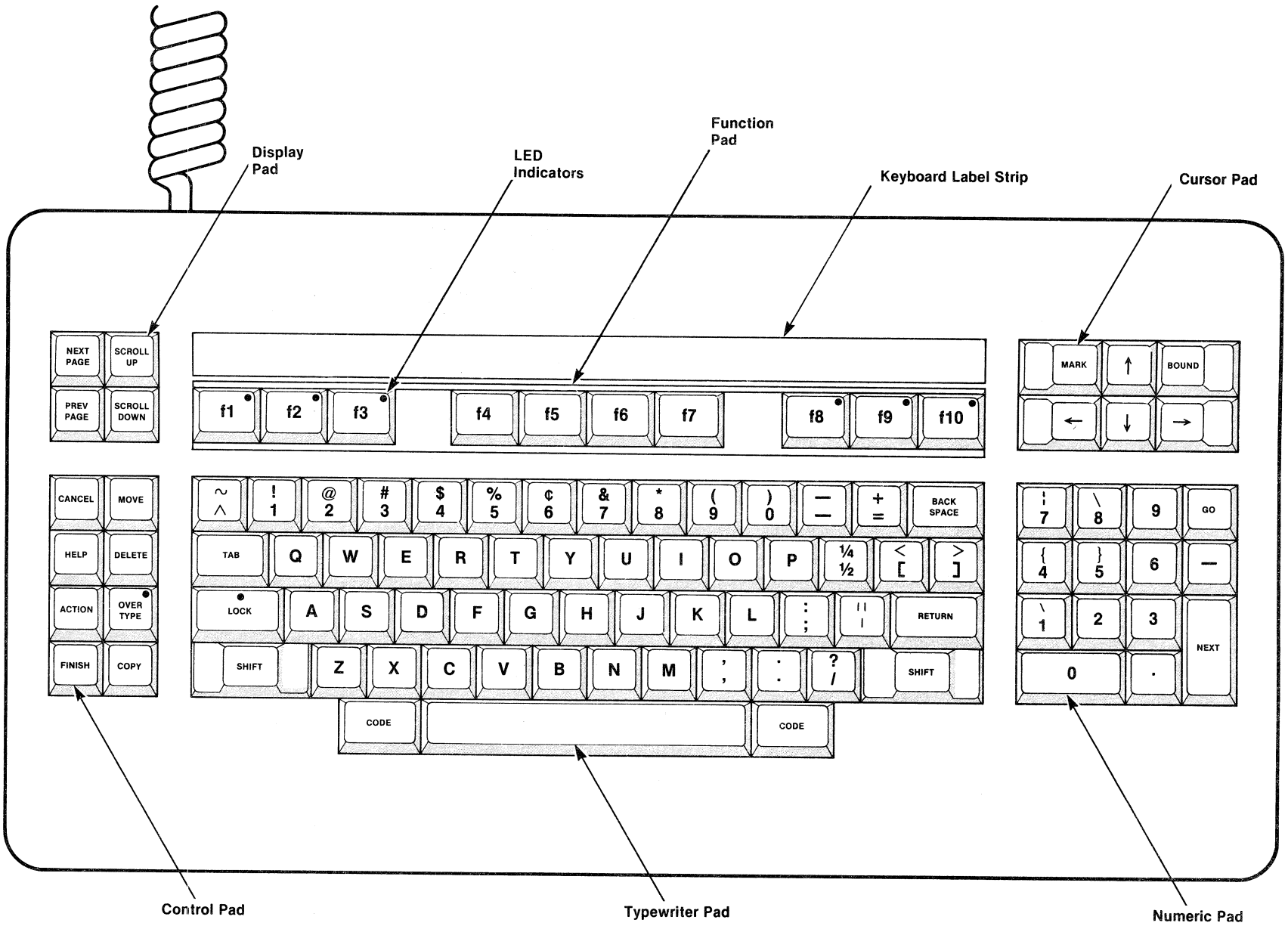


Figure 2-6. Keyboard.

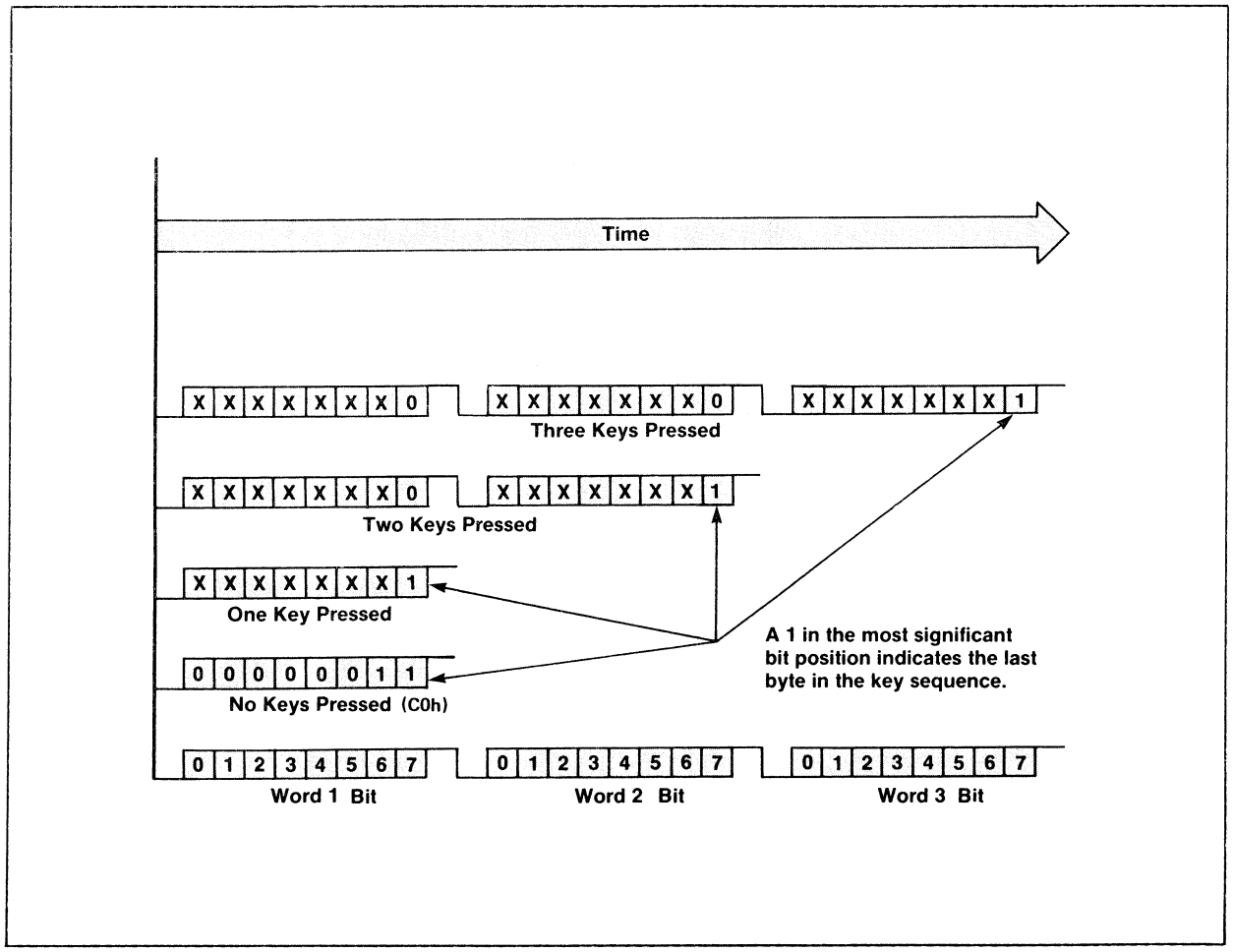


Figure 2-7. Data Format for Keyboard Output.

SPEAKER INTERFACE

The AWS-220, -230, and -240 are equipped with circuitry to generate alarm tones through a speaker. The frequency and duration of the generated tone are fully programmable.

Counter 0 of the 8253 is used to generate the tone. The input frequency to Counter 0 is 1.23 MHz. Programming the counter with an appropriate divisor results in a tone generated at the speaker.

The recommended sequence of commands for programming Counter 0 is:

1. write 36h to Port 46h,

2. write the low-order byte of the divisor to Port 40h, and

3. write the high-order byte of the divisor to Port 40h.

This sequence programs the specific mode that the 8253 operates in, and loads the two bytes of the divisor. Immediately, the tone is generated at the speaker.

To stop the tone, the mode is programmed again, but without the divisor:

write 36h to Port 46h.

To choose an appropriate divisor, first determine the desired tone frequency. An example is the standard Convergent audible alarm tone of 625 Hz. Next, divide the desired frequency into 1.23 MHz. The resulting divisor for this example is 1966 (decimal) or 7AEh. Therefore, program Counter 0 in the following sequence:

1. write 36h to Port 46h,

2. write AEh to Port 40h, and

3. write 07h to Port 40h.

CPU BOARD INTERRUPT CONTROLLER

All interrupts for input/output devices on the CPU Board are controlled by the 7201 on the CPU Board and the 8259A interrupt controller on either the FDC or the HDC Board (see "FDC and HDC Interrupt Controller" below). The 7201 provides a priority interrupt scheme. The priority is set in the 7201 Write Register 2 (Port 62h).

The only interrupt source on the CPU Board not related to either keyboard or cluster communications is Counter 2 of the 8253, which is used to generate general purpose interrupts for software. The output of Counter 2 is sent to the carrier detector pin of Channel B (the keyboard channel) of the 7201. Since the carrier detector pin is not used for the Channel B, Counter 2 of the 8253 can be used to generate an external/status interrupt in the 7201. The input frequency to Counter 2 is 76 kHz. Counter 2 is programmed in the following sequence:

1. write B0h to Port 46h (Mode 0),

2. write the low-order byte of the clock counts before interrupt, and

3. write the high-order byte of the clock counts before interrupt.

For example, to get an interrupt from Counter 2 in 1 ms, 76 counts (4Ch) are required. The programming sequence is:

1. write B0h to Port 46h,

2. write 4Ch to Port 44h, and

3. write 00 to Port 44h.

FDC AND HDC BOARD INTERRUPT CONTROLLER

Both the FDC and HDC Boards use an Intel 8259A programmable interrupt controller to service interrupts from the following five different input/output devices:

- o the CPU Board (via the 7201),
- o RS-232-C communications interface,
- o printer interface,
- o FDC or HDC Board 8253 Channel 0, and
- o the FDC or HDC Board disk controller.

Although interrupts from the CPU Board pass through the 8259A and are of the highest priority, their interrupt vectors still come from the 7201 on the CPU Board. The 8259A sends interrupt vectors to the CPU for the other interrupt sources, allows masking for individual interrupt levels, and has a priority scheme for inter-level arbitration and nesting. The interrupt level assignment is:

Level	Device
0	Unused
1	CPU Board
2	Unused
3	RS-232-C interface
4	Printer interface
5	8253 Counter 0
6	Disk controller
7	Unused

When an interrupt is requested from one or more of the input/output devices, the following events occur.

1. The input/output device requests an interrupt from the CPU when it asserts its corresponding 8259A input line.

2. The 8259A evaluates the interrupt requests and sends an INT+ (Interrupt) pulse to the CPU.

3. The CPU acknowledges the INT+ pulse by sending the first of two INTA- (Interrupt Acknowledge) pulses to the 8259A.

4. With the first INTA- pulse, the 8259A internally resolves the priority of the interrupting devices but does not drive an

interrupt vector onto the D0+-D7+ (Data Bus) lines.

5. The CPU sends the second INTA- pulse, which causes the 8259A to release the interrupt vector of the highest priority input/output device to the CPU on the BD0+-BD7+ lines.

6. At the end of the second INTA- pulse, the 8259A terminates the operation and resets the priority resolution circuitry for that interrupt. Lower priority interrupts are then serviced one at a time in the same manner.

Control and Status Registers

The 8259A must be programmed before it can be used. Up to four bytes of information called Initialization Command Words (ICWs) must be written to the 8259A before it can accept interrupt requests. After the ICWs are written, Operation Command Words (OCWs) can be written to the 8259A to select various interrupt modes. The following two input/output ports are used to perform these functions:

Port	Read Information	Write Information
A0h	Interrupt Status	Interrupt Control
A1h	Interrupt Mask	Interrupt Mask

Initialization Command Words

When the CPU addresses Port A0h and the D4+ data bit is high, two to four ICWs are written sequentially into the 8259A.

INITIALIZATION COMMAND WORD 1 (PORT A0h COMMAND)

Register AL Bit (CPU)	Write Information
0	ICW4. If 1, an ICW4 word is needed. If 0, ICW4 is not needed.
1	Single/cascade. Must be 0.
2	Call address interval. If 1, the inverrupt vector address interval is 4 bytes. If 0, the interrupt vector address interval is 8 bytes.
3	Trigger mode. If 1, the 8259A interrupt inputs are level-triggered. If 0, the 8259A interrupt inputs are edge-triggered.
4	Must be 1
5-7	Unused

INITIALIZATION COMMAND WORD 2 (PORT A1h COMMAND)

Register AL Bit (CPU)	Write Information
0-2	Unused
3-7	T3-T7 of the interrupt vector address

INITIALIZATION COMMAND WORD 3 (PORT Alh COMMAND)

Register AL Bit (CPU)	Write Information
0-7	For each bit in this byte, a 1 indicates that the corresponding 8259A interrupt input has a slave. Bit 1 is always 1; all others are always 0.

INITIALIZATION COMMAND WORD 4 (PORT A1h COMMAND)

Register AL Bit (CPU)	Write Information
0	Microprocessor mode. Must be 1.
1	End of interrupt mode (EOI). If 1, end of interrupt operation is automatic at the end of the last INTA- pulse. If 0, the CPU issues a command to the 8259A before the CPU returns from an interrupt service routine.
2	Master/remote. Must be 1.
3	Buffered mode. Must be 1.
4	Special fully nested mode. If 1, the special fully nested mode is used. If 0, the special fully nested mode is not used.
5-7	Unused

Operation Control Words

After the ICWs are written, the 8259A can accept interrupts from the five input/output devices listed above. Additionally, various modes of operation can be programmed into the 8259A through Operation Control Words (OCW1 through OCW3).

Note that the In-Service and Interrupt Request Registers can be read via the OCW3 Read Register bits. It is unnecessary to write a new OCW3 each time one of these registers is read, provided that the read bits correspond to the last ones received. The 8259A remembers which register was previously selected for a status read. In addition, the Interrupt Mask Register can be read whenever RD- is active and Port A0h is selected.

OPERATION CONTROL WORD 1 (PORT A1h COMMAND)

Register AL Bit (CPU)	Write Information
0-7	Each of these bits sets or clears a mask bit in the 8259A's Interrupt Mask Register. If a bit is 1, the corresponding channel is inhibited. If a bit is 0, the corresponding channel is enabled.

OPERATION CONTROL WORD 2 (PORT A0h COMMAND)

Register AL Bit (CPU)	Write Information
0-2	Interrupt level acted upon (0-7) when bit 6 of this word is 1
3-4	Unused
5-7	Rotate and end of interrupt modes (see below)

Rotate and End of Interrupt Modes

End of Interrupt:

AL7	AL6	AL5	Mode Selected
0	0	1	Nonspecific EOI command
0	1	1	Specific EOI command

Automatic Rotation:

AL7	AL6	AL5	Mode Selected
1	0	1	Rotate on nonspecific EOI command
1	0	0	Rotate in automatic EOI mode (set)
0	0	0	Rotate in automatic EOI mode (clear)

Specific Rotation:

AL7	AL6	AL5	Mode Selected
1	1	1	Rotate on specific EOI command (bits 0-2 of OCW4 are used)
1	1	0	Set priority command (bits 0-2 of OCW4 are used)
0	1	0	No operation

OPERATION CONTROL WORD 3 (PORT A0h COMMAND)

Register AL Bit (CPU)	Write Information
0-1	Read register command (see below)
2	Poll command. If 1, the CPU services the 8259A by polling it. If 0, 8259A interrupts the CPU when service is needed.
3	Unused
4	Unused
5-6	Special mask mode (see below)
7	Unused

Read Register Command

AL1	AL0	Read Register Selected
1	1	The In-Service Register on the next RD- (Read) pulse from the CPU
1	0	The Interrupt Request Register on the next RD- pulse from the CPU

Special Mask Mode

AL6	AL5	Mode Selected
1	1	Set special mask
1	0	Reset special mask

8253 COUNTER/TIMER

The Intel 8253 on the FDC and HDC Boards provides three fully programmable 16-bit counter/timer channels: one each for the two RS-232-C communications channels and one for a source of general purpose system interrupts.

The INT5- (Interrupt 5) output of Counter 0 is sent to an 8259A input. The outputs of Counter 1 and 2 are sent to the 7201 Channel B and A clock inputs, respectively, to supply internal clocks for asynchronous RS-232-C communications.

Control and Status Registers

The three counter/timer channels are programmed through the D0+-D7+ data lines. Three bytes of information must be written to each counter:

1. Mode Control Word,

2. low-order byte of the divisor, and

3. high-order byte of the divisor.

The Mode Control Word is written to each channel when the CPU writes to Port AFh.

MODE CONTROL WORD (PORT AFh COMMAND)

Register AL Bit (CPU)	Write Information
0	If 1, the counter counts in binary coded decimal. If 0, the counter operates as a binary counter.
1-3	Mode (see below)
4-5	Read/Load (see below)
6-7	Select counter (see below)

Mode

AL3	AL2	AL1	Mode Selected
0	0	0	0
0	0	1	1
X	1	0	2
X	1	1	3
1	0	0	4
1	0	1	5

Read/Load

AL5	AL4	Mode Selected
0	0	Counter latching operation
1	0	Read/Load most significant byte only
0	1	Read/Load least significant byte only
1	1	Read/Load least significant byte first, then most significant byte

Select Counter

AL7	AL6	Counter Selected
0	0	0
0	1	1
1	0	2
1	1	Unused

After the Mode Control Word is written, two divisor bytes are written to each of the three counters to select the counter rate. The divisor bytes work by dividing the counter input clock of 1.23 MHz by a selected number.

For example, if Counter 0 is to interrupt the CPU in 1 ms, 123 counts (98h) are required. The complete programming sequence for Counter 0 then is:

1. write 30h to Port AFh (Counter 0, Read/Load least then most significant divisor bytes, interrupt on terminal count, binary counter),

2. write 98h to Port ACh (least significant byte of divisor), and

3. write 00 to Port ACh (most significant byte of divisor).

The procedure for setting the baud rate for the RS-232-C communications ports is the same as that for counter 0 except that the CPU writes the divisor to input/output Ports ADh and AEh, respectively.

Assuming a required baud rate for RS-232-C Communications Port B of 1200, 1025 counts (401h) are required. The complete programming sequence is:

1. write 76h to Port AFh (Counter 1, Read/Load least then most significant divisor bytes, square wave, binary counter),

2. write 01h to Port ADh (least significant byte of divisor), and

3. write 04h to Port ADh (most significant byte of divisor).

Note that Counters 0, 1, and 2 can each be read independently by a CPU input instruction at any time without inhibiting the counter inputs.

RS-232-C COMMUNICATIONS

An NEC 7201 (or Intel 8274) Multi-Protocol Serial Controller (MPSC) chip on the FDC and HDC Boards provides two RS-232-C communications ports. The 7201 can operate in bit synchronous, byte synchronous, or asynchronous modes at baud rates from 50 to 19.2 kilobaud. The 7201 is interrupt controlled through the 8259A to the CPU on the CPU Board. The 7201 on the FDC or HDC Board is programmed in exactly the same manner as the 7201 on the CPU Board.

Each RS-232-C communications port is accessed through a 25-pin D-type connector on the back panel of the workstation. Both ports have the same function as Port B in the IWS workstation, and operate as Data Terminal Equipment for direct connection to a modem. The RS-232-C communications ports can connect to other types of Data Terminal Equipment with the appropriate cable and connectors (see "RS-232-C Communications Interface" in the "External Interfaces" section, below).

The following signals to and from the modem are supported:

- Transmit Data (to modem)
- Secondary Transmit Data (to modem)
- Request to Send (to modem)
- Data Terminal Ready (to modem)

- Receive Data (from modem)
- Secondary Receive Data (from modem)
- Clear to Send (from modem)
- Data Set Ready (from modem)
- Carrier Detect (from modem)
- Ring Indicator (from modem)

- External Transmit Clock (from modem)
- External Receive Clock (from modem)

Control and Status Registers

Each of the two RS-232-C communications ports is programmed using the following input/output ports:

Port	Device	Read	Write
A8h	7201	Port A data	Port A data
A9h	7201	Port A status	Port A command
AAh	7201	Port B data	Port B data
ABh	7201	Port B status	Port B command
ADh	8253	Port B baud rate	Port B baud rate
AEh	8253	Port A baud rate	Port A baud rate
AFh	8253	8253 mode	---
A4h	General	Extended Status Register (communications)	Extended Control Register

Ports A8h and AAh

Ports A8h and AAh are the Data Registers for RS-232-C Ports A and B, respectively. Ports A8h and AAh can be either read from or written to when the RS-232-C port is receiving or transmitting data, respectively.

Register AL Bit (CPU)	Read Information
0-7	Receive data bits 0-7

Register AL Bit (CPU)	Write Information
0-7	Transmit data bits 0-7

Ports A9h and ABh

Each of the two RS-232-C communications ports has a set of three status (read) registers and eight command (write) registers. The CPU transfers information to and from these registers by input/output Ports A9h (for RS-232-C Port A) and ABh for RS-232-C Port B). Since the 7201 uses the 8259A to send an interrupt vector to the CPU, Port ABh Write Register 2 of the 7201 is not used. The Pointer Register bits (in Write Register 0) at Ports A9h and ABh selects which read or write register is accessed when Ports A9h or ABh are used. When either a manual or power-up reset occurs, the Pointer Register is set to 0. Any read or write to Ports A9h and ABh then accesses Read Register 0 or Write Register 0,

respectively. The Pointer Register bits are programmed when Write Register 0 is written to. The Pointer Register bits are reset to 0 after any command or status access is made to a read or write register other than 0.

For example, to access Read Register 2, a 2 is written as the Pointer Register code to Write Register 0. The next read accesses Read Register 2. The hierarchy of registers in the 7201 is shown in Figure 2-4, above. The register format for the 7201 on the FDC or HDC Board is identical to that for the 7201 on the CPU Board. The format of the registers is given under "Cluster Communications Control and Status Registers," above.

Ports ADh, AEh, and AFh

Ports ADh, AEh, and AFh, used for setting the baud rate for RS-232-C Ports A and B and the counter mode, are described under "8253 Counter/Timer," above.

Port A4h

Port A4h, the Extended Control and Status Port, is used to provide several communications signals not directly supported by the 7201. The Extended Control Register is shared by the floppy disk controller on the FDC Board. Any programs which access this register must account for the state of bits 2, 3, and 7.

EXTENDED CONTROL REGISTER (PORT A4h)

Register AL Bit (CPU)	Write Information
0	Secondary Transmit Data (Channel B)
1	Secondary Transmit Data (Channel A)
2-3	Used by the floppy disk controller. These bits can be 1 or 0.
4	Channel B synchronous (external clocking)
5	Channel A synchronous (external clocking)
6	Unused
7	Used by the floppy disk controller. These bits can be 1 or 0.

EXTENDED STATUS REGISTER (Port A4h)

Register AL Bit (CPU)	Read Information
0	Secondary Receive Data (Port B)
1	Data Set Ready (Port B)
2	Ring Indicator (Port B)
3	Secondary Transmit Data (Port B)
4	Secondary Receive Data (Port A)
5	Data Set Ready (Port A)
6	Ring Indicator (Port A)
7	Secondary Transmit Data (Port A)

7201 Programming Example

The initialization sequence used for each of the two RS-232-C communications ports is identical to that used for the cluster communications and keyboard 7201 on the CPU Board. Figure 2-5 under "Cluster Communications," above, shows an assembly language example for this purpose. For the example to apply to RS-232-C communications, substitute Port A9h for 62h and Port ABh for 66h.

PRINTER INTERFACE

The FDC and HDC Boards provide a Centronics-compatible printer interface similar to that of the IWS workstation.

The CPU communicates with the printer interface through input/output Port B0h. The CPU writes eight bits of data to Port B0h which sends the data to the printer along with the STROBE- (Character Strobe) handshake line to inform the printer that data are available. The CPU reads Port B0h to get a single handshake flip-flop status bit and three bits of other printer status information.

The printer interface supports printers with and without storage buffers. After the CTOS Operating System writes a character to Port B0h, it reads B0h to test the BUFBUSY+ (Buffer Busy) handshake line. If BUFBUSY+ is low, another character can be sent.

PRINTER CONTROL DATA (Port B0h)

Register AL Bit (CPU)	Write Information
0-7	Printer data bits 0-7

PRINTER STATUS (PORT B0h)

Register AL Bit (CPU)	Read Information
0	LPTBUSY+ (Line Printer Busy). If 1, the printer is either printing or making some other mechanical movement.
1	SELECT+ (Printer Selected). If 1, the printer is online and ready to receive data.
2	BUFBUSY+ (Buffer Busy). If 1, this handshake line indicates that the printer has not yet acknowledged a character. If 0, the printer is waiting for another character to be sent.
3	NOPAPER+ (No Paper). If 1, the printer is out of paper. Note that not all Centronics-compatible printers use the NOPAPER+ status bit.
4-7	Unused

AWS-220 AND -230 FLOPPY DISK CONTROLLER

The floppy disk controller on the FDC Board controls one or two, single- or double-sided floppy disk drive(s), having 96 tracks per inch. A Modified Frequency Modulation (MFM) encoding technique is used to write double density data in 256-byte data sectors on the floppy disks.

An Intel 8272 (or NEC uPD 765) is used to control the floppy disk drives and transfer data to and from the RAM of the AWS-220 and -230 through DMA Channel 0 on the CPU Board. The 8272 also works in an interrupt controlled mode through the 8259A on the FDC Board when performing certain commands and for ready/not-ready status changes. The Extended Address Register provides four high-order address bits, which are used when the DMA address is programmed by the CPU. This allows the disk data buffer to be in any 64-kilobyte block of RAM on the CPU Board.

Read and Write Operations

A typical read or write operation to or from a floppy disk drive follows these basic steps:

1. DMA Channel 0 of the 8257 is programmed by the CPU at input/output Ports 8h, 0, and 1h for the data buffer address, transfer length, and transfer direction (to or from memory).

2. The Extended Address Register at Port B4h is loaded with the upper four bits of the disk data buffer address (LA10+-LA13+) and DMA Channel 0 is started (see "Direct Memory Access" above).

3. The CPU starts the motor of the appropriate floppy disk drive through bits in the Extended Control Register at Port A4h.

4. The CPU sends a write or read command (nine bytes) to the 8272 through Port 81h. After writing each command byte, the CPU reads the 8272's Main Status Register at Port 80h to determine when the 8272 can accept another byte.

5. When the last command byte is written to the 8272's Command Register, the read or write

operation begins when the 8272 sends a DREQ+ (DMA Request) pulse to the 8257.

6. The 8257 acknowledges the 8272's DMA request by pulsing DMACK- (DMA Acknowledge). The 8257 then requests the address and data buses from the CPU, generates the appropriate command strobes, and transfers data from RAM to the 8272 (write operation) or from the 8272 to RAM (read operation). Each time the 8272 is ready to accept another byte (or each time it has a byte to send), it must pulse the DREQ+ line.

7. During the transfer of the last byte, the 8257 asserts TC+ (Terminal Count) to the 8272 to terminate the operation.

8. When the transfer is complete, the 8272 generates an interrupt to the CPU and the 8257 returns control of the data and address buses to the CPU.

9. The CPU addresses the Main Status Register at Port 80h and other status registers at Port 81h to obtain status and housekeeping information.

Control Operations

Certain control operations, such as Seek and Recalibrate commands, do not use DMA Channel 0 since no data are being transferred. Instead, these operations result in an interrupt to the CPU when the operation is complete. The 8272 can operate in an interrupt driven mode for any command, but (in the case of read or write commands) it must interrupt the CPU for each byte transferred to or from RAM.

A typical control operation is executed in the following manner:

1. The CPU uses the Extended Control Register at Port A4h to start the motor of the floppy disk drive on which the operation is performed.

2. The CPU writes the appropriate command into the Command Register at input/output Port 80h.

3. For each command written to the 8272's Command Register (if the command is more than one byte), the 8272 pulses its INT6+ (Interrupt 6) line to the 8259A.

4. When the operation is complete, the 8272 again pulses INT6+ to the 8259A. The 8259 interrupts the CPU and supplies it with an interrupt vector during the CPU's interrupt acknowledge cycle.

5. If the command just executed requires that status registers in the 8272 be read, the CPU now performs the reads.

Control and Status Registers

There are four input/output ports associated with the floppy disk controller:

Port	Read Information	Write Information
80h	Floppy Main Status Register	---
81h	Floppy Status Registers 0-3/ data	Floppy commands/ /data
A4h	Unused with floppy disk controller	Extended Control Register
B4h	---	Extended Address Register

Port 80h

The CPU can read Port 80h anytime during the command or result phases of an operation. The DIO (Data Input/Output) and RQM (Request for Master) bits in the Main Status Register indicate to the CPU when data are ready and in which direction data will be transferred on the D0+-D7+ data bus.

Register AL Bit (CPU)	Read Information
0	If 1, floppy disk drive 0 is busy seeking a track.
1	If 1, floppy disk drive 0 is busy seeking a track.
2	Unused
3	Unused
4	Floppy disk controller busy. If 1, this bit indicates that the 8272 is in the execution phase of a read or write operation.
5	Non-DMA mode. If 1, the 8272 is not using Channel 0 of the 8257 to transfer data to or from memory.
6	Data input/output. If 1, the direction of data transfer is from the 8272 to the CPU. If 0, the direction is from the CPU to the 8272.
7	Request for master. If 1, the 8272 is either requesting another byte from the CPU or has a byte waiting for the CPU.

Port 81h

Port 81h is the command and status port for the floppy disk controller. When the CPU performs an output 81h instruction, it can write into the Command Register of the 8272. The AWS-220 and -230 use 9 of the 8272's 15 possible commands. A description of the commands used is in Table 2-1. The command mnemonics for the commands are listed in Table 2-2 below.

Commands. Commands for the 8272 have three distinct phases: command, execution, and result.

During the command phase, the 8272 receives all the information from the CPU that it requires to perform a particular operation. After each command byte transfer into the Command Register (if a multiple byte command is used), the CPU must read the Main Status Register to know when to transfer another byte. During the command phase, bits 6 and 7 of the Main Status Register must be 0 and 1, respectively.

During the execution phase, the 8272 performs the operation; the Main Status Register is not read. The execution phase ends when the 8272 receives a TC+ (Terminal Count) signal during the last byte of the data transfer.

During the result phase, all of the bytes in the command table for that command must be read. The Read Data command, for example, has seven bytes which must be read before the 8272 can accept another command. The CPU must issue seven consecutive read commands to complete the result phase.

Register AL Bit (CPU)	Write Information
0-7	Command bits 0-7

Status. Four status registers are available to the CPU when it performs an input 81h instruction (but only during the result phase of an operation). Only one of the status registers is presented to the CPU at a time. That is, if Status Register 0 is read, the next successive input 81h instruction will access Status Register 1 and so on until Status Register 3 is read. The particular command given to the 8272 during the command phase determines how many of the four status registers are read during the result phase.

Table 2-1. 8272 Commands. (Page 1 of 5)

READ DATA

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	MT	MFM	SK	0	0	1	1	0	Command codes
	0	0	0	0	0	HDS	DS1	DS0	
	◄---------- C ----------►								Sector identification information
	◄---------- H ----------►								
	◄---------- R ----------►								
	◄---------- N ----------►								
	◄---------- EON ----------►								
	◄---------- GPL ----------►								
	◄---------- DTL ----------►								
Execution:									Data transfer between the floppy disk drive and the RAM
Result:									
	◄---------- ST 0 ----------►								Status formation after command execution
	◄---------- ST 1 ----------►								
	◄---------- C ----------►								Sector identification information after command execution
	◄---------- H ----------►								
	◄---------- R ----------►								
	◄---------- N ----------►								

Table 2-1. 8272 Commands. (Page 2 of 5)

READ A TRACK

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	0	MFM	SK	0	0	0	1	0	Command codes
	0	0	0	0	0	HDS	DS1	DS0	
	◄---------- C ----------►								Sector identification information
	◄---------- H ----------►								
	◄---------- R ----------►								
	◄---------- N ----------►								
	◄---------- EOT ----------►								
	◄---------- GPL ----------►								
	◄---------- DTL ----------►								
Execution:									Data transfer between the floppy disk drive and RAM. This command reads all of the sectors contents from the index hole to the end of the track.
Result:									
	◄---------- ST 0 ----------►								Status information after command execution
	◄---------- ST 1 ----------►								
	◄---------- ST 2 ----------►								
	◄---------- C ----------►								Sector identification information after command execution
	◄---------- H ----------►								
	◄---------- R ----------►								
	◄---------- N ----------►								

Table 2-1. 8272 Commands. (Page 3 of 5)

WRITE DATA

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	MT	MFM	0	0	0	1	0	1	Command codes
	0	0	0	0	0	HDS	DS1	DS0	
	◄---------- C ----------►								Sector identification information
	◄---------- H ----------►								
	◄---------- R ----------►								
	◄---------- N ----------►								
	◄---------- EOT ----------►								
	◄---------- GPL ----------►								
	◄---------- DTL ----------►								
Execution:									Data transfer between the CPU Board and the floppy disk drive
Result:									
	◄---------- ST 0 ----------►								Status information after command execution
	◄---------- ST 1 ----------►								
	◄---------- ST 2 ----------►								
	◄---------- C ----------►								Sector identification information after command execution
	◄---------- H ----------►								
	◄---------- R ----------►								
	◄---------- N ----------►								

Table 2-1. 8272 Commands. (Page 4 of 5)

FORMAT A TRACK

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	0	MFM	0	0	1	1	0	1	Command codes
	0	0	0	0	0	HDS	DS1	DS0	
	◄---------- C ----------►								Bytes/Sector
	◄---------- SC ----------►								Sectors/Track
	◄---------- GPL ----------►								Gap 3
	◄---------- D ----------►								Filler byte
Execution:									8272 formats entire track
Result:									
	◄---------- ST 0 ----------►								Status
	◄---------- ST 1 ----------►								information
	◄---------- ST 2 ----------►								after command execution
	◄---------- C ----------►								Identification
	◄---------- H ----------►								information
	◄---------- R ----------►								has no meaning
	◄---------- N ----------►								

Table 2-1. 8272 Commands. (Page 5 of 5)

RECALIBRATE

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	0	0	0	0	0	1	1	1	Command codes
	0	0	0	0	0	0	DS1	DS0	
Execution:									Head retracted to track 0

SENSE INTERRUPT STATUS

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command	0	0	0	0	1	0	1	0	Command Codes
Result:									
	◄---------- ST 0 ----------►								Status information about the floppy disk controller at the end of each Seek command
	◄---------- PCN ----------►								

SPECIFY

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	0	0	0	0	0	0	1	1	Command codes
	◄------ SRT ------►				◄----- HUT -----►				
	◄---------- HLT ----------►|				◄ ND ►			

Table 2-2. 8272 Command Mnemonics. (Page 1 of 3)

Symbol	Name	Description
C	Cylinder number	C is the currently selected track (cylinder) number (0 through 76) of the floppy disk.
D	Data	D is the data pattern which is to be written in the sector.
D0-D7	Data bus	D7 is the most significant bit of the data bus; D0 is the least significant.
DS0-DS1	Drive select	DS is the selected drive number, either 0 or 1. Only DS0 is used.
DTL	Data length	When N is defined as 00, DTL is the length of data in a sector which is to be read from or written to.
EOT	End of track	EOT is the final sector number of a track.
GPL	Gap length	GPL is the length of gap 3 which is the spacing between sectors excluding the VCO (Voltage Controlled Oscillator) synchronization field.
H	Head address	H is the head number, 0 or 1, as specified in the identification field.
HDS	Head select	HDS is a selected head number, 0 or 1 (H = HDS in all command words).
HLT	Head load time	HLT is the head load time in the floppy disk drive and can be from 2 to 254 ms in 2-ms increments.

Table 2-2. 8272 Command Mnemonics. (Page 2 of 3)

Symbol	Name	Description
HUT	Head unload time	HUT is the head unload time after a read or write operation has occurred and can be from 16 to 240 ms in 16-ms increments.
MFM	MFM mode	This bit must be 1. It means that the MFM mode is selected.
MT	Multitrack	If MT is 1, a multitrack operation is performed. That is, a track under both HDO and HD1 is read or written.
N	Number	N is the number of data bytes written in a sector.
NCN	New cylinder number	NCN is the new track (cylinder) number that is to be reached as a result of a seek operation. This is the desired position of the read/write head.
ND	Non-DMA mode	If 1, the non-DMA mode is selected.
PCN	Present cylinder number	PCN is the cylinder number at the completion of the Sense Interrupt Status command. This is the present position of the read/write head.
R	Record	R is the sector number, where the operation will take place.
SC	Sector	SC is the number of sectors per track.
SK	Skip	SK is the skip deleted address mark.

Table 2-2. 8272 Command Mnemonics. (Page 3 of 3)

Symbol	Name	Description
SRT	Step Rate Time	SRT is the stepping rate for the floppy disk drive and can be 1 to 16 ms in 1-ms increments). The same stepping rate applies to all drives (Fh = 1 ms, Eh = 2 ms, etc.).
ST 0-3	Status 0-3	ST 0-3 are the four registers that store status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register. ST 0-3 can be read only after a command has been executed and contain information relevant to that particular command.

READ REGISTER 0 (PORT 81h STATUS)

Register AL Bit (CPU)	Read Information
0-1	US 0-1 (Unit Select 0 and 1). These bits indicate which drive was selected at the time of interrupt. Only the US 0 bit is used.
2	HD (Head Address). If 1, HD means that the head was on the first side of the floppy disk at the time of interrupt.
3	NR (Not Ready). When the floppy disk drive is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to side 1 of a single-sided drive, this flag is set.
4	EC (Equipment Check). If the 8272 receives a fault signal, or if the drive fails to find track 0 after 77 step pulses (the Recalibrate command), this bit is set.
5	SE (Seek End). When the floppy disk controller completes the Seek command, this bit is set to 1.
6-7	Interrupt code (see below).

Interrupt Code

AL7	AL6	Code meaning
0	0	Normal termination of command. The command was completed and properly executed.
0	1	Abnormal termination of command. Execution of command was started, but was not successfully completed.
1	0	Invalid command issue. The command was issued but never started.
1	1	Abnormal termination of command. During command execution, the ready signal from the floppy disk drive changed state.

READ REGISTER 1 (81h STATUS)

Register AL Bit (CPU)	Read Information
0	MA (Missing Address Mark). If the 8272 cannot detect the identificaiton address mark after encountering the index hole twice, this flag is set. Also, if the 8272 cannot detect the data address mark or deleted data address mark, this flag is set. At the same time in both instances, the MD bit of Status Register 2 is set.
1	NW (Not Writable). During the execution of a Write Data or Format a Track command, if the 8272 detects a write protect signal from the floppy disk drive, this bit is set.
2	ND (No Data). 1. During the execution of a Read Data or Scan command, if the 8272 cannot find the sector specified in the IDR Register, this flag is set. 2. During the execution of a Read a Track command, if the starting sector cannot be found, this bit is set.
3	Unused
4	OR (Over Run). If the 8272 is not serviced by the 8257 during a data transfer, this bit is set.

Register AL Bit (CPU)	Read Information
5	DE (Data Error). When the 8272 detects a CRC error in either the identification field or the data field, this bit is set.
6	Unused
7	EN (End of track). When the 8272 tries to access a sector beyond the final sector of a track, this bit is set.

READ REGISTER 2 (PORT 81h STATUS)

Register AL Bit (CPU)	Read Information
0	MD (Missing Address Mark in Data Field). When data are read from the floppy disk, if the 8272 cannot find a data address mark or deleted data address mark, this bit is set.
1	BC (Bad Track (Cylinder)). This bit is related to the ND bit. When the content of C on the floppy disk is different from that stored in the IDR and the content of C is FFh, this bit is set.
2	Unused
3	Unused
4	WC (Wrong Track (Cylinder)). This bit is related to the ND bit. When the content of C on the floppy disk is different from that stored in the IDR, this bit is 1.
5	DD (Data Error in Data Field). If the 8272 detects a CRC error in the data field, this bit is 1.
6	CM (Control Mark). During the execution of of a Read Data or Scan command, if the 8272 encounters a sector which contains a deleted data address mark, this bit is 1.
7	Unused

READ REGISTER 3 (PORT 81h STATUS)

Register AL Bit (CPU)	Read Information
0-1	US0-1 (Unit Select 0 and 1). These bits are used to indicate the status of the unit select signals to the floppy disk drives. Only US0 is used in the AWS-220 and -230.
2	HD (Head Address). If 1, the first side of the two-sided floppy disk is selected for an operation. If 0, the second side is selected.
3	TS (Two Side). Must always be 1.
4	T0 (Track 0). If 1, this bit indicates that the read/write head is over track 0.
5	RDY (Ready). If 1, this bit indicates that the floppy disk drive is ready for an operation.
6	WP (Write Protected). If 1, the floppy disk is write protected.
7	FT (Fault). If 1, the floppy disk drive has faulted.

Port A4h

While Port A4h has seven usable bits, only three of them are used for the floppy disk drive; two of the other bits are used for communications.

Register AL Bit (CPU)	Write Information
0	Used by RS-232-C communications ports. Must be set according to communications parameters in use.
1	Used by RS-232-C communications ports. Must be set according to communications parameters in use.
2	If 1, this bit starts the motor on floppy disk drive 0.
3	If 1, this bit starts the motor on floppy disk drive 1.
4	Used by RS-232-C communications ports. Must be set according to communications parameters in use.
5	Used by RS-232-C communications ports. Must be set according to communications parameters in use.
6	Unused. Must be 0.
7	If 1, this bit resets the 8272 (this bit is ORed with the power-up and manual reset line, BRESET+).

Port B4h

The four bits in Port B4h supply the four high-order bits in the DMA address. These four bits allow a DMA-controlled read or write operation to start at any 64-kilobyte boundary in the AWS-220 and -230 RAM.

Register AL Bit (CPU)	Write Information
0-3	Address bits 10h-13h

AWS-240 HARD DISK CONTROLLER

The hard disk controller on the HDC Board controls all disk related functions for the AWS-240. Drive 0 is always a 5 1/4-in floppy disk drive of the same data format as the drives installed in the AWS-220 and AWS-230. Drive 1 is a 5 1/4-in Winchester hard disk drive with a minimum formatted capacity of five megabytes. Although Drive 0 is a floppy disk drive, the hard disk controller regards it as a slower hard disk drive.

The controller is based on a Signetics 8X300 microcontroller, operating from a microprogram resident in four kilobytes of ROM. The 8X300 fetches instructions from its two ROMs with its address and instruction buses, which are isolated from the LA0+-LA13+ and BD0+-BD7+ buses used by the other devices on the HDC and CPU Boards.

The 8X300 communicates with external devices over its 8-bit IV (Instruction-Vector) bus. The IV bus accommodates separate right and left banks of input/output devices. The only device on the left bank of the IV bus is a 256-byte disk data buffer. All of the other disk controller input/output ports are on the right bank of the IV bus. The architecture of the 8X300 allows it to receive data on one bank, process the data, and then deposit the data on either bank, all in one machine cycle of 250 ns. Since the microprogram ROM is addressed with separate address lines and instruction lines, the next instruction can be fetched while the 8X300 is processing on the IV bus.

An 8X320 bus interface register array is the interface between the IV bus and the BD0+-BD7+ data lines. The 8X320 has sixteen 8-bit registers that contain disk data, and command or status information. DMA Channel 0 is used to control data transfers for disk read and write operations while an interrupt controlled mode is used for certain status commands and for ready/not-ready status changes. An Extended Address Register provides four high-order address bits, which are used when the DMA address is programmed by the CPU on the CPU Board. This allows the disk data buffer to be in any 64-kilobyte block of RAM.

Read and Write Operations

Disk Read and write operations performed by the 8X300 require that DMA Channel 0 be used to transfer data between the selected disk drive and the RAM on the CPU Board. A typical read or write operation follows these basic steps:

1. DMA Channel 0 of the 8257 is programmed by the CPU at input/output Ports 8h, 0, and 1h for the data buffer address, transfer length, and transfer direction (to or from memory).

2. The Extended Address Register at Port B4h is loaded with the upper four bits of the disk data buffer address (LA10+-LA13+) and DMA Channel 0 is started (see "Direct Memory Access" above).

3. The CPU sends a read or write command (five bytes) to the 8X300 through the 8X320 at Port 82h. This is the command phase of the read or write operation. The CPU can send one of the command bytes when handshake bit 5 of Flag Register 1 (Port 8Eh) is 0. When the CPU writes a command byte into the Command Register, bit 5 of Flag Register 1 is set in the 8X320; it is reset when the 8X300 processes the command byte. The CPU examines Flag Register 1 during the command phase of the read or write operation to see when another byte can be written to the Command Register. Flag Register 1 remains set after the last byte of the command is written into the Command Register.

4. When the last command byte is processed by the 8X300, the read or write operation begins the execution phase when the 8X300 sends a DMA request to the 8257 on the CPU Board through the EXTRQ+ (External Request) line.

5. The 8257 requests the address and data buses from the CPU, then acknowledges the 8X300's DMA request by pulsing DMACK- (DMA Acknowledge). The 8257 generates the appropriate command strobes, and transfers data from the CPU Board RAM to the DMA Data Register at Port 80h (for a write operation) or from the DMA Data Register to the CPU Board RAM (for a read operation). Each time the 8X300 is ready to transfer another byte, it makes a DMA request to the 8257.

6. When the transfer is complete, the 8257 returns control of the data and address buses to the CPU.

7. A short time later, the 8X300 interrupts the CPU via the 8259A interrupt controller, thus beginning the result phase of the operation.

8. After the CPU acknowledges the interrupt, it addresses Flag Register 0 at Port 8Fh. If bit 1 of the register is 1, the status register at Port 8Dh contains valid status information. The CPU can then read the Status 0 Register and reset bit 2 of Flag Register 0 after the last status byte is read.

Control Operations

Certain control operations, such as the Seek and Recalibrate commands, do not use DMA Channel 0 because data are not transferred. A typical control operation follows these basic steps:

1. At the beginning of the command phase of the operation, the CPU writes the appropriate command into the Command Register at input/output Port 82h. As with read or write commands, multiple-byte control commands require that the CPU examine Flag Register 1 at Port 8Eh after each byte is sent.

2. When the last byte of the command is processed by the 8X300, the execution phase of the command begins automatically.

3. When the control command completes, the 8X300 causes the INT6+ (Interrupt 6) line to pulse, thus causing an interrupt to the CPU on the CPU Board.

4. If the command just executed requires that one or more status registers be read, the CPU examines Flag Register 0 and reads the status bytes from Port 8Dh.

Control and Status Registers

There are several input/output ports in the 8X320 bus interface register array that affect the hard disk controller.

Port Number	Read Information	Write Information
80h	DMA Data Register	DMA Data Register
81h	Main Status Register	---
82h	---	Command Register
8Dh	Status	---
8Eh	Flag Register 1	---
8Fh	Flag Register 0	---
A4h	Unused with HDC.	Extended Control Register
B4h	---	Extended Address Register

Port 80h

The DMA Data Register is used for DMA transfers between the RAM array on the CPU Board and the 8X300. Since the CPU can have access to this register at any time, be sure that the Operating System does not access Port 80h while a DMA data transfer is occurring. At the conclusion of a DMA data transfer, the DMA Data Register contains the value of the last data byte transferred.

Register AL Bit (CPU)	Read or Write Information
0-7	Disk Data bits 0-7 (bit 0 is the least significant bit)

Port 81h

The Main Status Register contains information needed by the CPU to determine the general status of the hard disk controller, such as controller busy, interrupt request, drive ready, etc. The CPU can read this register at any time.

Register AL Bit (CPU)	Read Information
0	If 1, the floppy disk drive is ready.
1	If 1, hard disk drive is ready.
2	Unused
3	Unused
4	Controller busy. If 1, this bit indicates that the 8X300 is performing a read or write operation.
5	Interrupt request. This bit indicates the state of the interrupt request flag.
6	Unused
7	Unused

Port 82h

Port 82h is used by the CPU to issue commands to the hard disk controller. A description of the commands used is in Table 2-3. Commands for the hard disk controller have three distinct phases: command, execution, and result.

During the command phase, the 8X300 receives all the information from the CPU that it requires to perform a particular operation. After each command byte is transferred into the Command Register (if a multiple byte command is used), the CPU must read Flag Register 1 to know when to transfer another byte.

During the execution phase, the 8X300 performs the operation.

During the result phase, one or more of the status register bytes must be read. The Read Data command, for example, has only one byte which must be read before the 8X300 can accept another command.

Register AL Bit (CPU)	Write Information
0-7	Command bits 0-7 (Bit 0 is the least significant bit)

Port 8Dh

Status Registers 0-3 contain current status information for all of the disk drives under control of the 8X300, as well as information regarding the integrity of the CPU/8X300 communications protocol. All status information is maintained in a set of four registers, Status 0 through Status 3. A set of status registers is maintained for each drive in the system.

READ REGISTER 0 (STATUS)

Register AL Bit (CPU)	Read Information
0	USO (Drive select). If 1, the hard disk drive is selected to perform an operation. If 0, the floppy disk drive is selected.
1	Unused
2	Unused
3	If 1, the selected drive is not ready to perform an operation.
4	If 1, the selected drive is reporting a fault.
5	If 1, the selected drive has sucessfully performed a Seek command to a specific track.
6-7	Interrupt code (see below)

Interrupt Code

AL7	AL6	Code
0	0	Normal command termination
0	1	Unsuccessful command termination
1	0	Invalid command
1	1	Attention interrupt

READ REGISTER 1 (STATUS)

Register AL Bit (CPU)	Read Information
0	If 1, the head number selected during the command phase was invalid.
1	If 1, the media on the selected disk drive is write protected.
2	If 1, a read error was detected during the last read operation.
3	If 1, the sector number selected during the command phase was invalid.
4	If 1, a CRC (Cyclic Redundancy Check) error occurred during the last read operation.
5	If 1, data arrived at the controller too late.
6	If 1, a CRC error occurred in the identification field of a sector during the last read operation.
7	If 1, the track number selected during the command phase was invalid.

READ REGISTER 2 (STATUS)

Register AL Bit (CPU)	Read Information
0	If 1, the data address mark was not found during the last operation.
1	If 1, the identification address mark for the specified sector was not found during the last operation.
2	If 1, the disk on the drive was changed.
3	If 1, an error occurred with regard to the track number selected.
4	If 1, an error occurred with regard to the head number selected.
5	If 1, the last command was canceled.
6	If 1, an error occurred in the hard disk controller's data buffer.
7	If 1, an error occurred in the hard disk controller.

READ REGISTER 3 (STATUS)

Register AL Bit (CPU)	Read Information
0	USO (Drive select). If 1, the hard disk drive is selected to perform an operation. If 0, the floppy disk drive is selected.
1	Unused
2	Unused
3	If 1, the selected drive has sucessfully performed a Seek command to a specific track.
4	If 1, the read/write head of the selected drive is over track 00.
5	If 1, the selected drive is ready to perform an operation.
6	If 1, the media on the selected disk drive is write protected.
7	If 1, the selected drive is reporting a fault.

Port 8Eh

Flag Register 1 contains the handshake bit required for operation of the Command Register. If bit 5 of the register is 1, it indicates that the Command Register (Port 82h) is busy. CMDBSY (Command Register Busy) is set when the CPU writes to the Command Register; it is reset as soon as the 8X300 processes the byte in the Command Register. Bit 5 remains set once a complete set of command bytes is received by the 8X300, and the execution phase of the command is started.

FLAG REGISTER 1

Register AL Bit (CPU)	Read or Write Information
0-4	Unused
5	CMDBUSY (Command Register Busy)
6-7	Unused

Port 8Fh

Flag Register 0 contains the handshake bit required for operation of the Status Register. A 1 in bit position 2 of Flag Register 0 indicates that the Status Register (Port 8Dh) contains valid information. Once the CPU detects that STRDY (Status Ready) is 1, Port 8Dh can be read. Note that STRDY is not reset when the CPU reads the Status Register. The CPU must reset STRDY by writing a 0 to bit 2 of Port 8Fh.

FLAG REGISTER 0

Register AL Bit (CPU)	Read or Write Information
0	Unused
1	STRDY (Status Register Ready)
2-7	Unused

Table 2-3. Hard Disk Controller Commands. (Page 1 of 9)

READ DATA

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	X	USO	0	0	0	1	1	0	Command codes
	◄---- Head ------►|◄----- Track -------►								0-4/Most significant 4 bits
	◄---------- Track ----------►								Least significant 8 bits
	◄---------- 1st Sector ----------►								1-32
	◄-------- Number of Sectors ----------►								1 to 256 (2's complement)
Execution:									Data transfer between the disk drive and RAM
Result:									
	◄---------- Status 0 ----------►								Status information after command execution

Table 2-3. Hard Disk Controller Commands. (Page 2 of 9)

WRITE DATA

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:	X	USO	0	0	0	1	0	1	Command codes
	◄------ Head ----►|◄----- Track ------►								0-4/Most significant 4 bits
	◄-------------- Track ----------------►								Least significant 8 bits
	◄----------- 1st Sector -------------►								1-32
	◄-------- Number of Sectors ----------►								1 to 256 (2's complement)
Execution:									Data transfer between RAM and the disk drive
Result:	◄------------ Status 0 ---------------►								Status information after command execution

Table 2-3. Hard Disk Controller Commands. (Page 3 of 9)

FORMAT A TRACK

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	0	USO	0	0	1	1	0	1	Command codes
	◄------- Head ---►|◄----- Track-------►								0-4/Most significant 4 bits
	◄---------- Track ----------►								Least significant 8 bits
	◄---------- Offset ----------►								1-32
	◄---------- Spacing ----------►								1-32
	◄---------- Filler Data ----------►								0-255
Execution:									Controller formats the entire track of the selected disk drive
Result:									
	◄---------- Status 0 ----------►								Status information after command execution

Table 2-3. Hard Disk Controller Commands. (Page 4 of 9)

RECALIBRATE

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	0	USO	0	0	0	1	1	1	Command codes
Execution:									Head retracted to track 0
Result:									CPU must issue Sense Interrupt Status command

Table 2-3. Hard Disk Controller Commands. (Page 5 of 9)

SEEK

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	0	US0	0	0	1	1	1	1	Command codes
	◄------ Head ----►|◄---- Track -------►								0-4/Most significant 4 bits
	◄-------------- Track ----------------►								Least significant 8 bits
Execution:									Head is positioned over the proper track on the floppy disk
Result:									CPU must issue Sense Interrupt Status command

Table 2-3. Hard Disk Controller Commands. (Page 6 of 9)

SENSE INTERRUPT STATUS

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:	X	X	0	0	1	0	0	0	Command codes
Result:									CPU reads the following three bytes from the status port
	◄---------- STATUS 0 ----------►								Status
	◄------ Head ----►|◄----- Track ------►								0-4/Most significant 4 bits
	◄---------- Track ----------►								Least significant 8 bits

NOTE: The interrupt request flag is cleared immediately after Status 0 is read.

Table 2-3. Hard Disk Controller Commands. (Page 7 of 9)

READ DRIVE STATUS

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:	0	USO	0	0	0	1	0	0	Command codes
Result:									CPU reads the following three bytes from the status port
	◄---------- Status 3 ----------►								Status
	◄------ Head ----►|◄----- Track ------►								0-4/Most significant 4 bits
	◄---------- Track ----------►								Least significant 8 bits

Table 2-3. Hard Disk Controller Commands. (Page 8 of 9)

READ FULL STATUS

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:	X	USO	0	0	0	0	1	1	Command codes
Result:									CPU reads the following six bytes from the status port
	◄---------- Status 0 ----------►								Status information after command execution
	◄---------- Status 1 ----------►								
	◄---------- Status 2 ----------►								
	◄---------- Status 3 ----------►								
	◄---- Head ------►|◄------ Track -----►								0-4/Least significant 4 bits
	◄---------- Track ----------►								Least significant 8 bits

Table 2-3. Hard Disk Controller Commands. (Page 9 of 9)

READ DRIVE CONFIGURATION

Phase	Data Bit 7	6	5	4	3	2	1	0	Remarks
Command:									
	X	USO	0	0	1	1	0	0	Command codes
Result:									CPU reads the following six bytes from the status port
	◄------ Firmware Revision Level ------►								Status information after command execution
	◄------- Number of Tracks (LSB) ------►								
	◄------- Number of Tracks (MSB) ------►								
	◄------ Number of Heads per Track ----►								
	◄----- Number of Sectors per Track ---►								
	◄---------- Drive Present ----------►								

VIDEO DISPLAY CONTROLLER

The video display system is based on an Intel 8275 CRT controller chip and a font ROM. The 8275 is used to provide a video display with 80 character positions in the first 28 rows and 78 in row 29. The 8275 is highly programmable; it controls raster and cursor timing, row buffering, and special visual attribute decoding. The 8275 logic, operating in conjunction with DMA Channel 2, refreshes the video display directly from memory and contains a pair of row buffers to store the row of characters currently being refreshed.

Characters are generated with a font ROM that contains 256 displayable characters. A video attribute character is used to select which half of the font ROM is used for characters on the video display. The low-order seven bits of a character in the video display buffer select which of the 128 characters of the selected font is actually displayed. The font ROM determines which pixels are lit in each of the 2,318 displayable character cells on the video display.

Command and Status Registers

Commands given to the 8275 require from 0 to 4 associated parameters. The 8275 is programmed through Ports 20h and 22h as follows:

Port	Input	Output
20h	Not used	Video parameters
22h	Video status	Video commands

Register AL Bit (CPU)	Read Information
0	FIFO overrun (too many video attributes)
1	DMA underrun
2	Video enabled
3	Improper command
4	Light pen (not used)
5	Vertical retrace interrupt (not used)
6	Retrace interrupt enable (not used)
7	Must be 0

The commands used on the AWS-220, -230, and -240 CPU Board for the 8275 are Reset Video, Start Video, Stop Video, and Set Cursor.

Reset Video

Port	Binary Value (least significant bit at right)
22h	00000000
20h	SHHHHHHH
20h	00RRRRRR
20h	0000LLLL
20h	MF1C1001

where:

S is 0 for normal rows or 1 if every other row is to be blank.

H is the number (seven bits) of characters per row minus one (maximum of 79).

R is the number (six bits) of rows of characters minus one.

L is the number (four bits) of raster lines per row minus one.

M is 0 if the raster line numbers start at 0 (in the font ROM) or 1 if they start at 1.

F is 0 for invisible attribute characters or 1 for blank attribute characters.

C is 0 for a nonblinking cursor or 1 for a blinking one.

Start Video

Port	Binary Value (least significant bit at right)
22h	001SSSBB

where:

SSS	Number of Character Clocks Between DMA Requests
000	0 (continuous request)
001	7
010	15
011	23
100	31
101	39
110	47
111	55

BB	Character Burst Length
00	1
10	4
11	8

Stop Video

Port	Binary Value (least significant bit at right)
22h	01000000

Set Cursor

Port	Binary Value (least significant bit at right)
22h	10000000
20h	Column number
20h	Row number

Character Types

The 8275 requests characters from memory via the 8257 DMA controller. The three types of characters are:

- o normal,
- o control, and
- o attribute.

Normal Characters

A normal (displayable) character has the high-order bit set to 0. At the proper time, the 8275 presents the 7-bit character value to the font ROM to produce the desired pixel matrix.

Control Characters

A control character controls special blanking and DMA requirements. They are:

Value	Function
F0h	End-of-row. Causes the rest of the character row to be turned off. This control character is not used with the CTOS Operating System.
F1h	End-of-row/Stop DMA. Same as F0, but DMA is stopped for the row and the next DMA character read is the first character displayed in the next row. Not used with the CTOS Operating System.
F2h	End-of-screen. Causes the rest of the video display to be turned off. Not used with the CTOS Operating System.
F3h	End-of-screen/Stop DMA. Same as F2h, but DMA is stopped for the frame and the next DMA character read is the first character on the video display.

Attribute Characters

An attribute character is a special character that affects the appearance of a normal character. The normal character immediately following the attribute character has the attributes specified in it. The attributes remain in effect until the end of the frame or until another attribute character is encountered in the video display refresh buffer. The attribute bits can be used in any combination to select several simultaneous attributes. The attributes, as implemented on the CPU Board, are:

Value (binary)	Function
100URABH	U = 1 turns on underline.
	R = 1 sets reverse video.
	A = 1 selects alternate font.
	B = 1 turns on blinking.
	H = 1 sets half-bright.

Underline:
The ninth raster line in the cell is all light in normal video or all dark in reverse video.

Reverse video:
All pixels that are normally light are dark and vice versa. Spaces are displayed as all light.

Alternate font:
This selects the second 128 characters in the font ROM. The upper half of the alternate font is used for line-drawing (graphic) characters.

Blinking:
This causes the field to blink at approximately a 1 Hz rate.

Half-bright:
The selected field is displayed at approximately half the normal brightness.

There is a limit of 16 attribute characters per row of characters in the "invisible attribute" mode (that is, the mode in which the attribute characters do not appear as blank spaces in the video display row).

Font ROM Format and Line-Drawing Characters

The font ROM determines which pixels are lit in a 9-by-11 pixel character cell. The input (or address) to the font ROM is the 7-bit character

number from the video display refresh buffer, the alternate font attribute, and the 4-bit raster line number from the 8275. Based on those 12 bits, the font ROM emits eight bits of horizontal pixel information. Seven of the bits specify which individual pixels are lit; the eighth bit invokes half-bit shift. Half-bit shift is a special mechanism that shifts all the pixels of a particular raster line within a particular character one-half pixel to the right. This mechanism provides overlapped pixels, better centering, and smoother lines.

Font ROM Address Bit	Function
0-6	Character code bit 0-6
7-9	Raster line count bit 0-9
A	Raster line count bit 3
B	Alternate font attribute set

When 0, the high-order output bit of the font ROM turns on the half-bit shift mechanism. The use of the other outputs of the font ROM depends on whether a line-drawing or normal character is displayed. With the pixels numbered 0 to 8 (left to right), the correspondence between pixels and font ROM outputs is:

Normal Characters Horizontal Pixel	Function
0	Off except during underline
1-7	ROM output 0-6
8	Off except during underline

Line-Drawing Characters Horizontal Pixel	Function
0	ROM output 0
1-3	ROM output 2
4	ROM output 3
5	ROM output 4
6	ROM output 5
7	ROM output 6
8	ROM output 1

Line-drawing characters are used when connecting horizontal lines are required. Since the cell is nine pixels wide and only seven bits of font ROM output are available, normal characters have the two outside pixels turned off. The 256 characters of the font ROM are split into three groups:

Character Type	Alternate Font Attribute	Character Code Range
Normal characters standard font	Not set	0-7Fh
Normal characters alternate font	Set	0-3Fh
Line-drawing characters	Set	40h-7Fh

Programming Considerations

Control Characters

F3h control characters are used with the 8275 by the CTOS Operating System. They are inserted as the last two bytes in row 29 of the video display. The F3h character signals the 8275 that it is at the end of row 29 and that DMA must stop. The next time that DMA starts to refresh a row, the first character read by the 8257 is positioned in row 1 and in the first character position of the video display. Two F3h characters are used for character synchronization, which accounts for row 29 having only 78 characters.

If F3h characters are not used, the 8275 can lose synchronization with the 8257. If so, the first character on the video display that normally appears at row 1 on column 1 appears at another (unpredictable) position on the video display.

Attribute Characters

With the CTOS Operating System, the video map within the first 64 kilobytes of RAM consists of up to 96 bytes times 29 rows. Eighty bytes per row are used for normal characters. The remaining bytes are reserved for 16 mandatory video attribute characters. While the CTOS Operating System requires 16 attribute characters per row and 29 rows, other software can have, for example, a greater number of rows and fewer attribute characters.

The video attribute characters must never be next to each other in the video map. That is, each attribute character must have at least one normal character on which to operate. If a desired effect requires one or more simultaneous attribute sets, they must be combined into one attribute character.

For example, a group of half-bright, blinking, characters in reverse video would be represented by an attribute character equal to 93h. Assuming that one entire row of characters is desired to display this combination of attributes and that the Operating System requires 16 attribute characters, then the 93h attribute character must appear exactly 16 times within a 96-byte row of the video display. Again, the attribute characters can never appear next to each other. A row of normal characters with no attributes must still have 16 attribute characters, each equal to 80h, dispersed throughout the 96-byte row.

The video display can flash if the wrong number of video attributes (fewer or greater than the number required by the Operating System) appears on a row of the video display. This problem arises when the particular attributes within a row must be updated by the CPU. If the 8257 is ready to refresh the same row that the CPU is updating, the 8257 requests the bus from the CPU before the new attributes are completely updated. The row then displayed is incomplete and might contain either an incorrect number of attributes, consecutive attributes, or both. The solution is never to allow the CPU to update the attribute bytes on a row when the DMA address is within 48 bytes of the row.

For example, if row 14 of the video display is to be updated with a new set of attribute characters, the CPU must read the current DMA address with a Port 5h input instruction. If the DMA address indicates that the 8257 has read more than one-half of row 13 (more than 48 bytes in the CTOS Operating System), the CPU must wait until the 8257 begins to refresh the first character of row 15. Note that normal characters are not affected by this problem. As long as there are the proper number of nonconsecutive attributes within the row, the arrangement of normal characters is irrelevant.

8275 Programming Example

Figure 2-8 is a listing of the initialization sequence used for the 8275 and Channel 2 of the 8257. If more extensive information concerning the Intel 8275 is required, see the Component Data Catalog published by the Intel Corporation.

```
                    VIDEO DISPLAY MANAGER (WINDOW)

/* Literals for AWS-220, -230, and -240 video (8275) and DMA
(8257) */

/* Reset command arguments for 8275 */
DECLARE
VidNormalRows                                   LITERALLY '00H'
VidSpacedRows                                   LITERALLY '80H'
VidCols80                                       LITERALLY '4FH'
VidRows29                                       LITERALLY '28H'
VidUnderline7                                   LITERALLY '0AH'
VidLinesPerRow11                                LITERALLY '10H'
VidCounterMode0                                 LITERALLY '00H'
VidCounterMode1                                 LITERALLY '80H'
VidFieldAttrTransparent                         LITERALLY '00H'
VidFieldAttrNonTransparent                      LITERALLY '40H'
VidCursorFormatBlinkReversed                    LITERALLY '00H'
VidHzRetraceCnt20                               LITERALLY '09H'

/* 8275 command registers */
DECLARE
VidParamReg                                     LITERALLY '20H'
VidStatusReg                                    LITERALLY '22H'
VidCommandReg                                   LITERALLY '22H'

/* 8257 command registers */
DECLARE
VideoAddressInitReg                             LITERALLY '4H'
VideoCountInitReg                               LITERALLY '5H'
VideoAddressReInitReg                           LITERALLY '6H'
VideoCountReInitReg                             LITERALLY '7H'
DMAStatusReg                                    LITERALLY '8H'
DMAModeReg                                      LITERALLY '8H'

/* 8257 parameters */
DECLARE;
dmaModeChannel10                                LITERALLY '01H'
dmaModeChannel11                                LITERALLY '02H'
dmaModeChannel12                                LITERALLY '04H'
dmaModeChannel13                                LITERALLY '08H'
dmaModeRotatingPriority                         LITERALLY '10H'
dmaModeExtendedWrite                            LITERALLY '20H'
dmaModeTcStop                                   LITERALLY '40H'
dmaModeAutoLoad                                 LITERALLY '80H'
dmaCountModeVerify                              LITERALLY '00H'
dmaCountModeWrite                               LITERALLY '40H'
dmaCountModeRead                                LITERALLY '80H'
```

Figure 2-8. 8275 Programming Example. (Page 1 of 3)

```
CommandDma:  PROCEDURE (pb, cb) ErcType REENTRANT,
/* Program the video DMA channel and the 8275 to reset the video
display */

DECLARE;
pb POINTER    /* Pointer to video map */
rgbVidMem BASED pb (1) BYTE
cb WORD    /* Size of video map */
wPb (2) WORD AT (@pb)

DECLARE;
byteAddress (2) WORD
cRows WORD

cRows = 28;

/* Map pb into Address */
byteAddress (0) = SHL(wPb(1), 4) + wPb(0);

/* Disable interrupts and reset 8275 */
DISABLE;
OUTPUT (VidCommand Reg) = 0;

OUTPUT(VidParamReg) = VidNormalRows + VidCols80; /* Set normal
rows, 80 columns */

OUTPUT(VidParamReg) = cRows; /* Set to number of rows */

OUTPUT(VidParamReg) = VidUnderline7+VidLinesPerRow11; /* 11
rows, underline 7 */

OUTPUT(VidParamReg) = VidLineCounterMode0 +
VidFieldAttrTransparent + VidCursorFormatBlinkReversed +
VidHzRetraceCnt20; /* Nonoffset, transparent attributes,
blinking reversed cursor */

/* Set DMA count */
OUTPUT(VideoCountInitReg) = (cb - 1) AND OFFH; /* Low byte of
count */

OUTPUT(VideoCountInitReg) = DMACountModeRead + (SHR((cb - 1), 8)
AND OFFH);  /* High byte of count and direction */

OUTPUT(VideoCountReInitReg) = (cb - 1) AND OFFH;

OUTPUT(VideoCountReInitReg) = DMACountModeRead + (SHR((cb - 1),
8) AND OFFH);
```

Figure 2-8. 8275 Programming Example. (Page 2 of 3)

```
/* Set DMA address */
OUTPUT(VideoAddressInitReg) = LOW(byteAddress (0));

OUTPUT(VideoAddressInitReg) = HIGH(byteAddress (0));

OUTPUT(VideoAddressInitReg) = LOW(byteAddress (0));

OUTPUT(VideoAddressInitReg) = HIGH(byteAddress (0));

/* Disable 8275 interrupts */
OUTPUT(VidCommandReg) = 0C0H

/* Turn off cursor */
OUTPUT(VidCommandReg) = 80H;
OUTPUT(VidParamReg) = 0FFH;
OUTPUT(VidParamReg) = 0FFH;

/* Turn on interrupts */
ENABLE;

------------------------------------------------------------

pBuffer = pDist;
oBuffer = pBufferRa + SHL (pBufferSa, 4);  /* Address of row to
be updated */

DO FOREVER;

DISABLE;

oDMACurrent = INPUT (4);
w = INPUT (4);
oDMACurrent = oDMACurrent + SHL(w, 8);  /* Current DMA address
*/

IF ((oBuffer - 48) > oDMACurrent) OR ((oBuffer + 48) <=
oDMACurrent) THEN DO;
   CALL MOVW(pSrc, pDst, 48);
   ENABLE;
   RETURN;
   END;
ENABLE;
END;
```

Figure 2-8. 8275 Programming Example. (Page 3 of 3)

WORKSTATION INPUT/OUTPUT ADDRESS SUMMARY

Table 2-4 below is a summary of the input/output ports defined for the AWS-220, -230, and -240. Port number, logic associated with the port, input information, and output information are all listed. Note that Ports 6 and 7 are used for auto-initializing Ports 4 and 5.

Table 2-4. Input/Output Address Summary. (Page 1 of 4)

Port Number	Associated Logic	Input	Output
0	8257	Disk controller address	Disk controller address
1	8257	Disk controller count	Disk controller count
2	8257	Cluster communications address	Cluster communications address
3	8257	Cluster communications count	Cluster communications count
4	8257	Video address	Video address
5	8257	Video count	Video count
6	8257	Video address	Video address
7	8257	Video count	Video count
8	8257	DMA status	DMA mode
20	8275	Video parameters	Video parameters
22	8275	Video status	Video commands

Table 2-4. Input/Output Address Summary. (Page 2 of 4)

Port Number	Associated Logic	Input	Output
40	8253	Speaker frequency divisor	Speaker frequency divisor (Counter 0)
42	8253	Cluster communications divisor	Cluster communications divisor (Counter 1)
60	7201	Cluster data	Cluster data (Channel A)
62	7201	Cluster status	Cluster commands
64	7201	Keyboard data	Keyboard data (Channel B)
66	7201	Keyboard status	Keyboard commands
80	8272	Floppy main status	---
		or	
80	8X320	Hard disk DMA Data Register	Hard disk DMA Data Register
81	8272	Floppy status	Floppy commands
		or	
81	8X320	Hard disk status	
82	8X320	---	Hard disk commands
8D	8X320	Hard disk status	
8E	8X320	Flag Register 1	
8F	8X320	Flag Register 0	

Table 2-4. Input/Output Address Summary. (Page 3 of 4)

Port Number	Associated Logic	Input	Output
A0	8259A	Interrupt status	Interrupt control
A1	8259A	Interrupt mask	Interrupt mask
A4	General	Extended communication status	Extended communication control
A8	7201	Channel A data	Channel A data
A9	7201	Channel A status	Channel A status
AA	7201	Channel B data	Channel B data
AB	7201	Channel B status	Channel B status
AC	8253	Programmable timer	Programmable timer
AD	8253	Channel B baud rate	Channel B baud rate
AE	8253	Channel A baud rate	Channel A baud rate
AF	8253	8253 mode	---
B0	Printer	Status	Data
B4	Disk	---	Disk extended DMA address
E0	Parity	Low eight bits of address	---
E4	Parity	Middle eight bits of address	---

Table 2-4. Input/Output Address Summary. (Page 4 of 4)

Port Number	Associated Logic	Input	Output
E8	Parity	Bits 0-3 are the high 4 bits of the address; bit 4 is high if DMA caused the error.	---
F0	Parity	---	Enables parity detection
F4	Parity	---	Disables parity detection and clears error

3 THEORY OF OPERATION

INTRODUCTION

This section addresses the needs of the engineer who must understand the AWS-220, -230, and -240 hardware at the component level.

Figure 3-1 below shows the block diagram for this section. Each of the functional blocks in Figure 3-1 is discussed in relation to the logic that performs the function. With few exceptions, each description is a complete unit, with its own detailed functional block diagram and a reference to the appropriate schematic.

Most of the functional blocks of circuitry described in this section can be found on schematics for the two CPU Boards, the FDC Board, HDC Board, CRT Deflection Board, or keyboard.

Two CPU Boards can be used in the AWS-220, -230, and -240: the 8088 CPU Board, which uses an 8088 microprocessor, and the 8086 CPU Board, which uses an 8086 microprocessor. Each CPU Board contains a microprocessor, memory logic, four DMA channels, two communications channels (one for cluster and one for the keyboard), a programmable timer, and video display control logic. Throughout this section, where it is unnecessary to differentiate between the 8088 CPU Board and the 8086 CPU Board, the microprocessor and its associated logic is referred to as "the CPU." The schematic for the 8088 CPU Board is Figure 3-2; the 8086 CPU Board schematic is Figure 3-14.

The FDC (Floppy Disk Controller) Board contains a floppy disk controller for the AWS-220 and -230, two RS-232-C communications channels, a programmable timer, a printer interface, and interrupt control logic for the on-board devices. The FDC Board schematic is Figure 3-25 in the "Bus Interface and Interrupt Control Logic" subsection, below.

The HDC (Hard Disk Controller) Board contains a combined floppy/hard disk controller for the AWS-240 in place of the floppy disk controller used on the FDC Board. With this one exception, the logic on the HDC Board is identical to that on the FDC Board. The HDC Board is Figure 3-31

in the "Bus Interface and Interrupt Control Logic" subsection, below.

The CRT Deflection Board contains all the analog circuitry necessary to control the video display. The CRT Deflection Board is Figure 3-37 in the "CRT Deflection Board and Monitor" subsection, below.

The keyboard contains the 98-key keyboard and communications logic for communicating with the AWS-220, -230, and -240 workstation. The keyboard schematic is Figure 3-38 in the "Keyboard Interface Logic" subsection, below.

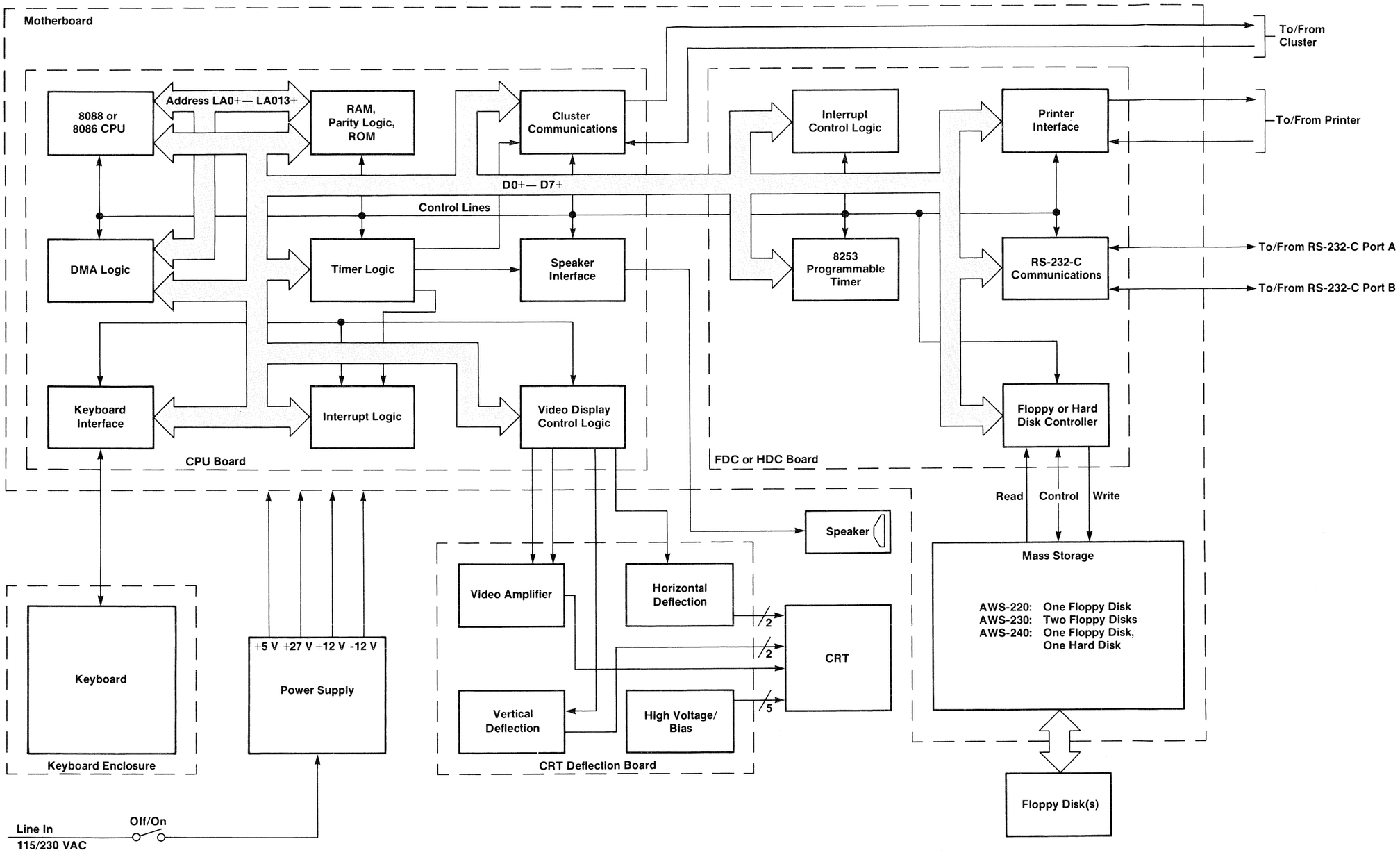


Figure 3-1. Theory of Operation.

8088 CPU BOARD

8088 Microprocessor Logic

Figure 3-2 below shows the major functional blocks of the 8088 microprocessor logic. The major blocks are:

- o the 8088 and its bus control logic;
- o clock, reset, and ready logic;
- o address and data latches; and
- o input/output address decoders.

In addition to Figure 3-2, see Figure 3-3 below, the CPU Board schematic, during the following discussion.

Bus Control Logic

As shown on page 2 of Figure 3-3, the 8088 at 5F is strapped at pin 33 to operate in the minimum mode. The minimum mode configures the 8088's bus control lines to be similar to those of an Intel 8085, thus making the lines compatible with 8085-type peripheral devices. The bus control lines include HOLD+ (Hold Request) at pin 31, HLDA+ (Hold Acknowledge) at pin 30, RD- (Read) at pin 32, WR- (Write) at pin 29, IO+/M- (Input/Output or Memory Decode) at pin 28, and ALE+ (Address Latch Enable) at pin 25.

Clock, Reset, and Ready Logic

The Intel 8284 clock generator (7F) provides several signals necessary for operation of the 8088. Crystal Y1 and capacitor C1 are connected to 7F pins 16 and 17 to form a 15-MHz oscillator. The 5-MHz PCLOCK+ (Processor Clock) at 7F pin 8 is generated by the 8284's division of the oscillator input frequency by three.

Power-up detection and reset switch debounce are provided by R1, C2, and CR1, which are connected to the 8284 pin 11 RES- (Reset) input. The 8284 internally conditions RES- with a Schmitt trigger, and, at its pin 10 output, generates RESET+ (General Purpose System Reset).

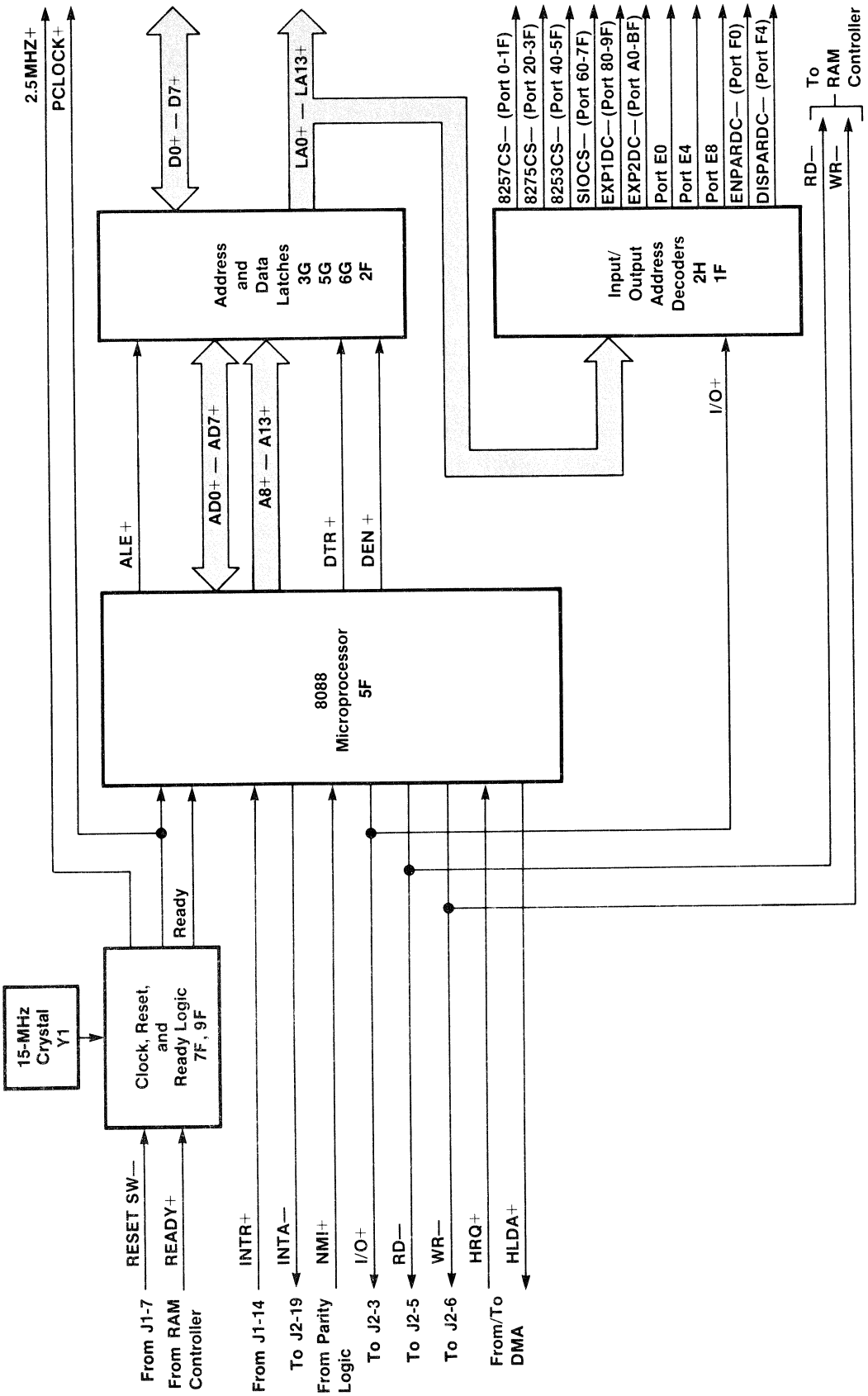


Figure 3-2. 8088 Microprocessor Logic.

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN PICOFARADS.
3. ALL DEVICES ARE STANDARD 7 & 14, 8 & 16, 10 & 20 GROUND AND POWER CONNECTIONS.
4. ALL DIODES ARE TYPE 1N914B.
5. 3301 (11G) IS AN ALTERNATE PART FOR THE 8275 (11G).

POWER AND GROUND LOCATOR CHART					
REF. DES.	TYPE	GND	+5V	+12V	-5V
7F	8284	9	18		
1G	8257	20	31		
5F	8088	1,20	40		
3H	2732	12	24		
11G	8275	20	40		
7H	8253	12	24		
8G	7201	20	40		
13H	2732-16	12	24		
6A-23A	4160-4	16	8		
6B-23B	4160-4	16	8		
6C-23C	4160-4	16	8		
6D-23D	4160-4	16	8		

SPARE GATES		
TYPE	REF. DESIGNATORS	QTY.
LS00	2A	2
LS04	8J	2
LS08	4B	1
LS74	2B, 9F	2
S74	10E	1
S132	1A	1
26LS02	9G	1
26LS31	10G	2
26LS32	10H	2

REF. DESIGNATORS	
LAST USED	NOT USED
RP15	
R20	
C132	
Q1	
CR10	
J2	

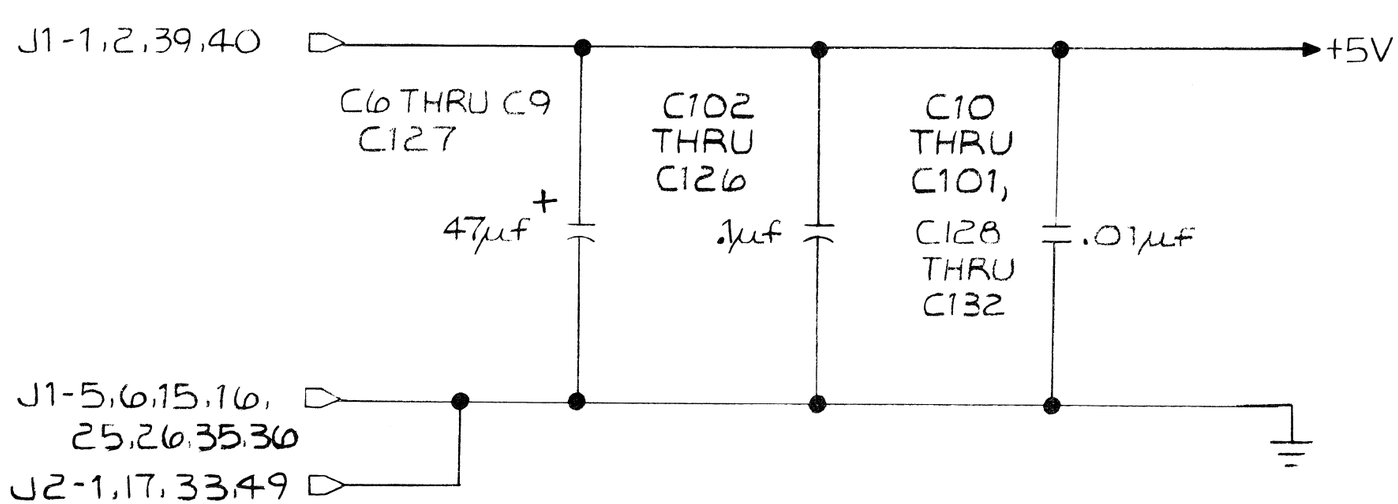


Figure 3-3. 8088 CPU Board Schematic. (Page 1 of 6)

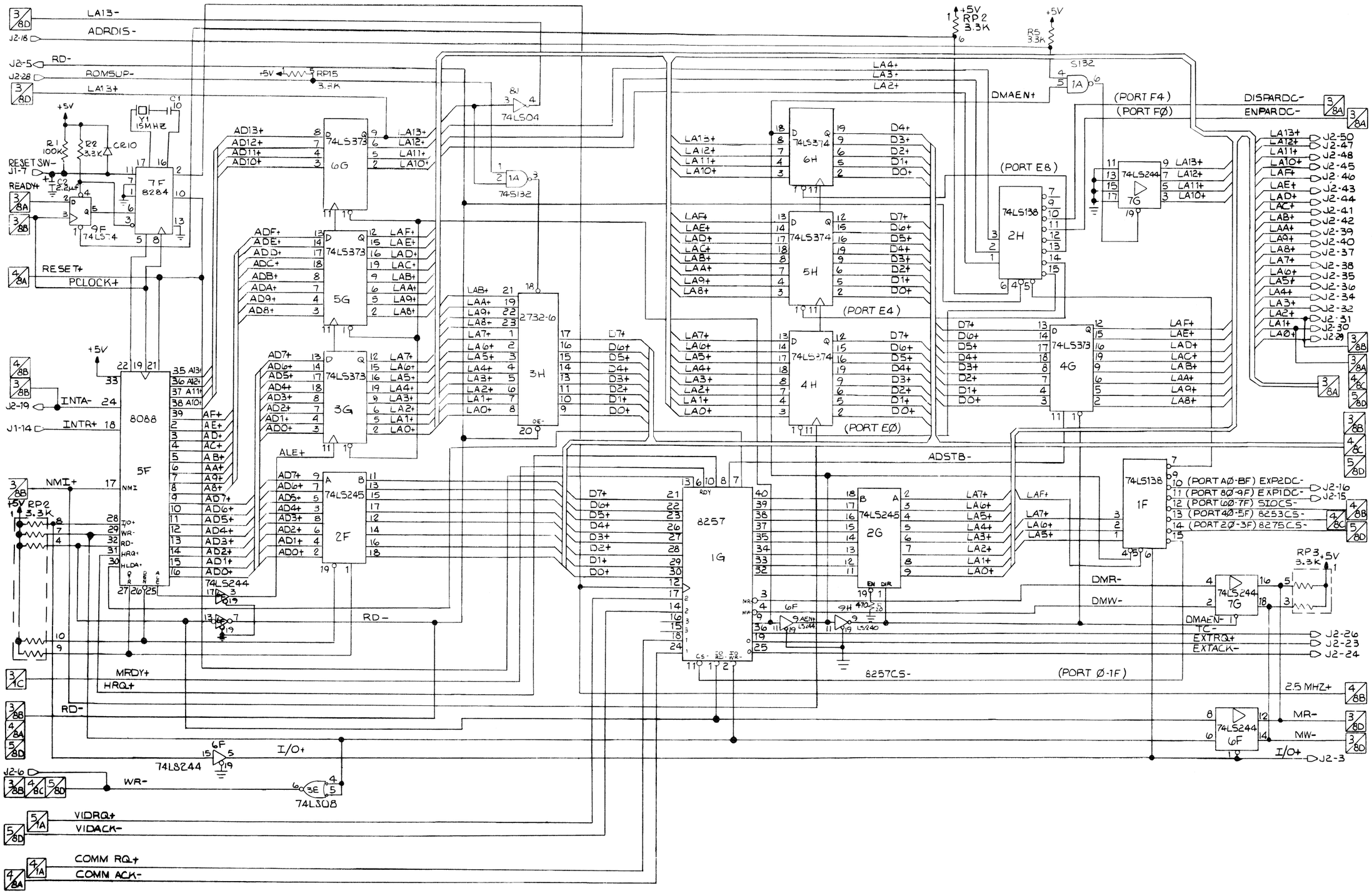


Figure 3-3. 8088 CPU Board Schematic. (Page 2 of 6)

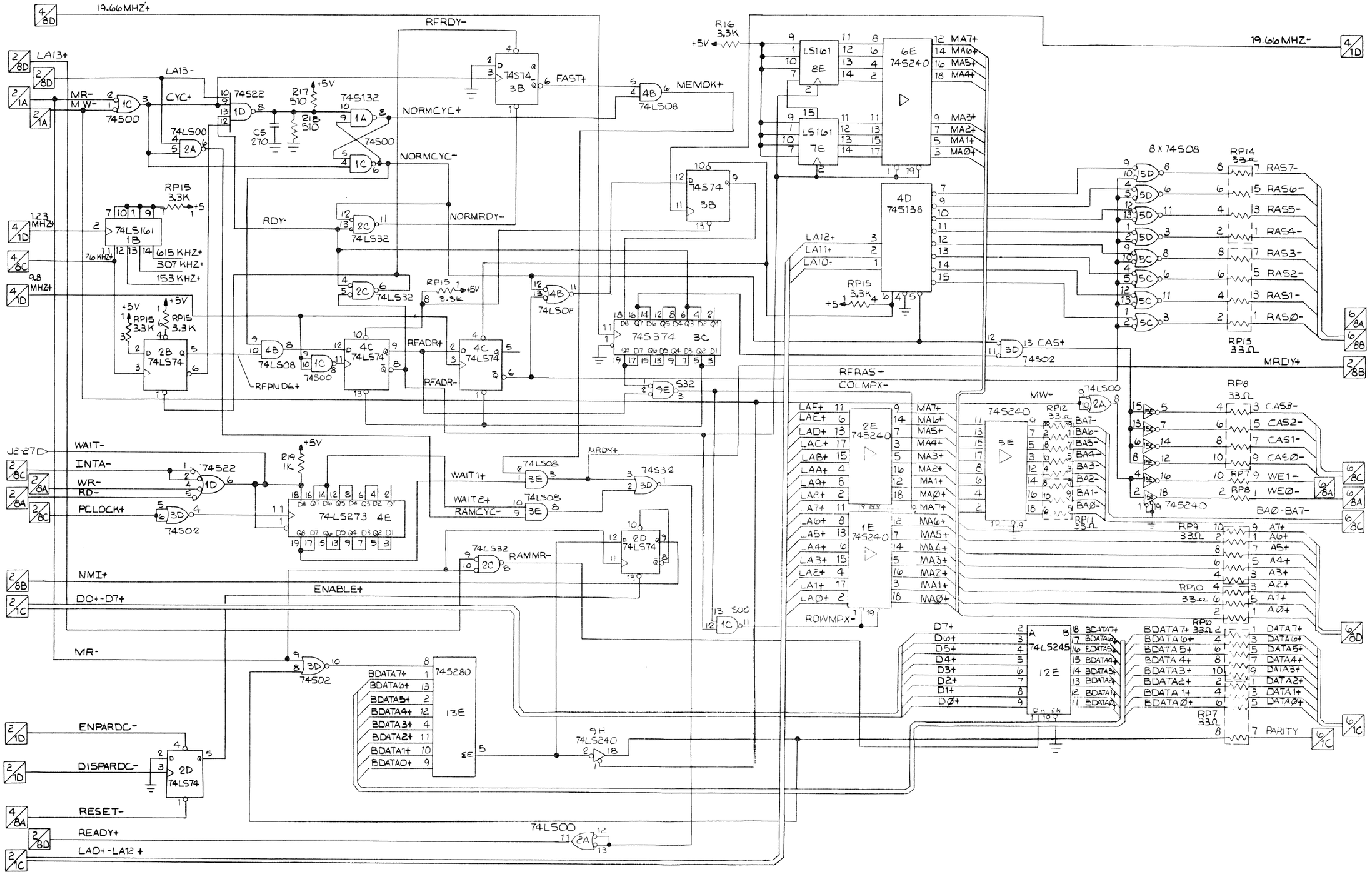


Figure 3-3. 8088 CPU Board Schematic. (Page 3 of 6)

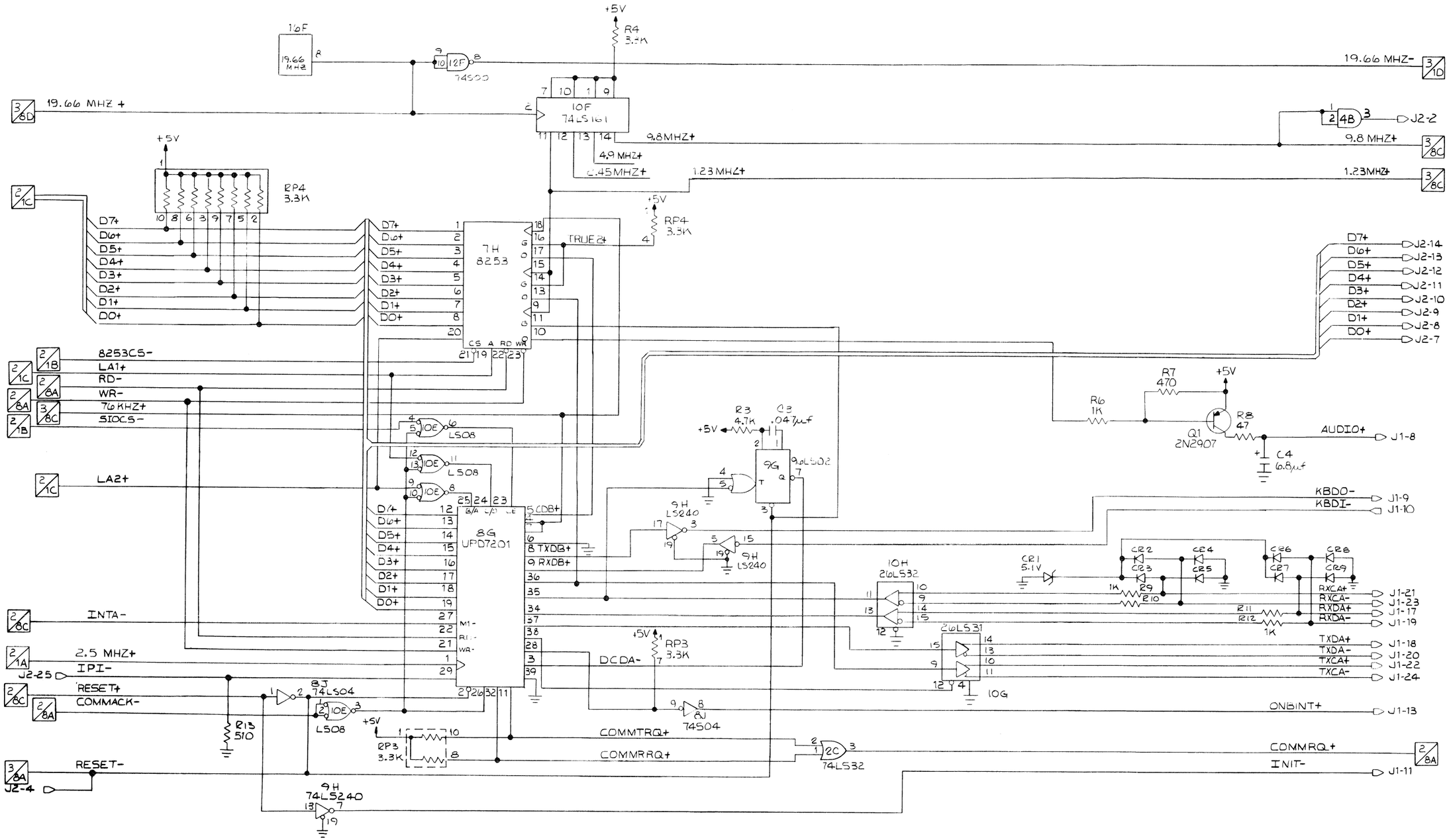


Figure 3-3. 8088 CPU Board Schematic. (Page 4 of 6)

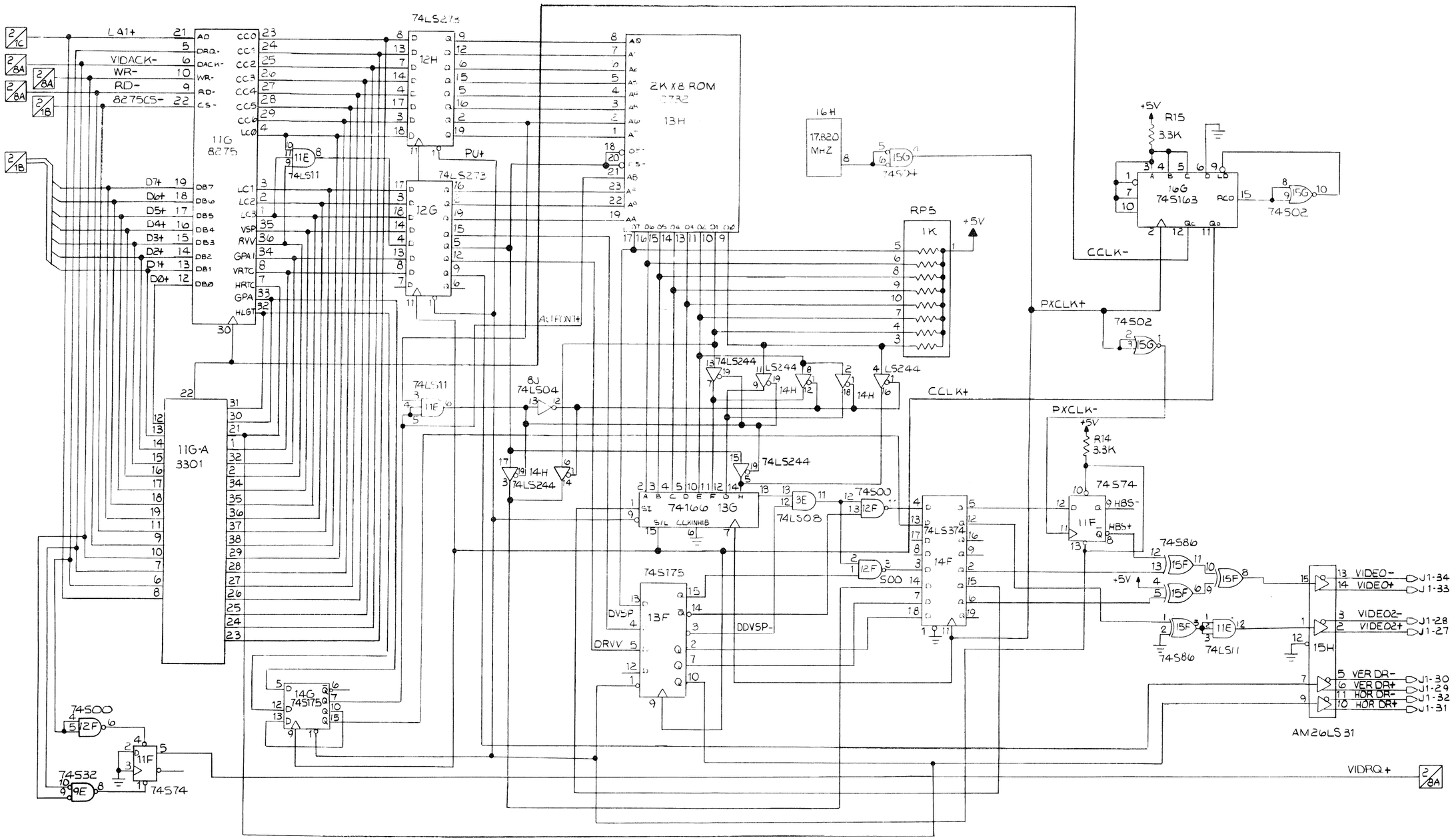
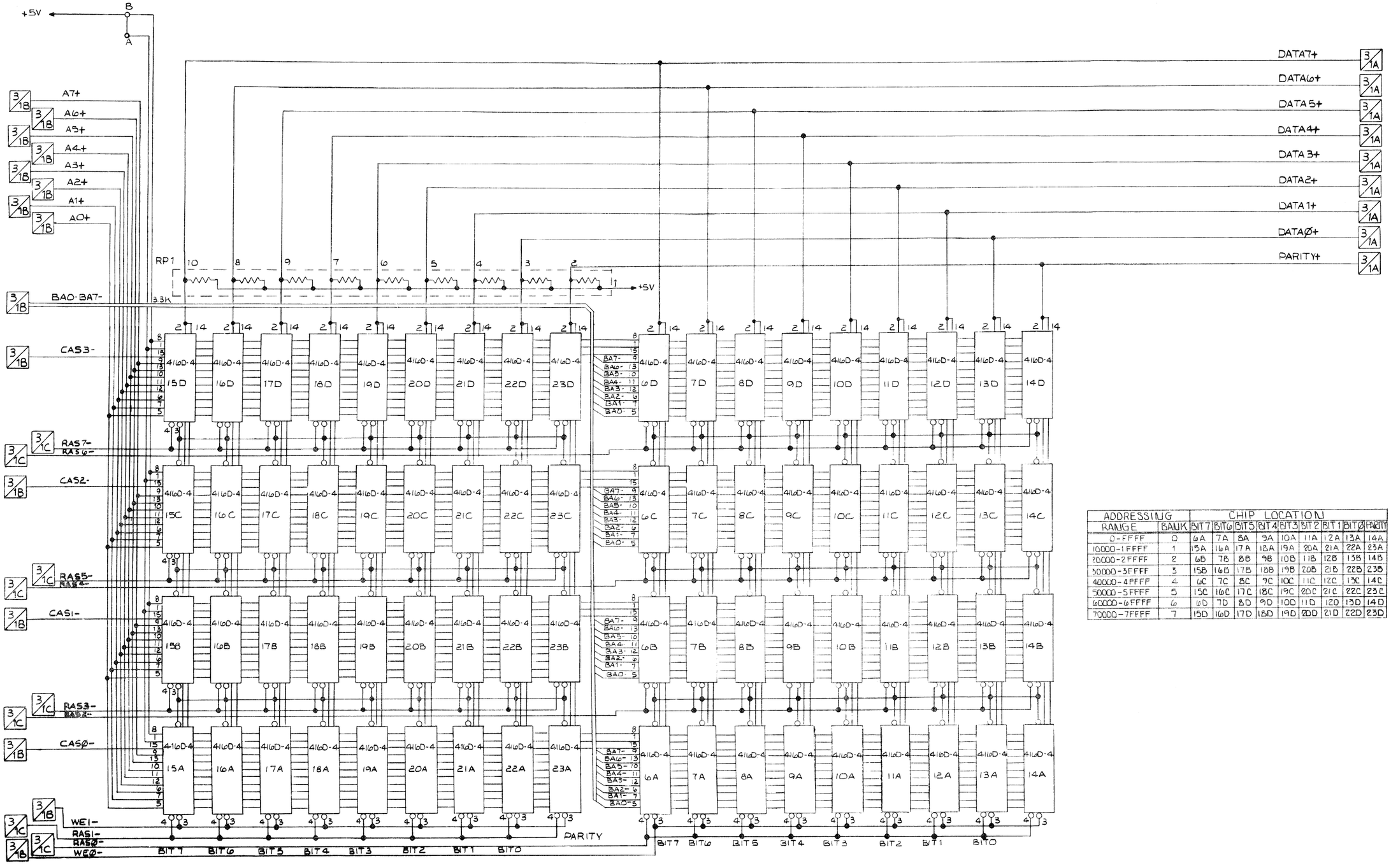


Figure 3-3. 8088 CPU Board Schematic. (Page 5 of 6)



ADDRESSING		CHIP LOCATION								
RANGE	BANK	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	PARITY
0-FFFF	0	6A	7A	8A	9A	10A	11A	12A	13A	14A
10000-1FFFF	1	15A	16A	17A	18A	19A	20A	21A	22A	23A
20000-2FFFF	2	6B	7B	8B	9B	10B	11B	12B	13B	14B
30000-3FFFF	3	15B	16B	17B	18B	19B	20B	21B	22B	23B
40000-4FFFF	4	6C	7C	8C	9C	10C	11C	12C	13C	14C
50000-5FFFF	5	15C	16C	17C	18C	19C	20C	21C	22C	23C
60000-6FFFF	6	6D	7D	8D	9D	10D	11D	12D	13D	14D
70000-7FFFF	7	15D	16D	17D	18D	19D	20D	21D	22D	23D

Figure 3-3. 8088 CPU Board Schematic. (Page 6 of 6)

Flip-flop 9F pin 5 is coupled to 7F pin 6 to synchronize the READY+ signal for the 8088 at the 7F pin 5 output. READY+ is a handshake signal sent from the memory controller to the 8088 to indicate that a memory or input/output cycle is complete and that the 8088 can request another cycle (see "Memory Logic" below).

Address and Data Buses

The tristate latches at 3G, 5G, and 6G latch the address coming from the 8088 on the multiplexed AD0+-AD7+ (Address/Data) lines and A8+-A13+ (Address) lines when the 8088 pulses ALE+. The outputs of the latches form the LA0+-LA13+ (Line Address) bus. When the 8088 is using the D0+-D7+ (Data) bus, transceiver 2F is enabled by DEN- (Data Bus Enable) from the 8088. The direction of the transceiver is established by DT+/R- (Data Transmit or Receive) from the 8088 at 5F pin 27. DT+/R- is active when data is being driven from the 8088 to the data bus.

Input/Output Address Decoders

The two decoders at 2H and 1F select input/output addresses. Decoder 1F is enabled when an 8088 input/output cycle is in progress, that is, when I/O+ (Input/Output) is high at 1F pin 6 and DMA is not in progress. DMAEN+ (DMA Enable) is low at 1F pin 4. After decoder 1F is enabled, it decodes address lines LA5+-LA7+ to generate the active-low enable signals:

Address Range	Active Signal	Origin	Device Accessed
0-1Fh	8257CS-	1F-15	8257 DMA controller
20h-3Fh	8275CS-	1F-14	8275 CRT controller
40h-5Fh	8253CS-	1F-13	8253 counter/timer
60h-7Fh	SIOCS-	1F-12	7201 communications
80h-9Fh	EXP1DC-	1F-11	Input/Output devices on FDC or HDC Board
A0h-BFh	EXP2DC-	1F-10	Input/Output devices on FDC or HDC Board
E0h-FFh	EXTDC-	1F-7	Decoder 2H

The decoder at 2H, enabled by EXTDC- (External Decoder Enable) and RD-, generates the following decoded read signals from address lines LA2+-LA4+:

Address Range	Active Signal	Origin	Device Accessed
E0h-E3h	---	2H-15	Reads parity error address latch at 4H
E4h-E7h	---	2H-14	Reads parity error address latch at 5H
E8h-EBh	---	2H-13	Reads parity error address latch at 6H
F0h-F3h	ENPARDC-	2H-11	Enables parity error detection and interrupts
F4h-F7h	DISPARDC-	2H-10	Disables parity error detection and parity error interrupts; clears existing errors

Memory Logic

Figure 3-4 below shows the functional blocks of the RAM, ROM, and parity logic.

The normal cycle logic performs both read and write memory cycles that can be used by the 8088 and 8257 to access up to 512 kilobytes of RAM.

Refresh cycles are initiated every 13 μs by the refresh cycle logic to maintain data stored in the dynamic RAM chips.

Ready (handshaking) logic controls the accesses by the 8088 and 8257. As long as the ready signal is not asserted to the appropriate bus master, the memory access is prolonged by wait states.

An even parity error detection scheme is used to ensure the integrity of data in the RAM array. A ninth bit is generated by the parity logic during normal write cycles and then checked during normal read cycles. If a parity error occurs, a nonmaskable interrupt is issued to the 8088.

The RAM array contains up to eight banks of dynamic RAM chips, which are 64 kilobits (kb) by 1 bit. Each bank of RAM contains nine chips: eight for data and one for parity.

The 4-kilobyte bootstrap ROM is used at system reset to run simple diagnostic tests and load the System Image from the cluster communications line. The bootstrap ROM can be suppressed by an external device to make other use of the upper 512-kilobyte address space, in which the ROM address space resides.

See the 8088 CPU Board schematic, Figure 3-3 above, in addition to the memory logic block diagram, during the following discussion.

Normal Read and Write Cycle Logic

As shown in the upper left corner of page 3 of Figure 3-3, MR- (Memory Read) and MW- (Memory Write) are ORed at gate 1C pin 3 to make CYC+ (Cycle). CYC+ indicates that one of the normal read or write cycles is being requested by the current bus master, either the 8088 or the 8257. When CYC+ is high, a normal cycle is started by pin 8 of gate 1D going low. Other conditions necessary for starting either cycle are:

- the current address must be in the lower 512 kilobytes of the address space (LA13+ must be low),
- a previous memory cycle cannot be in progress, that is, RDY- (Memory Ready) must be high, and
- a refresh cycle cannot be pending (gate 1D pin 12 must be low).

Gate 1D pin 8 being low sets the RS flip-flop 1A pin 8, NORMCYC+ (Normal Cycle). R17, R18, C5, and the gate 1A pin 10 Schmitt-trigger input ensure that the strobe at 1A pin 10 is long enough to preset flip-flop 1A.

NORMCYC- at decoder 4D pin 5 causes the RAS- (Row Address Strobe) for the appropriate row of RAMs to be generated. The RAS- signals, after being ORed with RFRAS- (Refresh Row Address Strobe) at gates 5D and 5C, go to the array of 64-kb

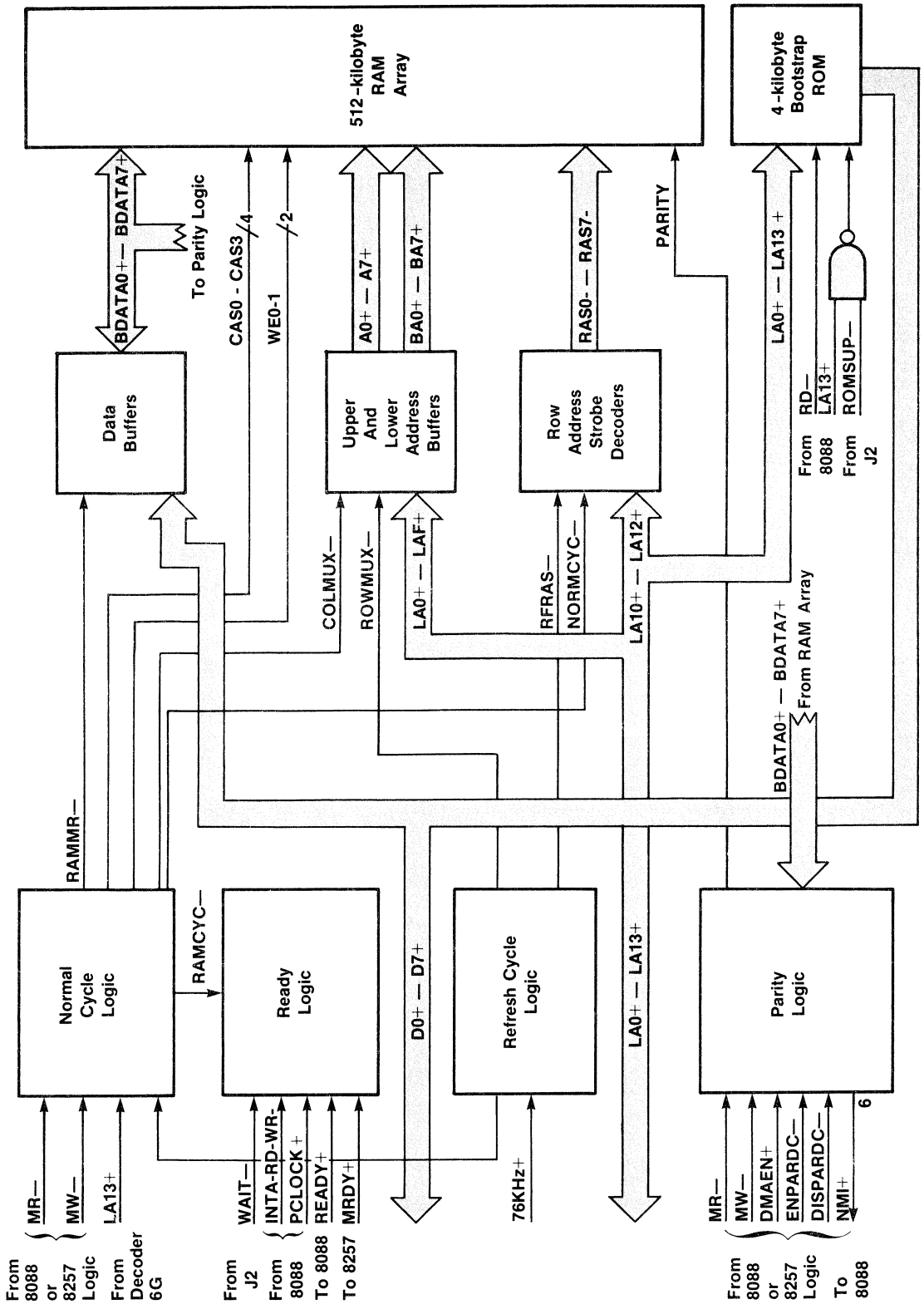


Figure 3-4. Memory Logic.

dynamic RAMs. Also, NORMCYC- causes the output of gate 4B pin 11 to go low, which feeds the digital delay line consisting of flip-flop 3B pin 9 and shift register 3C.

After a delay of 25-75 ns, gate 9E pin 3 activates COLMPX- (Column Multiplex) to switch the MA0+-MA7+ (Multiplexed Address) lines of the memory chips from the default row address to the column address. The buffers at 1E, 2E, and 6E form the multiplexer that selects the row, column, or refresh address, respectively. The MA lines go directly to one-half of the RAM array and are buffered at 5E for the other one-half of the RAM array.

Fifty nanoseconds after COLMPX- goes low, gate 3D pin 13 activates CAS+ (Column Address Strobe). CAS+ is buffered and inverted by 15E before going to the RAM array. Two hundred nanoseconds after CAS+ goes high, RDY- goes low at 3C pin 6 to indicate that the cycle finished and the RAM controller is ready for the 8088 or 8257 to go on with another cycle.

Data to and from the RAM array is buffered by transceiver 12E. The direction of the transceiver is established by RAMMR- (RAM Memory Read) at gate 2C pin 8. RAMMR- is usually high, causing D0+-D7+ to be driven to the DATA0+-DATA7+ (RAM Array Data) bus. When MR- is low at gate 2C pin 10 and RAM is being addressed (LA13+ = 0), gate 2C pin 8 asserts RAMMR-. WE0- and WE1- (Write Enable) are derived from MW- through gate 2A pin 8 and are buffered at 15E pins 18 and 16, respectively.

Refresh Logic

Every 13 μs, the RAM array requires a refresh cycle to maintain the content of the 64-kb dynamic RAMs. The refresh cycle differs from the normal cycle in that only eight row address bits and no column address bits are required.

The 76-kHz clock, 76KHZ+, sets the refresh pending flip-flop 2B pin 5 every 13 μs. This forces 2B pin 6 low, which prevents any new nonrefresh cycles from occurring at gate 1D pin 12.

At the next negative transition of the 9.8-MHz clock, and if NORMCYC- is high, RFADR+ (Refresh Address) at flip-flop 4C pin 9 is set. RFADR+ and RFADR- at 4C pin 8 cause address multiplexers 1E, 2E, and 6E to drive the refresh address from the two address counters at 7E and 8E.

At the next positive transition of the 9.8-MHz clock, refresh row address flip-flop 4C is set at pin 5. RFRAS- from 4C pin 6 causes all RAS signals to go low through OR gates 5C and 5D. In addition, gate 4B pin 11 causes the RAS signals to propagate through the shift register 3B pin 9 and flip-flop 3C. When the refresh cycle is complete, the signal RDY- from 2A pin 6 causes RFRDY- (Refresh Ready) to go low at gate 2C pin 6. RFRDY- indicates that the refresh cycle is complete and clears the refresh pending flip-flop 2B pin 4. Fifty nanoseconds later, the signal at shift register 3C pin 5 goes low, clearing the refresh address and RAS flip-flops at 4C pins 4 and 10. When RFADR- goes high, it increments the address for the next refresh cycle at 7E pin 2 and 8E pin 2.

Ready Logic

There are two handshake signals that go from the RAM controller to the two requesters: READY+ for the 8088, and MRDY+ (Memory Ready) for the 8257. These signals tell the requester that the cycle is complete and that the requester can go on to other cycles. As long as these signals are inactive, the requester inserts wait states and increases the time that MR- or MW- stays low.

All bus command strobes, WR-, RD-, and INTA- (Interrupt Acknowledge) are ORed at gate 1D pin 6 and sent to shift register 4E pin 18. Shift register 4E counts the number of processor clocks since the beginning of the command strobe. Shift register 4E's outputs, WAIT1+ and WAIT2+, go high, such that if the READY+ strobe is generated from them, one or two wait states, respectively, are generated.

The input to shift register 4E is an open-collector signal, WAIT-, that is also sent to the FDC or HDC Board interface connector at J2 pin 27. An external device can generate any number of wait states by asserting WAIT-. WAIT1+ is ANDed at gate 3E pin 3 to generate MRDY+. WAIT1+

ensures that all memory cycles have at least one wait state. When no memory cycle is in progress, RAMCYC- (RAM Cycle) is high, and the signal at gate 3E pin 8 generates a two wait-state ready. These two signals are ORed at gate 3D pin 1 to make the ready signal for the 8088, READY+. MEMOK+ (Memory OK), from gate 4B pin 6, is the other input to gate 3E pin 3, which generates MRDY+. MRDY+ is driven by the memory controller to indicate that the cycle is complete or will complete in one wait state. When the SLOW/FAST flip-flop 3B's pin 6 output, FAST+, is high and NORMCYC+ is high, MEMOK+ is asserted at gate 4B pin 6. As described above, NORMCYC+ indicates that a normal (nonrefresh) cycle is in progress.

The SLOW/FAST flip-flop is used in memory control arbitration. During a refresh cycle, the SLOW/FAST flip-flop is set to SLOW; during a normal cycle, it is set to FAST. This action causes all RAM accesses that are not interfered with by a refresh cycle to take exactly one wait state. The SLOW/FAST flip-flop is set to FAST at the beginning of each cycle by CYC+ going high at 3B pin 3, unless the preset RFRDY- indicates that a refresh cycle occurred since the beginning of the cycle. In this case, SLOW/FAST is set to SLOW and MEMOK+ is inhibited, thus adding extra wait states to the cycle.

When the cycle completes, NORMRDY- (Normal Cycle Ready) clears the SLOW/FAST flip-flop, which asserts FAST+ at 3B pin 6. FAST activates MEMOK+ and then READY+. NORMRDY- at gate 2C pin 11 is the AND function of both NORMCYC- and RDY- from the normal cycle logic. RFRDY- is the AND function of both RDY- and RFADR- at gate 2C pin 6. RFRDY- is used to preset the SLOW/FAST flip-flop to SLOW, and indicates that a refresh cycle is completing. Finally, READY+ for the 8088 is created by the OR of MRDY+ at gate 3D pin 3 and all other ready conditions, that is, input/output and ROM accesses, at gate 3D pin 2.

Parity Logic

To ensure data integrity, an even parity error detection scheme is used. Each data byte in the RAM array has a ninth bit associated with it, the parity bit. For any memory location, the total number of 1 bits in the 9-bit byte is always an even number. Therefore, when a location is read

and the number of 1 bits is found to be an odd number, the data (or possibly the parity bit) is in error. Once this error occurs, the status of the address bus is saved, and a nonmaskable interrupt is sent to the 8088 to invoke error-recovery software.

A single parity generator chip at 13E is used both to generate parity during memory writes and to check it during memory reads. The even output of the parity generator at 13E pin 5 is high, when the total number of 1 bits at its inputs is even.

During a write cycle, 13E pin 8 is forced low by gate 3D pin 10, since MR- is high at 3D pin 9. If the parity of the BDATA0+-BDATA7+ (Buffered RAM Data) bits is even, 13E pin 5 is high, indicating that a 0 should be written into the parity RAM. Correspondingly, if the parity of the data bit is odd, 13E pin 5 is low, indicating that a 1 should be written into the parity RAM. During a normal write cycle, the presence of MW- causes a parity bit to be driven to the parity RAM chips through an inverting tristate driver at 9H pin 18.

The parity enable flip-flop 2D pin 5 controls the parity circuitry during read cycles. It is cleared by either a manual or a power-up reset at flip-flop 2D pin 1. It is also cleared when the 8088 reads Port F4h. Parity checking is enabled when the 8088 reads Port F0h, which presets the parity enable flip-flop 2D pin 4.

As long as the parity enable flip-flop is not set, it holds the parity error flip-flop cleared at 2D pin 9. This mechanism is used both to disable parity errors and to clear existing ones. The parity error flip-flop generates a nonmaskable interrupt if a parity error occurs. If parity is disabled, a nonmaskable interrupt cannot occur.

When enabled, the parity error detection circuitry samples the output of the parity generator chip at the end of every RAM read to determine if an error occurred. Gate 3D pin 10 inverts the parity bit coming from the byte being read and sends it to 13E pin 8. The pin 5 output of 13E is therefore high if odd parity was read from the 9-bit byte and an error occurred.

RAMMR- at gate 2C pin 8 is generated for memory reads when LA13+ and MR- are both low. When MR- goes high, the error flip-flop 2D pin 12 samples 13E pin 5. When a parity error occurs, 2D pin 9 is set. The preset of the parity error flip-flop is connected to its own Q- output, pin 8. Therefore, the only way to clear the error condition is to disable parity, which causes the error flip-flop to clear at 2D pin 13.

The Q output of the parity error flip-flop, 2D pin 9, is connected to NMI+ (Nonmaskable Interrupt), which generates a nonmaskable interrupt to the 8088. In addition, NMI+ causes the status of the address bus to be latched to the parity error registers at 4H, 5H, and 6H (see page 2 of Figure 3-3 above). Bit 4 of 6H is high if the cycle was for DMA (DMAEN+ is high) or low if the read was for the 8088.

The nonmaskable interrupt causes the 8088 to jump into error-recovery software, which uses the parity error registers to determine the error address. Note that if an access is made to a memory location in the lower 512 kilobytes of the memory space, and the location contains no chips, FFh is read from the location and a parity error results.

RAM Array

As shown on page 6 of Figure 3-3 above, the RAM array contains up to eight banks of nine chips each: one chip for each data bit and one chip for the parity bit. The correspondence of chip locations to memory bits is:

Address Range	Bit 7	6	5	4	3	2	1	0	P
00000-0FFFFh	6A	7A	8A	9A	10A	11A	12A	13A	14A
10000-1FFFFh	15A	16A	17A	18A	19A	20A	21A	22A	23A
20000-2FFFFh	6B	7B	8B	9B	10B	11B	12B	13B	14B
30000-3FFFFh	15B	16B	17B	18B	19B	20B	21B	22B	23B
40000-4FFFFh	6C	7C	8C	9C	10C	11C	12C	13C	14C
50000-5FFFFh	15C	16C	17C	18C	19C	20C	21C	22C	23C
60000-6FFFFh	6D	7D	8D	9D	10D	11D	12D	13D	14D
70000-7FFFFh	15D	16D	17D	18D	19D	20D	21D	22D	23D

Bootstrap ROM

The 4-kilobyte bootstrap ROM runs simple diagnostic tests and loads the CTOS System Image from the cluster communications line. When the workstation receives either a manual or power-up reset, Register CS in the 8088 is set to FFFFh and Register IP is set to 0 before program execution begins. This causes the first instruction to be fetched from location FFFF:0. The ROM address space is arranged so that FFFF:0 refers to an address in the bootstrap ROM.

As shown on page 2 of Figure 3-3, when an address is in the upper half of the address space (LA13+ is high), gate 1A pin 3 selects the bootstrap ROM at 3H. When RD- goes low, the bootstrap ROM outputs are enabled at 3H pin 20. This allows data at the ROM's outputs onto the D0+-D7+ data bus lines.

ROMSUP- (ROM Suppress) is used by the FDC and HDC Boards to suppress the bootstrap ROM for parts of the upper 512 kilobytes of the address space. Those parts of the address space can be used for other purposes, such as for additional memory or memory-mapped input/output devices. Otherwise, any memory location read above the boundary of 512 kilobytes refers to the bootstrap ROM. Note that since the bootstrap ROM is only 4 kilobytes, it can be referenced at 128 different places in the upper 512-kilobyte address space.

Direct Memory Access Logic

Direct Memory Access (DMA) transfers data between memory and an input/output device without involving the 8088. The four-channel Intel 8257 DMA controller is responsible for getting control of the bus from the 8088 and generating the memory address and bus command strobes for the DMA transfers. The data is transferred directly between the memory and the input/output device.

Figure 3-5 below shows the functional blocks of the DMA logic. Also see the 8088 CPU Board schematic, Figure 3-3 above, during the following discussion.

The four DMA channels are assigned as listed below:

Channel	Priority	Device	Request	Acknowledge
0	High	FDC or HDC Board	EXTRQ+	EXTACK-
1	Medium	Communications	COMMRQ+	COMMACK-
2	Low	Video	VIDRQ+	VIDACK-
3	---	The Channel 3 registers are used to auto-initialize Channel 2.		

8257 Programming

The 8257 must be programmed with input and output instructions from the 8088, as described above under "Direct Memory Access" in the "Architecture" section. The "Architecture" section also lists the steps involved in a DMA transfer.

As shown on page 2 of Figure 3-3, the 8088 programs the 8257 via the data bus lines, D0+-D7+. When one of the registers within the 8257 is addressed, 8257CS- (8257 Chip Select) is asserted at 1G pin 11. The actual transfer occurs when the 8088 asserts either RD- at 1G pin 1 or WR- at 1G pin 2 while 8257CS- is active. DMA is never in progress while the 8257 is being programmed. A high DMAEN- from inverter 9H pin 9 causes the LA0+-LA7+ address lines from the 8088 to be driven through transceiver 2G to the 8257. These address lines are used to select registers within the 8257. The input/output read and write pins of the 8257, 1G pin 1 and 1G pin 2, respectively, are bidirectional. They are inputs during programming of the 8257 and outputs when HLDA+ is high.

DMA Operations

The 8257 and the 8088 are the two sources for the LA0+-LA13+ address lines on the CPU Board. During non-DMA bus cycles (HLDA+ is low), the address is driven by the tristate latches at 3G, 5G, and 6G. After HLDA+ goes active, the 8257 drives bits 8 through F of the memory address onto the data bus lines, D0+-D7+. Simultaneously, the 8257 asserts ADSTB+ (Address Strobe) output at 1G pin 8, which loads the address bits into the latch at 4G.

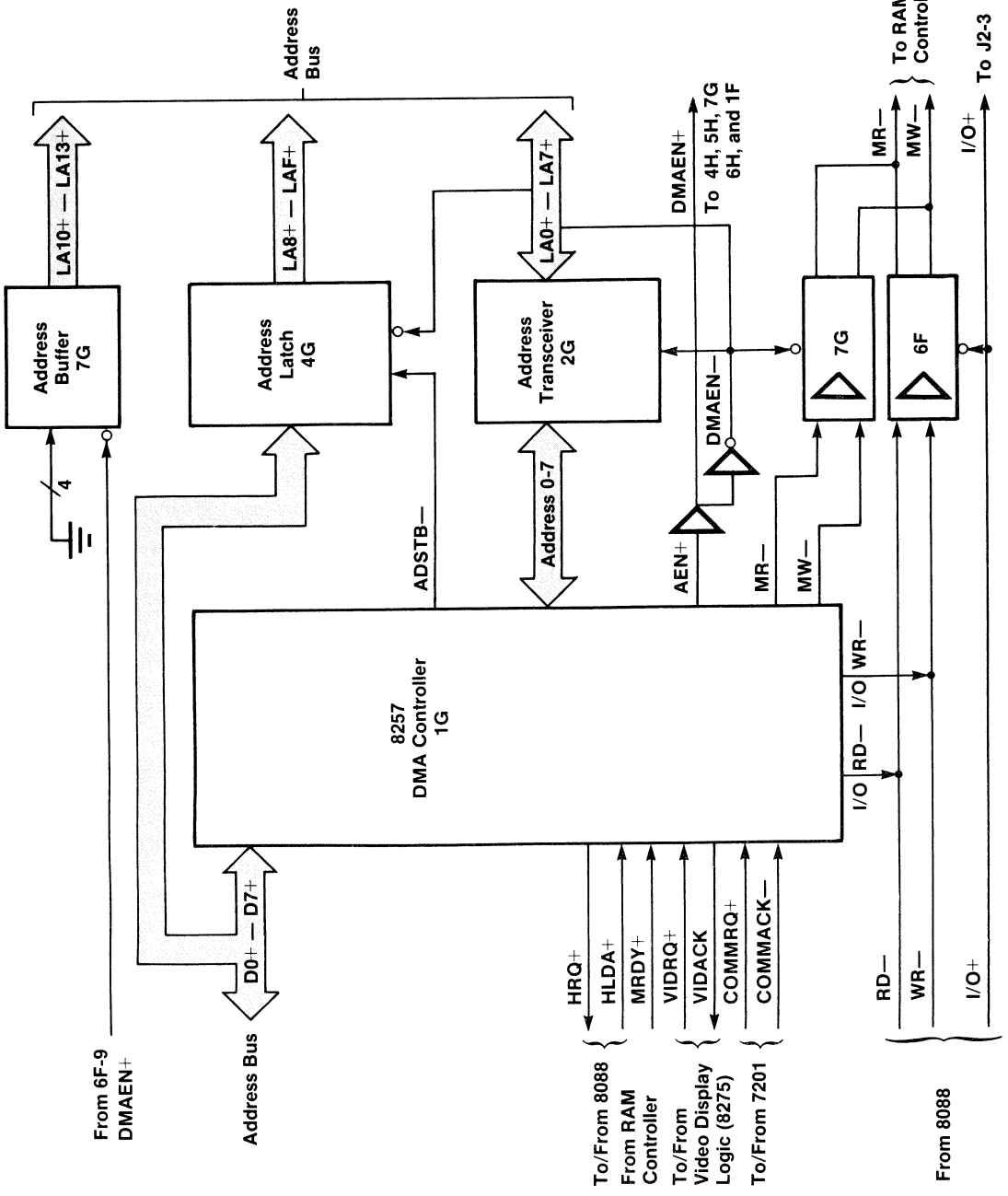


Figure 3-5. DMA Logic.

Next, the 8257 drives LA0+-LA7+ on its address lines to transceiver 2G and asserts AEN+ (Address Enable) at 1G pin 9 to enable the address drivers. AEN+ is buffered and inverted at 6F pin 9 and 9H pin 9 to make DMAEN+ and DMAEN-. DMAEN+ disables the 8088 address drivers 3G, 5G, and 6G, and DMAEN- enables the DMA address from the transceiver at 2G and drivers 7G and 4G. During programming, the address lines of the 8257 are inputs. When HLDA- is low from the 8088, the adress lines are outputs. Note that during a DMA cycle, the drivers at 7G pins 3, 5, 7, and 9 drive address lines LA10+-LA13+ low, which places all DMA accesses in the first 64 kilobytes of RAM. The FDC or HDC Board asserts ADRDIS- (Address Disable) to disable 7G. The FDC or HDC Board can then supply the four high-order address lines, LA10+-LA13+.

When HLDA+ is low, the memory read and write pins of the 8257, 1G pins 3 and 4, are not used. When HLDA+ is high, a DMA cycle is in progress and all four pins are outputs. The input/output read and write strobes access the input/output device, and the memory read and write strobes access the memory.

The signals MR- and MW- can originate from the 8257 through drivers 7G pins 16 and 18 or from the 8088 through drivers 6F pins 12 and 14. When the 8088 is doing memory cycles, the I/O+ (Input/Output) signal from the 8088 at 5F pin 28 is low. During input/output, the 8088 drives I/O+ high. During DMA cycles, the 8088 does not drive I/O+; the pullup resistor at RP2 pin 8 pulls I/O+ high. The 6F drivers are enabled when I/O+ is low during non-DMA cycles, and the 7G drivers are enabled by DMAEN-.

Input/output reads and writes are always controlled by RD- and WR-. The 8088 RD- and WR- pins are connected in parallel with the 8257 IORD- (Input/Output Read) and IOWR- (Input/Output Write) pins. The 8088 drives them only when HLDA+ is low, and the 8257 drives them only when HLDA+ is high. During 8088 input/output accesses, the address decoders 1F and 2H select the input/output device for the transfer. During DMA, DMAEN+ disables the address decoders at 1F pin 4, and the device acknowledge signals from the 8257, COMMACK- (Communications Acknowledge), VIDACK- (Video Acknowledge), and EXTACK-

(External DMA Acknowledge), select the input/output device.

Cluster Communications Logic

Cluster communications are based on an NEC 7201 (or Intel 8274) Multi-Protocol Serial Controller (MPSC). Although the 7201 has two channels, only Channel A is used for cluster communications. Channel B is used as the keyboard interface.

Figure 3-6 below shows the functional blocks of the cluster communications logic. Also see the 8088 CPU Board schematic, Figure 3-3 above, during the following discussion.

7201 Programming

As shown on page 4 of Figure 3-3, the 7201 is programmed through the eight data bus lines, D0+-D7+ when SIOCS- (Serial Input/Output Chip Select) is low at 1F pin 12, and RD- or WR- is low at 8G pins 22 or 21, respectively. LA1+ and LA2+ at 8G pins 24 and 25 are used to select the individual registers within the 7201. Interrupt acknowledges and the use of INTA- at 8G pin 27 are described in "Interrupt Logic" below.

Cluster communications operate under the control of DMA Channel 1. Once programmed, the 7201 asserts one of two signals to transfer data to or from memory, either COMMTRQ+ (Communications Transmit Request) at 8G pin 11, or COMMRRQ+ (Communications Receive Request) at 8G pin 32. Gate 2C pin 3 ORs the two requests to generate COMMRQ+ (Communications Request). COMMRQ+ is sent to the 8257 to transfer receive data from the data bus when RD- or WR- goes low. Once the transfer is complete, the 7201 takes COMMRQ+ low.

Communications Signals

The cluster workstations are connected by four wires: two for data and two for the transmit clock. Each pair consists of two RS-422 differential lines: one positive signal and one complement signal. All data transmission is half-duplex, since there is only a single data pair. The communications line is multidrop, that is, whichever workstation is driving the line

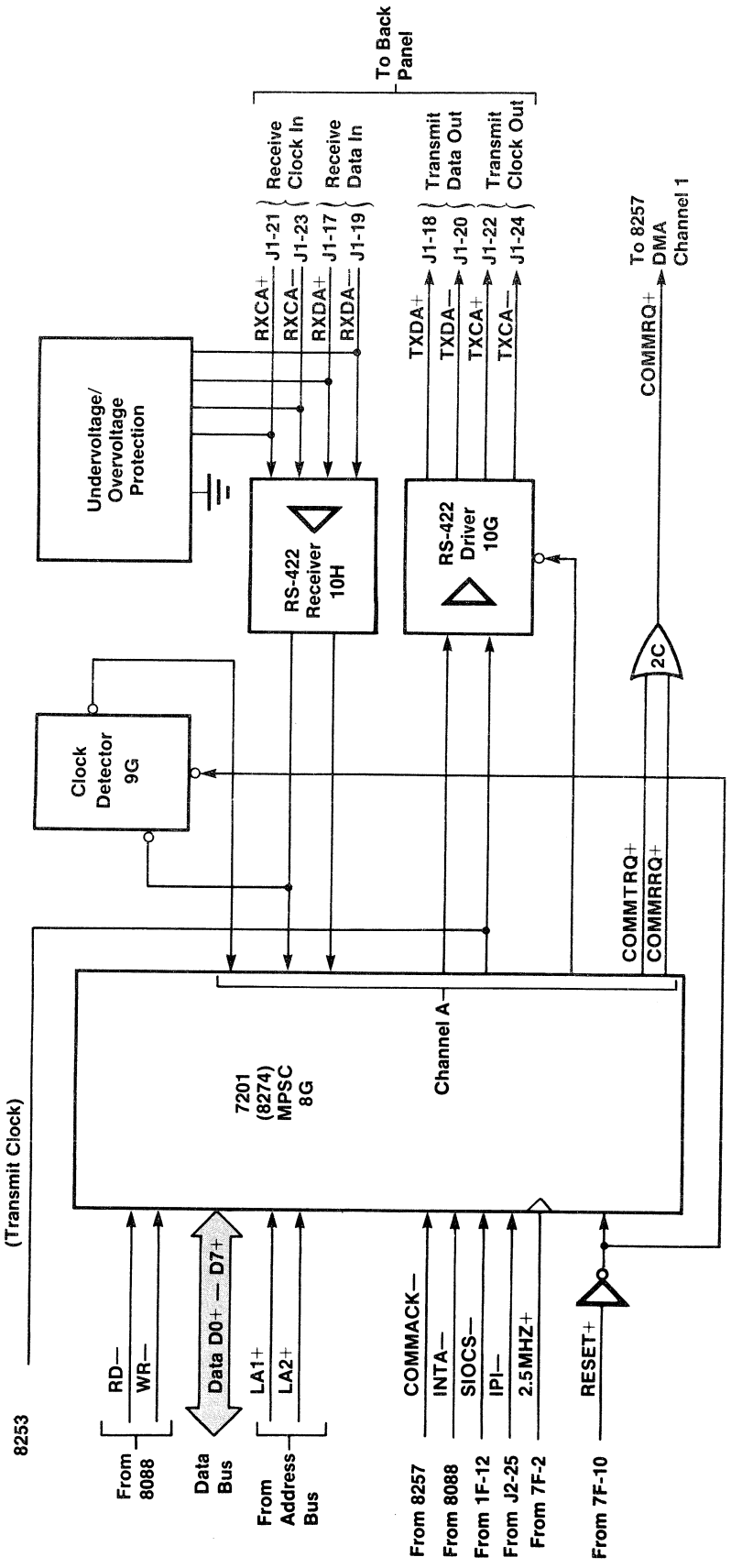


Figure 3-6. Cluster Communications Logic.

always drives both the data and clock signals. All receivers on the cluster use the clock that is currently on the communications line, never an internal clock.

The four cluster signals are terminated in series with 1-kilohm resistors R9, R10, R11, and R12. Diodes CR1-CR9 provide overvoltage and undervoltage protection for the receivers by shunting those voltages to ground. Overvoltages go through switching diodes and then through the reverse-biased 5.1-V Zener diode CR1. Undervoltages go directly through the switching diodes to ground.

The receive clock comes onto the CPU Board at J1 pins 21 and 23 as RXCA+ and RXCA- (Receive Clock Channel A). The receiver at 10H converts them to a single TTL receive clock signal at 10H pin 11. This signal is used to clock the receive data into the 7201 at 8G pin 35. It also goes to the clock-detect one-shot at 9G pin 5. The one-shot is used to determine when the line is being driven; its output drives the Channel A DCDA- (Carrier Detect) input to the 7201. When there is no clock present on the communications line, the one-shot returns to its stable state and deactivates carrier detect.

Receive data comes from J1 pins 17 and 19 as RXDA+ and RXDA- (Receive Data Channel A). They are received and converted to a single TTL receive data signal by the RS-422 receiver at 10H pin 13. This signal is connected to the receive data input of the 7201 at 8G pin 34.

The transmit clock is generated by Counter 1 of the 8253, described above in "Architecture" under "Cluster Communications Baud Rate." The transmit clock goes to the 7201 to time the transmit data at 8G pin 36. It also goes to the RS-422 drivers at 10G pin 9. Transmit data goes directly from the 7201 to the transmit driver at 10G pin 15. The drivers are tristate devices enabled by the Channel A request-to-send output of the 7201, 8G pin 38.

Keyboard Interface Logic

Channel B of the 7201 is used with a standard asynchronous protocol to communicate between the 7201 and the keyboard. Figure 3-7 below shows

the functional blocks of the keyboard interface logic. Also see page 4 of Figure 3-3 above, the 8088 CPU Board schematic, during the following discussion, which addresses the subject on a component level.

The 76KHZ+ clock signal is sent to 7201 8G pins 4 and 7. This provides for communications with the keyboard at 1200 baud when the divide-by-64 mode is selected in the 7201. Transmit data is sent from the 7201 to the keyboard through the buffer at 9H pin 3. Receive data is received from the keyboard at 9H pin 15 and, after it is buffered, is sent to the receive data input at 8G pin 9.

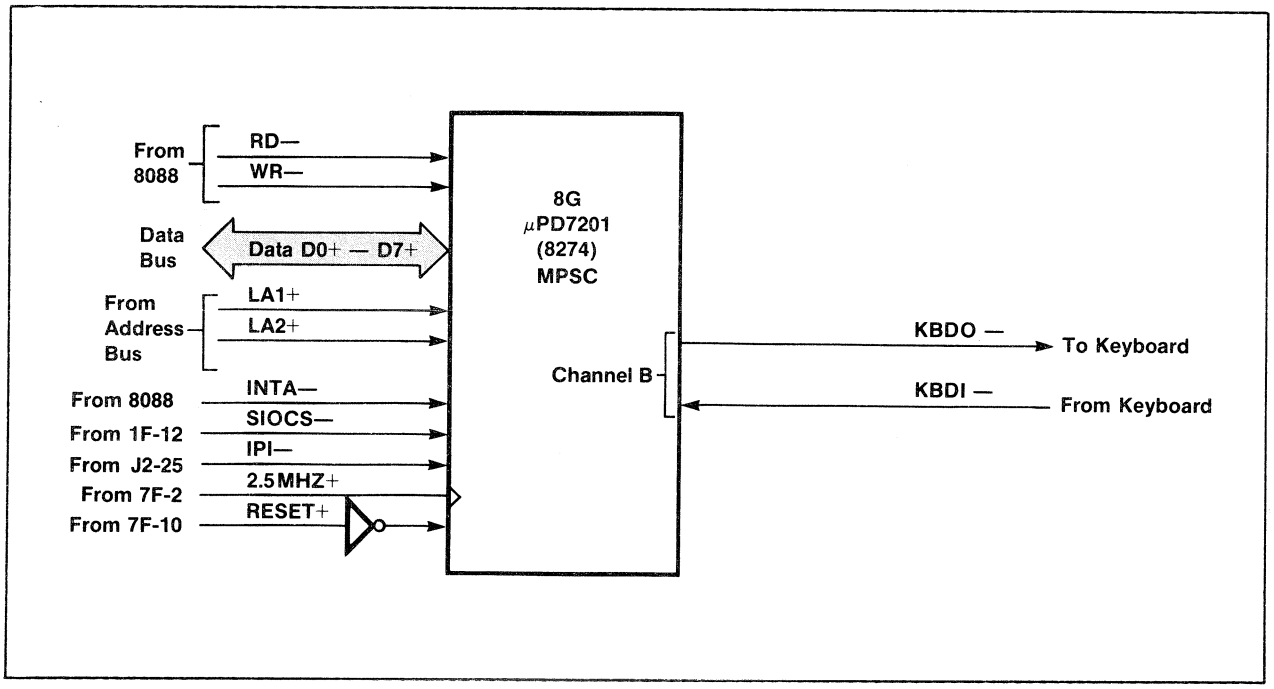


Figure 3-7. Keyboard Interface Logic.

Timer Logic and Speaker Interface

As shown on page 4 of Figure 3-3 above, the 8088 CPU Board schematic, the Intel 8253 timer at 7H is a programmable counter/timer with three fully independent 16-bit channels. Figure 3-8 shows the functional blocks of the timer logic and speaker interface.

8253 Programming

The three counter channels of the 8253 are used as the tone generator, cluster communications clock, and programmable timer interrupt source. The assignment and input frequency of each counter are:

Counter	Assignment	Input Clock Frequency
0	Tone generator	1.23 MHz
1	Cluster communications clock	1.23 MHz
2	Timer interrupt	76 kHz

Eight data bus lines, D0+-D7+, are connected to the 8253 for communications with the 8088. During input/output access to the 8253, the signal 8253CS- (8253 Chip Select) from the address decoder 1F (on page 2 of Figure 3-3 above) selects the timer. The actual transfer of data from the 8088 to the 8253 to program the timer channels occurs when either RD- at 7H pin 22, or WR- at 7H pin 23 goes low. Address lines LA1+ and LA2+ are used to select a particular register within the 8253. The programming information for the 8253 is described in the "Architecture" section for the particular channel used.

Speaker Interface

The speaker frequency is determined by Counter 0 of the 8253 timer, as described in the section above and in the "Architecture" section under "Speaker Interface." As shown on page 4 of Figure 3-3 above, the signal from the 8253 is amplified by R6, R7, and Q1 and then shaped by R8 and C4 before going to the speaker through J1 pin 8.

Interrupt Logic

Interrupts on the 8088 CPU Board are controlled by the 8088 microprocessor and a 7201 MPSC, both on the CPU Board, and by an 8259A interrupt controller on the FDC or HDC Board. All

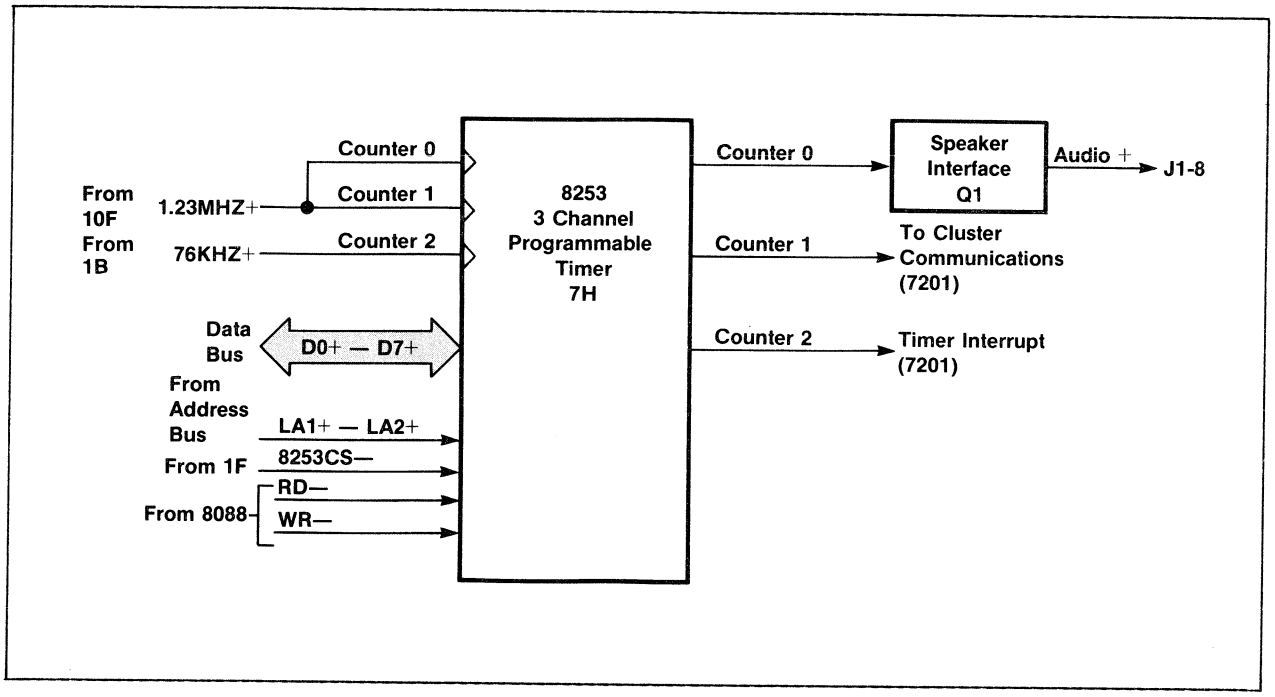


Figure 3-8. Timer Logic and Speaker Interface.

interrupts in the 8088 are maskable in software. The 7201 provides individual masking, interrupt vector generation, and priority setting. The 8259A services CPU Board interrupts along with interrupts from FDC or HDC Board sources, such as the disk controller and RS-232-C communications. Interrupts passing through the 8259A from the 8088 CPU Board are given the highest priority (see "Board Bus Interface and Interrupt Control Logic" for the FDC or HDC Board below).

The sources for interrupts on the CPU Board are:

- the keyboard interface,
- the cluster communications interface, and
- Counter 2 of the 8253 counter/timer chip.

Programming the 7201 is described above in the "Architecture" section under "Cluster Communications."

Figure 3-9 below shows the functional blocks of the interrupt logic. Also see page 4 of Figure 3-3 above, the 8088 CPU Board schematic, during the following discussion.

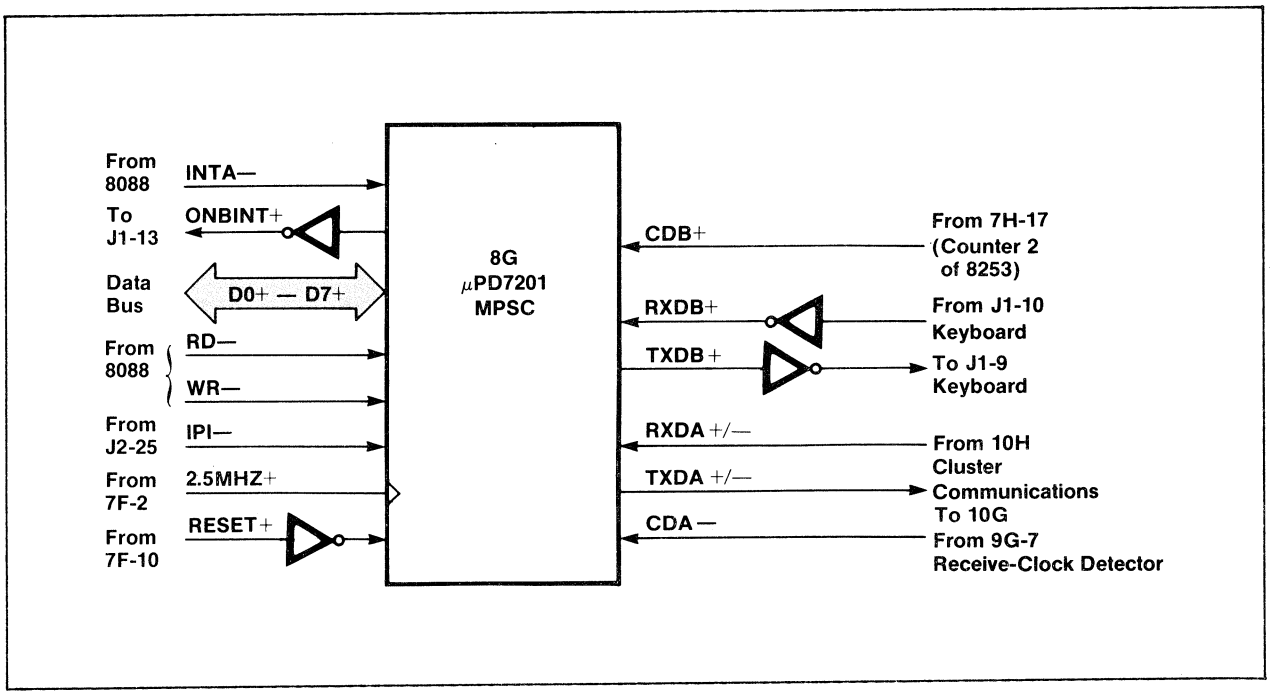


Figure 3-9. Interrupt Logic.

The Counter 2 output of the 8253 timer chip is connected to the DCDB+ (Carrier Detect Channel B) input of the 7201 at 8G pin 5. Counter 2 is used as a source of general purpose interrupts for the 8088 through Channel B of the 7201. The other two interrupt sources are handled internally in the 7201.

The 7201 asserts its interrupt output at 8G pin 28 to signal an interrupt request to the 8088. The interrupt signal is buffered and inverted at 8J pin 8 to make ONBDINT+ (On-Board Interrupt). ONBDINT+ is sent to the pin 19 INT1+ (Interrupt Priority 1) input of the 8259A on the FDC or HDC Board. Any 8088 CPU Board interrupt is assigned the highest priority. The resulting interrupt request is sent to the 8088 as INTR+ (Interrupt Request) at pin 14 of the J1 Motherboard connector.

The 8088 asserts INTA- twice at 5F pin 24 to acknowledge each interrupt. The first pulse is used by the 8259A on the FDC or HDC Board to assign the interrupt priority. The second pulse is used to read the interrupt vector from the 7201 to the 8088.

INTA- is connected to the 7201 at 8G pin 27. The 7201 determines the proper vector during the first of a pair of INTA- pulses and drives the data bus lines, D0+-D7+, with the vector during the second pulse. The 8259A on the FDC or HDC Board can drive the IPI- (Interrupt Priority In) signal low at J2 pin 25 to cause the 7201 to send its own interrupt vector to the 8088. IPI- is connected to the 7201 at 8G pin 29.

Video Display Control Logic

The video display control logic is used to interface the 8088 and 8257 to the CRT Deflection Board. It provides control of:

- the video display raster;
- video display refresh;
- font ROM output to pixel conversion;
- half-bit shift;
- full- and half-bright video display; and
- reverse video, blanking, and blinking.

The video display control logic is based on the Intel 8275 CRT controller and uses DMA Channels 2 and 3 to refresh the video display from memory. Figure 3-10 shows the functional blocks of the video display control logic. Also see the 8088 CPU Board schematic, Figure 3-3 above, during the following discussion.

8275 Programming

As shown on page 5 of Figure 3-3 above, the 8275 is programmed from data lines D0+-D7+ when 8275CS- (8275 Chip Select) is low and either RD- or WR- is low. Address line LA1+ is used to select among the internal registers in the 8275. Further programming information is

described above in the "Architecture" section under "Direct Memory Access" and "Video Display Control."

3301 Programming

An NEC 3301 is used as a second source for the Intel 8275. A set of socket pins next to the 8275 is used for mounting the 3301. The software requirements of the 3301 are incompatible with those of the 8275. See the 1981 Catalog published by NEC Microcomputers, Inc., for programming information.

Video DMA

After it is programmed, the 8275 asserts VIDRQ+ (Video DMA Request) at 11G pin 5 when it requires data. VIDRQ+ goes to the 8257 at 1G (page 2 of Figure 3-3) to request a DMA cycle. The 8257 responds by asserting VIDACK- (Video DMA Acknowledge). After the 8275 generates RD-, it asserts WR- to transfer the data to the 8275 from data bus lines D0+-D7+.

Raster

The video display raster is controlled by the 8275 with the HRTC+ (Horizontal Retrace) output at 11G pin 7 and the VRTC+ (Vertical Retrace) output at 11G pin 8. HRTC+ is sent to the RS-422 differential driver 15H which drives this signal as HORDR+ and HORDR- (Horizontal Drive) to the CRT Deflection Board. The vertical retrace signal is pipelined once at 12G pin 9 before being driven to the video display by 15H as VERDR+ and VERDR- (Vertical Drive).

Refresh

The 8275 has two row buffers that contain the character codes for the current row being refreshed and the next row to be refreshed. It receives the character codes via DMA as described above. Each character requires 11 horizontal scan lines to display. The conversion from the character codes to pixel information is done by the font ROM at 13H. The conversion is based on the character code and the current raster line

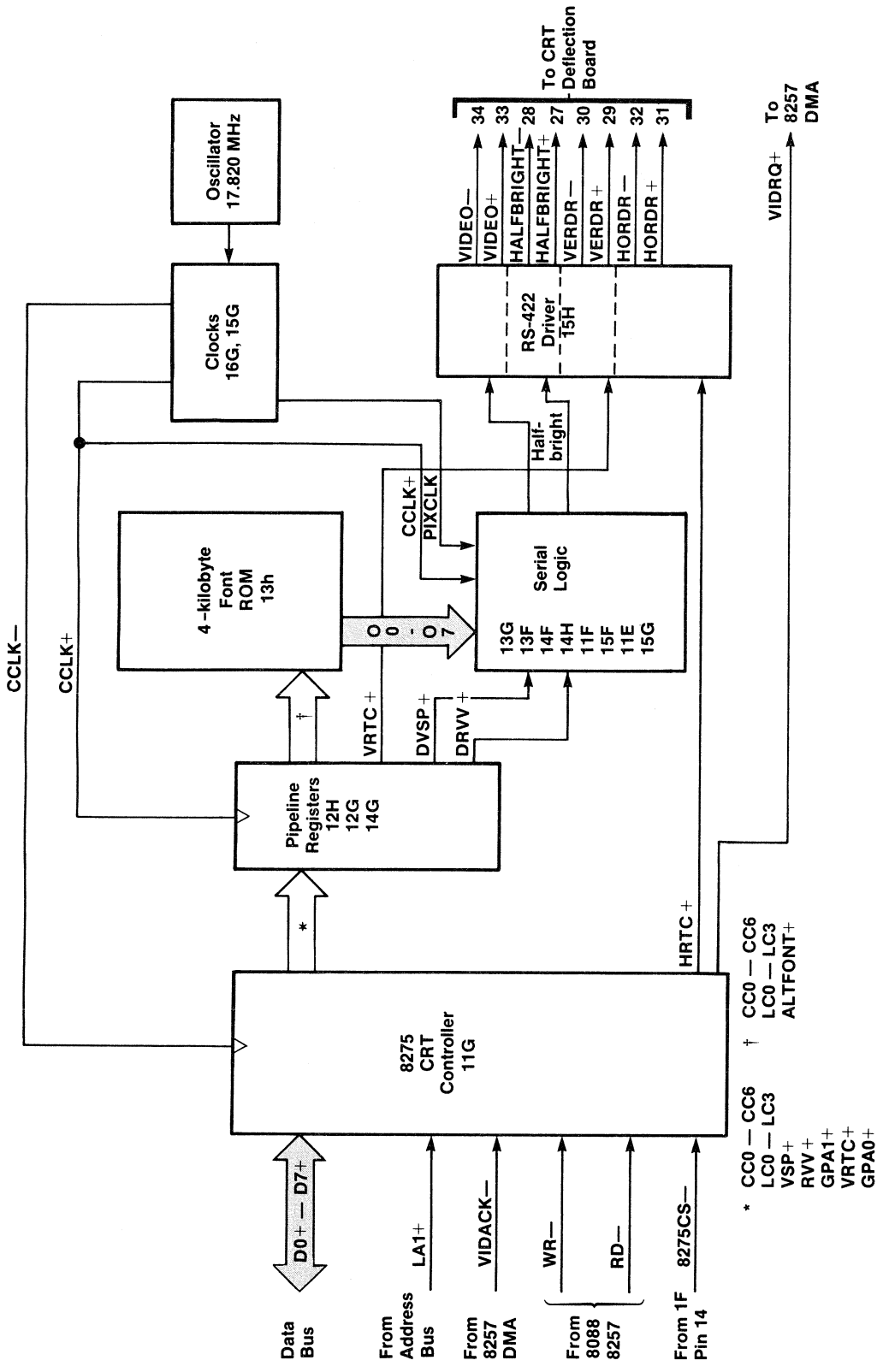


Figure 3-10. Video Display Control Logic.

number within the character row that is being refreshed. Thus, each character code read into the 8275 is presented to the font ROM as an address 11 times, each time with a different raster line number.

In addition to the character codes, the video display refresh buffer contains field attributes that affect the appearance of the displayed characters. The 8275 processes these field attributes and generates the appropriate control outputs.

Pipeline registers 12G, 12H, 14G, 13F, and 14F are used to give the font ROM the longest possible access time and to ensure that propagation delays do not affect the video display quality.

The character codes from the 8275 are driven from 11G pins 23 through 29 to pipeline register 12H. They are then used to directly address the font ROM, 13H. The raster line number is generated by the 8275 on 11G pins 1 through 4. These signals are pipelined at 12H, 12G, and also address the font ROM.

The 8275's GPA0+ (General Purpose Attribute 0) is used to select the alternate font. Pin 33 of the 8275 is high when GPA0 is invoked. After pipelining at 14G pin 7, the attribute becomes the high-order address bit of the font ROM. The organization of the font ROM is described above in the "Architecture" section under "Video Display Control."

There are two types of characters in the font ROM: line-drawing and normal. Line-drawing characters must fill the rightmost and/or leftmost pixel of the 9-by-11-pixel character cell. As shown in Figure 3-11 below, normal characters fill the inner 7-by-11-pixel character cell. The last (highest-numbered) 64 characters in the 256-character font ROM are the line-drawing characters.

Characters are generated one raster line (9 pixels) at a time by the font ROM. They are converted to the bit-serial pixel data by the shift register 13G with the ninth bit coming from 14F pin 15. The first pixel shifted out corresponds to the leftmost pixel in the cell as

it appears on the video display. The correspondence between displayed pixels and shift register inputs is:

Pixel →	1 Left	2	3	4	5	6	7	8	9 Right
Input →	13G 14	13G 12	13G 11	13G 10	13G 5	13G 4	13G 3	13G 2	14F 15

Font ROM Output to Pixel Conversion

The serialization of the font ROM output to bit-serial pixel information depends on whether a line-drawing character is displayed and on the status of the underline attribute. When a line-drawing character is output, gate 11E pin 6 is high. This allows an alternate set of buffers in 14H to direct the O0-O2 ROM outputs to the inputs of shift register 13G in a different order. Figures 3-11 and 3-12 below show the order in which the bits are shifted out of 13G to the CRT Deflection Board for both a normal and a line-drawing character.

Underlines and Normal Characters. The CPU Board uses the reverse video attribute of the 8275 to generate underlines because the underline capabilities of the 8275 are incompatible with the video display control logic. When the RVV+ (Reverse Video) attribute pin of the 8275 at 11G pin 36 is high and the raster line 9 is being refreshed, gate 11E pin 8 is driven high, which causes an underline to be displayed. This underline control signal is pipelined at 12G pin 5. The signal at 12G pin 5 disables the font ROM at 13H pins 18 and 20 and thus forces its outputs all high. Also with normal characters, the underline control signal (through tristate buffers 14H pins 3 and 5), forces the outer two pixels of the 9-by-11-pixel character cell high.

For normal characters not underlined, this same path forces the outer two pixels low; the other seven pixels of the cell go directly from the font ROM to 13G, with the low-order bits at 13H pins 9 and 10 buffered at 14H pins 7 and 9.

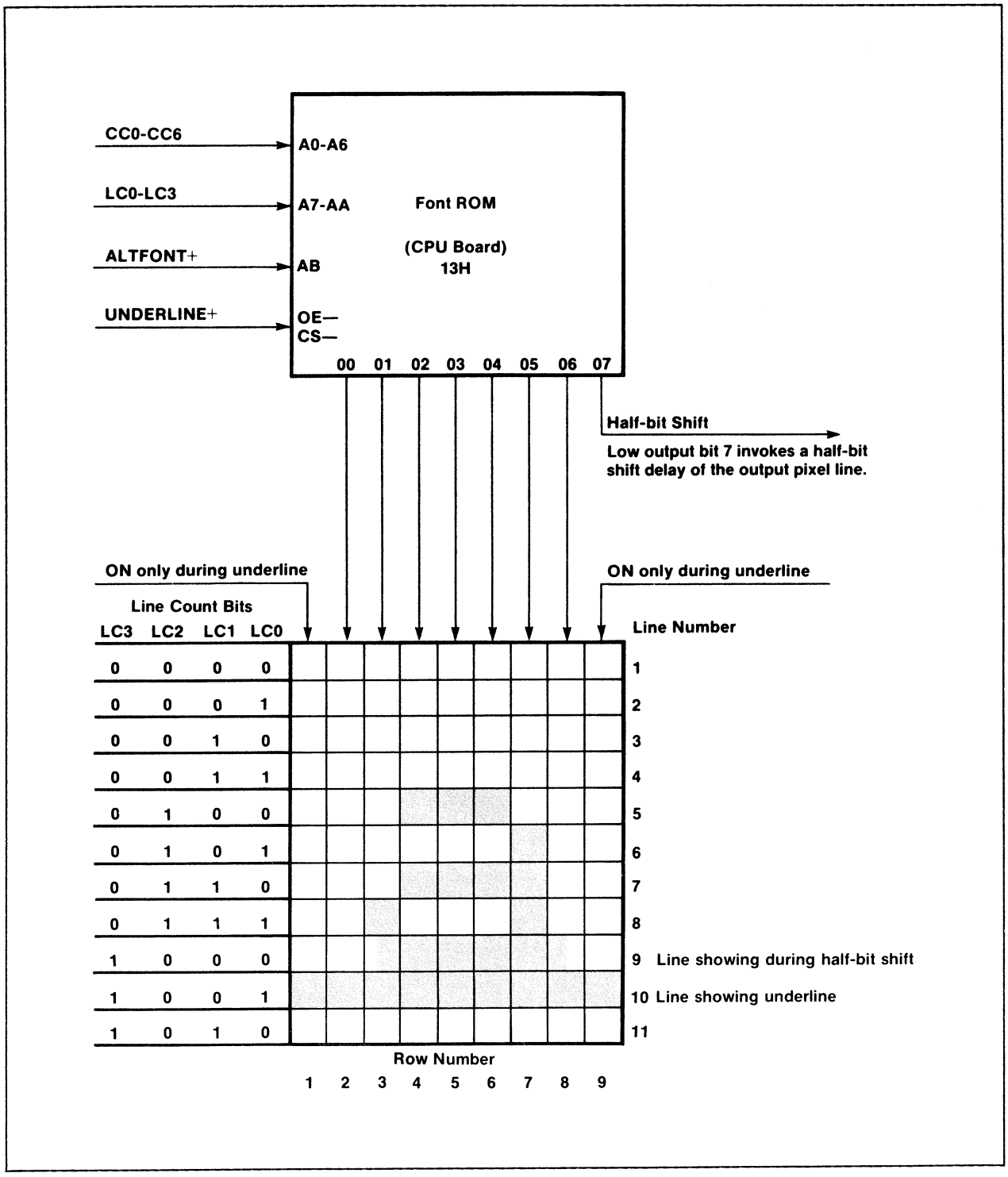


Figure 3-11. Generation of Normal Character 61h (Gate 11E Pin 6 = 0).

Line-Drawing Characters. For line-drawing characters, the high leftmost pixel is driven by 14H pin 16 from output bit 0 of the font ROM. The next two pixels are driven by 14H pins 12 and 18 from output bit 2 of the font ROM; the rightmost pixel is driven by 14H pin 14 from output bit 1 of the font ROM. The other five pixels come directly from the font ROM in the same manner as the normal characters.

The line-drawing mode is enabled by gate 11E pin 6 when the alternate font attribute is on; that is, ALTFONT+ (Alternate Font) is high, and the high-order character code bit is high at 12H pin 2. For either type of character, the bit-serial pixel data is shifted out of 13G pin 13 at the pixel clock frequency of 17.820 MHz.

Half-Bit Shift

Output bit 7 of the font ROM is used to select half-bit shift. Half-bit shift delays all pixels of one raster line of a particular character in the font. This allows characters to have overlapped pixels, smoother characters, and better centering. The shifted line of pixels turns on and off at the falling, rather than at the rising, edge of the pixel clock so that the pixels are delayed by a half-pixel period.

The O7 output of the font ROM at 13H pin 17 is pipelined at 13F pins 15 and 14. When enabled, the pixel data from 13G pin 13 goes through 12F pin 11 and, when disabled, through 12F pin 3. The two streams of data are pipelined at 14F pin 5 for the shifted bits and 14F pin 2 for the unshifted ones. The exclusive-OR gate at 15F ORs the shifted and nonshifted pixel data at 15F pin 11.

Brightness

The video display has a half-bright mode under software control as a field attribute (field attributes are fully described in the "Architecture" section). When the video display data is to be half-bright, the 8275 asserts HLGT+ (Highlight) at 11G pin 32. HLGT+ is pipelined twice by CCLK+ (Character Clock) at 14G pins 10 and 15. From there, HLGT+ is pipelined to PXCLK+ (Pixel Clock) through 14F pin 12. Finally, HLGT+

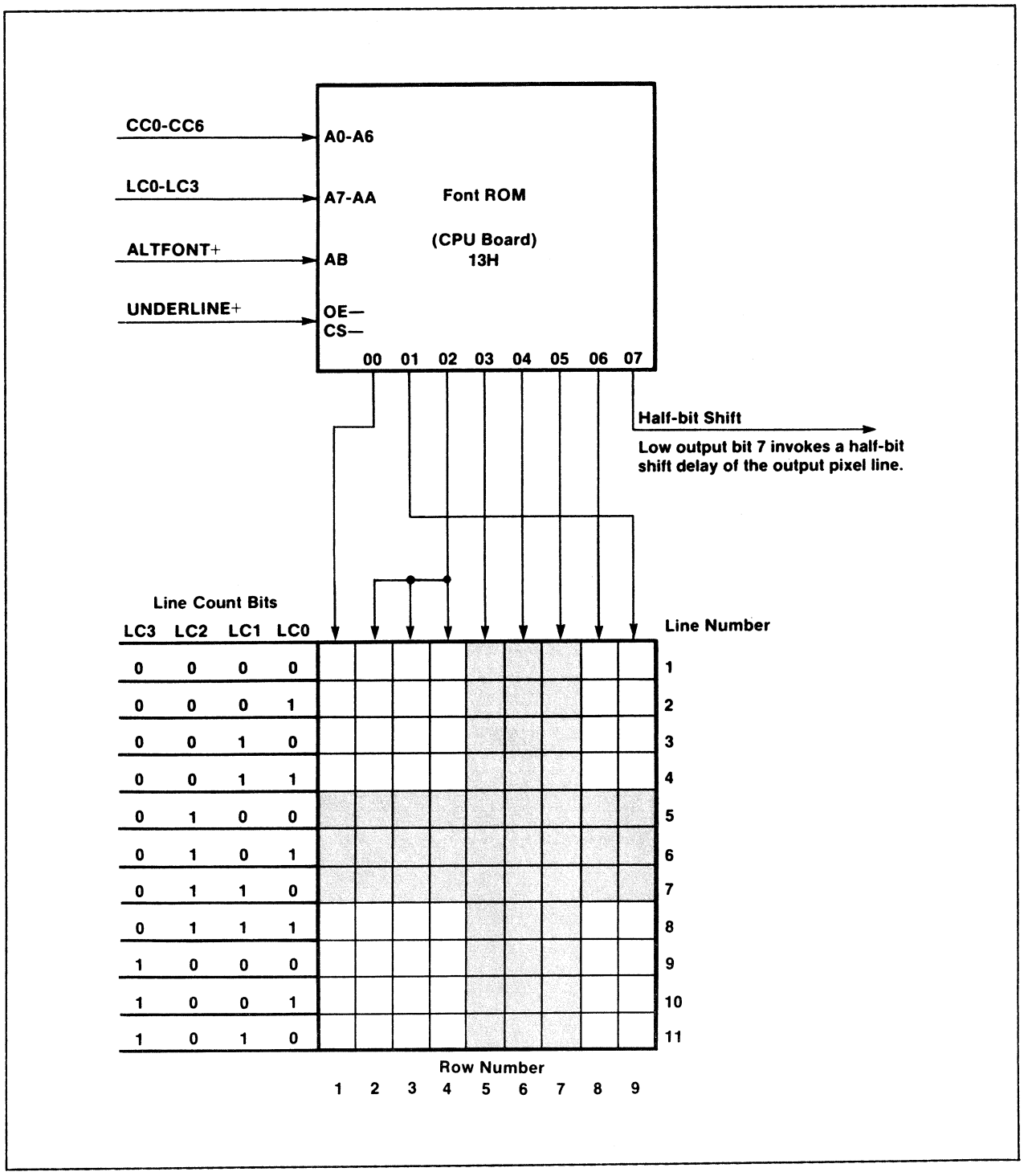


Figure 3-12. Generation of Line-Drawing Character C3h (Gate 11E Pin 6 = 1).

is sent to gate 15H pin 1 through gates 15F pin 3 and 11E pin 12 to provide a sufficient delay. HLGT+ is then buffered to the video display as HALFBRIGHT+ and HALFBRIGHT- by driver 15H pins 2 and 3, respectively.

Reverse, Blanking, and Blinking

Reverse video is controlled by the 8275's GPA1+ (General Purpose Attribute 1). GPA1+ at 11G pin 34 is pipelined at 12G pin 12, 13F pin 7, and 14F pin 6. GPA1+ is then exclusive-ORed with the pixel data at 15F pin 8.

Video blanking and blinking are controlled by the VSP+ (Video Suppress) output of the 8275 at 11G pin 35. VSP+ is pipelined at 12G pin 15 and 13F pin 3 and then gates off the video display data at 3E pin 12.

8086 CPU BOARD

8086 Microprocessor Logic

Figure 3-13 below shows the major functional blocks of the 8086 microprocessor logic. The major blocks are:

- o the 8086 microprocessor;
- o clock, reset, and ready logic;
- o address and data latches; and
- o input/output address decoders.

Also, see the 8086 CPU Board schematic, Figure 3-14 below, during the following discussion.

Bus Control Lines

As shown on page 2 of Figure 3-14, the 8086 (7F) is strapped at pin 33 to operate in the minimum mode. The minimum mode configures the 8086's bus control lines to be similar to those of an Intel 8085, thus making the lines compatible with 8085-type peripheral devices. The bus control lines include HOLD+ (Hold Request) at pin 31, HLDA+ (Hold Acknowledge) at pin 30, RD- (Read) at pin 32, WR- (Write) at pin 29, M+/IO- (Memory or Input/Output Decode) at pin 28, ALE+ (Address Latch Enable) at pin 25, PBHE- (Processor Bus High Enable) at pin 34, DT/R+ (Data Transmit or Receive) at pin 27, DEN- (Data Bus Enable) at pin 26, and AD0+ at pin 16.

Clock, Reset, and Ready Logic

The Intel 8284A clock generator at 7H provides the clock, reset and ready signals necessary for operation of the 8086. Crystal Y1 is connected to 7H pins 16 and 17 to form a 24-MHz oscillator. The 8-MHz PCLOCK+ (Processor Clock) at 7F pin 19 is generated when the 8284A divides the oscillator input by three.

Power-up detection and reset switch debounce are provided by R1, C108, and CR1, which are connected to the 8284A pin 11 RES- (Reset) input. The 8284A internally conditions RES- with

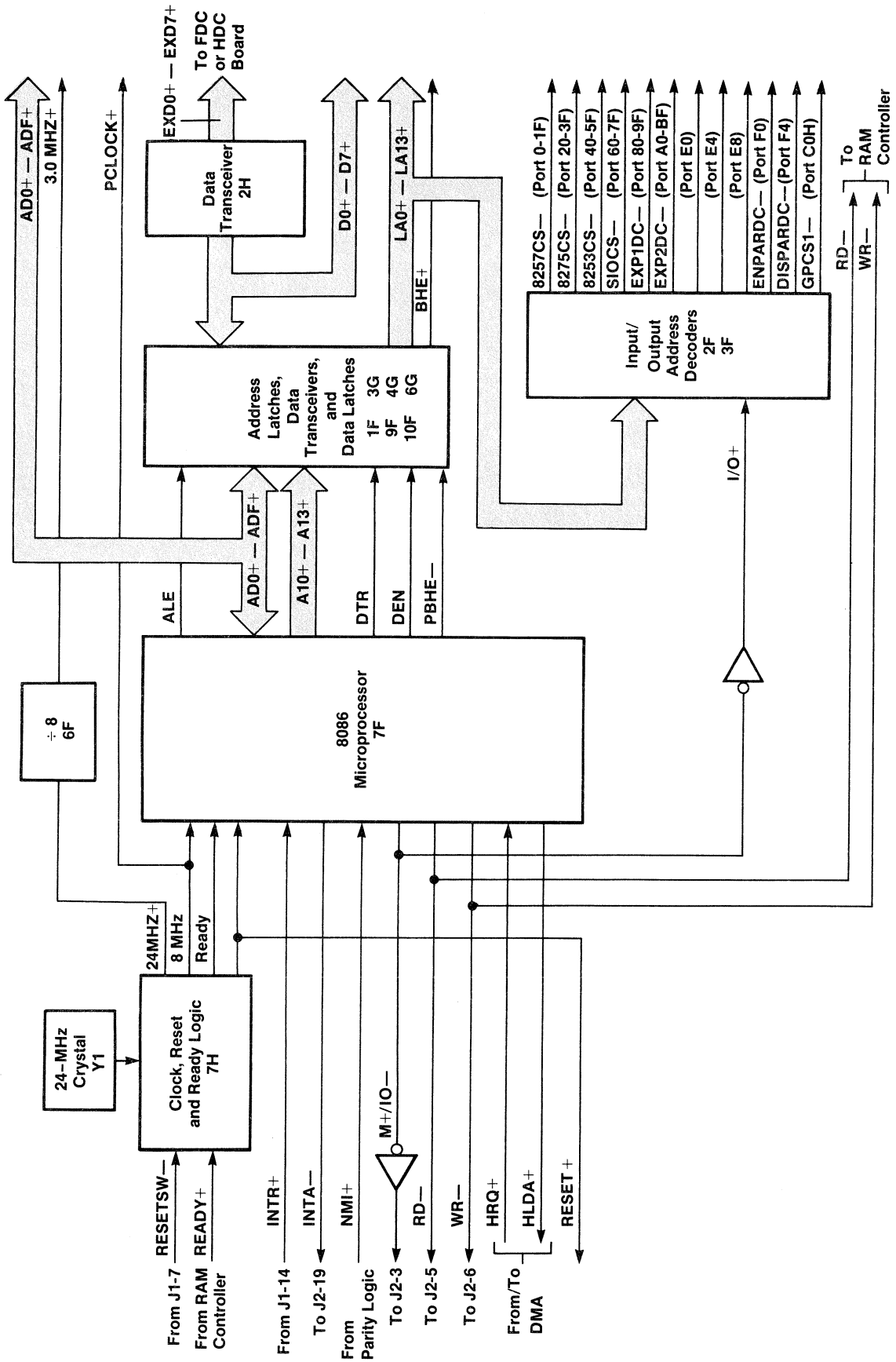


Figure 3-13. 8086 Microprocessor Logic.

a Schmitt trigger, and generates RESET+ (General Purpose System Reset) at pin 10.

READY+ is an asynchronous signal from the memory logic, which is connected to pin 6 of the 8284A. ASYNC- (Ready Synchronization) at pin 15 of 7H is always low to allow the READY+ signal to be synchronized to PCLOCK+ at pin 8 of 7H. The synchronized READY+ is sent to pin 22 of the 8086 to indicate that a memory or input/output cycle is ready to complete and that the 8086 can finish the cycle (see "Memory Logic" below).

Address and Data Buses

The 8086 at 7F communicates with RAM, ROM, and input/output devices on its AD0+-ADF+ (Address/Data) bus. AD0+-ADF+ are time-multiplexed during a cycle to contain, first, the address of the memory or input/output device to be read from or written to and, second, the data to be transferred between the 8086 and the RAM array or input/output device. Four other lines on the AD bus, AD10+-AD13+ are not time-multiplexed and contain only address information.

The 8086's cycles are divided into a number of T-states (PCLOCK+ processor clock cycles) with each T state having a period of 125 ns. The number of T states varies depending on the cycle performed, as shown below. Additionally, input/output read and write cycles can have additional T states (T wait) added to them to allow for the additional setup time required by certain input/output devices.

Cycle	Required T states	Equivalent Time
RAM read	4	500 ns
RAM write	4 or 5	500-625 ns
ROM read	12 +	1.5 μs +
Input/output read	12 +	1.5 μs +
Input/output write	12 +	1.5 μs +
One interrupt acknowledge cycle (two are used)	12	1.5 μs

NOTES; UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS 1/4W, 5%.
2. COMPACITANCE VALUES ARE IN PICOFARADS.
3. ALL DEVICES ARE STANDARD 7&14, 8&16 AND 10&20 GROUND & POWER CONNECTIONS.
4. ALL DIODES ARE TYPE IN914B EXCEPT FOR CR10.
5. 3301(16G) IS AN ALTERNATE PART FOR THE 8275(15G).

POWER AND GROUND LOCATOR CHART			
REF. DES	DEVICE TYPE	+5V	GROUND
1G	8257-5	31	20
7H	8284A	18	9
7F	8086-2	40	1,20
3H, 1BH	2732	24	12
15G(16G)	8275 (3301)	40	20
11H	8253-5	24	12
9G	7201	40	20
3H, 1BH	2732	24	12
7D-24D 7C-24C 7B-24B 7A-24A	μPD 4164-2	8	16

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
RP16	
R23	
C112	C7,C8,C105,C109
Q1	
CR10	
Y1	
J3	

SPARE GATES		
TYPE	REF. DESIG.	QTY
74LS00	4C	1
74LS08	5C 4E	2
74LS04	16E	3
74LS32	3B	1
74LS244	5F	1
74S02	4B	1
74S04	10G	1
74S132	1C	1
74S240	4A	1

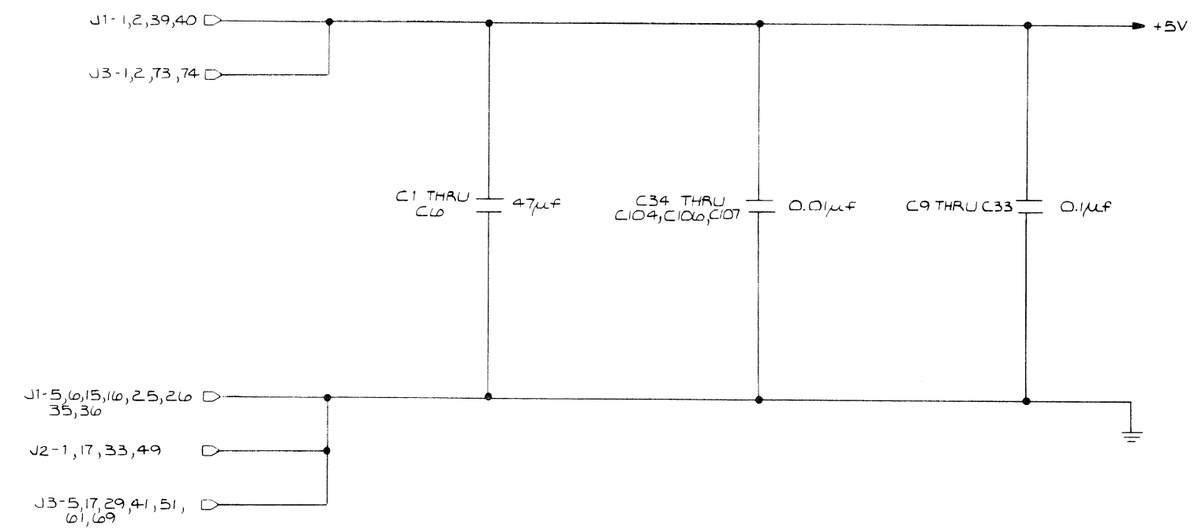


Figure 3-14. 8086 CPU Board Schematic. (Page 1 of 7)

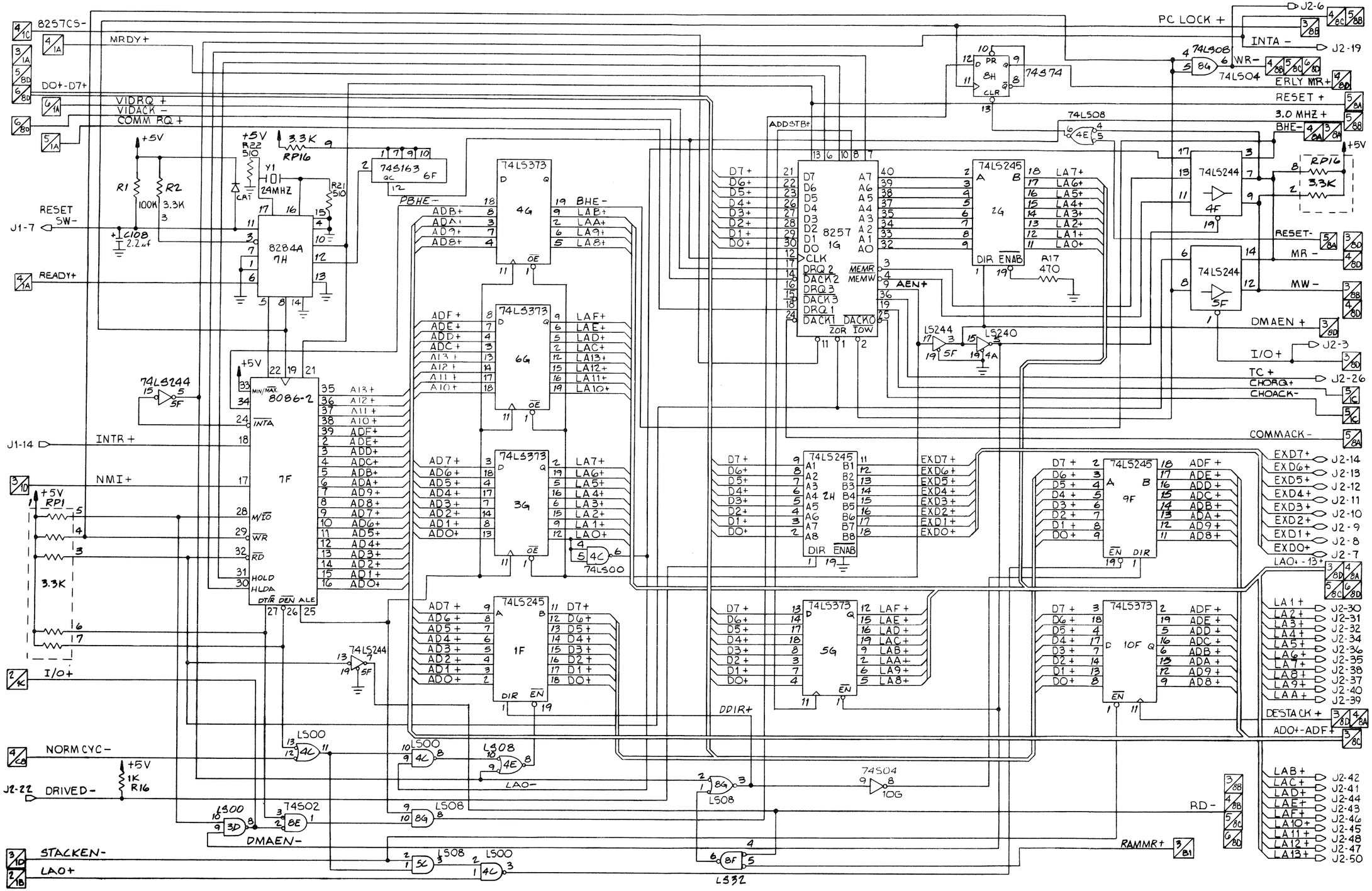


Figure 3-14. 8086 CPU Board Schematic. (Page 2 of 7)

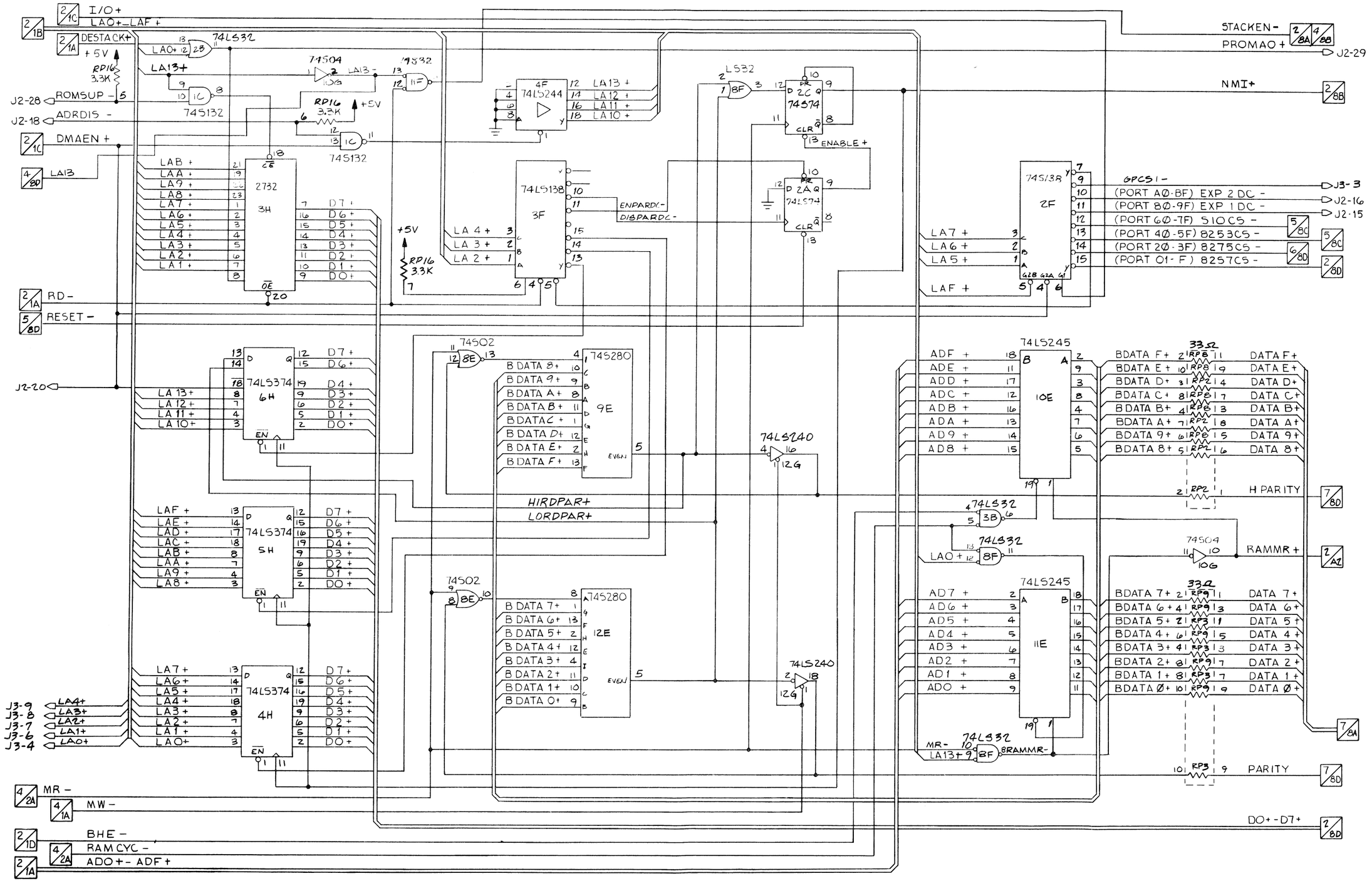


Figure 3-14. 8086 CPU Board Schematic. (Page 3 of 7)

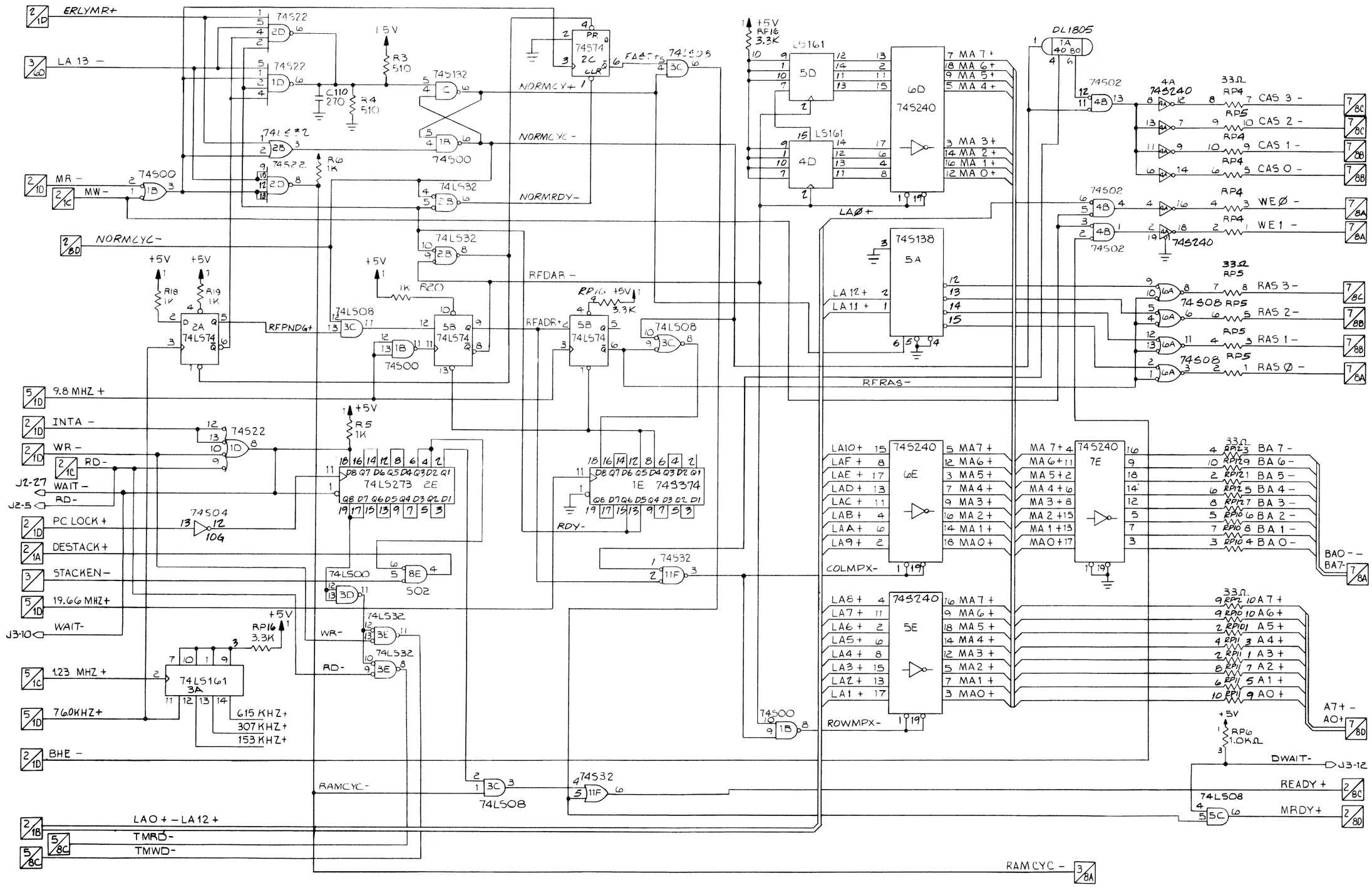


Figure 3-14. 8086 CPU Board Schematic. (Page 4 of 7)

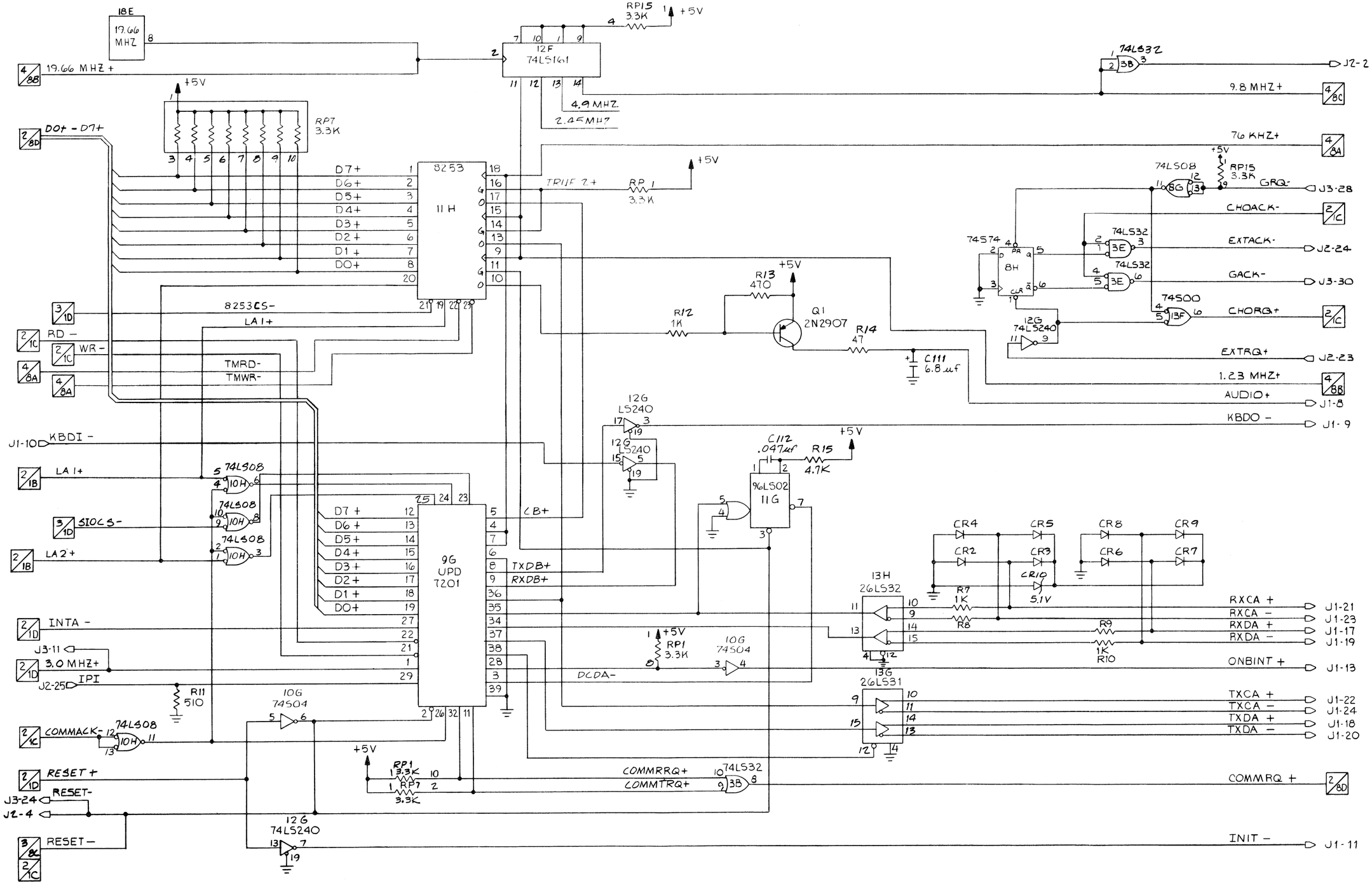
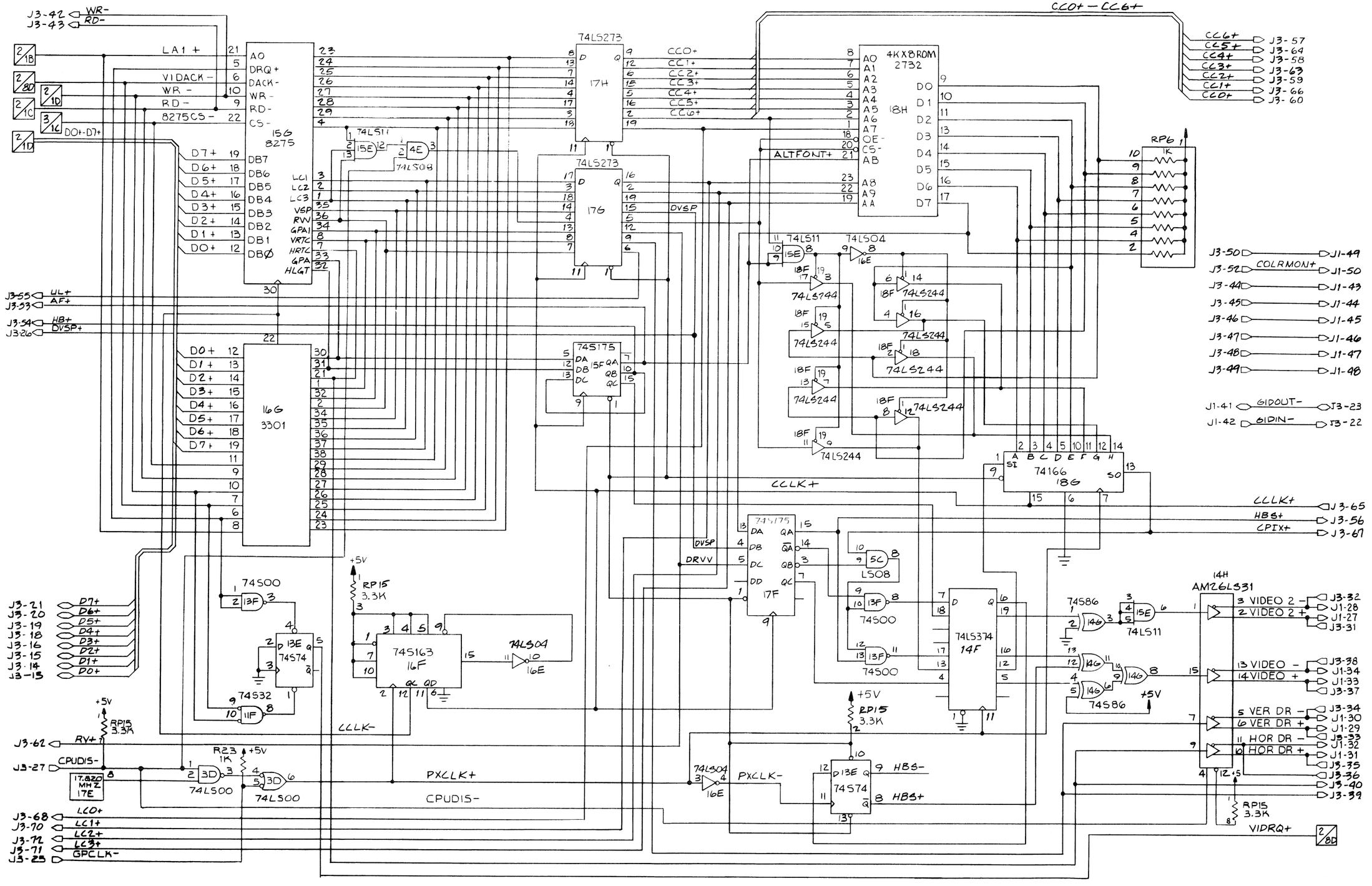


Figure 3-14. 8086 CPU Board Schematic. (Page 5 of 7)



Theory of Operation 3-61

Figure 3-14. 8086 CPU Board Schematic. (Page 6 of 7)

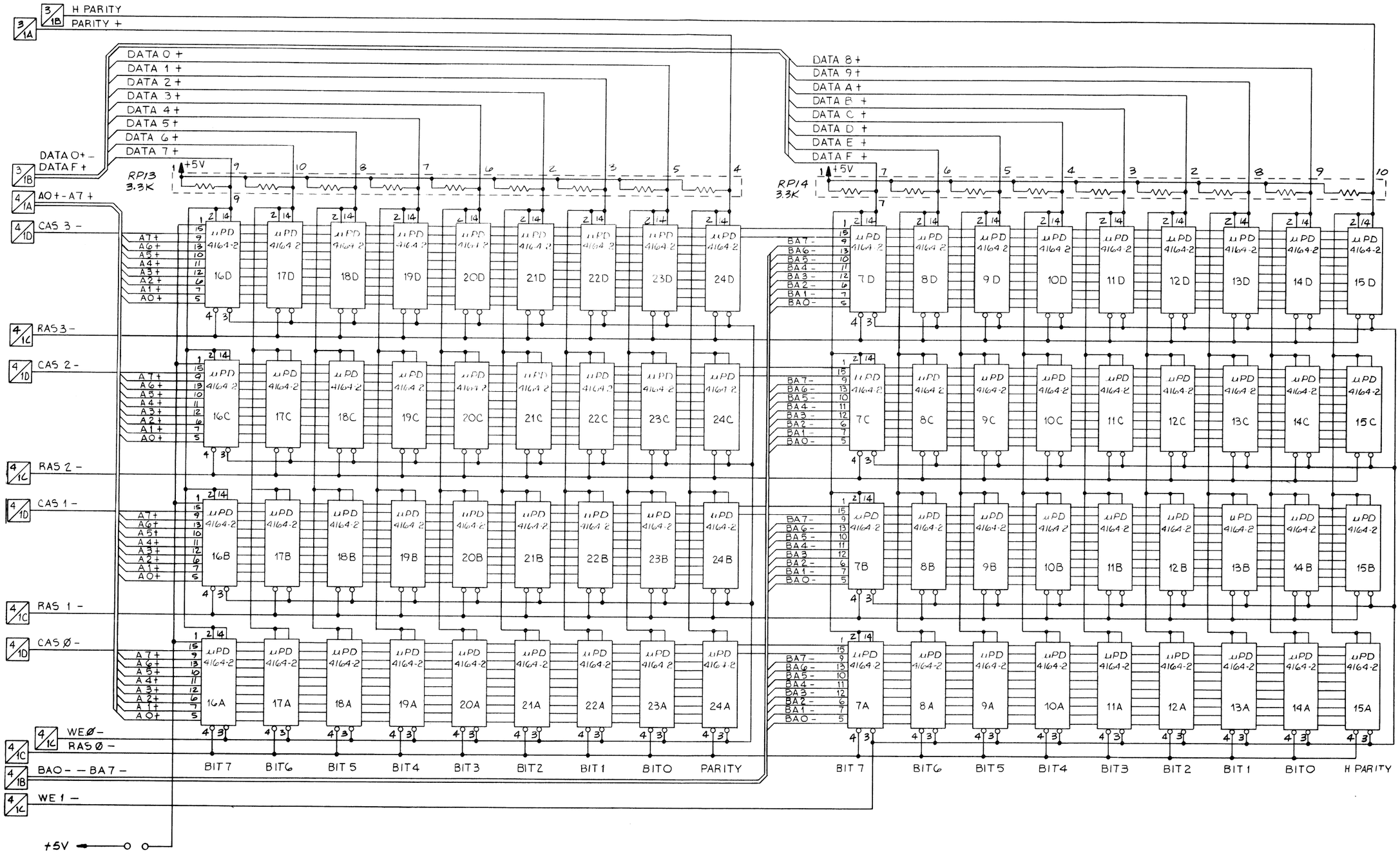


Figure 3-14. 8086 CPU Board Schematic. (Page 7 of 7)

At the beginning of any CPU cycle (T-1) the tri-state latches at 3G, 6G, and 4G latch the address of the memory or input/output device from the AD0+-ADF+ and AD10+-AD13+ lines when the 8086 pulses ALE+ at pin 25 of 7F. The outputs of the latch form the LA0+-LA13+ (Line Address) bus, which carries address information to the memory controller and input/output ports on the CPU Board and the FDC or HDC Board.

PBHE- from pin 34 of the 8086 is latched into 4G along with the address lines. Together with the LA0+ address line, PBHE- determines whether an even byte, odd-addressed byte, or a word access (both bytes) is made to the RAM array or input/output device. LA0+ and PBHE- are used to enable or disable certain transceivers during a DMA or input/output device read or write cycle. The coding of PBHE- and LA0+ is:

LA0+	PBHE-	Type of Access
0	0	Word (both odd and even bytes)
0	1	Even byte
1	0	Odd byte
1	1	None

After the address is latched on the LA0+-LA13+ bus, either the 8086 reads one or two bytes of data on the AD0+-ADF+ bus; or, during later T-states, it writes one or two bytes of data on the AD0+-ADF+ bus. To transfer the data, the 8086 enables certain 8-bit transceivers or latches on the CPU Board to channel the data to or from the addressed location.

RAM Read and Write Cycles. A RAM read or RAM write cycle can transfer either 8 or 16 bits of data between the 8086 and a RAM location. When the address from the 8086 is latched into 3G, 6G, and 4G by ALE+, the state of PBHE- at pin 34 of 7F is also latched into 4G. If PBHE- (BHE- after latch 4G) and address bit LA0+ are both low, transceivers 10E and 11E (page 3 of Figure 3-14) are enabled to transfer 16 bits of data between the BDATA0+-BDATAF+ (Buffered RAM Data) lines and the AD0+-ADF address/data lines. When BHE- is low and LA0+ is high, only 10E is enabled to transfer the odd byte of the memory location. Likewise, when only LA0+ is low, only 11E is

enabled to transfer the even byte of the memory location.

ROM Read Cycles. A ROM read cycle requires that address bit LA13+ be high when the address is latched into 3G, 6G, and 4G during T-1. LA13+ (along with a high ROMSUP- (ROM Suppress) from the FDC or HDC Board) enables ROM 3H and indicates that the address is in the upper 512-kilobyte address range of RAM array. The eight outputs of the ROM are connected to the D0+-D7+ 8-bit data bus.

In addition to byte instruction fetching, the 8086 can also fetch 16-bit words. The memory logic must split the ROM read cycle into halves to get two bytes of data on the AD0+-ADF+ lines during a single ROM read cycle (see "Memory Logic" below). The signals STACKEN- (Stack Enable), DESTACK+ (Stack Disable), and PROMA0+ (PROM Address Bit 0) are used to present two bytes of data from the ROM to the 8086 as a single 16-bit word.

As shown on page 3 of Figure 3-14, STACKEN- is low at pin 11 of gate 11F when RD- is low and LA13+ is high, indicating that a read cycle is occurring in the upper 512 kilobytes of RAM. STACKEN- works to stack a byte onto the AD8+-ADF+ lines while the other byte is placed on the AD0+-AD7+ lines. DESTACK+ is active during the first 625 ns of the ROM read cycle and is the NANDed result of STACKEN- and the signal from pin 6 of shift register 2E. As shown on page 4 of Figure 3-14, shift register 2E supplies a delayed and inverted copy of RD- from pin 8 of gate 1D that indicates the elapsed time since the start of the ROM read cycle. When DESTACK+ goes low at the beginning of the second half of the ROM read cycle, the data on the D0+-D7+ lines is placed on the AD0+-AD7+ lines to the 8086.

For any location, an odd or even byte is addressed in ROM by the state of PROMA0+ at pin 11 of OR gate 2B. Either a high DESTACK+ or a high LA0+ address bit causes PROMA0+ to go high, and thus causes the odd byte to be addressed in the ROM at pin 8 of 3H.

As shown on page 3 of Figure 3-14, when the 8086 starts the cycle by addressing an odd byte in ROM (LA0+ = 1 and BHE- = 0), DESTACK+ is high during

the first half of the cycle; therefore, PROMA0+ is high at pin 8 of ROM 3H. The odd byte appears at the outputs of the ROM on the D0+-D7+ data lines and is latched to the AD8+-ADF+ lines through 10F on page 2 of Figure 3-14. The outputs from latch 10F are enabled by STACKEN- at the beginning of the cycle. About 625 ns later, DESTACK+ goes low, which causes entry into the second half of the ROM read cycle.

Since DESTACK+ is low during the second half of the read cycle, PROMA0+ reflects the state of LA0+, which in this case is high. Therefore, the same byte is addressed during the second half of the ROM read cycle and placed on the D0+-D7+ data lines and onto the AD0+-AD7 lines through transceiver 1F. When the 8086 examines the AD lines for the odd byte, it ignores any data on the AD0+-AD7+ lines.

If the 8086 addresses an even byte in the ROM (LA0+ = 0 and BHE- = 1), PROMA0+ is again high during the first half of the cycle, and the resulting odd byte is latched into 10F by a high DESTACK+ and on the AD8+-ADF+ lines by STACKEN-. When DESTACK+ goes low during the second half of the cycle, PROMA0+ reflects the state of the LA0+ address line. Since LA0+ = 0 at pin 8 of ROM 3H, the even byte is addressed and appears on the D0+-D7+ data lines to transceiver 1F, which transfers the even data byte onto the AD0+-AD7+ lines. Transceiver 1F is enabled by a high LA0- (inverted from LA0+ at pin 9 of 4C) and a low DEN- at pin 13 of 4C. The direction of 1F is set by a combinaton of RD- and a low RAMMR+ (RAM Memory Read) from the memory logic. Again, when the 8086 examines the AD lines for the even byte at the end of the cycle, it ignores any data on the AD8+-ADF+ lines.

When the 8086 performs an aligned word read, that is, a read at an even address, the same process as described above for the even byte access occurs. However, at the end of the cycle, the 8086 reads both bytes on the AD0+-AD7+ and AD8+-ADF+ lines. When the 8086 performs a nonaligned read (odd address), it executes two read cycles. The first cycle operates as described above for an odd byte read: the second cycle operates as described above for an even byte read.

Input/Output Read and Write Cycles. Data, during an input/output read or write cycle, can take one of two paths on the CPU Board's data bus depending on the state of the LA0+ address line. Data takes the first path, through transceiver 1F (shown on page 2 of Figure 3-14), if the input/output address is even (LA0+ = 0). Transceiver 1F allows data to pass from the D0+-D7+ data lines to the AD0+-AD7+ lines; it is enabled through pins 11 and 8 of gates at 4C and pin 8 of gate 4E with a low LA0+ and a low DEN- from pin 26 of 8086 7F. Transceiver 1F's direction is determined by the state of RD- from pin 32 of 7F and a low RAMMR+ from pin 5 of 3A. Data takes a second path, through transceiver 9F, if the input/output address is odd (LA0+ = 1). Transceiver 9F is enabled by a low DEN- inverted at pin 11 of gate 4C, a high STACKEN- at pin 3 of gate 5C, and a high LA0+ at pin 3 of gate 4C. Transceiver 9F's direction is determined by the state of RD- from pin 26 of 7F.

Interrupt Acknowledge Cycle. The interrupt acknowledge cycle uses transceiver 1F to read an interrupt vector from the 7201 on the CPU Board or the 8259A on the FDC or HDC Board. Transceiver 1F is enabled when INTA- goes low at pin 24 of 7F. INTA- (Interrupt Acknowledge) is inverted at pin 5 of 5F and sent through pin 8 of gate 4E. The 8086 then reads the interrupt vector on the AD0+-AD7+ lines at the end of the second interrupt acknowledge cycle. Note that, whether or not transceiver 9F is enabled, its direction is forced by INTA- at pin 2 of gate 8G such that the data transfers from the D0+-D7+ data lines to the AD8+-ADF+ lines. The 8086 ignores any data present on its AD8+-ADF+ lines when the interrupt vector is read. Also, an interrupt vector from the FDC or HDC Board's 8259A interrupt controller is sent through transceiver 2H from the EXD0+-EXD7+ (Expansion Data) lines to the AD0+-AD7+ lines. 2H's direction is determined by the states of DRIVED- (Drive Data Bus) from the FDC or HDC Board's bus control logic (see "Bus Interface and Interrupt Control Logic" for either the FDC or HDC Board).

Input/Output Address Decoders

The two decoders at 2F and 3F select the input/output addresses.

Decoder 2F is enabled when an 8086 input/output cycle is in progress, that is, when I/O+ is high at 2F pin 6 and DMA is not in progress. DMAEN+ (DMA Enable) is low at 2F pin 4. Decoder 2F then decodes address lines LA5+-LA7+ to generate the active-low enable signals shown below:

Address Range	Active Signal	Origin	Device Accessed
0-1Fh	8257CS-	2F-15	8257 DMA controller
20h-3Fh	8275CS-	2F-14	8275 CRT controller
40h-5Fh	8253CS-	2F-13	8253 counter timer
60h-7Fh	SIOCS-	2F-12	7201 communications controller
80h-9Fh	EXP1DC-	2F-11	Input/output devices on FDC or HDC Board
A0h-BFh	EXP2DC-	2F-10	Input/output devices on FDC or HDC Board
E0h-FFh	EXTDC-	2F-7	Decoder 3F
C0h-DFh	GPCSI-	2F-9	Advanced video board

The decoder at 3F, enabled by EXTDC- (External Decode Enable) and RD-, generates several decoded read signals from address lines LA2+-LA4+, as shown below:

Address Range	Active Signal	Origin	Device Accessed
E0h-E3h	---	3F-15	Reads parity error address latch at 4H
E4h-E7h	---	3F-14	Reads parity error address latch at 5H
E8h-EBh	---	3F-13	Reads parity error address latch at 6H
F0h-F3h	ENPARDC-	3F-11	Enables parity error detection and interrupts

Address Range	Active Signal	Origin	Device Accessed
F4h-F7h	DISPARDC-	3F-10	Disables parity error detection, and parity error interrupts; clears existing errors

Memory Logic

Figure 3-15 below shows the functional blocks of the memory logic.

The normal cycle logic performs both read and write memory cycles that can be used by the 8086 and 8257 to access up to 512 kilobytes of RAM.

Refresh cycles are initiated every 13 μs by the refresh cycle logic to maintain data stored in the dynamic RAM chips.

Ready (handshaking) logic controls the memory accesses by the 8086 and 8257. As long as the ready signal is not asserted to the appropriate bus master, the memory access is prolonged by wait states.

An even parity error detection scheme is used to ensure the integrity of data in the RAM array. A ninth bit is generated by the parity logic during normal write cycles and then checked during normal read cycles. If a parity error occurs, a nonmaskable interrupt is issued to the 8086 if the parity check enable flip-flop is enabled through Port F0h.

The RAM array contains up to eight banks of dynamic RAM chips, which are 64-kilobit (kb) by 1 bit, on upper and lower halves of the RAM array. An even numbered bank and the next higher number odd-numbered bank make up a row of 18 chips: 16 for data and two for parity.

The 4-kilobyte bootstrap ROM is used upon a manual or power up reset to run simple diagnostic tests and load the CTOS System Image from the cluster communications line. The bootstrap ROM can be suppressed by an external device to make other use of the upper 512-kilobyte address space, in which the ROM address space resides.

See the 8086 CPU Board schematic, Figure 3-14 above, in addition to the memory logic block diagram, during the following discussion.

Normal Read and Write Cycle Logic

As shown in the upper left corner of page 4 of Figure 3-14, MR- (Memory Read) and MW- (Memory Write) are ORed at pin 3 of gate 1B indicating that either the 8257 DMA controller at 1G or the 8086 at 7F is requesting a read or write cycle. When pin 3 of 1B is high (MR- or MW- are low), a normal cycle is started by pin 6 of gate 1D going low. A read cycle requested by the 8086 starts early when ERLYMR+ (Early Memory Read) goes high at pin 1 of 2D. ERLYMR+ is used along with MR- to satisfy the timing requirements of the 64-kb dynamic RAM chips when used with the 8-MHz 8086.

ERLYMR+ is generated only when the 8086 requests a read cycle. As shown on page 2 of Figure 3-14, a high M+/IO- from pin 28 of 7F and DMAEN- are NANDed at pins 10 and 9 of gate 3D, indicating that an 8086 memory cycle (and not a DMA cycle) is being requested. The low pin 8 output of 3D I/O+ is NORed with a low DT+/R- at pins 2 and 3 of gate 8E. The high pin 1 output of 8E is ANDed with ALE+ from pin 25 of 7F at pins 10 and 9 of gate 8G. Finally, the high pin 8 output of 8G is sent to the pin 12 D input of flip-flop 8H where it is clocked by a transition of PCLOCK+ during the first T-state, T1. The high pin 9 output of 8H is ERLYMR+ and is sent to pin 1 of gate 2D (page 4 of Figure 3-14) to start the memory cycle. Note that the three other inputs and the output of gate 2D are wired parallel to those of gate 1D. Other conditions necessary for starting either cycle at pins 6 of gates 1D or 2D are:

- the current address must be in the lower 512 kilobytes of the address space (LA13+ must be low),
- a previous memory cycle cannot be in progress (RDY- (Memory Ready) must be high), and
- a refresh cycle cannot be pending (gate 1D pin 12 must be low).

When gate 1D pin 6 and/or gate 2D pin 6 is low, the RS flip-flop 1C pin 6, NORMCYC+ (Normal Cycle) is set. R3, R4, C110, and pin 5 of gate

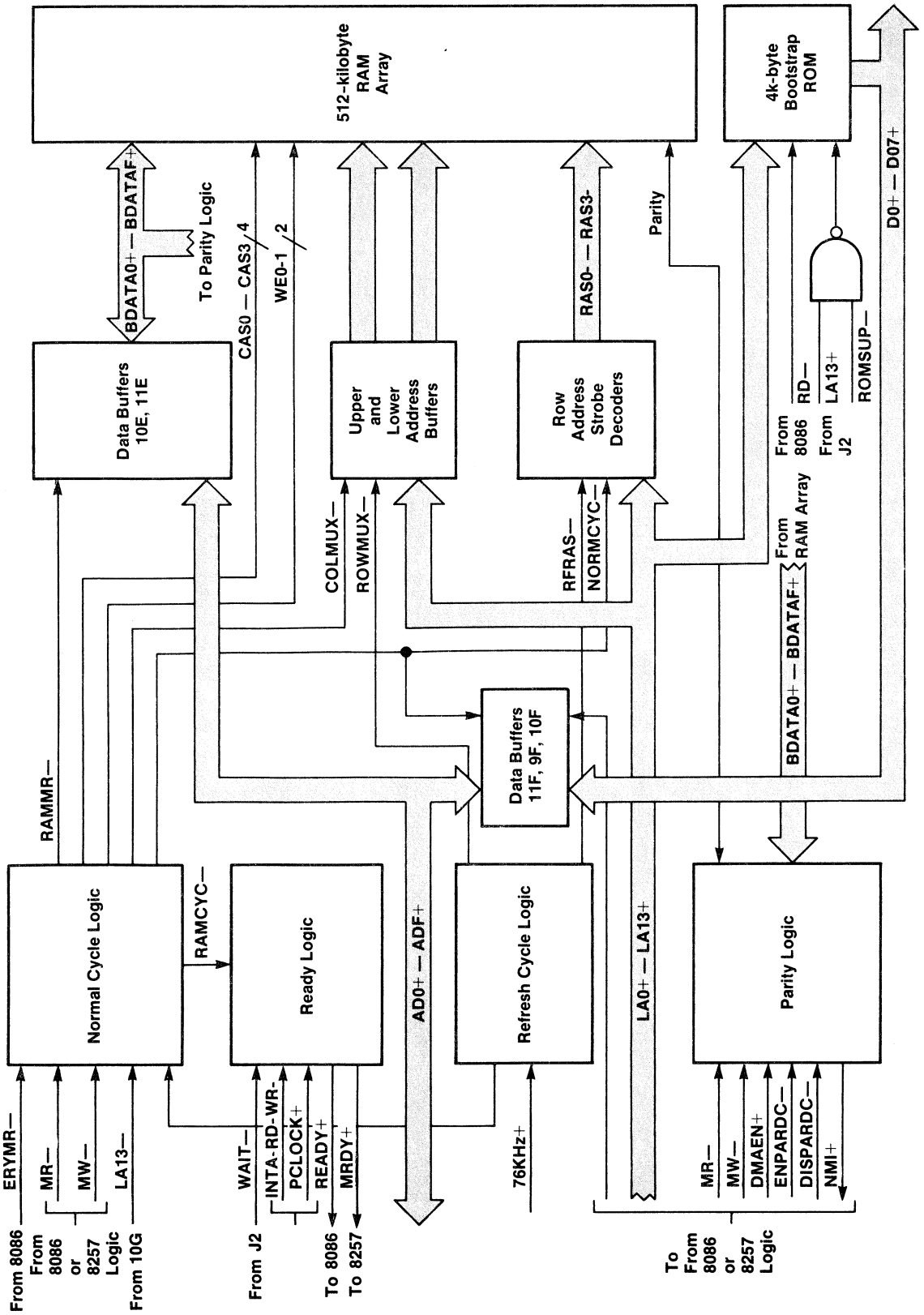


Figure 3-15. Memory Logic.

1C Schmitt-trigger input ensure that the strobe at pin 5 of 1C is long enough to preset flip-flop 1B.

NORMCYC- at decoder 5A pin 6 causes the RAS- (Row Address Strobe) for the appropriate row of RAMs to be generated. The RAS- signals, after being ANDed with RFRAS- (Refresh Row Address Strobe) at gate 6A, go to the array of 64-kb dynamic RAMs. NORMCYC- causes the output of gate 3C pin 8 to go low, which feeds the digital delay line, register 1E. Finally, NORMCYC- is sent to the pin 1 input of delay line 1A where it appears 40 ns later at pin 4 of 1A. NORMCYC-, now delayed by 40 ns, is ORed with a low RFADR+ (Refresh Address) at pins 1 and 2 of gate 11F. The low pin 3 of 11F activates COLMPX- (Column Multiplex) and deactivates ROWMUX- at pin 8 of 1B to switch the MA0+-MA7+ (Multiplexed Address) lines of the memory chips from the default row address to the column address. The buffers at 5E, 6E, and 6D form the multiplexer that selects the row, column, or refresh address, respectively. The MA lines go directly to the lower half of the RAM array and are buffered at 7E for the upper half of the RAM array.

Forty nanoseconds after COLMPX- goes low, pin 13 of gate 4B activates CAS0+-CAS3+ (Column Address Strobe) from NORMCYC- and from the NORMCYC- signal delayed by 80 ns. CAS0+-CAS3+ are buffered and inverted by 4A before going to the RAM array. After CAS0+-CAS3+ go high, a delay occurs and RDY- goes low at pin 15 of 1E to indicate that the cycle is finishing. The 8086 or 8257 can then go on with another cycle or a refresh cycle can start.

As shown on page 3 of Figure 3-14, data to and from the RAM array are buffered by transceivers 10E and 11E. The 8086 can enable transceivers 10E and 11E to perform a read or write cycle only to the upper or lower halves of the RAM array during a byte read or write cycle, or to both upper and lower halves of the RAM array for a word read or write cycle. Transceiver 10E is enabled by a low at pin 6 of gate 3B when both RAMCYC- (RAM Cycle) and BHE- (Bus High Enable) are low. RAMCYC- is low at pin 8 of gate 2D (as shown on page 4 of Figure 3-14) when MR- or MW- are low and LA13- is high, meaning that a RAM read or write cycle is being performed and the RAM address is in the lower 512 kilobytes of the

RAM array. On page 3 of Figure 3-14, RAMCYC- is ANDed with a low BHE- signal from the 8086 to enable transceiver 10E to transfer 8 bits of data between the upper half of the RAM array on the BDATA8+-BDATAF+ lines and the 8086 on the AD8+-ADF+ lines. Similarly, transceiver 11E is enabled at pin 11 of 8F when RAMCYC- and LA0+ are low. Transceiver 11E allows data between the lower half of the RAM array on the BDATA0+-BDATA7+ lines and the 8086 on the AD0+-AD7+ lines.

The direction of transceiver 10E is determined by the signal RAMMR- at pin 10 of gate 8F. RAMMR- is low when MR- and LA13+ are both low at pins 10 and 9, respectively, of gate 8F. Transceiver 10E's direction is set by RAMMR+, which is the inverted copy of RAMMR- through pin 10 of inverter 10G. Transceiver 11E's direction is set directly by RAMMR- from pin 8 of 8F.

In addition to the two separate transceivers for each enabled row of 18 chips in the RAM array, separate write enable signals are also used: WE0- (Write Enable) for the lower byte of the RAM array, and WE1- for the upper byte of the array. WE0- is generated from a low MW- and a low LA0+ address line at pins 5 and 6, respectively, of gate 4B. The low pin 6 of 4B is buffered and inverted at pin 16 of 4A and sent to the RAM array. WE1- for the upper byte of RAM is generated from MW- at pin 3 of gate 4B and a low BHE- at pin 2 of 4B. The pin 1 output of 4B is buffered and inverted at pin 18 of 4A and then sent to the RAM array.

If a byte is written only to the upper half of the RAM row enabled by the CAS and RAS signals, WE1- is low and transceiver 10E is set to transfer the byte from AD8+-ADF+ lines to the DATA8+-DATAF+ (RAM Data) lines because of the state of BHE-. Since LA0+ is high (lower half of RAM not written to), WE0- must be high, meaning that, by default, a read of a data byte from the lower half of RAM row can take place. To prevent a bus contention, LA0+ also disables transceiver 11E.

Refresh Logic

Every 13 μs, the RAM array requires a refresh cycle to maintain the content of the 64-kb

dynamic RAMs. The refresh cycle differs from the normal cycle in that only seven row address bits and no column address bits are required.

The 76-kHz clock, 76KHZ+, sets pin 5 of the refresh-pending flip-flop 2A every 13 μs, which forces 2A pin 6 low to prevent any new nonrefresh cycles from beginning at pins 4 of gates 1D and 2D.

At the next negative transition of the 9.8-MHz clock, and if NORMCYC- is high, RFADR+ (Refresh Address) at flip-flop 5B pin 9 is set. RFADR+ and RFADR- at 5B pin 8 cause address multiplexers 5E, 6E, and 6D to drive the refresh address from the two address counters at 4D and 5D through 6D.

At the next positive transition of 9.8MHZ+, RAS (refresh row address) flip-flop 5B is set at pin 5. RFRAS- from 5B pin 6 causes all RAS signals to go low through OR gate 6A. In addition, gate 3C pin 8 causes the RAS signals to propagate through the shift register 1E pin 18. When the refresh cycle is complete, the signal RDY- from 1E pin 15 causes pin 8 of gate 2B to go low, which indicates that the refresh cycle is almost complete. Pin 8 of 2B clears pin 1 of the refresh-pending flip-flop at 2A. Fifty nanoseconds later, the signal at shift register 1E pin 12 goes low, clearing the refresh address and RAS flip-flops at 5B pins 1 and 13. When RFADR- goes high, it increments the address for the next refresh cycle at 4D pin 2 and 5D pin 2. RDY- goes inactive after 150 ns, thus enabling the normal cycle and refresh cycle arbitration logic at 1D, 2D, 1C, and 1B. This guarantees the required precharge time for the RAM chips.

Ready Logic

There are two handshake signals that go from the RAM controller to the two requesters: READY+ for the 8086, and MRDY+ (Memory Ready) for the 8257. These signals tell the requester that a RAM or input/output read or write cycle, or interrupt acknowledge cycle is complete and that the requester can go on to other cycles. As long as these signals are inactive, the requester inserts wait states and increases the time that MR- or MW- stays low.

All bus command strobes, WR-, RD-, and INTA- (Interrupt Acknowledge) are NANDed at gate 1D pin 8 and sent to shift register 2E pin 18. Shift register 2E counts the processor clock cycles that have occurred since the beginning of the command strobe. Shift register 2E's output at pin 2 is used to generate 8 wait states for 8086 input/output or ROM cycles.

The input to 2E is an open-collector signal, WAIT-, from the FDC and HDC Boards on connector J2 pin 27 or from an advanced video board on connector J3 pin 10. An external device can generate any number of wait states by asserting WAIT-. When a memory cycle is not in progress, RAMCYC- is high at pin 1 of gate 3C and the signal at pin 2 of 3C generates an 8 wait-state ready signal. The high output pin 3 of 3C is ORed at gate pin 4 of gate 11F to make the ready signal for the 8086, READY+. MEMOK+ (Memory OK), from gate 3C pin 6, is the other input used during RAM read or write cycles to pin 5 of gate 11F. MEMOK+ is also sent to pin 5 of gate 5C where it is ANDed with DWAIT- (DMA Wait Request from an advanced video board) at pin 4. The high pin 6 output of 5C, MRDY+ is driven to the 8257 to indicate that the memory is ready for another cycle.

When the SLOW/FAST flip-flop 2C's pin 6 output, FAST+, is high at pin 5 of 3C and NORMCYC+ is high at pin 4 of 3C, MEMOK+ is asserted at pin 6 of gate 8C.

The SLOW/FAST flip-flop is used in memory control arbitration. During a refresh cycle, the SLOW/FAST flip-flop is set to SLOW; during a normal cycle, it is set to FAST. The SLOW/FAST flip-flop causes all RAM accesses that are not interfered with by a refresh cycle to take no wait states. The SLOW/FAST flip-flop is set to FAST at the beginning of each normal cycle by MR- or MW- causing a high at pin 3 of gate 1B. If pin 8 of gate 2B, RFRDY-, is low, indicating that a refresh cycle occurred since the beginning of the cycle, SLOW/FAST is set to SLOW and MEMOK+ is inhibited, thus adding extra wait states to the cycle. When set to SLOW, wait states are inserted for the 8086 or 8257; a normal cycle cannot start because a refresh cycle is in progress. Wait states are generated until the nonrefresh cycle completes.

When the cycle completes, NORMRDY- (Normal Cycle Ready) clears the SLOW/FAST flip-flop, which asserts FAST+ at 2C pin 6. FAST+, in turn, activates MEMOK+ and then READY+. NORMRDY- at gate 2B pin 6 is the OR of NORMCYC- and RDY- from the normal cycle logic. RFRDY- is the OR of RDY- and RFADR- at pin 8 of gate 2B. RFRDY- is used to preset the SLOW/FAST flip-flop to SLOW, so that any interrupted normal cycle does not finish the cycle prematurely.

Parity Logic

To ensure data integrity, an even parity error detection scheme is used. Each data byte in the RAM array has a ninth bit associated with it, the parity bit. For any memory location, the total number of 1 bits in the 9-bit byte is always an even number. Therefore, when a location is read and the number of 1 bits is found to be an odd number, the data (or possibly the parity bit) is in error. Once this error occurs, the status of the address bus is saved, and a nonmaskable interrupt is sent to the 8086 to invoke error-recovery software.

Two parity generator chips at 9E and 12E for the odd and even halves of RAM, respectively, are used to generate parity during writes and to check it during reads. The even output of either parity generator is high when the total number of 1 bits at its inputs is even.

During a write cycle, pin 8 of 12E is forced low by pin 10 of NOR gate 8E since MR- is high at pins 9 8E. If the parity of the BDATA0+-BDATA7+ (RAM Data) bits is even for 12E, pin 5 of 12E is high, indicating that a 0 should be written into the parity RAM for the lower half of the RAM array. Correspondingly, if the parity of the data bit is odd, 12E pin 5 is low, indicating that a 1 should be written into the parity RAM. During a normal write cycle, the presence of MW- causes a parity bit to be driven to the parity RAM chips through an inverting tristate driver at 12G pin 18, which is enabled by a low MW-. The parity generator at 9E works identically to the one at 12E except that the former generates and checks parity for the odd half of the RAM array using the BDATA8+-BDATAF+ lines.

The parity enable flip-flop at pin 9 of 2A controls the parity generators during read cycles. The flip-flop is cleared by either a manual or a power-up reset at pin 1. It is also cleared when Port F4h is read, activating DISPARDC- (Disable Parity), at pin 10 of decoder 3F. Parity error detection is enabled by reading port F0h, activating ENPARDC- (Enable Prity), at pin 11 of decoder 3F, which presets pin 10 of the parity enable flip-flop 2A.

As long as the parity enable flip-flop is not set, the parity error flip-flop at pin 9 of 2C is held clear. This mechanism is used both to disable parity errors and to clear existing ones. The parity error flip-flop generates a nonmaskable interrupt if a parity error occurs. If parity is disabled, a nonmaskable interrupt cannot occur.

When enabled, the parity error detection circuitry samples the output of the parity generator chip at the end of every RAM read to determine if an error occurred. Pins 10 and 13 of gate 8E invert the parity bits coming from the lower and upper RAM bytes being read and send them to 12E and 9E, respectively. The pin 5 outputs of 12E and 9E are therefore high if odd parity was read from the 9-bit byte and an error occurred.

RAMMR- at pin 8 of gate 2C is generated for memory reads when LA13+ and MR- are both low. When MR- goes high, pin 12 of the error flip-flop 2C samples pins 5 of 9E and 12E through pin 3 of OR gate 8F. When a parity error occurs, 2C pin 9 is set. The preset at pin 10 of the parity error flip-flop is connected to its own Q- output, pin 8. Therefore, the only way to clear the error condition is to disable parity, which causes the error flip-flop to clear at pin 13.

The pin 9 Q output of 2D is connected to NMI+ (Nonmaskable Interrupt), which generates a nonmaskable interrupt to the 8086. In addition, NMI+ causes the status of the address bus to be latched to the parity error registers at 4H, 5H, and 6H. Bit 4 of 6H is high if the cycle was for DMA (DMAEN+ high) or low if the read was for the 8086. If bit 7 of 6H is 1, a parity error occurred in the odd half of the RAM array. If bit 6 of 6H is 1, a parity error occurred in the even half of the RAM array.

The nonmaskable interrupt causes the 8086 to jump into the error-recovery software, which uses the parity error registers to determine the error address. Note that if access is made to a location in either half of the RAM array that contains no chips, FFh is read from the location and a parity error results.

RAM Array

As shown on page 7 of Figure 3-14 above, the RAM array contains up to eight banks of nine chips each: one chip for each data bit and one chip for the parity bit. The correspondence between RAM chip locations and memory bits is shown below. A "U" next to a parity chip designation indicates that the RAM is used for the odd half of that row in the RAM array.

Address Range	Bit Bank	7	6	5	4	3	2	1	0	P	
00000-1FFFFh	0	7A	8A	9A	10A	11A	12A	13A	14A	15A	(U)
	1	16A	17A	18A	19A	20A	21A	22A	23A	24A	
20000-3FFFFh	2	7B	8B	9B	10B	11B	12B	13B	14B	15B	(U)
	3	16B	17B	18B	19B	20B	21B	22B	23B	24B	
40000-5FFFFh	4	7C	8C	9C	10C	11C	12C	13C	14C	15C	(U)
	5	16C	17C	18C	19C	20C	21C	22C	23C	24C	
60000-7FFFFh	6	7D	8D	9D	10D	11D	12D	13D	14D	15D	(U)
	7	16D	17D	18D	19D	20D	21D	22D	23D	24D	

Bootstrap ROM

The 4-kilobyte bootstrap ROM runs simple diagnostic tests, loads the CTOS System Image from the cluster communications line, or transfers control of the workstation to a bootstrap ROM on the FDC or HDC Board. When the 8086 is reset either manually or by power-up, Register CS in the 8086 is set to FFFFh and Register IP is set to 0 before program execution begins. This reset causes the first instruction to be fetched from location FFFF:0. The ROM

address space is arranged so that FFFF:0 refers to an address in the bootstrap ROM.

As shown on page 3 of Figure 3-14, when an address is in the upper 512 kilobytes of the addressable memory space (LA13+ is high), gate 1C pin 8 selects the bootstrap ROM at 3H. When RD- goes low, the bootstrap ROM outputs are enabled at 3H pin 20. This allows ROM data to be placed on the D0+-D7+ data bus lines (also see "Address and Data Buses," above).

ROMSUP- (ROM Suppress) is used by the FDC or HDC Board to suppress the bootstrap ROM for parts of the upper 512 kilobytes of the address space. Those parts of the address space are used for the FDC or HDC Board bootstrap ROM, which is used to load the CTOS System Image from one of the local disk drives or generate error codes for the disk drives or drive controller (see "Error Codes" in the "Architecture" section). Otherwise, any memory read above 512 kilobytes refers to a location in the bootstrap ROM. Note that since the ROM is only 4-kilobytes long, it can be referred to at 128 different places in the upper 512 kilobytes of address space.

Direct Memory Access Logic

Direct Memory Access (DMA) transfers data between memory and an input/output device without involving the 8086. The four-channel 8257 is responsible for getting control of the bus from the 8086 and generating the memory address and bus command strobes for the DMA transfers. The data is transferred directly between the memory and the input/output device.

Figure 3-16 below shows the functional blocks of the DMA logic. Also see the 8086 CPU Board schematic, Figure 3-14 above, during the following discussion.

The four DMA channels are assigned as listed below:

Channel	Priority	Device	Request	Acknowledge
0	High	FDC, HDC, and advanced video boards	CH0RQ+	CHOACK+

Channel	Priority	Device	Request	Acknowledge
1	Medium	Communications	COMMRQ+	COMMACK-
2	Low	Video	VIDRQ+	VIDACK-
3	---	The Channel 3 registers are used to auto-initialize Channel 2.		

8257 Programming

The 8257 must be programmed with input and output instructions from the 8086, as described above under "Direct Memory Access" in the "Architecture" section. That section also lists the steps involved in a DMA transfer.

As shown on page 2 of Figure 3-14, the 8086 programs the 8257 via the data bus lines, D0+-D7+. When one of the registers within the 8257 is addressed, 8257CS- (8257 Chip Select) is asserted at 1G pin 11. The actual transfer occurs when the 8086 asserts either RD- at 1G pin 1 or WR- at 1G pin 2 while 8257CS- is active. DMA is never in progress while the 8257 is being programmed. When DMAEN- from inverter 4A pin 5 is high, the LA0+-LA7+ address lines from the 8086 is driven through transceiver 2G to the 8257. These address lines are used to select registers within the 8257. The input/output read and write pins of the 8257, 1G pin 1 and 1G pin 2, respectively, are bidirectional. They are inputs during programming of the 8257 and outputs when HLDA+ is high.

DMA Operations

The 8257 and the 8086 are the two sources for the LA0+-LA13+ address lines and the BHE- line on the CPU Board. During non-DMA bus cycles (HLDA+ is low), the address is driven by the tristate latches at 3G, 4G, and 6G. After HLDA+ goes active, the 8257 asserts ADSTB+ (Address Strobe) at 1G pin 8, which loads bits 8 through F of the address into the latch at 5G, the outputs of which are connected to the LA8+-LAF+ address lines. During a DMA read or write cycle, BHE- is always the same state as the LA0- line from pin 6 of gate 4C.

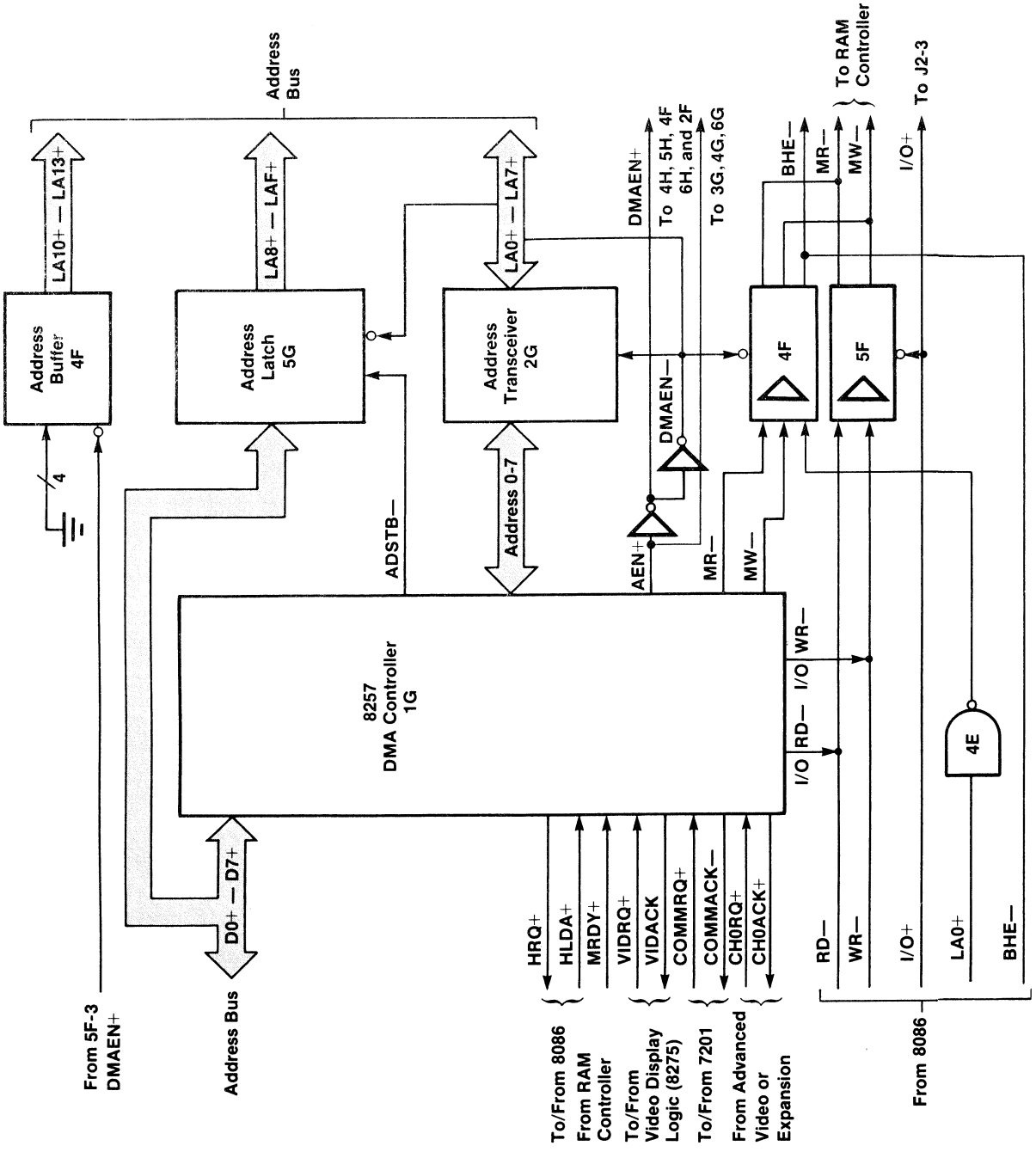


Figure 3-16. DMA Logic.

Next, the 8257 drives LA0+-LA7+ on its address lines to transceiver 2G and asserts AEN+ (Address Enable) at 1G pin 9 to enable the address drivers. AEN+ is buffered and inverted at 5F pin 3 and 4A pin 5 to make DMAEN+ and DMAEN-. DMAEN+ disables the 8086 address drivers 3G, 4G, and 6G, and DMAEN- enables the DMA address from the transceiver at 2G and drivers at 4F and 5G. During programming, the address lines of the 8257 are inputs. When HLDA+ is high from the 8086, they are outputs. Note that during a DMA cycle, the drivers at 4F pins 12, 14, 16, and 18 drive address lines LA10+-LA13+ low, which cause all DMA accesses to occur in the first 64 kilobytes of RAM. The FDC or HDC Board asserts ADRDIS- (Address Disable) to disable 4F. The FDC or HDC Board can then supply the four high-order address lines, LA10+-LA13+.

During the time that HLDA+ is low, the memory read and write pins of the 8257, 1G pins 3 and 4, are not used. When HLDA+ is high, a DMA cycle is in progress and both pins are outputs. The input/output read and write strobes access the input/output device, and the memory read and write strobes access the memory.

The signals MR- and MW- can originate at the 8257 through pins 7 and 9 of the drivers at 4F or from the 8086 through pins 14 and 12 of the drivers at 5F. When the 8086 is performing memory cycles, the I/O+ (Input/Output) signal from pin 8 of gate 3D is low. During input/output cycles, the 8086 drives M+/IO- low forcing I/O+ high; during DMA cycles, DMAEN- is active at pin 9 of 3D so that I/O+ stays high. The 5F drivers are enabled when I/O+ is low during non-DMA cycles, and the 4F drivers are enabled by DMAEN-.

Input/output reads and writes are always controlled by RD- and WR-. The 8086 RD- and WR- pins are connected parallel with the 8257 IORD- (Input/Output Read) and IOWR- (Input/Output Write) pins. The 8086 drives them only when HLDA+ is low, and the 8257 drives them only when HLDA+ is high. During 8086 input/output accesses, the address decoders 2F and 3F select the input/output device for the transfer. During DMA, DMAEN+ disables the address decoders at 2F pin 4, and the device acknowledge lines from the 8257, COMMACK- (Communications Acknowledge), VIDACK- (Video Acknowledge), and CH0ACK-

(Channel 0 Acknowledge), select the input/output device.

Once the input/output device is selected, the 8257 uses two different sets of bus transceivers to transfer data between an input/output device and the RAM array.

When the 8257 is performing a DMA operation from an input/output device to a location in the RAM array, transceivers 1F and 11E are used for the even byte transfer, and transceivers 9F and 10E are used for the odd byte transfer. When the even data byte from the input/output device becomes available on the D0+-D7+ data lines, it is sent through transceiver 1F to AD0+-AD7+ and then to BDATA0+-BDATA7+ through transceiver 11E. Transceiver 1F is enabled by NORMCYC- at pin 12 of OR gate 14C to pin 10 of 4C where it is NANDed at pin 9 with a high LA0- (inverted from LA0+ at pin 6 of 4C). The direction of 1F from the D0+-D7+ data lines to the AD0+-AD7+ lines is set by the low RAMMR+ at pin 5 of 8F and a low RD- from pin 7 of buffer 5F. Transceiver 11E is enabled by a low LA0+ and a low RAMCYC- at pins 12 and 13, respectively, at gate 8F. The direction of 11E from the AD0+-AD7+ address/data lines to the RAM array's BDATA0+-BDATA7+ data lines is set by a high at pin 8 of gate 8F since MR- and LA13+ are both low at pins 10 and 9 of gate 8F, respectively.

During the next DMA cycle, the odd byte of data from the input/output device appears on the D0+-D7+ data lines. The byte is sent through transceiver 9F to the AD8+-ADF+ address/data lines. Transceiver 9F is enabled when an odd byte is to be transferred by a high LA0+ at pin 1 of NAND gate 4C and a high at pin 2 of 4C. The resulting low at pin 3 of 4C enables transceiver 9F at pin 19. Transceiver 9F's direction is set from D0+-D7+ to the AD0+-AD7+ by a low RAMMR+ and a low RD-, which are ANDed at pin 6 of 8F, inverted at pin 8 of 10G, and sent to the pin 1 DIR (Direction) input of 9F. Transceiver 10E is enabled by a low RAMCYC- and a low BHE- at pins 5 and 4, respectively, at gate 3B. The low pin 6 output of 3B enables 10E at pin 19. The direction of transceiver 10E is set by the high at pin 8 of 8F but inverted at pin 10 of 10G.

When the DMA transfer is from the RAM array to an input/output device, the 8257 addresses the RAM

array as described above. Again, assuming an even byte transfer first (LA0+ = 0), the byte from the RAM chips drive the BDATA0+-BDATA7+ data lines. Transceiver 11E is enabled by a low LA0+ and BHE- at pins 12 and 13 of gate 8F. The direction from the BDATA0+-BDATA7+ lines to the AD0+-AD7+ address/data lines is set by a low MR- and a low LA13+ at pins 10 and 9 of gate 8F. The lower byte on the AD0+-AD7+ lines is sent to transceiver 1F, which is enabled by a low NORMCYC- (through pin 11 of NOR gate 4C from the memory logic) to pin 10 of 4C and a high LA0- at pin 9 of 4C. The low at pin 8 of 4C is sent through pin 8 of gate 4E to the pin 19 EN- input of transceiver 1F. Transceiver 1F's direction is set by a high at pin 3 of gate 8G to drive the even byte of data to the D0+-D7+ data lines and to the selected input/output device.

During the next DMA cycle, the odd byte from the RAM array (LA0+ = 1) appears at the inputs to transceiver 10E. The direction of 10E is set to drive the data byte from the BDATA8+-BDATAF+ lines to the AD8+-ADF+ lines by a high RAMMR+ from pin 10 of inverter 10G. The odd byte is sent on the AD8+-ADF+ lines to transceiver 9F, which is enabled by a high LA0+ line at pin 3 of NAND gate 4C. The direction of 9F is set by a high at pin 3 of gate 8G inverted at pin 8 of 10G.

Cluster Communications Logic

Cluster communications are based on an NEC 7201 (or Intel 8274) Multi-Protocol Serial Controller (MPSC). Although the 7201 has two channels, only Channel A is used for cluster communications. Channel B is used as the keyboard interface.

Figure 3-17 below shows the functional blocks of the cluster communications logic. Also see the 8086 CPU Board schematic, Figure 3-14 above, during the following discussion.

7201 Programming

As shown on page 4 of Figure 3-14, the 7201 is programmed through the eight data bus lines, D0+-D7+ when SIOCS- (Serial Input/Output Chip Select) is low at 2F pin 12, and RD- is low at pin 22 of 9G or WR- is low at pin 21 of 9G. LA1+ and LA2+

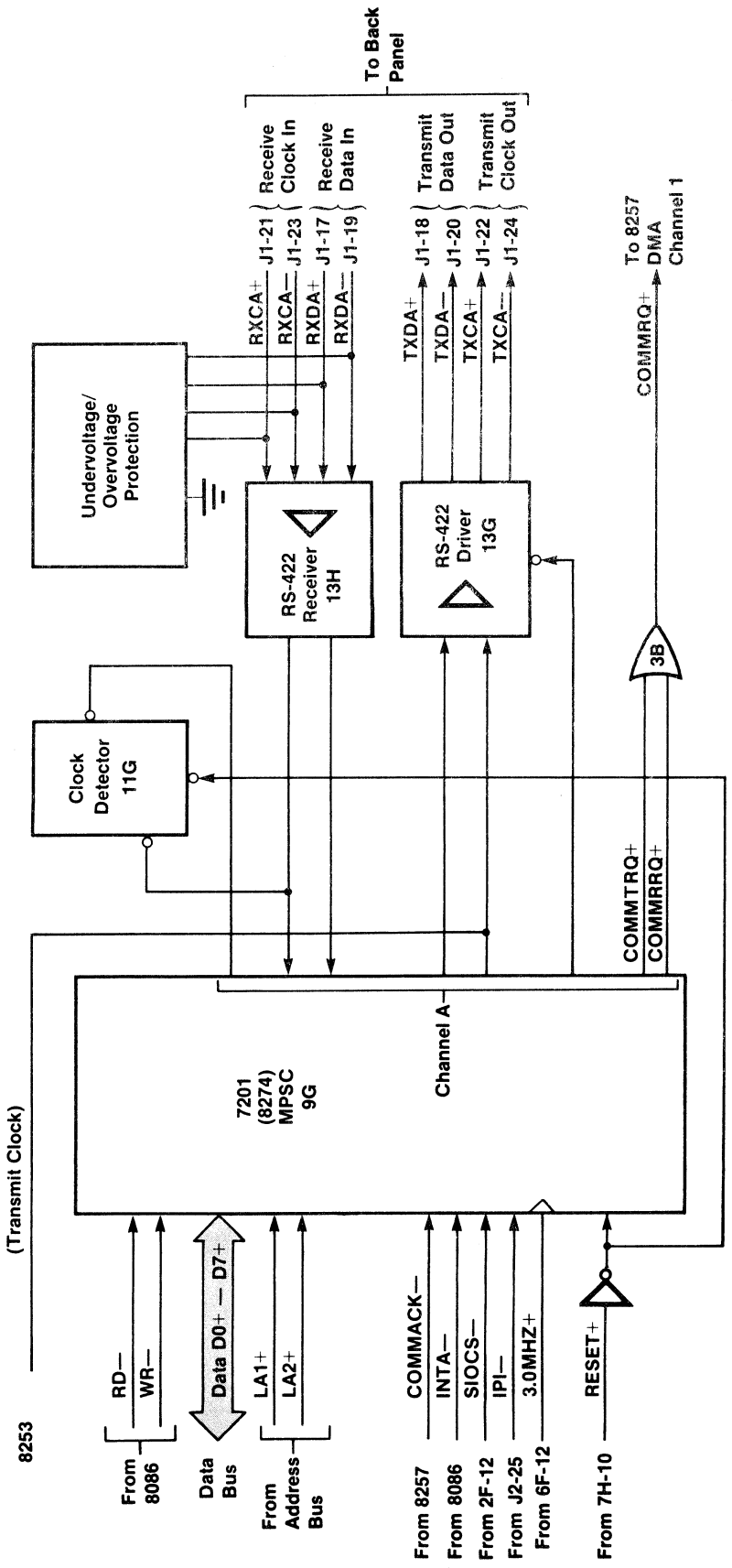


Figure 3-17. Cluster Communications Logic.

at 9G pins 24 and 25 are used to select the individual registers within the 7201. Interrupt acknowledgements and the use of INTA- at 9G pin 27 are described in "Interrupt Logic" below.

Cluster communications operate under the control of DMA Channel 1. Once programmed, the 7201 asserts one of two signals to transfer data to or from memory, either COMMTRQ+ (Communications Transmit Request) at 9G pin 11, or COMMRRQ+ (Communications Receive Request) at 9G pin 32. Gate 3B pin 8 ORs the two requests to generate COMMRQ+ (Communications Request). COMMRQ+ is sent to the 8257 to transfer data to or from the data bus when RD- or WR- goes low. Once the transfer is complete, the 7201 takes COMMRQ+ low.

Communications Signals

The cluster workstations are connected by four wires: two for data and two for the clock. Each pair consists of two RS-422 differential lines: one positive signal and one complement signal. All data transmission is half-duplex, since there is only a single data pair. The communications line is multidrop, that is, whichever workstation is driving the line always drives both the data and clock signals. All receivers on the cluster use the clock that is currently on the communications line, never an internal clock.

The four cluster signals are series-terminated, with 1-kilohm resistors R7, R8, R9, and R10. Diodes CR2-CR10 provide overvoltage and undervoltage protection for the receivers by shunting those voltages to ground. Overvoltages go through switching diodes and then through the reverse-biased 5.1-V dc Zener diode CR10. Undervoltages go directly through the switching diodes to ground.

The receive clock comes onto the CPU Board at J1 pins 21 and 23 as RXCA+ and RXCA- (Receive Clock Channel A). The receiver at 13H converts them to a single TTL receive clock signal at 13H pin 11. This signal is used to clock the receive data into the 7201 at 9G pin 35. It also goes to the clock detect one-shot at 11G pin 5. The one-shot is used to determine when the line is being driven; its output drives the Channel A DCDA- (Carrier Detect) input to the 7201. When there is no clock present on the communications line,

the one-shot returns to its stable state and deactivates carrier detect.

Receive data comes from J1 pins 17 and 19 as RXDA+ and RXDA- (Receive Data Channel A). They are received and converted to a single TTL receive data signal by the RS-422 receiver at 13H pin 13. This signal is connected to the receive data input of the 7201 at 9G pin 34.

The transmit clock is generated by Counter 1 of the 8253, described above in "Architecture" under "Cluster Communications Baud Rate." The transmit clock goes to the 7201 to time the transmit data at 9G pin 36. It also goes to the RS-422 drivers at 13G pin 9. Transmit data goes directly from the 7201 to the transmit driver at 13G pin 15. The drivers are tristate devices enabled by the Channel A request-to-send output of the 7201, 9G pin 38.

Keyboard Interface Logic

Channel B of the 7201 is used with a standard asynchronous protocol to communicate with the keyboard. Figure 3-18 below shows the functional blocks of the keyboard interface logic. Also see page 5 of Figure 3-14 above, the 8086 CPU Board schematic, during the following discussion, which describes in detail the functional blocks of the Keyboard Interface Logic.

The 76KHZ+ clock signal is connected to the 7201 at 9G pins 4 and 7. This clock provides communications between the 7201 and the keyboard at 1200 baud when the divide-by-64 mode is selected in the 7201. Transmit data is sent from the 7201 to the keyboard through the buffer at 12G pin 3. Receive data is received from the keyboard at 12H pin 15 and, after it is buffered, is connected to the receive data input at 9G pin 9.

Timer Logic and Speaker Interface

As shown on page 5 of Figure 3-14 above, the 8086 CPU Board schematic, the Intel 8253 timer at 11H is a programmable counter/timer element with three fully independent 16-bit channels. Figure 3-19 shows the functional blocks of the timer logic and speaker interface.

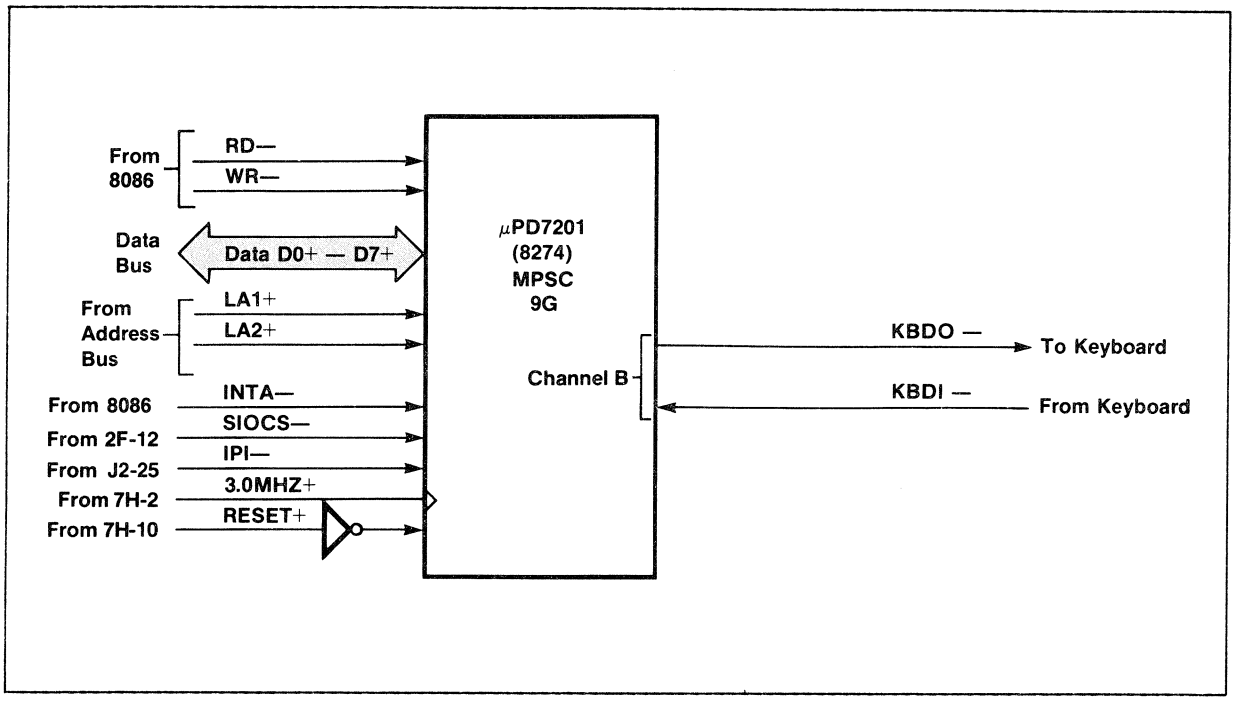


Figure 3-18. Keyboard Interface Logic.

8253 Programming

The three counter channels of the 8253 are used as the tone generator, cluster communications clock, and programmable timer interrupt source. The assignment and input frequency of each counter are:

Counter	Assignment	Input Clock Frequency
0	Tone generator	1.23 MHz
1	Cluster communications clock	1.23 MHz
2	Timer interrupt	76 kHz

Eight data bus lines, D0+-D7+, are connected to the 8253 for communications with the 8086. During input/output access to the 8253, the signal 8253CS- (8253 Chip Select) from the address decoder 2F (on page 3 of Figure 3-14 above) selects the timer. The actual transfer of data between the 8086 and the 8253 to program the

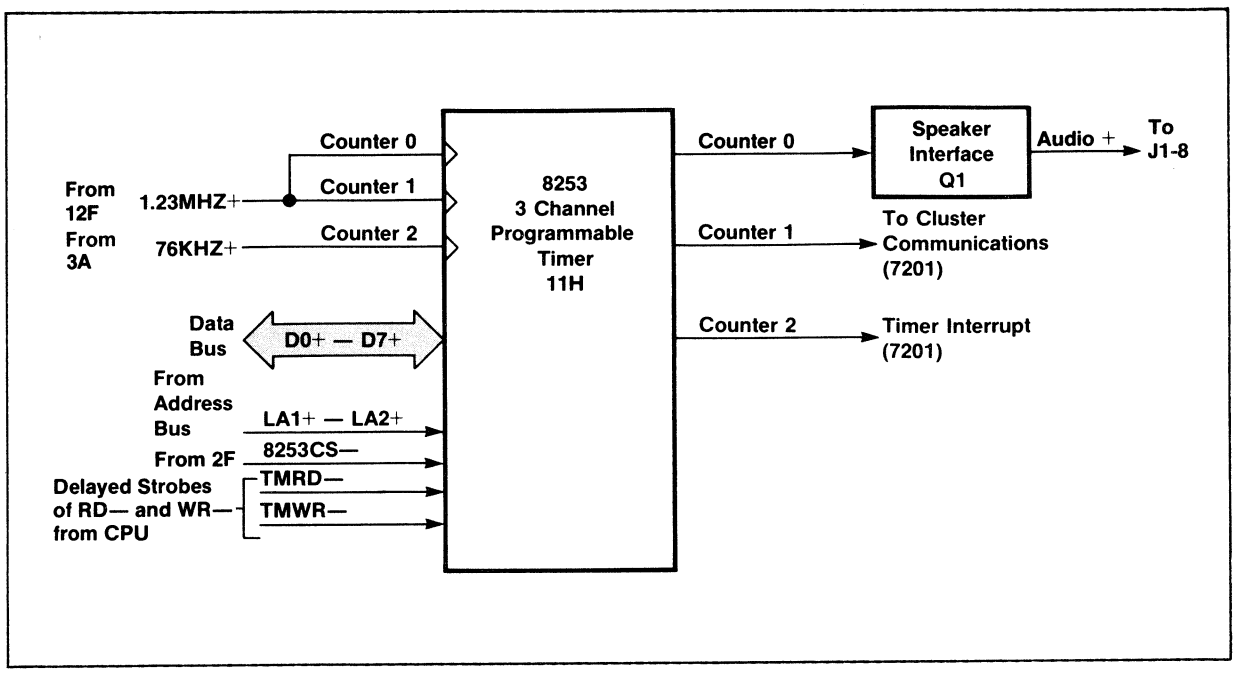


Figure 3-19. Timer Logic and Speaker Interface.

timer channels occurs when either TMRD- (Timer Read Strobe) at 11H pin 22, or TMWR- at 11H pin 23 goes low. TMRD- and TMWR- (Timer Write Strobe) are the RD- and WR- strobes conditioned at gate 3E pins 8 and 11, respectively, by the pin 19 output of shift register 2E (as shown on page 4 of Figure 3-14). The RD- and WR- strobes must be delayed to meet the timing requirements of the 8253 when used with the 8-MHz 8086. Address lines LA1+ and LA2+ are used to select a particular register within the 8253. The programming information for the 8253 is described in the "Architecture" section for the particular channel used.

Speaker Interface

The speaker frequency is determined by Counter 0 of the 8253 timer, as described in the section above and in the "Architecture" section under "Speaker Interface." As shown on page 5 of Figure 3-14 above, the signal from the 8253 is amplified by R12, R13, and Q1 and then shaped by R14 and C111 before going to the speaker through J1 pin 8.

Interrupt Logic

Interrupts on the 8086 CPU Board are controlled by the 8086 microprocessor and a 7201 MPSC both on the CPU Board and an 8259A interrupt controller on either the FDC or HDC Board. All interrupts in the 8086 are software maskable. Both the 7201 and 8259A provide individual masking, vector generation, and priority setting. The 8259A handles CPU Board interrupts as well as interrupts from FDC or HDC Board sources, such as the disk controller or RS-232-C communications logic. Interrupts passing through the 8259A from the 8086 CPU Board are given the highest priority (see "Bus Interface and Interrupt Control Logic" for the FDC or HDC Board below).

The sources for interrupts on the CPU Board are:

- the keyboard interface,
- the cluster communications interface, and
- Counter 2 of the 8253 counter/timer chip.

Programming the 7201 is described above in the "Architecture" section under "Cluster Communications."

Figure 3-20 below shows the functional blocks of the interrupt logic. Also see page 4 of Figure 3-14 above, the 8086 CPU Board schematic, during the following discussion.

The Counter 2 output of the 8253 timer chip is connected to the DCDB+ (Channel B Carrier Detect) input of the 7201 at 9G pin 5. This is done so that the timer causes external status interrupts for Channel B. The other two interrupt sources are handled internally in the 7201.

The 7201 asserts its interrupt output at 9G pin 28 to signal an interrupt request to the 8086. The interrupt signal is buffered and inverted at 10G pin 4 to make ONBDINT+ (On-Board Interrupt). ONBDINT+ is sent to the pin 19 INT1+ (Interrupt Priority 1) input of the 8259A on the FDC or HDC Board. The resulting interrupt request is sent to the 8086 as INTR+ at pin 14 of the J1 Motherboard connector.

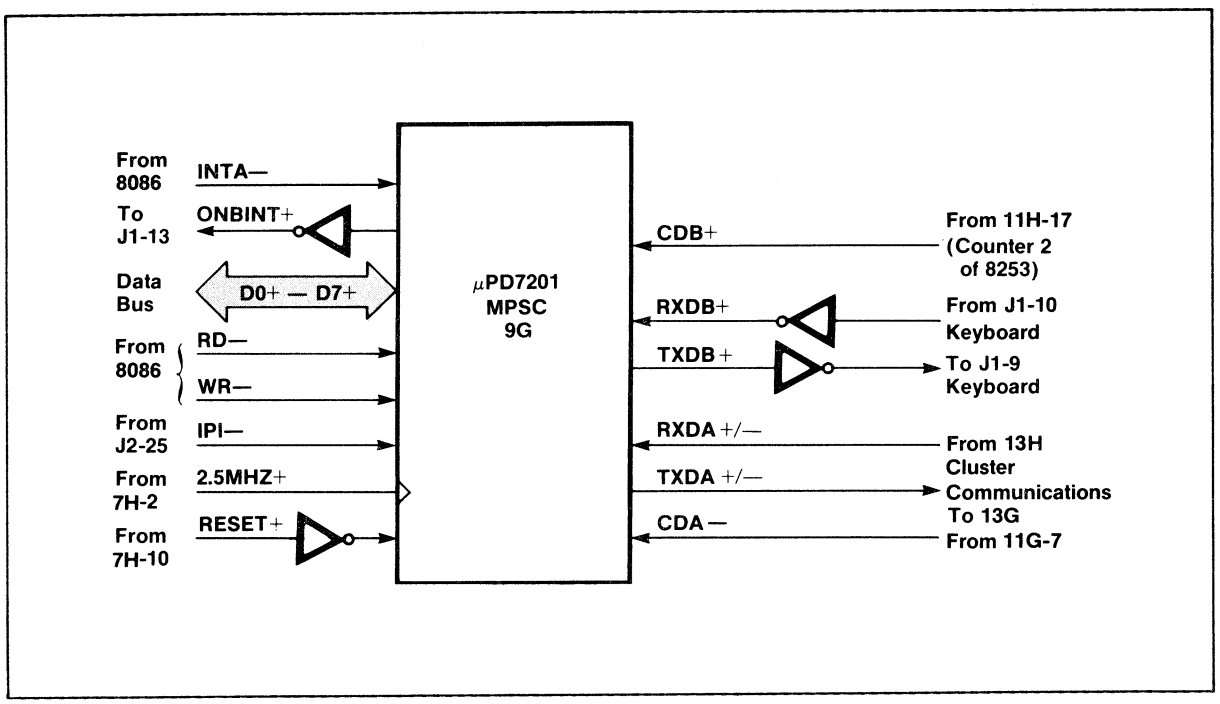


Figure 3-20. Interrupt Logic.

The 8086 asserts INTA- twice at 7F pin 24 to acknowledge each interrupt. The first pulse is used by the 8259A on the FDC or HDC Board to assign the interrupt priority. The second pulse is used to read an interrupt vector from the controller to the 8086.

INTA- is connected to the 7201 at 9G pin 27. The 7201 determines the proper vector during the first of a pair of INTA- pulses and drives the data bus lines, D0+-D7+ (and AD0+-AD7+ through transceiver 1F), with the vector during the second pulse if IPI- is low. The 8259A on the FDC or HDC Board can drive the IPI- (Interrupt Priority In) signal high at J2 pin 25 to cause the 7201 to not send its interrupt vector to the 8086. The 8259A then drives the interrupt vector onto D0+-D7+. IPI- is connected to the 7201 at 9G pin 29.

Video Display Control Logic

The video display control logic is used to interface the 8086, the 8257, and, if installed,

an advanced video board to the CRT Deflection Board. It provides control of:

- o the video display raster;
- o video display refresh;
- o font ROM output to pixel conversion;
- o half-bit shift;
- o full- and half-brightness video display; and
- o reverse video, blanking, and blinking.

The video display control logic is based on the Intel 8275 CRT controller and uses DMA Channels 2 and 3 to refresh the video display from memory. Figure 3-21 shows the functional blocks of the video display control logic. Also see the 8086 CPU Board schematic, Figure 3-14 above, during the following discussion.

8275 Programming

As shown on page 6 of Figure 3-14 above, the 8275 at 15G is programmed from data lines D0+-D7+ when 8275CS- (8275 Chip Select) is low and either RD- or WR- is low. Address line LA1+ is used to select among the internal registers in the 8275. Further programming information is described above in the "Architecture" section under "Direct Memory Access" and "Video Display Control."

3301 Programming

An NEC 3301 is used as a second source for the Intel 8275. A set of socket pins at 16 G next to the 8275 is used for mounting the 3301. The software requirements of the 3301 are incompatible with those of the 8275. See the 1981 Catalog published by NEC Microcomputers, Inc., for programming information.

Video DMA

After it is programmed, the 8275 asserts VIDRQ+ (Video DMA Request) at 13G pin 5 when it requires data. VIDRQ+ goes to the 8257 at 1G (page 2 of

Figure 3-14) to request a DMA cycle. The 8257 responds by asserting VIDACK- (Video Acknowledge). After asserting MEMR- (Memory Read) to read data from the RAM array, the 8257 asserts IOW- (Input/Output Write) to transfer the data to the 8275 from data bus lines D0+-D7+.

Raster

The video display raster is controlled by the 8275 with the HRTC+ (Horizontal Retrace) output at 15G pin 7 and the VRTC+ (Vertical Retrace) output at 15G pin 8. HRTC+ is sent to the RS-422 differential driver 14H which drives this signal as HORDR+ and HORDR- (Horizontal Drive) to the CRT Deflection Board. The vertical retrace signal is pipelined once at 12G pin 9 before being driven to the video display by 15H as VERDR+ and VERDR- (Vertical Drive).

Refresh

The 8275 has two row buffers that contain the character codes for the row currently being refreshed and the next row to be refreshed. It receives the character codes via DMA as described above. Each character requires 11 horizontal scan lines to display. The conversion from the character codes to pixel information is done by the font ROM at 18H. The conversion is based on the character code and the current raster line number within the character row being refreshed. Thus, each character code read into the 8275 is presented to the font ROM as an address 11 times, each time with a different raster line number.

In addition to the character codes, the video display refresh buffer contains field attributes that affect the appearance of the displayed characters. The 8275 processes these field attributes and generates the appropriate control outputs.

Pipeline registers 14F, 15F, 17F, 17G, and 17H are used to give the font ROM the longest possible access time and to ensure that propagation delays do not affect the video display quality. If an advanced video board (see

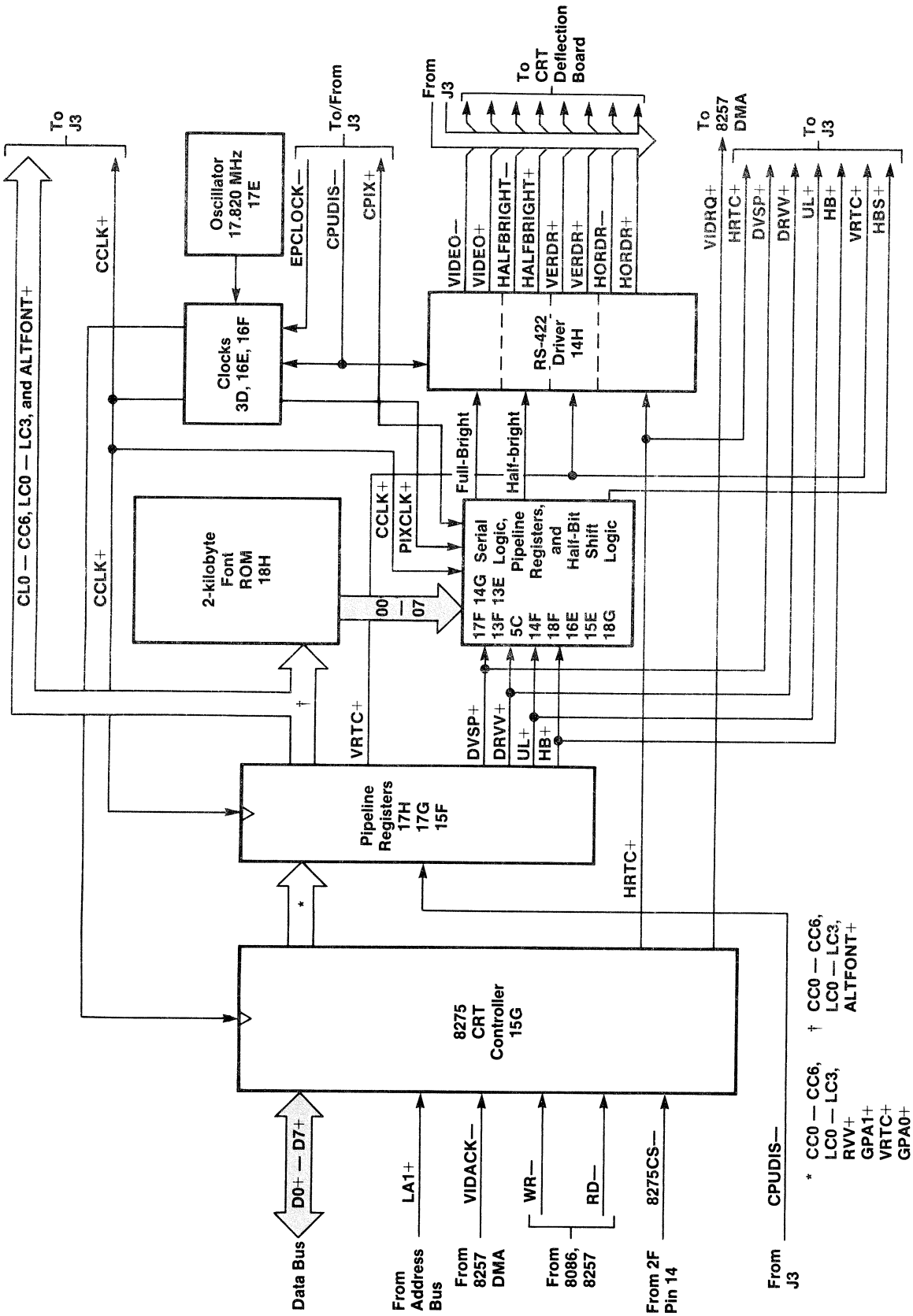


Figure 3-21. Video Display Control Logic.

below) is attached to the J3 connector and enabled, some alternate pipelining may occur.

The character codes from the 8275 are driven from 15G pins 23 through 29 to pipeline register 17H. They are then used to directly address the font ROM, 18H, and are also sent to the advanced video board at the J3 connector on the CPU Board. The raster line number is generated by the 8275 on 15G pins 1 through 4. These signals are pipelined at 17H, 17G, and also address the font ROM.

The 8275's GPA0 (General Purpose Attribute 0) is used to select the alternate font. Pin 33 of the 8275 is high when GPA0 is invoked. After pipelining at 15F pin 7, the attribute becomes the high-order address bit of the font ROM. The organization of the font ROM is described above in the "Architecture" section under "Video Display Control."

There are two types of characters in the font ROM: line-drawing and normal. Line-drawing characters are used to fill the rightmost and/or leftmost pixel of the 9-by-11-pixel character cell. As shown in Figure 3-22 below, normal characters fill the inner 7-by-11-pixel character cell. The last (highest-numbered) 64 characters in the 256-character font ROM are the line-drawing characters.

Characters are generated one raster line (9 pixels) at a time by the font ROM. They are converted to the bit-serial pixel data by the shift register 18G with the ninth bit coming from 14F pin 12. The first pixel shifted out corresponds to the leftmost pixel in the cell as it appears on the video display. The correspondence between displayed pixels and shift register inputs is shown below.

Pixel →	1 Left	2	3	4	5	6	7	8	9 Right
Input →	18G 14	18G 12	18G 11	18G 10	18G 5	18G 4	18G 3	18G 2	14F 12

Font ROM Output to Pixel Conversion

The serialization of the font ROM output to bit-serial pixel information depends on whether a line-drawing character is displayed and on the status of the underline attribute. When a line-drawing character is output, gate 15E pin 8 is high. This allows an alternate set of buffers in 18F to direct the O0-O2 ROM outputs to the inputs of shift register 18G in a different order. Figures 3-22 and 3-23 below show the order in which the bits are shifted out of 18G to the CRT Deflection Board for both a normal and a line-drawing character.

Underlines and Normal Characters. The CPU Board uses the reverse video attribute of the 8275 to generate underlines because the underline capabilities of the 8275 are incompatible with the video display control logic. When the RVV+ (Reverse Video) attribute pin of the 8275 at 15G pin 36 is high and the raster line 9 is being refreshed, gate 15E pin 12 goes high, which causes an underline to be displayed unless disabled (by an advanced video board) with CPUDIS- (CPU Disable) at pins 1 and 2 of gate 4E. This underline control signal is pipelined at 17G pin 5. The signal at 17G pin 5 disables the font ROM at 18H pins 18 and 20 and thus forces its outputs all high. Furthermore, with normal characters, through tristate buffers 18H pins 9 and 3, the underline control signal forces the outer two pixels of the 9-by-11-pixel character cell high.

For normal characters that are not underlined, this same path forces the outer two pixels low; the other seven pixels of the cell go directly from the font ROM to 18G, with the low-order bits at 18H pins 9 and 10 buffered at 18H pins 7 and 5.

Line-Drawing Characters. For line-drawing characters, the high leftmost pixel is driven by 18H pin 18 from output bit 0 of the font ROM. The next three pixels are driven by 18H pins 14 and 16 from output bit 2 of the font ROM; the rightmost pixel is driven by 18F pin 13 from output bit 1 of the font ROM. The other five pixels come directly from the font ROM in the same manner as the normal characters.

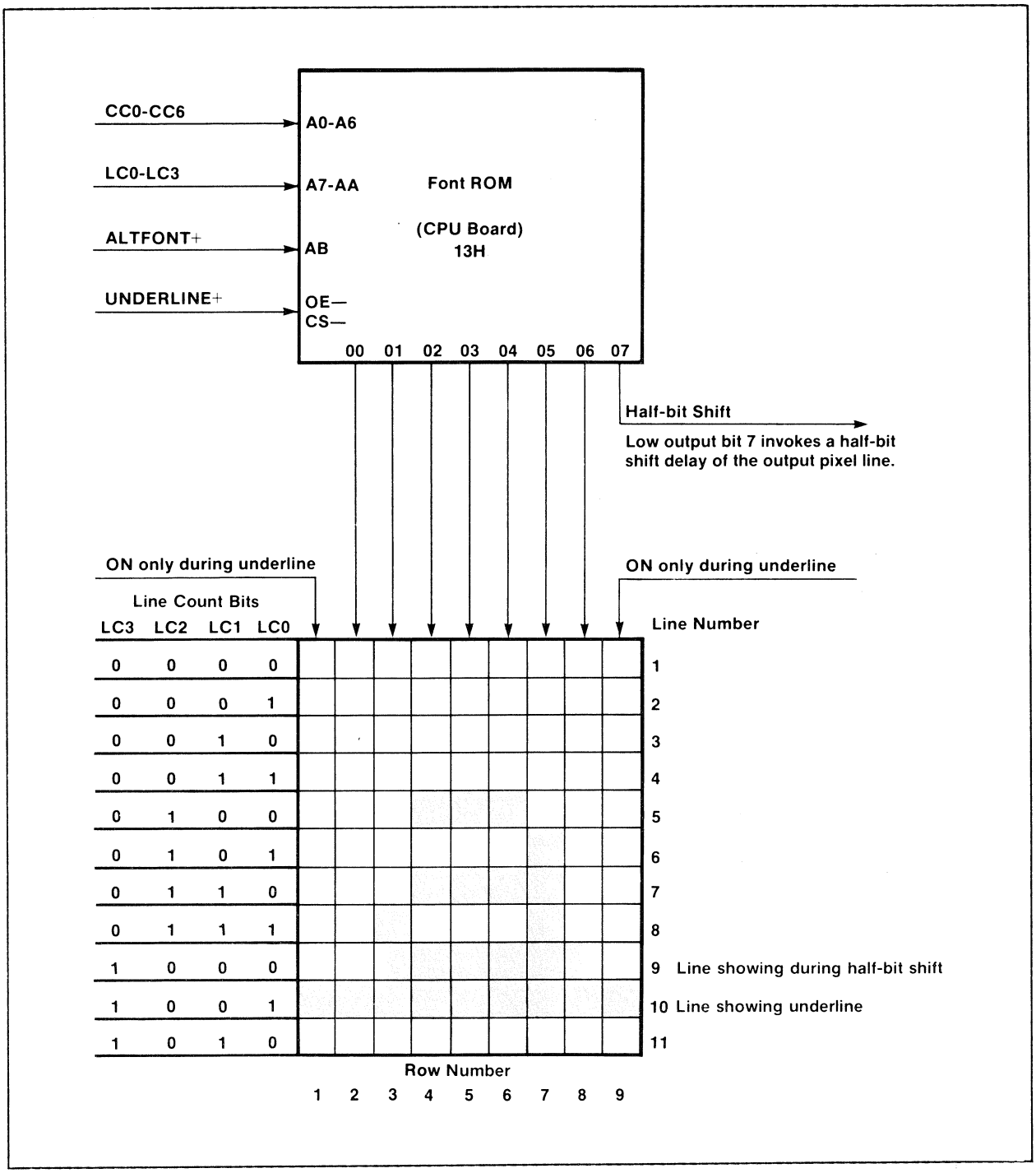


Figure 3-22. Generation of Normal Character 61h (Gate 15E Pin 8 = 0).

The line-drawing mode is enabled by gate 15E pin 8 when the alternate font attribute is on; that is, ALTFONT+ (Alternate Font) is high, and the high-order character code bit is high at 17H pin 2. For either type of character, the bit-serial pixel data is shifted out of 18G pin 13 at the pixel clock frequency of 17.820 MHz.

Half-Bit Shift

Output bit 7 of the font ROM is used to select half-bit shift. Half-bit shift delays all pixels of one raster line of a particular character in the font. This allows characters to have overlapped pixels, smoother characters, and better centering. The shifted line of pixels turns on and off at the falling, rather than at the rising, edge of the pixel clock so that the pixels are delayed by a half-pixel period.

The O7 output of the font ROM at 18H pin 17 is pipelined at 17F pins 15 and 14. When enabled, the pixel data from 18G pin 13 goes through 13F pin 8 and, when disabled, through 13F pin 11. The two streams of data are pipelined at 14F pin 6 for the shifted bits and 14F pin 16 for the unshifted ones. The exclusive-OR gate at 14G ORs the shifted and nonshifted pixel data at 14G pin 11.

Brightness

The video display has a half-bright mode under software control as one of several field attributes described in the "Architecture" section. When the video display data is to be half-bright, the 8275 asserts HLGT+ (Highlight) at 15G pin 32. HLGT+ is pipelined twice by CCLK+ (Character Clock) at 15F pins 10 and 15. From there, HLGT+ is pipelined by PXCLK+ (Pixel Clock) through 14F pin 18. Finally, HLGT+ is sent to gate 15E pin 6 through gates 14G pin 1 to provide a sufficient delay. HLGT+ is then buffered to the video display as HALFBRIGHT+ and HALFBRIGHT- by driver 14H pins 2 and 3, respectively.

Reverse, Blanking, and Blinking

Reverse video is controlled by the 8275's GPA1+ (General Purpose Attribute 1). GPA1+ at 15G pin

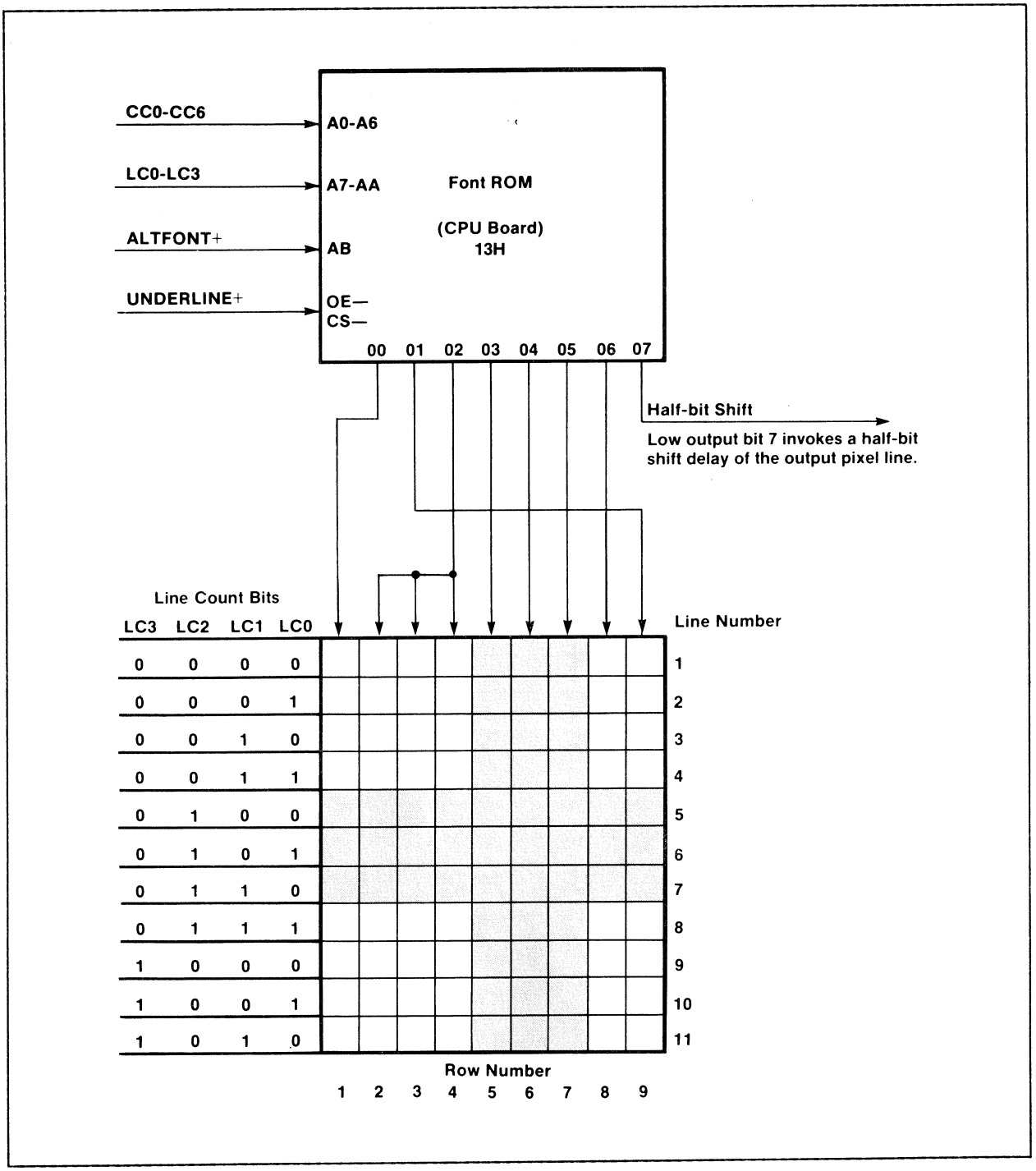


Figure 3-23. Generation of Line-Drawing Character C3h (Gate 15E Pin 8 = 1).

34 is pipelined at 17G pin 12, 17F pin 5, and 14F pin 5. GPA1+ is then exclusive-ORed with the pixel data at 14G pin 8.

Video blanking and blinking are controlled by the VSP (Video Suppress) output of the 8275 at 18G pin 35. VSP+ is pipelined at 17G pin 15 and 17F pin 4 and then gates off the video display data at 5C pin 8.

Advanced Video Board Interface

An advanced video board can be installed on the 8086 CPU Board. Connector J3 on the 8086 CPU Board provides various signals from the video display control logic to the advanced video board. When enabled, an advanced video board asserts CPUDIS-. CPUDIS- is gated through pin 3 of AND gate 3D to disable the 17.820 MHz pixel clock at 17E. Pin 3 of 3D is NORed with a substitute clock from the advanced video board, EPCLK- (External Pixel Clock), at pins 4 and 5 of 3D to clock counter 16F through pin 6 of inverter 16E. CPUDIS- also disables driver 14H at pin 4 so that the advanced video board logic can drive 14H's outputs to the CRT Deflection Board.

When an advanced video board is enabled, it generates the video clock, drives the video stream, and can add graphic, color, or additional font capabilities to the existing video display control logic. Table 3-1 lists the advanced video board signal name and J3 pin number, and gives a description of each signal.

Table 3-1. J3 Connector Pin Assignments. (Page 1 of 5)

Name	J3 Pin	Description
+5	1	+ 5 V dc
+5	2	+ 5 V dc
GPCS	3	Advanced video board select
LA0+	4	Local address bit 0 from latch 3G

Table 3-1. J3 Connector Pin Assignments. (Page 2 of 5)

Name	J3 Pin	Description
Ground	5	Ground
LA1+	6	Local address bit 1 from latch 3G
LA2+	7	Local address bit 2 from latch 3G
LA3+	8	Local address bit 3 from latch 3G
LA4+	9	Local address bit 4 from latch 3G
WAIT-	10	8086 wait request from advanced video board
3MHZ+	11	3-MHz DMA clock from 8257
DWAIT-	12	DMA wait request from advanced video board
D0+	13	Data bus bit 0 from/to 8086 and 8257
D1+	14	Data bus bit 1 from/to 8086 and 8257
D2+	15	Data bus bit 2 from/to 8086 and 8257
D3+	16	Data bus bit 3 from/to 8086 and 8257
Ground	17	Ground
D4+	18	Data Bus bit 4 from/to 8086 and 8257
D5+	19	Data bus bit 5 from/to 8086 and 8257
D6+	20	Data bus bit 6 from/to 8086 and 8257
D7+	21	Data bus bit 7 from/to 8086 and 8257
GIDIN-	22	Graphics input device input

Table 3-1. J3 Connector Pin Assignments. (Page 5 of 5)

Name	J3 Pin	Description
HBS+	56	Half-bit shift
CC6+	57	Character code bit 6 from 8275
CC4+	58	Character code bit 4 from 8275
CC2+	59	Character code bit 2 from 8275
CC0+	60	Character code bit 0 from 8275
Ground	61	Ground
RV+	62	Character attribute 0 (reverse video)
CC3+	63	Character code bit 3 from 8275
CC5+	64	Character code bit 5 from 8275
CCLK+	65	Character clock to advanced video board
CC1+	66	Character code bit 1 from 8275
CPIX+	67	Serial pixel output from 18G
LC0+	68	Line count bit 0 from 8275
Ground	69	Ground
LC1+	70	Line count bit 1 from 8275
LC3+	71	Line count bit 3 from 8275
LC2+	72	Line count bit 2 from 8275
+5	73	+ 5 V dc
+5	74	+ 5 V dc

FLOPPY DISK CONTROLLER (FDC) BOARD

Bus Interface and Interrupt Control Logic

Figure 3-24 below shows the functional blocks of the bus interface and interrupt control logic, which:

- buffers address, data, and control lines between the CPU Board and the FDC Board,
- selects various input/output devices or the bootstrap ROM on the FDC Board, and allows read and write operations between the CPU or 8257 and the input/output device or ROM,
- services interrupts from four FDC Board input/output devices as well as interrupts from the CPU Board, and
- provides 2.46-MHz and 1.23-MHz clocks for use by the FDC Board logic.

Refer to Figure 3-25, the FDC Board schematic, in addition to Figure 3-24, during the following discussion.

Buffers

As shown on page 2 of Figure 3-25, receivers 3D and 4D buffer control lines and the LA0+-LA4+ (Line Address) address lines from the CPU Board. The control lines from the CPU Board include RD- (Read) and WR- (Write) strobes, RESET-, a 9.8-MHz clock, EXP1DC- and EXP2DC- (Expansion Decode) input/output device enables, INTA- (Interrupt Acknowledge) and ONBDINT+ (On-Board Interrupt) interrupt controls, and TC+ (Terminal Count) and EXTACK- (External DMA Acknowledge) DMA controls. Transceiver 2D buffers the D0+-D7+ data lines to and from the FDC Board.

Address lines LA10+-LA13+ are output through the Extended Address Register at 8D for DMA operations. Transmitter 13D sends EXTRQ+ (External Request) for DMA, and IPI- (Interrupt Priority In) and INTR+ (Interrupt Request) interrupt controls to the CPU Board.

Table 3-1. J3 Connector Pin Assignments. (Page 5 of 5)

Name	J3 Pin	Description
HBS+	56	Half-bit shift
CC6+	57	Character code bit 6 from 8275
CC4+	58	Character code bit 4 from 8275
CC2+	59	Character code bit 2 from 8275
CC0+	60	Character code bit 0 from 8275
Ground	61	Ground
RV+	62	Character attribute 0 (reverse video)
CC3+	63	Character code bit 3 from 8275
CC5+	64	Character code bit 5 from 8275
CCLK+	65	Character clock to advanced video board
CC1+	66	Character code bit 1 from 8275
CPIX+	67	Serial pixel output from 18G
LC0+	68	Line count bit 0 from 8275
Ground	69	Ground
LC1+	70	Line count bit 1 from 8275
LC3+	71	Line count bit 3 from 8275
LC2+	72	Line count bit 2 from 8275
+5	73	+ 5 V dc
+5	74	+ 5 V dc

FLOPPY DISK CONTROLLER (FDC) BOARD

Bus Interface and Interrupt Control Logic

Figure 3-24 below shows the functional blocks of the bus interface and interrupt control logic, which:

- buffers address, data, and control lines between the CPU Board and the FDC Board,
- selects various input/output devices or the bootstrap ROM on the FDC Board, and allows read and write operations between the CPU or 8257 and the input/output device or ROM,
- services interrupts from four FDC Board input/output devices as well as interrupts from the CPU Board, and
- provides 2.46-MHz and 1.23-MHz clocks for use by the FDC Board logic.

Refer to Figure 3-25, the FDC Board schematic, in addition to Figure 3-24, during the following discussion.

Buffers

As shown on page 2 of Figure 3-25, receivers 3D and 4D buffer control lines and the LA0+-LA4+ (Line Address) address lines from the CPU Board. The control lines from the CPU Board include RD- (Read) and WR- (Write) strobes, RESET-, a 9.8-MHz clock, EXP1DC- and EXP2DC- (Expansion Decode) input/output device enables, INTA- (Interrupt Acknowledge) and ONBDINT+ (On-Board Interrupt) interrupt controls, and TC+ (Terminal Count) and EXTACK- (External DMA Acknowledge) DMA controls. Transceiver 2D buffers the D0+-D7+ data lines to and from the FDC Board.

Address lines LA10+-LA13+ are output through the Extended Address Register at 8D for DMA operations. Transmitter 13D sends EXTRQ+ (External Request) for DMA, and IPI- (Interrupt Priority In) and INTR+ (Interrupt Request) interrupt controls to the CPU Board.

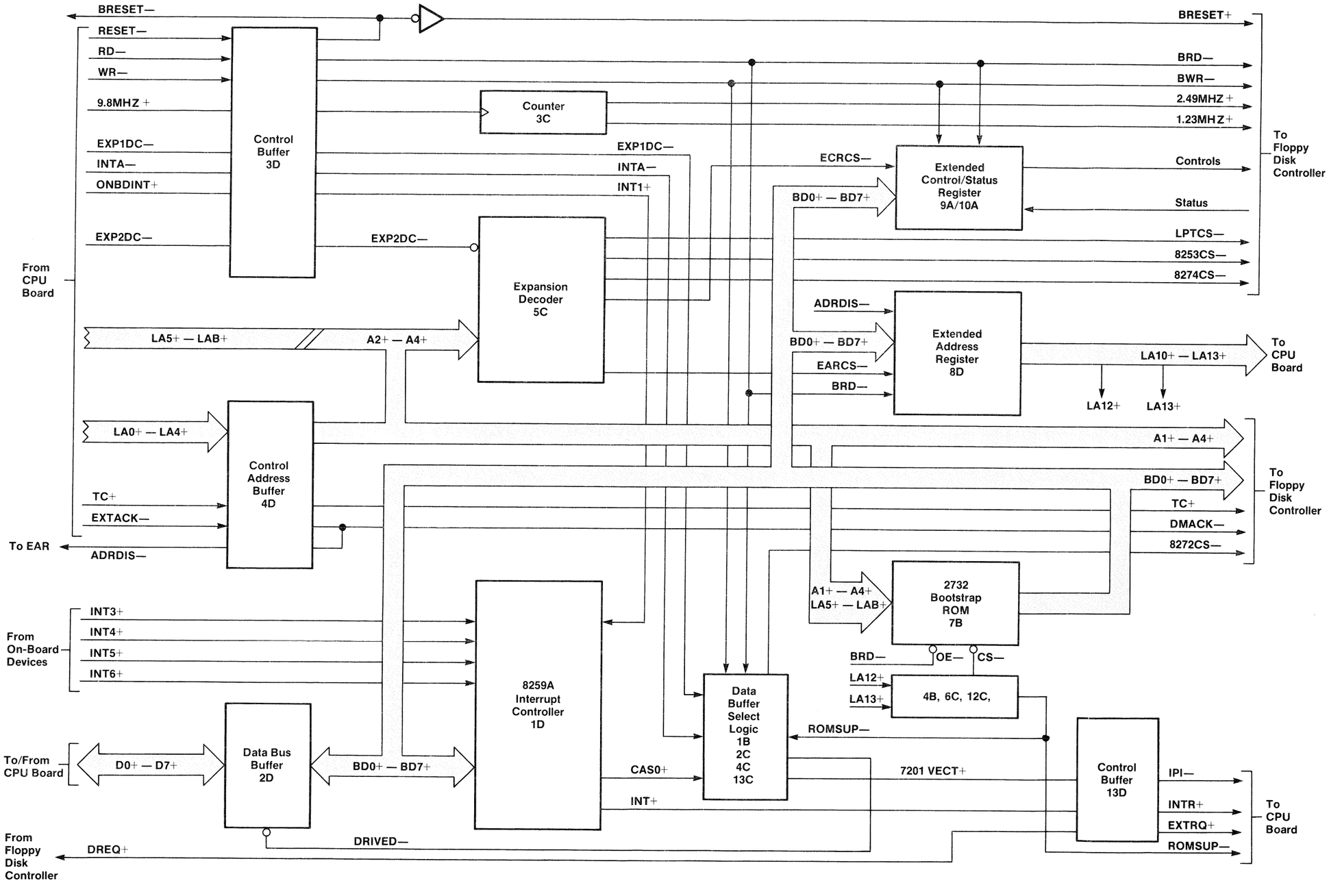


Figure 3-24. Bus Interface and Interrupt Control Logic.

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL DEVICES ARE STANDARD 4+8, 7+14, 8+16, 10+20 GROUND AND POWER CONNECTIONS.

POWER AND GROUND LOCATOR CHART					
REF. DES	TYPE	GND	+5	+12	-12
10D, 11D	1488	7		14	1
10B, 10C	1489	7	14		
11B, 11C	1489	7	14		
6A	8253	12	24		
1D	8259A	14	28		
1A	8272	20	40		
11A	8274	20	40		
7B	2732	12	24		

SPARE GATES		
TYPE	REF. DESIGNATOR(S)	QTY.
74LS04	2C	1
7414	4B	1
96LS02	7A	1
LM358	7D	1

REF. DESIGNATORS	
LAST USED	NOT USED
CR36	
RP2	
R26	
CR3	

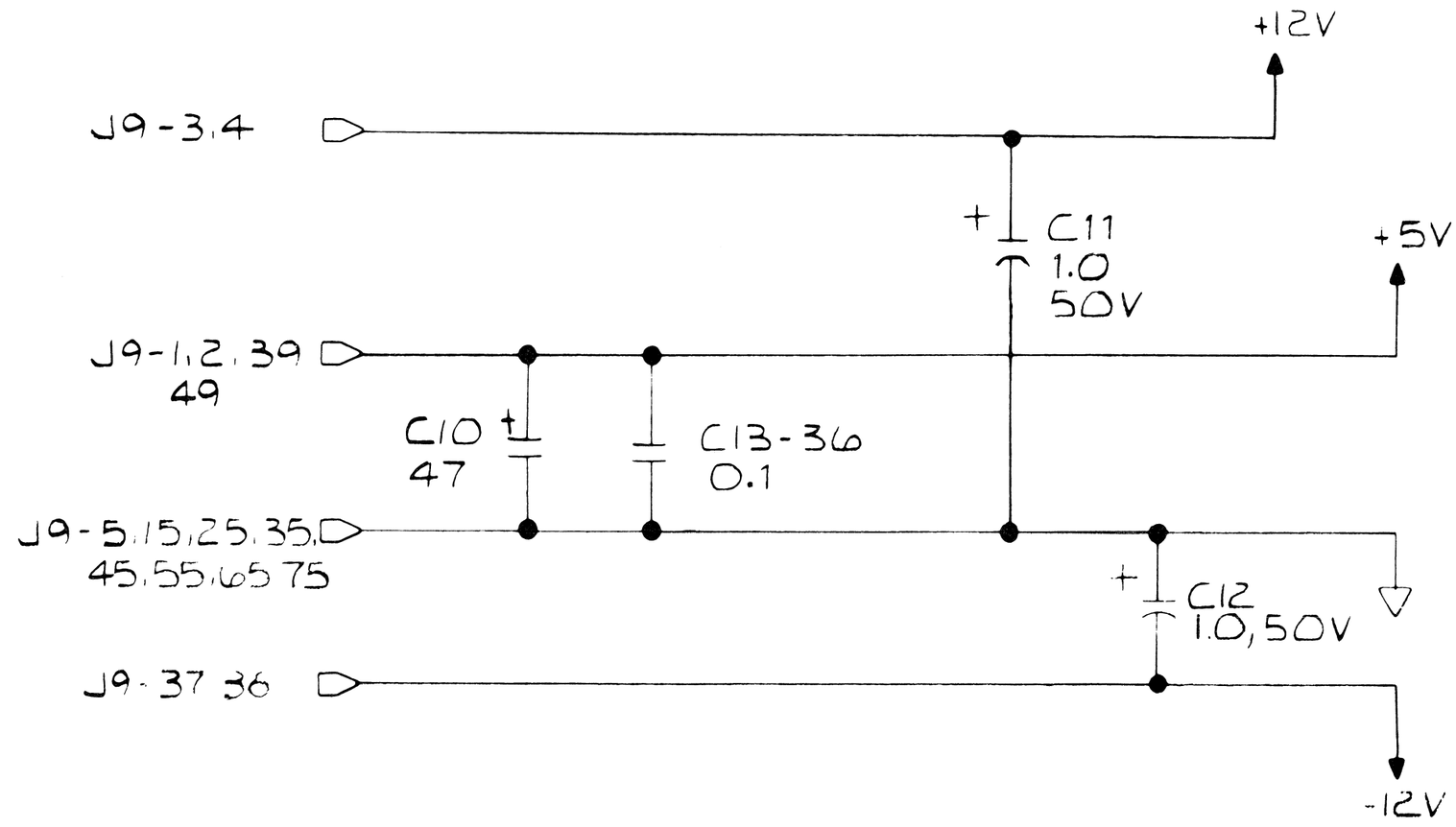


Figure 3-25. FDC Board Schematic. (Page 1 of 6)

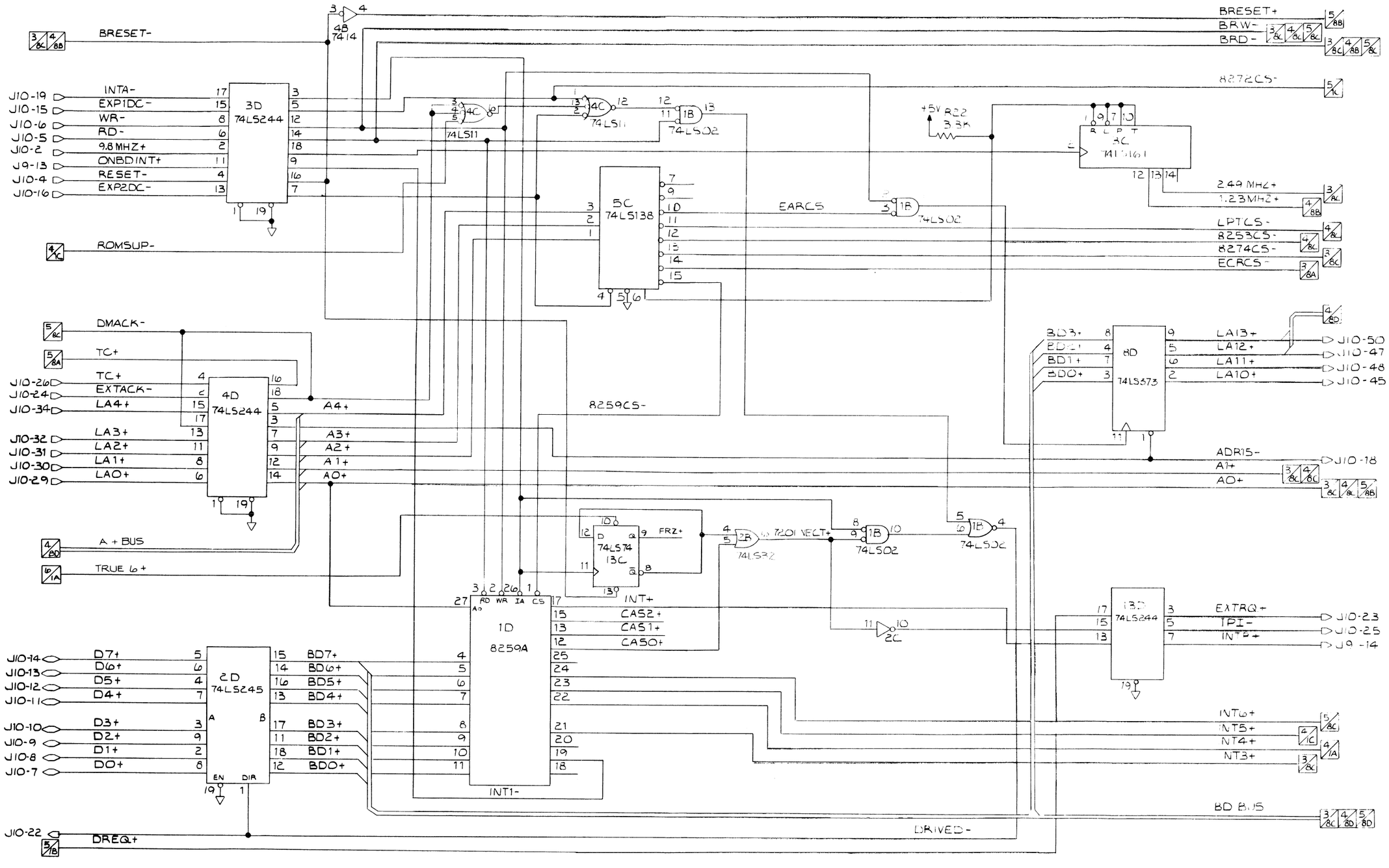


Figure 3-25. FDC Board Schematic. (Page 2 of 6)

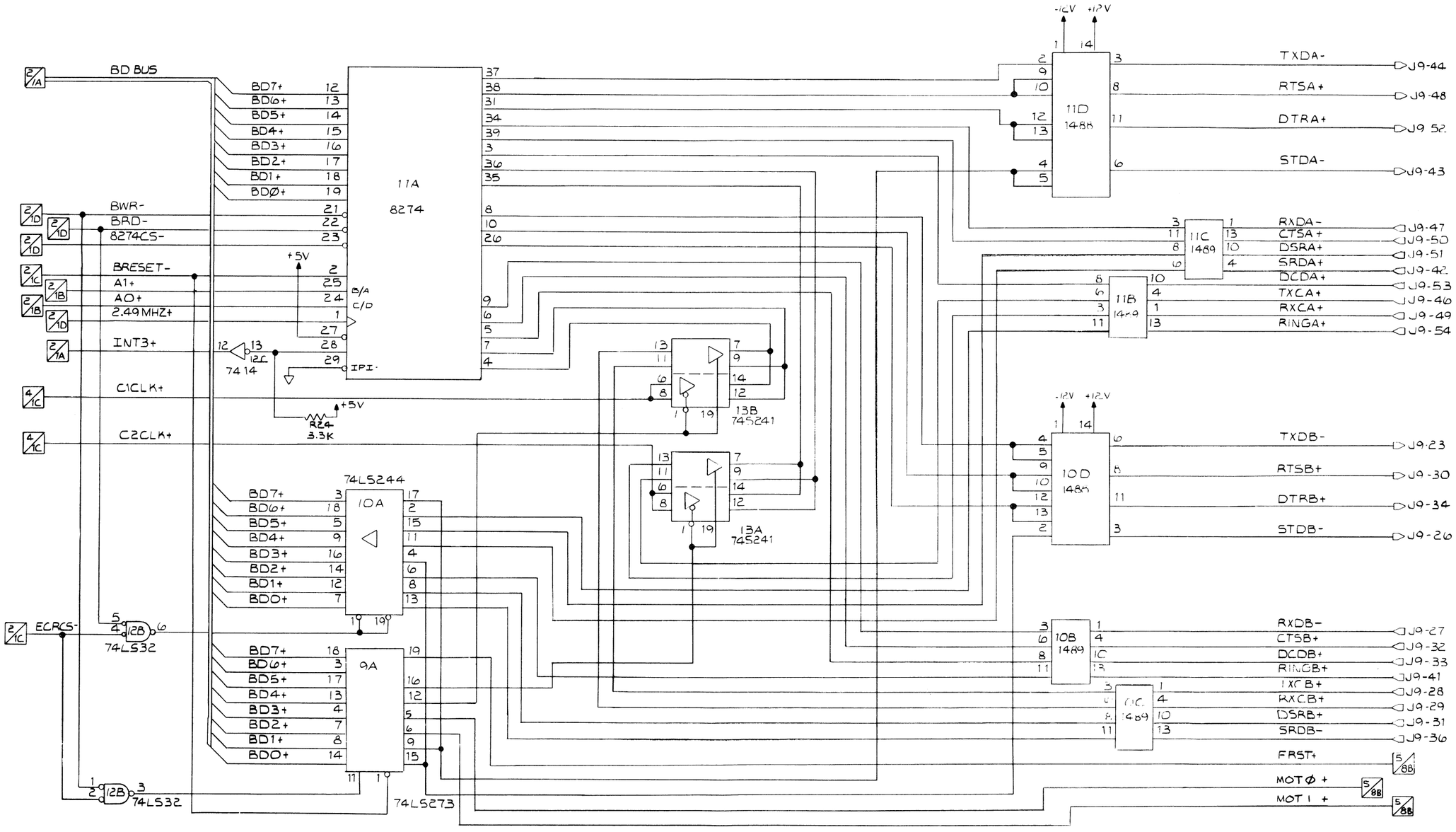


Figure 3-25. FDC Board Schematic. (Page 3 of 6)

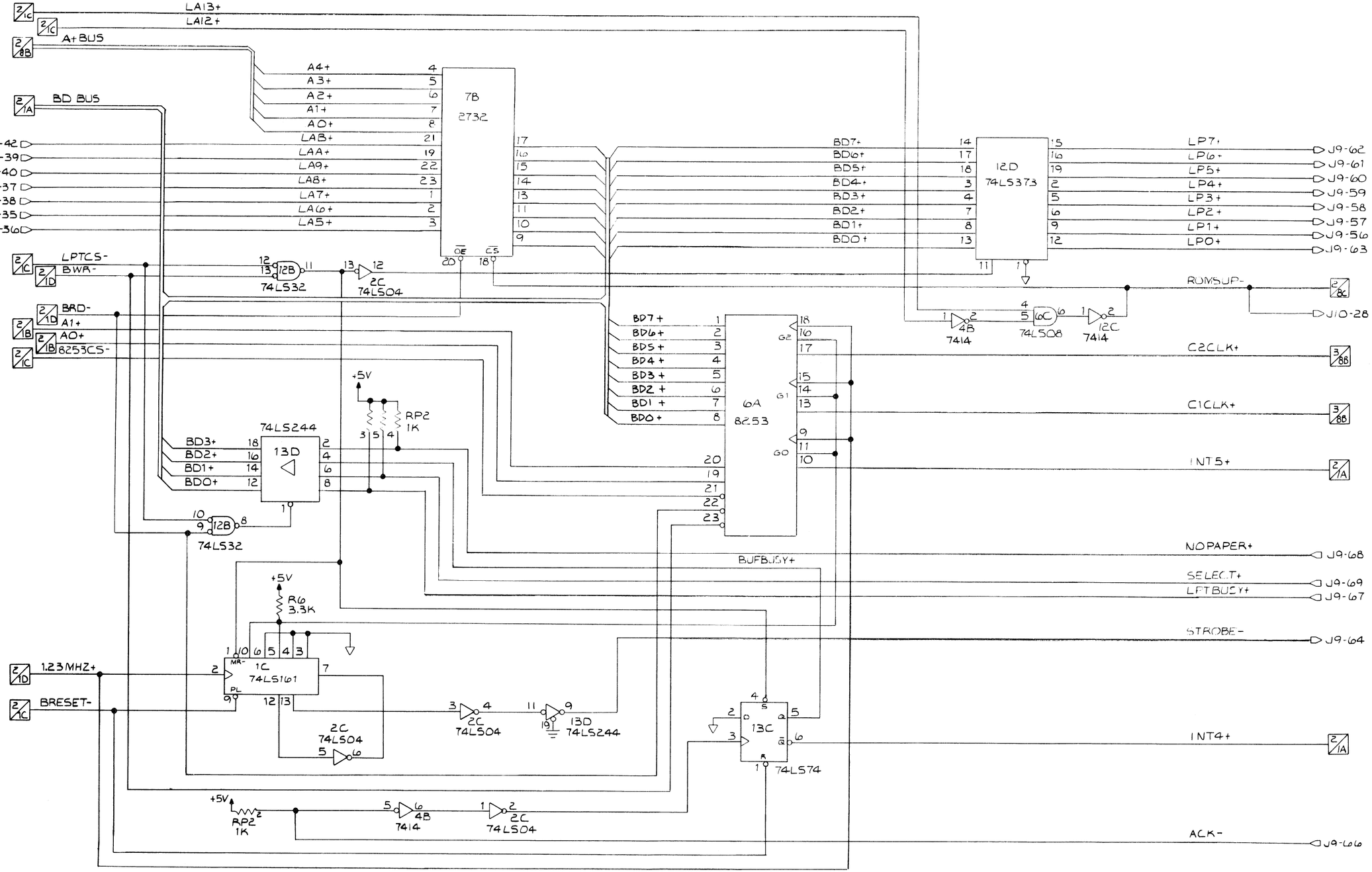


Figure 3-25. FDC Board Schematic. (Page 4 of 6)

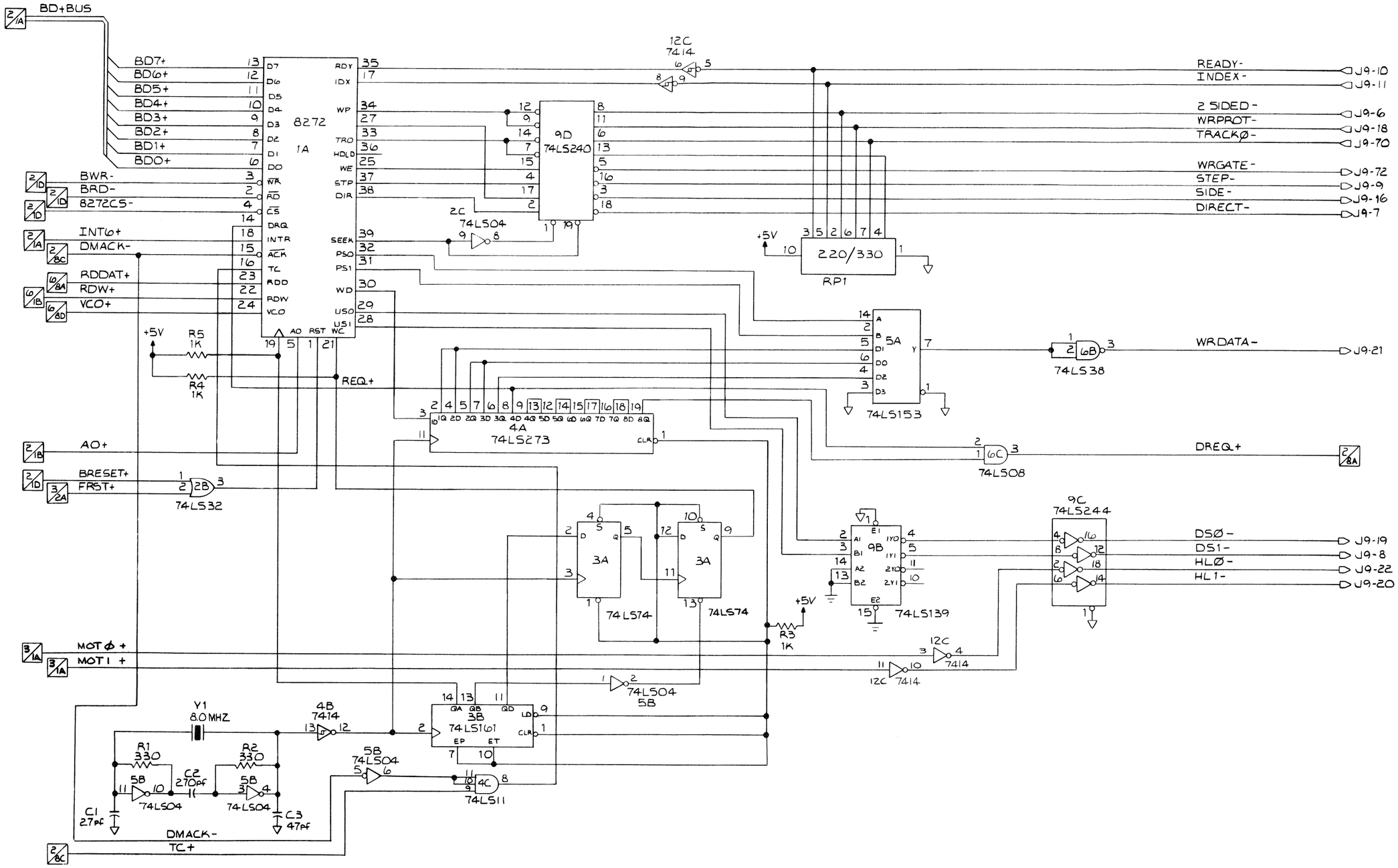


Figure 3-25. FDC Board Schematic. (Page 5 of 6)

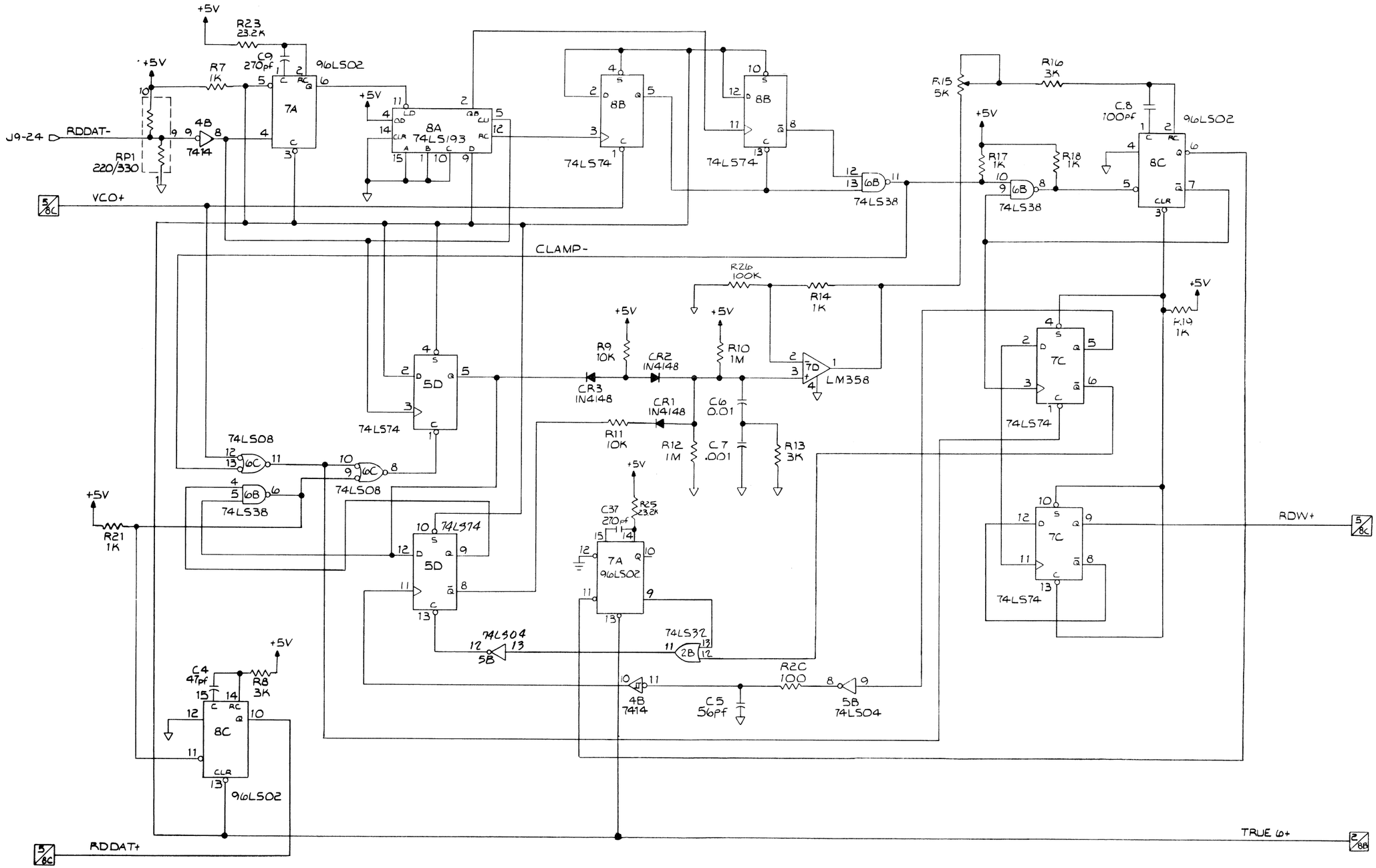


Figure 3-25. FDC Board Schematic. (Page 6 of 6)

Input/Output Port Selection

The CPU can read and write to five input/output devices and the Extended Control Register, or write to the Extended Address Register, all on the FDC Board. The register or input/output device is selected by the EXP1DC- or EXP2DC line. When input/output Port 80h or 81h is selected, EXP1DC- from pin 5 of receiver 3D is sent to the CS- (Chip Select) input of the 8272 floppy disk controller at 1A as 8272CS-.

EXP2DC-, at pin 7 of 3D, is sent to decoder 5C along with the LA2+, LA3+, and LA4+ lines from receiver 4D. The low (active) outputs of 5C are decoded as follows:

Address	Active Signal	Origin	Device Selected
A0h-A1h	8259CS-	5C-15	8259A interrupt controller
A4h	ECRCS-	5C-14	Extended Control and Status Register
A8h-ABh	8274CS-	5C-13	7201 MPSC
ACh-AFh	8253CS-	5C-12	8253 counter/timer
B0h	LPTCS-	5C-11	Printer interface
B4h	EARCS-	5C-10	Extended Address Register

The Extended Control/Status Register (ECR) at Port A4h provides several communications controls for the RS-232-C communications ports discussed below in "RS-232-C Communications Interface" and "RS-232-C Communications Logic" below. In addition, the ECR Register provides two lines, one for the floppy disk drive motor control and one for the floppy disk drive controller reset.

The Extended Address Register (EAR) at Port B4h is loaded prior to a disk read or write operation through the BD0+-BD3+ (Buffered Data) lines; it contains the upper four bits of the DMA address LA10+-LA13+. The EAR allows the data transfer to be in any 64-kilobyte block of RAM in the workstation, since the 8257 DMA controller can only address 16 bits. The output of the EAR is enabled by ADRDIS- (Address Disable) from buffer 4D. ADRDIS- is sent to the CPU Board to disable

the upper four bits of the address from the 8257 when a floppy disk drive read or write operation is in progress.

All other input/output ports, such as those for the 8272, 7201, and 8253 are discussed below under their respective headings.

With respect to read or write operations between the FDC Board and the CPU Board, the default is a write operation. The default is determined by the pin 1 direction input of transceiver 2D, which under normal circumstances, is high. The direction of 2D is changed by DRIVED- (Drive Data Bus) when an input/output port, or the FDC bootstrap ROM is selected, and the RD- strobe from the CPU Board is active.

The EXP1DC- and EXP2DC- decode lines are ORed at pins 1 and 2 of gate 4C, respectively. The third input at pin 13 of 4C is the ORed result of both ROMSUP- (ROM Suppress) at pin 5 of 4C and EXTACK- at pins 3 and 4 of 4C. ROMSUP- is an an output from pin 2 of inverter 12C on page 4; EXTACK- is the Expansion DMA acknowledge signal from the CPU Board's DMA controller. When any device or function on the FDC Board is selected, pin 12 of 4C goes low, which is sent to the pin 12 input of AND gate 1B. The pin 11 input of 1B is RD- from the CPU Board through receiver 3D. When RD- is low, and any FDC Board function is selected, the direction of data flow is set to be from the FDC Board to the CPU Board. The direction is set by a low from pin 13 of 1B through pin 4 of NOR gate 1B as DRIVED-.

Also, if line address bits LA12+ and LA13+ are high, ROMSUP- goes low, which enables bootstrap ROM 7B while simultaneously disabling the bootstrap ROM on the CPU Board.

Interrupt Control

As described above in the "Architecture" section under "Interrupt Control", the 8259A programmable interrupt controller accepts interrupt requests from five sources:

Interrupt Source	Origin	Interrupt Input 8259A 1D	Level
CPU Board	J9-13	INT1+ pin 19	1
Unused	---	---	2
7201	11A-28	INT3+ pin 21	3
Printer Interface	13C-6	INT4+ pin 22	4
8253	6A-10	INT5+ pin 23	5
8272	1A-18	INT6+ pin 24	6
Unused	---	---	7

When a device connected to the 8259A asserts its interrupt line, the 8259A takes INT+ (Interrupt) high at pin 17 of 1D. INT+ is sent to the CPU Board as INTR+ at pin 2 of transmitter 13D. The CPU responds to the interrupt request by sending two INTA- pulses through pin 3 of receiver 3D. The first INTA- pulse allows the 8259A to resolve the priority of the INT1+ through INT6+ (Interrupt Priority 1-6) lines. During the second INTA- pulse, the 8259A sends the appropriate interrupt vector to the CPU. Flip-flop 13C and gates at 1B ensure that DRIVED- is low only during the second INTA- pulse and only if the vector is from the 8259A.

The INTA pulses are sent to pin 26 of the 8259A, pin 11 of flip-flop 13C, and pin 8 of AND gate 1B. During the rising edge of the first INTA- pulse, the pin 9 FRZ+ (Freeze) output of 13C goes high. A low is sent from the pin 8 Q- output of 13C through pins 4 and 6 of OR gate 2B to pin 9 of gate 1B. Pin 8 of 1B is low during the next INTA- pulse from the CPU. The resulting high at pin 10 of 1B is sent to pin 6 of 1B and then output as a low DRIVED- at pin 4 of 1B to transceiver 2D. The 8259A next sends an 8-bit interrupt vector to the CPU on the BD0+-BD7+ data lines.

If the CPU Board (INT1-) is the interrupt requester, the interrupt vector comes from the CPU Board, not from the 8259A. The 8259A uses the CAS0+ (Cascade) line to send a high through pin 6 of gate 2B as 7201VECT+ (7201 Interrupt

Vector). 7201VECT+ is inverted at pin 10 of 2C and sent through pins 15 and 5 of transmitter 13D to the CPU Board as IPI- (Interrupt Priority In) to signal the 7201 when it should drive an interrupt vector to the CPU. 7201VECT+ also disables DRIVED- to prevent the 8259A from driving an interrupt vector onto the BD0+-BD7+ data lines.

Clock Divider

The clock divider is at counter 3C, which takes the 9.8MHZ+ (9.8-MHz clock) signal from the CPU Board as its input and divides it down to 2.46 MHz at pin 13, and down to 1.23 MHz at pin 12. The 2.46MHZ+ (2.46-MHz clock) is sent to the 7201 at 11A. The 1.23MHZ+ (1.23-MHz clock) is sent to both the printer interface strobe generator at 1C and the 8253 at 6A.

8253 Counter/Timer Logic

As shown on page 4 of Figure 3-25 above, the Intel 8253 counter/timer circuit at 6A provides three fully programmable 16-bit counter/timers. Two of the counters are used for generating the internal clocks for RS-232-C Ports A and B and a third counter is used to generate general purpose interrupts for software. Figure 3-26 below shows the functional blocks of the 8253 logic on the FDC Board.

8253 Programming

The input clock frequency sent to each counter channel is 1.23 MHz. The assignment of each counter channel in the 8253 on the FDC Board is:

Counter	Output	Assignment
0	6A-10	Timer Interrupts (INT5+)
1	6A-13	RS-232-C Port B (C1CLK+)
2	6A-17	RS-232-C Port A (C2CLK+)

The 8253 is programmed by the CPU through the eight buffered data bus lines BD0+-BD7+. During input/output read or write cycles to the 8253, 8253CS- (8253 Chip Select) from pin 12 of 5C

selects the timer. The data needed to program the channels are actually transferred when either BRD- (Buffered Read) at pin 22 of 6A or BWR- (Buffered Write) at pin 23 goes low. Address lines A0+ and A1+ are used to select the particular register within the 8253. Detailed programming information for the 8253 is described in the "Architecture" section under "8253 Counter/Timer."

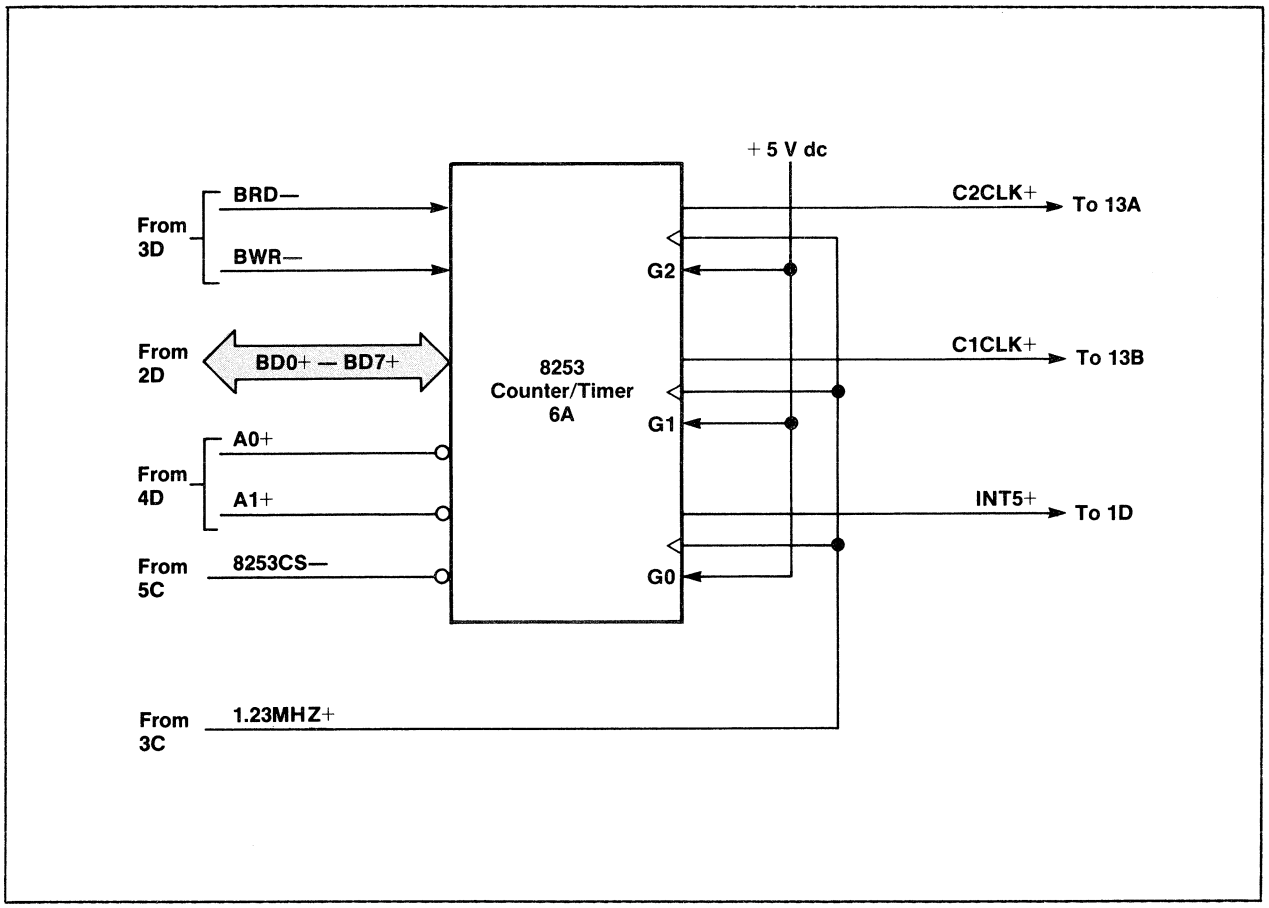


Figure 3-26. 8253 Counter/Timer Logic.

RS-232-C Communications Logic

RS-232-C communications with external devices are based on an NEC 7201 (Intel 8274) MPSC. Since the 7201 does not support secondary transmit and receive lines, the RS-232-C communications channels use the Extended Control Register at Port A4h for this purpose. The Extended Control

Register also contains two bits for selection of internal or external transmit and receive clocks for each of the communications channels. The status of several other lines not supported by the 7201 can be read in the Extended Communications Status Register, also at Port A4h.

Figure 3-27 below shows the functional blocks of the RS-232-C communications logic. Also see the FDC Board schematic, Figure 3-25 above, during the following discussion.

7201 and Extended Control Register Programming

As shown on page 3 of Figure 3-25, the 7201 is programmed through the eight buffered data bus lines, BD0+-BD7+ when 8274CS- (8274 Chip Select) is low at 11A pin 23, and BRD- or BWR- is low at 11A pins 22 or 21, respectively. A0+ and A1+ (Address) at 11A pins 24 and 25 are used to select the individual registers within the 7201. Both of the RS-232-C communications channels operate under interrupt control. Interrupt handling and the use of the 7201's INT3+ line is described under "Bus Interface and Interrupt Control Logic" above.

The Extended Control Register at 9A is enabled when ECRCS- and BWR- are both low at pins 2 and 1, respectively, of gate 12B. The low pin 3 output of 12B is sent to the pin 11 input of 9A to allow the CPU to write 8 bits of control data on the BD0+-BD7+ buffered data lines. The Extended Communications Status Register at 10A is enabled by a low ECRCS- and BRD- at pins 4 and 5, respectively, of 12B. A low output on pin 6 of 12B enables 10A at pins 1 and 19. The CPU can then read the 8 bits of status information on the BD0+-BD7+ buffered data lines.

RS-232-C Communications Signals

Each RS-232-C communications channel on the AWS-220, -230, and -240 has twelve data and control lines associated with it. All of the lines sent to the DCE (Data Communications Equipment) are converted from standard TTL levels used on the FDC Board to the RS-232-C standard levels at the interface. Lines from the DCE to the communications channels are converted from RS-232-C standard levels to TTL for use by the 7201

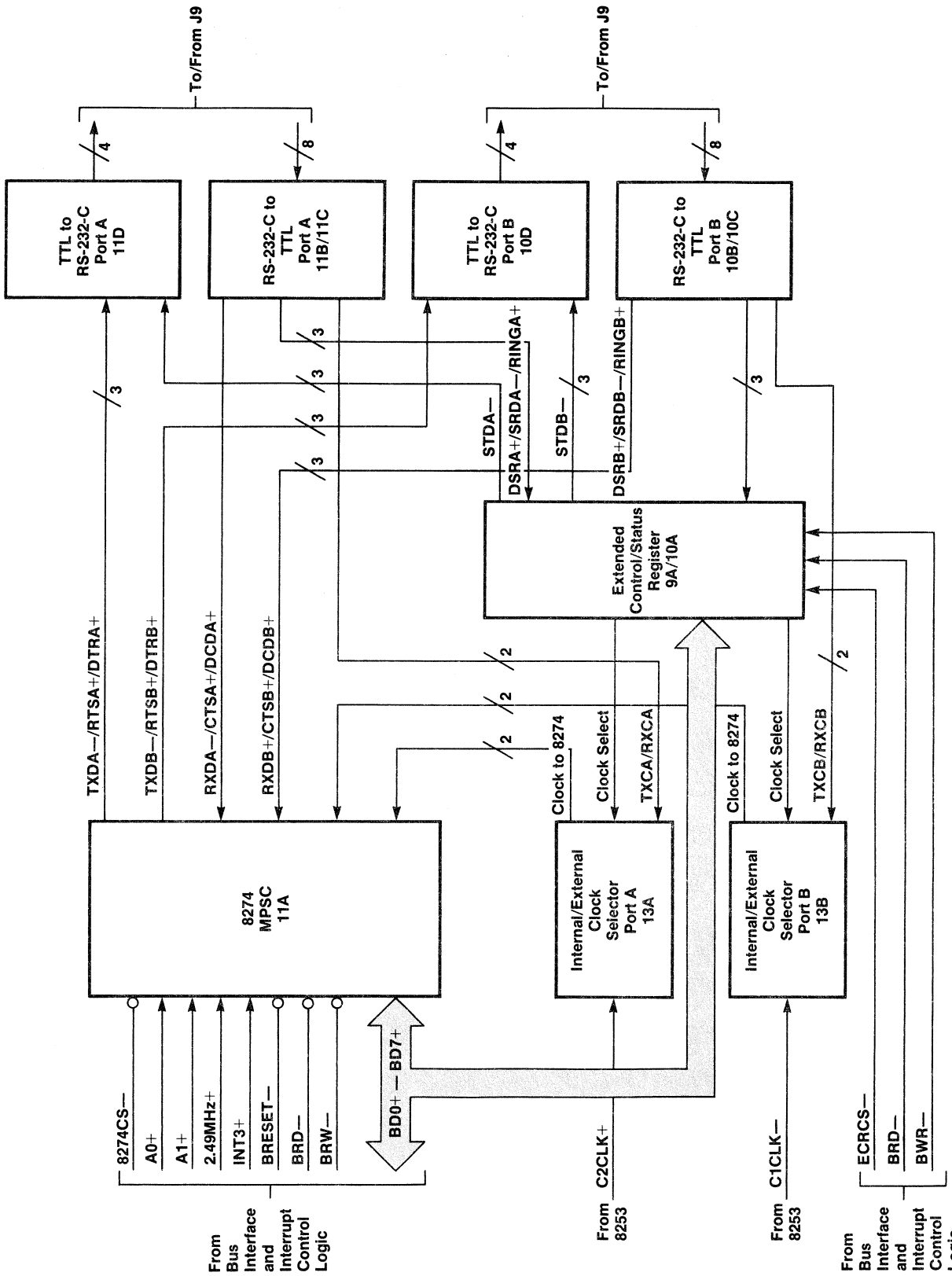


Figure 3-27. RS-232-C Communications Logic.

and the Extended Control and Status Register. The level converters at 10B, 10C, and 10D control communications Channel A; level converters 11B, 11C, and 11D control Channel B. The assignment for each line to and from the channels is:

Signal Name	Mnemonic	Channel	Converter
Transmit Data	TXDA-	A	11D
	TXDB-	B	10D
Secondary Transmit Data	STDA-	A	11D
	STDB-	B	10D
Request to Send	RTSA+	A	11D
	RTSB+	B	10D
Data Terminal Ready	DTRA+	A	11D
	DTRB+	B	10D
Receive Data	RXDA-	A	11C
	RXDB-	B	10B
Secondary Receive Data	SRDA+	A	11C
	SRDB+	B	10C
Clear to Send	CTSA+	A	11C
	CTSB+	B	10B
Data Set Ready	DSRA+	A	11C
	DSRB+	B	10C
Carrier Detect	DCDA+	A	11B
	DCDB+	B	10B
Ring Indicator	RINGA+	A	11B
	RINGB+	B	10B
External Transmit Clock	TXCA+	A	11B
	TXCB+	B	10C
External Receive Clock	RXCA+	A	11B
	RXCB+	B	10C

Transmit and receive clocks for both communications channels can come either from the on-board 8253 counter/timer at 6A (as shown on page 4 of Figure 3-25) or from the DCE through the TXCA+, TXCB+, RXCA+, and RXCB+ lines. Wired as multiplexers, drivers 13A and 13B perform the clock selection for RS-232-C communications Channels A and B, respectively. Selection pins 1 and 19 of 13A are controlled from pin 16 (bit D5)

of Extended Control Register 9A. When pin 16 of 9A is high, the TXCA+ and RXCA+ clock lines at pins 11 and 13, of 13A are sent to pins 9 and 7 of 13A and then to pins 36 and 35 of 7201 at 11A. When pin 16 of 9A is low (the default condition), the C2CLK+ (8253 Counter 2 Clock) output of the 8253 at pins 6 and 8, of 13A is sent to pins 14 and 12 of 13A and then to pins 35 and 36 of the 7201 at 11A.

The driver/multiplexer at 13B for communications Channel B operates in the same manner as 13A does for communications Channel A, except that bit D4 at pin 12 of 9A controls the selection, and TXCB+ and RXCB+ come from pins 3 and 6 of 10C. The C1CLK+ (Counter 1 Clock) output of the 8253 at 6A is used, and the destination pins on the 7201 are pins 7 and 4.

Printer Interface Logic

Figure 3-28 below shows the functional blocks of the Centronics-compatible printer interface. Also see page 4 of the FDC Board schematic, Figure 3-25 above, during the following discussion.

The CPU sends 8-bit characters to the printer interface on the BD0+-BD7+ buffered data lines. Data latch 12D is selected when both LPTCS- (Line Printer Chip Select) and BWR- go low at pins 12 and 13, of gate 12B. The low pin 11 output of 12B is sent to pin 11 of 12D to latch the character. The pin 1 output enable of 12D is always low, so the data is then immediately sent to the printer on the LPT0+-LPT7+ (Line Printer Data) printer output lines.

The low pin 11 of gate 12B also resets counter 1C, which generates a STROBE- (Character Strobe) pulse informing the printer that data is available on the LPT0+-LPT7+ printer output lines. Counter 1C is wired in a manner, such that, after pin 11 of 12B goes low to reset it, one microsecond lapses to allow the STROBE- pulse to go high at pin 13 of 1C for one microsecond. The pulse is inverted at pin 4 of 2C, buffered at pin 9 of 13D, sent off of the FDC Board as STROBE- through pin 64 of J9, and finally, sent to the Printer jack J3 on the back panel. After STROBE- goes high again, counter 1C waits for the next reset pulse from pin 11 of 12B.

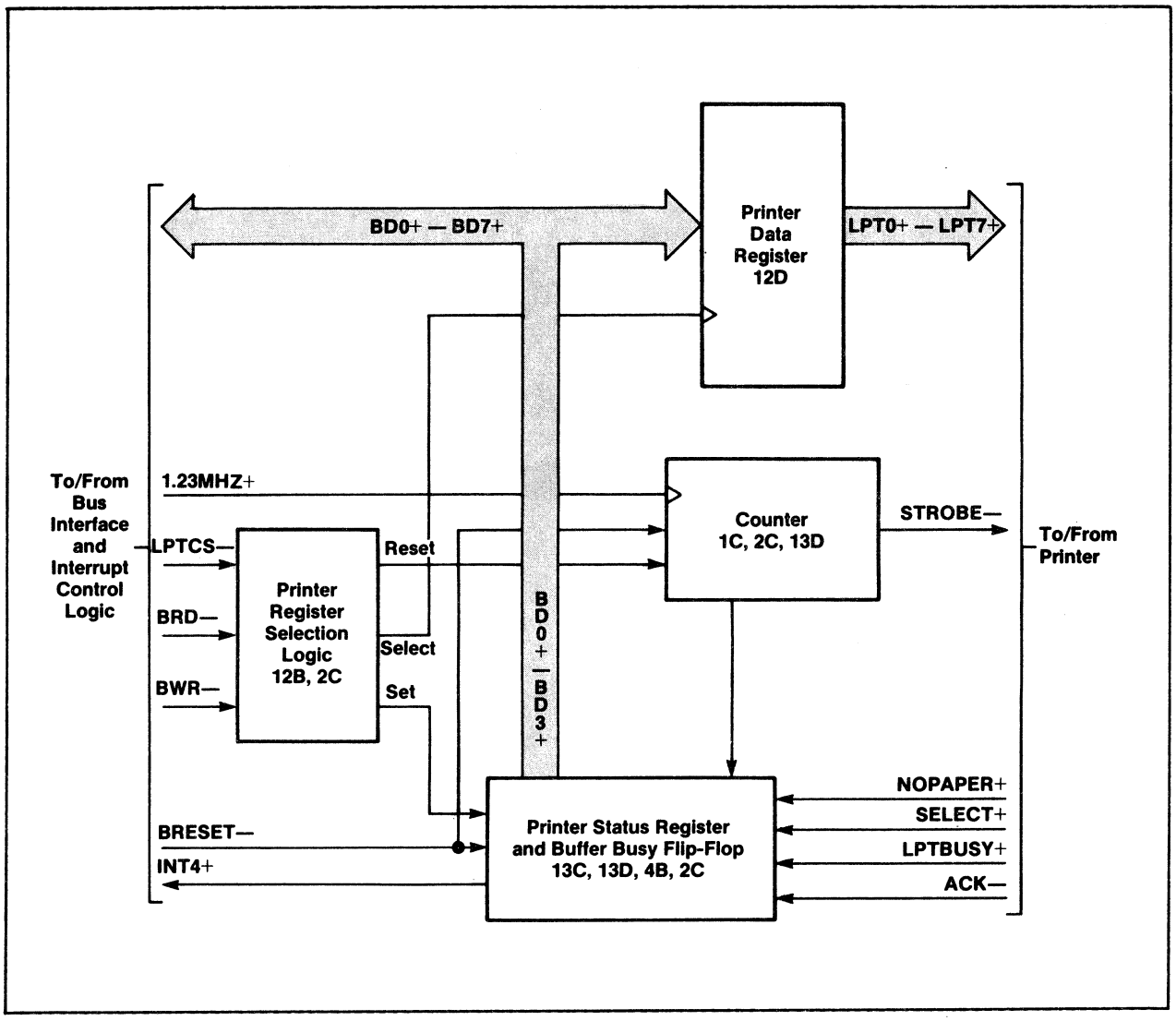


Figure 3-28. Printer Interface Logic.

Pin 11 of 12B also sets the buffer busy flip-flop at 13C. When the printer receives a character on the LPT0+-LPT7+ printer output lines, it responds by pulling the ACK- (Acknowledge) handshake line low. ACK- is inverted at pin 6 of 4B, inverted again at pin 2 of 2C, and sent to the pin 3 clock input of flip-flop 13C. The pin 5 BUFBUSY+ (Buffer Busy) output of 13C is high when the character is sent. When ACK- is pulsed, pin 5 of 13C goes low (grounded pin 2 D input), indicating that the CPU can send another character. The pin 5 output of 13C, BUFBUSY+, is sent to the Printer Status Register at pin 4 of buffer 13D.

When pin 5 of 13C is low, the pin 6 Q- output of 13C, INT4+, is high. INT4+ is sent to the pin 22 input of the 8259A interrupt controller. The software polls the BUFBUSY+ bit of the Printer Status Register at Port B0h to determine when the printer can accept another character. If the character is acknowledged quickly (BUFBUSY+ stays high for only a short time), the software assumes that the printer has a buffer and sends another character immediately. If the software polls the Printer Status Register and finds that BUFBUSY+ is staying high for a longer time between characters, the software enables the INT4+ mask bit in the 8259A. This allows the pin 6 Q- output of flip-flop 13C to interrupt the CPU when it requires another character or when the printer buffer is empty.

The Printer Status Register contains four bits of status information: LPTBUSY+, SELECT+, BUFBUSY+, and NOPAPER+, which correspond to bits BD0+-BD3+ in buffer 13D. The CPU reads the Printer Status Register when LPTCS- and BRD- are both low at pins 10 and 9 of gate 12B. The low pin 8 output of 12B enables buffer 13D.

AWS-220 and -230 Floppy Disk Controller Logic

The floppy disk controller on the FDC Board uses an Intel 8272 floppy disk controller to control one or two 96-track-per-in, single- or double-sided, 5 1/4-in floppy disk drives. The floppy disk controller operates only in a double-density (MFM) mode; using DMA Channel 0 on the CPU Board to perform read and write operations. The major functional groups of circuitry in the floppy disk controller are:

- the 8272 floppy disk controller,
- the controller's interface circuitry to the CPU Board and floppy disk drives,
- the clock and write precompensation circuits, and
- the data separator circuits.

Figure 3-29 shows the functional blocks of the floppy disk controller. Also see pages 2, 5, and 6 of the FDC Board schematic, Figure 3-25, during the following discussion.

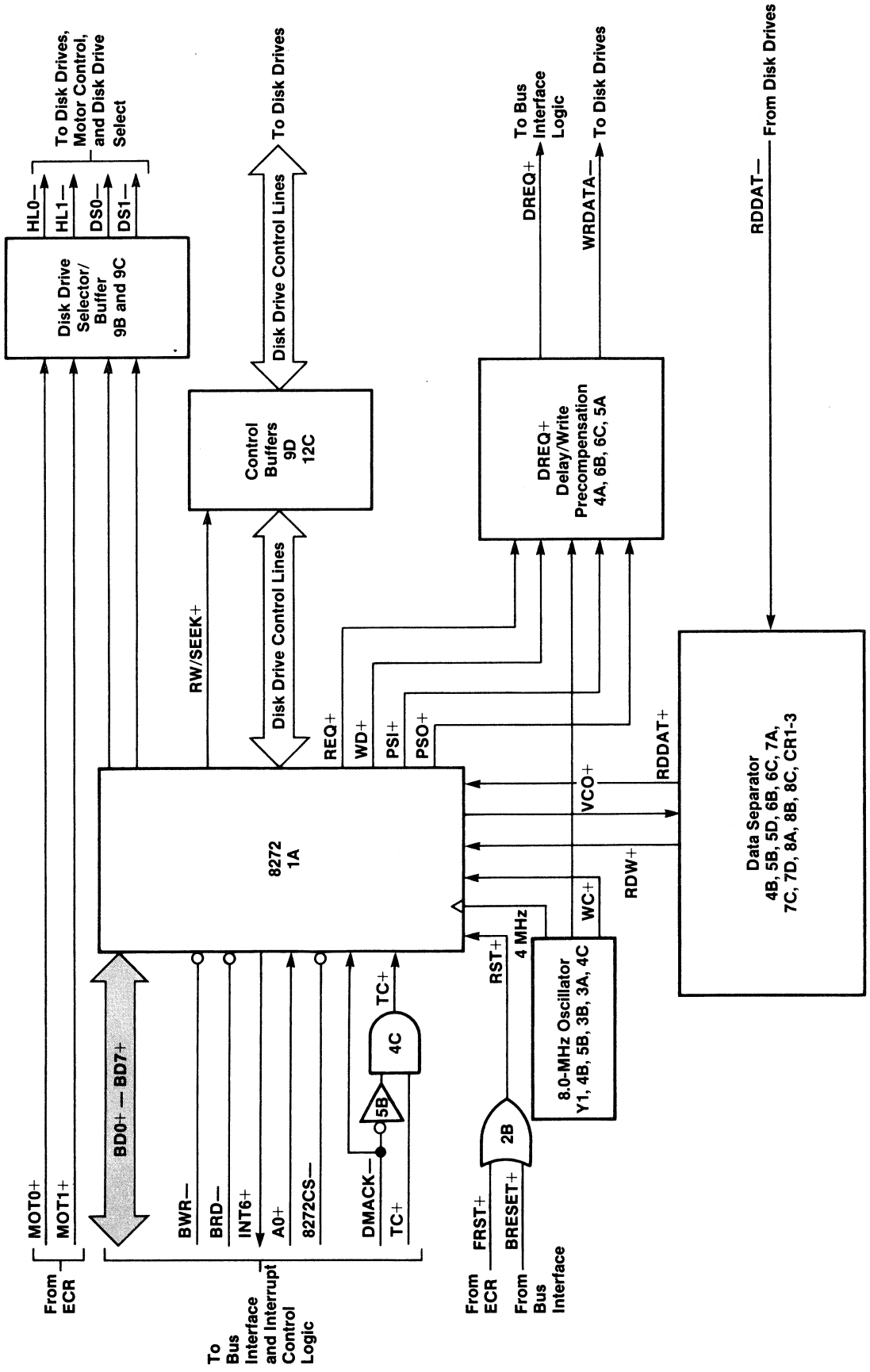


Figure 3-29. AWS-220 and -230 Floppy Disk Controller Logic.

8272 Programming

The CPU, depending on the command to be executed, writes from one to nine bytes into the 8272. Also, during the command phase of any operation (and before another command can be executed), the CPU must read one or more status registers.

As shown on page 5 of Figure 3-25, the 8272 is programmed when 8272CS- and BWR- or BRD- are low, through the BD0+-BD7+ buffered data lines to the 1A input pins 4 and 3 or 2, respectively. For command/status and status information, the A0+ address line is used to select between two input/output ports at 80h and 81h. For more complete programming information concerning the 8272, see "AWS-220 and -230 Floppy Disk Controller" in the "Architecture" section.

DMA and CPU Interface

To get an acceptable data transfer rate, read or write commands issued to the 8272 require that DMA Channel 0 be used to transfer data to or from the RAM array on the CPU Board.

Once the 8272 and DMA Channel 0 are programmed, the 8272 requests a DMA cycle by setting its pin 14 DRQ+ (Data Request) output low. This line is sent, as REQ+ (Request), to the pin 9 (4D) input of shift register 4A, where it is delayed by five clock cycles (625 ns). The delayed DMA request line exits 4A at its pin 19 Q8 output. It is gated with the undelayed REQ+ at pins 1 and 2 of gate 6C. The pin 3 output of 6C, DREQ+ (DMA Request), is sent to pin 17 of buffer 13D (shown on page 2 of Figure 3-25) and then to the CPU Board as EXTRQ- (External DMA Request).

The 8257 responds to EXTRQ- by asserting its DMACK- (DMA Acknowledge) line to the 8272 (shown on page 5). DMACK- from pin 18 of buffer 4D is sent to the ACK- pin 15 of the 8272. When the 8272 receives a DMA acknowledge, the read or write operation is in progress; the 8272 can then either place data on (read operation), or accept data from (write operation), the BD0+-BD7+ data lines.

DMACK- is also gated at pins 10 and 1 of 4C with TC+ at pin 9, at gate 4C. TC+ is sent by the 8257 during the final byte of the programmed byte

count to inform the 8272 that it must stop reading or writing on the current sector of the floppy disk. The high pin 8 output of 4C is sent to the pin 16 TC+ input of the 8272.

With certain operations, the 8272 must interrupt the CPU when it finishes. The INT6+ line from the pin 18 INTR+ output of the 8272 is sent to the pin 24 input of 8259A 1D. As described under "Bus Interface and Interrupt Control Logic" above, the 8259A interrupts the CPU on behalf of the 8272 and sends an interrupt vector during the CPU interrupt acknowledge cycle. The CPU then interrogates the 8272 to find the reason for the interrupt.

Floppy Disk Drive Controller Interface

As shown on page 5 of Figure 3-25, the READY- and INDEX- lines from the floppy disk drives to the 8272 are buffered by two inverters at pins 6 and 8 of 12C. READY- indicates that the selected drive is ready to send or receive data. INDEX- informs the 8272 that the floppy disk is at the beginning sector of a track.

Several of the control signals to and from the 8272 have dual meanings, depending on the state of the 8272's pin 39 RW-/SEEK+ (Read/Write or Seek) line. The tri-state octal buffer at 9D is configured as a driver/multiplexer to accomodate these control lines.

When the pin 39 RW-/SEEK+ output the 8272 is 1 (seek mode is active), pin 1 of 9D is low and pin 19 of 9D is high. The table below shows which buffers in 9D are enabled for the following control signals:

8272 Pin Number and Name	9D Buffer Input Pin	From/ To	J9 Pin Number and Name
38 DIR+	2	to	7 DIRECT-
37 STP+	4	to	9 STEP-
33 TR0+	6	from	70 TRACK0-
34 WP+	8	from	16 2SIDED-

When pin 39 of the 8272 is 0 (read/write mode active), pin 1 of 9D is high and pin 19 of 9D is

low. The following control signals are active through buffer 9D:

8272 Pin Number and Name	9D Buffer Input Pin	From/ To	J9 Pin Number and Name
27 HDSEL+	17	to	6 SIDE-
25 WE+	15	to	72 WRGATE-
33 TR0+	13	to	None (tied to +5 V dc)
34 WP+	8	from	9 WRPROT-

The floppy disk drive is selected by the pin 29 US0+ and pin 28 US1+ (Unit Select) lines of the 8272 through decoder 9B. US0 and US1 are both 0 when drive 0 is selected (pin 4 of 9B is low); US0 is 1 and US1 is 0 when drive 1 is selected (pin 5 of 9B is low). The outputs of 9B are buffered at pin 16 and 12 of 9C and sent to the floppy disk drives as DS0- and DS1- (Drive Select) on the pins 19 and 8, respectively, of J9.

Two other control signals for drive motor control come from the Extended Control Register at Port A4h. MOT0+ (Drive Motor), from pin 5 of latch 9A (page 3), is inverted at pin 4 of 12C (on page 5), buffered at pin 18 of 9C, and sent to the Drive 0 motor as HL0- (Head Load 0) at J9-22. MOT1+ comes from pin 6 of latch 9A, is inverted at pin 10 of 12C, buffered at pin 14 of 9C, and sent to the Drive 1 motor on as HL1- (Head Load 1) at J9-20.

8-MHz Clock and Write Precompensation Circuitry

An on-board 8-MHz oscillator is used to provide the basic timing for the 8272's operation and also generates a write clock for the floppy disk drives. On page 5 of Figure 3-25, the oscillator is shown to be composed of crystal Y1, three inverters at 5B and 5C, resistors R1 and R2, and three capacitors: C1, C2, and C3. The 8-MHz output of the clock at pin 12 of Schmitt-trigger inverter 4B is sent to the pin 2 clock input of counter 3B, the pin 3 clock input of flip-flop 3A, and pin 11 of shift register 4A.

Counter 3B provides a 4-MHz clock to the pin 19 input of the 8272 from its pin 14 QA output. The

pin 13 QB output of 3B is used to generate a 500-kHz write clock for the 8272 through the two flip-flops at 3A. The pin 13 QB output of 3B is inverted at pin 2 of 5B and sent to the pin 13 clear input of flip-flop 3A to limit the pulse width of the write clock to 250 ns. The write clock pulse is sent to the pin 21 WC (Write Clock) input of the 8272.

When a write operation to a floppy disk drive occurs, write data from pin 30 of the 8272 is sent to the pin 3 1D input of shift register 4A. The pin 2 1Q, pin 5 2Q, and pin 6 3Q outputs of 4A are separated at 125-ns intervals, to allow the write data bit to be sent to the floppy disk drive at the desired time, either early, normal or late. Write precompensation is selected at the pin 32 PS0 and pin 31 PS1 lines of the 8272. PS0 and PS1 are sent to pins 14 and 2, respectively, of multiplexer 5A. 5A selects one of 4A's 1Q, 2Q, or 3Q outputs at its corresponding pin 5, 6, and 4 inputs. The delayed write pulse is sent from pin 7 of 5A to pin 3 of inverting buffer 6B, and then to the floppy disk drives on pin 21 of J9.

Data Separator

During a read operation, the data separator decodes data received from the floppy disk drive. The data separator detects the preamble at the beginning of a data sector and generates a read window signal to determine when an MFM 1 or MFM 0 has been received. The data separator also sends MFM data to the 8272 for additional decoding. The major parts of the data separator are the:

- zero detector,
- phase detector and charge pump,
- read window generator, and
- data bit centering circuitry.

Zero Detector. Read data from the floppy disk drive arrives at the data separator input at pin 24 of J9, is inverted at pin 8 of 4B, and is then applied to pin 4 of one-shot 7A. 7A, together

with the counter at 8A and two flip-flops at 8B, forms a zero detection circuit.

Before the data separator's phase-locked loop is exposed to a stream of read data from a floppy disk, the zero detector detects the preamble of 12 bytes of consecutive) 0s (in the IBM System 34 floppy disk format). The RC time constant set by R23 and C9 between pins 1 and 2 of 7A is about 1.25-bit cell times, or 625 ns. That is, when 7A is triggered by the incoming data bits, it is set by the time constant at R23 and C9 to time out in a longer period of time than the next data bit cell where an MFM 0 is written. However, the time-out period is short enough for an MFM 1, written in the middle of the data bit cell, to be detected.

One-shot 7A is continually retriggered by a set of consecutive MFM 0s; since 7A's RC time constant is too long to time out, its pin 6 Q output stays high. Pin 6 of 7A is sent to the pin 11 LD (Load) input of counter 8A. When pin 6 of 7A goes low, meaning that an MFM 1 was detected after the MFM 0s, the counter is loaded to a binary 8. The counter load occurs because pin 9 of 8A is tied to +5 V dc and pin 6 of 7A goes low. Since the load also occurs prior to the detection of MFM 0s, 8A is counting the number of consecutive MFM 0s received at pin 8 of inverter 4B. When 8 MFM 0's are detected, pin 12 of 8A, RC (Ripple Count), goes high at the pin 3 clock input of flip-flop 8B. Since the pin 2 D input of 8B is high, the pin 5 Q output goes high to pin 13 of NAND gate 6B. Pin 5 of 8B also clears the other half of 8B at pin 13, which causes its Q- output at pin 8 to go high at pin 12 of 6B. The low pin 11 output of 6B is CLAMP-, which turns off the VFO (Variable Frequency Oscillator) clock at pin 13 of gate 6C. When four more MFM 0s are counted at pin 12 of counter 8A, its pin 2 QB output goes high to set flip-flop 8B at its pin 12 D input. This removes the high from pin 12 of 6B and thus causes CLAMP- to go high.

The VFO is a one-shot at 8C, which continually retriggers itself from its pin 7 Q- output to pin 9 of gate 6B. When CLAMP- goes high, pin 10 of 6B also goes high, which sends a low to 8C's pin 5 input, triggering 8C again. When 8C times out, pin 7 goes high again, repeating the oscillation.

Within several nanoseconds of gate delay between the time of the leading edge of the data pulse and the time that CLAMP- goes high, the VFO starts up in phase with the incoming data stream. Since it was the leading edge of the data pulse that clocked counter 8A's QB output and thus led to the removal of the active CLAMP- signal, the VFO clock always starts up in phase with the data. Since the phase-locked loop does not have to perform phase acquisition, the loop is not subject to the noise instablility problems that are inherent in more sensitive phase-locked loops.

Phase Detector and Charge Pump. The two flip-flops at 5D form the phase detector, which determines the amount of error between the frequency of the VFO and the frequency of the incoming data from the floppy disk drive. The phase detector flip-flops control a charge pump that directly controls the frequency of the VFO. The phase detector is turned on by VCO+ from pin 24 of the 8272.

When the 8272 is not performing a read or write operation, VCO+ (Voltage-Controlled Oscillator) is low, which causes flip-flop 8B to be cleared at pin 1. This, in turn, causes the pin 11 output of gate 6B (CLAMP-) to be high. CLAMP- at pin 13 of 6C causes one of the phase detector flip-flops at 5D to be cleared at its pin 1 (through pin 8 of gate 6C). The low pin 5 Q output is sent to the pin 12 D input of the other phase detector flip-flop at 5D, which results in this flip-flop being high at its pin 8 Q- output. Pin 5 of 5D low causes diode CR3 to be forward-biased. Because of the +5-V dc pullup resistor at R9, the junction between diodes CR2 and CR3 is low. The high output at pin 8 of flip-flop 5D causes CR1 to be reverse-biased, in the same manner as CR2. Under this low VCO+ condition, CR1 and CR2 act like open circuits: the voltage applied to the pin 3 input of operational amplifier 7D is then about 2.5 V dc. This voltage is determined by the connection of pin 3 of 7D to two 1-megohm resistors, R10 and R12, which are between +5 V dc and ground. Operational amplifier 7D acts as a buffer, supplying a nominal current to the VFO at variable resistor R15. R15 is adjusted to make the VFO oscillate at a frequency of 1 MHz.

When VCO+ is high, meaning that the 8272 is reading data from the floppy disk, both the zero and phase detectors are enabled. The CLAMP- signal is generated as described above, temporarily disabling the phase detector. At this time, the VFO at 8C is allowed to oscillate at its nominal frequency of about 1 MHz. When CLAMP- goes high again (and since VCO+ already is high), it causes pin 11 of gate 6C to go high (pin 8 output of 6C also goes high since pins 9 and 10 are both already high); and the signal that previously held flip-flop 5D cleared at pin 1 is taken away. The phase detector is now enabled, and the phase-locked loop can now synchronize itself with the incoming stream of data bits.

The data pulse arrives from the floppy disk drive at pin 8 of inverter 4B, clocks pin 3 of flip-flop 5D, and sets it, because of the high at its pin 2 D input. Pin 5 of 5D then represents the data sample and causes diode CR3 to be reverse-biased. Because of the pullup resistor at R9, CR2 is forward-biased and begins to charge pin 3 of operational amplifier 7D. The voltage at pin 1 of 7D increases, causing the frequency of the VFO to increase above its nominal frequency of 1 MHz. The voltage at pin 1 of 7D continues to increase the frequency of the VFO until a transition finally occurs at the pin 7 Q- output of 8C. Pin 7 of 8C is divided by two at pin 5 of flip-flop 7C. The other phase detector flip-flop is then clocked and set on the rising edge of the pin 5 7C output. The low pin 8 Q- output forward-biases CR1, which causes a discharge at pin 3 of 7D, resulting in a decrease in the frequency of the VFO at 8C.

Now that both of the phase detector flip-flops are set, pins 4 and 5 of gate 6B go high. The low pin 6 output of 6B clears the first phase detector flip-flop at its pin 1 clear input, and the second phase detector flip-flop clears on the falling edge of the pin 5 7C output.

Read Window Generator. Pin 5 of 7C creates a relative comparison window, which determines the net increase or decrease in VFO frequency, proportional to the time it takes for the data bit to set pin 5 of 5D. If the next data bit sets pin 5 of 5D early, pin 5 stays high for a longer period of time than a bit appearing at a

normal time, which causes the VFO frequency to increase for a longer period of time. When the transition occurs at pin 5 of flip-flop 7C, pin 9 of 5D is set, which decreases the frequency of the VFO. The amount of time that pin 9 decreases the frequency of the VFO is, with only slight variations, constant. Therefore, a data bit appearing early causes a net increase in the VFO frequency. The reason for the increase in the VFO frequency is to anticipate the next data bit, which may also appear early. If a bit appears late (relative to the comparison window), pin 5 of 5D increases the VFO frequency for a shorter period of time than pin 9 of 5D decreases it, resulting in a net decrease in VFO frequency.

The read window for the 8272 1A is the pin 5 output of 7C, divided by 2 at pin 9 of 7C as RDW+ (Read Window) and sent to pin 22 of 8272 1A.

Data Bit Centering Circuitry. The data bit is centered in the read window before it is presented to the 8272. The data bit is generated at pin 6 of gate 6B when pin 1 of flip-flop 5D is cleared. Pin 6 of 6B triggers pin 11 of flip-flop 8C which, in turn causes Pin 10 of 8C to go high as RDDAT+ (Read Data) for about 140 ns to pin 23 of 8272 1A.

HARD DISK CONTROLLER (HDC) BOARD

Bus Interface and Interrupt Control Logic

Figure 3-30 below shows the functional blocks of the bus interface and interrupt control logic, which:

- o buffers address, data, and control lines between the CPU Board and the HDC Board,
- o selects various input/output devices or the bootstrap ROM on the HDC Board, and allows read and write operations between the CPU or 8257 and the input/output device or ROM,
- o services interrupts from four HDC Board input/output devices as well as interrupts from the CPU Board, and
- o provides 2.46-MHz and 1.23-MHz clocks for use by the HDC Board logic.

Refer to Figure 3-31, the HDC Board schematic, in addition to Figure 3-30, during the following discussion.

Buffers

As shown on page 6 of the HDC Board schematic, Figure 3-31, receivers 2G and 3G receive control lines and the LA0+-LA4+ (Line Address) lines from the CPU Board. The control lines from the CPU Board include RD- (Read) and WR- (Write) strobes, RESET-, a 9.8-MHz clock, EXP1DC- and EXP2DC- (Expansion Decode) input/output device enables, INTA- (Interrupt Acknowledge) and ONBDINT+ (On-Board Interrupt) interrupt controls, and TC+ (Terminal Count) and EXTACK- (External DMA Ackowledge) DMA controls. Transceiver 1G buffers the D0+-D7+ data lines to and from the HDC Board through its pin 1 direction input.

Address lines LA10+-LA13+ are output through the Extended Address Register at 3F for DMA operations (shown on page 7 of Figure 3-31). Transmitter 4G (shown on page 6) sends EXTRQ+ (External DMA Request) for DMA, and IPI- (Interrupt Priority In) and INTR+ (Interrupt Request) interrupt controls to the CPU Board.

Input/Output Port Selection

The CPU can read and write to five input/output devices and the Extended Control Register, or write to the Extended Address Register on the HDC Board. First, the register or input/output device is selected by either the EXP1DC- or EXP2DC lines. EXP1DC-, from pin 5 of receiver 2G, is sent to pin 34 of the 8X320 (shown on page 2 of Figure 3-31).

EXP2DC-, at pin 3 of 2G is sent to decoder 4F along with the LA2+, LA3+, and LA4+ lines from receiver 3G. The low (active) outputs of 4F are decoded as follows:

Address	Active Signal	Origin	Device Selected
A0h-A1h	8259CS-	4F-15	8259A interrupt controller
A4h	ECRCS-	4F-14	Extended Control and Status Register
A8h-ABh	8274CS-	4F-13	7201 MPSC
ACh-AFh	8253CS-	4F-12	8253 counter/timer
B0h	LPTCS-	4F-11	Printer interface
B4h	EARCS-	4F-10	Extended Address Register

The Extended Control and Status Register (ECR) at Port A4h provides several communications controls for the RS-232-C communications ports discussed below in "RS-232-C Communications Logic." In addition, the ECR Register provides one bit for the hard disk controller reset.

The Extended Address Register (EAR) at Port B4h is loaded, prior to a disk read or write operation, through the BD0+-BD3+ (Buffered Data) lines; it contains the upper four bits of the DMA address LA10+-LA13+. The EAR allows the data transfer to be in any 64-kilobyte block of RAM in the AWS-220, -230, or -240 workstation, since the 8257 on the CPU Board has only 16 address bits. The output of the EAR is enabled by ADRDIS- (Address Disable) from buffer 3G. ADRDIS- is sent to the CPU Board to disable the upper four bits of the address from the CPU or 8257 when a hard disk drive read or write operation is in progress.

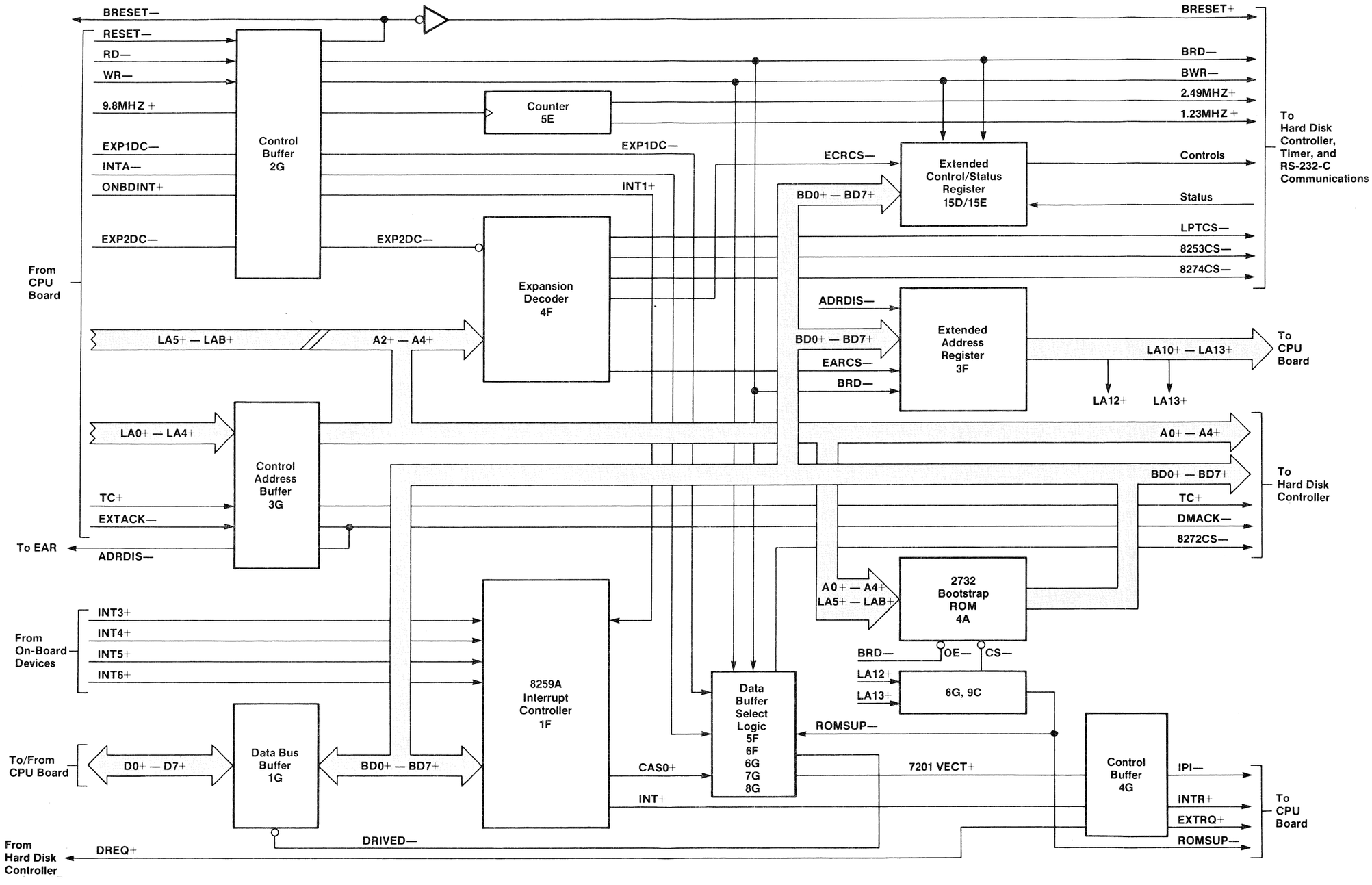


Figure 3-30. Bus Interface and Interrupt Control Logic.

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS, 1/4 W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL OTHER DEVICES ARE STANDARD 14 & 8, 7 & 14, 8 & 16, 10 & 20 DIP & PWR CONNECTIONS.

POWER AND GROUND LOCATOR CHART

REF. DES.	TYPE	GND	+5V	-12V	-12V	-5V
1B	8X300	12	37			
11E	LM339	12	3			
10G, 12G	1488	7		14	1	
12F	LM358			8		4
7B, 8B	93422	8	22			
9F	8X330	1,20	40			

SPARE GATES

TYPE	REF DESIGNATORS	QTY
74S00	7A	1
74LS04	6G	1
74S04	7C	2
74123	17A	1
74S74	15B	1
74S74	13D	1
74S86	13B	1
2GLS32	17C	3
74S08	14B	1
2GLS31	17B	3
74LS11	5F	1

REF. DESIGNATORS

LAST USED	NOT USED
C76	
RP2	
R58	
Q3	
CR6	
L2	
Y3	
VR1	

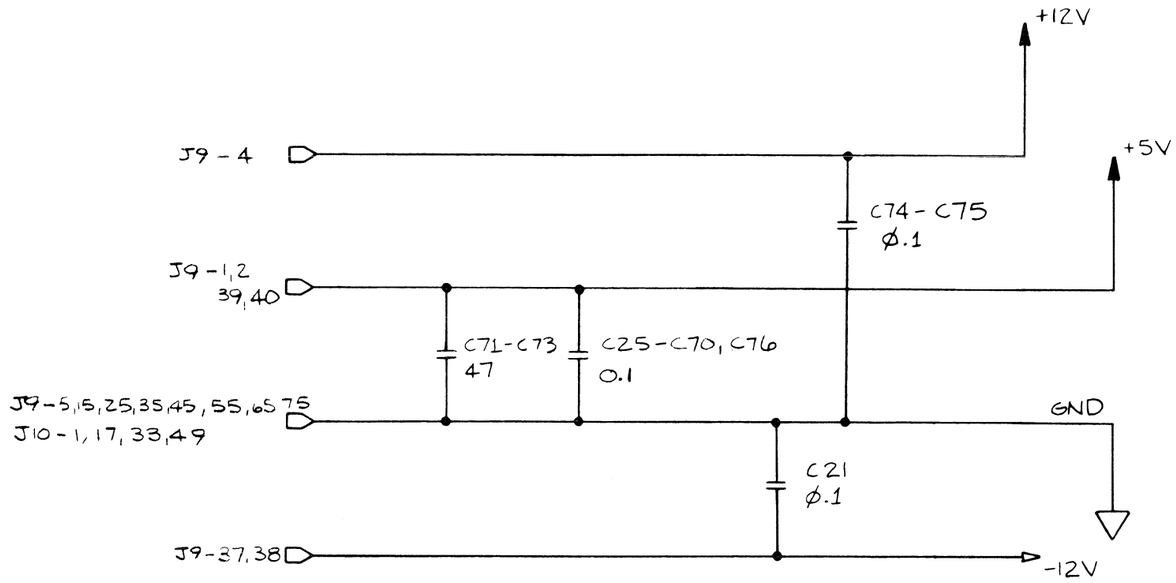


Figure 3-31. HDC Board Schematic. (Page 1 of 8)

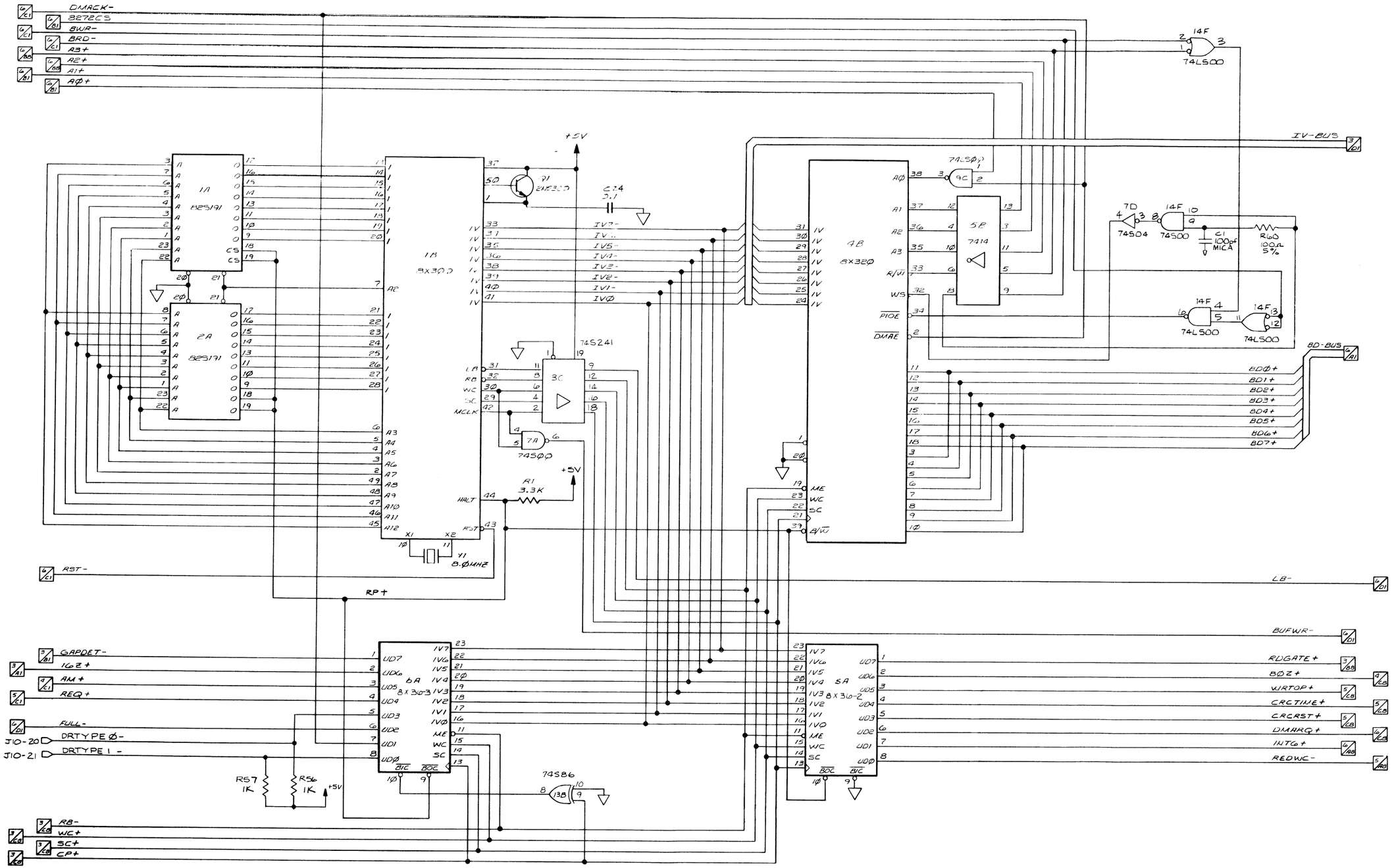


Figure 3-31. HDC Board Schematic. (Page 2 of 8)

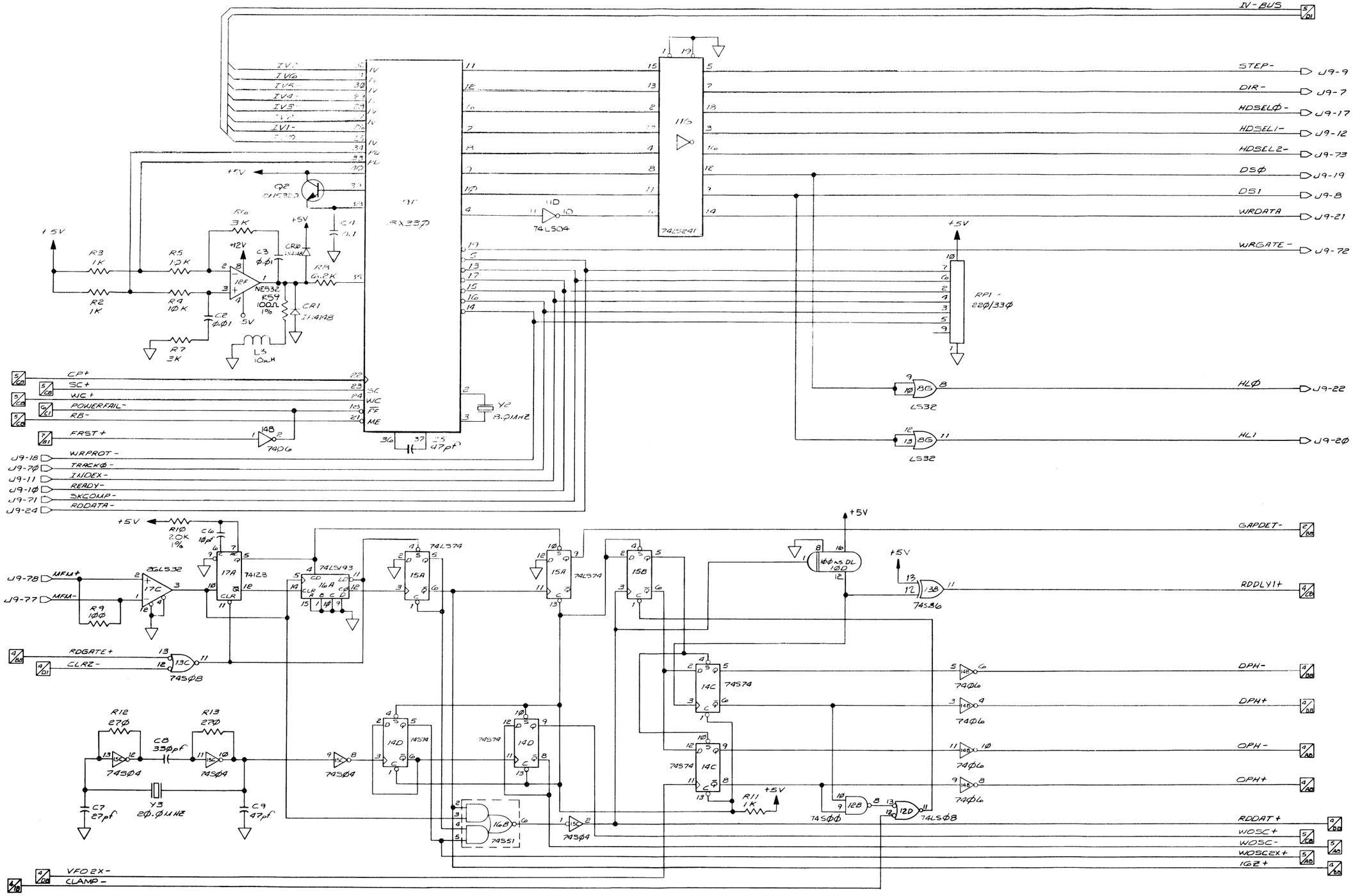


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Figure 3-31. HDC Board Schematic. (Page 3 of 8)

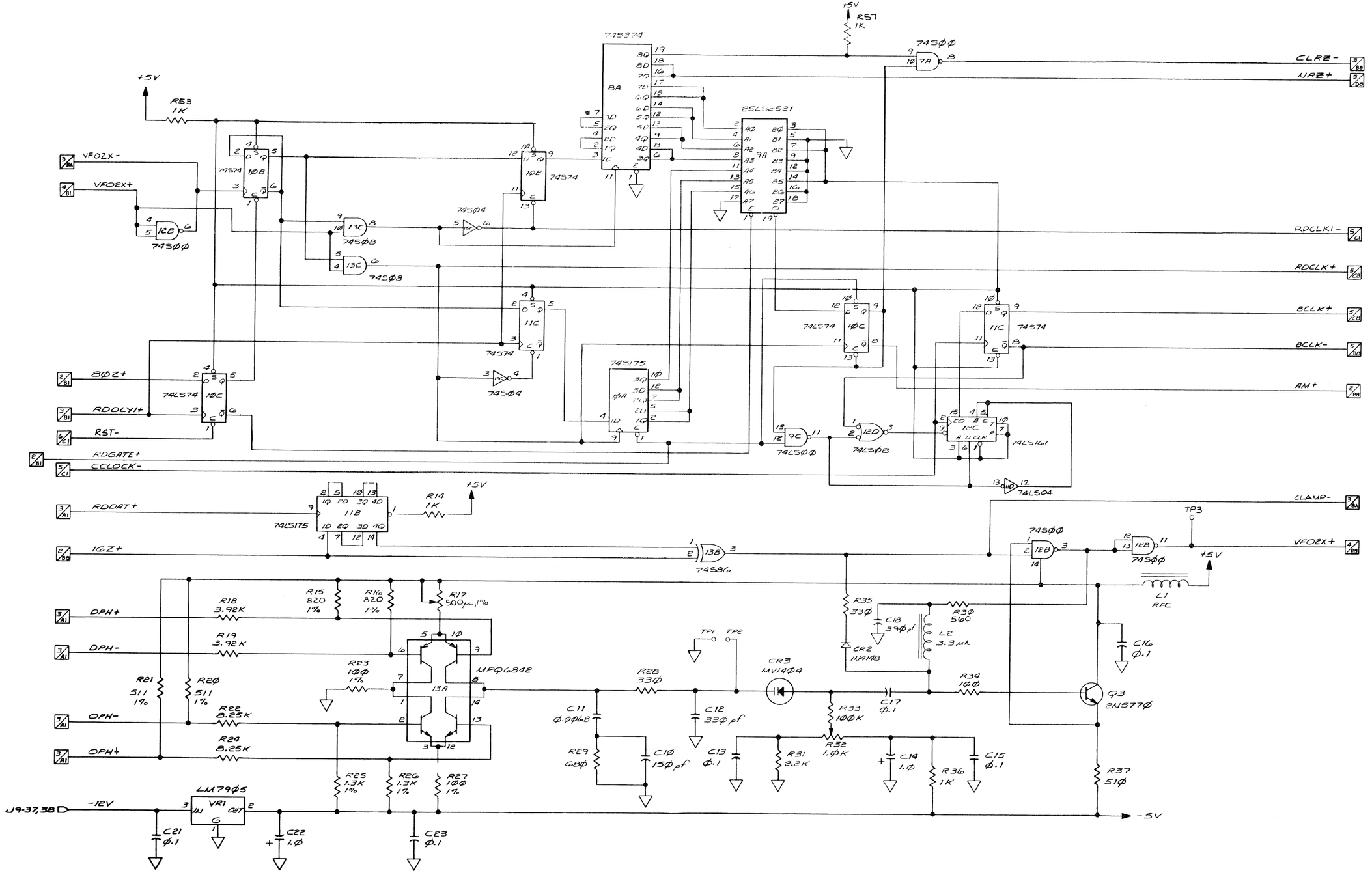

Figure 3-31. HDC Board Schematic. (Page 4 of 8)

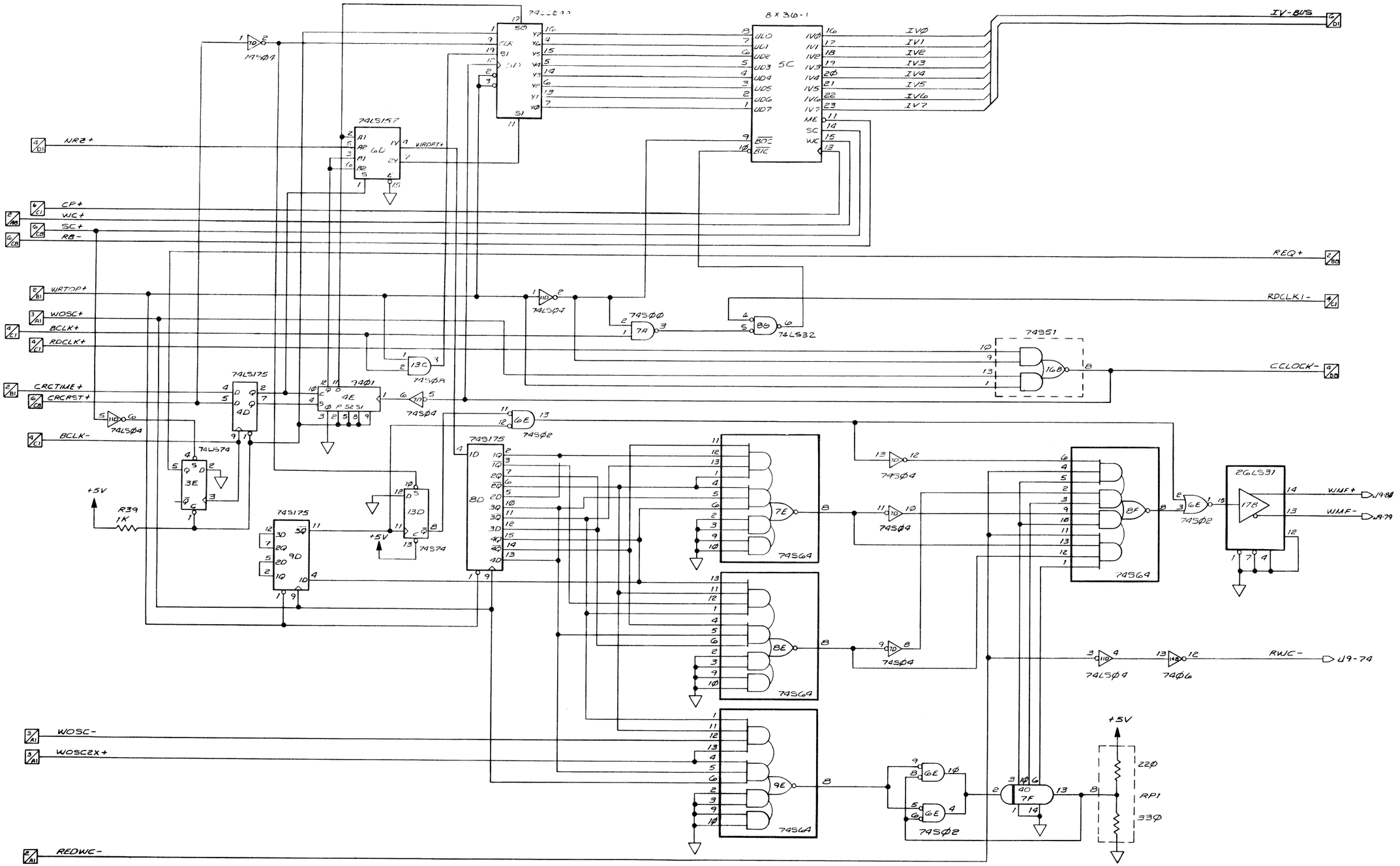

Figure 3-31. HDC Board Schematic. (Page 5 of 8)

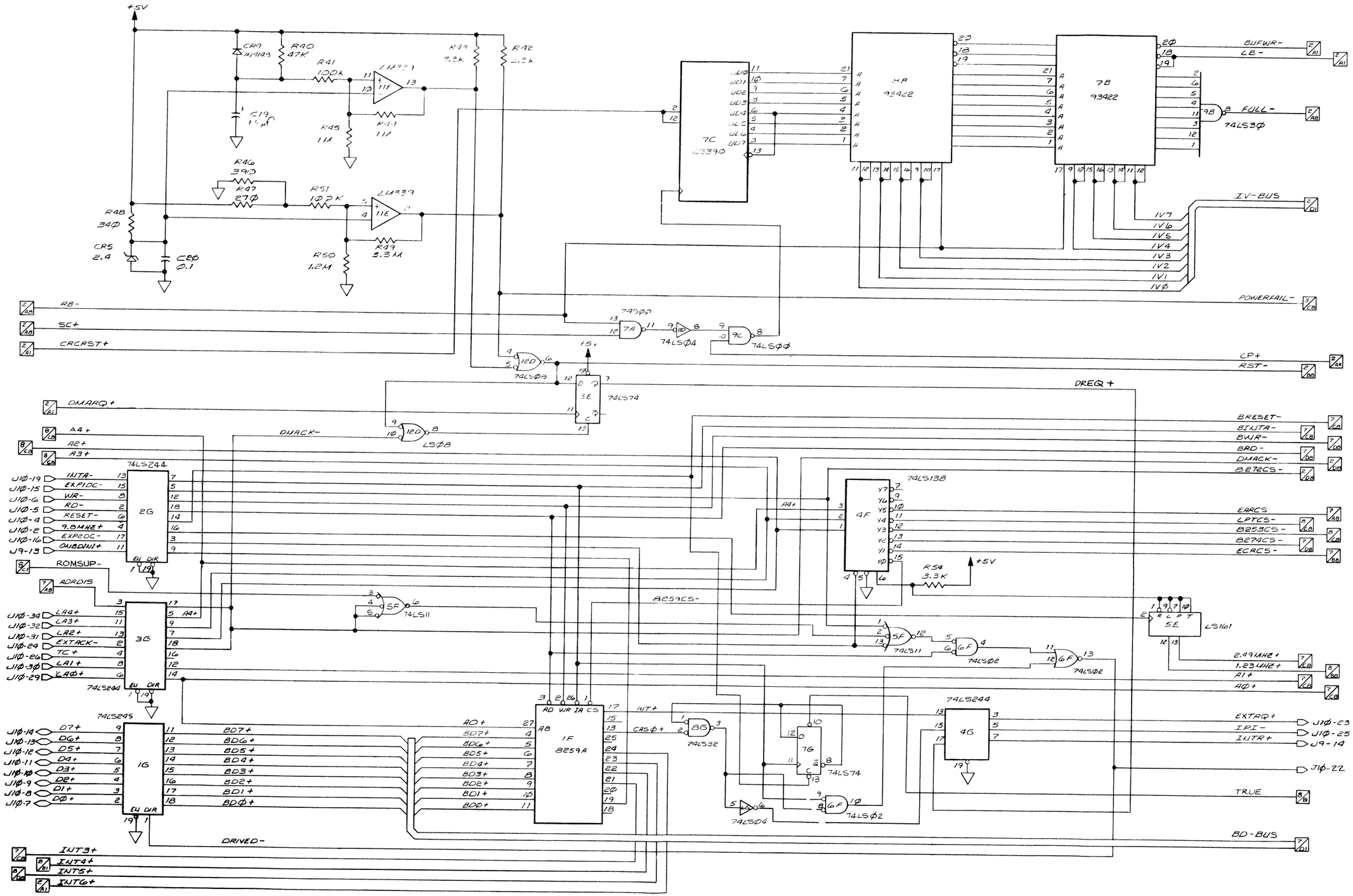

Figure 3-31. HDC Board Schematic. (Page 6 of 8)

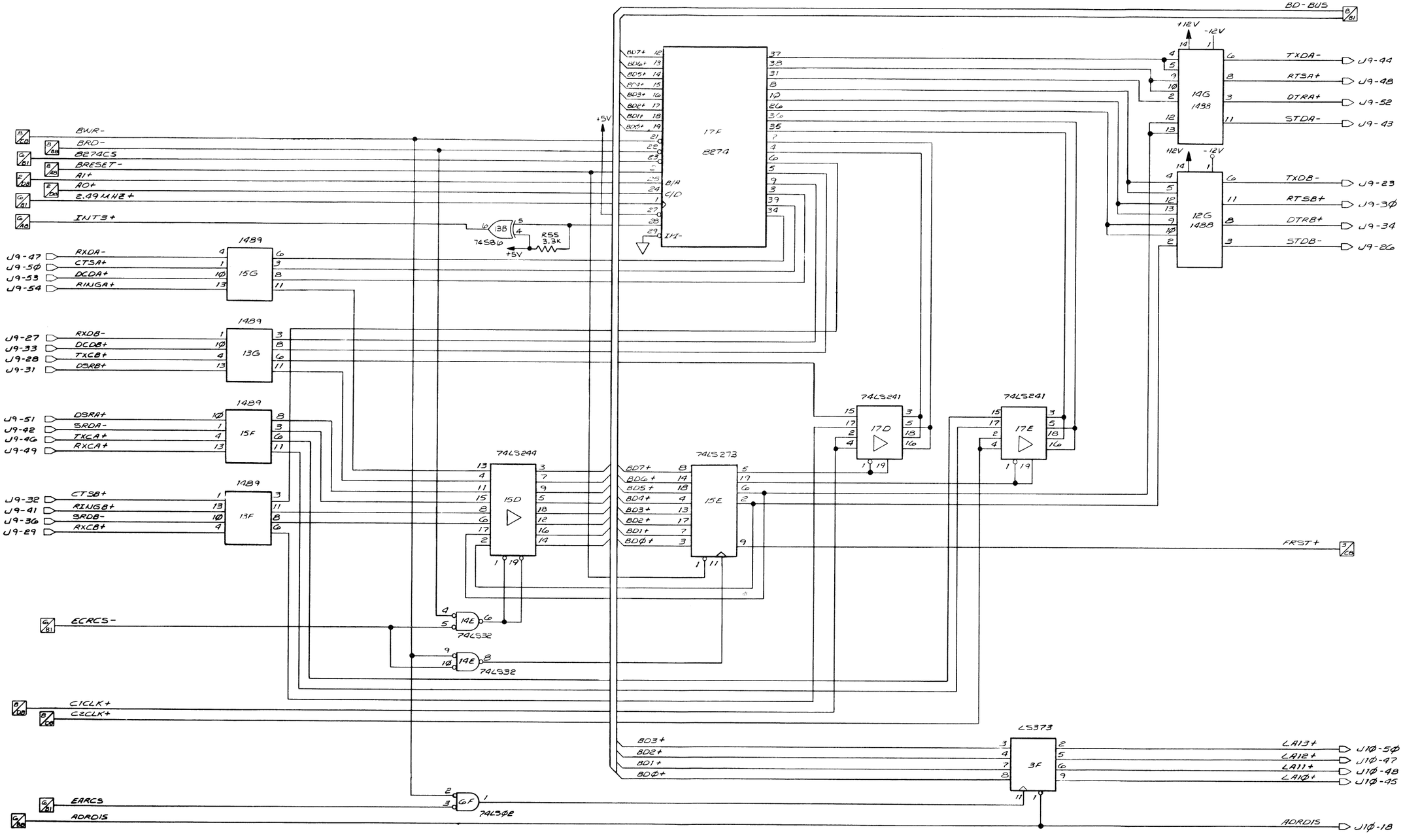

Figure 3-31. HDC Board Schematic. (Page 7 of 8)

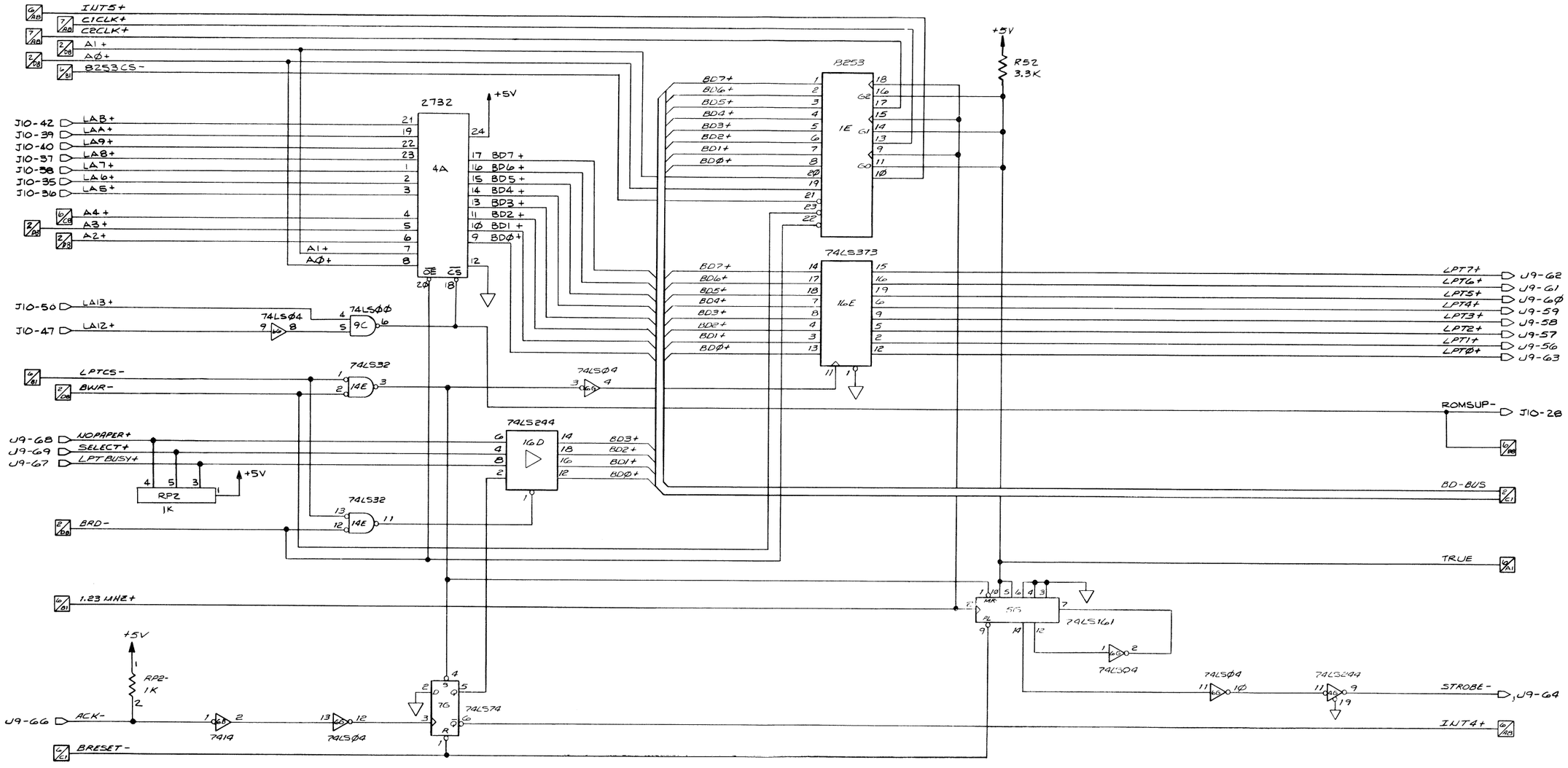

Figure 3-31. HDC Board Schematic. (Page 8 of 8)

If line address bits LA12+ and LA13+ are high, ROMSUP- (ROM Suppress) goes low, which enables bootstrap ROM 4A while simultaneously disabling the bootstrap ROM on the CPU Board.

All other input/output ports, such as those for the 8272, 7201, and 8253 are discussed below in their respective sections.

With respect to read or write operations between the HDC Board and the CPU Board, the default is a write operation. The default is determined by the pin 1 direction input of transceiver 1G, which, under normal circumstances is high. The direction of 1G is changed by DRIVED- (Drive Data Bus) when an input/output port is selected and the RD- strobe from the CPU Board is active.

The EXP1DC- and EXP2DC- decode lines are ORed at pins 1 and 13 of gate 5F, respectively. A third input at pin 2 of 5F is the ORed result of ROMSUP- at pin 3 of 5F and EXTACK- at pin 4 and 5 of 5F. ROMSUP- is an output from pin 6 of gate 9C (as shown on page 8 of Figure 3-31); EXTACK- is the External DMA Acknowledge signal from the CPU Board's DMA controller. When any device or function on the HDC Board is selected, pin 12 of 5F goes low to the pin 5 input of AND gate 6F. The pin 4 input of 6F is RD- from the CPU Board through receiver 3G. When RD- is low and any function is selected on the HDC Board, a low signal, DRIVED- is sent from pin 4 of 6F through pin 13 of NOR gate 6F to change the direction of data flow to be from the HDC Board to the CPU Board.

Interrupt Control

As described above in the "Architecture" section under "Interrupt Control", the 8259A interrupt controller accepts interrupt requests from five sources:

Interrupt Source	Origin	Interrupt Input 8259A 1F	Level
CPU Board	J9-13	INT1+ pin 19	1
Unused	---	---	2
7201	17F-28	INT3+ pin 21	3

Interrupt Source	Origin	Interrupt Input 8259A 1F	Level
Printer interface	7G-6	INT4+ pin 22	4
8253	1E-10	INT5+ pin 23	5
8X36	5A-7	INT6+ pin 24	6
Unused	---	---	7

When a device connected to the 8259A asserts its interrupt line, the 8259A takes INT+ (Interrupt) high at pin 17 of 1F. INT+ is sent to the CPU Board as INTR+ (Interrupt Request) at pin 7 of transmitter 4G. The CPU responds to the interrupt request by sending two INTA- pulses through pin 7 of receiver 2G. The first INTA- pulse allows the 8259A to resolve the priority of the INT1+ through INT6+ (Interrupt Priority 1-6) lines. During the second INTA- pulse, the 8259A sends the appropriate interrupt vector to the CPU. A Flip-flop at 7G and gates at 6G ensure that DRIVED- is low only during the second INTA- pulse.

The INTA pulses are sent to pin 26 of the 8259A, pin 11 of flip-flop 7G, and pin 9 of AND gate 6F. During the rising edge of the first INTA- pulse, the pin 9 FRZ+ (Freeze) output of 7G goes high. A low is sent from the pin 8 Q- output of 7G and ANDed with CAS0+ (Cascade) at pins 1 and 2 of gate 8G. The low pin 3 output of 8G is sent to pin 9 of gate 6F and ANDed with the INTA- pulse at pin 8. The resulting high at pin 10 of 6F is sent to pin 12 of 6F and is then output as a low DRIVED- at pin 13 of 6F to data transceiver 1G. The 8259A next sends an 8-bit interrupt vector to the CPU on the BD0+-BD7+ data lines.

If the CPU Board (INT1-) is the interrupt requester, the interrupt vector comes from the CPU Board, not from the 8259A. The 8259A uses the CAS0+ line to send a high through pin 3 of gate 8G as 7201VECT+ (7201 Interrupt Vector). 7201VECT+ is inverted at pin 6 of 6G and sent through pins 15 and 5 of transmitter 4G to the CPU Board as IPI- (Interrupt Pending In) to inform the 7201 when it should drive an interrupt vector to the CPU. 7201VECT+ also disables

DRIVED- to prevent the 8259A from driving an interrupt vector onto the BD0+-BD7+ data lines.

Clock Divider

The clock divider is at counter 5E. It takes the 9.8MHZ+ (9.8-MHz clock) signal from the CPU Board as its input and divides it down to 2.46 MHz at pin 13 and to 1.23 MHz at pin 12. The 2.46MHZ+ (2.46-MHz clock) is sent to the 7201 at 11A (17F). The 1.23MHZ+ (1.23-MHz clock) is sent to both the printer interface strobe generator at 5G and the 8253 at 1E.

8253 Counter/Timer Logic

As shown above on page 8 of the HDC Board schematic, Figure 3-31, the Intel 8253 counter/timer circuit at 1E provides three fully programmable 16-bit counter/timers. Two of the counters are used for generating the internal clocks for RS-232-C Ports A and B and the third counter is used to generate general purpose interrupts for software. Figure 3-32 below shows the functional blocks of the 8253 logic on the HDC Board.

8253 Programming

The input clock frequency sent to each counter channel is 1.23 MHz. The assignment of each counter channel in the 8253 on the FDC or HDC Board is:

Counter	Output	Assignment
0	1E-10	Timer interrupts (INT5+)
1	1E-13	RS-232-C Port B (C1CLK+)
2	1E-17	RS-232-C Port A (C2CLK+)

The eight buffered data bus lines BD0+-BD7+, are connected to the 8253 for communications with the CPU. During input/output access to the 8253, 8253CS- from pin 12 of 4F selects the timer. The data needed to program the channels is actually transferred when either BRD- at pin 22 of 1E or BWR- at pin 23 goes low. Address lines A0+ and A1+ are used to select the particular register

within the 8253. Detailed programming information for the 8253 is described in the "Architecture" section under "8253 Counter/Timer."

RS-232-C Communications Logic

As shown on page 7 of Figure 3-31, RS-232-C communications are based on an NEC 7201 (Intel 8274) MPSC. Since the 7201 does not support secondary transmit and receive lines, the RS-232-C communications channels use the Extended Control Register at Port A4h for this purpose. The Extended Control Register also contains two bits for selection of internal or external transmit and receive clocks for each of the communications channels. The status of several other lines not supported by the 7201 can be read in the Extended Communications Status Register, also at Port A4h.

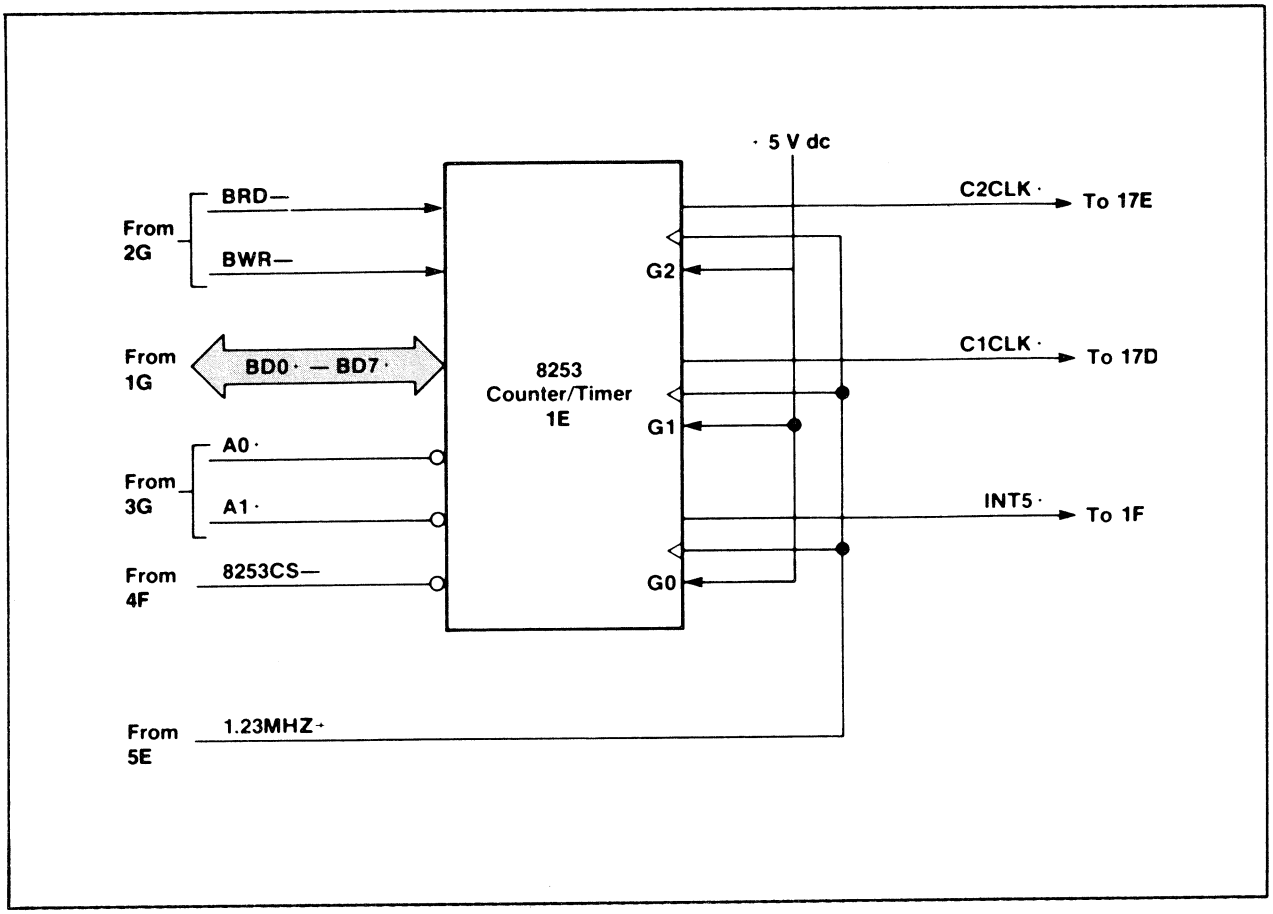

Figure 3-32. 8253 Counter/Timer Logic.

Signal Name	Mnemonic	Channel	Converter
Transmit Data	TXDA-	A	14G
	TXDB-	B	12G
Secondary Transmit Data	STDA-	A	14G
	STDB-	B	12G
Request to Send	RTSA+	A	14G
	RTSB+	B	12G
Data Terminal Ready	DTRA+	A	14G
	DTRB+	B	12G
Receive Data	RXDA-	A	15G
	RXDB-	B	13G
Secondary Receive Data	SRDA+	A	15F
	SRDB+	B	13F
Clear to Send	CTSA+	A	15G
	CTSB+	B	13F
Data Set Ready	DSRA+	A	15F
	DSRB+	B	13G
Carrier Detect	DCDA+	A	15G
	DCDB+	B	13G
Ring Indicator	RINGA+	A	15G
	RINGB+	B	13F
External Transmit Clock	TXCA+	A	15F
	TXCB+	B	13G
External Receive Clock	RXCA+	A	15F
	RXCB+	B	13F

Transmit and receive clocks for both communications channels can come either from the on-board 8253 counter/timer at 1E (as shown on page 8 of Figure 3-31) or from the DCE through the TXCA+, TXCB+, RXCA+, and RXCB+ lines. Wired as multiplexers, drivers 17E and 17D perform the clock selection for RS-232-C communications Channels A and B, respectively. Selection pins 1 and 19 of 17E are controlled from pin 19 (bit D5) of Extended Control Register 15E. When pin 16 of 15E is high, the TXCA+ and RXCA+ clock lines present at pins 15 and 17, of 17E are sent to pins 3 and 5 of 17E and then to pins 36 and 35 of the 7201. When pin 16 of 15E is low (the default

condition), the C2CLK+ (8253 Counter 2 Clock) output of 8253, present at pins 2 and 4, respectively, of 17E is sent to pins 18 and 16 of 17E and then to pins 35 and 36 of the 7201.

The driver/multiplexer at 17D for communications Channel B operates in the same manner as 17D does for communications Channel A, except that bit D4 at pin 5 of 15E controls the selection, and TXCB+ comes from pin 6 of 13G. RXCB+ comes from pin 6 of 13F. The C1CLK+ (8253 Counter 1 Clock) output of 8253 is used, and the destination pins on the 7201 are pins 7 and 4.

Printer Interface Logic

Figure 3-34 below shows the functional blocks of the Centronics-compatible printer interface. Also see page 8 of the HDC Board schematic, Figure 3-31, during the following discussion.

The CPU sends 8-bit characters to the printer interface on the BD0+-BD7+ buffered data lines. Data latch 16E on the HDC Board is selected when both LPTCS- (Line Printer Chip Select) and BWR- go low at pins 1 and 2, respectively, of gate 14E. The low pin 11 output of 14E is sent to pin 11 of 16E to latch the eight data bits. The pin 1 output enable of 16E is always low, so the data is then immediately sent to the printer on the LPT0+-LPT7+ (Line Printer Data) printer output lines.

The low pin 3 of gate 14E also resets counter 5G, which generates a STROBE- (Character Strobe) pulse informing the printer that data is available on the LPT0+-LPT7+ printer output lines. Counter 5G is wired in a manner, such that, after pin 3 of 14E goes low to reset it, one microsecond of time lapses to allow the STROBE- pulse to go high at pin 13 of 5G for one microsecond. The pulse is inverted at pin 10 of 6G, buffered at pin 9 of 4G, sent off of the HDC Board as STROBE- through pin 64 of J9, and finally sent to the Printer jack J3 on the back panel. After STROBE- goes high again, counter 5G waits for the next reset pulse from pin 3 of 14E.

Pin 3 of 14E also sets the buffer busy flip-flop at 7G. When the printer receives a character on the LPT0+-LPT7+ printer output lines, it responds by pulling the ACK- (Acknowledge) handshake line

low. ACK- is inverted at pin 2 of 6B, inverted again at pin 12 of 6G, and sent to the pin 3 clock input of flip-flop 7G. The pin 5 BUFBUSY+ (Buffer Busy) output of 7G is high when the character is sent. When ACK- goes low, pin 5 of 7G goes low (grounded pin 2 D input), indicating that the CPU can send another character. The pin 5 output of 7G is sent to the Printer Status Register at pin 2 of buffer 16D.

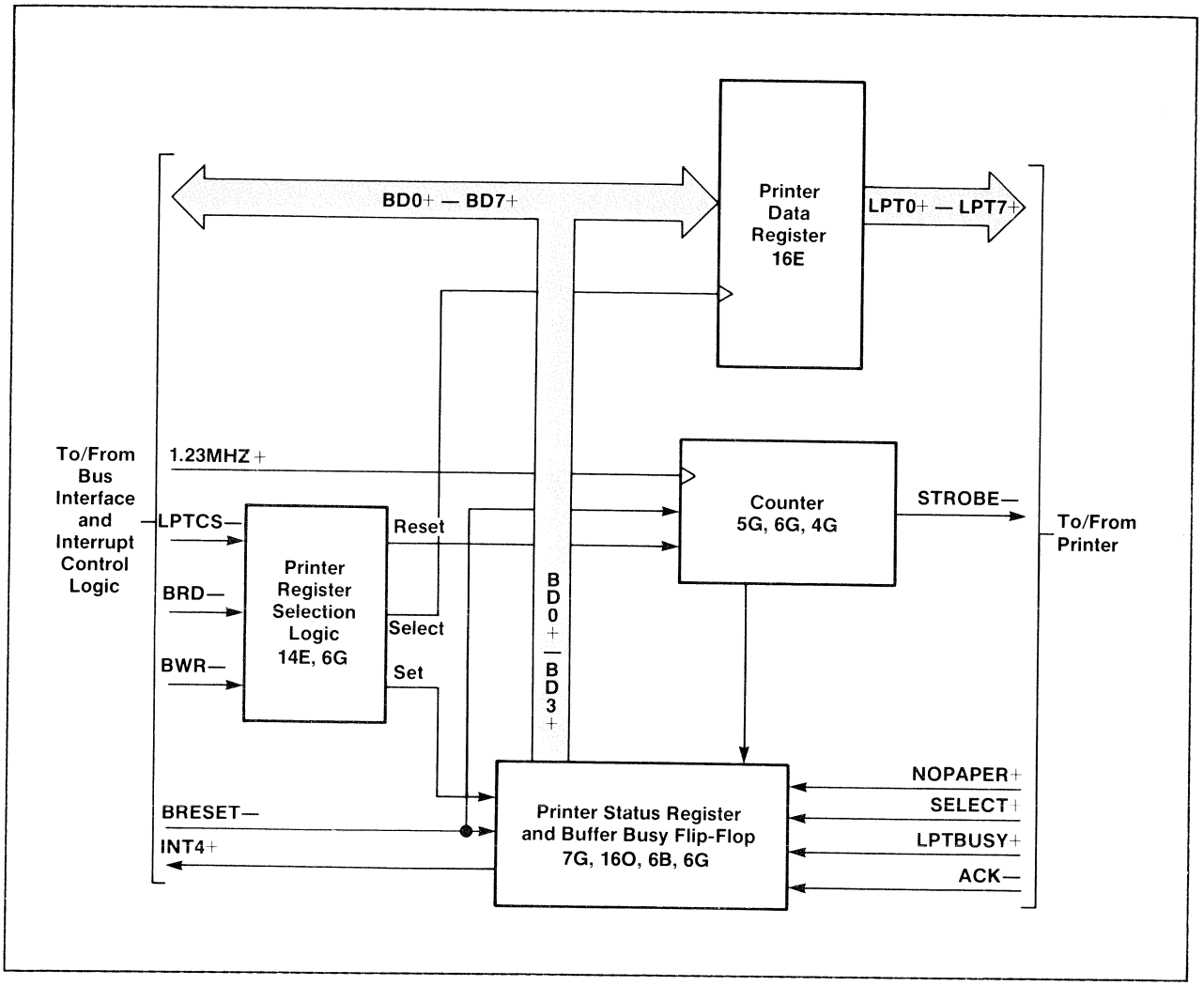

Figure 3-34. Printer Interface Logic.

When pin 5 of 7G is low, the pin 6 Q- output of 7G is high as INT4+. INT4+ is sent to the pin 22 input of the 8259A interrupt controller. The software polls the BUFBUSY+ bit of the Printer

Status Register at Port B0h to determine when the printer can accept another character. If the character is acknowledged quickly (BUFBUSY+ stays high for only a short time), the software assumes that the printer has a buffer and sends another character immediately. If the software polls the Printer Status Register and finds that BUFBUSY+ is staying high for a longer time between characters, the software enables the INT4+ mask bit in the 8259A. This allows the pin 6 Q- output of flip-flop 7G to interrupt the CPU when it requires another character or when the printer buffer is empty.

The Printer Status Register contains four bits of status information: LPTBUSY+, SELECT+, BUFBUSY, and NOPAPER+, which correspond to bits BD0+-BD3+ in buffer 16D. The CPU reads the Printer Status Register when LPTCS- and BRD- are both low at pins 13 and 12 of gate 14E. The low pin 11 output of 14E enables buffer 16D.

AWS-240 Hard Disk Controller Logic

The circuitry of the hard disk controller on the HDC Board can be separated into four major groups:

- the 8X300 microcontroller and its peripheral devices,
- floppy disk control interface,
- the floppy disk read and write circuits, and
- the hard disk read and write circuits.

Figure 3-35 below, shows the functional blocks of the floppy and hard disk controller and how the three major blocks of circuitry can be organized.

The microcontroller logic includes the Signetics 8X300 microcontroller, its microcode ROM, an interface element with the HDC Board bus interface logic, and input/output ports associated with control of the floppy and hard disk drives.

The disk drive control circuits include buffers and the 8X330 floppy disk controller.

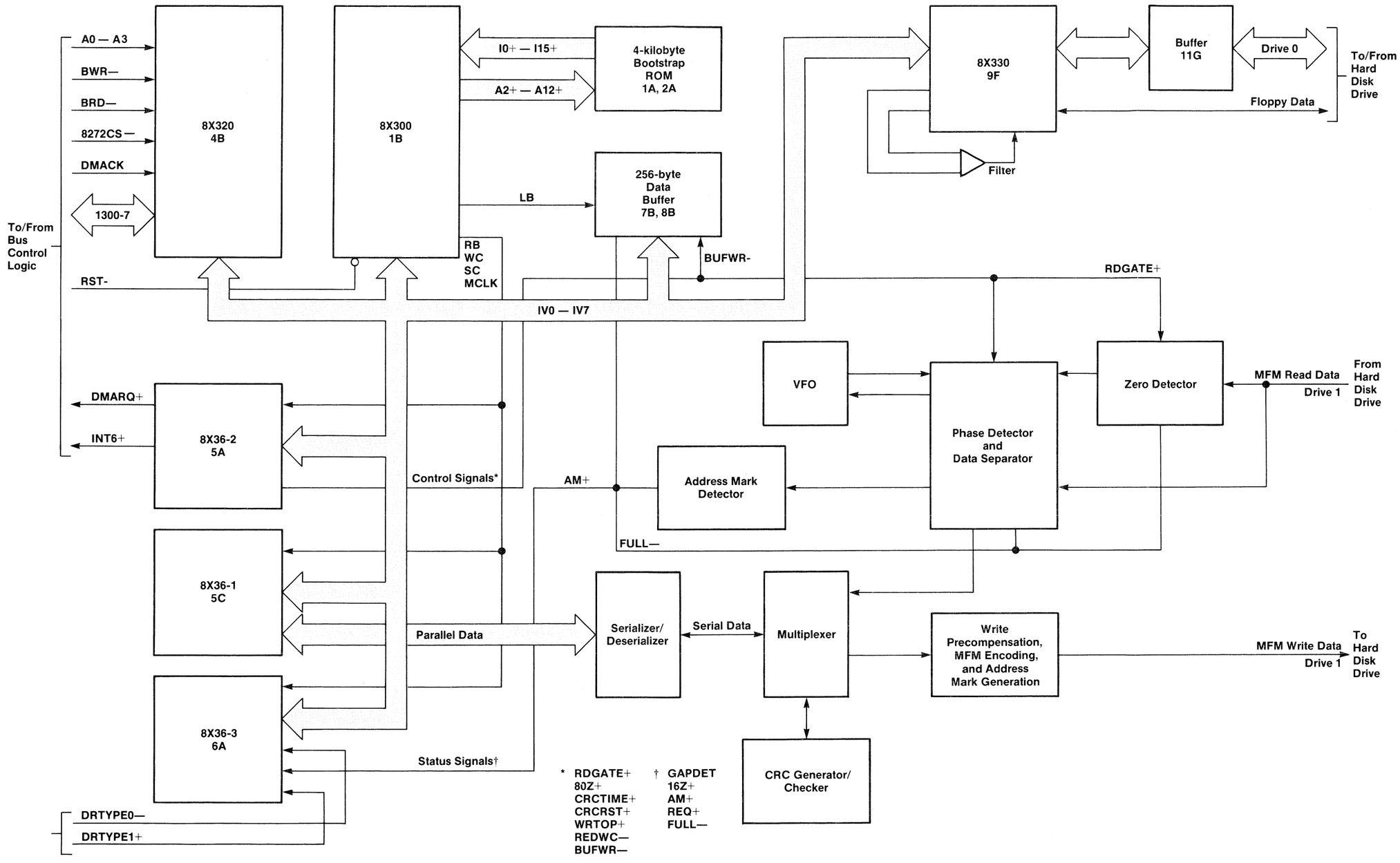

Figure 3-35. AWS-240 Hard Disk Controller Logic.

The floppy disk drive read and write circuits include an 8X330 floppy disk controller and a low-pass filter.

The hard disk drive read and write circuits include zero and phase detection, data separation, address mark generation and detection, write precompensation, and CRC generation and detection.

In addition to Figure 3-35, also refer to Figure 3-31 above, the HDC Board schematic, as the major reference during the following discussion.

8X300 Microcontroller Logic

As shown on page 2 of Figure 3-31, the Signetics 8X300 microcontroller at 1B is the single controlling element for the AWS-240 floppy and hard disk drives. The 8X300 has three separate address and data buses, none of which are associated with the LA0+-LA13+ or BD0+-BD7+ buses on the HDC Board.

The 8X300 operates from a microprogram stored in ROMs 1A and 2A. The two ROMs are addressed in parallel by the 8X300's A2-A12 (Address) bus. The resulting 16-bit microcode instruction is read by the 8X300 on its I0-I15 (Instruction) bus.

The 8X300 communicates with other devices associated with the hard disk controller on the IV0-IV7 (Instruction/Vector) bus. The IV bus is multiplexed to supply data (Instructions) and address information (Vectors) to the input/output devices. The IV bus serves two independent banks of input/output devices (right and left) for control of the hard disk drive read and write circuitry, and for communication with the CPU.

The only input/output device on the left bank of the IV bus is the 256-byte data buffer. The data buffer is made up of two RAMs at 7B and 8B (as shown on page 6 of Figure 3-31). The RAMs temporarily store data being transferred between one of the disk drives and the AWS-240 RAM array on the CPU Board.

All other input/output devices are on the right bank of the IV bus:

- An 8X320 bus interface register array at 4B, provides an interface between the IV bus and the BD0+-BD7+ data lines of the HDC Board.

- An 8X330 floppy disk controller at 4F (shown on page 3 of Figure 3-31), handles read and write data from the floppy disk drive and control signals for both drives.

- An 8X36 bidirectional input/output port is used for control of the hard disk circuitry. The 8X36 at 5A is an output port for eight hard disk, interrupt, and DMA control lines. The 8X36 at 6A is a status port for various hard disk read and write circuits and also provides two status lines, DRTYPE0- and DRTYPE1- (Drive Type), which are needed by the 8X300 to establish the type and capacity of the disk drives presently operating in the AWS-240.

- An 8X36 at 5C (shown on page 5 of Figure 3-31) serves as the bidirectional serializer/ deserializer port for the hard disk circuitry.

The 8X300 reads from and writes to all of the IV bus input/output devices using five control lines: LB- (Left Bank) and RB- (Right Bank) at 1B pins 31 and 32, WC+ (Write Command) at 1B pin 30, SC+ (Select Command) at pin 29, and MCLK- (Master Clock) at 1B pin 42. All of these lines are buffered at 3C and then sent to the input/output devices. The 8X300 selects either a right or left bank device and places an 8-bit address on the IV bus while both SC+ and MCLK+ are high.

Each port or register on the IV bus has a unique address programmed during the manufacture of the device. Once the 8X300 selects a port or register, that port or register remains selected until the SC line goes high again with a different address. To write data to a port or register on the IV bus, the 8X300 sets WC+ high, RB- (LB- if the disk data buffer is being written to) low, and MCLK+ high while the eight bits of data are on the IV bus. If WC+ is low, the 8X300 will read data from the port or register.

Hard Disk Controller Programming

The 8X320 at 4B contains sixteen 8-bit registers, which are accessible to the 8X300 through the IV bus, and either the CPU or the 8257 on the CPU Board, through the BD0+-BD7+ HDC Board data bus. For this reason, the 8X320 can be thought of as having a primary (HDC Board data bus) and a secondary (IV bus) port. The 16 registers store data, command, and status information for the controller. The content and use of the registers is described under "AWS-240 Hard Disk Controller" in the "Architecture" section, above.

The 8X300 reads from or writes to the secondary port as described above. In the programmed input/output mode, commands are written to, and status is read from, the primary port of the 8X320 when the CPU selects the hard disk controller with 8272CS- at pin 34 of 4B. The A0+-A3+ address lines select one of the 16 registers in the 8X320; either BRD- for a status read or BWR- for a command is pulsed; then the data is transferred on the BD0+-BD7+ data bus.

When a DMA mode read or write is in progress, the 8257 on the CPU Board controls the HDC Board address and data buses. The 8272CS- control line has no effect during the DMA mode. Only the BRD- or BWR- strobes are asserted causing the data transfer to occur on the BD0+-BD7+ data bus. Also during the DMA mode, only the DMA Data Register at Port 80h can be accessed. The DMACK- acknowledge strobe is NANDed with the A0+ address line at pins 2 and 1, respectively, of gate 9C to ensure that only the DMA Data Register can be accessed. During the DMA mode, when the 8X300 requires service, it sets DMARQ+ (DMA Request) high through input/output register 5A.

As shown on page 6 of Figure 3-31, DMARQ+, clocks pin 11 of 3E. Pin 9 of 3E is sent to buffer 4G pin 17 as DREQ+ (DMA Request) and then to the CPU Board as EXTRQ+ (External DMA Request). Flip-flop 3E is cleared either by DMACK- from the CPU Board or by RST- (Reset) at pin 9 of 12D.

Disk Drive Controller Interface

As shown on page 3 of Figure 3-31, the 8X330 at 9F provides the control and status line interface between the IV bus and two disk drives. The

8X300 loads internal registers in the 8X330 before each disk operation to tailor the operating characteristics of the control lines to the selected drive. The 8X330 also contains the floppy disk drive read and write circuits described below.

From the 8X300 at 9F, buffer 11G inverts and drives various control lines to the J9 Motherboard connector and to the disk drives. The STEP- (Step Pulse) line at pin 9 of J9 increments the drive read/write head carriage one track on the disk surface, either in or out, depending on the state of DIR- (Direction) at pin 7 of J9. HDSEL0- through HDSEL2- (Head Select) at pins 17, 12, and 73 of J9 select one of eight possible read/write heads on the drive selected by the DS0- (Drive Select) line at pin 19 of J9. DS1- at pin 8 of J9 is not used. WRDATA- (Write Data) at pin 21 of J9 is the precompensated write data sent only to the floppy disk drive. Finally, WRGATE- (Write Gate) at pin 72 of J9 is the write data enable for either selected disk drive. WRGATE- is automatically disabled upon power-up or during a power failure.

The status lines from the disk drives to 8X330 9F include WRPROT- (Write Protect) at pin 18 of J9 to indicate that the selected disk drive is allowing only read operations. TRACK0- (Track 0) at pin 70 of J9 indicates that the selected read/write head positioned over the first readable track on the disk media. INDEX- at pin 11 of J9 indicates that the disk drive is detecting the beginning of the first physical sector on the track. READY- at pin 10 of J9 indicates that the selected drive is ready to perform a read, write, or seek operation. SKCOMP- (Seek Complete) used for the hard disk drive only, indicates whether the seek operation just performed was successful. RDDATA- (Floppy Read Data), used only for the floppy disk drive, is the read data input to the 8X330 data separator and phase-locked loop.

The POWERFAIL- input to the 8X330 at pin 18 of 9F is used to disable WRGATE- when the +5-V dc power supply falls below +4.5 V dc. As shown on page 6 of Figure 3-31, a stable +2.4-V dc reference is generated at zener diode CR5. Comparator 11E pin 2 goes low when its pin 5 input drops below +2.4 V dc, meaning that the +5 V dc has dropped below 4.5 V dc. Pin 2 of 11E goes to the 8X300 as

POWERFAIL- and also propagates through pin 6 of gate 12D as RST- to reset the 8X300. Also, a power-on reset occurs through the pin 13 output of the other comparator at 11E. When the AWS-240 is powered-up, capacitor C19 must charge above 2.4 V dc through R40 before RST- goes high at pin 6 of 12D.

Floppy Disk Drive Read and Write Circuits

As shown on page 3 of Figure 3-31, the 8X330 floppy disk controller at 9F contains almost all of the read and write circuitry required to convert data bytes from the IV bus to MFM disk data during a write operation, and back again to data bytes during a read operation. The only components required to make the floppy disk controller complete are the 8.0-MHz crystal, Y2; a pass transistor, Q2, for the on-chip voltage regulator; and a low-pass filter, the active component of which is operational amplifier 12F.

Once a read or write command is sent to the Command Register at Port 82h and Drive 0 is specified, the 8X300 configures the 8X330's internal registers to perform the operation. The 8X300 (through the 8X330) selects the drive, read/write head, and the direction of read/write head travel. Next, the 8X300 performs a seek to the specified track on the floppy disk by pulsing the STEP- line a specified number of times. Finally, the 8X300 reads the identification field on the track; if it is correct, a read or write operation can begin.

Read data for the floppy disk drive appears at pin 24 of the J9 Motherboard connector and is sent to pin 5 of the 8X330 at 9F. Internally, 9F performs data separation to generate the data window and synchronized data to an on-chip data processor and CRC (Cyclic Redundancy Code) checker. The external low-pass filter is used during the data separation process to control the phase-locked oscillator in the 8X330. Two outputs from the 8X330's on-chip phase detector, PU (Pump Up) at 9F pin 34, and PD (Pump Down) at 9F pin 33, are used as inputs to the low-pass filter; they indicate that the frequency of the oscillator is either too low or too high. PU and PD are integrated by the low-pass filter and result in a change in the amount of current delivered to the pin 35 CCO (Current-Controlled

Oscillator) input of the 8X330, thus changing the frequency of the oscillator. If no floppy disk read operation is taking place, the 8X330's internal oscillator is locked to the 8.0-MHz crystal frequency.

After data separation, the 8X330 deserializes the disk data and is read by the 8X300 on the IV bus. The data buffer on the left bank of the IV bus is not used for floppy disk read and write operations. Instead, the 8X300 transfers the byte it just read from the 8X330 to the DMA Data Register (Port 80h) in the 8X320 at 4B and pulses the DMARQ- line. The 8257 on the CPU Board reads the byte from Port 80h during the DMA acknowledge cycle. If there is a disk read error, the data is still transferred from the floppy drive to the RAM array on the CPU Board. The error is detected when the CPU reads the status registers after the command completes (see "AWS-240 Hard Disk Controller" in the "Architecture" section for details).

For a floppy disk write operation, the 8257 writes data bytes to the DMA Data Register and the 8X300 transfers bytes to the 8X330. The bytes are then serialized, the amount of write precompensation is applied, and the bits are sent to Drive 0 on the WRDATA- line when WRGATE- is low at pin 72 of J9.

Hard Disk Drive Read and Write Circuits

As shown on page 3 of Figure 3-31, the reference clock for the hard disk read and write circuits is a 20.0-MHz oscillator composed of crystal Y3 and three inverters at 15C. The oscillator frequency is divided at pin 5 of flip-flop 14D to 10.0 MHz. The AND/OR gate operating as a multiplexer at 16B sends either the 10-MHz oscillator frequency or MFM read data from the disk drive to the phase-locked loop phase detector. The selection is made by the complementary outputs of pin 5 and 6 of flip-flop 15A, which is used as a detector flag for sixteen MFM 0s.

When RDGATE+ (Read Gate) is low at pin 13 of gate 13C (that is, when no read operation is taking place), pin 11 of 13C is low, clearing pin 11 of one-shot 17A, causing counter 16A at pin 11 to load all 0s, and resetting pin 4 of flip-flop 15A

(low D input). The devices 12F, 13C, 17A, counter 16A, and flip-flop 15A, form the zero detector.

Zero Detector. When MFM data from the hard disk drive appears at the pin 3 output of RS-422 receiver 12F, they are applied to the pin 10 input of one-shot 17A. 17A has a time constant, which is set by R10 and C6 to time out at an interval slightly longer than the 200 ns bit-cell time of the hard disk data. When a series of MFM 0s are read from the hard disk, 17A never has an opportunity to time out. The pin 5 output of 17A holds the CD (Count Down) input of 16A high; the MFM data from pin 3 of 12F causes 16A to count up until sixteen 0s occur. Pin 12 of 16A then pulses, clocking flip-flop 15A to a reset condition. The high at pin 6 of 15A causes the MFM data to be sent through pin 6 of AND/OR gate 16B. 16B's pin 6 output is inverted at pin 2 of 15C and sent to the phase detector as RDDAT+ (Read Data). The high at pin 6 of 15A is also sent to counter 11B and gate 13B (as shown on page 4 of Figure 3-31).

When no read operation is in progress, the phase detector is locked to the 10-MHz clock at pin 5 of 15A to pin 6 of 16B. This locking prevents the VFO from oscillating at a harmonic frequency due to the lack of updates for the phase-locked loop.

When the detector flag for sixteen MFM 0s is set, it also clocks pin 11 of flip-flop 15A. The low pin 9 output of 15A is sent to pin 1 of the 8X36 input/output port at 6A and then to the 8X300 as a status bit, GAPDET- (Gap Detect). GAPDET- is used as a status bit by the 8X300 to ensure that it is reading a valid gap before a sector and not just a long field of 0s in a sector. These two flags work differently to prepare the read circuitry for an operation. When 16 MFM 0s are detected, there is good reason to assume that what is being read is a valid gap before a data sector. Since it takes some time for the VFO to lock onto the MFM data, the presence of 16 MFM 0s is sufficient to start the lockup process. Since sixteen bytes of 0s are present in a gap (and two bytes are used to get the 16Z+ flag) another ten byte-intervals (about 16.0 μs) are allowed to ensure that the VFO has enough time to lock onto the incoming data stream. The 8X300 monitors

GAPDET-, while a timer in the 8X300 microprogram counts the ten bytes of 0s that should appear if the gap is valid.

If one-shot 17A detects an MFM 1 bit in the data stream, it will time out; its high pin 12 thus clears pin 14 of counter 16A. The low pin 5 output of 17A will set GAPDET- to a high at pin 10 of 15A. If GAPDET+ goes high, the 8X300 takes RDGATE+ low at pin 13 of gate 13C, which reloads counter 16A with all 0s, clears one-shot 17A, and sets the zero detector flip-flop at pin 4 of 15A. If GAPDET+ remained low during the ten byte-interval count, the 8X300 asserts 80Z+ (eighty 0s detected) at pin 2 of input/output port 5A.

Phase Detector. Three flip-flops form the phase detector for the phase-locked loop: the phase detector enable flip-flop at 15B, and two flip-flops at 14C. An MFM data bit from pin 6 of AND/OR gate 16B clocks pin 3 of flip-flop 15B, which sets it, thus enabling the two phase detector flip-flops at 14C. The output pins 5 and 6 at 14C are the data phase comparison signals DPH- and DPH+ (Data Phase), respectively. These two signals are compared with output pins 9 and 8 of flip-flop 14C, which are the VFO phase comparison signals, OPH- and OPH+ (Oscillator Phase).

The leading edge of the MFM data pulse enables the data and phase comparison flip-flops. At the same time, the data pulse is sent to the pin 1 input of delay line 10D where it is delayed 60 ns. The delayed data pulse at pin 12 of the delay line is sent to the VFO as RDDAT1+; it also clocks pin 3 of the data phase comparision flip-flop at 14C. The VFO phase comparison flip-flop is clocked at pin 11 by VFO2X- (VFO Frequency Times 2). When the flip-flops are enabled, and if an error exists between the frequency of the data and the VFO, one of the flip-flops at 14C will be set before the other one.

If, for instance, the VFO2X- signal clocks pin 11 of 14C before the delayed data pulse clocks pin 3 of 14C, the VFO frequency must be too fast. If the delayed data pulse clocks pin 3 of 14C before VFO2X- clock pin 11 of 14C, the VFO must be too slow. The two sets of complementary outputs of the 14C flip-flops are sent to a charge pump (as

shown on page 4 of Figure 3-31) to change the frequency of the VFO accordingly. Once both flip-flops are set, the high levels at input pins 9 and 10 of gate 12B cause, through pin 11 of gate 12D, the three flip-flops to be reset to their initial states.

Charge Pump and VFO Oscillator. As shown on page 4 of Figure 3-31, the four phase comparison signals described above are applied to a 4-transistor error amplifier at 13A. In the example given above, if the data phase comparison flip-flop sets before the VFO phase comparison flip-flop sets, the VFO frequency is too low to be in phase with the incoming data. The DPH- and DPH+ lines from the data phase comparison flip-flop cause the PNP transistor at pins 8, 9, and 10 of 13A to turn on before the OPH- and OPH+ signals cause the NPN transistor at pins 14, 13, and 12 to turn on. This causes the PNP transistor to turn on and increases the voltage on the cathode of varactor diode CR3 before the NPN transistor turns on. Since the PNP transistor is on for a longer time than the NPN transistor, there is a net increase in voltage at CR3. If the VFO frequency is too high, as indicated by the VFO phase comparison flip-flop setting first, the NPN transistor turns on first, causing a net decrease of voltage at CR3.

To keep the error amplifier 13A balanced, an operational amplifier at 12F monitors pins 1 and 7 of 13A at its inverting input. If the voltage at pins 1 and 7 of 13A is slightly positive, the error amplifier is unbalanced in the positive direction and requires a negative offset for correction. The positive voltage at inverting pin 6 input of 12F causes the pin 7 output to go low in proportion to the voltage. This, in turn, causes a lower voltage to appear (through R61 and R17) at pins 5 and 10 of the two PNP transistors, which gives a slight bias to the NPN transistors, and thus lowers the positive voltage at pins 1 and 7 of 13A. Also, if pins 1 and 7 of 13A are more negative than the grounded noninverting input of 12F, the output of 12F goes positive, thus removing the negative bias from the NPN transistors.

Phase-Locked Loop. The low-pass filter for the phase-locked loop is composed of R28, C12, C11,

R29, and C10. The varactor diode at CR3 is the main variable frequency control element; as the voltage from the error amplifier 13A changes, CR3's capacitance changes, thus adjusting the frequency of the VFO. The VFO is a Colpitts oscillator at Q3, where the output from the emitter goes to pin 1 of gate 12B. The pin 3 output of 12B is sent to a timing network composed of inductor L2, C17, and R30. These components provide proper phase shift for the oscillator.

A resistor network, which includes a 1-kilohm variable resistor at R32, is used to set the nominal bias voltage for the center freqency of the VFO. When test points TP1 and TP2 are jumpered, the error amplifier at 13A is effectively disabled. The center frequency of the VFO is set to 10.0 MHz as observed at TP3 (VFO2X+).

The VFO synchronizes to the incoming MFM data stream in the following manner. The 16Z+ flag from pin 6 of 15A is sent to the 1D input of shift register 11B and also to pin 2 of exclusive-OR gate 13B. The shift register is clocked by the MFM data stream from pin 2 of 15C, RDDAT+. When the VFO is locked to the 10-MHz crystal oscillator frequency (no gap is detected), pin 3 of 13B is high to pin 2 of 12B, thus keeping the VFO turned on. When the 16Z+ flag goes high, 13B pin 3 goes low for exactly four bit-intervals. Therefore, pin 3 of gate 12B goes high, breaking the feedback loop of the VFO, and thus turning the VFO off. Since shift register 11B is clocked by the leading edge of the MFM data, pin 3 of 13B goes high four bit-intervals later, at the leading edge of the MFM data pulse. The VFO then restarts in phase with the data stream. The output of the VFO at pin 11 of 12B is sent to the data separator as VFO2X+. CLAMP- at pin 2 of 12B is sent back to pin 12 of 12D to disable the three phase detector flip-flops during the time that the VFO is turned off. If the phase detector were not turned off at this time, it would generate a disproportionately large phase detection error.

Data Separator and Address Mark Detector. The output of the VFO, VFO2X+ is inverted at pin 6 of 12B and sent to the phase detector as VFO2X-. VFO2X- also clocks pin 3 of the toggle flip-flop

10B, dividing the VFO frequency by two, to equal 5.0 MHz at pin 5 of 10B. This 5.0-MHz signal corresponds to the rate at which data is read from or written to the hard disk.

In the MFM data stream, a 0 arrives at the boundaries of a bit cell; a 1 arrives in the middle of the bit cell. Therefore, the pin 5 output of 10B is high in the middle of the bit cell and low at the boundaries of the bit cell.

The toggle flip-flop is enabled when the 8X300's software timer counts 80 bit-intervals and sets the 80Z+ flag at pin 2 of input/output Port 5A. The 80Z+ flag is sent to the pin 2 D input of flip-flop 10C and clocked by the 60-ns-delayed MFM data pulse, RDDLY1+ (Read Delay 1). Until 80Z+ is set and RDDLY1+ appears, the toggle flip-flop is held clear at pin 1.

When enabled, the pin 5 output of 10B is sent to the pin 12 D input of 10B. Pin 11 is clocked by the delayed MFM data pulse RDDLY1+ so that if pin 12 is high when pin 11 is clocked, a high appears at the pin 9 Q output. A high at pin 9 means that the arriving data bit appeared in the middle of a bit cell and must be a 1.

Another flip-flop at 11C is clocked by RDDLY+ at pin 3. The D input at pin 2 of 11C is sent to the pin 6 Q output of the toggle flip-flop, 10B. The output at pin 5 of 11C then is a complement of pin 9 of 10B. If pin 9 of 10B is high, pin 5 of 11C must be low. Both the flip-flops at pin 9 of 10B and at pin 5 of 11C are always cleared to 0 at the end of a bit cell. However, since 11C pin 5 is receiving the complementary data from pin 6 of 10B, it remains a 0 while pin 9 of 10B is clocked to a 1. This characteristic is used to detect a unique address mark pattern that always directly precedes an MFM data field.

The address mark byte is A1h (10100001 binary). The unique aspect of this A1h byte is that when the address mark is written, the second 0 from the right (note the underline under this bit above) is inhibited. The MFM encoding rule states that the three 0s in the last four bits of the address mark byte are written at the beginning of the bit cell and the 1 bit is written in the middle of the final bit cell for this byte. The address mark simply has nothing

in the bit cell that corresponds to the second 0 in the last four bits of the byte. When the address mark is read back, and assuming that both the 10B and 11C flip-flops are cleared, the 10B flip-flop clocks the first MFM 0 as a low on its pin 9 Q output. Since 11C's data is the complement of 10B, pin 5 of 11C is high. Again, at the end of the bit cell, both flip-flops are cleared. At this point, the second 0 bit in the field of three 0s was never written on the disk so nothing exists to clock flip-flops 10B and 11C. A 0 still appears at pin 9 of 10B, which is valid for this A1h byte even though the 0 never actually appeared. However, since no complementary data bit (no 1) was present to clock flip-flop 11C, a 0 also appears at pin 9 of 11C. Once again, 10B and 11C are cleared at the end of the bit cell. The third MFM 0 that was written in the address mark byte clocks a 0 at pin 9 of 10B and a complement bit 1 at pin 5 of 11C.

For these three bit-intervals, a unique noncomplementary pattern occurred at the outputs of flip-flops 10B and 11C. For any other byte of data read from the hard disks, the pattern at pin 5 of 11C is always an exact complement of pin 9 of 10B. The address mark however, generates 000 at pin 9 of 10B and 101 at pin 5 of 11C. The outputs of both flip-flops are clocked into respective shift registers at 8A and 10A by clocks at pin 8 and pin 6 of gate 13C. The 000 and 101 patterns are compared at 9A. When 9A finds this special noncomplementary pattern in the data bit stream (according to 9A's externally wired code) pin 19 of 9A goes low, causing pin 8 of flip-flop 10C to go high as AM+ (Address Mark). AM+ is sent to pin 3 of status port 6A to the 8X300 (as shown on page 2 of Figure 3-31).

When the 8X300 first sets the 80Z+ flag, it waits for the AM+ signal. It is possible, at this point in the read operation, that the 80Z+ and previous 16Z+ flags were both set by a long field of MFM 0s in a data field and not by a valid intersector gap. If so, eventually either an MFM 1 or (if the whole sector is nothing but MFM 0s) an A1h address mark from the next sector will appear. Therefore, the first MFM 1 clocked through shift register 8A to its pin 19 8Q output is coupled to pin 9 of gate 7A. If an address mark is not found, pin 10 of 7A is high, causing pin 8 to go low as CLRZ- (Clear Z). CLRZ- has

the same effect at pin 12 of gate 13C (shown on page 3 of Figure 3-31) as taking RDGATE+ low. That is, it causes the zero detector to reset, the 16Z+ flag to go low, and the phase detector to synchronize to the 10-MHz crystal oscillator. Since the 8X300 senses that the 16Z+ flag has gone low through pin 2 of status port 5A, the 8X300 reinitializes the read operation.

If an address mark is detected at 9A, valid read data is forthcoming. When the 8X300 initially sets RDGATE+ high to enable the zero detector, pin 12 of gate 9C was high. Also, before the address mark is detected, the high pin 9 of 10C causes pin 13 of 9C to be high. The low at the pin 11 output of 9C propagates through pin 3 of gate 12D to load counter 12C in a certain pattern. Counter 12C stays preloaded until the address mark is detected. Pin 13 of 9C then goes low, causing counter 12C to begin its count. The preload is such that, when the pin 15 CO (Carry Out) output of 12C goes high to pin 12 of flip-flop 11C, a clock is generated exactly on a byte boundary of the incoming data stream. The outputs at pin 9 and 8, respectively, of 11C are BCLK+ and BCLK- (Byte Clock), and they pulse on every byte boundary.

Serializer/Deserializer. As shown on page 5 of Figure 3-31, NRZ data from pin 16 of shift register 8A is sent to pin 5 of multiplexer 6D and then to the pin 11 SI (Serial In) input of serializing/deserializing shift register 5D. During a read operation, WRTOP+ (Write Operation) is low at pins 2 and 3 of 5D, which keeps 5D's Y0-Y7 outputs enabled. Also, the signal that clocks NRZ data into 5D is derived from the VFO frequency; it is the ANDed result of WRTOP+ inverted at pin 2 of 11D and of RDCLK+ (Read Clock) at pins 9 and 10 of 6B. CCLK- (Cell Clock) appears at pin 8 of 16B and is sent to the pin 12 input of 5D.

The Y0-Y7 outputs from 5D correspond to the UD0-UD7 (User Data) inputs of input/output port 5C where UD7 is the least significant bit. The deserialized data byte is loaded into 5C by the low WRTOP+ through pin 2 of inverter 11D as a high to pin 2 of gate 7A and ANDed with a high transition of BCLK+ at pin 1 of 7A. The low pin 3 output of 7A is ANDed again with a low transition of RDCLK1- at pins 5 and 4 of gate

8G. The low at pin 6 of 8G is applied to the pin 10 BIC (Buffer Input Control) at 5C to load the byte.

At the same time that BCLK- makes a transition at a byte boundary, BCLK- clocks pin 3 of flip-flop 3E. The high at pin 5 of 3E is sent to pin 4 of the status port at 6A as REQ+ (Service Request). The 8X300 waits for this status line as soon as it detects the AM+ flag, since it means that a byte is available to read from the IV bus at 5C. The 8X300 immediately reads this byte from 5C and verifies that it is indeed the A1h address mark described above. The 8X300 then waits for the next byte in the disk sector's identification field, which is FEh, and again reads 5C as soon as the REQ+ flag is received. The 8X300 continues to read sector identification information bytes, such as head number, track number, and sector number.

Once the 8X300 reads the sector number, it reads two CRC bytes, both of which must be all 0s. The 8X300 sets CRCTIME+ and CRCRST+ (CRC Reset) high at pins 4 and 5 of flip-flop 4D. When 4D is clocked by BCLK- at pin 9 to enable the CRC generator, multiplexer 6D is switched to channel the CRC syndrome bits from pin 12 of 4E to deserializer 5D.

Write Circuitry. Write data to the hard disk drive is sent from the 8X300's IV bus to input/output port 5C and then to serializer/deserializer 5D when WRTOP+ is high. WRTOP+ is inverted at pin 2 of 11D and sent to the pin 9 BOC (Buffer Output Control) of 5C. The byte clock for the write operation is not derived from the VFO as it is in the read operation. Instead, WOSC+ (Write Oscillator) is a 5-MHz division of the 10-MHz crystal-generated reference oscillator and originates from pin 9 of flip-flop 14D (page 3 of Figure 3-31). WOSC+ is ANDed with WRTOP+ at pins 13 and 1 of AND/OR gate 16B. The CCLK- at pin 8 of 16B is sent to counter 12C and flip-flop 11C (page 4 of Figure 3-31) to generate BCLK+ and BCLK-. The write data is shifted out of the deserializer at 5D on its pin 17 SO (Serial Out) line, through pin 4 of multiplexer 6D as WRDAT+ (Write Data), and then to the pin 4 1D input of shift register 8D. The AND/OR gate at 9E examines some of the outputs of 8D, WOSC-, and WOSC2X+ (10-MHz Write

Oscillator). Pin 8 of 9E generates MFM data from these inputs and sends the data to pins 5 and 9 of gate 6E. The AND/OR gates at 7E and 8E examine a wider pattern of the bits shifted out of 8D; they form a history of bit patterns to determine when write precompensation can be applied. When pin 8 of 7E is low, the data bit is to be written early. If pin 8 of 8E is low, the data bit is to be written late. If both pins 8 of 7E and 8E are high, the data is to be written at the nominal time, that is, without write precompensation.

The MFM encoded data generated by 9E and applied to gate 6E are sent to pin 2 of delay line 7F, the three outputs of which are spaced in time at 12-ns intervals. Pin 6 of 7F represents a nominal delay, pin 3 represents a write delay 12 ns before the nominal, and pin 10 represents a write delay 12 ns later than nominal. The three outputs of the delay line 7F are applied to the inputs of AND/OR gate 8F along with inverted and noninverted outputs of AND/OR gates 7E and 8E. Pin 8 of 8F generates the MFM precompensated data bits, the bits propagate through gate 6E pin 3, and are then sent to the hard disk drive through differential driver 17B as WMF+ and WMF- (Write MFM Data).

Any time that a write operation is performed, a new gap and identification field are written for that sector. The 8X300 writes all of the gap and identification information except for the unique address mark described above. The 8X300 enables the writing of the address mark when it sets CRCRST+ at pin 5 of output port 5A. CRCRST+ is inverted at pin 2 of 7D to set pin 10 of flip-flop 13D. Pin 4 of shift register 9D is connected to the 4Q output of shift register 8D. Since the first nonzero information in the identification field is the address mark Alh (10100001), the first 1 bit to be detected clocks pin $\overline{11}$ of flip-flop 13D. The shift delay combination between the 8D and 9D shift registers is such that, when the 1 bit clocks 13D, it is at the same time that the second 0 from the right (note the underlined bit above) is at the output of AND/OR gate 8F. On the falling edge of the 1 bit, pin 13 of gate 6E goes high and inhibits the 0 bit, thus creating the address mark.

Data Buffer. As shown on page 6 of Figure 3-31, the data buffer on the left bank of the IV bus is composed of two 256-by-4-bit RAMs at 8B and 7B, and an address counter at 7C. When the 8X300 reads data, it must move the data into the data buffer before the data are transferred to the CPU Board during a DMA operation. For each byte interval (1.6 μs), the 8X300 has to detect REQ+ (Request), generated by the byte clock, to determine when a byte is available to be read at input/output port 5C. The 8X300 must also move the byte into the data buffer, examine pin 6 of status register 6A to determine if the data buffer is full (pin 8 of gate 9B); and if it is not, the 8X300 must increment the data buffer address, reset the REQ+ flag and wait for REQ+ to set again. Since the 8X300 is not quite fast enough to handle all of the functions associated with the address buffer, an address counter is used to increment the data buffer address when it is being used.

The counter at 7C is initially cleared before a read operation by CRCRST+ at pins 2 and 12 of 7C. The address of the data buffer is incremented by selecting the left bank of the IV bus and asserting an erroneous address. Since the SC+ line from the 8X300 is high at this time, it is ANDed with a high RB- at pins 12 and 13 of 7A. The low pin 11 of 7A is inverted at pin 8 of 11D and sent to pin 9 of gate 9C where it is ANDed with CP+ (Clock from Processor), the master clock output of the 8X300. The pin 8 output of 9C then clocks counter 7A at pin 1 and increments the data buffer address.

During a write operation, the same events described above occur with the addition of a low BUFWR- (Buffer Write) every time a byte is written to the buffer. BUFWR- is the ANDed result of the 8X300 strobe WC (Write Command) and MCLK+ from pins 5 and 4 of gate 7A.

CRT DEFLECTION BOARD AND MONITOR

The video monitor in the AWS-220, -230, and -240 contains a 15-in CRT with a maximum picture size of 10.5 in by 7.75 in. The video monitor also houses the CRT Deflection Board, which converts four data and synchronization signals from the CPU Board into drive signals for the CRT. Deflection is by a noninterlaced raster scan at 50 or 60 Hz. The CRT Deflection Board consists of four major functional areas: the horizontal deflection circuits, high voltage and bias supply circuits, vertical deflection circuits, and video amplifier circuits.

The horizontal deflection circuits deflect the video beam across each of the scan lines of the CRT.

The high voltage and bias supply circuits generate bias voltages for various CRT electrodes.

The vertical deflection circuits deflect the beam vertically through the 330 scan lines on the CRT.

The video amplifier circuits supply the cathode of the CRT with video information from the CPU Board.

Figure 3-36 below shows the functional blocks of the CRT Deflection Board and monitor. Also see Figure 3-37 below, the CRT Deflection Board schematic, during the following discussion.

Horizontal Deflection Circuits

The workstation monitor has 330 scan lines, of which 319 are visible. The remaining 11 scan lines are blanked during vertical retrace. A scanning rate of 19.8 kHz is required at a noninterlaced refresh rate of 60 Hz. The peak current required to move the video beam horizontally across the face of the CRT is typically 4A.

The 19.8-kHz synchronization signal for the horizontal deflection circuits comes from the CPU Board as an RS-422 differential signal pair, HORDR+ and HORDR-. These are converted to a TTL synchronization signal at U2 pin 13 and then coupled to pin 10 of one-shot multivibrator U5.

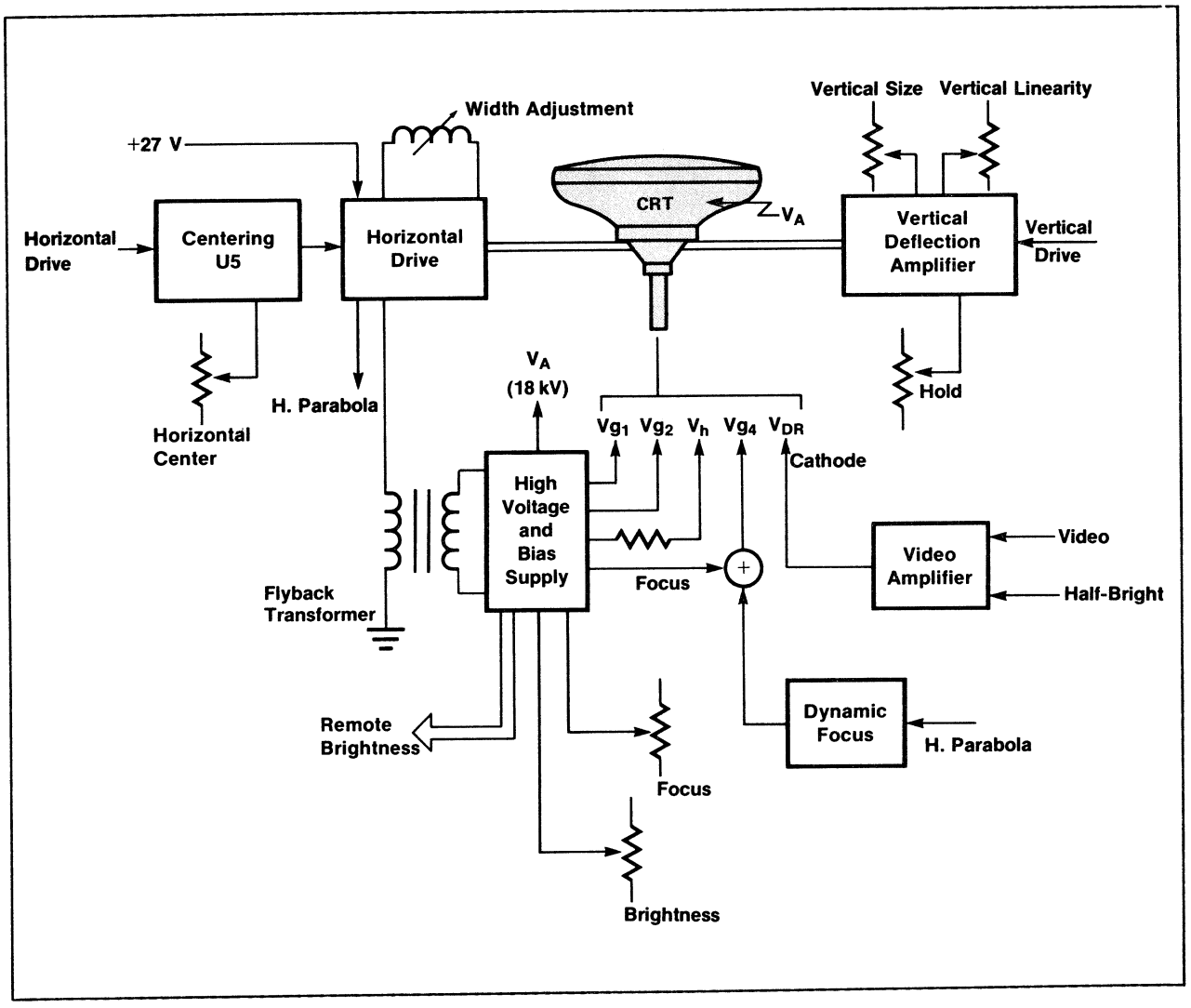

Figure 3-36. CRT Deflection Board and Monitor.

The RC network, consisting of R13, C7, and potentiometer R12 across pins 6 and 7 of U5, allows the horizontal synchronization signal to be delayed slightly for centering of the raster. The HORCTR (Horizontal Centering) potentiometer R12 controls the centering. The output of U5 pin 5 is sent to another one-shot at U5 to provide a 50 percent duty cycle of the synchronization signal required by transistor Q4.

Transistor Q4 drives the primary winding of transformer T1. T1 is the base drive transformer for Q5, the horizontal deflection switching transistor. It converts a low current, high

SPARE GATES		
TYPE	REF. DESIGNATOR(S)	QTY.
74S38	U3	2

REF. DESIGNATORS	
LAST USED	NOT USED
R67	R34 THRU R41
C40	C5,24
L4	L2
T2	
U6	U4
Q13	Q1,2,3,6,7,8,9
CR19	CR6,7,8
J8	J4
AA-1	

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL DEVICES ARE STANDARD 4+8, 7+14, 8+16, 10+20 GROUND AND POWER CONNECTIONS.

Figure 3-37. CRT Deflection Board Schematic.

voltage drive in its primary winding to a high current, low voltage supply in its secondary winding. The secondary winding of T1 causes a forced beta in Q5 as determined by the turns ratio between pins 4 and 3 and between pins 3 and 5, all of the secondary winding. The base and emitter of Q5 are connected between pins 3 and 4 of the secondary winding. The current from pin 5 of T1 represents the collector current of Q5. The forced beta in Q5 is therefore independent of the drive current to the horizontal yoke.

In the horizontal deflection circuit with Q5 are C13, as the flyback capacitor, and CR4, as the flyback diode. The 250-H horizontal yoke is ac-coupled to Q5 through C14, an S-correction capacitor that compensates for the curvature of the CRT face. C14 resonates with the yoke when Q5 is conducting.

Two adjustments are provided in series with the horizontal yoke. The WIDTH ADJ (Width Adjustment) inductor, L3, adds to the yoke's total inductance. L3 adjusts the voltage that appears across the yoke which, in turn, affects the peak current in the yoke at the end of a scan. L4's inductance is a function of yoke current. L4 has a permanent-magnet bias, which helps deliver a linear current slope to the yoke.

High Voltage and Bias Supply Circuits

Pin 4 of the T2 flyback transformer primary winding is supplied from the return path of the horizontal deflection circuits. The primary winding is wired with a technique that uses an autotransformer to increase the apparent voltage across the yoke during a CRT scan. The flyback transformer is, for ac purposes, connected in parallel with the horizontal yoke. Since the primary inductance of T2 is much higher than that of the yoke, most of the current flows through the yoke. However, enough current flows through the T2 primary winding to provide the bias supplies from the secondary circuit.

The secondary circuits of T2 supply the bias voltages for the CRT. Approximately 18 kV is supplied to the CRT anode. Aproximately 1.2 kV is supplied to the G2 brightness electrode at T2 pin 6. This secondary tap also supplies electrode G1, which is typically -20 V but can

become more negative through the REMOTE BRIGHTNESS potentiometer connected to J8 pins 1, 2, and 3. R46 and R48, in conjunction with CR12, R43, R44, and R45, set up the -20-V bias on G1 from the B+ supply.

B+ is also an output of the secondary of T2 at pin 9 and is approximately a 60-V dc supply. B+ is also used to supply the video amplifier, as discussed below.

Pin 8 of T2 is a 430-V dc output supplying a dynamic focus circuit that alters the focus voltage as a function of the horizontal beam position. The correction voltage is parabolic in nature and repeats at the 19.8-kHz horizontal scanning frequency. The parabolic correction waveform originates at the junction of C14 and L3 and is amplified by Q10. The resulting 250 to 300-V peak-to-peak signal is combined with a dc voltage from the R54 FOCUS potentiometer and sent to the CRT G4 electrode.

The two remaining outputs of the T2 flyback transformer supply a RMS heater voltage of 6.3 V ac through a 10-ohm, 2-W resistor, R50.

Vertical Deflection Circuits

The vertical deflection function of the CRT Deflection Board is primarily handled by an integrated circuit amplifier, U6. U6 is triggered from the positive edge of the differential signal pair VERDR+ and VERDR- and converted to a TTL level at pin 11 of U2. U6 creates a linear ramp current in the 15-mH vertical yoke synchronized to VERDR.

R42 senses current in the yoke. The current is determined by the feedback-biasing network composed of R28, R29, and R42, which forms the feedback for a current amplifier whose input is from pin 1 of U6. The other functions that U6 performs:

- supply a linear ramp voltage that can be applied to the input of the amplifier,
- control the amplitude of the ramp through the VER SIZE (Vertical Size) potentiometer at R24,

- control the linearity of the ramp through the VER LIN (Vertical Linearity) potentiometer R25, and

- set up the synchronization threshhold for U6 to the vertical drive signal through the VER HOLD (Vertical Hold) potentiometer at R21.

The rate of retrace is controlled by the voltage applied to the supply input of U6 at pin 5. CR9 and C6 allow the supply voltage of 27 V to be doubled to about 54 V at U6 pin 5 only during retrace. This results in twice the current in the vertical yoke, and thus in a retrace speed twice as fast as if only the 27-V supply were used.

Video Amplifier Circuits

The video amplifier provides a switching waveform to the CRT cathode. The waveform turns the video beam on and off at appropriate times to light pixels in each video display character cell.

The cathode is driven by transistor Q1 when the differential signal pair VIDEO+ and VIDEO- from the CPU Board are high at pin 3 of receiver U2. This causes gate U3 pins 11 and 3 to go low, which provides a path for current to flow through Q1, as determined by R6 and R7. About 25 to 28 V appear across load resistors R1, R2, and R3.

The differential signal pair HALFBRIGHT+ and HALFBRIGHT- at the pin 5 output of U2 allow the video signal to be displayed at about half-intensity. When the half-bright signal is active, pin 5 of U2 goes low, causing U3 pin 3 to go high, which isolates the current path from Q1 through R7. Therefore, with only R6 conducting, a lower voltage of 14 or 15 V appears across load resistors R1, R2, and R3.

CR1, CR2, R5, and AA-1 provide protection against arc-over from the anode of the CRT to the cathode. AA-1 is a neon lamp that turns on at about 100 V to dissipate much of the energy during arc-over. CR1 and CR2 clamp the voltage to ensure that the collector of Q1 never goes above 72 V.

Table 3-2 below lists the pin assignments of the connectors associated with the CRT Deflection

Board. The adjustment potentiometers on the board, along with a description of their functions, are listed in Table 3-3 below.

Table 3-2. CRT Deflection Board Connector Pin List. (Page 1 of 2)

Video Connector J1

Pin	Signal
1	+27 V
2	+27 V
3	GND
4	HORDR-
5	HORDR+
6	GND
7	No connection
8	GND
9	VIDEO+
10	VIDEO-
11	GND
12	HALFBRIGHT+
13	HALFBRIGHT-
14	No connection (PLUG)
15	GND
16	VERDR+
17	VERDR-
18	No connection
19	GND
20	No connection

Vertical and Horizontal Yoke Connectors J2, J3

Pin	Signal
J2-1	VERTICAL YOKE (Low)
J2-2	VERTICAL YOKE (High)
J3-1	HORIZONTAL YOKE (High)
J3-2	HORIZONTAL YOKE (Low)

Table 3-2. CRT Deflection Board Connector Pin List. (Page 2 of 2)

CRT Connectors J5 and J6

Pin	Signal
J5-1	G4 (Focus)
J5-2	No connection
J5-3	G2 (Brightness)
J5-4	No connection
J5-5	G1
J6-1	HEATER (High)
J6-2	HEATER (Low)
J6-3	CATHODE

Remote Brightness Connector J8

Pin	Signal
1	REMOTE BRIGHTNESS (High)
2	REMOTE BRIGHTNESS (Adjust)
3	REMOTE BRIGHTNESS (Ground)

Table 3-3. CRT Deflection Board Potentiometers.

Name	Function
BRIGHTNESS	An externally accessible thumbwheel control that controls the brightness of the video display. Located on the bottom left edge of the video display caseworks.
VER SIZE	Adjusts the height of the raster.
VER LIN	Adjusts the vertical linearity, that is, the separation between horizontal lines.
FOCUS	Adjusts the focus at the center of the screen.
WIDTH ADJ	Adjusts the width of the raster.
G2	Adjusts brightness. This control should be set with the BRIGHTNESS control at maximum to set the maximum brightness level.
HORCTR	Adjusts the horizontal position of the picture within the raster.
V HOLD	Adjusts the center frequency of the vertical deflection amplifier to ensure reliable locking of the VERDR synchronization signal.
LINEARITY ADJ	Adjusts the horizontal linearity, that is, the separation between the vertical lines on the video display.

KEYBOARD

The keyboard logic uses an 8048 microcomputer to communicate with Channel B of the 7201 on the CPU Board. The 8048 contains an on-chip ROM that stores the codes for keyboard communications. The 8048 can either send data to the 7201, indicating which of the 98 keys on the keyboard are pressed, or else receive data from the 7201, indicating which of the eight LED indicators on the keyboard to light. During the following circuit description, refer to Figure 3-38 below, the keyboard schematic.

The 8048 at DS4 scans the keyboard by generating a series of row addresses (pins 21-24) and by monitoring the state of the column lines (pins 27-34). Chip IC6 demultiplexes the row addresses and drives the corresponding row lines in the keyboard array.

The eight LED indicators are operated from the 8048's data lines DB0+-DB7+ through five inverters in IC2 and three NAND gates, each with one of the two inputs tied to +5 V dc.

Crystal Y36 and the program in the 8048's ROM determine the baud rate of keyboard communications, which is 1221 baud, the same as that of Channel B of the 7201 on the CPU Board.

DATAIN- from the CPU Board is buffered by a Schmitt-trigger inverter at IC1 pin 2 and then sent to DS4 pin 6. DATAOUT- to the CPU Board originates at DS4 pin 27 and is buffered through open-collector TTL gate IC3 pin 6, which has an external 1-kilohm pullup resistor. RESET- from the CPU Board is buffered twice by Schmitt-trigger inverters 1C pins 4 and 6 and then delivered to DS4 pin 4.

Tables 3-3 through 3-5 list the keyboard's ac and dc characteristics, key codes, connector pin assignments, LED indicators, and 8048 test points.

Table 3-4. Keyboard AC and DC Characteristics.

Signal/Parameter	Conditions	Minimum (mA)	Maximum (mA)
RESET-/Iil	Vi = 0.5 V	----	2.54
RESET-/Iih	Vi = 2.5 V	----	0.00
DATAIN-/Iil	Vi = 0.5 V	----	14.60
DATAIN-/Iih	Vi = 2.5 V	----	0.00
DATAOUT-, Iol	Vo = 0.5 V	4.35	-----
DATAOUT-, Ioh	Vo = 2.5 V	2.50	-----
Power Supply Current	V+ = +5.0 V	----	700.00

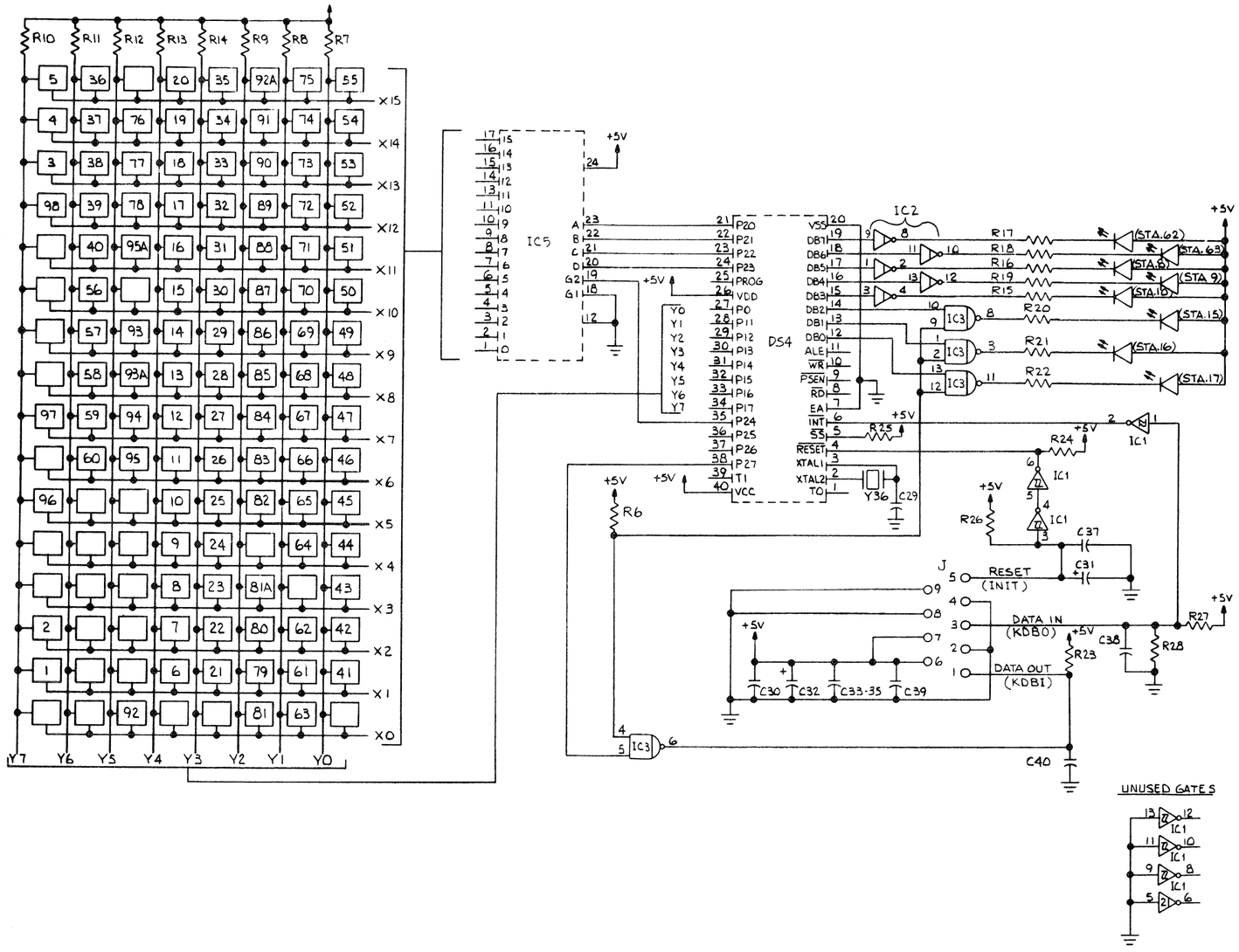

Figure 3-38. Keyboard Schematic.

Table 3-5. Keyboard Codes. (Page 1 of 2)

Keyboard Code (hexadecimal)	Key
00	HELP
01	up arrow
02	MARK
03	BOUND
04	FINISH
05	PREV PAGE
06	1/2
07	CANCEL
08	BACKSPACE
09	TAB
0A	RETURN
0B	down arrow
0C	NEXT PAGE
0D	NEXT
0E	left arrow
0F	right arrow
10	(SH-L')
11	SCROLL UP
12	MOVE
13	SCROLL DOWN
14	COPY
15	f1
16	f2
17	f3
18	f4
19	f5
1A	f6
1B	GO
1C	f7
1D	f8
1E	f9
1F	f10
20	space
21	number 9
22	(SH-R')
23	(0')
24	(NEXT')
25	unused code
26	unused code
27	' (single quote)
28	unused code
29	unused code

Table 3-5. Keyboard Codes. (Page 2 of 2)

Keyboard Code (hexadecimal)	Key
2A	unused code
2B	= (equals sign)
2C	, (comma)
2D	- (hyphen)
2E	. (period)
2F	/
30...39	numbers 0...9
3A	unused code
3B	;
3C	unused code
3D	unused code
3E	unused code
3F	invalid code
40	indicates the last key released; always has high bit on (that is, 0C0h)
41	number 6
42	number -
43	ACTION
44	OVERTYPE
46	number 2
47	number 3
48	left SHIFT
49	right SHIFT
4E...5A	unused codes
5B	[
5C	number 7
5D	]
5E	^ (caret)
5F	unused code
60	number 1
61...7A	a...z
7B	number 4
7C	number 8
7D	number 5
7E	unused code
7F	DELETE

Table 3-6. Keyboard Connector Pin Assignments.

Pin	Function
1	Data out
2, 4, 8, 9	Ground
6, 7	+5 V dc
5	Reset
3	Data in

Table 3-7. LED Indicators.

LED	Key	Legend
LED0	17	f10
LED1	16	f9
LED2	15	f8
LED3	10	f3
LED4	9	f2
LED5	8	f1
LED6	63	LOCK
LED7	62	OVERTYPE

Table 3-8. 8048 Test Points.

Point	8048 pin	Function
TP1	19	DB7
TP2	18	DB6
TP3	17	DB5
TP4	16	DB4
TP5	15	DB3
TP6	14	DB2
TP7	13	DB1
TP8	12	DB0

MOTHERBOARD

The Motherboard provides interconnecting lines for the various elements of the AWS-220, -230, and -240. The Motherboard is located horizontally at the bottom of the workstation card cage where the CPU and FDC or HDC Boards plug directly into the connectors supplied for them. The power supply, CRT Deflection Board, keyboard, speaker, reset switch, and power-on indicator plug into the Motherboard through wires or cables. At the rear of the AWS-220, -230, and -240 are the J1 and J2 connectors for cluster communications. J3, J4, and J5 provide connections for a parallel printer and two RS-232-C channels, A and B, respectively.

As shown in Figure 3-39 below, the Motherboard has 11 connectors of various types. P1 through P8 and P10 are plugs for interconnection of the internal elements of the workstation. Table 3-8 lists the connectors and their corresponding designations on the Motherboard.

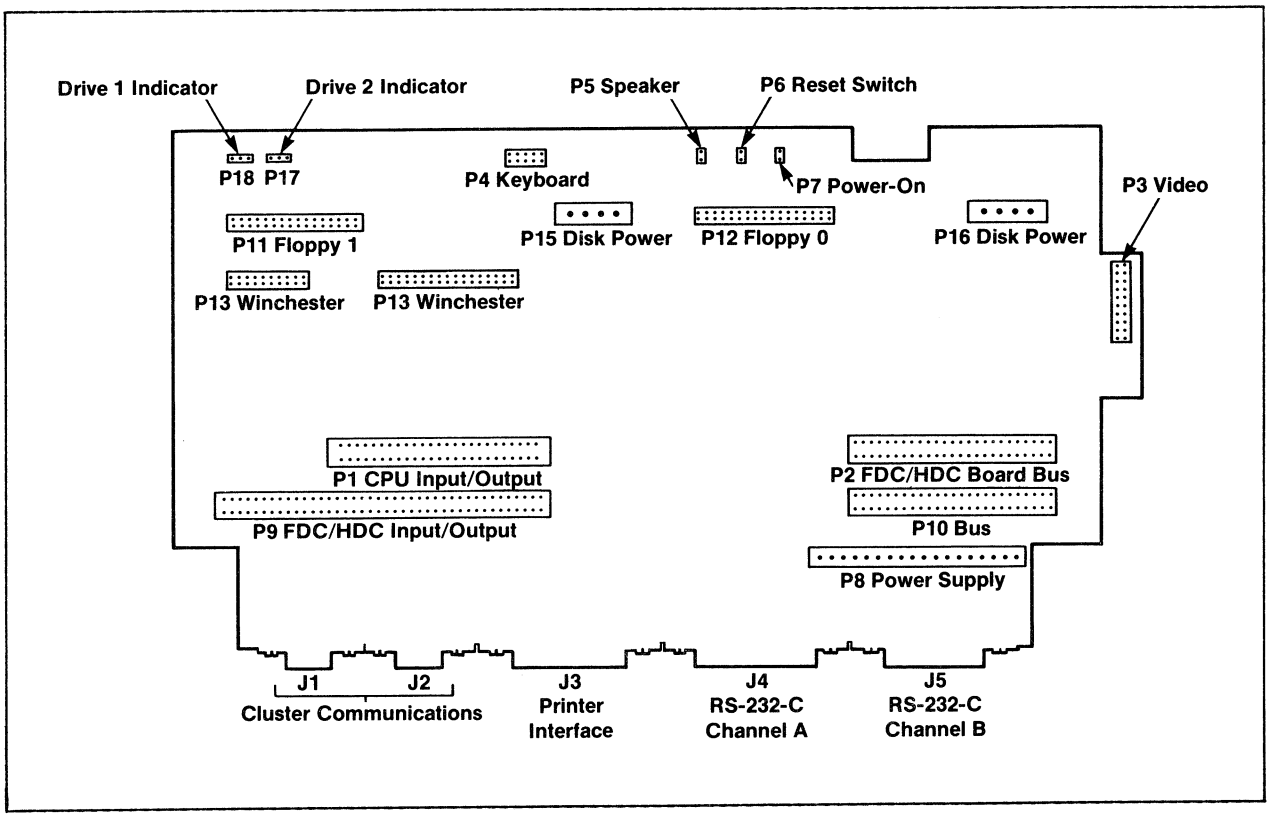

Figure 3-39. Motherboard Connector Locations.

Table 3-9 lists the pin assignments for cluster communications jacks J1 and J2, printer jack 3, and RS-232-C jacks J4 and J5. Table 3-10 is the Motherboard wire list for signals, and Table 3-11 is the wire list for power and grounds.

Table 3-9. Motherboard Connector Assignments.

Connector	Function
P1	CPU Board input/output
P2	FDC or HDC Board bus
P3	Video (to CRT Deflection Board)
P4	Keyboard
P5	Speaker
P6	Reset switch
P7	Power on lamp
P8	Power supply
P9	FDC or HDC input/output bus
P10	FDC or HDC bus
J1	Cluster communications (in)
J2	Cluster communications (out)
J3	Printer
J4	RS-232-C Channel A
J5	RS-232-C Channel B
P11	Floppy 1
P12	Floppy 0
P13	Winchester
P14	Winchester
P15	Disk power
P16	Disk power

Table 3-10. Connector Pin Assignments. (Page 1 of 2)

J1 and J2 Cluster Communications

Pin	Signal
1-5	Ground
6	RXC+
7	RXC-
8	RXD+
9	RXD-

Table 3-10. Connector Pin Assignments. (Page 2 of 2)

J3 Printer Interface

1	LPTØ +
2	LPT1 +
3	LPT2 +
4	LPT3 +
5	LPT4 +
6	LPT5 +
7	LPT6 +
8	LPT7 +
9	Ground (spare conductor)
10	Ground (spare conductor)
11	Ground (spare conductor)
12	Ground (spare conductor)
13	Ground (spare conductor)
14	STROBE-
15	Ground
16	LPTACK-
17	LPTBUSY+
21	NOPAPER+
22	SELECT+
23	Ground (spare conductor)
24	Ground (spare conductor)
25	Chassis Ground (shield)

J4 and J5 RS-232-C Communications Channels

1	Protective Ground (shield)
2	Transmit Data
3	Receive Data
4	Request To Send
5	Clear To Send
6	Data Set Ready
7	Signal Ground (Spare Conductor)
8	Carrier Detect
9	Ground (spare conductor)
14	Secondary Transmit Data
15	Transmit Clock
16	Secondary Receive Data
17	Receive Clock
20	Data Terminal Ready
22	Ring Indicator

Table 3-11. Motherboard Wire List for Signals.(Page 1 of 9)

Pin	Signal						
	9.8MHZ+	2SIDED-	ADRDIS-	AUDIO+	CTSA+	CTSB+	D0+
P1				8			
P2	2		18				7
P3							
P4							
P5				2			
P6							
P7							
P8							
P9		16			50	32	
P10	2		18				7
J1							
J2							
J3							
J4					5		
J5						5	
P11		32					
P12		32					
P13							
P14							
P15							
P16							

Pin	Signal									
	D1+	D2+	D3+	D4+	D5+	D6+	D7+	DCDA+	DCDB+	DIRECT-
P1										
P2	8	9	10	11	12	13	14			
P3										
P4										
P5										
P6										
P7										
P8										
P9								53	33	7
P10	8	9	10	11	12	13	14			
J1										
J2										
J3										
J4								8		
J5									8	
P11										18
P12										18
P13										
P14										34
P15										
P16										

Table 3-11. Motherboard Wire List for Signals. (Page 2 of 9)

Pin	Signal						
	DRIVED-	DRTYPE0-	DRTYPE1-	DS0-	DS1-	DSRA+	DSRB+
P1							
P2	22						
P3							
P4							
P5							
P6							
P7							
P8							
P9				19	8	51	31
P10	22	20	21				
J1							
J2							
J3						6	
J4							
J5							6
P11					10		
P12				10			
P13							
P14		30	32		28		
P15							
P16							

Pin	Signal					
	DTRA+	DTRB+	EXP1DC-	EXP2DC-	EXTACK+	EXTRQ+
P1						
P2			15	16	24	23
P3						
P4						
P5						
P6						
P7						
P8						
P9	52	34				
P10			15	16	24	23
J1						
J2						
J3						
J4	20					
J5		20				
P11						
P12						
P13						
P14						
P15						
P16						

Table 3-11. Motherboard Wire List for Signals. (Page 3 of 9)

Pin	Signal					
	HALFBRIGHT+	HALFBRIGHT-	HDSEL0-	HDSEL1-	HDSEL2-	HL0+
P1	27	28				
P2						
P3	12	13				
P4						
P5						
P6						
P7						
P8						
P9			17	12	73	22
P10						
J1						
J2						
J3						
J4						
J5						
P11						
P12						16
P13						
P14			14	18	4	
P15						
P16						

Pin	Signal							
	HL1+	HORDR+	HORDR-	INDEX-	INIT-	INTA-	INTR+	I/O+
P1		31	32		11		14	
P2						19		3
P3		5	4					
P4					5			
P5								
P6								
P7								
P8								
P9	20			11			14	
P10						19		3
J1								
J2								
J3								
J4								
J5								
P11	16			8				
P12				8				
P13								
P14				20				
P15								
P16								

Table 3-11. Motherboard Wire List for Signals. (Page 4 of 9)

Pin	Signal								
	IPI-	KBDI-	KBDO-	LA0+	LA1+	LA2+	LA3+	LA4+	LA5+
P1		10	9						
P2	25			29	30	31	32	34	36
P3									
P4		1	3						
P5									
P6									
P7									
P8									
P9									
P10	25			29	30	31	32	34	36
J1									
J2									
J3									
J4									
J5									
P11									
P12									
P13									
P14									
P15									
P16									

Pin	Signal								
	LA6+	LA7+	LA8+	LA9+	LA10+	LA11+	LA12+	LA13+	LAA+
P1									
P2	35	38	37	40	45	48	47	50	39
P3									
P4									
P5									
P6									
P7									
P8									
P9									
P10	35	38	37	40	45	48	47	50	39
J1									
J2									
J3									
J4									
J5									
P11									
P12									
P13									
P14									
P15									
P16									

Table 3-11. Motherboard Wire List for Signals. (Page 5 of 9)

Pin	Signal								
	LAB+	LAC+	LAD+	LAE+	LAF+	LPT0+	LPT1+	LPT2+	LPT3+
P1									
P2	42	41	44	43	46				
P3									
P4									
P5									
P6									
P7									
P8									
P9						63	56	57	58
P10	42	41	44	43	46				
J1									
J2									
J3						1	2	3	4
J4									
J5									
P11									
P12									
P13									
P14									
P15									
P16									

Pin	Signal						
	LPT4+	LPT5+	LPT6+	LPT7+	LPTACK-	LPTBUSY+	LPTNOPAPER+
P1							
P2							
P3							
P4							
P5							
P6							
P7							
P8							
P9	59	60	61	62	66	67	68
P10							
J1							
J2							
J3	5	6	7	8	16	17	21
J4							
J5							
P11							
P12							
P13							
P14							
P15							
P16							

Table 3-11. Motherboard Wire List for Signals. (Page 6 of 9)

Pin	Signal						
	LPTSELECT+	LPTSTROBE-	MFM+	MFM-	ONBDINT+	RD-	RDDATA-
P1					13		
P2						5	
P3							
P4							
P5							
P6							
P7							
P8							
P9	69	64	78	77	13		24
P10						5	
J1							
J2							
J3	22	14					
J4							
J5							
P11							30
P12							30
P13			17	18			
P14							
P15							
P16							

Pin	Signal						
	READY-	REDWC-	RESET+	RESETSW-	RINGA+	RINGB+	ROMSUP-
P1				7			
P2			4				28
P3							
P4							
P5							
P6							
P7							
P8							
P9	10	74			54	41	
P10			4				28
J1							
J2							
J3							
J4					22		
J5						22	
P11	34						
P12	34						
P13							
P14	22	2					
P15							
P16							

Table 3-11. Motherboard Wire List for Signals. (Page 7 of 9)

Pin	Signal								
	RTSA+	RTSB+	RXC+	RXC-	RXCA+	RXCB+	RXD+	RXD-	RXDA-
P1			21	23			17	19	
P2									
P3									
P4									
P5									
P6									
P7									
P8									
P9	48	30			49	29			47
P10									
J1			6	7			8	9	
J2			6	7			8	9	
J3									
J4	4				17				3
J5		4				17			
P11									
P12									
P13									
P14									
P15									
P16									

Pin	Signal							
	RXDB-	SIDED-	SKCOMPL-	STEP-	SRDA-	SRDB-	STDA-	STDB-
P1								
P2								
P3								
P4								
P5								
P6								
P7								
P8								
P9	27	16	71	9	42	36	43	26
P10								
J1								
J2								
J3								
J4					16		14	
J5	3					16		14
P11		4		20				
P12		4		20				
P13								
P14			8	24				
P15								
P16								

Table 3-11. Motherboard Wire List for Signals. (Page 8 of 9)

Pin	Signal								
	TC-	TRACK0-	TXC+	TXC-	TXCA+	TXCB+	TXD+	TXD-	TXDA-
P1			22*	24†			18**	20††	
P2	26								
P3									
P4									
P5									
P6									
P7									
P8									
P9		70			46	28			44
P10	26								
J1									
J2									
J3									
J4					15				2
J5						15			
P11		26							
P12		26							
P13									
P14		10							
P15									
P16									

*Trace-jumpered to RXC+; †Trace-jumpered to RXC-
**Trace-jumpered to RXC+ ††Trace-jumpered to RXD-

Pin	Signal							
	TXDB-	VERDR+	VERDR-	VIDEO+	VIDEO-	WAIT-	WMF+	WMF-
P1		29	30	33	34			
P2						27		
P3		16	17	9	10			
P4								
P5								
P6								
P7								
P8								
P9	23						80	79
P10						27		
J1								
J2								
J3								
J4								
J5	2							
P11								
P12								
P13							13	14
P14								
P15								
P16								

Table 3-11. Motherboard Wire List for Signals. (Page 9 of 9)

Pin	Signal			
	WR-	WRDATA-	WRGATE-	WRPROT-
P1				
P2	6			
P3				
P4				
P5				
P6				
P7				
P8				
P9		21	72	18
P10	6			
J1				
J2				
J3				
J4				
J5				
P11		22	24	28
P12		22	24	28
P13				
P14			6	12
P15				
P16				

Table 3-12. Motherboard Wire List for Power and Grounds. (Page 1 of 2)

Pin	Signal									
	+5V	+5V	+5V	+5V	+5V	+5V	+12V	+12V	-12V	-12V
P1	1	2	39	40			3	4	37	38
P2										
P3							20			
P4	6	7								
P5										
P6										
P7	2									
P8	1	2	3	7	10	18	5	6	8	
P9	1	2	39	40			3	4	37	38
P10										
J1										
J2										
J3										
J4										
J5										
P11										
P12										
P13										
P14										
P15										
P16										

Pin	Signal										
	+24V	+24V	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd
P1			5	6	15	16	25	26	35	36	
P2			1	17	33	49					
P3	1	2	3	6	8	11	15	19			
P4			2	4	8	9					
P5			1								
P6			1								
P7			1								
P8	12	24	4	9	11	13	15	17			
P9			5	15	25	35	45	55	65	76	
P10			1	17	33	49					
J1			1	2	3	4	5				
J2			1	2	3	4	5				
J3			9	10	11	12	15	25			
J4			1	7							
J5											
P11			1	3	5	7	9	11	13	15	17
P12			1	3	5	7	9	11	13	15	17
P13			2	4	6	8	10	11	12	15	16
P14			1	3	5	7	9	11	13	15	17
P15			2	3							
P16			2	3							

Table 3-12. Motherboard Wire List for Power and Grounds. (Page 2 of 2)

Pin	Signal							
	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd
P1								
P2								
P3								
P4								
P5								
P6								
P7								
P8								
P9								
P10								
J1								
J2								
J3								
J4								
J5								
P11	19	21	23	25	27	29	31	33
P12	19	21	23	25	27	29	31	33
P13	19	20						
P14	19	21	23	25	27	29	31	33
P15								
P16								

POWER SUPPLY

The power supply uses a 20-kHz switching regulator to generate four dc outputs:

Voltage	Tolerance	Maximum Output
+5 V dc	+ 2.0% to -2.0%	11.00 A
+27 V dc	+ 7.4% to -2.0%	1.25 A
+12 V dc	+10.0% to -10.0%	3.40 A
-12 V dc	+20.0% to -37.5%	0.20 A

The maximum power output of the power supply is 137 W. Short circuit protection is provided for all power supply outputs; over voltage protection is provided for the +5-V dc output at a maximum of 6.5 V dc.

Figure 3-40 below shows the power supply wiring. The power supply is factory wired to operate with a line voltage input of either 115 V ac or 230 V ac. It is not recommended that the user modify the power supply. The pin assignments for the power supply connectors are listed in Table 3-12 below.

The power supply can tolerate a line input frequency in a range of 47-440 Hz. The overall efficiency of the power supply exceeds 70 percent.

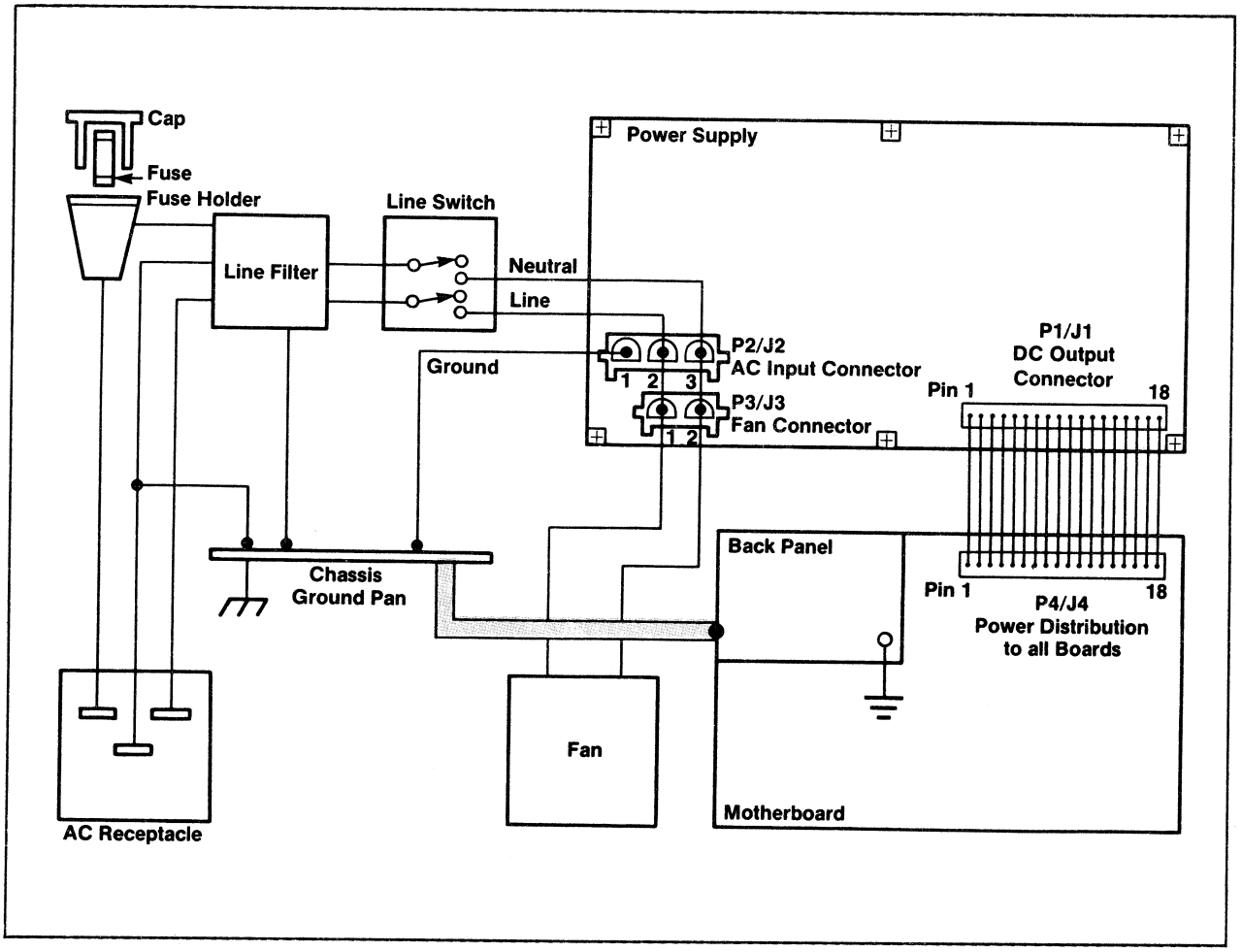

Figure 3-40. Power Supply Wiring.

Table 3-13. Power Supply Connector Pin Assignments.

J1 Pin	Signal
1	+5 V dc
2	+5 V dc
3	+5 V dc
4	Ground
5	+12 V dc
6	+12 V dc
7	+5 V dc
8	-12 V dc
9	Ground
10	+5 V dc
11	Ground
12	+27 V dc
13	Ground
14	+24 V dc
15	Ground
16	Unused
17	Ground
18	+5 V dc

J2 Pin	Signal
1	Ground
2	Line
3	Neutral

J3 Pin	Signal
1	Line
2	Neutral

CASEWORKS

The caseworks of the AWS-220, -230, and -240 consist of the base, lectern, video display, and keyboard. This section describes the location and function of the console switches and the controls and adjustment of the tilt-and-swivel feature of the video display.

Console Controls

The console control set includes power-on and reset switches, the power-on indicator, fuses, and the video display brightness control. As shown in Figure 3-41 below, the only front panel control is the power switch, which has a built-in power-on indicator. The reset switch is accessible from the back panel, next to the power cord input. Also next to the power cord input, on the opposite side, is the fuse holder. The thumbwheel video display brightness control is accessible from under the lower left corner of the video display.

Adjusting the Tilt and Swivel of the Video Display

The tilt and swivel of the video display are preset at the factory. If excessive free play is evident, the video display is tightened by turning the knurled knob under the workstation base. If tension is not kept on the swivel joint at all times, the bearing surfaces can unseat.

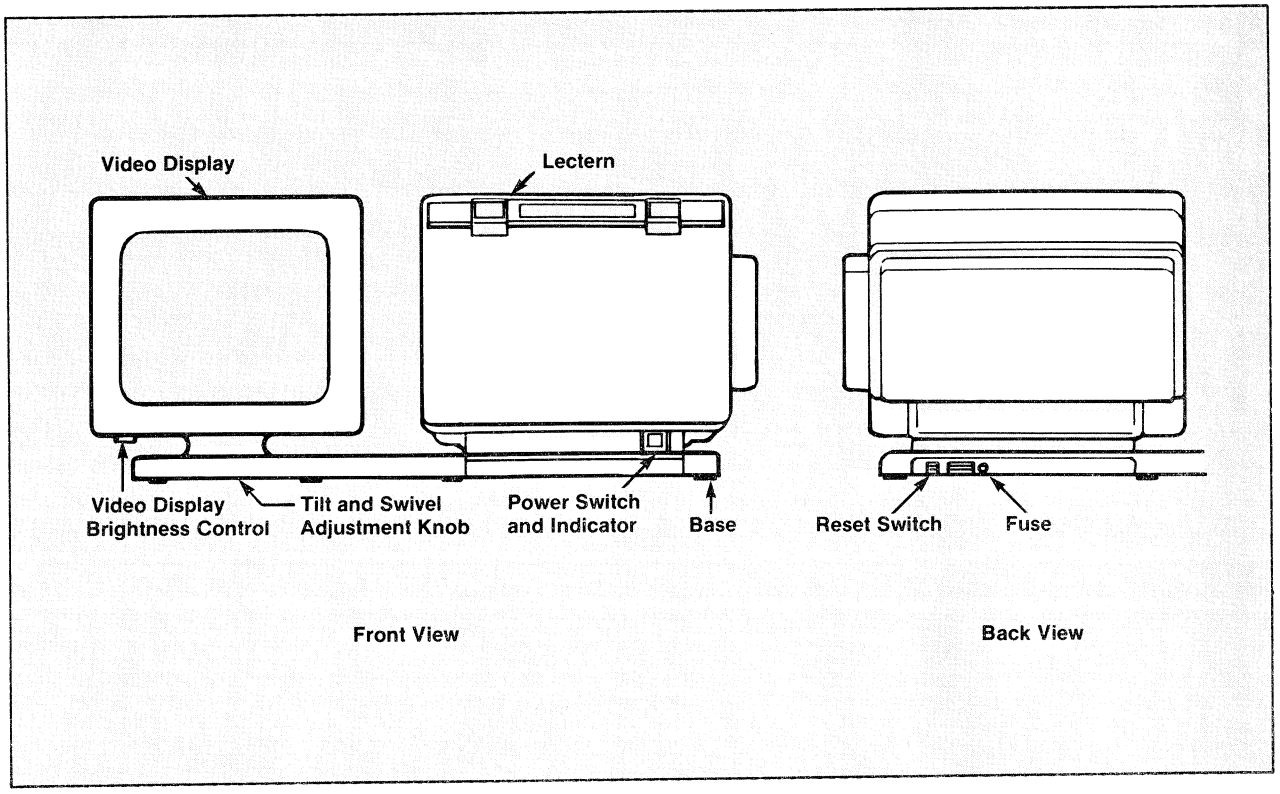

Figure 3-41. Workstation Layout and Controls.

USER'S COMMENT SHEET

AWS-220, -230, -240 Hardware Manual
EW-220 Volume 1: A-09-00111-01-A

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