CODATA SYSTEMS CORPORATION

# Winchester Disk Controller Hardware Reference Manual

# WINCHESTER DISK CONTROLLER

## DESCRIPTION, OPERATION AND MAINTENANCE

CONTENTS



ILLUSTRATIONS





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## 1. GENERAL

1.01 This manual provides a physical and functional description and operating theory for effective field maintenance of the Codata Systems Winchester Disk Controller (WDC) 92-1011-xx.

1.02 This Controller is supplied as a single printed circuit assembly (PCA) for use as a system component in Codata Systems Corp.:

(1) CTS—Series Mainframes,

(2) CTW—Series Mainframes.

### Features

1.03 The Controller utilizes a microprocessor ($\mu$P) in an intelligent controller design providing for mass storage on either 8.0-inch or 5.25-inch Winchester disks in an easy to use command/status structure. Blocking/deblocking, bad sector detection/reassignment and retry on error are performed by the WDC firmware minimizing system software complexity. WDC features include:

- IEEE 796 microcomputer bus compatible.
- The entire WDC is on a single PCA.
- Controls up to four Winchester Disk Drives.
- Supports full 20-bit 796 Bus address for command blocks and data transfers.
- Retry on error automatically performed by the WDC firmware.
- Data transfers to Mainframe RAM through direct memory access (DMA) 8-bit or 16-bit word transfers program selectable.
- Bad sector detection/alternate sector reassignment performed by the Controller firmware.
- Blocking/deblocking from logical sectors to blocks of 4096 bytes performed in the WDC firmware providing ease of implementation with operating systems such as CP/M(TM), MP/M(TM), UNIX(TM) and MERLIN(TM) while maintaining fast system access times.
- Convenient logical sector size of 128 bytes.
- Contiguous sector transfers up to 4096 bytes long may be performed which eliminates the need to interleave sectors to obtain high system through put.
- Byte count as high as 64k, 16-bit, is allowed.
- MFM data separation and write precompensation is provided by the WDC.
- Device address and interrupt level set with option jumpers.

**NOTE**

*The following reference notations apply in this technical manual.*

*(1) A * suffix to a signal name indicates logical NOT and active low.*

*(2) In and out references are in respect to CPU or bus master.*

*(3) 1k byte equals 1,024 bytes, i.e., 64k bytes equals 65,536 bytes.*

*(4) Codata Systems Corp. part numbers are made up of eight digits, e.g., the part number of this manual is 05-0003-01.*

*(5) A suffix -xx to a part number indicates the part or assembly may have more than one configuration in production, i.e., Winchester Disk Controller is 92-1011-xx.*

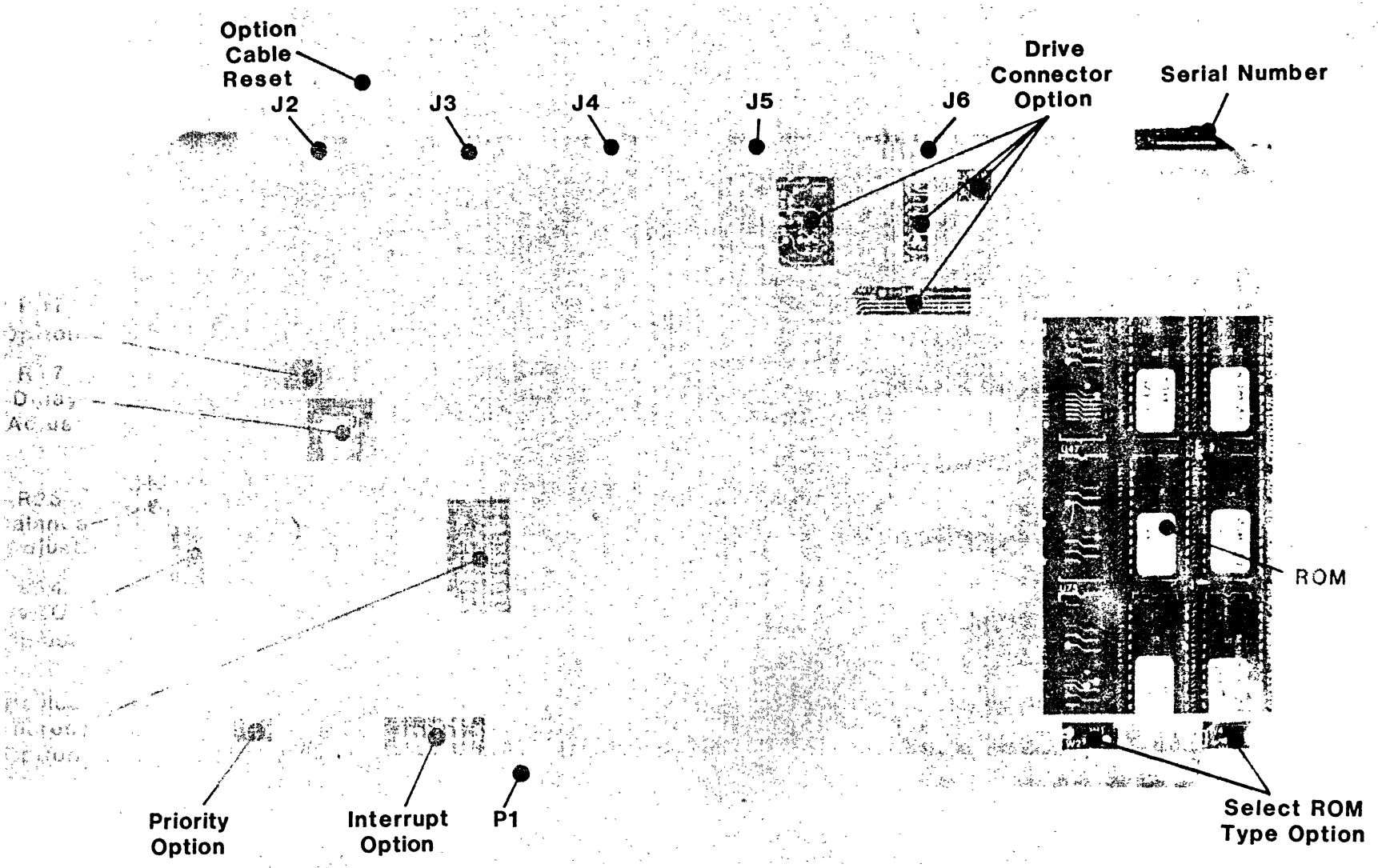



Figure 2-1 — Winchester Disk Controller — 92-1011-xx

## 2. PHYSICAL DESCRIPTION

2.01 The Winchester Disk Controller (WDC) 92-1011-xx is an integrated system component incorporating all the necessary component parts to provide the Mainframe with a single PCA Controller. Figure 2-1 illustrates the WDC. The PCA contains:

(1) A $\mu$P section. A dedicated 8-bit $\mu$P designed specifically for control applications,

(2) A memory section for storage of the control program and variables,

(3) 796 Bus Interface section to provide for bus arbitration,

(4) Control and Status Register section,

(5) Read and Write section,

(6) Phase-Locked Data Recovery section.

2.02 The PCA measures 6.0 inches by 12.0 inches. A pair of edge-type PC connectors, P1 and P2, mate with the 796 Bus backplane connectors.

(1) P1 is a dual 43-position, 86-conductor PC connector. The pin assignments conform to the 796 Bus specifications.

(2) P2 is a dual 30-position, 60-conductor PC connector. The pins are vacant and are not used by the bus.

2.03 Five edge-type PC connectors, J2 through J6, provide for the data control and status to control up to four drives.

(1) J2 through J5 are dual 10-position, 20-conductor PC connectors. These provide for the data communication between the WDC and each drive. A separate cable is connected to each drive, i.e., star connection.

(2) J6 is a dual 25-position, 50-conductor PC connector. This provides for the status and control signals between the WDC and Drives. A single cable is connected to each drive, i.e., daisy chain connection.

### Options

2.04 Several alternate features can be configured through option jumpers on the PCA. Refer to Figure 2-1.

(1) W1 through W8 select the ROM type when WDC is optioned for ROM.

(2) W9 through W18 configures the disk drive connectors for 8.0-inch or 5.25-inch drive signal locations.

(3) W19 through W26 select the interrupt level for WDC.

(4) W27 through W28 select WDC for 8- or 16-bit data transfers.

(5) W29 through W44 set the I/O port address. Normally this is 90-97H.

(6) W45 sets WDC to highest bus master priority.

(7) W46 and W47 set the INIT* for master or slave operation.

### Adjustments

2.05 Three multi-turn trim potentiometers are provided for adjustments in the analog sections:

(1) R17 sets the delay for the Synch Field Detector.

(2) R23 balances the VCO Error Amplifier.

(3) R34 adjusts the VCO frequency.

Refer to Figure 2-1 for the locations of these adjustments.

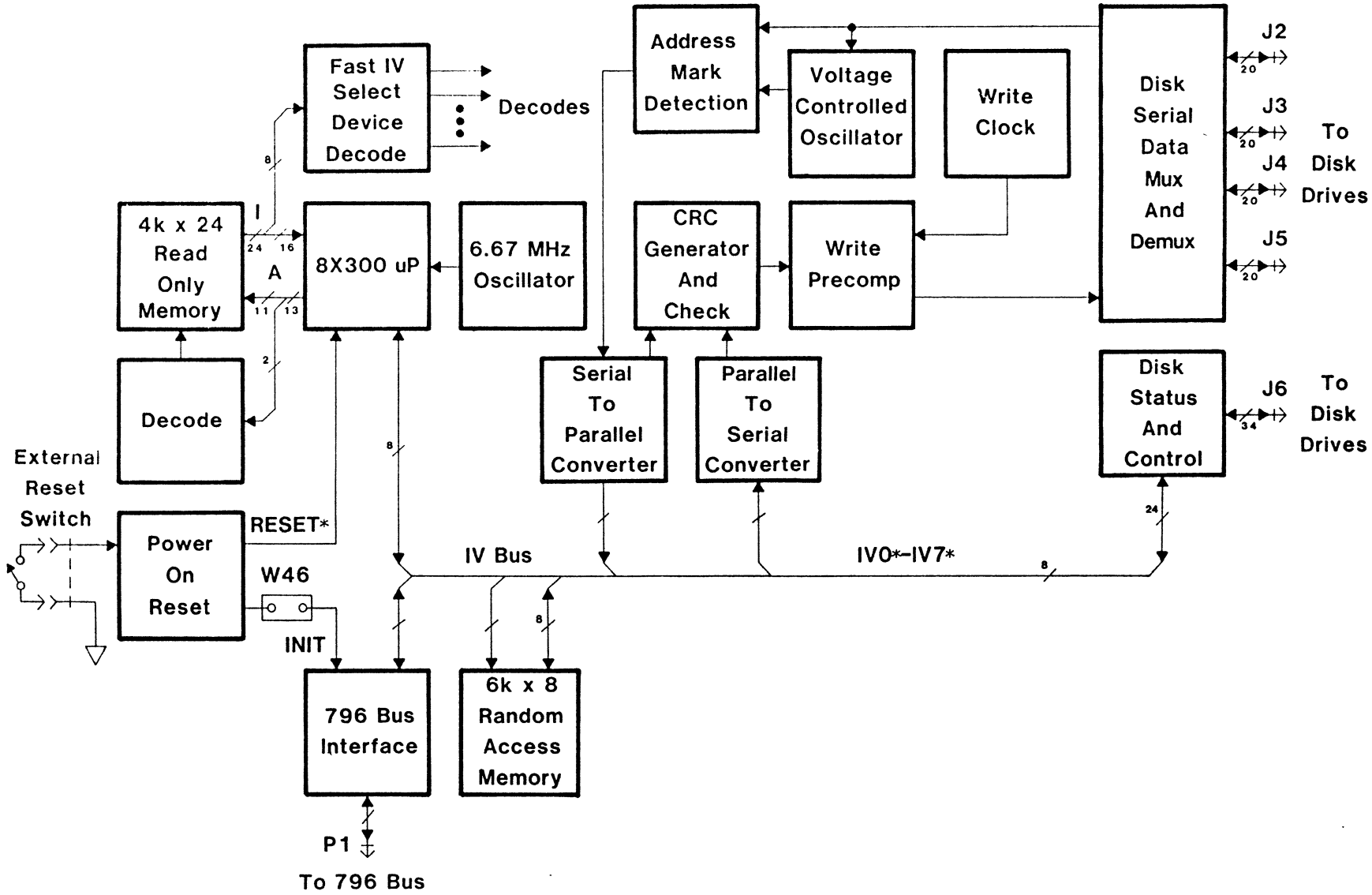



Figure 3-1 — Winchester Disk Controller Block Diagram

## 3. FUNCTIONAL DESCRIPTION

3.01 The basic function of a disk drive controller is to provide dedicated electronics for control and positioning of the drive read/write head(s) and the logic for read/write operations.

### Disk Storage

3.02 The Winchester Disk Controller (WDC) stores random access data and program files on two non-removable 5.25-inch disks. Each of these disk surfaces employs one movable head to service 153 data tracks. The media is made up of a rigid aluminum disk substrate coated on both sides with ferrous oxide similar to that found on audio tape. Read/write head(s) do not come into physical contact with the media.

3.03 Low cost and high drive reliability are achieved through the use of a band actuator and an open loop stepper motor positioned head. Refer to the OEM Disk Drive Technical Manual for a detailed functional description.

3.04 Formatting the disk divides the media read/write area into logically numbered tracks. Individual tracks are further subdivided into logical sectors. Each sector is 128 Bytes with 38,144 sectors per drive. Sector locations are determined logically and termed *Soft Sectored.* Information is stored on both surfaces of the disk(s). A single disk index position is monitored by the drive status logic. This logic issues an INDEX* pulse to the WDC each time the disk starts a new revolution. The computer Operating System uses the logical sector location and the indexing information to randomly access the stored files.

### Overview

3.05 Figure 3-1 illustrates the principal sections of the WDC in block diagram. This figure and Figures 3-2 through 3-6 should be used in conjunction with the WDC logic diagram for the descriptions which follow.

3.06 Direct Memory Access (DMA) operation is performed by the WDC or Bus Master, as well as, Bus slave operation through the use of a unique device; a 8X300 microprocessor ($\mu$P). This *8-Bit $\mu$P* is designed for fast control applications, such as, disk controllers. It has a limited instruction set of eight instruction types.

3.07 A *6.67 MHz* oscillator clocks the $\mu$P resulting in a 300 ns instruction cycle time.

3.08 A firmware control program is stored in the *4k x 24 ROM.* Thirteen $\mu$P lines address this ROM and its associated *Decode* device. A 16-Bit instruction is returned to the $\mu$P and an additional 8-Bits are appended to the instruction used by the *Fast IV Select Decode* for direct I/O addressing.

3.09 Both the source device, first 4 bits, and the destination device, remaining 4 bits, are specified in the 8 bit word furnished to the *Fast IV Select Decode* for data to be transferred over the 8-bit bi-directional IV Bus, IV0*-IV7*. Table 3-1 lists the decoded signals by their functions. This method of device addressing permits greatly increase system speed over conventional $\mu$P design since conventional I/O addressing requires individual instructions.

3.10 The 8X300 $\mu$P can address a source device, have that device place data on the IV Bus, and this data can then be taken into the $\mu$P all in the first half cycle or 150 ns. Data can be processed by an arithematic function included in the instruction read from ROM and the result placed back on the IV Bus targeted for storage in another device during the second half cycle.

3.11 A RESET* issued from *Power-On-Reset* causes the $\mu$P to initialize. Activation of the *Power-On-Reset* can be through these channels.

(1) Application of power to the +5 Vdc Bus.

(2) An INIT* received from the 796 Bus. Optionally, a INIT* can be issued to the 796 Bus.

3.12 I/O information can be transferred over the IV Bus between any of the WDC devices with or without passing through the $\mu$P.

(1) *6k x 8 Random Access Memory* — WDC status and control variables are stored in RAM, e.g., data transferred to or from the 796 Bus.

(2) *796 Bus Interface* — this device handles 796 Bus arbitration.

Table 3-1 – Fast IV Select Decode Signals

| Mnemonic | Function |
|---|---|
| LMBAM* | Load 796 Bus Address Middle, A8-AF. |
| LMBAH* | Load 796 Bus Address High, A10-A13. |
| LRAMAL* | Load RAM Address Low, RA0-RA7. |
| LRAMAH* | Load RAM Address High, RA8-RA10 and CE0-CE3. |
| LDCNL* | Load Disk Control Register. |
| LMUX* | Load Multiplexer. |
| LMBD* | Load 796 Bus Data, DB0-DB7 or DB8-DB15. |
| LFCNL* | Load Function Control Register. |
| LDSKDAT* | Load Disk Data Register. |
| LRAM* | Load RAM Data Register. |
| PTIMER* | Pulse Timeout Timer. |
| PMBACK* | Pulse 796 Bus Acknowledge. |
| MBRD* | Pulse 796 Bus Read Request Flip Flop. |
| PCIDX* | Pulse Clear Index Flip Flop. |
| RMBCMD* | Read 796 Bus Command Register. |
| RRAM* | Read RAM Data Register. |
| RMUX* | Read Mux. |
| RMBD* | Read 796 Bus Data Register. |
| RFCNTL* | Read Function Control Register. |
| RDSKDAT* | Read Disk Data Register. |

(3) *Read and Write Logic* — data is transferred between the IV Bus and disk drive(s).

(4) *Disk Status and Control* — contains disk status buffers and control registers.

(5) *Interrupt* — provides for setting WDC interrupt level.

3.13 The on-card *6k x 8 RAM* stores control variables and data. Addressing of this memory is controlled by external registers in the form of counters. The μP loads these initially with the device decoder.

3.14 The WDC has both 796 Bus Master or slave device attributes.

(1) As a master device the WDC generates requests to the *796 Bus Interface* for storing and receiving data in other 796 Bus devices.

(2) As a slave device, other 796 Bus Master devices, e.g. CPU, can address the WDC.

The on-card RAM is not accessable by 796 Bus devices.

3.15 The most complex portion of the WDC is the Read and Write Logic. Complexity is greatly reduced through the use of a five device set which performs the functions:

(1) The *Address Mark Detection* is used by the WDC to find an ID address mark or data address mark in the serial data stream.

(2) The *Serial to Parallel and Parallel to Serial Converters* are shift registers used to convert serial data to the parallel IV Bus.

(3) Write serial data has a CRC word calculated and appended for each block of data as it is written to the disk. A check of this CRC word is made for each block of data read. Both of these operations are performed by the *CRC Generation and Check*.

(4) *Write Precompensation* is performed to data depending on the disk location which the data is to be written. An individual recording transition is either made slightly early or late to compensate for bit crowding on the disk. The write data passes through a multiplexer associated with a delay line to provide the actual compensation in time. Individual line drivers are used to supply write data to up to four drives due to the high data rate of 5 MHz.

(5) The *Voltage Controlled Oscillator* is used to develop the read clock. It is referenced to the VCO center frequency when reading is inactive.

3.16 The WDC can generate interrupts to the 796 Bus on any of the eight 796 Bus levels, INT0*-INT7*, through option jumpers. An interrupt is used to tell the 796 Bus an WDC operation is completed.

**Memory**

3.17 Refer to Figure 3-2 for the description which follows. The contents of the *6k x 8 Random Access Memory* is exchanged as data to the IV Bus, IV0*-IV7*, with one of two instructions:

(1) LRAM* — Load RAM Data Register,

(2) RRAM* — Read RAM Data Register.

3.18 The starting *RAM* address is stored in a counter and a register from the IV Bus with the commands LRAMAL* and LRAMAH* issued by the control program.

(1) The *Low RAM Counter* stores the least significant 8 bits.

(2) The *High RAM Register* stores the most significant 3 bits and the chip enables for individual 2k RAM devices.

Both of these form the 11-bit RAM Address Bus, RA0-RA10. This method of addressing provides for performing block data exchanges with memory using a single instruction once the control program initializes them. The *Address Counter* is incremented at the completion of each read, RRAM*, or write, LRAM*, operation. This auto-incrementing feature permits very fast data transfers.

3.19 The *High RAM Address Register* is reloaded, LRAMH*, by the control program when a boundary is crossed, e.g., when the 8-bit *Low RAM Counter* might overflow. Individual memory device selects, CE0*-CE3*, are generated

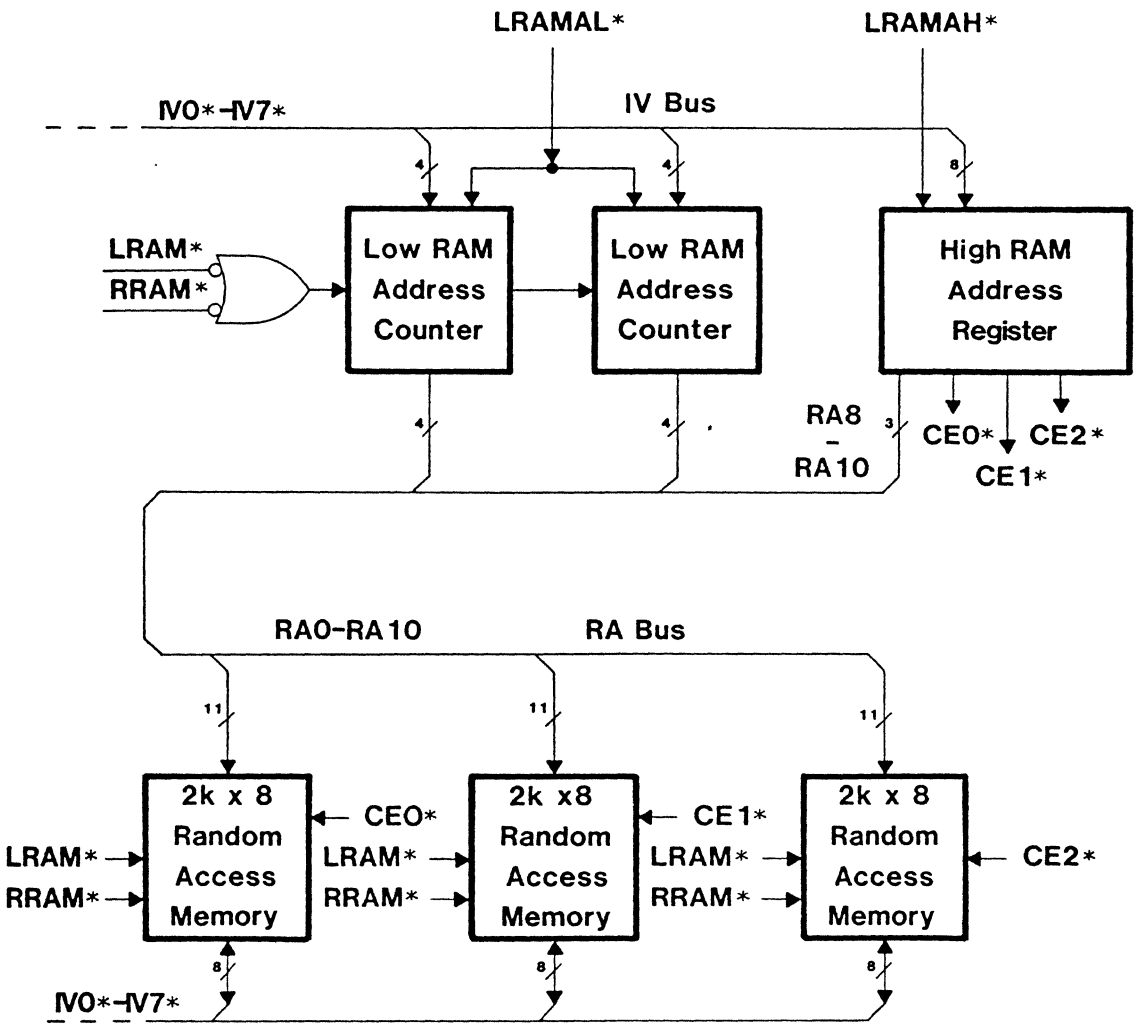



Figure 3-2 – Memory Block Diagram

by the remaining portion of the *Address Register* eliminating the need for an individual device decoder.

**796 Bus Interface**

3.20 Refer to Figure 3-3 for the description which follows. The 796 Bus Interface is made up of two subsections.

(1) Data and address registers which communicate with the 796 Address Bus, AD0*-AD13*, and 796 Data Bus, DAT0*-DATF*.

(2) Control signals and logic for timing data transfers with the 796 Bus.

3.21 Signal ADEN* from the *796 Bus Control Logic* gates the *796 Address 0-7, 8-F, and 10-13* registers on to the 796 Bus. The *796 Address* registers are loaded from the IV Bus, IV0*-IV7*. Fast IV device decodes are supplied to load each register.

(1) LMBAM* to *796 Bus 8-F* register,

(2) LMBAH* to *796 Bus 10-13* register,

(3) PMBRD* or PMBWR* to *796 Bus Address 0-7* register.

Each time read or write request, PMBRD* or PMBWR*, is made to the *796 Bus Control Logic* the least significant bits of the address are loaded into the $\mu$P.

3.22 The $\mu$P monitors the 796 Address Bus, ADR0-ADR2, and IOWRDEC during I/O cycles through the *796 Bus Command Gate*, if the WDC is idle, the $\mu$P checks IOWRDEC. If set, ADR0-ADR3, are checked to determine what to do with the data presented on the 796 Data Bus. It will interpret this as:

(1) The least significant 8 bits of a Command Block Pointer.

(2) The next 8 bits of a Command Block Pointer.

(3) The most significant 8 bits of a Command Block Pointer.

This operation performs the function of an address decoder normally performed by firmware. After this is stored in a $\mu$P register, an external acknowledge, XACK* is issued completing the 796 I/O cycle. Typically this cycle will be 1.5 $\mu$s, because of the fast $\mu$P response time.

3.23 796 Bus address lines, ADR3* through ADF*, are input to *Address Decode* and compared to the *Address Option Jumper* thereby determining the unique 796 Bus device I/O address. The *8 or 16-bit Option Jumper* determines the address length. The address option jumpers apply to A4-A7 and A8-AF. For example, if the desired address for 8-bit addressing is 90H, the same strapping would make the 16-bit address 9090H.

3.24 The output of the *Address Decoder(s)* is a device select to *Input Output Control* created from:

(1) 796 Bus I/O Write, IOWC*, or I/O Read, IORC*.

(2) A comparison between the address presented on the 796 Bus and the unique WDC address.

3.25 *Input Output Control* performs two functions.

(1) On an I/O Read, and I/O Read Decode, IORDDEC, is issued to the *Busy Interrupt Status*.

(2) On an I/O Write, and I/O Write Decode, IOWDEC, is issued to the *796 Bus Command Gate*.

3.26 The WDC data register is made up of four 8-bit registers.

(1) *796 Bus Data Input 0-7*.

(2) *796 Bus Data Input 8-F*.

The 796 Data Bus is connected to the register inputs and the IV Bus is connected to the register outputs.

(3) *796 Bus Data Output 0-7*.

(4) *796 Bus Data Output 8-F*.

The IV Bus is connected to the register inputs and the 796 Bus is connected to the register outputs.

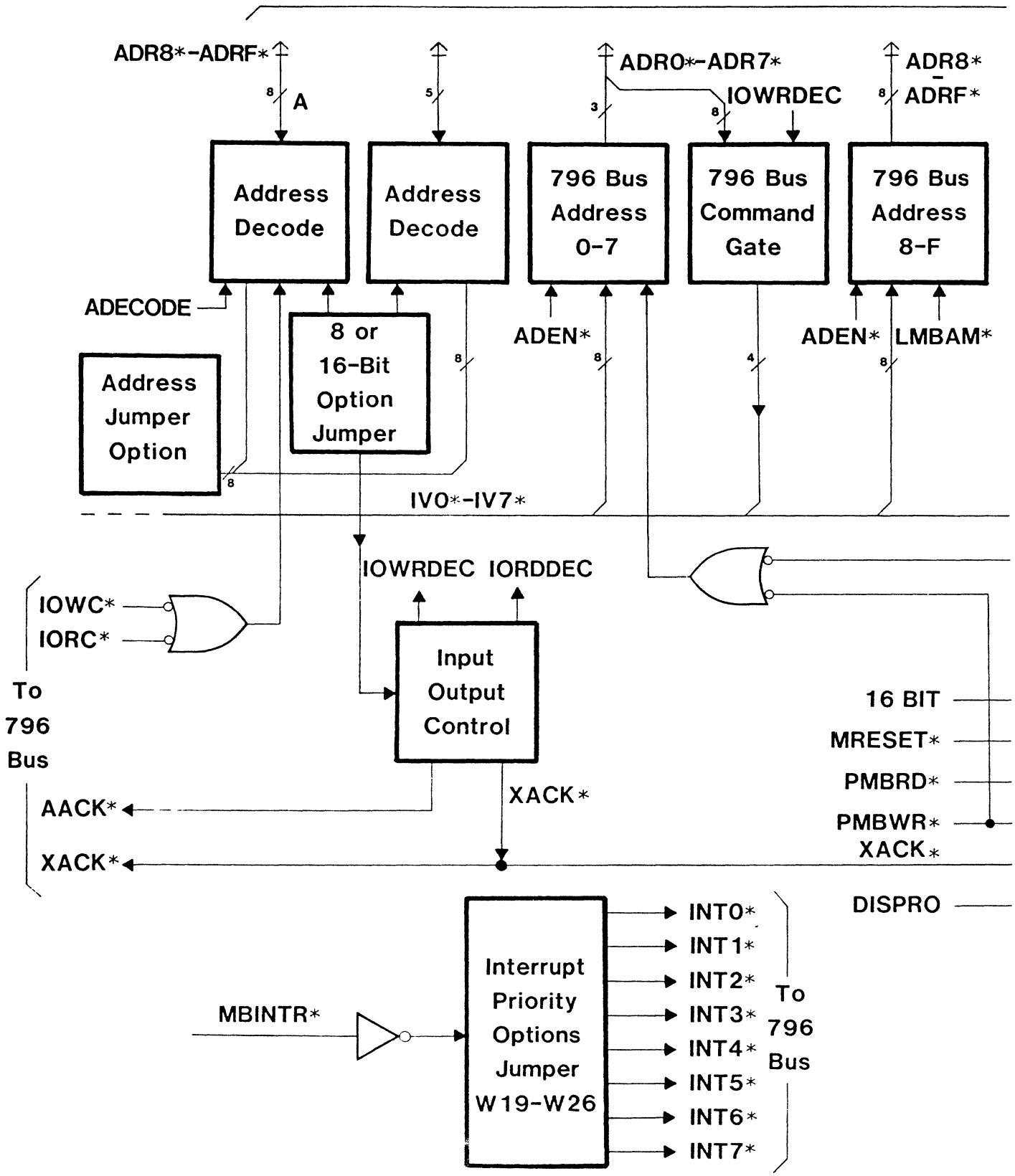



Figure 3-3 – 796 Bus Interface Block Diagram

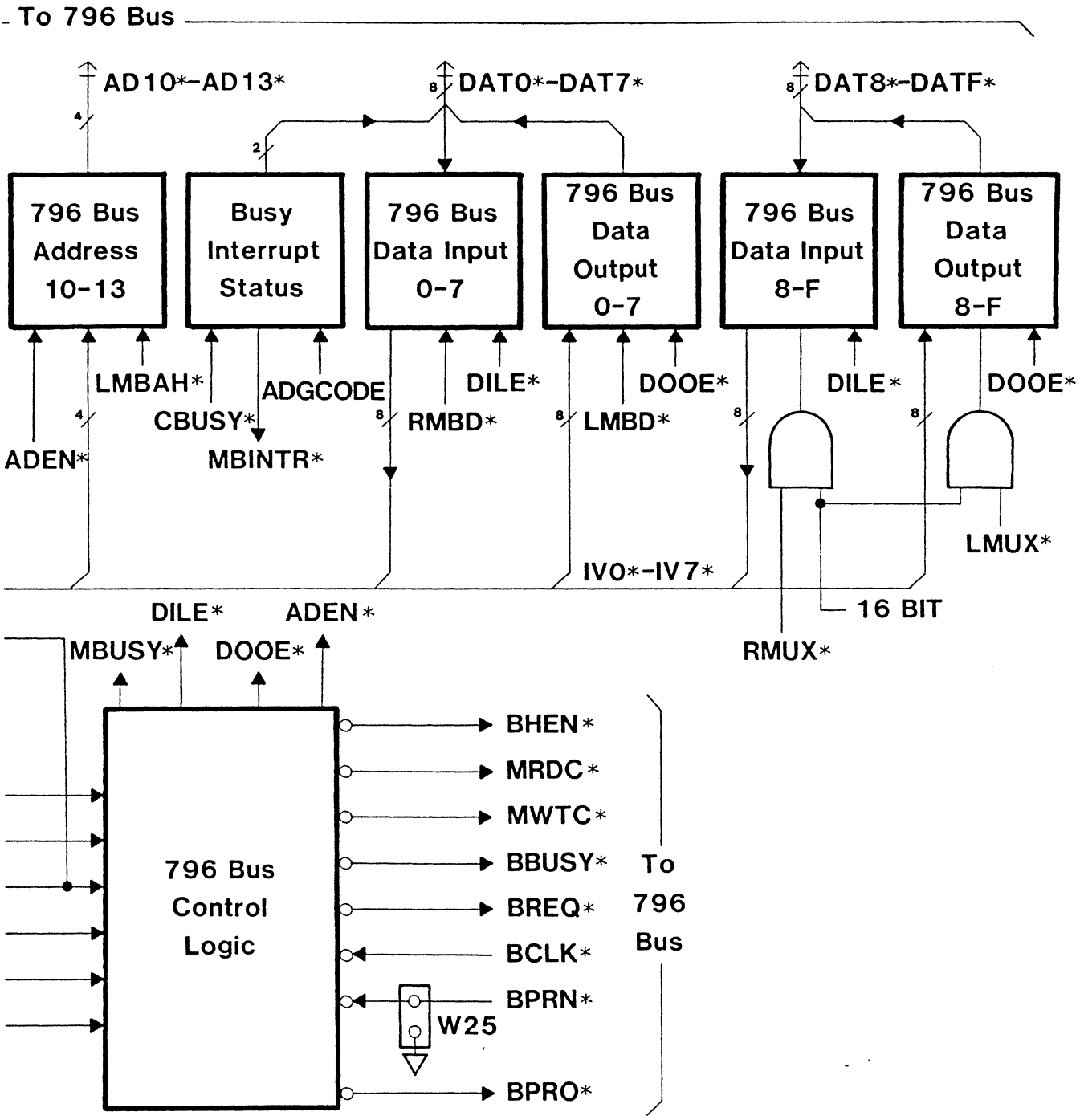



Figure 3-3 – 796 Bus Interface Block Diagram (Continued)

3.27 In the DMA mode, the loading and reading of these registers is in part under control of the *796 Control Logic.*

(1) DILE* — Data Input Load Enable,

(2) DOOE* — Data Output Output Enable,

To load data from the 796 Bus into the *796 Bus Input* register DILE* is asserted. Data is sent to the 796 Bus from the *796 Bus Outout* register when DOOE* is asserted. Both of these signals apply to the external side of the WDC and are dependent on the direction or transfer of data.

3.28 On the internal side, Fast IV select decode signals handle loading and reading of these registers to IV Bus.

(1) RMBD* — Read 796 Bus Data Register.

(2) LMBD* — Load 796 Bus Data Register.

(3) RMUX* — Read Multiplexer.

(4) LMUX* — Load Multiplexer.

Table 3-2 — Winchester Disk Controller Active 796 Bus Signals

| Diagram Mnemonic | 796 Bus Mnemonic (1) | Pin | Function |
|---|---|---|---|
| BCLK* | BCLK* | 13 | Bus Clock. |
| MBINIT* | INIT* | 14 | Initialize. |
| BPRN* | BPRN* | 15 | Bus Priority In. |
| BPRO* | BPRO* | 16 | Bus Priority Out. |
| BBUSY* | BUSY* | 17 | Bus Busy. |
| BREQ* | BREQ* | 18 | Bus Request. |
| MRDC* | MRDC* | 19 | Memory Read Command. |
| MWTC* | MWTC* | 20 | Memory Write Command. |
| IORC* | IORC* | 21 | I/O Read Command. |
| IOWC* | IOWC* | 22 | I/O Write Command. |
| XACK* | XACK* | 23 | Xfer Acknowledge. |
| AACK* | LOCK* | 25 | Lock. |
| BHEN* | BHEN* | 27 | Byte High Enable. |
| INT0*—INT7* | INT0*—INT7* | 35-42 | Parallel Interrupt Requests. |
| A0*—A13* | ADR0* | Various | 20-Bit Address Bus. |
| DB0*—DBF* | DAT0*—DATF* | Various | 16-Bit Data Bus. |

Note:

(1) Address and data bus lines are in hexadecimal notation.

3.29 The *796 Bus Control Logic* exchanges the 796 Bus arbitration signals.

(1) BHEN*,

(2) MRDC*,

(3) MWTC*,

(4) BBUSY*,

(5) BREQ*,

(6) BCLK*,

(7) BPRN*,

(8) BPRO*,

The functions of each are described in Table 3-2. Option Jumper, W25, provides for making the WDC highest priority Bus Master.

3.30 On the other side of the *796 Bus Control Logic* are the signals generated on the WDC or used to control the 796 Bus signals.

(1) 16 BIT — defines whether the WDC is transferring 8- or 16-bit words to the 796 Bus.

(2) MRESET* — is the WDC reset.

(3) PMBRD* — a Fast IV Select Decode signal.

(4) PMBWR* — a Fast IV Select Decode signal.

When (3) or (4) are strobed, the *796 Bus Control Logic* initiates the 796 Bus handshaking, and transfers the data. During the transfer, the $\mu$P checks:

(5) MBUSY* — 796 Bus Busy over the IV Bus to determine when the transfer is completed.

3.31 Option Jumpers, W16-W26, set the *Interrupt Priority* for MBINTR* to the 796 Bus Interrupt Levels, INT0*-INT7*. MBINTR* is generated by the $\mu$P over the IV Bus at the end of a data transfer.

3.32 The transfer acknowledge, XACK*, has two possible directions.

(1) This signal is created on the WDC and sent to the 796 Bus in response to an I/O read or write.

(2) This signal is input to the WDC from the 796 Bus at the completion of a data transfer from another Bus Master.

**Control and Status**

3.33 Figure 3-4 illustrates the internal WDC status and control registers and transfer gates in block diagram. The *Disk Select Register*, *Disk Control Register*, and *Disk Status Gate* connect directly to the Winchester Drive by the disk status and control cable.

3.34 Option Jumpers, W13-W18, provide for alternate, J6, wiring to accommodate two different Winchester disk drives.

(1) Seagate Technology 506. The 506 uses a 34-conductor connector.

(2) Shugart Associates 1000. The 1000 uses a 50-conductor connector.

3.35 The *Disk Select and Control Registers* are enabled with DSKEN*. This provision is made to prevent invalid write operation to the disk drive before the $\mu$P sets up the initial values in the registers, e.g., during power on operation. The *Disk Select Register* determines which drive and surface is accessed.

(1) DS0*-DS3* are the drive select lines for up to four drives. Only one of these are asserted at a time.

(2) HS0*-HS2* are coded head select lines for up to 8 heads.

The remaining register output is used internally to the WDC.

(3) MBINT* is the interrupt generated by the $\mu$P and furnished to the 796 Bus. Refer to Figure 3-3. 16 BIT and LMUX* furnish the control for this register.

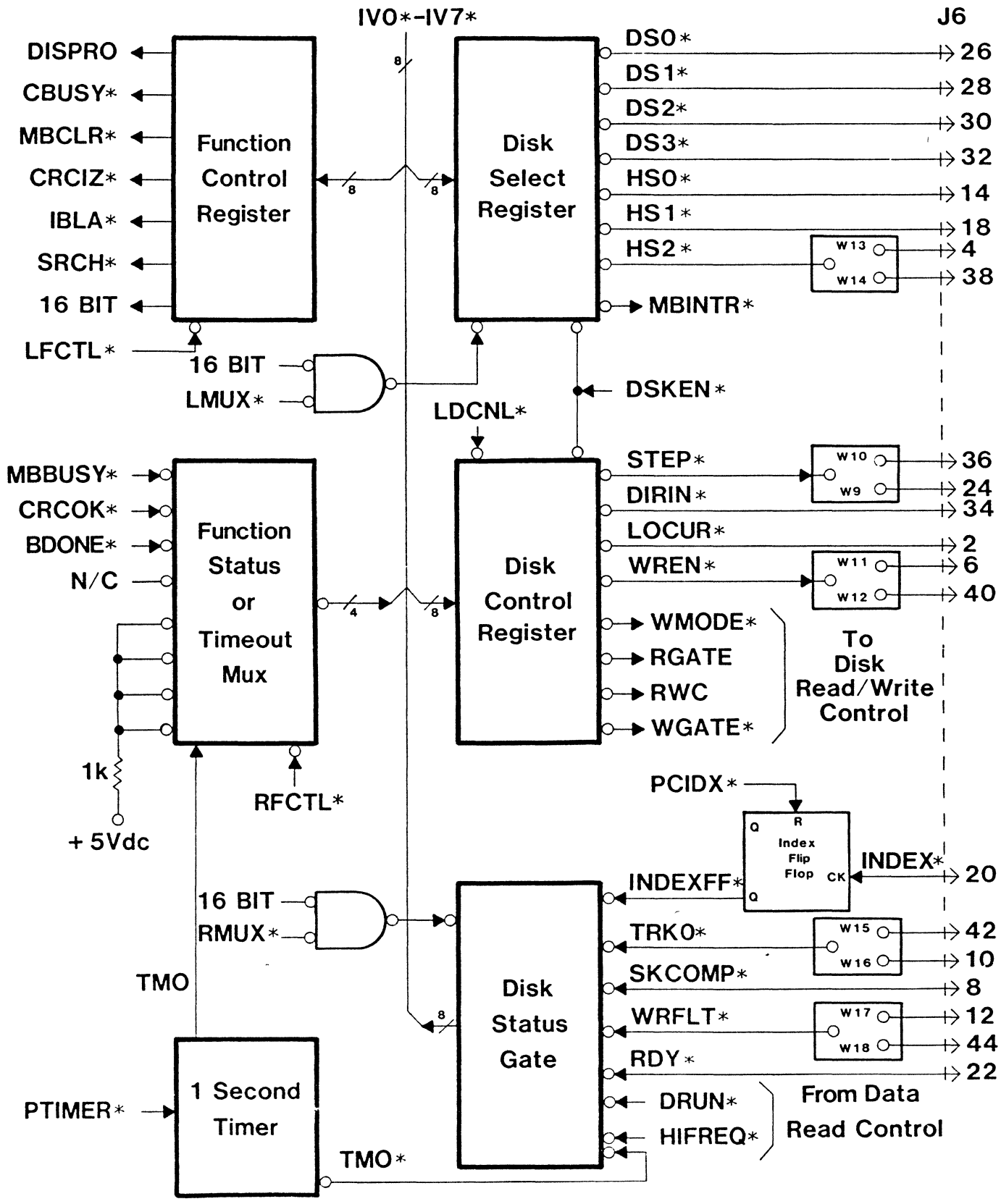



Figure 3-4 – Control and Status Block Diagram

3.36 Head position and write control information are determined by the value in the *Disk Control Register.*

(1) STEP* moves the head one increment.

(2) DIRIN* determines the direction of the head movement.

(3) LOCUR* is a control signal furnished to the drive to reduce the write current on different tracks. These tracks vary for different drive types. This line allows the control program to adjust the current when appropriate.

(4) WREN* is the write enable signal to the drive.

The four remaining lines are supplied to the Disk Read Write Control. Refer to Figure 3-5.

(5) WMODE* sets the Read/Write logic to Write Mode.

(6) RGATE* sets the Read/Write logic to Read Mode.

(7) RWC* is Reduce Write Current and means to internally perform write precompensation in the Read/Write logic.

(8) WGATE* is the Write Gate or data.

LDCNL* from the Fast IV Select Decode furnishes the control for this register.

3.37 Current disk status information is gated onto the IV Bus, IV0*-IV7*, through the *Disk Status Gate.*

(1) INDEX* is a short duration pulse furnished by the drive at the start of each disk revolution. The *Index Flip Flop* functions as a storage register and is cleared by the control program with Fast IV Select Decode PCIDX*.

(2) TRK0* indicates the drive heads are positioned at Track 0, the lateral indexing location on the disk.

(3) SKCOMP* is the Seek Complete signal.

(4) WRFLT* is the Write Fault signal.

(5) RDY* is the disk drive Ready signal.

The three remaining status signals are generated within the WDC.

(6) DRUN* indicates the Synch Field Detector has detected a field of all zero's. This is the synch field before the Address Mark.

(7) HIFREQ* indicates the Address Mark Detector has detected a high frequency field. This is a 5 MHz signal which may be an all zero's pattern. The all zero's pattern is the bitsynch field preceeding an ID Address Mark or a Data Address Mark.

(8) TMO* indicates the data transfer was abortive and must be restarted.

3.38 The *Function Status or Timeout Multiplexer* monitors the WDC status lines:

(1) MBBUSY* is the signal furnished from the *796 Control Logic* indicating the 796 Bus is performing a data transfer.

(2) CRCOK* is the signal furnished from the Read and Write logic indicating that the CRC check was made.

(3) BDONE* is the signal furnished from the Read and Write logic indicating serial to parallel conversion was performed.

The control program cannot interleave the statusing of these lines within every data transfer operation and maintain high speed operation. At the start of transfer the control program asserts Fast IV Select Decode PTIMER* starting the *1 Second Timer.* Should any of lines (1), (2) or (3) above not go high in 1 second, the WDC control program considers the operation abortive. The WDC logic must be cleared and the operation restarted. After one second TMO* forces the outputs high and asserts TMO* to the *Disk Status Gate.* At the completion of each transfer, the control program checks TMO*. If a time out has decoded, it asserts RFCTL* and checks the *Function Status* to determine which input caused the aborted operation and then restarts the data transfer.

3.39 The *Function Control Register* outputs are used within the WDC.

(1) DISPRO* disables the priority out. Refer to Figure 3-3.

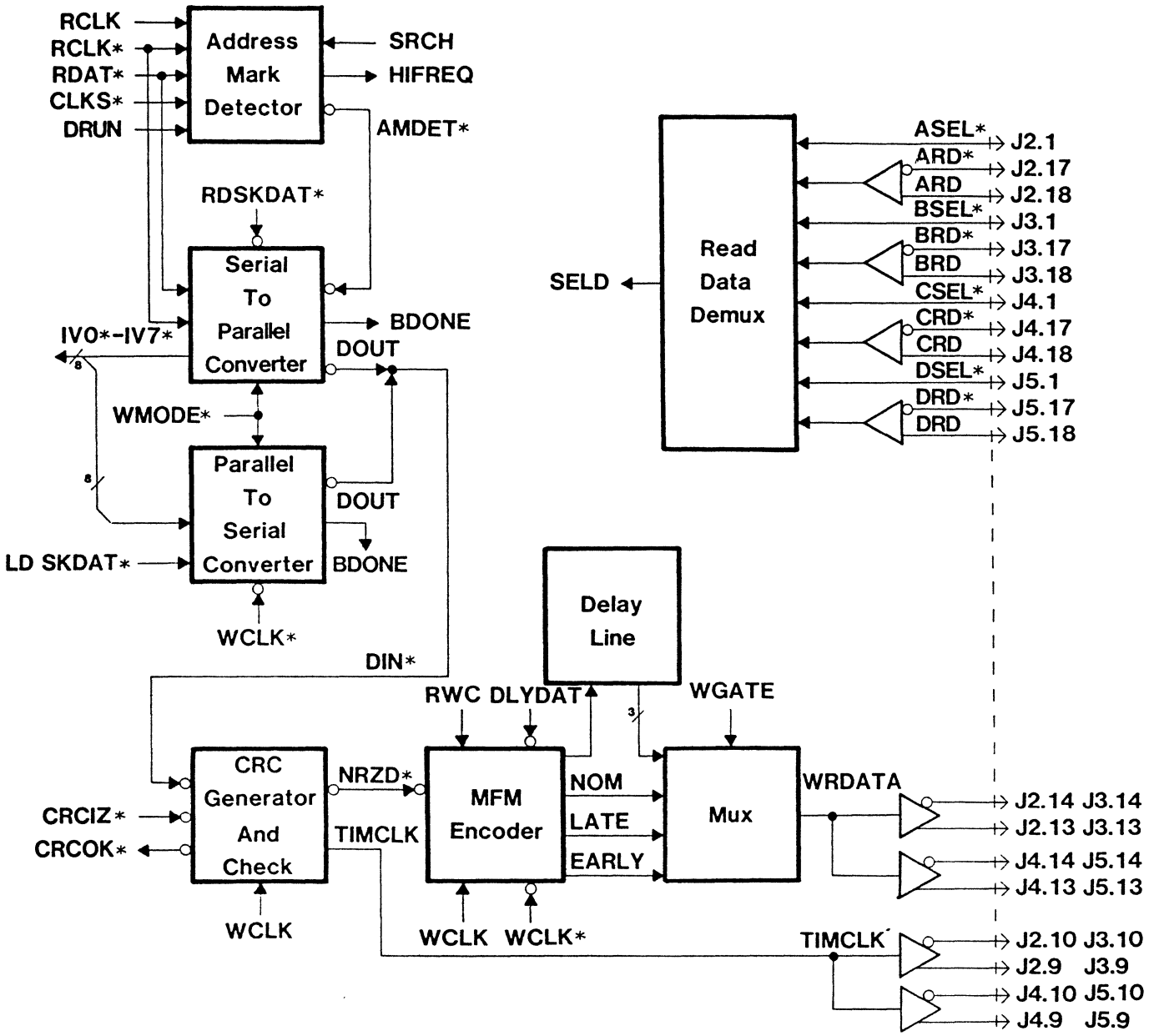



Figure 3-5 — Read and Write Logic Block Diagram

(2) CBUSY* indicates the controller is busy and is used by the Busy Interrupt Status.

(3) MBCLR* generates a 796 Bus INIT* and will initialize the Bus if Option Jumper W47 is installed.

(4) CRCIZ* initializes the CRC Generation and Check. Refer to Figure 3-5.

(5) IBLA* generates an Address Mark.

(6) SRCH* initiates a search for an Address Mark in the read data. Refer to Figure 3-5.

(7) 16 BIT indicates a 16 bit data transfer.

**Read and Write Logic**

3.40 Refer to Figure 3-5 for the description which follows. The Read and Write Logic perform the function of MFM Generation and Decode.

3.41 In the Read Mode, the first operation to perform is to locate the Address Mark in the Read data, so the preamble can be checked for addressed sector and cylinder number. The *Address Mark Detector* has four signals from the Phase-Locked Data Recovery input to it.

(1) RCLK and RCLK* are the Read Clock generated by the VCO.

(2) RDAT* is the Read Data and is synchronized to the VCO. A RDAT* transition indicates a data transition.

(3) CLKS* is the signal clock. CLKS* indicates a clock transition.

(4) DRUN* indicates the Synch Field Detector has detected a field of all zero's. This is the synch field before the Address Mark.

3.42 The $\mu$P uses two signals to control and monitor the *Address Mark Detector.*

(1) SRCH* initiates a search for an Address Mark in the read data.

(2) HIFREQ* indicates the *Address Mark Detector* has detected a high frequency field. This is a 5 MHz signal which may or may not be all zero's.

When the *Address Mark Detector* detects the Address Mark, AMDET* is asserted to the *Serial to Parallel Converter.*

3.43 RCLK* and RDAT* are both used as inputs to the *Serial to Parallel Converter.* Read Data is shifted into an internal shift register until an 8-bit word has been assembled. The converter then asserts BDONE.

(1) BDONE at this time indicates to the $\mu$P that a word has been assembled and been transferred to a separate internal buffer register. This provides the $\mu$P with one word time to read the assembled word onto the IV Bus and clear BDONE.

The Fast IV Select Decode asserts RDSKDAT* to gate this word onto the IV Bus and clear BDONE.

3.44 The last operation performed in the Read Mode is to make a CRC check on the Preamble and the Read Data words. RCLK* clocks these words through the *CRC Generator and Check.* If the check is determined to be correct:

(1) CRCOK* is asserted to the Disk Status Gate.

(2) CRCIZ* is issued from the Function Control Register to clear out the *CRC Generator and Check* before it is used again.

3.45 In the Write Mode, the first operation to perform is a Read Mode operation until the addressed sector is located. A switch is made at the end of the Preamble to the Write Mode by asserting WMODE*.

3.46 LDSKDAT* loads the 8-bit Write Data word from the IV Bus into an internal register of the *Parallel to Serial Converter.* The Write Data word is shifted out as serial data, DOUT*, and on to DIN* of the *CRC Generator and Check.* The clocking is performed by WCLK*.

3.47 A CRC word is calculated from and appended to the Write Data. Output data:

(1) NRZD* is Non-Return to Zero data format.

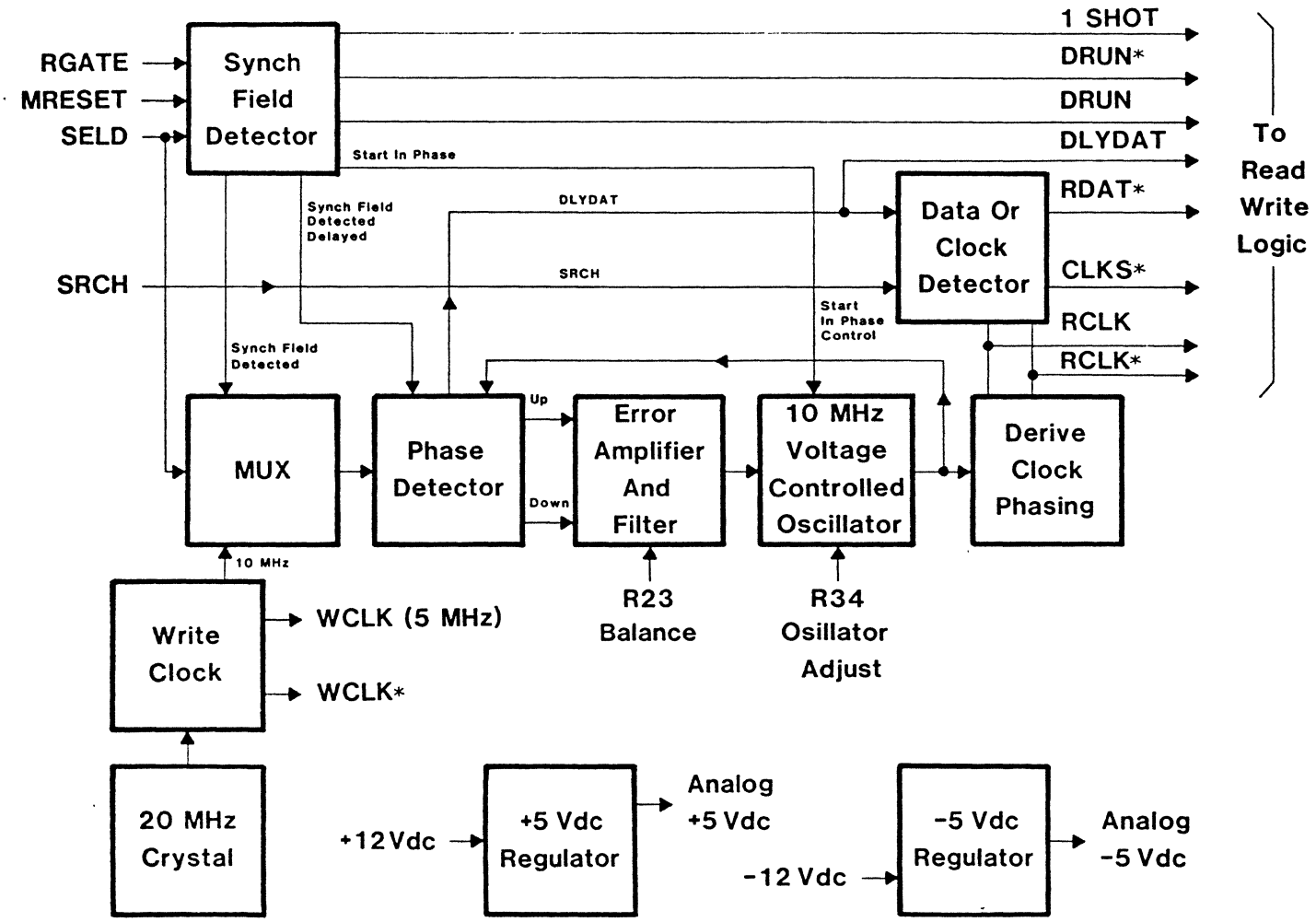



Figure 3-6 — Phase-Locked Data Recovery Block Diagram

3.48 The *MFM Encoder* performs two operations to the Write Data.

(1) The Write Data is converted from NRZ format to a MFM encoded signal.

(2) The Encoder provides the control lines NOMINAL, LATE or EARLY for the write precompensation. A particular write transition will be held at its true position which falls on either a data or clock transition, if the NOMINAL line is selected. If the LATE line is selected, the write transition will shift 12 ns after the true position, or if the EARLY line is selected, the shift will be 12 ns before the true position. The true position is referenced to the WCLK* transition.

3.49 A *Delay Line* furnishes the delay outputs to the *Multiplexer.*

(1) Early is a 24 ns delay.

(2) Nominal is a 36 ns delay.

(3) Late is a 48 ns delay.

3.50 Write precompensation is necessary when the disk has bit crowding. Bit crowding is caused by higher bit densities in sectors toward the center of the disk. Exact cylinder positions to begin with precompensation depend on the disk drive type. For this reason, exact cylinder locations for write precompensation are provided in the control program. Write precompensation has the effect of restoring the phase relationship in the Read Data during data recovery.

3.51 Two control lines are input to the *MFM Encoder.*

(1) RWC activates write precompensation to the Write Data. RWC is not asserted in those sectors of the disk which do not have bit crowding.

(2) DLYDAT is generated in the Read Data Phase Detector. It is the Write Clock delayed by 60 ns.

3.52 WRDATA, the Write Data output line, is distributed through two differential line drivers to up to four disk drives. Each drive has a separate disk data connectors, J2-J5. Additionally, TIMCLK, Time Clock, a general purpose reference frequency required by some drive types, is also distributed from these disk data connectors.

3.53 MFM Encoded Read Data is input to four differential receivers connected to the disk data connectors as lines:

(1) ARD*/ARD.

(2) BRD*/BRD.

(3) CRD*/CRD.

(4) DRD*/DRD.

Note each differential line has an associated select line, A/B/C or DSEL*. Incorrect cable connections between the disk drives and the WDC are eliminated through a unique design. The select line from the accessed disk drive is asserted by the drive. The *Read Data Multiplexer* then connects its input to the associated receiver. SELD, Selected Data, is output to the Phase-Locked Data Recovery.

#### Phase-Locked Data Recovery

3.54 Figure 3-6 illustrates the Phase-Locked Data Recovery in block diagram for the description which follows. Initially, the MFM encoded Selected Data Line, SELD, is input to the *Synch Field Detector* which looks for a series of zero's proceeding an Address or Data Mark. Since this same pattern can also appear in a normal data field, the $\mu$P causes the detector to read the incoming data for a preset interval until it does or does not read an Address Mark.

3.55 Once a synch field is detected, the *Multiplexer* is switched by the Synch Field Detected line. The *Multiplexer* has two inputs.

(1) A 10 MHz reference from the *Write Clock* is initially connected to the *Phase Detector* to develop DLYDAT for Write Mode.

(2) When a potential synch field is detected, the *Multiplexer* switches to SELD as the input to the *Phase Detector* because the incoming Read Data is potential valid data.

3.56 The Phase-Lock loop is made up of three sections.

(1) The *Phase Detector* which produces an error signal derived from a phase comparison of Read Data and the 10 MHz output of the *Voltage Controlled Oscillator* (VCO).

(2) The error signals, Up and Down, are filtered in the *Error Amplifier and Filter* to provide the proper loop response.

(3) The *10 MHz Voltage Controlled Oscillator* is adjusted in frequency by the error signal.

The VCO output is phase-locked to the incoming Read Data.

3.57 The purpose of the *Derived Clock Phasing* is to produce a 5 MHz Read Clock, RCLK/RCLK*, which is in half bit synchronization with the incoming Read Data.

3.58 The DLYDAT line derived in the *Phase Detector* is input to the *Data or Clock Detector* and output to the Read Write Logic for the Write Mode. RCLK/RCLK* is input to the *Data or Clock Detector* as a reference. The outputs are:

(1) RDAT* is the Read Data. A transition indicates Read Data.

(2) CLKS* is the Signal Clock. A transition indicates a clock.

3.59 A second input to the *Data or Clock Detector* is search, SRCH, a control line from the $\mu$P. Once a possible synch field has been located and the VCO is locked onto the Read Data, SRCH is asserted. This causes the *Data or Clock Detector* to start generating data for the Read Logic.

3.60 The $\mu$P monitors DRUN* to determine when a possible synch field has been detected, phase locked and acquiring data. A built in delay is provided in the control program to allow for the phase lock to take place before the $\mu$P asserts SRCH.

3.61 Exceptionally fast aquisition time is provided by the Start in Phase line from the *Synch Field Detector*. The phase lock does not have to go through a long initialization period since the VCO is started in phase. The oscillator is actually stopped and restarted again to assure proper phasing. There is some phase delay between the VCO and the Read Data immediately after starting the oscillator. For this reason, a delay of about 1 ns is built into the control program to allow for the phase lock to take place.

3.62 The status line, ONE SHOT, is used by the $\mu$P to determine if the *Synch Field Detector* is still in a possible synch field. A One Shot is held retriggered while a 5 MHz signal is detected, as soon as it becomes untriggered, the bounds of a possible synch field have been exceeded. In this case, the $\mu$P restarts the phase lock procedure by looking for a synch field. The trigger is set for 270 ns or 1.5 clock times.

3.63 The criteria for a valid synch field are:

(1) The ONE SHOT is retriggered.

(2) 16 bits of all zero's counted by the *Synch Field Detector.*

## 4. SPECIFICATIONS

4.01 The following furnishes the user with information for shipping and installation and should be used to establish acceptance criteria if they are performed. Minor deviations from the specifications tabulated in Table 4-1 which do not affect the Winchester Disk Controller performance are excluded from the Codata Systems Corp. warranty.

Table 4-1 — Winchester Disk Controller 92-1011-xx Specifications

| PARAMETER | CHARACTERISTICS |
|---|---|
| Controller Device | Signetics 8X300. |
| Drive, Type | ST506. |
| , Number | Four. |
| , Capacity Formatted | 4,882,432 bytes. |
| Recording Format | |
| Type | MFM. |
| Data Rate | 5 MHz. |
| Error Checking | 16-bit CRC. |
| Data Buffer Size | 4k bytes. |
| Disk Format, Logical | |
| Sector Size | 128 bytes. |
| Sectors | 38,144 maximum. |
| Disk Format, Physical | |
| Bytes Per Sector | 256. |
| Sectors Per Track | 32. |
| Tracks Per Cylinder | 4. |
| Cylinders Per Drive | 153. |
| Cylinders, Spare | 4. |
| Alternate Sector Assignment | |
| Block Size | 4096 bytes. |
| Blocks | 28. |
| Bus Interface | IEEE 796 Bus Specification. |
| Mode | Master or slave. |
| Data Width | 16 bit. |
| Address Width | 20 bit. |
| Connector, P1 | IEEE 796 Bus Specification. |
| , P2 | Vacant. |
| I/O Port Address | |
| Address, Size | 8 or 16 bit. |
| , Operation | Option jumper. |
| , Standard | 90-97H; 8 bit. |

Table 4-1 — Winchester Disk Controller 92-1011-xx Specifications (Continued)

| PARAMETER | CHARACTERISTICS |
|---|---|
| Interrupt | |
| Operation | Option jumper. |
| Type | Level. |
| Levels | Eight. |
| Reset | |
| 796 Bus INIT* | Option jumper; master or slave. |
| External | Switch contact closure optional. |
| PCA Dimensions | IEEE 796 Bus Specification. |
| Length | 30.5 cm (12.0 inch). |
| Width | 17.1 cm (6.75 inch). |
| Spacing | 1.3 cm (0.5 inch). |
| Input Output Connector, J2-J5 | 20-conductor; mates to Ansley 609-2015M. |
| , J6 | 50-conductor; mates to Ansley 609-5015M. |
| Environment | |
| Temperature | |
| Operating | 4 C to 55 C (32 F to 131 F). |
| Storage | 0 C to 65 C (32 F to 149 F). |
| Humidity | 5% to 90%, noncondensing. |
| Power Requirements | |
| +12 Vdc Bus | 0.5 A. |
| +5 Vdc Bus | 2.5 A. |
| —12 Vdc Bus | 0.5 A. |
| Weight | 397 g. (14.0 oz.). |

## 5. OPERATION AND PROGRAMMING

### Options

5.01 Before the Winchester Disk Controller WDC is installed into the Mainframe card cage, the PCA options should be verified.

(1) Check the W1 through W47 Option Jumpers. Refer to Table 5-1.

(2) Check U30, U31, U48, U49, U76, and U77 ROM. Refer to Table 5-1.

5.02 Install the PCA into card position designated for the WDC. Refer to the Mainframe Hardware Reference Manual. Connect the disk I/O cables to J1 through J6.

### Controller Programming – General

5.03 Disk commands and addressing parameters are sent to the WDC by a Command Parameter Block (CPB) located in system RAM. The pointer to the CPB address is sent to the WDC by a series of bytes output via I/O ports.

5.04 The CPB contains information defining two other blocks of system RAM, the Data Block and a Status Block. A typical command sequence is:

(1) Read I/O port WDCBASE+0 and wait until the WDC is not busy.

(2) Set up the CPB in system RAM for the next operation.

(3) Issue the pointer to the CPB using I/O writes to WDCBASE+0, WDCBASE+2, and WDCBASE+4 in that order.

(4) Start the controller by issuing WDCBASE+6.

If not operating under interrupts, wait until:

(5) The WDC is not busy by reading I/O port WDCBASE+0 until the busy bit is reset.

(6) Check the status of the last operation by referring to the status block in system RAM.

If operating under interrupts:

(7) Return to normal processing until an interrupt from the WDC occurs.

(8) When the interrupt has occurred, check that the interrupt was caused by this device by reading I/O port WDCBASE+0 and inspecting the interrupt bit. If this device caused the interrupt, clear the interrupt by issuing a write to I/O port WDCBASE+7 to clear the interrupt.

(9) Determine the status of the last operation by referring to the status block in system RAM.

### I/O Ports – CPB Pointer

5.05 Eight Consecutive I/O port addresses are used by the WDC to provide the following control information described below. The base address of the block WDCBASE is set by option jumpers. Table 5-2 tabulates these I/O port address assignments.

5.06 *WDC Busy and Interrupt Status* – The byte read at WDCBASE+0 represents the following:

(1) Bit 7 WDC Busy. If set, the WDC is busy with an operation. If reset, the WDC may accept a new command.

(2) Bit 6 WDC Interrupting. If set, the WDC is currently interrupting at the priority level set by option jumpers.

(3) Bits 5-0 are not assigned.

5.07 *CPB Address* – The 20-bit address formed by the three bytes of CPB Address point to a Command Parameter Block (CPB) which determines the type of operation, disk address, data address, block length and status block address.

Table 5-1 — Winchester Disk Controller Options — P/N 92-1011-xx

| Option | Flag 01 | Description |
|---|---|---|
| | | ROM Type Select |
| W1 | | IS3 = L. |
| W2 | x | IS3 = H. |
| W3 | | IS2 = L. |
| W4 | x | IS2 = H. |
| W5 | | A10 = GND. |
| W6 | x | A10 = A10. |
| W7 | | A9 = GND. |
| W8 | x | A9 = A9. |
| | | 8.0-Inch or 5.25-Inch Disk |
| W9 | x | STEP* to J6-24. |
| W10 | | STEP* to J6-36. |
| W11 | x | WREN* to J6-6. |
| W12 | | WREN* to J6-40. |
| W13 | x | HS2* to J6-4. |
| W14 | | HS2* to J6-38. |
| W15 | x | TRK0* to J6-10. |
| W16 | | TRK0* to J6-42. |
| W17 | x | WRFLT* to J6-12. |
| W18 | | WRFLT* to J6-44. |
| | | Interrupt Select |
| W19 | | MBINTR* to INT6. |
| W20 | | MBINTR* to INT7. |
| W21 | | MBINTR* to INT4. |
| W22 | | MBINTR* to INT5. |
| W23 | | MBINTR* to INT2. |
| W24 | | MBINTR* to INT3. |
| W25 | | MBINTR* to INT0. |
| W26 | | MBINTR* to INT1. |
| | | 16-Bit or 8-Bit I/O Address |
| W27 | | 16-Bit I/O Address. |
| W28 | x | 8-Bit I/O Address. |
| | | I/O Address Select |
| W29 | x | ADRF = 1, ADR7 = 1. |
| W30 | | ADRF = 0, ADR7 = 0. |
| W31 | | ADR8 = 1. |
| W32 | | ADR8 = 0. |
| W33 | | ADRE = 1, ADR6 = 1. |
| W34 | x | ADRE = 0, ADR6 = 0. |

Table 5-1 — Winchester Disk Controller Options — P/N 92-1011-xx (Continued)

| Option | Flag 01 | | | | | Description |
|---|---|---|---|---|---|---|
| W35 | | | | | | ADR9 = 1. |
| W36 | | | | | | ADR9 = 0. |
| W37 | | | | | | ADRD = 1, ADR5 = 1. |
| W38 | x | | | | | ADRD = 0, ADR5 = 0. |
| W39 | | | | | | ADRA = 1. |
| W40 | | | | | | ADRA = 0. |
| W41 | x | | | | | ADRC = 1, ADR4 = 1. |
| W42 | | | | | | ADRC = 0, ADR4 = 0. |
| W43 | | | | | | ADRB = 1, ADR3 = 1. |
| W44 | x | | | | | ADRB = 0, ADR3 = 0. |
| W45 | | | | | | BPRN* to Ground. |
| W46 | x | | | | | MBINIT* from 796 Bus to Card. |
| W47 | | | | | | MBINIT* from Card to 796 Bus. |

| Option | Flag 01 | | | | | Description | |
|---|---|---|---|---|---|---|---|
| | | | | | | Mnemonic | Codata Part Number |
| U77 | x | | | | | ROM0A HX0 | 27-0030-01 |
| U49 | x | | | | | ROM0A HX1 | 27-0029-01 |
| U31 | x | | | | | ROM0A HX2 | 27-0028-01 |
| U76 | x | | | | | ROM1 HX0 | 27-0027-01 |
| U48 | x | | | | | ROM1 HX1 | 27-0026-01 |
| U30 | x | | | | | ROM1 HX2 | 27-0025-01 |

Notes:

(1) An X in the Flag column indicates a jumper is installed, a wrapped wire is installed, the switch is set or the ROM is installed.

Table 5-2 — I/O Port Address Assignments

| Address | Type | Function |
|---|---|---|
| WDCBASE+0 | Read | WDC Busy and Interrupt Status. |
| WDCBASE+0 | Write | CPB Address Bits 0—7. |
| WDCBASE+2 | Write | CPB Address Bits 8—15. |
| WDCBASE+4 | Write | CPB Address Bits 16—19. |
| WDCBASE+6 | Write | WDC Configuration Parameters and GO. |
| WDCBASE+7 | Write | Reset WDC Interrupt. |

5.08 *WDC Configuration and GO* – Issuing this byte performs two functions. Certain configuration parameters of the WDC are defined and the WDC is commanded to GO. This byte should be issued only after the CPB has been defined in system RAM, and all three bytes of the CPB pointer have been output. The meaning of the configuration portion of this byte are:

(1) Bit 7 Interrupt Enable. If set an interrupt will be generated at the end of the current operation. If reset no interrupt will be issued.

(2) Bit 6 Data Word Length. If set the Data Word Length is 16 bits. If reset the Data Word Length is 8 bits.

(3) Bits 5-0 are not assigned.

5.09 *Reset WDC Interrupt* – Issuing an I/O write to this port causes the Interrupt from the WDC to be reset. In addition, the interrupt status, Bit 6, of WDCBASE+0 Read will be reset.

**Command Parameter Block**

5.10 The CPB organization is listed in Table 5-3. The *Command Byte* code description is listed in Table 5-4.

**Table 5-3 – Command Parameter Address Block Assignments**

| Location | Description | |
|---|---|---|
| CPB+0 | Command Byte. | |
| CPB+1 | Unit Number. | |
| CPB+2 | Logical Sector Number | Bits 0-7. |
| CPB+3 | Logical Sector Number | Bits 8-15. |
| CPB+4 | Logical Sector Number | Bits 16-23. |
| CPB+5 | Byte of 00 (1) | |
| CPB+6 | Byte Count | Bits 0-7. |
| CPB+7 | Byte Count | Bits 8-15. |
| CPB+8 | System RAM Address | Bits 0-7. |
| CPB+9 | System RAM Address | Bits 8-15. |
| CPB+10 | System RAM Address | Bits 16-19. |
| CPB+11 | Byte of 00 (1) | |
| CPB+12 | Status Block Pointer | Bits 0-7. |
| CPB+13 | Status Block Pointer | Bits 8-15. |
| CPB+14 | Status Block Pointer | Bits 16-19. |
| CPB+15 | Byte of 00 (1) | |

Note:

(1) Reserved for expansion.

5.11 *Unit Number* – This defines the logical unit number of the disk drive. Option jumpers on each drive define the individual disk. The allowed range of unit is 0 to 3.

5.12 *Logical Sector Number* (LSN) — Refers to the 128 byte logical sector used to address the disk. The range of addressing is 0 to 094FFH.

5.13 *Byte Count* – Refers to the number of bytes to be transferred. If a count is given which when taken with the System RAM Address exceeds the currently defined 64k Bank, transfer will continue into the next bank.

5.14 If a byte count is given which when taken with the LSN, exceeds the capacity of the drive, an error flag will be returned.

**IMPORTANT**

*If an odd byte count is specified, the Controller will transfer data in an 8-bit word length even if a word length of 16 bits was specified in the data sent to I/O port WDCBASE+5.*

5.15 *System RAM Address* – The System RAM Address defined in the CPB consists of a 16-bit RAM address and a 4-bit bank address. If the address specified does not exist, then MBTMO, 796 Bus TIMEOUT, status will be returned.

**IMPORTANT**

*If the starting address specified is an odd address, DMA data transfers will be performed on a 8-bit basis even if the word length was defined to be 16 bit.*

The WDC uses the INTEL (R) convention of byte addressing when using 16-bit memory addressing:

(1) Least significant byte is an even address.

(2) Most significant byte is an odd address.

Table 5-4 – Command Byte Code

| Code | Description |
|---|---|
| 00H | Return status of specified drive. |
| 01H | Seek/Read. |
| 02H | Close Buffer. |
| 03H | Close Buffer then verify after write is complete. |
| 04H | Not assigned. |
| 05H | Format Disk. |
| 06H | Surface Analysis. |
| 07H | Restart WDC. |
| 08H | Reserved for diagnostic operation code. |
| 09H | Reserved for diagnostic operation code. |
| 0AH | Reserved for diagnostic operation code. |
| 0BH | Reserved for diagnostic operation code. |
| 0CH | Reserved for diagnostic operation code. |
| 0DH | Reserved for diagnostic operation code. |
| 0EH | Reserved for diagnostic operation code. |
| 0FH | Reserved for diagnostic operation code. |
| 10H | Reserved for diagnostic operation code. |
| 11H | Reserved for diagnostic operation code. |
| 12H | Seek/Write. |
| 13H | Seek/Write then verify CRC after write is done. |
| 14H | Seek/Write unallocated. |
| 15H | Seek/Write unallocated then verify CRC after write is done. |
| 16H-FFH | Not assigned. |

5.16 *Status Block Pointer* (SBP) — The SBP defined by the SBP refers to the location of system RAM where the two byte status block is to be returned. If the SBP refers to a location which does not actually exist in system RAM, then the WDC will time out while attempting to return the status. Busy will be cleared and an interrupt, if requested, will be generated. Since the Status Block is illegal, however, the system will be unable to determine status.

Table 5-5 – Status Block Address Assignments

| Location | Description |
|---|---|
| SBP+0 | Current Status. |
| SBP+1 | Current Configuration. |

Status Block

5.17 The Status Block is returned to system RAM after the completion of an operation. The location of the Status Block is defined by the Status Block Pointer in the CPB. Table 5-5 lists the Status Block address assignments.

5.18 *Status Code* – Table 5-6 describes the status code.

5.19 *Configuration Code* – The byte returned defines the drive type for which the WDC is configured. Normally this is 00H.

Data Block

5.20 The Data Block location is defined by System RAM Address in the CPB. The length is dependent upon Byte Count.

Table 5-6 — Status Byte Code

| Code | Description |
|---|---|
| AxH | No error after x retries, alternate sector was assigned. |
| 9xH | No error after x retries. Alternate sector was used. |
| 8xH | No error after x retries. |
| | Operator Correctable Errors |
| 41H | Drive not ready. |
| | Unrecoverable System Errors |
| 21H | Unrecoverable Read Error. |
| 22H | Preamble not found in three revolutions. |
| 23H | Timeout during preamble search. |
| 24H | Timeout during 796 Bus transfer. |
| 25H | Timeout during write operation. |
| 26H | Timeout during seek or restore. |
| 27H | Timeout during Format. |
| 28H | Timeout during Read. |
| 29H | Alternate Sector Table full. Cannot reassign. |
| 2AH | Unrecoverable error during alternate table save. |
| 2BH | Sequence Error — IDAM instead of DAM. |
| 2CH | Cannot read alternate sector table. |
| | Programming Parameter Errors |
| 11H | Unit Address Error. |
| 12H | Logical Sector Address Error. |
| 13H | 796 Bus Memory Address Error. |
| 14H | Illegal Command Error. |

**Interrupts**

5.21 An interrupt to one of the 796 Bus pins INT0* through INT7* will be generated after completion of an operation under the following circumstances:

(1) The interrupt level has been option jumpered on PCA.

(2) Interrupt enable has been set in I/O port WDCBASE+6, Bit 7 = 1, during command set up.

5.22 The interrupt appears as a low true level on the 796 Bus. The level will be reset to a high level by issuing either:

(1) I/O write to WDCBASE+7, or

(2) Starting a new operation by issuing a CPB pointer, an I/O sequence ending in an I/O write to WDCBASE+6.

**Power On Sequence**

5.23 The power on sequence is as follows:

(1) WDC Busy is set and WDC Interrupt is clear as soon as power is applied.

(2) Approximately one second after power on, WDC Busy is reset and the WDC Interrupt remains inactive.

(3) The WDC is ready to accept commands.

Table 5-7 — 8-Bit Address Option Jumpers

| WDCBASE | Options | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | W30 | W29 | W34 | W33 | W38 | W37 | W42 | W41 | W44 | W43 | W27 | W28 |
| 00H | X | | X | | X | | X | | X | | | X |
| 08H | X | | X | | X | | X | | | X | | X |
| 10H | X | | X | | X | | | X | X | | | X |
| 18H | X | | X | | X | | | X | | X | | X |
| 20H | X | | X | | | X | X | | X | | | X |
| 28H | X | | X | | | X | X | | | X | | X |
| 30H | X | | X | | | X | | X | X | | | X |
| 38H | X | | X | | | X | | X | | X | | X |
| 40H | X | | | X | X | | X | | X | | | X |
| 48H | X | | | X | X | | X | | | X | | X |
| 50H | X | | | X | X | | | X | X | | | X |
| 58H | X | | | X | X | | | X | | X | | X |
| 60H | X | | | X | | X | X | | X | | | X |
| 68H | X | | | X | | X | X | | | X | | X |
| 70H | X | | | X | | X | | X | X | | | X |
| 78H | X | | | X | | X | | X | | X | | X |
| 80H | | X | X | | X | | X | | X | | | X |
| 88H | | X | X | | X | | X | | | X | | X |
| 90H | | X | X | | X | | | X | X | | | X |
| 98H | | X | X | | X | | | X | | X | | X |
| A0H | | X | X | | | X | X | | X | | | X |
| A8H | | X | X | | | X | X | | | X | | X |
| B0H | | X | X | | | X | | X | X | | | X |
| B8H | | X | X | | | X | | X | | X | | X |
| C0H | | X | | X | X | | X | | X | | | X |
| C8H | | X | | X | X | | X | | | X | | X |
| D0H | | X | | X | X | | | X | X | | | X |
| D8H | | X | | X | X | | | X | | X | | X |
| E0H | | X | | X | | X | X | | X | | | X |
| E8H | | X | | X | | X | X | | | X | | X |
| F0H | | X | | X | | X | | X | X | | | X |
| F8H | | X | | X | | X | | X | | X | | X |

### Configuration Option Jumpers

5.24 The configuration of the WDC is set through option jumpers. The -xx suffix to the PCA part number indicates the different versions. Table 5-1 tabulates the current configurations.

### I/O Address

5.25 The address of WDCBASE for I/O ports used on the WDC is provided in two ways:

(1) 8-bit address. Refer to Table 5-7.

(2) 16-bit address. Refer to Table 5-8 and Table 5-9.

Table 5-8 — 16-Bit Address Option Jumers — Digits w, y

| Digit Value | Option | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | W30 | W29 | W34 | W33 | W38 | W37 | W42 | W41 | W27 | W28 |
| 0 | X | | X | | X | | X | | X | |
| 1 | X | | X | | X | | | X | X | |
| 2 | X | | X | | | X | X | | X | |
| 3 | X | | X | | | X | | X | X | |
| 4 | X | | | X | X | | X | | X | |
| 5 | X | | | X | X | | | X | X | |
| 6 | X | | | X | | X | X | | X | |
| 7 | X | | | X | | X | | X | X | |
| 8 | | X | X | | X | | X | | X | |
| 9 | | X | X | | X | | | X | X | |
| A | | X | X | | | X | X | | X | |
| B | | X | X | | | X | | X | X | |
| C | | X | | X | X | | X | | X | |
| D | | X | | X | X | | | X | X | |
| E | | X | | X | | X | X | | X | |
| F | | X | | X | | X | | X | X | |

Table 5-9 — 16-Bit Address Option Jumper — Digit x

| Digit Value | Options | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | W44 | W43 | W40 | W39 | W36 | W35 | W32 | W31 |
| 0 | X | | X | | X | | X | |
| 1 | X | | X | | X | | | X |
| 2 | X | | X | | | X | X | |
| 3 | X | | X | | | X | | X |
| 4 | X | | | X | X | | X | |
| 5 | X | | | X | X | | | X |
| 6 | X | | | X | | X | X | |
| 7 | X | | | X | | X | | X |
| 8 | | X | X | | X | | X | |
| 9 | | X | X | | X | | | X |
| A | | X | X | | | X | X | |
| B | | X | X | | | X | | X |
| C | | X | | X | X | | X | |
| D | | X | | X | X | | | X |
| E | | X | | X | | X | X | |
| F | | X | | X | | X | | X |

5.26 If 16-bit I/O addressing is used, WDCBASE can assume one of 256 possible groups. The address is determined as follows:

(1) WDCBASE = wxyzH.

Digits w, y are defined as follows:

(2) w = y can have a range of 0 to F. The digit value is set by option jumpers. Refer to Table 5-8.

Digits x, z are defined as follows:

(3) if 0 x 7, z = 0
if 8 x F, z = 8

the digit value is set by option jumpers. Refer to Table 5-9.

### Interrupt Priority Level

5.27 Table 5-10 tabulates the interrupt option jumpers by function.

### 796 Bus INIT* Master/Slave

5.28 An Option Jumper, W46, provides for making the WDC a master or slave to the INIT*.

(1) For INIT* master operation, omit Option Jumper W46, install Option Jumper W47.

(2) For INIT* slave operation, install Option Jumper W46, omit Option Jumper W47.

### 796 Bus Priority In

5.29 If the WDC is installed as the highest priority device and the system in which it is installed has no provision for asserting PRN* then the following option jumper should be installed:

(1) If WDC highest priority device, install Option Jumper W45.

Table 5-10 — Interrupt Level Option Jumper

| Level | W25 | W26 | W23 | W24 | W21 | W22 | W19 | W20 |
|---|---|---|---|---|---|---|---|---|
| INT0 | X | | | | | | | |
| INT1 | | X | | | | | | |
| INT2 | | | X | | | | | |
| INT3 | | | | X | | | | |
| INT4 | | | | | X | | | |
| INT5 | | | | | | X | | |
| INT6 | | | | | | | X | |
| INT7 | | | | | | | | X |

Note:

(1) Only ONE jumper above should be installed.

(2) If WDC not highest priority device, omit Option Jumper W47.

**5.30** If the WDC is not the highest priority device, be sure the serial priority chain is not broken by empty card slots between the highest priority device and the WDC.

### Drive Address Assignments

**5.31** The Unit number of individual drives is determined by internal drive option jumpers. Refer to the Mainframe Hardware Reference Manual or drive OEM Technical Manual.

**5.32** The Logical Unit address sent to the WDC will be in the range 0 to 3. The drive option jumpering is defined in the range 1 to 4, the correlation is:

(1)

| Logical Unit | Drive Number |
|---|---|
| 0 | 1 |
| 1 | 2 |
| 2 | 3 |
| 3 | 4 |

## 6. MAINTENANCE

6.01 The Winchester Disk Controller is a result of several years of design, development and modern electronic manufacturing. The system components are designed with the latest semiconductors and integrated circuits. They operate at relatively low power levels with adequate cooling. Each WDC is operated under power and functionally tested in the Codata Systems Corp. factory for a minimum of 72 hours before shipment. The WDC can be expected to operate at peak performance for long intervals.

6.02 No routine maintenance should be performed on the WDC.

### Diagnostics

6.03 WDC diagnostic software is under development and not released for production at this manual revision.

### Diagnostic Commands

6.04 The command bytes listed in Table 5-4 describe a group of command bytes, 08H through 11H, reserved for diagnostic operation codes. The following paragraphs describe the individual diagnostic commands.

### Command Parameter Block

6.05 The command parameter block used with the diagnostic commands refers to absolute disk address of:

(1) Unit,

(2) Cylinder,

(3) Head,

(4) Sector.

rather than logical addresses defined in the *normal* commands. The organization of the CPB for diagnostic commands is tabulated in Table 6-1.

6.06 *Unit Number* – This defines the logical unit number of the disk drive. Option jumpers on each drive define the individual disk. The allowed range of unit is 0 to 3.

Table 6-1 – Command Parameter Block Address Assignments

| Location | Description |
|---|---|
| CPB+0 | Command Byte. |
| CPB+1 | Unit Number. |
| CPB+2 | Head and Sector. |
| CPB+3 | Cylinder (LS Bits). |
| CPB+4 | Cylinder (MS Bits). |
| CPB+5 | Byte of 00. (1) |
| CPB+6 | Byte of 00. (1) |
| CPB+7 | Block Count. |
| CPB+8 | System RAM Address Bits 0-7. |
| CPB+9 | System RAM Address Bits 8-15. |
| CPB+10 | System RAM Address Bits 16-19. |
| CPB+11 | Byte of 00. (1) |
| CPB+12 | Status Block Pointer Bits 0-7. |
| CPB+13 | Status Block Pointer Bits 8-15. |
| CPB+14 | Status Block Pointer Bits 16-19. |
| CPB+15 | Byte of 00. (1) |

Note:

(1) Reserved for expansion.

6.07 *Head and Sector Number* – This byte performs two functions:

(1) Bits 7-6 select head 0-3.

(2) Bits 5-1 define the absolute sector of the drive, based on 256 bytes per sector.

(3) Bit 0 is vacant and must be set to 0.

6.08 *Block Count* – This byte defines the number of 256 byte blocks to transfer in the currently specified operation.

6.09 *System RAM Address* – same as controller programming refer to 5.15.

6.10 *Status Block Pointer* – same as controller programming refer to 5.16.

### Command Descriptions

6.11 *Seek Cylinder Only* – This command causes the heads to be positioned over the absolute cylinder address specified by the Command Parameter Block (CPB). The head specified by the command will also be selected.

6.12 *Restore Drives to Cylinder 0* – This command causes the drive specified by Unit to reposition to absolute cylinder 0.

6.13 *Input WDC RAM* – The contents of the entire WDC RAM will be input to the specified System RAM Address. The Block Count should be set to 18H to input the entire 6144 bytes.

6.14 *Output Data to WDC Buffer* – The data block starting at the location specified by System RAM Address will be output to the Buffer portion of the WDC RAM. The Block Count should be set to 17H to load the entire 5888 byte buffer.

6.15 *Input Data from WDC Buffer* – The contents of the WDC Buffer portion of WDC RAM will be input to the specified System RAM Address. The Block Count should be set to 17H to input the entire 5888 bytes of buffer.

6.16 *Input Alternate Sector Table* – The contents of the WDC Alternate Sector Table for the specified unit will be input starting at the specified System RAM Address. The Block Count should be set to 1 to input the alternate sector table.

6.17 The alternate sector table contains the absolute disk address of 4k disk blocks which have been reassigned to the reserved alternate area. The table consists of 24 entries of 4 bytes each, starting at the beginning of the table. The 4 byte group contains the following information about the disk block which was reassigned.

(1) Byte 0 — Cylinder Number, Bits 8-16.

(2) Byte 1 — Cylinder Number, Bits 0-7.

(3) Byte 2 — Head Number.

(4) Byte 3 — Disk Block Number (either 0 or 10H).

The end of the table is indicated by the value 0E5H in byte 0 of an entry set, or 24 sets, which ever occurs first.

6.18 The position of the 4 byte group in the table implies the disk location where the alternate has been reassigned. The reassignment area begins on cylinder 1, head 0, block 0, and continues through cylinder 3, head 3, block 10H.

6.19 If a 4 byte group has the value 0FEH assigned to each of the 4 bytes then the alternate block implied by this location in the table has been found to be bad, and subsequently skipped.

6.20 *NOP* – No operation is performed.

6.21 *Seek/Read at Absolute Disk Address* – The number of disk sectors specified by Block Count is read from the disk and input at the address specified by System RAM Address. The starting disk address is specified by Head, Sector, Cylinder and Unit. The Block Count must be selected so that:

(1) Block Count in range of 1 to 10H, inclusive.

(2) The arithmetic sum of Sector + Block Count must not exceed 3FH.

6.22 *Seek/Write at Absolute Disk Address* – Data is transferred to the disk at the specified absolute disk address. The same restriction for Block Count as specified in the description of Seek/Read apply to Seek/Write.

### Warranty Service

6.23 Codata Systems Corp. Customer Service is available by telephone for assistance in troubleshooting and recommendations for repairs. All communications and material should be directed to:

Codata Systems Corp.
Customer Service Manager
285 North Wolfe Road
Sunnyvale, CA. 94086
(408) 735-1744
TWX 171119

### Returning Material for Repair

6.24 The Mainframe Hardware Reference Manual outlines the procedure for returning material.

Table 6-2 – Command Byte Code

| Code | Description |
|---|---|
| 08H | Seek Cylinder and Select Head. |
| 09H | Restore to Cylinder 0. |
| 0AH | Not assigned. |
| 0BH | Input WDC RAM. |
| 0CH | Output Data to WDC Buffer. |
| 0DH | Input Data from WDC Buffer. |
| 0EH | Input Alternate Sector Tables. |
| 0FH | NOP. |
| 10H | Seek/Read at Absolute Disk Address. |
| 11H | Seek/Write at Absolute Disk Address. |

## 7. REFERENCE

### Logic Diagram and Replaceable Parts List

7.01 Figure 7-1 will furnish the service technician with the logic diagram of the Winchester Disk Controller (WDC). Table 7-1 is the replaceable parts list for the WDC indexed by reference designator appearing on the logic diagram. Enough information is furnished so the maintenance technician should be able to purchase replaceable parts from a local supplier or make a substitution if necessary. WDC PCAs, ROMs and I/O cables should be ordered directly from Codata Systems Corp. Customer Service.

### IEEE 796 Microcomputer Bus

7.02 Table 7-2 and 7-3 tabulate connectors P1 and P2 pin assignments for the 796 Bus specification.

7.03 The WDC was developed several years prior to adoption of the IEEE 796 Bus Specification. The logic diagram, Figure 7-1, uses references, mnemonics and conventions in use prior to the 796 Bus specification.

### Technical Manual Revisions

7.04 The following summarizes the change history for this technical manual.

(1) Revision A, initial release, October 1982.

7.05 Codata Systems Corp. makes changes to drawings and products through engineering change notices (ECN)s. Before a change to a product is approved or made:

(1) The implications to systems in the field are determined.

(2) Rework instructions are included for the equipment in the field when appropriate.

Codata Systems Corp. Customer Service receives copies of all ECNs.

7.06 There are no pertinent ECNs affecting this WDC at this manual revision.

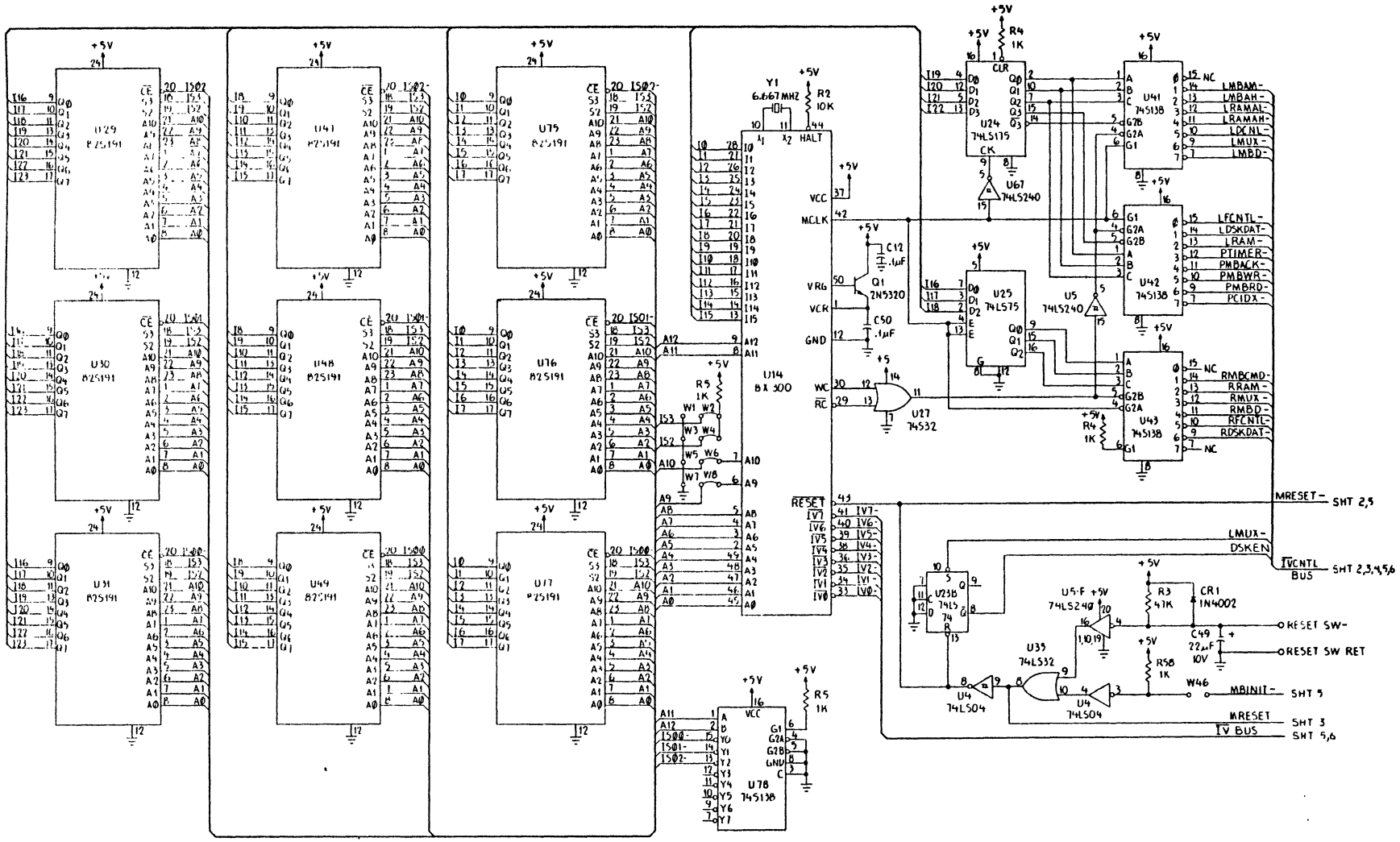



Figure 7-1 — Winchester Disk Controller Logic Diagram

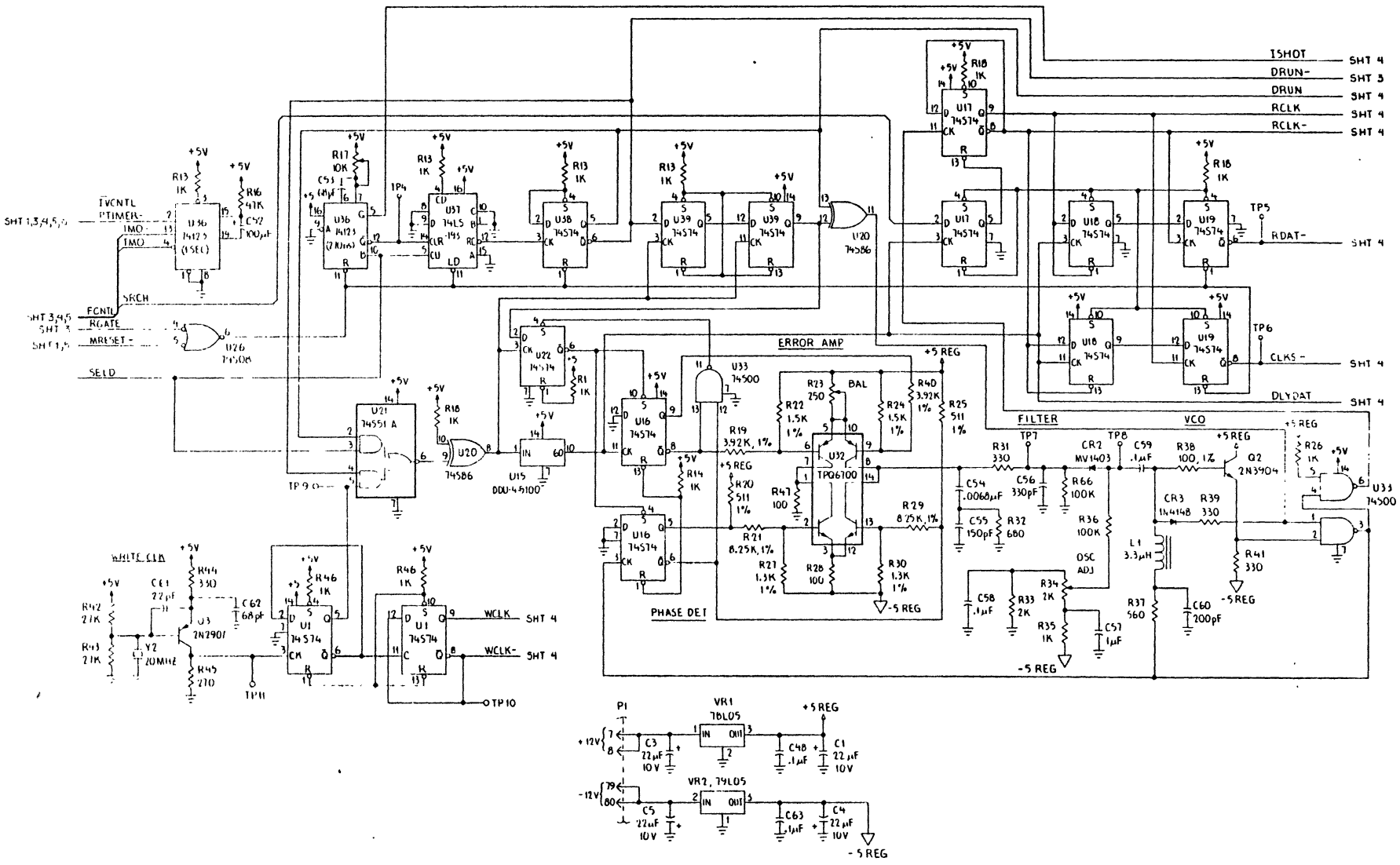



Figure 7-1 — Winchester Disk Controller Logic Diagram (Continued)

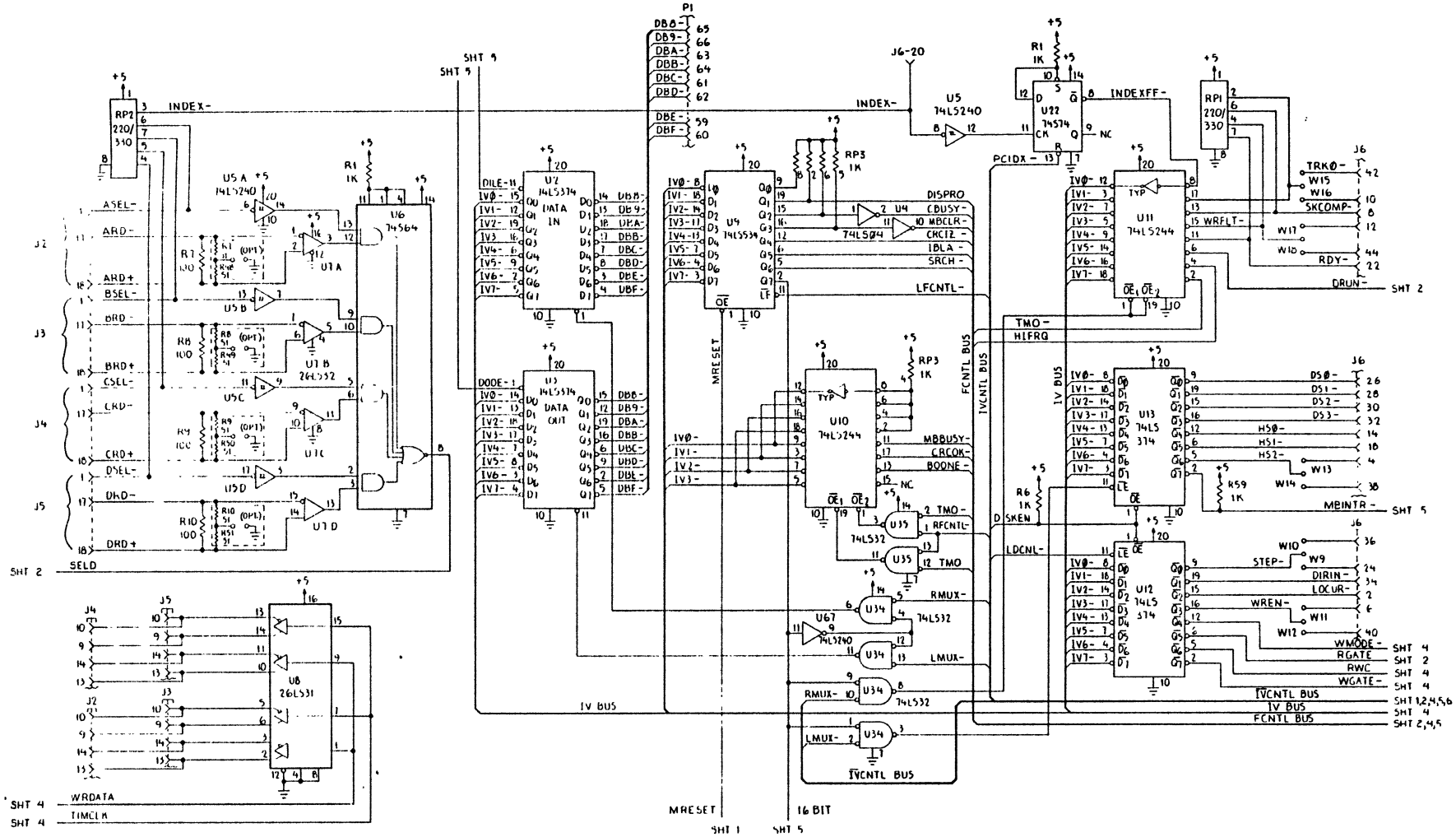



Figure 7-1 — Winchester Disk Controller Logic Diagram (Continued)

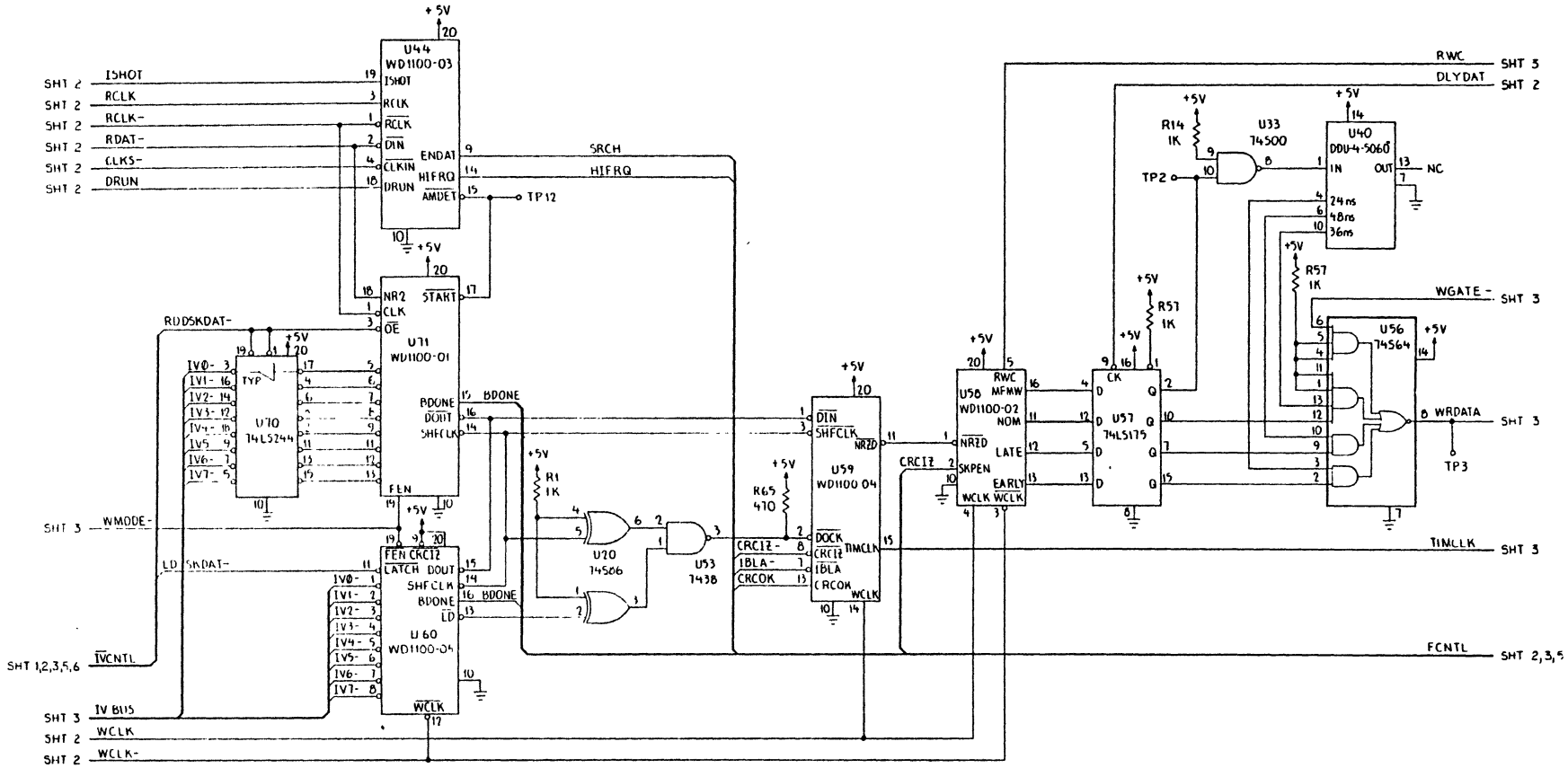



Figure 7-1 — Winchester Disk Controller Logic Diagram (Continued)

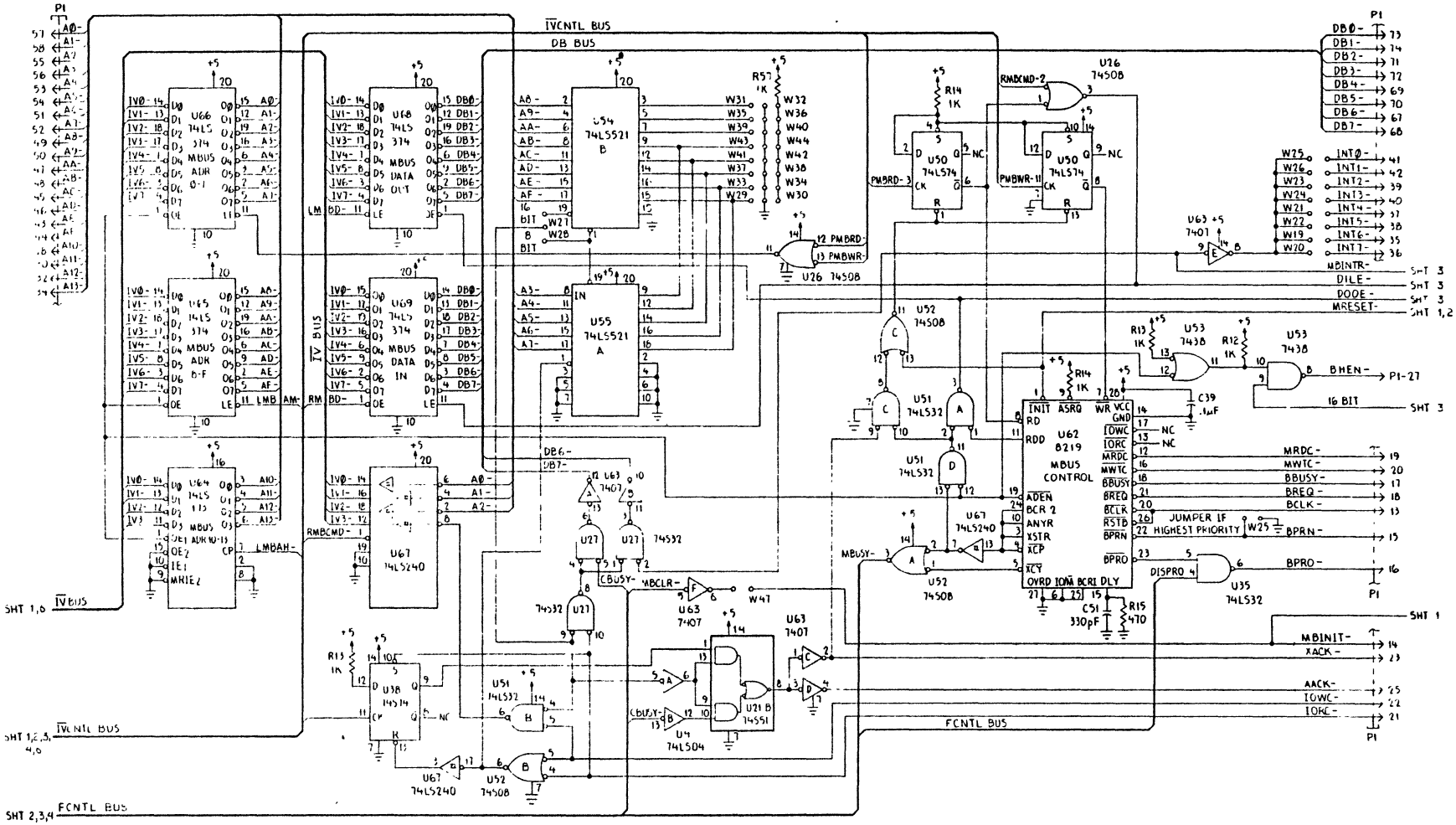
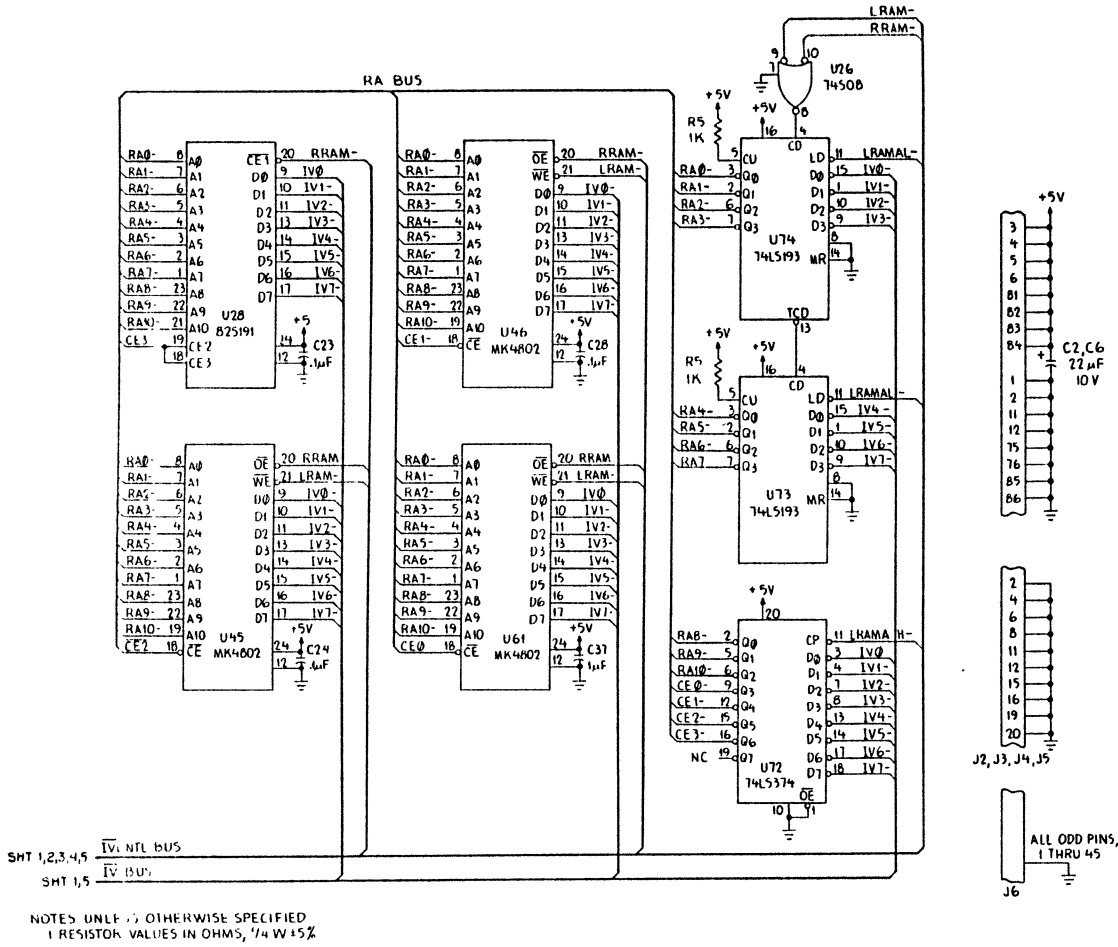



Figure 7-1 — Winchester Disk Controller Logic Diagram (Continued)




| I.C. | LOCATION (SHEET 88) | GND PIN | VCC PIN | UNUSED GATES |
|---|---|---|---|---|
| 7407 | U63(5) | 7 | 14 | -- |
| 7438 | U53(4,5) | 7 | 14 | (4,5 6) |
| 74123 | U36(2) | 8 | 16 | -- |
| 74LS04 | U4(1,3,5) | 7 | 14 | -- |
| 74LS32 | U34(3), U35(3,5), U51(5) | 7 | 14 | -- |
| 74LS74 | U23(1), U50(5) | 7 | 14 | U23(1,2,3,4,5,6) |
| 74LS75 | U25(1) | 12 | 5 | -- |
| 74LS173 | U64(5) | 8 | 16 | -- |
| 74LS175 | U24(1), U57(4) | 8 | 16 | -- |
| 74LS193 | U37(2), U73(6), U74(6) | 8 | 16 | -- |
| 74LS240 | U5(1,3), U67(1,3,5) | 10 | 20 | U5(2,4) |
| 74LS244 | U11(3), U70(4), U40(3) | 10 | 20 | -- |
| 74LS374 | U2(3), U3(3), U12(3), U13(3), U65(5), U66(5), U68(5), U69(5), U72(6) | 10 | 20 | -- |
| 74LS521 | U54(5), U55(5) | 10 | 20 | -- |
| 74LS534 | U9(3) | 10 | 20 | -- |
| 74S00 | U33(2,4) | 7 | 14 | -- |
| 74S04 | U26(2,5 6), U52(5) | 7 | 14 | U5.(8,9,10) |
| 74S32 | U27(1,5) | 7 | 14 | -- |
| 74S51 | U21(2) | 7 | 14 | -- |
| 74S64 | U6(3), U56(4) | 7 | 14 | -- |
| 74S74 | U1(2), U16(2), U17(2), U18(2), U19(2), U22(2,3), U38(2,5), U39(2) | 7 | 14 | -- |
| 74S86 | U20(2,4) | 7 | 14 | -- |
| 74S138 | U41(3), U42(3), U43(3), U78(3) | 8 | 16 | -- |
| MK4802-1 | U45(6), U46(6), U61(6) | 12 | 24 | -- |
| 8219 | U62(5) | 14 | 28 | -- |
| 825191 | U28(6), U29(3), U30(3), U31(3), U47(3), U48(3), U49(3), U75(3), U76(3), U77(3) | 12 | 24 | -- |
| 26LS31 | U8(3) | 8 | 16 | -- |
| 26LS32 | U7(3) | 8 | 16 | -- |
| WD1100-01 | U71(4) | 10 | 20 | -- |
| WD1100-02 | U58(4) | 10 | 20 | -- |
| WD1100-03 | U44(4) | 10 | 20 | -- |
| WD1100-04 | U59(4) | 10 | 20 | -- |
| WD1100-05 | U60(4) | 10 | 20 | -- |
| 8 X 300 | U14(1) | 12 | 37 | -- |
| 220/330 RP | RP1(3), RP2(3) | 8 | 1 | RP1(3)(4), RP2(3) |
| 1K RP | RP3 | -- | 1 | (3) (7) |
| DDU-4-5060 | U40(4) | 7 | 14 | -- |
| DDU-4-5160 | U15(2) | 7 | 14 | -- |

Figure 7-1 — Winchester Disk Controller Logic Diagram (Continued)

## Table 7-1 — Winchester Disk Controller — Replaceable Parts List

| Reference | Description | Manufacturer | Manufacturer's Part Number | Codata Part Number |
|---|---|---|---|---|
| | PCA: Winchester Controller | Codata Sys | 92-1011-01 | 92-1011-01 |
| C 01 | C: Fxd Tant 25V 10% 22uF | Sprague | 199D226X0025AB | 18-0197-02 |
| C 02 | C: Fxd Tant 25V 10% 22uF | Sprague | 199D226X0025AB | 18-0197-02 |
| C 03 | C: Fxd Tant 25V 10% 22uF | Sprague | 199D226X0025AB | 18-0197-02 |
| C 04 | C: Fxd Tant 25V 10% 22uF | Sprague | 199D226X0025AB | 18-0197-02 |
| C 05 | C: Fxd Tant 25V 10% 22uF | Sprague | 199D226X0025AB | 18-0197-02 |
| C 06 | C: Fxd Tant 25V 10% 22uF | Sprague | 199D226X0025AB | 18-0197-02 |
| C 07 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 08 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 09 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 10 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 11 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 12 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 13 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 14 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 15 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 16 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 17 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 18 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 19 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 20 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 21 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 22 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 23 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 24 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 25 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 26 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 27 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 28 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 29 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 30 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 31 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 32 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 33 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 34 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 35 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |

Table 7-1 — Winchester Disk Controller — Replaceable Parts List (Continued)

| Reference | Description | Manufacturer | Manufacturer's Part Number | Codata Part Number |
|---|---|---|---|---|
| C 36 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 37 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 38 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 39 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 42 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 43 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 44 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 45 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 46 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 47 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 48 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 49 | C: Fxd Tant 25V 10% 22uF | Sprague | 199D226X0025AB | 18-0197-02 |
| C 50 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 51 | C: Fxd Mica 50V 10% 330pF | CD | CM05FD331J03 | 18-0052-01 |
| C 52 | C: Fxd Al 10V 10% 100uF | Kemet | T110C107K010AS | 18-0400-01 |
| C 53 | C: Fxd Cer 50V 10% 68pF | CD | CM04FD101J03 | 18-0036-01 |
| C 54 | C: Fxd Poly 50V 10% 0.0068uF | Panasonic | ECQ-N1682KZ | 18-0092-01 |
| C 55 | C: Fxd Mica 50V 10% 150pF | CD | CD15FD151J03 | 18-0044-01 |
| C 56 | C: Fxd Mica 50V 10% 330pF | CD | CM05FD331J03 | 18-0052-01 |
| C 57 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 58 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 59 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 60 | C: Fxd Mica 50V 10% 200pF | CD | CM04FD201J03 | 18-0047-01 |
| C 61 | C: Fxd Cer 50V 10% 22pF | Erie | 8131-050-X7RD-224K | 18-0024-01 |
| C 62 | C: Fxd Cer 50V 10% 68pF | CD | CM04FD101J03 | 18-0036-01 |
| C 63 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| C 64 | C: Fxd Cer 50V 10% 0.1uF | Centralab | CY20C104M | 18-0122-01 |
| CR 01 | Diode: Switch 1N4002 | Motorola | 1N4002 | 16-0001-01 |
| CR 02 | Diode: Tuning | Motorola | MV1403 | 16-0007-01 |
| CR 03 | Diode: Switch 1N4148 | Motorola | 1N4148 | 16-0006-01 |
| L 01 | Inductor: 3.3 uH | Miller | 9310-26/3.9 | 30-0003-01 |
| Q 01 | Xstr: NPN Power 2N5320 | Motorola | 2N5320 | 16-1004-01 |
| Q 02 | Xstr: NPN Switch 2N3904 | Motorola | 2N3904 | 16-1002-01 |
| Q 03 | Xstr: PNP General 2N2907 | Motorola | 2N2907 | 16-1001-01 |

Table 7-1 — Winchester Disk Controller — Replaceable Parts List (Continued)

| Reference | Description | Manufacturer | Manufacturer's Part Number | Codata Part Number |
|---|---|---|---|---|
| R 01 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 02 | R: Fxd CF 0.25W 5% 10k Ohm | Rohm | RC07GF103J | 20-0096-01 |
| R 03 | R: Fxd CF 0.25W 5% 47k Ohm | Rohm | RC07GF473J | 20-0112-01 |
| R 04 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 05 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 06 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 07 | R: Fxd CF 0.25W 5% 100 Ohm | Rohm | RC07GF101J | 20-0048-01 |
| R 08 | R: Fxd CF 0.25W 5% 100 Ohm | Rohm | RC07GF101J | 20-0048-01 |
| R 09 | R: Fxd CF 0.25W 5% 100 Ohm | Rohm | RC07GF101J | 20-0048-01 |
| R 10 | R: Fxd CF 0.25W 5% 100 Ohm | Rohm | RC07GF101J | 20-0048-01 |
| R 12 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 13 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 14 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 15 | R: Fxd CF 0.25W 5% 470 Ohm | Rohm | RC07GF471J | 20-0064-01 |
| R 16 | R: Fxd CF 0.25W 5% 47k Ohm | Rohm | RC07GF473J | 20-0112-01 |
| R 17 | R: Var MF 0.25W 20% 10k Ohm | CTS | 752-207-10K | 20-2004-01 |
| R 18 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 19 | R: Fxd MF 0.25W 1% 3.92k Ohm | Panasonic | 5043E0392K0F | 20-3008-01 |
| R 20 | R: Fxd MF 0.25W 1% 511 Ohm | Bourns | RN5505110F | 20-3005-01 |
| R 21 | R: Fxd MF 0.25W 1% 8.25k Ohm | Bourns | RN5508251F | 20-3009-01 |
| R 22 | R: Fxd MF 0.25W 1% 1.5k Ohm | Dale | CCF-55-1.501F | 20-3007-01 |
| R 23 | R: Var MF 0.25W 20% 250 Ohm | Beckman | 68X250 | 20-2002-01 |
| R 24 | R: Fxd MF 0.25W 1% 1.5k Ohm | Dale | CCF-55-1.501F | 20-3007-01 |
| R 25 | R: Fxd MF 0.25W 1% 511 Ohm | Bourns | RN5505110F | 20-3005-01 |
| R 26 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 27 | R: Fxd MF 0.25W 1% 1.3k Ohm | Bourns | RN5501301F | 20-3006-01 |
| R 28 | R: Fxd MF 0.25W 1% 100 Ohm | Dale | 5BB-100-5 | 20-3004-01 |
| R 29 | R: Fxd MF 0.25W 1% 8.25k Ohm | Bourns | RN5508251F | 20-3009-01 |
| R 30 | R: Fxd MF 0.25W 1% 1.3k Ohm | Bourns | RN5501301F | 20-3006-01 |
| R 31 | R: Fxd CF 0.25W 5% 330 Ohm | Rohm | RC07GF331J | 20-0060-01 |
| R 32 | R: Fxd CF 0.25W 5% 680 Ohm | Rohm | RC07GF681J | 20-0068-01 |
| R 33 | R: Fxd CF 0.25W 5% 2k Ohm | Rohm | RC07GF202J | 20-0079-01 |
| R 34 | R: Var MF 0.25W 20% 2k Ohm | CTS | 752-207-2K | 20-2003-01 |
| R 35 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 36 | R: Fxd CF 0.25W 5% 100k Ohm | Rohm | RC07GF104J | 20-0120-01 |
| R 37 | R: Fxd CF 0.25W 5% 560 Ohm | Rohm | RC07GF561J | 20-0066-01 |

Figure 7-1 — Winchester Disk Controller Logic Diagram (Continued)

| Reference | Description | Manufacturer | Manufacturer's Part Number | Codata Part Number |
|---|---|---|---|---|
| R 38 | R: Fxd MF 0.25W 1% 100 Ohm | Dale | 5BB-100-5 | 20-3004-01 |
| R 39 | R: Fxd CF 0.25W 5% 330 Ohm | Rohm | RC07GF331J | 20-0060-01 |
| R 40 | R: Fxd MF 0.25W 1% 3.92k Ohm | Panasonic | 5043E0392K0F | 20-3008-01 |
| R 41 | R: Fxd CF 0.25W 5% 330 Ohm | Rohm | RC07GF331J | 20-0060-01 |
| R 42 | R: Fxd CF 0.25W 5% 27k Ohm | Rohm | RC07GF273J | 20-0106-01 |
| R 43 | R: Fxd CF 0.25W 5% 27k Ohm | Rohm | RC07GF273J | 20-0106-01 |
| R 44 | R: Fxd CF 0.25W 5% 330 Ohm | Rohm | RC07GF331J | 20-0060-01 |
| R 45 | R: Fxd CF 0.25W 5% 270 Ohm | Rohm | RC07GF271J | 20-0058-01 |
| R 46 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 47 | R: Fxd MF 0.25W 1% 100 Ohm | Dale | 5BB-100-5 | 20-3004-01 |
| R 57 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 58 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 59 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 64 | R: Fxd CF 0.25W 5% 1k Ohm | Rohm | RC07GF102J | 20-0072-01 |
| R 65 | R: Fxd CF 0.25W 5% 470 Ohm | Rohm | RC07GF471J | 20-0064-01 |
| R 66 | R: Fxd CF 0.25W 5% 100k Ohm | Rohm | RC07GF104J | 20-0120-01 |
| RP 01 | R: SIP MF 0.25W 5% 220/330 Ohm | CTS | 750-85-R220/330 | 20-1007-01 |
| RP 02 | R: SIP MF 0.25W 5% 220/330 Ohm | CTS | 750-85-R220/330 | 20-1007-01 |
| RP 03 | R: SIP MF 0.25W 5% 1k Ohm | Dale | MSP08A-01-1K-2 | 20-1008-01 |
| U 01 | IC: Dual D-Type Flip Flop | TI | SN74S74N | 17-3074-01 |
| U 02 | IC: Octal D-Type Flip Flop | TI | SN74LS374N | 17-1374-01 |
| U 03 | IC: Octal D-Type Flip Flop | TI | SN74LS374N | 17-1374-01 |
| U 04 | IC: Hex Inverters | TI | SN74LS04N | 17-1004-01 |
| U 05 | IC: Octal Buffer | TI | SN74LS240N | 17-1240-01 |
| U 06 | IC: 4-2-3-2 In And-Or-Inv | TI | SN74S64N | 17-3064-01 |
| U 07 | IC: Quad Line Receiver | AMD | AM26LS32 | 17-8013-01 |
| U 08 | IC: Quad Line Driver | AMD | AM26LS31 | 17-8024-01 |
| U 09 | IC: Octal D-Type Flip Flop | TI | SN74LS534N | 17-1534-01 |
| U 10 | IC: Octal Buffer | TI | SN74LS240N | 17-1240-01 |
| U 11 | IC: Octal Buffer | TI | SN74LS244N | 17-1244-01 |
| U 12 | IC: Octal D-Type Flip Flop | TI | SN74LS374N | 17-1374-01 |
| U 13 | IC: Octal D-Type Flip Flop | TI | SN74LS374N | 17-1374-01 |
| U 14 | IC: Processor | Fairchild | 8X300 | 17-8023-01 |
| U 15 | Delay Line: | Data Delay | DDU-4-5100 | 19-4002-01 |
| U 16 | IC: Dual D-Type Flip Flop | TI | SN74S74N | 17-3074-01 |

Table 7-1 — Winchester Disk Controller — Replaceable Parts List (Continued)

| Reference | Description | Manufacturer | Manufacturer's Part Number | Codata Part Number |
|---|---|---|---|---|
| U 17 | IC: Dual D-Type Flip Flop | TI | SN74S74N | 17-3074-01 |
| U 18 | IC: Dual D-Type Flip Flop | TI | SN74S74N | 17-3074-01 |
| U 19 | IC: Dual D-Type Flip Flop | TI | SN74S74N | 17-3074-01 |
| U 20 | IC: Quad 2-In Exclusive Or | TI | SN74S86N | 17-3086-01 |
| U 21 | IC: And-Or-Inv | TI | SN74S51N | 17-3051-01 |
| U 22 | IC: Dual D-Type Flip Flop | TI | SN74S74N | 17-3074-01 |
| U 23 | IC: Dual D-Type Flip Flop | TI | SN74LS74N | 17-1074-01 |
| U 24 | IC: Quad D Flip Flop | TI | SN74LS175N | 17-1175-01 |
| U 25 | IC: 4-Bit Bistable Latches | TI | SN74LS75N | 17-1075-01 |
| U 26 | IC: Quad 2-In And | TI | SN74S08N | 17-3008-01 |
| U 27 | IC: Quad 2-In Or | TI | SN74S32N | 17-3032-01 |
| U 30 | IC: Read Only Memory ROM1 HX2 | Codata Sys | 27-0025-01 | 27-0025-01 |
| U 31 | IC: Read Only Memory ROM0A HX2 | Codata Sys | 27-0028-01 | 27-0028-01 |
| U 32 | IC: Quad Xstr | Motorola | TPQ-6700 | 17-4001-01 |
| U 33 | IC: Quad 2-In Nand | TI | SN74S00N | 17-3000-01 |
| U 34 | IC: 8-In Nand | TI | SN74LS32N | 17-1032-01 |
| U 35 | IC: 8-In Nand | TI | SN74LS32N | 17-1032-01 |
| U 36 | IC: Dual Monostable | TI | SN74123N | 17-0123-01 |
| U 37 | IC: Synchronous Dual Clock Cntr | TI | SN74LS193N | 17-1193-01 |
| U 38 | IC: Dual D-Type Flip Flop | TI | SN74S74N | 17-3074-01 |
| U 39 | IC: Dual D-Type Flip Flop | TI | SN74S74N | 17-3074-01 |
| U 40 | Delay Line: | Data Delay | DDU-4-5060 | 19-4001-01 |
| U 41 | IC: 3-To-8 Line Dec/Mux | TI | SN74S138N | 17-3138-01 |
| U 42 | IC: 3-To-8 Line Dec/Mux | TI | SN74S138N | 17-3138-01 |
| U 43 | IC: 3-To-8 Line Dec/Mux | TI | SN74S138N | 17-3138-01 |
| U 44 | IC: AM Detector | Disital | WD1100-03 | 17-8020-01 |
| U 45 | IC: Random Access Memory 2k x 8 | Fujitsu | MK4802-1 | 17-7010-01 |
| U 46 | IC: Random Access Memory 2k x 8 | Fujitsu | MK4802-1 | 17-7010-01 |
| U 48 | IC: Read Only Memory ROM1 HX1 | Codata Sys | 27-0026-01 | 27-0026-01 |
| U 49 | IC: Read Only Memory ROM0A HX1 | Codata Sys | 27-0029-01 | 27-0029-01 |
| U 50 | IC: Dual D-Type Flip Flop | TI | SN74LS74N | 17-1074-01 |
| U 51 | IC: 8-In Nand | TI | SN74LS32N | 17-1032-01 |
| U 52 | IC: Quad 2-In And | TI | SN74S08N | 17-3008-01 |
| U 53 | IC: Quad 2-In Nand | TI | SN7438N | 17-0038-01 |
| U 54 | IC: Octal Comparator | Fairchild | 74F521 | 17-6015-01 |
| U 55 | IC: Octal Comparator | Fairchild | 74F521 | 17-6015-01 |
| U 56 | IC: 4-2-3-2 In And-Or-Inv | TI | SN74S64N | 17-3064-01 |

Table 7-1 – Winchester Disk Controller – Replaceable Parts List (Continued)

| Reference | Description | Manufacturer | Manufacturer's Part Number | Codata Part Number |
|---|---|---|---|---|
| U 57 | IC: Quad D Flip Flop | TI | SN74LS175N | 17-1175-01 |
| U 58 | IC: MFM Generator | Digital | WD1100-02 | 17-8019-01 |
| U 59 | IC: CRC Generator/Checker | Digital | WD1100-04 | 17-8021-01 |
| U 60 | IC: Parallel/Serial Converter | Digital | WD1100-05 | 17-8022-01 |
| U 61 | IC: Random Access Memory 2k x 8 | Fujitsu | MK4802-1 | 17-7010-01 |
| U 62 | IC: Multibus Controller | Intel | 8219 | 17-8008-01 |
| U 63 | IC: Hex Buffer | TI | SN7407N | 17-0007-01 |
| U 64 | IC: 4-Bit D-Type Register | TI | SN74LS173N | 17-1173-01 |
| U 65 | IC: Octal D-Type Flip Flop | TI | SN74LS374N | 17-1374-01 |
| U 66 | IC: Octal D-Type Flip Flop | TI | SN74LS374N | 17-1374-01 |
| U 67 | IC: Octal Buffer | TI | SN74LS240N | 17-1240-01 |
| U 68 | IC: Octal D-Type Flip Flop | TI | SN74LS374N | 17-1374-01 |
| U 69 | IC: Octal D-Type Flip Flop | TI | SN74LS374N | 17-1374-01 |
| U 70 | IC: Octal Buffer | TI | SN74LS244N | 17-1244-01 |
| U 71 | IC: Serial-To-Parallel Convertr | Western | WD1100-01 | 17-8018-01 |
| U 72 | IC: Octal D-Type Flip Flop | TI | SN74LS374N | 17-1374-01 |
| U 73 | IC: Synchronous Dual Clock Cntr | TI | SN74LS193N | 17-1193-01 |
| U 74 | IC: Synchronous Dual Clock Cntr | TI | SN74LS193N | 17-1193-01 |
| U 76 | IC: Read Only Memory ROM1 HX0 | Codata Sys | 27-0027-01 | 27-0027-01 |
| U 77 | IC: Read Only Memory ROM0A HX0 | Codata Sys | 27-0030-01 | 27-0030-01 |
| U 78 | IC: 3-To-8 Line Dec/Mux | TI | SN74S138N | 17-3138-01 |
| VR 01 | IC: +5Vdc Regulator | National | LM78L05 | 16-2000-01 |
| VR 02 | IC: -5Vdc Regulator | National | LM79L05 | 16-2001-01 |
| Y 01 | Xtal: 0.0005% 6.667 Mhz | M-Tron | HC-18/V | 26-0005-01 |
| Y 02 | Xtal: 0.0005% 20 MHz | M-Tron | HC-18/V | 26-0006-01 |
| | PCA: Winchester Controller | Codata Sys | 92-1011-02 | 92-1011-02 |
| R 07 | R: Fxd CF 0.25W 5% 51 Ohm | Rohm | RC07GF510J | 20-0041-01 |
| R 08 | R: Fxd CF 0.25W 5% 51 Ohm | Rohm | RC07GF510J | 20-0041-01 |
| R 09 | R: Fxd CF 0.25W 5% 51 Ohm | Rohm | RC07GF510J | 20-0041-01 |
| R 10 | R: Fxd CF 0.25W 5% 51 Ohm | Rohm | RC07GF510J | 20-0041-01 |
| R 48 | R: Fxd CF 0.25W 5% 51 Ohm | Rohm | RC07GF510J | 20-0041-01 |
| R 49 | R: Fxd CF 0.25W 5% 51 Ohm | Rohm | RC07GF510J | 20-0041-01 |
| R 50 | R: Fxd CF 0.25W 5% 51 Ohm | Rohm | RC07GF510J | 20-0041-01 |
| R 51 | R: Fxd CF 0.25W 5% 51 Ohm | Rohm | RC07GF510J | 20-0041-01 |

Table 7-2 – Pin Assignment of Bus Signals on 796 Bus Board Connector (P1)

| | Pin | (Component Side) | | Pin | (Circuit Side) | |
|---|---|---|---|---|---|---|
| | | Mnemonic | Description | | Mnemonic | Description |
| Power Supplies | 1 | GND | Signal GND | 2 | GND | Signal GND |
| | 3 | +5V | +5Vdc | 4 | +5V | +5Vdc |
| | 5 | +5V | +5Vdc | 6 | +5V | +5Vdc |
| | 7 | +12V | +12Vdc | 8 | +12V | +12Vdc |
| | 9 | | Reserved, bussed | 10 | | Reserved, bussed |
| | 11 | GND | Signal GND | 12 | GND | Signal GND |
| Bus Controls | 13 | BCLK* | Bus Clock | 14 | INIT* | Initialize |
| | 15 | BPRN* | Bus Pri. In | 16 | BPRO* | Bus Pri. Out |
| | 17 | BUSY* | Bus Busy | 18 | BREQ* | Bus Request |
| | 19 | MRDC* | Mem Read Cmd | 20 | MWTC* | Mem Write Cmd |
| | 21 | IORC* | I/O Read Cmd | 22 | IOWC* | I/O Write Cmd |
| | 23 | XACK* | XFER Acknowledge | 24 | INH1* | Inhibit 1 (disable RAM) |
| Bus Controls and Address | 25 | LOCK* | Lock | 26 | INH2* | Inhibit 2 (disable PROM or ROM) |
| | 27 | BHEN* | Byte High Enable | 28 | AD10* | |
| | 29 | CBRQ* | Common Bus Request | 30 | AD11* | Address |
| | 31 | CCLK* | Constant Clk | 32 | AD12* | Bus |
| | 33 | INTA* | Intr Acknowledge | 34 | AD13* | |
| Interrupts | 35 | INT6* | Parallel | 36 | INT7* | Parallel |
| | 37 | INT4* | Interrupt | 38 | INT5* | Interrupt |
| | 39 | INT2* | Requests | 40 | INT3* | Requests |
| | 41 | INT0* | | 42 | INT1* | |
| Address | 43 | ADRE* | | 44 | ADRF* | |
| | 45 | ADRC* | | 46 | ADRD* | |
| | 47 | ADRA* | Address | 48 | ADRB* | Address |
| | 49 | ADR8* | Bus | 50 | ADR9* | Bus |
| | 51 | ADR6* | | 52 | ADR7* | |
| | 53 | ADR4* | | 54 | ADR5* | |
| | 55 | ADR2* | | 56 | ADR3* | |
| | 57 | ADR0* | | 58 | ADR1* | |
| Data | 59 | DATE* | | 60 | DATF* | |
| | 61 | DATC* | | 62 | DATD* | |
| | 63 | DATA* | Data | 64 | DATB* | Data |
| | 65 | DAT8* | Bus | 66 | DAT9* | Bus |
| | 67 | DAT6* | | 68 | DAT7* | |
| | 69 | DAT4* | | 70 | DAT5* | |
| | 71 | DAT2* | | 72 | DAT3* | |
| | 73 | DAT0* | | 74 | DAT1* | |
| Power Supplies | 75 | GND | Signal GND | 76 | GND | Signal GND |
| | 77 | | Reserved, bussed | 78 | | Reserved, bussed |
| | 79 | -12V | -12Vdc | 80 | -12V | -12Vdc |
| | 81 | +5V | +5Vdc | 82 | +5V | +5Vdc |
| | 83 | +5V | +5Vdc | 84 | +5V | +5Vdc |
| | 85 | GND | Signal GND | 86 | GND | Signal GND |

Notes:

(1) All Reserved pins are reserved for future use and should not be used if upward compatibility is desired.

Table 7-3 – Pin Assignment of Bus Signals on 796 Bus Board Connector (P2)

| | Pin | (Component Side) | | Pin | (Circuit Side) | |
|---|---|---|---|---|---|---|
| | | Mnemonic | Description | | Mnemonic | Description |
| | 1 | | Reserved, Not Bussed | 2 | | Reserved, Not Bussed |
| | 3 | | Reserved, Not Bussed | 4 | | Reserved, Not Bussed |
| | 5 | | Reserved, Not Bussed | 6 | | Reserved, Not Bussed |
| | 7 | | Reserved, Not Bussed | 8 | | Reserved, Not Bussed |
| | 9 | | Reserved, Not Bussed | 10 | | Reserved, Not Bussed |
| | 11 | | Reserved, Not Bussed | 12 | | Reserved, Not Bussed |
| | 13 | | Reserved, Not Bussed | 14 | | Reserved, Not Bussed |
| | 15 | | Reserved, Not Bussed | 16 | | Reserved, Not Bussed |
| | 17 | | Reserved, Not Bussed | 18 | | Reserved, Not Bussed |
| | 19 | | Reserved, Not Bussed | 20 | | Reserved, Not Bussed |
| | 21 | | Reserved, Not Bussed | 22 | | Reserved, Not Bussed |
| | 23 | | Reserved, Not Bussed | 24 | | Reserved, Not Bussed |
| | 25 | | Reserved, Not Bussed | 26 | | Reserved, Not Bussed |
| | 27 | | Reserved, Not Bussed | 28 | | Reserved, Not Bussed |
| | 29 | | Reserved, Not Bussed | 30 | | Reserved, Not Bussed |
| | 31 | | Reserved, Not Bussed | 32 | | Reserved, Not Bussed |
| | 33 | | Reserved, Not Bussed | 34 | | Reserved, Not Bussed |
| | 35 | | Reserved, Not Bussed | 36 | | Reserved, Not Bussed |
| | 37 | | Reserved, Not Bussed | 38 | | Reserved, Not Bussed |
| | 39 | | Reserved, Not Bussed | 40 | | Reserved, Not Bussed |
| | 41 | | Reserved, Bussed | 42 | | Reserved, Bussed. |
| | 43 | | Reserved, Bussed | 44 | | Reserved, Bussed. |
| | 45 | | Reserved, Bussed | 46 | | Reserved, Bussed. |
| | 47 | | Reserved, Bussed | 48 | | Reserved, Bussed |
| | 49 | | Reserved, Bussed | 50 | | Reserved, Bussed |
| | 51 | | Reserved, Bussed | 52 | | Reserved, Bussed |
| | 53 | | Reserved, Bussed | 54 | | Reserved, Bussed |
| Address | 55 | ADR16* | Address Bus | 56 | ADR17* | Address Bus |
| | 57 | ADR14* | | 58 | ADR15* | |
| | 59 | | Reserved, Bussed | 60 | | Reserved, Bussed |

Notes:

(1) All Reserved Pins are reserved for future use and should not be used if upwards compatibility is desired.

(2) Pins 1—40 are for "SPECIAL USE". Special uses are defined in categories. Only category No. 1 is currently described in the IEEE 796 Bus Specification. Category No. 1 is unconstrained use. Other categories are expected to include higher performance busses, I/O interfaces, etc.

(3) Pins 41—60 are intended for future address, data and/or other P1-related signals.