CONTROL DATA CORPORATION

CBE PLATO TERMINAL

COMMUNICATIONS PRACTICES

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1.0 INTRODUCTION

PLATO is different. Its telecommunication signals have been optimized for coding efficiency rather than code compatibility. The telecommunication techniques originally developed by the University of Illinois were intended to represent minimum cost in an environment of campus and urban signal distribution, where wideband CATV cables can provide very low cost communications to classroom clusters of terminals through the medium of binary data embedded in television video signals.

It became evident as PLATO networks expanded beyond campus and urban boundaries that the original communication system architecture was incompatible with many industry standard data transmission techniques, character codes and signalling rates. Steps were taken by Control Data in 1976 to minimize these differences and to thereby reduce the costs of communication. Both the original architecture and the revised architecture are described below.

In the systems descriptions that follow, the word "output" always refers to data signals originating in the CYBER host processor. The word "input" always refers to signals originating in a PLATO terminal unit.

2.0 COMMUNICATION ARCHITECTURE EVOLUTION

The early PLATO system data communication architecture developed by the University of Illinois was designed primarily for minimum cost and maximum performance through the innovative selection of signalling rates, codes, communication circuits, modems and interface circuits. Because the need to utilize industry standards was secondary to cost and performance, the following communication features evolved:

a. 1260 baud signalling rate

b. 21 bit data word output

c. 12 bit data word input

d. inverted signal sense (negative start pulse)

e. marginal interface voltage (5.VDC)

f. metallic circuit (local) modems

With the introduction of widely distributed terminals and clusters of terminals that resulted from the establishment by Control Data of commercial learning centers it became necessary to reduce the cost of data communication. The system features that provided minimum cost in an urban area did not provide minimum cost for geographically dispersed terminals. It was quickly determined that many terminals would have to share each telephone long line if communication costs were to be held within acceptable limits.

The obvious technique for line sharing is multiplexing; however, the 1260 baud rate of the PLATO terminal did not fit into the industry standard which includes integral multiples of 1200 bauds. Some PENRIL Corporation and General DataComm Indust. multiplexers were procured which offered four ports and seven ports respectively for 1260 baud terminals. The PENRIL unit included an internal modem operating at a non-standard bit rate.

The cost per port of 1260 baud terminal multiplexing still appeared excessive. A program was therefore initiated by Control Data to simultaneously reduce multiplexer cost and to permit the use of separate modems having standard EIA RS232C/CCITT V.24 interfaces.

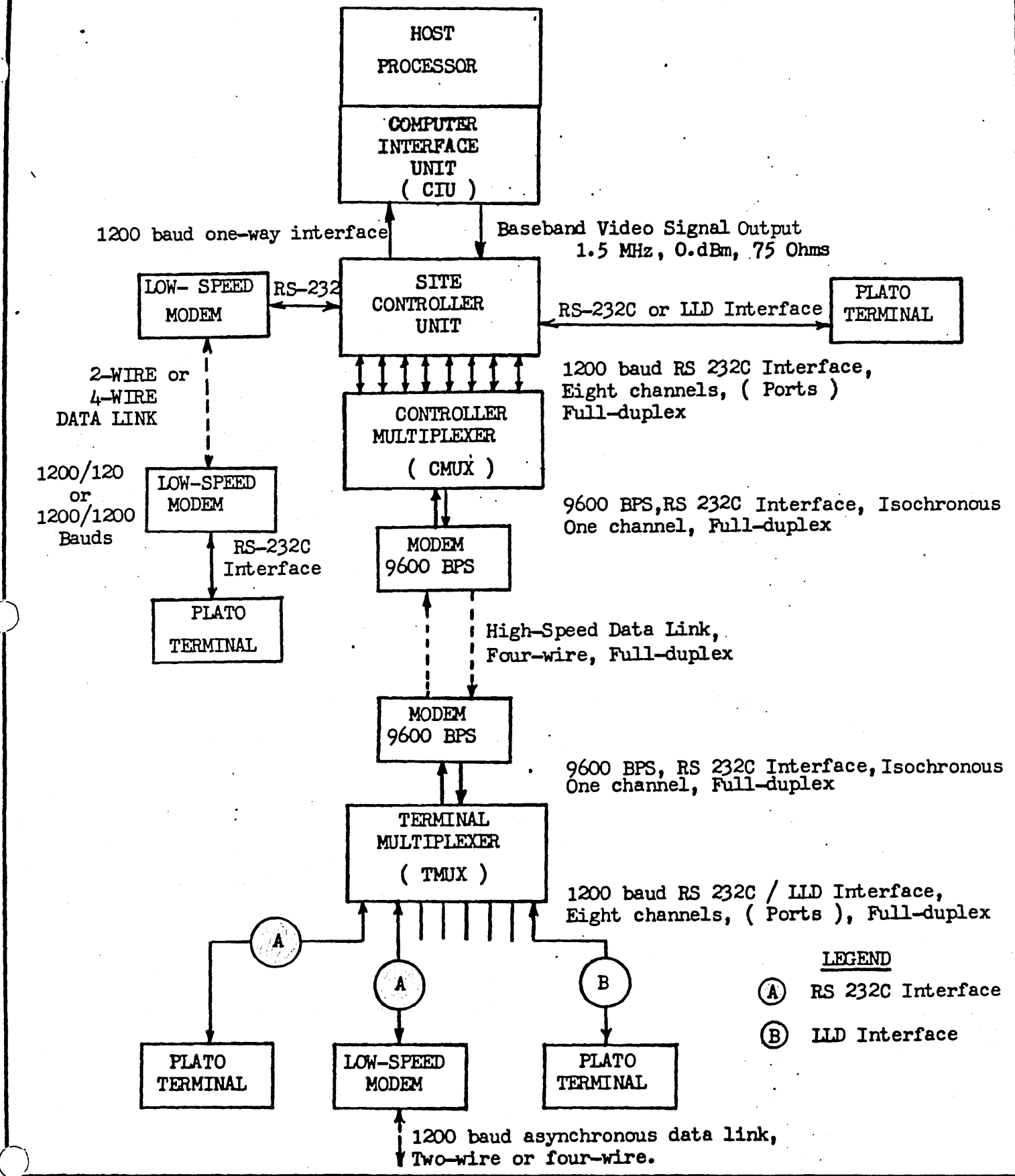
Specifications for low-cost time-division multiplexers were delivered to several manufacturers, and the low bidder was issued a purchase order.

Interface adapters were constructed to invert the signal sense of the terminals and site controllers to conform to the EIA/CCITT standards.

The TV system clock originating in the computer interface unit was adjusted from 60 to 57.14 fields per second to move the data signalling rate from 1260 to 1200 bauds. It was required that all of the PLATO terminal clocks and interfaces be made compatible at the same time. Accordingly, the hardware conversion took place on a weekend in May, 1976. No software conversion was required.

Finally, a family of modules was developed which allows interconnection of all kinds of communications networks except those exhibiting signal delaying characteristics detrimental to PLATO operations. By these means, video circuits, digital data circuits, and voiceband telephone lines can all be connected in tandem, using the appropriate classes of modems, data service units and time division multiplexers to provide service to both isolated and clustered PLATO terminals. Please refer to Figure 1, which illustrates various signal distribution methods.

A more detailed description of the communication equipment operation follows.



CONTROL DATA	SYSTEM CONFIGURATION	CODE IDENT	A	DWG NO	CD
CBE SYSTEMS & SERVICES DIVISION	Figure 1			SHEET	

3.0 THEORY OF OPERATION

In the descriptions that follow, the signal is traced, starting in the CYBER host processor and working outward to the PLATO terminal. The signal is then traced from the terminal keyboard, through the various interfaces, to the host processor. The various transformations of the signal are described in sufficient detail to permit system diagnostics or reconfiguration.

3.1 COMPUTER INTERFACE UNIT (OUTPUT MODE)

The CIU is a peripheral device connected to the I/O channel of a PPU on a Control Data CYBER host processor. The CIU is a buffered time division multiplexer whose internal clock rate is controlled by a quartz crystal. This clock also regulates the flow of data on the processor I/O channel and establishes a timing reference for data communications throughout the network.

The PPU delivers 12-bit bytes to the CIU in bit parallel format, across the I/O interface, at a maximum rate of 1×10^6 bytes per second.

The CIU assembles three 12-bit bytes to form each 20-bit PLATO output word. The words are placed in sequential locations in a buffer memory, to a limit of 1008 word locations. Each location serves a different PLATO terminal in the system. If no data are available for a terminal that memory location is bypassed. It then contains a "blank word" or NO-OP. The buffer memory locations are to be read sequentially by the hardware. All 1008 locations will be scanned, regardless of their status of filled or empty.

When a CIU buffer memory has been filled with 1008 words it is disconnected from the host processor output and made available to a bit serializer circuit associated with the video output signal source. At the same time a second

buffer memory is connected to the processor output to receive data while the first buffer is being emptied. The two CIU buffers automatically alternate as they are filled and emptied.

An (almost) standard NTSC (television) monochrome video field is generated at intervals of 17.5 mS, (57.14 Hz). It includes both horizontal and vertical synchronizing pulses, used as timing references when emptying the CIU buffer memory. Each line of the TV field is divided into 100 time slots, 84 of which are used to carry output data bits.

Bit number one of each data word for all of 1008 terminals is transmitted before bit number two of any terminal. Twelve lines of the TV field are required for all number one bits. The number two bits are carried by the next twelve lines, and so on until bits numbered 20, which occupy the last twelve lines are transmitted, a total of 240 lines. The remainder of the TV field lines and retrace interval are not used for data.

The NTSC video field is transmitted serially at baseband into a 75 ohm coaxial cable. There is no return channel into this coaxial cable, but 32 narrow bandwidth input ports on the CIU are used for that purpose.

The nominal bandwidth required before output modulation is 1.5 MHz. The maximum signalling rate is 1.21 MBPS, but extra bandwidth is required by the synchronizing pulses in the NTSC field.

Once a video field is placed on the coaxial cable by the CIU it must be delivered to demultiplexing devices for signal conversion to the form required by a PLATO terminal. The demultiplexer is called a site controller unit, SCU.

Any number of SCU's, to the limit of 32 may be attached (bridged) to the coaxial cable. The output signal may also be extended by means of CATV cables or microwave channels to distant sites where SCU's are located.

3.2 SITE CONTROLLER UNIT (OUTPUT MODE)

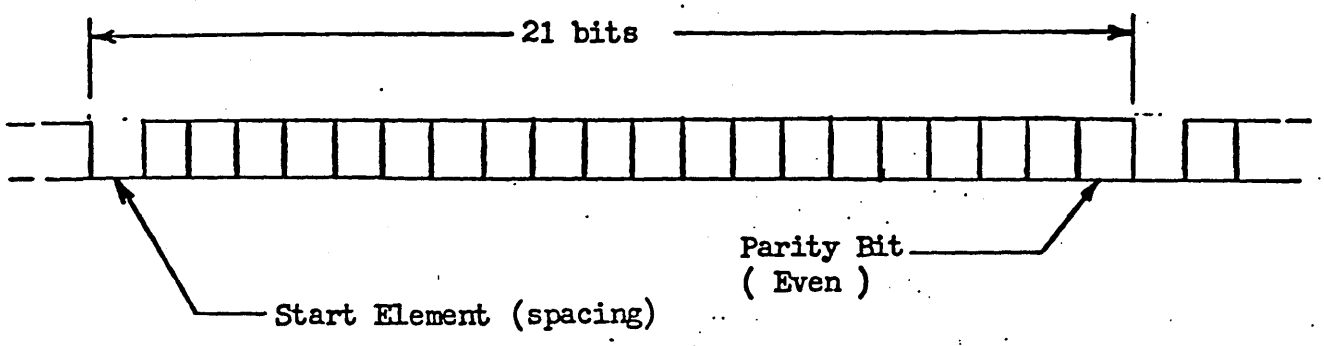
Each site controller is connected by means of a high impedance tap to the output signal cable from the CIU. All site controllers receive every video frame identically, but each SCU is programmed to recognize only the 32 (or fewer) time slots associated with the PLATO terminals served by that SCU. Whereas the data bits are embedded in horizontal lines in the TV fields, the time slots for any specific word appear within vertical boundaries in the TV field.

As data bits for a particular SCU are detected by the SCU, they are distributed sequentially to 32 two-bit shift registers. Here the bits are re-timed so that the serial bit data words for all 32 terminal ports exit simultaneously, (in phase).

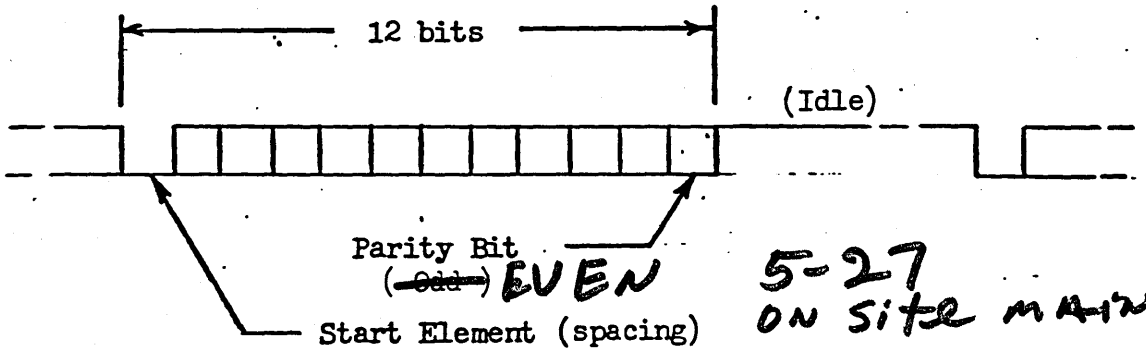
The first bit of each PLATO output word at an SCU port is a start element of logical ZERO polarity. (A spacing signal.) The 20 bits that follow may be ONES and ZEROES in any combination, except that the last bit represents even parity; that is, the number of ONE bits, including the parity bit, must be even. See Figure 2.

At the EIA interface a positive voltage represents a spacing ZERO state, and a negative voltage represents a marking ONE state.

Each start element immediately follows the parity bit of the previous data word. Stop elements are not required, although they are permitted if they are of marking polarity. It is seen that transmission is isochronous, in spite of the use of start elements.



PLATO OUTPUT WORD STRUCTURE, (To Terminal)



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PLATO INPUT WORD STRUCTURE, (From Terminal)

CONTROL DATA CBE SYSTEMS & SERVICES DIVISION	PLATO WORD STRUCTURE Figure 2	CODE IDENT	A	DWG NO SHEET 8	CD

When there is no output data word to be delivered to a PLATO terminal port the SCU generates a blank word consisting of a start element followed by 20 elements of marking polarity. These words are called NO-OPS and are used for time-fill.

Because the NTSC TV field rate is 57.14/sec., each of the 32 ports transmits data at nominally 1200 BPS toward the PLATO terminal. This rate is carefully controlled to remain just outside of, and below, the $\pm$ 0.01 percent standard clock rate tolerance of isochronous (synchronous) data links. The controlled rate range is 1199.2 to 1199.88BPS. At these rates the data bit stream can never exceed the capacity of a standard isochronous data link.

A directly-connected PLATO terminal is tolerant of the reduced signalling rate, as is any asynchronous data link. If, however, it becomes necessary to employ an isochronous (synchronous) data link to convey output signals from the SCU to PLATO terminals, means are required outside of the SCU to periodically insert marking bits between PLATO words. This technique adjusts the bit rate to the synchronous signalling rate standard, which includes integral multiples of 1200 $\pm$ 0.01% BPS. This is normally accomplished by an external multiplexer that is an optional part of the communication system.

The time interval between inserted marking bits will depend on the rate difference between the CIU clock and the data link clock. The inserted marking bits will be passed on to the PLATO terminal where they will be ignored.

Interconnection between the new SCU output ports and the PLATO terminals is accomplished in four ways, as follows:

a. hard-wired dc connection, RS-232C/CCITT V.24

b. long-line driver (LLD) optical isolator

c. FSK long distance modems, RS-232C/CCITT V.24

d. time-division multiplexer, (TDM), RS-232C/CCITT V.24

The LLD is an asynchronous device, used as an alternative to a hard-wired RS-232C connection between the SCU and a PLATO terminal. It is less costly than a local modem, and allows physical separation of the PLATO terminal from the SCU of several thousand feet, without interference resulting from common-mode grounding system noise. The LLD interface employs optical isolators at each receiving point, and a four-wire transmission system, two wires for each direction.

The FSK long distance modems are described in Section 5.2, below. Time division multiplexers are described in Section 4.0, below.

3.3 PLATO TERMINAL, (OUTPUT MODE)

The interface options of the SCU (Paragraph 3.2) are also the options of the terminal. Serial-by-bit 21-bit words arrive at the terminal at the 1200 baud rate established by the SCU. The terminal resynchronizes its crystal-controlled receiving clock divider whenever a start element is recognized. Thereafter it counts bits, looking for start elements at 21-bit intervals. The clocking system provides for mid-bit strobes my means of a divide-by-16 counter that subdivides each data bit and resets on every data signal transition. Although transmission to the terminal from the SCU is isochronous (synchronous), the terminal resynchronizes its deserializer circuit on every data word or NO-OP, in the manner of an asynchronous receiver. This eliminates the need for a separate clock signal across the interface.

The internal circuits of the PLATO terminal analyze the 20 data bits of the output word. Of these bits, one is parity and another is a control bit which indicates the nature of the remaining 18 bits. The 18 may consist of two 9-bit addresses or three 6-bit alphanumeric chracters. The 9-bit addresses specify points on the 512 x 512 display screen.

Whenever the parity check fails, the terminal automatically re-requests the last data sequence from the host processor via the input communication system. If the request fails, the terminal operator must initiate a manual restart at some control point in the program or lesson.

3.4 PLATO TERMINAL, (INPUT MODE)

A PLATO terminal is a full-duplex device. Data and NO-OP's arrive continuously from the SCU, and are not interrupted for input transmissions from the terminal to the SCU.

Input data can originate in the terminal keyboard, the touch panel, the automatic re-request circuit, or in an external attachment to the terminal. The data word, which is 12 bits long, consists of a (ZERO) start element plus a 7-bit character followed by a 3-bit modifier and a parity bit. Odd parity is used. The modifier bits identify the code and source of code.

Unlike the output words, the input words are transmitted asynchronously, (start-stop). Words may be briefly contiguous, in which case there are no stop elements, but under most conditions (marking signal) stop elements appear as time-fill between data words. These are ignored by the SCU.

The interface between the terminal and the SCU provides RS-232C/V.24 and LLD options. Data bits are transmitted serially at any of the following pre-selected rates:

1200 ± 0.1% bauds —

150 ± 0.1% bauds

120 ± 0.1% bauds —

75 ± 0.1% bauds

When the terminal is co-located with the SCU, or when 4-wire full-duplex communication lines are available, the 1200 baud option is recommended to minimize response time.

On two-wire telephone circuits, full-duplex transmission at a reduced input rate is possible, using reverse channel modulation schemes. A rate of 120 bauds is required for compatibility with some older models of PLATO terminals, but standard rates of 150 and 75 bauds are available for use in newer systems.

3.5 SITE CONTROLLER UNIT, (INPUT MODE)

The SCU contains a maximum of 16 input modules, each of which can accommodate two PLATO terminals operating at the same baud rate. The rate options are described in Section 2.4, above.

The SCU contains a buffered multiplexer which performs the following functions:

a. Accepts input data words from 32 ports independently, placing them in 32 four-word buffers.

b. Deletes start elements from input words.

c. Adds five bits of port identification to each input word.

d. Adjusts word parity to include port identification bits.

e. Places each input word in a FIFO (first-in-first-out) buffer.

f. Withdraws each word and transmits it serially-by-bit at 1200 bauds towards the CIU, first adding a start bit.

The interface options include LLD and the modem standard which complies with the conventions of EIA STD RS-232C and CCITT Recommendation V.24, as follows:

LOGICAL	SIGNAL	POLARITY
ONE	MARKING	~~NEGATIVE~~ Pos
ZERO	SPACING	~~POSITIVE~~ Neg

The transmission medium between each SCU and the CIU port assigned to that SCU is a one-way 1200 baud asynchronous circuit. All 32 ports of the SCU are served by this one 1200 baud circuit on a contention basis. Both RS232 and LLD interfaces are provided at the SCU/CIU intercommunication ports.

If too many terminals contend for SCU service, data will be lost and each terminal operator affected must re-submit the keyboard entry. Normally the keyboard duty cycle is low so that the FIFO buffer capacity in the SCU is not exceeded. When data are lost because of buffer contention, the terminal operator is immediately aware of that fact because of the absence of the rapid responses characteristic of PLATO, (typically less than 250 millisecond delay).

3.6 COMPUTER INTERFACE UNIT, (INPUT MODE)

Each PLATO terminal input word arriving at a CIU port from an SCU is 17 bits long, (12 bits plus a 5-bit SCU port identifier). The CIU discards the start element, adds a 5-bit CIU port identifier, and replaces the parity bit with a valid/invalid word "flag" bit. The resulting 21-bit word is placed in a CIU buffer from which it will be read by the CYBER host processor.

Every PLATO terminal is identified to the processor by the ten bits added by the SCU and CIU to each input data word. This is the only identification required by the communications network, although the terminal user must be separately identified for accounting and security purposes. User identification procedures are not described here.

The CIU divides each 21-bit word into two parts for compatibility with the 12-bit I/O requirements of the CYBER host. In two input cycles the host reads the input data and the address of one PLATO terminal. A few milliseconds later the processor responds to the terminal input, transmitting the response via the CIU. This closes the signalling description "loop" which began with the host processor output to the CIU.

4.0 TIME DIVISION MULTIPLEXERS

Several TDM designs have been tested in PLATO service. TDM's are employed between the SCU ports and distant PLATO terminals to reduce the number of telephone lines required. Earlier TDM versions used non-standard interfaces, modems and signalling rates. Later design allow TDM interfaces to run at industry standard signalling rates and to use EIA standard interface signals.