77715975 H

CONTROL DATA CORPORATION

CONTROL DATA®
WREN™ I DISK DRIVE
MODEL 9415

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY
DIAGRAMS
MAINTENANCE
PARTS DATA

MAGNETIC PERIPHERALS, INC.
a Control Data Company

MAINTENANCE MANUAL

REVISION RECORD

REV	DATE	MANUAL/SECTION REVISION STATUS										CHANGE AUTHORITY
		1	2	3	4	5	6	7	8	9	10	
A	ISSUE	A	A	A	A	A	A	A				G. Workman R. Mach
B	dc 84 FEB7	A	A	A	A	B	A	A				PL 59207
C	dc 84 FEB17	A	A	A	A	C	A	A				PL 59211
D	dc 84 APR9	A	A	B	A	C	A	A				PL 59233
E	ii thru vi 84 dc AUG3	B	B	C	B	D	B	B				PL 59282
F	ii and iv 84 dc OCT29	B	B	C	B	D	B	B				PL 59302
G	ii 85 dc JAN24	B	B	D	B	D	B	B				PL 59337
H	ii	B	B	D	B	E	B	B				PL 59387

REVISION I, O, Q, S, X and Z are not used.

Address all comments concerning this publication to the distributor or use the enclosed user comment sheet located in the back of this publication.

PREFACE

This manual provides the information needed to install, operate, maintain, troubleshoot, and refurbish the WREN I DISK DRIVES Model 9415-3 (BJ7D4-A) and Model 9415-5 (BJ7D5-A)

The total content of the Manual is comprised of seven (7) sections, each having a unique publication number and is contained in one volume. The manual's publication number (77715975) should be used when making reference to the WREN I Maintenance Manual.

The following table identifies the contents of this manual:

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EMI NOTICE

WARNING: This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of the FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

SAFETY INSTRUCTIONS

1. The WREN is to be installed in a customer supplied cabinet where the surrounding air does not exceed 46^{o} C.
2. Four (4) 6-32 UNC-2A screws are required for installation.
3. The power requirements are:
   +5 VDC $\pm$3% 1.5 A
   +12 VDC $\pm$5% 2.5 A (4 A for 30 seconds)
4. The power supply must satisfy safety requirements for SELV (Safety Extra Low Voltage) circuits.
5. Service is to be provided only by trained service personnel.
6. The incorporation of the WREN into a customer-supplied cabinet must meet the appropriate safety requirements of the country in which it is to be used (eg. UL, IEC 380).

SICHERHEITSANLEITUNG

1. Das Gerat ist ein Einbaugerat, vorgesehen fur eine maximale Umgebungstemperatur von 46° C.
2. Zur Befestigung des Wren-Drives werden 4 Schrauben 6-32 UNC-2A benotigt.
3. Als Versorgungsspannungen werden benotigt:
   +5 VDC ±3% 1.5 A
   +12 VDC ±5% 2.5 A (4.0 A fur ca. 30 Sek.)
4. Die Versorgungsspannung muss SELV entsprechen.
5. Alle Arbeiten durfen nur von ausgebildetem Servicepersonal durchgefuhrt werden.
6. Der Einbau des Drives muss den Anforderungen gemass DIN IEC 380/VDE 0806/8.81 entsprechen.

WARNING

This product is an electromechanical device which could present hazards if improperly handled. The device should be maintained only by qualified personnel in accordance with instructions contained in this manual and sound safety practices. Careless disassembly or maintenance procedures may result in damage to the device or injury to personnel. Observe all CAUTIONS or WARNINGS attached to the device or contained in this manual.

These WARNINGS and or CAUTIONS are not exhaustive. The manufacturer cannot know in advance all possible maintenance procedures, or tools, which may be devised by persons who choose not to follow the instructions in this manual. Any deviation from the prescribed procedures may entail risks which have not been evaluated by the manufacturer.

Any persons who use a non-approved procedure or tool must satisfy themselves that no injury to personnel, no damage to the device, and no deterioration of device performance will result.

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1.1 INTRODUCTION

The CDC Model 9415 WREN I Disk Drive is a small, low-cost, medium performance, random-access rotating-disk, mass-memory device designed to record and recover data on up to three rigid 5-1/4 inch nonremoveable fixed disk media. The WREN uses low-mass flying read/write heads attached to a precisely controlled rotary positioner.

1.2 GENERAL DESCRIPTION

1.2.1 STANDARD FEATURES

The following standard features of the Model 9415 WREN I Disk Drive are:

- Either Seagate Interface (Model 9415-5) or CDC Interface (Model 9415-3).
- Full data recovery circuitry for drives with CDC interface.
- Sealed disk, head, and actuator chamber.
- No preventive maintenance required.
- LSI circuitry for high reliability.
- Low audible noise for office environments.
- Vertical (side) or horizontal (bottom) mounting.
- Low power consumption.
- Rotary voice-coil actuator.
- Terminators.
- Shock mounts.

1.2.2 OPTIONAL FEATURES

The following optional features (factory-installed only) are available for the WREN I.

- 21 or 35 megabytes rigid fixed-disk data storage capacity for units with CDC interface (Model 9415-3).
- 21.7 or 36.2 megabytes rigid fixed-disk data storage capacity for units with Seagate interface (Model 9415-5).

1.2.3 ACCESSORIES

The following accessories are available for the WREN and must be ordered and shipped separately:

- Front panel kit, 77712595.
- Power supply - includes five-foot power cable.
- 9410-3 to 9415-3 Interface Adapter Kit, TBD, for Model 9415-3.
- Lark Device Interface Adapter, 77732426, for Model 9415-3.
- Top Mount PWA Adapter, 77715495.

1.2.4 MAJOR COMPONENTS

The major components of the WREN are shown in Figure 1-1.

CAUTION

NEVER remove the top cover of the WREN. This exploded view is for information only. Servicing items in the upper sealed environmental enclosure (heads, media, actuator, etc.) requires special facilities. Only the printed circuit boards and solenoid brake external to the sealed area can be replaced without special facilities.

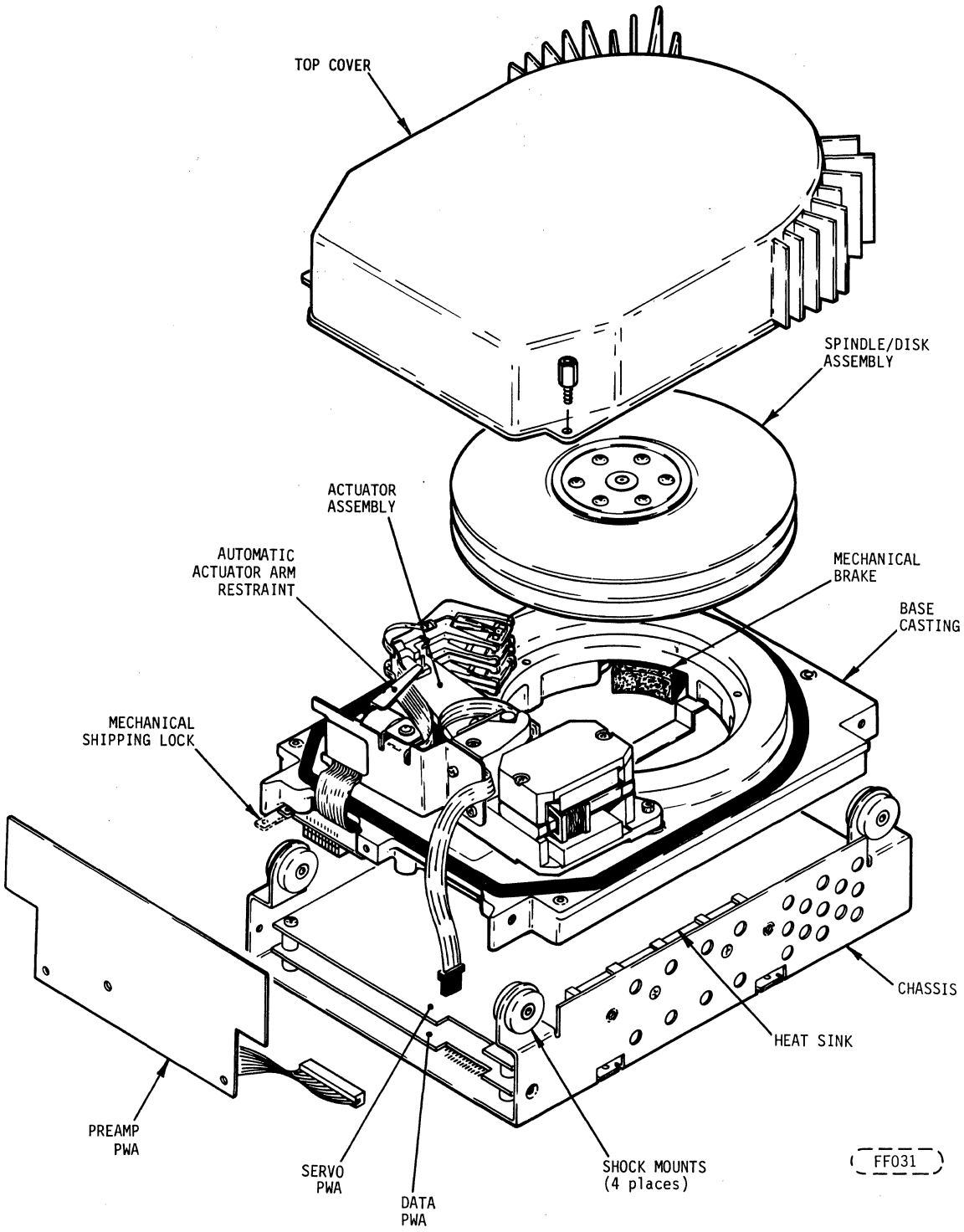


FIGURE 1-1. MODEL 9415 WREN I

2.1 INTRODUCTION

There is only one mechanical function required of the operator: to ensure that power is applied. During routine computer operations, the operator should, of course, note any malfunctions or problems and report them.

2.2 OPERATING AND PRELIMINARY DIAGNOSIS PROCEDURE

Due to the sophisticated design and special equipment required to repair the WREN, most repairs may only be effected at a properly equipped and staffed depot service and repair facility. These repair facilities will be capable of performing all warranty and routine repair activities.

Because the front panel indicator provides limited failure conditions (see paragraph 2.2.2) and no operator/drive interaction is required, operating systems must contain sufficient error reporting information to allow the operator to make preliminary diagnosis of problems. In other words, software must adequately inform the operator if any technical difficulties arise. In multi-unit installations, logical and physical identification are necessary for the operator to identify a defective unit.

2.2.1 OPERATING INSTRUCTIONS

1. The following conditions must be met to initiate operation of the disk drive.
   a. The DC power cable from the power supply must be connected.
   b. Mechanical shipping lock must be in operating position.
2. The operating temperature of the drive is 50^{o} to 115^{o} F (10^{o} to 46^{o} C) with a maximum temperature change of 18^{o} F (10^{o} C) per hour.
3. In case of a malfunction, the unit is to be serviced only by trained personnel.

2.2.2 FRONT PANEL INDICATOR (AVAILABLE ONLY WITH FRONT PANEL KIT.)

The front panel indicator under normal operation will serve as a Drive Selected indicator. It will also flash to indicate a drive failure when one of the following conditions exist.

1. Rotor is locked.
2. Spindle speed exceeds $\pm$5% tolerance for more than 30 seconds.
3. The WREN cannot load heads after 6 attempts (i.e. mechanical shipping lock left on, PLO does not lock, automatic arm restraint fails to release, etc.).

3.1 INTRODUCTION

This section provides the information and procedures necessary to install and checkout the CDC Model 9415 WREN I Disk Drive. The WREN is designed, manufactured, and tested with a "Plug-in and Play" installation philosophy. Basically, this philosophy minimizes the requirements for a highly trained person to integrate a WREN into their system.

3.2 UNPACKING

Visually inspect the shipping container for any obvious damage. During unpacking, exercise care so that any tools being used do not cause damage to the unit. As the drive is unpacked, inspect it for possible shipping damage. All claims of this type should be filed promptly with the transporter involved. If a claim is filed for damages, save the original packing materials.

CAUTION

Figure 3-1 shows the mechanical shipping lock which is accessible from both the front and the rear of the WREN. To prevent damage to the read/write heads or the disk itself, move the mechanical shipping lock to the operating position only after installation has been completed.

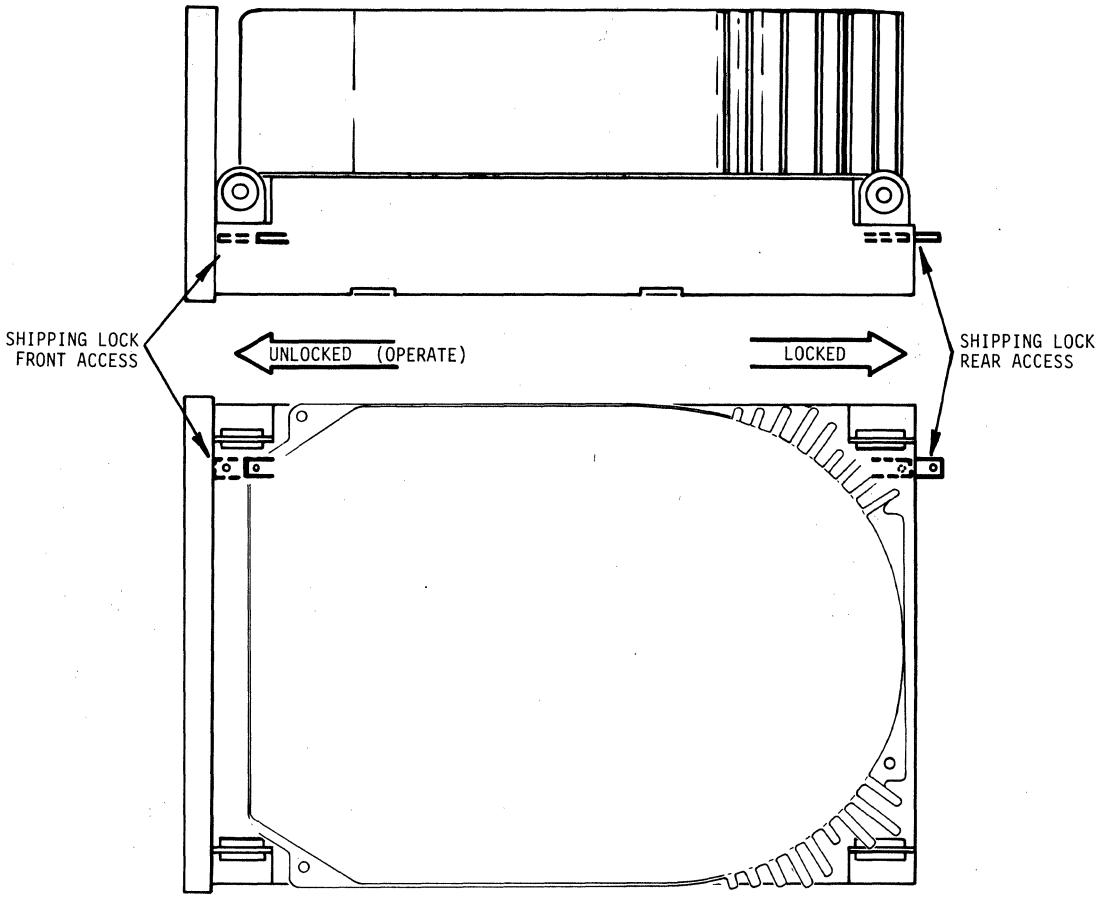
After the drive is unpacked, inspect the drive for any visual damage. Compare all parts listed on the shipping bill with the received equipment. Discrepancies or damage should be reported to the Sales Representative. Save the packing materials; they can be used for reshipment.

3.3 OPERATING ENVIRONMENT

The environmental conditions required for optimum performance of the disk drive are, in general, the same as those in an office environment with minimum or no environmental control. These conditions are:

Temperature	50^{o} to 115^{o} F (10^{o} to 46^{o} C)
Humidity	20% to 80%
Altitude	-983 to +6,562 feet (-300 to +2,000 meters)

The room temperature should not change more than 18° F (10° C) per hour. Relative humidity should be kept between 20% and 80%. Avoid high relative humidity as much as possible since it can cause condensation in the drive. Very low relative humidity should also be avoided because it can lead to particle attraction and accumulation by static electricity.



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REAR ACCESS

THE SHIPPING LOCK WILL PROTRUDE OUT THE REAR IN THE LOCKED POSITION. A HOLE IN THE ARM OF THE LOCK IS PROVIDED FOR ACTIVATING THE LOCK.

FRONT ACCESS

A HOLE IN THE FRONT PANEL ALLOWS FRONT ACCESSIBILITY TO THE SHIPPING LOCK.

FIGURE 3-1. MECHANICAL SHIPPING LOCK POSITION

3.4 SPACE ALLOCATION AND MOUNTING REQUIREMENTS

Figure 3-2 shows overall dimensions of the drive for determining space allocation and mounting requirements.

The WREN is designed for multiple unit installation in a standard 19-inch rack. Since the WREN is a fixed drive, slides are not provided, but tapped holes are placed at various locations, on the chassis for mounting in the enclosure.

The WREN uses air from the rotating disks for cooling the PWA's and mechanical components. The WREN design also uses the outer case to dissipate heat. Direct contact to the internal WREN heat sink can be made through the two mounting holes on the right side of the WREN (see Figure 3-3). Good metal to metal thermal contact of this surface with the customer cabinet mounting hardware is highly recommended for optimized heat transfer. Consideration should also be given to minimizing restriction of airflow through cooling holes in the drive.

A sometimes overlooked consideration when mounting several drives in the same enclosure is heat dissipation. Because power supplies, for example, are typically heavy and produce large amounts of heat, they are usually mounted in the bottom of an enclosure. This heat rises to the top of the cabinet or enclosure and the temperature can increase drastically. Cabinet ventilation, either by natural convection or forced cooling, must be provided to keep the internal air temperature around the disk drive within the limits specified in paragraph 3.3.

3.5 MOUNTING ORIENTATIONS

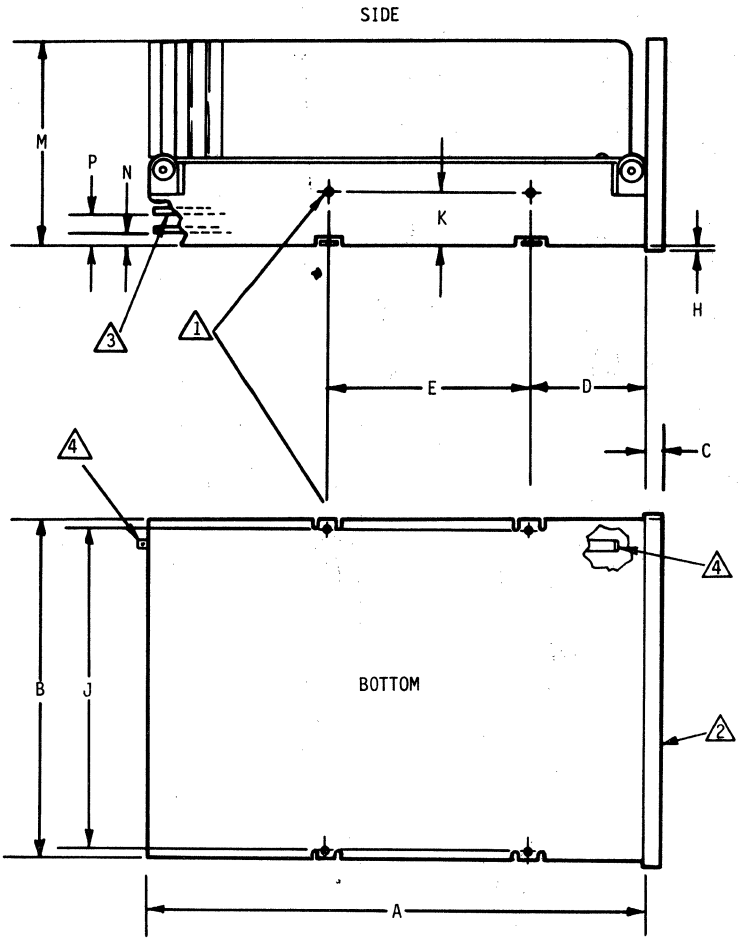
CAUTION

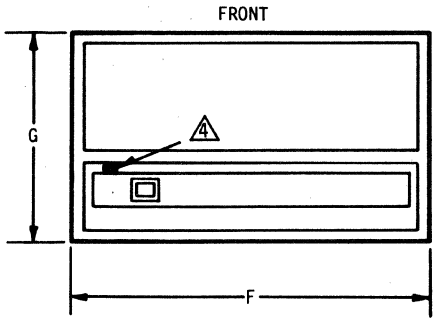
The drive should never be shipped without the mechanical shipping lock in the locked position to prevent damage to the disk and/or heads.

There are only two mounting orientations: disk in a horizontal plane and disks in a vertical plane. In either the horizontal or vertical mounting, the uppermost casting surface should be in a level position or drive performance may be affected.

3.5.1 VERTICAL ORIENTATION MOUNTING

In the vertical orientation, the drive must be mounted so that the mechanical shipping lock is in the up position as shown in Figure 3-1. This is to ensure that the read/write heads will return to the dedicated landing zone when power is removed.





NOTES:

1. MOUNTING HOLES, FOUR ON BOTTOM, TWO ON EACH SIDE. 6-32 UNC. MAX SCREW LENGTH INTO CHASSIS 0.31 IN. (7.87 mm)
2. FRONT PANEL ACCESSORY
3. DRIVE INTERFACE CONNECTIONS
4. MECHANICAL SHIPPING LOCK
5. WEIGHT IS APPROX. 7.50 LBS (3.4 Kg)

	IN	CM
A	8.0 MAX	20.32
B	5.75 $\pm^{0.00}_{0.02}$	14.6
C	0.29 ± 0.02	.74
D	1.87 ± 0.02	4.75
E	3.12 ± 0.01	7.92
F	5.88 ± 0.01	14.9
G	3.38 ± 0.02	8.58
H	0.065 ± 0.02	.165
J	5.50 ± 0.02	13.97
K	0.86 ± 0.02	2.18
M	3.25 ± 0.02	8.25
N	0.37 REF	.94 REF
P	0.63 REF	1.60 REF

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FIGURE 3-2. MOUNTING DIMENSIONS

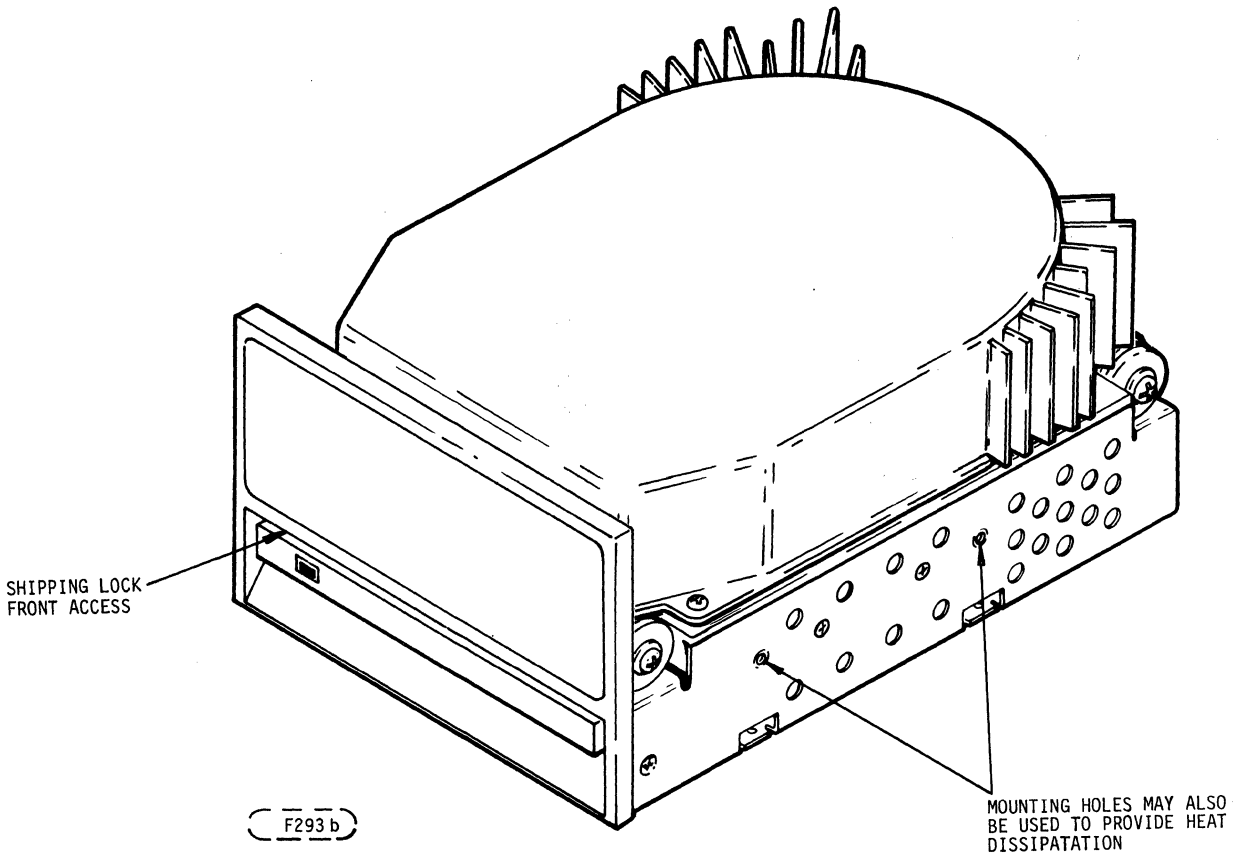

FIGURE 3-3. HEAT SINK MOUNTING HOLE LOCATION

Two tapped holes are provided on each side of the drive for securing the drive to the enclosure (cabinet). The drive may be bolted to an overhead member in a suspended mount and/or bolted from below in a supportive mount. Screws with 6-32 threads and sufficient length to allow several threads of engagement in the casting after passing through the cabinet mounting member should be used. Maximum screw penetration into WREN chassis should not exceed 0.31 inch.

3.5.2 HORIZONTAL ORIENTATION MOUNTING

As shown in Figure 3-2, four 6-32 tapped holes are provided in the base of the chassis to facilitate mounting in the horizontal position.

The WREN may be mounted directly to the rack using size 6-32 screws. Place the drive in the rack or cabinet and secure it with screws with sufficient length to ensure adequate thread engagement and such that screw penetration into the WREN chassis does not exceed 0.31 inch.

3.6 DRIVE CABLING

The required connections to the drive are power and signal cables. All input/output cables exit at the rear of the disk drive. The signal cables consist of a command interface cable and a data interface cable. Figure 3-4 shows the orientation of the command, DC power and data connectors.

Figure 3-5 shows the intercabling and terminator placement for the various drive connection arrangements. Shown are radial and daisychained system configurations. A single drive would be connected as shown for the radial configuration.

Terminator resistor packs are included in each drive. The terminator consist of a DIP resistor module which is plugged into a DIP socket in each drive. (See Figure 3-4 and 3-6 for location.) An equivalent terminator must be provided in the controller on each input signal line from the WREN to the controller.

RADIAL CONFIGURATION

View A of Figure 3-5 shows each drive interfaced to its own Command cable, which, in turn, allows interfacing of more than four drives and a variety of system operational techniques. Each drive has its Data cable and Command cable radially connected to the host controller. The length of each individual cable must not exceed 20 feet (6.1 meters). Terminator resistors must be installed in the host controller for each Data cable and for each Command cable.

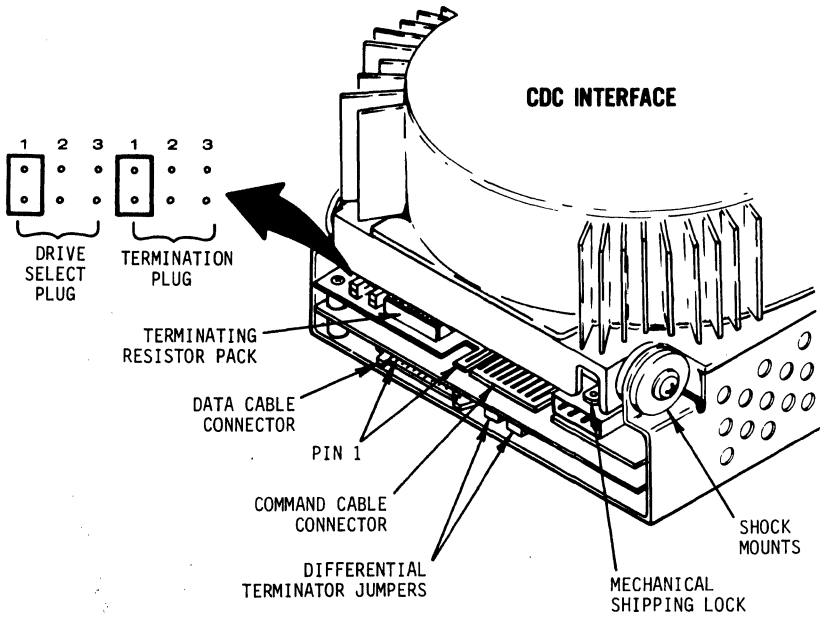

FIGURE 3-4A. COMMAND, DATA, AND POWER CABLE REQUIREMENTS FOR MODEL 9415-3

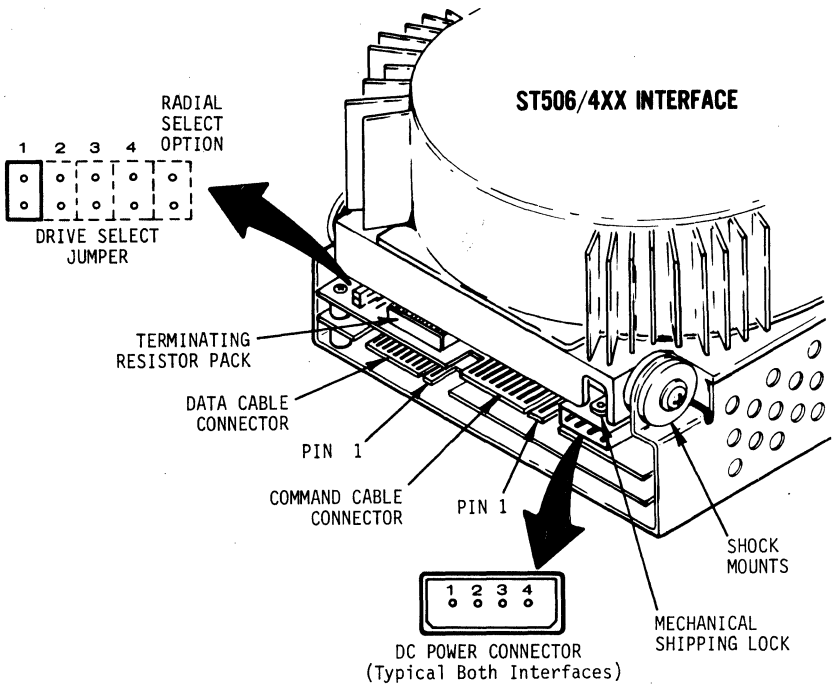

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FIGURE 3-4B. COMMAND, DATA, AND POWER CABLE REQUIREMENTS FOR MODEL 9415-5

Each Command cable is terminated in the drive by installing the terminating resistor pack. Each Data cable is terminated in the drive by resistors mounted on the Servo PWA.

DAISYCHAINED CONFIGURATION

In a daisychain configuration, the Data cables are connected in a radial configuration and the drives are connected in daisychain on the Command cable. The total length of all Command cables used shall be less than or equal to 20 feet (6.1 m). The logical address of each drive in the daisychain is determined by the "DRIVE SELECT" plug on the Servo PWA (Figure 3-6A and 3-6B). Each Data and Command cable must be terminated in the Host Controller.

Units with the CDC Interface (Model 9415-3) can have up to three drives daisychained (Figure 3-5A and 3-5B). Of the three drives, one or two can be Flexible Disk Drives, however the last drive in the daisychain must be a WREN to insure that WREN unique lines are terminated. This last drive in the daisychain requires a Terminating Resistor pack. These resistor packs must be removed from the other drives (if WRENS) in the daisychain.

Units with the ST506/4XX Interface can also be connected in a daisychain configuration of the Command cable. (Figure 3-5A and 3-5B.) Up to four WRENS can be daisychained, however, Flexible Disk Drives cannot be a part of the daisychain. Again, the last WREN in the daisychain will have the Command cable terminated by use of the termination resistor pack. The pack will be removed from all other WRENS in the daisychain.

SIGNAL/CHASSIS GROUNDS

The WREN I Disk Drives are manufactured with the signal and chassis grounds common. Zero ohm resistors (designated W1 and W2) on the Data board allows modificaton of this relationship at the customer's option. The results of connecting/disconnecting the zero ohm resistors are listed in Table 3-1. The customer can select any of these grounding options by removing W1 and/or W2.

TABLE 3-1

W1	W2	RESULT
X	X	Grounds common, quick connect terminal tied to common ground (as manufacatured)
X	O	Grounds separate, quick connect terminal tied to chassis ground
O	X	Grounds separate, quick connect terminal tied to signal ground
O	O	Grounds separate, quick connect terminal floating

X = Connected
O = Not Connected

See Figure 3-4C for physical locations of W1 and W2 and Figure 3-4D for schematic.

Zero ohm resistors are on the data boards of drives which are series code four and above. The series code of the drive is indicated by the first two digits of the serial number, ie, 04000001.

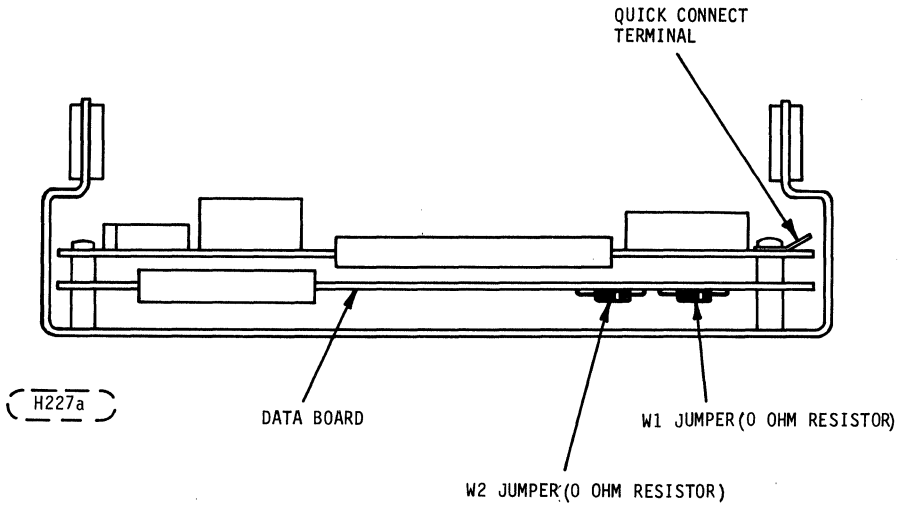

FIGURE 3-4C. PHYSICAL LOCATION OF W1 AND W2.

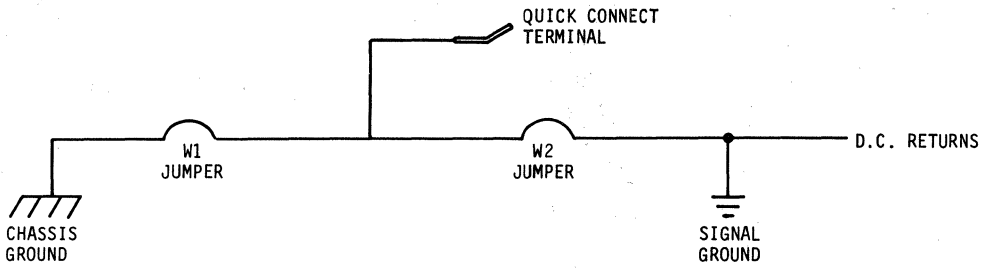

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FIGURE 3-4D. SCHEMATIC DIAGRAM OF W1 AND W2.

3.7 DRIVE SELECTION

The logical address of the WREN Disk Drives is selected by installing a jumper into the appropriate location on the DRIVE SELECT header which is available from the back of the drive and located on the SERVO PWA. (See Figure 3-6A and 3-6B.) This selection is done at the time of installation.

The drives with the CDC Interface (Model 9415-3) have three locations in the header for drive selection and three for termination of the drive select lines. The drive select jumper and the termination jumper are to occupy the same location, i.e. 1 and 1, 2 and 2, or 3 and 3. For radial configurations, it is recommended that these jumpers be in location 1.

For daisychain configurations, the jumpers should be in position 1, 2, or 3 depending on the location of the drive in the daisychain. If the daisychain contains Flexible Disk Drives, the drive select termination will not be used as the FDDS do not have this feature.

The drives with the ST506 Interface (Model 9415-5) have five locations in the header for drive selection. If the drive is to be operated in a radial configuration, the jumper should be in location five. For a daisychain configuration, the jumper should be in position 1, 2, 3, or 4, depending on the location of the drive in the daisychain.

3.8 AUTO VELOCITY ADJUST

After power has been applied and spindle speed is in tolerance, the WREN actuator will perform several seeks (approximately 15) to fine tune the actuator for optimum performance. After all seeks are complete, the heads will be loaded over cylinder 00.

3.9 SELF SEEK TEST

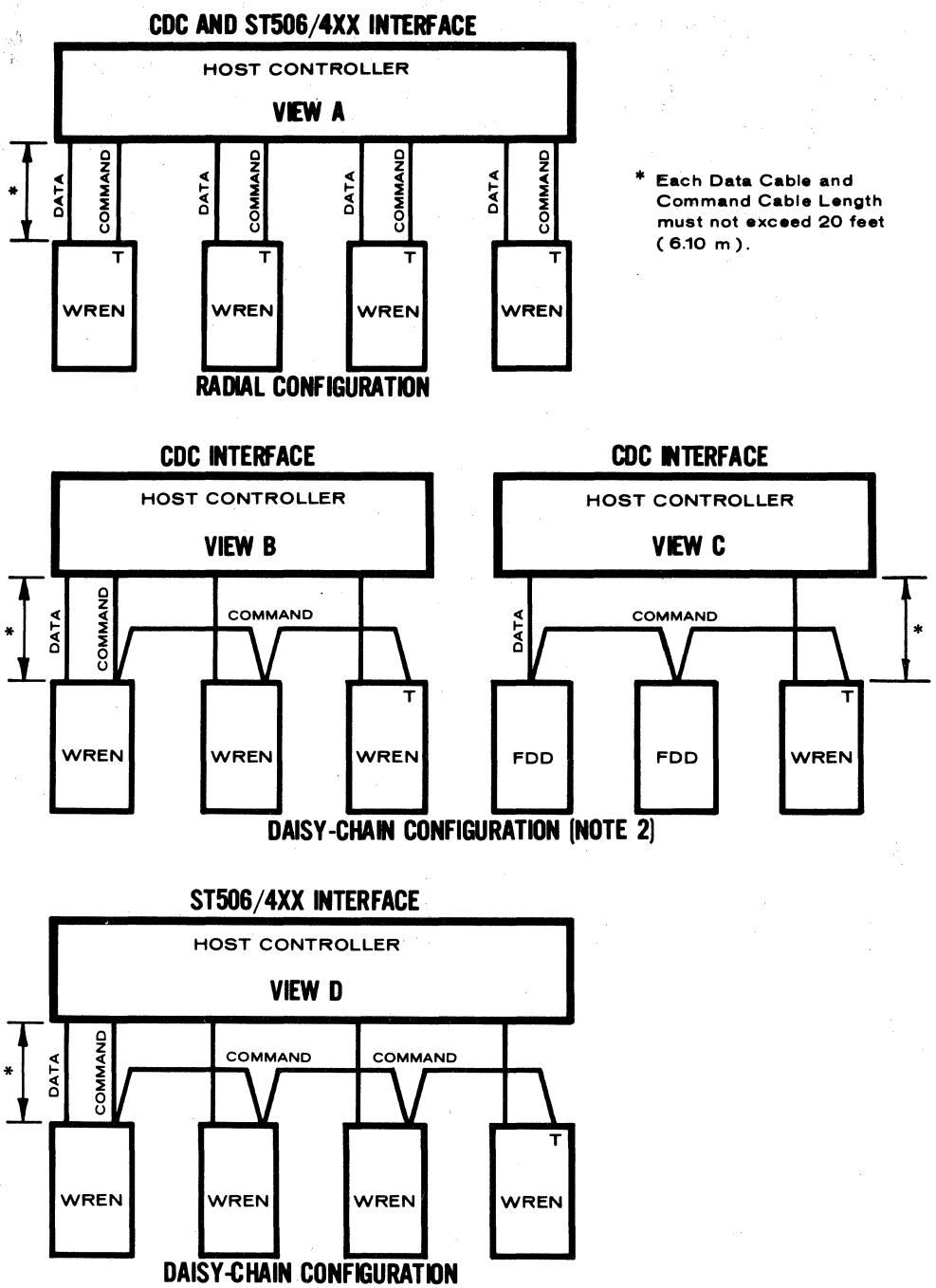
The WREN I has the capability to perform full stroke seeks by installing a jumper as shown in Figure 3-7. Use a UNIT SELECT jumper for this test. Removal of the front panel is required. The jumper must be installed prior to power-up. The full stroke seeks are performed immediately after the auto velocity adjust is performed. Full strokes will continue until the WREN is powered down or jumper is removed.

3.10 DIFFERENTIAL TERMINATION JUMPER

The differential receivers used in the WREN with the CDC Interface are compatible with both 26LS31 differential drivers or 75110 differential drivers. However, a different termination network is required for each configuration. Two jumpers are provided on the WREN as shown in Figure 3-6A. When both jumpers are installed, the WREN is configured for 75110 operation. When both jumpers are removed the WREN is configured for 26LS31 operation.

3.11 INITIAL CHECKOUT AND STARTUP PROCEDURE

1. Mount the Drives either horizontally or vertically in the enclosure using standard hardware.
2. Connect the cables for either radial or daisychained configuration. Terminate as required.
3. Connect the Command cable, a 34-conductor ribbon cable, between the Controller and the Drive.
4. Connect the Data cable, a 20-conductor ribbon cable, between the Controller and the Drive.
5. Attach DC power cable from power supply to connector on the rear of the WREN.
6. Move the mechanical shipping lock to the operating position.
7. Apply power to the drive. Front Panel Indicator will flash if the shipping lock is not released.
8. Run system diagnostics to ensure the operability of the disk subsystem.



NOTE 1: 'T' Indicates Terminating Resistor Pack. WREN Data Cables are Permanently Terminated.

NOTE 2: A WREN Must be the Last Drive in the Daisy Chain. A Maximum of Three Drives may be Daisy Chained.

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FIGURE 3-5. INTERFACE CABLING OPTIONS

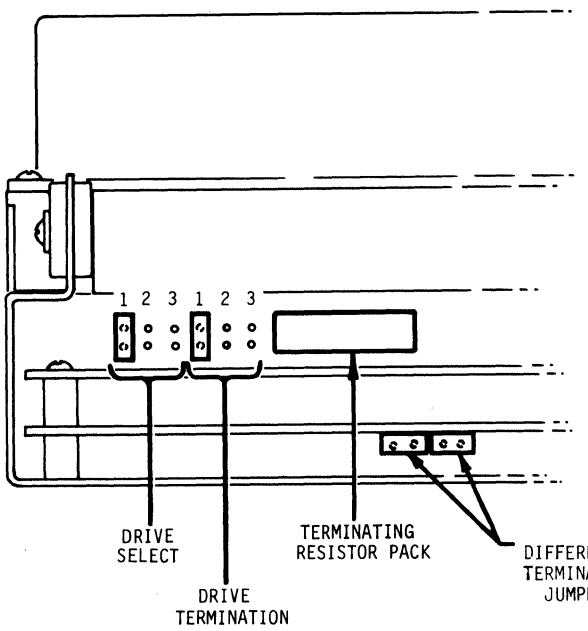

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FIGURE 3-6A. DRIVE SELECT AND TERMINATING JUMPER LOCATIONS MODEL 9415-3

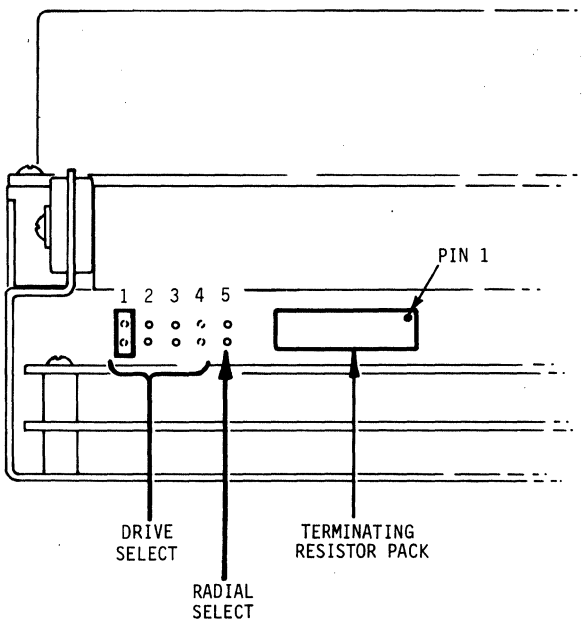

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FIGURE 3-6B. DRIVE SELECT AND TERMINATING JUMPER LOCATIONS MODEL 9415-5

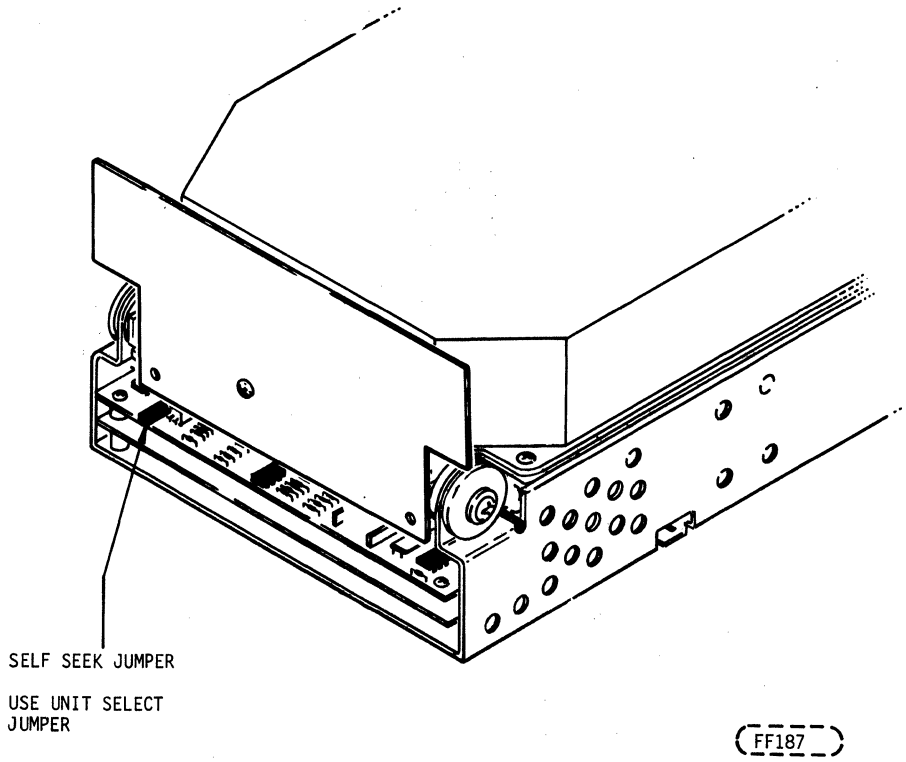


FIGURE 3-7. SELF SEEK JUMPER LOCATION

4.0 THEORY OF OPERATION, WREN I DISK DRIVES

4.1 INTRODUCTION

The Theory of Operation Section will cover both WREN I Disk Drives (i.e., the drive with the CDC Interface, Model 9415-3, and the drive with the Seagate Interface, Model 9415-5). The paragraphs of Section 4.0 will be identified as to whether it applies to the drives with the CDC Interface, the drives with the Seagate Interface or both.

The general block diagram of the WREN I is shown in Figure 4-1. Other block diagrams will be used to aid in the description of the drives.

Logic signal names may be followed by the symbol "+L" or "-L". Active high (+4 volts for TTL or -0.8 volts for ECL) have "+L" while active low (+0.8 volts for TTL or -1.7 volts for ECL) have "-L". ECL signals may also indicate active high with "-P" and active low with "-N" suffix.

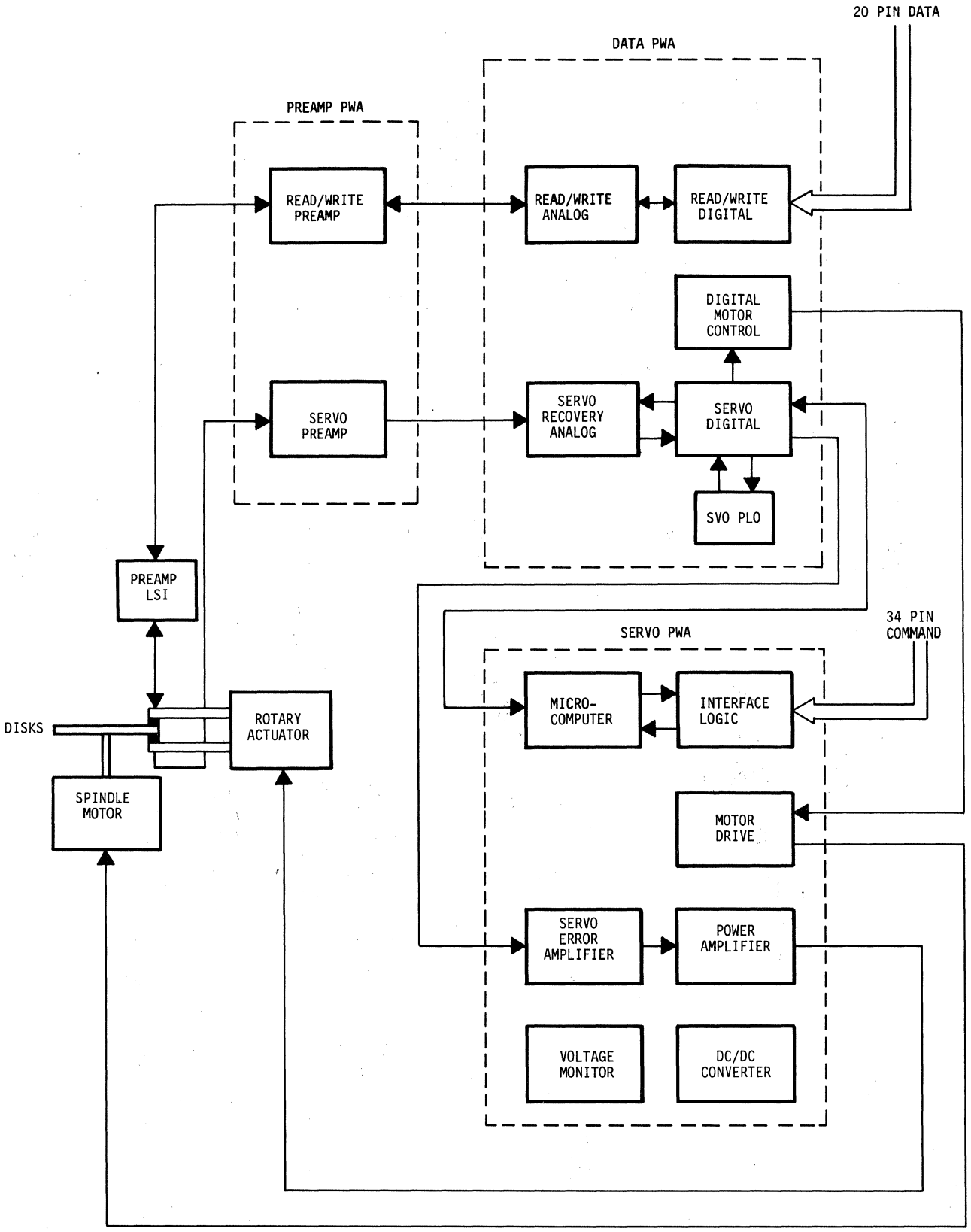
Integrated circuit pins will be identified by IC location and pin number. For example, "U25-12" is pin 12 of IC at location U25.

4.2 ASSEMBLIES (CDC AND SEAGATE INTERFACES)

Figure 4-2 illustrates the physical placement of the major assemblies of the WREN I Disk Drive. The following paragraphs describe the operation of these assemblies.

4.2.1 MECHANICAL ASSEMBLIES (CDC AND SEAGATE INTERFACES)

There are just two major subassemblies which make up a WREN I Disk Drive (Figure 4-2). The base assembly contains the media, filtration system and spindle motor. The base is built and tested as a unit and then mated with the actuator assembly. The actuator assembly contains the bobbin, coil, magnets, rotary arm and heads. After the actuator is mated to the base the information needed to position the heads is written on the bottom surface of the bottom disk. This operation is called servo track writing (STW). After STW the stop is installed and adjusted. The stop keeps the servo head over the servo data and will be adjusted only in connection with STW. The cover assembly is then installed with three screws. These operations are performed in special clean rooms to keep the media contamination free. For this reason the top cover of a WREN should not be removed. The assemblies and components described in the following paragraphs are in an environmentally sealed area and shall be serviced at factory level depot ONLY. See Maintenance Section 6 for the items of General Maintenance.



(FF378a) FIGURE 4-1. WREN I GENERAL BLOCK DIAGRAM (CDC AND SEAGATE INTERFACES)

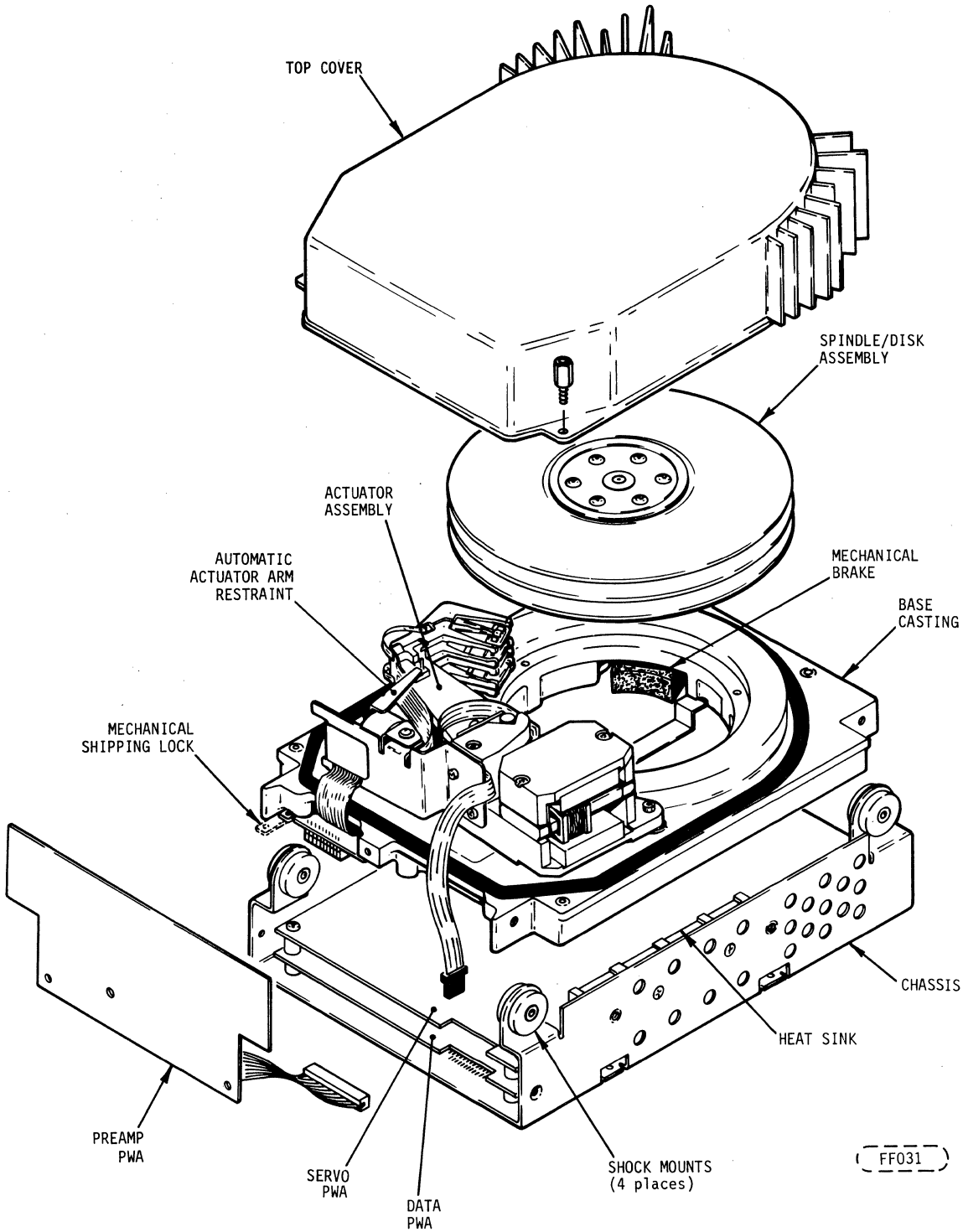


FIGURE 4-2. WREN I MAJOR ASSEMBLIES (CDC AND SEAGATE INTERFACES)

4.2.1.1 ACTUATOR ASSEMBLY (CDC AND SEAGATE INTERFACES)

The WREN I actuator is a rotary voice coil positioner. The voice coil can be thought of as a motor that moves through only a small angle. The motor stator consists of two permanent magnets, one upper and one lower, and a core bar (Figure 4-3). The motor rotor is a coil on a bobbin which fits around the stator core. By controlling the magnitude and direction of the rotor current, the rotor can be positioned any where in its range. The bobbin is attached to the rotary arm which provides the head mounting.

There are two bearings mounted in a bore thru the area. A shaft runs thru these bearings. This shaft is held in two V shape grooves on the housing which holds the magnets. The housing is later mounted to the base deck. Connection is made to the bobbin thru a three conductor flex cable.

The heads are mounted by screwing them into six slots at the end of the actuator arm. Each head has a short flex cable on it which must be soldered to a flex cable on the actuator arm.

The flex cable on the actuator arm has an SSI115 integrated circuit on it. The signals to and from the five data heads pass thru this circuit. The signal from the servo head passes directly to the connector which passes all signals to the Preamp PWA.

Removal and replacement of the actuator is a depot level maintenance procedure ONLY.

4.2.1.2 BASE ASSEMBLY (CDC AND SEAGATE INTERFACES)

The base assembly consists of the base casting, spindle assembly, head actuator assembly and two filtration systems as shown in Figure 4-4.

The base casting is the frame of the drive and all assemblies mount to it. The base casting also divides the drive into sealed and unsealed compartments. The area above the base casting and under the cover is sealed and provides a clean environment. The heads in the WREN fly at only 15 to 18 microinches, therefore the air in the sealed compartment must be kept very clean.

The spindle to which the disks are attached is an integral part of the spindle motor. The disks are the recording media for the drive. The recording surface of each disk is coated with a layer of magnetic iron oxide and related binders. The WREN Disks also have a lubricant over the oxide, this reduces the friction when the heads are landing. The drive can have up to three disks, each separated by a spacer. The whole assembly is held together by a clamp plate which bolts to the top of the spindle hub. The assembly then is bolted to the base casting with the spindle shaft protruding through the base.

The spindle motor is a two phase brushless DC motor. The motor rotor mounted on the opposite end from the spindle which serves as a braking surface and has fan blades which provides some air flow to cool the electronics. A grounding spring rests on the center of the rotor and bolts to the base casting, this provides a path for any static electricity generated by the head-disk interface to flow to the ground.

The arm restraint solenoid holds the arm and heads over the landing zone next to the spindle when power is not applied. The shipping lock reinforces the holding action to assure heads will not move during any shocks that may occur during shipping.

A brake on the bottom of the drive presses against the rotor of the spindle motor anytime power is not applied to the drive. This brake stops the spindle quickly to protect the surface of the disk in the landing zone.

The first of the filtration is a breather filter. It is bolted over a hole in the base casting and provides clean air to equalize the pressure between the sealed compartment and the outside world. The second system is a recirculating absolute filter. It removes any foreign material that may be present in the sealed compartment. Air is pulled out of the filter by the low pressure created near the spindle. Air then can circulate thru open areas in the spindle and flow out across all the disks. Some of the air will flow through this filter whenever the disk is spun. Over the life of the drive all the air in the sealed compartment will be cleaned many times.

Any servicing of the spindle assembly, spindle motor and filters is a depot level procedure ONLY.

4.3 FUNCTIONAL DESCRIPTION (CDC AND SEAGATE INTERFACES)

4.3.1 GENERAL (CDC AND SEAGATE INTERFACES)

This description is organized into the following major headings:

- Overall Drive Control System
- Head Positioning System
- Read/Write System
- Auxiliary Systems

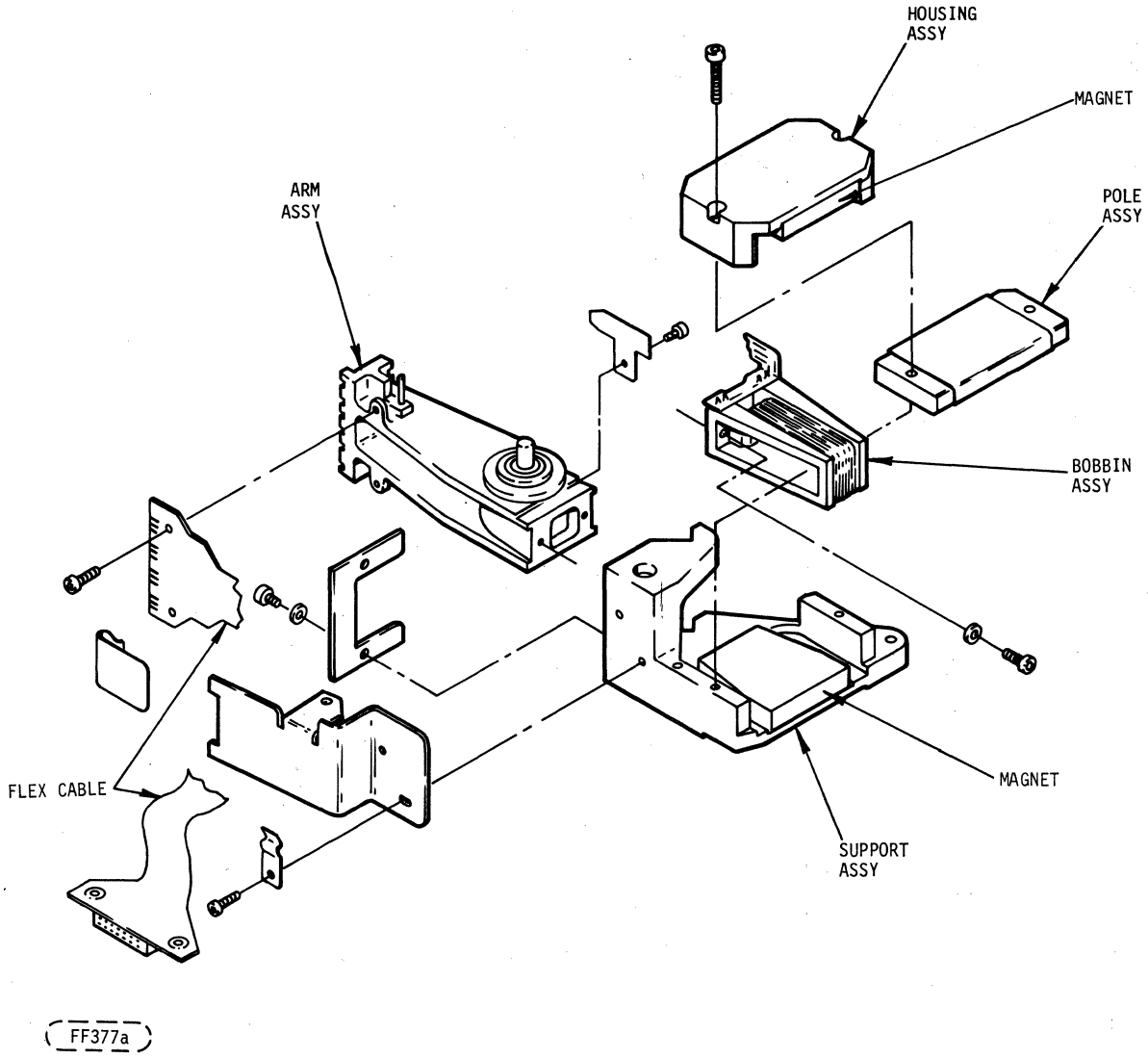


FIGURE 4-3. WREN I ACTUATOR ASSEMBLY
(CDC AND SEAGATE INTERFACES)

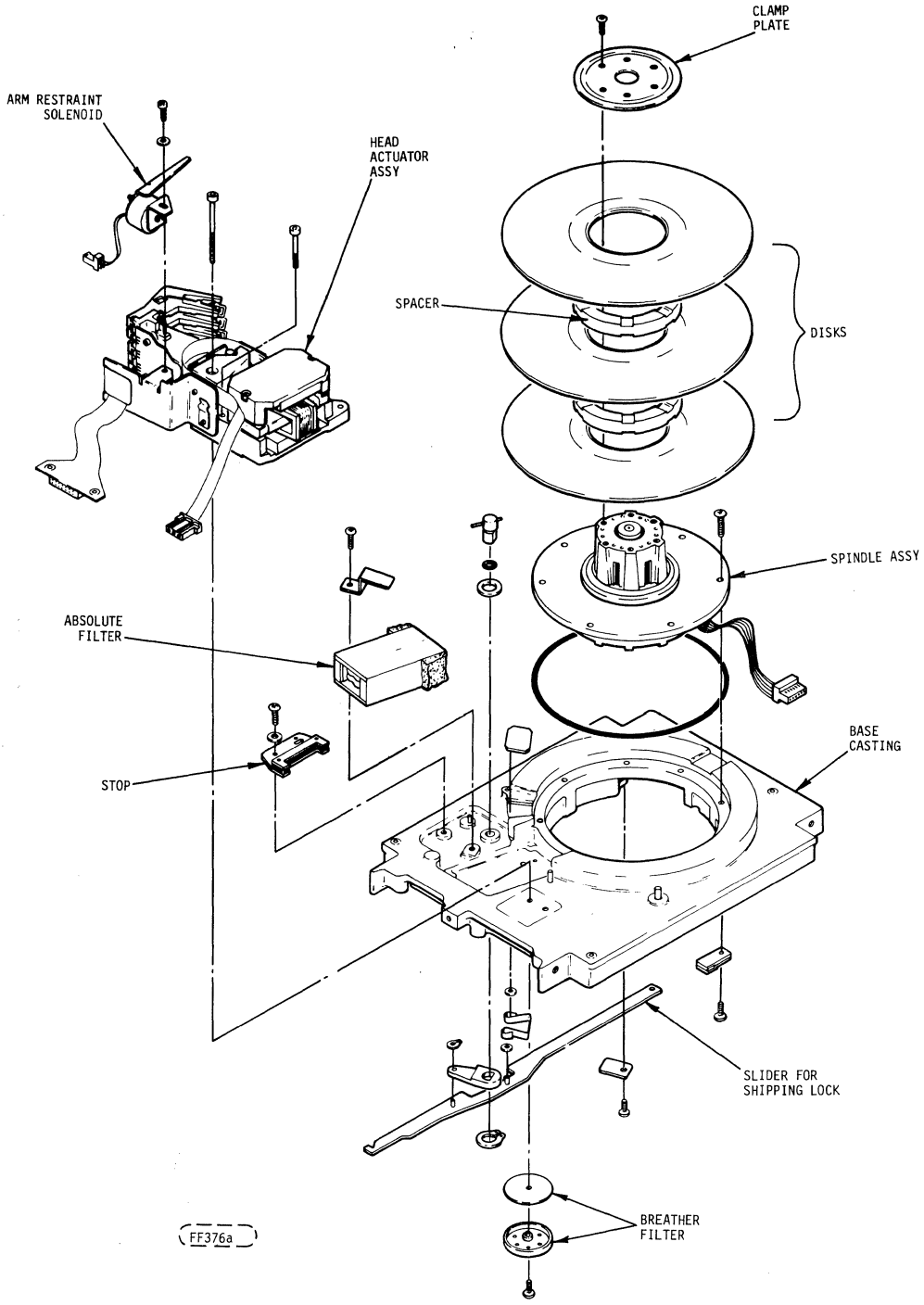


FIGURE 4-4. WREN I BASE ASSEMBLY (CDC AND SEAGATE INTERFACES)

4.3.2 OVERALL DRIVE CONTROL SYSTEM (CDC AND SEAGATE INTERFACES)

The WREN is under the control (excluding any control exerted by the controller via the interface lines) of the Microcomputer on the Servo PWA. The Microcomputer system is described in the following paragraphs. Any further details of the Microcomputer Theory must be taken from vendor publications for the various chips in the Microcomputer System.

4.3.2.1 MICROCOMPUTER OVERVIEW (CDC INTERFACE)

Figure 4-5 shows a simplified block diagram of the microcomputer. The microcomputer is an 8749 with two kilobytes of internal program memory. The microcomputer has no control of the read/write section with the exception of the write current magnitude.

When a step is received from the command cable interface, it is synchronized with the microcomputer clock and applied to the Test 1 input of the 8749. This causes a firmware counter to be incremented with each step pulse. The interface direction line is latched with the step pulse and applied to one of the Bus Port inputs. These two lines have all the information needed to cause a seek operation.

When a seek is in progress, track-crossing pulses are generated in the servo LSI logic; these are applied to the 8749's Interrupt input. This input remains active until the Interrupt is serviced and a track-pulse reset is sent to the servo LSI on a Port 2 line. In this manner, the microcomputer keeps track of all incoming step pulses and track crossings that occur. The address latch enable (ALE) signal is also sent to the spindle motor control as a reference signal for motor speed. During a seek, a seven-bit velocity command is output on Port 1 and goes to a D/A converter in the servo amplifier. The eighth bit on Port 1 is active for a high velocity command, and inactive for a low velocity command. A line from Port 2, titled "VCLO" (Velocity Command Low) is active for a low velocity command, and inactive for a high velocity command. During coarse mode either, but not both, line must be active. If both lines are inactive this indicates fine mode. These lines are used in conjunction with the forward/odd lines. Forward refers to a seek from a lower to a higher numbered cylinder. In the coarse mode, this line is active during a forward seek and inactive during a reverse seek. When the drive switches to the fine mode this line is active when the target track is even and inactive when the target track is odd.

Two lines from Port 2 generate Power-On Reset. If the track pulse reset and Disable Servo lines are both active, Power-On Reset is active. If either line is inactive, Power-On Reset is inactive. During start-up, Power-On Reset is active for approximately 6 seconds. This enables the current regulator in the spindle motor control. When it is inactive, it enables the speed regulator. It is also used to provide appropriate resets to sequential logic contained in the drive electronics. During start-up, motor speed is monitored on the Bus Port from the Motor Speed line. The phase lock oscillator (PLO) lock line is continuously monitored. Also during start-up, the servo is disabled via the Servo Disable line.

When the servo PLO is locked and the spindle motor is up to speed, head loading can commence. This is accomplished by the microcomputer issuing a velocity command, detecting guard band, performing an RTZ, and switching back to fine mode on cylinder zero. The data zone latch is set by Index. Index code is written only in the data and guard band zones. This enables the microcomputer to distinguish between these zones and the start zone.

There is a guard band latch external to the microcomputer that will disable the servo if guard band is encountered after the initial head load. During the head load and return to zero (RTZ) operations, this latch is disabled because guard band is then used to locate cylinder zero. This disable is activated by the guard band latch clear line from Port 2.

There is one other input to the Bus Port, called Test Seek. This input can be grounded with a jumper shunt and causes the drive to go into a continuous test seek following head load and the calibrate operation.

With the completion of head load, the microcomputer puts the drive through an automatic calibration procedure. During the calibrate sequence, a test seek is performed and timed by the microcomputer. When the microcomputer detects that the test seek is too slow, a short pulse is output on the Servo Disable line. This pulse is too short to actually permit the servo to disable but cause the automatic gain control (AGC) amplifier gain to decrease one step. This sequence is then repeated until the test seek is performed in the required time. The drive then returns to cylinder zero and sets the ready line. The ready line serves to indicate that the drive is on cylinder and ready to read or write. It will be false whenever the heads are outside the data zone, performing a seek operation, or off track center with the write gate enabled.

The servo will be disabled and the ready line made false at any time that loss of servo PLO lock is detected. A timing diagram for the step-pulse synchronizer is shown in Figure 4-7.

4.3.2.2 MICROCOMPUTER OVERVIEW (SEAGATE INTERFACE)

Figure 4-6 shows a simplified block diagram of the microcomputer. The microcomputer is an 8749 with two kilobytes of internal program memory. It also uses an 8243 port expander to increase the number of output signals. The microcomputer has no control of the read/write section with the exception of the write current magnitude.

When a step is received from the command cable interface, it is synchronized with the microcomputer clock and applied to the Test 1 input of the 8749. This causes a counter to be incremented with each step pulse. The interface direction line is latched with the step pulse and applied to one of the Bus Port inputs. These two lines have all the information needed to cause a seek operation.

When a seek is in progress, track-crossing pulses are generated in the servo LSI logic; these are applied to the 8749's Interrupt input. This input remains active until the Interrupt is serviced and a track-pulse reset is sent to the servo LSI on a Port 2 line. In this manner, the microcomputer keeps track of all incoming step pulses and track crossings that occur. The address latch enable (ALE) signal is sent to the spindle motor control as a clock for the speed regulator. During a seek, a seven-bit velocity command is output on Port 1 and goes to a D/A converter in the servo amplifier. The eighth bit on Port 1 is active for a high velocity command, and inactive for a low velocity command. A line from the port expander, titled "VCLO" (Velocity Command Low) is active for a low velocity command, and inactive for a high velocity command. The FINE signal puts the servo system into either the fine or coarse mode of operation. This signal is used in conjunction with the forward/odd lines. Forward refers to a seek from a lower to a higher numbered cylinder. In the coarse mode, this line is active during a forward seek and inactive during a reverse seek. When the drive switches to the fine mode this line is active when the target track is even and inactive when the target track is odd.

The Power On Reset signal originates from the port expander. During start-up, Power-On Reset is active for approximately 6 seconds. This enables the current regulator in the spindle motor control. When it is inactive, it enables the speed regulator. It is also used to provide appropriate resets to sequential logic contained in the drive electronics. During start-up, motor speed is monitored on the Bus Port from the Motor Speed line. The phase lock oscillator (PLO) lock line is continuously monitored. Also during start-up, the servo is disabled via the Servo Disable line.

When the servo PLO is locked and the spindle motor is up to speed, head loading can commence. This is accomplished by the microcomputer issuing a velocity command, detecting guard band, performing an RTZ, and switching back to fine mode on cylinder zero. The data zone latch is set by Index. Index code is written only in the data zone. This enables the microcomputer to distinguish between the data zone and the start zone.

There is a guard band latch external to the microcomputer that will disable the servo if guard band is encountered after the initial head load. During the head loading, this latch is disabled while setting on Track "0" or while performing a seek to Track "0". This is true because Track "0" is in the guard band. This disable is activated by the guard band latch clear line from the port expander.

There is one other input to the Bus Port, called Test Seek. This input can be grounded with a jumper shunt and causes the drive to go into a continuous test seek following head load and the calibrate operation.

With the completion of head load, the microcomputer puts the drive through an automatic calibration procedure. During the calibrate sequence, a test seek is performed and timed by the microcomputer. When the microcomputer detects that the test seek is too slow, a short pulse is output on the Velocity adjust line. This pulse causes the automatic gain control (AGC) amplifier gain to decrease one step. This sequence is then repeated until the test seek is performed in the required time. The drive then returns to cylinder zero and sets the ready line. The ready line serves to indicate that the drive is on cylinder and ready to read or write. It will be false whenever the heads are outside the data zone. The SEEK COMP line issues a pulse at the end of a seek to set the seek complete latch.

A servo will be disabled and the ready line made false at any time that loss of servo PLO lock is detected. A timing diagram for the step-pulse synchronizer is shown in Figure 4-9.

4.3.3.3 MICROCOMPUTER FIRMWARE ROUTINES (CDC INTERFACE)

The flow charts that follow illustrate the manner in which the microcomputer controls servo operation in the WREN. Figure 4-8 shows a chart of the primary modules that make up the WREN firmware. On power-up, the program enters and always returns to the Main Idle module. During start-up, the program exits the Main Idle module and goes to the System Initialize module. Following System Initialize, it then goes to the Head Load module. Upon completion of Head Load, the program branches back to the Main Idle Loop.

4.3.3.4 MICROCOMPUTER FIRMWARE ROUTINES (SEAGATE INTERFACE)

The flow charts that follow illustrate the manner in which the microcomputer controls servo operation in the WREN. Figure 4-10 shows a chart of the primary modules that make up the WREN firmware. On power-up, the program starts and always returns to the Main Idle module. During start-up, the program exits the Main Idle module and goes to the System Initialize module. Following System Initialize, it then goes to the Head Load module. Upon completion of Head Load, the program branches back to the Main Idle Loop.

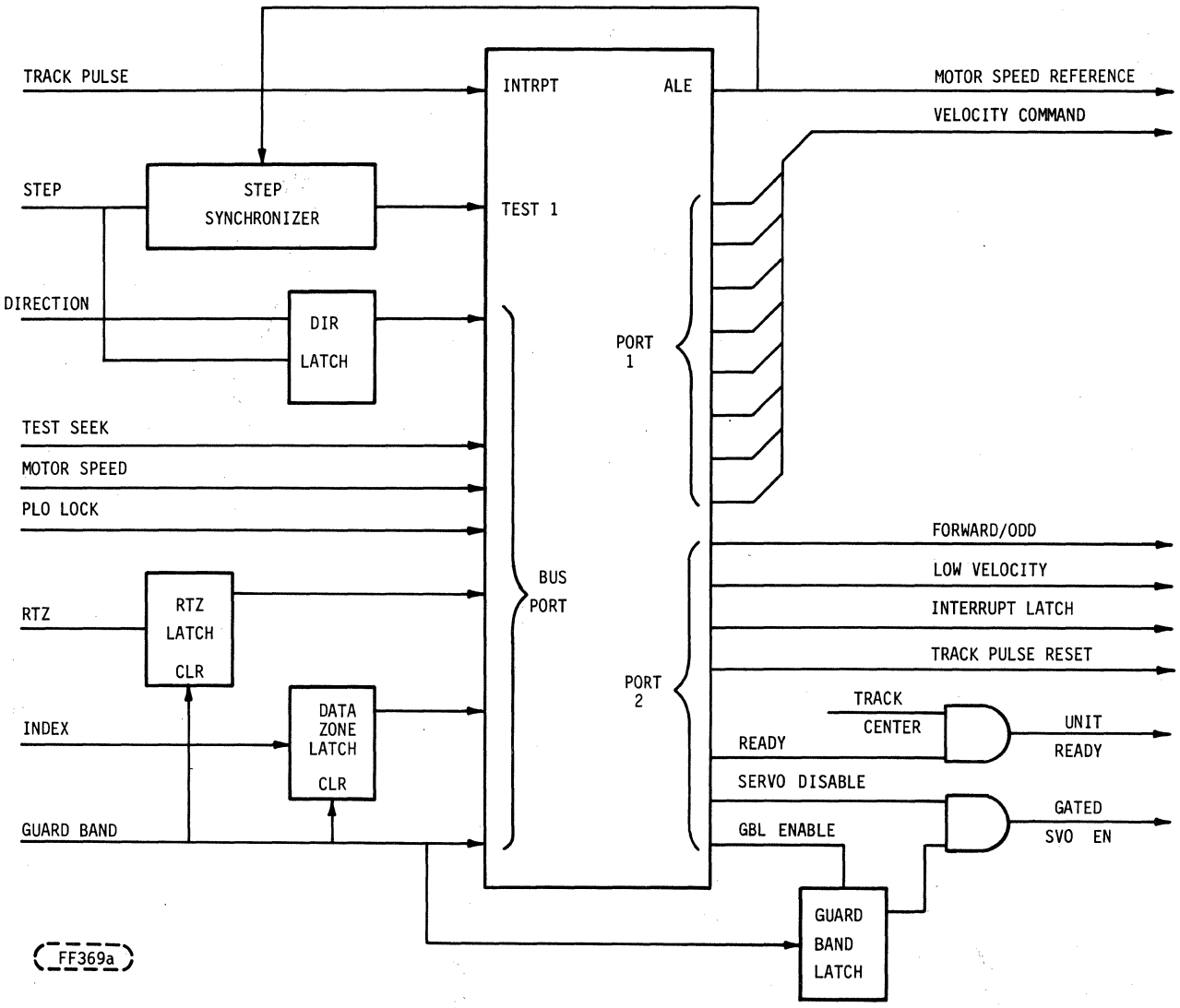


FIGURE 4.5. WREN I MICROCOMPUTER BLOCK DIAGRAM (CDC INTERFACE)

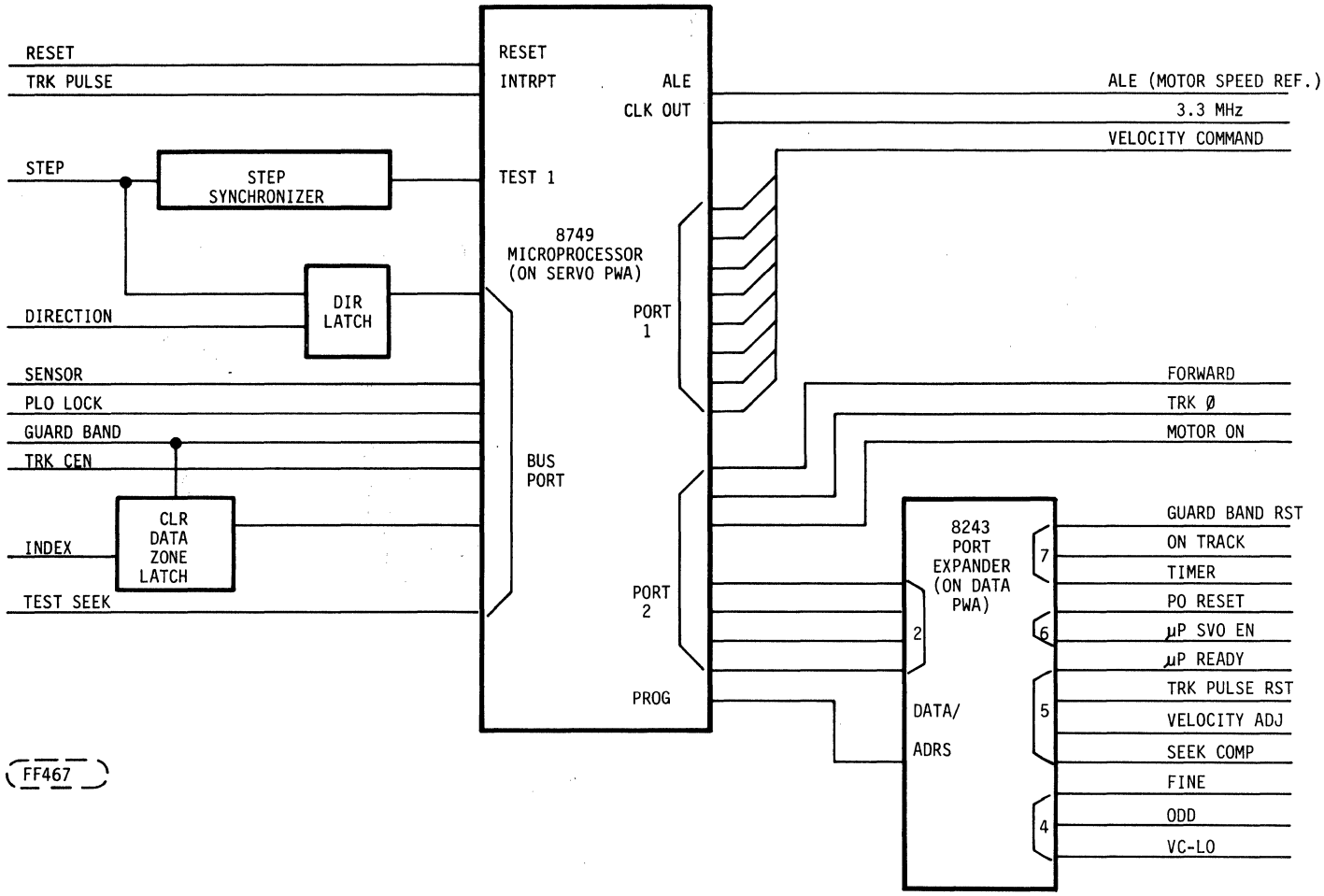


FIGURE 4-6. WREN I MICROCOMPUTER BLOCK DIAGRAM (SEAGATE INTERFACE)

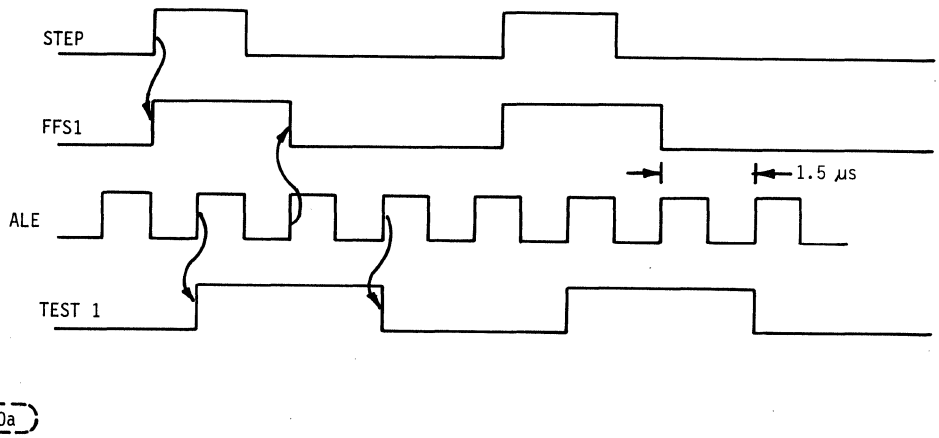
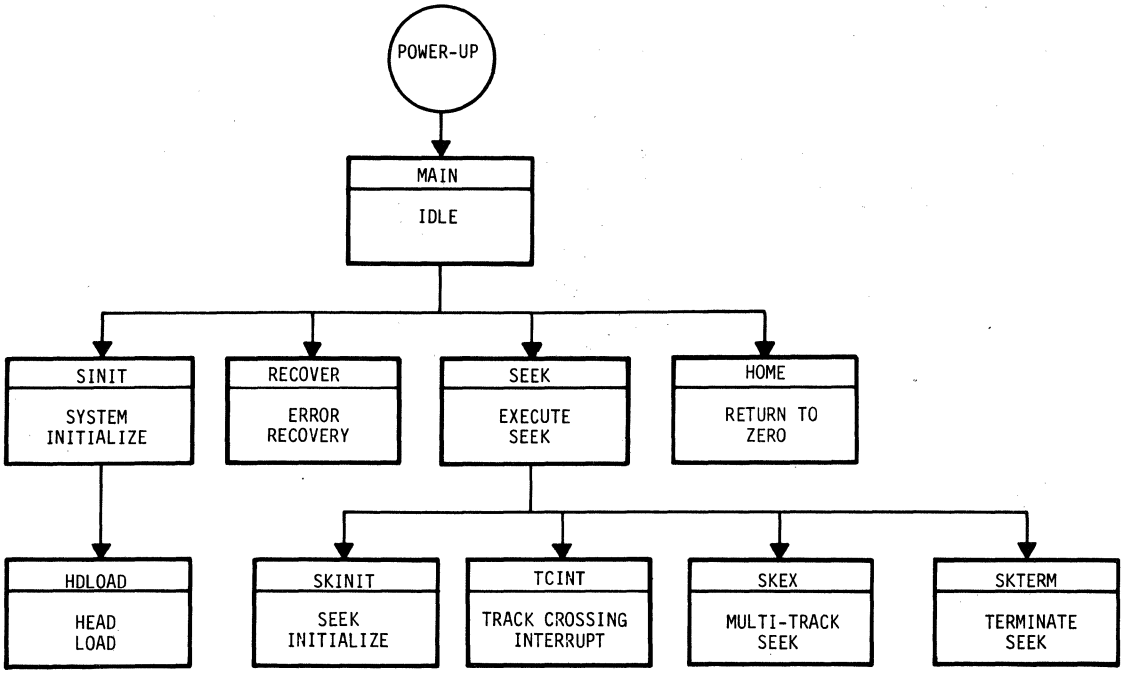
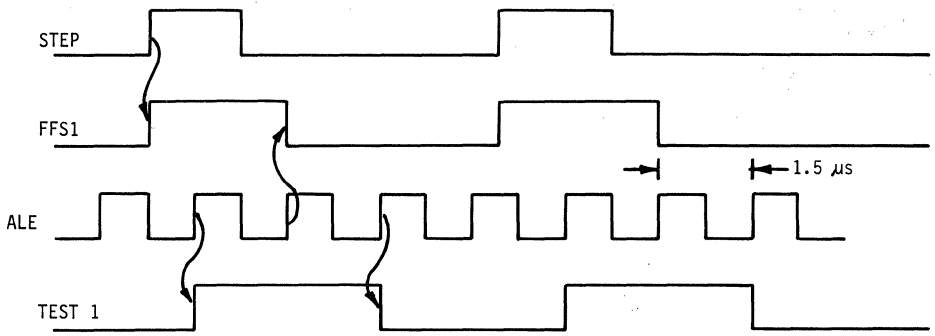


FIGURE 4-7. WREN I MICROCOMPUTER STEP PULSE SYNCHRONIZER (CDC INTERFACE)



H097

FIGURE 4-8. FIRMWARE MODULE CHART (CDC INTERFACE)



F210a

FIGURE 4-9. WREN I MICROCOMPUTER STEP PULSE SYNCHRONIZER (SEAGATE INTERFACE)

(A) MAIN IDLE LOOP MODULE (CDC INTERFACE)

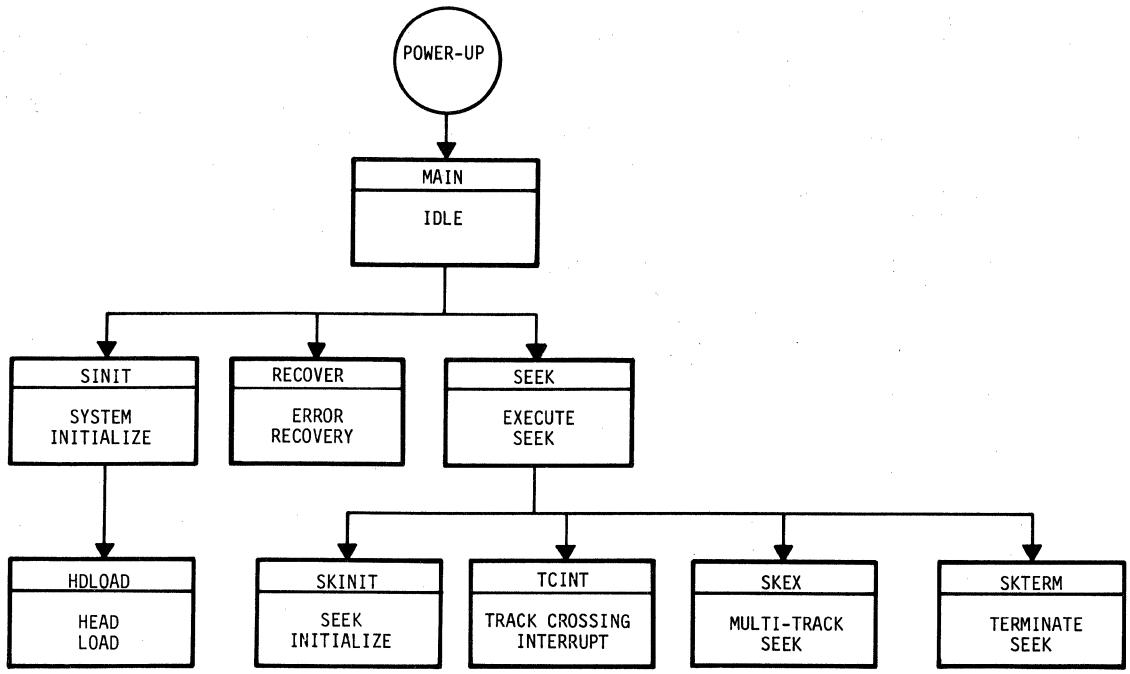
Assuming a normal power-up sequence has been completed, the program goes to the Main Idle Loop (Figure 4-11). Upon receipt of a Step pulse, the program will branch to the Seek module. From the Seek module, it proceeds to the Seek Initialize module. From the Seek Initialize module, it branches to a seek execution module. At the conclusion of a seek, it will go to the Terminate module. Upon completion of the Seek Terminate, it will return to the Main Idle Loop.

An RTZ command will cause a branching to the Home Module. When the operation is completed, it will return to the Main Idle Loop. In the Main Idle Loop the processor checks for three possible status fault conditions (1) incorrect motor speed, (2) loss of servo PLO lock and (3) servo systems disabled (an internal flag). If a Status Fault condition is present, the program will go into one of several recovery routines. Normally it is during this time that the servo is disabled and the heads would be reloaded. In the event of a servo disable, the microcomputer will automatically attempt to reload heads to cylinder zero. If there are six unsuccessful attempts, a trap state is entered. Operator intervention is the only way out of a trap state. Cycling power will restart the program and a new System Initialize sequence will be attempted.

(B) MAIN IDLE LOOP MODULE (SEAGATE INTERFACE)

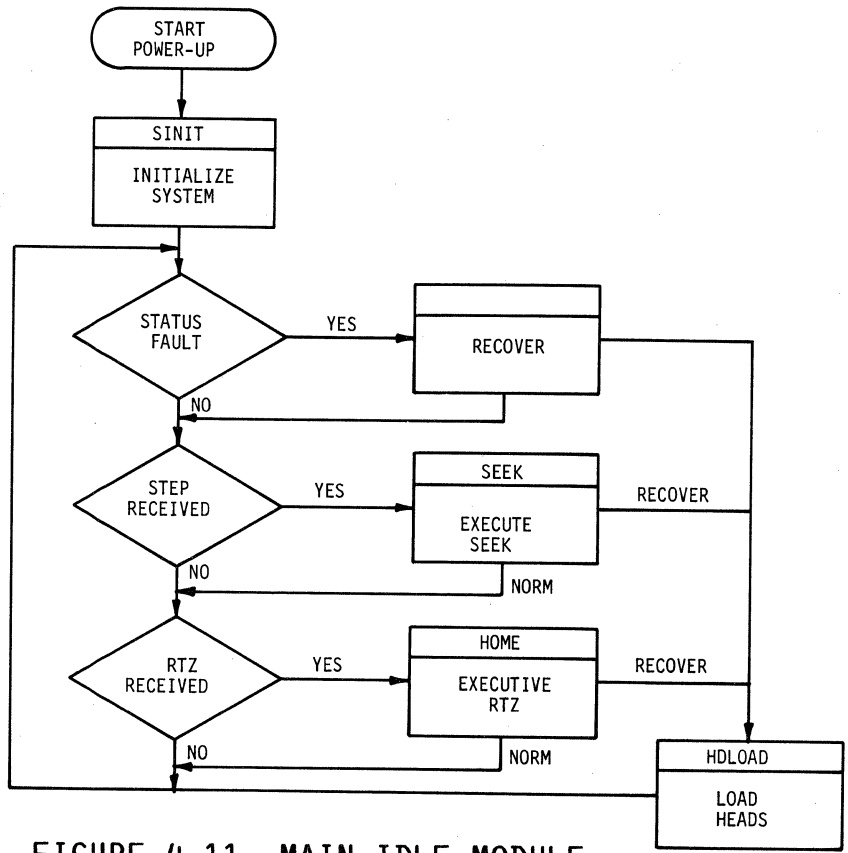
Assuming a normal power-up sequence has been completed, the program goes to the Main Idle Loop (Figure 4-12). Upon receipt of a Step pulse, the program will branch to the Seek module. From the Seek module, it proceeds to the Seek Initialize module. From the Seek Initialize module, it branches to a seek execution module. At the conclusion of a seek, it will go to the Terminate module. Upon completion of the Seek Terminate, it will return to the Main Idle Loop.

In the Main Idle Loop the processor checks for three possible status fault conditions (1) incorrect motor speed, (2) loss of servo PLO lock and (3) servo system disabled (an internal flag). If a Status Fault condition is present, the program will go into one of several recovery routines. Normally it is during this time that the servo is disabled and the heads would be reloaded. In the event of a servo disable, the microcomputer will automatically attempt to reload heads to cylinder zero. If there are six unsuccessful attempts, a trap state is entered. Operator intervention is the only way out of a trap state. Cycling power will restart the program and a new System Initialize sequence will be attempted.



FF394a

FIGURE 4-10. FIRMWARE MODULE CHART (SEAGATE INTERFACE)



F210c

FIGURE 4-11. MAIN IDLE MODULE (CDC INTERFACE)

(C) SYSTEM INITIALIZE MODULE (CDC AND SEAGATE INTERFACES)

The System Initialize module (Figure 4-13) starts with processor self-tests, then issues a System Reset for 4 seconds to bring the motor up to speed. A speed check is made, then the program branches to the Head Load routine. Following the Head Load, a velocity test is performed. This test will be attempted repeatedly, incrementing the velocity each time the test fails, until the test passes. There is then a check to see if the seek test pin has been grounded, and if so, the seek test continues. If not, errors are checked and the module returns to the Main Idle Loop.

(D) HEAD LOAD MODULE (CDC AND SEAGATE INTERFACES)

In the Head Load routine (Figure 4-14) the presence of a guard band dibit signal pattern is checked. In the start zone, there should be no guard band. Next the data zone is checked. If the head load is occurring during a power-up, the data zone flip-flop may be in an ambiguous state. In this case the data zone check is skipped.

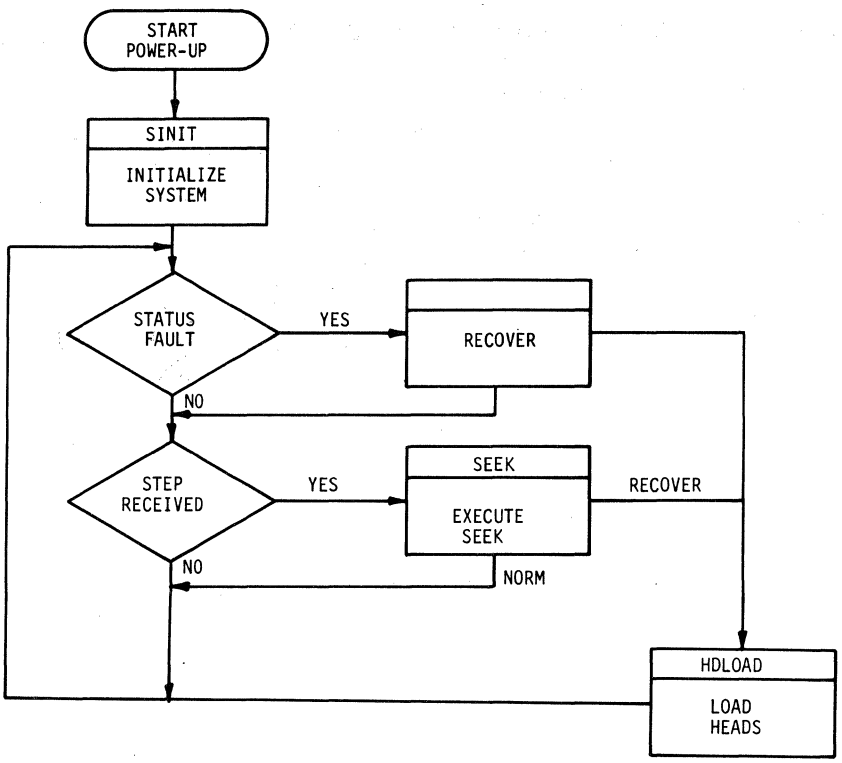
The next step is to move the arm out of the start zone across the disk and to position it on Track 0.

The head load velocity command is issued, the reverse and coarse load are enabled, the guard band detector is disabled and the positioner movement begins. After guard band is detected, the sequence continues looking for the exit of guard band. After exiting guard band, the first track-crossing pulse detected sets the Odd and Fine mode. The guard band latch is now enabled.

If during the start of a head load the guard band is detected in the start zone, the servo will be enabled and set in Forward. This is an attempt to drive the arm back into the start zone. It should be noted that during a head load sequence at this point, if data zone is detected, the same form of recovery results.

After the arm is commanded to move a timer will be started in anticipation of detecting guard band. If this timer times out, the servo is disabled. Once in guard band, a similar time-out test occurs which if failed also results in disabling the servo. Following exit of guard band, if a track crossing is not detected within an appropriate time-out, the servo will also be disabled.

The Disable Servo Routine (DISSVO) is described in Figure 4-22.



FF468a FIGURE 4-12. MAIN IDLE MODULE (SEAGATE INTERFACE)

(E) RETURN TO ZERO MODULE (CDC INTERFACE)

When the Home (RTZ) module is called, the actuator should not be in the guard band (see Figure 4-15). If it is, the Disable Servo routine is called. Anytime the Disable Servo is applied, a return is made immediately afterward to the caller of the Return to Zero module.

If no guard band is detected, a seek to cylinder 10 is done if the actuator is on a large cylinder number. Then the home velocity is set, reverse coarse mode is set, and guard band disabled.

The servo is expected to enter the guard band next. If it doesn't, the Disable Servo routine is applied. When guard band is detected, the direction is set to forward, and the guard band is expected to disappear. If it doesn't, the Disable Servo routine is applied. When guard band becomes false, a track crossing interrupt is expected. If none is detected, the Disable Servo routine is applied. When the interrupt is received, even and fine modes are set, and guard band is enabled.

The servo should be entering the data zone. If it doesn't, the Disable Servo routine is called. When the data zone is detected, firmware registers are cleared, write current set, and some settling time allowed for the actuator before return.

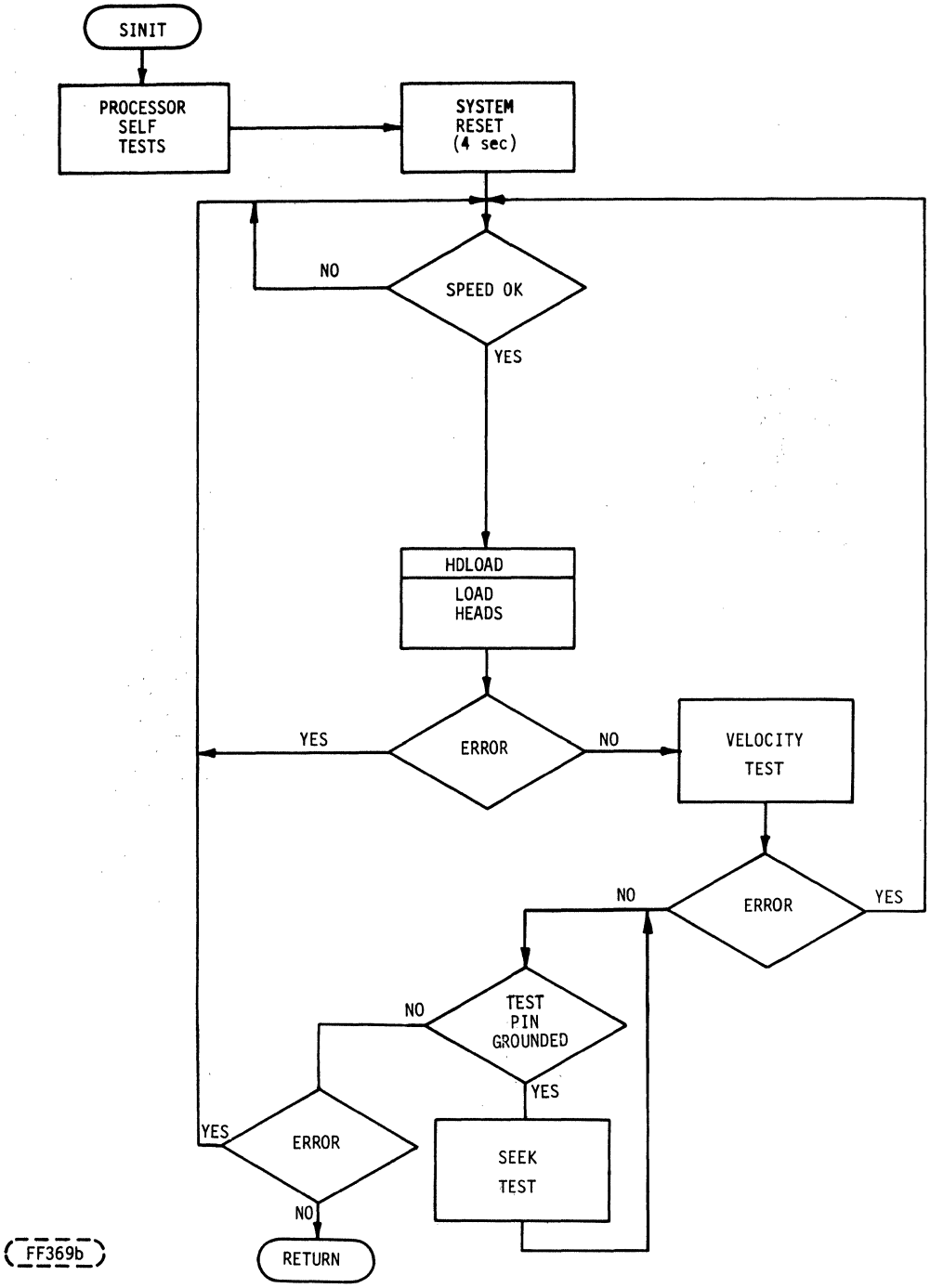
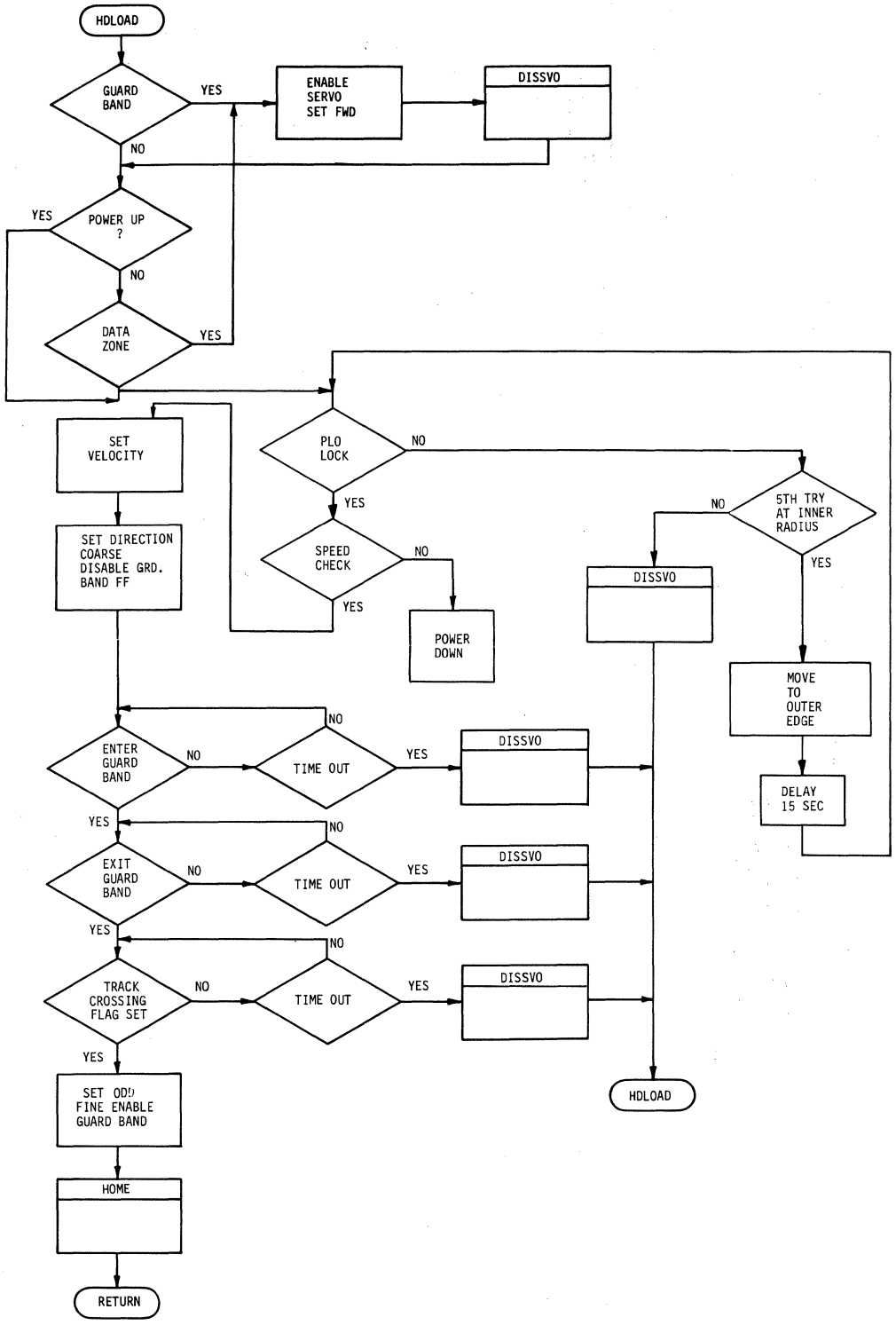


FIGURE 4-13. SYSTEM INITIALIZE (CDC AND SEAGATE INTERFACES)



FF370a

FIGURE 4-14. HEAD LOAD (CDC AND SEAGATE INTERFACES)

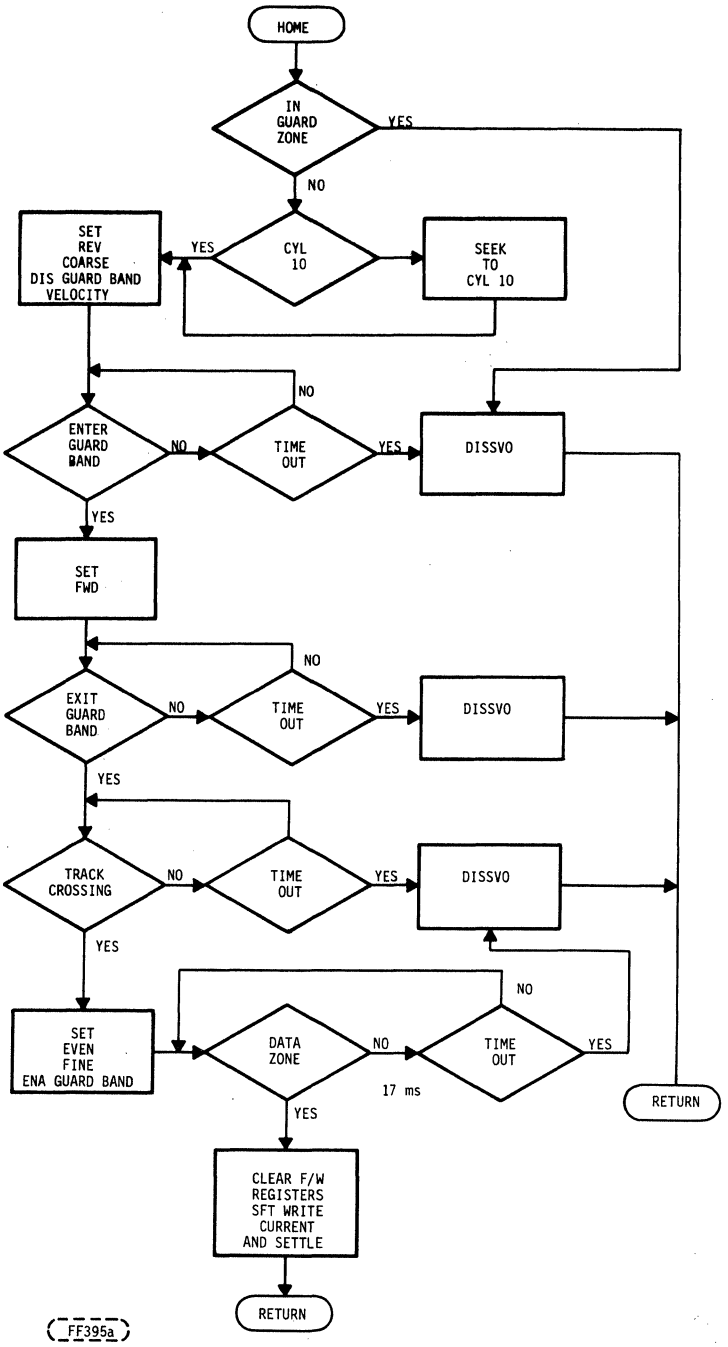


FIGURE 4-15. HOME (RTZ)
(CDC INTERFACE)

(F) EXECUTE SEEK (CDC AND SEAGATE INTERFACES)

When a Step pulse is received from the command interface, a branch is made from the Main Idle Loop into the Seek module (Figure 4-16). First a Seek Initialize routine is carried out. This will be covered in a later paragraph. Next the seek length is calculated based on a number of Step pulses that have been received to this point. A test is performed to determine if the seek length has exceeded the limit of the data zone. If this occurs, an automatic RTZ is performed by branching to the Home or RTZ module. If the step limit has not been exceeded, a branch is made to Seek Execution module. On return from the seek module, the program will continue into the Seek Terminate module, and finally a return to the idle mode.

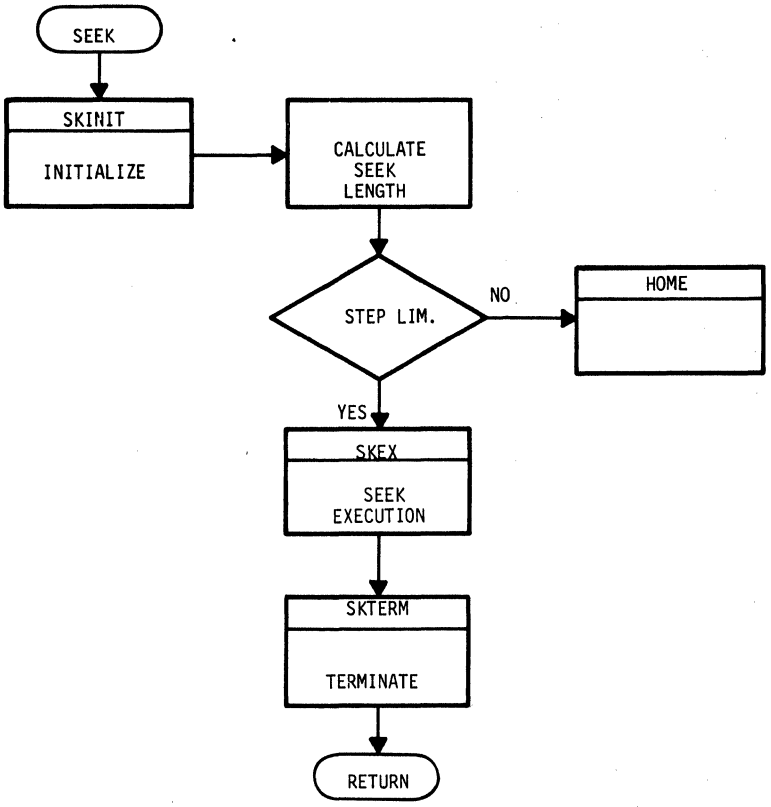
(G) SEEK INITIALIZE MODULE (CDC AND SEAGATE INTERFACES)

In the Seek Initialize module (Figure 4-17), the direction input is read and stored. Next all initial conditions are saved and the step limit, or a number of steps acceptable without exiting the data zone, is calculated. There is then a return to the seek module.

Once a seek has started, when a cylinder is crossed, a track crossing interrupt will be received (Figure 4-19). When servicing the interrupt, the current address counter is updated. Next the track-crossing flag will be set, the interrupt logic will be cleared and there is a return to the sending module.

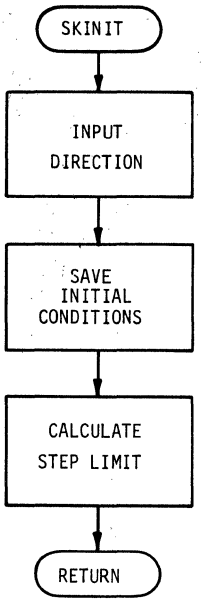
(H) MULTI TRACK SEEK MODULE (CDC AND SEAGATE INTERFACES)

The Seek Execution module (Figure 4-16) first sets the direction and coarse mode, then a large loop is entered. While the seek is taking place, the status is monitored. If an error occurs, the servo is disabled. The step count is also monitored. A step limit has already been established at this point, and if it is exceeded, a return is made to the main seek module. Each time the step count is determined, the number of steps left can be calculated. This value will determine the velocity to send. This loop is exited when only one step is left in the seek, at which time it must be determined if this was a one-track seek to begin with or not. If it was, nothing is done to the velocity at this point, but if this was a multi-track seek, an intermediate velocity is sent out. Then when track center is observed, the one-track seek velocity is sent. In either case, the last track-crossing interrupt is expected. If it does not come soon enough (or if track center does not come for a multi-track seek) the Disable-Servo routine is called and a return made to the main seek module. If the last track-crossing interrupt is detected, the new track address is calculated, fine mode is set, and return is made to the main seek module.



FF387d

FIGURE 4-16. EXECUTE SEEK
(CDC AND SEAGATE INTERFACES)



F212b

FIGURE 4-17. SEEK INITIALIZE
(CDC AND SEAGATE INTERFACES)

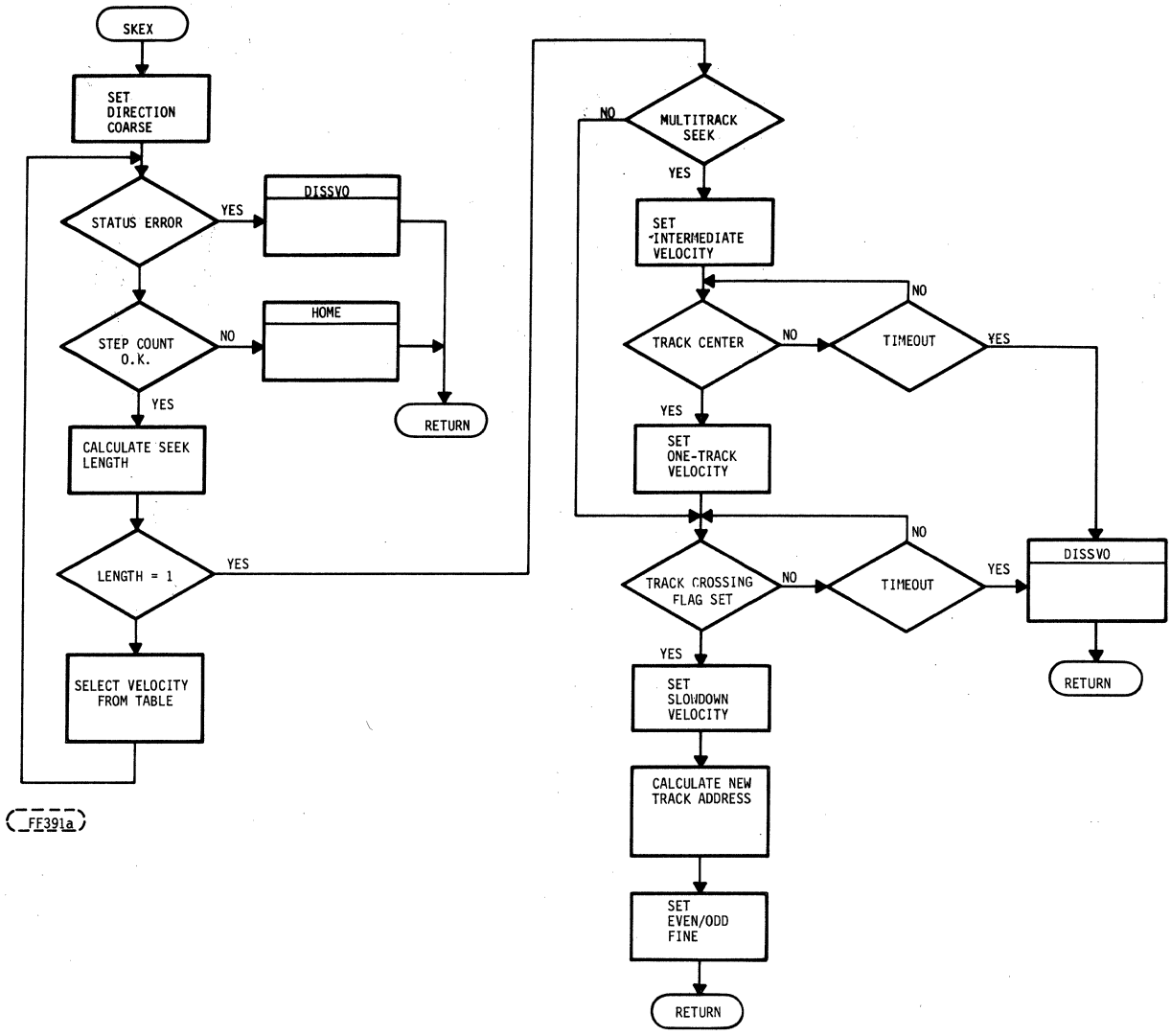


FIGURE 4-18. MULTI-TRACK SEEK (CDC AND SEAGATE INTERFACES)

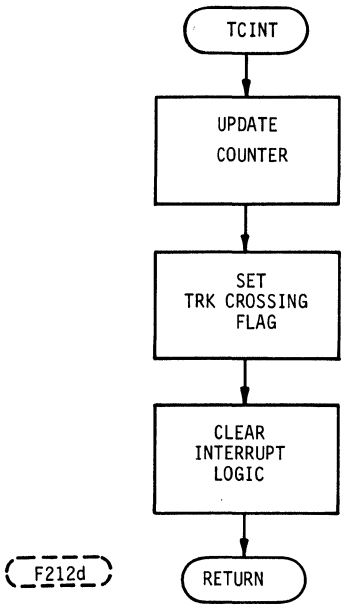


FIGURE 4-19. TRACK CROSSING INTERRUPT
(CDC AND SEAGATE INTERFACES)

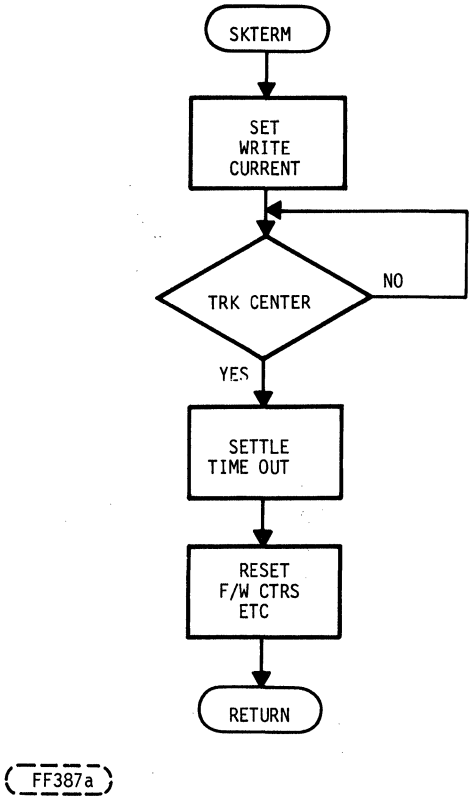


FIGURE 4-20. SEEK TERMINATE
(CDC AND SEAGATE INTERFACES)

(I) TRACK CROSSING INTERRUPT MODULE (CDC AND SEAGATE INTERFACES)

The Track Crossing Interrupt updates the counter that records which track the head is on. It also sets a track crossing flag so that the multiseek module knows when a track is crossed.

(J) SEEK TERMINATE MODULE (CDC AND SEAGATE INTERFACES)

The Seek Terminate module is used to complete a seek. The system is in Fine mode upon entering this module. First an eight-bit word is output on Port 1. This word sets the write current level used if a write command is received for this cylinder address. Then a track-center signal is detected which starts a settling timeout. This lasts approximately three microseconds. Lastly, firmware counters are reset.

(K) ERROR RECOVERY MODULE (CDC AND SEAGATE INTERFACES)

The Recover module (Figure 4-21) first checks the PLO lock, if the PLO is unlocked, filter runout is checked. If not, a check for servo error is made. Filter runout is checked on error. Next guard band is checked, if guard band is found, the guard band filter runout is checked. If guard band is not found, control is turned back to the calling module. This completes the fast recover module. If filter runout is not all right, Disable servo is called first.

(L) DISABLE SERVO MODULE (CDC AND SEAGATE INTERFACES)

In the Disable Servo Routine (Figure 4-22) the following lines are set inactive:

- Guard band latch
- Ready

The track-crossing interrupt and step counter are also disabled. Then a re-entry counter is incremented and tested to see if this is the sixth pass. If it is, the processor stops and will do nothing until the drive is powered down and up again. If not, control is returned to the calling module.

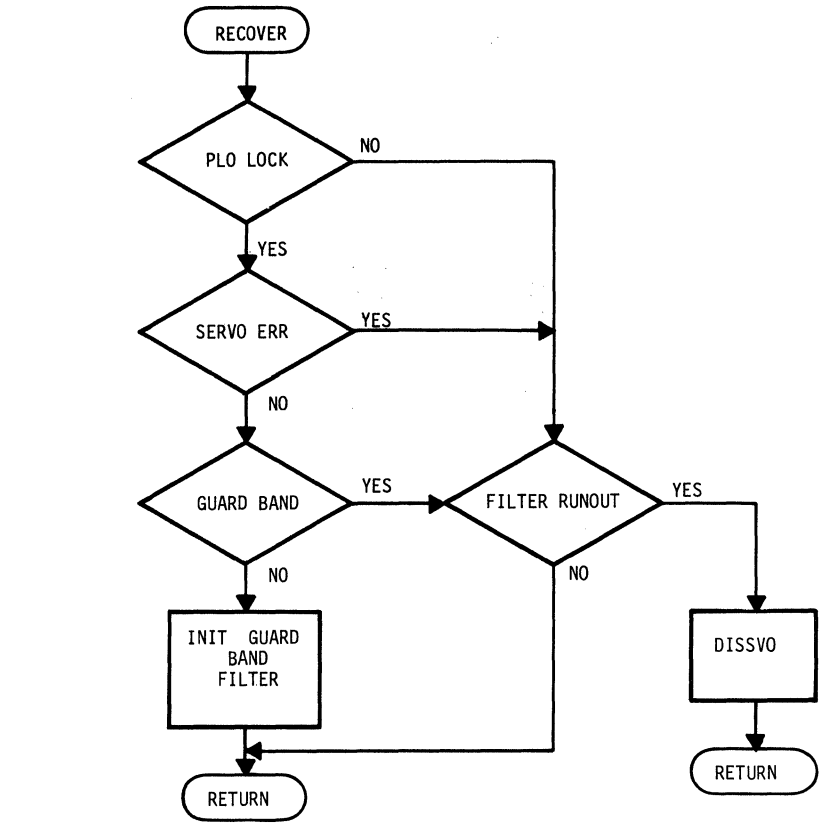
4.3.3 HEAD POSITIONING SYSTEM (CDC AND SEAGATE INTERFACES)

4.3.3.1 GENERAL (CDC AND SEAGATE INTERFACES)

The data heads are positioned on the disk by a closed loop servo system (Figure 4-23). Mounted on the same actuator as the data head is a servo head which reads the specially formatted information on the servo surface (lower surface of the bottom disk). This information is decoded and amplified for the error signal needed to keep the actuator on track. The microcomputer provides a command signal to move from track to track.

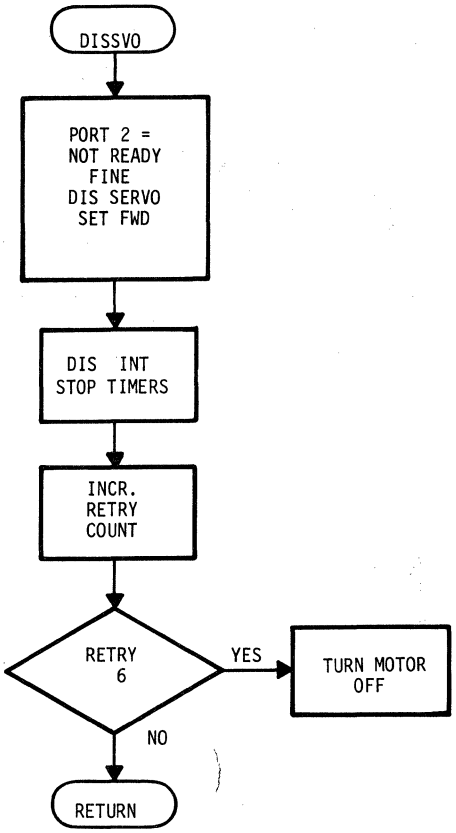
The servo system contains a position loop, a velocity loop and a current loop. Figure 4-23 is a simplified block diagram of the servo system. The current loop is analog while the velocity and position loops are a combination of digital and analog circuitry. The compensation loops are not shown for simplicity. The positioning servo system utilizes velocity information that is obtained by differentiation of position signals.

The positioning operation begins when the system controller sends a step and direction command. The microcomputer then initiates and controls the seek. There are times when the microcomputer initiates a seek without a system controller command. Initial head-load and recovery from faults are two of these times.



FF387b

FIGURE 4-21. RECOVER (CDC AND SEAGATE INTERFACES)



FF387c

FIGURE 4-22. DISABLE SERVO (CDC AND SEAGATE INTERFACES)

The microcomputer counts the number of tracks to be traversed and searches a velocity profile table for the correct velocity command code. The microcomputer outputs a digital number representing the initial velocity taken from the velocity profile table. A digital to analog converter generates an analog voltage which is amplified and applied to the actuator voice coil. The microcomputer also switches the servo circuit into the velocity mode. This begins the move to the destination track and causes information on the servo surface to be decoded into a velocity feedback signal. Each time the center of a track is crossed, the servo circuitry detects it and informs the microcomputer. The target track distance is then recalculated. As the heads approach the target track the microcomputer reduces the velocity. When the heads are within less than one-half track of their destination the microcomputer switches the servo to the fine mode.

In the fine mode the information on the servo surface is decoded into positional feedback. The microcomputer also decides if the target track is odd or even and sets a line to tell the servo circuit which track to center on.

4.3.3.2 SERVO SURFACE FORMAT (CDC AND SEAGATE INTERFACES)

The Servo surface is divided into four zones as shown in Figure 4-24. The data zone defines the read/write area on the other surfaces (Track 00 to 696). The guard bands have coded information to tell the drive when the heads are outside the data zone. The WREN uses a landing zone because the heads are over media at all times. Flying and landing the heads in this zone prevents damage to customer data when cycling power. The landing zone also has data to enable the servo timing circuits to synchronize during start-up. Special data on Track -79 is used during manufacturing to set the mechanical stop.

The servo format used in the WREN is composed of a five-dibit pattern. There are 2688 servo fields per track. The individual dibits within the servo field are called:

- Sync
- Code
- Even
- Odd
- Quadrature

The sync bits are used to lock the PLO which then provides the basic timing to decode the rest of the dibits. The code bit is used to mark the index and to differentiate the data zone from the guard band. The even, odd and quadrature bits are used to drive the position and velocity feedback signals.

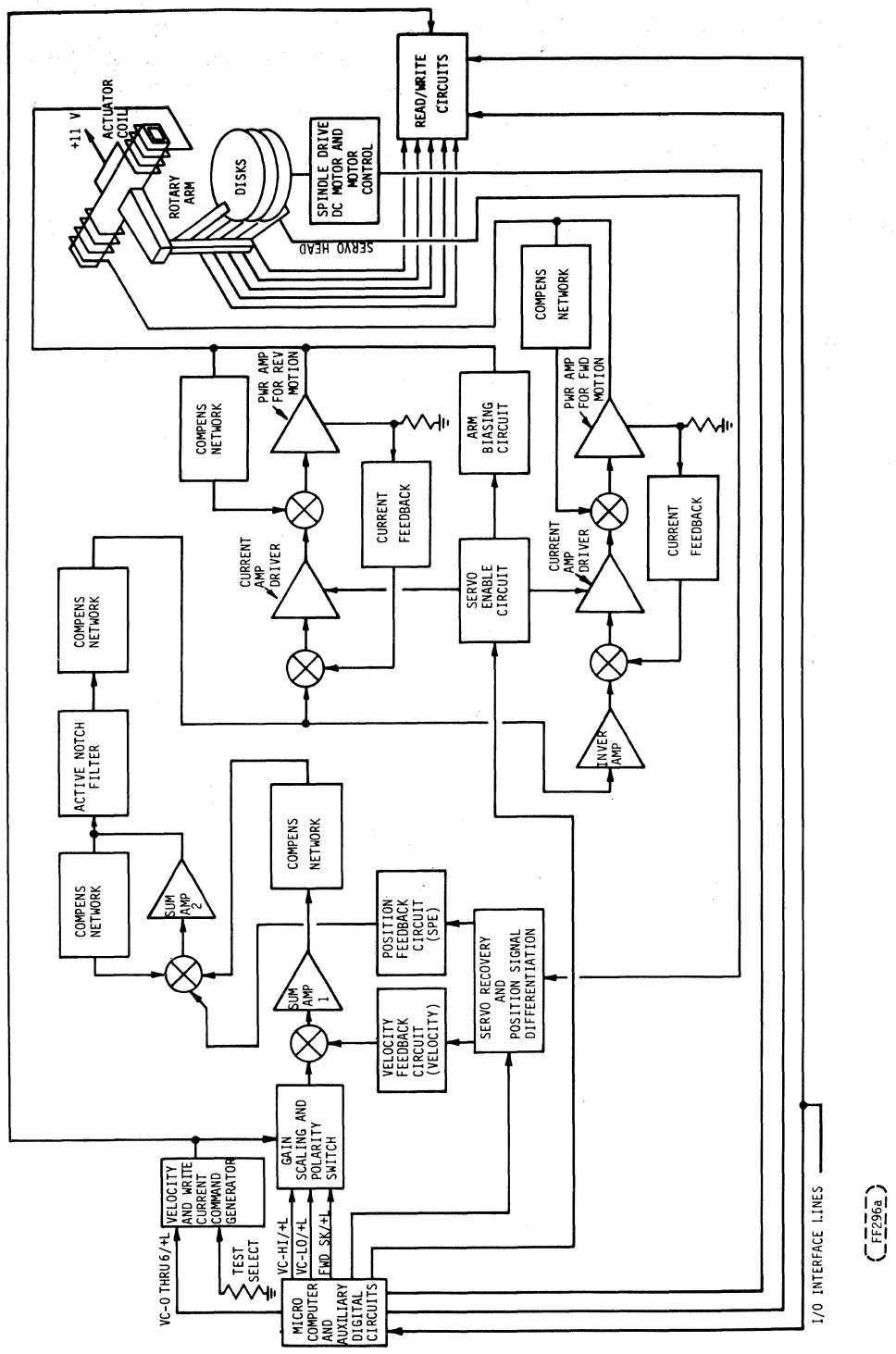


FIGURE 4-23. SERVO GENERAL BLOCK DIAGRAM (CDC AND SEAGATE INTERFACES)

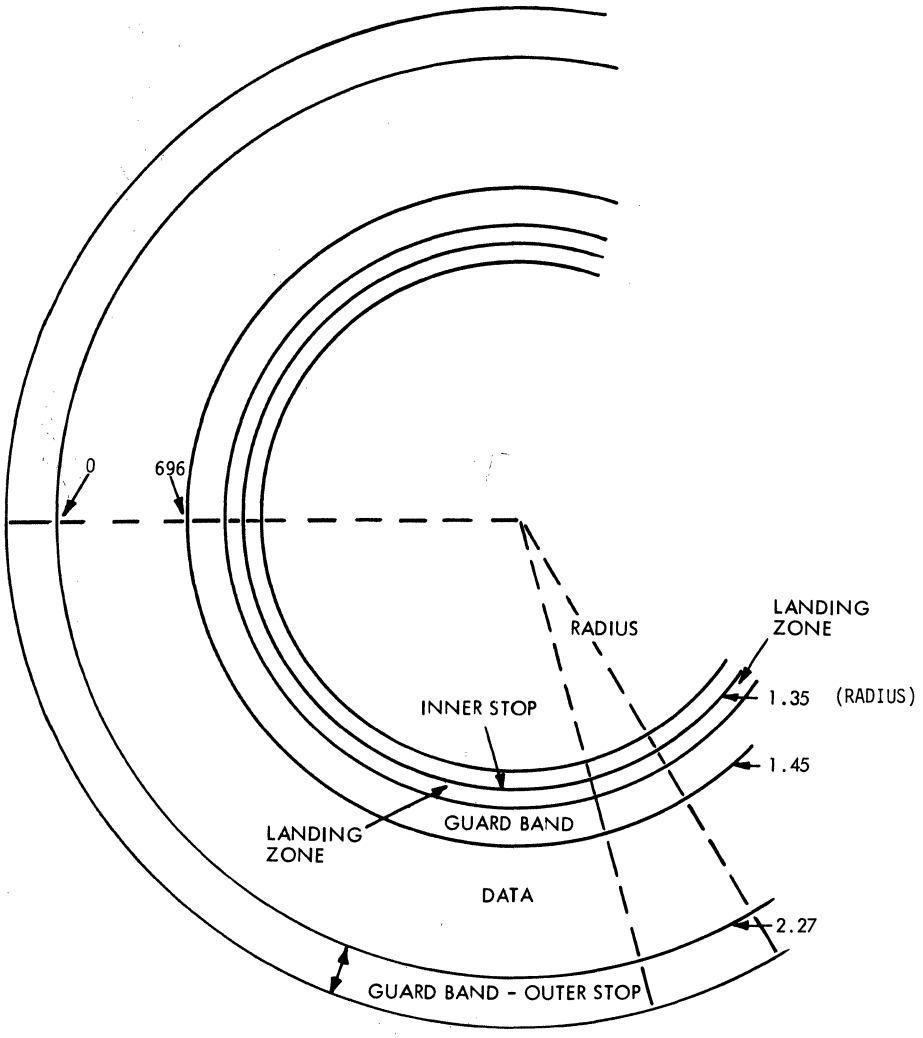


FIGURE 4-24. WREN I SERVO TRACK LOCATIONS (CDC AND SEAGATE INTERFACES)

Servo tracks come in two varieties, even and odd. All tracks have sync bits. The code bit is present in the guard band, but only in every other field. The code bit is also present for four fields at the beginning of each data track to mark the index. Only even tracks have even bits and only odd tracks have odd bits. The quadrature bit is written half on the outside of the even track and half on the inside of the odd track as shown in Figure 4-25.

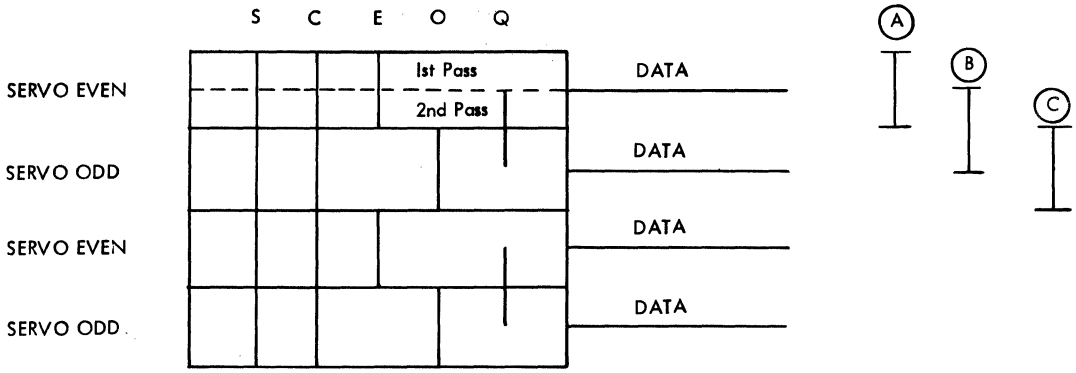
Data tracks on the other surfaces are offset one-half track from servo tracks, this means that when the servo head is halfway between an odd and even track the data head is on track center. Dibit pattern B in Figure 4-25 shows what the servo information will look like when the data head is on track center. NOTE: That the odd and even bits are of equal amplitude and the quadrature bit is a maximum amplitude. The servo circuits find the center of data tracks by subtracting the peak values of the odd dibits from the peak values of even dibits (see Figure 4-26). When this value is zero the data heads are centered. If the peak values of the quadrature dibit are also zero the track is odd. On the other hand if the quadrature dibit are at their maximum value the track is even.

When the servo is in the velocity mode the absolute value of the slope of the position signal is used as the velocity feedback. However, this slope has a discontinuity between tracks due to a change in sign. Therefore, when the position signal is over a set threshold the absolute value of the quadrature slope is used as the velocity feedback.

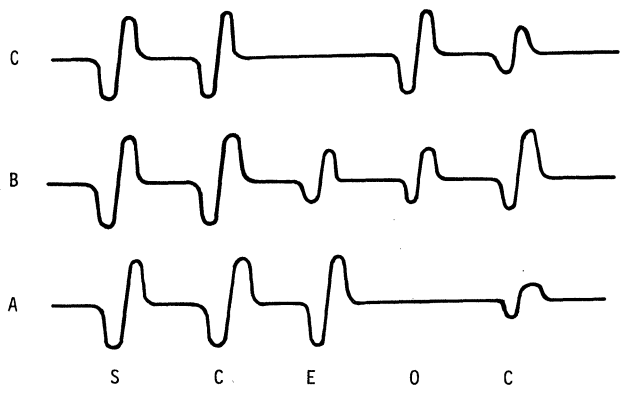
4.3.3.3 DETAILED POSITIONING SYSTEM DESCRIPTION (CDC INTERFACE)

A block diagram of the WREN Servo System is shown in Figure 4-19. Two signals derived by the Servo Analog Data Recovery circuits are position and velocity signals. A block diagram of the analog circuits used to provide these signals is shown in Figure 4-27. These signals are used by the closed loop servo system to control the seeking and positioning of the heads. The analog circuits are controlled by the digital LSI circuit, which provides the proper gating signals, and by the microcomputer.

A detailed description of the functions of the circuits shown in Figure 4-27 is as follows:



G297a



FF393a

FIGURE 4-25. DIBIT PATTERNS
(CDC AND SEAGATE INTERFACES)

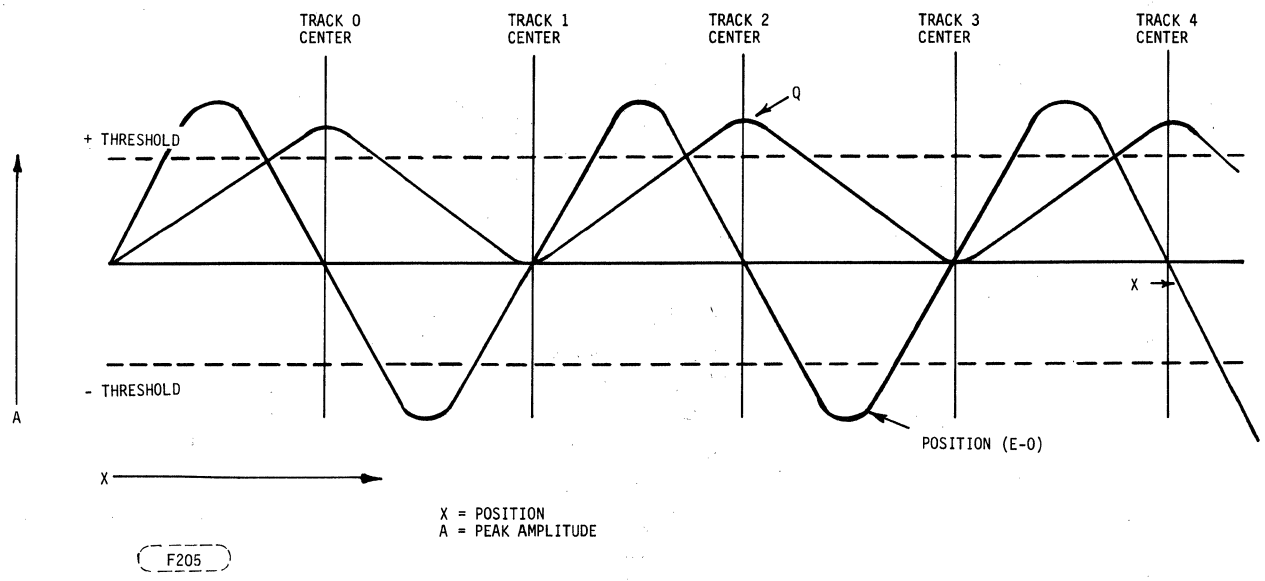


FIGURE 4-26. DERIVED POSITION AND QUADRATURE SIGNALS (CDC AND SEAGATE INTERFACES)

The signal from the servo disk is amplified by a low noise preamp (M116) and filtered. This preamp is located on the Preamp PWA. The output is sent to the Data PWA where it is again amplified (733) and filtered and applied to the Servo Analog LSI chip. The Analog LSI chip contains an automatic gain control (AGC) amp which is the controlling element in an AGC loop contained within the chip. Also in the chip is a high speed comparator with a threshold set at 50% of the peak dibit level which outputs a pulse when any dibits amplitude exceed 50% of the peak AGC level. The input signal from the 733 amp is applied to the AGC amp in the analog LSI. It is then amplified again and coupled to a buffer amp. The buffer amp drives a gated AGC current pump detector. The detector is gated such that only the sync dibit is used for AGC. The combined action of the AGC system is to produce a constant amplitude sync dibit at the output of the buffer amp. The AGC reference voltage controls the peak amplitude of the output of the buffer. This voltage is supplied externally to the LSI chip by a D/A converter circuit. The reference voltage is set up during a calibration cycle when power is applied to the drive.

The internal buffer output is also applied to three gated peak detectors which peak detect the three position dibits, even, odd and quad. The even and odd peak detectors are applied to difference amps with a gain of 4.5. The output of the difference amp is filtered by a two-pole active filter. This signal is E-O (even-odd) and is inverted to produce O-E (odd-even). These signals are shown in Figure 4-28. During seeks no position feedback is used and the position switching circuit grounds the SPE signal (servo position error). During track following mode (FINE) the position switching circuit selects either the E-O or O-E signal depending upon what polarity track (even or odd) is to be followed.

The velocity signal is developed from the position signal by taking the derivative of the E-O and O-E signals. These two velocity signals, (i.e.Ve-o and Vo-e) are applied to the velocity switches. These signals are of opposite polarity and the proper one is selected depending upon the position of the head over an even or odd track. The position of the head is determined by the servo digital LSI which detects the presence or absence of a Q dibit pulse. This signal is outputted by the LSI as Q 50 and Q 50. These two signals control what velocity feedback signal is used. As the head moves between tracks, the E-O and O-E signals become non-linear and their velocity signals are not accurate. To overcome this a quadrature dibit is written on the servo surface which is offset by 1/2 track from the even and odd dibits. This dibit is peak detected by the Q peak detector and amplified and filtered to generate the Qp signal.

This is inverted and becomes -Qp, Qp and -Qp are also differentiated to produce two other velocity signals V_Q and $-V_Q$. One of these signals is selected by comparing the amplitudes of the E-O and O-E signals. If either of these go too positive and enter their nonlinear region the velocity feedback signal is switched to the V_Q or $-V_Q$ signal. The output from the velocity switches is buffered by an amplifier (LM308A) and this output is applied to the servo error amp as the velocity feedback.

The gain of the position and velocity feedback signals is controlled by the amplitude of dibits that are peak detected. The amplitude of the dibits is set by the AGC system which is referenced to an external voltage (AGC REF VOLTAGE). By changing the reference voltage the amount of feedback to the servo loop may be changed. This fact is used to adjust the velocity feedback signal to the exact amount required independent of component tolerances, etc. This is done upon power up sequence under control of the microcomputer circuits. The microcomputer does test seeks during which it measures the velocity of the arm. If the velocity is incorrect it will increment the auto velocity adjust counter which changes the AGC REF VOLTAGE. Another test seek is performed and the process repeats until the correct velocity is achieved. This adjusts for errors associated with normal component tolerances.

Also located in the Servo Analog LSI are several comparator circuits. One of these is the Track Center Comparators which tells the microcomputer circuit that the head has reached the center of the track. This is used in the settle routine and also will indicate if the head has gone off track for some reason. Another comparator simply senses if the E-O signal is positive (E-O $>$ 0). This signal is used by the servo digital LSI in the track crossing generator circuit.

In addition to the position and velocity signals, the analog circuits of the servo system provides the following functional groups. (See Figure 4-27.)

- Velocity and write current command generator
- Actuator drive circuits:
  1. Gain scaling and polarity switch
  2. Summing amplifiers
  3. Power amplifier
- Servo system velocity feedback circuit
- Servo system position feedback and offset generating circuit
- Active notch filter and compensation networks
- Servo enable and rotary arm biasing circuit.

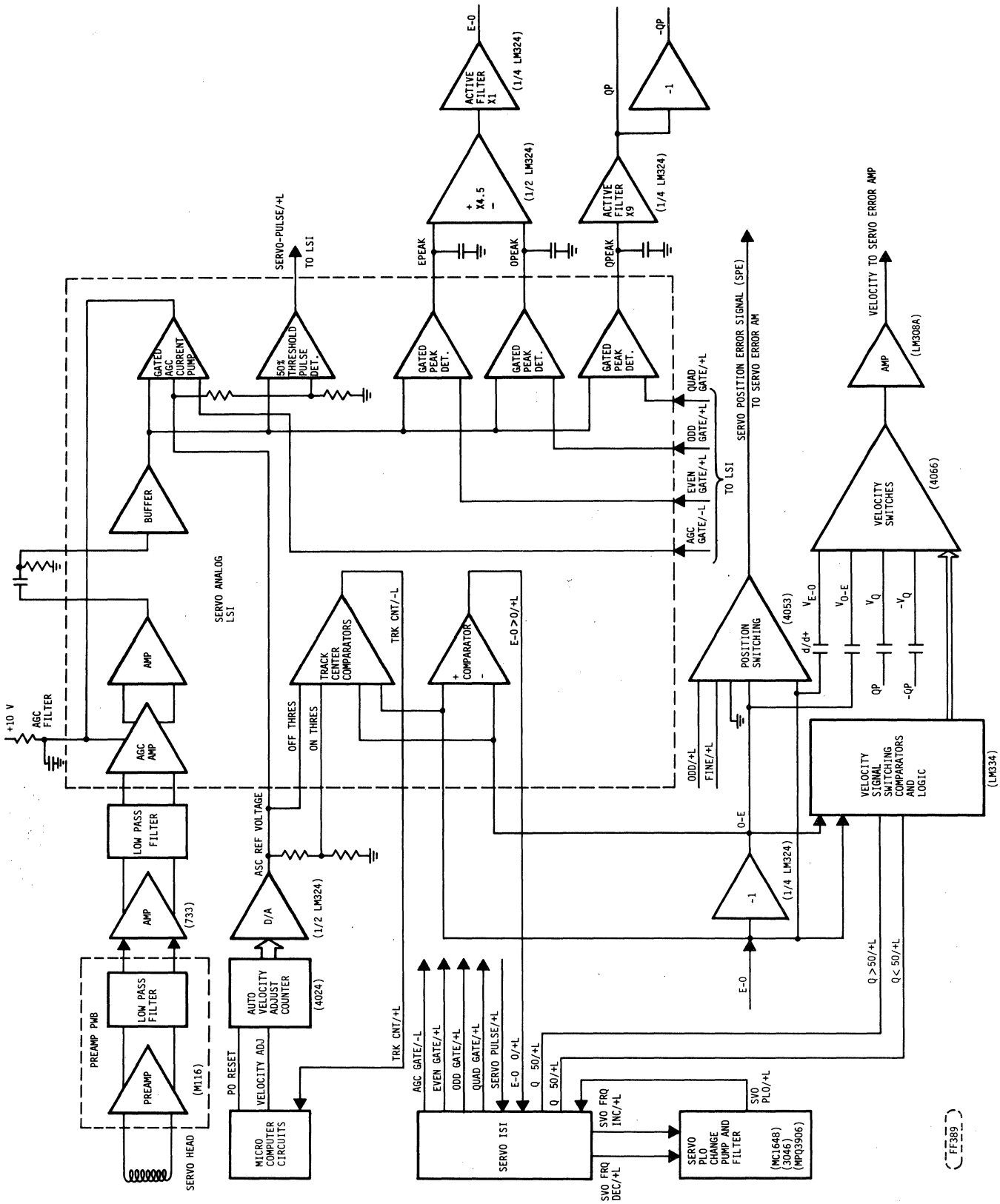


FIGURE 4-27. WREN I SERVO ANALOG DATA RECOVERY CIRCUITS (CDC AND SEAGATE INTERFACES)

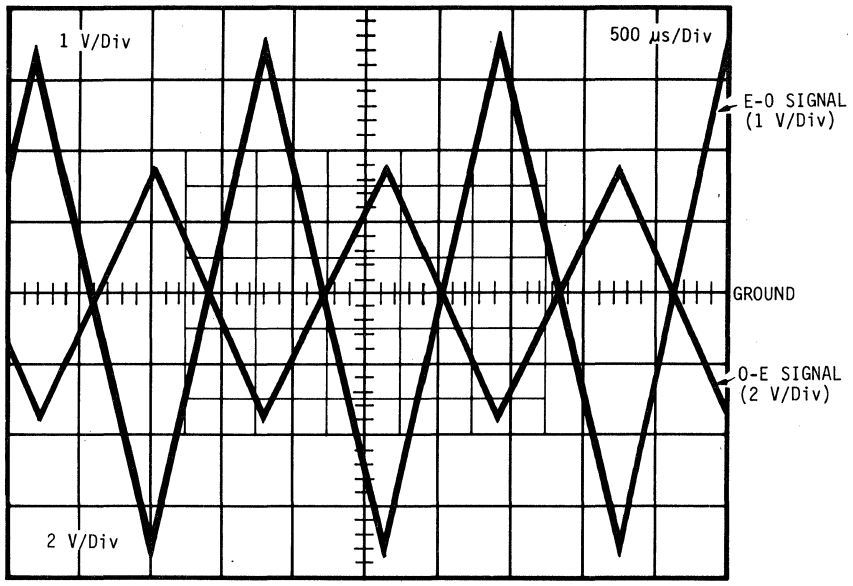


FIGURE 4-28. E-O AND O-E SIGNALS
(CDC AND SEAGATE INTERFACES)

The velocity and write current command generator is located on the Servo PWA. The microcomputer outputs a seven bit digital command by proper activation of the VC-0/+L through VC-6/+L lines to the digital to analog converter (DAC) U26. The DAC output is connected to current to voltage converter U22-1. Scaling of the DAC output is accomplished at the factory by selecting the value of the test select resistor R70. The two velocity ranges are chosen by the microcomputer by activating the VC-LO/+L or VC-HI/+L lines. The gain scaling of the amplifier U-34 is provided thru analog switches U30-14 and U30-4. The ODD/-L line controls the direction of the seek by determining the inverting or noninverting configuration of the polarity switching amplifier U22-7. When ODD/-L line is set "HIGH" the actuator drive circuits provide "REVERSE" motion of the rotary arm (from lower numbered tracks towards higher numbered tracks). When seek is complete and both lines VC-HI/+L, VC-LO/+L are set "LOW", R148 and R149 are disconnected from U22-7 and U34 output is grounded. This allows write current levels to be set at U22-1 without affecting the servo system. Summing amplifier U21 in the seek mode subtracts the velocity feedback signal from the velocity command signal to generate the velocity error signal.

The velocity error signal drives the power amplifier through amplifier U14 and active notch filter U10-7. During the seek mode the line FINE/+L is "LOW" and position feedback signal is removed. When the rotary arm is positioned on track (FINE/+L is "HIGH") the position signal will be active.

The power amplifier drives the head actuator coil. Q2 emitter resistor R21 feeds back a voltage proportional to the current in the actuator coil for "FORWARD" motion. The feedback voltage is summed with the actuator drive signal at pin 13 of U10. Q1 emitter resistor R20 feeds back a voltage proportional to the current in the actuator coil for "REVERSE" motion. The feedback voltage is summed with the actuator drive signal at pin 9 of U10.

The compensation networks (R14, C6 and R9, C7) control the gain and band width of the output stages of the Power Amp in order to insure high frequency stability. The compensation networks (R32, R33, C13 and R93, C30) control the band width of the current loop. The U14 compensation feedback network (R105, R103, C43) together with the active 2.4 kHz notch filter provides high frequency compensation in the velocity loops and attenuates frequencies that may cause mechanical resonances.

The U14 compensation feedback network (R105, R103, C43) provides low frequency compensation for the position loop.

The network (R132, R133, C58) provides low frequency compensation in the velocity loop. The noise in velocity feedback is attenuated by compensation networks (R129, R130, C57 and R131, and C56). The offset generator (U22-8) can be activated by selecting POS OFFSET/+L or NEG OFFSET/+L lines when positioning on track during read operation in order to aid full data recovery. When POS OFFSET/+L is set "HIGH" and NEG OFFSET/+L is set "LOW" (U22-8 is in inverting configuration) the rotary actuator arm is shifted towards the outer diameter of the disk from the center of the track. When POS OFFSET/+L is set "LOW" and NEG OFFSET/+L is set "HIGH" (U22-8 is in noninverting configuration) the rotary actuator arm is shifted towards the inner diameter of the disk from the center of the track. The offset command signal is summed together with position feedback signal.

Servo disable and actuator retract are controlled by DISABLE/+L line and provided by CR8, CR9, Q5, U7 (6,7,8) and Q8. The actuator retract procedure energizes the reverse winding with a controlled current to pull the arm into the landing zone. The DISABLE/+L line can be activated by both the microcomputer (UP SERVO EN/-L) and the voltage fault monitor. Voltage fault monitor sets the DISABLE/+L line "HIGH" anytime either of the external power supplies (+12 V or +5 V) or internally generated -5 V is lost. In this case RESET/-L line is set "LOW". That resets the microcomputer. Anytime the DISABLE/+L line is active, WRT INHIBIT/+L is also set "HIGH" and disables the write function.

4.3.3.4 DETAILED POSITIONING SYSTEM DESCRIPTION (SEAGATE INTERFACE)

A block diagram of the WREN Servo System is shown in Figure 4-23. Two signals derived by the Servo Analog Data Recovery circuits are position and velocity signals. A block diagram of the analog circuits used to provide these signals is shown in Figure 4-27. These signals are used by the closed loop servo system to control the seeking and positioning of the heads. The analog circuits are controlled by the digital LSI circuit, which provides the proper gating signals, and by the microcomputer.

A detailed description of the functions of the circuits shown in Figure 4-27 is as follows:

The signal from the servo disk is amplified by a low noise preamp (M116) and filtered. This preamp is located on the Preamp PWA. The output is sent to the Data PWA where it is again amplified (733) and filtered and applied to the Servo Analog LSI chip. The Analog LSI chip contains an automatic gain control (AGC) amp which is the controlling element in an AGC loop contained within the chip. Also in the chip is a high speed comparator with a threshold set at 50% of the peak dibit level which outputs a pulse when any dibits amplitude exceed 50% of the peak AGC level. The input signal from the 733 amp is applied to the AGC amp in the analog LSI. It is then amplified again and coupled to a buffer amp. The buffer amp drives a gated AGC current pump detector. The detector is gated such that only the sync dibit is used for AGC. The combined action of the AGC system is to produce a constant amplitude sync dibit at the output of the buffer amp. The AGC reference voltage controls the peak amplitude of the output of the buffer. This voltage is supplied externally to the LSI chip by a D/A converter circuit. The reference voltage is set up during a calibration cycle when power is applied to the drive.

The internal buffer output is also applied to three gated peak detectors which peak detect the three position dibits, even, odd and quad. The even and odd peak detectors are applied to difference amps with a gain of 4.5. The output of the difference amp is filtered by a two-pole active filter. This signal is E-O (even-odd) and is inverted to produce O-E (odd-even). These signals are shown in Figure 4-28. During seeks no position feedback is used and the position switching circuit grounds the SPE signal (servo position error). During track following mode (F1NE) the position switching circuit selects either the E-O or O-E signal depending upon which polarity track (even or odd) is to be followed.

The velocity signal is developed from the position signal by taking the derivative of the E-O and O-E signals. These two velocity signals, (i.e. Ve-o and Vo-e) are applied to the velocity switches. These signals are of opposite polarity and the proper one is selected depending upon the position of the head over an even or odd track. The position of the head is determined by the servo digital LSI which detects the presence or absence of a Q dibit pulse. This signal is outputted by the LSI as Q 50 and Q 50. These two signals control what velocity feedback signal is used. As the head moves between tracks, the E-O and O-E signals become non-linear and their velocity signals are not accurate. To overcome this a quadrature dibit is written on the servo surface which is offset by 1/2 track from the even and odd dibits. This dibit is peak detected by the Q peak detector and amplified and filtered to generate the Qp signal.

This is inverted and becomes -Qp, Qp and -Qp are also differentiated to produce two other velocity signals V_Q and $-V_Q$. One of these signals is selected by comparing the amplitudes of the E-O and O-E signals. If either of these go too positive and enter their nonlinear region the velocity feedback signal is switched to the V_Q or $-V_Q$ signal. The output from the velocity switches is buffered by an amplifier (LM308A) and this output is applied to the servo error amp as the velocity feedback.

The gain of the position and velocity feedback signals is controlled by the amplitude of dibits that are peak detected. The amplitude of the dibits is set by the AGC system which is referenced to an external voltage (AGC REF VOLTAGE). By changing the reference voltage the amount of feedback to the servo loop may be changed. This fact is used to adjust the velocity feedback signal to the exact amount required independent of component tolerances, etc. This is done upon power up sequence under control of the microcomputer circuits. The microcomputer does test seeks during which it measures the velocity of the arm. If the velocity is incorrect it will increment the auto velocity adjust counter which changes the AGC REF VOLTAGE. Another test seek is performed and the process repeats until the correct velocity if achieved. This adjusts for errors associated with normal component tolerances.

Also located in the Servo Analog LSI are several comparator circuits. One of these is the Track Center Comparators which tells the microcomputer circuit that the head has reached the center of the track. This is used in the settle routine and also will indicate if the head has gone off track for some reason. Another comparator simply senses if the E-0 signal is positive (E-0 $>$0). This signal is used by the servo digital LSI in the track crossing generator circuit.

In addition to the position and velocity signals, the analog circuits of the servo system provides the following functional groups. (See Figure 4-27.)

- Velocity and write current command generator
- Actuator drive circuits:
  1. Gain scaling and polarity switch
  2. Summing amplifiers
  3. Power amplifier
- Servo system velocity feedback circuit
- Servo system position feedback and offset generating circuit
- Active notch filter and compensation networks
- Servo enable and rotary arm biasing circuit.

The velocity and write current command generator is located on the Servo PWA. The microcomputer outputs a seven bit digital command by proper activation of the VC-0/+L through VC-6/+L lines to the digital to analog converter (DAC) (U25). The DAC output is connected to the current to voltage converter (U21-1). Scaling of the DAC output is accomplished at the factory by selecting the value of the test select resistor R70. The two velocity ranges are chosen by the microcomputer by activating the VC-LO/+L or VC-HI/+L lines. The gain scaling of the amplifier (U-34) is provided thru the analog switches U29-14 and U29-4. The Microprocessor controls the direction of the seek by determining the inverting or noninverting configuration of the polarity switching amplifier U21-7. When this line is set "HIGH" the actuator drive circuits provide "REVERSE" motion of the rotary arm (from lower numbered tracks towards higher numbered tracks). When the seek is complete, R148 and R149 are disconnected from U21-7 and U34 output is grounded. This allows write current levels to be set at U22-1 without affecting the servo system. Summing amplifier U20 in the seek mode subtracts the velocity feedback signal from the velocity command signal to generate the velocity error signal.

The velocity error signal drives the power amplifier through amplifier U14 and active notch filter U10-7. During the seek mode the line FINE/+L is "LOW" and position feedback signal is removed. When the rotary arm is positioned on track (FINE/+L is "HIGH"), the position signal will be active.

The power amplifier drives the head actuator coil. Q2 emitter resistor R21 feeds back a voltage proportional to the current in the actuator coil for "FORWARD" motion. The feedback voltage is summed with the actuator drive signal at pin 13 of U10. Q1 emitter resistor R20 feeds back a voltage proportional to the current in the actuator coil for "REVERSE" motion. The feedback voltage is summed with the actuator drive signal at pin 9 of U10.

The compensation networks (R14, C6 and R9, C7) control the gain and band width of the output stages of the Power Amp in order to insure high frequency stability. The compensation networks (R32, R33, C13 and R93, C30) control the band width of the current loop. The U14 compensation feedback networks (R105, R103, C43) together with the active 2.4 kHz notch filter provides high frequency compensation in the velocity loops and attenuates frequencies that may cause mechanical resonances.

The U14 compensation feedback network (R104, R103, C11) provides low frequency compensation for the position loop.

The network (R132, R133, C58) provides low frequency compensation in the velocity loop. The noise in velocity feedback is attenuated by compensation networks (R139, R130, C57 and R131 and C56).

Servo disable and actuator retract are controlled by DISABLE/+L line and provided by CR8, CR9, Q5, U7 (6,7,8) and Q8. The actuator retract procedure energizes the reverse winding with a controlled current to pull the arm into the landing zone. The DISABLE/+L line can be activated by both the microcomputer (UP SERVO EN/-L) and the voltage fault monitor. Voltage fault monitor sets the DISABLE/+L line "HIGH" anytime either of the external power supplies (+12 V or +5 V) or internally generated -5 V is lost. In this case RESET/-L line is set "LOW". That resets the microcomputer. Anytime the DISABLE/+L line is active, WRT INHIBIT/+L is also set "HIGH" and disables the write function.

4.3.4 READ/WRITE SYSTEM (CDC INTERFACE)

4.3.4.1 GENERAL (CDC INTERFACE)

The read/write functions are shown in block diagram, Figure 4-29. The digital functions are performed mostly by circuitry on the Data PWA. The analog functions are located on the Data PWA and Pre-amp PWA. In addition read preamplification and write drivers are located in a LSI preamp chip. This chip is part of a flexible PWA which is mounted on the actuator arm.

When the drive is ready, a head is selected and positioned over the proper sector to perform a read or write operation. The controller initiates a read operation by sending a TTL low on the READ-ENABLE line of the command cable. The data is sent differentially on the data cable (RD-DATA + and RD-DATA -). Read clock is also sent for timing information nd it is also sent differentially on the data cable (RD/SVO CLK + and RD/SVO CLK -).

During a write operation the WRITE-ENABLE signal on the command cable is set to a TTL low. The write data is sent on the data cable (WR-DATA + and WR-DATA -), along with the write clock (WRT-CLK + and WRT-CLK -).

The write data is sent coded as non-return to zero (NRZ) data. The drive then processes the data through a NRZ to Modified Frequency Modulation (MFM) encoder/compensator. The write compensation slightly changes the position of the data transition according to the data pattern present. This process minimizes the effects of bit crowding and frequency variations during readback. The compensated data is then written on the disk by the write driver and preamp circuits.

4.3.4.2 PRINCIPLES OF MFM RECORDING (CDC INTERFACE)

To maximize the amount of data stored on the disk, the frequency of the flux reversals must be carefully controlled. Several recording methods are available and each has its advantages and disadvantages. The WREN uses the MFM technique.

The time required to define one bit of information is called a cell. Each cell is nominally 206.6 ns in width. The data transfer rate is therefore, nominally 4.84 mega data bits/sec.

MFM defines a 1 by writing a flux transition at mid cell time. It defines a 0 by writing a flux transition at the end of cell time except when the cell is followed by a 1 in which case no flux transition is written in that cell.

The advantage and disadvantages of MFM recording are listed below:

- Fewer flux reversals are needed to represent a given binary number because there are no compulsory flux reversals at the end of cell boundaries. This results in higher recording densities of data without increasing the number of flux reversals per inch.

- Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency. This is true because fewer flux reversals are required for a given binary number.

- Pulse polarity has no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic and high quality recording media.

4.3.4.3 DIGITAL READ/WRITE CIRCUITRY (CDC INTERFACE)

The heart of the digital circuitry is a custom LSI chip (U4). This chip has three primary functions which are listed below:

1. Write data synchronization and pre-compensation is the first function. NRZ data from the controller is synchronized to the speed of the disk by the servo PLO. The NRZ data is then encoded to MFM data and sent to a delay line external to the LSI chip. Three different delay signals are then returned to the chip for mixing. An early-shift decoder and a late-shift decoder determine whether the MFM data should be shifted early or late to pre-compensate the write data. The delay-select logic then controls the mixing of the delay data lines and the pre-compensated write data is sent to the R/W analog PWA for processing.

2. The write fault logic detects write faults if any of the following conditions are true during write enable:

   a. Drive not ready.
   b. Read enabled.
   c. Unsafe from the pre-amp PWA.
   d. Offset strobe is true. (Head not close enough to track center.)

3. The read data is synchronized and decoded. The read PLO phase detector synchronizes the read clock to the disk speed. The read clock then is used to synchronize the read data which is received from the analog data recovery circuitry. The MFM data is then converted to NRZ data and sent to the controller.

Figure 4-30 depicts the synchronization and pre-compensation circuitry inside the Read LSI. The write data and write gate are synchronized with the write clock and the PLO clock. This compensates for any delay that may be induced in the interface. The PLO clock is then divided by two, to produce a two phase clock which clocks the retimed data into two shift registers. The data is taken from register A (a four bit register) and encoded into MFM data. This data is sent to an external delay line and three sets of data are returned. The early data has no delay, the on time data has twelve nanoseconds (ns) of delay and the late data has twenty four ns of delay. The output of the two shift registers is combined and used to select which data will be sent on as compensated data.

The delay select logic analyzes the NRZ data and determines if the frequency is increasing, decreasing or constant. This is then used to pre-compensate the data which improves the performance on subsequent read operations.

The frequency is constant if all ones or all zeros are being recorded because all flux transitions are separated by one cell time (206.6 ns). However, a 011 pattern has an increasing frequency because there is one and one half cells between the 01 and only one cell between the 11. On the other hand 110 has a decreasing frequency because the 11 has one cell time and the 10 has one and one half. These are two examples as the actual patterns are more complex. In addition patterns will overlap which will make the detection even more complex.

The output of the delay select logic enables either the early, late or nominal gate. If the frequency is constant, there will be no peak shift and the data that has been delayed 12 ns will be selected. If the frequency is decreasing the apparent readback peak would occur later than nominal. To compensate the data is not delayed and is therefore 12 ns earlier than nominal. If the frequency is increasing the apparent readback peak would occur earlier than nominal. Therefore the data is delayed 24 ns which is 12 ns later than nominal. After the properly delayed data is selected it is sent on to the read/write analog PWA.

The read phase locked loop is used as part of the read data recovery system. A block diagram is shown in Figure 4-31. When a read operation is not in progress the READ-ENABLE line selects phase detector "B" to provide the up and down control. The up control adds current to the charge pump and the down subtracts it. The loop filter converts the current to a voltage which controls the voltage controlled oscillator (VCO). The VCO output is then divided by two and fed back to the phase detector. Both outputs of the divider are used (READ-PLO-0 and READ-PLO-1). When the loop is locked the up and down controls will be of equal time. The down control is turned on when the servo PLO goes high and turned off when the servo PLO goes low.

The down control is turned on when VCO/2 goes low and turned off when servo PLO goes high. The VCO is thereby adjusted until VCO/2 is equal to the servo PLO and is in phase with it. When read is enabled phase detector "A" is selected and the read PLO will track the read data in the same way. In this way the read PLO will have a transition at each half cell. The read data, however, is half the frequency of the servo PLO and therefore the VCO must change frequency. To speed this process the gain of the charge pump is increased. This is done with the WIDE BAND ENABLE line. This line goes low for 58 bits (about 12 microseconds) at the start of each read. The read must have a sync field to allow the PLO to sync. The customer can change the phase relationship of the read PLO and the read data from the interface with the EARLY/OFFSET PLUS/-L and LATE/OFFSET MINUS/-L lines. This is useful in recovering data from marginal areas of the disk. The read PLO and the read data are then used to convert the read data to NRZ data.

Additional circuitry is also needed for level translation. Three types of translation is done. Differential to single ended is needed for signals coming from the interface. Single ended to differential is required for signals going to the interface. ECL to TTL is used for some internal signals.

4.3.4.4 ANALOG READ/WRITE CIRCUITRY (CDC INTERFACE)

The magnitude of the write current is controlled as a function of the cylinder address. The microcomputer uses the same digital to analog converter (D/A) that was used for the velocity command. The D/A is set to zero for the inner tracks where the write current is minimum. It is set to 83 for the outer tracks which need the maximum write current. The output of the D/A will vary from zero to about 2.85 volts. The write current is therefore changed about every eight tracks. The WRITE CURRENT signal passes to the preamp chip which generates an equal current to do the actual writing.

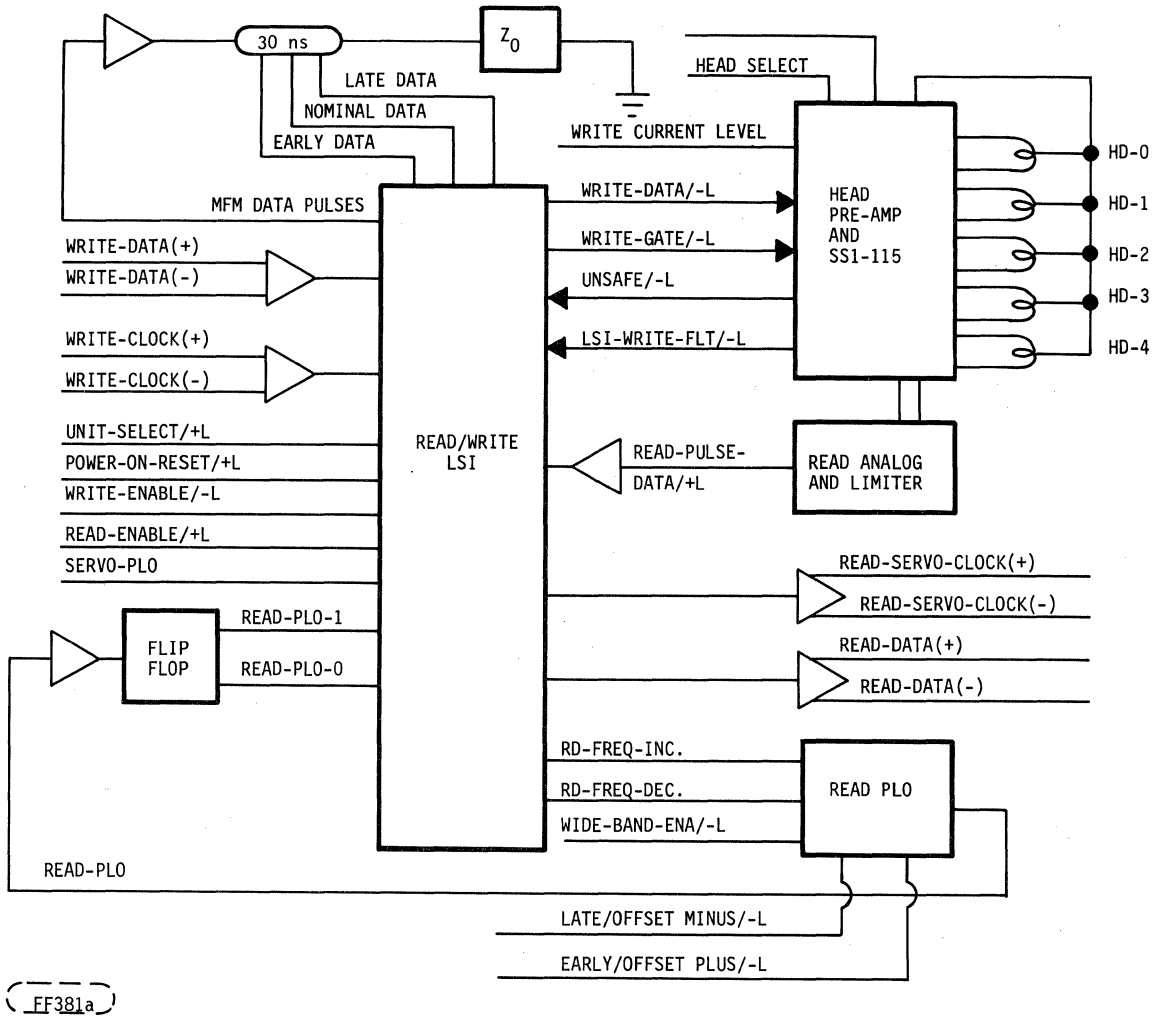


FIGURE 4-29. WREN I DATA BLOCK DIAGRAM (CDC INTERFACE)

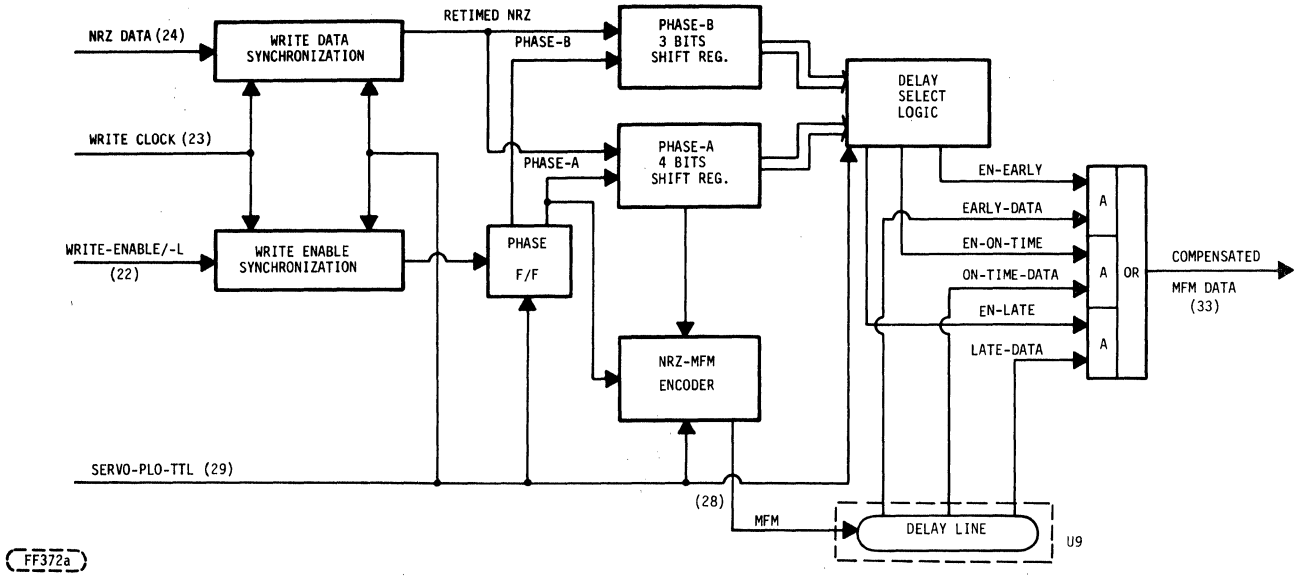


FIGURE 4-30. MFM ENCODER-COMPENSATOR INSIDE THE READ/WRITE LSI (CDC INTERFACE)

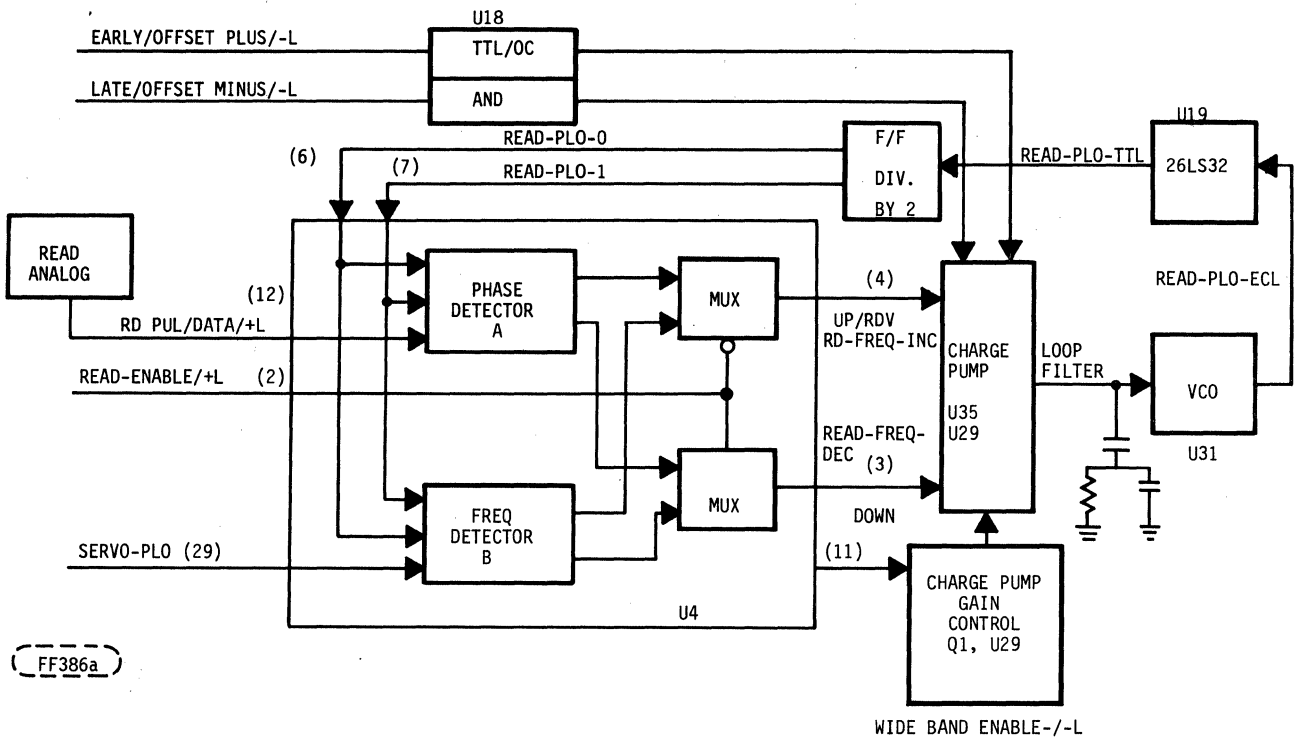


FIGURE 4-31. READ PLO (CDC INTERFACE)

Figure 4-32 is a block diagram of the Pre-Amp PWA. When the write gate is enabled the write data is clocked into the write data flip-flop. The single ended data is converted to differential data to provide both inverted and non-inverted outputs. The data is then sent on to the preamp.

The WRITE SELECT/-L signal is an active low TTL level signal to enable writing. The write enable circuit controls the following:

1. The write data circuit which was explained above can be disconnected to allow reading.

2. The WRITE SELECT/-L puts the preamp in the write mode. When write select is inactive the preamp will be in the read mode.

3. The write current level circuit which controls the magnitude of the write current is disabled by the unsafe signal. This is used to prevent data destruction during power interrupts.

The unsafe latch is set by an unsafe signal generated by the head preamp. It disables the write current and sets the unsafe latch. The unsafe latch holds the write select, write current, and write enable circuits disabled until they are reset by the controller or the digital circuits.

When the disk drive is not writing, the signal from the Read/Write heads is amplified by the head preamp located at the head flex cable close to the head. By being near the heads the signal to noise ratio is improved. The signal is amplified (39 times nominal) and sent through the flex cable in a differential mode outside the sealed unit.

This signal is received by the pre-amp PWA as RD-DATA-N and RD-DATA-P. The amplitude of this signal is in the millivolt range. A three pole linear phase low pass filter reduces the high frequency noise of the signal. The signal is amplified and processed by a pulse-slimming network. The pulse-slimmer improves the signal resolution and conditions it for signal detection and recovery. This enhanced signal is amplified and applied differentially as RD-ANALOG-N and RD-ANALOG-P to the data PWA (see Figure 4-33).

The preamp PWA also amplifies the servo signal that comes from the servo head. This signal is then filtered and sent differentially as SERVO-ANALOG-N and SERVO-ANALOG-P to the data PWA.

The read circuitry of the read/write analog PWA (see Figure 4-33) converts the preamplified analog read data to digital MFM data and sends it to the R/W LSI to be decoded. The data is first attenuated by a FET for gain control. The signal is then amplified and sent through a five pole linear phase filter to improve the signal to noise ratio. The signal is differentiated to convert the signal peaks to zero-crossings by an active differentiator for good common mode rejection.

At this point the data is split into three parallel paths. In the AGC circuit path the signal is peak detected and filtered. The peaks are averaged by a current amplifier and a capacitor. Controlling the attenuator with this voltage gives the circuit automatic gain control. The two remaining data paths are the high resolution and low resolution channels. In the high resolution path no further filtering is added. The signal is buffered and sent through a delay line.

The low resolution path adds a low pass filter to reject high frequency components (mostly third harmonics). This reduces the possibility of extraneous zero-crossing when the data frequency is low. This also induces a phase lag so that the signal now matches the delayed high resolution signal.

Both path signals are now converted to digital type signals by sending them through differential comparators. The signals are then sent to a pair of flip-flops which resolve the differences. The high resolution data clocks both flip-flops and the low resolution data enables them. Therefore the low resolution data acts as a qualifier and eliminates false transitions without changing true ones. The outputs of the flip-flops are wire-ored to produce a pulse for each flux transition. This data is then sent to the R/W LSI to be decoded into NRZ data. The timing diagram (see Figure 4-34), shows the waveform relationships. FET Q3 is turned on during the write mode to clamp the signal into the PWA. This limits the amplitude of the signals to read circuits seen during writing. This reduces the time required to switch from writing to reading.

4.3.5 READ/WRITE SYSTEM (SEAGATE INTERFACE)

4.3.5.1 GENERAL (SEAGATE INTERFACE)

To maximize the amount of data stored on the disk, the frequency of the flux reversals must be carefully controlled. Several recording methods are available and each has its advantages and disadvantages. The WREN with the Seagate Interface uses the MFM recording method.

The time required to define one bit of information is called a cell. Each cell is nominally 200 ns in width. The data transfer rate is therefore, nominally 5.0 mega data bits/sec.

MFM defines a 1 by writing a flux transition at mid cell time. It defines a 0 by writing a flux transition at the end of cell time except when the cell is followed by a 1 in which case no flux transition is written in that cell.

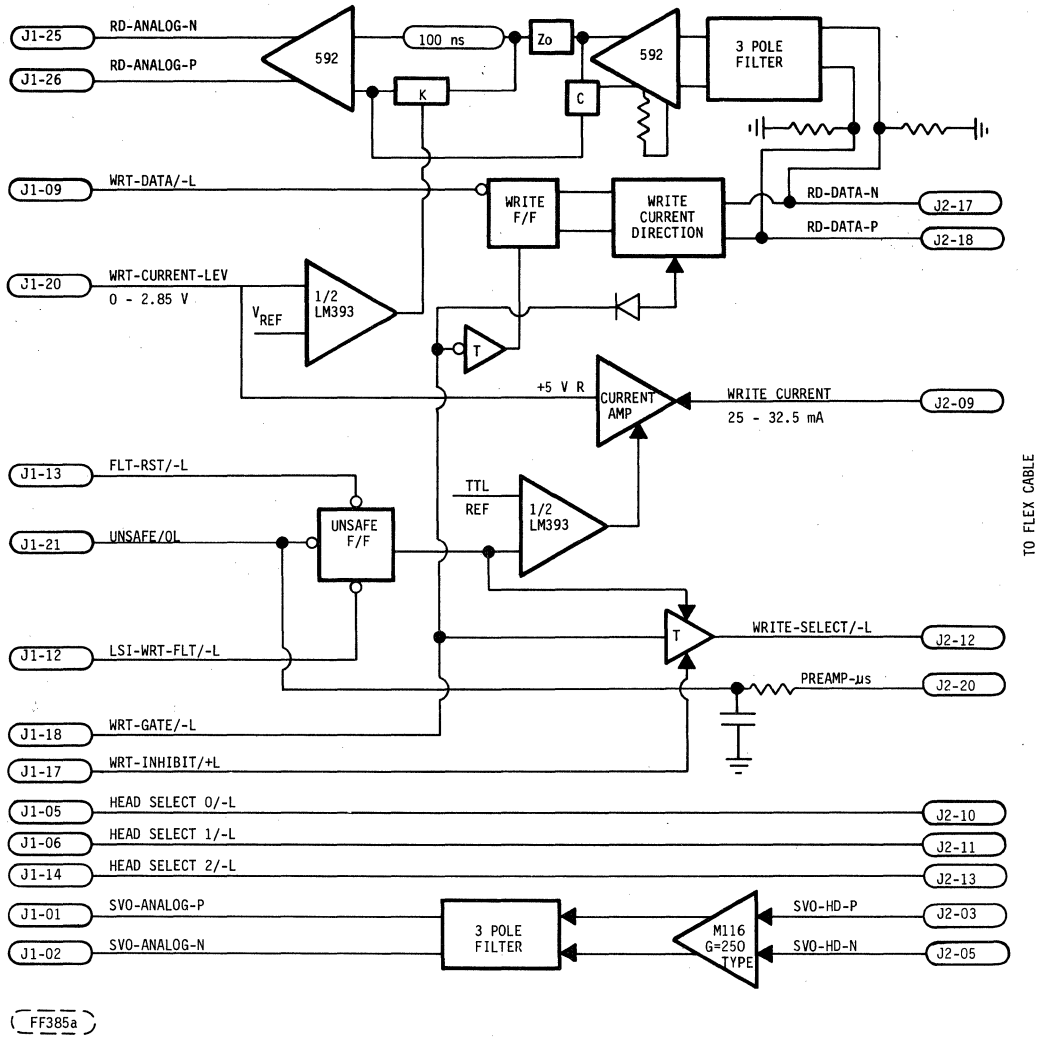


FIGURE 4-32. PRE-AMP BLOCK DIAGRAM (CDC INTERFACE)

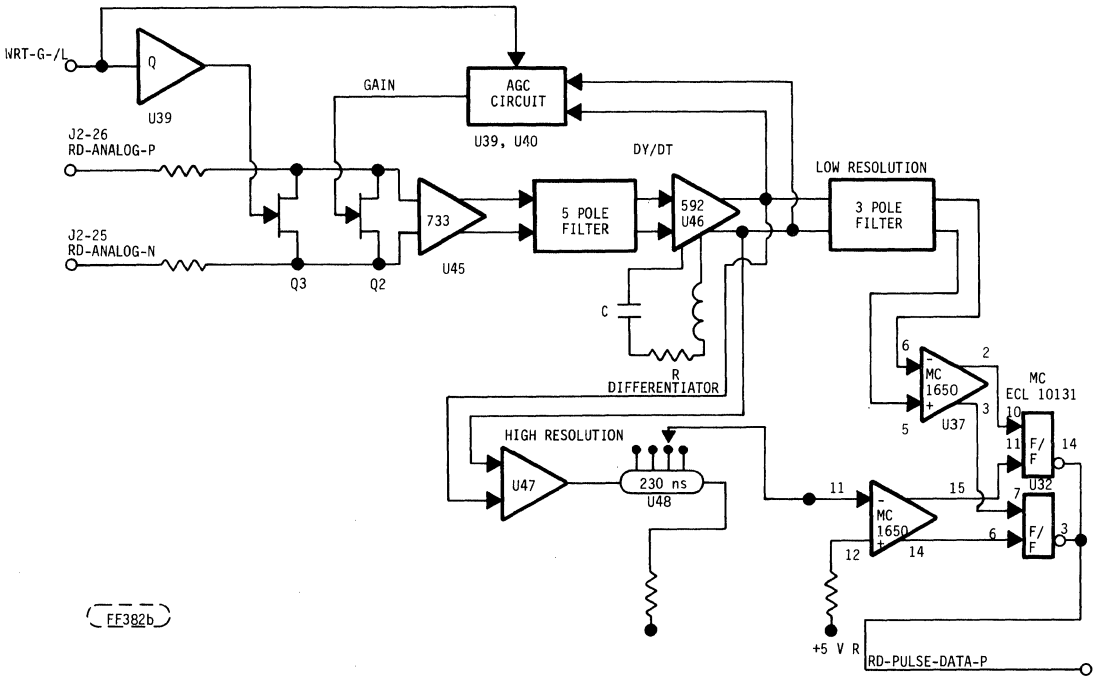


FIGURE 4-33. DATA PWA READ ANALOG FUNCTION (CDC INTERFACE)

The advantages and disadvantages of MFM recording are listed below:

- Fewer flux reversals are needed to represent a given binary number because there are no compulsory flux reversals at cell boundaries. Therefore, higher recording densities of data are achieved without increasing the number of flux reversals per inch. The number of flux reversals varies from a maximum of one reversal per bit (all "1's" or all "0's") to a minimum of one reversal for every two bits (alternating "1's" and "0's").
- Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency achieved because of fewer flux reversals required for a given binary number.
- Transition polarities have no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic which include a PLO and high quality recording media.

4.3.5.2 WRITE CIRCUITS (SEAGATE INTERFACE)

The magnitude of the write current is changed as a function of the cylinder address. The microcomputer uses the same digital to analog converter (D/A) that was used for the velocity command. The D/A is set to zero for the inner tracks where the write current is minimum. It is set to 83 for the outer tracks which need the maximum write current. The output of the D/A should vary from zero to about 2.85 volts. The write current is therefore increased about every eight tracks.

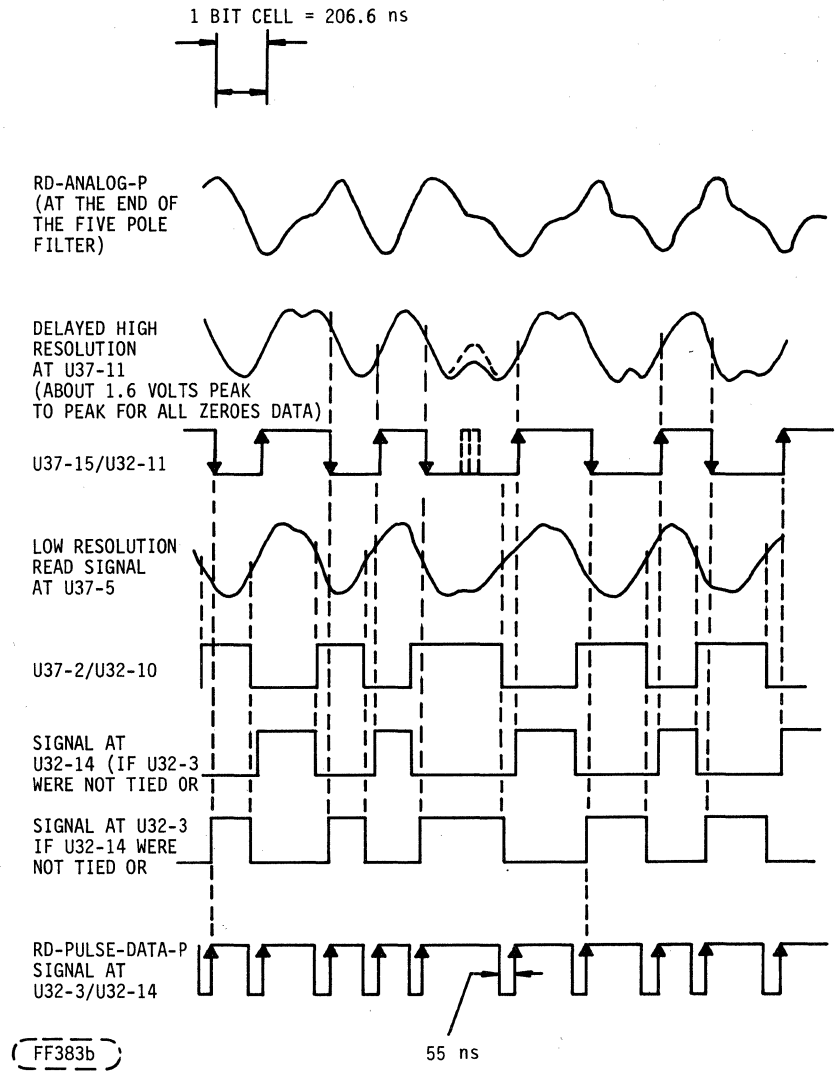


FIGURE 4-34. READ ANALOG TIMING DIAGRAM (CDC INTERFACE)

Figure 4-35 is a block diagram of the Pre-Amp PWA. When the write gate is enabled, the write data is clocked into the write data flip-flop. This converts the data to differential data by the use of both inverted and non-inverted outputs. The write data circuit provides equal current to both polarities of the write data. The data is then sent on to the preamp. The WRITE SELECT/-L signal is a low TTL level signal to enable the write of the head preamp. The write enable circuit controls the following:

1. The write data circuit which was explained above.

2. The write select circuit which puts the preamp in the write mode. When write select is inactive the preamp will be in the read mode.

   The write current level circuit which controls the magnitude of the write current is disabled by the unsafe signal. This circuit sets the minimum current and adds an adjusted current with the aid of the write current control (as explained above). The signal labeled write current sinks current of amplitude almost equal to the write current through one side of the head coils.

The unsafe latch is set by an unsafe signal generated by the head preamp. It disables the write current and sets the unsafe latch. The unsafe latch holds the write select, write current, and write enable circuits disabled until they are reset by the controller or the digital circuits.

4.3.5.3 READ CIRCUITS (SEAGATE INTERFACE)

When the disk drive is not writing, the signal from the Read/Write heads is amplified by the head preamp located at the head flex cable close to the head. By being near the heads the signal to noise ratio is improved. The signal is amplified (39 times nominal) and sent through the flex cable in a differential mode outside the sealed unit.

This signal is received by the pre-amp PWA as RD-DATA-N and RD-DATA-P. The amplitude of this signal is in the millivolt range. A three pole linear phase low pass filter reduces the high frequency noise of the signal. The signal is amplified and processed by a pulse-slimming network. The pulse-slimmer improves the signal resolution and conditions it for signal detection and recovery. The enhanced signal is amplified and applied differentially as RD-ANALOG-N and RD-ANALOG-P to the data PWA.

The read circuitry of the read/write analog PWA (see Figure 4-36) converts the preamplified analog read data to digital MFM data. The data is first attenuated by a FET for gain control. The signal is then amplified and sent through a five pole linear phase filter to improve the signal to noise ratio. The signal is differentiated to convert the signal peaks to zero-crossings by an active differentiator for good common mode rejection.

At this point the data is split into three parallel paths. In the AGC circuit path the signal is peak detected and filtered at this point. The peaks are averaged by a current amplifier and a capacitor. Controlling the attenuator with this voltage gives the circuit automatic gain control. The two remaining data paths are the high resolution and low resolution channels. In the high resolution path no further filtering is added. The signal is buffered and sent through a delay line.

The low resolution path adds a low pass filter to reject high frequency components (mostly third harmonics). This reduces the possibility of extraneous zero-crossing when the data frequency is low. This also induces a phase lag so that the signal now matches the delayed high resolution signal.

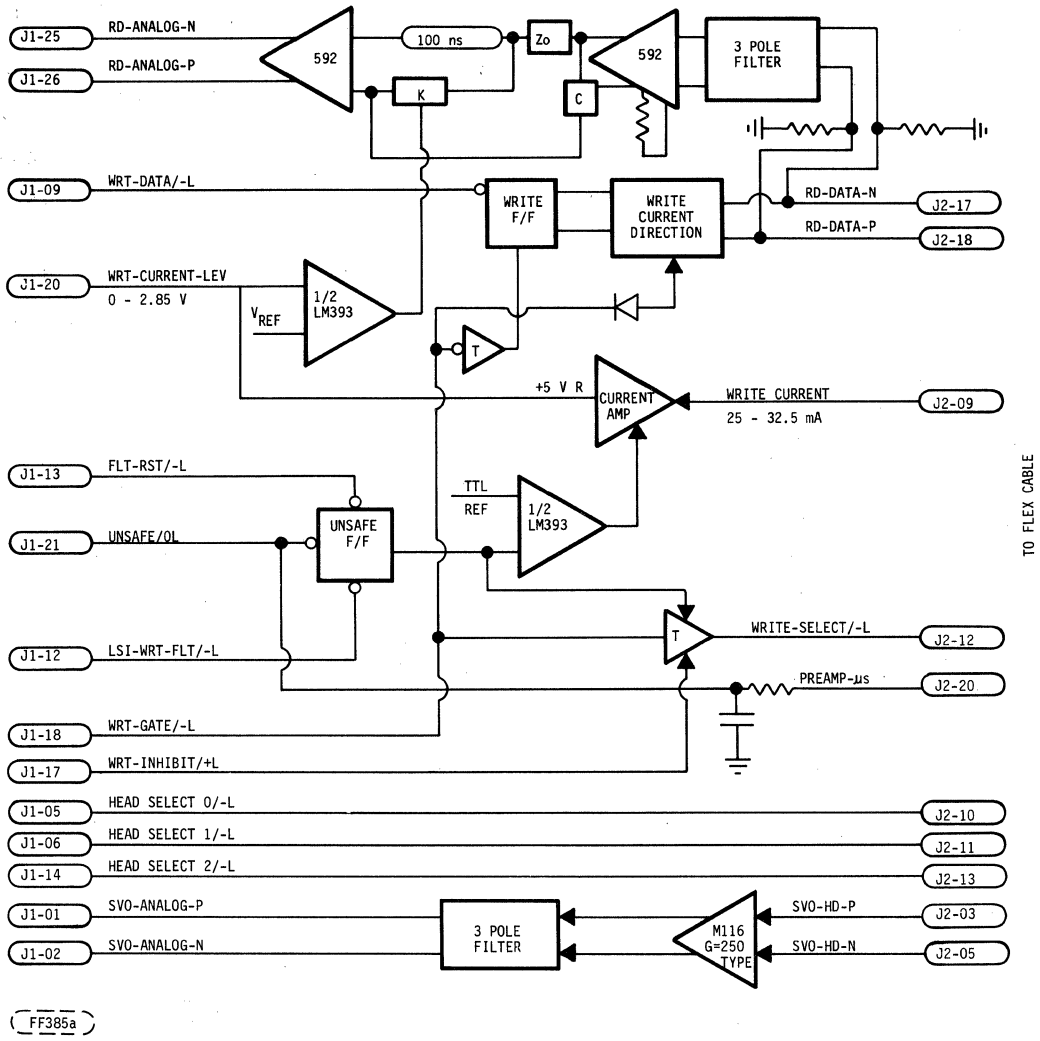


FIGURE 4-35. PRE-AMP BLOCK DIAGRAM (CDC INTERFACE)

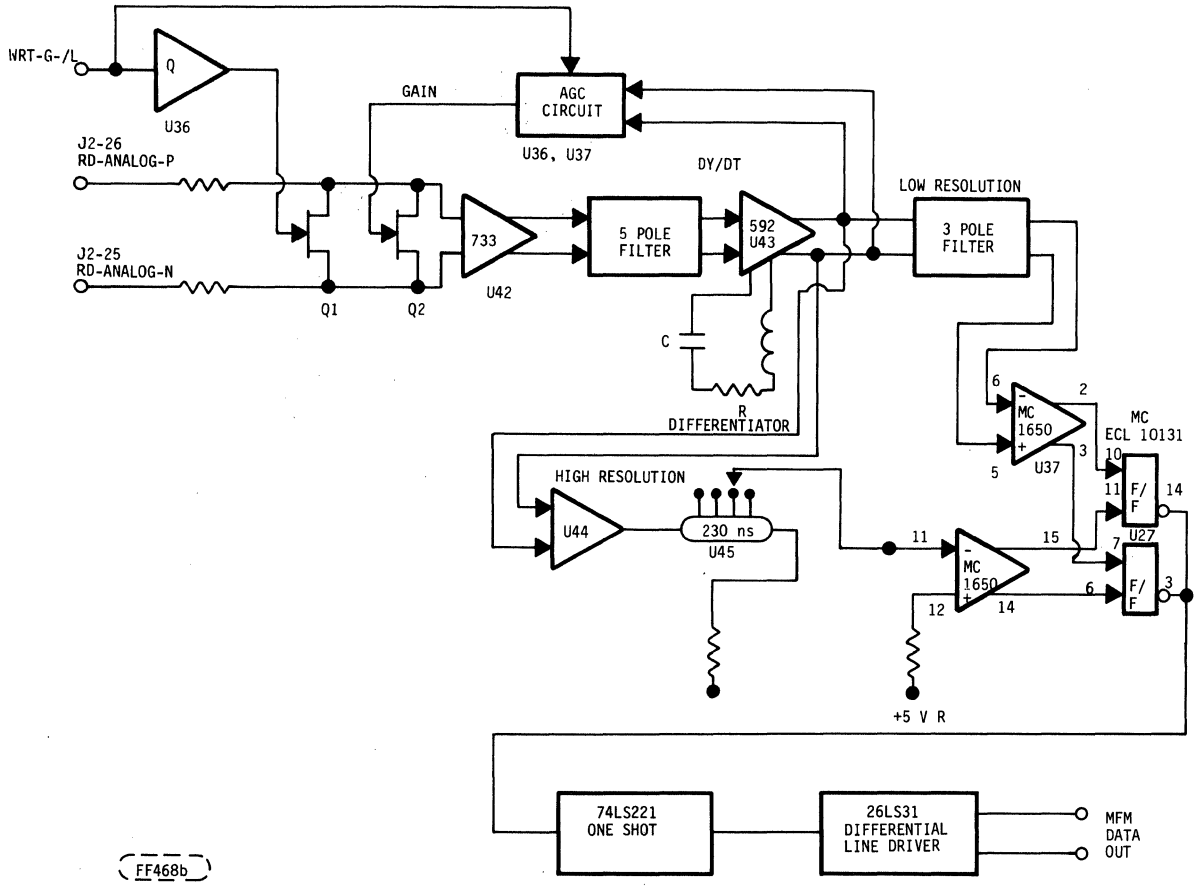


FIGURE 4-36. DATA PWA READ ANALOG FUNCTION (SEAGATE INTERFACE)

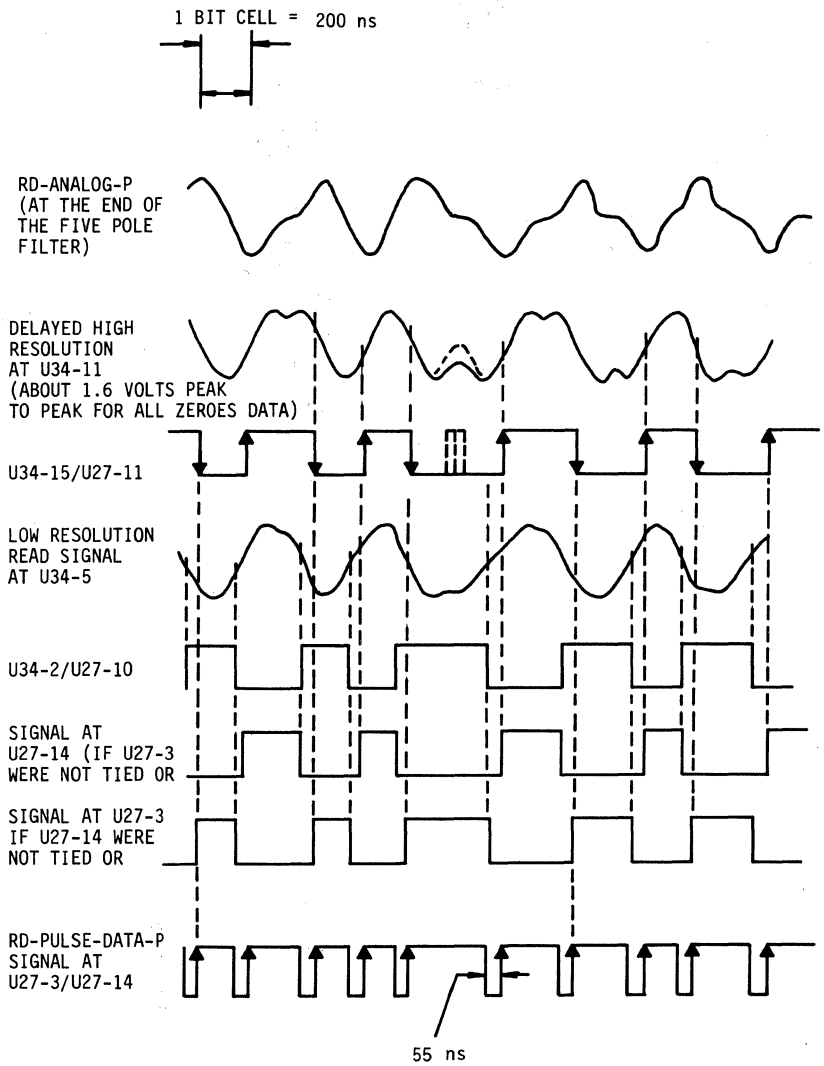


FIGURE 4-37. READ ANALOG TIMING DIAGRAM (SEAGATE INTERFACE)

Both path signals are now converted to digital type signals by sending them through differential comparators. The signals are then sent to a pair of flip-flops which resolve the differences. The high resolution data clocks both flip-flops and the low resolution data enables them. Therefore the low resolution data acts as a qualifier and eliminates false transitions without changing true ones. The outputs of the flip-flops are wire-"OR"ed to produce a pulse for each flux transition. This data is used to trigger a 74LS221 one shot which generates 25 ns pulses. This signal is amplified by a 26LS31 to generate the balanced differential READ signals which are outputted on the interface. The timing diagram (see Figure 4-37), shows the waveform relationships. FET Q2 is turned on during the write mode to clamp the signal and reduce the write to read switch time.

4.3.5.4 HEAD PREAMP CHIP AT THE FLEX CABLE (CDC AND SEAGATE INTERFACES)

The read/write preamp performs the following four functions:

1. The preamp selects the correct head.

2. The preamp diverts the write current to the selected head.

3. The preamp creates an unsafe signal for the following conditions:
   a. Shorted heads.
   b. Open heads.
   c. Write current in the read mode.
   d. No write data in the write mode.

4. The preamp amplifies the read data from the selected head.

The head select encoding is shown in Figure 4-38 and a block diagram of the head preamp in Figure 4-39. NOTE that the disk surfaces are numbered from the bottom up. It should also be noted that the preamp operates on +5 and -5 volts. When the preamp is in the read mode the data is presented on the READ-DATA-N and READ-DATA-P lines. If the WRITE SELECT line is taken to low TTL level the preamp is switched to the write mode. The proper value of write current must then be sinked from the write current (WC) line. If an unsafe condition is present the preamp will bring the unsafe line from TTL high to TTL low. This will cause the digital circuitry to set the fault latch. The preamp will perform read or write operations on the head selected at the time; therefore, the head selection must be made before write is enabled.

INTERFACE LEVEL						
HD-SEL-2 J3-06	HD-SEL-1 J3-04	HD-SEL-0 J3-32	HEAD LOCATION	MEDIA SELECTED	HEAD PREAMP SSI 115	HEAD NUMBER
0	0	0	TOP HEAD	BOTTOM MEDIA	22,23	0
0	0	1	BOTTOM HEAD	MIDDLE MEDIA	20,21	1
0	1	0	TOP HEAD	MIDDLE MEDIA	18,19	2
0	1	1	BOTTOM HEAD	TOP MEDIA	16,17	3
1	0	0	TOP HEAD	TOP MEDIA	14,15	4

NOTE - A "1" corresponds to 0 to 0.4 volts and a "0" to 2.4 to 5.25 volts at the interface.

During read, an invalid head select input code (5, 6 or 7) have the effect of not selecting any heads. An unsafe is produced when writing an invalid head or if there is no data transitions during a write.

FIGURE 4-38. WREN I HEAD-SELECT ENCODING (CDC AND SEAGATE INTERFACES)

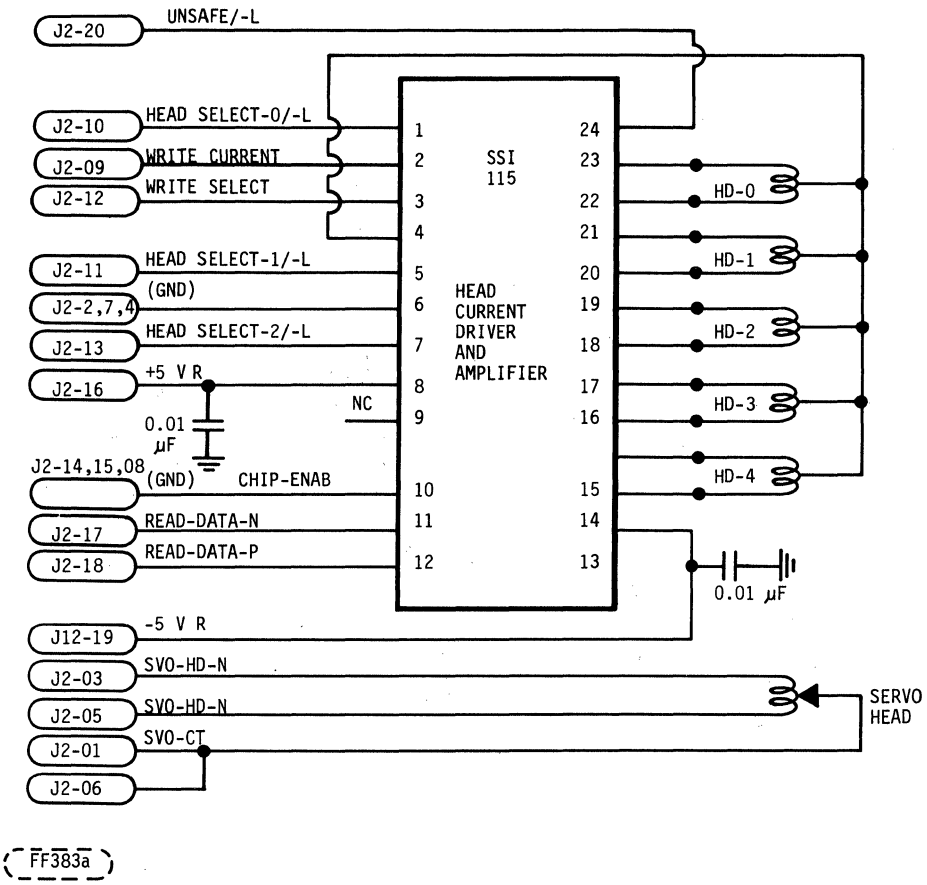
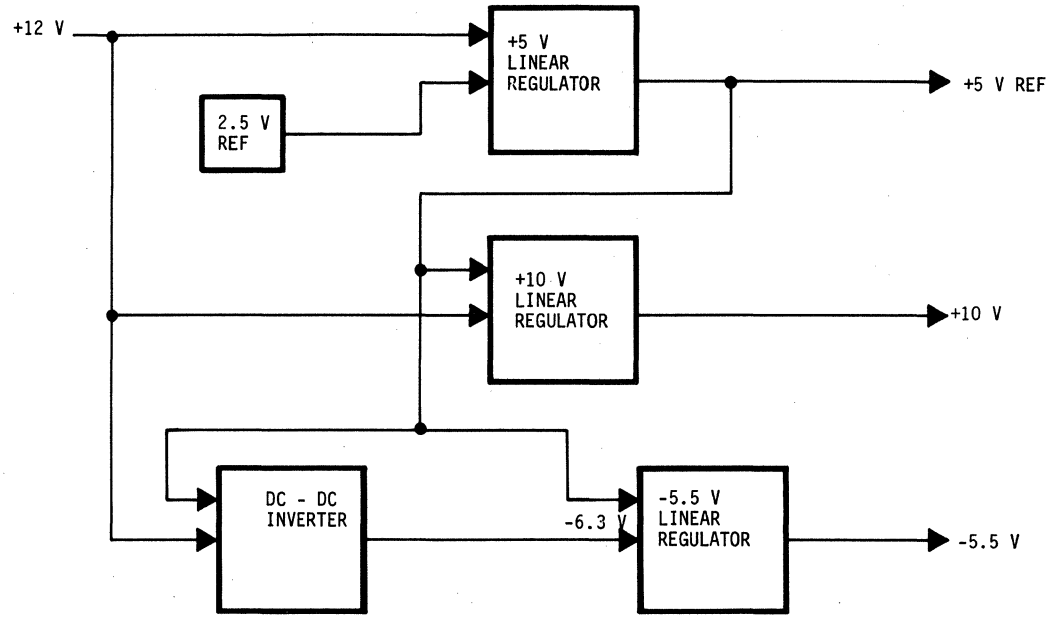


FIGURE 4-39. HEAD PREAMP AND DRIVER (AT THE FLEX CABLE) (CDC AND SEAGATE INTERFACES)

4.3.6. AUXILIARY SYSTEMS (CDC AND SEAGATE INTERFACES)

4.3.6.1 WREN POWER SUPPLY CIRCUITS (CDC AND SEAGATE INTERFACES)

The WREN requires only two external voltages, +12 volts and +5 volts but some circuits in the WREN require a negative voltage. This negative voltage is provided by a DC-DC converter circuit. In addition to this converter, voltage regulators provide +10 volts and +5 volts for critical read/write and servo circuits. Figure 4-40 is a block diagram of the power supply circuits internal to the WREN.



FF380b

FIGURE 4-40. WREN I POWER SUPPLY CIRCUITS (CDC AND SEAGATE INTERFACES)

Figure 4-41 shows the schematic of the DC-DC converter and linear regulator. Two comparators (LM393) control the operation of the switcher. If the output voltage at point C is too low then the bottom comparator will turn off and allow the switch transistor (3762) to apply +12 volts to point A of the 100 uH coil. This causes the current through the coil to increase linearly. This current is sensed by a 0.51 ohm resistor and when the current reaches $\approx$ 1 amp the upper comparator will turn on which turns off the switch transistor. The voltage at point A will then go negative until the catch diode (1N5818) turns on. This clamps the voltage across the inductor to $\approx$ 6.7 volts and the current in the inductor decreases linearly to zero. This current charges the 39 µF output capacitor which increases the output voltage. This increase in output voltage causes the lower comparator to switch on which will inhibit the switch transistor from turning on. The load current will discharge the 39 µF capacitor until the lower comparator switches states and starts the cycle over. Figure 4-35 gives typical waveforms for a load current of 200 mA. The output of C is well regulated but has high ripple (ie $\approx$ 200 mV). This voltage is then regulated by a linear regulator to remove ripple and decrease output impedance. The output of the linear regulator is -5.525 volts. This output is referenced to the +5 V R voltage and is sensed by an op-amp (LM324) which drives a NPN pass transistor (MPQ2222) via a PNP current source (MPQ3762). The use of a NPN pass transistor allows the regulator to function to very low voltage across the pass transistor (typically $\approx$ 0.3 volts).

+5 VOLT AND +10 VOLT REGULATORS

Figure 4-43 is a schematic of the +5 volt and +10 volt regulators. The +5 volt regulator is a conventional series pass design referenced to a 2.5 volt reference (MC 1403). The output (+5 V R) is used as the reference for all other regulators. The 10 volt regulator is similar to the -5.525 volt design except the transistors are of opposite polarity (ie NPN vs PNP). This allows the regulator to keep a 10 volt output even if the +12 volt input reduces to $\approx$ 0.4 volt. Two pass transistors are used with current balancing resistors (4.7 ohm) to insure adequate power dissipation.

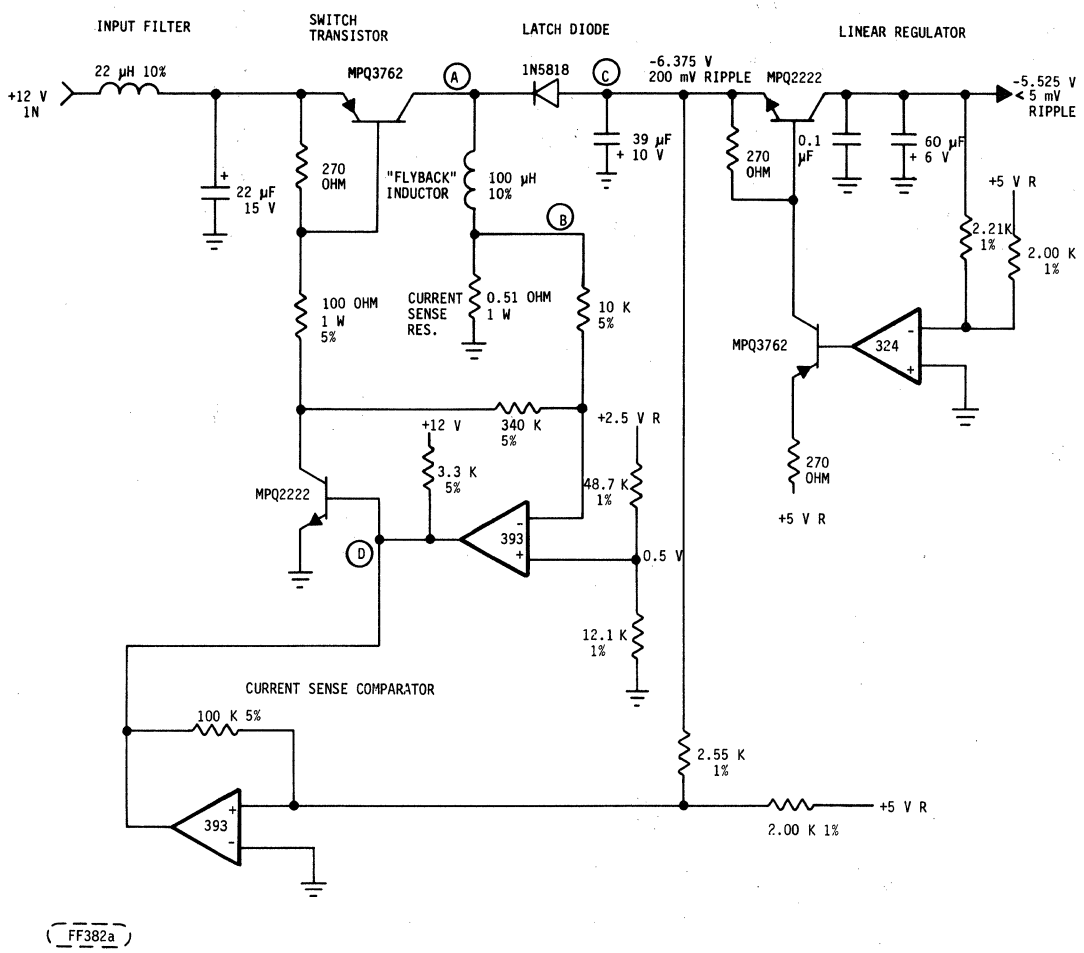


FIGURE 4-41. WREN I DC-DC CONVERTER (CDC AND SEAGATE INTERFACES)

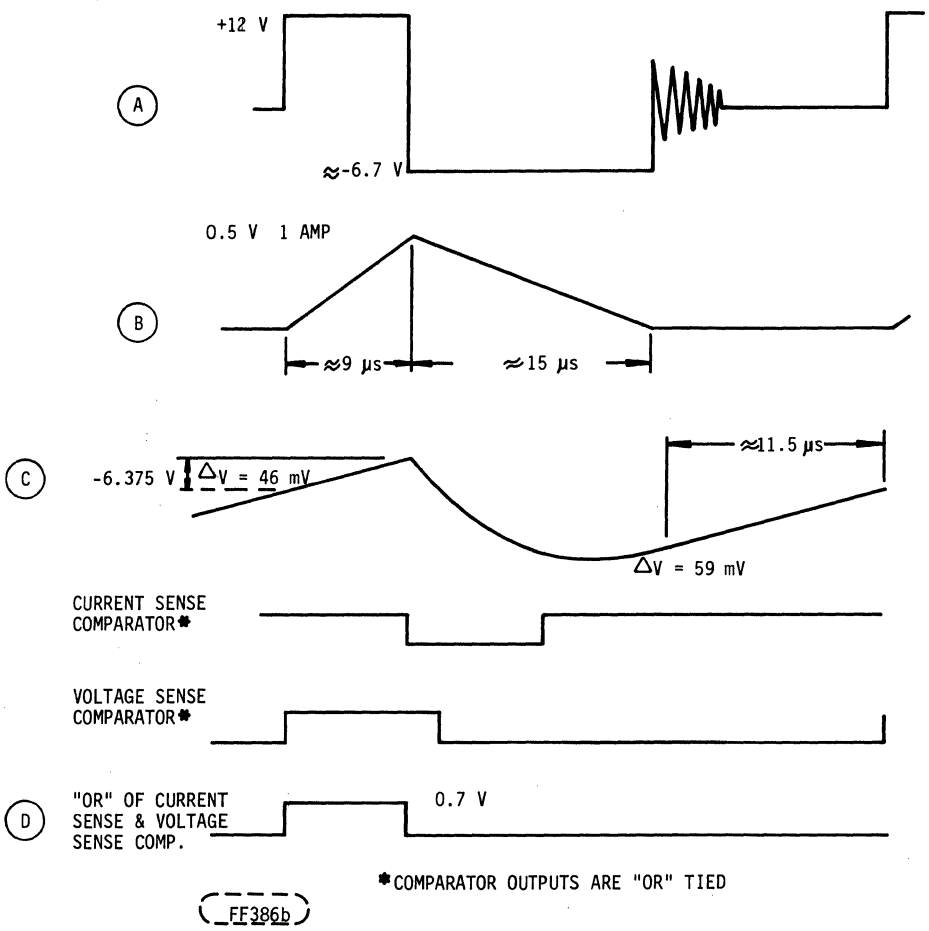


FIGURE 4-42. DC-DC CONVERTER WAVEFORMS (CDC AND SEAGATE INTERFACES)

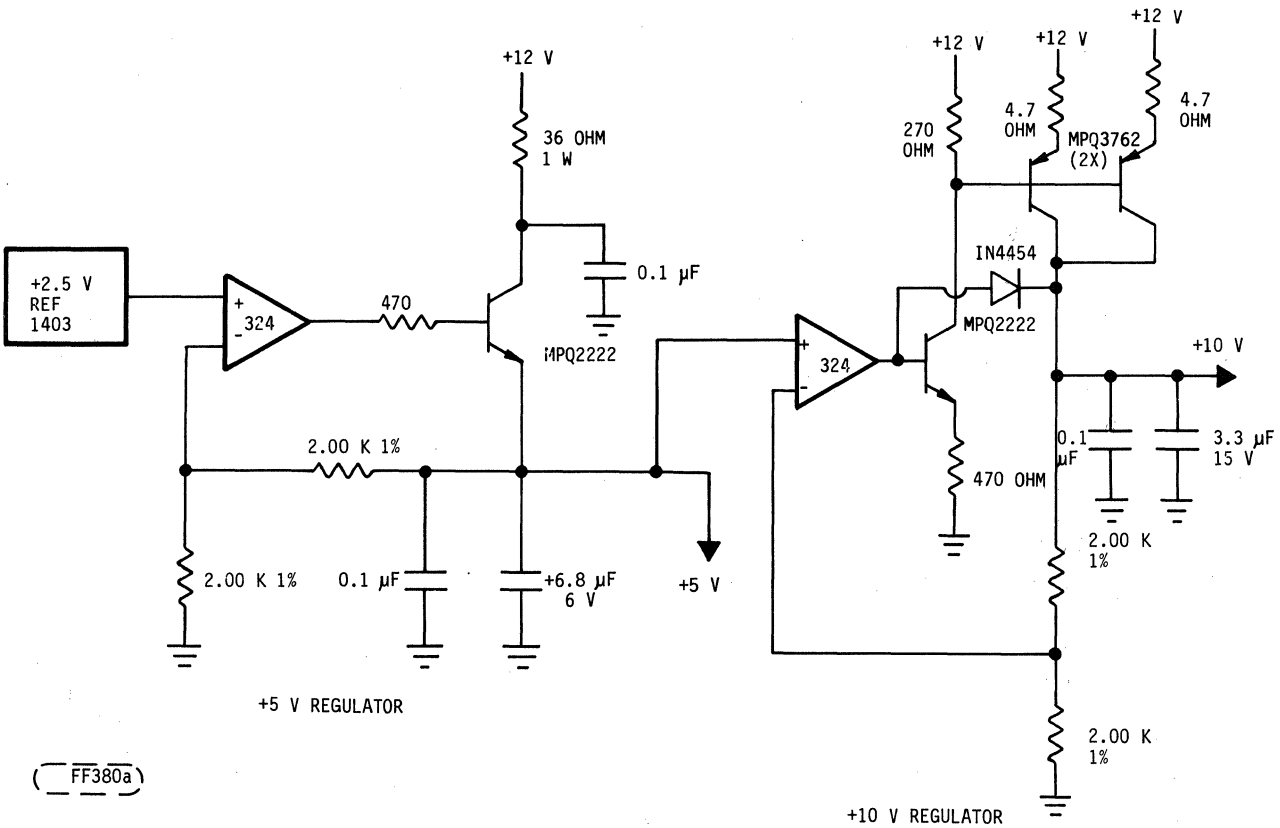


FIGURE 4-43. +5 AND +10 VOLT REGULATORS (CDC AND SEAGATE INTERFACES)

4.3.6.2 VOLTAGE MONITORING (CDC AND SEAGATE INTERFACES)

The WREN I monitors the internal and external power supplies. This is done to assure data on the disk is not destroyed when power is shut off or interrupted. The circuits for doing this are on the SERVO-PWA. These circuits monitor the +5 and +12 volt external sources and the +10 and -5.5 volt supplies internal to the drive. These circuits also provide a delay of approximately 0.3 seconds after the +5 volt supply is turned on to allow the logic and microprocessor to be reset.

The outputs of the voltage monitoring circuits are used to directly inhibit any write current and to signal the microprocessor of voltage loss.

4.3.6.3 SPINDLE MOTOR CONTROL (CDC AND SEAGATE INTERFACES)

A two phase brushless DC motorized spindle is driven by a current controlled power amplifier and commutation is regulated once per phase by a sensor device inside the spindle motor. The motor current is set by the amplitude of a filtered pulse width modulated signal generated by the speed control circuits located in the servo-motor control LSI. (See Figure 4-44.)

The motor control logic in the servo LSI chip uses the clock signal derived from the microprocessor clock as a reference to determine the motor speed error. The servo LSI generates an output width proportional to the amount that the motor speed is under the desired speed. The duty cycle of this signal is divided into 8 steps between 0% (minimum error) and 100% (maximum error). The 100% duty cycle is used while starting.

The back EMF derived from the stored energy in the disks and spindle is used to hold the actuator solenoid in an unlocked position while moving the head actuator into the landing zone after external power is removed.

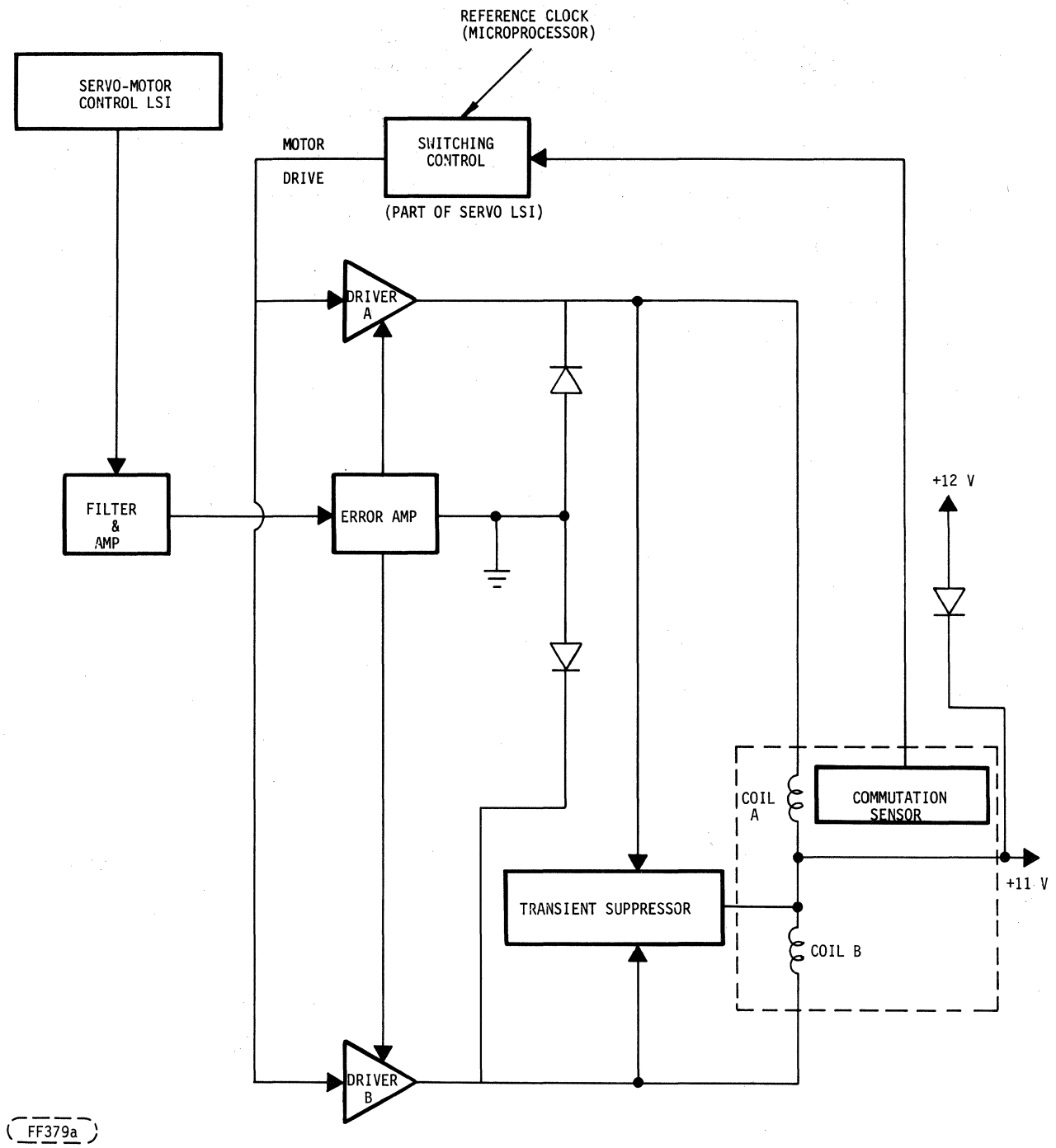


FIGURE 4-44. MOTORIZED SPINDLE DRIVE
(CDC AND SEAGATE INTERFACE)

5.1 INTRODUCTION

Most of the electronic functions of the WREN are included in three PWAs which are external to the sealed enclosure and one PWA (Flex Circuit) which is internal to the sealed enclosure. A block diagram of the function included in each board is as shown in Figure 5-1. Interface diagrams are shown in Figures 5-2A and 5-2B.

5.2 SCHEMATIC/PWA ORDERING

Schematic Diagrams and/or Printed Wire Assembly layouts can be ordered by contacting the CDC OEM Sales Office. Information needed will be the part number and the serial number from the label (Figure 5-3) located on the back of the cover. The Printed Wire Assembly number will also be needed. This number is stamped on the PWA (example shown in Figure 5-4).

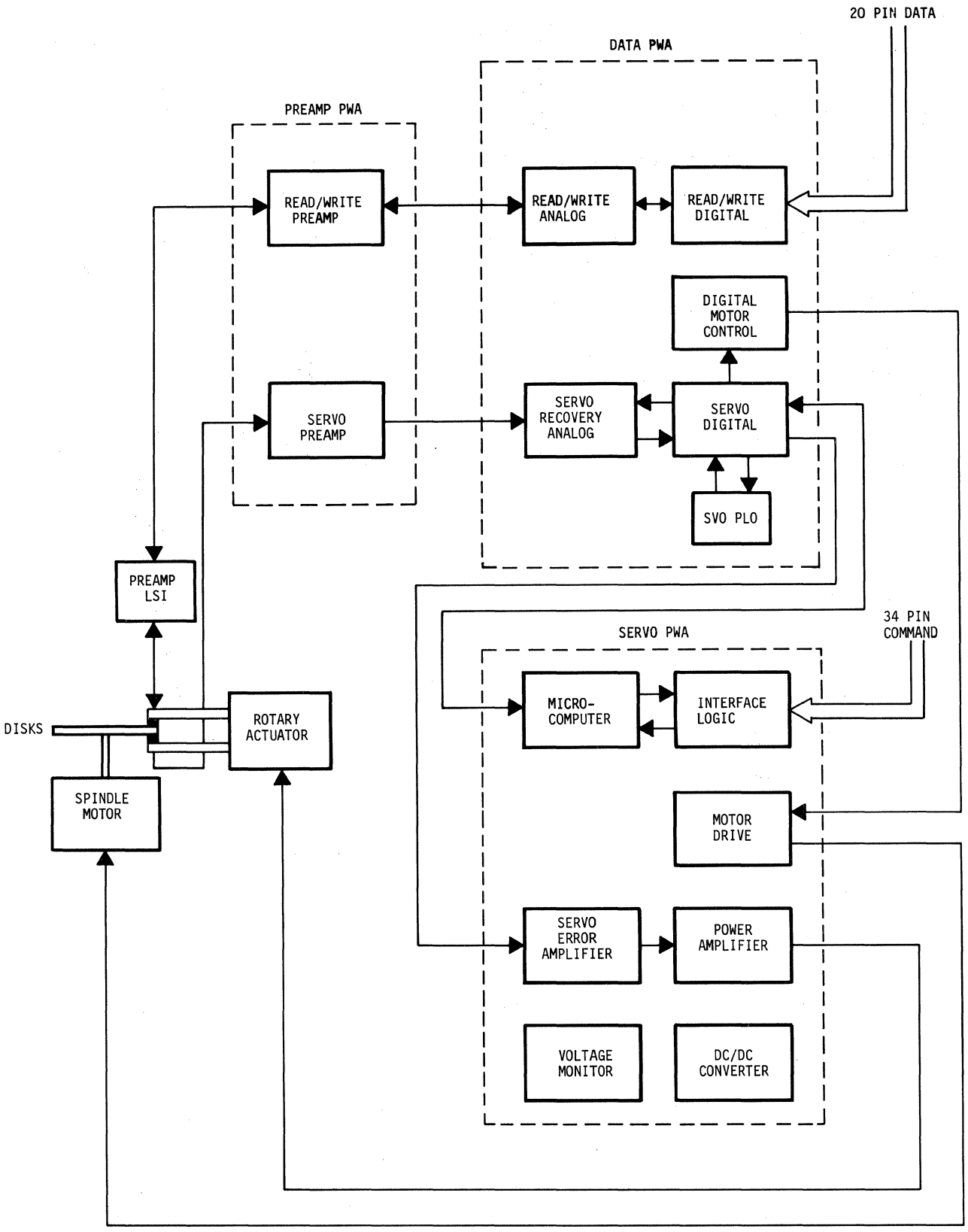
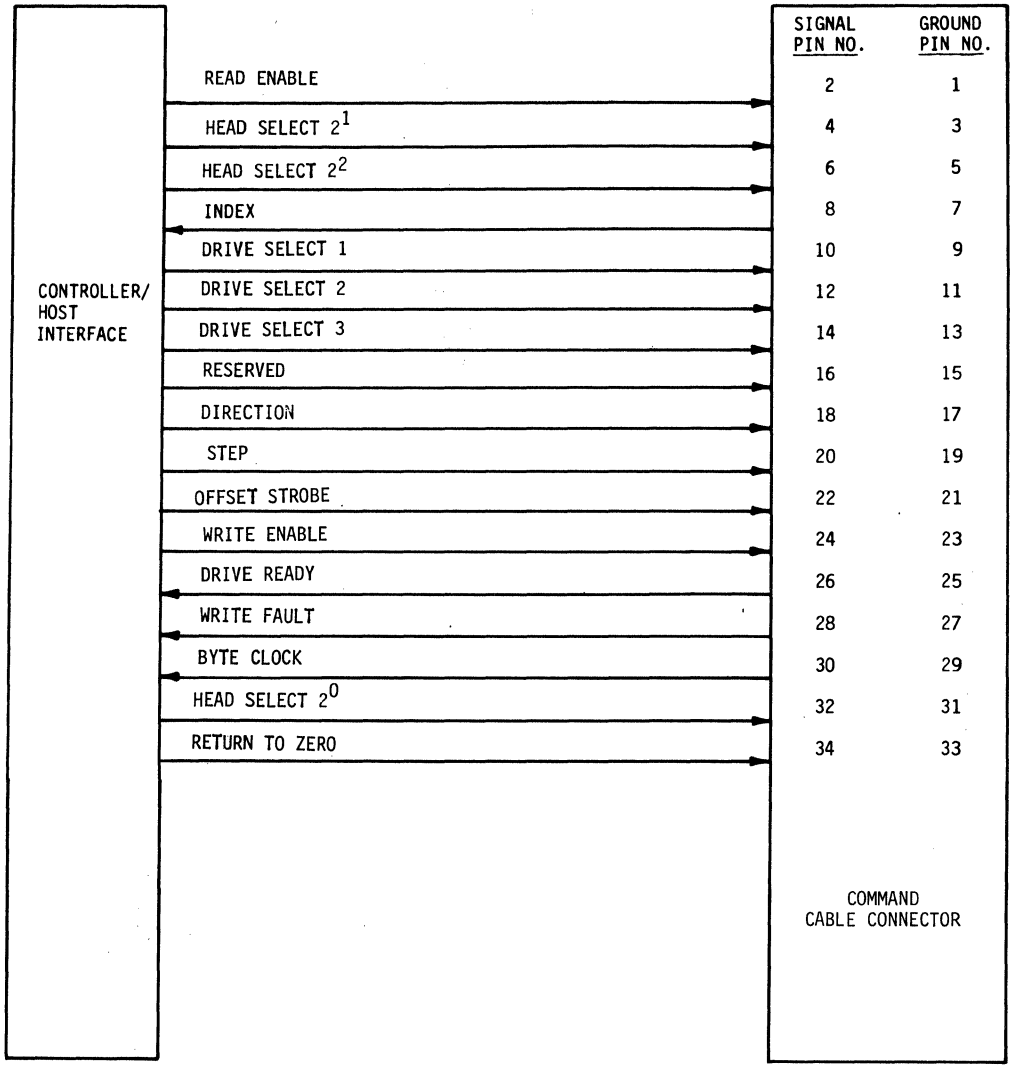


FIGURE 5-1. WREN I BLOCK DIAGRAM



NOTE: ALL RESERVED SIGNALS TO THE WREN DRIVE SHALL BE TERMINATED IN THE WREN.
ALL SIGNALS IN THE COMMAND CABLE ARE SINGLE-ENDED SIGNALS.

GG275a

FIGURE 5-2A. COMMAND CABLE INTERFACE FOR UNITS WITH CDC INTERFACE

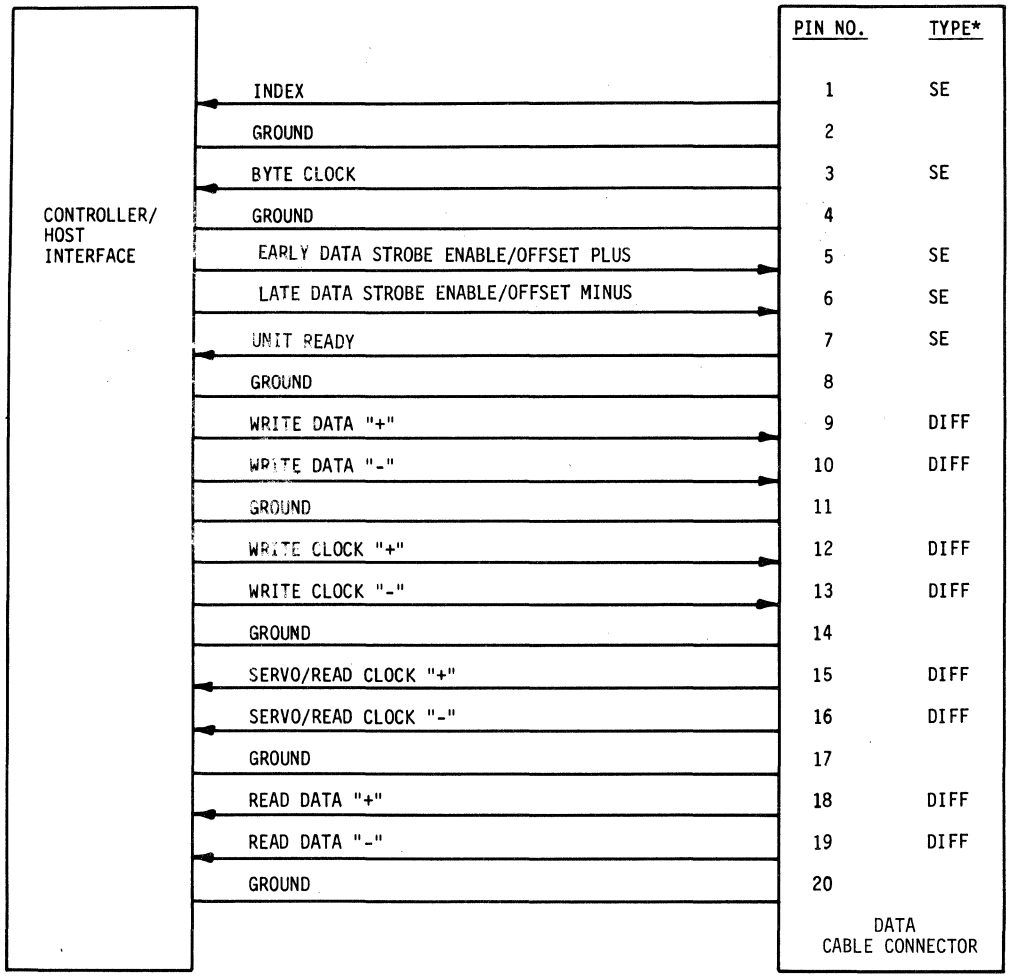
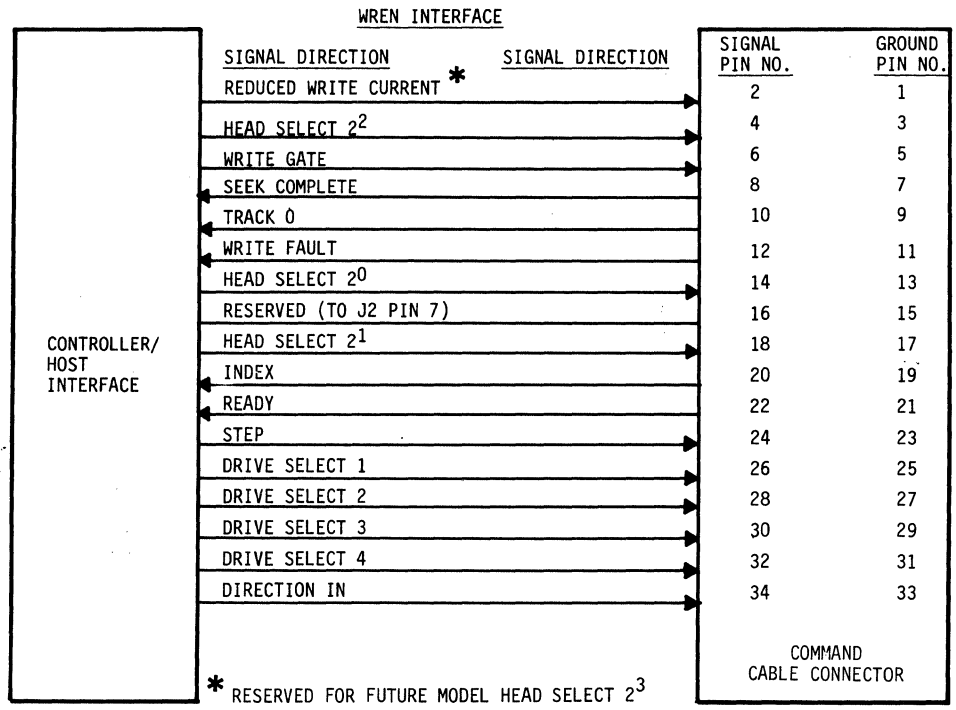


FIGURE 5-2A. DATA CABLE INTERFACE FOR UNITS WITH CDC INTERFACE



NOTE: ALL SIGNALS IN THE COMMAND CABLE ARE SINGLE ENDED SIGNALS.

FF143a

FIGURE 5-2B. COMMAND CABLE INTERFACE FOR UNITS WITH ST506 INTERFACE

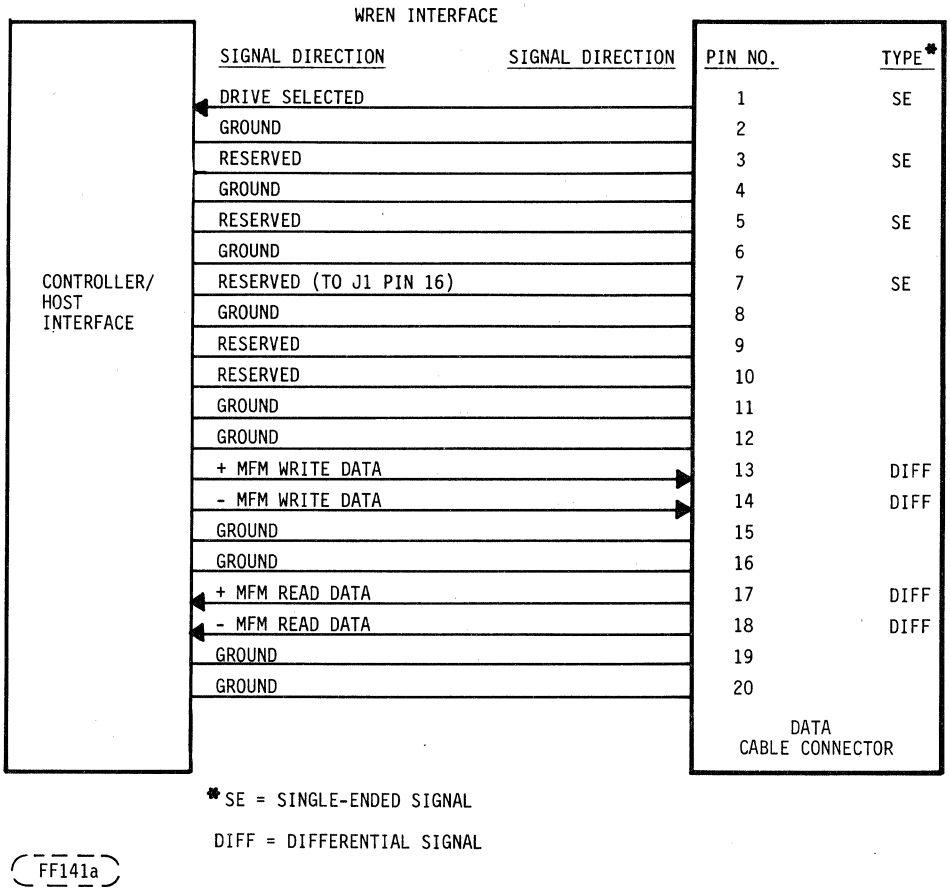


FIGURE 5-2B. DATA CABLE INTERFACE FOR UNITS WITH ST506 INTERFACE

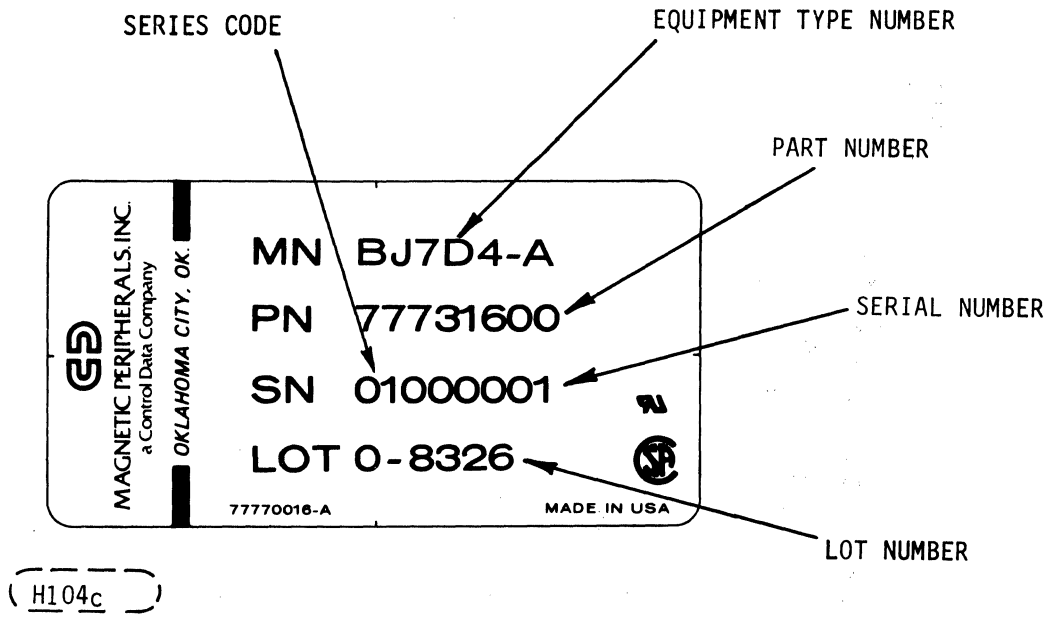


FIGURE 5-3. SAMPLE WREN I LABEL

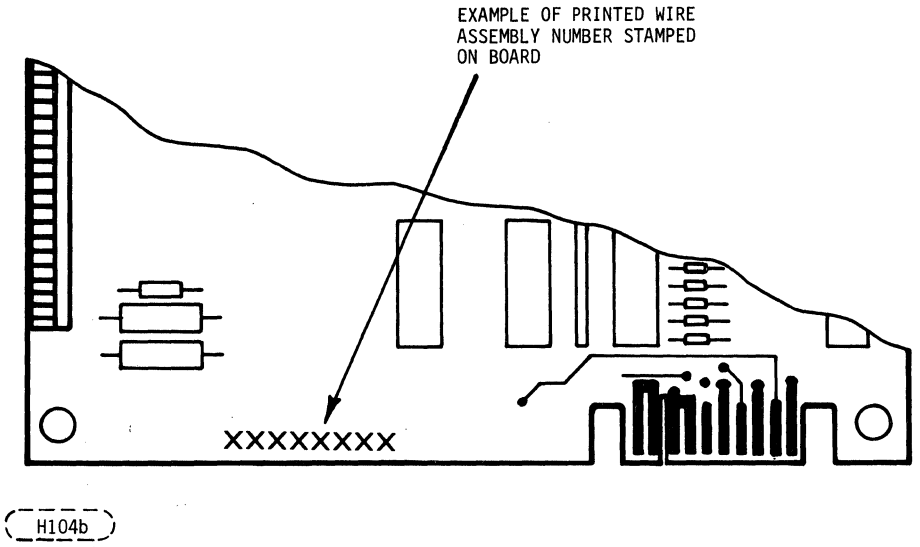


FIGURE 5-4. PWA NUMBER

6.1 INTRODUCTION

This section contains the instructions required to maintain the CDC Model 9415 WREN I Disk Drive. The information presented is provided for corrective maintenance as no preventative maintenance is required. All maintenance should be performed by qualified and trained service personnel.

The maintenance procedures detailed below should be performed only after power to the WREN drive has been turned off, the shipping lock engaged, the DC power, interface, and data-signal cable connectors removed. The drive should then be placed with the chassis on a sponge rubber or foam mat on a flat surface.

The maintenance procedures provided in this section assume that the proper test equipment is available to troubleshoot and replace selected malfunctioning parts. Parts replacement is performed OUTSIDE THE SEALED AREA OF THE DRIVE, ONLY. ENCROACHMENT OF THE SEALED AREA VOIDS THE UNIT WARRANTY.

6.2 SAFETY AND SPECIAL MAINTENANCE PRECAUTIONS

- Avoid overtightening hardware (screws, nuts, etc.) when replacing assemblies and components. All screws and nuts are of the low carbon variety.

- Do not connect or disconnect cables without first removing all power from the drive.

CAUTION

The circuit assemblies contained in this equipment can be degraded or destroyed by ELECTROSTATIC DISCHARGE (ESD).

Static electrical charges can accumulate quickly on personnel, clothing, and synthetic materials. When brought in close proximity to or, in contact with delicate components, ELECTROSTATIC DISCHARGE OR FIELDS can cause damage to these parts. This damage may result in degraded reliability or immediate failure of the affected component or assembly.

CAUTION (contd.)

To insure optimum/reliable equipment operation, it is required that technical support personnel discharge themselves by periodically touching the chassis ground prior to and during the handling of ESD susceptable assemblies. This procedure is very important when handling Printed Circuit Boards.

Printed Circuit Boards should be handled or transported in electrically conductive plastic bags to insure optimum protection against potential ESD damage.

6.3 MAINTENANCE TOOLS

Additional tools other than those normally used by computer and data processing service personnel are required. These tools (Table 6-1) are used to maintain that part of the Model 9415 WREN I Disk Drive external to the sealed area.

TABLE 6-1. SPECIAL TOOLS

SPECIAL TOOLS	APPLICATION
TORX TX-15 TORX TX-09	6-32 SIX SPLINE SOCKET DRIVE MACHINE 4-40 SCREWS

6.4 MAINTENANCE PROCEDURES

The WREN is designed to require no preventive maintenance at the user site. The procedures outside the sealed area can be performed in an office or other reasonably clean environment. No special testing is required to confirm repairs other than the test that is used to isolate the fault.

6.5 REMOVAL AND REPLACEMENT PROCEDURES OUTSIDE SEALED AREA

Table 6-2 lists the removal and replacement procedures provided in this section. The procedures are for the removal and replacement of recommended spare assemblies and components for the WREN.

TABLE 6-2. LIST OF REMOVAL AND REPLACEMENT PROCEDURES OUTSIDE SEALED AREA

PARAGRAPH NO.	REMOVAL AND REPLACEMENT PROCEDURE
6.5.1	LED/Mount
6.5.2	PWA, R/W Preamp
6.5.3	PWA, Servo
6.5.4	PWA, Data
6.5.5	Ground Spring
6.5.6	Brake Mechanism

6.5.1 LED/MOUNT REMOVAL AND REPLACEMENT

CAUTION

Be sure to support the drive so it does not fall on to the PWA boards during replacement of PWA.

1. Remove power from WREN Disk Drive.
2. Engage shipping lock.
3. Disconnect DC power, interface, and data cables.
4. Place the WREN on a sponge rubber or foam pad on a flat surface with the chassis down.
5. Remove front panel by removing the two mounting screws.
6. Remove the section of the LED mount by prying it up with a small flat blade screwdriver.
7. Slide the LED out the front of the front panel.
8. Replace the LED by reversing the procedure.

NOTE

The shorter lead of the LED is nearest to the outside edge of the front panel.

6.5.2 R/W PREAMP PWA REMOVAL AND REPLACEMENT

1. Follow instructions 1-5 in paragraph 6.5.1 describing LED/MOUNT removal and replacement.
2. Remove mounting screw in middle of the R/W Preamp.
3. Carefully pull the R/W Preamp away from the drive. This disengages the connection from the R/W Preamp to the Preamp Flex Circuit.
4. Disconnect the cable coupling the R/W Preamp and the Data PWA at the Data PWA.

The R/W Preamp is installed by reversing these instructions. When tightening the screw that holds the PWA in place be sure that the two black wires which run under the top cover in that area are not pinched between the flex cable connector and the base deck.

6.5.3 SERVO PWA REMOVAL AND REPLACEMENT

1. Follow instructions 1-4 in paragraph 6.5.2 describing R/W Preamp PWA removal and replacement.
2. Loosen but do not remove the two chassis mounting screws nearest the square end of the cover.
3. Remove the two chassis mounting screws from the rounded end of the cover.
4. Lift the sealed area of the drive carefully and disconnect the connectors of the four cables coming from the sealed area.
5. Continue supporting sealed area while removing the two remaining chassis mounting screws (these were loosened in instruction number 2).
6. Place the sealed area on its cover (upside down) on the sponge rubber or foam pad.
7. Remove the 4 screws holding the PWA assembly. Two are located on the bottom and two on the side of the chassis.
8. Remove the 4 screws holding the PWA assembly together.
9. Separate the two PWA boards, being careful not to lose the four spacers

The Servo PWA is installed by reversing these instructions.

6.5.4 DATA PWA REMOVAL AND REPLACEMENT

1. Follow instructions 1-9 in paragraph 6.5.3 describing Servo PWA removal and replacement.
2. Remove the four spacers, being careful not to lose them.

The Data PWA is installed by reversing these instructions.

6.5.5 GROUND SPRING REMOVAL AND REPLACEMENT

1. Follow instructions 1-6 in paragraph 6.5.3 describing Servo PWA removal and replacement.
2. Remove the two screws holding the ground spring down.
3. Remove ground spring.

Install ground spring by reversing the instructions.

NOTE

Center the ground spring over the center of the motor as much as possible.

6.5.6 BRAKE MECHANISM REMOVAL AND REPLACEMENT

1. Follow instruction 1-6 in paragraph 6.5.3 describing Servo PWA removal and replacement.
2. Remove screw and washer in the center of the brake.

Replacement of Brake Mechanism.

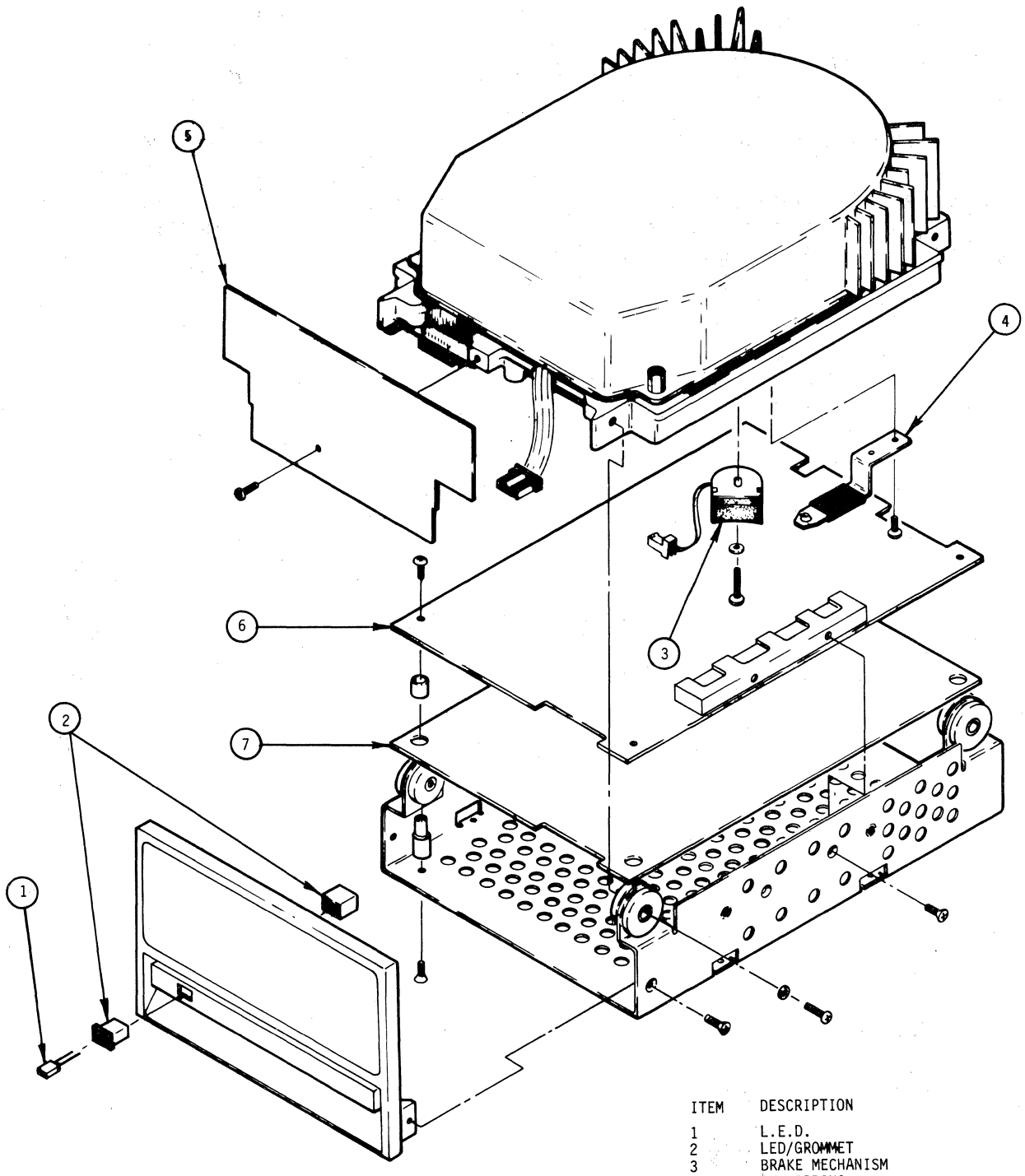
3. Install brake with hinged side away from the ground spring.
4. Install screw and bellville washer, but do not tighten at this time.
5. Insert 0.010 inch shim between brake and motor.
6. Push brake into the motor and tighten screw.
7. Remove shim.
8. Hold brake shoe against brake mechanism and rotate motor counter clockwise. This is a check to make sure brake doesn't hinder operation.
9. Reverse operations in instruction number 1 to finish replacement.

7.1 INTRODUCTION

The recommended spare parts for the WREN external to the sealed area are shown and listed in Figure 7-1. No preventive maintenance is required. Special tools and procedures required to remove and replace these spare parts are listed in Section 6.

> CAUTION
>
> NEVER remove the cover of the WREN. Servicing items in the upper sealed environmental enclosure (heads, media, actuator, etc.) requires special facilities. Encroachment of the sealed enclosure voids the unit warranty. Only the printed-circuit boards, solenoid brake mechanism, LED/grommet and ground spring external to the sealed area can be replaced without special facilities.

When ordering replacement parts for the WREN, describe the part and include the part number and serial number from the label (Fig. 5-3) located on the back of the unit.



ITEM	DESCRIPTION
1	L.E.D.
2	LED/GROMMET
3	BRAKE MECHANISM
4	GND SPRING
5	R/W PREAMP PWA
6	SERVO PWA
7	DATA PWA

FF390a

FIGURE 7-1. WREN I RECOMMENDED SPARES

USER COMMENTS

FILE REFERENCE

FROM:

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Name _____

Address _____

City _____

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Area Code _____ Phone _____

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