PRODUCT SPECIFICATION
FOR
MODEL 9415-3
WREN DISK DRIVE

WrenI - 5
9415 -36   -5 interface = ST506
5 heads   697 trk   36.29MB uniform.

Applications   405-324-3061
Tech Support   405-324-3007

CONTROL DATA CORPORATION

PRODUCT SPECIFICATION
FOR
MODEL 9415-3
WREN DISK DRIVE

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1.0   SCOPE

This specification describes the Control Data Corporation Model 9415-3 WREN Disk Drive. This 5 1/4-inch member of the rigid disk family utilizes a digital interface and is available in 21 and 35 megabyte unformatted capacities. The basic model configurations are 9415-3-21 and 9415-3-35.
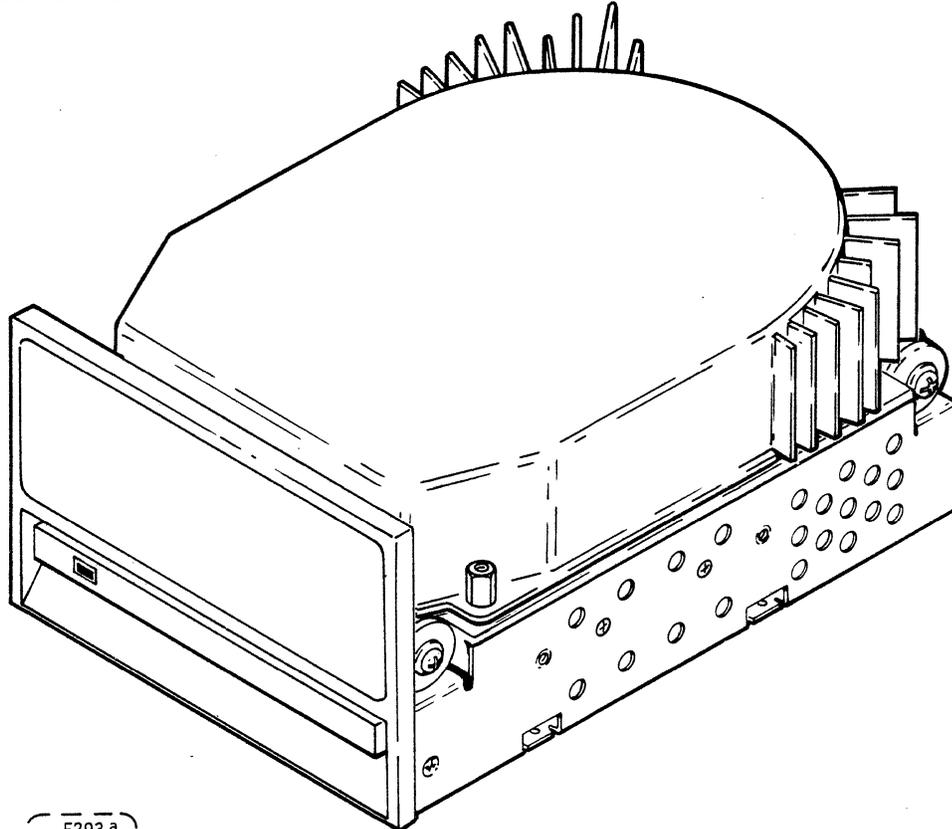
FIGURE 1. THE 9415-3 WREN

2.0   APPLICABLE DOCUMENTS

2.1   STANDARDS

The 9415-3 WREN has been developed as a system peripheral to the highest standards of design and construction. The drive, however, must depend upon its host equipment to receive adequate power and environment in order to provide optimum performance and compliance with applicable industry and governmental regulations. Special attention must be given in the areas of safety, power distribution, shielding, audible noise control, and temperature regulation of the device to ensure specified performance and compliance with all applicable regulations.

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2.1   -Continued

The 9415-3 WREN shall comply with CDC standards as noted in the appropriate sections of this specification.

In addition to the CDC standards, the 9415-3 WREN shall be recognized by UL as a component under UL 478 and be certified by CSA as a component under CSA Standard C22.2 No. 154-1975 and meet the requirements of DIN IEC 380/VDE 0806/8.81.

The 9415-3 WREN, as delivered, is designed for system integration prior to utilization. As such, the 9415-3 WREN is supplied as a component and is not subject to standards imposed by FCC Rules and Regulations, Part 15, Subpart J governing EMI of computing devices. However, the 9415-3 WREN tested as delivered, does comply with Class A of the referenced FCC regulations.

2.2   DOCUMENTATION

The following documentation is available for field support of the 9415-3 WREN.

77715950   OEM Manual
77715975   Hardware Maintenance Manual
77715840   Application Note Using the FDI Adapter

3.0   GENERAL DESCRIPTION

The 9415-3 WREN is a member of a family of low-cost, high-performance, highly reliable, random access storage devices designed to meet the needs of the OEM marketplace.

The 9415-3 WREN is designed to record and recover data on up to three 5 1/4-inch (130 mm) fixed disk; it does not contain removable media capability.

The 9415-3 WREN digital interface is intended to utilize a single controller design capable of controlling both the 9415-3 WREN and the 5 1/4-inch 9409 Flexible Disk Drive (FDD).

The 9415-3 WREN Interface consists of a 34-pin command interface cable and a 20-pin data interface cable. The 34-pin command interface is designed to allow daisychained or radial connections to 9415-3 WREN and 9409 FDDs.

3.0   -Continued

Thus, the 34-pin 9415-3 command interface cable contains functionally and electrically compatible signals to a 9409; however, due to different step rates, access time, and data transfer rates, the timing relationships of the individual signals may vary. The 20-pin radial data interface cable is unique to the 9415-3 and is based on differential NRZ data plus clocks to meet electrical requirements for a 4.84 MHz data rate.

The 9415-3 WREN interface is also designed to be easily adapted to the 9410-3 FINCH interface via an In-Line passive cable adapter which is available from CDC as an accessory.

The Head, Disk and Actuator chamber (HDA) is environmentally sealed. Air is recirculated within the disk/actuator chamber and passes through an absolute filter to ensure the maintenance of a contamination-free disk/actuator environment.

Refer to Figure 2 for an exploded view of the 9415-3. NEVER disassemble the WREN HDA. This exploded view is for information only. Servicing items in the upper sealed environmental enclosure (heads, media, actuator, etc.) requires special facilities. Only the printed circuit boards external to the sealed area may be replaced without special facilities. Any disassembly of this type should be in accordance with the Hardware Maintenance Manual.

The 9415-3 WREN utilizes a dedicated landing zone at the innermost radius of the media thus eliminating the possibility of destroying or degrading data by not landing in the data zone.

The 9415-3 WREN includes a mechanical shipping lock (40 g's) (Figure 2) that eliminates actuator movement during shipment or handling. An automatic carriage restraint (25 g's) minimizes actuator movement when the device is powered down.

The 9415-3 WREN performs an auto velocity adjust after power up before loading the heads on Track 0. This design feature eliminates the calibration requirement normally attributed to velocity adjustment.

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TOP COVER

SPINDLE/DISK
ASSEMBLY

ACTUATOR
ASSEMBLY

AUTOMATIC
ACTUATOR ARM
RESTRAINT

MECHANICAL
BRAKE

BASE
CASTING

MECHANICAL
SHIPPING LOCK

CHASSIS

HEAT SINK

FF031

PREAMP
PWA

SERVO
PWA

DATA
PWA

SHOCK MOUNTS
(4 places)
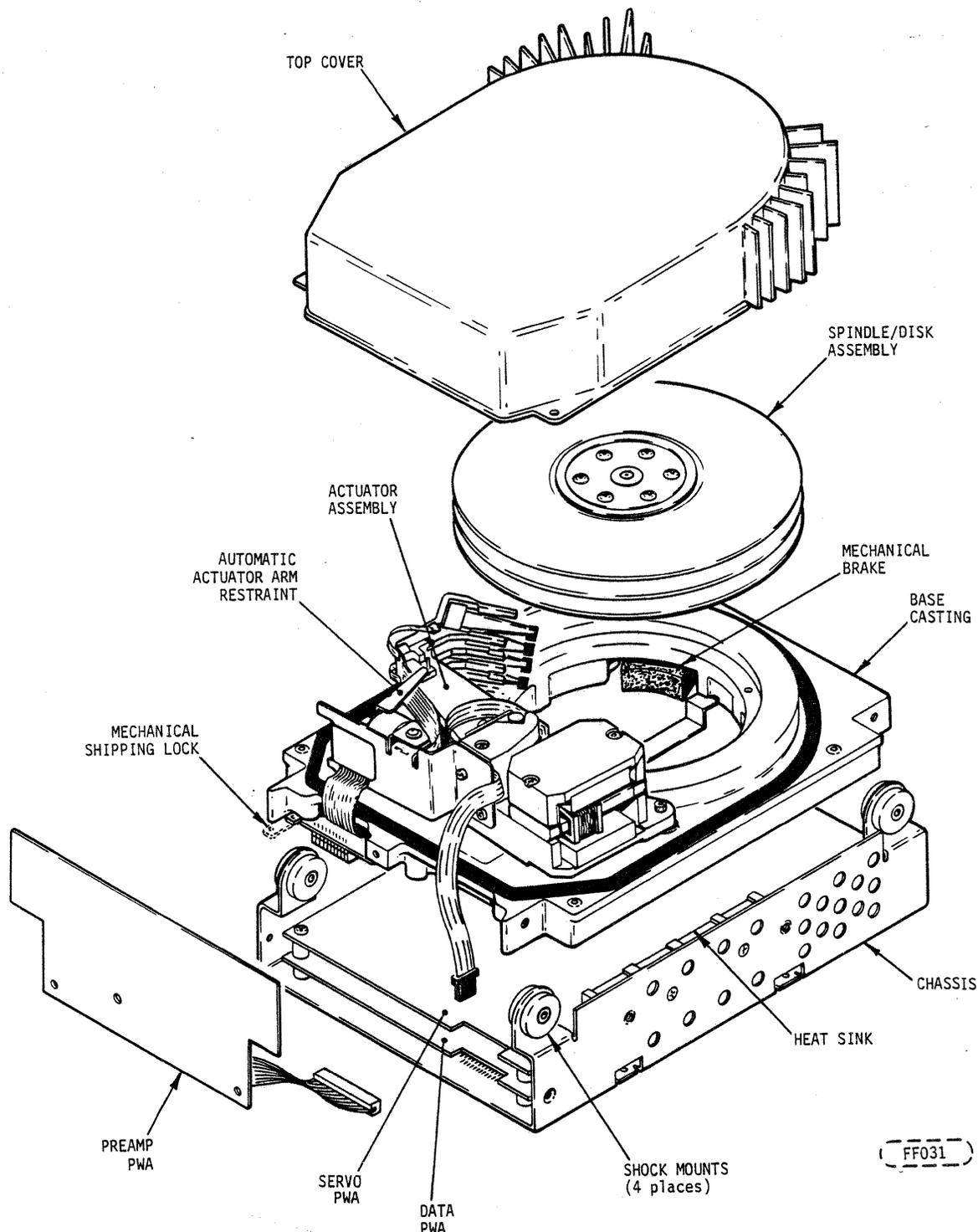
FIGURE 2. 9415-3 WREN

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3.0   -Continued

The 9415-3 WREN applies a brake to the spindle on power down. Disk rotation is stopped in less than 30 seconds, thus minimizing head to disk contact on landing.

4.0   FEATURES

4.1   STANDARD FEATURES

The 9415-3 WREN has the following standard features:

- Full data recovery circuitry

- Sealed head, disk, and actuator chamber

- No preventive maintenance required

- LSI circuitry for high reliability

- Low audible noise for office environments

- Vertical (side) or horizontal (bottom) mounting

- Low power consumption

- Rotary voice coil actuator

- Mechanical shipping lock

- OEM Manual

- Automatic actuator arm restraint

- Terminators

- Dedicated landing zone

- Shock mounts

- Spindle brake

4.2   OPTIONAL CONFIGURATION (FACTORY INSTALLED ONLY)

The following optional capacities are available for the 9415-3 WREN:

- 21 or 35 megabyte capacity

5.0   PERFORMANCE CHARACTERISTICS

9415-3 WREN I	Model Capacity (Unformatted)	
● 9415-3-21	21,077,280 Bytes	
	2 Disks per Drive	
	3 Data Surfaces	
● 9415-3-35	35,128,800 Bytes	
	3 Disks per Drive	
	5 Data Surfaces	

Data Capacity Parameters (Unformatted)		
Bytes/Track	10,080 Bytes	
Bytes/Surface	7,025,760 Bytes	(NOTE 1)
Tracks/Surface	697	(NOTE 2)
Tracks/Inch	800 TPI	
Bits/Inch	9,244 BPI	
Track Format		
Soft Sectored	User Defined	
Recording Mode	MFM	
Data Transfer Rate	4.84 Megabits/sec (605 Kilobytes/sec)	
Data Interface	NRZ Data + Clock	
Rotational Speed	3600 r/min ±1.0%	
Average Latency	8.33 ms	
Step Pulse Rate Maximum	8 µs between Steps	
Step Pulse Rate Minimum	200 µs between Steps	(NOTE 3)
Single Track Seek Time	MAXIMUM 9 ms	(NOTE 4)
	TYPICAL 5 ms	
Average Seek Time (See 5.1.1)		
(Step Pulse Rate:	MAXIMUM 45 ms	(NOTE 4)
Less than 80 µs	TYPICAL 40 ms	
Between Steps)		
Maximum Seek Time		
(697 Tracks) (Step	MAXIMUM 90 ms	(NOTE 4)
Pulse Rate: Less than	TYPICAL 80 ms	
80 µs between Steps)		

NOTE 1: Based on 697 cylinders. Spare tracks are included.
NOTE 2: See Media Characteristics, paragraph 8.0.
NOTE 3: See Step pulse description, paragraph 13.1.2.
NOTE 4: The maximum is specified over the worse case conditions of temperature, voltage margins and drive orientation. All seek times include settle time. When comparing seek times, care should be taken not to mix typical seek times with maximum seek times. The only true comparison is with system benchmark tests.

5.1   ACCESS TO DATA CHARACTERISTICS

5.1.1   Seek Time

Seek time is defined as the time required from the receipt of a seek or position command by the 9415-3 WREN until the drive signals the controller that is is ready to perform another seek or read/write function on the new cylinder. Average seek time is determined by dividing the sum of the time for all possible movements by the total number of movements.

5.1.2   Spindle Speed and Latency

The spindle speed is 3600 $\pm$1.0% r/min. The speed tolerance includes motor performance and motor control circuit tolerances.

The average latency time is 8.33 milliseconds, based on a nominal disk speed of 3600 r/min. The maximum latency time is 16.83 milliseconds based on a minimum disk speed of 3564 r/min.

5.1.3   Read to Write Recovery Time

Assuming a read operation is in progress, the required minimum time interval between the end of Read Enable and the initiation of Write Enable is 5 servo clock periods.

5.2   READ DATA TRANSFER RATE

The nominal read serial data transfer rate is 4.84 Mbits per second. The range of transfer rate variations on a bit per second basis for read/write operations is $\pm$3% of the nominal. This range includes the effects of all factors including spindle speed variations and dynamic jitter on a byte to byte basis. Data on the interface is NRZ plus clock.

5.3   START/STOP TIME

The 9415-3 WREN will become ready less than 35 seconds after application of DC power. Stop time will be less than 30 seconds after removal of DC power.

There is no power control switch on the drive.

6.0   RELIABILITY SPECIFICATIONS

The following reliability specifications assume correct host/drive operational interface has been implemented, including all interface timings, power supply voltages, environmental conditions, and appropriate data-handling circuits in the host system.

Error Rates
  Soft Read Errors   Less than 1 in 10^{10} bits transferred
  (Recoverable)

  Hard Read Errors   Less than 1 in 10^{12} bits transferred
  (Unrecoverable)

  Seek Errors   Less than 1 in 10^{6} seeks

MTBF   Mature MTBF = 15,000 Hours

Service Life   5 years or 30,000 Hours

Preventive Maintenance   None Required

6.1   ERROR RATES

The error rates stated in this specification assume the following:

a. That the 9415-3 WREN is operated per this specification utilizing the CDC provided accessory power supply or its equivalent.
b. That a data format is employed fulfilling the requirements of the 9415-3 WREN as outlined in Section 14.
c. That errors caused by media defects or host system failures are excluded from error rate computations. Refer to paragraph 8.0, Media Defect Recognition.
d. That power requirements are as specified in paragraph 7.2.
e. That all read/write operations are accomplished with the same physical orientation of the drive. (Refer to paragraph 7.5.1.)
f. That nominal strobe timing and no offset conditions are used.

6.1.1   Read Errors

Prior to the determination or measurement of read error rates:

a. The data which is to be used for a measurement of read error rates must be verified as being written correctly on the media.
b. All media defect induced errors must be excluded from error rate calculations.

A recoverable read error is one that can be reread correctly in 2 sets of 10 retries. After 10 retries, a recalibrate (RTZ) and seek to desired address must be accomplished. The recoverable read error rate for any read operation shall be less than one error in 10^{10} bits read.

An unrecoverable read error is one that cannot be read correctly after 2 sets of 10 retries. The unrecoverable read error rate for any read operation shall be less than one bit in 10^{12} bits read. A customer may wish to implement early/late strobe and offset +/- in his retry routine (see paragraph 9.0).

6.1.2   Environmental Interference

When operating at low effective data transfer rate, (that is, random access of single short records) the effective error rate may be expected to exceed the specified limits due to environmental interference. Excluding environmental interference, the recoverable read error rate shall be no more than one error in eight hours of operation.

When evaluating system operation under conditions of EMI the performance of the 9415-3 WREN within the system shall be considered acceptable if the device does not generate an unrecoverable error, or incur an unrecoverable condition.

An unrecoverable error, or condition, is defined as one which:

1. Is not detected and corrected by the device itself;
2. Or is not capable of being detected from the error or fault status provided through the device/system interface;
3. Or is not capable of being recovered by normal device or system recovery procedures without requiring operator intervention.

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6.1.3   Write Errors

Write errors can occur as a result of the following: write data not being presented correctly, media defects, environmental interference, or equipment malfunction. As such, write errors are not predictable as a function of the number of bits passed.

If an unrecoverable write error occurs because of an equipment malfunction in the 9415-3 WREN, the error is classified as a failure affecting MTBF. Unrecoverable write errors are those which cannot be corrected within four attempts at writing the record with a verify after each attempt, (excluding identified media defects).

6.1.4   Seek Errors

A seek error is defined as a condition where the drive fails to position the heads to the addressed track provided the correct stepping information has been presented to the 9415-3 WREN. This condition must be determined by the controller by reading headers. There shall be no more than one recoverable seek error in 10^6 physical seek operations. Unrecoverable seek errors are classified as failures for MTBF calculations.

6.2   RELIABILITY AND SERVICE

6.2.1   Mean Time Between Failure

The mature mean time between failure (MTBF) shall exceed 15,000 hours for the 9415-3 WREN I. MTBF is further defined as the "Operating Hours" divided by the "Number of Equipment Failures".

"Operating Hours" means total power on hours less any maintenance time. "Equipment Failure" means any stoppage or substandard performance of the equipment because of equipment malfunction, excluding stoppages or substandard performance caused by operator error, adverse environment, power failure, controller failure, cable failure, or other failure not caused by equipment. To establish a meaningful MTBF, operation hours must be greater than an average of 5200 hours per drive and shall include field performance data from all field sites.

The term equipment failure implies that maintenance is required because of a hardware failure.

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6.2.2   Preventive Maintenance

No routine scheduled preventive maintenance shall be required.

6.2.3   Service Life

The 9415-3 WREN shall have a useful service life of five years or 30,000 hours, whichever occurs first, before requiring factory overhaul. Depot repair or replacement of major parts will be permitted during the lifetime (6.2.4).

6.2.4   Service Philosophy

Due to the sophisticated design and special equipment required to repair the 9415-3 HDA, repairs may only be effected at a properly equipped and staffed depot service and repair facility. Although 9415-3 is designed for depot repair service, some items may be replaced in the field as defined in the Maintenance Manual.

6.2.5   Installation

The 9415-3 is designed, manufactured, and tested with a "Plug-in and Play" installation philosophy. Basically, this philosophy minimizes the requirements for highly trained personnel to integrate a 9415-3 into the OEM's system, whether in a factory or field environment. An OEM Manual is provided to facilitate installation.

6.2.6   Service Tools

No special tools are required for site installation. Should field repair of items external to the HDA be desired, two sizes of 6 point TORX drivers are required. They may be ordered through CDC by the following part numbers:

        PN 1226 3628 - T9
        PN 1226 3629 - T15

7.0   PHYSICAL ELECTRICAL SPECIFICATIONS

7.1   AC POWER REQUIREMENTS

None.

7.2   DC POWER REQUIREMENTS

The voltage and current requirements for a single 9415-3 WREN are shown in the following table. Values indicated apply at the drive power connector.

TABLE 1. DC POWER REQUIREMENTS

	+5 V DC	+12 V DC
VOLTAGE -		
REGULATION	±5%	±5% ②
RIPPLE	50 mV	100 mV
MAXIMUM OPERATING CURRENT ①	1.5 A	2.5 A
TYPICAL OPERATING CURRENT ①	1.2 A	1.8 A
MAXIMUM STARTING CURRENT (PEAK)	2.0 A	4.5 A

① Measured with average reading DC ammeter.

② A 10% tolerance is permissible during power up.
The ±5% must be maintained commencing with Unit Ready.

NOTE 1:   At power-up, the motor current regulator will limit the 12-volt current to a peak value of less than 4.5 amps.

NOTE 2:   Minimum current loading for each supply voltage is not less than 30% of the maximum operating current shown in Table 1.

NOTE 3:   The +5 and +12 volt supplies shall have separate returns.

NOTE 4:   Where power is provided to multiple drives from a common supply, careful consideration for individual drive power requirements should be noted. Where multiple units are powered on simultaneously, the peak starting current must be available to each device (Reference Table 1).

7.2.1   Power Sequencing

Power sequencing is not required for the WREN 1. The 9415-3 protects against inadvertent writing during power up and down. Daisychain operation requires that power be maintained on the terminated unit to insure proper termination of the peripheral I/O.

FF039c
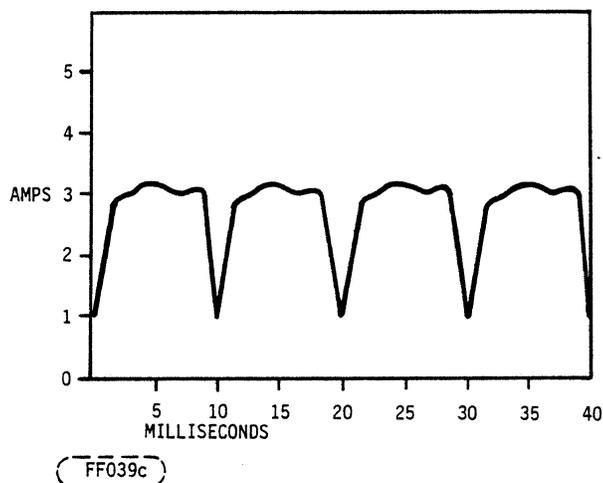
FIGURE 3. TYPICAL STARTING CURRENT
(+12 V SUPPLY)

7.2.2   12 V Current Profile

Figure 4 identifies the 9415-3 WREN 12 V DC current profile. The current during the various times is as shown:

T1 Power is initially applied to the drive, the spindle brake is released and the spindle begins to accelerate under current limiting.

T2 The spindle continues to accelerate, but current is less than the current limit.

T3 The spindle is up to speed (3600 RPM).

T4 The auto-velocity adjust sequence is performed.

7.2.2   -Continued

T5 Velocity is set and the drive is ready for reading and writing.

T6 Power is removed from the drive.

NOTE

All time and currents are typical. See Table 1 for worst case current requirements.
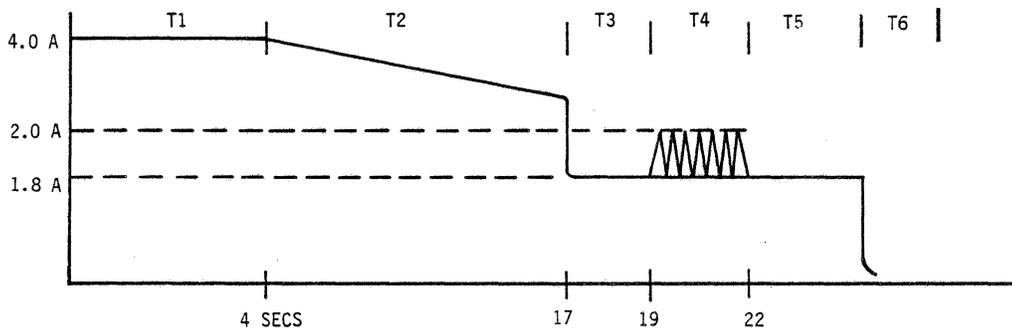
FIGURE 4. TYPICAL 9415-3 WREN +12 V CURRENT PROFILE

7.3   HEAT/POWER DISSIPATION

Each 9415-3 WREN will dissipate no more than 38 watts (133 BTU's per hour) of DC power average. Typical power dissipation under nominal conditions is 28 watts.

7.4   ENVIRONMENTAL LIMITS

Temperatures and humidity specifications preclude condensation on any drive part. Altitude and atmospheric pressure specifications are referenced to a standard day at 58.7° F (14.8° C).

7.4.1   Temperature

a. Operating

50° to 114.8° F (10° to 46° C) operating ambient with a maximum gradient of 18° F (10° C) per hour. Above 983 feet (300 meters) altitude the maximum temperature is derated linearly to 104° F (40° C) at 6562 feet (2000 meters). Cabinet packaging designs must provide ample air circulation around the 9415-3 to ensure environmental limits are not exceeded as a result of heat transfer from other systems components. The temperature of the base deck should not be allowed to exceed 135° F.

Operating ambient for specification purposes is defined as the environment immediately surrounding the 9415-3.

b. Transit

-40° to 158° F (-40° to 70° C) package ambient with a maximum gradient of 36° F (20° C) per hour. This specification assumes that the drive is packaged in the shipping container designed by CDC for use with the 9415-3 WREN.

c. Storage

14° to 122° F (-10° to 50° C) device ambient with a maximum gradient of 27° F (15° C) per hour.

7.4.2   Relative Humidity

a. Operating

20% to 80% relative humidity with a maximum gradient of 10% per hour.

b. Transit

5% to 95% relative humidity.

c. Storage

10% to 90% relative humidity.

7.4.3   Effective Altitude (Sea Level Reference)

a. Operating

-983 to +9,830 feet (-300 to +3000 meters)

b. Transit

-983 to +9,830 feet* (-300 to +3000 meters)

c. Storage

-983 to 9,830 feet (-300 to +3000 meters)

7.4.4   Shock and Vibration

Shock and vibration limits specified in this document are measured directly on the drive chassis. If the 9415-3 is installed in an enclosure to which the stated shock and/or vibration criteria is applied, resonances may occur internally to the enclosure resulting in 9415-3 movement in excess of the stated limits. If this situation is apparent, it may be necessary to add shock or isolation mounts to the enclosure to minimize 9415-3 movement.

7.4.4.1   Shock

a. Operating - Normal

Equipment, as installed for normal operation, shall comply with the complete specified performance while subjected to intermittent shock not exceeding 2 g's at a maximum duration of 10 ms (half sinewave). Shock may be applied to the X, Y, or Z axis. Shock is not to be repeated more than two times per second.

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*Suitable for Commercial Air Freight Transportation.

7.4.4.1 -Continued

    b. Operating - Abnormal

    Equipment, as installed for normal operation, shall not incur non-recoverable errors or exhibit damage while subjected to intermittent shock not exceeding 10 G at a maximum duration of 10 ms (half sinewave). Shock may be applied in the X, Y, or Z axis. Shock is not to be repeated more than two times per second. Operator intervention will not be required. This assumes that normal system recovery routines are available.

    c. Non-Operating

    The limits of non-operating shock shall apply to all conditions of handling and transportation. This includes both isolated devices and integrated equipment.

    1. Manual Shipping Lock Not Activated (Unlocked)

    Equipment subjected to intermittent shock not exceeding 25 G at a maximum duration of 10 ms (half sinewave) shall not exhibit any form of device damage or performance degradation. Shock may be applied in the X, Y, or Z axis. Shock is not to be repeated more than two times per second.

    2. Manual Shipping Lock Activated (Locked)

    Equipment subjected to intermittent shock not exceeding 40 G at a maximum duration of 10 ms (half sinewave) shall not exhibit any form of device damage or performance degradation. Shock may be applied in the X, Y, or Z axis. Shock is not to be repeated more than two times per second.

    d. Packaged

    The 9415-3 as packaged by CDC for van or air freight shipment shall withstand drop test from 48 inches (1219.2 mm) against a concrete floor or equivalent. See Figure 5.
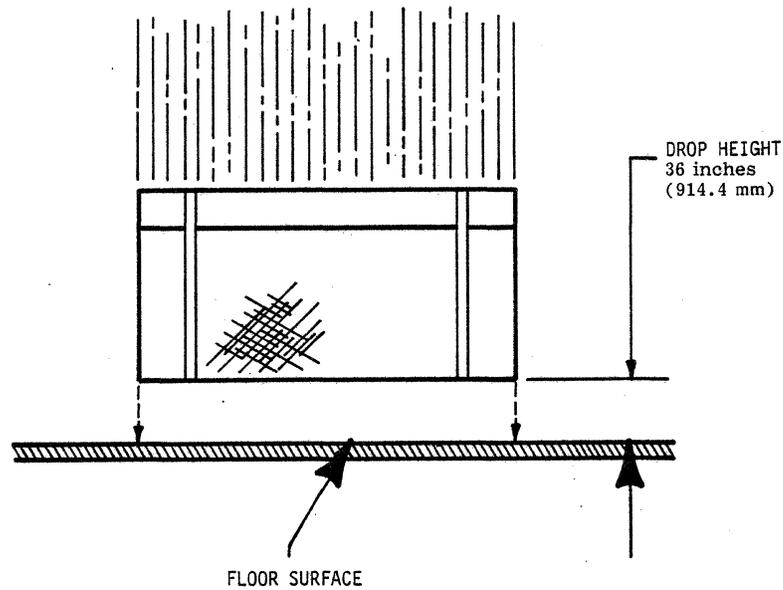
(G040a)

FIGURE 5. FLAT DROP TEST

7.4.4.2 Vibration

a. Operating-Normal

Equipment as installed for normal operation, shall comply with the complete specified performance while subjected to continuous vibration not exceeding

        5-22 Hz @ 0.010 inches displacement
        22-500 Hz @ 0.25 G

Vibration may be applied in the X, Y, or Z axis.

b. Operating-Abnormal

Equipment as installed for normal operation, shall not incur physical damage while subject to periodic vibration not exceeding

        15 minutes of duration at major resonant frequency
         5-22 Hz @ 0.010 inches displacement
        22-500 Hz @ 0.50 G

7.4.4.2 -Continued

Vibration occurring at these levels may promote degraded operational performance during the abnormal vibration period. Specified operational performance will continue without operator intervention when normal operating vibration levels are resumed. This assumes system recovery routines are available. Abnormal vibration may be applied in the X, Y, or Z axis.

c. Non-Operating

The limits of non-operating vibration shall apply to all conditions of handling and transportation. This includes both isolated devices and integrated equipment.

1. Manual Shipping Lock Not Activated (Unlocked)

Equipment shall not incur damage or degraded performance as a result of continuous vibration not exceeding

15 minutes of duration at major resonant frequency
 5-10 Hz @ 0.010 inches displacement
10-500 Hz @ 0.5 G

Vibration may be applied in the X, Y, or Z axis.

2. Manual Shipping Lock Activated (Locked)

Equipment shall not incur damage or degraded performance as a result of continuous vibration not exceeding

15 minutes of duration at major resonant frequency
 5-10 Hz @ 0.020 inches displacement
10-500 Hz @ 1.0 G

7.4.5   Air Cleanliness

The 9415-3 WREN is designed to operate in a typical office environment with minimum environmental control.

7.5 MECHANICAL SPECIFICATIONS

The following dimensions are exclusive of the decorative front panel accessory. Refer to Figure 6a for detailed mounting configuration dimensions. The illustration and dimensions are preliminary and subject to revision.

Height:	3.25 inches	82.55 millimeters
Width:	5.75 inches	146.05 millimeters
Depth:	8.0 inches	203.2 millimeters
Weight:	Approximately 7.5 pounds	Approximately 3.375 kilograms

NOTES:

1. MOUNTING HOLES, FOUR ON BOTTOM, TWO ON EACH SIDE. 6-32 UNC. MAX SCREW LENGTH INTO CHASSIS 0.31 IN. (7.87 mm)

2. FRONT PANEL ACCESSORY

3. DRIVE INTERFACE CONNECTIONS

4. MECHANICAL SHIPPING LOCK

5. WEIGHT IS APPROX. 7.50 LBS (3.4 Kg)

	IN	CM
A	8.0 MAX	20.32
B	5.75 +0.00 -0.02	14.6
C	0.29 ± 0.02	.74
D	1.87 ± 0.02	4.75
E	3.12 ± 0.01	7.92
F	5.88 ± 0.01	14.9
G	3.38 ± 0.02	8.58
H	0.065 ± 0.02	.165
J	5.50 ± 0.02	13.97
K	0.86 ± 0.02	2.18
M	3.25 ± 0.02	8.25
N	0.37 REF	.94 REF
P	0.63 REF	1.60 REF

FIGURE 6a. MOUNTING CONFIGURATION DIMENSIONS

(FF036)

7.5.1 Drive Orientation

The 9415-3 WREN can be mounted in either of two positions:

Vertical Mount - Vertical mounting (see Figure 6a, Note 4), Mechanical shipping lock must always be located on top.

7.5.1   -Continued

<u>Horizontal Mount</u> - On its electronics chassis with the sealed unit facing up.

Further details on mounting are included in the OEM Manual.

7.5.2   Cooling

The cabinet cooling must be designed by the customer so that the ambient temperature around the 9415-3 WREN will not violate temperature conditions specified in 7.4.1.

The 9415-3 WREN design uses the WREN chassis to dissipate heat. Direct contact to the internal WREN heat sink can be made through the two mounting holes on the right side of the WREN (see Figure 6b). Good metal to metal thermal contact of this surface with the customer cabinet mounting hardware is highly recommended for optimized heat transfer. Consideration should also be given to minimizing restriction of airflow through cooling holes in the drive.

THERMAL COUPLE SHOULD BE PLACED BETWEEN THE BASE PLATE AND SHOCK MOUNT. TEMPERATURE MUST NOT EXCEED 134.6° F.

SHIPPING LOCK FRONT ACCESS

F293 b

MOUNTING HOLES MAY ALSO BE USED TO PROVIDE HEAT DISSIPATATION
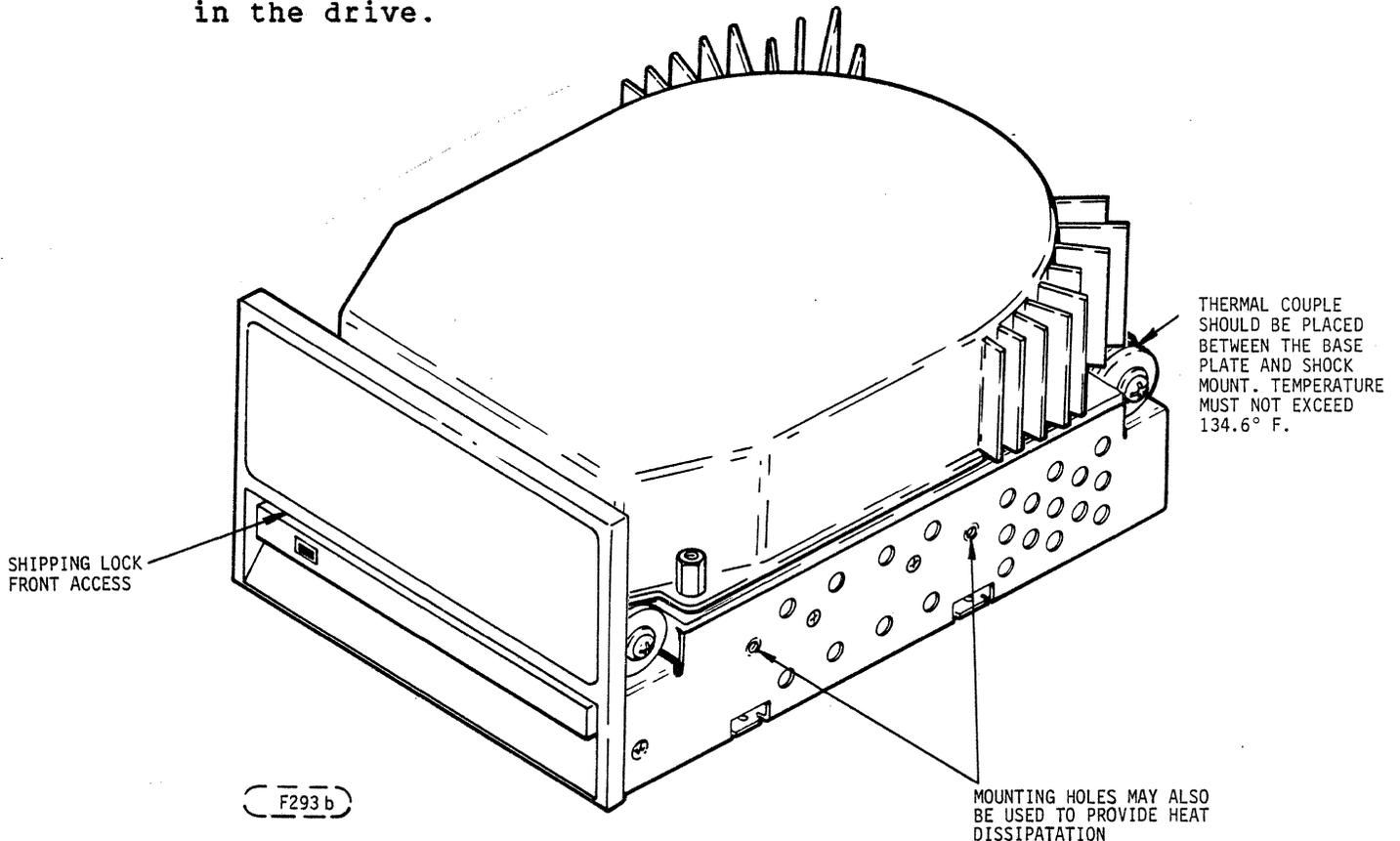
FIGURE 6b. 9415-3 WREN COOLING

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8.0   MEDIA CHARACTERISTICS

8.1   MEDIA DESCRIPTION

The media used on the 9415-3 WREN has a diameter of approximately 5 1/4 inches (130 mm). The aluminum substrate is coated with ferrous oxide and lubrication to permit the heads to contact the surface when starting and stopping.

Each data surface has total of 697 tracks and is capable of recording 7,025,760 bytes of unformatted data. Eighteen spare tracks are provided for track reallocation in the event of media flaws.

Media defects are characterized as being either correctable or uncorrectable as a function of the type and magnitude of the media flaw. Various error correction codes may be implemented to correct errors in the data read from the disk. However, the code chosen should be consistent with the media manufacturers media testing and certification methods. In the 9415-3 WREN media certification is performed using the following standards:

1. An error burst of 11 bits or less is a correctable error.
2. An uncorrectable error is one greater than 11 bits in length.

Host systems utilizing the 9415-3 WREN should have, as a minimum, resident capabilities to recognize and map defective tracks and perform tracks allocation routines.

At the time of shipment from the point of manufacture, the 9415-3 WREN recording surfaces will meet the following requirements.

1. 697 Total tracks per surface
2. Track 0 to be error free on each data surface.
3. 11 Defects per surface maximum.
4. Accumulative defects not to exceed 1 per megabyte based on total available data capacity.

At the time of manufacture, media defect information is recorded in surface 0, track 696, and sector 0 (see Figure 7). This identifies flagged track data for those customers who wish to use it as part of a system initialization and track deallocation routine without recertification. If the customer wishes to use this data, it is imperative not to write on this area of the disk until the information has been recovered.

8.1   -Continued

Because the 9415-3 WREN is a soft sectored unit, the customer, after retrieving the ETF information, must calculate where the defective sector is located. Following is an example of how this should be done.

Using the formula of $L = \dfrac{N.D}{210}$

where N = the number of sectors in the customer's format
where *D = the byte count divided by 48 (BCD48). The BCD48 number will be in the format log at Track 696 and also on the flag track label supplied with the unit
where L = the customer's defective sector

EXAMPLE: Sectors in customer's format   = 24
           Byte count in factory format log = 150

           $L = \dfrac{24.150}{210}$
           L = 17 rounded down
           Sector 17 will be the customer's defective sector.

The ETF information will also be recorded on a label affixed to the WREN HDA. This label will record the media defects by cylinder, head, byte count after index, and type. The byte count after index (BCAI) is relative to a single record with a total length of 10080 bytes. The customers defective sector can be calculated by multiplying the number of sectors in the customer format by the ratio if BCAI to total single record length.

EXAMPLE: Sectors in customers format = 24
         BCAI = 7200
Defective sector = 24. $\dfrac{7200}{10080}$ = 17 (rounded down)

Error type will be either correctable (C) or uncorrectable (U).

_____

*The format log has room for only one byte of the byte count information. Therefore, the 10,080 bytes per track are divided by 210. This gives a number that will fit into the one byte area.
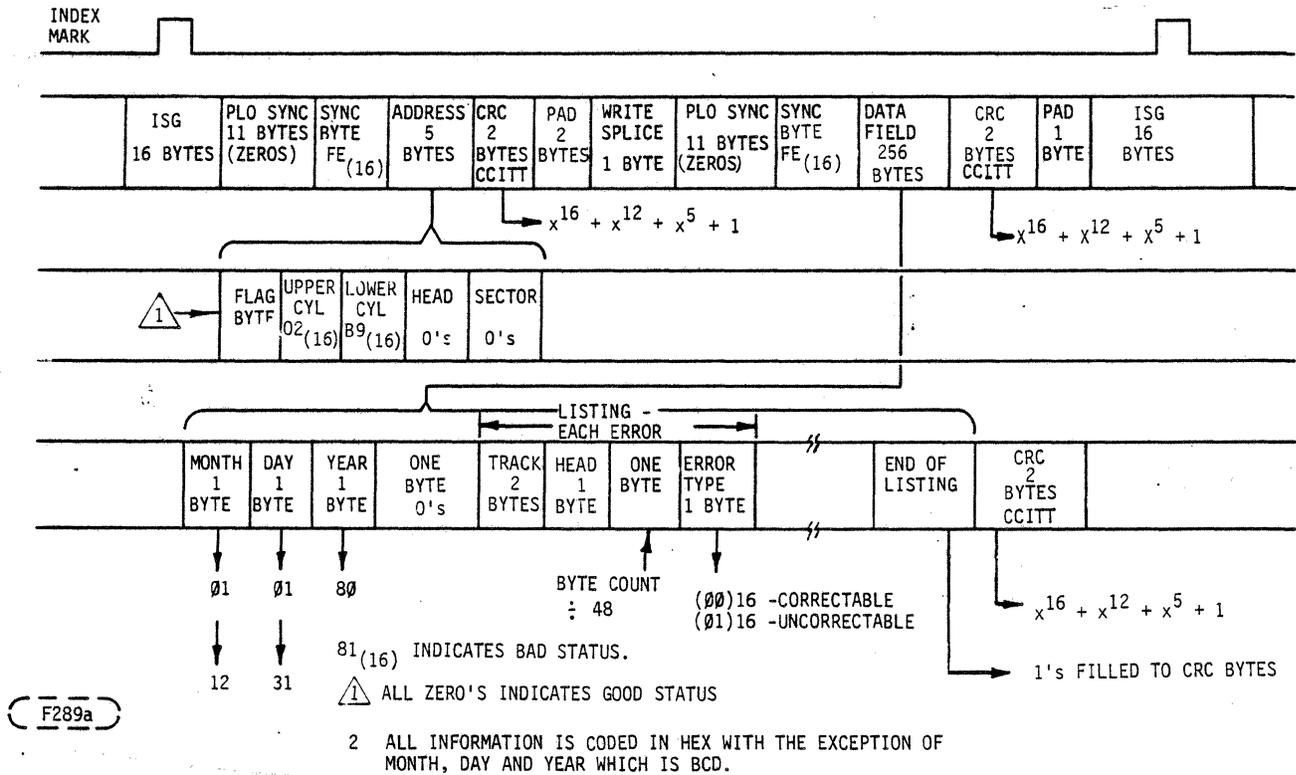
FIGURE 7. FORMAT FOR SURFACE 0, TRACK 696, SECTOR 0--
FACTORY FLAGGED TRACK DATA TRACK

9.0   EARLY/LATE STROBE AND OFFSET PLUS/MINUS

The Read Error rate is specified with normal strobe
timing and no offset. The use of early and late strobes
and plus and minus offsets are provided for utilization
as marginal data recovery mechanisms only. Long term
operation in these modes is not recommended or specified.
Refer to Section 13.1.5.

The following outline is a suggested retry format:

1. First use Early/Late Data Strobes
2. Second use Actuator Offsets plus and minus
3. Third use combinations of Early/Late Data Strobes and
   Actuator Offsets

	1	2	3	4	5	6	7	8	9
NOMINAL	X								
EARLY DATA STROBE		X				X		X	
LATE DATA STROBE			X				X		X
OFFSET PLUS				X		X	X		
OFFSET MINUS					X			X	X

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10.0   TRACK OR SECTOR REALLOCATION

The error rate and data capacity specifications of the
9415-3 WREN do not require the utilization of sector
reallocation or error correction codes (ECC). However,
the 9415-3 WREN design does not preclude the use of
sector reallocation or ECC to aid in recovery of marginal
data areas if desired by the user. The use of either
method permits the continued use of the major portion, or
perhaps all, of a track when a defect is found.

To maximize the available storage capacity, a bad track
or bad sector reallocation customer-designed program is
required.

Under typical bad track reallocation, the defective track
is reallocated to one of the spare tracks provided. Bad
track (or sector) location information is normally
recorded on track 696 and read into the customer's
operating program during program initialization.

11.0   INTERFACE CABLING REQUIREMENTS/OPTIONS

11.1   RADIAL CONFIGURATION

Interface cabling options for the 9415-3 WREN are shown
in Figure 8. View A of Figure 8 shows each drive
interfaced to its own command cable, which, in turn,
allows interfacing of any number of drives and a variety
of system operational techniques. Each drive has its data
cable and command cable radially connected to the host
controller. The length of each individual cable must not
exceed 20 feet (6.1 meters). Terminator resistors must be
installed in the host controller for each data cable and
for each command cable. If instead of all 9415-3 WRENs
there are FDDs plus 9415-3 WRENs in this radial
configuration, then a terminator resistor pack also would
be installed in each FDD for its data/command cable.

11.2   DAISYCHAIN CONFIGURATION

A daisychain configuration incorporates parallel
interfacing of the disk drives on a common command cable.
A maximum of three drives may be daisychained on the
command cable. Only the drive which is selected by the
host system has its control and data signals through this
common interface.

11.2   -Continued

View B of Figure 8 consists only of 9415-3 WRENs. A terminator resistor pack is required in the host controller for each data cable. Only the last 9415-3 WREN in the daisychain requires a terminator resistor pack for the command cable. Terminator resistor packs for the command cable of other drives are removed. The total combined command cable length (from the controller to the first drive, to the second and subsequent drives) must not be more than 20 feet (6.1 meters).

View C of Figure 8 consists of a common controller for both 9415-3 WRENs and FDDs. A maximum of three drives (any combination of FDDs plus 9415-3 WRENs) may be daisychained on the command cable. Terminator resistors are required in the controller and in the last drive in the daisychain for the command cable. Terminator resistor packs for the command cable of other drives would be removed. A terminator resistor pack is required in the controller for each data cable. The total combined command cable length (from the controller to the first drive, to the second and subsequent drives) must not be more than 20 feet (6.1 meters).

CAUTION

A 9415-3 WREN must be the last drive in
the daisychain.

Refer to paragraph 13.1.1 for logical drive selection.
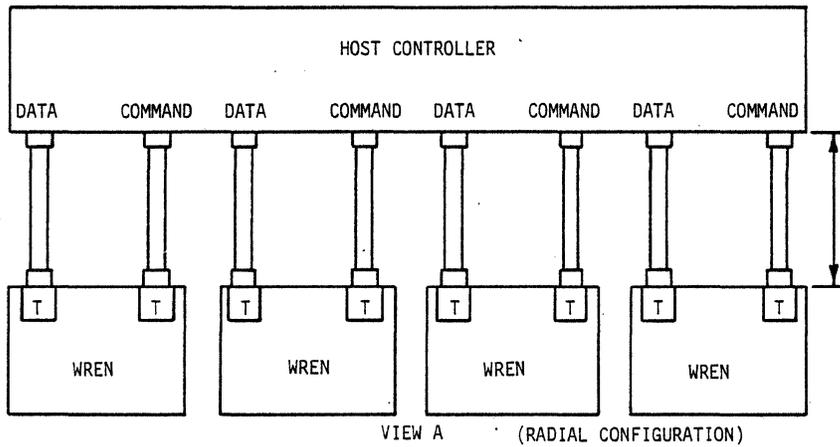
NOTE 3: EACH COMMAND CABLE LENGTH MUST NOT EXCEED 20 FEET (6.10 m). EACH DATA CABLE LENGTH MUST NOT EXCEED 20 FEET (6.10 m).

VIEW A   (RADIAL CONFIGURATION)

NOTE 3: TOTAL COMMAND CABLE LENGTH MUST NOT EXCEED 20 FEET (6.10 m). EACH DATA CABLE LENGTH MUST NOT EXCEED 20 FEET (6.10 m).

VIEW B   (DAISY-CHAIN CONFIGURATION)

NOTE 3: TOTAL COMMAND CABLE LENGTH MUST NOT EXCEED 20 FEET (6.10 m). EACH DATA CABLE LENGTH MUST NOT EXCEED 20 FEET (6.10 m).

VIEW C   (DAISY-CHAIN CONFIGURATION)
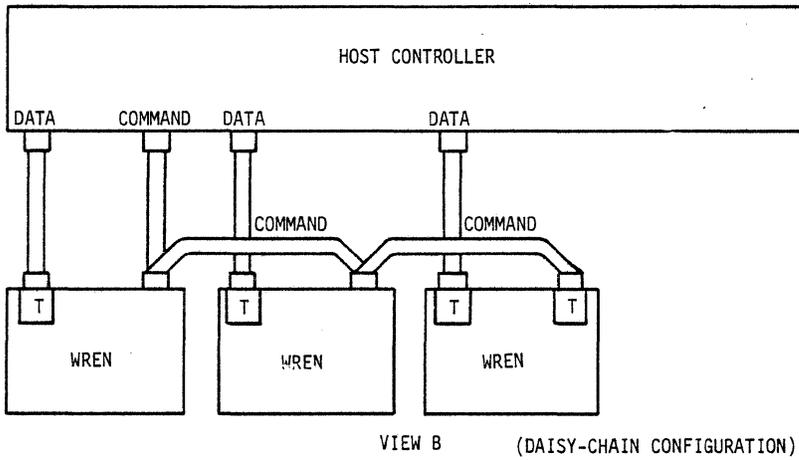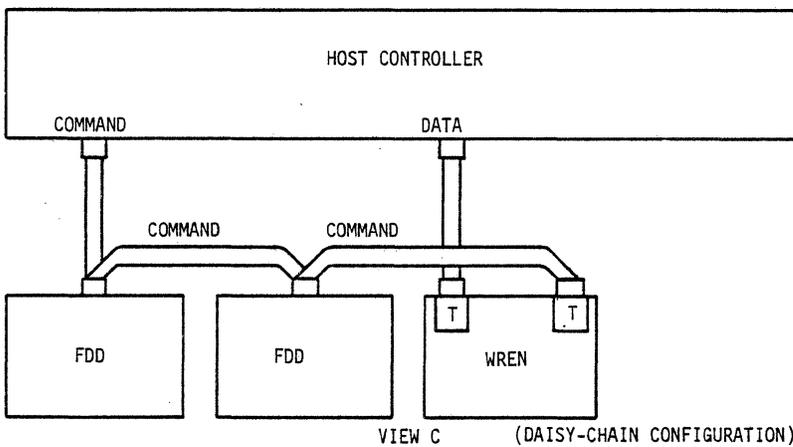
NOTE 1: T INDICATES TERMINATOR RESISTOR PACK. WREN DATA CABLES ARE PERMANENTLY TERMINATED.

NOTE 2: A WREN MUST BE THE LAST DRIVE IN THE DAISY CHAIN. A MAXIMUM OF THREE DRIVES MAY BE DAISY CHAINED.

G163a

FIGURE 8. INTERFACING CABLING OPTIONS

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11.3   DC CABLE AND CONNECTOR

The 9415-3 WREN receives DC power through a 4-pin right angle connector (see Table 2 for pin assignment) mounted on the servo circuit board (see Figure 9). Recommended part numbers for the mating connector are included below, but equivalent parts may be used (see Table 3).

TABLE 2. DC INTERFACE

POWER LINE DESIGNATION	PIN NUMBER
+12 Volts	J2-01
+12 Volts Return	J2-02
+5 Volts Return	J2-03
+5 Volts	J2-04

TABLE 3.

TYPE OF CABLE	CONNECTOR	CONTACTS
18 AWG	AMP 1-480424-0	AMP 60619-4 (Loose Piece)
		AMP 61117-4 (Strip)

11.4   DATA CABLE AND CONNECTOR

Refer to Figure 9a for a pictorial representation of the Data cable interface. Recommended part numbers for the mating connector are included below, but equivalent parts may be used.

CONNECTOR (20-Pin) PART NO.

3M-3421-3000
AMP 86904-2

CABLE

Flat Cable (Stranded AWG 28)
3M-3365-20

Flat Cable (Stranded AWG 28)
3M-3476-20 (Shielded Cable)

DRIVE SELECT
PLUG

TERMINATION
PLUG

TERMINATOR
RESISTOR PACK

DATA CABLE
CONNECTOR

COMMAND CABLE
CONNECTOR

DIFFERENTIAL
TERMINATOR
JUMPERS

DC POWER CONNECTOR

POWER	
1 - +12 V	
2 - +12 V RET	
3 - +5 V RET	
4 - +5 V	

FF025
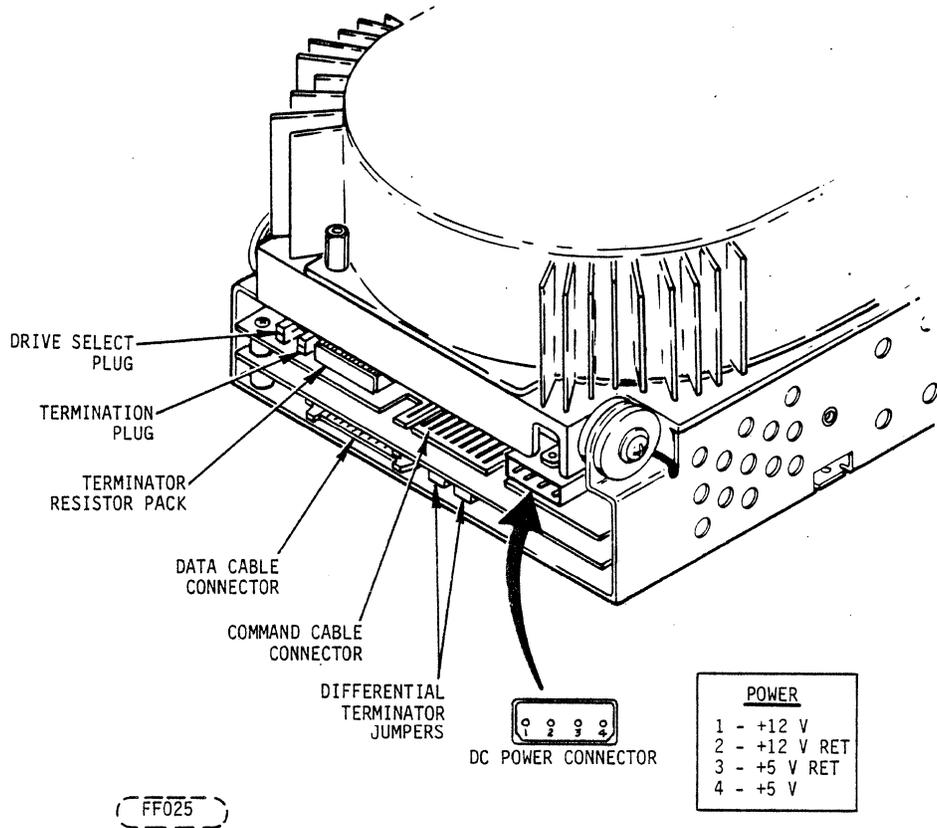
FIGURE 9. 9415-3 I/O CONNECTION

33
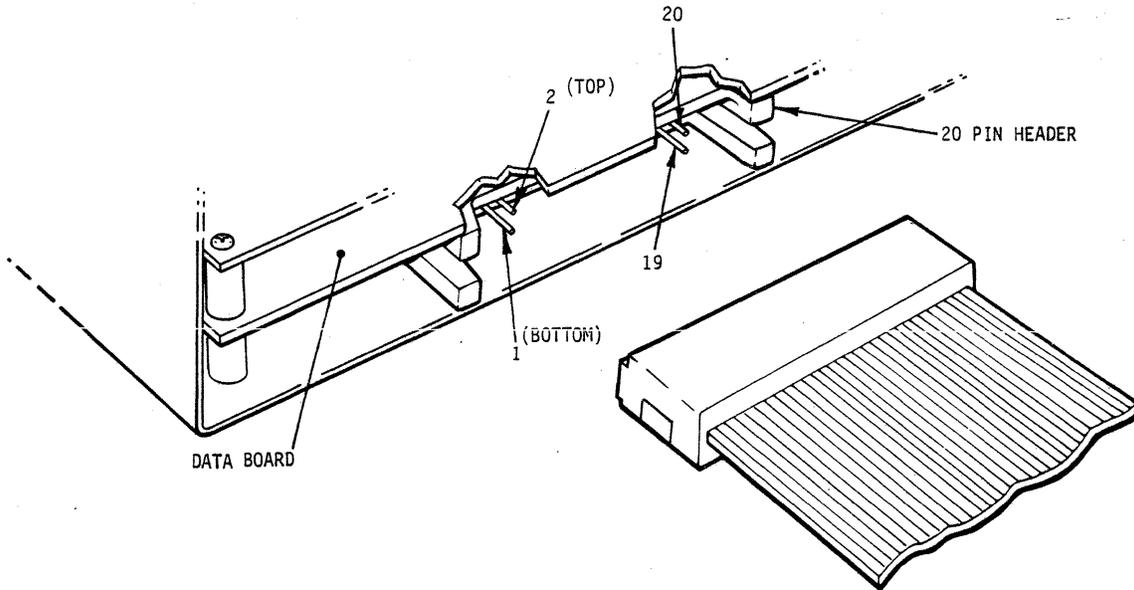
(FF054)

FIGURE 9a. DATA CABLE INTERFACE

11.5   COMMAND CABLE AND CONNECTOR

The I/O connector for the command interface is a 34-pin
board-edge connector. The odd pins are located on the
non-component side of the printed circuit board and are
connected to the ground plane. The even pins are on the
component side of the printed circuit board. A key slot
is provided between pin 4 and 6. (See Figure 9b.) CDC
recommends keying this connector to prevent the
possibility of installing it upside down.

Recommended part numbers for the mating connector are
included below, but equivalent parts may be used.

CONNECTOR (34-Pin)

3M-3463-0001
AMP 88373-3

CABLE

Flat Cable (Stranded AWG 28) 3M-3365-34
Flat Cable (Stranded AWG 28) 3M-3476-34 (Shielded
cable)
Spectra Strip Twist'n Flat 455-248-34 (Stranded AWG
28 Twisted Pair)

11.5   -Continued

KEYED CONNECTOR

AMP 583764-1
3M 3439-0000

11.6   INTERFACE DRIVERS/RECEIVERS

The 9415-3 WREN utilizes two types of signals --
single-ended and balanced differential. The data and
clock signals utilize balanced differential drivers and
receivers. All other signals utilize single-ended drivers
and receivers.

11.6.1   Single-Ended Drivers/Receivers

11.6.1.1 Transmitter Characteristics

The 9415-3 WREN uses the 7438 open collector quad-2-input
driver to transmit status to the host. This driver is
capable of sinking a current of 48 mA with a low-level
output voltage of 0.4 volt (see Figure 10).
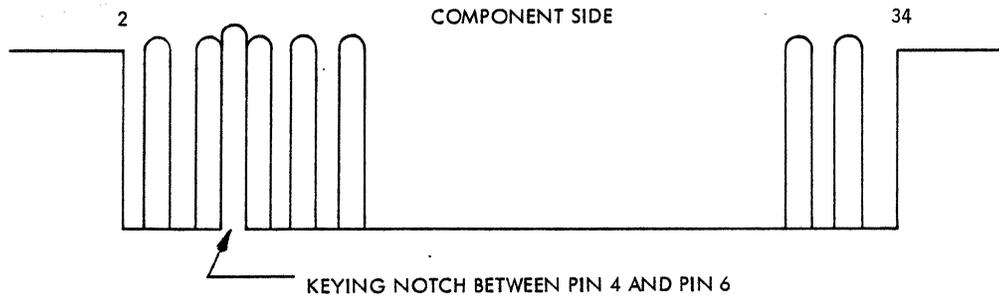
FIGURE 9b. COMMAND CABLE INTERFACE

11.6.1.2 Receiver Characteristics

The 9415-3 WREN uses the 74LS14 Hex Inverter with
hysteresis gate as a line receiver. The input of each
receiver is terminated in 150 ohms as shown in Figure 10,
except the Drive Select lines (Figure 11) and Write
Enable (Figure 12).

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HOST LINE DRIVER

WREN LINE RECEIVER
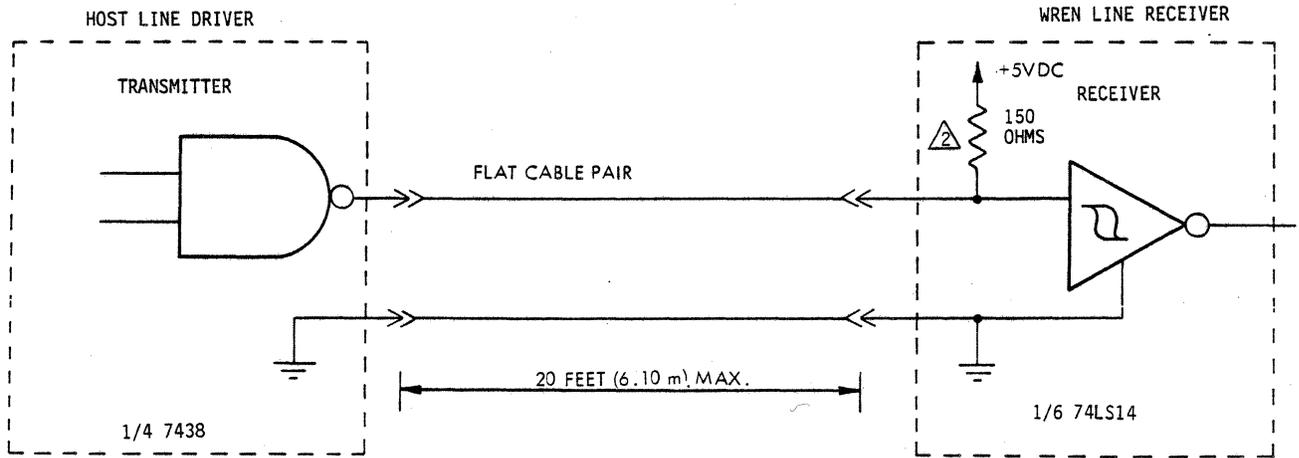
1. INTERFACE SIGNALS LEVELS AND LOGICAL SENSE AT THE WREN I/O CONNECTOR ARE DEFINED AS FOLLOWS:

⚠2 PART OF REMOVABLE RESISTOR PACK.

LOGIC LEVEL		WREN OUTPUT	WREN INPUT
HIGH (FALSE OR DEACTIVATED)	(0)	≥ 2.4 V; ≤ 5.0 V	≥ 2.0 V; ≤ 5.0 V
LOW (TRUE OR ACTIVATED)	(1)	≤ 0.4 V; ≥ 0.0 V	≤ 0.8 V; ≥ 0.0 V

THE DIFFERENCE IN THE VOLTAGES BETWEEN INPUT AND OUTPUT SIGNALS IS DUE TO THE LOSSES IN THE CABLE.

F290a

FIGURE 10. SINGLE-ENDED TRANSMITTERS AND RECEIVERS

11.6.1.3 Terminator Characteristics (General)

The terminators for all single-ended input lines to the 9415-3 WREN (except the Drive Select and Write Enable lines) consist of a DIP resistor module pack which is inserted as shown in Figure 9.

11.6.1.4 Termination of Drive Select Lines

Whereas all the other input lines to the 9415-3 WREN are terminated only in the last drive on the daisychain, it is recommended that each 9415-3 WREN on the daisychain terminate its own unit select line. This ensures that all drives will not be selected should the last drive in the line lose power. Termination of the Drive Select lines is accomplished by installing a shunt on the Drive Select termination jumper in the position which matches that to which the drive is selected (see Figure 11). Should the 9415-3 WREN be daisychained with an FDD which does not provide its own termination of Drive Select, the Drive Select line for the FDD may be terminated by installing an additional jumper in the appropriate position on the last 9415-3 WREN in the chain.

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FIGURE 11. DRIVE SELECT TERMINATION
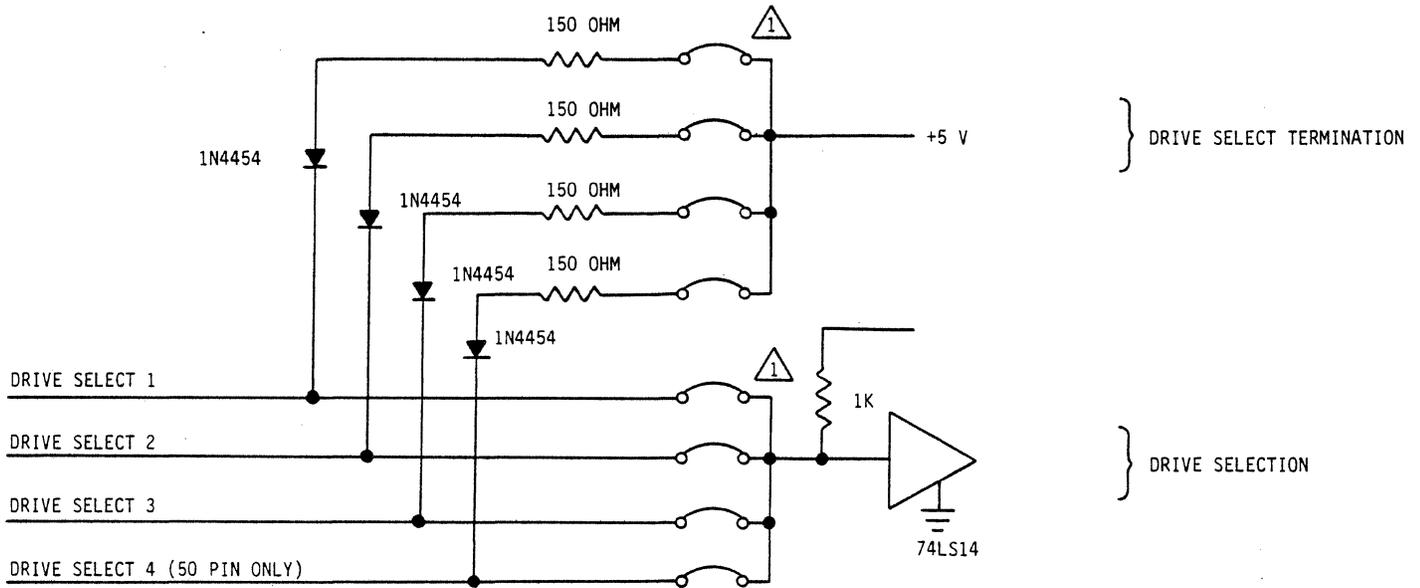
1. See Figure 9 for location of Drive Select and terminating jumper.
2. All components are permanently mounted on the PWA.

11.6.1.5 Termination of Write Enable

The Write Enable input line to the 9415-3 WREN is permanently terminated in a 3.9 kilohm pullup resistor isolated from the +5 V supply with a diode as well as the 150 ohm removable terminating resistor via a blocking diode (see Figure 12). This ensures that Write Enable line will not be pulled low (true) when power is lost.

11.6.2 Balanced Differential Drivers/Receivers

11.6.2.1 Transmitter Characteristics

The 9415-3 WREN uses 26LS31 type balanced differential drivers. Logic 1 on the interface is defined when the "+" output is more positive than the "-" output.

11.6.2.2 Receiver Characteristics

The 9415-3 WREN uses the 26LS32 type balanced differential receiver. Logic 1 on the interface is defined when the "+" input is more positive than the "-" input.
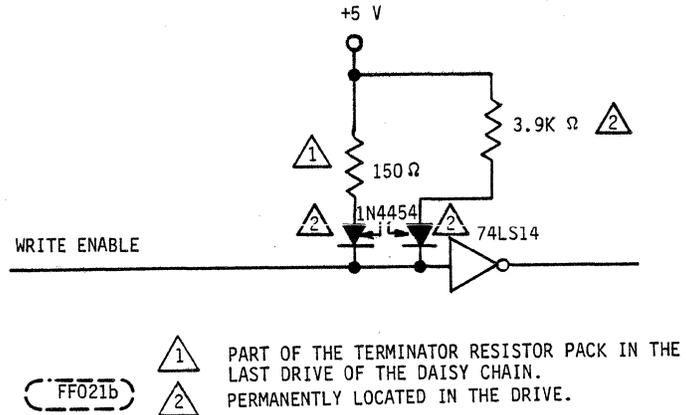
FIGURE 12. WRITE ENABLE TERMINATION

11.6.2.3 Terminator Requirements

The terminator used in the 9415-3 depends on the type of drivers and receivers being used by the controller. The 26LS31 can be terminated by two methods in the 9415-3.

Method 1 - This method of termination is used to support 26LS31/26LS32 type drivers and receivers. This is shown in Figure 13a. This method of using 26LS31/26LS32 in the Controller is recommended by CDC. The differential terminator jumpers (Figure 9) must be removed when operating in this mode.

Method 2 - This method of termination is used to support 75107/75110 type drivers and receivers. This is shown in Figure 13b. The differential terminator jumpers (Figure 9) must be installed when operating in this mode.

11.7   SIGNAL/CHASSIS GROUNDS

The WREN I Disk Drives are manufactured with the signal and chassis grounds common. Zero ohm resistors (designated W1 and W2) on the Data board allows modification of this relationship at the customer's option. The results of connecting/disconnecting the zero ohm resistors are listed in Table 3A. The customer can select any of these grounding options by removing W1 and/or W2.

TABLE 3A.

W1	W2	RESULT
X	X	Grounds common, quick connect terminal tied to common ground (as manufactured)
X	O	Grounds separate, quick connect terminal tied to chassis ground
O	X	Grounds separate, quick connect terminal tied to signal ground
O	O	Grounds separate, quick connect terminal floating

X = Connected
O = Not Connected

See Figure 12A for physical locations of W1 and W2 and Figure 12B for Schematic.

Zero ohm resistors are on the Data Boards of drives which are Series Code Four and above. The series code of the drive is indicated by the first two digits of the serial number, ie, 04000001.
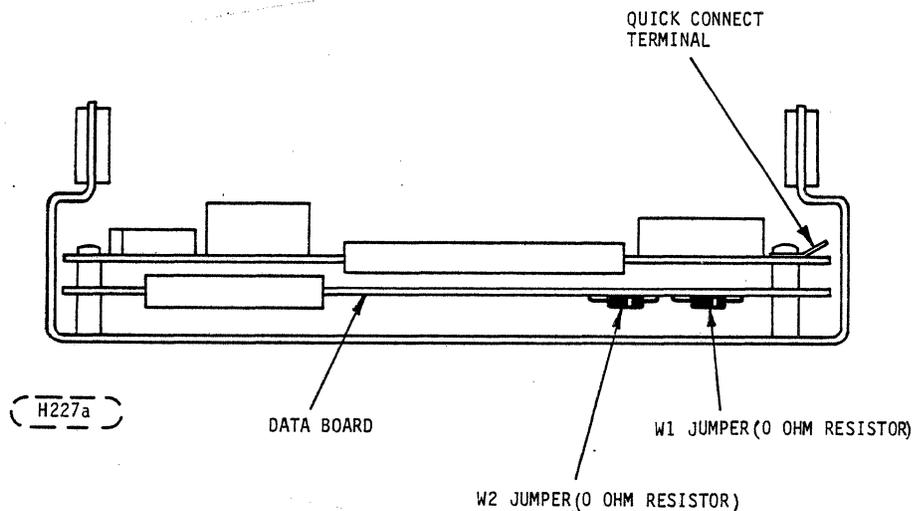
FIGURE 12A. PHYSICAL LOCATION OF W1 AND W2

QUICK CONNECT
TERMINAL

W1
JUMPER

W2
JUMPER

D.C. RETURNS

CHASSIS
GROUND
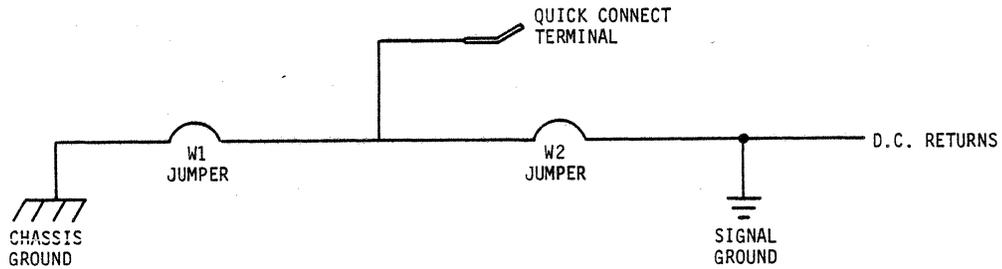
SIGNAL
GROUND

H227b

FIGURE 12B.   SCHEMATIC DIAGRAM OF W1 AND W2.

12.0   DIGITAL-INTERFACE SIGNAL DEFINITIONS

The 9415-3 WREN utilizes two digital interface cables
(Command and Data) for information transfer between it
and the controller/host system. The connector pin
assignment for the Command cable is shown in Figure 14.
The connector pin assignment for the Data cable is shown
in Figure 15. The signal direction, as well as type, is
also shown on these figures. (All single-ended signals
are true when the interface voltage level is less than
0.4 volts.)

CONTROLLER

26LS31

WRITE DATA

$\triangle$ $\triangle$

WREN

470 OHM   26LS32

470 OHM

82 OHM   82 OHM

$\triangle$

JUMPER
REMOVED

26LS32

100 OHM

READ DATA

$\triangle$ $\triangle$

47 OHM   26LS31

47 OHM

$\triangle$

|>— 20 FT. (6.10 m)—>|
MAX
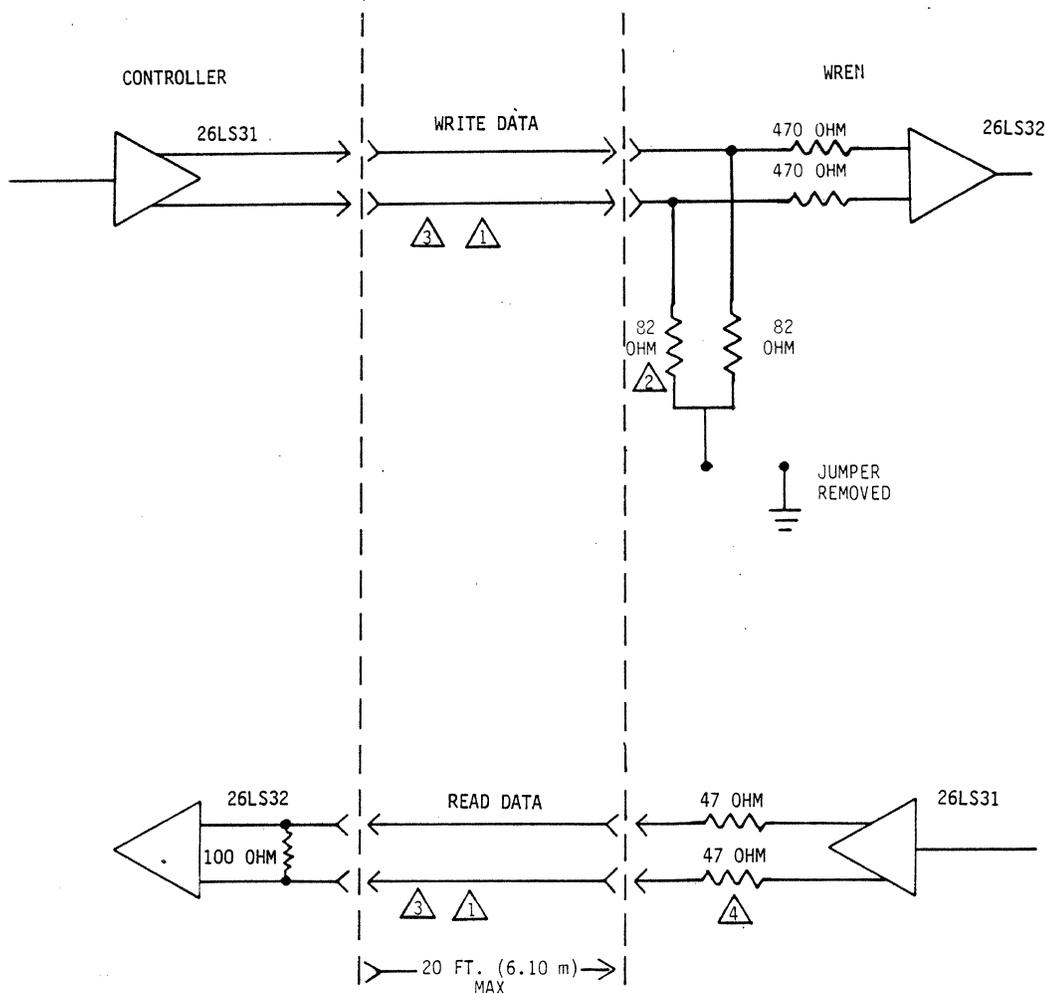
FF053

$\triangle$ CABLE SHALL BE FLAT CABLE 3M-3365-20 OR EQUIVALENT

$\triangle$ TERMINATOR RESISTORS ARE LOCATED ON DRIVE LOGIC CARD OR IN CONTROLLER.
THESE SIGNALS MUST BE RADIALLY-CABLED.

$\triangle$ NOMINAL "-" LINE

LOGIC 0   LOGIC 1

NOMINAL "+" LINE

$\triangle$ TERMINATOR RESISTORS ARE LOCATED AT ALL DRIVER OUTPUTS. THESE SIGNALS
MUST BE RADIALLY CONNECTED.

*See Figure 9 for location of differential terminator jumpers.

FIGURE 13a. METHOD 1 - BALANCED DIFFERENTIAL DRIVERS/RECEIVERS
FOR CONTROLLERS WITH 26LS31/26LS32 DEVICES

39
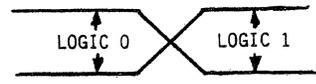
*See Figure 9 for location of differential terminator jumpers.

FIGURE 13b. METHOD 2 – BALANCED DIFFERENTIAL DRIVERS/RECEIVERS FOR CONTROLLERS WITH 75107A/75110A DEVICES

	SIGNAL PIN NO.	GROUND PIN NO.
READ ENABLE	2	1
HEAD SELECT 2^1	4	3
HEAD SELECT 2^2	6	5
INDEX	8	7
DRIVE SELECT 1	10	9
DRIVE SELECT 2	12	11
DRIVE SELECT 3	14	13
RESERVED	16	15
DIRECTION	18	17
STEP	20	19
OFFSET STROBE	22	21
WRITE ENABLE	24	23
DRIVE READY	26	25
WRITE FAULT	28	27
BYTE CLOCK	30	29
HEAD SELECT 2^0	32	31
RETURN TO ZERO	34	33

CONTROLLER/ HOST INTERFACE

COMMAND CABLE CONNECTOR
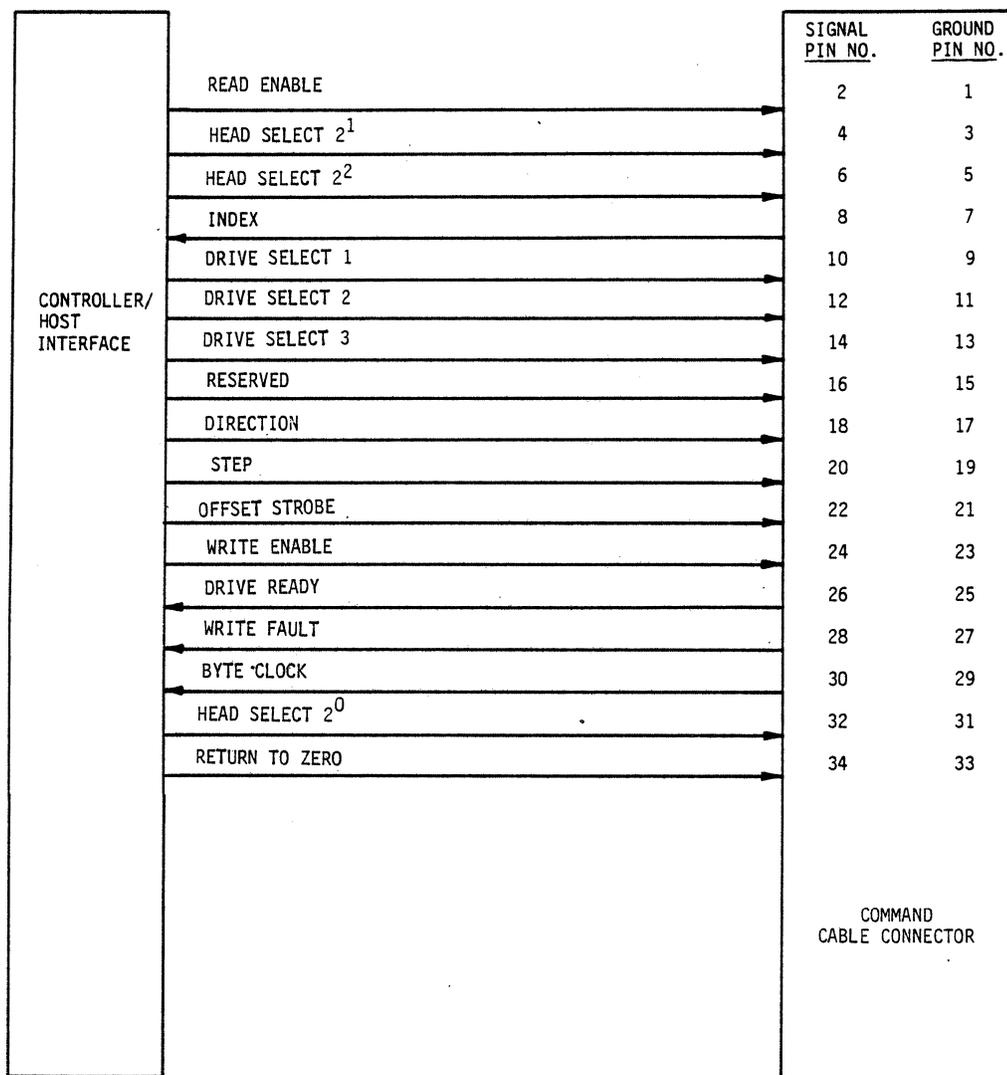
NOTE: ALL RESERVED SIGNALS TO THE WREN DRIVE SHALL BE TERMINATED IN THE WREN.
ALL SIGNALS IN THE COMMAND CABLE ARE SINGLE-ENDED SIGNALS.

GG275a

FIGURE 14. 9415-3 WREN COMMAND CABLE INTERFACE

	PIN NO.	TYPE*
INDEX	1	SE
GROUND	2	
BYTE CLOCK	3	SE
GROUND	4	
EARLY DATA STROBE ENABLE/OFFSET PLUS	5	SE
LATE DATA STROBE ENABLE/OFFSET MINUS	6	SE
UNIT READY	7	SE
GROUND	8	
WRITE DATA "+"	9	DIFF
WRITE DATA "-"	10	DIFF
GROUND	11	
WRITE CLOCK "+"	12	DIFF
WRITE CLOCK "-"	13	DIFF
GROUND	14	
SERVO/READ CLOCK "+"	15	DIFF
SERVO/READ CLOCK "-"	16	DIFF
GROUND	17	
READ DATA "+"	18	DIFF
READ DATA "-"	19	DIFF
GROUND	20	

CONTROLLER/
HOST
INTERFACE

DATA
CABLE CONNECTOR

*SE = SINGLE-ENDED SIGNAL

DIFF = DIFFERENTIAL SIGNAL

GG275b

FIGURE 15. 9415-3 WREN DATA CABLE INTERFACE

13.0   INTERFACE SIGNAL DEFINITIONS

          This section lists and defines standard input and output
          signals. All non-reserved signal leads not used by the
          controller must be either terminated or set to a logic 0
          state. Reserved interface leads are discussed in
          paragraph 13.3. All timing diagrams for single-ended
          signals are drawn with the true or logic 1 state signaled
          by the low voltage level.

          All information in this section assumes valid drive
          operating conditions have been accommodated. Refer to
          Figures 14 and 15.

13.1   INPUT SIGNAL LINES (Figures 14 and 15)

13.1.1   Drive Select -- 1-2-3

          These lines are used to activate a device's drivers and
          receivers for up to three drives in a daisychain
          operation.

                                   NOTE

                    All signals from the drive in the
                    radial data cable are available to the
                    controller regardless of the state of
                    the Drive Select lines; however, except
                    for the Host monitoring of the Index,
                    Byte Clock and Unit Ready Signals
                    contained in the radial data cable,
                    Drive Select must remain active during
                    any communication with the host
                    controller.

          Logical unit designation is accomplished at the time of
          installation by setting the Drive Select and the Drive
          Select termination jumpers located on the servo board
          assembly. (See Figure 9.)

          All command cable lines are gated with Drive Select. No
          data cable signal lines are gated with Drive Select.

          The 9415-3 WREN should not be selected until the radial
          Unit Ready signal (in the Data Cable) is a logic one after
          DC power is applied (Figure 16). The Drive Ready input (in
          the Command Cable) will be valid within 500 ns after the
          Drive is selected.

13.1.1   -Continued

The 9415-3 WREN will be selected within 1-µs after the activation of Drive Select. The 9415-3 WREN will be deselected within 1-µs after the deactivation of Drive Select (Figure 17).

Drive Select must be valid 1-µs before the first step pulse is received and 1-µs after the last step pulse is received (Figure 17).

At the completion of a write operation, Drive Select must remain active for 1-µs (Figure 18).

13.1.2   Step

This line is used in conjunction with Direction to cause head-positioner movement. Each pulse on the Step line causes the head to be moved one cylinder in the direction defined by the state of the Direction line.

Step pulses must be at least 0.5-µs at the logic 1 or logic 0 level (see Figure 17). The minimum time between Step pulses is 8-µs.

NOTE

To meet the 9415-3 WREN seek performance characteristics, the maximum time between Step pulses is 80-µs. Longer step times degrade 9415-3 WREN seek performance.

The 9415-3 WREN operates in a semi-buffered Step mode. The R/W heads will start to move when the first Step pulse is received. The rate of head movement is partially determined by the rate of the incoming Step pulses; however, the Step pulse rate may exceed the head movement rate. The Drive Ready line is used to indicate that a seek is in progress (Figure 17). The Drive Ready line will be deactivated within 100-µs after the leading edge of the first Step pulse and will be activated when the seek function is successfully completed.

13.1.2   -Continued

After the last Step pulse has been sent to the WREN the Drive Select line may be deactivated and a different drive selected. The minimum time after the last Step pulse before the Drive Select or Direction line can be deactivated is 1-µs.

The first Step pulse to initiate a seek should not be sent to the WREN unless the Drive Ready line is true.

NOTE

The drive will always attempt to maintain the heads over the recording zone of the media (i.e., at or between track 0 and maximum track) regardless of the number of Step pulses sent to the drive. Extra Step pulses which would position the heads outside of the recording zone or a hardware fault occurring within the drive such that the head was driven outside of the recording zone, will result in the head being automatically repositioned over track 0 if possible. If the head can be repositioned within the recording zone successfully, no fault will be signified and the Drive's Ready line will be activated. It is the controller's responsibility to verify the correct head position after a seek function.
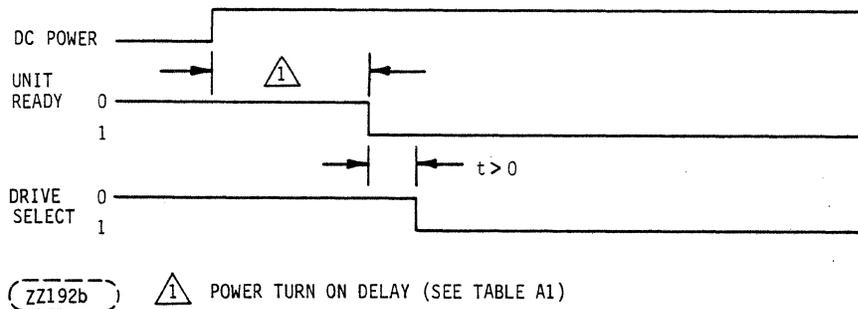
FIGURE 16. POWER TURN ON AND DRIVE SELECTION

13.1.2   –Continued

$\triangle1$ -- 9 ms FOR A SINGLE TRACK SEEK (I.E., 1 STEP PULSE).
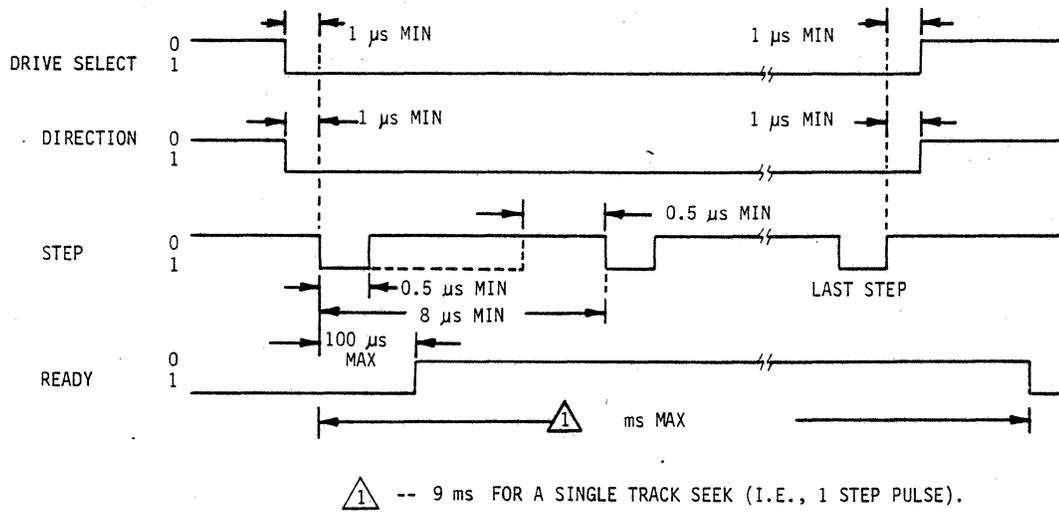
ZZ192c

FIGURE 17. TRACK-ACCESS TIMING
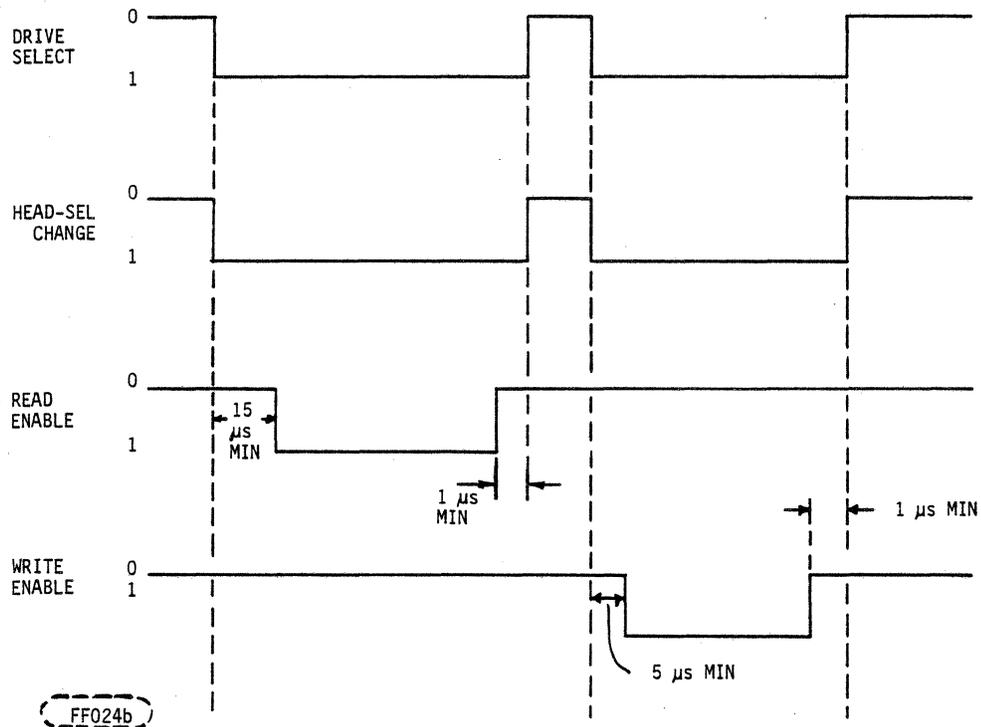
FF024b

FIGURE 18. HEAD-SELECT TIMING

13.1.2   -Continued

DRIVE SELECT

OFFSET STROBE

⚠ 1 OFFSET PLUS/EARLY

⚠ 1 OFFSET MINUS/LATE

VALID RD DATA TIME

FF026a

1 µs min

⚠ 2 OFFSET STROBE MUST NOT BE ACTIVE DURING SEEK, RTZ OR WRITE.

⚠ 1 ONLY ONE SIGNAL LINE MAYBE ACTIVATED AT A TIME.
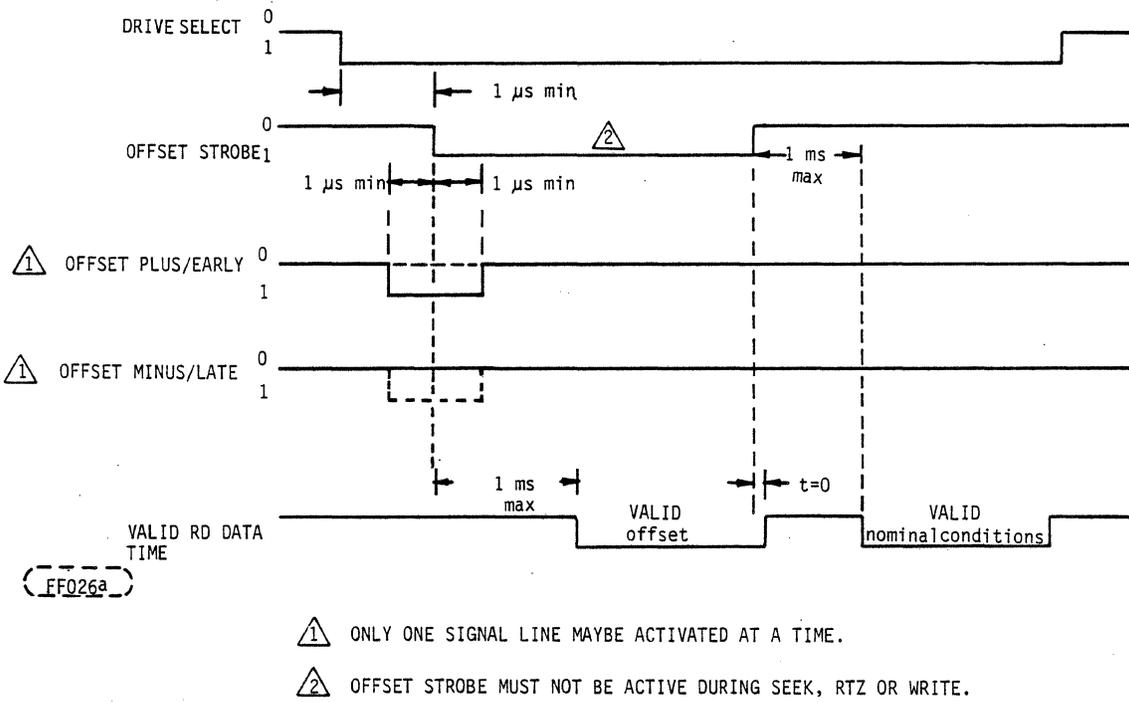
FIGURE 19a. OFFSET PLUS/MINUS TIMING

DRIVE SELECT

OFFSET STROBE

＊OFFSET PLUS/EARLY

＊OFFSET MINUS/LATE

VALID RD DATA TIME

FF026b

t = 1 µs   t = 1 µs

VALID
early or late

VALID
nominal conditions

＊ ONLY ONE SIGNAL LINE MAY BE ACTIVATED AT A TIME.
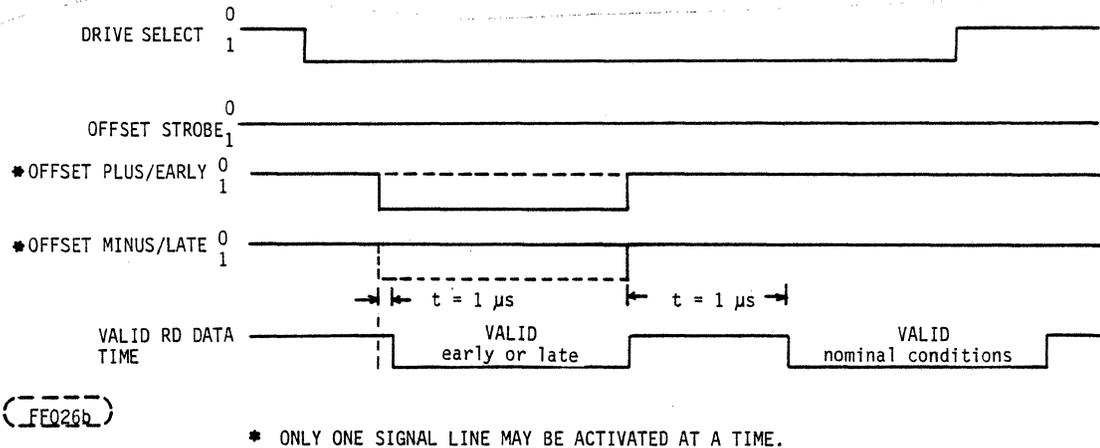
FIGURE 19b. EARLY/LATE STROBE TIMING

47

13.1.2   -Continued

OFFSET STROBE MUST BE DEACTIVATED 1 μs   PRIOR TO UNIT DESELECTION.

OFFSET STROBE NOT ALLOWED DURING SEEK, RTZ OR WRITE.

ONLY ONE SIGNAL LINE MAY BE ACTIVATED AT A TIME.
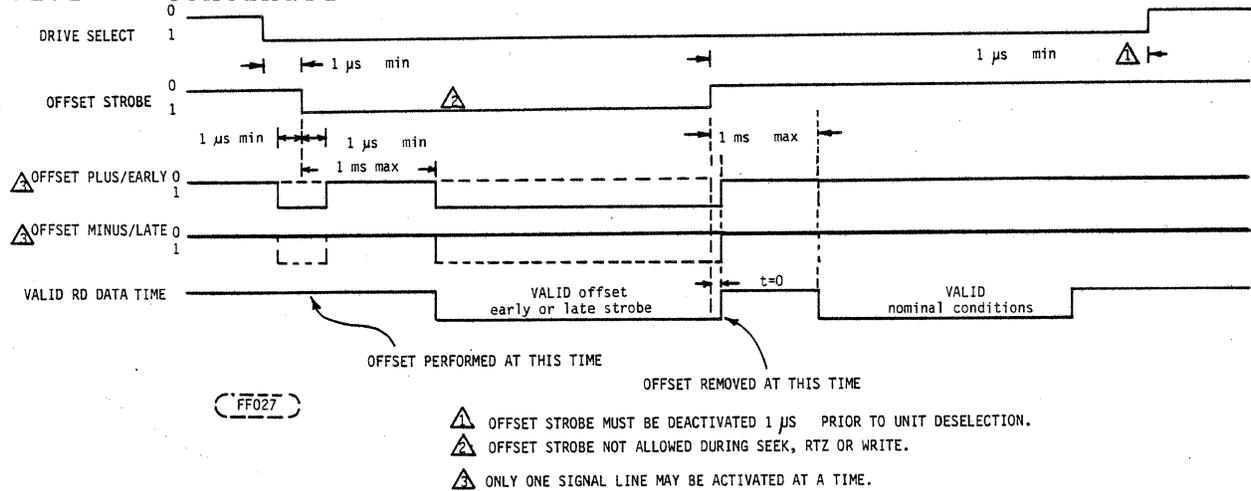
FIGURE 19c. OFFSET PLUS/MINUS, EARLY/LATE STROBE TIMING

13.1.3   Direction

The state of this line determines the direction of movement of the head carriage. A logic 1 on this line signifies head-carriage movement is to be toward the higher-numbered cylinders. A logic 0 on this line signifies head-carriage movement toward the low-numbered cylinders, i.e., toward track 0. Track 0 is located on the outer radius of the disk.

Direction must be stable a minimum of 1-μs before each Step pulse and 1-μs after the last Step pulse (see Figure 17).

13.1.4   Head Select 2^0, 2^1, 2^2

These lines are used to select the proper media and head for data transfer per Table 4.

TABLE 4. HEAD-SELECT ENCODING

Head Select			Head No.	Media Selected
2^2	2^1	2^0		
1	1	1	Invalid Head Select	----
1	1	0	Invalid Head Select	----
1	0	1	Invalid Head Select	----
1	0	0	4 Top Head	Top Media
0	1	1	3 Bottom Head	Top Media
0	1	0	2 Top Head	Middle Media
0	0	1	1 Bottom Head	Middle Media
0	0	0	0 Top Head	Bottom Media

13.1.4   -Continued

Head selection may be changed at any time following activation of Drive Select, but must occur a minimum of 15-μs prior to a read operation (Figure 18) or 5-μs prior to a write operation. Read Enable or Write Enable must be deactivated a minimum of 1-μs prior to a head change.

The Drive Ready line will not change as a result of head change.

13.1.5   Offset Strobe

This line is used to initiate an actuator offset from the nominal On Cylinder position. The offset function is intended to be used to aid in the recovery of marginal data which has been previously recorded on the disk media and should only be utilized after rereads without actuator offset have been attempted. The leading edge of offset strobe will initiate an actuator offset movement in the direction specified by the Offset Plus or Offset Minus leads (Section 13.1.11 and Section 13.1.12).

Offset Strobe must remain activated as long as the actuator offset is desired. The trailing edge of Offset Strobe will initiate an actuator movement back towards the normal On Cylinder position (see Figure 19a, b, and c). When the state of Offset Strobe is changed (i.e., either leading or trailing edge), a one millisecond delay is required before a read or write operation is initiated. When in the offset mode (Offset Strobe active), no write data operation or seek operation should be attempted. If Write Gate is activated while in the offset mode, the Write Fault line (Section 13.2.4) will be activated. Offset Strobe must be false for up to 1 microsecond after a Drive Select sequence and must be deactivated 1 microsecond prior to a unit deselection sequence.

NOTE

The Drive Ready lead will not be deactivated as a result of an offset function. No seek function (i.e. either by STEP PULSES or the RTZ function) should be initiated while in the offset mode.

13.1.6   Return to Zero (RTZ)

This line is used to cause the actuator to return to
track zero and to reset the write fault latch if the
fault no longer exists. The Return to Zero function is
longer than a seek to track zero and should normally be
used for recalibration or to reset the write fault latch.

The RTZ function will be initiated by a logic 1 pulse
(0.5 to 25-µs). The Ready signals will be deactivated
within 100-µs after reception of an RTZ command. The
successful completion of an RTZ will be signified by the
activation of the Ready signals. The maximum time to
complete a RTZ function is 200 milliseconds.

13.1.7   Read Enable

Activation (logic 1) of the Read Enable signal enables
digital read data on the Read Data lines and enables Read
Clock on the Servo/Read clock lines. The leading edge of
Read Enable triggers the read chain to synchronize the
internal phase-locked oscillator to a media-recording PLO
synchronization field (refer to Section 15.0).

13.1.8   Write Enable

Activation (logic 1) of the Write Enable signal enables
the write driver and initiates recording of the contents
of the Write Data lines onto the media. (Refer to Section
15.0 for timing.)

13.1.9   Write Data "+" and "-"

Data to be recorded on the media is supplied on these
balanced differential lines. These lines carry NRZ data
which is in phase sync with the Write Clock lines. (See
Figure 20.)

13.1.10   Write Clock "+" and "-"

These lines carry the balanced differential Write Clock
signal which must be synchronized with the NRZ Write Data
as illustrated in Figure 20. The Write Clock is the Servo
Clock retransmitted to the drive during a Write
operation. The Write Clock need not be retransmitted
continuously but must be transmitted at least 2-1/2 servo
clock periods prior to Write Enable.

13.1.11   Early Data Strobe Enable/Offset Plus

This line, when used in conjunction with the Offset Strobe Signal can be used to obtain three combinations of Plus Offset, Early Data Strobe Enable or both during a Read Operation.

When this line is true in conjunction with Offset Strobe, an actuator offset from the normal On Cylinder Position towards the higher numbered cylinder addresses is generated.

This line must be activated a minimum of 1 microsecond before the activation of Offset Strobe and remain true for at least 1 microsecond after the activation of Offset Strobe. Offset Strobe must be held true during the entire read operation to maintain the actuator in the offset mode.

For Offset Plus mode only the Early Data Strobe/Plus Offset line must be deactivated prior to Read Enable (Figure 19a).

If only Early Data Strobing is required, activation of this line during a Read Operation is necessary (Figure 19b) without activating Offset Strobe. If the Early Data Strobe Enable and Plus Offset is desired, this line is activated 1-us before Offset Strobe and also activated for the entire Read Operation.

The Device PLO Data Separator will Strobe Data at a time earlier than nominal along with the Plus Offset (Figure 19c).

13.1.12   Late Data Strobe Enable/Offset Minus

This line, when used in conjunction with the Offset Strobe Signal can be used to obtain these combinations of Minus Offset, Late Data Strobe Enable or both during a Read Operation.

When this line is true in conjunction with Offset Strobe an actuator offset from the normal On Cylinder Position towards the lower numbered cylinder addresses is generated.

13.1.12   -Continued

This line must be activated a minimum of 1 microsecond before the activation of Offset Strobe and remain true at least 1 microsecond after the activation of Offset Strobe. Offset Strobe must be held true during the entire read operation to maintain the actuator in the offset mode.

For Offset Minus mode only Late Data Strobe/Minus Offset must be deactivated prior to Read Enable (Figure 19a).

If only Late Data Strobing is required, activation of this line during a Read Operation is necessary (Figure 19b).

If Late Data Strobe Enable and Minus Offset is desired, this line is activated 1-μs before Offset Strobe and also activated during the Read Operation. The Device PLO Data Separator will Strobe Data at a time later than nominal along with the Minus Offset (Figure 19c).

13.2   OUTPUT SIGNAL LINES

13.2.1   Drive Ready (Daisychained Signal -- See Figure 14)

A logic 1 on this line indicates that the disk is up-to-speed and the drive is on cylinder and not executing a seek function. This line is gated with Drive Select. This signal is also available in the data cable not gated with Drive Select and is referred to as Unit Ready. The Drive Ready signal will be valid within 500 nanoseconds after the appropriate Drive Select is activated. This line will not be deactivated when an offset function is initiated.

FIGURE 20. NRZ DATA AND CLOCK TIMING
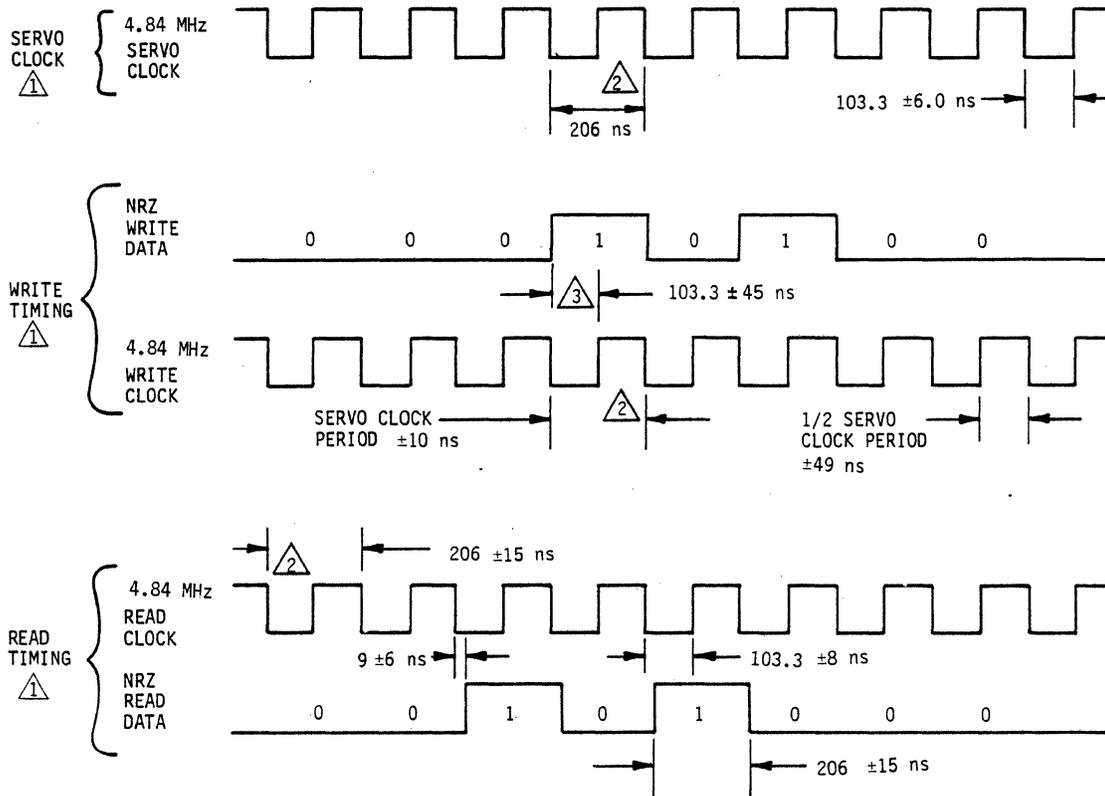
NOTES

1 ALL TIMES IN NANOSECONDS MEASURED AT DRIVE I/O CONNECTOR

2 SIMILAR PERIOD SYMMETRY SHALL BE ± 3 ns BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.

3 THIS TIME (103.3 ± 45 ns) IS MEASURED FROM THE ACTIVATION (OR DEACTIVATION) OF THE NRZ WRITE DATA LINE AND RISING EDGE OF THE WRITE CLOCK LINE.

ALL CLOCK TIMES ARE NOMINAL. A COMBINED SPINDLE SPEED AND CLOCK CIRCUIT TIMING TOLERANCE NOT EXCEEDING 3.0% MUST BE TAKEN INTO ACCOUNT.

SERVO CLOCKS ARE VALID WHEN NOT READING. OTHER TIMING IS APPLICABLE DURING READING OR WRITING.

13.2.2   Index

This signal occurs once per revolution and its function is to indicate the physical beginning of the track. The Index pulse width is 1.65-μs nominal. (See Figure 21.)

This signal in the command cable is gated with Drive Select and is also available in the data cable not gated with Drive Select.

T1 = 0.2 μs to 0.41 μs
T2 = 0.41 μs to 0.53 μs
T3 = 0.83 μs
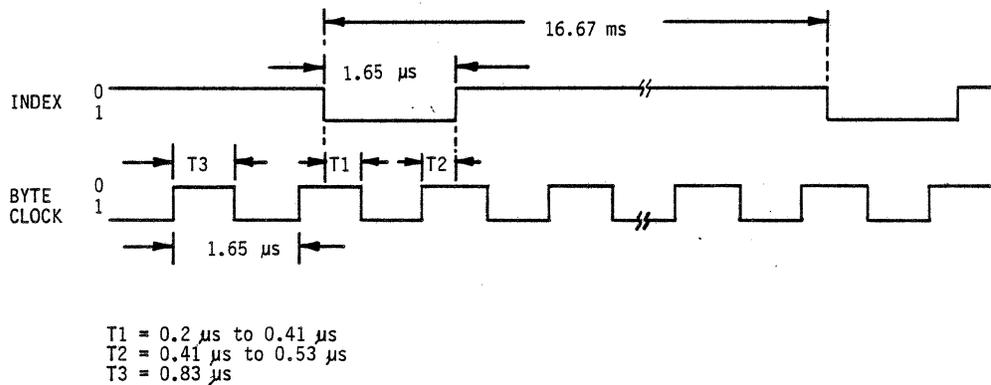
NOTE: TIMING IS NOMINAL AND MAY VARY BY ±3.0%

ZZ092b

FIGURE 21. INDEX AND BYTE CLOCK RELATIONSHIP

13.2.3   Byte Clock

This signal occurs once per every eight Servo Clock periods. There are 10,080 Byte Clocks per disk revolution at a 605 kHz nominal rate. This signal is provided for the controller to count the desired number of Byte Clocks to determine the sector size and beginning sector locations. The inter-relationship of Index and Byte Clock is shown in Figure 21. This signal is continuously transmitted if the medium is up to speed and the heads are positioned over the recording zone of the medium. This clock does not have a fixed phase relationship to the recorded data. This signal gated with Drive Select is contained in the Command cable; it is also available not gated with Drive Select in the Data cable.

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13.2.4   Write Fault

Write Fault conditions detected by the WREN will activate
the Write Fault signal. The Write Fault signal will
remain activated until it is deactivated by the Return to
Zero signal or by power sequencing the WREN. The Write
Fault signal will be deactivated within 0.5-μs from the
leading edge of the Return to Zero signal. Writing of the
disk media will be inhibited if Write Fault is active.

A Write Fault condition will occur if Write Enable is
true and either:

a. Write current is absent; or
b. Write data is absent; or
c. The drive is not ready; or
d. Invalid head or internal multiple heads are selected;
   or
e. Read Enable is true; or
f. Offset Strobe is true.

A Write Fault condition will also occur if Write Enable
is false and write current is present.

13.2.5   Unit Ready

Same as Drive Ready but contained in the Data Cable and
not gated with Drive Select. See Section 14.2.1.

13.2.6   Servo/Read Clock "+" and "-"

These balanced differential lines contain the drive
generated Read Clocks if the Read Enable signal is true,
or the drive-generated Servo Clocks if the Read Enable
signal is false. This signal is located in the Data cable
and is not gated with Drive Select.

The Read Clock defines the beginning of a data cell.
Whenever it is valid it is in phase and frequency
synchronization with the Read Data as specified in Figure
20. The Read clocks will be valid within 88 Read Clock
periods from the concurrence of Read Enable and a PLO
synchronization field (refer to Section 14 for detailed
interface timing).

13.2.6   -Continued

The Servo Clock is an internally generated phase-locked clock (4.84 MHz nominal) which is used by the controller to generate Write Clock (see Figure 20). This clock is phase and frequency locked to the disk rotational speed. Servo Clocks will be valid within two Servo Clock periods after the termination of Read.

NOTE

Phase/Frequency discontinuities may exist, by no clock transitions, in the Servo/Read Clock signal when the Read Enable signal is switched between the True and False conditions (see Figure 25).

13.2.7   Read Data "+" and "-"

These balanced differential lines transmit the recovered media data in the NRZ form from the WREN to the controller. This data is in frequency and phase synchronization with the Read Clocks as specified in Figure 20. The Read Data signal is valid within 88 Read Clock periods from the concurrence of Read Enable and the PLO synchronization field. Refer to Figure 22 for detailed timing and Section 14.0 for recommended format timings. The Read Data lines are located in the data cables and will be a logic zero until PLO synchronization is established with a Read function.
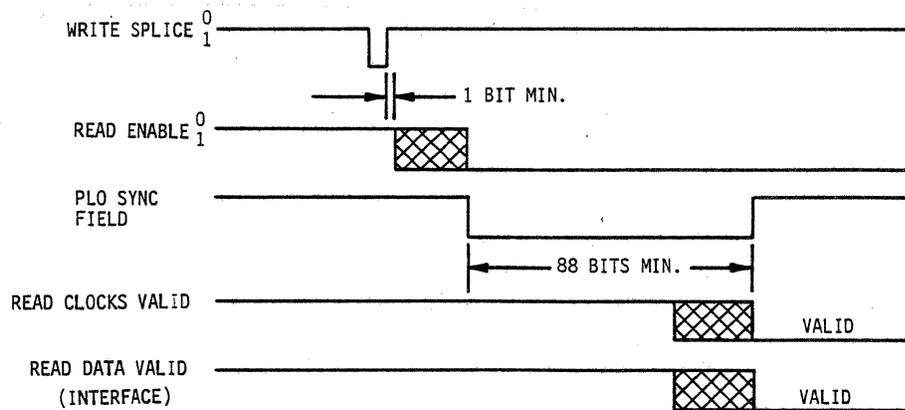
READ ENABLE MUST BE DEACTIVATED PRIOR TO THE WRITE SPLICE. READ ENABLE MAY BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF PLO SYNC REMAINING IN THE SYNC FIELD.

FIGURE 22. READ TIMING

13.3   RESERVED SIGNAL LINES

Command cable pin 16 - This signal line is used for Motor On in the 5-1/4 FDD.

14.0   DATA FORMAT AND DATA CONTROL TIMING

14.1   FORMAT DEFINITION (Hard Sector)

The record format on the disk is under control of the controller. The Index pulse and Byte Clocks are available for use by the controller to indicate the beginning of a track and allow the controller to define the beginning of a sector. A suggested format for fixed data records is shown in Figure 23.

The format presented in Figure 23 consists of three functional areas: Intersector Gap, Address and Data. The Data area is used to record the system's data files. The Address area is used to locate and verify the track and sector location on the Disk where the Data areas are to be recorded. This section refers to a Sector pulse which is generated internal to the controller from the Byte Clock to ease the format description.

14.1.1   Intersector Gap (ISG)

The Intersector Gap is 16 bytes long and is oriented to begin four bytes before a Sector (Index) pulse and 12 bytes after a Sector (Index) pulse. This gap size was chosen for the following reasons:

a. It satisfies the drive-required write-to-read recovery time (i.e., minimum time between the deactivation of Write Enable to the activation of Read Enable);
b. It allows the head to be switched during an ISG and the header of the sector following this ISG to be read without incurring a rotational latency;
c. It allows for controller decision making time between sectors.

14.1.2   Address Area (Figure 23)

The address area provides a positive indication of the track and sector locations. The address area is normally read by the controller and the address bytes verified prior to a data area read or write. The address area is normally only written by the controller during a format function (Section 14.2) and thereafter only read to provide a positive indication of the sector location and establish the boundaries of the data area. The address area consists of the following bytes.

a. PLO Sync (11 bytes minimum)

These 11 bytes of zeros are required by the drive to allow the drive's read data phase-locked oscillator to become phase and frequency synchronized with the data bits recorded on the media.

b. Byte Sync Pattern (one byte)

This byte establishes byte synchronization (i.e. the ability to partition this ensuing serial bit stream into meaningful information groupings, such as bytes) and indicates to the controller the beginning of the address field information. It is recommended that the Byte Sync Pattern contain more than a single one bit for a greater confidence level of detection.

c. Address Field

These bytes are user-defined and interpreted by the user's controller. A suggested format consists of five bytes, which allows one byte to define flag status bits or logical unit number, two bytes to define the cylinder address, one byte to define the head address and one byte to define the sector address.

d. ADR CRC (two bytes recommended) -
       (Address Field Check Codes)

Selection of an appropriate error-detection mechanism, such as a cyclic redundancy check (CRC) code, is generated by the controller and applied to the address for file-integrity purposes. These codes are generated by the controller and written on the media during formatting. Data integrity is maintained by the controller recalculating and verifying the address field check codes when the address field is read.

14.1.2   -Continued

    e. ADR Pad (one byte) - (Address Field Pad)

       The Address Field Pad byte must be written by the
       controller and is required by the drive to ensure
       proper recording and recovery of the last bits of the
       address-field check codes.

14.1.3   Data Area (Figure 23)

    The Data Area is used to record data fields. The contents
    of the data fields within the Data Area are specified by
    the host system.

    The remaining parts of the Data Area are specified and
    interpreted by the disk controller to recover the data
    fields and ensure their integrity. The Data Area consists
    of:

    a. Write Splice (one byte)

       This byte area is required by the drive to allow time
       for the write drivers to turn on and reach a recording
       amplitude sufficient to ensure data recovery. This
       byte should be allowed for in the format and is
       described in greater detail in Section 14.3.

    b. PLO Sync (11 bytes)

       These 11 bytes of zeros are required when reading to
       allow the drive's phase-locked oscillator to become
       phase and frequency synchronized with the data bits
       recorded on the media.

    c. Byte Sync Pattern (one byte)

       This byte establishes byte synchronization and
       indicates, to the controller, the beginning of the
       data field. It is recommended that this byte contain
       more than a single one bit.

    d. Data Field

       The data field contains the host system's data files.

14.1.3   -Continued

e. Data CRC (two bytes) - (Data-Field Check Codes)

The CRC bytes are generated by the controller and written on the media with the Data Field. Data integrity is maintained by the controller recalculating and verifying the Data Field Check Codes when the Data Field is read.

f. Data Pad (one byte) - (Data Field Pad)

The Data Field Pad byte must be issued by the controller and is required by the drive to ensure proper recording and recovery of the last bits of the data field check codes.

INDEX/SECTOR   FIXED SECTOR: "N" IDENTICAL SECTORS   SECTOR
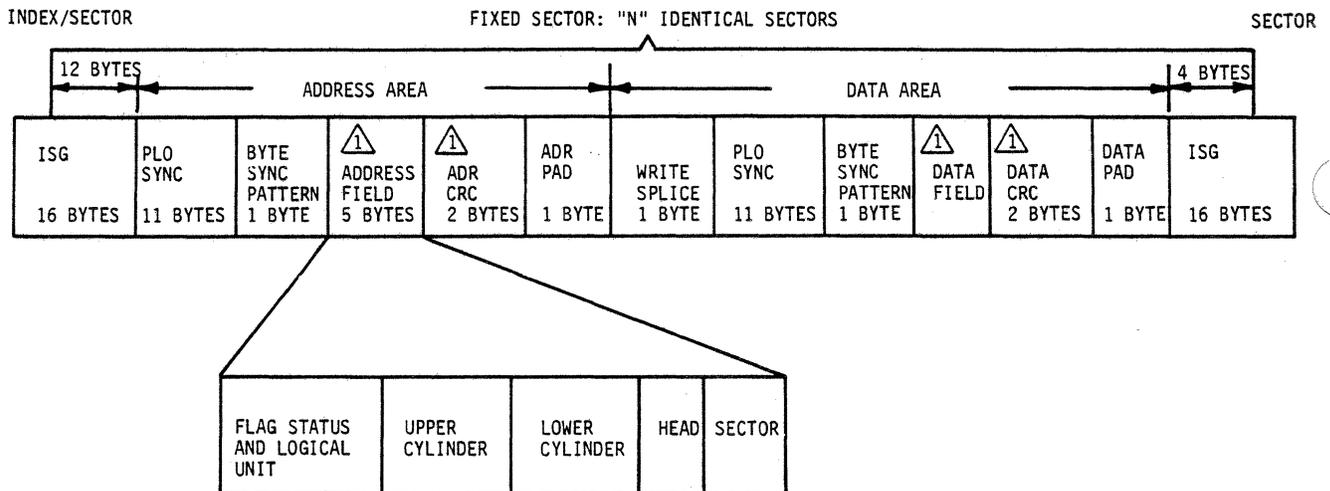
⚠️1   THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

(G042a)

FIGURE 23. SECTOR FORMAT

14.2   WRITE-FORMAT PROCEDURE

Provisions must be made within the controller to format the disk. The following procedure is recommended for fixed-sector formats with separate address and data fields. This procedure is based on formatting from "Index to Index".

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14.2   -Continued

Procedure (Refer to Figure 23)

1. Select the desired unit, cylinder and head.

<div align="center">NOTE</div>

> The controller must wait for Ready to
> begin a search for the leading edge of
> Index. If only a head change was
> affected the controller must provide a
> 5-μs minimum delay before Write Enable
> may be activated.

2. Search for the leading edge of Index and when
   detected, activate Write Enable.

3. Write 12 bytes of zeros for the ISG following the
   Index/Sector pulse.

4. Write 11 bytes of zeros for the Address field PLO sync
   area.

5. Write a byte sync pattern, the address field, the
   address field check bytes (2).

6. Write all zeros for the address pad byte, the write
   splice byte and 11 bytes of the data area PLO sync.

7. Write the data area byte sync byte, the data field,
   two data field check bytes and the data pad byte.

8. Write four bytes of zeros for the ISG preceding the
   sector pulse.

9. If the next sector of the same track is to be
   formatted and the head is not deselected, Write Enable
   should remain true, while writing zeros until the
   leading edge of the sector pulse is detected and the
   format procedure then repeated starting at Step 3. If
   the last sector of the track was just formatted, zeros
   should be written until the Index pulse is again
   detected, then Write Enable should be deactivated ;
   and then proceed to Step 1.

14.2   -Continued

NOTE

Write Enable must be deactivated at
least 1-μs before a head change can be
initiated, and Write Enable may not be
activated until 5-μs after a head
change, thus it may be desired to
affect the head change prior to the
Index pulse according to the format
chosen.

14.3   READ/WRITE CONTROL TIMING (See Figure 24)

The objective of this section is to specify the
interrelationship of the drive interface control lines
necessary to recover or record data fields on a formatted
disk media. The format of Section 14.1 will be assumed;
however, critical drive-dependent parameters will be
summarized to enable controller variations in the read/
write timing.

To perform a data-field read function, the address field
is read and verified, then its data field is read. To
perform a data-field write function, the address field is
read and verified, then the data area is written. The
following sections will expand on these concepts.

14.3.1   Read Function

The read function consists of reading the address fields
and then the data fields. The critical interface lines
associated with a read function are the Index, Byte Clock
(to generate sector), Read Enable, Read Data, and Read
Clock lines.

● Address-Field Read (See Figure 24 and 25)

The location of the address field is defined relative
to the Sector (Index) pulse. To recover the address
field, the controller waits for the leading edge of a
Sector (or Index) pulse; 80 ±4 servo clock periods
after the leading edge of a sector (or Index) pulse,
Read Enable may be activated. The leading edge of Read
Enable forces the phase-locked oscillator to
synchronize on the PLO sync field. Read Enable also
enables the read output of the data separator after
frequency and phase synchronization is established.

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14.3.1   -Continued

Read   Clocks   will   be   in   phase   and   frequency
synchronization with the Read Data within 88 Servo
Clock periods after the concurrence of Read Enable and
the PLO Sync field. The Read Data lines will be a
logic zero until the first one bit of the byte sync
pattern is detected. The controller then establishes
byte   synchronization,   performs   the   Address   Field
verification and interprets the address field check
codes (CRC). Read Enable may be deactivated after the
last bit of the address field check code is received
by the controller and must be deactivated at least one
bit prior to a Write Splice area.

For example, consider the data field read function
shown in Figure 24. This example has a Write Splice
area located on the disk one byte after the address
field check codes (the creation of this Write Splice
area   will   be   explained   in   Section   14.3.2).   An
examination of the interface Data (Read) timing signal
of Figures 24 and 25 reveals that the Interface Read
Data is delayed by three bit times from data recorded
on the media. Thus, to meet the requirement that Read
Enable must be deactivated at least one bit prior to a
Write Splice area, requires that, for the format of
Figure 24, Read Enable be deactivated within four bit
times after the reception of the last bit of the
address-field check code by the controller.

The controller may compare the contents of the disk
media-recorded address field to the desired sector
location as they are received from the drive. However,
a valid comparison should not be assumed until the
disk media-recorded CRC check code verifies its
correctness.   If   the   recorded   and   desired   address
fields compare and no check-code error is detected,
then the desired Data Area for either a data-field
update or data-field read function has been found.

14.3.1   -Continued

- Data-Field Read (See Figures 24 and 25)

   After the desired sector location has been found by comparison of the address field, the data field may be read. When a data field is updated, a three-bit-wide Write Splice area is created on the media (see Section 14.3.2). Read Enable must be deactivated a minimum of one bit time preceding a Write Splice area and may be activated a minimum of one bit after a Write Splice area. For example, consider the format of Figure 25. To satisfy the Read Enable/Write Splice timing requirements, Read Enable could be deactivated as soon as the last bit of the Address Field check code was received by the controller and activated 11 Servo/Read Clock periods later. The example chose to deactivate Read Enable as soon as the last bit of the address field check code was received (versus deactivating Read Enable four bit times after the last bit of the address-field check code) for timing compatibility with the data-field update function (Section 14.3.2) which assumed this timing relationship to enable Write Gate and create the Write Splice area in the location shown in Figure 24 and 25. The example also chose to activate Read Enable by counting 11 Servo/Read Clock periods because the 11 Servo/Read Clock periods guarantees that 11 PLO sync bytes will be seen for read PLO synchronization, and it guarantees that the Read Enable signal will be enabled at least one bit past the write splice. This counting of 11 Servo/Read Clock periods to reactivate Read Enable also allows the Write Splice to be shifted two bit positions to the right of Bit 1 of the Address Pad and still guarantees that in the worst case, Read Enable was not activated until one bit time after a shifted write splice. This shifted write splice could occur if the controller counted five Interface Servo/Read Clock periods between the deactivation of Read Enable and the activation of Write Enable due to the one-half bit minimum of two bits maximum period of no Interface Servo/Read Clocks when Read Enable is deactivated.

14.3.1   -Continued

Per Figure 24, if Read Enable is activated after the
Write Splice and at the beginning of the Data Field
PLO Sync area, the Interface Read Data lines will be
valid within 88 servo clock periods. When Read Enable
is activated, the Interface Servo/Read Clock line will
switch from servo clocks to read clocks within two bit
times. This transition area will contain no shortened
pulse width but may contain no clocks for up to two
clock periods.

Thus within 88 servo clock periods from the start of a
PLO sync field the controller may search for the Data
field   byte   sync   pattern,   establish   byte
synchronization, and read the Data field plus read and
interpret the Data field check codes. Read Enable may
be deactivated after the last bit of the Data field
check code (Data CRC) is received.

● Summary of Critical Read-Function Timing Parameters

Controller variations of the read timing are allowed
if the following drive-dependent parameters are met:

a. Read Initialization Time

A read operation may not be initiated until 15-μs
following a head change.

b. Read-Enable Timing

Requesting   the   drive   to   establish   bit
synchronization (i.e., enabling Read Enable) for
the address area should be done no earlier than 80
±4 bits from the leading edge of a Sector (Index)
pulse and at least 11 bytes prior to the address
field byte sync pattern.

Read Gate may not be enabled or true during a Write
Splice area (Read Gate must be deactivated one bit
time minimum before a Write Splice area and may be
enabled one bit time minimum after a Write Splice
area.)

NOTE
Data (Read) at the Interface is delayed
by three bit times from the data
recorded on the disk media.

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14.3.1   -Continued

c. Read Clock Timing

Read Clock and Read Data are valid within 11 bytes after Read Enable and a PLO sync field.

d. The Interface Servo/Read Clock line may contain no transitions for up two Servo Clock periods for transitions between servo and read clocks. The transition period will also be one-half of a Servo Clock period minimum with no shortened pulse widths.

14.3.2   Write Function (Figure 24 and 25)

The Write function consists of reading the address field to verify the sector location, and then writing the Data Area PLO Sync characters, the Byte Sync pattern, the Data Field, the Data Field Check Codes (CRC) and a Data Field Pad byte. The critical interface lines associated with the write function are the Write Enable, Write Data, Write Clock and Servo/Read Clock lines.

● Read-Address Field Prior to Write

The address field and address field check codes should be read and verified prior to writing the data area except while formatting.

● Write-Splice Creation

A write-splice area is created on the disk media when the Write Enable signal is either activated or deactivated. A write splice three Servo Clock periods wide is created due to write-driver turn-on time plus data-encoder turn-on delays. The example of Figure 24 shows a write-splice area located between the address field and the data field. The creation of this write-splice area will now be explained in detail.

The write-splice area shown in Figures 24 and 25 was created at a location relative to the address field. Its location is defined by the following drive parameters:

a. Interface Data (Read) is delayed by three bit times from data recorded on the media.

14.3.2   -Continued

    b. Write Clocks must precede Write Enable by a minimum
       of two and a half servo clock periods.

    c. Servo clocks (used by the controller to create
       Write Clocks) may not be valid on the Servo/Read
       Clock lines until two servo clock periods after
       Read Enable is deactivated.

    d. Read Enable and Write Enable may not occur
       simultaneously.

Thus, from Figure 24 and 25, if Read Enable was
deactivated when the last interface data bit of the
address field check code was received by the controller
and Write Enable was activated five Servo Clock periods
after Read Enable was deactivated, a Write Splice area
would be created at the location shown in Figures 24 and
25 (i.e., the Write Splice area on the media would start
eight bit times from the last bit of the recorded address
field check code). In addition, if Write Clocks were
enabled two Servo clock periods after Read Enable was
deactivated, the drive requirement for Write Clocks to
precede Write Gate by two and a half Servo Clock periods
would also be met.

                              NOTE

        If   the   clocks   available   on   the
        Interface Servo/Read Clock lines are
        used to count five servo clock periods
        from the deactivation of Read Enable to
        the activation of Write Enable, the
        Write splice may be shifted two bit
        positions to the right of the first bit
        of the address pad because the
        Interface Servo/Read Clock line may
        contain no clock transitions for up to
        two servo clock periods after Read
        Enable is deactivated.

Since the write-driver turn-on plus data-encoder turn-on
delay is three Servo Clock periods maximum from the
leading edge of Write Enable, the width of the Write
Splice area recorded on the disk media will be three
Servo Clock periods maximum.

14.3.2   -Continued

- PLO Sync-Field Write

  The PLO Sync Field must consist of a minimum of 11 valid and recoverable bytes of interface data zeros. From Figure 24, a five-bit pad area is shown between the three-bit splice area and the start of the data field PLO sync. This five-bit pad area allows Read Enable to be activated one bit minimum after a Write Splice and be valid at the Drive Interface prior to the Data Field PLO sync bytes.

  Thus to guarantee writing 11 valid bytes of PLO Sync characters, allow for the Write Splice area, and allow Read Enable to be activated one bit time after a Write Splice but prior to an 11-byte PLO Sync Field, it is recommended that the controller transmit 12 bytes of zeros after Write Enable is activated.

- Byte-Sync, Data-Field, Data-CRC and Data-Pad Write

  After the Data Field PLO sync field is written, a Byte Sync character should be written to enable the controller to establish byte synchronization for the data field.

  After the Data Field is written, the Data Field check codes should be written followed by one Data Pad byte at the end of the check field to ensure proper recording and recovery of the check field codes.

  After the Data Pad byte is written, the Write Enable should be deactivated and Read Enable should not be activated to read the address Area of the next sector until 80 $\pm$4 Servo clock periods after the next Sector pulse is detected. This will allow ample time for the write-to-read recovery time (i.e., the 10-μs minimum between the trailing edge of Write Enable and the leading edge of Read Enable).

  NOTE

  With the four bytes of ISG preceding the Index/Sector pulse, a head change can be made after a sector update and read the next sequential header of the new track.

14.3.2   -Continued

- Summary of Critical Write-Function Parameters

  Controller timing variations in the record-update function are allowed if the following drive-dependent write (and interrelated read) timing parameters are met:

  1. Read-to-Write Recovery Time

     Assuming head selection is stabilized, the time lapse from deactivating Read Enable to activating Write Enable shall be five Servo Clock periods minimum.

  2. Write Clock-to-Write Enable Timing

     Write Clocks must precede Write Enable by a minimum of two and a half Servo clock periods.

  3. Write Driver Plus Data-Encoder Turn-On from Write Enable

     The write driver plus data-encoder turn-on time (write splice width) is three Servo Clock periods maximum.

  4. Write-Driver Turn-Off from Write Enable

     To account for data-encoding delays. Write Enable must be held on for at least one byte time after the last bit of the information to be recorded. (Refer to "Data Pad" in Figure 24.)

  5. Write-to-Read Recovery Time

     The time lapse before Read Enable can be activated after deactivating the Write Enable is 10-µs.

  6. Head Switching Time

     Write Enable must be deactivated at least 1-µs before a head change.

     Write Enable may not be activated until 5-µs after a head change command is received by the Drive.

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14.3.2   –Continued

7. Servo Clocks Valid Time

The Servo/Read Clock lines will contain valid Servo Clocks within two Servo Clock periods after the deactivation of Read Enable. Pulse widths will not be shortened during this transition time but clock transitions may not occur for up to two servo clock periods.

8. Read Clocks Valid Time

The Servo/Read Clock lines will contain valid Read clocks within two Servo Clock periods after PLO synchronization is established. Pulse widths will not be shortened during this transition time, but missing clocks may occur for up to two clock periods.

9. Write Propagation Delay

Write Data received at the I/O connector will be delayed by the Write Data Encoder by 4 BIT Times maximum prior to being recorded on the media.

FIGURE 24. TYPICAL READ/WRITE TIMING
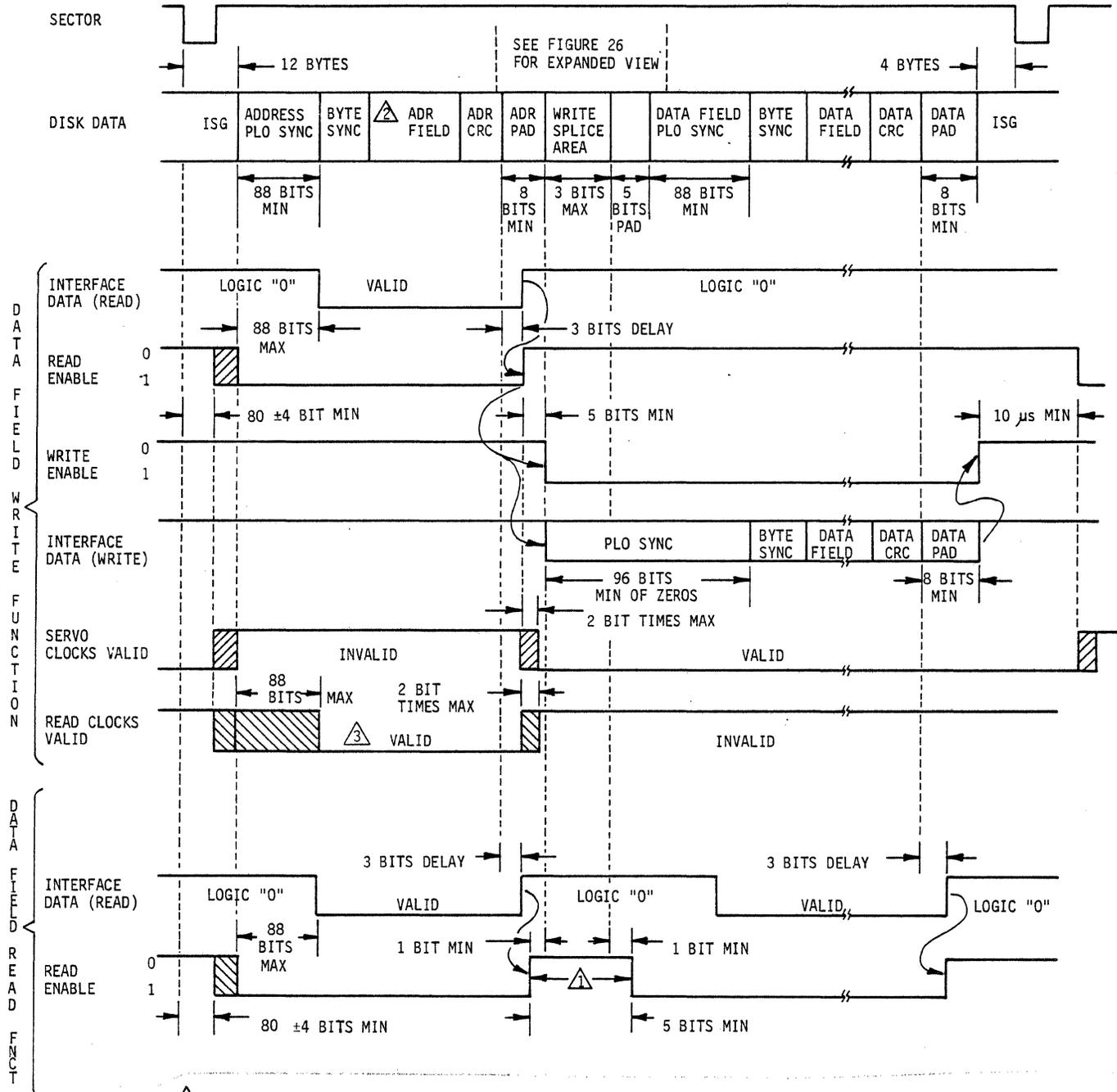
1. READ ENABLE MUST BE DEACTIVATED PRIOR TO THE WRITE SPLICE. READ ENABLE MAY BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF PLO SYNC REMAINING IN THE SYNC FIELD. THE 12 BYTE EXAMPLE CONSISTS OF ONE BYTE OF WRITE SPLICE AND 11 BYTES FOR PLO SYNC.

2. THE ADDRESS FIELD INCLUDES THE TRACK, HEAD, AND SECTOR LOCATION.

3. READ CLOCKS ARE AVAILABLE BUT NOT PHASE AND FREQUENCY SYNCHRONIZED FOR 88 BITS.

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⚠️ WHEN READ ENABLE IS DEACTIVATED, THE INTERFACE SERVO/READ CLOCK LINE WILL CONTAIN VALID SERVO CLOCKS WITHIN ONE HALF OF A SERVO CLOCK PERIOD MINIMUM TO TWO-SERVO CLOCK PERIODS MAXIMUM. THIS TRANSITION AREA WILL NOT CONTAIN ANY SHORTENED PULSE WIDTHS, BUT IT MAY CONTAIN NO TRANSITIONS FOR UP TO TWO-CLOCK PERIODS MAXIMUM.

⚠️ WHEN READ ENABLE IS ACTIVATED, THE INTERFACE SERVO/READ CLOCK LINE WILL CONTAIN SERVO CLOCKS UNTIL PLO SYNCHRONIZATION IS ESTABLISHED. THE TRANSITION FROM SERVO CLOCKS TO READ CLOCKS WILL BE ACCOMPLISHED IN THE SAME MANNER DESCRIBED IN NOTE ⚠️, i.e., NO TRANSITIONS FOR UP TO TWO-CLOCK PERIODS MAXIMUM, ETC.

ZZ075a

FIGURE 25. TYPICAL READ/WRITE DATA-EXPANDED WRITE SPLICE AREA

15.0   ACCESSORIES

15.1   FRONT PANEL KIT

The front panel kit for the WREN consists of a plastic
front panel which may be installed to the front of the
WREN. The front panel will also provide a Drive Selected
indicator.

15.2   9410-3 to 9415-3 INTERFACE ADAPTER

This optional interface adapter is a passive adapter
which will convert the 50-pin FINCH command connector to
the 34-pin WREN command connector.

15.3   WREN POWER SUPPLY

The WREN power supply is an accessory supply which will
provide the necessary DC power to support one 9415-3 WREN
drive. The characteristics of the supply are shown below:

	+5 V	+12 V
Voltage	+5 V	+12 V
Regulation	±3%	±5%
Ripple	50 mV	100 mV
Maximum Operating Current	1.5 A	2.5 A
Operating Current (Typical)	1.2 A	1.8 A
Operating Current (Peak)	1.5 A	4.0 A

15.4   HARDWARE MAINTENANCE MANUAL

The Maintenance Manual will provide the user with a
general overview and description of the WREN operation
and design basics.

15.5   TOP MOUNT PWA ADAPTER

The top mount PWA Adapter is an accessory which allows a
user to mount an additional PWA (LDI Adapter, Controller,
etc.) above the WREN. See Figure 26.

15.6   LARK DEVICE INTERFACE (LDI) ADAPTER

The LDI adapter is an accessory which can be mounted to
the top mount PWA adapter and is used to convert the
9415-3 WREN Interface to the LARK Device Interface. The
WREN-to-LDI consists of one printed wiring assembly. See
Figure 27. Two short (7 inches) flexible cables from the
adapter mate with the command and data connectors of the
WREN. These cables are permanently attached to the
adapter. A WREN compatible power connector is provided to
supply the +5 V DC power required by the adapter. An
additional 1.3 A of power must be available to the
adapter PWA for worst case operating current. Connectors
for the LDI are provided on the adapter. Reference
Engineering Specification - WREN to LDI Difference
(77715949) for details of this adapter.
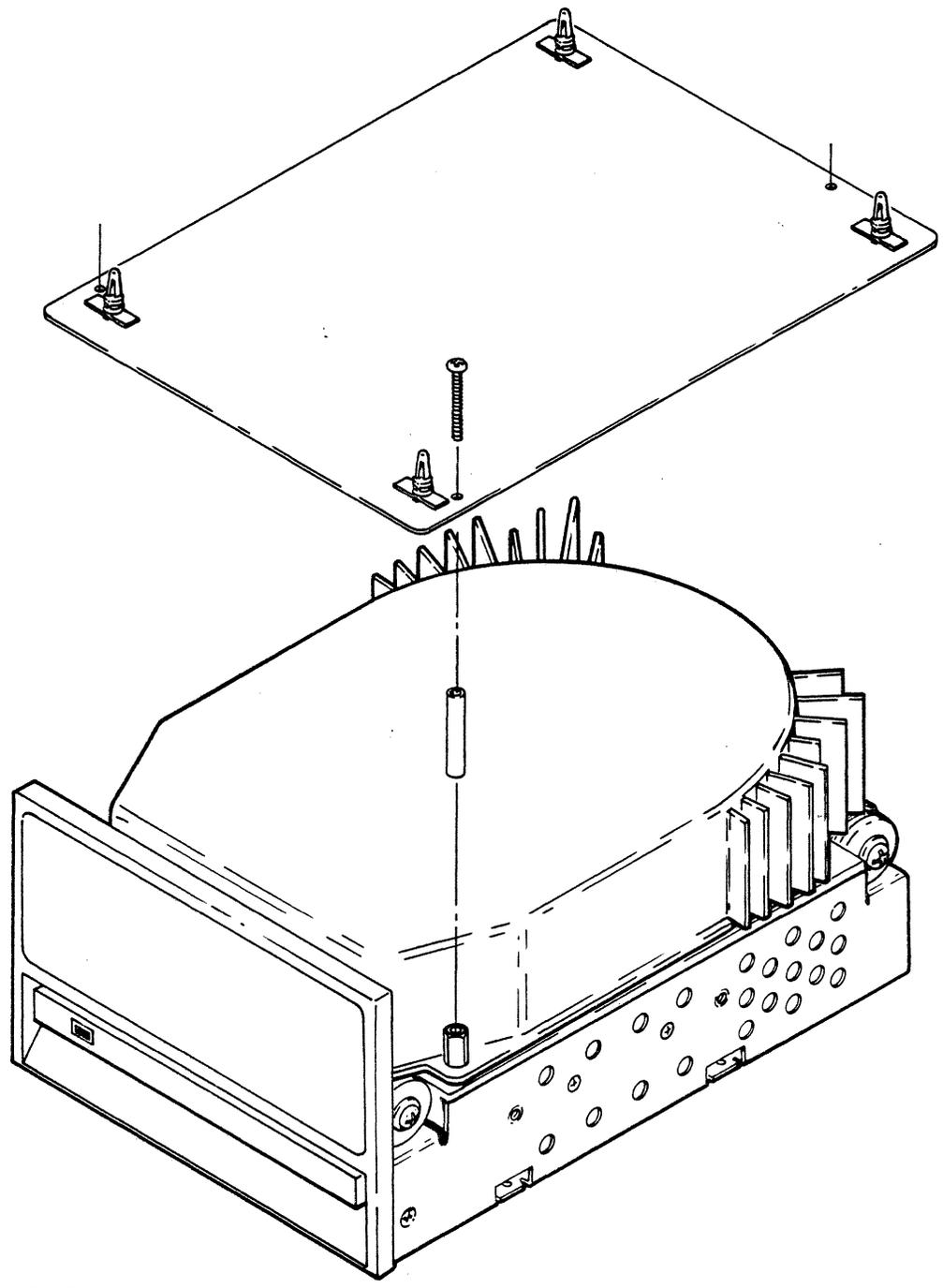
FF331a

FIGURE 26. TOP MOUNT PWA KIT
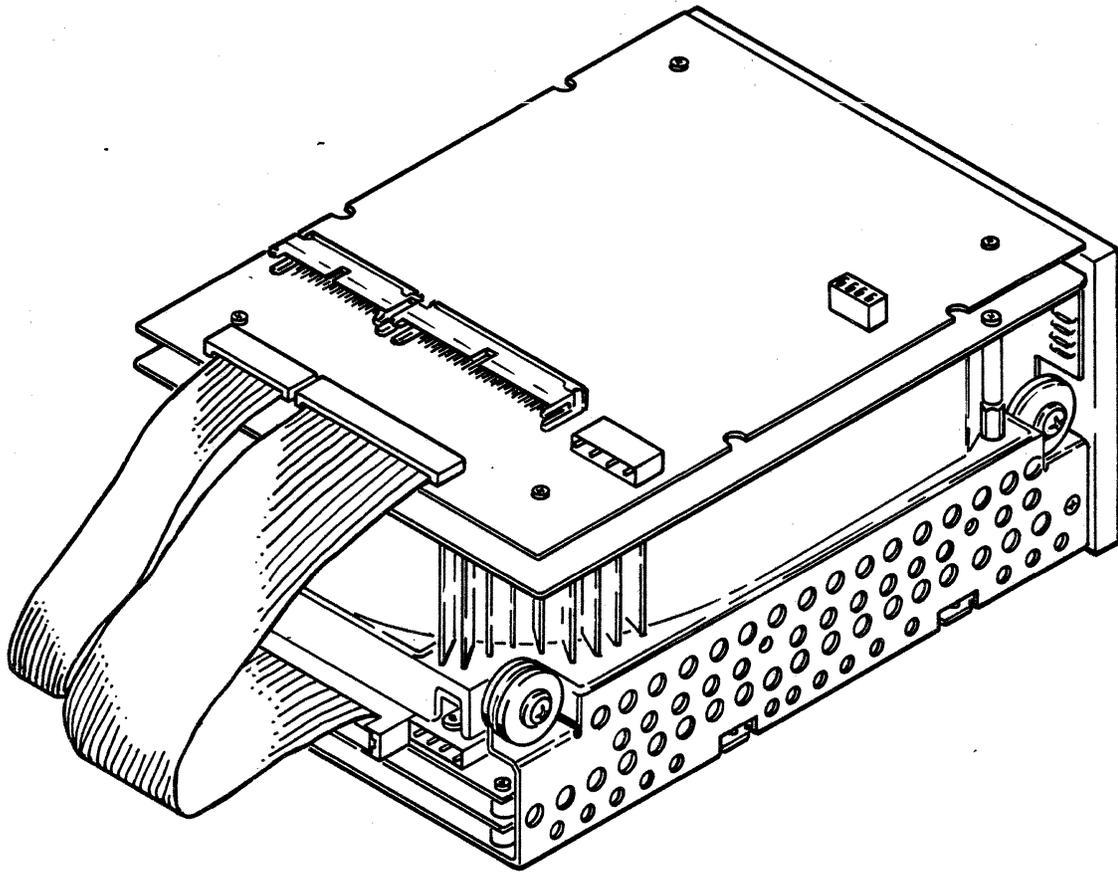
(H011a)

FIGURE 27. WREN TO LDI ADAPTER

TECHNICAL INQUIRY

FILE REFERENCE	

FROM:

Date _____

Name _____

Address _____

City _____

State _____   Zip Code _____

Area Code _____   Phone _____

FOR ADDITIONAL INFORMATION CONTACT:

Rigid Disk
Applications Engineering
Mail Station: OKM 272
Phone: (405) 324-3062

Magnetic Peripherals, Inc.
P.O. BOX 12313
Oklahoma City, Oklahoma
73157

PLEASE SUPPLY:

Document Title _____   Number _____   Revision _____

COMMENTS:
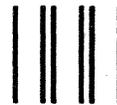
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OKLAHOMA CITY, OKLAHOMA 73157

Attention *Rigid Disk Applications Engineering, OKM 272*

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Name _____

Address _____

City _____

State _____ Zip Code _____

Area Code _____ Phone _____

FOR ADDITIONAL INFORMATION CONTACT:

Customer Training
Mail Station: OKM 154
Phone: (405) 324-3001

Magnetic Peripherals, Inc.
P.O. BOX 12313
Oklahoma City, Oklahoma
73157

FOR INFORMATION CONCERNING OEM MAINTENANCE TRAINING ON THIS EQUIPMENT MAIL THIS INQUIRY FORM OR CALL MAGNETIC PERIPHERALS, INC. (405) 324-3001

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POSTAGE WILL BE PAID BY ADDRESSEE

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P.O. BOX 12313

OKLAHOMA CITY, OKLAHOMA 73157

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