83322460J

CONTROL DATA CORPORATION

CDC® STORAGE MODULE DRIVE

BJ4M1

BJ4M2

BJ402

GENERAL DESCRIPTION

OPERATION

THEORY OF OPERATION

DISCRETE COMPONENT CIRCUITS

HARDWARE REFERENCE MANUAL

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or use Comment Sheet in the back of this manual.

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PREFACE

This manual contains reference information applicable to Control Data® BJ4M1/BJ4M2/BJ402 Storage Module Drives (SMD's). The specific types of BJ4M1/BJ4M2/BJ402 drives and their configurations are listed in the Configuration Chart (refer to table of Contents.

Most of the information in this manual is applicable to all types of the above drives. However, where information is applicable to only specific types, this is noted in the text.

The manual has been prepared for customer engineers and other technical personnel directly involved with maintaining the storage module drive (SMD).

Reference information is provided in four sections in this manual. Section numbers and a brief description of their contents are listed below.

Section 1 - General Description. Describes equipment functions, specifications, and equipment number identification.

Section 2 - Operation. Describes and illustrates the location and use of all controls and indicators, power on sequencing, and disk pack installation and removal.

Section 3 - Theory of Operation. Describes basic logic and mechanical functions.

Section 4 - Description of discrete components and their functions. For ease of use the logic diagrams, transistors and their associated components are frequently condensed into an equivalent logic symbol. This section explains these functions and illustrates the discrete elements.

Other manuals applicable to the BJ4M1/BJ4M2/402 SMD's are:

Publication No.	Title
83322450	Hardware Maintenance Manual
83322440	Normandale Circuits Manual, Vol 1.
83324440	Normandale Circuits Manual, Vol 2.

WARNING

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of the FCC Rules which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

A guide for the Disk Drive Operator Publication number 83323780, is also available. The guide may be ordered through Literature Distribution Services at the following address:

Control Data Corporation
Literature Distribution Services
308 North Dale Street
St. Paul, MN 55103.

CONTENTS

FIGURES

TABLES

CONFIGURATION CHART

EQUIP (BK)	TLA* NUMBER	POWER		RD PLO DATA SEPARATOR	PACK ACCESS COVER SOLENOID
		V	Hz		
BJ4M1 A	77445204	208/240	60	No	No
BJ4M1 B	77445205	220	50	No	No
BJ4M1 D	77445206	220	50	No	No
BJ4M2 A	77445016	208/240	60	No	No
BJ4M2 B	77445017	220	50	No	No
BJ4M2 C	77445028	208/240	60	No	No
BJ4M2 D	77445018	220	50	No	No
BJ402 A	77445021	208/240	60	No	No
BJ402 B	77445022	220	50	No	No

* For factory use only.

ABBREVIATIONS

ABR	Absolute Reserve
ABV	Above
ADDR	Address
ADRS	Address
AGC	Automatic Gain Control
AM	Address Mark
AMPL	Amplifier
AMPTD	Amplitude
BLK	Black
BLW	Below
CAR	Cylinder Address Register
CH	Channel
CHAN	Channel
CKT	Circuit
CNTLGL	Centrifugal
CNTR	Counter
COMP	Compensaton
CONFIG	Configuration
CONTD	Continued
CR REF	Cross Reference
CYL	Cylinder
DES	Desired
D/A	Digital to Analog
DCDR	Decoder
DIFF	Difference
DIR	Direction
DLY	Delay
DRV	Drive
DRVR	Driver
DSBL	Disable
ECL	Emitter Coupled Logic
ECO	Engineering Change Order
EMER	Emergency
EN	Enable
EOT	End of Travel
EQUIV	Equivalent
FCO	Field Change Order
FCTN	Function
FF	Flip Flop
FIG	Figure
FLT	Fault

ABBREVIATIONS (Contd)

FREQ	Frequency
FTU	Field Test Unit
FWD	Forward
GEN	Generator
GND	Ground
HD	Head
I/O	Input-Output
INTLK	Interlock
INTGRTR	Integrator
LD	Load
MAINT	Maintenance
MAX	Maximum
MB	Megabyte
MFM	Modified Frequency Modulation
MK	Mark
MULT	Multiple
NC	No Connection
NEG	Negative
NOM	Nominal
NORM	Normal
NRM	Normal
NRZ	Nonreturn to Zero
PCPT	Piece Part
PLO	Phase Lock Oscillator
PN	Part Number
POS	Positive
PWR	Power
RCVRS	Receivers
RD	Read
RDY	Ready
REC	Receiver
REF	Reference
REG	Register
REV	Reverse
RGTR	Register
RTM	Reserve Timer
RTZ	Return to Zero
S&IOBC	Sector and Index on B Cable
S/C	Series Code
SEC	Second
SEL	Select
SEQ	Sequence

ABBREVIATIONS (Contd)

SER	Servo
SH	Sheet
SOL	Solenoid
SR	Servo
SW	Switch
T	Track
TBS	To Be Supplied
TLA	Top Level Assembly
TP	Test Point
TRK	Track
TTL	Transistor Transistor Logic
UNREG	Unregulated
VCO	Voltage Controlled Oscillator
W+R	Write or Read
W·R	Write and Read
W/	With
W/O	Without
WRT	Write
WT	White
XDUCER	Transducer
XMTR	Transmitter

SECTION 1

GENERAL DESCRIPTION

GENERAL DESCRIPTION 1

INTRODUCTION

The BJ4M1 and BJ4M2 Storage Module Drives (SMDs) are random access digital data storage devices that connect to a central processor through a controller. The major difference between them is in their data storage capacity. The BJ4M1 stores 150 megabytes of data and the BJ4M2/BJ402 stores 300 megabytes. All the equipment specifications for these drives are listed in table 1-1.

The remainder of this section provides a general description of the drive and is divided into the following areas:

- Disk Storage Medium - Describes the disk pack that is the medium used to store the data.
- Drive Functional Description - Explains the basic function of the drive.
- Drive Physical Description - Provides a basic description of the drive's physical characteristics.
- Equipment Configuration - Describes the various drive configurations and how to identify them.

TABLE 1-1. EQUIPMENT SPECIFICATIONS

Specification	Value
Size	
Height	914 mm (36 in)
Width	914 mm (36 in)
Depth	584 mm (23 in)
Weight	249 kg (550 lb)
Temperature	
Operating	15°C(59°F) to 32°C (90°F
Operating Change	6.7°C (12°F) per hour
Transit (packed for shipment)	-40°C (-40°F) to 70°C (158°F)
Non-Operating Change	20°C (36°F) per hour
Relative Humidity	Without condensation
Operating	20% to 80%
Transit (packed for shipment)	5% to 95%
Altitude	
Operating	-305 m (-1000 ft) to 1981 m (6500 ft)
Transit (packed for shipment)	-305 m (-1000 ft) to 4572 m (15 000 ft)

Table Continued on Next Page

TABLE 1-1. EQUIPMENT SPECIFICATIONS (Contd)

Specification	Value
Disk Pack	
Type	883-91 (one per drive)
Disks/Pack	12 (Top and bottom disks are for protection only)
Data Surfaces	19
Servo Surfaces	1
Usable Tracks/Surface	823 (150 MB units can use only 411 of these tracks)
Tracks/inch	384
Track Spacing	0.066 mm (0.0026 in) center-to-center
Coating	Magnetic Oxide
Data Capacity	Values quoted below are based on 8-bit bytes, not allowing for tolerance gaps, sectoring, etc.)
	150 MB / 300 MB
Bytes/Track	20 160 / 20 160
Bytes/Cylinder	383 040 / 383 040
Bytes/Spindle	154 748 160 / 309 496 320
Cylinders/Spindle	411 / 823

Table Continued on Next Page

TABLE 1-1. EQUIPMENT SPECIFICATIONS (Contd)

Specification	Value
Recording Characteristics	
Mode	Modified Frequency Modulation (MFM)
Density (nominal)	
Outer Track	1590 bits/cm (4038 bits/in)
Inner Track	2377 bits/cm (6038 bits/in)
Rate (nominal)	9.67 MHz (1 209 600 bytes/s)
Heads	
Read/Write	19
Servo	1
Read/Write Width (150 MB)	0.102 mm (0.004 in)
Read/Write Width (300 MB)	0.051 mm (0.002 in)
Seek Characteristics	
Mechanism	Voice coil, driven by servo loop
Maximum Seek Time	55 ms (411 or 823 tracks)
Maximum Seek Time	6 ms (one track)
Average Seek Time	30 ms

Table Continued on Next Page

TABLE 1-1. EQUIPMENT SPECIFICATIONS (Contd)

Specification	Value
Latency	Latency is time required to reach specific track location after drive is on cylinder.
Average	8.33 ms (at 3600 r/min)
Maximum	17.3 ms (at 3474 r/min)
Spindle Speed	3600 r/min
Controllers per Drive	1
Power Requirements	Refer to configuration chart in front matter of this manual

DISK STORAGE MEDIUM

The disk pack is the storage medium for the drive. The disk pack contains 12 14-inch disks (10 of which are used) center-mounted on a hub (refer to figure 1-1). The disk pack is portable and interchangeable between equivalent drives.

The ten usable disks have 1 servo surface and 19 data surfaces. The data surfaces provide data storage and are referred to as read/write surfaces. The servo surface contains information prerecorded at the factory and is used by the drive to generate various timing and position signals.

The servo surface and the data surfaces are coated with a layer of magnetic oxide and related binders and adhesives. Each of these surfaces has its recording tracks grouped in a 2-inch band near the outer edge of the disk. The number of tracks contained on each data surface and the spacing between the tracks are listed in table 1-1.

Both the 150 MB and 300 MB drives use the same disk pack. The specifications for this disk pack are found in table 1-1.

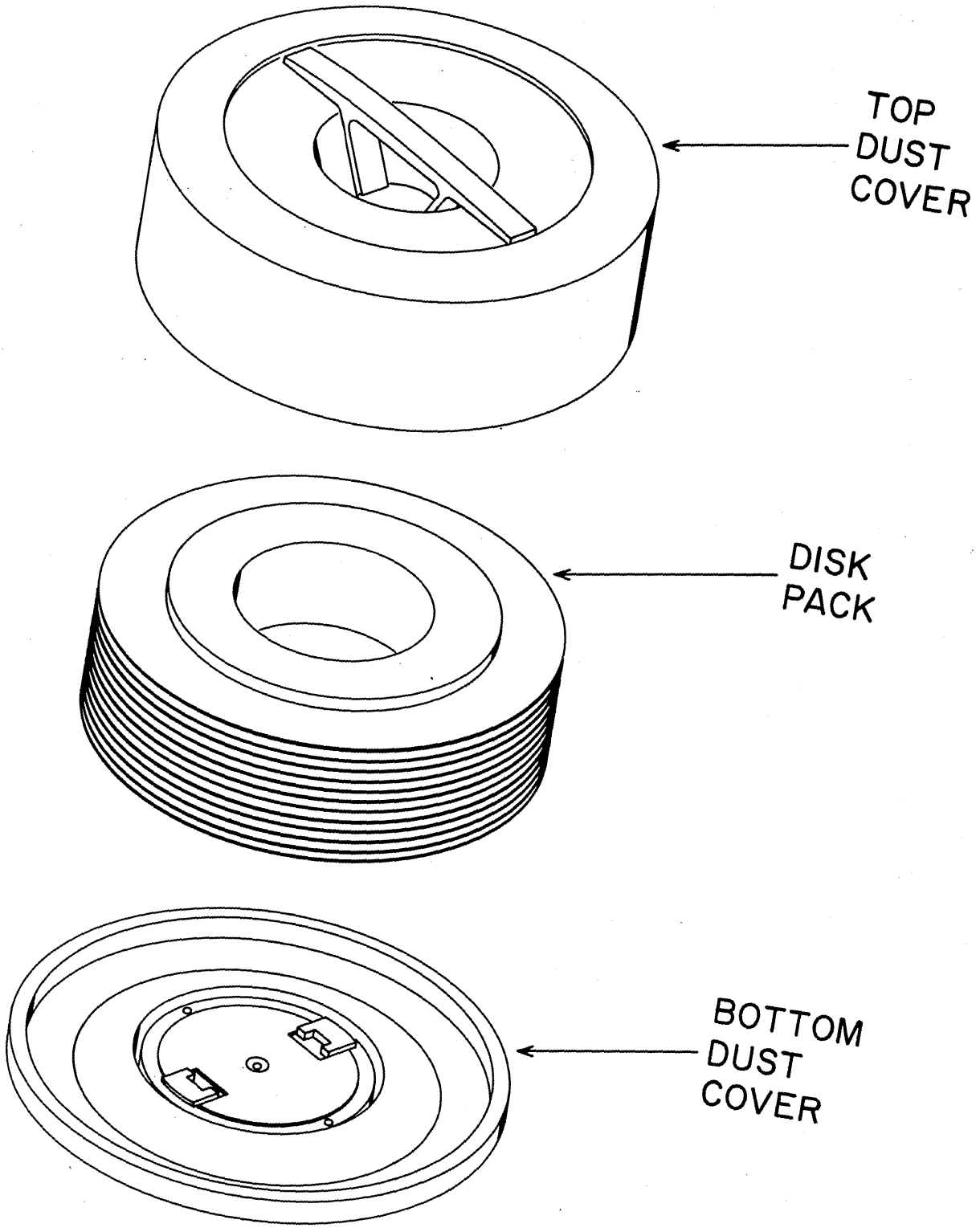

Figure 1-1. Disk Pack

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DRIVE FUNCTIONAL DESCRIPTION

The drive contains all the circuit and mechanical devices necessary to record data on and recover it from the disk pack (refer to figure 1-2). The power required for this is provided by the drives power supply, which receives its input power from the site main power source.

All functions performed by the drive are done under direction of the controller. The controller communicates with the drive via the interface which consists of a number of I/O lines carrying the necessary signals to and from the drive.

Some interface lines, including those that carry commands to the drive are not enabled unless the drive is selected by the controller. Unit selection allows the controller, which can be connected to more than one drive, to initiate and direct an operation on a specific unit.

All operations performed by the drive are related to data storage and recovery (normally referred to as writing and reading). The actual reading and writing is performed by electromagnetic devices called heads that are positioned over the recording surfaces of the rotating disk pack. There is a separate head for each surface in the pack and the heads are positioned in such a way that data is written in concentric tracks around the disk surfaces (refer to figure 1-2).

Before any read and write operation can be performed the controller must instruct the drive to position the heads over the desired track (this function is called seeking) and also to use the head located over the surface where the operation is to be performed (head selection).

After selecting a head and arriving at the data track, the controller still must locate that portion of the track where the data is to be written or read. This is called track orientation and is done by using the Index and Sector signals generated by the drive. The Index signal indicates the logical beginning of each track and the Sector signals are used by the controller to determine the position of the head on the track with respect to Index.

When the desired location is reached, the controller commands the drive to actually read or write the data. During a read operation the drive recovers data from the pack, and transmits it to the controller. During a write operation, the drive receives data from the controller, processes it, and writes it on the disk pack.

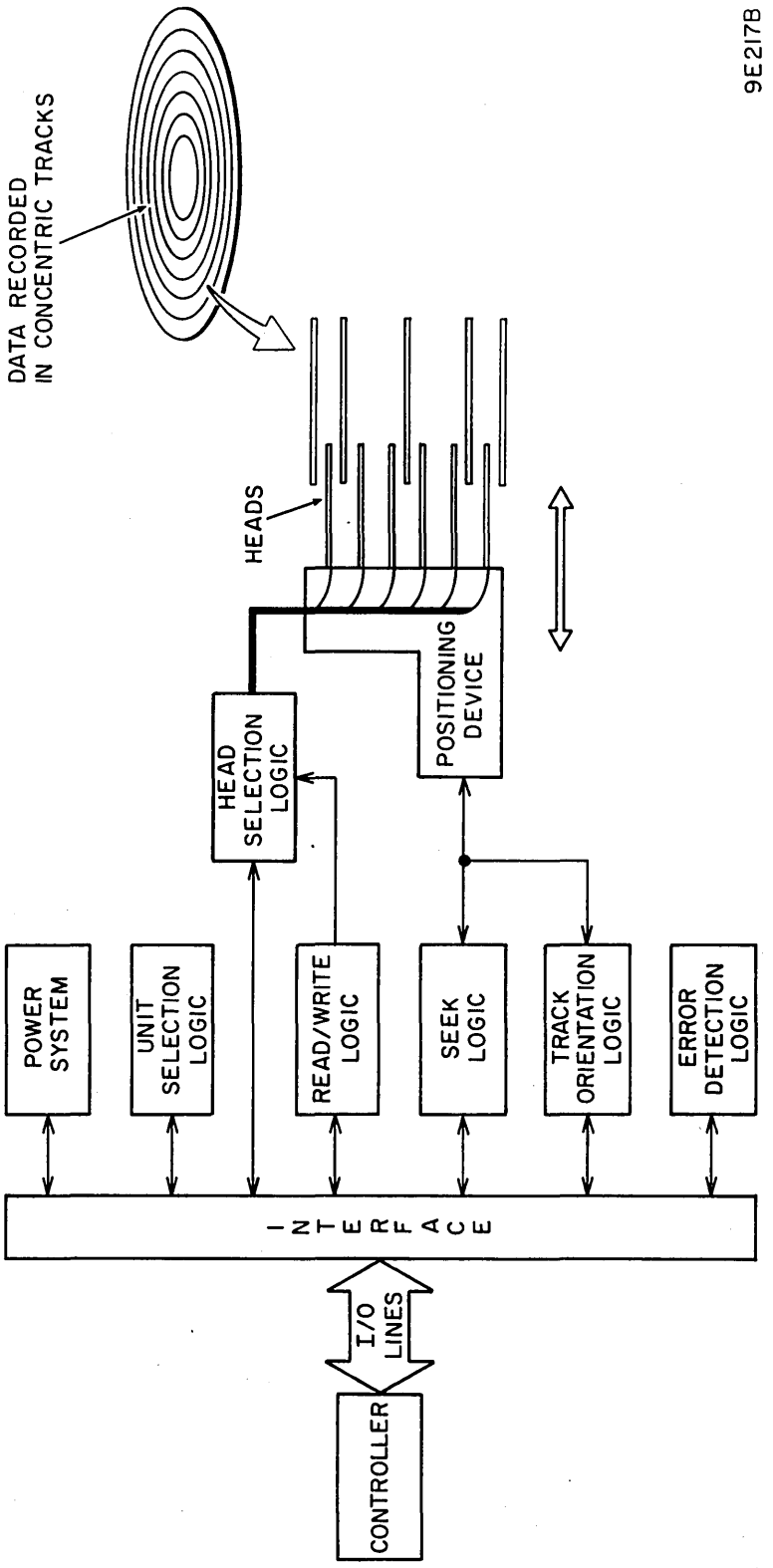

Figure 1-2. Drive Functional Blocks

The drive is also capable of recognizing certain errors that may occur during its operation. When an error is detected, it is indicated either by a signal to the controller or by a maintenance indicator on the drive itself.

DRIVE PHYSICAL DESCRIPTION

GENERAL

The following describes the physical characteristics of the drive. The discussion is divided into two major areas (1) assemblies and (2) logic and circuitry.

ASSEMBLIES

The major drive assemblies are shown on figure 1-3 and described in table 1-2. A more complete description of the drive assemblies is found in the Parts Data Section of the maintenance manual.

TABLE 1-2. DRIVE ASSEMBLIES

Actuator	Contains voice coil and carriage. This assembly positions the heads over the disk pack.
Blower Assembly	Contains a blower motor that circulates cooling air for the drive.
Deck Cover	Provides an electrical interference shield for the drive and also reduces noise level output from drive.
Drive Motor	Provides rotational motion that turns spindle and disk pack.
Front Door	Provides access to blower assembly and the lower front part of cabinet.
Table Continued on Next Page	

TABLE 1-2. DRIVE ASSEMBLIES (Contd)

Heads	Detect data transitions that are on the pack if drive is reading. Writes data transitions on the disk pack if drive is writing.
Logic Chassis	Contains logic cards that control operation of drive.
Magnet	Provides permanent magnetic field that is used in conjunction with voice coil to move carriage and heads.
Operator Control Panel	Contains switches that allow operator to control and monitor basic operation of drive.
Pack Access Cover	Provides access to disk pack and pack area.
Pack Access Cover Solenoid (Note 1)	Prevents pack access cover from being opened if the pack is spinning.
Pack Access Cover Switch (Note 1)	Interlock that deenergizes drive motor if pack access cover is opened while pack is spinning. It also prevents motor from starting unless cover is closed.
Pack On Switch	Interlock that prevents drive motor from starting when pack is not installed.
Parking Brake	Holds spindle while disk pack is being installed and removed.
Power Supply	Furnishes all necessary voltages for drive operation.
Read/Write Chassis	Contains cards that are essential to drive read/write operations.

Table Continued on Next Page

TABLE 1-2. DRIVE ASSEMBLIES (Contd)

Rear Door	Provides access to power supply, logic chassis and lower rear of cabinet.
Shroud and Shroud Cover	Provides protection and ventilation for disk pack.
Side Panels	Provide access to either side of drive.
Spindle and Lockshaft	Provides mounting surface for disk pack. Lockshaft secures disk pack to spindle. Drive motor transmits rotational motion to spindle via drive belt thereby causing pack to rotate.
Top Cover	Covers entire top of drive thereby protecting drive assemblies and reducing output noise level.

Notes:

1. The pack access cover interlock switch and solenoid are part of the interlock assembly on VDE units.

LOGIC AND CIRCUITRY

The drive contains integrated and discrete component circuits as well as relays, switches and other electromechanical elements. All of these work together in performing the various drive functions.

Diagrams showing all circuits and interconnecting wiring are contained in the maintenance manual.

EQUIPMENT CONFIGURATION

GENERAL

The equipment configuration is identified by the cabinet identification plate and by the FCO log. It is necessary to identify the equipment configuration to determine if the manuals being used are applicable to the equipment. The following describes the cabinet identification plate, FCO log and manual to equipment correlation.

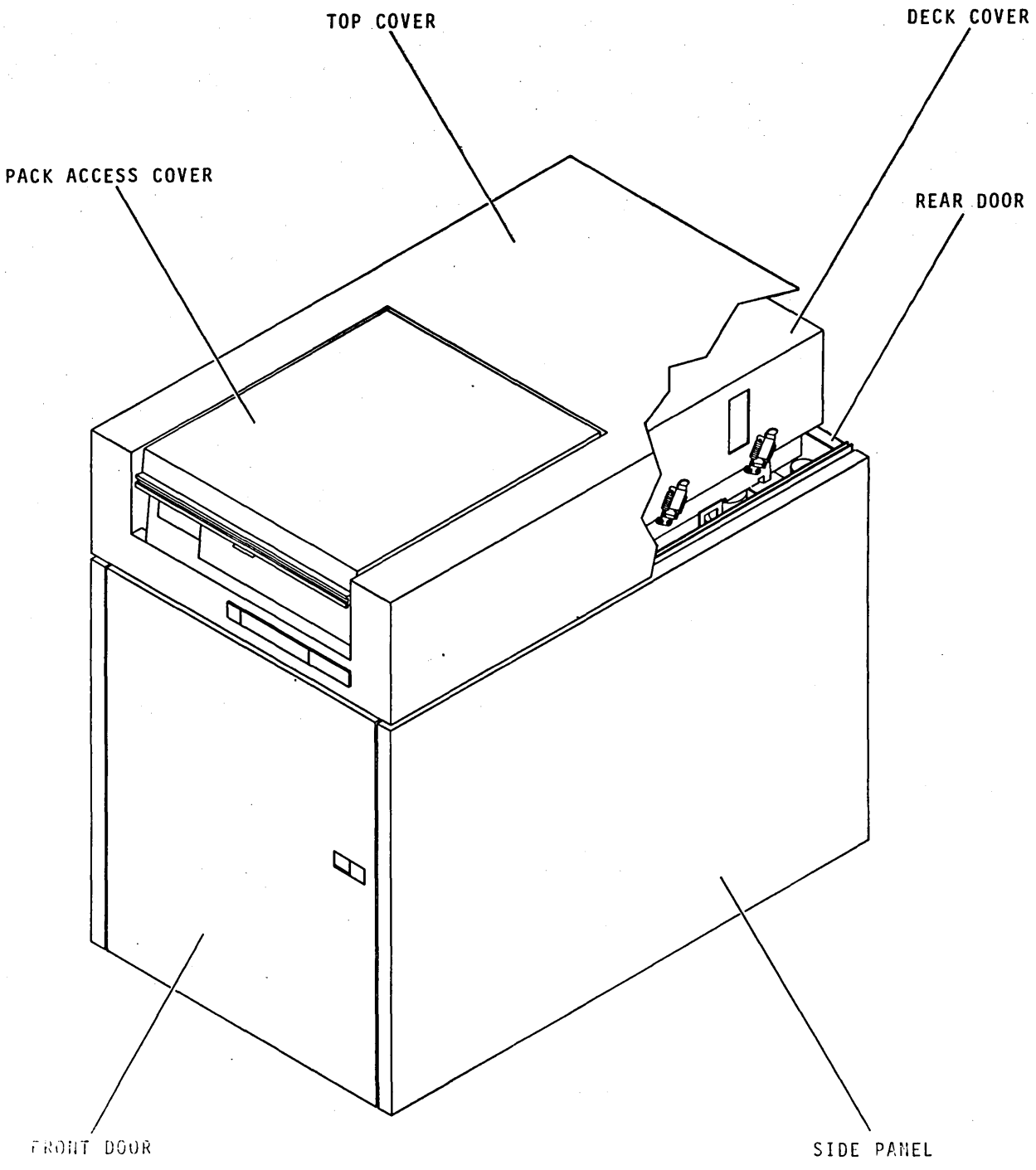

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Figure 1-3. Drive Assemblies (Sheet 1)

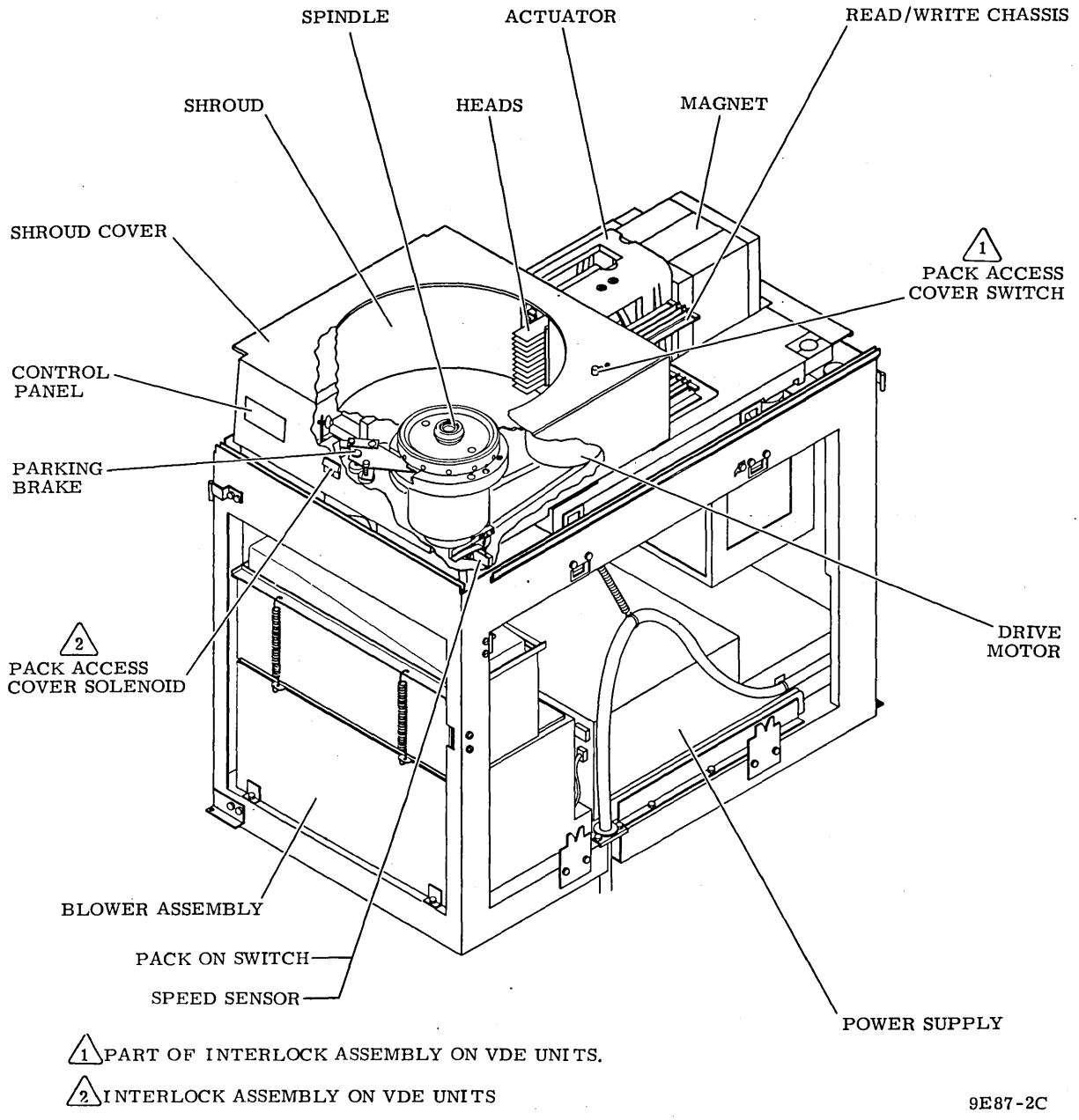


Figure 1-3. Drive Assemblies (Sheet 2)

EQUIPMENT IDENTIFICATION PLATE

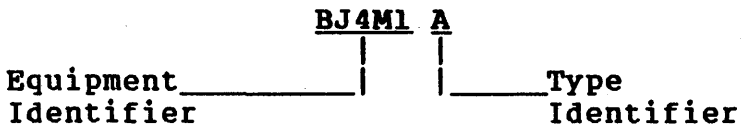
GENERAL

This plate is attached to the frame at the rear of the drive (refer to figure 1-4). This plate identifies the drives basic mechanical and logical configuration at the time it leaves the factory. The information contained on this plate is defined in the following.

Equipment Identification Number

This number is divided into the two parts shown in the example:

EXAMPLE:



The equipment identifier indicates the basic functional capabilities of the drive. This number will be either BJ4M1 or BJ4M2/BJ402. The differences between these units can be determined by referring to table 1-1.

The type identifier indicates differences between drives that have the same equipment number. These differences are necessary to adapt a drive to specific system requirements. However, they do not change the overall capabilities of the drive as defined in table 1-1.

The various types differ according to their input voltage requirements and standard options. The standard options are those features with which the drive is equipped when it leaves the factory. The Configuration Chart in the front matter of this manual (refer to table of Contents) lists both input voltage requirements and standard options for all types of BJ4M1, BJ4M2, and BJ402 drives.

The standard options listed in the Configuration Chart are as follows:

- Pack Access Cover Solenoid - Solenoid that locks the pack access cover in the closed position when the pack is spinning.

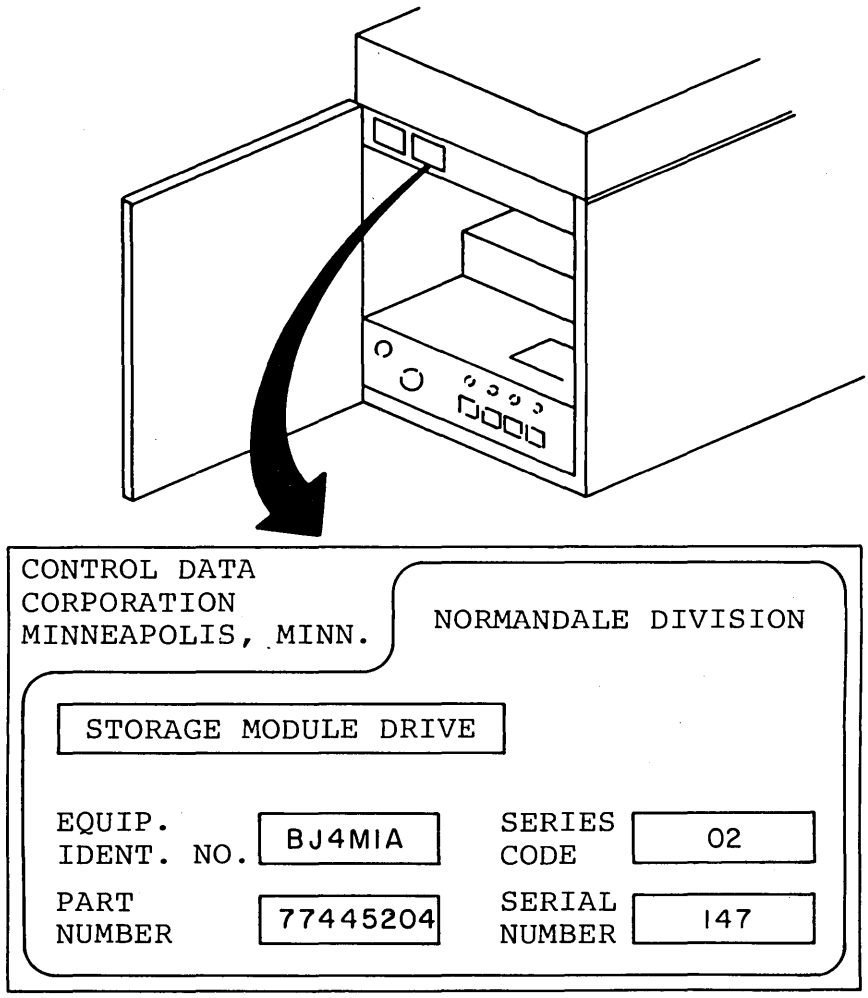


Figure 1-4. Equipment Identification Plate

- Read PLO/Data Separator - Converts MFM data, read from disk into NRZ data and generates read clock signals which are synchronized to NRZ data. Both of these are sent to controller.

Series Code

The series code represents a time period within which a unit is built. While all units are interchangeable at the system level regardless of series code, parts differences may exist within units built in different series codes. When a parts difference exists, that difference is noted in the parts data section of the hardware maintenance manual.

Part Number

This number indicates the top level assembly number of the equipment and is for factory use only.

Serial Number

Each drive has a unique serial number assigned to it. Serial numbers are assigned sequentially within a family of drives. Therefore, no two equipments will have the same serial number.

FCO LOG

Field Change Orders (FCO's) are electrical or mechanical changes that may be performed either at the factory or in the field. FCO changes do not affect the series code but are indicated by an entry on the FCO log that accompanies each machine. The components of a machine with an FCO installed may not be interchangeable with those of a machine without the FCO; therefore, it is important that the FCO log be kept current by th person installing each FCO.

MANUAL TO EQUIPMENT CORRELATION

Throughout the life cycle of a machine, changes are made either in the factory (a series code change) or by FCOs installed in the field. All of these changes are also reflected in changes to the manual package. In order to assure that the manual correlates with the machine, refer to the Manual to Equipment Level Correlation sheet located in the front matter of the hardware maintenance manual. This sheet records all the FCOs which are included in the manual. It should correlate with the machine FCO log if all the FCOs have also been installed in the machine.

SECTION 2

OPERATION

OPERATION 2

INTRODUCTION

This section provides the information and instructions necessary for operating the drive and is divided into the following areas:

- Controls and Indicators - Locates and describes various controls and indicators related to operation of the drive.
- Operating Instructions - Describes procedures for operating the drive.

CONTROLS AND INDICATORS

GENERAL

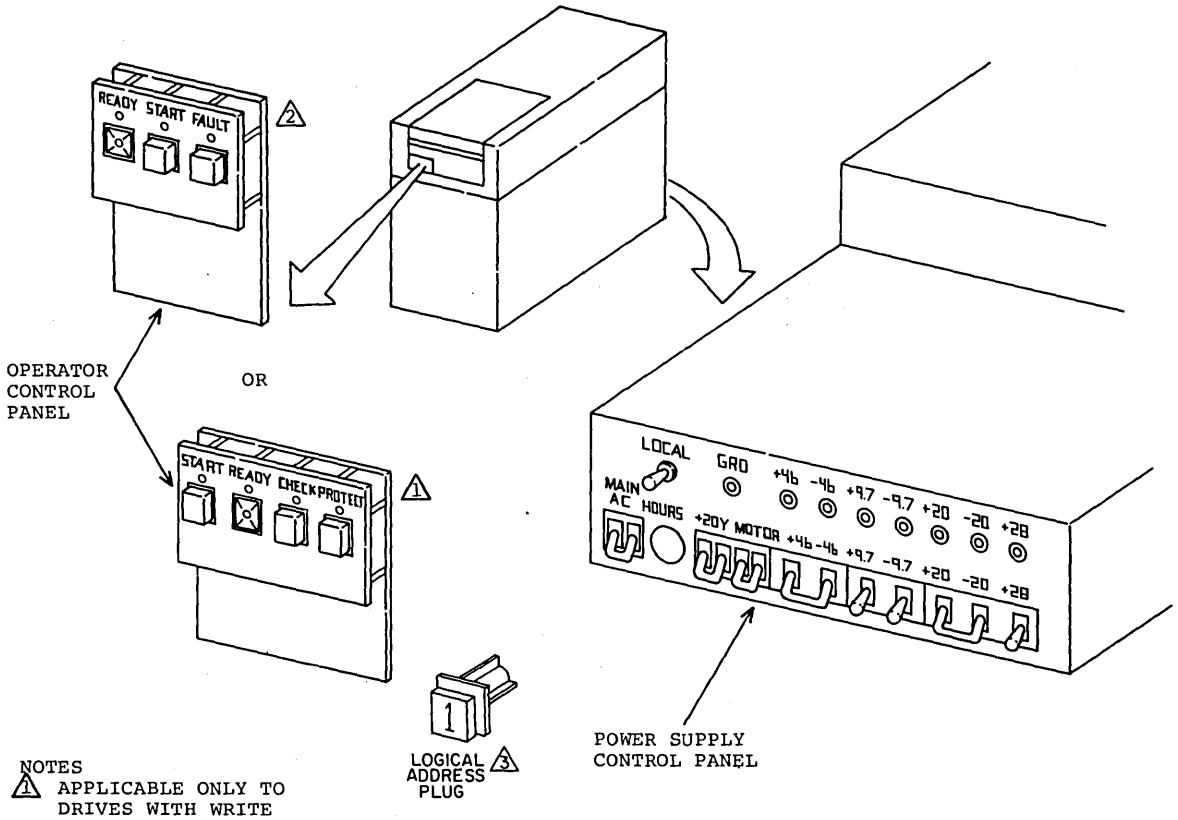
The drive contains two non-maintenance control panels. These are: (1) operator control panel and (2) power supply control panel. These are shown on figures 2-1 and 2-2.

NOTE

Additional controls, indicators and test points used primarily for maintenance are described in the hardware maintenance manual.

OPERATOR CONTROL PANEL

The operator control panel contains switches and indicators to control and monitor the basic operation of the drive. These switches and indicators are illustrated in figures 2-1 and 2-2 and are described in table 2-1.



NOTES

1. APPLICABLE ONLY TO DRIVES WITH WRITE PROTECT OPTION.
2. APPLICABLE ONLY TO UNITS WITHOUT WRITE PROTECT OPTION.
3. FITS INTO SLOT BENEATH READY INDICATOR. LOGICAL ADDRESS MAY BE ANY NUMBER FROM 0 TO 15.

9H330A

Figure 2-1. Controls and Indicators (Non-VDE)

TABLE 2-1. OPERATOR CONTROL PANEL FUNCTIONS

Control or Indicator	Function
Logical Address Plug	Determines logical address of drive. Address can be set to any number from 0 to 15 by installing the proper plug. If no plug is installed, the address is 15. Drive comes from the factory with a complete set of logical address plugs, each having a unique address. The available plugs with their associated address and part number are listed in the parts data section of the hardware maintenance manual.
START switch/indicator	Pressing switch when drive is in power off condition (disk pack not spinning) lights indicator and starts power on sequence, provided that the following conditions are met: • Disk pack is installed. • Pack access cover is closed. • All power supply circuit breakers are on. On VDE units, the pack access cover will lock when the START switch is pressed. It cannot be opened unless the START switch is pressed to its off condition.
Table Continued on Next Page	

TABLE 2-1. OPERATOR CONTROL PANEL FUNCTIONS (Contd)

Control or Indicator	Function
READY indicator	Lights when unit is up to speed, the heads are loaded, and no fault condition exists. Flashes during power on and off sequences.
FAULT switch/indicator	Lights if a fault condition exists within the drive. It is extinguished by any of the following, provided that the reason for the fault is no longer present: • Pressing FAULT switch on operator control panel. • Fault Clear signal from controller. • Maintenance Fault Clear switch on fault card in logic chassis location A17. Conditions causing faults are described in the Fault Detection discussion in section 3 of this manual.
WRITE PROTECT switch/indicator	Pressing switch to light indicator disables the write driver circuits and prevents them from writing data on the pack. Pressing the switch to turn off the indicators removes the disable from the write circuits.

POWER SUPPLY CONTROL PANEL

The power supply control panel contains circuit breakers, test points and an elapsed time meter. These provide the means of controlling and monitoring operation of the power supply. The control panel is accessed by opening the rear door of the drive cabinet. Figures 2-1 and 2-2 show the power supply control panel and table 2-2 explains its functions.

TABLE 2-2. POWER SUPPLY CONTROL PANEL FUNCTIONS

Control or Indicator	Function
MAIN AC circuit breaker	Controls application of site ac power to drive. Closing this breaker applies power to elapsed time meter. On VDE units, the pack access cover cannot be opened for approximately 30 seconds after this breaker is placed in the on position.
HOURS elapsed time meter	Records accumulated ac power-on time. Meter starts when MAIN AC circuit breaker is closed.
LOCAL/REMOTE switch	Controls whether drive can be powered up from drive (LOCAL) or controller (REMOTE). In LOCAL position, drive power-on sequence starts when START switch is pressed. In REMOTE position, drive power-on sequence starts when START switch is pressed and sequence power ground is received from controller.
+20Y, MOTOR, +46, -46, +9.7, -9.7, +20, -20, and +28 circuit breakers	Each circuit breaker controls application of associated voltages to drive, and also provides overload protection.

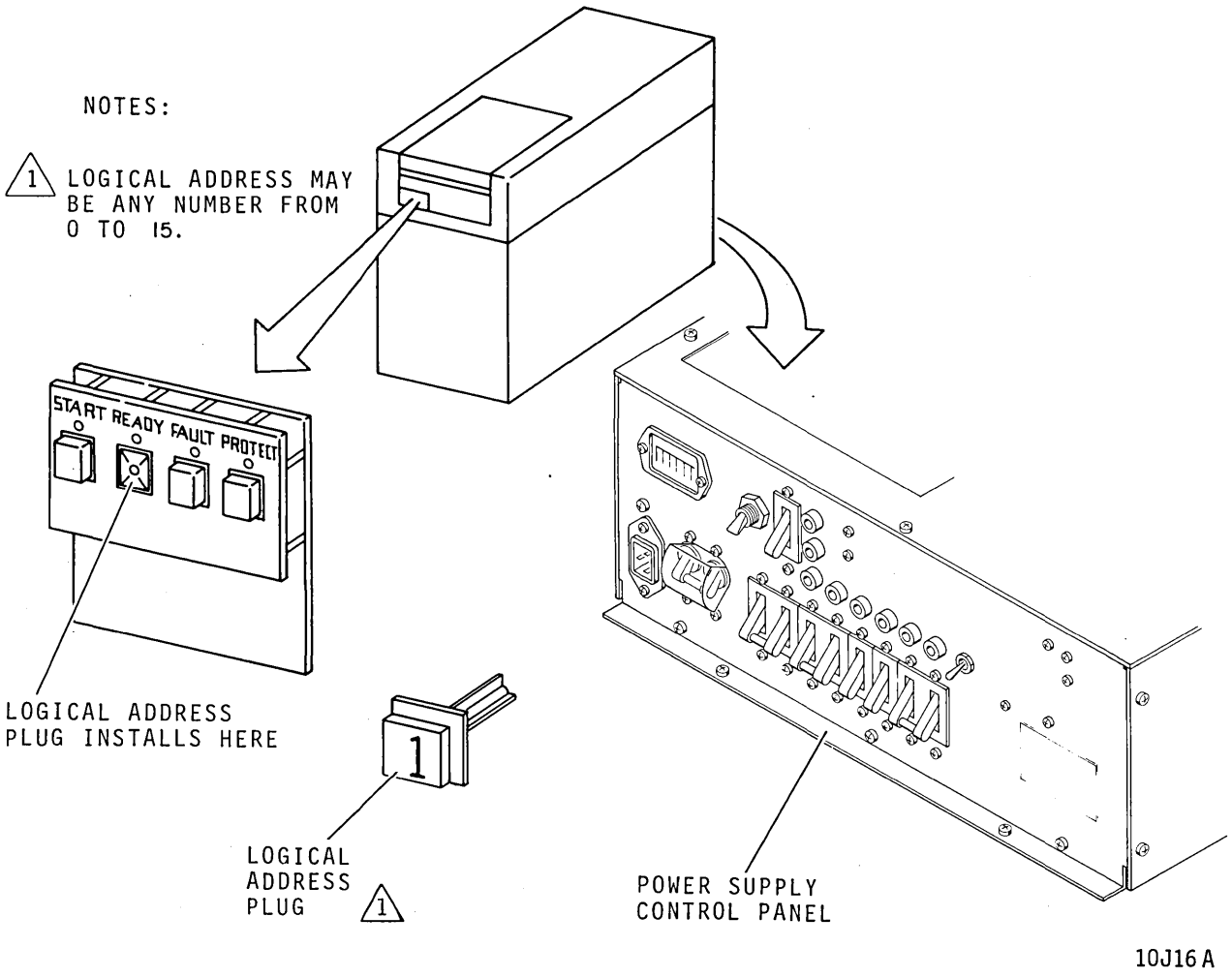


Figure 2-2. Controls and Indicators (VDE)

OPERATING INSTRUCTIONS

GENERAL

The following information describes the procedures that are performed during normal operation of the drive. These procedures are: disk pack storage, handling, inspection and cleaning, disk pack removal and installation, and power on and off.

DISK PACK STORAGE

To ensure maximum disk pack life and reliability, observe the following precautions:

- Store disk packs in machine-room atmosphere (60°F to 90°F, 10% to 80% relative humidity).
- If disk pack must be stored in different environment, allow two hours for adjustment to computer environment before use.
- Never store disk pack in direct sunlight or in dirty environment.
- Store disk packs flat, not on edge. They may be stacked with similar packs when stored.
- Always be sure that both top and bottom plastic covers are on disk pack and locked together whenever it is not actually installed in a drive.
- Do not mark on disk packs. Residue may be released that could cause airborne contamination.
- Do not attach any label to the disk pack itself. Labels will not remain attached when the pack is spinning and catastrophic head crashes may result. All labels should be placed on the pack canister if required.
- Cleaning of pack surfaces is not recommended.

DISK PACK INSTALLATION

The disk pack must be installed prior to performing any drive operations. Disk Pack installation consists of setting the pack on the drive spindle and rotating the pack until the pack lockscrew is locked to the spindle lockshaft. Install pack as follows:

CAUTION

Make certain that no dust or other foreign particles are present in shroud area. Also, blowers must operate for at least two minutes prior to disk pack installation in order to purge blower system.

1. Set circuit breakers to on and observe that blower starts.

2. Raise pack access cover.

3. Disengage bottom dust cover from disk pack by squeezing levers of release mechanism in center of bottom dust cover and set cover aside to an uncontaminated storage area.

CAUTION

Non-fully retracted heads indicate a problem in the drives servo and may result in damage to the pack or heads during pack installation or removal. If heads are not fully retracted, contact maintenance personnel. DO NOT push on heads.

NOTE

Top dust cover actuates parking brake when pack is set on spindle. Actuating brake holds spindle stationary while pack is installed. An audible click indicates brake is engaged.

4. Set disk pack on spindle, avoiding abusive contact between disk pack and spindle, then twist clockwise until it is secured to spindle lockshaft.

5. Lift top dust cover clear of drive and store it with bottom dust cover.

CAUTION

Spin pack to ensure that removing top dust cover released parking brake.

DISK PACK REMOVAL

Disk pack removal consists of removing the pack from the spindle, installing the dust covers and setting the pack aside in a storage area. Remove the disk pack as follows:

1. Press START switch to stop drive motor and unload heads.

2. When disk pack rotation has stopped completely, open pack access cover.

CAUTION

Non-fully retracted heads indicate a problem in the drive's servo and may result in damage to the pack or heads during pack installation or removal. If heads are not fully retracted, contact maintenance personnel. DO NOT push on heads.

3. Place top dust cover over disk pack so post protruding from center of disk pack fits into dust cover handle.

4. Turn cover counterclockwise until disk pack is free of spindle.

CAUTION

Avoid abusive contact between disk pack and spindle.

5. Lift top cover and disk pack clear of drive. Close pack access cover.

6. Place bottom dust cover on disk pack and store pack in an uncontaminated storage area.

POWER ON PROCEDURE

The following procedure describes how power is applied to the drive.

1. Set all power supply circuit breakers to on, and observe that blowers start.

CAUTION

Allow blowers to operate for at least two minutes before installing disk pack.

2. Install disk pack as instructed in disk pack installation procedure.

3. Set LOCAL/REMOTE switch to desired position.

4. Press START switch to light START indicator. If drive is in Local mode, drive motor starts immediately and heads will load when motor is up to speed. If drive is in remote mode, drive motor starts and heads load whenever Sequence Power Ground is available from controller (refer to discussion on power system in section 3 of this manual).

5. Observe that READY indicator lights when heads have loaded. The drive is now ready for online operations.

POWER OFF PROCEDURE

The power off sequence can be started either locally or remotely depending on the setting of the LOCAL/REMOTE switch. If this switch is in LOCAL, the sequence starts when the START switch is pressed to extinguish the START indicator. If the switch is in REMOTE, the sequence starts either when the START switch is pressed or when the Sequence Power Ground signal is disabled at the controller (refer to discussion on Power System in section 3 of this manual).

In either case, the power off sequence unloads the heads, stops the drive motor and extinguishes the READY indicator.

SECTION 3

THEORY OF OPERATION

INTRODUCTION

The theory of operation section describes drive operations and the hardware used in performing them. The descriptions in this section apply, except where indicated, to all non-VDE units. VDE units use a different power supply and have other significant differences. Theory for the VDE units is provided in Section 3A when it differs significantly.

Figure 3-1 is a functional block diagram of the drive. Theory is divided into the following areas:

- Power System Functions - Describes how the drive provides the voltage necessary for drive operation.
- Electromechanical Functions - Provides a physical and functional description of the mechanical description of the mechanical and electromechanical portions of the drive's disk pack rotation, head positioning and air flow system.
- Interface Functions - Describes the signal lines connecting the drive and controller. It also describes the I/O signals carried by these lines and how they are processed by the drive logic.
- Unit Selection - Explains how the controller logically selects the drive so the drive will respond to controller commands.
- Seek Functions - Explains how the servo logic controls the movements of the head positioning mechanism in positioning the heads over the disk pack.
- Machine Clock Functions - Explains how this circuit uses signals derived from the disk pack to generate timing pulses for the index, sector and read/write circuits.

- Index Detection - Describes how the drive detects the index pattern which is used to indicate the logical beginning of each track.

- Sector Detection - Explains how the drive derives the sector pulses, which are used to determine the angular position, with respect to Index of the read/write heads.

- Head Selection - Explains the head selection process.

- Read/Write Functions - Describes how the drive processes the data that it reads from and writes on the disk pack.

- Fault and Error Conditions - Describes the conditions that the drive interprets as faults and errors.

The descriptions in this section are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software environments.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in the hardware maintenance manual should take precedence over those in this manual if there is a conflict between the two.

POWER SYSTEM FUNCTIONS

GENERAL

The major element in the drives power system is the power supply. The power supply receives its input from the site ac power source which produces all the ac and dc voltages necessary for drive operation. These voltages are distributed to the drive circuitry via circuit breakers.

The power system descriptions in this chapter pertain to all non-VDE units. Power system descriptions for VDE units are provided in section 3A.

The drive motor is started and heads load function initiated during the power on sequence. The power off sequence unloads the heads and stops the drive motor. The drives LOCAL/REMOTE switch initiates these sequences either at the drive (local) or at the controller (remote).

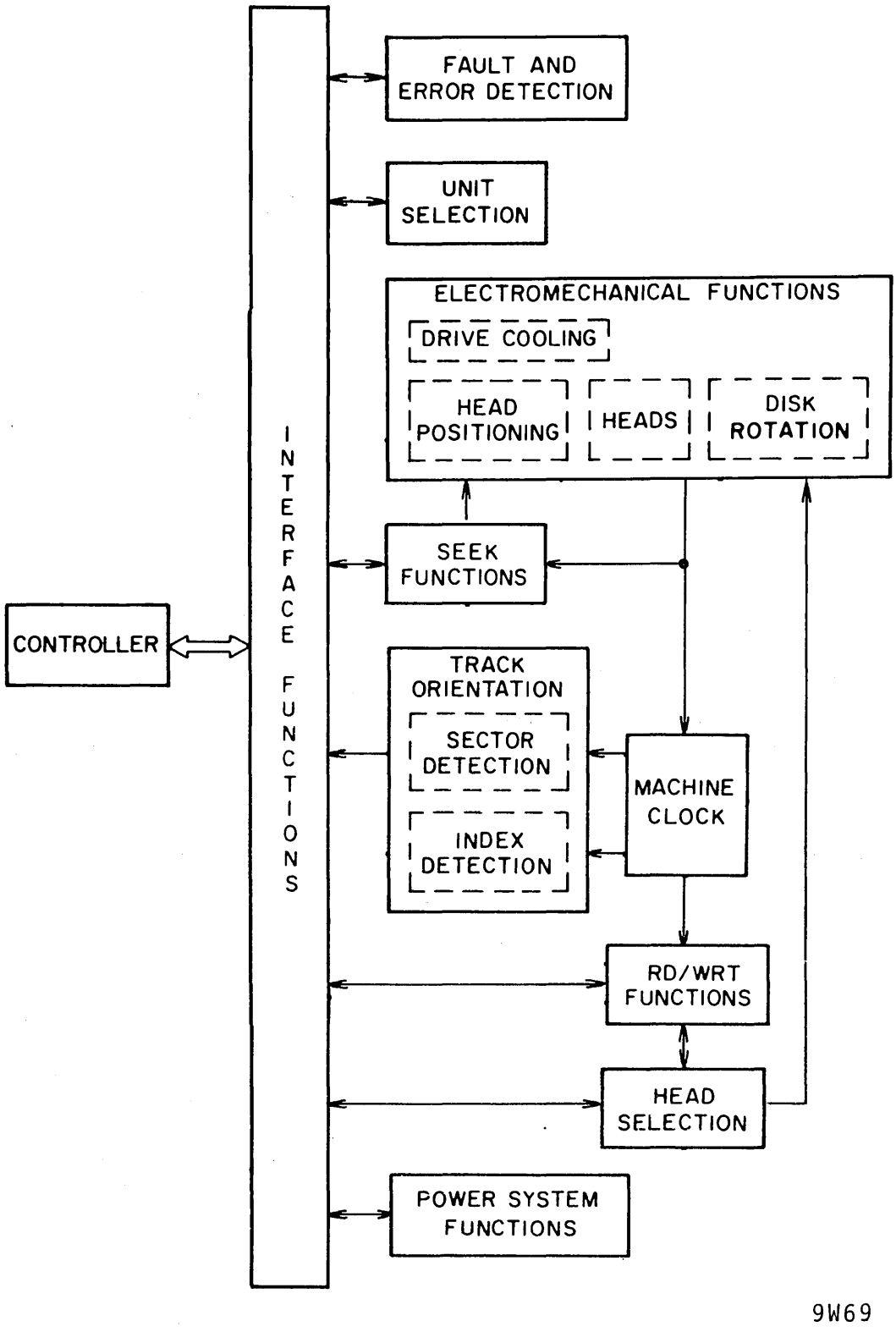


Figure 3-1. Drive Functional Block Diagram

The remainder of this discussion provides further description of the power system and is divided into the following areas:

- Power Distribution - Describes how the power is distributed to the drive circuitry.
- Local/Remote Power Sequencing - Explains how the drive may be powered up either at the drive or the controller.
- Power On Sequence - Describes how power is applied to the drive motor and the heads load sequence initiated.
- Power Off Sequence - Describes how the heads are unloaded and the drive motor stopped.
- Emergency Retract - Explains sequence performed when conditions exist requiring the heads be unloaded immediately to avoid damage to them or the disk pack.

POWER DISTRIBUTION

Power distribution consists of routing power to the various elements in the power supply and rest of the drive so that the power on sequence can be performed. The distribution is controlled by circuit breakers located within the power supply. These circuit breakers also provide overload protection for their associated voltages. The power distribution circuits are shown on figure 3-2 and basic operation is explained in the following.

Site main ac power is input to the power supply via the MAIN AC circuit breaker. When this breaker is closed, it applies power to the HOUR meter. It also provides the input to the drive motor control triacs; however, the motor does not start until the power on sequence.

Closing CB2 applies power to T3 and enables +20Y. With +20Y available, the transformers control triacs are enabled and power is applied to transformers T1 and T2 and the blower motor. These transformers provide inputs to the rectifier and capacitor board (_YEN), which in turn produces the dc voltages. The dc voltages are applied to the rest of the drive when their associated circuit breakers are closed.

When all circuit breakers are closed, the drives power on sequence can begin.

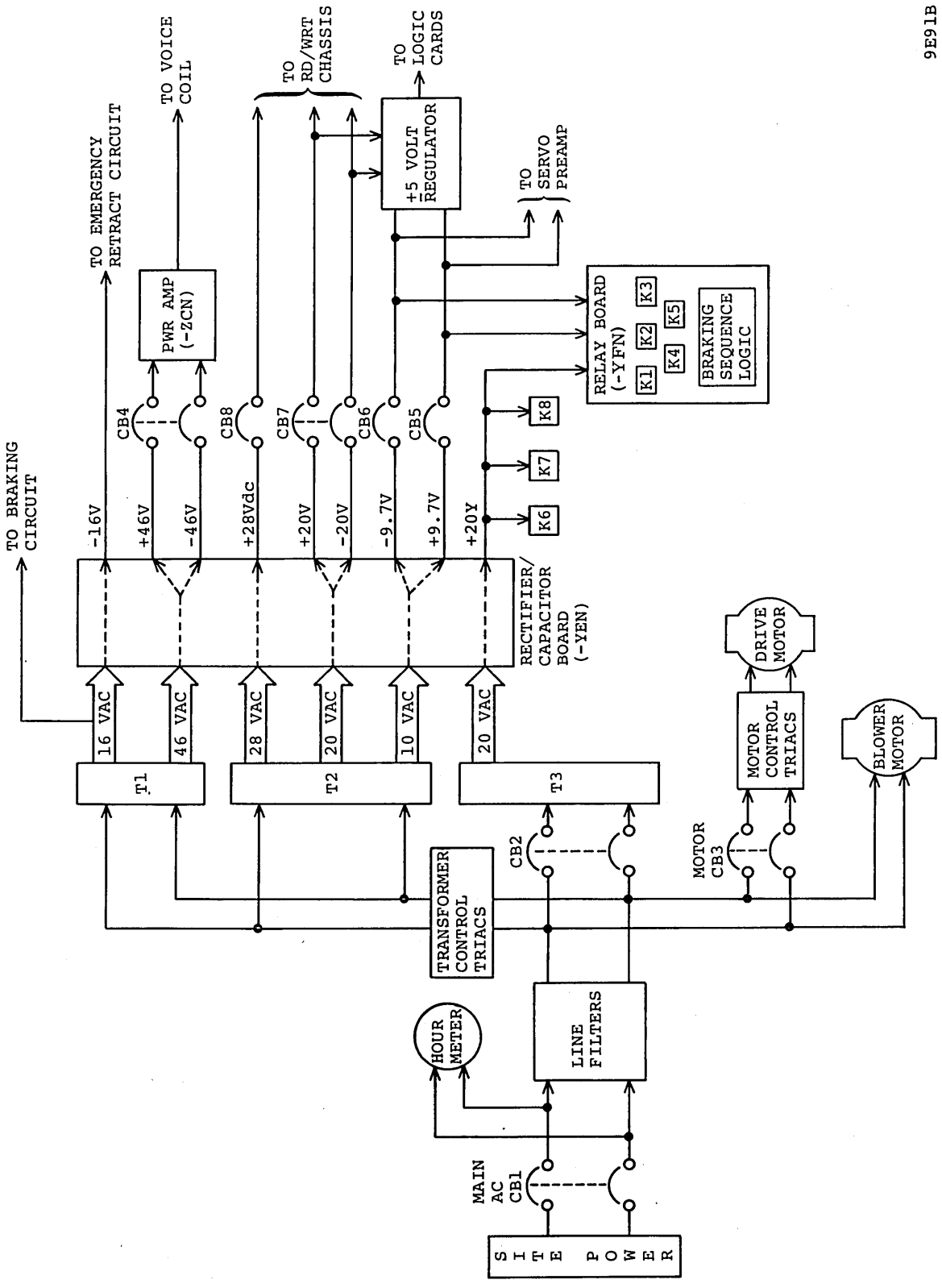


Figure 3-2. Power Distribution

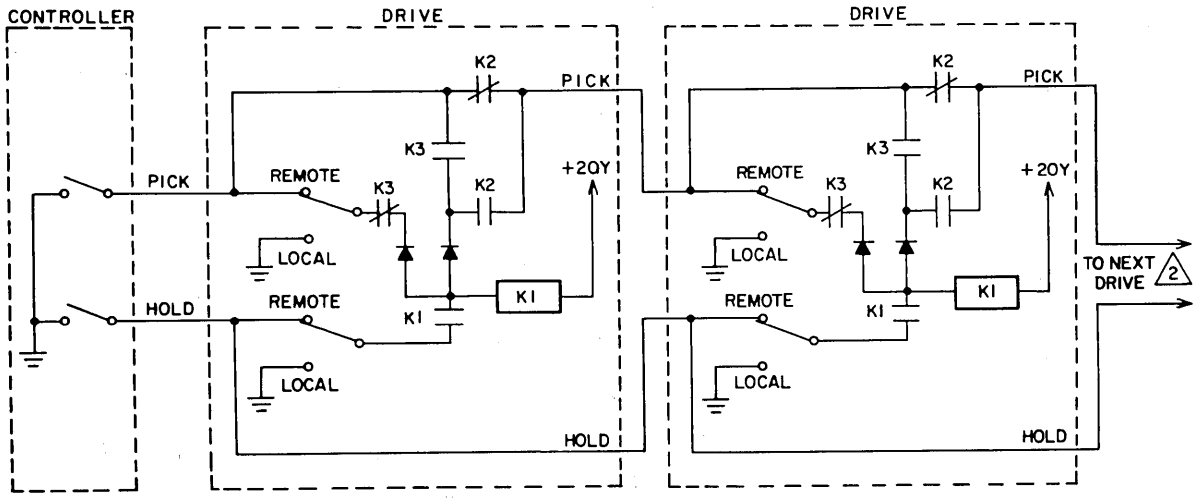
LOCAL/REMOTE POWER SEQUENCING CONTROL

General

The power on and off sequence of each drive can be controlled either locally or remotely depending on the setting of its LOCAL/REMOTE switch. When this switch is set to LOCAL, the sequences are initiated at the drive. When the switch is set to REMOTE, the sequences are initiated at the controller.

The LOCAL/REMOTE switch is located on the power supply control panel and controls the mode of operation by determining how the drives sequence power relay (K1) is energized and deenergized. This relay works in conjunction with the drives START switch to control the power on and off sequences.

Figure 3-3 shows the LOCAL/REMOTE power sequencing control circuits. The operation of these circuits in both local and remote modes is explained in the following paragraphs.



NOTE: 1. ALL RELAYS SHOWN IN THEIR NORMAL POWER OFF CONDITION.
2 TERMINATED AT LAST DRIVE IN DAISY CHAIN.

9E92C

Figure 3-3. Local/Remote Power Sequencing Control Circuits

Local Control

When the drive is in the local mode, the sequence power relay (K1) energizes whenever +20Y is available. This voltage is available whenever the MAIN AC circuit breaker (CB1) and +20Y circuit breaker (CB2) are closed. In this mode, the power on sequence begins when the START switch is pressed (providing all circuit breakers are closed). The power off sequence is initiated by pressing the START switch to extinguish the indicator. Figure 3-4 is a flowchart of the local power control sequence.

Remote Control

If the drive is in remote mode, the power sequence relay (K1) is energized by the power sequence signals (Pick and Hold) from the controller. Therefore, even if the START switch is pressed, the power on sequence does not begin until the power sequence signals go active and energize the sequence power relay.

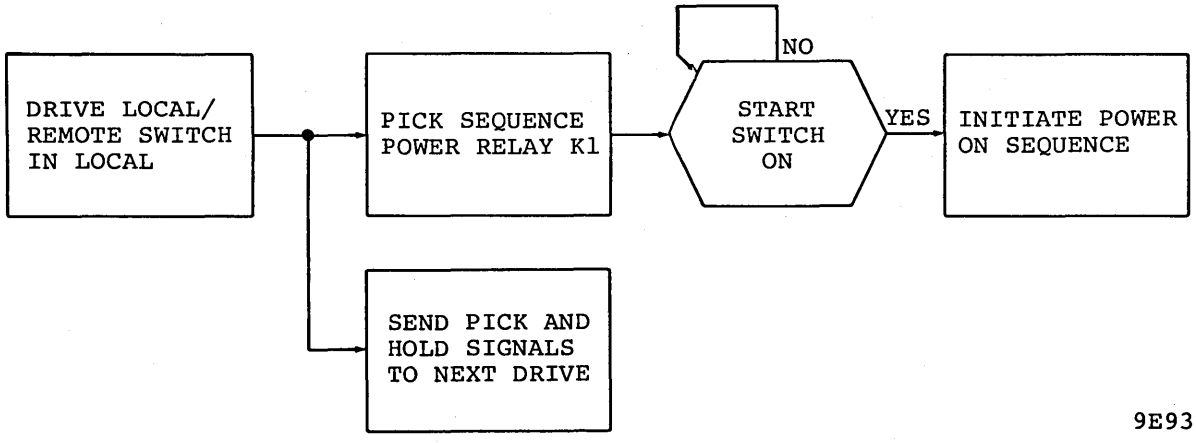


Figure 3-4. Local Mode Power Sequencing

It is then possible to power up drives sequentially in a system where the power sequence lines are connected in a daisy chain. A sequential power up prevents the current surge that occurs if a number of drives are powered up simultaneously.

Only the drives in the Remote mode with their START switches on (lighted) are involved in the power up. Those drives in Local mode or with the START switches off (light extinguished) are not involved in the power up and have no effect on it.

The sequential power up occurs because each drive involved waits until its spindle is up to speed (K3 energized) before passing the sequence signals to the next drive in the daisy chain. If a drive is not involved (Local mode or START switch off) it passes the sequence signals to the next drive without delay. This continues until all drives in Remote mode with START switch on are powered up. The signals are terminated at the last drive in the daisy chain.

The drives are powered down either individually by pressing the START switches, or all at once by deactivating the sequence signals at the controller.

Figure 3-5 is a flow chart of the remote power control sequence.

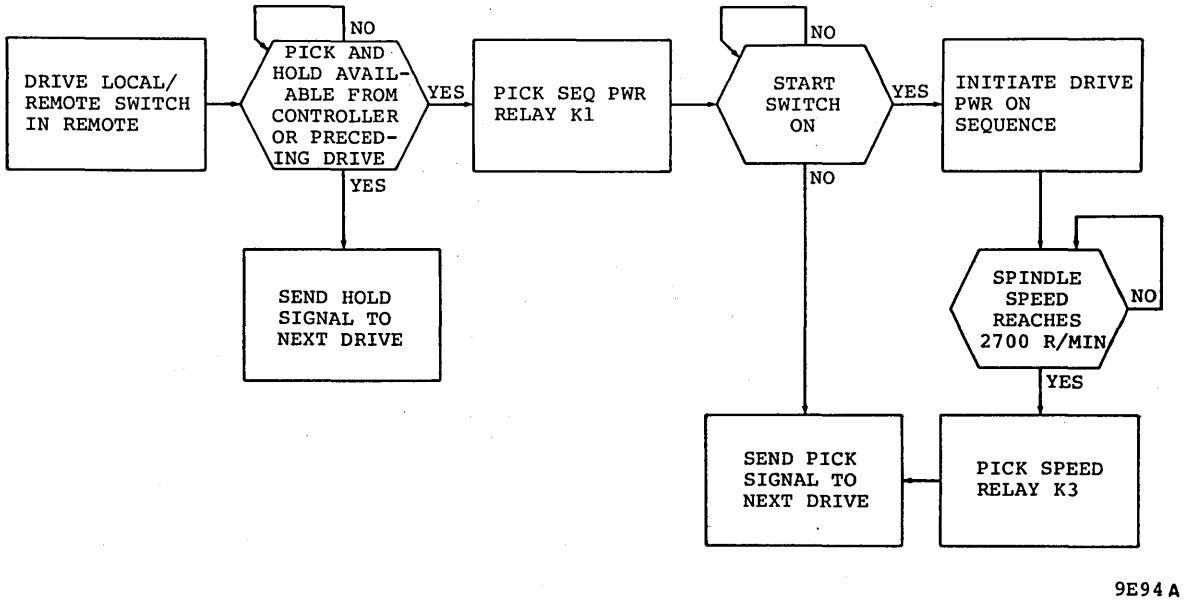


Figure 3-5. Remote Mode Power Sequencing

POWER ON SEQUENCE

The power on sequence starts the drive motor and initiates loading of the heads. The following description pertains to non-VDE units. The power on sequence description for VDE units is provided in section 3A.

The sequence is initiated by pressing the START switch on the operator control panel. If all circuit breakers are closed, the disk pack is installed and the pack access cover is closed, pressing the START switch energizes the Start relay (K2).

The Start relay causes the Motor relay (K4) to energize and enable the motor control triacs. This applies power to the drive motor causing it to start and also causes the READY light on the operator control panel to start flashing. The drive motor transfers motion to the spindle via the drive belt and the disk pack starts to rotate.

When the speed sensing circuits indicate the spindle speed is about 2700 r/min, the Speed relay (K3) energizes. This does two things: (1) energizes the Emergency Retract relay (K7) and (2) triggers the 10 second Load Delay one shot.

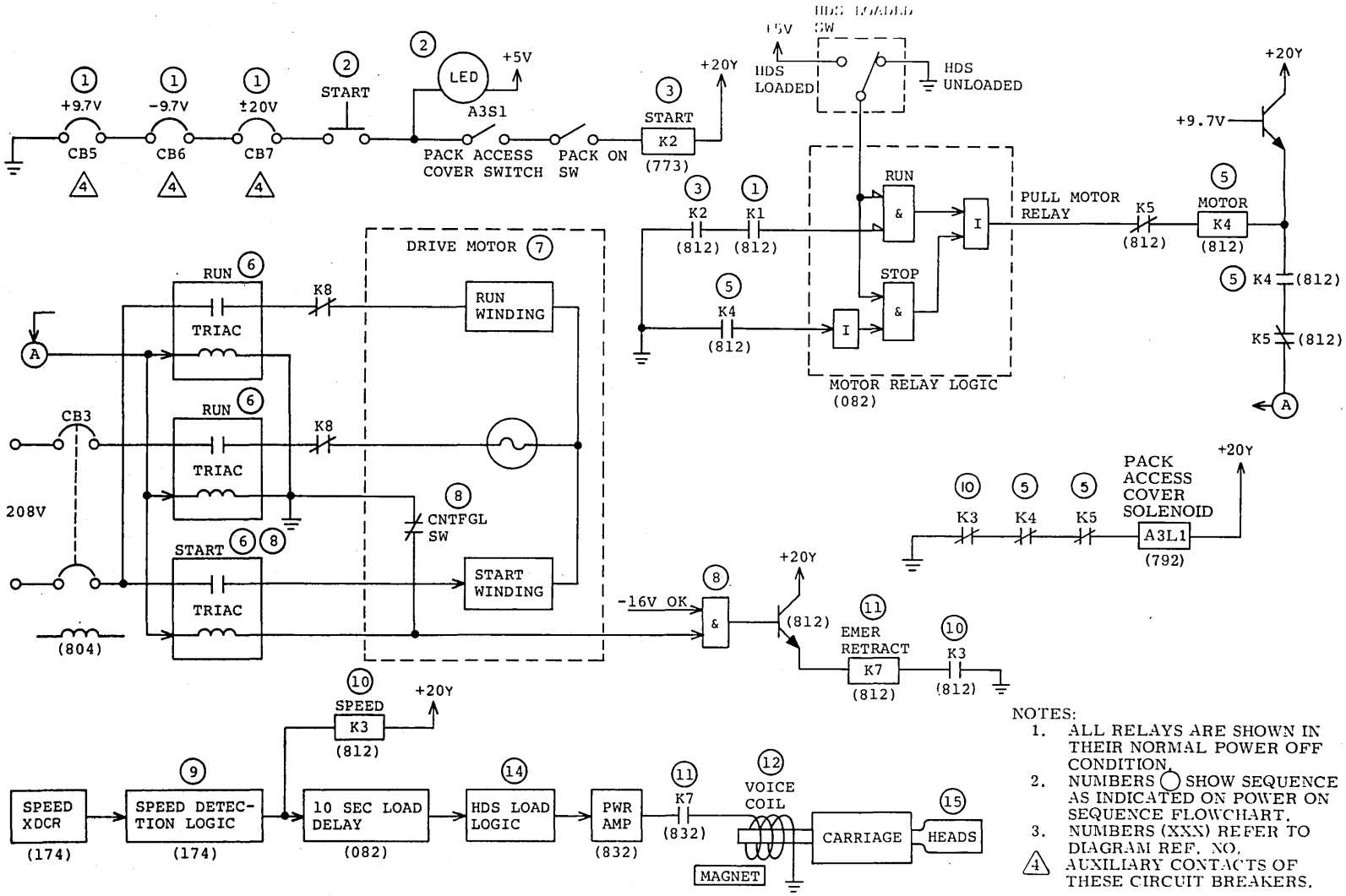
Energizing the Emergency Retract relay connects the power amplifier to the voice coil and connects the Emergency Retract capacitor to -16 volts. This prepares the voice coil to respond to commands from the servo logic and charges the Emergency Retract capacitor so it is ready for an emergency retract condition.

The Heads Load Delay allows the spindle time to reach 3000 r/min before enabling the heads load logic. When the delay times out, the heads load sequence is initiated causing the heads to load. The READY light stops flashing and remains lighted after the heads are loaded. The heads load sequence is covered in the discussion on Load Seeks.

Figure 3-6 shows the circuitry involved in the power up sequence and figure 3-7 is a flow chart of the operation.

POWER OFF SEQUENCE

The power off sequence unloads the heads and stops the drive motor. The following description applies to all non-VDE units. The power off sequence description for VDE units is provided in section 3A.



NOTES:
1. ALL RELAYS ARE SHOWN IN THEIR NORMAL POWER OFF CONDITION.
2. NUMBERS ◯ SHOW SEQUENCE AS INDICATED ON POWER ON SEQUENCE FLOWCHART.
3. NUMBERS (XXX) REFER TO DIAGRAM REF. NO.
4. AUXILIARY CONTACTS OF THESE CIRCUIT BREAKERS.

9E199B

Figure 3-6. Power On Circuit

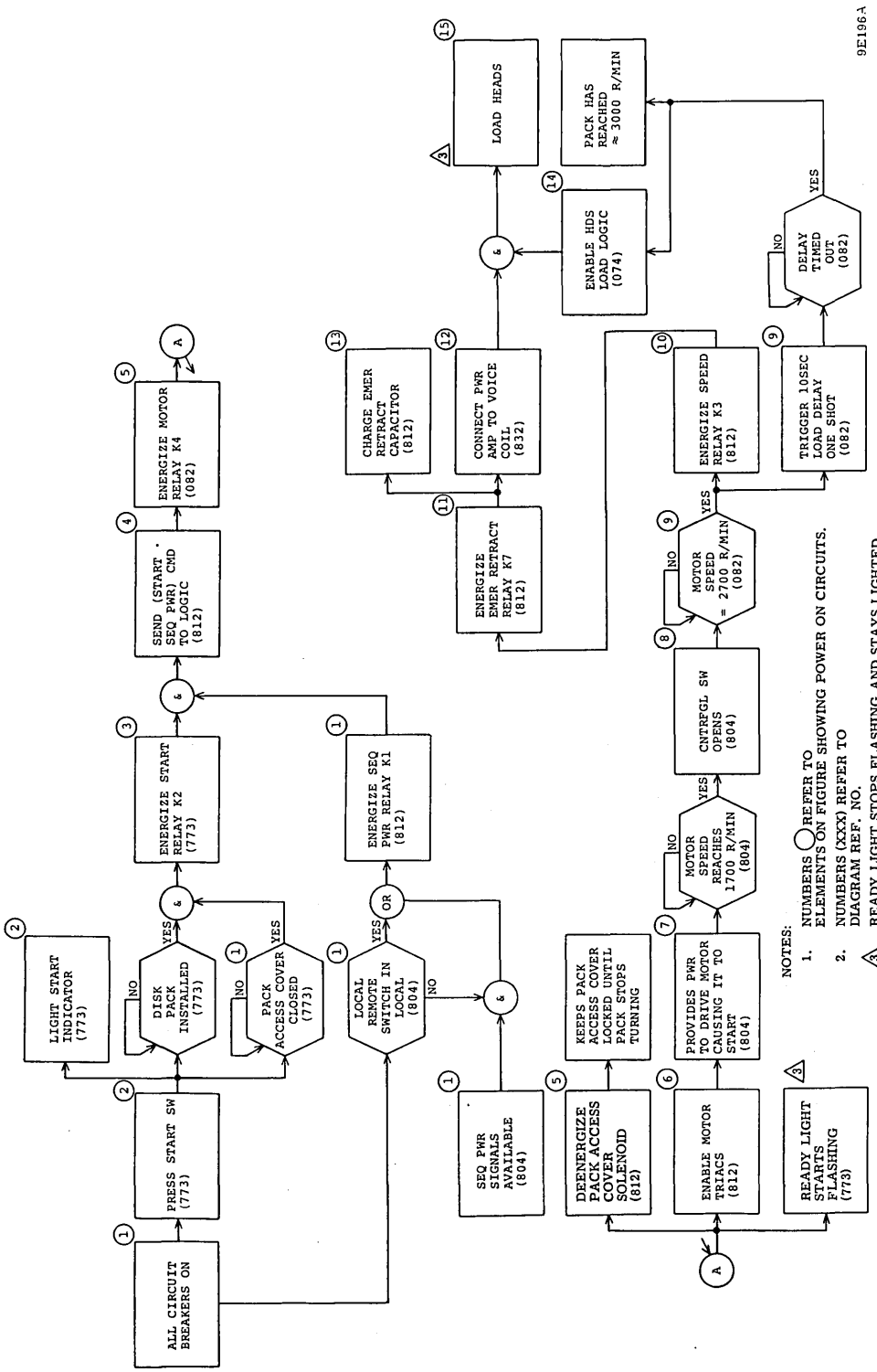


Figure 3-7. Power On Sequence Flow Chart

The sequence begins when either the START switch is pressed or the Sequence Power relay (K1) is de-energized. In either case the Start relay (K2) deenergizes and the RTZ logic is enabled (refer to discussion on Return to Zero Seeks). This causes the heads to move in the reverse direction and the READY light to start flashing.

When the Heads Unloaded switch indicates the heads are unloaded, the RTZ is disabled and the motor relay (K4) is deenergized. Deenergizing the Motor relay (K4) removes power from the drive motor and enables the braking logic. Enabling the brake logic initiates the braking sequence.

The braking sequence begins by energizing the Brake Power relay (K5) which in turn energizes the Brake relay (K8). The Brake relay applies -16 Vdc across the run winding of the drive motor. The -16 Vdc causes a current to flow through the winding and the magnetic field generated by this current has a braking effect on the motor.

The motor slows down and when its speed is less than 2700 r/-min, the Speed relay (K3) deenergizes. This in turn causes the Emergency Retract relay (K7) to deenergize thus disconnecting the power amplifier from the voice coil.

The Brake Power and Brake relays deenergize approximately 30 seconds after the start of the braking sequence. This removes braking voltage from the drive motor, which by this time is stopped. This also extinguishes the READY light and deenergizes the pack access solenoid thus allowing the pack access cover to be opened.

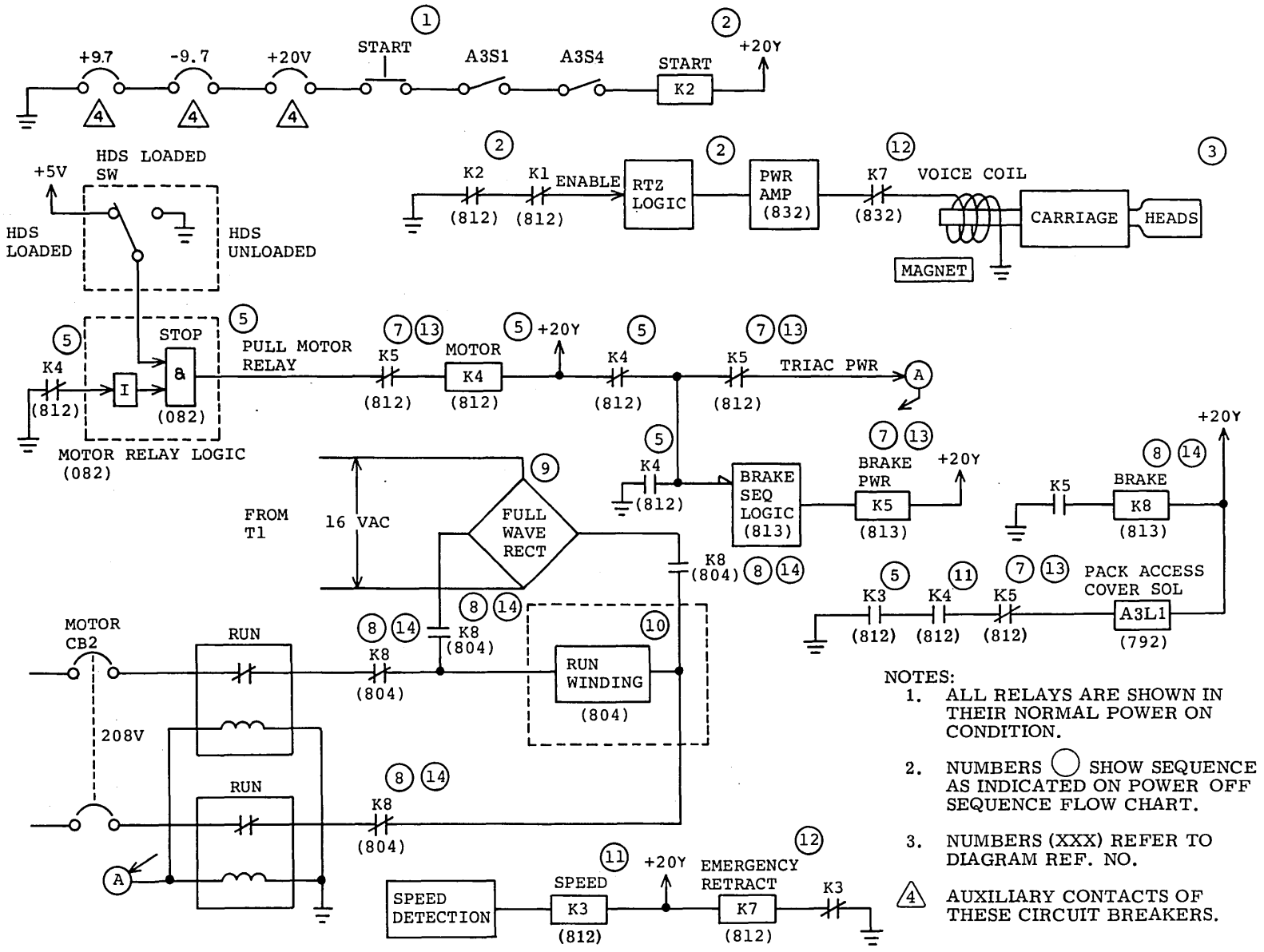
Figure 3-8 shows the circuitry involved in the power off sequence and figure 3-9 is a flow chart of the operation.

EMERGENCY RETRACT

The emergency retract function provides an emergency means of retracting the heads from the pack area. This sequence is initiated if disk speed is reduced or if conditions indicate that it may be reduced. Failure to retract the heads under these conditions could result in head crash and subsequent damage to the heads and disk pack.

Any of the following conditions initiate an emergency retract sequence:

- Loss of AC Power - If site ac power is lost, all dc power is also lost. This power loss includes +20Y, +9.7, and -16, any of which cause an emergency retract to occur.



NOTES:

1. ALL RELAYS ARE SHOWN IN THEIR NORMAL POWER ON CONDITION.
2. NUMBERS ◯ SHOW SEQUENCE AS INDICATED ON POWER OFF SEQUENCE FLOW CHART.
3. NUMBERS (XXX) REFER TO DIAGRAM REF. NO.
4. AUXILIARY CONTACTS OF THESE CIRCUIT BREAKERS.

9E197A

Figure 3-8. Power Off Circuits

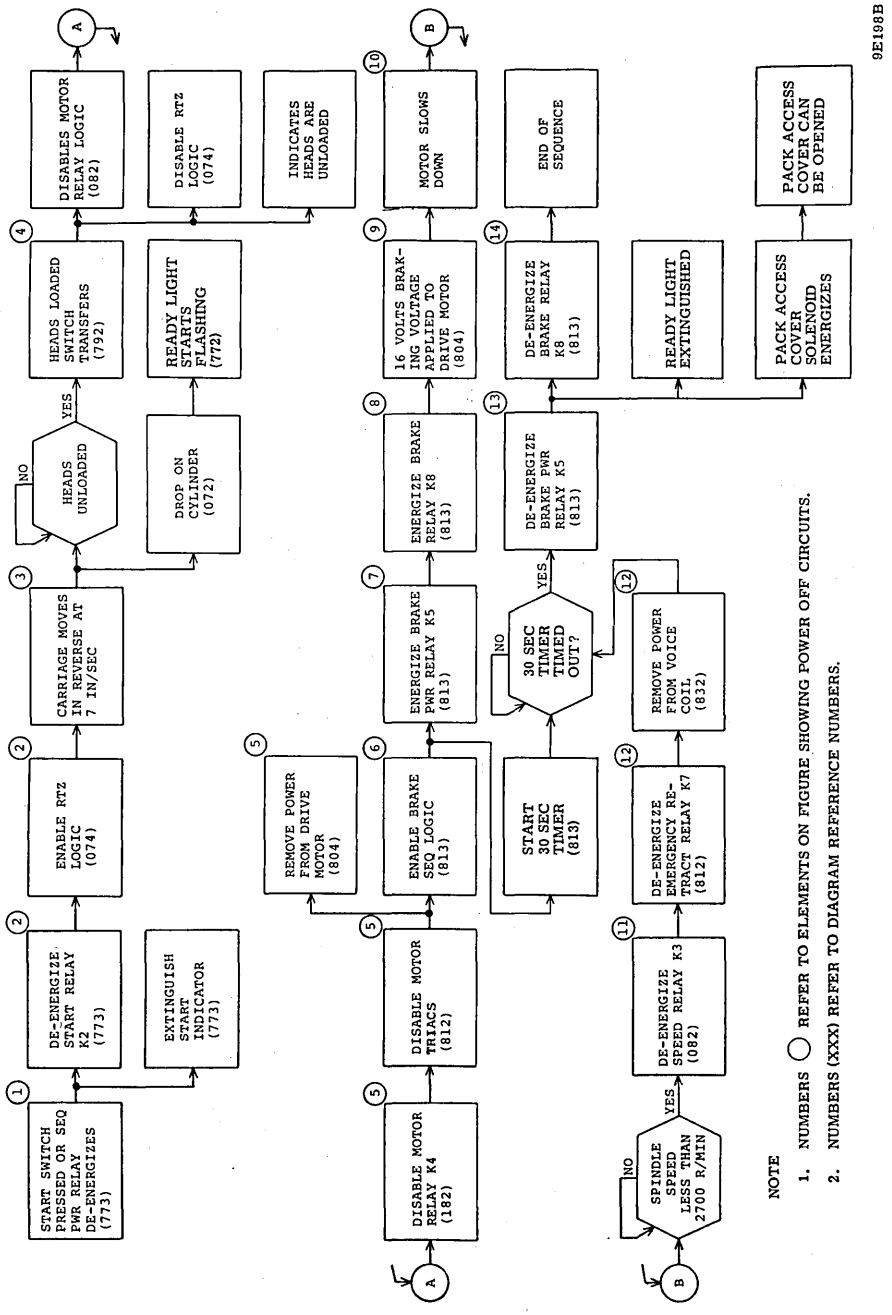


Figure 3-9. Power Off Sequence Flow Chart

- Loss of +20Y, -16, or +9.7 Vdc - Losing any of these voltages directly causes the emergency retract relay to deenergize thus starting the emergency retract sequence.

- Loss of Speed - If drive motor speed drops below 2700 r/-min, the speed detection circuits cause the emergency retract capacitor to deenergize.

- Drive Motor Thermal Overload - If the drive motor overheats, a thermal relay within the motor opens. This results in the motor circuit breaker opening and removing power from the drive motor. The motor then slows down and the loss of speed causes an emergency retract.

Figure 3-10 shows the circuitry involved in the emergency retract sequence.

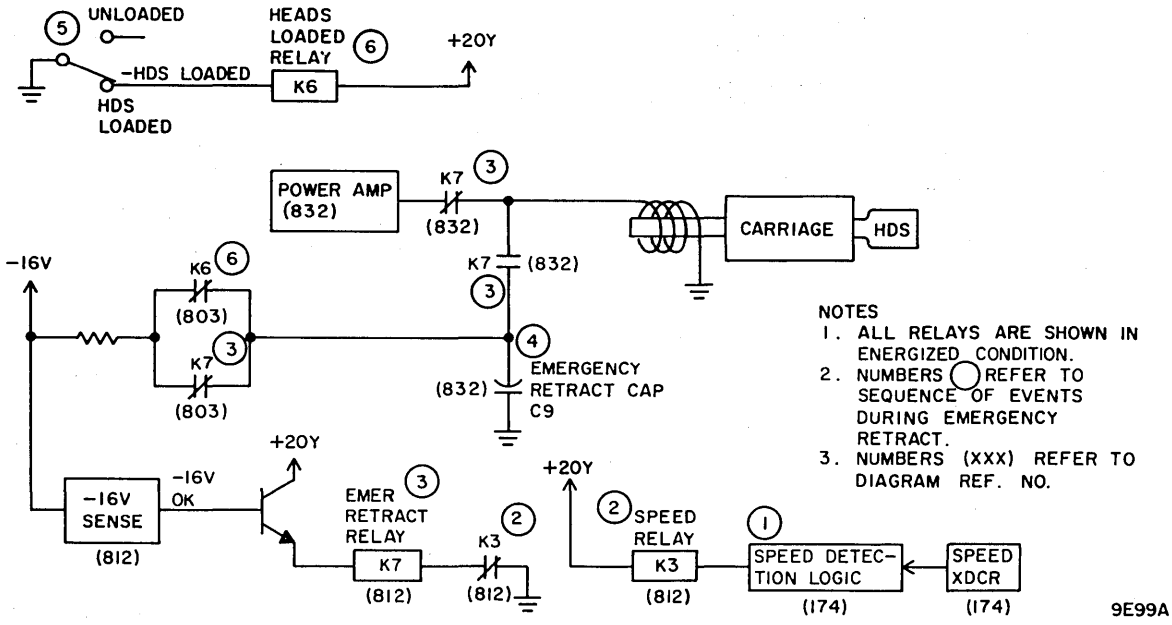


Figure 3-10. Emergency Retract Circuits

ELECTROMECHANICAL FUNCTIONS

GENERAL

Certain drive functions are a result of the electromechanical devices working under the control of logical circuitry. These functions include disk pack rotation, head positioning, and drive cooling and ventilation.

Disk pack rotation is performed by the disk pack rotation mechanism, which is controlled by the power system. The purpose of disk pack rotation is to create a cushion of air on the disk surfaces. The cushion of air allows the heads (which read and write the data) to move over the disk surfaces without actually contacting them.

The heads are positioned over specific data tracks on the disk surface by the head positioning mechanism. The mechanism is controlled by the servo circuits (refer to discussion of Seek Operations) and the power system.

Drive cooling and ventilation is provided by the air flow system. The main element in this system is the blower motor which receives its power from the power system.

Figure 3-11 is a block diagram showing each of the previously discussed mechanisms. A more detailed physical and functional description of each is provided in the following discussions.

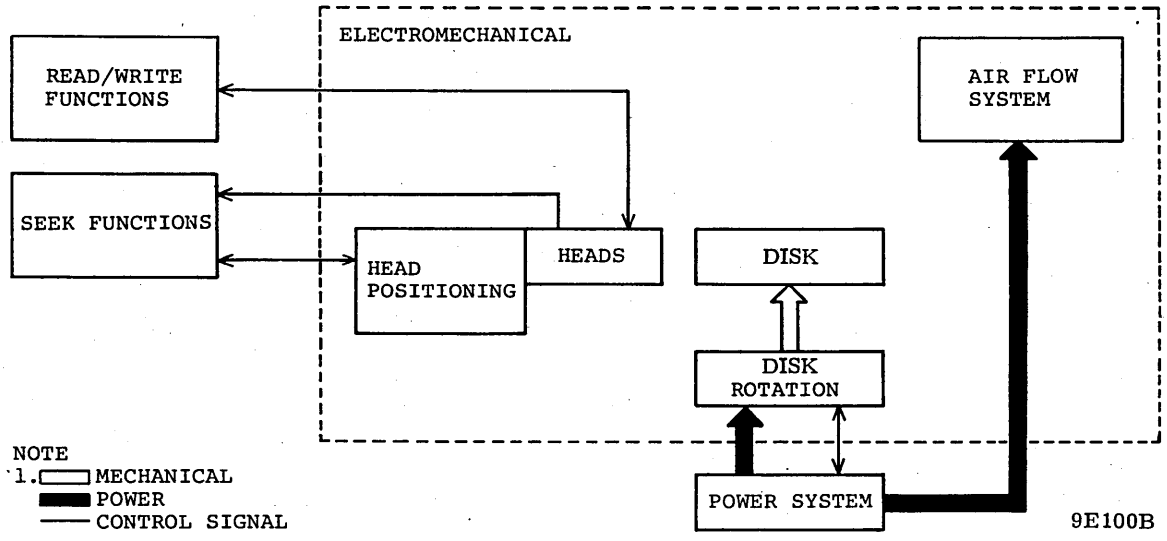


Figure 3-11. Electromechanical Functions Block Diagram

DISK PACK ROTATION

General

The disk pack must be rotating fast enough to allow the heads to fly before any drive operation can be performed. The following mechanisms work in conjunction with the power system to control disk pack rotation (refer to figure 3-12):

- Drive Motor - Provides rotating motion for the spindle and disk pack.
- Spindle - Provides rotating mounting surface for disk pack.
- Parking Brake - Holds spindle while pack is being installed.
- Speed Sensor - Generates pulses that are used to determine speed of spindle.
- Pack On Switch - Actuated when pack is installed on spindle, this device must indicate the pack is installed before the power on sequence can be performed.

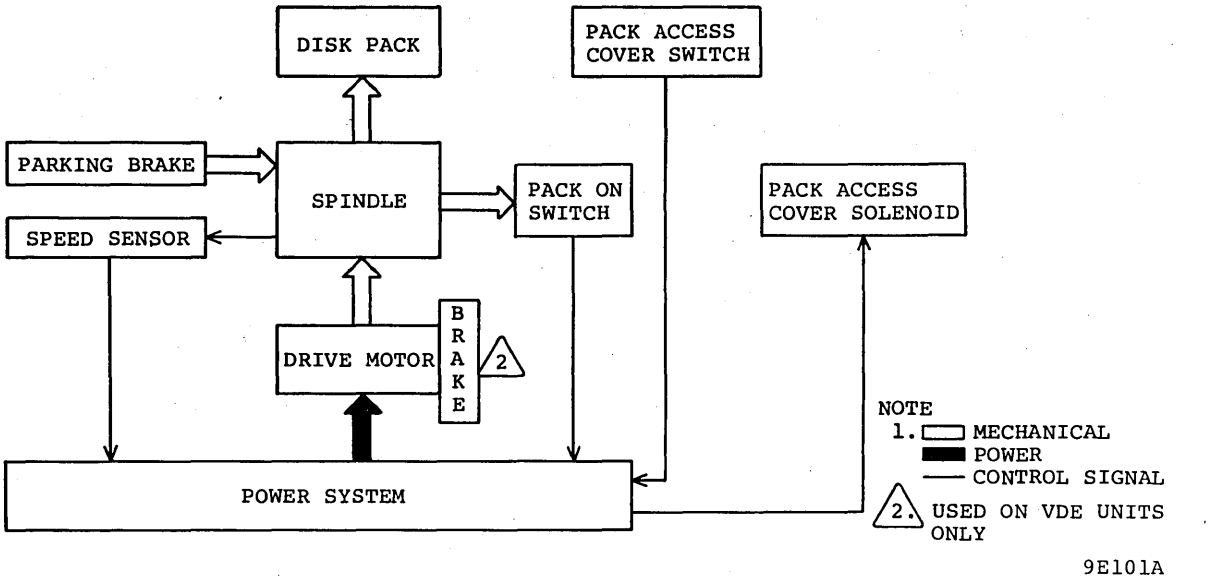


Figure 3-12. Disk Pack Rotation Functional Block Diagram

- Pack Access Cover Switch - Ensures that pack access cover is closed before disk pack rotation begins.

- Pack Access Cover Solenoid - Prevents pack access cover from being opened while pack is rotating.

These mechanisms are further described in the following paragraphs.

Drive Motor

The drive motor provides the rotational energy required to rotate the spindle and disk pack. The motor is mounted on a movable plate which in turn is mounted on the underside of the deck casting (refer to figure 3-13).

Motion is transferred from motor to spindle via the drive belt. This belt connects the pulley on the shaft of the drive motor to the pulley on the lower end of the spindle.

The springs attached between the motor mounting plate and deck casting, maintain enough tension on the plate to keep the drive belt tight. The spring tension is adjustable so tension on the belt can be adjusted to provide the best coupling between drive motor and spindle pulleys.

The motor starts during the power on sequence when power is applied to its start and run windings (refer to Power On Sequence discussion). The start winding helps the run winding start the motor in motion and get it up to speed. When the motor speed reaches approximately 1700 r/min, the start winding is no longer needed and a centrifugal switch (within the motor) opens thus disabling the start winding. The motor continues to accelerate (using only its run winding) until it reaches its maximum speed (approximately 3600 r/min). This speed is maintained until power is removed from the motors run winding (refer to discussion on Power System).

The temperature of the motor is monitored by the thermal switch. If the motor overheats, this switch opens resulting in loss of power to the drive motor. The motor slows down causing an emergency retract and power off sequence. The drive motor cannot be restarted until it cools off, thereby causing the thermal switch to close.

Spindle

The spindle (refer to figures 3-13 and 3-14) provides the means of mounting the disk pack within the drive and also of rotating the pack when the drive motor is energized.

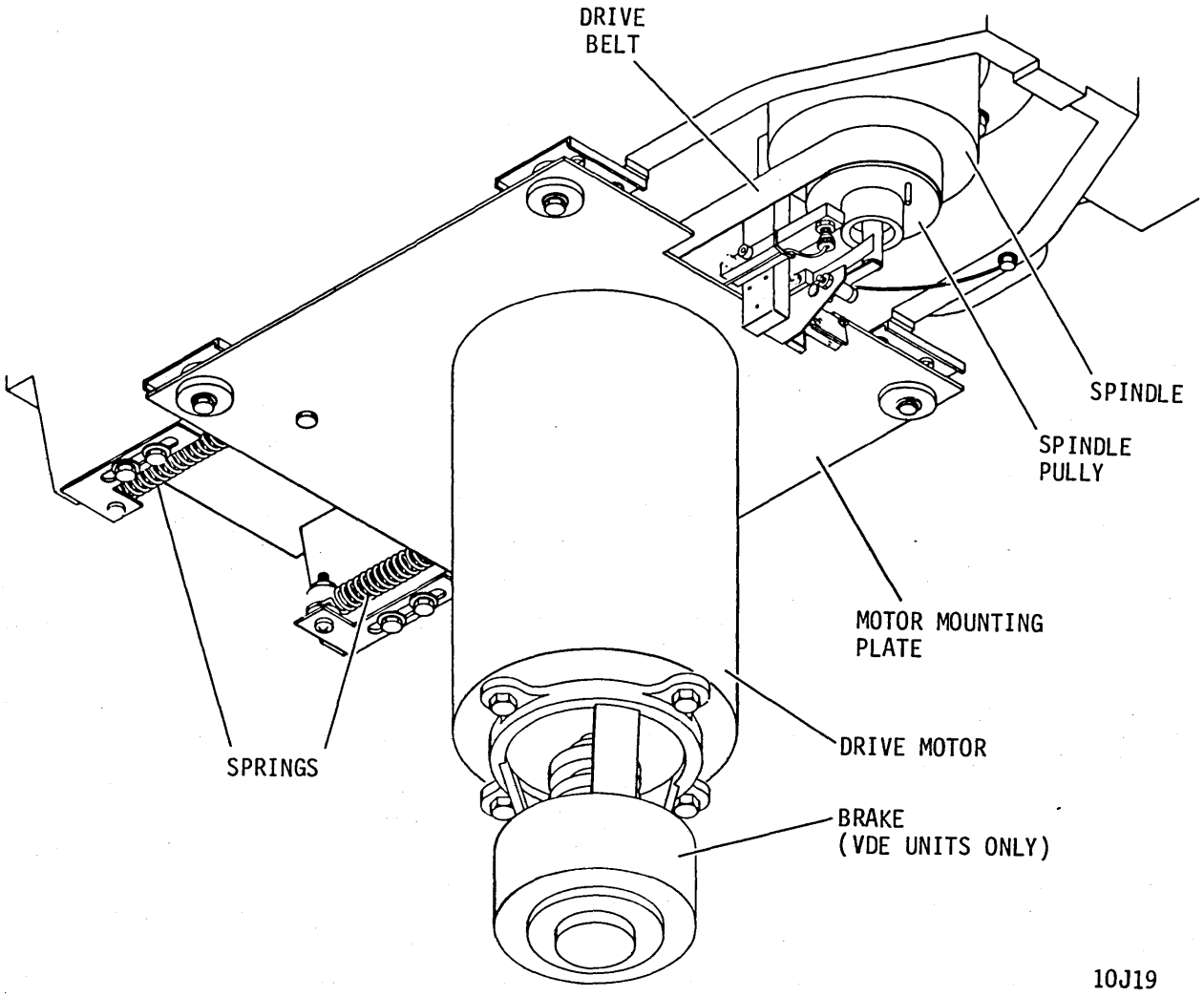


Figure 3-13. Drive Motor Assembly

When the pack is mounted, its lower disk rests on the pack mounting plate. This plate connects to a shaft which in turn connects to the pulley on the lower end of the spindle. When the drive motor starts, it transfers motion to this pulley via the drive belt and causes the pack mounting plate and disk pack to rotate.

The disk pack must be secured to the mounting plate with enough force so the two of them will rotate together. This force is provided by the lockshaft, which is a spring loaded shaft located within the spindle. When the pack is installed, the mounting screw on the bottom of the pack is threaded into the internal threads in the upper end of the lockshaft. As the pack is tightened down against the mounting plate, the springs holding down the lockshaft exert a downward force on the pack. When this force is sufficient, a release mechanism (in the handle of the disk pack top dust cover) releases the top dust cover from the pack. The pack is now installed and will rotate whenever the drive is energized.

A ground spring (refer to figure 3-14) bleeds off any static electricity accumulating on the spindle.

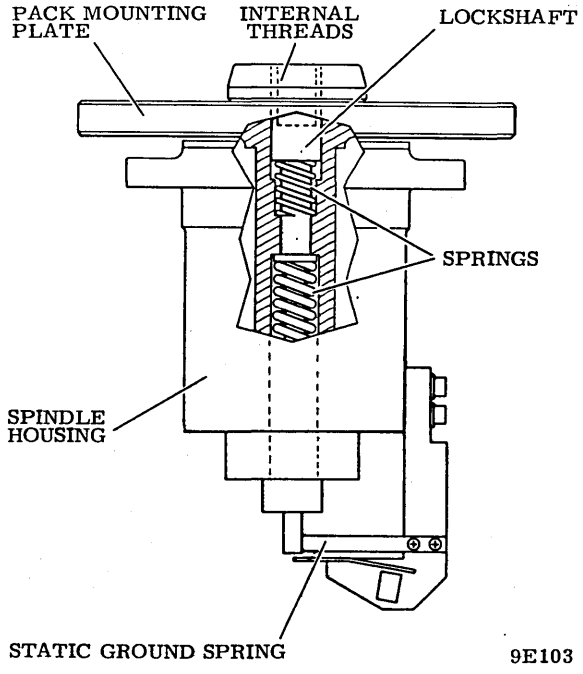


Figure 3-14. Spindle Assembly

Parking Brake

The parking brake (refer to figure 3-15) holds the spindle stationary whenever a disk pack is installed or removed. It is actuated by the disk pack top dust cover which contacts the brake actuator button. This causes the brake tooth to move up and engage a slot in the bottom of the spindle thus preventing the spindle from rotating. When the dust cover is removed, the actuator button is released, the brake tooth disengages, and the spindle is free to turn.

Speed Sensor

The speed sensor (refer to figures 3-16 and 3-17) is a device that generates signals used to determine if spindle speed is sufficient to allow the heads to fly. The sensor is mounted beneath the spindle and consists of a small coil and core assembly. The coil has a current flowing through it and each time the pin mounted on the bottom of the rotating spindle aligns itself with the core of the coil, a signal is generated.

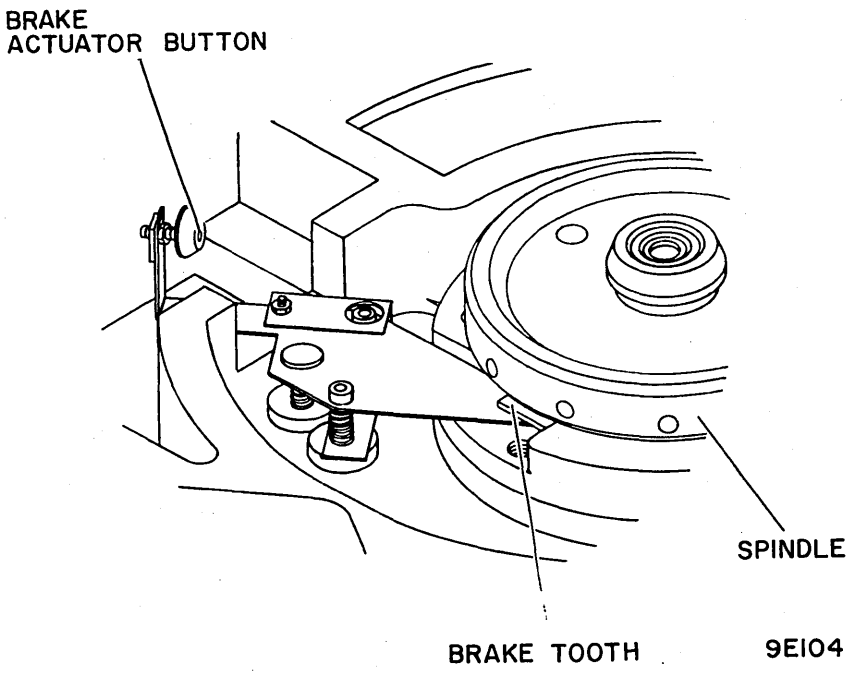


Figure 3-15. Parking Brake Assembly

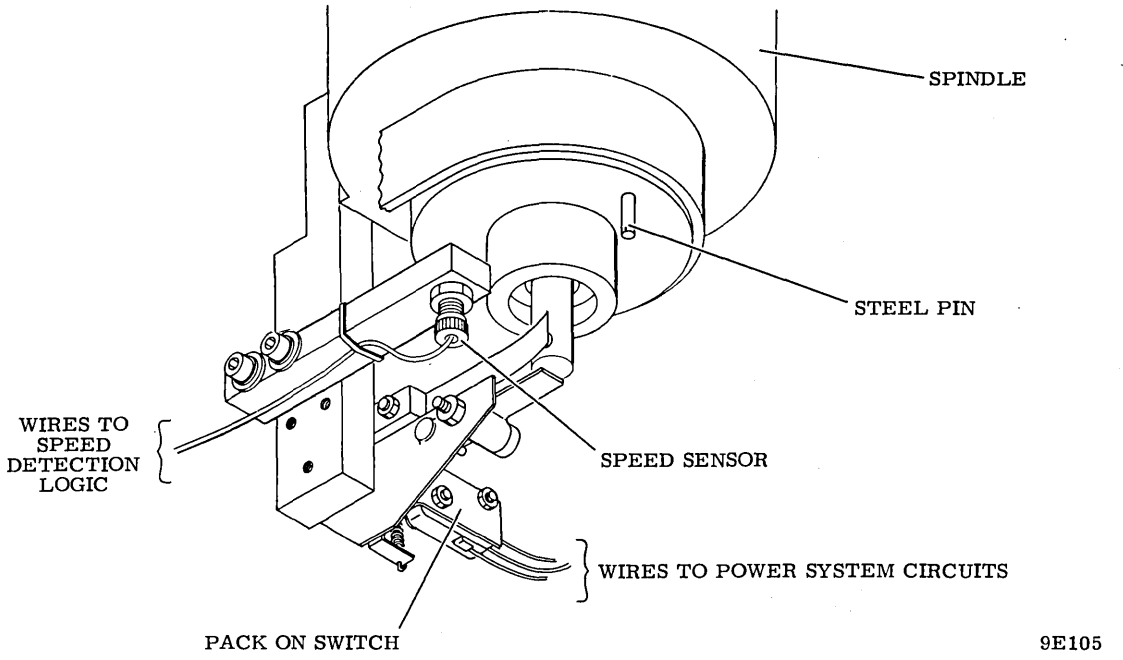


Figure 3-16. Speed Sensor and Pack On Switch Assemblies

The speed sensor logic monitors these signals and uses them to determine if spindle speed is at least 3000 r/min. When this speed is reached, the speed relay is energized; and it remains energized as long as this speed is maintained. However, if spindle speed drops below 3000 r/min the speed relay deenergizes (refer to discussion on Emergency Retract).

Pack On Switch

The disk pack must be securely installed on the spindle for the drive motor to run. This condition is ensured by the pack on switch. The switch is located beneath the spindle (refer to figure 3-18) and is actuated by the lockshaft when the pack is installed.

If the pack is not completely installed, the switch will not be closed and the drive motor will not start. If the pack comes loose during drive operation and the pack on switch opens, the power off sequence is initiated thus stopping the drive motor.

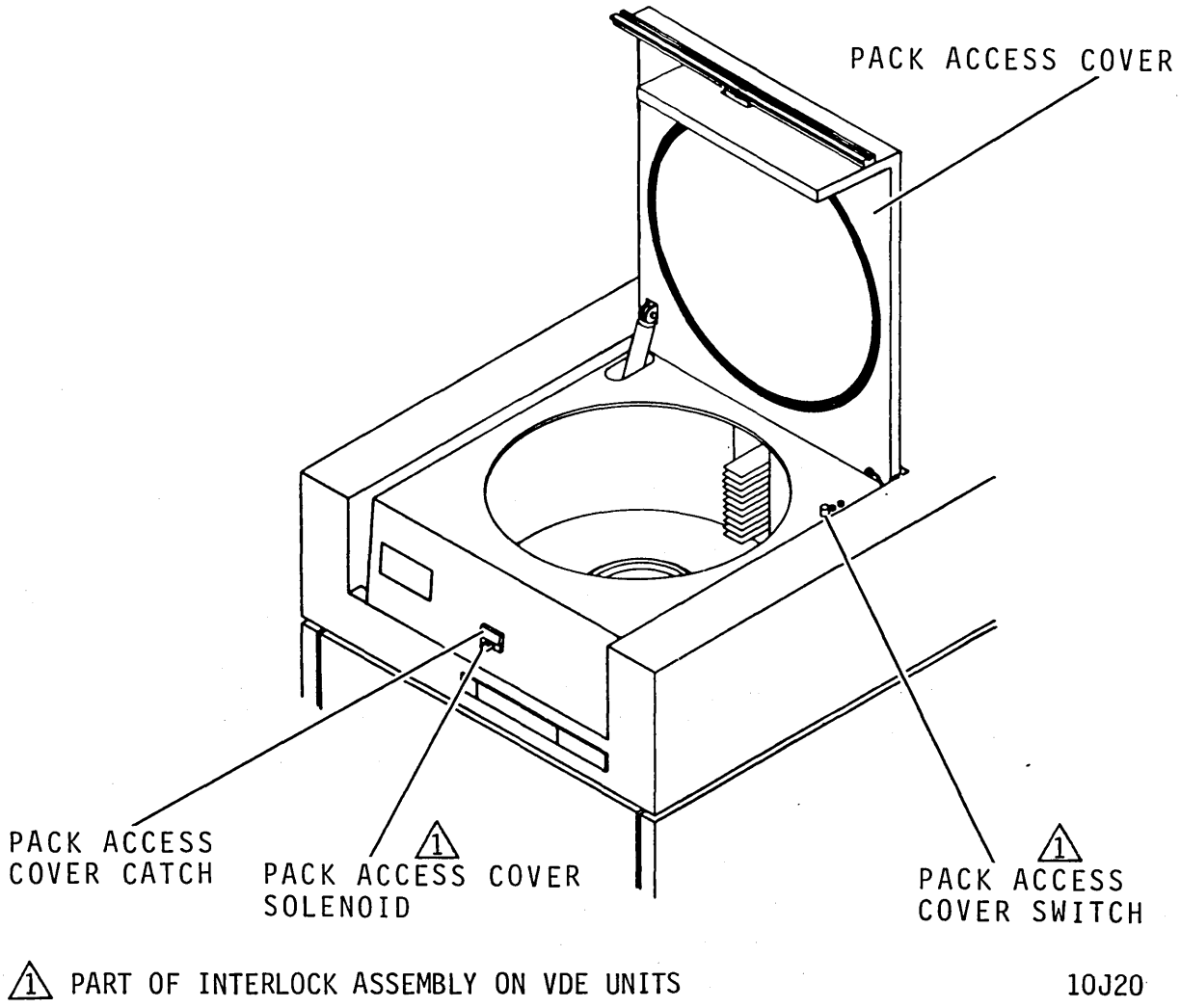


Figure 3-17. Pack Access Cover Switch and Solenoid

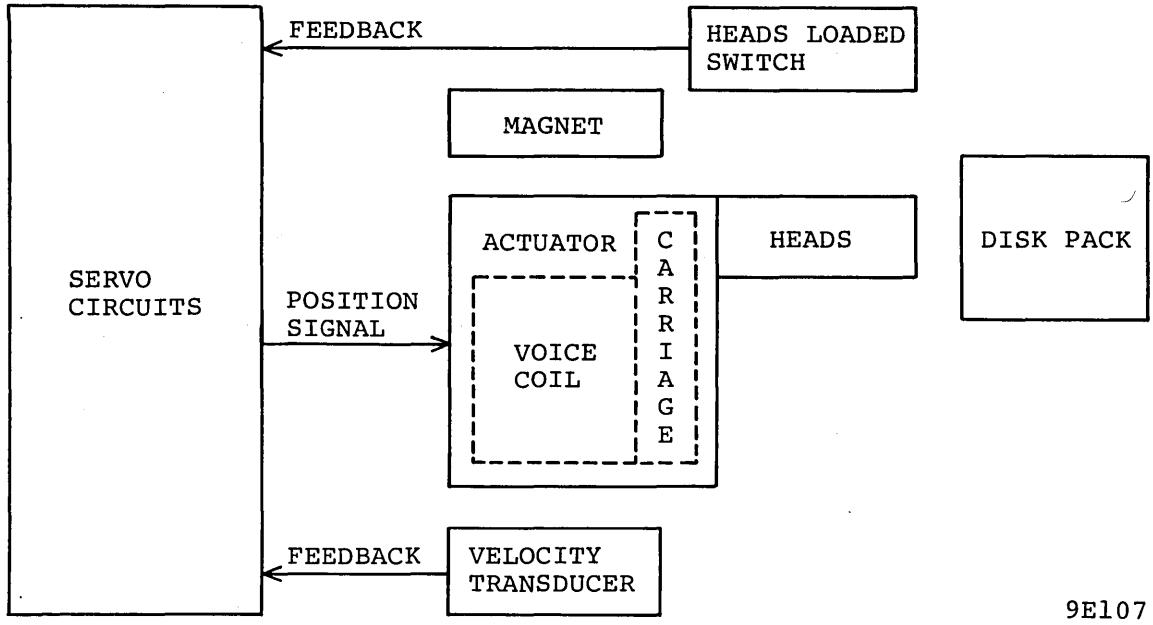


Figure 3-18. Head Positioning Functional Block Diagram

Pack Access Cover Switch

In addition to the pack on switch, the pack access cover switch (refer to figure 3-19) must be closed for the drive motor to run. This switch ensures that the pack access cover is closed.

Opening the switch has the same effect as opening the pack on switch.

Pack Access Cover Solenoid

If the drive is equipped with a pack access cover solenoid (refer to figure 3-17), the pack access cover can be opened only if the drive is in a standby condition, that is, with the circuit breakers on but the heads unloaded and the disk not rotating. The solenoid controls the operation of the pack access cover as follows.

During the power on sequence when the pack starts turning, the solenoid is deenergized and a spring pulls the solenoid arm upwards. This locks the pack access cover latch and prevents the cover from being opened.

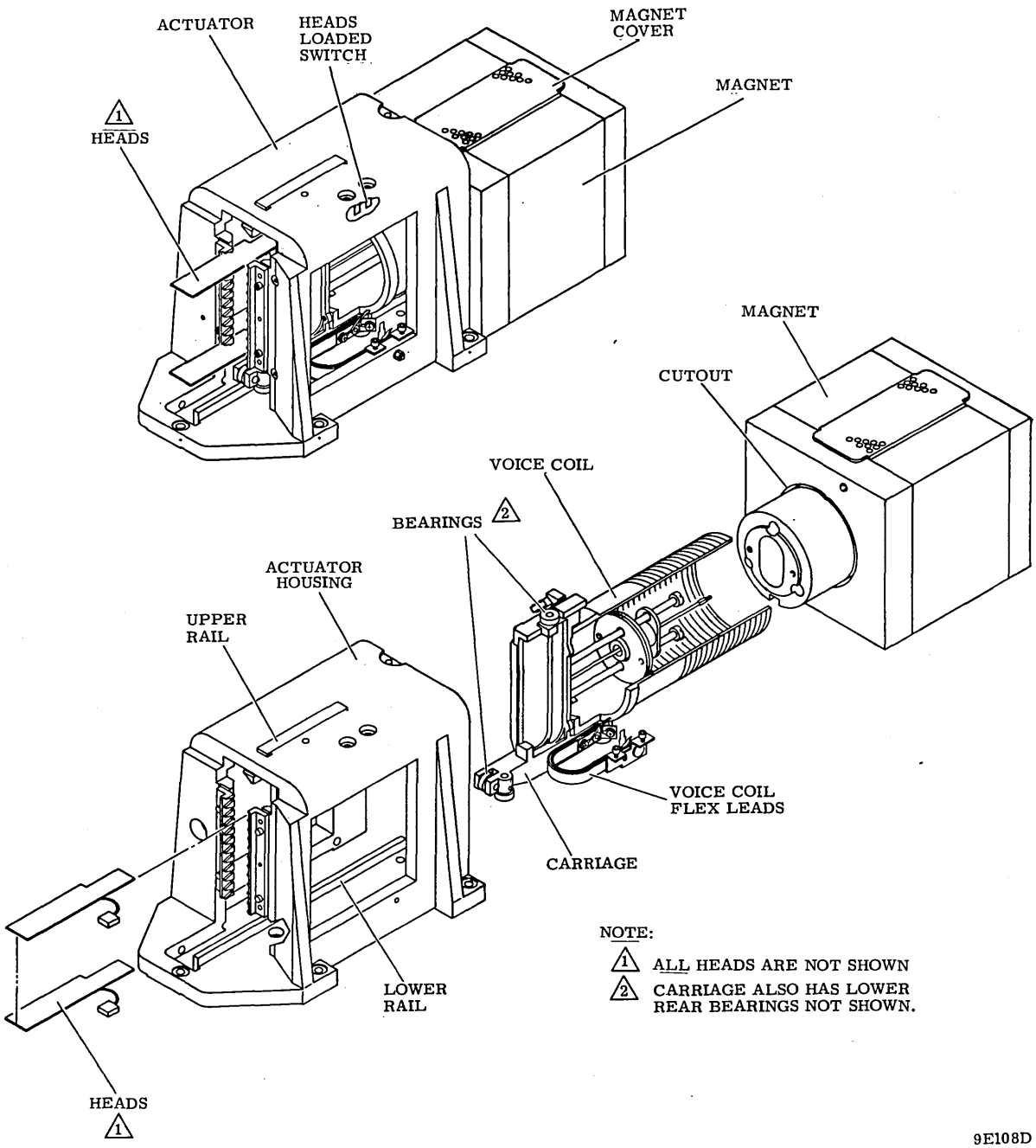


Figure 3-19. Actuator and Magnet Assembly

If the drive is in a power off condition with the disk pack stopped, the solenoid is deenergized and the arm is pulled down. This releases the pack access cover latch and allows the cover to be opened.

HEAD POSITIONING

General

Data is read from and written on the disk by the heads. However, the drive must position the heads over a specific data track on the disk before a read or write operation can be performed. Head positioning is performed by the head positioning mechanism.

This mechanism consists of the actuator, magnet, velocity transducer and heads loaded switch.

The actual positioning is performed by the actuator and magnet. The positioner is controlled by signals received from the servo circuits (refer to discussion on Seek Functions).

The velocity transducer and heads loaded switch provide signals that are used by the servo circuits in controlling head positioning.

Figure 3-18 is a functional block diagram of the head positioning mechanism. The following paragraphs provide further description of the elements shown on this figure.

Actuator and Magnet

General

The actuator and magnet (refer to figure 3-19) work together to position the heads. The following paragraphs provide a physical and functional description of the actuator and magnet assemblies.

Actuator and Magnet Physical Description

The actuator and magnet are located on the rear half of the deck (refer to figure 3-19).

The actuator consists of the carriage and voice coil both of which are contained in the actuator housing. The carriage is mounted on bearings that allow it to move in a forward or reverse direction along rails attached to the actuator housing. The rear of the carriage forms a cylinder around which the voice coil is wrapped. The heads are mounted on the forward end of the carriage; therefore, the heads, carriage, and voice coil move together as a unit.

The magnet mounts directly behind the actuator and is a one piece assembly consisting of a large permanent magnet. The magnet contains a circular cutout which allows the voice coil to move in and out of the magnet as the carriage moves.

Actuator and Magnet Functional Description

The movement of the carriage and voice coil (and therefore the heads) is controlled by positioning signals from the servo logic. The positioning signals are derived in the seek logic and processed by the power amplifier. The output of the power amplifier is a current signal which is applied to the voice coil via two flexible insulated metal strips called the voice coil flex leads.

The current from the power amplifier generates a magnetic field around the voice coil which reacts with the permanent magnetic field around the magnet. This reaction either draws the voice coil into the magnetic field or forces it away, depending upon the polarity of the current through the voice coil. The acceleration of the voice coil is dependent on the amplitude of the voice coil current.

Velocity Transducer

The velocity transducer (refer to figure 3-20) mounts within the magnet and consists of a stationary coil and a movable magnetic core. The core is contained within the coil and connects to the carriage via an extension rod. Therefore, when the carriage moves, the motion is transferred via the extension rod to the core.

When the carriage and core move, a voltage (an EMF) is induced in the coil. The amplitude of this EMF varies directly with the velocity of the carriage and the polarity of the EMF depends on the direction of carriage motion.

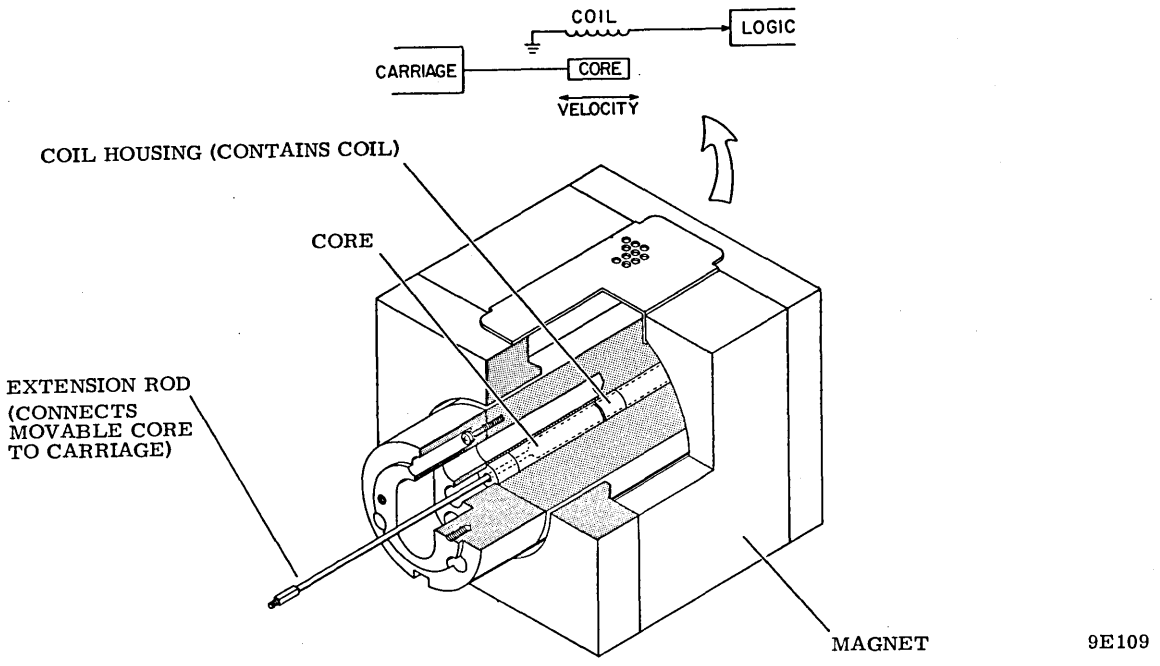


Figure 3-20. Velocity Transducer Assembly

The output of the velocity transducer is sent to the servo logic which uses it to control the acceleration of the carriage during seek operations.

Heads Loaded Switch

The heads loaded switch (refer to figure 3-21) mounts in the actuator housing and indicates whether the heads are loaded or unloaded. This information is used by the seek logic and power on/off sequencing circuits.

The switch is actuated by the carriage as the heads are loaded (moved out over the disk surfaces) or unloaded (moved clear of the disk surfaces and pack area). The switch indicates an unloaded status when the carriage is fully retracted and the heads are clear of the pack area.

During a load sequence, the carriage moves forward from the retracted stop and transfers the switch, to indicate a loaded condition, just as the heads are about to enter the pack area.

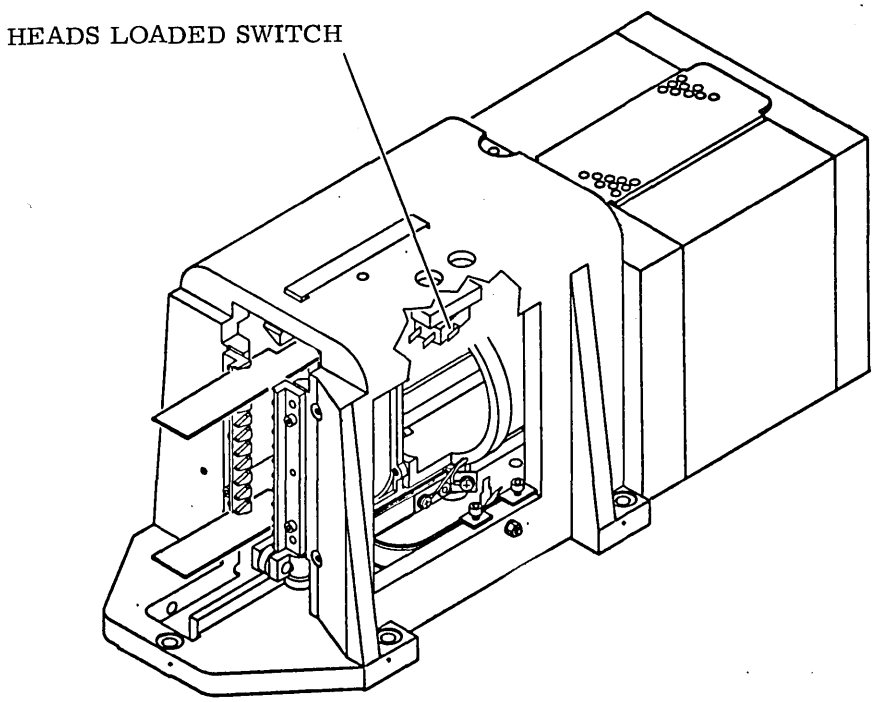
During an unload sequence, the carriage retracts and transfers the switch, to indicate an unloaded condition, just as the heads leave the pack area.

HEADS

General

The heads are electromagnetic devices that record (write) data and retrieve (read) it from the disk pack. They are mounted in the end of a supporting arm; head and arm together are called a head-arm assembly. The head-arm assemblies attach to the carriage (refer to figure 3-22).

The drive has 20 heads, one for each disk surface. There are two types of heads: (1) read/write and (2) servo. There are 19 read/write heads which are used to record data on and read it from the data surface. The one servo head is used to read information from the servo surface. This information is used by the drive servo circuits.



9E110A

Figure 3-21. Heads Loaded Switch Assembly

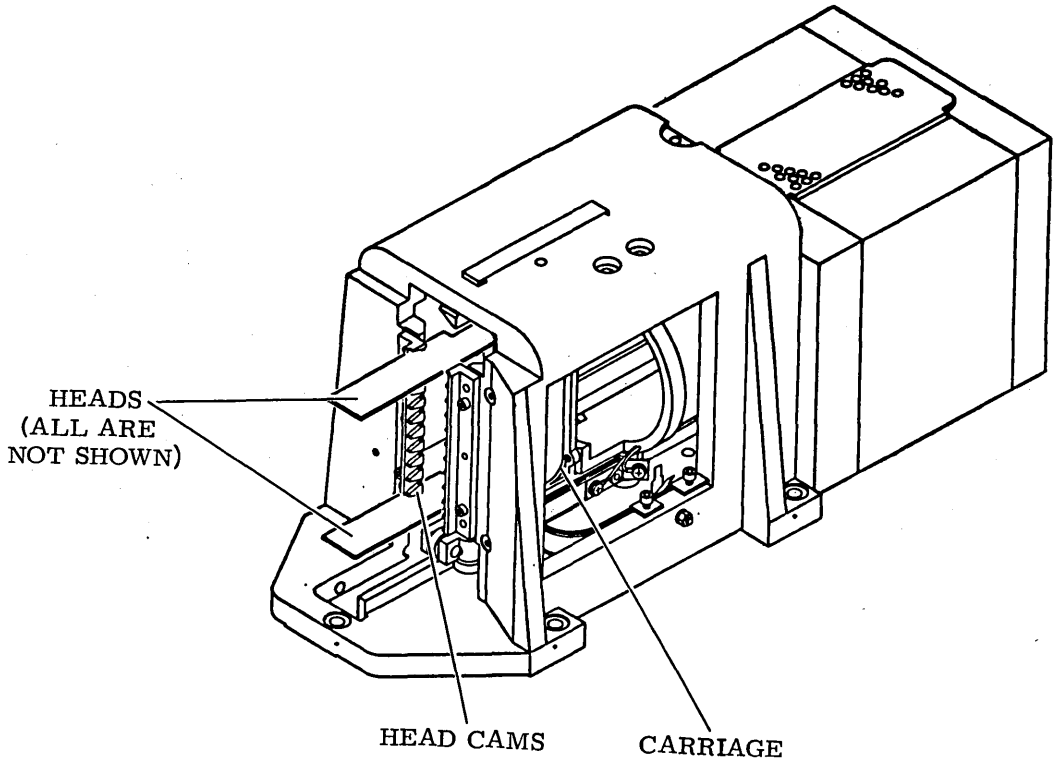


Figure 3-22. Heads

The following paragraph describe the physical characteristics of the head-arm assemblies and also how they function during head load and unload sequences. Further information concerning the heads is located in the discussions on read/write and seek functions.

Head-Arm Assemblies Physical Description

Each head-arm assembly consists of a rigid arm, head load spring, gimbal spring, and the head (refer to figure 3-23).

The rigid arm is mounted on the carriage and causes carriage motion to be transmitted to the head. However, the arm does not provide the action necessary for the head to load, unload and follow the disk surface. This action is provided by the head load and gimbal springs.

The head load spring attaches to the rigid arm and is the mounting point for the gimbal spring. The head in turn attaches to the gimbal spring.

During head loading and unloading, the head load springs ride on the head cams and keep the heads from contacting one another. When the heads are loaded, the head load and gimble springs work together and allow the heads to move simultaneously and also allow the heads to move independently of the rigid arms in the directions shown in figure 3-23. Such motion is necessary because when the the heads are over the disk surfaces they do not contact the disk but actually fly on a cushion of air created by the spinning of the disk pack.

Information is sent to and from the heads via the head-arm cables. One end of each cable connects to a head and the other end has a plug which connects to a card in the read/write chassis.

Head Loading

The heads must be loaded before the heads can be positioned to a data track for the recording and reading of data. Loading the heads consists of moving them forward from their retracted (unloaded) positions until they are over the disk surfaces. All heads are loaded simultaneously.

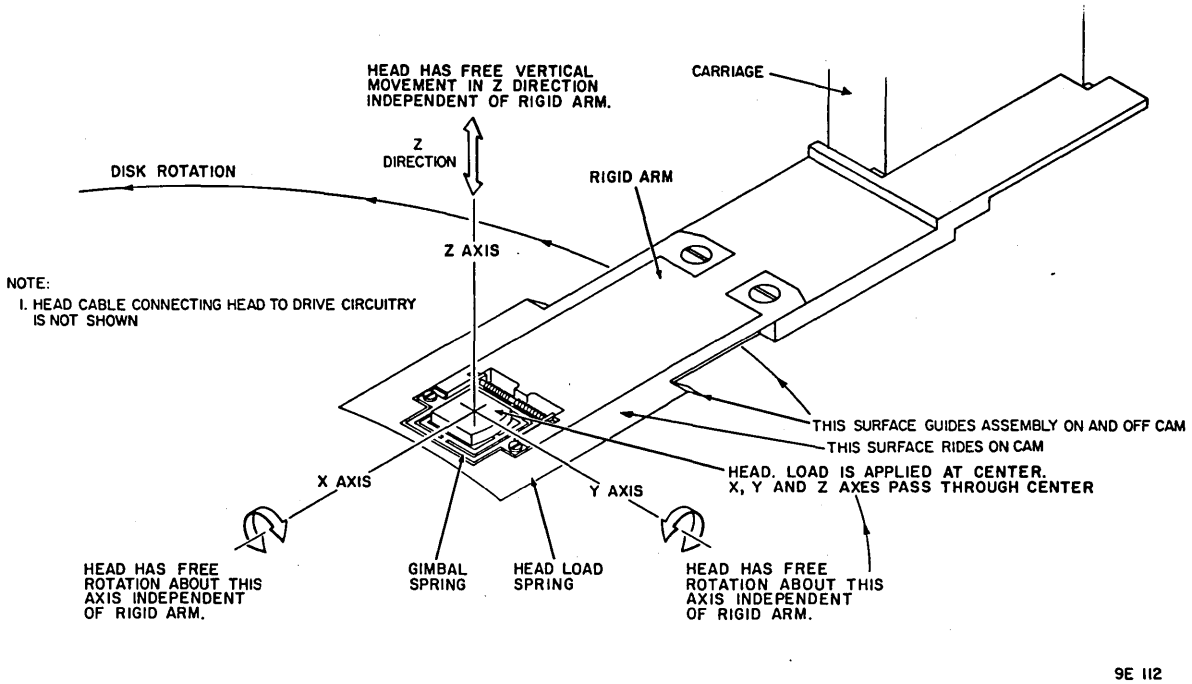


Figure 3-23. Head-Arm Assembly

The load sequence is initiated during the power up sequence when the disk pack has reached 3000 r/min. At this speed the spinning disk creates a sufficient cushion of air to allow the heads to fly.

When the pack is up to speed and the load logic is enabled, the heads move forward with the head load springs riding on the head cams. As the heads move out over the disk surfaces, the head load springs ride off the surfaces of the head cams (refer to figure 3-24).

The load springs, while riding off the cams, unflex and force the heads toward the air cushions on the spinning disk surfaces. When the cushions of air are encountered, they resist any further approach by the heads. However, the head load springs continue to force the heads down until the opposing air and spring pressures are equal.

The air cushion pressure varies directly with disk speed and if the disk pack is rotating at the proper speed, the air and spring pressures should be equal when the heads are flying at the correct height above the disks.

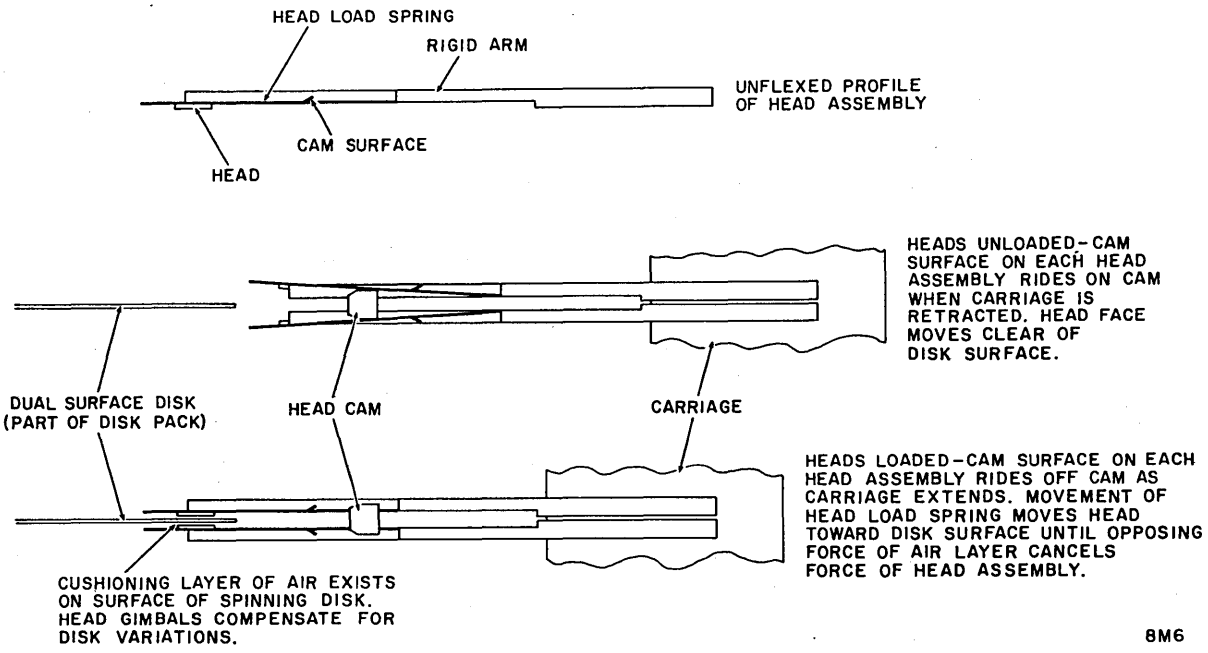


Figure 3-24. Head Loading

If the disk pack drops below this speed, air cushion pressure decreases and the head load springs force the heads closer to the disks. Sufficient loss of speed causes the heads to stop flying and contact the disk surfaces. This is called head crash and can cause damage to both the head and disk surfaces.

Because insufficient disk speed causes head crash, loading occurs only after the disk pack is up to speed. For the same reason, the heads unload automatically if disk pack speed drops below a safe operating level (refer to discussion on emergency retract).

Head Unloading

The heads must be unloaded whenever the pack is stopped or if it is spinning too slowly to fly the heads. Unloading consists of retracting the heads until they are no longer touching the disk surfaces.

The unload sequence is initiated either during a normal power off sequence, or during an emergency retract function. In both cases current is applied to the voice coil that causes the carriage to move back towards the retracted stop.

As the carriage retracts, the head load springs encounter the head cam surfaces and the heads are pulled away from the disk surfaces. The carriage continues to move back until it is fully retracted.

AIR FLOW SYSTEM

The air flow system (refer to figure 3-25) provides ventilation and cooling air for the drive.

The heart of the air flow system is the blower assembly. This assembly consists of the blower motor, absolute filter, input port from primary filter and output ports to the logic chassis, power supply and pack area.

The blower motor provides the pressure needed to draw air into and push it through the system. The system intake port is located beneath the rear of the cabinet. This port is covered by the primary filter which keeps large particles from being drawn into the system. Air flows from the intake port through a duct in the floor of the cabinet to the blower motor.

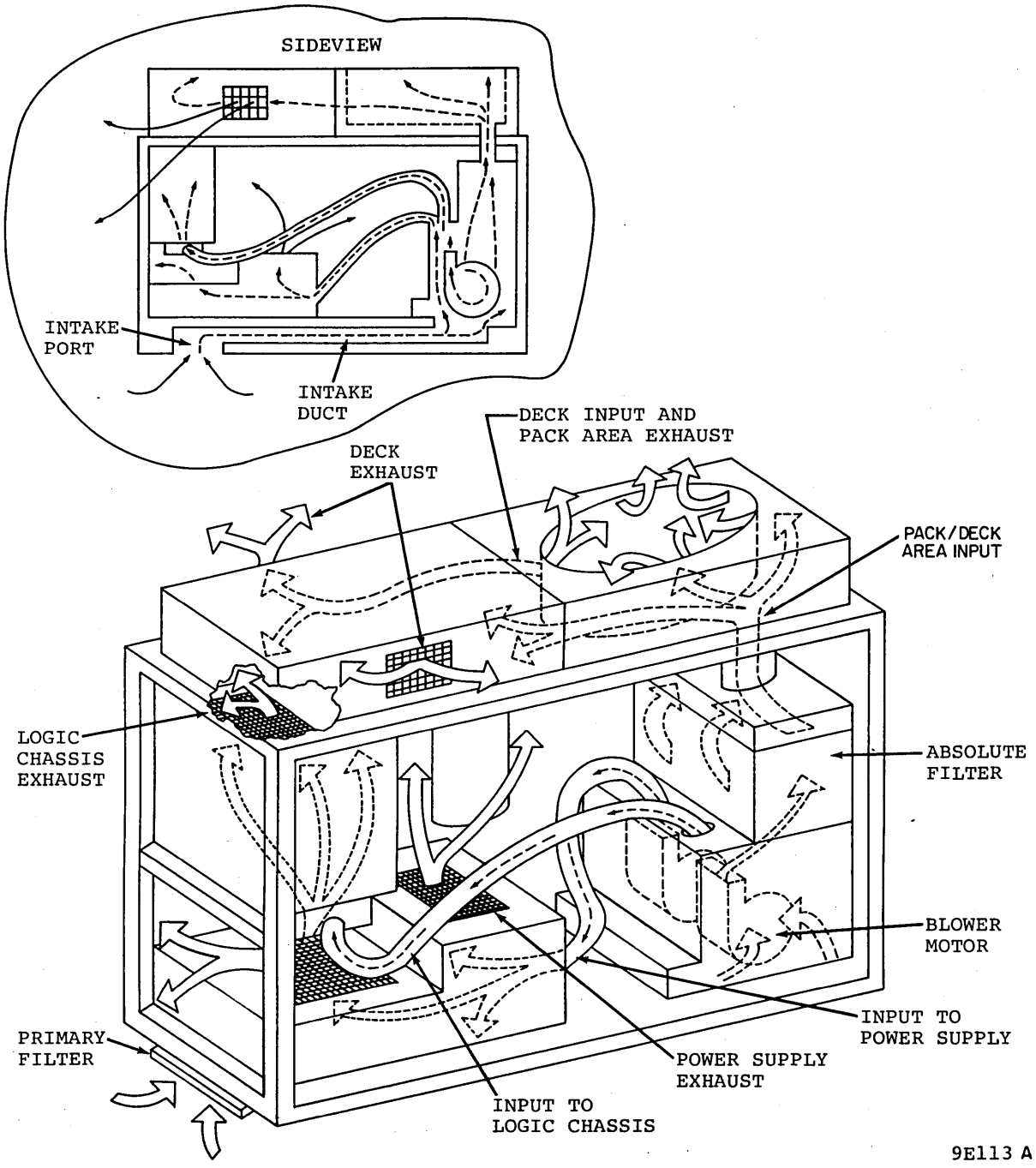


Figure 3-25. Air Flow System

The blower motor forces the air to the power supply, logic chassis, pack area and deck areas. The air to the logic chassis and power supplies flows through hoses connected between these assemblies and the blower assembly. The air exhausted by the power supply and logic chassis circulates through the lower part of the the drive cabinet and provides cooling air for the spindle motor.

The air to the pack area is cleansed by the absolute filter which removes particles that might cause damage to the pack or heads. The air is forced into the pack area from all sides causing a positive pressure. This results in an upward dispersion of air, thus preventing the entrance of contaminated air through the pack access cover.

The air intake for the pack area is also forced into the deck area through vents in the rear of the shroud. This air cools the deck components and exits through vents on each side of the deck cover.

INTERFACE

GENERAL

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals and read/write data transmitted and received by the drive.

The interface consists of the I/O cables and the logic required to process the signals sent between drive and controller.

The following describes both the I/O cables and I/O signal processing.

I/O CABLES

All signal lines between drive and controller are contained in two I/O cables. These are referred to as the A and B cables.

The A cable contains lines connected in twisted pairs, which carry commands and control information to the drive and status information to the controller.

The B cable contains lines which are either shielded or connected as twisted pairs. These lines carry read/write data, clock and status information between drive and controller.

Figure 3-26 shows all lines (except those not used) in the A and B cables. The functions of each of these lines is explained in tables 3-1 and 3-2.

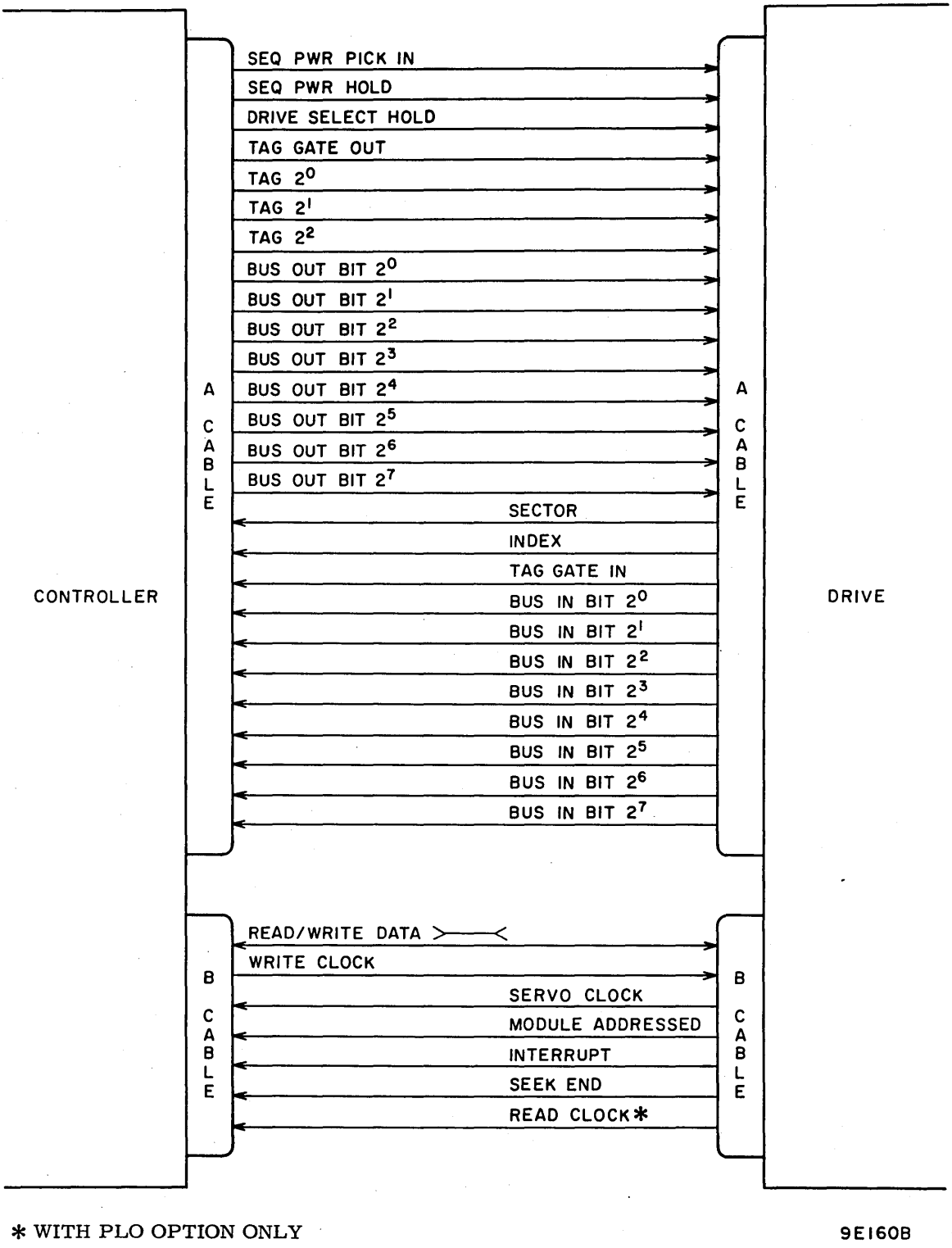


Figure 3-26. Interface Lines

TABLE 3-1. CONTROLLER TO DRIVE SIGNAL LINE FUNCTIONS

Signal Line	Signal Function
Sequence Power Pick	Used for power sequencing. A ground on this line powers up drive if LOCAL/REMOTE switch is in REMOTE. and START switch is on (refer to discussion on Power System).
Sequence Power Hold	Used for power sequencing. This line must be grounded at controller for drive to complete and hold remote power up sequence (refer to discussion on Power System).
Drive Select Hold	Allows signal information to be received by drive. Signal must be active to select or control drive. Essentially an open cable detector.
Tag Gate Out	Enables drives tag bus decode thus gating the tag bus commands to the drive logic (refer to discussion in I/O Signal Processing).
Tag Bus 0 - 2	Carry information which is decoded by drives tag bus decode and used in conjunction with Bus Out Lines to produce desired function (refer to table 3-3 and to discussion on I/O Signal Processing).
Bus Out Bits	Carry information which is used in conjunction with Tag Bus lines to produce specific drive functions (refer to table 3-3 and to discussion on I/O Signal Processing).
Write Clock	Used by drive write circuits this signal is synchronized to NRZ data sent from controller. This signal is actually Servo Clock retransmitted to the drive by the controller. It is transmitted continuously as long as the drive is ready.
Read/Write Data	Carries Write data to drive during write operations and Read data to controller during read operations (refer to discussions on Read/Write functions).

TABLE 3-2. DRIVE TO CONTROLLER SIGNAL LINE FUNCTIONS

Signal	Function
Sector	Derived from servo surface of disk pack, this signal can occur any number of times per revolution of disk pack. Number of sector pulses occurring per revolution depends on setting of switches on card in position A06 in logic chassis (refer to discussion on Sector Detection).
Index	Occurs once per revolution of disk pack and its leading edge is considered leading edge of sector zero. This pulse is typically 2.5 us in width (refer to discussion on Index).
Tag Gate In	Goes active about 300 ns after the drive has received Select Hold and Tag Gate Out; by this time Bus In is stable and can be sampled by controller. It should be noted that during read/write operations Bus In is dynamic and Tag Gate In indicates compliance with the command.
Bus In Bits	Carry status information concerning operation being performed (refer to table 3-3).
Servo Clock	Derived from disk pack servo surface this signal has a nominal frequency of 9.67 MHz but varies as disk pack rotational speed varies (refer to discussion on Machine Clock).
Module Addressed	Goes active when drive receives Tag 000 accompanied by logical address (on Bus Out Bits 4 - 7) that match logical address as indicated by drive Logical address Plug (refer to discussion on Unit Selection).

Table Continued on Next Page

TABLE 3-2. DRIVE TO CONTROLLER SIGNAL LINE FUNCTIONS (Contd)

Signal	Function
Interrupt	Goes active when drives rotational position sensing is activated and the drive is over a specified sector (refer to discussion on rotational position sensing).
Seek End	Indicates a seek operation has been completed. It is an indication of On Cylinder or seek error; therefore, the seek may or may not have been successful (refer to discussion on Seek Functions).
Read Clock	Derived from NRZ read data in those units with Read PLO option (refer to discussions on Read/Write Functions).

I/O SIGNAL PROCESSING

General

I/O signals from the controller initiate and control all drive operations except power on (refer to discussion on Power System). The I/O signals are sent to receivers in the drive and are routed from the receivers to the appropriate drive logic. The drive in turn sends information back to the controller via the transmitters. Figure 3-27 shows all I/O signals and how they are routed to and from the drive logic.

There are two basic types of I/O signals: (1) tag/bus out/bus in and (2) discrete. The two types differ in that the tag/bus out/bus in signals work in conjunction to perform a variety of functions while generally the discrete signals work independently each performing a specific function. Both types are described in the following.

Tag/Bus Signals

All commands are sent to the drive via the tag and bus out signal lines. The tag lines define the basic operation to be performed and the bus out lines modify or further define the basic operation. Whenever the drive receives a tag/bus out command it responds by sending status information back to the controller via the bus in lines.

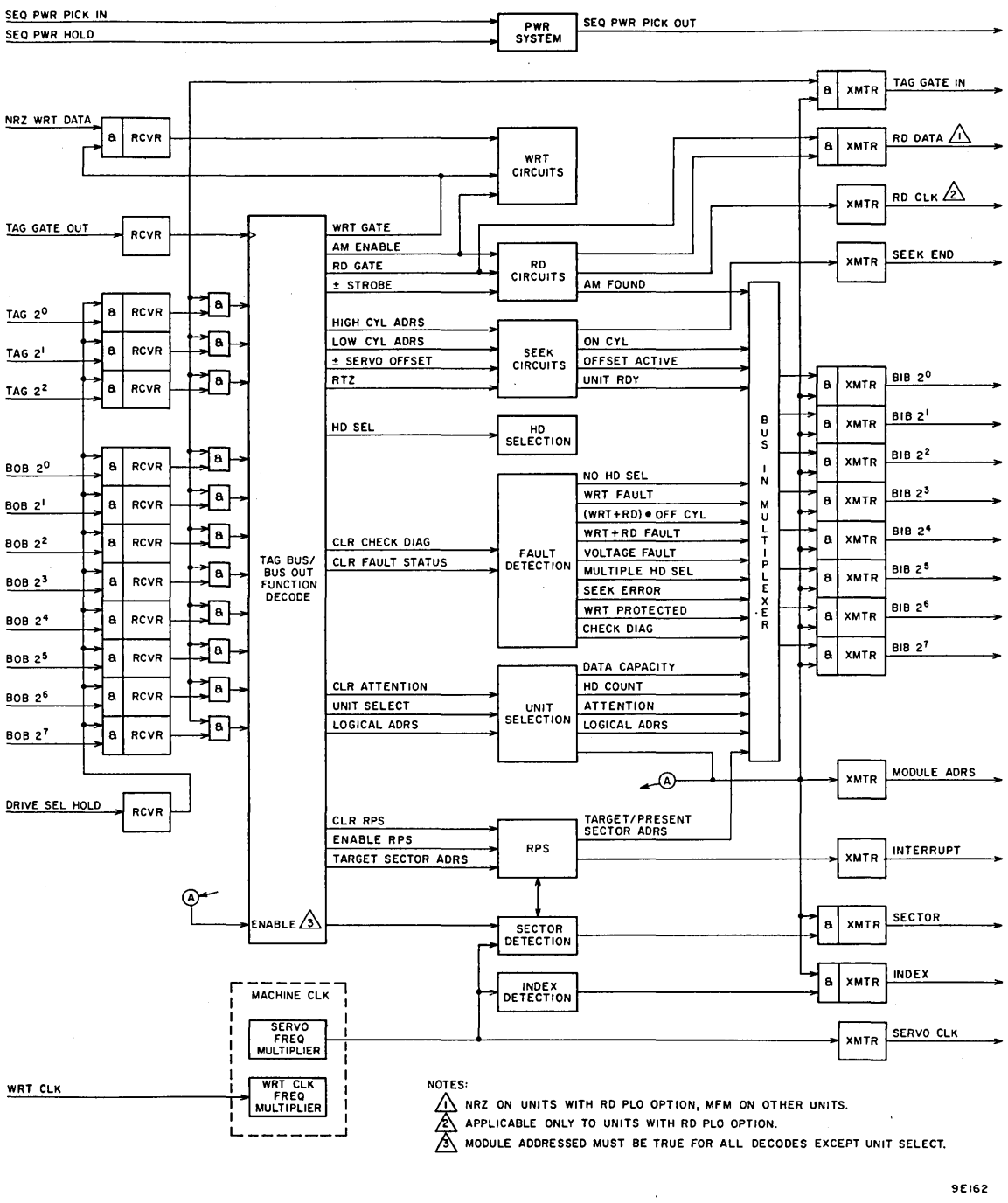


Figure 3-27. I/O Signal Processing Logic

Table 3-3 explains all the tag/bus out commands recognized by the drive and also describes the drives bus in responses to them. Figure 3-28 is a flow chart of the basic tag/bus out command sequence.

Discrete Signals

In addition to the tag/bus out/bus in signals, there are various discrete signal lines going between drive and controller. These lines carry clock, status, control and read/write data signals. The function of each of the discrete lines is explained in table 3-2.

UNIT SELECTION

The drive must be selected before it will respond to any commands from or transmit certain I/O signals to the controller. This is the case because Tag/Bus Out decode and certain transmitters are not enabled until the drive's Module Selected signal is active (this is shown on figure 3-27).

The unit select sequence is initiated by a Select tag (000) accompanied by an address on Bus Out bits 2^4 through 2^7. Because the tag and Bus Out receivers are enabled by the Drive Select Hold signal, it is necessary that this signal be active when the Unit Select Tag and logical address are sent.

When the drive recognizes the Unit Select tag, it compares its own logical address to the address sent by the controller. The drives logical address is determined by the logical address plug which fits into the operator control panel. Depending on the plug used, this address can be any number from 0 to 15. If no plug is used the number is 15.

If the address sent by the controller is the same as that of the drive, the drive enables its Module Addressed signal. This signal is sent to the controller and is also used by the drive to enable certain transmitters and to enable Tag/Bus Out function decode to decode other commands.

Figure 3-29 shows the logic involved in unit selection and table 3-4 briefly describes the major elements shown in this figure.

TABLE 3-3. TAG FUNCTIONS

Tag	Function
000 Unit Select	1. Used in conjunction with Bus Out bits 4 - 7 to initiate drive selection. Once selected, the drive replies with Module Addressed and status on Bus In (refer to discussion on Unit Selection for more information). 2. Bus Out is defined as follows: BOB 0-3 Not Used 4 Logical Address Bit 2^3 5 Logical Address Bit 2^2 6 Logical Address Bit 2^1 7 Logical Address Bit 2^0 3. Bus In is defined as follows: BIB 0 Data Capacity: If logical one it indicates 300 MB drive. If logical zero it indicates 150 MB drive. BIB 1 Head Count: Always true to indicate that this unit has 19 heads. BIB 2 Not Used BIB 3 Attention: When true it indicates that heads were unloaded and disk pack slowed down (possible pack change). This bit is cleared by Tag 010, BOB 1 (Clear Attention). BIB 4 Logical Address: Reflect contents of Bus Out bits 4 - 7.
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
001 Error Recovery	1. Initiate data error recovery operations. Specific operation is determined by Bus Out bits accompanying tag. 2. Bus Out is defined as follows: BOB 0* Early Strobe: Conditions MFM to NRZ converter circuits to strobe data at earlier than optimum time (refer to discussion on Read PLO/Data Separator). BOB 1* Late Strobe: Same as early strobe except that data is strobed at later than optimum time. BOB 2* Positive Offset: Causes drive to move heads slightly away from the on cylinder position in a direction towards the spindle (refer to discussion on Direct Seek Fine Control Track Following). BOB 3 Negative Offset: Same as positive offset except heads are moved away from spindle. BOB 4-7 Not Used These conditions are disabled by any of the following commands: RTZ (Tag 010, BOB 0), Low Cylinder (Tag 110), Clear Error Recovery (Tag 010, BOB 4), or another Tag 001 with the associated bit (0, 1, 2, or 3) false. 3. Bus In is the same as for Tag 000.

Table Continued on Next Page

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
010 Diagnostic	1. Causes drive to perform various diagnostic functions, the specific functions performed depends on the contents of Bus Out. 2. Bus Out is defined as follows: BOB 0 Return to Zero Seek (RTZ): Causes the drive to perform a seek to cylinder 000. It also clears the Seek Error FF, resets the head register and disables the Early/Late strobe and servo offset conditions. BOB 1 Clear Attention: Clears the drives Attention FF. BOB 2 Clear Check Diagnostic: Provided fault condition no longer exists, this clears drives Fault FF and the Check Diagnostic bit. However, fault register FFs and indicators are not cleared (refer to discussion on Fault and Error Detection). BOB 3 Clear Fault Status: Provided fault no longer exists, this clears drives Fault latch, Fault registers FF's and maintenance indicators (refer to discussion of Fault and Error Detection). BOB 4 Clear Error Recovery: Disables error recovery conditions initiated by Error Recovery Tag (001). BOB 5 Clear RPS: Disables rotational position sensing (refer to discussion on rotational position sensing).

Table Continued on Next Page

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	BOB 6, 7 Not Used 3. Bus In is defined as follows: BIB 0 No Head Select: Indicates drive has been commanded to select a head address greater than 19 (maximum head address). It is cleared by selecting a valid head count (address less than 19). BIB 1 Write Fault: Indicates an absence of write current when a write operation is being performed. Detection of this fault prevents drive from writing data. BIB 2 Write or Read and Off Cylinder: Indicates that a write or read operation has been attempted while the heads are on cylinder. Detection of this fault prevents drive from writing data. BIB 3 Write and Read: Indicates that a write and a read operation were commanded at the same time. Detection of this fault prevents drive from writing data. BIB 4 Voltage Fault: Indicates below normal ±5, ±20, or ±46 voltages. This fault prevents drive from writing. BIB 5 Multiple Head Select: Indicates more than one head selected at same time. This fault prevents drive from writing. BIB 6 Seek Error: Indicates one of the following errors occurred during seek operation.
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	• Drive unable to complete seek within 500 ms. • Carriage move to position outside recording field (forward or reverse EOT detected). • Drive was commanded to seek to cylinder address greater than 822 (410 on 150 MB units). Seek error condition is cleared only by Return to Zero Seek command (Tag 010, BOB 0). BIB 7 Write Protect: Indicated drives write circuits are disabled. This signal goes true under any of the following conditions: • WRITE PROTECT switch on drive operator panel is depressed and indicator is lighted. • Head alignment is being performed. • Fault condition exists that inhibits writer. Write protect condition is disabled when WRITE PROTECT switch on drive operator panel is pressed to extinguish indicator. If a write operation is commanded during a write protect condition the Check Diagnostic bit goes true.
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
011 Head Select	1. Initiates selection of head indicated by address on Bus Out (refer to discussion on Head Selection). 2. Bus Out is defined as follows: BOB 0-2 Not Used 3 Head Address 2^4 4 Head Address 2^3 5 Head Address 2^2 6 Head Address 2^1 7 Head Address 2^0 3. Bus In bits are defined the same as for Tag 010.
High Cylinder 100	1. Sends high cylinder address bits (2^8 and 2^9) to the drive via Bus Out. These bits must always precede the low cylinder address bits sent via Tag 010 (refer to discussion on Direct Seek Position Control). 2. Bus Out is defined as follows: BOB 0-5 Not Used 6 Cylinder Address Bit 2^9 (used only on 300 MB units) 7 Cylinder Address Bit 2^8

Table Continued on Next Page

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	3. Bus In contains Target register bits 2^0 through 2^7. This information is loaded into Target register during a Tag 101 and is defined as follows: BIB 0 Enable RPS 1 Target Sector Bit 2^6 2 Target Sector Bit 2^5 3 Target Sector Bit 2^4 4 Target Sector Bit 2^3 5 Target Sector Bit 2^2 6 Target Sector Bit 2^1 7 Target Sector Bit 2^0
Target Register 101	1. Used to initiate rotational position sensing (RPS) and also to read contents of drives Present Sector register. The specific function performed depends on the contents of Bus Out (refer to discussion on Rotational Position Sensing). 2. Bus Out is defined as follows: BOB 0 Enable RPS: When true it causes drive to store, in its Target register, the sector address contained on But Out bits 1 - 7 and also enables RPS so drive will raise its Interrupt line each time it reaches this sector. When false, it causes drive to store, in its Target register, the address of sector it is in when command is received. RPS is not enabled when the bit is false.

Table Continued on Next Page

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	BOB 1 Target Sector Bit 2^6 BOB 2 Target Sector Bit 2^5 BOB 3 Target Sector Bit 2^4 BOB 4 Target Sector Bit 2^3 BOB 5 Target Sector Bit 2^2 BOB 6 Target Sector Bit 2^1 BOB 7 Target Sector Bit 2^0 3. When BOB 0 is true, Bus In reflects what was sent on Bus Out (target sector). When BOB 0 is false, Bus In displays sector drive was in when command was received (present sector). Bit assignments in both cases are as follows:

BIB	With BOB 0 True	With BOB 0 False
0	Enable RPS	Store Present Sector
1	Target Sector 2^6	Present Sector 2^6
2	Target Sector 2^5	Present Sector 2^5
3	Target Sector 2^4	Present Sector 2^4
4	Target Sector 2^3	Present Sector 2^3
5	Target Sector 2^2	Present Sector 2^2
6	Target Sector 2^1	Present Sector 2^1
7	Target Sector 2^0	Present Sector 2^0

Table Continued on Next Page

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
Low Cylinder 110	1. Sends lower seven bits of new cylinder address to drive and initiates seek operation. This tag must be provided by a high cylinder tag (100) if there is a change in the high cylinder address (bits 2^8 and 2^9). Refer to discussion on Direct Seek Position Control for more information. 2. Bus Out is defined as follows: BOB 0: Cylinder Address 2^7 — BOB 4: Cylinder Address 2^3 BOB 1: Cylinder Address 2^6 — BOB 5: Cylinder Address 2^2 BOB 2: Cylinder Address 2^5 — BOB 6: Cylinder Address 2^1 BOB 3: Cylinder Address 2^4 — BOB 7: Cylinder Address 2^0 3. Bus In is defined the same as for Tag 111.
Control 111	1. Initiates various functions depending on the contents of Bus Out. 2. Bus Out is defined as follows: BOB 0 Transfer Sector Count: Causes drive to enable RPS and transfer present sector count to Target register (refer to discussion on RPS). BOB 1 Write Gate: Causes drive to start writing data on disk (refer to discussion on Write Circuits). BOB 2 Not used

Table Continued on Next Page

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	BOB 3 Read Gate: Causes drive to read data from disk and send it to controller (refer to discussion on Read Circuits). BOB 4 Address Mark Enable: Causes drive to either read or write address marks. When this bit is true, along with BOB 1 (Write Gate) the drive creates an address mark and write fault detection is inhibited. When this bit is true along with BOB 3 (Read Gate) the drive searches for an address mark and when it is found sets BIB 4 (refer to discussions on Read/Write Functions). BOB 5-7 Not Used 3. Bus In is defined as follows: BIB 0 Address Mark Found: Goes true when drive detects an address mark during a read operation. BIB 1 Not Used BIB 2 On Cylinder: Indicates heads are positioned and drive is ready to read, write or perform another seek operation (refer to discussion on Direct Seek Fine Control-On Cylinder Detection). BIB 3 Unit Ready: Indicates drive is up to speed, heads are loaded, and no fault condition exists. BIB 4,5 Not Used BIB 6 Offset Active: Indicated drive servo is in offset mode.
Table Continued on Next Page	

TABLE 3-3. TAG FUNCTIONS (Contd)

Tag	Function
	BIB 7 Check Diagnostics: Indicates one of the following conditions exists: o Seek Error latch set o Fault latch set o No Head Selected fault o Write Gate true during write protect condition Further information status can be obtained via a Tag 010 (Diagnostic).
* Applicable only to units with Read PLO option.	

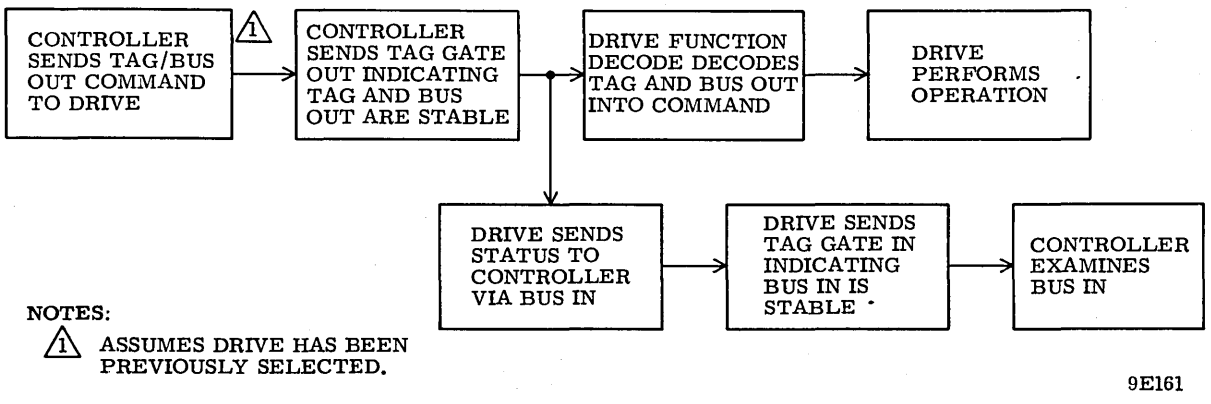


Figure 3-28. Tag/Bus Out Command Sequence Flow Chart

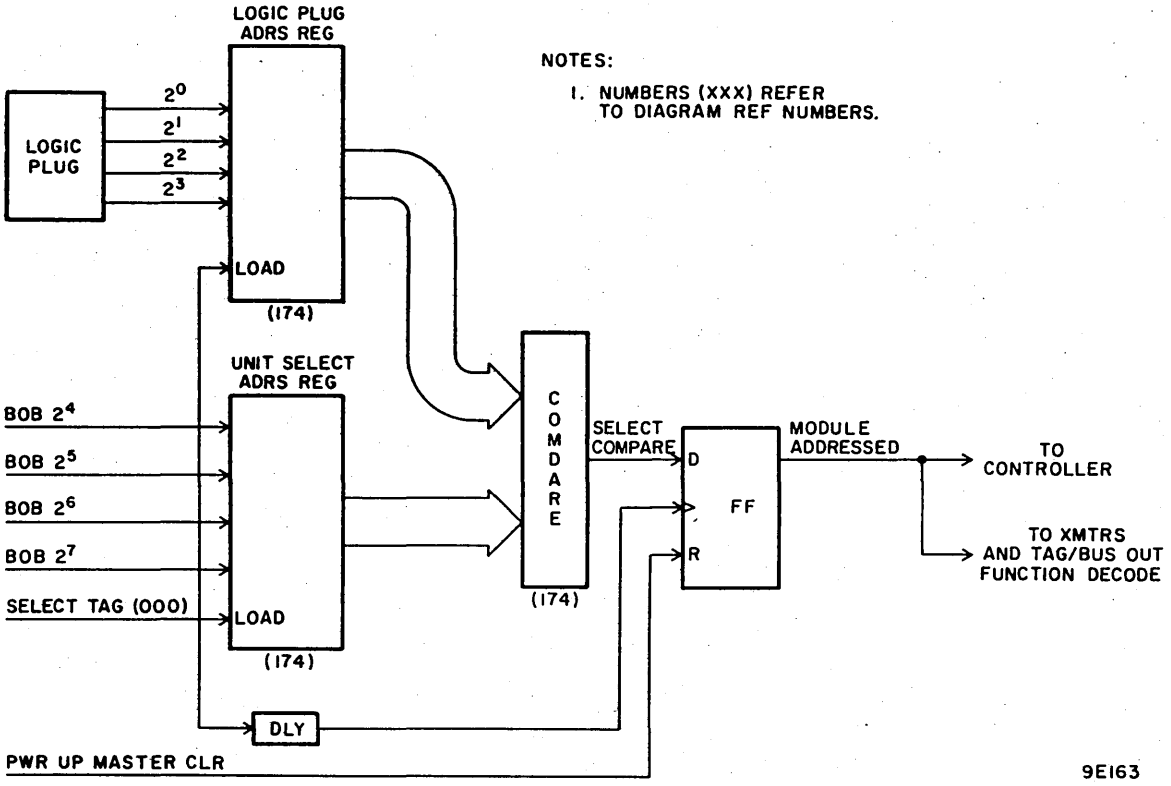


Figure 3-29. Unit Select Logic

SEEK FUNCTIONS

GENERAL

The drive must move the heads to the desired position over the disk pack before any read or write operation can be performed. This is done during seek functions and is performed by the drives servo circuits.

The servo circuits form a closed loop servo system that controls movement by comparing the present position of the heads to the desired future position and generating a position control signal proportional to the difference between them.

TABLE 3-4. UNIT SELECT CIRCUIT FUNCTIONS

Element	Function
Compare Circuits	Compares address sent from controller with that of drive logical address plug and provides active output when they are the same.
Logic Plug	Fits into drive operator control panel and determines logical address of drive.
Logic Plug Address Register	Loads address of logic plug when Unit Select Tag is received and applies it to input of compare circuit.
Unit Select Address Register	Loads address sent by controller when Unit Select tag is received and applies it to input of compare circuits.
Module Addressed FF	Setting this FF enables Module Addressed signal to controller indicating drive is selected. Enables Tag and Bus Out function decode so drive can respond to further commands, and also enables Bus In and various other transmitters to controller.

The major elements in the servo loop are shown on figure 3-30. The drive servo loop, the circuits it contains, and how it works during seek functions are described in the following discussions. These discussions are organized as follows:

- Overall Loop Description - Provides overall explanation of servo loop and how it functions during various seeks.
- Servo Disk Information - Describes the information that is permanently recorded on the servo surface of the disk pack and used by the servo loop to control positioning.
- Position Feedback Generation - Explains how the servo disk information is converted to feedback signals that are used to control positioning of the heads.

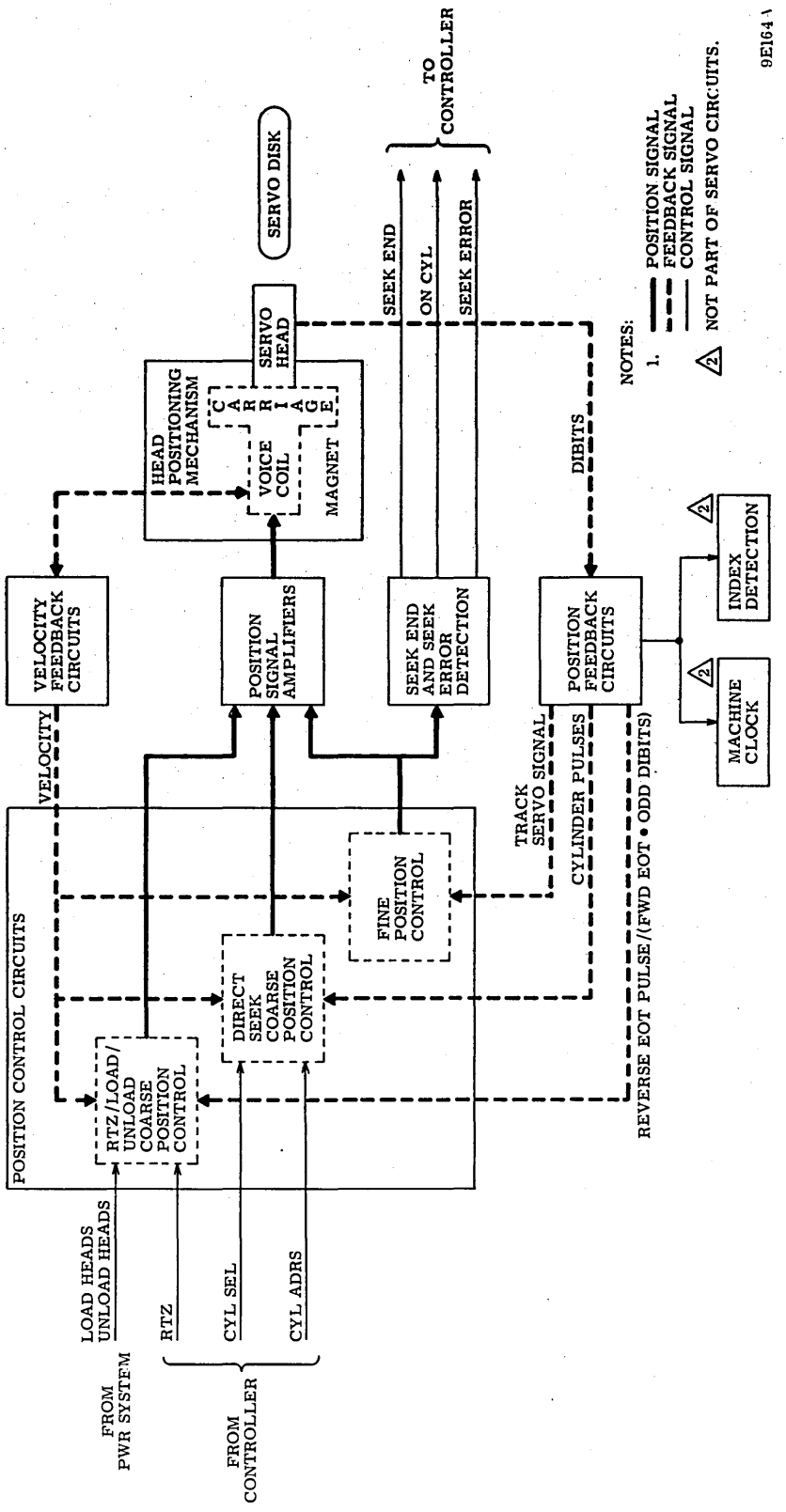


Figure 3-30. Servo System Functional Block Diagram

- Velocity Feedback Generation - Explains how the speed of the carriage is monitored and how this information is used to generate signals to control the speed of the carriage.

- Position Signal Amplification - Explains how the position signals from the position control circuits are used to generate current for the voice coil.

- Direct Seek Position Control - Explains how the positioning signals are generated and how the overall loop functions during direct seek sequences.

- Load Seek Position Control - Explains how the positioning signals are generated and how the servo loop functions during load seeks. These occur during the power up sequence when the heads are loaded.

- Return to Zero Seek Position Control - Explains how the positioning signals are generated and how the servo loop functions when the controller commands a return to zero (RTZ) seek.

- Unload Seek Position Control - Explains how the positioning signals are generated and how the servo loop functions during power off sequences when the heads unload.

- Seek End and Seek Error Detection - Describes indications sent to the controller at the end of a seek and also describes various seek errors detected by the drive.

These discussions are applicable to both the 150 MB BJ4M1 and 300 MB BJ4M2/BJ402 drives. For the most part, these drives function identically; however, some things such as cylinder numbers are different and these differences are noted in the text.

EXAMPLE: When logical cylinders to go are less than 64 (150 MB) or 128 (300 MB) ...

In this case, 64 applies only to 150 MB BJ4M1 drives and 128 applies only to 300 MB BJ4M2 drives. Similar notes accompany all differences wherever they occur.

OVERALL LOOP DESCRIPTION

The servo loop (refer to figure 3-30) consists of the position control circuits, position signal amplifiers, head positioning mechanism, and feedback circuits (both velocity and position).

The inputs to the loop are applied to the position control circuits. These inputs come either from the controller (in the case of a direct or return to zero seek) or from the power system (in the case of a load or unload sequence). This is explained further in the discussions on position control.

The position control circuits are divided into three parts (1) RTZ/load/unload coarse position control (2) direct seek coarse position control and (3) Fine position control. Which of these is used to control positioning depends on the type of seek being performed and how close the heads are to the desired position. The following explains the action of the position control circuits and the rest of the servo loop during a typical seek operation.

At the start of a seek, the initial positioning information is input to either the RTZ/load or direct seek coarse position control circuits (depending on the seek being performed). These circuits then generate a control signal proportional to the distance to the destination and its polarity depends on the direction of the seek.

The position control signal is processed by the position signal amplifier which generates current for the voice coil. The voice coil is attached to the carriage which supports and moves the heads. The voice coil is located within a magnet and whenever a current passes through the coil windings, the interaction between the induced EMF and the magnetic flux field causes the voice coil and carriage to move. The acceleration of the motion is proportional to the polarity and magnitude of the voice coil current (the head positioning mechanism is discussed in detail in the discussions on Electromechanical Functions).

As the heads move, feedback signals are generated that indicate how fast the heads are moving (velocity feedback) and how far the heads have move towards the desired destination (position feedback).

The velocity information is derived from the velocity transducer which generates signals proportional to carriage speed. The position feedback signals are generated from information read from the servo disk by the servo head.

Both velocity and position feedback signals are used by the coarse position feedback circuits to vary this position control signal as the destination is approached. They are also used to determine when the servo system should switch from coarse to fine control.

When this switch is made, the coarse position control circuits are disabled and the fine position circuits are enabled. Fine control is necessary to ensure that the heads are accurately positioned over the destination and also to keep it positioned once the seek is complete. The fine position control circuits also use signals from the feedback circuits to control positioning.

The seek end and seek error detection circuits sense when the seek is complete and at this time indicate whether or not it was successful.

The preceding described basic loop operation. More detailed descriptions of the elements in the loop and loop operation are contained in the following discussions.

SERVO DISK INFORMATION

General

The servo disk surface (refer to figure 3-31) contains servo positioning information that is recorded on the disk at the time of manufacture.

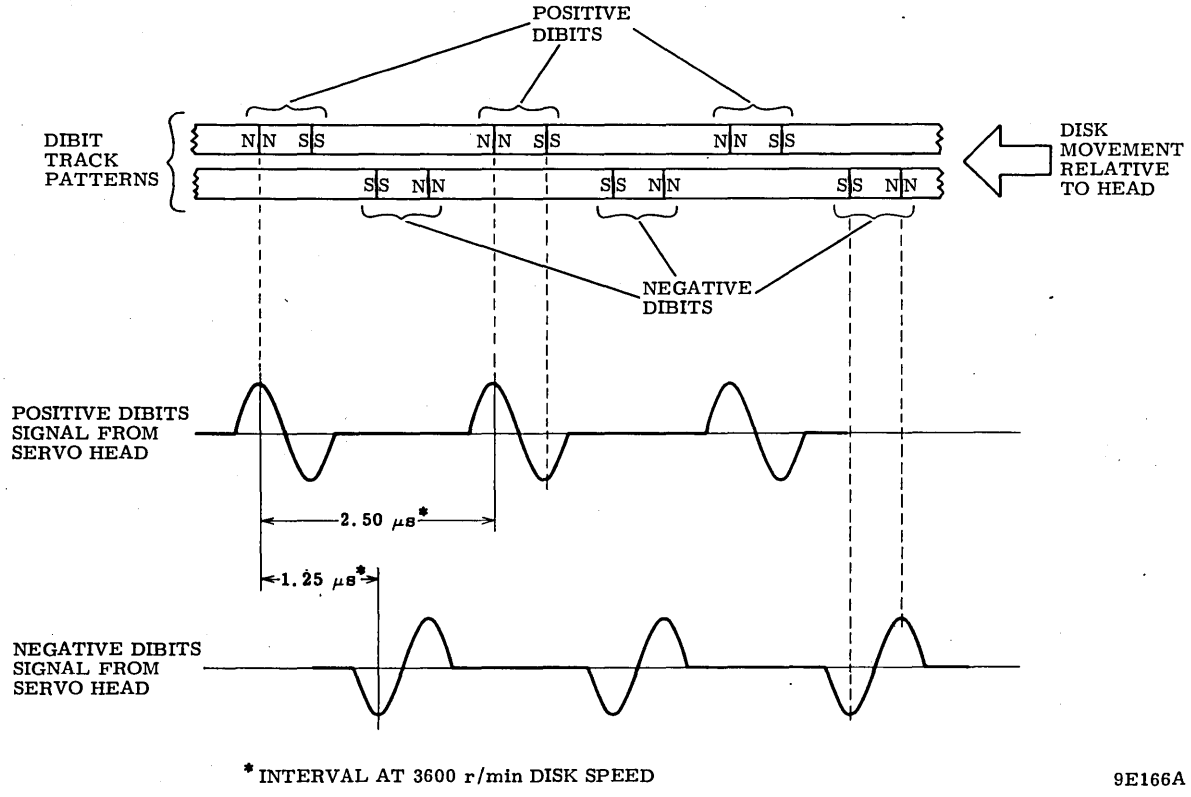


Figure 3-31. Positive and Negative Dibit Pattern

This information is read by the servo head and processed by the position feedback circuits. These circuits generate position feedback signals that are used by the positioning circuits to control the positioning of the heads. The servo disk information is also used to generate clock signals used by the Index and Machine clock circuits.

The following describes the information recorded on the servo surface.

Dibits

The servo positioning information is recorded on the disk as specific patterns of flux reversals referred to as dibits. There are two types of dibits: positive and negative.

The positive and negative dibits are classified according to the type of waveform produced when they are read by the servo head (the waveform actually appears at the output of the track servo preamp). The positive dibits produce a waveform with the leading pulse positive and the trailing pulse negative. The negative dibits produce a waveform with the leading pulse negative and the trailing pulse positive. The dibit patterns and their associated waveforms are shown on figure 3-31.

Dibit Tracks

The dibits are recorded in track patterns around the disk. The servo surface has 883 dibit tracks each recorded exclusively with either positive or negative dibits. These tracks are recorded adjacent to one another with no void area between them. Those tracks containing only positive dibits are termed odd dibit tracks and those tracks containing only negative dibits are termed even dibit tracks.

Outer and Inner Guard Bands

The outer 24 tracks are odd dibit tracks and contain only positive dibits. This area is known as the outer guard band or the reverse end of travel (EOT) area.

The inner 36 tracks are even dibit tracks and are known as the inner guard band or the forward end of travel EOT) area.

Both the outer and inner guard bands are shown on figure 3-32.

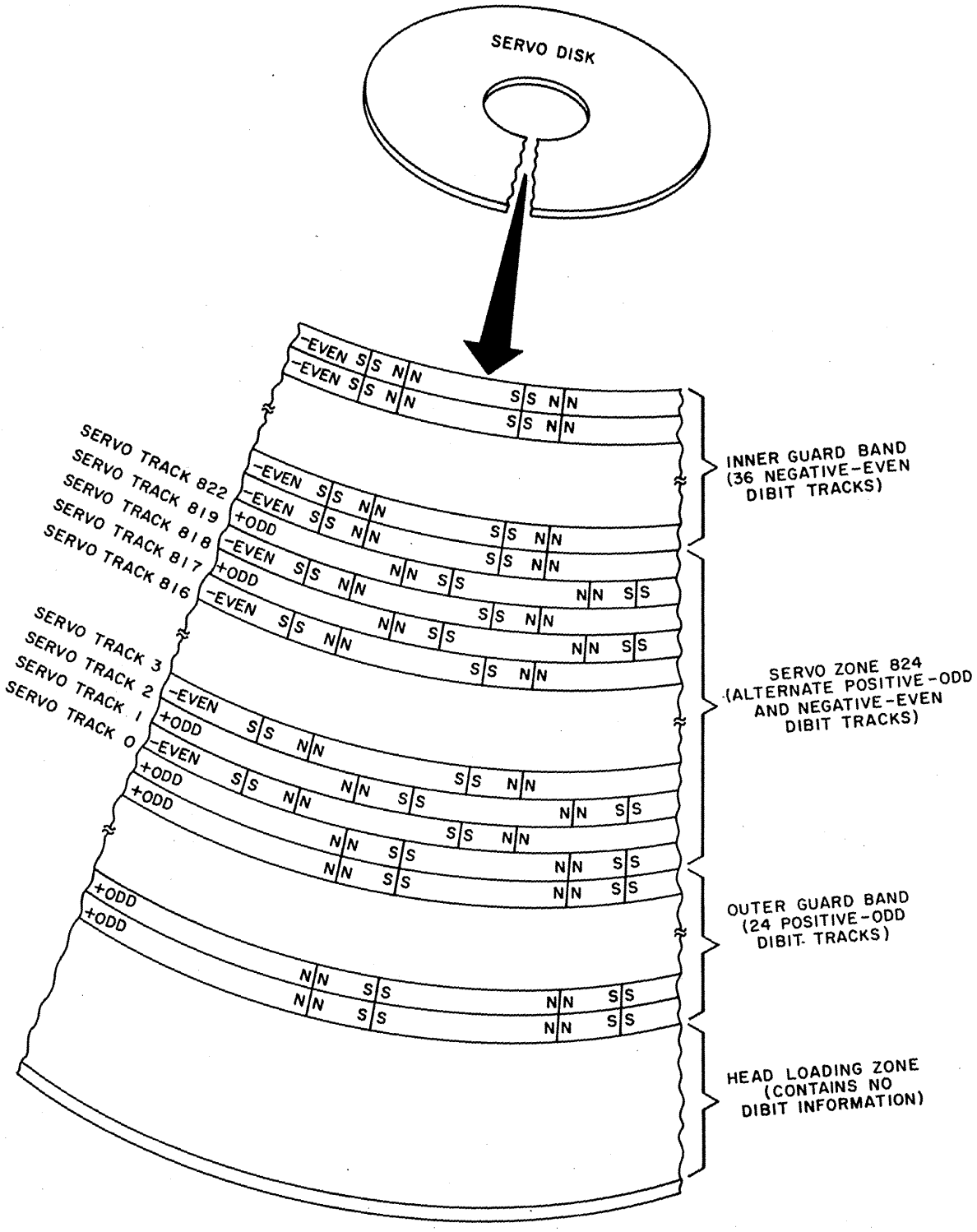


Figure 3-32. Servo Disk Format

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Servo Zone

In between the inner and outer guard bands is an area called the servo zone. The servo zone consists of 824 alternately spaced odd and even dibit tracks. Because the dibit tracks are adjacent to one another, junctions are formed between the positive and negative tracks. The null areas between dibit tracks are referred to as servo tracks. The drive contains 823 servo tracks numbered from 000 to 822.

When the servo head is centered over a servo track, it will alternately detect both positive and negative dibits. The combination of these signals results in each servo track being divided into exactly 13 440 intervals (where an interval is the time between the leading peaks of successive dibits).

In addition to this, each dibit track in the servo zone is encoded with an Index pattern of missing dibits. The index pattern is the same on each servo track and is recorded at a specific circumferential location on the tracks.

Further information about Index and its application is given in the discussions on Track Orientation.

Cylinder Concept

The data recording zones on the data surfaces are aligned vertically with the servo track zone on the servo surface. For this reason, all head movement and positioning is referenced to the position of the servo head over the servo surface.

Therefore, when the servo head is positioned over a specific servo track on the servo surface, all other heads are positioned over the corresponding data tracks on their respective data surfaces. For example, if the servo head is over track 10, all other heads are also over track 10. The vertical alignment of these tracks create an imaginary cylinder as shown on figure 3-33.

Physical to Logical Cylinder/Track Correlation

The 150 MB and 300 MB drives both use the same disk pack. This pack has 823 servo tracks and therefore 823 cylinders that can be addressed and used for data recording.

These cylinders are numbered from 000 to 822 (refer to figure 3-34) and are defined as physical cylinders. Each track, in these cylinders is defined as a physical track.

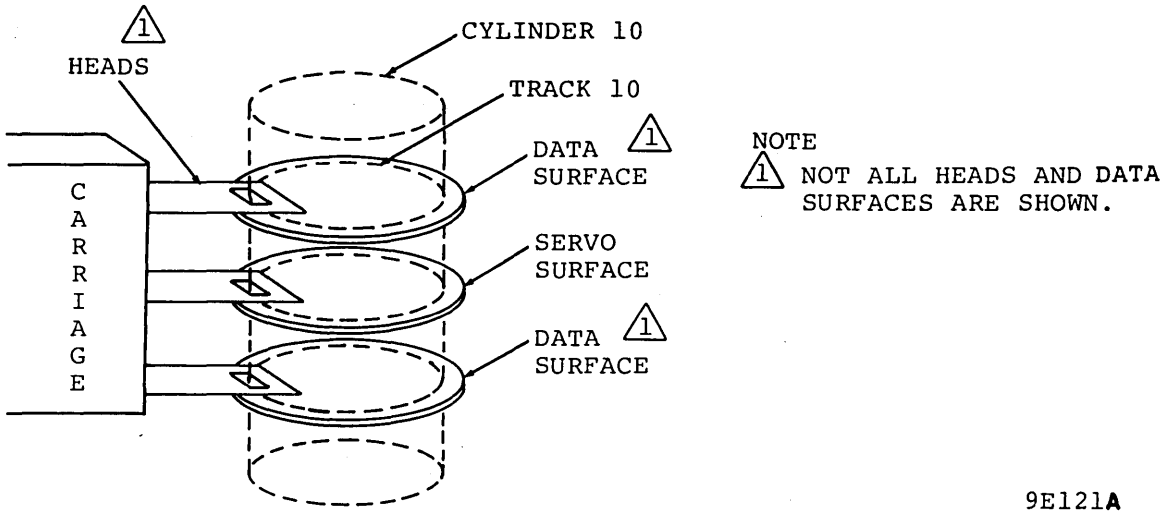


Figure 3-33. Cylinder Concept

Each physical cylinder has an associated logical address. This is the address used to reference the cylinder during seek operations. This logical address is different depending upon whether the pack is used on 150 MB or 300 MB drive.

When used on a 300 MB drive, the logical cylinder address corresponds to the physical cylinder address. This is the case because the 300 MB drive is capable of addressing 823 logical cylinder addresses (000 to 822) and therefore can seek to all 823 physical cylinders.

However, a 150 MB drive can address only 411 logical cylinders (000 to 410) and seeks to only the even numbered physical cylinders. In this case, the physical and logical cylinder addresses do not directly correspond. For example, logical cylinder 001 is actually physical cylinder 002 and logical cylinder 410 is physical cylinder 820.

The physical to logical track correlation for both the 150 MB and 300 MB drives is shown on figure 3-34.

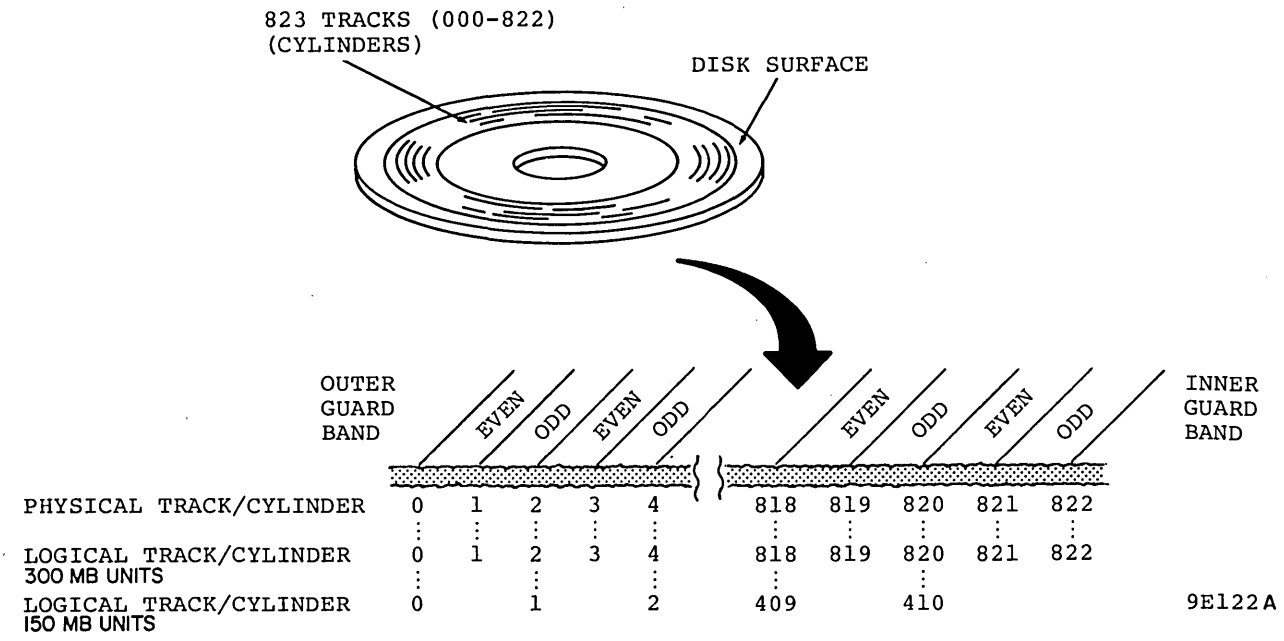


Figure 3-34. Physical to Logical Track Correlation

POSITION FEEDBACK GENERATION

General

All position feedback information is generated by the position feedback circuits. These circuits use the dibits data read from the servo disk to generate the feedback signals required by the position control circuits.

The feedback signals generated and their basic functions are as follows:

- Track Servo signal - Used by the fine position control circuits to control positioner movement during the last half track of a seek.
- Cylinder Pulses - Pulses that occur each time the servo head crosses a servo track. These pulses are used by the coarse position control to determine the distance to the desired cylinder.
- Reverse EOT Pulse - Provides feedback to the RTZ coarse position control circuits during a return a zero seek (RTZS).

- Forward EOT Enable and Odd Dibits - Provides feedback during RTZ, load and unload seek that cause positioning control to be switched from the RTZ load/unload coarse position control circuits to the fine position control circuits.

In addition to providing these signals, the position control feedback circuits also produce the Odd/even dibit signals used by the machine clock and index detection circuits.

A basic block diagram of the feedback circuits is shown on figure 3-35 and each of the elements on the diagram are explained in the following discussion.

Track Servo Preamp

The signal from the servo head must be processed by the track servo preamplifier before the servo track information can be used by the rest of the position feedback circuits.

The signal received from the servo head depends on the type of servo dibit track it is reading. When the head is over the outer or inner guard bands, it reads from tracks that have either all positive or all negative dibits. In this case, the preamp produces either all positive or all negative dibit waveforms (refer to figure 3-31).

When the head is over the servo zone, it passes over both types of dibit tracks and the preamp produces a waveform that is a mixture of both types of dibit signals.

The amplitude of each dibit component in the waveform is proportional to how much the servo head is overlapping the tracks. If the head is centered over a servo track the signal has equal positive and negative dibit components. However, when the head is away from the centerline, the amplitude of one dibit component is greater than the other (this is shown on figure 3-36).

If the servo head is moving through the servo zone, each component alternately increases and decreases as the servo tracks are passed. This is also shown on figure 3-36.

The output of the track servo preamp is sent to the AGC and dibits detect circuit.

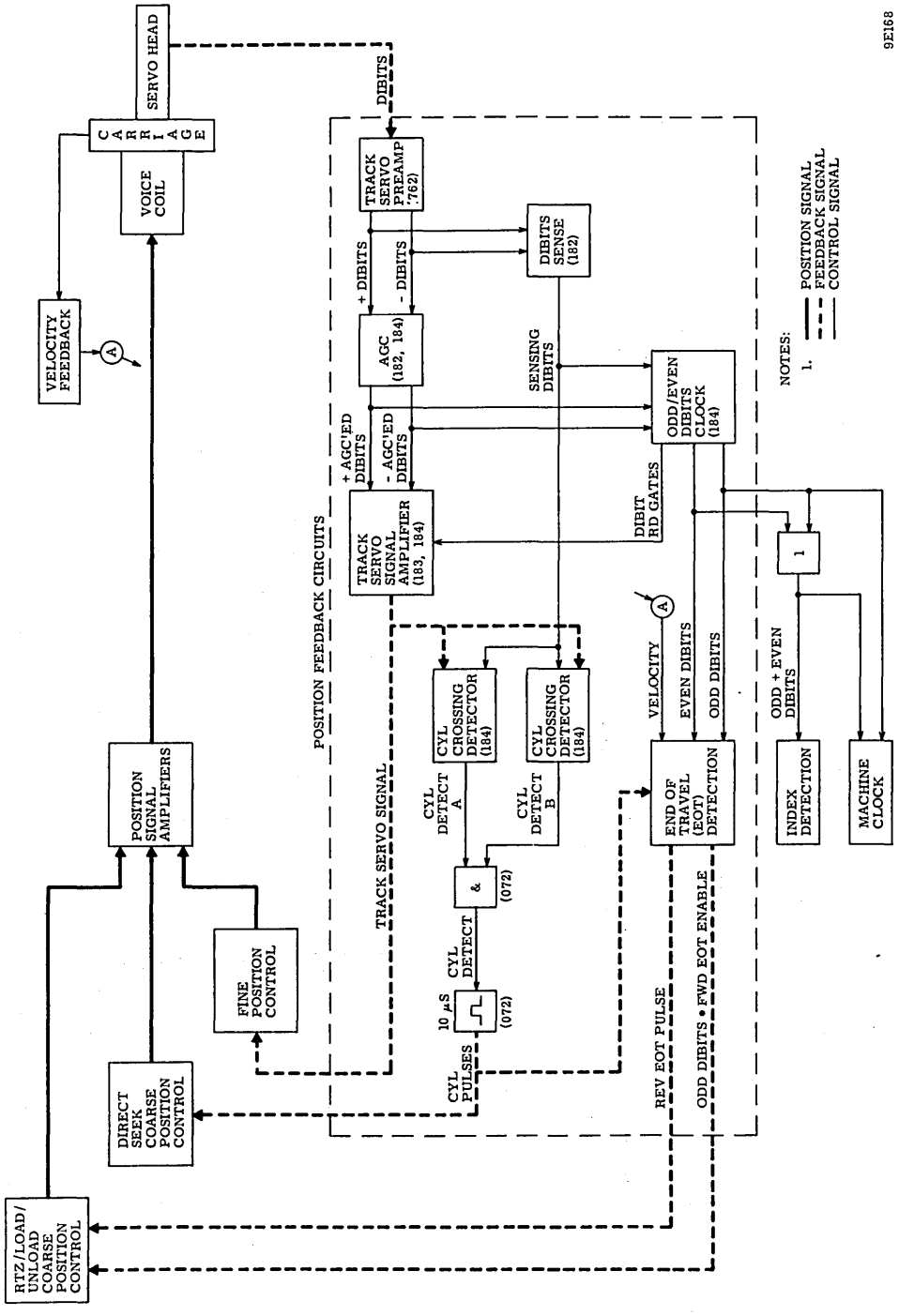


Figure 3-35. Position Feedback Circuits

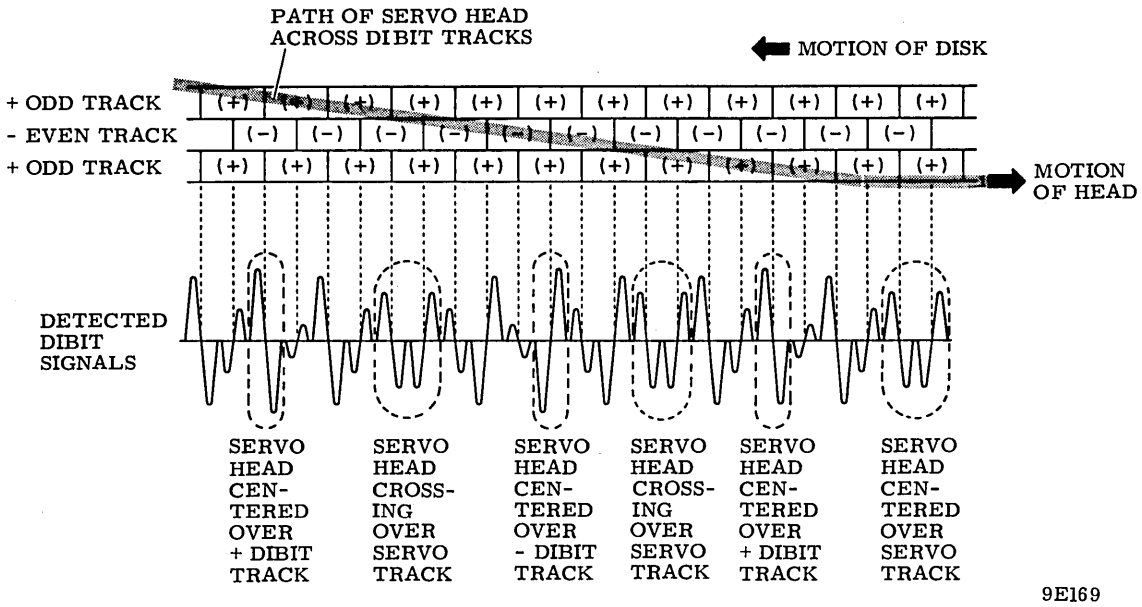


Figure 3-36. Servo Preamp Output

Dibits Sensing

The dibits sense circuit (refer to figure 3-35) detects the presence of dibits data. The output from this circuit is the Dibits Sense signal and it must be active (indicating dibits are present) for the position feedback circuits to function. This prevents them from generating false signals when no dibits are present (as for example during a heads load or when heads are unloaded).

The Dibits Sense signal is first enabled during the heads load sequence when the heads loaded switch transfers. The signal goes active when dibits with an amplitude of at least 145 mv peak to peak have been present for 3 ms. If the Dibits Signal should drop below this level for more than 50 us, the Dibits Sense signal goes inactive thus disabling the cylinder crossing, odd/even dibits clock and track servo amplifier circuits.

Therefore, losing dibits results in totally disabling the position feedback circuits.

Automatic Gain Control (AGC)

The purpose of the AGC circuits (refer to figure 3-35) is to provide gain control for the digits signal before applying them to the track servo amplifier and odd/even dibits clock circuits. This gain control is necessary for proper servo system operation. The outputs from the AGC circuits are the AGC'd Servo signals.

Gain control is obtained by feeding back a signal from the track servo circuit to the AGC circuits. This feedback signal, referred to as AGC, is derived from the AGC'ED Servo signals and the amplitude of the AGC and AGC'ED Servo signals are directly proportional. Therefore, when the AGC'ED Servo signals increase it causes an increase in the AGC signal and vice versa.

When the AGC signal increases, it causes a decrease in the gain of the AGC circuits. This results in reducing the amplitude of the AGC'ED Servo signal.

When the AGC signal decreases, the gain of the AGC circuits increases and the AGC'ED Servo signal becomes larger.

The net result is that the overall gain of the AGC Circuit remains constant.

Track Servo Signal Amplification

The track servo amplifier circuits (refer to figure 3-37) used the AGC'ED Servo signal from the AGC circuit and the Dibit read gate signals from the odd/even dibit clock circuits to product a signal that varies as the position of the servo head changes with respect to the dibit tracks. This signal is referred to as the track Servo signal.

The main elements in the track servo circuits are the peak detectors, peak detector buffers, AGC control amplifier and differential amplifier (refer to figure 3-37).

The peak detectors monitor the AGC'ED Dibits signals and are enabled by the Positive-Odd and Negative-Even Dibit Read Gate signals.

The positive peak detector is enabled by the Positive-Odd Dibit Read Gate signal and is active during the positive portion of the positive-odd dibit cycle. The negative peak detector is enabled by the Negative-Even Dibit Read Gate signal and is active during the negative portion of the negative-even dibit cycle. The peak detectors are inactive at all other times.

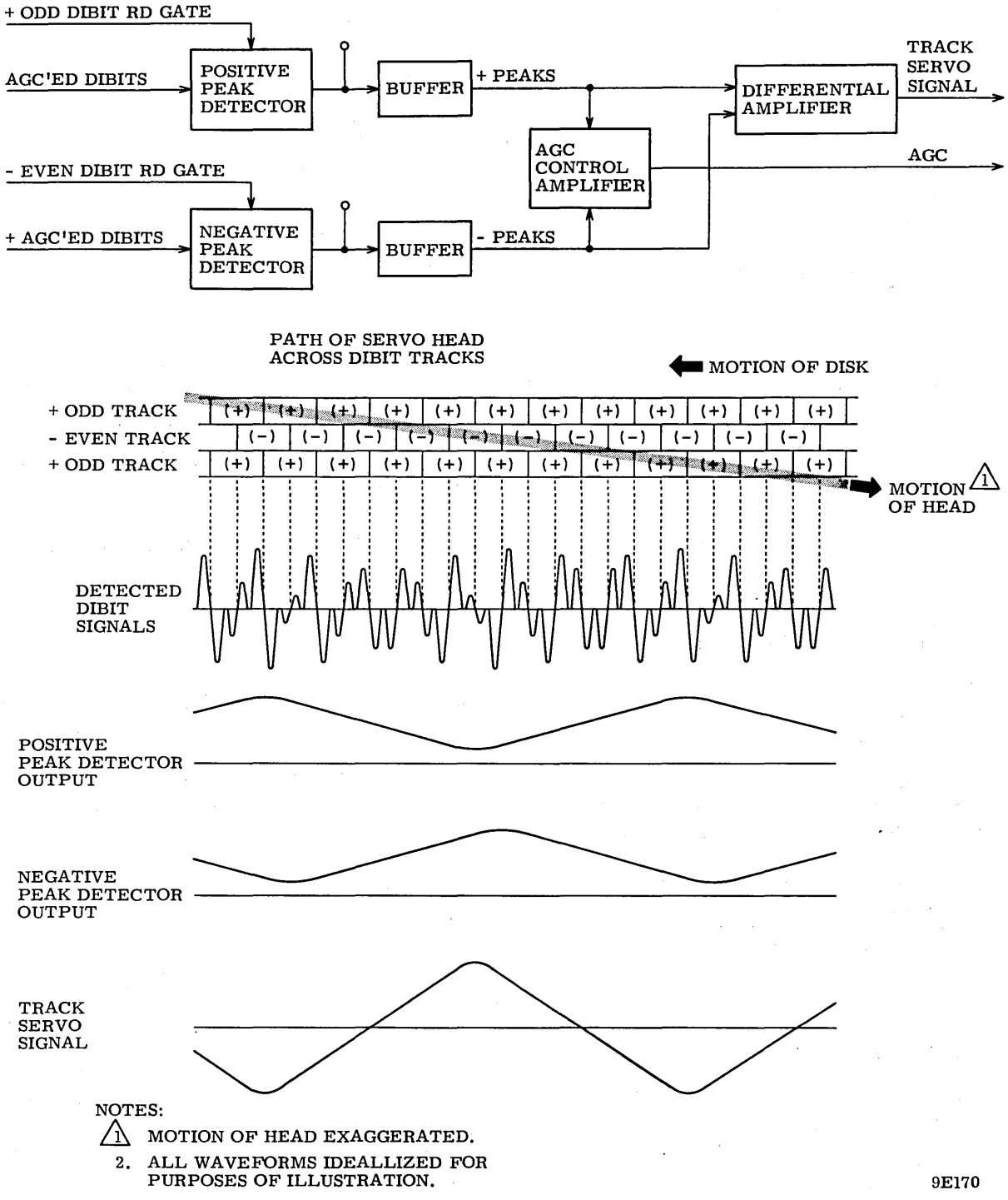


Figure 3-37. Track Servo Amplifier Circuit and Signals

This results in peak detector outputs that are proportional to the amplitude of the dibit signals they are monitoring. Therefore, the positive peak detector output is maximum when the servo head is over an odd dibit track and the negative peak detector output is maximum when the head is over an even dibit track (refer to figure 3-37).

The outputs of the peak detectors are processed by the peak detector buffers to provide signals of the proper amplitude and polarity for the AGC and differential amplifiers.

The AGC control amplifier uses the buffer outputs to generate the AGC voltage that is used by the AGC circuits.

The differential amplifier uses the two buffer outputs to produce a voltage with a polarity and magnitude directly proportional to the difference between them. This is the Track Servo signal.

The Track Servo signal is at its maximum positive value when the servo head is over even dibit tracks and maximum negative when the servo head is over odd dibit tracks.

If the servo head is centered over a servo track (between odd and even dibit tracks) the signal is zero. Therefore when the servo head moves through the servo zone, the Track Servo signal passes through zero each time the head crosses a servo track (refer to figure 3-37).

The Track Servo signal is applied to the Fine Position control and Cylinder crossing detection circuits. The Fine position control circuits use the Track Servo signal to control carriage movement during the last one-half track of a seek (and during forward EOT conditions). The Cylinder crossing detect circuits use the Track Servo signal to generate cylinder pulses as each servo track is crossed.

Odd/Even Dibits Clock Generation

The odd/even dibits clock circuit (refer to figure 3-38) generates Odd Dibits, Even Dibits and also the Odd and Even Dibits Read Clock signals. These signals are derived from the AGC'd Dibits signals applied to the level detectors.

The level detectors create digital pulses from the AGC'ED Dibits signals by switching state whenever they sense the corresponding odd or even dibit signals. The level detectors are enabled by the Sensing Dibits signal which is active only when dibits are being read from the disk.

The Odd and Even dibits Read Gate signals are generated when their respective one shots are triggered by the negative going edge of the level detector outputs. The dibit read gate signals are used to enable the track servo amplifier circuits.

The Odd Dibits and Even Dibits signals are produced by the outputs of the level detectors working in conjunction with the outputs of the dibits read gate one shots. The logic and timing for this is shown on figure 3-38.

The Odd Dibits and Even Dibits signals have a nominal frequency of 403 KHz. However, because they are derived from dibits which are in turn derived from the rotating disk, this frequency will vary with disk speed.

The Odd or Even Dibits signal is generated by ORing the Odd Dibits and Even Dibits signals. This produces an 806 KHz (nominal) signal which also varies with disk speed.

The Odd Dibits, Even Dibits and Odd or Even Dibits signals are used by the machine clock, index detection and End of travel detection circuits (refer to discussion on these circuits for more information).

Cylinder Crossing Detection

The cylinder crossing detection circuits (refer to figure 3-36) use the Track Servo signal to generate a pulse as each servo track is crossed.

The movement of the servo head across a servo track generates a Cylinder Pulse (refer to discussion on Cylinder Concept).

The cylinder crossings are detected by cylinder crossing detectors A and B. Cylinder crossing detector A produces an output pulse from the time the Track Servo signal goes through zero in a positive direction until it goes through -0.4 v in a negative direction. Cylinder crossing detector B produces an output pulse from the time the Track Servo signal goes through zero in a negative direction until it goes through +0.4 v in a positive direction.

This results in an overlapping of the two pulses after each zero crossing (refer to figure 3-39) and combining them produces a pulse to trigger the 10 us Cylinder Pulse one shot.

The 10 us Cylinder Pulses from the one shot are used by the direct seek coarse control circuits to count the number of cylinders crossed during a seek. They are also used by the End of Travel Detection circuits. Refer to the discussions on these circuits for further descriptions of how they are used.

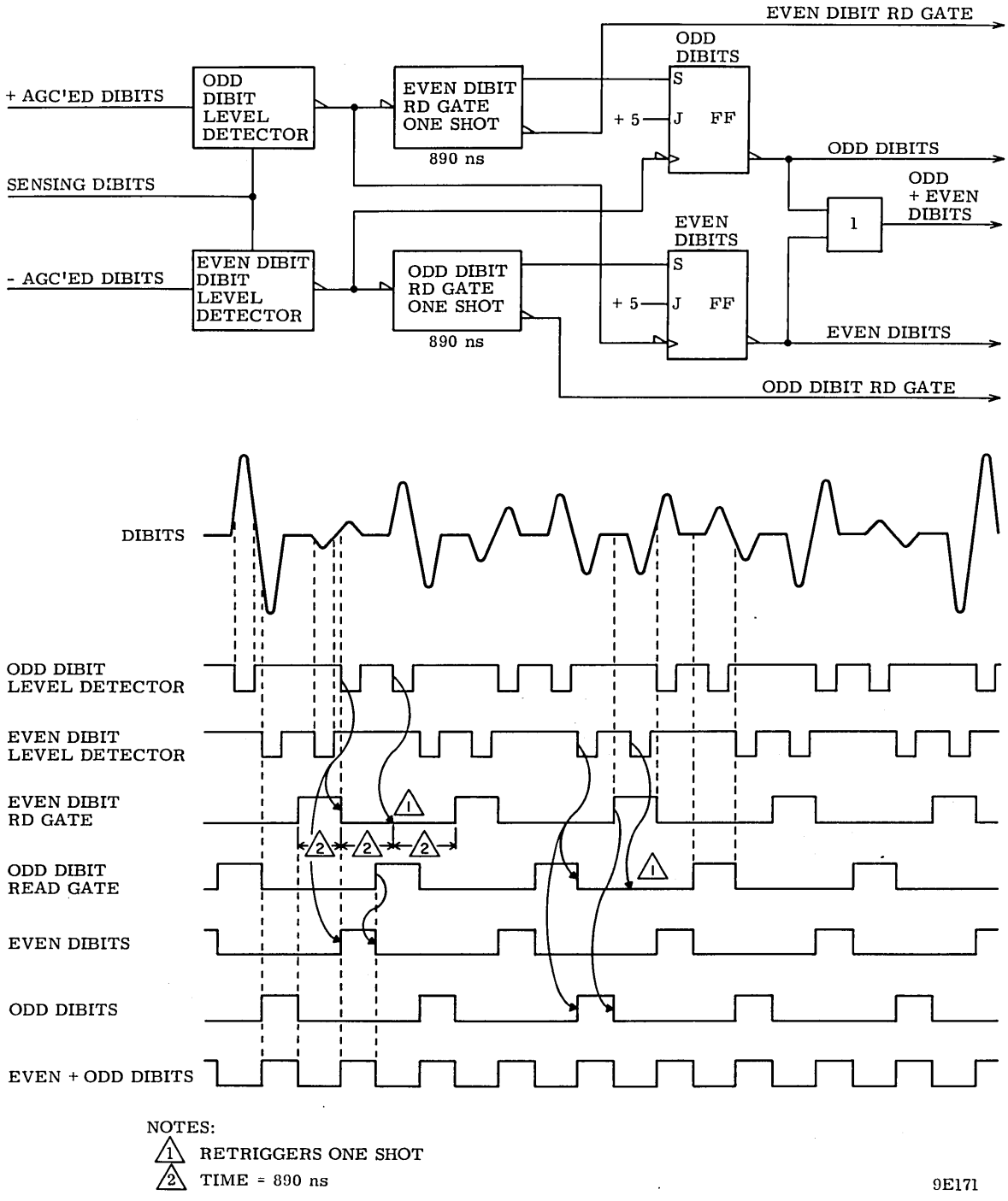


Figure 3-38. Odd/Even Dibits Clock - Logic and Timing

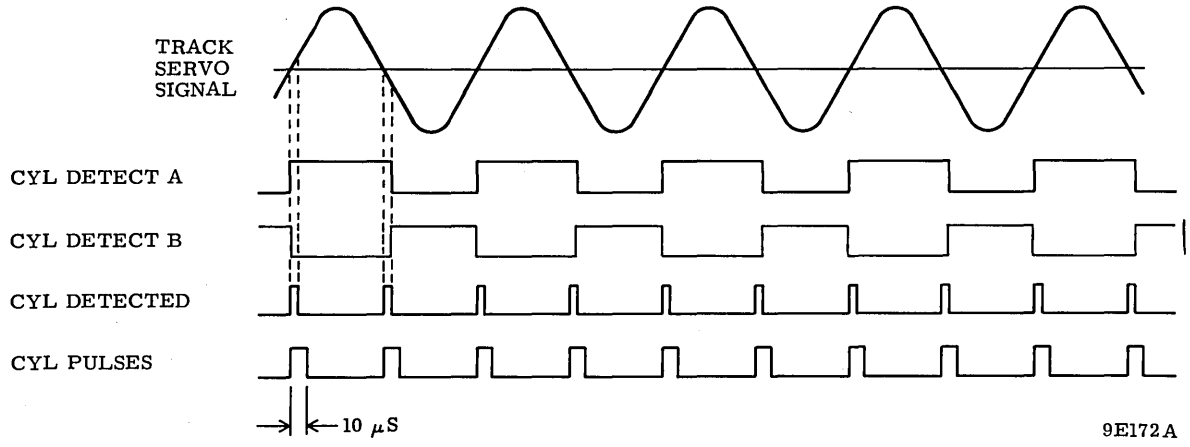


Figure 3-39. Cylinder Pulse Detection

It should be noted that the cylinder crossing detection circuits are operative only when the heads are loaded and dibits are being read from the disk. At all other times, the Sensing Dibits signals is inactive thus disabling the cylinder crossing detectors. This prevents false Cylinder Pulses from being generated.

End of Travel Detection

The end of travel (EOT) detection logic (refer to figure 3-40) is used to sense when the heads are outside of the data area and over one of the guard bands. Depending on the type of seek being performed, the output from this circuit will be interpreted as either an error indication or a feedback signal.

If the drive is performing a direct seek to one of the tracks in the data area, an EOT is interpreted as a positioning error and the proper error sequence is initiated. However if an RTZ or Load seek is being performed, the EOT signals are used as feedback for the load/RTZ coarse position control circuits.

The main elements in the EOT detection circuits are the EOT Integrator, EOT detectors and the Forward and Reverse EOT FFs.

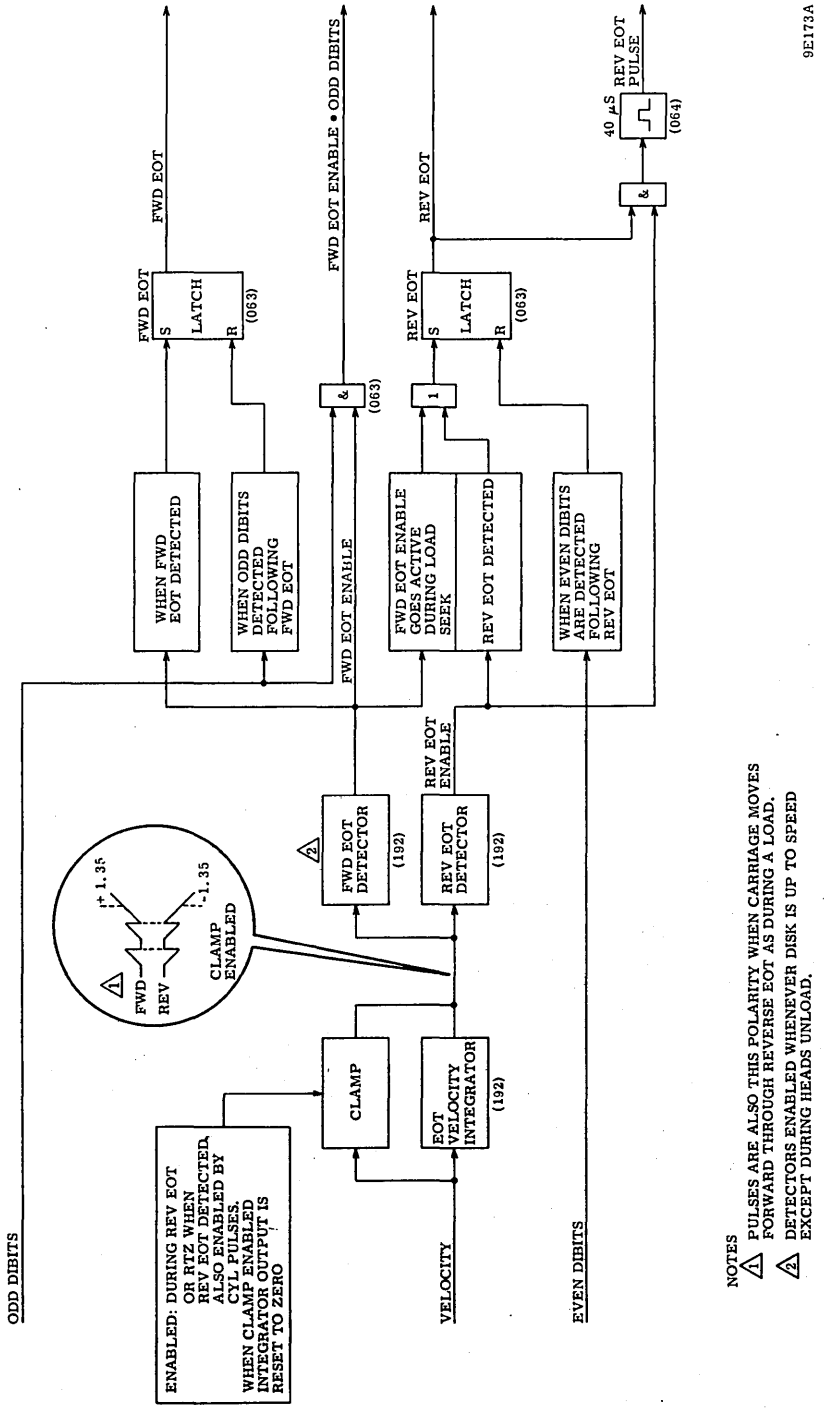


Figure 3-40. End of Travel Detection Circuits

The EOT Velocity Integrator works similar to the Desired Velocity Integrator in the direct seek coarse position control circuits. It monitors the Velocity signal and generates a sawtooth output waveform that rises from zero until reset by either a Cylinder pulse (when moving through data area) or by the Reverse EOT Pulse (during an RTZ when it detects the reverse EOT). If neither of these are present (as when moving over the outer or inner guard band) the output continues to rise.

The output from the EOT Velocity Integrator is monitored by the Forward and Reverse EOT detectors. The Forward EOT Detector is enabled whenever the integrator output exceeds +1.35 volts. This occurs either during a load when the heads are moving forward through the inner guard band or whenever the heads move into the outer guard band. In both of these cases the Velocity signal is of the proper polarity and there are no pulses to reset the integrator.

The Reverse EOT Detector is enabled whenever the Integrator output exceeds -1.35 volts. This occurs when the heads are moving in reverse over the inner guard band.

The Forward and Reverse EOT Enables are applied to the Forward and Reverse EOT FFs. The conditions causing these FFs to set and clear are shown on figure 3-40.

VELOCITY FEEDBACK GENERATION

The velocity of the carriage must be optimized to achieve the shortest seek time without overshooting or oscillating around the desired cylinder. The velocity feedback circuits (refer to figure 3-41) control the velocity (speed) of the carriage during a seek.

The velocity of the carriage is sensed by the velocity transducer. This is mounted within the magnet and consists of a stationary coil and movable magnetic core (refer to figure 3-20).

When the carriage moves, the core moves thus inducing an EMF in the coil. This EMF is converted by the velocity amplifier into the velocity signal.

The amplitude of this signal varies with the speed of the carriage and the polarity depends on the direction of movement. If the seek is in a forward direction, the polarity is negative and if it is in a reverse direction the polarity is positive.

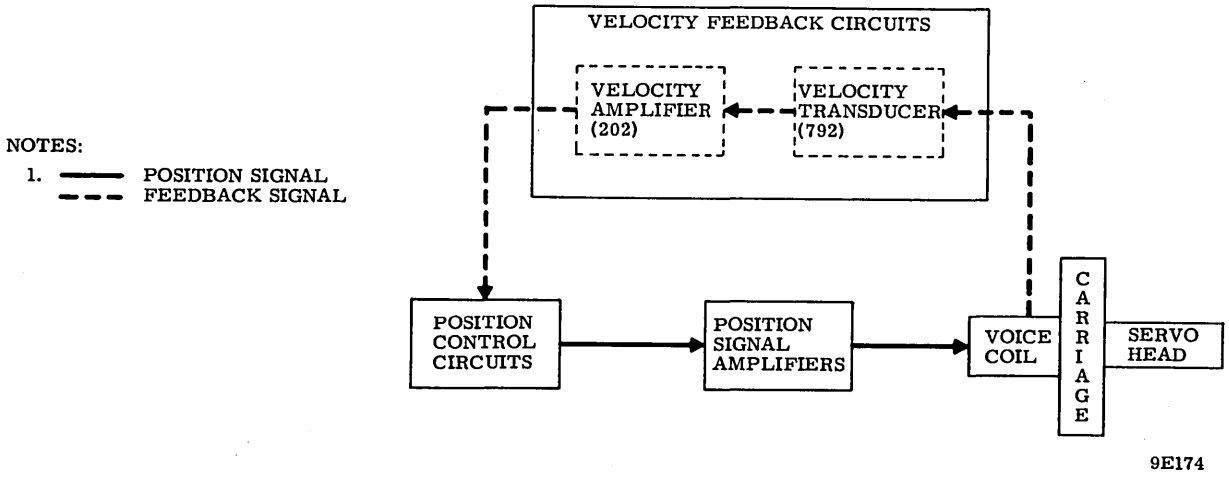


Figure 3-41. Velocity Feedback Circuits

Refer to the discussion on Electromechanical Functions for further description of the velocity transducer.

POSITION SIGNAL AMPLIFICATION

The signals from the position control circuits are processed by the position amplifier circuits (refer to figure 3-42) to provide the current for the voice coil.

Any one of the three position signals may provide the input to these circuits depending on the type of seek being performed and how close the heads are to the destination. This input is applied to the summing amplifier.

The output from the summing amplifier is then applied to the power amplifier driver which uses it to generate the Forward and Reverse Current signals. These signals are sent to the power amplifier.

The power amplifier uses the Forward and Reverse Current signals to produce a voice coil current with the proper polarity and amplitude to move the voice coil and carriage thereby positioning the heads.

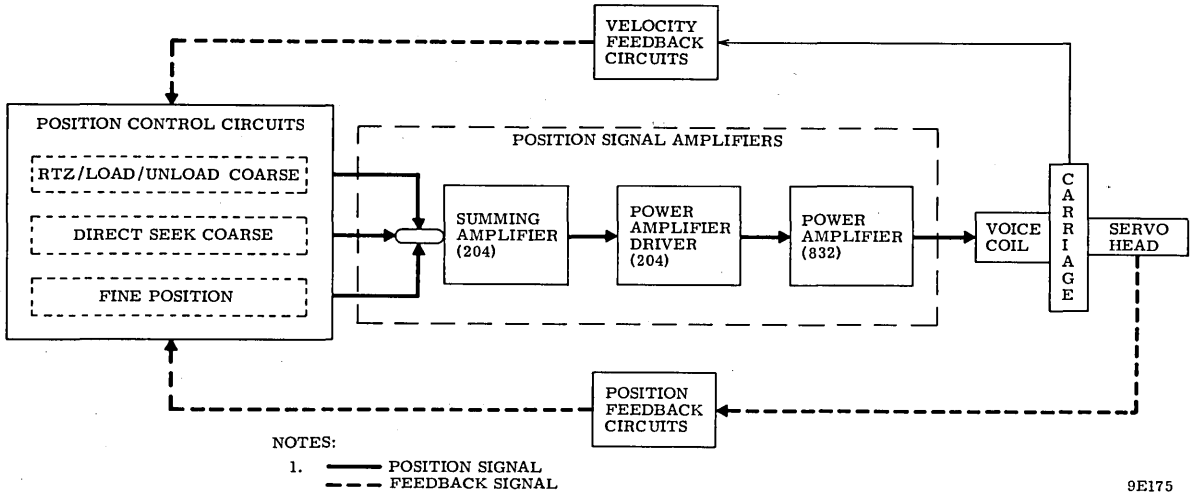


Figure 3-42. Position Signal Amplifier Circuits

DIRECT SEEK POSITION CONTROL

General

A direct seek is one in which the drive is commanded by the controller to move the heads from their current logical cylinder location to another specified by the controller.

The controller initiates direct seek via the High Cylinder (Tag 100) and Low Cylinder (Tag 110) commands.

The High Cylinder command is used to transmit the two high order bit (2^8 and 2^9) of the new cylinder address (150 MB units use only 2^8). The High Cylinder command always precedes the Low Cylinder command and the drive stores the high order address bits (or bit) until the Low Cylinder command is received.

The Low Cylinder command is used to transmit the eight low order bits (2^0 - 2^7) of the cylinder address and to actually initiate the seek.

The direct seek function is divided into two phases: (1) coarse and (2) fine. The coarse mode consists of all but the last half cylinder of the seek. The servo system is in fine mode during the last half cylinder and while the heads are tracking over the desired cylinder.

The following discussions describe both the coarse and fine modes. Figure 3-43 is a flow chart of the entire direct seek function.

Direct Seek Coarse Control

General

The direct seek is controlled by the direct seek coarse control circuits for all but the last half cylinder of the seek. Figure 3-44 shows these circuits and the signals they generate.

The three main inputs to these cylinders are the address of the destination cylinder (received from the controller in conjunction with the cylinder address tags), the Cylinder pulses (received from the position feedback circuits), and the velocity feedback circuits). These signals are used to produce a coarse positioning signal that varies with distance and also controls the speed of the carriage as it moves toward the destination.

How the coarse positioning signal is generated and also how the loop operates under coarse control is explained in the following paragraphs.

Coarse Position Signal Generation

At the start of the seek, the distance to the destination cylinder is determined by the adder. It does this by comparing the address sent by the controller with the address presently contained in the cylinder address register (this is the address at which the heads are presently located) and then generating a difference count indicating how many logical cylinders the heads will have to cross in reaching the new address.

The difference count is loaded into the Difference counter. After the difference counter is loaded, the address (received from the controller) is loaded into the Cylinder Address register and will be the present address at the start of the next seek.

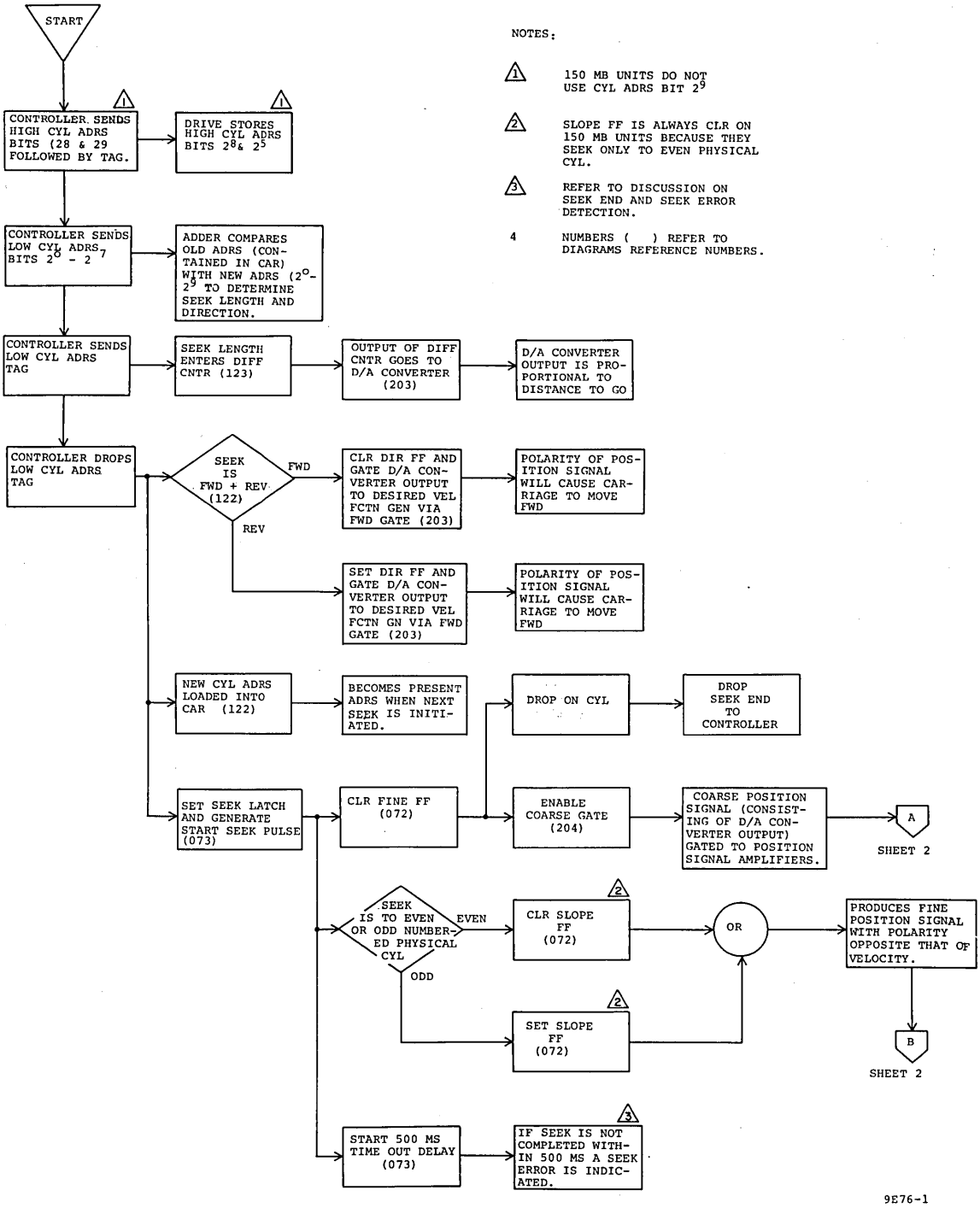


Figure 3-43. Direct Seek Flow Chart (Sheet 1 of 2)

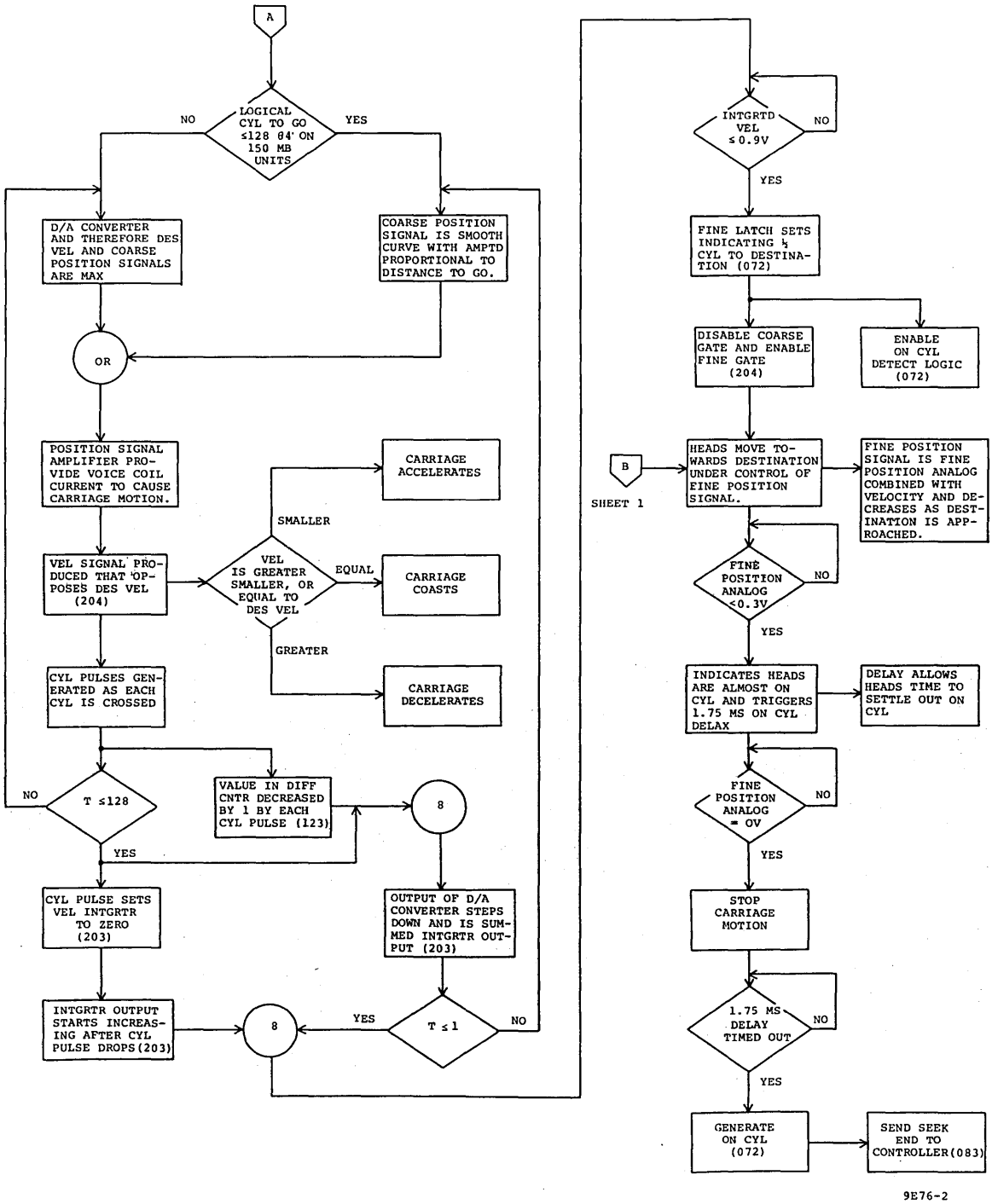


Figure 3-43. Direct Seek Flow Chart (Sheet 2)

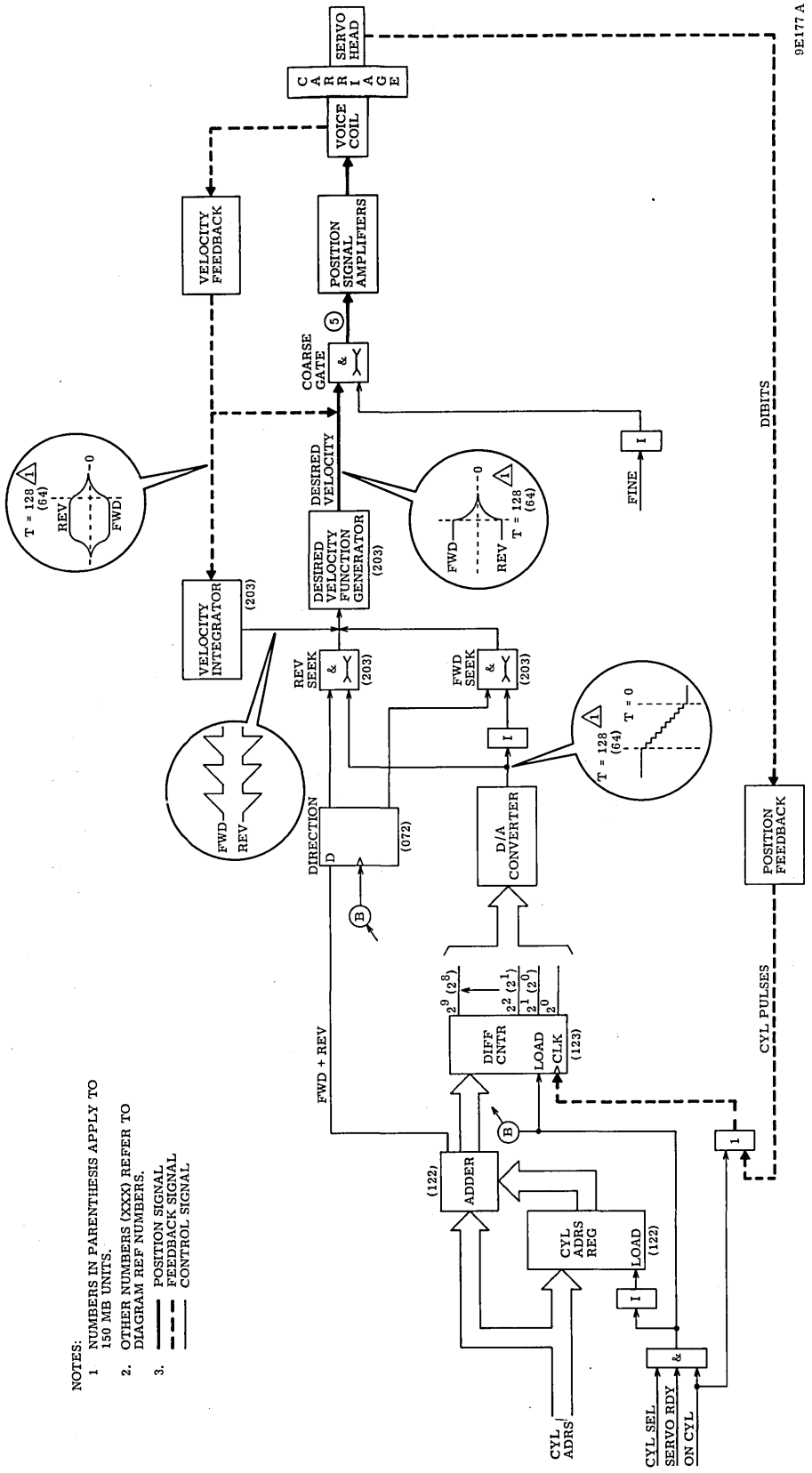


Figure 3-44. Direct Seek Coarse Position Control Circuits

The Difference counter is decremented by the cylinder pulses as each logical cylinder is crossed thus keeping track of the number of logical cylinders left in the seek. It should be noted that because the 150 MB units can seek to only the even numbered physical cylinders only every other cylinder pulse (those associated with even numbered cylinders) decrement the Difference counter. This is accomplished by not using the lowest order stage of the counter and is shown on figure 3-44. In both 150 MB and 300MB units the seven low order bits of the Difference counter go to the D/A converter.

The output of the D/A converter is determined by the value of the input bits from the Difference counter. When these bits are all active, the D/A Converter output is maximum. This is the case where the number of logical cylinders to go exceeds 128. However, when logical cylinders to go are less than 64 (150 MB) or 128 (300 MB), the D/A Converter output steps down (with the counter output) as each logical cylinder is crossed.

The D/A Converter output signal is gated via either the Forward or Reverse gate to the Desired Velocity Function Generator. The output of the Desired Velocity Function Generator (Desired Velocity) varies in amplitude with the D/A Converter output (and therefore with distance to the destination) and in polarity with direction of the seek.

The seek direction is determined at the start of the seek by the adder which generates the Forward or Reverse signal. This signal is used to either set or clear the Direction FF and thereby enable either the Forward or Reverse Gate.

If the seek is in a forward direction (towards the spindle), the Direction FF is cleared thus enabling the Forward gate. This causes a Desired Velocity signal that varies from a negative voltage to zero.

If the seek is in a reverse direction (away from the spindle), the Direction FF is set thus enabling the Reverse gate. In this case, the Desired Velocity signal varies from a positive voltage to zero.

In either case the output from the D/A Converter must be smoothed out during the last 64 (150 MB) or 128 (300 MB) logical cylinders of a seek to prevent steps from appearing in the Desired Velocity output. This function is performed by the Velocity Integrator.

The Velocity Integrator is enabled when logical cylinders to go reaches 64 (150 MB) or 128 (300 MB) and at this point starts generating sawtooth pulses. These pulses start from zero at the time the Cylinder pulse goes false (which occurs after the cylinder crossing) and rises until reset by the next cylinder pulse (which occurs at the next cylinder crossing).

When the sawtooth pulses are summed with the D/A Converter output, the resulting Desired Velocity signal is a smooth curve that decreases in amplitude with distance to te destination cylinder.

The Desired Velocity signal is then summed with the Velocity signal which is received from the velocity feedback circuits. The Velocity signal varies in amplitude with carriage speed and is opposite in polarity to the Desired Velocity signal. It is necessary to sum Desired Velocity with Velocity in order to control carriage speed and thus ensuring minimum seek time without overshooting the destination cylinder.

The resultant signal, Desired Velocity summed with Velocity, is the final output of the coarse position circuits and is applied to the position signal amplifiers via the coarse gate.

Loop Operation During Coarse Control

The position signal amplifiers use the output from the coarse position amplifiers circuits to produce current for the voice coil. This current controls carriage motion.

The coarse control position of a typical direct seek can be divided into three phases:

- Accelerate Phase - Voice coil receives maximum current and carriage accelerates from zero to maximum velocity.
- Coast Phase - Carriage is at maximum velocity and coasts along under its own inertia.
- Deceleration Phase - Carriage approaches destination and must slow down to avoid overshoot.

It should be noted that it takes about 60 cylinders for the carriage to reach maximum velocity (about 55 in/sec.). During shorter seeks, particularly those less than 64 (150 MB) or 128 (300 MB) logical cylinders, maximum velocity will not be obtained. In cases where maximum velocity is not reached the primary functions remain the same but the coast phase will not occur (or be very short) and the carriage begins to decelerate sooner.

The following describes how the servo loop operates during a typical direct seek long enough for the drive to obtain maximum velocity. The signals generated are shown on figure 3-45.

The acceleration phase occurs during the first part of the seek. At this time, the carriage is stationary and the output from the coarse gate is due entirely to the Desired Velocity signal with no opposing Velocity signal. Therefore, voice coil current is maximum in the direction necessary to cause maximum carriage acceleration.

As the carriage accelerates a Velocity signal is generated by the velocity feedback circuits. Because this signal opposes the Desired Velocity signal, the resultant signal to the position signal amplifiers is reduced thereby reducing voice coil current. However, Desired Velocity signal is still greater and the carriage continues to accelerate.

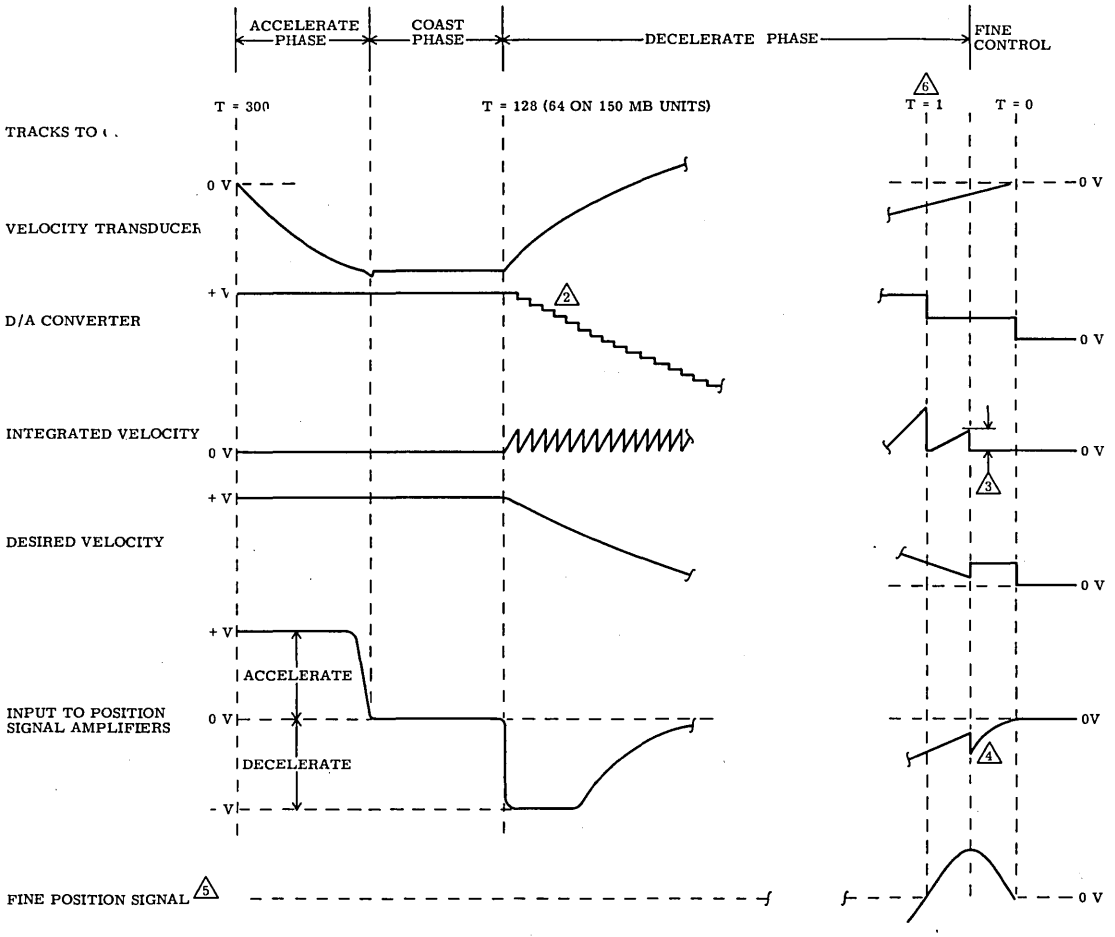
Eventually carriage speed increases to the point where the Velocity signal equals the Desired Velocity signal and the two signals cancel one another. This causes the positioning signal from the coarse gate, and therefore the voice coil current, to drop to zero. The carriage now coasts along at maximum velocity of about 55 in/sec.

As the carriage coasts, friction losses and back EMF of the moving voice coil tend to slow it down. However, when this occurs the velocity signal becomes less than the Desired Velocity signal (which is still maximum) thus causing enough voice coil current to speed up the carriage until the two signals cancel again.

This continues as long as the Desired Velocity signal remains at its maximum value, which is until less than 64 (150 MB) or 128 (300 MB) logical cylinders remain in the seek. Beyond this point, the carriage starts to decelerate.

When less than 64 (150 MB) or 128 (300 MB) logical cylinders remain, the D/A Converter starts to step down thus causing the Desired Velocity signal to decrease. When Desired Velocity is less than Velocity, current is applied to the voice coil in the reverse direction causing the carriage to slow down until the Velocity signal is again equal to Desire Velocity. The carriage now coasts under its own inertia until the D/A Converter steps down again.

This process continues and the carriage gradually slows down as the destination cylinder is approached. When the heads are within one-half cylinder of the destination, the servo system switches to fine control.



NOTES:

1. SIGNALS SHOWN APPLY TO FWD SEEK ABOUT 300 CYL IN LENGTH. ALL POLARITIES EXCEPT D/A CONVERTER ARE OPPOSITE FOR REV SEEKS. TIMING AND AMPLITUDE ARE NOT TO SCALE.

2. OUTPUT DECREASES WITH EACH CYLINDER PULSE.

3. SERVO SYSTEM SWITCHES TO FINE CONTROL WHEN INTEGRATED VELOCITY EXCEEDS 0.9 V.

4. GAIN CHANGE CAUSED BY SWITCH FROM COARSE TO FINE CONTROL. SIGNAL FOR LAST HALF TRACK IS DUE TO FINE POSITION INPUT AND IS SHOWN HERE FOR REFERENCE ONLY.

5. FROM FINE POSITION CONTROL CIRCUITS AND IS SHOWN FOR REFERENCE ONLY.

6. SCALE EXPANDED FOR CLARITY BEYOND T = 1.

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Figure 3-45. Direct Seek Coarse Position Control Signals

Direct Seek Fine Control

General

The last half track of a direct seek is controlled by the fine position control circuits (refer to figure 3-46). These circuits generate the signal used to bring the drive over the desired cylinder and to keep it tracking properly over this cylinder.

In addition to this, these circuits also control coarse to fine switching and generate the On Cylinder signal. The following paragraphs describe all of these functions and is divided into these areas:

- Fine to Coarse Switching
- Fine Position Signal Generation and Basic Loop Operation
- On Cylinder Detection
- Track Following

Figure 3-46 shows the fine position control circuits and figure 3-47 shows timing during fine position control.

Coarse to Fine Switching

Coarse to fine switching is controlled by the Fine latch. When this latch is set, the Fine gate is enabled and the output of the fine position control circuits is gated to the position signal amplifiers. Whenever this latch is cleared, the coarse gate is enabled thus putting the servo system in coarse control.

During a direct seek, the Fine latch is cleared at the start of the seek and remains clear until the heads are within one-half cylinder of the destination.

The coarse to fine sequence starts when the Difference counter indicates one logical cylinder to go. At this time the $T \leq 1$ signal goes active indicating the last cylinder is being crossed.

The one-half cylinder point is sensed by the fine control level detect circuit. The input to this circuit is the Integrated Velocity signal (refer to discussion on Direct Seek Coarse Control) which is set to zero by the same cylinder pulse that decrements the Difference counter to one. When this cylinder pulse drops, the Velocity Integrator output starts to increase again. When it reaches 0.9 V, the heads are about one-half

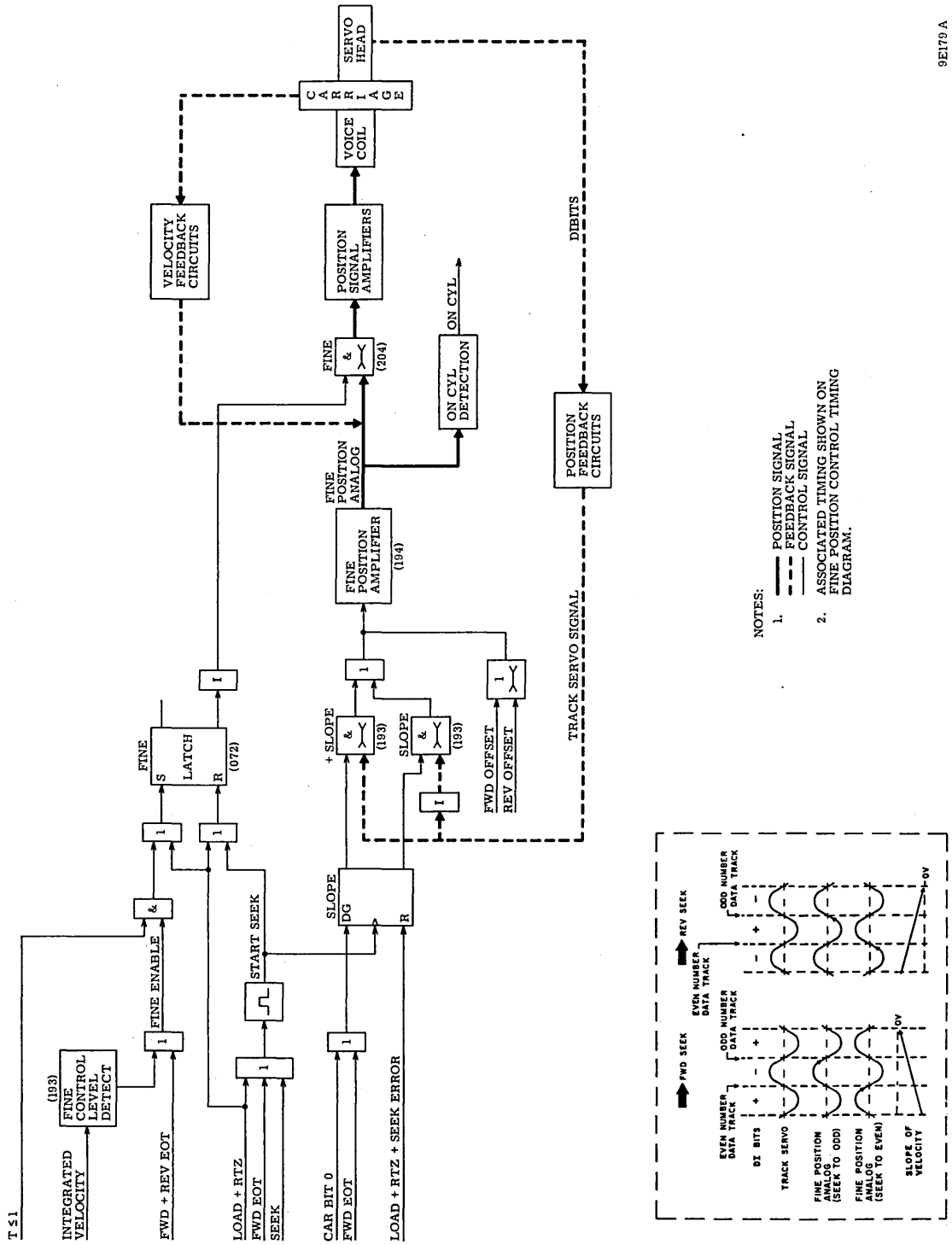
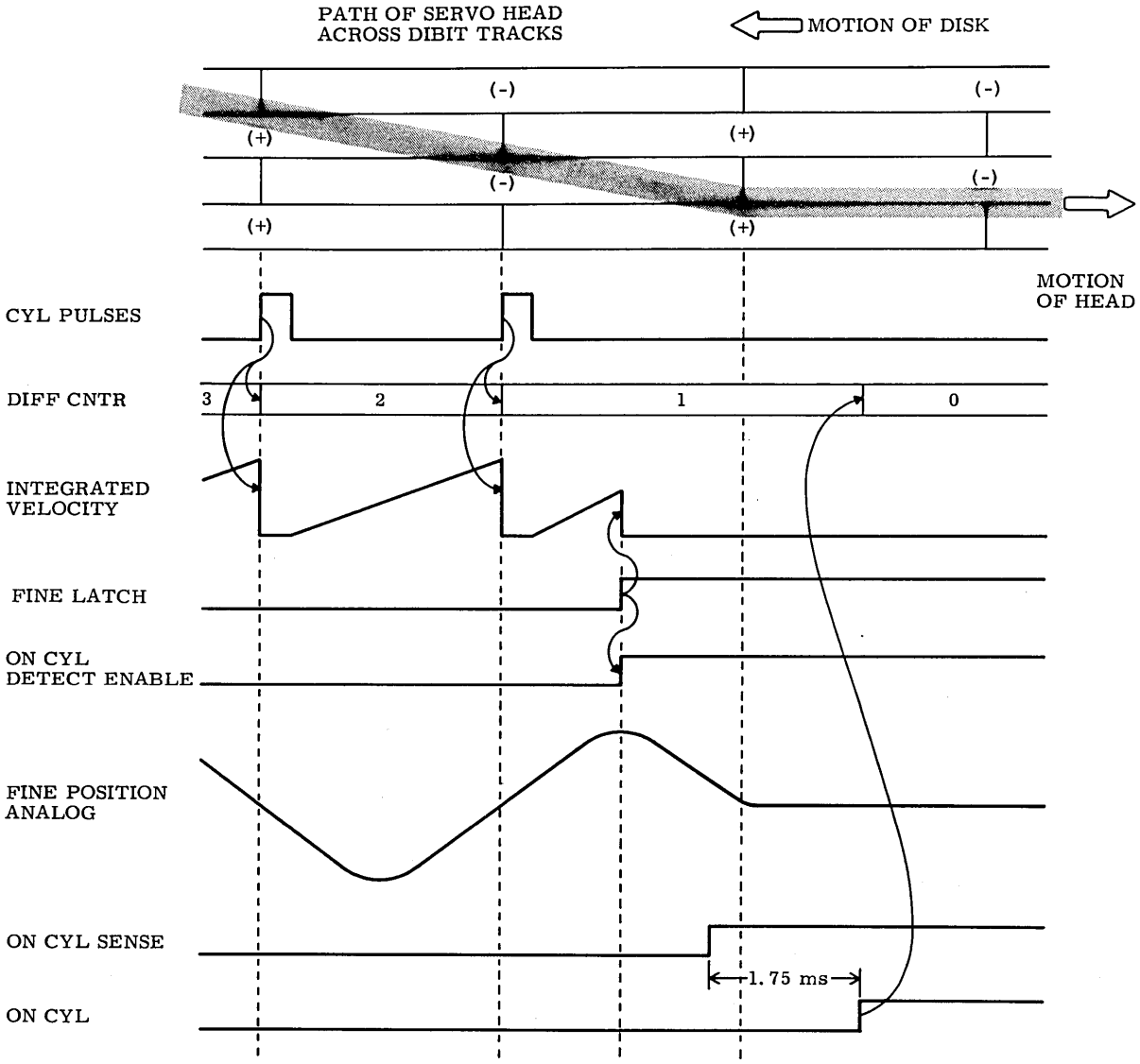


Figure 3-46. Fine Position Control Circuits



NOTES:

1. REFER TO FIGURES SHOWING FINE POSITION CONTROL AND ON CYL DETECTION CIRCUITS FOR LOGIC ASSOCIATED WITH THIS TIMING.

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Figure 3-47. Fine Position Control Timing

cylinder from the centerline of the destination cylinder and this causes the fine control level detect output to go active. This in turn causes the Fine Enable signal to go active. The Fine Enable signal is then ANDed with the T≤1 signal to set the Fine latch.

When the Fine latch sets, the coarse gate is disabled and the Fine gate is enabled thus gating the fine positioning signal to the position signal amplifiers.

Fine Position Signal Generation

The fine positioning signal is produced by combining The Fine Position Analog and Velocity signals. The Fine Position Analogue signal varies with distance to the destination cylinder centerline and Velocity varies with speed of the carriage.

The Fine Position Analog signal is derived from the Track servo signal which is received from the position feedback circuits and provides the position feedback during fine control. The amplitude of the Fine Position Analog and Track Servo signals are directly proportional and as the heads approach the centerline of the destination cylinder both signals decrease from maximum to zero.

The Fine Position Analog signal is summed with the Velocity signal to provide speed control. These signals are of opposite polarity with the polarity of Fine Position Analog such as to cause an increase in carriage speed and the polarity of Velocity such as to cause a decrease.

Because during this phase, the carriage must decelerate, the amplitude of the Velocity signal will normally be greater than that of Fine Position Analog. How much greater depends on the speed of the carriage.

If the carriage starts moving too fast, the Velocity signal will increase and therefore exceed Fine Position Analog by a greater amount. This results in greater deceleration. However, if the carriage decelerates too quickly the Velocity signal decreases and approaches that of Fine Position Analog resulting in less deceleration.

Ideal speed is obtained when the two signals are nearly equal and the resultant produces a voice coil current that brings the heads to rest at the destination cylinder without overshoot or oscillation.

Because of the polarities of the Velocity and Fine Position Analog signals must be opposite, it is sometimes necessary to invert the Track Servo signal to obtain the proper polarity of Fine Position Analog. This is the case, because although the Velocity signal always has the same polarity (negative for forward seeks, positive for reverse seeks), the polarity of the Track Servo signal depends on whether it is approaching an odd or even numbered physical cylinder. On forward seeks, the Track Servo signal decreases from a maximum positive to zero when approaching an odd cylinder and increases from a maximum negative to zero when approaching an even cylinder. The opposite is true for reverse seeks. Refer to discussion on position feedback for more information on Track Servo signal generation.

What polarity the Fine Position Analog signal, which is derived from the Track Servo signal, will have is controlled by the Slope FF. This FF is either set or cleared at the start of the seek.

If the seek is to an odd numbered cylinder, the Slope FF is set and the Fine Position Analog and Track Servo signals are of the same polarity. If the seek is to an even numbered cylinder the Slope FF is cleared and the signals are of opposite polarities. It should be noted that this FF is always clear on 150 MB units because they seek only to even numbered physical cylinders (refer to discussion on Physical to Logical Cylinder/ Track Correlation). The phase relationships between the Track Servo and Fine Position Analog signals are shown on figure 3-46.

When the heads are centered over and tracking over the destination cylinder, both the Fine Position Analog and Velocity signals are zero. When this occurs the heads are considered to be on cylinder. This condition is sensed by the on cylinder detection circuits.

On Cylinder Detection

On Cylinder detection is enabled when the servo system goes into fine control (Fine latch sets). At this time, the on cylinder detection circuits (refer to figure 3-48) start to monitor the Fine Position Analog signal. When this signal is small enough to indicate the heads are approximately over the servo track (of the destination cylinder), Cylinder Detect A and B signals go active thus enabling the On Cylinder Sense signal. The On Cylinder Sense signal triggers the 1.75 ms On Cylinder Delay which allows the heads time to settle out over the servo track. When the delay times out the On Cylinder FF sets.

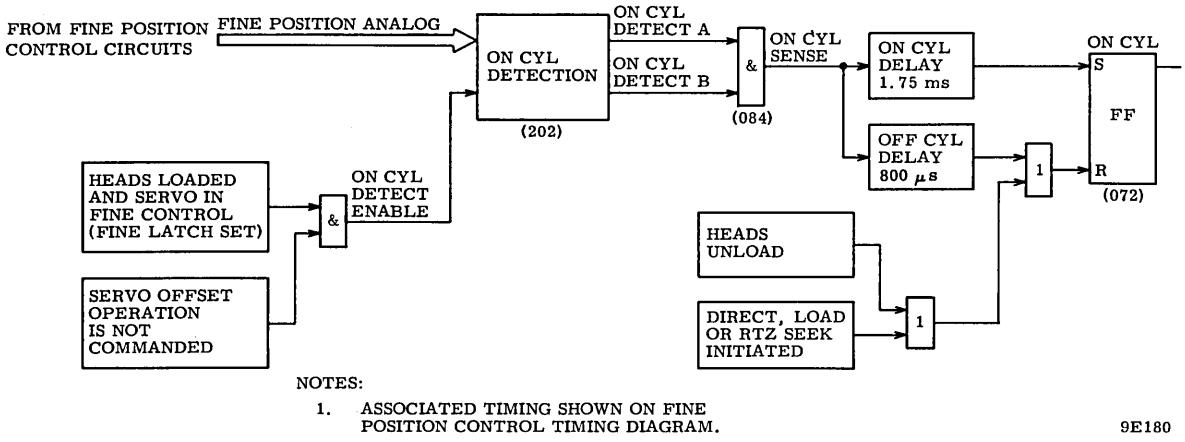


Figure 3-48. On Cylinder Detection Logic

The On Cylinder signal cause the Seek End line to the controller to go active and is also used to perform various functions within the drive logic.

Track Following

Even after the on cylinder position is obtained it is necessary to keep the servo system under control of the fine position control circuits. This is necessary to ensure that the heads do not drift far enough off the track centerline to cause errors during a read or write operation.

If the heads should drift off the centerline, the Track Servo signal will increase or decrease slightly from zero (depending on th direction of the drift) and this is translated into the Fine Position Analog signal. The polarity of the Fine Position Analog is such that the position signal amplifier generates the proper voice coil current to drive the heads back to the track centerline.

If the heads drift sufficiently to cause a Fine Position Analog signal greater than 0.4 V for more than 800 us, the Off Cylinder Delay times out causing the On Cylinder FF to clear.

This in turn causes a seek error to be generated (refer to discussion on Seek End and Seek Error Detection).

It is possible for the controller to command the drive to move the heads slightly off the track centerline if it is necessary for data recovery. This is done via an Error Recovery command (Tag 001) and either Bus Out bit 2 or Bus Out bit 3 active.

If Bus Out bit 2 (Positive Offset) is active, the heads move about 250 uin towards the spindle. If Bus Out bit 3 (Negative Offset) is active, the heads move about 250 uin away from the spindle.

In both cases, the bias signal is summed with the normal position signal at the input to the fine position amplifier (refer to figure 3-46). This causes the carriage to move until the Track Servo signal, which is of a polarity to move the heads back to the centerline, equals and cancels the bias signal.

LOAD SEEK POSITION CONTROL

General

During a load seek, the heads are moved from the fully retracted position and positioned out over the disk pack at cylinder 000.

The load seek must be successfully completed before the drive can respond to a read, write or seek command from the controller. When the sequence is completed, the Seek End line goes true and the READY indicator on the drives operator control panel lights.

The seek is initiated at the same time as the power on sequence by pressing the START switch. However, the actual positioning does not begin until after the power on sequence is complete (disk pack is up to speed). The positioning is divided into coarse and fine modes which are explained in the following. The power on sequence is described in the Power System Discussion.

Figure 3-49 is a flow chart of the entire load sequence (except for power on).

Load Seek Coarse Control

The servo system is under coarse control from the time the load is initiated until the reverse end of travel zone (refer to discussion on Servo Disk Information) is detected. The circuits involved are shown on figure 3-50 and the timing is on figure 3-51.

The load seek coarse control sequence begins when the power on sequence has been completed and the disk has reached 3000 revolutions per minute. At this time, the load latch sets and enables the Load Gate. The Load Gate combines a bias signal with the Velocity signal and applies the resultant signal to the position signal amplifiers. This causes the carriage to move forward at about seven inches per second.

When the heads are over the disk, the heads loaded switch transfers to the heads loaded position thus enabling the dibits sense logic (refer to discussion on Dibits Sensing). The drive now starts searching for the positive-odd dibits indicating the reverse end of travel area.

Because the heads are moving in a forward direction and the polarity of the Velocity signal is such as to cause the Forward EOT Enable signal to go active (refer to discussion on End of Travel Detection), when positive-odd dibits are detected, the Forward EOT Odd Dibits signal also goes active. This causes the Load latch to clear thus disabling the Load gate. It also sets the Reverse EOT FF which in turn causes the Fine latch to set thereby enabling the Fine gate. The carriage is now controlled by the fine position control circuits (refer to figure 3-47).

If for any reason the dibits signals are not detected within 350 ms after the Load latch is set, the RTZ latch sets and the heads unload to the fully retracted position. This also causes the Fault latch to set and FAULT indicator to light.

Pressing the FAULT switch (extinguishing the indicator) clears the fault latch and initiates another load seek. However, the head will unload again thus lighting the FAULT indicator and setting the Fault latch if dibits are not detected within 350 ms.

Load Seek Fine Control

The fine positioning signal used during load seek fine control is the same as is used during direct seeks and the component of this signal that varies with distance to the destination is also derived from the Track Servo signal.

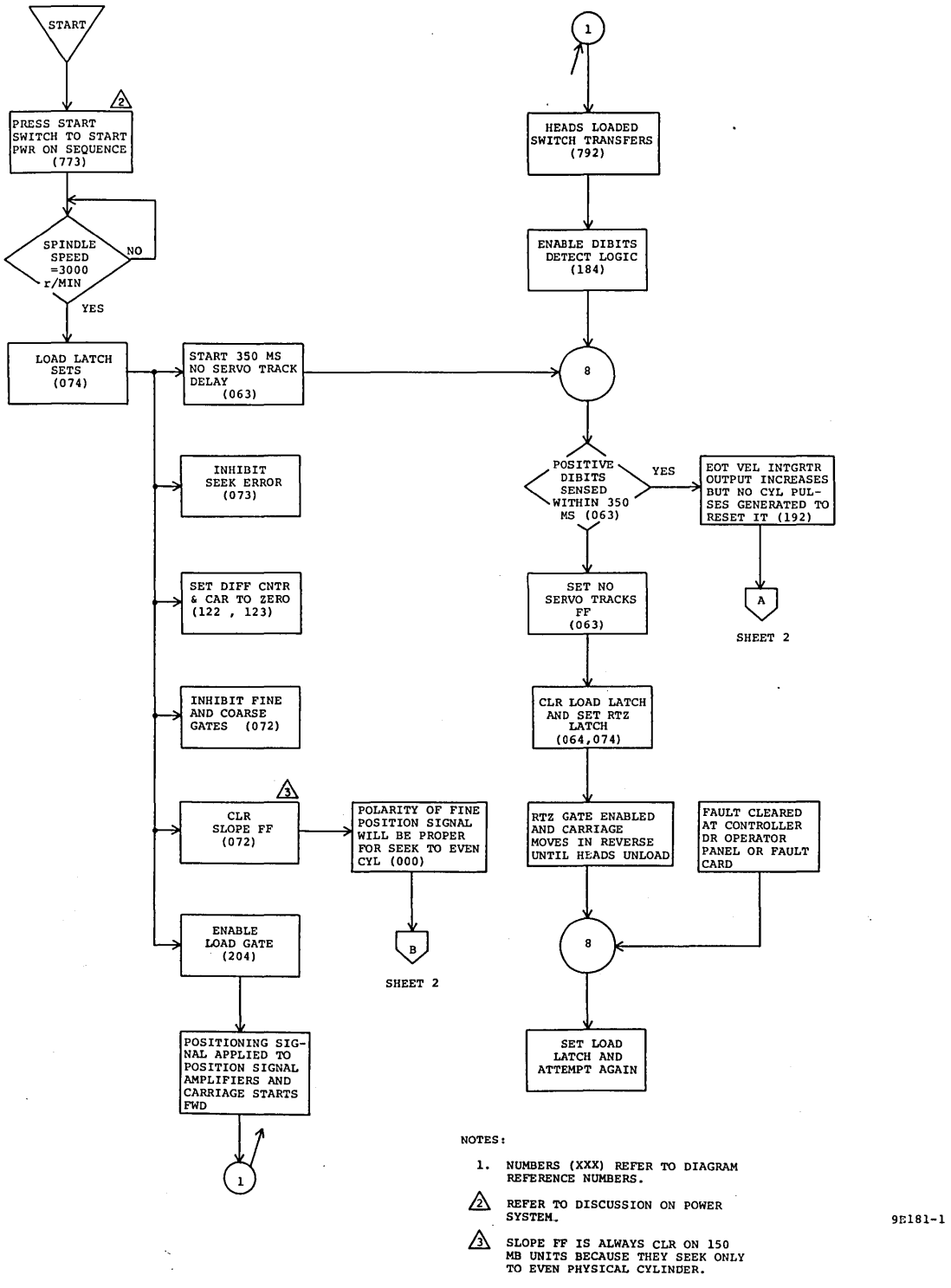


Figure 3-49. Load Seek Flow Chart (Sheet 1 of 2)

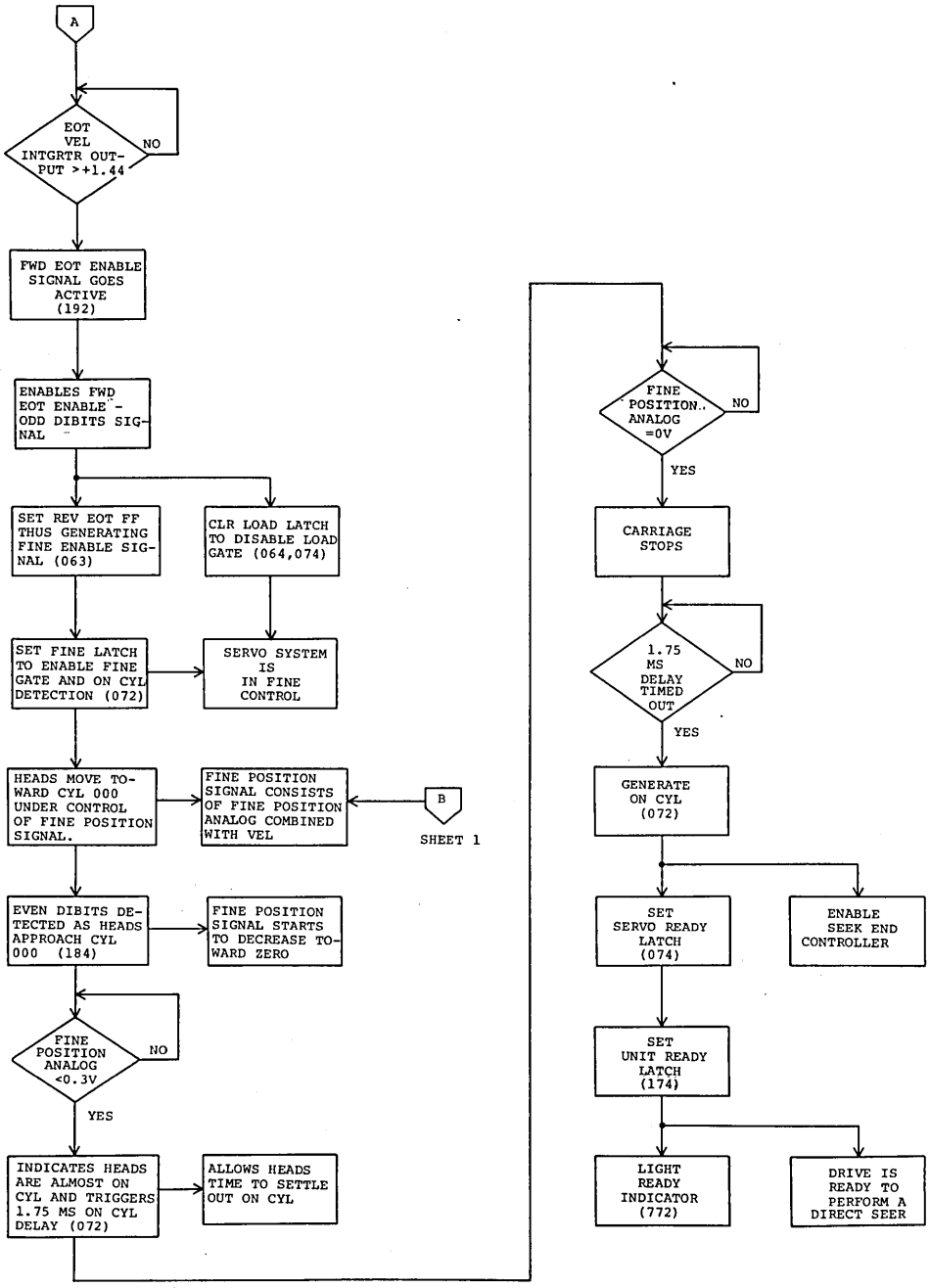


Figure 3-49. Load Seek Flow Chart (Sheet 2)

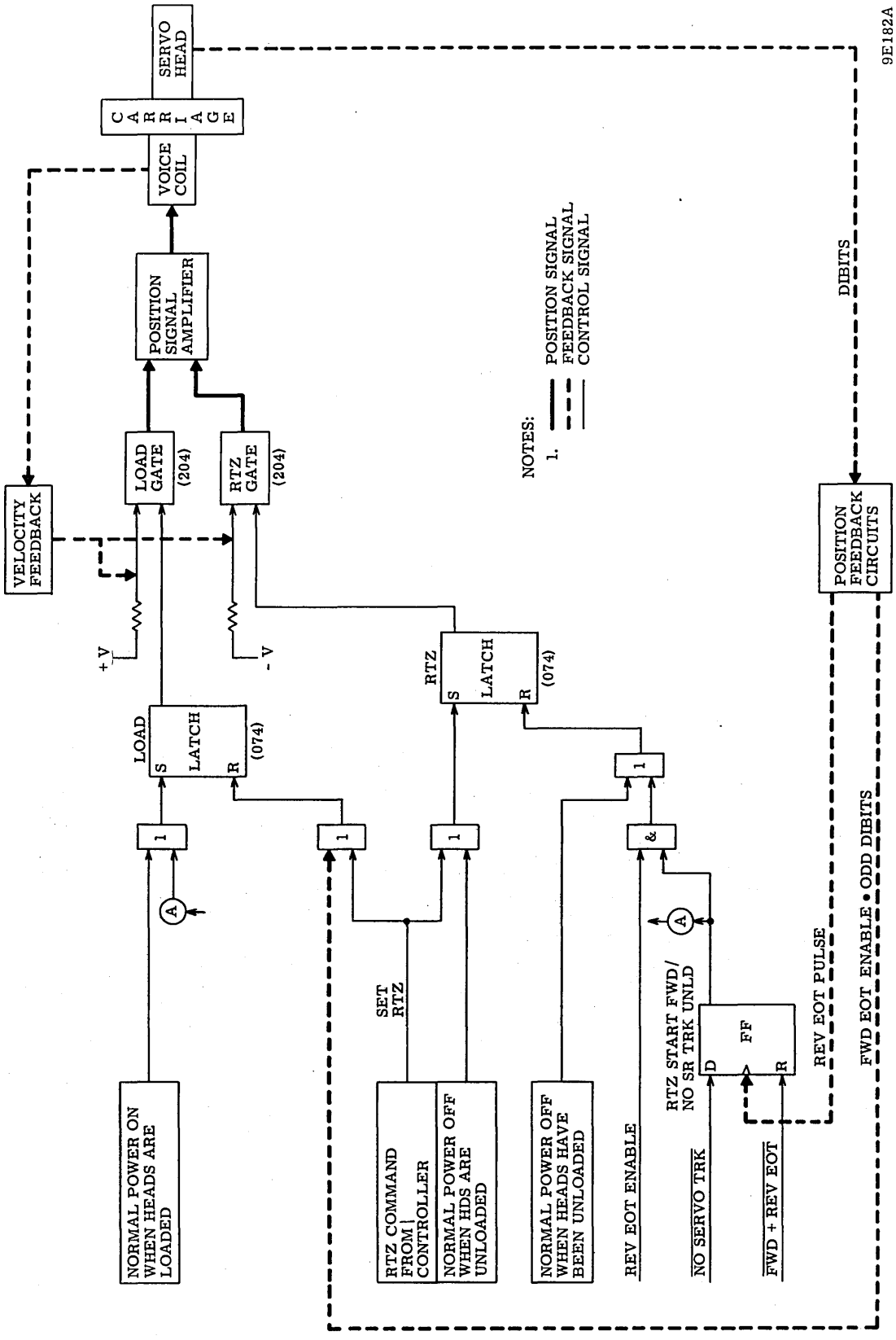


Figure 3-50. RTZ/Load Seek Coarse Position Control Loop

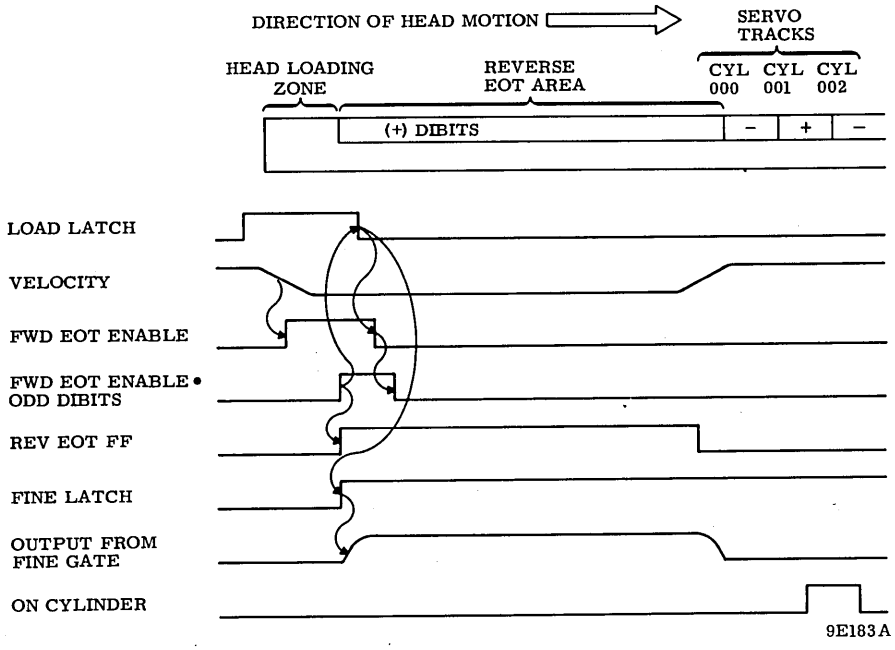


Figure 3-51. Load Seek Timing

When the heads are over the reverse end of travel area, (odd dibits are being detected) the Track Servo signal is at its maximum negative value and the Fine Position Analog signal (derived from it) is at its maximum positive value. This value is such that a constant forward motion is obtained at the proper speed.

When the heads approach cylinder 000, even dibits are detected. This causes the Track Servo signal, and therefore the Fine Position Analog signal to decrease toward zero. The carriage now decelerates until on cylinder is detected. On Cylinder detection and track following for a Load Seek is the same as discussed for direct seeks.

RETURN TO ZERO SEEK POSITION CONTROL

The return to zero seek (RTZS) function is an alternate means for the controller to command the drive to seek to cylinder 000 without issuing a direct seek command. This might be necessary in cases where a seek error has occurred.

The controller initiates a return to zero seek via a tag 010 (Diagnostic) accompanied by Bus Out bit 0 (RTZ). When the drive receives this command, the RTZ latch sets and enables the RTZ gate (refer to figure 3-50). The RTZ gate, like the Load gate, combines a bias signal with the Velocity signal and applies the result to the position signal amplifiers. However, in this case the resultant signal causes the carriage to move in reverse at about seven inches per second.

When the carriage moves past cylinder 000, it enters the reverse end of travel area and no more cylinder pulses are generated. The loss of cylinder pulses allows the EOT Velocity Integrator output (which is normally reset to zero by cylinder pulses) to exceed -1.4 V. This causes the Reverse EOT Enable signal to go true and set the Reverse EOT FF (Refer to discussion on End of Travel Detection). Setting the Reverse EOT FF causes the Velocity Integrator to reset but the carriage continues moving in reverse and the integrator output starts to rise again.

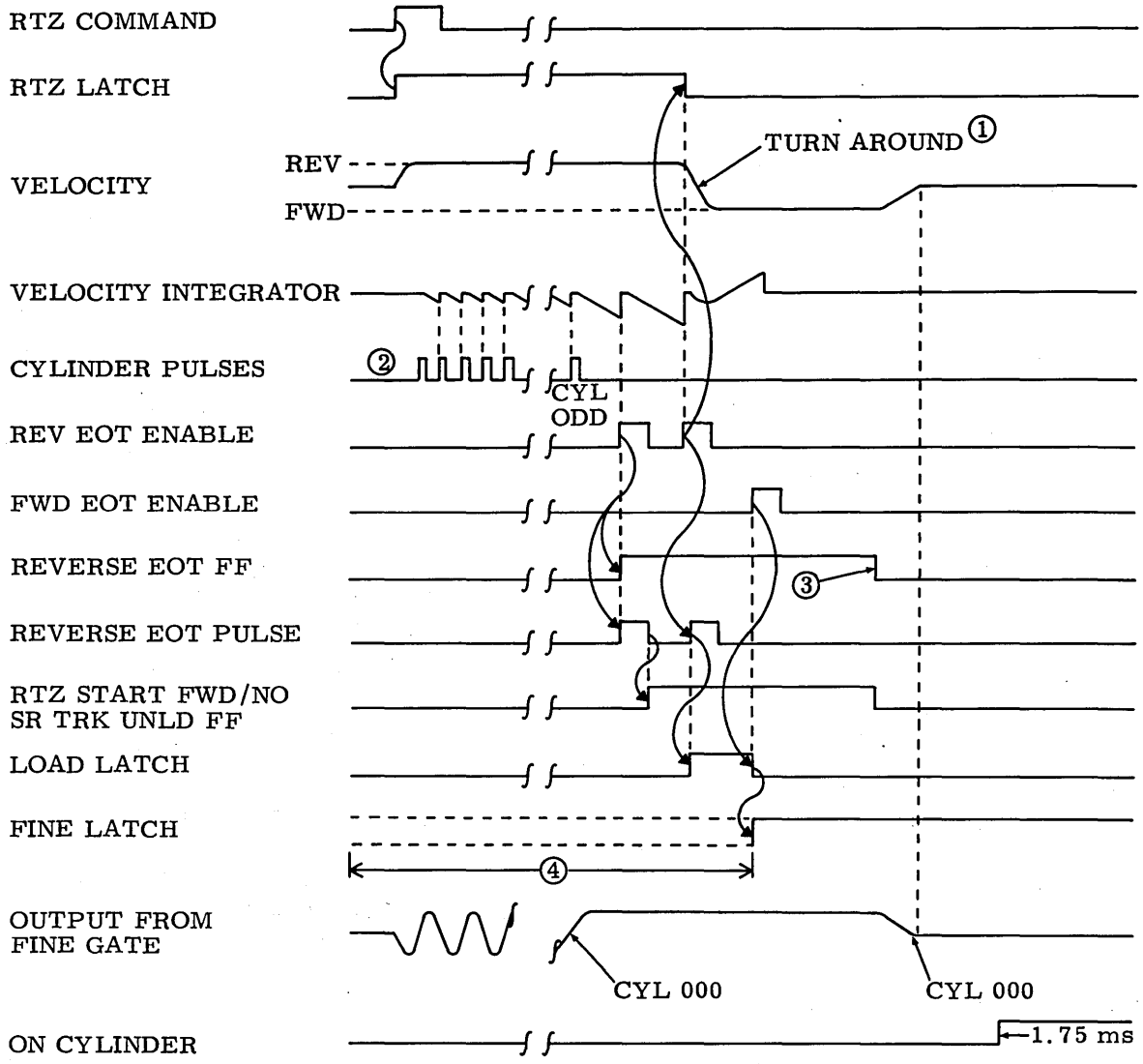
After an additional reverse motion of about two tracks, the Velocity Integrator output again exceeds -1.4 V. This time the Reverse EOT Enable signal enables the Set Load signal which sets the Load latch and clears the RTZ latch.

Setting the Load latch causes the carriage to reverse direction and start back toward cylinder 000. During the remainder of the operation, the drive seeks to cylinder 000 as during a load sequence (refer to discussion on Load Seek Position Control).

Figure 3-52 shows the timing for, and figure 3-53 is a flow chart of, the entire return to zero seek function.

UNLOAD HEADS POSITION CONTROL

The heads are normally unloaded at the start of the power off sequence (refer to discussion on Power System). This is necessary to make certain the heads are not over the disk when it slows down as this would cause head crash. The heads are also unloaded during certain error conditions (refer to discussions on Emergency Retract and Seek End and Seek Error Detection). The following describes the heads unload sequence occurring during a normal power off.



NOTES:

① CLEARING RTZ AND SETTING LOAD LATCH CAUSES CARRIAGE TO REVERSE DIRECTION AND MOVE FWD.

② CYLINDER PULSES RESET VELOCITY INTEGRATOR.

③ REV EOT FF CLEARED WHEN NEGATIVE-EVEN DIBITS ARE DETECTED AS HEADS APPROACH 000.

④ FINE LATCH IS JAMMED (BOTH INPUTS HIGH) THUS DISABLING BOTH COARSE AND FINE GATES AS LONG AS EITHER LOAD OR RTZ LATCH IS SET.

9E184

Figure 3-52. Return to Zero Seek Timing

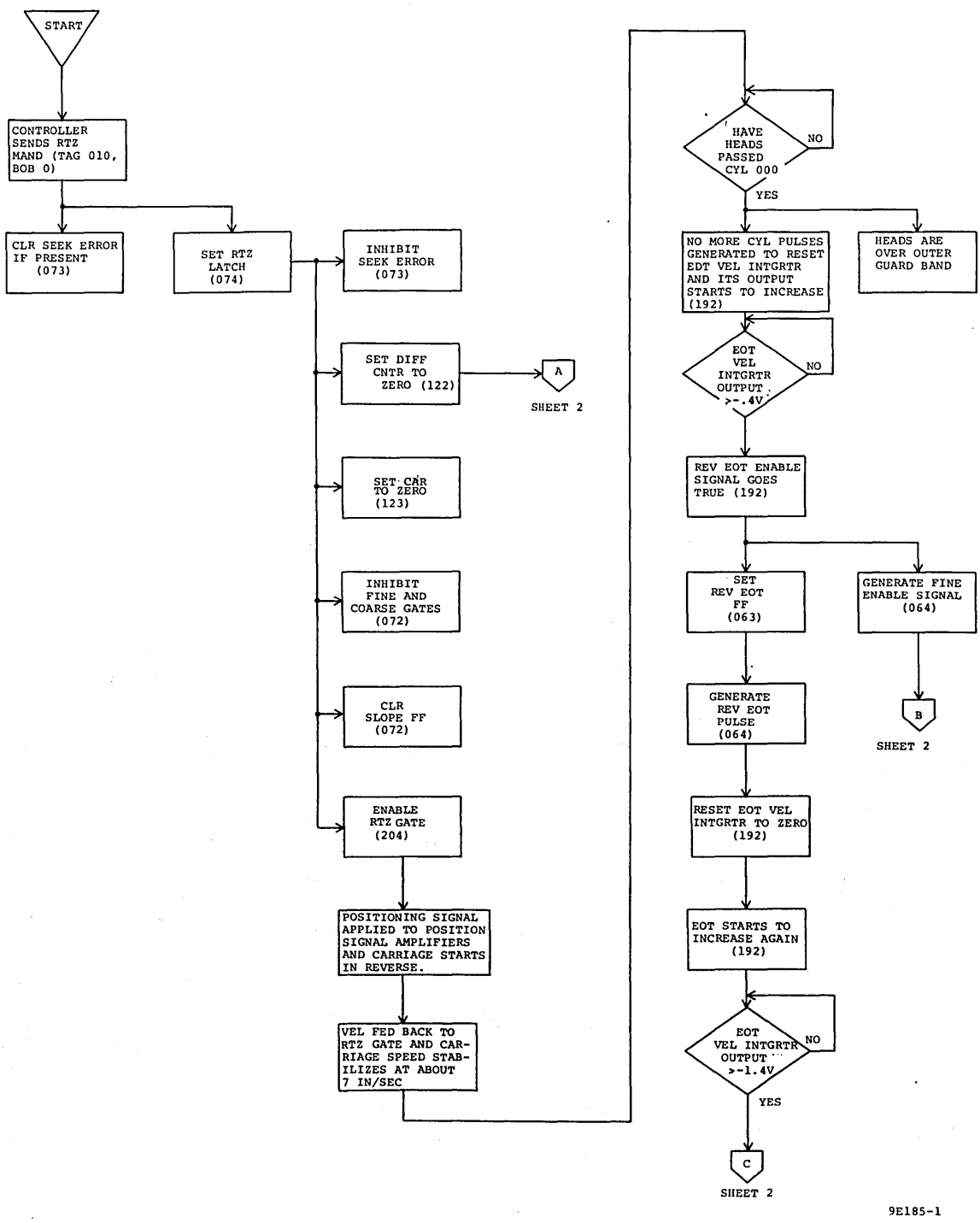


Figure 3-53. Return to Zero Seek Flow Chart (Sheet 1 of 2)

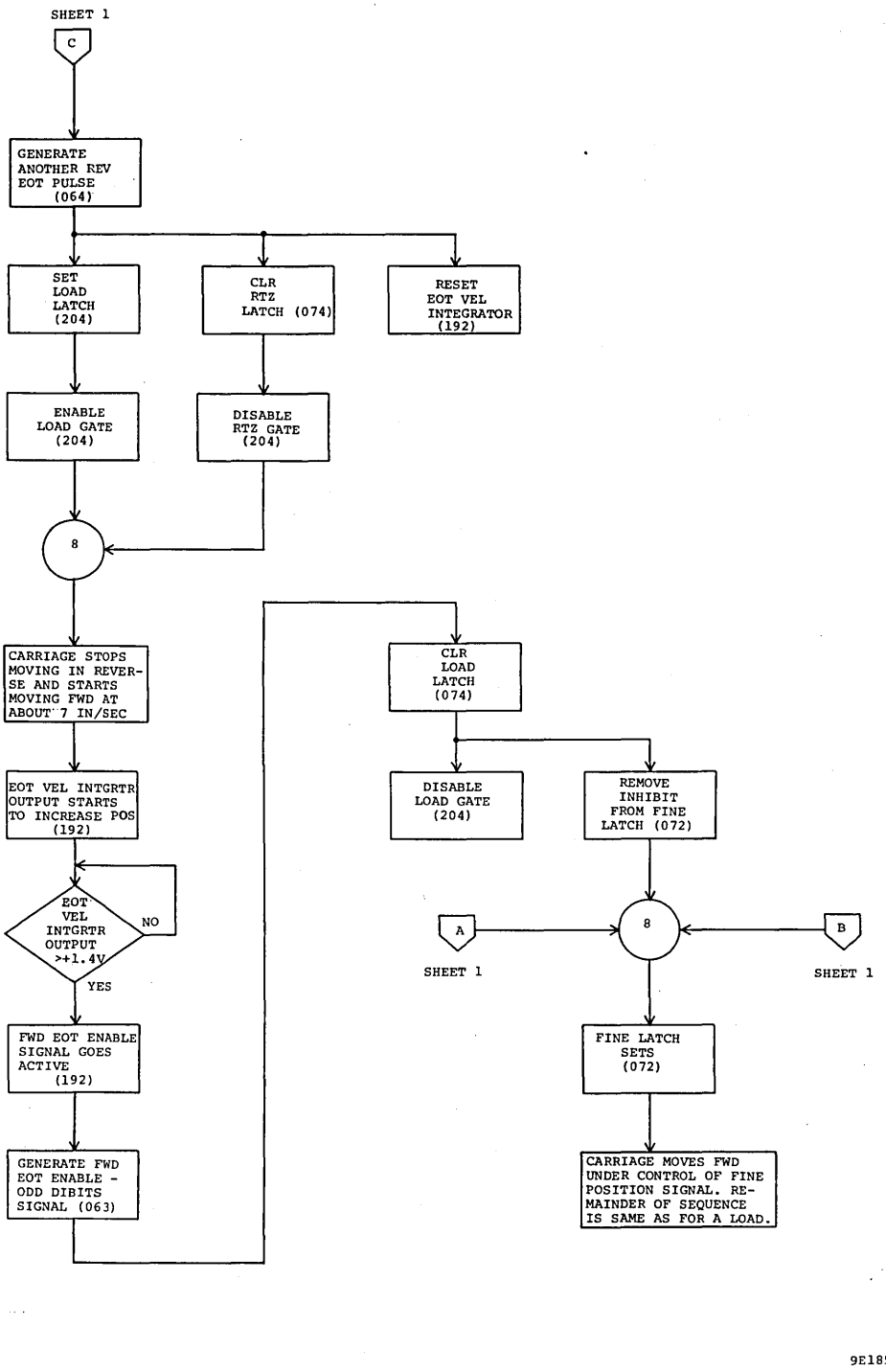


Figure 3-53. Return to Zero Seek (Sheet 2)

The sequence is initiated when the START switch is pressed and the power supply circuits generate signals that set the RTZ latch (refer to discussion on Power System). Setting the RTZ latch enables the RTZ gate and the carriage starts retracting at seven inches per second. The action is similar to an RTZ seek except that the EOT detection circuit is disabled so that the Reverse EOT Enable signal never goes active. Therefore, the RTZ latch remains set and motion continues until the heads unload.

When the heads loaded switch transfers, indicating the heads are unloaded, the RTZ latch is cleared. This disables the current to the voice coil and the carriage stops driving in reverse. However, the power off sequence continues and this is described in the discussions on the Power System.

SEEK END AND ERROR DETECTION

General

The seek End line goes true at the end of every seek operation and indicates that either the seek has been successfully completed and the heads are over the desired logical cylinder or that a seek error has occurred.

Successful completion is indicated when the drives On Cylinder signal is active and the Seek Error latch is not set. An unsuccessful seek is indicated whenever the Seek Error latch is set (either with or without On Cylinder). This occurs if the drive cannot complete the seek or if an error occurs during the seek operation. If the seek error latch is set, the drive cannot perform another seek until the latch is cleared. This is done via an RTZ command (Tag 010, BOB 0).

The controller determines whether the seek was successful or unsuccessful by monitoring the bus in bits returned during either a Low Cylinder command (Tag 110) or Control command (Tag 111). In both cases Bus In Bit 2 indicates On Cylinder and Bus In Bit 7 indicates Check Diagnostic. When On Cylinder is true it indicates the seek was successful and when Check Diagnostic is true it indicates a seek error has occurred.

The conditions interpreted by the drive as seek error are described in the following paragraphs. The basic logic is shown on figure 3-54.

Timeout Error

If the drive does not generate On Cylinder within 500 ms of the start of the seek the Seek Error latch sets.

Setting the Seek Error latch causes the Difference counter to be reset to zero and the Slope FF to be cleared. This in turn causes the drive to seek the nearest even numbered physical cylinder and generate On Cylinder.

Maximum Address Fault

If the controller commands the drive to seek to a logical cylinder address greater than 822 (410 on 150 MB units) the Seek Error latch is set and the drive will not perform the seek.

End of Travel Errors

General

Whenever a direct seek is being performed and the heads are positioned outside of the normal data area, an end of travel condition exists and the Seek Error latch sets.

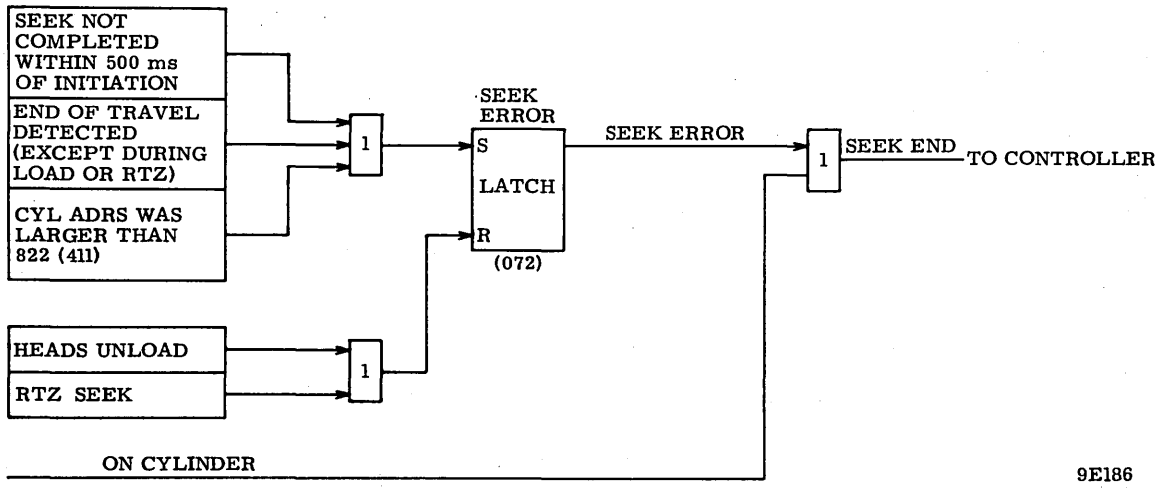


Figure 3-54. Seek End and Seek Error Detection Logic

It is possible for the heads to be positioned over either the forward or reverse end of travel area and both of these sequences are described in the following (also refer to discussion on End of Travel Detection).

Forward End of Travel

When the heads move past physical cylinder 822 they enter the forward end of travel area (inner guard band).

Because cylinder pulses are not generated as the heads move over this area, the EOT Velocity Integrator output is able to exceed +1.35 V (refer to discussion on End of Travel Detection). This causes the Forward EOT Enable signal to go active and set the Forward EOT FF.

This in turn causes the following:

- Seek Error latch sets sending a Seek End to the controller.
- Seek FF (set at start of seek) clears.
- Difference counter set to 000 (T=0).
- Fine Enable signal goes active.
- Slope FF is cleared to indicate a seek to an even numbered cylinder.

When the Fine Enable signal is active and the Difference counter equals zero the Fine latch is enabled thereby enabling the Fine gate.

Because the heads are over the inner guard band and all even dibits are being detected, the Track Servo signal is at its maximum positive value. This results in a Fine Position Analog signal that is at its maximum negative value and the carriage moves in reverse toward physical cylinder 822.

When physical cylinder 822 is approached, odd dibits are detected, the Track Servo and Fine Position Analog signals decrease, and the carriage decelerates until it is on cylinder at physical cylinder 822.

The heads remain at this location until the drive receives an RTZ command.

Reverse End of Travel

A Reverse End of Travel condition indicates the heads have moved in reverse past physical cylinder 000 and into the outer guard band.

When this occurs, the Reverse EOT FF sets and initiates a load sequence that returns the heads to cylinder 000. The heads remain at this location until the drive receives an RTZ command.

MACHINE CLOCK

GENERAL

The machine clock circuits generate the clock signals necessary for drive operation. These circuits are divided into two areas (1) Servo Clock Multiplier and (2) Write Clock Multiplier. These are both explained in the following discussions.

SERVO CLOCK MULTIPLIER

The servo clock multiplier circuits (refer to figure 3-55) generates clock pulses used by the sector detection, Index detection and the Read PLO circuits. It also generates the 9.67 MHz Servo Clock signal that is sent to the controller.

The main element in the servo clock multiplier circuit is the phase lock loop. This loop consists of a phase and frequency detector, error amplifier, voltage controlled oscillator and a divide by 12 circuit. The function of the loop is to adjust itself until its output is identical in phase and frequency to its input.

The input to the loop consists of the dibit signals from the track servo circuit (refer to discussion on Position Feedback Generation). The nominal frequency of these signals is 806 kHz; however, their actual frequency is a function of and varies directly with disk pack speed. This means that the output of the loop will also vary with disk pack speed.

The phase and frequency detection circuit makes the comparison between the input dibits and the output of the loop.

The input dibits are applied via two retriggerable multivibrators. One of these multivibrators provides a 750 ns (approximate) output pulse which is then fed through a pulse forming circuit to provide a 25 ns input pulse for the phase and frequency detector. These pulses vary at the dibit frequency. The other multivibrator has a 1.6 us output which

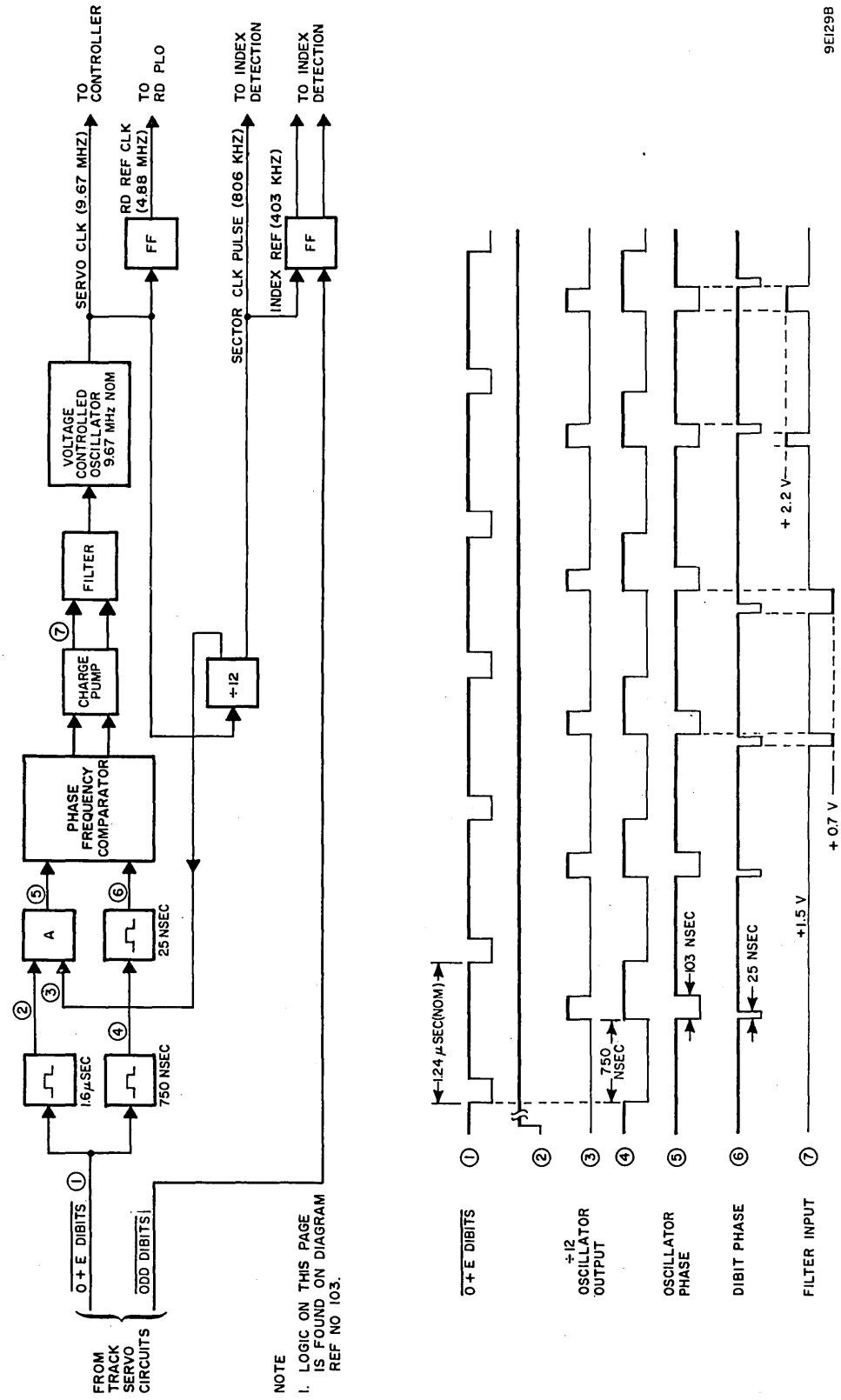


Figure 3-55. Servo Clock Multiplier

is used to enable the feedback pulses from the loop output to the input of the phase and frequency detector. The 1.6 us pulse is longer than the period of the nominal dibit frequency (806 KHz); therefore, the feedback pulses are continuously gated as long as dibits are present. The outputs from the detector are fixed amplitude pulses which are a function of the time (or phase) difference between the positive going edges of the two inputs (refer to figure 3-55).

These outputs are applied to the error amplifier which integrates them and generates a voltage proportional to the phase difference between them. This voltage is used as a control voltage for the Voltage controlled oscillator.

The control voltage causes the VCO frequency to vary in the direction necessary to eliminate the phase or frequency difference between the input and output of the loop. The VCO output is then divided by 12, by the divide by 12 circuit, and fed back to the loop input.

When the VCO output is 9.67 MHz, the feedback provided by the divide by 12 circuit will be 806 KHz and the loop will be synchronized.

Both the 9.67 MHz and 806 KHz signals are divided by two to generate the 4.84 MHz and 403 KHz signals. All four of these frequencies are used by the drive as shown on figure 3-55.

WRITE CLOCK FREQUENCY MULTIPLIER

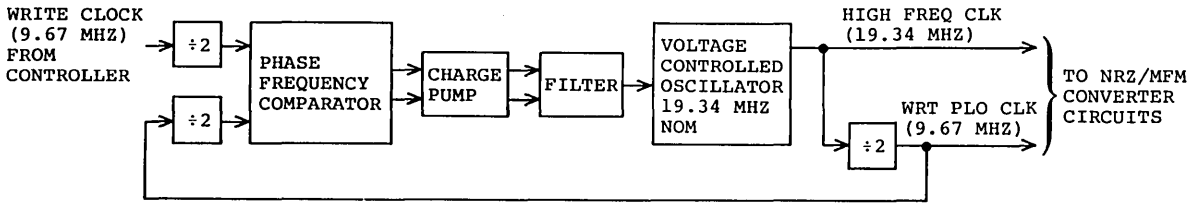
The write clock frequency multipliers circuit (refer to figure 3-56) generates the 19.34 MHz and 9.67 kHz signals used during write operations.

This circuit consists mainly of a phase lock loop and operates essentially the same as the servo clock multiplier. However, the input to the write clock multiplier is the 9.67 MHz Write Clock signals from the controller. The phase lock loop synchronizes to these signals and provides the 19.34 MHz and 9.67 MHz outputs. These outputs are used by the NRZ to MFM converter and Write Compensation circuits during write operations.

HEAD OPERATION AND SELECTION

GENERAL

Information is recorded on and read from the disk by the read/write heads (refer to figure 3-57). The drive has 19 read/



NOTE
1. LOGIC ON THIS PAGE IS FOUND ON DIAGRAM REF. NUMBER 104.

9E130

Figure 3-56. Write Clock Multiplier

write heads, one for each data recording surface in the disk pack. For this reason, before a read or write can be performed, the controller must command the drive to select the head located over the disk surface where the data is to be read written.

The following discusses how the heads read and write the data and also how the desired head is selected.

HEAD FUNCTIONAL DESCRIPTION

Data is written by passing a current through a read/write coil within the selected head. This generates a flux field across the gap in the head (figure 3-58). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a North pole and a South pole. The writing process orients the poles to permanently store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of Write current polarity while its amplitude depends on the amount of current: the greater the current, the more oxide particles that are affected.

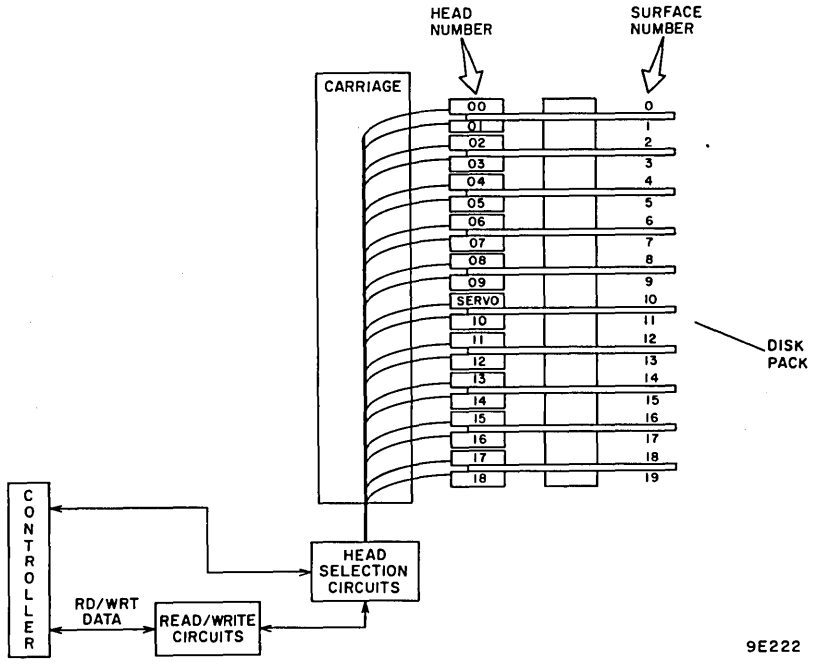


Figure 3-57. Read/Write Heads

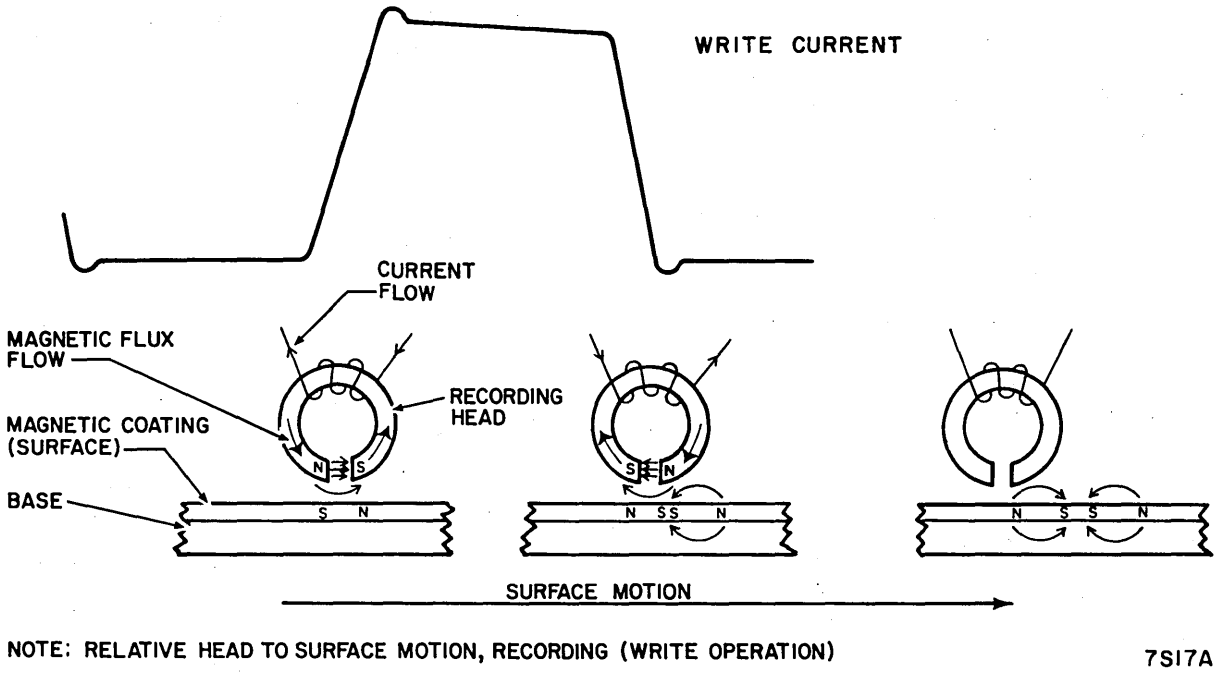


Figure 3-58. Writing Data

Information (data) is written by reversing the current through the head. This change in current polarity switches the direction of the flux field across the gap. The flux change defines a data bit.

Erasing old data is accomplished by writing over any data which may already be on the disk. The write current is zoned in four current zones to ensure proper saturation level for best head resolution (refer to discussion on Write Current Control). The write current is maximum on the outer tracks and progressively decreased for inner tracks.

During a read operation, disk motion beneath the head causes the stored flux to induce a voltage in the head windings (refer to figure 3-59). This voltage is analyzed by the read circuit to define the data recorded on the disk. Each flux reversal (caused by a current polarity change while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

Head Selection

A head must be selected before a read or write operation can be performed. Head selection starts when the controller sends the drive a Head Select tag and a head address. The head address is sent on But Out bits 3 through 7).

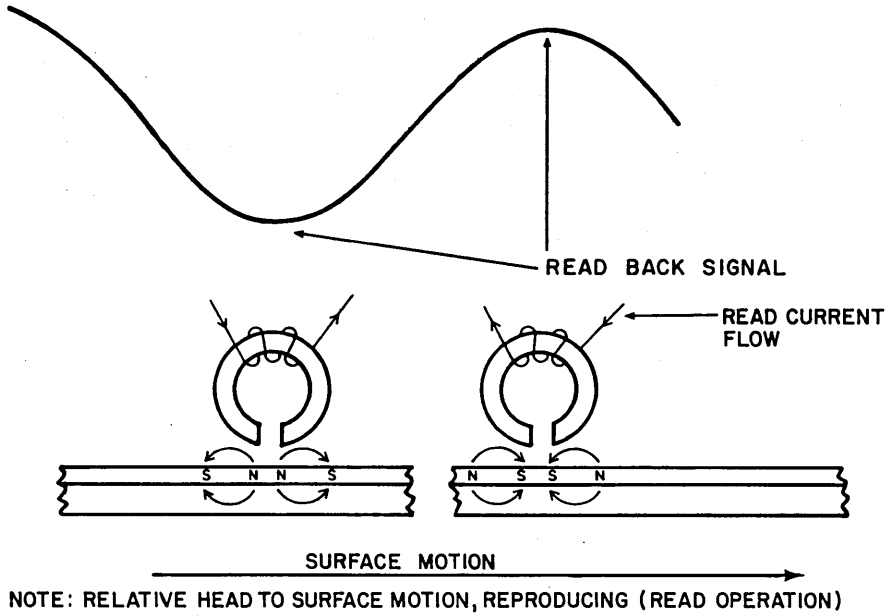


Figure 3-59. Reading Data

The Head Select tag gates the address into the Head Address register. This address is then decoded to a Head Enable signal (0 through 1 depending on Bus Out bits 3 through 7). This signal then enables the head current drive associated with the addressed head and allows the head to conduct as shown on figure 3-60.

If more than one head is selected, a fault is indicated (refer to discussion on Fault and Error Conditions).

TRACK ORIENTATION

GENERAL

After finding the proper cylinder and selecting a head, the controller still may not read or write data until it determines the head is over that part of the data track where the data is to be read or written. The controller accomplishes this by using the Index and Sector signals which are generated by the drive. How the drive generates these signals is explained in the following.

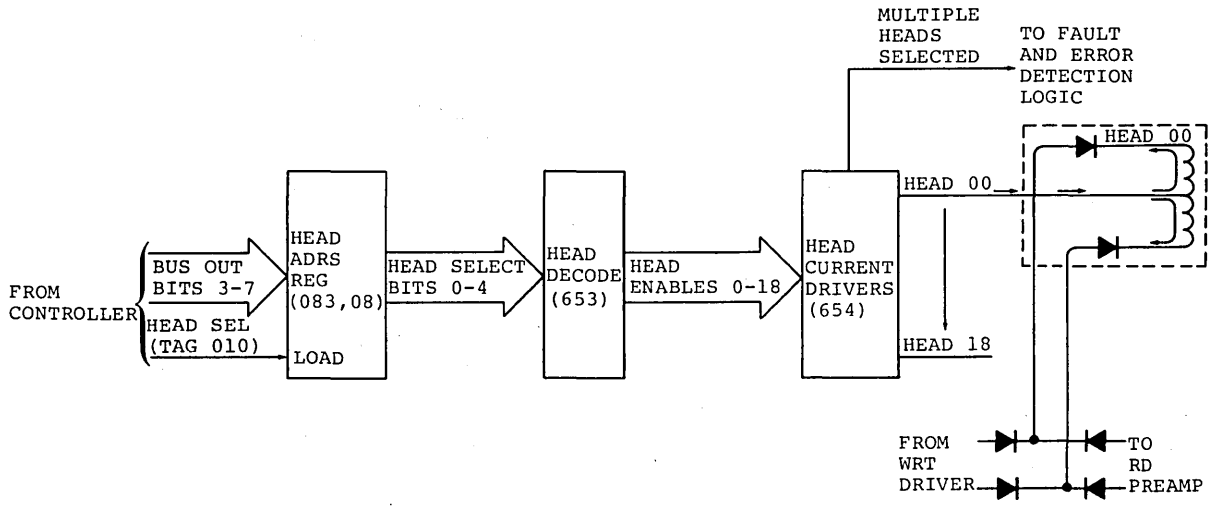


Figure 3-60. Head Select Circuits

INDEX DETECTION

Each track on the servo disk contains a pattern of missing dibits referred to as the Index pattern (refer to discussion on Servo Zone). When the drives Index Detection circuits (refer to figure 3-61) detect this pattern, they generate a 2.5 us Index signal. The Index signal indicates, both to the drive and controller, the logical beginning of a track.

The Odd Or Even Dibits signal provides the data necessary to actually detect the missing dibit pattern. This signal is derived from the dibits detected from the disk and has a nominal frequency of 806 KHz (refer to discussion on Odd/Even Dibits Clock Generation). Because this signal is derived from the dibits, whenever a dibit is missing an Odd Or Even Dibits pulse is also missing.

Detection of missing dibits is done by the Missing Dibits one shot. This one shot is triggered by the Odd Or Even Dibits signals and will not time out as long as dibits are present. However, if two or more consecutive dibits are missed the one shot times out. The output of the Missing Dibits one shot provides the data input for the first stage of the Index Shift register.

The Index Shift register loads the output of the Missing Dibits one shot into its first stage (and also performs its shift) each time a 403 KHz Index Reference Clock pulse occurs. When the one shot is in a triggered state (indicating dibits were present) a one is loaded into the register. However, when the one shot is timed out (indicating two or more dibits were missing) a zero loads into the register.

The contents of the Index shift register are continuously compared to the Index pattern by the Index Decoder and when the shift register contains the pattern indicating Index has occurred, the Index Decoder generates an Index signal. The missing dibit pattern associated with Index and the pattern contained in the shift register when Index has occurred are shown on figure 3-61.

In summary, the Index detection circuit contains three main elements:

- Missing Dibits one shot - Detects the missing dibits in the Index pattern.
- Index Shift register - Accumulates the dibit pattern so that it can be compared with the pattern occurring during Index.

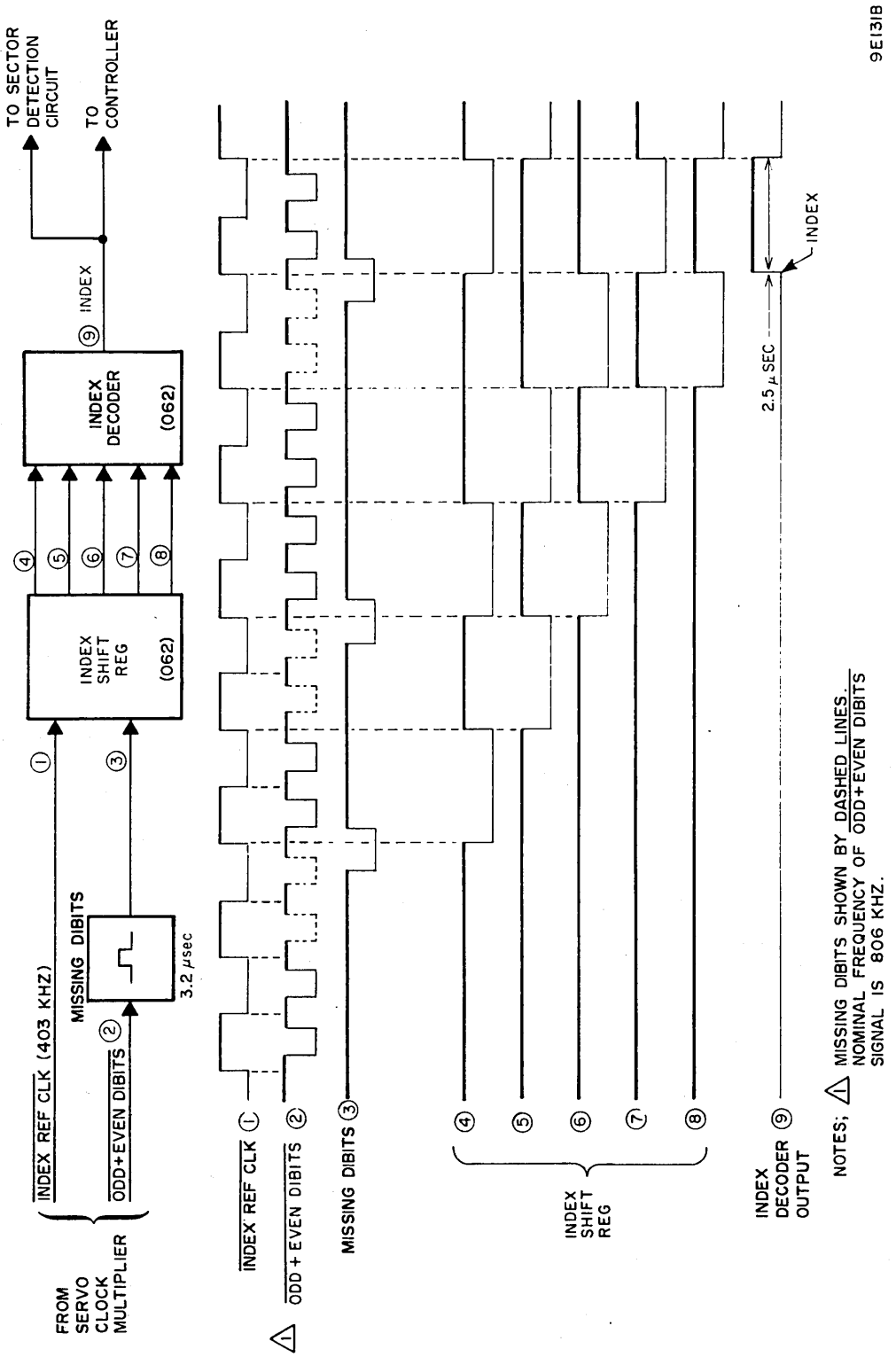


Figure 3-61. Index Detection - Logic and Timing

- Index Decoder - Compares the contents of the Index Shift register with the Index pattern and generates an output signal when Index is detected.

These elements work in conjunction with the two input signals (Odd or Even Dibits and 403 KHz Index Reference Clock) to produce the Index signal. The Index signal is sent to the controller and is also used to reset the drive's sector detection circuitry.

SECTOR DETECTION

General

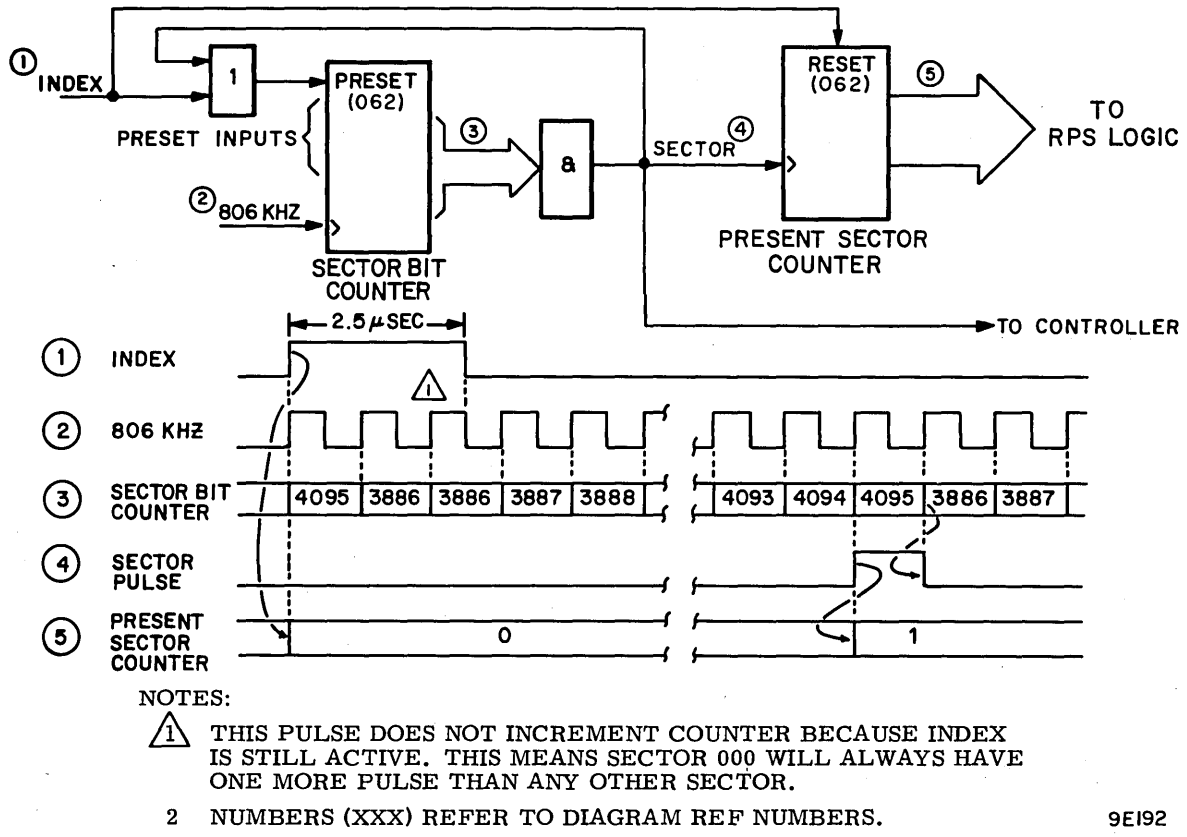
The sector circuits generate signals which are used by the system to determine the angular position of the heads with respect to Index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disk pack. The Sector pulses logically divide the disk into areas called sectors. The following describes how the sector pulses are generated and also describes rotational position sensing (RPS).

Sector Pulse Generation

The Sector pulses are generated by the Sector Bit counter which causes a pulse to be generated each time it indicates its maximum value of 4095 (refer to figure 3-62).

One counter is incremented by the 806 kHz clock pulses. These clock pulses are derived from the servo track dibit signals (refer to discussion on track servo circuit) and exactly 13,440 clock pulses occur during each revolution of the disk pack.

The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution. This done by presetting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors, the counter would have to count 210 clock pulses in each sectors (13,440 divided by 64) and the counter would be preset to 3886. In this case the counter starts at 3886 and increments each clock time until it reaches the maximum count of 4095. Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (210) presets the counter back to 3886 (thus disabling the Sector pulse) and the counter begins the next sector. The 3886 is obtained by subtracting 210 from 4096 which is the total number of clock pulses the counter is capable of counting (0 through 4095 = 4096).



NOTES:

1. THIS PULSE DOES NOT INCREMENT COUNTER BECAUSE INDEX IS STILL ACTIVE. THIS MEANS SECTOR 000 WILL ALWAYS HAVE ONE MORE PULSE THAN ANY OTHER SECTOR.
2. NUMBERS (XXX) REFER TO DIAGRAM REF NUMBERS.

9E192

Figure 3-62. Sector Detection - Logic and Timing

The sector length is varied by changing the value of the preset inputs to the counter. This is done by rewiring the sector plug located on the logic chassis backpanel at position A06. Refer to section 1 of the maintenance manual for details regarding the rewiring of the sector plug.

The Sector pulses are sent to the controller and are also used to increment the Present Sector Counter.

The Present Sector counter counts the Sector pulses (starting at Index) and therefore always indicates the number of the sector the heads are currently over. This count is used by the rotational position sensing circuits.

Rotational Position Sensing (RPS)

The RPS operation consists of the drive raising its Interrupt line to the controller each time it reaches a specific sector. The sector is specified by the controller at the start of the operation. The Interrupt line is raised each time the sector is detected (even if the drive is deselected) unless the RPS is disabled. The purpose of the function is to free the system for other operations while the drive searches for the sector.

RPS is enabled by a Tag 101 (Target Register) with Bus Out bit 0 true. This command causes the drive to set the RPS Enabled latch and enable the contents of Bus Out bit 1 through 7 to the Target mux (refer to figure 3-63). Bus Out bits 1 through 7 contain the number of the target sector at which the drive will raise the Interrupt line.

The Target register is loaded with the target sector at the next Sector or Index pulse following the receipt of the Target Register command (refer to figure 3-64).

As the disk rotates, the Sector pulses continue to increment the present sector count and this count is compared with the contents of the Target register. When the two are equal, the drive has reached the target sector and the Sector Compare signal goes true. This sets the Enable Interrupt FF which, in turn, enables the Interrupt signal to the controller. The Interrupt signal remains active until the end of the target sector. The drive raises the Interrupt line each revolution (even if the drive is deselected) until the RPS is disabled via a Clear RPS command (Tag 010 and Bus Out bit 5).

The RPS circuits are also used to store the number of the sector where a read or write command is received. This function is initiated when the drive receives a Control tag (111) with Bus Out bit 0 true. This causes the drive to load the Target register with the present sector count which remains in the Target register until a Control tag (with Bus Out bit 0 true) loads another number into it. The controller can retrieve the sector number via a Target Register tag with Bus Out bit 0 false.

READ/WRITE FUNCTIONS

GENERAL

When the drive is on cylinder, has a head selected, and has located the proper place on the data track, it is ready to perform a read or write operation. The controller initiates a read or write operation by sending the drive a Control tag (111) and the proper Bus Out bits (refer to discussion on Interface functions).

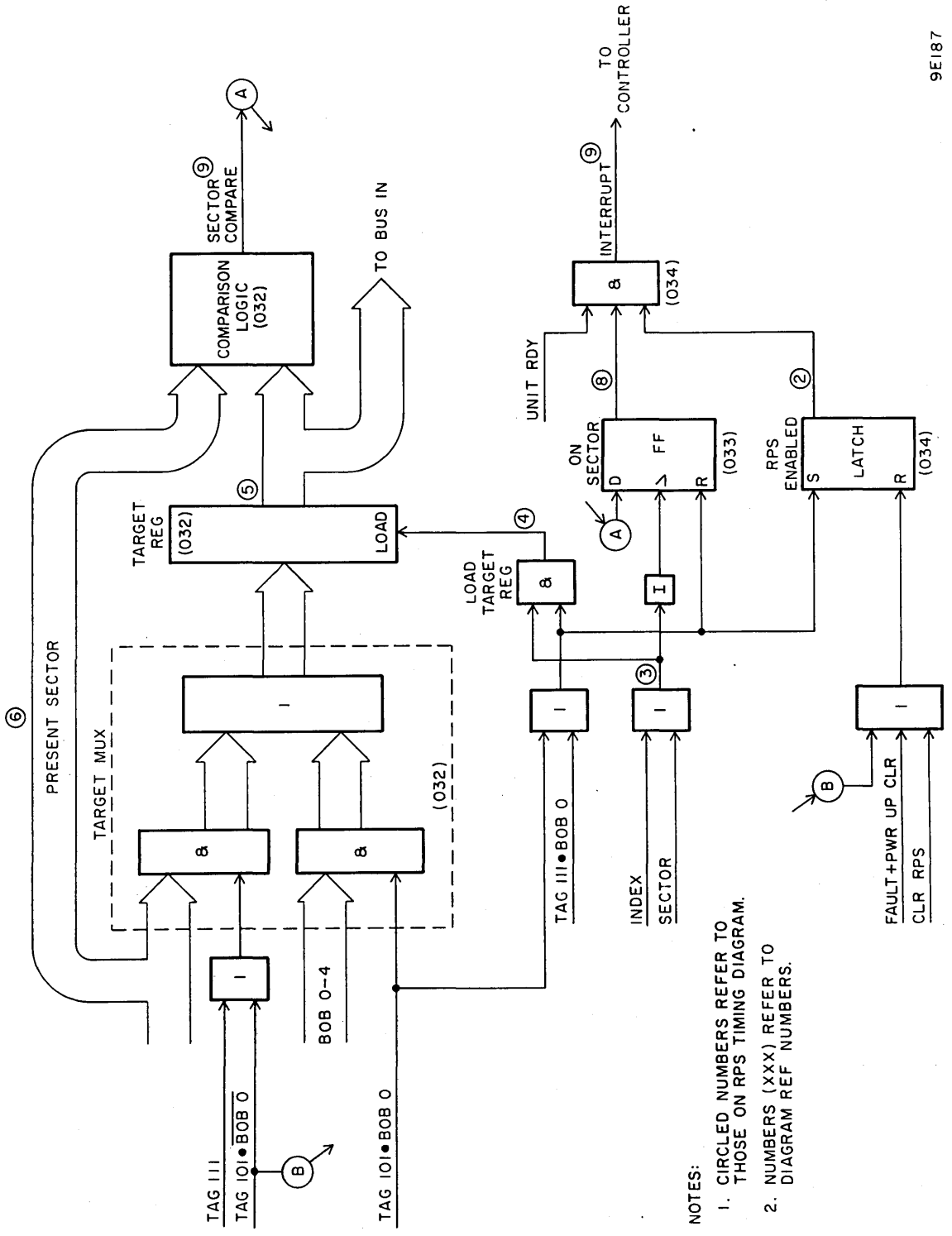


Figure 3-63. Rotational Position Sensing Logic

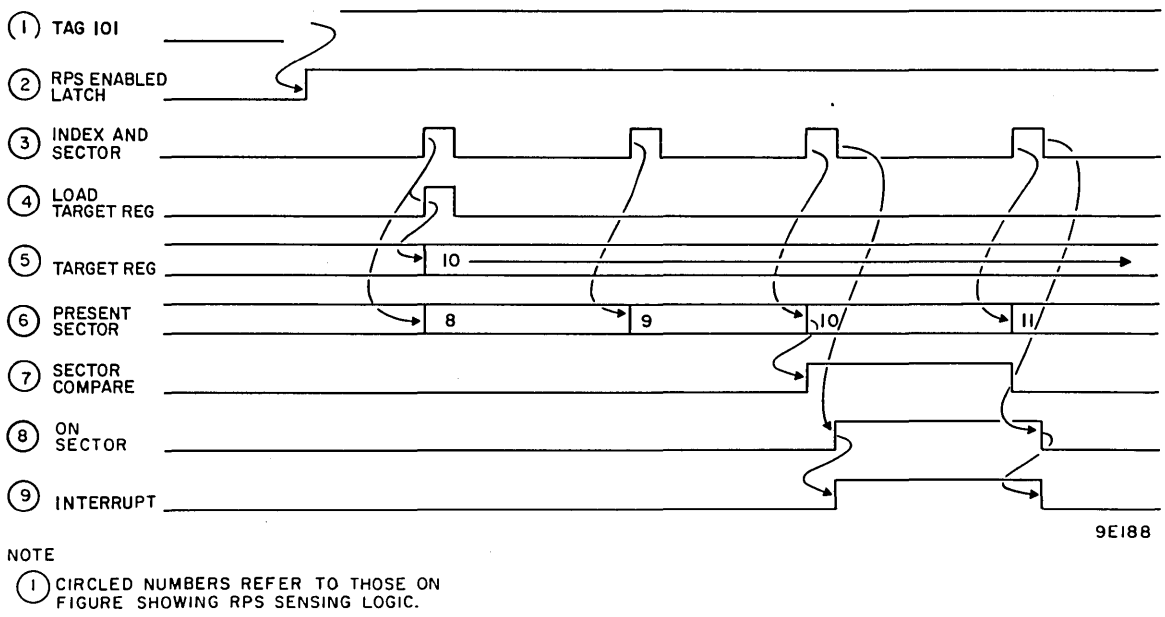


Figure 3-64. Rotational Position Sensing Timing

During a read operation, the drive recovers data from the disk and transfers it to the controller. During a write operation, the drive receives data from the controller and records it on the disk.

Figure 3-65 is a block diagram of the read/write circuits. The remainder of this discussion describes the read/write circuits and is divided into the following areas.

WRITE OPERATIONS

General

The Write circuits operation is initiated by a Control tag (3) with Bus bit 0 true. This allows the drive to start processing serial NRZ data received from the controller. The write data is received via the bidirectional Read/Write data line and is first sent to the NRZ to MFM converter/write compensation circuits. These circuits convert the data to MFM and also compensate it for problems caused by variations in data frequency. The compensated data is then processed by the write drive circuits and written on the disk.

Figure 3-66 shows the write circuits and table 3-5 briefly explains their function.

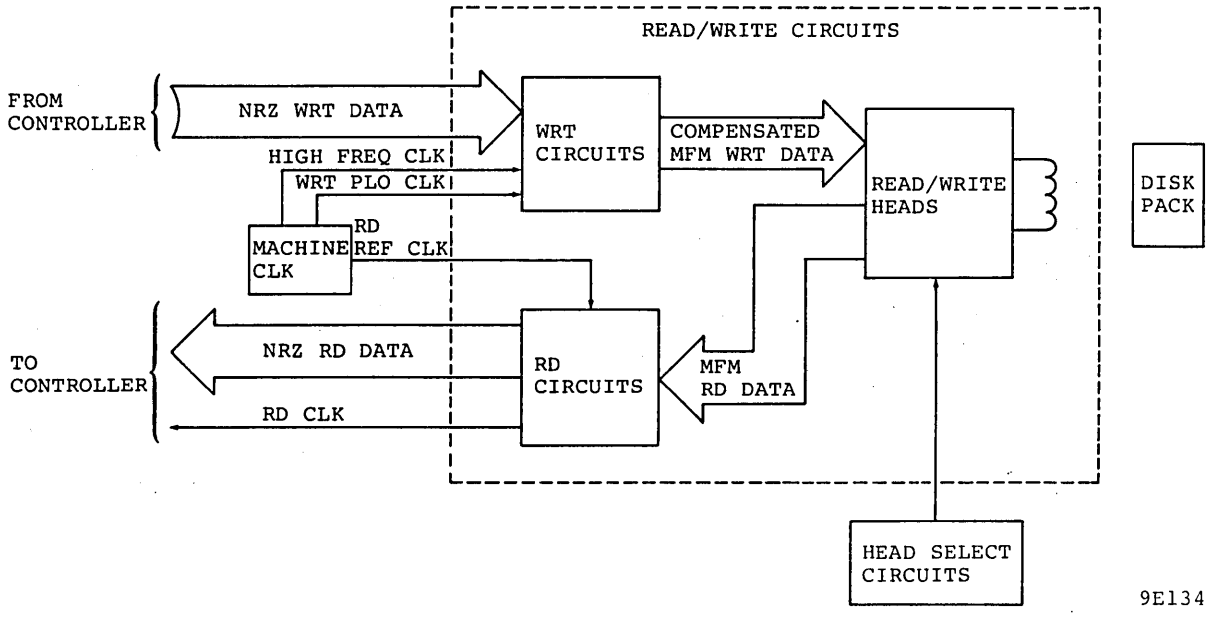


Figure 3-65. Read/Write Circuits Block Diagram

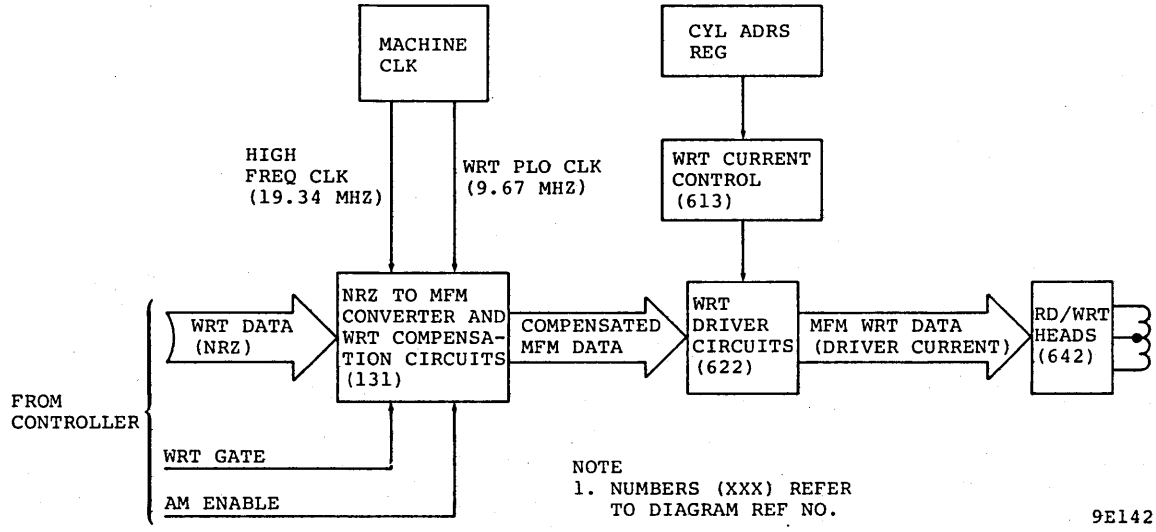


Figure 3-66. Write Circuits Block Diagram

TABLE 3-5. WRITE CIRCUIT FUNCTIONS

Circuit	Function
NRZ to MFM Converter and Write Compensation Circuits	Converts the NRZ data from the controller to MFM data and also compensates the data for problems caused by variations in the write data frequency.
Write Driver Circuits	Uses the MFM data to produce the current necessary to record data on the disk.
Write Current Control	Reduces the write current amplitude as the heads move from the outer tracks to inner tracks. This assures that the correct amount of current will be used as the circumference of the cylinders decrease.

The following paragraphs describe MFM recording, which is the technique used for recording data on the disk, and also explains how the drive circuits function during a read or write operation.

Principles of MFM Recording

In order to define the binary dibits stored on the pack, the frequency of the flux reversals must be carefully controlled. Several recording methods are available; each has its advantages and disadvantages. This unit uses the Modified Frequency Modulation (MFM) technique.

The length of time required to define one bit of information is the cell. Each cell is nominally 103 nsec in width. The data transfer rate is, therefore, nominally 9.677 MHz.

MFM defines a "1" by writing a pulse at the half-cell time (figure 3-67). A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is Clock; however, Clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell.

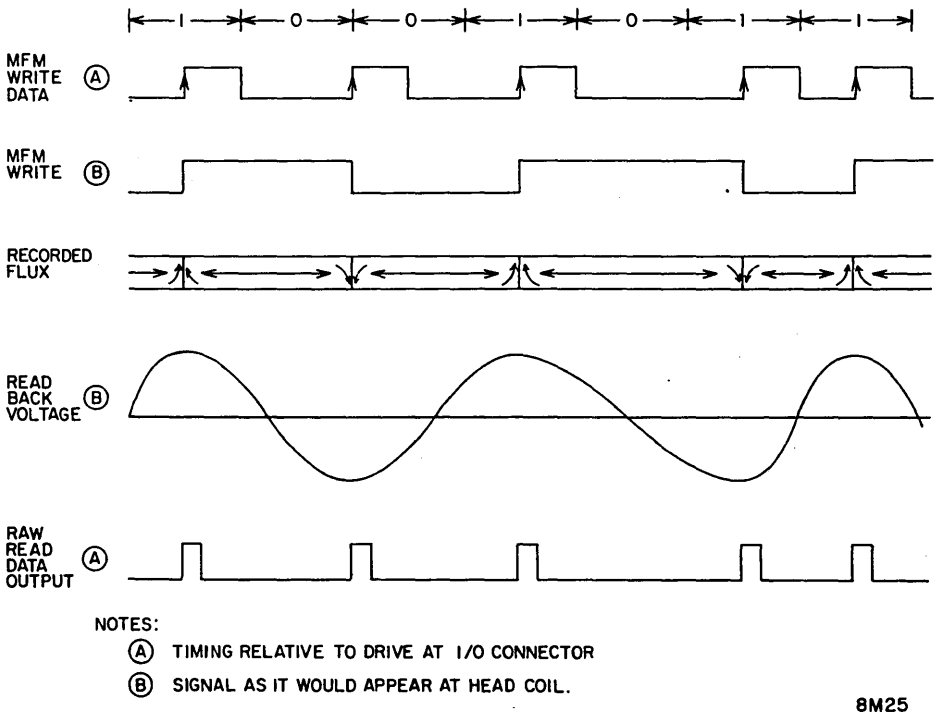


Figure 3-67. MFM Recording - Waveforms and Timing

The rules for MFM recording may be summarized as follows:

- There is a flux transition for each "1" bit at the time of the "1".
- There is a flux transition between each pair of "0" bits.
- There is no flux transition between the bits of a "10", "11" or "01" combination.

NRZ to MFM Converter/Write Compensation Circuits

The NRZ to MFM Converter/Write Compensation circuits convert the NRZ data into MFM data and also shift the output MFM pulses to compensate for problems caused by variations in data frequency. Figures 3-68 and 3-69 show simplified logic and timing for these circuits.

The 9.67 MHz and 19.34 MHz signals from the servo frequency multiplier circuit provide basic timing signals for these circuits. The NRZ data from the controller provides the data input.

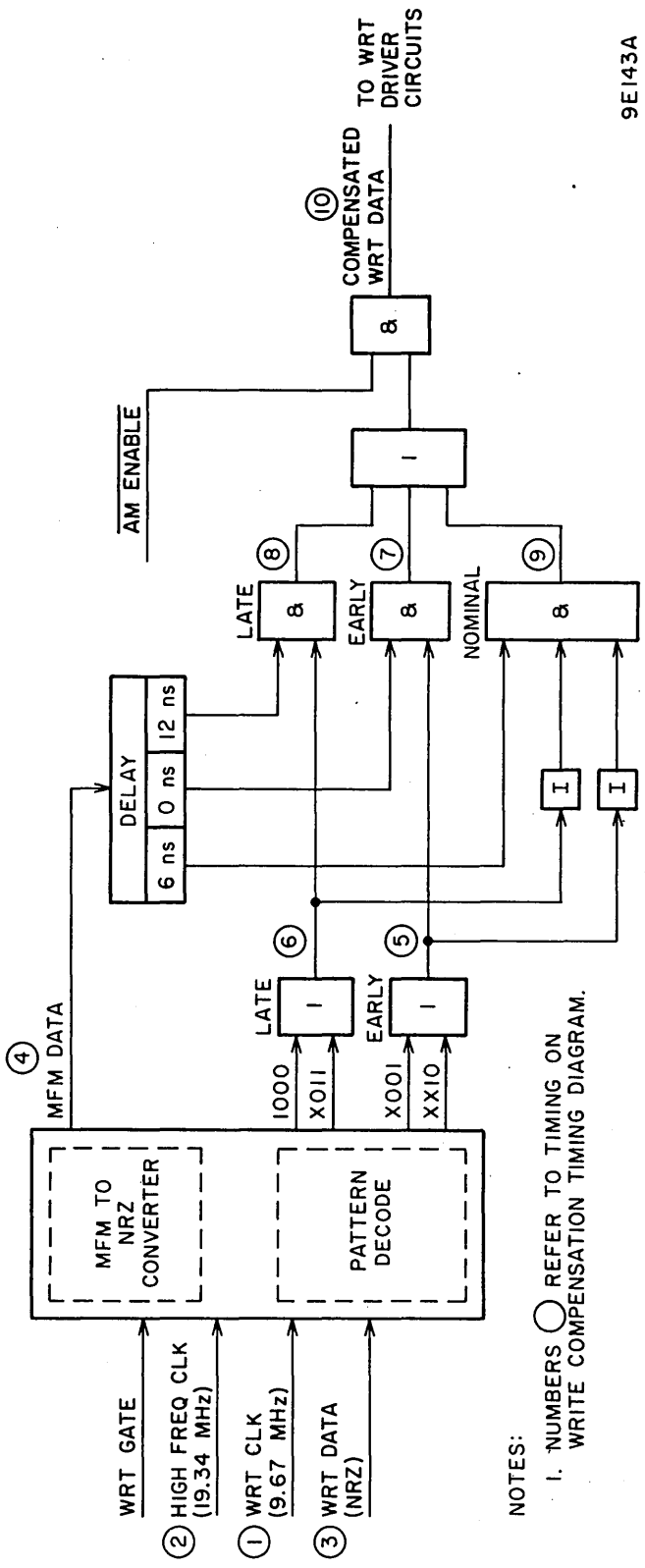


Figure 3-68. Write Compensation NRZ to MFM Converter Circuits

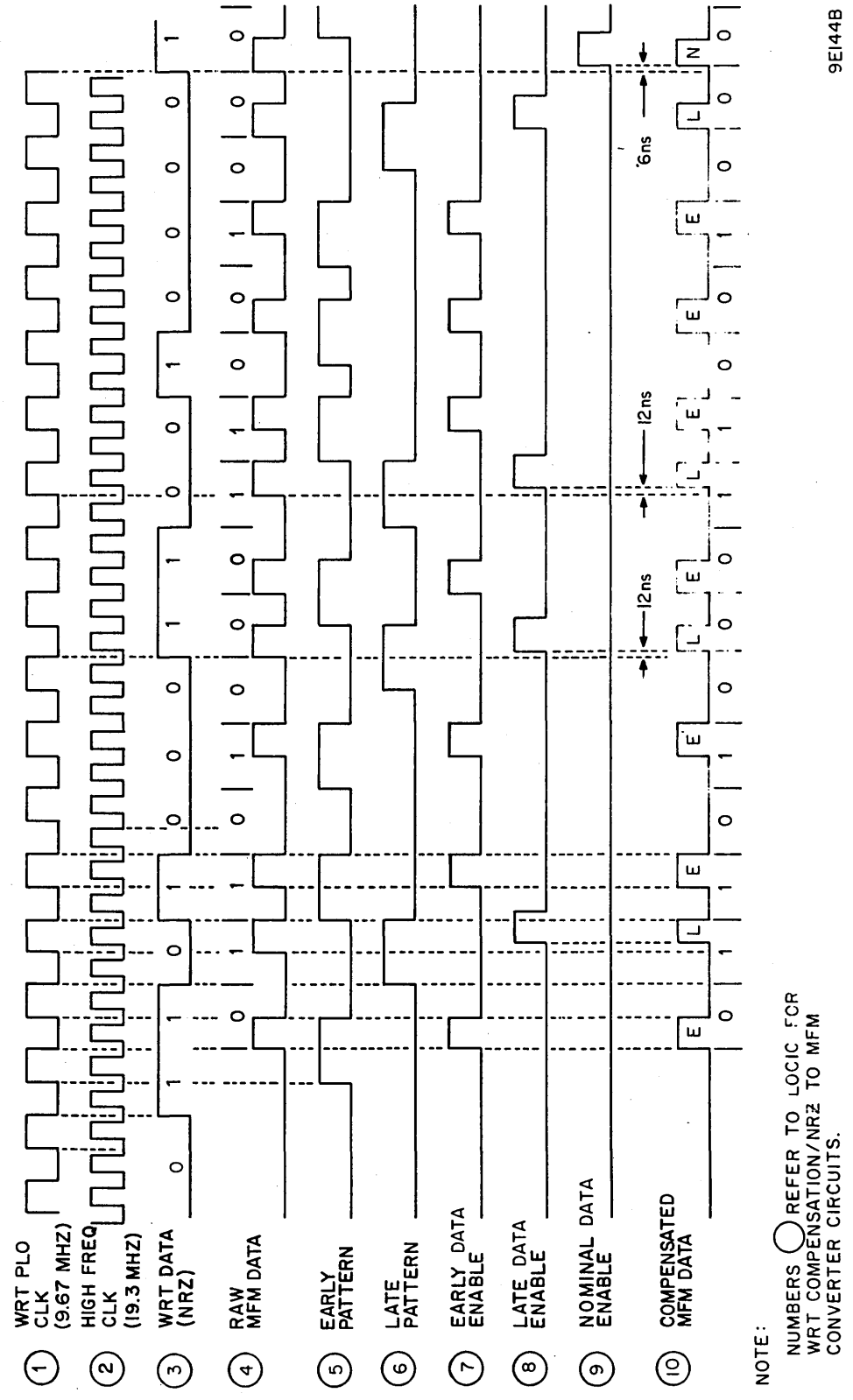


Figure 3-69. Write Compensation Timing

The NRZ to MFM converter converts the NRZ data into MFM data applies it to a delay line in the write compensation circuits. This delay line has three outputs which are combined with the outputs of the pattern decode logic (at the Early, Late, and Nominal gates) to produce compensated write data.

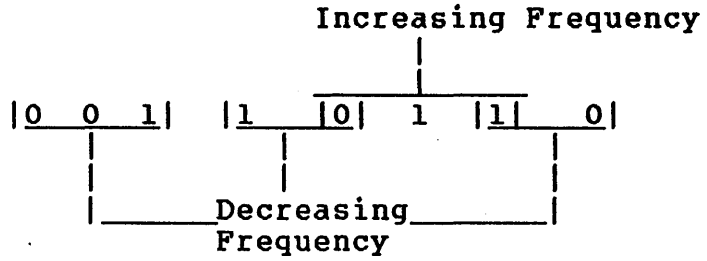
The pattern decode logic analyzes the NRZ data and determines if its frequency is constant, increasing or decreasing. This is necessary because if the frequency is increasing or decreasing, problems can occur during subsequent read operations. These problems are eliminated by compensating the data before writing it on the disk.

The data frequency is constant whenever all ones or all zeros are being recorded because all pulses are separated by one cell (103 ns). However, a 011 pattern represents a frequency increase since there is a delay of about 1.5 cell between the 01 and only 1.0 cell between the 11. On the other hand a 10 pattern represents a frequency decrease since a pulse is not written at all in the second cell. A 001 pattern is also a frequency decrease since there is a 1.0 cell interval between the first two bits and 1.5 cell between the last two.

The previous examples examined only two or three bits without regard to the preceding or subsequent data pattern. The actual combinations are somewhat more complex. The drive logic examines and defines the following patterns:

Pattern	Frequency Change
011	Increasing
1000	Increasing
10	Decreasing
001	Decreasing

Any data pattern will have considerable overlapping of the data pattern frequency changes. Consider the overlap of these eight bits:



The outputs from the pattern decode logic enable either the Early, Late or Nominal gate (depending on the input frequency) to provide compensated Write data as follows:

- If frequency is constant, there will be no peak shift. In this case the data is defined as nominal and is delayed 6 nsec.

- If frequency is decreasing, the apparent readback peak would occur later than nominal. To compensate for this, the data is not delayed and is therefore 6 nsec earlier than the nominal data.

- If frequency is increasing, the apparent readback peak would occur earlier than nominal. Therefore, this data is delayed 12 nsec which is 6 nsec later than nominal.

After being write compensated the data is transmitted to the write driver circuits.

Write Driver Circuit

The compensated write data is sent to the read/write chassis and applied to a differential receiver in the write driver circuits (refer to figure 3-70). The output of the receiver then serves as a clock for the Write Toggle FF. This flip flop toggles only when the Write Enable signal is active. The output of this flip flop provide the input to the Write Driver which in turn generates the current for the read/write heads. The magnitude of the current applied to the heads is controlled by the write current control circuits.

Write Current Control

The magnitude of the write current sent to the heads is controlled as a function of cylinder address. This is referred to as write current zoning as the zones are divided into the following segments of tracks: 0-127, 128-255, 256-383, 384-511, 512-639, 640-767, and 768-822. Write current is reduced at each zone boundary from outer to inner tracks.

Writing Address Marks

The Address Mark is an area that contains neither MFM "1's" or "0's". The drive starts writing an Address Mark when it receives Tag 111 and Bus Out bits 1 and 4 from the controller.

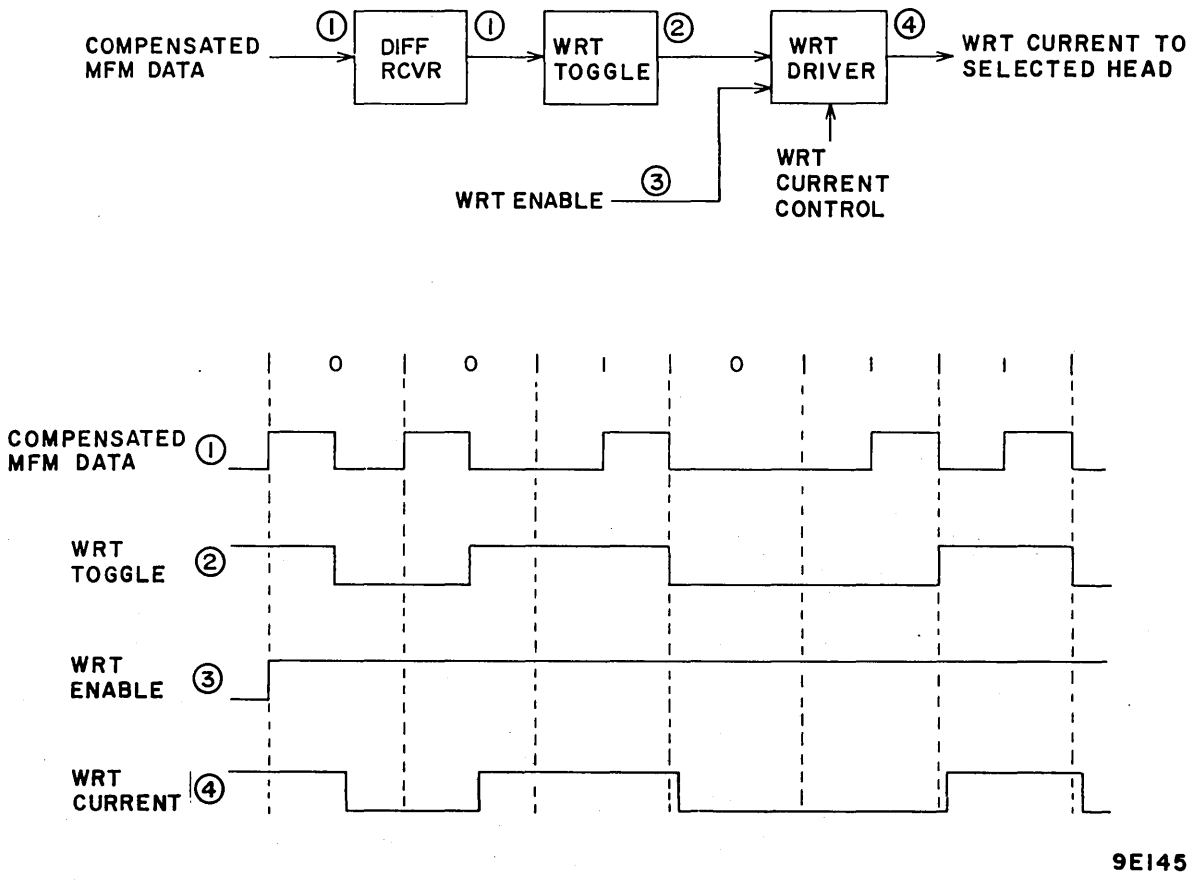


Figure 3-70. Write Driver Circuits and Timing

This activates the Address Mark Enable signal which prevents compensated write data from going to the write driver circuits. The Write Driver continues to generate current for the write coil but without data no current reversals occur. The effect is to erase all information from the disk. The drive stops writing the Address Mark when the controller drops Tag 111 or Bus Out bits 1 or 4.

General

Write data protection consists of disabling the write data circuit whenever there is a danger of writing faulty data on the disk pack. It is initiated if the drive detects the Write Protect signal active, Fault latch set, or a low voltage condition. All of these are described in the following.

Write Protect

The Write Protect signal goes active if any of the following occurs.

- Controller commands a write while the heads are in an offset position (refer to discussion on Direct Seek Fine Position Control-Track Following).
- WRITE PROTECT switch on drive operator panel has been depressed to light the indicator. In this case, depressing the switch to extinguish the indicator causes the Write Protect signal to go inactive.
- Head alignment is being performed.
- Low dc voltage condition is detected or the disk pack speed slows down below 2700 r/min. Both of these conditions will also cause an emergency retract of the heads (refer to discussion on Emergency Retract).

Fault

The Fault latch sets as a result of a number of drive malfunctions. The conditions causing the Fault latch to set are described in the discussion on Fault and Error Conditions.

Loss of Voltage

If power is lost or drops below a certain level, an emergency retract is performed. However, in this case it is possible that the other signals used to disable the write driver (Write Protect and Fault) will not function properly and the drive will continue to write while the heads are being retracted. This could alter or destroy data already on the pack. The loss of voltage protection circuit consists of a capacitive discharge network that ensures the write circuits are disabled until the heads are unloaded.

READ OPERATIONS

General

Read operations are initiated by a Control tag (111) with Bus Out bit 3 true. This enables the analog data detection circuits, which sense the data written on the disk and generate analog read data signals.

The analog data goes to the read analog to digital converter which changes it into digital MFM data.

In units with the Read PLO/Data Separator option, the read PLO and data separator change the MFM data to NRZ and also generate a 9.67 MHz Read Clock signal. Both data and clock are then sent to the controller. In units without this option, the digital MFM data is sent directly to the controller.

The read circuits also detect the Address Mark area and send an Address Mark Found signal to the controller.

Figure 3-71 shows the main elements in the read circuits and table 3-6 briefly describes each of these elements. The following paragraphs further describe the read circuits.

TABLE 3-6. READ CIRCUIT FUNCTIONS

Circuit	Function
Analog Read Data Detection Circuits	Processes the analog signals sensed by the read/write heads to that they can be used by the digital to analog converter.
Digital To Analog Converter	Changes the analog MFM data into digital MFM data. This data is sent to the read PLO and data separator.
Read PLO and Data Separator	This circuit converts the MFM data to NRZ and also generates a 9.67 MHz Read Clock signal. It transmits both of these to the controller.
Address Mark Detection	Detects the Address Mark and transmits an Address Mark Found signal to the controller.

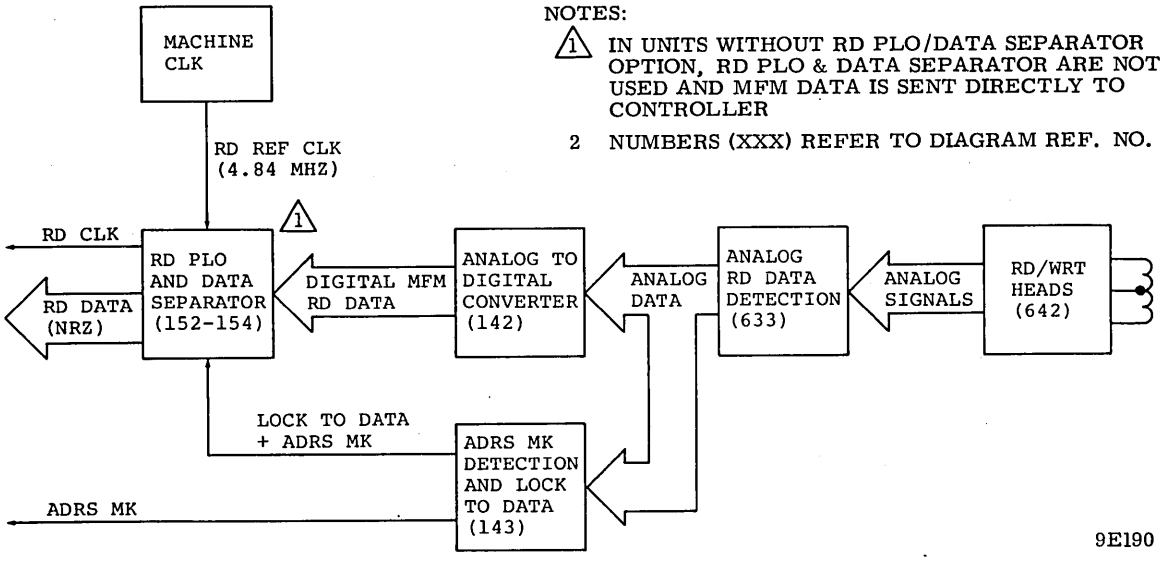


Figure 3-71. Read Circuits Block Diagram

Analog Read Data Detection Circuits

The analog read data detection circuits (refer to figure 3-72) processes the analog MFM data detected from the disk so it can be used by the analog to digital converter circuits.

The Read Pre-amplifier provides preliminary amplification of the analog voltage induced in the real coil. This voltage is induced by the coil by the magnetic flux stored in the disk oxide during write operations (refer to discussion on Basic Read/Write Principles). The frequency of the analog voltage is proportional to the frequency of the magnetic field flux transitions sensed by the read coil.

The low pass filter on the output of the Read Pre-amplifier attenuates the high frequency noise on the read data signals and provides a linear phase response over the range of read data frequencies. The output of the filer is applied to the AGC amplifier. This circuit generates an output signal amplitude that remains within certain limits regardless of the amplitude of the input signal. The AGC Gain Control circuit provides the control voltage for the AGC amplifier and also provides inputs to the Address Mark detection circuits.

The Buffer amplifier processes the AGC amplifier output to provide the proper input for the analog to digital circuit.

Read Analog To Digital Converter

The read analog to digital converter circuit consists of high and low resolution channels and the Data Latch FF. The high and low resolution channels detect the analog data by means of zero cross detectors consisting of Schmidt triggers. The zero cross detectors convert the analog data to digital pulses which are then applied to the Data Latch FF. The FF uses the outputs of both channels to produce a digital MFM data output. The low resolution channel provides the D input to the FF and the high resolution channel provides the clock. This produces an output from the Data Latch FF which retains the timing of the high resolution channel.

Both channels are necessary because of certain high frequency components present in the analog read data signals. These components can cause extraneous zero crossings which are detected by the zero cross detectors. However, the low pass filter in the low resolution channel attenuates the high frequency components thus eliminating any possible extraneous outputs from the channels zero crossing detector.

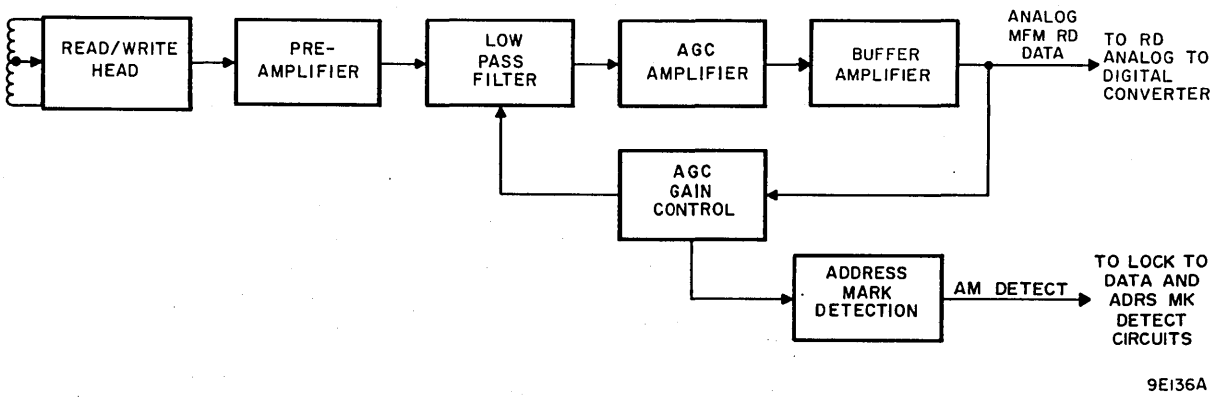


Figure 3-72. Analog Read Data Detection Circuits

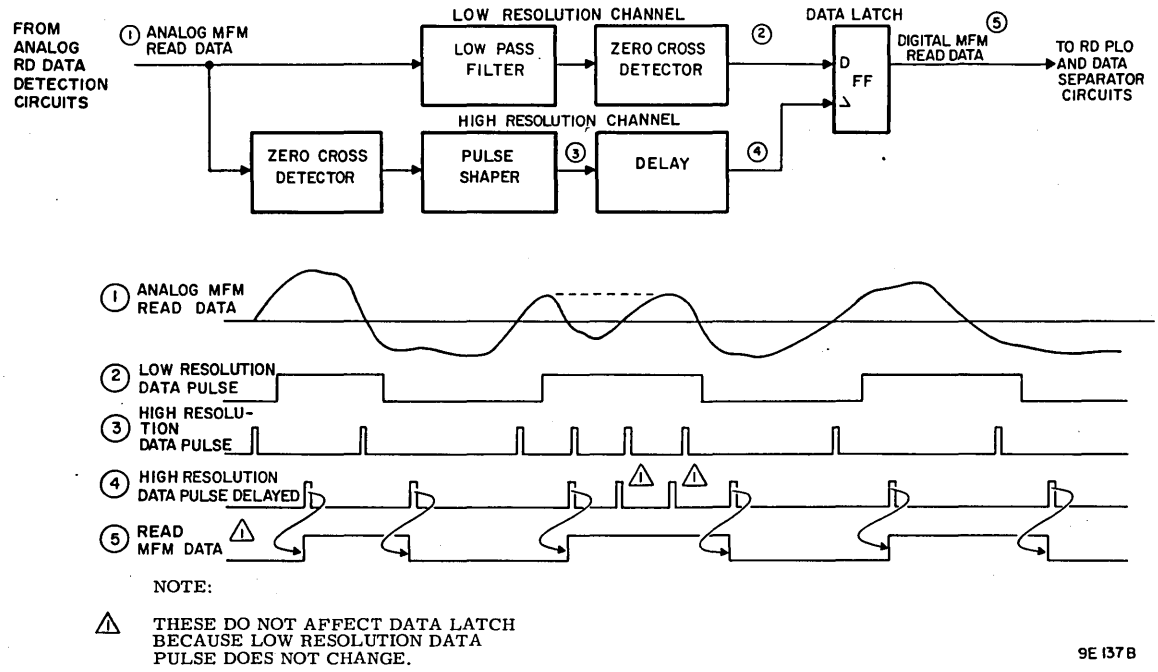


Figure 3-73. Read Analog To Digital Converter Logic and Timing

The high resolution channel still detects the crossings and generates clock inputes to the FF, but without the D input provided by the low resolution channel the extraneous clock pulses are ignored.

If the drive has the Read PLO/Data Separator option, the digital MFM read data is sent to the PLO and data separator which use it to generate the NRZ data and Read clock. However, if the drive does not have this option the data is sent directly to the controller.

Lock To Data And Address Mark Detection Circuits

These circuits generate (refer to figure 3-74) the Lock to Data signal and also detect the Addresses Mark area. The Lock to Data signal is used to synchronize the read PLO and data separator circuits on these units with this option (other units do not use the signal). Finding the address mark area sets Bus In bit 0 to the controller.

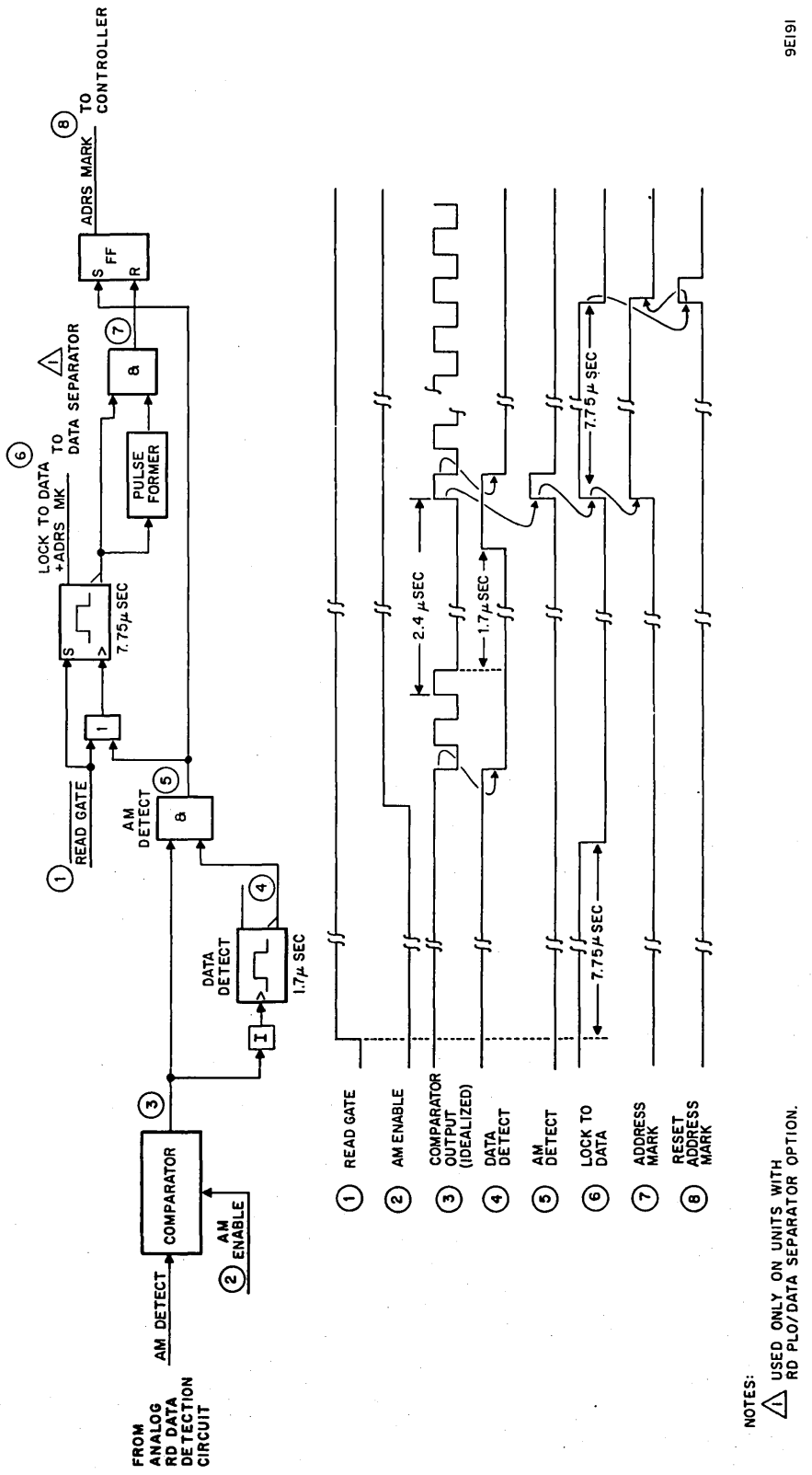


Figure 3-74. Lock to Data/Address Mark Detection Logic and Timing

The Lock to Data signal is active whenever the Lock to Data one shot is in the set state. This one shot is triggered (to the set state) when either the Read Gate signal (Tag 111, Bus Out bit 3) goes inactive or the Address Mark is detected.

When the Read Gate signal goes inactive it triggers the one shot and also causes it to be held in the set state. When the Read Gate signal goes active again, it removes the set conditions from the one shot and allows it to time out after 7.75 usec. Therefore, a 7.75 usec lock to data period occurs at the beginning of every read operation.

Detecting the Address Mark also triggers a 7.75 usec pulse from the one shot. The Address Mark consists of an area about 2.4 usec in length that contains neither MFM ones or zeros.

The address mark detection circuit is enabled only during read operations (Tag 3 and Bus bit 3 active). The controller activates the circuit by raising Bus Out bit 4 (Address Mark Enable).

The Address Mark Enable signal causes the comparator to start generating output pulses that trigger and retrigger the Data Detect one shot. The comparator generates the output pulses only when there are input data pulses. Therefore, during the Address Mark area the comparator stops generating pulses and the one shot times one 1.7 usec after the last data pulse was detected. The first data pulse following the Address Mark area enables the Address Mark Detect gate. This triggers the Lock to Data one shot which causes a 7.75 usec Lock to Data period and also a 7.75 usec Address Mark signal.

Read PLO and Data Separator (Applicable Only to Units with RD PLO/Data Separator Option)

General

This circuit has two functions: (1) to convert the MFM data from the analog to digital converter into NRZ data and (2) to generate a Read Clock signal which is locked to the frequency of the read data (9.67 MHz nominal). Both the NRZ data and the Read Clock signal are transmitted to the controller.

The read PLO and data separator circuits consist of four main parts (refer to figure 3-75):

- Input Control - Controls whether MFM data or 4.84 MHz clock pulses will furnish the input to the circuit.

- Data Strobe Delay - Delays the pulses to provide the proper unit to the VCO. These circuits also provide error recovery capability.

- Phase Lock Loop - Synchronizes the circuit outputs to the phase and the frequency of the inputs.

- Data Separator - Converts the MFM data to NRZ data and generates the Read clock. This circuit is actually a part of the phase lock loop.

The remainder of this discussion further describes the read PLO and data separator circuits.

Input Control

The input control circuit (refer to figure 3-75) selects the input that will be used by the read PLO and data separator circuits. This input will always be either MFM data from the read analog to digital converter or 4.84 MHz clock pulses from the servo frequency multiplier circuit.

The 4.84 MHz clock signal is used only when the drive is not reading MFM data, such as before Read Gate is raised. It also uses the 4.84 MHz clock whenever the Address Mark Enable signal is active because this indicates the drive is expecting the Address Mark which contains no MFM data. The drive uses the clock signal as a substitute for the read data for two reasons: (1) the signal is derived from the track servo dibits and therefore, its frequency (like that of the read data) varies directly with disk pack speed and (2) after being processed by the pulse forming circuits, it has about the same nominal frequency as the read data (9.67 MHz). This results in it being easier for the phase lock loop to synchronize to the proper frequency when switching from one of the signals to the other.

Once selected the signal is applied to a pulse forming network which generates a 20 nsec pulse for each transition of the input. These pulses are the applied to the data strobe delay circuits and also furnish the data input to the data separator.

Data Strobe Delay

The purpose of the data strobe delay circuit (refer to figure 3-75) is to delay the data pulses sufficiently to provide the proper timing relationship at the input to the phase lock loop. The output of the data strobe delay circuit is delayed

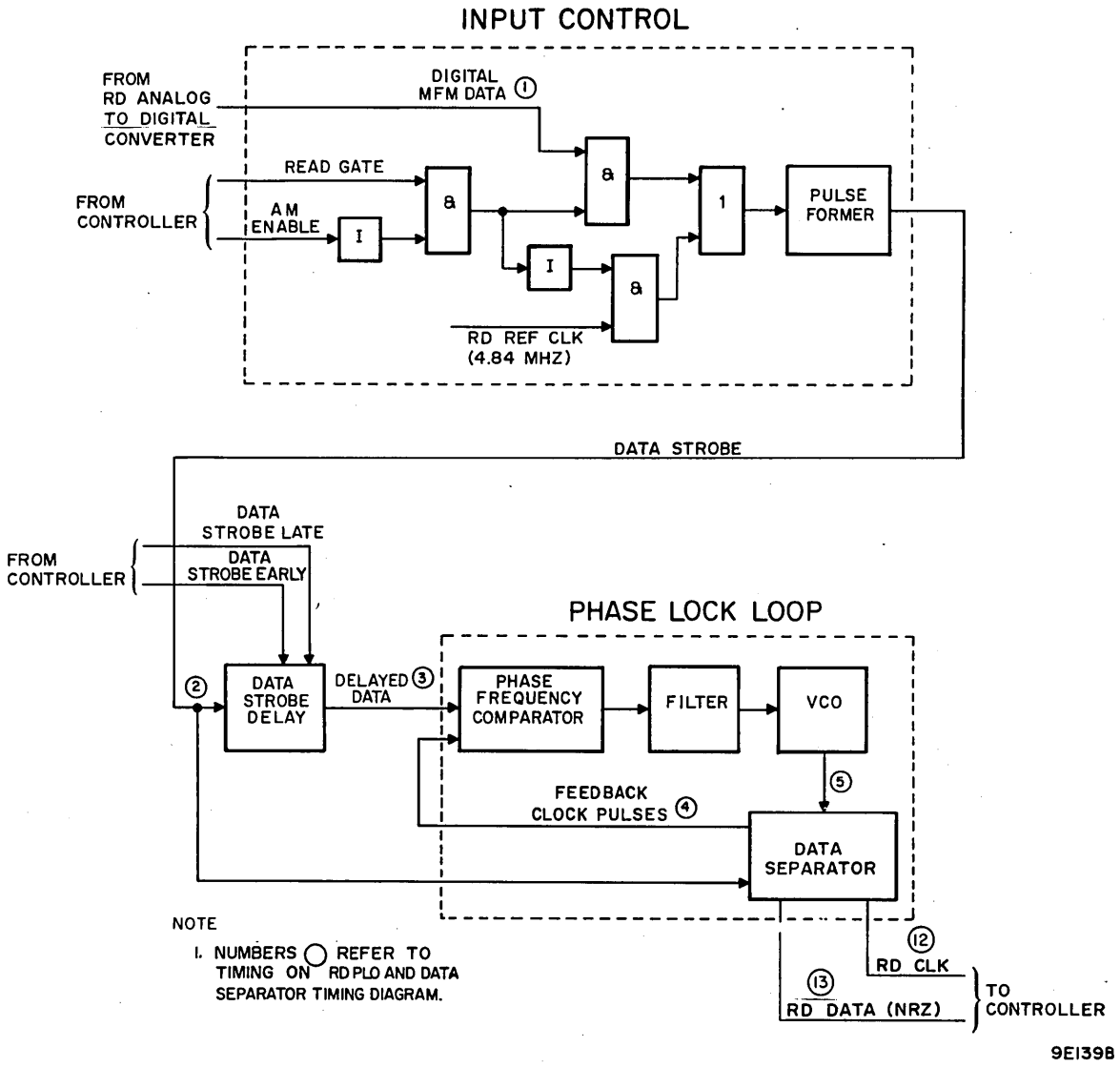


Figure 3-75. Read PLO and Data Separator Circuits

by a time determined by the state of the Data Strobe Early and Data Strobe Late signals. These signals facilitate the recovery of marginal data and are enabled by the Error Recovery tag (001).

The output of this circuit is the Delayed Data signals which are sent to the input of the phase lock loop.

Phase Lock Loop

The phase lock loop (refer to figure 3-75) synchronizes the read PLO/data separator circuit outputs (NRZ data and Read Clock) to the input (either MFM data or 4.84 MHz clock). The loop accomplishes this by comparing and following two signals: (1) the Delayed Data signals which have a constant phase and frequency relationship to the input MFM data or 4.84 MHz Clock (whichever is used) and (2) the Feedback Close Pulse signals which have a constant phase and frequency relationship to the output NRZ data and Read Clock signals. The loop inputs are applied to the phase/frequency comparator.

The phase/frequency comparator generates output pulses which are a function of the phase and frequency between the positive going edges of the inputs. The filter circuit uses the comparator outputs to generate a control voltage for the voltage controlled oscillator (VCO).

This control voltage causes the frequency of the VCO to vary in the direction necessary to eliminate the phase and frequency differences between the two signals that were input to the comparator.

The output frequency of the VCO is actually twice that of the input so for an input of 9.67 MHz it has an output of 19.34 MHz. However, the data separator divides this by two before generating the Feedback Clock Pulse signals thereby providing a feedback to the comparator that satisfies the loop.

Data Separator

This circuit determines if the data pulses represent a one or zero and then converts the data to NRZ. It also generates the Feedback Clock Pulses to the comparator and the 9.67 MHz Read Clock that is sent to the controller. Figures 3-76 and 3-77 show simplified logic and timing for the data separator circuit.

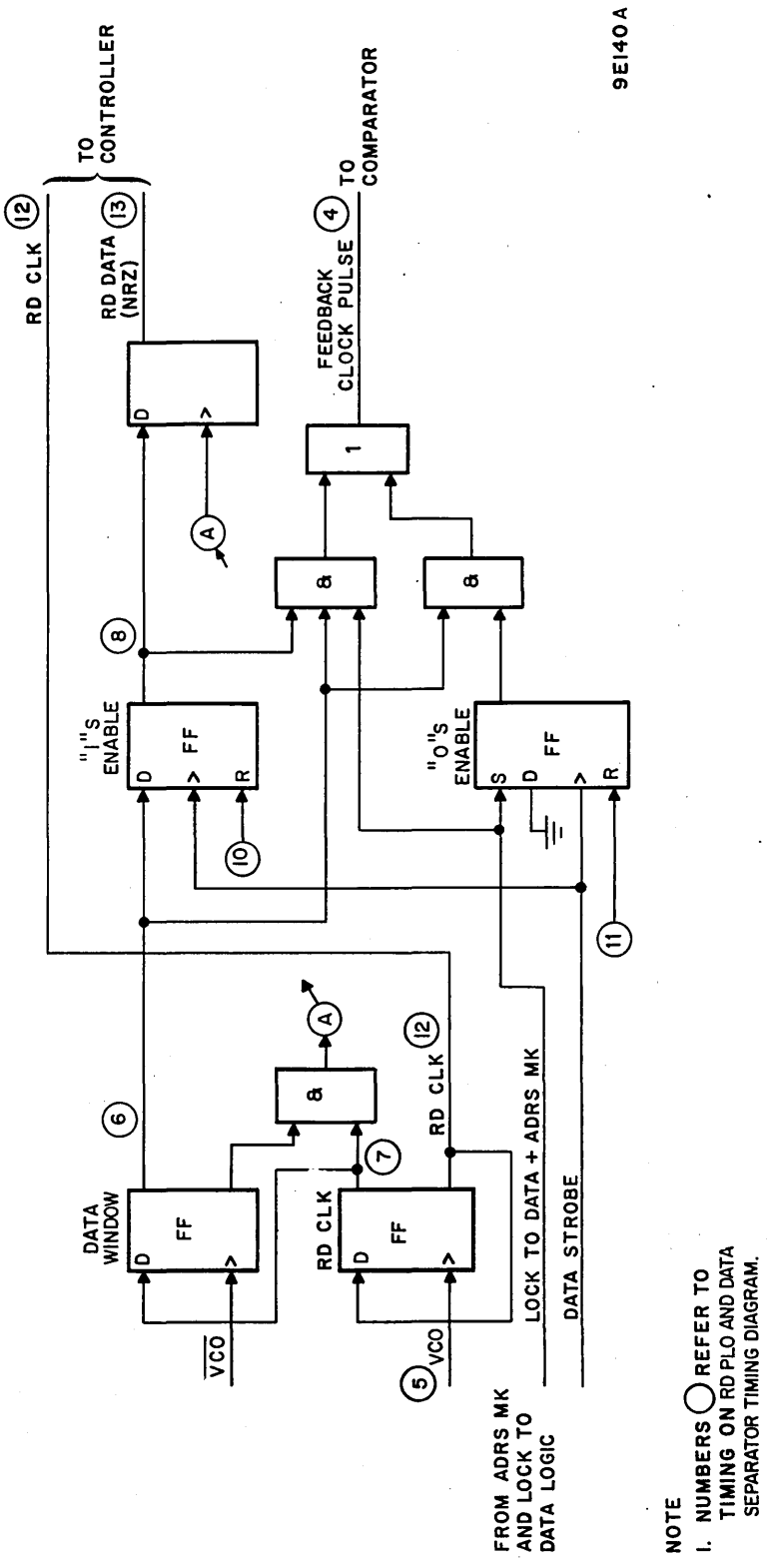
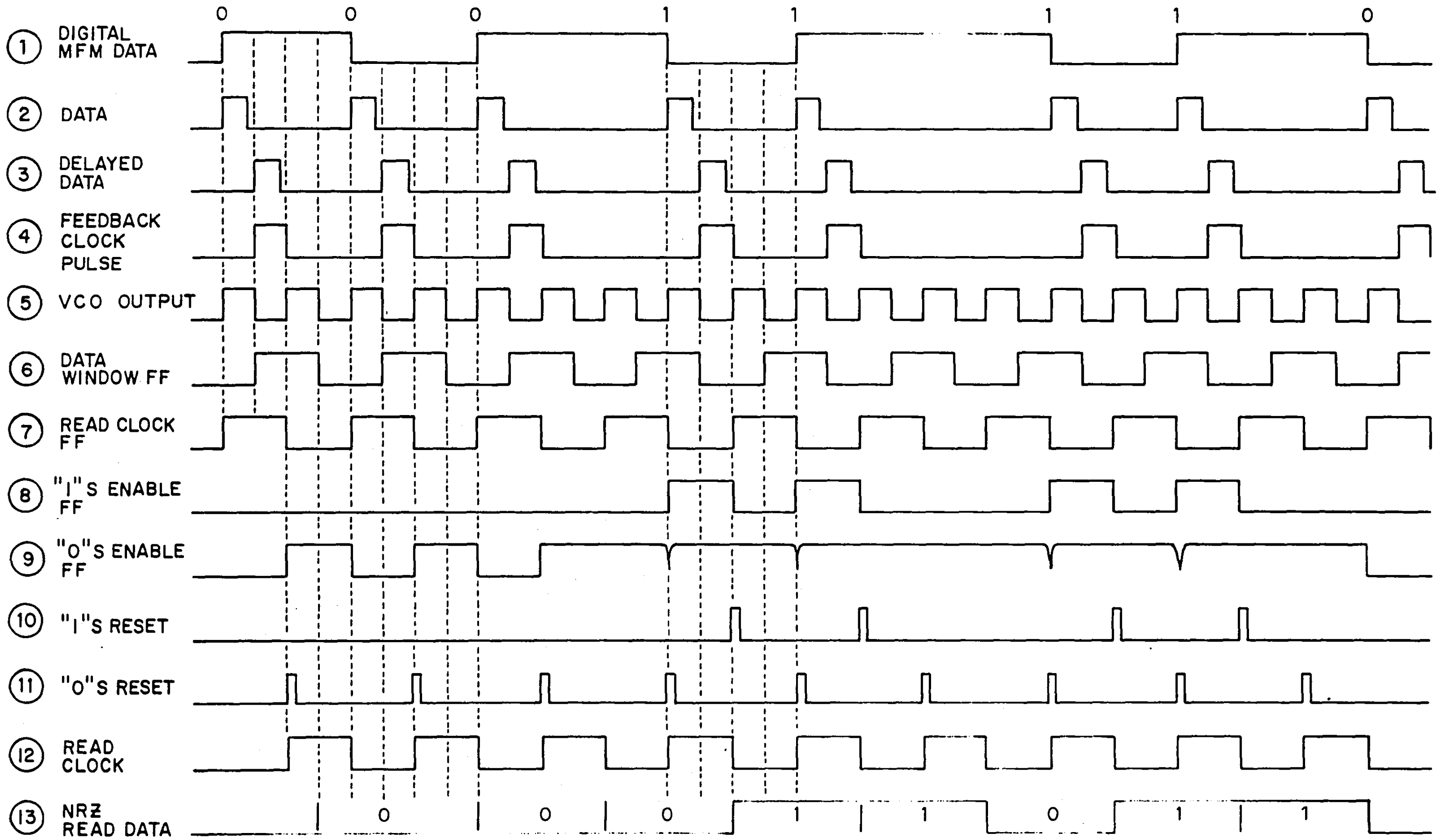


Figure 3-76. Data Separator Logic



NOTE

NUMBERS ◯ REFER TO THOSE ON FIGURE SHOWING RD PLO AND DATA SEPARATOR CIRCUITS.

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Figure 3-77. RD PLO and Data Separator Timing

The VCO outputs provide the proper timing relationships for the data separator by controlling the Data Window and Read Clock FFs. The Read Clock FF generates the 9.67 MHz Read Clock signal and also provides timing signals to the data separator logic. The Data Window FF generates the Data window which is used to determine whether the input data pulses represent ones or zeros. The actual decoding of the data is done by the "1's" Enable and "0's" Enable FFs.

If a data pulse represents a one it occurs during the data window and sets the "1's" Enable FF. Setting this FF generates a Feedback Clock pulse and causes the Data Buffer to generate a NRZ one.

If the data pulse represents a zero the "1's" Enable FF is not set and the Data Buffer FF generates a NRZ zero. In this case the "0's" Enable FF which is set by every data pulse generates the Feedback Clock Pulse signal.

Before accurate detection of data can begin, the proper phase relationship must be established between the data (representing ones and zeros) and the VCO output pulses. This is done during a 7.75 usec lock to data period which is initiated by the Lock to Data signal. This signal is a 7.75 usec pulse that occurs when the Read Gate signal goes true or when the Address Mark is detected. The Lock to Data signal holds the "0's" Enable FF set and disables the output of the "1's" Enable FF. Therefore, if the circuit is to synchronize properly the pulse must occur during a period when the drive is reading only zeros.

FAULT AND ERROR CONDITIONS

GENERAL

The following describes those conditions which are interpreted by the drive as errors. Error conditions either light an indicator at the drive and/or send a signal to the controller indicating an error has occurred.

These errors are divided into two categories: (1) those indicated by Fault Latch and register (2) those not indicated by Fault Latch and register. Both are explained in the following (refer to figure 3-78).

ERRORS INDICATED BY FAULT LATCH AND REGISTER

General

Certain errors set the drive's Fault Latch and also set the fault register latches associated with the error condition.

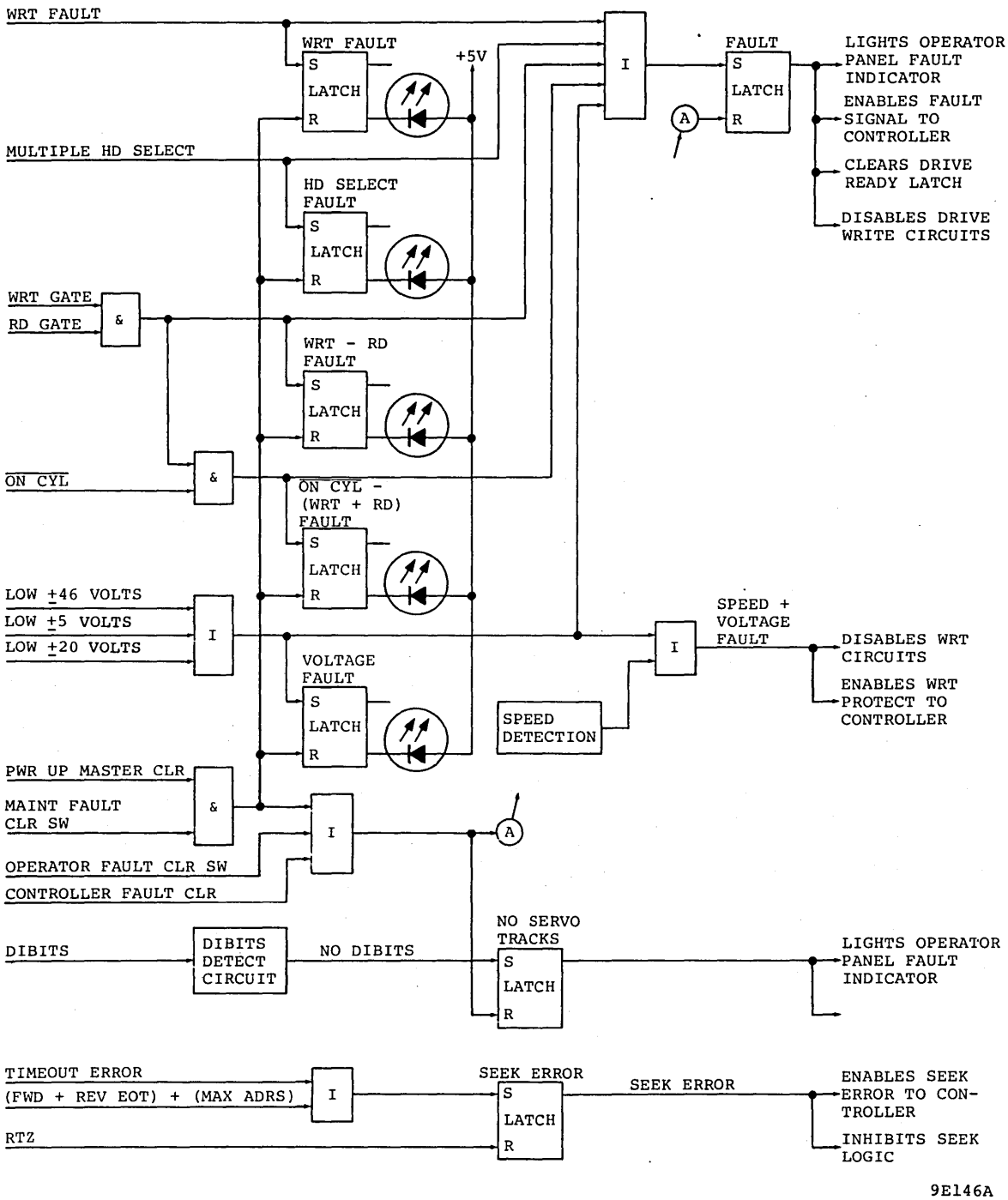


Figure 3-78. Fault and Error Detection Logic

Setting the Fault Latch does five things: (1) enables the fault line to the controller (2) lights the FAULT indicator on the drive's operator control panel (3) clears the drive's Unit Ready signal (4) inhibits the drive's write and load circuitry and (5) causes the Check Diagnostic bit (bit 7), of the Low Cylinder (110) and Control (111) Tag bus in status bytes (refer to discussion on I/O Signal Processing), to be true. These events prevent further drive operations from being performed until the error is corrected and the Fault latch is cleared.

Providing the error condition or conditions no longer exist, the Fault latch is cleared by any of the following:

- FAULT switch on operator panel.
- Controller Fault Clear signal from the controller.
- Maintenance Fault Clear switch on Fault card.
- Powering down the unit.

Whenever an error occurs that sets that Fault latch, it also sets a latch in the fault register. These latches provide a means of storing the error indication so it can be referred to later for maintenance purposes. They also cause a corresponding bit to be true in the Error Recovery (001) and Diagnostic (010) bus in status bytes (refer to discussion on I/O Signal Processing). The fault register latches are cleared only by powering down the drive or by the Maintenance Fault Clear switch on the fault card.

The following describes each of the conditions causing the Fault latch and fault register latches to be set.

Write Fault

A write fault is indicated if any of the following conditions exist:

- Low output from write driver indicating it may not be operating properly.
- Low current input to write driver.
- Low +22 volts to write driver.
- No write data transitions when Write Gate is active.

More Than One Head Selected

This fault is generated whenever more than one head is selected. The outputs of the head select circuits are monitored by summing and voltage comparator circuits. If more than one head is selected, the circuit generates a Multiple Select Fault.

Read and Write

This fault is generated whenever the drive receives a Read gate and Write gate simultaneously from the controller.

(Read or Write) and Off Cylinder

This fault is generated if the drive is in an Off Cylinder condition and it receives a Read or Write gate from the controller.

Voltage Fault

This fault is generated whenever the ± 46, ± 5 or ± 20 voltages are below satisfactory operating levels.

Errors Not Indicated by Fault Latch or Register

General

The following errors are detected by the drive but are not stored in the fault register and do not set the Fault latch. However, they do cause the drive to give other error indications as explained in the following paragraphs.

Low Speed or Voltage

The Speed or Voltage Fault signal goes true when the drive detects either a low voltage condition or that drive spindle speed is below 2700 r/min. When either of these are detected, the drive write circuits are disabled and the Write Protect signal is sent to the controller. These also result in an emergency retract of the heads (refer to discussion on Emergency Retract).

No Servo Tracks Fault

If dibits are not detected within 350 ms after the load seek sequence begins, the No Servo Tracks latch is set. This light the FAULT indicator on the drive operator control panel and also enables the Return to Zero (RTZS) logic. Enabling the RTZS logic causes the heads to unload. Another load cannot be started until the No Servo Tracks latch is cleared. The No Servo Track's latch is cleared in the same manner as the Fault Latch.

Seek Error

The Seek Error latch is set by any of the following error conditions:

- On Cylinder was not obtained within 500 ms from the start of the seek.
- Forward or reverse end of travel (EOT) sensed.
- Drive is commanded to seek to a cylinder address greater than 822 (410).

Setting the Seek Error latch enables the Seek Error line to the controller, inhibits the drive from performing another seek until the Seek Error latch is cleared, and also causes the Check Diagnostic bit (7), of the low cylinder (110) and control (111) tag bus in status bytes, to be true. The latch is cleared by a Return to Zero Seek command.

SECTION 3A

VDE DIFFERENCES

GENERAL

This section provides theory of operation descriptions for drives with VDE-approved power supplies. These units differ significantly from earlier units. Specifically, these units include a redesigned power supply that incorporates solid state switching on a number of new circuit boards. A different drive motor is used and it includes an externally mounted hysteresis brake assembly. A different motor mounting method is also used.

All descriptions in this section replace the corresponding descriptions in chapter 3. Minor differences between units are discussed in chapter 3.

POWER DISTRIBUTION

Power distribution consists of routing power to the various elements in the power supply, and throughout the drive so the power on sequence can be performed. Power distribution is controlled by circuit breakers on the power supply control panel. Power distribution circuits are illustrated on figure 3-79.

Site ac power is supplied to the power supply through jack J1 and is switched by circuit breaker CB1. Closing CB1 applies power to the hour meter M1, blower motor B1, and transformer T2. AC power is routed to the drive motor control triacs Q6 and Q7 through circuit breaker CB2. Although power is applied to the drive motor control circuits, the motor does not start until the power on sequence is initiated. Transformer T1 provides 10, 20, 28, and 46 V ac to the rectifier/filter board _CBN. The corresponding dc outputs from the rectifier/filter board are routed throughout the drive and are controlled by individual circuit breakers.

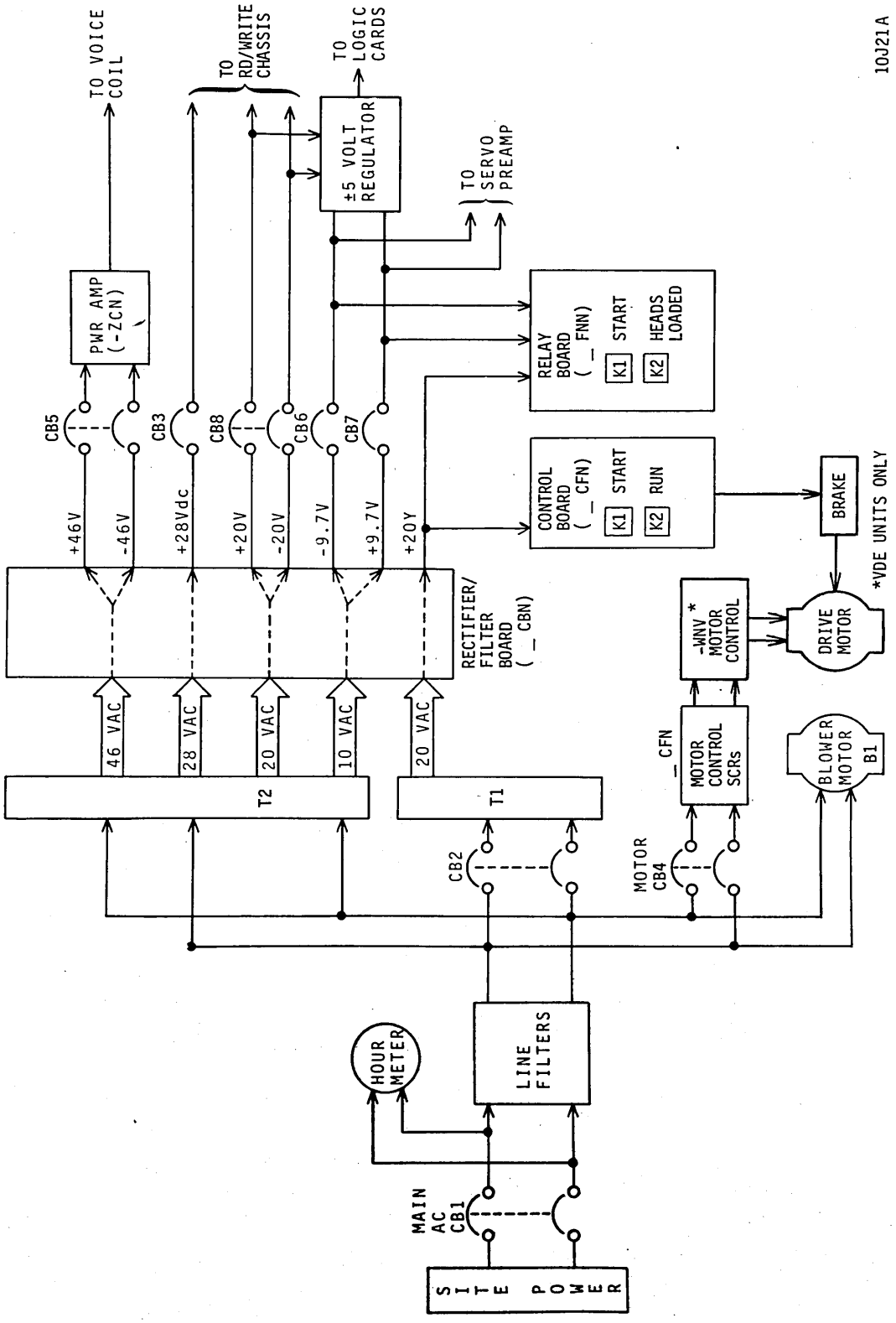


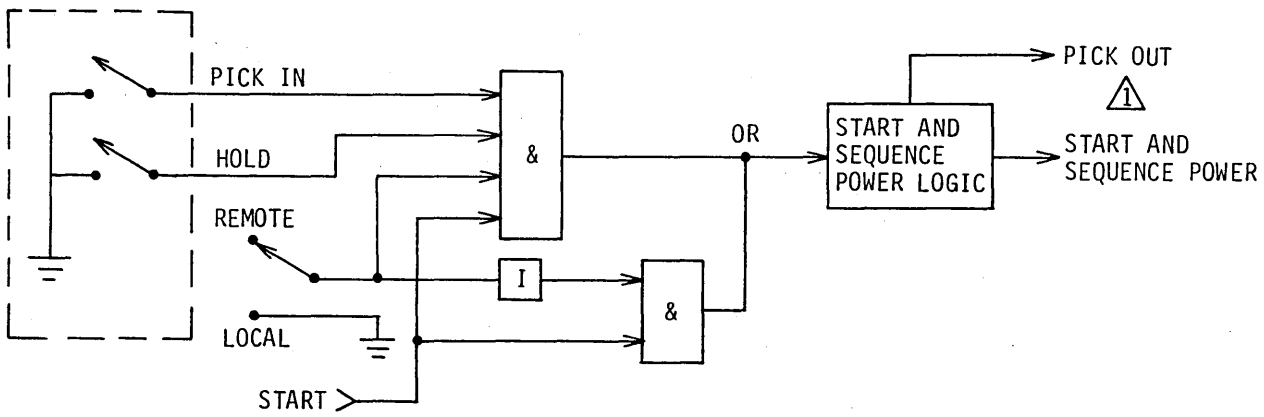
Figure 3-79. Power Distribution

LOCAL/REMOTE POWER SEQUENCING CONTROL

The power on and power off sequences on each drive can be controlled either locally or remotely depending on the setting of the LOCAL/REMOTE switch. This switch is located on the power supply control panel. With the switch in the LOCAL position the power on sequence is initiated at the drive. When the switch is in the REMOTE position, the sequences are initiated at the controller. Local/remote power sequencing circuits are illustrated on figure 3-80.

POWER ON SEQUENCE

The power on sequence starts the drive motor and loads the heads. See figures 3-81 and 3-82.



NOTES:

1. PICK OUT IS PICK IN ON NEXT DRIVE (IF APPLICABLE)

10J22A

Figure 3-80. Local/Remote Power Sequence

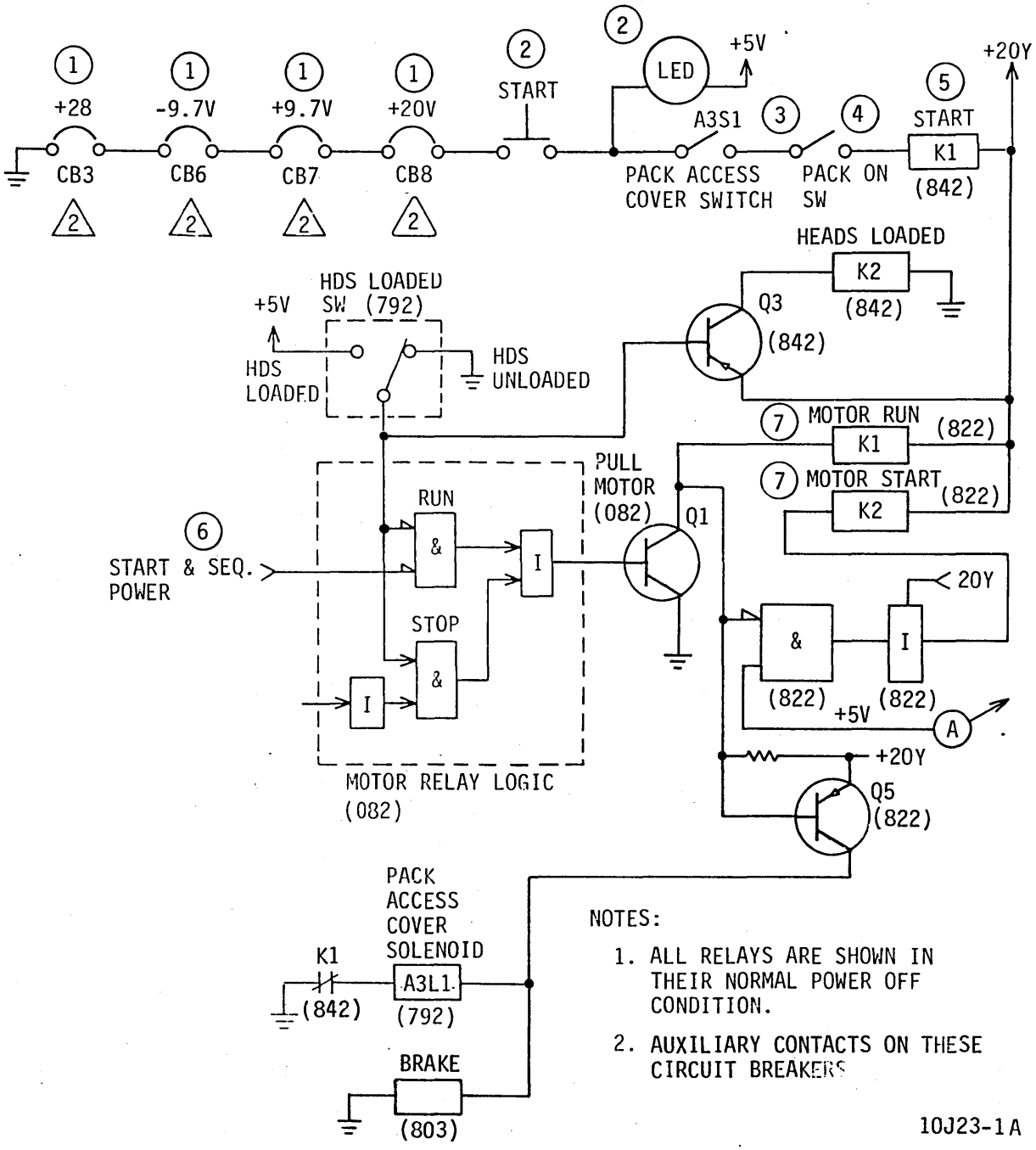


Figure 3-81. Power On Circuit (Sheet 1 of 2)

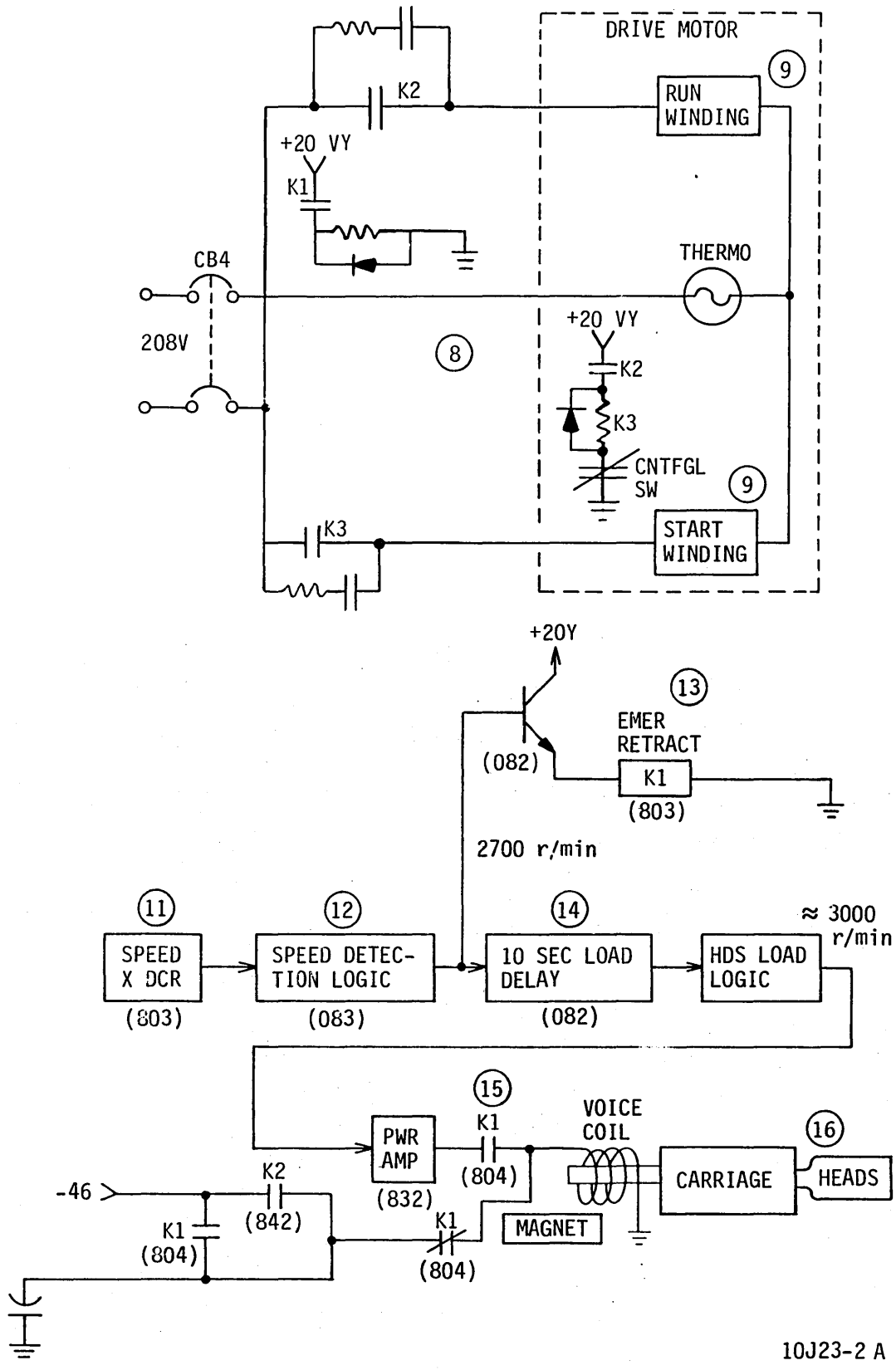


Figure 3-81. Power On Circuit (Sheet 2)

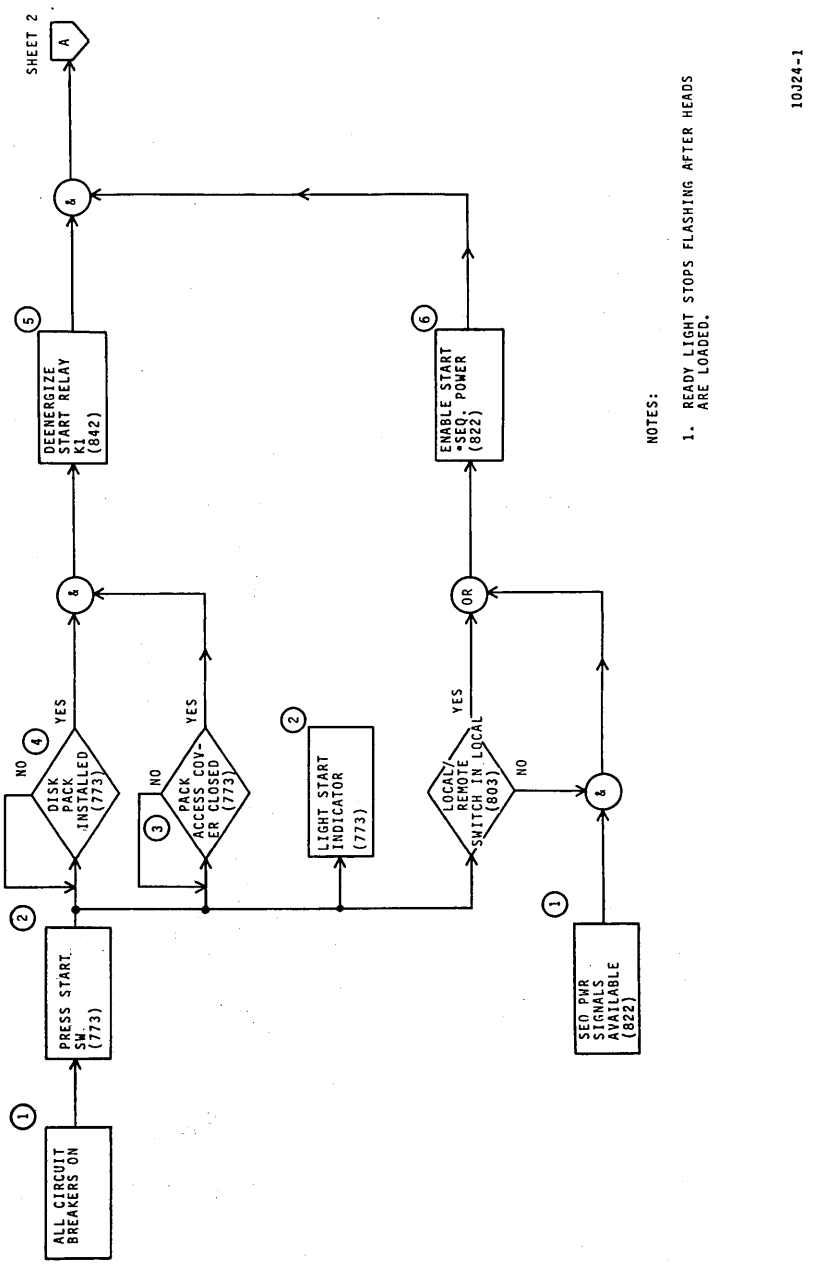


Figure 3-82. Power On Sequence Flow Chart (Sheet 1 of 2)

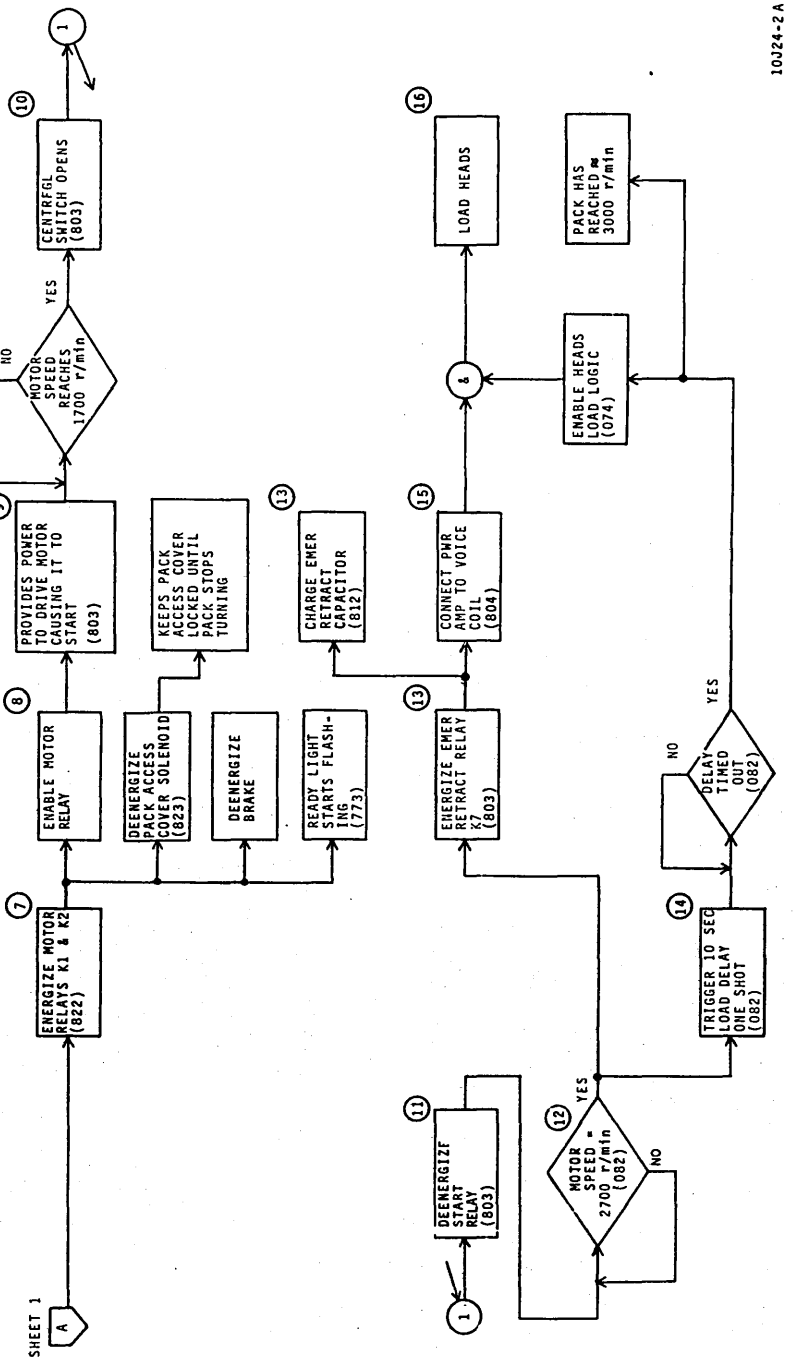


Figure 3-82. Power On Sequence Flow Chart (Sheet 2)

Provided all circuit breakers are closed, a pack is installed, and the access cover is closed, pressing the START switch:

- locks the pack access cover,
- deenergizes the Start Switch relay K1 on the relay board _FNN, and
- lights the START indicator.

The Start signal, entering the control board _CFN, initiates the Start and Sequence Power signal. The Interlock signal (all circuit breakers on) energizes DC relay K3 which connects ac power to transformer T2. Transformer T2 and the rectifier/filter board _CBN provides the dc voltages required by the drive.

Start and Sequence Power causes the Motor Start relay K2 and Motor Run relay to energize. These relays cause triacs Q6 and Q7 to turn on. This energizes the motor start and motor run windings; the motor begins to rotate.

At approximately 1700 revolutions per minute, the centrifugal switch in the motor opens and the Motor Start relay K2 deenergizes. Motor speed continues to increase and, at approximately 2700 revolutions per minute, pulses from the speed transducer generate an up to speed signal. A ten-second delay is initiated and, when the delay times out, the motor will be turning at 3000 revolutions per minute or more. The Up To Speed signal causes the Pull Speed relay (transistor Q3) to energize the Emergency Retract relay K1. The Emergency Retract relay connects the voice coil to the power amplifier. At a motor speed of 3000 revolutions per minute, the heads are able to fly over the disk surface and the head loaded sequence can occur. The head load sequence is explained in the discussion of Load Seeks.

POWER OFF SEQUENCE

The power off sequence consists of unloading the heads and stopping the drive motor. The sequence begins when the START switch is pressed, or if the Start and Sequence Power signal goes inactive. In either case, Start relay K1 energizes and the RTZ logic is enabled. The RTZ logic causes the heads to begin retracting. When the heads loaded switch transfers to the unloaded position, indicating the heads are unloaded, the Heads Loaded relay K2 deenergizes. The RTZ logic is disabled and the motor run winding will be removed; the motor begins to decrease in speed. As motor power is removed, the hysteresis brake is energized and the motor will begin to slow rapidly. The Emergency Retract relay K1 is deenergized to disconnect the voice coil from the power amplifier. The pack access cover so-

lenoid is energized and the cover may be opened only if the START switch is pressed (off).

Figure 3-83 illustrates the power off circuits and figure 3-84 is a flow diagram for the operation.

EMERGENCY RETRACT

The emergency retract circuits provide a means of retracting the heads from the pack area in the event of an emergency condition within the drive. This sequence is initiated if disk speed is reduced, or if conditions indicate that it may be reduced. Failure to retract the heads under these conditions could result in a head crash and subsequent damage to the heads and disk pack.

Any of the following conditions initiate an emergency retract sequence:

- Loss of ac power - If site ac power is lost, all dc power is also lost.
- Loss of any dc voltages causes the emergency retract relay to deenergize, thus initiating the sequence.
- Loss of speed - If motor speed drops below 2700 revolutions per minute, the speed detection circuits cause the emergency retract sequence to be initiated.
- Drive motor thermal overload - If the drive motor overheats, a thermal switch in the motor opens. This switch will remove power from the motor and, as it slows, the speed detection circuits initiate the emergency retract sequence

The emergency retract sequence is initiated when the Emergency Retract relay (K1) is deenergized due to any of the above conditions. As the relay deenergizes, the power amplifier is disconnected from the voice coil, and the voice coil is connected to the emergency retract capacitor. The charged capacitor discharges through the voice coil, thus retracting the heads.

Figure 3-85 illustrates the emergency retract circuits.

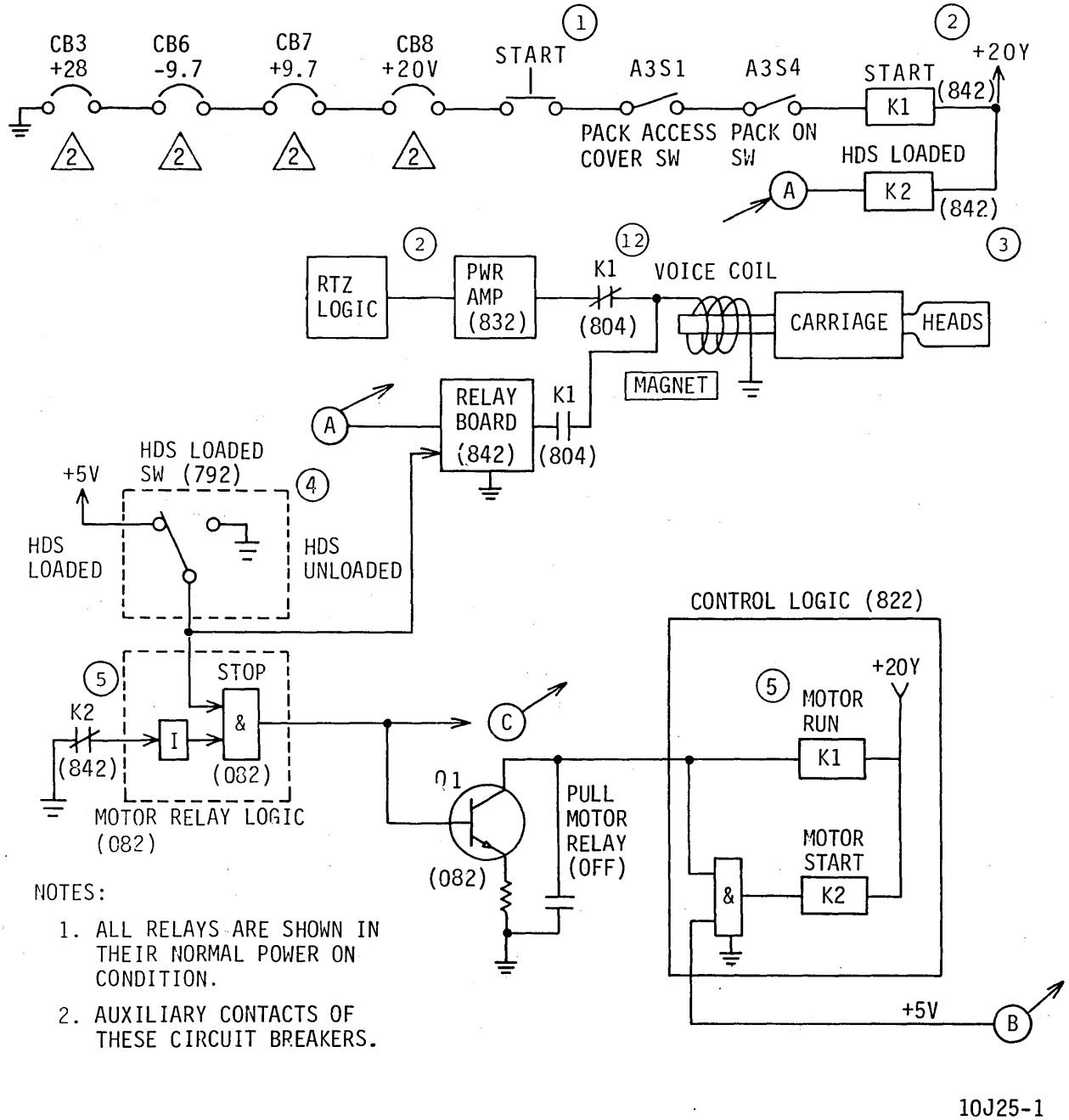


Figure 3-83. Power Off Circuits (Sheet 1 of 2)

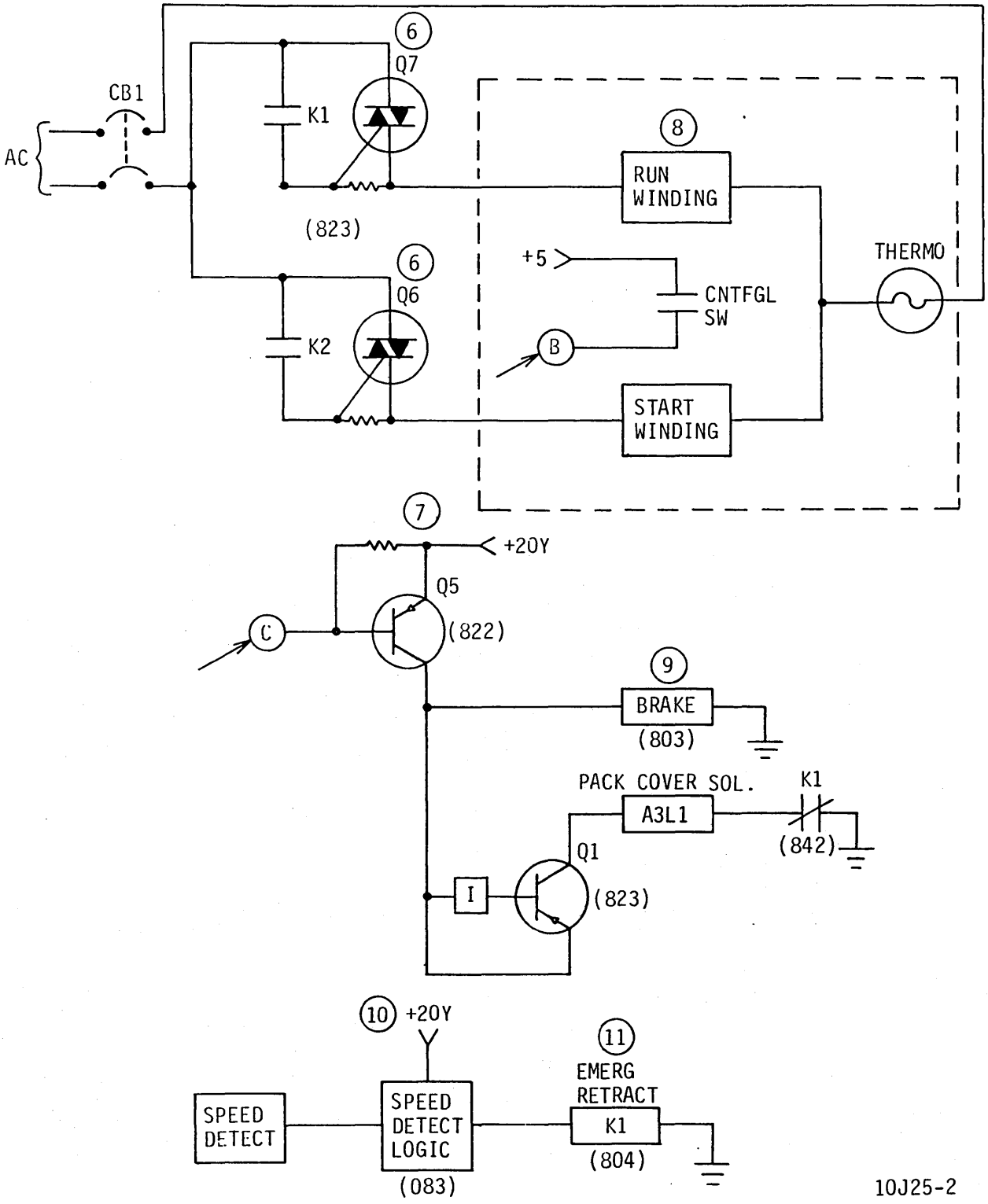


Figure 3-83. Power Off Circuits (Sheet 2)

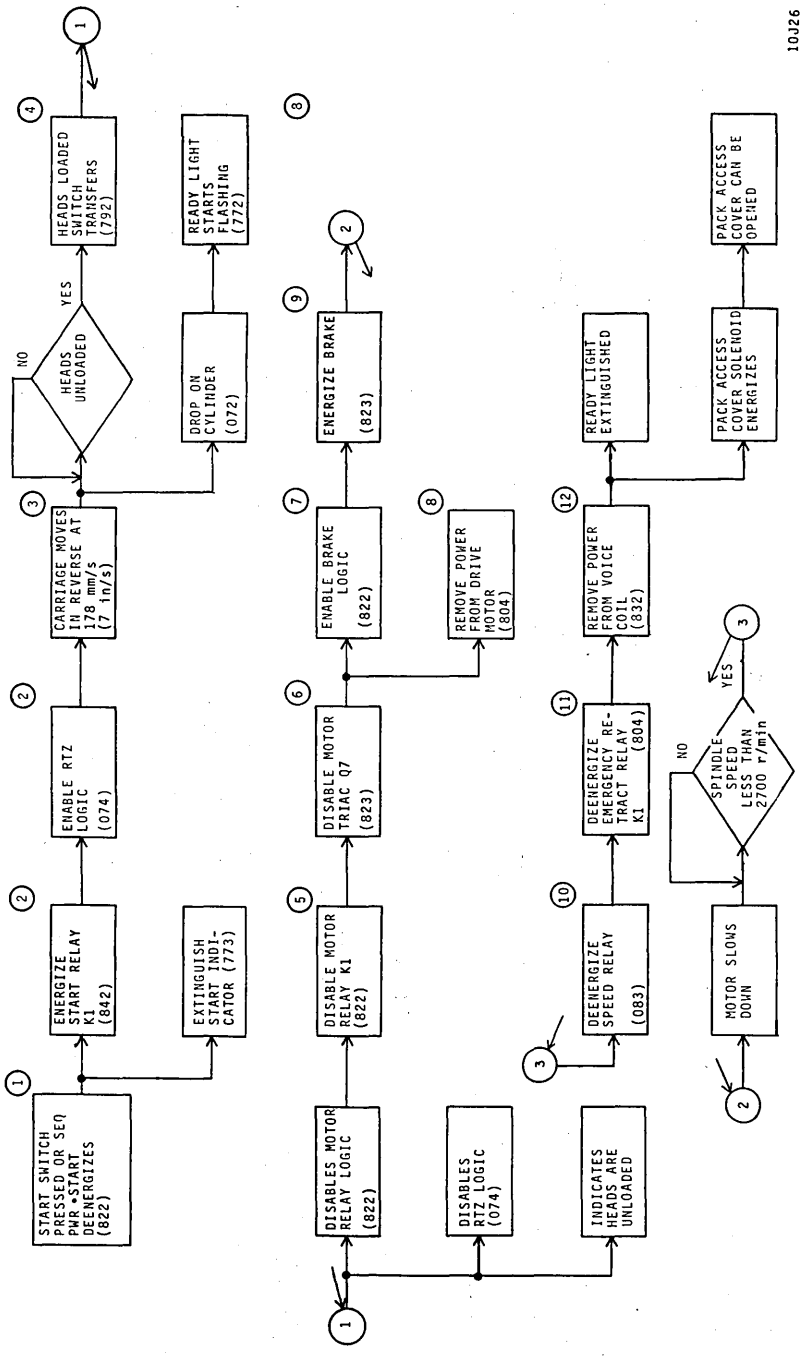
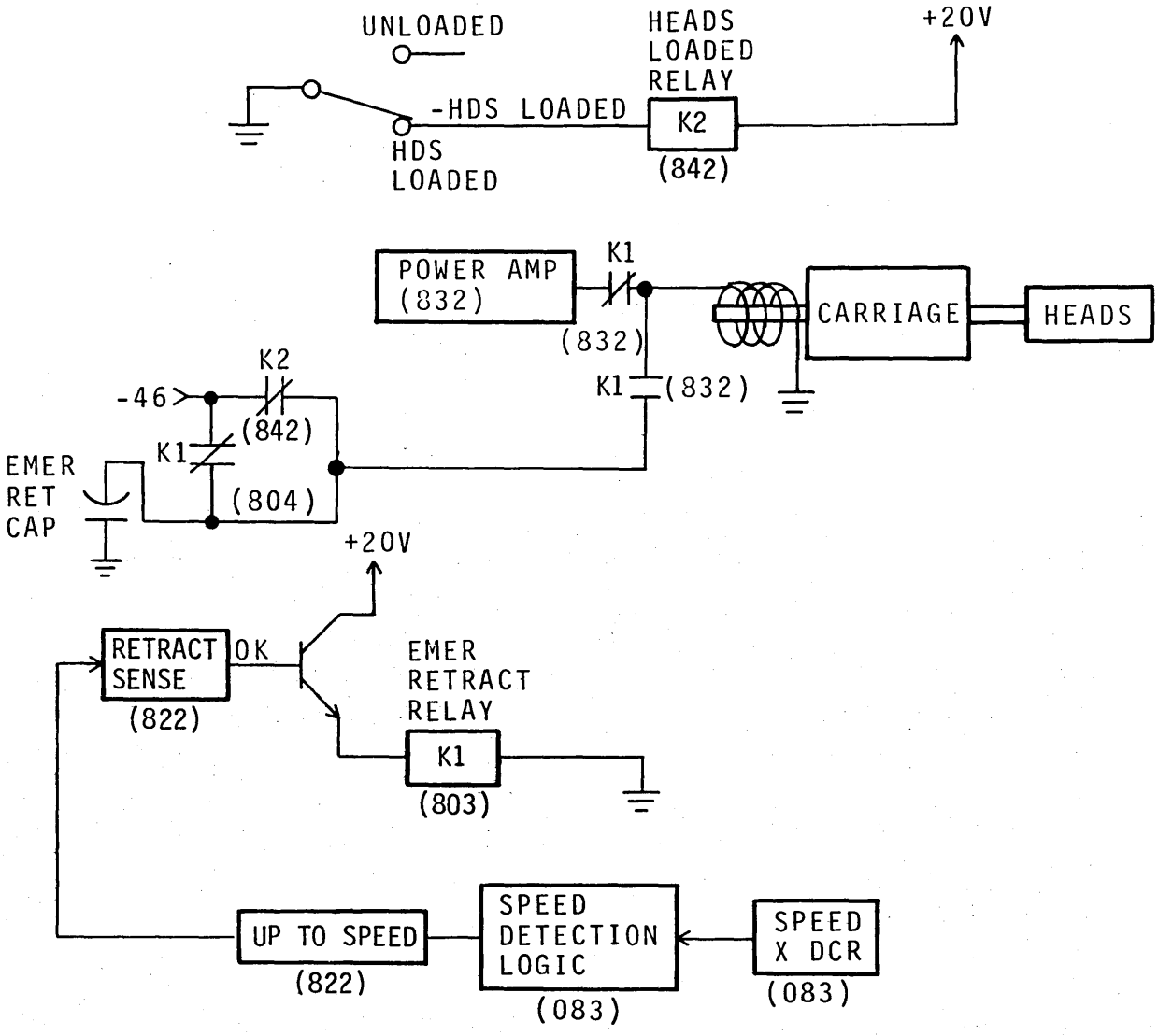


Figure 3-84. Power Off Sequence Flow Chart



NOTES:

1. ALL RELAYS ARE SHOWN IN ENERGIZED CONDITION.

10J27

Figure 3-85. Emergency Retract Circuits

SECTION 4

DISCRETE COMPONENT CIRCUITS

GENERAL

This section contains a circuit description for each type of discrete component circuit used in various drive models covered in this manual. These circuits use discrete components mounted on a card, and form specialized logical or analog functions for which no integrated circuit is available. Figure 4-1 is a typical example of the manner in which discrete component circuits are presented in this section. A schematic is provided along with the logic symbol for that circuit as it would appear in the logic diagrams manual. Only the circuit function (▷, amplifier in this case) and the circuit-type designator are shown within the logic symbols in this section. The circuit type, HAB, for instance denotes a high-level amplifier.

Numbers on the input and output lines indicate which transistors are being driven or which are acting as drivers. The brackets inside the symbol at both the input and output lines denote that those lines are differentials. A slash on any line shows that the signal level is a non-standard logic level.

Presentation of the circuit descriptions in this section is by the three-letter circuit type designator in alphabetical order.

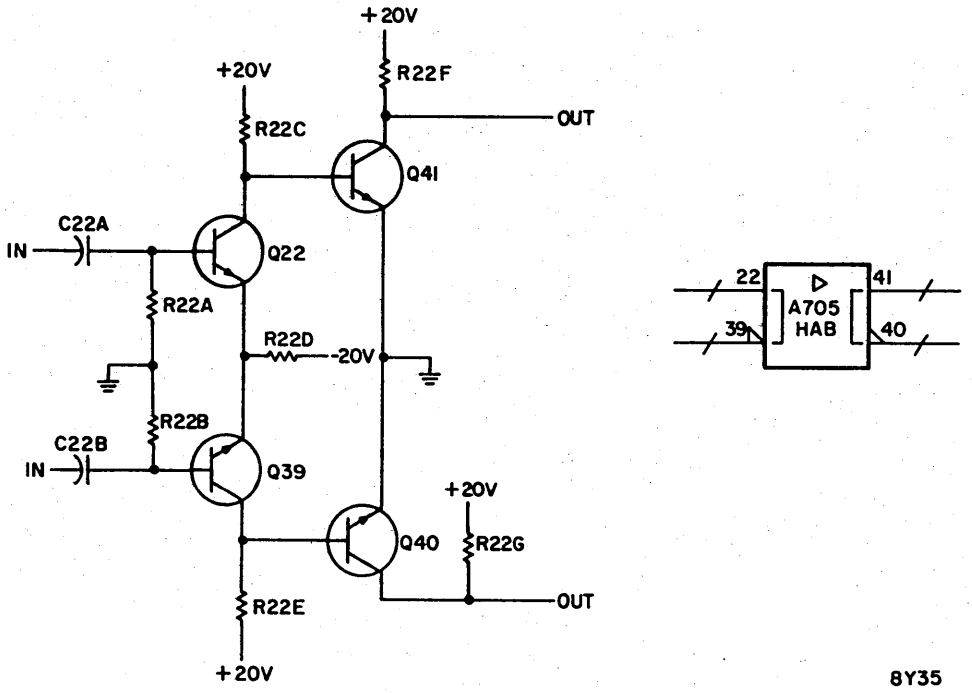


Figure 4-1. Typical Discrete Component Circuit Schematic

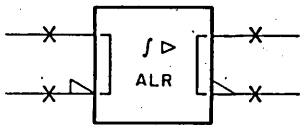
Amplifier and Filter - ALR

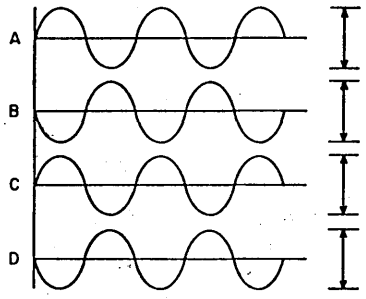
The ALR circuit is a differential amplifier and a 2 pole linear phase filter followed by a differential buffer amplifier. The amplifier stage has a gain of approximately 2.

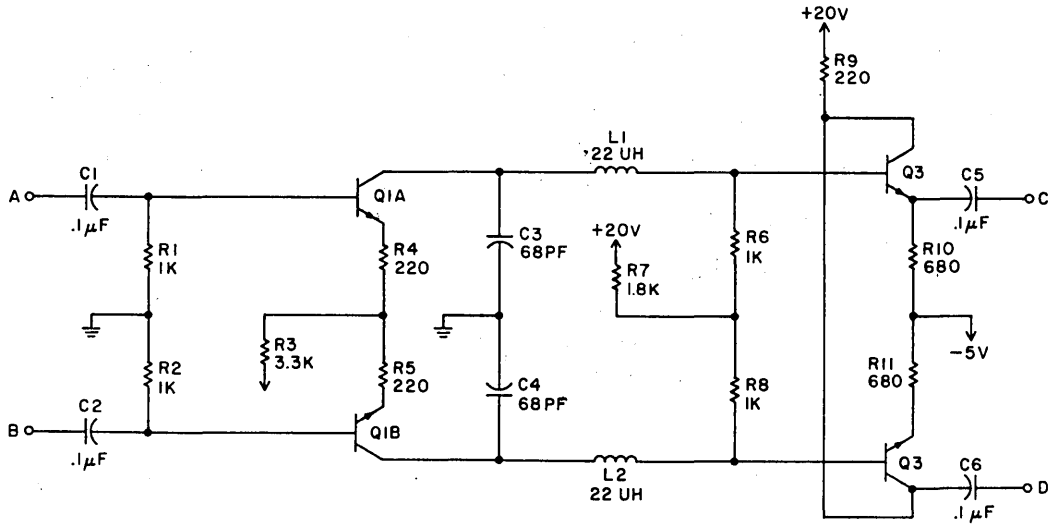
Q1A and B form the differential amp with R6 and R8 being the load resistors and also impedance matching resistors for the filter. The inductors L1 and L2 and capacitors C3 and C4 make up the rest of the filter. The upper break design fequence (-3 db point) of the filter is 3.13 MHz.

The input coupling capacitors C1 and 2 in conjuction with bias resitors R1 and 2 give the circuit a low frequency cutoff (-3 db point) of less than 2 kHz.

The output is a differential emitter follower buffer consisting of Q3 and 4 and R10 and 11, that is used to reduce the output impedance.







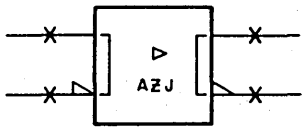
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

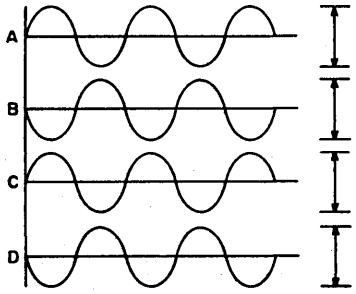
ALR
Rev A
Sheet 1 of 1

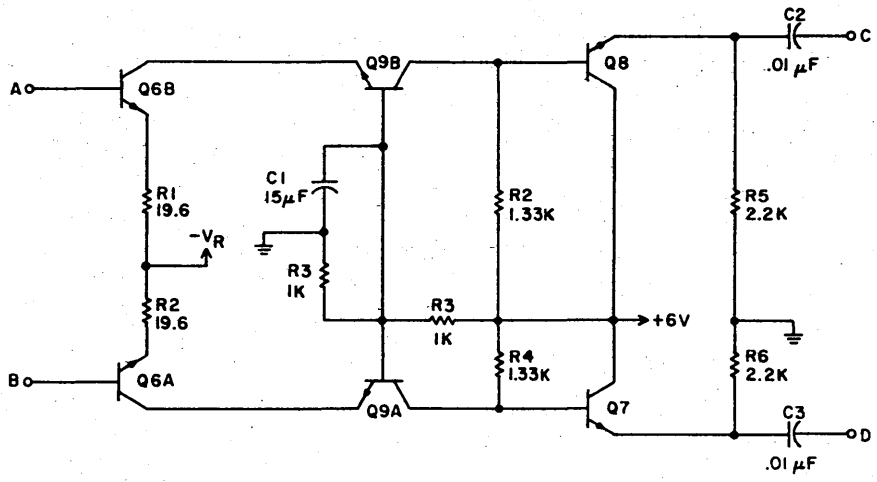
Differential Amplifier - AZJ

The preamplifier is a cascade type with a matched pair of transistors (Q6A and Q6B) used as a common emitter front end followed by another matched pair of transistors (Q9A and Q9B) used as a common base second stage, this effectively reduces the emitter collector capacitance of the common emitter front end.

The final stage of the front end is an emitter follower (Q7 and Q8) used as a buffer between the preamp and filter section. Resistors R1 and R2 in the emitter circuit give the front end an input impedance of just under 500 ohms. The constant current source for the preamp supplies approximately 2.5 ma.







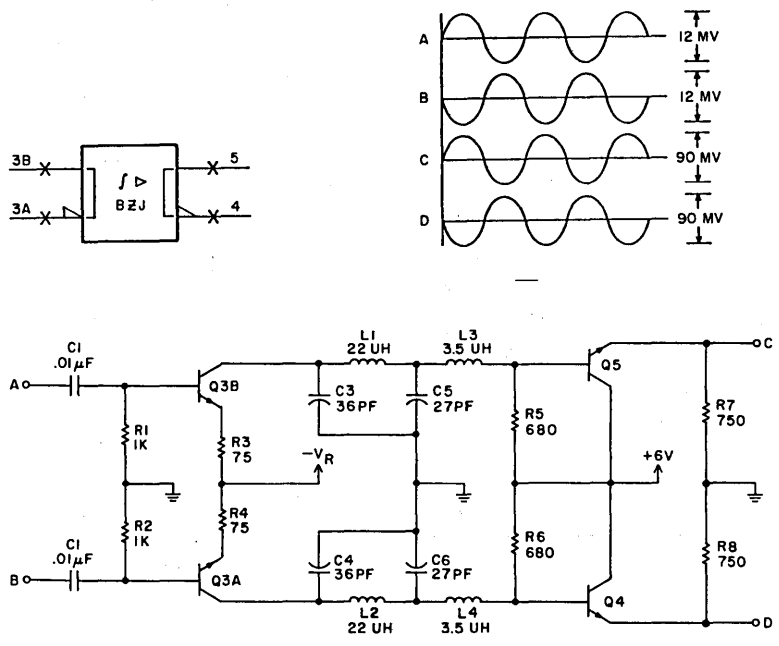
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

AZJ
Rev A
Sheet 1 of 1

Level Translator (Comparator Section) - BRD

The BRD circuit is a differential voltage comparator. It operates in conjuction with the SHT circuit to translate input signal levels below +23 V to a low TTL output, and input signal levels above +23 V to a high TTL output.

The BRD circuit functions in conjuction with the SHT circuit to indicate whether or not the write current is below a minimum value. (See SHT circuit description.) A voltage reference of +23 V is applied to the base of transistor QP. With normal write current, the base of QN is below +23 V. Under these conditions transistor QN is on and transistor QP is off, and the resistor in the collector circuit of QN provides a forward bias voltage to the SHT circuit. If the write current is below the acceptable minimum, the voltage at the base of QN goes above +23 V. Then QN turns off and QP turns on, and the resistor in the collector circuit of QN does not develop sufficient forward bias for the SHT circuit.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

BRD
Rev B
Sheet 1 of 1

Amplifier and Filter - BZJ

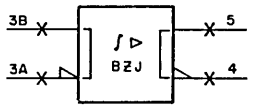
The BZJ circuit is a differential amplifier and a 4 pole low pass Butterworth filter followed by a differential buffer amplifier. The amplifier stage has a gain of approximately 7.5.

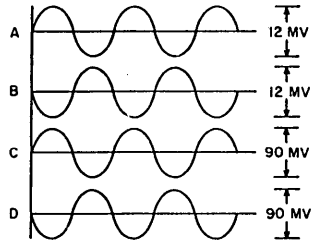
Q3A and B form the differential amplifier with R5 and R6 being the load resistors and also impedance matching resistors for the filter. The inductors L1, L2, L3, and L4 and capacitors C1, C2, C3, and C4 make up the rest of the filter. The upper break frequency (-3 db point) of the filter is approximately 6.8 MHz.

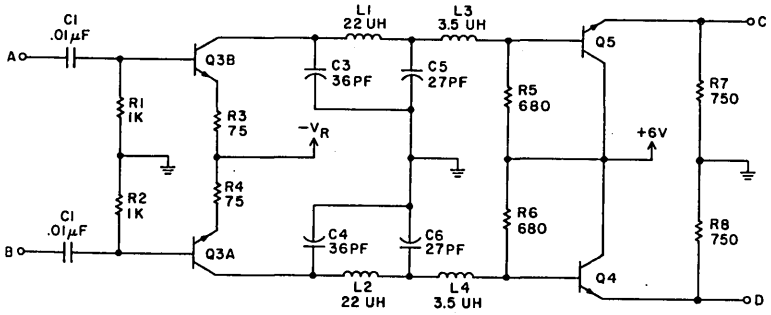
The input capacitors C1 and C2 in conjunction with resistors R1 and R2 give the circuit a low frequency cutoff (-3 db point) of less than 20 kHz.

The output is a differential buffer consisting of Q4, Q5, R7, and R8 that is used to reduce the output impedance and give more drive.

The constant current source for the differential amp supplies approximately 4.75 mA.



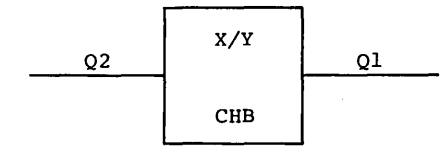


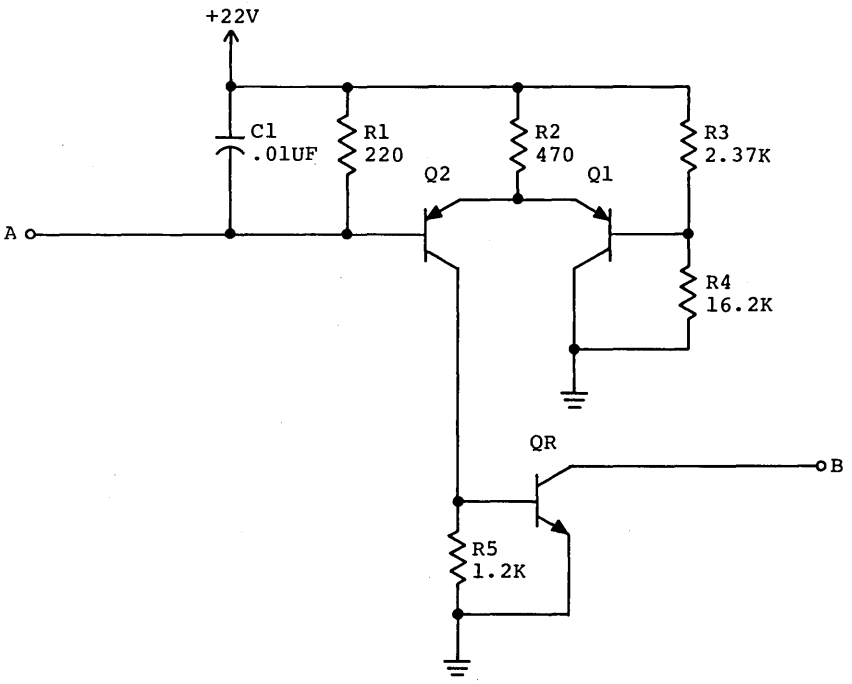


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

BZJ
Rev A
Sheet 1 of 1

Circuit functional description will be included in a later revision.

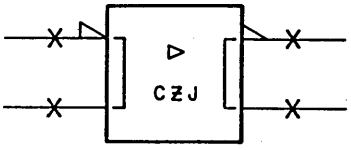


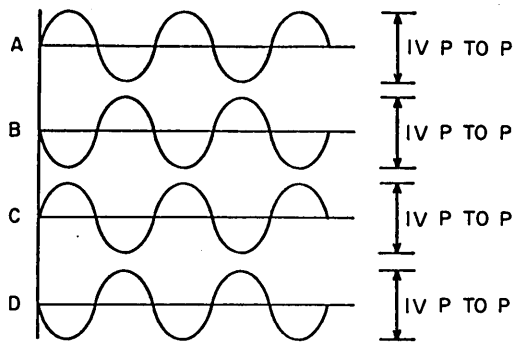


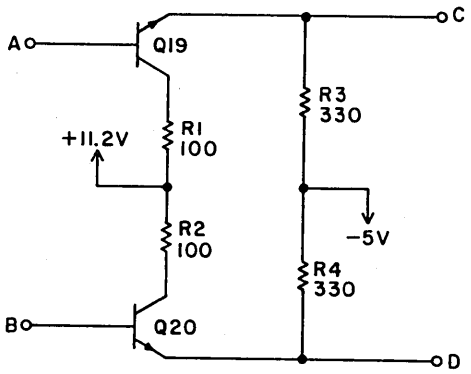
CHB
Rev A
Sheet 1 of 1

Buffer Amplifier - CZJ

The CZJ circuit is a buffer amplifier designed to increase the output signal driving capability of a differentially amplified signal. Q19 and Q20 are emitter followers that present comparatively high input impedance and low output impedance.







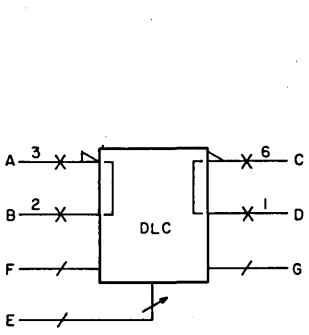
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

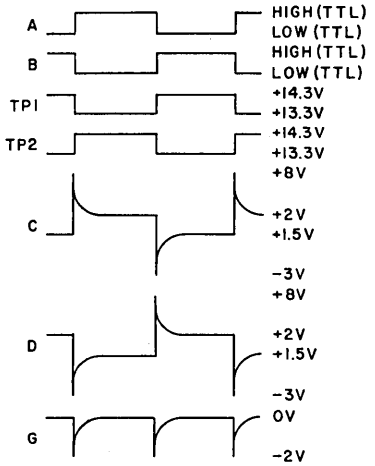
CZJ
Rev A
Sheet 1 of 1

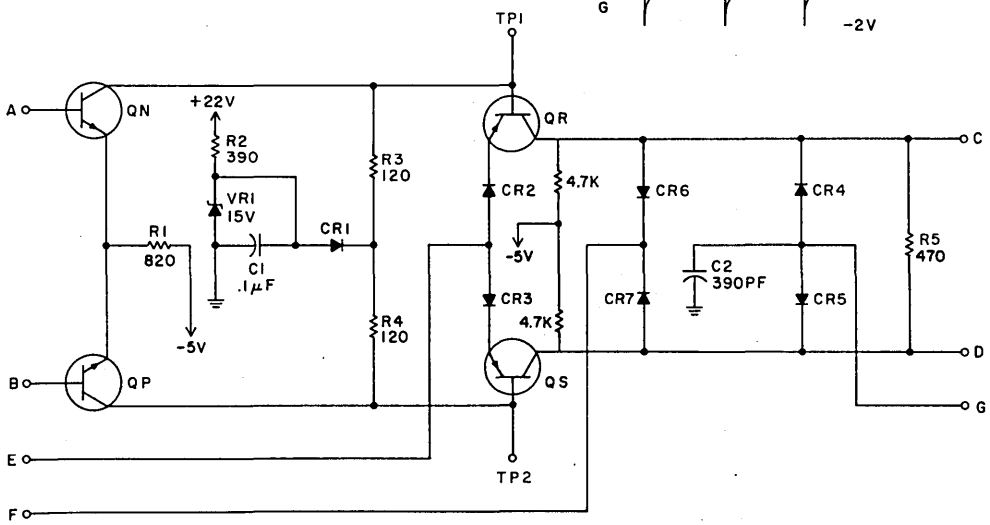
Write Driver - DLC

The DLC circuit is a differential current switch which converts voltage input signals to current for driving a differential recording head.

TTL level signals are applied to inputs A and B. Transistors QN and QP drive the bases of transistors QR and QS to control current to the head. The current source is connected to input E and supplied to the emitters of transistors QR and QS through diodes CR2 and CR3. Differentiated current is available to the head at outputs C and D. Diodes CR6 and CR7 provide a path to ground for write current when input F is grounded by a write protect circuit. Diodes CR4 and CR5 rectify the echo pulses from the head and apply them to a write voltage fault circuit through output G.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

DLC
Rev C
Sheet 1 of 1

Rectifier - DZJ

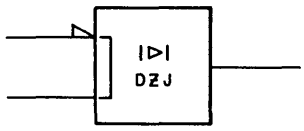
The DZJ circuit is a full wave rectifier with a differential input and single ended output.

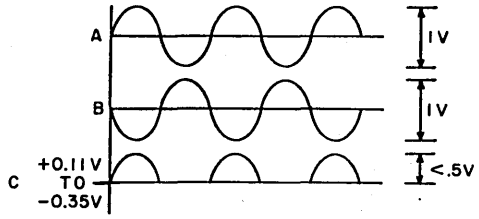
The rectifier consists of a matched pair of transistors (Q1A and B) used as differential pair. Q1A and Q1B conduct during the positive half input cycle and back biased during the negative half input cycle. Q2 is used as a constant current source supplying about 4.5 mA.

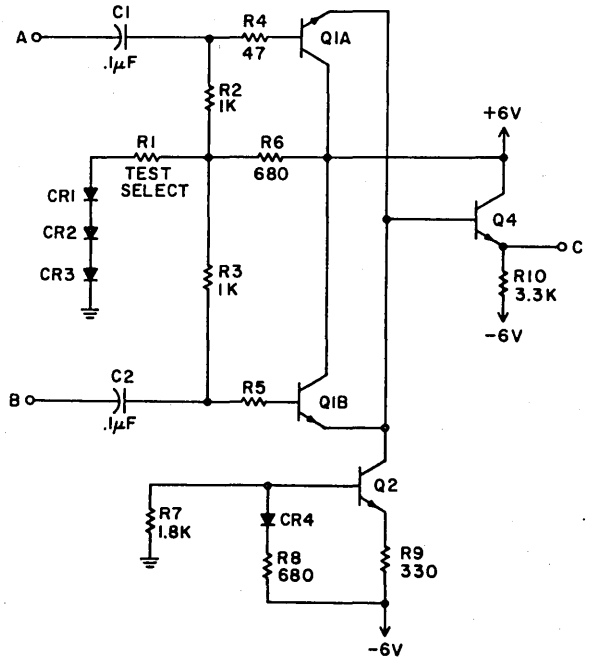
Diodes CR1, 2, and 3 along with test select R1 and R2 form an adjustable bias network. This adjusts the DC base line at output C from about -0.35 V to +0.11 V and is set so that the output of the AGC amplifier is 2V p-p.

The output buffer amplifier is Q4 and presents a comparatively high input impedance and a low output impedance.

The input frequence response is greater than 2 kHz.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

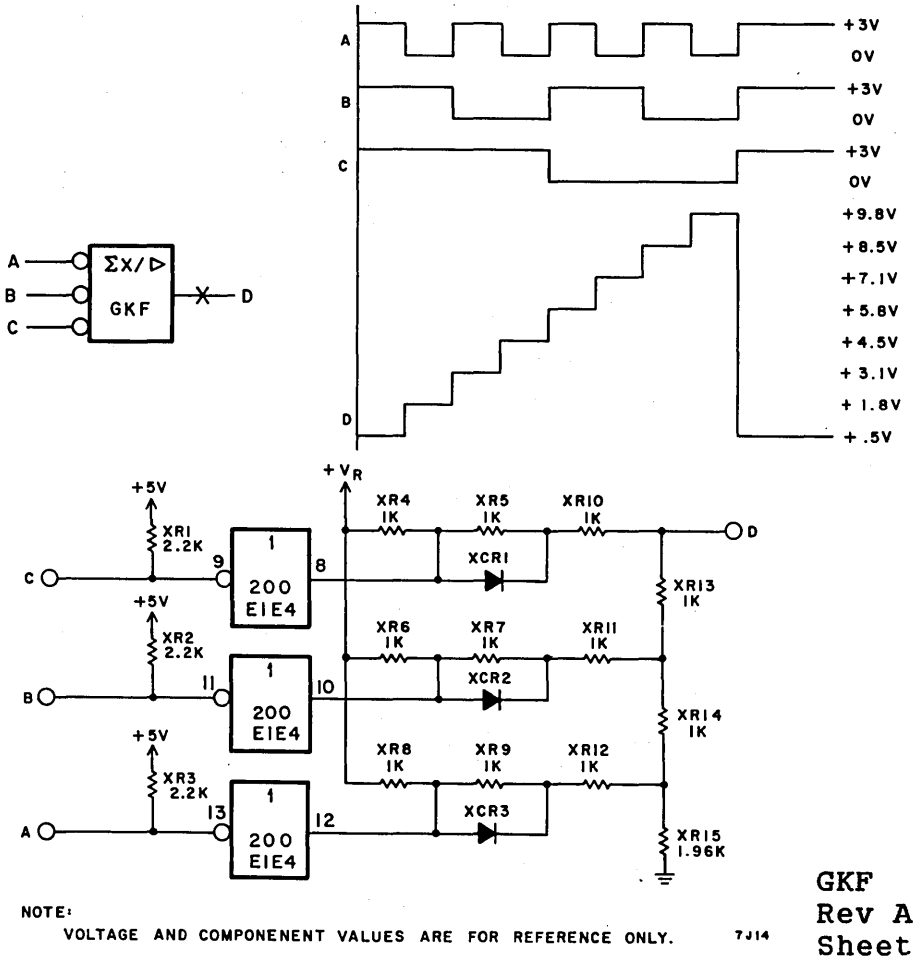
DZJ
Rev A
Sheet 1 of 1

Digital To Analog Converter - GKF

The GKF circuit converts three digital input signals to an analog output whose level depends upon the logical combination at the inputs.

The element 200 is an open collector IC. When pin 9 of element 200 is +3 volts or a "1", its output (pin 8) is 0 volts. When pin 9 is 0 volts or a "0", its output (pin 8) is open and the resistor divider (XR4, XR10, XR13, etc.) determines the voltage at point D.

When V_r is +12 volts the output at D corresponds to the various combinations of logic input shown in the waveform diagram.



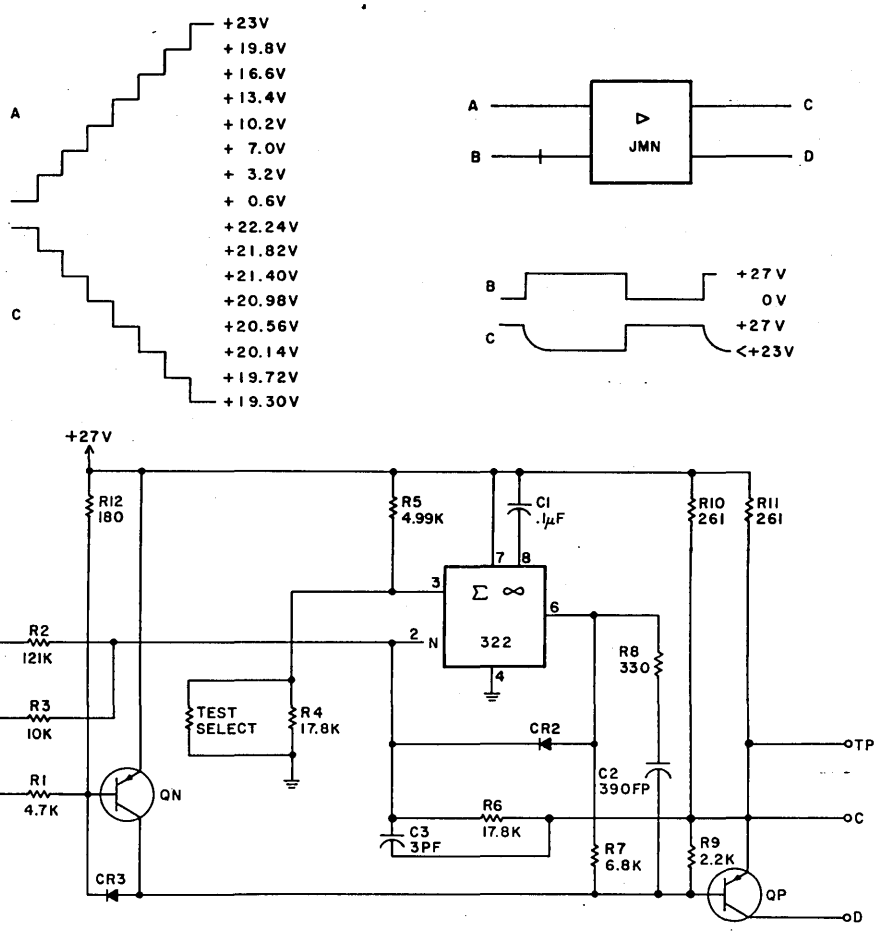
NOTE:
VOLTAGE AND COMPONENENT VALUES ARE FOR REFERENCE ONLY. 7J14

GKF
Rev A
Sheet 1 of 1

Voltage Controlled Current Source - JMN

The JMN circuit accepts an analog input voltage and converts it to a voltage controlled current for the write driver.

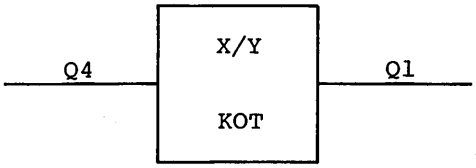
The JMN circuit receives the analog output of a digital to analog converter. The 322 operational amplifier in the JMN circuit inverts the analog input at A and translates the voltage level to drive the base of current source transistor QP. Write current output is supplied at output D. Current sensing is provided at output C so that other circuitry can test for proper current level output. Control from a write current protect circuit is applied to input B. Current is supplied at output D when input B is +27 V. Current source transistor QP is shut off when input B goes to ground.

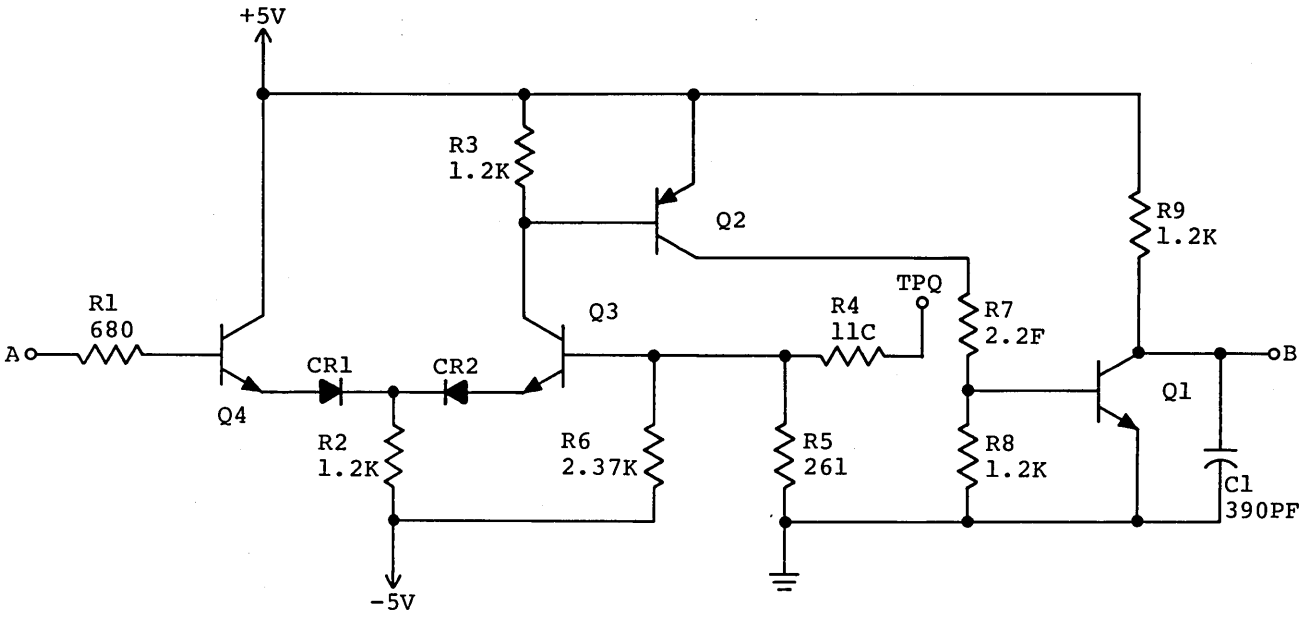


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

JMN
Rev B
Sheet 1 of 1

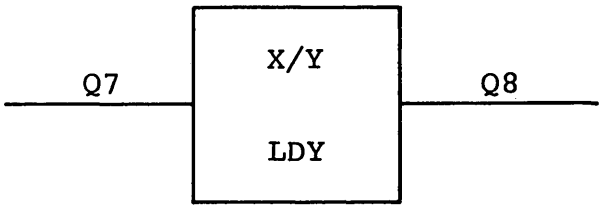
Circuit functional description will be included in a later revision.

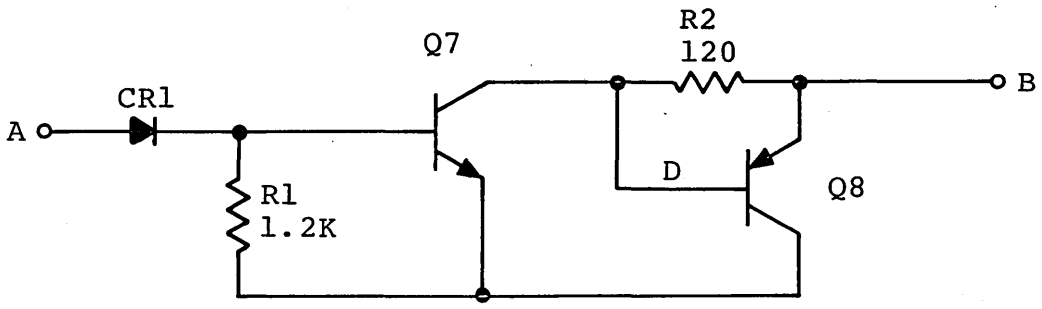




KOT
Rev A
Sheet 1 of 1

Circuit functional description will be included in a later revision.

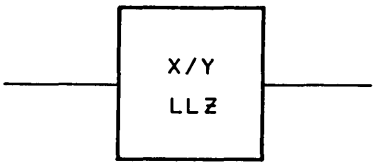


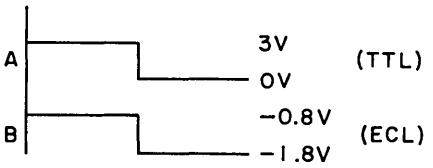


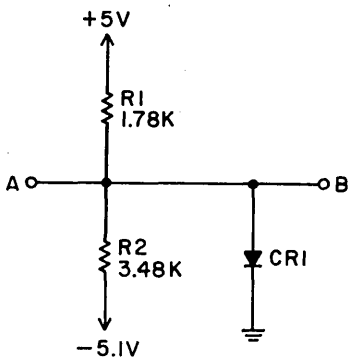
LDY
Rev A
Sheet 1 of 1

Passive Translator (TTL To ECL) - LLZ

R3 and R2 form a resistor that changes normal (and worst case) TTL levels into normal (and worst case) ECL levels. A "1" TTL will translate into a "1" ECL. R1 serves as a pullup in case there is no input and causes a "1" to be outputted. CR1 is a germanium clamp to limit the output voltage to +0.2 in case an input voltage of +5 or greater is applied.



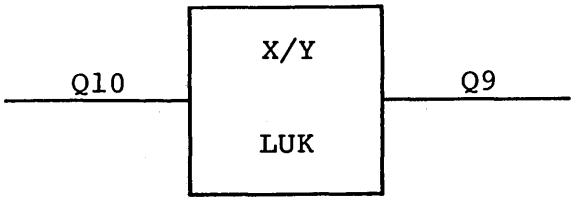


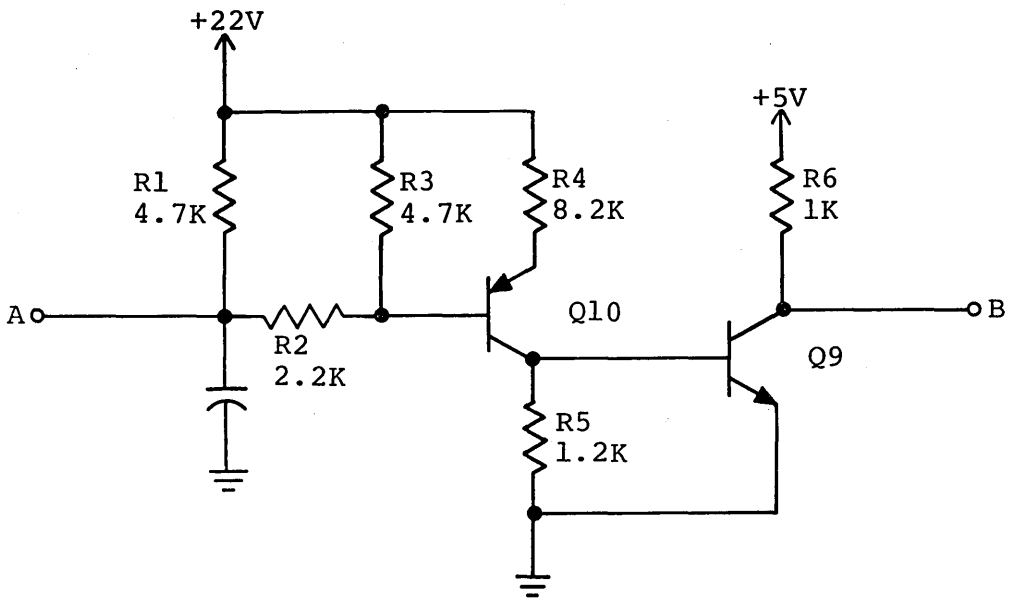


NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

LLZ
Rev A
Sheet 1 of 1

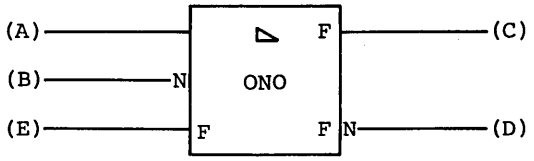
Circuit functional description will be included in a later revision.

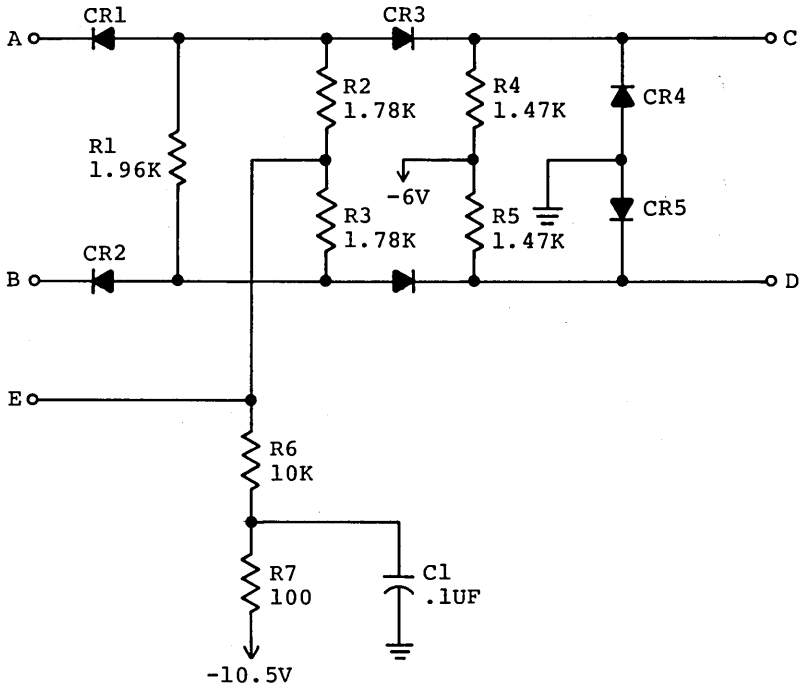




LUK
Rev A
Sheet 1 of 1

Circuit functional description will be included in a later revision.





ONO
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Delay - UBD/UBE/UBF/UBH/UBL

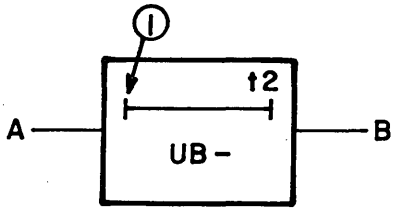
The capacitor delay circuits delay a "1" input at A for a specified period of time before providing a "1" output at B. Delay time for a "0" pulse is negligible.

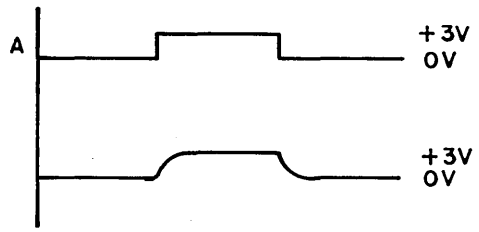
Assume a "0", (ground) enters at A. If the capacitor is discharged, it remains discharged and the output remains "0". If the capacitor is charged when the "0" signal appears, the capacitor discharges almost instantaneously, and the "0" appears with no noticeable delay.

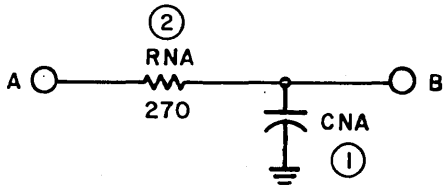
If a "1", +3 volts, enters A while the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage before a "1" can appear at B. The required charge time is the delay time of the circuit. The charge time is dependent on the capacitor value, the resistance between the source voltage and the capacitor, and the minimum voltage required to produce a "1" output.

Delay times for capacitive delays used are as follows:

Delay Type	Time
UBD	200 nsec
UBE	0.5 ms
UBF	0.2 ms
UBH	100 nsec
UBL	25 nsec







NOTES:

(1) VARIES WITH TYPE

(2) NOT USED ON UBF AND UBL

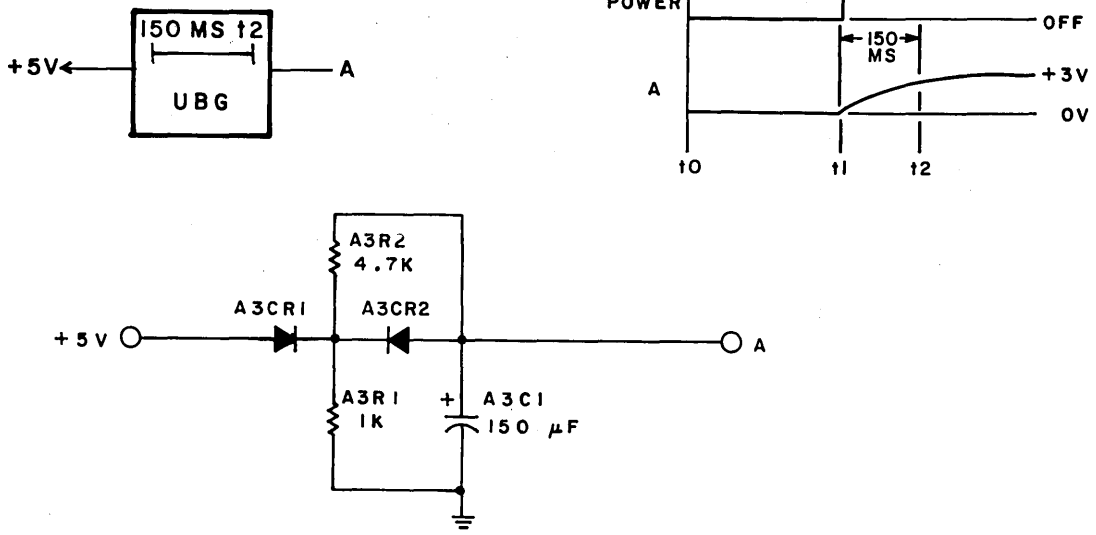
UB-
Rev B
Sheet 1 of 1

Delay - UBG

The UBG circuit is used to delay application of +5 volts during a power up sequence. Output A drives a standard TTL gate (element number 140).

During a power off phase (t_0), capacitor A3C1 is discharged. When power is applied (t_1), input A is still below the turn-on threshold of the TTL gate due to the discharged state of A3C1. However, the capacitor begins charging through A3CR1, A3R2 and the input resistance of the TTL gate. At time t_2 the capacitor voltage reaches the turn-on threshold of the TTL gate (approximately 1.5 V). The capacitor then continues to charge to full capacity.

When the +5 voltage is removed, A3C1 discharges through A3CR2 and A3R1 returning circuit output A to a level below the turn-on threshold of the TTL gate.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J37

UBG
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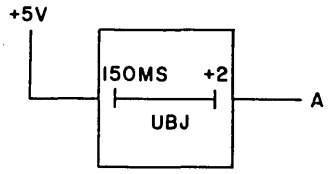
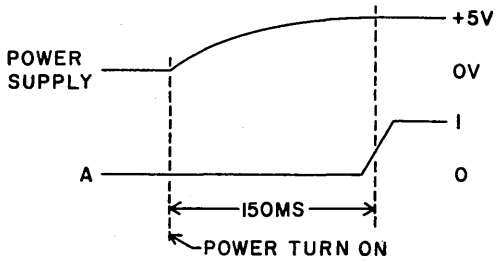
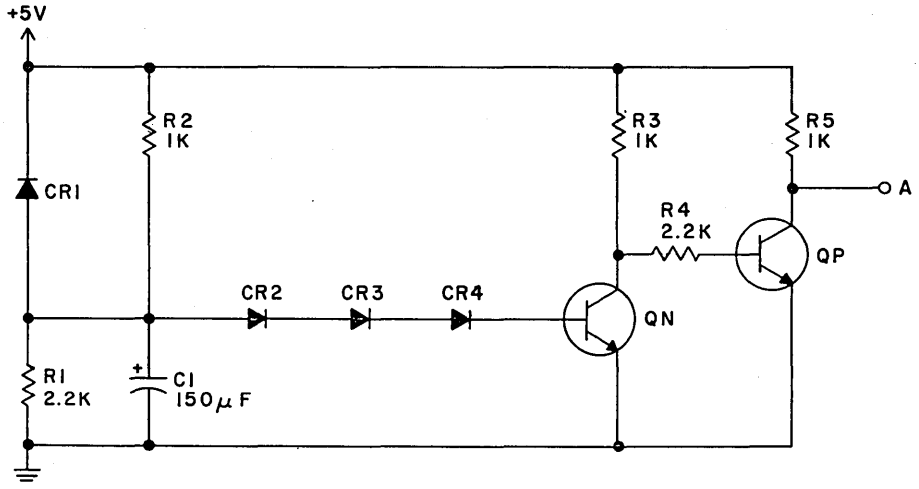
Delay - UBJ

The UBJ circuit delays application of a "1" to a standard TTL circuit after power is applied.

When power is applied to the UBJ circuit, C1 is charged through R2. After approximately 150 ms from initiation of power-up transistor QN is turned on and transistor QP is turned off, providing a TTL level "1" at output A.







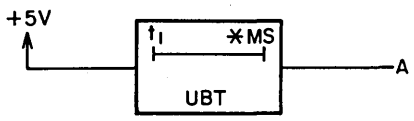
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

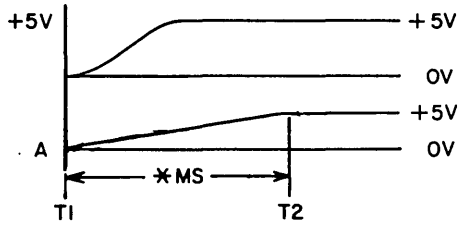
UBJ
Rev A
Sheet 1 of 1

Delay - UBT

The UBT delay circuit delays application +5 volts to a standard TTL gate during a power up sequence.

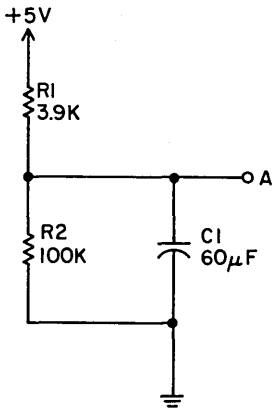
Applying +5 V (T1) slowly raises output A to +5 volts as C1 is charging. As the voltage across C1 approaches 5 volts, output A raises to 5 volts after a specific delay time determined by the values of R1, R2, and C1.





* TYPICAL DELAY TIMES

R1	R2	C1	DELAY TIME
3.9K	100K	60μF	80 MS
6.8K	10K	60μF	30 MS



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

UBT
Rev A
Sheet 1 of 1

Delay - UC

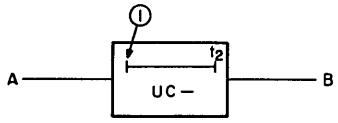
The UC-delay circuit is used to delay open-collector integrated circuits. The circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5 V and a capacitor connected to ground.

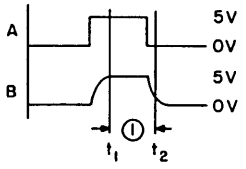
Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

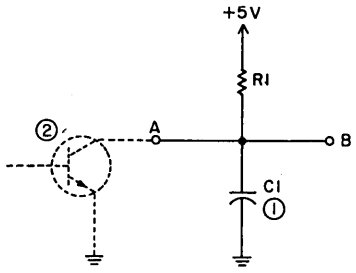
If a "1" (+3.0 V) enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7 V) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.

Characteristics of the UC-circuits are as follows:

Circuit Type	Capacitance	Resistance	Delay
UCM	5600PF	1.2K	1.5US
UCP	5600PF	560	0.8US
UCR	5600PF	1K	1.3US
UCS	3.3UF	2.2K	1MS
UCV	270PF	2.61K	175NS
UCY	200PF	10K	200NS







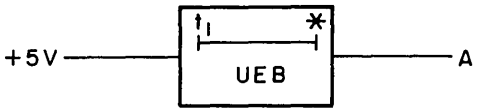
NOTES:
① DELAY TIME DEPENDENT ON CIRCUIT TYPE.
② OPEN COLLECTOR TRANSISTOR IN PRECEDING STAGE.

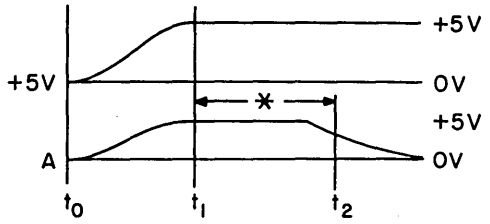
UC-
Rev B
Sheet 1 of 1

Delay - UEB

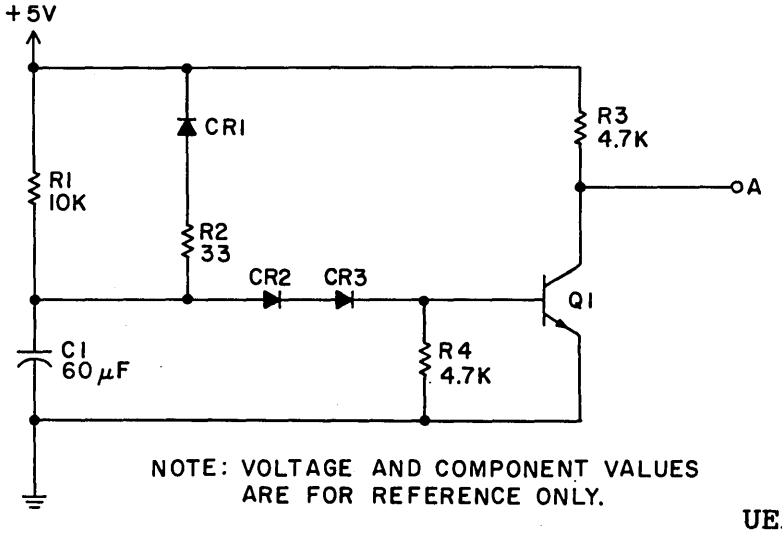
The UEB circuit delays application of ground to a standard TTL gate during a power-up sequence.

During power off phase (T_0), capacitor C1 is discharges by R4, CR2, and CR3. Applying +5 V power (T_1) raises output A to +5 V as power comes up. At this time (T_1) Q1 is off and C1 is charging. As the voltage across C1 approaches 5 volts, Q1 turns (T_2) on reducing output A to about 0 volts.





* DELAY TIME VARIES WITH COMPONENT VALUES, SEE LOGIC DIAGRAMS FOR SPECIFIC DELAY TIME.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

UEB
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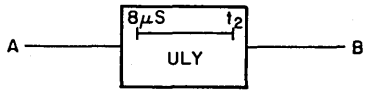
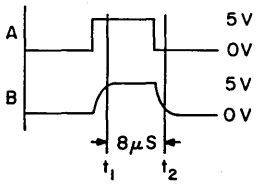
Delay - ULY

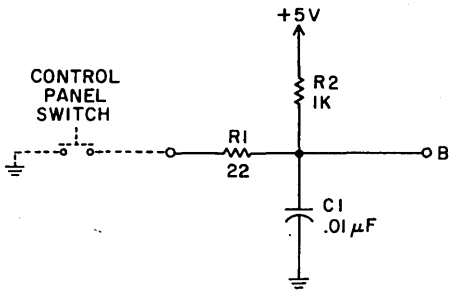
The ULY-delay circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5 V, a capacitor connected to ground, and a series input resistor.

Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

If an open circuit ("1") enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7 V) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

ULY
Rev A
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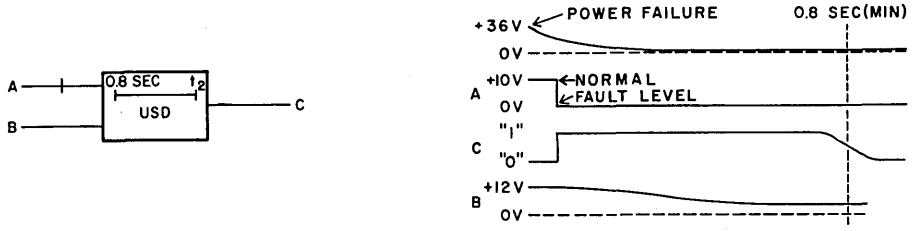
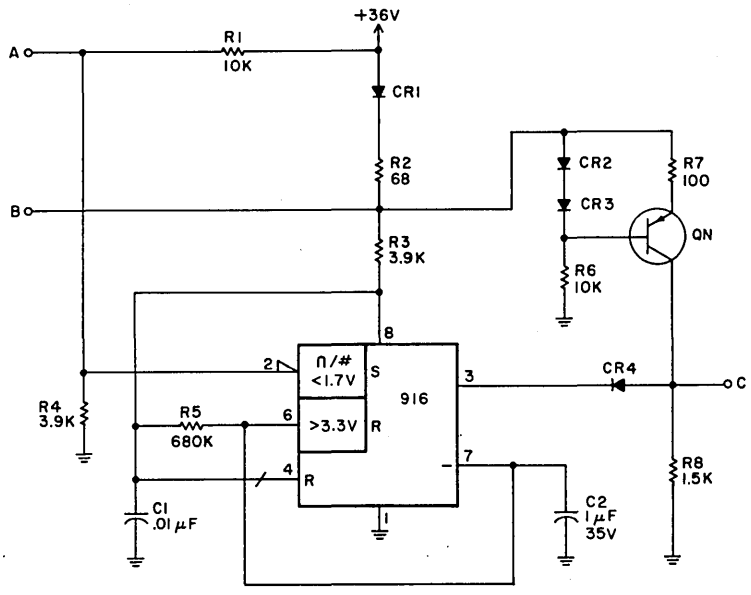
Delay - USD

The USD circuit maintains a TTL high level output for 0.8 second during the time that the power supply voltage is dropping.

The USD circuit functions as the delay portion of a write fault clamp circuit which prevents write current from reaching the head during a +36 V supply voltage fault condition. The switching action of transistor QN is initiated by the fault trigger at input A. QN is turned on when input A goes to 0 V, causing output C to go high. Resistor R5 and capacitor C2 provide the time-out constant to keep output C high for 0.8 second. Stored energy is supplied at input B to maintain QN in the on state for the 0.8 second duration. The high output at C is used to switch on a write clamp circuit.





NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

USD
Rev B
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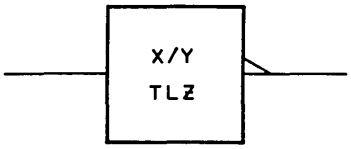
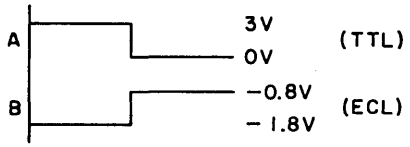
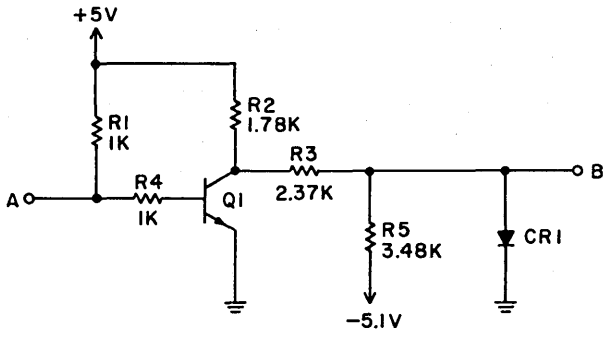
Inverting Translator (TTL To ECL) - TLZ

The first part, consisting of R_1, R_4, and Q_1 form a sim- ple transistor inverter to turn TTL "1's" into TTL "0's". The second part, R_2, R_3, R_5, and CR_1, form a LLZ passive translator which produces ECL levels from TTL inputs.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

TLZ
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Sheet 1 of 1

Circuit functional description will be included in a later revis
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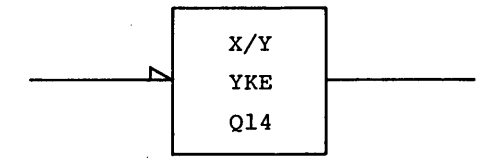

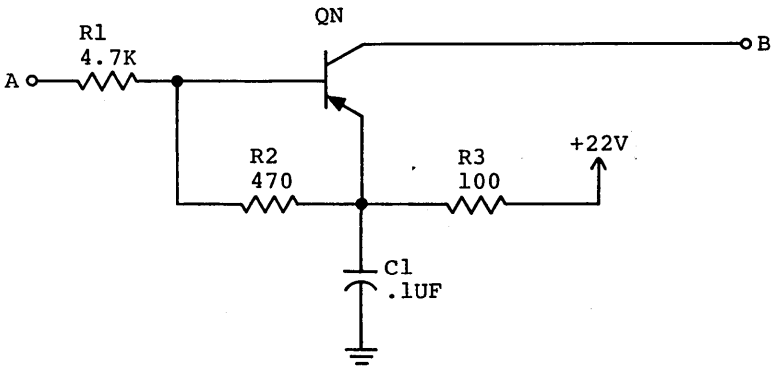

YKE
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Sheet 1 of 1

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