PRODUCT SPECIFICATION

FOR THE

MINI-MODULE DRIVE FAMILY

9730-12	9730-12F
9730-24	9730-24F
9730-80	9730-80F

RESPONSIBLE ORGANIZATION	ORIGINATOR	UNIT MANAGER	SECTION MANAGER	DEPARTMENT MANAGER
PRODUCT MANAGEMENT				7/11
OEM ENGINEERING		6/28/77		
DISK DRIVE DEVELOPMENT				6/15/77
CONTROLLER DEVELOPMENT				
DISK SYSTEM DEVELOPMENT				
SOFTWARE DEVELOPMENT				
MEDIA DEVELOPMENT			7-1-77	
HEAD DEVELOPMENT				7/1/77
CIRCUIT DESIGN			6/27/77	

TABLE OF CONTENTS

ILLUSTRATIONS

9730 MINI-MODULE DRIVES

1.0 SCOPE

This document describes the MAGNETIC PERIPHERALS, INC. 9730 Mini-Module Drive (MMD) and its available configurations.

2.0 APPLICABLE DOCUMENTS

DWG 73020700 - MMD Mechanical Interface
PUBL 83322720 - Maintenance Manual
PUBL 83322730 - Reference Manual
UL 478 - Electronic Data-Processing Units and System (60 Hz Units)

3.0 GENERAL DESCRIPTION

3.1 Equipment Definition

The MMD is a 3600 rpm, 9.677 MHz data rate, random-access, fixed-media device consisting of a drive motor and brake, power supply; electronic printed circuit boards with read/write, fault, transmitter/receiver electronics; a disk module containing disk, heads, actuator, and air filters, sealed to minimize the effects of environmental contamination, contained within a metal enclosure (see Figures 1, 2 and 32). Several features to enhance system integrity are included. They are phase-locked data separation, NRZ-to-MFM data conversion, variable sector (address mark), and daisy-chain interface capability. Various electrical and mechanical options are available to the user to select the optimum configuration. The MMD is designed to be rack mounted in either domestic or European enclosures (see Figure 3). There are three basic models:

a. 9730-12

A one disk model containing two data heads and one servo head. This model has 320 cylinders with an unsectored capacity of 12.9 megabytes.

b. 9730-24

A two disk model containing four data heads (on two surfaces) and one servo head. This model has 320 cylinders with an unsectored capacity of 25.8 megabytes.

c. 9730-80

A four disk model containing ten data heads (on five surfaces) and one servo head. This model has 823 cylinders with an unsectored capacity of 82.9 megabytes. This model addresses heads and cylinders the same as the 80 megabyte SMD.

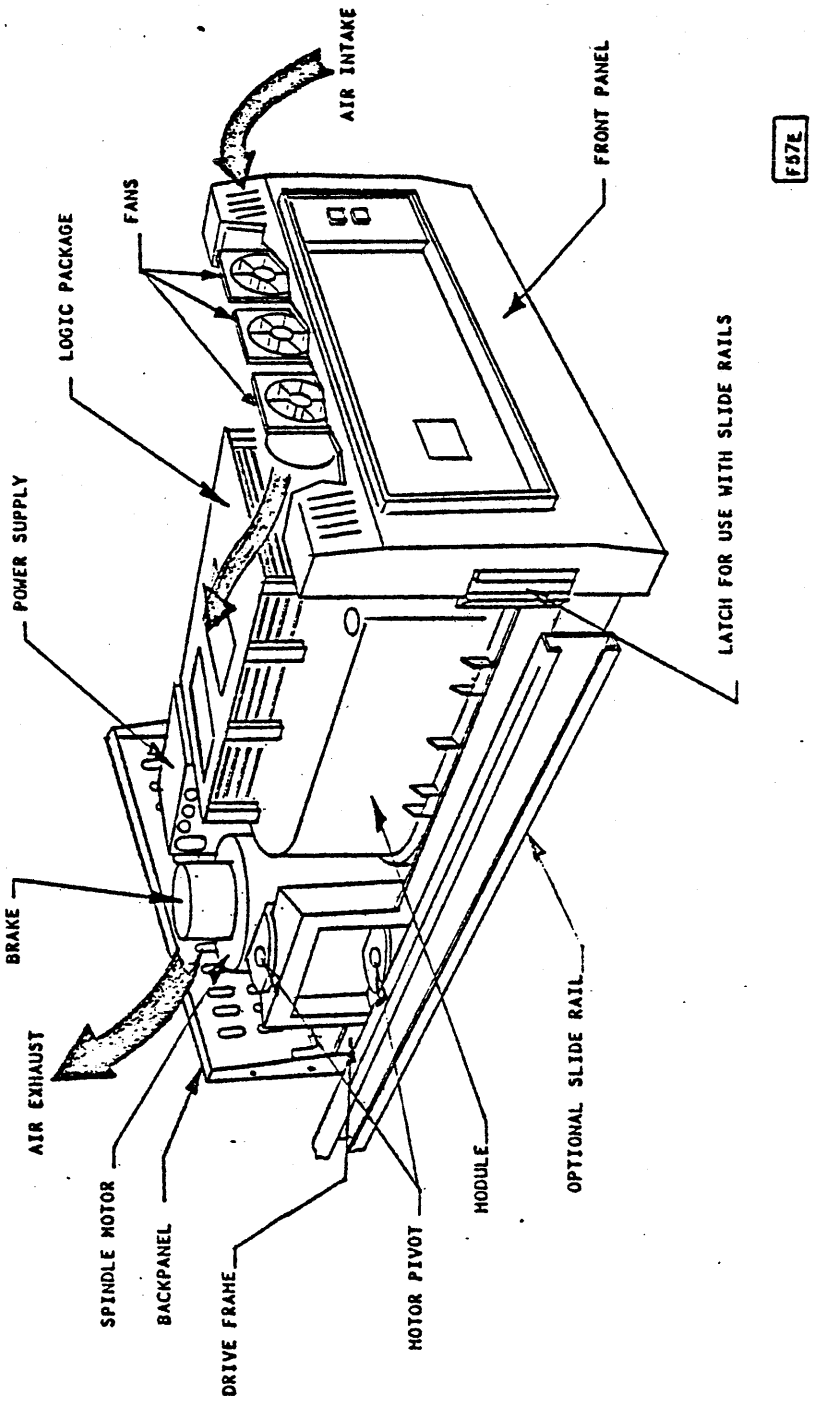
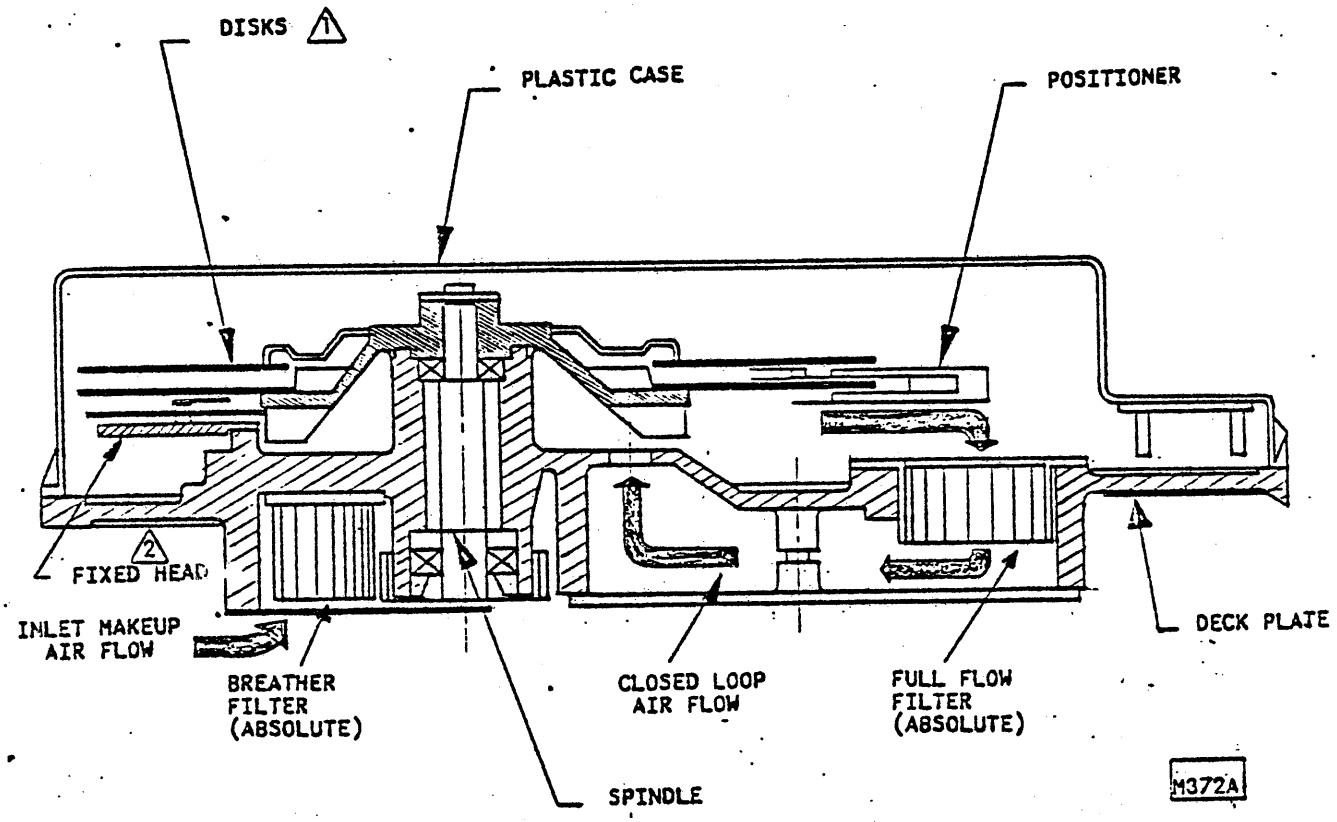


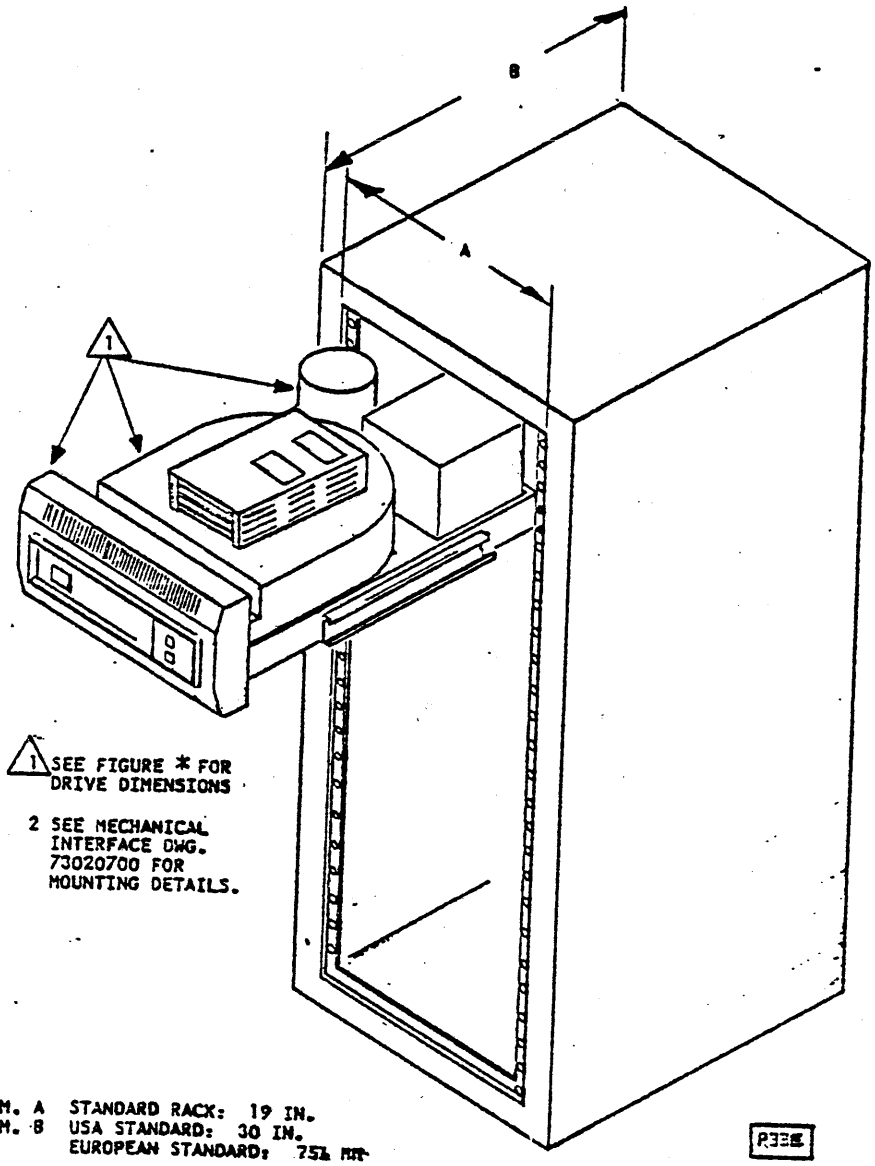
FIGURE 1. MAJOR COMPONENT PLACEMENT AND AIR FLOW



1 12 MB DRIVE MODULE CONTAINS ONLY ONE DISK.
24 MB DRIVE MODULE SHOWN.
80 MB MODULE CONTAINS FOUR DISKS.

2 FIXED HEAD OPTION ONLY

FIGURE 2. MODULE COMPONENT PLACEMENT AND AIR FLOW



* Figure 32

FIGURE 3. SLIDE MOUNT OPTIONS FOR RACK OR CABINET INSTALLATION

3.1.1 Paint Configuration

See Figure 4.

ITEM	DESCRIPTION	STANDARD COLOR
1	Inserted Panel	Black
2	Front Panel	Off-White
3	Product Identification Emblem	CDC
4	Switch/Indicator Frame	Black
5	Switch/Indicator Buttons	White
6	Latch Handle	Black

TABLE 1. COLOR STYLING DETAILS

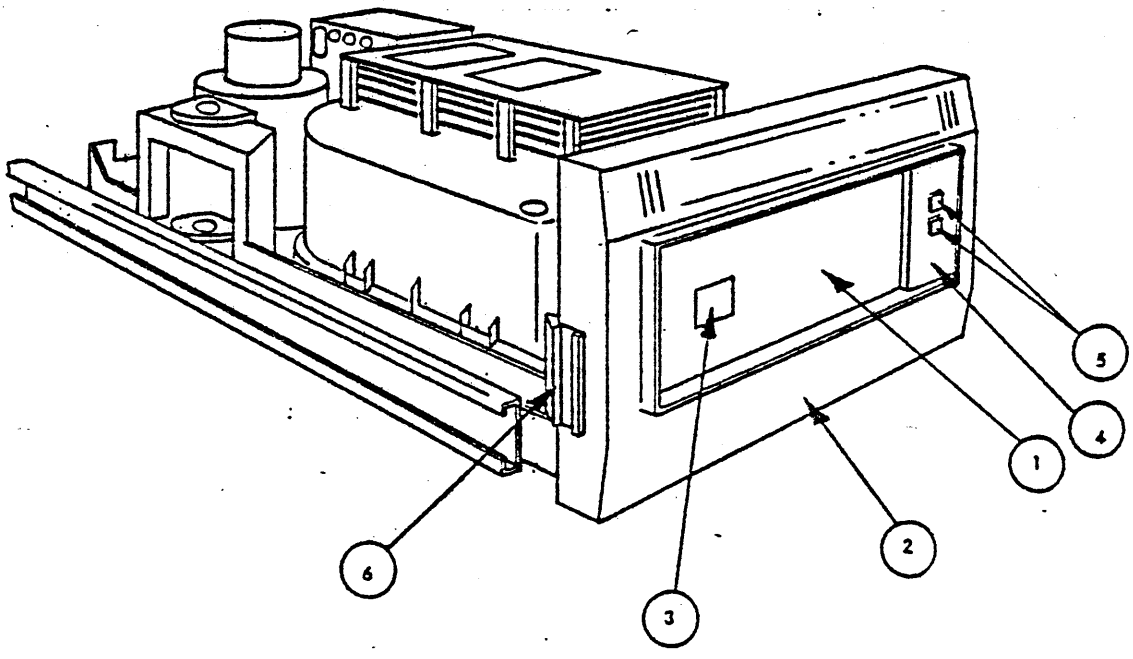


FIGURE 4. PAINT CONFIGURATION

3.2 Options and Variations

3.2.1 9730-12F, 9730-24F, 9730-80F Fixed Head Models

All models have the capability of being configured with a fixed head assembly which contains 48 heads and adds 967 680 bytes of unsectored capacity to the moving head configuration. As an alternate, the 9730-80 may be configured with a fixed head assembly which contains 96 heads and adds 1 935 360 bytes of unsectored capacity to the moving head configuration. This feature permits high speed head-per-track access, 8.3 ms average latency. The option is incorporated into the MMD by replacing the module assembly and is available as either a factory or field installed option. {See 6.4 for interface details, and Figure 7 for head configuration.}

3.2.2 Dual Channel

This feature permits two controllers to have access to the same device. The device is shared in the sense that either controller can select and reserve the MMD for that controller. The device then becomes busy to the other controller if it attempts to gain access. Release of the device by the controller is accomplished by issuing a release command, allowing the release timer to time out or the opposite controller can issue a priority select. {See 6.2 for interface details.}

All models are factory prewired for dual channel so that this feature can be factory or field installed by the addition of logic cards only.

3.2.3 Power {See 10.1.1}

The MMD will accommodate the following line voltages and frequencies:

60 HZ	50 HZ
120 Vac	220 Vac
	240 Vac

Field options are available for converting between power configurations. The 50 Hz units are shipped wired for 220 Vac and can be converted to 240 Vac operation by changing tap on transformer.

3.2.4 Rack Mount Slides

Rack mount slides are available as shown in Figure 1.

3.2.5 Index and Sector in "B" Cable Option

An option is available that places the index and sector pulses on the "B" Cable. See Figure 16.

3.3 Accessories

Accessory items that are required but not furnished with the units are shown in Table 2. Various cable lengths are shown in Table 3. These items must be purchased separately.

Description	Quantity Required	Note	Part No.
"A" Cable (Controller to MMD)	One per MMD in star, one per multi-spindle installation in Daisy Chain	2,4	775642XX
"A" Cable (MMD to MMD)	One less than total MMD in the system	1,2,4	775642XX
"B" Cable (Controller to MMD)	One per MMD	4	775643XX
Terminator	One per MMD in star, one per multi-spindle installation in Daisy Chain	4	75841300
T83048 Field Exerciser		3,5	77449301
T8304C Field Exerciser		3	77449302

1. Multiple, number of cables required depends on number of units in daisy chain.
2. Last two digits denote length. (For cable length see Table 3.)
3. Quantity as required for regional maintenence.
4. In systems using the dual channel operation, twice the number of cables and terminators are required.
5. With head alignment features.

The above accessories are required but not included with the units; they must be purchased separately.

TABLE 2. ACCESSORIES LIST

PART NO. TAB	Cable Length In Feet 5	6	8	10	15	20	25	30	40	50
"A" Cable 775642XX	00	01	02	03	04	05	06	07	08	09
"B" Cable 775643XX	00	01	02	03	04	05	06	07	08	09

TABLE 3. I/O CABLE LENGTH AND TABS

3.4 Major Components

3.4.1 Logic Assembly

The standard logic building blocks are dual-in-line, low power Schottky integrated circuits. The logic is packaged on modular removeable printed circuit boards which are housed in a logic chassis and mounted on the top of the MMD module. The cards are interconnected by a wire wrapped back plane and the I/O cables attach to the out board edge of the I/O cards.

3.4.2 Module

The MMD module is a sealed assembly that consists of a deck plate, spindle, disks, heads, positioner and closed loop air system. For component placement and air flow see Figure 2.

3.4.2.1 Positioner

Head positioning is performed by a closed loop servo system. The heads are driven by a voice coil rotary actuator with position feedback provided from the disk servo surface.

3.4.2.2 Disks

The MMD utilizes a coated, oriented magnetic oxide disk for the recording media. The surface is lubricated to allow the heads to start and stop in contact with the disk.

3.4.2.3 Heads

Low mass, lightly loaded heads are utilized to allow start/stop contact operation and low flying heights.

3.4.2.4 Closed Loop Air System

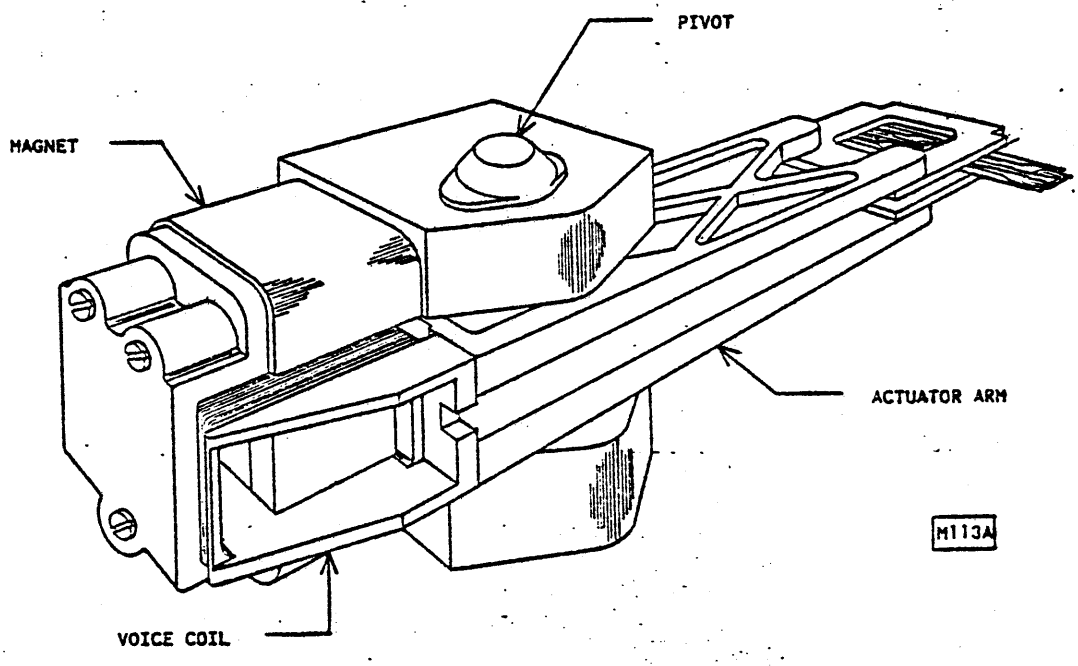
A closed-loop system ensures continuous circulation of filtered air through the head and disk area. The air within the sealed module is isolated from the external environment with the exception of a small amount of filtered make-up air to allow for pressure differential (see Figure 2).

3.4.3 Drive Frame and Spindle Motor

A rigid cast aluminum deck, 1/6 hp (1/2 hp for 80 MB) spindle motor and spindle preserve the dimensional and speed integrity necessary to the recording system. The module spindle is belt driven by the spindle motor.

3.4.4 Open Cooling Air System

Fans located in the front of the unit provide coarse filtered air to the device for cooling of the logic chassis, power supply and spindle motor (see Figure 1).



NOTE: 12 MB MODEL SHOWN

FIGURE 5. ACTUATOR ASSEMBLY (POSITIONER)

4.0 PERFORMANCE

4.1 Access-To-Data Characteristics

4.1.1 Positioning Times

All positioning times are measured from initiating a seek to the On Cylinder condition.

The maximum positioning time is 65 ms for 12/24 MB, 55 ms for 80 MB. This is defined as the time to move the heads from track 0 to track 319 (0 to 822 for 80 MB).

The maximum single track positioning time is 10 ms for 12/24 MB, 7 ms for 80 MB. This is defined as the time to move between any pair of adjacent tracks.

The average positioning time is 40 ms maximum (30 ms for 80 MB). This is defined as the time taken to make all possible moves divided by the number of all possible moves. (See Figure 6 for maximum seek time profile.)

4.1.2 Latency Time

The average latency time is 8.33 ms, based on a nominal disk speed of 3600 rpm.

The maximum latency time is 17.3 ms, based on a minimum disk speed of 3474 rpm (3600 -3.5%).

Latency time is defined as the time required to reach a particular location on a track after positioning is complete.

4.1.3 Read Initialization Time

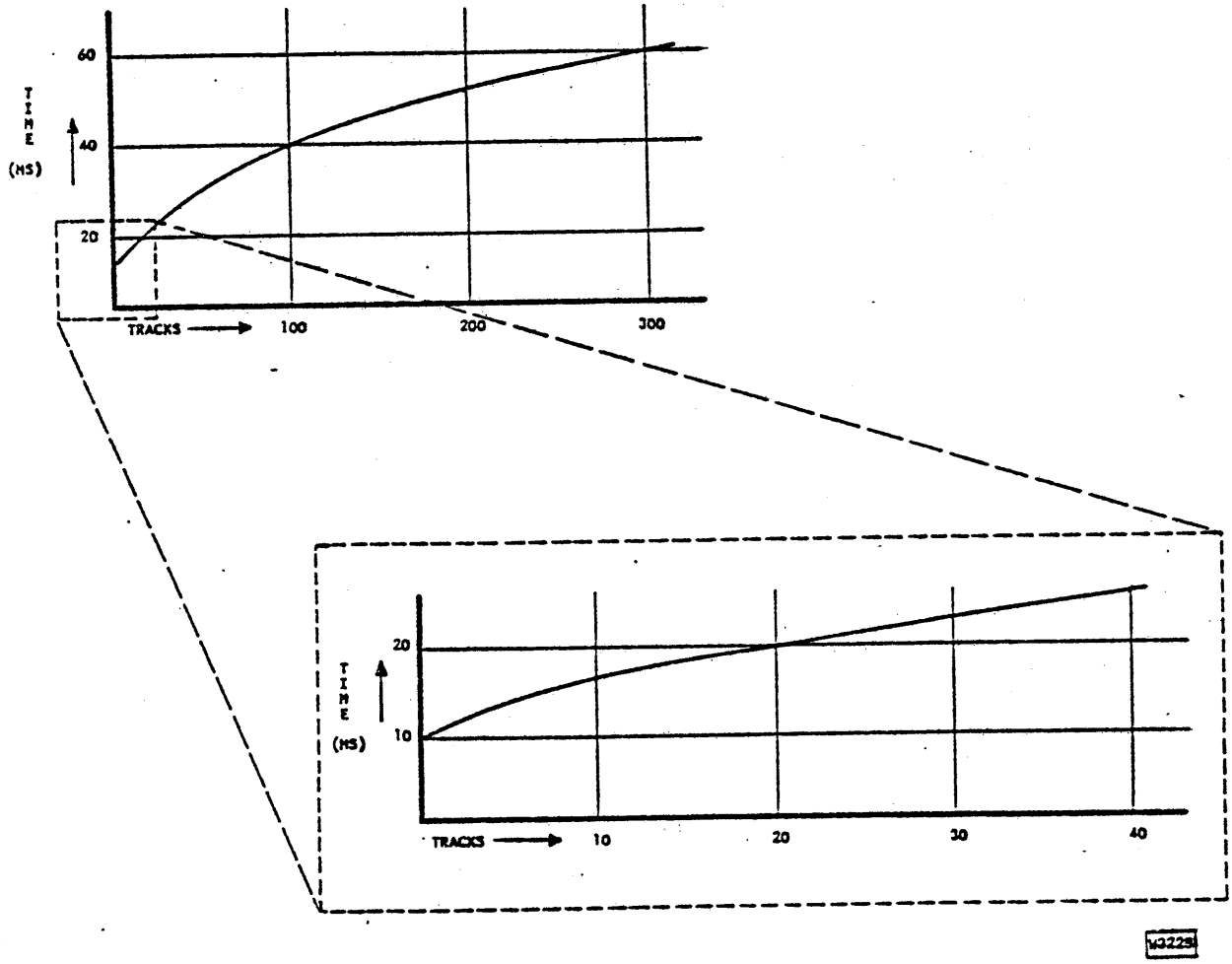
Between the deselection of one head and the selection of another head, there is a 5.0 µs delay within the MMD due to circuit characteristics. The time from the initiation of a head change until data can be read with a selected head without error, shall be 24.0 µs, maximum (5.0 µs for head selection, 10 µs for read amplifier stabilization, and an additional 9 µs to complete phase lock synchronization).

4.1.4 Write-to-Read Recovery Time

Assuming head selection is stabilized, the time lapse before read gate can be enabled after switching the write gate off is 10 µs, minimum (Figure 26).

4.1.5 Read-To-Write Recovery Time

Assuming head selection is stabilized, the time lapse from dropping read gate to enabling write gate shall be 0.3 µs, minimum (Figure 26).



NOTE: SEEK PROFILE FOR THE 80 MB UNIT WILL BE SUPPLIED.

FIGURE 6. MMD MAXIMUM SEEK PROFILE

4.2 Data Capacity

The data capacity specified is based on the number of bits that are recorded on a track. The unsectored capacity below does not include an allowance for tolerance gaps.

Data Capacity - Unsectored	Moveable Heads 12 MB	Moveable Heads 24 MB	Moveable Heads 80 MB	Fixed Heads (Optional)	Fixed Heads (Optional)
Heads	2	4	5	48	96 ⚠1
Bytes/Track	20 160	20 160	20 160	20 160	20 160 ⚠1
Bytes/Cylinder	40 320	80 640	100 800	*	*
Cylinders/Spindle	320	320	823	*	*
Bytes/Spindle	12 902 400	25 804 800	82 958 400	967 680	1 935 360

See 6.4 for head/cylinder addressing characterics.

⚠1 APPLIES TO 80 MB ONLY.

4.3 Data Transfer Rate

Nominal bit rate: 9.677 MHz.

4.4 Error Rate

The following error rates assume that the MMD is being operated within this specification. Errors caused by media defects or equipment failures are excluded.

4.4.1 Read Errors

Prior to determination of a read error rate, the data shall have been verified as written correctly and all media defects flagged.

a. Recoverable Error Rate - 1 in 10^{10}

The recoverable error rate is the number of errors encountered which are recoverable within three retries as a function of the number of bits transferred.

b. Unrecoverable Error Rate

An unrecoverable read error is one which cannot be read correctly within 9 retries (three retries at each data strobe setting).

Unrecoverable read errors shall be considered as failures affecting MTBF.

4.4.2 Write Errors

Write errors can occur as a result of the following: write data not being presented correctly, media defects, or equipment malfunction. As such, write errors are not predictable as a function of the number of bits passed.

For the case of an unrecoverable write error occurring because of a MMD equipment malfunction, the error is classified as a failure affecting MTBF.

Unrecoverable write errors are those which cannot be corrected within three attempts at writing the record with a read verify after each attempt.

4.4.3 Environmental Errors

When operating at low effective data transfer rate; e.g., random access of single short records, the effective error rate may be expected to exceed the above limits due to external environmental interference. The resulting recoverable read error rate shall be less than one error in eight hours of operation.

4.4.4 Media Errors

The media utilized in the MMD has been certified under the assumption that the user has implemented error correction code (ECC) techniques and/or bad spot mapping methods for proper handling of media flaws.

Media flaws are characterized as correctable and uncorrectable errors. A correctable error is one being equal to or less than 11 bits in length and not exceeding one error of this type per track. An uncorrectable error is one greater than 11 bits in length or two or more correctable errors per track.

The allowable media error criteria for the MMD is:

a. No errors of either type at cylinder 000, head 00 and 01. (Also Heads 02 and 03 on 9730-24).

b. No errors of either type for 200 bytes following index on all tracks.

c. No errors of either type for all fixed head tracks.

d. Maximum correctable errors per drive will not exceed:

9730-12	6
9730-24	12
9730-80	30

e. There are no uncorrectable errors.

4.5 Data Security

Under no circumstance of normal Controller I/O operation is it possible to write a pattern not corresponding to that on the write data lines. It is possible to alter the bit pattern only when the MMD signifies an On-Cylinder Status, and then only upon specific MMD selection. Data is protected by inhibiting Write Gate in all fault conditions including a loss of On Cylinder, or low voltage. Under any of the following conditions, an emergency retract of the heads is performed so that data is protected either by the above mentioned fault condition, or by switching off the voltage required to write. These conditions are:

a. Loss of ac line power.
b. Loss of speed.
c. Loss of a power supply voltages.

4.6 Start Time

The time for the MMD to be in the Ready state after power has been turned on is 30 seconds.

4.7 Access Errors

There shall be no more than one positioning error in 10^6 seeks.

5.0 RECORDING CHARACTERISTICS

5.1 Recording

	12 MB	24 MB	80 MB
Mode: MFM			
Nominal BPI Density (inner track, moving heads)	6131	6131	6417
Nominal BPI Density (inner track, fixed heads)	6409	6409	6409

5.2 Disks (Figure 7)

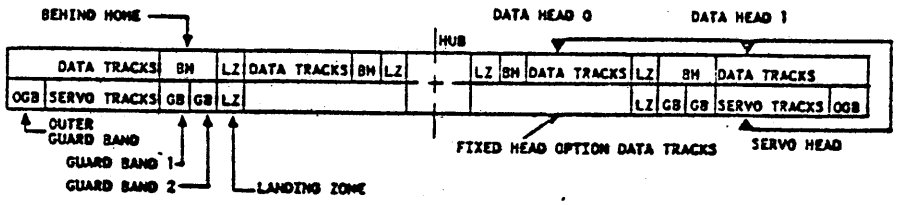
	12 MB	24 MB	80 MB
Total number:	1	2	4
Servo surface:	1	1	1
Total recording surfaces:	1	2	5
Active Tracks per surface:	640	640	822
Nominal disk diameter:	14 in.	14 in.	14 in.
Nominal track spacing:	0.00337 in.	0.00337 in.	0.00294 in.
Tracks per inch:	296	296	340

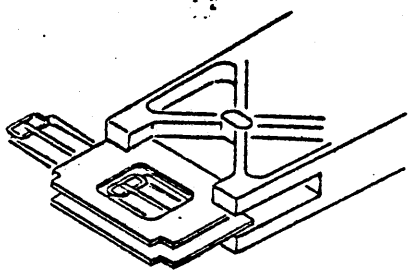
5.3 Heads (Figure 7)

Servo head:	1	1	1
Recording heads:	2	4	10
Read/Write width:	0.0023 in.	0.0023 in.	0.0020 in.

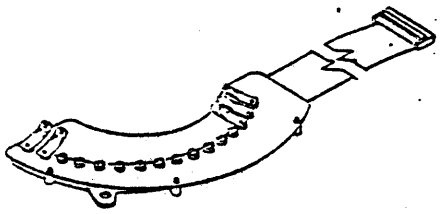
5.4 Spindle

The spindle speed is 3600 rpm (+2.5% -3.5%). The speed tolerance includes motor performance, pulley tolerances and the main power and frequency variations specified in 10.1.1.

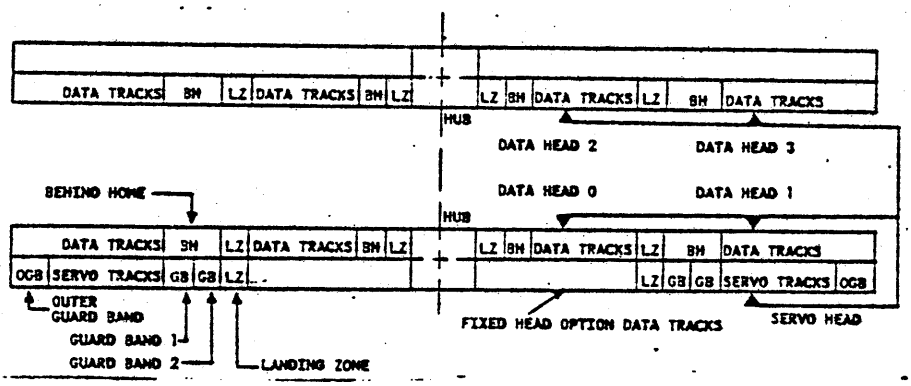


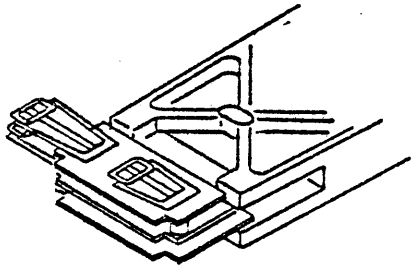


12 MB DISK FORMAT AND HEAD CONFIGURATION

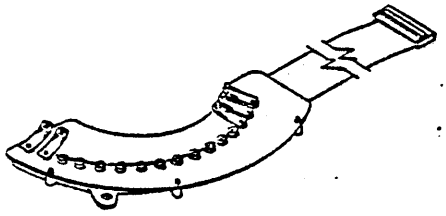


FIXED HEADS OPTION (48 HEADS)





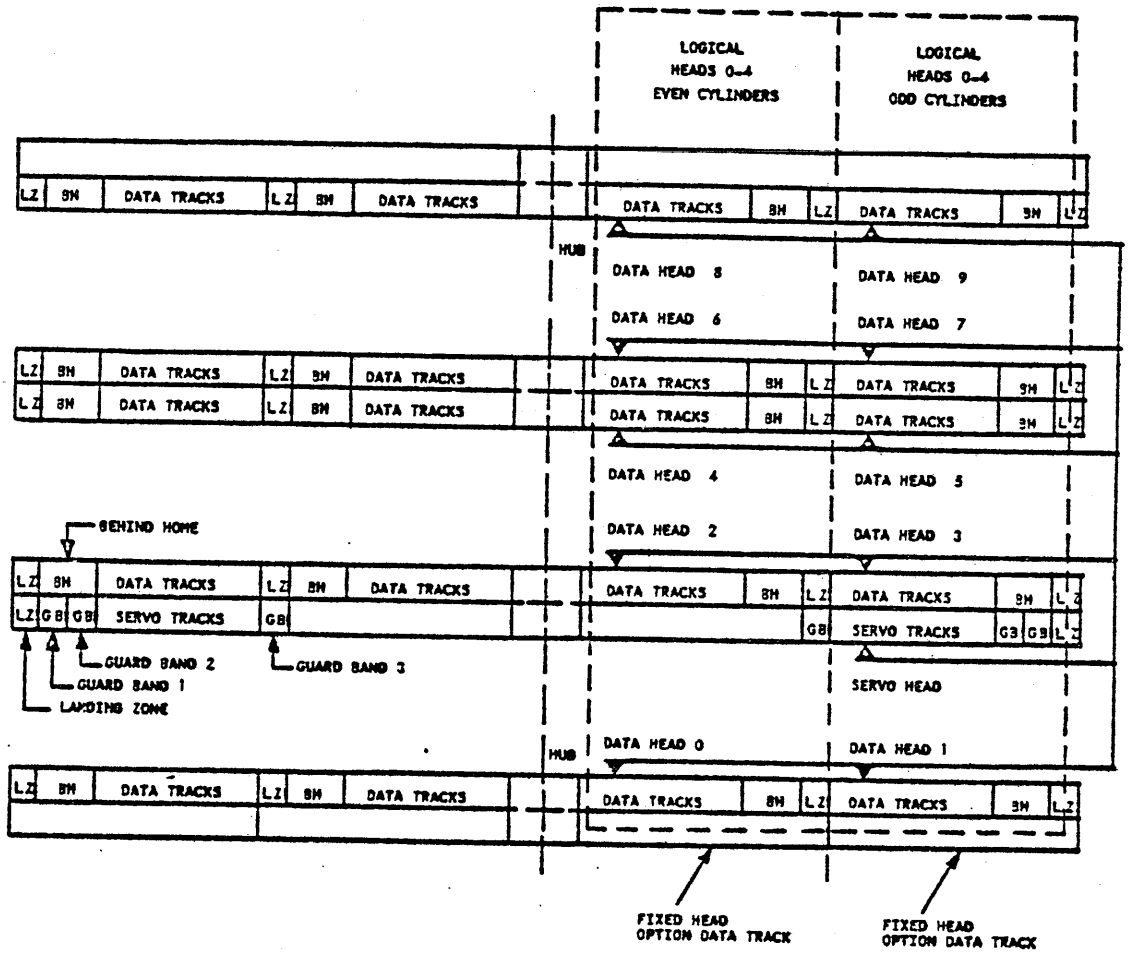
24 MB DISK FORMAT AND HEAD CONFIGURATION

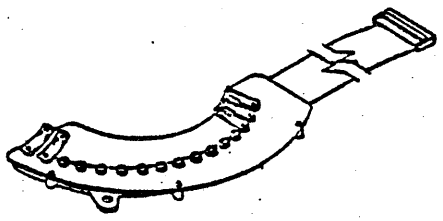


FIXED HEADS OPTION (48 HEADS)

H114C

FIGURE 7A. 12/24 HEAD CONFIGURATION





FIXED HEADS OPTION (48 HEADS)

TWO REQUIRED FOR 96 HEADS

M430A

FIGURE 7B. 80 MB HEAD CONFIGURATION

6.0 INTERFACE

6.1 Interface Definition

The Standard "A" cable I/O is 60 pin configuration. The Standard "B" cable is 26 pin configuration. (See Table 2 and 3 for I/O cables.)

All input and output signals are digital, utilizing industry standard transmitters and receivers to provide a terminated, balanced, transmission system for long distances and/or noisy electrical environment. Figure 8 is a block diagram of the MMD.

The "A" cable is a twisted-pair flat cable. The "B" cable is a ribbon flat-cable with ground plane and drain wire. Twisted-pair and/or ground plane shielding is utilized to minimize cross-talk and reduce inductive coupling due to static discharges, as well as control impedance variations regardless of cable lay.

6.1.1 Terminated, Balanced Transmission System

Transmitters and receivers of the industry standard type 75110A and 75108 or equivalent are used to provide a terminated, balanced transmission system (see Figure 9).

6.1.2 Line Transmitter Characteristics

The MMD Controller line transmitter (Figure 10) are compatible with the MPI line receiver described in 6.1.3.

1. Output Signal Levels

   Control Signals - See Figure 10.
   Data Signals - See Figure 9.

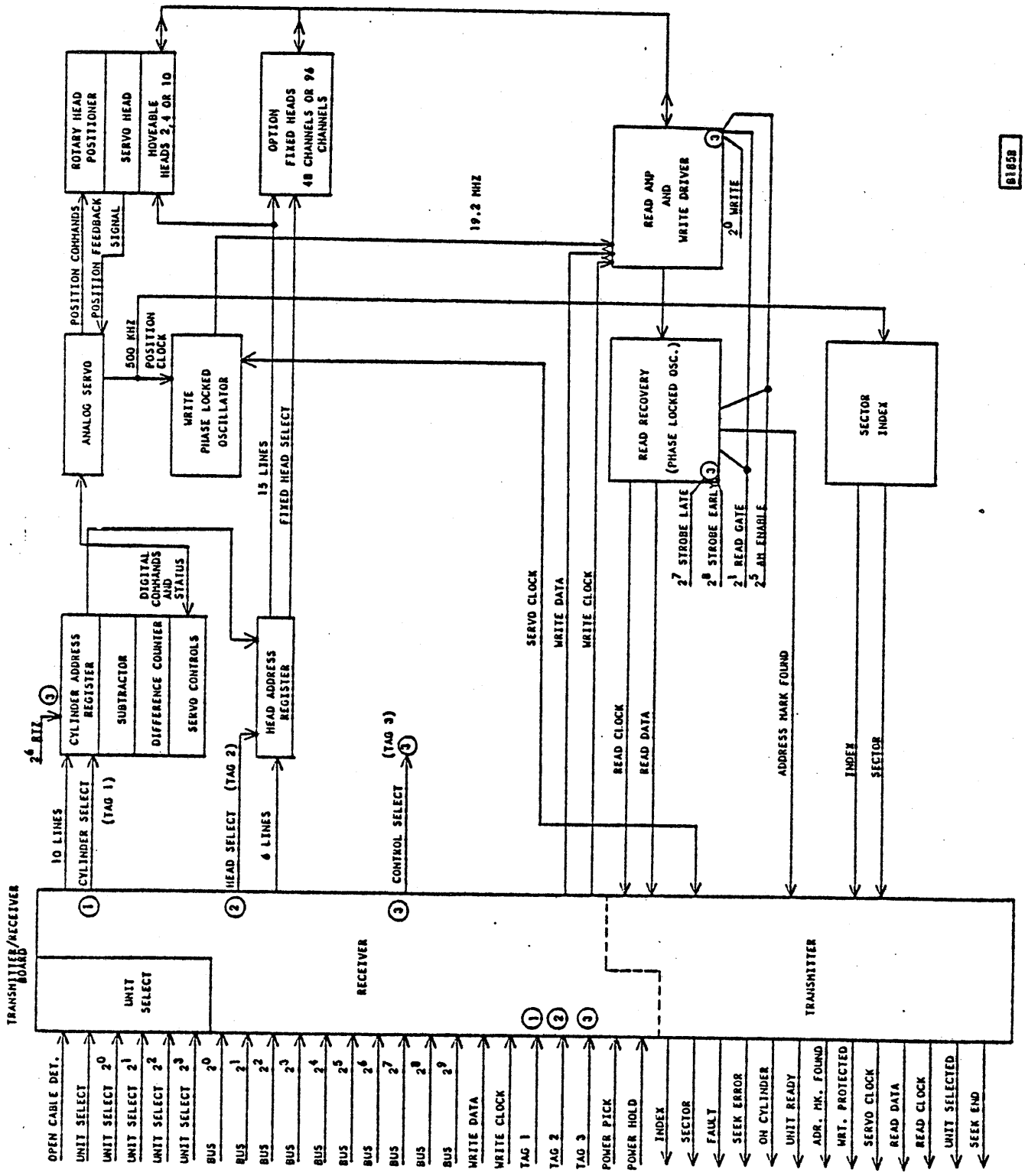
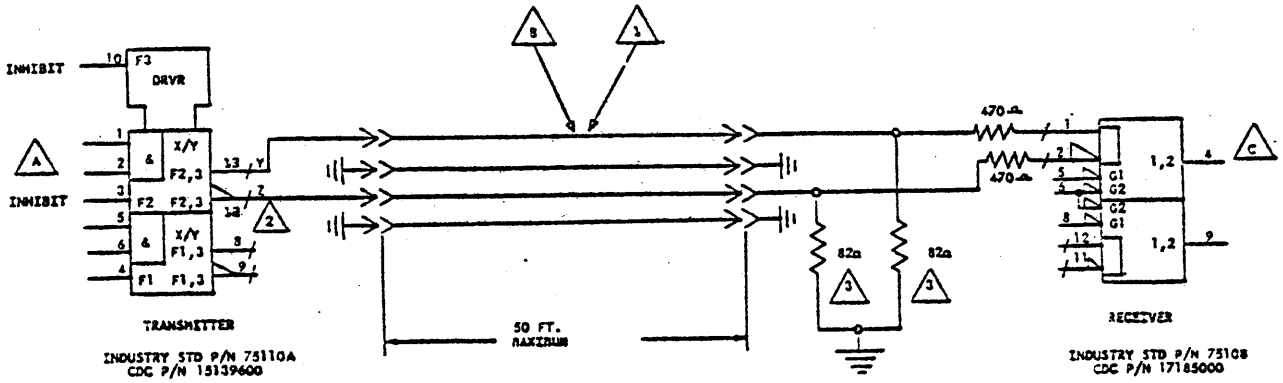
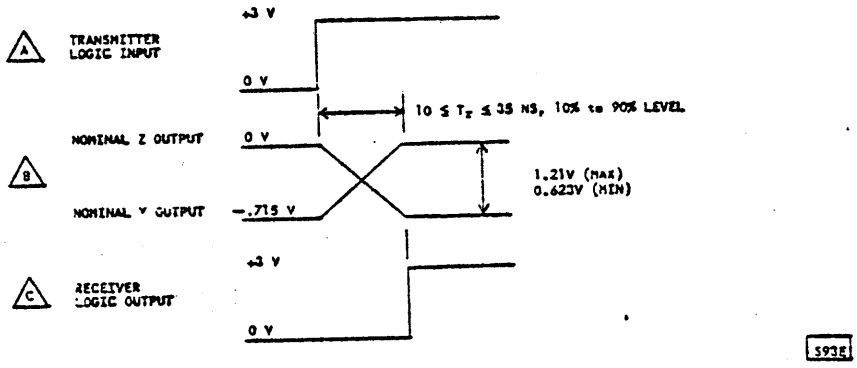


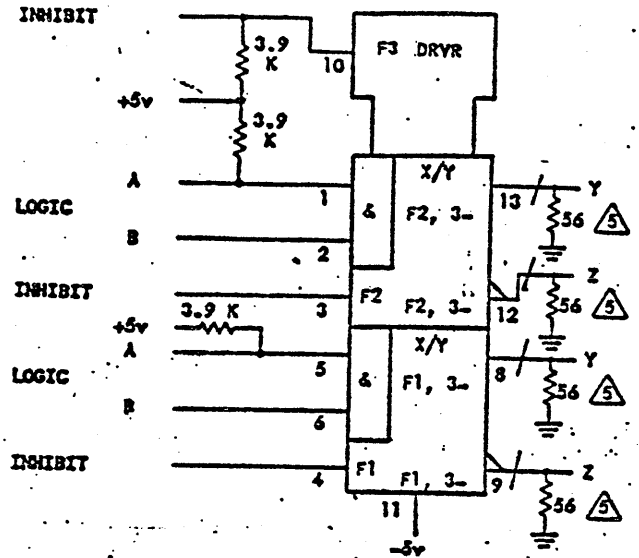
FIGURE 8. BLOCK DIAGRAM



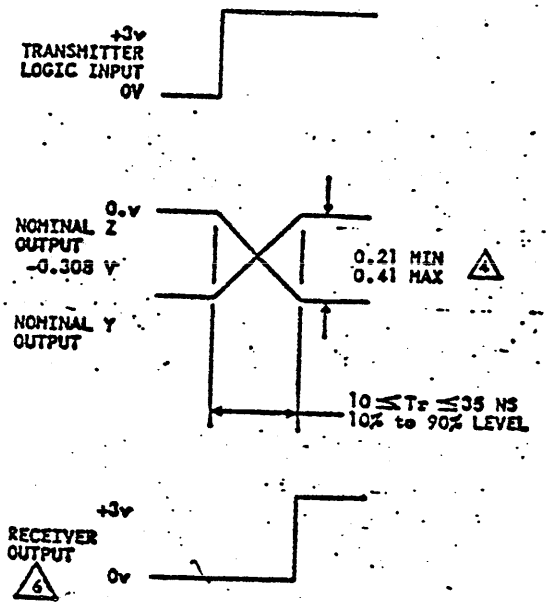


1. CABLE SHALL BE FLAT CABLE WITH CHARACTERISTIC IMPEDANCE 130 ±12 OHMS, CDC P/N 77564300 OR EQUIVALENT.
2. FOR LOGIC LEVELS AND TRUTH TABLE, REFER TO TRANSMITTER AND RECEIVER TEXT.
3. TERMINATOR RESISTORS ARE LOCATED ON DRIVE LOGIC CARD OR IN CONTROLLER. THESE SIGNALS MUST BE STAR CABLED.

FIGURE 9. TYPICAL READ/WRITE DATA AND CLOCK TRANSMITTER AND RECEIVER



TRANSMITTER CDC P/N 15139600
(INDUSTRY STD P/N 75110A)



LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS	
A	B	F2	F1	Y	Z
L or H	L or H	L	L or H	H	3
L or H	L or H	L or H	L	H	3
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

TRUTH TABLE

5116A

NOTES:

1. OUTPUT LEVELS - L = MOST NEGATIVE LEVEL
   H = LEAST NEGATIVE LEVEL
2. INPUT LEVELS - H = MOST POSITIVE LEVEL
   L = LEAST POSITIVE LEVEL
3. THIS IS AN INDETERMINATE INSTRUCTION WHEN SENSED BY AN ACTIVE (SELECTED) RECEIVER.
4. VOLTAGE RANGE INCLUDES TRANSMITTER OUTPUT SWING IN LOW STATE OF 11 ±3 MA, AND TERMINATING RESISTOR RANGE OF 56 ±5% OHMS.
5. TERMINATING RESISTORS ARE REQUIRED ON ALL "A" CABLE TRANSMITTERS. TRANSMITTERS IN THE DRIVE ARE TERMINATED BY THE TERMINATOR ASSEMBLY. REFER TO SINGLE AND DUAL CHANNEL INTERFACE ILLUSTRATION, AND THE TERMINATOR PARAGRAPH.
6. RECEIVER INPUTS A AND B ARE CONNECTED TO TRANSMITTER OUTPUTS Y AND Z RESPECTIVELY.

FIGURE 10. CONTROL LINE TRANSMITTER

2. Output Line Polarity

Control Signals - The MPI transmitter (Figure 10) shall be connected to the I/O line such that the output, labeled Z, shall correspond with the low order pin number of the pin assignments and in turn connect to receiver pin labeled B, except for the unit selected line which is connected in the opposite manner.

When transmitter and receiver are connected in this manner, a logical 1 into the transmitter produces a logical 1 out of the receiver, except for the unit selected line where a logical 1 into the transmitter produces a logical 0 out of the receiver.

6.1.3 Input Amplifier (Receiver) Characteristics

The MMD Controller input amplifier (Figure 11) is compatible with the MPI transmitter described in 6.1.2.

1. Receiver Propagation Delay

The receiver propagation delay shall typically be 17 ns in the direction of the logical 1, and 17 ns in the direction of the logical 0.

2. Receiver Input Polarity

Control Signals - The input (labeled "B") of the receiver (Figure 11) is connected to the lowest numbered pin of the pair in the cable and in turn connected to the transmitter pin labeled Z.

Data Signals - See Figure 9.

6.1.4 Terminator

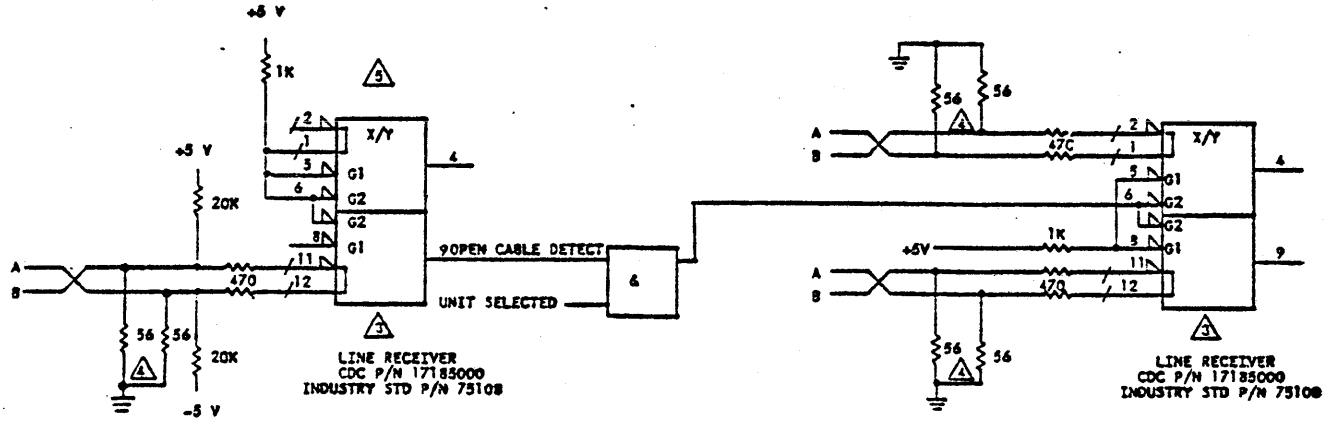
1. "A" Cable

A terminator resistance as shown in Figures 10 and 11 is required at the transmitter and receiver end of each transmission line of the "A" cable. This resistance is provided on the unit by the terminator assembly (see Table 2), which must be ordered separately (P/N 75841300).

A termination resistance is required at the controller end of each line of the "A" cable except for the Open Cable Detect line. See Paragraph 6.2.2-7. No termination resistance is used on the Power Sequence lines in the "A" cable.

2. "B" Cable

A termination resistance as shown in Figure 9 is required at the receiver end of each transmission line of the "B" cable. This resistance is provided at the unit's receiver logic card.



51068

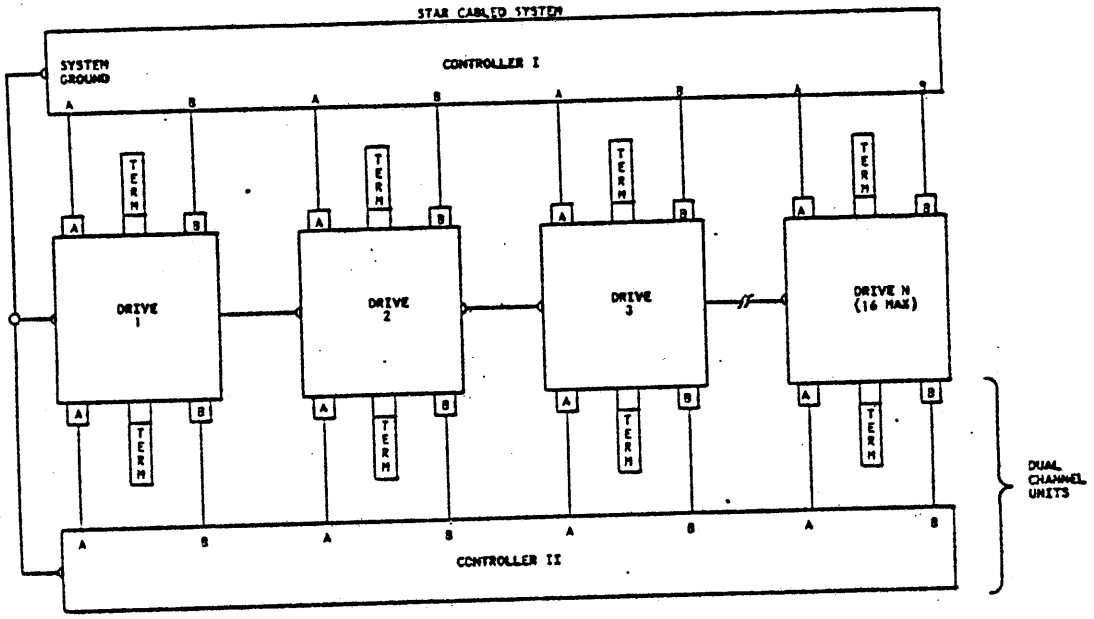
DIFFERENTIAL INPUTS	INHIBIT G1	INHIBIT G2	OUTPUT
$V_A - V_B \geq 25mv$	L or H	L or H	H
$\lvert V_A - V_B \rvert < 25mv$	L or H	L	H
	L	L or H	H
	H	H	IND.
$V_B - V_A \geq 25mv$	L or H	L	H
	L	L or H	H
	H	H	L

LINE RECEIVER TRUTH TABLE

NOTES:

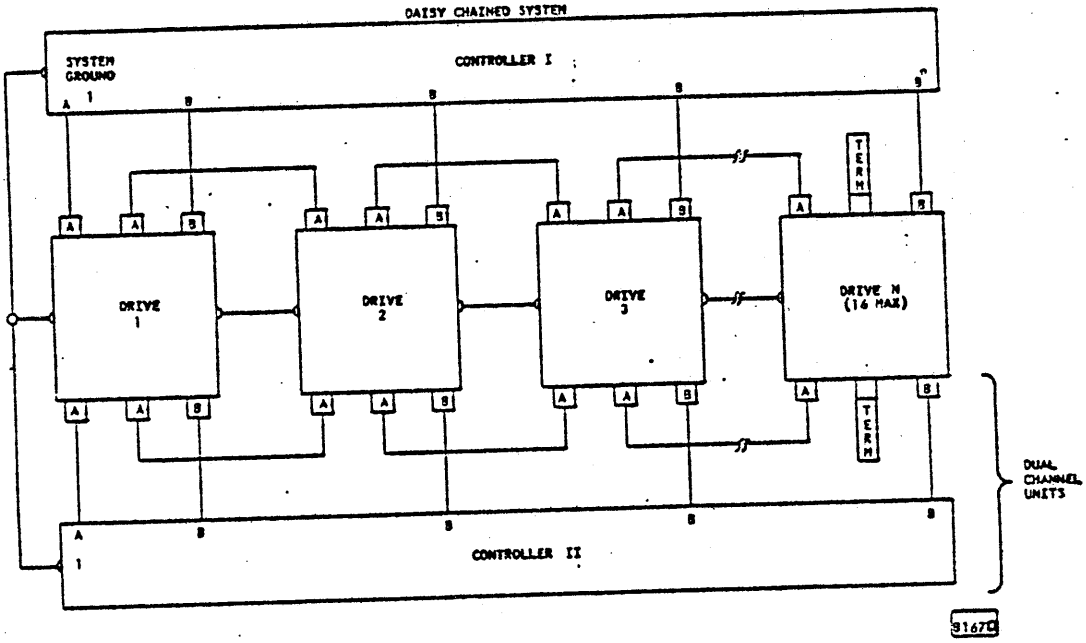
1. 20K OHM RESISTORS ARE TYPICAL VALUES.
2. ALL VALUES IN OHMS UNLESS INDICATED OTHERWISE.
3. A BIAS NETWORK SHOULD BE USED TO PREVENT FALSE STATUS OR INTERRUPT CONDITIONS WHEN DRIVE POWER IS OFF AT CONTROLLER END OF UNIT SELECTED AND SEEK END SIGNALS.
4. TERMINATING RESISTORS ARE LOCATED:
   A. ON LOGIC CARD FOR "9" CABLE LINES.
   B. IN SEPARATE TERMINATOR ASSEMBLY FOR "A" CABLE.
5. SEE 6.2.2.7 FOR DESCRIPTION OF OPEN CABLE DETECT SIGNAL.

FIGURE 11. CONTROL LINE RECEIVER



NOTES

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET



NOTES

1. TERMINATION OF "A" CABLE LINES ARE REQUIRED AT CONTROLLER AND THE LAST UNIT OF THE DAISY CHAIN OR EACH UNIT IN A STAR. SEE 6.1.4.1.
2. TERMINAT ON OF "B" CABLE RECEIVER LINES ARE REQUIRED AT THE CONTROLLER AND ARE ON THE UNIT'S RECEIVER-CARDS. SEE 6.1.4.2.
3. MAXIMUM CUMULATIVE A CABLE LENGTH PER CONTROLLER = 100 FEET .
   MAXIMUM INDIVIDUAL B CABLE LENGTH = 50 FEET.

FIGURE 12. UNIT CABLING

6.1.5 I/O Cables (See Figure 13)

6.1.5.1 "A" Cable

ITEM	DESCRIPTION	MPI P/N	BERG P/N	P/N SPECTRA-STRIP
1	Connector (60 Pos)	94361115	65043-007	
1.a	Contact, Insert	94245603	48048	-----
2	Flat Cable (twisted-pair), 30 pair, 28 AWG	95043902		3CT-6028-78-05-100

6.1.5.2 "A" Cable Mating Receptacle on Unit or Controller

ITEM	DESCRIPTION	MPI P/N	AMP P/N
1.a	60 pin, right angle header	94369804	3-86479-4
1.b	60 pin, vertical header	94385129	3-87227-0

6.1.5.3 "B" Cable

ITEM	DESCRIPTION	MPI P/N	3M P/N
1.a	Connector (26 pos.)	65853402	3399-3000
.b	Connector Pull Tab	92004801	3490-2
2.	Flat Cable (26 pos.) with ground plane and drain wire.	95028509	3476-26

6.1.5.4 "B" Cable Mating Receptacle on Unit or Controller

ITEM	DESCRIPTION	MPI P/N	AMP P/N
1.a	26 pin, right angle header	94369802	1-86479-0
1.b	26 pin, vertical header	94385106	1-87227-3

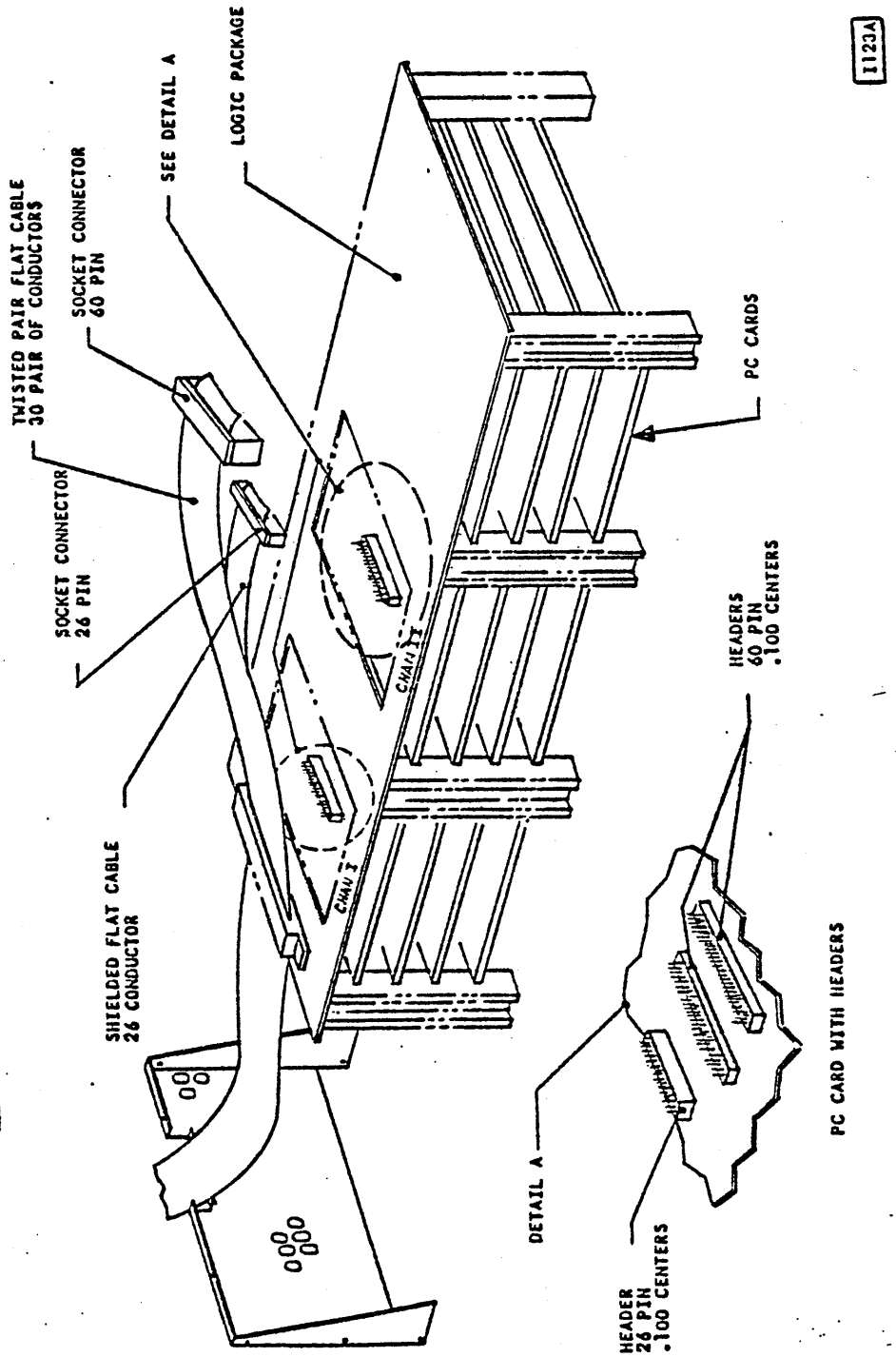


FIGURE 13. I/O CONNECTORS

6.1.6 I/O Cable Characteristics

"A" Cable

Type: 30 twisted pair, flat-cable
Twists per inch: 2
Impedance: 100 ±10 ohms
Wire size: 28 AWG, 7 strands
Propagation time: 1.6 to 1.8 ns/ft
Maximum cable length: 100 ft cumulative
Voltage Rating: 300 V rms

"B" Cable (with ground plane)

Type: 26 conductor, flat cable with ground plane and drain wire
Impedance: 130 ±15 ohms (3M P/N 3476-26)
Wire size: No. 28 AWG - 7 strands
Propagation velocity: 1.65 ns/ft (nominal)
Maximum cable length: 50 ft
Voltage Rating: 300 V rms

6.2 Signal Lines

6.2.1 Address and Control Tag Functions (received by the unit)

Address and control functions are transferred on 10 lines. The significance of the information on these lines is indicated by one of three tag lines (see Figures 14, 15 and 16).

6.2.1.1 Cylinder Address (Tag 1)

A. MMD Moving Head

Ten bus lines (Tag 1) are used to carry the cylinder address to the MMD. Since the MMD is a direct addressing device, the Controller need only place the new address on the lines and strobe the lines with Tag 1 (see Figure 17). The unit must be On Cylinder before Tag 1 is sent. The bus lines should be stable throughout the tag time.

B. MMD Fixed Head Tag and Bus

Transfer of cylinder and head address information is controlled by the same timing requirements as the moving head sequence which is defined in Figure 17. Because no positioner move is involved and it would be expected that a head select would immediately follow a cylinder select, the minimum Tag/Bus timing is as shown in Figure 28.

The fixed heads may be used to either read or write data while the moveable head positioner is in motion. The normal sequence of events would occur in the following order:

1. The controller issues a cylinder select with the desired moveable head cylinder location on the bus. "On Cylinder" and "Seek End" will drop.

2. The controller accesses the desired fixed head location with the appropriate cylinder select and head select signals.

3. Conforming to the specified times for head select to read or write, the controller can read or write on the fixed head memory. The absence of "On Cylinder" and "Seek End" will not cause a "Fault" in the unit when reading or writing on the fixed head shoe.

4. At the completion of the seek by the moveable head positioner, "On Cylinder" and "Seek End" will become true.

5. When the read or write operation is complete on the fixed head, the controller may readdress the moveable heads by sending the appropriate cylinder select (zero track seek) and head select signals. The cylinder select command is required in order to clear the fixed head mode.

6.2.1.2 Head Select (Tag 2)

This signal is the head address that will be selected by bits 0 through 2 (Figures 14 and 15).

6.2.1.3 Control Select (Tag 3)

This signal acts as an enable and must be true for the entire control operation.

1. Write Gate (Bit 0)

   The Write Gate line enables the write driver (Figure 15).

2. Read Gate (Bit 1)

   Enabling of the Read Gate (Figure 15), enables digital read data on the transmission lines. The leading edge of Read Gate triggers the read chain to syncronize on an all zeros pattern. (See Figure 18 for read gate and write splice relationship with Address Mark, and Figure 26 for Read Gate Timing with fixed sectors.)

3. Servo Offset Plus (Bit 2)

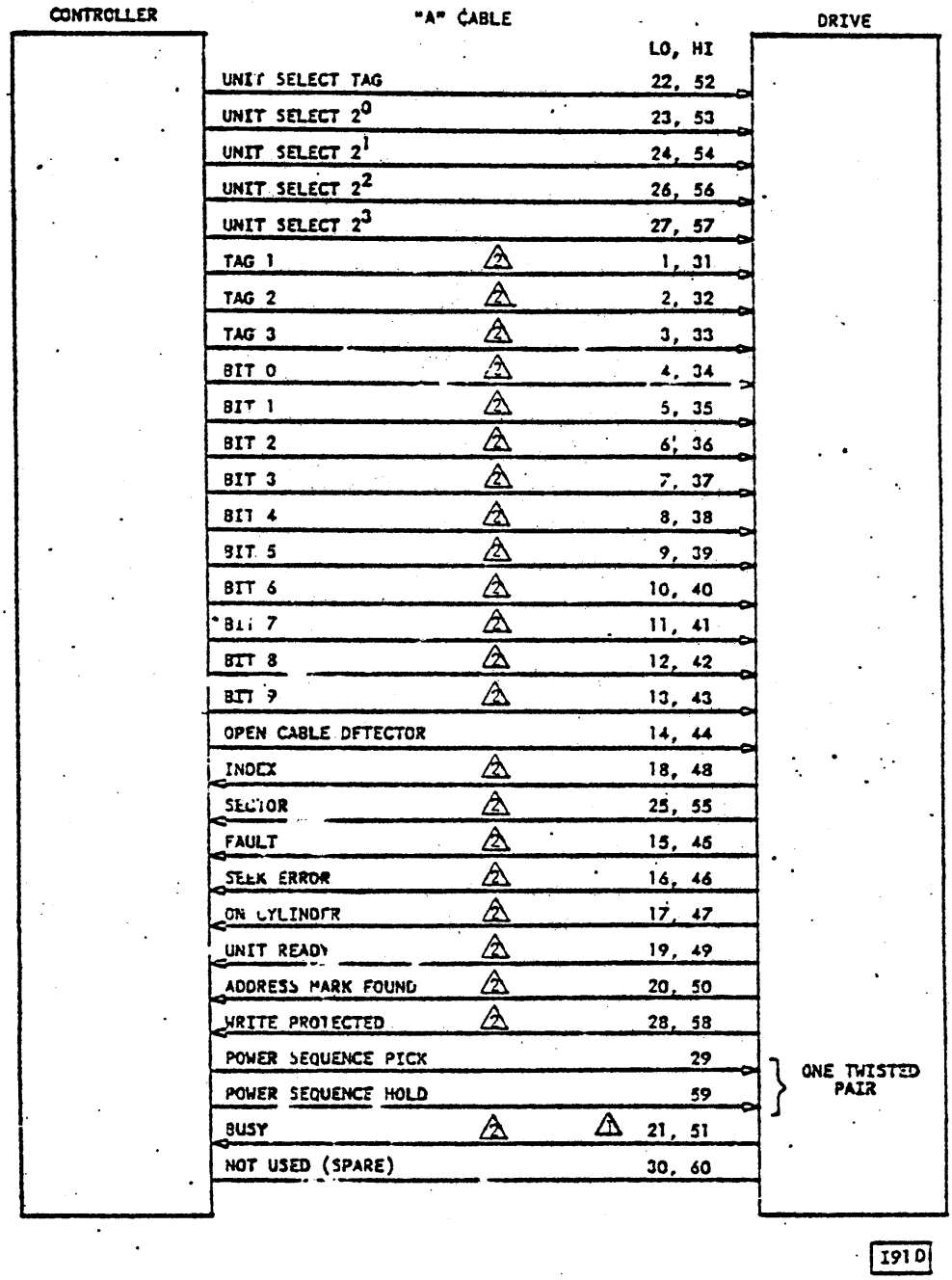
   When this signal is true, no physical movement of the heads is performed in the drive, used only to meet timing requirements of SMD Drive Family. (See Figure 17 for timing.)

4. Servo Offset Minus (Bit 3)

   When this signal is true, no physical movement of the heads is performed in the drive, used only to meet timing requirements of SMD Drive Family. (See Figure 17 for timing.)

5. Fault Clear (Bit 4)

   A pulse, 100 ns minimum, sent to the MMD will clear the fault flip-flop if the fault condition no longer exists.



NOTE: 60 POSITION
28 AWG, 30 PAIR, TWISTED-STRAIGHT FLAT CABLE
MAXIMUM LENGTH - 100 FT

1 DUAL CHANNEL UNITS ONLY.

2 GATED BY UNIT SELECTED.

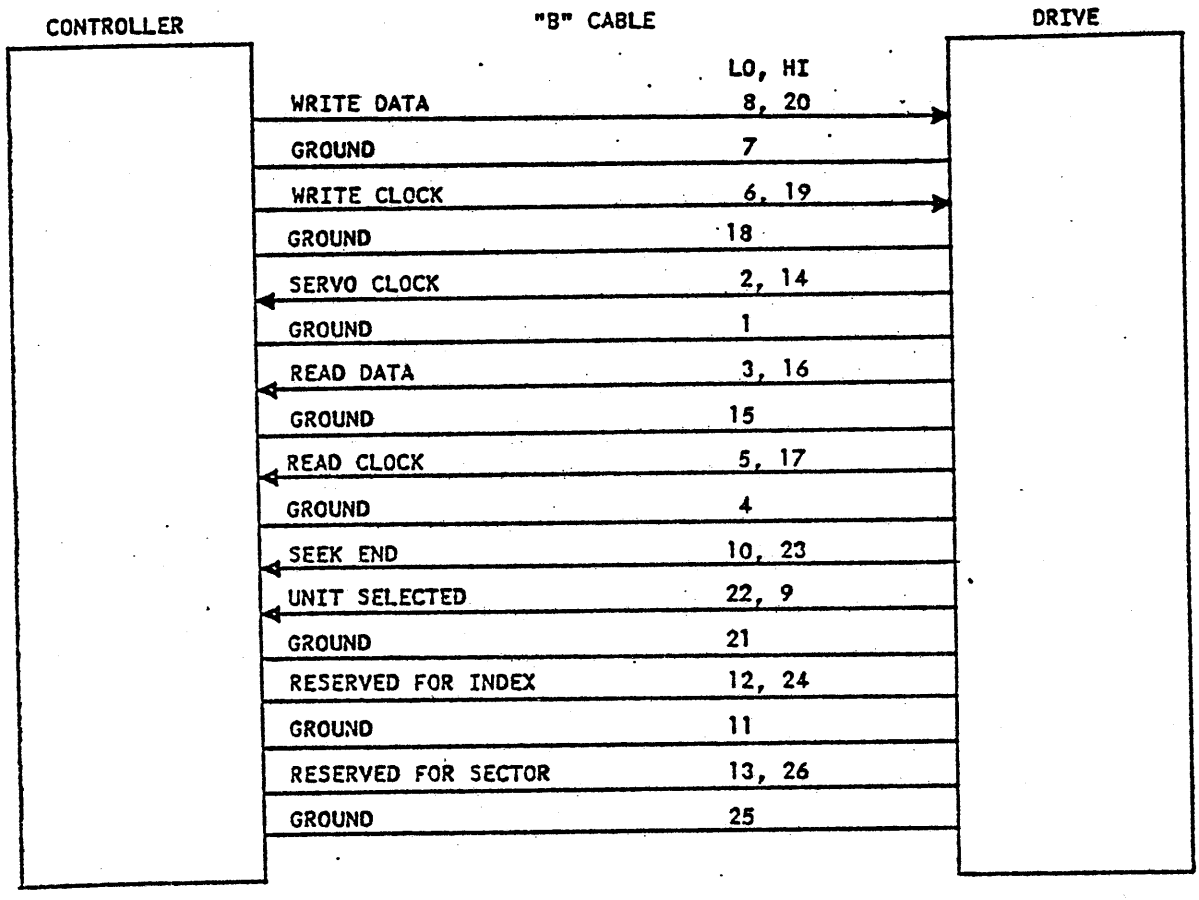
FIGURE 14. "A" CABLE TAG/BUS I/O INTERFACE

BUS	TAG 1 IN CYLINDER ADDRESS	TAG 2 IN HEAD SELECT	TAG 3 IN CONTROL SELECT	UNIT SELECT
Bit 0	2^0	2^0	Write Gate	
1	2^1	2^1	Read Gate	
2	2^2	2^2	Servo Offset Plus	
3	2^3	2^3 (1)	Servo Offset Minus	
4	2^4	2^4 (1)	Fault Clear	
5	2^5		AM Enable	
6	2^6		RTZ	
7	2^7		Data Strobe Early	
8	2^8		Data Strobe Late	
9	2^9		Release (2)	(2) Priority Select

(1) ASSIGNED TO SMD FAMILY (9764/66)

(2) DUAL CHANNEL ONLY

FIGURE 15. TAG BUS DECODE

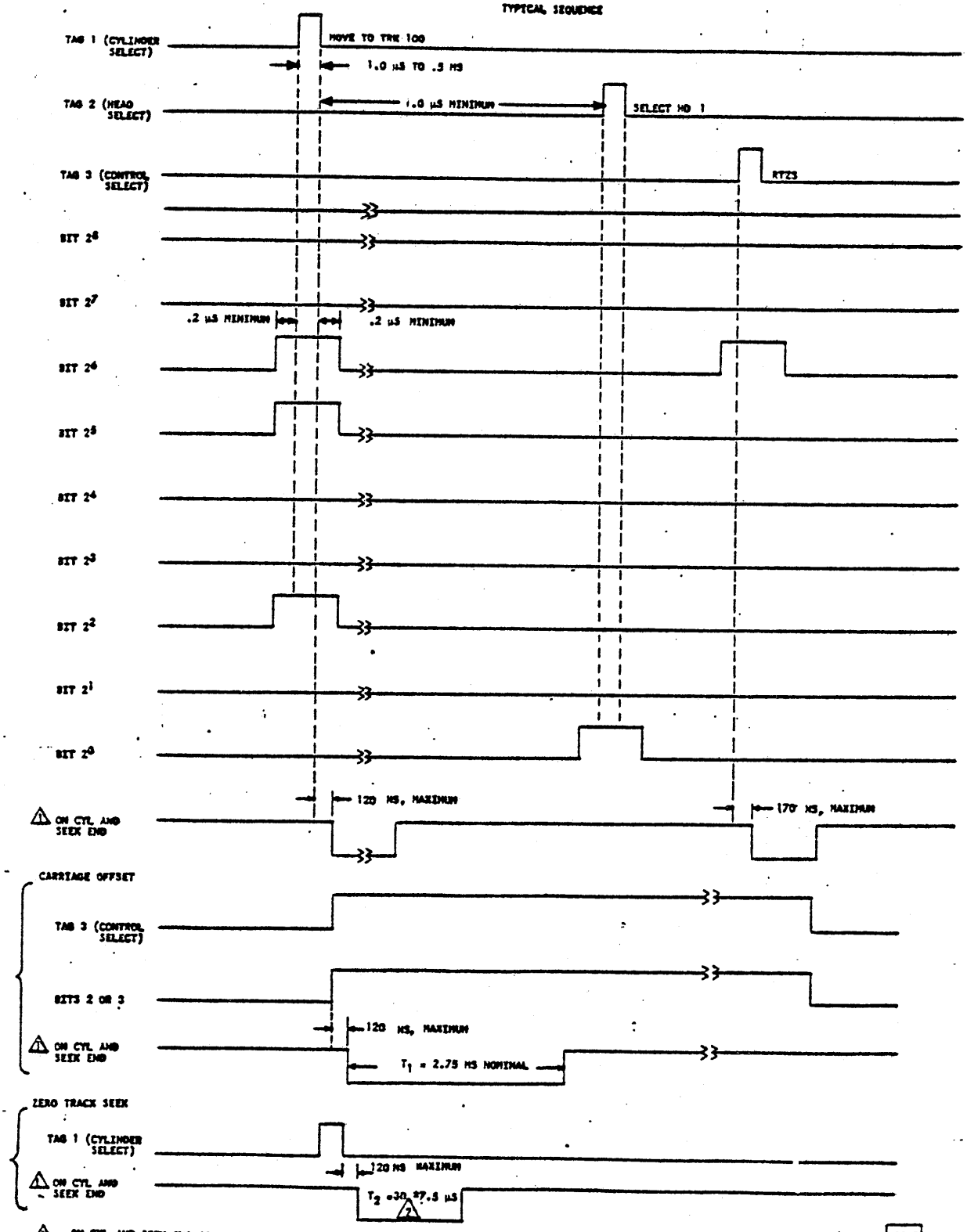


I88C

NOTES: 1. 26 CONDUCTOR FLAT CABLE. MAXIMUM LENGTH - 50 FT.

2. NO SIGNALS GATED BY UNIT SELECTED.

FIGURE 16. "B" CABLE TAG/BUS I/O INTERFACE



1. ON CYL AND SEEK END SIGNALS ARE IDENTICAL UNLESS SEEK ERROR OCCURS. SEEK ERROR INITIATES A CONSTANT SEEK END. TIMING SHOWN IS AT THE INPUT TO THE TRANSMITTER, ALSO SEE 6.2.2.11.
2. T_2 = 150 µS MAXIMUM FOR 80 MB.

VC0680

FIGURE 17. TAG AND BUS TIMING

6. AM Enable (Bit 5) (See Note)

The AM (Address Mark) Enable line, in conjunction with Write Gate or Read Gate, allows the writing or recovering of Address Marks (Figure 18). When AM Enable is true while Write Gate is true, the writer stops toggling and erases the data, creating an Address Mark. Write Fault detection in the unit is inhibited by this signal.

When AM Enable is true while Read Gate is true, an analog voltage comparator detects the absence of read signal. If the duration of the erased area is greater than 16 bits, an Address Mark Found signal will be issued.

NOTE: If Address Mark is not used, Bit 5 must be held inactive during Control Select functions.

7. RTZ (Bit 6)

A pulse, 250 ns minimum, 1.0 ms maximum, sent to the MMD will cause the actuator to seek track 0, reset the Head Register and clear the Seek Error flip flop.

This seek is significantly longer than a normal seek to track 0, and should only be used for recalibration, not Data acquisition.

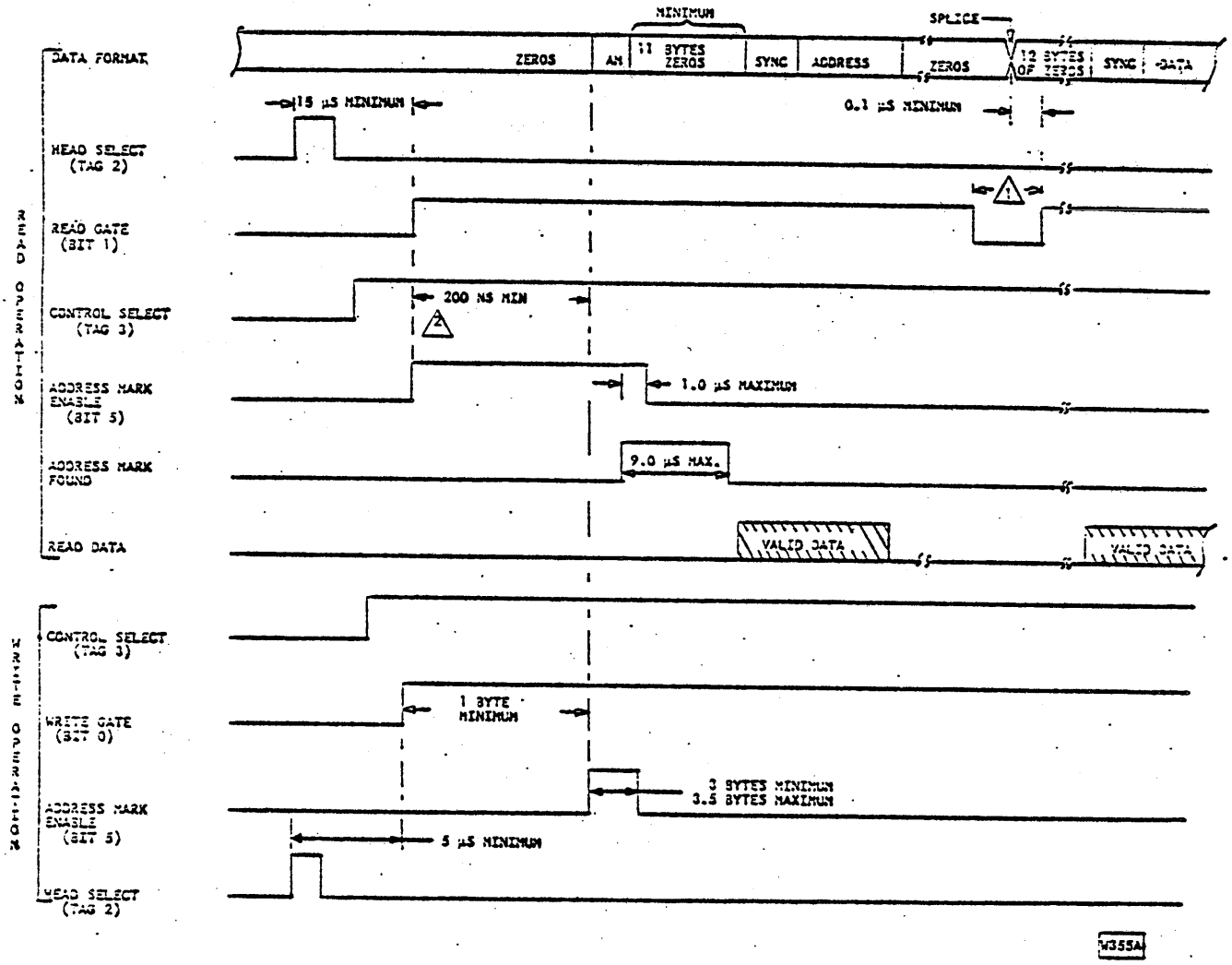
8. Data Strobe Early (Bit 7)

When this line is true, the MMD PLO Data Separator will strobe the data at a time earlier than nominal. Normal strobe timing will be returned when the line is false.

9. Data Strobe Late (Bit 8)

When this line is true, the MMD PLO Data Separator will strobe the data at a time later than nominal. Normal strobe timing will be returned when the line is false.

NOTE: The Data Strobe signals are intended to be an aid in recovering marginal data. The data strobe position returns to nominal when the respective signals go false. A carriage offset will result in loss of On Cylinder and Seek End for a period of 2 ms maximum (see Figure 17). The maximum time from forward to reverse offset or vice versa will not exceed 4 ms. Data shall not be written while in the offset mode.



NOTES: ⚠1 READ GATE MUST BE DROPPED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF ZERO BITS REMAINING IN THE SYNC FIELD. 12 BYTE (EXAMPLE) CONSISTS OF ONE BYTE FOR WRITE SPLICE AND 11-BYTES FOR PLO SYNC.

⚠2 ADDRESS MARK ENABLE SHOULD OCCUR SIMULTANEOUSLY WITH READ GATE.

FIGURE 18. TYPICAL READ/WRITE TIMING WITH ADDRESS MARK

10. Release (Bit 9) (Dual Channel Only)

Enabling this line will release channel reserve and Channel Priority Select Reserve in the MMD, making alternate channel access possible after selection by the other channel ceases. If the unit is desired to function with "Reserve Timer" feature, release will occur 500 ms (nominal) following the deselection of the MMD. If a longer or shorter time is desired, the timer may be customer altered by changing a resistor and capacitor to obtain delays from 500 ns to 10 seconds. Enabling Release will always clear Reserve and allow alternate channel access independent of the Reserve Timer feature. The Reserve Timer is enabled by means of a switch in the logic chassis. Inhibiting the Reserve Timer causes the MMD to stay Reserved until specifically released by the operating channel. A unit is Reserved immediately upon selection, but may be released any time after 500 ns following selection. By means of a switch in the logic chassis, it is also possible to absolutely reserve an MMD to one or the other channels.

6.2.1.4 Unit Select

Priority Select (Bit 9) (Dual Channel Only)

When this line is true, the unit will be unconditionally selected and absolutely reserved by the respective channel providing both channels are enabled and a priority select condition does not exist on the opposite channel. Once the Priority Select function has been performed the respective channel has exclusive access to the drive. The opposite channel can gain access only after a release function has been performed on the selected channel (see 6.2.1.3.10). For timing see Figure 19. When a priority selection exist on one channel, all interface signals are inhibited on the opposite channel including UNIT SELECTED and BUSY.

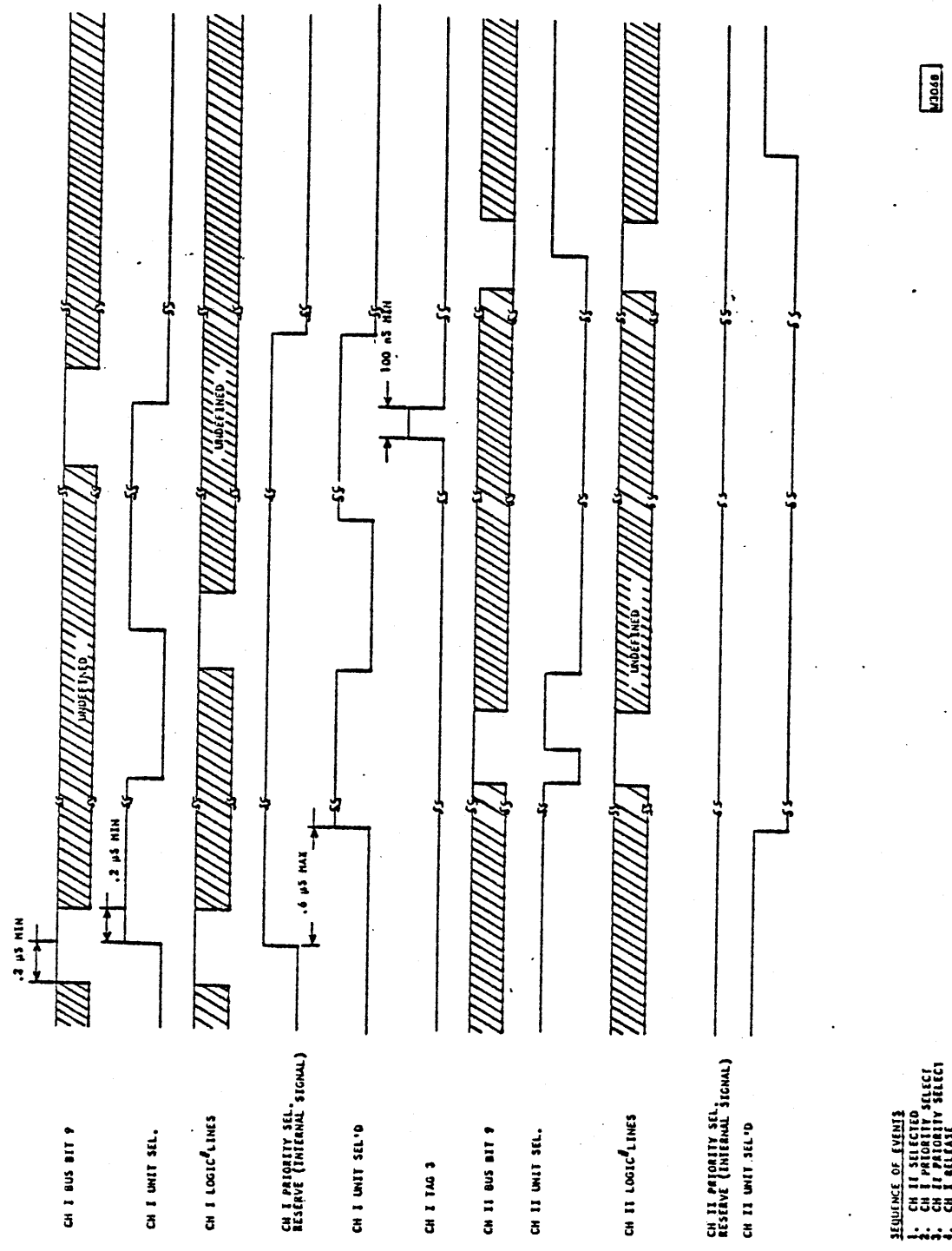


FIGURE 19. SAMPLE PRIORITY SELECT TIMING

6.2.2 Individual Lines

1. Sector Mark

The Sector Mark is derived from the servo track. Timing integrity is maintained throughout seek operations (see Figure 20). The number of sectors per revolution is switch selectable and is determined by counting sector clocks. The switches are located on a card within the logic chassis. Each switch represents a fixed number of sector clocks when closed.

Switch:	0	1	2	3	4	5	6	7	8	9	10	11
No. of sector clocks:	1	2	4	8	16	32	64	128	256	512	1024	2048

To calculate the proper switch positions for the number of sectors desired, use the following formula:

$$\frac{\text{Sector Clocks/Revolution}}{\text{No. Sectors}} - 1 = \text{Sector Clock Count/Sector}$$

Example for 8 sectors: $\frac{13\,440}{8} - 1 = 1679$

close switch

10 = 1024
9 = 512
7 = 128
3 = 8
2 = 4
1 = 2
0 = 1
One sector clock for SM counter reset 1
1680 sector clocks/sector

Each sector clock (806 kHz clock) is equivalent to 12 data bits.

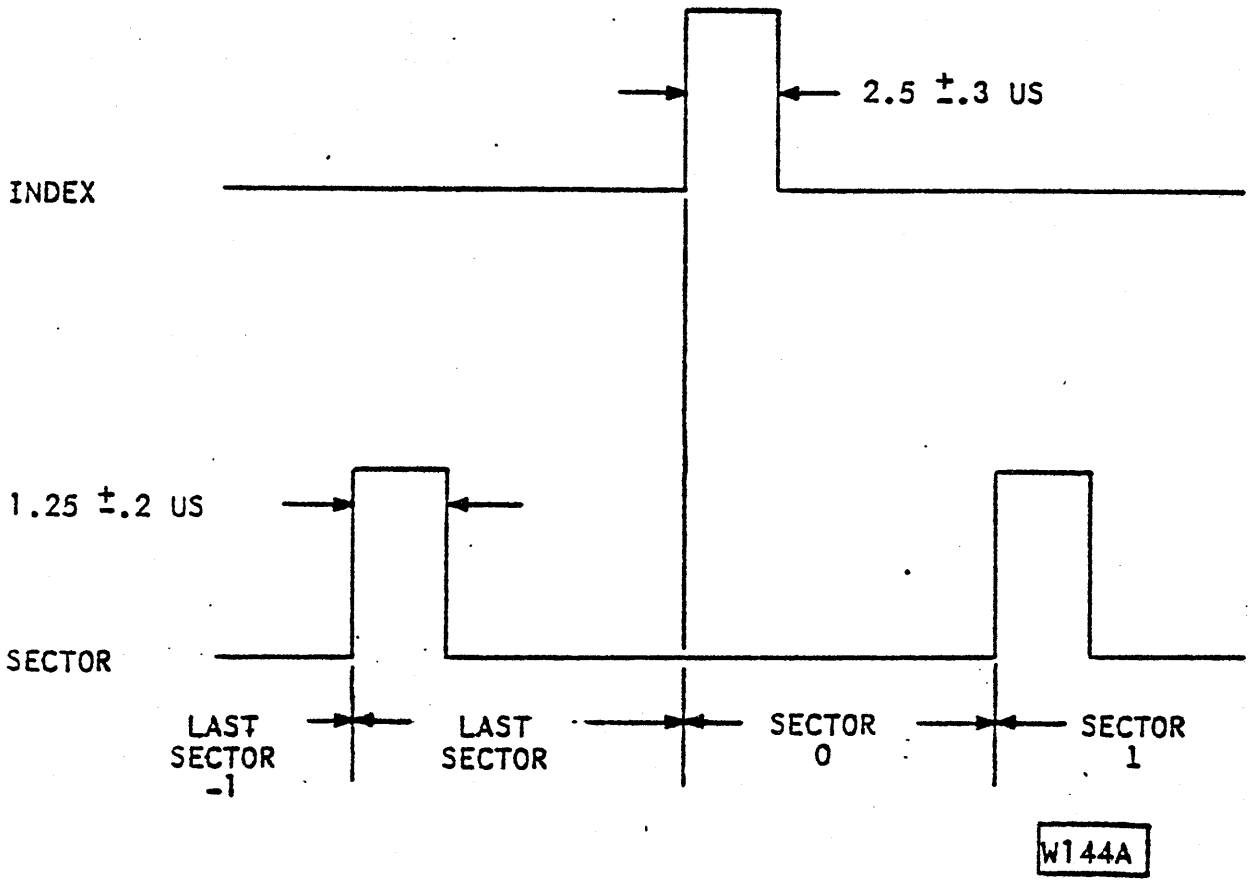


FIGURE 20. INDEX AND SECTOR TIMING

2. Fault

When this line is true, a fault condition exists in the MMD. The following types of faults may be detected by the MMD: DC Voltage Fault, Head Select Fault, Write Fault, Write or Read while Off Cylinder, and Write Gate during a Read operation. A fault condition will immediately inhibit the writer to prevent data destruction. The DC Voltage Fault indicates a below normal voltage from the positive or negative power supplies. The Head Select Fault indicates that more than one head is selected. The Write Fault indicates low (or the absence of) write current as well as the absence of write data.

This line may be cleared by Control Select, or Fault Clear on the Operator Panel, or Master Fault Clear on the Fault card (providing the fault no longer exists). Faults are stored in individual flip flops as a maintenance aid, and may be cleared only by powering down dc power or clearing the fault by means of the switch on the fault card.

3. Seek Error

When this line is true, a Seek Error has occurred. The error may only be cleared by performing a RTZ. This signal indicates that the carriage has moved to a position outside the recording field.

NOTE: Because of the recording characteristics of the servo positioning tracks, some modules may not detect a Seek Error at cylinder address 320 (an illigal address). In this case, a Seek Error will be detected at cylinder address 321 (12 and 24 only).

The 12 and 24 MB MMD's will not decode a seek error for an illegal track address until the positioner moves the heads into a guard band area. This requires approximately 65 ms under worst case conditions. There is no seek error status for cylinders beyond the designated fixed head cylinders.

The 80 MB MMD will decode a seek error for an illegal track address of 823 to 895 for the moving head portion. A seek error will also be decoded at cylinder 916 and above for fixed heads. The device will not decode a seek error in units without fixed heads or units with only one fixed head assembly (48 heads) if the designated fixed head cylinders are addressed. Response time for an invalid cylinder is 250 µs max.

A Return-to-Zero Seek Command will clear the Seek Error condition, return the heads to cylinder zero, and enable an On Cylinder signal to the Controller.

4. On Cylinder

This status indicates the servo has positioned the heads over a track. The status is cleared with any seek instruction causing carriage movement, or a zero-track seek. A carriage offset will result in loss of On Cylinder for a period of 2.75 ms (nominal). For a zero track seek, on cylinder drops for 30 µs nominal 12/24 MB, 150 µs max. for 80 MB.

5. Index

This signal occurs once per revolution, and its leading edge is considered the leading edge of the Sector Zero, typically 2.5 µs (see Figure 20). Timing integrity is retained throughout seek operations.

6. Unit Ready

When true, and the unit is selected, this line indicates that the unit is up to speed, and the heads are over the recording tracks and no fault condition exists within the MMD.

7. Open Cable Detector

The open cable detect circuit (see Figure 11) disables the interface in the event that the "A" interface cable is disconnected or controller power is lost.

It is recommended that the controller circuitry have sufficient voltage margins and interlocks to prevent operation on the MMD before controller is Ready or prior to impending controller power failure. Relay logic and passive terminations sometimes aid this requirement. If 75110A transmitters are used to drive the Open Cable Detect line from the controller, two transmitters should be paralleled, and no 56 ohm termination resistance to ground should be used at the controller end.

8. Unit Select Tag

This signal gates the desired logic number into the logic number compare circuit. The unit will be selected internally 600 ns (maximum) after leading edge of this signal. For timing see Figure 21. Note that this function must be edge triggered.

In Dual-Channel Units, Unit Select tag also forces the MMD to be reserved to that channel, providing selection occurs. The reserve will not be cancelled unless by release command, Reserve Timer or dc power-down/power-up. If Bus Bit 9 and the desired logic number is present with Unit Select Tag, a Priority Select will be performed, refer to paragraph 6.2.1.4. The unit will be selected internally 600 ns (maximum) after leading edge of Unit Select Tag. For timing see Figure 21. If both controllers request access simultaneously, Channel A will be granted priority.

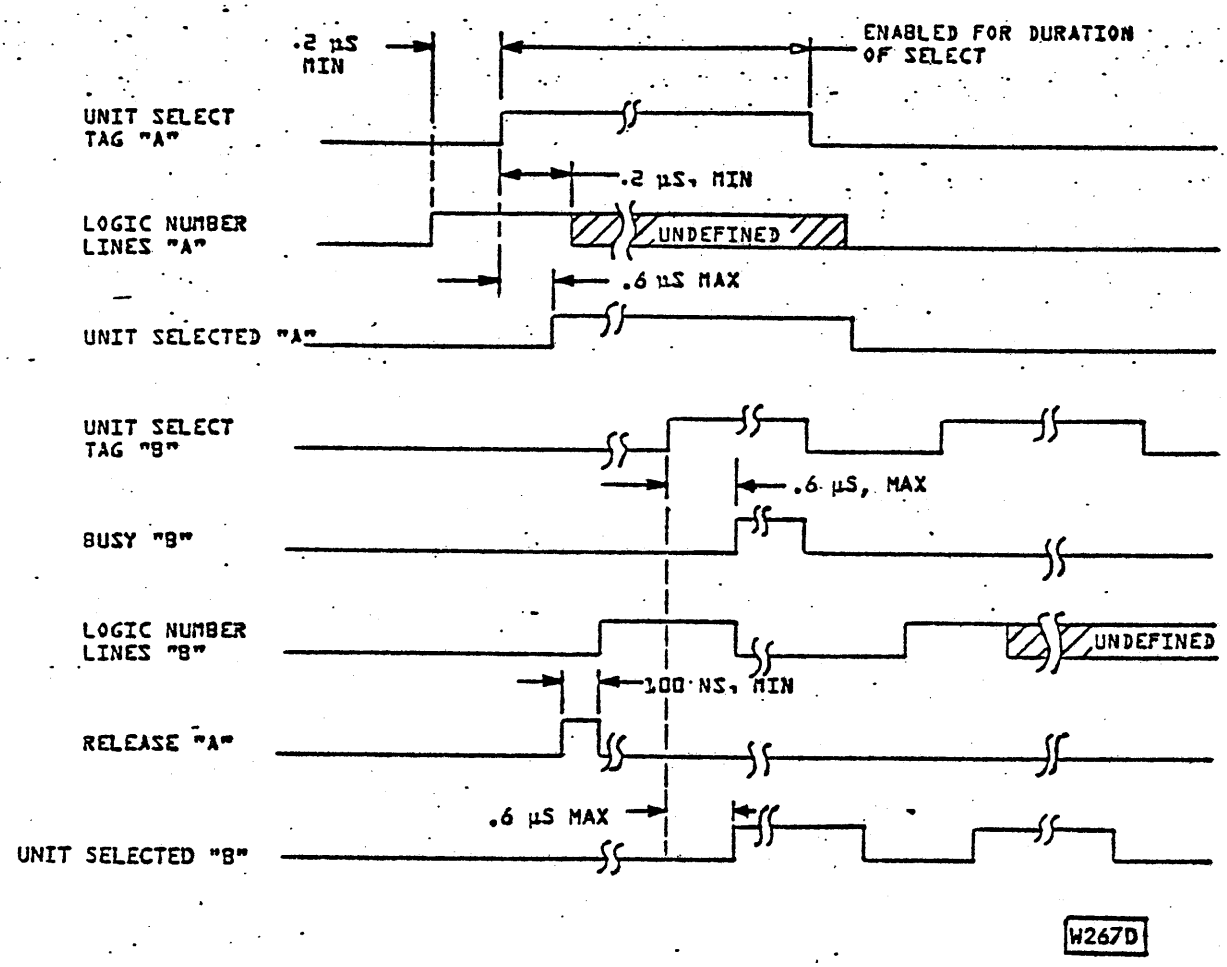


FIGURE 21. LOGIC NUMBER SELECT AND TIMING DIAGRAM

9. Unit Select (2^0, 2^1, 2^2, and 2^3)

These four lines are binary coded to select the logical number of 1 of 16 MMDs. The unit number (0 through 15) is selectable by means of switches located on a card in the logic chassis.

10. Address Mark Found

Address Mark Found is a pulse which is sent to the controller following recognition of at least 16 missing transitions and the first zero of the zeros pattern.

The controller must drop the Address Mark Enable line (Bit 5) upon receiving Address Mark Found (AMF) and valid data will be presented on the I/O lines following the AMF pulse. Upon sensing the dropping of Address Mark Enable line, the Address Mark Found pulse will be reset within 8.0 µs maximum (see Figure 18).

NOTE: Under certain conditions it is possible that the MMD could issue a false Address Mark Found signal during an address mark search operation. This would occur if a media flaw existed which simulated the electrical characteristics of an address mark (at least 16 missing transitions followed by a zero).

It is recommended provisions be made in system hardware or software to allow recovery from, or avoid the possibility of detecting false AMF signals.

11. Seek End

Seek End is the combination of ON CYLINDER or SEEK ERROR indicating that a seek operation has terminated. In Dual Channel Drives, the Seek End Signal sent to the unselected channel will normally be a constant one. However, if while the Drive is selected on a channel, and the opposite channel receives a select, this action will be noted by circuitry within the Drive. Then, when the selected channels Select and Reserve Latches are cleared, the Seek End Signal sent to the waiting channel will go to a zero for 30 µs. For a zero track seek, "seek end" drops for 30 µs nominal 12/24 MB, 150 µs max. for 80 MB.

12. Unit Selected

When the four Unit Select bit lines compare with the settings of the Unit Select switches in the logic chassis, and when the leading edge of Unit Select tag is received, the Unit Selected line becomes true and is transmitted to the controller on the "B" cable (see Figure 21). Multiple Unit Selected responses on a daisy-chain system indicate duplicate switch settings have been used.

13. Write Protected

Enabling the Write Protect function inhibits the writer under all conditions, illuminates a LED located on logic cards, and sends a Write Protected signal to controller. Attempting to write while protected will cause a fault to be issued. The Write Protect function is enabled by a switch located on a card in the logic chassis.

14. Power Sequencing (Figure 22)

Power Sequencing requires ac power on, and REMOTE START switch (switch selectable in MMD) in the Remote position. Applying ground to the Pick and Hold lines will cause the first MMD in sequence to power up. Once this MMD is up to speed, the Pick signal is transferred to the next active MMD and repeated until all active MMD's or SMD's are powered up. Individual MMD's may be started and stopped once power sequencing is completed.

A power failure necessitates a new power up sequence.

When in Local Start mode, each MMD is independently operated by its respective AC Power switch.

In the Remote Mode a Pick or Hold is considered to be present from the Controller when a ground is present on "A" cable Pin 29 for Pick and Pin 59 for Hold.

15. Busy (Dual Channel Only)

If the MMD is already reserved and/or selected, a Busy signal will be issued to the "A" cable and unit selected will be issued on the "B" cable to the channel attempting the select. This busy signal will be issued from the MMD at its I/O connector within 600 ns following the selection attempt, and will remain at this status until Unit Select tag is dropped or the unit is no longer busy. Unit Selected should be used to enable Busy in the Controller.

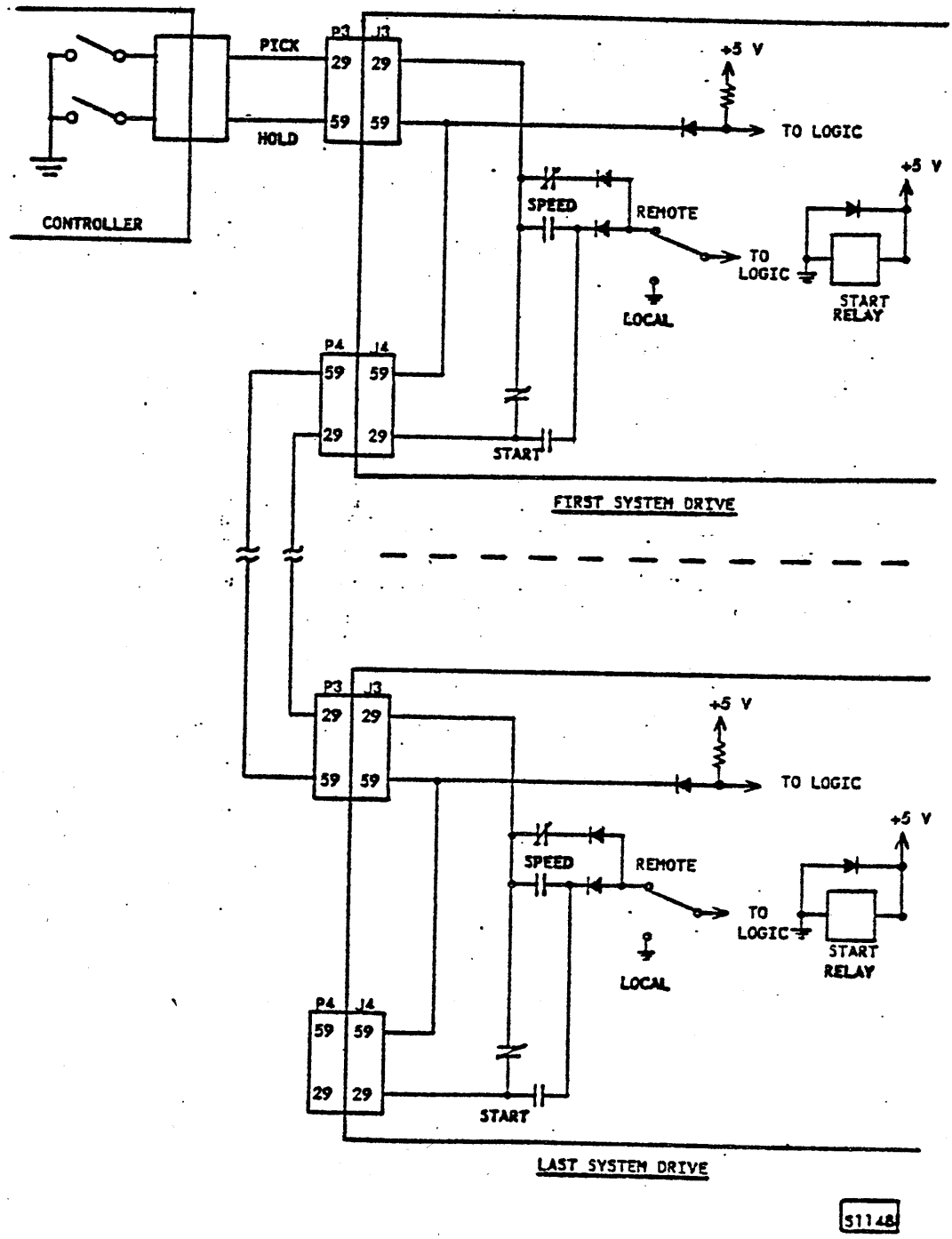


FIGURE 22. SEQUENCE POWER LINES

6.2.3 Data and Clock Lines (Figure 23)

1. Write Data

This line carries data which is to be recorded on the disk pack.

2. Servo Clock

The servo clock is a phase-locked 9.677 MHz clock generated from the servo track quadbits. This phase-locked clock (Figure 23) is used to generate write data. Servo clock is available at all times (not gated with Unit Select).

3. Read Data

This line transmits the recovered data in the NRZ form (Figure 23) data.

4. Read Clock

The read clock defines the beginning of a data cell. It is an internally derived clock signal and is synchronous with the detected data as specified in Figure 23. This signal is transmitted continuously, and is in phase sync within 9 µs after Read Gate.

5. Write Clock

This line transmits the Write Clock signal which must be synchronized to the NRZ data as illustrated in Figure 23. The Write Clock is the Servo Clock retransmitted to the MMD during a write operation. The Write Clock need not be transmitted continuously, but must be transmitted at least 250 ns prior to Write Enable.

6.3 Data Format and Data Control Timing

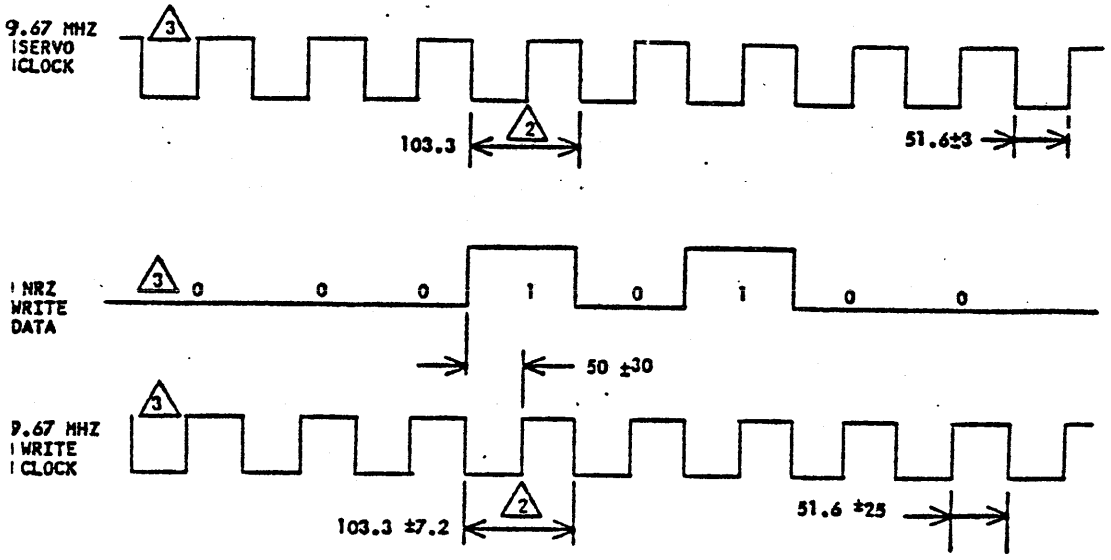
The Record Format on the disk is under control of the controller. The index and sector pulses are available for use by the controller to indicate the beginning of a track or sector. Suggested formats for fixed and variable sector data records are shown in Figures 24 and 25.

Some hardware-oriented constraints must be recognized when designing a format. The following is a list of those format parameters:

1. Beginning-of-Record Tolerance (See notes on Figures 24 and 25)

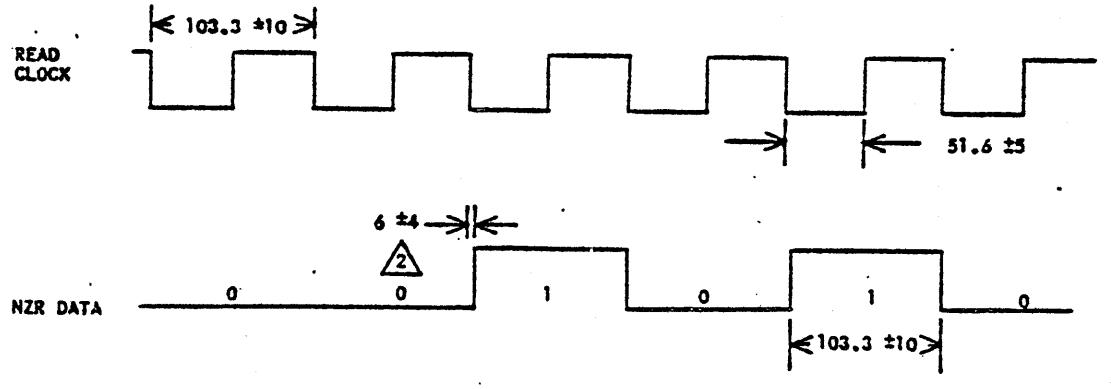
This tolerance must be provided to allow for worst case conditions of head skew and circuit tolerances.

This gap must be written with a minimum of 16 bytes of zeros.



NOTES:

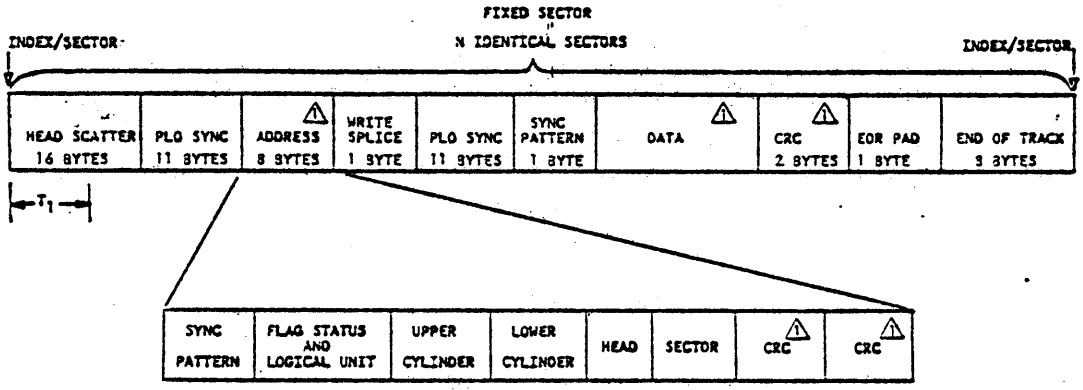
1. ALL TIMES IN NS.
2. SIMILAR PERIOD SYMMETRY SHALL BE ±2 NS. AT I/O CONNECTOR IN DRIVE, SPEED VARIATION TOLERANCE SHALL BE ±5% OF PERIOD WHICH INCLUDES SPINDLE SPEED TOLERANCE AND DIBIT DROPOUT WHILE CARRIAGE IS MOVING.
3. AT I/O CONNECTOR IN CONTROLLER.



NOTES:

1. ALL TIMES IN NS.
2. NEGATIVE EDGE OF CLOCK PRECEDES SIGNIFICANT EDGE OF DATA AT I/O CONNECTOR.

FIGURE 23. WRITE DATA AND SERVO CLOCK TIMING



T_1 = TIME BETWEEN LEADING EDGE OF INDEX/SECTOR AND READ GATE IS 8 BYTES. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

D1358

EXAMPLE NO. 1: WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - (\text{SYNC FIELDS, TOLERANCE GAPS, AND ADDRESS})$$

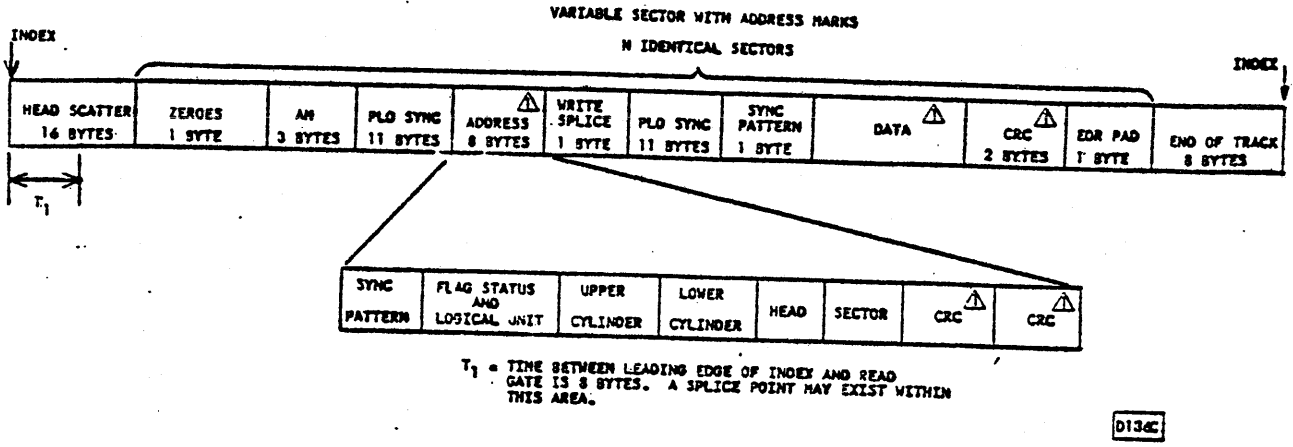
$$\text{DATA FIELD} = \frac{20\,160}{64} - 59 = 256\ \frac{\text{BYTES}}{\text{SECTOR}}$$

DATA = 256 BYTES/SECTOR

$$\%\ \text{EFFICIENCY} = \frac{256 \times 64}{20\,160} \times 100 = 81\%$$

⚠ THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

FIGURE 24. FIXED SECTOR FORMAT



T_1 = TIME BETWEEN LEADING EDGE OF INDEX AND READ GATE IS 8 BYTES. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

D136C

EXAMPLE NO. 1: WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK} - \text{MECHANICAL TOLERANCES}}{\text{NUMBER OF SECTORS/TRACK}} - (\text{SYNC FIELDS AND ADDRESS})$$

$$\text{DATA FIELD} = \frac{20\,160 \frac{\text{BYTES}}{\text{TRACK}} - 24 \frac{\text{BYTES}}{\text{TRACK}}}{64 \frac{\text{SECTORS}}{\text{TRACK}}} - 39 \frac{\text{BYTES}}{\text{SECTOR}} = 275 \frac{\text{BYTES}}{\text{SECTOR}}$$

$$\% \text{ EFFICIENCY} = \frac{275 \times 64}{20\,160} \times 100 = 87\%$$

EXAMPLE NO. 2: WHAT IS NUMBER OF SECTORS USING 256 DATA BYTES?

$$\text{N SECTORS} \quad \frac{20\,160 - 24}{256 + 39} = 68 \text{ SECTORS}$$

$$\% \text{ EFFICIENCY} = \frac{256 \times 68}{20\,160} \times 100 = 86\%$$

⚠ THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

FIGURE 25. VARIABLE SECTOR FORMAT

2. Read PL0 Synchronization

   The synchronization time needed to allow the phase-locked oscillator to synchronize is 9 µs of zeros.

3. Sync Pattern

   The Sync Pattern consists of "one" bits indicating the beginning of the address or data area (one "one" bit is the minimum required).

4. Write Driver Turn On

   The Write Driver Turn On time is about 0.8 µs or one byte. This time has to be accounted for in order to know where possible splice areas are located.

5. End-of-Record Tolerance (See notes on Figures 24 and 25)

   This tolerance is an eight byte pad of zeros which eliminates the possibility of destroying the end of a record written with a late displacement head.

6.3.1 Write Format Procedure

Provisions must be made within the Controller to format the disk. The following procedure is recommended for fixed sector formats:

PROCEDURE

1. Select desired unit, cylinder, head, and sector.
2. The Controller must provide a 5 µs minimum delay between selecting a head and initiating a search for leading edge of sector. This delay will ensure that the unit will be ready to write when the sector leading edge is detected.
3. Search for leading edge of desired sector.
4. Detect leading edge of selected sector.
5. Immediately bring up Write Gate and start writing zeros.
6. Write all zeros for head scatter and PL0 sync areas (27 bytes).
7. Write a sync pattern, the address, and the address checkword.
8. Write all zeros for write splice gap and PL0 sync field (12 bytes).

9. Write a sync pattern, the data field, the two byte data field checkword, and the one byte pad at the end of the checkword. The data field should be written with all ones or preferably a worst case pattern.

10. The end tolerance gap is the only part of the format where there may be erased areas with no write data. If erased areas occur in Gap 2 there may be problems in recovering the data following this gap.

11. If the next sector of the same track is to be formatted and the head is not deselected, the Write Gate may be left on. In this case, the Controller should write all zeros in the tolerance gap.

6.3.2 Control Timing (Figure 26)

1. Read

The control line associated with a read command is the Read Gate line.

The leading edge of Read Gate forces the phase locked oscillator to synchronize on an all zeros pattern. Read Gate also enables the output of the data separator onto the I/O lines after a lock-to-data internal time out. Read Gate must be dropped and raised again after going through a splice area. Read Gate may be enabled 60 ±4 clock counts after the leading edge of index or sector.

The sync pattern search may begin 88 servo clock counts after the leading edge of Read Gate, or after the trailing edge of Address Mark Found.

Head switching and read amplifier stabilization (see Figure 26) shows the latest acceptable time at which a head can be selected in order to read the next successive sector (with the format described in 6.3).

Data I/O lines may not have valid data until 9 µs from leading edge of Read Gate, due to phase lock synchronizing time.

Ensure that there will be no splice area after Read Gate is brought up.

2. Write Data Field

The control line associated with a Write operation is Write Gate.

The sector address must always be read and verified prior to writing the data field, except while formatting.

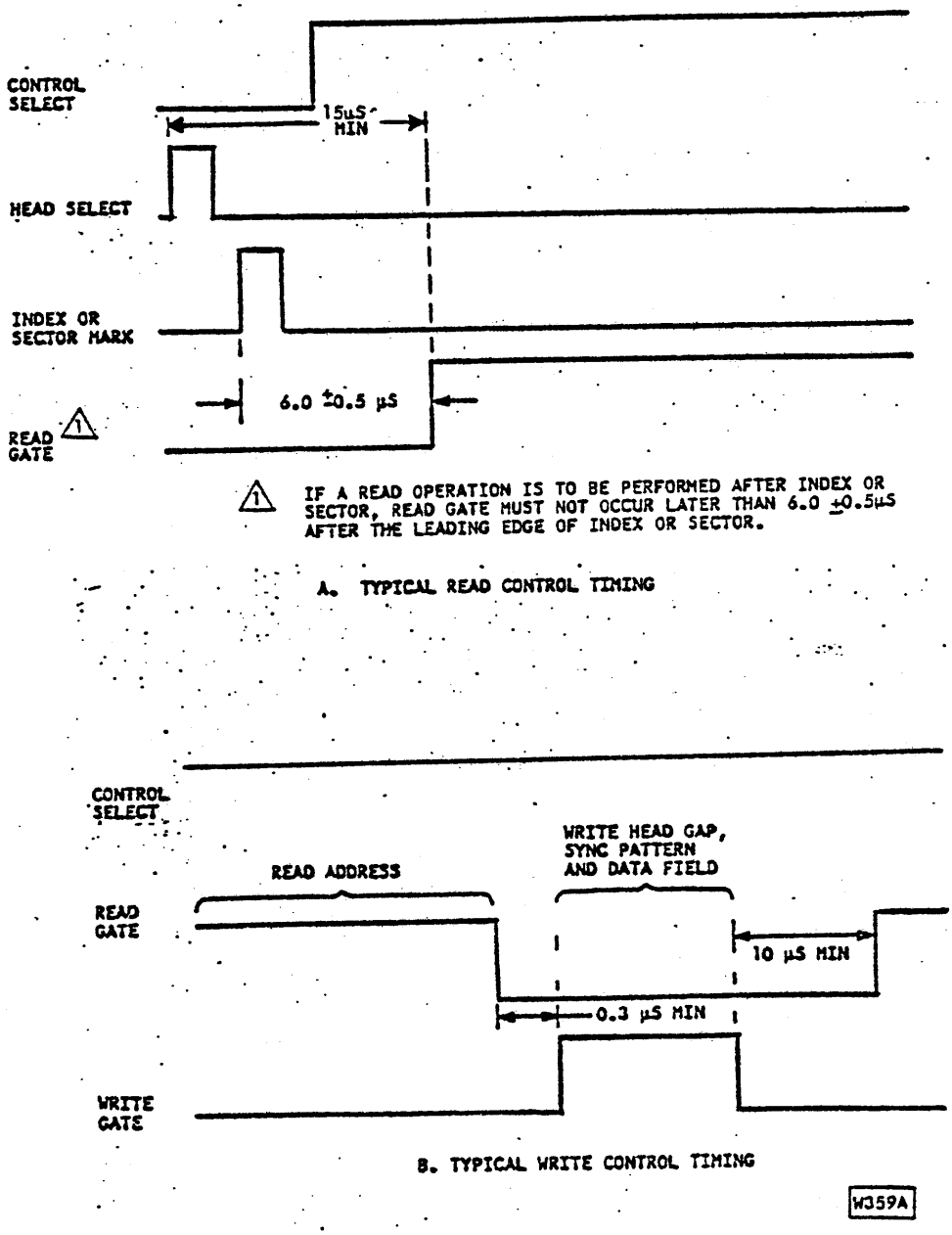


FIGURE 26. CONTROL TIMING

Writing the data field must always be preceded by writing the PLO sync field and sync pattern.

The Controller must provide a three bit internal delay (approximately 0.3 µs) between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal (see Figure 26). This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the unit.

Writing the data field must always be followed by writing the checkword and at least an eight bit pad at the end of the checkword.

During formatting, Write Gate is raised immediately upon sensing index or sector. During a record update, Write Gate is raised within two bits of the last bit of an address.

6.4 Fixed Head (Optional)

6.4.1 Logical Addressing

With the fixed head option incorporated in the MMD, the 48/96 physical fixed heads are addressed by the controller as logical cylinders. This addressing scheme allows maximum interface commonality with the moving head storage of the MMD and also with the MPI Storage Module family of removable media drives. The logical/physical addressing relationship for these devices is summarized in Table 4 and Figure 27. The remainder of fixed heads are addressed in the highest fixed head cylinder (see example below):

MEDIA DATA→	MMD 12 MB	MMD 24 MB	MMD 80 MB	SMD 40/80 MB	SMD 150/300 MB
DATA SURFACES/DEVICE	1	2	5	5	19
MOVEABLE HEADS/SURFACE	2	2	2	1	1
FIXED HEADS/DEVICE	48	48	48/96	0	0
MOVEABLE CYLINDERS/DEVICE	320	320	823	411/823	411/823
FIXED CYLINDERS/DEVICE	12	12	10/20	0	0
MOVEABLE HEADS/LOGICAL CYLINDER	2	4	5	5	19
FIXED HEADS/LOGICAL CYLINDER	4	4	5 ⚠1 ⚠2	0	0
MOVEABLE CYLINDER ADDRESSES	0-319	0-319	0-822	0-410/0-822	0-410/0-822
FIXED CYLINDER ADDRESSES	896/907	896/907	896/905/915	-	-

⚠1 .96 MB FIXED HEAD OPTION HAS 3 ADDRESSABLE HEADS IN CYLINDER 905.

⚠2 1.92 MB FIXED HEAD OPTION HAS 1 ADDRESSABLE HEADS IN CYLINDER 915.

M369D

TABLE 4. MMD/SMD LOGICAL/PHYSICAL ADDRESSING

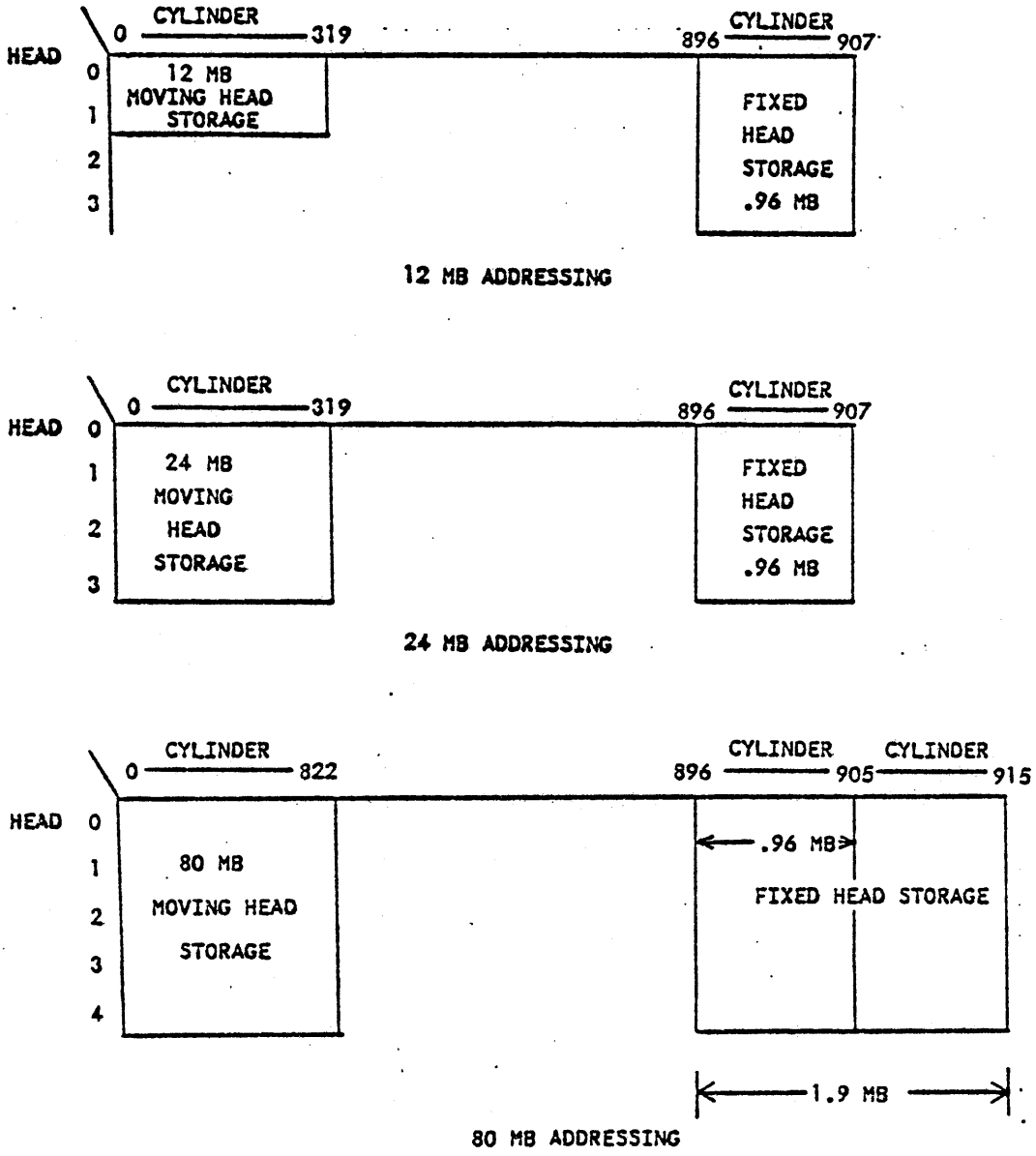
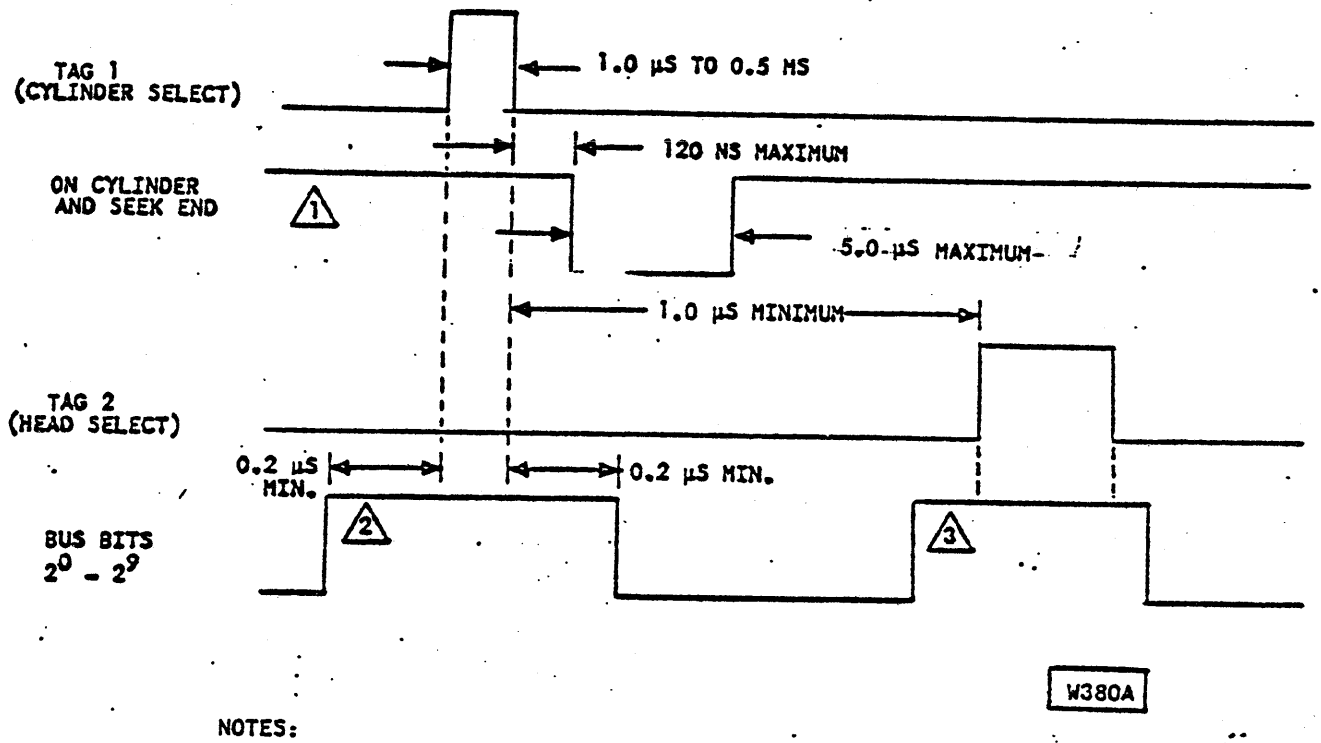


FIGURE 27. STORAGE ADDRESSING



NOTES:

1. TIMING SHOWN IS AT THE INPUT TO THE TRANSMITTER.
2. CYLINDER ADDRESSES 896-907 FOR FIXED HEAD (12 AND 24 MB).
   CYLINDER ADDRESSES 896/905/915 FOR FIXED HEAD (80 MB).
3. HEAD ADDRESSES 0 - 4 FOR FIXED HEAD.
4. TAG 1 and TAG 2 MAY BE ISSUED IN EITHER ORDER PROVIDING 1.0 µS MINIMUM TIMING IS ALLOWED BETWEEN COMMANDS.
5. HEAD SELECT MUST BE REISSUED WHEN SWITCHING BETWEEN FIXED AND MOVEABLE STORAGE.

FIGURE 28. FIXED HEAD TAG/BUS TIMING

7.0 CONTROLS AND INDICATORS

7.1 Operator Panel

The unit contains a front panel with a ready indicator and a fault/clear, switch/indicator.

NAME	TYPE LIGHT	TYPE SW	FUNCTION
READY	X (Green)		Indicates Unit Ready status, i.e., pack is up to speed, the heads are loaded, and no fault condition exists within the unit.
FAULT / CLEAR	X (Red)	X	Indicates any fault condition. The switch clears the fault flip-flop.

7.2 Maintenance Switch and Indicators

Fault conditions listed below are stored (in a flip-flop register with L.E.D. display for easy read out) on a card in the logic chassis and are visible only when the MMD is in the maintenance position. The indicators are cleared by the switch on the fault card or by removing dc power.

NAME	TYPE LIGHT	TYPE SW	FUNCTION
WRITE	X		Indicates that a write fault had occurred.
HEAD SELECT	X		Indicates that a multiple head select had occurred.
WRITE AND READ	X		Indicates write and read conditions existed simultaneously.
WRITE OR READ AND OFF CYL	X		Indicates write or read conditions existed during a seek operation (off cylinder).
VOLTAGE	X		Indicates a below normal voltage had existed.
FAULT CLEAR		X	Master clears all faults providing the fault no longer exists.
SEEK ERROR	X		Indicates that a SEEK ERROR had occurred.

7.3 Channel Select and Reserve Switches and Indicators {Located on logic circuit board.}

NAME	TYPE		FUNCTION
	Light	Sw	
DI/NRM		X	Switch will disable Channel I or allow Channel I to be selected.
DII/NRM		X	Switch will disable Channel II or allow Channel II to be selected.
ABR/RTM		X	In ABR position once drive is selected it must be released in order for reserve to drop. In RTM position once drive is deselected, reserve will drop after 500 msec.
Ch. I Sel	X		Indicates Channel I is selected.
Ch. I Res	X		Indicates Channel I is reserved.
Ch. II Sel	X		Indicates Channel II is selected.
Ch. II Res	X		Indicates Channel II is reserved.

7.4 Miscellaneous Switches and Indicators {Located on logic circuit board.}

NAME	TYPE		FUNCTION
	Light	Sw	
Write Protect	X	X	Inhibits writer.

8.0 PHYSICAL SPECIFICATIONS

Weight and dimensions are shown in the Plan View, Figure 32, and do not include the shipping container or packaging.

9.0 RELIABILITY AND SERVICE GOALS

9.1 Mean Time Between Failure - Applies to any MMD configuration defined in this specification.

Following an initial period of 200 hours, the Mean Time Between Failure shall exceed 5500 hours for units manufactured in the first year of production and 7000 hours for units manufactured in the second year. For units manufactured after the second year, the MTBF shall exceed 8000 hours. The following expression defines MTBF:

$$\text{MTBF} = \frac{\text{Operating Hours}}{\text{No. of Equipment Failures}}$$

Operating hours means total time meter hours less any maintenance time recorded. Equipment failures means any stoppage or substandard performance of the equipment because of equipment malfunction, excluding stoppages or substandard performance caused by operator error, adverse environment, power failure, controller failure, cable failure, or other failure not caused by the equipment. To establish a meaningful MTBF, operation hours must be greater than 5200 hours and shall include field performance data from all field sites.

For the purpose of this specification, equipment failures are defined as those failures necessitating repairs, adjustments or replacements on an unscheduled basis. Essentially, the term equipment failure implies that emergency maintenance is required because of hardware failure or substandard performance.

9.2 Mean Time to Repair

The mean time to repair shall not exceed 1.0 hours; it is defined as the time for an adequately trained and competent serviceman to diagnose and correct a malfunction.

9.3 Preventive Maintenance Time

No scheduled maintenance is required, other than course filter cleaning or replacement.

9.4 Service Life

The Mini-Module Drive is designed and constructed to provide a useful life of five years before factory overhaul or replacement is required. Repair or replacement of major parts will be permitted during the MMD's lifetime.

10.0 INSTALLATION AND MAINTENANCE

Required connections to the device are power (dependent upon options selected), signal cables and a system ground consistent with normal peripheral equipment grounding practices. The only physical requirement is adequate clearances for maintenance and air intake/exhaust. Detailed instructions are found in the equipment maintenance manuals.

10.1 Power Requirements

10.1.1 Primary Power Requirements

The primary voltage, frequency, and power requirements are shown in Tables 5 and 6.

VOLTAGE (VAC)	TOLERANCE (VAC)	FREQUENCY (HZ)	TOLERANCE (HZ)
120	+8.0, -18	60	+.6, -1.0
220	+15.0, -25	50	+.5, -1.0
240	+17.0, -27	50	+.5, -1.0

TABLE 5. PRIMARY VOLTAGE AND FREQUENCY REQUIREMENTS

UNIT STATUS	UNIT TYPE	AC POWER (VAC-HZ)	LINE CURRENT *	KVA *	CONSUMPTION *	
					KW	BTU/HR
Disks and Carriage in Motion	9730-12/24	120-60	3.7	0.444	0.350	1200
	9730-12/24	220-50	2.0	0.444	0.370	1265
	9730-12/24	240-50	1.92	0.460	0.375	1280
	9730-80 (1)					
Disks not in Motion (Standby)	9730-12/24	120-60	1.2	0.144	0.10	345
	9730-12/24	220-50	0.74	0.154	0.140	480
	9730-12/24	240-50	0.77	0.184	0.160	550
	9730-80 (1)					

* The numbers shown in this table are maximum values.

(1) To be supplied for 80 MB configuration.

TABLE 6. MAXIMUM MAINS POWER REQUIREMENTS

10.1.2 AC Power Connector (See Figure 31)

NOTE: The customer may elect to hardwire or use his own connector consistent with his system's ac distribution; connectors will be furnished with the 120 V, 60 Hz MMD's only.

Description	CDC P/N	NEMA Configuration
120 V, 15 A, 60 Hz, 1Ø 2 pole, 3 wire, male connector	24531601	5-15 p

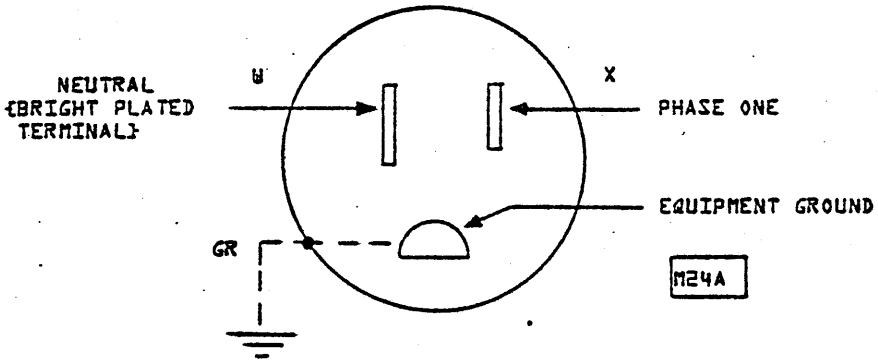


FIGURE 29. OUTLET PIN CONFIGURATION

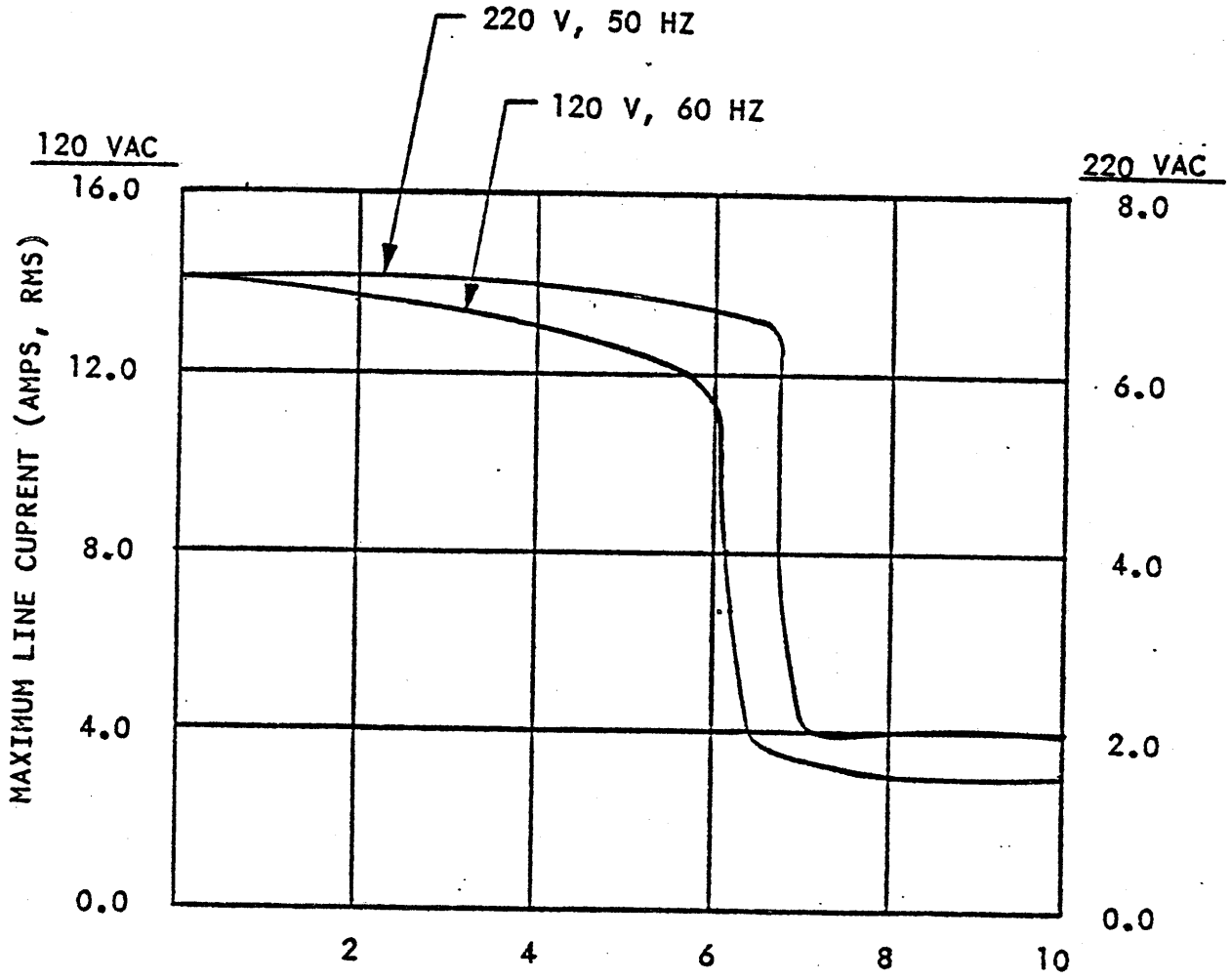
220 V or 240 V, 50 Hz MMD's

No connector furnished
Cable color code is:

Brown - Phase One
Blue - Neutral
Green and Yellow - AC Equipment Ground

10.1.3 Line Current

Start up current is shown in Figure 30 below.



NOTE: TO BE SUPPLIED FOR 80 MB CONFIGURATION

M351A

FIGURE 30. LINE CURRENT VERSUS START-UP TIME

10.2 Grounding

A ground strap shall be connected between the power supply dc grounds of the controller and MMD [s]. Detailed instructions are in the Equipment Maintenance Manual.

10.3 Environmental Limits

See Table 7 and Figure 31.

10.4 Air Flow

The enclosure must provide an exhaust opening for the fan air flow across the electronics, motor and power supply.

An open inlet and exhaust area of 40 sq. inches for each module can be used as nominal design figure for the enclosure. The ideal location for the exhaust opening is a rear position on the top panel, the second choice would be a top position on the rear panel. The openings especially if on the top panel should be louvered, baffled or screened to prevent debris from being dropped onto the unit.

An open bottom on the enclosure which allows air to enter around the base and be exhausted at the top of the cabinet will promote a natural air flow through the cabinet which will aid the air flow from the fan.

ENVIRONMENTS	STORAGE RANGE	TRANSIT RANGE	ON SITE NONOPERATING	OPERATING OFFICE ENVIRONMENT
TEMPERATURE	14°F to 122°F -10°C to 50°C MAX CHANGE 27°F/HOUR 15°C/HOUR	-40°F to 158°F -40°C to 70°C MAX CHANGE 36°F/HOUR 20°C/HOUR	50°F to 104°F 10°C to 40°C MAX CHANGE 18°F/HOUR 10°C/HOUR GRADIENT 18°F, 10°C	50°F to 104°F 10°C to 40°C MAX CHANGE 18°F/HOUR 10°C/HOUR GRADIENT 18°F, 10°C
HUMIDITY	10% to 90% RH NO CONDENSATION	0% to 100% RH NO CONDENSATION	20% to 80% RH MAX CHANGE - 10%/HR NO CONDENSATION	20% to 80% RH MAX CHANGE - 10%/HR NO CONDENSATION
BAROMETRIC PRESSURE STANDARD DAY	31 IN. Hg to 23.9 IN. Hg -980 FT to 8200 FT	31 IN. Hg to 23.9 IN. Hg -980 FT to 8200 FT	31 IN. Hg to 23.9 IN. Hg -980 FT to 8200 FT	31 IN. Hg to 23.5 IN. Hg -980 FT to 6560 FT
AIR CLEANLINESS	SAME AS OPERATING WITH PROPER PACKING	SAME AS OPERATING WITH PROPER PACKING	SAME AS OPERATING	PARTICLE SIZE MICRONS: PARTICLES/METER^3 >1: 4×10^7 >1.5: 4×10^6 >5: 4×10^5 SULPHUR DIOXIDE 0.19 PPM MAX
VIBRATION	SEE CURVE C	SEE CURVE C	SEE CURVE B	(1) SEE CURVE A
SHOCK	LBS: 45-175; kg: 21-80; G's: 45; ms: 15	LBS: 45-175; kg: 21-80; G's: 45; ms: 15	HALF SINE WAVE UP TO 3 g's FOR 10 ms 5 ms BETWEEN SHOCKS	(1) HALF SINE WAVE UP TO 2 g's FOR 10 ms NOT MORE THAN 2/SEC
TRANSIENT ENERGY LOSS	NOT APPLICABLE	NOT APPLICABLE	NOT APPLICABLE	ONE PHASE: 50% OF NOMINAL FOR 1/2 CYCLE ONCE IN 10 SEC ALL PHASES: 80% OF NOMINAL FOR 10 CYCLES ONCE IN 60 SEC

(1) EQUIPMENTS SHALL MEET THE FULL SPECIFIED PERFORMANCE WITH THE CONDITIONS INJECTED FROM THE FLOOR IN A VERTICAL DIRECTION.

M127C

TABLE 7. ENVIRONMENTAL REQUIREMENT

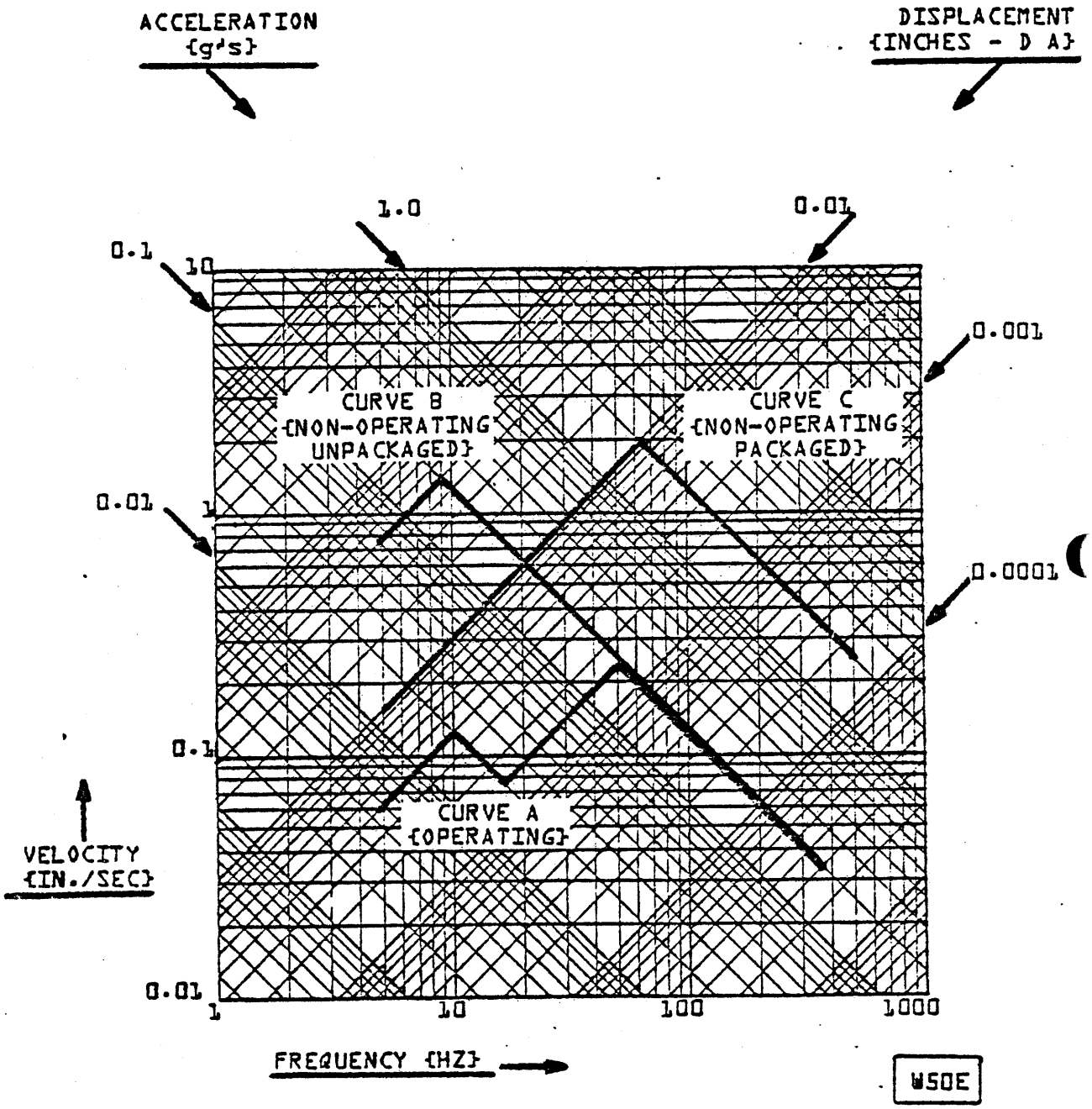
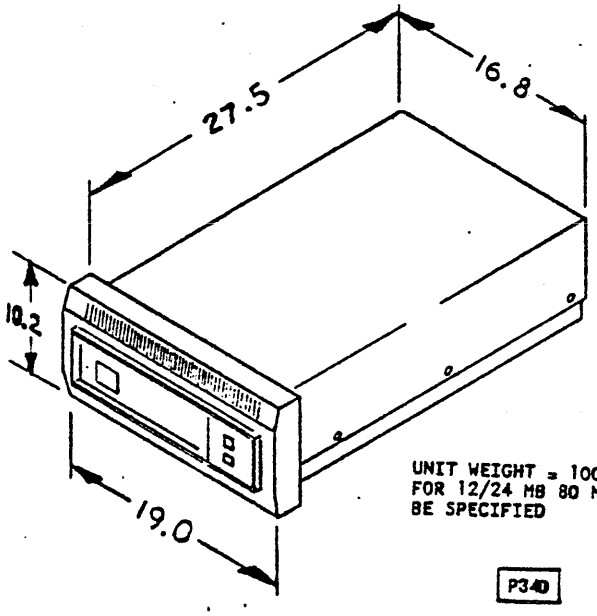


FIGURE 31. VIBRATION LEVELS



UNIT WEIGHT = 100 LBS.
FOR 12/24 MB 80 MB WEIGHT TO
BE SPECIFIED

MMD WITH ENCLOSURE

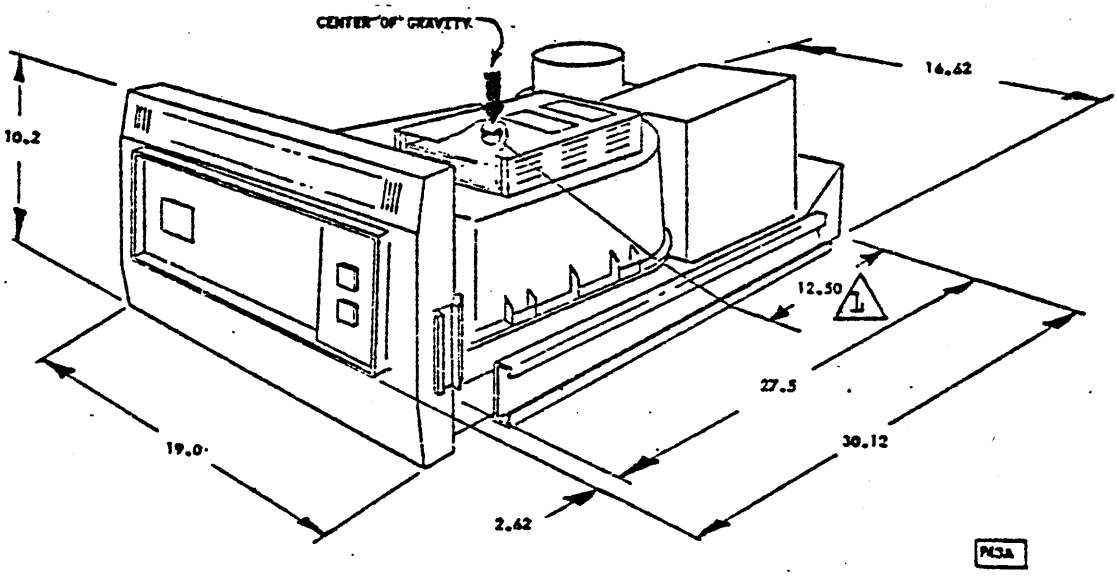


FIGURE 32. PLAN VIEW