Sabre Disc Drive

ST8741J/N, ST8851J/N

ST81123J, ST81154K

ST81236J/K/N

Theory Manual

(All Interfaces)

Seagate

WARNING

Do not attempt to install, operate, or repair the unit, before you read the important safety information located directly after the table of contents in this manual. Failure to follow that and other safety precautions in this manual could cause injury to yourself or others.

WARNING

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of the FCC Rules which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

If the operator or status/control panel (component assembly) is not installed in the inner drawer, it is your responsibility to provide any additional RFI shielding or grounding needed to ensure FCC Class A compliance.

KOR 0756

Sabre Disc Drive

ST8741J (97200-736)
ST8741N (97201-736)
ST8851J (97200-850)
ST8851K (97209-850)
ST8851N (97201-850)
ST81123J (97200-11G)
ST81154K (97229-11G)
ST81236J (97200-12G)
ST81236K (97209-12G)
ST81236N (97201-12G)

Theory Manual
(All Interfaces)

Overview of the Drive
Power and Control Functions
Interface Functions
Servo Surface Decoding
Seek Functions
Read/Write Functions
Detecting and Analyzing Errors

Publication Number: 83325690-E

Seagate

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We value your comments. A Comment Sheet is provided at the back of this manual.

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PREFACE

This manual describes the theory of operation of the Seagate PA8XX SABRE eight-inch module drive. It is prepared for customer engineers and other technical personnel directly involved with maintaining the drive.

The information in this manual is presented as follows:

Section 1 - Overview of the Drive

Section 2 - Power and Control Functions

Section 3 - Interface Functions

Section 4 - Servo Surface Decoding

Section 5 - Seek Functions

Section 6 - Read/Write Functions

Section 7 - Detecting and Analyzing Errors

Section 1 provides a guide to the overall organization of the manual with brief descriptions of each section.

New features, technical changes, additions, and deletions in this manual are indicated as follows:

- A vertical bar in the outer margin of a page marks the changed area.
- A dot by the page number indicates the entire page contains new or changed information.
- A vertical bar by the page number indicates the information was moved from another page, but there were no technical or editorial changes.

The following manuals apply to the SABRE and are available from:

Seagate Technology, Inc.
Customer Services
12701 Whitewater Drive
Minnetonka, MN 55343

Phone: (612) 931-8612
Fax: (612) 931-8817

Publication No.	Title
83325660	Reference Card (summarizes status codes and diagnostic operation for drives with the SMD and IPI interfaces)
83325690	PA8XX Theory Manual
83325700	PA8XX Parts Data Manual (contains listings of field replaceable parts, manufacturer's recommended spare parts, and accessories)
83325710	PA8G1/PA8G2/PA8K1/PA8K2/PA8N1/PA8N2/PA8W2 User's Manual (contains general description, operation, installation and checkout information)
83325720	PA8XX Maintenance Manual
83325730	PA8XX Diagrams Manual
83325810	Reference Card (summarizes status codes and diagnostic operation for drives with the SCSI interface)
83325860	PA8H1/PA8L1/PA8P1/PA8P3 User's Manual (contains general description, operation, installation and checkout information)
83326010	PA8M2/PA8R2/PA8Y2 User's Manual (contains general description, operation, installation and checkout information)
83327150	Special Supplement (applies to PA8K2D)
83327160	Special Supplement (applies to half-rack mounting kit)

For more information about the interfaces described in this manual, you can request copies of interface specifications from your Seagate sales representative. The following specifications are available:

Specification No.	Title
64712402	SMD-E Interface Specification
64721701	Interface Specification for the MPI Small Computer System Interface (SCSI)
64731600	Interface Specification for IPI-2 Intelligent Peripheral Interface

The following table lists the drives covered by this manual:

Equipment Number	Interface	Data Capacity (MB)	Sector Length
PA8G1A	Single Channel SMD	736	Unspecified
PA8G2A	Dual Channel SMD	736	Unspecified
PA8G2C*	Dual Channel SMD	736	Unspecified
PA8G2D	Dual Channel SMD	736	Unspecified
PA8H1A	STD SCSI (Differential)	736	512 Bytes
PA8H1B	STD SCSI (Single-ended)	736	512 Bytes
PA8H1C	STD SCSI (Differential)	736	256 Bytes
PA8H1D	STD SCSI (Single-ended)	736	256 Bytes
PA8H1E	STD SCSI (Differential)	736	512 Bytes
PA8K1A	Single Channel SMD	850	Unspecified
PA8K2A	Dual Channel SMD	850	Unspecified
PA8K2D	Dual Channel SMD	850	Unspecified
PA8K2E*	Dual Channel SMD	850	Unspecified
PA8K2F*	Dual Channel SMD	850	Unspecified
PA8K2H	Dual Channel SMD	850	Unspecified
PA8K2J	Dual Channel SMD	850	Unspecified
PA8L1A	STD SCSI (Differential)	850	512 Bytes
PA8L1B	STD SCSI (Single-ended)	850	512 Bytes
PA8L1C	STD SCSI (Differential)	850	256 Bytes

* This drive has an optional voltage converter to permit operation with a power supply providing fewer output voltages than the standard supply.

Continued

Equipment Number	Interface	Data Capacity (MB)	Sector Length
PA8L1D	STD SCSI (Single-ended)	850	256 Bytes
PA8L1E	STD SCSI (Differential)	850	512 Bytes
PA8L1K	STD SCSI (Single-ended)	850	512 Bytes
PA8M2A	IPI	850	Std Format
PA8M2B	IPI	850	512 Bytes
PA8M2C	IPI	850	1024 Bytes
PA8M2D	IPI	850	Std Format
PA8N1A	Single Channel SMD	1230	Unspecified
PA8N1B	Single Channel SMD	1230	Unspecified
PA8N2A	Dual Channel SMD	1230	Unspecified
PA8N2B*	Dual Channel SMD	1230	Unspecified
PA8N2C	Dual Channel SMD	1230	Unspecified
PA8N2D	Dual Channel SMD	1230	Unspecified
PA8N2E	Dual Channel SMD	1230	Unspecified
PA8N2F	Dual Channel SMD	1230	Unspecified
PA8N2G	Dual Channel SMD	1230	Unspecified
PA8P1A	HP SCSI (Differential)	1230	512 Bytes
PA8P1B	HP SCSI (Single-ended)	1230	512 Bytes
PA8P1C	HP SCSI (Differential)	1230	256 Bytes
PA8P1D	HP SCSI (Single-ended)	1230	256 Bytes
PA8P1E	HP SCSI (Differential)	1230	512 Bytes
PA8P1F	HP SCSI (Differential)	1230	512 Bytes
PA8P1G	HP SCSI (Differential)	600	256 Bytes
PA8P1H	HP SCSI (Single-ended)	1230	512 Bytes

* This drive has an optional voltage converter to permit operation with a power supply providing fewer output voltages than the standard supply.

Continued

Equipment Number	Interface	Data Capacity (MB)	Sector Length
PA8P3A	HP SCSI (Differential)	1230	256 Bytes
PA8P3B	HP SCSI (Differential)	1230	512 Bytes
PA8P3C	HP SCSI (Differential)	1230	256 Bytes
PA8P3D	HP SCSI (Differential)	600	512 Bytes
PA8R2A	IPI	1230	Std Format
PA8R2B	IPI	1230	512 Bytes
PA8R2C	IPI	1230	1024 Bytes
PA8R2D	IPI	1230	288 Bytes
PA8R2E	IPI	1230	2308 Bytes
PA8W2A	Dual Channel SMD	1120	Unspecified
PA8W2B*	Dual Channel SMD	1120	Unspecified
PA8W2C	Dual Channel SMD	1120	Unspecified
PA8W2D	Dual Channel SMD	1120	Unspecified
PA8Y2A	IPI (2-Head Parallel)	1153	

* This drive has an optional voltage converter to permit operation with a power supply providing fewer output voltages than the standard supply.

CONTENTS

FIGURES

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IMPORTANT SAFETY INFORMATION AND PRECAUTIONS

Use of proper safety and repair techniques is important for safe, reliable operation of this unit. Service should be done only by qualified persons. We recommend the procedures in this manual as effective ways of servicing the unit. Some procedures require the use of special tools. For proper maintenance and safety, you must use these tools as recommended.

The procedures in this manual and labels on the unit contain warnings and cautions that must be carefully read and followed to minimize or eliminate the risk of personal injury. The warnings point out conditions or practices that may endanger you or others. The cautions point out conditions or practices that may damage the unit, possibly making it unsafe for use.

You must also understand that these warnings and cautions are not exhaustive. We cannot possibly know, evaluate, and advise you of all the ways in which maintenance might be performed or the possible risk of each technique. Consequently, we have not completed any such broad evaluation. If you use a non-approved procedure or tool, first ensure that the method you choose will not risk either your safety or unit performance.

For the safety of yourself and others, observe the following warnings and precautions.

- Perform all maintenance by following the procedures in this manual.
- Follow all cautions and warnings in the procedures and on unit labels.
- Use the special tools called out in the procedures.
- Use sound safety practices when operating or repairing the unit.
- Use caution when troubleshooting a unit that has voltages present. Remove power from unit before servicing or replacing parts.
- Wear safety glasses when servicing units.
- Wear safety shoes when removing or replacing heavy parts.
- Use only designated Seagate replacement parts. Non-Seagate replacement parts can adversely affect safety in addition to degrading reliability, increasing maintenance downtime, and voiding warranty coverage.

(continued on next page)

- Use care while working with the power supply because line voltages are always present when the ac power cord is connected to a power source. Setting the power supply switch to Standby (⏻) disables dc power to the drive but has no effect on ac power within the supply. For complete safety, remove the ac power plug from the site power outlet.

- In case of fire or other emergency, isolate the drive from main power by removing the drive power plug from the ac outlet. In situations where pulling the plug is not possible or practical, use the system main power disconnect to isolate the drives from main power.

- When the drive is mounted in an equipment rack or cabinet, ensure that the internal temperature of the rack or cabinet will not exceed the limits defined for the drive. Where units are stacked vertically, pay special attention to the top where temperatures are usually highest.

- This drive is designed to be installed and operated in accordance with IEC380, IEC435, VDE805, VDE806.

- Follow the precautions listed under Electrostatic Discharge Protection.

- If the power supply is placed on a bench for testing, position the supply so all ventilation holes are open, to allow proper air flow to internal components.

- Do not attempt to disassemble the module. It is not field repairable. Replace the entire module assembly if it is defective.

- Do not operate the drive over an extended period of time without the top cover installed.

- If the power supply is connected to an IT network, ensure that the input voltage is limited to 230 volts.

- Do not attempt to disassemble the power supply. It is not field repairable. Replace the entire supply if it is defective.

- Always deenergize drive before removing or installing circuit boards, cables, or any other electrical components.

- If you do not use a recommended Imprimis power supply, ensure that the supply meets the specifications in this manual and is designed to be used in accordance with IEC380, IEC435, VDE805, VDE806.

ABBREVIATIONS

A	Ampere
ABV	Above
ac	Alternating Current
ADD	Address
ADDR	Address
ADJ	Adjust
ADRS	Address
AGC	Automatic Gain Control
ALT	Alternate
AM	Address Mark
AME	Address Mark Enable
AMP	Amplifier, Ampere
ASSY	Assembly
BLW	Below
C	Celsius
CB	Circuit Breaker
CDA	Complete Drive Assembly
CDIC	Controller/Drive Interface Chip
CH	Channel
CHK	Check
CLK	Clock
CLR	Clear
cm	Centimetre
CNTR	Counter
COMP	Comparator
CONT	Control
CONTD	Continued
CT	Center Tap
CYL	Cylinder
D/A	Digital to Analog
DAC	Digital-to-Analog Converter
dc	Direct Current
DET	Detect
DIFF	Differential
DIV	Division
DLY	Delay
DMA	Direct Memory Access
DRVR	Driver
ECC	Error Correction Code
ECL	Emitter Coupled Logic
ECO	Engineering Change Order

ABBREVIATIONS (Contd)

EMD	Eight-Inch Module Drive
EN	Enable
ENBL	Enable
ESP	Enhanced SCSI Protocol
EXT	External
F	Fahrenheit, Fuse
FCO	Field Change Order
FDBK	Feedback
FIG	Figure
FLT	Fault
FRU	Field Replaceable Unit
ft	Foot
FWD	Forward
GND	Ground
HD	Head
HEX	Hexagon, Hexadecimal
Hg	Mercury
HP	High Performance
HR	High Resolution
HYST	Hysteresis
Hz	Hertz
IC	Integrated Circuit
ID	Identification
IDENT	Identification
in	Inch
IND	Index
INTRPT	Interrupt
I/O	Input/Output
IPB	Illustrated Parts Breakdown
IPC	Interface Protocol Circuit
IPI	Intelligent Peripheral Interface
IPIP	IPI Parallel
kg	Kilogram
kW	Kilowatt
lb	Pound
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
LSI	Large Scale Integration
LTD	Lock to Data
m	Metre
MAC	Merged Architecture Controller

ABBREVIATIONS (Contd)

MAX	Maximum
MB	Megabyte
MEM	Memory
MHz	Megahertz
mm	Millimetre
MPU	Microprocessor Unit
MRK	Mark
ms	Millisecond
MSB	Most Significant Bit
MTR	Motor
mV	Millivolt
NC	No Connection
NORM	Normal
NRZ	Non Return to Zero
ns	Nanosecond
OC	On Cylinder
OS	One-Shot
OSC	Oscillator
P	Plug
PD	Peak Detect
pF	Picofarad
PFTU	Programmable Field Test Unit
PG	Page
PLO	Phase Lock Oscillator
PROC	Procedure
PROG	Programmable
PS	Power Supply
PWR	Power
RCVR	Receiver
RD	Read
RDY	Ready
RECT	Rectified
REF	Reference
REQ	Request
RES	Resolution
REV	Reverse, Revision
RGTR	Register
r/min	Revolutions Per Minute
RPS	Rotational Position Sensing
RTZ	Return to Zero
R/W	Read/Write
s	Second
SBC	SCSI Bus Controller
S/C	Series Code

ABBREVIATIONS (Contd)

SCSI	Small Computer System Interface
SEL	Select
SEQ	Sequence
SFC	SERDES Formatter Circuit
SPD	Speed
SS	Sector Switch
STD	Standard
SYNC	Synchronization
T	Tracks to go
TIM	Timer
TP	Test Point
TTL	Transistor-Transistor Logic
V	Volts, Voltage
Vbb	Bias Voltage
VCC	Bias Voltage
VCO	Voltage Controlled Oscillator
W	Watts
W/	With
W/O	Without
W P	Write Protect
W+R	Write or Read
W·R	Write and Read
WRT	Write
XFR	Transfer
Ω	Ohms
$	Hexadecimal Address
µF	Microfarad
µs	Microsecond
2HP	Two-Head Parallel

SECTION 1

OVERVIEW OF THE DRIVE

OVERVIEW OF THE DRIVE 1

INTRODUCTION

The theory manual describes drive operations and the hardware used in performing them. This section describes what the drive does in its operation, and the remaining sections discuss how it operates.

Each section in this manual describes a general function of the drive. Some of the functions are ongoing -- others are called upon for particular operations. In fact, all operations involve more than one of the functions.

This section provides a link between understanding the drive functions and the drive operations. It contains the following topics:

- Drive Functional Description -- Shows the organization of the remaining sections in the manual.
- Summary of Drive Operations -- Describes each drive operation with references to other sections of the manual.
- How to Use This Manual -- Lists special symbols and terminology used in this manual.

DRIVE FUNCTIONAL DESCRIPTION

The individual functions of the drive are shown in figure 1-1 and described in this manual as follows:

Section 2, Power and Control Functions, describes the following:

- The roles of the microprocessors in the drive
- What happens when dc power is applied to the drive
- What happens when dc power is removed from the drive
- How disk rotation is controlled and why proper rotational speed is essential for flying the heads above the disks
- How the drive components are kept cool and air in the module is kept clean

Section 3, Interface Functions, uses separate subsections to discuss the individual interface types covered in this manual (SMD, SCSI, and IPI). Each subsection describes the following:

- The signal lines connecting the controller and the drive*
- How unit selection enables one (or two) controller(s) to select one drive from a group of drives for an operation
- How the drive responds to commands from the controller
- How data is transferred between the controller and drive
- How the drive sends status to the controller

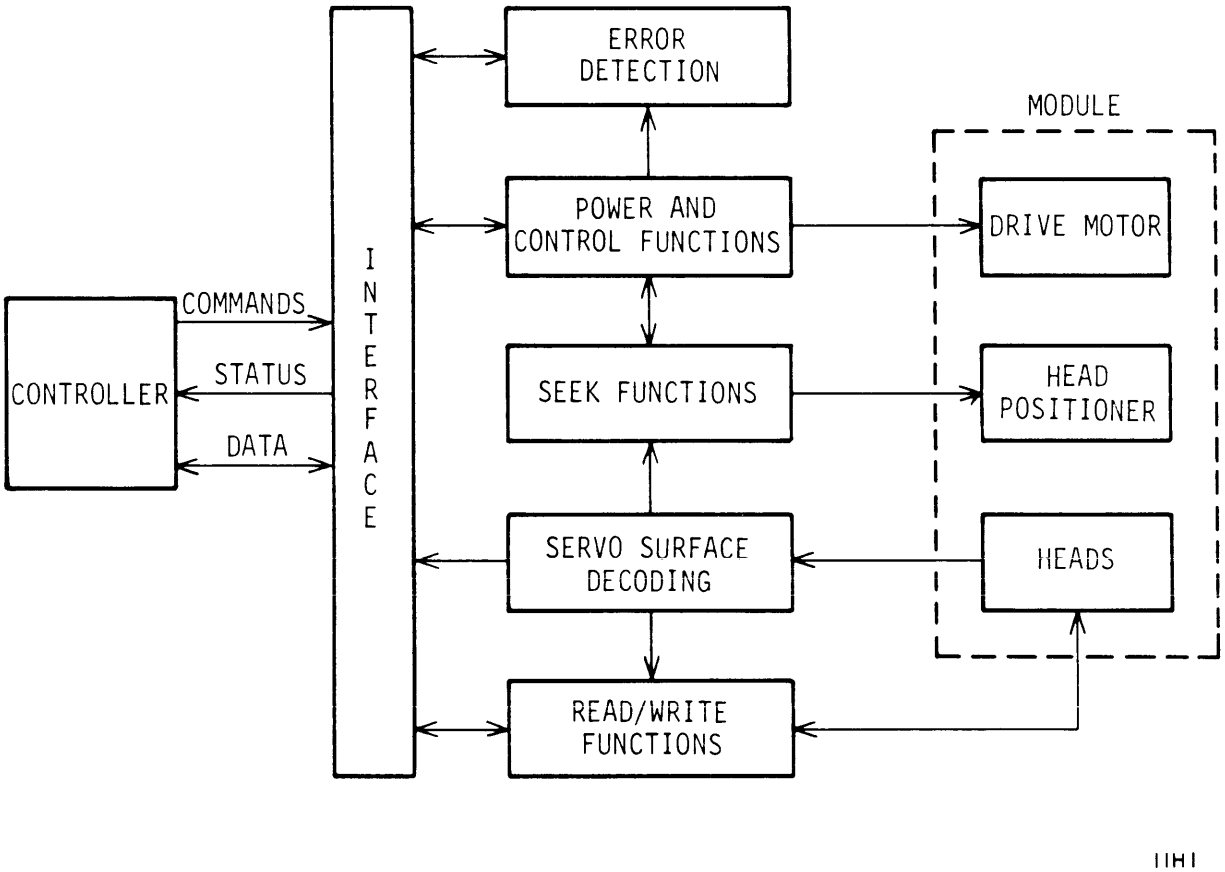

Figure 1-1. Drive Functional Block Diagram

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* Throughout this manual the terms "controller" and "drive" refer to the units connected by the interface cable. SCSI interface drives (which have controller functions) use different terminology, discussed at the end of this section.

Section 4, Servo Surface Decoding, describes the following:

- How information is recorded on the servo surface
- How this information provides servo signals that locate the radial position of the heads
- How this information provides timing signals that synchronize other drive functions to the disk rotation
- How this information provides interface signals that locate the rotational position of the heads relative to the disks

Section 5, Seek Functions, describes the following:

- How the servo circuits develop control signals that change or maintain the position of the heads
- How the positioning mechanism in the module responds to these control signals
- The sequencing of events during each type of head movement

Section 6, Read/Write Functions, describes the following:

- How the heads transfer data to and from the disks
- How a head is selected prior to a data transfer
- How the drive processes data in a write operation (a data transfer to the disk)
- How the drive processes data in a read operation (a data transfer from the disk)

Section 7, Detecting and Analyzing Errors, describes the following:

- How and why fault and error indications appear
- How the drive responds to system or operator actions after an error has occurred
- How the operator and status/control panels transfer information to and from other circuits in the drive
- How the drive operates during diagnostic testing.

SUMMARY OF DRIVE OPERATIONS

Transfers of data from the host system to a disk and later retrievals of data from a disk to the host system are the primary operations of a disk drive. There are other important operations that prepare the disk drive for a data transfer. Some of these operations are ongoing and others occur when the drive receives commands from the controller.

In the following topics, numbers in parentheses indicate sections of this manual where you can find additional information.

ONGOING OPERATIONS

The drive receives dc power when the power supply On/Standby switch is set in the On position. After receiving dc power, the drive does the following:

- It initializes its microprocessors (2)
- It constantly monitors its power supply voltages (7) and microprocessor activity (2, 7) to react to any error conditions that may occur.
- It waits for start conditions.

When start conditions become available (2, 3), the following sequence occurs:

- The motor control circuitry brings the drive motor up to speed (2).
- The drive motor rotates the disks, and as the disks rotate faster, the heads are lifted from the landing zones, where they were in contact with the disks.
- With the disks up to speed, the carriage latch unlocks the heads and the servo system loads them, moving them from the landing zone to the data zone (5) and calibrating itself.
- When the load operation is complete, the controller gets a ready indication (3) and the drive waits for further commands.

While the drive is ready, it maintains several ongoing operations:

- The motor control circuitry continues to control motor rotation and notifies other drive circuits if there is a motor speed problem (2, 5).
- The servo circuitry holds the heads at their current location until commanded to move them (5).
- If problems develop with servo positioning or motor speed, they are detected and relayed to the controller (7).

COMMANDED OPERATIONS

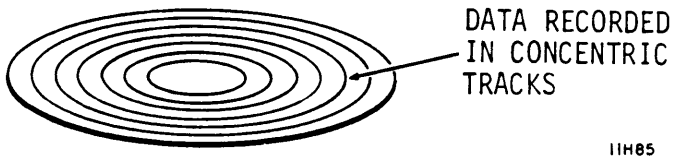
Data transfer and the functions that lead up to it are performed under the direction of the controller. Here are some typical operations.

Start — The controller may start the drive motor and cause the heads to load, depending on how the drive is configured (2). Some drives are set up to do this independent of the controller. The controller must receive a ready indication (3) before proceeding with other operations.

Select a Drive — The drive must be selected before it will respond to other commands from the controller. The controller selects the drive by transmitting the drive's logical address on the interface (3). The drive returns selected status on the interface (3). Some drives also provide rotational position information to the controller as long as they remain selected (4).

Select a Cylinder — After the controller has selected the unit with which it wishes to perform an operation, it must then direct the drive to the specific location on the data recording surface where it wants the operation to be performed (3).

The disks are mapped into narrow concentric bands called tracks that cover the entire circumference of the circle. The tracks are then further subdivided into equal areas called sectors. The collection of all tracks in the same vertical plane is termed a cylinder.



The operation of positioning the heads over the desired track is called a seek operation. A seek moves the heads from their current cylinder address to a new cylinder address. The drive servo system performs the seek operation (5) by using information read from the servo surface by the servo head (4). When the seek operation is completed, the drive returns on cylinder status to the controller (3).

Select a Head — Once a particular cylinder is selected, the controller then issues a head selection command. The drive addresses one of the heads located at the selected cylinder (6). The head is an electromagnetic device that transfers data to and from the disk.

Wait for a Sector — After selecting a head and arriving at the data track, the controller must locate that portion of the track where the data is to be written or read. This is called track orientation and is done by using the Index and Sector signals generated by the drive (4). The Index signal indicates the logical beginning of each track. The Sector signals are used by the controller to determine the position of the head on the track with respect to Index.

Transfer the Data — When the desired location is reached, the controller commands the drive to actually read or write the data. During a read operation, the drive recovers data from the disks (6) and transmits it to the controller (3). During a write operation, the drive receives data from the controller (3), processes it and writes it on the disks (6).

Watch for Problems — The drive is also capable of recognizing certain errors that may occur during its operation (7). When an error is detected, it is indicated either by a signal to the controller or by a maintenance indicator on the drive itself.

Stop — When start conditions are removed (either by the controller or drive operator), the servo system retracts the heads to the landing zone and a mechanical latch locks them there (5). Once the heads are retracted, the motor control circuitry applies reverse current to the drive motor to stop it (2). The drive remains in this state until either start conditions reappear or dc power is removed.

HOW TO USE THIS MANUAL

The descriptions in this manual are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in the diagrams manual should take precedence over those in this manual if there is a conflict between the two.

The four-digit numbers in parentheses that are used on the simplified logic diagrams are logic diagram cross reference numbers. They indicate the logic page(s) where the function or operation can be found. In cases where older and newer circuit boards have different cross reference numbering, the cross references in this manual apply to the newer boards. If an X appears in a cross reference number (5X03), that number represents different specific numbers (5103, 5203, 5303, etc.) for different series of drives.

All references in this manual to the optional operator panel apply to both the status/control panel and the operator panel. The status/control panel has a maintenance keyboard in addition to the switches and indicators found on the simpler operator panel. References in this manual to the status/control panel cover that panel's unique features and do not apply to the simpler operator panel.

Terminology problems arise in discussing disk drives with the SCSI interface at the same time as disk drives with other interfaces. For drives with the SCSI interface, the I/O board includes a SCSI controller, and the SCSI interface cable allows communications between the drive (or "target") and host (or "initiator"). For drives with other interfaces, the controller is a unit in the subsystem that communicates between the host and the drive interface.

Unless the SCSI interface is being discussed specifically, this manual will use the term controller to refer to the external unit that connects via the interface cable to the disk drive. The controller portion of the SCSI I/O circuitry will always be called the SCSI controller. The term device will be used to refer to the SCSI disk drive minus the SCSI I/O board.

SECTION 2

POWER AND CONTROL FUNCTIONS

POWER AND CONTROL FUNCTIONS 2

INTRODUCTION

This section describes control functions internal to the drive. These control functions start when dc power is applied to the drive. Depending on other inputs, they initiate power on and power off sequences. Discussion of these processes is divided into the following areas:

- Microprocessor Control System Functions -- Describes the roles of the drive's three microprocessors.
- Power Functions -- Describes distribution of dc power, power on sequencing, and power off sequencing.
- Disk Rotation and Head Loading -- Describes motor speed control and head movement.
- Drive Ventilation -- Describes air circulation around drive components and inside the module.

MICROPROCESSOR CONTROL SYSTEM FUNCTIONS

The three microprocessors in the microprocessor control system control all of the major operations of the drive except head selection and read/write functions. All operations in the microprocessor control system are performed under the direction of firmware for the Control MPU.

A description of the operations performed by the Motor MPU firmware can be found later in this section. Detailed descriptions of the operations performed by Servo MPU firmware can be found in section 5 under Servo Circuit Functions.

All functions performed by the control firmware, except drive initialization, are interrupt-driven. Three interrupt routines are provided:

- Timer interrupt
- I/O interrupt
- Servo interrupt.

At the conclusion of initialization, the program enables the three interrupt routines and then branches to an idle routine to wait for an interrupt. Interrupt priority is as follows:

1. servo interrupt
2. timer interrupt
3. I/O interrupt.

If two interrupts are received at the same time, the higher priority interrupt is serviced first. After processing the interrupt, the control program returns to the idle routine.

TIMER INTERRUPT

The timer interrupt routine is divided into eight sections, and one section is executed at each timer interrupt. The routine generates an interrupt every 3.75 milliseconds. Execution sequence is fixed to ensure that each section is repeated every 30 milliseconds.

Figure 2-1 shows how the timer interrupt monitors and controls various functions in the drive. In this diagram, functional areas relating to the timer interrupt are shaded. The timer interrupt routine has the following functions:

- It polls the switches on the operator panel or status/control panel
- It checks the Motor MPU
- It starts and stops the drive motor and loads and unloads the heads (power sequencing)
- It checks the Servo MPU
- It triggers the hang-detect one-shot for the Control MPU
- It initiates diagnostic tests
- It updates the liquid crystal display and LEDs on the status/control panel (LEDs on the operator panel)
- It directs sweep cycle activities. If the sweep cycle feature is enabled, the Control MPU periodically takes the drive offline (when idle) and moves the heads to various regions of the disks.

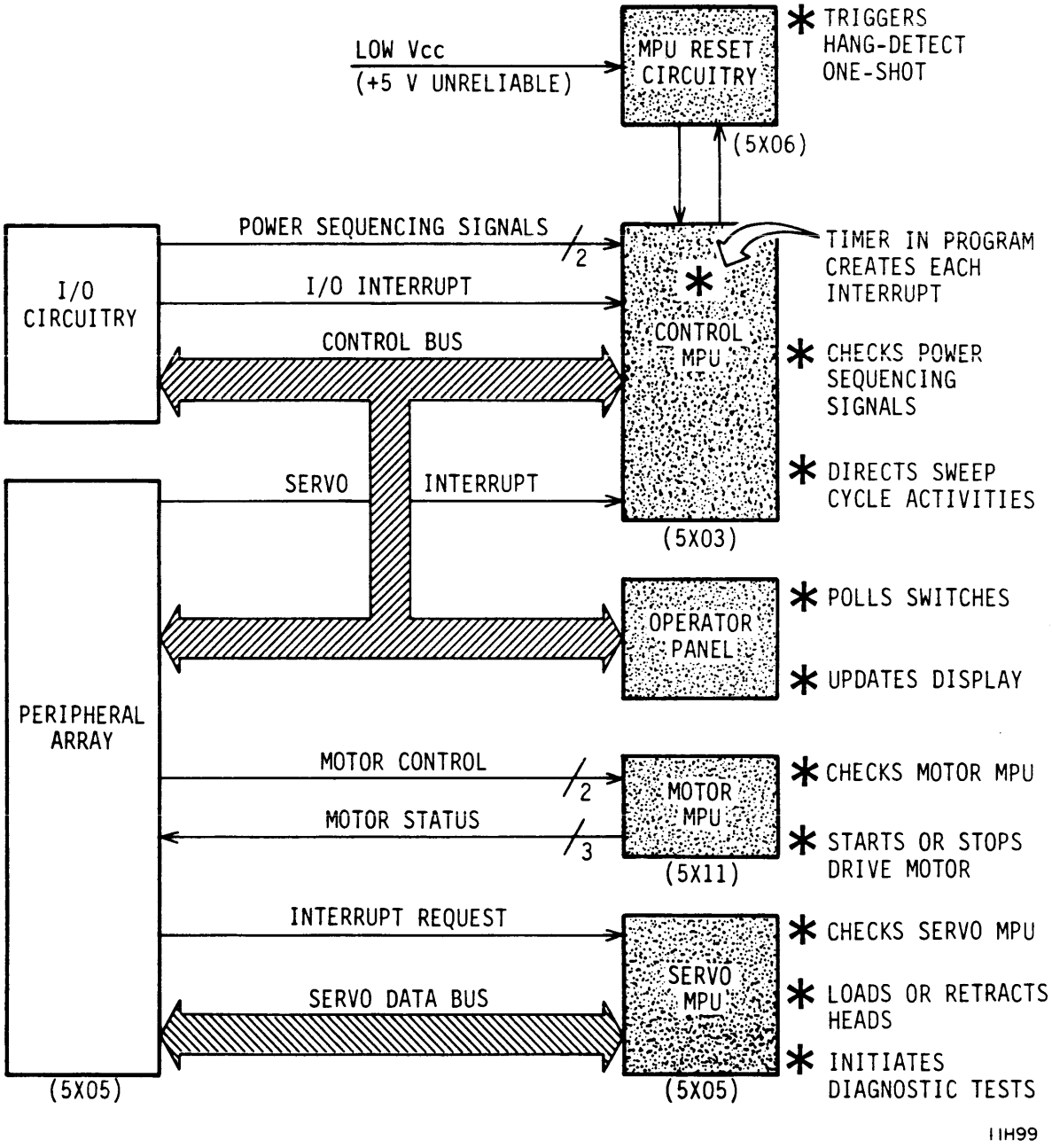


Figure 2-1. Control MPU and its Timer Interrupt

I/O INTERRUPT

The I/O interrupt routine is used to process commands from the controller that require microprocessor assistance. Figure 2-2 shows how the I/O interrupt monitors and controls various functions in the drive. In this diagram, functional areas relating to the I/O interrupt are shaded.

The routine is divided into five sections to handle the following types of interrupt requests: RTZ, seek, offset, execute diagnostics, and status request (operating and diagnostic status). Those sections that initiate servo operations all operate by sending a command (and operand, if required) to the Servo MPU and then waiting for a response.

The I/O interrupt routine monitors the time required for these servo operations and stops them if they take too long to complete. Finally, the routine determines whether the servo operation completed successfully, and then sends the appropriate signal to the controller.

As a precondition, normal seek, RTZ, and offset commands require unit ready status. An execute diagnostics command can be requested only when the motor is up to speed and the unit is ready (heads loaded). A status request (operating and diagnostic status) can be issued at any time.

SERVO INTERRUPT

The servo interrupt routine is used to process status responses from the Servo MPU to the Control MPU. Following a command by the Control MPU to perform a servo operation, the Servo MPU sends status to the Control MPU to tell it if the operation was completed successfully.

Figure 2-3 shows how the Control MPU receives a servo interrupt from the Servo MPU via the Peripheral Array.

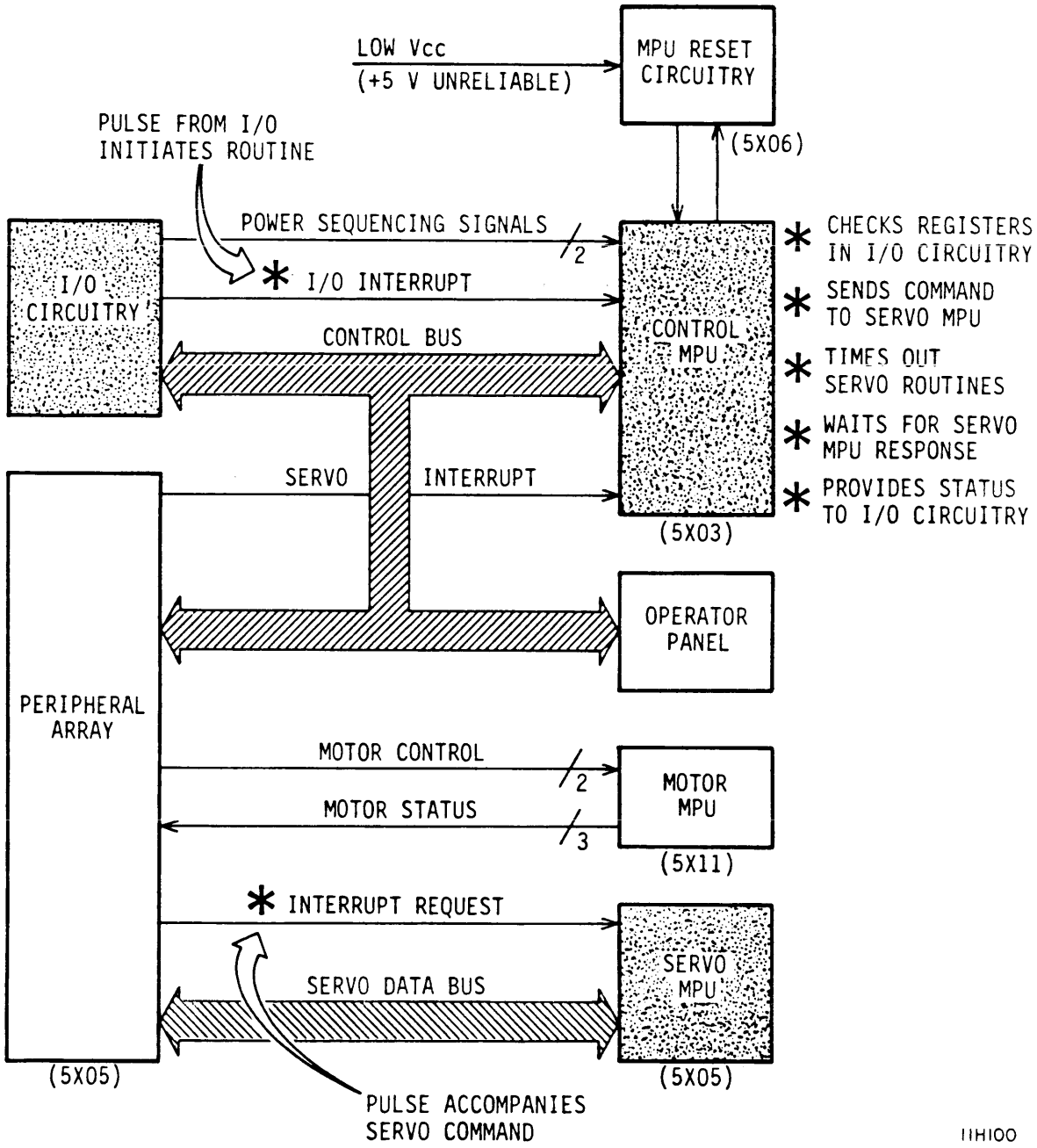


Figure 2-2. Control MPU and its I/O Interrupt

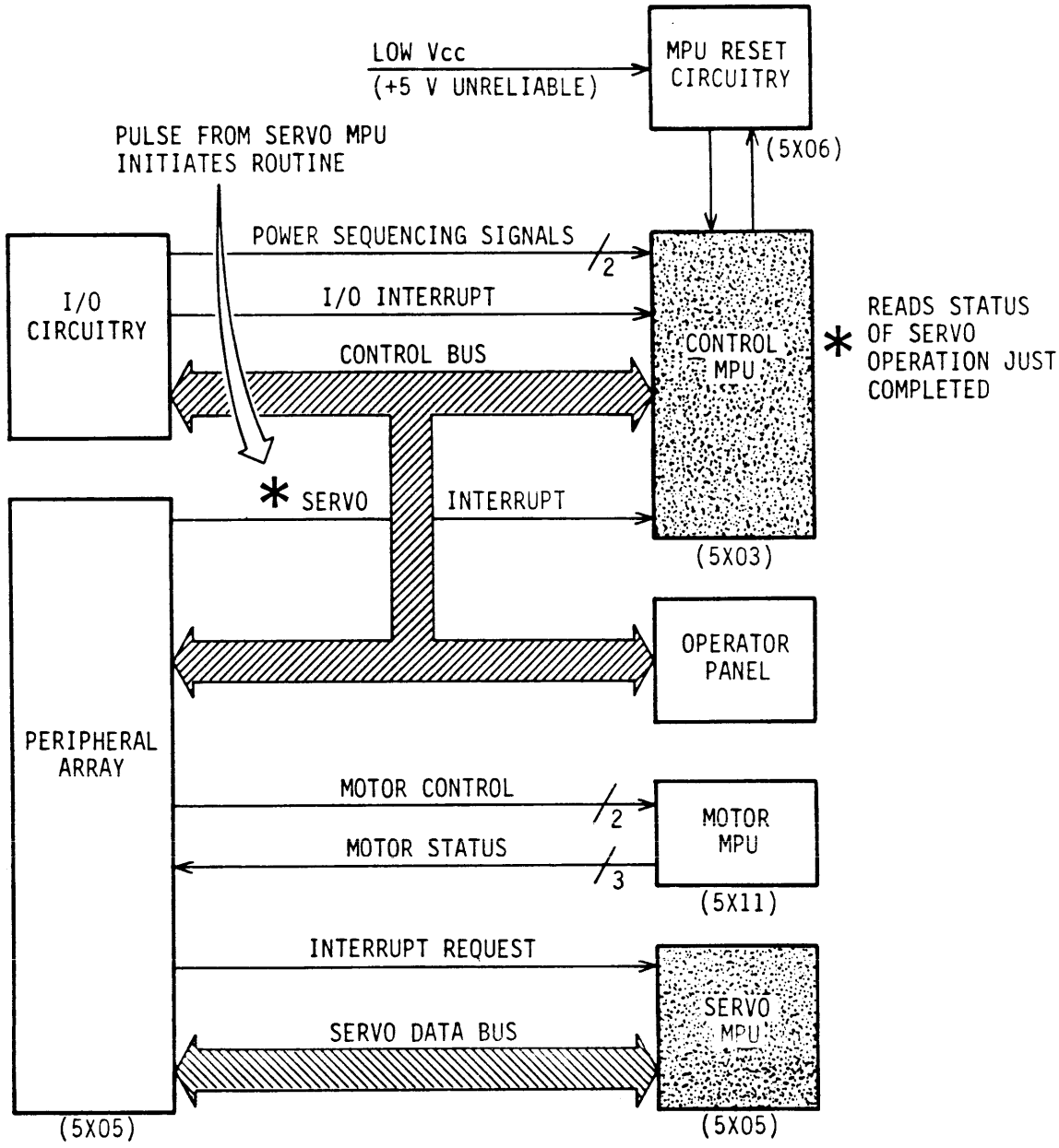


Figure 2-3. Control MPU and its Servo Interrupt

POWER FUNCTIONS

Power functions are processes that take place within the power supply and the drive when the drive is powered on and powered off. The power on and power off sequences are directed by the Control MPU, which monitors whether start conditions are present and whether certain interlock and operating conditions are satisfactory. The following areas of the power functions will be discussed in detail:

- Power Distribution -- Describes how power is distributed to the drive circuitry.
- Power On Sequence -- Describes how the drive circuitry is initialized when power is applied and how the drive is prepared for normal operation.
- Power Off Sequence -- Describes how the drive is powered off, including unloading the heads and stopping the disk rotation.

POWER DISTRIBUTION

The power supply provides the drive with basic dc supply voltages shown in figure 2-4. The drive itself has no ac power requirements. All drive components, including the logic, cooling fan (optional), and drive motor, are supplied with dc power. The ac power cable connects the power supply to site ac power. The power supply can be conditioned for operation with any standard ac input voltage, as described in the installation and checkout section of the user's manual.

The dc power cable connects the power supply to the drive. When the On/Standby (1/0) switch is On (1), this cable transmits four basic dc supply voltages to the drive electronics. These voltages are +5 V, -5 V, +24 V, and -12 V. Some drives are configured to operate with three basic dc supply voltages (+5 V, +24 V, and -12 V). These drives have a voltage converter mounted in front of the fan on the rear panel. The voltage converter develops a -5 V source from the -12 V input.

The optional power supply has both overcurrent and overvoltage protection. All dc voltages are overcurrent-protected. Overcurrent on the +24 volt source causes the power supply to shut down. However, overcurrent on the -12 volt source does not cause the power supply to shut down. Overcurrent on either the +5 volt or -5 volt source causes a reduction to zero current or a shutdown of the power supply.

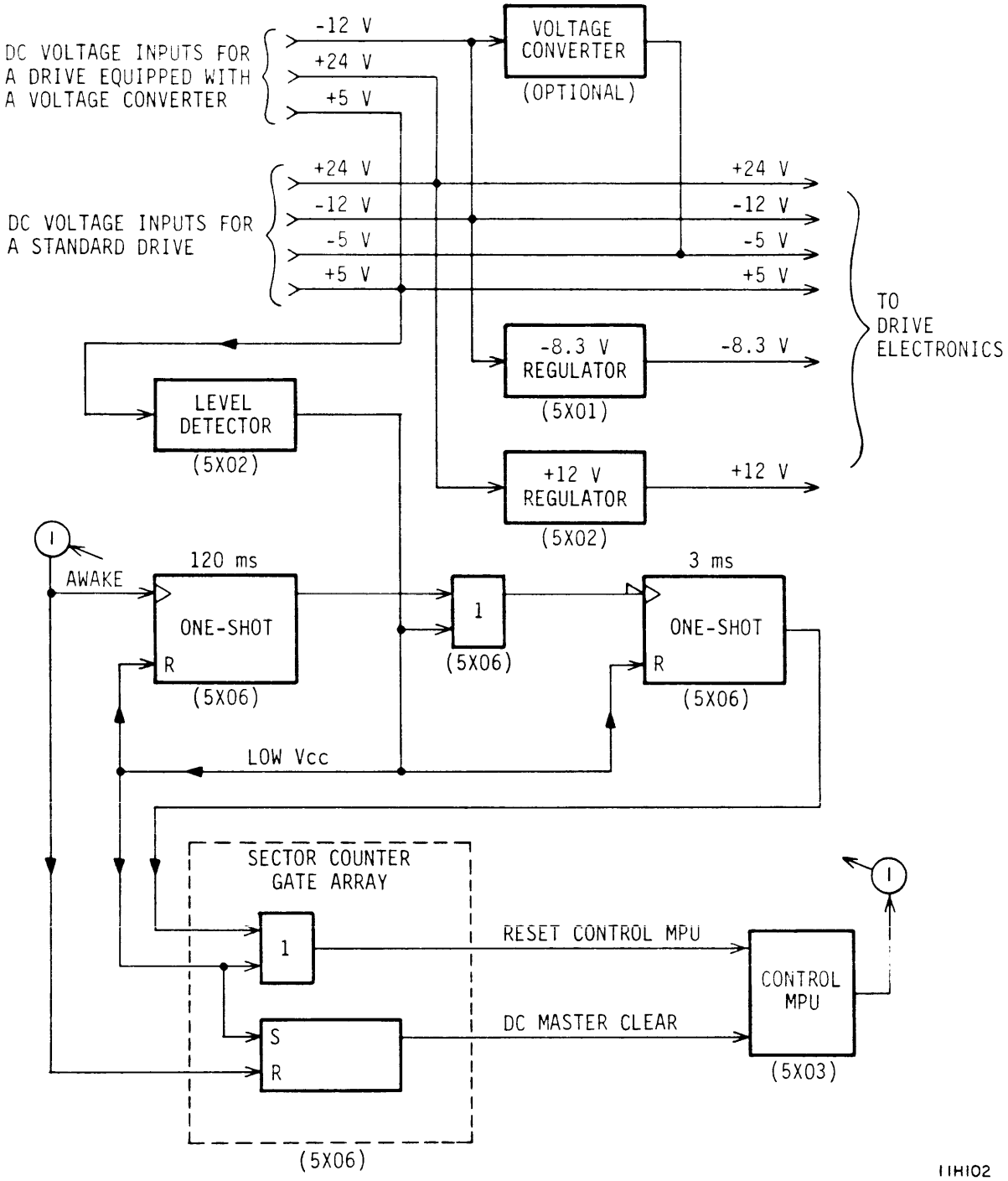


Figure 2-4. Power Distribution and MPU Reset

Operation resumes without manual intervention after correction of an overcurrent condition. An overvoltage condition on either the +5 volt or -5 volt output causes the power supply to shut down. Operation resumes without manual intervention after correction of an overvoltage condition.

There are three secondary power supplies on the control board that develop additional bias voltages for certain integrated circuits. One supply steps down the +24 V input and develops a regulated +12 V source. Another supply steps down the -12 V supply to develop a regulated bias of -8.3 V for the servo preamp chip. The third supply provides a +10 V reference for the voltage fault comparators.

The drive has circuitry that monitors the various supply voltages and disables write and/or servo functions when dc power is unreliable. For more information about voltage faults, refer in section 7 to How Errors are Detected.

POWER ON SEQUENCE

The power on sequence takes place in the following steps:

- Power On Initialization -- describes what happens when dc power is applied to the drive.
- Power Sequencing -- explains how each interface type may provide a delay between power on initialization and the beginning of the load operation.
- Load Operation -- summarizes what happens each time that start conditions become available. For more information, see Types of Seeks in section 5.

Power On Initialization

Regardless of interface type, the control board circuitry has the same response when dc power is applied to the drive. For certain interfaces, the I/O board goes through its own initialization.

Control Board Initialization

Applying dc power to the drive resets its circuitry and initiates self-tests. Refer back to figure 2-4 to see how the reset signal is activated. Figure 2-5 is a flowchart of the power on sequence.

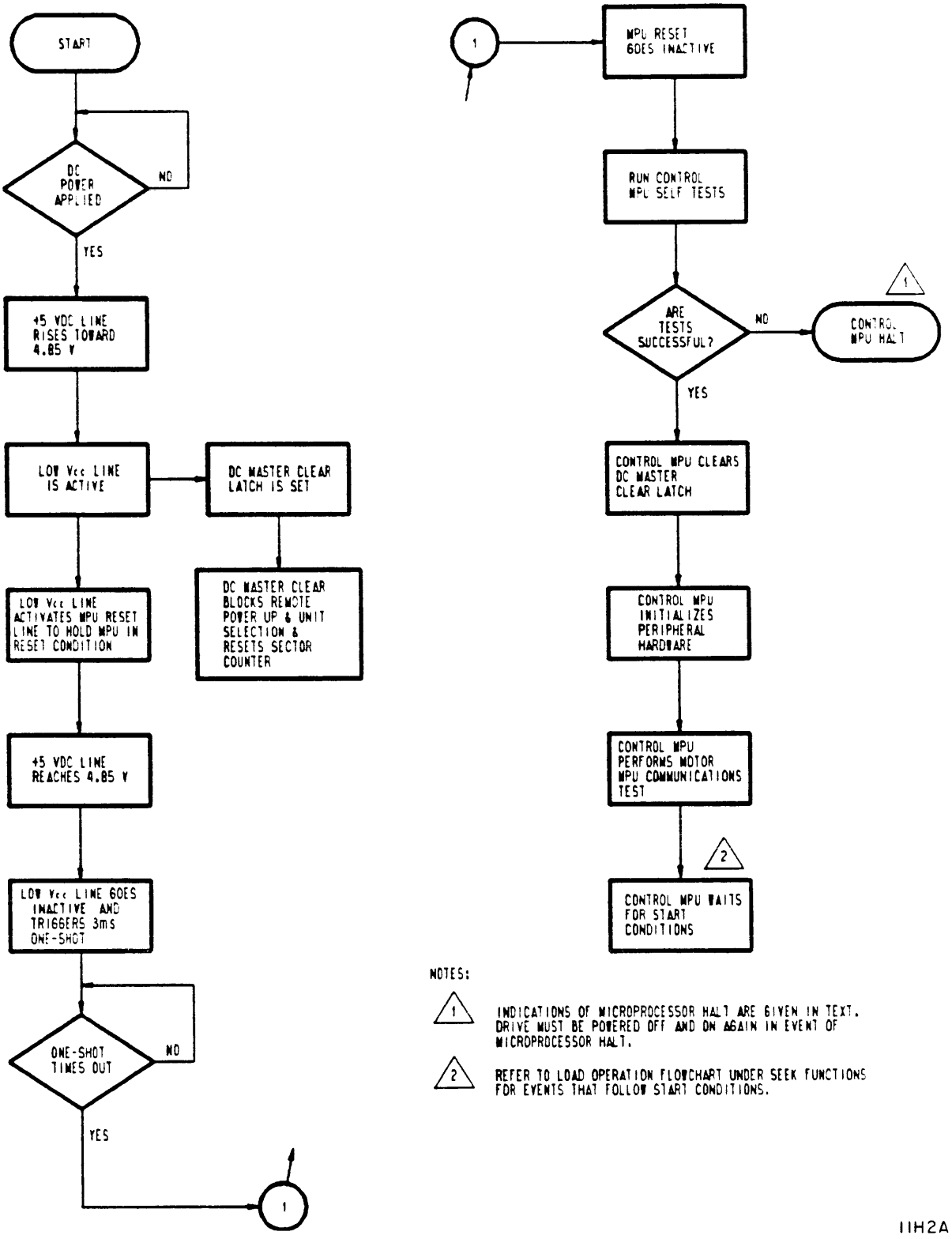


Figure 2-5. Power On Sequence Flowchart

Placing the power supply On/Standby (1/0) switch to the On (1) position enables dc power to the drive. A level detector on the control board monitors the +5 V input from the power supply and activates the Low Vcc line as this input rises toward +4.85 V. During this time, the DC Master Clear latch in the Sector Counter Gate Array is set, and its output, the DC Master Clear signal, remains active. A DC master clear resets the sector counter and the head address register. In addition, a DC master clear disables the interface by blocking unit selection. In dual-channel drives, a DC master clear blocks unit selection by either controller.

The Reset Control MPU line to the Control MPU goes active when the Low Vcc signal goes active, or a hang condition in the Control MPU fails to keep the hang detect one-shot delay retriggered. When the Reset Control MPU signal is inactivated, the Control MPU performs the initialization routine.

The initialization routine starts by running self-tests on the Control MPU and its peripheral hardware (including Servo MPU, operator panel, and I/O gate array). If a failure occurs during self-testing, the Control MPU stops and the failing component is indicated by a code displayed on the address indicators. Refer to the trouble analysis section of the maintenance manual for a description of these codes. With the self-tests complete, the Control MPU clears the DC Master Clear latch in the Sector Counter Gate Array, initializes the peripheral hardware, and initiates the Motor MPU communication test.

At this point, power on initialization is complete. This process will not be repeated until dc power is removed and reapplied to the drive (via the On/Standby (1/0) switch). The Control MPU waits for start conditions, as described later in this section under Power Sequencing.

SCSI I/O Board Initialization

Two power on test sequences occur as dc power is applied to the drive. The SCSI controller (I/O board) firmware is tested and initialized first. This is not an exhaustive diagnostic test but it verifies the integrity of the major components. The drive firmware is initialized if SCSI firmware testing and initialization are successful.

Controller testing consists of a hardware self-test that verifies the integrity of the controller hardware. The controller halts further initialization if this test fails.

The initialization sequence occurs under any of the following three conditions:

- Controller (I/O) power-up sequence occurs
- SCSI Bus Reset (-RST signal is asserted)
- BUS DEVICE RESET message is received on SCSI Bus

The controller does not respond to a Selection Phase on the SCSI bus during the self-test sequence. The self-test sequence consists of the following events:

- Test Microprocessor
- Test Buffer Controller
- Test RAM Memory
- Test SCSI Interface

The SCSI Firmware initialization sequence is as follows:

- Set status for the LUN (logical unit number) to Busy
- Initialize the SCSI

The Drive Firmware initialization sequence occurs next and is as follows:

- Initialize disk interface (I/O board-to-drive)
- Initialize LUN parameters
- Start the drive spindle (only during power on sequence)
- Read parameters from cylinder 0 sector 0 of the drive (only during power on sequence)
- Test controller/drive interface (only during power on sequence)
- Do write/read test on diagnostic cylinder (only during power on sequence)

When the SCSI controller firmware is initialized, the controller will respond to a Selection Phase. It returns BUSY status until the entire drive initialization process is complete.

The drive initialization firmware spins up the drive, and it attempts to read the saved controller parameters from a reserved area of the drive. These parameters define the disk characteristics and other operating parameters. As part of a power on sequence, the drive initialization concludes with the following tests:

- Test controller/drive interface
- Do write/read test on diagnostic cylinder (2 patterns)

Errors encountered during these tests will result in flashing I/O LEDs as explained in the maintenance manual. If an error occurs, the drive will no longer respond to SCSI commands. However, a SCSI reset will abort the error indication and any further diagnostic testing, and it will complete the initialization sequence. Powering down and then up while in the failure mode will restart the test.

The controller uses the default parameters if it cannot read the saved controller parameters from a reserved area of the disk or if that data is invalid (the disk has not been formatted). No controller/drive interface or write/read test will be done in this mode.

When the entire initialization process is complete, the first command sent by an Initiator is terminated with CHECK status and UNIT ATTENTION Sense Key.

IPI I/O Board Initialization

When dc power is applied, a circuit on the IPI I/O board monitors the Low Vcc signal and forms a reset pulse for the I/O MPU. After the reset pulse goes inactive, the I/O MPU does the following:

- It performs a self-test, checking its internal registers, internal RAM, and internal ROM. It initializes the internal registers.
- It tests and initializes all LSI chips on the I/O board.
- It tests and initializes the nonvolatile RAM (NOVRAM) containing the IPI configuration information.
- It initializes the head address register.
- It initializes the set of unique drive parameters that can be transmitted across the interface.
- It enables the two IPI ports.

The drive is then ready to begin power sequencing and to accept commands from the controller.

Power Sequencing

Each interface offers unique choices for power sequencing. Depending on switch selections, the load operation may begin immediately after power on initialization, or the load operation may be delayed. A separate topic describes power sequencing for each interface type.

Power Sequencing on SMD Interface Drives

The remote/local feature selects whether or not the controller can start the drive motor and perform a load operation. Part of drive installation is setting the REMOTE/LOCAL switch (on the drive I/O board) for either local or remote operation. Figure 2-6 shows the circuitry involved in power sequencing.

With the REMOTE/LOCAL switch in LOCAL, start conditions are as follows:

- On units with an operator panel, a load operation begins when you press the START switch.
- On units without an operator panel, a load operation begins when you activate the power supply.

With the REMOTE/LOCAL switch in REMOTE, start conditions are as follows:

- On units with an operator panel, a load operation begins when you press the START switch and the controller activates either Sequence Pick or Sequence Hold.
- On units without an operator panel, the load operation begins when the controller activates either Sequence Pick or Sequence Hold.

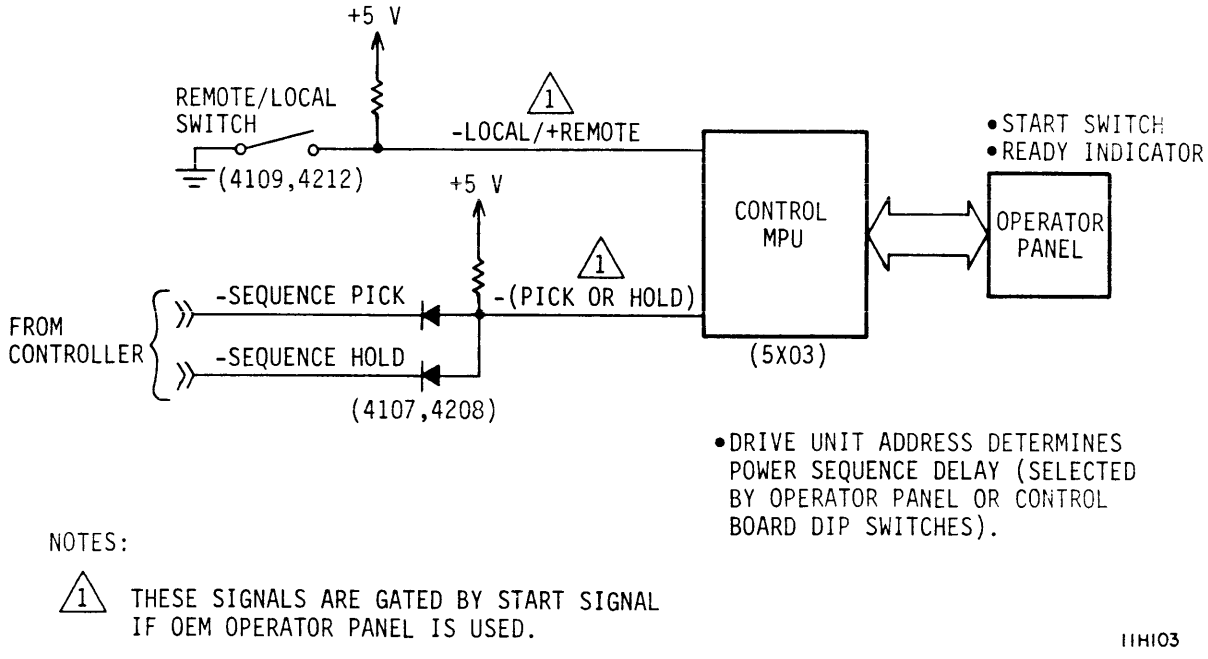


Figure 2-6. SMD Power Sequencing Circuitry

In a system of several drives set up for remote operation, all drives receive Sequence Pick or Sequence Hold at the same time. Once Sequence Pick or Sequence Hold is received, a delay routine in the Control MPU activates Motor Run after an interval equal to five seconds multiplied by the drive address. Thus, each drive in the system has a unique start-up interval. However, when start conditions are removed, all drives stop their drive motors and retract heads at the same time.

Power Sequencing on SCSI Interface Drives

Power sequencing is the process by which all disk drives in a string are started. Power sequencing can occur in either of two ways depending on how the Power On Sequence switch (DIP Switch 3) on the I/O board is set. The setting of this switch determines when the I/O circuitry drops the -Local/+Remote line to the Control MPU (see figure 2-7). While this line remains high, the Control MPU waits for start conditions. Once the line goes low (and the START switch is pressed on units with an operator panel), the Control MPU is ready to begin the load operation.

If the Power On Sequence switch on the I/O board is set to open (0), the power on sequence for each disk drive is delayed. The delay starts when dc power is applied. The length of the delay

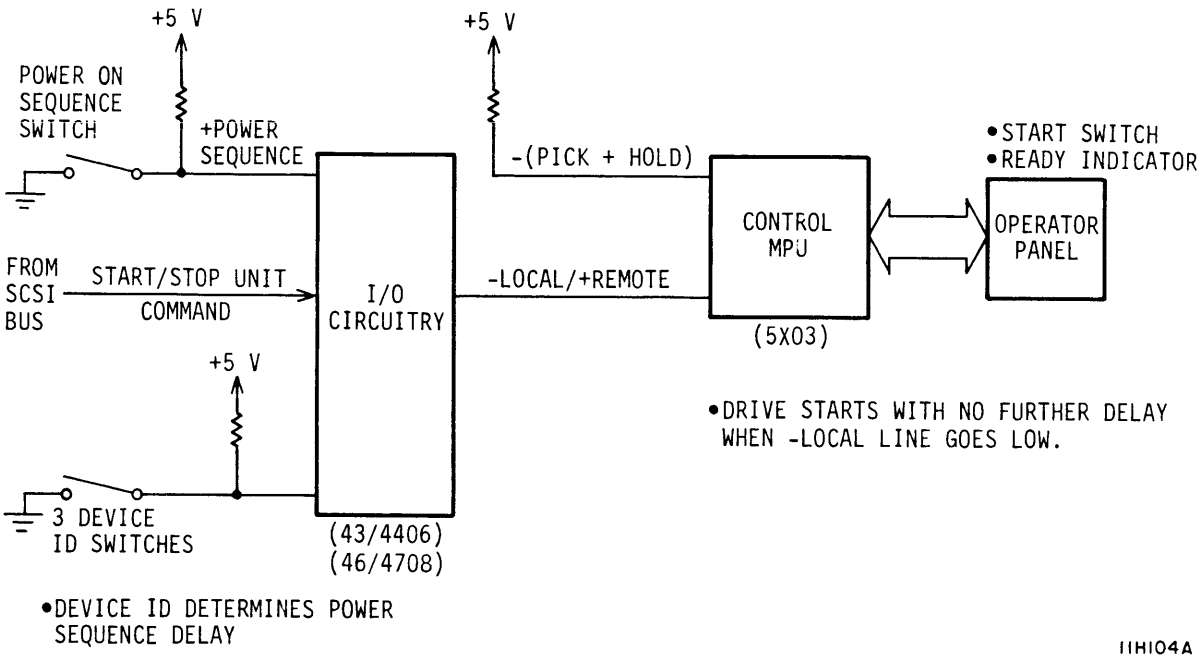


Figure 2-7. SCSI Power Sequencing Circuitry

is equal to the SCSI device address multiplied by a period of five seconds. The delay for device address 0 is zero seconds and the delay for device address 7 is 35 seconds. At the end of the delay, the -Local/+Remote line goes low.

If the Power On Sequence switch is set to closed (1), each disk drive in the string begins the power on sequence with no delay. The -Local/+Remote line stays low, enabling the Control MPU load operation.

The SCSI command set includes a START/STOP UNIT command, allowing the initiator to control when load and unload operations occur. A START UNIT command is not needed during the initial power on sequence. Following a power off sequence that results from a STOP UNIT command, a START UNIT command reestablishes start conditions. In this case, there is no power sequence delay.

Power Sequencing on IPI Interface Drives

The local/remote feature selects whether or not the controller can start the drive motor and perform a load operation. Part of drive installation is setting the LOCAL/REMOTE switch (on the drive I/O board) for either local or remote operation. Figure 2-8 shows the circuitry involved in power sequencing.

With the LOCAL/REMOTE switch in LOCAL, start conditions are as follows:

- On units with an operator panel, a load operation begins when you press the START switch.
- On units without an operator panel, a load operation begins when you activate the power supply.

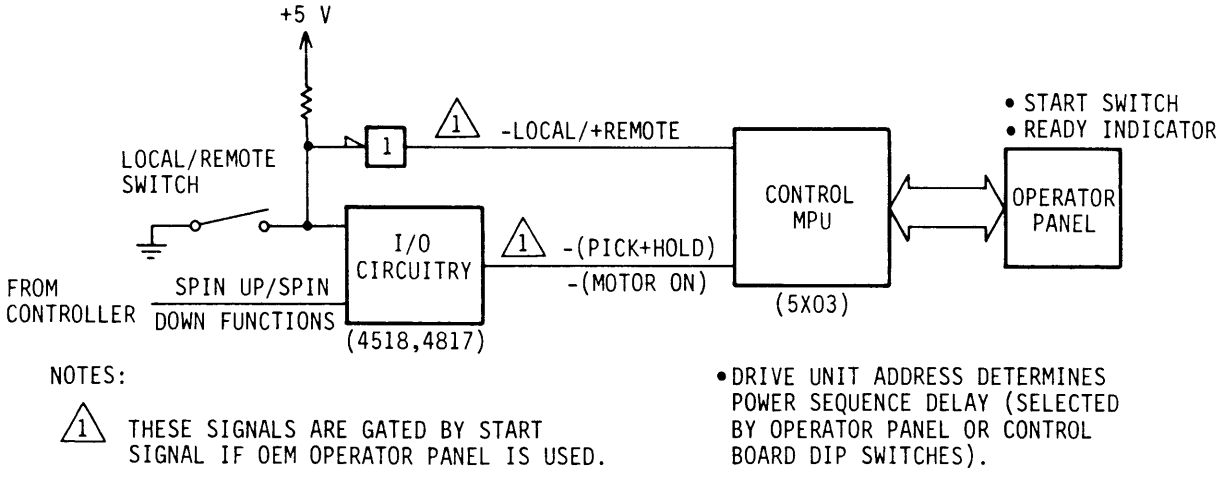


Figure 2-8. IPI Power Sequencing Circuitry

With the LOCAL/REMOTE switch in REMOTE, start conditions are as follows:

- On units with an operator panel, a load operation begins when you press the START switch and the controller selects the drive and issues a Spin Up function.

- On units without an operator panel, the load operation begins when the controller selects the drive and issues a Spin Up function.

In a system of several drives set up for remote operation, each drive must be selected and then issued a Spin Up function. Once the Spin Up function is received, a delay routine in the Control MPU activates Motor Run after an interval equal to five seconds multiplied by the drive address. Thus, each drive in the system has a unique start-up interval.

The controller can remove start conditions from each drive by selecting the drive and issuing a Spin Down function.

Load Operation

When start conditions are present, the Control MPU directs the load operation. The load operation energizes the drive motor to bring the disks up to speed and loads the heads to position them at cylinder zero on the disks. Details of the load operation are given under Types of Seeks in section 5. When the load operation is complete, the drive waits for commands from the controller.

POWER OFF SEQUENCE

The power off sequence unloads the heads and stops the drive motor. There are two conditions that initiate a power off sequence. One is a loss of start conditions, and the other is a loss of dc power to the drive.

Loss Of Start Conditions

A loss of start conditions occurs when the START switch is pressed, or a specific interface signal is received. The interface signals are as follows:

- SMD interface (remote only) -- the controller deactivates Sequence Pick and Sequence Hold.

- SCSI interface -- the initiator issues a STOP UNIT command.

- IPI interface (remote only) -- the controller selects the drive and issues a Spin Down function.

The Control MPU monitors the start conditions and directs an unload operation when they are removed. An unload operation (discussed under Types of Seeks in section 5) uses servo control to position the heads over the landing zone. The heads are held in this position by a retract command until the actuator is locked by the carriage latch. The Control MPU then drops the Motor Run command. Loss of Motor Run command causes the Motor MPU to reverse the motor drive signals causing a controlled deceleration. The drive remains in this condition until start conditions reappear.

Loss Of DC Power

A loss of dc power results when the power supply On/Standby (1/0) switch is switched to Standby (0) or when there is a loss of site ac power. When the dc voltages drop, an emergency retract takes place under hardware control. The emergency retract operation (described under Power Amplifier in section 5) requires no Control MPU intervention, and it uses voltage generated by the decelerating drive motor to drive the heads toward the landing zone. When the heads reach the landing zone, the carriage latch automatically holds them in this position. As the motor speed is dropping during a loss of dc power, the dynamic braking relay deenergizes and its contacts close. This shorts the motor stator windings together and makes the drive motor stop faster.

DISK ROTATION AND HEAD LOADING

The previous topic described the sequencing of starting and stopping the drive motor relative to loading and retracting the heads. Control of motor speed is coordinated with control of head position to ensure that the heads contact the disks only in the landing zone.

CONTROLLING THE DISK ROTATION

The control of disk rotation is discussed in two separate topics. The first topic covers the standard version of speed control, which is used in most drives described in this manual. The second topic discusses the synchronized version of speed control, a feature that allows a system of drives to have synchronized spindle rotation. Most of the information about the standard version applies also to the synchronized version.

Standard Motor Speed Control

Disk rotation is accomplished by an electromechanical system that accelerates the disks to 3600 r/min during power on and stops disk rotation with reverse current braking during power off. The spindle is directly coupled to the motor, which is mounted inside the spindle. The disks, in turn, are mounted on the spindle assembly. When the spindle is rotated by the drive motor, the disks rotate with the spindle.

The motor has a three-phase stator surrounded by a four-pole rotor. The Motor MPU provides pulsed excitation to the three stator windings. To keep the stator pulses in phase with rotor position, the Motor MPU uses feedback from three sensors located in the motor. These sensors detect flux reversals from the rotor magnets. As the rotor magnets pass each sensor, its output line toggles.

The Control MPU activates the Motor Run line to the Motor MPU to start the drive motor during the power on sequence (see Power On Sequence discussion). The Motor MPU firmware controls the direction of rotation and speed of the drive motor. The control and status lines between the Control MPU and the Motor MPU are shown in figure 2-9. The Motor MPU uses the +24 V output of the power supply to excite the stator windings in the drive motor. The drive motor current consumption is held to 7 amperes by a current limiting circuit.

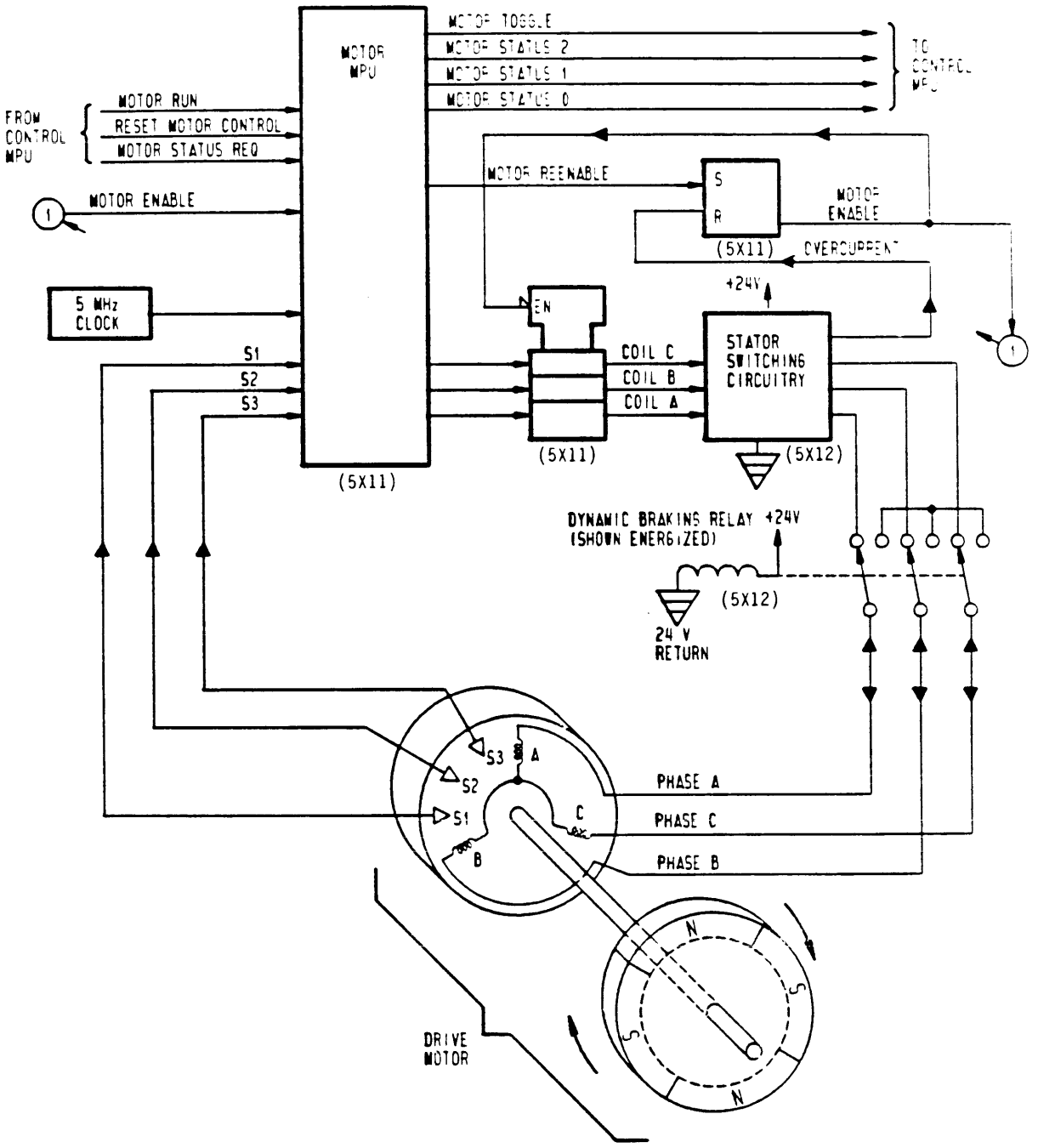


Figure 2-9. Standard Motor Speed Control Logic

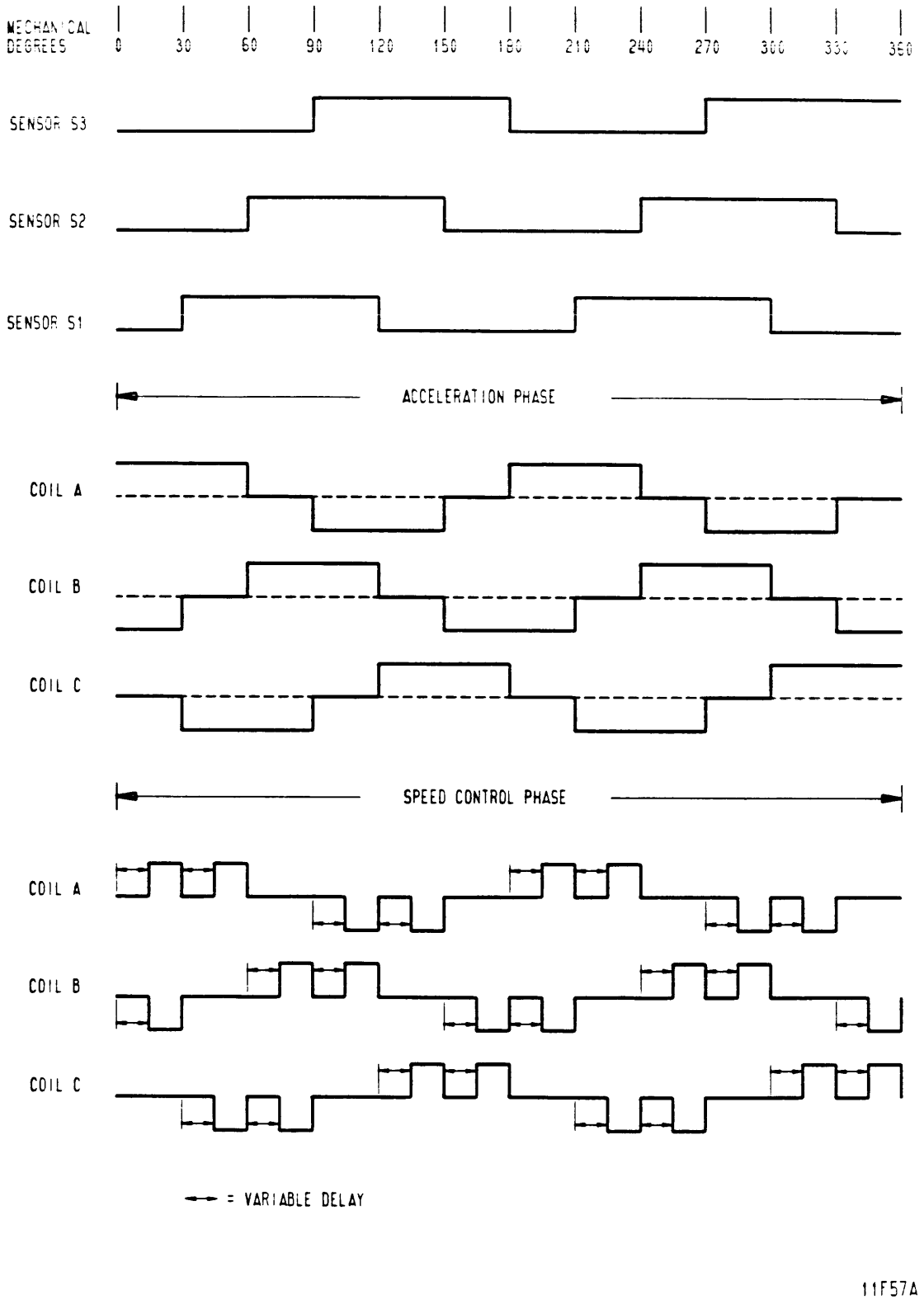


Figure 2-10. Speed Control Waveforms and Timing

The Motor MPU checks sensors S1, S2, and S3 to determine which pair of stator windings must be energized to maintain counterclockwise rotation (viewed from logic side of module). One of the three position sensors switches on or off every 30^{o} of shaft rotation. The waveforms of S1, S2, and S3 and corresponding excitation to the stator windings are shown in figure 2-10.

Motor speed is controlled by regulating the duration of power to the stator windings. During initial acceleration, power is applied for the entire amount of time that each stator winding is active until operating speed is reached. After reaching operating speed, the Motor MPU reduces the duty cycle of the pulses applied to the stator windings.

As shown in figure 2-10, there is a variable delay in which no power is applied to the stator windings. When the motor speed falls below 3600 r/min, the Motor MPU decreases the delay, increasing the width of power pulses (or duty cycle) applied to the motor. If the motor speed exceeds 3600 r/min, the Motor MPU increases the delay to reduce the applied power. Motor speed is maintained within the range of 3564 r/min (16.83 ms/rev) to 3636 r/min (16.34 ms/rev).

The Control MPU requests status (motor speed, fault conditions etc.) at 30-millisecond intervals from the Motor MPU by toggling the Motor Status Request line. The Motor MPU places the status information on the Motor Status 0-2 lines and toggles the Motor Toggle line to inform the Control MPU that status is available.

Motor speed is continuously monitored by the Motor MPU. When the spindle speed falls below 3564 r/min, the Motor MPU inactivates the Speed OK code to the Control MPU on the Motor Status 0-2 signal lines. Inactivating this code causes the Control MPU to provide write protection by activating the MP Write Protect line.

Write protection is needed to safeguard existing data on the disk by inhibiting the write circuitry while a motor speed error exists. The Control MPU deactivates the Write Enable line by activating the Write Protect latch (in the Peripheral Array) when a speed loss occurs and keeping it active for about 1/2 second after the condition is corrected.

If a loss of speed condition occurs, the Control MPU also drops the Ready signal and performs a retract operation. When the motor speed is restored and the heads are reloaded, the Control MPU returns the Ready signal to the controller. The Motor MPU automatically attempts to restore motor speed.

Reverse current motor braking decelerates the drive motor during a power off sequence. It occurs when motor speed drops below 1000 r/min. When this happens, the Motor MPU gates reverse current into the motor windings to slow down the spindle rotation. Refer to Power Off Sequence for a description of motor braking following a loss of dc power.

The Motor MPU places a code (Motor Stopped) on the Motor Status 0-2 lines to indicate to the Control MPU that braking is complete. When the Control MPU reads this status code, it turns off the Ready indicator to show that the power off sequence is complete.

Synchronized Motor Speed Control

The synchronized version of speed control allows a system of drives to have synchronized spindle rotation. The motor speed control operates in both asynchronous and synchronous modes, as dictated by the state of the Sync Circuit Enable signal, shown in figure 2-11. When the Sync Circuit Enable signal is inactive (asynchronous mode), the speed control operates exactly as described in the previous topic. Refer to that topic before going on with your study of synchronous operation.

The speed control always operates in the asynchronous mode whenever the spindle motor is being started or stopped. Asynchronous control continues during normal operation if no Motor Sync Reference pulses are being supplied to the drive.

A spindle sync cable carries the Motor Sync Reference signal to all drives in the system. Each drive has a timing circuit that can generate that signal, but only one of the drives is selected as a master to supply the signal to the other (slave) drives.

The Motor MPU monitors the Motor Sync Reference and Demodulator Active lines. The Motor MPU shifts from asynchronous to synchronous operation if the following conditions are met:

- Motor Sync Reference pulses are being supplied.
- The demodulator is active (indicating that the Index signal is reliable).
- The motor speed is within the allowable range.

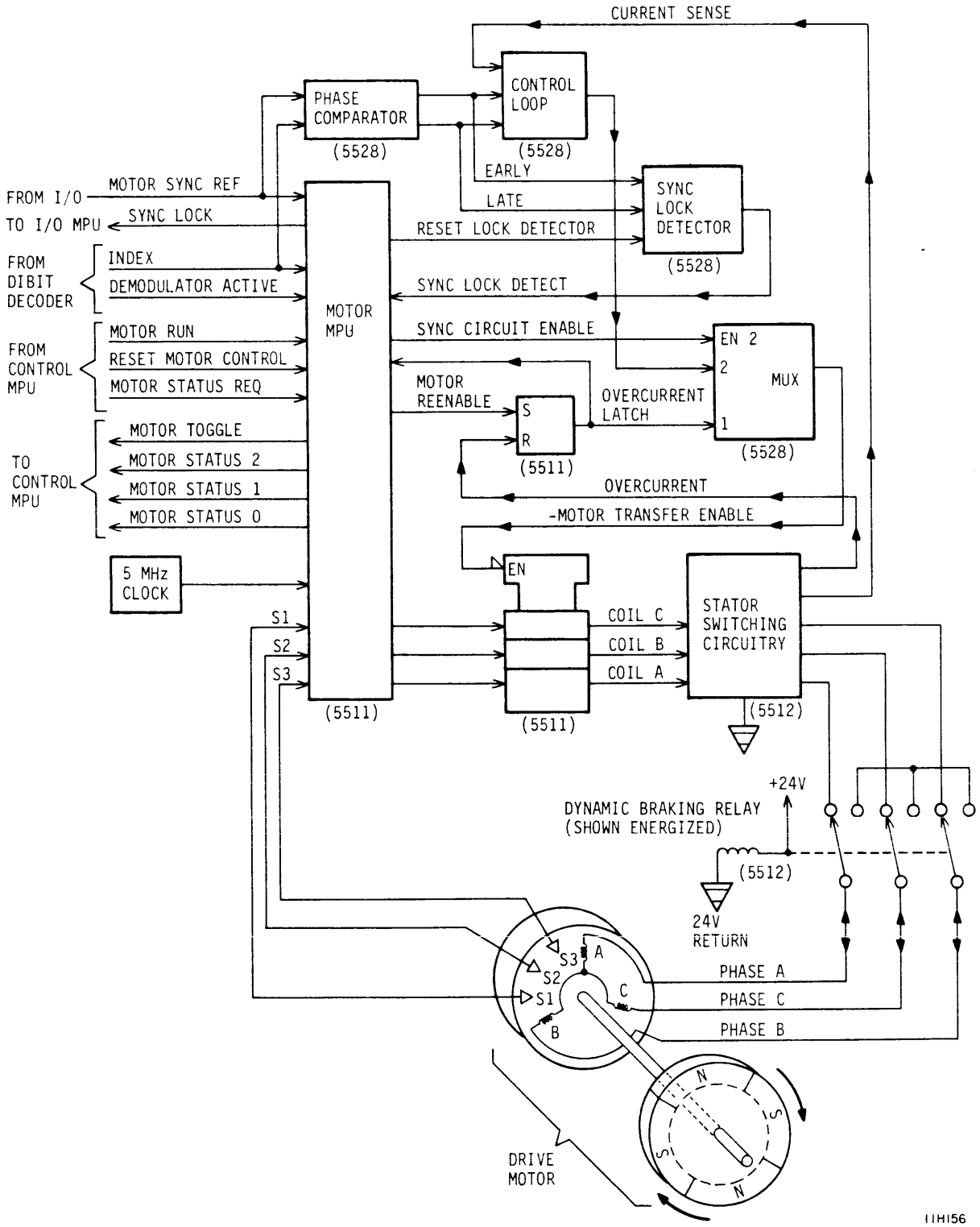


Figure 2-11. Synchronized Motor Speed Control Logic

In the synchronous mode, the Motor MPU continues to control the intervals in which each pair of motor windings is activated. However, the motor speed is regulated by a control loop. The control loop varies the average current to the motor windings as necessary to keep the Index signal synchronized to the Motor Sync Reference pulses. These reference pulses are supplied to all drives in the system. Once per disk rotation, the Index signal is decoded from the servo disk (as described in section 4).

In asynchronous mode, the Motor MPU varies the width of pulses applied to the motor to change its duty cycle. Shifting to synchronous control, the Motor MPU supplies full-width pulses on the Coil A, B, and C lines (refer to the Acceleration Phase waveforms in figure 2-10).

A phase comparator monitors its two timing inputs and develops either Early or Late pulses based on their phase difference. The greater the phase difference, the longer the Early or Late pulse stays active. The control loop filters the pulse inputs to develop a desired current value for the motor. The loop constantly monitors a Current Sense signal and adjusts drive to the motor to make the actual current match the desired current.

The loop controls the motor drive (or average current) by pulsing the Motor Transfer Enable signal many times per motor rotation. The duty cycle of the motor is simply the percentage of time that this signal is active.

If Motor Sync Reference pulses are present when a power on sequence begins, the transition to synchronous control occurs early in the calibration interval for the actuator servo. The transition is complete before the drive becomes ready. Once synchronous control is established, the Motor MPU resets and monitors the Sync Lock Detector. If the Motor MPU senses that sync lock is lost, it deactivates the Sync Lock signal, a latched input to the I/O MPU.

Spindle sync status is reported on the IPI interface if the drive has received a command enabling that type of status reporting. If so, when the drive is deselected, it posts an attention with a Class 3 interrupt to indicate that there is status pending. The loss of spindle synchronization will not interrupt any read or write operations. Refer to section 3C for status reporting information.

During synchronous operation, the Motor MPU continues to provide status periodically to the Control MPU. However, it uses the same status codes used for asynchronous operation. The Control MPU receives no status about spindle synchronization. It watches for loss of speed just as it does in asynchronous operation.

LOADING AND RETRACTING THE HEADS

People sometimes draw an analogy between airplanes and heads in a disk drive. Heads are described as flying when they lift away from the rotating disk surfaces. Heads are described as landing when they contact the disk surfaces. To extend the analogy, the landing zone on each disk surface is comparable to the runway at an airport. The landing zone is the region on the disk where head landing is safe.

Like airplanes, heads in a disk drive are moved away from the landing zone (are loaded) during their flight and returned to the landing zone (are retracted) before the flight ends.

Heads are magnetic devices that record data on, and read data from, the disk surface (the servo head, however, reads prerecorded data but cannot write). Two heads are attached to each supporting arm. The combined arm and heads are called a head-arm assembly. The eight head-arm assemblies are part of a rotating carriage.

Each head-arm assembly consists of a rigid arm, supporting two heads on load springs and gimbal springs (figure 2-12). The rotating carriage has a bearing cartridge at its pivot point. The head-arm assemblies, in turn, are mounted on the bearing cartridge. The carriage rotates when the magnetic field of its voice coil reacts to the field of permanent magnets. The rigid arm by itself does not provide the action necessary for the heads to load or unload. A head load spring forces the associated head toward the disk surface; a gimbal spring allows the head free axial movement along its vertical and horizontal axes independent of the rigid arm.

In the retract (nonoperating) condition, the head load springs force their respective heads against the disk surface in the landing zones. There is one landing zone on each data surface. At their extreme inward travel, the heads are located over their respective landing zones. During the power on sequence, the control firmware turns on the drive motor. When the drive motor is rotating the disks at acceptable speed, the heads move away from the disk surfaces and fly on the cushion of air created by disk rotation. At this point in the power on sequence, the rotary actuator is unlocked and the heads are moved outward to track zero. Until the power off sequence is begun, the heads continue to fly on the cushion of air.

The head load spring forces the head toward the disk surface, while the cushion of air pushes against the head to resist its closer approach. The air cushion pressure varies directly with disk speed, so that at proper speed the forces of the head load spring pressing the head towards the disk surface and the opposing force of the air cushion resisting the closer approach of the head are balanced such that the heads fly at the correct height above the disk.

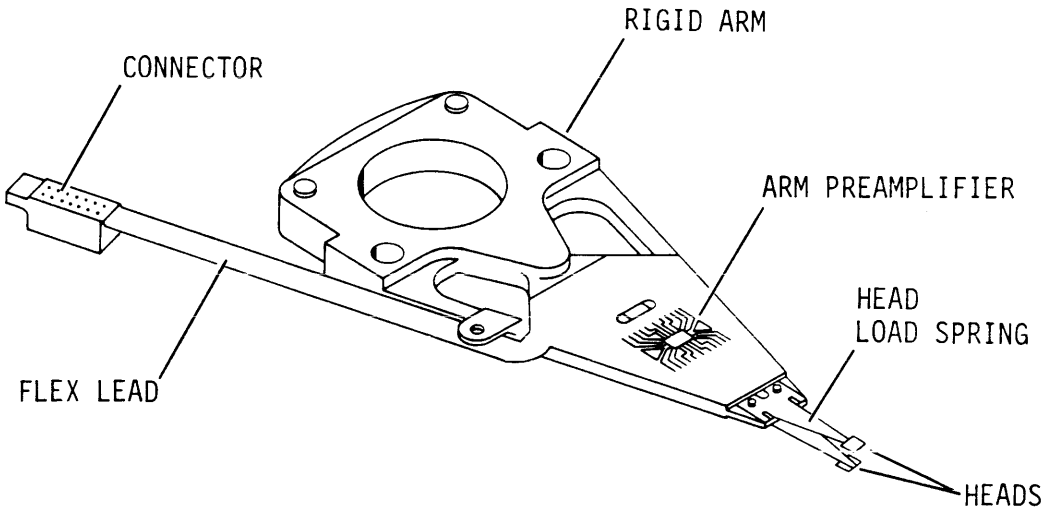


Figure 2-12. Head-Arm Assembly

If the disk speed drops, the air cushion pressure decreases and the head load springs force the heads closer to the disk surface. Sufficient loss of speed would cause the heads to stop flying and contact the disk. This is called head landing. Because insufficient disk speed causes head landing, heads are not moved into the data areas until the disks have come up to speed. For the same reason, the heads are retracted from the data areas and locked over the landing zone when the disk speed drops below a safe operating level.

VENTILATION SYSTEM

The ventilation system is divided into two parts, one for the drive unit and the other for the sealed module.

The drive ventilation system (figure 2-13) provides continuous air replacement and circulation to dissipate the heat generated by drive operation. The main component of the drive ventilation system is the fan mounted in the optional external power supply, or the auxiliary fan accessory attached to the rear of the unit. The auxiliary fan motor is driven by the +24 V power from the external power supply.

Both fan options push ambient air through the drive. When incorporating the optional power supply with integral cooling fan, the air circulation travels through the power supply and then enters the front of the drive. With the auxiliary fan, air travels from the rear of the drive to the front. Both fan options direct air over the drive electronics to cool these assemblies.

The ventilation system for the module is a self-contained closed loop system that consists of a fan, circulation filter, and breather filter. The fan blades are located at the top of the hub assembly, and the rotation of the spindle rotates these fan blades. The motion of the blades above the hub assembly pulls air through the circulation filter into the disk area.

If the pressure within the module becomes less than the surrounding atmosphere, makeup air enters through the breather filter to equalize the pressures. Likewise, if the module pressure exceeds atmospheric pressure, air leaves the module through the breather filter.

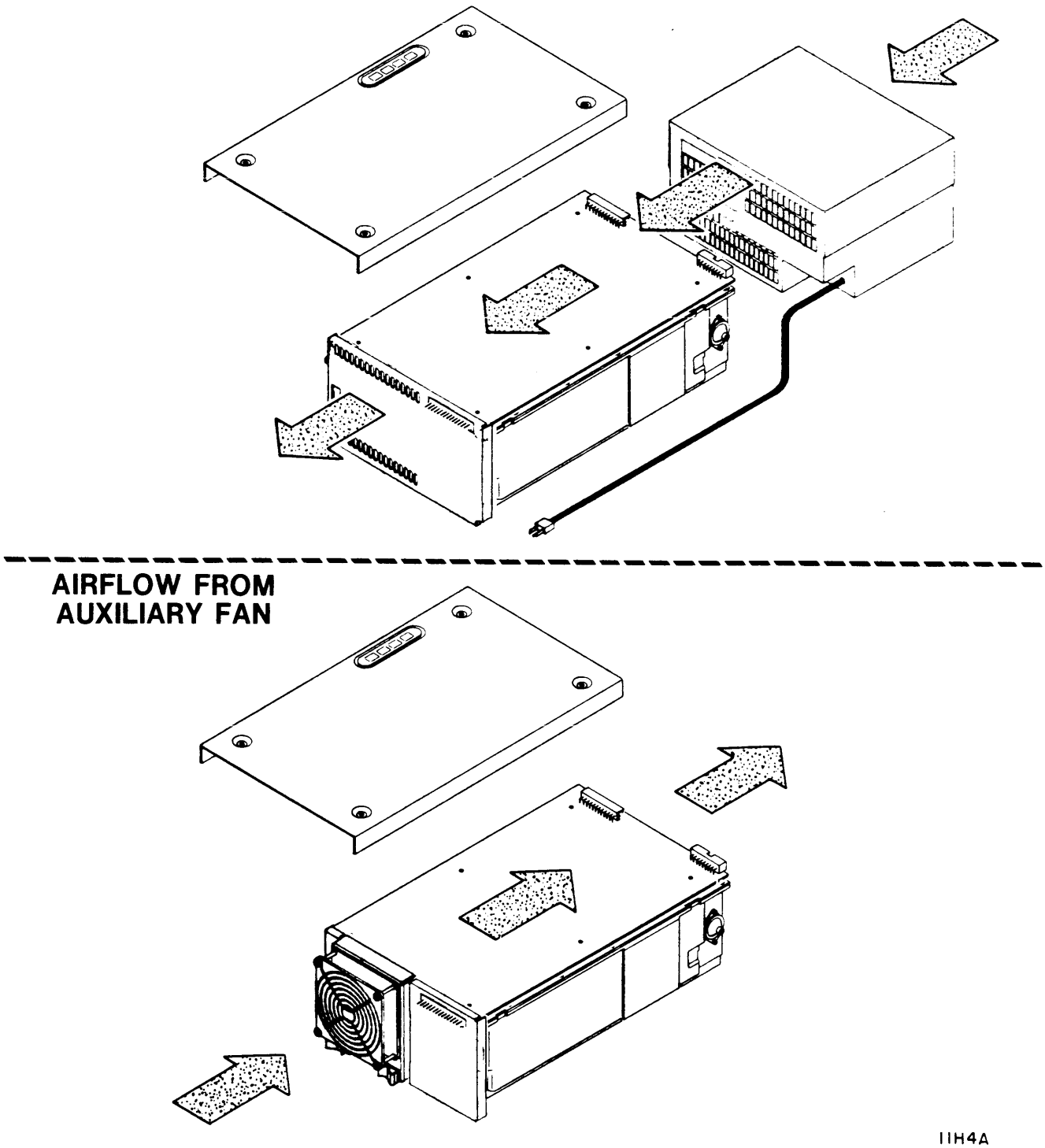


Figure 2-13. Drive Ventilation

SECTION 3

INTERFACE FUNCTIONS

INTERFACE FUNCTIONS 3

INTRODUCTION

The interface is the communications channel between the controller and the drive. Many of these communications are enabled only when the controller has the drive selected. This section is subdivided to cover the following types of interfaces:

- SMD Interface -- Section 3A
- SCSI Interface -- Section 3B
- IPI Interface -- Section 3C

These three interfaces are very different in the way the drive and controller communicate. However, the drives for these interfaces all use the same control board. Therefore, all three I/O boards communicate in the same manner with the control board. Figure 3-1 emphasizes these similarities.

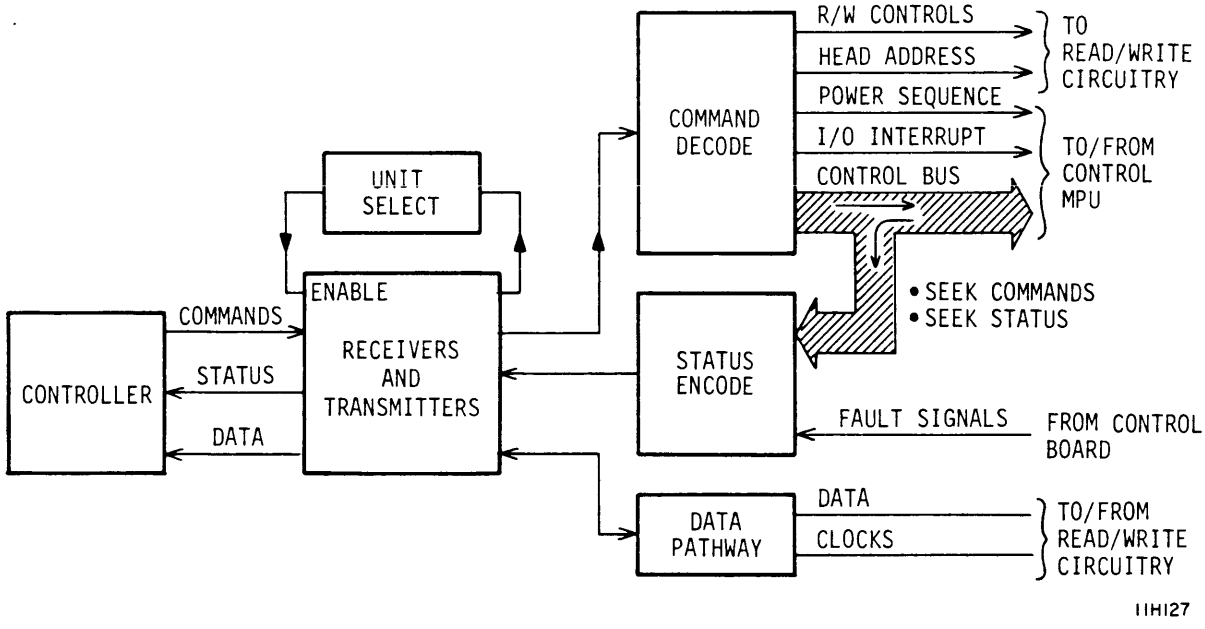


Figure 3-1. Interface Functions Block Diagram

SECTION 3A

SMD INTERFACE FUNCTIONS

SMD INTERFACE FUNCTIONS 3A

INTRODUCTION

This section, describing the SMD interface and its associated hardware, is divided into the following areas:

- Interface Operation -- Describes the signal lines on the interface and shows how the interface transfers commands, status, and data.
- Unit Selection -- Describes drive selection either by one controller or by one of two controllers.

INTERFACE OPERATION

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals, and read/write data transfers.

The interface consists of the I/O cables and the logic required to process the signals sent between drive and controller. A switch setting selects the version of SMD interface used:

- SMD-0 -- Standard SMD interface uses Tags 1 through 3.
- SMD-E -- Enhanced SMD interface uses Tags 1 through 6.

More information about the SMD-0/SMD-E selection and about the other options for extended cylinder addressing appears later in this section under I/O Signal Processing.

I/O CABLES

The drive has two I/O cables per channel, consisting of an A cable and a B cable. These cables contain all the lines going between the drive and controller.

The A cable carries commands and control information to the drive and status information to the controller. The B cable carries read/write data, clock, and status information between drive and controller. Figure 3A-1 shows all lines (except those not used) in the A and B cables. The function of each of these lines is explained in tables 3A-1 and 3A-2.

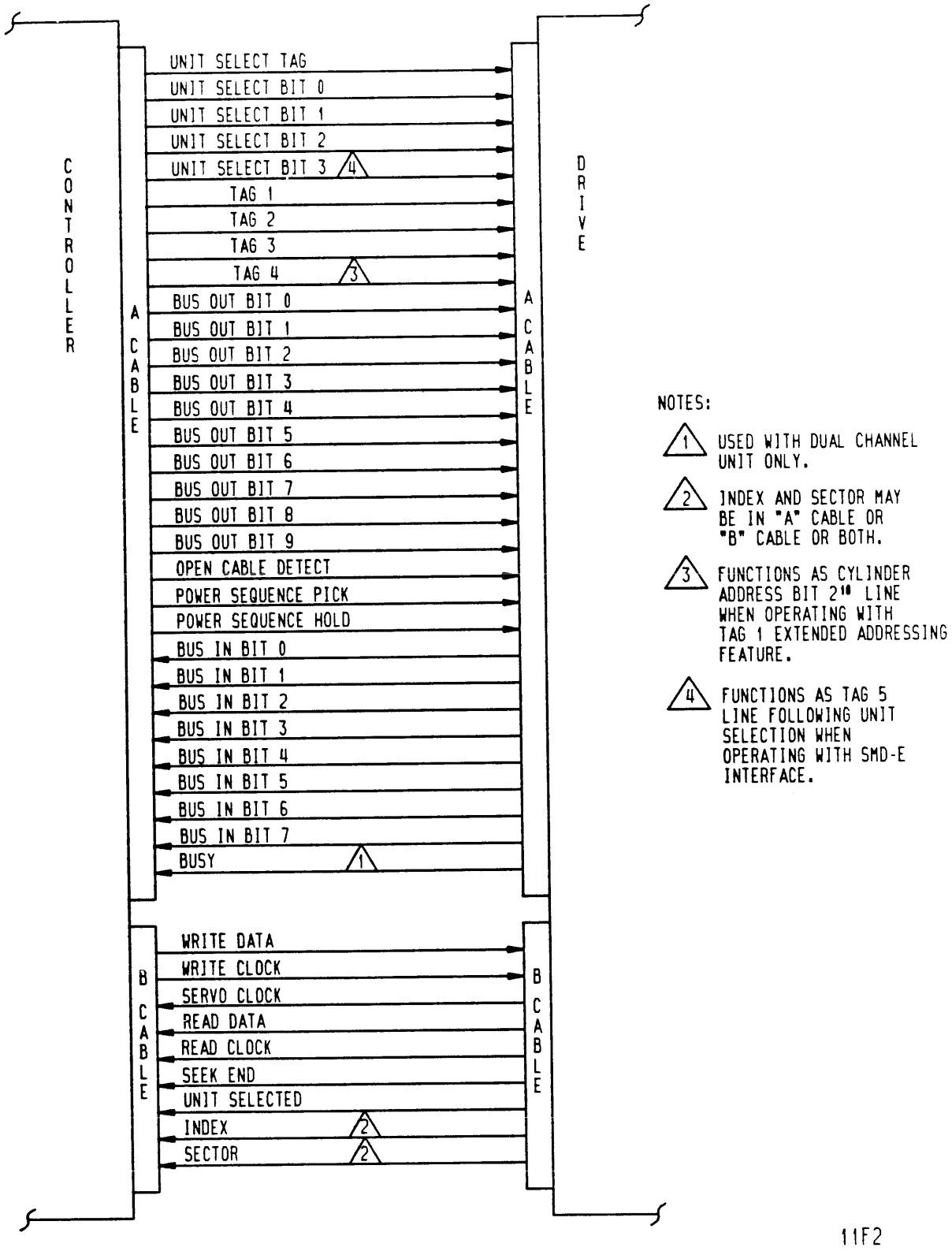


Figure 3A-1. Interface Lines

TABLE 3A-1. CONTROLLER TO DRIVE INTERFACE LINES

Line	Function
Bus Out Bits 0-9	These ten lines carry data to the drive. The meaning of the data is a function of the active tag line.
Open Cable Detect	A voltage is supplied by the controller to override the bias voltage at the drive receivers. If the A cable is disconnected or if controller power is lost, unit selection and controller commands are inhibited.
Sequence Pick or Sequence Hold	A ground from the controller on either of these lines starts the power on cycle on all drives in the string providing the following conditions exist: • the REMOTE/LOCAL switch is set to REMOTE, and • the START switch has been pressed to start motor (if an operator panel is installed). These lines have no effect in the Local mode.
Tags 1-3, Tag 4/Cyl. Addr. Bit 2^{10}	These lines carry information that is decoded by the drive tag/bus decode logic and used in conjunction with Bus Out lines 0 through 9 to produce desired functions (refer to table 3A-3). When operating with the Tag 1 Extended Addressing Feature, the Tag 4 line functions as the Cylinder Address Bit 2^{10} line.
Unit Select Bits 0, 1, 2, and 3/ Tag 5	A binary code is placed on these four lines to select a drive. The binary code must match the logical address assigned to the drive. Drives can be numbered 0 through 15. Bit 3 serves a dual purpose as follows:
Table Continued on Next Page	

TABLE 3A-1. CONTROLLER TO DRIVE INTERFACE LINES (Contd)

Line	Function
	1. When gated with Unit Select Tag, this line must match the high order bit of the unit number for a unit selection to occur. 2. Following unit selection on drives configured with the SMD-E interface, this bit functions as the Tag 5 line.
Unit Select Tag	This signal gates Unit Select lines into a compare circuit. The unit is selected 600 ns (maximum) after Unit Select Tag becomes active. The drive will not process commands until selected. Drive status is returned on Bus In lines while unit is selected (refer to Tag 1 Bus In description). Deselection occurs 600 nanoseconds (maximum) after Unit Select Tag drops. In dual-channel units, the Unit Select Tag also causes the drive to be reserved to the issuing channel provided selection occurs. The reserve condition can be cancelled by a Release command, a reserve timeout, or by a Priority Select (i.e Unit Select Tag accompanied by proper logical address and Bus Out Bit 9 active). The drive is unconditionally selected and reserved by the channel issuing a Priority Select command provided that the issuing channel has not been disabled.
Write Clock	This clock is the Servo Clock retransmitted to the drive during a write operation. Write Clock must be synchronized to the NRZ data and must be transmitted 250 ns prior to Write Gate.
Write Data	This line transmits NRZ data from the controller to the drive for recording on the disk surface.

TABLE 3A-2. DRIVE TO CONTROLLER INTERFACE LINES

Line	Function
Bus In Bits 0-7	These eight lines carry status, drive identity, and current sector location information to the controller.
Busy	Used only in dual-channel drives, this signal is generated when a controller attempts to select a drive that has already been selected or reserved by the other controller. This signal is sent to the controller attempting the selection.
Index Mark	This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero. Note: This signal may be disabled by a switch selection on the I/O board.
Read Clock	This clock is derived from, and is synchronous with, the detected data. Read Clock defines the beginning of a data cell.
Read Data	This line transmits data recovered from the disk. The data is transmitted in NRZ form to the controller.
Sector Mark	This signal is derived from the servo tracks. The number of sector signals that occur for each revolution of the disk is selected by switches on the control board. Note: This signal may be disabled by a switch selection on the I/O board.

Table Continued on Next Page

TABLE 3A-2. DRIVE TO CONTROLLER INTERFACE LINES (Contd)

Line	Function
Seek End	This signal indicates either on cylinder status or seek error status resulting from a seek operation that has terminated. When SMD-E interface drives respond to a Tag 5 execute diagnostic test command, Seek End indicates that test execution is complete. In dual-channel configurations, the Seek End signal to the unreserved channel is active continuously except when the unreserved channel attempts to select the drive (Tried latch set). Setting the Tried latch causes Seek End to the unreserved channel to drop for 30 microseconds when the reserved channel drops its Select and Reserve latches.
Servo Clock	Servo Clock is a phase-locked signal generated from the servo track dibits. It is continuously transmitted. The Servo Clock frequency is as follows: • 14.52 MHz on 736 MB drives • 19.72 MHz on 850 MB drives • 21.99 MHz on 1120 MB drives • 24.20 MHz on 1230 MB drives
Unit Selected	This signal indicates the drive has accepted a Unit Select request. The line must be active before the drive will respond to any command from the controller.

I/O SIGNAL PROCESSING

I/O signals from the controller initiate and control all drive operations except Local mode power-on when the unit is configured with an operator panel (refer to the discussion on Power Functions in section 2). The I/O signals are received in the drive I/O board where they are routed to the appropriate logic in the drive. In turn, the drive sends information back to the controller via drivers on the I/O board.

The drive can be configured to operate with either a standard SMD (SMD-0) interface or an enhanced SMD (SMD-E) interface. A switch setting selects the version of SMD interface used:

- SMD-0 -- Standard SMD interface uses Tags 1 through 3.
- SMD-E -- Enhanced SMD interface uses Tags 1 through 6.

In addition, two types of extended addressing are available with either interface type: Tag 1 Extended Addressing, and Tag 2 Extended Addressing. Because of signal line contention, SMD-E units configured with Tag 1 Extended Addressing cannot use Tags 4 and 6.

Units not configured with either extended addressing feature can address up to 1024 cylinders. Both extended addressing features allow the 736 MB, 1120 MB, and 1230 MB drives to address up to 1635 cylinders. They allow 850 MB drives to address up to 1381 cylinders.

Figure 3A-2 is a drive block diagram showing the I/O signal lines and their routing to and from the drive logic. When the drive is selected, the tag receivers are enabled. With the Unit Select Tag active, commands are generated based upon the tag code as defined by the Bus Out lines.

Table 3A-3 provides a summary of the tag and bus decoding. Table 3A-4 expands on this summary by defining Bus Out and Bus In for each tag. The other theory discussions in this manual further define the effects of the I/O commands and the encoding of fault status and diagnostic information.

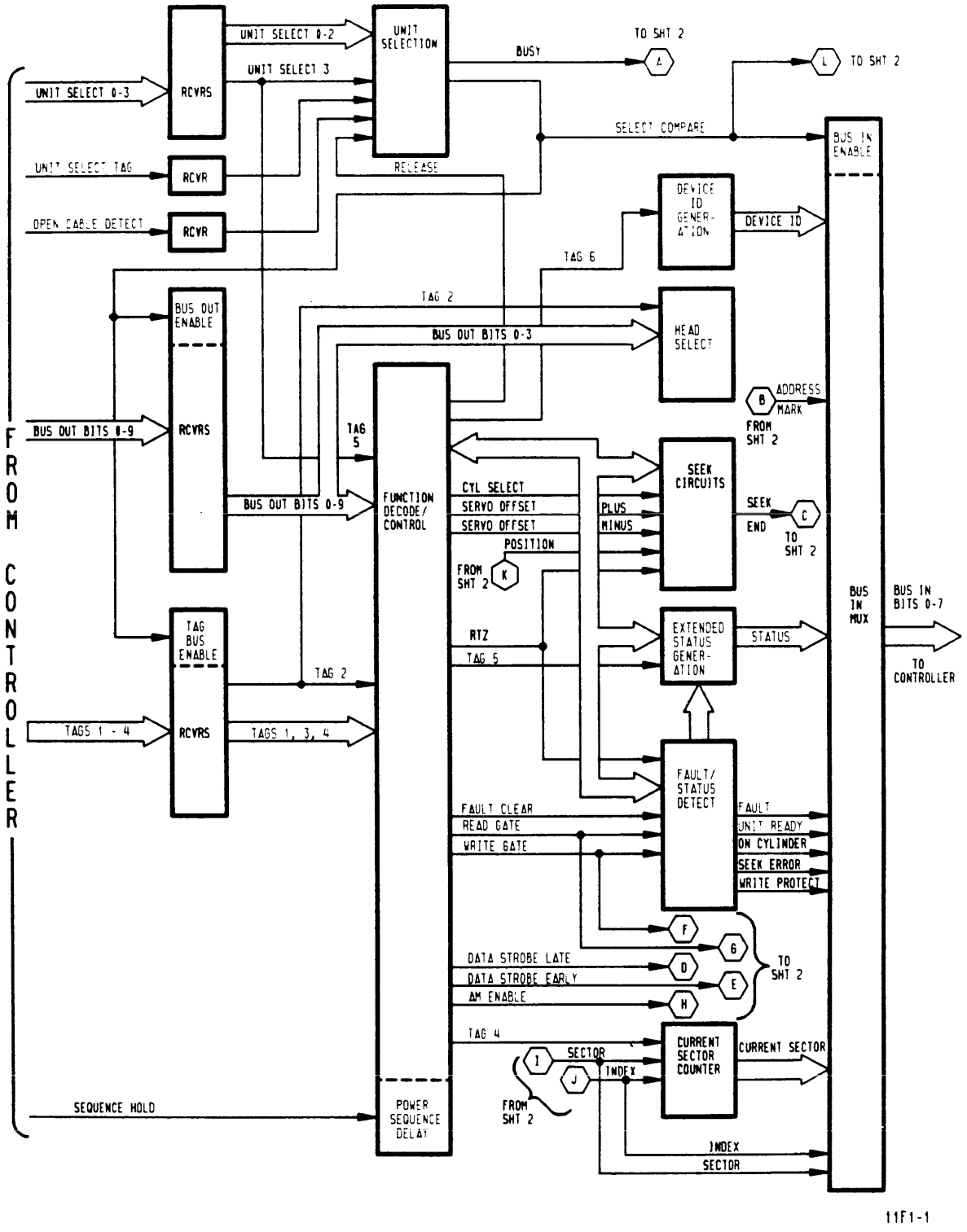


Figure 3A-2. Drive I/O Signal Processing (Sheet 1 of 2)

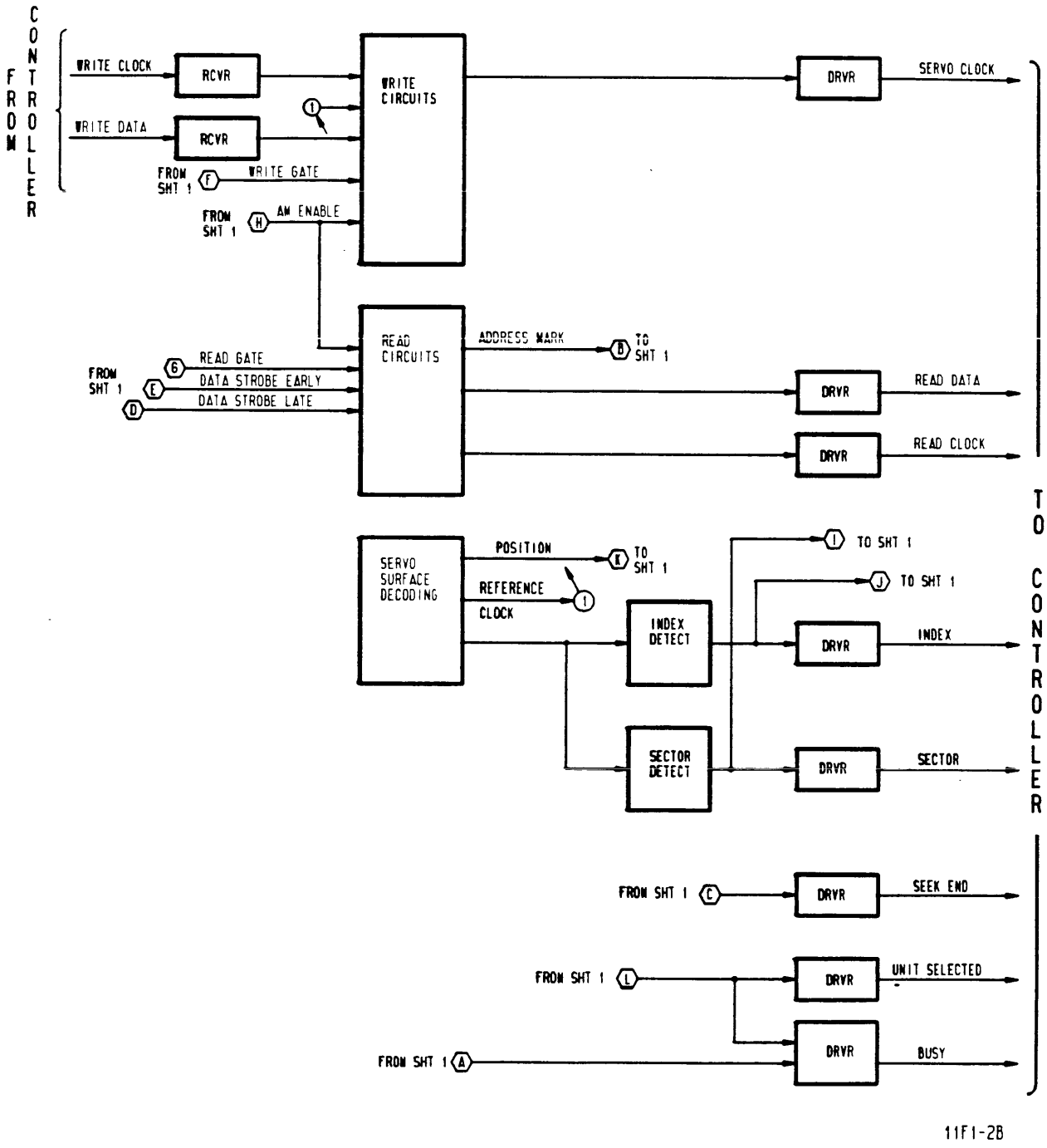


Figure 3A-2. Drive I/O Signal Processing (Sheet 2)

TABLE 3A-3. SUMMARY OF TAG/BUS DECODING

Bus Out Bits	Unit Select Tag	Tag 1	Tag 2	Tag 3
		Low Cylinder Select	Head and High Cylinder Select	Control Select
0		2^0	2^0	Write Gate
1		2^1	2^1	Read Gate
2		2^2	2^2	Servo Offset Plus
3		2^3	2^3	Servo Offset Minus
4		2^4	2^4	Fault Clear
5		2^5		Address Mark Enable
6		2^6		Return to Zero
7		2^7	2^{10} *	Data Strobe Early
8		2^8	2^{11} *	Data Strobe Late
9	Priority Select	2^9		Release
10		2^{10} *		

Bus In Bits	Unit Select Tag	Tag 1	Tag 2	Tag 3
	Drive Status			
0	← - - - - - - - - - - - - - - - Unit Ready - - - - - - - - - - - - - - - →			
1	← - - - - - - - - - - - - - - - On Cylinder - - - - - - - - - - - - - - - →			
2	← - - - - - - - - - - - - - - - Seek Error - - - - - - - - - - - - - - - →			
3	← - - - - - - - - - - - - - - - Fault - - - - - - - - - - - - - - - →			
4	← - - - - - - - - - - - - - - - Write Protect - - - - - - - - - - - - - - - →			
5	← - - - - - - - - - - - - - - - Address Mark - - - - - - - - - - - - - - - →			
6	← - - - - - - - - - - - - - - - Index Mark - - - - - - - - - - - - - - - →			
7	← - - - - - - - - - - - - - - - Sector Mark - - - - - - - - - - - - - - - →			

Bus Out Bits	Tag 4*	Tag 5				Tag 6*
	Current Sector	Fault Status Request	Operating Status Request	FRU Status Request	Execute Diagnostic Test Command	Device Type
0	0	0	1	0	1	0
1	0	0	0	1	1	0
2-9	0	0	0	0	0	0
10	X	0	0	0	0	X

Bus In Bits	Tag 4*	Tag 5				Tag 6*
	Current Sector Count	Extended Fault Status	Operating Status	FRU Codes	Diagnostic Execute Status	Device Type Status
0	2^0	Read • Write	↑	↑	0	↑
1	2^1	Read + Write • Not On Cylinder	See	See	0	Customer
2	2^2	First Seek			0	Defined
3	2^3	Write	Maintenance	Table	0	By
4	2^4	Write • Write Protected			0	Switch
5	2^5	Head Select	Manual	3A-4	0	
6	2^6	Voltage	↓	↓	0	Settings
7	2^7	Valid Status Available	Valid Status Available	Valid Status Available	Test is Executing	↓

* Choice of Tag 1 or Tag 2 Extended Addressing affects position of Cylinder Address Bit 2^{10} in this table. Tags 4 and 6 are not available if Tag 1 Extended Addressing is chosen.

TABLE 3A-4. TAG/BUS COMMAND DECODE FUNCTIONS

I/O Signals	Function
TAG 1 -- CYLINDER SELECT/LOW CYLINDER SELECT This tag initiates a seek operation. On units not configured with the Tag 1 extended addressing feature, this tag line gates ten address lines to the drive Cylinder Address register. In addition, on units with the Tag 1 extended addressing feature, this tag gates Bit 2^{10} of the cylinder address to the drive Cylinder Address register on A cable lines 30 and 60 (Tag 4). Extended addressing allows drives to address all legal cylinders (including those greater than 1023). Commanding a drive to seek beyond its maximum legal cylinder address will cause a seek error. Drive status information is returned on the Bus In lines. On units configured with the Tag 2 extended addressing feature, Tag 2 must precede Tag 1 to ensure that the higher order cylinder address bits are gated into the Cylinder Address register before the seek is initiated.	
Bus Out Bits	Defined as follows:
BOB0	Cylinder Address 2^0
BOB1	Cylinder Address 2^1
BOB2	Cylinder Address 2^2
BOB3	Cylinder Address 2^3
BOB4	Cylinder Address 2^4
BOB5	Cylinder Address 2^5
BOB6	Cylinder Address 2^6
BOB7	Cylinder Address 2^7
BOB8	Cylinder Address 2^8
BOB9	Cylinder Address 2^9
Bus In Bits	Defined as follows:
BIB0	Unit Ready -- Unit Ready indicates that the drive is up to speed, that the first seek was successful, and that no fault condition exists.

Table Continued on Next Page

TABLE 3A-4. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
BIB1	On Cylinder -- This signal indicates that the servo head is positioned at a track. This line goes inactive if the positioner drifts off cylinder.
BIB2	Seek Error -- this signal indicates one of the following conditions: • The drive took too long to complete a seek. • The positioner has moved outside the recording field. • The drive was commanded to seek beyond its maximum legal cylinder (1634 for 736 MB, 1120 MB, and 1230 MB drives; 1380 for 850 MB drives). The seek error can be cleared by an RTZ command.
BIB3	Fault -- When this line is active, it indicates that one or more of the following faults exist: • Read and Write Fault • Write or Read Attempted While Off Cylinder • First Seek Fault • Write Fault • Write and Write Protected Fault • Head Select Fault • Voltage Fault

Table Continued on Next Page

TABLE 3A-4. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
BIB4	Write Protect -- This signal indicates that the drive write circuits are disabled. Attempting to write while the write protect mode is active results in a fault condition. The write protect mode is enabled by any of the following: • a switch on the control board • a switch on the operator panel • a fault condition • a loss of motor speed.
BIB5	Address Mark -- When an address mark has been found during an address mark search operation, this line goes high (refer to Tag 3 description).
BIB6	Index Mark -- This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero. Note: This signal may be disabled by a switch selection on the I/O board.
BIB7	Sector Mark -- This signal is derived from the servo tracks. The number of sector signals that occur for each revolution of the disk is selected by switches on the control board. Note: This signal may be disabled by a switch selection on the I/O board.
Table Continued on Next Page	

TABLE 3A-4. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
TAG 2 -- HEAD SELECT/HIGH CYLINDER SELECT This tag line gates the data on the bus out lines to the drive Head Address register and also provides the high order Cylinder Address Bits 2^{10} and 2^{11} on units configured with the Tag 2 extended addressing feature. Extended addressing allows drives to address all legal cylinders (including those greater than 1023). Commanding a drive to seek beyond its maximum legal cylinder address will cause a seek error. Drive status information is returned on the Bus In lines (refer to Tag 1 Bus In description). On units configured with the Tag 2 extended addressing feature, Tag 2 must precede Tag 1 to ensure that the higher order cylinder address bits are gated into the Cylinder Address register before the seek is initiated.	
Bus Out Bits	Defined as follows:
BOB0	Head Address 2^0
BOB1	Head Address 2^1
BOB2	Head Address 2^2
BOB3	Head Address 2^3
BOB4	Head Address 2^4
BOB5-6	Not used
BOB7	Cylinder Address 2^{10}
BOB8	Cylinder Address 2^{11}
BOB9	Not used
Bus In Bits	Refer to description of Bus In Bits under Tag 1.
TAG 3 -- CONTROL SELECT This tag line gates the data on the bus lines to the logic circuits of the drive for commanding various operations. The operation performed is dependent upon which of the Bus Out lines is active. Drive status information is returned on the Bus In lines (refer to Tag 1 Bus In description).	
Table Continued on Next Page	

TABLE 3A-4. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
Bus Out Bit	Defined as follows:
BOB0	Write Gate -- Enables write driver. Not accepted if there is a seek error or fault status.
BOB1	Read Gate -- Enables read circuitry. Leading edge triggers the read chain circuit to synchronize on an all zeros pattern. Not accepted if there is a seek error or fault status.
BOB2	Servo Offset Plus -- Offsets the positioner from the on cylinder position by shifting it slightly toward the spindle. Disables On Cylinder for 2.75 milliseconds.
BOB3	Servo Offset Minus -- Offsets the positioner from the on cylinder position by shifting it slightly away from the spindle. Disables On Cylinder for 2.75 milliseconds.
BOB4	Fault Clear -- A pulse sent to the drive that clears the Fault latch provided that the fault condition no longer exists.
BOB5	Address Mark Enable -- When this signal occurs with a Write Gate, an address mark is written. When this signal occurs with a Read Gate, an address mark search is initiated.
BOB6	RTZ -- A pulse sent to the drive to move the positioner to track zero. It also resets the Head Address register, Cylinder Address register, and Seek Error latch.

Table Continued on Next Page

TABLE 3A-4. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
BOB7	Data Strobe Early -- Enables the read comparator to strobe the data at a time earlier than nominal.
BOB8	Data Strobe Late -- Enables the read comparator to strobe the data at a time later than nominal.
BOB9	Release -- Used with dual-channel option only, it clears channel reserved and channel priority select status. (Refer to Unit Selection discussion.)
Bus In Bits	Refer to description of Bus In Bits under Tag 1.
TAG 4 -- CURRENT SECTOR (SMD-E ONLY) This tag allows the current sector address to be transmitted to the controller on the Bus In lines. A sector address can be any number from 0 to 255. Bus Out Bits 0 through 9 are undefined. Note: This tag is not usable when the unit is configured with Tag 1 Extended Addressing.	
Bus In Bits	Defined as follows:
BIB0	Sector Address 2^0
BIB1	Sector Address 2^1
BIB2	Sector Address 2^2
BIB3	Sector Address 2^3
BIB4	Sector Address 2^4
BIB5	Sector Address 2^5
BIB6	Sector Address 2^6
BIB7	Sector Address 2^7

Table Continued on Next Page

TABLE 3A-4. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
TAG 5 -- EXTENDED STATUS (SMD-E ONLY) This tag allows extended fault status, operating status, and diagnostic FRU status to be transmitted to the controller on Bus In lines or allows the execute diagnostic test command to be issued. Except for the execute diagnostic test commands, this tag can be executed at any time. Execute diagnostic test command can be requested whenever the drive has completed the load sequence. The type of status transmitted on Bus In is determined by the state of Bus Out Bits 0 and 1. Note: Bus Out Bits 2 through 9 should be set to zero.	
Bus Out Bits 0-1 00	Extended Fault Status -- When Bus Out Bits 0 and 1 are set to zero, current fault status is transmitted on Bus In as follows:
Bus In Bits	
BIB0	Read and Write Fault
BIB1	Read or Write and Off Cylinder Fault
BIB2	First Seek Fault
BIB3	Write Fault
BIB4	Write and Write Protected Fault
BIB5	Head Select Fault
BIB6	Voltage Fault
BIB7	Valid Status Available
	For a description of these individual fault conditions, see How Errors are Detected in section 7 of the manual.

Table Continued on Next Page

TABLE 3A-4. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
Bus Out Bits 0-1 10	Operating Status -- When Bus Out Bit 0 is a "1" and Bus Out Bit 1 is a "0", then Bus In Bits 0 through 6 reflect drive operating status codes. Bus In Bit 7 indicates that valid status is available. Refer to the maintenance manual for drive operating status codes and their definitions.
01	Diagnostic FRU Status -- When Bus Out Bit 1 is a "1" and Bus Out Bit 0 is a "0", then Bus In Bits 0 through 3 reflect the most likely failed field replaceable unit (FRU) as defined in the following list.
Bus In Bits 3-0	Field Replaceable Units
0001	Control Board
0010	Module
0011	Power Supply
0100	I/O Board
0101	Control Board
0110	Module
0111	Not Used
1000	Not Used
1001	Not Used
1010	Not Used
1011	Not Used
1100	Not Used
1101	Not Used
1110	Not Used
1111	Not Used
BIB4-6	Bus In Bits 4 through 6 are not used.
BIB7	Bus In Bit 7 indicates that valid status is available

Table Continued on Next Page

TABLE 3A-4. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
Bus Out Bits 0-1 11	Execute Diagnostic Test Command -- When Bus Out Bits 0 and 1 are "1", then Bus In Bits 0 through 6 are undefined and Bit 7 indicates that a diagnostic test is executing. For more information on Execute Diagnostic Test Command, see Diagnostic Functions in section 7.
TAG 6 -- DEVICE TYPE (SMD-E ONLY) Tag 6 (activating Tags 4 and 5 simultaneously) causes customer selected device type status to be returned on Bus In lines 0 through 7. Note: This tag is not usable when the unit is configured with Tag 1 Extended Addressing.	

UNIT SELECTION

The drive must be selected before it will respond to any commands from the controller. This is the case because the tag and bus bit receivers, as well as certain drivers, are not enabled until the drive is selected.

In both single- and dual-channel units, the select sequence is initiated by a Unit Select Tag signal from the controller. However, the sequence performed is different depending on whether a single or dual channel is being considered. Since only one controller can communicate with the drive at a time, dual-channel logic must solve the problem of priority when more than one controller wants to select the drive at the same time. The following paragraphs describe both single- and dual-channel selection.

SINGLE-CHANNEL UNIT SELECTION

The single-channel unit select sequence (see figure 3A-3) starts when the controller sends the Unit Select Tag accompanied by a logical address on the four unit select lines.

When the drive recognizes the Unit Select Tag, it compares its own logical address to the address sent by the controller. The drive's logical address is determined by switch settings on the operator panel (if installed) or by switch settings on the control board. This address can be any number from 0 to 15.

If the address sent by the controller is the same as that of the drive and if the Open Cable Detect signal is inactive (indicating the A cable is connected, controller has power, and the channel is not disabled), the drive enables its Select Compare signal.

The Select Compare signal enables the Unit Selected signal. The Select Compare signal also causes the Selected FF to set, thereby enabling the receivers and drivers to the controller. The drive is now ready to respond to further commands from the controller.

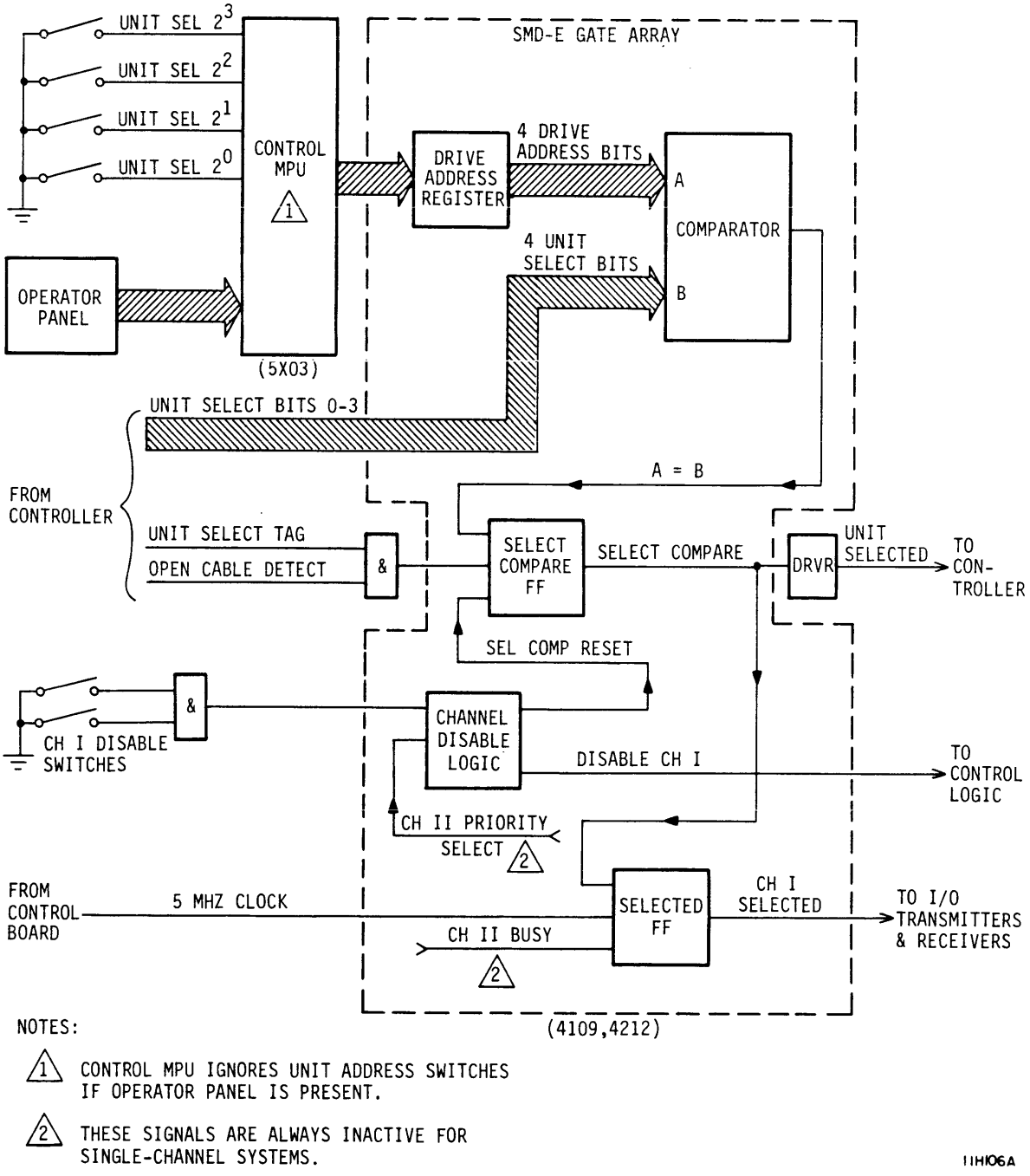


Figure 3A-3. Unit Select Logic (Single-Channel)

DUAL-CHANNEL UNIT SELECTION

General

Dual-channel drives are connected to, and can be selected by, either of two controllers. However, because the drive is capable of responding to only one controller at a time, the controllers must compete for use of the drive. For this reason, there are functions associated with dual-channel selection that are not necessary when selecting single-channel units.

The functions controlling dual-channel selection are as follows:

- Select -- Logically connects the drive to the controller, thus enabling it to respond to commands from the selecting controller.
- Reserve -- Reserves the drive so it can be selected at any time by the reserving controller, but prevents it from being selected by the other controller.
- Release -- Releases drive from reserved condition.
- Priority Select -- Allows controller to force select the drive by disabling the interface to the controller having the drive selected or reserved.
- Disable -- Allows disabling either channel interface during maintenance.

The following discussions describe each of these functions. Because these functions are basically the same regardless of which channel is involved, they are described only as they relate to Channel I. Figure 3A-4 shows the select logic associated with channel I selection and table 3A-5 describes the major elements on this figure. Figure 3A-5 is a flowchart of the dual-channel unit select and reserve functions.

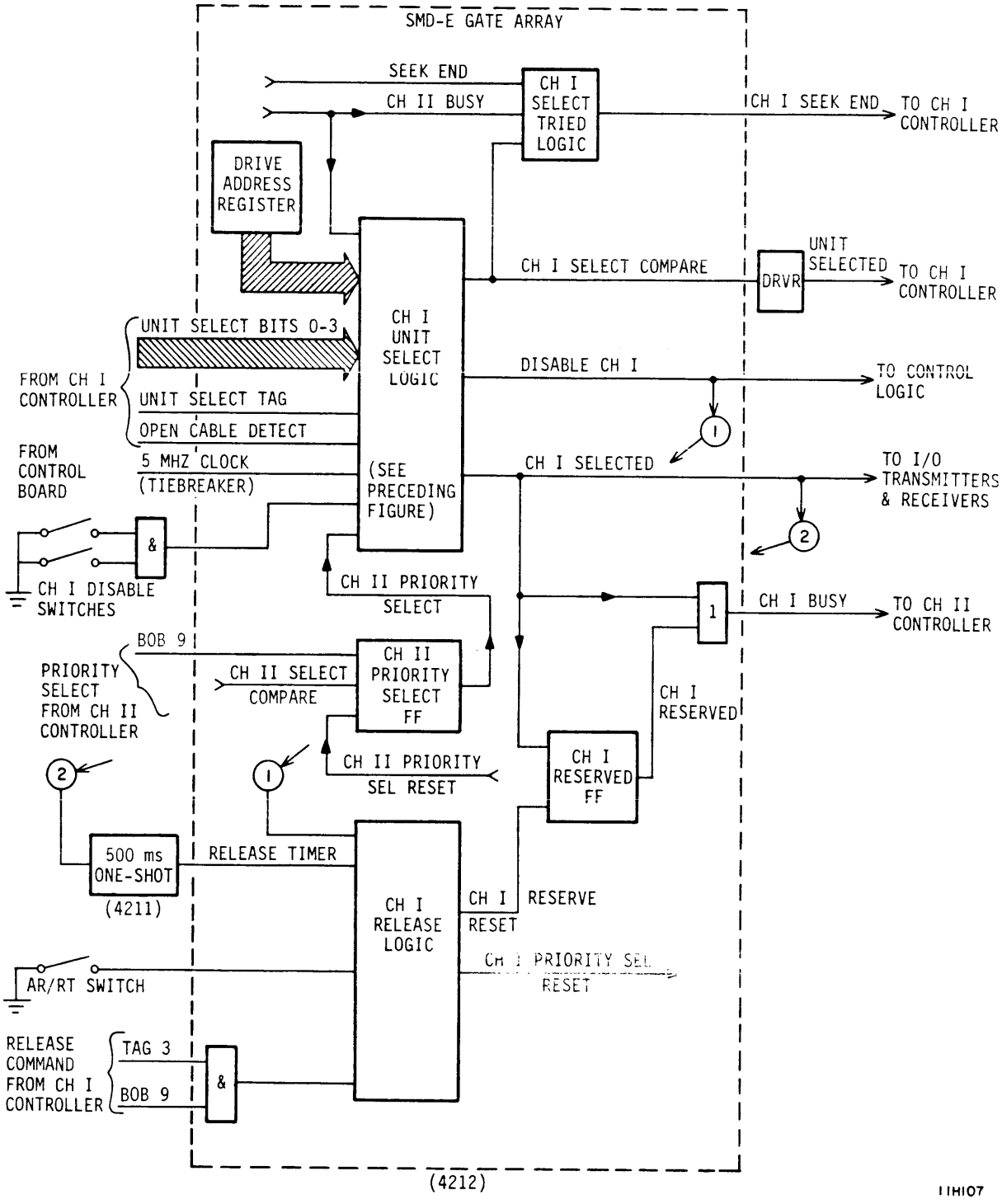


Figure 3A-4. Channel I Dual-Channel Logic

TABLE 3A-5. DUAL-CHANNEL UNIT SELECT CIRCUIT FUNCTIONS

Element*	Function
AR/RT Switch	Determines whether the drive will be in AR (absolute reserve) or RT (reserve timeout) mode. If switch is in RT position, drive is released from reserved condition 500 ms (nominal) after being deselected. If switch is in AR position, drive remains reserved until it receives either a release or priority select command.
Release Timeout One-Shot	Times out 500 ms after drive is deselected. If drive is in RT mode, the reserved FF is cleared when timeout occurs.
Channel I Disable Switches	Disable channel I whenever both switches are set to Disable position.
Channel I Priority Select FF	Sets if drive receives Priority Select command. This causes drive to be selected and reserved for controller issuing command and disables channel to other controller.
Channel I Reserved FF	Sets during select and reserve sequence. When set it keeps drive reserved to channel I until channel I releases or channel II issues a Priority Select command.
Channel I** Selected FF	Sets during select and reserve sequence and enables drivers and receivers to channel I controller.
Channel I Select and Compare Logic	Compares logical address of drive with that sent by controller (see Single-Channel Unit Selection).

Table Continued on Next Page

TABLE 3A-5. DUAL-CHANNEL UNIT SELECT CIRCUIT FUNCTIONS (Contd)

Element*	Function
Channel I Select Tried Logic	Sets a FF if channel I tries to select and reserve drive while it is already selected or reserved by channel II. When drive is deselected and released by Channel II, this FF clears and thereby triggers the Select Tried one-shot. The one-shot sends a pulse to controller on the Seek End line.

* Includes only those elements directly concerning channel I and shown in figure 3A-4.

** The Channel Selected FFs are alternately clocked by the 5 MHz Oscillator signal to prevent simultaneous selection.

Select And Reserve Function

The drive is both selected and reserved during the same sequence and this sequence is initiated by a Unit Select Tag accompanied by a logical address. However, the drive can be successfully selected and reserved only if none of the following conditions exist:

- Drive is already selected and reserved by other controller.
- Drive is not selected but is reserved by other controller.
- Channel to drive attempting selection has been disabled by either a priority select or disable function.

The following paragraphs describe how the drive is initially selected and also how it responds to a Unit Select Tag when it is selected, reserved, or disabled.

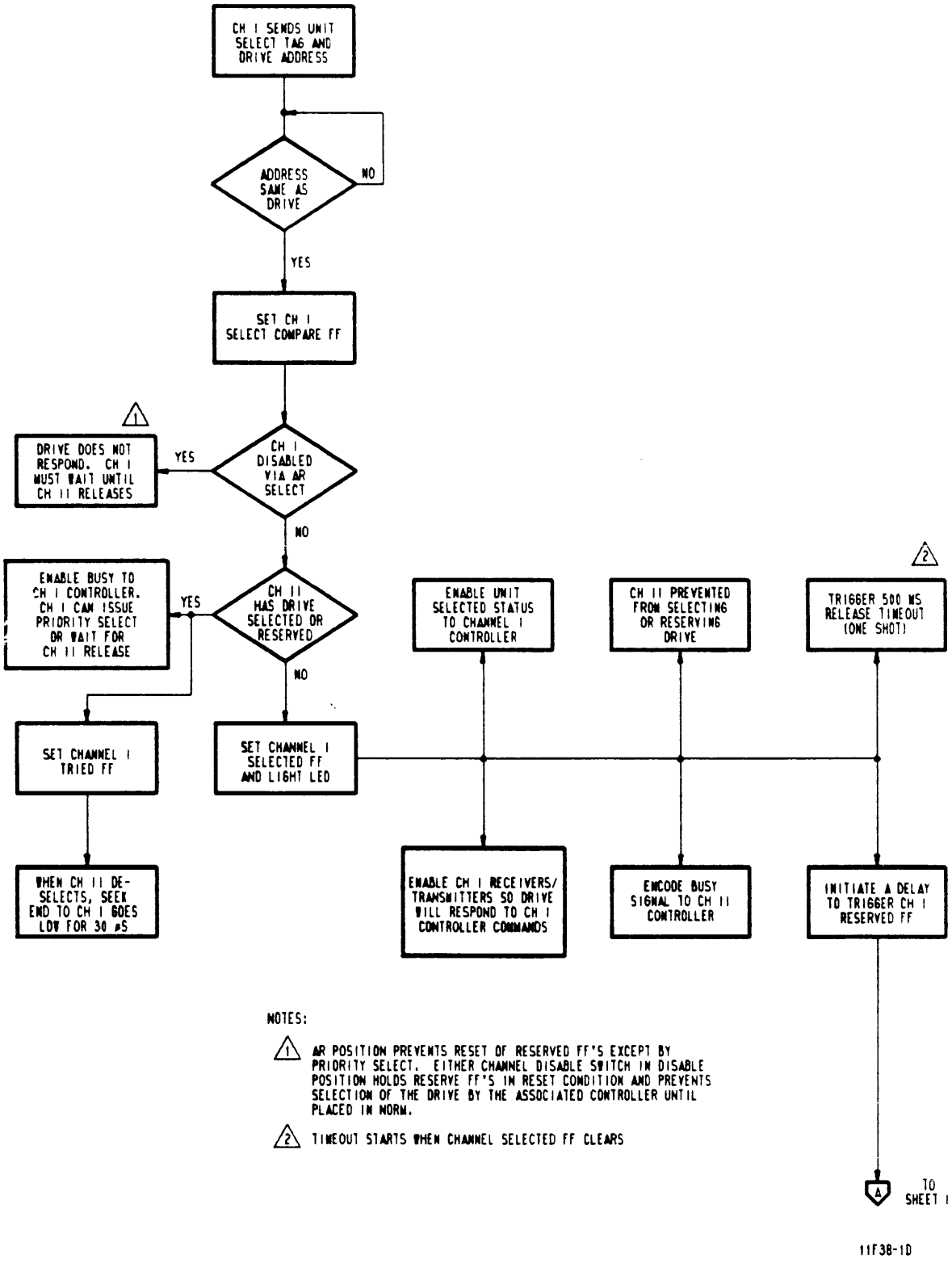


Figure 3A-5. Dual-Channel Selection Flowchart (Sheet 1 of 2)

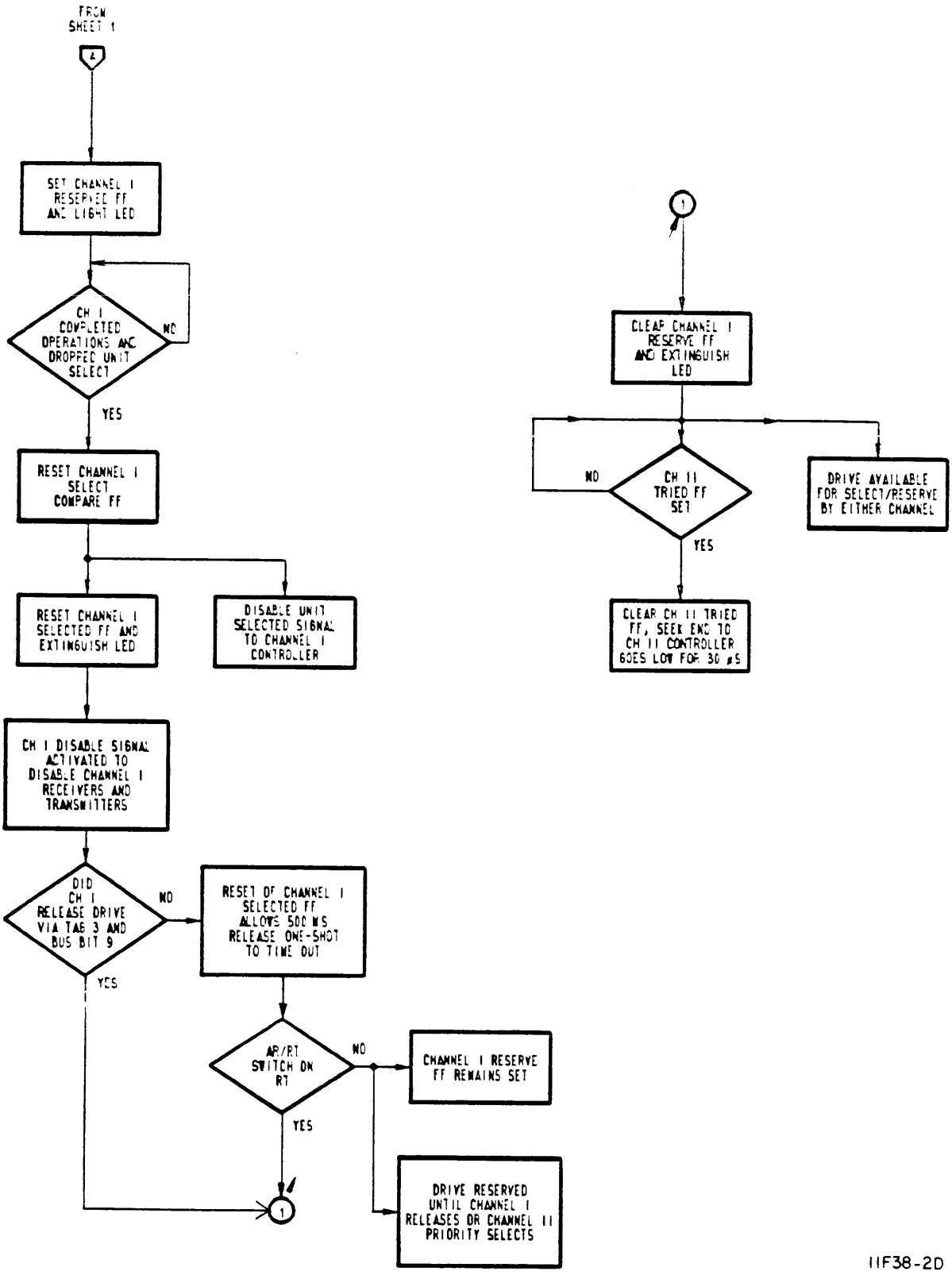


Figure 3A-5. Dual-Channel Selection Flowchart (Sheet 2)

Assuming the drive is available (not selected, reserved, or disabled) and it receives a Unit Select Tag and logical address from the controller on channel I, it compares the address received with that indicated by its logical address switches. If the two addresses are the same, the drive enables the Channel I Select Compare signal. The logic used to generate this signal is identical to that used in the single-channel units.

With the Channel 1 Select Compare signal active, the drive sends Unit Selected to the channel 1 controller. The Select Compare signal also causes the Channel I Selected FF to set, thereby enabling the receivers and drivers to the Channel I controller and triggering the Reserve one-shot. The output pulse from this one-shot clocks and sets the Channel I Reserved FF.

Providing channel II does not issue a priority select command (see Priority Select Function discussion), the drive remains selected to channel I until the controller on channel I drops its Unit Select Tag. At this time, the drive's Channel I Select Compare FF clears. This clears the Channel I Selected FF, thereby disabling the drivers and receivers for that channel. Clearing the Select Compare FF also disables the Unit Selected signal thus informing the controller that the drive will no longer respond to commands. However, the drive remains reserved to channel I (allowing channel I to reselect while preventing channel II from selecting) until the Channel I Reserve FF is also cleared. The Reserve FF is cleared by either a release or priority select function (refer to these discussions).

If channel I attempts to select and reserve the drive while it is selected and reserved by channel II, the Channel I Select Compare signal is still generated as during the initial select and reserve sequence. However, the Channel I Select and Reserve FFs do not set, and therefore the attempt is unsuccessful. The drive still sends the Channel I Unit Selected signal to the controller, but, in this case, it is accompanied by the Channel I Busy signal. The Busy signal indicates that the drive is selected or reserved by channel II.

The drive also sets its Channel I Tried FF, thus recording the unsuccessful attempt. When the drive is no longer selected or reserved by channel II, this FF clears, causing Seek End to the channel I controller to go low for 30 microseconds. This informs the channel 1 controller that the drive is no longer selected or reserved.

If the channel I controller tries to select the drive while channel I is disabled (either by a priority select or maintenance disable function), the attempt is unsuccessful and no response is sent back to the channel I controller.

Release Function

The release function will release the drive from either a reserved or priority selected condition. There are two types of release functions:

- Timeout release pulse
- Release command

The timeout release pulse is capable of releasing the drive from the reserved condition only. This pulse is generated by the 500 ms Timeout Release one-shot and releases the drive by clearing the Reserve FF. The pulse times out 500 ms after the drive is deselected (Select FF clears).

Whether or not the one-shot has any effect on the Release FF depends on the position of the AR/RT switch. If this switch is in the RT (reserve timeout) position, the FF clears when the one-shot times out, thus making the drive available to the other channel. However, if this switch is in AR (absolute reserve) position, the one-shot has no effect on the FF and the drive remains reserved.

A Release command will release the drive from both the reserved and priority selected conditions. This command is initiated by the reserving and/or priority selecting controller when it issues a Tag 3 (Control Select) with Bus Out Bit 9 active. This clears the Reserve and Disable FFs and allows the other controller to select the drive once the issuing controller drops its Unit Select Tag, and the Select FF for that channel has cleared.

Priority Select Function

If the drive is selected and reserved, the other controller can force selection by issuing a Priority Select command (Unit Select Tag accompanied by drive logical address and Bus Out Bit 9). This command will disable the channel to the controller presently using the drive and also select and reserve the drive to the controller issuing the Priority Select command.

For example if channel I has the drive and channel II wants to select, channel II issues a Priority Select command. In this case, the command sets the Channel I Disable FF which in turn results in clearing the Channel I Selected and Reserved FFs. It also sets the Channel II Selected and Reserved FFs, thereby selecting and reserving the drive for channel II.

Once the Disable FF is set, that channel (in this case channel I) is disabled until the other controller (in this case channel II) issues a command to clear it.

Disable Function

It is also possible to disable either channel by setting both Disable switches for that channel (refer to figure 3A-4) to the DISABLE position.

SECTION 3B

SCSI INTERFACE FUNCTIONS

SCSI INTERFACE FUNCTIONS 3B

INTRODUCTION

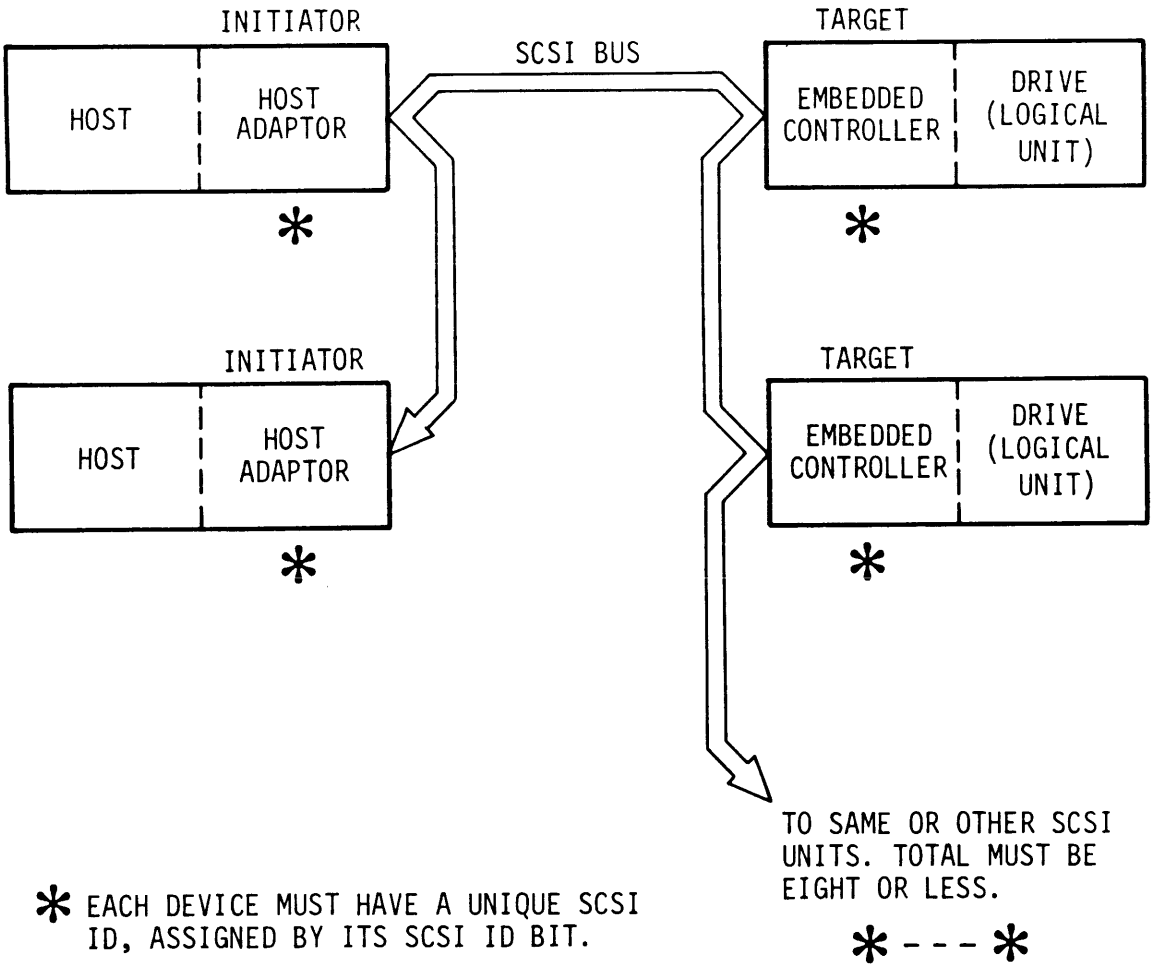
The following descriptions of the Small Computer System Interface (SCSI) bus are intended to provide an overview of the interface and the associated drive hardware. It is beyond the scope of this manual to provide a detailed description of all the features, capabilities, variations, and protocol of the SCSI. This information is provided in the specification for the Small Computer System Interface (document 64721701).

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals, and read/write data transfers. The interface consists of the I/O cables and the logic (I/O board) required to process the signals sent between drive and controller.

SCSI BUS CONFIGURATION

Figure 3B-1 illustrates the configuration of the SCSI bus. The SCSI bus can have a maximum of eight devices connected to it and communication can occur between any two devices at any given time. The device that originates an operation is an initiator and the device that performs the operation is the target.

The disk drive uses one shielded or unshielded I/O cable to attach it to the SCSI bus. Shielded cables are typically used where electromagnetic compatibility (EMC) and electrostatic discharge (ESD) protection are required. A typical use of unshielded cables might be in a customer-supplied cabinet or enclosure where the cabinet or enclosure itself provides the EMC and ESD protection. Unshielded cables must be supplied by the customer. The I/O cable carries commands, data, and status information across the SCSI bus. Figure 3B-2 shows the lines (except those not used) in the I/O cable. The function of each of these lines is explained in table 3B-1.



DATA BUS BIT	DB(7)	DB(6)	DB(5)	DB(4)	DB(3)	DB(2)	DB(1)	DB(0)
SCSI ID	7	6	5	4	3	2	1	0

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Figure 3B-1. SCSI Bus Configuration

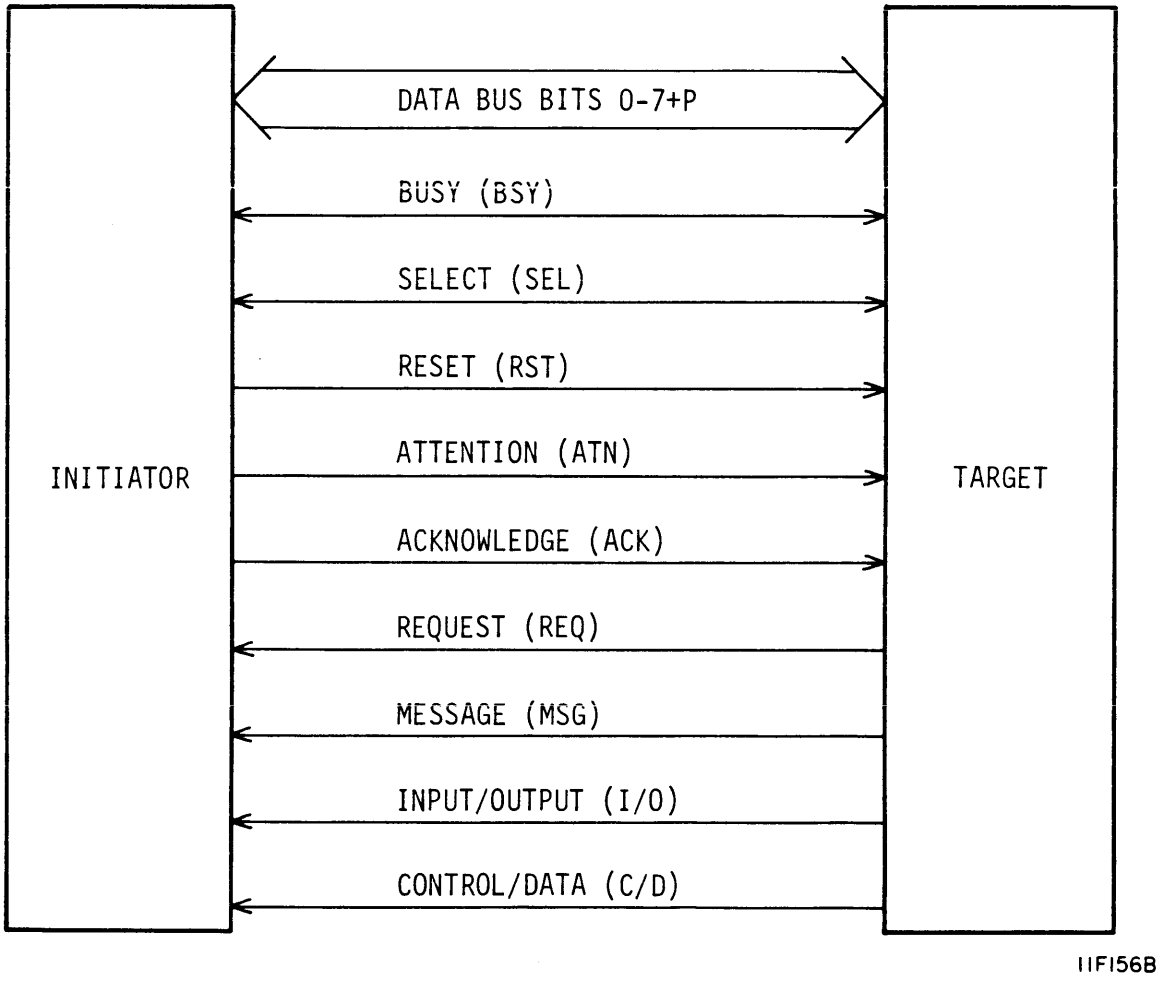

Figure 3B-2. SCSI Bus Signal Lines

TABLE 3B-1. SCSI BUS SIGNAL LINES

Signal	Source	Function
DATA BUS (DB 7-0+P)	I - T	Eight data-bit signals, plus a parity bit signal that form the DATA BUS. DB(7) is the most-significant bit and has the highest priority during the ARBITRATION phase. Bit number, significance, and priority decrease downward to DB(0). A data bit is defined as one when the signal is true and zero when false. Data parity DB(P) is odd. The use of parity is a switch-selectable option and is not valid during the ARBITRATION phase.
BUSY (BSY)	I - T	An "or-tied" signal that indicates to the initiator or target that the bus is being used.
SELECT (SEL)	I - T	Used by an initiator to select a target, or by a target to select an initiator.
RESET (RST)	I - T	An "or-tied" signal that indicates the reset condition exists.
ATTENTION (ATN)	I	Driven by an initiator to indicate ATTENTION condition.
ACKNOWLEDGE (ACK)	I	Driven by initiator to acknowledge a REQ/ACK data transfer handshake.
REQUEST (REQ)	T	Driven by target to indicate a request for a REQ/ACK data transfer handshake.
MESSAGE (MSG)	T	Driven by target during message phase.
INPUT/ OUTPUT (I/O)	T	Driven by target to control the direction of data movement on the DATA BUS with respect to an initiator. True indicates input to the initiator. Also used to distinguish between SELECTION and RESELECTION phases.
CONTROL/DATA (C/D)	T	Driven by target to indicate whether CONTROL or DATA information is on the DATA BUS. True indicates CONTROL.
T = Target I = Initiator		

SCSI CONTROLLER

The I/O board is available in two versions -- the standard SCSI controller and the high-performance SCSI controller. They are discussed separately in the topics that follow.

STANDARD SCSI CONTROLLER

Figure 3B-3 illustrates the standard SCSI controller (I/O board) in block diagram form. The controller is contained on the single I/O board mounted at the rear of the drive. It is organized around a disk formatter/buffer controller, an I/O microprocessor unit (I/O MPU), controller/drive interface chip (CDIC), and the SCSI Bus Controller (SBC).

The disk formatter/buffer controller functions are combined on one VLSI chip. The controller has a separate data and microprocessor bus. The disk formatter/buffer controller provides an interface between the two busses, a data path between the I/O MPU, dynamic buffer memory, and FIFO logic. The microprocessor bus provides a path for transmission of control and status information between the disk formatter/buffer controller, I/O MPU, EPROM, CDIC, and the transceivers.

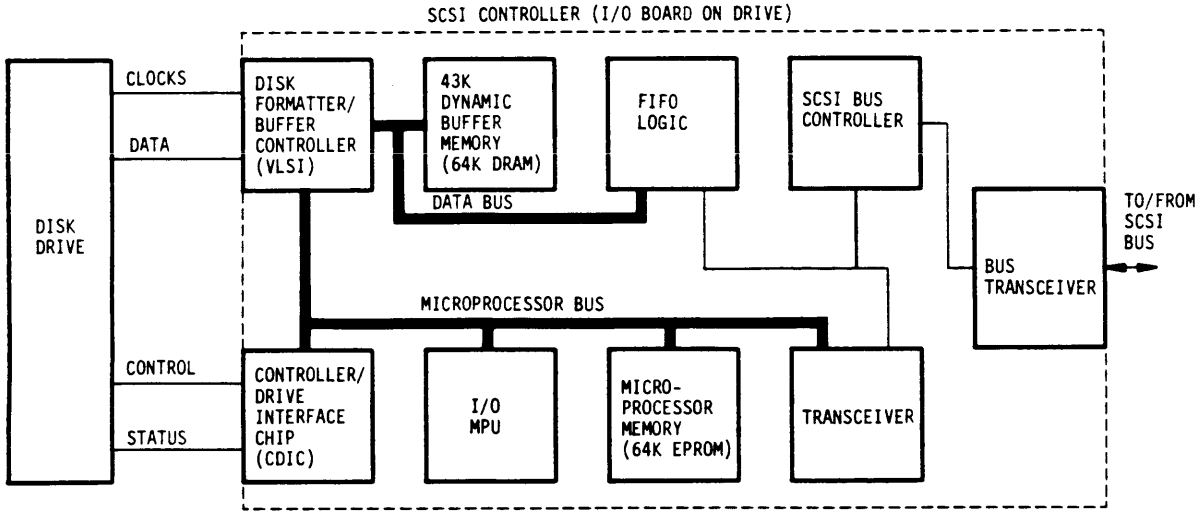

Figure 3B-3. Standard SCSI Controller Block Diagram

Disk Formatter And Buffer Controller

The disk formatter, in conjunction with the I/O MPU, handles the read and write operations. The buffer controller is a three-channel, direct-access controller. It controls data movement in or out of a dynamic buffer memory and provides the interface between the I/O MPU and data bus.

The buffer controller performs the following operations:

- Handles addressing and controls operations for the disk formatter
- Handles addressing and control operations for the SCSI Bus Controller (SBC)
- Handles dynamic memory timing and refresh
- Performs parity checking and generation for the dynamic buffer memory
- Connects the MPU bus to the data bus
- Decodes the MPU address for the dynamic buffer memory and the internal I/O space
- Determines priority of buffer memory access

I/O MPU

The I/O MPU, disk formatter, and CDIC control all disk drive operations, including drive control, head positioning, and reading drive status. The disk formatter controls formatting of the data written to and read from the disk. The I/O MPU issues read and write commands that are executed by the disk formatter. All read and write commands involve operations on a single data block.

Controller/Drive Interface Chip (CDIC)

The CDIC connects the MPU bus to the drive control interface. Two multiplexed address/data ports are provided -- Port 0 for the controller and port 1 for the drive. This chip serves as an interface between the drive electronics and the SCSI controller.

SCSI Bus Controller (SBC)

The SBC contains the arbitration, parity, and synchronous transfer control logic as well as the SCSI protocol logic. The SCSI Bus signal lines reach the SBC through the transceivers.

Transceivers

One group of transceivers connects signals on the SCSI Bus signal lines to the SBC. Another group of transceivers connects the MPU bus to the SBC.

HIGH-PERFORMANCE SCSI CONTROLLER

Figure 3B-4 illustrates the high-performance SCSI controller (I/O board) in block diagram form. The controller is contained on the single I/O board mounted at the rear of the drive. It is organized around the merged architecture controller (MAC) chip, an I/O microprocessor unit (I/O MPU), controller/drive interface chip (CDIC), and the enhanced SCSI protocol (ESP) chip.

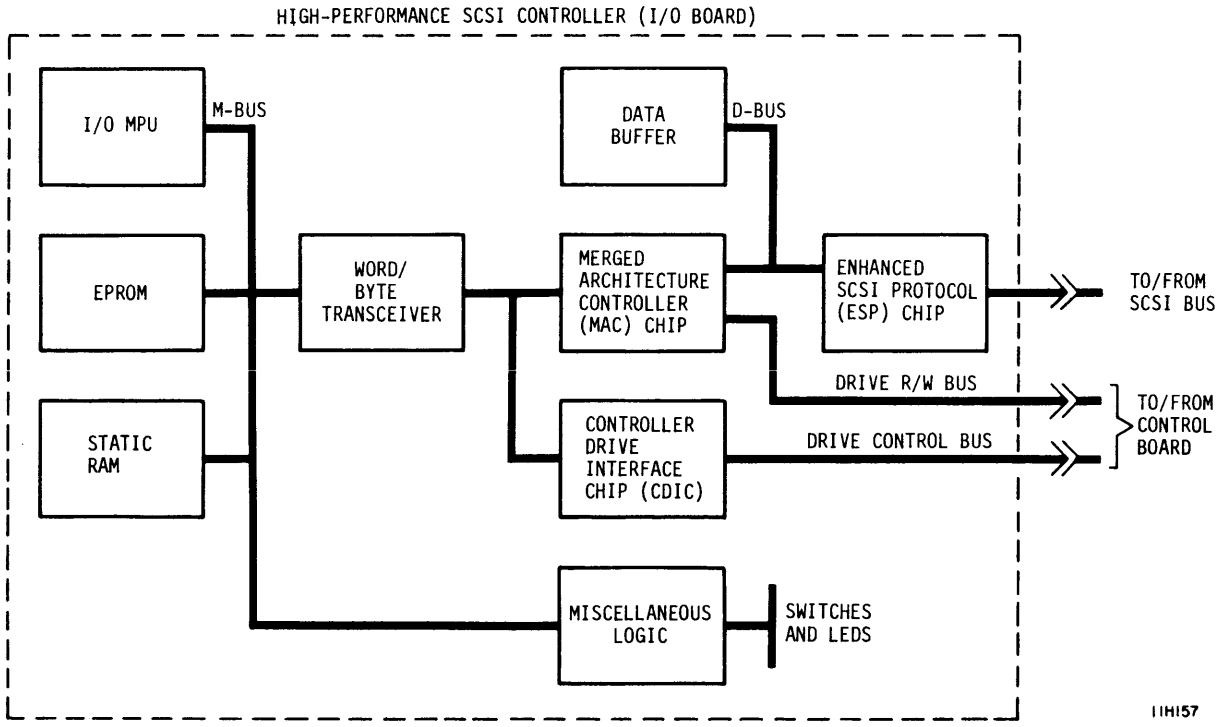

Figure 3B-4. High-Performance SCSI Controller Block Diagram

Two completely separate busses are used in the controller: the data bus and the microprocessor bus. The MAC chip provides an interface between the two busses, and a data path between the I/O MPU, dynamic buffer memory, and the ESP. The microprocessor bus provides a path for data, control, and status information between the MAC chip, the I/O MPU, the EPROM, the CDIC, and the transceivers.

MAC Disk Formatter

The disk formatter circuit, in conjunction with the I/O MPU, handles the read and write operations of the disk drive.

MAC Buffer Controller

The buffer controller is basically a three-channel Direct Memory Access (DMA) controller. The buffer controller controls data movement in or out of a dynamic buffer memory and provides the interface between the microprocessor bus and the data bus.

The buffer controller circuit provides the address and control for multiple controller activities that access the dynamic buffer memory. The buffer controller performs the following operations:

- Handles addressing and DMA operations for the disk formatter
- Handles addressing and DMA operations for the ESP chip
- Handles dynamic memory timing and refresh
- Performs parity checking and generation for the dynamic buffer memory
- Connects the microprocessor bus to the data bus
- Determines priority of buffer memory access
- Decodes the MPU address for the dynamic buffer memory and the internal I/O space in the controller

I/O MPU

The I/O MPU, in conjunction with the MAC disk formatter and CDIC, controls all disk drive operations. The disk operations include drive control, head positioning, and reading drive status. During disk operations, the MAC disk formatter controls formatting of the data written to and read from the disk. The I/O MPU issues read and write commands that are executed by the MAC disk formatter. All read and write commands involve operations on a single data block.

Controller/Drive Interface Chip (CDIC)

The CDIC connects the microprocessor bus to the drive control interface. Two multiplexed address/data ports are provided -- Port 0 for the controller and port 1 for the drive. This chip serves as an interface between the drive electronics and the SCSI controller.

Enhanced SCSI Protocol (ESP) Chip

The ESP contains the arbitration, parity, and synchronous transfer control logic as well as the SCSI protocol logic. The SCSI Bus signal lines reach the SBC through the transceivers.

I/O SIGNAL PROCESSING

The following paragraphs describe the basic SCSI Bus communication process. They describe the bus PHASES, command set, messages, and a typical command sequence.

SCSI BUS PHASES

Communication on the SCSI Bus occurs in eight phases depending on the type of operation or information transfer being performed. The bus phases pertain to the condition or state of the lines at a given time. The SCSI Bus can never be in more than one phase at any given time. The SCSI Bus Phases are listed and described in table 3B-2.

TABLE 3B-2. SCSI BUS PHASE DESCRIPTIONS

Phase	Description
BUS FREE	No SCSI device is asserting BUSY or SELECT for at least one bus settle delay.
ARBITRATION	Allows one SCSI device to gain access to the bus based on its priority ID bit.
SELECTION	Allows an initiator to select a target. The I/O line must not be asserted in this phase.
RESELECTION	Allows a target to reconnect to an initiator so it can continue an operation started by an initiator, but suspended by the target before it was complete. The I/O line must be asserted during this phase.
COMMAND	Allows the target to request command information from the initiator.
DATA	The DATA IN phase allows the target to request that data be sent to the initiator from the target. The DATA OUT phase allows the target to request that data be sent from the initiator to the target.
STATUS	Allows the target to request that status information be sent from the target to the initiator.
MESSAGE	The MESSAGE IN phase allows the target to request that messages be sent to the initiator from the target. The MESSAGE OUT phase allows the target to request that messages be sent from the initiator to the target. The target can invoke this phase at its convenience, in response to ATTENTION created by the initiator.

SCSI COMMAND EXECUTION

Figure 3B-5 illustrates the basic flow of a command sequence. The sequence illustrated cannot and does not represent all variations. Refer to specification 64721701 for command descriptions, execution details, and timing constraints. The command set for the drive is shown in table 3B-3.

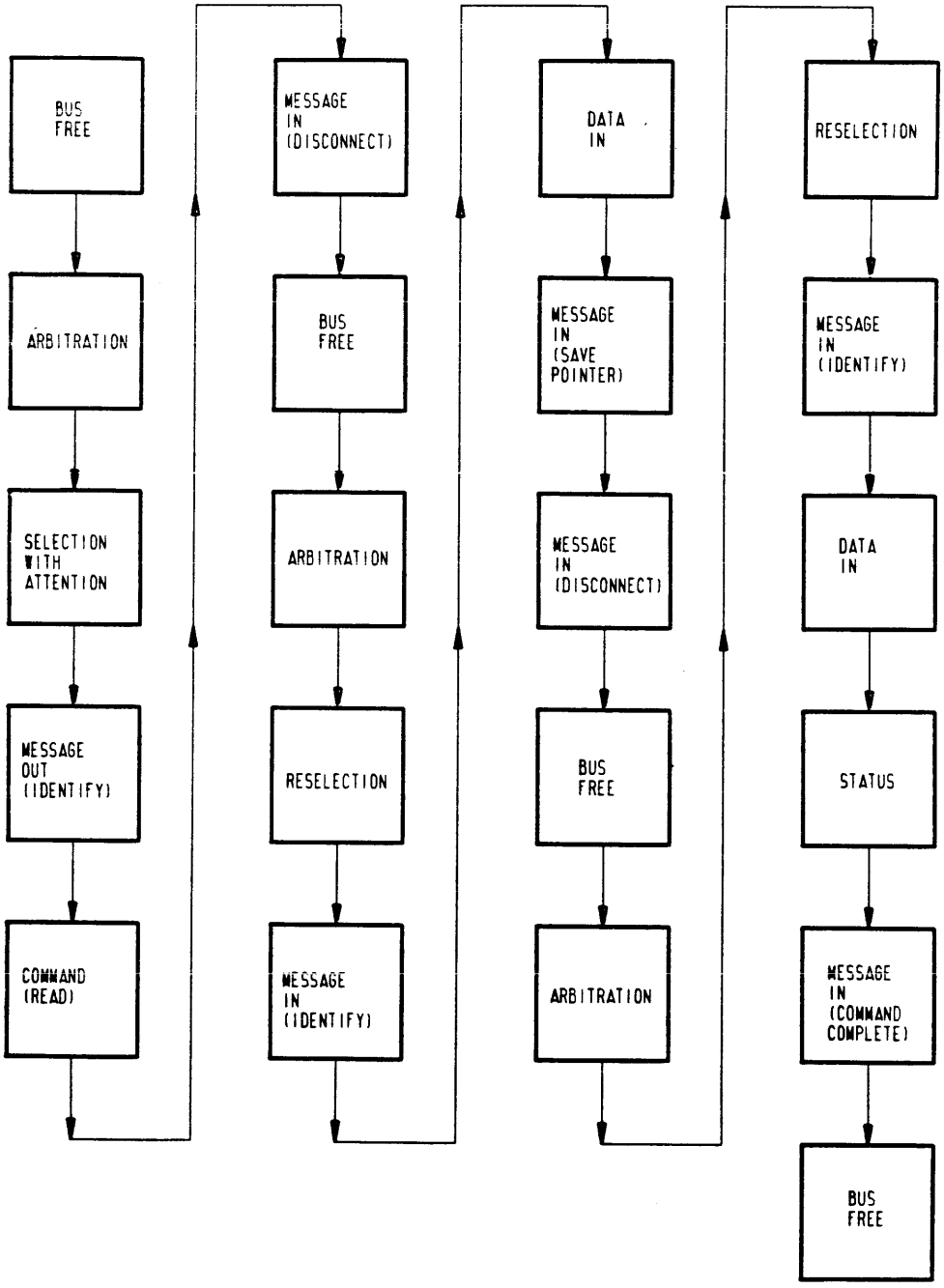

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Figure 3B-5. Sequence of Typical Commands

TABLE 3B-3. COMMAND SET

Op Code	Type	Command Name
Group 0 Commands For Direct Access Devices		
00	M	TEST UNIT READY
01	M	REZERO UNIT
02	R	
03	M	REQUEST SENSE
04	M	FORMAT UNIT
05-06	R	
07	M	REASSIGN BLOCKS
08	M	READ
09	R	
0A	M	WRITE
0B	M	SEEK
0C-11	R	
12	M	INQUIRY
13-14	R	
15	M	MODE SELECT
16	M	RESERVE
17	M	RELEASE
18	O	COPY (Not Supported)
19	R	
1A	M	MODE SENSE
1B	O	START/STOP UNIT
1C	O	RECEIVE DIAGNOSTIC RESULTS
1D	M	SEND DIAGNOSTIC
1E	O	PREVENT/ALLOW MEDIA REMOVAL (Not Supported)
1F	R	

Table Continued on Next Page

TABLE 3B-3. COMMAND SET (Contd)

Oper	Type	Command Name
Group 1 Commands For Direct Access Devices		
20-24	R	
25	M	READ CAPACITY
26-27	R	
28	M	READ EXTENDED
29	R	
2A	M	WRITE EXTENDED
2B	M	SEEK EXTENDED
2C-2D	R	
2E	O	WRITE & VERIFY
2F	O	VERIFY
30-36	R	
37	M	READ DEFECT DATA
38-3A	R	
3B	M	WRITE DATA BUFFER
3C	M	READ DATA BUFFER
3D-3F	R	
Group 7 Commands For Direct Access Devices		
E8	VU	READ LONG
EA	VU	WRITE LONG

M = mandatory R = reserved
O = optional VU = vendor unique

As shown in figure 3B-5, the communication sequence starts with the SCSI Bus in the BUS FREE phase. This phase indicates no other SCSI devices are using the bus and it is free for use by other devices. Each device detects the BUS FREE phase when the SELECT and BUSY lines are both false.

The BUS FREE phase is followed by an ARBITRATION phase where the initiator attempts to gain access to the BUS. Access to the bus is based on the device priority ID bit. ARBITRATION occurs when the device asserts BUSY and its ID on the DATA BUS. This ID bit is a single bit on the DATA BUS that corresponds to the unique SCSI address assigned to each device when it was installed. The other seven bits are released by the SCSI device. The SCSI device examines the DATA BUS. If a higher priority SCSI ID bit is true (DATA BUS BIT 7 is the highest) the SCSI device loses arbitration and the device releases its signals. If no higher priority bit is true, the device wins arbitration.

Having won the ARBITRATION, the initiator selects the target (SELECTION phase). The initiator places the SCSI ID of the target on the bus (asserts the DATA BUS bit), as well as its own ID. After a delay, the initiator asserts the SELECT line. The target determines it is selected when its SCSI Bus ID bit and the SELECT line are true, and the BUSY and I/O lines are false. Selection with ATTENTION informs the target that the initiator has a message ready.

The selected device responds to the initiator by entering the MESSAGE OUT phase. In this phase, the target requests that the initiator send messages to it. The MESSAGE, CONTROL/DATA, and INPUT/OUTPUT lines are used in combinations to indicate the various information transfer phases. The state of the three signal lines is controlled by the target and the phase selected by the state of these three signal lines is shown in table 3B-4. In this example, the IDENTIFY message is the first message sent by the initiator after the SELECTION phase. This message identifies the physical path for the logical unit (only logical unit 0 is supported) specified by the initiator. The IDENTIFY message is also the first message sent by the target following the RESELECTION phase.

The initiator can request a MESSAGE OUT phase by asserting ATTENTION. Message codes and the direction of information flow are shown in table 3B-5.

TABLE 3B-4. INFORMATION TRANSFER PHASES

MSG	C/D	I/O	Phase Name	Direction Of Transfer
0	0	0	DATA OUT	Initiator to target
0	0	1	DATA IN	Initiator from target
0	1	0	COMMAND	Initiator to target
0	1	1	STATUS	Initiator from target
1	0	0	Reserved	
1	0	1	Reserved	
1	1	0	MESSAGE OUT	Initiator to target
1	1	1	MESSAGE IN	Initiator from target
0 = False, 1 = True				

Following the MESSAGE OUT phase, the initiator responds to the COMMAND phase and, in this example, issues a READ command to the drive. The MESSAGE IN phase is entered (DISCONNECT message) followed by the BUS FREE phase. The ARBITRATION phase is again entered, followed by the RESELECTION and the MESSAGE IN (IDENTIFY message) phases. The requested read data is then transferred to the initiator.

Following the DATA IN phase, the target enters the MESSAGE IN phase and, in this example, requests the initiator to SAVE DATA POINTER. There are current (also called active) pointers that represent the state of the interface and point to the next command, data, or status byte to be transferred between the initiator's memory and the target. Current pointers are used with the target currently connected to the initiator.

TABLE 3B-5. MESSAGE CODE DESCRIPTIONS

Oper Code	Target	Init.	Description	Direction In	Direction Out
00	M	M	Command Complete	X	
01	O	O	Sync Data Transfer Request	X	X
02	M	O	Save Data Pointer	X	
03	M	O	Restore Pointers	X	
04	M	M	Disconnect	X	
05	M	O	Initiator Detected Error		X
06	M	M	Abort		X
07	M	M	Message Reject	X	X
08	M	M	No Operation		X
09	M	M	Message Parity Error		X
0A	O	O	Linked Command Complete	X	
0B	O	O	Linked Command Comp. With Flag	X	
0C	M	O	Bus Device Reset		X
0D-7F	R	R	Reserved Codes	-	-
80-FF	M	M	Identify*	X	X

* = Identify messages establish the communication path connection between an initiator and target for a logical unit.
Bit 7 = 1: Indicates an IDENTIFY message.
Bit 6 = 1: Indicates the initiator allows disconnection and reselection.
Bit 5 - 3: These bits are reserved.
Bit 2 - 0: Specify a logical unit in a target

M = Command implementation is mandatory.
O = Command implementation is optional.
R = Command implementation is reserved.

In = Direction of transfer is target to initiator.
Out = Direction of transfer is target from initiator.

Another set of pointers called saved pointers are provided for each active command, whether or not it is currently connected. The command pointer points to the start of the command descriptor block for that command. The saved data pointer points to the start of the data area at the beginning of each command and it remains at this value until the target sends the SAVE DATA POINTER message to the initiator. In response to this message, the initiator stores the value of the current data pointer into the saved data pointer. Only the saved pointer values are retained when a device disconnects from the bus. The current pointer values are restored from the saved values at the next reconnection.

At this point, the MESSAGE IN phase is entered with a DISCONNECT message code. Following the disconnect, the bus is in the BUS FREE phase in preparation for the ARBITRATION and RECONNECTION phases. RESELECTION is a phase that allows the target to reconnect to the initiator so it can continue an operation that was started by an initiator, but suspended by the target before it was complete.

The sample process continues with the MESSAGE IN and DATA IN phases previously described. The STATUS phase occurs at the end of the operation. It allows the target to send status information to the initiator. Status codes are contained in bits 4 - 1 of the status byte. The various codes are shown in figure 3B-6. The process ends with the MESSAGE IN phase and a COMMAND COMPLETE message followed by the BUS FREE phase.

BIT	7	6	5	4	3	2	1	0
BYTE 00	0	0	0	← STATUS BYTE CODE →				

BIT 7 IS RESERVED AND IS ALWAYS ZERO.

STATUS BYTE
CODE
00 = GOOD
02 = CHECK CONDITION
08 = BUSY
10 = INTERMEDIATE/GOOD
18 = RESERVATION CONFLICT

04 = CONDITION MET/GOOD AND 14 = INTERMEDIATE CONDITION MET/GOOD ARE NOT USED IN THESE DRIVES.

NOTE: CODES 06, 0A, 0C, 0E, 12, 16, 1A, 1C, AND 1E ARE RESERVED.

Figure 3B-6. Status Codes

SECTION 3C

IPI INTERFACE FUNCTIONS

IPI INTERFACE FUNCTIONS 3C

INTRODUCTION

This section provides an overview of the Intelligent Peripheral Interface (IPI) and associated drive hardware. This drive-to-controller interface uses commands defined in the Level 2 (IPI-2) specification developed by the American National Standards Institute (ANSI). Level 2 refers to the commands that are used to control drive-dependent operations.

It is beyond the scope of this manual to provided a detailed description of all the features, capabilities, variations, and protocol of the IPI interface. This information is provided in the Interface Specification for IPI-2 Intelligent Peripheral Interface (document 64731600).

The interface is the communications channel between the controller and the drive. Many of these communications are enabled only when the controller has the drive selected. This section is divided into the following areas:

- Interface Operation -- Describes the signal lines on the interface and shows how the interface transfers commands, status, and data.
- Unit Selection -- Describes drive selection by either of two controllers.

INTERFACE OPERATION

All communications between drive and controller must pass through the interface. It provides high-speed transfer of commands, responses, and data between controller and drive.

The interface consists of the I/O cables and the logic required to process the signals sent between drive and controller.

I/O CABLES

The drive has one I/O cable per port. This cable is a 50-conductor, twisted-pair cable. It contains all the interface lines going between the drive and controller. Figure 3C-1 shows the interface lines in the cable. The function of each of the lines is summarized in table 3C-1.

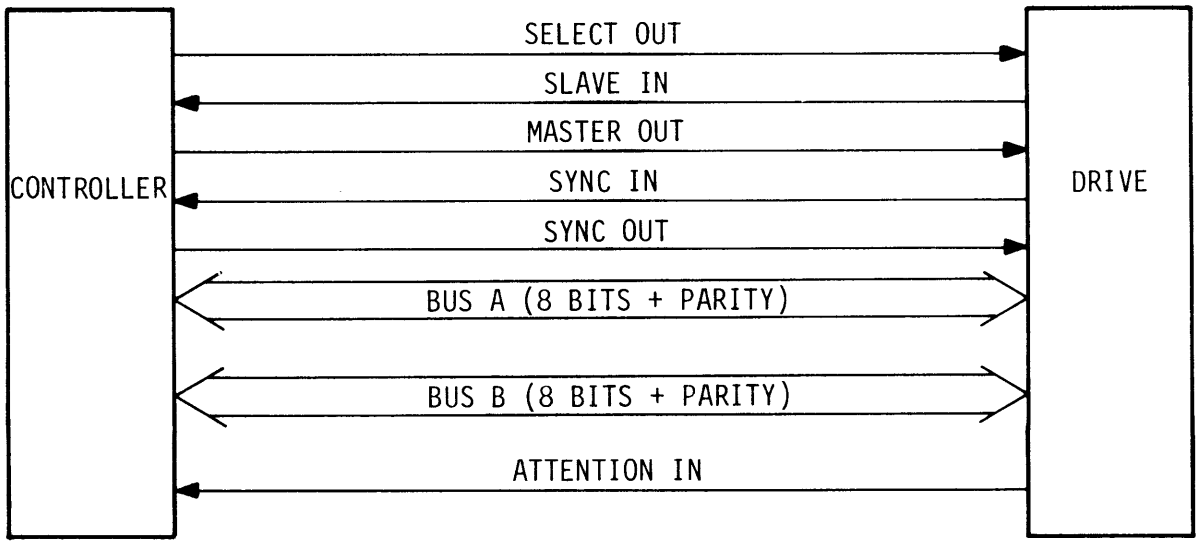


Figure 3C-1. Interface Lines

TABLE 3C-1. INTERFACE LINES

Signal	Source	Function
Bus A	C - D	Nine bidirectional lines: Bits 0 - 7 plus an odd parity bit. During command and control sequences, Bit 7 is the most significant bit. The controller uses Bus A for all control sequences. Data is transferred in parallel over Bus A and Bus B.
Bus B	C - D	Like Bus A except that the drive uses Bus B for all control sequences.
Select Out	C	Selects the drive and maintains the selection.
Slave In	D	Acknowledges controller-started control sequences and request sequences. Ends information transfers.
Master Out	C	Starts or stops information transfers and certain control sequences.
Sync In	D	During information transfers to the drive, indicates that the drive is ready to receive information. During information transfers to the controller, indicates that the drive has placed valid information on the buses.
Sync Out	C	During information transfers to the drive, indicates that the controller has placed valid information on the buses. During information transfers to the controller, indicates that the controller has accepted the information. Goes active to start each bus control sequence.
Attention In	D	Informs the controller that one or more drives that require service. When certain interrupts go active, the drive activates Attention In, provided that no drive is selected.
C = Controller		D = Drive

I/O CIRCUIT DESCRIPTION

This topic provides a brief overview of the circuit elements in the available I/O boards. One I/O board is used in drives that have one read/write channel (standard read/write). The other I/O board is used in drives that have two read/write channels (parallel read/write). Details of I/O protocol are discussed later in this section. For the purpose of this discussion, consider the following types of interface activities:

- Drive Control -- A command bus control sequence sent to the drive, followed by the appropriate parameters.
- Drive Status -- A response bus control sequence sent to the drive, causing the drive to return status information to the controller.
- Read/Write Operation -- Following an input/output sequence to the drive, a data transfer between the controller and the drive.

I/O Board With Standard Read/Write

Figure 3C-2 is a block diagram of the I/O board used with drives that have standard read/write electronics. The two Interface Protocol Circuits (IPC chips) along with the SERDES/Formatter Circuit (SFC chip) are responsible for interpreting all bus control sequences. The IPC directs all bus controls to the proper circuits where they are interpreted and executed. Command/response bus controls are directed to the I/O MPU; data bus controls are directed to the SFC chip.

The SFC chip provides the means to format, record, and recover data on the drive. After the operating mode and data format have been established in the SFC chip, it can execute all data bus controls without further assistance.

The SERDES (SERialize/DESerialize) function, performed by the SFC chip, is required because parallel data is transferred on the IPI interface while serial data is transferred to and from the drive read/write circuits. Serializing write data consists of moving 8-bit bytes from a buffer in the IPC chip to a shift register in the SFC chip. Data shifts out of the register one bit at a time to the write circuits. Deserializing read data is the reverse process, changing serial data from the read circuits into parallel data for the interface.

The I/O MPU is an 8-bit microcontroller that interprets and executes all command/response bus controls along with their parameters. The I/O MPU also becomes involved when master status is received, slave status is required, or an error occurs. The I/O MPU monitors changes in drive status through discrete inputs and MPU bus inputs from the Controller-Device Interface Chip (CDIC). The I/O MPU can perform some limited diagnostics on the read/write circuits in the SFC chip.

The CDIC contains the cylinder address register, the head address register, the fault latches and fault register, the head increment circuitry, and other control circuits. The CDIC acts as the interface for any information passed between the I/O MPU and the Control MPU.

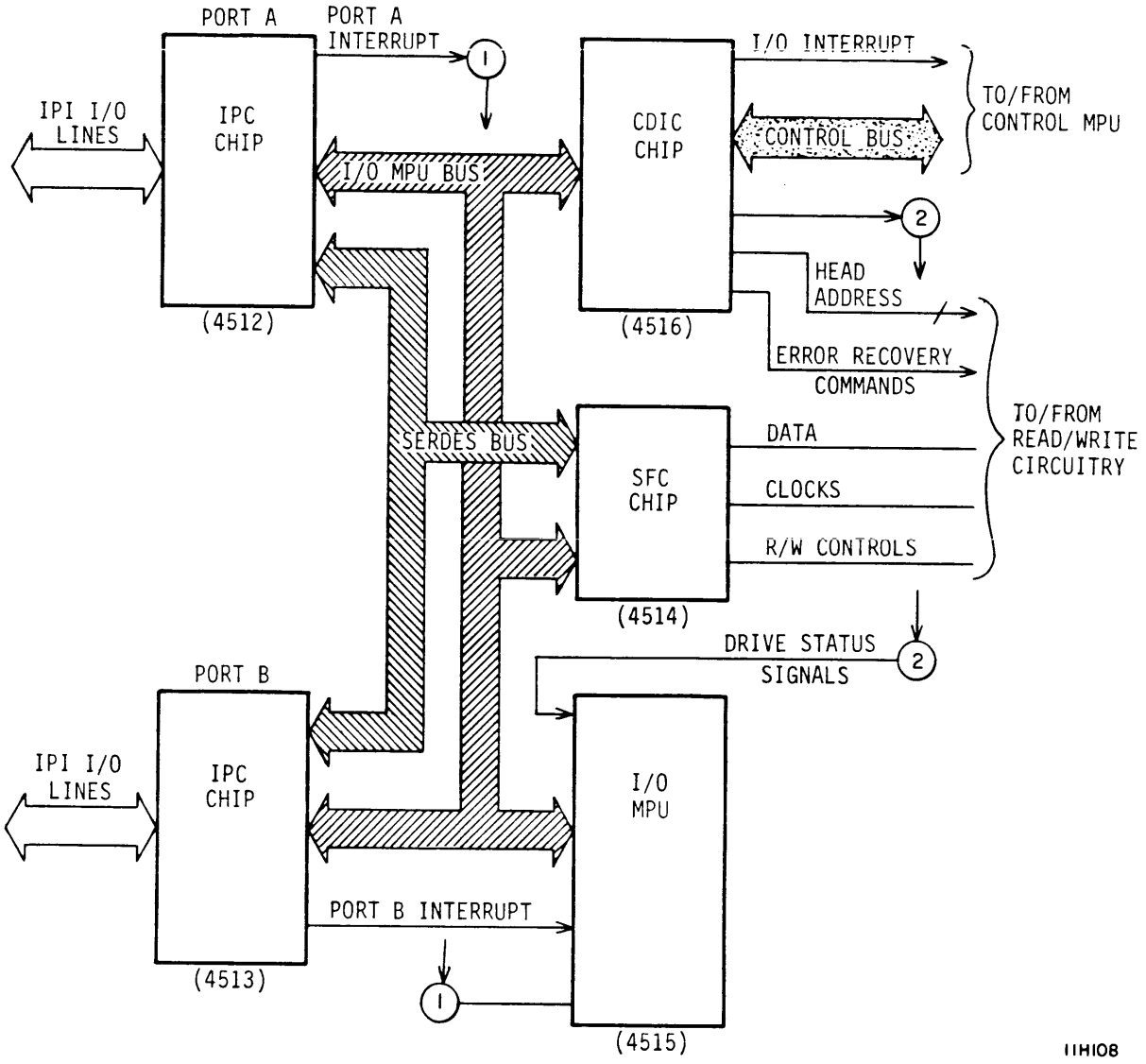


Figure 3C-2. IPI I/O Block Diagram (Standard Read/Write)

I/O Board With Parallel Read/Write

Figure 3C-3 is a block diagram of the I/O board used with drives that have parallel read/write electronics. The IPIP Array is responsible for interpreting all bus control sequences. This LSI chip directs all bus controls to the proper circuits where they are interpreted and executed. Command/response bus controls are directed to the I/O MPU; data bus controls are processed within the IPIP Array.

The IPIP Array provides the means to format, record, and recover data on the drive. After the operating mode and data format have been established in the chip, it can execute all data bus controls without further assistance.

The SERDES (SERialize/DESerialize) function, performed by the IPIP Array, is required because parallel data is transferred on the IPI interface while two channels of serial data are transferred to and from the drive read/write circuits. Depending on its operating mode, the I/O circuitry alternates either bits, bytes, or words between the two read/write channels. Data shifts out of registers one bit at a time to the two write channels. Deserializing read data is the reverse process, changing serial data from two read channels into parallel data for the interface.

The I/O MPU is an 8-bit microcontroller that interprets and executes all command/response bus controls along with their parameters. The I/O MPU also becomes involved when master status is received, slave status is required, or an error occurs. The I/O MPU monitors changes in drive status through discrete inputs and MPU bus inputs from the Controller-Device Interface Chip (CDIC). The I/O MPU can perform some limited diagnostics on the read/write circuits in the IPIP Array.

The CDIC contains the cylinder address register, the head address register, the fault latches and fault register, the head increment circuitry, and other control circuits. The CDIC acts as the interface for any information passed between the I/O MPU and the Control MPU.

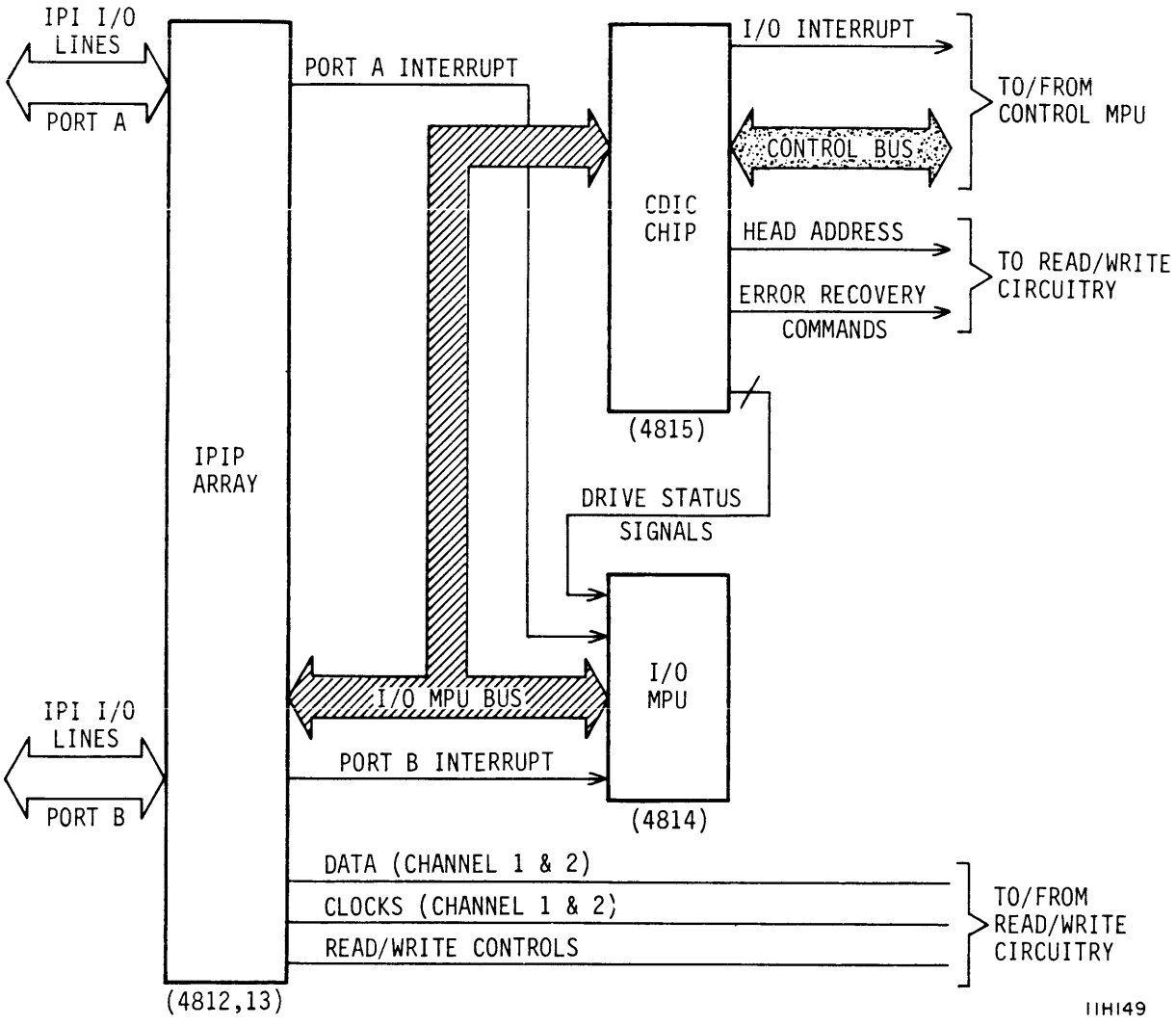


Figure 3C-3. IPI I/O Block Diagram (Parallel Read/Write)

INTERFACE SIGNAL PROCESSING

Signal processing on the IPI interface follows a state-driven protocol. Specification 64731600 provides the details of this protocol. This topic provides an overview of the following aspects of signal processing:

- States
- Sequences
- Bus Controls
- Status

States

States are interface conditions defined by the logic levels of the following control lines:

- Select Out
- Slave In
- Master Out
- Sync In
- Sync Out

For each state transition on the interface, only one control line changes. Figure 3C-4 is a state diagram showing possible state transitions. Table 3C-2 lists the states and provides a brief explanation of their functions.

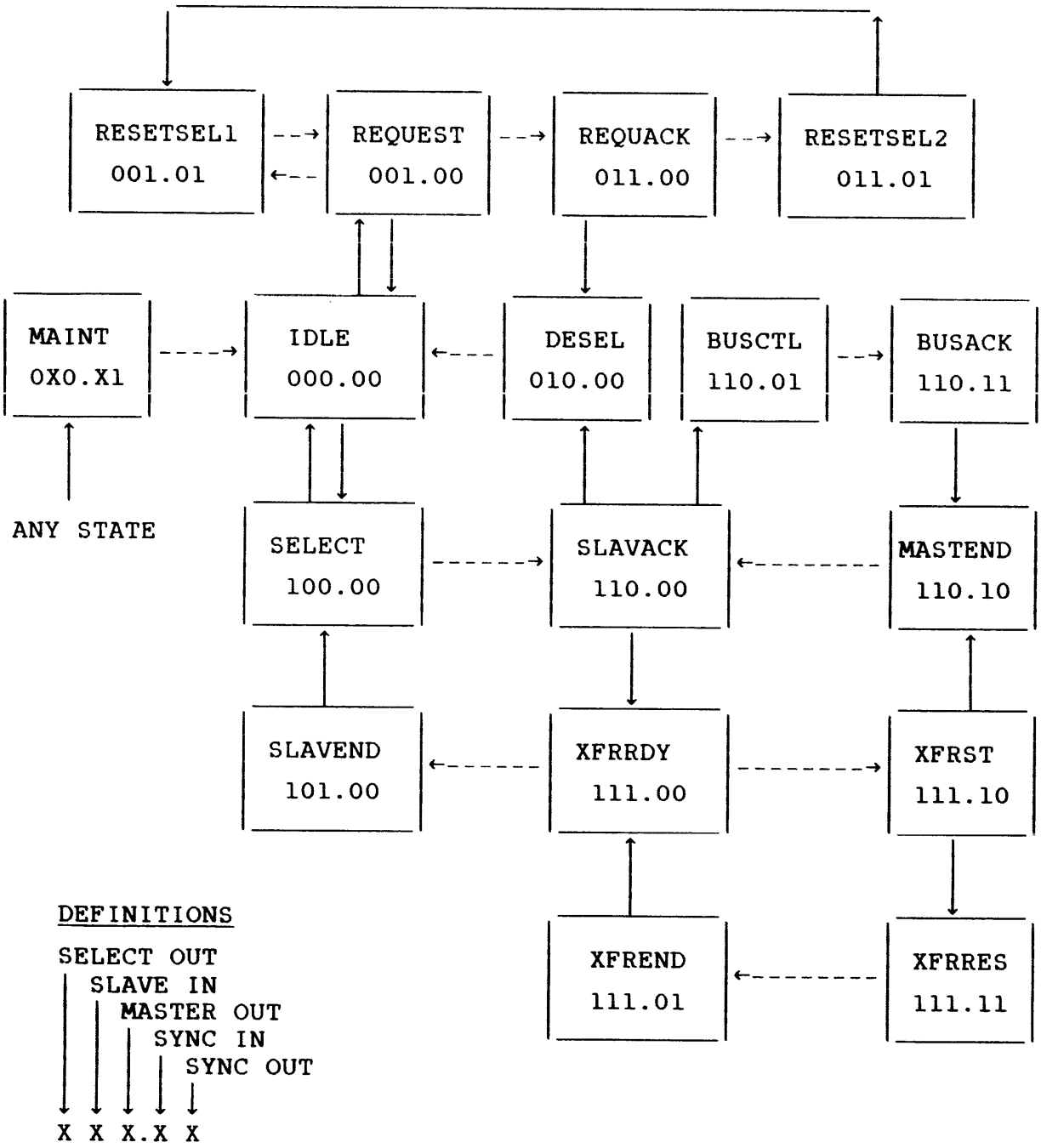


Figure 3C-4. Bus State Diagram

TABLE 3C-2. INTERFACE STATE FUNCTIONS

State Abbreviation	State Name	C/D*	Comments
BUSACK	Bus Acknowledge	D	Acknowledges that the bus control octet has been accepted by the drive.
BUSCTL	Bus Control	C	Conditions the transceivers for the following information transfer.
DESEL	Deselection	C	Starts the deselection of the drive by the controller.
IDLE	Idle	-	The interface is in the IDLE state when all the control signals are inactive. Abnormal entries to this state occur whenever the controller and drive(s) recognize an undefined state or state transition. The buses are released prior to entering the IDLE state, except during the request interrupts and master reset sequences.
MAINT	Maintenance	C	Starts maintenance mode on all drives. The controller starts the maintenance mode by executing a master reset sequence.

* = Indicates whether entry into this state is controlled by the Controller or Drive.

Table Continued on Next Page

TABLE 3C-2. INTERFACE STATE FUNCTIONS (Contd)

State Abbreviation	State Name	C/D	Comments
MASTEND	Master End	C	Either acknowledges that the bus acknowledge octet has been accepted, or it starts termination of an information transfer by the controller.
REQUACK	Request Acknowledge	D	The drive sets the requested response on Bus B and raises Slave In to enter this state.
REQUEST	Request	C	Causes the drive to respond with the address octet, the drive interrupts octet, the transfer settings octet, or to start selective reset.
RESETSEL1	Selective Reset 1	C	Starts a reset of the drive identified by the selective reset control octet on Bus A. Also ends maintenance mode.
RESETSEL2	Selective Reset 2	C	The drive releases or drops all interface lines upon recognition of this state, and causes an entry to RESETSEL1.
SELECT	Selection	C	This state starts the selection sequence. In the SELECT state it is necessary to know the previous state in order to respond correctly.

Table Continued on Next Page

TABLE 3C-2. INTERFACE STATE FUNCTIONS (Contd)

State Abbreviation	State Name	C/D	Comments
SELECT (Contd)			• When entered from IDLE, it is a true selection and the drive responds with select status on Bus B. • When entered from SLAVEND, SELECT is an intermediate state following an information transfer between the controller and the selected drive.
SLAVACK	Slave Acknowledge	D	Acknowledges selection, the end of a bus control sequence, or the end of an information transfer. In the SLAVACK state, it is necessary to know the previous state because Bus B contents are different depending on the state that SLAVACK was entered from.
SLAVEND	Slave End	D	Used by the drive to end an information transfer.
XFREND	Transfer End	D	Used by the drive to acknowledge the acceptance of information on transfers "out" and to complete the transferring of each double octet of an information transfer.

Table Continued on Next Page

TABLE 3C-2. INTERFACE STATE FUNCTIONS (Contd)

State Abbreviation	State Name	C/D	Comments
XFRRDY	Transfer Ready	C	Used by the controller to transfer each double octet of an information transfer.
XFRRES	Transfer Response	C	Used by the controller to acknowledge the acceptance of information on the buses for transfers "In," or to validate that the buses have stable information on transfers "out."
XFRST	Transfer Start	D	Acknowledges the start of an information transfer: • Indicates that the drive is ready to accept information for transfers "out." • For transfers "In," it validates that the buses have stable information.

Sequences

Sequences are a series of states that follow each other in a definite order to accomplish a function. Table 3C-3 lists the available sequences.

TABLE 3C-3. SEQUENCES

Name	Description
Master Reset	Allows the controller to start maintenance mode for all drives in a daisy chain.
Selective Reset	Allows the controller to reset a single drive and to end maintenance mode.
Selection	Occurs when the controller addresses a drive.
Deselection	Allows the controller to deselect the drive by dropping Select Out.
Request Interrupts	Allows the controller to interrogate all drives to determine the service (or class of service) desired.
Request Drive Interrupts	Allows the controller to interrogate a specific drive to determine the service (or class of service) desired.
Request Transfer Settings	Allows the controller to interrogate the specified drive as to its information transfer characteristics. The transfer characteristics apply to command/response transfers only.
Information Transfer	Information transfers are interchanges on the physical interface of commands, responses, and data that are part of a single bus exchange. All information transfers are preceded by a bus control sequence and end with an ending status sequence. The bus control sequence defines what type of information transfer is to follow.
Bus Control	Allows the controller to establish the bus configuration for the next information transfer. The ending status sequence starts when the transfer ends.
Ending Status	Allows the controller and drive to present the status of the previous information transfer.

Bus A Parameters (To Drive)	Bus B Parameters (From Drive)
Master Reset Octet (specific bits active)	Undefined
Selective Reset Control (reset type, drive address)	Undefined
Selection Octet (priority, drive address)	Selection Status Octet (drive address response)
Undefined	Undefined
Request Interrupts Octet (type of interrupt requested)	Bit-Significant Address Octet (drive address response)
Request Drive Int. Octet (specific bits active, drive address)	Drive Interrupts Octet (various interrupt bits defined)
Request Transfer Settings Octet (specific bits active, drive address)	Transfer Settings Octet (various bits define different transfer modes)
Bus A and Bus B each transfer 8 bits of a 16-bit word	
Bus Control Octet (describes next command, response, or data transfer; see Bus Controls topic)	Undefined
Controller Status Octet (controller describes previous information transfer)	Drive Status Octet (drive describes previous information transfer)

Bus Controls

The bus controls specify the condition of the bus and the information to be transferred. The three bus controls are: Command, Response, and Data.

Command Controls

The Command Controls are eight-bit codes supplied as part of a bus control sequence. They allow commands to be transmitted to the drive. The valid Command Controls and their hexadecimal codes are listed in table 3C-4.

TABLE 3C-4. COMMAND SUMMARY

Code	Name and Definition
01	Load Drive Function -- causes the drive to perform the function specified in the function code (for example: selection, enable interrupts, power sequencing, error recovery, drive diagnostics, enable/disable master (spindle) sync, and enable/disable reporting for spindle sync).
02	Load Format Specification -- a time dependent function that transmits a Format Specification to the drive. A Format Specification is an ordered list of parameters that specify the format of the tracks and sectors on the disk.
03	Load Drive Specific Information -- transmits drive specific information to the drive (for example: sync byte value, device unique ID, and [for parallel-head drives] operating mode).
04	Load Cylinder Address -- a time dependent function that causes the drive to seek to the cylinder specified in the command.
05	Load Head Address -- causes the drive to select the head specified in the command.

Table Continued on Next Page

TABLE 3C-4. COMMAND SUMMARY (Contd)

Code	Name and Definition
06	Load RPS Target Sector Address -- causes the drive to select the physical sector specified for the target in the command.
07	Load Position -- causes the drive to seek to the specified cylinder, select the specified head, and select the specified RPS target sector.
30	Reserve -- reserves the drive to this port until released, or until a Priority Select or Reset is received. This command must be enabled by a function code within Bus Control 01, or it will be rejected.
31	Release -- releases the drive, upon deselection, from being reserved by this port. This command must be enabled by a function code within Bus Control 01, or it will be rejected.

Response Controls

The Response Controls are eight-bit codes supplied as part of a bus control sequence. They allow responses to be read from the drive. The valid Response Controls and their hexadecimal codes are listed in table 3C-5.

TABLE 3C-5. RESPONSE SUMMARY

Code	Name and Definition
41	Read Configuration -- causes the drive to transfer configuration information (for example: drive type, features, cylinder addressing, switch settings).
42	Read Format Specification -- causes the drive to transfer the current Format Specification (see code 02).
43	Read Drive Specific Information -- causes the drive to transfer drive specific information (includes status codes, FRU codes, and fault codes).
44	Read Status -- causes the drive to transfer up to eight octets of status (defined later in figure 3C-5).
46	Read Current Sector Address -- causes the drive to transfer the current sector address.
47	Read Current Position -- causes the drive to transfer the current position (cylinder address, head address, and RPS target sector address).
48	Read Extended Status -- causes the drive to transfer extended status (defined later in figure 3C-6).

Data Controls

The Data Controls provide for reading and writing on the disk. They specify the direction of the transfer, the fields involved, the orientation of those fields, and step head control.

There are two Data Controls, field and sector. The field controls specify operations on a single field or a pair of fields. The sector controls are combined controls that specify operations on sectors having a header and 1 or 2 data fields. When using field controls, the previous field must have been operated on by a field or sector Data Control.

The Data Controls are eight-bit codes supplied as part of a bus control sequence. When Bit 4 is set in any Data Control, the head address counter advances at the end of a successful transfer. The head address counter is advanced unconditionally by the step head control.

The Data Control format results in eight groups and a special control as shown below:

- Skip/Write Data Field
- Verify Header, Write Data
- Write Header, Write Data
- Write Header, Write Data at Target
- Skip/Read Data Field
- Skip Header, Read Data
- Read Header, Read Data
- Read Header, Read Data at Target
- Step Head

Table 3C-6 is a summary of these Data Controls. When two hexadecimal codes are listed in the table, the first includes no head step; the second includes head step.

TABLE 3C-6. DATA CONTROL SUMMARY

Code	F/S*	Name
80	F	Skip Data Field
81,91	F	Write Data Field
82,92	F	Skip Data Field and Write Data Field
83,93	F	Write Two Data Fields
84,94	S	Verify Header
* = Indicates whether the data control operates on fields (F) or sectors (S).		

Table Continued on Next Page

TABLE 3C-6. DATA CONTROL SUMMARY (Contd)

Code	F/S	Name
85,95	S	Verify Header and Write Data Field 1
86,96	S	Verify Header and Write Data Field 2
87,97	S	Verify Header and Write Data Fields 1 and 2
88,98	S	Write Header
89,99	S	Write Header and Data Field 1
8A,9A	S	Write Header and Data Field 2
8B,9B	S	Write Header and Data Fields 1 and 2
8C,9C	S	Write Header at Target
8D,9D	S	Write Header and Data Field 1 at Target
8E,9E	S	Write Header and Data Field 2 at Target
8F,9F	S	Write Header and Data Fields 1 and 2 at Target
90	-	Step Head
C0	F	Skip Two Data Fields
C1,D1	F	Read Data Field
C2,D2	F	Skip Data Field and Read Data Field
C3,D3	F	Read Two Data Fields
C4,D4	S	Skip Header
C5,D5	S	Skip Header and Read Data Field 1
C6,D6	S	Skip Header and Read Data Field 2
C7,D7	S	Skip Header and Read Data Fields 1 and 2

Table Continued on Next Page

TABLE 3C-6. DATA CONTROL SUMMARY (Contd)

Code	F/S	Name
C8,D8	S	Read Header
C9,D9	S	Read Header and Data Field 1
CA,DA	S	Read Header and Data Field 2
CB,DB	S	Read Header and Data Fields 1 and 2
CC,DC	S	Read Header at Target
CD,DD	S	Read Header and Data Field 1 at Target
CE,DE	S	Read Header and Data Field 2 at Target
CF,DF	S	Read Header and Data Fields 1 and 2 at Target
D0	-	Reserved

Status

Status Response

The status bits of the status response indicate exception conditions. They are set on the occurrence of an exception event. The setting of any exception status bit activates the status pending interrupt and the Attention In signal, if enabled. Refer to figure 3C-5 for a description of all status response bits.

The drive transfers the status response to the controller upon receiving a read status bus control. Drive faults are cleared when the status response is read, if the fault no longer exists.

Extended Status Response

The drive transfers the Extended Status Response to the controller upon receiving a read extended status bus control. The extended status bits are static indications of the current flag states and drive conditions. Refer to figure 3C-6 for a description of all the extended status response bits.

OCTET NAME	OCTET	MSB 7	6	5
EXCEPTION STATUS	0	STATUS RESPONSE	UNSOLICITED EXCEPTION	BUS CONTROL EXCEPTION
UNSOLICITED EXCEPTION	1	RESET COMPLETE	ALTERNATE PORT PRIORITY SELECT	ALTERNATE PORT FORMAT CHANGED
BUS CONTROL EXCEPTIONS	2	INVALID BUS CONTROL	INVALID PARAMETER	UNSUPPORTED BUS CONTROL
DRIVE EXCEPTIONS	3	SPEED FAULT	OFF CYLINDER FAULT	HEAD SELECT FAULT
DRIVE EXCEPTIONS	4	WRITE PROTECT FAULT	RESERVED	WRITE TRANSITION FAULT
DRIVE EXCEPTIONS	5	DIAGNOSTIC STATUS AVAILABLE	DIAGNOSTIC TESTS INCOMPLETE	W/R DIAGNOSTIC TESTS DISABLED
DRIVE EXCEPTIONS	6	RESERVED	RESERVED	RESERVED
DRIVE EXCEPTIONS	7	RESERVED	RESERVED	RESERVED

Figure 3C-5. Status Response (Sheet 1 of 2)

OCTET	4	3	2	1	LSB 0
0	READ FAULT	WRITE FAULT	SEEK FAULT	SPINDLE FAULT See Note 1	EXECUTION FAULT
1	ALTERNATE PORT FORMAT COMPLETE	RESERVED	READY TO NOT READY TRANSITION	NOT READY TO READY TRANSITION	RESERVED
2	BUS CONTROL CONTEXT	DATA BUS CONTROL LATE	RESERVED	RESERVED	RESERVED
3	RESERVED	RESERVED	VOLTAGE FAULT	LOGIC TEMP FAULT	RESERVED
4	HEAD OFFSET FAULT	DATA STROBE FAULT	RESERVED	RESERVED	RESERVED
5	RESERVED	RESERVED	RESERVED	RESERVED	NO SYNC TRANSITION See Note 1
6	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
7	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Note 1: For drives with synchronized spindles, these bits are set in response to a loss of spindle sync.

Figure 3C-5. Status Response (Sheet 2)

OCTET NAME	OCTET	MSB 7	6	5
INTERFACE FLAGS	0	EXTENDED STATUS	PORT NUMBER	ALTERNATE PORT ENABLED
DATA RECOVERY FLAGS	1	OFFSET DIRECTION	OFFSET MSB	OFFSET LSB
DRIVE CONTROL FLAGS	2	WRITE PROTECTED	SPINDLE POWER ON	RESERVED
DRIVE STATUS	3	UP TO SPEED	ON CYLINDER	RESERVED
DRIVE ALARMS	4	RESERVED	RESERVED	ILLEGAL HEAD SELECT
VENDOR DEFINED	5	RESERVED	RESERVED	RESERVED
VENDOR DEFINED	6	RESERVED	RESERVED	RESERVED
VENDOR DEFINED	7	RESERVED	RESERVED	RESERVED

Figure 3C-6. Extended Status Response (Sheet 1 of 2)

OCTET	4	3	2	1	LSB 0
0	RESERVE ACTIVE	COMMAND COMPLETE INTERRUPT ENABLED	RPS INTERRUPT ENABLED	STATUS PENDING INTERRUPT ENABLED	FORMAT SPECIFI-CATION PRESENT
1	EARLY DATA STROBE	LATE DATA STROBE	RESERVED	HEADER ECC ENABLED (Optional)	DATA ECC ENABLED (Optional)
2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
3	RESERVED	RESERVED	RESERVED	HDA READY	MEDIA PRESENT
4	RESERVED	RESERVED	VOLTAGE RANGE ERROR	LOGIC OVER TEMP	RESERVED
5	RESERVED	RESERVED	RESERVED	RESERVED	SYNC ACTIVE See Note 1
6	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
7	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Note 1: For drives with synchronized spindles, this bit is set whenever the spindle is synchronized to its reference.

Figure 3C-6. Extended Status Response (Sheet 2)

UNIT SELECTION

GENERAL

The drive must be selected before it will respond to any commands from the controller. This is the case because some drive transmitters are not enabled until the drive is selected.

The dual port selection logic consists of port enable/disable controls and the means for switching the drive between two ports. For drives with standard read/write, this is done by the two Interface Protocol Circuits (IPC chips), one for each port. For drives with parallel read/write, this is done by the IPIP Array. When both ports require the use of the drive at the same time, they must arbitrate. Only one controller is allowed to gain selection of the drive at any given time. A controller attempting to select, when the other controller has already selected or reserved the drive, will receive a busy indication at the time of selection.

The functions controlling port selection are as follows:

- Accessibility - Reflects the current mode of the drive: neutral or switched.
- Select - Logically connects the drive to the controller, thus enabling it to respond to commands from the selecting controller.
- Priority Select - Allows a controller to force selection of a drive by releasing the interface to the controller currently having the drive selected or reserved.
- Reserve - Reserves the drive so it can be reselected at any time by the reserving controller. This prevents it from being selected by the other controller, unless a priority select is issued.
- Priority Reserve - Unconditionally reserves the drive to this controller. A priority select from the other controller overrides a priority reserve.
- Release - Releases drive from a reserved condition.
- Enable/Disable - Allows disabling either port during maintenance.

The following discussions describe each of these functions.

DRIVE ACCESSIBILITY

The drive can appear in one of two accessibility modes: neutral or switched. While in the neutral mode, the drive can be accessed through either enabled port. In the switched mode the drive can be accessed only through the switched port, unless a priority select is used.

The drive can become switched to a port under the following conditions:

- Selection of the port. If the Reserve or Priority Reserve function is issued after selection, the drive will remain switched to the port after deselection.
- A Priority Select is issued with a Selection sequence.

The drive remains switched to a port until one of the following conditions occur:

- The port is deselected and is not reserved.
- The port is deselected and has executed a Release function.
- An appropriate reset is executed on the port.
- The alternate port issues a Priority Select.
- The drive power is turned off and on.

SELECT

Unit selection starts when the controller initiates a selection sequence with a Selection byte on Bus A. Each drive in the string compares the drive address from the Selection byte to its own address stored in its Configuration register. If the address compares, there was no parity error on the Bus A, and the drive is not busy, the drive responds by putting its bit-significant address on Bus B and raising Slave In. The drive is now ready to accept further commands from the controller.

The drive's logical address is determined by switch settings on the operator panel (if installed) or by switch settings on the control board. This address can be any number from 0 to 7. The drive's logical address is loaded into the configuration register during the power on initialization.

The port that is selected will set the Force Selection Busy bit in the alternate port. This will cause a busy indication if selection is attempted on the alternate port.

When the drive is busy, Slave In is raised but no bit-significant address is put on Bus B. If a parity error was detected on Bus A, no drive response is made to the controller.

When two controllers attempt selection at the same time, the ports must arbitrate to determine which port will gain selection and which port will present a busy indication.

PRIORITY SELECT

If one controller has a drive selected and reserved the other controller can force selection by issuing a Priority Select command. This command forces deselection from the controller presently using the drive and selects the drive for the controller issuing the Priority Select command.

RESERVE

When a controller gains selection and issues a Reserve command, the other controller will receive a busy indication when selection is attempted. This continues until the reserving controller issues a Release command, an appropriate reset is received from either controller, or a Priority Select is received from the other controller. This allows the reserving controller to deselect, while a busy condition is maintained on the alternate port.

PRIORITY RESERVE

When a controller gains selection and issues a Priority Reserve command, a Priority Select from the other controller breaks the reservation.

RELEASE

The release function causes the drive to be released from this port and to enter the neutral mode. This function takes effect when the controller deselects from the port. Both ports are initially released at power on and following a reset.

PORT ENABLE/DISABLE

Ports may be individually enabled or disabled by command and by manual switches located on the I/O board. When a port is disabled, it is made not operational at the physical interface. Both ports are initially enabled when power is applied, if not disabled by the manual switches.

If a controller gains selection and issues a Disable Alternate Port command, the alternate port is made not operational at the physical interface until the selected port receives an Enable Alternate Port command. If a port is disabled by command, changing the manual switch from Disable to Enable will cause the port to be enabled. However, the disabling of a port by the manual switch cannot be overridden by command.

The disabling of a port, either by command or switch, will cause all reservations to be cleared and will cause any status associated with the disabled port to be reset.

ATTENTION

When the drive is in the neutral mode, Attention is sent to both ports. When the drive is switched, the Attention is sent to the switched port. The generation of Attention from the interrupts may be enabled/disabled on a port basis by command. All Attention generation is enabled by a reset.

SECTION 4

SERVO SURFACE DECODING

SERVO SURFACE DECODING 4

INTRODUCTION

The servo surface is a prerecorded disk surface in the module that provides three basic types of information to the drive electronics. Information from the servo surface is read by the servo head. The servo head is mounted on the same positioner as the data heads; thus, movements of the data heads across the data surface correspond exactly to movements of the servo head across the servo surface.

The three types of information available from the servo surface are as follows:

- Radial movement of the heads, indicated by the Position signal
- Rotational position of the disks, indicated by the Index signal
- Exact rotational speed of the disks, indicated by the clock signal from the servo PLO.

The significance of each type of information for drive operation and the development of the basic feedback signals from the servo signal are presented under the following topics:

- Dibit Recording Scheme
- Servo Surface Format
- Dibit Decoder Circuit Operation

DIBIT RECORDING SCHEME

Servo information consists of dibit coding on a series of concentric tracks located on the servo surface. The pattern of flux reversals alternates from track to track.

Unless the servo head is positioned directly over one dibit track, the signal it detects is a composite of signals from the two tracks nearest the head. Figure 4-1 shows servo information recorded on two adjacent tracks and the signal detected when the servo head is halfway between the tracks.

Figure 4-1 shows two normal servo bytes. Each normal servo byte contains two dibits -- an odd dibit followed by an even dibit. Odd dibits have a positive pulse followed by a negative pulse, and even dibits have a negative pulse followed by a positive pulse. The odd and even dibits are staggered from track to track so that they make separate contributions to the composite servo signal.

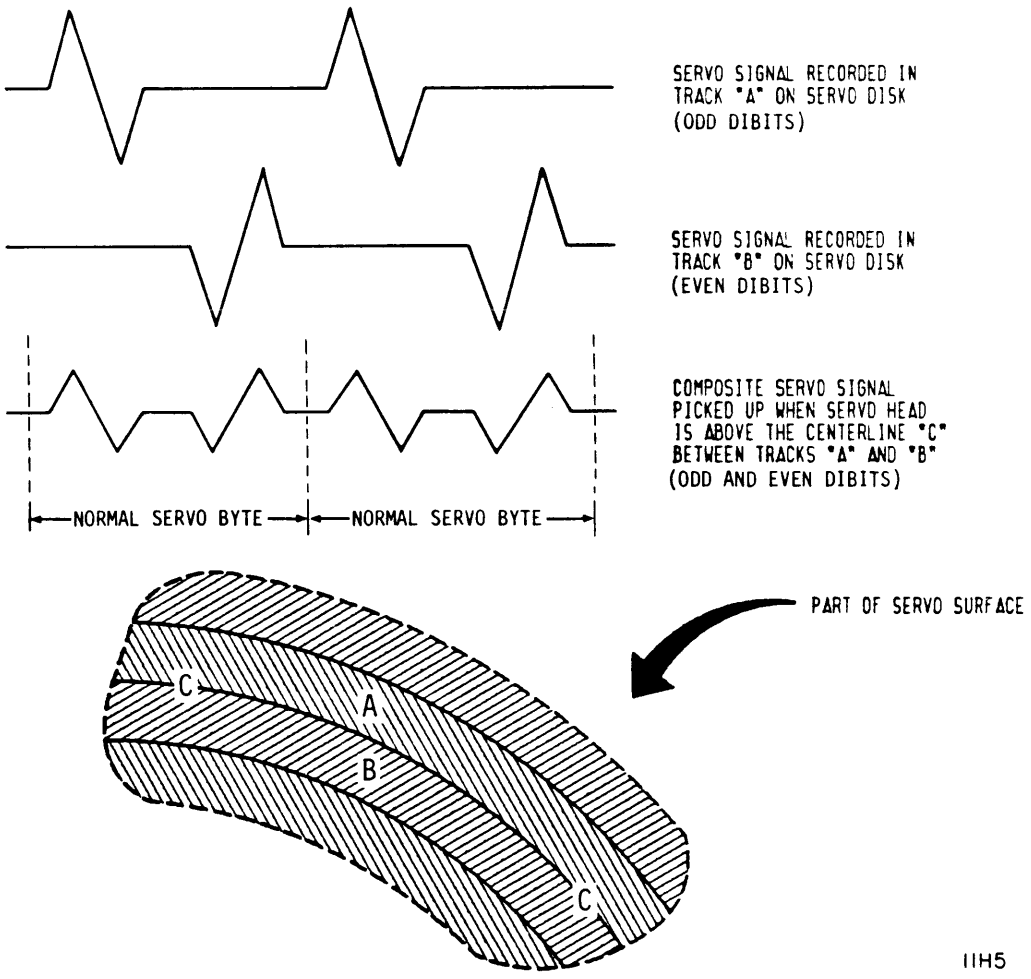


Figure 4-1. Dibit Pattern

The relative amplitude of the two patterns within each servo byte indicates the precise position of the servo head and, therefore, the data heads. When the data heads are located at the centerline of a data track, the servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent dibit signals. The amplitude of each dibit component within a servo byte is proportional to the read coil overlap of the recorded servo tracks. With the head centered, the amplitudes of the two types of dibits are equal. As the head moves away from its centered position toward one servo track, the amplitude of one dibit component increases while the other decreases. The dibit demodulator converts this variation into the position signal used by the seek circuitry (see Position Circuits).

Figure 4-2 shows the detected servo signal for three different servo head positions. In one of the three cases, the servo head is located on the centerline between two servo tracks, and the dibit components have equal amplitudes. In the other two cases, the servo head is located on either side of the centerline, and the dibit components have different amplitudes.

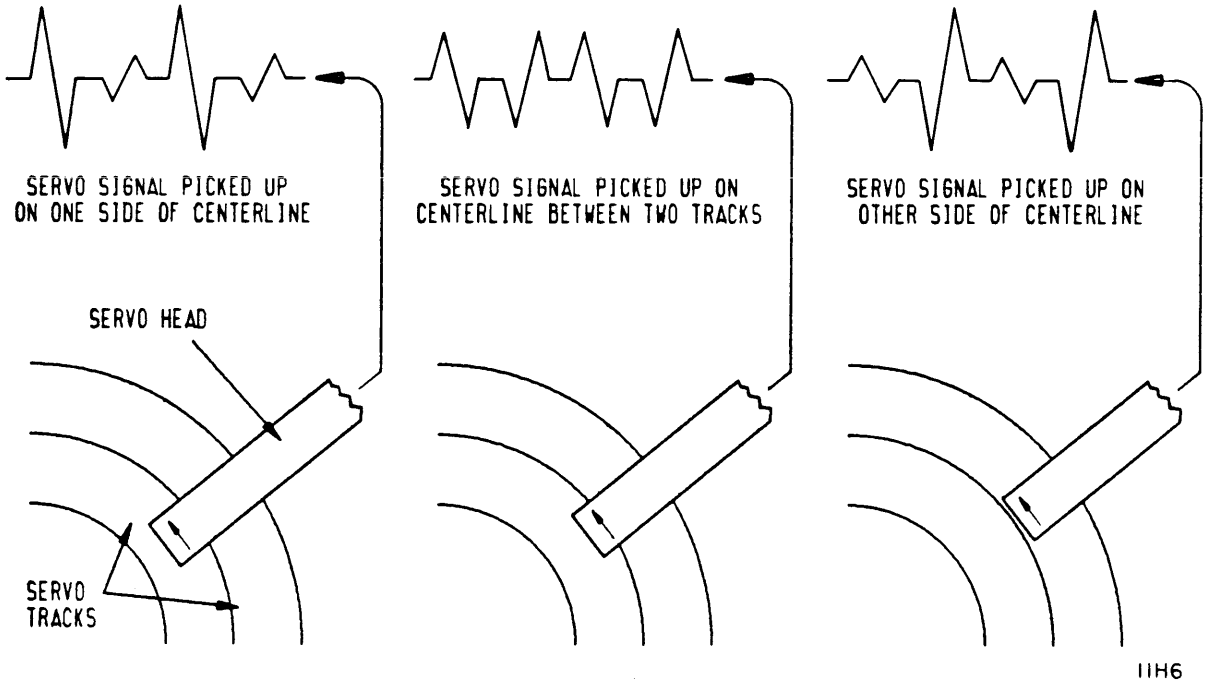


Figure 4-2. Dibit Signal Variations

SERVO SURFACE FORMAT

The servo surface, through its encoding format, establishes the format of the disk data surfaces. The landing zone, which has no servo encoding, is located at the inner radius of the disks. Each of the following zones is encoded differently:

- Outer Guard Band -- a region on the outer portion of the disk that cannot be used for recording of data. The outer guard band has 157 tracks on 736 MB, 1120 MB, 1153 MB, and 1230 MB drives (132 tracks on 850 MB drives).

- Buffer Zone -- 2 tracks located between the outer guard band and the data zone

- Data Zone -- a region used for recording of data. The data zone has 1635 tracks on 736 MB, 1120 MB, 1153 MB, and 1230 MB drives (1381 tracks on 850 MB drives).

- Inner Guard Band -- a region on the inner portion of the disk that cannot be used for recording of data. The inner guard band has 13 tracks on 736 MB, 1120 MB, 1153 MB, and 1230 MB drives (11 tracks on 850 MB drives).

Servo encoding extends to include the guard band areas even though they are not used for data storage. In addition, all four zones contain an encoded reference line which establishes the logical beginning of each track. When this reference is decoded, the drive sends the Index signal to the controller via the interface.

Figure 4-3 shows the positioning of heads on the module disk surfaces. The exploded portion of the drawing explains how formatting information is encoded on the disk. This format information is encoded in a pattern of nine consecutive servo bytes containing additional negative and positive pulses. The arrangement of these additional pulses makes it possible to distinguish between the patterns assigned for index, outer guard band, and inner guard band.

The index pattern marks the logical beginning of servo tracks for both the data zone and the guard bands. It is the only unique format pattern found on those servo tracks in the data zone. The guard bands have, in addition to the index pattern, other coded patterns spaced at regular intervals around each servo track. When the guard band patterns are decoded, they indicate to the servo system that the heads are outside the data zone.

A description of the circuitry that performs this decoding appears later in this section under Index and Guard Band Decoding.

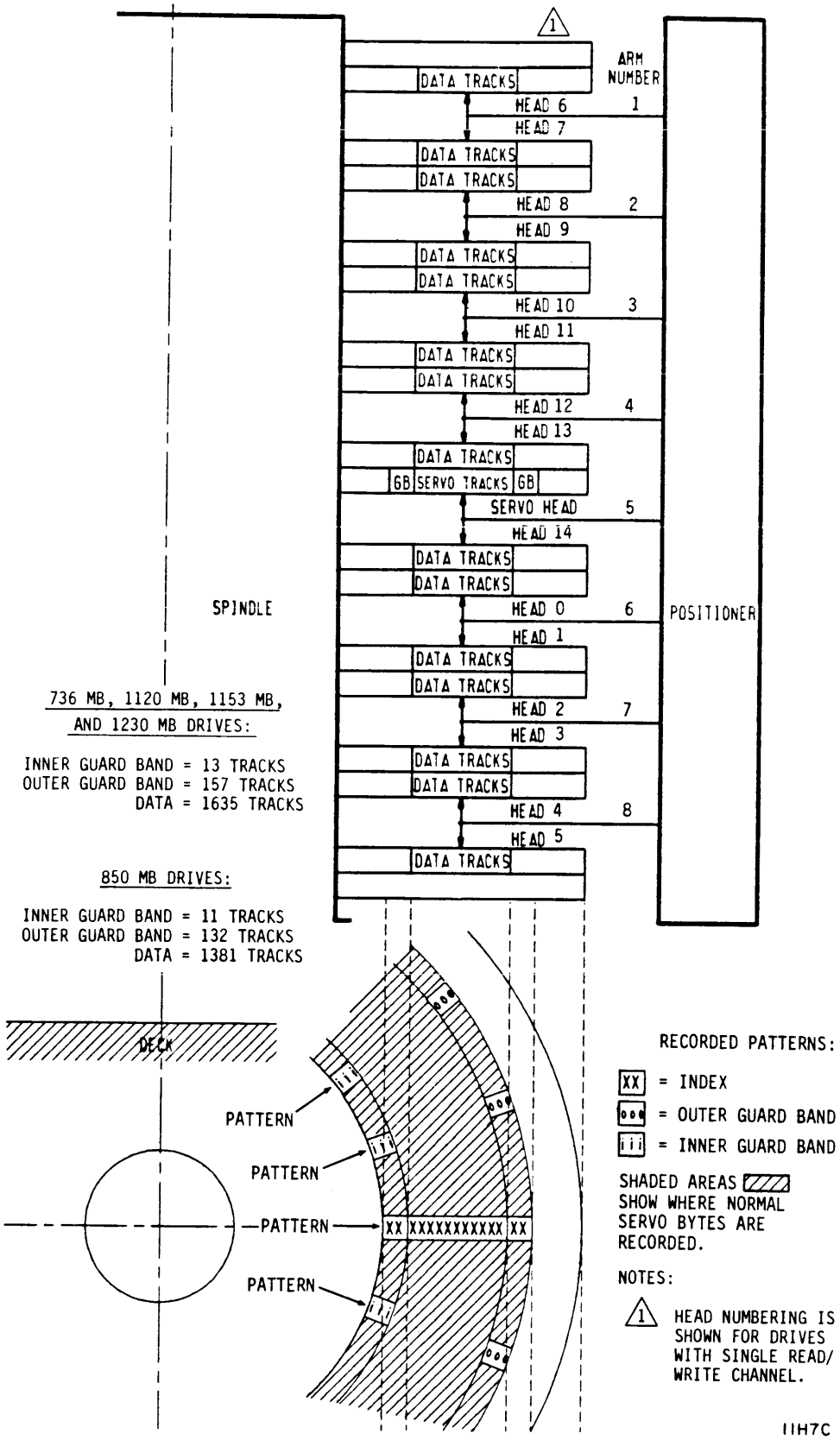


Figure 4-3. Servo Disk Format

DIBIT DECODER CIRCUIT OPERATION

Operation of the dibit decoder circuitry is discussed first in terms of its relation to other systems within the drive. This is followed by explanations of the individual functions performed by the decoder.

SYSTEM OVERVIEW

Decoding the information present in the servo signal is essential for other functional areas of drive operation. Figure 4-4 is a functional block diagram showing signal flow between the dibit decoder and these other functional areas.

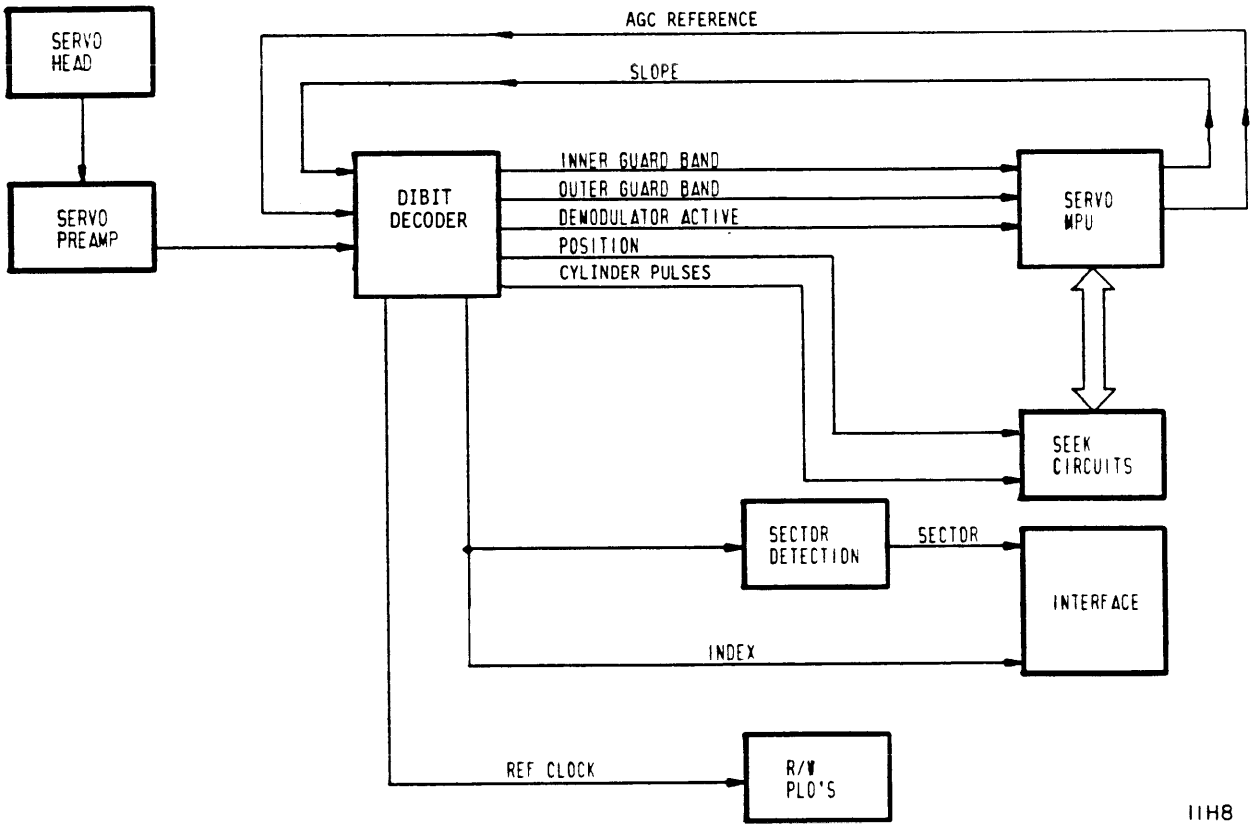


Figure 4-4. Dibit Decoder System Diagram

Inputs to the decoder come from the servo preamplifier and the Servo MPU. The servo preamplifier amplifies the signal detected by the servo head. The Servo MPU supplies information on slope and position gain on its data bus. The Slope signal, supplied by the Servo MPU, sets up the polarity of the decoded Position signal so that it can be used by the seek circuits. The Servo MPU monitors the Position signal amplitude during seeks and provides an AGC reference to the decoder to modify that amplitude.

As the servo system moves the heads during a seek, the Position signal changes polarity at each cylinder crossing. A circuit in the dibit decoder develops a cylinder pulse line whenever this happens. Cylinder pulses enable the servo system to measure the progress of a seek.

The Servo MPU monitors three output signals from the decoder. During normal seek operations, the servo head remains over the data zone. Thus, when the inner or outer guard band pulses go active, the Servo MPU reacts by altering the seek protocol. Improper decoder operation can affect seek reliability. For this reason, the Servo MPU monitors the Demodulator Active line.

Data transfers to and from the disk must be coordinated with respect to the rotational position of the disk. The Index signal is decoded and is supplied to the Sector Detection circuitry which, in turn, generates a given number of sector pulses per disk rotation. The Sector and Index signals are supplied to the I/O board.

These signals are used differently with each interface type. With the SMD interface, the controller coordinates data transfers based upon the index and sector pulses transmitted to it via the interface. With the SCSI and IPI interfaces, the I/O circuitry performs its own function of rotational position sensing using Index as a reference.

The R/W PLO circuitry uses a reference clock from the decoder to generate the Servo Clock signal. The Servo Clock operates at an exact multiple of the reference clock frequency, and thus both clock signals track the rotational velocity of the disk.

Write data is transferred serially from the I/O board to the disk in sync with the Servo Clock. This compensation in the rate of data transfers to the disk makes the written data pattern independent of disk speed. With the SMD interface, Servo Clock is sent to the controller. With the SCSI and IPI interfaces, the I/O board receives parallel write data and uses Servo Clock when serializing the data.

The remaining topics within this discussion cover the operation of circuits within the dibit decoder. Figure 4-5 is a block diagram showing these circuits and their interconnections.

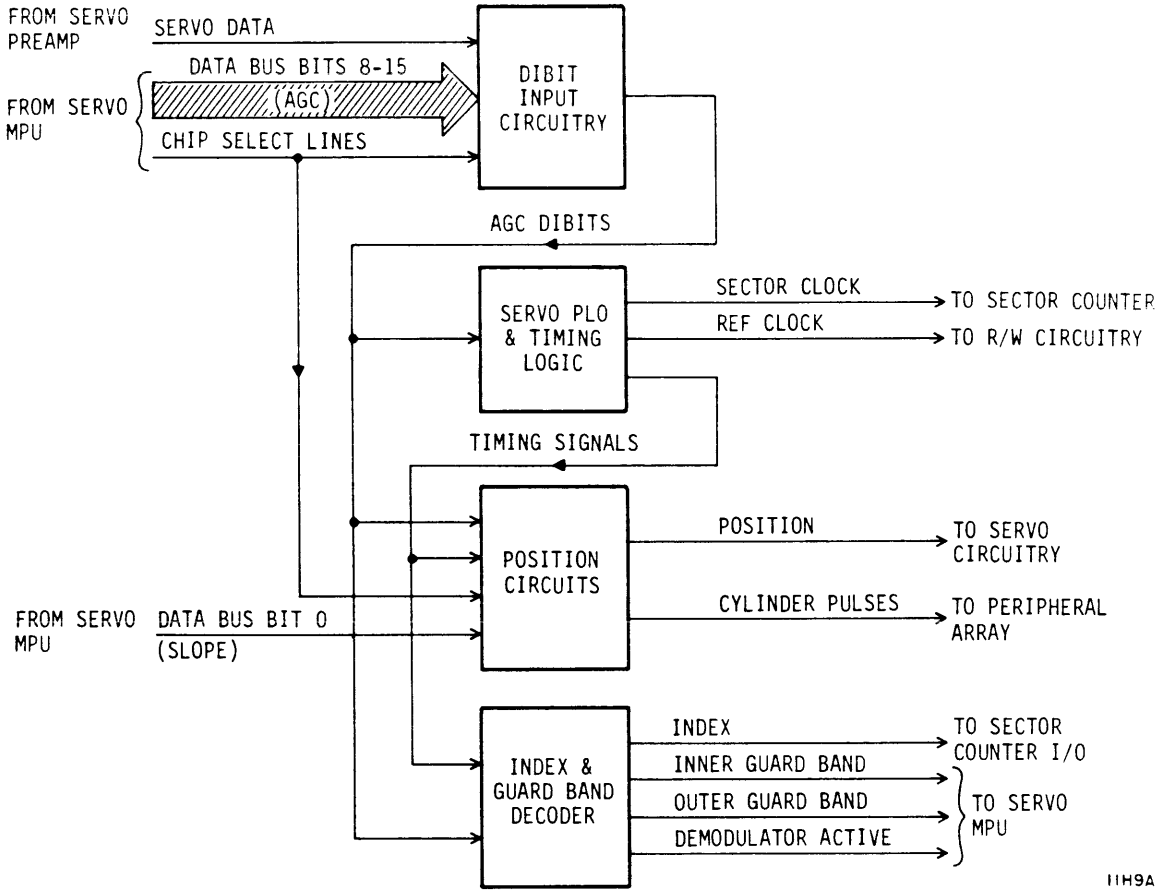


Figure 4-5. Dibit Decoder Block Diagram

DIBIT INPUT CIRCUITRY

The dibit input circuitry filters and amplifies the Servo Data signal from the servo preamp. As shown in figure 4-6, much of this circuitry is located inside the Dibit Demodulator Array. This circuitry produces the AGC Dibits signal (routed inside the array). The AGC Dibits signal is a basic input to all other circuits inside the array.

The AGC amplifier, located inside the array, operates under the control of two feedback loops. As described in the following paragraphs, these loops provide automatic gain control (AGC) and offset reduction.

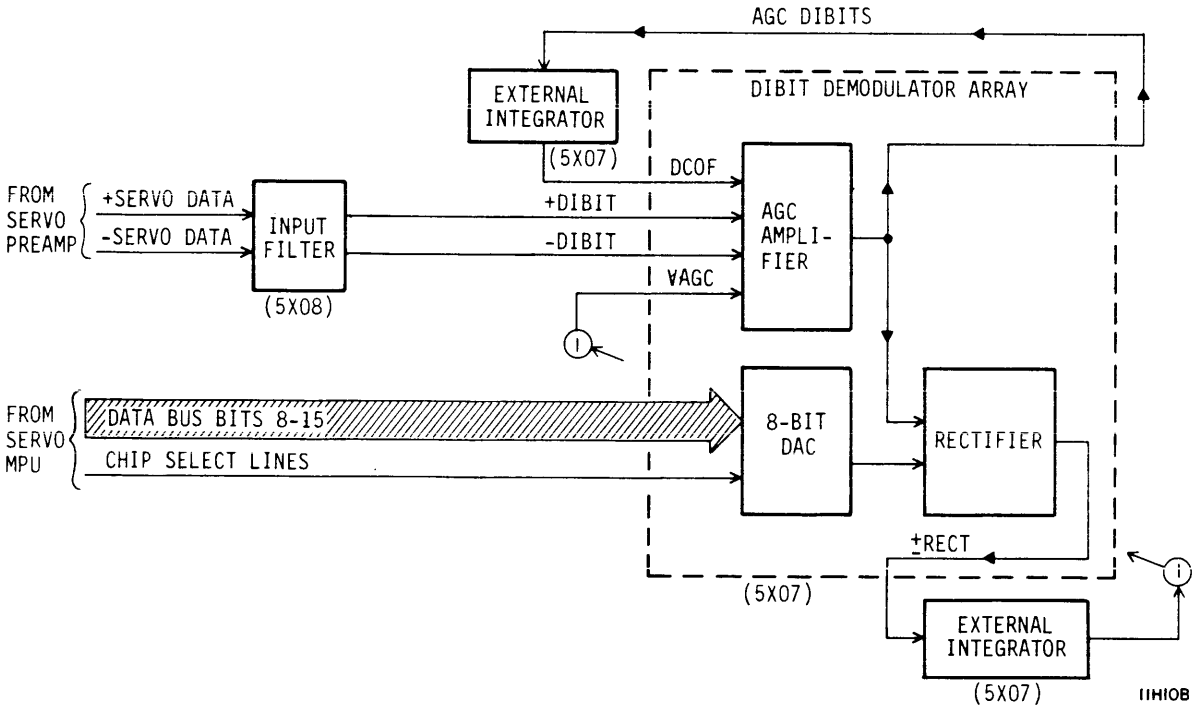


Figure 4-6. Dibit Input Circuitry

For the AGC loop, a circuit in the array rectifies the output of the AGC amplifier and compares the resulting signal with an external reference from the Servo MPU. The Servo MPU monitors the Position signal amplitude during seeks. The Servo MPU can change the gain of the dibit decoder by placing a reference byte on the data bus and activating lines that select the Dibit Demodulator Array for a bus transfer. A digital-to-analog converter (DAC) inside the array changes that reference byte into an analog control voltage. An external integrator takes the rectified signal (RECT) and develops an input signal (VAGC) to complete the AGC loop.

Another feedback loop reduces the dc offset in the AGC Dibits signal. In this loop the AGC Dibits signal is applied to an external integrator. The integrated output (DCOF) goes to the AGC amplifier to complete the loop.

SERVO PLO AND TIMING LOGIC

The Servo PLO uses a phase-locked loop to keep the timing in the dibit decoder synchronized to the timing contained in the Dibit signal. As shown in figure 4-7, a portion of the Servo PLO circuitry is located in the Dibit Demodulator Array. Circuitry external to the chip includes a charge pump and a voltage-controlled oscillator (VCO). Table 4-1 lists the frequency of the VCO signal and of signals derived from the VCO signal for each type of drive.

The phase comparator for the phase-locked loop receives two inputs -- the AGC Dibits signal, which reflects the timing present on the servo disk, and the VCO Clock signal, which completes the loop. Whenever a phase difference arises between the two inputs, the phase comparator supplies a current difference (IP and IN signals) to the charge pump. The charge pump reacts by changing the control voltage for the VCO. The changing control voltage keeps the VCO synchronized to any changes in the timing of the servo signal.

Synchronizing logic inside the array develops internal timing signals used by the position demodulator and by the index and guard band decoder. The circuit also produces external clocks derived by dividing the VCO signal. These include the reference signal supplied to the Write PLO and the Sector Clock signal (see table 4-1).

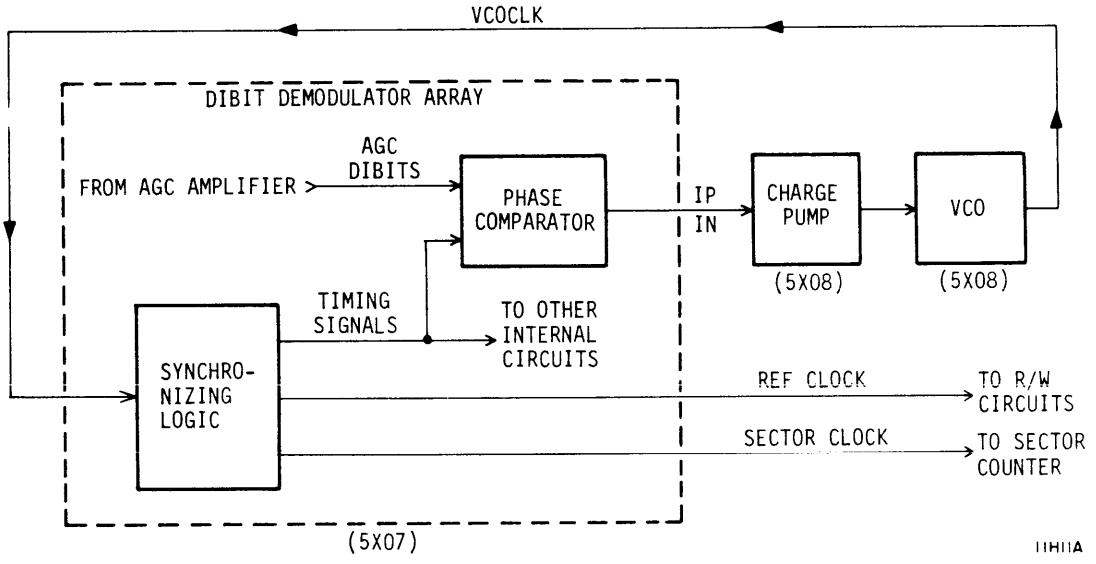


Figure 4-7. Servo PLO and Timing Circuitry

TABLE 4-1. CLOCK FREQUENCIES FOR THE SERVO PLO

Signal Name	Signal Frequencies (MHz) by Capacity			
	736 MB Drives	850 MB Drives	1120 MB Drives	1153 MB Drives 1230 MB Drives
VCO clock	9.67 (VCO)	9.86 (VCO)	10.99 (VCO)	12.10 (VCO)
Reference clock (to Write PLO)	2.41 (VCO÷4)	3.28 (VCO÷3)	3.67 (VCO÷3)	4.03 (VCO÷3)
Low frequency sector clock*	1.6 (VCO÷6)	1.6 (VCO÷6)	1.83 (VCO÷6)	2.016 (VCO÷6)

* An alternate sector clock (at the byte frequency) is generated within the Sector Counter Gate Array.

POSITION CIRCUITS

The position circuits contain a position demodulator to develop the Position signal and a cylinder pulse detector to register cylinder crossings. The servo system uses both the position and cylinder pulse information to sense where the heads are located and how fast they are moving.

Figure 4-8 shows which portions of the position circuits are located inside and outside the Dibit Demodulator Array. The position demodulator receives these input signals internal to the array:

- AGC Dibits signal -- from the AGC amplifier. This signal contains position information in dibit components contributed from two adjacent servo tracks.
- Timing signals -- from the synchronizing logic. These signals reflect the timing present in the AGC Dibits signal and make it possible for the demodulator to isolate one set of dibit components from the other.
- Slope signal -- gated into the input buffer by the Servo MPU. This allows the Servo MPU to set the polarity of the Position signal so that the signal will have the required slope as the seek circuits position the heads at their new destination.

The position demodulator takes these inputs and develops a differential output, the Position Error signal. Demodulation consists of separating the two sets of dibit components. The dibit components contributed by an even servo track drive the Position Error signal in one direction. The components contributed by an odd servo track have the opposite effect. The Slope signal determines whether the position signal goes positive or negative as the heads move over an even servo track.

The Position Error signal is filtered outside the array and returned to the array for further amplification. Finally, an external gain circuit amplifies the signal and removes any offset introduced in the decoding process. From this circuit the Position signal goes to the servo circuitry and the cylinder pulse detector.

The Position signal is attenuated before it goes to the cylinder pulse detector, located inside the array. During a seek, the Position signal alternates between positive and negative values. Each zero-crossing of that signal corresponds to a cylinder crossing. The cylinder pulse detector triggers a one-shot that generates a pulse at each zero-crossing. The cylinder pulses allow the servo circuits to monitor the distance travelled in a seek.

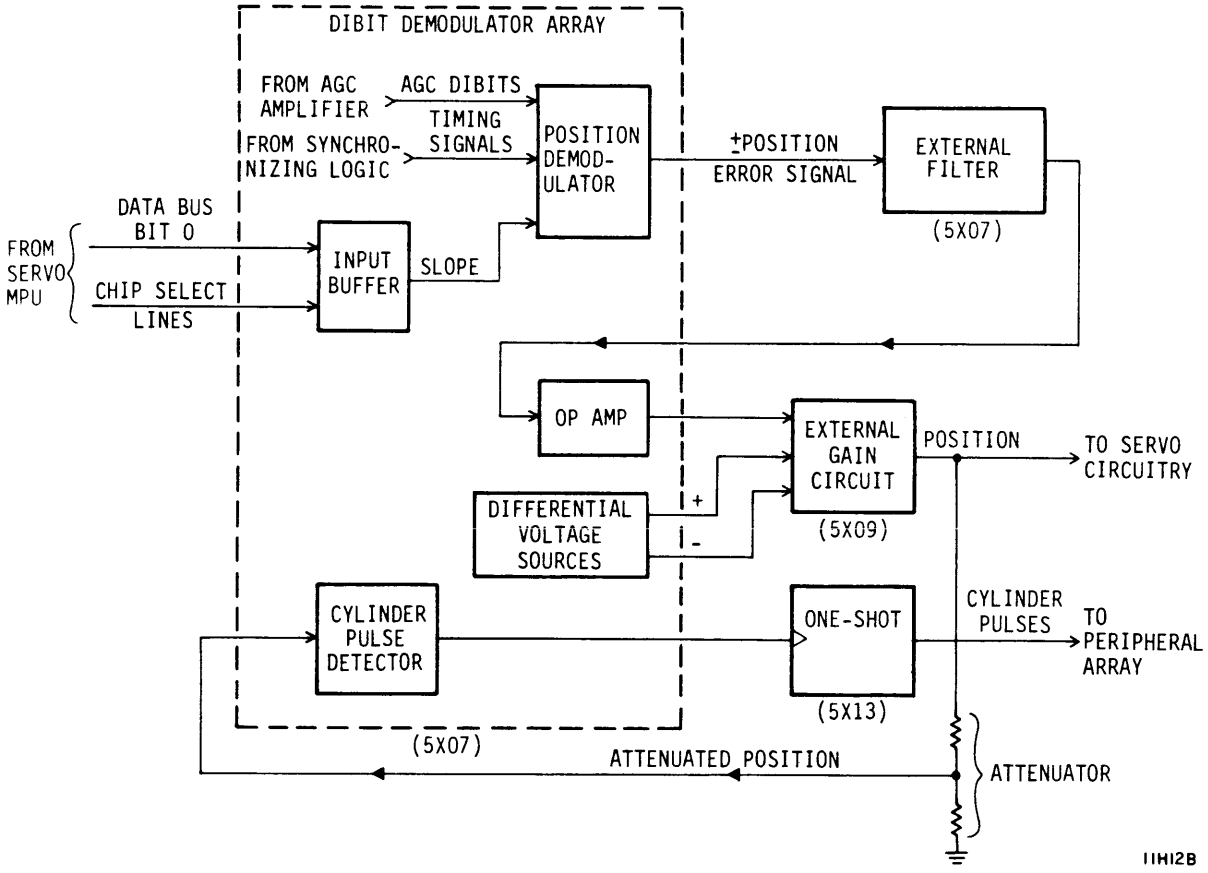


Figure 4-8. Position Circuits

INDEX AND GUARD BAND DECODING

The index and guard band decoding circuitry produces output pulses each time the servo head picks up certain patterns encoded on the servo surface. Refer to Servo Surface Format for a description of the codes and their location on the servo disk.

Figure 4-9 is a block diagram of the index and guard band decoding circuitry. This circuitry, located in the Dibit Demodulator Array, consists of a pulse detector and a pattern recognition network.

The pulse detector generates a digital pulse train each time a format pattern appears in the AGC Dibits signal. The pulse detector recognizes additional negative and positive pulses in the AGC Dibits signal as part of that format pattern. These pulses differ from the pulses of normal servo bytes in their timing and amplitude. Timing signals in the array make it

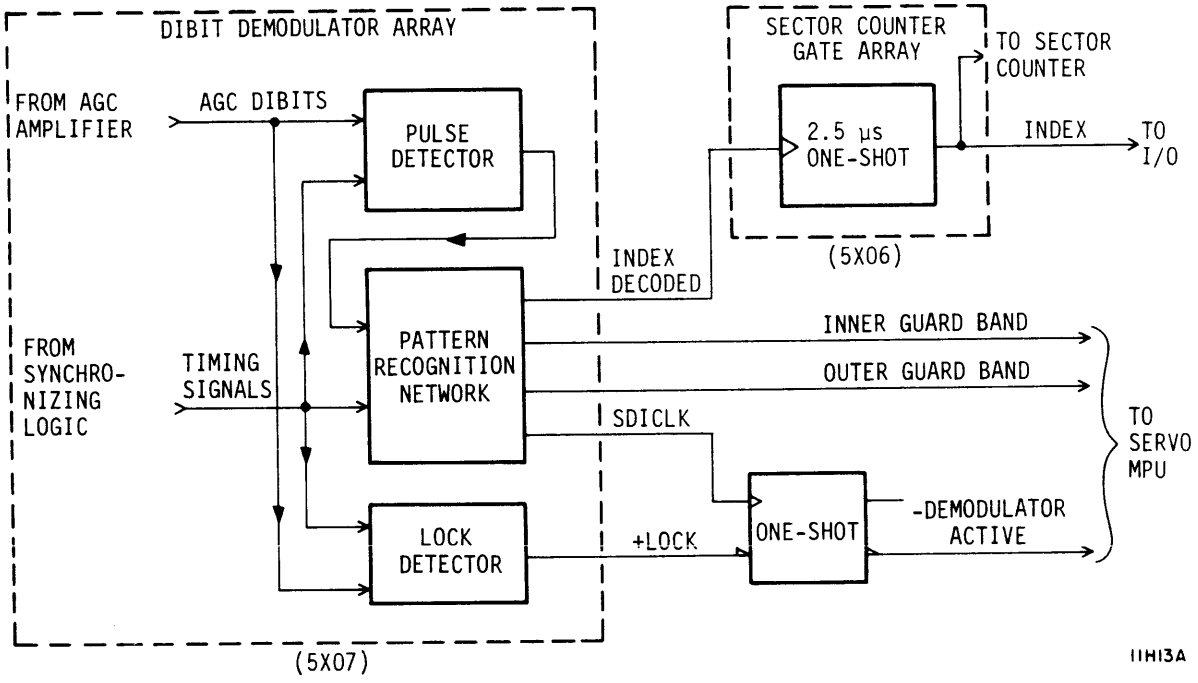


Figure 4-9. Index and Guard Band Decoder

possible to distinguish between normal pulses and format pulses. Unique patterns are defined for index, inner guard band, and outer guard band.

Digital pulses from the pulse detector pass through a pattern recognition network. As patterns shift through the network, it creates an output pulse any time a valid pattern appears. The Inner and Outer Guard Band pulses are supplied as interrupts to the Servo MPU. These interrupts inform the Servo MPU that the heads are not located over the data zone. Each pulse on the Index Decoded line triggers the Index one-shot, which is located in the Sector Counter Gate Array.

The Index signal is used by the Sector Counter, as described in the next topic. It is also sent to the I/O board, where it is used as follows:

- SMD interface -- The I/O board sends Index to the controller and uses it as a reset for the Current Sector Counter in the SMD-E Gate Array.

- SCSI and IPI interfaces -- The I/O board performs its own function of rotational position sensing using Index as a reference.

A related circuit develops the Demodulator Active signal for the Servo MPU. The pattern recognition network supplies pulses the SDICLK line whenever dibits are being decoded. A second circuit in the array, the lock detector, activates the Lock signal whenever the Servo PLO is in phase lock. The lock detector monitors the same internal signals as the phase comparator for the Servo PLO. The Lock signal enables a retriggerable one-shot. The SDICLK pulses keep the one-shot triggered as long as dibits are being decoded properly. If the one-shot times out, the Demodulator Active line to the Servo MPU goes inactive to indicate improper decoding.

SECTOR DETECTION

The following description of the sector detection circuit relates only to drives with the SMD interface. Although SCSI and IPI interface drives have a sector detection circuit, IPI drives do not use the Sector signal, and SCSI drives use it only as a reference clock in the I/O circuitry.

The sector detection circuit (figure 4-10) generates signals that are used by the drive to determine the angular position of the heads with respect to index. These signals are called sector pulses and a specific number of them are generated during each rotation of the disks. The sector pulses logically divide the disk into areas called sectors.

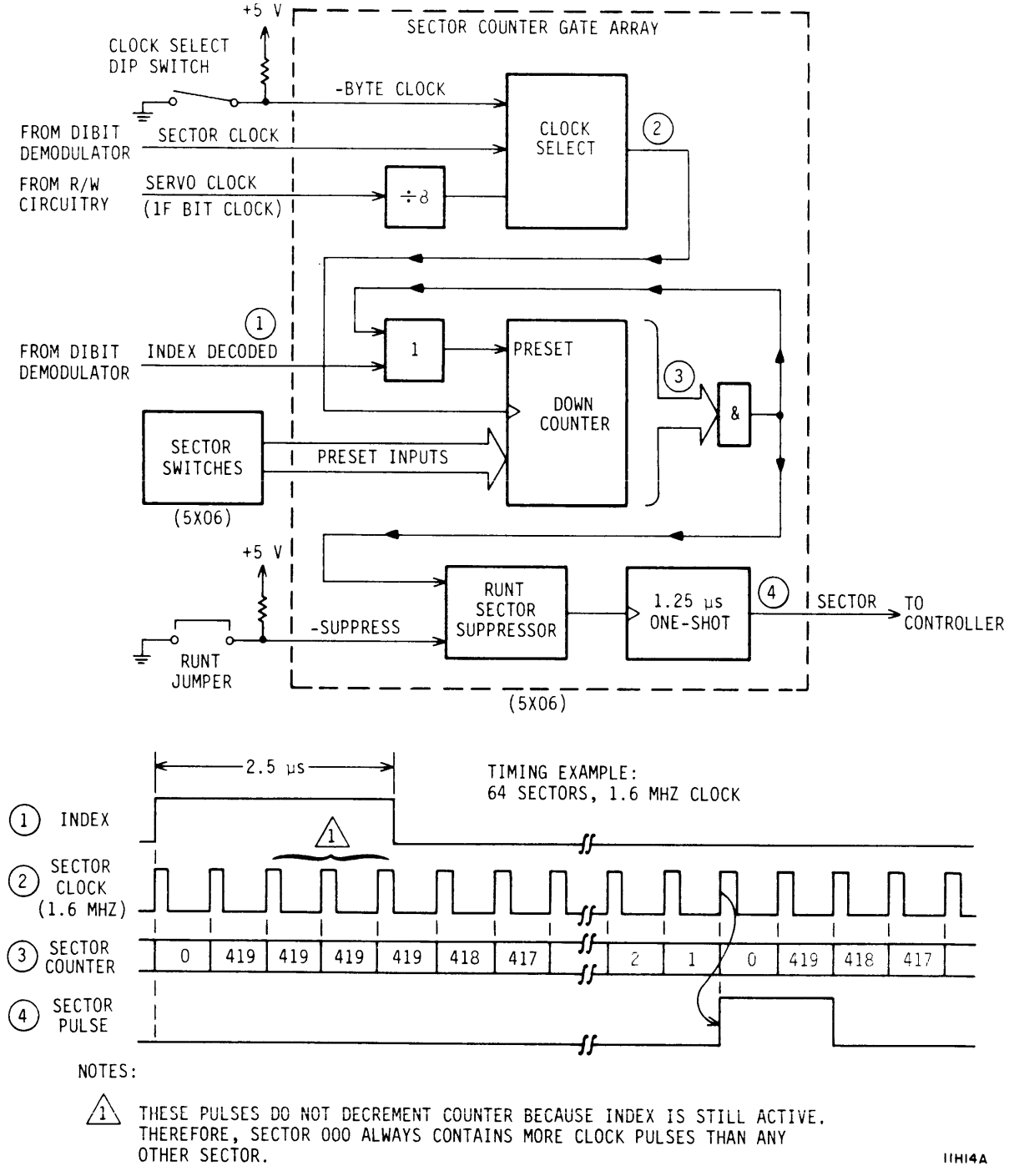


Figure 4-10. Sector Detection -- Logic and Timing

A sector pulse is generated each time the Sector counter counts down to zero. A borrow from the counter triggers a one-shot that generates the sector pulse. Depending on how a DIP switch on the control board is set, a clock select circuit picks one of the following signals as a clock for the Sector counter:

- Sector Clock signal -- derived from the Servo PLO signal in the Dibit Demodulator Array
- Byte Clock signal -- derived by dividing (by eight) the 1F Servo Clock signal from the read/write circuitry

The counter is decremented by the sector clock pulses. Table 4-2 lists the frequency and number of clock pulses per disk rotation for the various drives available.

The index pulse resets the counter allowing a fixed number of clock pulses per rotation of the disk. While Index is active, the sector counter does not count down. This lengthens the first sector and shortens the last sector by the sector length adjustment value given in table 4-2. The index pulse also resets the Current Sector counter in the SMD-E Gate Array.

TABLE 4-2. SECTOR COUNTER DATA

Characteristics	736 MB Drives	850 MB Drives	1120 MB Drives	1230 MB Drives
Bytes per track	30 240	41 088	45 792	50 400
Trigger frequency (MHz)				
Sector Clock used	1.6	1.6	1.83	2.016
Byte Clock used	1.814	2.465	2.75	3.024
Sector clock pulses per disk rotation				
Sector Clock used	26 880	27 392	30 528	33 600
Byte Clock used	30 240	41 088	45 792	50 400
Bytes per sector clock pulse				
Sector Clock used	1.125	1.5	1.5	1.5
Byte Clock used	1.0	1.0	1.0	1.0
Sector length adjustment (bytes)				
Sector Clock used	4.5	6.0	6.0	7.5
Byte Clock used	5.0	6.0	7.0	8.0

The fact that the same number of sector clock pulses occur during each rotation makes it possible to program the counter to reach the zero count (thus generating a sector pulse) any desired number of times per rotation. This is done by presetting the counter at the beginning of each sector as follows:

$$\text{Preset Value} = \frac{\text{Sector Clock Pulses/Rotation}}{\text{Number of Sectors Desired}} - 1$$

It is possible, when the number of sector clock pulses per rotation is not evenly divisible by the number of sectors, to have a runt sector just before index. A runt sector is a short interval marked by an extra sector pulse following the last usable sector. If runt sectors are a problem, you can set a jumper on the control board, causing a circuit in the Sector Counter Gate Array to suppress them. The circuit determines whether each borrow from the down counter represents a valid sector pulse or a runt sector pulse; it gates only valid sector pulses to the one-shot.

Figure 4-10 includes a timing diagram for one example of sector counter operation for 736 MB drives. The following examples include the one in the illustration plus others for 850 MB drives and 1230 MB drives:

Example 1: 64 sectors, 1.6 MHz sector clock frequency used on 736 MB drives

> The counter would have to count 420 clock pulses in each sector (26 880 divided by 64 is exactly 420), and the counter would be preset to 419 (or 420 - 1). Starting at its preset value of 419 (or 420 - 1), the counter decrements each clock time until it reaches the zero count. Reaching the zero count causes a sector pulse to be generated. The next clock pulse presets the counter back to 419, and the counter begins the next sector. With an even division there is no runt sector.

Example 2: 64 sectors, 1.814 MHz Byte clock used on 736 MB drives, runt sector pulses suppressed

> The counter would have to count 472 clock pulses in each sector (30 240 divided by 64 is 472.5, rounded down to 472). Starting at its preset value of 471 (or 472 - 1), the counter decrements each clock time until it reaches the zero count. Reaching the zero count causes a sector pulse to be generated. The next clock pulse presets the counter back to 471, and the counter begins the next sector. After the counter reaches zero for the 64th sector, the resulting sector pulse is suppressed because less than 471 clock pulses remain before the next index.

Example 3: 64 sectors, 1.6 MHz sector clock frequency used on 850 MB drives

The counter would have to count 428 clock pulses in each sector (27 392 divided by 64 is exactly 428). Starting at its preset value of 427 (or 428 - 1), the counter decrements each clock time until it reaches the zero count. Reaching the zero count causes a sector pulse to be generated. The next clock pulse presets the counter back to 427, and the counter begins the next sector. With an even division there is no runt sector.

Example 4: 64 sectors, 3.024 MHz Byte clock used on 1230 MB drives, runt sector pulses allowed

The counter would have to count 787 clock pulses in each sector (50 400 divided by 64 is 787.5, rounded down to 787). Starting at its preset value of 786 (or 787 - 1), the counter decrements each clock time until it reaches the zero count. Reaching the zero count causes a sector pulse to be generated. The next clock pulse presets the counter back to 786, and the counter begins the next sector. After the counter reaches zero for the 64th sector, the resulting (runt) sector pulse is allowed even though less than 786 clock pulses remain before the next index.

The sector length is varied by presetting the sector switches located on the control board. Refer to the installation and checkout section of the user's manual for instructions on setting the sector switches.

The Current Sector counter in the SMD-E Gate Array provides an address of the current sector to be transmitted to the controller on Bus In Bits 0 through 7 when the controller issues a Tag 4 command. The range of addresses is dependent on drive sector switch settings on the control board. The Current Sector counter is reset by each index pulse and incremented by sector pulses.

SECTION 5

SEEK FUNCTIONS

SEEK FUNCTIONS 5

INTRODUCTION

During seek operations, the drive positions the heads over the desired cylinder on the disk. The drive servo circuits, under the direction of the Servo MPU, control this function. The drive servo circuits translate Servo MPU instructions into electromechanical motion to position the read/write heads accurately. When positioned, the read/write heads can transfer information to and from the disk storage surfaces.

This section is divided into the following areas:

- System Overview -- Describes the servo functions in general terms, including the roles played by the interface and the Servo MPU.
- Actuator and Magnet -- Describes the mechanical components that move the heads in response to servo signals.
- Servo Circuit Functions -- Describes the servo loops that control head positioning.
- Types of Seeks -- Describes the sequencing of events in different types of seeks.

SYSTEM OVERVIEW

Seek operations move the heads from one location on the disks to another. The drive has five basic types of seeks:

- Load Operation -- Starts the drive motor and moves the heads from the landing zone to track 0.
- Normal Seek -- Moves the heads from one cylinder on the disk to another.
- Return to Zero (RTZ) Seek -- Clears a seek error and moves the heads from any location on the disk to track 0.
- Unload Operation -- Moves the heads back to the landing zone during a power off operation.
- Sweep Cycle -- Varies the position of the heads during idle periods by doing patterns of normal seeks.

Upon successful completion of a load, normal seek, or RTZ operation, the Servo MPU remains active and continues to maintain the actuator on track.

Each seek operation can be described in terms of four basic drive activities. These activities require communication between several functional areas of the drive, as shown in figure 5-1. These activities occur in the following sequence:

- Command -- The Control MPU processes a command from the controller that instructs the drive to move the heads to a new location on the disks.
- Control -- The Control MPU sends a seek command and destination address to the Servo MPU. The Servo MPU interprets the seek command, then translates the command into a sequence of controls sent to the servo circuitry. These controls dictate the direction of the seek, specify actuator velocity throughout the seek, and step the servo through its operating modes.

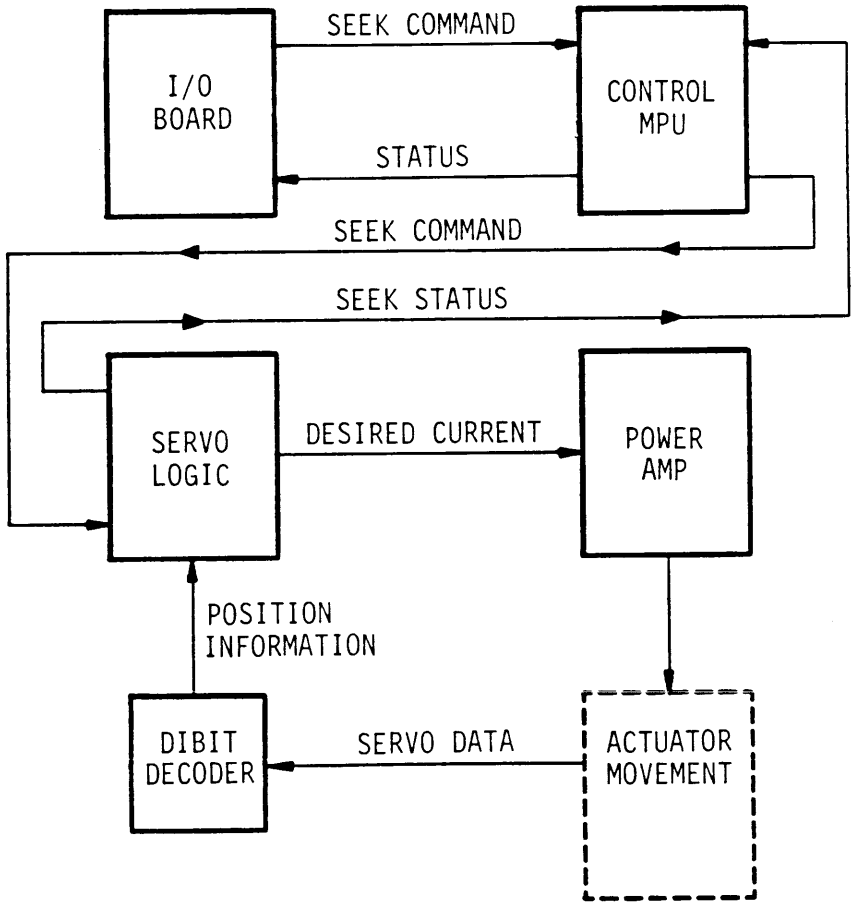


Figure 5-1. Seek Functions Block Diagram

- Execution -- The servo circuitry executes the seek in response to control information received from the Servo MPU. The Servo MPU moves the actuator and heads by controlling the current in the voice coil. Position information from the dibit decoder serves as a feedback source to the servo loop.

- Status -- The Servo MPU informs the controller via the Control MPU whether or not the seek was accomplished successfully. This indicates whether or not a reliable data transfer can be performed on the selected cylinder.

The concept of a closed loop is essential to understanding the operation of the servo system. Figure 5-2 shows a generalized servo loop that illustrates several principles governing the servo loops in the drive. Throughout the servo operation, the Servo MPU processes various inputs. If the combination of inputs to the Servo MPU indicates that the servo is unbalanced, the Servo MPU issues a correction to the electromechanical system. The response of the mechanical system is converted into an electrical signal which is an input to the Servo MPU. Mechanical movement continues until the system balance is restored, corresponding to a null in the Servo MPU inputs.

As discussed later under Servo Circuit Functions, there are actually two servo loops -- a coarse loop used for velocity control and a fine loop used for position control. Both loops resemble the generalized servo loop shown in figure 5-2. However, response measurement and Servo MPU operation differ for the two loops.

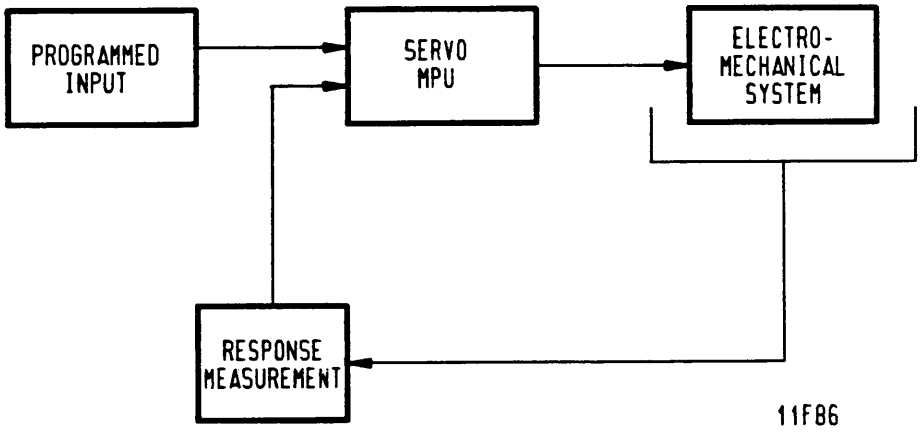


Figure 5-2. Generalized Servo Loop

ACTUATOR AND MAGNET

Data is written on and read from the disk by the heads. The drive must position the heads over a specific data track before a read or write operation can be performed. Head positioning is performed by a rotary actuator mechanism mounted near the disks inside the module. The actuator is controlled by inputs received from the servo circuits (described later in this section).

The actuator (shown in figure 5-3) has a housing mounted on the deck of the module. The actuator housing supports four permanent magnets and provides a pivot point for the rotating carriage. The carriage consists of the set of head-arms stacked on a bearing cartridge. The bearing cartridge provides a solid support for the head-arms and allows them to rotate about the pivot point. This rotation moves the heads across the disk surfaces.

A carriage latch locks the actuator when the heads are located over the landing zone. The actuator remains locked there until the next load operation. Prior to moving the heads in a load operation, the Control MPU energizes the carriage latch to unlock the actuator. The carriage latch remains energized until the heads are retracted to the landing zone. The automatic carriage-locking feature eliminates the need to manually lock the carriage when transporting the drive.

The voice coil moves in the gap between the permanent magnets as the servo signals change. The voice coil is an integral part of the head-arm supporting the servo head. To move the heads, the servo circuitry supplies a varying current to the voice coil. As shown at the bottom of figure 5-3, the current interacts with the flux lines of the permanent magnets to produce a sideways force on the coil (and carriage). The heads move either inward or outward depending on the polarity of the voice coil current. Increasing the voice coil current increases the force on the carriage. This force may either accelerate or decelerate the carriage as the servo loop controls carriage positioning.

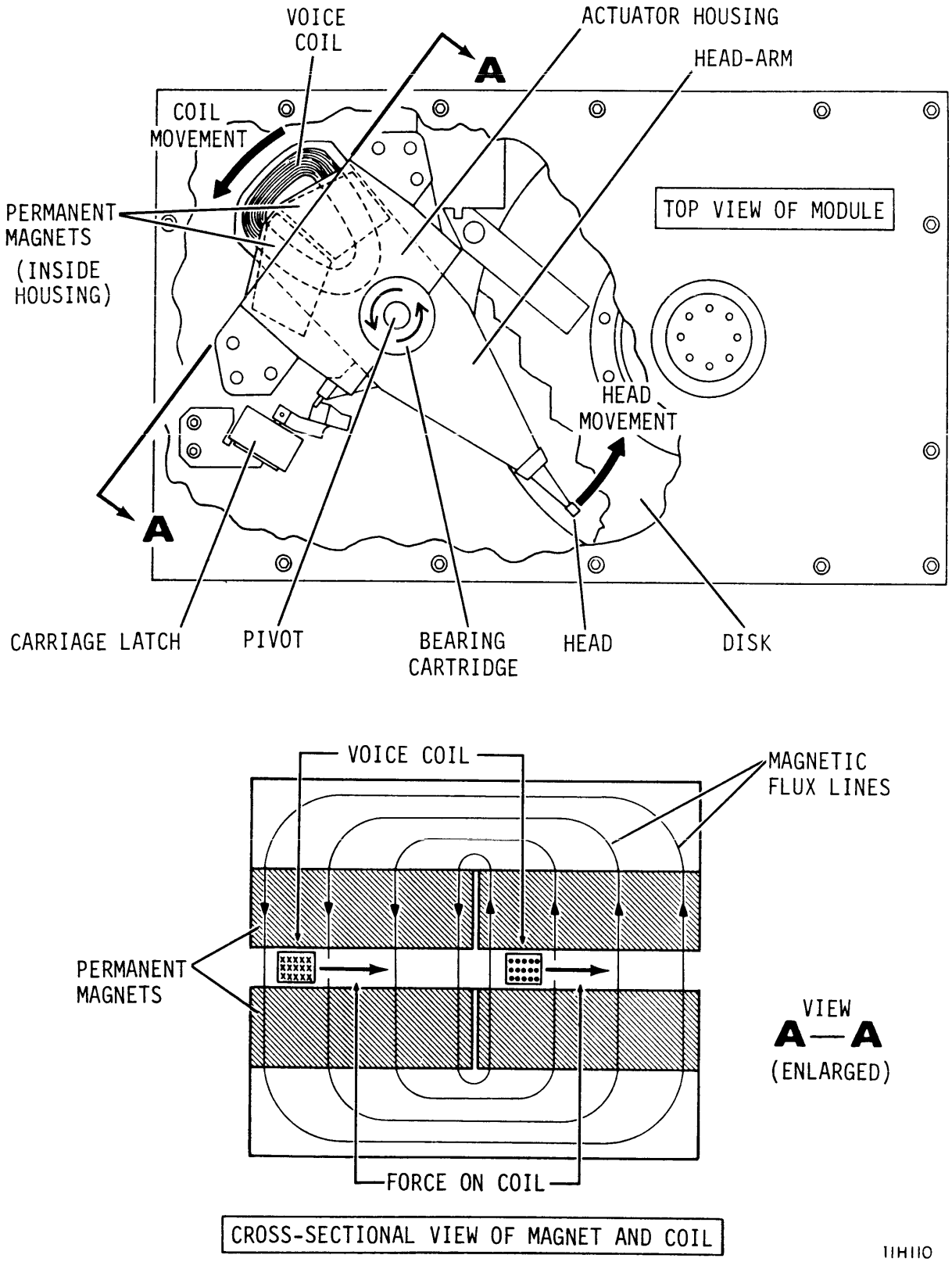


Figure 5-3. Actuator and Magnet Assembly

SERVO CIRCUIT FUNCTIONS

Where applicable, servo circuit functions are discussed in terms of the two basic loops within the servo circuitry (coarse and fine loops). With the exception of the cylinder pulse timer in the Peripheral Array, the coarse loop and the fine loop use the same circuit elements. These circuit elements are described in detail under the following topics:

- Servo MPU (including associated Peripheral Array logic)
- Desired Current Generator
- Position Sampling Circuitry
- Power Amplifier

SERVO MPU

The Servo MPU starts the seek, determines the seek direction, and periodically adjusts the speed of the actuator to ensure seek completion in the shortest possible time without overshoot. Between seeks, the Servo MPU maintains the heads on track. An external ROM contains firmware instructions for the Servo MPU and a lookup table that specifies the actuator velocity for normal seeks.

The Peripheral Array (shown in figure 5-4) provides the following signal paths for the Servo MPU:

- It can monitor certain signals developed in external circuitry.
- It can issue control signals to external circuitry.
- It can communicate with the Control MPU.

Certain inputs to the Peripheral Array from the Control MPU form maskable interrupts to the Servo MPU. When unmasked, these interrupts inform the Servo MPU of status changes that require switching to a different routine within its firmware. The Servo Data Bus connects the Servo MPU to the Peripheral Array.

The Control Bus connects the Control MPU to the Peripheral Array and to a gate array on the I/O board. This bus allows the Control MPU to communicate with the I/O circuitry in response to inputs from the Servo MPU. These communications include setting the On Cylinder and Seek Error FFs, multiplexing cylinder addresses out of the gate array, and reading fault status.

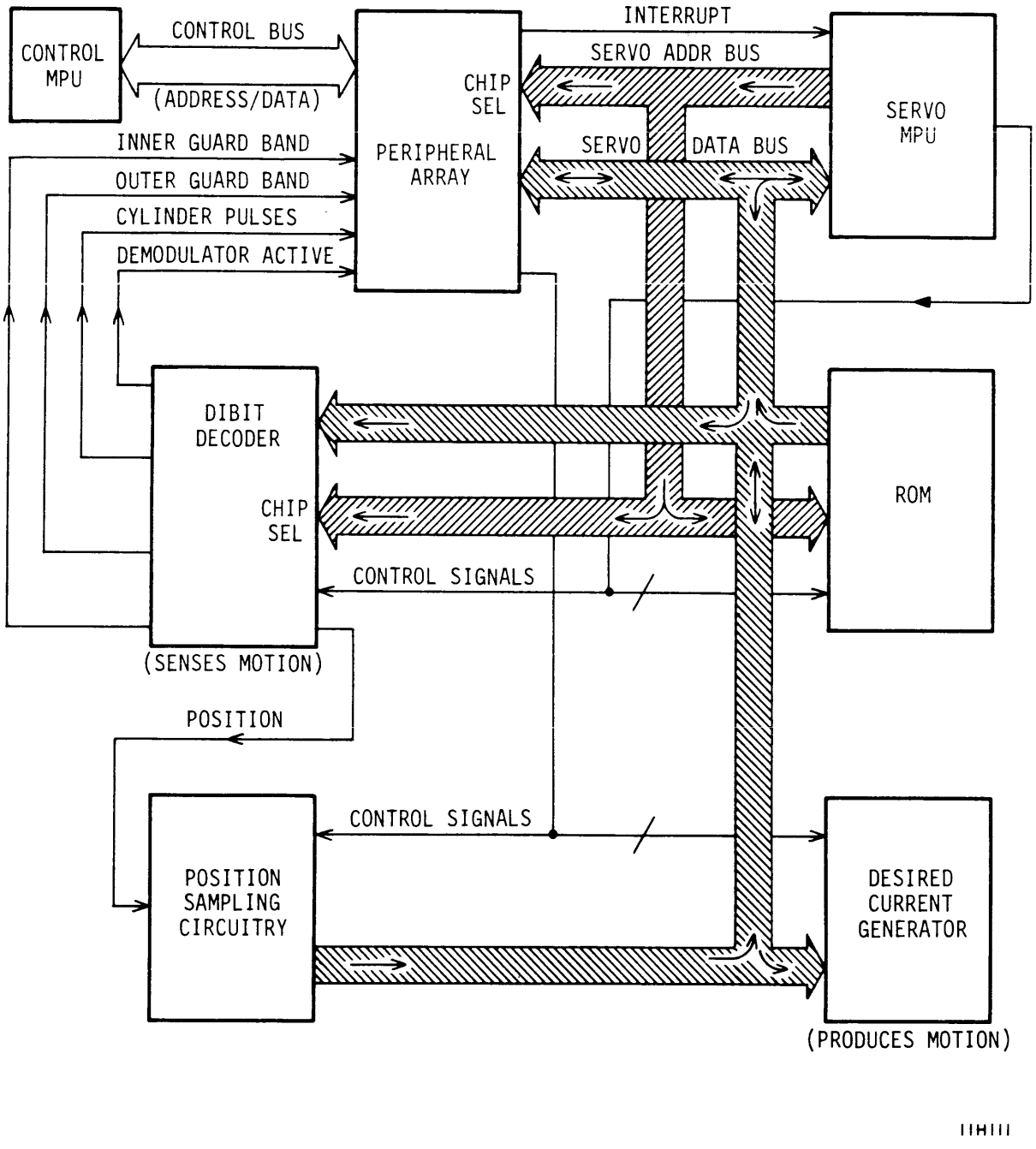


Figure 5-4. Servo MPU and Associated Circuitry

The cylinder pulse counter in the Peripheral Array allows the Servo MPU to count tracks-to-go in a seek. This counter is decremented during seeks by Cylinder Pulses. During the faster portion of a seek, the cylinder pulse timer (also located in the Peripheral Array) allows the Servo MPU to determine the elapsed time between cylinder pulses.

The Servo MPU performs the following basic functions during drive operation:

- It examines the destination address from the Control MPU to determine desired velocity and seek direction.
- It monitors actual velocity and uses this information to control the motion of the actuator during seeks.
- It monitors position error during track-following and uses this information to hold the actuator on track.
- It establishes servo calibration during the load operation and, during longer seeks, updates this calibration.
- It supplies AGC and slope inputs to the dibit demodulator, as described in section 4.
- It provides status to the Control MPU at the end of each seek. This enables the Control MPU to make status transfers to the I/O circuitry and the operator panel (if installed).
- It performs diagnostic seeks requested by the Control MPU. The Control MPU performs diagnostic functions in response to controller commands or to inputs entered on the status/control panel.

Diagnostic operations are described in detail under Diagnostic Functions. In addition, the Servo MPU transmits error status to the Control MPU. This activity is discussed under Fault and Error Conditions in section 7.

The drive employs two basic servo loops, a coarse loop used in the coarse mode and a fine loop used in the settle-in and track-following modes. In the coarse loop, the Servo MPU uses velocity control to move the heads from their starting location to a point close to their destination. In the fine loop, the Servo MPU uses position control to stop the heads at their destination (settle-in mode) and keep them there (track-following mode).

Coarse Loop Operation

The servo system, operating in the coarse loop, moves the heads from the existing cylinder address to within one-half track of the new address. Figure 5-5 is a simplified block diagram of the coarse servo loop. Throughout the coarse seek, the Servo MPU refers to a table in ROM that specifies desired velocity as a function of the number of track crossings (T) remaining until the heads reach their destination.

The velocity table is organized in a manner that allows one table of values to be used for all seeks. The maximum velocity of the table is for 255 tracks. For each number of tracks less than 255, the velocity table specifies a unique velocity value. The way the velocity decreases throughout the remainder of a seek is called a velocity profile. This profile produces constant deceleration of the heads in order to minimize seek times while controlling the approach of the heads to their final position.

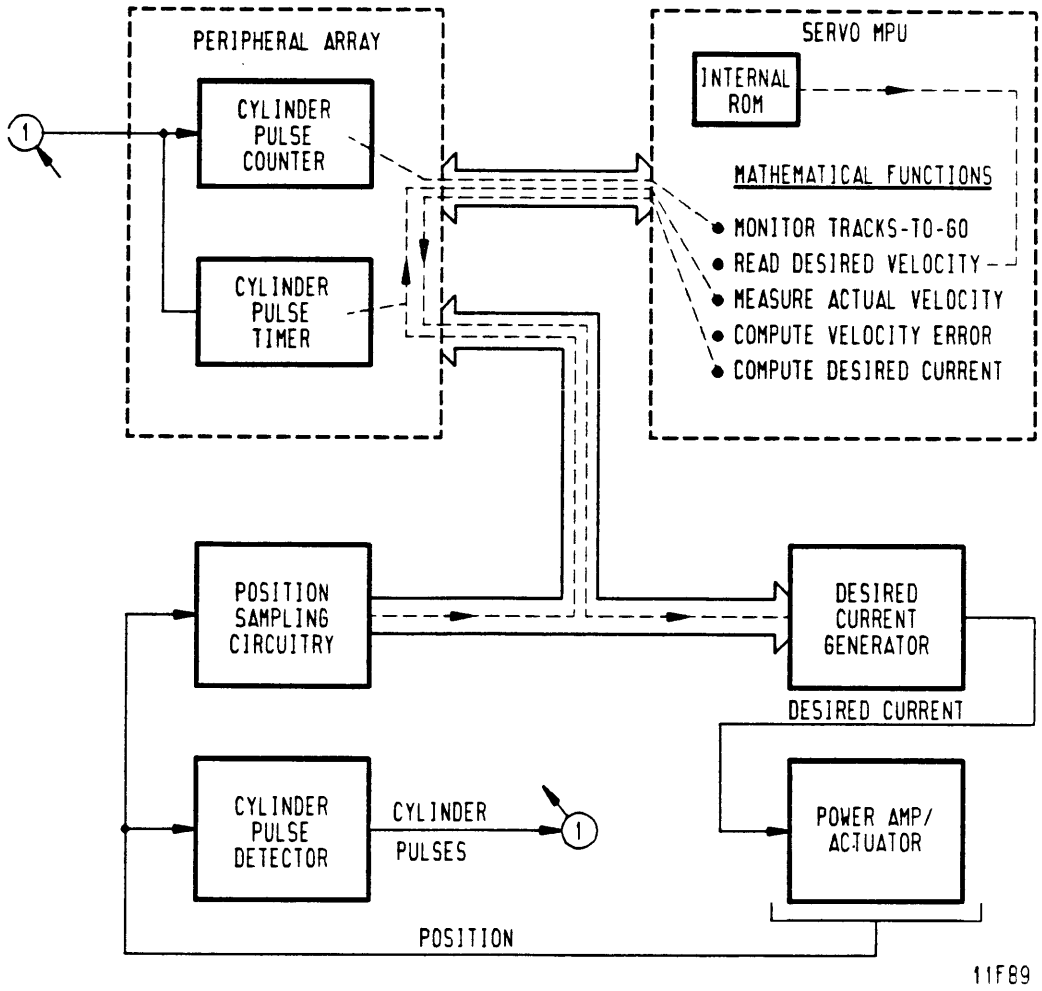


Figure 5-5. Simplified Coarse Servo Loop

An organization of tabulated velocity in terms of tracks to go makes it possible to use one table for all seeks. Different seek lengths start at different points within the table. For example, the velocity specified when T=30 is the same regardless of the total seek length.

At each cylinder crossing, the Servo MPU refers in ROM to the current value of desired velocity. It then compares the current value of desired velocity to actual velocity and computes the difference (error value). Until the next cylinder crossing, the Servo MPU continues to update its computation of desired current based on the computed error value and to output desired current information to the power amplifier.

The Servo MPU needs a continuous indication of actuator velocity throughout seek operations. During coarse loop operation, it computes velocity using two methods -- one method for the high-speed portion of a seek, and another method for the low-speed portion. For longer seeks, the Servo MPU uses high-speed control to move the heads until they are close to their destination; it switches to low-speed control for the remainder of these seeks (typically a number in the range of 5 to 20 tracks-to-go). The Servo MPU uses only low-speed control for very short seeks.

High-Speed Control

During the high-speed portion of a seek operation, the Servo MPU senses actuator velocity indirectly by measuring elapsed time between consecutive cylinder pulses. The elapsed time is counted on a cylinder pulse timer in the Peripheral Array. The desired velocity during high-speed control is read from the velocity table as a desired time-per-track. Both desired velocity and measured velocity have the same form and can be compared to determine velocity error.

Figure 5-6 shows the sequence of activities managed by the Servo MPU during one track of a high-speed seek. When the Servo MPU sees a cylinder pulse, it looks in the velocity table for the desired velocity (time-per-track) for the following track of the seek. It measures the actual velocity by reading the time-per-track count from the cylinder pulse timer.

Knowing both the desired and the actual velocity, the Servo MPU executes a repeating instruction loop. This loop continues until the Servo MPU detects the next cylinder pulse. In each repetition of the loop, the Servo MPU updates the level of desired current specified for the power amplifier. Changes in desired current from one update to the next are limited by filtering.

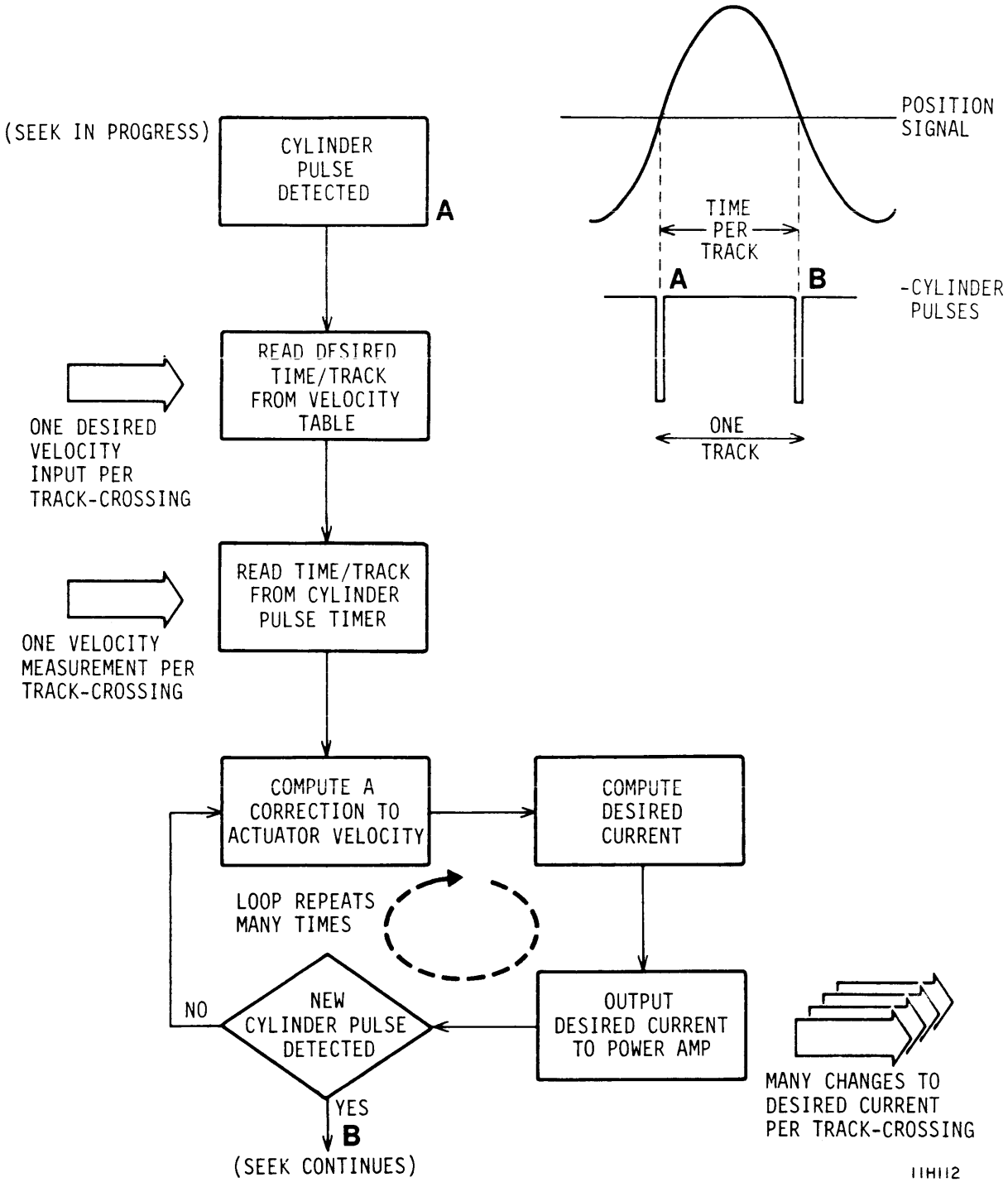


Figure 5-6. One Track of a High-Speed Seek

Low-Speed Control

The Servo MPU uses low-speed control for very short seeks and for the final tracks in longer seeks. During the low-speed portion of a seek operation, the Servo MPU senses actuator velocity from two types of inputs. The Servo MPU examines the Position signal and determines whether the signal is in a peak region or a linear region. While the Position signal is varying in a linear region, the Servo MPU senses velocity by differentiating the Position signal.

During the linear regions, the differentiated Position signal is proportional to velocity. However, when the Position signal is at or near a peak (nonlinear), it contains no velocity information. In the peak regions, the Servo MPU senses velocity by integrating the desired current output it develops for the power amplifier.

Figure 5-7 shows the sequence of activities managed by the Servo MPU during one track of a low-speed seek. When the Servo MPU sees a cylinder pulse, it looks in the velocity table for the desired velocity for the following track of the seek. It measures the actual velocity as described above.

Knowing both the desired and the actual velocity, the Servo MPU executes a repeating instruction loop. This loop continues until the Servo MPU detects the next cylinder pulse. In each repetition of the loop, the Servo MPU samples the position signal, calculates the actual velocity, and updates the level of desired current specified for the power amplifier. Changes in desired current from one update to the next are limited by filtering.

The Servo MPU calibrates its process for measuring low velocities during the backup portion of long return-to-zero (RTZ) seeks. The Servo MPU compares the sensed velocity with a time-per-track measurement and readjusts a mathematical constant used for the low-velocity calculation. The measurement of high velocities requires no calibration because it is based on elapsed-time measurements.

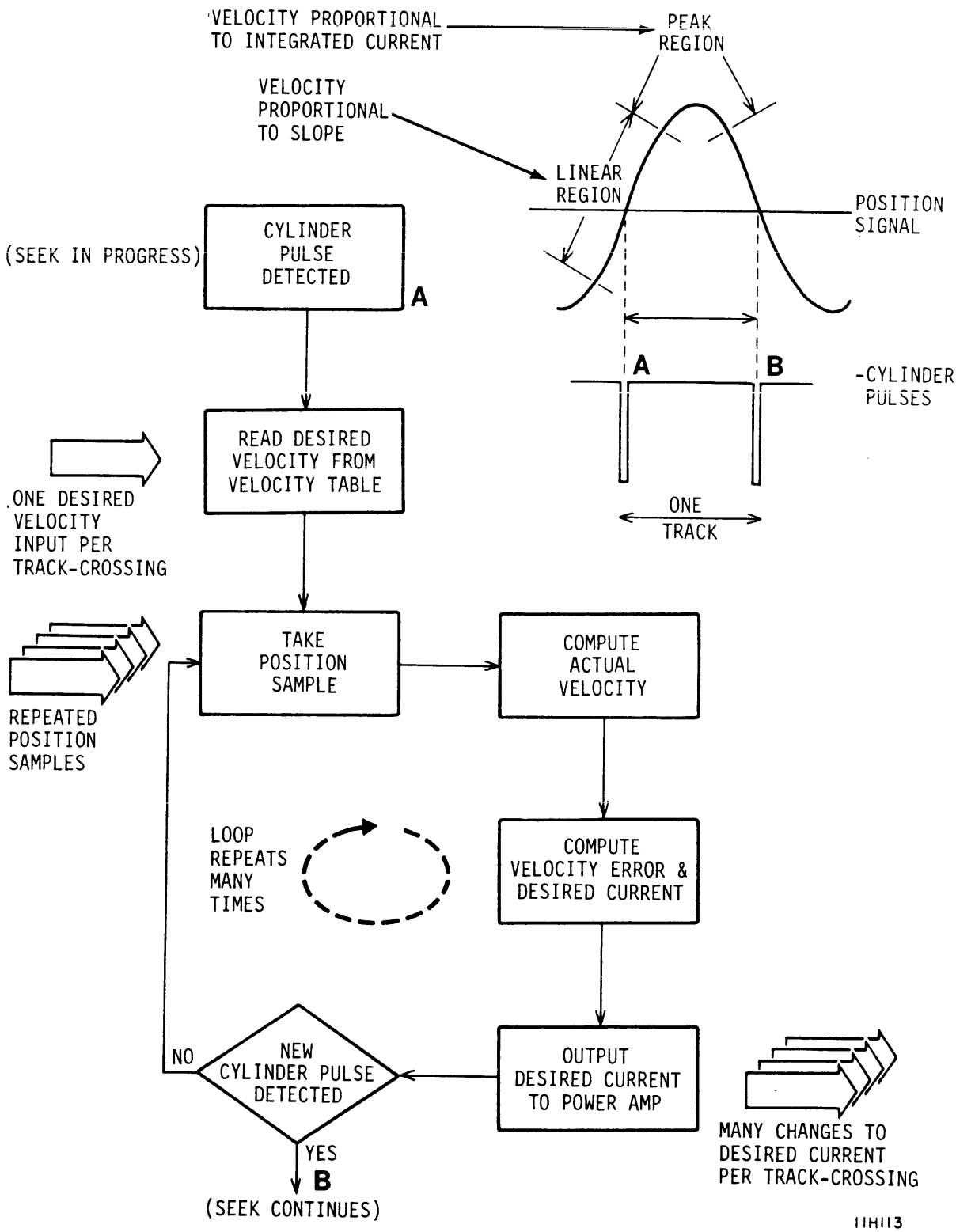


Figure 5-7. One Track of a Low-Speed Seek

Fine Loop Operation

The servo system shifts from the coarse loop to the fine loop when there is 1/2 track remaining in the seek. Fine loop operation continues until the beginning of the following seek. In fine loop operation, the servo system halts the actuator at the destination track during settle-in mode and holds the actuator on track during track-following mode. Figure 5-8 is a simplified block diagram of the fine servo loop.

At the start of a seek, the Servo MPU provides a slope input to the dibit decoder to ensure that Position goes positive as the heads move inward and negative as the heads move outward from their destination track. The Position signal is zero with the heads exactly on track.

The Position signal is the basic error signal for fine loop operation. However, the Servo MPU alters the error signal in the following ways:

- Stability of fine servo loop -- requires the addition of a differentiated position signal to the position signal to create an error signal for the loop.
- Servo offsets -- allow the controller to reposition the heads to either side of track center to recover read errors.
- Increased gain in track-following mode -- gives the servo more responsive control when keeping the heads on track.

In both the settle-in mode and the track-following mode, the Servo MPU samples the Position signal and performs error calculations based on that signal. Using these error calculations, the Servo MPU updates its computation of desired current and outputs desired current information to the power amplifier. Figure 5-9 shows how this loop functions. Because settle-in and track-following make different demands on the servo, each mode has its own type of error calculations.

During the settle-in mode, the Servo MPU controls actuator movement through the last 1/2 track of the seek. The error calculations used in settle-in mode address the goal of stopping actuator movement efficiently.

During the track-following mode, the Servo MPU holds the actuator on track. The error calculations used in track-following mode increase the servo gain at low frequencies to prevent the actuator from drifting off track. An additional shift is added to the position error value if a servo offset is selected. Servo offsets are discussed in the next topic.

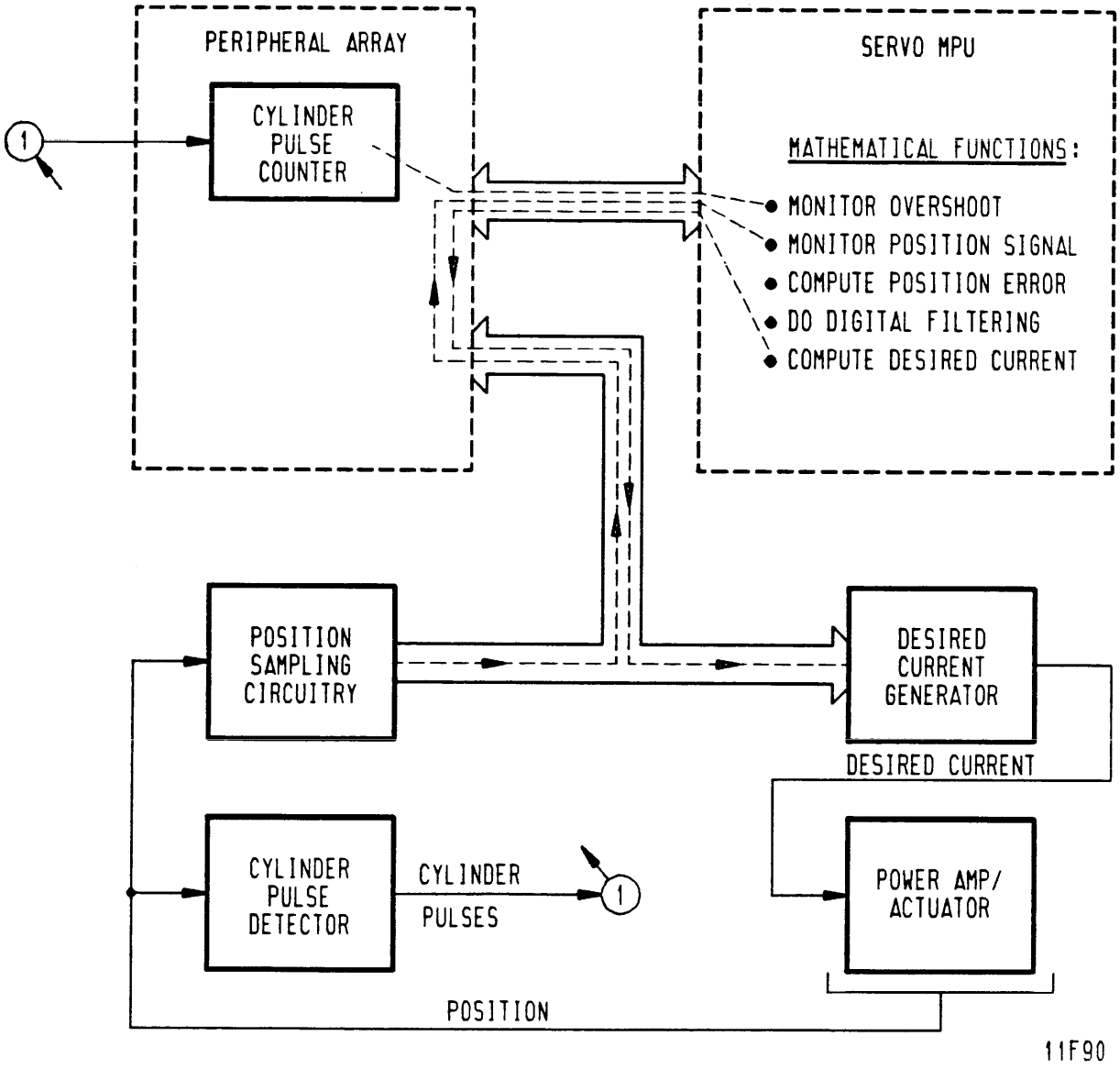


Figure 5-8. Simplified Fine Servo Loop

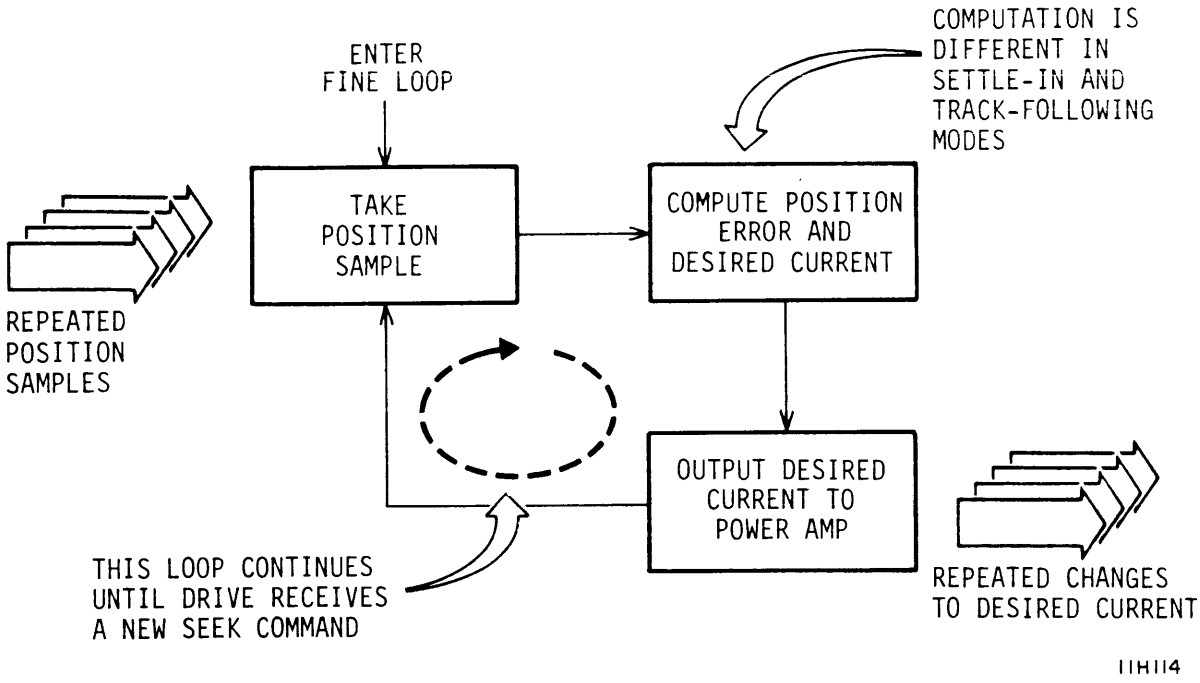


Figure 5-9. Staying on Track with Position Control

The Servo MPU determines whether the heads are on cylinder by examining the voltage level of the Position signal. When the Position signal voltage remains within the on-cylinder limits, the Servo MPU provides status to the Control MPU via the Peripheral Array. In response, the Control MPU transfers On Cylinder status to the I/O circuitry.

Servo Offsets

An offset, a displacement of the heads from track center, results when the controller issues a Servo Offset command in order to recover marginal read data. A gate array on the I/O board decodes the Servo Offset command, activates a bit in its status register, and transmits an I/O Interrupt to the Control MPU.

After receiving an interrupt from either offset command, the Control MPU checks the status of the registers and latches in the I/O gate array. If no faults are present, the Control MPU sends an offset command to the Servo MPU. The offset command contains the amount of offset and the direction of the offset.

With an offset command in effect, the Servo MPU shifts the voltage limits defining an on-cylinder condition. Servo Offset Plus displaces the heads inward from the track center, and Servo Offset Minus displaces the heads outward.

DESIRED CURRENT GENERATOR

The desired current generator (shown in figure 5-10) consists of a 12-bit register and a digital-to-analog (D/A) converter. Each time the Servo MPU updates the desired current, it places a 12-bit digital code on the Servo Data Bus and pulses the D/A Enable line. A pulse on this line clocks the digital levels into the register. The D/A converter changes the register contents to an analog signal, Desired Current, which drives the power amplifier. This signal remains constant until the next update by the Servo MPU.

During power on or system failure, the Control MPU activates the Servo Reset signal. This signal clears the register, ensuring that there will be no force applied to the actuator by the Servo MPU.

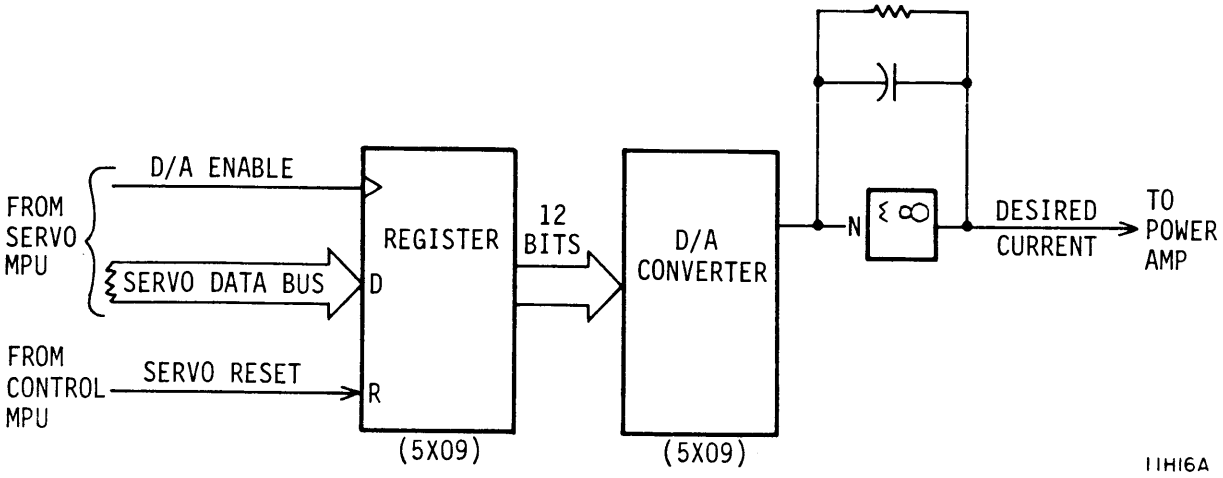


Figure 5-10. Desired Current Generator

POSITION SAMPLING CIRCUITRY

The position sampling circuitry converts the analog Position signal from the dibit demodulator into digital information for the Servo MPU. The Servo MPU samples the Position signal periodically during low-speed control and during position control. No sampling occurs during high-speed control or when the actuator is not on cylinder due to an error condition.

The position sampling circuitry (shown in figure 5-11) consists of a sample and hold circuit driving a analog-to-digital (A/D) converter. When the +Sample/-Hold signal input to the sample and hold circuit is high, the analog values present on the Position signal are gated to the input of the A/D converter. During the A/D conversion, the Servo MPU freezes the input signal to the A/D converter by forcing the +Sample/-Hold signal to go low; this prevents the output of the sample and hold circuit from changing value.

The A/D converter converts the analog Position signal into a digitized Position signal. The Servo MPU starts the conversion by activating the A/D Start line. Data is gated out of the A/D converter when the A/D Enable 0 line goes active.

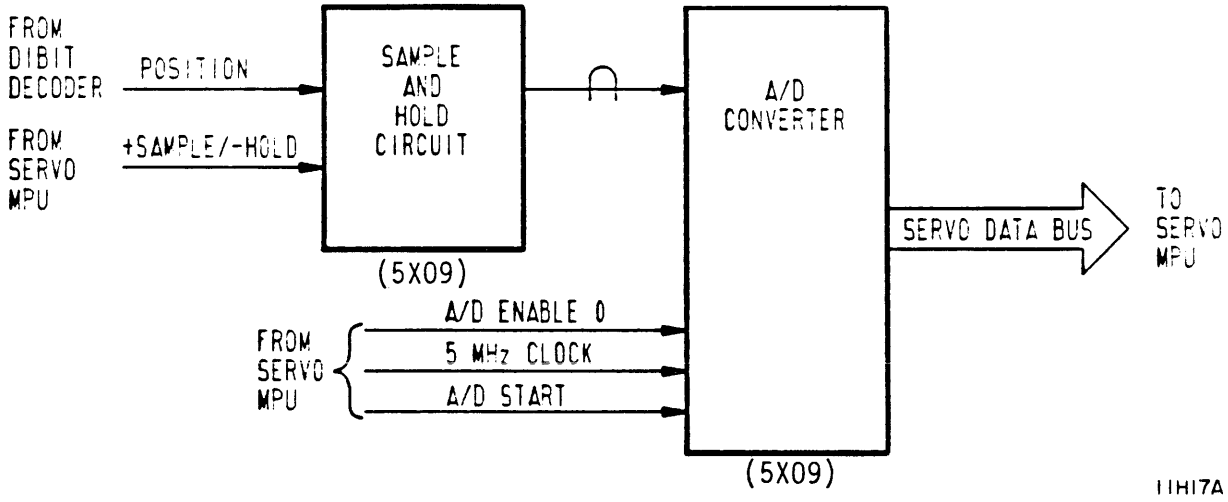


Figure 5-11. Position Sampling Circuitry

POWER AMPLIFIER

The power amplifier produces the actuator current required by the servo loop. The amplifier has two channels -- one channel controlling outward force on the actuator and the other controlling inward force. For purposes of this discussion, they are labelled channel A and channel B on figure 5-12, the simplified block diagram of the power amplifier. Actuator current from channel A forces the actuator to move inward. Current from channel B has the opposite effect.

The Control MPU supplies two input signals that control the power amplifier. The Power Amp Enable signal is active during normal servo operation, where the desired current generator specifies the coil current required by the Servo MPU. The Retract signal is inactive during normal servo operation.

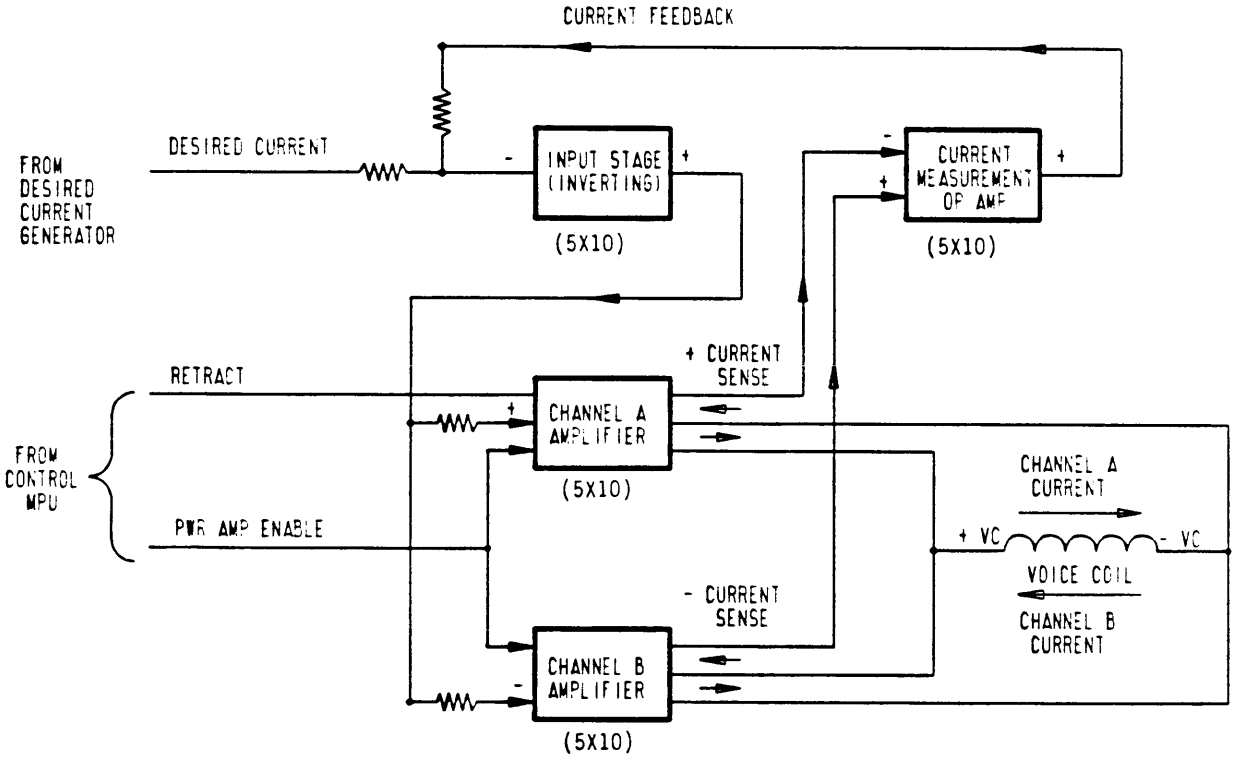


Figure 5-12. Power Amplifier Circuitry

The power amplifier generates coil current from either channel A or channel B in response to the voltage level on the Desired Current line. Through a feedback loop that monitors actuator current, the power amplifier adjusts the gain of the input stage as needed to produce the required coil current. An op amp measures coil current by amplifying current sense signals. The resulting feedback signal and the Desired Current signal are applied to the input stage.

Depending on its polarity, the inverted signal coming from the input stage cuts off one channel and enables the other. Although both channels are powered by the +24 volt supply, they produce opposite currents in the voice coil. The magnetic field of the voice coil interacts with the field of permanent magnets placed near the voice coil. The resulting force causes the actuator to accelerate or decelerate during servo positioning.

A retract operation moves the actuator until the heads are located in the landing zone. The Servo MPU uses the Desired Current line for normal head unloading before powering down the spindle. The Servo MPU performs a normal retract also when a loss of motor speed is detected.

An emergency retract operation occurs as the result of a power loss (Low Vcc active). When the Retract line is active and the Power Amp Enable line is inactive, the channel B amplifier is shut off. However, a separate biasing circuit in the channel A amplifier enables that channel. Although voltages from the power supply are dropping during a power loss, the channel A amplifier continues to receive the power it needs from the +24 volt line. The drive motor generates current as it decelerates, and that current is available to the power amplifier.

TYPES OF SEEKS

The drive has five basic types of seeks:

- Load Operation -- Starts the drive motor and moves the heads from the landing zone to track 0.
- Normal Seek -- Moves the heads from one cylinder on the disk to another.
- Return to Zero (RTZ) Seek -- Clears a seek error and moves the heads from any location on the disk to track 0.
- Unload Operation -- Moves the heads back to the landing zone during a power off operation.
- Sweep Cycle -- Varies the position of the heads during idle periods by doing patterns of normal seeks.

The load and RTZ operations use both the outward and inward movements to move the actuator to track 0. The unload operation is an inward movement that moves the heads to the landing zone beyond the inner guard band.

Normal seek operations can be either inward or outward movements, depending upon where the new address is located relative to the present address. Upon successful completion of a load, normal seek, or RTZ operation, the Servo MPU remains active and continues to maintain the actuator on track. The five basic seek operations and track following are discussed in the following text.

LOAD OPERATION

The load operation starts the drive motor and moves the heads from the landing zone to track 0. A load operation cannot take place until power on initialization is successfully completed. Refer to the Power Functions discussion in section 2 for details about power on initialization. The load operation is described in the following paragraphs and is flowcharted in figure 5-13.

With start conditions present (refer to Power Sequencing in section 2), the Control MPU starts the drive motor by activating the Motor Run line to the Motor MPU. Thereafter, the Control MPU requests status from the Motor MPU at 30 millisecond intervals. When speed OK is sensed on the Motor Sense 0-2 status lines, the Control MPU enables the power amplifier, unlocks the actuator, and sends a load command to the Servo MPU. Operation of the Motor MPU and drive motor is discussed in section 2 under Controlling the Disk Rotation.

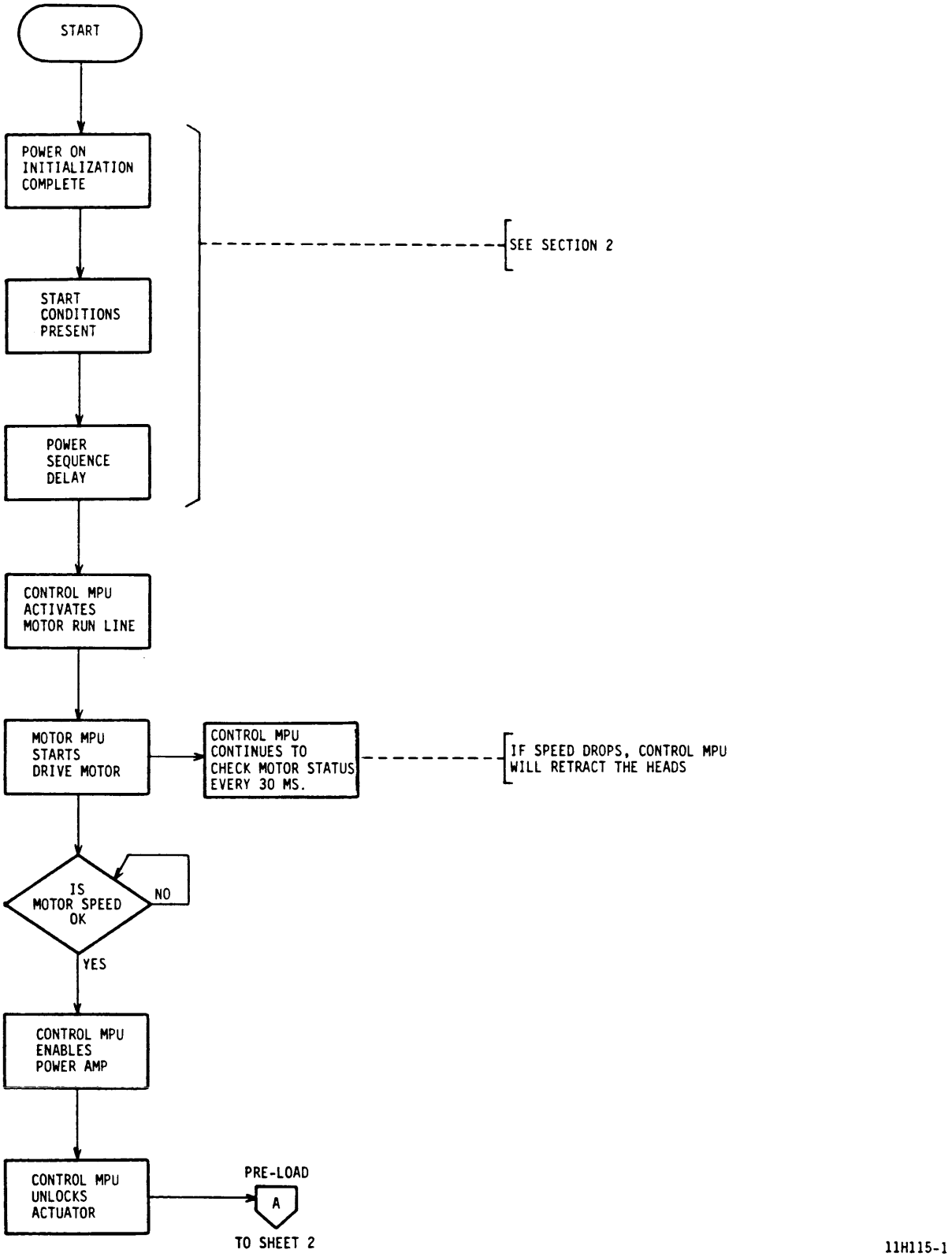


Figure 5-13. Load Operation Flowchart (Sheet 1 of 4)

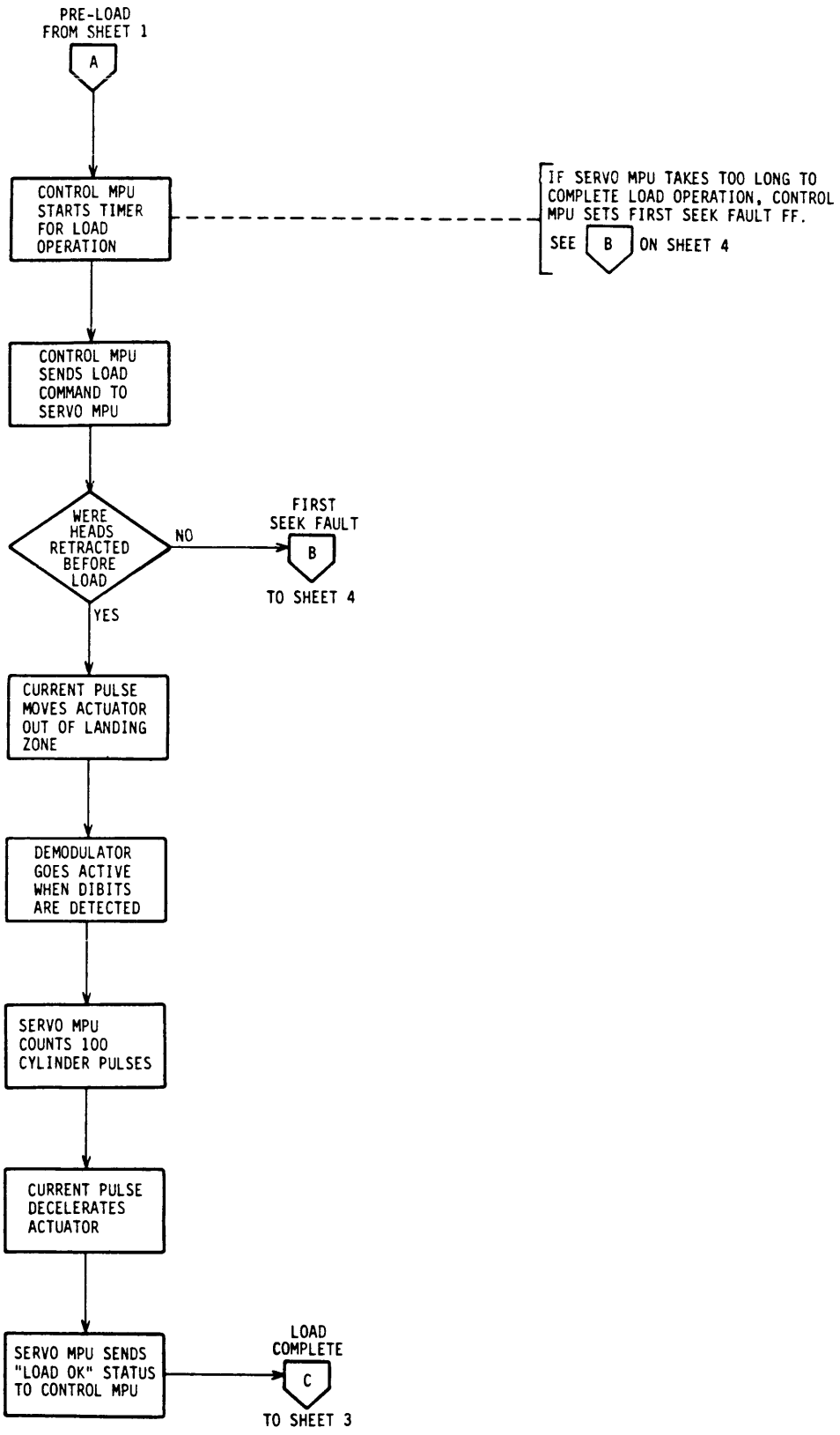


Figure 5-13. Load Operation Flowchart (Sheet 2)

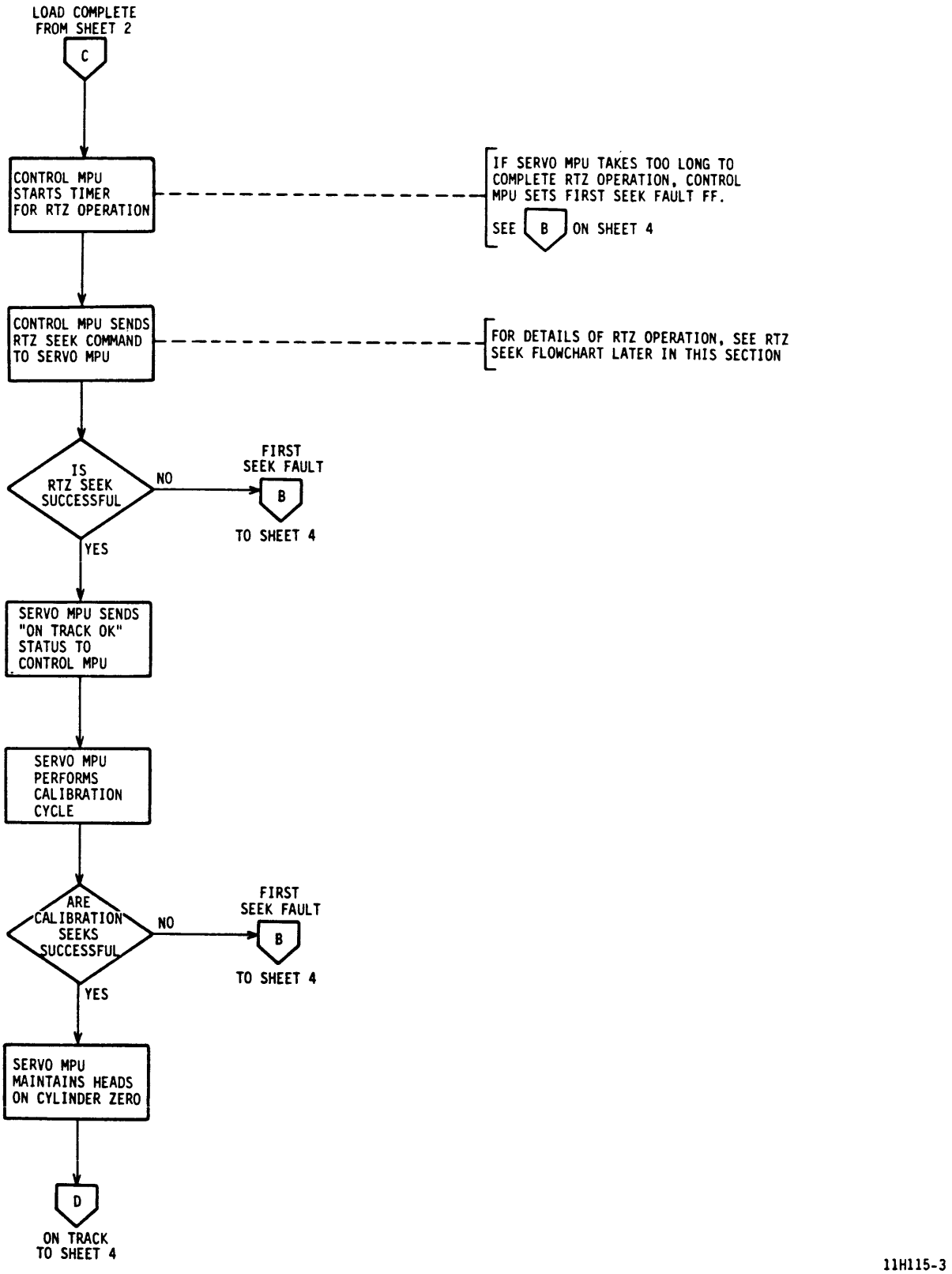


Figure 5-13. Load Operation Flowchart (Sheet 3)

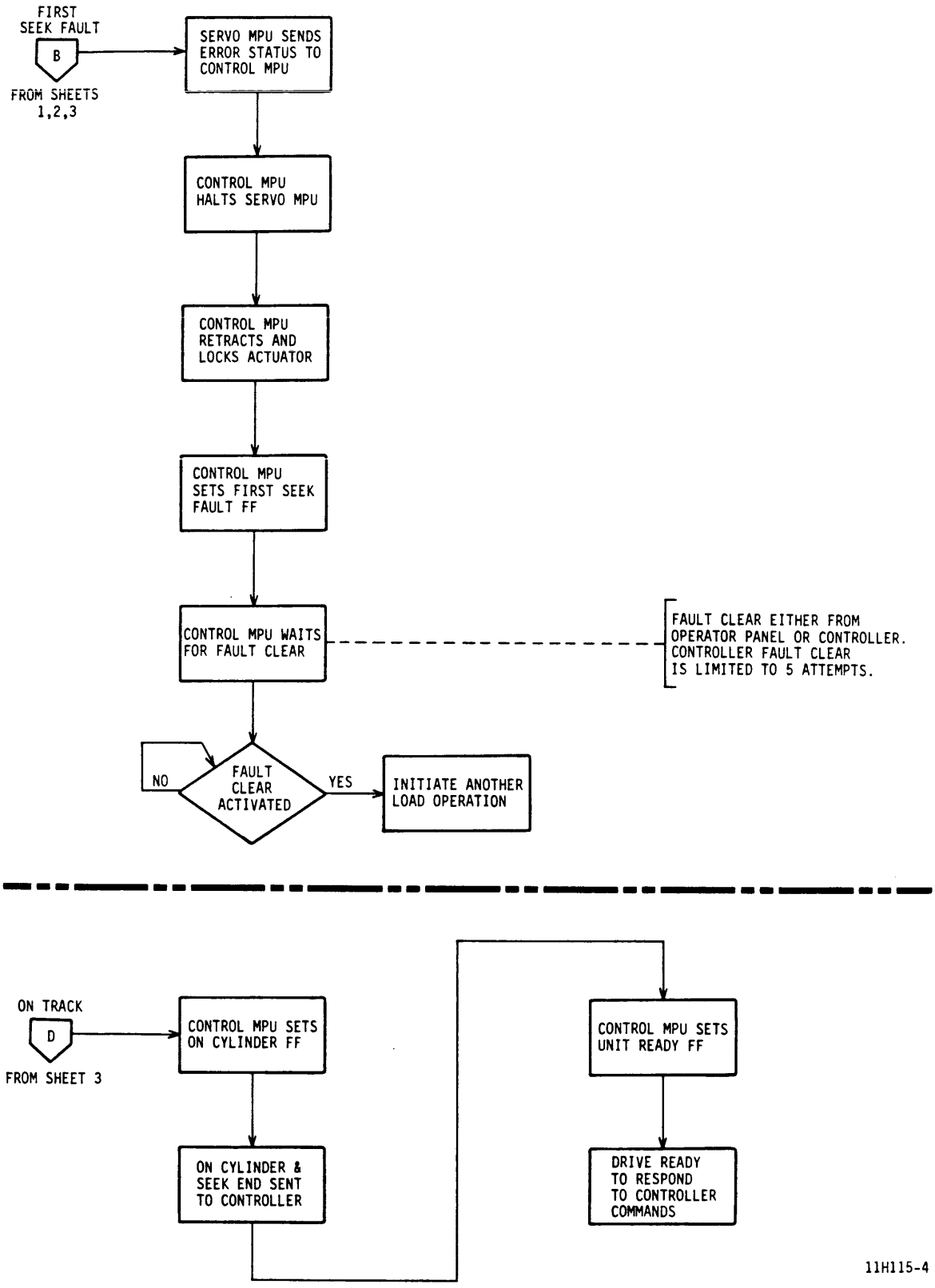


Figure 5-13. Load Operation Flowchart (Sheet 4)

Prior to moving the heads, the Servo MPU checks to ensure that the Demodulator Active line is inactive following a successful retract. This is expected because there is no dibit pattern present in the landing zone. The Demodulator Active line can be active only when the heads are over the guard bands or the data zone.

Assuming a successful retract, the Servo MPU develops a desired current pulse that forces the actuator to move from the landing zone toward the data zone. Figure 5-14 shows that the actuator moves outward from the inner radius of the disks during the load seek. The Demodulator Active signal goes active when the dibit decoder has locked onto the servo signal. At this time, the Servo MPU turns off desired current, allowing the actuator to coast.

The Servo MPU counts cylinder pulses during the coast phase. After counting 100 cylinder pulses, the Servo MPU develops a desired current pulse that slows the actuator. The Servo MPU then reports Load OK status to the Control MPU. If this status is not received within a reasonable time, the Control MPU aborts the first seek and issues a first seek fault.

If the load was completed within the allotted time, the Control MPU issues an RTZ command to the Servo MPU. At the completion of the RTZ portion of the load operation, the Servo MPU sends On Track OK status to the Control MPU. If this status is not received within a reasonable time, the Control MPU aborts the first seek and issues a first seek fault.

With the load operation complete, a calibration cycle takes place. The Control MPU issues the Servo MPU a series of commands that result in sequences of seeks. These sequences include short seeks, starting at track 0 and extending across the data zone, return-to-zero (RTZ) seeks, and continuous seeks at the outer and inner limits of the data zone. Using these seeks, the Servo MPU calibrates the following servo functions:

- Position Gain -- During the continuous seeks, the Servo MPU samples the peak-to-peak level of the Position signal and supplies an AGC input to the dibit decoder circuit. This also calibrates velocity measurement in the low velocity mode.

- Actuator Force -- During the continuous seeks, the Servo MPU makes time-per-track measurements. Using these measurements, it adjusts the actuator force constant to compensate for any variations in the servo system. This constant determines the level of Desired Current sent to the power amplifier.

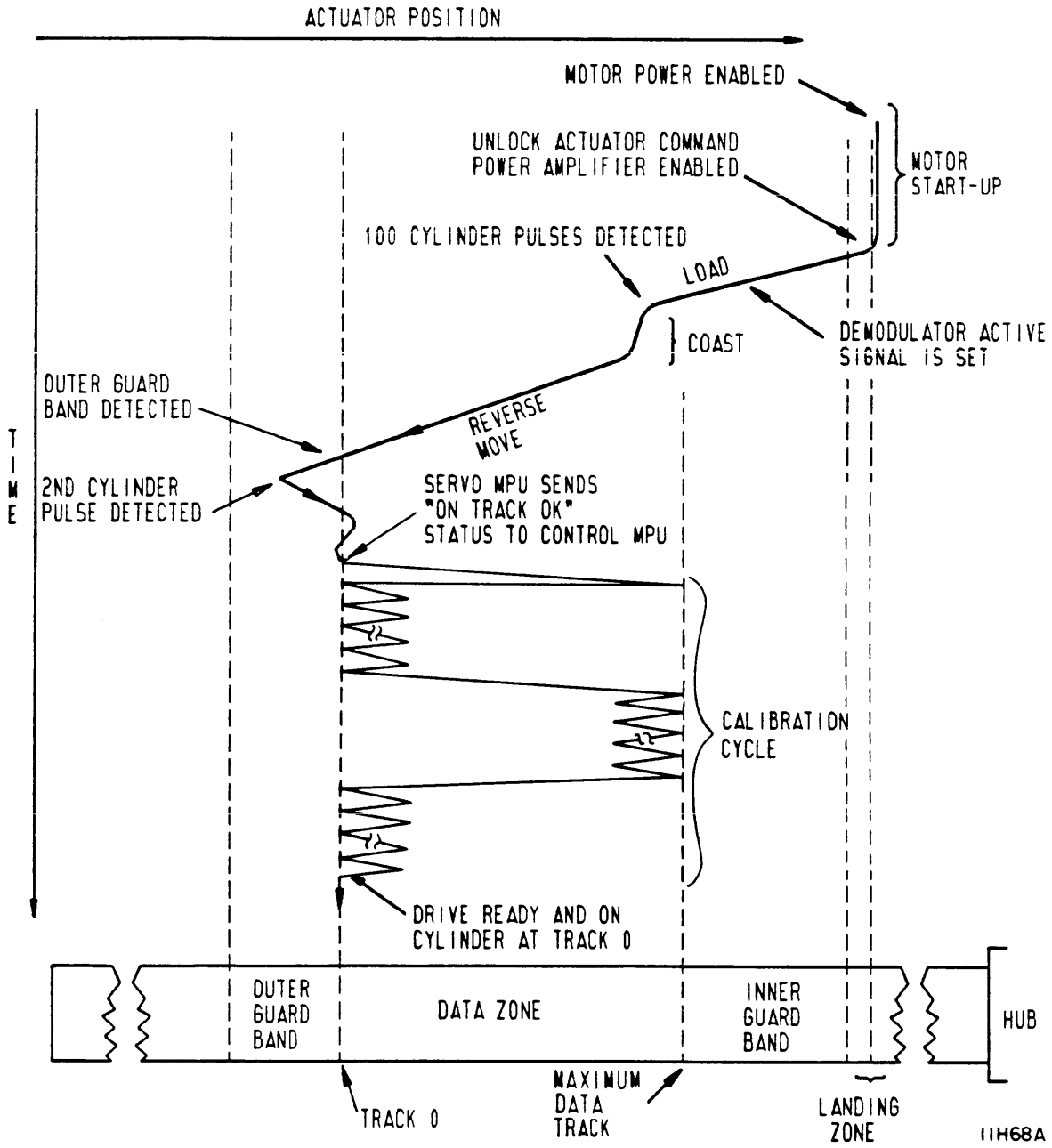


Figure 5-14. Load Seek Trajectory

As shown in the flowchart, a successful load operation must meet a number of requirements. These requirements include:

- The load portion of the operation must be completed successfully within a reasonable time.
- The RTZ portion of the operation must be completed successfully within a reasonable time.
- The calibration cycle must be completed properly within two attempts.

If all these requirements are met, the Control MPU sets the On Cylinder FF and Unit Ready FF. With these FFs set, On Cylinder status, Seek End status, and Unit Ready status are available to the controller.

If any requirement fails to be met, the Control MPU attempts to retract and lock the actuator. It then sets the First Seek Fault FF. As a maintenance aid, the Control MPU displays a status code on the status/control panel. These codes, discussed in the maintenance manual, indicate where the seek operation failed.

You can clear the fault by pressing the Fault Clear switch (on units with an operator panel), or by issuing a Fault Clear command from the controller. Pressing the Fault Clear switch or issuing a Fault Clear command initiates another load attempt. The drive recognizes up to five Fault Clear commands from the controller.

After sending On Track OK status to the Control MPU, the Servo MPU remains active. The Servo MPU continually makes corrections to the actuator position to keep the heads on track zero. If the Servo MPU fails to maintain the heads on cylinder, it sends error status to the Control MPU. For more details refer to the description under Track Following.

NORMAL SEEK

Normal seeks are initiated by controller command and implemented by the drive servo circuitry. The normal seek is the operation used to move the heads from one location to another on the disk surface. The same track can also be selected, but a zero-track seek requires no actuator movement, and the operation is handled within the I/O circuitry.

The normal seek occurs in two directions, reverse (from the center towards the outer edge) and forward (from the outer edge towards the center). Going from a higher-numbered track to a lower-numbered one involves an outard movement of the actuator, while going from a lower-numbered track to a higher numbered one involves an inward movement. Figure 5-15 is a detailed flowchart showing the normal seek operation.

On longer seeks, the Servo MPU makes time-per-track measurements and uses this data to readjust the actuator force constant (see Load Operation).

With the drive in the unit ready and on cylinder conditions, the controller initiates a normal seek by selecting the drive and transmitting a seek command (refer to I/O Signal Processing in section 3 for details). The cylinder address is gated into the Cylinder Address register (in a gate array on the I/O board) by the seek command.

If a new seek command leaves the Cylinder Address register contents unchanged (a zero-track seek), the I/O circuitry responds to the command, and no I/O Interrupt is enabled to the Control MPU. If a new seek command requires a seek to a different seek address, however, the seek command clears the On Cylinder FF and generates an I/O Interrupt to the Control MPU.

The Control MPU responds to this interrupt by examining the state of the registers and latches in the I/O gate array. The Control MPU transfers the destination cylinder address from the Cylinder Address register into the Peripheral Array and checks whether this address is legal. The highest legal address is cylinder 1634 on 736 MB, 1120 MB, 1153 MB, and 1230 MB drives (1380 on 850 MB drives). If the address is legal, the Control MPU sends a seek command to the Servo MPU. If the address is illegal, the Control MPU sets the Seek Error FF in the I/O circuitry and waits for an RTZ seek command from the controller.

Prior to starting a seek operation and at 30 millisecond intervals thereafter, the Control MPU checks the Motor Status 0-2 lines to make sure that no motor fault condition exists and the motor is up to speed. At the start of the seek, the Control MPU loads a timer (so that a Seek Error will be indicated if the seek is not completed at the end of the timeout).

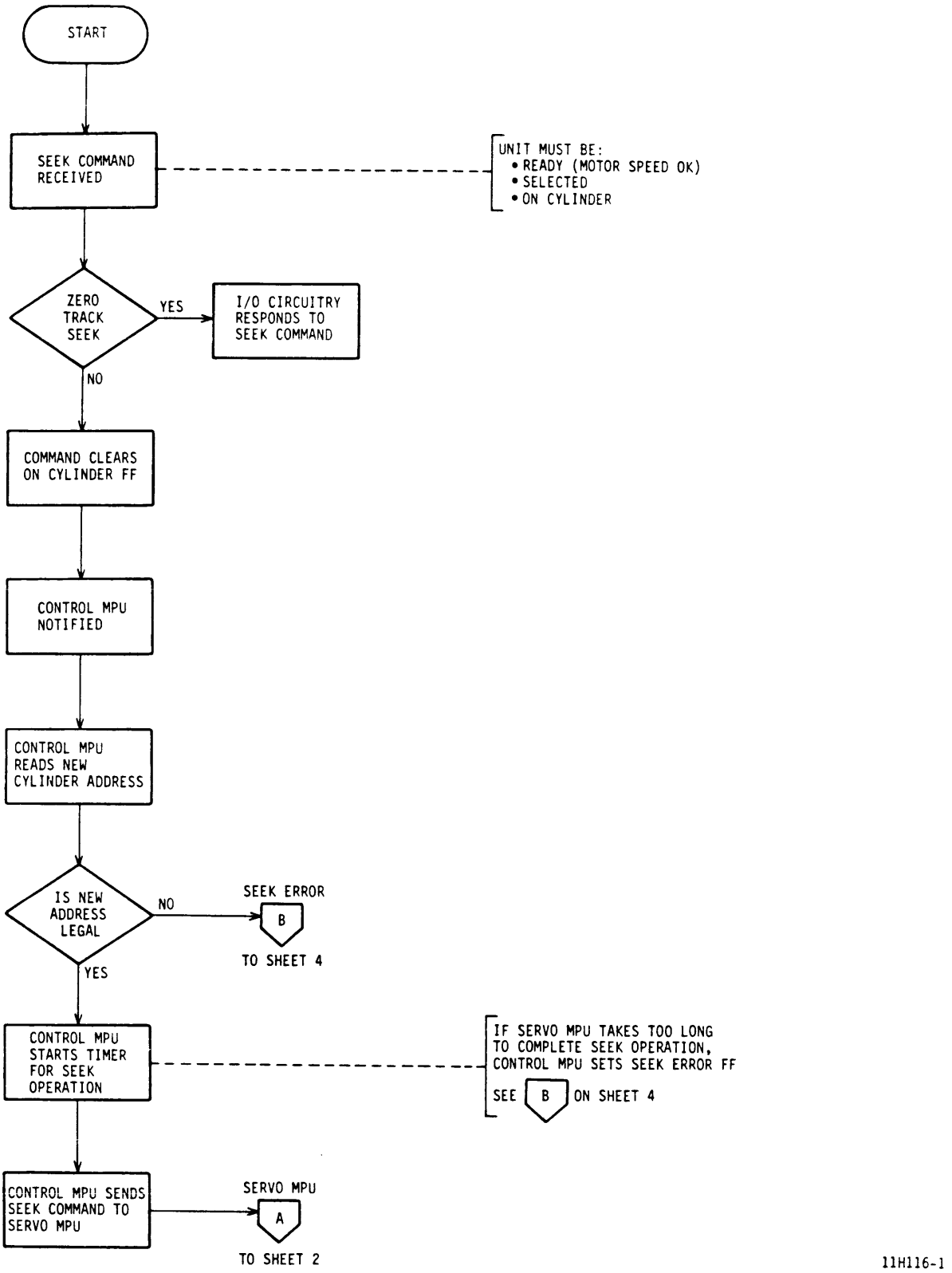


Figure 5-15. Normal Seek Flowchart (Sheet 1 of 4)

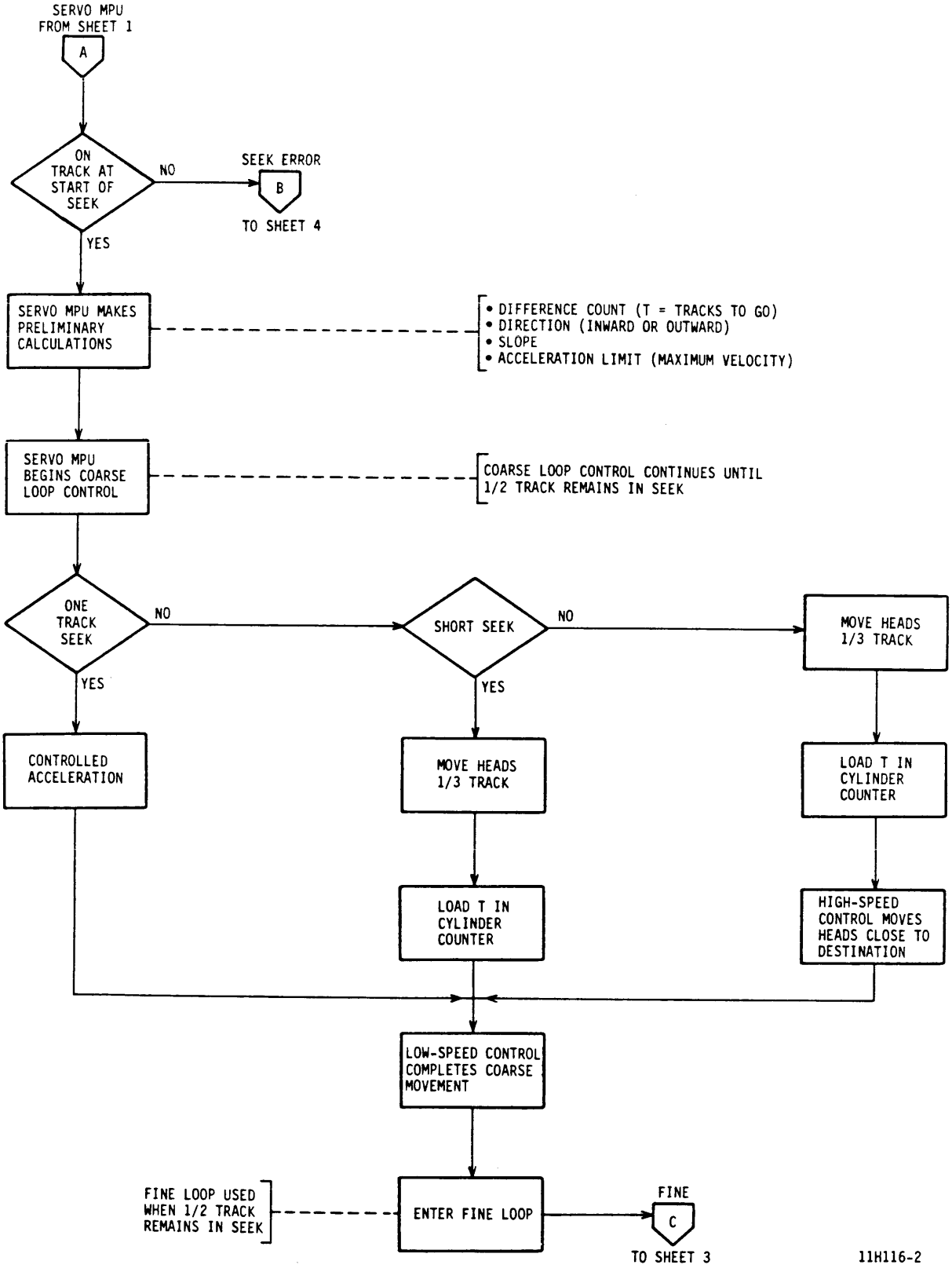


Figure 5-15. Normal Seek Flowchart (Sheet 2)

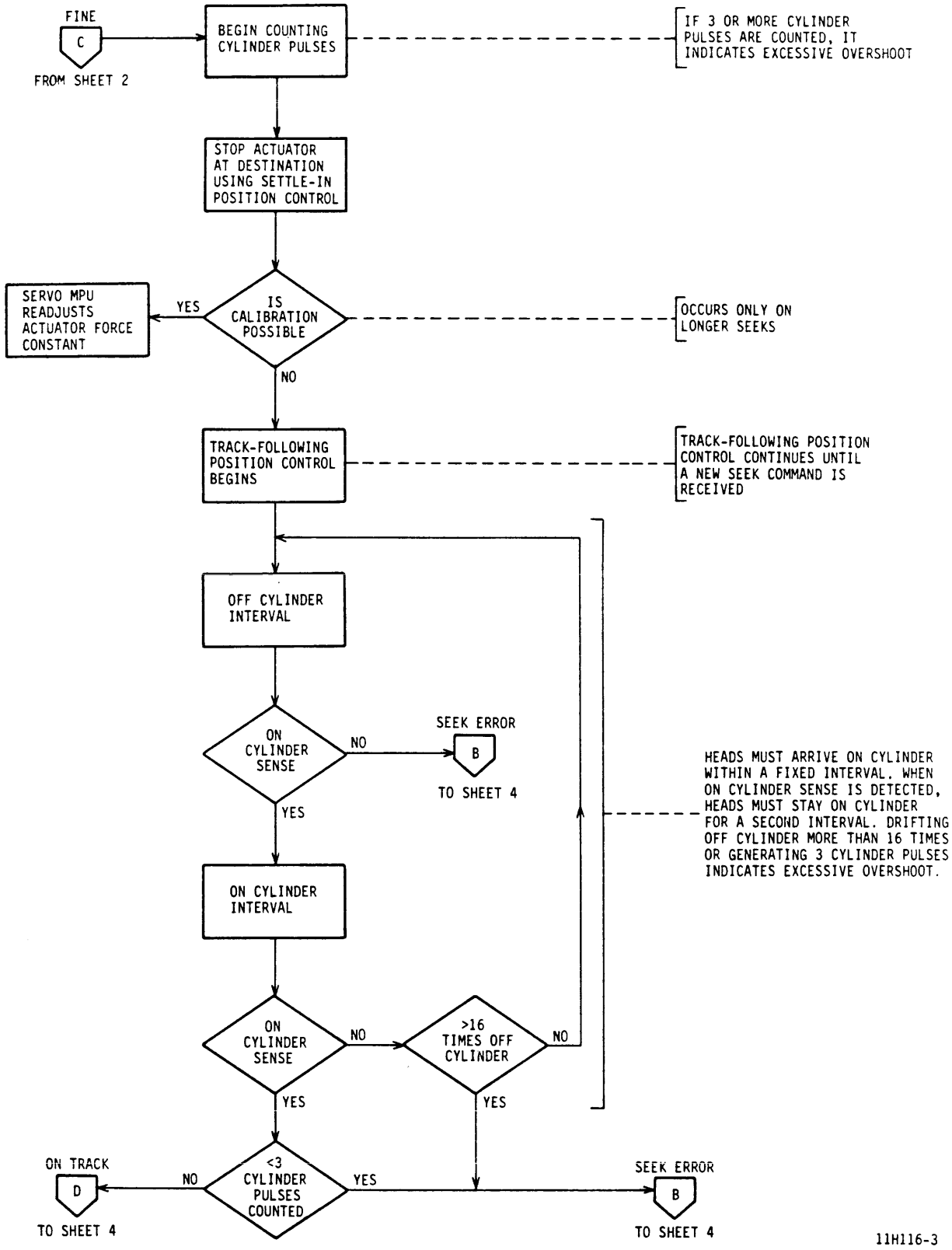


Figure 5-15. Normal Seek Flowchart (Sheet 3)

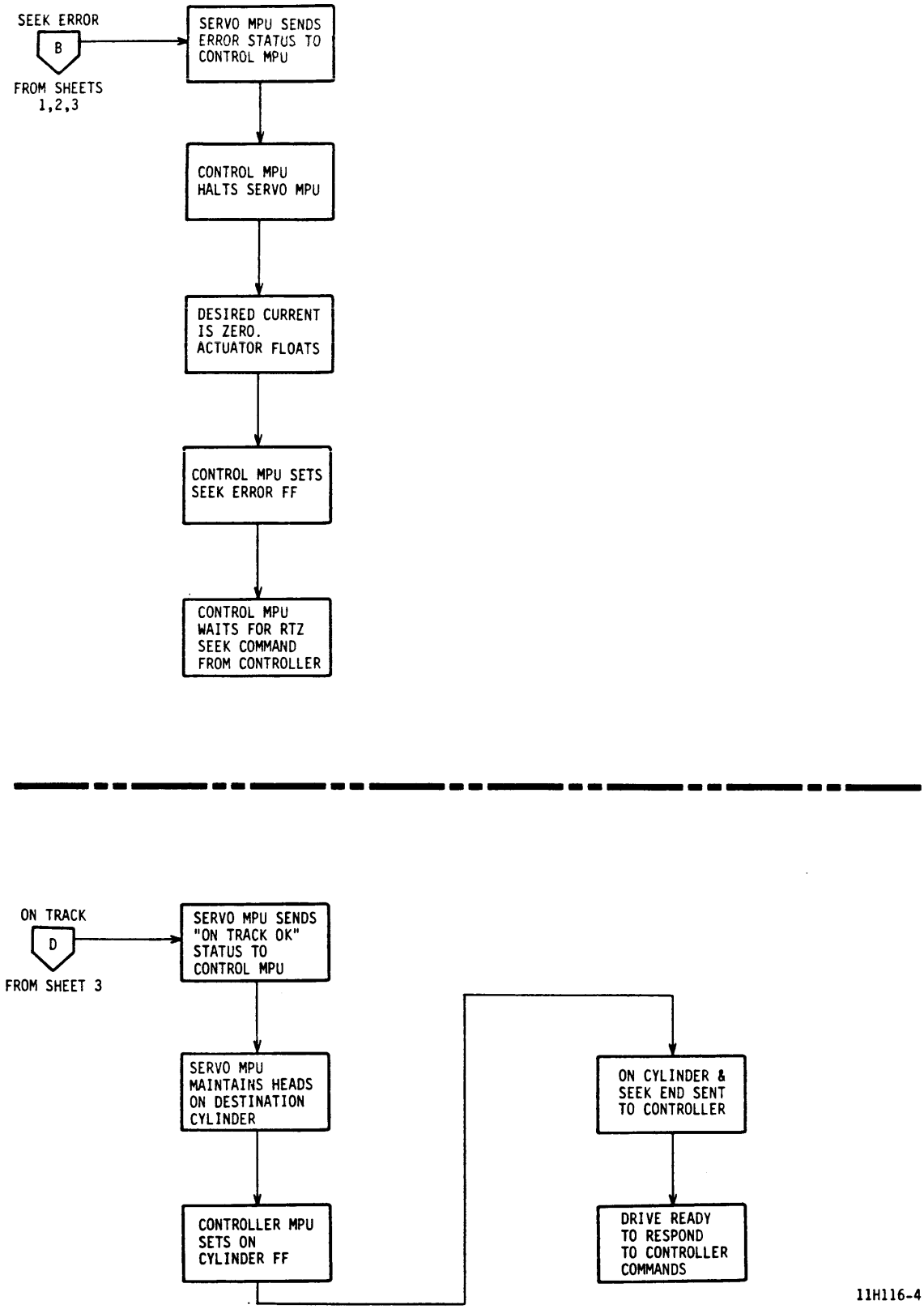


Figure 5-15. Normal Seek Flowchart (Sheet 4)

The seek operation from this point until the on cylinder condition is achieved is under the control of the Servo MPU. Initially, the Servo MPU checks to ensure that the actuator is on cylinder at the start of the seek. After performing this check, the program compares the new address with the present address (stored in ROM memory) to calculate the difference between the two (T=tracks to go), and the direction of the move (in or out). The difference count is then transmitted to the cylinder pulse counter in the Peripheral Array.

The Servo MPU provides a slope input to the dibit decoder circuit to ensure that the decoded position signal has the proper phase at the destination track.

At this point, the Servo MPU begins coarse loop control. This control remains in effect until the heads are within 1/2 track of their destination. Operation of the coarse loop depends on the seek length as follows:

- One-track seeks -- The Servo MPU builds an accelerating velocity ramp after starting a timeout. At the completion of the timeout, there is a controlled deceleration.

- Short seeks -- The actuator accelerates until its velocity matches the velocity profile. It then decelerates under low-speed control.

- Long seeks -- The actuator accelerates until its velocity matches the velocity profile. If it reaches maximum velocity with more than 255 tracks-to-go, it coasts under high-speed control. It then decelerates under high-speed control. Close to the destination the deceleration switches over to low-speed control.

For more information about high-speed control and low-speed control, refer to Coarse Loop Operation earlier in this section. High-speed control and low-speed control differ mainly in the way that velocity is measured. With both methods, the Servo MPU compares the values obtained for actual velocity to tabulated values of desired velocity stored in memory. The error value produced by each comparison is used to generate a level of desired current for the power amplifier.

Starting with T less than 1, the Servo MPU begins to integrate actual velocity to determine when 1/2 track remains in the seek. When 1/2 track is detected, the Servo MPU sets the cylinder counter to 3, and initiates a settle-in delay. In settle-in mode, the Servo MPU shifts from velocity control to position control. The Servo MPU examines the position signal, computes a position error, and then uses this error value to generate desired current.

After the settle-in delay times out, the Servo MPU enters the track-following mode. When operating in the track-following mode, the Servo MPU adds a low frequency gain boost to the positioning loop. During this time the Servo MPU starts two timeouts in succession to ensure that the actuator arrives on cylinder and remains on cylinder. In this phase of the seek, the Servo MPU declares error status if any of the following occurs:

- The actuator fails to arrive on cylinder during the first timeout.
- The actuator drifts off cylinder more than 16 times during the second timeout.
- The Servo MPU detects three or more cylinder pulses after entering fine loop operation.

At the end of the seek operation, the Servo MPU sends status to the Control MPU. The Control MPU aborts the seek and issues a seek error for any of the following reasons:

- Servo MPU status is not received within a reasonable time.
- The seek operation is unsuccessful.
- The controller requested an illegal address.

In these cases, the Control MPU sets the Seek Error FF in the I/O circuitry. With this FF set, Seek Error and Seek End status are available to the controller. As a maintenance aid, the Control MPU displays a status code on the status/control panel. These codes, discussed in the maintenance manual, indicate where the seek operation failed.

If the seek operation was successful, the Control MPU sets the On Cylinder FF in the I/O circuitry. With this FF set, On Cylinder and Seek End status are available to the controller.

After sending On Track OK status to the Control MPU, the Servo MPU remains active. The Servo MPU continually makes corrections to the actuator position to keep the heads on the destination track. If the Servo MPU fails to maintain the heads on cylinder, it sends error status to the Control MPU. For more details refer to the description under Track Following.

RETURN TO ZERO SEEK

Return to Zero (RTZ) seeks move the heads from any location on the disk to track 0. Although the Control MPU uses an RTZ seek as part of the load operation, the controller can command RTZ seeks also. Both types of RTZ seeks are identical, except for the status presented if they fail.

If the RTZ seek in a load operation is unsuccessful, or takes too long to complete, the Control MPU sets the First Seek Fault FF. A reattempt occurs if the Fault Clear switch is pressed (units with an operator panel), or if the controller issues a Fault Clear command.

If a controller-initiated RTZ seek is unsuccessful, or takes too long to complete, the Control MPU does the following:

- It sets the Seek Error FF.
- It clears the On Cylinder FF.
- It disables the power amplifier.

In this case, the drive waits for another RTZ command from the controller.

This discussion pertains both to the controller-initiated RTZ seek and to the RTZ portion of a load operation. The controller-initiated RTZ seek is flowcharted in figure 5-16.

With the drive in the Unit Ready condition, the controller initiates an RTZ seek by selecting the drive and transmitting an RTZ Seek command (refer to I/O Signal Processing in section 3 for details). The RTZ Seek command clears the Cylinder Address register, the Head Address register, the On Cylinder FF, and the Seek Error FF.

The decoded command also sends an I/O interrupt to the Control MPU. The Control MPU responds to this interrupt by communicating with a gate array on the I/O board. Prior to starting an RTZ operation and at 30 millisecond intervals thereafter, the Control MPU checks the Motor Status 0-2 lines to make sure that no motor fault condition exists and the motor is up to speed. The Control MPU then directs the Servo MPU to initiate an RTZ operation.

Beginning with this command to the Servo MPU and ending with a status transfer to the Servo MPU, both the controller-initiated RTZ seek and the RTZ portion of the load operation follow identical sequences.

The Servo MPU reads the RTZ command and initiates the RTZ. The Servo MPU checks the Demodulator Active signal, the Outer Guard Band signal, and the Inner Guard Band signal. If the heads are outside the data zone, the Servo MPU moves the heads back into the data zone. Initially, the Servo MPU cuts off actuator current and waits for the actuator velocity to drop to 2 inches per second.

When this occurs, the Servo MPU initiates a slow reverse move. After detecting the Outer Guard Band, the Servo MPU reduces the desired velocity and continues the reverse move for two cylinder counts. Following this, the Servo MPU resets the cylinder counter to 2 and begins a slow forward move. It then checks to ensure that the Outer Guard Band signal goes inactive before the cylinder counter decrements to zero.

Starting with T less than 1, the Servo MPU begins to integrate actual velocity to determine when 1/2 track remains in the seek. When 1/2 track is detected, the Servo MPU sets the cylinder counter to 3, and initiates a settle-in delay. In settle-in mode, the Servo MPU shifts from velocity control to position control. The Servo MPU examines the position signal, computes a position error, and then uses this error value to generate desired current.

After the settle-in delay times out, the Servo MPU enters the track-following mode. When operating in the track-following mode, the Servo MPU adds a low frequency gain boost to the positioning loop. During this time the Servo MPU starts two timeouts in succession to ensure that the actuator arrives on cylinder and remains on cylinder. In this phase of the seek, the Servo MPU declares error status if any of the following occurs:

- The actuator fails to arrive on cylinder during the first timeout.
- The actuator drifts off cylinder more than 16 times during the second timeout.
- The Servo MPU detects three or more cylinder pulses after entering fine loop operation.

At the end of the RTZ operation, the Servo MPU sends status to the Control MPU. For controller-initiated RTZ seeks, the Control MPU aborts the seek and issues a seek error for any of the following reasons:

- Servo MPU status is not received within a reasonable time.
- The seek operation is unsuccessful.

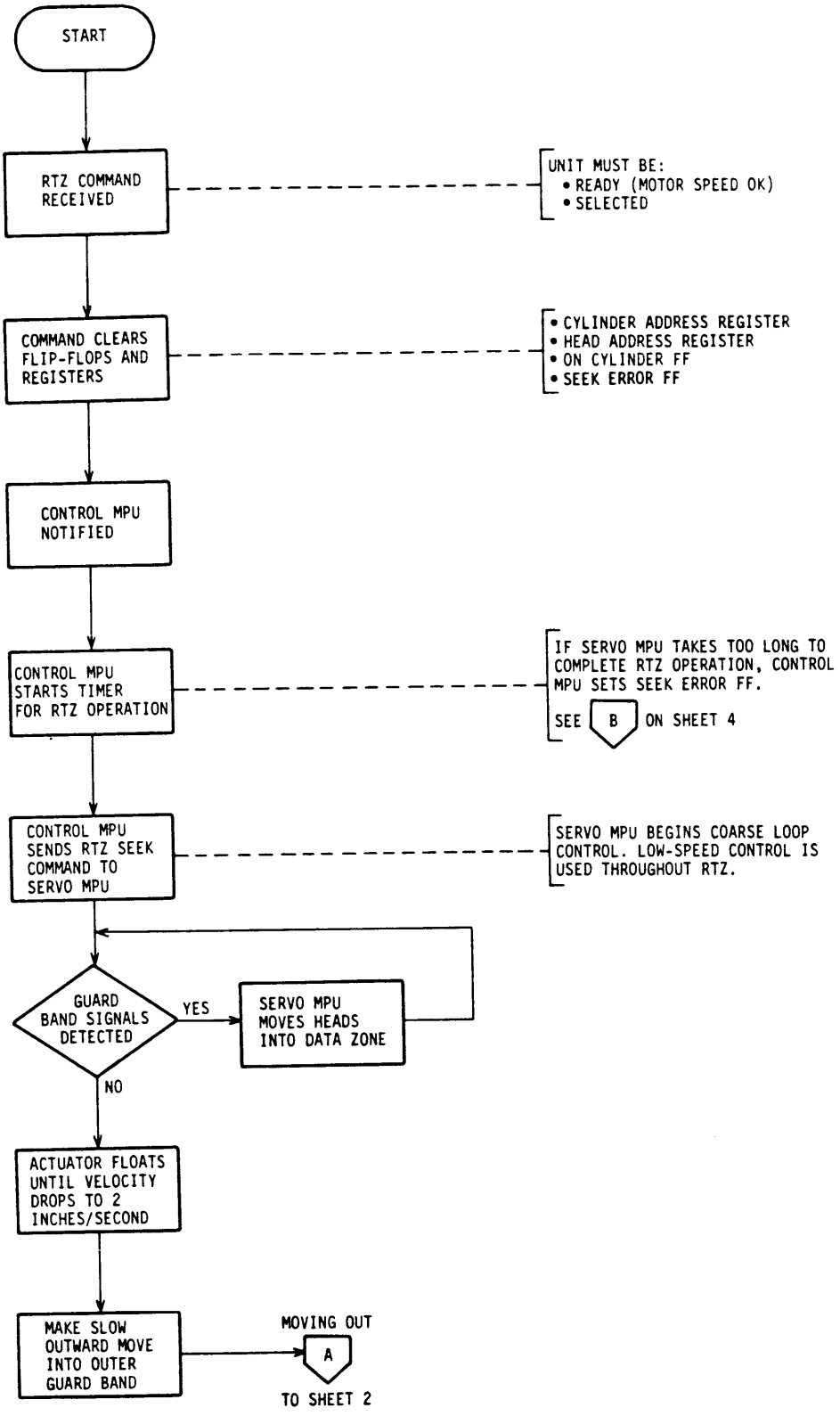


Figure 5-16. Return to Zero (RTZ) Seek (Sheet 1 of 4)

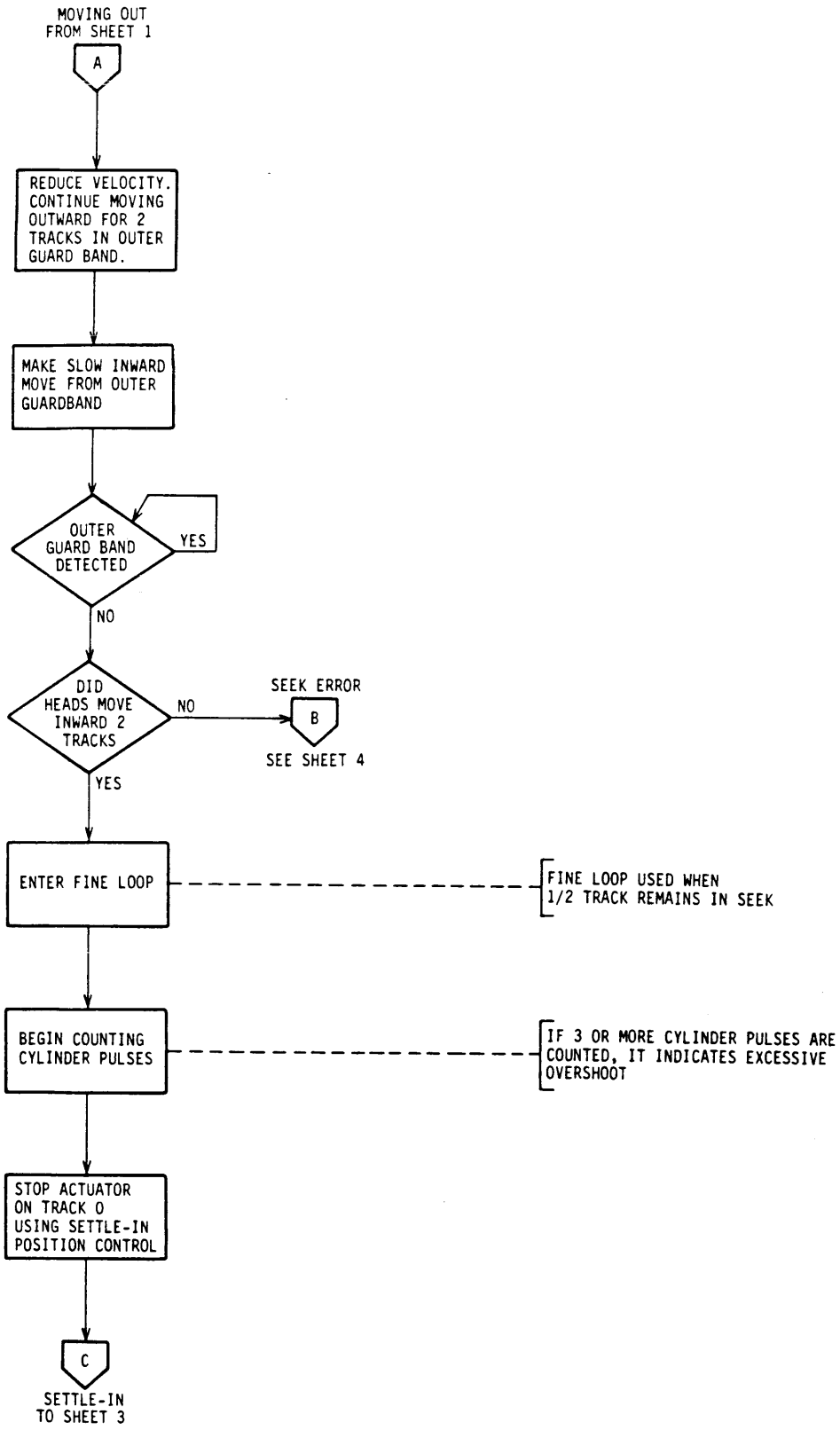


Figure 5-16. Return to Zero (RTZ) Seek (Sheet 2)

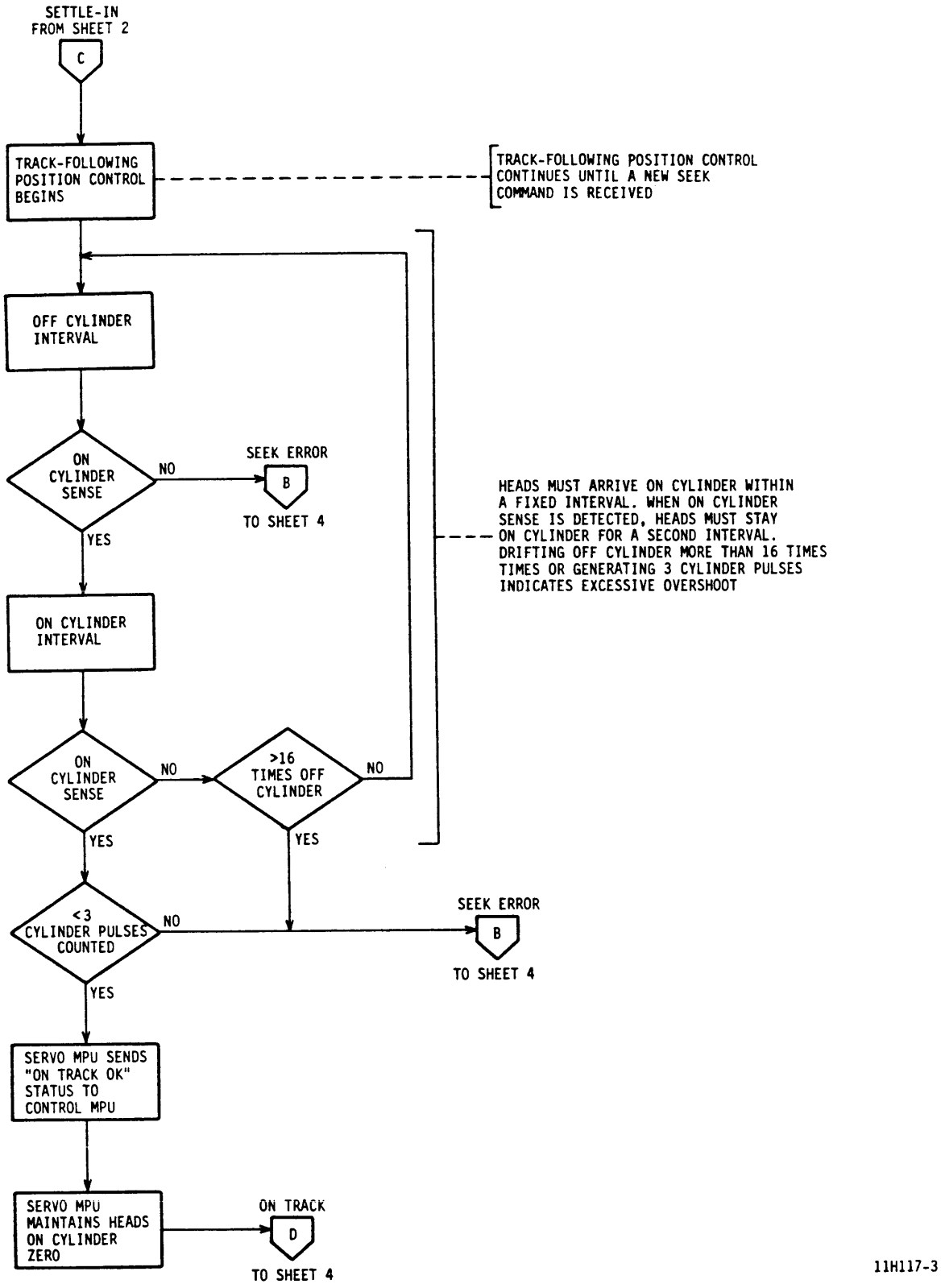


Figure 5-16. Return To Zero (RTZ) Seek (Sheet 3)

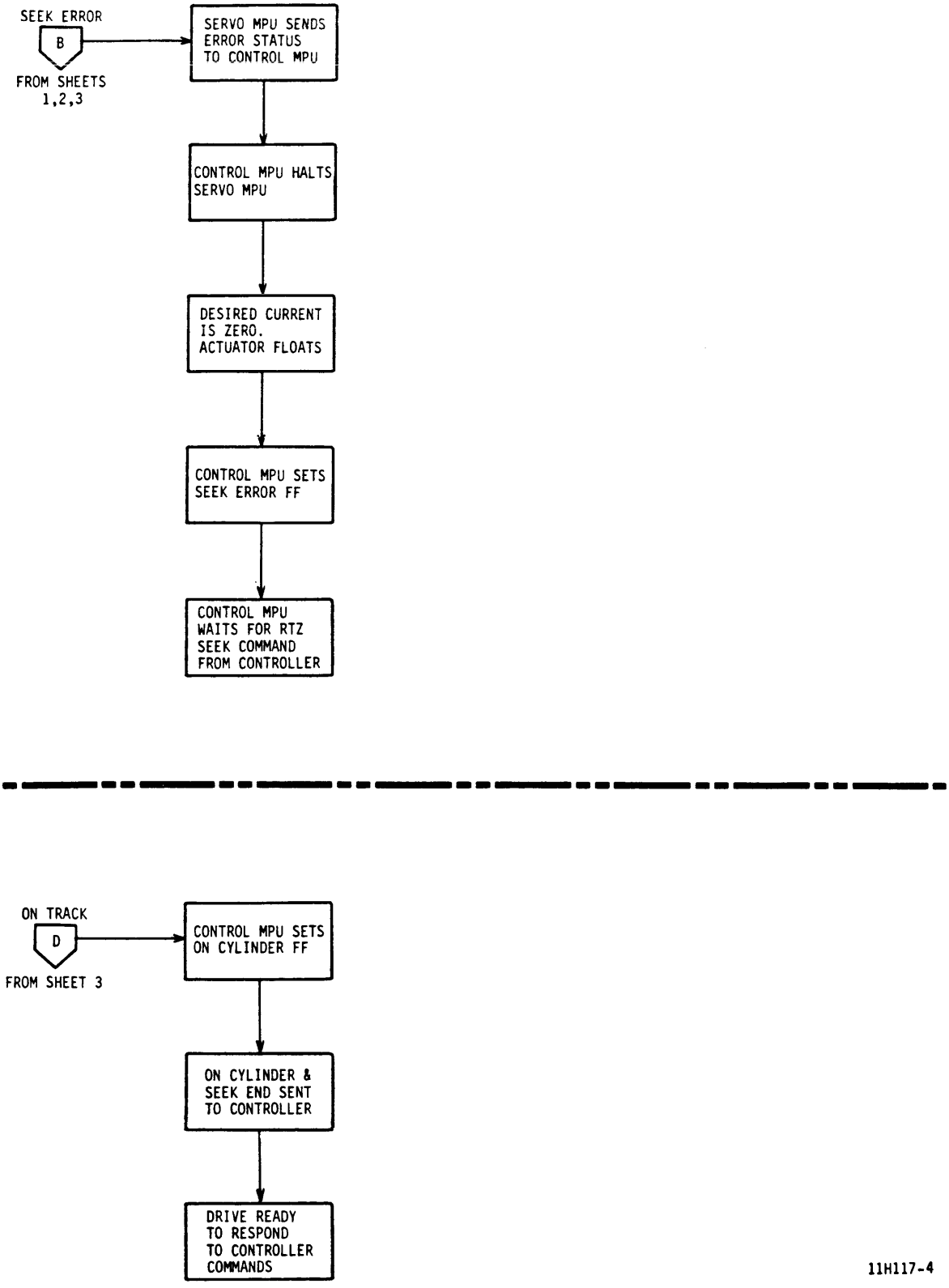


Figure 5-16. Return To Zero (RTZ) Seek (Sheet 4)

In these cases, the Control MPU sets the Seek Error FF in the I/O circuitry. With this FF set, Seek Error status and Seek End status are available to the controller. As a maintenance aid, the Control MPU displays a status code on the status/control panel. These codes, discussed in the maintenance manual, indicate where the RTZ operation failed.

If the RTZ operation was successful, the Control MPU sets the On Cylinder FF in the I/O circuitry. With this FF set, On Cylinder and Seek End status are available to the controller.

After sending On Track OK status to the Control MPU, the Servo MPU remains active. The Servo MPU continually makes corrections to the actuator position to keep the heads on cylinder zero. If the Servo MPU fails to maintain the heads on cylinder, it sends error status to the Control MPU. For more details refer to the next topic.

TRACK FOLLOWING

Following successful load, normal seek, or RTZ operations, the Servo MPU monitors on cylinder status and repositions the actuator if it drifts off cylinder. Throughout track following the Servo MPU periodically samples the position signal, computes a position error and desired current, and outputs desired current to the power amplifier.

If the actuator fails to stay on cylinder, the Servo MPU reports error status to the Control MPU. The Control MPU then halts the Servo MPU, cutting off current to the actuator. The Control MPU sets the Seek Error FF, clears the On Cylinder FF, and waits for an RTZ command from the controller.

UNLOAD OPERATION

The Control MPU uses the unload operation during the power off sequence to move the heads completely inward until they are located over the landing zone. The Control MPU initiates the unload sequence when it detects a loss of start conditions or a loss of motor speed. A loss of start conditions occurs when the START switch is pressed on units with an operator panel. As discussed under Power Sequencing in section 2, the controller can also remove start conditions on some drives.

Sensing a loss of start conditions or a loss of motor speed, the Control MPU clears the Unit Ready FF in the I/O circuitry, and then issues a Retract command to the Servo MPU. The Servo MPU generates a desired current level to move the heads slowly inward to the landing zone. After a delay, the Servo MPU checks the Demodulator Active signal to verify that the heads are over the landing zone. The Servo MPU then sends status to the Control MPU.

If the demodulator is inactive, the Control MPU deenergizes the carriage latch electromagnet and halts the Servo MPU. Stopping the Servo MPU causes desired current to drop to zero. If the demodulator is still active after the first delay, the Control MPU attempts a retract operation by making the Retract signal active and the Power Amp Enable signal inactive. After a second delay, the Control MPU looks for demodulator inactive. When the demodulator goes inactive, the Control MPU deenergizes the carriage latch electromagnet, and makes the Retract signal inactive to shut off retract current to the coil.

The Control MPU then drops the Motor Run line and continues to monitor the Motor Status 0-2 lines to determine when the motor has stopped rotating.

SWEEP CYCLE

The sweep cycle is a feature that periodically moves the heads to different locations on the disks during intervals when the drive is idle. Using the sweep cycle enhances drive reliability. We encourage you either to enable the drive sweep cycle or to use a sweep cycle driven at the system or subsystem level.

The drive is preset during manufacturing with a set of sweep cycle options selected. Three jumpers on the control board select the following options:

1. Enable or disable the sweep cycle function.

2. Enable or disable the option to sweep only on seeks.

3. Enable or disable the option to return the heads to their original cylinder following a sweep segment.

If the first option is disabled, the drive never performs sweep cycles, and the other two options are ignored.

If the second option is enabled, sweep movements can occur only in conjunction with seeks required by the controller. Each time the drive performs a sweep cycle, it starts a 12-minute timeout. When the timeout has elapsed, the drive performs

another sweep cycle only when it receives a Seek command. When combining a sweep cycle with a seek, the drive performs the sweep cycle first and then executes the Seek command.

If the third option is enabled, the drive performs the sweep and returns to the original cylinder (where it was before the sweep occurred) with the following exceptions:

- If the sweep was initiated by a Seek command, the drive performs the sweep function and then moves the heads to the cylinder requested by the controller.

- If the drive had not been selected during the 12 minutes prior to a sweep, the heads stay on a cylinder accessed during the sweep segment. Later, when the drive is reselected, the heads return to the original cylinder.

If the third option is disabled, the heads always stay on a cylinder accessed during the sweep segment and On Cylinder status remains inactive with the following exception: If the sweep was initiated by a Seek command, the drive performs the sweep function and then moves the heads to the cylinder requested by the controller.

Figure 5-17 shows a profile (not to scale) of typical sweep activity for the case where sweeps can be initiated within the drive (option 2 disabled) and the heads return to their original position following a sweep segment (option 3 enabled).

The picture shows how each sweep segment consists of a series of short seeks followed by a longer seek to the maximum data cylinder. During a sweep segment, the heads remain for one disk rotation on each track accessed. In addition to the sweep segments, the picture shows two controller-requested seeks. Prior to issuing the first seek command, the controller reselects the drive; at this time, the heads return to the original cylinder. A sweep segment occurs in conjunction with the second seek requested by the controller.

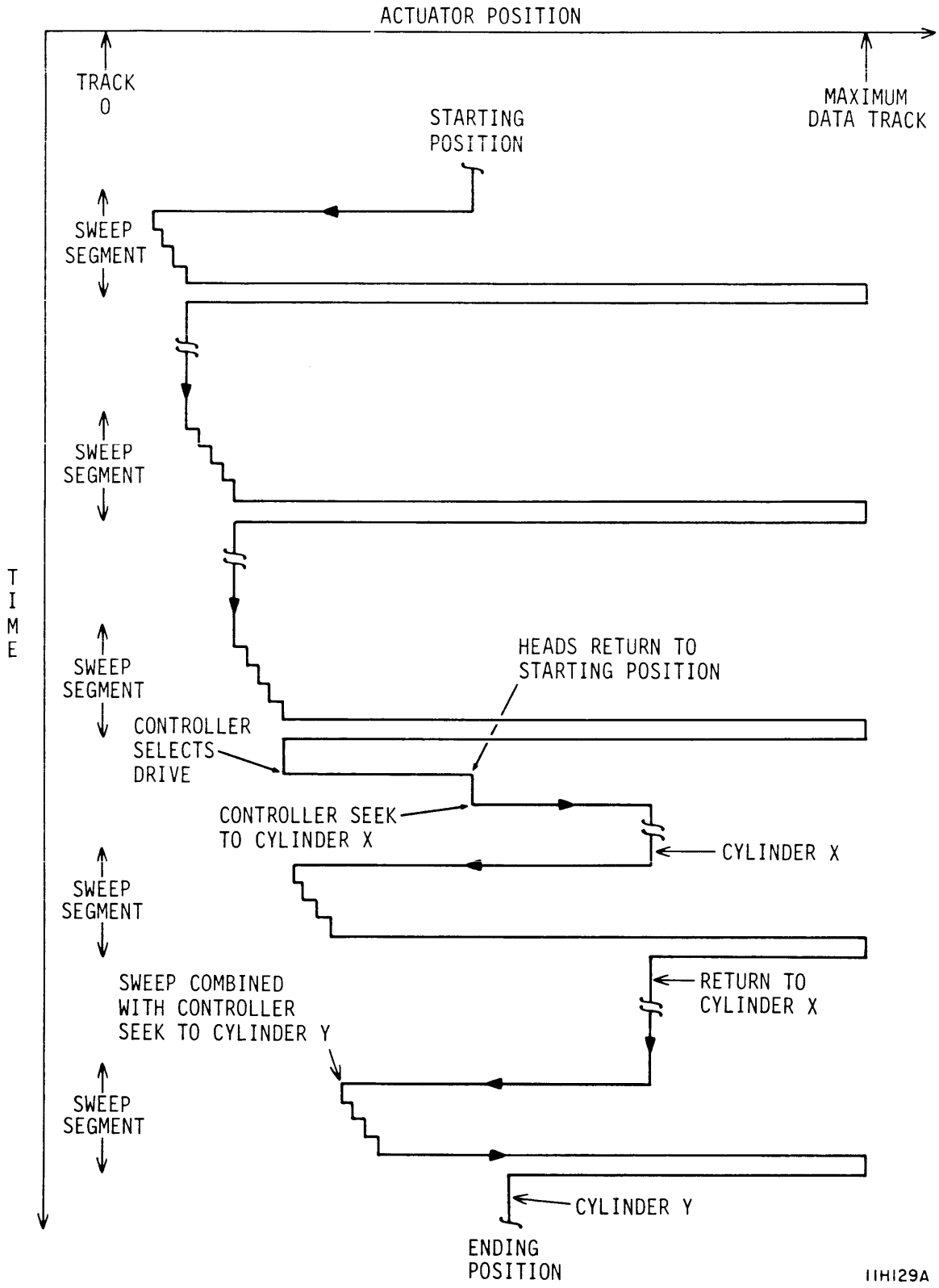


Figure 5-17. Typical Sweep Cycle Activity

SECTION 6

READ/WRITE FUNCTIONS

READ/WRITE FUNCTIONS 6

INTRODUCTION

When the drive is on cylinder, it is ready to select a head and perform a read or write operation. The controller issues one command to select a head and another command to initiate a read or write operation. During a write operation, the drive receives data from the controller and writes it on the disk. During a read operation, the drive recovers data from the disk and transfers it to the controller.

This section provides a general description of the read/write circuits. It is divided into the following areas:

- Read/Write Overview -- Defines standard and parallel read/write circuits, and lists the signal frequencies present in the circuits.
- Basic Read/Write Principles -- Explains the principles of recording and recovering data from a magnetic disk.

Specific information about read/write circuit operation is presented in subsections 6A and 6B.

READ/WRITE OVERVIEW

Drives with standard read/write electronics and drives with parallel read/write electronics differ in the number of heads used simultaneously.

In the standard version, one read/write head is selected at a time, and that head is used to record data on a disk or read data from a disk. Figure 6-1 is a basic block diagram of a standard read/write channel. Section 6A describes head selection, write circuits, and read circuits for the standard version.

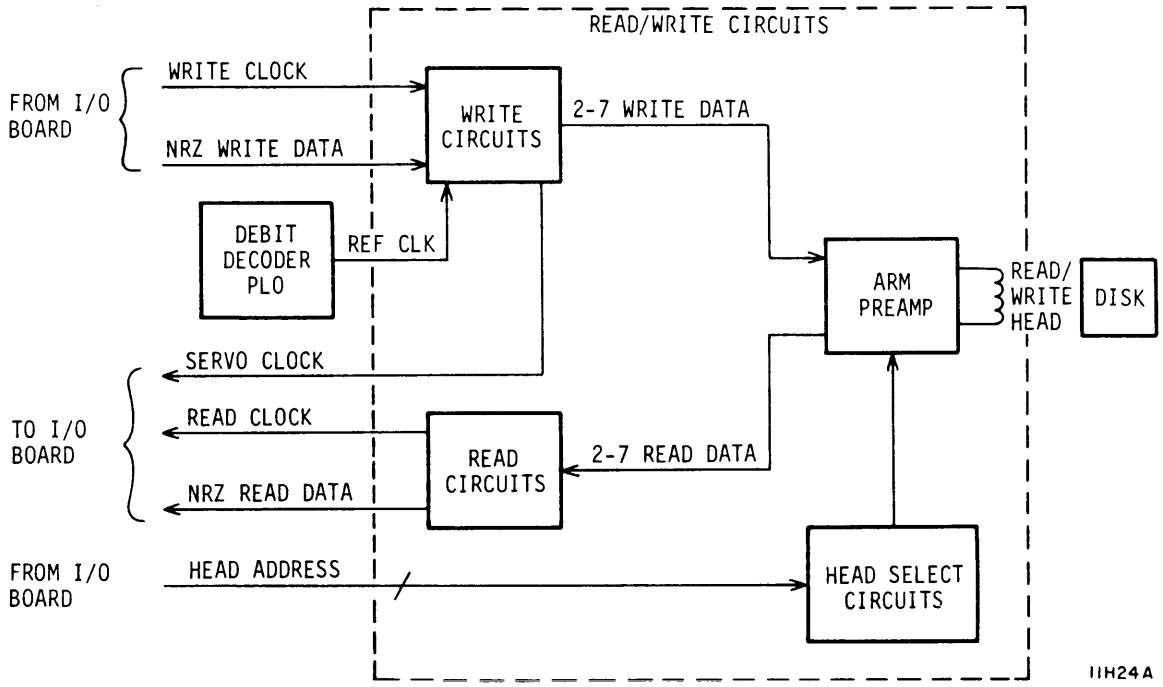


Figure 6-1. Standard Read/Write Circuits

In the parallel version, two read/write heads are selected at a time, and those heads are used to record data on disks or read data from disks. Figure 6-2 is a basic block diagram of two parallel read/write channels. Section 6B describes head selection, write circuits, and read circuits for the parallel version.

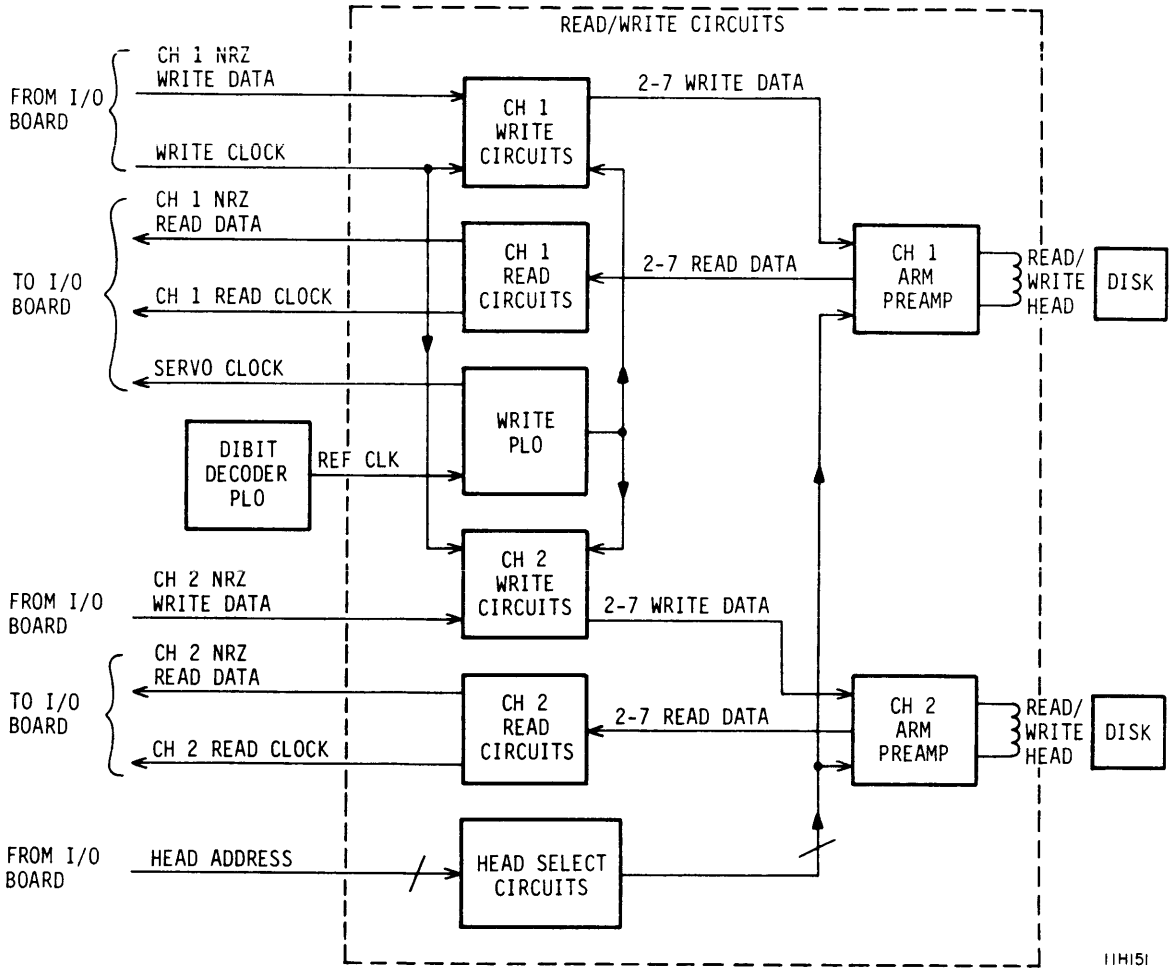


Figure 6-2. Parallel Read/Write Circuits

The discussion of read/write functions makes references to signal frequencies in relation to the transfer rate (1F) of the drive. Table 6-1 shows these frequency relationships for the the various drives described in this manual.

TABLE 6-1. SYMBOLS FOR READ/WRITE FREQUENCIES

Symbol	Read/Write Frequencies (MHz)			
	736 MB Drives	850 MB Drives	1120 MB Drives	1153 MB Drives 1230 MB Drives
REF	2.41	3.28	3.67	4.03
0.5F	7.25	9.86	10.99	12.10
1F	14.52	19.72	21.98	24.20
2F	29.04	39.44	43.96	48.40

BASIC READ/WRITE PRINCIPLES

HOW THE HEADS READ AND WRITE

Heads are magnetic devices that record data on, and read data from, the disk surface. Each read/write head has a coil wound on its core. This coil interfaces to the read/write circuitry via a preamplifier mounted on the head-arm. Selecting a head enables an arm preamplifier. The enabled arm preamplifier provides current switching for the head in write operations or amplification of voltage induced in the head in read operations. Refer to Write Circuits and Read Circuits in section 6A for details about the arm preamplifier.

During write operations, the read/write head develops a changing flux pattern on the disk surface passing beneath it. The arm preamplifier supplies the selected head with a source of write current. At each transition of the write data signal, the preamplifier reverses the current in the head coil. This switching reverses the flux across the gap in the head (see figure 6-3). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a north pole and a south pole. The writing process orients the poles to store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of write

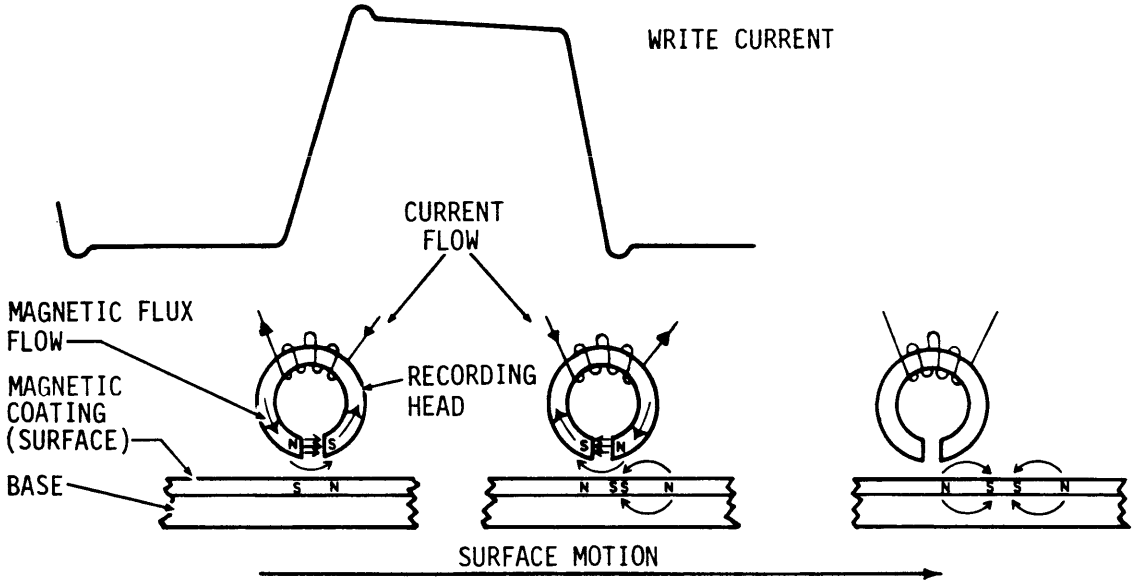
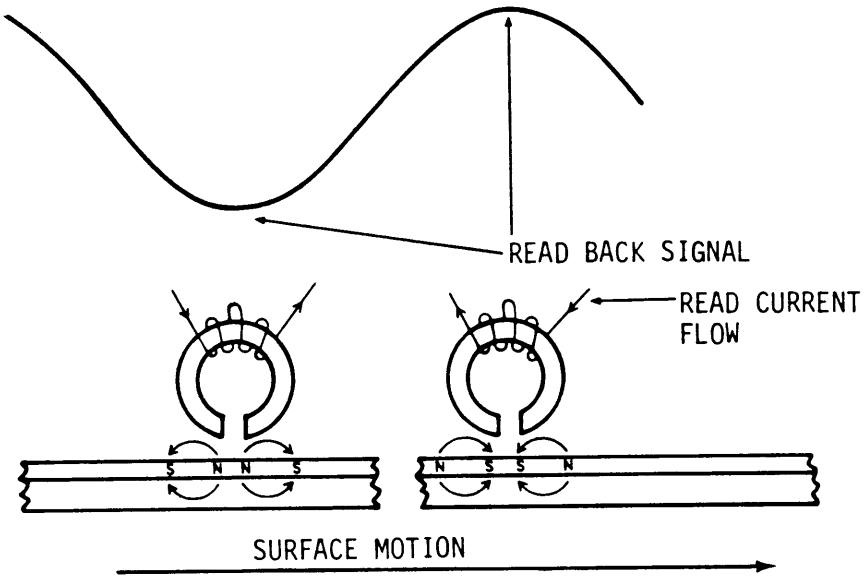


Figure 6-3. Writing Data

current switching while its amplitude depends on the amount of current (the greater the current, the more oxide particles that are affected).

Information (data) is written by switching the current through the head. Switching this current reverses the direction of the flux field across the gap. The flux change defines a data bit. New data is written simply by writing over any data which may already be on the disk.

During a read operation, disk motion beneath the head causes the stored flux to induce a voltage in the heads (refer to figure 6-4). This voltage is analyzed by the Read circuit to define the data recorded on the disk. Each flux reversal (produced while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.



NOTE: RELATIVE HEAD TO SURFACE MOTION, REPRODUCING (READ OPERATION)

11D190

Figure 6-4. Reading Data

PRINCIPLES OF 2-7 RECORDING

The drive employs two modulation schemes for read/write data transfers. The controller transfers data on the interface with Non Return to Zero (NRZ) modulation in a write or read operation. Transfers between the read/write circuitry and the disk use 2-7 modulation. During a write operation, write circuitry decodes the incoming NRZ modulated data and converts it into 2-7 modulated data for storage on the disk surface. In a read operation, read circuitry in the drive decodes the 2-7 read data to create NRZ data which is suitable for the controller. The following paragraphs define both modulation schemes and then explain why 2-7 modulation is used in the drive.

NRZ data is transferred at a nominal 1F rate. The interval between consecutive 1F clock cycles is called a bit cell. Each data bit is defined throughout a bit cell. For consecutive cells indicating binary 1, the read or write interface line stays active. For consecutive cells indicating binary 0, the read or write interface line stays inactive. Thus, NRZ data lines return to zero only when the transferred data changes from binary 1 to binary 0.

For disk transfers, the 2-7 scheme is superior to the NRZ scheme in two ways. First, it reduces the maximum rate of flux reversals on the disk; this permits greater recording density on the disk. Second, the recording bandwidth, or frequency range of the read/write signals, is limited; this improves the signal-to-noise ratio.

The translation between NRZ modulation and 2-7 modulation is a translation of seven basic code words, as shown in table 6-2. Any string of NRZ data can be expressed as a series of these individual code words. The corresponding 2-7 data string is a series of translated code words where each 2-7 code word has replaced its corresponding NRZ word. So, the write circuitry encodes the NRZ data as 2-7 data, and the read circuitry decodes the 2-7 data as NRZ data. Figure 6-5 shows the encoding process for a series of three code words; the decoding process is the reverse of what is shown in the picture.

Each 2-7 code word has twice as many bits as its related NRZ code word. Therefore, the 2-7 bit cell is half as long as the NRZ bit cell. As the 2-7 data is written on the disk, the head changes its flux each time the code contains a binary 1. Although 2-7 uses twice the bit rate of NRZ, binary ones appear in 2-7 code less frequently than level changes occur in the corresponding NRZ code. Therefore, use of 2-7 code allows data to be written more densely on the disk.

The name 2-7 derives from the fact that preceding and following each occurrence of binary 1 in the code, there are at least two zeros and as many as seven zeros.

TABLE 6-2. TRANSLATION BETWEEN NRZ AND 2-7 CODES

NRZ Code Words	2-7 Code Words
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

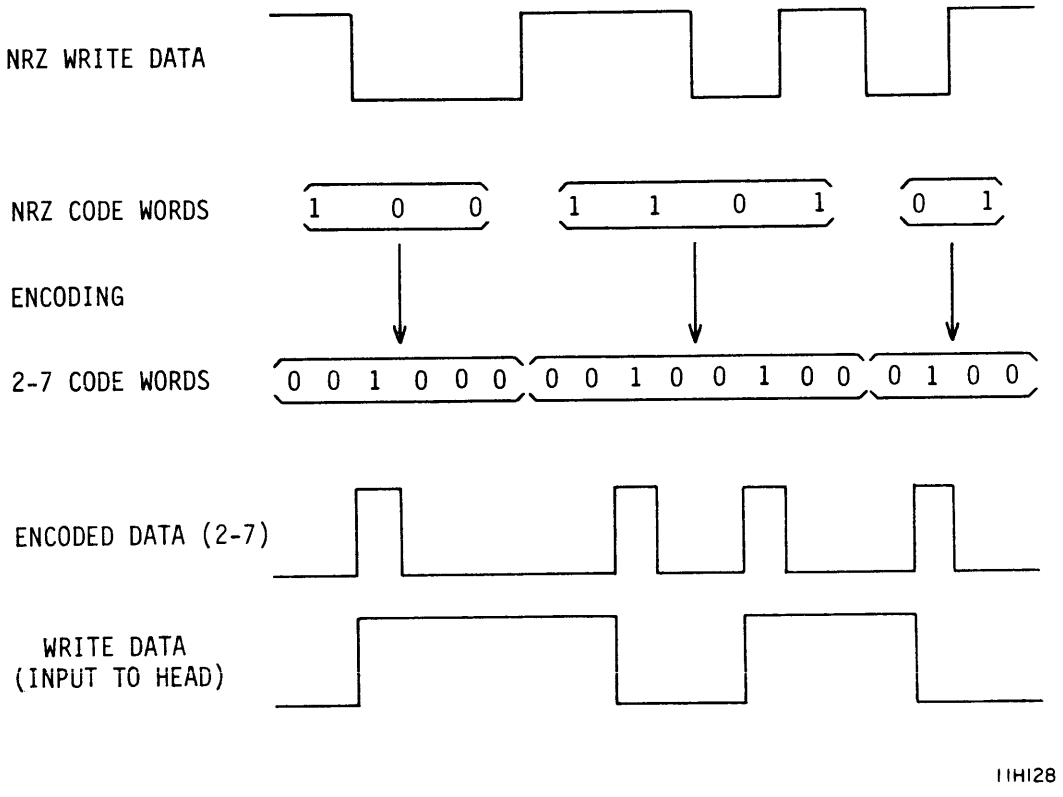


Figure 6-5. Converting from NRZ to 2-7 Data

SECTION 6A

STANDARD READ/WRITE FUNCTIONS

STANDARD READ/WRITE FUNCTIONS 6A

INTRODUCTION

This section describes read/write functions for a drive that has a single read/write channel and selects only one head at a time. When the drive is on cylinder, it is ready to select a head and perform a read or write operation. The controller issues one command to select a head and another command to initiate a read or write operation.

During a write operation, the drive receives data from the controller and writes it on the disk. During a read operation, the drive recovers data from the disk and transfers it to the controller. The principles of recording and recovering data from a magnetic disk are discussed in section 6 under Basic Read/Write Principles.

The description of the read/write circuits is divided into the following areas:

- Head Selection -- Describes the circuitry used for head selection and the arrangement of read/write heads in the module.
- Write Circuits -- Describes the circuits used by the drive to record data on the disk.
- Read Circuits -- Describes the circuits used by the drive to recover data from the disk.

The discussion of read/write functions makes references to signal frequencies in relation to the transfer rate (1F) of the drive. The signal frequencies are defined in table 6-1 near the beginning of section 6.

HEAD SELECTION

A head must be selected before a read or write operation can be performed. Under Servo MPU control, the servo system moves the heads to the cylinder specified by the controller. By selecting a head, the controller specifies a particular track within that cylinder. As part of a Head Select command, the controller indicates the new head address.

The drive has one read/write head for each data recording surface in the disk module: 15 recording surfaces and 15 read/write heads as shown in figure 6A-1. In addition, the drive has one servo head. The servo head continuously reads prerecorded data from the servo disk surface for use by the drive servo circuits.

Read/write information is transferred to and from the heads through cables connected to a preamplifier mounted on the arm. The preamplifiers connect to the read/write circuitry via the arm matrix board, located inside the sealed module.

The Head Select command gates the address into the Head Address register (HAR) located on the I/O board. Figure 6A-2 shows the head selection circuits.

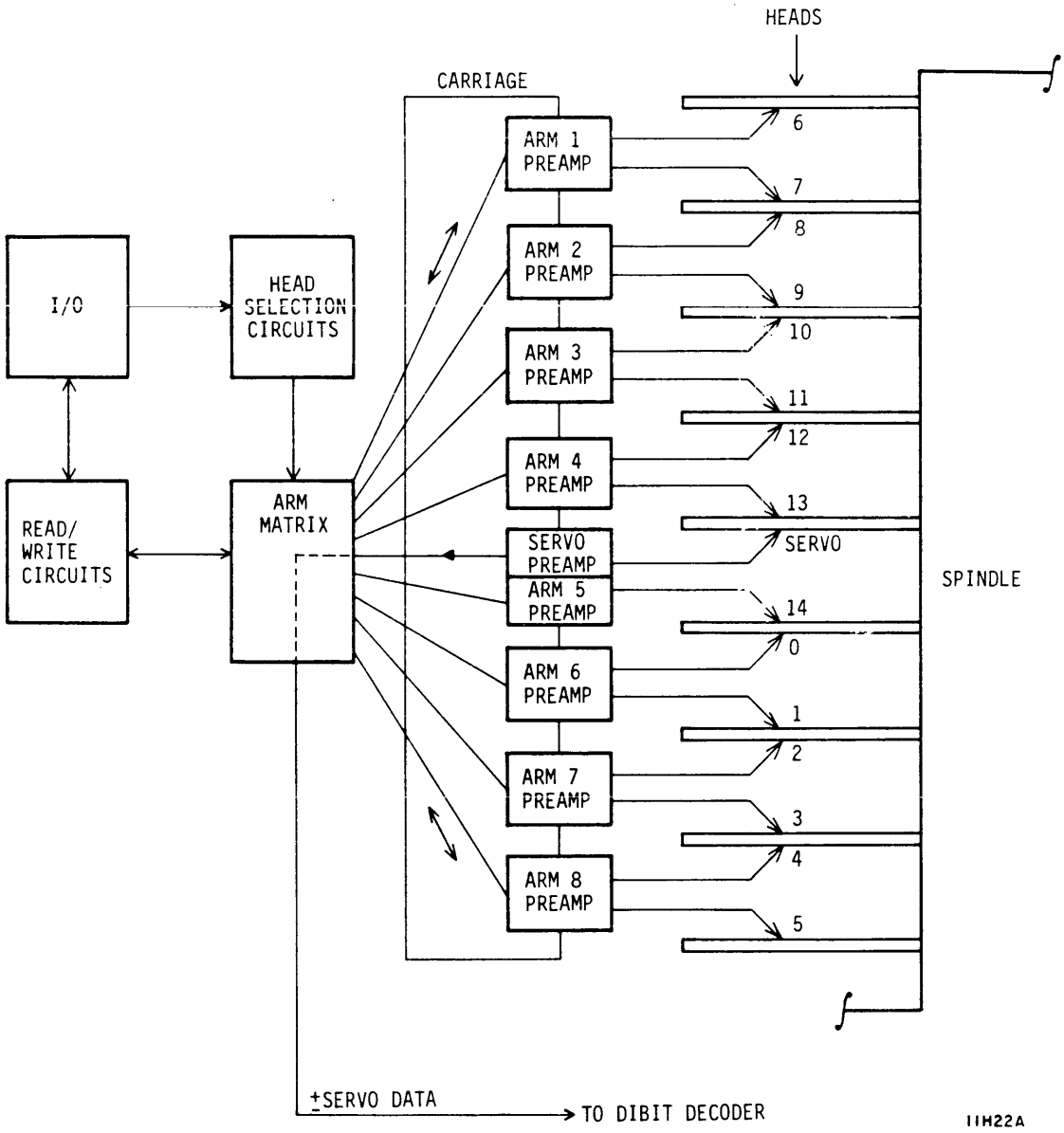


Figure 6A-1. Read/Write Heads

The Head Address lines go from the I/O board to the control board where they address a ROM. Depending on its addressing, the ROM activates one of its output lines, Arm Select 1-8, to enable one arm preamplifier. The enabled arm preamplifier in turn selects the head on its head-arm in response to the Head Select 1 line. This line is activated by Head Address line 0. The Arm Select, Head Select, and common control lines for the preamplifiers are routed through the arm matrix board (inside the module) to the individual arm preamplifiers.

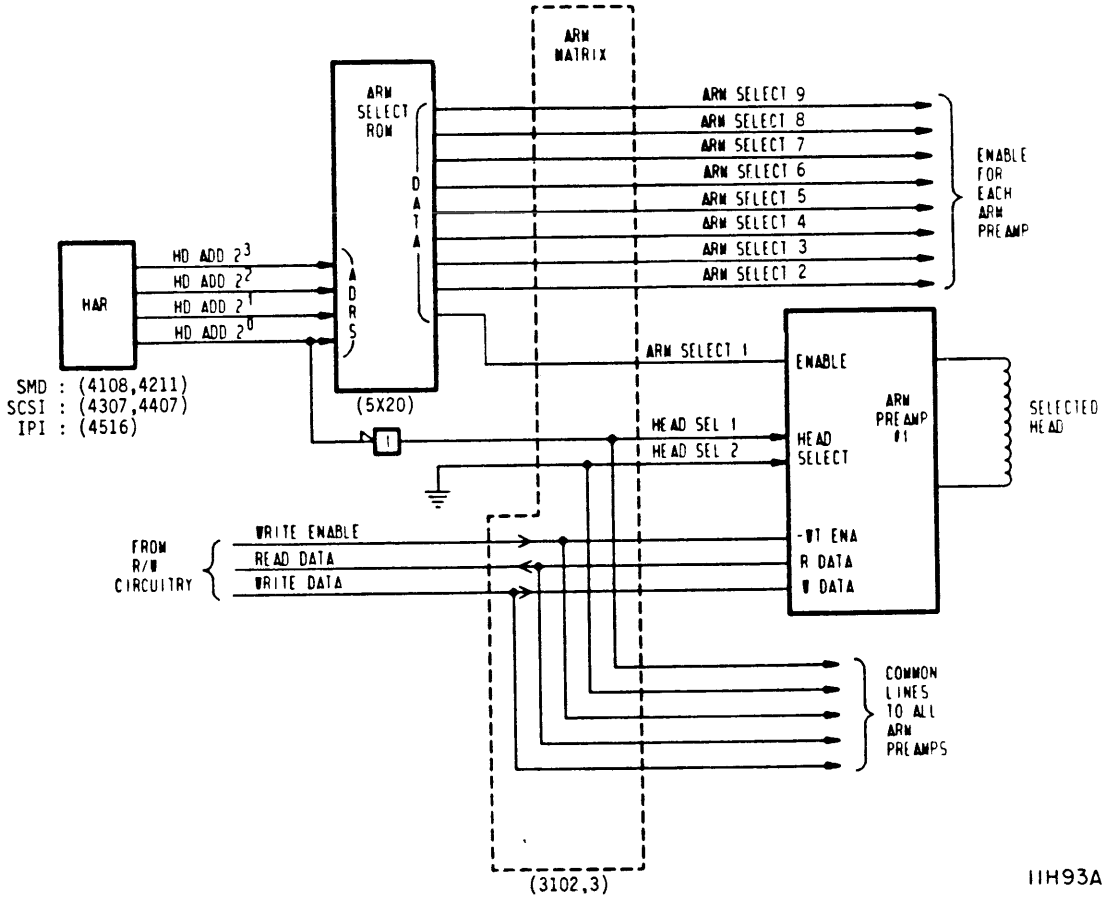


Figure 6A-2. Head Selection Circuits

If an illegal head address (greater than 14) is received, no head is selected. A Write Fault occurs if the drive attempts to write data with no head selected. Table 6A-1 shows the combination of address lines that selects each head.

TABLE 6A-1. HEAD SELECT ADDRESSING

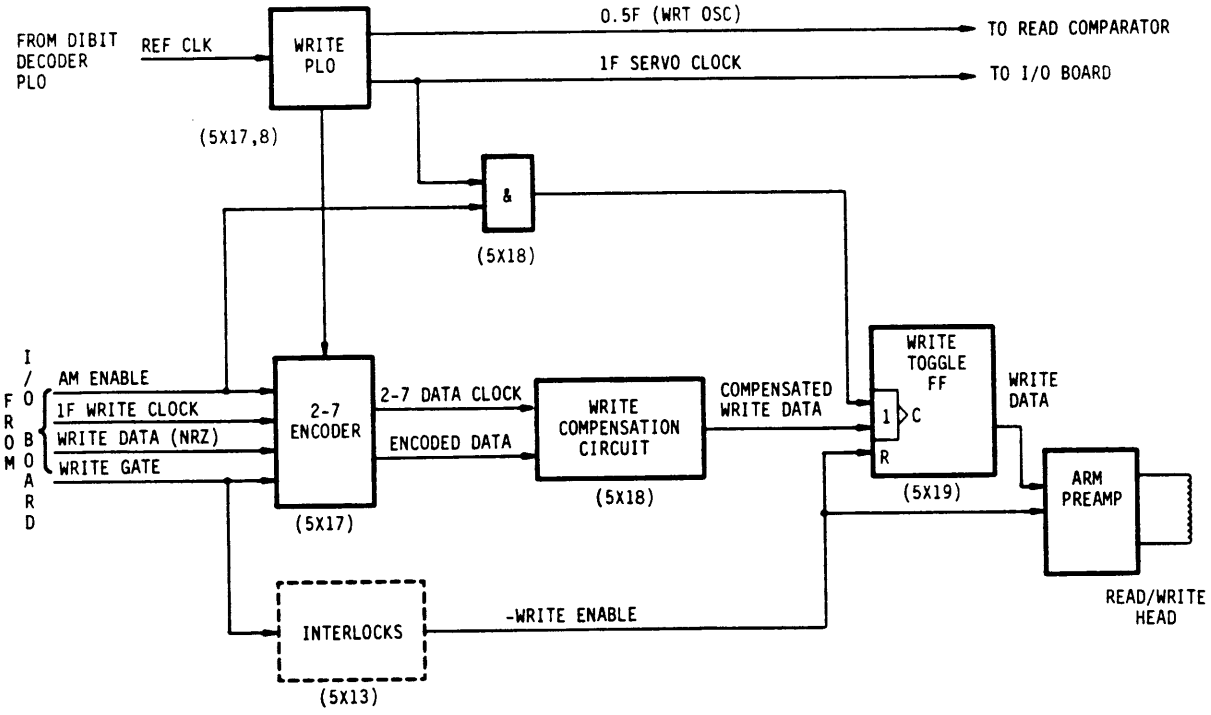
Head Selected	Arm Selected	Head Address Lines			
		0	1	2	3
0	6	0	0	0	0
1	6	1	0	0	0
2	7	0	1	0	0
3	7	1	1	0	0
4	8	0	0	1	0
5	8	1	0	1	0
6	1	0	1	1	0
7	1	1	1	1	0
8	2	0	0	0	1
9	2	1	0	0	1
10	3	0	1	0	1
11	3	1	1	0	1
12	4	0	0	1	1
13	4	1	0	1	1
14	5	0	1	1	1

WRITE CIRCUITS

GENERAL

The write circuits process data from the I/O board, making it suitable for transfer to the disks. The Write Gate signal allows the drive to start processing serial NRZ data received from the controller. NRZ data is synchronized to the 1F Servo Clock derived from the Write PLO. The Write Data is received via the Write Data line and is first sent to the 2-7 encoder circuit. This circuit converts the data to 2-7 modulation and sends it to the write compensation circuit. Write compensation modifies the data timing, and the compensated data is then processed by the Write Toggle FF. The Write Toggle FF provides the data signal that controls current switching in the selected arm preamplifier.

Figure 6A-3 shows the write circuits and table 6A-2 briefly explains their function.



11H25B

Figure 6A-3. Write Circuits Block Diagram

TABLE 6A-2. WRITE CIRCUIT FUNCTIONS

Circuit	Function
Write PLO	Generates the 2F Write Clock which is divided by two to develop the 1F Servo Clock.
2-7 Encoder	Converts the NRZ data from the controller to 2-7 data.
Write Compensation Circuit	Compensates the data for problems caused by peak shift.
Write Toggle FF	Produces a write signal that changes polarity each time the compensated 2-7 data goes to a binary 1.
Arm Preamplifier	Switches the write current in the head coil as the signal from the Write Toggle FF changes polarity.

WRITE PLO

The Write PLO circuitry uses a phase-locked loop to generate the 2F Write Clock. As shown in figure 6A-4, this circuitry consists of frequency dividers, a coincidence comparator, a charge pump, and a voltage-controlled oscillator (VCO). The frequency dividers and coincidence comparator are located in the Write Compensation and PLO ECL Logic Array.

The phase-locked loop uses a clock signal from the Dibit Decoder PLO as a frequency reference (refer to Servo PLO and Timing Logic in section 4). This frequency is listed under REF in table 6-1. The Write VCO operates under loop control to generate the 2F Write Clock, at twelve times the frequency of the reference clock. Two divisions by two and one division by three of the VCO output develop a feedback signal that can be compared to the reference clock to adjust the loop operation.

The loop reaches phase lock by comparing the coincidence of the leading edges of the reference and feedback clocks. Each time the feedback clock leads the reference clock, the coincidence comparator pulses the Pump Down line. Pump Down pulses cause the charge pump to vary the Control Voltage signal as necessary

to reduce the Write VCO frequency until the reference and feedback clocks are coincident (phase-locked). Each time the feedback clock lags the reference clock, the coincidence comparator pulses the Pump Up line. Pump Up pulses cause the charge pump to vary the Control Voltage signal as necessary to increase the Write VCO frequency until phase lock occurs.

The Write PLO circuit operates continuously whenever the servo signal is being decoded. The PLO provides the following outputs to other circuits:

- 2F Write Oscillator signal to the 2-7 Encoder circuit.
- 1F Servo Clock to the controller (via the interface). This is returned to the drive as Write Clock.
- 0.5F clock to the Read Comparator circuit.

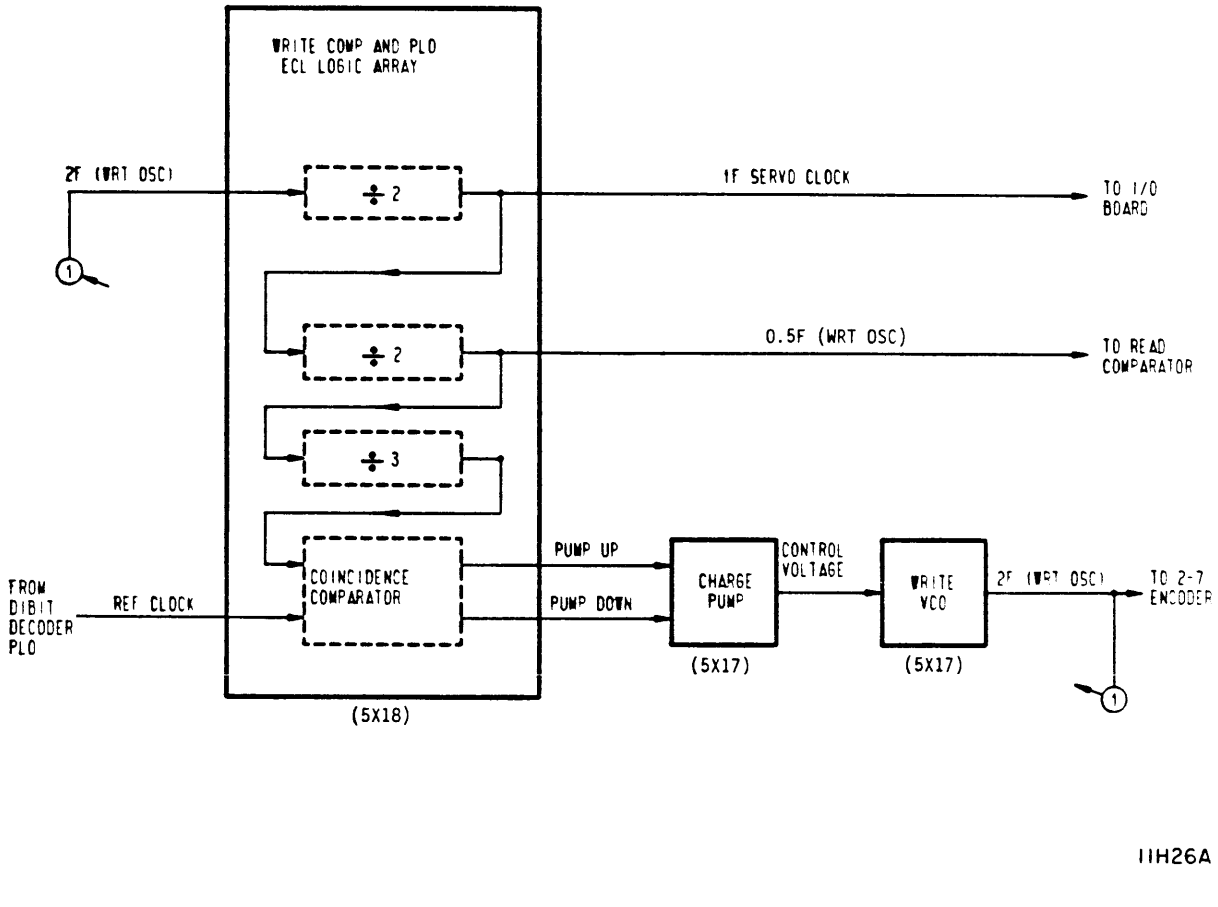
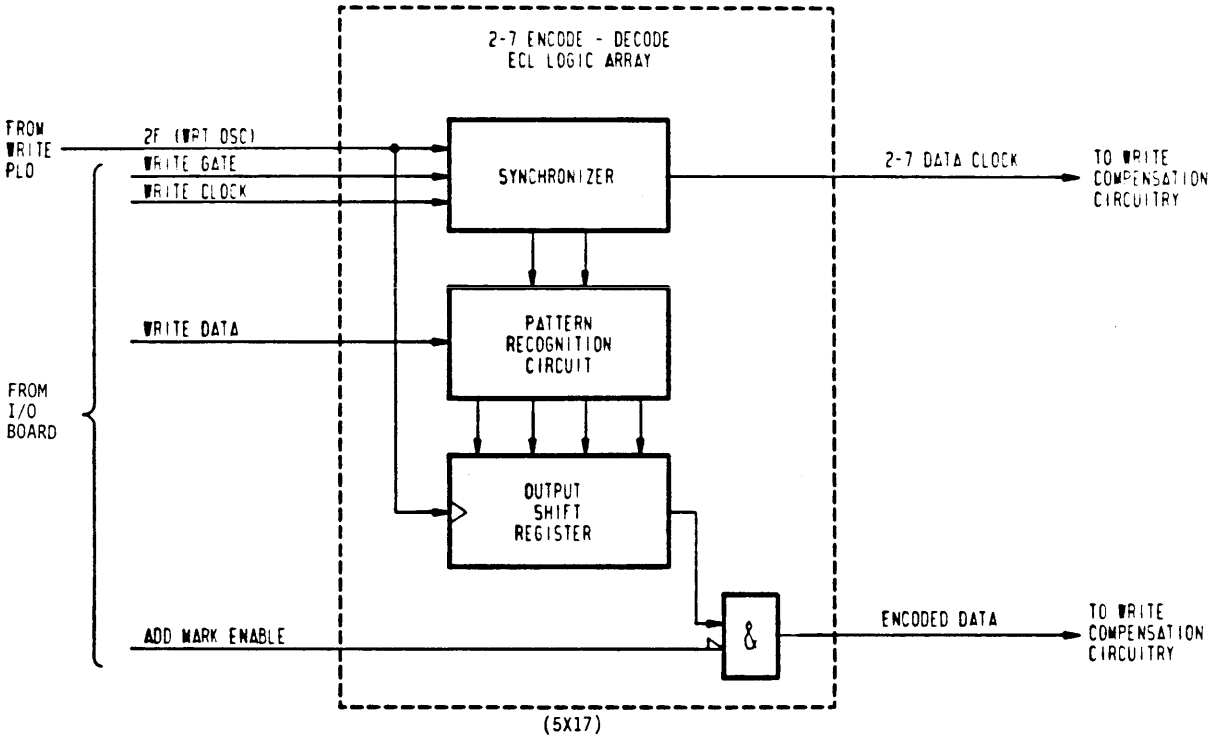


Figure 6A-4. Write PLO Block Diagram

2-7 ENCODER

The 2-7 Encoder converts NRZ data into 2-7 data. As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven NRZ code words and seven 2-7 code words. The encoder recognizes the coding in the write data string as a succession of the seven NRZ words, and outputs a series of 2-7 code words, each one translated from its NRZ equivalent. Table 6-2, presented under Basic Read/Write Principles, shows the translation used between the two groups of seven code words. The 2-7 encoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

The encoder uses synchronous timing circuitry controlled by two clock inputs, the 1F Write Clock from the controller and the 2F Clock from the Write PLO (see figure 6A-5). The encoder has a synchronizer that develops two clocks in phase with the 2F Clock -- the 2-7 Data Clock and a 1F internal clock. The 2-7 Data Clock is supplied to the write compensation circuit. The internal clock shifts NRZ data into a pattern recognition circuit. Each time this circuit recognizes one of the seven NRZ code words, it parallel-loads an output shift register and starts looking for the following word.



11H27A

Figure 6A-5. 2-7 Encoder Block Diagram

The output shift register shifts its contents on each rising edge of the 2F Clock. The serial output of the register is the Encoded Data line. This line is active for binary ones and inactive for binary zeros in the 2-7 data.

The encoder begins translating NRZ code words with the second data bit clocked in by Write Clock after Write Gate goes inactive. Encoder operation proceeds continuously, processing all NRZ data except for the last bit received before Write Gate goes inactive.

WRITE COMPENSATION CIRCUIT

The write compensation circuit modifies the timing of transitions in the encoded 2-7 data in a manner that compensates for peak shift. Peak shift changes certain timing intervals in the read data signal. These timing changes are predictable from the spacing of adjacent peaks.

Encoded 2-7 data contains isolated bit cells at binary one preceded and followed by from two to seven bit cells at binary zero. Each time the data changes from binary zero to binary one, the head reverses its flux direction. Write compensation shifts this positive-going edge away from its nominal timing, and this timing change is related to the number of zeros preceding and trailing a binary one in the data pattern.

The write compensation function takes place in the Write Compensation and PLO ECL Logic Array (see figure 6A-6). The delays with which the 2-7 Data Clock enters chip inputs E1-E3, L1-L3, or NOM produce given time shifts for each possible data pattern. The pattern of time shifts is divided into two zones: a zone for the outer tracks and a zone for the inner tracks.

Uncompensated data enters the circuit via the Encoded Data line. This data is clocked into a 9-bit shift register. The delay line develops the clock input by delaying the 2-7 Data Clock. When the center bit of the shift register contains a binary one, the circuit looks at the number of register bits which are zero on each side of the center bit. Depending on the number of leading zeros and trailing zeros, one of the delayed clocks E1-E3, L1-L3, or NOM is applied to an AND gate along with the center bit of the register. Thus, the AND gate sees the center register bit go active, followed by the applied clock going active; with both inputs active, the gate outputs a compensated write data pulse. The positive edge of the compensated data pulse is timed by the clock selected. Note that a majority of the data patterns use the NOM clock and have the nominal delay.

After being write compensated, the data is transmitted to the Write Toggle FF.

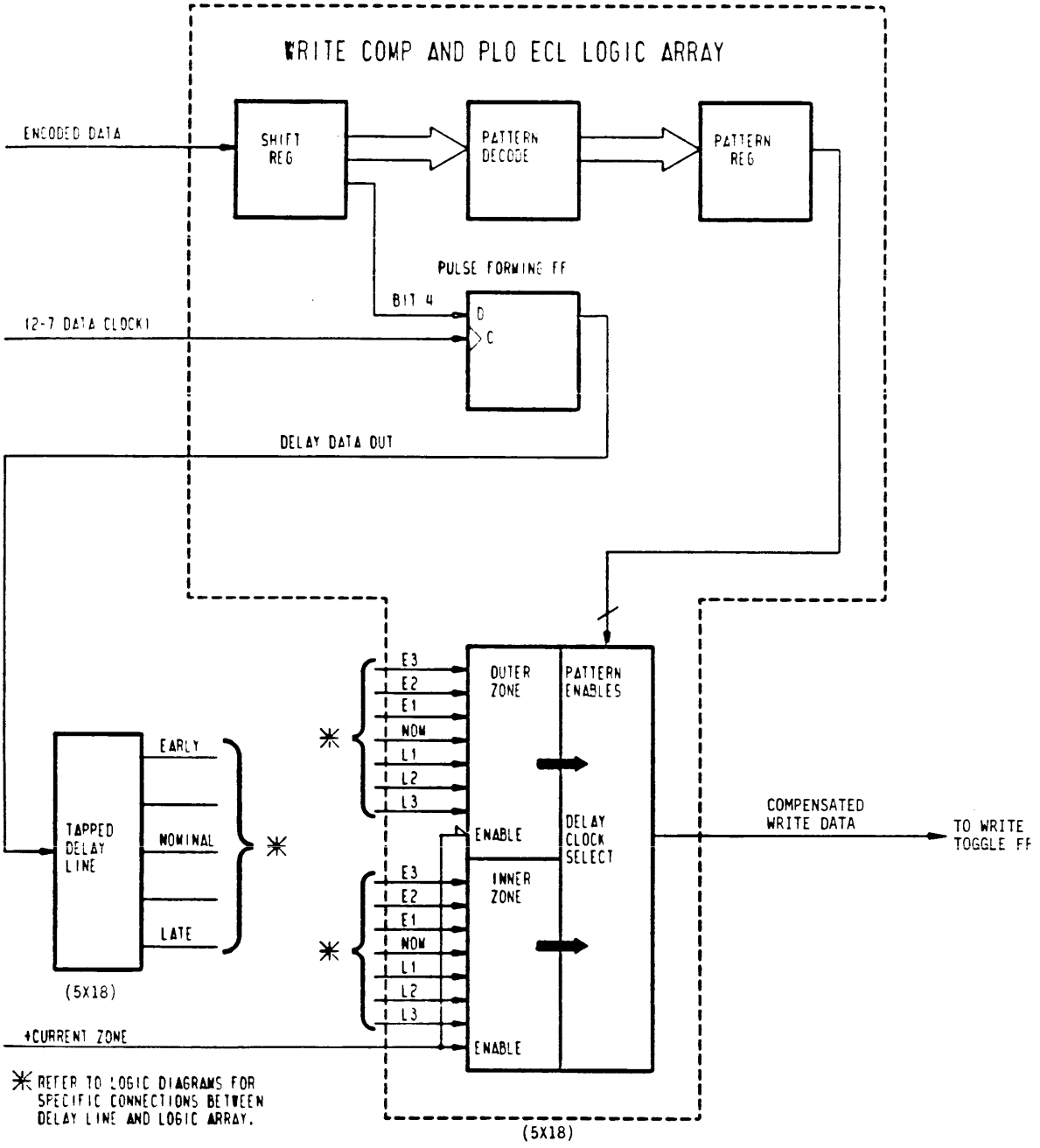


Figure 6A-6. Write Compensation Block Diagram

WRITE TOGGLE FF

The Write Toggle FF generates the Write Data signal that drives the arm preamplifier. As shown in figure 6A-7, the Write Toggle FF has two clock inputs. For normal write operations, compensated write data is applied to one of the clock inputs. When an address mark is being written, a 1F clock signal is gated (by the Address Mark Enable signal) to the other clock input. In either case, the FF changes state with each positive edge at its clock input.

The Write Toggle FF operates only when the Write Enable line is active. With Write Enable inactive, the latch remains cleared, and the Write Data lines to the arm preamplifier do not toggle. The Interlocks circuit activates the Write Enable line only when all of the following are true:

- Write Gate is active
- Write Protect is not active
- No faults exist
- Speed OK is active
- Power Amp Enable signal is active

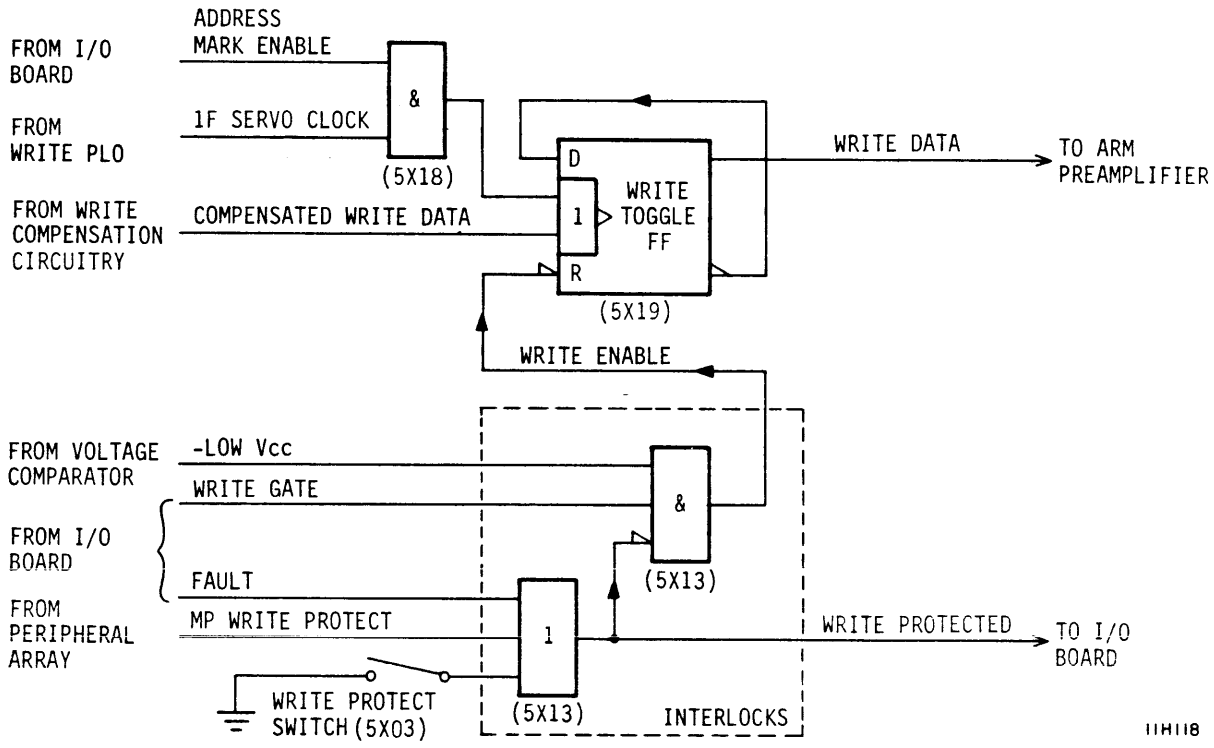


Figure 6A-7. Write Toggle FF and Interlocks

ARM PREAMPLIFIER

Each head-arm contains an LSI chip that serves as a preamplifier for the heads attached to that arm. This LSI chip selects the data head and either switches write current through the head or amplifies the read signal detected by the head (see figure 6A-8). These paragraphs concentrate on the preamplifier write function and assume that head selection has occurred.

The LSI chip functions as a write driver when the Write Enable line goes active. The chip develops regulated current for the selected head coil and reverses the current in that coil to produce flux reversals on the disk.

Throughout a write operation, write current is always flowing through the head coil. The Write Toggle FF inputs two Write Data lines to the selected arm preamplifier. When a transition occurs on the input lines, the LSI chip switches the write current direction through the head coil. This switching action produces a recorded flux reversal on the disk surface.

While an address mark is being written, the recorded flux reversals cycle at a 0.5F rate.

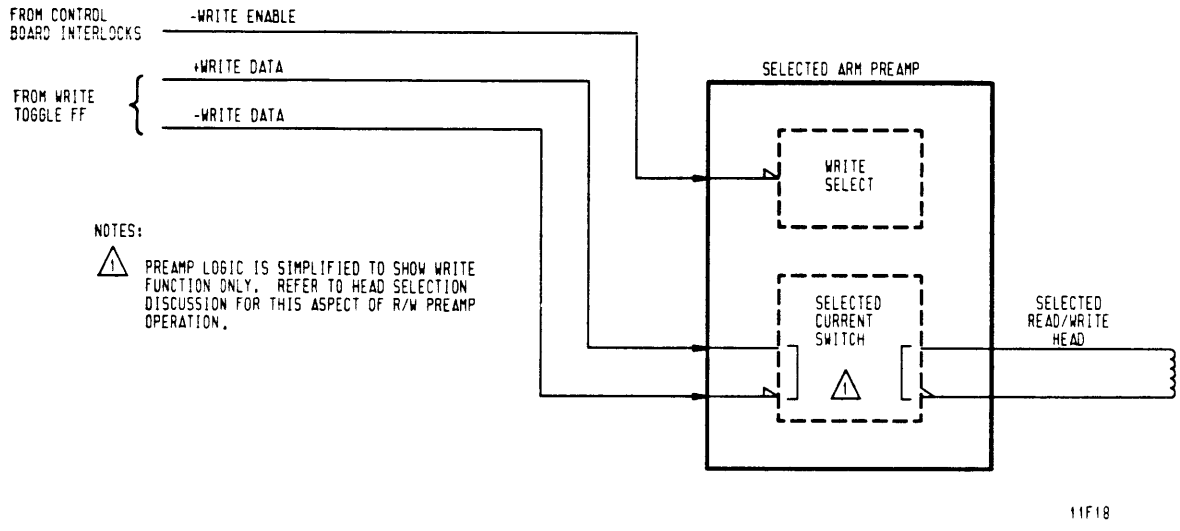


Figure 6A-8. Arm Preamplifier in Write Operations

READ CIRCUITS

GENERAL

The read circuits process data from the disks, making it suitable for transfer to the I/O board. When the Write Enable signal is inactive, an arm preamplifier circuit senses the data written on the disk and generates an analog read data signal.

The analog data goes to the Data Latch circuit which changes it into digital 2-7 data.

The Read Comparator and PLO circuit generates a 2F Read Clock signal that is phase-locked to the 2-7 read data when Read Gate is active. The 2-7 Decoder changes the 2-7 data to NRZ data synchronized to a 1F Read Clock. Both data and clock are then sent to the I/O board.

Figure 6A-9 shows the main elements in the read circuits and table 6A-3 briefly describes each of these elements. The following paragraphs further describe the read circuits.

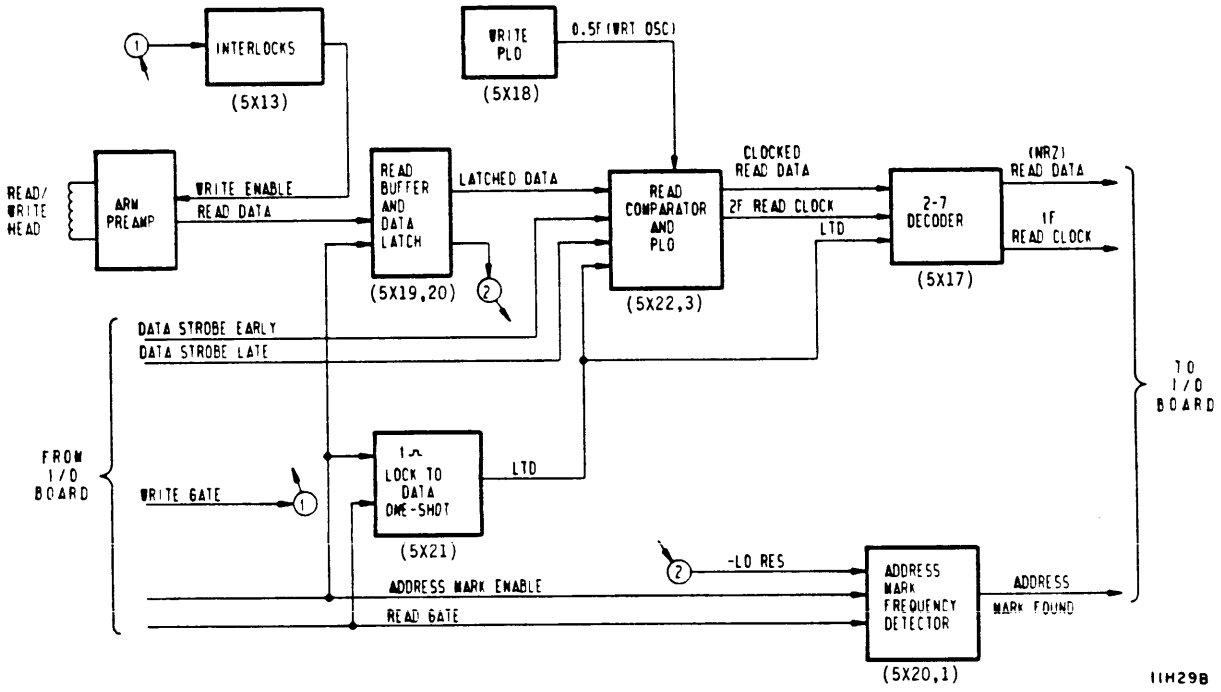


Figure 6A-9. Read Circuits Block Diagram

TABLE 6A-3. READ CIRCUIT FUNCTIONS

Circuit	Function
Arm Preamplifier	Processes the analog signal from the data head for use by the Data Latch.
Data Latch Circuit	Changes the analog 2-7 data into digital 2-7 data. This data is sent to the Read Comparator circuit.
Read Comparator and PLO Circuit	Develops a 2F Read Clock that is synchronized to 2-7 read data.
2-7 Decoder	Translates data coding from 2-7 to NRZ modulation and generates 1F Read Clock synchronized to NRZ data. NRZ data and the 1F Read Clock go to the controller.
Address Mark Detector	Detects the address mark frequency (0.5F) and transmits an Address Mark Found to the controller.

ARM PREAMPLIFIER

The arm preamplifier is an LSI chip that selects one of the data heads on its head-arm and either switches write current through the head or amplifies the read signal detected by the head (see figure 6A-10). These paragraphs concentrate on the preamplifier's read function and assume that head selection has occurred.

The LSI chip functions as a read preamplifier when the Write Enable line is inactive. The chip contains a differential amplifier that is enabled by head selection. In read operations, the coil in the selected head develops a read-back pulse when the head passes over a written flux reversal on the disk. The read-back pulse is supplied as a differential input to the preamplifier.

The differential amplifier selected in the chip amplifies the read signal and sends it on the Read Data lines to the data latch circuitry.

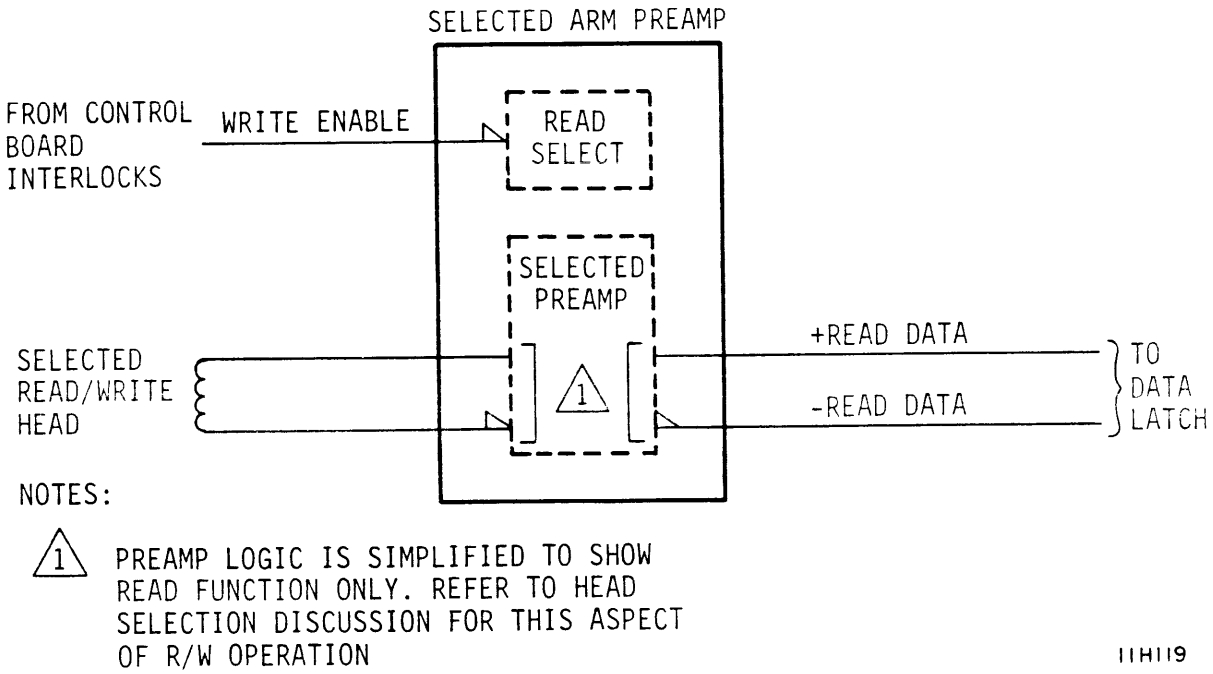


Figure 6A-10. Arm Preamplifier in Read Operations

DATA LATCH CIRCUIT

The Data Latch circuit receives analog read data from the selected arm preamplifier and converts it into digital data. As shown in figure 6A-11, the Data Latch circuit consists of the Data Latch chip and two waveshaping networks that are external to the chip. After being amplified by the read buffer, the analog read data is split into two signal paths -- the high resolution channel and the low resolution channel. The two channels condition the read signal independently to create separate inputs to the Data Latch FF.

The Data Latch chip contains an internal timing circuit that creates the various time delays required by other circuits in the chip. This timing circuit uses the 1F clock signal from the Write PLO as a reference frequency. As shown in figure 6A-11, the timing circuit controls the delays in the digital filter circuit, the lockout circuit, the programmed delay, and the output one-shot.

Splitting the analog data signal into two paths and combining the high and low resolution channels in the Data Latch FF is a system that discriminates against high frequency noise components in the Analog Data but maintains the timing of the data transitions.

The low resolution channel supplies a D-input to the Data Latch FF. The low resolution signal is first conditioned by the low resolution waveshaping network, a band-pass filter. Because it differentiates its input signal, the filter output has a zero-crossing for each peak in the input signal. Inside the Data Latch chip, a comparator hard-limits the signal to develop the digital signal applied to the digital filter. This low-pass filter prevents false zero-crossings from being applied to the Data Latch FF.

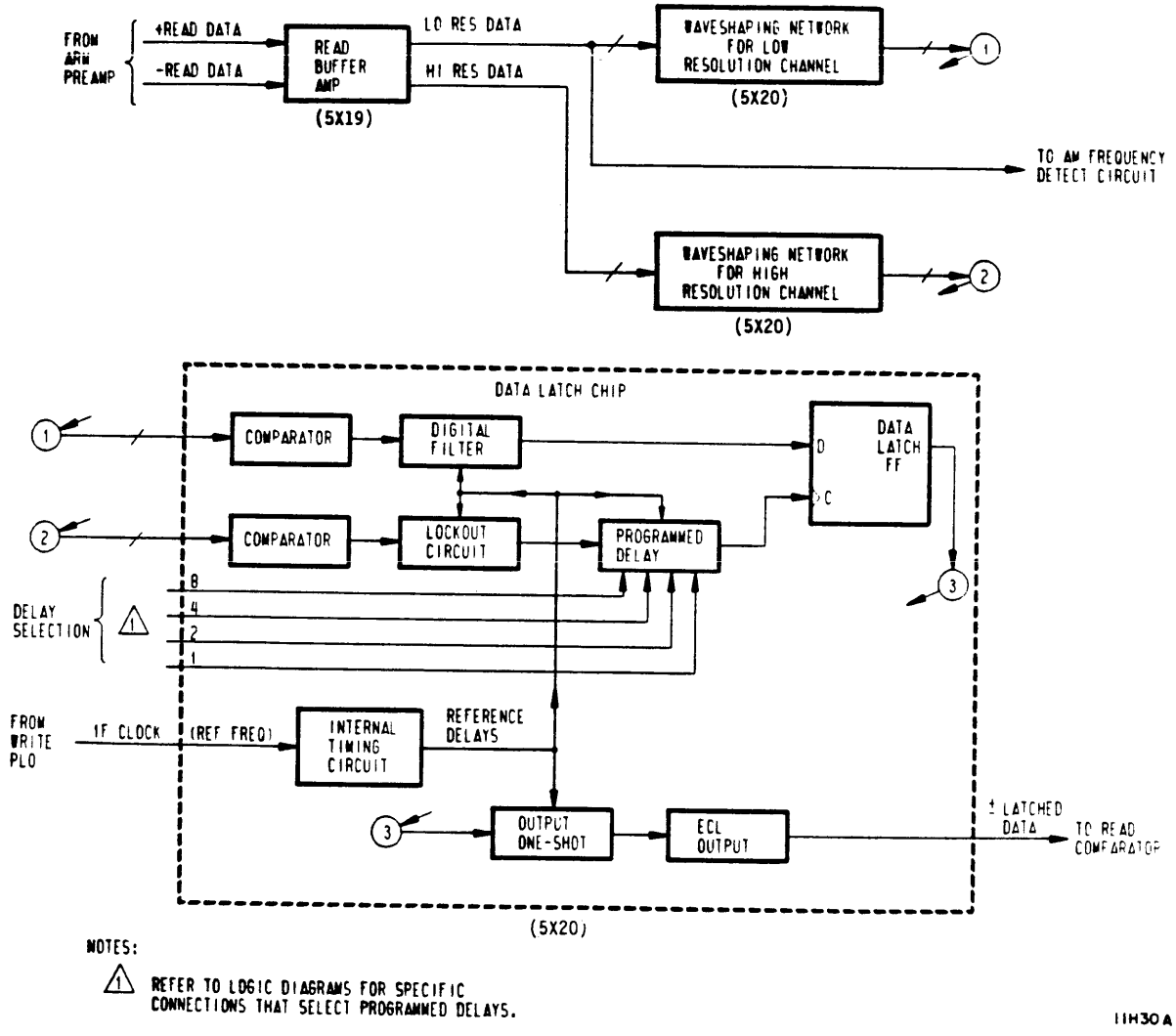


Figure 6A-11. Data Latch Block Diagram

The output of the low resolution channel is a digital waveform similar to the Write Data waveform used in recording. However, filtering out the high frequency components of the input signal lowers the timing resolution in this channel. In the high resolution channel, however, the output signal closely follows the timing present in the input signal.

The high resolution channel supplies delayed clock pulses to the Data Latch FF. The high resolution signal is first conditioned by the high resolution waveshaping network, a band-pass filter with a wider bandwidth than the one used in the low resolution channel. Like the low resolution channel, the output of the wave-shaping network has a zero-crossing for each peak in the input signal. This signal, in turn, is digitized by a comparator and is supplied to a lockout circuit. Each time the lockout circuit is triggered, a delay must elapse before it can be retriggered. Output pulses from the lockout circuit receive a programmed delay, dependent on hardwired connections outside the Data Latch chip. This delay compensates for timing differences between the two channels.

Successive clock pulses toggle the Data Latch FF when the D-input has changed. Erroneous clock pulses from the high resolution channel do not toggle the Data Latch FF because they do not follow a change in the FF's D-input. For each transition of the Data Latch FF, a one-shot pulses the Latched Data output lines. Thus, there is an output pulse for each written flux transition sensed by the data head. The Latched Data from the Data Latch circuitry is sent to the Read Comparator ECL Logic Array.

READ COMPARATOR AND PLO

The Read Comparator and PLO circuitry uses a phase-locked loop to generate the 2F Read Clock, and processes latched read data from the Data Latch to develop clocked read data. Data Strobe commands from the controller condition the timing of clocked read data relative to the read clock to provide a means of error recovery to the read circuitry.

Figure 6A-12 is a simplified block diagram of the Read Comparator and PLO circuitry. The phase-locked loop uses the Read Oscillator Control portion of the Read Comparator ECL Logic Array to regulate operation of the Current Pump and to provide stop/start control of the Voltage-Controlled Oscillator (VCO). The Current Pump supplies a Control Voltage signal to the VCO that determines the frequency of the 2F Read Oscillator signal output from the VCO. The 2F Read Oscillator signal is fed back to the Read Oscillator Control to complete the loop.

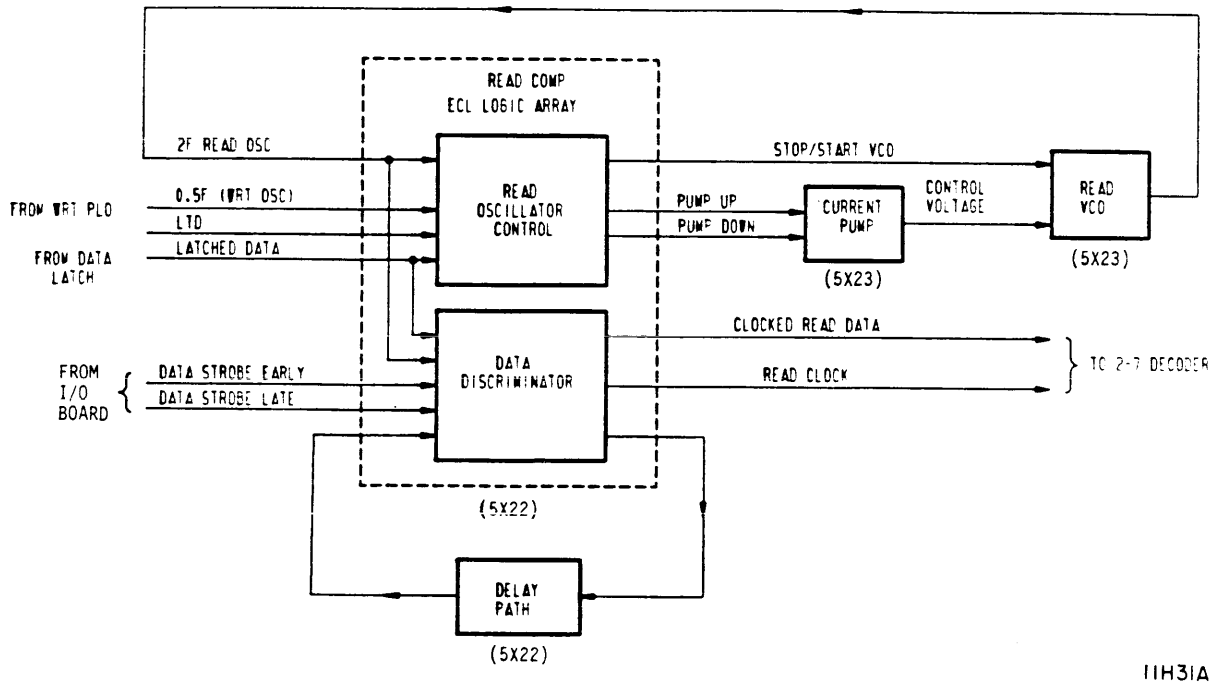


Figure 6A-12. Read Comparator and PLO Block Diagram

The phase-locked loop locks the VCO frequency to one of two reference signals. When the drive is reading data, the phase-locked loop uses the pulse train on the Latched Data line as a timing reference. In this case, the Read Oscillator Control varies the pulse length on the Pump Up and Pump Down lines. This keeps the rising edges of the 2F Read Oscillator signal coincident with the rising edges of Latched Data pulses. When the Pump Up and Pump Down pulses differ in length, the Control Voltage to the VCO varies accordingly to phase shift the VCO and bring it into phase lock.

When the drive is not reading data, the phase-locked loop maintains the VCO frequency close to the value it has during read operations. In this mode, the Read Oscillator Control monitors the phase difference between the 0.5F Write Oscillator signal (derived from the Write PLO) and the 2F Read Oscillator signal fed back from the VCO. Pulses on either the Pump Up or the Pump Down line keep the 2F Read Oscillator signal in phase with the 0.5F Write Oscillator signal.

The Read Oscillator Control circuitry uses the Stop/Start VCO line to control VCO operation while beginning and ending read operations. A pulse appears on the Stop/Start VCO line following a change in the Read Gate signal. While the Stop/Start VCO line is active, the VCO is inhibited, and its control voltage is held constant. This enables the Read PLO to phase lock quickly during the switching transitions.

The Data Discriminator portion of the Read Comparator ECL Logic Array conditions the 2F Read Clock and Clocked Read Data signals for use in the 2-7 Decoder (see figure 6A-12). With nominal timing, pulses on the Clocked Read Data line are active for one 2F bit cell, and positive transitions of the 2F Read Clock coincide with the center of Clocked Read Data pulses.

For error recovery, the controller can issue a Data Strobe Early or a Data Strobe Late command to shift this timing either way from its nominal value. In response to a Data Strobe Early command, the Data Discriminator routes the clock signal through a delay path. This process delays the 2F Read Clock relative to the Clocked Read Data pulses. In response to a Data Strobe Late command, the Data Discriminator routes the data signal through a delay path. This process delays the Clocked Read Data pulses relative to the 2F Read Clock.

The Clocked Read Data and 2F Read Clock signal are sent to the 2-7 Decoder, which converts the read data from 2-7 code into NRZ form and generates the 1F Read Clock.

2-7 DECODER

The 2-7 Decoder converts 2-7 data into NRZ data and generates the 1F Read Clock from the 2F Read Clock. Both inputs, the 2-7 data and the 2F Read Clock, come from the Read Comparator and PLO circuitry.

As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven 2-7 code words and seven NRZ code words. The decoder recognizes the coding in the 2-7 read data input as a succession of the seven 2-7 words, and outputs a series of NRZ code words, each one translated from its 2-7 equivalent. Table 6-2, presented under Basic Read/ Write Principles, shows the translation used between the two groups of seven code words. The 2-7 decoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

Figure 6A-13 is a simplified block diagram of the 2-7 Decoder. The decoder synchronizes after the Lock to Data input goes inactive. The lock to data interval occurs after Read Gate or Address Mark Enable goes active. Once Lock to Data goes inactive, synchronization occurs when the 2-7 input data contains three or more binary zeros followed by a binary one. This binary one sets up the proper phase of the 1F Read Clock relative to the NRZ Data output line and initiates the decoding process. The clock and decoding operations are discussed in the following paragraphs.

The 1F Read Clock is generated from the 2F Read Clock as this signal clocks a divide-by-two FF. The Q-output of the FF is inverted and supplied to the D-input through a gate that is enabled as a result of synchronization. Synchronization selects which positive edge of the 2F Read Clock determines the positive edge of the 1F Clock.

The decoding function is performed by a state sequencer. The state sequencer has eight FFs, and each of the eight states corresponds to one of the FFs being set. It operates by shifting states on each falling edge of the 1F Read Clock. Thus, the interval for each state is one NRZ bit cell. Two factors determine the current state of the sequencer. These are the previous state and the binary values of the last two

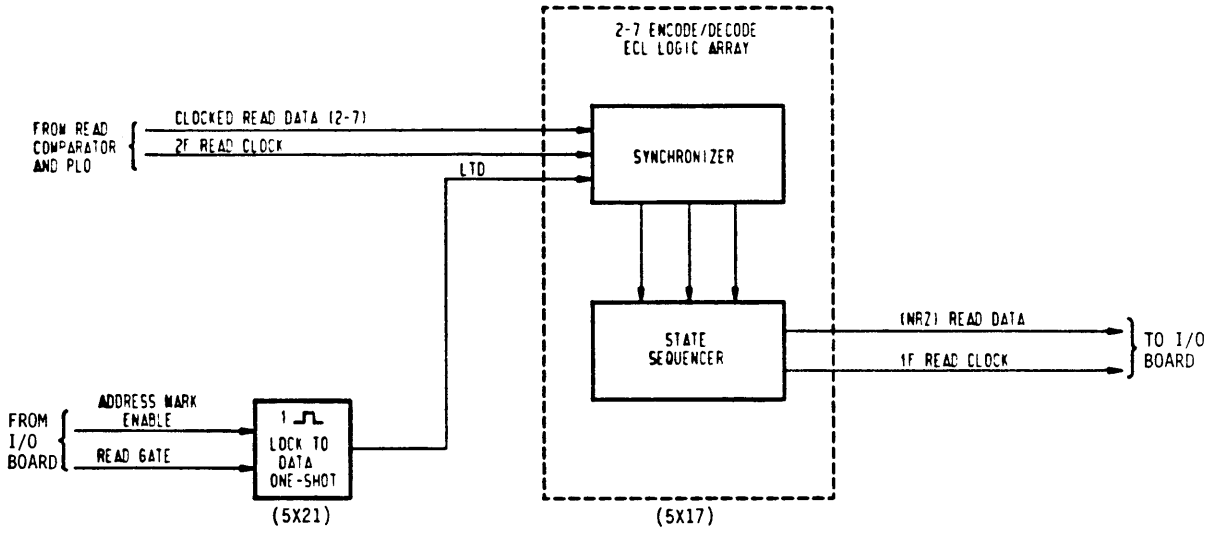


Figure 6A-13. 2-7 Decoder Block Diagram

2-7 data bits input to the circuit. Therefore, at any time the state of the sequencer reflects the recent decoder inputs. The binary level decoded on the NRZ Data lines is state-dependent. During two of the states (NRZ bit cells), the output is binary zero, and during the other states, the output is binary one. In summary, the way the sequencer maps one state into the next state implements the specified translation from 2-7 data words into NRZ data words.

The decoder output stays low until synchronization occurs, and there is a processing delay of four 2-7 bit cells within the decoder.

The decoder sends the NRZ Read Data and Read Clock outputs to the I/O board.

ADDRESS MARK DETECTION

The Address Mark Detector (shown in figure 6A-14) monitors the Low Resolution signal from the Read Amplifier during an address mark search. If a frequency of 0.5F is decoded over a period equivalent to three byte times, the detector activates the Address Mark line, which in turn clocks a latch.

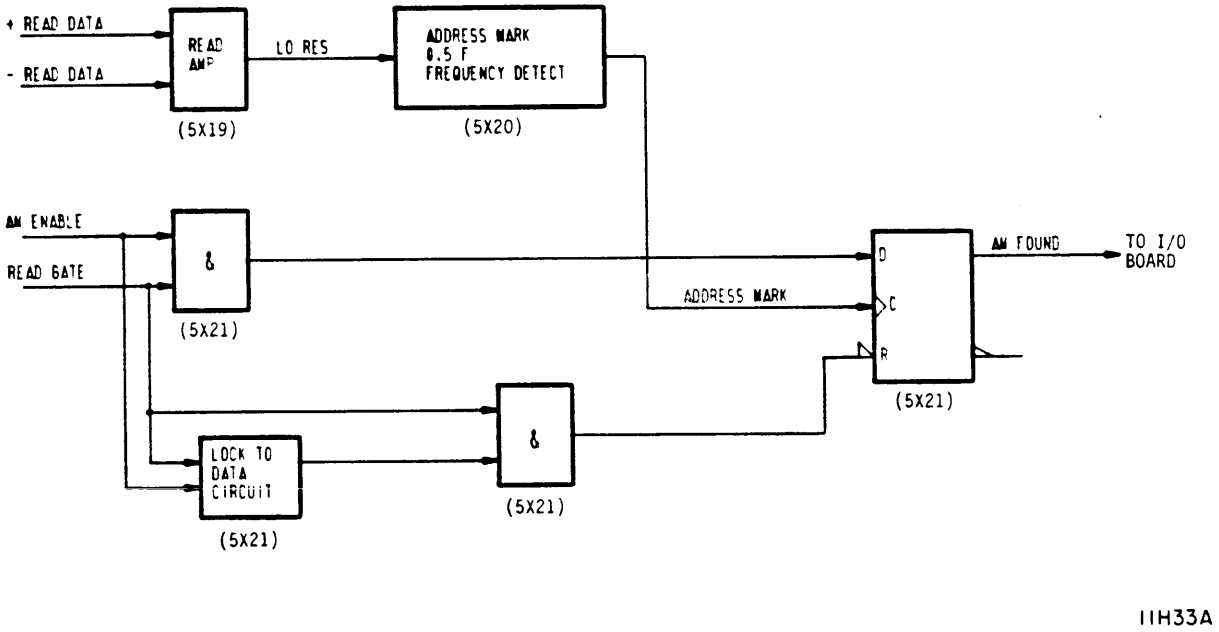


Figure 6A-14. Address Mark Detector Block Diagram

Figure 6A-14 shows the input and output signals for the Address Mark Detector. During an address mark search, the Read Gate line and the Address Mark Enable line are both active. With these signals active, the Address Mark Found latch gets set when an address mark pattern is detected.

The Address Mark Found line remains set until Read Gate goes inactive or the lock-to-data interval ends. A delay occurs between the time that Address Mark Enable is cleared and the end of the lock-to-data interval.

SECTION 6B

PARALLEL READ/WRITE FUNCTIONS

PARALLEL READ/WRITE FUNCTIONS 6B

INTRODUCTION

This section describes read/write functions for a drive that has two read/write channels and selects two heads at a time. When the drive is on cylinder, it is ready to select the heads and perform a read or write operation. The controller issues one command to select the heads and another command to initiate a read or write operation.

During a write operation, the drive receives data from the controller, separates it into two write channels, and writes it on two disks. During a read operation, the drive recovers data from two disks, processes it in two read channels, recombines it, and transfers it to the controller. The principles of recording and recovering data from a magnetic disk are discussed in section 6 under Basic Read/Write Principles.

The description of the read/write circuits is divided into the following areas:

- Head Selection -- Describes the circuitry used for head selection and the arrangement of read/write heads in the module.
- Write Circuits -- Describes the circuits used by the drive to record data on the disk.
- Read Circuits -- Describes the circuits used by the drive to recover data from the disk.

The discussion of read/write functions makes references to signal frequencies in relation to the bit transfer rate (1F) of each read/write channel. The signal frequencies are defined in table 6-1 near the beginning of section 6.

HEAD SELECTION

A pair of physical heads must be selected before a read or write operation can be performed. Under Servo MPU control, the servo system moves the heads to the cylinder specified by the controller. By selecting a pair of heads, the controller specifies two particular tracks within that cylinder. As part of a Head Select command, the controller indicates the new logical head address.

The drive has one read/write head for each data recording surface in the disk module: 14 recording surfaces and 14 read/write heads as shown in figure 6B-1. (One read/write head is not used.) In addition, the drive has one servo head. The servo head continuously reads prerecorded data from the servo disk surface for use by the drive servo circuits.

Read/write information is transferred to and from the heads through cables connected to a preamplifier mounted on the arm. The preamplifiers connect to the read/write circuitry via the arm matrix board, located inside the sealed module.

The Head Select command gates the logical head address into the Head Address register (HAR) located on the I/O board. For each logical head address, two physical heads are enabled. Figure 6B-2 shows the head selection circuits.

The Head Address lines go from the I/O board to the control board where they address a ROM. Depending on its addressing, the ROM activates two of its output lines, Arm Select 1-8, to enable two arm preamplifiers. Each of the enabled arm preamplifiers in turn selects a physical head on its head-arm in response to the Head Select 1 line. This line is activated by Head Address line 0. The Arm Select, Head Select, and common control lines for the preamplifiers are routed through the arm matrix board (inside the module) to the individual arm preamplifiers.

If an illegal head address is received, no head is selected. A Write Fault occurs if the drive attempts to write data with no head selected.

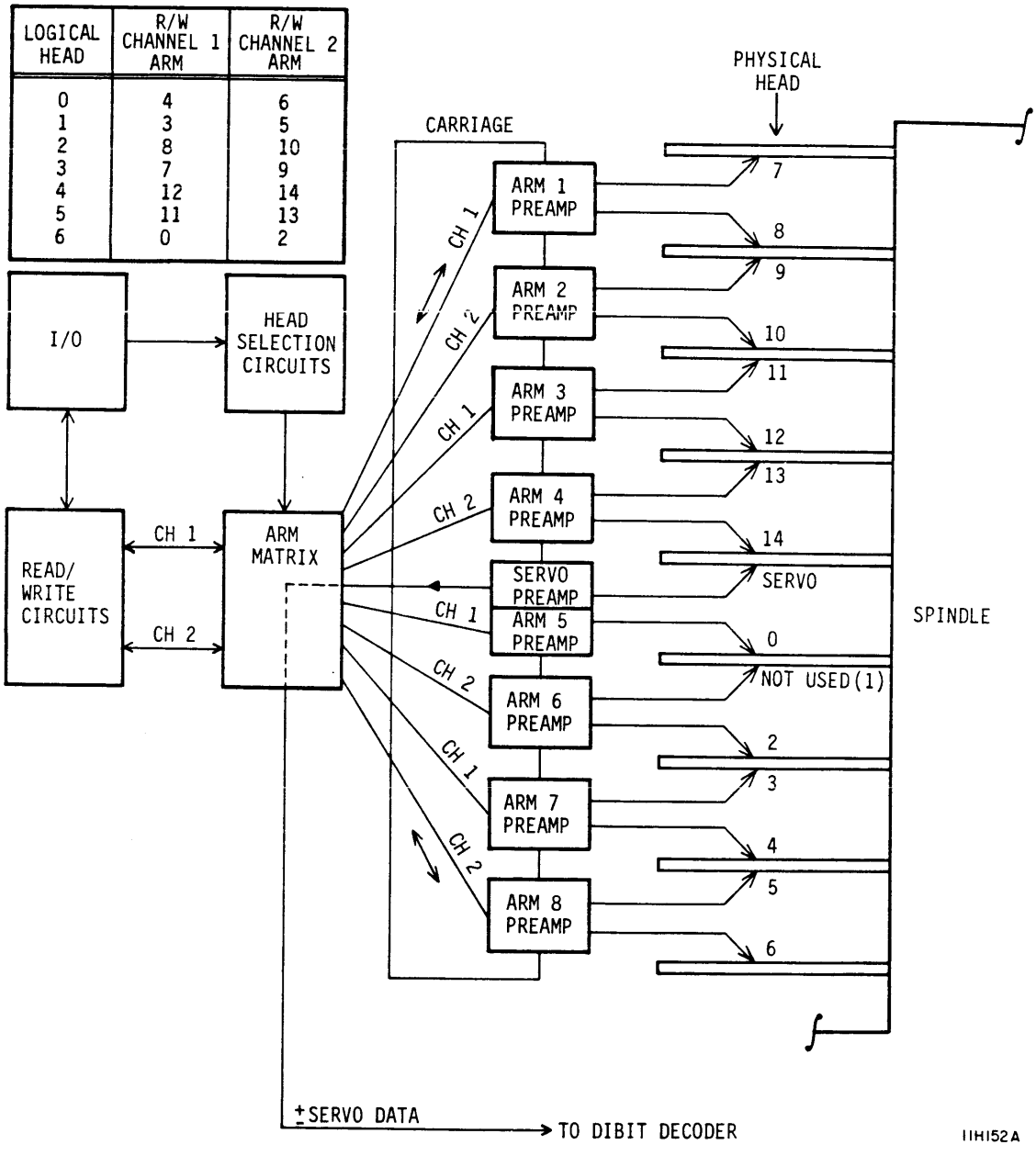


Figure 6B-1. Read/Write Heads (Parallel)

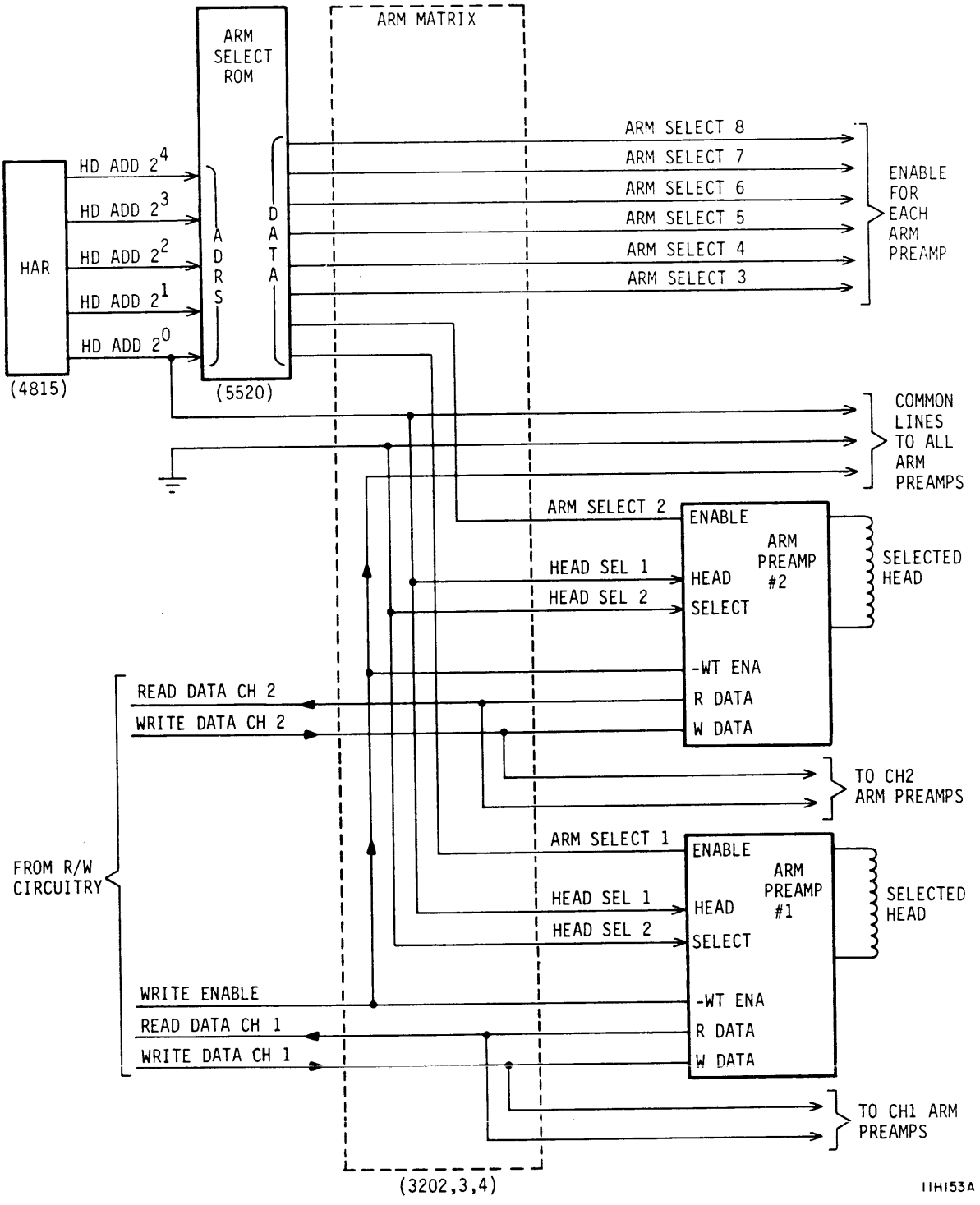


Figure 6B-2. Head Selection Circuits (Parallel)

WRITE CIRCUITS

The write circuits process data from the I/O board, making it suitable for transfer to the disks. Figure 6B-3 shows the write circuits. The Write Gate signal allows the drive to start processing serial NRZ data received (in two write channels) from the I/O board. NRZ data is synchronized to the 1F Servo Clock derived from the Write PLO. The Write Data is received via the two Write Data line and is first sent to the 2-7 encoder circuits, one for each write channel.

For each write channel, the 2-7 encoder circuit converts the data to 2-7 modulation and sends it to the corresponding write compensation circuit. Write compensation modifies the data timing, and the compensated data is then processed by the Write Toggle FF. The Write Toggle FF provides the data signal that controls current switching in the selected arm preamplifier.

For more information about the individual write circuits, refer to section 6A. The individual write circuits are similar in standard and two-head parallel drives.

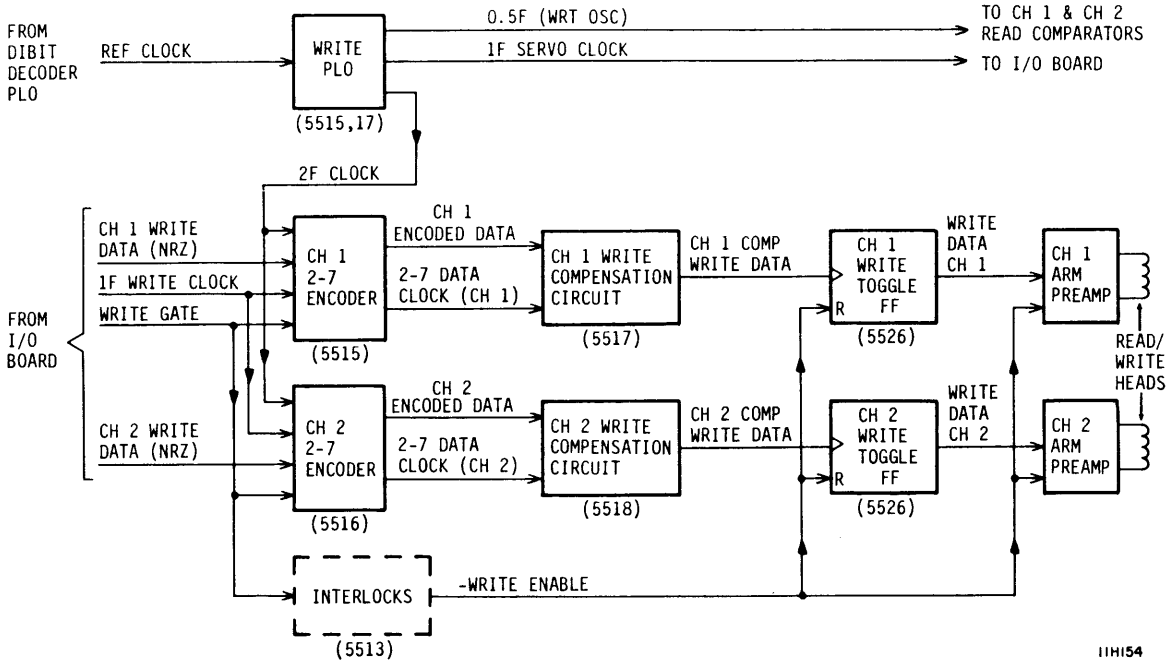


Figure 6B-3. Write Circuits Block Diagram (Parallel)

READ CIRCUITS

The read circuits process data from the disks, making it suitable for transfer to the I/O board. Figure 6B-4 shows the read circuits. To allow data to be read from two read/write heads in parallel, there are two read channels. When the Write Enable signal is inactive, two arm preamplifier circuits sense the data written on the disks and generate analog read data signals, one for each channel.

For each read channel, the analog data goes to the Data Latch circuit which changes it into digital 2-7 data. The Read Comparator and PLO circuit generates a 2F Read Clock signal that is phase-locked to the 2-7 read data when Read Gate is active. The 2-7 Decoder changes the 2-7 data to NRZ data synchronized to a 1F Read Clock. Data and clock signals for each channel are then sent to the I/O board, where they are combined for transfer to the controller.

For more information about the individual read circuits, refer to section 6A. The individual read circuits are similar in both standard and two-head parallel drives.

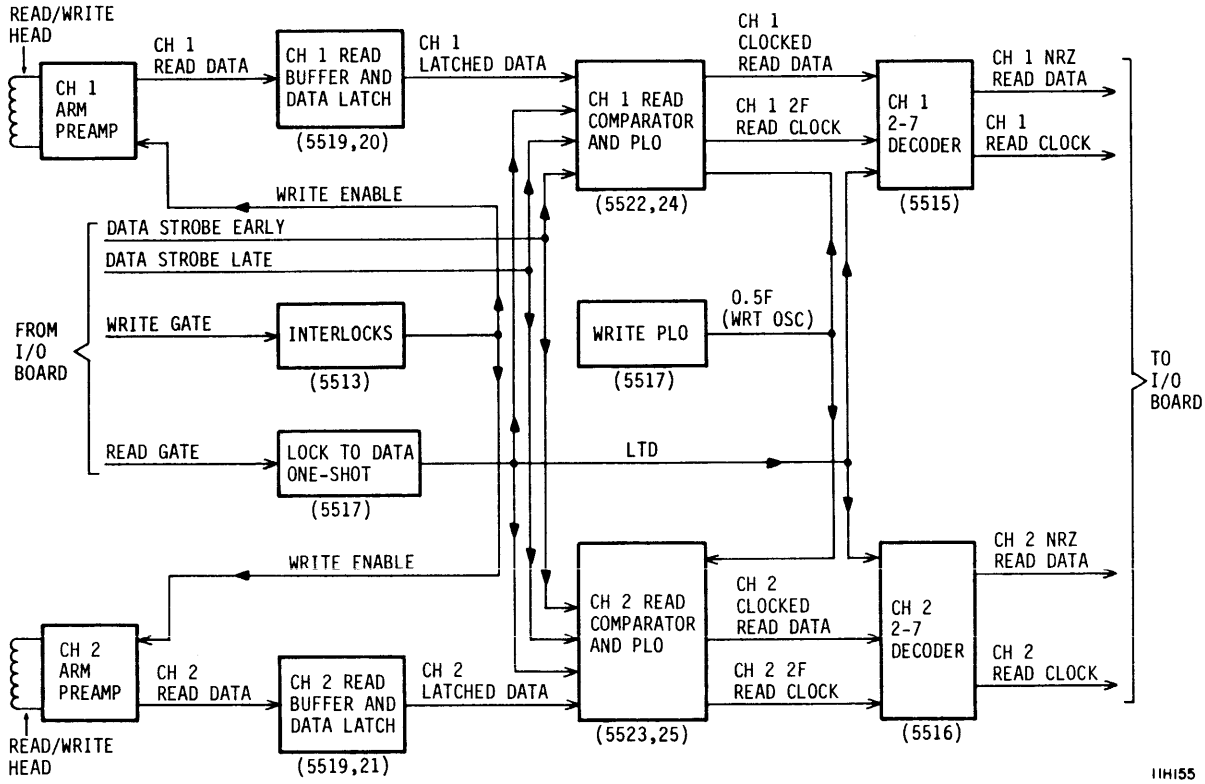


Figure 6B-4. Read Circuits Block Diagram (Parallel)

SECTION 7

DETECTING AND ANALYZING ERRORS

DETECTING AND ANALYZING ERRORS 7

INTRODUCTION

This section discusses how the drive circuits recognize errors, how errors are indicated and cleared, and how the drive operates during diagnostic testing. This description is divided into the following areas:

- Error Conditions -- Describes errors: how they are recorded, how they are cleared, and how they are detected.
- Operator Panel and Status/Control Panel Functions -- Describes how information is transferred between these panels and other circuits in the drive.
- Diagnostic Functions -- Describes the running of diagnostic tests.

ERROR CONDITIONS

The following topics describe those conditions which are interpreted by the drive as either faults or errors:

- How Errors are Recorded and Cleared -- Explains the effect of faults and seek errors on drive operation and actions that clear them to return the drive to normal operation.
- How Errors are Detected -- Lists the conditions that produce error status.

HOW ERRORS ARE RECORDED AND CLEARED

Error Latch Circuitry

Seven error conditions in the drive result in an active Fault line. A gate array in the I/O circuitry has one latch for each of these fault conditions and a latch for seek errors. Drives with the SMD interface use the SMD-E Gate Array (shown in figure 7-1). Drives with the SCSI and IPI interfaces use the CDIC chip (shown in figure 7-2). Throughout the remainder of this section, the SMD-E Gate Array and the CDIC chip will be called simply the I/O gate array. When any of these error conditions occurs, the drive sets the respective latch in the I/O gate array.

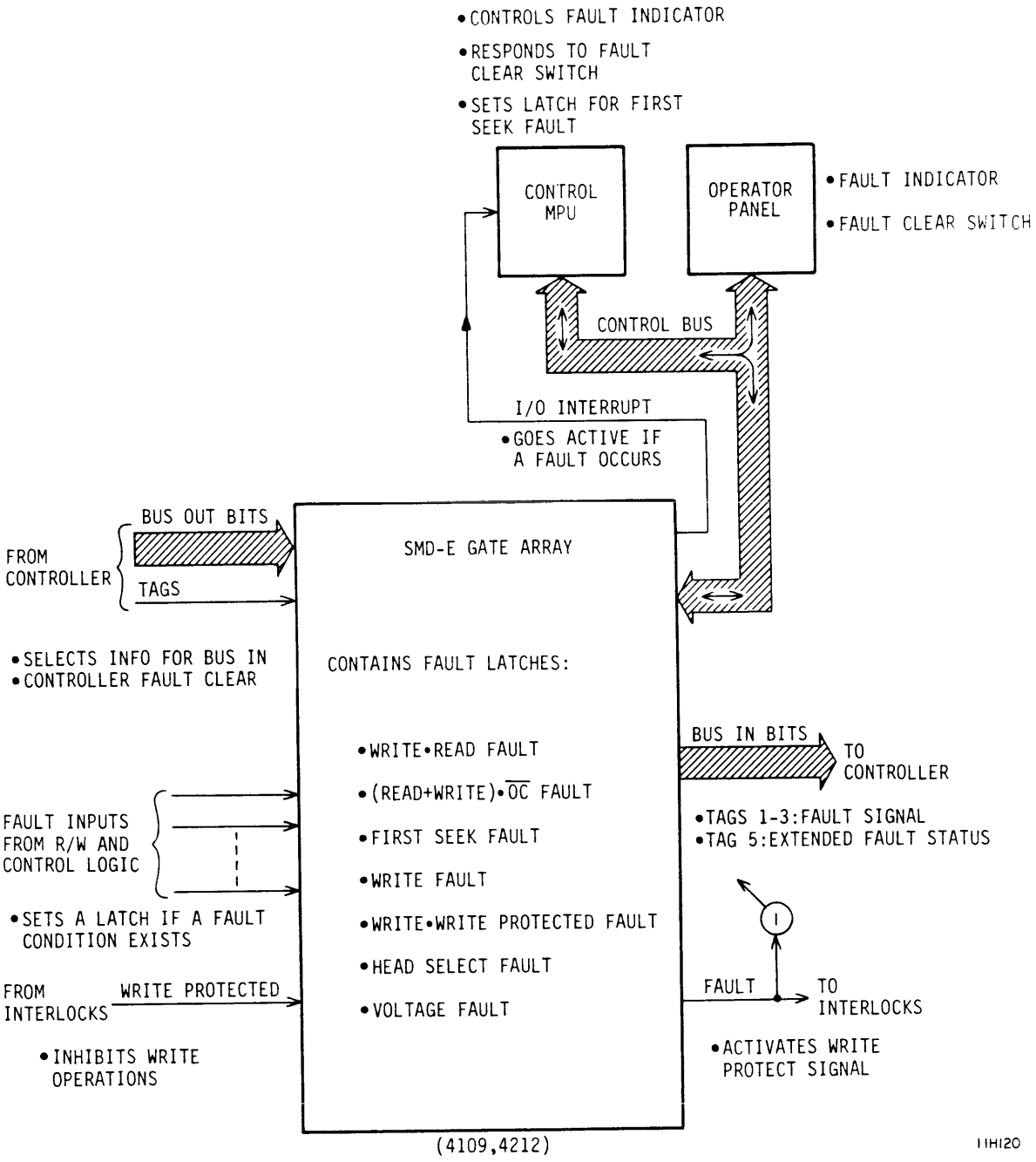


Figure 7-1. SMD Error Circuitry

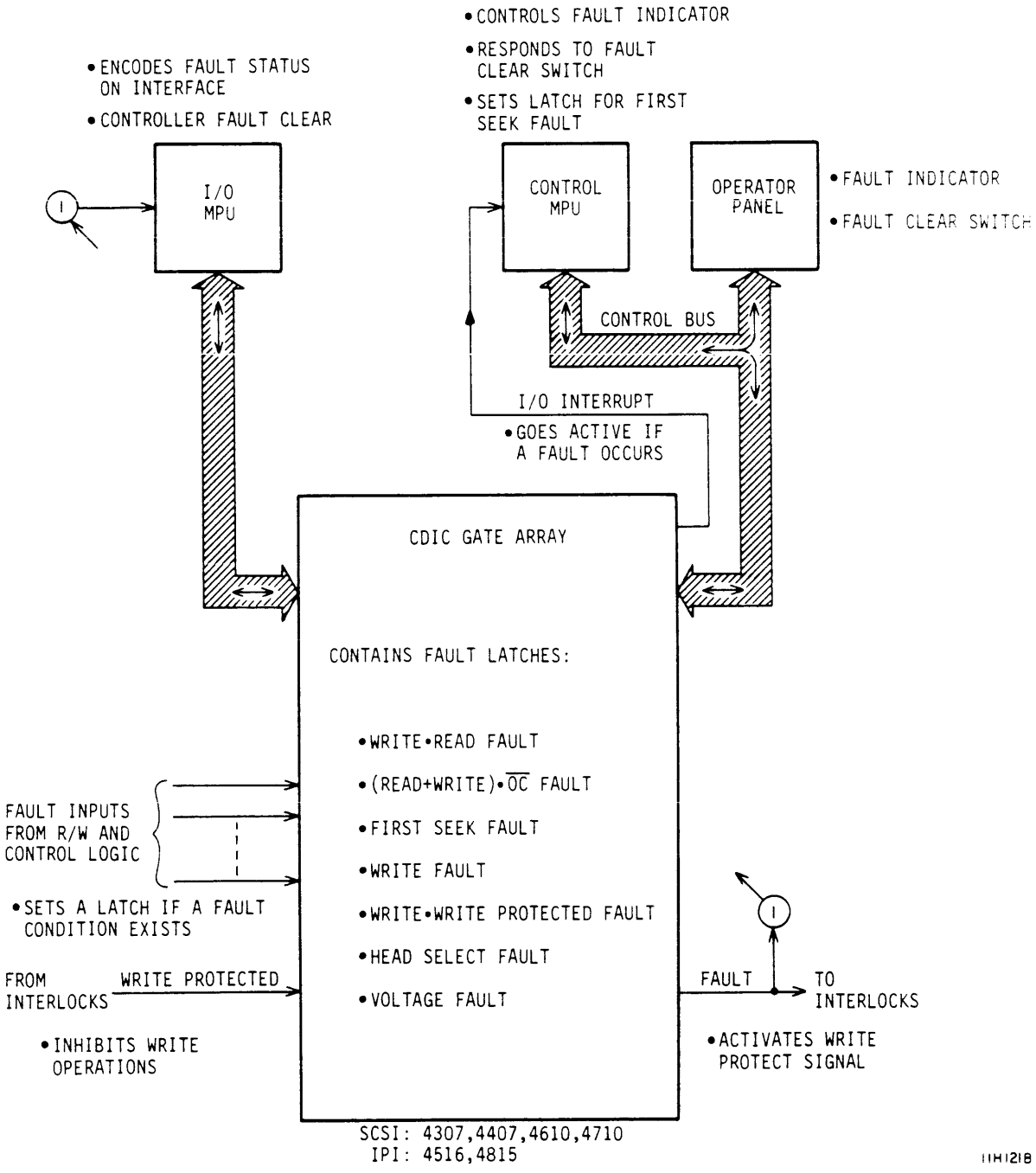


Figure 7-2. SCSI and IPI Error Circuitry

An OR circuit in the I/O gate array receives inputs from each of the seven fault latches (but not the Seek Error latch). If one or more of the fault latches is set, the OR circuit activates the Fault line.

When a fault condition occurs, the Control MPU lights the FAULT indicator on the operator panel (if installed), disables write operations, and clears the Ready latch in the same gate array. Clearing the Ready latch causes the Ready indicator on the operator panel to flash until the fault is cleared.

Provided the fault condition or conditions no longer exist, the Fault signal is cleared by the following:

- Fault Clear switch on the operator panel (if present)
- Controller Fault Clear command (see next topic)
- Powering down the drive

When the Fault Clear switch (if present) is pressed, it interrupts the Control MPU. The Control MPU responds by sending a reset code on the Control Bus lines for the seven fault latches. The gate array develops a second reset signal for the seven fault latches in response to a controller Fault Clear command. In either case, the reset input will clear a latch only if it is no longer being set by the error condition. In the process of removing and reapplying power to the drive, the fault circuitry is initialized as part of the power sequence, and any preexisting fault status is lost.

Communicating Errors

This topic describes how errors are reported on each interface and how the error signals can be cleared through each interface.

Errors on the SMD Interface

For both the SMD-O and SMD-E interfaces, Fault status is returned to the controller on Bus In Bit 3 in response to Tags 1 through 3 or the Unit Select Tag. The Fault line remains active until the latches are cleared. Provided the fault condition or conditions no longer exist, the controller can clear the fault by issuing a Fault Clear command (Tag 3 with Bus Out Bit 4 active).

Seek Error status is returned to the controller on Bus In Bit 2 in response to Tags 1 through 3 or the Unit Select Tag. The controller can clear the Seek Error by issuing an RTZ Seek command (Tag 3 with Bus Out Bit 6 active).

If the unit is configured with an SMD-E interface, the controller can request extended fault status. The controller issues Tag 5 with all Bus Out Bits set to zero and sees the seven possible fault conditions on Bus In Bits 0 through 6. Section 3A describes how the SMD-0 and SMD-E interfaces differ and defines the Bus In Bit assignments for Tag 5.

Errors on the SCSI Interface

When either the Seek Error latch or one of the fault latches is set, the I/O MPU sets up CHECK CONDITION status in the next STATUS phase on the SCSI Bus. The initiator can determine the type of error present by issuing the target a REQUEST SENSE command. The target responds by transferring sense data encoded in the EXTENDED SENSE DATA FORMAT. An error code included in this format specifies the type of error present.

If a fault latch is set, but the fault condition no longer exists, the latch will be cleared when the initiator issues the REQUEST SENSE command. If the Seek Error latch is set, the Seek Error is cleared when the initiator issues a REZERO UNIT command.

Errors on the IPI Interface

When either the Seek Error latch or one of the fault latches is set, the I/O MPU performs the following:

- It activates the Status Pending interrupt.
- It sets up exception status for the controller.
- It activates the Attention In line.

The controller can determine the type of error present by issuing a Read Status bus control, described earlier in section 3C. The drive reacts by transferring a status response to the controller. This response indicates the specific error present.

If a fault latch is set, but the fault condition no longer exists, the latch will be cleared when the controller issues the Read Status bus control. If the Seek Error latch is set, the Seek Error is cleared when the initiator issues a Recalibrate function (available through the Load Drive Function bus control).

HOW ERRORS ARE DETECTED

This topic describes the individual error conditions that set each of the latches in the I/O gate array.

Voltage Fault

This fault is generated whenever the +12, -12, +5 or -5 voltages are detected to be below satisfactory operating levels. As shown in figure 7-3, these voltages are monitored by threshold detectors on the control board.

When the Voltage Fault signal goes active, it sets the individual fault latch in the I/O gate array and latches the Power Amp Enable signal inactive in the Peripheral Array. Resetting the Power Amp Enable latch sets the MP Write Protect latch. Setting the MP Write Protect latch protects existing

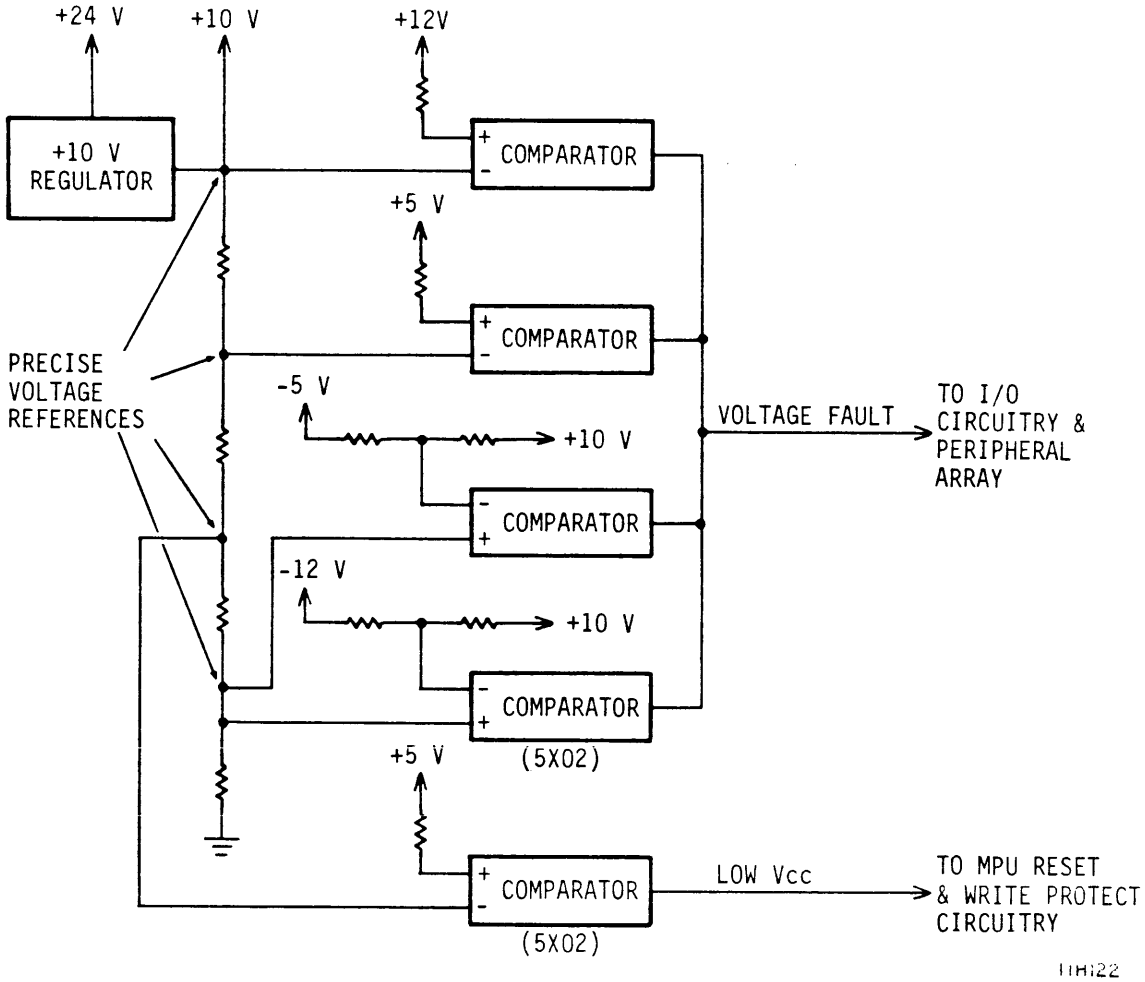


Figure 7-3. Detecting Voltage Faults

data on the disks by inhibiting the write circuitry while a voltage problem exists. This supplements the write protection normally invoked when the Fault line is active or when the drive is placed in the Write Protect mode.

An additional voltage detector circuit detects when the +5 V supply drops to 4.67 V, making microprocessor operation unreliable. This condition generates a Low Vcc signal used to reset the Sector Counter, the Servo MPU, Motor MPU, and produce the DC Master Clear signal for the Control MPU. Also, when the Low Vcc signal goes active, the Control MPU issues a Retract command and drops the Power Amp Enable command (via the Peripheral Array) to produce an emergency retract of the actuator.

Read Or Write and Off Cylinder Fault

This fault is generated if the controller initiates a read or write operation while the drive is in an off cylinder condition. The fault detection logic, located inside the I/O gate array, receives Write Gate, Read Gate, and the output of the On Cylinder FF. When the On Cylinder FF is cleared and either gate goes active, logic in the gate array sets the associated fault latch.

Write Fault

The circuitry that detects a write fault monitors inputs from the arm preamps and the 2-7 encoder. Figure 7-4 shows how write faults are detected in drives that have a single write channel. Drives that write with two heads in parallel monitor the same fault conditions in each write channel. A write fault is encoded if any of the following conditions exist:

- No write current in the selected arm preamp (makes Write OK signal inactive)
- Write Clock not present when Write Gate is active (makes Clock Fault signal active)
- No write data transitions when the Write Gate is active (makes Write OK signal inactive)
- Head open (bad head detected makes Write OK signal inactive)
- No Arm Enable signal is active when Write Enable is active (makes Write Select Verify signal inactive).

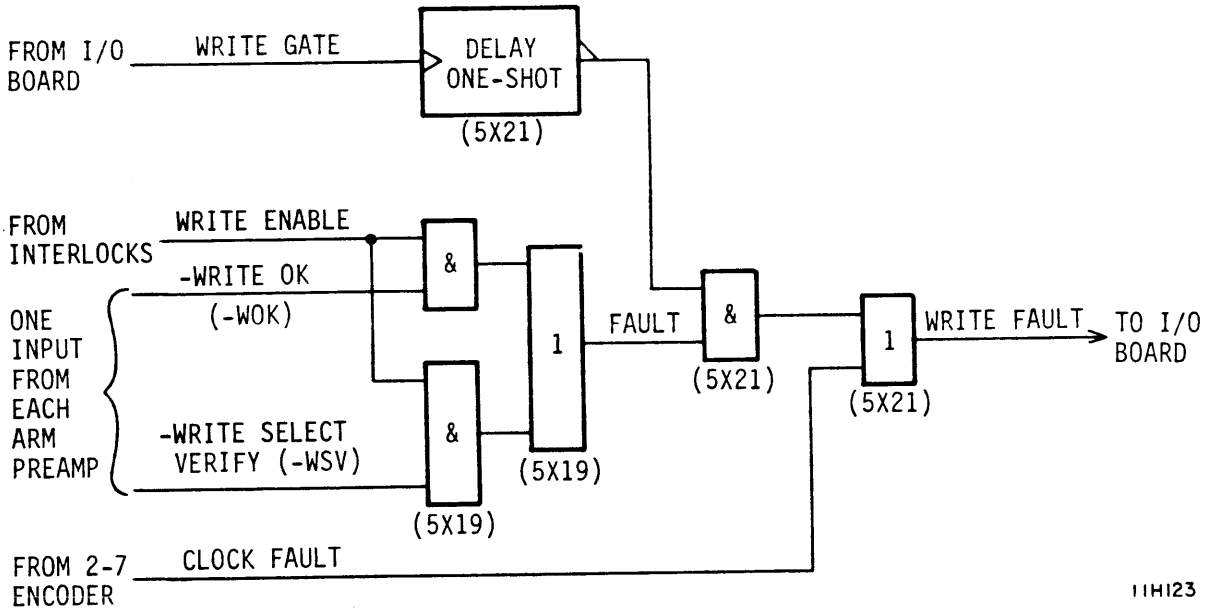


Figure 7-4. Detecting Write Faults

All of these conditions activate the Write Fault line going to the I/O gate array. A gate in the read/write circuitry allows these individual fault conditions to activate the Write Fault signal only when Write Enable is active. The gate keeps the Write Fault line inactive during transitions between read and write operation. The active Write Fault line sets the associated latch in the I/O gate array.

Head Select Fault

In drives that have a single read/write channel, this fault is generated when more than one arm preamp is selected during a write operation. In drives that have two parallel read/write channels, this fault is generated when more than one arm preamp is selected for either channel during a write operation. When this condition is detected, it sets the associated latch in the I/O gate array.

Read and Write Fault

This fault is generated whenever the drive receives a Read Gate and a Write Gate simultaneously. This condition is detected inside the I/O gate array and sets the associated latch.

Write and Write Protected Fault

This fault is generated whenever a write operation is attempted while the drive is in a Write Protected mode. Figure 7-5 shows what happens in this situation:

- Write Enable is inhibited.
- The I/O gate array receives a Write and Write Protected Fault input.

The Control MPU activates the MP Write Protect line during a drop in motor speed, after a voltage fault, or in response to the Write Protect switch on the optional operator panel.

First Seek Fault

First Seek fault, as opposed to Seek Error, results from error conditions that occur during the load operation. Seek Error, on the other hand, indicates error conditions that occur during normal seeks and RTZ seeks. A First Seek fault generates an active Fault signal while a Seek Error does not. Seek Errors are discussed in the next topic, and the error conditions that cause a First Seek fault are described in the following paragraphs.

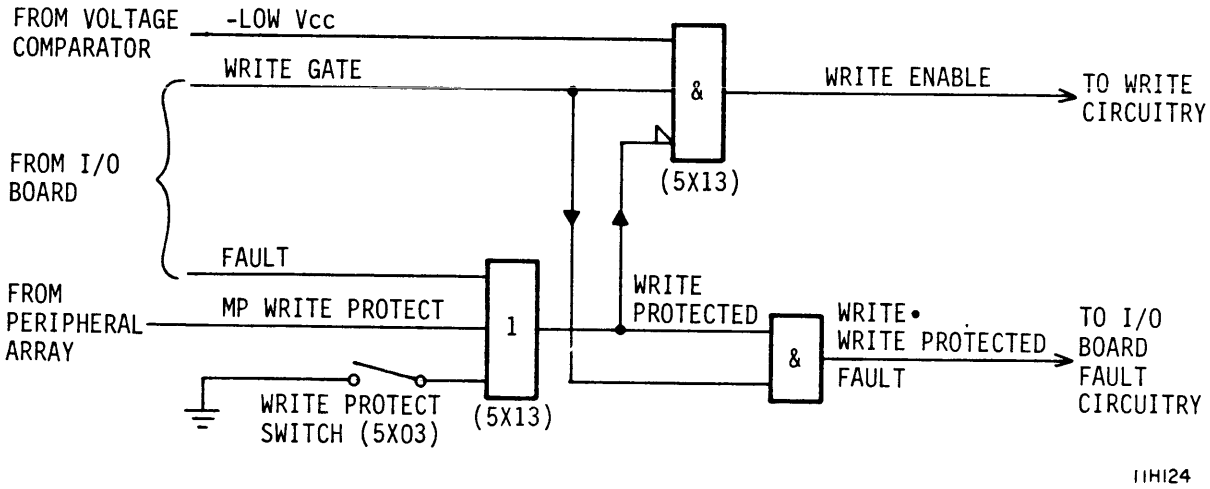


Figure 7-5. Detecting Write and Write Protected Faults

Unlike the other individual fault latches, the latch for First Seek fault is set by the Control MPU. To set the latch, the Control MPU inputs the I/O gate array with an address on the Control Bus. The error conditions resulting in a First Seek fault are monitored by the Control MPU during the power on initialization and load operation. Assuming that the Control MPU is operational, it sets the associated latch in the I/O gate array if any of the following tests fail:

- Demodulator inactive at the start of the load, but changing to active after the heads move outward from the landing zone. Demodulator must remain active throughout the rest of the load.
- The Fault line stays inactive during the load.
- The Servo MPU moves the heads out of the landing zone and detects 100 cylinder pulses before a timeout occurs.
- At least one cylinder pulse is detected by the Servo MPU in the outer guard band as the heads approach track zero.
- The load portion of the seek is completed within the time allowed by the Control MPU.
- The RTZ portion of the seek is completed within the time allowed by the Control MPU.
- On cylinder sense is detected during track-following. If on cylinder sense goes inactive after start of track-following, it returns to the active state and does not go inactive more than 16 times.
- Fewer than three cylinder pulses are detected during track-following.

The Control MPU aborts the load operation when a First Seek fault is detected. A controller Fault Clear command or pressing the Fault Clear switch on the operator panel (if present) will reset the Fault signal, turn off the Fault indicator on the panel, and initiate another load attempt.

Seek Error

Seek Error is a status signal indicating error conditions that occur during normal seeks and RTZ seeks. The Seek Error signal is active when the Seek Error FF, located in the I/O gate array, is set. Seek Error does not activate the Fault signal.

During normal seeks and RTZ seeks, the Servo MPU tests certain error conditions and provides status to the Control MPU. If any tests fail, the Control MPU sets the Seek Error FF in the I/O gate array. These tests include the following:

- The new cylinder address, specified by the controller for a normal seek, is less than or equal to the maximum legal cylinder. This cylinder address is 1634 on 736 MB, 1120 MB, 1153 MB, and 1230 MB drives (1380 on 850 MB drives).
- The Demodulator Active signal is active at the start and end of normal seeks, and it is active throughout RTZ seeks.
- Fault stays inactive throughout seeks.
- The seek is completed within the time allowed by the Control MPU.
- On cylinder sense detected during track-following. If on cylinder sense goes inactive after start of track-following, it returns to the active state and does not go inactive more than 16 times.
- Fewer than three cylinder pulses are detected during track-following.
- A voltage fault has not occurred.

If any test fails, the Control MPU sends Seek Error status to the controller. In the event of a Seek Error, the Control MPU halts the Servo MPU. This disables the power amplifier, allowing the heads to float freely over the disks. The seek error condition cannot be cleared except by a controller RTZ command (see Communicating Errors, earlier in this section). An attempt to perform a read or write operation while the seek error condition exists results in the generation of a Read or Write and Off Cylinder fault.

OPERATOR PANEL AND STATUS/CONTROL PANEL FUNCTIONS

Although the optional operator panel and the status/control panel have functional differences, much of their circuitry is identical. As shown in figures 7-6 and 7-7, both panels connect to control board circuitry primarily through the control bus (Address/Data bus) for the Control MPU. The Control MPU senses when switches on the panel are pressed and provides inputs that drive the indicators on the panel.

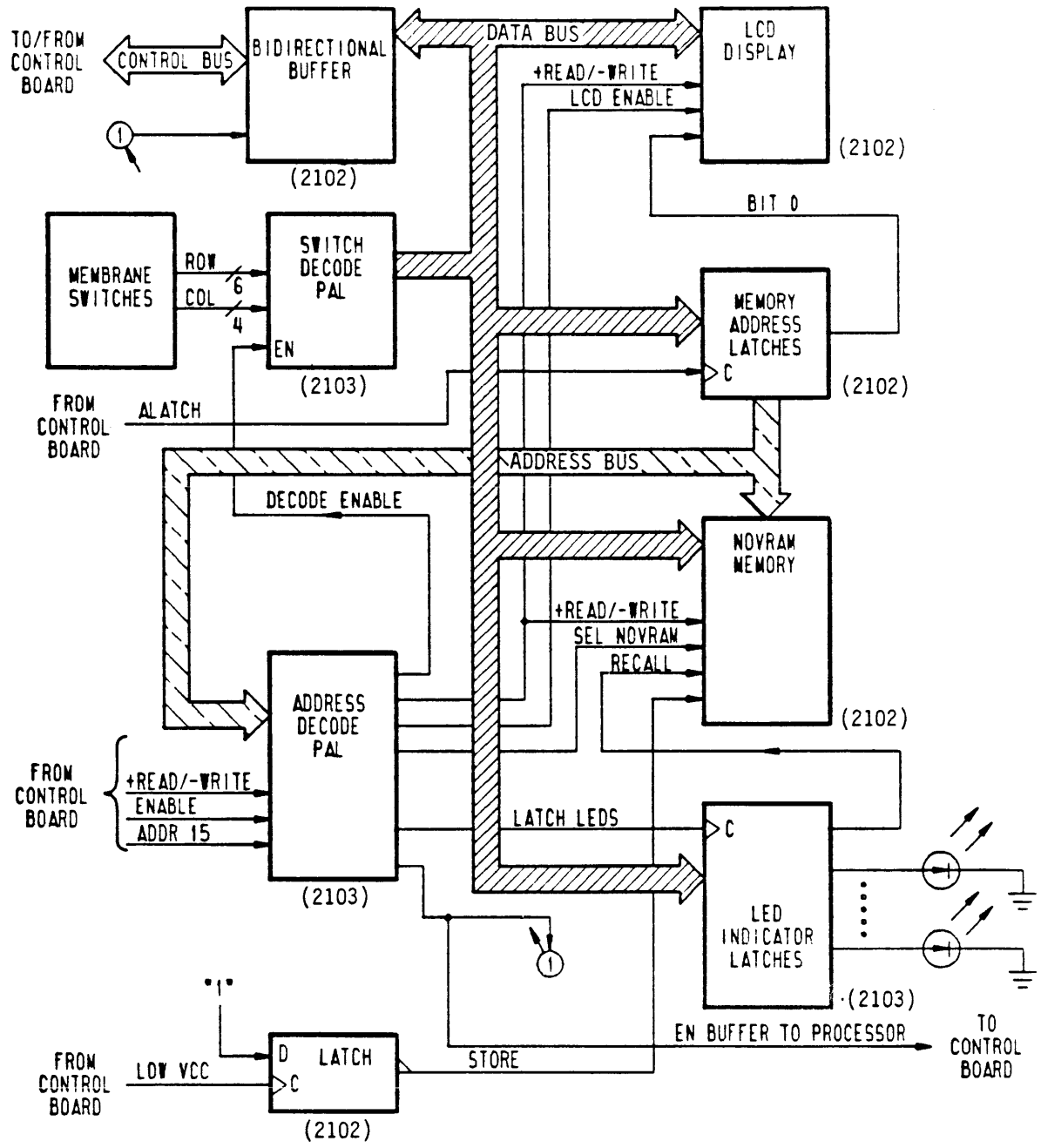


Figure 7-6. Status/Control Panel Block Diagram

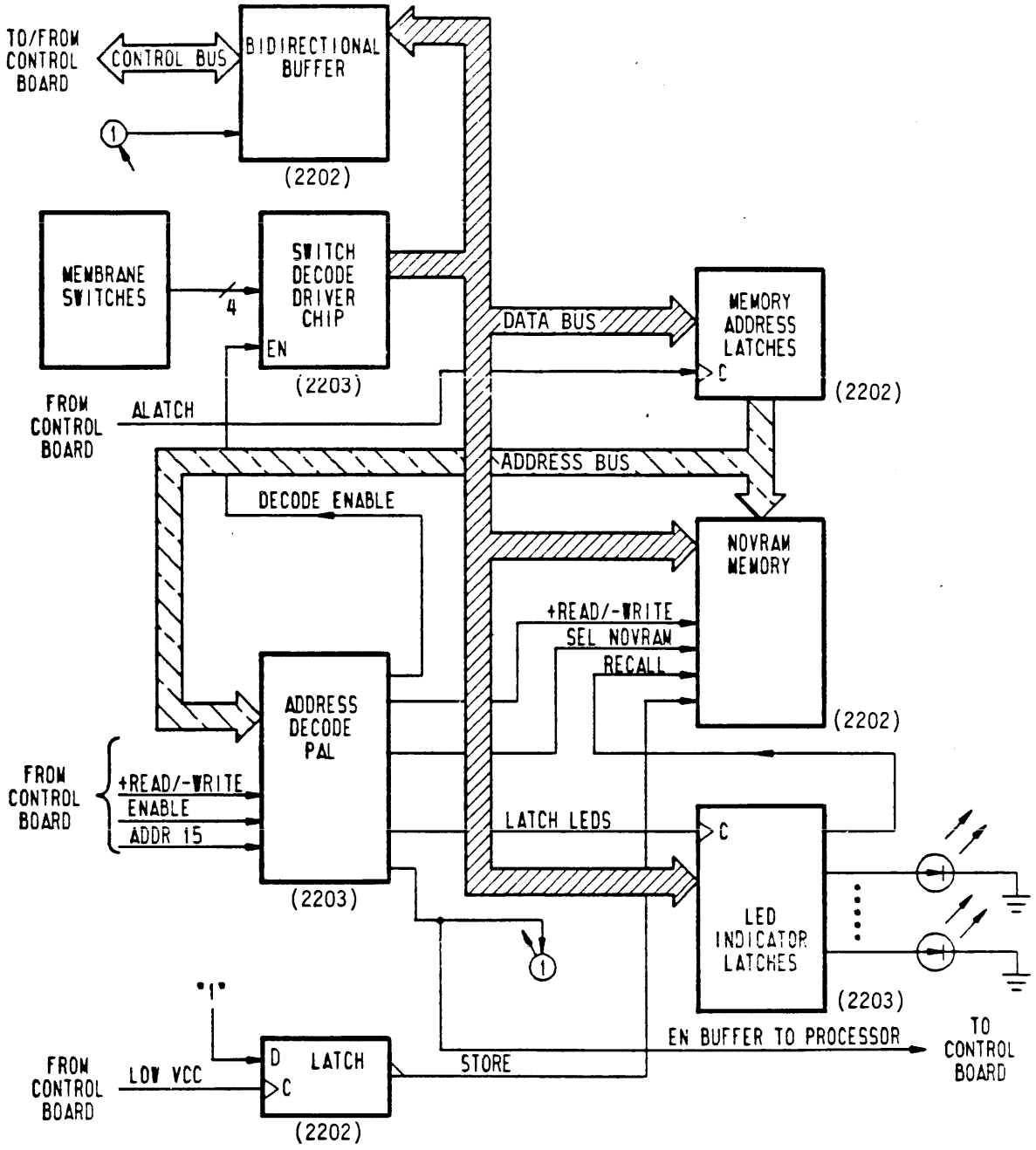


Figure 7-7. Operator Panel Block Diagram

As described in section 2 under Microprocessor Control System Functions, many functions of the Control MPU take place under its timer interrupt routine. These functions include the communications with the operator panel or status/control panel. Through the timer interrupt routine, the switches on the panel are checked at 30-millisecond intervals. If necessary, the LED indicators on both panels and the liquid crystal display (LCD) on the status/control panel are updated every 30 milliseconds also.

The Control MPU uses address decodes to activate various control signals on the panel. The panel contains an eight-bit register that latches the lower eight address bits during each MPU cycle. These eight bits and several other signals from the Control MPU are applied to the Address Decode PAL. The PAL issues the following signals:

- The Latch LEDs signal clocks the register that drives the LED indicators on the panel. The Control MPU supplies data inputs to the register on its data bus.

- The Select NOVRAM signal is a chip select for the nonvolatile RAM (NOVRAM) memory chip. As described below, this chip stores certain switch settings and LED indications when dc power is lost.

- The Decode Enable signal gates the status of the membrane switches onto the data bus. The switches on the operator panel supply individual inputs to a driver chip. On the status/control panel, the switches supply matrixed inputs to the Switch Decode PAL.

- The +Read/-Write signal that controls the direction of data transfer on the panel's bus. With the signal low, the Control MPU transfers data to a peripheral chip.

- The Enable Buffer to Processor signal enables bus transfers from the panel to the control board.

- The LCD Enable signal is a chip select for the liquid crystal display (on the status/control panel only). This chip displays status and diagnostic messages in two rows of alphanumeric characters.

As mentioned above, the nonvolatile RAM keeps a record of which switches were pressed and which LEDs were lit prior to a loss of dc power. For example, if the power supply is turned off and later turned back on, the LEDs will continue to show the same logical address and write protect status. Even though the START switch has momentary action, the last use of the switch (either starting or stopping the drive) will continue to be in effect when power is reapplied.

The nonvolatile RAM offers both RAM and ROM storage. During normal operation, the Control MPU addresses the RAM portion of the chip and updates information as needed. As dc voltages drop during a power loss (or power supply shutdown), the Low Vcc signal goes active and sets a latch. This latch activates the Store signal to the nonvolatile RAM. The Store command causes all data stored in the RAM portion to be transferred to the ROM portion of the chip. On power up, the Control MPU activates the Recall line. The Recall command causes the data to be copied from the ROM portion back into the RAM portion of the chip.

These panels are optional in the sense that the drive can function with no panel installed. If no panel is installed, switches on the control board determine the drive's logical address and write protect status; power sequencing depends on the presence of dc power and, in local mode, of sequence power signals from the controller.

The OEM Operator Panel connector, located on SMD and IPI I/O boards, offers the possibility of connecting a customer-designed operator panel to the drive. Magnetic Peripherals does not offer an optional operator panel using this connection.

DIAGNOSTIC FUNCTIONS

All drives, regardless of their interface, offer a series of offline diagnostic tests via the optional status/control panel. The maintenance manual has information on running and interpreting these diagnostic tests. Each interface provides diagnostic options also. They are outlined in the following paragraphs.

TESTING SMD-E INTERFACE DRIVES

Two diagnostic functions are performed in response to the appropriate Tag 5 Bus Out Bit decode (refer to table 3A-4).

The Diagnostic FRU Status command presents a code to the controller indicating the field replaceable unit (FRU) that most likely failed. The codes are presented on Bus In Bits 0-3 with Bus In Bit 7 indicating that status is valid. Refer to table 3A-4 for codes and FRUs.

The Execute Diagnostic Test command clears past drive status logs and attempts to execute the following diagnostic tests:

- Return to Zero Seek (RTZ)
- Single Track Seek
- Servo Recalibrate (MPU)
- Maximum Seek

Execution stops when the test sequence is complete or if an error occurs.

Tag 5 must be active with Bus Out Rits 0 and 1 active until Bus In Bit 7 is active, indicating diagnostic execution has begun. During test execution Seek End is inactive. When execution stops, Seek End is active.

TESTING SCSI INTERFACE DRIVES

The SEND DIAGNOSTIC RESULTS command (1D) and RECEIVE DIAGNOSTIC RESULTS command (1C) can be used to perform tests to determine what field replaceable unit (FRU) most likely failed. The SEND DIAGNOSTIC RESULTS command causes the controller to perform diagnostic tests on itself, the drive, or both. This command is usually followed by a RECEIVE DIAGNOSTIC RESULTS command.

The codes for the four most likely FRUs are reported in bytes 2 through 5 of of the RECEIVE DIAGNOSTIC RESULTS command. An error code, indicating what part of a diagnostic operation failed, is reported in bytes 6 and 7 of the command. Refer to the maintenance manual for information about how to run and interpret diagnostic tests.

TESTING IPI INTERFACE DRIVES

Online IPI diagnostics are initiated through the IPI interface using the Load Drive Function bus control (01) with the Execute Internal Diagnostics function (29). The following diagnostic tests are included:

- Servo Test
- Random Seeks
- Return to Zero
- Seek to Diagnostic Cylinder
- Head Select Test
- Write/Read Test

The write/read diagnostic test can occur only if it is enabled by a switch setting on the I/O board. Only the read portion of the test will run if the drive is write-protected. The other tests require that the drive must be ready with no faults active.

If failures occur during online diagnostics, use the Read Drive Specific Information bus control (43) to read status codes, fault codes, and FRU codes. For detailed listings of these codes, refer to the maintenance manual.

COMMENT SHEET

Manual Title:

Publication No: **Revision:**

Name: _____

Company: _____

Street Address: _____

City: _____ **State:** _____ **Zip Code:** _____

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