83325420 A

CONTROL DATA CORPORATION

CDC® EIGHT-INCH MODULE DRIVE

PA8A2

THEORY OF OPERATION
GENERAL MAINTENANCE INFORMATION
TROUBLE ANALYSIS
ELECTRICAL CHECKS
REPAIR AND REPLACEMENT

Volume 2

HARDWARE MAINTENANCE MANUAL

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LIST OF EFFECTIVE PAGES

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PREFACE

This manual contains maintenance information for the CONTROL DATA® PA8A2 Eight-Inch Module Drive (EMD). It is prepared for customer engineers and other technical personnel directly involved with maintaining the EMD.

The information in this manual is presented as follows:

- Section 1 - Theory of Operation. Describes power functions, electromechanical functions, interface, unit selection, servo surface decoding, sector detection, seek functions, head selection, read/write functions, and fault detection.
- Section 2 - General Maintenance Information. Contains information on warnings and precautions, maintenance tools and materials, testing the drive, and accessing the drive for maintenance.
- Section 3 - Trouble Analysis. Contains procedures and information to assist in troubleshooting the drive.
- Section 4 - Electrical Checks. Provides electrical test procedures.
- Section 5 - Repair and Replacement. Contains procedures and information on the replacement and adjustment of drive assemblies.

The following manuals apply to the EMD and are available from Control Data Corporation, Literature Distribution Services, 308 North Dale Street, St. Paul, MN 55103:

Publication No.	Title
83325410	PA8A2 Hardware Maintenance Manual, Volume 1 (contains general description, operation, installation and checkout information, and parts data)
83325420	PA8A2 Hardware Maintenance Manual, Volume 2
83325430	PA8A2 Hardware Maintenance Manual, Volume 3 (contains diagrams)

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IMPORTANT SAFETY INFORMATION AND PRECAUTIONS

Proper safety and repair is important to the safe, reliable operation of this unit. Service should be done by qualified personnel only. This maintenance manual describes procedures recommended by the manufacturer as effective methods of servicing the unit. Some of these procedures require the use of specially designed tools. For proper maintenance and safety, these specially designed tools should be used as recommended.

The procedures in this maintenance manual and labels on the unit contain warnings and cautions which must be carefully read and observed in order to minimize or eliminate the risk of personal injury. The warnings point out conditions or practices that are potentially hazardous to maintenance personnel. The cautions point out practices which, if disregarded, could damage the unit and make it unsafe for use.

For the safety of maintenance and operating personnel, the following precautions must be observed:

- Perform all maintenance by following the procedures given in this manual and using only CDC/MPI replacement parts.
- Read and observe all cautions and warnings provided in the procedures and labeled on the unit.
- Use the special tools called out in the maintenance procedure.
- Observe sound safety practices when performing maintenance.
- Use caution when troubleshooting a unit that has voltages present. Remove power from unit before servicing or replacing components.
- Wear safety glasses when servicing units.
- Wear safety shoes when removing or replacing heavy components.

It is also important to understand that these warnings and cautions are not exhaustive. The manufacturer could not possibly know, evaluate and advise maintenance personnel of all conceivable ways in which maintenance might be performed or the possible risk of each maintenance technique. Consequently, the manufacturer has not completed any such broad evaluation. Thus, any persons who use any non-approved maintenance procedure or tool must first satisfy themselves that neither their safety nor the unit performance will be jeopardized by the maintenance techniques they select.

ABBREVIATIONS

A	Ampere
ABV	Above
ac	Alternating Current
ADD	Address
ADDR	Address
ADJ	Adjust
ADRS	Address
AGC	Automatic Gain Control
ALT	Alternate
AM	Address Mark
AME	Address Mark Enable
AMP	Amplifier, Ampere
ASSY	Assembly
BLW	Below
C	Celsius
CB	Circuit Breaker
CDA	Complete Drive Assembly
CDC	Control Data Corporation
CH	Channel
CHK	Check
CLK	Clock
CLR	Clear
cm	Centimeter
CNTR	Counter
COMP	Comparator
CONT	Control
CONTD	Continued
CT	Center Tap
CYL	Cylinder
D/A	Digital to Analog
dc	Direct Current
DET	Detect
DIFF	Differential
DIV	Division
DLY	Delay
DRVR	Driver
ECL	Emitter Coupled Logic
ECO	Engineering Change Order
EMD	Eight-Inch Module Drive
EN	Enable

ABBREVIATIONS (Contd)

ENBL	Enable
EXT	External
F	Fahrenheit, Fuse
FCO	Field Change Order
FDBK	Feedback
FIG	Figure
FLT	Fault
ft	Foot
FTU	Field Test Unit
FWD	Forward
GND	Ground
HD	Head
HEX	Hexagon
Hg	Mercury
HR	High Resolution
HYST	Hysteresis
Hz	Hertz
IC	Integrated Circuit
IDENT	Identification
in	Inch
IND	Index
INTRPT	Interrupt
I/O	Input/Output
IPB	Illustrated Parts Breakdown
IPS	Inches per Second
kg	Kilogram
kPa	Kilopascal
kW	Kilowatt
lb	Pound
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSI	Large Scale Integration
LTD	Lock to Data
m	Meter
MAX	Maximum
MB	Megabyte
MEM	Memory
MHz	Megahertz
mm	Millimeter

ABBREVIATIONS (Contd)

MPI	Magnetic Peripherals, Inc.
MPU	Microprocessor Unit
MRK	Mark
ms	Millisecond
MTR	Motor
mV	Millivolt
NC	No Connection
NORM	Normal
NRZ	Non Return to Zero
ns	Nanosecond
OC	On Cylinder
OS	One-Shot
OSC	Oscillator
P	Plug
PD	Peak Detect
pF	Picofarad
PFTU	Programmable Field Test Unit
PG	Page
PHH	Phillips Head
PLO	Phase Lock Oscillator
PROC	Procedure
PROG	Programmable
PS	Power Supply
PWR	Power Supply
RCVR	Receiver
RD	Read
RDY	Ready
REF	Reference
REQ	Request
RES	Resolution
REV	Reverse, Revision
RGTR	Register
r/min	Revolutions Per Minute
RTZ	Return to Zero
R/W	Read/Write
s	Second
S/C	Series Code
SEC	Second
SEL	Select

ABBREVIATIONS (Contd)

SEQ	Sequence
SPD	Speed
SS	Sector Switch
T	Tracks to go
TF	Thread Forming
TIM	Timer
TP	Test Point
TSP	Troubleshooting Procedure
TTL	Transistor-Transistor Logic
V	Volts, Voltage
Vbb	Bias Voltage
VCC	Bias Voltage
VCO	Voltage Controlled Oscillator
W	Watts
W/	With
W/O	Without
W PROT	Write Protect
W+R	Write or Read
W·R	Write and Read
WRT	Write
XFR	Transfer
Ω	Ohms
$	Hexadecimal Address
uF	Microfarad
us	Microsecond

SECTION 1

THEORY OF OPERATION

INTRODUCTION

The theory of operation section describes drive operations and the hardware used in performing them. It is divided into the following major areas (refer to figure 1-1):

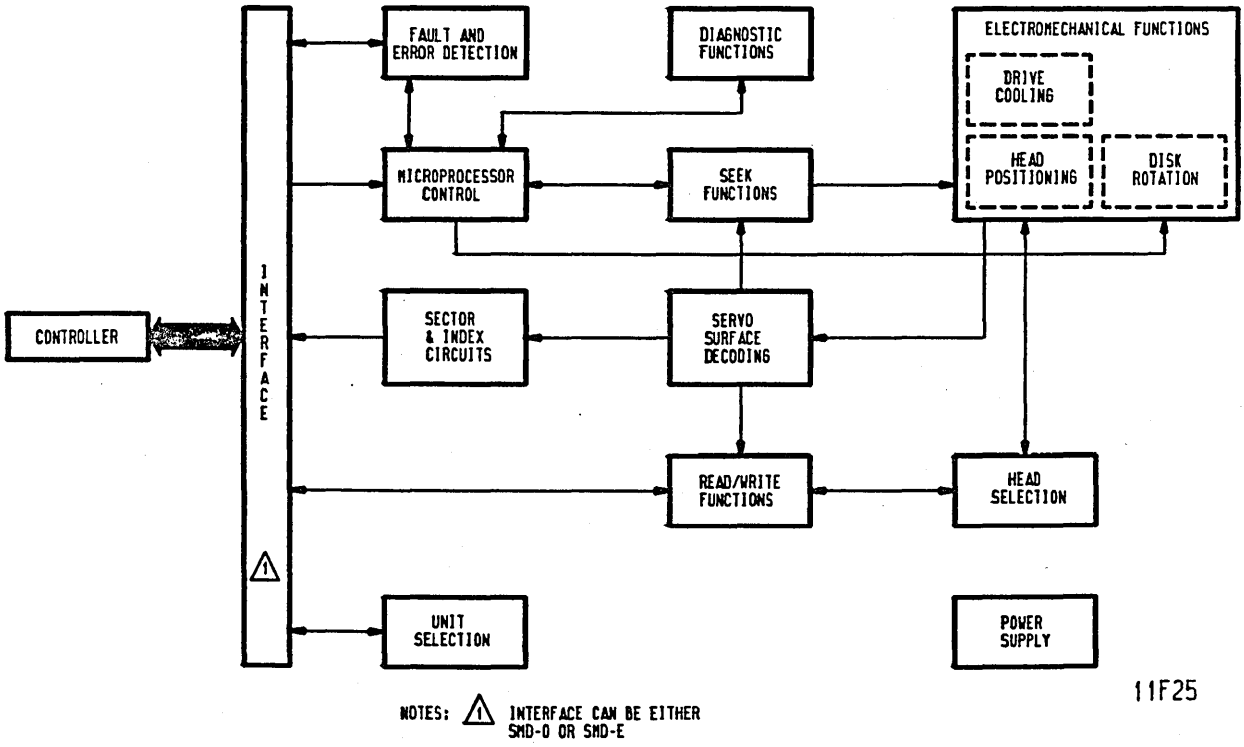

Figure 1-1. Drive Functional Block Diagram

- Microprocessor Control System Functions - Describes the operations performed by the control firmware resident in the Control MPU.

- Power Functions - Describes how the drive provides the voltages necessary for drive operation.

- Electromechanical Functions - Provides a physical and functional description of the mechanical and electromechanical portions of the drive disk rotation, head positioning, and air flow systems.

- Interface - Describes the signal lines connecting the drive and controller. It also describes the I/O signals carried by these lines and how they are processed by the drive logic.

- Unit Selection - Explains how the controller logically selects the drive so the drive will respond to controller commands.

- Servo Surface Decoding - Explains how the decoding of the data read from the servo surface by the servo head is used to locate the radial position of the heads during a seek movement, the rotational position of the disks (indicated by the Index signal) when the heads are on track, and the exact speed of the disks (indicated by the 2.41/1.612 MHz clock signal).

- Sector Detection - Explains how the drive derives the sector pulses that are used to determine the angular position, with respect to index, of the read/write heads.

- Seek Functions - Explains how the servo logic controls the movements of the head positioning mechanism in positioning the heads over the disks.

- Head Selection - Explains the head selection process.

- Read/Write Functions - Describes how the drive processes the data that it reads from and writes on the disk.

- Fault Detection - Describes the conditions that the drive interprets as faults.

- Status/Control Panel Functions - Describes the functions associated with the status/control panel switches and indicators.

- Diagnostic Functions - Describes the drive's capabilities to transmit and display diagnostic information.

The descriptions in this section are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in volume 3 of the hardware maintenance manual should take precedence over those in this section if there is a conflict between the two.

MICROPROCESSOR CONTROL SYSTEM FUNCTIONS

The three microprocessors in the microprocessor control system control all of the major operations of the drive except head selection and read/write functions. All operations in the microprocessor control system are performed under the direction of firmware resident in the Control MPU. The following paragraphs describe the operations performed by the control firmware. A description of the operations performed by the Motor MPU firmware can be found under Electromechanical Functions. Detailed descriptions of the operations performed by Servo MPU firmware can be found under Seek Functions. Figure 1-2 shows the major hardware components comprising the microprocessor control system.

All functions performed by the control firmware, except drive initialization, are interrupt driven. Three interrupt routines are provided: a timer interrupt, an I/O interrupt, and a servo interrupt. At the conclusion of initialization, the program enables the three interrupt routines and then branches to an idle routine to wait for an interrupt.

The timer interrupt routine is used to poll the operator switches and indicators on the status/control panel, check motor speed, initiate and control power sequencing, check the Servo MPU, initiate diagnostic tests, and update the liquid crystal display on the status/control panel. The timer interrupt routine is divided into six sections and one section is executed at each timer interrupt. The routine is programmed to generate an interrupt every 4.9 milliseconds. Execution sequence is fixed to ensure that each section is repeated every 30 milliseconds.

The I/O interrupt routine is used to process commands from the controller that require microprocessor assistance. The routine is divided into five sections to handle the following types of interrupt requests: RTZ, seek offset, execute diagnostics, and

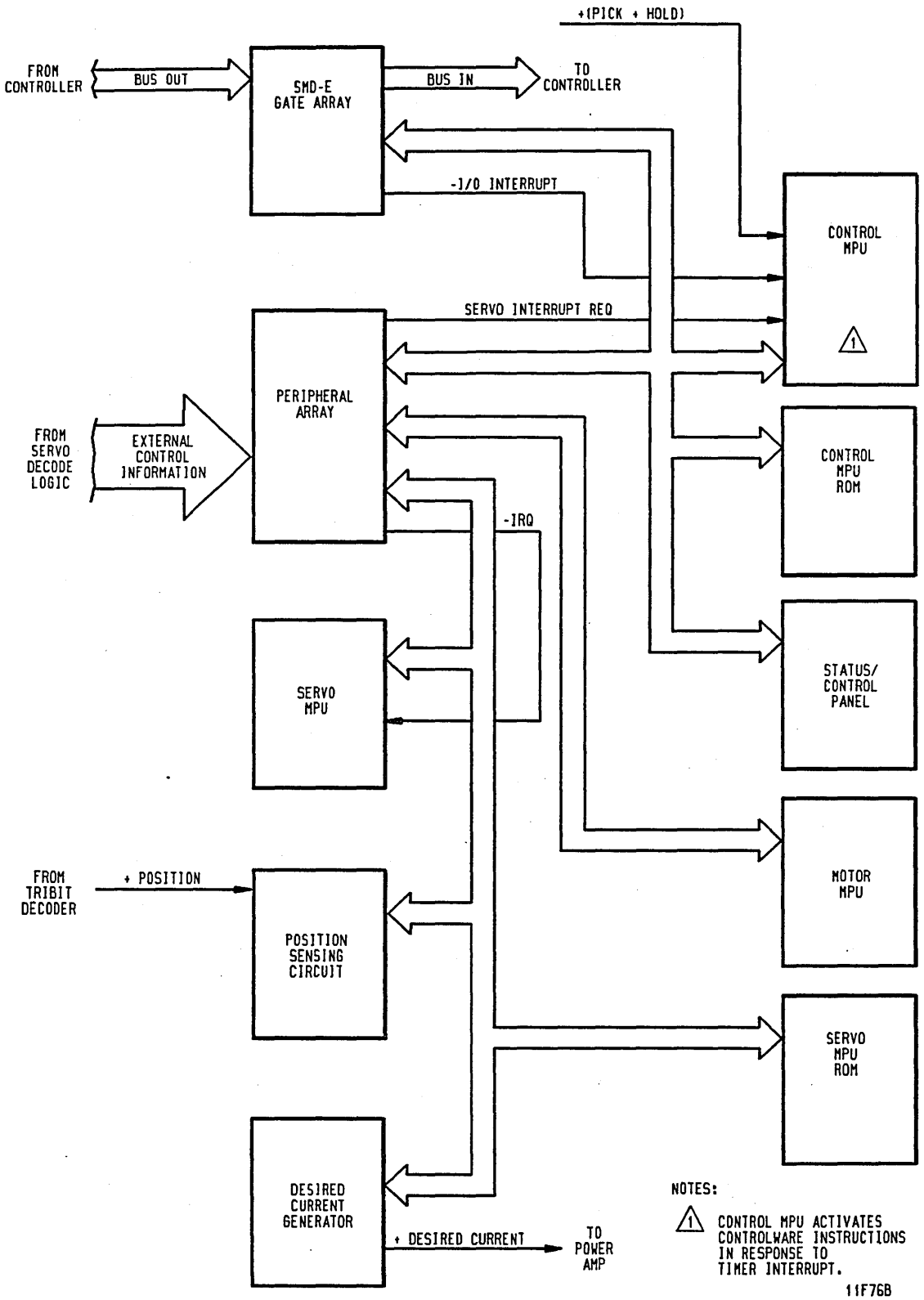

Figure 1-2. Microprocessor Functions Block Diagram

status request (operating and diagnostic status). Those sections that initiate servo operations all operate by sending a command (and operand, if required) to the Servo MPU and then waiting for a response. In addition, the routine times out these servo routines and terminates them if they take too long to complete. Finally, the routine determines whether the servo operation completed successfully, and then sends the appropriate signal to the controller.

As a precondition, normal seek, RTZ, and offset commands require unit ready status. Diagnostic execute status under Tag 5 can be requested only when the motor is up to speed. Tag 5 diagnostic and operating status can be requested at any time.

The servo interrupt routine is used to process status responses from the Servo MPU to the Control MPU. Following a command by the Control MPU to perform a servo operation, the Servo MPU sends status to the Control MPU to tell it if the operation was completed successfully.

Interrupt priority is as follows: 1. servo interrupt, 2. timer interrupt, 3. I/O interrupt. If two interrupts are received at the same time, the higher priority interrupt is serviced first. After processing the interrupt, the control program returns to the idle routine.

POWER FUNCTIONS

GENERAL

Power functions are processes that take place within the power supply and the drive when the drive is powered up and powered down. These processes depend on whether the drive is set up for local or remote operation. The power up and power down sequences are controlled by firmware resident in the Control MPU that monitors whether start conditions are present and whether certain interlock and operating conditions are satisfactory. The following areas of the power functions will be discussed in detail:

- Power Distribution -- Describes how power is distributed to the drive circuitry.
- Local/Remote Power Sequencing -- Explains how the drive may be powered up either by switch selection on the drive status/control panel or by a signal line from the controller.
- Power On Sequence -- Describes how the drive circuitry is initialized when power is applied and how the drive is prepared for normal operation.

- Power Off Sequence -- Describes how the drive is powered down, including unloading the heads and stopping the disk rotation.

POWER DISTRIBUTION

The power supply provides the drive with basic dc supply voltages shown in figure 1-3. The drive itself has no ac power requirements. All drive components, including the logic, cooling fan (optional), and drive motor, are supplied with dc power. The ac power cable connects the power supply to site ac power. The power supply can be conditioned for operation with any standard ac input voltage, as described in the Installation and Checkout section of Hardware Maintenance Manual, Volume 1.

The dc power cable connects the power supply to the drive. When the On/Standby (1/0) switch is On (1), this cable transmits four basic dc supply voltages to the drive electronics. These voltages are +5 V, -5 V, +24 V, and -12 V.

All dc voltages are overcurrent protected. Overcurrent on the +24 volt source causes the power supply to shut down. However, overcurrent on the -12 volt source does not cause the power supply to shut down. Overcurrent on either the +5 volt or -5 volt source causes a reduction to zero current or a shut down of the power supply. Operation resumes without manual intervention after correction of an overcurrent condition.

An overvoltage condition on either the +5 volt or -5 volt output causes the power supply to shut down. Operation resumes without manual intervention after correction of an overvoltage condition.

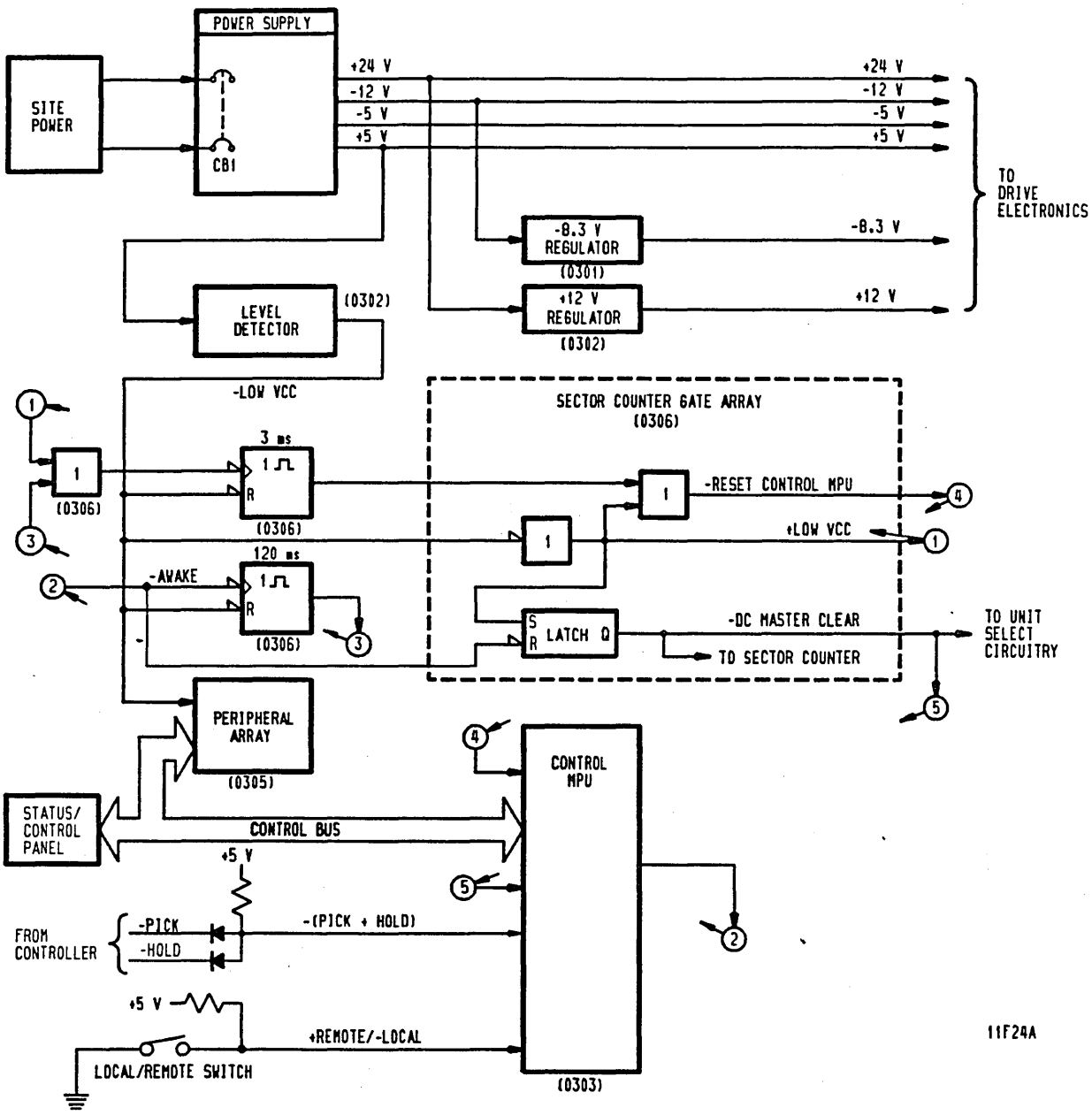

Figure 1-3. Power On Circuitry

There are three secondary power supplies on the control board that develop additional bias voltages for certain integrated circuits. One supply steps down the +24 V input and develops a regulated +12 V source. Another supply steps down the -12 V supply to develop a regulated bias of -8.3 V for the servo preamp chip. The third supply provides a +10 V reference for the voltage fault comparators.

The drive has circuitry that monitors the various supply voltages and disables write and/or servo functions when dc power is unreliable. For more information about voltage faults, refer to the Fault and Error Conditions discussion.

REMOTE/LOCAL POWER SEQUENCING

The remote/local feature selects whether or not the controller can start the drive motor and perform a load operation. Part of drive installation is setting the REMOTE/LOCAL switch (on the drive I/O board) for either local or remote operation. The REMOTE/LOCAL switch setting determines start conditions for the drive motor during power up.

With the REMOTE/LOCAL switch in LOCAL, start conditions are as follows:

- On units configured with a status/control panel, the operator must press the START switch to initiate a load operation.
- On units not configured with a status/control panel, activating the power supply initiates a load operation.

With the REMOTE/LOCAL switch in REMOTE, start conditions are as follows:

- On units configured with a status/control panel, the Sequence Pick or Hold signal from the controller must be active and the operator must press the START switch to initiate a load operation.
- On units not configured with a status/control panel, the load operation is initiated when Sequence Pick or Hold from the controller is activated.

In a system of several drives set up for remote operation, all drives receive Sequence Pick or Hold at the same time. Once Sequence Pick or Hold is received, a delay circuit in the Control MPU activates -Motor Run after an interval equal to five seconds multiplied by the drive address. Thus, each drive in the system has a unique start-up interval. However, when start conditions are removed, all drives stop their drive motors and retract heads at the same time.

POWER ON SEQUENCE

The power on sequence takes place in two steps. Power on initialization occurs when dc power is applied to the drive. Following successful initialization, a load operation occurs each time that start conditions become available. Figure 1-3 is a simplified diagram of the power on circuitry, and figure 1-4 is a flowchart of the sequence. The following paragraphs describe power on initialization in detail and summarize the load operation. More information about load operations is given under Seek Functions.

Placing the power supply On/Standby (1/0) switch to the On (1) position enables dc power to the drive. A level detector on the control board monitors the +5 V dc input from the power supply and sets the -Low Vcc line high when this input drops to +4.75 V. Until this time, the DC Master Clear latch in the Sector Counter Gate Array is set, and its output, the -DC Master Clear signal, remains low. The low -DC Master Clear signal resets the sector counter and the head address register. In addition, the low -DC Master Clear signal disables the interface by blocking unit selection. In dual channel drives, the low -DC Master Clear signal blocks unit selection by either controller.

The -Reset Control MPU line to the Control MPU goes low when -Low VCC goes low, or a hang condition in the Control MPU fails to keep the hang detect one-shot delay retriggered. When -Reset Control MPU is inactivated, the Control MPU performs the initialization routine.

The initialization routine starts by running self tests on the Control MPU and its peripheral hardware (including Servo MPU, status/control panel, and I/O gate array). If a failure occurs during self testing, the Control MPU stops and the failing component is indicated by a code displayed on the address indicators. Refer to section three for a description of these codes. With the self tests complete, the Control MPU clears the DC Master Clear latch in the Sector Counter Gate Array, initializes the peripheral hardware, and initiates the Motor MPU communication test.

At this point, power on initialization is complete. This process will not be repeated until dc power is removed and reapplied to the drive (via the On/Standby (1/0) switch). The Control MPU waits for start conditions by monitoring the START switch (if the optional status/control panel is installed), or (in remote operation) the Sequence Pick or Hold signal from the controller.

When start conditions are present, the Control MPU directs the load operation. The load operation energizes the drive motor to bring the disks up to speed and loads the heads to position

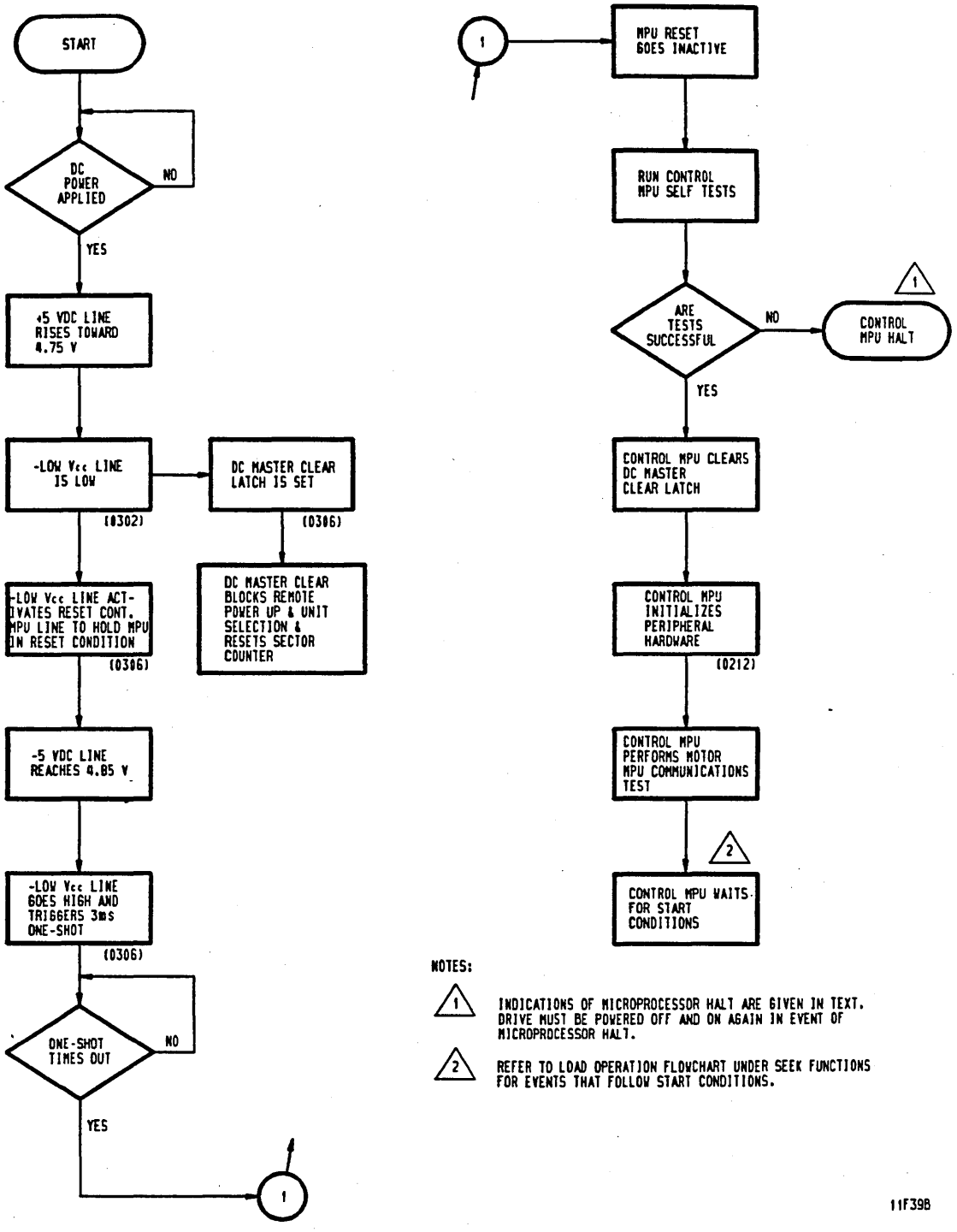

Figure 1-4. Power On Sequence Flowchart

them at cylinder zero on the disks. Details of the load operation are given under Seek Functions. When the load operation is complete, the drive waits for commands from the controller.

POWER OFF SEQUENCE

The power off sequence unloads the heads and stops the drive motor. There are two conditions that initiate a power off sequence. One is a loss of start conditions, and the other is a loss of dc power to the drive.

A loss of start conditions occurs when the START switch is pressed, or (in remote operation) when the controller deactivates Sequence Pick and Hold. The Control MPU monitors the start conditions and directs an unload operation when they are removed. An unload operation (discussed under Seek Functions) uses servo control to move the heads completely outward over the landing zone. The heads are held in this position by a retract command until the actuator is locked by the carriage latch electromagnet. The Control MPU then drops the Motor Run command. Loss of Motor Run command causes the Motor MPU to reverse the motor drive signals causing a controlled deceleration. The drive remains in this condition until start conditions reappear.

A loss of dc power results when the power supply On/Standby (1/0) switch is switched to Standby (0) or when there is a loss of site ac power. When the dc voltages drop, an emergency retract takes place under hardware control. The emergency retract operation (described under Power Amplifier in Seek Functions) requires no Control MPU intervention, and it uses voltage generated by the decelerating drive motor to drive the heads outward to the landing zone. When the heads have moved outward to the landing zone, the carriage latch electromagnet automatically holds them in this position. After motor speed drops to approximately 750 r/min following a loss of dc power, the dynamic braking relay closes. Closing this relay shorts the motor stator windings together and stops drive motor rotation within 29 seconds.

ELECTROMECHANICAL FUNCTIONS

GENERAL

Certain drive functions are performed by electromechanical components. These functions include disk rotation, head positioning, and drive ventilation. Disk rotation and head positioning are controlled by drive logic circuitry. Drive ventilation is controlled by power supply circuitry.

DISK ROTATION

General

Disk rotation is accomplished by an electromechanical system that accelerates the disks to 3600 r/min during power up and stops disk rotation with reverse current braking during power down. The mechanical and electrical aspects of this system are discussed in the following paragraphs.

Mechanical Description

The mechanical components used for disk rotation are the spindle and drive motor.

Spindle

The spindle is directly coupled to the motor which is mounted inside the spindle. The disks, in turn, are mounted on the spindle assembly. When the spindle is rotated by the drive motor, the disks rotate with the spindle.

Drive Motor

The motor has a three-phase stator surrounded by a four-pole rotor. The Motor MPU (described in the next topic) provides pulsed excitation to the three stator windings. To keep the stator pulses in phase with rotor position, the Motor MPU uses feedback from three sensors located in the motor. These sensors detect flux reversals from the rotor magnets. As the rotor magnets pass each sensor, its output line toggles. The drive motor current consumption is held to 7 amperes by a current limiting circuit.

Electrical Description

General

Electrical operation of the drive motor is discussed in two functional areas:

- Motor MPU -- discusses how the drive motor is started and how its speed is regulated.
- Reverse Current Braking -- discusses how the drive motor is decelerated.

Motor MPU

The Motor MPU firmware controls the direction of rotation and speed of the drive motor. Activating the -Motor Run line to the Motor MPU starts the drive motor during the power on sequence (see Power On Sequence discussion). The Motor MPU uses the +24 V dc output of the power supply to excite the stator windings in the drive motor. The control and status lines between the Control MPU and the Motor MPU are shown in figure 1-5.

The Motor MPU checks sensors S1, S2, and S3 to determine which pair of stator windings must be energized to maintain counterclockwise rotation (viewed from logic side of module). One of the three position sensors switches on or off every 30^{o} of shaft rotation. The waveforms of S1, S2, and S3 and corresponding excitation to the stator windings are shown in figure 1-6.

Motor speed is controlled by regulating the duration of power to the stator windings. During initial acceleration, power is applied for the entire amount of time that each stator winding is active until operating speed is reached. After reaching operating speed, the Motor MPU turns off all power to each active pair of stator windings for a period of time (delay) after detecting a change of state by one of the position sensors. The active pair of stator windings is re-energized after the delay.

The length of the delay is based on several computations as follows: the actual time required to revolve through 30^{o} is measured by an 8-bit timer with a clock period of 9.6 microseconds. This computation is performed twelve times to obtain the actual speed of revolution. The minimum allowed value of revolution time is then subtracted from the actual revolution time. This value is then subtracted from the maximum allowed revolution time to produce the new delay value to be used for the next revolution. The delay value is limited to a maximum value of one millisecond to allow sufficient processing time between sensor transitions. Motor speed is maintained within the following range: 3564 r/min (16.83 ms/rev) to 3636 r/min (16.34 ms/rev).

The Control MPU requests status (motor speed, fault conditions etc.) at 30 millisecond intervals from the Motor MPU by toggling the +Motor Status Request line. The Motor MPU places the status information on the +Motor Status 0-2 lines and toggles the +Motor Toggle line to inform the Control MPU that status is available.

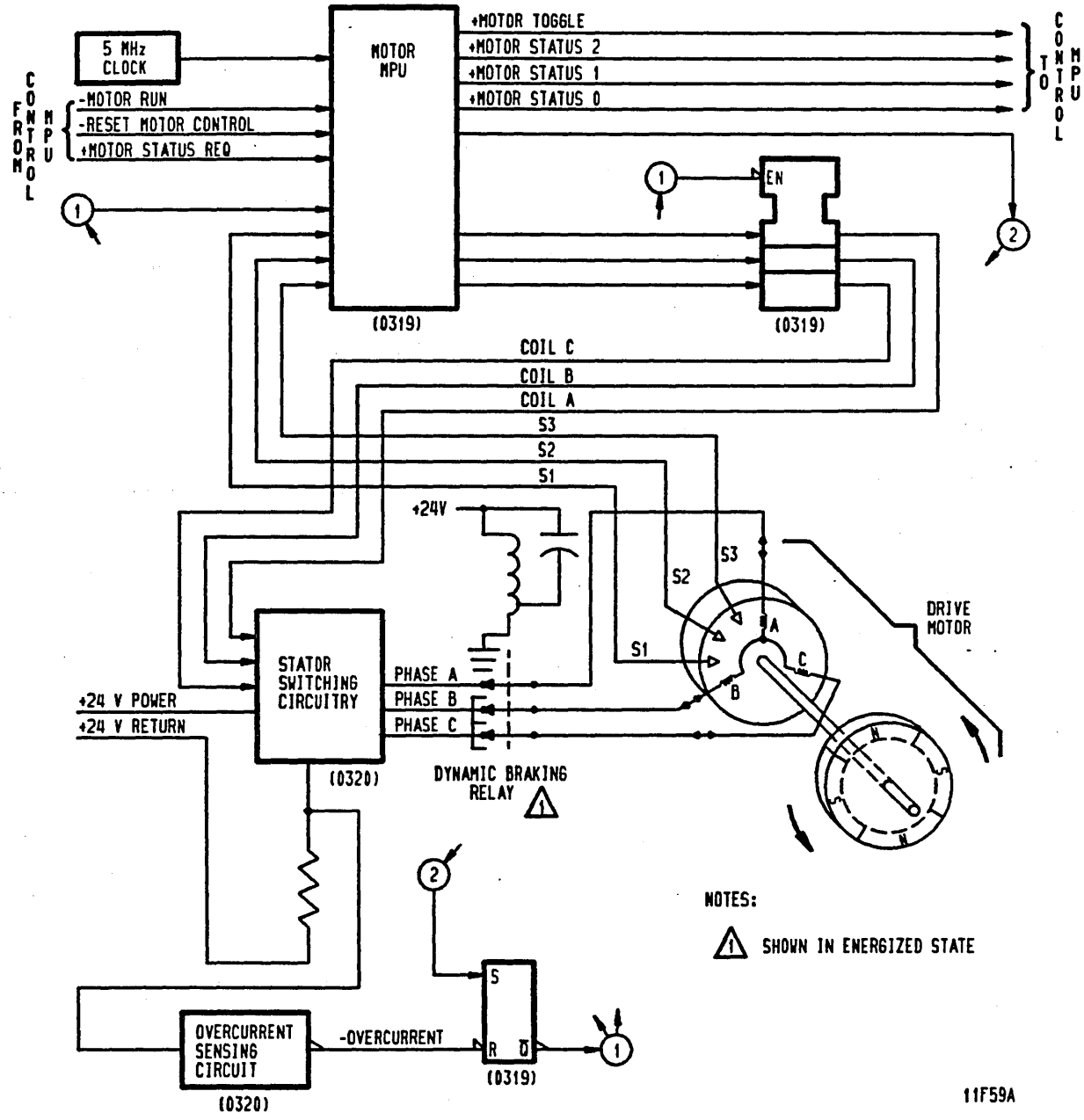

Figure 1-5. Motor Speed Control Simplified Logic

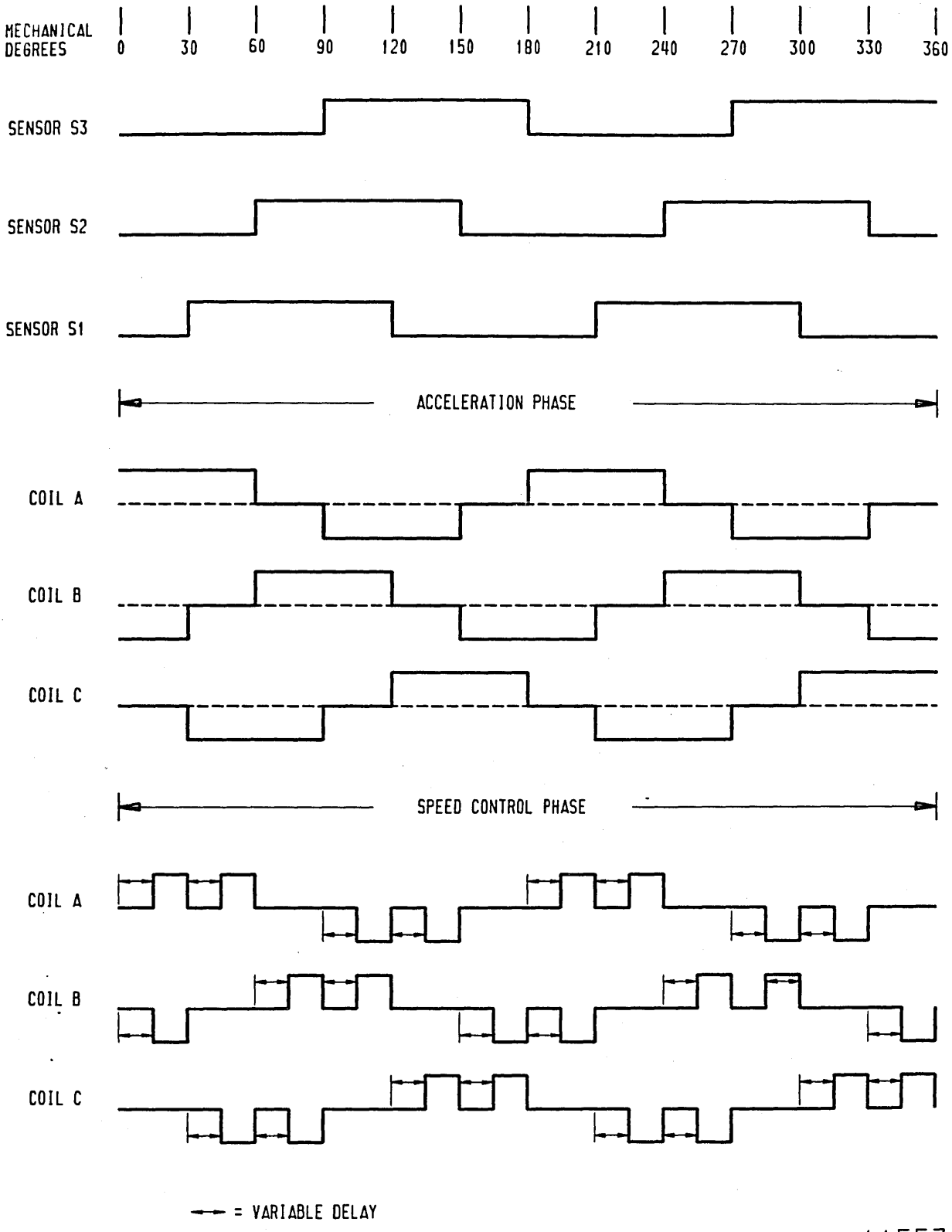

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Figure 1-6. Speed Control Waveforms and Timing

Motor speed is continuously monitored by the Motor MPU. When the spindle speed falls below 3564 r/min, the Motor MPU inactivates the Speed OK code to the Control MPU on the +Motor Status 0-2 signal lines. Inactivating this code causes the Control MPU to provide write protection by activating the +MP Write Protect line.

Write protection is needed to safeguard existing data on the disk by inhibiting the write circuitry while a motor speed error exists. The Control MPU deactivates the -Write Enable line by activating the Write Protect latch when a speed loss occurs and keeping it active for about 1/2 second after the condition is corrected.

The Control MPU also drops the Ready signal, and performs a retract operation. If a loss of speed condition occurs, the Control MPU drops the Ready signal to the controller, and the Motor MPU automatically attempts to restore motor speed.

Reverse Current Braking

Reverse current motor braking decelerates the drive motor during a power off sequence. It occurs when motor speed drops below 1000 r/min. When this happens, reverse current is gated into the motor windings with amplitude sufficient to cause the spindle to stop rotating within 44 seconds. Refer to Power Off Sequence for a description of motor braking following a loss of dc power.

The Motor MPU places a code (Motor Stopped) on the +Motor Status 0-2 lines to indicate to the Control MPU that braking is complete. This output to the Control MPU allows it to turn off the Ready indicator to show that power down is complete.

HEAD POSITIONING

General

Data is written on and read from the disk by the heads. The drive must position the heads over a specific data track before a read or write operation can be performed. Head positioning is performed by the rotary actuator mechanism which is an integral part of the drive. The actuator is controlled by inputs received from the servo circuits (refer to the discussion on Seek Functions).

Actuator and Magnet Physical Description

The actuator (shown in figure 1-7) consists of the actuator housing, the carriage and voice coil assemblies, and the head-arm assemblies. The head-arm assemblies are mounted at the forward end, and the voice coil at the opposite end, of the carriage assembly. The carriage assembly fits within and is attached to the actuator housing by means of a pivot shaft. During head positioning, the carriage rotates about the pivot thereby moving the heads out over the disk surfaces.

Whenever the drive heads are unloaded, the actuator is latched in the unloaded position with the heads over the landing zone. The actuator remains locked until the next load operation when the Control MPU energizes the carriage latch electromagnet. The automatic carriage locking feature eliminates the need to manually lock the carriage when transporting the drive.

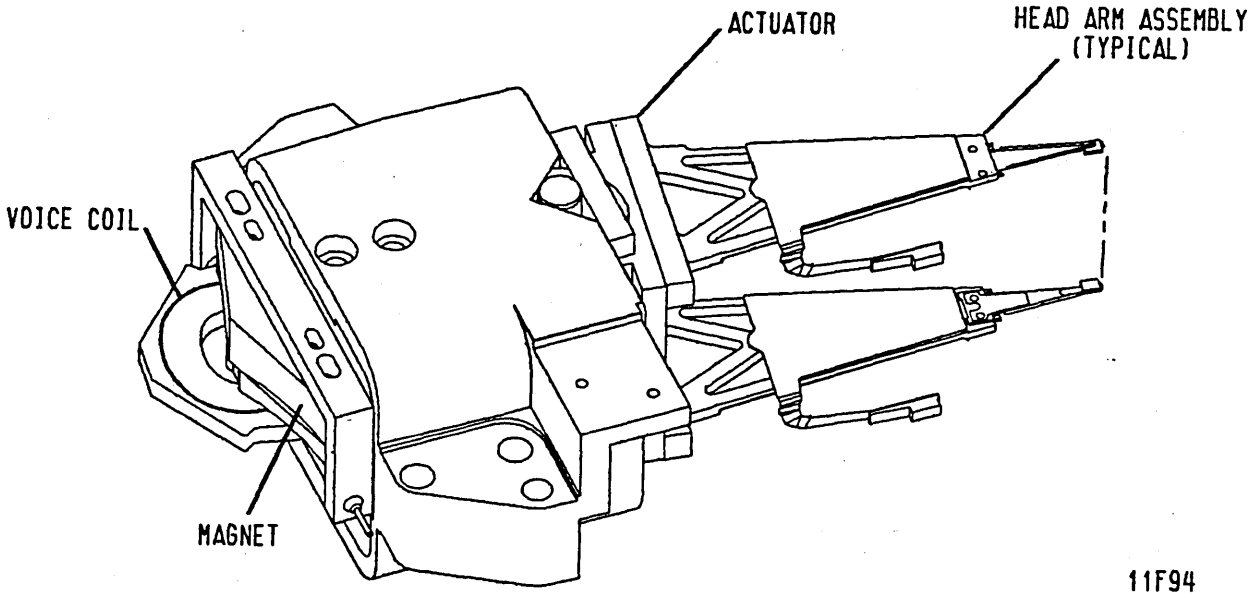


Figure 1-7. Actuator and Magnet Assembly

Actuator and Magnet Functional Description

The voice coil is mounted at the opposite end of the arm assembly and moves in and out of the magnet as the servo signals change. The magnet is mounted on the housing in a position which allows the voice coil to move as the field in the coil changes. This small in and out motion of the voice coil in the magnet provides the motion for the heads over the disk surface. The movement of the carriage and voice coil (and therefore the heads) is controlled by positioning signals from the servo logic. Positioning signals are generated by the Servo MPU and converted to analog voltage levels by the desired current generator. The output of the desired current generator is fed to the power amplifier which applies a current signal to the voice coil.

The current from the power amplifier causes a magnetic field in the voice coil which either aids or opposes the field around the permanent magnet. This reaction either draws the voice coil into the magnet or forces it away, depending on the polarity of the current through the voice coil. The acceleration of the voice coil is dependent on the amplitude of the voice coil current.

HEADS

General

The heads are magnetic devices that record data on, and read data from, the disk surface (the servo head, however, reads prerecorded data but cannot write). Up to two heads are attached to each supporting arm. The combined head and arm are called a head-arm assembly. The seven head-arm assemblies are attached to the front of the actuator assembly (figure 1-7).

The drive has 10 data heads and one servo head. Data (or read/write) heads are used to record data on and read data from the disk data surfaces. The servo head is used to read prerecorded data from the servo disk surface for use by the drive analog servo circuits.

The following paragraphs describe the physical characteristics of the movable head-arm assemblies and how they function during head load and retract sequences. Further information about the heads is found in the discussions on seek and read/write functions.

Head-Arm Assembly

Each head-arm assembly consists of a rigid arm, supporting either one or two heads on load springs and gimbal springs (figure 1-8). The head-arm assemblies are mounted at the front of the rotary actuator carriage and follow the angular motion of the carriage created by the reaction of the voice coil magnetic field to the field of the permanent magnet. The rigid arm by itself does not provide the action necessary for the heads to load or unload. A head load spring forces the associated head toward the disk surface; a gimbal spring allows the head free axial movement along its vertical and horizontal axes independent from the rigid arm.

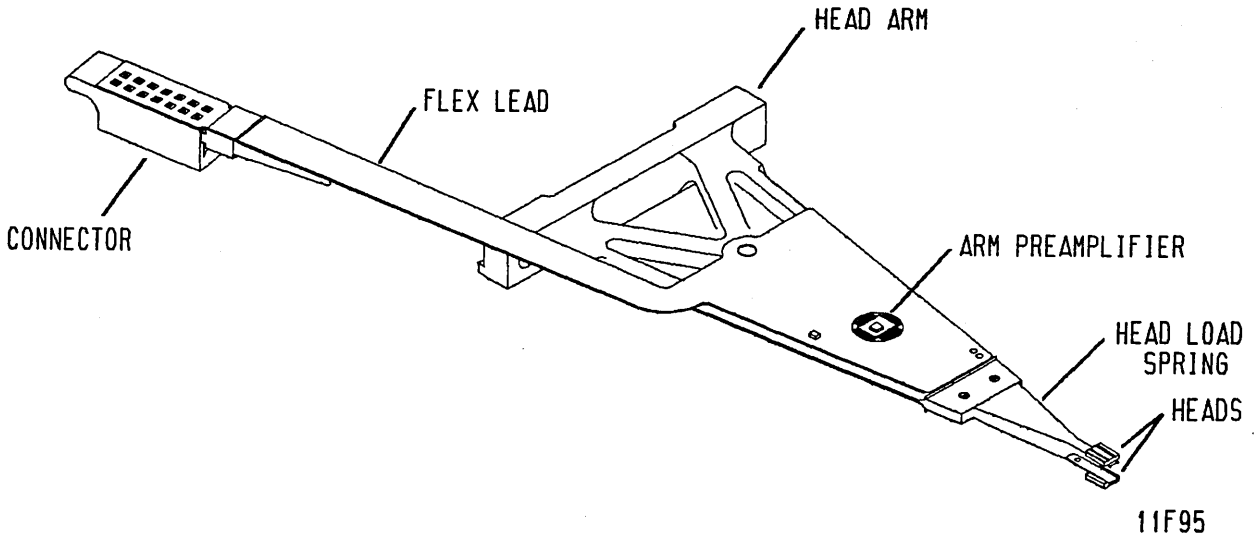


Figure 1-8. Data Heads

Read/write information is transferred to and from the heads through cables connected to a preamplifier mounted on the arm. The preamplifiers interface to the read/write circuitry via the arm matrix board, located inside the sealed module.

Head Loading

In the retract (non-operating) condition, the head load springs force their respective heads against the disk surface in the landing zones. There is one landing zone on each data surface. At their extreme outward travel, the heads are located over their respective landing zones. When the system powers up, the control firmware turns on the drive motor. When the drive motor is rotating the disks at acceptable speed, the heads move away from the disk surfaces and fly on the cushion of air created by disk rotation. At this point in the power on sequence, the rotary actuator is unlocked and the heads are moved inward to track zero. Until the power off sequence is begun, the heads continue to fly on the cushion of air.

The head load spring forces the head toward the disk surface, while the cushion of air pushes against the head to resist its closer approach. The air cushion pressure varies directly with disk speed, so that at proper speed the forces of the head load spring pressing the head towards the disk surface and the opposing force of the air cushion resisting the closer approach of the head are balanced such that the heads fly at the correct height above the disk.

If the disk drops below speed, the air cushion pressure decreases and the head load springs force the heads closer to the disk surface. Sufficient loss of speed would cause the heads to stop flying and contact the disk. This is called head landing. Because insufficient disk speed causes head landing, heads are not moved into the data areas until the disks have come up to speed. For the same reason, the heads are retracted from the data areas and locked over the landing zone when the disk speed drops below a safe operating level.

VENTILATION SYSTEM

The ventilation system is divided into two parts, one for the drive unit and the other for the sealed module.

The drive ventilation system (figure 1-9) provides continuous air replacement and circulation to dissipate the heat generated by drive operation. The main component of the drive ventilation system is the fan mounted in the optional external power supply, or the auxiliary fan accessory attached to the rear of the unit. The auxiliary fan motor is driven by the +24 V power

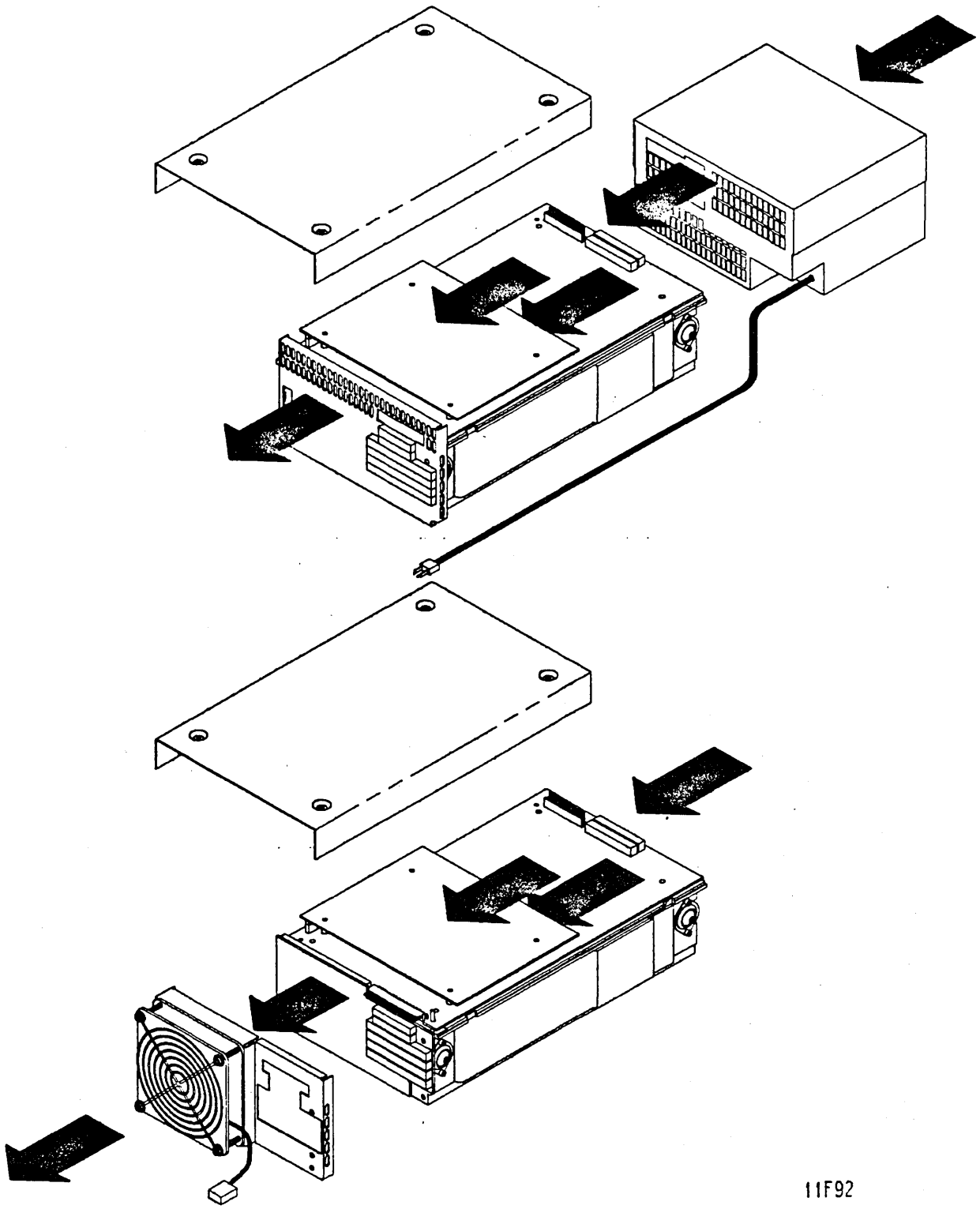


Figure 1-9. Air Flow System

from the external power supply. Either fan option moves ambient air through the drive cabinet from front to back. When incorporating the optional power supply with integral cooling fan, the air circulation travels through the power supply and then enters the front of the drive. Both fan options direct air over the drive electronics, cooling these assemblies before leaving the drive through the back of the unit.

The ventilation system for the module is a self-contained closed loop system that consists of a fan, circulation filter, and breather filter. The fan blades are located at the top of the hub assembly, and the rotation of the spindle rotates these fan blades. The motion of the blades above the hub assembly pulls air through the circulation filter into the disk area.

If the pressure within the module becomes less than the surrounding atmosphere, makeup air enters through the breather filter to equalize the pressures. Likewise, if the module pressure exceeds atmospheric pressure, air leaves the module through the breather filter.

INTERFACE

GENERAL

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals, and read/write data transfers.

The interface consists of the I/O cables and the logic required to process the signals sent between drive and controller.

The following discussion describes both the I/O cables and I/O signal processing.

I/O CABLES

The drive has two I/O cables per channel, consisting of an A cable and a B cable. These cables contain all the lines going between the drive and controller.

The A cable carries commands and control information to the drive and status information to the controller. The B cable carries read/write data, clock, and status information between drive and controller. Figure 1-10 shows all lines (except those not used) in the A and B cables. The function of each of these lines is explained in tables 1-1 and 1-2.

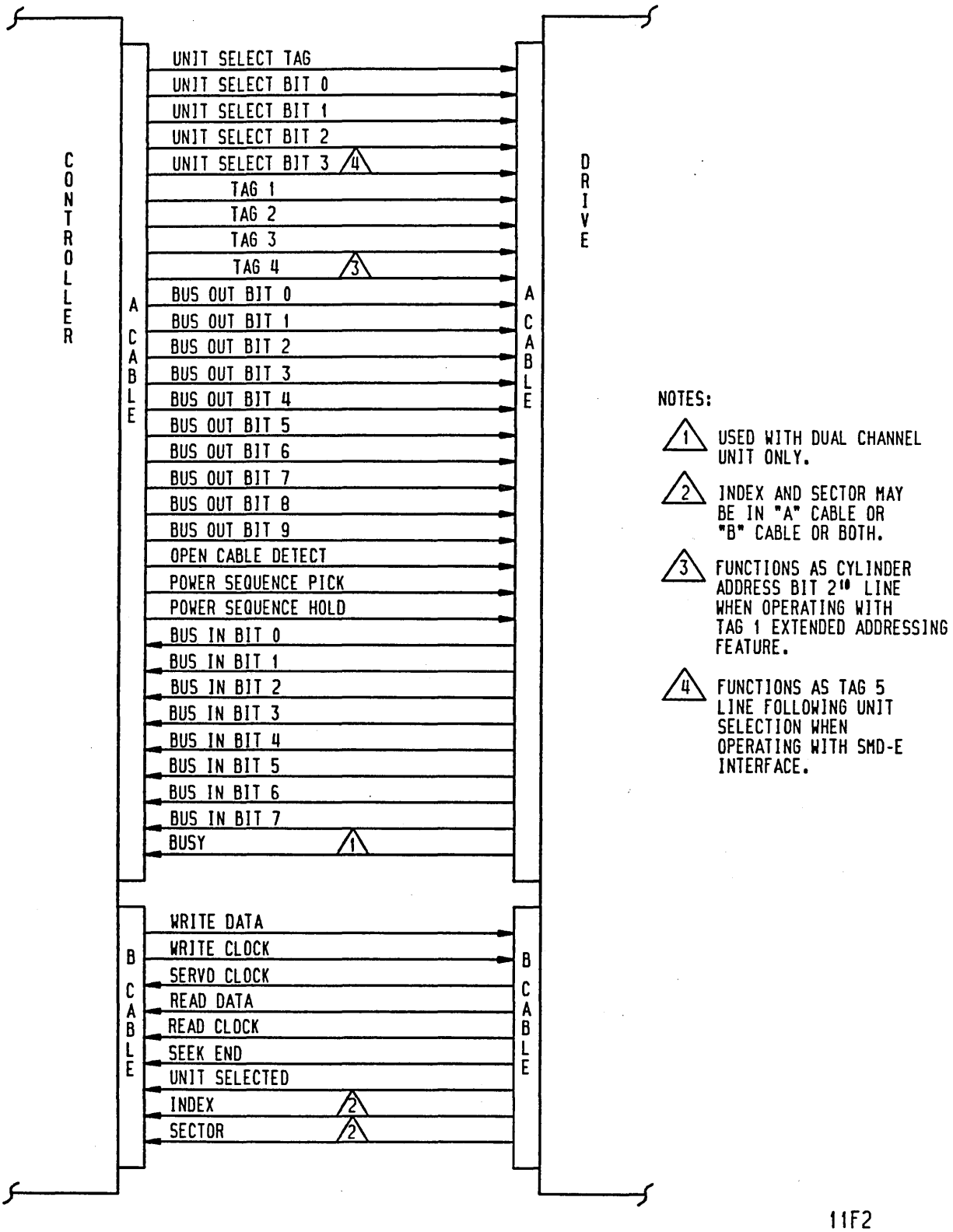


Figure 1-10. Interface Lines

TABLE 1-1. CONTROLLER TO DRIVE INTERFACE LINES

Line	Function
Sequence Pick or Hold	A ground from the controller on either of these lines starts the power on cycle on all drives in the string providing the following conditions exist: • the REMOTE/LOCAL switch is set to REMOTE, and • the START switch has been pressed to start motor (if a status/control panel is installed). These lines have no effect in the Local mode.
Unit Select Tag	This signal gates Unit Select lines into a compare circuit. The unit is selected 600 ns (maximum) after Unit Select Tag becomes active. The drive will not process commands until selected. Drive status is returned on Bus In lines while unit is selected (refer to Tag 1 Bus In description). Deselection occurs 600 nanoseconds (maximum) after Unit Select Tag drops. In dual channel units, the Unit Select Tag also causes the drive to be reserved to the issuing channel provided selection occurs. The reserve condition can be cancelled by a Release command, a reserve timeout, or by a Priority Select (i.e Unit Select Tag accompanied by proper logical address and Bus Out Bit 9 active). The drive is unconditionally selected and reserved by the channel issuing a Priority Select command provided that the issuing channel has not been disabled.
Table Continued on Next Page	

TABLE 1-1. CONTROLLER TO DRIVE INTERFACE LINES (Contd)

Line	Function
Unit Select Bits 0, 1, 2, and 3/ Tag 5	A binary code is placed on these four lines to select a drive. The binary code must match the logical address assigned to the drive. Drives can be numbered 0 through 15. Bit 3 serves a dual purpose as follows: 1. When gated with Unit Select Tag, this line must match the high order bit of the unit number for a unit selection to occur. 2. Following unit selection on drives configured with the SMD-E interface, this bit functions as the Tag 5 line.
Bus Out Bits 0-9	These ten lines carry data to the drive. The meaning of the data is a function of the active tag line.
Write Data	This line transmits NRZ data from the controller to the drive for recording on the disk surface.
Write Clock	This clock is the Servo Clock retransmitted to the drive during a write operation. Write Clock must be synchronized to the NRZ data and must be transmitted 250 ns prior to Write Gate.
Tags 1-3, Tag 4/Cyl. Addr. Bit 2^{10}	These lines carry information that is decoded by the drive tag/bus decode logic and used in conjunction with Bus Out lines 0 through 9 to produce desired functions (refer to table 1-3). When operating with the Tag 1 Extended Addressing Feature, the Tag 4 line functions as the Cylinder Address bit 2^{10} line.
Open Cable Detect	A voltage is supplied by the controller to override the bias voltage at the drive receivers. If the A cable is disconnected or if controller power is lost, unit selection and/or controller commands are inhibited.

TABLE 1-2. DRIVE TO CONTROLLER INTERFACE LINES

Line	Function
Bus In Bits 0-7	These eight lines carry status, drive identity, and current sector location information to the controller.
Busy	Used only in dual channel drives, this signal is generated when a controller attempts to select a drive that has already been selected and/or reserved by the other controller. This signal is sent to the controller attempting the selection.
Seek End	This signal indicates either on cylinder status or seek error status resulting from a seek operation that has terminated. When executing a Tag 5 Diagnostic Status operation on a drive configured with SMD-E interface, Seek End indicates that test execution is complete. In dual channel configurations, the Seek End signal to the unreserved channel is active continuously except when the unreserved channel attempts to select the drive (Tried latch set). Setting the Tried latch causes Seek End to the unreserved channel to drop for 30 microseconds when the reserved channel drops its Select and Reserve latches.
Unit Selected	This signal indicates the drive has accepted a Unit Select request. The line must be active before the drive will respond to any command from controller.
Read Data	This line transmits data recovered from the disk. The data is transmitted in NRZ form to the controller.

Table Continued on Next Page

TABLE 1-2. DRIVE TO CONTROLLER INTERFACE LINES (Contd)

Line	Function
Read Clock	This clock is derived from, and is synchronous with, the detected data. Read Clock defines the beginning of a data cell.
Servo Clock	Servo Clock is a phase-locked signal generated from the servo track tribits. The Servo Clock frequency is 14.52 MHz. Servo Clock is continuously transmitted.
Index Mark	This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero. Note: This signal may be disabled by a switch selection on the I/O board.
Sector Mark	This signal is derived from the servo tracks. The number of sector signals that occur for each revolution of the disk is selected by switches on the control board. Note: This signal may be disabled by a switch selection on the I/O board.

I/O SIGNAL PROCESSING

I/O signals from the controller initiate and control all drive operations except Local mode power on when the unit is configured with a status/control panel (refer to the discussion on Power Functions). The I/O signals are received in the drive I/O board where they are routed to the appropriate logic in the drive. In turn, the drive sends information back to the controller via drivers on the I/O board.

The drive can be configured to operate with either a standard SMD (SMD-O) interface or an enhanced SMD (SMD-E) interface. The enhanced SMD interface adds Tags 4, 5, and 6. In addition, two types of extended addressing are available with either interface type: Tag 1 Extended Addressing, and Tag 2 Extended Addressing. Because of signal line contention, SMD-E units configured with Tag 1 Extended Addressing cannot use Tags 4 and 6.

Units not configured with either extended addressing feature can address up to 1024 cylinders. Units with either extended addressing feature can address up to 1217 cylinders.

Figure 1-11 is a drive block diagram showing the I/O signal lines and their routing to and from the drive logic. When the drive is selected, the tag receivers are enabled. With the Unit Select Tag active, commands are generated based upon the tag code as defined by the Bus Out lines.

Table 1-3 provides a systematic definition of Bus Out and Bus In for each tag. The other theory discussions in this manual further define the effects of the I/O commands and the encoding of fault status and diagnostic information.

UNIT SELECTION

GENERAL

The drive must be selected before it will respond to any commands from the controller. This is the case because the tag and bus bit receivers, as well as certain drivers, are not enabled until the drive is selected.

In both single and dual channel units, the select sequence is initiated by a Unit Select Tag signal from the controller. However, the sequence performed is different depending on whether a single or dual channel is being considered. Since only one controller can communicate with the drive at a time, dual channel logic must solve the problem of priority when more than one controller wants to select the drive at the same time. The following paragraphs describe both single and dual channel selection.

SINGLE CHANNEL UNIT SELECTION

The single channel unit select sequence (see figure 1-12) starts when the controller sends the Unit Select Tag accompanied by a logical address on the four unit select lines.

When the drive recognizes the Unit Select Tag, it compares its own logical address to the address sent by the controller. The drive's logical address is determined by switch settings on the status/control panel (if installed) or by switch settings on the control board. This address can be any number from 0 to 15.

If the address sent by the controller is the same as that of the drive and if the Open Cable Detect signal is inactive (indicating the A cable is connected, controller has power, and the channel is not disabled), the drive enables its Select Compare signal.

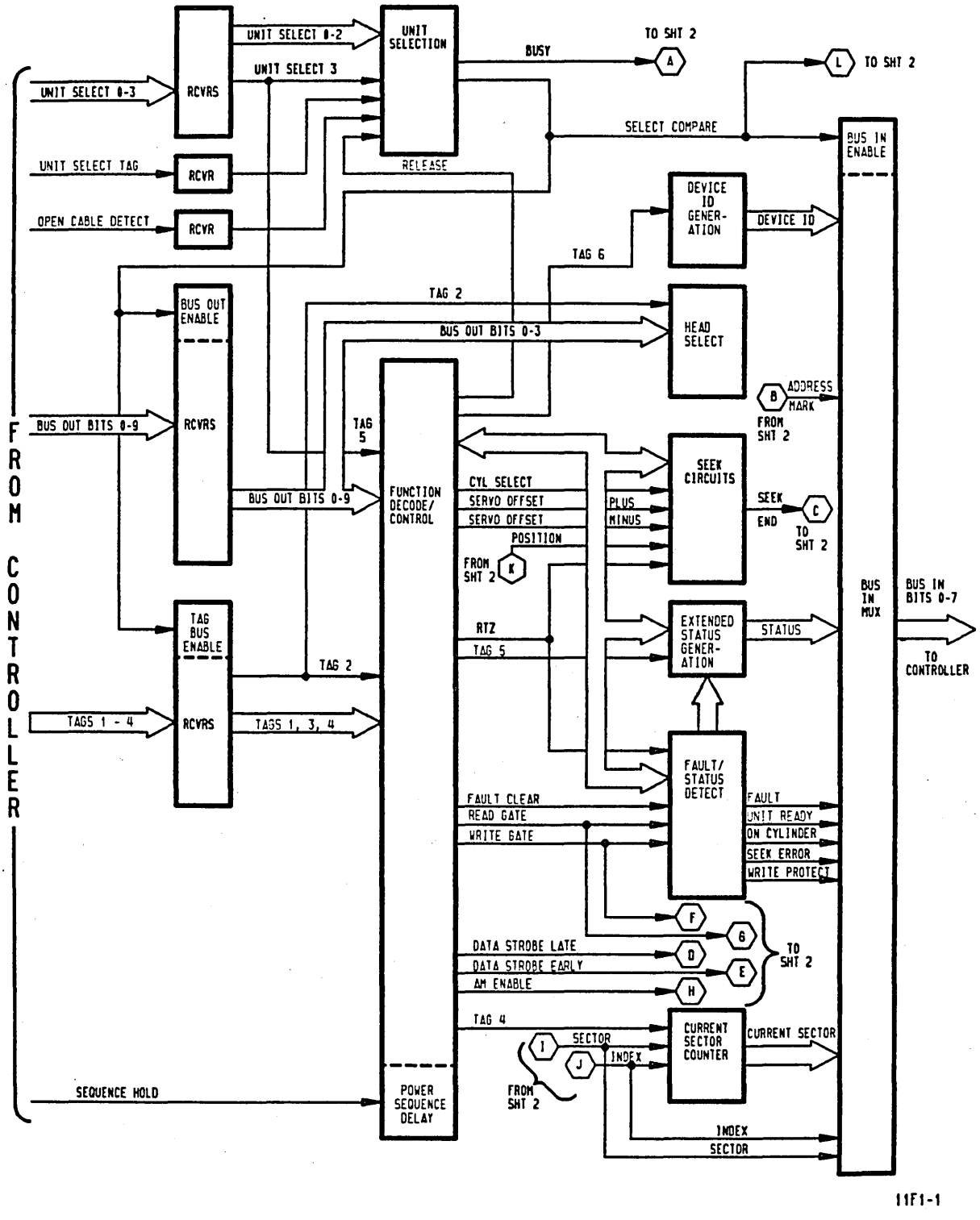


Figure 1-11. Drive I/O Signal Processing (Sheet 1 of 2)

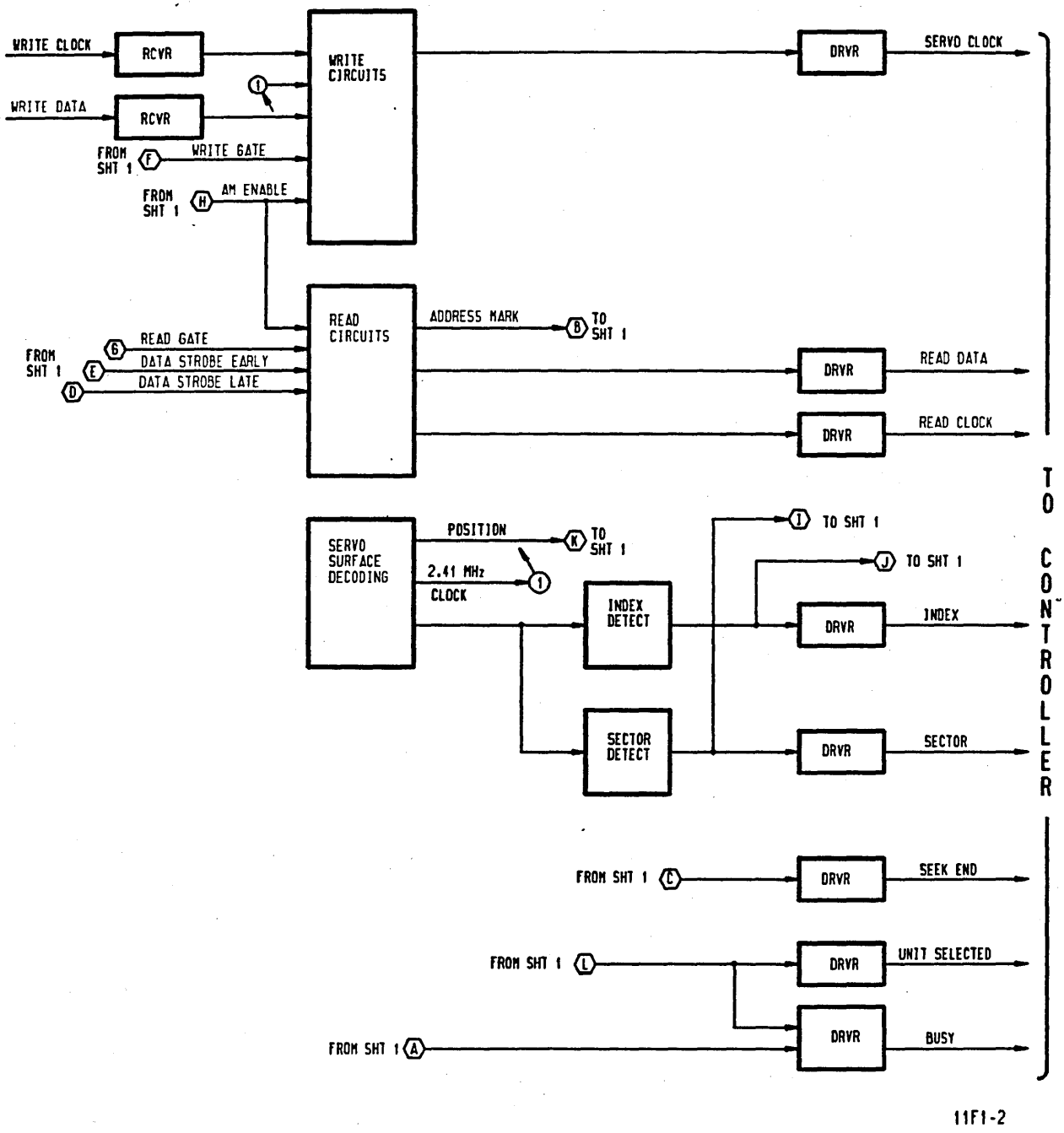


Figure 1-11. Drive I/O Signal Processing (Sheet 2)

TABLE 1-3. TAG/BUS COMMAND DECODE FUNCTIONS

I/O Signals	Function
TAG 1 -- CYLINDER SELECT/LOW CYLINDER SELECT This tag initiates a seek operation. On units not configured with the Tag 1 extended addressing feature, this tag line gates ten address lines to the drive Cylinder Address register. In addition, on units with the Tag 1 extended addressing feature, this tag gates Bit 2^{10} of the cylinder address to the drive Cylinder Address register on A cable lines 30 and 60 (Tag 4). Tag 1 extended addressing permits the user to address up to 1217 cylinders. Cylinder addresses above 1216 are illegal and will cause a seek error. On units configured with the Tag 2 extended addressing feature, Tag 2 must precede Tag 1 to ensure that the higher order cylinder address bits are gated into the Cylinder Address register before the seek is initiated. Drive status information is returned on the Bus In lines.	
Bus Out Bits	Defined as follows:
BOB0	Cylinder Address 2^0
BOB1	Cylinder Address 2^1
BOB2	Cylinder Address 2^2
BOB3	Cylinder Address 2^3
BOB4	Cylinder Address 2^4
BOB5	Cylinder Address 2^5
BOB6	Cylinder Address 2^6
BOB7	Cylinder Address 2^7
BOB8	Cylinder Address 2^8
BOB9	Cylinder Address 2^9
Bus In Bits	Defined as follows:
BIB0	Unit Ready - Unit Ready indicates that the drive is up to speed, that the first seek was successful, and that no fault condition exists.

Table Continued on Next Page

TABLE 1-3. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
BIB1	On Cylinder - This signal indicates that the servo head is positioned at a track. This line goes inactive if the positioner drifts off cylinder.
BIB2	Seek Error - this signal indicates that the drive took too long to complete a seek, that the positioner has moved outside the recording field, or that the drive was commanded to seek beyound cylinder 1216. The seek error can be cleared by an RTZ command.
BIB3	Fault - When this line is active, it indicates that one or more of the following faults exist: • Read and Write Fault • Write or Read attempted while Off Cylinder • First Seek Fault • Write Fault • Write and Write Protected Fault • Head Select Fault • Voltage Fault
Table Continued on Next Page	

TABLE 1-3. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
BIB4	Write Protect - This signal indicates that the drive write circuits are disabled. The write protect mode is enabled by a switch on the control board, by a switch on the operator panel, by a fault condition, or by a loss of motor speed. Attempting to write while the write protect mode is active results in a fault condition.
BIB5	Address Mark - When an address mark has been found during an address mark search operation, this line goes high (refer to Tag 3 description).
BIB6	Index Mark - This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero. Note: This signal may be disabled by a switch selection on the I/O board.
BIB7	Sector Mark - This signal is derived from the servo tracks. The number of sector signals that occur for each revolution of the disk is selected by switches on the control board. Note: This signal may be disabled by a switch selection on the I/O board.
Table Continued on Next Page	

TABLE 1-3. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
TAG 2 -- HEAD SELECT/HIGH CYLINDER SELECT This tag line gates the data on the bus out lines to the drive Head Address register and also provides the high order Cylinder Address Bits 2^{10} and 2^{11} on units configured with the Tag 2 extended addressing feature. Tag 2 extended addressing permits the user to address up to 1217 cylinders. Cylinder addresses above 1216 are illegal and will cause a seek error. Drive status information is returned on the Bus In lines (refer to Tag 1 Bus In description).	
Bus Out Bits BOB0 BOB1 BOB2 BOB3 BOB4 BOB5-6 BOB7 BOB8 BOB9 Bus In Bits	Defined as follows: Head Address 2^0 Head Address 2^1 Head Address 2^2 Head Address 2^3 Head Address 2^4 Not used Cylinder Address 2^{10} Cylinder Address 2^{11} Not used Refer to description of Bus In bits under Tag 1.
TAG 3 -- CONTROL SELECT This tag line gates the data on the bus lines to the logic circuits of the drive for commanding various operations. The operation performed is dependent upon which of the Bus Out lines is active. Drive status information is returned on the Bus In lines (refer to Tag 1 Bus In description).	
Table Continued on Next Page	

TABLE 1-3. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
Bus Out Bit	Defined as follows:
BOB0	Write Gate - Enables write driver. Not accepted if there is a seek error or fault status.
BOB1	Read Gate - Enables read circuitry. Leading edge triggers the read chain circuit to synchronize on an all zeros pattern. Not accepted if there is a seek error or fault status.
BOB2	Servo Offset Plus - Offsets the positioner 57 microinches toward the spindle from the on cylinder position. Disables On Cylinder for 2.75 milliseconds.
BOB3	Servo Offset Minus - Offsets the positioner 57 microinches away from the spindle from the on cylinder position. Disables On Cylinder for 2.75 milliseconds.
BOB4	Fault Clear - A pulse sent to the drive that clears the Fault latch provided that the fault condition no longer exists.
BOB5	Address Mark Enable - When this signal occurs with a Write Gate, an address mark is written. When this signal occurs with a Read Gate, an address mark search is initiated.
BOB6	RTZ - A pulse sent to the drive to move the positioner to track zero. It also resets the Head Address register, Cylinder Address register, and Seek Error latch.

Table Continued on Next Page

TABLE 1-3. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
BOB7	Data Strobe Early - Enables the read comparator to strobe the data at a time earlier than nominal.
BOB8	Data Strobe Late - Enables the read comparator to strobe the data at a time later than nominal.
BOB9	Release - Used with dual channel option only, it clears channel reserved and channel priority select reserve status. (Refer to Unit Selection discussion.)
Bus In Bits	Refer to description of Bus In bits under Tag 1.
TAG 4 -- CURRENT SECTOR (SMD-E ONLY) This tag allows the current sector address to be transmitted to the controller on the Bus In lines. A sector address can be any number from 0 to 255. Bus Out bits 0 through 9 are undefined. Note: This tag is not usable when the unit is configured with Tag 1 Extended Addressing.	
Bus In Bits	Defined as follows:
BIB0	Sector Address 2^0
BIB1	Sector Address 2^1
BIB2	Sector Address 2^2
BIB3	Sector Address 2^3
BIB4	Sector Address 2^4
BIB5	Sector Address 2^5
BIB6	Sector Address 2^6
BIB7	Sector Address 2^7

Table Continued on Next Page

TABLE 1-3. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
TAG 5 -- EXTENDED STATUS (SMD-E ONLY) This tag allows fault status, operating status, diagnostic status, and diagnostic execute status to be transmitted to the controller on Bus In lines. Except for diagnostic execute status, this tag can be executed at any time. Diagnostic execute status can be requested whenever the drive is up to speed. The type of status transmitted on Bus In is determined by the state of Bus Out bits 0 and 1. Note: Bus Out bits 2 through 9 should be set to zero.	
	Fault Status - When Bus Out bits 0 and 1 are set to zero, fault status is transmitted on Bus In as follows:
Bus In Bits	
BIB0	Read and Write Fault
BIB1	Read or Write and not On Cylinder Fault
BIB2	First Seek Fault
BIB3	Write Fault
BIB4	Write and Write Protected Fault
BIB5	Head Select Fault
BIB6	Voltage Fault
BIB7	Valid Status Available
Table Continued on Next Page	

TABLE 1-3. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
	Operating Status - When Bus Out bit 0 is a "1" and Bus Out bit 1 is a "0", then Bus In bits 0 through 6 reflect operating status. Bus In bit 7 indicates that valid status is available. Refer to Trouble Analysis for a description of operating status. Diagnostic Status - When Bus Out bit 1 is a "1" and Bus Out bit 0 is a "0", then Bus In bits 0 through 3 reflect the most likely failed field replaceable unit as defined in the following list.
Bus In Bits 3-0	Field Replaceable Units
0001	Power Supply
0010	Control Board
0011	Not Used
0100	Not Used
0101	Read/Write Board
0110	Module
0111	Cooling Fan (drive mount option only)
1000	I/O Board
1001	Status/Control Panel
1010	Not Used
1011	Carriage Latch Electromagnet
1100	Not Used
1101	Not Used
1110	Not Used
1111	Not Used
	Bus In bits 4 through 6 are not used. Bus In bit 7 indicates that valid status is available

Table Continued on Next Page

TABLE 1-3. TAG/BUS COMMAND DECODE FUNCTIONS (Contd)

I/O Signals	Function
	Diagnostic Execute Status - When Bus Out bits 0 and 1 are "1", then Bus In bits 0 through 6 are undefined and bit 7 indicates that a diagnostic test is executing.
TAG 6 -- DEVICE TYPE (SMD-E ONLY) Tag 6 (activating Tags 4 and 5 simultaneously) causes customer selected device type status to be returned on Bus In lines 0 through 7. Note: This tag is not usable when the unit is configured with Tag 1 Extended Addressing.	

The Select Compare signal enables the Unit Selected signal. The Select Compare signal also causes the Selected FF to set, thereby enabling the receivers and drivers to the controller. The drive is now ready to respond to further commands from the controller.

DUAL CHANNEL UNIT SELECTION

General

Dual channel drives are connected to, and can be selected by, either of two controllers. However, because the drive is capable of responding to only one controller at a time, the controllers must compete for use of the drive. For this reason, there are functions associated with dual channel selection that are not necessary when selecting single channel units.

The functions controlling dual channel selection are as follows:

- Select - Logically connects the drive to the controller, thus enabling it to respond to commands from the selecting controller.
- Reserve - Reserves the drive so it can be selected at any time by the reserving controller, but prevents it from being selected by the other controller.

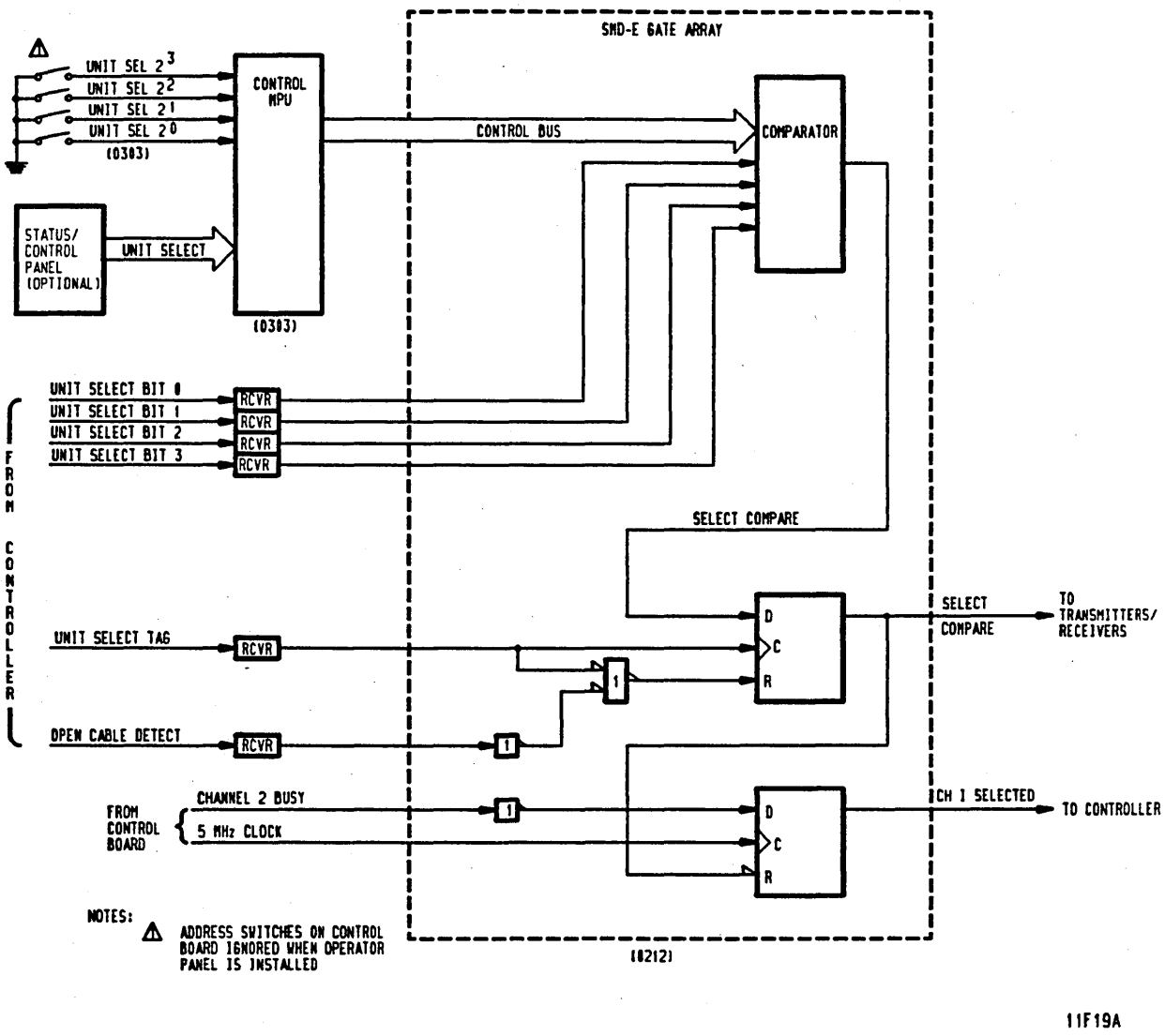


Figure 1-12. Unit Select Logic (Single Channel)

- Release - Releases drive from reserved condition.

- Priority Select - Allows controller to force select the drive by disabling the interface to the controller having the drive selected or reserved.

- Disable - Allows disabling either channel interface during maintenance.

The following discussions describe each of these functions. It should be noted that because these functions are basically the same regardless of which channel is involved, they are described only as they relate to Channel I. Figure 1-13 shows the select logic associated with channel I selection and table 1-4 describes the major elements on this figure. Figure 1-14 is a flowchart of the dual channel unit select and reserve functions.

Select and Reserve Function

The drive is both selected and reserved during the same sequence and this sequence is initiated by a Unit Select Tag accompanied by a logical address. However, the drive can be successfully selected and reserved only if none of the following conditions exist:

- Drive is already selected and reserved by other controller.

- Drive is not selected but is reserved by other controller.

- Channel to drive attempting selection has been disabled by either a priority select or disable function.

The following paragraphs describe how the drive is initially selected and also how it responds to a Unit Select Tag when it is selected, reserved, or disabled.

Assuming the drive is available (not selected, reserved, or disabled) and it receives a Unit Select Tag and logical address from the controller on channel I, it compares the address received with that indicated by its logical address switches. If the two addresses are the same, the drive enables the Channel I Select Compare signal. The logic used to generate this signal is identical to that used in the single channel units.

With the Channel 1 Select Compare signal active, the drive sends Unit Selected to the channel 1 controller. The Select Compare signal also causes the Channel I Selected FF to set, thereby enabling the receivers and drivers to the Channel I controller and triggering the Reserve one-shot. The output pulse from this one-shot clocks and sets the Channel I Reserved FF.

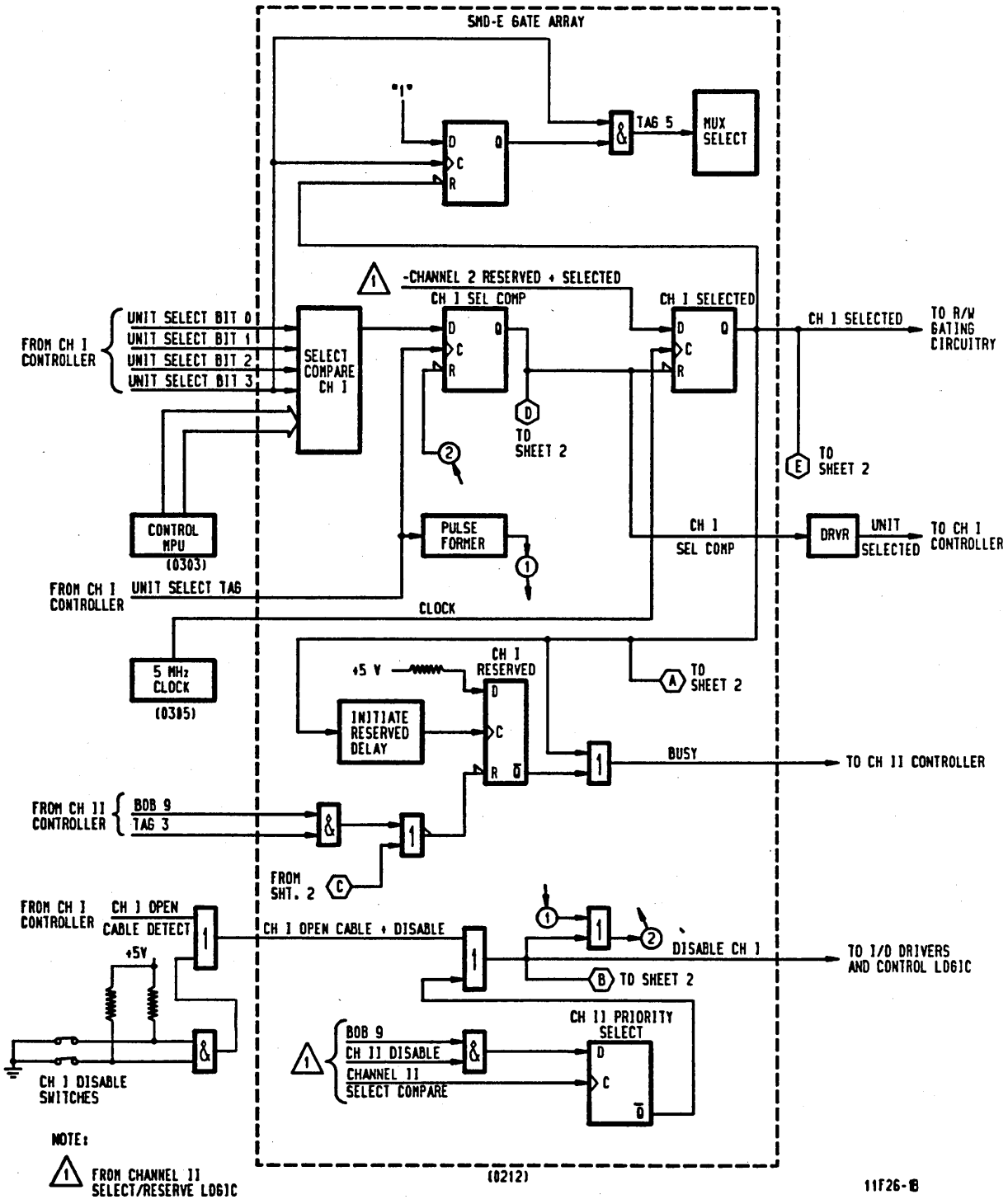


Figure 1-13. Channel I Dual Channel Logic (Sheet 1 of 2)

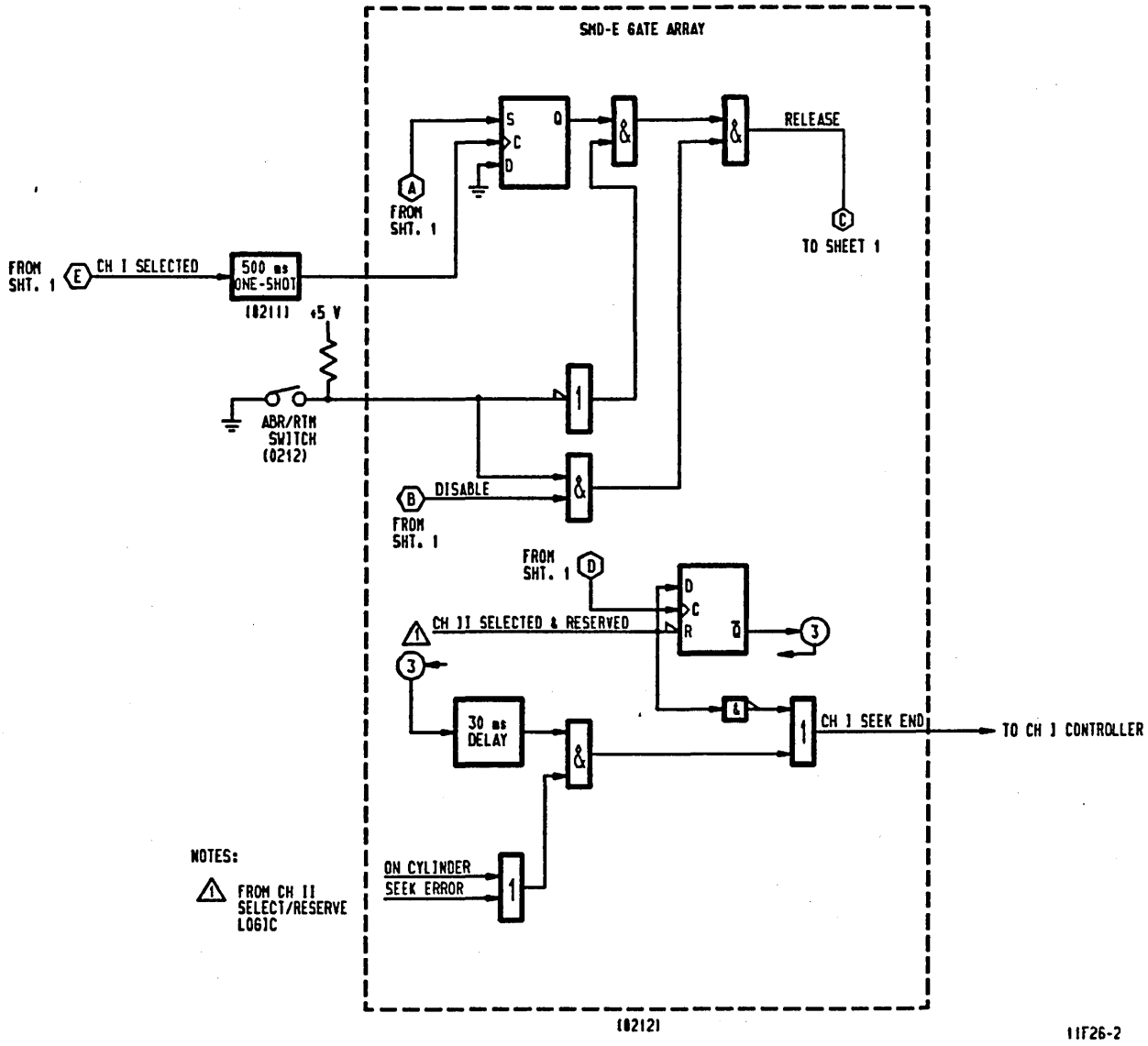


Figure 1-13. Channel I Dual Channel Logic (Sheet 2)

TABLE 1-4. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS

Element*	Function
ABR/RTM Switch	Determines whether the drive will be in ABR (absolute reserve) or RTM (reserve timeout) mode. If switch is in RTM position, drive is released from reserved condition 500 ms (nominal) after being deselected. If switch is in ABR position, drive remains reserved until it receives either a release or priority select command.
Release Timeout One Shot	Times out 500 ms after drive is de selected. If drive is in RTM mode, the reserved FF is cleared when timeout occurs.
Channel I Disable Switches	Disable channel I whenever both switches are set to Disable position.
Channel I Disable FF	Sets if drive receives Priority Se lect command. This causes drive to be selected and reserved for controller issuing command and disables channel to other controller.
Channel I Reserved FF	Sets during select and reserve se quence. When set it keeps drive reserved to channel I until channel I releases or channel II issues a Priority Select command.
Channel I** Selected FF	Sets during select and reserve se quence and enables drivers and receivers to channel I controller.
Channel I Select and Compare Logic	Compares logical address of drive with that sent by controller (see Single Channel Unit Selection).

Table Continued on Next Page

TABLE 1-4. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS (Contd)

Element*	Function
Initiate Reserved Pulse	Generates a pulse whenever Select Compare signal goes true. The pulse length is 300 ns (nominal). This pulse creates a delayed clock for the Channel I and Channel II Reserve FFs.
Channel I Select Tried FF	Sets if channel I tries to select and reserve drive while it is already selected and/or reserved by channel II. When drive is deselected and released by Channel II, this FF clears and thereby triggers the Select Tried one shot.
Select Tried One Shot	Generates a pulse whenever either Tried FF clears. The pulse length is 30 microseconds. This pulse is sent to controller (associated with the Channel Tried FF that triggered the one shot) via the Seek End line.

* Includes only those elements directly concerning channel I and shown in figure 1-14.

**The Channel Selected FF's are alternately clocked by the +5 MHz OSC signal to prevent simultaneous selection.

Providing channel II does not issue a priority select command (see Priority Select Function discussion), the drive remains selected to channel I until the controller on channel I drops its Unit Select Tag. At this time, the drive's Channel I Select Compare FF clears. This clears the Channel I Selected FF, thereby disabling the drivers and receivers for that channel. Clearing the Select Compare FF also disables the Unit Selected signal thus informing the controller that the drive will no longer respond to commands. However, the drive remains reserved to channel I (allowing channel I to reselect while preventing channel II from selecting) until the Channel I Reserve FF is also cleared. The Reserve FF is cleared by either a release or priority select function (refer to these discussions).

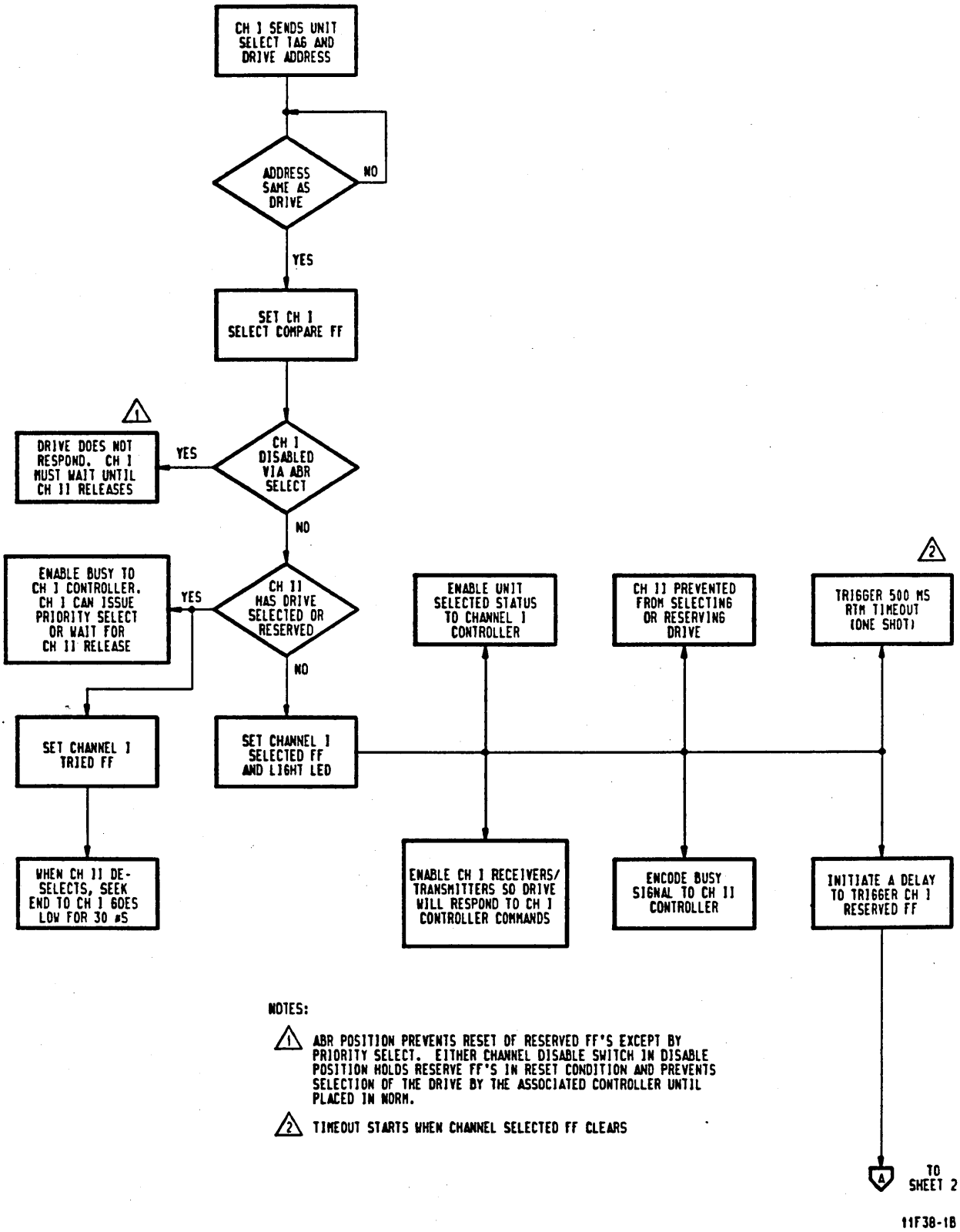


Figure 1-14. Dual Channel Selection Flowchart (Sheet 1 of 2)

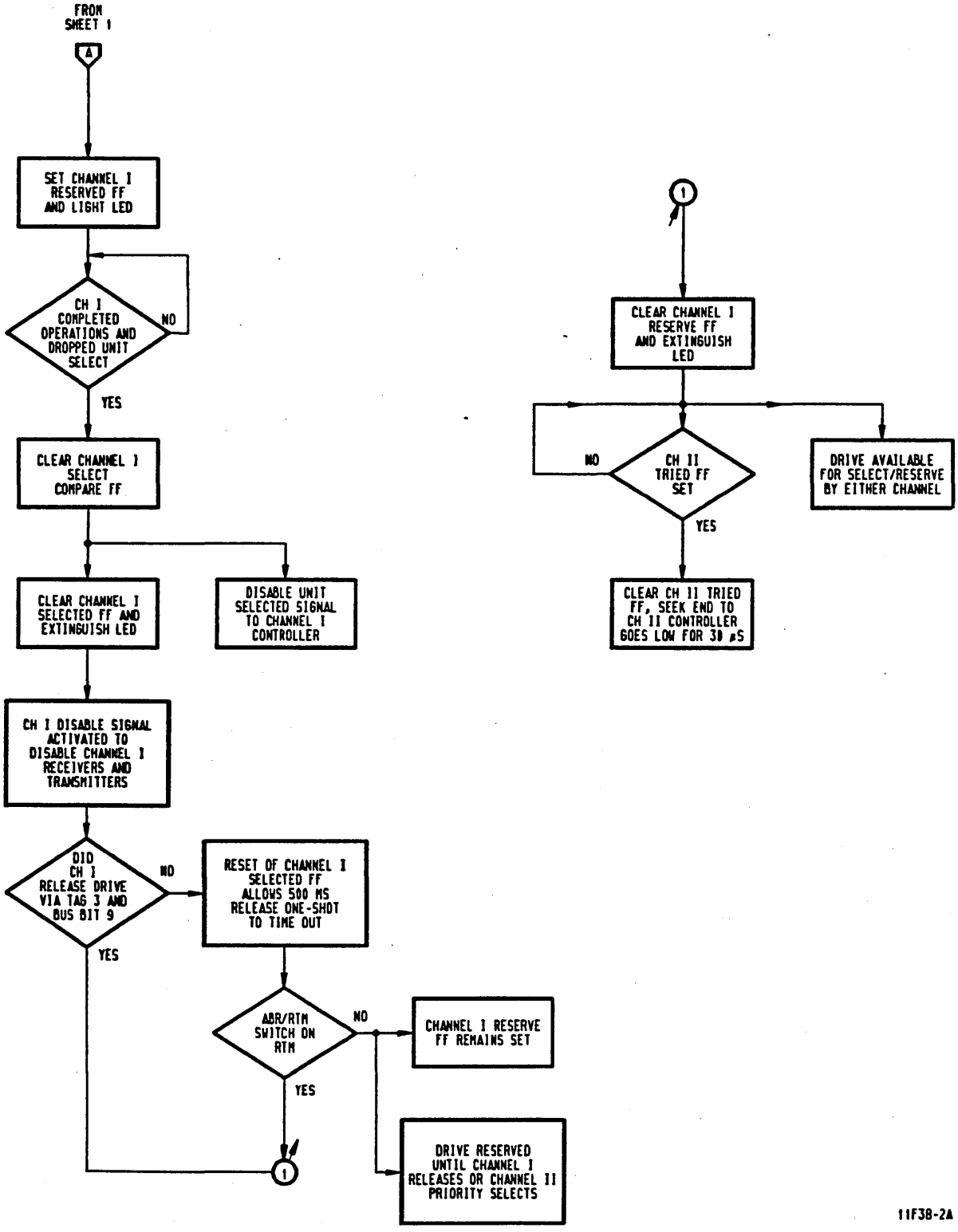


Figure 1-14. Dual Channel Selection Flowchart (Sheet 2)

If channel I attempts to select and reserve the drive while it is selected and reserved by channel II, the Channel I Select Compare signal is still generated as during the initial select and reserve sequence. However, the Channel I Select and Reserve FFs do not set, and therefore the attempt is unsuccessful. The drive still sends the Channel I Unit Selected signal to the controller, but, in this case, it is accompanied by the Channel I Busy signal. The Busy signal indicates that the drive is selected or reserved by channel II.

The drive also sets its Channel I Tried FF, thus recording the unsuccessful attempt. When the drive is no longer selected or reserved by channel II, this FF clears, causing Seek End to the channel I controller to go low for 30 microseconds. This informs the channel 1 controller that the drive is no longer selected or reserved.

If the channel I controller tries to select the drive while channel I is disabled (either by a priority select or maintenance disable function), the attempt is unsuccessful and no response is sent back to the channel I controller.

Release Function

The release function will release the drive from either a reserved or priority selected condition. There are two types of release functions:

- Timeout release pulse
- Release command

The timeout release pulse is capable of releasing the drive from the reserved condition only. This pulse is generated by the 500 ms Timeout Release one-shot and releases the drive by clearing the Reserve FF. The pulse times out 500 ms after the drive is deselected (Select FF clears).

Whether or not the one-shot has any effect on the Release FF depends on the position of the ABR/RTM switch. If this switch is in the RTM (reserve timeout) position, the FF clears when the one-shot times out, thus making the drive available to the other channel. However, if this switch is in ABR (absolute reserve) position, the one-shot has no effect on the FF and the drive remains reserved.

A Release command will release the drive from both the reserved and priority selected conditions. This command is initiated by the reserving and/or priority selecting controller when it issues a Tag 3 (Control Select) with Bus Out bit 9 active. This clears the Reserve and Disable FFs and allows the other controller to select the drive once the issuing controller drops its Unit Select Tag, and the Select FF for that channel has cleared.

Priority Select Function

If the drive is selected and reserved, the other controller can force selection by issuing a Priority Select command (Unit Select Tag accompanied by drive logical address and Bus Out bit 9). This command will disable the channel to the controller presently using the drive and also select and reserve the drive to the controller issuing the Priority Select command.

For example if channel I has the drive and channel II wants to select, channel II issues a Priority Select command. In this case, the command sets the Channel I Disable FF which in turn results in clearing the Channel I Selected and Reserved FFs. It also sets the Channel II Selected and Reserved FFs, thereby selecting and reserving the drive for channel II.

Once the Disable FF is set, that channel (in this case channel I) is disabled until the other controller (in this case channel II) issues a command to clear it.

Disable Function

It is also possible to disable either channel by setting both Disable switches for that channel (refer to figure 1-13) to the DISABLE position.

DRIVE SERVO SYSTEM OVERVIEW

The drive writes data on and reads data from the disk data recording areas under controller direction. These operations cannot be done randomly, however, for when the controller wishes to retrieve data, it must be able to find the exact location where that data has been stored. This problem is resolved by mapping the disks into narrow concentric bands called "tracks" that cover the entire circumference of the circle. The tracks are then further subdivided into equal areas called "sectors". The collection of all tracks in the same vertical plane is termed a "cylinder".

After the controller has selected the unit with which it wishes to perform an operation, it must then direct the drive to the specific location on the data recording surface where it wants the operation to be performed. The operation of positioning the heads over the desired track is called a seek operation. The drive servo system under the direction of the Servo MPU performs the Seek operation to position the heads by using information read from the servo surface by the servo head.

The data recording areas of each of the disks (1 area on each of 10 disk surfaces) are divided into 1217 tracks, and these are assigned sequential number addresses from 0, which is located on the outer edge of the recording area, through 1216 which is located on the inner edge of the data recording area closest to the hub. Note: On units not configured with either of the extended addressing features, only 1024 tracks are available for data storage. Since there are 10 data recording areas, each with 1217 tracks with addresses 0 through 1216, the controller must select 1 of 10 possible tracks with the same cylinder address number. This further selection is done by assigning numbers to the data recording areas (and the heads associated with the data areas) from 0 through 9.

Once a particular cylinder is selected, the controller then further narrows down location selection by addressing one of 10 heads located at the selected cylinder. Each track is subdivided into equal segments called "sectors". This division is accomplished by the setting of a group of switches called Sector switches (see the discussion called Sector Detection). When the controller has selected the unit, the track, and the head, it waits for the particular sector(s) where it wishes to write (store) or retrieve (read) data. Another option for locating an area on a track to be operated upon is by writing an Address Mark at a specific location on the track, and then looking for the mark at the beginning of a read operation.

When the controller commands the drive to go to a cylinder/head/sector where it wishes to perform a read or write operation, the drive servo system under the direction of the Servo MPU performs the positioning (Seek) operation. The Servo MPU firmware uses information read from the servo surface by the servo head to do the Seek operation. The following discussion will describe servo surface decoding and then describe seek functions.

SERVO SURFACE DECODING

GENERAL

The servo surface is a prerecorded disk surface in the module that provides three basic types of information to the drive electronics. Information from the servo surface is read by the servo head. The servo head is mounted on the same positioner as the data heads; thus, movements of the data heads across the data surface correspond exactly to movements of the servo head across the servo surface.

The three types of information available from the servo surface are as follows:

- Radial movement of the heads, indicated by the Position signal
- Rotational position of the disks, indicated by the Index signal
- Exact rotational speed of the disks, indicated by the clock signal from the servo PLO.

The significance of each type of information for drive operation and the development of the basic feedback signals from the servo signal are presented under the following topics:

- Tribit Recording Scheme
- Servo Surface Format
- Tribit Decoder Circuit Operation

TRIBIT RECORDING SCHEME

Servo information consists of tribit coding on a series of concentric tracks located on the servo surface. The pattern of flux reversals alternates from track to track. Each track has eighty segments, each consisting of a special nine-byte resync pattern followed by 327 normal servo bytes.

Unless the servo head is positioned directly over one tribit track, the signal it detects is a composite of signals from the two tracks nearest the head. Figure 1-15 shows servo information recorded on two adjacent tracks and the signal detected when the servo head is halfway between the tracks.

In figure 1-15, two normal bytes are followed by a resync byte. Each normal byte contains three bits -- a sync bit and two position bits. The sync bits have negative polarity and are recorded on all tracks. The position bits have positive polarity and are staggered from track to track so that they make separate contributions to the composite servo signal.

The resync byte shown in figure 1-15 has a missing sync bit and one position bit (half the number of position bits in the normal byte). Adjacent tracks have coinciding sync bits as well as staggered position bits.

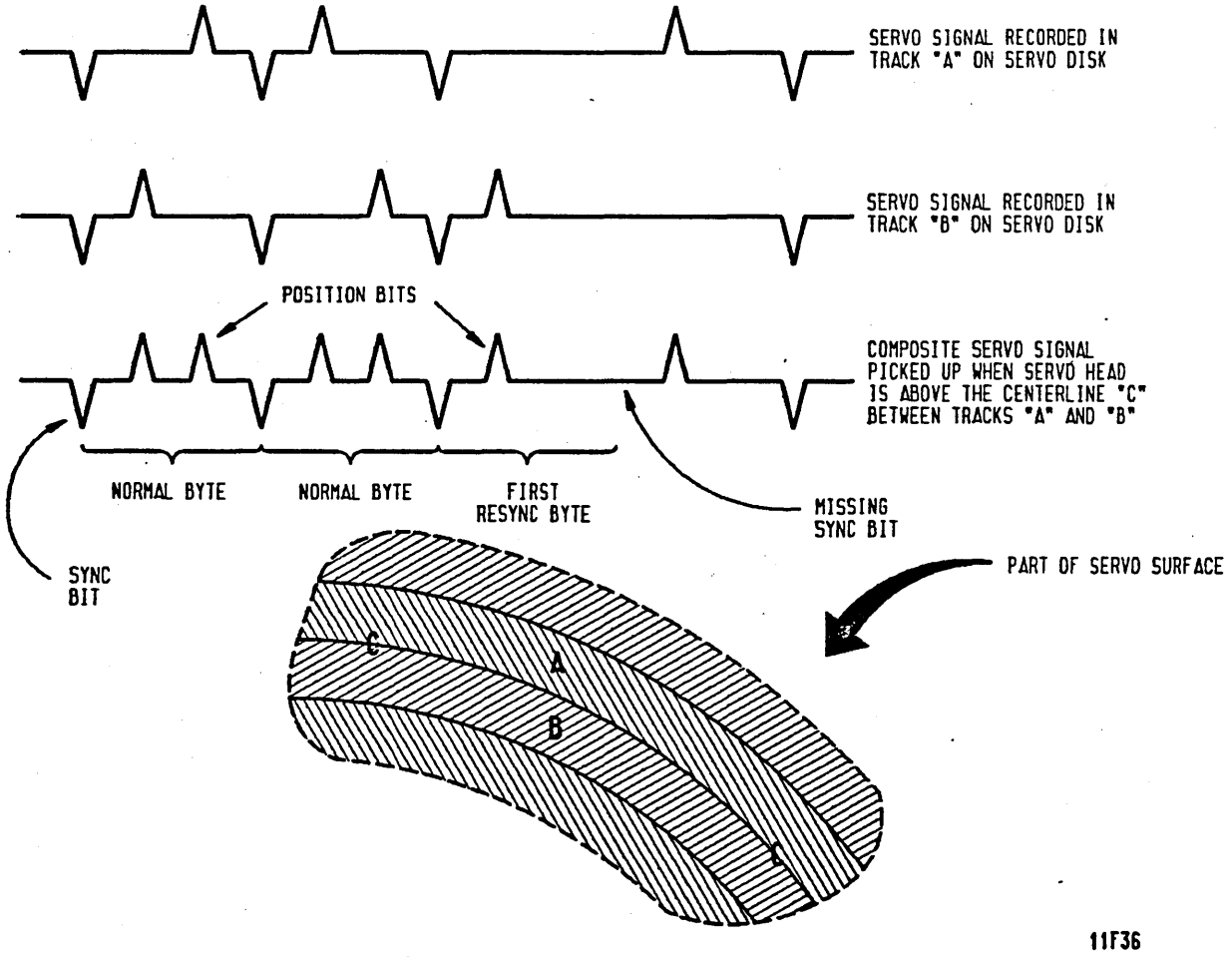


Figure 1-15. Tribit Pattern

The special nine-byte resync patterns appearing 80 times per disk revolution contain different combinations of resync bytes and normal bytes, depending on what the pattern designates on the disk surface. The different patterns and their relation to the disk format are explained under the next topic. Each nine-byte pattern is followed by 327 normal bytes. Thus, for each disk rotation, the servo head detects 80 X 336 or 26 880 servo bytes.

The relative amplitude of the position bits within each servo byte is used to indicate the precise position of the servo head and, therefore, the data heads. When the data heads are located at the centerline of a data track, the servo head is actually centered between two of the prerecorded tribit tracks and is reading an edge of each. The detected signal called a servo track is a mixture of the two adjacent tribit tracks. The amplitude of each position bit within a servo byte is proportional to the read coil overlap of the recorded tribit tracks. With the head centered, each adjacent tribit track contributes equal position bit amplitudes. As the head moves away from its centered position toward one tribit track, the track being approached makes a greater contribution to the detected position bits than the one being left. The tribit demodulator converts this variation into the position signal used by the seek circuitry (see Position Demodulation).

Figure 1-16 shows the detected servo signal for three different servo head positions. In one of the three cases, the servo head is located on the centerline between two tribit tracks, and the position bits have equal amplitudes. In the other two cases, the servo head is located on either side of the centerline, and the position bits have different amplitudes.

SERVO SURFACE FORMAT

The servo surface, through its encoding format, establishes the format of the disk data surfaces. The servo surface format divides the disk surfaces into four zones: a 1217-track data zone, two guard bands, and a buffer zone. The guard bands indicate areas of the disk that cannot be used for recording of data, however, servo encoding extends to include the guard band areas. The outer guardband consists of 10 tracks on the outer portion of the disk. The inner guardband consists of 95 tracks on the inner portion of the disk. The buffer zone consists of two tracks located between the outer guard band and the data zone. In addition, all four zones contain an encoded "reference line" which establishes the logical beginning of each track. When this reference is decoded, the drive sends the Index signal to the controller via the interface.

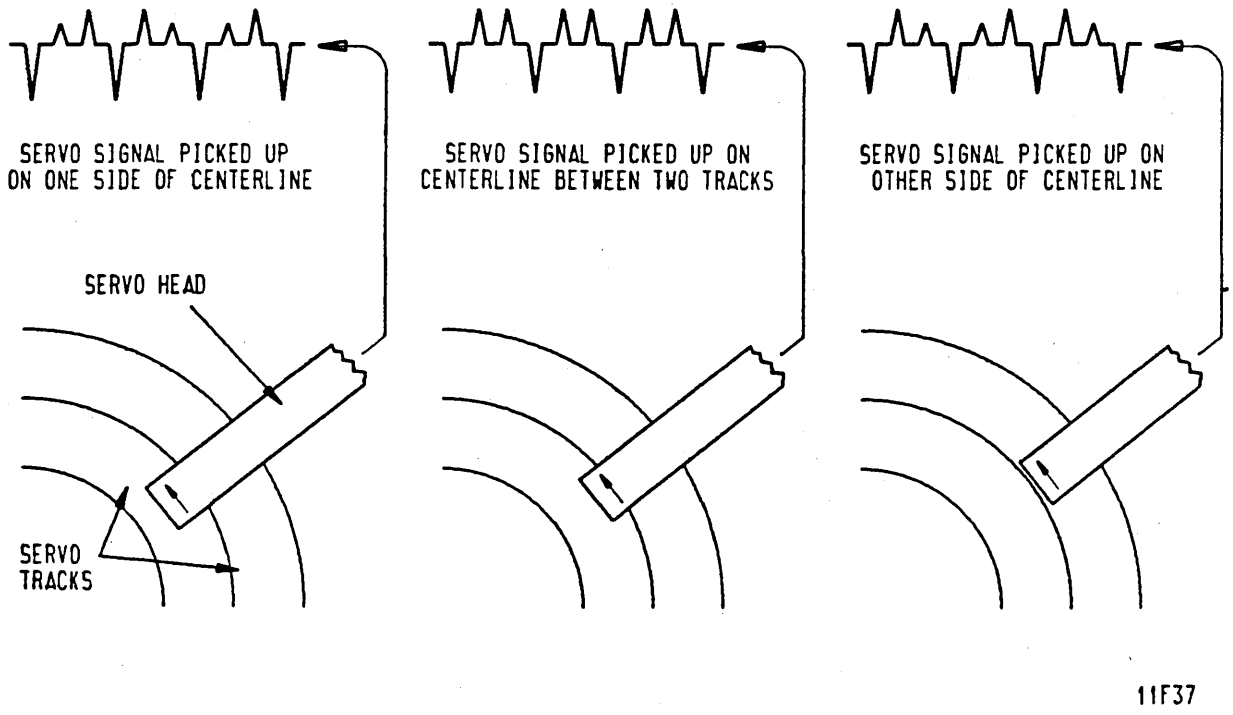


Figure 1-16. Tribit Signal Variations

Figure 1-17 shows the positioning of heads on the module disk surfaces and explains, in the exploded portion of the drawing, how formatting information is encoded on the disk. As described in the Tribit Recording Scheme discussion, nine-byte resync patterns are used as format indicators. Each of the nine bytes is either a resync byte (labelled "1") or a normal byte (labelled "0"). With the two bytes labelled in this manner, each nine-byte code can be designated as a nine-bit pattern number. The Index pattern (101000101) marks the logical beginning of each servo track. The remaining 79 coded patterns spaced around each servo track depend on the zone for that track. The outer guardband is encoded with pattern 100010101, the data zone and buffer zone with pattern 100010001, and the inner guardband with pattern 101010001.

Refer to the Index and Guardband Decoding discussion for a description of the circuitry that performs this decoding.

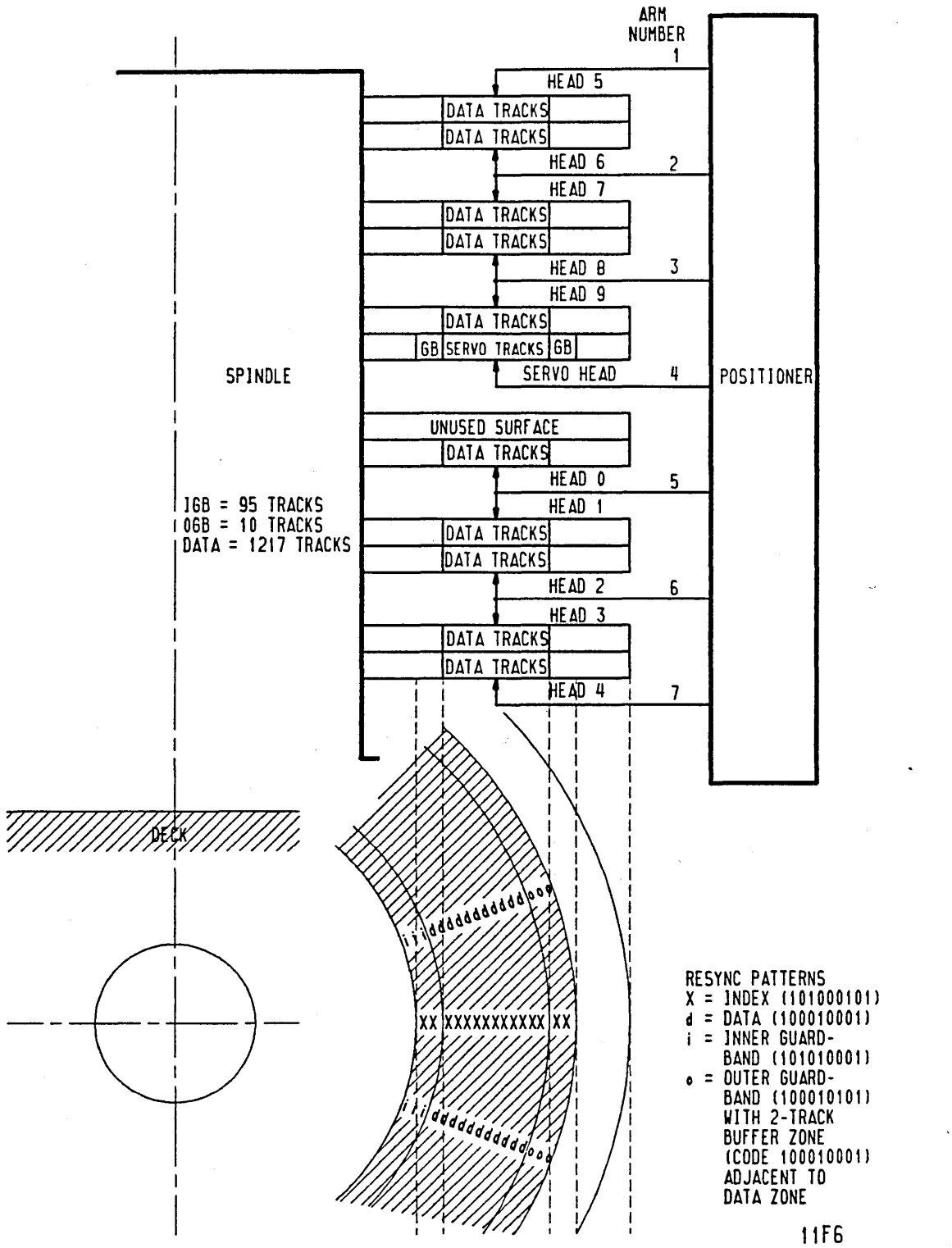


Figure 1-17. Servo Disk Format

TRIBIT DECODER CIRCUIT OPERATION

General

Operation of the tribit decoder circuitry is discussed first in terms of its relation to other systems within the drive. This is followed by explanations of the individual functions performed by the decoder.

System Overview

Decoding the information present in the servo signal is essential for other functional areas of drive operation. Figure 1-18 is a functional block diagram showing signal flow between the tribit decoder and these other functional areas.

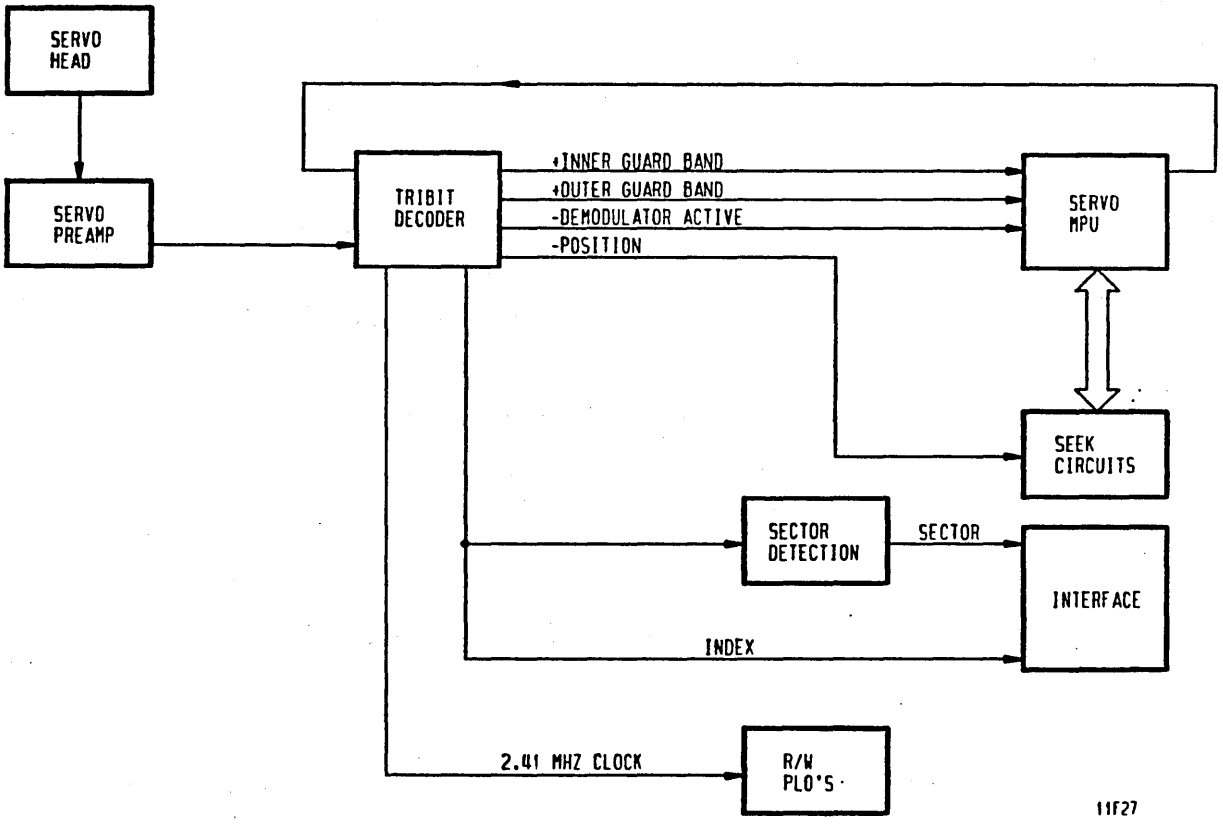


Figure 1-18. Tribit Decoder System Diagram

Inputs to the decoder come from the servo preamplifier and the Servo MPU. The servo preamplifier amplifies the signal detected by the servo head. The +Slope signal, supplied by the Servo MPU, sets up the phase of the decoded Position signal so that it can be used by the seek circuits.

The Servo MPU monitors three output signals from the decoder. During normal seek operations, the servo head remains over the data zone. Thus, when the Inner or Outer Guard Band Pulses go active, the Servo MPU reacts by altering the seek protocol. Improper decoder operation can affect seek reliability. For this reason, the Servo MPU monitors the -Demodulator Active line.

Data transfers to and from the disk must be coordinated with respect to the rotational position of the disk. The Index signal is decoded and is input to the Sector Detection circuitry which, in turn, generates a given number of Sector pulses per disk rotation. The controller coordinates data transfers based upon the Index and Sector pulses transmitted to it via the interface.

The 2.41 MHz Clock from the decoder is used by the R/W PLO circuitry to form a 14.5 MHz Servo Clock. The Servo Clock operates at exactly six times the frequency of the clock from the tribit decoder, and it tracks the rotational velocity of the disk. The controller transfers data to the disk in sync with the Servo Clock. This compensation in the rate of data transfers to the disk makes the written data pattern independent of disk speed.

The remaining topics within this discussion cover the operation of circuits within the tribit decoder. Figure 1-19 is a block diagram showing these circuits and their interconnections.

Sync Bit Detector

The Sync Bit Detector monitors the ±Servo Data signals from the servo preamplifier and generates a pulse on the -Sync Detect line each time a sync bit occurs in the Tribits signal. Sync bit detection is essential for all other tribit decoder functions because sync bits are the primary input to the Servo PLO circuit which in turn controls the timing of the Position Demodulator and the Index and Guard Band Decoder.

In addition, the -Sync Detect signal reflects the encoding used to indicate Index, Data, and Guardband regions on the servo surface. Figure 1-20 is a block diagram of the Sync Bit Detector.

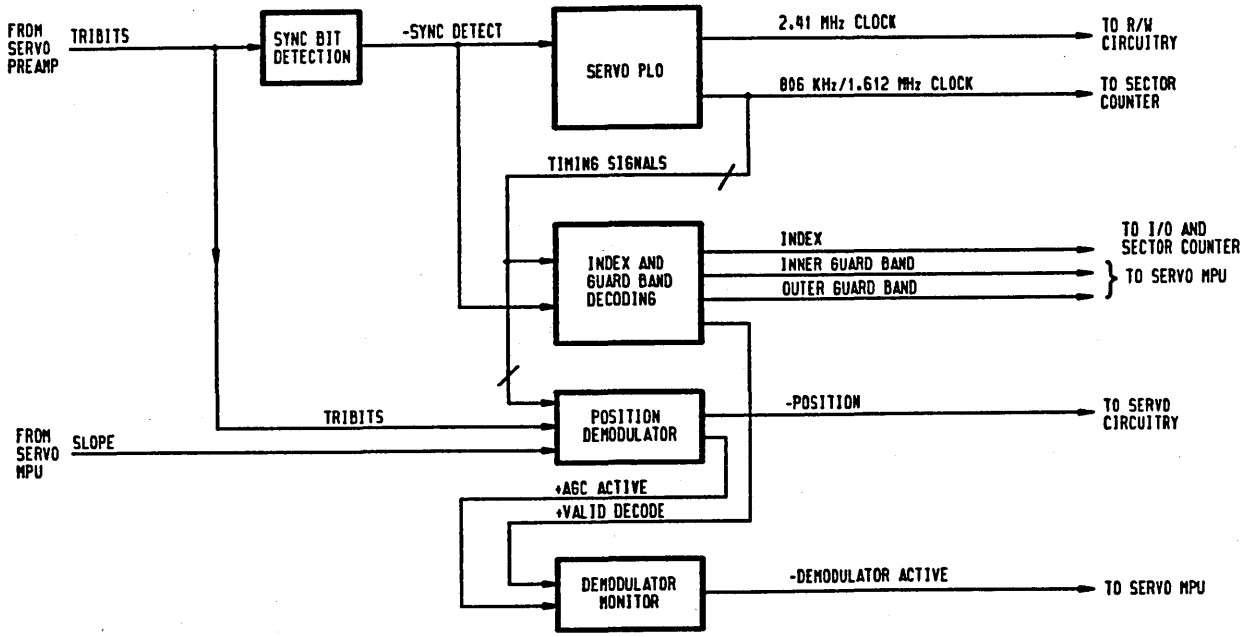


Figure 1-19. Tribit Decoder Block Diagram

The Tribits signal is applied to an AGC-controlled differential amplifier. The amplifier output passes through a buffer stage and is ac-coupled to the input of the first comparator. A dc offset at the comparator input allows the comparator to be enabled only by the most negative portion of each sync bit.

Output pulses from the first comparator perform two functions. The AGC amplifier looks at these pulses and develops an AGC voltage to control the gain of the differential amplifier at the input. This AGC loop operates to ensure that the pulses coming from the first comparator have a constant duty cycle.

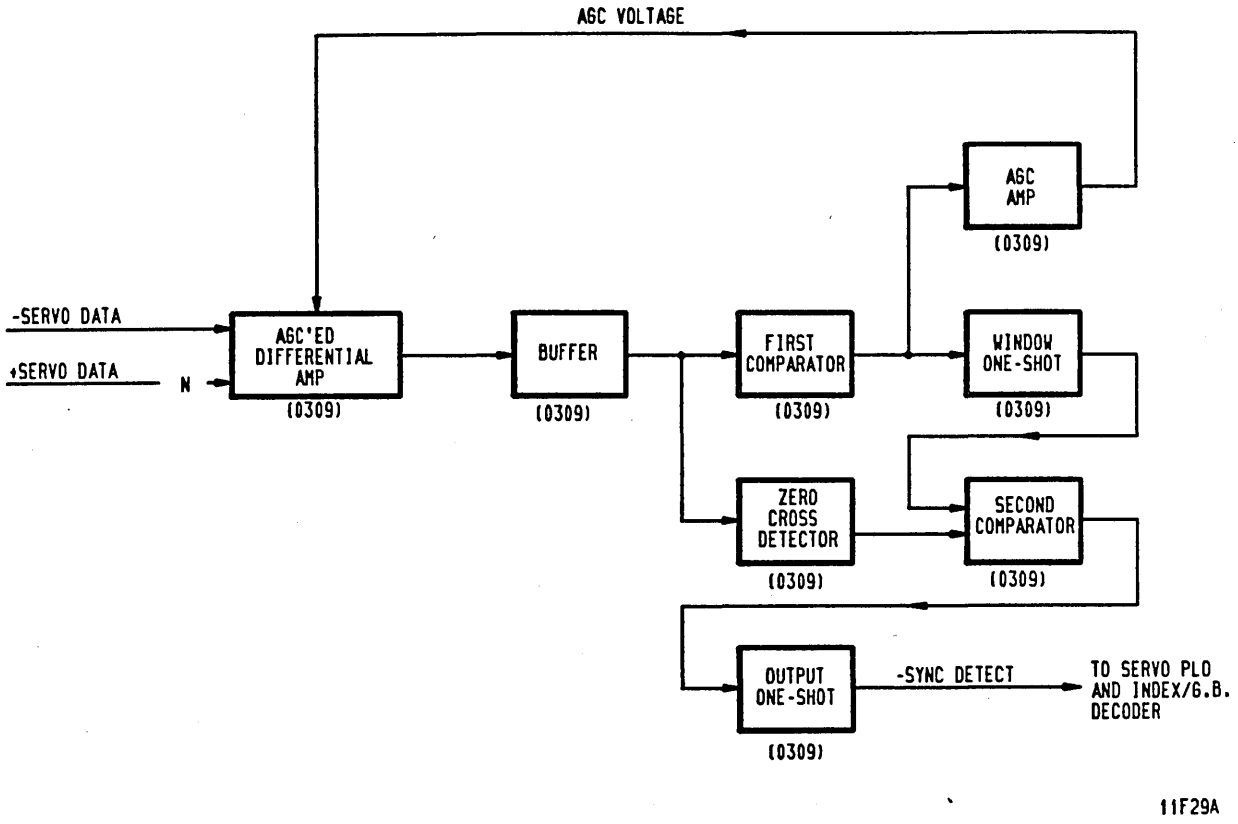


Figure 1-20. Sync Bit Detector

In addition to controlling AGC, the output pulses trigger a one-shot to develop a window during which sync bit detection is enabled. The gate from the window one-shot enables a second comparator. The input to the second comparator is the Tribits signal, differentiated by a zero-cross detector. The second comparator reacts only to zero-crossings produced when sync bits are expected because it is disabled at other times. Seeing an acceptable zero crossing, the second comparator triggers the output one-shot to generate a negative pulse on the -Sync Detect line.

Servo PLO

The Servo PLO uses a phase-locked loop to keep the timing in the tribit decoder synchronized to the detection of sync bits in the Tribit signal. As shown in figure 1-21, a portion of the Servo PLO circuitry is located in the Demodulator Logic Chip. Circuitry external to the chip includes a charge pump, the 9.67 MHz Voltage-Controlled Oscillator (VCO) and logic that compensates for missing sync bits.

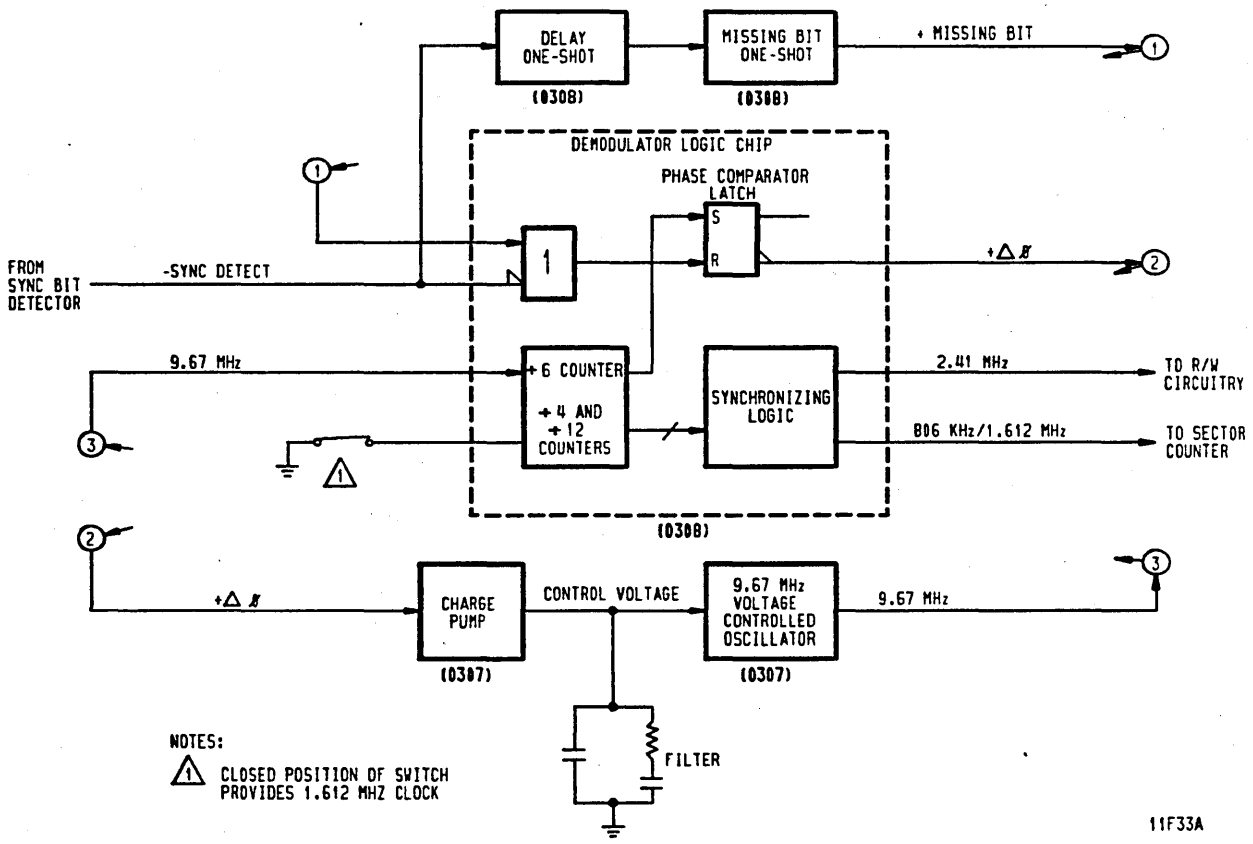


Figure 1-21. Servo PLO Block Diagram

The Sync Bit Detector supplies -Sync Detect pulses to the phase comparator in the Demodulator Logic Chip. As described under Servo Surface Format, each servo track has patterns encoded by missing sync bits to locate index on the disk and to indicate whether the track is in an inner or outer guard band or in the data zone. However, the phase comparator latch must be reset at regular intervals of about 620 ns. Because the encoded patterns never contain two consecutive missing sync bits, it is possible to develop a "dummy" trigger pulse whenever a sync bit is missed. To do this, -Sync Detect pulses clock a retriggerable one-shot. Each missing bit allows the one-shot to time out and trigger the missing bit one-shot. In this way, the phase comparator latch is reset periodically either by pulses on the -Sync Detect line or on the +Missing Bit line.

The Set input to the phase comparator latch is derived from a Divide-by-Six counter in the Demodulator Logic Chip. This counter is clocked by the 9.67 MHz signal from the VCO, which oscillates at six times the repetition rate of -Sync Detect pulses. The counter subdivides the interval between -Sync Detect pulses into six equal parts. Through various logical combinations of the outputs of the counter stages, the synchronizing logic develops gates needed for the different decoding operations. Because the PLO keeps the Divide-by-Six counter phase-locked to the detected sync bits, these timing gates stay synchronous with the tribit pattern. One of these gates, the Set input to the phase comparator latch, goes active when three VCO oscillations have occurred following reset of the latch. Thus, the +Delta Ø signal generated by the latch is active for three VCO oscillations and is then inactive until the next Reset input occurs (approximately three VCO oscillations later).

The phase comparator latch causes the VCO to shift in frequency when the active interval and the inactive interval of the +Delta Ø signal are not equal. This frequency shift is governed by a charge pump that supplies the control voltage to the VCO. When the +Delta Ø signal is inactive, the charge pump supplies current to the capacitors filtering the control voltage to the VCO (making the control voltage more negative). When the +Delta Ø signal is active, the charge pump draws current from these capacitors (making the control voltage more positive). Thus, any imbalance in the set and cleared intervals of +Delta Ø produces a net change in the control voltage.

Consider three situations of changing disk speed and its effect on the Servo PLO. When the disks are rotating at constant speed and the VCO is phase-locked, the set and cleared intervals of the phase comparator latch are equal, the control voltage is normal, and the VCO frequency remains the same. During a decrease in disk speed, the VCO frequency must decrease. In this case, the Set input to the latch is early, and +Delta Ø is inactive longer than it is active. This makes the control

voltage more negative which in turn reduces the VCO frequency. During an increase in disk speed, the VCO frequency must increase. In this case, the Set input to the latch is late, and +Delta Ø is active longer than it is inactive. This makes the control voltage more positive which in turn increases the VCO frequency.

The Divide-by-Six counter develops timing signals used by the Position Demodulator and by the Index and Guard Band Decoder. In addition, the following clocks are derived from the VCO signal:

- 806 kHz -- derived by dividing the VCO signal by twelve and supplied to the Sector Counter Gate Array.
- 2.41 MHz -- derived by dividing the VCO signal by four and supplied to the Write PLO.
- 1.612 MHz -- derived by dividing the VCO signal by six (available as an alternate clock to the Sector Counter Gate Array).

Position Demodulator

The Position Demodulator consists of the circuitry in the Tribit Decoder that develops the -Position signal. It derives this signal from the position bits in the Tribit pattern while depending on timing information developed from the sync bits in the Tribit pattern. The timing information is consistent on all servo tracks while the position information changes from track to track. Consistent timing information keeps the demodulator synchronized (regardless of the position or velocity of the servo head) and allows the demodulator to detect the changes in position information from which the -Position signal is derived. Figure 1-22 is a block diagram of the Position Demodulator, and figure 1-23 provides typical waveforms for the circuit. The following paragraphs review how position is encoded on the servo surface, discuss signal flow through the demodulator, and describe briefly how the Position signal is used by the servo circuitry.

As described earlier under Tribit Recording Scheme, any given tribit pattern contains two position bits. One bit is supplied by each of the two tribit tracks closest to the servo head, and the two bits are staggered so they appear in sequence in the Tribit signal. If the position bits available from one set of alternate tribit tracks are designated as #1 bits and the position bits from the remaining tracks are designated as #2 bits, then the -Position signal is positive when the #2 bit amplitudes exceed the #1 bit amplitudes and is negative when the #1 bit amplitudes exceed the #2 bit amplitudes. The synchronizing

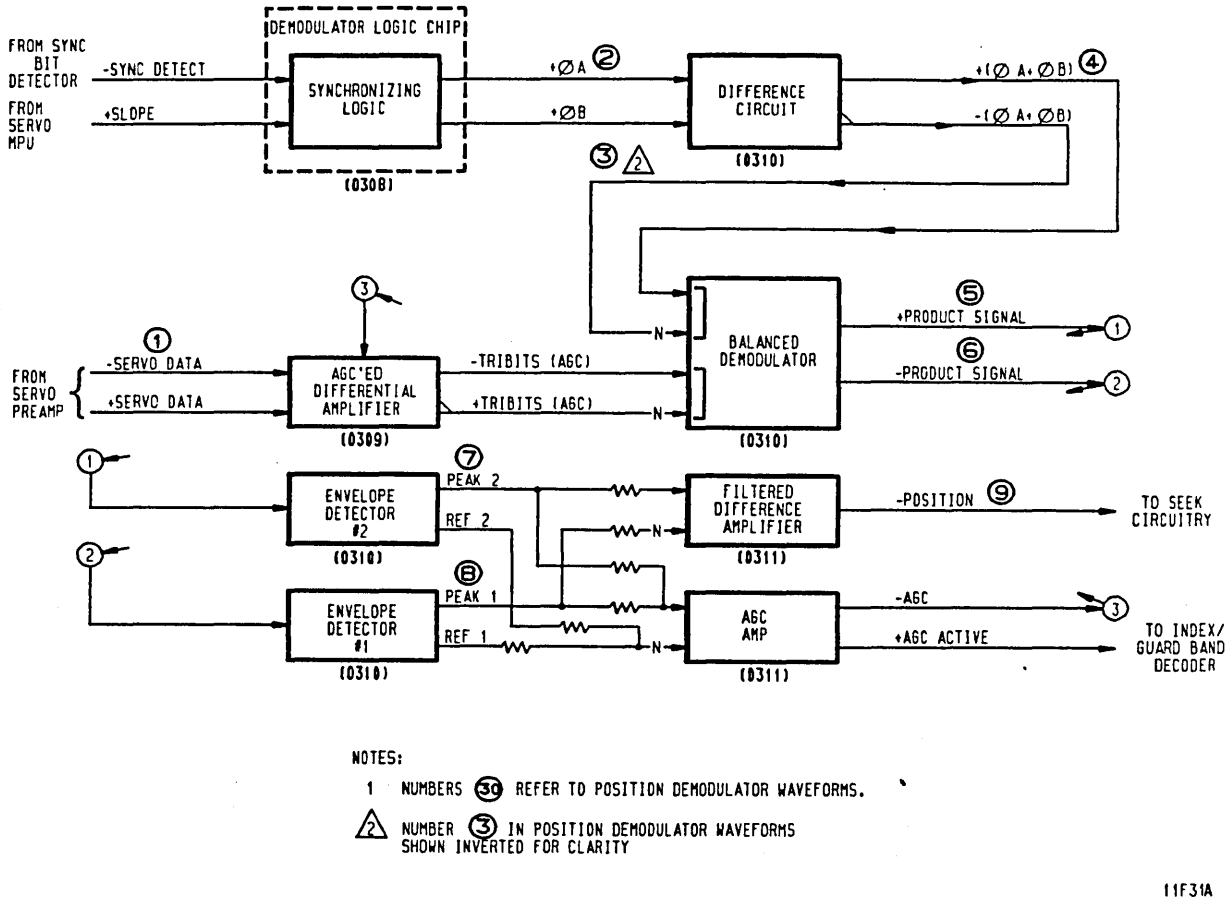


Figure 1-22. Position Demodulator Circuitry

logic in the Demodulator Logic Chip develops gating signals (+ØA and +ØB) that discriminate between the #1 bits and #2 bits. This logic is initialized when an Index pattern (resync pattern) occurs in the Tribit signal (see Index and Guard Band Decoding). Through the resync process, gating signals internal to the Demodulator Logic Chip are forced to match the format of the tribits as they were recorded on the servo surface.

These internal gating signals are output from the Demodulator Logic Chip as the +ØA and +ØB signals. However, the Servo MPU controls which internal gate becomes +ØA and which gate becomes +ØB via the +Slope signal. At the start of a new seek, the Servo MPU sets the level of the +Slope signal, thereby choosing whether or not to interchange the +ØA and +ØB signals. Interchanging them inverts the Position signal and allows the Servo MPU to ensure that the +Position signal will have the required slope as the seek circuits position the heads at their new destination. This slope requirement is discussed further under Seek Functions.

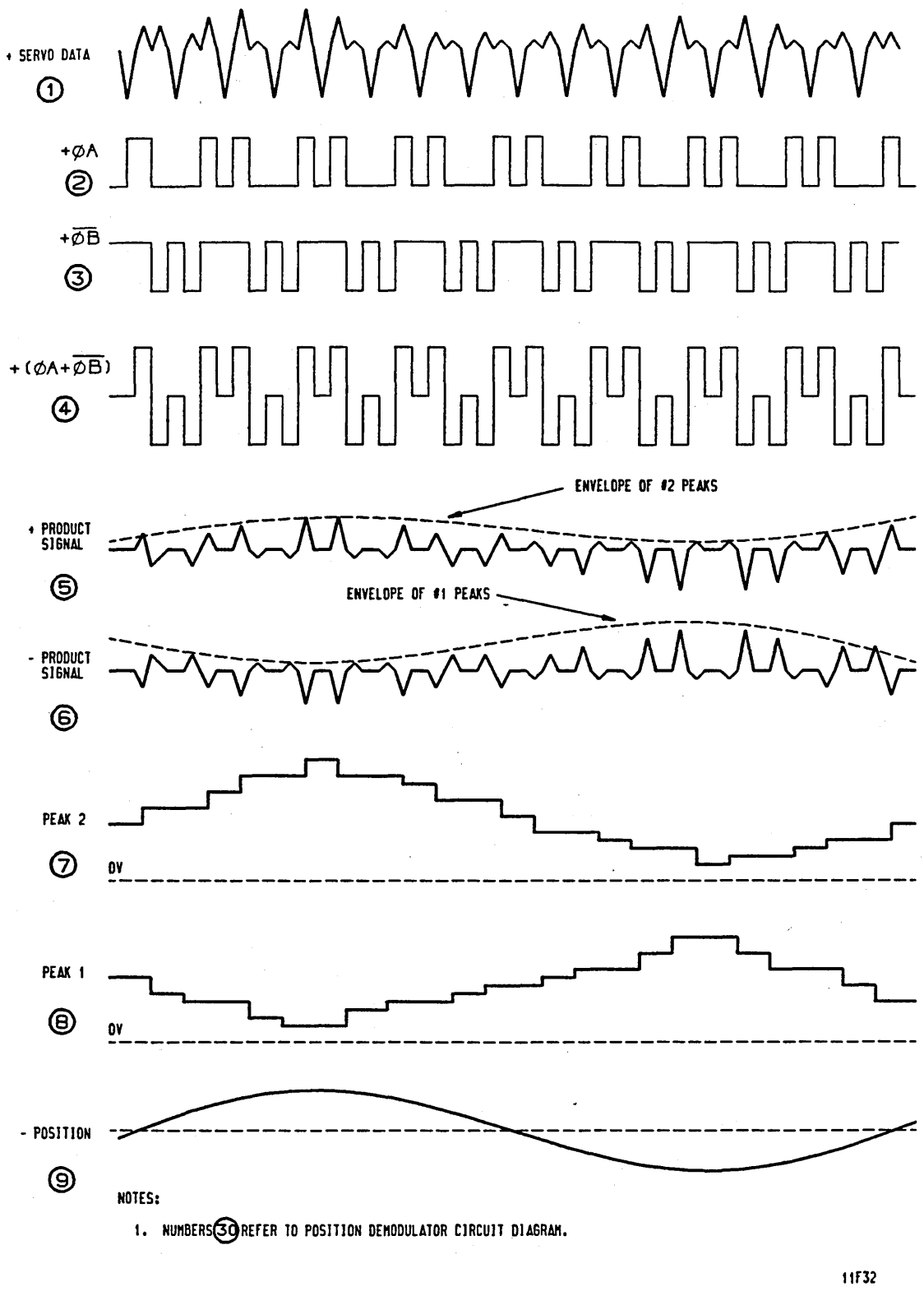


Figure 1-23. Position Demodulator Waveforms

As shown in figure 1-22, the balanced demodulator uses the +ØA and +ØB signals to develop, from the Tribits signal, input signals for the two channels of envelope detection. The balanced demodulator has two differential inputs: a three-step gating signal and an Amplified Tribits signal. The Amplified Tribits signal is produced from the Tribits signal by an AGC-controlled differential amplifier. A difference circuit develops the +(ØA + not-ØB) signal and its inverse from the +ØA and +ØB gates.

Figure 1-23 shows typical input and output waveforms for the balanced demodulator. The balanced demodulator multiplies the two input signals to create complementary product signals. Because the three-step gating signal is zero when sync bits appear, the product signals contain only position peaks. In the +Product signal, the #2 bits are positive and the #1 bits are negative. In the -Product signal, the opposite is true.

Although each envelope detector's input contains both positive and negative peaks, the detector is sensitive only to changes in the positive peaks. Each detector uses two transistors to update the voltage on a capacitor. In intervals where the envelope amplitude is increasing (successive peaks are more positive), one transistor pulls the capacitor voltage up. In intervals where the envelope amplitude is decreasing, the other transistor pulls the capacitor voltage down. Because this adjustment occurs at the instant of peak detection, the output signal from the detector steps to a new level, holding that level until the next peak. Additional transistors in each detector circuit act as current sources and provide temperature compensation.

The envelope detectors' outputs, the Peak 1 and Peak 2 signals, are differential inputs to a filtered difference amplifier. This stage develops the -Position signal by subtracting Peak 1 from Peak 2. It uses a low-pass filter to remove from the -Position signal any high frequency noise, resulting from the steps in the Peak 1 and Peak 2 inputs. The -Position signal is zero when the servo head is centered between two tribit tracks. At this time, the data heads are positioned directly over a data track. The -Position signal varies either positive or negative depending on displacement of the servo head from that centerline.

The AGC amplifier monitors the sum of the Peak 1 and Peak 2 signals, relative to the sum of two bias voltages (Ref 1 and Ref 2) from the envelope detectors, to produce an AGC voltage for the differential input amplifier. AGC action keeps the peak-to-peak amplitude of the -Position signal independent of servo signal variations. A level detector, connected to the AGC voltage, issues the +AGC Active signal to indicate that position demodulation is satisfactory. If the +AGC Active signal goes low or if valid decoding ceases (see the next topic), the -Demodulator Active line goes high, warning the Servo MPU that the tribit decoder is not functioning properly.

With one exception, movement of the servo head from one track to an adjacent track reverses the polarity of the Position signal. This is true when the servo head crosses tracks in the guard bands and the data zone. However, the buffer zone, located between the outer guard band and data zone, has two consecutive tracks that are recorded with identical (not alternating) position information. Thus, as the servo head moves across these tracks, the Position signal stays negative and does not cross zero as it does in the other zones. This characteristic of the Position signal is needed for Return to Zero seeks (see Seek Functions).

Index and Guard Band Decoding

The index and guard band decoding circuitry produces output pulses each time the servo head detects certain codes in the pattern of sync bits on the servo surface. This circuitry also originates the +Valid Decode signal which is used to indicate reliable decoder operation. Refer to Servo Surface Format for a description of the sync bit codes and their location on the servo disk.

Figure 1-24 is a block diagram of the index and guard band decoding circuitry. This circuitry is located in the Demodulator Logic Chip.

The decoding circuit responds to three timing signals that repeat in sequence for each tribit pattern detected. The synchronizing logic, controlled by the Servo PLO, issues the Sync Reset signal prior to the detection of each sync bit. If a sync bit is detected, a low pulse on the -Sync Detect line sets a FF. If no sync bit was detected, however, the FF remains reset. The next timing signal, Shift Clock, clocks the output of the FF into the first stage of a 9-bit shift register and produces a shift in the register.

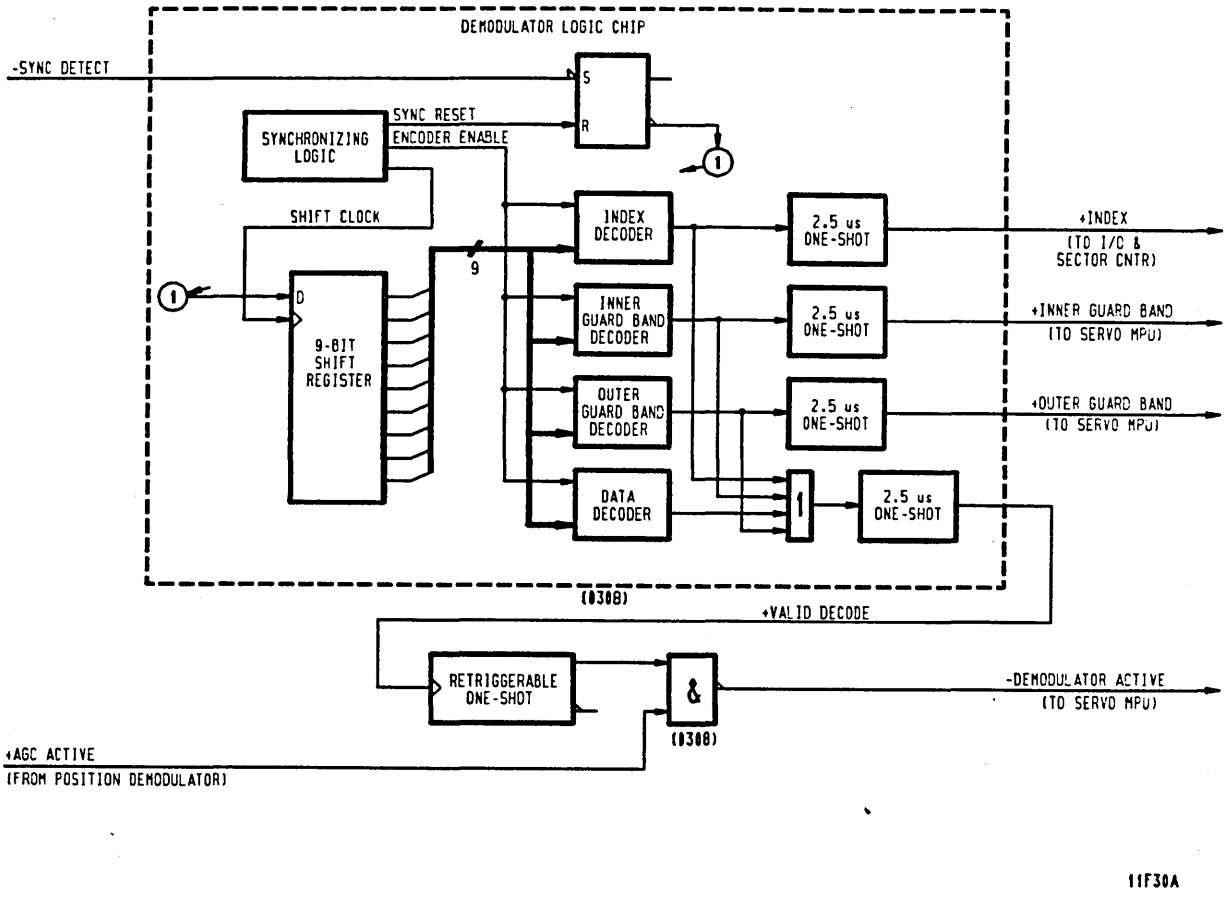


Figure 1-24. Index and Guard Band Decoder

The shift register contains information about whether a sync bit was present in each of the nine preceding tribit patterns. After clocking the shift register, the synchronizing logic activates a gate (Decoder Enable) that enables each of the decoder circuits shown in figure 1-23. Each decoder looks for a particular pattern of ones and zeros in the shift register's outputs corresponding to a code of missing sync bits on the servo track. The codes detected are as follows:

- When the register contains 101000101, the Index Decoder triggers two one-shots to activate the +Index and +Valid Decode lines for 2.5 microseconds.

- When the register contains 100010101, the Outer Guard Band Decoder triggers two one-shots to activate the +Outer Guard Band and +Valid Decode lines for 2.5 microseconds.

- When the register contains 101010001, the Inner Guard Band Decoder triggers two one-shots to activate the +Inner Guard Band and +Valid Decode lines for 2.5 microseconds.

- When the register contains 100010001, the Data Decoder triggers a one-shot to activate the +Valid Decode line for 2.5 microseconds. The Demodulator Logic Chip has no output corresponding to the code for the data zone.

When any of the above codes are present, a pulse is transmitted on the Valid Decode line. Pulses on the Valid Decode line are supplied as triggers to a retriggerable one-shot. During normal decoder operation, this one-shot stays set. If the oneshot times out, the -Demodulator Active line to the Servo MPU goes high to indicate improper decoding.

The Inner and Outer Guard Band signals are supplied as interrupts to the Servo MPU. These interrupts inform the Servo MPU that the heads are not located over the data zone. The Index signal is sent to the controller and is used by the Sector Counter, as described in the next topic. The Index pulse is also sent to the Current Sector Counter in the SMD-E Gate Array to be used as a reset.

Sector Detection (806 KHz Clock)

The sector detection circuit (figure 1-25) generates signals which are used by the drive to determine the angular position of the heads with respect to index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disks. The Sector pulses logically divide the disk into areas called sectors.

A Sector pulse is generated each time the Sector counter reaches its maximum count (4095). A carry from the counter triggers a 1.25 microsecond one-shot which generates the Sector pulse. The counter is incremented by the 806 kHz clock pulses, derived from the Servo PLO signal in the Demodulator Logic Chip. The Index pulse resets the counter allowing 13 440 clock pulses per revolution of the disk. The Index Pulse also resets the Current Sector Counter in the SMD-E Gate Array.

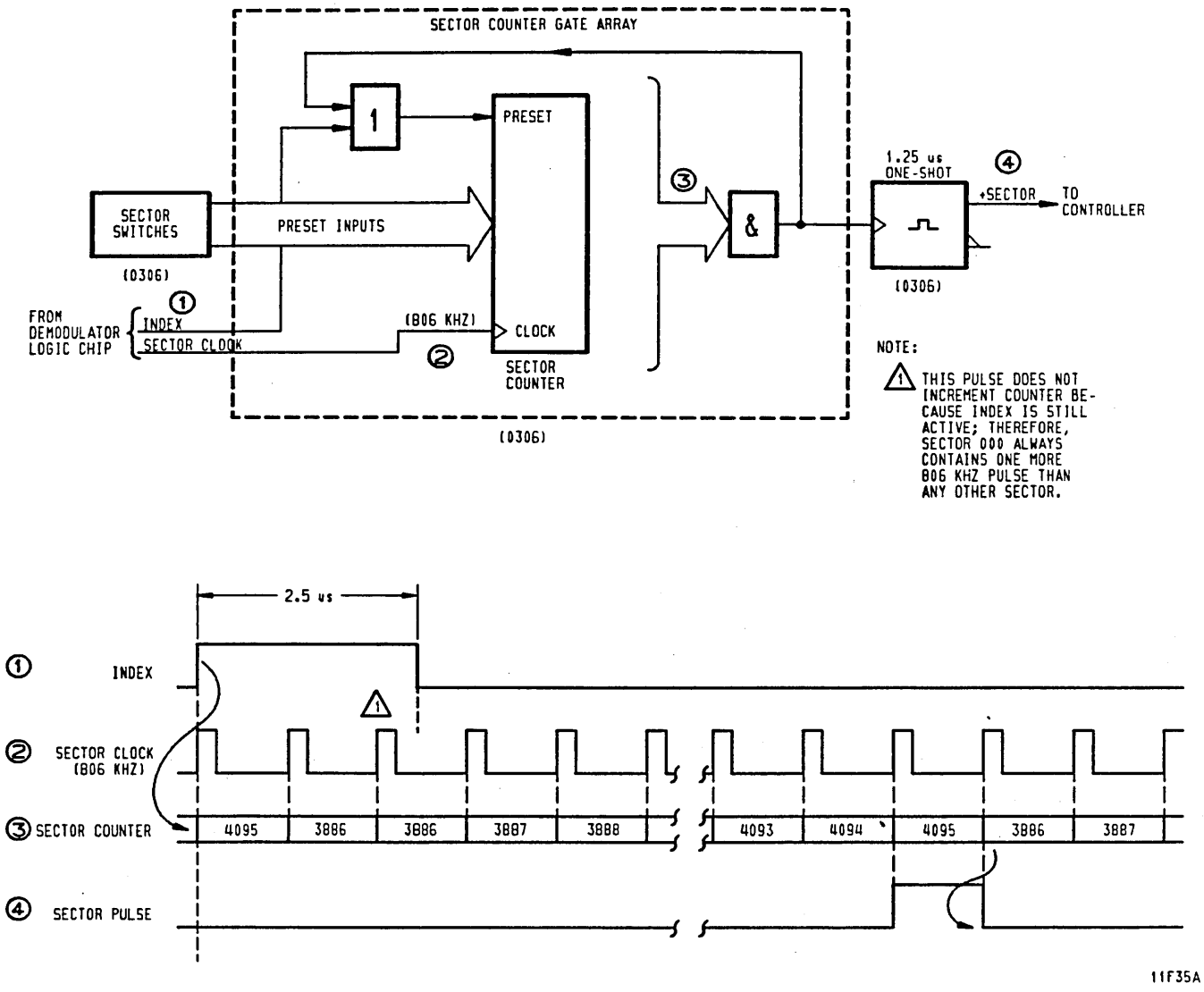


Figure 1-25. Sector - Logic and Timing (806 KHz)

The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution. This is done by presetting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors, the counter would have to count 210 clock pulses in each sector (13 440 divided by 64) and the counter would be preset to 3886. In this case, the counter starts at 3886 and increments each clock time until it reaches the maximum count (4095). Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (210) presets the counter back to 3886 and the counter begins the next sector.

The sector length is varied by presetting the sector switches located on the control board. Refer to volume 1 of the maintenance manual for details regarding the setting of the sector switches.

The Current Sector Counter in the SMD-E Gate Array provides an address from 0-255 to be transmitted to the controller on Bus In bits 0 through 7 when the controller issues a Tag 4 command. The range of addresses is dependent on drive sector switch settings on the control board. The Current Sector Counter is reset by each Index pulse and incremented by Sector pulses.

Sector Detection (1.612 MHz Clock)

The sector detection circuit (figure 1-26) generates signals which are used by the drive to determine the angular position of the heads with respect to index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disks. The Sector pulses logically divide the disk into areas called sectors.

A Sector pulse is generated each time the Sector counter reaches its maximum count (4095). A carry from the counter triggers a 1.25 microsecond one-shot which generates the Sector pulse. The counter is incremented by the 1.612 MHz clock pulses, derived from the Servo PLO signal in the Demodulator Logic Chip. The Index pulse resets the counter allowing 26 880 clock pulses per revolution of the disk. The Index Pulse also resets the Current Sector Counter in the SMD-E Gate Array.

The fact that the same number of 1.612 MHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution. This is done by presetting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors,

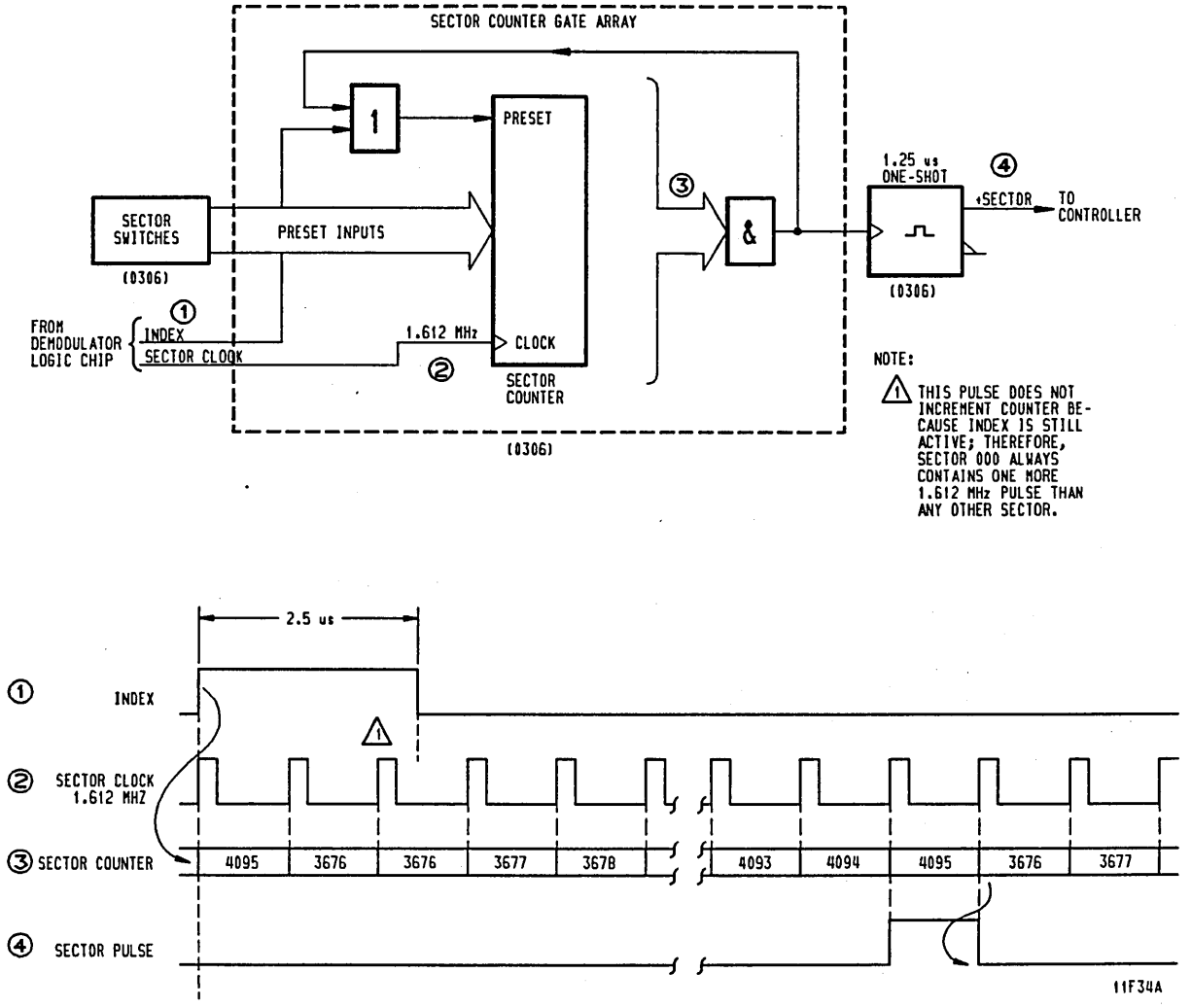


Figure 1-26. Sector Detection - Logic and Timing (1.612 MHz)

the counter would have to count 420 clock pulses in each sector (26 880 divided by 64) and the counter would be preset to 3676. In this case, the counter starts at 3676 and increments each clock time until it reaches the maximum count (4095). Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (420) presets the counter back to 3676 and the counter begins the next sector.

The sector length is varied by presetting the sector switches located on the control board. Refer to volume 1 of the maintenance manual for details regarding the setting of the sector switches.

The Current Sector Counter in the SMD-E Gate Array provides an address from 0-255 to be transmitted to the controller on Bus In bits 0 through 7 when the controller issues a Tag 4 command. The range of addresses is dependent on drive sector switch settings on the control board. The Current Sector Counter is reset by each Index pulse and incremented by Sector pulses.

SEEK FUNCTIONS

GENERAL

During seek operations, the drive positions the heads over the desired cylinder on the disk. The drive servo circuits, under the direction of the Servo MPU, control this function. The drive servo circuits translate Servo MPU instructions into electromechanical motion to position the read/write heads accurately and to allow the transfer of magnetic pulses to and from a disk storage surface. The two main topics of this section describe servo circuit operation and the sequencing of events in different types of seeks. Since these subjects are interrelated, they are preceded by an overview of system operation that explains the roles played by the interface and the Servo MPU, and that describes the servo functions in general terms.

SYSTEM OVERVIEW

Each seek operation can be described in terms of four basic drive activities. These activities are shown in terms of general information flow between major drive functional elements in figure 1-27. These activities occur in the following sequence:

- Command -- The Control MPU processes the command from the controller that instructs the drive to seek to a different cylinder on the disks.

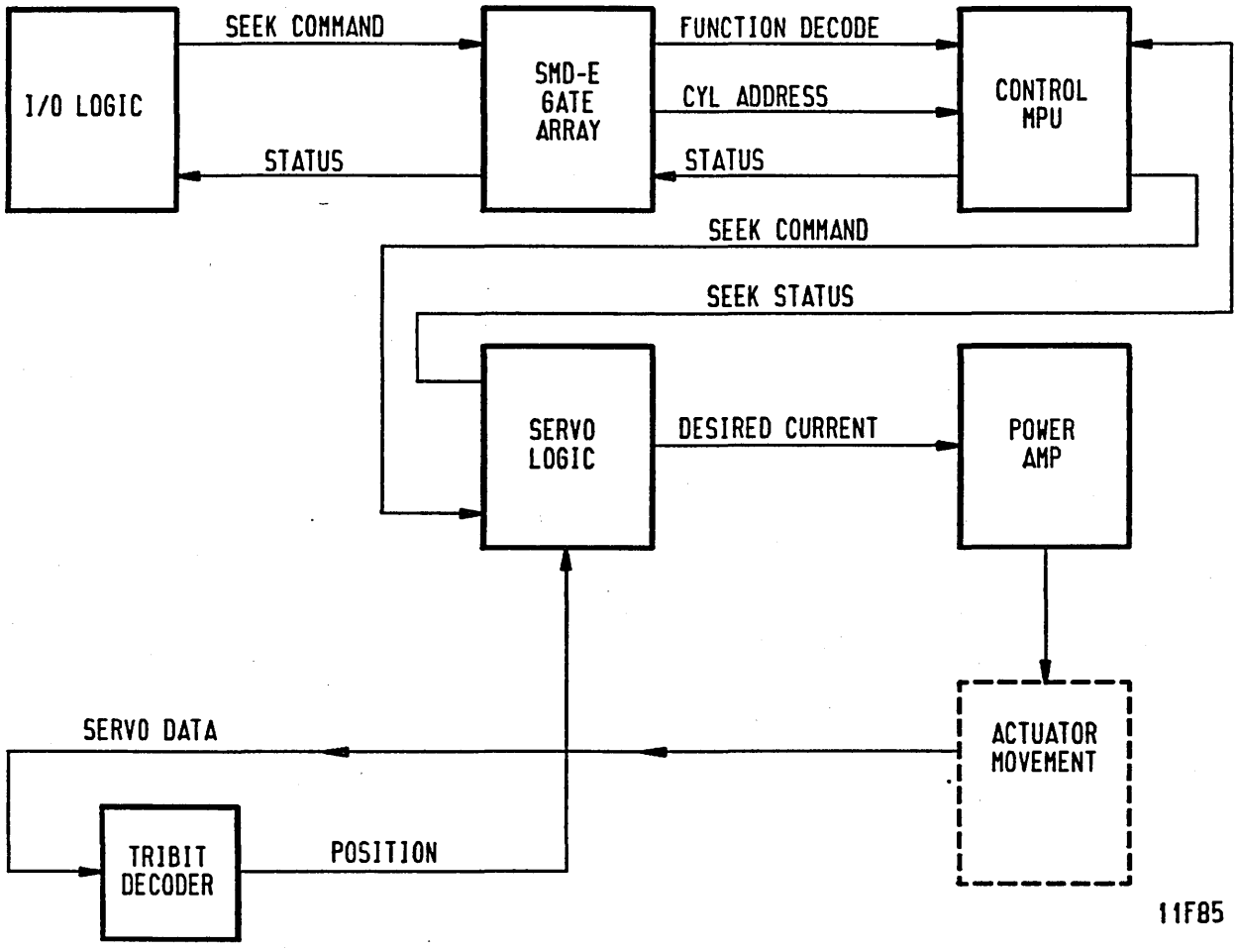


Figure 1-27. Seek Functions Block Diagram

- Control -- The Control MPU sends a seek command and destination address to the Servo MPU. The Servo MPU interprets the seek command, then translates the command into a sequence of controls sent to the servo circuitry. These controls dictate the direction of the seek, specify actuator velocity throughout the seek, and step the servo through its operating modes.

- Execution -- The servo circuitry executes the seek in response to control information received from the Servo MPU. This execution is accomplished in three modes: the coarse mode, during which the actuator is moved at a controlled velocity toward its destination; the settle-in mode, in which the actuator locks in to its final position; and the track-following mode, in which the actuator position is maintained until another seek is commanded. The Servo MPU controls current to the voice coil to move the actuator/heads via a desired current signal to the power amplifier. Position information from the tribit decoder serves as a feedback source to the servo loop and is converted into cylinder crossing information for the Servo MPU.

- Status -- The Servo MPU informs the controller via the the Control MPU whether or not the seek was accomplished successfully. This indicates whether or not a reliable data transfer can be performed on the selected cylinder.

The concept of a closed loop is essential to understanding the operation of the servo system. Figure 1-28 shows a generalized servo loop that illustrates several principles governing the servo loops in the drive. Throughout the servo operation, the Servo MPU processes various inputs. If the combination of inputs to the Servo MPU indicates that the servo is unbalanced,

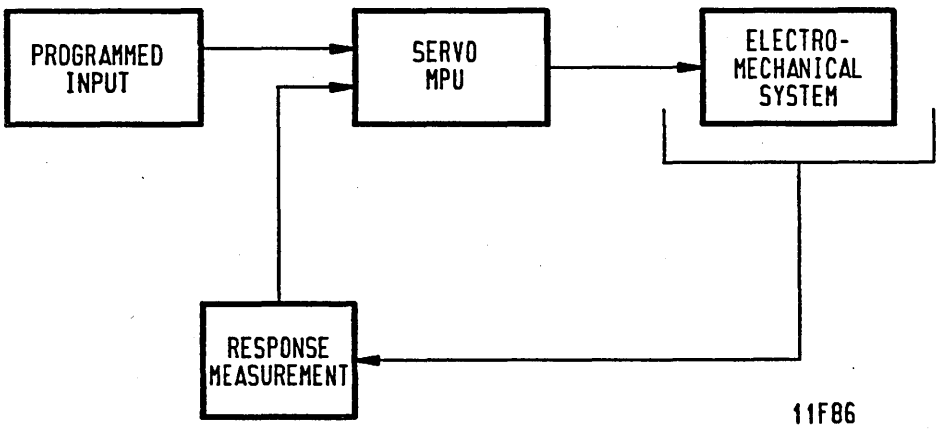


Figure 1-28. Generalized Servo Loop

the Servo MPU issues a correction to the electro-mechanical system. The response of the mechanical system is converted into an electrical signal which is an input to the Servo MPU. Mechanical movement continues until the system balance is restored, corresponding to a null in the Servo MPU inputs.

The drive employs two basic servo loops, a coarse loop used in the coarse mode and a fine loop used in the settle-in and track-following modes. In figure 1-29, the model of figure 1-28 is used to show the coarse servo loop in simplified form. In the coarse loop, the actuator moves at a prescribed velocity from the original cylinder address to the final cylinder address. The Servo MPU refers to tabulated values of desired velocity required for the seek profile and measures actual velocity throughout the seek. When the desired velocity exceeds the measured velocity, desired current is increased to accelerate the actuator. When the measured velocity exceeds the desired velocity, desired current is reduced to decelerate the actuator. The actuator is allowed to coast when the two inputs are equal.

In figure 1-30, the model of figure 1-28 is used to show the fine servo loop in simplified form. In the fine loop, the heads settle-in to their destination position and then maintain their position on track. Any displacement of the heads from track center is adjusted by passing the servo data through a digital filter circuit and using the output to develop a desired current correction to the power amplifier.

The following paragraphs discuss the circuit operation of these loops in more detail and then go on to describe the sequence of events in typical seeks.

SERVO CIRCUIT FUNCTIONS

General

Where applicable, servo circuit functions are discussed in terms of the two basic loops within the servo circuitry (coarse and fine loops). With the exception of the cylinder pulse counter in the Peripheral Array, the coarse loop and the fine loop use the same circuit elements. These circuit elements are described in detail under the following topics:

- Servo MPU (including associated Peripheral Array logic)
- Desired Current Generator
- Cylinder Pulse Detection
- Position Sampling Circuitry
- Power Amplifier

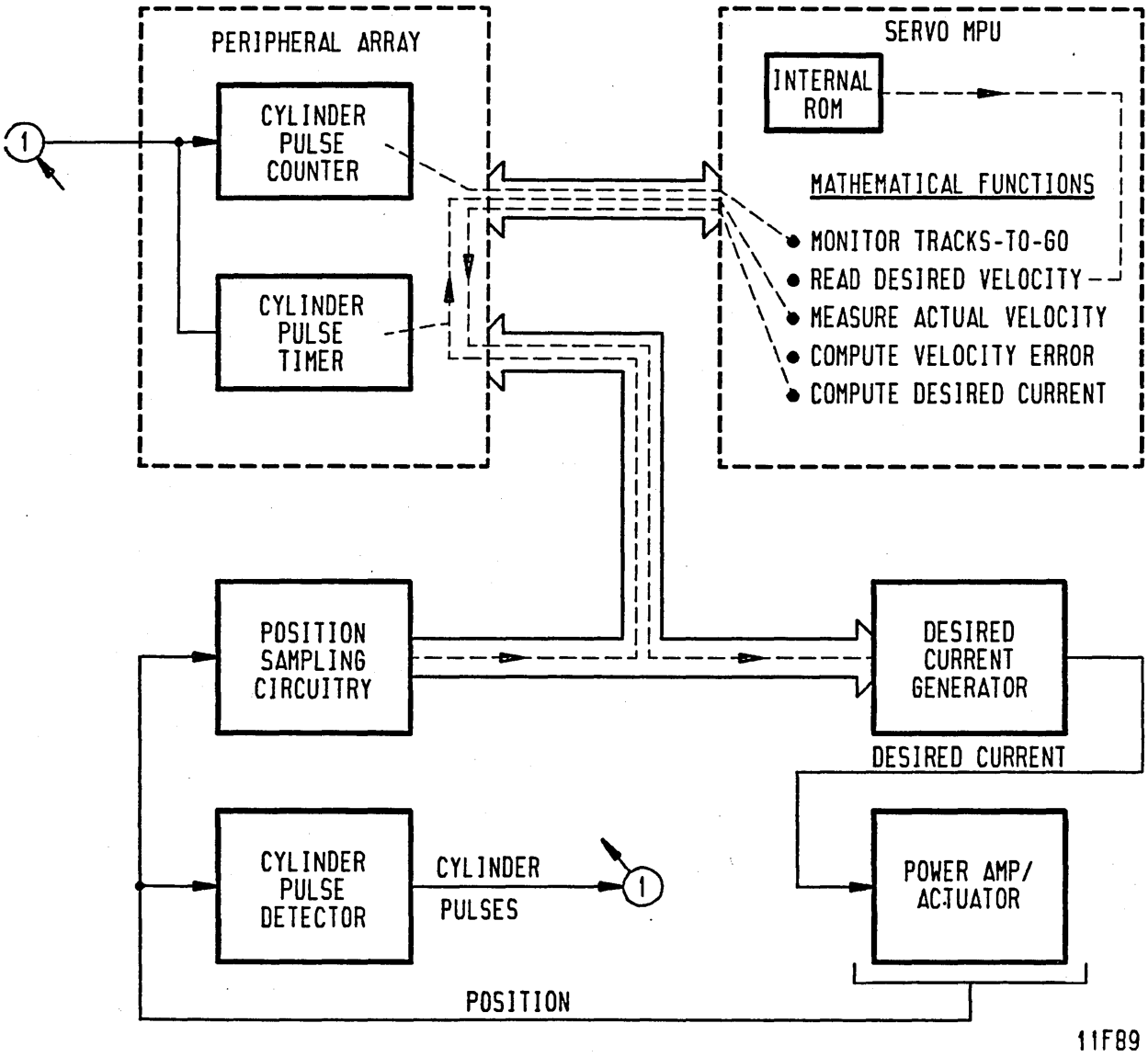


Figure 1-29. Simplified Coarse Servo Loop

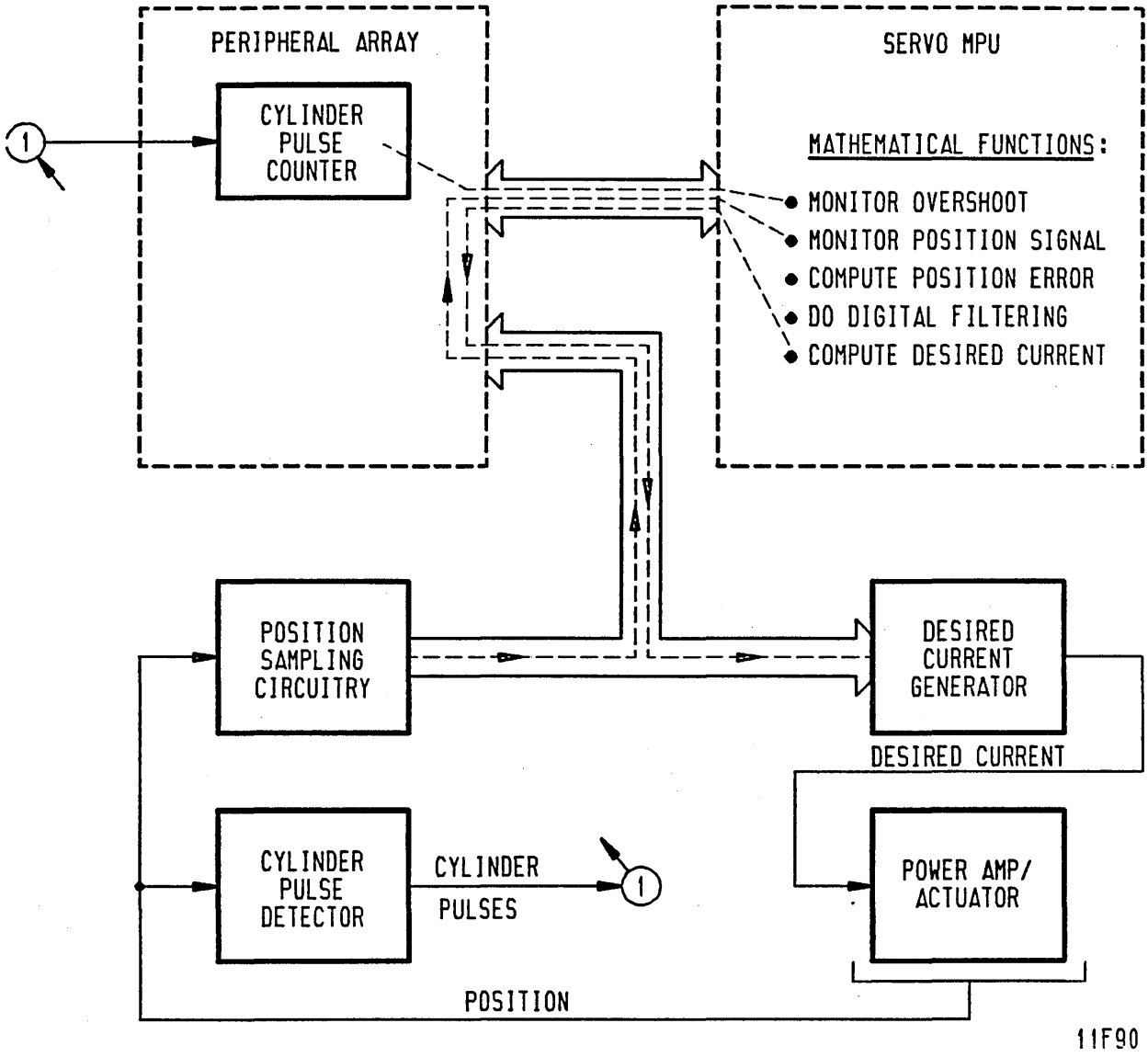


Figure 1-30. Simplified Fine Servo Loop

Servo MPU

The Servo MPU initiates the seek, determines the direction, and periodically adjusts the speed of the actuator to ensure seek completion in the shortest possible time without overshoot. Firmware instructions for the Servo MPU reside in ROM. The ROM also contains a lookup table used to index a velocity table for normal seeks. The following paragraphs provide a general description of the functions performed by the Servo MPU.

The Peripheral Array allows the Servo MPU to monitor the digital levels of certain signals developed in external hardware and also to communicate with the Control MPU. Certain inputs to the Peripheral Array from the Control MPU form maskable interrupts to the Servo MPU. When unmasked, these interrupts inform the Servo MPU of status changes that require switching to a different routine within its firmware. The Servo Data Bus connects the Servo MPU to the Peripheral Array. The Control Bus connects the Control MPU to the SMD-E Gate Array and the Peripheral Array. This bus allows the Control MPU to perform various operations inside the SMD-E Gate Array in response to inputs from the Servo MPU, such as setting the On Cylinder and Seek Error FFs, multiplexing cylinder addresses out of the array, and reading various fault statuses.

The cylinder pulse counter in the Peripheral Array allows the Servo MPU to count tracks-to-go in a seek. This counter is decremented during seeks by Cylinder Pulses. When operating in coarse mode, the cylinder pulse timer, also located in the Peripheral Array, allows the Servo MPU to determine the elapsed time between cylinder pulses.

The Servo MPU performs the following basic functions during drive operation:

- It examines the destination address from the Control MPU to determine desired velocity and seek direction.
- It monitors actual velocity and uses this information to adjust the amount of current applied to the actuator to ensure that the seek conforms to the predetermined velocity profile.

- It transmits data to the Control MPU to allow it to control selected registers and latches in the SMD-E Gate Array and the status/control panel (if installed).

- It transmits data to the Control MPU to enable the Control MPU to perform diagnostic functions in response to inputs entered on the status/control panel.

Diagnostic operations are described in detail under Diagnostic Functions. In addition, the Servo MPU transmits error status to the Control MPU. This activity is discussed under Fault and Error Conditions.

Coarse Loop Operation

The servo system, operating in the coarse loop, moves the heads from the existing cylinder address to within one-half track of the new address. Throughout the coarse seek, the Servo MPU refers to a table in ROM that specifies desired velocity as a function of the number of track crossings (T) remaining until the heads reach their destination.

The velocity table is organized in a manner that allows one table of values to be used for all seeks. The maximum velocity of the table is for 255 tracks, and as the values decrease, a velocity profile is developed whereby velocity is proportional to the square root of the distance remaining. This profile produces constant deceleration of the heads in order to minimize seek times while controlling the approach of the heads to their final position. An organization of tabulated velocity in terms of tracks to go makes it possible to use one table for all seeks. Different seek lengths start at different points within the table. For example, the velocity specified when T=30 is the same regardless of the total seek length.

At each cylinder crossing, the Servo MPU refers in ROM to the current value of desired velocity. It then compares the current value of desired velocity to actual velocity and computes the difference (error value). Until the next cylinder crossing, the Servo MPU continues to update its computation of desired current based on the computed error value and to output desired current information to the power amplifier.

A continuous indication of actuator velocity is needed throughout a seek operation. Two methods are used to compute velocity during coarse loop operation: one method for the high speed portion of a seek (T greater than 5), and another method for the low speed portion (T less than or equal to 5). During the high speed portion of the seek operation, the Servo MPU divides the track spacing by the time required to move between cylinders and uses the quotient as a correction to desired current. During the low speed portion of the seek operation, the Servo MPU computes the derivative of the linear portion of the Position signal and uses the outcome as a correction to desired current. During the linear portion, the differentiated position outputs are proportional to velocity because velocity is the time rate of position change.

Fine Loop Operation

The servo system shifts from the coarse loop to the fine loop when there is 1/2 track remaining in the seek. Fine loop operation continues until the beginning of the following seek.
In fine loop operation, the servo system adjusts the position of the actuator to ensure that it does not overshoot the destination track.

At the start of a seek, the Servo MPU sets or clears the +Slope input to the Tribit Decoder to ensure that +Position goes positive as the heads move inward and negative as the heads move outward from their destination track. The +Position signal is zero with the heads exactly on track.

This relationship is true for every destination track on the disk. Thus, with some modification, a digitized +Position is a suitable error signal for the Servo MPU in the fine loop. The modification takes into account the following considerations:

- Stability of fine servo loop -- requires the addition of digital filtering to the differentiated error signal.
- Servo offsets -- allow the controller to reposition the heads to either side of track center to recover read errors.
- Increased gain in track-following mode -- gives the servo more responsive control when keeping the heads on track.

Upon entering the settle-in stage of fine loop, the Servo MPU computes a proportional derivative error by adding the value of position as it approaches zero to the derivative of position (velocity). The error signal is then passed through a series of digital filters. The compensated position error value is converted directly into a voltage level that corresponds to desired current. An additional error value is added to the position error value if servo offset is selected. See Servo Offsets.

After completing the settle-in stage, the Servo MPU enters the track-following stage. In the track-following mode, the servo maintains the heads on cylinder until a new seek command appears. When operating in track-following mode, the Servo MPU passes the error signal through an additional integrating filter network to increases the gain at low frequencies and thereby prevent overshooting and drifting off track.

The Servo MPU derives on cylinder sense by examining the voltage level of the +Position signal. When the position signal voltage remains within the limits defining on cylinder sense, the Servo MPU provides status to the Control MPU via the Peripheral Array. In response, the Control MPU issues On Cylinder status to the SMD-E Gate Array.

Servo Offsets

An offset, a dc shift of the position signal, results when the controller issues a Servo Offset command in order to recover marginal read data. When the SMD-E Gate Array decodes Servo Offset Plus (Tag 3 and Bus Out bit 2), it activates a bit in its status register and transmits an I/O Interrupt to the Control MPU. When the SMD-E Gate Array decodes Servo Offset Minus (Tag 3 and Bus Out bit 3), it activates a different bit in its status register and transmits an I/O Interrupt to the Control MPU.

After receiving an interrupt from either offset command, the Control MPU checks the status of the registers and latches in the SMD-E Gate Array. Assuming no faults are present, the Control MPU sends an offset command to the Servo MPU. The offset command contains the amount of offset and the direction of the offset.

With an offset command in effect, the Servo MPU shifts the voltage limits defining on cylinder sense. Servo Offset Plus displaces the heads inward from the track center, and Servo Offset Minus displaces the heads outward from track center.

Desired Current Generator

The desired current generator shown in figure 1-31 develops a -Desired Current analog signal that is equivalent to the 8-bit digital code received from the Servo MPU on the Servo Data Bus. The Servo MPU activates the -D/A Enable signal whenever a new value is available on the Servo Data Bus. The -Servo Reset signal is activated by the Control MPU during power up or servo system failure.

Cylinder Pulse Detection

A Cylinder Pulse is generated each time the heads cross a servo track during the coarse seek operation. Cylinder pulses decrement a counter in the Peripheral Array, keeping its difference count equal to the number of tracks to go in the seek; this points the Servo MPU to the correct tabulated velocity value which is stored in ROM.

During a seek, the Position signal from the Tribit Decoder alternates between positive and negative values (see Servo Surface Decoding discussion). Each zero-crossing of the Position signal corresponds to a cylinder crossing. Figure 1-32 provides a simplified logic diagram and waveforms for this circuit.

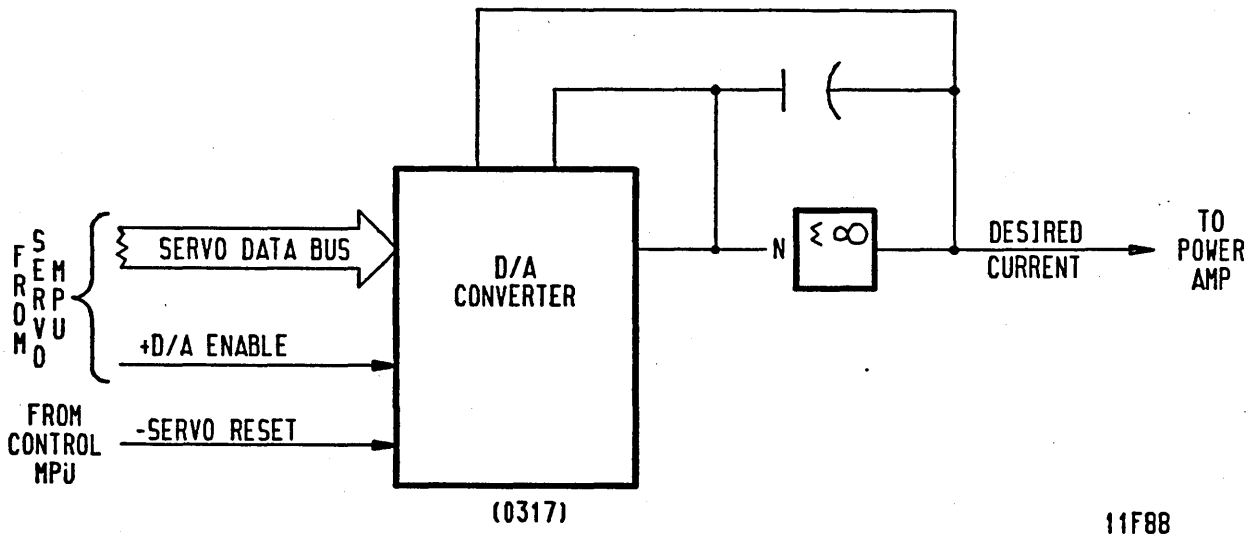


Figure 1-31. Desired Current Generator

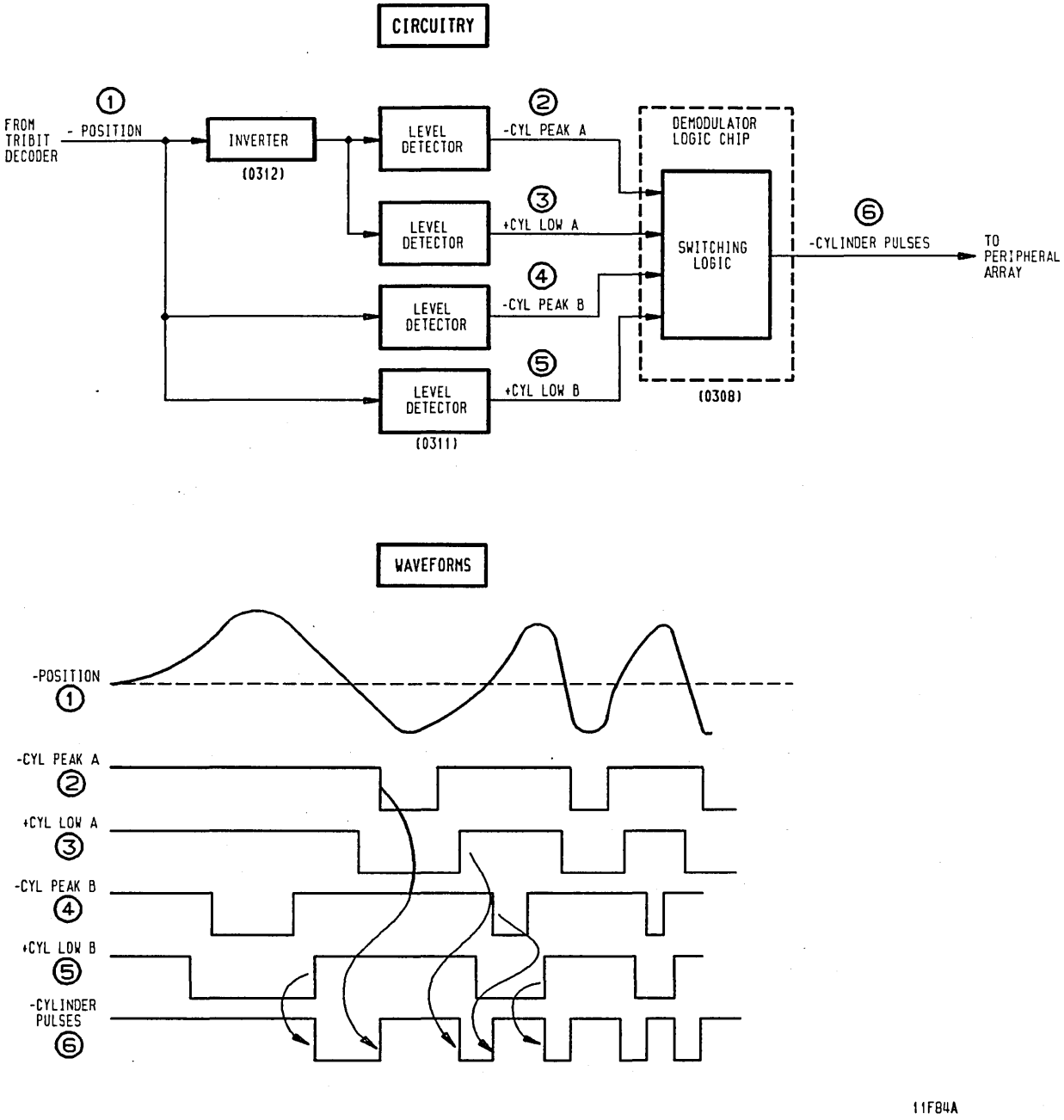


Figure 1-32. Cylinder Pulse Circuitry and Waveforms

The cylinder pulse detector uses four level detectors in conjunction with switching logic located in the Demodulator Logic Chip. The two level detectors, designated "A", monitor the +Position signal, and the two level detectors, designated "B", monitor the -Position signal. Each level detector switches its output signal at unique levels, based on its thresholds and hysteresis. The "A" level detectors recognize zero-crossings and position peaks of one polarity by activating the +Cylinder Low A and the -Cylinder Peak A lines respectively. Similarly, the "B" level detectors recognize zerocrossings and position peaks of the other polarity by activating the +Cylinder Low B and the -Cylinder Peak B lines.

The four level detector outputs supply control signals to switching logic in the Demodulator Logic Chip. In developing the -Cylinder Pulses signal, this logic must sense a position peak prior to responding to a position zero-crossing. Figure 1-32 shows how transitions in the four input signals produce the changes in the -Cylinder Pulses signal. This design ensures that only one Cylinder Pulse is generated for each zero crossing of the Position signal.

Position Sampling Circuitry

The Position Sampling circuitry shown in figure 1-33 samples the +Position signal at 20 microsecond intervals during coarse mode and fine mode operation. It is active during the low velocity portion of a seek (T equal to 5 or less), and also when the actuator is track-following. It is inactive during the high velocity portions of the seek, and also when the actuator is not on cylinder due to an error condition. When the +Sample/-Hold signal input to the sample and hold circuit is high, the analog values present on the +Position signal are gated to the input of the A/D converter. During the A/D conversion, the Servo MPU freezes the input signal to the A/D converter by forcing the +Sample/-Hold signal to go low preventing the output of the sample and hold circuit from changing value. The A/D converter converts the analog Position signal into a digitized Position signal. The Servo MPU starts the conversion by activating the +A/D Start line. Data is gated out of the A/D converter when the -A/D Enable 0 line goes low.

Power Amplifier

The power amplifier, acting on inputs from the desired current generator, produces the actuator current required by the servo loop. Figure 1-34 is a simplified drawing of the power amplifier circuitry.

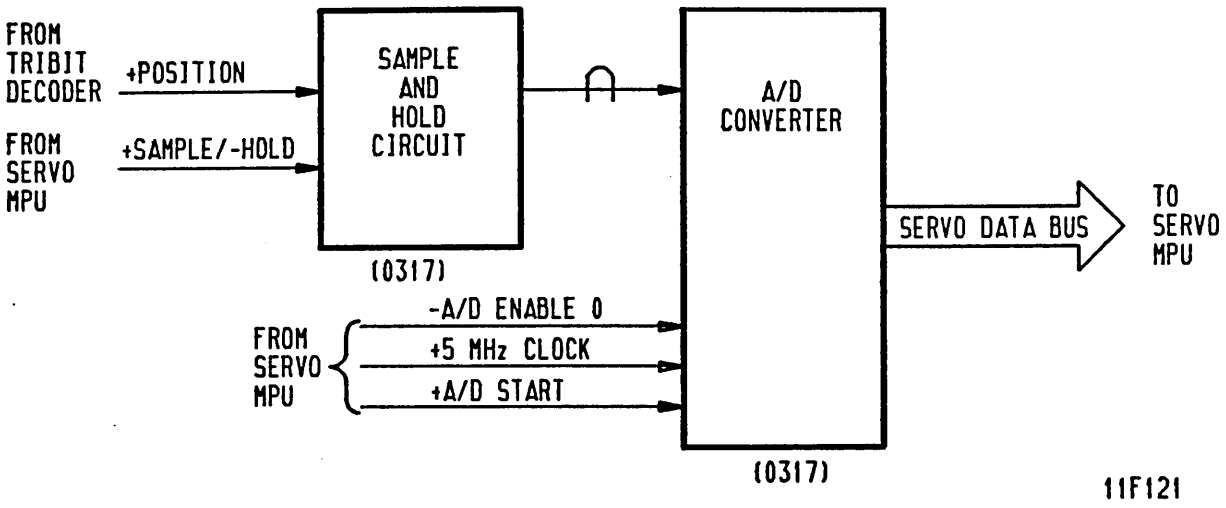


Figure 1-33. Position Sampling Circuitry

When negative actuator current is required, the power amplifier transmits current to the voice coil on the -VC line and returns this current on the +VC line. Current is sent through these lines in the opposite direction when positive actuator current is required. The corresponding In Direction Amplifier or Out Direction Amplifier circuit amplifies this input current and regulates current flow from ground through the sampling resistor and the actuator coil to +24 V. In direction actuator current forces the actuator to accelerate during a forward move and to decelerate during a reverse move. Out direction actuator current forces the actuator to accelerate during a reverse move and to decelerate during a forward move.

The power amplifier generates in drive or out drive currents in response to the voltage level on the +Desired Current line from the desired current generator. The in direction amplifier and out direction amplifier are each configured with a feedback loop consisting of a sampling resistor and a comparator. This circuitry monitors the +Desired Current line and adjusts the biasing to the corresponding in drive amplifier and out drive amplifier in accordance with +Desired Current voltage amplitude and polarity.

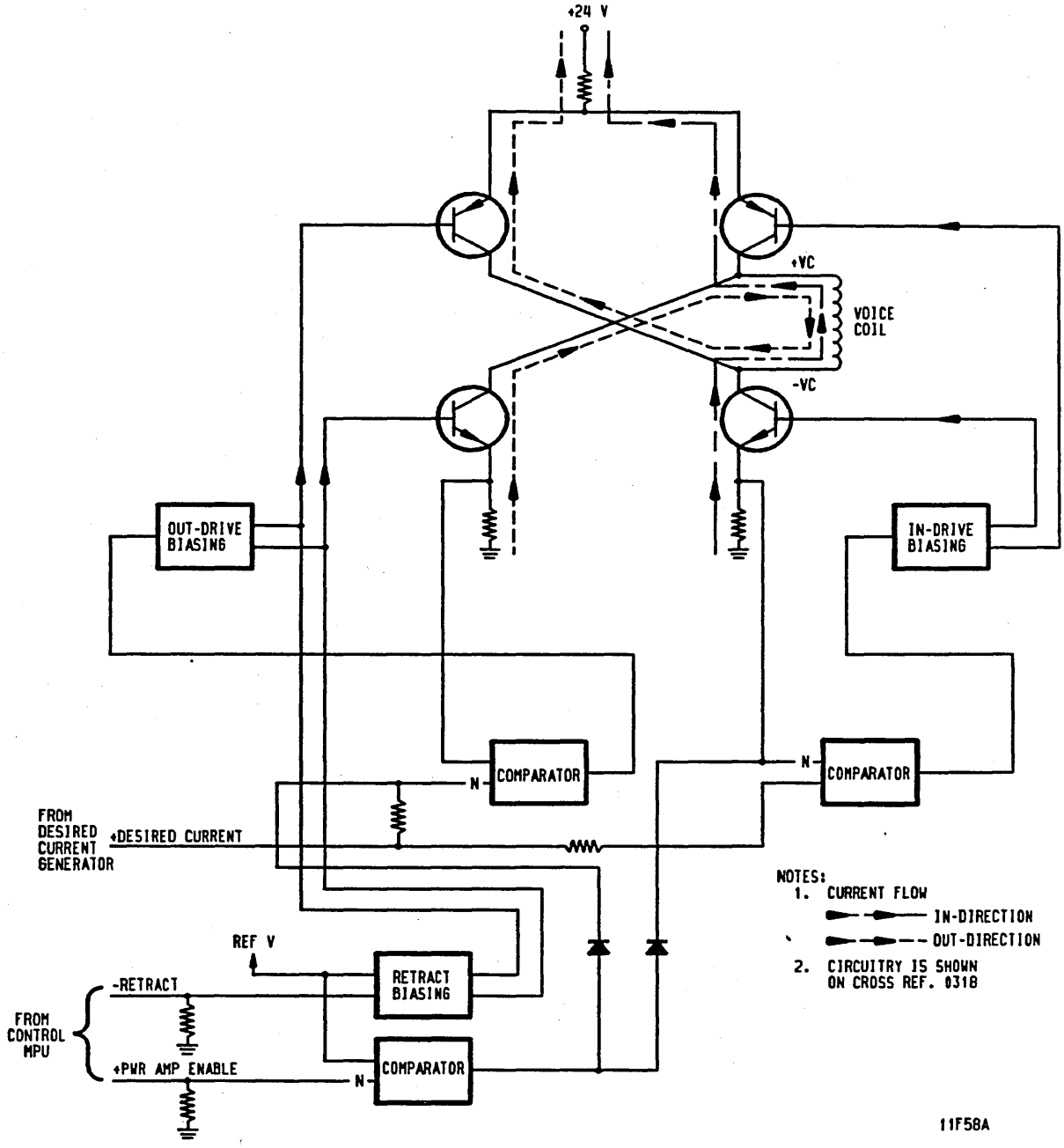


Figure 1-34. Power Amplifier Circuitry

A retract operation moves the actuator outward until the heads are located in the landing zone. The Servo MPU uses the +Desired Current line for normal head unloading before powering down the spindle. The +Desired Current line is also used to retract the heads when a loss of motor speed is detected. During an emergency retract operation, a low on the -Retract line and a low +Power Amp Enable signal from the Control MPU (via the Peripheral Array) as the result of a power loss (-Low VCC active) activates a separate biasing circuit feeding the out drive amplifier. Because the power amplifier and motor control circuitry operate from the same +24 volt source voltage, a power loss enables the power amplifier to be energized by the decelerating drive motor acting as a generator.

TYPES OF SEEKS

General

The drive has four basic types of seeks: the load operation, normal seek, return to zero (RTZ) seek, and unload operation. The load and RTZ operations use both the outward and inward movements to move the actuator to track 0. The unload operation is an outward movement that moves the heads to the landing zone beyond the outer guard band. Normal seek operations can be either inward or outward movements, depending upon where the new address is located relative to the present address. Upon successful completion of a load, normal seek, or RTZ operation, the Servo MPU remains active and continues to maintain the actuator on track. The four basic seek operations and track following are discussed in the following text.

Several firmware sequences are common to some or all of the seek operations mentioned above. These sequences are duplicated in each flowchart to avoid the need to refer the reader outside the flowchart in question.

Load Operation

The load operation starts the drive motor and moves the heads from the retracted position to track 0. A load operation cannot take place until power on initialization is successfully completed. Refer to the Power Functions discussion for details about power on initialization. The load operation is described in the following paragraphs and is flow-charted in figure 1-35.

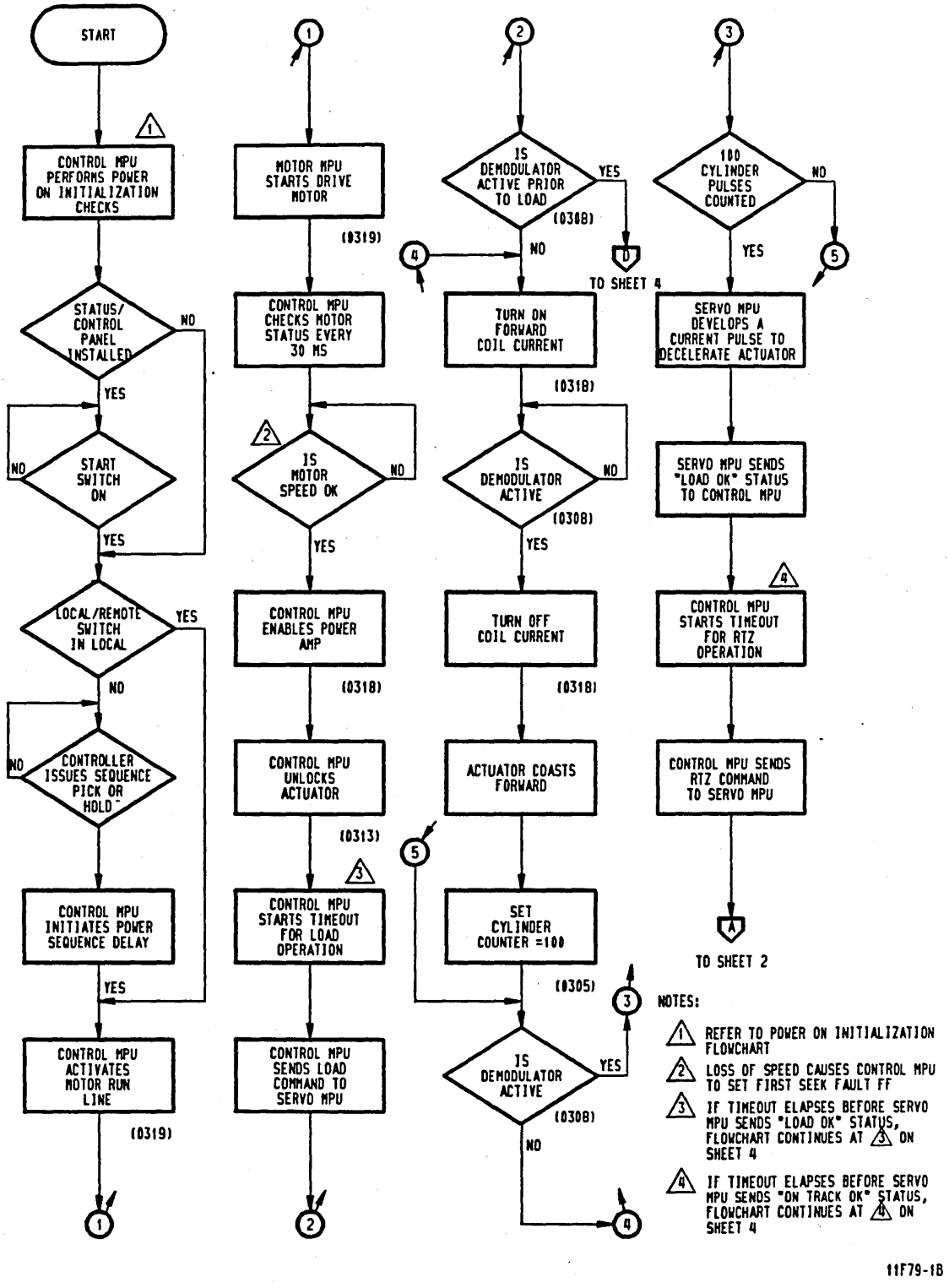


Figure 1-35. Load Operation Flowchart (Sheet 1 of 4)

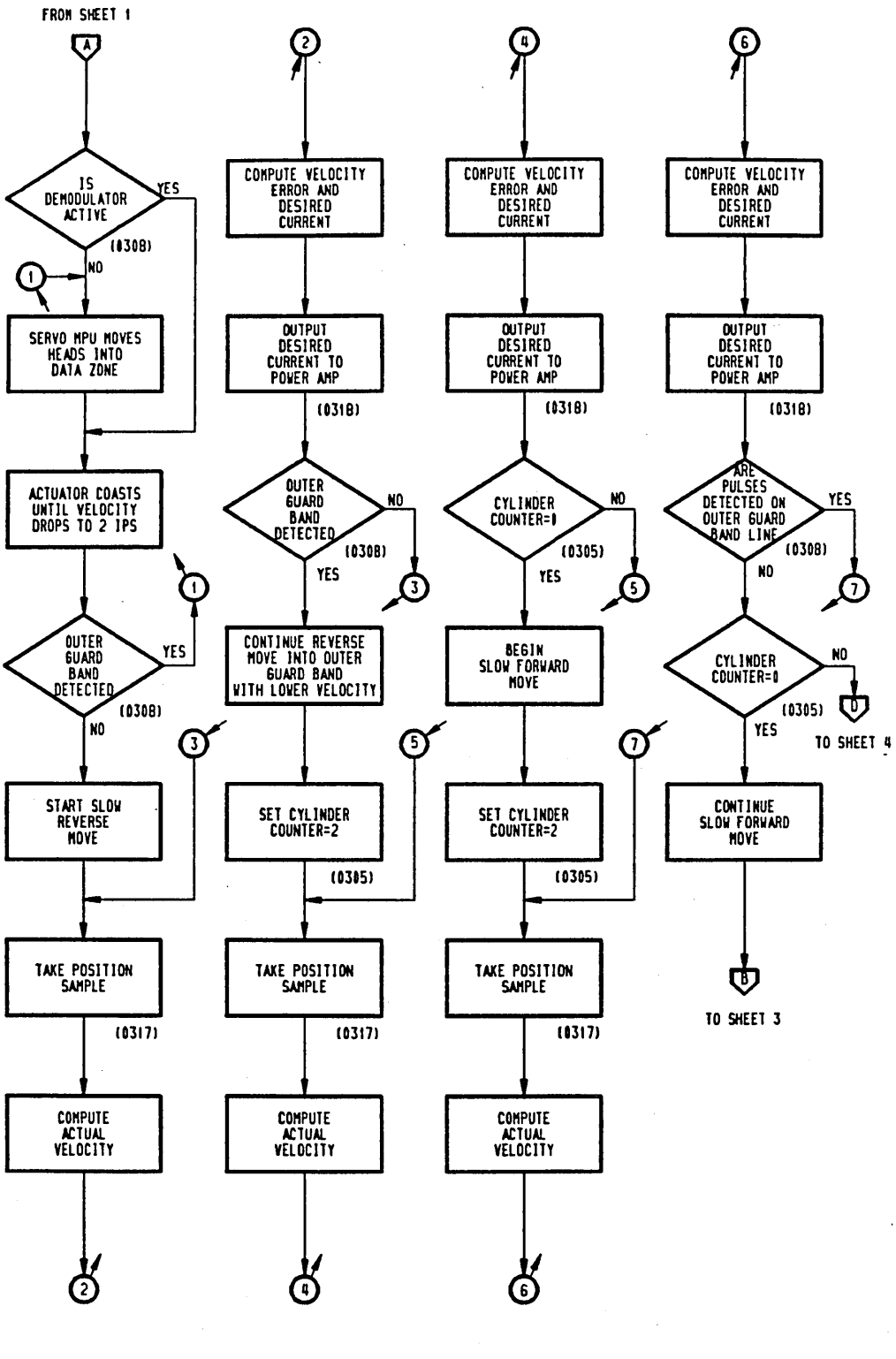


Figure 1-35. Load Operation Flowchart (Sheet 2)

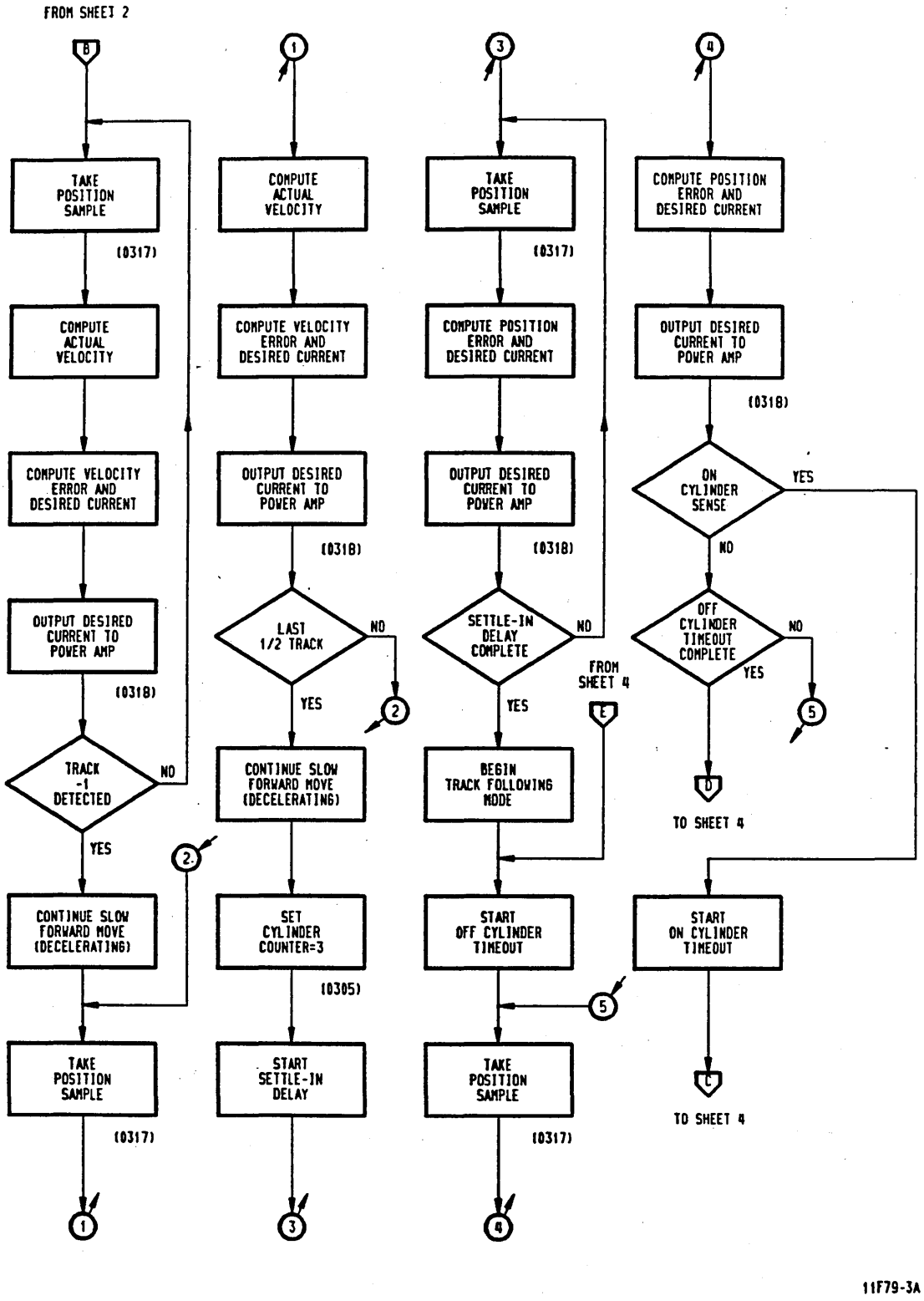


Figure 1-35. Load Operation Flowchart (Sheet 3)

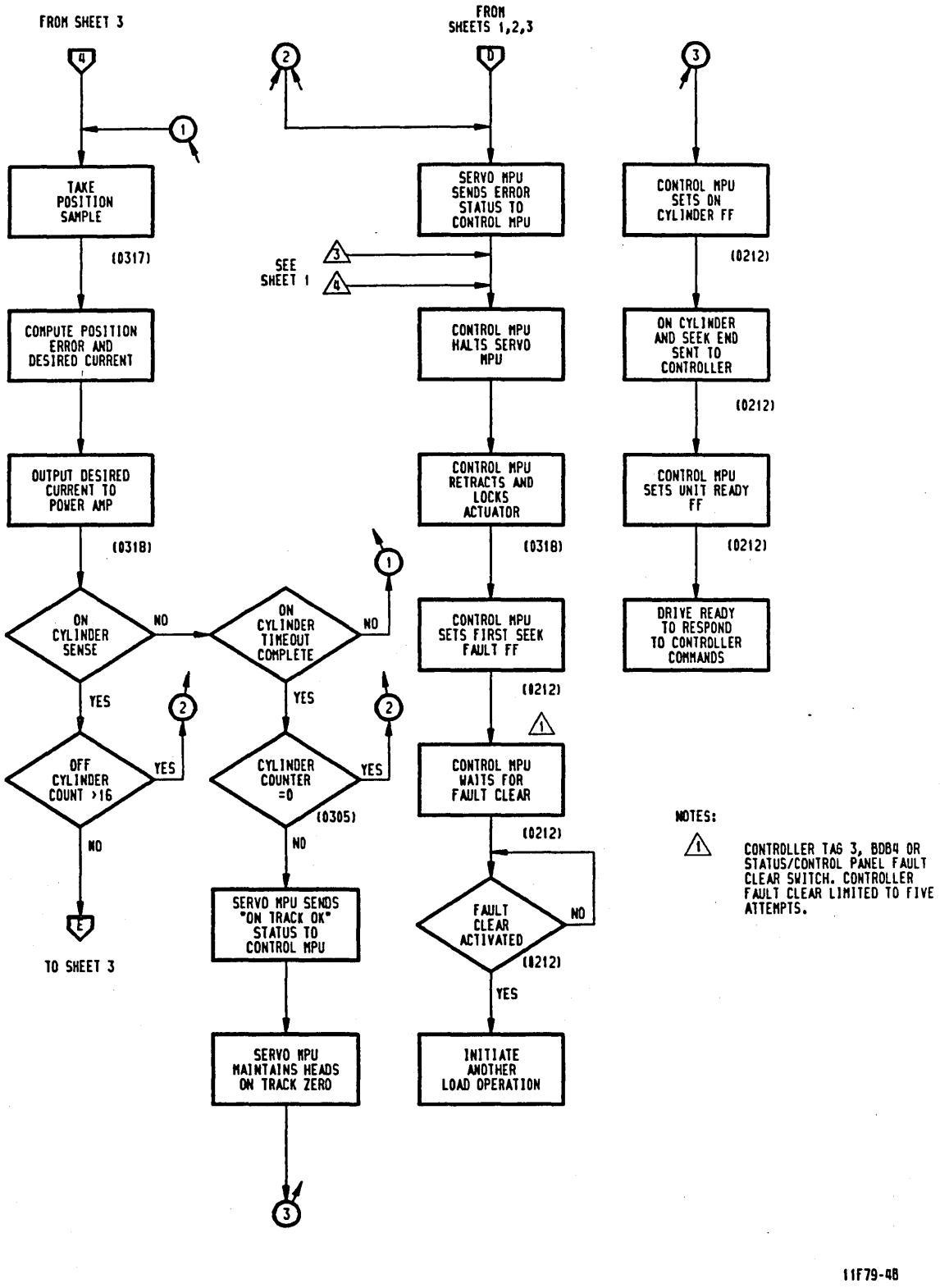


Figure 1-35. Load Operation Flowchart (Sheet 4)

With start conditions present (refer to Local/Remote Power Sequencing), the Control MPU starts the drive motor by activating the -Motor Run line to the Motor MPU. Thereafter, the Control MPU requests status from the Motor MPU at 30 millisecond intervals. When speed OK is sensed on the +Motor Sense 0-2 status lines, the Control MPU enables the power amplifier, unlocks the actuator, and sends a load command to the Servo MPU. Operation of the Motor MPU and drive motor is discussed under Electromechanical Functions.

Prior to moving the heads, the Servo MPU checks to ensure that the -Demodulator Active line is high following a successful retract. Assuming a successful retract, the Servo MPU outputs a value on the Servo Data Bus that causes the desired current generator to output a pulse that forces the actuator to move forward from the landing zone. Figure 1-36 shows the carriage trajectory during the load seek. Once the -Demodulator Active signal goes low, indicating that the Tribit Decoder has locked onto the servo signal, the Servo MPU stops placing values on the Servo Data Bus allowing the actuator to coast, and also begins counting cylinder pulses.

After counting 100 cylinder pulses, the Servo MPU develops a desired current pulse that slows the actuator down. The Servo MPU then reports "Load OK" status to the Control MPU. Throughout the forward move, the Control MPU checks to ensure that the move is completed within 500 milliseconds.

If the forward move was completed within the allotted time, the Control MPU issues an RTZ command to the Servo MPU. The Servo MPU then waits for the actuator velocity to drop to 2 inches per second. When this occurs, the Servo MPU initiates a slow reverse move. After detecting the Outer Guard Band, the Servo MPU reduces the desired current and continues the reverse move for two cylinder counts. Following this, the Servo MPU resets the cylinder counter to 2 and begins a slow forward move. It then checks to ensure that the Outer Guard Band signal goes inactive before the cylinder counter decrements to zero.

Starting with T less than 1, the Servo MPU begins to integrate actual velocity to determine when 1/2 track remains in the seek. When 1/2 track is detected, the Servo MPU sets the cylinder counter to 3, and initiates a settle-in delay. In settle-in mode, the Servo MPU shifts from velocity control to position control. The Servo MPU examines the position signal, computes a position error, and then uses this error value to generate desired current.

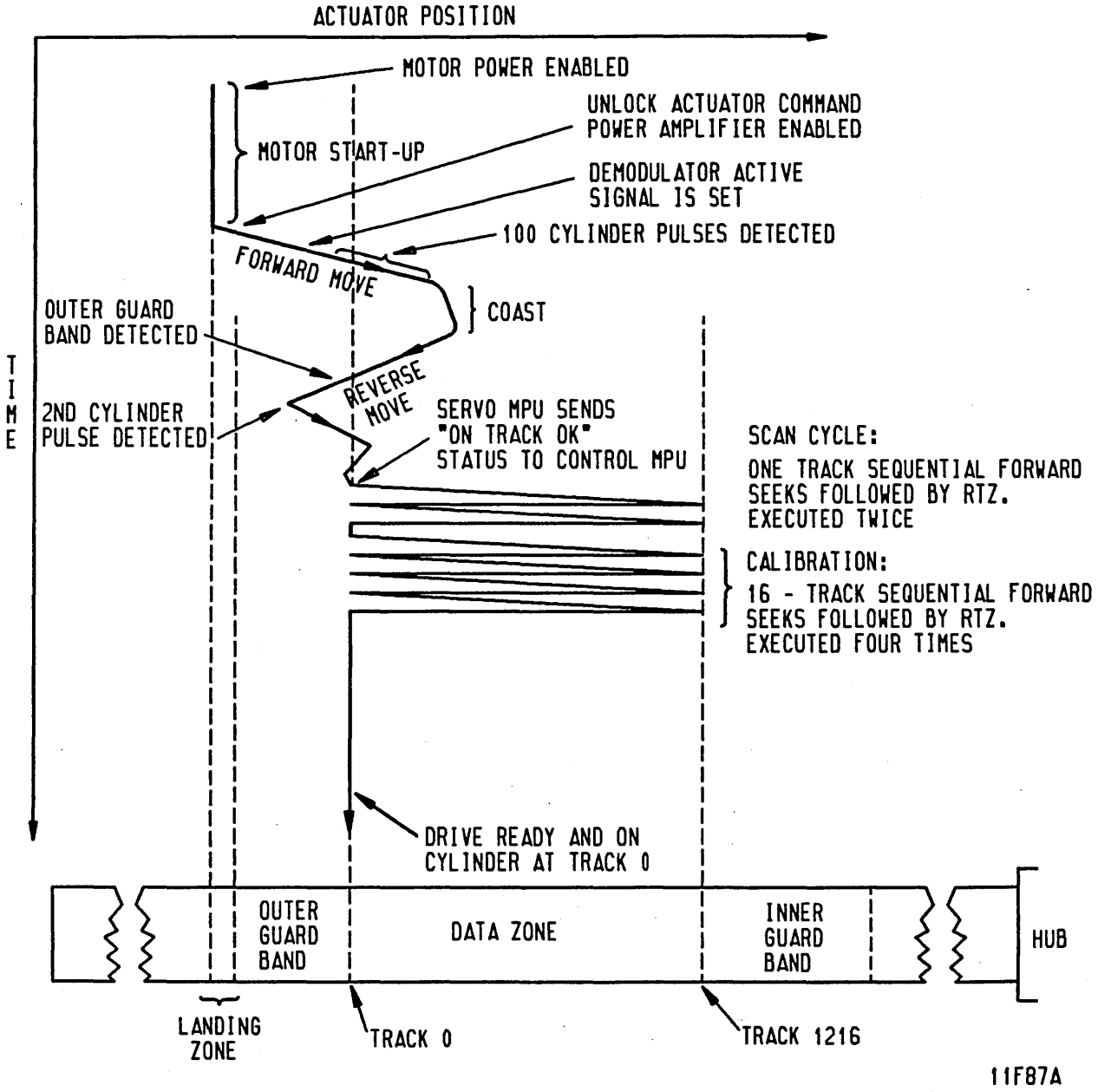


Figure 1-36. Load Seek Trajectory

After the settle in delay times out, the Servo MPU enters the track-following mode. When operating in the Track Following mode the Servo MPU adds a low frequency gain boost to the positioning loop. During this time the Servo MPU starts two successive timeouts to ensure that the actuator reaches on cylinder and remains on cylinder. Failure to achieve on cylinder during the first timeout, or drifting off cylinder more than 16 times during the second timeout, or detecting three or more cylinder pulses after the expiration of these timeouts causes the Servo MPU to record error status.

At the completion of the RTZ portion of the load operation, the Servo MPU sends "On Track OK" status to the Control MPU. Throughout the RTZ, the Control MPU checks to ensure that the move is completed within 500 milliseconds.

After completing the load operation, the Control MPU commands the Servo MPU to perform a scan cycle, and a calibration routine.

The scan cycle consists of forward one-track sequential seeks starting at track 0 and ending at track 1216, followed by a return-to-zero (RTZ) seek. This sequence is executed twice.

The calibrate routine consists of forward 16-track sequential seeks starting at track 0 and ending at track 1216, followed by a RTZ seek. This sequence is executed four times. During these seeks, the Servo MPU examines the amount of overshoot on the Position signal. The data obtained is used to compensate for drive variations requiring a change in the actuator force constant. The actuator force constant determines the level of Desired Current sent to the power amplifier. Calibrating this constant ensures that the force applied by the servo system to the actuator meets the requirements of the closed loop system. During the low velocity RTZ portions of the calibrate operation, the Servo MPU computes a constant used to calibrate the velocity measurement (low velocity mode).

If the load and RTZ portions of the operation were successful and did not take too long, and the scan/calibrate completed properly, the Control MPU sets the On Cylinder FF and Unit Ready FF and also sends Seek End to the Controller. With these FF's set, On Cylinder and Unit Ready status are available on Bus In.

If either the load or RTZ seeks were unsuccessful or took too long, or the scan/recalibrate did not complete properly after two attempts, the Control MPU attempts to retract and lock the actuator. It then sets the First Seek Fault FF. A fault can be cleared by operation of the Fault Clear switch on the optional status/control panel, or by a Fault Clear command (Tag 3, BOB4) from the controller. Pressing the Fault Clear switch or executing a Fault Clear command (limited to 5 attempts) initiates another load attempt.

After sending "On Track OK" status to the Control MPU, the Servo MPU remains active. The Servo MPU continually makes corrections to the actuator position to keep the heads on track zero. If the Servo MPU fails to maintain the heads on cylinder, it sends error status to the Control MPU. For more details refer to the description under Track Following.

Normal Seek

Normal seeks are initiated by controller command and implemented by the drive servo circuitry. The normal seek is the operation used to move the heads from one location to another on the disk surface. The same track can also be selected, but a zero track seek requires no actuator movement and the operation is handled by the SMD-E Gate Array.

The normal seek occurs in two directions, reverse (from the center towards the outer edge) and forward (from the outer edge towards the center). Going from a higher-numbered track to a lower-numbered one involves an out direction movement of the actuator, while going from a lower-numbered track to a higher numbered one involves an in direction movement. Figure 1-37 is a detailed flowchart showing the normal seek operation.

On seeks of 12 tracks or more in length, the Servo MPU examines the amount of overshoot at the end of the seek and uses this data to re-adjust the actuator force constant (see Load Operation).

With the drive in the unit ready and on cylinder conditions, the controller initiates a normal seek by transmitting a cylinder select command (refer to description of Tags 1 and 2 under I/O Signal Processing). The cylinder address is gated into the Cylinder Address register (in the SMD-E Gate Array) by the Cylinder Select Tag.

If a new seek command leaves the Cylinder Address register contents unchanged (a zero-track seek), the On Cylinder line and Seek End line to the controller are disabled for 30 microseconds and no I/O Interrupt is enabled to the Control MPU. If a new seek command requires a seek to a different seek address, however, the Cylinder Select tag clears the On Cylinder FF and generates an I/O Interrupt to the Control MPU. The Control MPU responds to this interrupt by examining the state of the registers and latches in the SMD-E Gate Array, and then directing the Servo MPU to initiate a seek operation. The Control MPU transfers the destination cylinder address from the SMD-E Gate Array to the Servo MPU via the Peripheral Array.

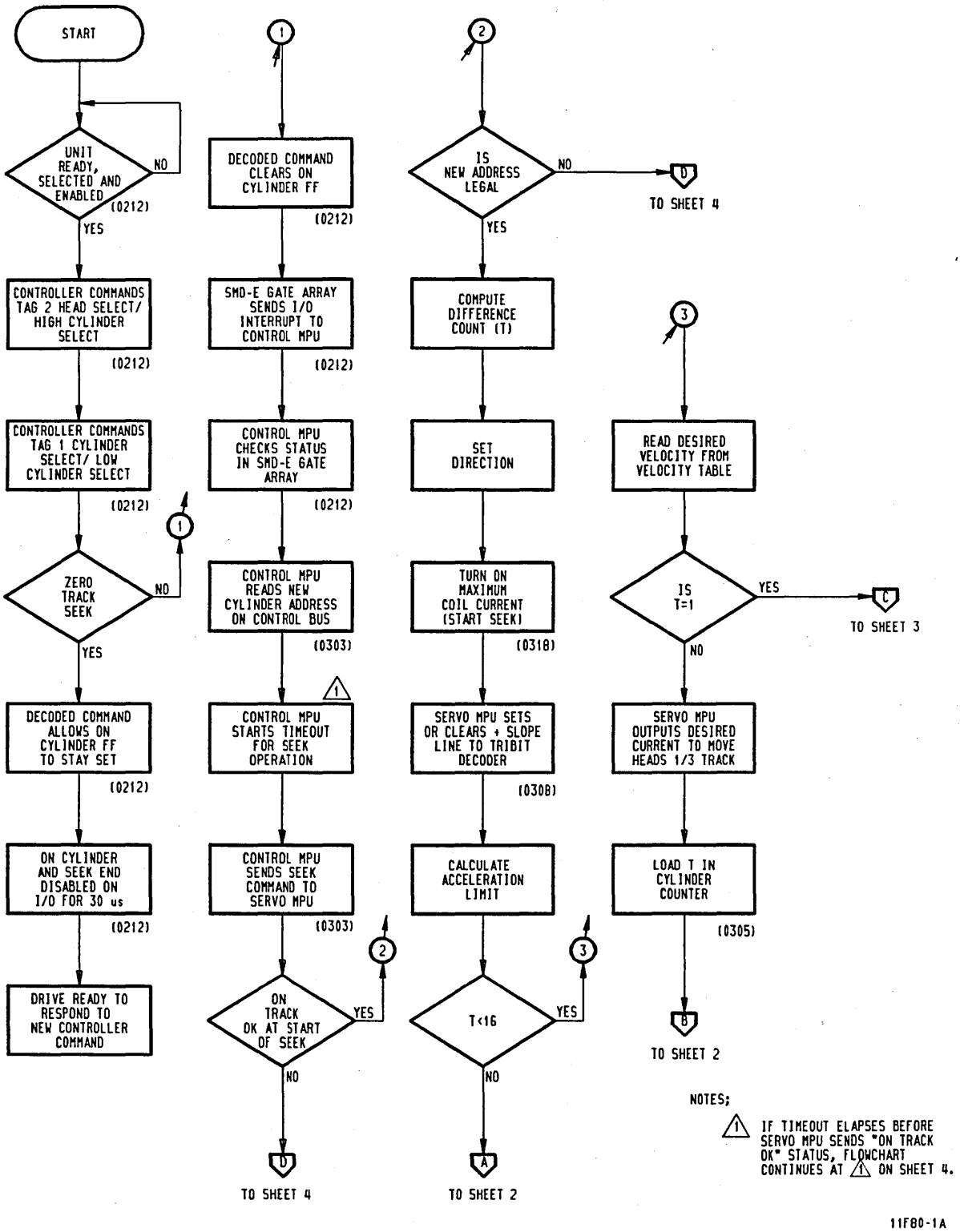


Figure 1-37. Normal Seek Flowchart (Sheet 1 of 4)

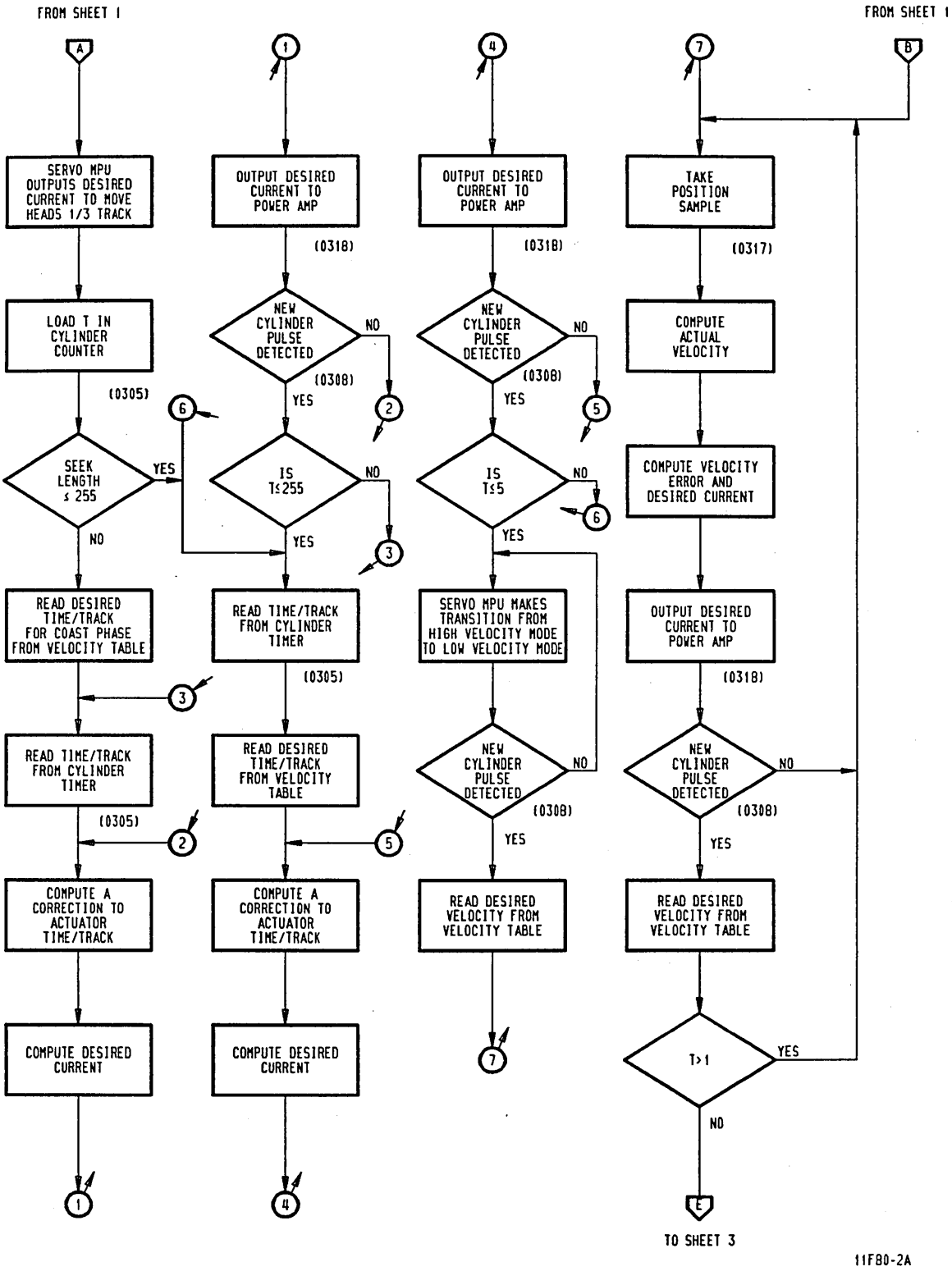


Figure 1-37. Normal Seek Flowchart (Sheet 2)

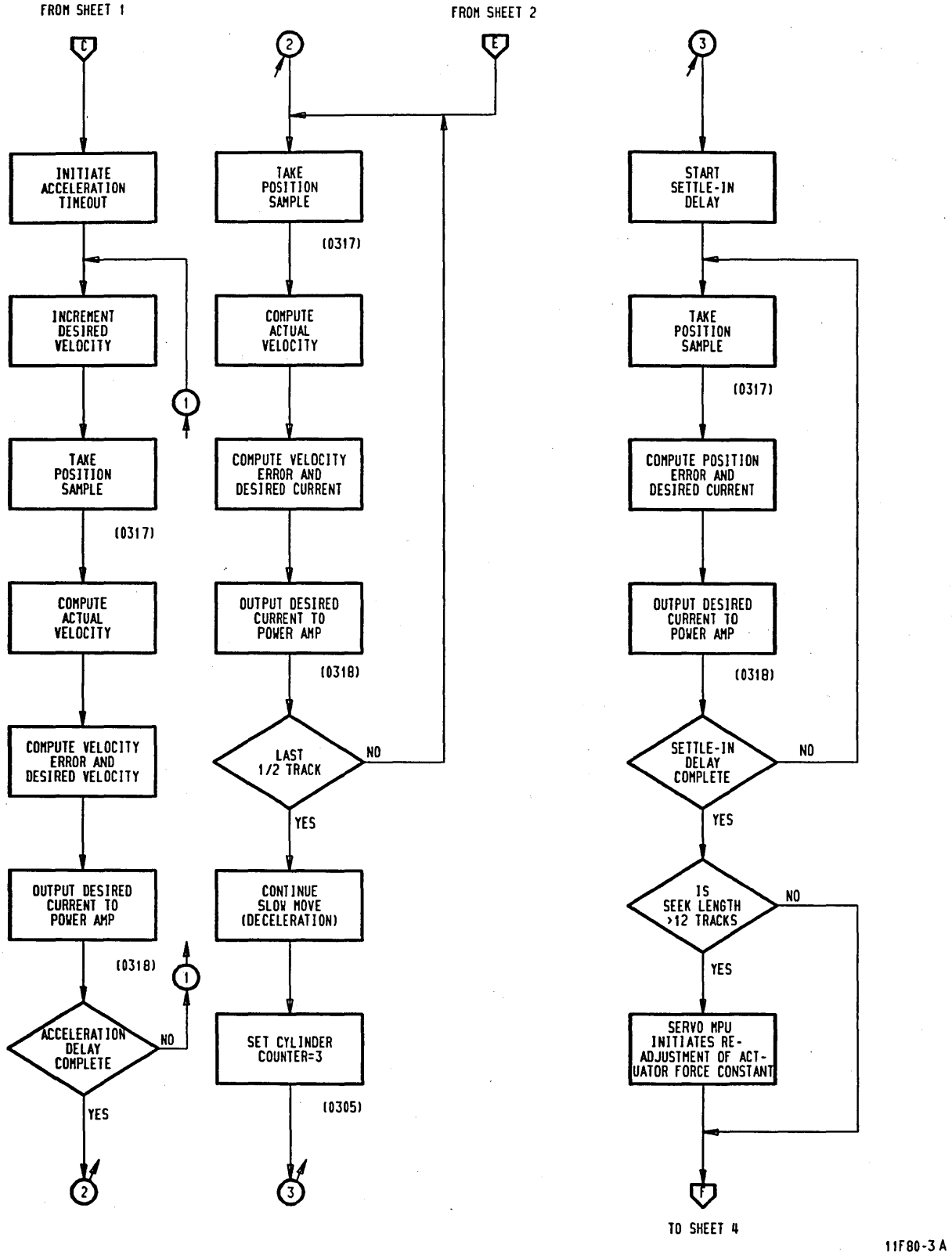


Figure 1-37. Normal Seek Flowchart (Sheet 3)

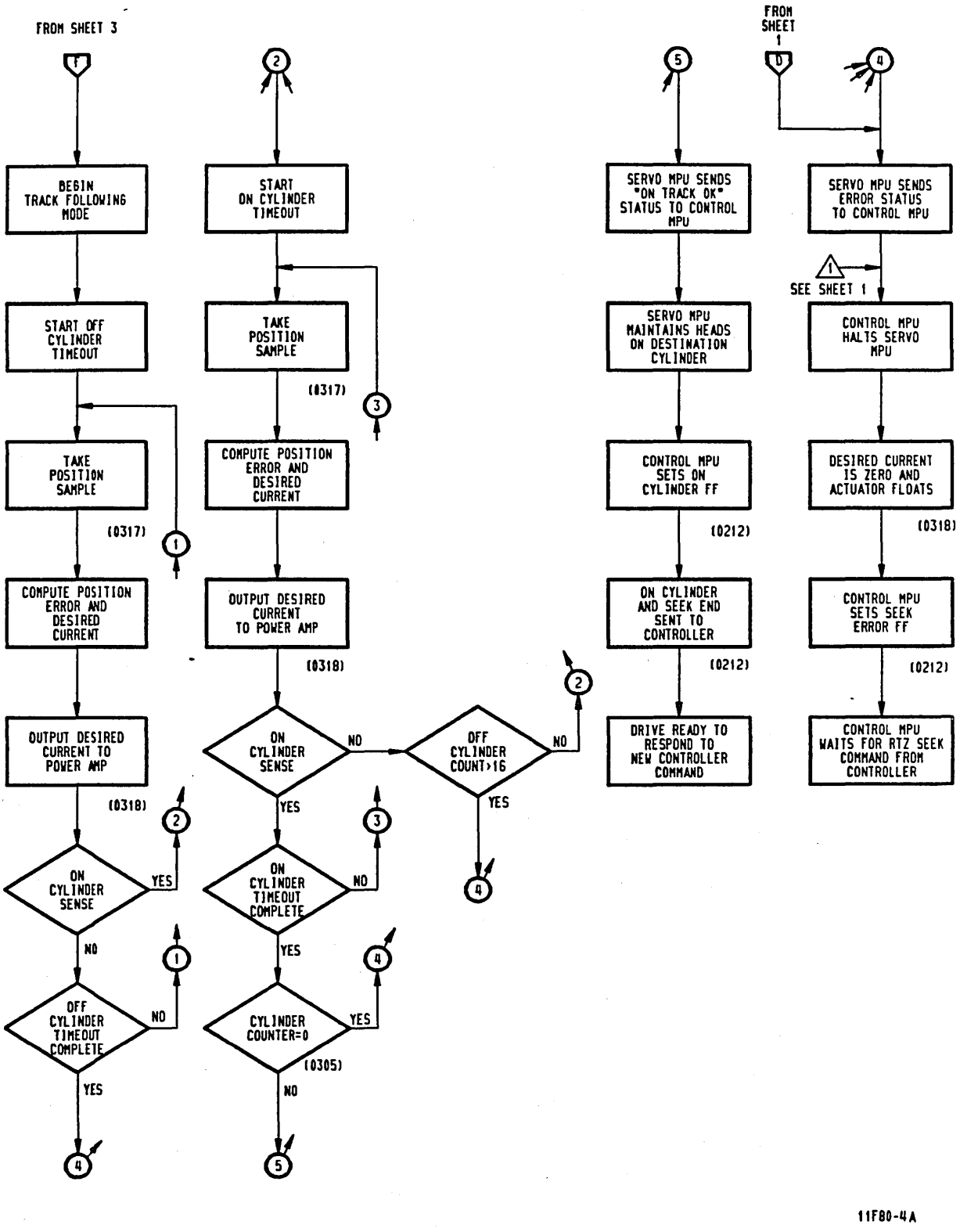


Figure 1-37. Normal Seek Flowchart (Sheet 4)

Prior to starting a seek operation and at 30 millisecond intervals thereafter, the Control MPU checks the Motor Status 0-2 lines to make sure that no motor fault condition exists and the motor is up to speed. At the start of the seek, the Control MPU loads a timer (so that a Seek Error will be indicated if the seek is not completed at the end of the timeout).

The seek operation from this point until the on cylinder condition is achieved is under the control of the Servo MPU. Initially, the Servo MPU checks to ensure that the actuator is on cylinder at the start of the seek, and the address provided by the controller is legal. After performing these checks, the program compares the new address with the present address (stored in ROM memory) to calculate the difference between the two (T=tracks to go), and the direction of the move (in or out). The difference count is then transmitted to the cylinder pulse counter in the Peripheral Array.

The Servo MPU sets or clears the +Slope line to the tribit decoder circuit to ensure that the decoded position signal has the proper phase at the destination track.

The remainder of the seek is conditioned by its length. For one-track seeks, the Servo MPU builds an accelerating velocity ramp after starting a timeout. At the completion of the timeout, there is a controlled deceleration until the seek has one-half track remaining (initiate settle-in mode). From this point on, a one track seek is completed in the same manner as longer seeks.

During the acceleration phase of longer length seeks, the Servo MPU adjusts the acceleration limit to correspond to the length of the seek. If the seek length is greater than 255 tracks, the actuator is allowed to coast at the maximum acceleration limit until tracks to go becomes less than 255.

When tracks to go becomes less than 255, or the acceleration limit is reached on shorter seeks, the Servo MPU generates a decelerating velocity profile. Throughout the deceleration portion of the coarse seek, the Servo MPU updates the D/A count at each cylinder crossing. When T=5, the Servo MPU activates the Position Sampling circuit.

The Servo MPU uses two methods to determine actual velocity during a normal seek. When tracks-to-go (T) is greater than 5, the Servo MPU determines actual velocity by measuring the elapsed time between cylinder pulses. When T is equal to or less than 5, the Servo MPU differentiates the linear portion of the Position signal to determine actual velocity. Until T is less than 1/2 track, the Servo MPU compares the values obtained for actual velocity to tabulated values of desired velocity stored in memory. The error value produced by each comparison is used to generated a level of desired current for the power amplifier.

Starting with T less than 1, the Servo MPU begins to integrate actual velocity to determine when 1/2 track remains in the seek. When 1/2 track is detected, the Servo MPU sets the cylinder counter to 3, and initiates a settle-in delay. In settle-in mode, the Servo MPU shifts from velocity control to position control. The Servo MPU examines the position signal, computes a position error, and then uses this error value to generate desired current.

After the settle in delay times out, the Servo MPU enters the track-following mode. When operating in the Track Following mode the Servo MPU adds a low frequency gain boost to the positioning loop. During this time the Servo MPU starts two timeouts in succession to ensure that the actuator reaches on cylinder and remains on cylinder. Failure to achieve on cylinder during the first timeout, or drifting off cylinder more than 16 times during the second timeout, or detecting three or more cylinder pulses after the expiration of these timeouts causes the Servo MPU to record error status.

At the end of the seek operation, the Servo MPU sends status to the Control MPU. If the seek operation was successful, did not take more than 60 milliseconds, and did not request an illegal address, the Control MPU sets the On Cylinder FF in the SMD-E Gate Array. With this FF set, On Cylinder status is available on Bus In and the Seek End line is active. If the seek operation was unsuccessful or took too long, or the controller requested an illegal address, the Control MPU sets the Seek Error FF in the SMD-E Gate Array. With this FF set, Seek Error status is available on Bus In and the Seek End line is active. As a maintenance aid, the Control MPU displays a status code on the status/control panel. These codes, discussed in section 3, indicate where the seek operation failed.

After providing Seek End status, the Control MPU waits for further commands from the controller.

After sending "On Track OK" status to the Control MPU, the Servo MPU remains active. The Servo MPU continually makes corrections to the actuator position to keep the heads on the destination track. If the Servo MPU fails to maintain the heads on cylinder, it sends error status to the Control MPU. For more details refer to the description under Track Following.

Return to Zero Seek

The Return to Zero (RTZ) seek is the operation that moves the heads from any location on the disk to track 0. Although the MPU uses an RTZ seek as part of the load operation, the controller can command RTZ seeks also. Both types of RTZ seeks are identical, except for the status presented if they fail.

If the RTZ seek in a load operation is unsuccessful, or took more than 1 second to complete, the Control MPU sets the First Seek Fault FF, and a re-attempt occurs if the Fault Clear switch is pressed (units with status/control panel), or the controller activates Tag 3 with Bus Out bit 4 active (Controller Fault Clear).

If a controller-initiated RTZ seek is unsuccessful, or took more than 1 second to complete, the Control MPU sets the Seek Error FF, clears the On Cylinder FF (Seek End active on the I/O), and disables the power amplifier. In this case, the drive waits for another RTZ command from the controller.

This discussion pertains specifically to the controller-initiated RTZ seek. This seek is flow-charted in figure 1-38. Refer to the Load Operation discussion for details about the RTZ portion of the load operation.

The controller initiates an RTZ operation by outputting Tag 3 (Control Select) along with Bus Out bit 6. The RTZ Seek command clears the Cylinder and Head Address registers, the On Cylinder FF, and Seek Error FF. Note: All of these components except the Head Address register are located inside the SMD-E Gate Array.

The decoded command also sends an I/O interrupt to the Control MPU. The Control MPU responds to this interrupt by examining the state of the registers and latches in the SMD-E Gate Array, and then directing the Servo MPU to initiate a RTZ operation. Prior to starting an RTZ operation and at 30 millisecond intervals thereafter, the Control MPU checks the Motor Status 0-2 lines to make sure that no motor fault condition exists and the motor is up to speed.

The Servo MPU reads the RTZ command and initiates the RTZ. If the -Demodulator Active signal is high, the Servo MPU moves the heads out into the data zone. If the -Demodulator Active signal is low at the start of an RTZ, the actuator is allowed to float freely over the data zone. The Servo MPU then waits for the actuator velocity to drop to 2 inches per second. When this occurs, the Servo MPU initiates a slow reverse move. After detecting the Outer Guard Band, the Servo MPU reduces the desired current and continues the reverse move for two cylinder counts. Following this, the Servo MPU resets the cylinder counter to 2 and begins a slow forward move. It then checks to ensure that the Outer Guard Band signal goes inactive before the cylinder counter decrements to zero.

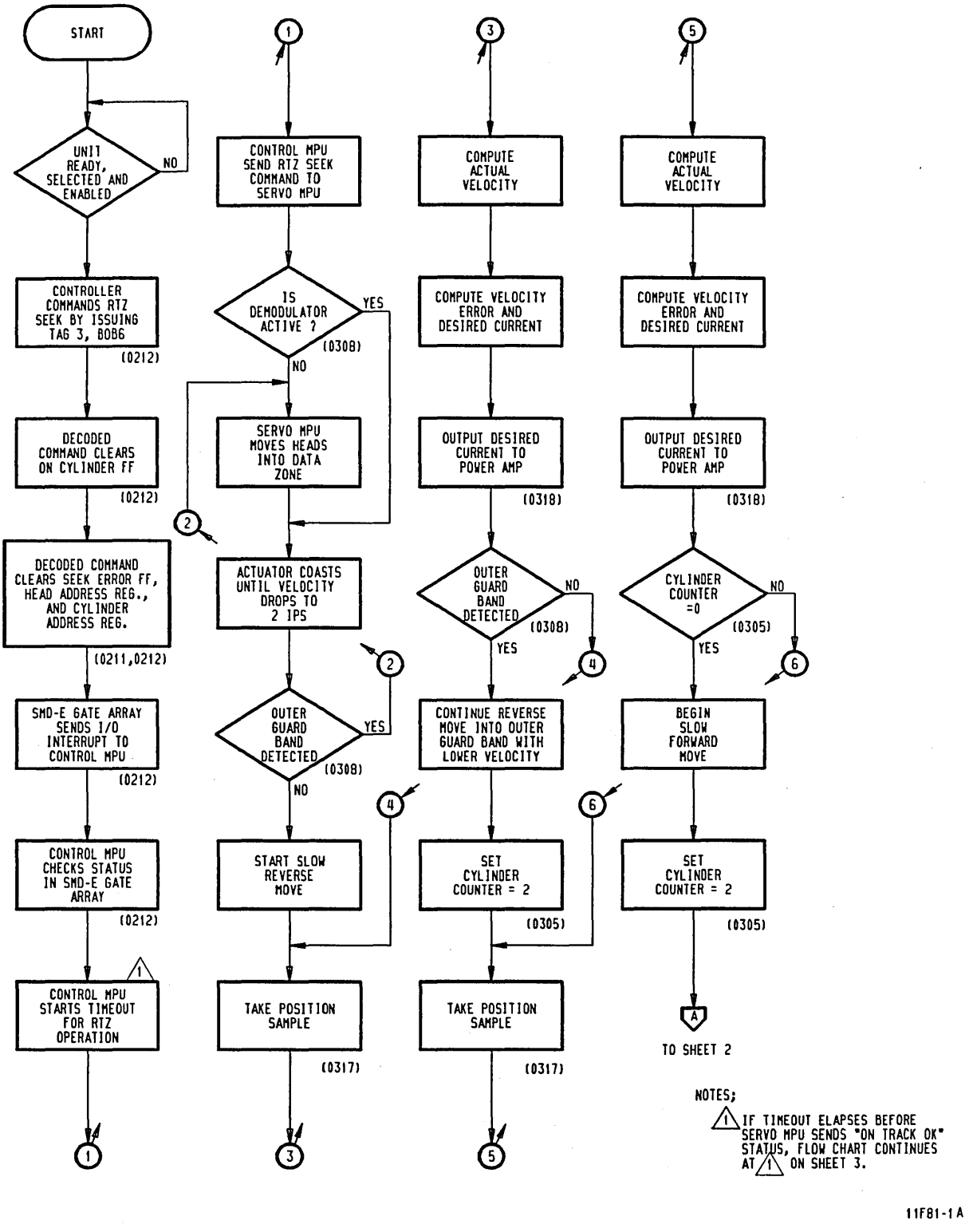


Figure 1-38. Return to Zero (RTZ) Seek (Sheet 1 of 3)

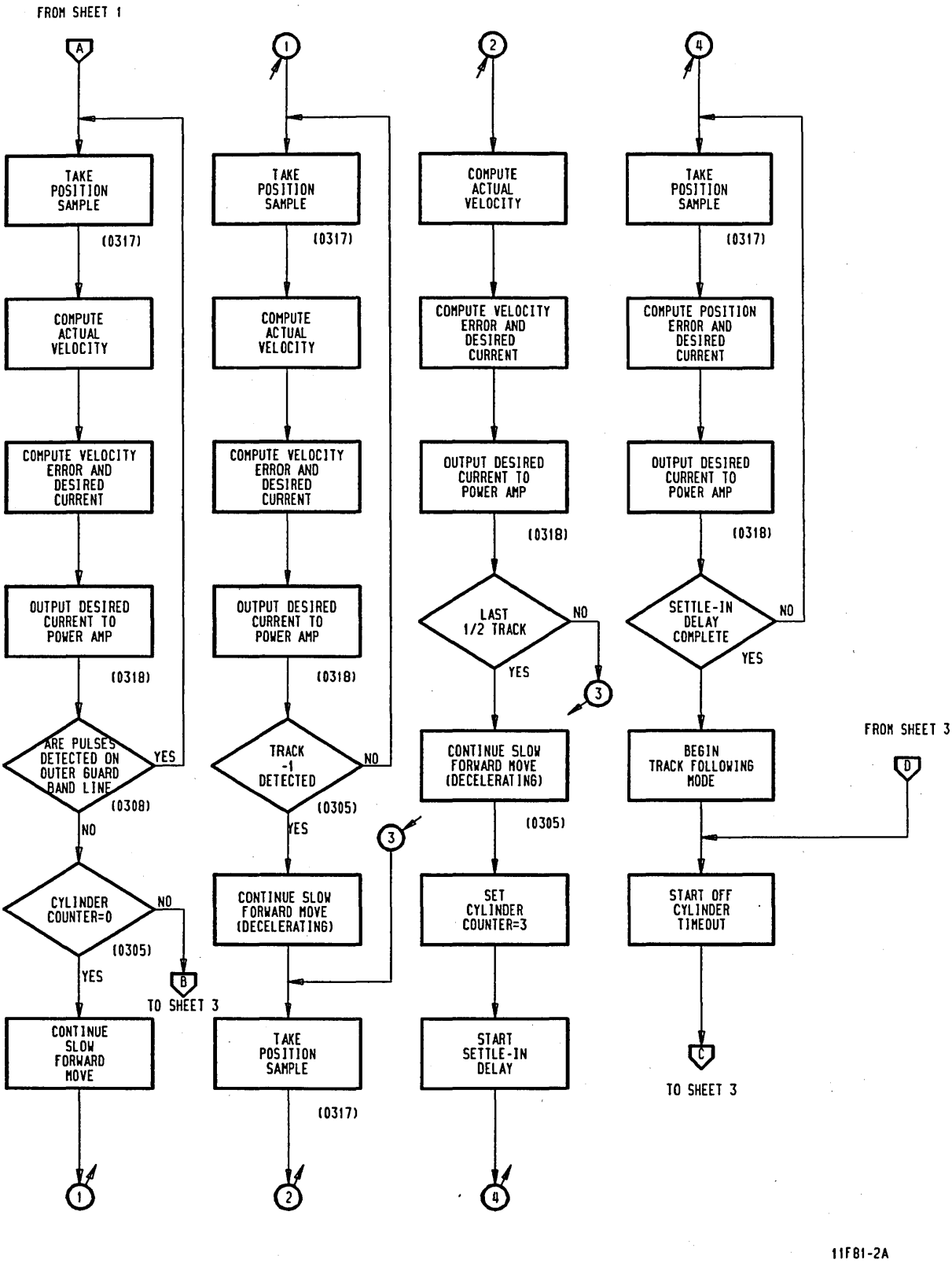


Figure 1-38. Return to Zero (RTZ) Seek (Sheet 2)

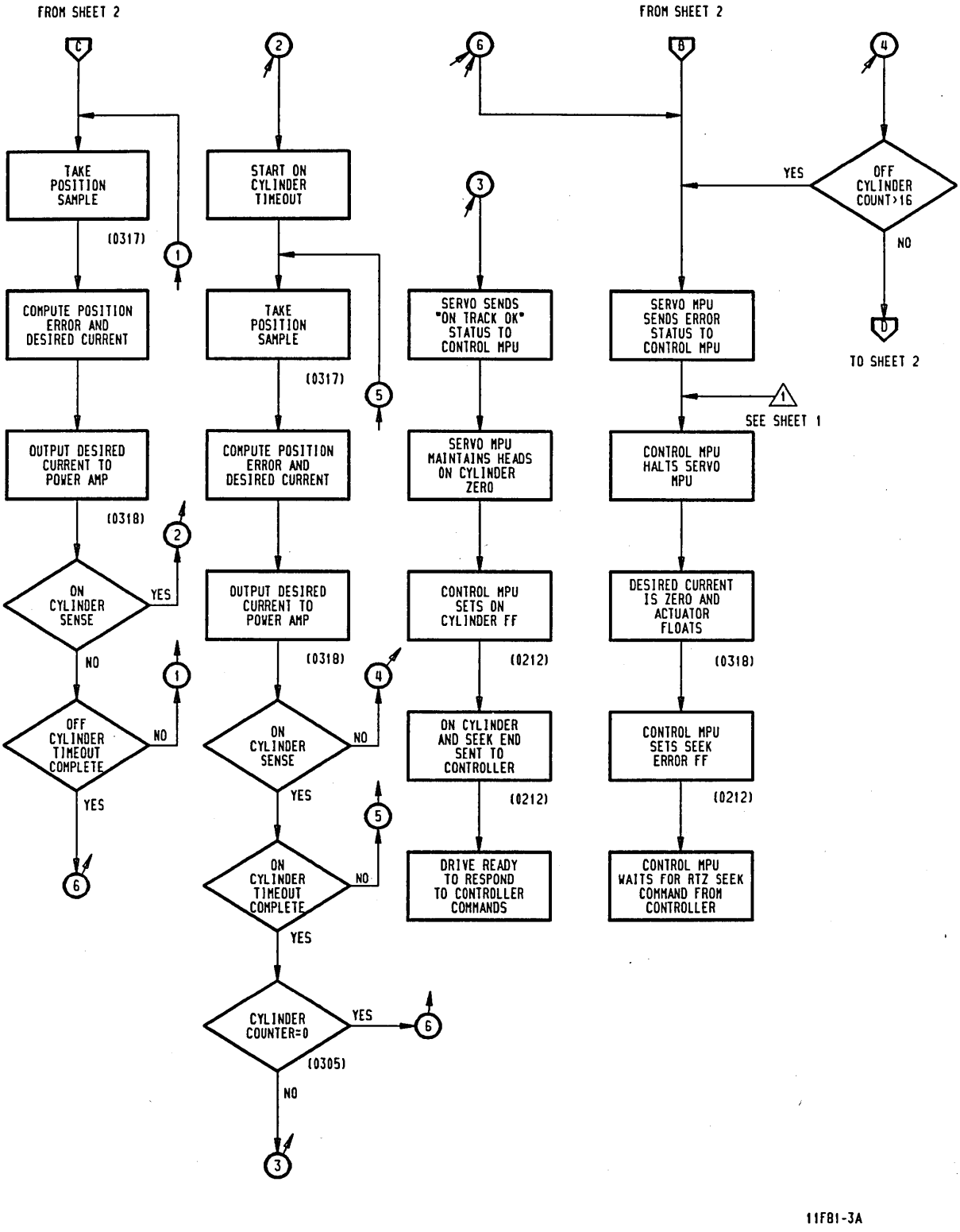


Figure 1-38. Return To Zero (RTZ) Seek (Sheet 3)

Starting with T less than 1, the Servo MPU begins to integrate actual velocity to determine when 1/2 track remains in the seek. When 1/2 track is detected, the Servo MPU sets the cylinder counter to 3, and initiates a settle-in delay. In settle-in mode, the Servo MPU shifts from velocity control to position control. The Servo MPU examines the position signal, computes a position error, and then uses this error value to generate desired current.

After the settle in delay times out, the Servo MPU enters the track-following mode. When operating in the Track Following mode the Servo MPU adds a low frequency gain boost to the positioning loop. During this time the Servo MPU starts two timeouts in succession to ensure that the actuator reaches on cylinder and remains on cylinder. Failure to achieve on cylinder during the first timeout, or drifting off cylinder more than 16 times during the second timeout, or detecting three or more cylinder pulses after the expiration of these timeouts causes the Servo MPU to record error status.

At the end of the RTZ operation, the Servo MPU sends status to the Control MPU. If the RTZ operation was successful and did not take more than 500 milliseconds to complete, the Control MPU sets the On Cylinder FF in the SMD-E Gate Array. With this FF set, On Cylinder status is available on Bus In and the Seek End line is active. If the RTZ operation was unsuccessful or took too long, the Control MPU sets the Seek Error FF in the SMD-E Gate Array and also disables the power amplifier. With this FF set, Seek Error status is available on Bus In and the Seek End line is active. As a maintenance aid, the Control MPU displays a status code on the status/control panel (if installed). These codes, discussed in section 3, indicate where the seek operation failed.

After providing Seek End status, the Control MPU waits for further commands from the controller.

After sending "On Track OK" status to the Control MPU, the Servo MPU remains active. The Servo MPU continually makes corrections to the actuator position to keep the heads on track zero. If the Servo MPU fails to maintain the heads on cylinder, it sends error status to the Control MPU. For more details refer to the description under Track Following.

Track Following

Following successful load, normal seek, or RTZ operations, the Servo MPU monitors on cylinder status and repositions the actuator if it drifts off cylinder. Throughout track following the Servo MPU periodically samples the position signal, computes a position error and desired current, and outputs desired current

to the power amplifier. If the position error exceeds a wide threshold defining on cylinder sense, the Servo MPU continues to maintain actuator control for a delay period to allow transient signal problems to be resolved. After this delay, the Servo MPU starts a shorter delay period in which on cylinder sense has a narrow threshold. If this threshold is not exceeded during the second delay, the Servo MPU continues actuator control with the wider threshold in effect. However, if the narrow threshold is exceeded, the Servo MPU reports error status to the Control MPU. The Control MPU then halts the Servo MPU (actuator floats), sets the Seek Error FF, clears the On Cylinder FF, and waits for an RTZ command from the controller.

Unload Operation

The Control MPU uses the unload operation during the power off sequence to move the heads completely outward until they are located over the landing zone. The Control MPU initiates the unload sequence when it detects a loss of start conditions or a loss of motor speed. A loss of start conditions occurs when the START switch is pressed (units configured with status/control panel), or (in remote operation) when the controller deactivates Sequence Hold.

Sensing a loss of start conditions or a loss of motor speed, the Control MPU clears the Unit Ready FF in the SMD-E Gate Array, and then issues a Retract command to the Servo MPU. The Servo MPU generates a desired current level to move the heads slowly outward into the landing zone. After a delay of 300 milliseconds, the Servo MPU checks for demodulator inactive. Following the delay, the Servo MPU sends status to the Control MPU.

If the demodulator is inactive, the Control MPU deenergizes the carriage latch electromagnet and halts the Servo MPU. Stopping the Servo MPU causes desired current to drop to zero. If the demodulator is still active after the first delay, the Control MPU attempts a retract operation by making the -Retract and +Power Amp Enable signals low. After a second delay, the Control MPU looks for demodulator inactive. When the demodulator goes inactive, the Control MPU deenergizes the carriage latch electromagnet, and makes the -Retract signal high to shut off retract current to the coil.

The Control MPU then drops the Motor Run line and continues to monitor the Motor Status 0-2 lines to determine when the motor has stopped rotating.

HEAD OPERATION AND SELECTION

GENERAL

Information is recorded on and read from the disk by the read/ write heads. The drive has one read/ write head for each data recording surface in the disk module: 10 recording surfaces and 10 read/ write heads as shown in figure 1-39. Before a read or write can be performed, the controller must command the drive to select the head located over the disk surface where the data is to be read or written. The following discusses how the heads read and write the data and also how the desired head is selected.

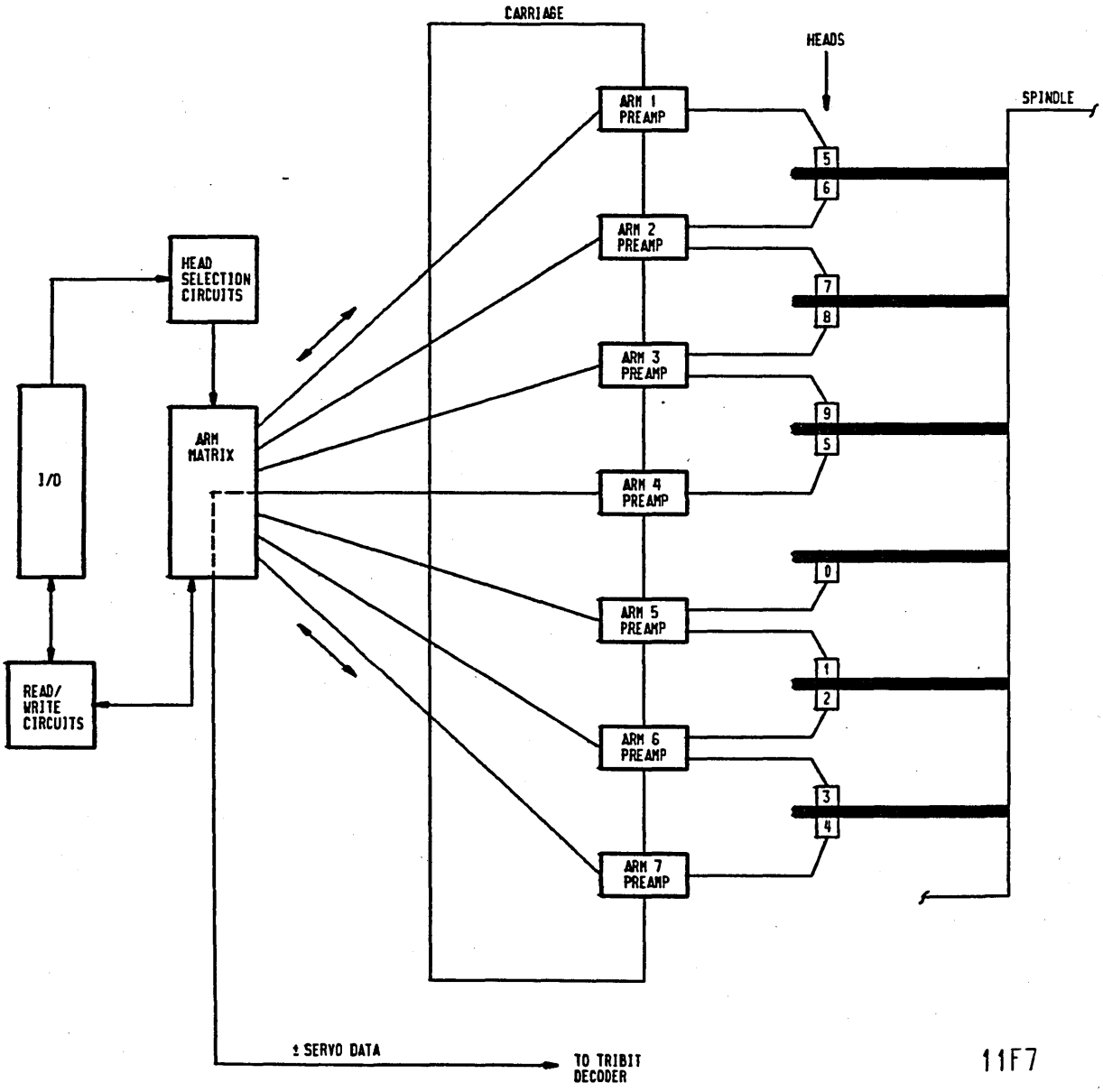


Figure 1-39. Read/Write Heads

HEAD FUNCTIONAL DESCRIPTION

Each read/write head has a coil wound on its core. This coil interfaces to the read/write circuitry via a preamplifier mounted on the head-arm. Selecting a head enables an arm preamplifier. The enabled arm preamplifier provides current switching for the head in write operations or amplification of voltage induced in the head in read operations. Refer to Read/ Write Functions for details about the arm preamplifier.

During write operations, the read/write head develops a changing flux pattern on the disk surface passing beneath it. The arm preamplifier supplies the selected head with a source of write current. At each transition of the write data signal, the preamplifier reverses the current in the head coil. This switching reverses the flux across the gap in the head (see figure 1-40). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a north pole and a south pole. The writing process orients the poles to store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of write current switching while its amplitude depends on the amount of current (the greater the current, the more oxide particles that are affected).

Information (data) is written by switching the current through the head. Switching this current reverses the direction of the flux field across the gap. The flux change defines a data bit. New data is written simply by writing over any data which may already be on the disk.

During a read operation, disk motion beneath the head causes the stored flux to induce a voltage in the heads (refer to figure 1-41). This voltage is analyzed by the Read circuit to define the data recorded on the disk. Each flux reversal (produced while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

HEAD SELECTION

A head must be selected before a read or write operation can be performed. Under Servo MPU control, the servo system moves the heads to the cylinder specified by the controller. By selecting a head, the controller specifies a particular track within that cylinder. Head selection starts when the controller sends the drive a Head Select (Tag 2) command and a head address. The head address is sent on Bus Out bits 0 through 3.

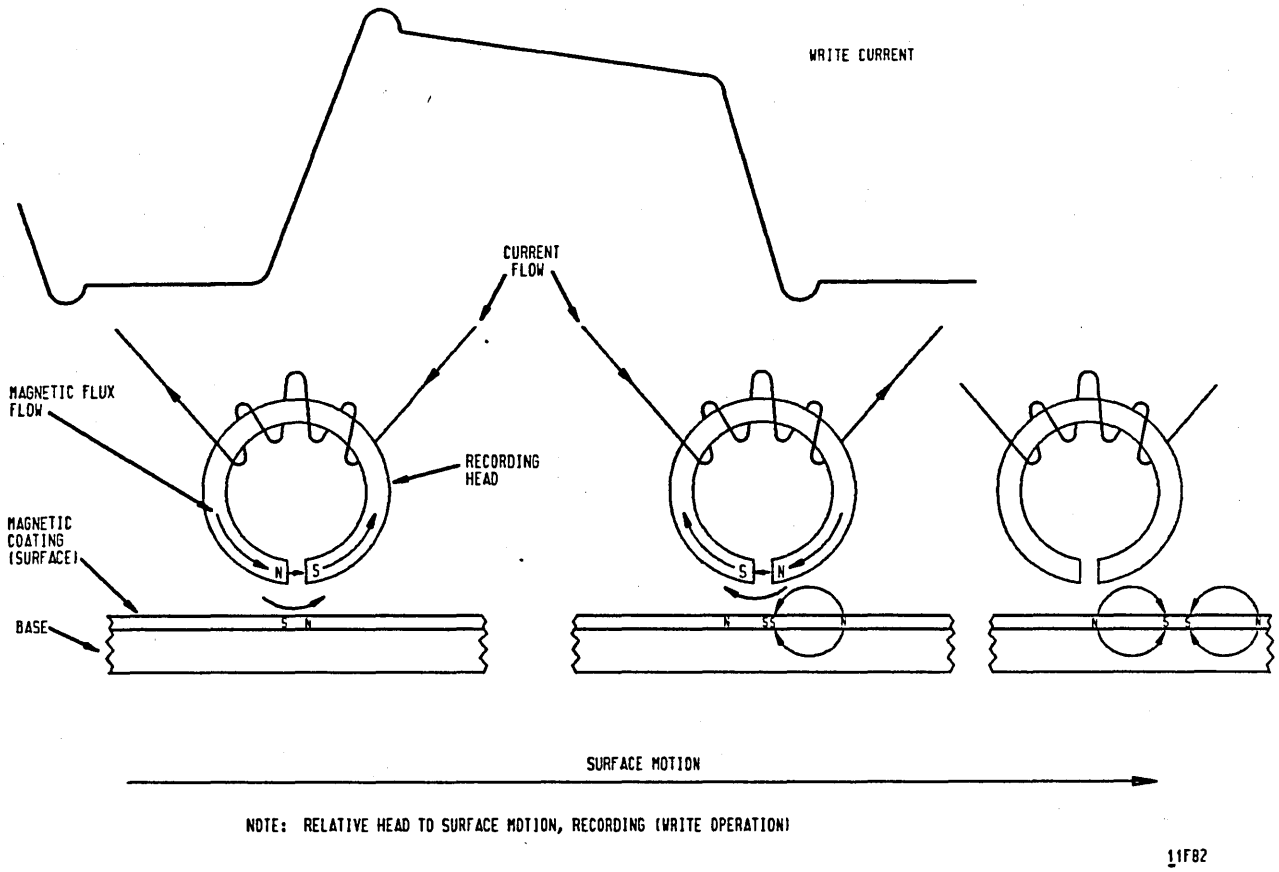


Figure 1-40. Writing Data

The Head Select tag gates the address into the Head Address register (HAR) located on the interface board. Figure 1-42 shows the head selection circuits.

The Head Address lines go from the I/O board to the Read/Write board via the control board. The read/write board contains a ROM, addressed by Head Address lines 0-3. Depending on its addressing, the ROM activates one of its output lines, -Arm Select 1-7, to enable one arm preamplifier. The enabled arm preamplifier in turn selects the head on its head-arm in response to the +Head Select 1 line. This line is activated by Head Address line 0. The Arm Select, Head Select, and common control lines for the preamplifiers are routed through the arm matrix board (inside the module) to the individual arm preamplifier.

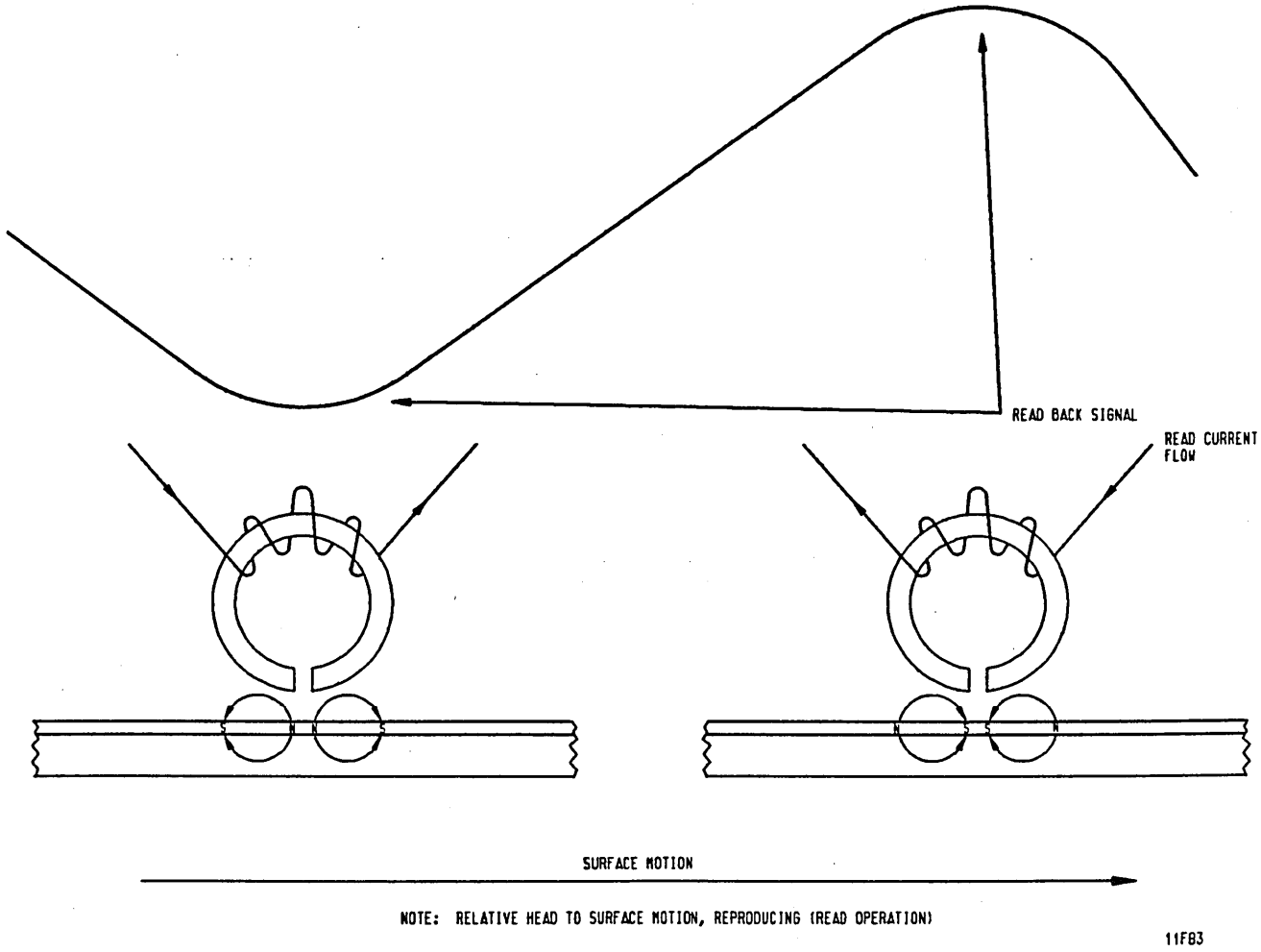


Figure 1-41. Reading Data

If an illegal head address (greater than 9) is received, no head is selected. A Write Fault occurs if the drive attempts to write data with no head selected. Table 1-5 shows the combination of address lines that selects each head.

READ/WRITE FUNCTIONS

GENERAL

When the drive is on cylinder and has a head selected, it is ready to perform a read or write operation. The controller initiates a read or write operation by sending a Control Select (Tag 3) along with the proper bus bit (Bus Out bit 0 for Write Gate and Bus Out bit 1 for Read Gate). During a write operation, the drive receives data from the controller and writes it on the disk. During a read operation, the drive recovers data from the disk and transfers it to the controller.

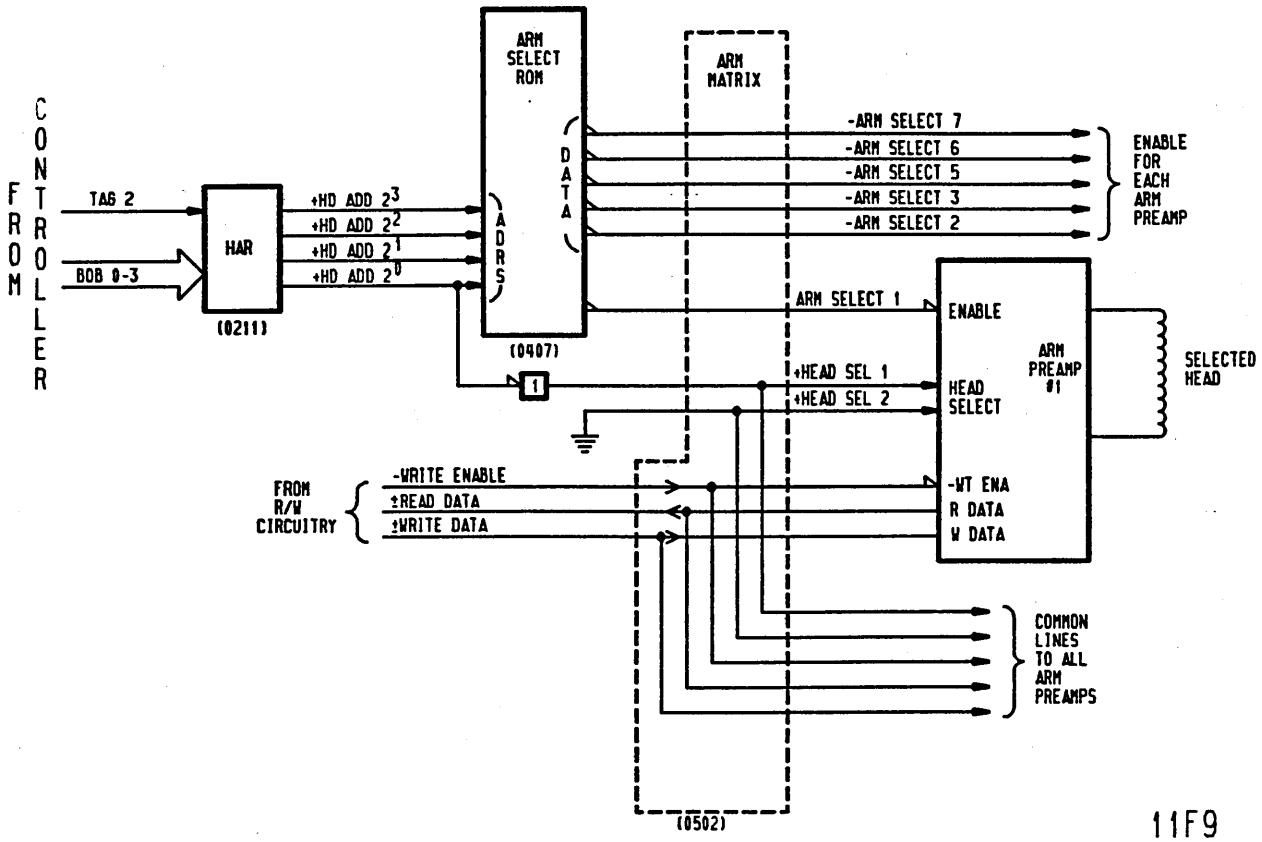


Figure 1-42. Head Selection Circuits

Figure 1-43 is a block diagram of the read/write circuits. The remainder of the discussion describes the read/write circuits and is divided into the following areas:

- Basic Read/Write Principles -- Explains the principles of recording and recovering data from a magnetic disk.
- Write Circuits -- Describes the circuits used by the drive to record data on the disk.
- Read Circuits -- Describes the circuits used by the drive to recover data from the disk.

TABLE 1-5. HEAD SELECT ADDRESSING

Head Selected	Arm Selected	+Head Address Lines			
		0	1	2	3
0	5	0	0	0	0
1	5	1	0	0	0
2	6	0	1	0	0
3	6	1	1	0	0
4	7	0	0	1	0
5	1	1	0	1	0
6	2	0	1	1	0
7	2	1	1	1	0
8	3	0	0	0	1
9	3	1	0	0	1

BASIC READ/WRITE PRINCIPLES

Principles Of 2-7 Recording

The drive employs two modulation schemes for read/write data transfers. The controller transfers data on the interface with Non Return to Zero (NRZ) modulation in a write or read operation. Transfers between the read/ write circuitry and the disk use 2-7 modulation. During a write operation, write circuitry decodes the incoming NRZ modulated data and converts it into 2-7 modulated data for storage on the disk surface. In a read operation, read circuitry in the drive decodes the 2-7 read data to create NRZ data which is suitable for the controller. The following paragraphs define both modulation schemes and the explain why 2-7 modulation is used in the drive.

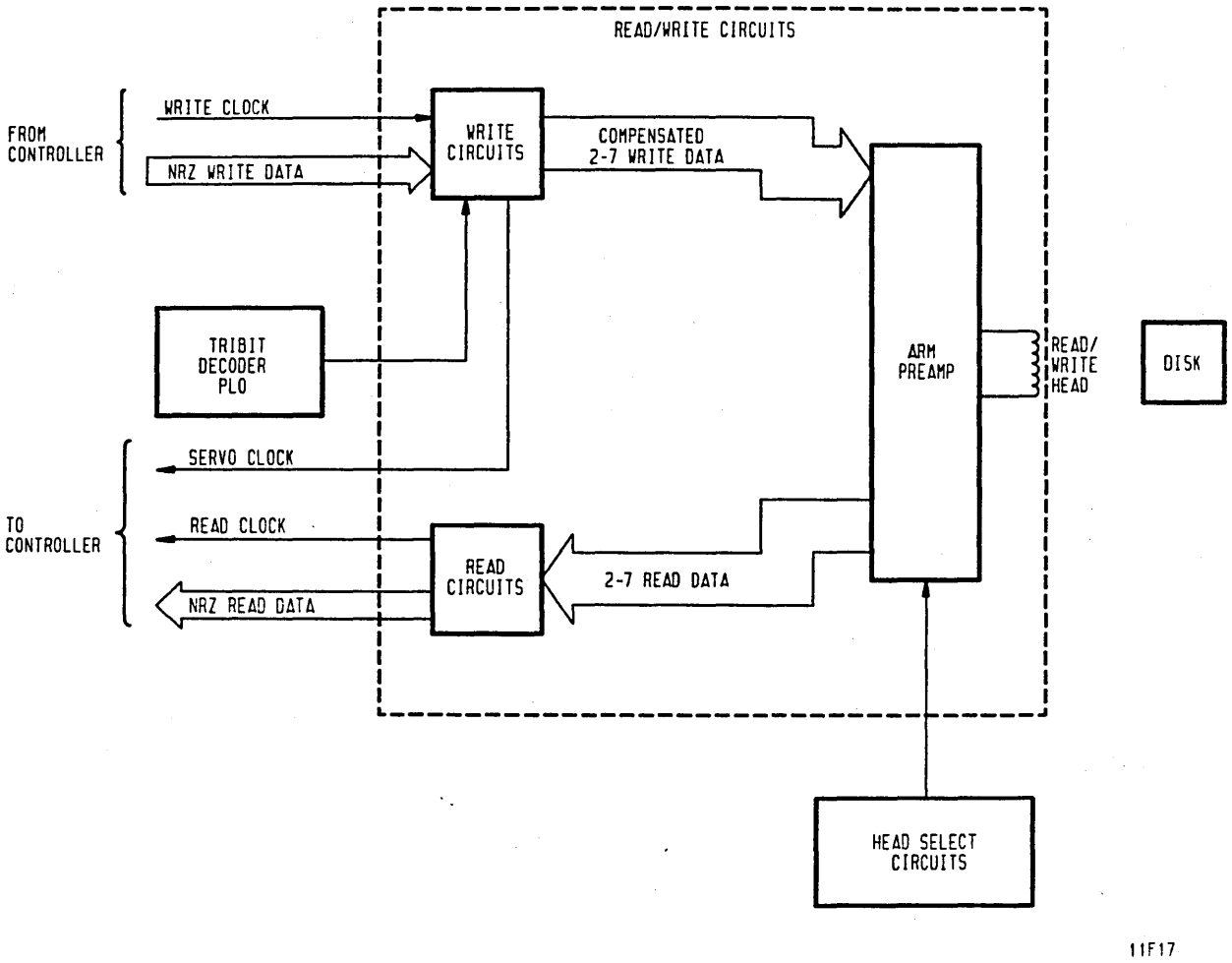


Figure 1-43. Read/Write Circuits

NRZ data is transferred at a nominal rate of 14.5 MHz. Each data bit is defined throughout an interval called a bit cell, and the nominal duration of each bit cell is 68.9 ns. For consecutive cells indicating binary 1, the read or write interface line is driven at the active level. For consecutive cells indicating binary 0, the read or write interface line is driven at the inactive level. Thus, NRZ data lines return to zero only when the transferred data changes from binary 1 to binary 0.

For disk transfers, the 2-7 scheme is superior to the NRZ scheme in two ways. First, it reduces the maximum rate of flux reversals on the disk; this permits greater recording density on the disk. Second, the recording bandwidth, or range from the minimum to maximum flux reversal rate, is limited; with narrowed bandwidth, the read/write circuitry has fewer noise problems.

The translation between NRZ modulation and 2-7 modulation is a translation of seven basic code words, as shown in table 1-6. Any string of NRZ data can be expressed as a series of these individual code words. The corresponding 2-7 data string is a series of translated code words where each 2-7 code word has replaced its corresponding NRZ word. So, the write circuitry encodes the NRZ data as 2-7 data, and the read circuitry decodes the 2-7 data as NRZ data.

Each 2-7 code word has twice as many bits as its related NRZ code word. Therefore, the 2-7 bit cell is half the NRZ bit cell or 34.45 ns, nominal. As the 2-7 data is written on the disk, the head changes its flux each time the code contains a binary 1. Although 2-7 uses twice the bit rate of NRZ, binary ones appear in 2-7 code less frequently than level changes occur in the corresponding NRZ code. Therefore, use of 2-7 code allows data to be written more densely on the disk.

The name 2-7 derives from the fact that preceding and following each occurrence of binary 1 in the code, there are at least two zeros and as many as seven zeros.

TABLE 1-6. TRANSLATION BETWEEN NRZ AND 2-7 CODES

NRZ Code Words	2-7 Code Words
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

Peak Shift

Peak shift is a predictable effect that would complicate decoding of the 2-7 read signal if it were not compensated in the write circuitry. The following paragraphs explain why peak shift occurs and how write compensation reduces the effect of peak shift.

Figure 1-44 shows selected write and read signals that are relevant to the description of peak shift. The write data line toggles each time a binary 1 appears in the 2-7 data string. Each toggle of write data reverses the magnetic flux in the data head to produce a region of changing recorded flux in the disk surface. The flux reversal on the disk has a finite length on the disk because of the shape of the flux pattern from the head gap and the inability of the head to reverse its magnetic flux instantaneously.

In read operations, the data head develops a composite readback voltage as it intercepts changing flux from the disk surface. Each flux reversal creates a readback voltage peak, as shown in figure 1-44. The composite readback voltage, developed by the head passing over a flux reversal, is a superposition of the peak caused by that flux reversal and by the leading and trailing edges of the peaks caused by the adjacent flux reversals. Any difference in the contributions of the two adjacent peaks will shift the central peak away from the closer adjacent peak.

Accurate decoding in read operations requires that the raw read data signal has timing intervals identical to those in the write data signal. Peak shift lengthens certain intervals and shortens other intervals in a manner that is predictable from the spacing of adjacent peaks. Write compensation anticipates this problem by advancing or delaying each write transition by an amount that depends on the number of binary 0s leading and trailing the binary 1 producing that transition. When the number leading exceeds the number trailing, write compensation delays the write transition. When the number trailing exceeds the number leading, write compensation advances the write transition. When the two numbers are equal, the transition occurs without compensation. Thus, compensated write data drives the heads, and the raw read data contains the same timing as the uncompensated write data.

The discussion of Write Compensation under Write Circuits includes tables that define the compensation shift for each possible data pattern.

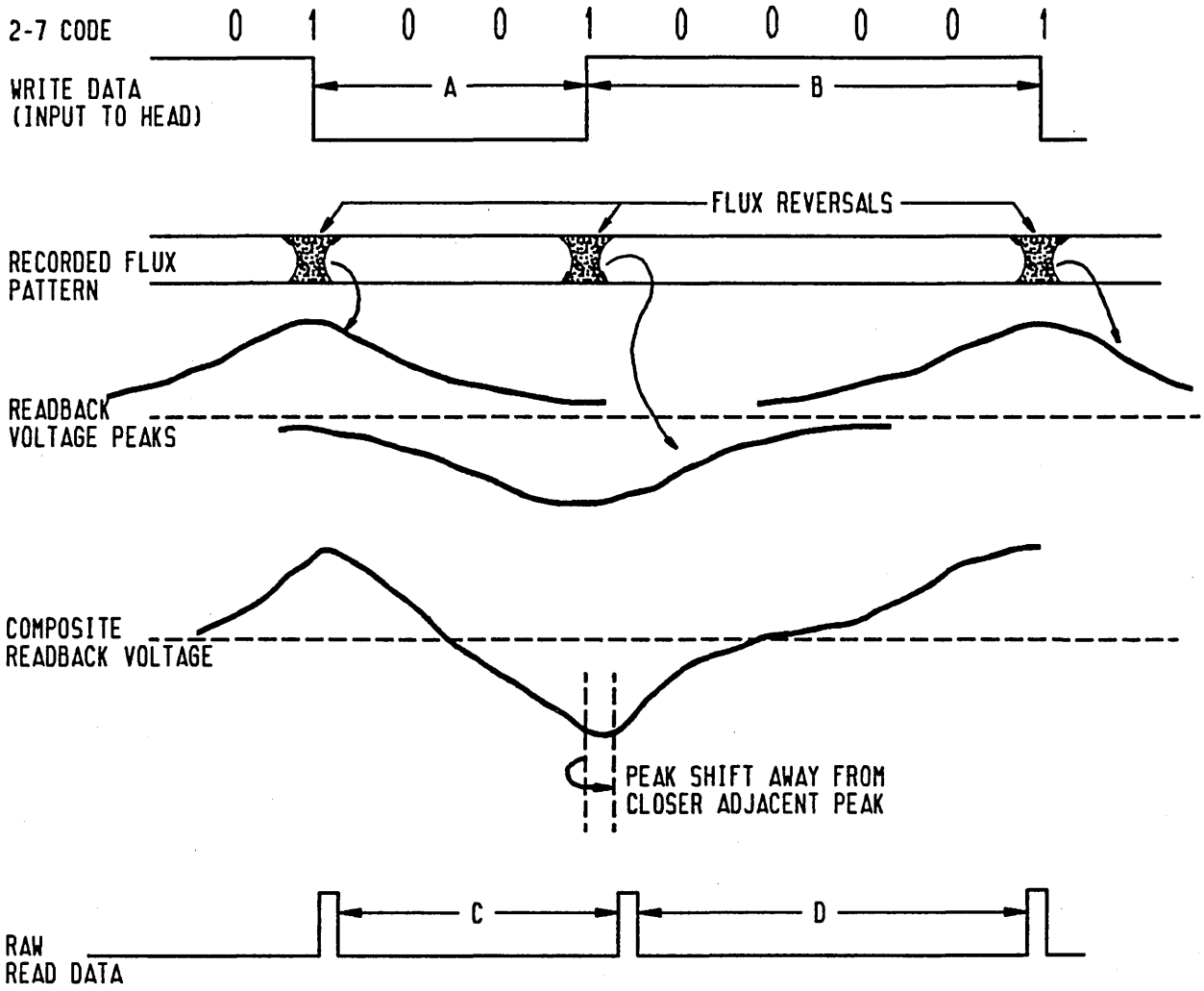


Figure 1-44. Peak Shift Waveforms

WRITE CIRCUITS

General

The write circuit operation is initiated by Tag 3 (Control Select) with Bus Out bit 0 true. This allows the drive to start processing serial NRZ data received from the controller. NRZ data is synchronized to the 14.5 MHz Servo Clock derived from the Write PLO. The Write Data is received via the Write Data line and is first sent to the 2-7 encoder circuit. This circuit converts the data to 2-7 modulation and sends it to the write compensation circuit. Write compensation modifies the data timing to compensate it for peak shift (refer to discussion on basic read/write principles for more information concerning peak shift). The compensated data is then processed by the write driver circuit. The write driver circuit provides the data signal that controls current switching in the selected arm preamplifier.

Figure 1-45 shows the write circuits and table 1-7 briefly explains their function.

Write PLO

The Write PLO circuitry uses a phase-locked loop to generate the 29.01 MHz (2F) Write Clock. As shown in figure 1-46, this circuitry consists of frequency dividers, a coincidence comparator, a charge pump, and a voltage-controlled oscillator (VCO). The frequency dividers and coincidence comparator are located in the Write Compensation and PLO ECL Logic Array.

The phase-locked loop uses the 2.41 MHz Clock from the Tribit Decoder PLO as a frequency reference (refer to the Servo Surface Decoding discussion). The Write VCO operates under loop control to generate the 29.01 MHz (2F) Write Clock, at twelve times the frequency of the reference clock. Two divisions by two and one division by three of the VCO output develop a 2.41 MHz feedback signal that can be compared to the reference clock to adjust the loop operation.

The loop reaches phase lock by comparing the coincidence of the leading edges of the reference and feedback clocks. Each time the feedback clock leads the reference clock, the coincidence comparator pulses the Pump Down line. Pump Down pulses cause the charge pump to vary the Control Voltage signal as necessary to reduce the Write VCO frequency until the reference and feedback clocks are coincident (phase-locked). Each time the feedback clock lags the reference clock, the coincidence comparator pulses the Pump Up line. Pump Up pulses cause the charge pump to vary the Control Voltage signal as necessary to increase the Write VCO frequency until phase lock occurs.

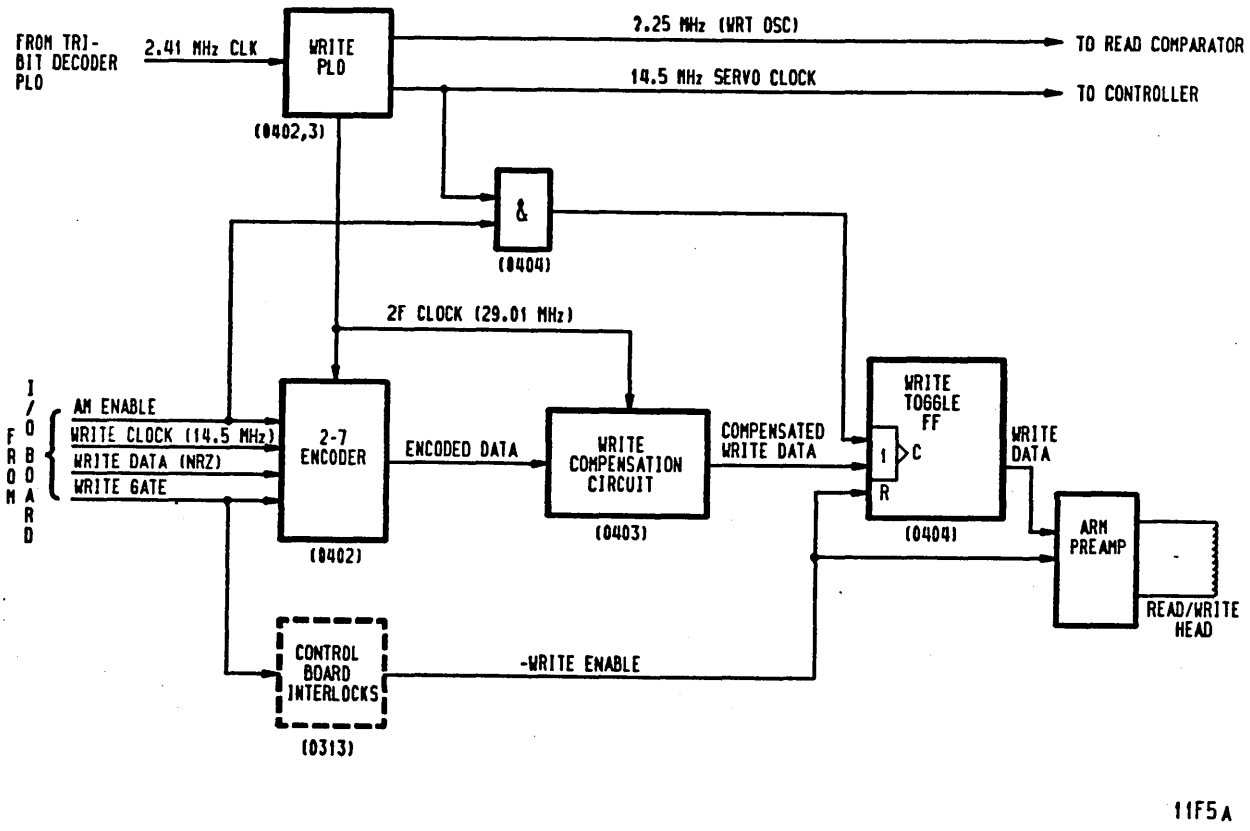


Figure 1-45. Write Circuits Block Diagram

The Write PLO circuit operates continuously whenever the servo signal is being decoded. The PLO provides the following outputs to other circuits:

- 2F (WRT OSC) signal to the 2-7 Encoder circuit.
- 14.5 MHz Servo Clock to the controller (via the interface). This is returned to the drive as Write Clock.
- 7.25 MHz clock to the Read Comparator circuit.

TABLE 1-7. WRITE CIRCUIT FUNCTIONS

Circuit	Function
Write PLO	Generates the 29.01 MHz Write Clock which is divided by two to develop the 14.5 MHz Servo Clock.
2-7 Encoder	Converts the NRZ data from the controller to 2-7 data.
Write Compensation Circuit	Compensates the data for problems caused by peak shift.
Write Toggle FF	Produces a write signal that changes polarity each time the compensated 2-7 data goes to a binary 1.
Arm Preamplifier	Switches the write current in the head coil as the signal from the write driver circuits changes polarity.

2-7 Encoder

The 2-7 Encoder converts NRZ data into 2-7 data. As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven NRZ code words and seven 2-7 code words. The encoder recognizes the coding in the write data string as a succession of the seven NRZ words, and outputs a series of 2-7 code words, each one translated from its NRZ equivalent. Table 1-6, presented under Basic Read/Write Principles, shows the translation used between the two groups of seven code words. The 2-7 encoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

The encoder uses synchronous timing circuitry controlled by two clock inputs, the 14.5 MHz Write Clock from the controller and the 29.01 MHz 2F Clock from the Write PLO (see figure 1-47). The encoder has a synchronizer that develops two clocks in phase with the 2F Clock -- the 2-7 Data Clock and a 14.5 MHz internal clock. The 2-7 Data Clock is supplied to the write compensation circuit. The internal clock shifts NRZ data into a pattern recognition circuit. Each time this circuit recognizes one of the seven NRZ code words, it parallel-loads an output shift register and starts looking for the following word.

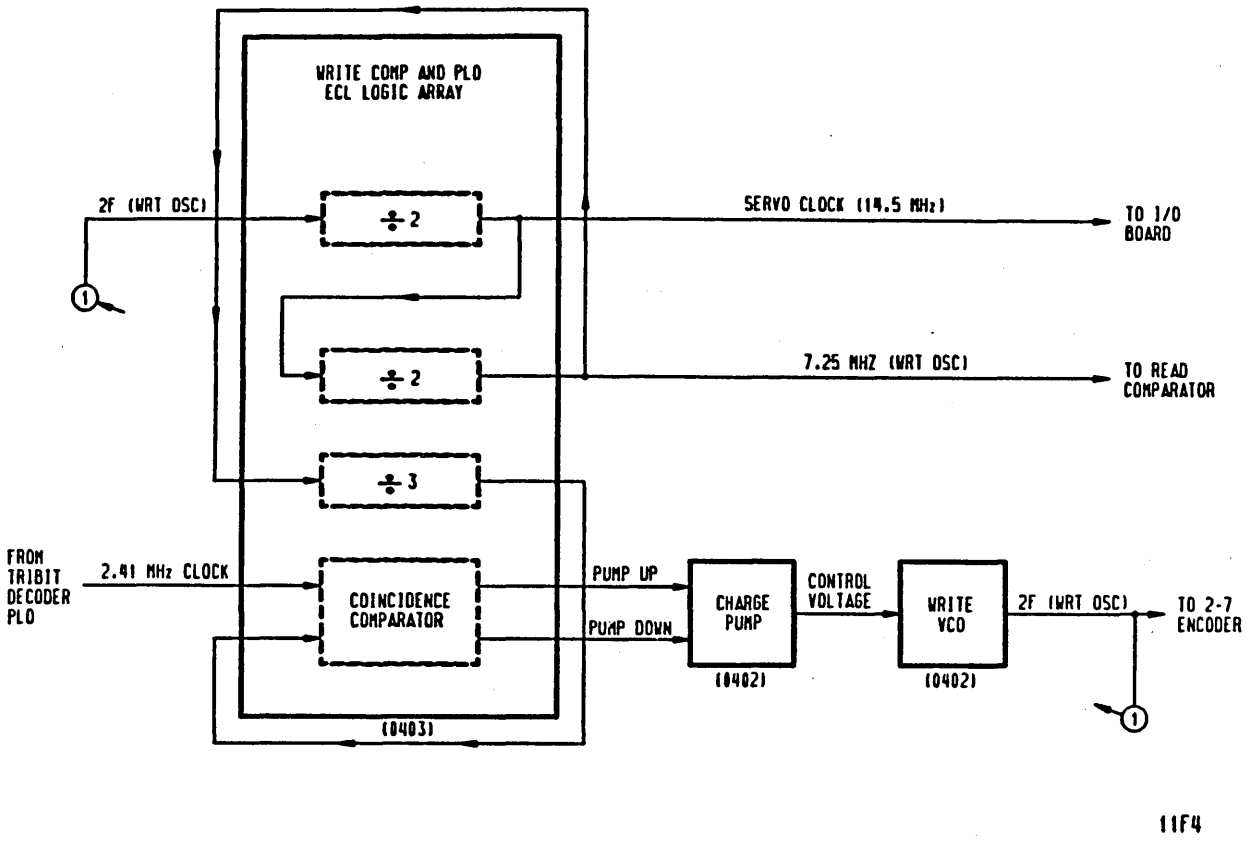


Figure 1-46. Write PLO Block Diagram

The output shift register shifts its contents on each rising edge of the 2F Clock. The active low serial output of the register is -Encoded Data. This line is active for binary ones and inactive for binary zeros in the 2-7 data.

The encoder begins translating NRZ code words with the second data bit clocked in by Write Clock after Write Gate goes inactive. Encoder operation proceeds continuously, processing all NRZ data except for the last bit received before Write Gate goes inactive.

Write Compensation Circuit

The write compensation circuit modifies the timing of transitions in the encoded 2-7 data in a manner that compensates for peak shift (refer to discussion on basic read/write principles).

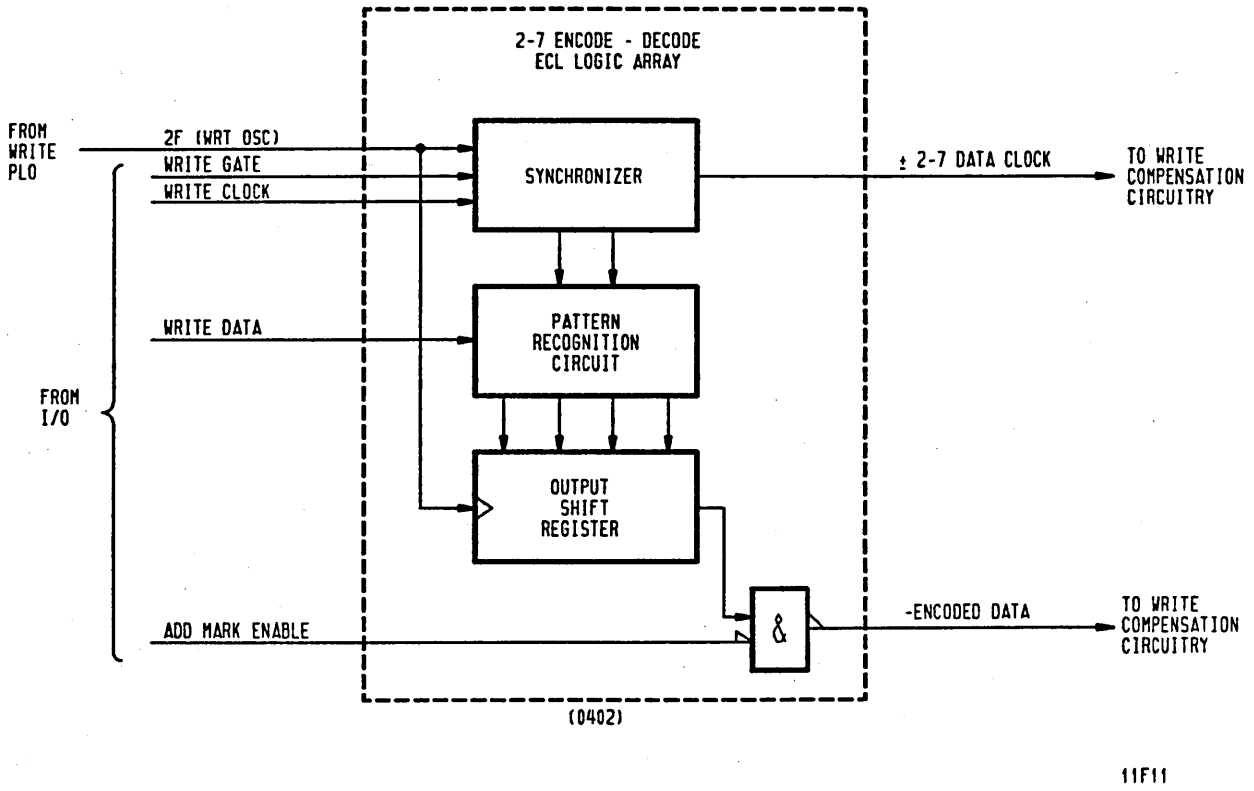


Figure 1-47. 2-7 Encoder Block Diagram

Encoded 2-7 data contains isolated bit cells at binary one preceded and followed by from two to seven bit cells at binary zero. Each time the data changes from binary zero to binary one, the head reverses its flux direction. Write compensation shifts this positive-going edge away from its nominal timing, and this timing change is related to the number of zeros preceding and trailing a binary one in the data pattern.

The write compensation function takes place in the Write Compensation and PLO ECL Logic Array (see figure 1-48). The delays with which the 2-7 Data Clock enters chip inputs E1-E3, L1-L3, or NOM produce specified time shifts for each possible data pattern. The pattern of time shifts is divided into two zones; an outer zone applicable to tracks 0 through 511, and an inner zone applicable to tracks 512 through 1216.

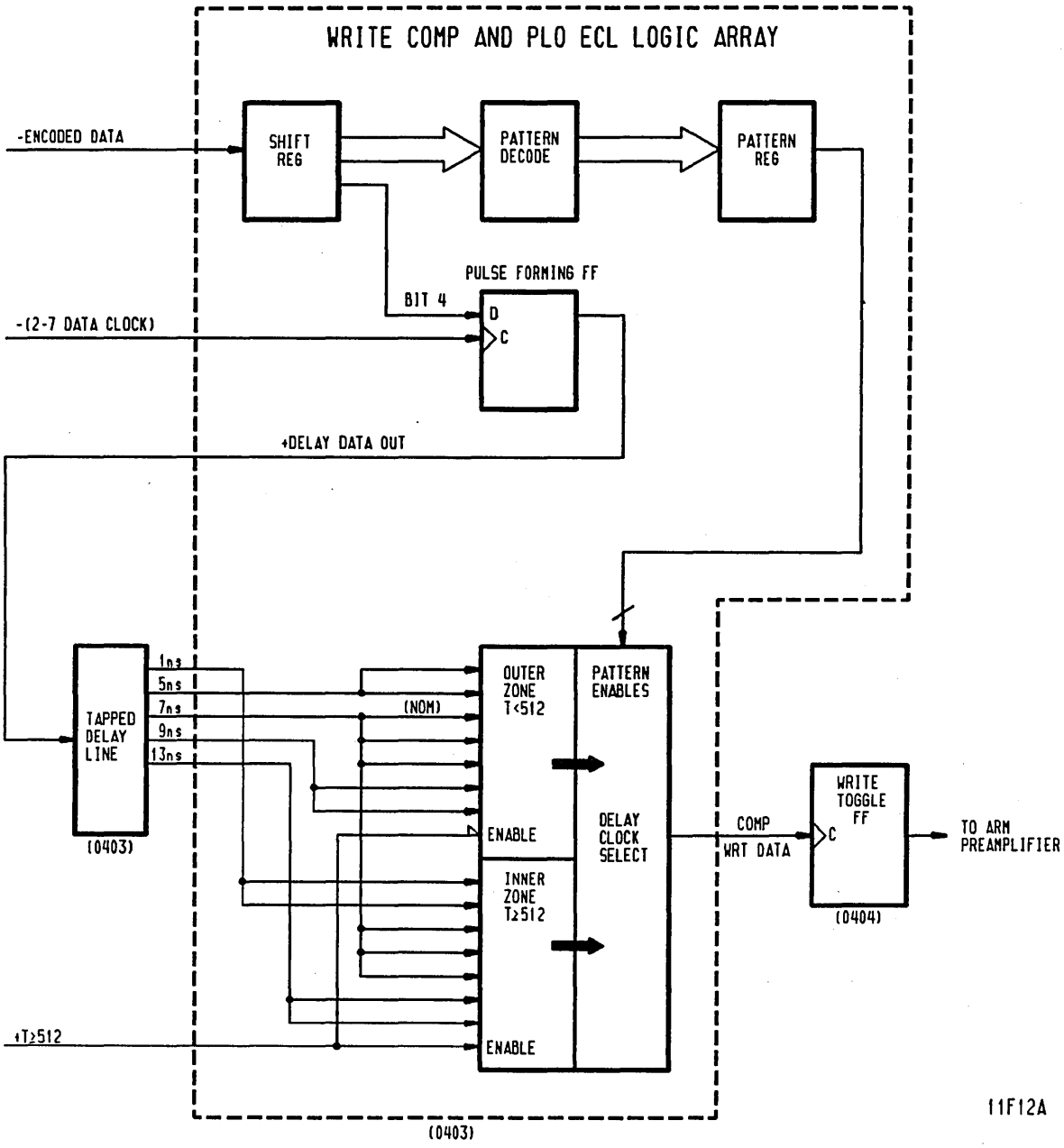


Figure 1-48. Write Compensation Block Diagram

Uncompensated data enters the circuit via the -Encoded Data line. This data is clocked into a 9-bit shift register. The delay line develops the clock input by delaying the 2-7 Data Clock. When the center bit of the shift register contains a binary one, the circuit looks at the number of register bits which are zero on each side of the center bit. Depending on the number of leading zeros and trailing zeros, one of the delayed clocks E1-E3, L1-L3, or NOM is applied to an AND gate along with the center bit of the register. Thus, the AND gate sees the center register bit go active, followed by the applied clock going active; with both inputs active, the gate outputs a compensated write data pulse. The positive edge of the compensated data pulse is timed by the clock selected. Tables 1-8 and 1-9 specify the clock input gated out of the write compensation circuit for each possible data pattern. Note that a majority of the data patterns use the NOM clock and have the nominal delay.

After being write compensated, the data is transmitted to the write driver circuit.

TABLE 1-8. DATA PATTERN (INNER TRACKS)

		Number of Trailing Zeros					
		2	3	4	5	6	7
Number of Leading Zeros	2	0 ns* NOM**	-6 ns E2	-6 ns E3	-6 ns E3	-6 ns E3	-6 ns E3
	3	+6 ns L2	0 ns NOM	0 ns E1	0 ns E1	0 ns E1	0 ns E1
	4	+6 ns L3	0 ns L1	0 ns NOM	0 ns NOM	0 ns NOM	0 ns NOM
	5	+6 ns L3	0 ns L1	0 ns NOM	0 ns NOM	0 ns NOM	0 ns NOM
	6	+6 ns L3	0 ns L1	0 ns NOM	0 ns NOM	0 ns NOM	0 ns NOM
	7	+6 ns L3	0 ns L1	0 ns NOM	0 ns NOM	0 ns NOM	0 ns NOM

* Top entry gives delay relative to nominal timing where negative numbers show early timing and positive numbers show late timing.

**Bottom entry indicates which delayed clock enables a compensated output pulse.

TABLE 1-9. DATA PATTERN (OUTER TRACKS)

		Number of Trailing Zeros					
		2	3	4	5	6	7
Number of Leading Zeros	2	0 ns* NOM**	-2 ns E2	-2 ns E3	-2 ns E3	-2 ns E3	-2 ns E3
	3	+2 ns L2	0 ns NOM	0 ns E1	0 ns E1	0 ns E1	0 ns E1
	4	+2 ns L3	0 ns L1	0 ns NOM	0 ns NOM	0 ns NOM	0 ns NOM
	5	+2 ns L3	0 ns L1	0 ns NOM	0 ns NOM	0 ns NOM	0 ns NOM
	6	+2 ns L3	0 ns L1	0 ns NOM	0 ns NOM	0 ns NOM	0 ns NOM
	7	+2 ns L3	0 ns L1	0 ns NOM	0 ns NOM	0 ns NOM	0 ns NOM

* Top entry gives delay relative to nominal timing where negative numbers show early timing and positive numbers show late timing.

**Bottom entry indicates which delayed clock enables a compensated output pulse.

Write Toggle FF

The Write Toggle FF has two clock inputs. For normal write operations, compensated write data is applied to one of the clock inputs. When an address mark is being written, a 14.5 MHz clock signal is gated (by the Address Mark Enable signal) to the other clock input. In either case, the FF changes state with each positive edge at its clock input. The write toggle FF operates only when the -Write Enable line is active (low), or when the -AME line is active (low) along with -Write Enable

active (low). With -Write Enable inactive, the latch remains cleared, and the Write Data lines to the arm preamplifier remain inactive. The -Write Enable line is active only when all the following are true:

- Write Gate is active
- Write Protect is not active
- No faults exist
- Speed OK is active
- Power Amp Enable signal is active

Arm Preamplifier

Each head arm contains an LSI chip that serves as a preamplifier for the heads attached to that arm. This LSI chip selects the data head and either switches write current through the head or amplifies the read signal detected by the head (see figure 1-49). These paragraphs concentrate on the preamplifier write function and assume that head selection has occurred.

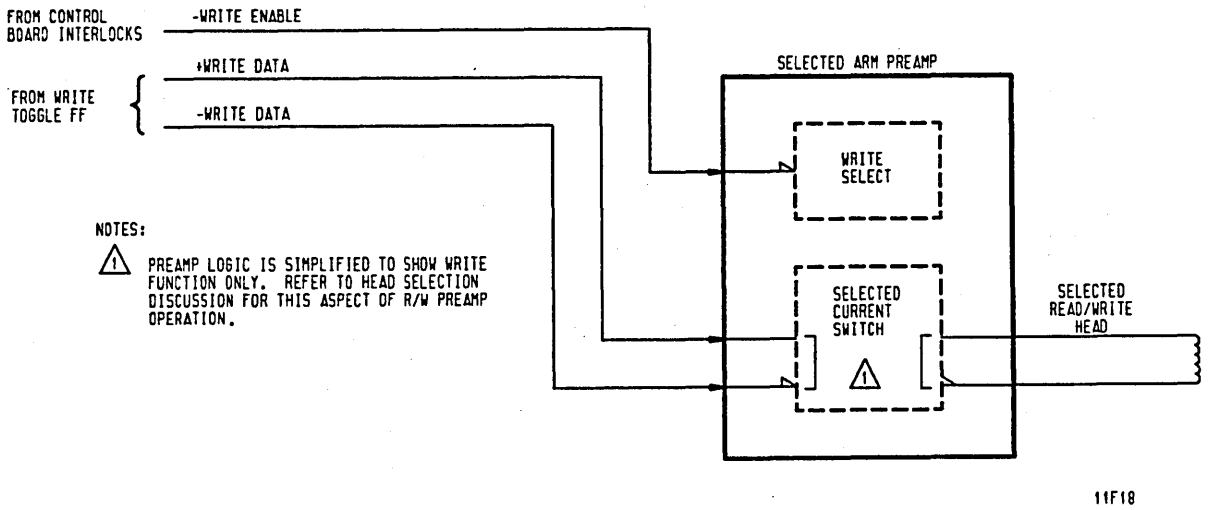


Figure 1-49. Arm Preamplifier

The LSI chip functions as a write driver when the -Write Enable line goes active (low). The chip develops regulated current for the selected head coil and reverses the current in that coil to produce flux reversals on the disk.

Throughout a write operation, write current is always flowing through the head coil. The Write Driver circuit inputs two Write Data lines to the selected arm preamplifier. When a transition occurs on the input lines, the LSI chip switches the write current direction through the head coil. This switching action produces a recorded flux reversal on the disk surface.

While an address mark is being written, the recorded flux reversals cycle at a 7.25 MHz rate.

READ CIRCUITS

General

Read operations are initiated by a Control Select (Tag 3) with Bus Out bit 1 true. This enables the preamplifier circuits, which sense the data written on the disk and generate analog read data signals.

The analog data goes to the Data Latch circuit which changes it into digital 2-7 data.

The Read Comparator and PLO circuit generates a 29.01 MHz Read Clock signal that is phase-locked to the 2-7 read data. The 2-7 Decoder changes the 2-7 data to NRZ data synchronized to a 14.5 MHz Read Clock. Both data and clock are then sent to the controller.

Figure 1-50 shows the main elements in the read circuits and table 1-10 briefly describes each of these elements. The following paragraphs further describe the read circuits.

Arm Preamplifier

The arm preamplifier is an LSI chip that selects one of the data heads on its head arm and either switches write current through the head or amplifies the read signal detected by the head. These paragraphs concentrate on the preamplifier's read function and assume that head selection has occurred.

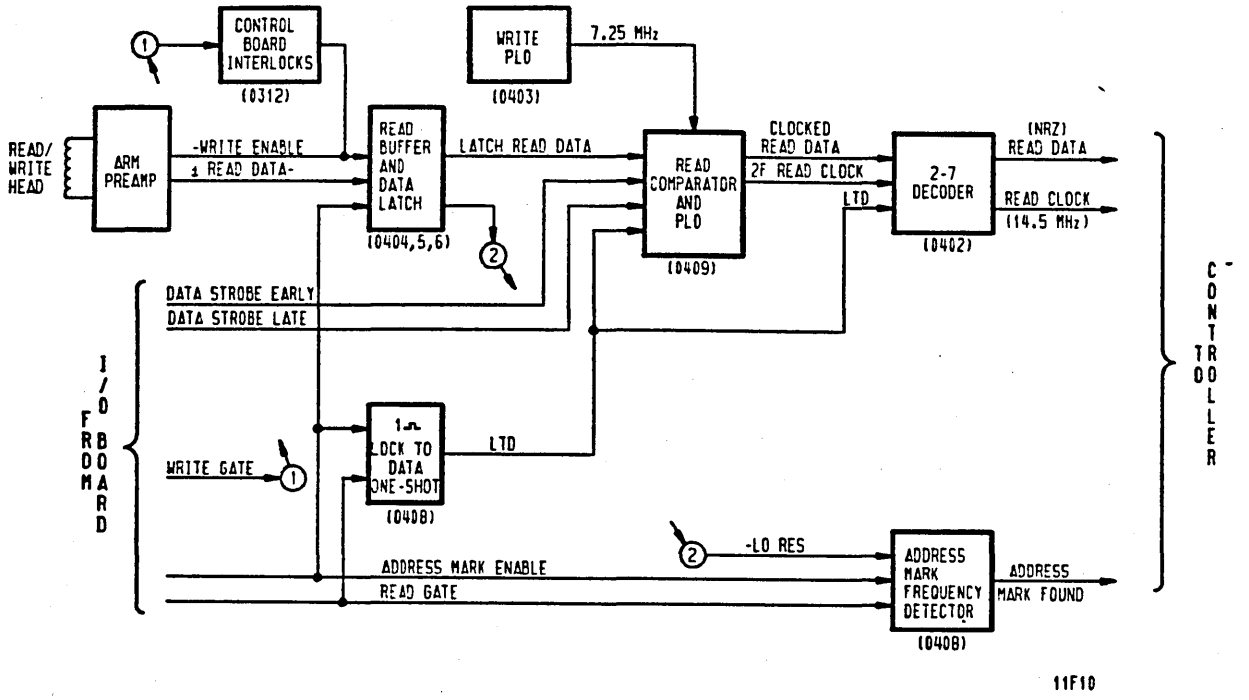


Figure 1-50. Read Circuits Block Diagram

The LSI chip functions as a read preamplifier when the -Write Enable line is inactive (high). The chip contains a differential amplifier that is enabled by head selection. In read operations, the coil in the selected head develops a read-back pulse when the head passes over a written flux reversal on the disk. The read-back pulse is supplied as a differential input to the preamplifier.

The differential amplifier selected in the chip amplifies the read signal and sends it on the Read Data lines to read circuitry on the read/write board.

Data Latch Circuit

The Data Latch circuit receives analog read data from the selected arm preamplifier and converts it into digital data. As shown in figure 1-51, most of the Data Latch circuit is located inside the Data Latch Analog Master Chip.

TABLE 1-10. READ CIRCUIT FUNCTIONS

Circuit	Function
Arm Preamplifier	Processes the analog signal from the data head so that it can be used by the Data Latch circuit.
Data Latch Circuit	Changes the analog 2-7 data into digital 2-7 data. This data is sent to the Read Comparator circuit.
Read Comparator and PLO Circuit	Develops a 29.01 MHz Read Clock that is synchronized to 2-7 read data.
2-7 Decoder	Translates data coding from 2-7 to NRZ modulation and generates 14.5 MHz Read Clock synchronized to NRZ data. NRZ data is sent to the controller with the 14.5 MHz Read Clock.
Address Mark Detector	Detects the address mark frequency (7.25 MHz) and transmits an Address Mark Found to the controller.

The input signal is amplified by the amplifier, provided that -Write Enable is inactive (high). The signal is split into two signal paths -- the high resolution channel and the low resolution channel. The high and low resolution channels contain independent wave-shaping circuitry, and they provide separate inputs to the Data Latch FF. The high resolution channel supplies delayed clock pulses to the Data Latch FF, and the low resolution channel supplies a D-input to the Data Latch FF. Successive clock pulses toggle the FF when the D-input has changed. For each transition of the Data Latch FF, a one-shot pulses the $\pm$Latched Data output lines. Thus, there is an output pulse for each written flux transition sensed by the data head.

Splitting the analog data signal into two paths and combining the high and low resolution channels in the Data Latch FF is a system that discriminates against high frequency noise components in the Analog Data but maintains the timing of the data transitions. The low resolution channel uses a band-pass filter (with a 5 MHz bandwidth) followed by a zero-cross detector

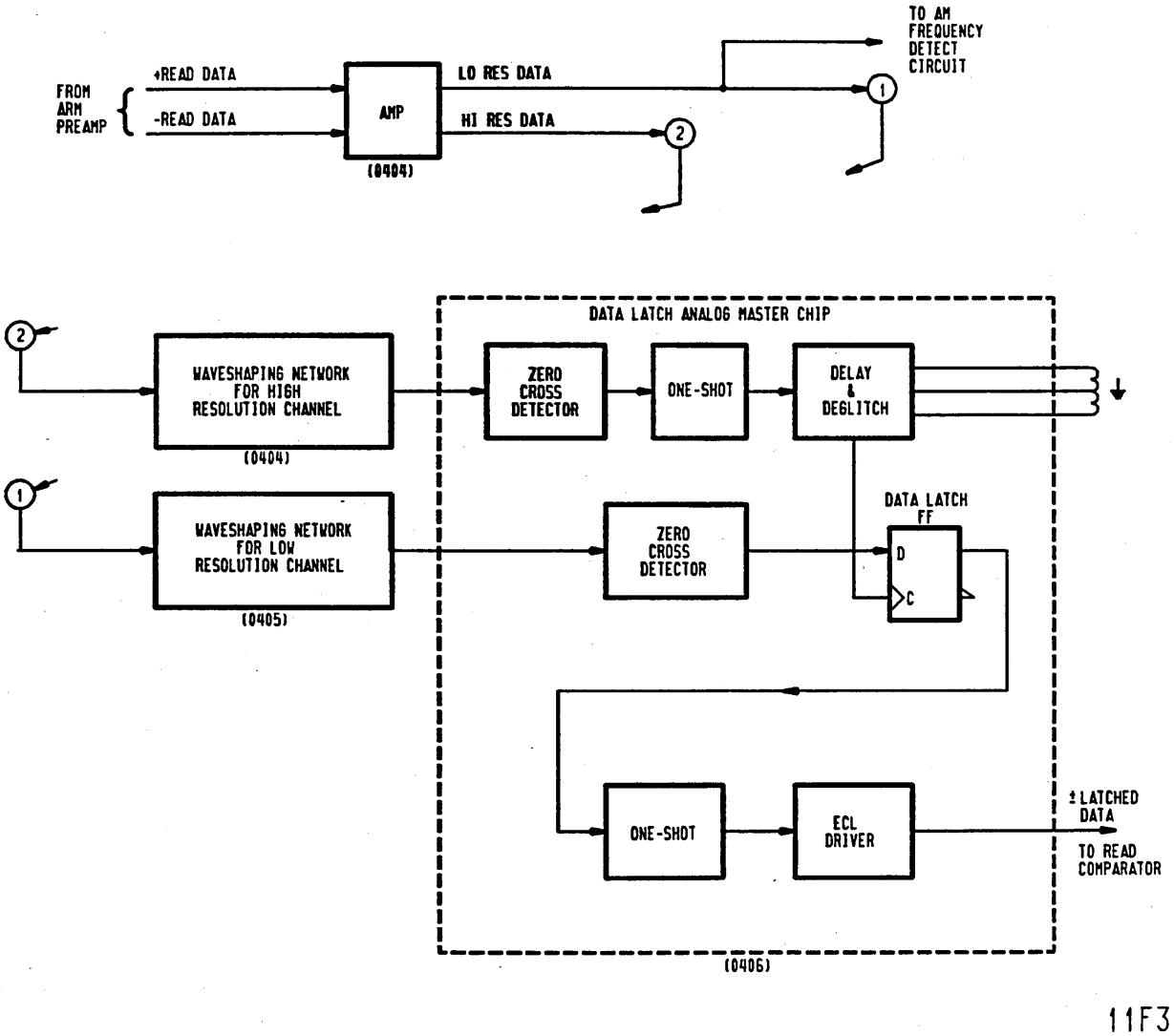


Figure 1-51. Data Latch Block Diagram

to develop a digital waveform similar to the Write Data waveform used in recording. However, filtering out the high frequency components of the input signal lowers the timing resolution of the channel's output signal. The high resolution channel uses a band-pass filter (with a 13 MHz bandwidth) followed by a zero-cross detector and a delayed pulse-forming circuit. With its wider bandwidth, this channel closely follows the timing present at its input. Each change in the low resolution signal is clocked into the Data Latch FF by a delayed clock pulse from the high resolution channel. Erroneous clock pulses from the high resolution channel do not toggle the Data Latch FF because they do not follow a change in the FF's D-input.

The ±Latched Data from the Data Latch circuitry is sent to the Read Comparator ECL Logic Array.

Read Comparator and PLO

The Read Comparator and PLO circuitry uses a phase-locked loop to generate the 29.01 MHz Read Clock, and processes latched read data from the Data Latch to develop clocked read data. Data Strobe commands from the controller condition the timing of clocked read data relative to the read clock to provide a means of error recovery to the read circuitry.

Figure 1-52 is a simplified block diagram of the Read Comparator and PLO circuitry. The phase-locked loop uses the Read Oscillator Control portion of the Read Comparator ECL Logic Array to regulate operation of the Current Pump and to provide stop/start control of the Voltage-Controlled Oscillator (VCO). The Current Pump supplies a Control Voltage signal to the VCO that determines the frequency of the 2F RD OSC signal output from the VCO. The 2F RD OSC signal is fed back to the Read Oscillator Control to complete the loop.

The phase-locked loop locks the VCO frequency to one of two reference signals. When the drive is reading data (-Read Gate low), the phase-locked loop uses the pulse train on the Latched Data line as a timing reference. In this case, the Read Oscillator Control uses a quadrature comparator to drive the Pump Up and Pump Down lines as necessary to keep the rising edges of the 2F RD OSC signal coincident with the rising edges of +Latched Data pulses. For each Latched Data pulse, the quadrature comparator outputs a variable-length pulse on the Pump Up line, followed by a fixed-length pulse on the Pump Down line. When the Pump Up and Pump Down pulses differ in length, the Control Voltage to the VCO varies accordingly to phase shift the VCO and bring it into phase lock.

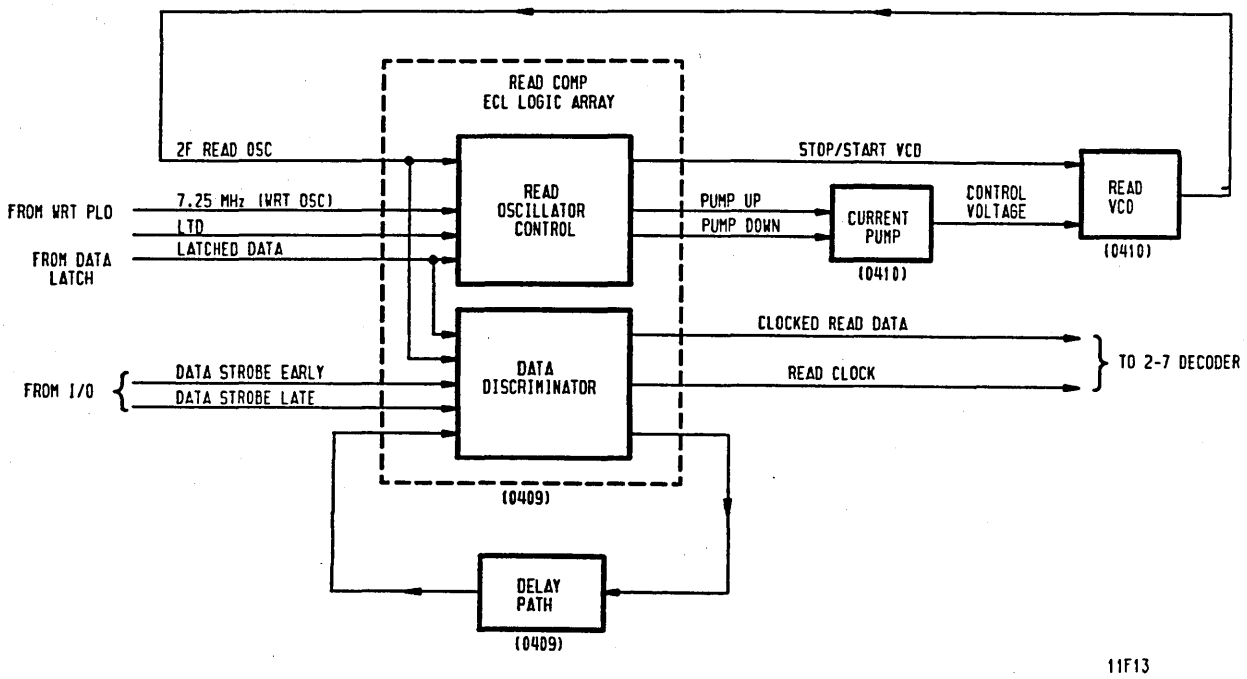


Figure 1-52. Read Comparator and PLO Block Diagram

When the drive is not reading data (-Read Gate high), the phase-locked loop maintains the VCO frequency close to the value it has during read operations. In this mode, a coincidence comparator in the ECL Logic Array monitors the phase difference between the 7.25 MHz WRT OSC signal (derived from the Write PLO) and the 2F RD OSC signal fed back from the VCO. When the rising edge of the 7.25 MHz signal leads the rising edge of the 2F signal, this comparator pulses the Pump Up line to increase the Read VCO frequency. Conversely, when the rising edge of the 7.25 MHz signal lags the rising edge of the 2F signal, this comparator pulses the Pump Down line to decrease the Read VCO frequency.

The Read Oscillator Control circuitry uses the Stop/Start VCO line to control VCO operation while switching between the quadrature and coincidence comparators. The Stop/Start VCO line goes active for approximately 138 ns after the Latched Data pulse following a change in the Read Gate signal. While the Stop/Start VCO line is active, the VCO is inhibited, and its control voltage is held constant. This enables the Read PLO to phase lock within 2 microseconds during the switching transitions.

The Data Discriminator portion of the Read Comparator ECL Logic Array conditions the 2F Read Clock and Clocked Read Data signals for use in the 2-7 Decoder (see figure 1-52). With nominal timing, pulses on the Clocked Read Data line are active for one 2F bit cell (34.45 ns), and positive transitions of the 2F Read Clock coincide with the center of Clocked Read Data pulses. For error recovery, the controller can issue a Data Strobe Early or a Data Strobe Late command to shift this timing either way from its nominal value. The controller commands Data Strobe Early by issuing Tag 3 (Control Select) with Bus Out bit 7 active. The Data Discriminator responds by routing the clock signal through a 2.9 ns delay path. This process delays the 2F Read Clock relative to the Clocked Read Data pulses. The controller commands Data Strobe Late by issuing Tag 3 with Bus Out bit 8 active. The Data Discriminator responds by routing the data signal through a 2.9 ns delay path. This process delays the Clocked Read Data pulses relative to the 2F Read Clock.

The Clocked Read Data and 2F Read Clock signal are input to the 2-7 Decoder, which converts the read data from 2-7 code into NRZ form and generates the 14.5 MHz Read Clock.

2-7 Decoder

The 2-7 Decoder converts 2-7 data into NRZ data and generates the 14.5 MHz Read Clock from the 29.01 MHz Read Clock. Both inputs, the 2-7 data and the 29.01 MHz Read Clock, come from the Read Comparator and PLO circuitry.

As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven 2-7 code words and seven NRZ code words. The decoder recognizes the coding in the 2-7 read data input as a succession of the seven 2-7 words, and outputs a series of NRZ code words, each one translated from its 2-7 equivalent. Table 1-6, presented under Basic Read/Write Principles, shows the translation used between the two groups of seven code words. The 2-7 decoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

Figure 1-53 is a simplified block diagram of the 2-7 Decoder. The decoder synchronizes after the +Lock to Data input goes inactive (low). This occurs 3 microseconds after Read Gate or Address Mark Enable goes active. Once +Lock to Data goes inactive, synchronization occurs when the 2-7 input data contains three or more binary zeros followed by a binary one. This binary one sets up the proper phase of the 14.5 MHz Read Clock relative to the NRZ Data output line and initiates the decoding process. The clock and decoding operations are discussed in the following paragraphs.

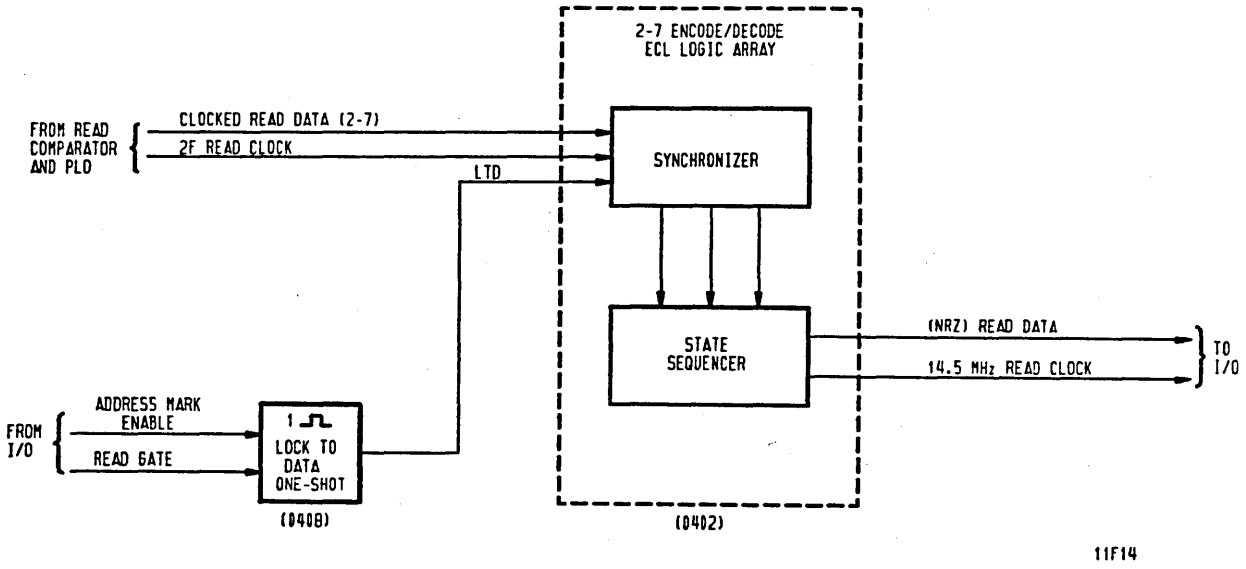


Figure 1-53. 2-7 Decoder Block Diagram

The 14.5 MHz Read Clock is generated from the 29.01 MHz Read Clock as this signal clocks a divide-by-two FF. The Q-output of the FF is inverted and supplied to the D-input through a gate that is enabled as a result of synchronization. Synchronization selects which positive edge of the 29.01 MHz Read Clock determines the positive edge of the 14.5 MHz Clock.

The decoding function is performed by a state sequencer. The state sequencer has eight FFs, and each of the eight states corresponds to one of the FFs being set. It operates by shifting states on each falling edge of the 14.5 MHz Read Clock. Thus, the interval for each state is one NRZ bit cell (68.9 ns). Two factors determine the current state of the sequencer. These are the previous state and the binary values of the last two 2-7 data bits input to the circuit. Therefore, at any time the state of the sequencer reflects the recent decoder inputs. The binary level decoded on the NRZ Data lines is state-dependent. During two of the states (NRZ bit cells), the output is binary zero, and during the other states, the output is binary one. In summary, the way the sequencer maps one state into the next state implements the specified translation from 2-7 data words into NRZ data words.

The decoder output stays low until synchronization occurs, and there is a processing delay of four 2-7 bit cells within the decoder.

The decoder sends the ±NRZ Read Data and ±Read Clock outputs to the I/O board to be transmitted on the interface to the controller.

Address Mark Detection

The Address Mark Detector, monitors the -Low Resolution signal from the Read Amplifier during an address mark search. If a frequency of 7.25 MHz is decoded over a period equivalent to three byte times, the detector sets the +Address Mark line, and the I/O circuitry sends the Address Mark Found signal to the controller.

Figure 1-54 shows the input and output signals for the Address Mark Detector. An address mark search occurs when the controller issues Tag 3 (Control Select) with Bus Out bits 1 and 5 active. In this situation, the -Read Gate line and the -Address Mark Enable line are both low. Together, these two signal inputs enable the Address Mark Detector.

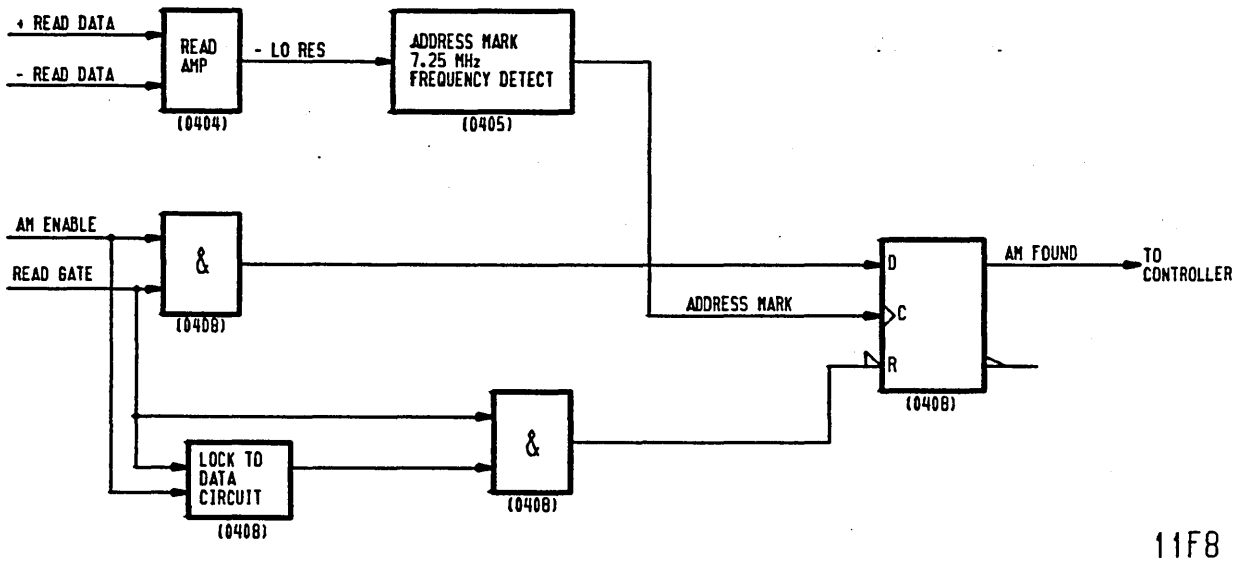


Figure 1-54. Address Mark Detector Block Diagram

The Address Mark Found line remains set until the lock-to-data interval ends (3 microseconds after Address Mark Enable is cleared) or until -Read Gate goes high.

FAULT AND ERROR CONDITIONS

GENERAL

The following paragraphs describe those conditions which are interpreted by the drive as either faults or errors. These conditions are divided into two categories: (1) those that generate the Fault signal and (2) those that do not generate the Fault signal. Included in the following descriptions are a list of conditions that produce specific fault or error status, the effect of that status on drive operation, and actions that clear the status indication to return the drive to normal operation.

CONDITIONS INDICATED BY FAULT SIGNAL

General

The drive has monitoring circuitry that recognizes seven types of error conditions. When any of these fault conditions occurs, the drive sets the respective latch in the SMD-E Gate Array. An OR circuit in the gate array receives inputs from the seven latches; if one or more of the latches is set, the OR circuit activates the Fault line. Fault status is returned to the controller on Bus In bit 3 in response to Tags 1 through 3 or the Unit Select Tag. The Fault line remains active until the latches are cleared.

If the unit is configured with an SMD-E interface, the seven possible fault conditions can be interrogated directly by the controller on Bus In bits 0 through 6 by executing a Tag 5 with all Bus Out bits set to zero.

When the Fault condition occurs, the Control MPU lights the Fault indicator on the status/control panel (if installed), disables write operations, and inactivates the Ready latch in the SMD-E Gate Array. If start conditions exist, the Ready indicator on the status/control panel (if installed) flashes until the fault is cleared (see figure 1-55).

Provided the fault condition or conditions no longer exist, the Fault signal is cleared by the following:

- Controller Fault Clear command (Tag 3 with Bus Out bit 4)
- Fault Clear switch on status/control panel (if present)
- Powering down the drive

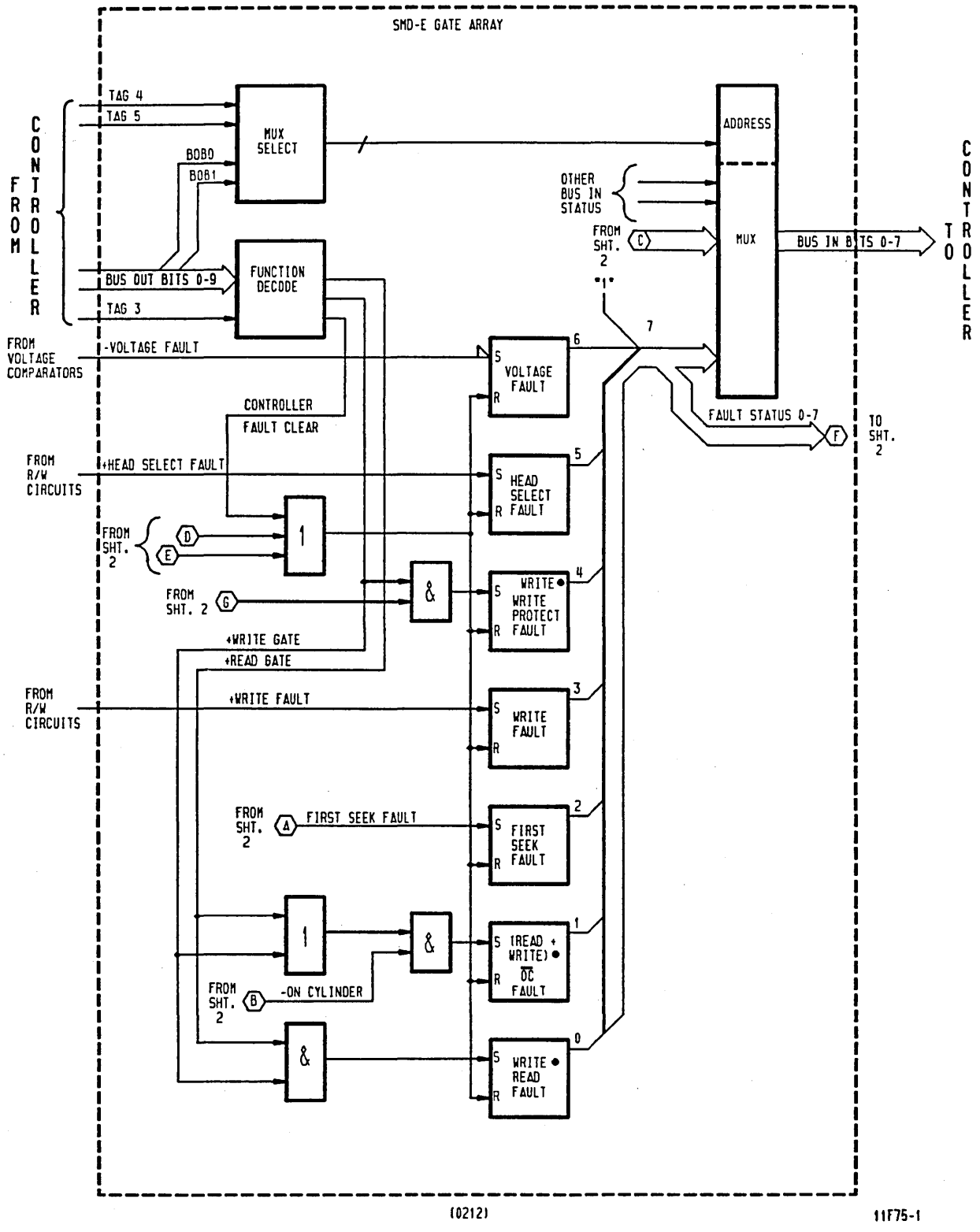


Figure 1-55. Fault and Error Detection Circuitry
(Sheet 1 of 2)

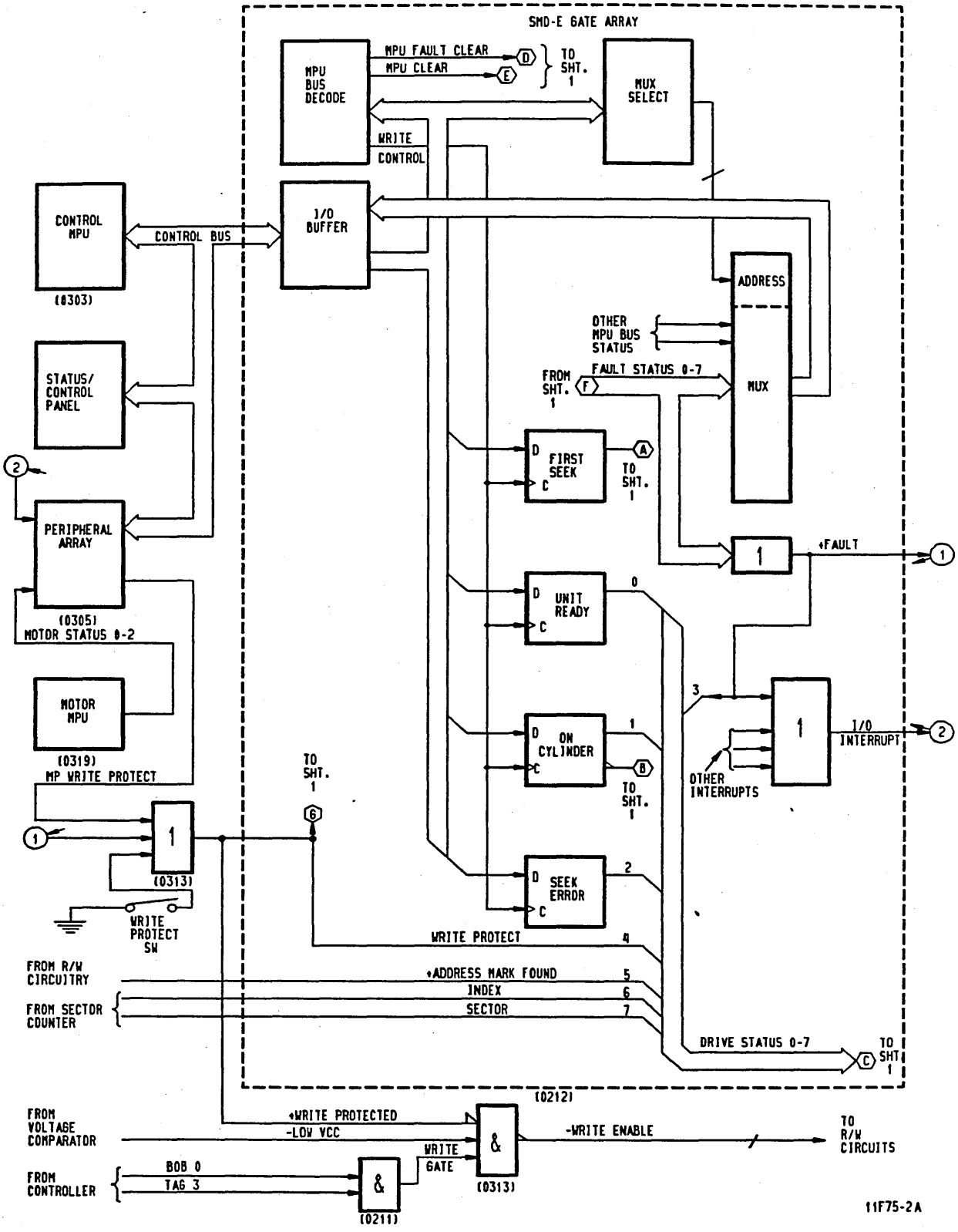


Figure 1-55. Fault and Error Detection Circuitry (Sheet 2)

The controller Fault Clear command is decoded inside the SMD-E Gate Array to develop a reset input for the seven latches. When the Fault Clear switch (if present) is pressed, it interrupts the Control MPU. The Control MPU responds by sending a reset code on the Control Bus lines for the seven latches. In either case, the reset input will clear a latch only if it is no longer being set by the error condition. In the process of removing and reapplying power to the drive, the fault circuitry is initialized as part of the power sequence, and any pre-existing fault status is lost.

The following paragraphs describe the individual fault conditions which set each of the latches in the SMD-E Gate Array and thus activate the Fault signal.

Voltage Fault (Tag 5, BIB6)

This fault is generated whenever the +12, -12, +5 or -5 voltages are detected to be below satisfactory operating levels. These voltages are monitored by threshold detectors on the control board.

When the Voltage Fault signal goes low, it sets the individual fault latch in the SMD-E Gate Array and latches the Power Amp Enable signal inactive in the Peripheral Array. Resetting the Power Amp Enable latch sets the +MP Write Protect latch. Setting the +MP Write Protect latch protects existing data on the disks by inhibiting the write circuitry while a voltage problem exists. This supplements the write protection normally invoked when the Fault line is active or when the drive is placed in the Write Protect mode.

An additional voltage detector circuit detects when the +5 V supply drops to 4.67 V, making microprocessor operation unreliable. This condition generates a -Low Vcc signal used to reset the Sector Counter, the Servo MPU, Motor MPU, and produce the DC Master Clear signal for the Control MPU. Also, when the Low Vcc signal goes active, the -Retract and +Power Amp Enable signals from the Control MPU (via the Peripheral Array) go low to produce an emergency retract of the actuator.

Read or Write and Off Cylinder (Tag 5, BIB1)

This fault is generated if the drive is in an off cylinder condition and it receives a Read or Write gate from the controller (Tag 3 and Bus Out bit 0 or 1). The SMD-E Gate Array contains decode logic for both Read Gate and Write Gate, and also contains the On Cylinder FF. When the On Cylinder FF is cleared and either gate goes active, logic in the gate array sets the associated fault latch.

Write Fault (Tag 5, BIB3)

A write fault is encoded if any of the following conditions exist:

- Write Gate received while drive is in Write Protected mode
- Write Clock not present when Write Gate is active
- No write data transitions when the Write Gate is active
- Head open (bad head detected)
- No Arm Enable signal is active when Write Enable is active.

All conditions except the first one activate the Write Fault line coming from the read/write board. Gating circuitry on the read/write board develops the Write Fault signal when individual fault conditions are detected, provided that Write Enable or Address Mark Enable are active. The gating circuitry keeps the Write Fault line inactive during transitions between read and write operation. The Write Fault line or the combination of Write Protect and Write Gate lines active sets the associated latch in the SMD-E Gate Array.

Head Select Fault (Tag 5, BIB5)

This fault is generated when more than one head is selected during a write operation. When this condition is detected, it sets the associated latch in the SMD-E Gate Array.

Read and Write Fault (Tag 5, BIB0)

This fault is generated whenever the drive receives a Read Gate and a Write Gate simultaneously. This condition is detected in the SMD-E Gate Array and sets the associated latch.

Write and Write Protected Fault (Tag 5, BIB4)

This fault is generated whenever a write operation is attempted while the drive is in a Write Protected mode.

First Seek Fault (Tag 5, BIB2)

First Seek fault, as opposed to Seek Error, results from error conditions that occur during the load operation. Seek Error, on the other hand, indicates error conditions that occur during normal seeks and RTZ seeks. A First Seek fault generates an active Fault signal while a Seek Error activates the Seek End line to the controller. Seek Errors are discussed in the next topic, and the error conditions that cause a First Seek fault are described in the following paragraphs.

Unlike the other individual fault latches, the latch for First Seek fault is set by the Control MPU. To set the latch, the Control MPU inputs the SMD-E Gate Array with an address on the Control Bus. The error conditions resulting in a First Seek fault are monitored by the Control MPU during the power on initialization and load operation. Assuming that the Control MPU is operational, it sets the associated latch in the SMD-E Gate Array if any of the following tests fail:

- Demodulator inactive at the start of the load, but changing to active after the heads move inward from the landing zone. Demodulator must remain active throughout the rest of the load.
- The Fault line stays inactive during the load.
- The Servo MPU moves the heads out of the landing zone and detects 100 cylinder pulses before a timeout occurs.
- At least one cylinder pulse is detected by the Servo MPU in the outer guard band as the heads approach track zero.
- The time required for the load portion of the seek is less than the 500 millisecond timeout allowed by the Control MPU.
- The time required for the RTZ portion of the seek is less than the 500 millisecond timeout allowed by the Control MPU.
- On cylinder sense detected during track-following. If on cylinder sense goes inactive after start of trackfollowing, it returns to the active state and does not go inactive more than 16 times.
- Fewer than three cylinder pulses detected during track following.

The Control MPU aborts the load operation when a First Seek fault is detected. A controller Fault Clear command or pressing the Fault Clear switch on the status/control panel (if present) will reset the Fault signal, turn off the Fault indicator on the panel, and initiate another load attempt.

ERRORS NOT INDICATED BY FAULT SIGNAL

General

One type of error does not generate Fault status -- seek error. The seek error does, however, have an associated status FF.

Seek Error

Seek Error is a status signal indicating error conditions that occur during normal seeks and RTZ seeks. The Seek Error signal is active when the Seek Error FF, located in the SMD-E Gate Array, is set.

During normal seeks and RTZ seeks, the Servo MPU tests certain error conditions. If any tests fail, the Servo MPU sets the Seek Error FF in the SMD-E Gate Array. These tests include the following:

- The new cylinder address, specified by the controller for a normal seek, is less than or equal to 1216.
- The Demodulator Active signal is active at the start and end of normal seeks, and it is active throughout RTZ seeks.
- Fault stays inactive throughout seeks.
- The time required for a normal seek is less than the 60 millisecond timeout allowed by the Control MPU.
- On cylinder sense detected during track-following. If on cylinder sense goes inactive after start of track-following, it returns to the active state and does not go inactive more than 16 times.
- Fewer than three cylinder pulses are detected during track-following.
- A voltage fault has not occurred.

If any test fails, the Control MPU sends Seek Error status to the controller. In the event of a Seek Error, the Control MPU halts the Servo MPU which disables the power amplifier allowing the heads to remain in their current position over the disks. The seek error condition cannot be cleared except by a controller RTZ command. An attempt by the controller to perform a read or write operation while the seek error condition exists will result in the generation of a Read or Write and Off Cylinder fault.

STATUS/CONTROL PANEL FUNCTIONS

The status/control panel switches permit the user to select a logical unit number for the drive (Note: A logical unit selection made at the status/control panel overrides a selection made on the control board switches), initiate a load/unload operation on units configured for local mode operation, clear fault conditions, activate write protect mode, and initiate off-line diagnostic testing. The status/control panel LEDs indicate the logical unit number selection, unit selected, unit ready, fault condition active, and write protect mode active.

The circuitry consists of a bidirectional buffer, a command decode PAL, a membrane keyboard, a switch decode PAL, a combination 4 X 64 memory chip, a liquid crystal display (LCD), and miscellaneous switch selection/display latches (refer to figure 1-56).

The Control MPU periodically checks the status/control panel logic to determine if any of the membrane switches have been pressed (Note: Control MPU does not respond to numeric, execute, backspace, and space keys when operating in normal mode). If a switch has been pressed, the Control MPU firmware decodes the switch selection and performs the requested function. In addition, if the logical address of the unit was entered, or the Start, or Write Protect switch on the status/control panel was pressed, the Control MPU stores this information in the RAM portion of the memory chip. (Note: If a status/control panel is not installed, the Control MPU determines the logical unit number and write protect status from switches on the control board.) If dc power is lost, the +Low VCC signal from the Control MPU causes the Start, Write Protect, and logical unit switch selections stored in the RAM portion to be transferred to the ROM portion of the memory chip. On power up, the Control MPU activates the -Recall line causing the data to be copied from the ROM portion back into the RAM portion of the memory chip.

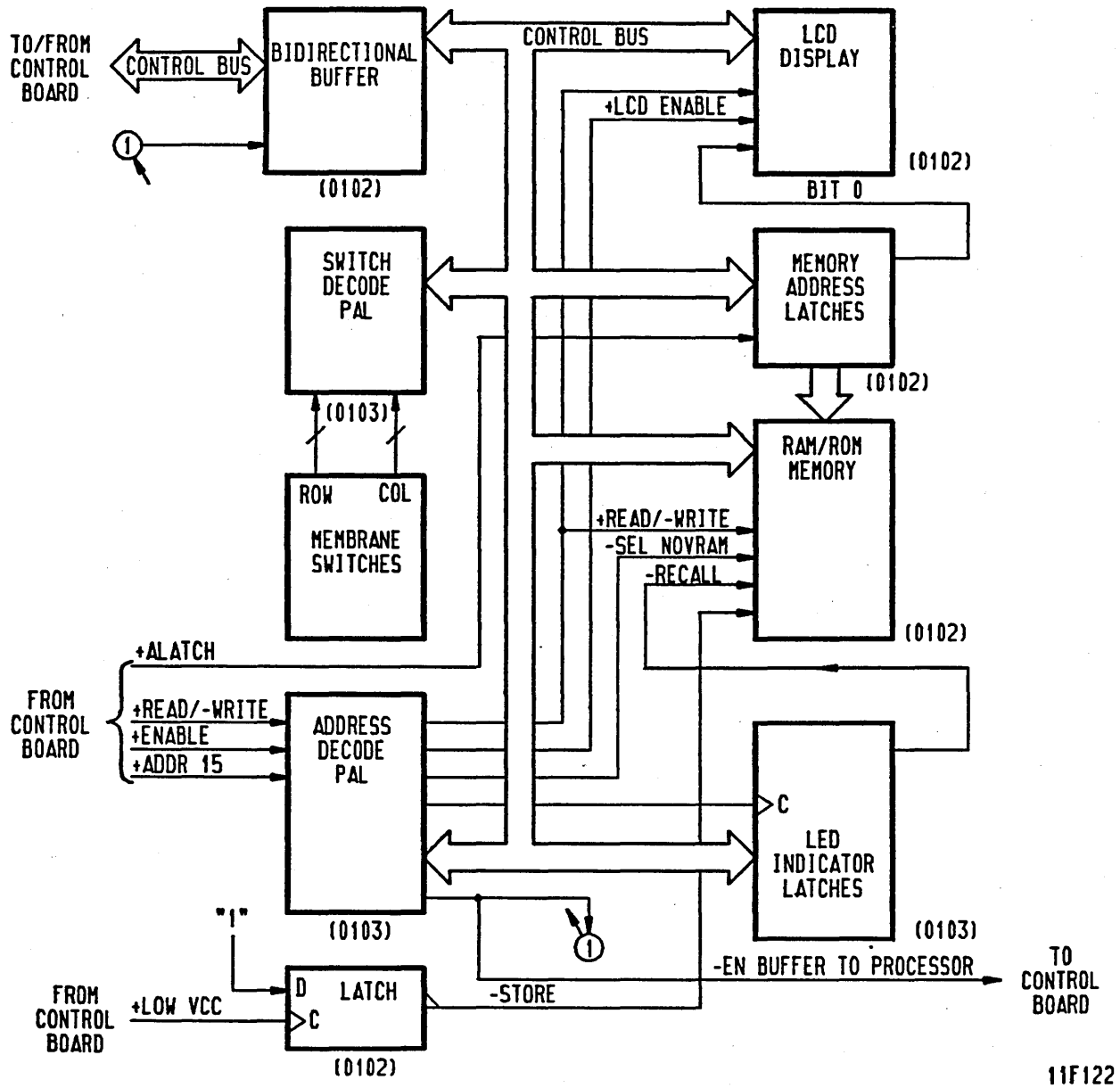


Figure 1-56. Status/Control Panel Block Diagram

The liquid crystal display can be used to display drive status/ error codes, fault messages, and the current cylinder address.

DIAGNOSTIC FUNCTIONS

The off-line diagnostics provided with the drive allow the operator to locate and isolate drive malfunctions to the field replaceable unit (FRU) level. Testing consists of a master diagnostic test, and a number of selectable subtests, that can be activated at the status/control panel. When configured for SMD-E interface, the master diagnostic test can also be activated by performing a diagnostic execute status command (Tag 5 with Bus Out bits 0 and 1 both set to 1).

During diagnostic testing, the Control MPU examines internal data logs to determine which field replaceable unit is malfunctioning. These internal data logs contain a history of the 8 most recent fault codes, and the 8 most recent drive status codes.

Section 3 of this manual provides instructions on initiating diagnostic tests via the status/control panel, and information on interpreting the test results indicated on the status/control panel liquid crystal display (LCD).

SECTION 2

GENERAL MAINTENANCE INFORMATION

INTRODUCTION

This section contains general information relating to maintenance of the drive. A person performing maintenance should be familiar with the information in this section, in addition to being thoroughly familiar with drive operation. Information is divided into the following areas:

- Warnings and Precautions - Lists warnings and precautions that must be observed when working on the drive.
- Electrostatic Discharge Protection - Provides instructions for the proper handling of electrostatically sensitive devices.
- Maintenance Tools and Materials - Lists the tools and materials required to perform maintenance on the drive.
- Testing the Drive - Provides information concerning the electrical testing of the drive.
- Accessing Assemblies for Maintenance - Identifies the various parts of the drive and describes how to access these parts for maintenance.

WARNINGS AND PRECAUTIONS

WARNING

The following topic provides warnings and precautions that must be observed during maintenance. Refer also to Important Safety Information and Precautions located in the front of this manual following the table of contents. Failure to observe the warnings, precautions, and other safety information provided in this manual could result in personal injury.

Observe the following warnings and precautions at all times. Failure to do so may cause equipment damage and/or personal injury.

- Use only CDC/MPI replacement parts. Using non-CDC/MPI replacement parts can adversely affect safety. Using other manufacturers' parts could also degrade reliability, increase maintenance downtime, and void warranty coverage.

- Use care while working with the power supply because line voltages are always present when the ac power cord is connected to a power source.

- Do not attempt to disassemble the module. It is not field repairable. Replace the entire module assembly if it is found to be defective.

- Do not operate the drive over an extended period of time without the top cover installed.

- Always deenergize drive before removing or installing circuit boards, cables, or any other electrical components.

- Observe the precautions listed under Electrostatic Discharge Protection.

- If the power supply is placed on a bench for testing, position the supply so that all ventilation holes are open, to allow proper air flow to internal components.

ELECTROSTATIC DISCHARGE PROTECTION

All drive electronic assemblies are sensitive to static electricity, due to the electrostatically sensitive devices used within the drive circuitry. Although some of these devices such as metal-oxide semiconductors are extremely sensitive, all semiconductors as well as some resistors and capacitors may be damaged or degraded by exposure to static electricity.

Electrostatic damage to electronic devices may be caused by a direct discharge of a charged conductor, or by exposure to the static fields which surround charged objects. To avoid damage to drive electronic assemblies, service personnel must observe the following precautions when servicing the drive:

- Ground yourself to the drive - whenever the drive electronics are or will be exposed, connect yourself to ground with a wrist strap (see table 2-1). Connection may be made to any metal assembly on the drive. As a general rule, remember that you, the drive, and the circuit boards must all be at ground potential to avoid potentially damaging static discharges.

TABLE 2-1. MAINTENANCE TOOLS AND MATERIALS

Description	Part Number
Programmable Field Test Unit (TB2A3-F with SMD-O option)	CDC 73086307
Field Test Unit (TB216-C) (includes tester and accessories)	CDC 75144002
Oscilloscope, Dual Trace	Tektronix 475A or equivalent
Scope Probe Tip (Hatchet type)	CDC 12212885
Static Shielding Bags and Ground Wrist Straps	See Accessories in Parts Data (Section 4 of Hardware Maintenance, Volume 1)
Volt/ohmmeter	Ballantine 345 or equivalent digital voltmeter
Electromagnet Alignment Tool	CDC 85273100

- Keep boards in conductive bags - when circuit boards are not installed in the drive, keep them in conductive static shielding bags (see table 2-1). These bags provide absolute protection from direct static discharge and from static fields surrounding charged objects. Remember that these bags are conductive and should not be placed where they might cause an electrical short circuit.

- Remove boards from bags only when you are grounded - all boards received from the factory are in static shielding bags, and should not be removed unless you are grounded.

- Turn off power to drive before removing or installing any circuit boards.

- Never use an ohmmeter on any circuit boards, unless directed to in troubleshooting procedures.

MAINTENANCE TOOLS AND MATERIALS

The maintenance procedures described in this manual require the use of certain special tools, test equipment, and materials. These are listed in table 2-1 along with the appropriate CDC part number. Note that the list includes only special tools. It is assumed that the service person has normal maintenance tools.

Use of the items listed in table 2-1 is described in the procedures in which they are required. Additional information is provided on the optional status/control panel (see section 3, Trouble Analysis) and the programmable field test unit (see Testing the Drive).

TESTING THE DRIVE

GENERAL

During testing and troubleshooting the drive is normally required to perform various operations such as reading and writing test data. Either a field test unit or system software can be used to control the drive during these operations.

FIELD TEST UNITS

Either the TB2A3F programmable field test unit (PFTU) or the TB216C field test unit (FTU) are recommended for use with the drive (see table 2-1 for tester part numbers). The tester allows the drive to be operated and controlled independent of the rest of the system. The following outlines the procedure for connecting the tester to the drive. For specific instructions on connecting and operating the tester, see the tester manual.

CAUTION

To avoid possible damage to interface circuitry, always deenergize drive, controller, and tester before removing or installing I/O cables.

During testing, the tester I/O cables must be connected to the drive in place of the system I/O cables. Before disconnecting the system I/O cables, disable the controller and set power supply On/Standby switch to the Standby (0) position. In a daisy chain system, power off all the drives.

When the drive is powered down, remove the system I/O cables from the drive to be tested. Connect the tester A cable to drive connector 1J03 and the tester B cable to drive connector 1J02. Connect a terminator to drive connector 1J04. See the installation section of hardware maintenance volume 1 for the terminator and its part number. In a daisy chain system, make whatever connections are necessary to ensure that the other drives remain under system control, and restore power to the other drives.

At the completion of testing, restore the drive to normal operation by reversing the process outlined above.

DRIVE DIAGNOSTICS

The drive has built in diagnostic tests. These diagnostic tests may be performed via the status/control panel (optional), located behind the drive front panel insert. See section 3, Trouble Analysis for operating instructions.

SYSTEM SOFTWARE

The drive may also be tested by use of system diagnostic test programs. This requires use of the controller and the appropriate software. In this type of testing, the drive communicates with the controller as in normal online operations, and special I/O connections are unnecessary.

Refer to manuals or other documentation applicable to the specific system or subsystem for information concerning the system software routines.

IDENTIFYING TEST POINTS

The drive circuit boards have test points to aid in signal tracing during maintenance and troubleshooting. These test points appear physically as shown on figure 2-1 and may be located anywhere on the component side of the circuit boards.

The diagrams and maintenance procedures identify a test point by referring to a connector. J80-1 is an example of a test point reference, where J80 is the connector and 1 is the pin number. TP-G620 is an example of a test point, where G620 is the coordinate locator. Where there is no test point, a board coordinate is used to locate a chip or other component. The introduction to diagrams section explains how to use the coordinate locators. The connector designators are letters, silkscreened onto the board. The coordinate locators progress in alphabetical order from left to right and top to bottom.

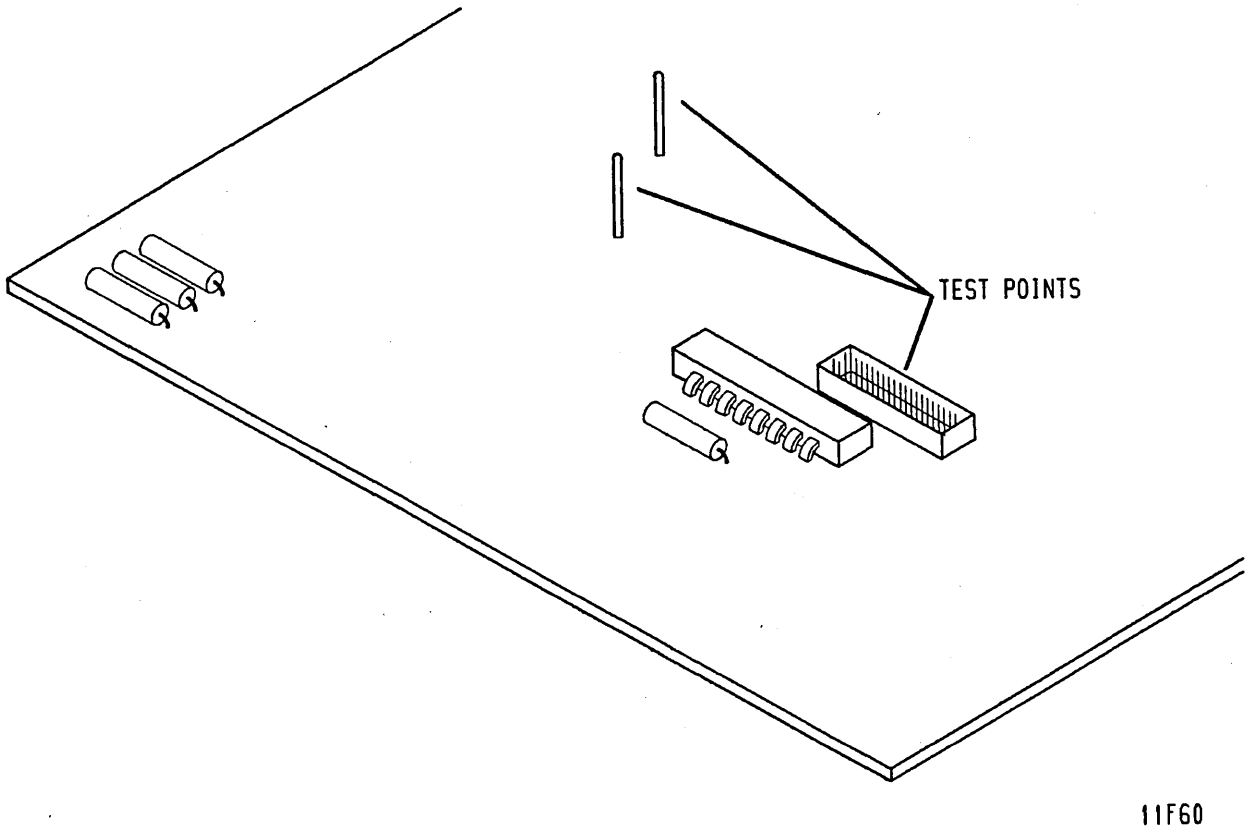


Figure 2-1. Test Points

ACCESSING ASSEMBLIES FOR MAINTENANCE

The major drive assemblies and components are shown on figure 2-2. These parts are accessed by extending the 2X drawer on its slides, sliding the drive outward, and removing the drive top cover.

When extending the 2X drawer and drive, exercise caution to ensure that the equipment rack remains stable. Also, take care that the system cabling is not damaged when sliding the drive in the drawer and the drawer in and out of the rack.

If it is necessary to remove the drive from the drawer, see entire drive removal procedure in section 5 of this manual. Section 5 also contains a top cover removal procedure and procedures for removing most of the other field replaceable parts, including the circuit boards.

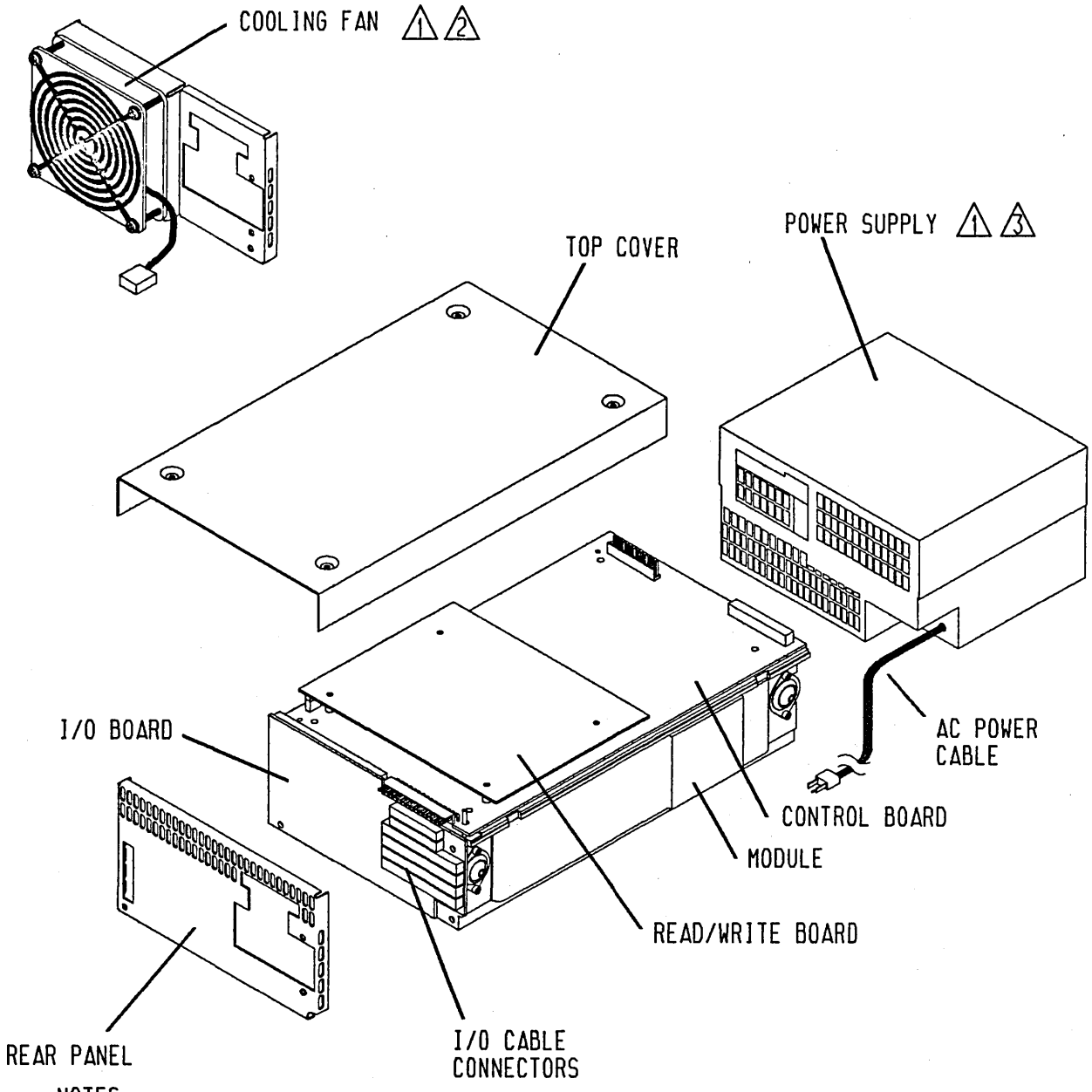


Figure 2-2. Component Locator (Sheet 1 of 4)

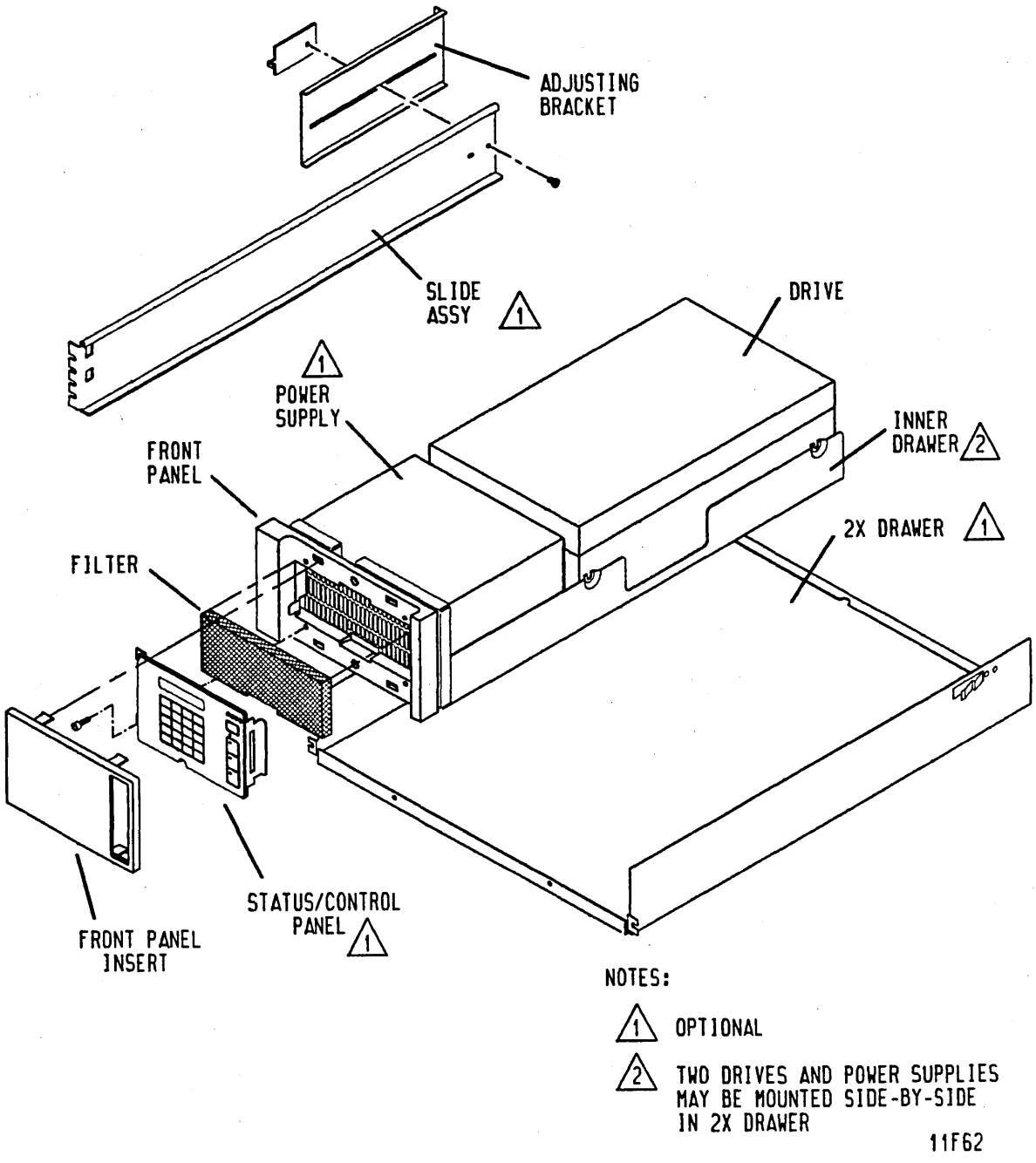
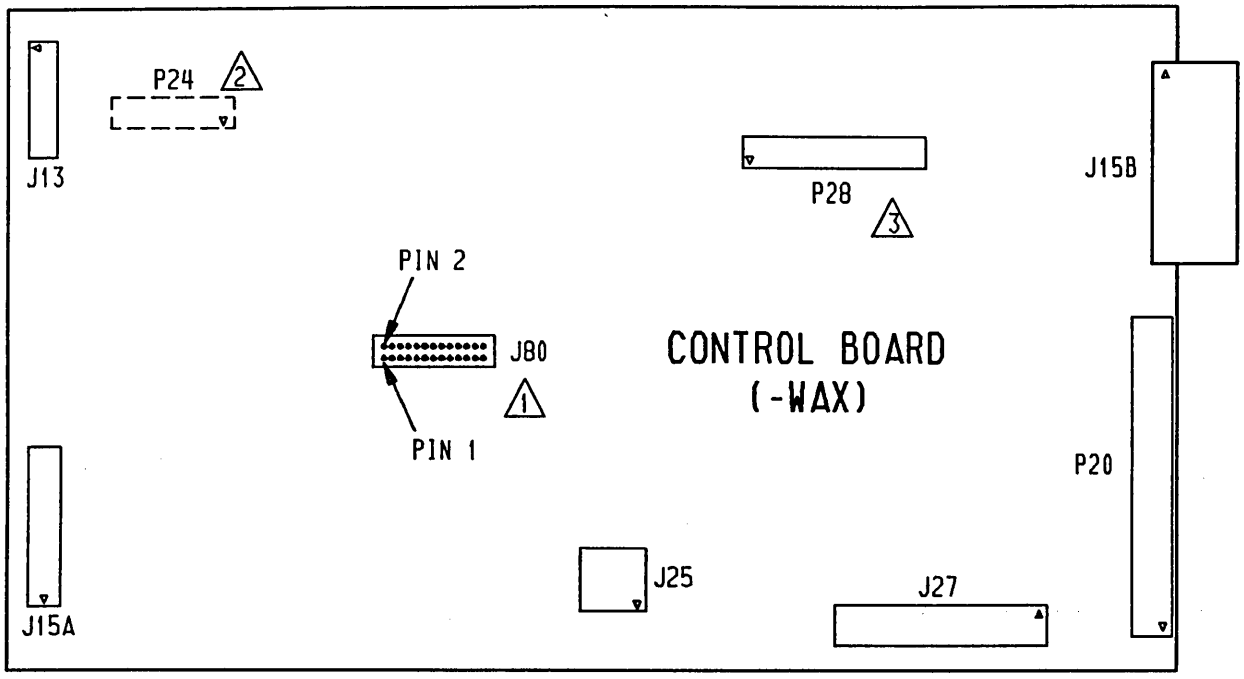
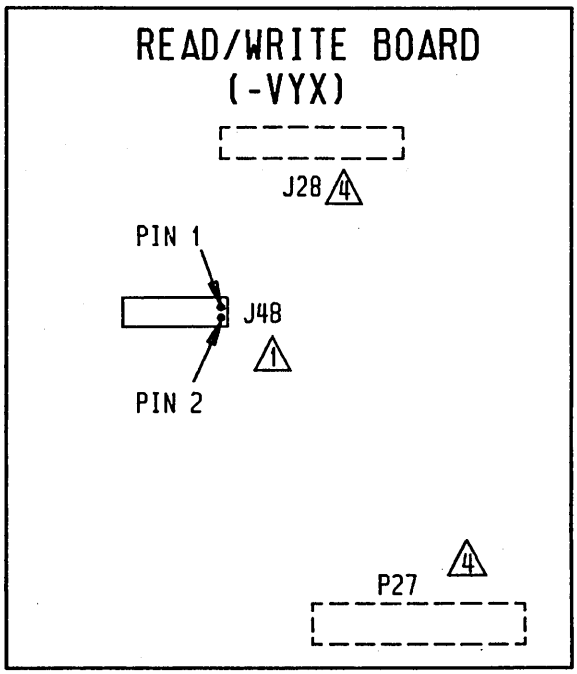


Figure 2-2. Component Locator (Sheet 2)



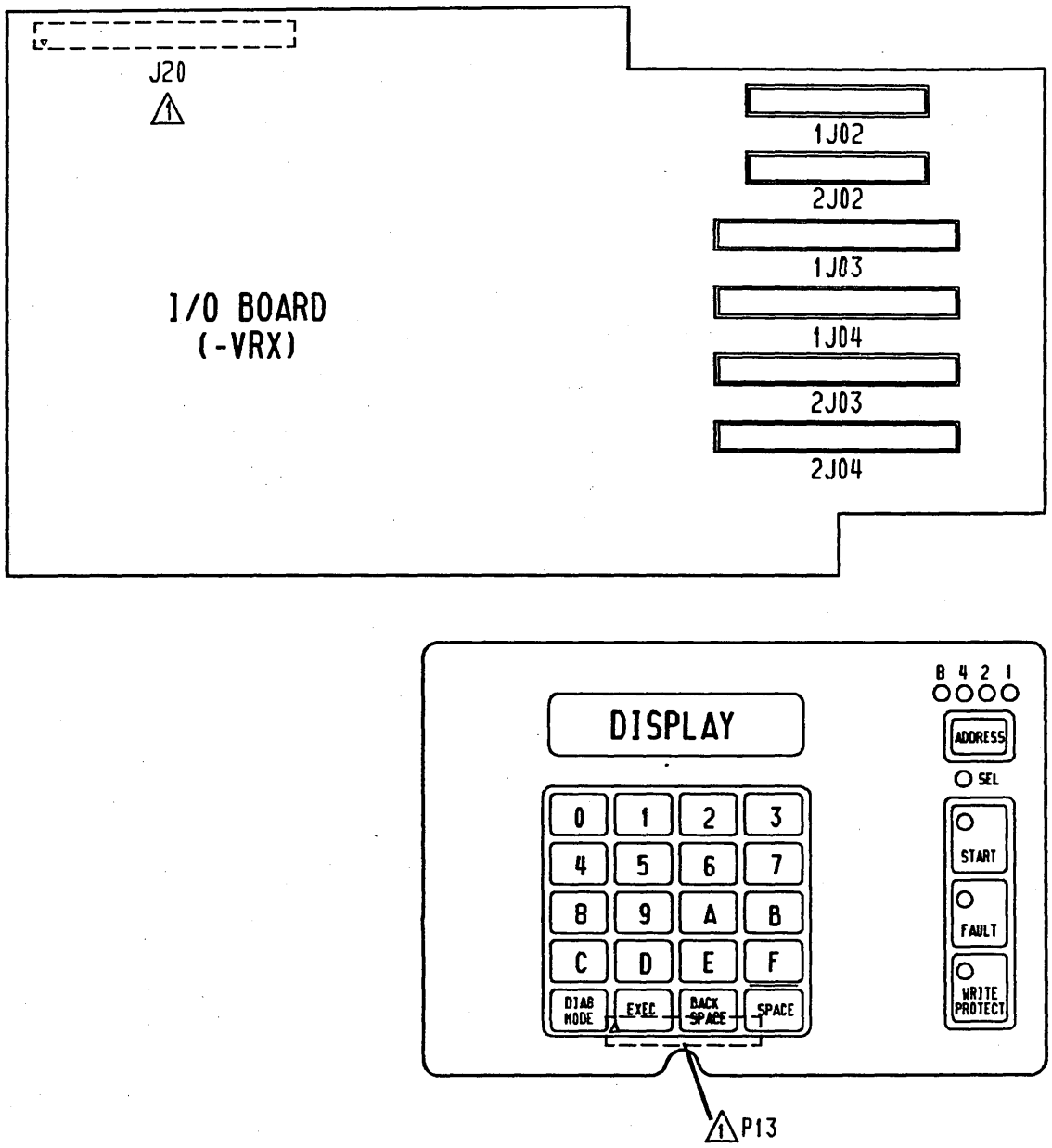
NOTES:

1. TEST POINTS
2. CONNECTS TO MODULE
3. A PORTION OF P28 PROVIDES FEEDTHROUGH CONNECTIONS BETWEEN READ/WRITE BOARD AND MODULE
4. CONNECTS TO CONTROL BOARD
5. △ = LOCATION OF PIN 1



11F63

Figure 2-2. Component Locator (Sheet 3)



STATUS/CONTROL PANEL (OPTIONAL) 2

NOTES:

1 CONNECTS TO CONTROL BOARD

2 MOUNTS TO INNER DRAWER OR REMOTE LOCATION

3 ▵= LOCATION OF PIN 1

11F64

Figure 2-2. Component Locator (Sheet 4)

Extending the drive and removing the top cover allows access to the circuit board test points. As shown on figure 2-2, the I/O board (_VRX), read/write board (_VYX), and control board (_WAX) are readily accessible. The arm matrix board (_WBX) is located within the module and cannot be serviced.

The power supply (see figure 2-2) can be attached to the inner drawer (directly in front of the drive) or mounted in a remote location, provided clearance for proper air flow is available.

When the power supply is mounted in the 2X drawer (in line with the drive), drive cooling is provided by the fan in the power supply. When the power supply is mounted in a remote location, drive cooling is provided by a fan and bracket assembly that mounts to the I/O board.

The status/control panel (optional) mounts to the front panel. It provides the user with operator controls and a diagnostic keyboard and display. Removing the front panel insert allows access to the diagnostic keyboard and display.

SECTION 3

TROUBLE ANALYSIS

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

The trouble analysis section contains information on isolating and correcting problems causing improper drive operation. Persons performing troubleshooting should be thoroughly familiar with drive operation and with all information in the general maintenance section of this manual (particularly the warnings and precautions).

Because of the many types of malfunctions that may occur, the information in this section will not provide a solution to every problem. The intention, therefore, is to solve common problems and to provide a starting point for the rest. The final recommendation in all cases is to call field support.

For trouble analysis, a status/control panel is needed. If the drive installation does not include a status/control panel, we advise that you connect one to the drive during troubleshooting.

Trouble analysis information is divided into two parts:

- Power Up Test
- Troubleshooting Procedures
- Diagnostic/Drive Operating Status Codes

The power up test describes drive self tests that occur when dc power is applied to the drive. It also lists what corrective actions to take if a test failure occurs. The troubleshooting procedures describe how to isolate and correct common drive problems. The procedures cover all the major areas of drive operation: power, servo, read and write. Diagnostic testing is used to determine which major drive assembly has failed. The drive operating status codes provide information on correcting problems associated with drive power-up/power-down and servo status (provided by the Control MPU).

Many of the corrective actions in this section refer to procedures given in section 4, Electrical Checks and section 5, Repair and Replacement. All procedures are referred to by number. For example, a reference to procedure 4101 refers to 4101 - Power Check in section 4. The first digit always indicates the section (4 or 5) where the procedure is found.

POWER UP TEST

When dc power is applied to the drive, the Control MPU performs a series of self tests. During these tests the Address, Ready, FAULT, and WRITE PROTECT lights on the status/control panel will be lit. After approximately four seconds, the FAULT light will go off; indicating successful completion of the self tests. If the Ready and FAULT lights remain on constantly, it indicates the drive failed the power up self test. The Address lights will then indicate which self test routine the drive failed to complete. Refer to table 3-1 to determine which test failed and what action to take.

TROUBLESHOOTING PROCEDURES

The troubleshooting procedures describe how to isolate and correct common drive problems. Figure 3-1 is an example of a troubleshooting procedure and explains the format. The following paragraphs explain how to use the troubleshooting procedures.

Before starting a procedure, ensure that all assumptions have been satisfied. The assumptions along with other advisory information is given in the introductory paragraph to the procedure and describe conditions that must exist for the procedure to be valid.

When the assumptions are satisfied, proceed to the first step of the procedure. After performing the action or answering the question, follow the line down to the next step. For a question, follow the line beneath the appropriate Y (yes) or N (no) response. Continue until a corrective action is reached.

After taking the first recommended action, retest the unit. If the test results do not change, try recommended action 2, and so on, being sure to retest after each action. The corrective actions which are easier to perform (checking a signal or changing a circuit board, for example) are listed before the more difficult tasks such as replacing the module. If the corrective actions do not solve the problem, call field support.

TABLE 3-1. POWER UP TEST FAILURE

Address Lights* 8 4 2 1	Hex Code	Test Failed** & Actions
● ● ● ●	F	RAM Test Action: 1. Replace control board.
● ● ● o	E	ROM Test Action: 1. Replace control board.
● ● o ●	D	I/O Chip Test Actions: 1. Replace I/O board. 2. Replace control board.
● ● o o	C	Peripheral Chip (Test 1) Action: 1. Replace control board.
● o ● ●	B	Peripheral Chip (Test 2) Action: 1. Replace control board.
● o ● o	A	Motor MPU Test Action: 1. Replace control board.

* Darkened circles indicate light is On.
**Ready and FAULT lights remain on constantly, indicating drive failed four second power up self test.

The procedures appear in the following order:

- TSP1 - Power Check: Isolates problems in the drive related to short circuits.
- TSP2 - Voltage Fault Check: Isolates problems in the drive related to dc power failures.
- TSP3 - First Seek Check: Provides possible causes for the drive failing to successfully complete a first seek.
- TSP4 - Seek Check: Provides possible causes for the drive failing to successfully complete a seek.
- TSP5 - Write Check: Provides information for isolating cause of write errors.
- TSP6 - Read Check: Provides information for isolating cause of read errors.
- TSP7 - Address Mark Check: Provides possible causes for read or write address mark problems.

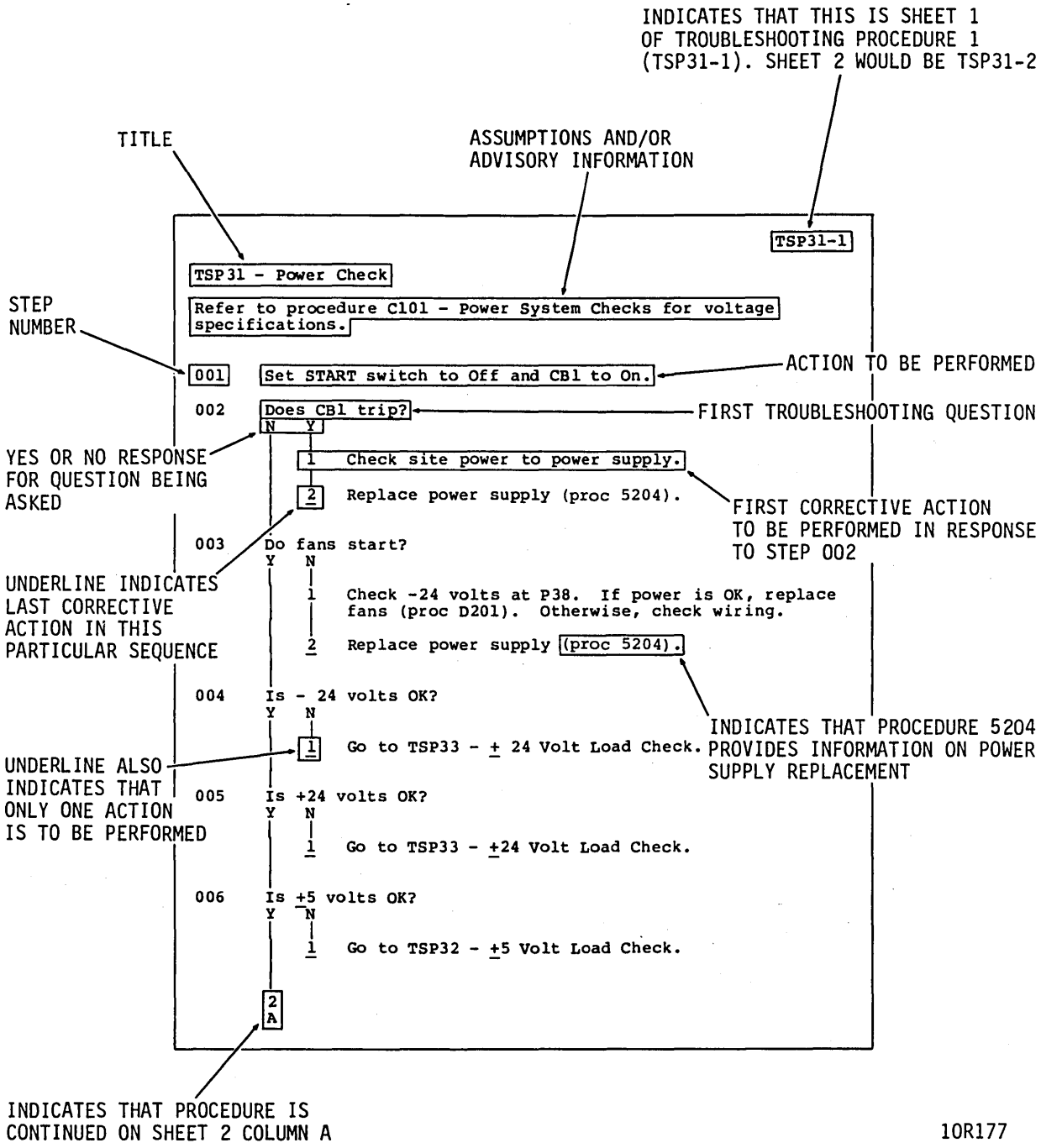


Figure 3-1. Example of Troubleshooting Procedure

TSP1 - Power Check

This procedure isolates problems in the drive or power supply related to short circuits. Refer to procedure 4101 - Power Checks for voltage specifications.

001 Apply ac power and set power supply On/Standby switch to On (1).

↓

002 Does fan in power supply start?

N Y

N: ↓

Y: ↓

003 No short circuit exists. Power check is OK.

004 Set power supply On/Standby switch to Standby (0) and remove ac power cord from site power source.

↓

005 Check for short circuits between the dc voltages and to ground at the following locations:

- +5 volts: J15-1
- -5 volts: J15-5
- -12 volts: J15-7
- +24 volts: J15-12
- Ground: J15-3

↓

006 Do any short circuits exist?

Y N

Y: ↓

1 Inspect dc power cable (P15) between power supply and drive, for open ±5 volt sense lines (J15-2, J15-4, J15-6).

↓

2 Replace power supply (proc 5203).

N: ↓

007 Inspect dc power cable (P15) between power supply and drive. If cable is OK, disconnect dc power cable from drive and recheck for short circuits at J15 on control board.

↓

2

A

A
1
↓

008 Do any short circuits exist?

Y | N
| ↓
| 1 Replace power supply (proc 5203).
↓

009 Disconnect status/control jumper cable from J13 (control board).
↓

010 Do any short circuits exist at J15 on control board?

Y | N
| ↓
| 1 Replace status/control panel (proc 5202).
↓

011 Disconnect P25 from J25 (control board).
↓

012 Do any short circuits exist at J15 on control board?

Y | N
| ↓
| 1 Inspect P25 cable from carriage latch electromagnet.
| ↓
| 2 Replace carriage latch electromagnet (proc 5205).
↓

013 Remove read/write board (proc 5301).
↓

014 Do any short circuits exist?

Y | N
| ↓
| 1 Replace read/write board (proc 5301).
↓

015 Remove I/O board (proc 5302).
↓
3
A

A
2
↓

016 Do any short circuits exist?

Y | N
| ↓
| 1 Replace I/O board (proc 5302).
↓

017 Remove control board (proc 5303).

↓

018 Do any short circuits exist at J15 on control board?

N | Y
| ↓
| 1 Replace control board (proc 5303).
↓

019 1 Replace module (proc 5204).

TSP2 - Voltage Fault Check

This procedure isolates problems in the drive or power supply, related to dc power failures.

001 Apply ac power and set power supply On/Standby switch to On (1).

↓

002 Does a voltage fault exist? See status/control panel or check if J80-11 -(Voltage Fault) is active (low).

Y → 003 No voltage fault exists. Voltage fault check is OK.

N ↓

004 Check dc voltages at the following locations. Refer to procedure 4101 - Power Checks, for voltage specifications.

- +5 volts: J80-20
- -5 volts: J80-22
- -12 volts: J80-23
- +12 volts: J80-21
- Ground: J80-9

↓

005 Are dc voltages OK?

N → 006 Is voltage fault intermittent?

N → 1 Replace I/O board (proc 5302).

↓

2 Replace control board (proc 5303).

Y → 1 Replace control board (proc 5303).

↓

2 Replace I/O board (proc 5302).

↓

007 Is -12 volts OK?

Y → 008 Set power supply On/Standby switch to Standby (0) and disconnect ac power cord from site power source.

↓

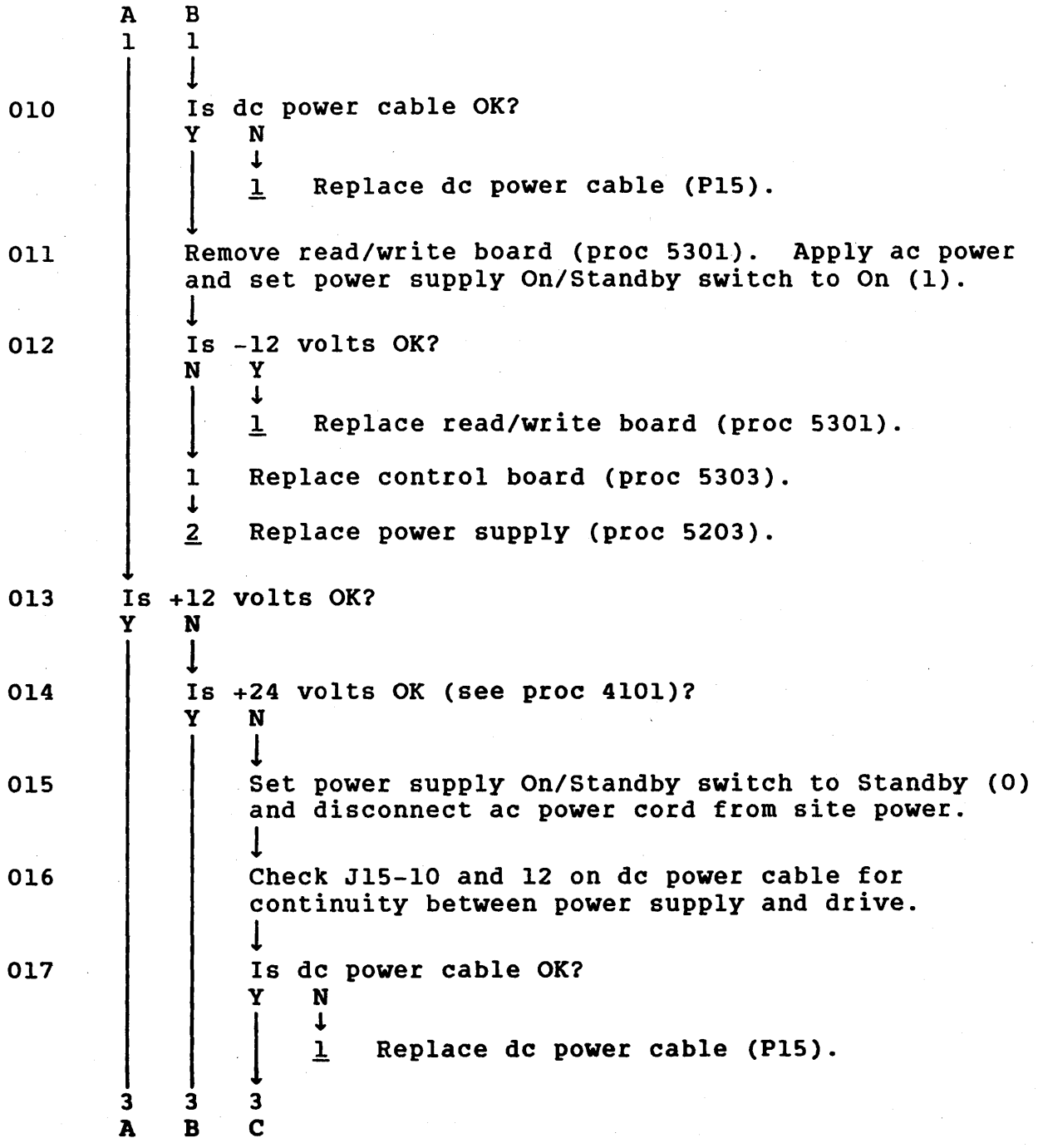
009 Check J15-7 on dc power cable for continuity between power supply and drive.

↓

2 A

N ↓

2 B


A
B
1
1
010
Is dc power cable OK?
Y
N
1 Replace dc power cable (P15).
011
Remove read/write board (proc 5301). Apply ac power and set power supply On/Standby switch to On (1).
012
Is -12 volts OK?
N
Y
1 Replace read/write board (proc 5301).
1 Replace control board (proc 5303).
2 Replace power supply (proc 5203).
013
Is +12 volts OK?
Y
N
014
Is +24 volts OK (see proc 4101)?
Y
N
015
Set power supply On/Standby switch to Standby (0) and disconnect ac power cord from site power.
016
Check J15-10 and 12 on dc power cable for continuity between power supply and drive.
017
Is dc power cable OK?
Y
N
1 Replace dc power cable (P15).
3
3
3
A
B
C

```
        A   B   C
        2   2   2
        |   |   ↓
018     |   |   Disconnect P25 from J25 (control board).
        |   |   Check control board for a short circuit (0 ohms)
        |   |   in both directions between J25-3 and ground and
        |   |   J25-1 and J15-12 (+24 volts).
        |   |   ↓
019     |   |   Does a short circuit exist?
        |   |   N   Y
        |   |   |   ↓
        |   |   |   1   Replace control board (proc 5303).
        |   |   ↓
020     |   |   Apply ac power and set power supply On/Standby
        |   |   switch to On (1).
        |   |   ↓
021     |   |   Is +24 volts OK?
        |   |   N   Y
        |   |   |   ↓
        |   |   |   1   Replace carriage latch electromagnet
        |   |   |       (proc 5205).
        |   |   ↓
        |   |   1   Replace control board (proc 5303).
        |   |   ↓
        |   |   2   Replace power supply (proc 5203).
        |   |   ↓
        |   |   3   Replace module (proc 5204).
        |   ↓
022     |   Disconnect status/control jumper cable from J13
        |   (control board).
        |   ↓
023     |   Is +12 volts OK?
        |   N   Y
        |   |   ↓
        |   |   1   Replace status/control panel
        |   |       (proc 5202).
        |   ↓
024     |   Remove read/write board (proc 5301).
        |   ↓
025     |   Is +12 volts OK?
        |   N   Y
        |   |   ↓
        |   |   1   Replace read/write board (proc 5301).
        |   ↓
        |   1   Replace control board (proc 5303).
        ↓
        4
        A
```

```
        A
        3
        |
        v
026     Is -5 volts OK?
        Y   N
        |   |
        |   v
027     |   Set power supply On/Standby switch to Standby (0) and
        |   disconnect ac power cord from site power source.
        |   |
        |   v
028     |   Check J15-5 and 6 on dc power cable for continuity
        |   between power supply and drive.
        |   |
        |   v
029     |   Is dc power cable OK?
        |   Y   N
        |   |   v
        |   |   1   Replace dc power cable (P15).
        |   |
        |   v
030     |   Remove read/write board (proc 5301).  Apply ac power
        |   and set power supply On/Standby switch to On (1).
        |   |
        |   v
031     |   Is -5 volts OK?
        |   N   Y
        |   |   v
        |   |   1   Replace read/write board (proc 5301).
        |   |
        |   v
        |   1   Replace I/O board (proc 5302).
        |   v
        |   2   Replace control board (proc 5303).
        |   v
        |   3   Replace power supply (proc 5203).
        |
        v
032     Is +5 volts OK?
        Y   N
        |   |
        |   v
033     |   Set power supply On/Standby switch to Standby (0) and
        |   disconnect ac power cord from site power.
        |   |   |
        v   v   v
        5   5
        A   B
```

```
      A   B
      4   4
          |
          ↓
034       Check J15-1 and 2 on dc power cable for continuity
          between power supply and drive.
          |
          ↓
035       Is dc power cable OK?
          Y   N
          |   ↓
          |   1   Replace dc power cable (P15).
          |
          ↓
036       Disconnect P25 from J25 (control board).  Apply dc
          power and set power supply On/Standby switch to
          On (1).
          |
          ↓
037       Is +5 volts OK?
          N   Y
          |   ↓
          |   1   Replace carriage latch electromagnet
          |       (proc 5205).
          |
          ↓
038       Disconnect status/control jumper cable from J13
          (control board).
          |
          ↓
039       Is +5 volts OK?
          N   Y
          |   ↓
          |   1   Replace status/control panel
          |       (proc 5202).
          |
          ↓
040       Remove read/write board (proc 5301).
          |
          ↓
041       Is +5 volts OK?
          N   Y
          |   ↓
          |   1   Replace read/write board (proc 5301).
          |
          ↓
          1   Replace I/O board (proc 5302).
          ↓
          2   Replace control board (proc 5303).
          ↓
          3   Replace power supply (proc 5203).
          ↓
          4   Replace module (proc 5204).
          |
          ↓
042   Voltage Fault Check is OK.  If problem persists, call
      field support.
```

TSP3 - First Seek Check

This test assumes that the status/control panel is connected to the drive.

001 Initiate first seek as follows:

a. Set Remote/Local switch to Local.

b. Apply power to drive.

c. Press START switch on status/control panel. After power up delay is completed, observe rapid blinking of Ready indicator (indicating spindle power up is in progress).

002 Does Ready indicator light steadily?

N Y

003 Drive has successfully completed first seek.

004 Is FAULT indicator on?

N Y

1 Check status/control panel for type of fault and perform corrective actions as indicated in diagnostic status code table (in this section).

1 Replace control board (proc 5303). If problem persists, call field support.

TSP4 - Seek Check

This test assumes that the following conditions exist: (1) drive is operating under control of the FTU and (2) first seek was successfully completed.

001 Does FAULT indicator light?
N Y

002 Check status/control panel for type of fault and perform corrective actions as indicated in diagnostic status code table (in this section).

003 Is Seek Error active?
N Y

004 Perform the following electrical checks (found in section 4):

- 4201 - Position Signal Check
- 4202 - On Cylinder Check
- 4203 - One Track Scan
- 4204 - Cylinder Address Bit Check

005 Does drive fail Cylinder Address Bit Check (proc 4204)?
N Y

1 Replace I/O board (proc 5302).

2 Replace control board (proc 5303).

006 Is problem related to seek length?
N Y

1 Replace control board (proc 5303).

2 Replace module (proc 5204).

007 Does seek error occur at or near the same cylinder?
N Y

1 Replace module (proc 5204).

008 If problem persists, call field support.

009 Seek Check is OK.

TSP5 - Write Check

This check assumes that the drive is performing write or write format operations under control of the FTU. If a fault occurs during testing, observe the status display window (on status/control panel) for type of fault present.

001 Does a Voltage Fault exist?
N Y
↓
1 Power problem. Go to TSP2.

002 Does a Write and Write Protect fault exist?
N Y
↓

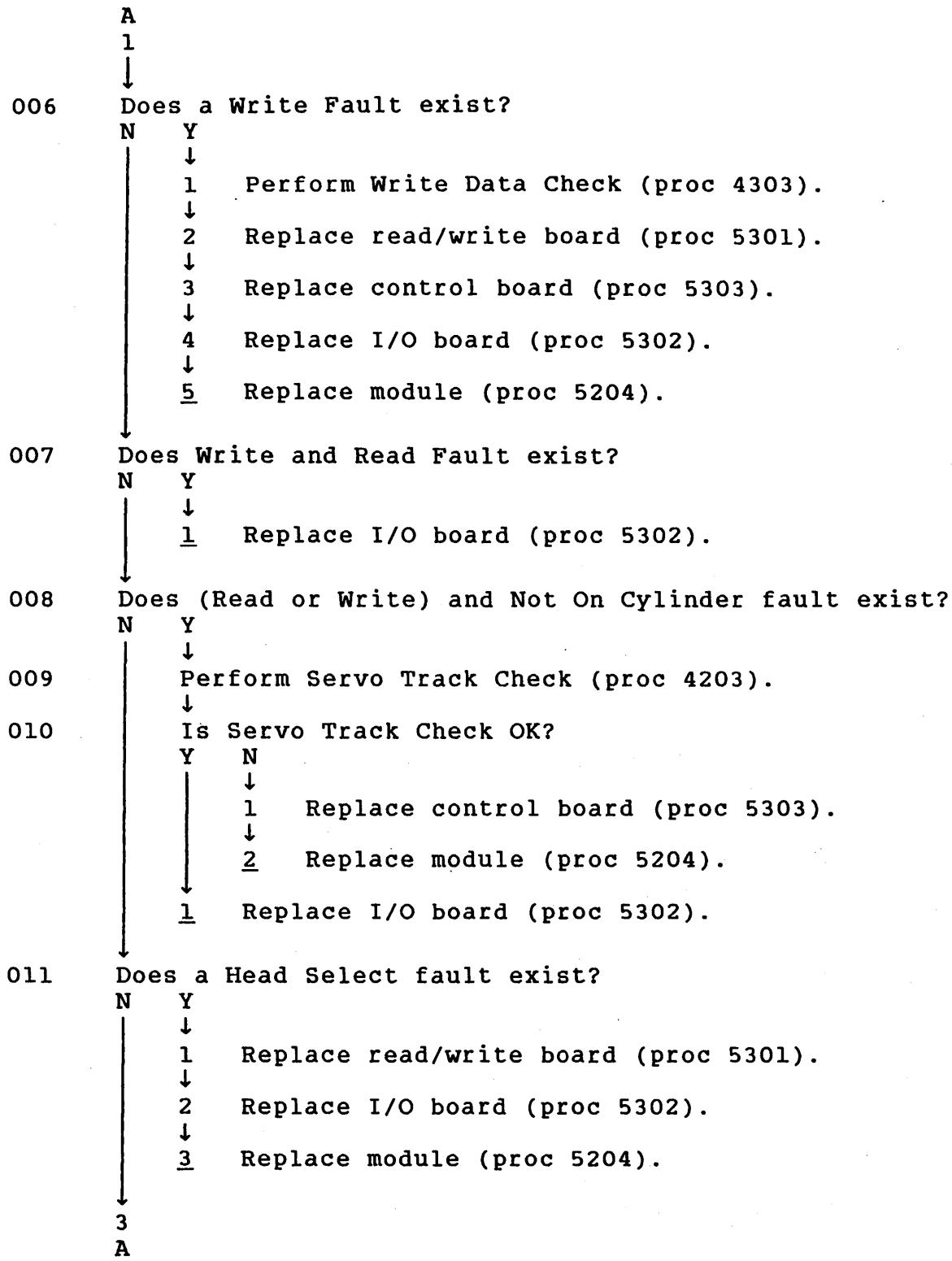
003 Is Write Protect switch (on control board) set to Off?
Y N
↓
1 Set Write Protect switch to Off.

004 Is Write Protect switch on status/control panel set to Off?
Y N
↓
1 Set Write Protect switch to Off.

005 Is motor speed OK (check motor status)?
Y N
↓
1 Replace control board (proc 5303).
↓
2 Replace module (proc 5204).

1 Replace I/O board (proc 5302).
↓
2 Replace control board (proc 5303).

2
A


A
1
006 Does a Write Fault exist?
N Y
1 Perform Write Data Check (proc 4303).
2 Replace read/write board (proc 5301).
3 Replace control board (proc 5303).
4 Replace I/O board (proc 5302).
5 Replace module (proc 5204).
007 Does Write and Read Fault exist?
N Y
1 Replace I/O board (proc 5302).
008 Does (Read or Write) and Not On Cylinder fault exist?
N Y
009 Perform Servo Track Check (proc 4203).
010 Is Servo Track Check OK?
Y N
1 Replace control board (proc 5303).
2 Replace module (proc 5204).
1 Replace I/O board (proc 5302).
011 Does a Head Select fault exist?
N Y
1 Replace read/write board (proc 5301).
2 Replace I/O board (proc 5302).
3 Replace module (proc 5204).
3
A

A
2
↓

012 Are Index and Sector pulses OK?

Y N
| ↓
| 1 Replace control board (proc 5303).
↓

013 Perform Write PLO Check (proc 4302).

↓

014 Is Write PLO Check OK?

Y N
| ↓
| 1 Replace read/write board (proc 5301).
| ↓
| 2 Replace control board (proc 5303).
| ↓
| 3 Replace module (proc 5204).
↓

015 Perform Write Data Check (proc 4303).

↓

016 Are Write Data (NRZ), Write Clock (14.5 MHz), and Write Gate OK?

Y N
| ↓
| 1 Replace control board (proc 5303).
↓

017 Is write data (going to head arm preamp) OK?

Y N
| ↓
018 | Is Write Enable present?
| Y N
| | ↓
| | 1 Replace read/write board (proc 5301).
| | ↓
| | 2 Replace control board (proc 5303).
| ↓
019 | Is Compensated Write Data OK?
| Y N
| | ↓
| | 1 Replace read/write board (proc 5301).
| ↓
| 1 Replace module (proc 5204).
↓

020 Write Check is OK. If problem persists, call field support.

TSP6 - Read Check

This check assumes that the drive is performing read operations under control of the FTU. If a fault occurs during testing, observe the status display window (on status/control panel) for type of fault present.

001 Does a Voltage Fault exist?

N Y

↓

1 Power problem. Go to TSP2.

002 Does Write and Read Fault exist?

N Y

↓

1 Replace I/O board (proc 5302).

003 Does (Read or Write) and Not On Cylinder fault exist?

N Y

↓

1 Servo problem. See TSP2.

004 Is Read Gate active?

Y N

↓

1 Replace I/O board (proc 5302).

005 Perform Read PLO Check (proc 4401).

↓

006 Is Read PLO Check OK?

Y N

↓

1 Replace read/write board (proc 5301).

↓

2 Replace control board (proc 5303).

↓

3 Replace I/O board (proc 5302).

↓

4 Replace module (proc 5204).

↓

2

A

```
        A
        1
        |
        ↓
007     Perform Read Data Check (proc 4402).
        |
        ↓
008     Is Latched Read Data OK?
        Y   N
        |   ↓
        |   1   Replace read/write board (proc 5301).
        |   ↓
        |   2   Replace control board (proc 5303).
        |   ↓
        |   3   Replace module (proc 5204).
        |
        ↓
009     Is NRZ Read Data OK?
        Y   N
        |   ↓
        |   1   Replace read/write board (proc 5301).
        |
        ↓
010     Is Address Mark OK?
        Y   N
        |   ↓
        |   1   Perform procedure 4403 - Read AM Check and go
        |       to TSP7.
        |
        ↓
011     Is there a data error?
        Y   N
        |   ↓
        |   1   Read operation is OK.
        |
        ↓
012     Are errors head related?
        N   Y
        |   ↓
        |   1   Replace read/write board (proc 5301).
        |   ↓
        |   2   Replace I/O board (proc 5302).
        |   ↓
        |   3   Replace module (proc 5204).
        |
        ↓
013     1   Replace module (proc 5204).  If problem persists,
            call field support.
```

TSP7 - Address Mark Check

The following check assumes that the drive is under control of the FTU.

001 Perform procedure 4403 - Read AM Check.

002 Is AM Enable active?

- N
  - 1 Replace I/O board (proc 5302).
  - 2 Replace read/write board (proc 5301).

003 Is AM Found active?

- N
  - 1 Replace read/write board (proc 5301).

004 Is AM proper length?

- N

005 Perform procedure 4304 - Write AM Check.

006 Is AM Enable active?

- N
  - 1 Replace I/O board (proc 5302).
  - 2 Replace read/write board (proc 5301).

007 Are there double frequency pulses during AM?

- N
  - 1 Replace read/write board (proc 5301).

008 Write AM Check OK. If problem persists, call field support.

009 Is lock to data timing OK?

- N
  - 1 Replace read/write board (proc 5301).

010 Read AM Check OK. If problem persists, call field support.

DIAGNOSTIC/DRIVE STATUS CODES

Information on diagnostic and drive status codes was not available at the time of printing. It will be included in the next revision of this manual.

DRIVE STATUS CODES AND DIAGNOSTIC TESTING

GENERAL

The drive status codes (displayed on the status/control panel) are two digit hexadecimal codes, generated by the Control MPU, that indicate operational status of the drive. In addition to displaying drive status, the status/control panel also provides a means for diagnostic testing. The following discussions explain how to perform diagnostic tests and define various drive status codes.

DIAGNOSTIC TESTING

General

This section describes the steps required to execute the off-line diagnostics provided with the drive. These tests are initiated and monitored via the keyboard and LCD (liquid crystal display) of the status/control panel (see figure 3-2). Table 3-2 describes the function of the switches and indicators.

Test Selection Procedure

Pressing the Diagnostic Mode switch will cause the display to be cleared and a message ("DIAG TEST XX") will be displayed. To enter a particular test, the operator must use the hexadecimal switches on the status/control panel. To select a test requires the input of two hexadecimal characters. In the event that the operator enters an incorrect character, the Back Space switch can be used to return to the previous position and the proper character can now be input. Once the operator has entered the desired test, pressing the Execute switch will start the test. The Liquid Crystal Display (LCD) will display some message, indicating that either the test is running or has completed. Pressing the Execute switch again will end the test and return to the diagnostic monitor, allowing another test to be entered. To end diagnostic testing, press the Diagnostic Mode switch. Drive operating status will then be displayed.

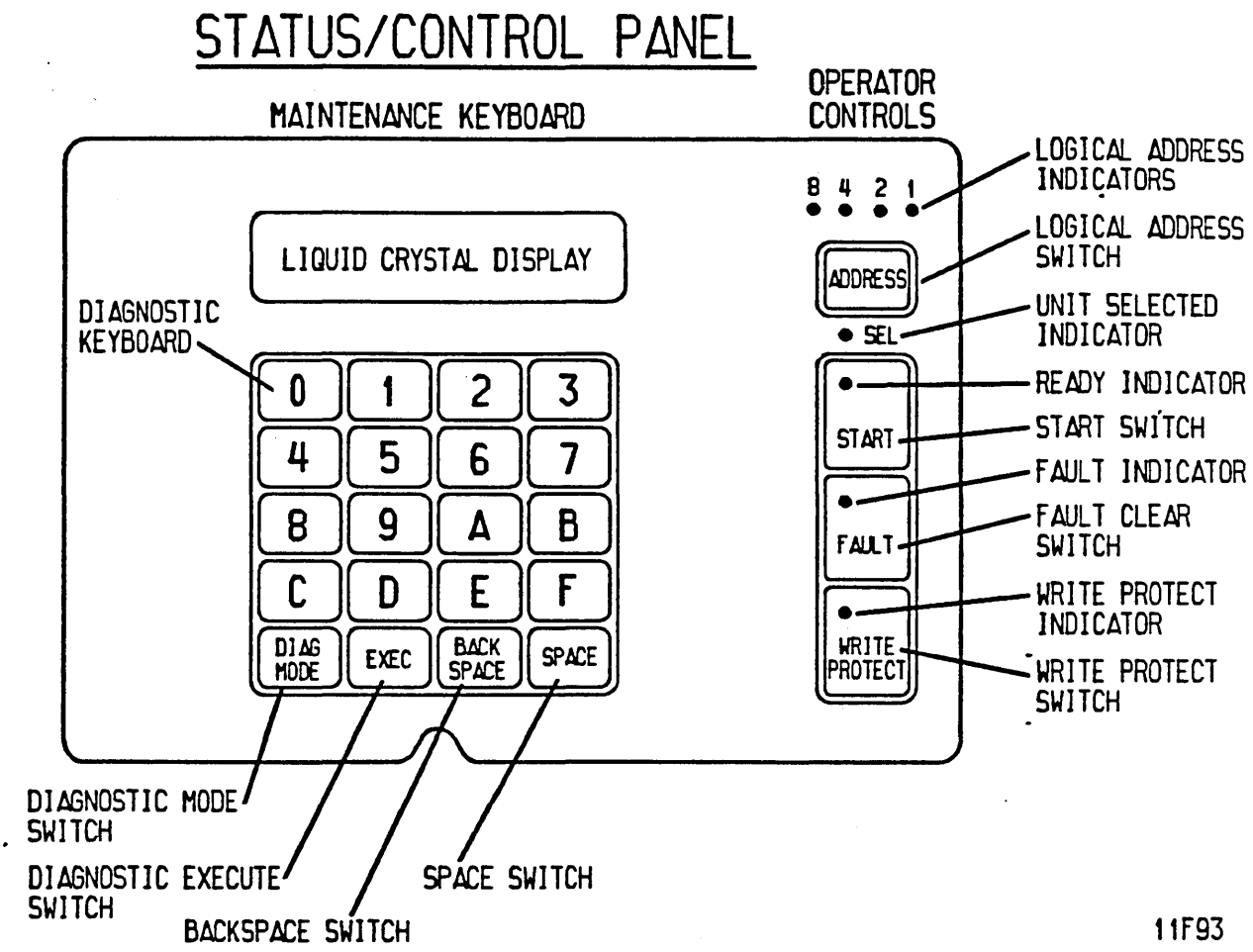


Figure 3-2. Switches and Indicators

TABLE 3-2. SWITCH/INDICATOR DESCRIPTIONS

Description	Function
Diagnostic Mode Switch (DIAG MODE)	Pressing the Diagnostic Mode switch places the unit in diagnostic mode and disables the interface. The LCD (liquid crystal display) will indicate that the drive is now in the diagnostic test mode. Pressing the Diagnostic Mode switch again will take the drive out of the diagnostic mode, initiate an RTZ seek, and enable the interface.
Diagnostic Execute Switch (EXEC)	Used to begin and end execution of a selected diagnostic test.
Back Space Switch (BACK SPACE)	Allows the operator to back space to correct a character, entered during diagnostic test selection or when selecting a cylinder during seek operations.
Space Switch (SPACE)	Used to step through portions of a test.
Hexadecimal Switches (A-F)	Used to enter test selection or additional parameters.

Test Descriptions

The individual diagnostic tests are listed in table 3-3 and are described in the following topics.

Do not attempt to enter any test numbers that are not listed in table 3-3. Doing so will result in invalid test information.

TABLE 3-3. SUMMARY OF DIAGNOSTIC TESTS

Test Number	Title
00	Display Drive Operating Status Log
01	Display Fault Log
04	Calculate Three Most Likely Field Replaceable Units
05	Servo Test
06	Clear Drive Operating Status Log
07	Clear Fault Log
08	Direct Or Continuous Seeks
09	Random Seek
0C	Display EPROM Part Number
0E	Return To Zero

Test 00 -- Display Drive Operating Status Log

This test displays the 8 most recently generated drive status codes. After test selection, the display provides a hexadecimal status code from the internal log. To execute test 00, perform the following steps:

1. Enter Test 00, then press EXEC switch. The LCD will display "DRIVE LOG XX".

2. Press SPACE switch until a code appears, preceded by an asterisk. This indicates the most recent code stored in the status log.

3. Use the SPACE switch to step through from the 8th most recent to the most recent status.

4. Press EXEC switch to end the test and return to test selection.

Test 01 -- Display Fault Log

This test displays the 8 most recently stored fault codes. After test selection, a hexadecimal fault code will be displayed. To execute test 01, perform the following steps:

1. Enter Test 01, then press EXEC switch. The LCD will display "FAULT LOG XX".

2. Press SPACE switch until a code appears, preceded by an asterisk. This indicates the most recent code stored in the fault log.

3. Use the SPACE switch to step through from the 8th most recent to the most recent fault.

4. If more than one fault occurs simultaneously (multiple faults), calculate the byte count to determine which faults occurred.

The definition of each bit within the fault byte is as follows:

Bit		Definition
0	(LSB)	Read·Write Fault (01)
1		(Read+Write)·Off Cylinder Fault (02)
2		First Seek Fault (04)
3		Write Fault (08)
4		Write·Write Protected Fault (10)
5		Head Select Fault (20)
6		Voltage Fault (40)
7	(MSB)	Not Used (80)

5. Press EXEC switch to end the test and return to test selection.

Test 04 -- Calculate Three Most Likely Field Replaceable Units

NOTE

Do not execute Tests 05, 06, or 07 prior to running Test 04.

This test uses the fault status and the drive operating status history (Tests 00 and 01) to predict the most likely cause of drive failure. Table 3-4 lists the individual codes and their corresponding replacement part. To execute Test 04, perform the following steps:

1. Enter Test 04, then press EXEC switch. The LCD will display "FRUS: XX XX XX". Upon test completion, the three field replaceable units will be displayed, with the first hexadecimal code being the most likely cause of the failure.

2. Press EXEC switch to end the test and return to test selection.

TABLE 3-4. CODING OF FIELD REPLACEABLE UNITS

Hex Display	Field Replaceable Unit
01	Control Board
02	Module
03	Power Supply
04	I/O Board
05	Read/Write Board
06	Carriage Latch Electromagnet
07	Cooling Fan
08	Status/Control Panel

Test 05 -- Servo Test

This test clears both the drive status log and fault Log. Test 05 automatically performs several types of seek operations. They are as follows:

Operation	Number Of Times Executed
RTZ	1
1 Track Seek	16
RTZ	1
Partial Servo Recalibrate	1
RTZ	1
Maximum Length Seek	16
RTZ	1

Execution stops when an error is detected or the test completes. To execute Test 05, perform the following steps:

1. Enter Test 05, then press EXEC switch. Upon successful completion of the test, the LCD will display "OK, CYL: 000". If an error occurs, the LCD will display "SVO ERR: XX". Drive status codes (SVO ERR) are defined in a table at the end of this section.

2. Press EXEC switch to end the test and return to test selection.

Test 06 -- Clear Drive Operating Status Log

This test clears the drive status log resident in program RAM. To execute Test 06, perform the following steps:

1. Enter Test 06 and press EXEC switch. The LCD will display "D LOG CLR".

2. Press EXEC switch to end the test and return to test selection.

Test 07 -- Clear Fault Log

This test clears the fault log. To execute Test 07, perform the following steps:

1. Enter Test 07 and press EXEC switch. The LCD will display "F LOG CLR".

2. Press EXEC switch to end the test and return to test selection.

Test 08 -- Direct Or Continuous Seeks

This test performs direct or continuous seeks between cylinders 0 and the desired cylinder address. The operation is terminated if an error occurs or if the Execute switch is pressed. To execute Test 08, perform the following steps:

1. Enter Test 08 and press EXEC switch.

2. The display "HEX CYL: XXX" asks you to supply a valid destination address (between 0 and 4C0). Enter three characters and press SPACE switch.

3. The display "D OR C ?" asks you to select either direct (D) or continuous (C) seeks. Enter either "C" or "D" and press EXEC switch.

4. If "D" was entered and the direct seek was successful, the LCD will display "OK, CYL: XXX", where "XXX" is the destination address previously entered. Press EXEC switch to end the test and return to test selection.

5. If either "D" or "C" was entered and an error occurs, the LCD will display "SVO ERR: XX". Drive status codes (SVO ERR) are defined in a table at the end of this section.

6. If "C" was entered, press EXEC switch to end the test and return to test selection.

Test 09 -- Random Seek

This test performs random seeks between cylinders 0 and 1216 (maximum cylinder address). Operation is terminated by an error condition or by pressing the Execute switch. To execute Test 09, perform the following steps:

1. Enter Test 09 and press EXEC switch.

2. The LCD will display "OK, CYL: XXX" if execution was successful.

3. If an error occurs during the test, the LCD will display "SVO ERR: XX". Drive status codes (SVO ERR) are defined in a table at the end of this section.

4. Press EXEC switch to end the test and return to test selection.

Test 0C -- Display EPROM Part Number

This test displays the eight digit part number of the control microprocessor EPROM. To execute Test 0C, perform the following steps:

1. Enter Test 0C and press EXEC switch. The LCD will display the 8 digit part number of the EPROM.

2. Press EXEC switch to end the test and return to test selection.

Test 0E -- Return To Zero

This test initiates a return to zero command. To execute Test 0E, perform the following steps:

1. Enter Test 0E and press EXEC switch. The LCD will display "OK, CYL: 00".

2. If an error occurs during the test, the LCD will display "SVO ERR: XX". Drive status codes (SVO ERR) are defined in a table at the end of this section.

3. Press EXEC switch to end the test and return to test selection.

DRIVE STATUS CODES

Whenever the drive is in a power on condition (dc power active), the Control MPU is periodically checking the operation of the drive and generating appropriate operating status codes.

Drive status codes are reported to the controller via the SMD-E interface when it issues Tag 5 with Bus Out bit 0 true and Bus Out bit 1 false. If a status/control panel is attached to the drive, the codes can be visually monitored by removing the drive front panel insert. Table 3-5 lists the status codes and a definition of each code. If a drive malfunction occurs, observe the error code and perform Diagnostic Test 04 to calculate the action to be taken.

Figure 3-3 shows an example of the LCD (Liquid Crystal Display) during normal operation and when a fault occurs. During normal operation, the LCD displays current drive status, current cylinder address, and which drive channel is selected and/or reserved. If a fault occurs, the LCD displays the type of fault(s) that occurred along with the current drive status. If more than one fault occurred, use the space switch to step through the fault log to determine what faults are present.

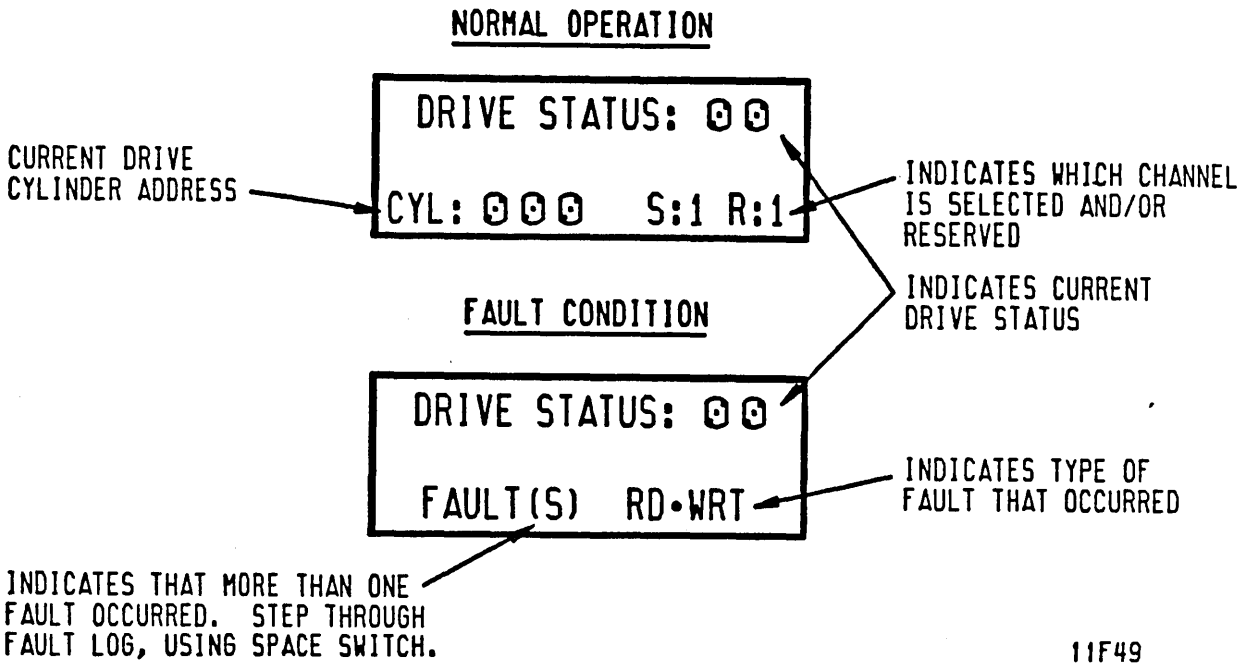


Figure 3-3. Example of LCD (Liquid Crystal Display)

TABLE 3-5. DRIVE STATUS CODES

Code	Title	Description
NORMAL START/STOP STATUS		
00	Ready & On Cylinder	When the Control MPU displays this status code, it indicates that the drive is on cylinder and ready to perform normal operations.
01	Carriage Parked	Indicates that the carriage latch electromagnet is holding the carriage in the landing zone.
(Table Continued on Next Page)		

TABLE 3-5. DRIVE STATUS CODES (Contd)

Code	Title	Description
NORMAL START/STOP STATUS (Contd)		
02	Motor Stopping	The Control MPU sets this status code during the motor braking period.
03	Motor Stopped	The Motor MPU sets this status code when it detects that the motor is stopped. The status remains at 03 until start conditions are available.
04	First Load/Calibrate	When this status code is displayed, the heads move from the landing zone to track 0 and a servo calibration (self test) is initiated. During this time the Servo MPU examines the amount of overshoot on the position signal and the time it takes to complete an RTZ operation and makes the necessary corrections.
05	Sequence Delay	If the Remote/Local switch is set to Remote, the power up sequence to each drive is delayed. The length of delay is determined by the logical address number used in increments of 5 seconds. After the delay, the status changes to 07.
06	Start Switch Pressed and Waiting for (PICK/HOLD + LOCAL)	The Control MPU sets this status code when the START switch is pressed. If the drive is in Local, the status code changes to 07. If the drive is in Remote and Sequence Pick or Hold from the controller goes active, the status changes to 05.

(Table Continued on Next Page)

TABLE 3-5. DRIVE STATUS CODES (Contd)

Code	Title	Description
	NORMAL START/STOP STATUS (Contd)	
07	Starting Motor	The Control MPU displays this status code when all start conditions (codes 05 and 06) have been satisfied. The status remains at 07 until the motor reaches full speed.
08	Motor Up To Speed	The Control MPU displays this status code when the motor is up to full speed.
	SEEK ERROR STATUS	
46	Seek Timeout	Indicates that during a normal seek the drive took longer than 100 milliseconds to reach on cylinder. When the drive displays code 46, the following error indications also appear: • Seek Error and Seek End lines go active. • Motor continues to run but servo system is disabled and the heads, although loaded, float freely over the disk surfaces. An RTZ clears the Seek Error and initiates a seek to cylinder 0.
	(Table Continued on Next Page)	

TABLE 3-5. DRIVE STATUS CODES (Contd)

Code	Title	Description
SEEK ERROR STATUS (Contd)		
4B	Off Track Seek Error	Indicates that either the drive failed to stay on cylinder or cylinder pulses were detected during track-following. When the drive displays code 4B, the following error indications also appear: • On Cylinder goes inactive. • Seek Error and Seek End go active. • Motor continues to run, but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. An RTZ command clears the Seek Error and initiates a seek to cylinder 0.
4D	Illegal Cylinder Address	Indicates that during a normal seek, the Control MPU received too high a cylinder address (greater than 1216). When the drive displays code 4D, the following error indications also appear: • On Cylinder goes inactive. • Seek Error and Seek End go active.
(Table Continued on Next Page)		

TABLE 3-5. DRIVE STATUS CODES (Contd)

Code	Title	Description
SEEK ERROR STATUS (Contd)		
4F	Seek Error On Settle In	• The drive remains on cylinder because no commands have been sent to the Servo MPU. Indicates that the drive could not settle in on the destination cylinder. The following error indications also appear: • Seek Error and Seek End lines go active. • Motor continues to run but servo system is disabled and the heads, although loaded, float freely over the disk surfaces. An RTZ clears the Seek Error and initiates a seek to cylinder 0.
CONTROL MPU ERRORS		
50	Low Vcc Glitch	Indicates that the Control MPU was reset and that DC Master Clear is active due to Low Vcc (power loss).
51	Control MPU Reset	Indicates that the Control MPU was reset due to a hang condition.

(Table Continued on Next Page)

TABLE 3-5. DRIVE STATUS CODES (Contd)

Code	Title	Description
	FIRST SEEK FAULT STATUS	
54	First Seek Fault On Retract	Indicates that the Servo MPU failed to complete the retract portion of the first seek.
55	First Seek Fault On Load	Indicates that the drive failed to load the heads.
56	First Seek Fault On RTZ	Indicates that the drive failed to complete the return to zero (RTZ) portion of the first seek.
57	First Seek Fault On Calibrate	Indicates that the drive did not complete the velocity calibration operation.
	ERROR CONDITION STATUS	
58	Speed Loss	Indicates that the spindle speed fell below 3564 r/min. The Motor MPU inactivates the Speed OK code to the Control MPU. This causes the Control MPU to activate the Write Protect line. The Control MPU also drops the Ready signal and performs a retract operation.
59	Motor Can't Start Due to Error	Indicates that the Control MPU did not receive start conditions from the Motor MPU due to an error caused by overcurrent or other bad status between the Motor and Control MPU's.

(Table Continued on Next Page)

TABLE 3-5. DRIVE STATUS CODES (Contd)

Code	Title	Description
ERROR CONDITION STATUS (Contd)		
5A	Emergency Retract	Indicates that the heads retracted back to the landing zone due to a power loss (-Low Vcc active), or that the Servo MPU is unable to perform a retract operation.
MOTOR AND SERVO MPU ERRORS		
60	Motor MPU Failure	Indicates that the Control MPU was unable to communicate with the Motor MPU.
61	Servo MPU Failure	Indicates that the Control MPU was unable to communicate with the Servo MPU.

SECTION 4

ELECTRICAL CHECKS

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in Section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

This section contains electrical checks intended for use in isolating problems causing improper drive operation. These procedures should be used in conjunction with the troubleshooting information in section 3.

If the drive appears to be operating properly, failure to meet a specification given here does not in itself indicate improper drive operation. The person performing these procedures should be thoroughly familiar with drive operation and with all information in the general maintenance section of this manual (particularly the warnings and precautions).

When performing electrical checks, refer to section 2, figure 2-2 (component locator) for pin orientation of test points J80 (on the control board) and J48 (on the read/write board). Many read/write electrical checks require the use of a chip clip.

Each electrical check procedure is assigned a unique number. The numbers are used elsewhere in the manual to reference the procedures. The procedure numbers are organized into five categories: 41XX - power checks, 42XX - servo checks, 43XX - write checks, 44XX - read checks, and 45XX - miscellaneous.

The procedures appear in the following order.

- 4101 - Power Checks
- 4201 - Position Signal Check
- 4202 - Cylinder Pulse Check
- 4203 - Servo Track Check
- 4204 - Cylinder Address Bit Check
- 4301 - Write Fault Grounding
- 4302 - Write PLO Check
- 4303 - Write Data Check
- 4304 - Write Address Mark Check
- 4401 - Read PLO Check
- 4402 - Read Data Check
- 4403 - Read Address Mark Check
- 4501 - Index Check
- 4502 - Sector Check

4101 - POWER CHECKS

The following procedure provides an overall check of the dc voltages used by the drive. Table 4-1 shows the voltages required by each drive component. See the diagrams section of hardware maintenance manual volume 3 for specific information concerning voltage test points.

CAUTION

Because some voltage measurements are on pins adjacent to each other, it is possible to touch both pins simultaneously, thus causing a short circuit. A short circuit will cause serious damage to drive electronic assemblies. Therefore, use extreme caution when performing the following steps.

1. Command continuous seeks between cylinder 0 and 256.

2. Connect voltmeter ground lead to J80-9 (chassis ground).

3. Measure between ground and the appropriate connection points to check the following voltages:

Voltage	Connection	Specification
+5 volts	J80-20	+4.85 to +5.20 volts
-5 volts	J80-22	-4.90 to -5.30 volts
-12 volts	J80-23	-11.15 to -12.60 volts
+24 volts	J15-12	+22.8 to +25.2 volts
+12 volts	J80-21	+11.80 to +12.20 volts
Ground	J80-9	

4. Proceed to next test or return drive to online operation.

TABLE 4-1. DC VOLTAGE DISTRIBUTION

Component	Voltage				
	+5V	-5V	-12V	+12V	+24V
Control Board	X	X	X	X	X
Read/Write Board	X	X	X	X	
I/O Board	X	X			
Status/Control Panel	X	X		X	
Fan					X

4201 - POSITION SIGNAL CHECK

This check verifies the amplitude of the position signal over the period of a complete seek.

1. Connect oscilloscope as shown on figure 4-1.

2. Command continuous seeks between cylinders 0 and 256.

3. Observe that the peak to peak value of -Position signal over the period of a complete seek is approximately as shown in figure 4-1.

4. Command continuous seeks between cylinders 0 and 1216 and observe that -Position is as described in step 3 (see figure 4-2).

5. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	J80-7 ON -WAX	-POSITION
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-EXT	J80-4 ON -WAX	-FORWARD

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 2.0 MS/CM MODE:

NOTES:

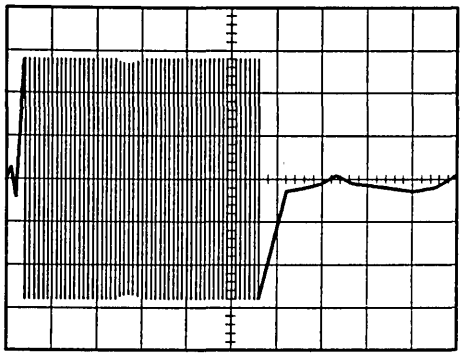


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Figure 4-1. Position Signal (Tracks 0-256)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	J80-7 ON -WAX	-POSITION
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+EXT	J80-4 ON -WAX	-FORWARD

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 5.0 MS/CM MODE:

NOTES:

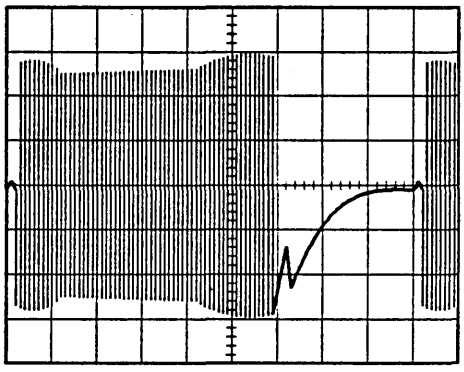

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Figure 4-2. Position Signal (Tracks 0 to 1216)

4202 - CYLINDER PULSE CHECK

This procedure verifies that cylinder pulses occur at the proper time.

1. Connect oscilloscope as shown in figure 4-3.
2. Command continuous seeks between cylinders 0 and 30.
3. Observe that track crossing occurs approximately as shown in figure 4-3.
4. Proceed to next test or return drive to online operation.

4203 - SERVO TRACK CHECK

This procedure checks each servo track for an off cylinder condition during on cylinder.

NOTE

The measurements given in this procedure are approximate. They are used as an aid for troubleshooting seek problems (for example, failure to remain on cylinder).

1. Connect oscilloscope as shown in figure 4-4.
2. Command a continuous 1 track forward sequential scan with read gate active and one head selected.
3. Ensure that the drive is within the following limits:
   - Any spikes occurring during track-following should be less than 1 volt, either side of ground
   - The average voltage of the position signal during track-following should be within 0.5 volts, either side of ground
   - Consistency from track to track
4. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	5.0 V/CM	J80-7 ON -WAX	-POSITION
CH 2	2.0 V/CM	J80-3 ON -WAX	-CYLINDER PULSES

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-EXT	J80-4 ON -WAX	-FORWARD

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 MS/CM MODE: ALT

NOTES:

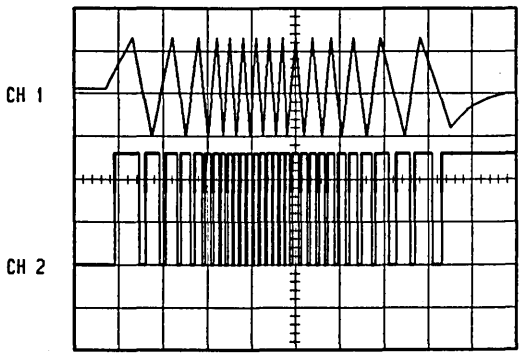

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Figure 4-3. On Cylinder Check

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	J80-7 ON -WAX	-POSITION
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-EXT	J80-4 ON -WAX	-FORWARD

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 5.0 MS/CM MODE: CH 1

NOTES:

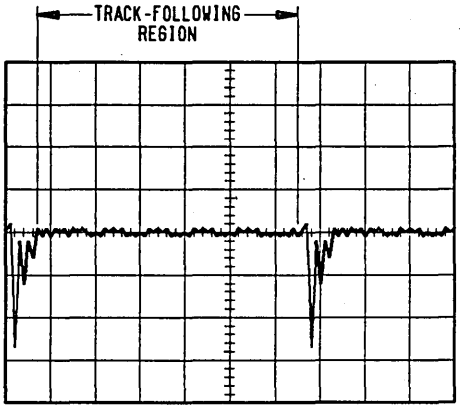

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Figure 4-4. Servo Track Check

4204 - CYLINDER ADDRESS BIT CHECK

This check ensures that the cylinder address bits 0-10 are OK.

1. Perform a direct seek using each cylinder address bit 0 through 10.

2. Ensure that an on cylinder condition occurs at the completion of each seek.

3. Proceed to next test or return drive to online operation.

WRITE CHECKS

GENERAL

The following procedures, 4301 through 4304, check various aspects of the drive write circuit operation. Figure 4-5 is a block diagram showing the major components in the write circuits and the test points used in the procedures.

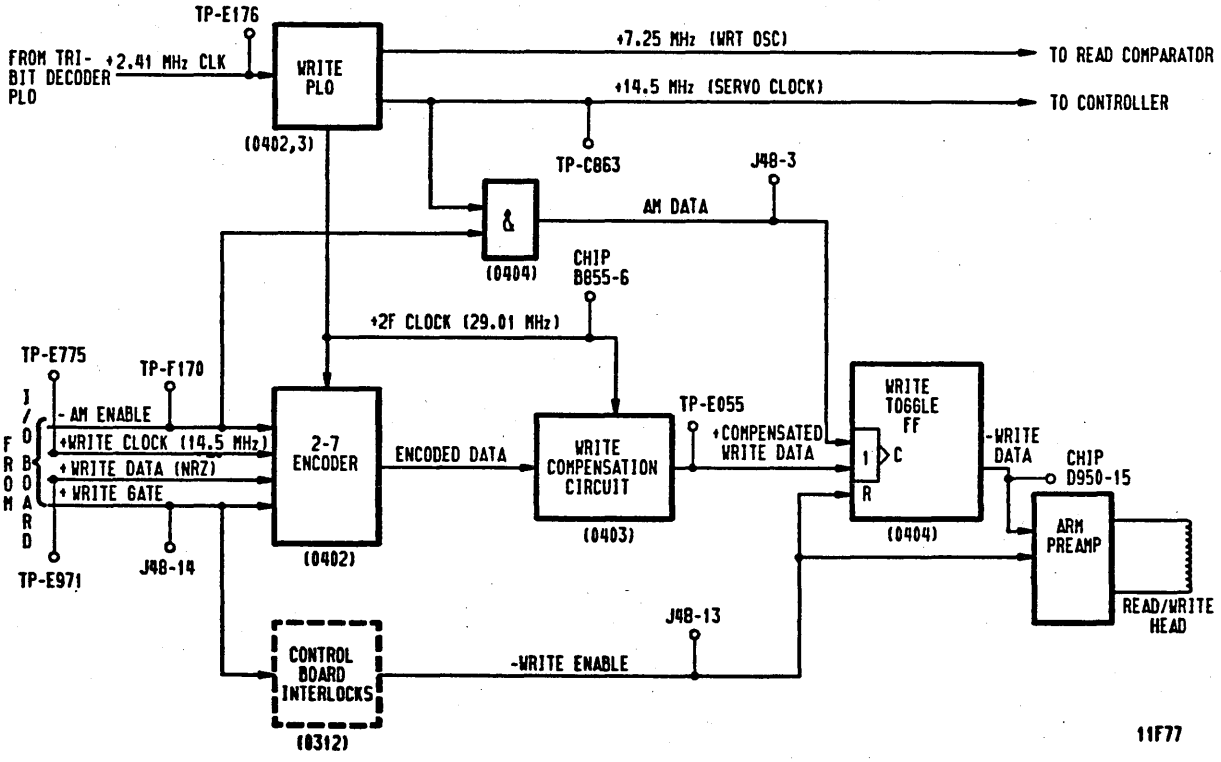


Figure 4-5. Write Circuits Test Points

4301 - WRITE FAULT GROUNDING

If a write fault condition exists, the drive write circuits are disabled. This makes it difficult to test the write circuits and isolate the problem. Grounding the Write Fault signal at the point where it leaves the read/write board disables the write fault function, thus allowing the drive to perform write operations even though fault conditions exist. The following procedure describes the proper method for grounding the Write Fault signal.

CAUTION

Perform this procedure only during trouble-shooting, when a write fault condition interferes with isolating the problem.

1. Remove power from drive as follows:

   a. Press START switch to stop motor and unload heads.

   b. Set On/Standby switch on power supply to Standby (0).

CAUTION

Be certain to remove jumper wire when testing is complete. Failure to remove wire can result in loss of customer data.

2. Connect jumper wire between chip F468-11 (+Write Fault) and ground on read/write board.

3. Power up drive and perform tests. Monitor chip F468-10 (+Fault) on read/write board to determine if write fault condition persists. When testing is complete, remove jumper wire.

4302 - WRITE PLO CHECK

This procedure checks the operation of the write PLO. The PLO provides timing signals, used during write operations by both the drive and controller.

1. Connect oscilloscope and observe that the 2.41 MHz Clock frequency is approximately as shown on figure 4-6.

2. Connect oscilloscope and observe that the 14.5 MHz Clock frequency is approximately as shown on figure 4-7.

3. Connect oscilloscope and observe that the 2F Clock timing is approximately 29.01 MHz (see figure 4-8).

4. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-E176 ON -VYX	+2.41 MHz CLOCK
CH 2			

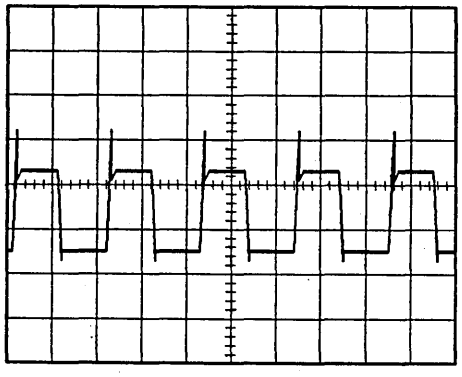
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.2 µS/CM MODE: CH 1

NOTES:



11F100

Figure 4-6. 2.41 MHz Clock Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-C863 ON -VYX	+14.5 MHz (SERVO CLOCK)
CH 2			

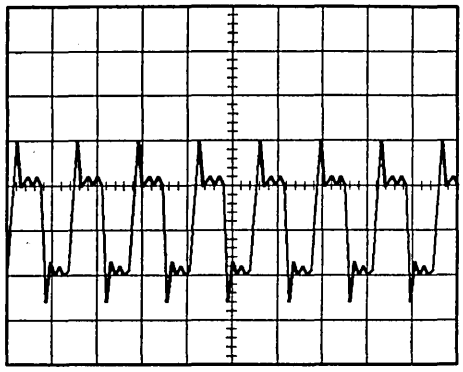
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: CH 1

NOTES:



11F101

Figure 4-7. 14.5 MHz Servo Clock Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP B855-6 ON -VYX	+2F CLOCK
CH 2			

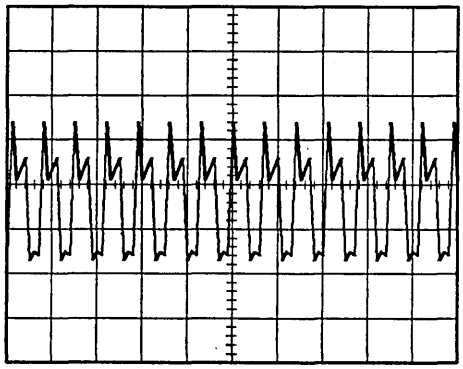
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: CH 1

NOTES:



11F103

Figure 4-8. 2F (29.01 MHz) Clock Timing

4303 - WRITE DATA CHECK

This procedure checks for the presence of write data at various points in the write circuits (see figure 4-5). If the signals at these points are correct, it indicates the circuits are performing their basic functions. This procedure will normally be performed because of a write problem. In that case, a write fault condition may exist and it will be necessary to perform procedure 4301 - Write Fault Grounding, to perform a write operation.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

1. Command drive to seek to desired cylinder and select desired head.

2. Command drive to write a 1010... pattern.

3. Connect oscilloscope as shown on figure 4-9 and observe that Write Gate and Write Enable appear as shown.

4. Check inputs to 2-7 encoder circuit. Timing relationships between these signals, NRZ write data and write clock, must be correct before encoding and write compensation can be properly performed.

   a. Connect oscilloscope as shown on figure 4-10 and observe that Write Clock frequency is approximately 14.5 MHz.

   b. Observe that timing relationship between Write Data (NRZ) and Write Clock is similar to that on figure 4-10. Write Clock should go positive at approximately the center of the data "1" pulses.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.2 V/CM	J48-14 ON -VYX	+WRITE GATE
CH 2	0.2 V/CM	J48-13 ON -VYX	-WRITE ENABLE

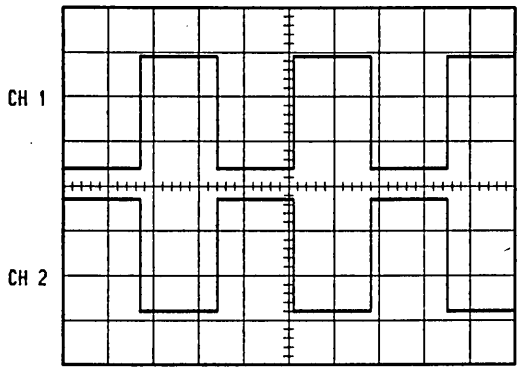
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 10 MS/CM **MODE:** CHOPPED

NOTES:



11F104

Figure 4-9. Write Gate Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-E971 ON -VYX	+WRITE DATA (NRZ)
CH 2	0.5 V/CM	TP-E775 ON -VYX	+WRITE CLOCK

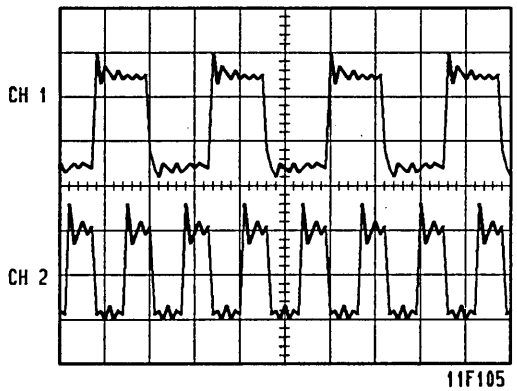
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM **MODE:** ALT

NOTES:



11F105

Figure 4-10. Write Data to Write Clock Timing

5. Check write data (compensated) control circuits as follows:

   a. Connect oscilloscope as shown on figure 4-11.

   b. Observe that timing relationship between write data (compensated) and 2F (write oscillator) is similar to that on figure 4-11.

6. Check output of write toggle circuit as follows:

   a. Move oscilloscope channel 2 probe to Chip D950, pin 15 on read/write board (see figure 4-12).

   b. Observe that signals are approximately as shown on figure 4-12.

7. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-E055 ON -VYX	+COMPENSATED WRITE DATA
CH 2	0.5 V/CM	CHIP B855-6 ON -VYX	+2F CLOCK

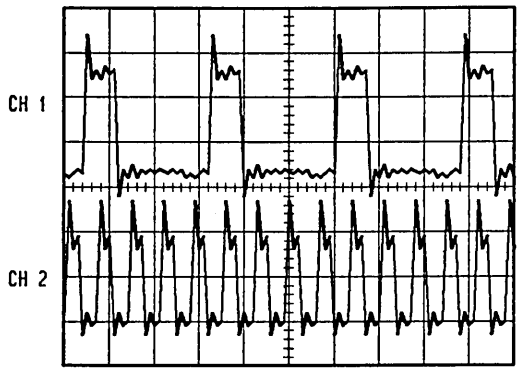
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:



11F106

Figure 4-11. Compensated Write Data Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-E055 ON -VYX	+COMPENSATED WRITE DATA
CH 2	0.5 V/CM	CHIP D950-15 ON -VYX	-WRITE DATA

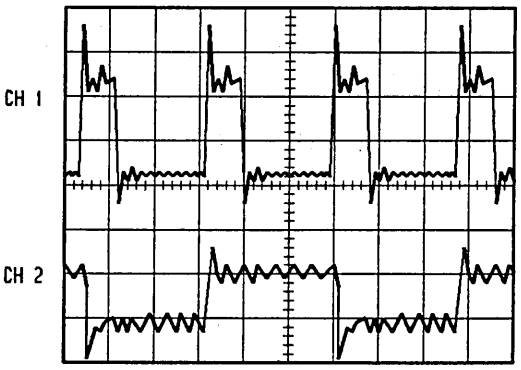
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:



11F107

Figure 4-12. Write Toggle Output

4304 - WRITE ADDRESS MARK CHECK

This procedure verifies that the drive writes the address mark pattern during the time that Address Mark Enable is active.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

1. Command continuous write format with address mark operations using a 1010... data pattern.
2. Connect oscilloscope as shown on figure 4-13.
3. Observe that a 7.25 MHz clock occurs during the time that Address Mark Enable is active.
4. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-F170 ON -VYX	-AM ENABLE
CH 2	0.5 V/CM	J48-3 ON -VYX	AM DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM MODE: ALT

NOTES:

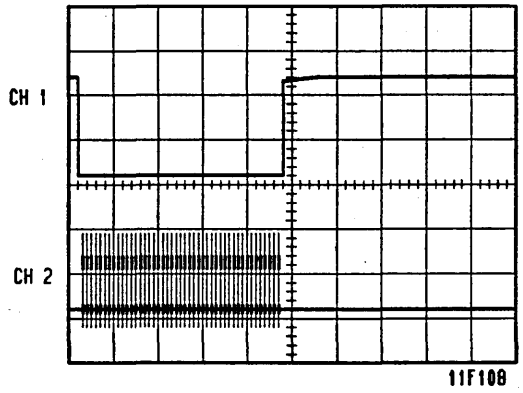


Figure 4-13. Write Address Mark Timing

READ CHECKS

The following procedures, 4401 through 4403, check various aspects of drive read circuit operation. Figure 4-14 is a block diagram showing the major components in the read circuits and the test points used in the procedures.

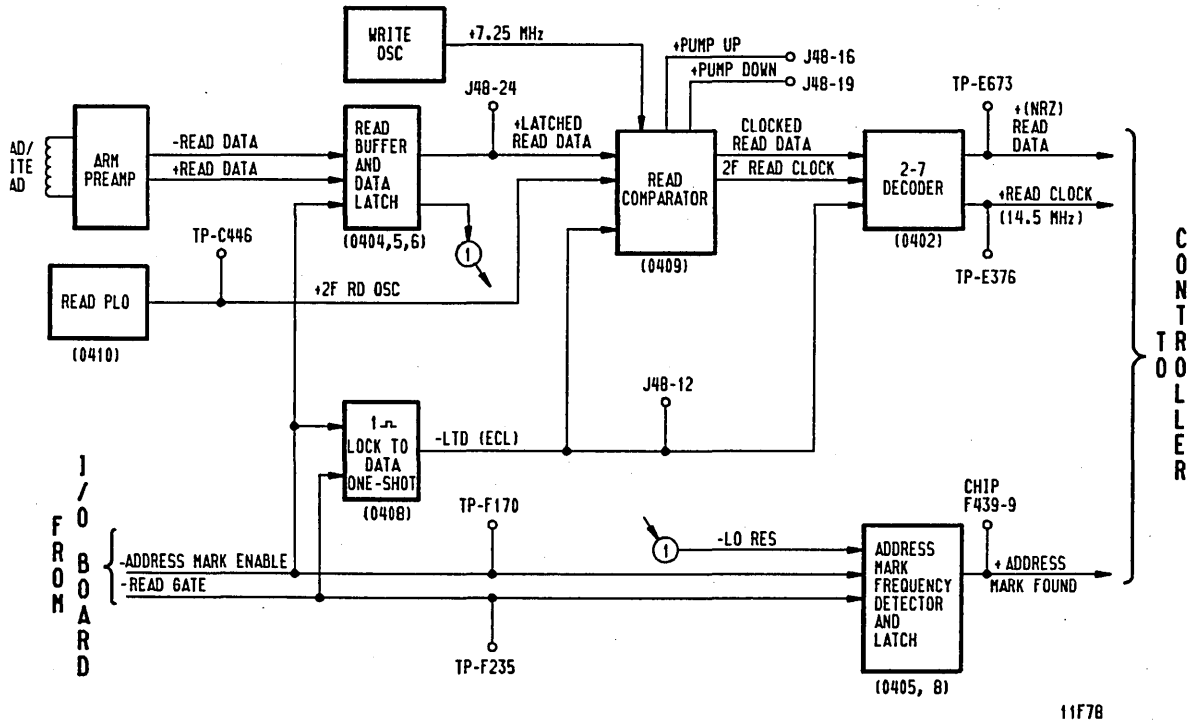


Figure 4-14. Read Circuits Test Points

4401 - READ PLO CHECK

This procedure checks the operation of the read PLO circuits. The read PLO provides timing signals used during read operations.

1. Connect oscilloscope as shown on figure 4-15 and observe that 2F Read Oscillator frequency is approximately 29.01 MHz.

2. Connect oscilloscope as shown on figure 4-16 and observe that the +Pump Up and +Pump Down signals are coincident.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

3. Command drive to write a 1010... pattern using any head.

4. Command drive to perform continuous read operations.

5. Observe that +Pump Up and +Pump Down signals have the same timing relationship shown on figure 4-17.

6. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP A837-4 ON -VYX	+2F READ OSC
CH 2			

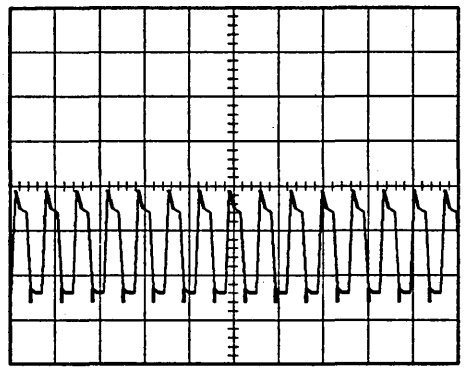
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: CH 1

NOTES:



11F109

Figure 4-15. 2F Read Oscillator Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	J48-16 ON -VYX	+PUMP UP
CH 2	0.5 V/CM	J48-19 ON -VYX	+PUMP DOWN

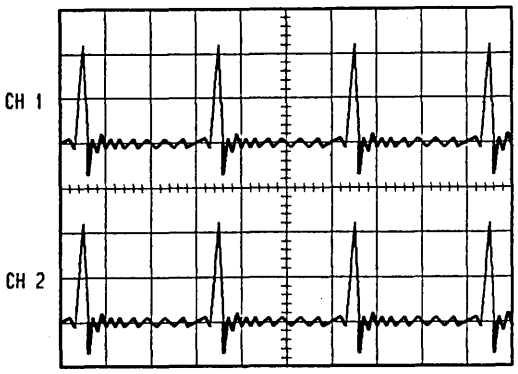
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM **MODE:** ALT

NOTES:



11F110

Figure 4-16. Pump Up/Down Timing (Not Reading)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	J48-16 ON -VYX	+PUMP UP
CH 2	0.5 V/CM	J48-19 ON -VYX	+PUMP DOWN

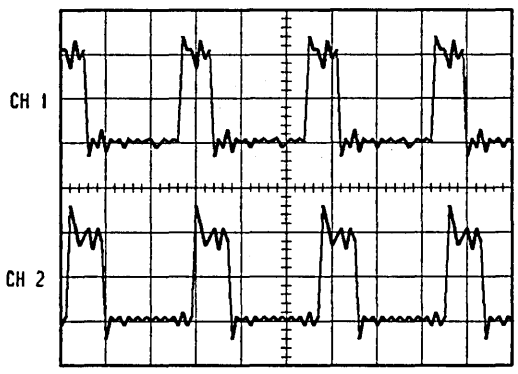
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM **MODE:** ALT

NOTES:



11F111

Figure 4-17. Pump Up/Down Timing (Reading)

4402 - READ DATA CHECK

This procedure checks the operation of the data latch, read comparator, and 2-7 decoder circuits.

1. Perform Write Data Check (proc 4303).

2. Perform Read PLO Check (proc 4401).

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

3. Command drive to seek to desired cylinder and select desired head.

4. Command drive to write a 1010... pattern and then to perform continuous read operations.

5. Check the Latched Read Data signal and its timing relationship with the 2F Read oscillator signal.

   a. Connect oscilloscope as shown on 4-18 and observe that Latched Read Data pulse width is as shown.

   b. Observe that Latched Read Data pulses and 2F Read Oscillator pulses have the approximate phase relationship shown in figure 4-18.

   c. Observe that the data pattern is correct.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	J48-24 ON -VYX	+LATCHED READ DATA
CH 2	0.5 V/CM	TP-C446 ON -VYX	+2F READ OSCILLATOR

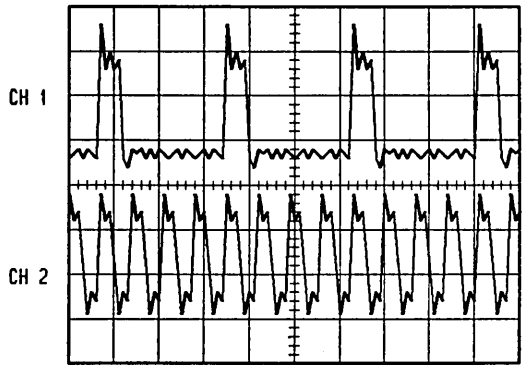
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM **MODE:** ALT

NOTES:



11F112

Figure 4-18. Latched Read Data Timing

6. Check Read Data to Read Clock Timing.

   a. Connect oscilloscope as shown on figure 4-19 and observe that Read Clock frequency is approximately 14.5 MHz.

   b. Observe that Read Data to Read Clock timing is approximately as shown. Read Clock should go positive approximately at the center of the data "1" pulses.

   c. Observe that the NRZ data has a 1010... pattern.

7. Check Read Gate to Lock to Data timing.

   a. Connect oscilloscope as shown on figure 4-20.

   b. Observe that -Lock to Data goes high at the proper time (see figure 4-20).

8. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	TP-E673 ON -VYX	+READ DATA (NRZ)
CH 2	0.5 V/CM	TP-E376 ON -VYX	+READ CLOCK

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

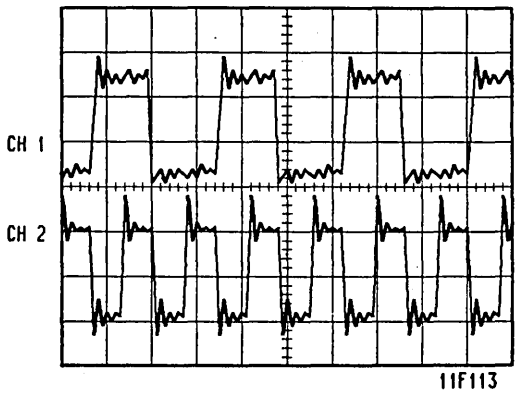


Figure 4-19. NRZ Read Data Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-F235 ON -VYX	-READ GATE
CH 2	0.5 V/CM	J48-12 ON -VYX	-LTD (ECL)

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1.0 µS/CM MODE: ALT

NOTES:

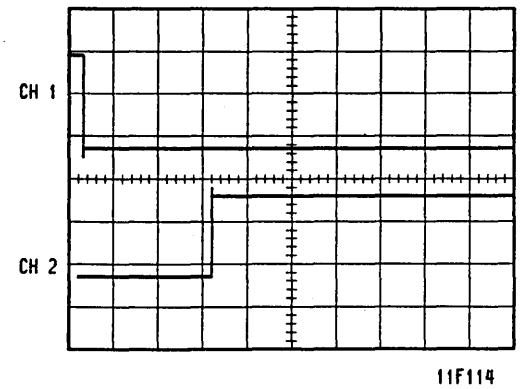


Figure 4-20. Read Gate to Lock to Data Timing

4403 - READ ADDRESS MARK CHECK

This procedure checks for the presence of address marks and verifies that the timing is correct.

CAUTION

To avoid possible loss of customer data, select a head and cylinder that will result in data being written on an unused track.

1. Command a write format in address mark mode using a 1010.. pattern. Then command a continuous read address mark operation.

2. Connect oscilloscope as shown on figure 4-21.

3. Check that the length of the address mark area is within the limits shown on figure 4-21. If it is outside these limits the address mark detection circuits may not function properly.

4. Observe that Address Mark Found goes active immediately following the address mark area.

5. Connect oscilloscope as shown on figure 4-22.

6. Observe that -Lock to Data goes active at the proper time (see figure 4-22).

7. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	J48-24 ON -VYX	+LATCHED READ DATA
CH 2	2.0 V/CM	CHIP F439-9 ON -VYX	+ADDRESS MARK FOUND

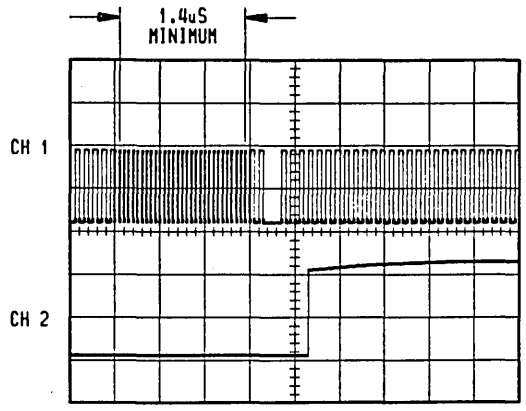
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+EXT	J80-6 ON -WAX	+INDEX

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: **MODE:**

A TIME/DIV: 5uS/CM



11F116

NOTES:

1. EXPAND TO 10X MAGNIFICATION AND ADJUST HORIZONTAL POSITION TO MAKE ADDRESS MARK AREA VISIBLE.

Figure 4-21. AM Found Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-F170 ON -VYX	-AM ENABLE
CH 2	0.5 V/CM	J48-12 ON -VYX	-LTD (ECL)

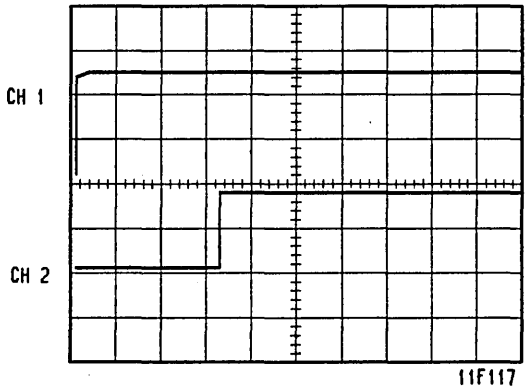
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1.0 µS/CM **MODE:** ALT

NOTES:



11F117

Figure 4-22. AM to Lock To Data Timing

MISCELLANEOUS LOGIC CHECKS

4501 - INDEX CHECK

This procedure checks that Index is present and has the proper pulse width. It also checks the time between successive Index pulses which is an indication of disk rotational speed.

1. Connect oscilloscope as shown on figure 4-23.
2. Observe that the Index pulse width is between 2.2 and 2.8 microseconds.
3. Connect oscilloscope as shown on figure 4-24.
4. Observe that the time between Index pulses is between 16.5 and 16.8 milliseconds.
5. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	J80-6 ON -WAX	+INDEX
CH 2			

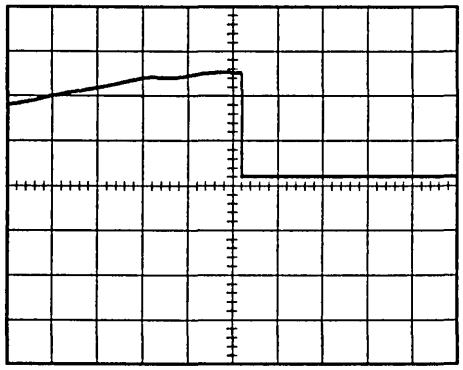
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM MODE: CH 1

NOTES:



11F118

Figure 4-23. Index Pulse Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	J80-6 ON -WAX	+INDEX
CH 2			

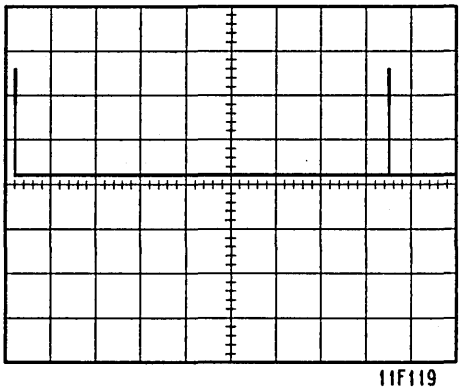
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 2.0 MS/CM MODE: CH 1

NOTES:



11F119

Figure 4-24. Index to Index Timing

4502 - SECTOR CHECK

This procedure checks for the presence of sector pulses and that they have the proper width.

1. Connect oscilloscope as shown on figure 4-25.
2. Observe that the Sector pulse width is between 1.05 and 1.45 microseconds.
3. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	J80-5 ON -WAX	+SECTOR
CH 2			

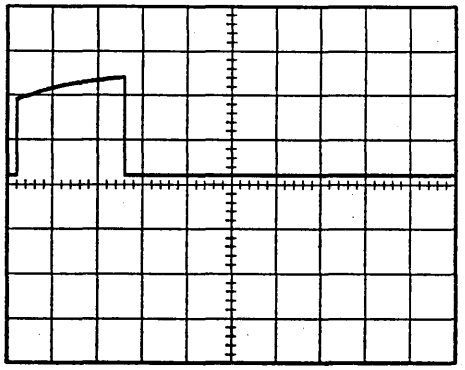
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH 1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM MODE: CH 1

NOTES:



11F120

Figure 4-25. Sector Pulse Timing

SECTION 5

REPAIR AND REPLACEMENT

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

Repair of the drive is limited to replacement of defective parts and assemblies. This section describes removal and replacement of all major field replaceable parts and assemblies. The information here should be used in conjunction with that in the parts data section of Hardware Maintenance Volume 1.

The procedures in this section assume that the drive is mounted in the 2X drawer, and the drawer is mounted on slides in an equipment rack or cabinet. But unless otherwise specified, it is not necessary to remove the drive from the 2X drawer to perform maintenance. All procedures require that power be removed from the drive and power supply. The person performing the maintenance should be thoroughly familiar with the operation of the drive and with all information in the general maintenance section of this manual (particularly warnings and precautions).

Each procedure is assigned a unique number. The numbers are used elsewhere in the manual to reference the procedures. The procedures and numbers are organized into three categories: 51XX - mechanical, 52XX - electromechanical, and 53XX - electronic (circuit boards).

- 5101 - Top Cover Removal & Replacement
- 5102 - Entire Drive Removal & Replacement
- 5103 - Front Panel Removal & Replacement
- 5201 - Fan Removal & Replacement
- 5202 - Status/Control Panel Removal & Replacement
- 5203 - Power Supply Removal & Replacement
- 5204 - Module Removal & Replacement
- 5205 - Carriage Latch Electromagnet Removal & Replacement
- 5301 - Read/Write Board (_VYX) Removal & Replacement
- 5302 - I/O Board (_VRX) Removal & Replacement
- 5303 - Control Board (_WAX) Removal & Replacement

5101 - TOP COVER REMOVAL & REPLACEMENT

REMOVAL

CAUTION

With the top cover removed, electrostatic sensitive components are exposed and may be seriously damaged by static electricity. To avoid possible damage, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual.

CAUTION

Be careful not to damage the system cabling when sliding the drive in the drawer and the drawer in and out of the rack.

1. Remove front panel insert from each drive (see figure 5-1).

NOTE

The release latch on the left-hand drive locks the 2X drawer in the rack. The release latch on the right-hand drive has no function.

2. Push 2X drawer release latch to the right and extend 2X drawer to fully extended position.

3. Remove power from drive as follows:

   For drives with status/control panel:

   a. Press START switch to stop the drive.

   b. Wait for Ready indicator (on START switch) to stop flashing; then, set On/Standby switch on power supply to Standby (0) position.

   For drives without status/control panel, set On/Standby switch on power supply to Standby (0) position.

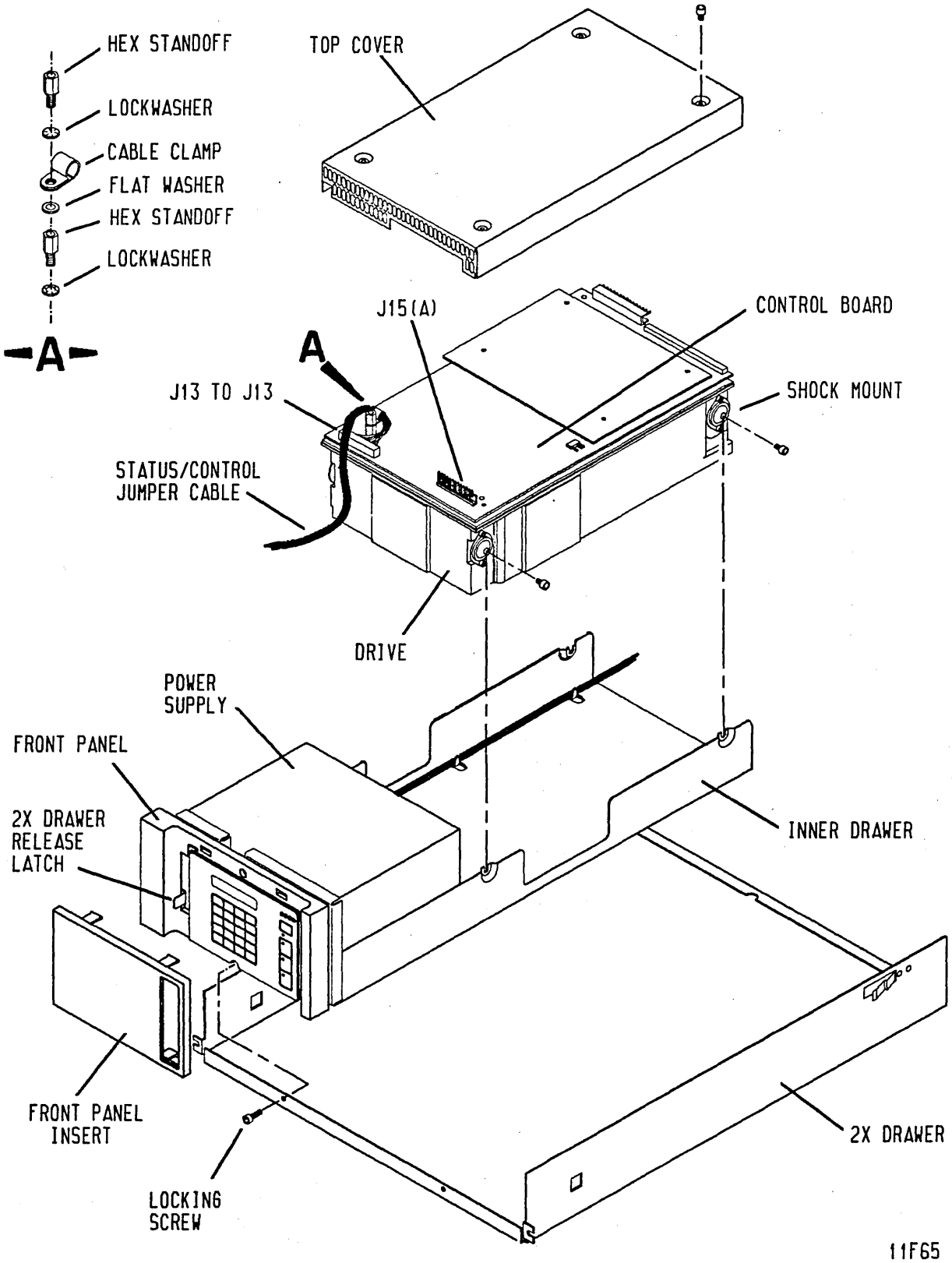


Figure 5-1. Drive Removal & Replacement

4. Remove inner drawer locking screw. Push 2X drawer release latch to the right, lift inner drawer up, and slide it outward to gain access to top cover.

5. Remove screws securing top cover to drive.

NOTE

To maintain drive configuration whenever the top cover is removed, always identify which drive that the top cover was removed from.

6. Carefully, lift off cover.

REPLACEMENT

1. If a new (replacement) top cover is being installed, copy the drive information from the labels of the old top cover to the new labels and attach the new labels to the new top cover.

CAUTION

When replacing cover, use care to avoid damaging logic boards.

2. Ensure power is removed from drive. Place top cover on drive and secure with screws (see figure 5-1).

3. Push inner drawer back into 2X drawer, and secure into place with locking screw.

4. Set On/Standby switch on power supply to On (1) position.

5. Push 2X drawer back to closed position in rack.

6. Install front panel insert.

5102 - ENTIRE DRIVE REMOVAL & REPLACEMENT

The following procedure provides instructions for removing and replacing the entire drive. The drive is mounted in the 2X drawer, and the drawer is mounted on slides in an equipment rack (see figure 5-1).

REMOVAL

1. Remove front panel insert from each drive.

NOTE

The release latch on the left-hand drive locks the 2X drawer in the rack. The release latch on the right-hand drive has no function.

2. Push 2X drawer release latch to the right and extend 2X drawer to gain access to On/Standby switch on power supply.

3. Remove power from drive as follows:

   For drives with status/control panel:

   a. Press START switch to stop the drive.

   b. Wait for Ready indicator (on START switch) to stop flashing; then, set On/Standby switch on power supply to Standby (0) position.

   For drives without status/control panel, set On/Standby switch on power supply to Standby (0) position.

4. Push 2X drawer back to closed position in rack.

5. Remove I/O cover and cable clamps from I/O cable bracket.

CAUTION

Remove terminators by hand. They could be damaged if a pliers or other tool is used.

6. Disconnect I/O cables, terminators, and system ground strap from drive.

7. Remove I/O cable bracket from drive rear panel.

8. Disconnect ac power cable from site power.

9. Push 2X drawer release latch to the right and extend 2X drawer to fully extended position.

10. Remove inner drawer locking screw.

11. Push 2X drawer release latch to the right, lift inner drawer up and remove it from 2X drawer. Place inner drawer on work table.

12. Remove screws securing top cover to drive.

NOTE

To maintain drive configuration whenever the top cover is removed, always identify which drive that the top cover was removed from.

13. Carefully, lift off cover.

14. Disconnect dc power cable from J15 (A) on control board (_WAX).

15. Disconnect dc ground strap from module.

16. For drives with status/control panel, perform the following:

    a. Disconnect jumper cable from J13 on control board (see figure 5-1).

    b. Remove cable clamp from control board.

17. Loosen shock mount screws securing module to inner drawer.

18. Carefully, lift drive out of drawer and move to desired location.

REPLACEMENT

1. Mount drive to inner drawer (see figure 5-1).

2. Connect dc ground strap to module and secure module to shock mounts.

3. For drives with status/control panel, perform the following:

   a. Connect jumper cable to J13 on control board.

   b. Attach cable clamp to control board as shown in figure 5-1.

4. Connect dc power cable to J15 (A) on control board.

CAUTION

When replacing top cover, use care to avoid damaging logic boards.

5. Place top cover on drive and secure with screws.

6. Place inner drawer in 2X drawer and secure with locking screw.

7. Push 2X drawer back to closed position in rack.

8. Attach I/O cable bracket to drive rear panel.

9. Connect I/O cables and terminators to drive connectors, and attach strain relief clamp to cable bracket.

10. Attach I/O cable cover and grounding clamp to cable bracket.

11. Connect system ground strap to drive rear panel.

12. Connect ac power cord to site power.

13. Push 2X drawer release latch to the right and extend 2X drawer to gain access to On/Standby switch on power supply.

14. Set On/Standby switch on power supply to On (1) position.

15. Push 2X drawer back to closed position in rack.

16. Install front panel insert.

5103 - FRONT PANEL REMOVAL & REPLACEMENT

The front panel attaches to the inner drawer. The following procedure provides instructions for removing and replacing the front panel.

REMOVAL

1. Remove front panel insert from each drive (see figure 5-2).

NOTE

The release latch on the left-hand drive locks the 2X drawer in the rack. The release latch on the right-hand drive has no function.

2. Push 2X drawer release latch to the right and extend 2X drawer to gain access to On/Standby switch on power supply.

3. Remove power from drive as follows:

   For drives with status/control panel:

   a. Press START switch to stop the drive.

   b. Wait for Ready indicator (on START switch) to stop flashing; then, set On/Standby switch on power supply to Standby (0) position.

   For drives without status/control panel set On/Standby switch on power supply to Standby (0) position.

4. Remove front panel as follows:

   For drives with status/control panel:

   a. Remove the two screws (left side of front panel) securing status/control panel to front panel.

   b. Disconnect jumper cable from P13 while removing status/control panel from front panel.

   c. Remove filter from front panel.

   d. Remove the two screws (right side of front panel) securing front panel to inner drawer and remove front panel from drawer.

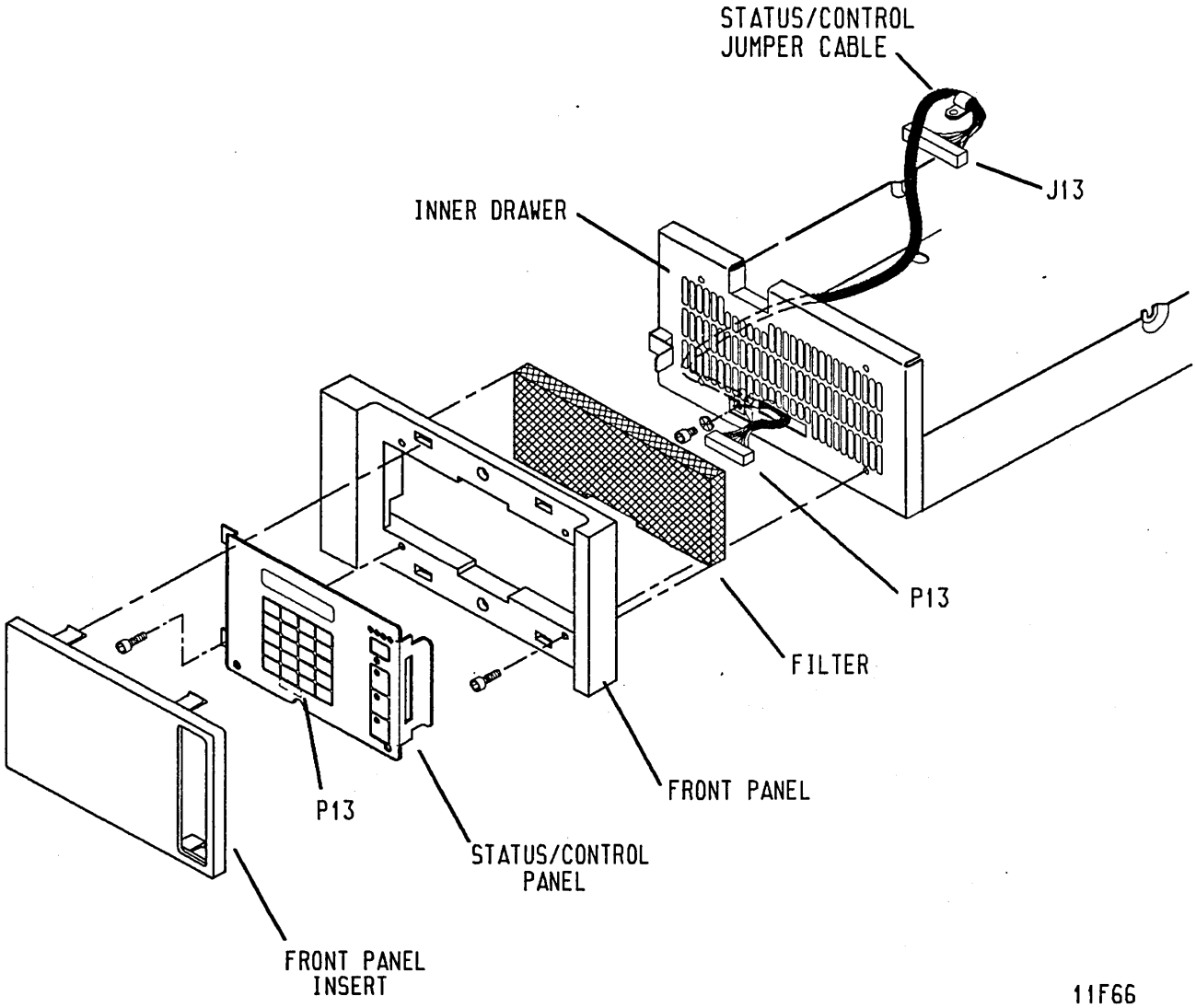


Figure 5-2. Front Panel Removal & Replacement

For drives without status/control panel:

a. Remove filter from front panel.

b. Remove screws securing front panel to inner drawer and remove front panel from drawer.

REPLACEMENT

NOTE

When installing the front panel, ensure that the overhang covers the rack frame (vertical support). If left and right hand inner drawers are interchanged in the 2X drawer, rotate the front panels 180 degrees.

1. Install front panel as follows (see figure 5-2):

   For drives with status/control panel:

   a. Align top edge of front panel to top edge of inner drawer.

   b. Secure front panel into place with the two screws on right side of front panel.

   c. Place filter in front panel.

   d. Connect jumper cable to P13 while attaching status/ control panel to front panel and secure with screws.

   e. Install front panel insert.

   For drives without status/control panel:

   a. Align top edge of front panel to top edge of inner drawer.

   b. Secure front panel into place with screws.

   c. Place filter in front panel.

   d. Install front panel insert.

2. Set On/Standby switch on power supply to On (1) position.

3. Push 2X drawer back to closed position in rack.

5201 - FAN REMOVAL & REPLACEMENT

This procedure describes how to remove and replace the cooling fan (see figure 5-3).

REMOVAL

1. Perform top cover removal procedure (5101).
2. Place inner drawer back into 2X drawer and push 2X drawer back to closed position in rack.
3. Disconnect ac power cable from site power source.
4. Disconnect P15 (fan connector) from J15 (B) (pins 14 and 15) on control board (_WAX).
5. Remove screws securing fan to bracket and remove fan from drive. Retain fan guard for use with replacement fan.

REPLACEMENT

1. Orient fan and fan guard to bracket as shown in figure 5-3 (note direction of air flow) and secure into place with screws.
2. Connect P15 (fan connector) to J15 (B) (pins 14 and 15) on control board.
3. Connect ac power cord to site power.
4. Push 2X drawer release latch to the right and extend 2X drawer to fully extended position.
5. Perform top cover replacement procedure (5101).

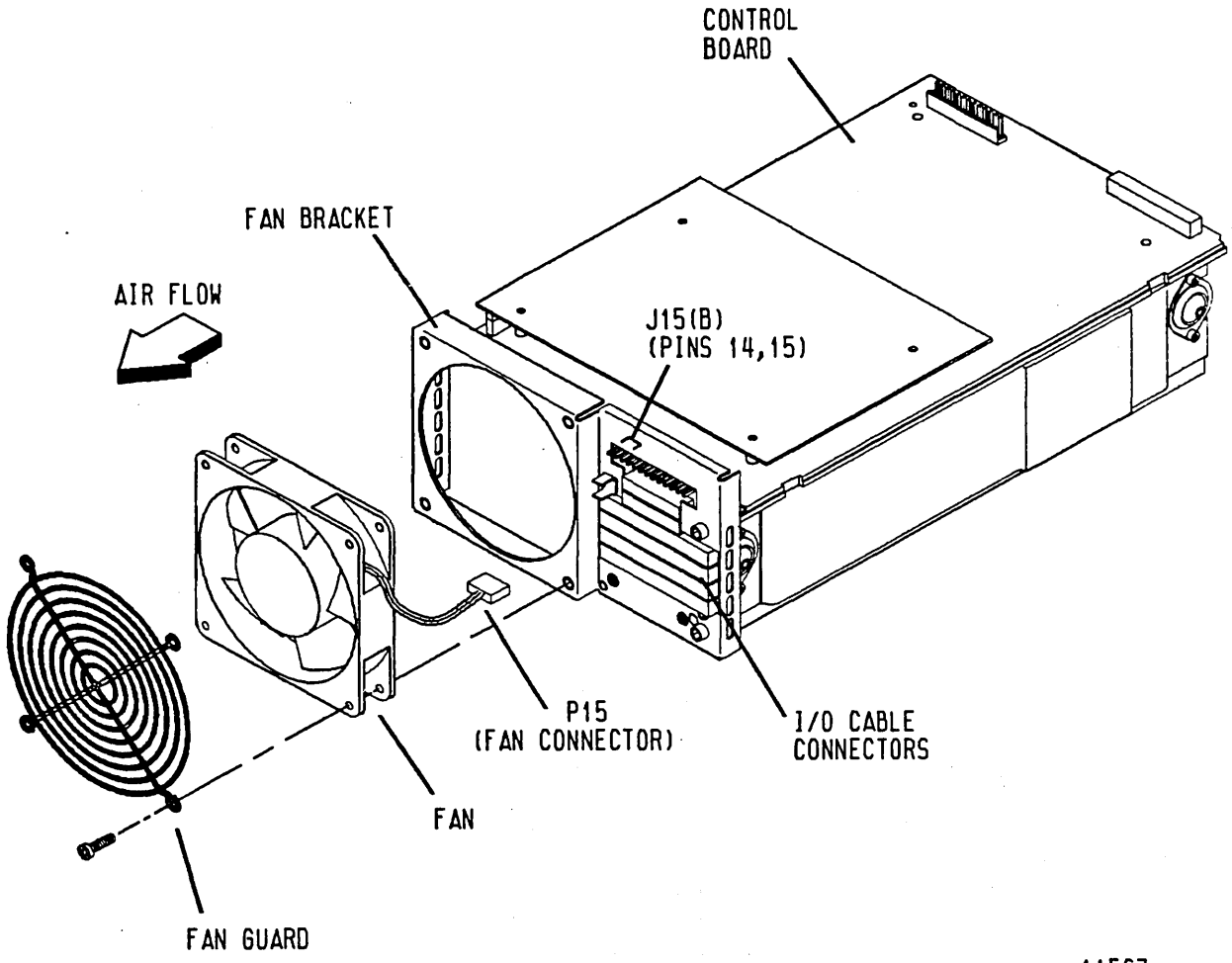


Figure 5-3. Fan Removal and Replacement

5202 - STATUS/CONTROL PANEL REMOVAL & REPLACEMENT

The status/control panel (located behind front panel insert) cannot be repaired. It must be replaced as an assembly. The following procedure describes removal and replacement of the status/control panel.

REMOVAL

1. Remove front panel insert from each drive (see figure 5-4).

   NOTE

   The release latch on the left-hand drive locks the 2X drawer in the rack. The release latch on the right-hand drive has no function.

2. Push 2X drawer release latch to the right and extend 2X drawer to gain access to On/Standby switch on power supply.

3. Remove power from drive as follows:

   a. Press START switch to stop the drive.

   b. Wait for Ready indicator (on START switch) to stop flashing; then, set On/Standby switch on power supply to Standby (0) position.

4. Remove screws securing status/control panel to front panel.

5. Disconnect jumper cable from P13 while removing status/control panel from front panel.

REPLACEMENT

1. Connect jumper cable to P13 while attaching status/control panel to front panel and secure with screws (see figure 5-4).

2. Set On/Standby switch on power supply to On (1) position.

3. Push 2X drawer to closed position in rack.

4. Install front panel insert.

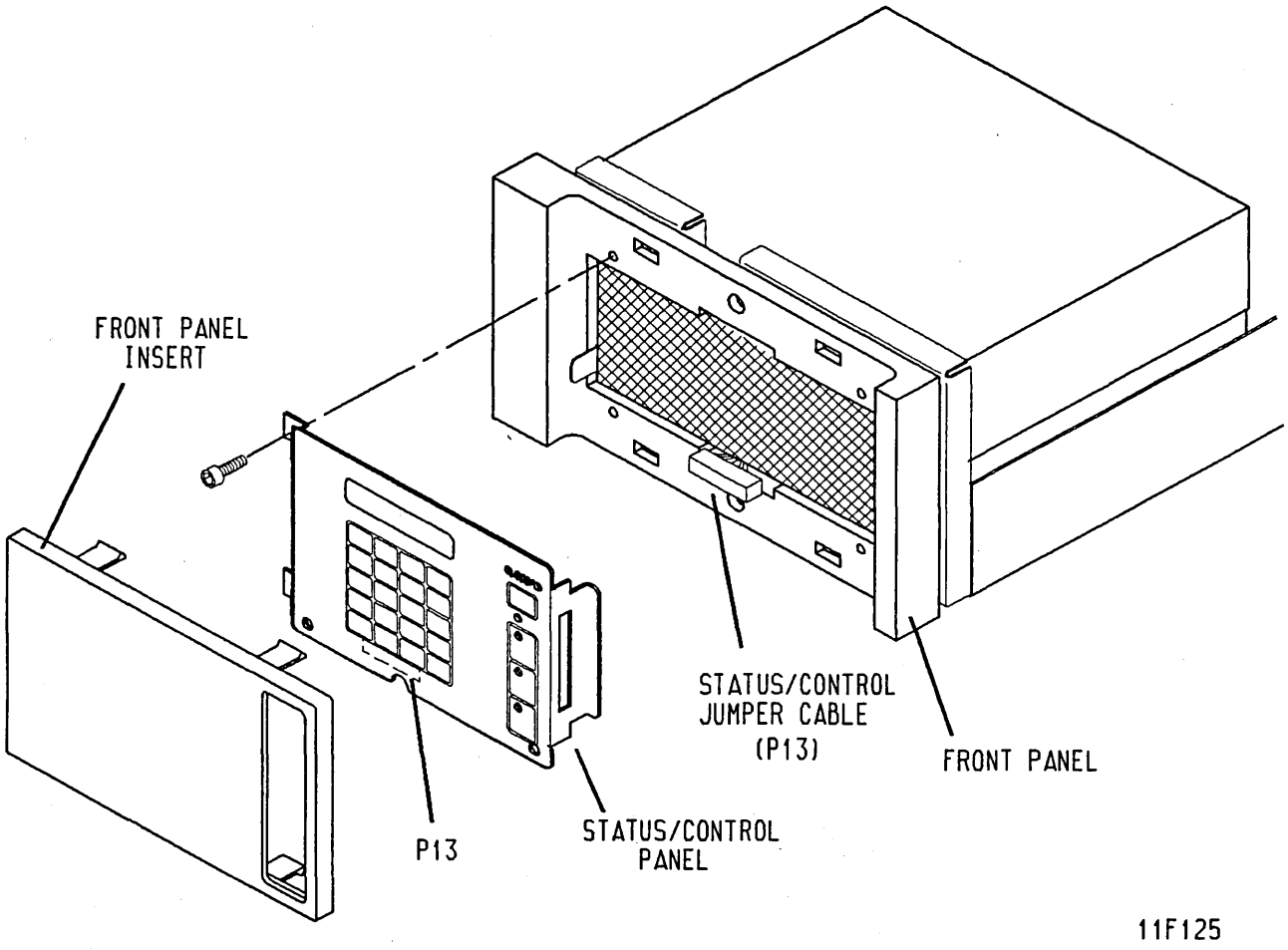


Figure 5-4. Status/Control Panel Removal & Replacement

5203 - POWER SUPPLY REMOVAL & REPLACEMENT

The following procedure provides instructions for removing and replacing the power supply when it is mounted in line with the drive (see figure 5-5).

REMOVAL

1. Perform top cover removal procedure (5101).
2. Place inner drawer back into 2X drawer and push 2X drawer back to closed position in rack.
3. Remove I/O cover and cable clamps from I/O cable bracket.

CAUTION

Remove terminators by hand. They could be damaged if a pliers or other tool is used.

4. Disconnect I/O cables, terminators, and system ground strap from drive.
5. Disconnect ac power cable from site power.
6. Push 2X drawer release latch to the right and extend 2X drawer to fully extended position.
7. Push 2X drawer release latch to the right, lift inner drawer up and remove it from 2X drawer. Place inner drawer on work table.
8. Disconnect dc power cable from J15 (A) on control board (_WAX).
9. Disconnect dc ground strap from module.
10. Remove screws securing power supply to inner drawer.
11. Disconnect ac power cable from ac input connector J1 while removing power supply from inner drawer.
12. Disconnect dc ground strap from power supply.
13. Disconnect dc power cable from J15 on power supply.

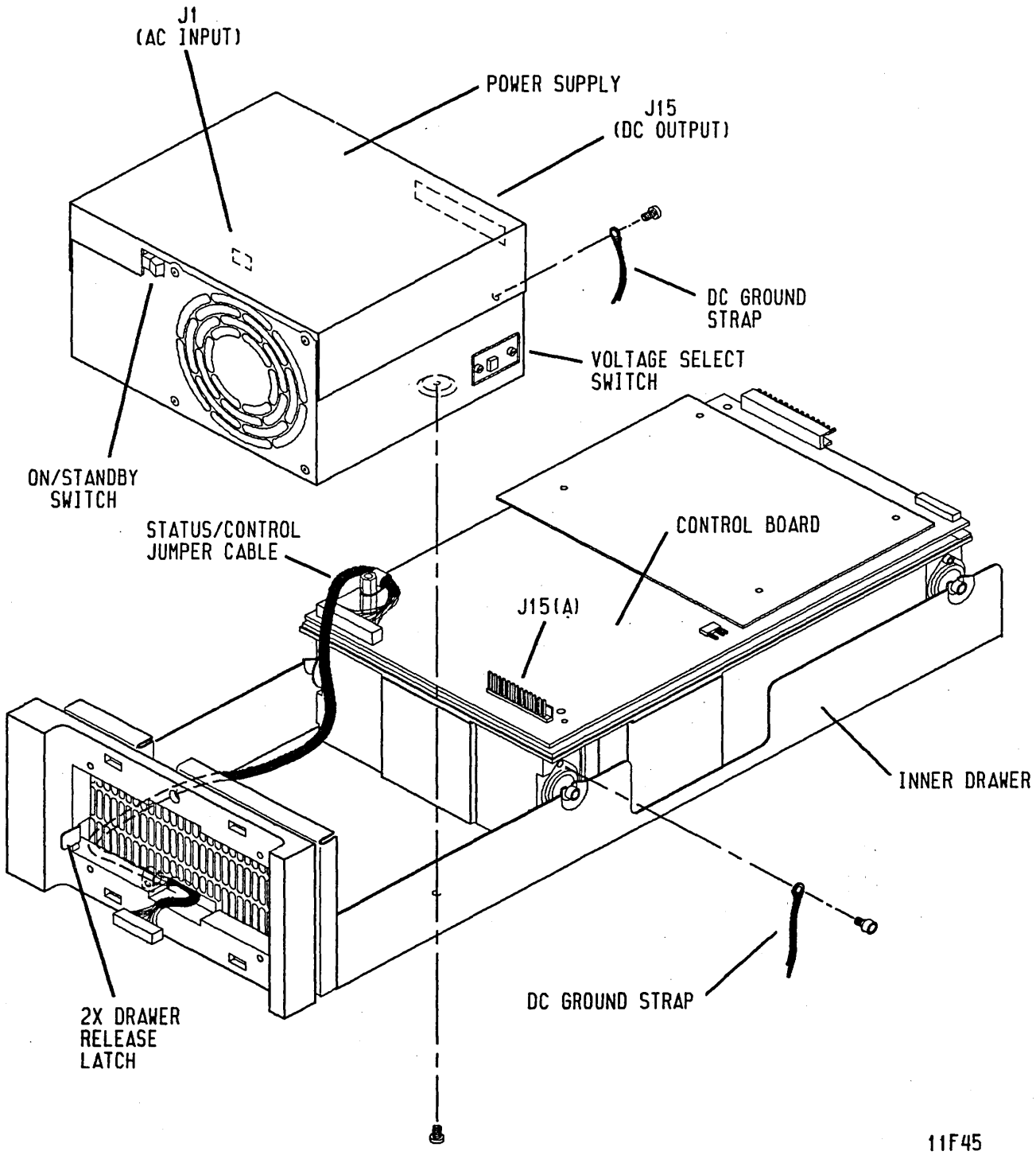


Figure 5-5. Power Supply Removal & Replacement

REPLACEMENT

1. Ensure voltage select switch is set to desired voltage range. See hardware maintenance manual, volume 1, for instructions on setting voltage select switch.

2. Connect dc power cable to J15 on power supply (see figure 5-5).

3. Connect dc ground strap to power supply.

NOTE

Ensure that the status/control jumper cable (shown in figure 5-5) does not interfere with the power supply as it is placed into position in inner drawer.

4. Connect ac power cable to ac input connector J1, while placing power supply into position in inner drawer.

5. Secure power supply to inner drawer with screws.

6. Connect dc ground strap to module.

7. Connect dc power cable to J15 (A) on control board (_WAX).

CAUTION

When replacing top cover, use care to avoid damaging logic boards.

8. Place top cover on drive and secure with screws.
9. Place inner drawer in 2X drawer and secure with locking screw.
10. Push 2X drawer back to closed position in rack.
11. Connect I/O cables and terminators to drive connectors, and attach strain relief clamp to cable bracket.
12. Attach I/O cable cover and grounding clamp to cable bracket.
13. Connect system ground strap to drive rear panel.
14. Connect ac power cord to site power.
15. Push 2X drawer release latch to the right and extend 2X drawer to gain access to On/Standby switch on power supply.
16. Set On/Standby switch on power supply to On (1) position.
17. Push 2X drawer back to closed position in rack.
18. Install front panel insert.

5204 - MODULE REMOVAL & REPLACEMENT

This procedure describes removal and replacement of the module.

REMOVAL

1. Perform entire drive removal procedure (5102), except for removing I/O cable bracket from rear panel.
2. Perform control board removal procedure (5303).

REPLACEMENT

1. Perform control board replacement procedure (5303).
2. Perform entire drive replacement procedure (5102).

5205 - CARRIAGE LATCH ELECTROMAGNET REMOVAL, REPLACEMENT & ADJUSTMENT

The carriage latch electromagnet unlocks the carriage inside the module during first seek (load) operations. It is located on the bottom side of the module. The adhesive covers, protecting the electromagnet and cable, must be replaced with new covers whenever the old covers are removed. See hardware maintenance manual, volume 1, for replacement part numbers.

REMOVAL

1. Perform entire drive removal procedure (5102).
2. Place module on its side, as shown in figure 5-6.
3. Peel off electromagnet and cable covers from module. Remove any adhesive left on module by old covers.
4. Disconnect P25 from J25 on control board (_WAX).
5. Remove screws securing electromagnet to module and remove electromagnet from module.

REPLACEMENT

1. Place electromagnet into position on module, as shown in figure 5-6.
2. Loosely, attach electromagnet to module with washers and screws.
3. Connect P25 to J25 on control board (_WAX).
4. Route electromagnet cable into position, in notch on module, and attach new cable cover to module.
5. Perform electromagnet adjustment procedure, starting with step 5.

ADJUSTMENT

1. Perform entire drive removal procedure (5102).
2. Place module on its side, as shown in figure 5-6.
3. Peel off electromagnet cover from module. Remove any adhesive left on module by old cover.
4. Loosen screws securing electromagnet to module.

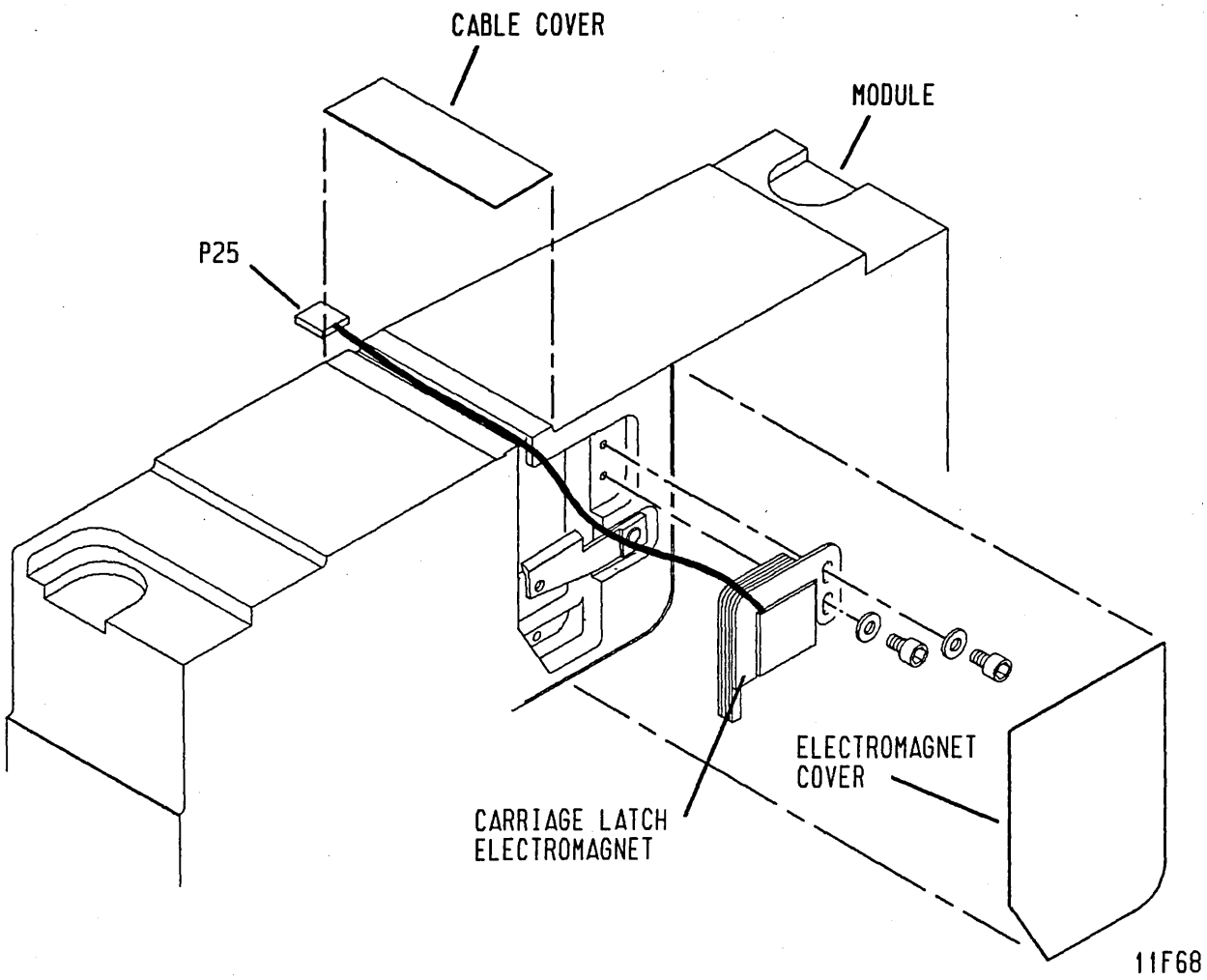


Figure 5-6. Carriage Latch Electromagnet Removal & Replacement

5. Insert alignment tool between electromagnet and carriage latch arm, as shown in figure 5-7.

6. Move electromagnet towards end of carriage latch arm to set gap "A" (end gap), then allow the weight of the electromagnet to rest squarely on the alignment tool to set gap "B" (striker gap).

7. Hold the electromagnet in this position and tighten screws to secure into place.

8. Remove alignment tool, then re-insert alignment tool to ensure gap is correct.

9. After the gap has been checked, remove the alignment tool and attach new electromagnet cover to module.

10. Perform entire drive replacement procedure (5102).

11. Start the drive in either Remote or Local mode.

12. Ensure that the drive completes a first seek (load) operation.

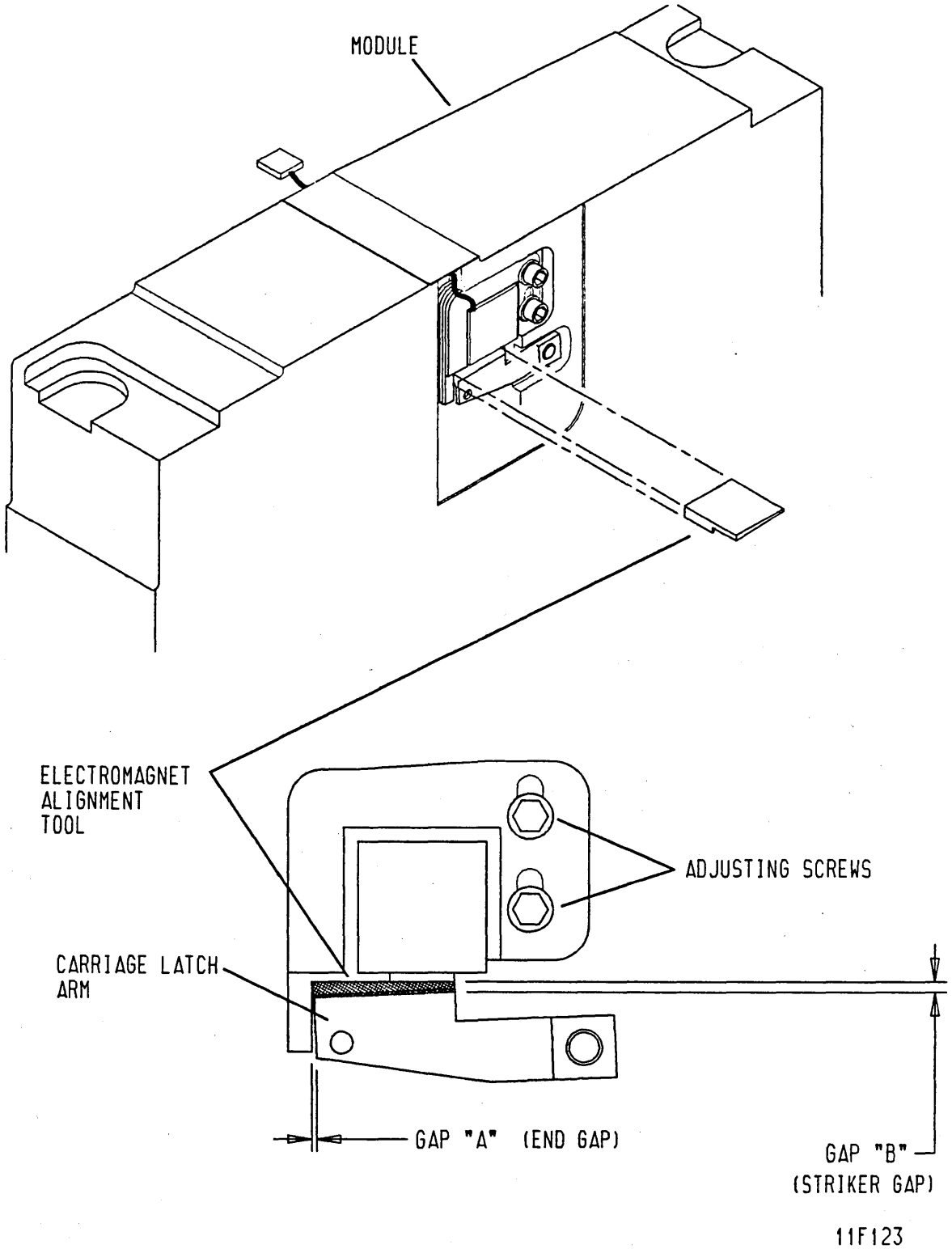


Figure 5-7. Carriage Latch Electromagnet Adjustment

5301 - READ/WRITE BOARD (–VYX) REMOVAL & REPLACEMENT

This procedure describes removal and replacement of the read/write board.

REMOVAL

1. Perform top cover removal procedure (5101).
2. Remove screws securing read/write board to control board (_WAX) (see figure 5-8).
3. Grasp each end of read/write board edge (next to J28 and P27 connectors).
4. Carefully, lift read/write board off control board.

REPLACEMENT

1. Align read/write board connectors to control board (_WAX) connectors (P28 to J28 and P27 to J27) and push down on read/write board (see figure 5-8).
2. Secure read/write board into place with screws.
3. Perform top cover replacement procedure (5101).

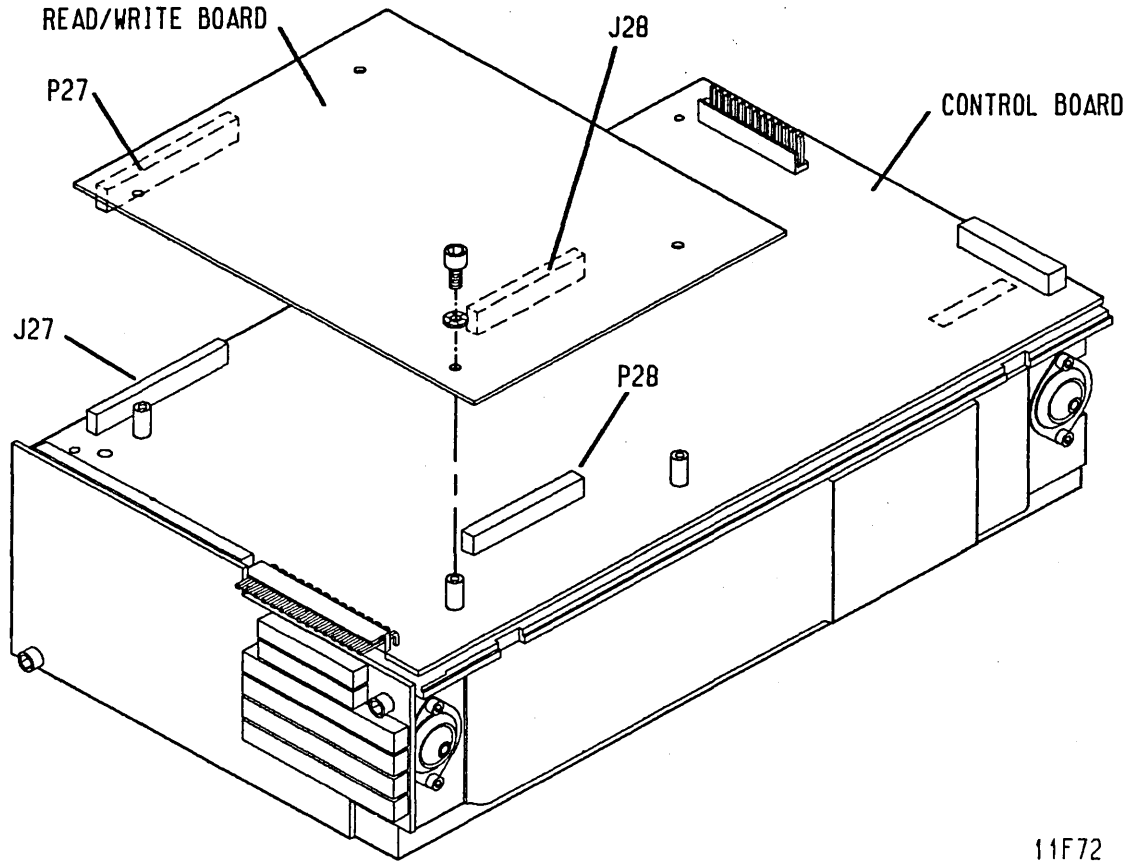


Figure 5-8. Read/Write Board (_VYX) Removal & Replacement

5302 - I/O BOARD (_VRX) REMOVAL & REPLACEMENT

This procedure describes removal and replacement of the I/O board.

REMOVAL

1. Perform top cover removal procedure (5101).
2. Place inner drawer back into 2X drawer and push 2X drawer back to closed position in rack.
3. Remove I/O cover and cable clamps from I/O cable bracket.

CAUTION

Remove terminators by hand. They could be damaged if a pliers or other tool is used.

3. Disconnect I/O cables and terminators from drive.
4. For drives with fan on rear panel, disconnect P15 (fan connector) from J15 (B) (pins 14 and 15) on control board (_WAX).
5. Remove screws securing rear panel and I/O board to drive (see figure 5-9).
6. Remove rear panel from drive. Retain panel and hardware.
7. Remove I/O board by disconnecting J20 from P20 on control board.

REPLACEMENT

1. Ensure that all circuit board switches are set either to match removed board or as indicated in the installation section of hardware maintenance manual, volume 1.
2. Align J20 on I/O board to P20 on control board (_WAX) and push the two connectors together (see figure 5-9).
3. Align rear panel to I/O board and secure in place with screws.
4. For drives with fan on rear panel, connect P15 (fan connector) to J15 (B) (pins 14 and 15) on control board.

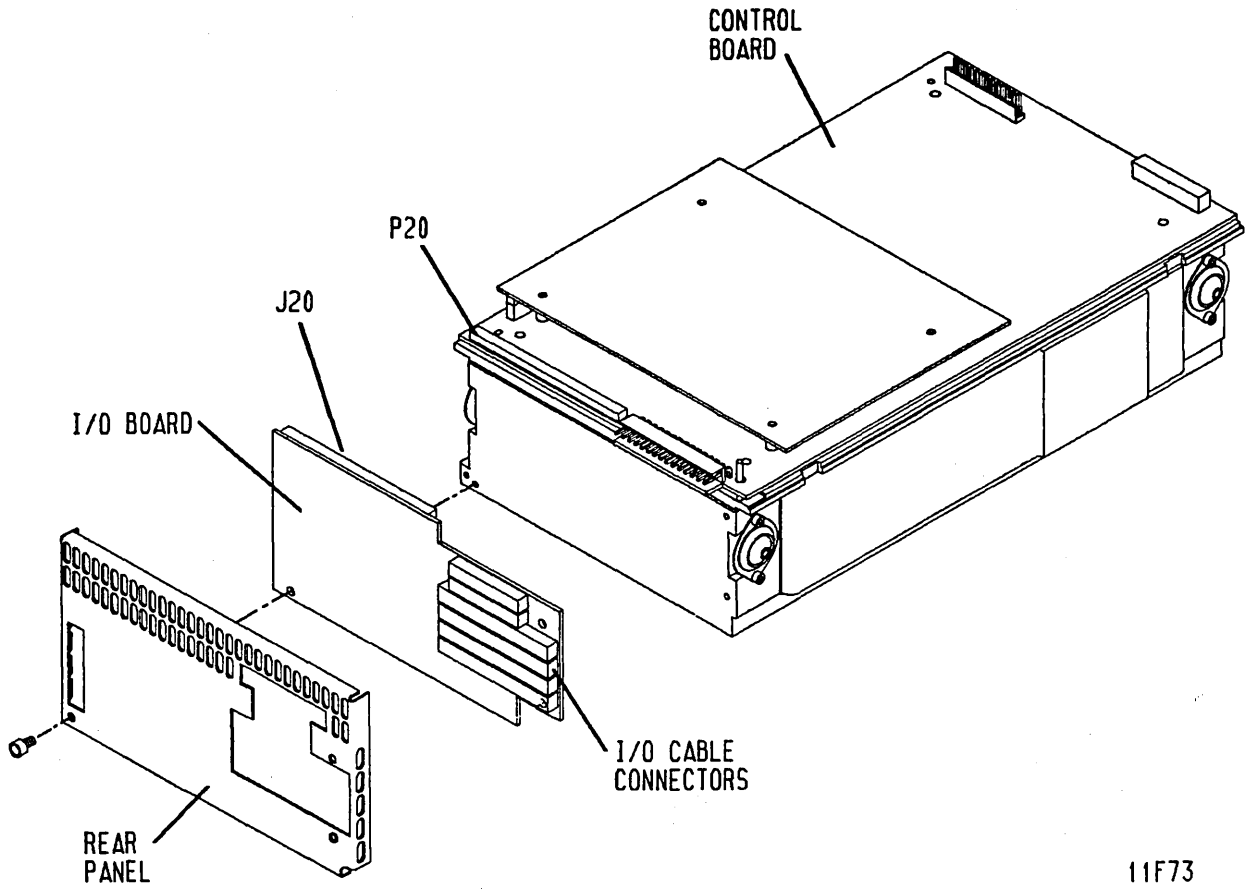


Figure 5-9. I/O Board (_VRX) Removal & Replacement

5. Connect I/O cables and terminators to drive connectors, and attach strain relief clamp to cable bracket.

6. Attach I/O cable cover and grounding clamp to cable bracket.

7. Perform top cover replacement procedure (5101).

5303 - CONTROL BOARD (–WAX) REMOVAL & REPLACEMENT

This procedure describes removal and replacement of the control board.

REMOVAL

1. Perform read/write board removal procedure (5301).
2. Perform I/O board removal procedure (5302).
3. Disconnect P25 from J25, J13 from J13, and P15 from J15 (A) (or J15 B if power supply is mounted in a remote location) on control board (see figure 5-10).
4. For drives with cooling fan mounted to rear panel, disconnect P15 from J15 (B) pins 14 and 15 on control board as shown in figure 5-10.
5. Remove screws and standoffs securing control board to module.

CAUTION

Pins on P24 and P28 on control board are not protected in a connector. Be careful not to bend pins after control board is removed from module or they will not align properly when attaching board to module.

6. Disconnect P24 from J24 and P28 from J28, by carefully lifting up on board to remove it from module.

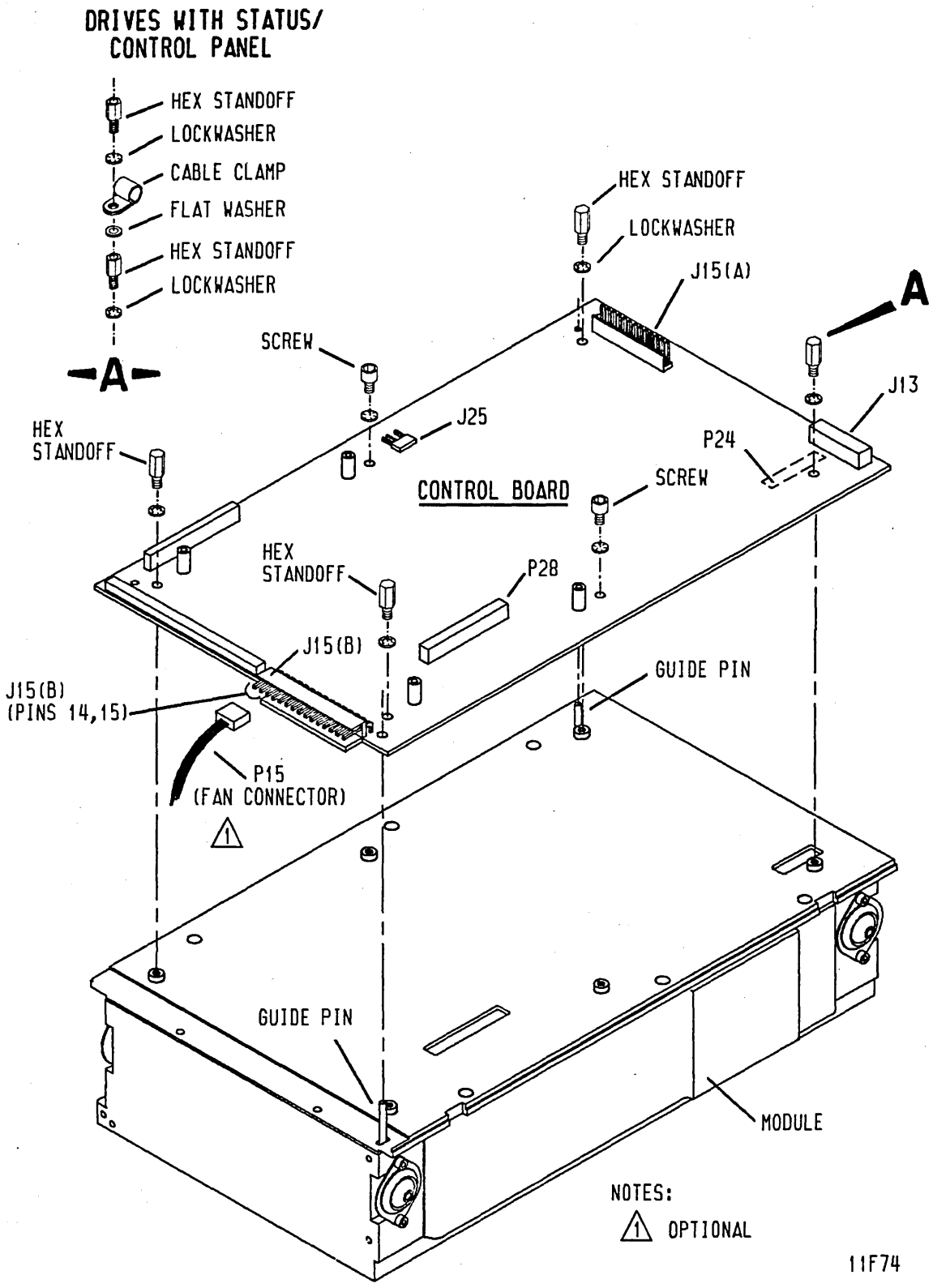


Figure 5-10. Control Board (_WAX) Removal & Replacement

CAUTION

Ensure that there are no bent pins on P24 and P28 on control board prior to attaching board to module.

1. Ensure that all circuit board switches are set either to match removed board or as indicated in the installation section of hardware maintenance manual, volume 1.

2. Place control board on module guide pins (see figure 5-10).

3. Align P24 to J24 and P28 to J28 and push down to connect board to module.

4. Secure control board to module with screws and standoffs.

5. Connect P25 to J25, P13 to J13, and P15 to J15 (A) (or J15 B if power supply is mounted in a remote location) on control board.

6. For drives with cooling fan mounted to rear panel, connect P15 to J15 (B) pins 14 and 15 on control board as shown in figure 5-10.

7. Perform read/write board replacement procedure (5301).

8. Perform I/O board replacement procedure (5302),

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