83324510

CONTROL DATA

CDC® FIXED STORAGE DRIVE

PA5A1

PA5A2

THEORY OF OPERATION

GENERAL MAINTENANCE INFORMATION

TROUBLE ANALYSIS

ELECTRICAL CHECKS

REPAIR AND REPLACEMENT

Volume 2

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
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Address comments concerning this manual to:

Control Data Corporation
Twin Cities Disk Division
Customer Documentation Dept.
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Minnetonka, Mn. 55343

or use Comment Sheet in the back of this manual.

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PREFACE

This manual contains maintenance information for the CONTROL DATA® PA5A1/PA5A2 Fixed Storage Drives (FSDs). It is prepared for customer engineers and other technical personnel directly involved with maintaining the FSD.

The information in this manual is presented as follows:

Section 1 - Theory of Operation. Describes power functions, electromechanical functions, interface, unit selection, servo surface decoding, sector detection, seek functions, head selection, read/write functions, and fault detection.

Section 2 - General Maintenance Information. Contains information on warnings and precautions, maintenance tools and materials, testing the drive, and accessing the drive for maintenance.

Section 3 - Trouble Analysis. Contains procedures and information to assist in troubleshooting the drive.

Section 4 - Electrical Checks. Provides electrical test procedures.

Section 5 - Repair and Replacement. Contains procedures and information on the replacement and adjustment of drive assemblies.

The following manuals apply to the FSD and are available from Control Data Corporation, Literature Distribution Services, 308 North Dale Street, St. Paul, MN 55103:

Publication No.	Title
83324500	PA5A1/PA5A2 Hardware Maintenance Manual, Volume 1 (contains general description, operation, installation and checkout information, and parts data)

(Continued on Next Page)

Publication No.	Title
83324510	PA5A1/PA5A2 Hardware Maintenance Manual, Volume 2 (contains theory of operation and maintenance)
83324640	PA5A1/PA5A2 Hardware Maintenance Manual, Volume 3 (contains diagrams)
83325440	RSD/FSD Power Supply Diagrams Manual (contains power supply diagrams, which are intended for reference use only)
83325310	A Guide for the Disk Drive Operator
83325360	Reference Card (provides status code and diagnostics information)
83322440	CDC Microcircuits, Volume 1 (provides functional descriptions for integrated circuits)
83324440	CDC Microcircuits, Volume 2 (provides functional descriptions for integrated circuits)

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IMPORTANT SAFETY INFORMATION AND PRECAUTIONS

Proper safety and repair is important to the safe, reliable operation of this unit. Service should be done by qualified personnel only. This maintenance manual describes procedures recommended by the manufacturer as effective methods of servicing the unit. Some of these procedures require the use of specially designed tools. For proper maintenance and safety, these specially designed tools should be used as recommended.

The procedures in this maintenance manual and labels on the unit contain warnings and cautions which must be carefully read and observed in order to minimize or eliminate the risk of personal injury. The warnings point out conditions or practices that are potentially hazardous to maintenance personnel. The cautions point out practices which, if disregarded, could damage the unit and make it unsafe for use.

For the safety of maintenance and operating personnel, the following precautions must be observed:

- Perform all maintenance by following the procedures given in this manual and using only CDC/MPI replacement parts.
- Read and observe all cautions and warnings provided in the procedures and labeled on the unit.
- Use the special tools called out in the maintenance procedures.
- Observe sound safety practices when performing maintenance.
- Use caution when troubleshooting a unit that has voltages present. Remove power from unit before servicing or replacing components.
- Wear safety glasses when servicing units.
- Wear safety shoes when removing or replacing heavy components.

It is also important to understand that these warnings and cautions are not exhaustive. The manufacturer could not possibly know, evaluate and advise maintenance personnel of all conceivable ways in which maintenance might be performed or the possible risk of each maintenance technique. Consequently, the manufacturer has not completed any such broad evaluation. Thus, any persons who use any non-approved maintenance procedure or tool must first satisfy themselves that neither their safety nor the unit performance will be jeopardized by the maintenance techniques they select.

ABBREVIATIONS

A	Ampere
ABV	Above
ac	Alternating Current
ADD	Address
ADDR	Address
ADJ	Adjust
ADRS	Address
AGC	Automatic Gain Control
ALT	Alternate
AM	Address Mark
AME	Address Mark Enable
AMP	Amplifier, Ampere
ASSY	Assembly
BLW	Below
C	Celsius
CB	Circuit Breaker
CDA	Complete Drive Assembly
CDC	Control Data Corporation
CH	Channel
CHK	Check
CLK	Clock
CLR	Clear
cm	Centimeter
CNTR	Counter
COMP	Comparator
CONT	Control
CONTD	Continued
CT	Center Tap
CYL	Cylinder
D/A	Digital to Analog
dc	Direct Current
DET	Detect
DIFF	Differential
DIV	Division
DLY	Delay
DRVR	Driver
ECL	Emitter Coupled Logic
ECO	Engineering Change Order
EN	Enable
ENBL	Enable

ABBREVIATIONS (Contd)

EXT	External
F	Fahrenheit, Fuse
FCO	Field Change Order
FDBK	Feedback
FIG	Figure
FLT	Fault
FSD	Fixed Storage Drive
ft	Foot
FTU	Field Test Unit
FWD	Forward
GND	Ground
HD	Head
HEX	Hexagon
Hg	Mercury
HR	High Resolution
HYST	Hysteresis
Hz	Hertz
IC	Integrated Circuit
IDENT	Identification
in	Inch
IND	Index
INTRPT	Interrupt
I/O	Input/Output
IPB	Illustrated Parts Breakdown
IPS	Inches per Second
kg	Kilogram
kPa	Kilopascal
kW	Kilowatt
lb	Pound
lbf	Pounds/Force
LED	Light Emitting Diode
LSI	Large Scale Integration
LTD	Lock to Data
m	Meter
MAX	Maximum
MB	Megabyte
MEM	Memory
MHz	Megahertz
mm	Millimeter

ABBREVIATIONS (Contd)

MPI	Magnetic Peripherals, Inc.
MPU	Microprocessor Unit
MRK	Mark
ms	Millisecond
MTR	Motor
mV	Millivolt
N	Newton
NC	No Connection
NORM	Normal
NRZ	Non Return to Zero
ns	Nanosecond
OC	On Cylinder
OS	One-Shot
OSC	Oscillator
P	Plug
PD	Peak Detect
pF	Picofarad
PG	Page
PHH	Phillips Head
PLO	Phase Lock Oscillator
PROC	Procedure
PROG	Programmable
PS	Power Supply
PWR	Power Supply
RCVR	Receiver
RD	Read
RDY	Ready
REF	Reference
REQ	Request
RES	Resolution
REV	Reverse, Revision
RGTR	Register
r/min	Revolutions Per Minute
RSD	Removable Storage Drive
RTZ	Return to Zero
R/W	Read/Write
s	Second
S/C	Series Code
SEC	Second
SEL	Select
SEQ	Sequence
SPD	Speed

ABBREVIATIONS (Contd)

SS	Sector Switch	W	Watts
T	Tracks to go	W/	With
TF	Thread Forming	W/O	Without
TIM	Timer	W PROT	Write Protect
TP	Test Point	W+R	Write or Read
TSP	Troubleshooting Procedure	W·R	Write and Read
TTL	Transistor-Transistor Logic	WRT	Write
V	Volts, Voltage	XFR	Transfer
Vbb	Bias Voltage	Ω	Ohms
VCC	Bias Voltage	$	Hexadecimal Address
VCO	Voltage Controlled Oscillator	uF	Microfarad
		us	Microsecond

SECTION 1

THEORY OF OPERATION

THEORY OF OPERATION 1

INTRODUCTION

The theory of operation section describes drive operations and the hardware used in performing them. It is divided into the following major areas (refer to figure 1-1):

- Power Functions - Describes how the drive provides the voltages necessary for drive operation.
- Electromechanical Functions - Provides a physical and functional description of the mechanical and electromechanical portions of the drive disk rotation, head positioning, and air flow systems.

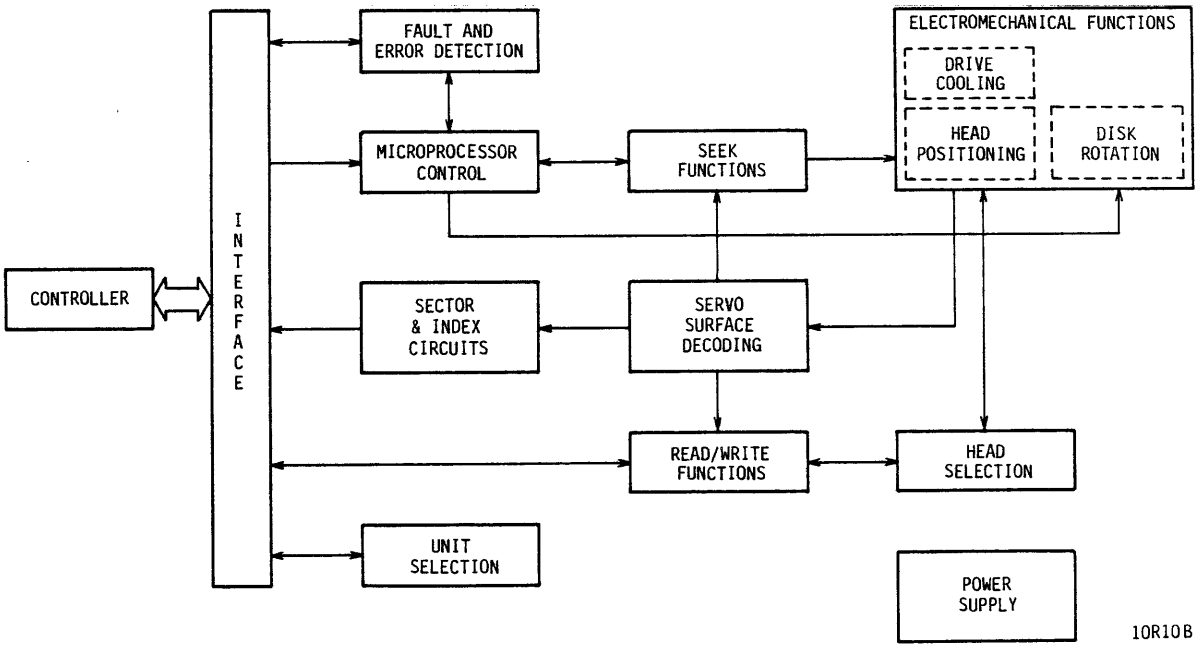


Figure 1-1. Drive Functional Block Diagram

- Interface - Describes the signal lines connecting the drive and controller. It also describes the I/O signals carried by these lines and how they are processed by the drive logic.

- Unit Selection - Explains how the controller logically selects the drive so the drive will respond to controller commands.

- Servo Surface Decoding - Explains how the decoding of the data read from the servo surface by the servo head is used to locate the radial position of the heads during a seek movement, the rotational position of the disks (indicated by the Index signal) when the heads are on track, and the exact speed of the disks (indicated by the 1.612 MHz clock signal).

- Sector Detection - Explains how the drive derives the sector pulses that are used to determine the angular position, with respect to index, of the read/write heads.

- Seek Functions - Explains how the servo logic controls the movements of the head positioning mechanism in positioning the heads over the disks.

- Head Selection - Explains the head selection process.

- Read/Write Functions - Describes how the drive processes the data that it reads from and writes on the disk.

- Fault Detection - Describes the conditions that the drive interprets as faults.

The descriptions in this section are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software.

Functional descriptions are frequently accompanied by simplified logic and timing diagrams. These are useful both for instructional purposes and as an aid in troubleshooting. However, they have been simplified to illustrate the principles of operation. Therefore, the diagrams (and timing generated from them) in volume 3 of the hardware maintenance manual should take precedence over those in this section if there is a conflict between the two.

The four digit number in parentheses that are used on the simplified logic and flowcharts are logic diagram cross reference numbers. They indicate the logic page(s) where the function or operation can be found.

POWER FUNCTIONS

GENERAL

Power functions are processes that take place within the power supply and the drive when the drive is powered up and powered down. These processes depend on whether the drive is set up for local or remote operation. In all cases, the power up and power down sequences are controlled through MPU programming that monitors whether start conditions are present and whether certain interlock and operating conditions are satisfactory. The following areas of the power functions will be discussed in detail:

- Power Distribution -- Describes how power is distributed to the drive circuitry.
- Local/Remote Power Sequencing -- Explains how the drive may be powered up either at the drive or by the controller.
- Power On Sequence -- Describes how the drive circuitry is initialized when power is applied and how the drive is prepared for normal operation.
- Power Off Sequence -- Describes how the drive is powered down, including unloading the heads and stopping the disk rotation.

POWER DISTRIBUTION

The power supply, provides the drive with basic dc supply voltages when circuit breaker CB1 is placed in the ON position. The drive itself has no ac power requirements. All drive circuitry, including the electronics, cooling fan, and drive motor, is operated with the dc supply voltages. The ac power cable connects the power supply (through CB1) to site ac power. The power supply can be conditioned for operation with any standard ac input voltage, as described in the Installation and Checkout section of Hardware Maintenance Manual, Volume 1.

The dc power cable connects the power supply to the drive. When CB1 is ON, this cable transmits four basic dc supply voltages to the drive electronics. These voltages are +5 V, -5 V, +24 V, and -24 V. The -5, -24, and +24 V supplies are protected against overload by pop-out circuit breakers on the power supply. The dc power cable also contains signal lines, which are enabled by control circuitry in the drive, to switch on 40 V dc power to the drive motor and produce disk rotation.

There are secondary power supplies on the drive's Control Board that develop additional bias voltages for certain integrated circuits. One supply steps down the +24 V input and develops a regulated +15 V source. Another supply steps down the -24 V input and develops a regulated -15 V source. A third supply steps down the -15 V supply to develop a regulated bias of -8.3 V for the servo preamp chip.

The drive has circuitry that monitors the various supply voltages and disables write and/or servo functions when dc power is unreliable. For more information about voltage faults, refer to the Fault and Error Conditions discussion.

LOCAL/REMOTE POWER SEQUENCING

The local/remote feature selects whether or not the controller can control starting and stopping the drive motor. Part of drive installation is setting the LOCAL/REMOTE switch (on the drive I/O Board) for either local or remote operation. The LOCAL/REMOTE switch setting determines start conditions for the drive motor during power up. With the LOCAL/REMOTE switch in LOCAL, start conditions require only that the START switch is in the On position. With the LOCAL/REMOTE switch in REMOTE, start conditions require that the START switch is in the On position and that the controller has activated the Sequence Hold signal.

In a system of several drives set up for remote operation, the Sequence Hold command affects all drives simultaneously. When Sequence Hold goes active, it enables all drives to start their drive motors at the same time. When Sequence Hold goes inactive, it causes all drives to stop their drive motors at the same time.

POWER ON SEQUENCE

The power on sequence takes place in two steps. Power on initialization occurs when dc power is applied to the drive. Following successful initialization, a load operation occurs each time that start conditions become available. Figure 1-2 is a simplified diagram of the power on circuitry, and figure 1-3 is a flowchart of the sequence. The following paragraphs describe power on initialization in detail and summarize the load operation. More information about load operations is given under Seek Functions.

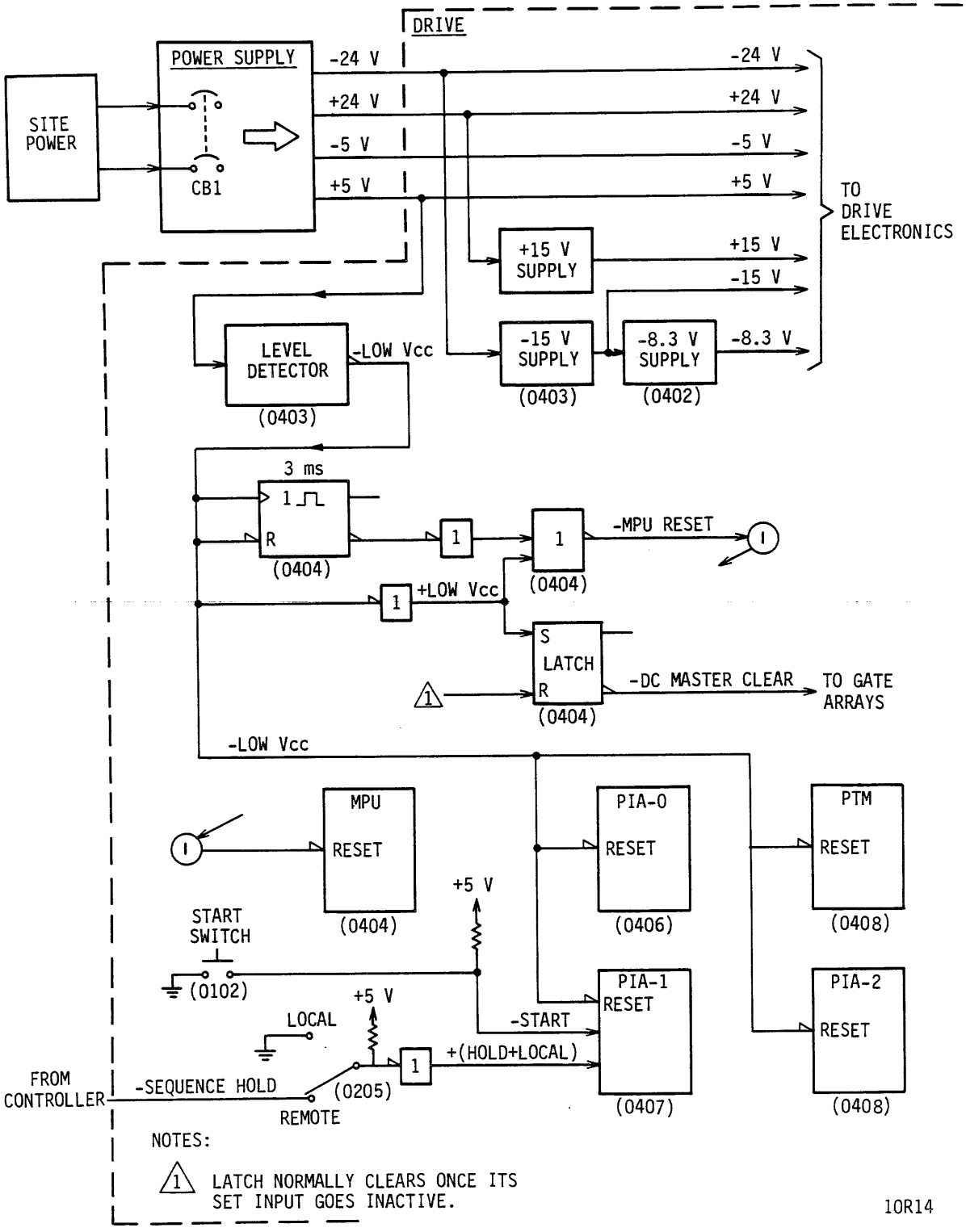


Figure 1-2. Power On Circuitry

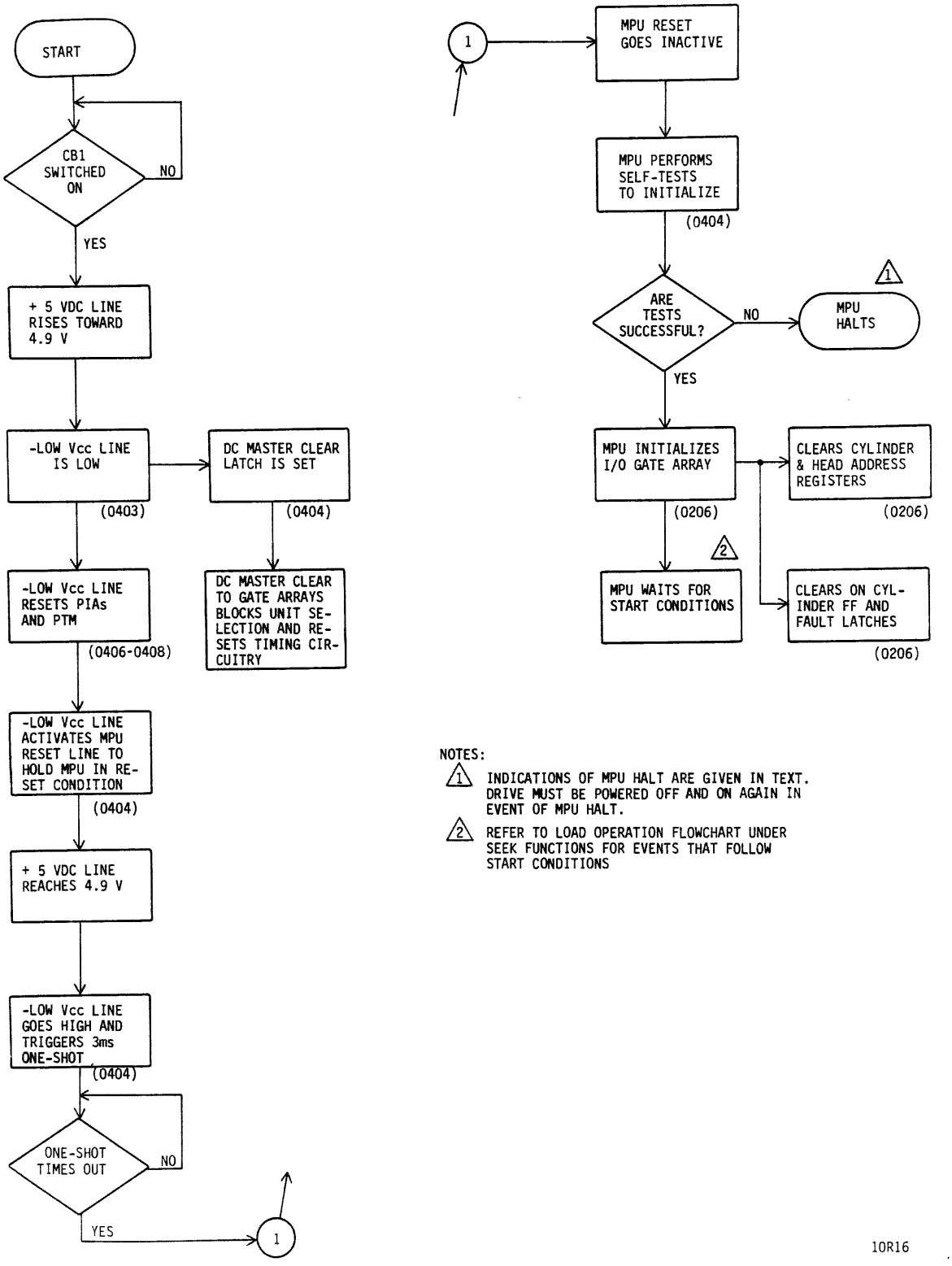


Figure 1-3. Power On Sequence Flowchart

Placing power supply circuit breaker CB1 ON enables dc power to the drive. A level detector on the control board monitors the +5 Vdc input from the power supply and sets the -Low Vcc line high when this input reaches +4.9 V. Until this time, the DC Master Clear latch is set, and its output, the -DC Master Clear signal, remains low. In the Sector Counter Gate Array, the low -DC Master Clear signal resets the sector counter and the servo pattern decode circuitry. In the Address Decode Gate Array, the low -DC Master Clear signal disables the interface by blocking unit selection, and it resets timing circuitry that develops Index and Cylinder pulses. In dual channel drives, the low -DC Master Clear signal blocks unit selection by either controller.

The -Reset line to the MPU goes low when -DC Master Clear goes low, and it is held low by a one-shot for about 3 ms after the -Low Vcc line goes high. When -Reset goes high, the MPU performs three self-test operations to initialize itself. These tests are as follows:

- The MPU performs a checksum calculation on the ROM contents. This test validates that the MPU's firmware instructions are readable.
- The MPU tests its internal RAM by writing information into it and reading it back.
- The MPU initializes its PIAs by sending data to them and reading it back.

If the first two tests fail, the MPU halts and all the individual fault LEDs on the control board remain lit. If the third test fails, the MPU tries to light the First Seek LED and halts. None of these tests can produce an operating panel FAULT indication, and there is no way to clear these faults except for turning CB1 OFF.

With the self-tests complete, the MPU initializes the circuitry within the I/O Gate Array. The MPU communicates with the I/O Gate Array via I/O Control lines 1, 2, and 3. The MPU pulses I/O Control lines 1 and 2 with a serial code that clears the Cylinder Address register (CAR), the Head Address register (HAR), the On Cylinder FF, and the Fault latches.

At this point, power on initialization is complete. Unless the +5 Vdc supply voltage drops, this process will not be repeated until dc power is removed and reapplied to the drive (via CB1). The MPU waits for start conditions by monitoring the START switch and (in remote operation) the Sequence Hold signal from the controller.

When start conditions are present, the MPU directs the load operation. The load operation energizes the drive motor to bring the disks up to speed and loads the heads to position them at track 0 on the disks. Details of the load operation are given under Seek Functions. When the load operation is complete, the drive waits for commands from the controller.

POWER OFF SEQUENCE

The power off sequence unloads the heads and stops the drive motor. There are two conditions that initiate a power off sequence. One is a loss of start conditions, and the other is a loss of dc power to the drive.

A loss of start conditions occurs when the START switch is pressed to release it from the Start position or (in remote operation) when the controller deactivates Sequence Hold. The MPU monitors the start conditions and directs an unload operation when they are removed. The unload operation (discussed under Seek Functions) uses servo control to move the heads completely inward over the landing zone. The heads are held in this position by a retract command until the actuator is locked by the actuator locking solenoid. The MPU then drops the Motor Run command to disable the Motor Speed Control, and the friction brake stops the drive motor. The drive remains in this condition until start conditions reappear.

A loss of dc power results when power supply circuit breaker CB1 is switched OFF or when there is a loss of site ac power. When the dc voltages drop, an emergency retract takes place under hardware control. The emergency retract operation (described under Seek Functions) requires no MPU intervention, and it uses voltage generated by the decelerating drive motor to drive the heads inward to the landing zone. When the heads have moved inward to the landing zone, the actuator locking solenoid automatically holds them in this position. With a loss of dc power, the drive motor loses its excitation and is stopped by the friction brake.

ELECTROMECHANICAL FUNCTIONS

GENERAL

Certain drive functions are a result of the electromechanical devices using drive power and working under the control of drive logic circuitry. These functions include disk rotation, head positioning, and drive cooling and ventilation.

DISK ROTATION

General

Disk rotation is accomplished by an electromechanical system that accelerates the disks to 3600 r/min during power up and stops disk rotation with friction braking during power down. The mechanical and electrical aspects of this system are discussed in the following paragraphs.

Mechanical Description

The mechanical components used for disk rotation are the spindle, the drive motor, and the brake.

Spindle

The disks are mounted on the spindle assembly. The spindle, like the disks, is part of the module. When the spindle is rotated by the drive motor, the disks rotate with the spindle.

Drive Motor

The FSD has a direct drive system for disk rotation with the drive motor mounted concentrically on the spindle. The motor has a three-phase stator surrounded by a four-pole rotor. The motor speed control (described in the next topic) provides pulsed excitation to the three stator windings. To keep the stator pulses in phase with rotor position, the speed control uses feedback from sensors located in the motor. These sensors employ the Hall Effect to sense flux reversals from the rotor magnets. As the rotor magnets pass each sensor, its output line toggles.

Electrical Description

General

Electrical operation of the drive motor is discussed in two functional areas:

- Motor Control System -- discusses how the drive motor is started and how its speed is regulated.
- Friction Motor Braking -- discusses how the drive motor is decelerated.

Motor Speed Control

The motor speed control regulates operation of the drive motor. Subject to interlocks, the microprocessor issues a command to start the drive motor during the power on sequence (see Power On Sequence discussion). The motor speed control activates the 40 V dc output of the power supply and uses this power source to excite the stator windings in the drive motor. The control and status lines between these system elements are shown in figure 1-4.

To start the drive motor, the microprocessor drops the -Motor Run line. The drive motor receives power as long as this line is held low. With the -Motor Run line low, the motor speed control issues the -Enable Motor Power command to switch on the 40 V dc output of the power supply.

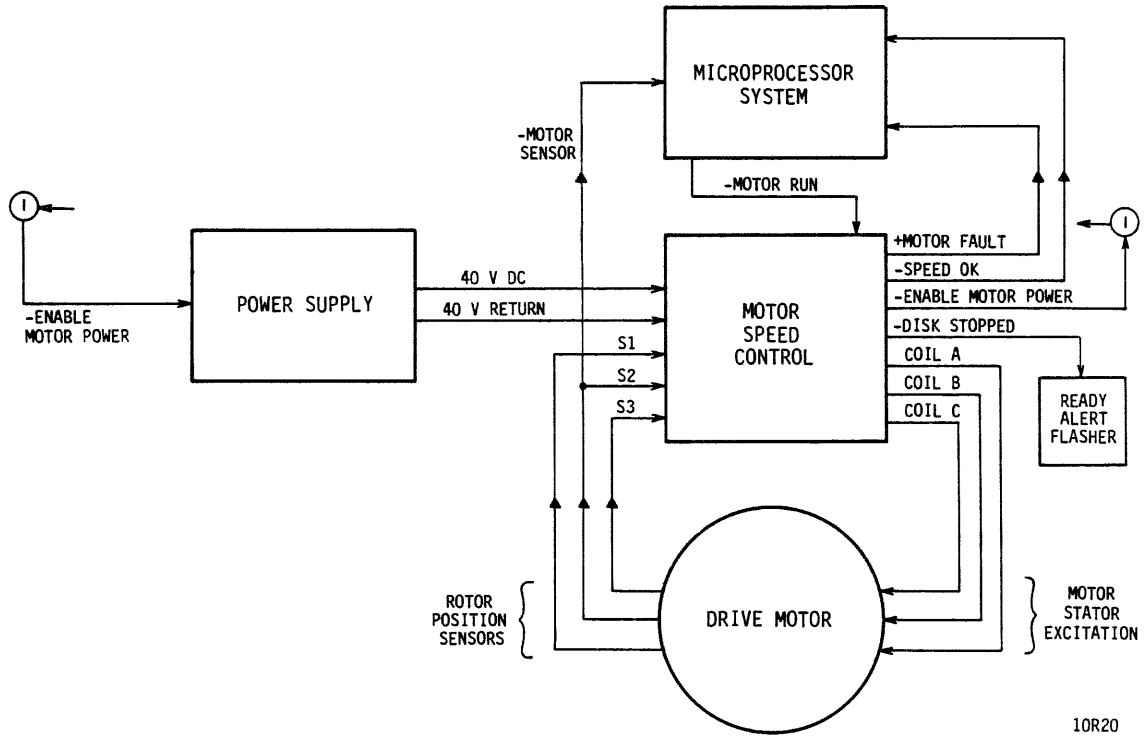


Figure 1-4. Motor Speed Control System Diagram

The motor speed control divides each shaft rotation of the motor into twelve 30° segments. During each segment, a current path is selected through two of the three stator coils. These stator excitations are timed so that, in each segment, the selected stators exert a counterclockwise torque on the permanent magnets of the rotor.

Rotational position of the motor shaft is relayed to the motor speed control by sensors S1, S2, and S3 located inside the motor. The sensors are positioned at 30° intervals. Each sensor employs the Hall Effect to output a digital level that switches when the polarity of the local magnetic field reverses. The waveforms of S1, S2, and S3 are shown in figure 1-5.

The motor speed control regulates motor speed by modulating the width of the pulses applied to the stator coils. The motor speed is kept within the following range: 3564 r/min (16.83 ms/rev) to 3636 r/min (16.49 ms/rev). The pulses have maximum width until the rotation time decreases to 16.83 ms. Then the pulse width decreases linearly to a zero value corresponding to a rotation time of 16.49 ms.

Figure 1-6 shows simplified logic for the motor speed control. The control modulates the motor pulses as follows: Once per rotation, a signal called +360° Pulse goes active. This signal triggers a 16.49 ms reference delay, derived by subdividing the 4 MHz clock in the motor speed control. This reference delay corresponds to one motor rotation at the maximum allowable speed. A comparator circuit outputs a pulse that is active from the end of the reference delay until the next 360° Pulse. The active time for the comparator output pulse determines the on-time of the +Drive Enable line during each 30° segment of motor rotation. Power is applied to the stator windings only when +Drive Enable is high. This condition is updated once per motor rotation, and the duty cycle of the motor is readjusted to keep the motor speed within its specified range.

Three status outputs are generated by the motor speed control and are used as follows:

- +Motor Fault -- indicates to the MPU that the drive motor has a bad magnetic sensor.
- -Speed OK -- indicates to the MPU that the drive motor speed is between 3564 and 3636 r/min and that no motor fault is present.
- -Disk Stopped -- indicates to the interlock circuitry that the last disk rotation exceeded two seconds.

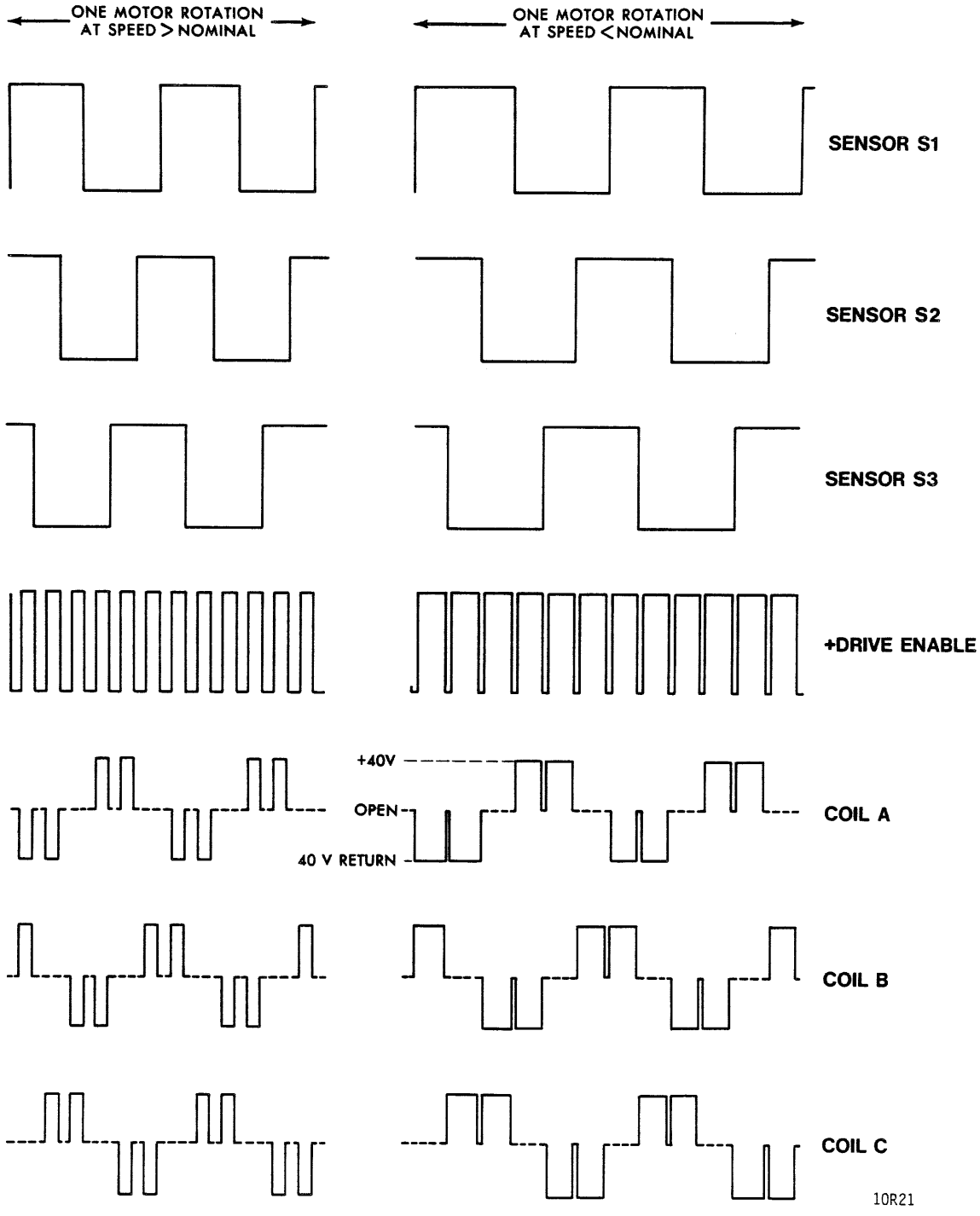


Figure 1-5. Speed Control Waveforms and Timing

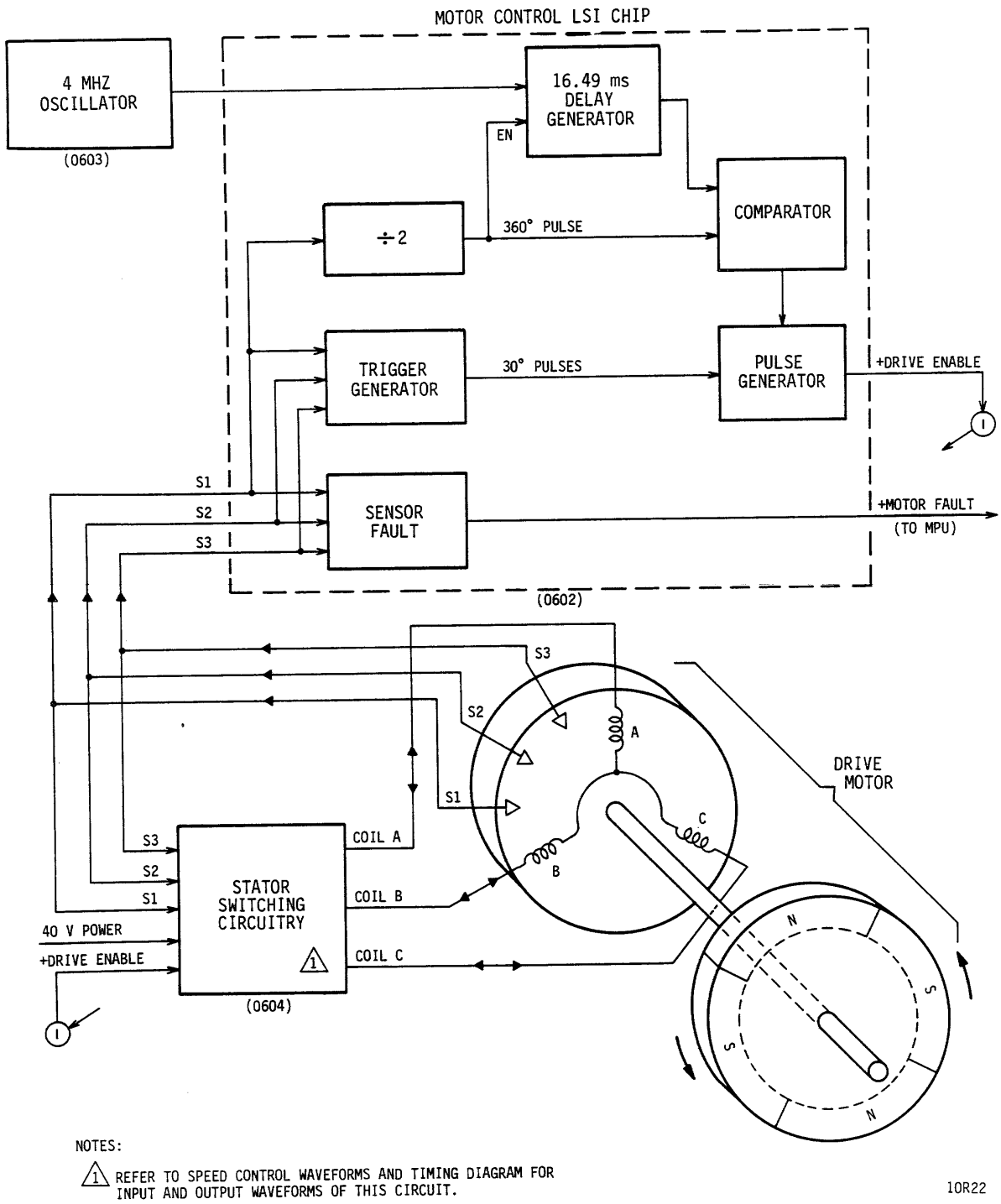


Figure 1-6. Motor Speed Control Simplified Logic

Friction Motor Braking

The drive motor decelerates during the power off sequence under control of the friction brake. A transistor switch on the motor speed control board energizes the brake during drive motor operation to release the brake and allow the motor to turn. The brake remains energized as long as the -Enable Power Supply control line is low. When the motor is powered down, this line goes high, deenergizing the brake and allowing it to contact the rotor in the drive motor.

The motor speed control board also has a provision for dynamic braking of the drive motor, but this is not used in the FSD. With the -Brake Control input to the Motor Control Gate Array tied low, the -Brake A and -Brake B lines from the gate array remain high to prevent any dynamic braking action.

The motor speed control activates the -Disk Stopped line to indicate that braking is complete. This output to the interlock circuitry turns off the flasher circuit for the Ready indicator to show that power down is complete.

HEAD POSITIONING

General

Data is written on and read from the disk by the heads . The drive must position the heads over a specific data track before a read or write operation can be performed. Head positioning is performed by the actuator mechanism which is an integral part of the drive. The actuator is controlled by inputs received from the servo circuits (refer to the discussion on Seek Functions).

Actuator and Magnet Physical Description

The actuator (shown in figure 1-7) consists of the actuator housing, the carriage and voice coil assemblies, and the head-arm assemblies. The head-arm assemblies, with the heads mounted at their front, are mounted at the forward end, and the voice coil at the opposite end, of the carriage assembly. The carriage assembly fits within and is attached to the actuator housing by means of a pivot shaft. During head positioning, the carriage rotates about the pivot thus moving the heads out over the disk surface (this movement is a segment of an arc).

Whenever the drive is powered down, the actuator is latched in the unloaded position with the heads over the landing zone. The actuator remains locked until the next power up sequence

when the MPU releases the actuator locking solenoid. The automatic actuator locking feature eliminates the need to manually lock the actuator when transporting the drive.

Actuator and Magnet Functional Description

The voice coil is mounted at the opposite end of the arm assembly and moves in and out of the magnet as the servo signals change. The magnet is mounted on the housing in a position which allows the voice coil to move as the field in the coil changes. This small in and out motion of the voice coil in the magnet provides the motion for the heads over the disk surface. The movement of the carriage and voice coil (and therefore the heads) is controlled by positioning signals from the servo logic. The positioning signals are derived in the analog servo system and processed by the power amplifier. The output of the power amplifier is a current signal which is applied to the voice coil.

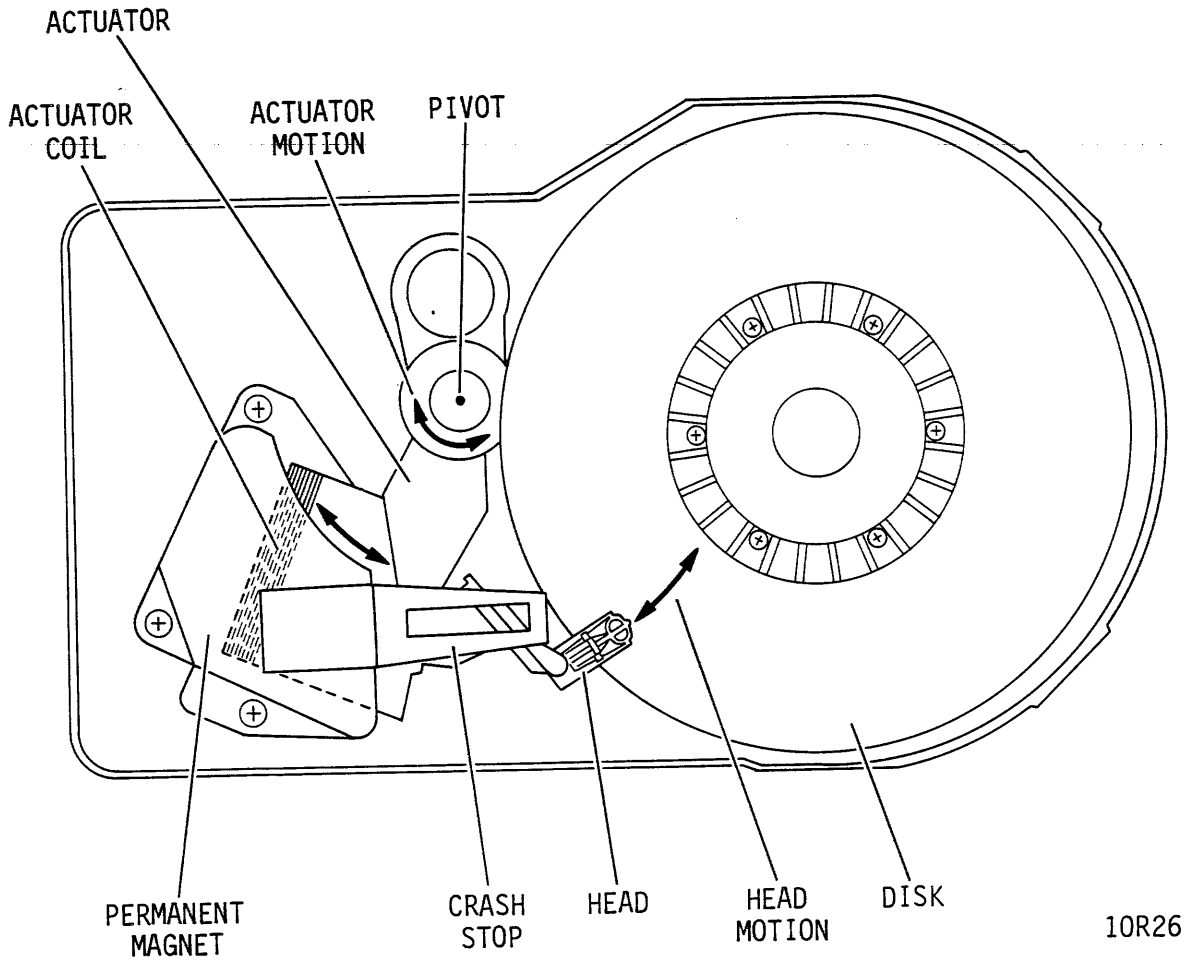


Figure 1-7. Actuator and Magnet Assembly

The current from the power amplifier causes a magnetic field in the voice coil which either aids or opposes the field around the permanent magnet. This reaction either draws the voice coil into the magnet or forces it away, depending on the polarity of the current through the voice coil. The acceleration of the voice coil is dependent on the amplitude of the voice coil current.

HEADS

General

The heads are magnetic devices that record data on, and read data from, the disk surface (the servo head, however, reads prerecorded data but cannot write). Each head is mounted at the end of a supporting arm. Head and arm together are called a head-arm assembly. The head-arm assemblies are attached to the front of the actuator assembly (figures 1-7 and 1-8).

The drive has ten data heads and one servo head. The data (or read/write) heads are used to record data on and read data from the disk data surfaces. The servo head is used to read prerecorded data from the servo disk surface for use by the drive analog servo circuits.

The following paragraphs describe the physical characteristics of the movable head-arm assemblies and how they function during head load and retract sequences. Further information about the heads is found in the discussions on seek and read/write functions.

Head-Arm Assembly

Each head-arm assembly consists of a rigid arm, load spring, gimbal spring, and the head (figure 1-8). The head-arm assemblies are mounted at the front of the actuator carriage and follow the in/out motion of the carriage created by the reaction of the voice coil magnetic field to the field of the permanent magnet. The rigid arm by itself does not provide the action necessary for the heads to load or unload. The head load spring forces its associated head toward the disk surface; the gimbal spring allows the head free axial movement along its vertical and horizontal axes independent from the rigid arm.

Read/write information is transferred to and from the heads through the head-arm cables. One end of each cable connects to a head and the other end has a plug which connects to the Read/Write Preamp board.

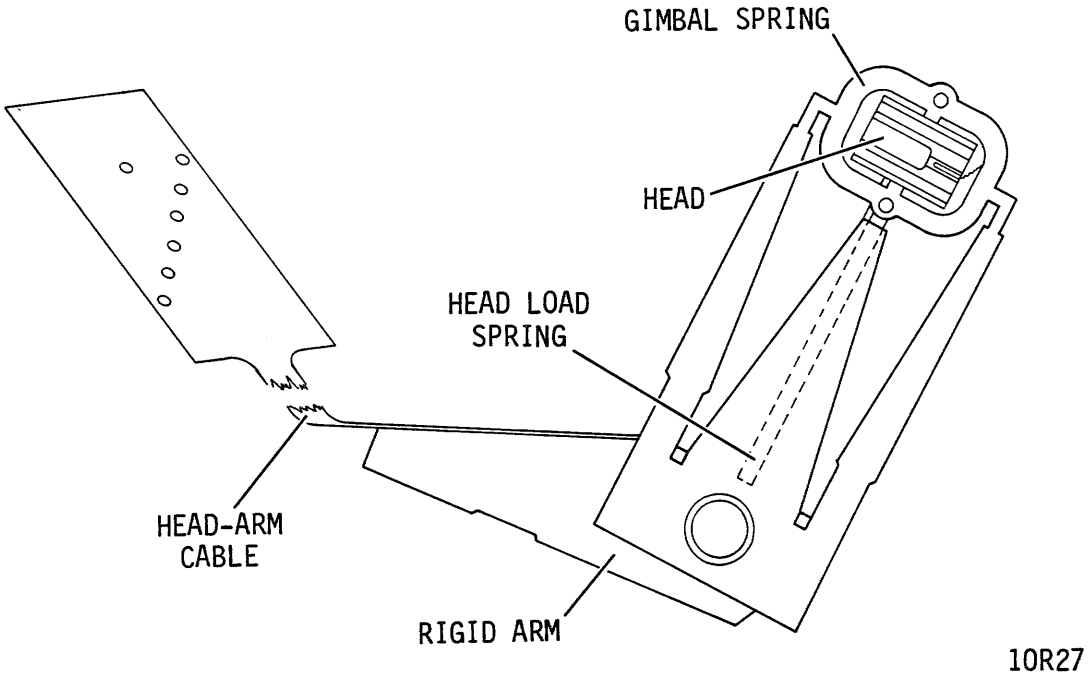


Figure 1-8. Data Heads

Head Loading

In the retract (non-operating) condition, the head load springs are forcing their respective heads against the disk surface in the landing zone. The landing zone is located in the extreme inner guard band on the disks. When the system powers up, the program turns on the drive motor. When the drive motor is rotating the disks at acceptable speed, the heads move away from the disk surfaces and fly on the cushion of air created by disk rotation. At this point in the power on sequence, the actuator is unlocked and the heads are moved outward to track zero. Until the power off sequence is begun, the heads continue to fly on the cushion of air.

The head load spring forces the head toward the disk surface, while the cushion of air pushes against the head to resist its closer approach. The air cushion pressure varies directly with disk speed, so that at proper speed the forces of the head load spring pressing the head towards the disk surface and the opposing force of the air cushion resisting the closer approach of the head are balanced such that the heads fly at the correct height above the disk.

If the disk drops below speed, the air cushion pressure decreases and the head load springs force the heads closer to the disk surface. Sufficient loss of speed would cause the heads to stop flying and contact the disk. This is called head landing. Because insufficient disk speed causes head landing, heads are not moved into the data areas until the disks have come up to speed. For the same reason, the heads are retracted from the data areas and locked over the landing zone when the disk speed drops below a safe operating level.

AIR FLOW SYSTEM

The air flow system is divided into two parts, one for the drive unit and the other for the sealed module.

The drive air flow system (figure 1-9) provides continuous air replacement and circulation to dissipate the heat generated by drive operation. The main component of the drive air flow system is the fan that is mounted on the rear panel. The fan motor is driven from the -24 V power from the power supply. The fan pulls ambient air through the input and primary filter of the front panel. The fan circulation travels over the electronics, cooling these assemblies before leaving the drive through the back panel. The system intake port is located on the front panel. This port is covered by the primary filter which keeps large particles from being drawn into the system.

The air flow system for the module is a self-contained closed loop system (figure 1-10). The system consists of a fan, circulation filter, and breather filter. The fan blades are located at the top of the hub assembly, and the rotation of the spindle rotates these fan blades. The motion of the blades above the cut out pulls air through the circulation filter into the disk area.

If the pressure within the module becomes less than the surrounding atmosphere, makeup air enters through the breather filter to equalize the pressures. Likewise, if the module pressure exceeds atmospheric pressure, air leaves the module through the breather filter.

INTERFACE

GENERAL

All communications between drive and controller must pass through the interface. This communication includes all commands, status, control signals, and read/write data transfers.

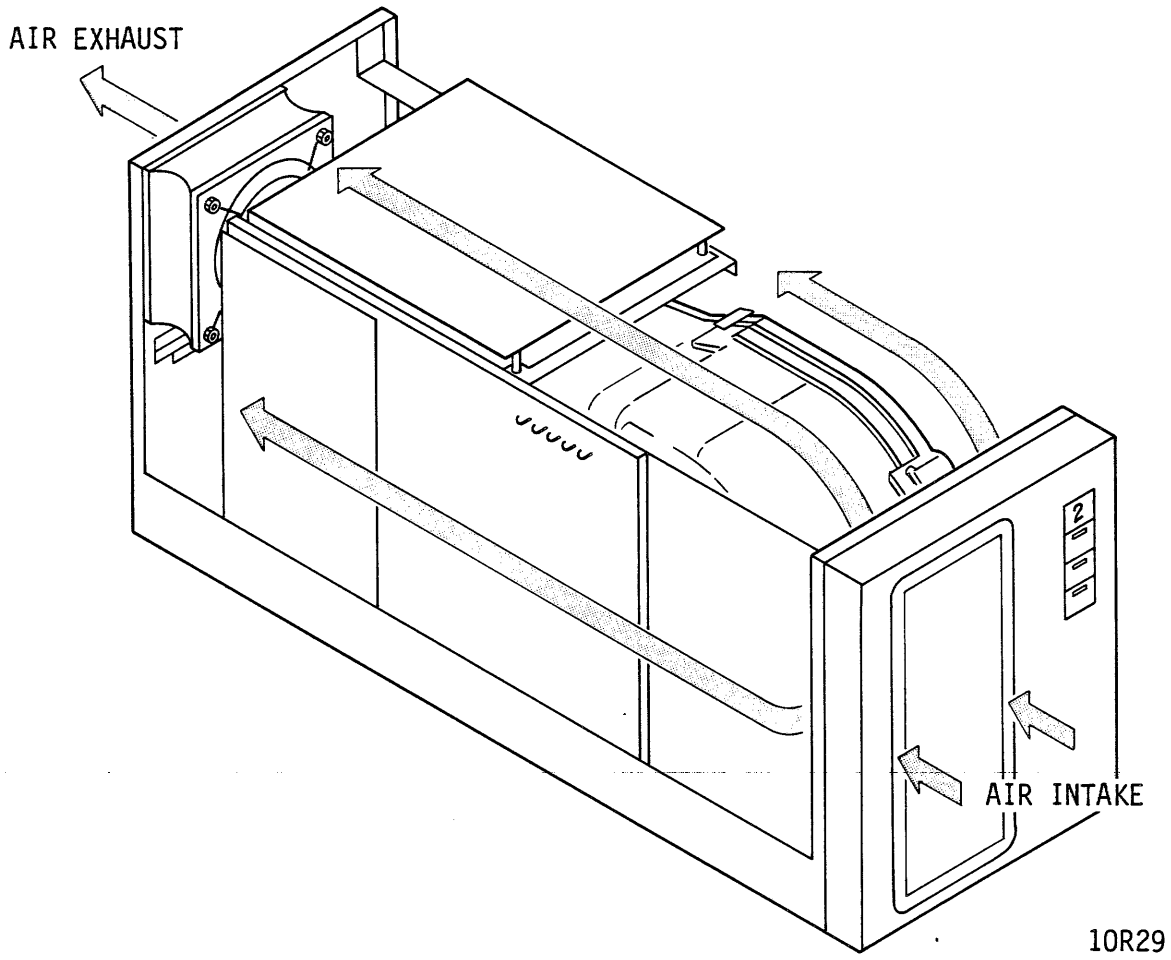


Figure 1-9. Drive Air Flow System

The interface consists of the I/O cables and the logic required to process the signals sent between drive and controller.

The following discussion describes both the I/O cables and I/O signal processing.

I/O CABLES

The drive has two I/O cables per channel, consisting of an A cable and a B cable. These cables contain all the lines going between the drive and controller.

The A cable carries commands and control information to the drive and status information to the controller.

The B cable carries read/write data, clock, and status information between drive and controller. Figure 1-11 shows all lines (except those not used) in the A and B cables. The functions of each of these lines are explained in table 1-1.

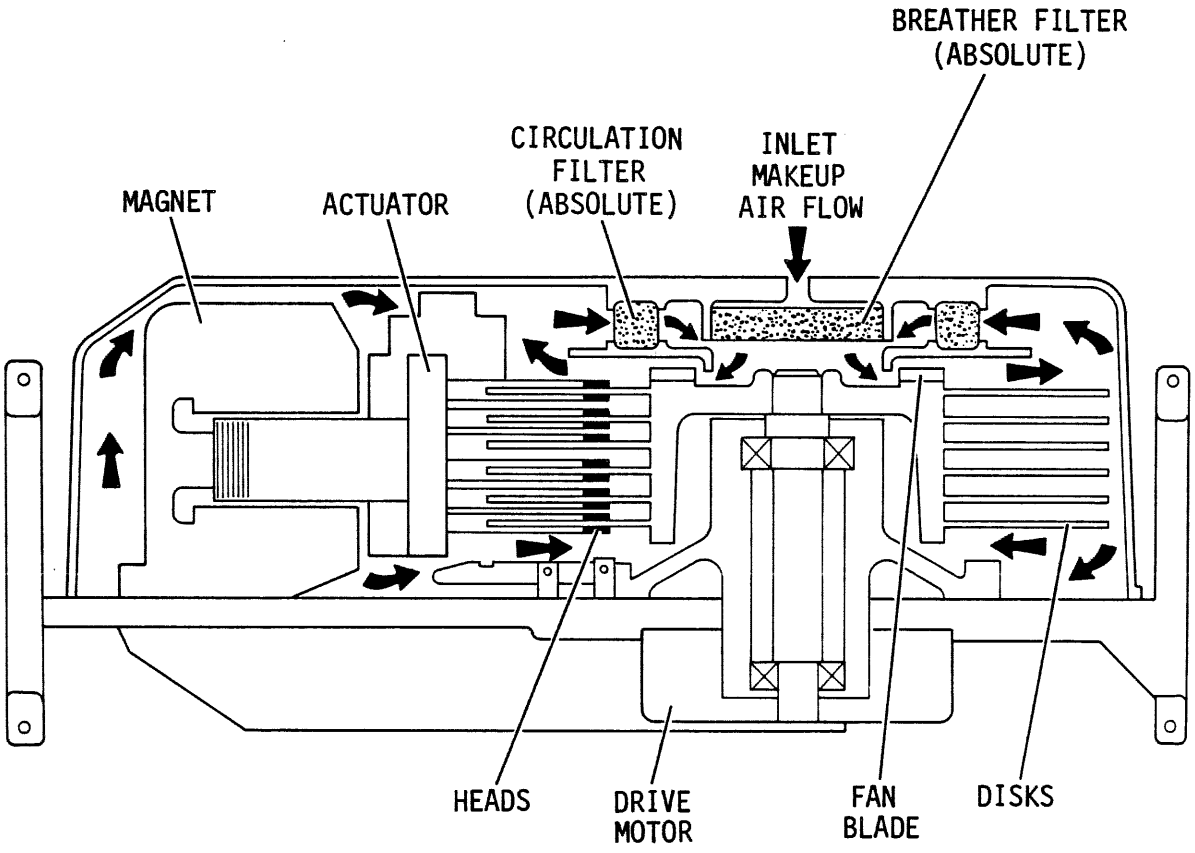


Figure 1-10. Module Component Placement and Air Flow

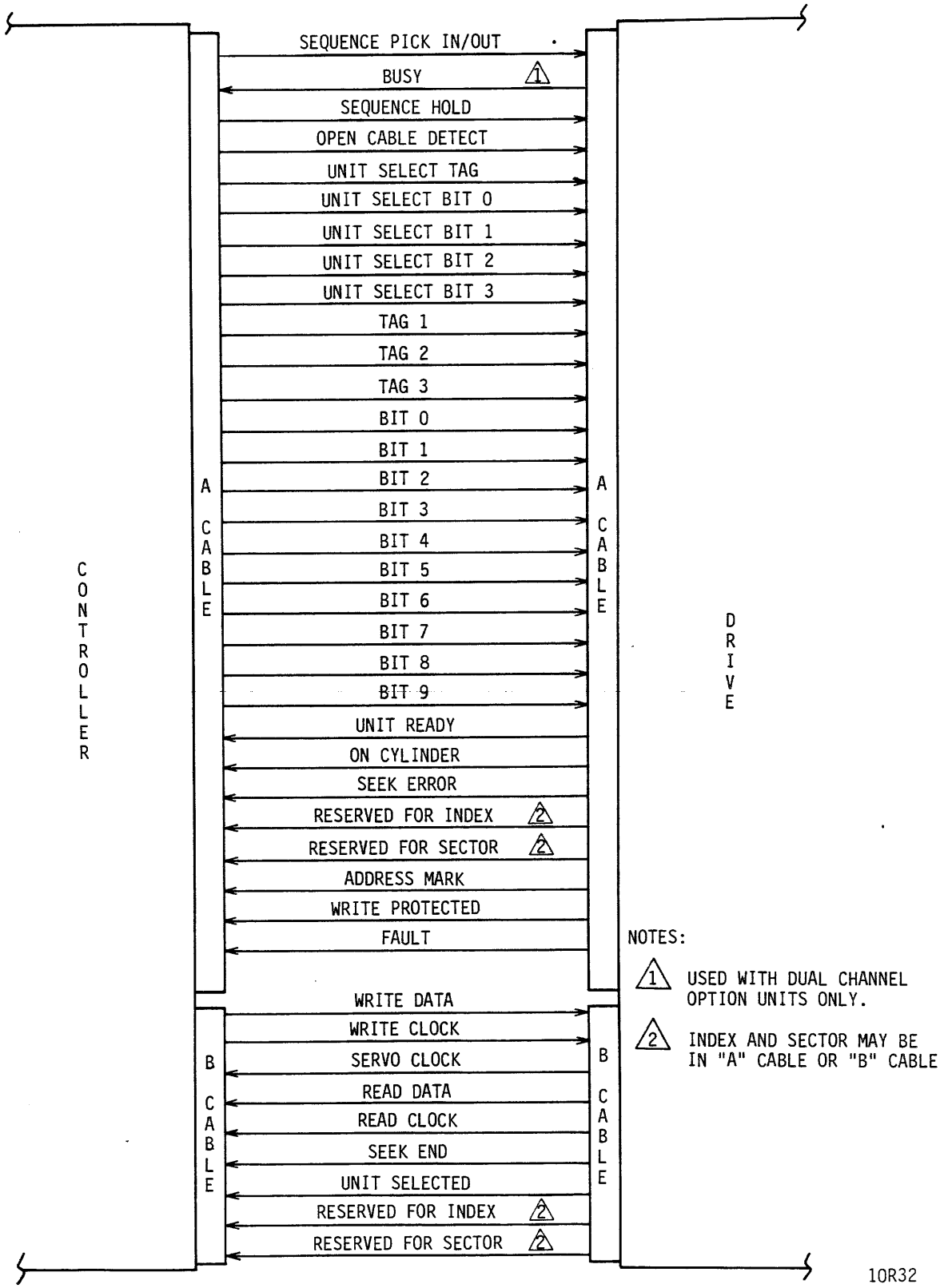


Figure 1-11. Interface Lines

TABLE 1-1. INTERFACE LINES

Signal	Meaning
Function: Power Up Sequencing	
Sequence Hold	A ground from the controller on this line starts the power on cycle when the drive's LOCAL/REMOTE switch is in the REMOTE position and the START switch on the operator panel is pressed.
Sequence Pick In	This line is not used in the drive.
Sequence Pick Out	This line is connected to Sequence Pick In. It transfers the sequence pick immediately to the next drive connected in a daisy chain configuration.
Function: Controller Selecting Drive	
Unit Select Tag	This signal gates Unit Select lines into logical number compare circuit. Unit is selected after 600 ns (maximum) internal time lapse. Drive will not process commands until selected. When the Unit Select Tag is accompanied by Bus Bit 9 active, this indicates a priority select status in dual channel systems. The drive is unconditionally selected and reserved by the channel issuing this command provided that both channels are enabled and a priority select condition does not exist on the other channel.
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Unit Select Bits 0, 1, 2, and 3	A binary code is placed on these four lines to select a drive. The binary code must match the logical address of the drive determined by the logical address plug inserted in the operator panel. Single-channel drives and older dual-channel drives can be numbered 0 through 7. Newer dual-channel drives can be numbered 0 through 15. Bit 3 must be inactive for a unit selection to occur.
Unit Selected	This signal indicates the drive has accepted a Unit Select request. This line must be active before drive will respond to any command from controller.
Open Cable Detect	A voltage is supplied by the controller to override the bias voltage at drive receiver. If the A cable is disconnected or if controller power is lost, unit selection and/or controller commands are inhibited.
Function: Drive Indicates Operational Status	
Unit Ready	Unit Ready indicates that the drive is up to speed, that the servo head is positioned on cylinder, and that no fault condition exists.
Index	This signal is derived from the servo tracks. It occurs once per revolution of the disk, and its leading edge is the leading edge of sector zero.
Sector	This signal is derived from the servo tracks. The number of sector signals that occur for each revolution of the disk is selected by switches on the Control board.
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Busy	Used only in dual channel drives, this signal is generated when a controller attempts to select or reserve a drive that has already been selected and/or reserved by the other controller. This signal is sent to the controller attempting the selection.
Write Protected	This signal indicates that the drive write circuits are disabled. The write protect mode is enabled by switches on the Control board and the operator panel, or by a fault condition. Attempting to write while the write protect mode is active results in a fault condition.
On Cylinder	This signal indicates that the servo head is positioned at a track. This line goes inactive if the positioner drifts off cylinder.
Seek End	This signal indicates either an on cylinder status or seek error status resulting from a seek operation that has terminated.
Seek Error	This signal indicates that the drive was unable to complete a seek within 250 ms, that the positioner has moved outside the recording field, or that the drive was commanded to seek beyond cylinder 822. The seek error can be cleared by an RTZ command or by a power up operation.

Table Continued on Next Page

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Fault	When this line is active, it indicates that one or more of the following faults exist: • First Seek fault • DC voltage fault • Write fault • Write or read attempted while off cylinder • Write gate during a read operation
Address Mark	When an address mark has been found, this line goes high.
Function: Controller Sends Commands to Drive	
Bits 0 through 9 (Bus Lines)	These ten lines carry data to the drive. The meaning of the data is a function of the active tag line.
Tag 1 (Cylinder Select)	This tag line gates the data on the bus lines to the drive Cylinder Address register. The bus bits have the significance listed below. Bus bits 0-9, with the value shown below, encode the cylinder address for the seek operation. Cylinder addresses above 822 are illegal and will encode a seek error.
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
	Bus Bit — Function 0 — Cylinder Address 2^0 1 — Cylinder Address 2^1 2 — Cylinder Address 2^2 3 — Cylinder Address 2^3 4 — Cylinder Address 2^4 5 — Cylinder Address 2^5 6 — Cylinder Address 2^6 7 — Cylinder Address 2^7 8 — Cylinder Address 2^8 9 — Cylinder Address 2^9
Tag 2 (Head Select)	This tag line gates the data on the bus lines to the drive Head Address register. The bus bits have the significance listed below. Bus Bit — Function 0 — Head Address 2^0 1 — Head Address 2^1 2 — Head Address 2^2 3 — Head Address 2^3
Tag 3 (Control Select)	This tag line gates the data on the bus lines to the logic circuits of the drive for commanding various operations. The operation performed is dependent upon which of the bus lines is active. The significance of the bus bits is as follows:

Table Continued on Next Page

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Tag 3 (Contd)	Bus Bit / Name / Function Performed 0 Write Gate — Enables write driver. Not accepted if there is a seek error or fault status. 1 Read Gate — Enables read circuitry. Leading edge triggers the read chain circuit to synchronize on an all zeros pattern. Not accepted if there is a seek error or fault status. 2 Servo Offset Plus — Offsets the positioner 100 microinches toward the spindle from the on cylinder position. Disables On Cylinder for 2.75 ms. 3 Servo Offset Minus — Offsets the positioner 100 microinches away from the spindle from the on cylinder position. Disables On Cylinder for 2.75 ms. 4 Fault Clear — A pulse sent to drive that clears the Fault flip-flop provided that the fault condition no longer exists.

Table Continued on Next Page

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Tag 3 (Contd)	Bus Bit / Name / Function Performed 5 Address Mark Enable — When this signal occurs with a Write Gate, an address mark is written. When this signal occurs with a Read gate, an address mark search is initiated. 6 RTZ — A pulse sent to the drive to move the positioner to track zero. It also resets the Head Address register, Cylinder Address register, and Seek Error flip-flop. 7 Data Strobe Early — Enables the read comparator to strobe the data at a time earlier than nominal. 8 Data Strobe Late — Enables the read comparator to strobe the data at a time later than nominal. 9 Release — Used with dual channel option only, it clears channel reserved and channel priority select reserve status. (Refer to Unit Selection discussion.)
Table Continued on Next Page	

TABLE 1-1. INTERFACE LINES (Contd)

Signal	Meaning
Functions: Read, Write, and Clocks	
Read Data	This line transmits data recovered from the disk. This data is transmitted in NRZ form to the controller.
Read Clock	This clock is derived from, and is synchronous with, the detected data. Read Clock defines the beginning of a data cell and is transmitted continuously.
Write Data	This line transmits NRZ data from the controller to the drive for recording on the disk surface with 2-7 encoding.
Write Clock	This clock is the Servo Clock retransmitted to the drive during a write operation. Write Clock must be synchronized to the NRZ data and must be transmitted 250 ns prior to Write Enable.
Servo Clock	Servo Clock is a phase-locked 9.67 MHz signal generated from the servo track tribits. Servo Clock is continuously transmitted.

I/O SIGNAL PROCESSING

I/O signals from the controller initiate and control all drive operations except local power on. The I/O signals are sent to receivers in the drive and are routed from the receivers to the appropriate drive logic. The drive in turn sends information concerning the operation back to the controller via the drivers. Figure 1-12 shows the basic logic involved in the routing of the I/O signals.

Certain I/O signals cannot be transmitted or received unless the drive is selected. These signals include the tag and bus bit signals from the controller and the status bits to the controller.

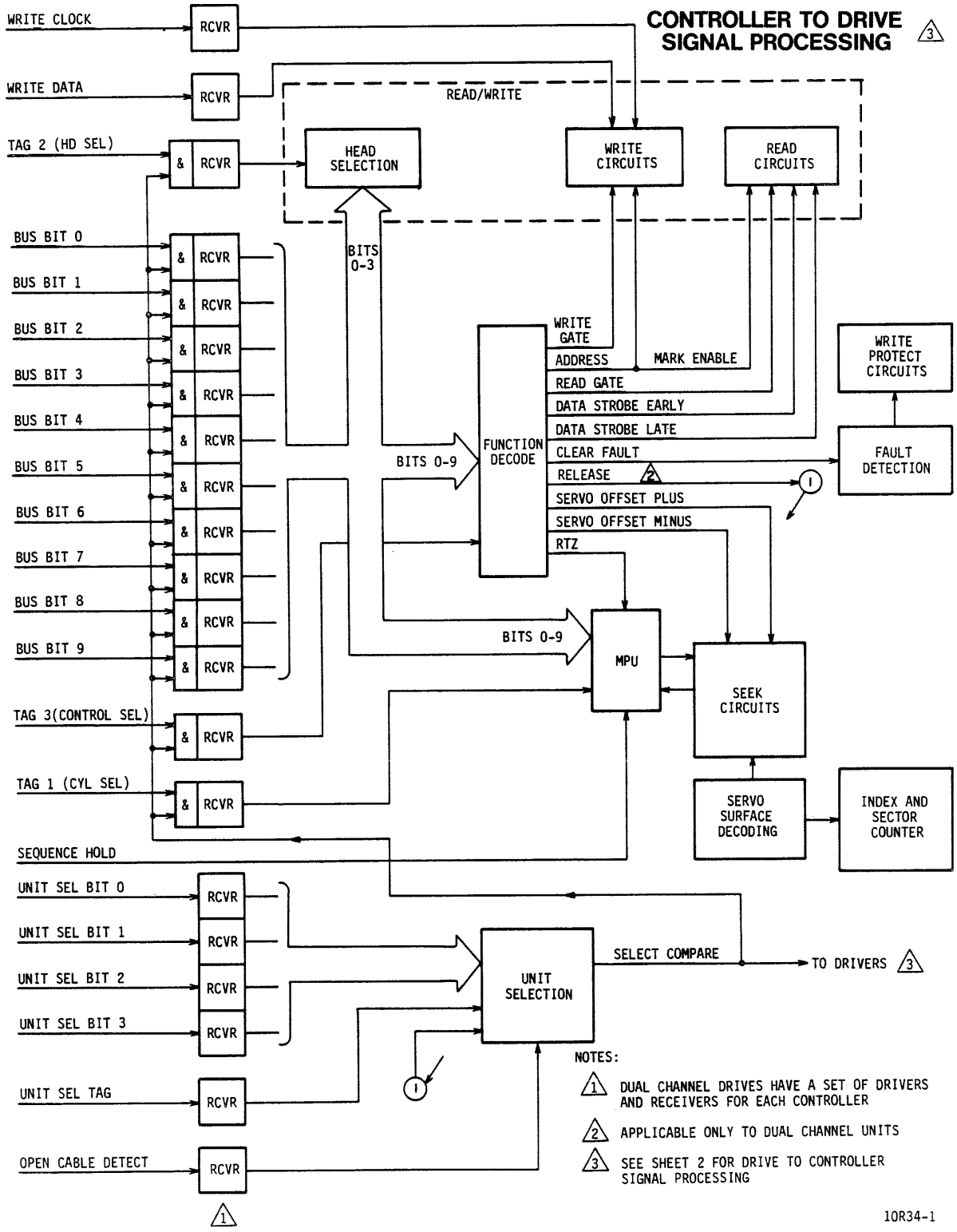
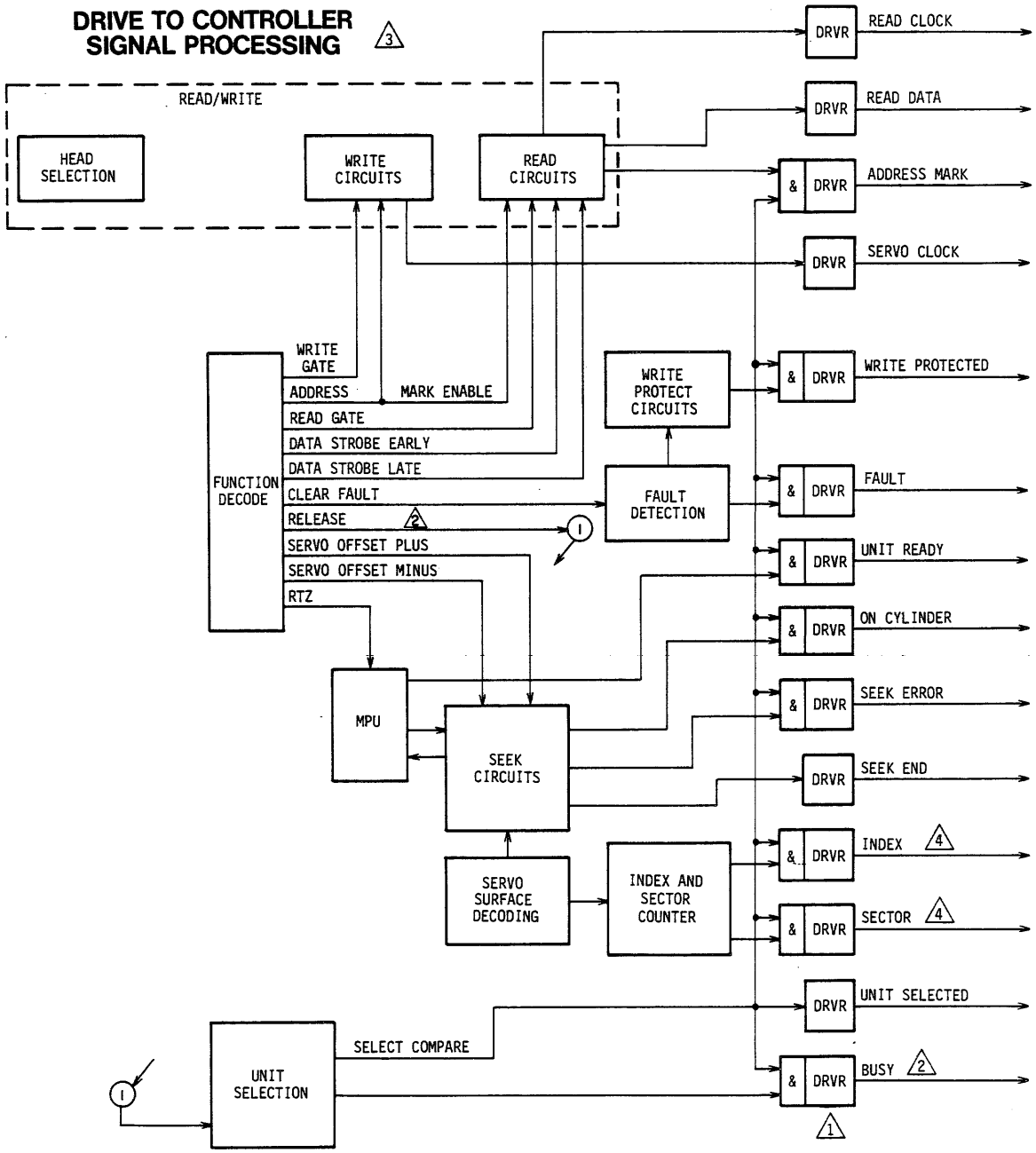


Figure 1-12. I/O Signal Processing (Sheet 1 of 2)



NOTES:

1. DUAL CHANNEL DRIVES HAVE A SET OF DRIVERS AND RECEIVERS FOR EACH CONTROLLER
2. APPLICABLE ONLY TO DUAL CHANNEL UNITS
3. SEE SHEET 1 FOR CONTROLLER TO DRIVE SIGNAL PROCESSING
4. INDEX AND SECTOR SIGNALS ARE SENT CONTINUOUSLY WHEN INDEX/SECTOR JUMPER PLUG IS IN "B" POSITION

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Figure 1-12. I/O Signal Processing (Sheet 2)

All commands (except unit select) are sent to the drive via the tag and bus bit lines. The tag lines define the basic operation to be performed and the bus bits further define and modify the basic operation. Table 1-1 explains the functions of all tag and bus lines.

UNIT SELECTION

GENERAL

The drive must be selected before it will respond to any commands from the controller. This is the case because the tag and bus bit receivers, as well as certain drivers, are not enabled until the drive is selected.

In both single and dual channel units, the select sequence is initiated by a Unit Select Tag signal from the controller. However, the sequence performed is different depending on whether a single or dual channel is being considered. Since only one controller can communicate with the drive at a time, dual channel logic must solve the problem of priority when more than one controller wants to select the drive at the same time. The following paragraphs describe both single and dual channel selection.

SINGLE CHANNEL UNIT SELECTION

The single channel unit select sequence (see figure 1-13) starts when the controller sends the Unit Select Tag accompanied by a logical address on the four unit select lines.

When the drive recognizes the Unit Select Tag, it compares its own logical address (as indicated by the logical address plug) to the address sent by the controller. The drive's logical address is determined by the logical address plug which fits into the operator panel. Depending on the plug used, this address can be any number from 0 to 7. If no plug is used, the number is 7.

If the address sent by the controller is the same as that of the drive and the Open Cable Detect signal is active (indicating the A cable is connected and controller has power), the drive enables its Select Compare signal.

The Select Compare signal enables the receivers and drivers to the controller and also enables the Unit Selected signal. The drive is now ready to respond to further commands from the controller.

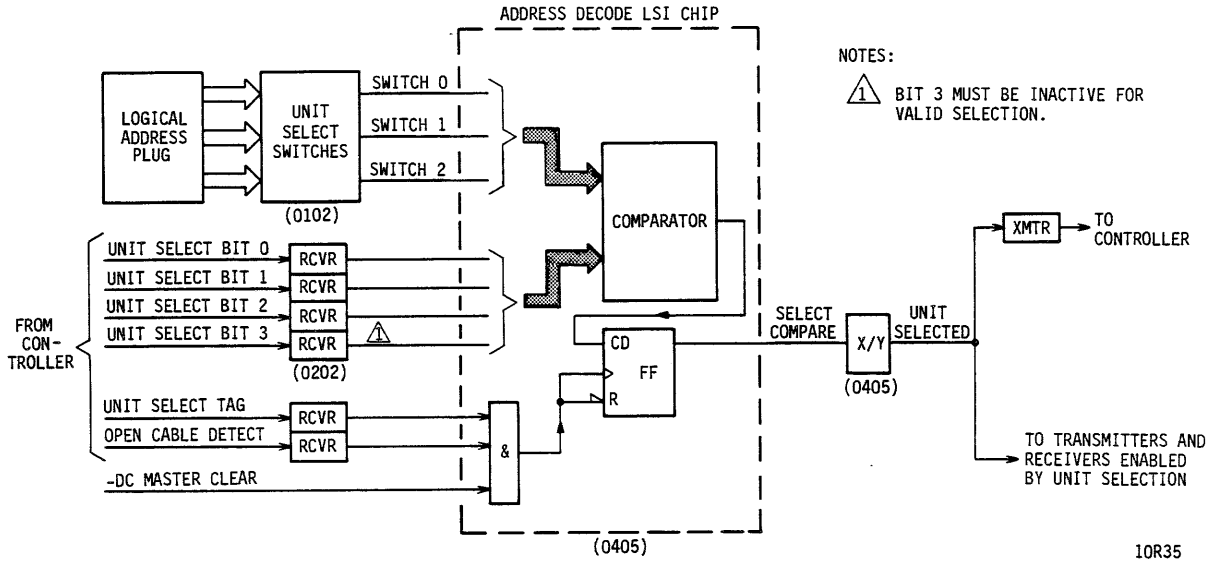


Figure 1-13. Unit Select Logic (Single Channel)

DUAL CHANNEL UNIT SELECTION

General

Dual channel drives are connected to, and can be selected by, either of two controllers. However, because the drive is capable of responding to only one controller at a time, the controllers must compete for use of the drive. For this reason, there are functions associated with dual channel selection that are not necessary when selecting single channel units.

The functions controlling dual channel selection are as follows:

- Select - Logically connects the drive to the controller, thus enabling it to respond to commands from the selecting controller.
- Reserve - Reserves the drive so it can be selected at any time by the reserving controller, but prevents it from being selected by the other controller.

- Release - Releases drive from reserved condition.

- Priority Select - Allows controller to force select the drive by disabling the interface to the controller having the drive selected or reserved.

- Maintenance Disable - Allows disabling either channel interface during maintenance.

The following discussions describe each of these functions. It should be noted that because these functions are basically the same regardless of which channel is involved, they are described only as they relate to Channel I. Figure 1-14 shows the select logic associated with channel I selection and table 1-2 describes the major elements on this figure. Figure 1-15 is a flowchart of the dual channel unit select and reserve functions.

Select and Reserve Function

The drive is both selected and reserved during the same sequence and this sequence is initiated by a Unit Select Tag accompanied by a logical address. However, the drive can be successfully selected and reserved only if none of the following conditions exist:

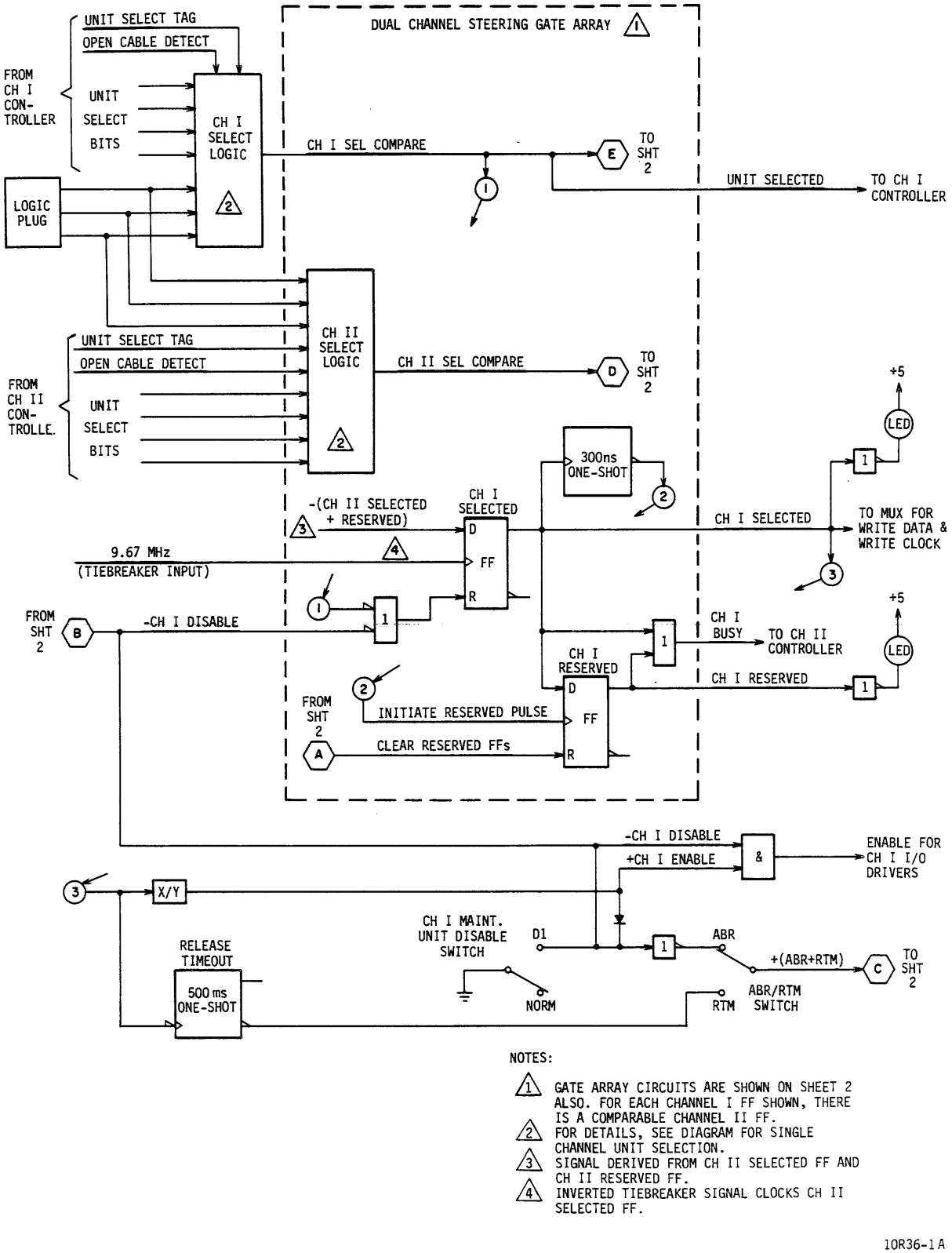
- Drive is already selected and reserved by other controller.

- Drive is not selected but is reserved by other controller.

- Channel to drive attempting selection has been disabled by either a priority or maintenance disable function.

The following paragraphs describe how the drive is initially selected and also how it responds to a Unit Select Tag when it is selected, reserved, or disabled.

Assuming the drive is available (not selected, reserved, or disabled) and it receives a Unit Select Tag and logical address from the controller on channel I, it compares the address received with that indicated by its logical address plug. (The address can be any number from 0 through 15. If no plug is used with unit select jumper set to 0-7, drive cannot be selected. If no plug is used with unit select jumper set to 0-15, the address is 15.) If the two addresses are the same, the drive enables the Channel I Select Compare sig- nal. The logic used to generate this signal is identical to that used in the single channel units (refer to figure 1-13).



NOTES:

1. GATE ARRAY CIRCUITS ARE SHOWN ON SHEET 2 ALSO. FOR EACH CHANNEL I FF SHOWN, THERE IS A COMPARABLE CHANNEL II FF.
2. FOR DETAILS, SEE DIAGRAM FOR SINGLE CHANNEL UNIT SELECTION.
3. SIGNAL DERIVED FROM CH II SELECTED FF AND CH II RESERVED FF.
4. INVERTED TIEBREAKER SIGNAL CLOCKS CH II SELECTED FF.

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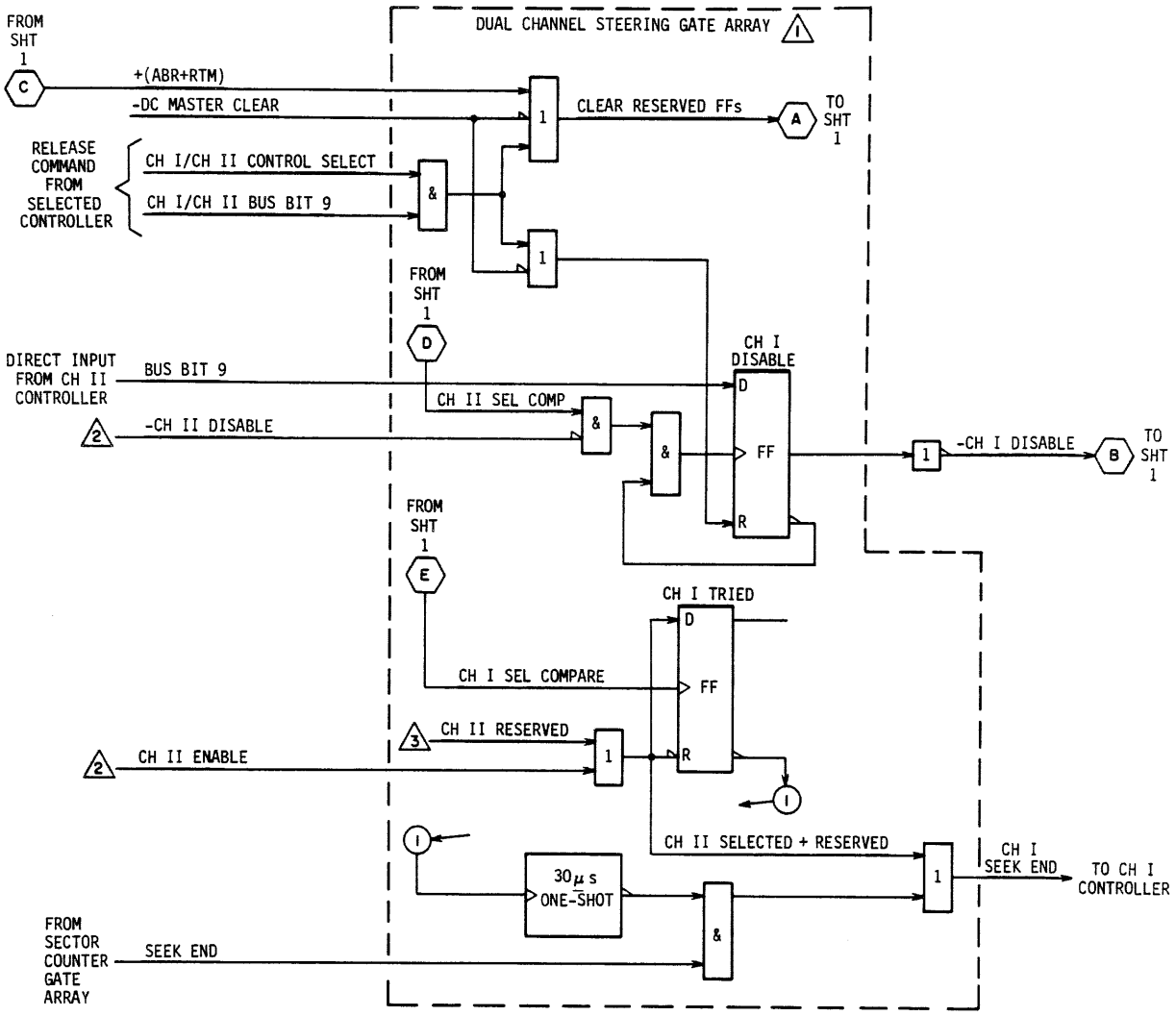
Figure 1-14. Channel I Dual Channel Logic (Sheet 1 of 2)



NOTES:

1. GATE ARRAY CIRCUITS ARE SHOWN SHEET 1 ALSO. FOR EACH CHANNEL I FF SHOWN, THERE IS A COMPARABLE CHANNEL II FF.
2. SIGNALS DERIVED FROM CHANNEL II OUTPUTS OF GATE ARRAY.
3. SIGNAL DERIVED FROM CH II RESERVED FF.

10R36-2

Figure 1-14. Channel I Dual Channel Logic (Sheet 2)

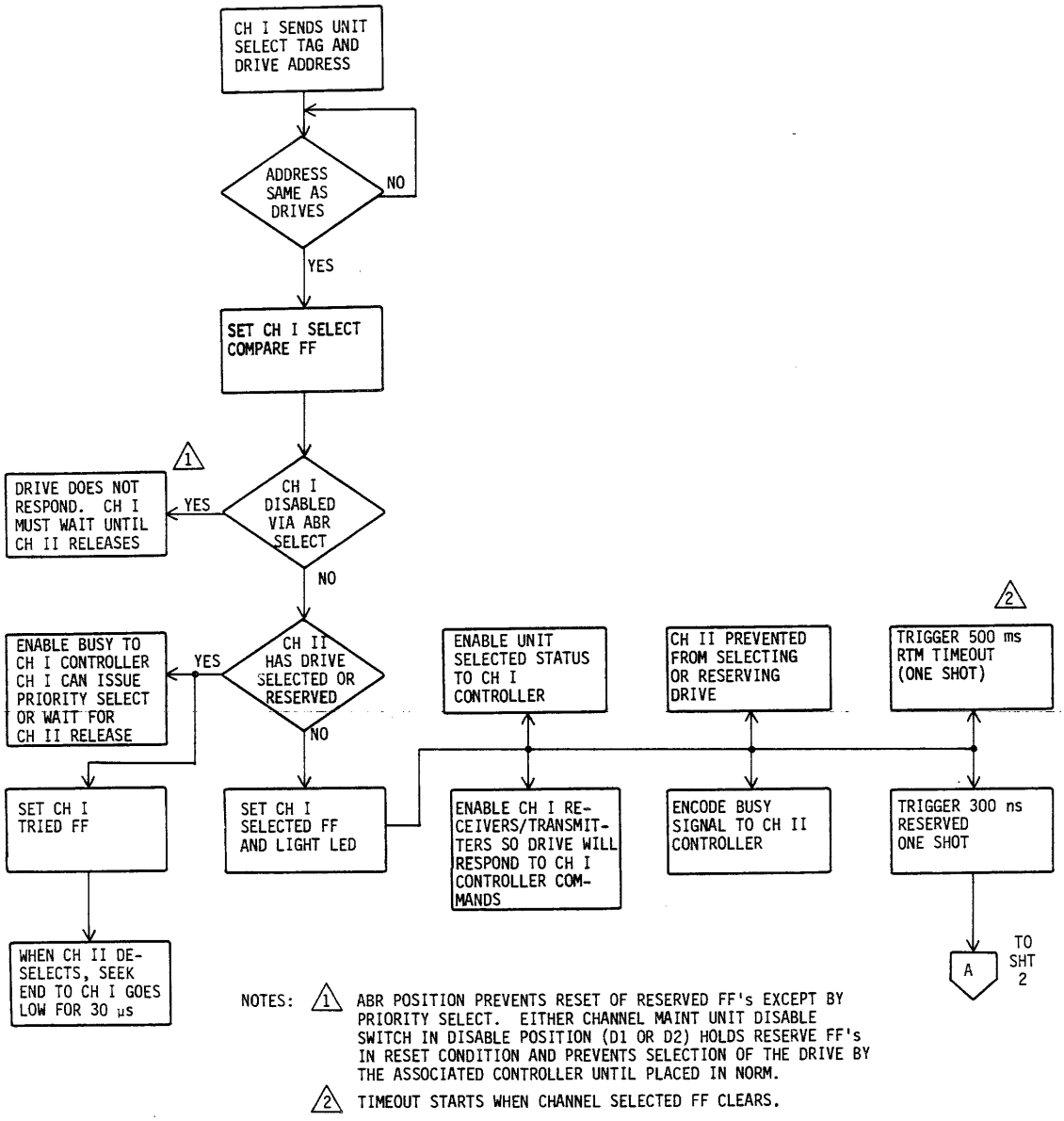


Figure 1-15. Dual Channel Selection Flowchart (Sheet 1 of 2)

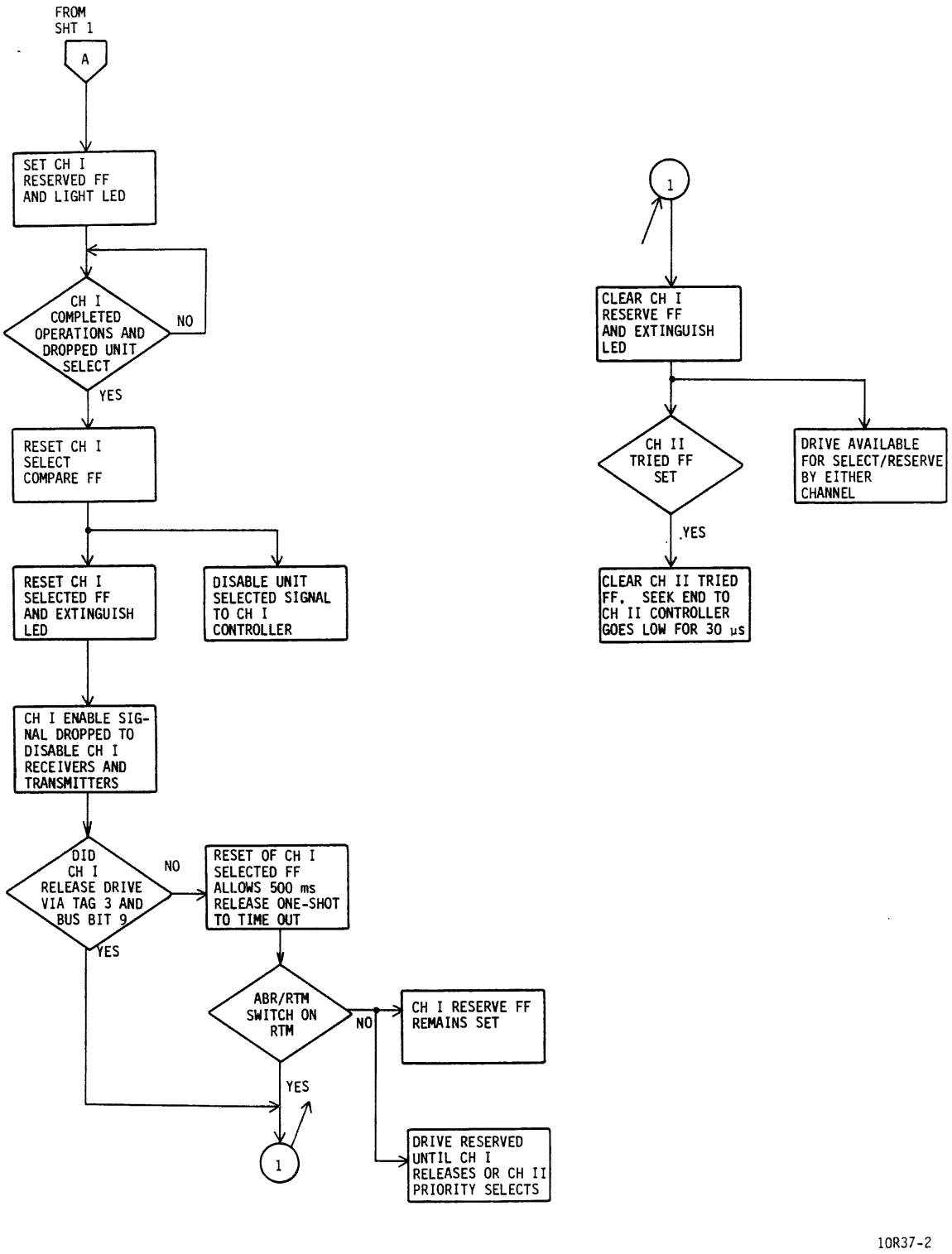


Figure 1-15. Dual Channel Selection Flowchart (Sheet 2)

TABLE 1-2. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS

Element*	Function
ABR/RTM Switch	Determines whether the drive will be in ABR (absolute reserve) or RTM (reserve timeout) mode. If switch is in RTM position, drive is released from reserved condition 500 ms (nominal) after being deselected. If switch is in ABR position, drive remains reserved until it receives either a release or priority select command.
Release Timeout One Shot	Deselecting drive causes this one shot to generate a 500 ms (nominal pulse). If drive is in RTM mode the trailing edge of this pulse clears the reserved FF.
Channel I Disable FF	Sets if drive receives Priority Select command. This causes drive to be selected and reserved for controller issuing command and disables channel to other controller.
Channel I Maintenance Unit Disable Switch	Disables channel I whenever it is set to DI (disable) position. It must be in NORM position during normal operations.
Channel I Reserved FF	Sets during select and reserve sequence. When set it keeps drive reserved to channel I until channel I releases or channel II issues a Priority Select command.
Channel I** Selected FF	Sets during select and reserve sequence and enables drivers and receivers to channel I controller.
Channel I Select and Compare Logic	Compares logical address of drive with that sent by controller (see Single Channel Unit Selection).

Table Continued on Next Page

TABLE 1-2. DUAL CHANNEL UNIT SELECT CIRCUIT FUNCTIONS (Contd)

Element*	Function
Initiate Reserved Pulse	Generates 300 ns pulse whenever Select Compare signal goes true. Leading edge of this pulse clocks Channel I and Channel II Reserve FF.
Channel I Select Tried FF	Sets if channel I tries to select and reserve drive while it is already selected and/or reserved by channel II. When drive is deselected and released by Channel II, this FF clears and thereby triggers the Select Tried one shot.
Select Tried One Shot	Generates 30 microsecond pulse whenever either Tried FF clears. This pulse is sent to controller (associated with the Channel Tried FF that triggered the one shot) via the Seek End line.

* Includes only those elements directly concerning channel I and shown in figure 1-14.

**The Channel Selected FF's are alternately clocked by the 9.67 MHz clock signal to prevent simultaneous selection.

The Select Compare signal causes the Channel I Selected FF to set, thereby enabling the receivers and drivers to the Channel I controller and triggering the 300 ns Reserve one-shot. The output pulse from this one-shot clocks and sets the Channel I Reserved FF. With these FFs set, the drive sends Unit Selected to the channel I controller indicating that it is ready to accept further commands.

Providing channel II does not issue a priority select command (see Priority Select Function discussion), the drive remains selected to channel I until the controller on channel I drops its Unit Select Tag or changes the logical address to another drive. At this time, the drive's Channel I Selected FF clears,

thus disabling the drive drivers and receivers for that channel. This also disables the Unit Selected signal thus informing the controller that the drive will no longer respond to commands. However, the drive remains reserved to channel I (allowing channel I to reselect while preventing channel II from selecting) until the Channel I Reserve FF is also Clear. This is cleared by either a release or priority select function (refer to these discussions).

If channel I attempts to select and reserve the drive while it is selected and reserved by channel II, the Channel I Select Compare signal is still generated as during the initial select and reserve sequence. However, the Channel I Select and Reserve FFs do not set, and therefore the attempt is unsuccessful. The drive still sends the Channel I Unit Selected signal to the controller, but, in this case, it is accompanied by the Channel I Busy signal. The Busy signal indicates that the drive is being used by channel II.

The drive also sets its Channel I Tried FF, thus recording the unsuccessful attempt. When the drive is no longer selected or reserved by channel II, this FF clears, causing Seek End to the channel I controller to go low for 30 microseconds. This informs the controller that the drive is no longer selected or reserved.

If the channel I controller tries to select the drive while channel I is disabled (either by a priority select or maintenance disable function), the attempt is unsuccessful and no response is sent back to the channel I controller.

Release Function

The release function will release the drive from either a reserved or priority selected condition. There are two types of release functions:

- Timeout release pulse
- Release command

The timeout release pulse is capable of releasing the drive from only the reserved condition. This pulse is generated by the 500 ms Timeout Release one-shot and releases the drive by clearing the Reserve FF. The pulse is triggered when the drive is selected (Select FF sets) and times out 500 ms after the drive is deselected (Select FF clears).

Whether or not the one shot has any effect on the Release FF depends on the position of the ABR/RTM switch. If this switch is in the RTM (reserve timeout) position, the FF clears when the one-shot times out, thus making the drive available to the other channel. However, if this switch is in ABR (absolute reserve) position, the one-shot has no effect on the FF and the drive remains reserved.

A Release command will release the drive from both the reserved and priority selected conditions. This command is initiated by the reserving and/or priority selecting controller when it issues a Tag 3 (Control Select) with Bus Bit 9 active. This clears the Reserve and Disable FFs and allows the other controller to select the drive.

Priority Select Function

If the drive is selected and reserved, the other controller can force selection by issuing a Priority Select command (Unit Select Tag accompanied by drive logical address and Bus Bit 9). This command will disable the channel to the controller presently using the drive and also select and reserve the drive to the controller issuing the Priority Select command.

For example if channel I has the drive and channel II wants to select, channel II issues a Priority Select command. In this case, the command sets the Channel I Disable FF which in turn results in clearing the Channel I Selected and Reserved FFs. It also sets the Channel II Selected and Reserved FFs, thereby selecting and reserving the drive for channel II.

Once the Disable FF is set, that channel (in this case channel I) is disabled until the other controller (in this case channel II) issues a command to clear it.

Maintenance Disable Function

It is also possible to disable either channel by setting the Maintenance Unit Disable switch for that channel (refer to figure 1-14) to the DI or DII position.

DRIVE SERVO SYSTEM

The drive writes data on and reads data from the disk data recording areas under the directions of the controller. These operations cannot be done randomly, however, for when the controller wishes to retrieve data, it must be able to find the exact location where that data has been stored. This problem

is resolved by mapping the disks into discrete sections called "Tracks" which are narrow concentric bands that cover the entire circumference of the circle. The tracks are then further subdivided into equal areas called "Sectors".

After the controller has selected the unit with which it wishes to perform an operation, it must then direct the drive to the specific location on the data recording surface where it wants the operation to be performed. The operation of positioning the heads over the desired track is called a Seek operation. The drive servo system under the direction of the microprocessor unit (MPU) performs the Seek operation to position the heads by using information read from the servo surface by the servo head.

The data recording areas of each of the disks (10 surfaces total) are divided into 823 tracks, and these are assigned sequential number addresses from 0, which is located on the outer edge of the recording area, through 822, which is located on the inner edge of the data recording surface closest to the hub. Since there are ten data recording surfaces, each with 823 tracks with addresses 0 through 822, the controller must select one of ten possible tracks with the same cylinder address number. This further selection is done by assigning numbers to the data recording surfaces (and the heads associated with the disk surfaces) from 0 through 9.

Once a particular cylinder is selected, the controller then further narrows down location selection by addressing one of ten heads located at the selected cylinder. Each track is subdivided into equal segments called "Sectors". This division is accomplished by the setting of a group of switches called Sector switches (see the discussion called Sector Detection). When the controller has selected the unit, the track, and the head, then it waits for the particular sector(s) where it wishes to write (store) or retrieve (read) data. Another option for locating an area on a track to be operated upon is by writing an Address Mark at a specific location on the track, and then looking for the mark at the beginning of a read operation.

When the controller commands the drive to go to a cylinder/head/sector where it wishes to perform a read or write operation, the drive servo system under the direction of the MPU performs the positioning (Seek) operation. The MPU program uses information read from the servo surface by the servo head to do the Seek operation. The following discussions will describe servo surface decoding and then describe seek functions.

SERVO SURFACE DECODING

GENERAL

The servo surface is a prerecorded disk surface in the module that provides three basic types of information to the drive electronics. Information from the servo surface is read by the servo head. The servo head is mounted on the same positioner as the data heads; thus, movements of the servo head across the servo surface correspond exactly to movements of the data heads across the data surfaces.

The three types of information available from the servo surface are as follows:

- Radial movement of the heads, indicated by the Position signal
- Rotational position of the disks, indicated by the Index signal
- Exact speed of the disks, indicated by the 1.612 MHz Clock signal.

The significance of each type of information for drive operation and the development of the basic feedback signals from the servo signal are presented under the following topics:

- Tribit Recording Scheme
- Servo Surface Format
- Tribit Decoder Circuit Operation

TRIBIT RECORDING SCHEME

Servo information consists of tribit coding on a series of concentric tracks located on the servo surface. The pattern of flux reversals alternates from track to track. Each track has eighty segments, each consisting of a special five-byte code followed by 79 normal servo bytes.

Unless the servo head is positioned directly over one servo track, the signal it detects is a composite of signals from the two tracks nearest the head. Figure 1-16 shows servo information recorded on two adjacent tracks and the signal detected when the servo head is halfway between the tracks.

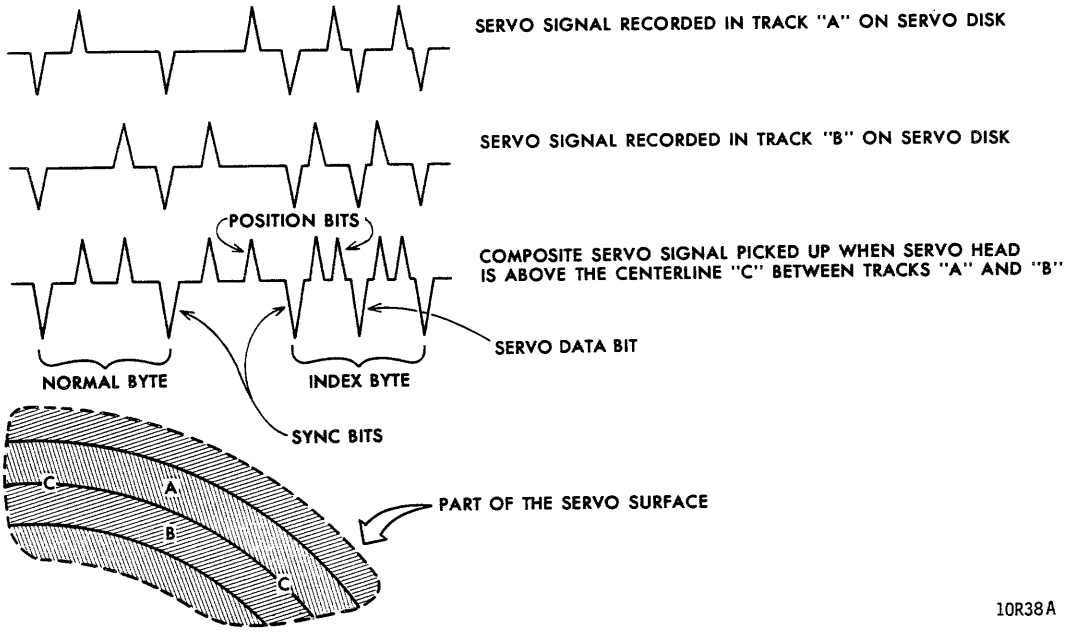


Figure 1-16. Tribit Pattern

In figure 1-16, two normal bytes are followed by an index byte. Each normal byte contains three bits -- a sync bit and two position bits. The sync bits have negative polarity and are recorded on all tracks. The position bits have positive polarity and are staggered from track to track so that they make separate contributions to the composite servo signal.

The index byte shown in figure 1-16 has a sync bit, an extra negative pulse called a servo data bit, and four position bits (twice the number of position bits in the normal byte). Adjacent tracks have coinciding sync and servo data bits as well as staggered position bits.

The special five-byte codes appearing 80 times per disk rotation contain different combinations of index bytes and normal bytes, depending on what the code designates on the disk surface. The different codes and their relation to the disk format are explained under the next topic. Each five-byte code is followed by 79 normal bytes. Thus, for each disk rotation, the servo head detects 80 X 84 or 6720 servo bytes.

The relative amplitude of the position bits within each servo byte is used to indicate the precise position of the servo head and, therefore, the data heads. When the data heads are located at the centerline of a data track, the servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent tribit signals. The amplitude of each position bit within a servo byte is proportional to the read coil overlap of the recorded servo tracks. With the head centered, each adjacent servo track contributes equal position bit amplitudes. As the head moves away from its centered position toward one servo track, the track being approached makes a greater contribution to the detected position bits than the one being left. The tribit demodulator converts this variation into the position signal used by the seek circuitry (see Position Demodulation).

Figure 1-17 shows the detected servo signal for three different servo head positions. In one of the three cases, the servo head is located on the centerline between two servo tracks, and the position bits have equal amplitudes. In the other two cases, the servo head is located on either side of the centerline, and the position bits have different amplitudes.

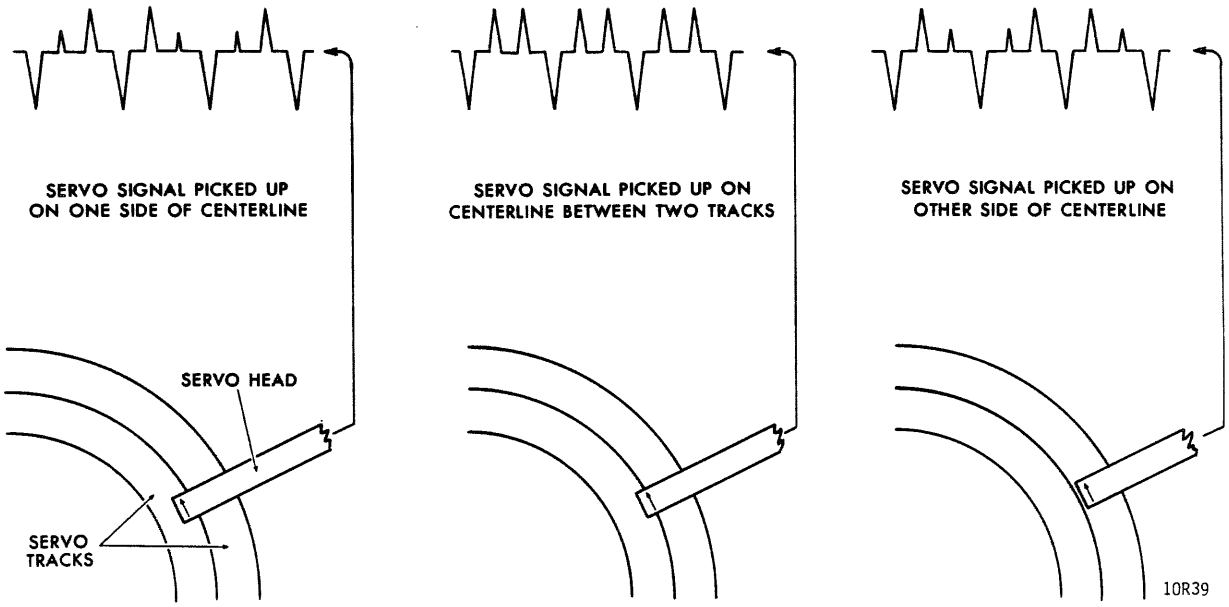


Figure 1-17. Tribit Signal Variations

SERVO SURFACE FORMAT

The servo surface, through its encoding format, establishes the format of the disk data surfaces. The servo surface format divides the disk surfaces into four zones: an 823-track data zone, two guardbands, and a buffer zone. The guardbands indicate areas of the disk that cannot be used for recording of data, and servo encoding extends beyond the normal limits of head positioning. The outer guardband consists of 80 tracks on the outer portion of the disk, including 62 tracks that extend beyond normal outward travel of the heads. The inner guardband consists of 164 tracks on the inner portion of the disk, including 28 tracks allotted for the head landing zone and 63 tracks that extend beyond normal inward travel of the heads. The buffer zone consists of 5 tracks located between the outer guard band and the data zone. In addition, all four zones contain an encoded "reference line" which establishes the logical beginning of each track. When this reference is decoded, the drive sends the Index signal to the controller via the interface.

Figure 1-18 shows the positioning of heads on the module disk surfaces and explains, in the exploded portion of the drawing, how formatting information is encoded on the disk. As described in the Tribit Recording Scheme discussion, five-byte codes are used as format indicators. Each of the five bytes is either an index byte (labelled "1") or a normal byte (labelled "0"). With the two bytes labelled in this manner, each five-byte code can be designated as a five-bit pattern number. Thus, Index, with a pattern number of 11011, is encoded on the disk by two index bytes, followed by a normal byte and two more index bytes. This pattern marks the logical beginning of each servo track. The remaining 79 coded patterns spaced around each servo track depend on the zone for that track. The outer guardband is encoded with pattern 10111, the data zone and buffer zone with pattern 10101, and the inner guardband with pattern 11101.

Refer to the Index and Guardband Decoding discussion for a description of the circuitry that performs this decoding.

TRIBIT DECODER CIRCUIT OPERATION

General

Operation of the tribit decoder circuitry is discussed first in terms of its relation to other systems within the drive. This is followed by explanations of the individual functions performed by the decoder.

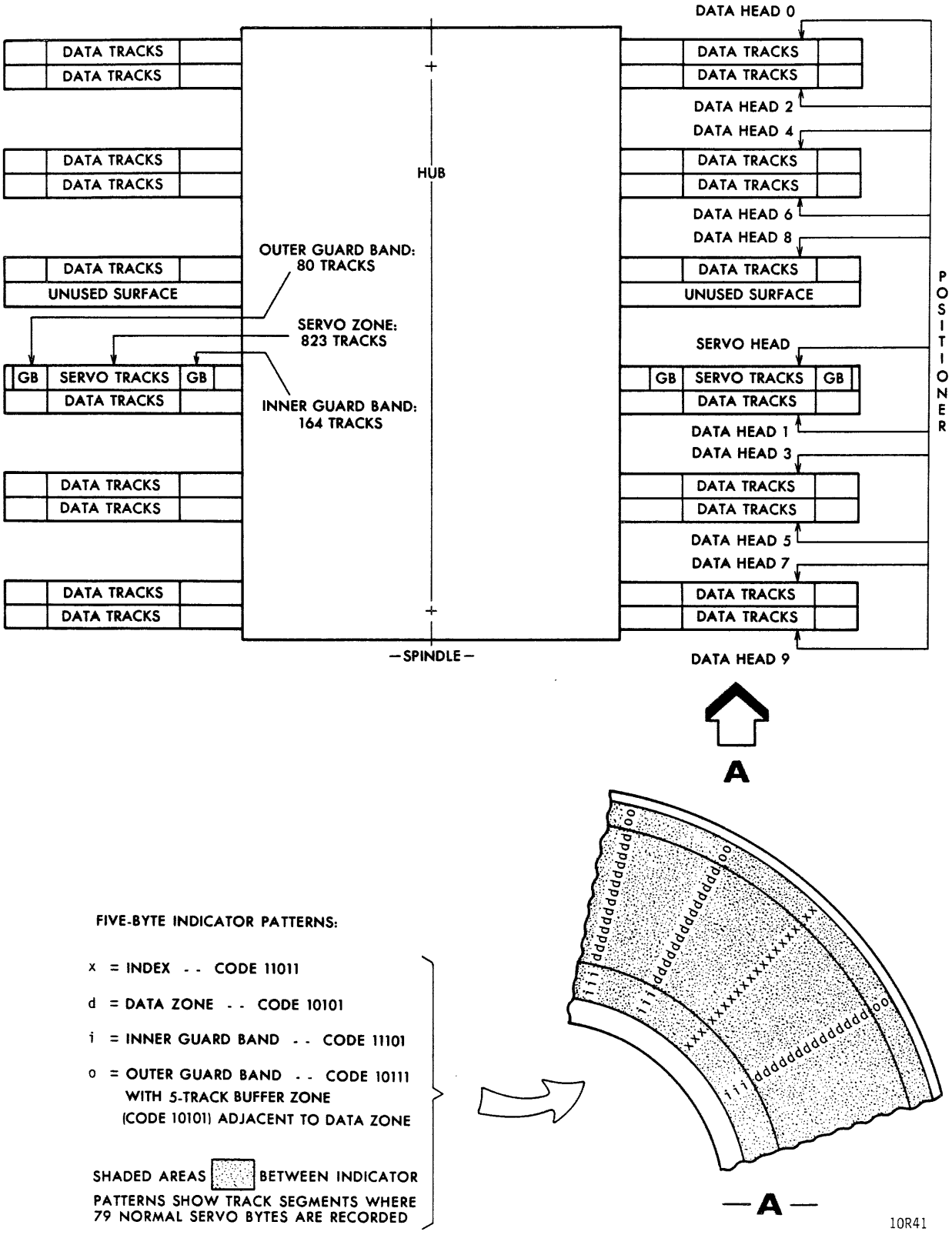


Figure 1-18. Servo Disk Format

Decoding the information present in the servo signal is essential for other functional areas of drive operation. Figure 1-19 is a functional block diagram showing signal flow between the tribit decoder and these other functional areas.

Inputs to the decoder come from the servo preamp and the MPU. The servo preamp amplifies the signal detected by the servo head. The +Slope signal, supplied by the MPU, sets up the phase of the decoded Position signal so that it can be used by the seek circuits.

The MPU monitors three output signals from the decoder. During normal seek operations, the servo head remains over the data zone. Thus, when the Inner or Outer Guard Band Pulses go active, the MPU reacts by altering the seek protocol. Improper decoder operation can affect seek reliability. For this reason, the MPU monitors the -Demodulator OK line.

Data transfers to and from the disk must be coordinated with respect to the rotational position of the disk. The Index signal is decoded and is input to the Sector Detection circuitry which, in turn, generates a given number of Sector pulses per disk rotation. The controller coordinates data transfers based upon the Index and Sector pulses transmitted to it via the interface.

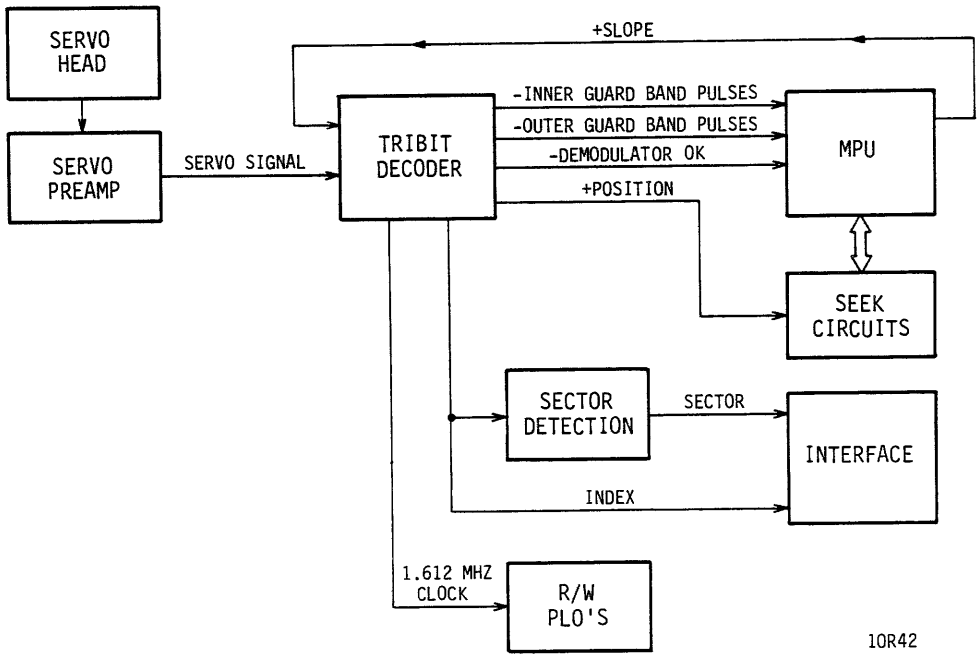


Figure 1-19. Tribit Decoder System Diagram

The 1.612 MHz Clock from the decoder is used by the R/W PLO circuitry to form a 9.67 MHz Servo Clock. The Servo Clock operates at exactly six times the frequency of the 1.612 MHz Clock, and it tracks the rotational velocity of the disk. The controller transfers data to the disk in sync with the Servo Clock. This compensation in the rate of data transfers to the disk makes the written data pattern independent of disk speed.

The remaining topics within this discussion cover the operation of circuits within the tribit decoder. Figure 1-20 is a block diagram showing these circuits and their interconnections.

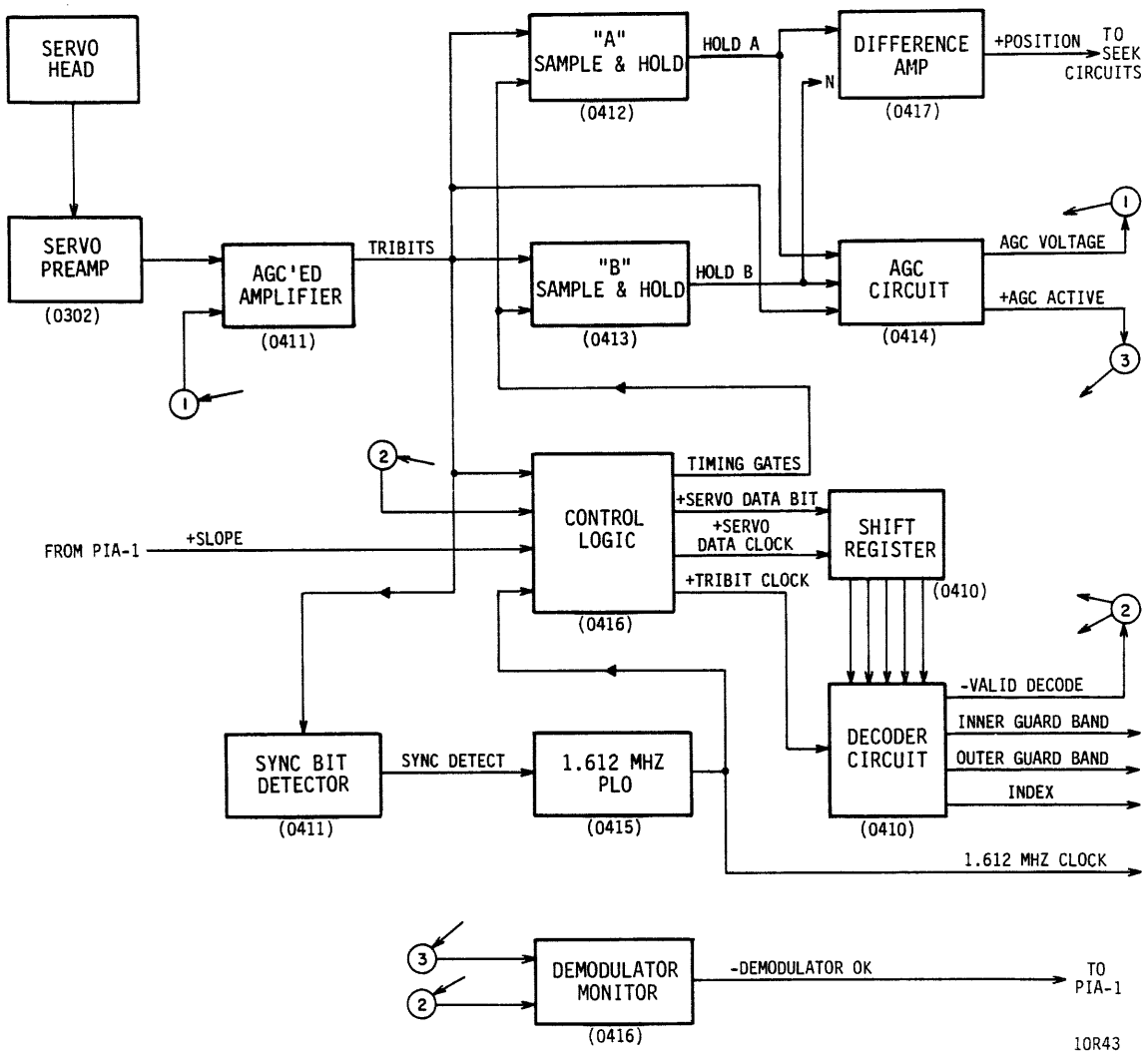


Figure 1-20. Tribit Decoder Block Diagram

Position Demodulation

The control logic subdivides each tribit pattern into four equal intervals in order to regulate measurement of position bit amplitudes by the "A" and "B" Sample and Hold circuits. The Preset gate, active during the first interval, initializes both sampling circuits following the sync bit in each tribit pattern. The two Peak Detect gates, active in the second or third interval, select the position bit to be measured by each sampling circuit. In any two consecutive tribit patterns, a servo track provides one position bit in the second time interval and one position bit in the third time interval. The same two tribit patterns, derived from an adjacent servo track, contain position bits in the opposite time slots. Thus, the Peak Detect "A" gate alternates its active time between the second and third time intervals. For a tribit pattern where Peak Detect "A" is active during the second interval, Peak Detect "B" is active during the third interval. The Transfer gate, active during the fourth interval, inputs the two sampled voltages into the two associated hold circuits where the Hold "A" and Hold "B" signals are adjusted to reflect the latest amplitudes of the position bits.

The Hold "A" and Hold "B" signals follow the peak amplitude of the position bits detected on the two tracks nearest to the servo head. The Hold "A" and Hold "B" signals are input to a difference amplifier to derive the Position signal, an analog signal which is proportional to (Hold "A" - Hold "B"). The Position signal is positive when the servo head is closer to a track containing "A" position bits and is negative when the servo head is closer to a track containing "B" position bits. When the data heads are positioned directly over a data track, the servo heads are centered between two servo tracks and the Position signal is zero.

With one exception, movement of the servo head from one track to an adjacent track reverses the polarity of the Position signal. This is true when the servo head crosses tracks in the guard bands and the data zone. However, the buffer zone, located between the outer guard band and data zone, has five consecutive tracks that are recorded with identical (not alternating) position information. Thus, as the servo head moves across these tracks, the Position signal stays negative and does not cross zero as it does in the other zones. This characteristic of the Position signal is needed for Return to Zero seeks (see Seek Functions).

Initialization of the control logic determines which group of position bits is measured by the "A" Sample and Hold circuit and which group is measured by the "B" Sample and Hold cir-

cuit. The first step in initialization resolves the ambiguity present in the tribit modulation scheme. In successive tribit patterns from a given servo track, the position bit alternates between two possible locations. Throughout drive operation, the -Valid Decode signal is returned to the control logic immediately after each five-byte format code appearing at regular intervals on the servo track. At this time, the Peak Detect "A" and "B" gates are forced to match the format of the tribits as they were recorded on the servo surface. The second step in initialization occurs each time a new seek is commanded. By setting the level of the +Slope signal, the MPU can cause the waveforms of the Peak Detect "A" and "B" gates to be interchanged. Interchanging Peak Detect "A" and "B" inverts the Position signal and allows the MPU to ensure that the +Position signal will have the required slope as the seek circuits position the heads at their new destination. This slope requirement is discussed further under Seek Functions.

Tribit Decoder PLO

The PLO in the tribit decoder generates a clock signal that establishes the basic timing for the tribit decoder control logic and is used as the reference frequency to develop Servo Clock. The PLO oscillates at a nominal frequency of 1.612 MHz, which is four times the repetition rate of sync bits in the detected servo signal. The PLO is part of a phase-locked loop that phase modulates the PLO to keep its output under the control of the sync bit repetitions. Thus, any variation in the rotational speed of the disk produces a proportional variation in the 1.612 MHz clock frequency.

Figure 1-21 is a block diagram of the phase-locked loop, and figure 1-22 is a timing diagram for the circuit.

As shown in the block diagram, the tribit signal is input to a zero cross detector which produces a Sync Detect pulse at every Sync bit and Servo Data bit in the servo signal. To prevent Servo Data bits from affecting the PLO frequency, the Servo Data Bit Inhibitor produces -PLO Drive pulses only for the Sync bits in the Sync Detect signal. The -PLO Drive pulses are narrowed, inverted, and applied to the Set input of the Phase Comparison FF. At approximately the midpoint between -PLO Drive pulses, a Reset pulse is applied to the Phase Comparator FF. The Reset pulse is developed as follows: the 1.612 MHz output of the PLO is divided by four to produce the Q1 signal, a square wave whose frequency matches the repetition rate of the Sync bits. The negative transitions of Q1 coincide with the -PLO Drive pulses, and the positive transitions are 180° out of phase with the negative transitions. A pulse slimmer circuit reduces the length of the Q1 positive oscillation to produce a narrow Reset pulse for the Phase Comparator FF.

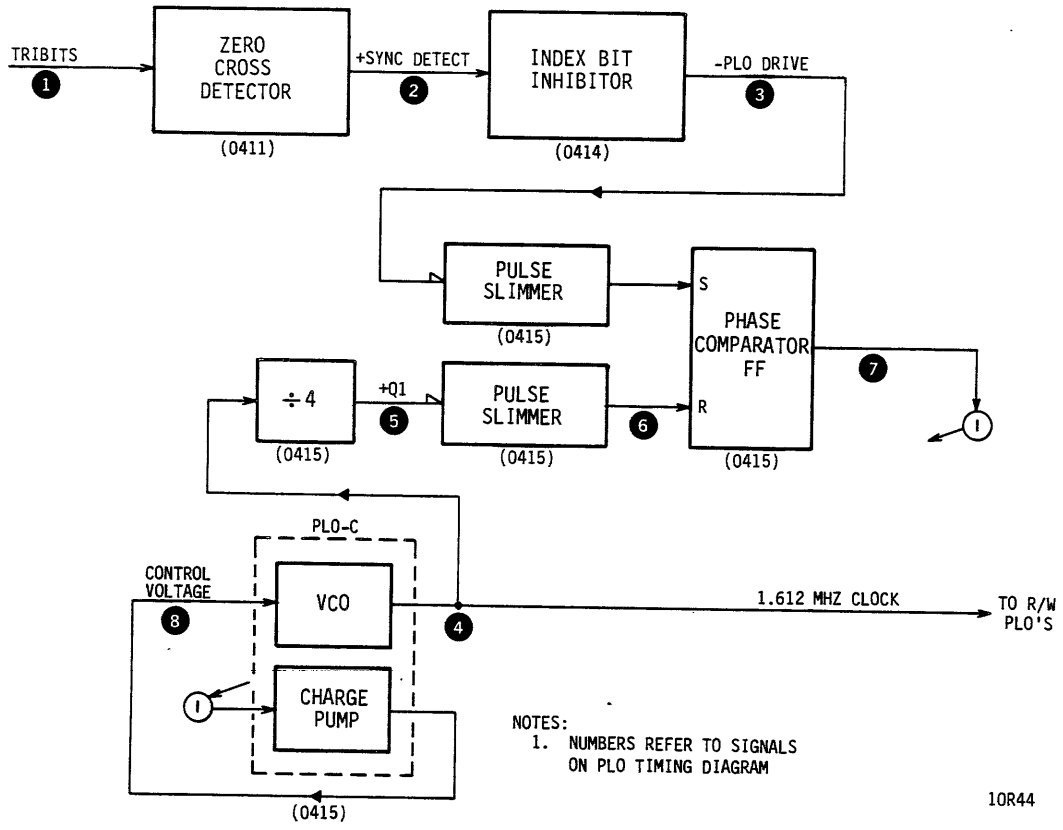
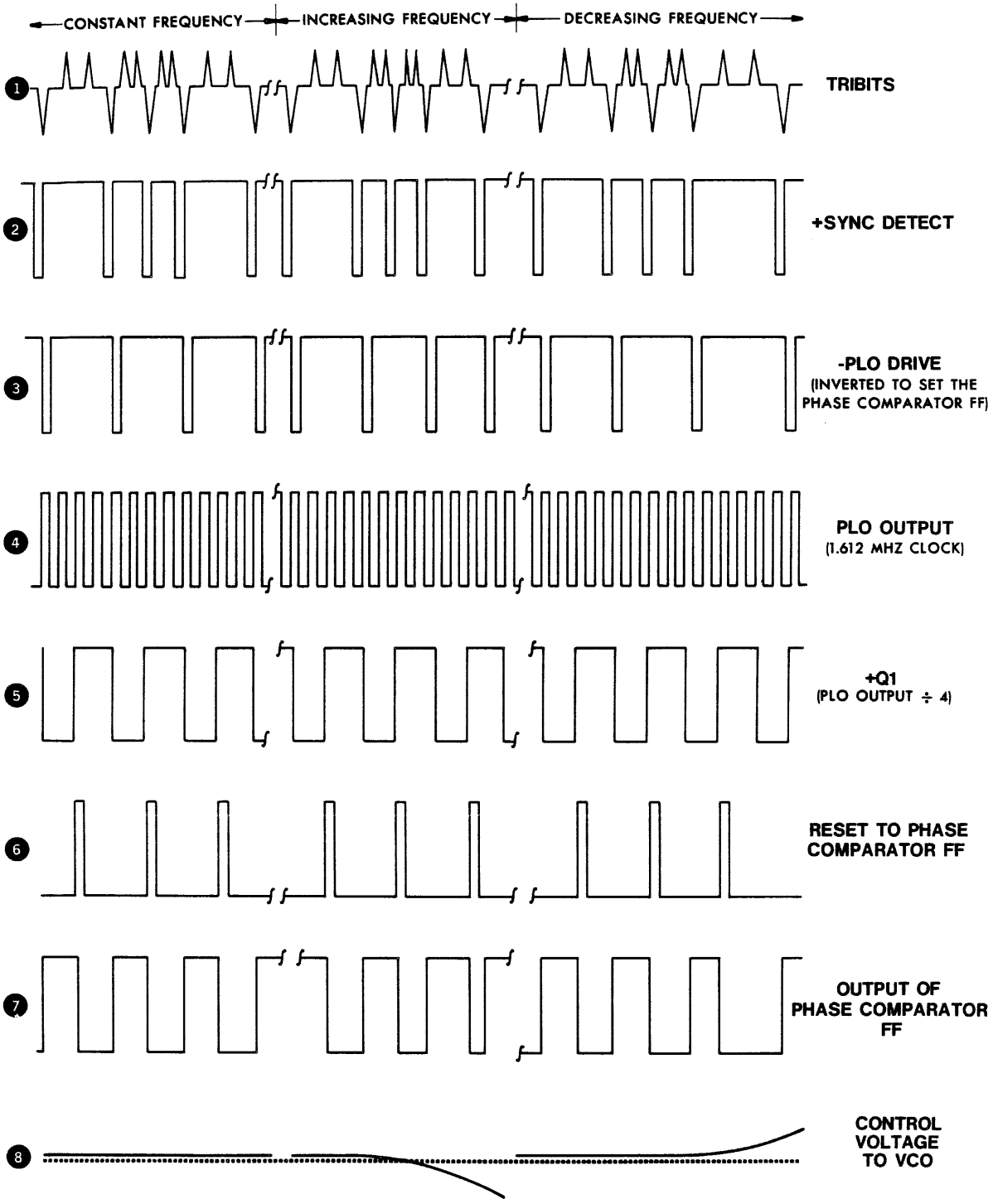


Figure 1-21. PLO Block Diagram

The Phase Comparator FF causes the PLO to shift in frequency when the set interval and the cleared interval of the FF are not equal. This frequency shift is governed by the charge pump within the PLO. The charge pump supplies a control voltage to the voltage-controlled oscillator (the VCO is also part of the PLO): the charge pump looks at the set and cleared intervals of its input signal (from the Phase Comparator FF) and varies the control voltage from its normal value depending on the balance of the two intervals. The control voltage, in turn, shifts the VCO frequency as needed to phase lock the VCO signal, via the feedback loop, to the -PLO Drive signal.



NOTE:

1. NUMBERS REFER TO SIGNALS ON PLO BLOCK DIAGRAM

10R45

Figure 1-22. PLO Timing

Three timing situations are shown in figure 1-22. When the VCO frequency is correct, the set and cleared intervals of the Phase Comparison FF are equal, the control voltage is normal, and the frequency of the VCO stays the same. When the VCO frequency is too high, the Reset input to the Phase Comparison FF is early, and the FF is cleared longer than it is set. This causes the charge pump to shift the control voltage more positive than normal which, in turn, decreases the VCO frequency. When the VCO frequency is too low, the Reset input to the Phase Comparison FF is late, and the FF is set longer than it is cleared. This causes the charge pump to shift the Control Voltage more negative than normal which, in turn, increases the VCO frequency.

Index and Guard Band Decoding

The index and guard band decoding circuitry produces output pulses each time the servo head detects format indicators on the servo surface. This circuitry also originates the -Valid Decode signal which is used to initialize the position demodulating circuitry. Refer to Servo Surface Format for a description of the format indicators and their location on the servo disk.

Figure 1-23 is a block diagram of the index and guard band decoding circuitry. Figure 1-24 shows the timing relations when the index pattern is decoded from the servo signal. In guard band decoding, the same timing relations apply, but the servo signal input is different.

Index and guard band information is decoded from the servo signal in three steps. The control logic develops intermediate signals from the servo tribit pattern. These signals, in turn, operate a shift register that contains information about the last servo bytes detected. Finally, the decoder samples the shift register contents each byte, and when the register contents match one of the format indicators, the decoder activates the corresponding output line.

As shown in figure 1-24, the +Servo Data Bit line goes active when a Servo Data bit occurs and stays active until the next Sync bit. The +Servo Data Bit signal is the D-input to a five-stage shift register. A timing signal, called +Servo Data Clock, is developed by the control logic. The leading edge of +Servo Data Clock, which occurs just prior to each sync bit, shifts the +Servo Data Bit signal into the shift register. Thus, the shift register indicates whether each of the last five servo bytes were index bytes or normal bytes. A decoder circuit monitors the five outputs of the shift register. The decoder circuit is enabled only during the first half of each servo byte, when the control logic activates the +Tribit Clock line.

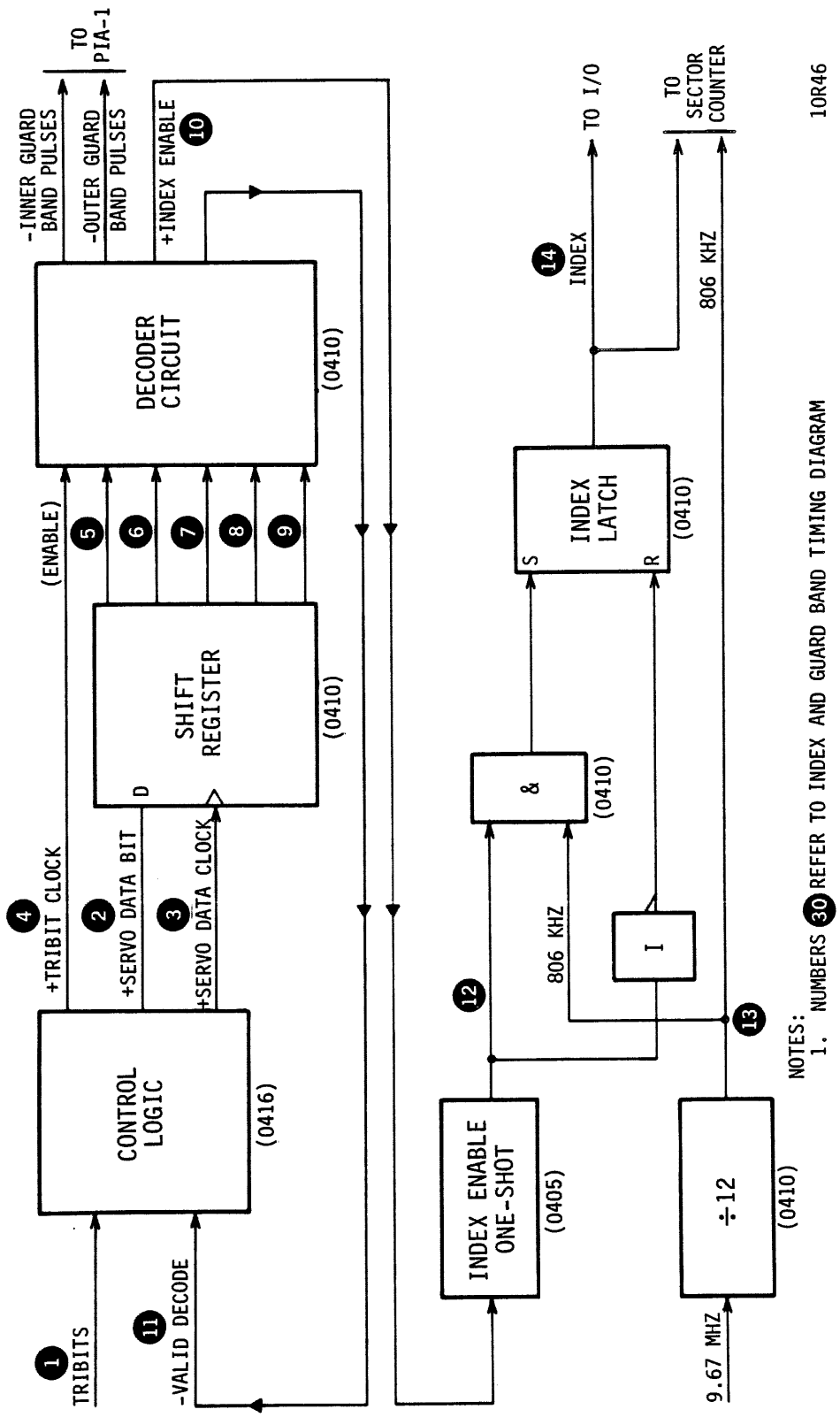


Figure 1-23. Index and Guard Band Decoding Circuitry

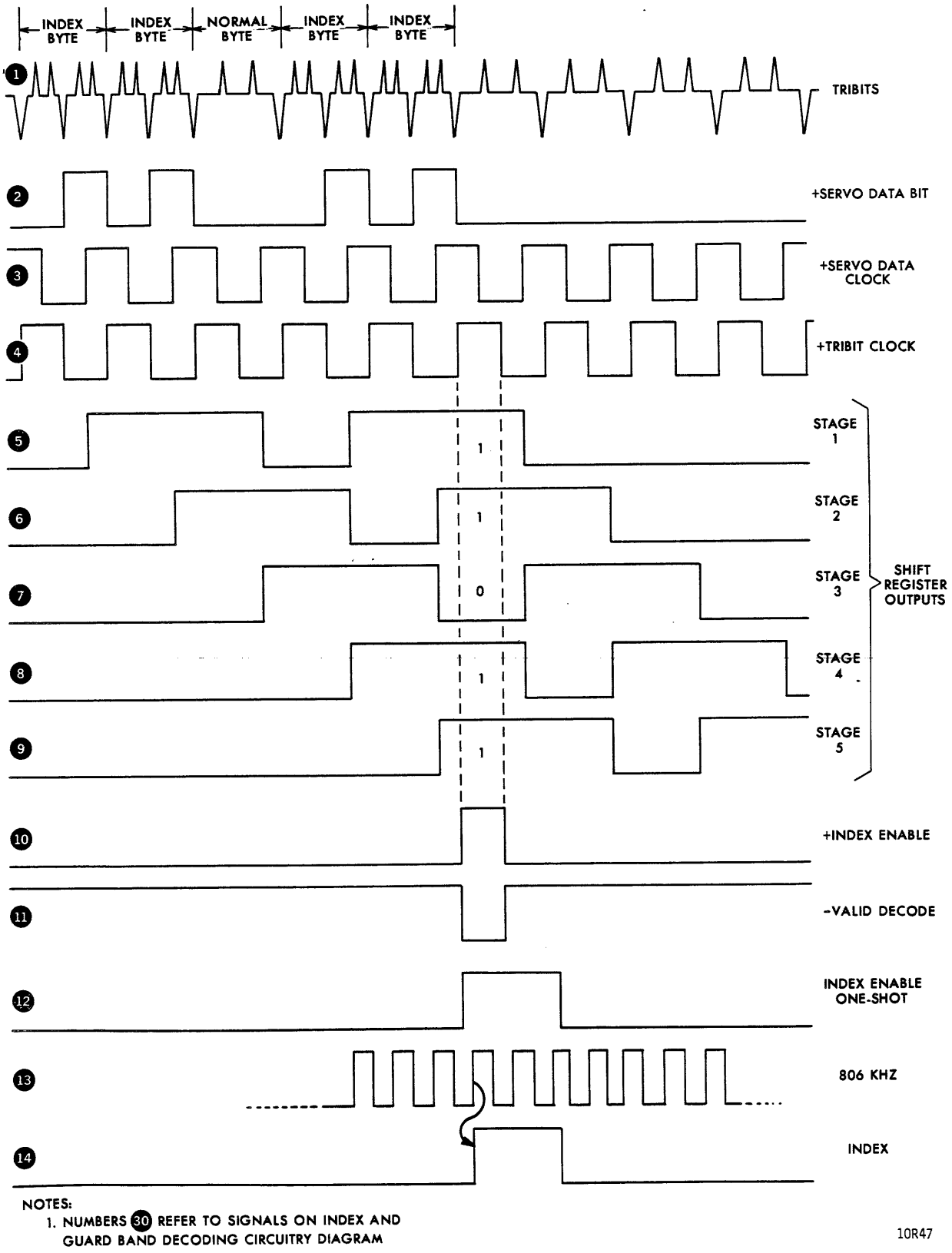


Figure 1-24. Timing Relations in Index Decoding

The decoder recognizes specific patterns in the shift register by activating its output lines as follows:

- When the register contains 11011, there are active pulses on the +Index Enable and -Valid Decode lines.
- When the register contains 10111, there are active pulses on the -Outer Guard Band Pulses and -Valid Decode lines.
- When the register contains 11101, there are active pulses on the -Inner Guard Band Pulses and -Valid Decode lines.
- When the register contains 10101, there is an active pulse on the -Valid Decode line. This code is produced by format indicators in the data zone and has no individual decoder output.

Additional circuitry extends the Index pulse to 2.5 microseconds and synchronizes the timing of Index to the Sector pulses produced by the Sector Counter. The Index Enable pulse triggers a 2.5 microsecond one-shot. The one-shot output is ANDed with an 806 kHz clock, the timing signal for the Sector Counter, to set the Index latch. The Index latch is cleared when the Index Enable one-shot output goes inactive. Operation of the Sector Counter is described under Sector Detection.

Sector Detection

The sector detection circuit (figure 1-25) generates signals which are used by the drive to determine the angular position of the heads with respect to index. These signals are called Sector pulses and a specific number of them are generated during each revolution of the disks. The Sector pulses logically divide the disk into areas called sectors.

The Sector pulses are generated by the Sector counter which generates a pulse each time it reaches its maximum count (4095). The counter is incremented by the 806 kHz clock pulses. These clock pulses are derived from the 9.67 MHz Servo Clock and represent the beginning of each data byte. The Index pulse resets the counter allowing 13 440 clock pulses per revolution of the disk.

The fact that the same number of 806 kHz clock pulses occur during each revolution makes it possible to program the counter to reach the maximum count (thus generating a Sector pulse) any desired number of times per revolution. This is done by presetting the counter to the proper value at the beginning of each sector. For example, if it is desired to have 64 sectors,

the counter would have to count 210 clock pulses in each sector (13 440 divided by 64) and the counter would be preset to 3886. In this case, the counter starts at 3886 and increments each clock time until it reaches the maximum count (4095). Reaching the maximum count causes the Sector pulse to be generated. The next clock pulse (210) presets the counter back to 3886 (thus disabling the Sector pulse) and the counter begins the next sector.

The sector length is varied by presetting the sector switches located on the control board. Refer to Volume 1 of the maintenance manual for details regarding the setting of the sector switches.

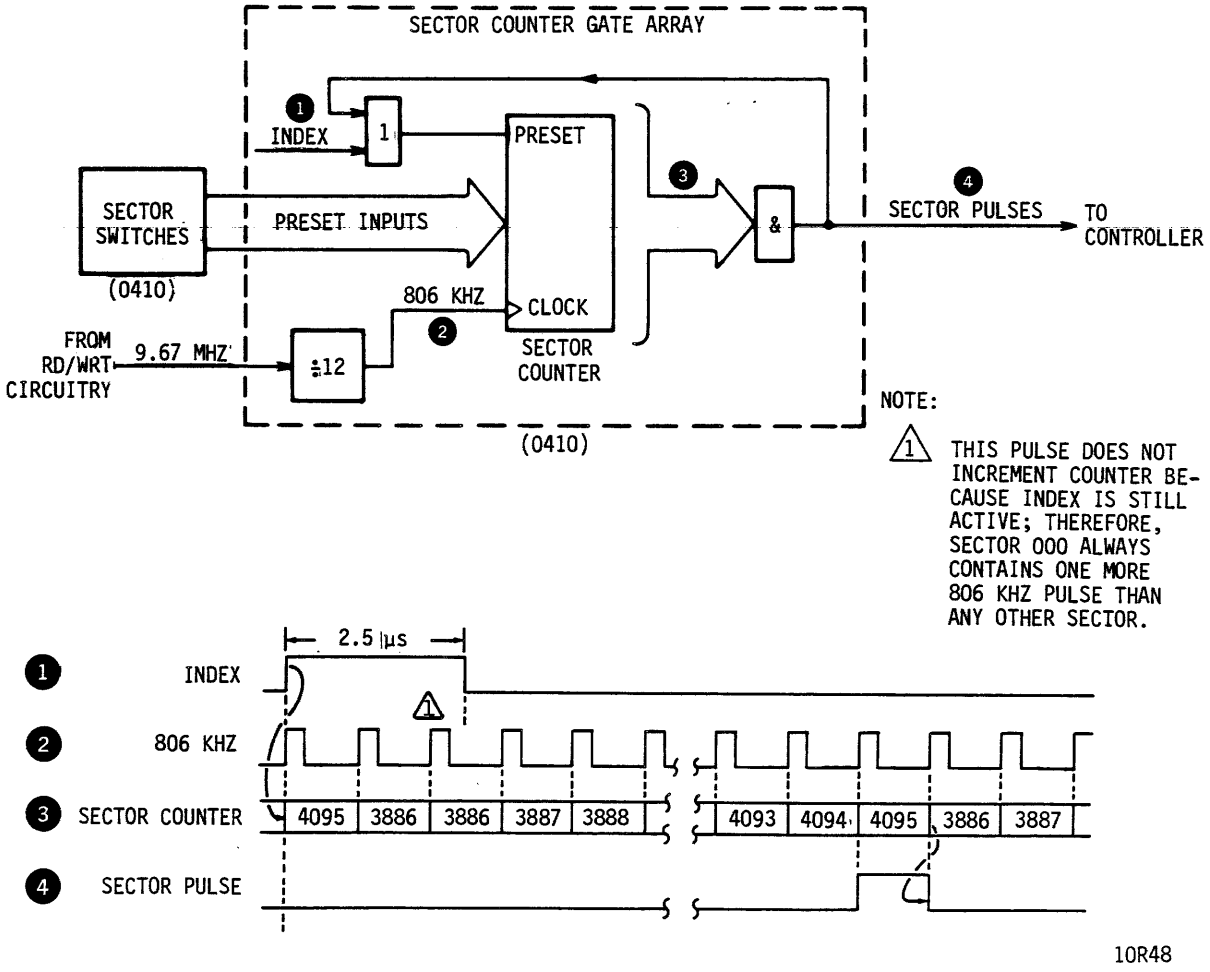


Figure 1-25. Sector Detection - Logic and Timing

SEEK FUNCTIONS

GENERAL

During seek operations, the drive positions the heads over the desired cylinder on the disk. The drive servo circuits, under the direction of a microprocessor unit (MPU), control this function. The drive servo circuits translate MPU instructions into electromechanical motion to position the read/write heads accurately and to allow the transfer of magnetic pulses to and from a disk storage surface. The two main topics of this section describe servo circuit operation and the sequencing of events in different types of seeks. Since these subjects are interrelated, they are preceded by an overview of system operation that explains the roles played by the interface and the MPU, and that describes the servo functions in general terms.

SYSTEM OVERVIEW

Each seek operation can be described in terms of four basic drive activities. These activities are shown in terms of general information flow between major drive functional elements in figure 1-26. These activities occur in the following sequence:

- Command -- The interface processes the command from the controller that instructs the drive to seek to a different cylinder on the disks.

- Control -- The MPU interprets the seek command, then translates the command into a sequence of controls sent to the servo circuitry. These controls dictate the direction of the seek, specify actuator velocity throughout the seek, and step the servo through its operating modes.

- Execution -- The servo circuitry executes the seek in response to control information received from the MPU. This execution is accomplished in three modes: the coarse mode, during which the actuator is moved at a controlled velocity toward its destination; the settle-in mode, in which the actuator locks in to its final position; and the track-following mode, in which the actuator position is maintained until another seek is commanded. The servo controls current to the voice coil to move the actuator/heads via in and out drive signals to the power amp. Position information from the tribit decoder serves as a feedback source to the servo loop and is converted into cylinder crossing information for the MPU.

- Status -- The MPU informs the controller via the interface whether or not the seek was accomplished successfully. This indicates whether or not a reliable data transfer can be performed on the selected cylinder.

The concept of a closed loop is essential to understanding the operation of the servo system. Figure 1-27 shows a generalized servo loop that illustrates several principles governing the servo loops in the drive. The inputs to the summing amp are added, and any departure of the sum away from zero indicates that the system is unbalanced. To compensate for the imbalance, the summing amp issues a correction signal to the mechanical system. The response of the mechanical system is converted into an electrical signal which is an input to the summing amp. Mechanical movement continues until the system balance is restored, corresponding to a null in the summing amp inputs.

The Drive employs two basic servo loops, a coarse loop used in the coarse mode and a fine loop used in the settle-in and track-following modes. In figure 1-28, the model of figure 1-27 is used to show the coarse servo loop in simplified form. In the coarse loop, the actuator moves at a prescribed velocity from the original cylinder address to the final cylinder address. The summing amp receives two inputs -- one signal

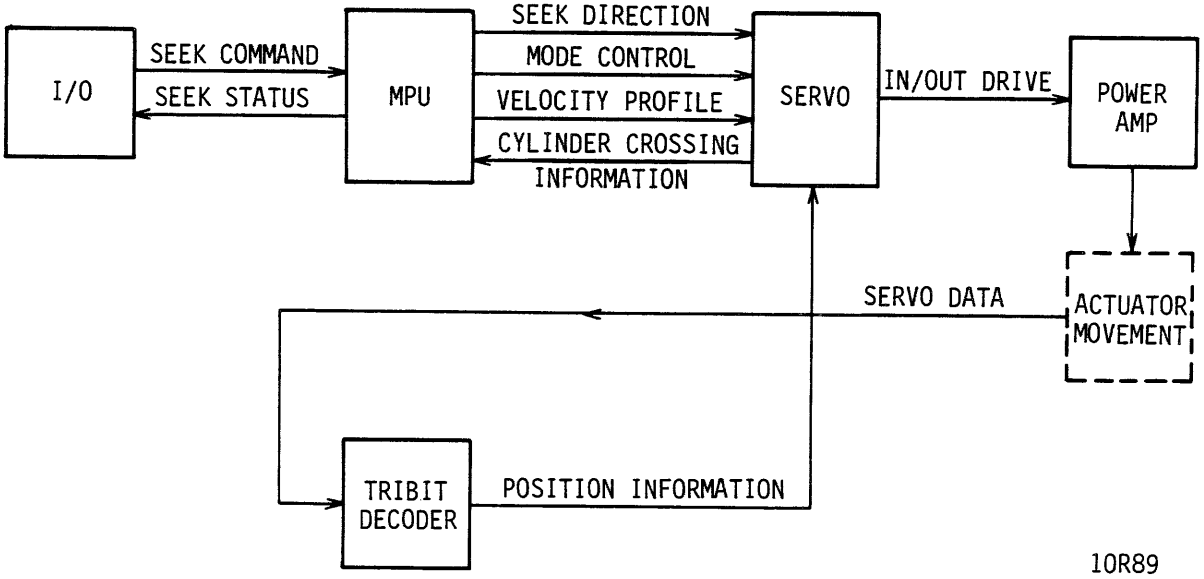


Figure 1-26. Seek Functions Block Diagram

represents the prescribed (desired) velocity of the actuator and the other represents the measured velocity of the actuator. When the desired velocity exceeds the measured velocity, desired current is produced to accelerate the actuator. When the measured velocity exceeds the desired velocity, desired current is produced to decelerate the actuator. The actuator is allowed to coast when the two inputs are equal.

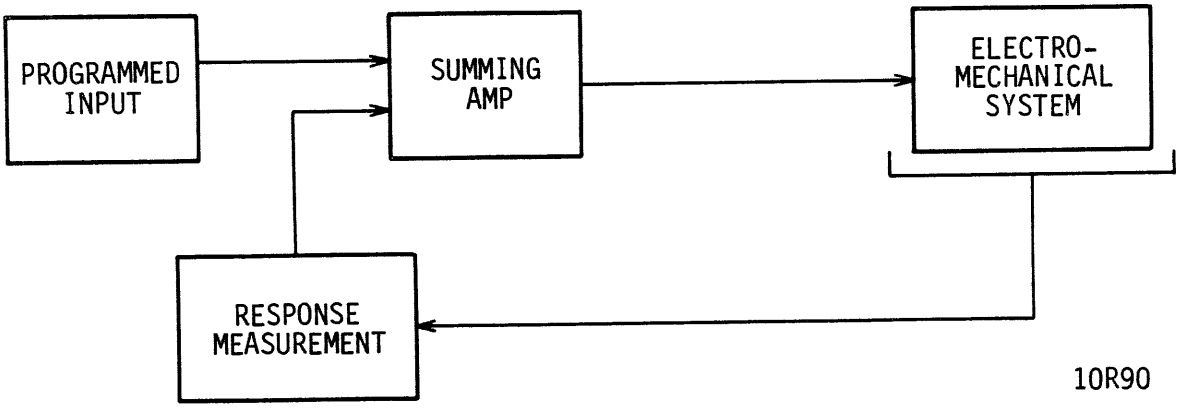


Figure 1-27. Generalized Servo Loop

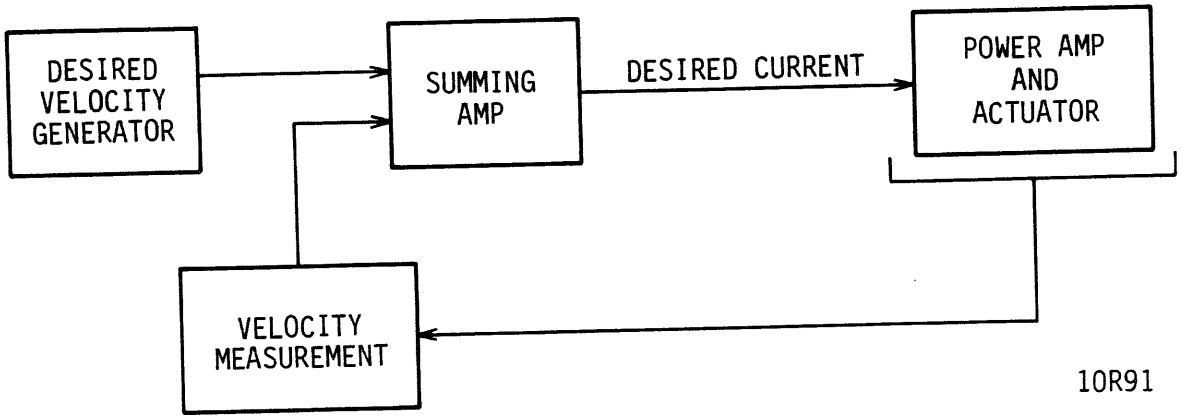


Figure 1-28. Simplified Coarse Servo Loop

In figure 1-29, the model of figure 1-27 is used to show the fine servo loop in simplified form. In the fine loop, the heads settle-in to their destination position and then maintain their position on track. The summing amp has no programmed input. Its only input is the Position signal, which is nulled at track center and varies positive or negative depending on how far the heads are displaced from track center. Any displacement of the heads from track center is adjusted by the fine loop until the summing amp input is nulled.

The following paragraphs discuss the circuit operation of these loops in more detail and then go on to describe the sequence of events in typical seeks.

SERVO CIRCUIT FUNCTIONS

General

Servo circuit functions are discussed in terms of the two basic loops within the servo circuitry (coarse and fine loops). The coarse loop and the fine loop have some circuit elements in common. These common circuit elements are described in detail under Coarse Loop Operation and are mentioned briefly under Fine Loop Operation. Seek operations follow defined sequences in which the MPU exercises control over the servo circuitry. These sequences are described under the next topic, Types of Seeks.

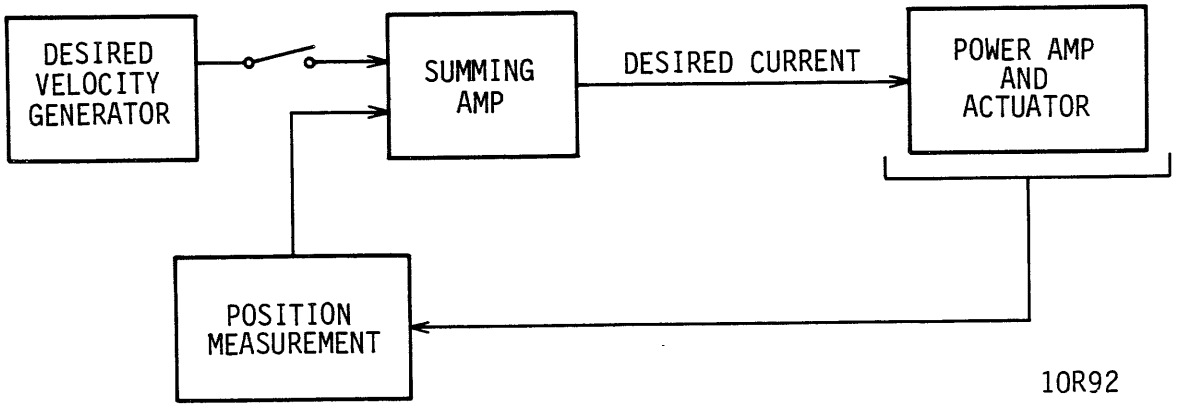


Figure 1-29. Simplified Fine Servo Loop

Coarse Loop Operation

General

The servo system, operating in the coarse loop, moves the heads from the existing cylinder address to within one half track of the new address. Figure 1-30 is an overall block diagram of the coarse loop circuitry. Discussion of the coarse loop is presented in the following topics:

- Microprocessor Control System
- Desired Velocity Generation
- Cylinder Pulse Detection
- Velocity Measurement
- Summing Amp
- Power Amp Drive
- Power Amplifier

Microprocessor Control System

The microprocessor control system monitors various functions of the drive and executes most of the control sequences required for seek functions. The following paragraphs provide a general description of the components and signal paths in the microprocessor system, and describe the role of the microprocessor system pertaining to seek functions. Figure 1-31 is a block diagram of the microprocessor system. Readers interested in internal operation of the microprocessor and its peripheral chips may refer to the CDC Microcircuits Manual for more information.

The microprocessor control system consists of a 6802 microprocessor unit (MPU), a 4K-byte read-only memory (ROM), three peripheral interface adapter (PIA) chips, and a programmable timing module (PTM). The MPU communicates with its peripheral chips via an 8-bit bidirectional data bus, a 16-bit address bus, and several control lines. Circuitry within the Address Decode Gate Array monitors Address lines 12 through 14 and develops chip select signals for each peripheral chip whenever the Valid Memory Address line is active. The MPU sets the Read line to read data from a peripheral or clears the line to write data into a peripheral. The Phase 2 Clock, developed by a crystal-controlled oscillator in the MPU, provides a timing reference for the system.

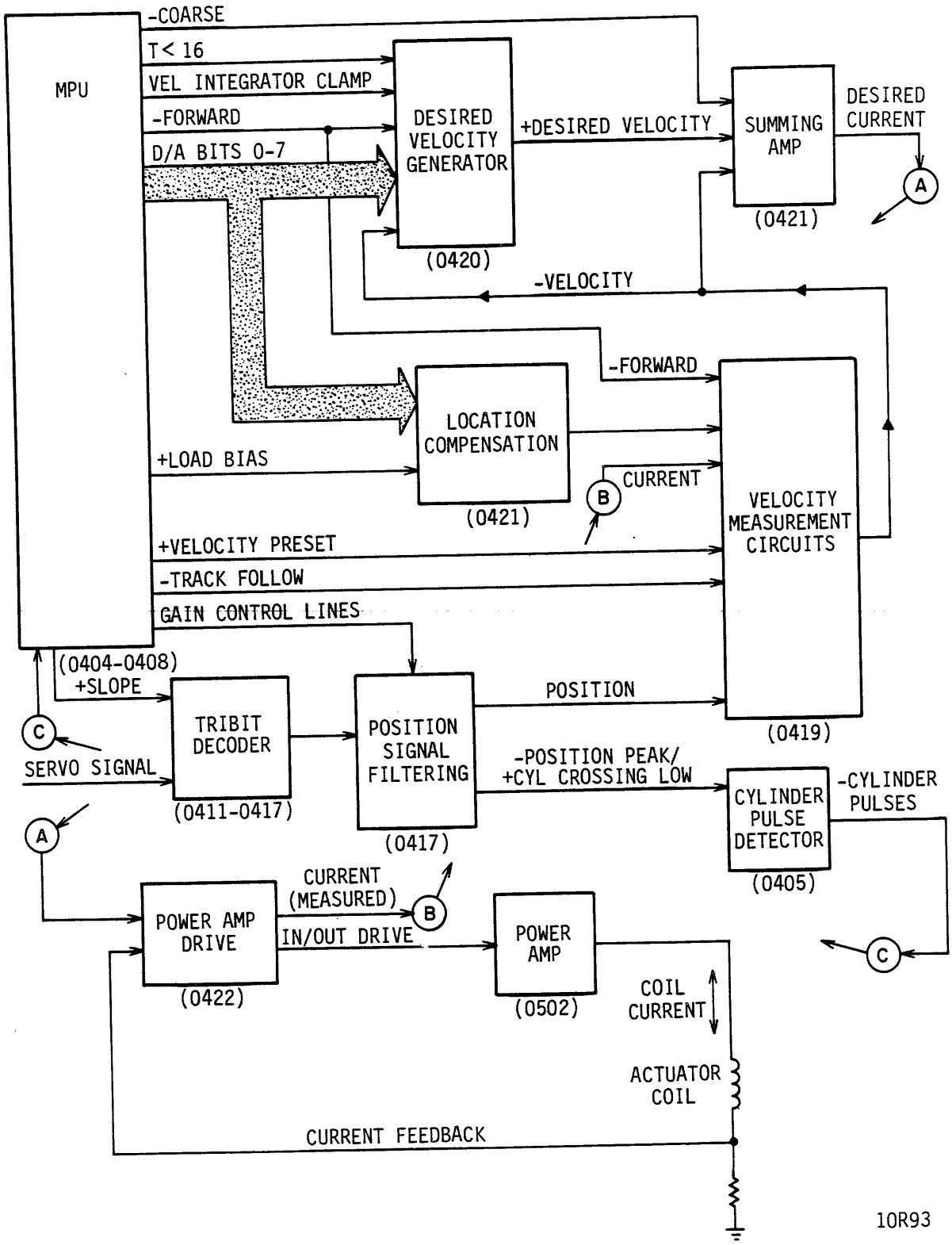


Figure 1-30. Coarse Loop Block Diagram

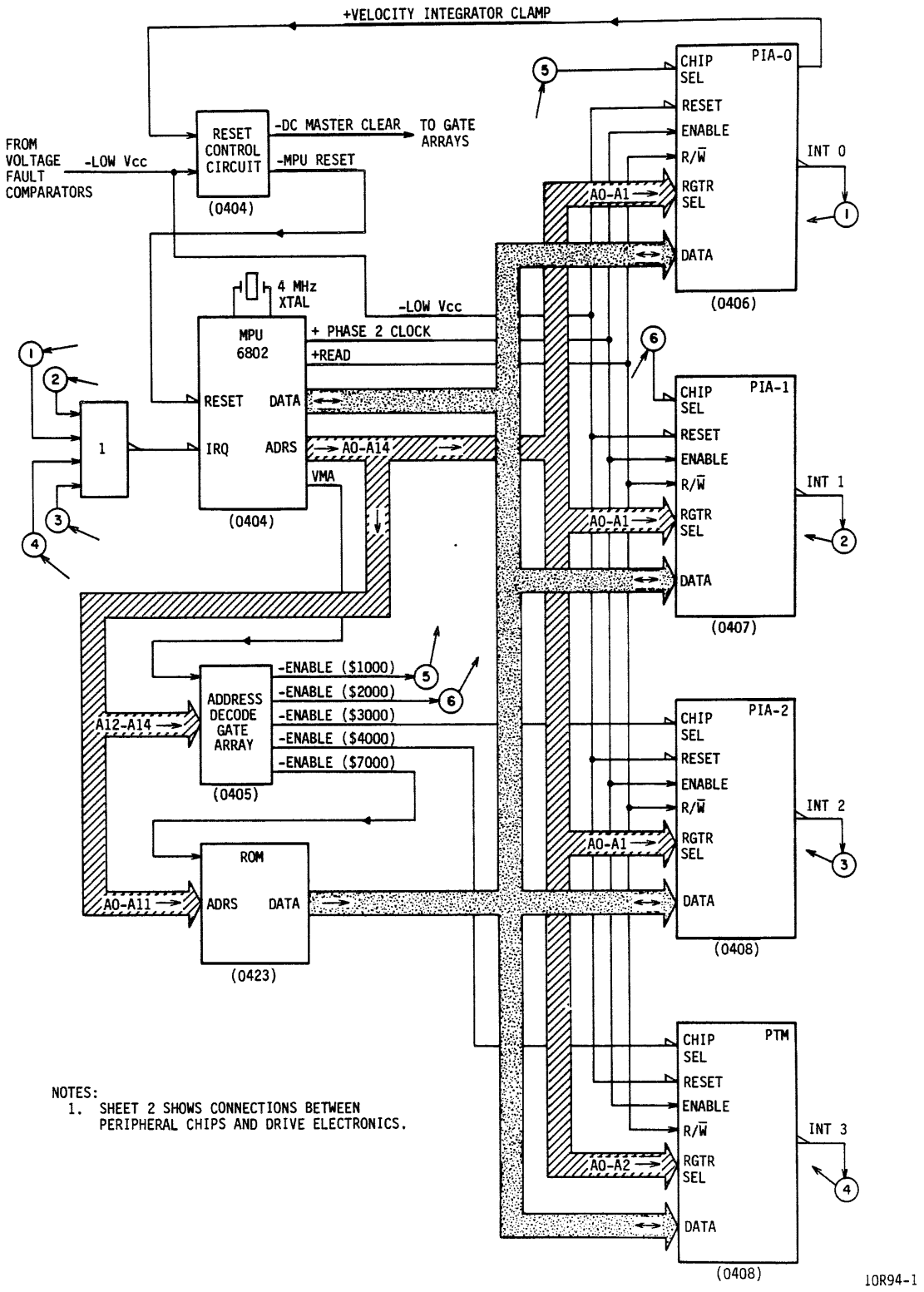


Figure 1-31. Microprocessor Control System (Sheet 1 of 2)

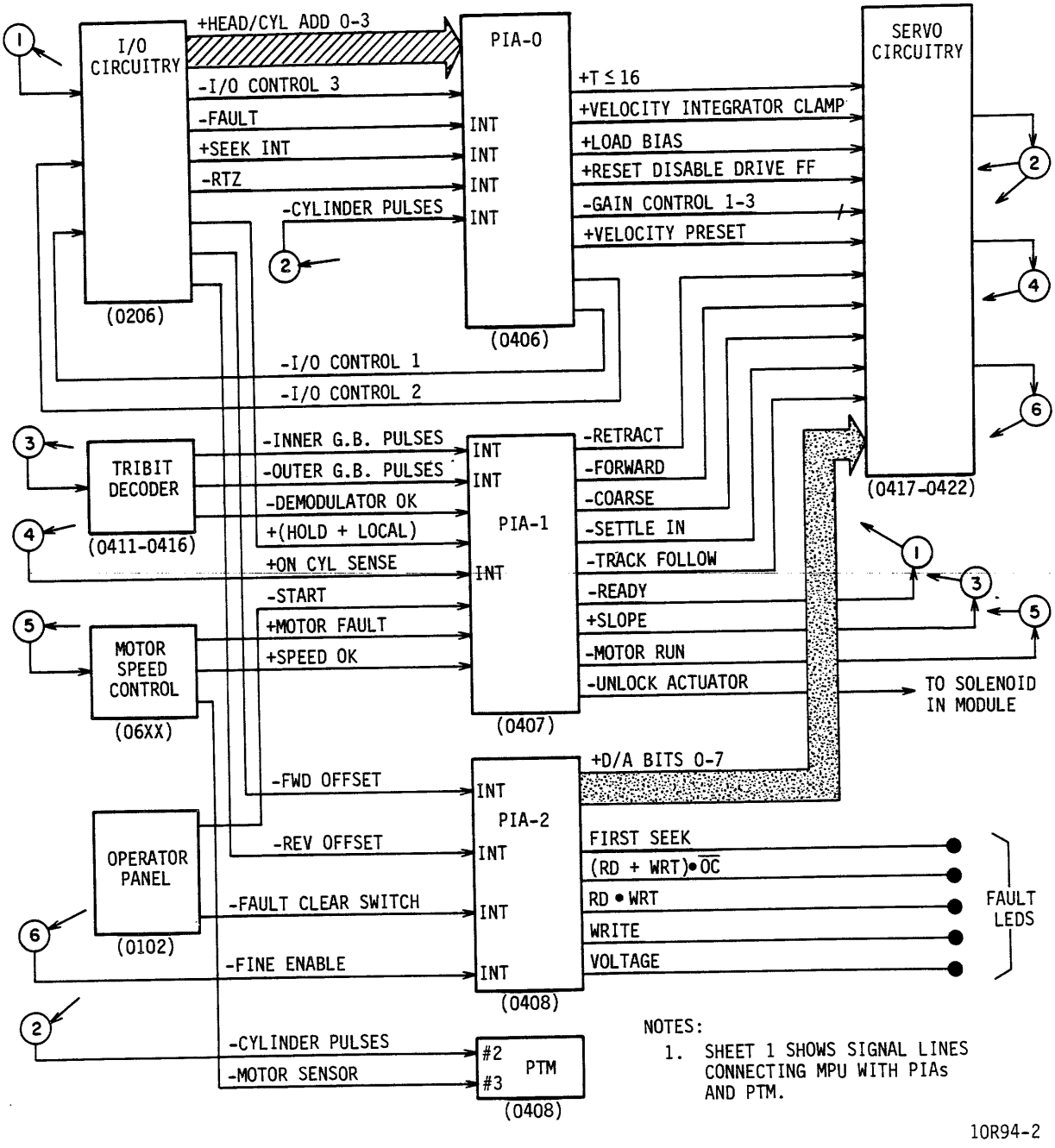


Figure 1-31. Microprocessor Control System (Sheet 2)

The firmware instructions for the MPU reside in the ROM. Detailed information about the MPU programming is beyond the scope of this manual. However, the various sequences which the MPU performs are outlined under Power Functions and Types of Seeks. The ROM also contains a lookup table that specifies a velocity profile for normal seeks.

The PIAs allow the MPU to monitor the digital levels of certain signals developed in hardware external to the microprocessor system. In addition, the MPU can output various command signals via the PIAs. Certain PIA input signals form maskable interrupts to the MPU. When unmasked, these interrupts inform the MPU of status changes that require switching to a different routine within its firmware. The specific PIA inputs and outputs are listed in figure 1-31 and are referenced in the applicable circuit descriptions. A set of PIA lines requiring additional explanation includes I/O Control lines 1, 2, and 3. I/O Control lines 1 and 2 go from PIA-0 to the I/O Gate Array. These lines allow the MPU to perform various operations inside the gate array, such as setting the On Cylinder and Seek Error FFs, multiplexing cylinder and head addresses out of the array, and reading the status of various faults via the I/O Control 3 line.

Within the PTM, counter #2 allows the MPU to count tracks-to-go in a seek. This counter is decremented during seeks by cylinder pulses. Counter #3 is used by the MPU to generate timeouts for various operations and to make speed checks of the drive motor.

The MPU system performs the following basic functions during drive operation:

- It monitors start and interlock conditions to initiate load and retract operations.
- It starts and stops the drive motor, and it checks motor speed.
- It monitors the Seek Interrupt line and executes normal seeks.
- It specifies the desired actuator velocity during coarse seeks.
- It monitors the RTZ Interrupt line and executes RTZ seeks.
- It controls the On Cylinder and Seek Error FFs in the I/O Gate Array.

These functions are described in detail in the remainder of Seek Functions. In addition, the MPU exchanges fault status with the I/O Gate Array. This activity is discussed under Fault and Error Conditions.

Desired Velocity Generation

The desired velocity circuit generates the +Desired Velocity signal, a changing analog voltage that indicates the desired velocity of the actuator throughout the coarse mode of the seek. Throughout the seek, the MPU refers to a table in the ROM that specifies desired velocity in binary form as a function of the number of tracks to go (T), which is the number of track crossings remaining until the heads reach their destination.

The velocity table is organized in a manner that allows one table of values to be used for all seeks. The maximum velocity of the table is for 255 tracks, and as the values decrease, a velocity profile is developed whereby velocity is proportional to the square root of the distance remaining. This profile produces constant deceleration of the heads in order to minimize seek times while controlling the approach of the heads to their final position. The organization of tabulated velocity in terms of tracks to go makes it possible to use one table for all seeks. Different seek lengths start at different points within the table. For example, the velocity specified when T=30 is the same regardless of the total seek length.

The desired velocity circuit provides a ramp signal from the D/A (Digital to Analog) Converter based upon the eight D/A Bits it receives from the ROM table via PIA-2 (see figure 1-32). When $T \leq 16$, however, the two uppermost D/A bits are masked out at the D/A and are used elsewhere, and the +Velocity Integrator Clamp signal is input via PIA-0 to provide a sawtooth signal from the Velocity Integrator to add fill-in current to the ramp as the heads approach the selected track. At each cylinder crossing, the MPU refers to a count of tracks to go in PTM Counter #2 and outputs the current value of tabulated velocity using the D/A Bits. Each change in the D/A Bits results in a stepped change in the D/A ramp. Typical waveforms for the desired velocity circuit are given in figure 1-33.

The sawtooth from the Velocity Integrator compensates for the stepped nature of the D/A ramp by filling in the sudden changes in the ramp. When $T \leq 256$, the sawtooth output is obtained by integrating the -Velocity signal from the velocity circuit. This output is clamped to zero each time a cylinder crossing occurs. D/A Bits 6 and 7 are reserved for controlling the degree of filling provided by the sawtooth in the final portion

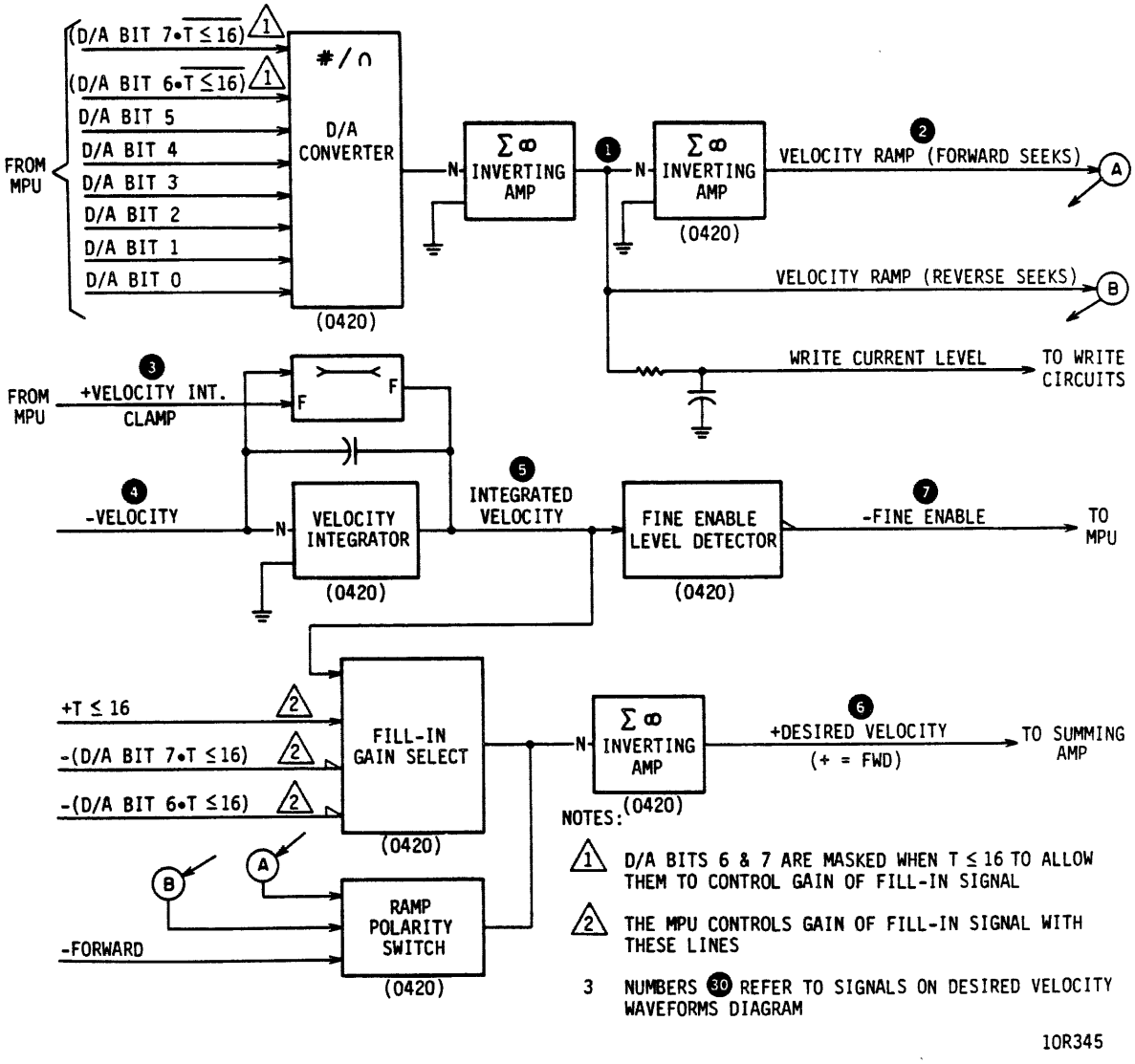


Figure 1-32. Desired Velocity Circuit

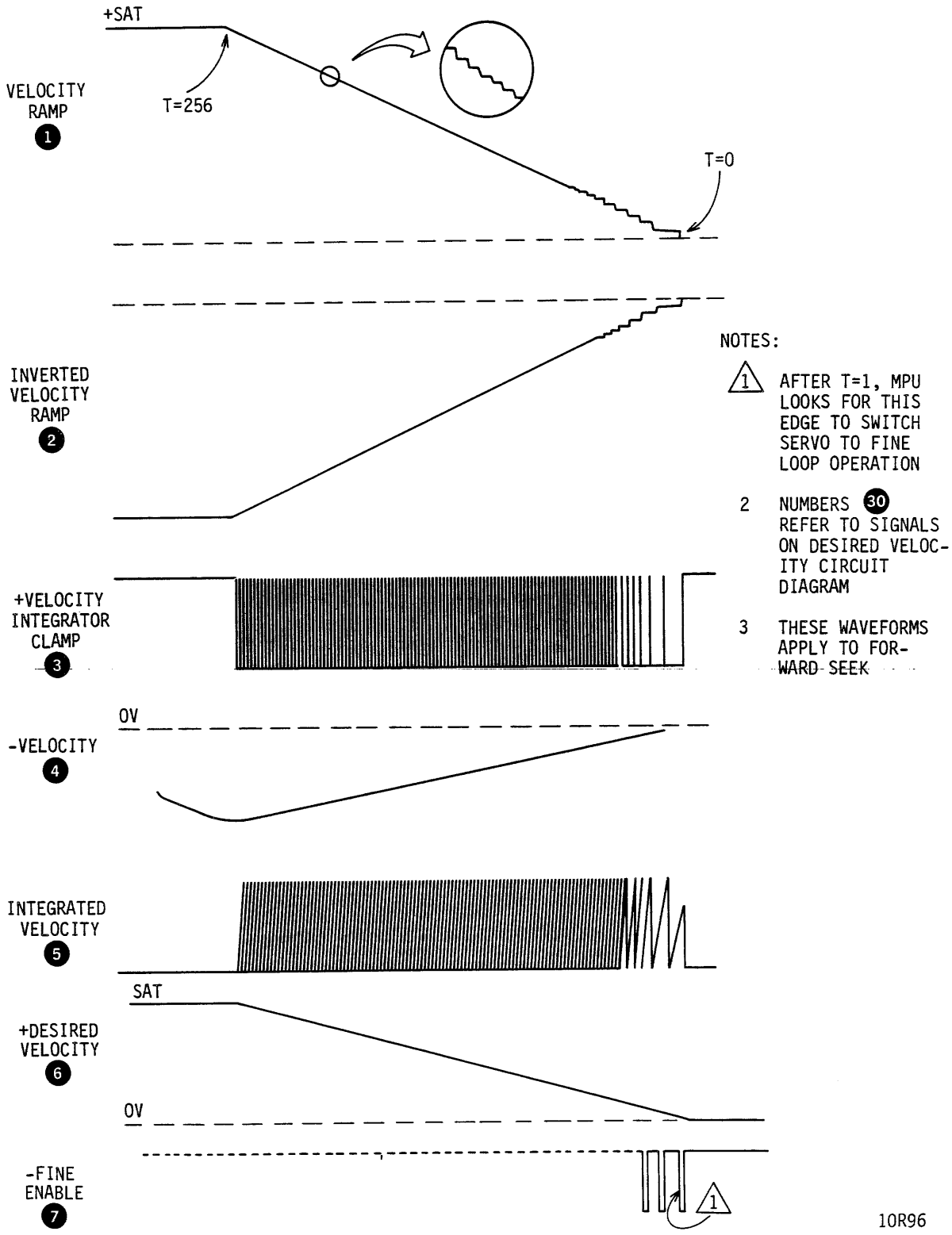


Figure 1-33. Desired Velocity Waveforms

of the seek (when T≤16). These bits are set or cleared according to the ROM velocity table, but they are masked out of the D/A Converter input when T≤16. In the final tracks of the seek, when the velocity signal being integrated is reduced, the portion of the sawtooth applied to the +Desired Velocity signal is increased accordingly.

The sawtooth from the Velocity Integrator serves an additional purpose in the final track of coarse mode. Integrating velocity gives an indication of displacement. Each time the sawtooth reaches a specified value corresponding to a 1/2 track displacement from the last cylinder crossing, a level detector which monitors the sawtooth issues the -Fine Enable signal. With T<1, the MPU looks for this signal and reacts by switching servo operation from the coarse mode to the settle-in mode.

Cylinder Pulse Detection

A Cylinder Pulse is generated each time the heads cross a servo track during the coarse seek operation. Cylinder pulses serve two purposes. First, they decrement Counter #2 in the PTM, keeping its difference count equal to the number of tracks to go in the seek; this points the MPU to the correct tabulated velocity value which is stored in ROM. Second, for T<256 the +Velocity Integrator Clamp line goes active during cylinder pulses to clamp the sawtooth output of the Velocity Integrator to zero. Thus, the sawtooth waveform returns to zero each time that the D/A Converter gets a revised input (see Desired Velocity Generation discussion).

During a seek, the Position signal from the Tribit Decoder alternates between positive and negative values (see Servo Surface Decoding discussion). Each zero-crossing of the Position signal corresponds to a cylinder crossing. Figure 1-34 provides a simplified block diagram and waveforms for this circuit. To ensure that only one Cylinder Pulse is generated as the Position signal crosses zero, two sets of level detectors monitor its amplitude. One set of level detectors activates the -Position Peak line during each peak of the Position signal. With the -Position Peak line active, a one-shot in Address Decode Gate Array is conditioned to accept a trigger from the second set of level detectors. As the +Position signal crosses zero volts, these level detectors activate the +Cyl Crossing Low line, and trigger the one-shot to produce a 4 microsecond Cylinder pulse.

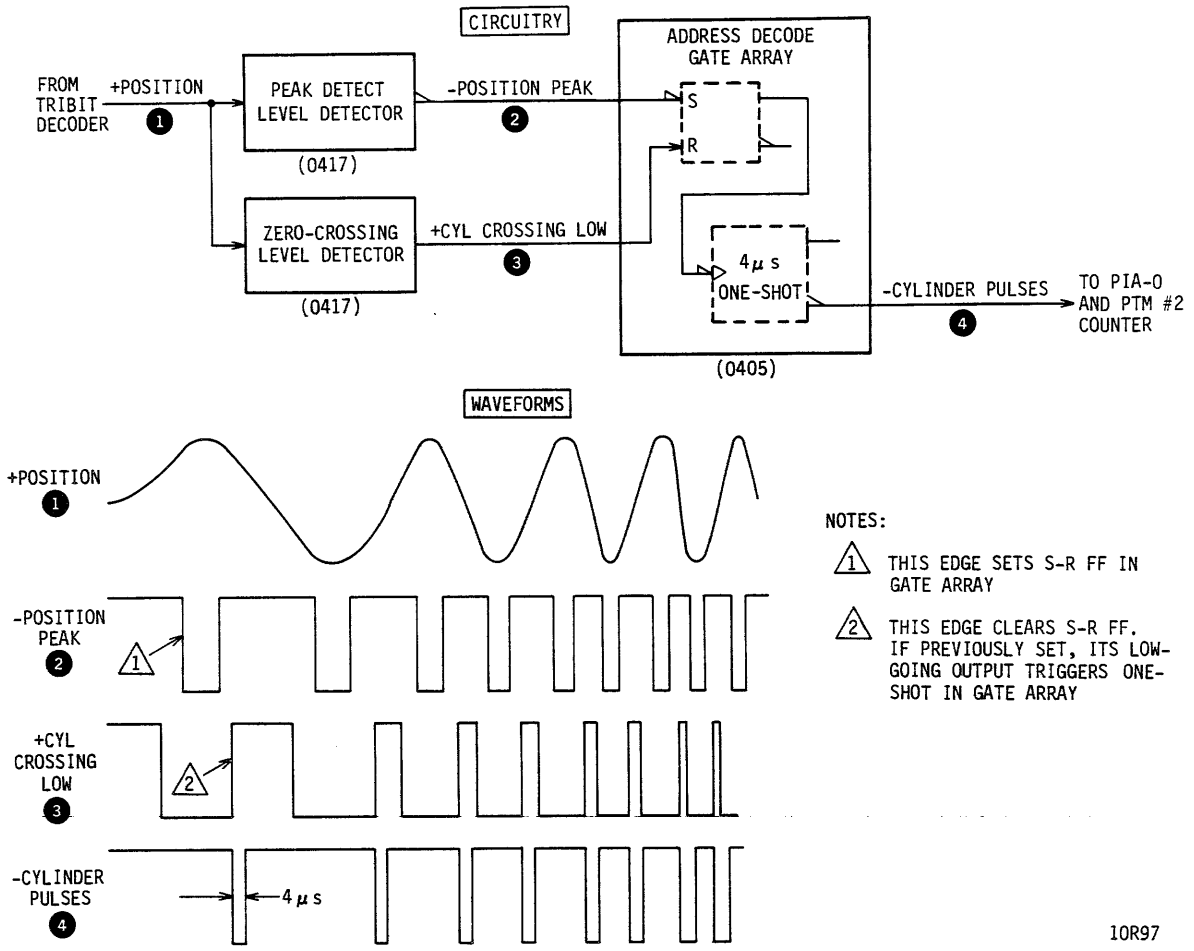


Figure 1-34. Cylinder Pulse Circuitry and Waveforms

Velocity Measurement

A continuous indication of actuator velocity is needed during the coarse seek mode. The -Velocity signal is developed and introduced to the coarse loop so that the servo loop can force actual velocity to match desired velocity. The -Velocity signal is negative during a forward movement (positive during a reverse movement), and its amplitude is proportional to velocity.

Figure 1-35 is a simplified block diagram of the velocity measurement circuits. Velocity measurement is a sequenced operation in which the switching control circuit selects different signal inputs for the Velocity Signal Generator and determines the operating mode of the Velocity Signal Generator.

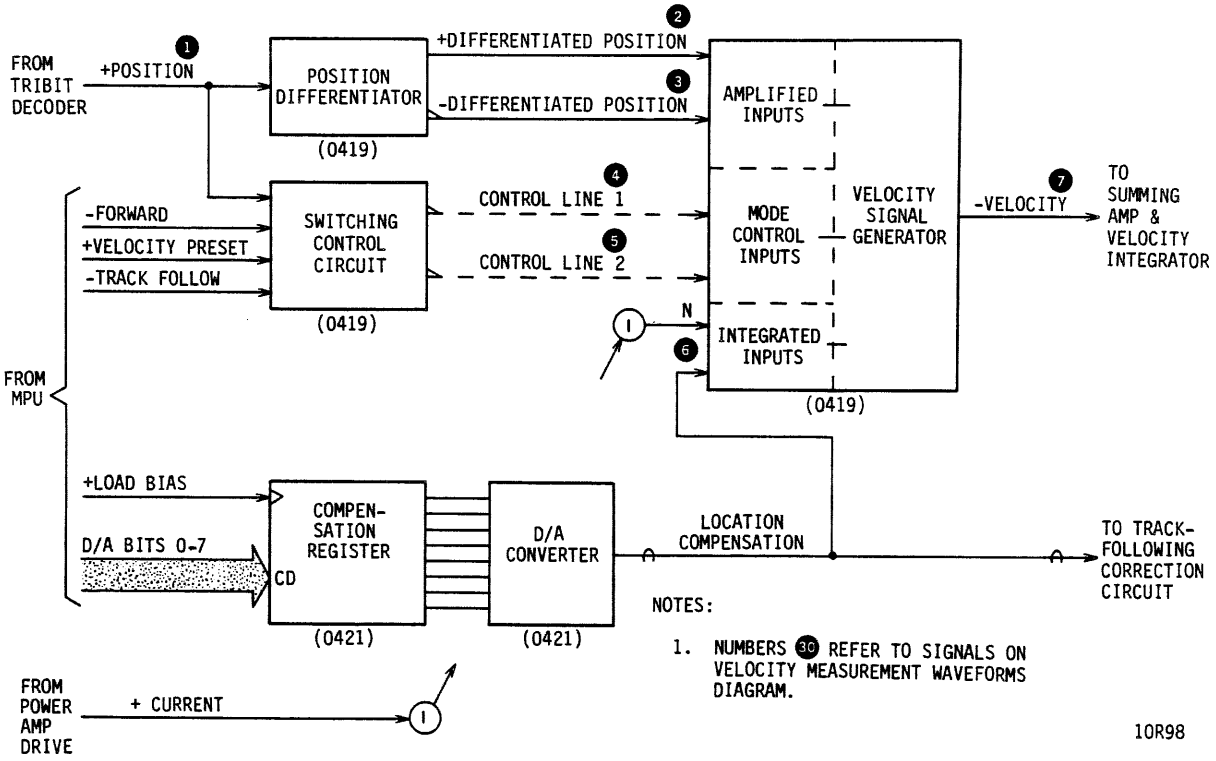


Figure 1-35. Velocity Measurement Circuits

The sequencing pattern repeats itself with every complete oscillation of the +Position signal. Each oscillation of the +Position signal has four distinct regions, as shown in figure 1-36. The positive peak region is followed by a linear region with falling slope. Then there is a negative peak region followed by a linear region with rising slope. The switching control circuit monitors the +Position signal with two level detectors, one that senses the positive peak region and another that senses the negative peak region.

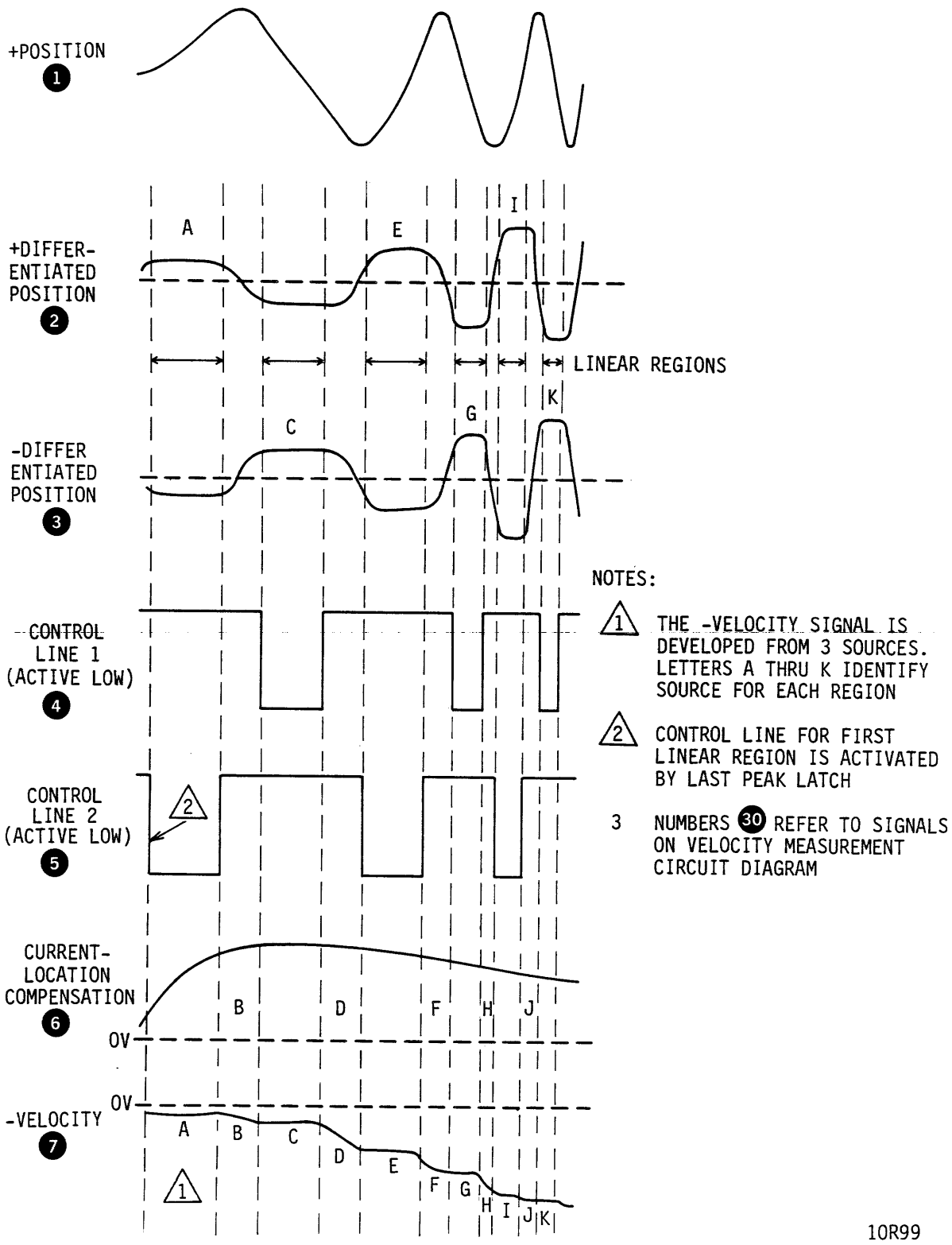


Figure 1-36. Velocity Measurement Waveforms

In each sequence pattern, the switching control circuit activates one control line during one linear region and the other control line during the other linear region. During the linear regions, the differentiated position outputs are proportional to velocity because velocity is the time rate of position change. So during linear regions, the switching control circuit places the Velocity Signal Generator in the amplifying mode and selects the differentiated input of the proper polarity in each region. In the first linear region of the coarse seek (the first 1/2 track), the MPU selects one of the control lines by setting or clearing the +Velocity Preset line at PIA-0 and by clocking the +Velocity Preset level into the Last Peak Latch when the -Track Follow line goes positive. Through the rest of the seek, the circuit is self-running. The detected position signal peaks alternately set and clear the latch, and the latch alternately activates the two control lines in successive linear regions. The proper input polarity to the Velocity Signal Generator is a function of the latch state and the level of the -Forward line; this makes the -Velocity signal polarity match the seek direction.

When the +Position signal is in the peak regions and thus neither control line is active, the switching control circuit allows the Velocity Signal Generator to integrate its Current and Location Compensation inputs. This fills in the gaps in the -Velocity Signal at times when no differentiated position signal is available.

The Current signal is derived in the Power Amp Drive by amplifying Current Feedback sampled at the actuator. Any acceleration or deceleration of the actuator produced by the servo loop is proportional to this current. Velocity is the integral of acceleration; therefore, when the Velocity Signal Generator integrates the Current signal, it is deriving a velocity signal during Position signal peaks.

As the actuator approaches its destination track and the current-induced force approaches zero, other forces on the actuator become significant. The actuator, rotating in a vertical plane, is subjected to varying gravitational force. This force and other minor forces are compensated by the MPU during coarse seeks. At the beginning of coarse mode, the MPU places the eight higher-order cylinder address bits (for the destination cylinder) on D/A Bits 0-7 and loads these values into an octal register. The register contents, which remain fixed during the seek, are developed into the Location Compensation voltage by a D/A Converter. By integrating both the Current and Location Compensation during the peak regions of the +Position signal, the Velocity Signal Generator includes the effects of all forces acting on the actuator and generates a smooth velocity signal throughout the seek.

Summing Amp

The servo system operates, in each mode, to null the input to the summing amp. The MPU selects the signal input to the summing amp via PIA-1 by enabling one of three analog gates. In coarse loop operation, the -Coarse line is active, and velocity information is input to the Summing Amp. In fine loop operation, one analog gate is enabled for settle in mode, and another is enabled for track-following mode (see discussion of Fine Loop Operation).

The Summing Amp input in coarse loop operation is the sum of the +Desired Velocity and -Velocity signals. When measured velocity is equal to desired velocity, these signal inputs add to zero, and -Desired Current, the output of the Summing Amp, is zero. With unmatched inputs, the -Desired Current line has a voltage level that indicates both the magnitude and the polarity of actuator current that will bring the servo system into balance. Zener diodes in the feedback path of the Summing Amp prevent amplifier saturation by keeping the output amplitude between -10 volts and +10 volts. When -Desired Current is negative, the resulting actuator current will accelerate the heads in a forward seek or decelerate the heads in a reverse seek.

Power Amp Drive

The Power Amp Drive generates In Drive or Out Drive currents as inputs to the Power Amp in response to the voltage level on the -Desired Current line from the Summing Amp. Together, the Power Amp Drive and the Power Amp make up a current feedback amplifier. Through a feedback loop that monitors actuator current, the Power Amp Drive adjusts the current in the In Drive line or the Out Drive line as necessary to produce the actuator current specified by the -Desired Current signal. Figure 1-37 shows the Power Amp Drive in simplified form, and the following paragraphs provide a detailed description of its circuit operation.

The -Desired Current line enters the Power Amp Drive through an analog gate which is enabled when the +Disable Drive line is low. A loss of motor speed makes the +Disable Drive line high, turning off the analog gate to remove the input to the Power Amp Drive. This disables the servo as long as motor speed is low. With the analog gate enabled, -Desired Current is inverted and fed into one input of a differential amplifier.

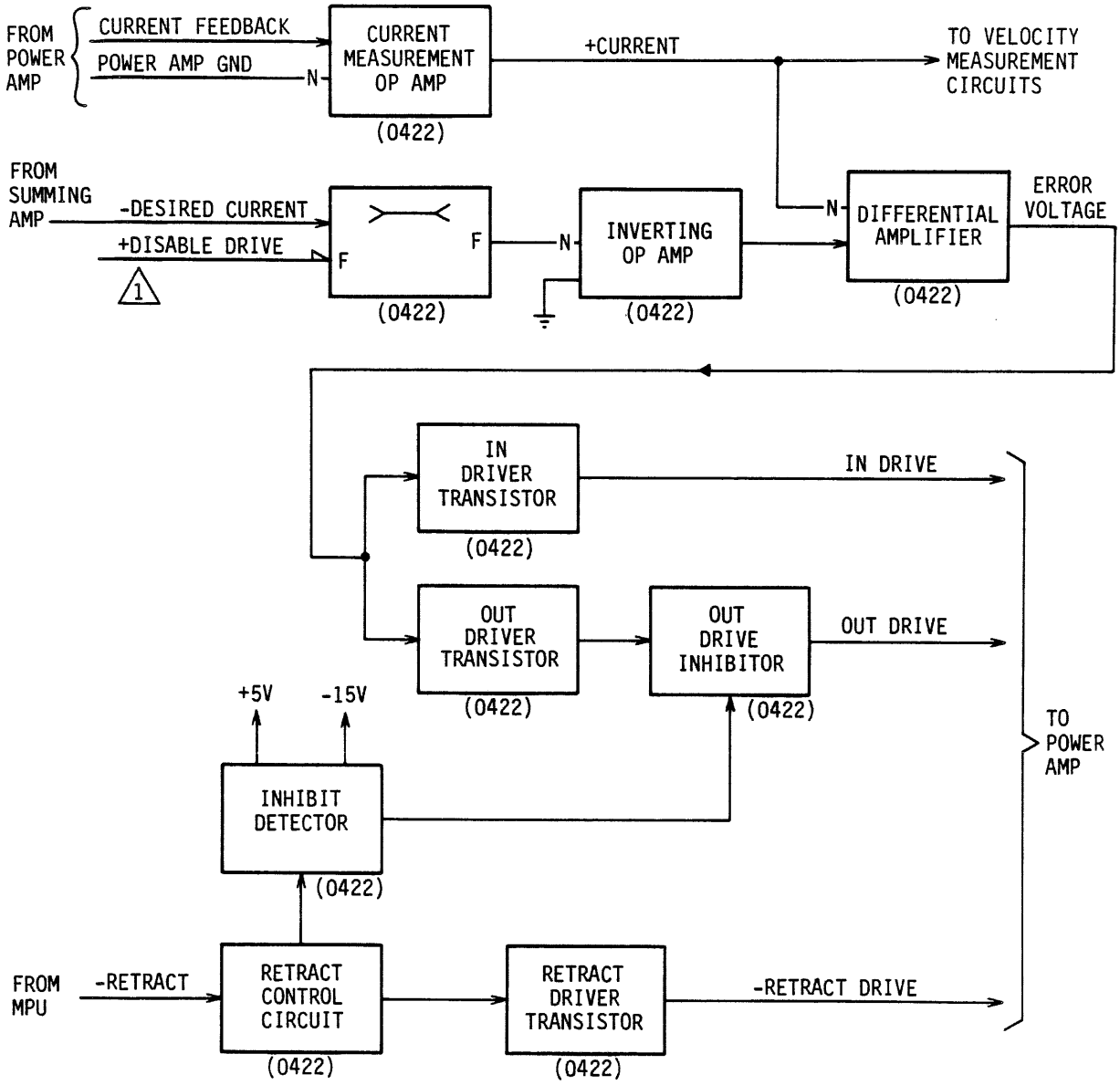


Figure 1-37. Power Amp Drive Circuitry

The +Current signal is the other input to the differential amplifier, and it is obtained by amplifying the current feedback in the Current Measurement op amp. In addition to acting as a reference input to the differential amplifier, the +Current line goes to velocity measurement circuitry.

The differential amplifier amplifies the difference between measured current and desired current to develop an error voltage that biases the In Driver and Out Driver transistors. When the error voltage is positive, it cuts off the Out Driver transistor and regulates the current in the In Drive output line. When the error voltage is negative, it cuts off the In driver transistor and regulates the current in the Out Drive output line. When the error voltage changes sign, it reverses the direction of actuator current, thereby reversing the force applied to the actuator.

Out Drive current passes through a switching transistor in the Out Drive Inhibitor Circuit. During retract operations or loss of +5 V or -15 V supply voltage, this transistor is cut off by a bias voltage from the Inhibit Detector. In these situations, Out Drive current would interfere with the head retract by moving the heads away from the landing zone. Retract operations are discussed in more detail under Retract Control Circuitry.

Power Amp

The Power Amp, acting on inputs from the Power Amp Drive, produces the actuator current required by the servo loop. Figure 1-38 is a simplified drawing of the Power Amp circuitry.

When positive actuator current is required, the Power Amp Drive generates current in the In Drive line. The In Direction Amplifier amplifies this input current and regulates current flow from ground through the sampling resistor and the actuator coil to +24 V. The positive voltage on the Current Feedback line is supplied to the Power Amp Drive to complete the loop regulating the amplifier (see discussion of Power Amp Drive). Positive actuator current forces the actuator to accelerate during a forward move and to decelerate during a reverse move.

When negative actuator current is required, the Power Amp Drive generates current in the Out Drive line. The Out Direction Amplifier amplifies this input current and regulates current flow from -24 V through the actuator coil and the sampling resistor to ground. In this case, the voltage on the Current Feedback line is negative. Negative actuator current forces the actuator to accelerate during a reverse move and to decelerate during a forward move.

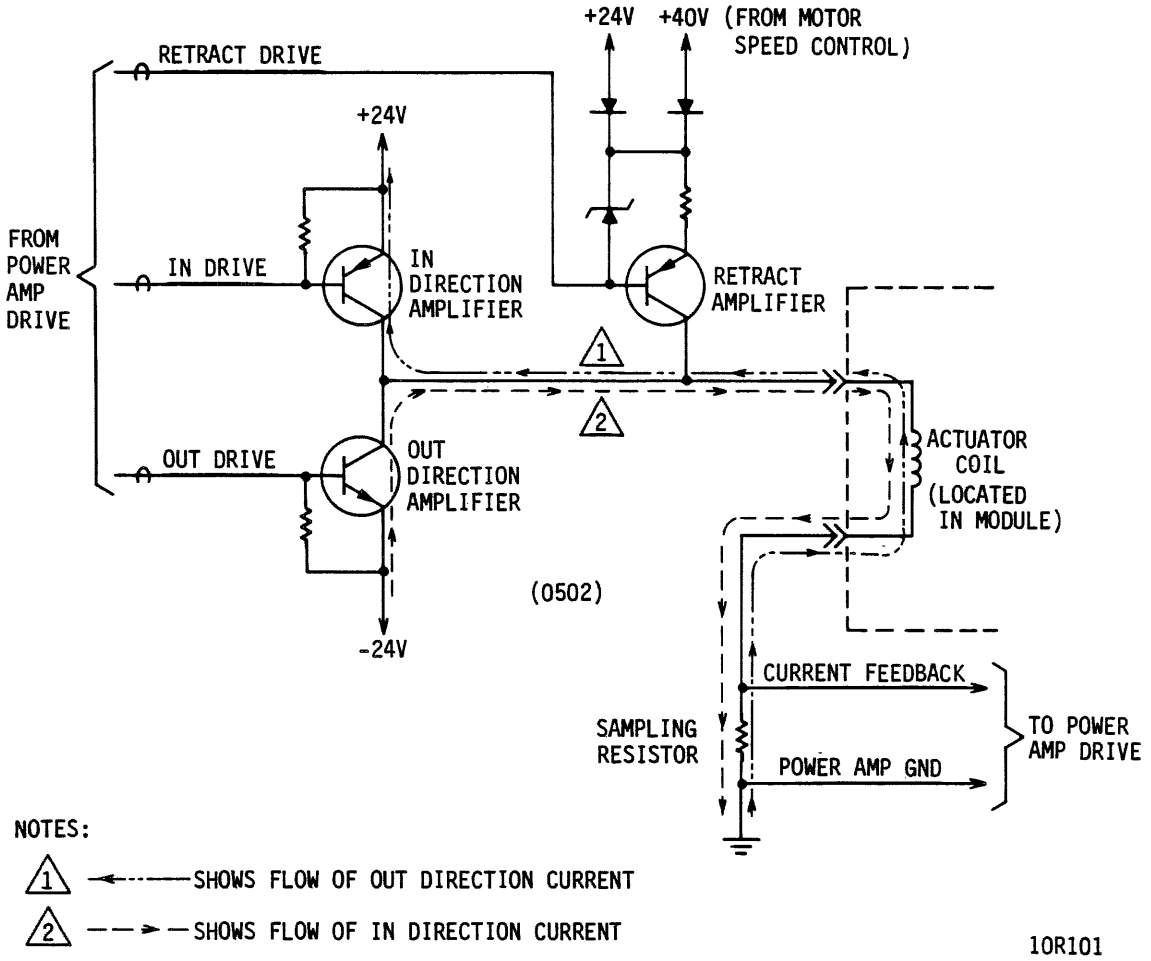


Figure 1-38. Power Amp Circuitry

During retract operations, the Retract Amplifier generates positive current in the actuator to move the heads forward to the landing zone. This operation is discussed under Retract Control Circuitry.

Fine Loop Operation

General

The servo system shifts from the coarse loop to the fine loop when there is 1/2 track remaining in the seek. Fine loop operation continues until the beginning of the following seek. Figure 1-39 is a simplified block diagram of the fine loop circuitry. Discussion of the fine loop is presented in the following topics:

- Position Error Generation
- Fine Loop Actuator Movement

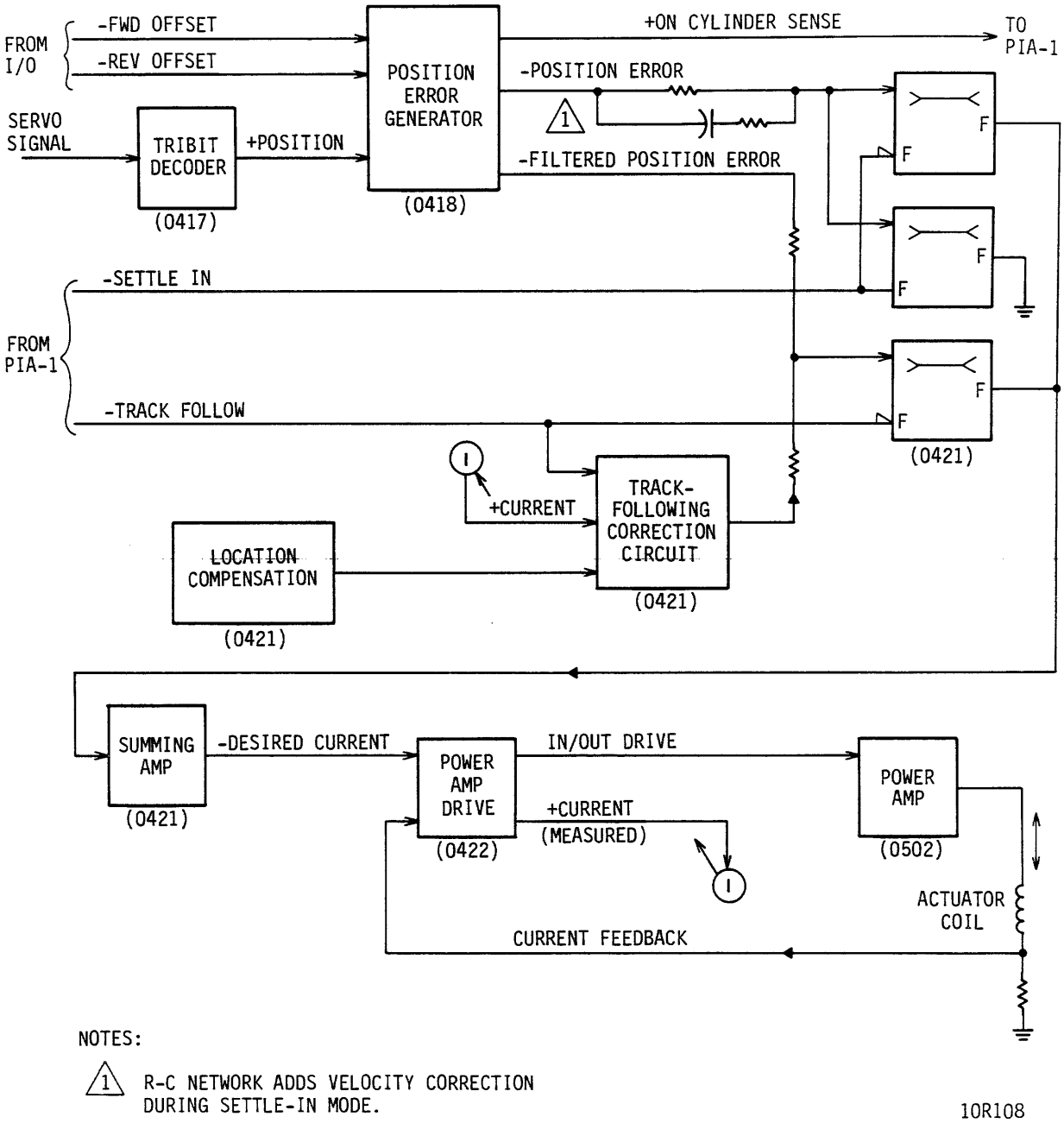


Figure 1-39. Fine Loop Block Diagram

Position Error Generation

In fine loop operation, the servo system adjusts the position of the actuator to null the input signal to the Summing Amp. The Summing Amp input developed for fine loop operation is different for settle in and for track-following modes. However, both of these error signals basically derive from the +Position signal from the Tribit Decoder.

At the start of a seek, the MPU sets or clears the +Slope input to the Tribit Decoder to ensure that +Position goes positive as the heads move inward and negative as the heads move outward from their destination track. The +Position signal is zero with the heads exactly on track. This relationship is true for every destination track on the disk. Thus, with some modification, +Position is a suitable error signal for the Summing Amp in the fine loop. The modification takes into account the following considerations:

- Stability of fine servo loop -- requires the addition of a velocity correction to the error signal.
- Servo offsets -- allow the controller to reposition the heads to either side of track center to recover read errors.
- Increased gain in track-following mode -- gives the servo more responsive control when keeping the heads on track.

Figure 1-40 shows the position error circuitry in simplified form. The -Position signal enters a calibration network from the Tribit Decoder. During a first seek, the MPU activates the optimum combination of Gain Control lines to select the position signal amplitude to compensate for variations in the servo disk. PIA-0 holds these Gain Control lines at the selected levels until a new first seek occurs.

An op amp inverts -Position and applies it with an optional offset to a second inverting op amp. An offset, a dc shift of the position signal, results when the controller issues a Servo Offset command in order to recover marginal read data. When the I/O Gate Array decodes Servo Offset Plus (Tag 3 and Bus bit 2), it activates -FWD Offset, and the Offset Bias circuit shifts the position signal about 0.75 V negative. When the I/O Gate Array decodes Servo Offset Minus (Tag 3 and Bus bit 3), it activates -REV Offset, and the Offset Bias circuit shifts the position signal about 0.75 V positive. Servo Offset Plus displaces the heads inward from track center.

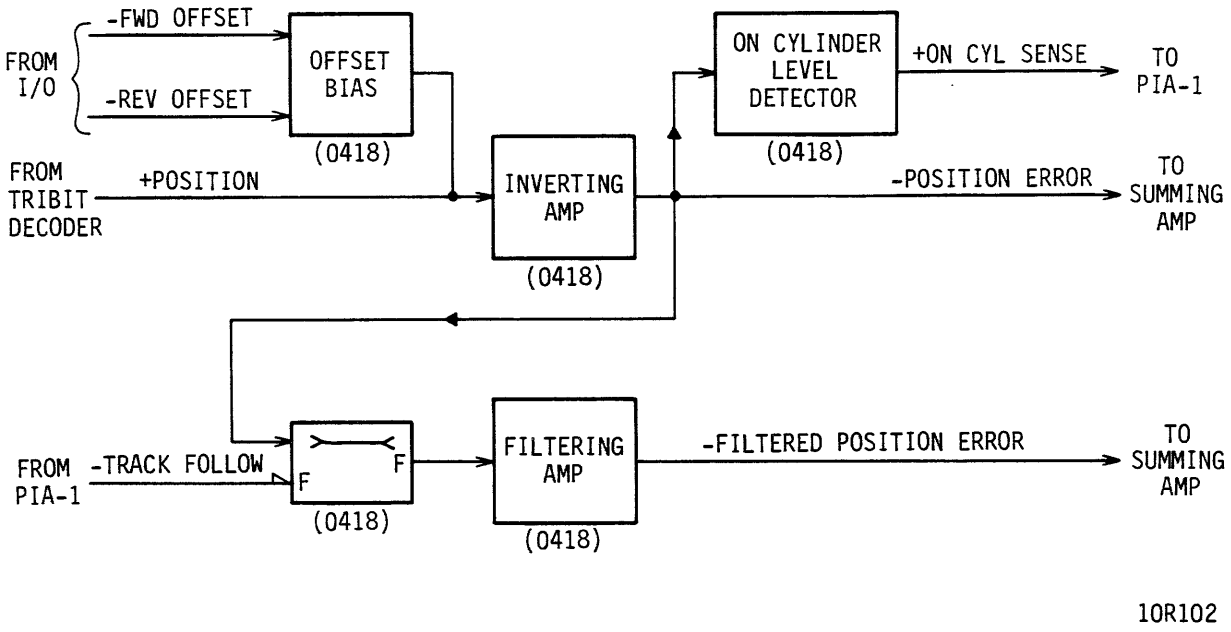


Figure 1-40. Position Error Circuitry

The -Position signal from the second op amp develops error signals for the settle in and track-following modes, and it inputs the On Cylinder level detector. For settle in mode, the -Position signal passes through a resistor which is in parallel with a series-RC differentiator. The differentiator adds velocity dependence to the position information to improve fine loop stability in settle-in mode. Prior to settle-in (T>1/2 track), an analog gate prevents an erroneous charge build-up on the capacitor in the differentiator. This permits a smooth transition from the Coarse to the Settle In mode. When -Settle In goes active, it disables that analog gate, allowing the velocity correction to operate. A second analog gate passes the error voltage on to the Summing Amp input.

When the position signal drops to 0.75 V, the On Cylinder level detector activates +On Cylinder Sense signal to generate an interrupt via PIA-1. The MPU responds to this interrupt by inactivating the -Settle In line, activating the -Track Follow line, and issuing On Cylinder status to the I/O Gate Array. The servo enters track-following mode to maintain the heads on track until a new seek command appears.

The track-following mode uses an error signal developed by adding the -Filtered Position Error signal with a track-following correction voltage. In track-following, the fine loop uses a high amplitude position signal for tight servo control with filtering to provide greater stability in the loop. The track-following correction circuit supplies velocity-dependent feedback for stable loop operation. Prior to track-following, the MPU loads this circuit with a location compensation voltage (see Velocity Measurement topic under Coarse Loop Operation). During track-following, this circuit maintains a correction voltage by integrating the +Current signal.

Thus, the Summing Amp receives a different input in each seek mode. Response of the servo circuitry to the Summing Amp input is summarized in the next topic.

Fine Loop Actuator Movement

In the fine loop, as in the coarse loop, the Summing Amp develops the -Desired Current signal in response to its input error signal. The Power Amp Drive and Power Amp, acting as a current feedback amplifier, develop current in the actuator to match the -Desired Current input signal. This actuator current moves the heads toward track center. As the heads move toward track center, the position error signal goes to zero. The loop is balanced when the heads are at track center and the Summing Amp input is nulled. With a positive Summing Amp input, -Desired Current is negative; this results in positive actuator current and inward force on the heads.

For details about this circuit operation, refer to the following topics presented under Coarse Loop Operation:

- Summing Amp
- Power Amp Drive
- Power Amp

Retract Control Circuitry

The retract control circuitry is used for two functions. During the normal head unloading process, the circuitry applies a force to the actuator that holds the heads in the landing zone until the actuator locking solenoid locks them in that position and the drive motor stops. During emergency retract operations, the circuitry moves the heads into the landing zone where they are automatically latched. Both circuit functions are discussed in the following paragraphs.

To apply an inward holding force to the actuator, the MPU issues the Retract command (see figure 1-41). The retract control circuit reacts by forward-biasing the retract driver transistor. When this transistor conducts, current in the Retract Drive line switches on the Retract Amplifier on the Power Amp board. The Retract Amplifier is a source of (positive) in direction current that is independent of the servo electronics, and this in direction current forces the heads to remain over the landing zone. With the heads locked in this position and the drive motor stopped, the MPU drops the Retract command.

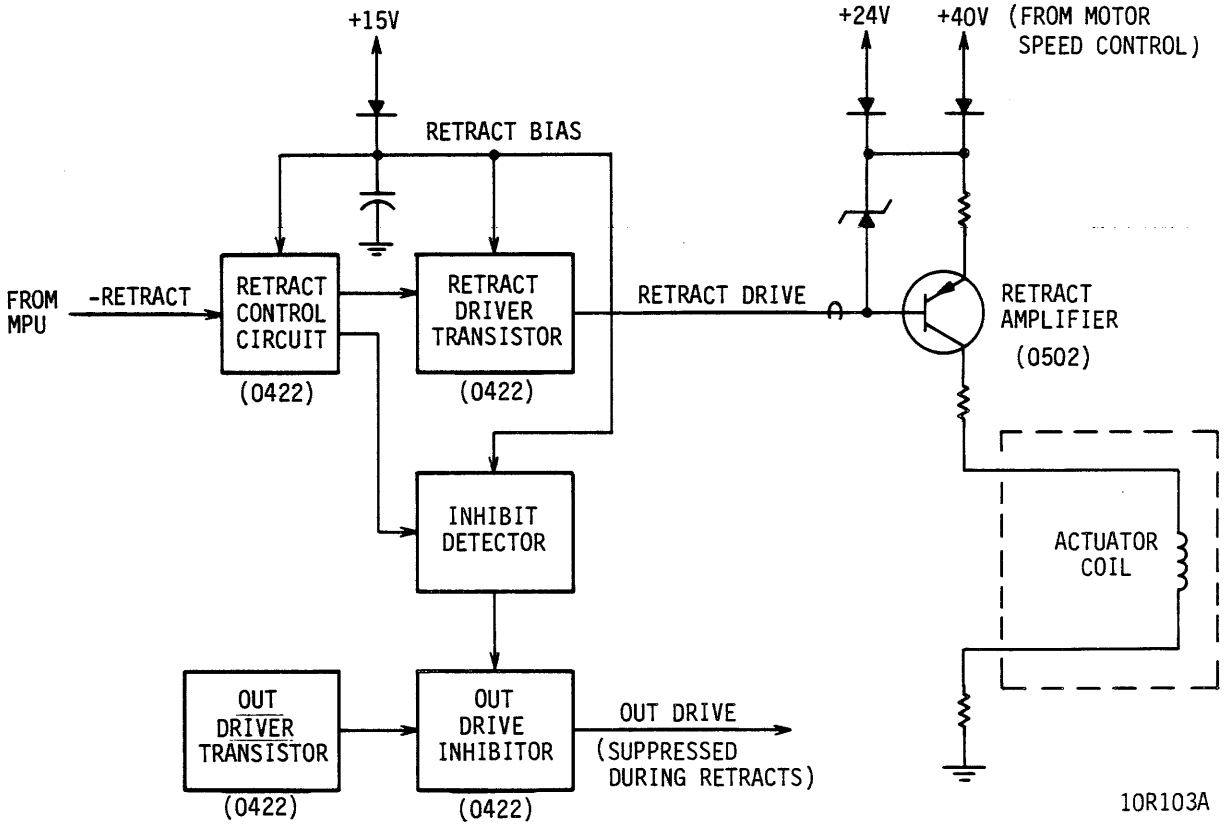


Figure 1-41. Retract Circuitry Block Diagram

The emergency retract function moves the heads to the landing zone to prevent them from landing in the data zone during a loss of +5 Vdc or of motor speed. With a loss of speed, the MPU issues the Retract command, switching the -Retract line low. With a loss of +5 Vdc (making the MPU inoperative), the -Retract line goes low automatically. When the -Retract line is low, the Retract Amplifier is switched on to produce in direction current, as described in the previous paragraph. During retract operations, the Out Drive Inhibitor transistor is cut off to ensure that the Power Amplifier produces no out direction current.

The emergency retract circuitry must operate at times when power loss occurs. For this reason, the transistors that develop Retract Drive are supplied with operating voltage (+15 Vdc) by slowly discharging capacitors. In addition, the Retract Amplifier on the Power Amp board has two voltage sources -- +24 Vdc from the power supply and the voltage generated by the decelerating drive motor. The power amplifier develops actuator current from the source with the highest potential.

TYPES OF SEEKS

General

The drive has four basic types of seeks: the load operation, normal seek, return to zero (RTZ) seek, and unload operation. The load and RTZ operations use both the outward and inward movements to move the actuator to track 0. The unload operation is an inward movement that moves the heads to the landing zone in the inner guard band. Normal seek operations can be either inward or outward movements, depending upon where the new address is located relative to the present address. The four basic seek operations are discussed in the following text.

Load Operation

The load operation is an MPU-controlled sequence that starts the drive motor, moves the heads from the retracted position to track 0, and calibrates the velocity measurement circuitry. A load operation cannot take place until power on initialization is successfully completed. Refer to the Power Functions discussion for details about power on initialization. The load operation is described in the following paragraphs and is flowcharted in figure 1-42.

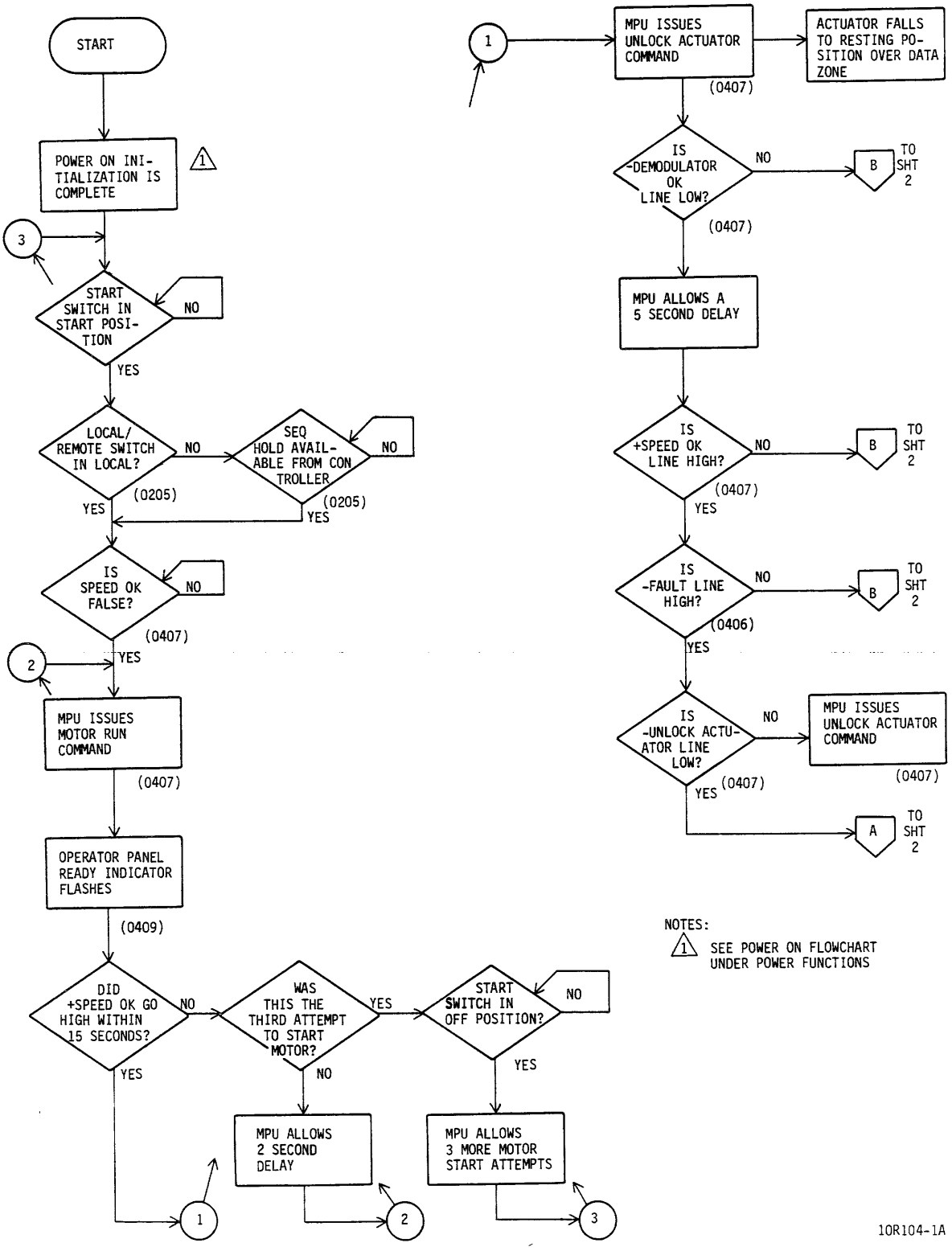


Figure 1-42. Load Operation Flowchart (Sheet 1 of 2)

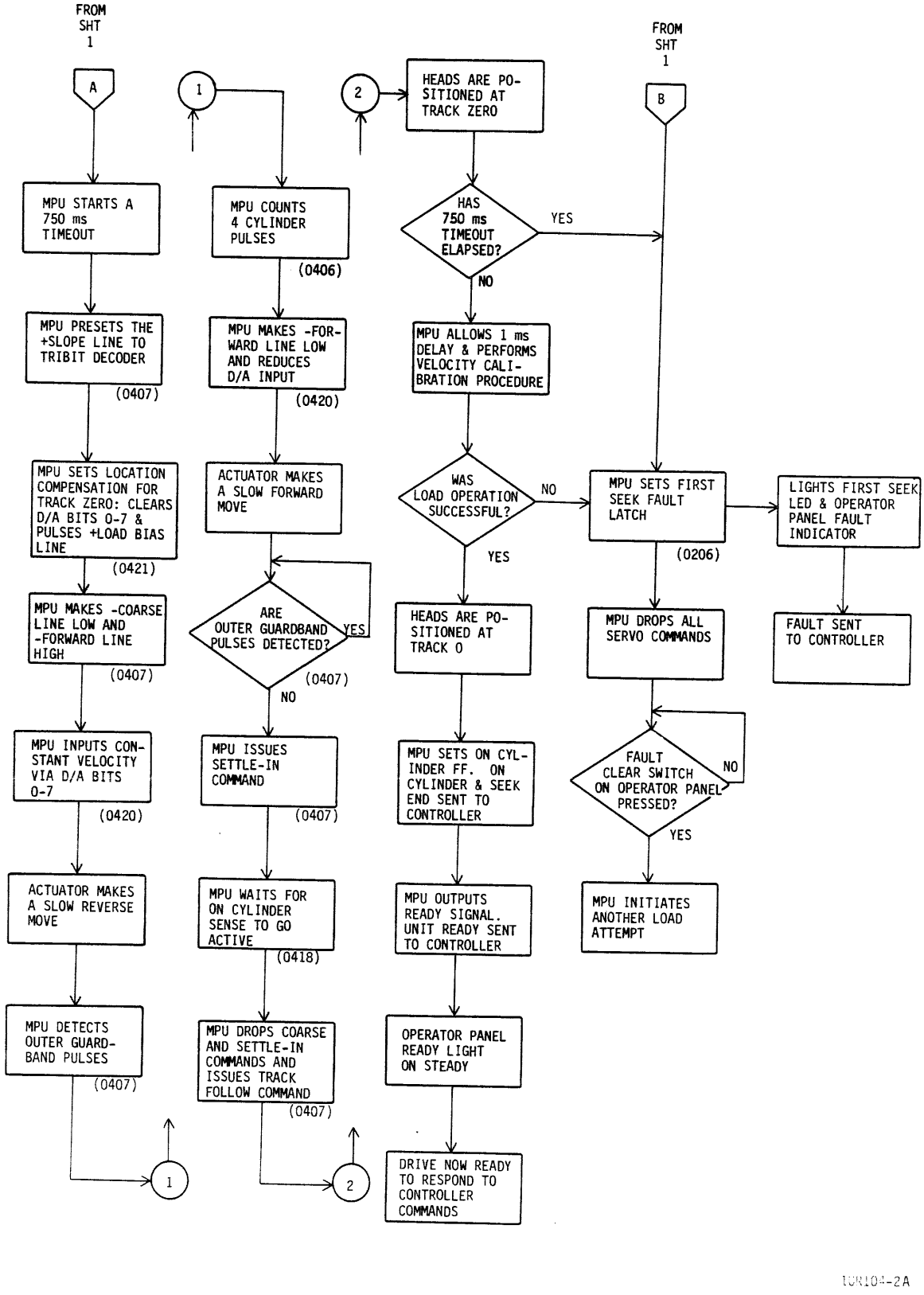


Figure 1-42. Load Operation Flowchart (Sheet 2)

When power on initialization is complete, the MPU waits for start conditions before initiating the load operation. The MPU requires that the START switch is placed in the Start position and (in remote operation) that Sequence Hold is available from the controller. With start conditions present, the MPU checks that Speed OK is false, indicating that it is safe to start the drive motor.

The MPU starts the drive motor by issuing the -Motor Run command to the Motor Speed Control (via PIA-1) and requires that the +Speed OK line from the Motor Speed Control goes high within 15 seconds. Operation of the Motor Speed Control and drive motor is discussed under Electromechanical Functions. With the motor up to speed, the MPU verifies that -Demodulator OK is low, indicating that the tribit decoder is working properly.

To start the heads moving outward from the landing zone, the MPU issues the Unlock Actuator command at PIA-1. With the actuator locking solenoid energized, the heads are free to move outward over the disks in response to gravitational torque on the actuator. Figure 1-43 shows the head trajectory during a load seek. During this free movement, which takes about 3 seconds, the MPU validates the -Demodulator OK signal to ensure that the tribit decoder is working properly.

After unlocking the actuator, the MPU allows a 5 second timeout before initiating a servo-controlled movement toward track 0. At the end of the timeout, the MPU doublechecks Speed OK and ensures that the -Fault line is high. The MPU also doublechecks the -Unlock Actuator line at PIA-1 to ensure that the actuator has been released.

The MPU starts a 750 ms timeout for the completion of the load operation, and it will set the First Seek fault latch and light the front panel FAULT indicator if the load operation is incomplete at the timeout.

The MPU presets the Slope line to ensure that the +Position signal will have the correct phase as the heads settle in at their destination track (track 0). Also, the MPU clears D/A bits 0-7 and loads their values into the location compensation D/A converter by pulsing the +Load Bias line at PIA-0. This prepares the location compensation for operation at track 0.

The MPU commands a slow reverse move to take the heads from their resting position (in the data zone) into the outer guard band. To do this, the MPU switches the -Coarse line low and the -Forward line high. The MPU inputs the D/A converter with a constant desired velocity via D/A bits 0-7 from PIA-2.

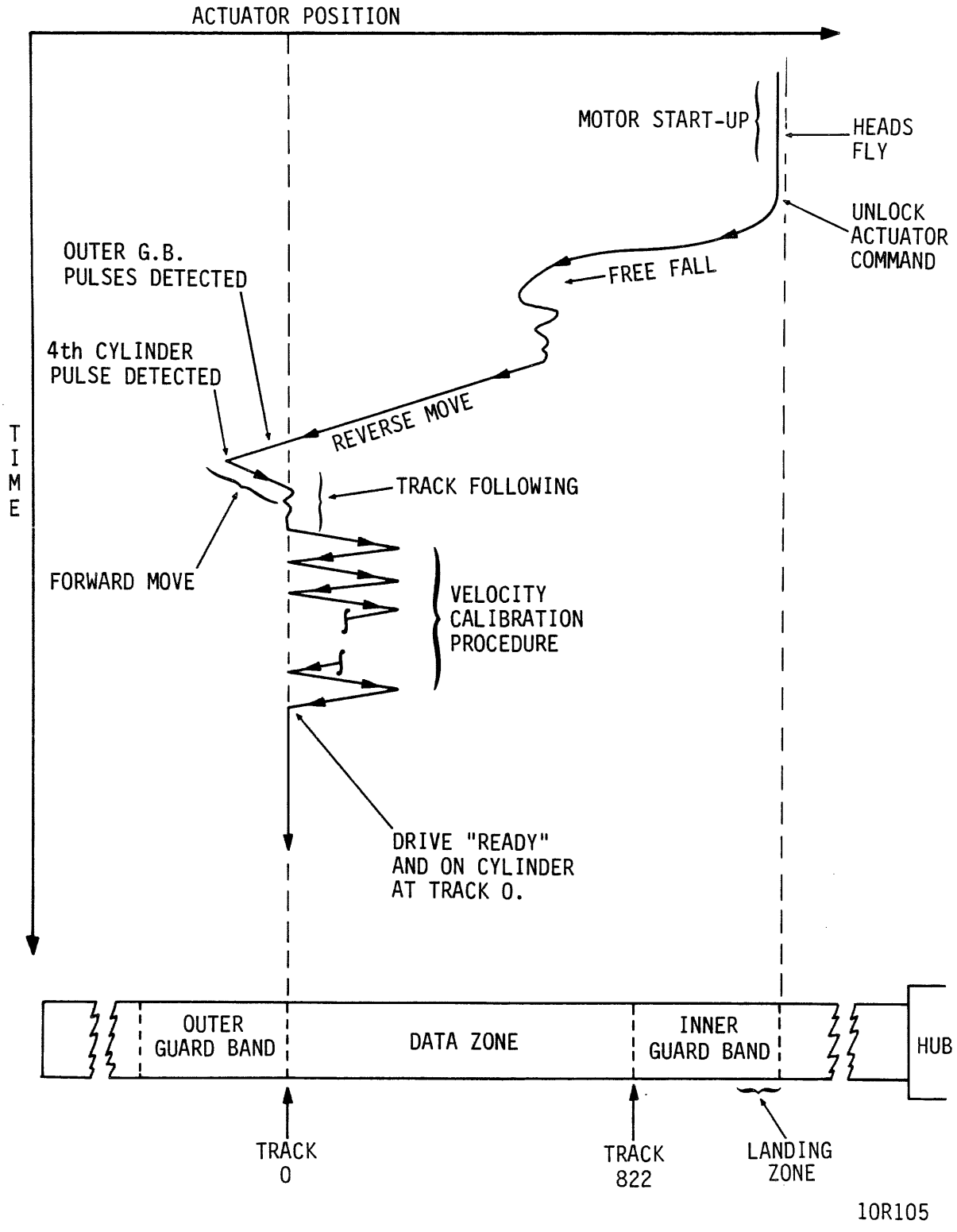


Figure 1-43. Load Seek Trajectory

The reverse move continues until the MPU sees Outer Guard Band Pulses at PIA-1 followed by 4 Cylinder pulses. After the fourth Cylinder pulse, the MPU commands a slower forward move by switching the -Forward line low and inputting reduced values to the D/A converter.

The forward movement uses the Coarse servo input to the Summing Amp initially and, when Outer Guard Band Pulses cease, adds the Settle-In servo input to the Summing Amp. As described under Servo Surface Decoding, the buffer zone consists of 5 tracks located between the outer guard band and track 0 of the data zone. As the servo head moves through the buffer zone, the tribit demodulator develops a constant negative Position signal. Adding the Settle-In input develops a controlled velocity profile from this feature of the Position signal.

The MPU looks for the On Cylinder Sense signal (which goes high when the Position signal reaches 0.75 V) from the servo level detect circuits. With On Cylinder Sense active, the MPU drops the Coarse and Settle-In commands and issues the Track Follow command. After a 1 ms delay, the MPU performs a velocity calibration procedure. In this procedure, the MPU commands a series of 274-track normal seeks where it adjusts the level of the Position signal coming from the tribit decoder. This adjustment compensates for gain variations in the servo disk. The gain is adjustable in steps depending on which combination of the three gain control lines is set. Upon finding the optimum combination of settings, the MPU maintains that combination (output from PIA-0) until the first load operation is repeated.

With the velocity calibration procedure complete, the heads are positioned at track 0. If the load operation was successful, the MPU issues the Ready signal at PIA-0 and sets the On Cylinder FF in the I/O Gate Array. The front panel Ready indicator lights steadily, and On Cylinder, Seek End, and Unit Ready status appear on the interface. The MPU then waits for further instructions from the controller.

If the load operation was unsuccessful, the MPU sets the First Seek fault latch, lights the front panel FAULT indicator, and drops all commands to the servo. With no servo commands, the heads come to rest over the data zone and remain there until the next load attempt. The First Seek fault can be cleared only by operation of the Fault Clear switch. Pressing the Fault Clear switch initiates another load attempt.

Normal Seek

Normal seeks are initiated by controller command and implemented by the drive servo circuitry. The normal seek is the operation used to move the heads from one location to another on the disk surface. The same track can also be selected, but a zero track seek requires no actuator movement and the operation is handled by the I/O Gate Array.

The normal seek occurs in two directions, reverse (from the center towards the outer edge) and forward (from the outer edge towards the center). Going from a higher-numbered track to a lower-numbered one involves an out direction movement of the actuator, while going from a lower-numbered track to a higher-numbered one involves an in movement. Figure 1-44 is a detailed flowchart showing the normal seek operation.

With the drive in the unit ready and on cylinder conditions, the controller initiates a normal seek by placing the desired cylinder address on the Bus bits 0 through 9 and raising the Tag 1 (Cylinder Select) signal. The address is gated into the Cylinder Address register (in the I/O Gate Array) by the Cylinder Select Tag.

Inside the I/O Gate Array several processes take place. If the controller issues a seek command to an address greater than track 822, a decoder inside the gate array recognizes this as an illegal address and sets the Seek Error FF. The On Cylinder line remains set, and no Seek Interrupt is enabled to PIA-0. If a new seek command leaves the Cylinder Address register contents unchanged (a zero-track seek), the On Cylinder line remains set and no Seek Interrupt is enabled to PIA-0. However, the On Cylinder and Seek End lines to the controller go inactive for 30 microseconds. If a new seek command requires a seek to a different (legal) seek address, however, the Cylinder Select tag clears the On Cylinder FF and triggers a one-shot that sends Seek Interrupt to PIA-0. The MPU responds to this interrupt by initiating a seek routine.

The MPU transfers the destination cylinder address from the I/O Gate Array into its RAM via PIA-0 by pulsing the I/O Control 1 and 2 lines. These control lines operate a multiplexer in the gate array to place the address, four bits at a time, on Head/Cylinder Address lines 0-3. After reading the cylinder address, the MPU pulses the control lines to cause the Head Address to be multiplexed onto Head/Cylinder Address lines 0-3.

The seek operation from this point until the on cylinder condition is achieved is under the control of the MPU programming. The program compares the new address with the present address (stored in RAM memory) to calculate the difference between the two (T=tracks to go) and the direction of the move (in or out).

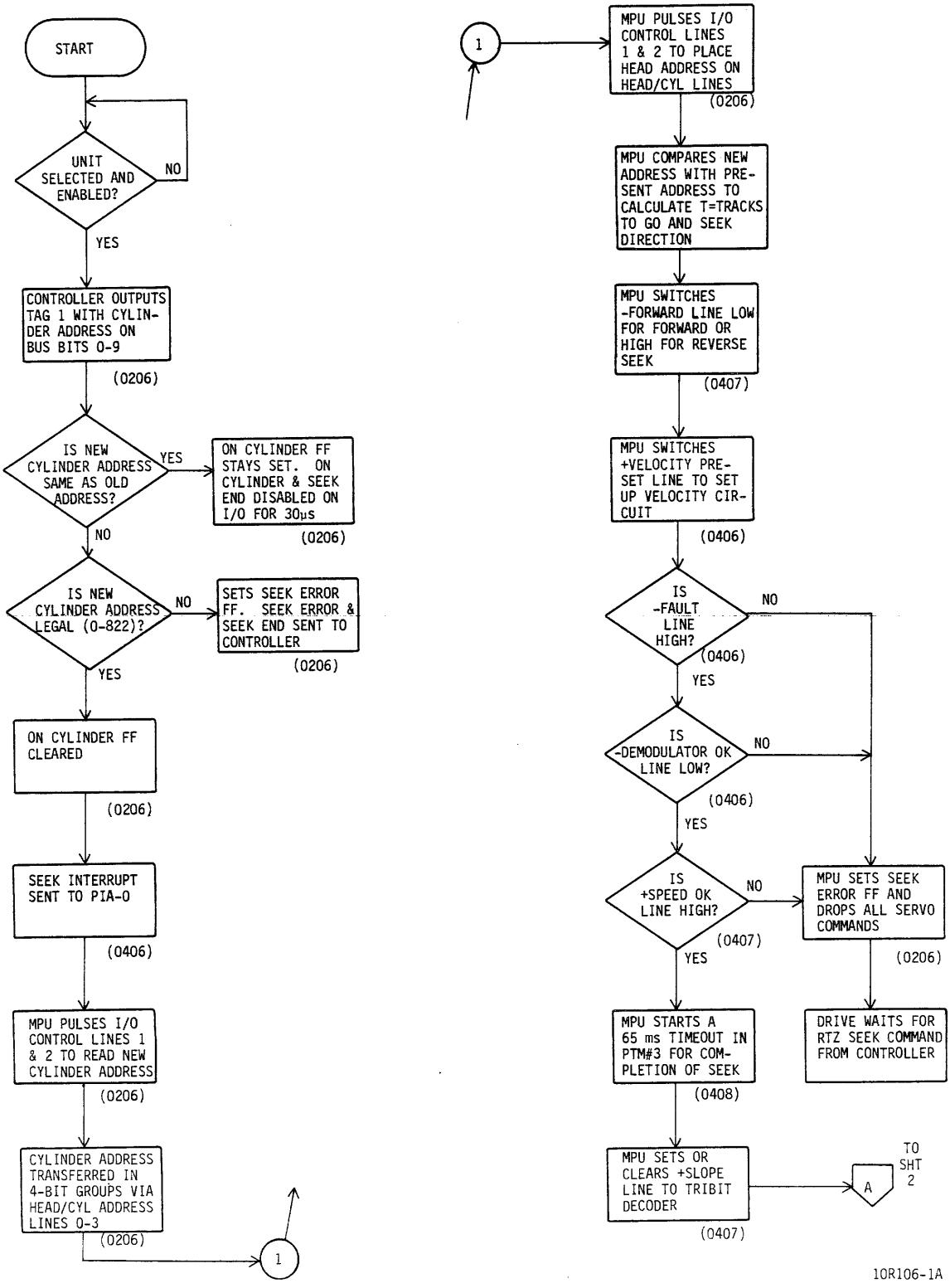


Figure 1-44. Normal Seek Flowchart (Sheet 1 of 4)

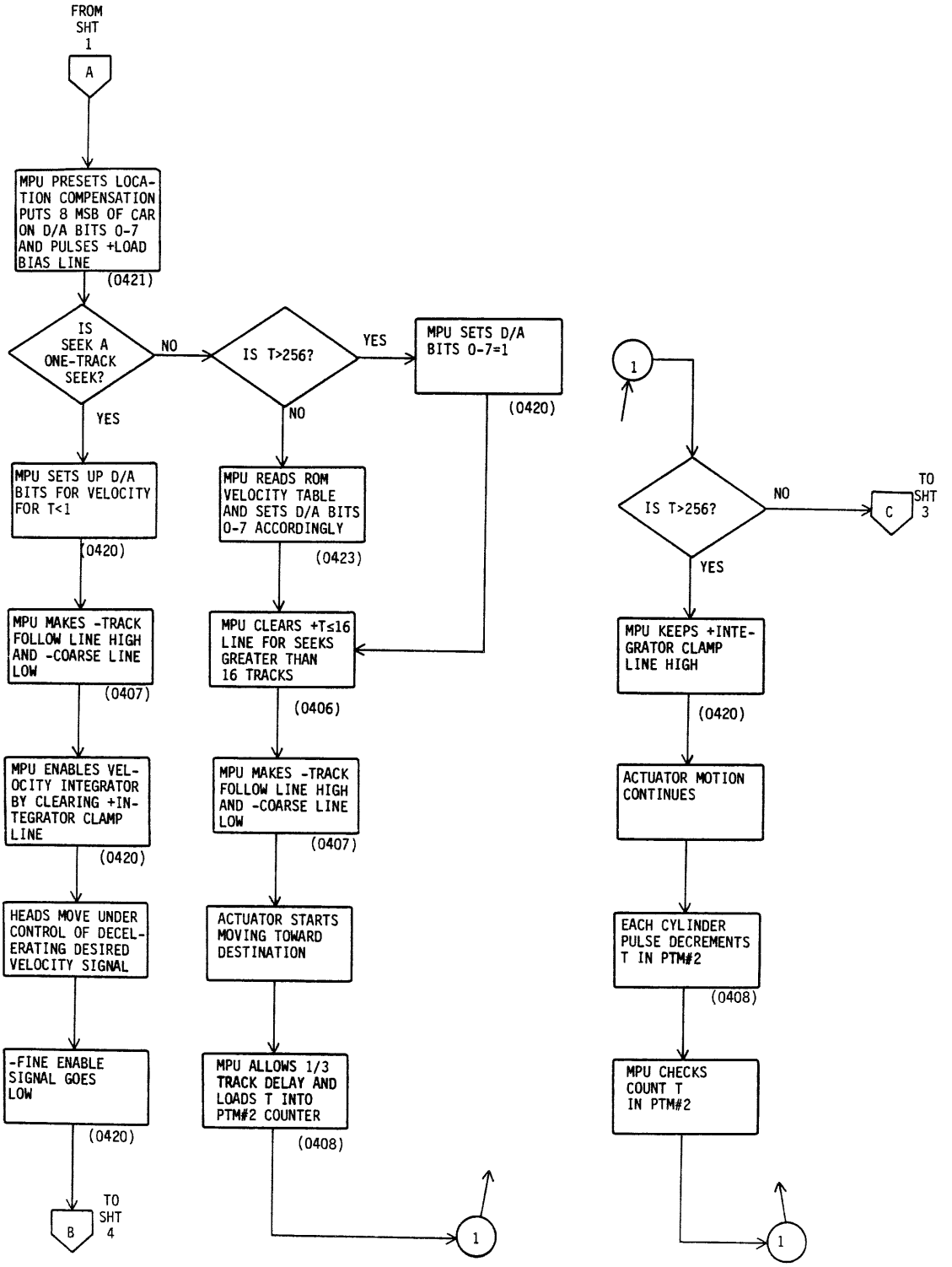


Figure 1-44. Normal Seek Flowchart (Sheet 2)

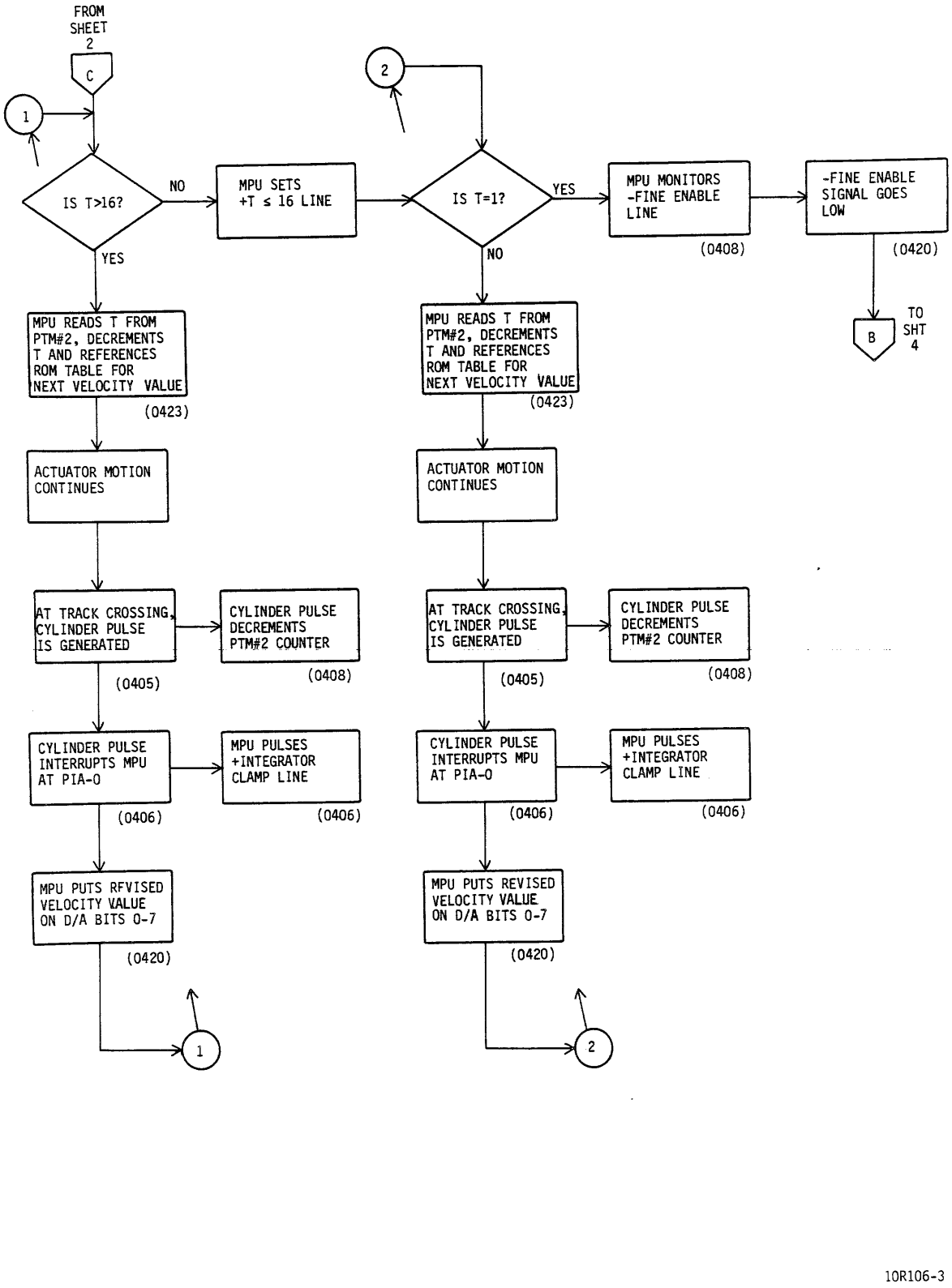


Figure 1-44. Normal Seek Flowchart (Sheet 3)

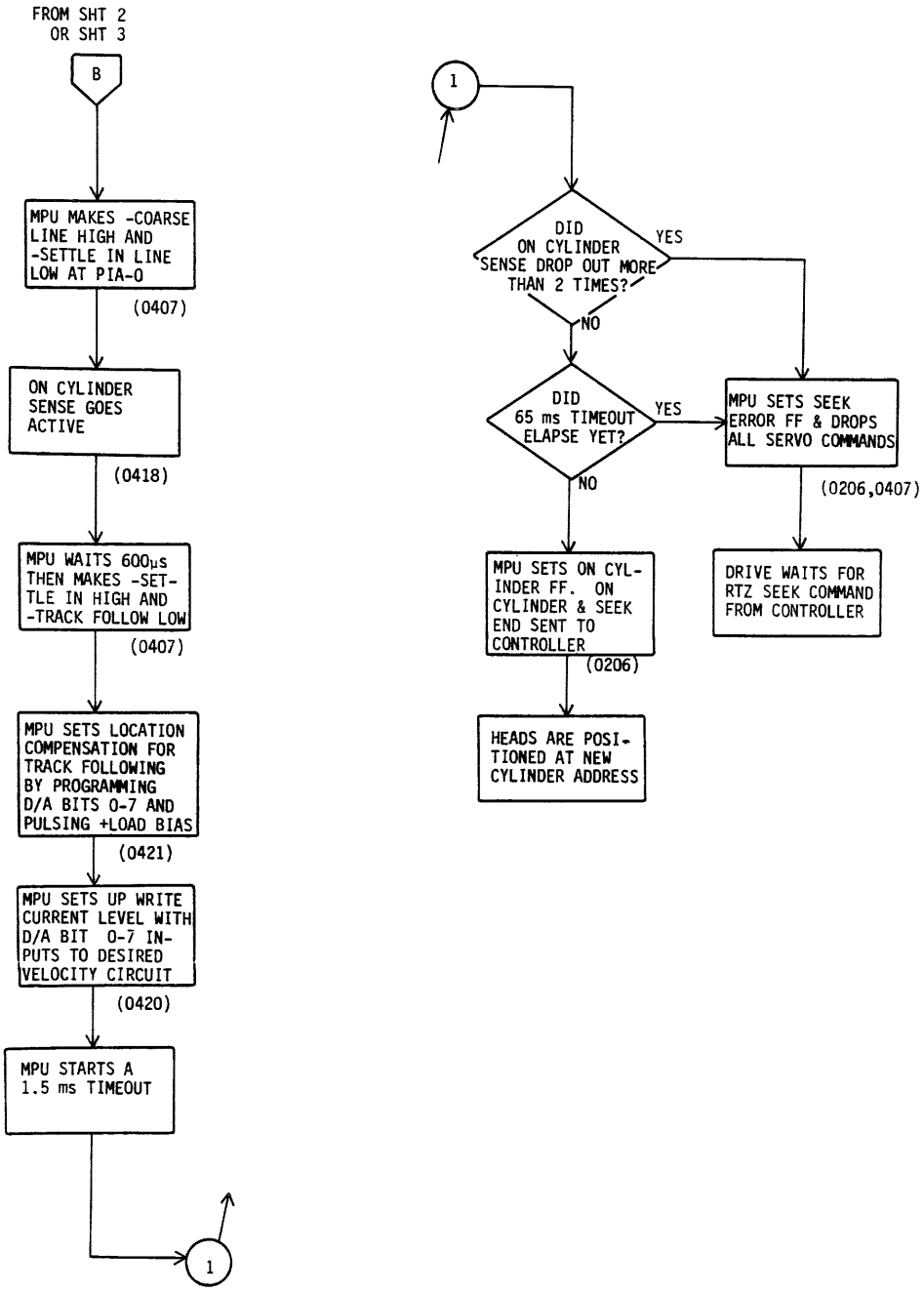


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Figure 1-44. Normal Seek Flowchart (Sheet 4)

In all seeks, the MPU presets certain signal lines to condition the coarse servo loop. The -Forward line is switched low for in direction seeks or high for out direction seeks. The MPU initializes the velocity measurement circuit by setting or clearing the Last Peak latch. It uses the +Velocity Preset line to set or clear the latch when the -Track Follow line goes high. The MPU checks to make sure that there is no fault condition and that the Speed OK and Demodulator OK signals are active. If these conditions are met, the MPU loads the PTM #3 counter with an 65 millisecond timeout count (so that a Seek Error will be indicated if the seek is not completed at the end of the timeout). The MPU sets or clears the +Slope line to the tribit decoder circuit to ensure that the decoded position signal has the proper phase at the destination track. The MPU presets the location compensation circuit to the value required at the destination track by placing the eight most significant cylinder address bits on the D/A Bit 0-7 lines. The MPU pulses the +Load Bias line to load these values into the circuit.

The remaining coarse seek is very different for one-track seeks than it is for longer seeks. For one-track seeks, the MPU references the velocity table in the ROM and inputs the desired velocity D/A Converter with the value for T<1. The MPU then starts the seek by making the -Track Follow line high and the -Coarse line low. It also clears the +Velocity Integrator Clamp line, allowing the Velocity Integrator to generate the Integrated Velocity signal. The level of Integrated Velocity contributing to the +Desired Velocity signal is determined by the $+T \leq 16$ line (which is set) and D/A bits 6 and 7 (which are controlled by the velocity table). With a constant D/A input, a decelerating velocity profile results as the Integrated Velocity signal ramps up. The Integrated Velocity signal subtracts more and more from the D/A Converter velocity signal to bring the Desired Velocity signal toward zero. The MPU monitors the -Fine Enable line, and it switches from coarse to fine loop operation when -Fine Enable goes low.

For seeks greater than one track, a different coarse seek sequence is managed by the MPU. For T<256, the MPU gives the desired velocity D/A Converter its maximum input (setting D/A Bits 0-7 to one). For T<256, the MPU references the velocity table in the ROM and inputs the desired velocity D/A Converter with the values tabulated for T. Also, if the seek length is greater than 16 tracks, the MPU clears the $+T \leq 16$ line. The MPU then starts the seek by making the -Track Follow line high and the -Coarse line low. At approximately 1/3 of a track into the seek, the MPU loads T, the number of tracks to go, into the PTM #2 counter. (A cylinder pulse, generated as the heads cross each track, decrements PTM #2 directly to keep the count T current.)

For seeks greater than 256 tracks, the MPU holds the D/A count at maximum and disables the Velocity Integrator by keeping the +Velocity Integrator Clamp line high until T=256. Each Cylinder Pulse input to PIA-0 causes the MPU to check the count T in PTM #2. When T reaches 256, the MPU controls the deceleration of the actuator.

For seeks less than 256 tracks and for longer seeks that have entered the deceleration phase, the MPU changes its inputs to the desired velocity circuit every time it sees a Cylinder Pulse at PIA-0. The MPU prepares the next circuit input with the following loop operation. It reads the current difference count T from the PTM #2 counter and decrements this count by one. It references the velocity table in ROM to obtain the values for D/A Bits 0-7 during the next track. The MPU waits for the next Cylinder Pulse input to PIA-0 and then revises the D/A count to the values it just prepared. Also, the MPU pulses the +Velocity Integrator Clamp line at each cylinder crossing. Each pulse on this line clamps the Integrated Velocity signal to zero. The MPU repeats this loop operation at each cylinder crossing until T=1.

As the loop repeats, the MPU also monitors T and sets the $+T\leq16$ line when T=16. The $+T\leq16$ line, when true, increases the fill-in signal from the Velocity Integrator and gates D/A Bits 6 and 7 so they also control the level of fill-in signal in this portion of the seek.

When T=1, the MPU monitors the -Fine Enable signal. This signal goes low with approximately 1/3 of a track to go. The MPU reacts by switching the -Coarse signal high and the -Settle In signal low via PIA-1 to place the servo in the first (track-capture) phase of the Fine Servo loop.

The MPU looks for the On Cylinder Sense signal (which goes high when the Position signal reaches 0.75 V) from the servo level detect circuits. With On Cylinder Sense active, the MPU waits 600 microseconds and then drops the Settle-In command and issues the Track Follow command. Switching from the settle-in loop to the track-following loop provides a low frequency gain boost to the positioning signal. The MPU presets the location compensation circuit for track-following operation by setting certain D/A bit 0-7 lines and then pulsing the +Load Bias line to latch these values for input into the Location Compensation D/A Converter. The location compensation circuit converts these digital inputs to a zero volt analog output. The MPU sets the Write Current Level for the destination track by placing the eight most significant cylinder address bits on the D/A bit 0-7 lines for input to the D/A Converter in the desired velocity circuit.

The MPU again checks for an active On Cylinder Sense signal, and then allows a 1.5 millisecond timeout to ensure that the actuator has settled on track. The MPU checks overshoot by monitoring On Cylinder Sense during the timeout and requiring that the signal goes inactive no more than two times. The MPU ends the seek routine by setting either the On Cylinder FF or the Seek Error FF in the I/O Gate Array, using I/O Control lines 1 and 2. It sets the On Cylinder FF provided that settle-in occurred without excessive overshoot. Otherwise, the MPU sets the Seek Error FF and drops all servo commands, allowing the actuator to fall to the resting position over the data zone. In either case, the MPU then waits for further commands from the controller.

Return to Zero Seek

The Return to Zero (RTZ) seek is the operation that moves the heads from any location on the disk to track 0. Although the MPU uses an RTZ seek as part of the load operation, the controller can command RTZ seeks also. Both types of RTZ seeks are identical, except for the status presented if they fail. If the RTZ seek in a load operation is unsuccessful, the MPU lights the First Seek fault indicator, and a reattempt occurs only if the Fault Clear switch is pressed. If a controller-initiated RTZ seek is unsuccessful, the MPU sets the Seek Error FF, and Seek Error is active on the I/O. In this case, the drive waits for another RTZ command from the controller.

This discussion pertains specifically to the controller-initiated RTZ seek. This seek is flow-charted in figure 1-45. Refer to the Load Operation discussion for details about the RTZ portion of the load operation.

The controller initiates an RTZ operation by outputting Tag 3 (Control Select) along with Bus bit 6. The RTZ Seek command is decoded on the I/O Gate Array where it clears the Cylinder and Head Address registers, the On Cylinder FF, and Seek Error FF (all in the I/O Gate Array). In addition, the I/O Gate Array sends the RTZ interrupt to PIA-0 on the Control Board to generate an interrupt to the MPU.

The MPU reads the RTZ interrupt and initiates the RTZ. The MPU presets the Slope line to ensure that the +Position signal will have the correct phase as the heads settle in at their destination track (track 0). Also, the MPU clears D/A bits 0-7 and loads their values into the location compensation D/A converter by pulsing the +Load Bias line at PIA-0. This prepares the location compensation for operation at track 0.

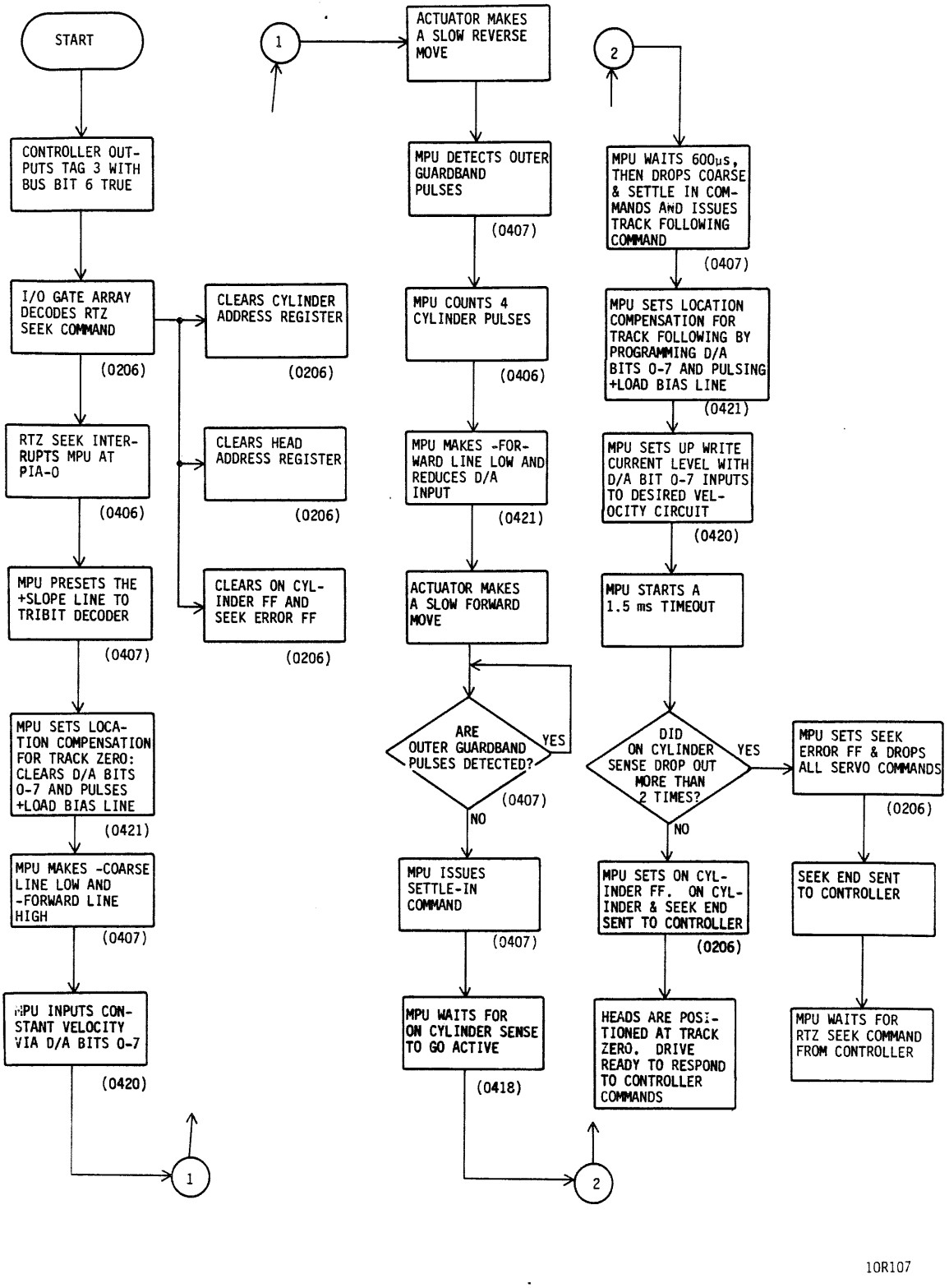


Figure 1-45. Return to Zero (RTZ) Seek

The MPU commands a slow reverse move to take the heads from their resting position (in the data zone) into the outer guard band. To do this, the MPU switches the -Coarse line low and the -Forward line high. The MPU inputs the D/A converter with a constant desired velocity via D/A bits 0-7 from PIA-2.

The reverse move continues until the MPU sees Outer Guard Band Pulses at PIA-1 followed by 4 Cylinder pulses. After the fourth Cylinder pulse, the MPU commands a slower forward move by switching the -Forward line low and inputting reduced values to the D/A converter.

The forward movement uses the Coarse servo input to the Summing Amp initially and, when Outer Guard Band Pulses cease, adds the Settle-In servo input to the Summing Amp. As described under Servo Surface Decoding, the buffer zone consists of 5 tracks located between the outer guard band and track 0 of the data zone. As the servo head moves through the buffer zone, the tribit demodulator develops a constant negative Position signal. Adding the Settle-In input develops a controlled velocity profile from this feature of the Position signal.

The MPU looks for the On Cylinder Sense signal (which goes high when the Position signal reaches 0.75 V) from the servo level detect circuits. With On Cylinder Sense active, the MPU waits 600 microseconds and then drops the Coarse and Settle-In commands and issues the Track Follow command. The Track Follow signal adds a low frequency gain boost to the positioning loop. The MPU presets the location compensation circuit for track-following operation by setting certain D/A bit 0-7 lines and then pulsing the +Load Bias line to latch these values for input into the Location Compensation D/A Converter. The location compensation circuit converts these digital inputs to a zero volt analog output. The MPU sets the Write Current Level for track 0 by placing the eight most significant cylinder address bits (all zeros) on the D/A bit 0-7 lines for input to the D/A Converter in the desired velocity circuit.

The MPU again checks for an active On Cylinder Sense signal, and then allows a 1.5 millisecond timeout to ensure that the actuator has settled on track. The MPU checks overshoot by monitoring On Cylinder Sense during the timeout and requiring that the signal goes inactive no more than two times. The MPU ends the RTZ operation by setting either the On Cylinder FF or the Seek Error FF in the I/O Gate Array, using I/O Control lines 1 and 2. It sets the On Cylinder FF provided that settle-in occurred without excessive overshoot. Otherwise, the MPU sets the Seek Error FF and drops all servo commands, allowing the actuator to fall to the resting position over the data zone. In either case, the MPU then waits for further commands from the controller.

Unload Operation

The MPU uses the unload operation during the power off sequence to move the heads completely inward until they are located over the landing zone. The MPU initiates the unload sequence when it detects a loss of start conditions. A loss of start conditions occurs when the START switch is pressed to release it from the Start position or (in remote operation) when the controller deactivates Sequence Hold.

Seeing a loss of start conditions, the MPU drops all commands to the servo circuitry and then commands a forward seek at low constant velocity. This requires switching the -Coarse and -Forward lines low and supplying the D/A Converter in the desired velocity circuit with constant inputs via D/A Bits 0-7. Also, the MPU starts a timeout for the coarse seek portion of the unload operation.

The MPU maintains these servo inputs while monitoring the -Cylinder Pulses line at PIA-0. When the actuator reaches its end of travel and is held in contact with its inward crash stop, no more Cylinder Pulses are generated. The coarse seek portion of the unload operation ends when no more Cylinder Pulses are generated or when the timeout has elapsed. The MPU drops the Coarse command and issues the Retract command. With the Retract command in effect, the Retract Amplifier on the Power Amp board supplies the actuator with in direction current that holds the heads over the landing zone (see the Retract Control Circuitry discussion).

After issuing the Retract command, the MPU delays 1/2 second and drops the Unlock Actuator command, causing the actuator locking solenoid to latch the actuator with the heads located over the landing zone. One second later, the MPU drops the Motor Run command. The MPU monitors Motor Sensor pulses at the PTM #3 counter; when the motor has stopped rotating, the MPU waits two seconds and drops the Retract command. The MPU then waits for start conditions to reappear before initiating a load operation.

HEAD OPERATION AND SELECTION

GENERAL

Information is recorded on and read from the disk by the read/write heads (refer to figure 1-46). The drive requires one read/write head for each data recording surface in the disk module as shown. The FSD drive has ten recording surfaces. For this reason, before a read or write can be performed, the controller must command the drive to select the head located over the disk surface where the data is to be read or written.

The following discusses how the heads read and write the data and also how the desired head is selected.

HEAD FUNCTIONAL DESCRIPTION

Each read/write head has two opposing coils wound on the same core. The coils interface to the read/write circuitry via LSI chips in the R/W Preamp. There are two LSI chips, each responsible for five of the ten heads. In response to the signal inputs, the LSI chips select one of the ten heads, and either provide current switching for the head in write operations or amplification of voltage induced in the head in read operations. Refer to Read/Write Functions for details about the R/W Preamp.

During write operations, the read/write head develops a changing flux pattern on the disk surface passing beneath it. The R/W Preamp supplies the selected head with a source of write current. At each transition of the write data signal,

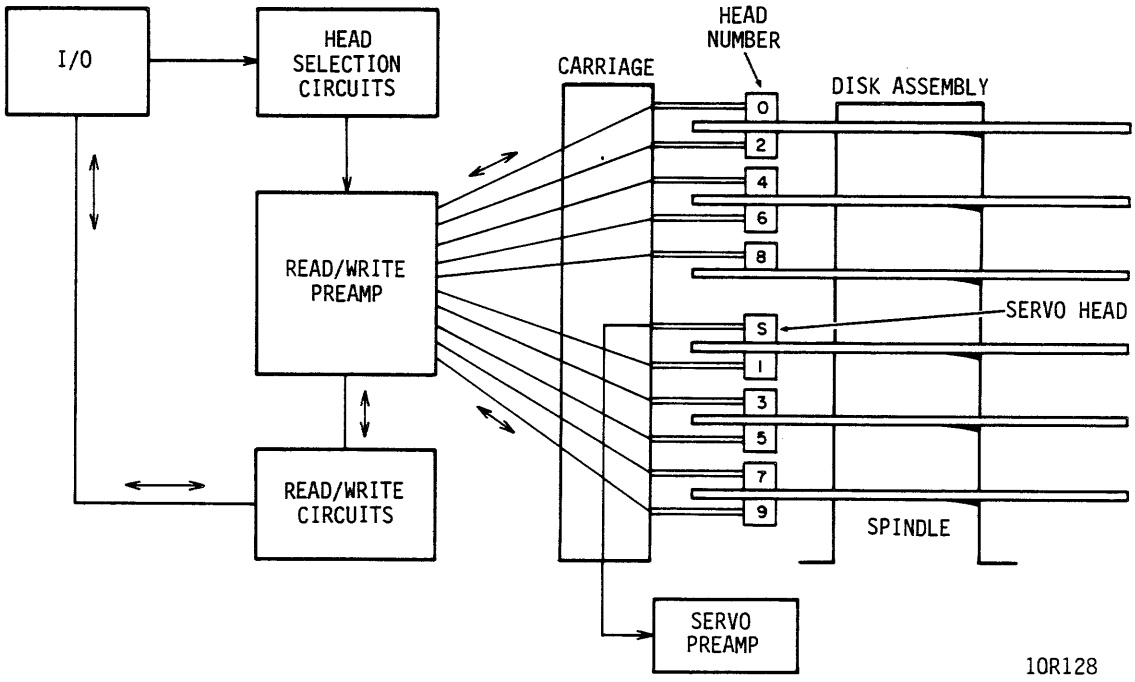


Figure 1-46. Read/Write Heads

the preamp disables one coil and enables the other. Since the two coils have opposing windings, this switching reverses the flux across the gap in the head (see figure 1-47). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a north pole and a south pole. The writing process orients the poles to store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of write current switching while its amplitude depends on the amount of current (the greater the current, the more oxide particles that are affected).

Information (data) is written by switching the current through the head. Switching between the two head coils reverses the direction of the flux field across the gap. The flux change defines a data bit.

New data is written simply by writing over any data which may already be on the disk. The write current is zoned to ensure proper saturation level for best head resolution (refer to discussion on Write Current Control). The write current is maximum on the outer tracks and minimum for the inner tracks.

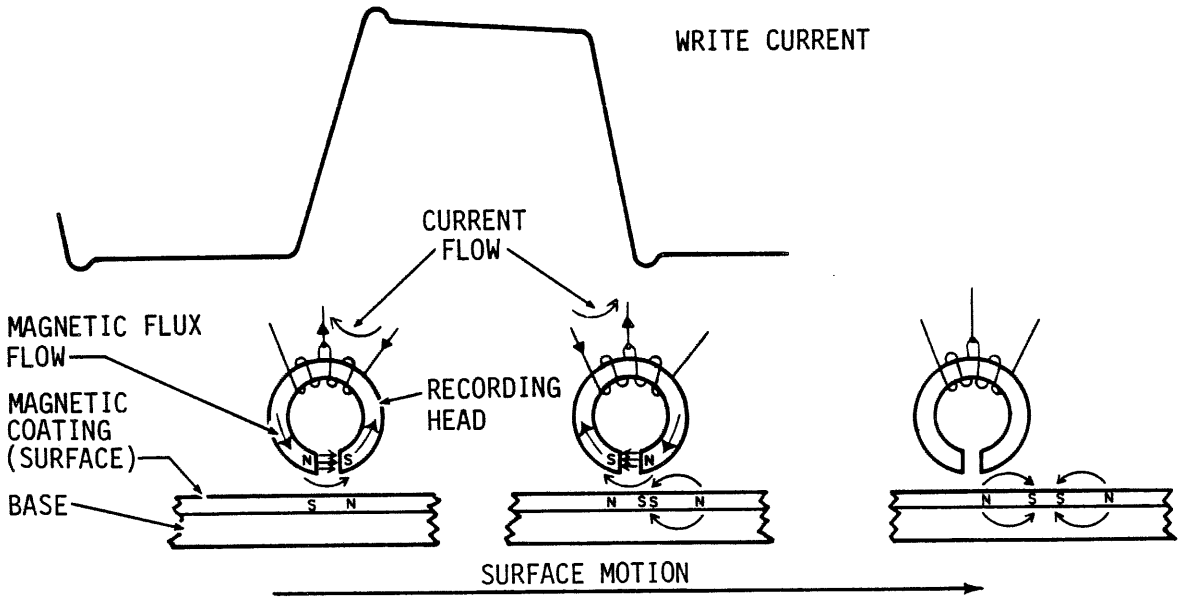
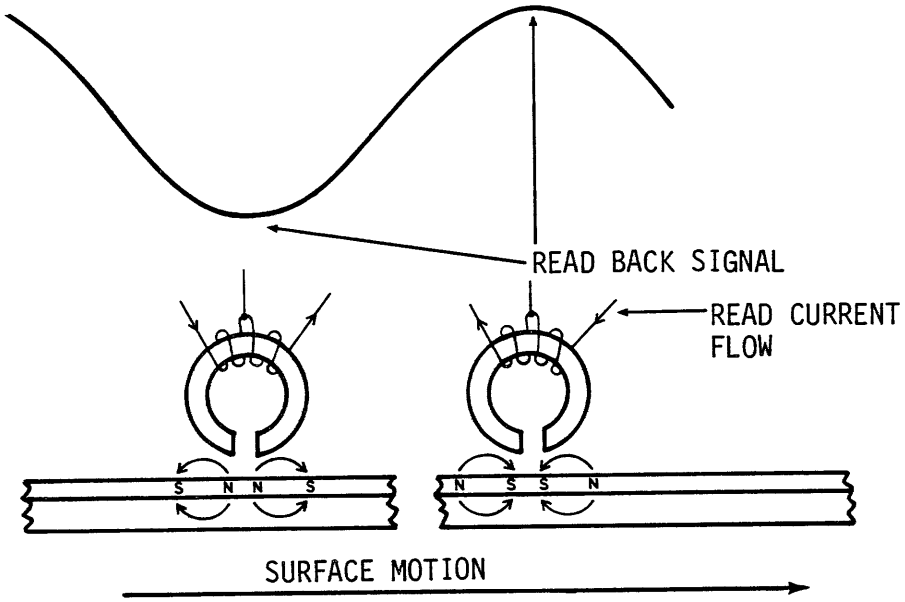


Figure 1-47. Writing Data



NOTE: RELATIVE HEAD TO SURFACE MOTION, REPRODUCING (READ OPERATION)

10R130

Figure 1-48. Reading Data

During a read operation, disk motion beneath the head causes the stored flux to induce a voltage in the heads (refer to figure 1-48). This voltage is analyzed by the Read circuit to define the data recorded on the disk. Each flux reversal (produced while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

HEAD SELECTION

A head must be selected before a read or write operation can be performed. Prior to head selection, the controller issues a cylinder select command. Under MPU control, the servo system moves the heads to the cylinder specified by the controller. By selecting a head, the controller specifies a particular track within that cylinder. Head selection starts when the controller sends the drive a Head Select (Tag 2) command and a head address. The head address is sent on Bus bits 0 through 3.

The Head Select tag gates the address into the Head Address register (HAR) in the I/O Gate Array. Figure 1-49 shows the head selection circuits. The cylinder address and the head address are multiplexed out of the gate array on +Head/Cylinder Address lines 0-3. The MPU controls this multiplexing with I/O Control lines 1 and 2. In the initial phase of a seek, the Head/Cylinder Address lines transfer the new cylinder address to the MPU. With this transfer complete, the lines carry head address information. Thus, whenever the heads are on cylinder, +Head Address line 0 reflects HAR bit 0, and so forth.

The Head/Cylinder Address lines go from the I/O board to the Data Latch board via the Control board. The Data Latch board develops the -Head/Cylinder Address 0 signal, which it sends with the four active-high lines to the R/W Preamp. The R/W Preamp has two LSI chips: one controls the five odd-numbered heads and the other controls the five even-numbered heads. The +Head/Cylinder Address 0 line selects one LSI chip when it is high and the other when it is low. The selected LSI chip enables one of its five associated heads depending on +Head/Cylinder Address lines 1-3, which connect to its addressing inputs. If the preamp receives an illegal head address (10 through 15), no head is selected. A Write Fault occurs if the drive attempts to write data with no head selected. Table 1-3 shows the combination of address lines that selects each head.

READ/WRITE FUNCTIONS

GENERAL

When the drive is on cylinder and has a head selected, it is ready to perform a read or write operation. The controller initiates a read or write operation by sending a Control Select (Tag 3) along with the proper bus bit (Bit 0 for Write Gate and Bit 1 for Read Gate). During a write operation, the drive receives data from the controller and writes it on the disk. During a read operation, the drive recovers data from the disk and transfers it to the controller.

Figure 1-50 is a block diagram of the read/write circuits. The remainder of the discussion describes the read/write circuits and is divided into the following areas:

- Basic Read/Write Principles -- Explains the principles of recording and recovering data from a magnetic disk.
- Write Circuits -- Describes the circuits used by the drive to record data on the disk.
- Read Circuits -- Describes the circuits used by the drive to recover data from the disk.

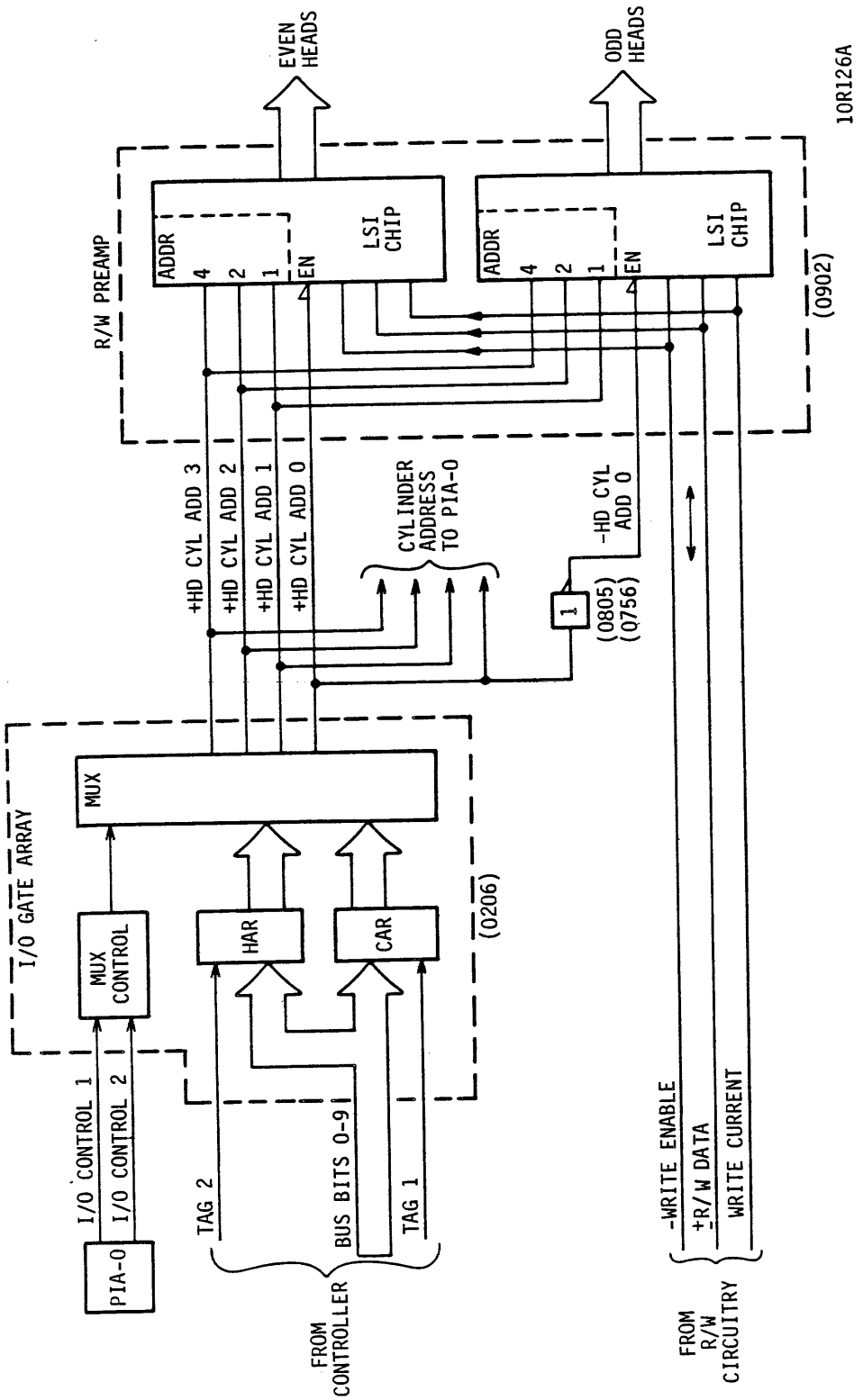


Figure 1-49. Head Selection Circuits

TABLE 1-3. HEAD SELECT ADDRESSING

Head Selected	+Head/Cylinder Address Lines			
	0	1	2	3
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
	0	1	0	1
Illegal	1	1	0	1
	0	0	1	1
	1	0	1	1
Addresses	0	1	1	1
	1	1	1	1

Depending on drive configuration, the drive has either one read/write board (__RUX) or two read/write boards (__PFX and _PGX). The cross reference numbers assigned to these logic diagrams and used in the block diagrams for this read/write function discussion are:

- 070X for _PGX board
- 080X for _PFX board
- 075X for _RUX board

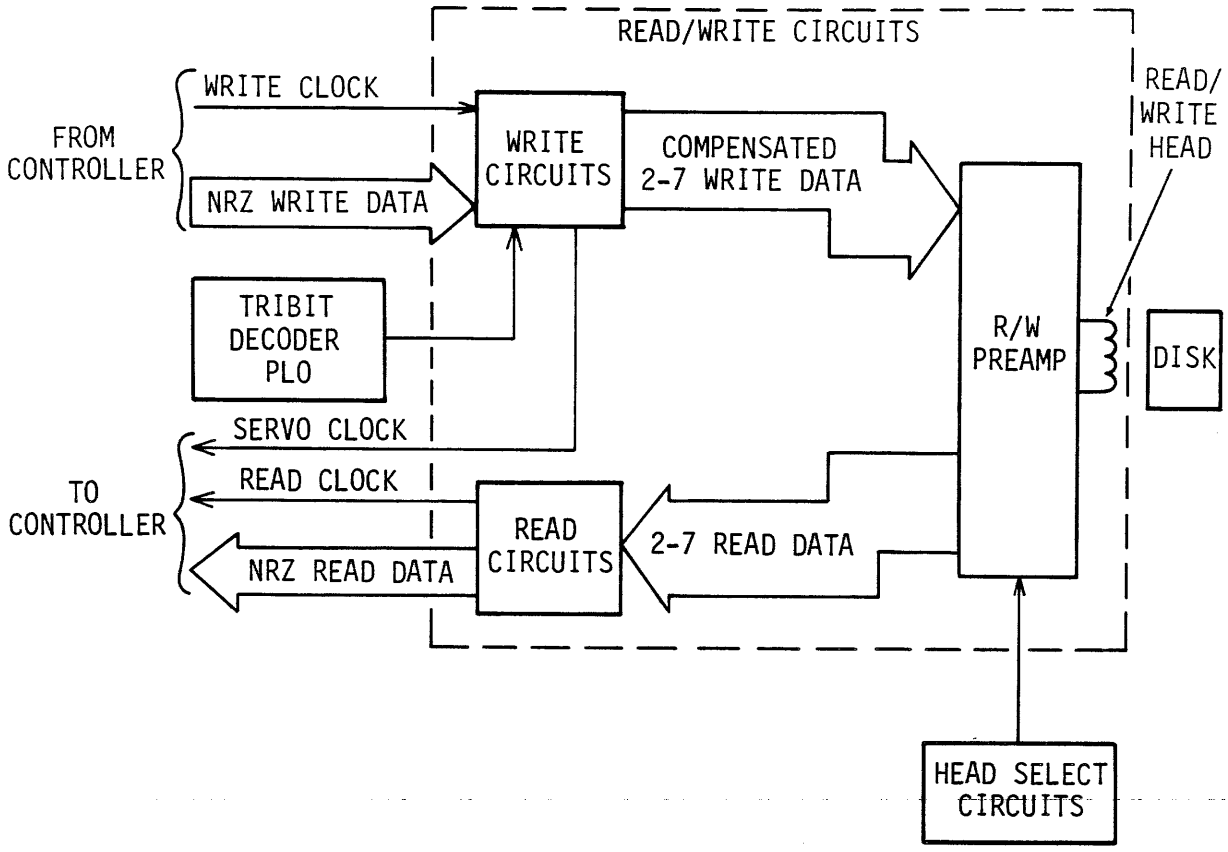


Figure 1-50. Read/Write Circuits

BASIC READ/WRITE PRINCIPLES

Principles of 2-7 Recording

The FSD employs two modulation schemes for read/write data transfers. The controller transfers data on the interface with Non Return to Zero (NRZ) modulation in a write operation.

Write circuitry in the drive encodes the incoming data by changing it to 2-7 modulation. Transfers between the read/write circuitry and the disk use 2-7 modulation. Therefore, in a read operation, read circuitry in the drive must decode the 2-7 read data to create NRZ data which is suitable for the controller. The following paragraphs define both modulation schemes and explain why 2-7 modulation is used in the drive.

NRZ data is transferred at a nominal rate of 9.67 MHz. Each data bit is defined throughout an interval called a bit cell, and the nominal duration of each bit cell is 103 ns. For consecutive cells indicating binary 1, the read or write interface line is driven at the active level. For consecutive cells indicating binary 0, the read or write interface line is driven at the inactive level. Thus, NRZ data lines return to zero only when the transferred data changes from binary 1 to binary 0.

For disk transfers, the 2-7 scheme is superior to the NRZ scheme in two ways. First, it reduces the average rate of flux reversals on the disk; this permits greater recording density on the disk. Second, the recording bandwidth, or range from the minimum to maximum flux reversal rate, is limited; with narrowed bandwidth, the read/write circuitry has fewer noise problems.

The translation between NRZ modulation and 2-7 modulation is a translation of seven basic code words, as shown in table 1-4. Any string of NRZ data can be expressed as a series of these individual code words. The corresponding 2-7 data string is a series of translated code words where each 2-7 code word has replaced its corresponding NRZ word. So, the write circuitry encodes the NRZ data as 2-7 data, and the read circuitry decodes the 2-7 data as NRZ data.

Each 2-7 code word has twice as many bits as its related NRZ code word. Therefore, the 2-7 bit cell is half the NRZ bit cell or 51.5 ns, nominal. As the 2-7 data is written on the disk, the head changes its flux each time the code contains a binary 1. Although 2-7 uses twice the bit rate of NRZ, binary ones appear in 2-7 code less frequently than level changes occur in the corresponding NRZ code. Therefore, use of 2-7 code allows data to be written more densely on the disk.

The name 2-7 derives from the fact that preceding and following each occurrence of binary 1 in the code, there are at least two zeros and as many as seven zeros.

Peak Shift

Peak shift is a predictable effect that would complicate decoding of the 2-7 read signal if it were not compensated in the write circuitry. The following paragraphs explain why peak shift occurs and how write compensation reduces the effect of peak shift.

TABLE 1-4. TRANSLATION BETWEEN NRZ AND 2-7 CODES

NRZ Code Words	2-7 Code Words
00	1000
01	0100
100	001000
101	100100
111	000100
1100	00001000
1101	00100100

Figure 1-51 shows selected write and read signals that are relevant to the description of peak shift. The write data line toggles each time a binary 1 appears in the 2-7 data string. Each toggle of write data reverses the magnetic flux in the data head to produce a region of changing recorded flux in the disk surface. The flux reversal on the disk has a finite length on the disk because of the shape of the flux pattern from the head gap and the inability of the head to reverse its magnetic flux instantaneously.

In read operations, the data head develops a composite readback voltage as it intercepts changing flux from the disk surface. Each flux reversal creates a readback voltage peak, as shown in figure 1-51. The composite readback voltage, developed by the head passing over a flux reversal, is a superposition of the peak caused by that flux reversal and by the leading and trailing edges of the peaks caused by the adjacent flux reversals. Any difference in the contributions of the two adjacent peaks will shift the central peak away from the closer adjacent peak.

Accurate decoding in read operations requires that the raw read data signal has timing intervals identical to those in the write data signal. Peak shift lengthens certain intervals and shortens other intervals in a manner that is predictable from the spacing of adjacent peaks. Write compensation anticipates this problem by advancing or delaying each write transition by an amount that depends on the number of binary 0s leading and trailing the binary 1 producing that transition. When the number leading exceeds the number trailing, write compensation de-

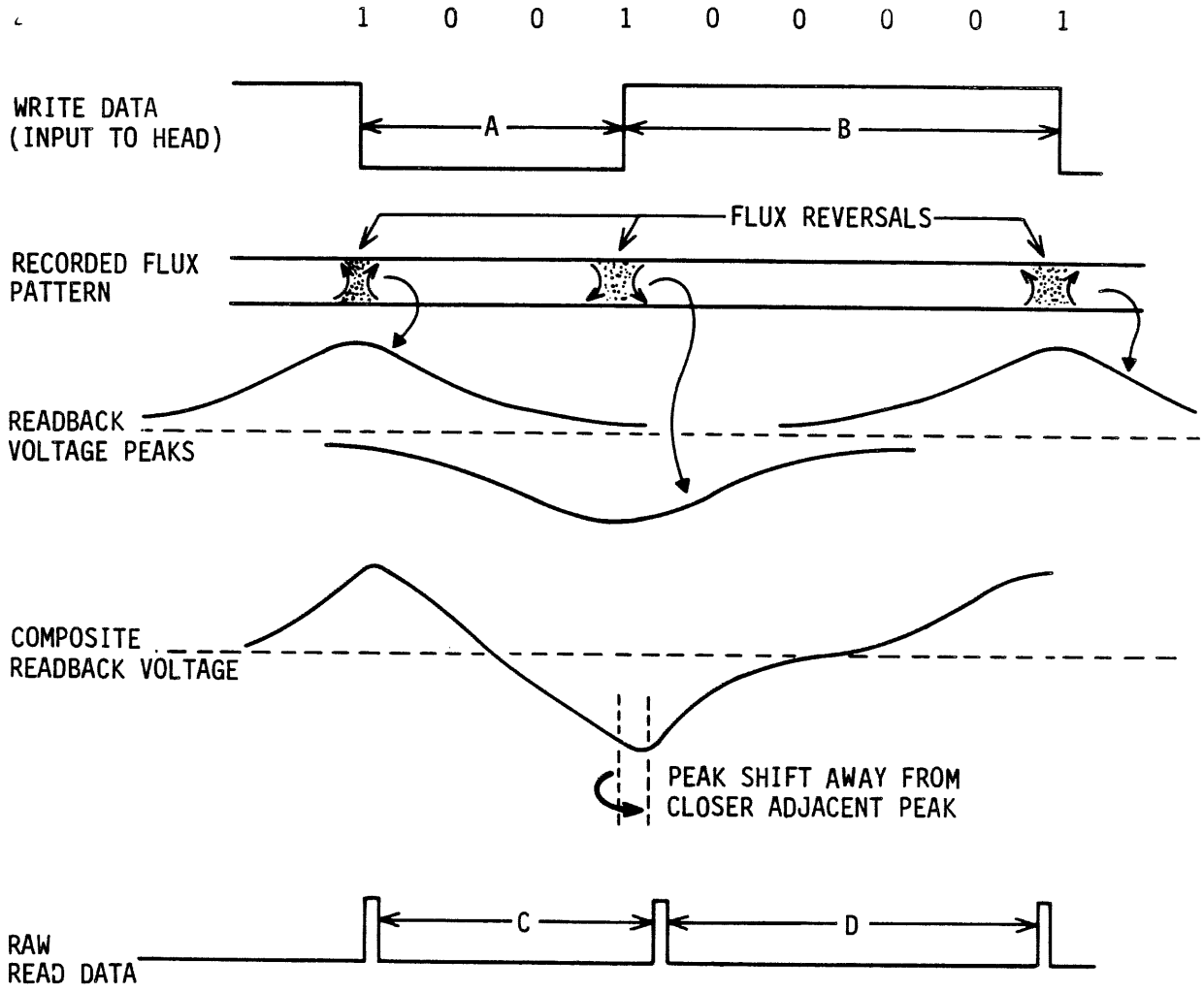


Figure 1-51. Peak Shift Waveforms

lays the write transition. When the number trailing exceeds the number leading, write compensation advances the write transition. When the two numbers are equal, the transition occurs without compensation. Thus, compensated write data drives the heads, and the raw read data contains the same timing as the uncompensated write data.

The discussion of Write Compensation under Write Circuits includes a table that defines the compensation shift for each possible data pattern.

WRITE CIRCUITS

General

The write circuit operation is initiated by Tag 3 (Control Select) with Bus Bit 0 true. This allows the drive to start processing serial NRZ data received from the controller. NRZ data is synchronized to the 9.67 MHz Servo Clock derived from the Write PLO. The Write Data is received via the Write Data line and is first sent to the 2-7 encoder circuit. This circuit converts the data to 2-7 modulation and sends it to the write compensation circuit. Write compensation modifies the data timing to compensate it for peak shift (refer to discussion on basic read/write principles for more information concerning peak shift). The compensated data is then processed by the write driver circuit. The write driver circuit provides the data signal that controls current switching in the R/W preamp, and the current being switched is supplied by the write current control.

Figure 1-52 shows the write circuits and table 1-5 briefly explains their function.

Write PLO

The Write PLO circuitry uses a phase-locked loop to generate the 19.34 MHz (2F) Write Clock. As shown in figure 1-53, this circuitry consists of frequency dividers, a coincidence comparator, a charge pump, and a voltage-controlled oscillator (VCO). The frequency dividers and coincidence comparator are located in the Write Compensation and PLO ECL Logic Array.

The phase-locked loop uses the 1.612 MHz Clock from the Tribit Decoder PLO as a frequency reference (refer to the Servo Surface Decoding discussion). The Write VCO operates under loop control to generate the 19.34 MHz (2F) Write Clock, at twelve times the frequency of the reference clock. Two divisions by two and one division by three of the VCO output develop a 1.612 MHz feedback signal that can be compared to the reference clock to adjust the loop operation.

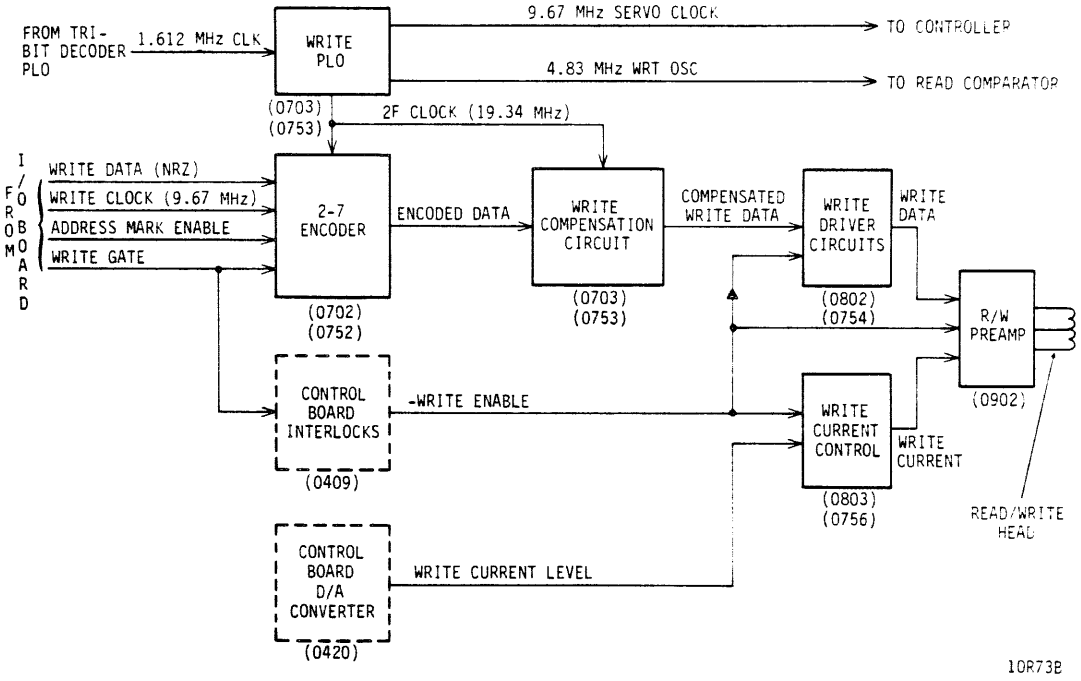


Figure 1-52. Write Circuits Block Diagram

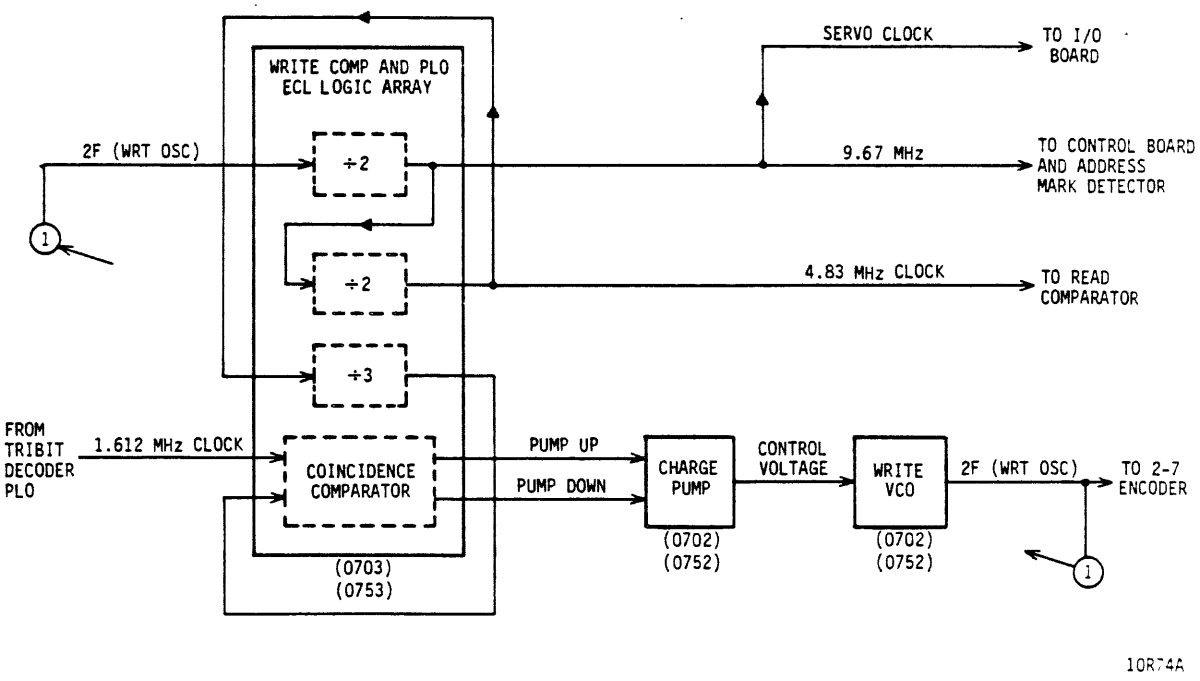


Figure 1-53. Write PLO Block Diagram

TABLE 1-5. WRITE CIRCUIT FUNCTIONS

Circuit	Function
Write PLO	Generates the 19.34 MHz Write Clock which is divided by two to develop the 9.67 MHz Servo Clock.
2-7 Encoder	Converts the NRZ data from the controller to 2-7 data.
Write Compensation Circuit	Compensates the data for problems caused by peak shift.
Write Driver Circuits	Produces a write signal that changes polarity each time the compensated 2-7 data goes to a binary 1.
Write Current Control	Produces a write current amplitude that is suited to the diameter of the track being recorded. Recording requires less current as the diameter is reduced.
R/W Preamp	Switches the write current between two opposing head coils as the signal from the write driver circuits changes polarity.

The loop reaches phase lock by comparing the coincidence of the leading edges of the reference and feedback clocks. Each time the feedback clock leads the reference clock, the coincidence comparator pulses the Pump Down line. Pump Down pulses cause the charge pump to vary the Control Voltage signal as necessary to reduce the Write VCO frequency until the reference and feedback clocks are coincident (phase-locked). Each time the feedback clock lags the reference clock, the coincidence comparator pulses the Pump Up line. Pump Up pulses cause the charge pump to vary the Control Voltage signal as necessary to increase the Write VCO frequency until phase lock occurs.

The Write PLO circuit operates continuously whenever the servo signal is being decoded. The PLO provides the following outputs to other circuits:

- 2F (WRT OSC) signal to the 2-7 Encoder circuit.

- 9.67 MHz Servo Clock to the controller (via the interface). This is returned to the drive as Write Clock.
- 9.67 MHz clock to several timing circuits on the Control Board.
- 4.83 MHz clock to the Read Comparator circuit.

2-7 Encoder

The 2-7 Encoder converts NRZ data into 2-7 data. As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven NRZ code words and seven 2-7 code words. The encoder recognizes the coding in the write data string as a succession of the seven NRZ words, and outputs a series of 2-7 code words, each one translated from its NRZ equivalent. Table 1-4, presented under Basic Read/Write Principles, shows the translation used between the two groups of seven code words. The 2-7 encoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

The encoder uses synchronous timing circuitry controlled by two clock inputs, the 9.67 MHz Write Clock from the controller and the 19.34 MHz 2F Clock from the Write PLO (see figure 1-54). The encoder has a synchronizer that develops a 9.67 MHz internal clock in phase with the 2F Clock. This internal clock shifts NRZ data into a pattern recognition circuit. Each time this circuit recognizes one of the seven NRZ code words, it parallel-loads an output shift register and starts looking for the following word.

The output shift register shifts its contents on each rising edge of the 2F Clock. The active low serial output of the register is -Encoded Data. This line is active for binary ones and inactive for binary zeros in the 2-7 data unless an address mark is being written. During an address mark, there are no transitions in the written flux, and a segment of the data track is erased. To command an address mark, the controller issues Tag 3 along with Bus bit 0 (Write Gate) and Bus bit 5 (Address Mark Enable). When Bus bit 5 goes inactive, the encoder resumes normal operation.

The encoder begins translating NRZ code words with the first binary zero in the NRZ data occurring on or after the second rising edge of Write Clock. Encoder operation proceeds continuously, processing all NRZ data input to it until Write Gate goes inactive.

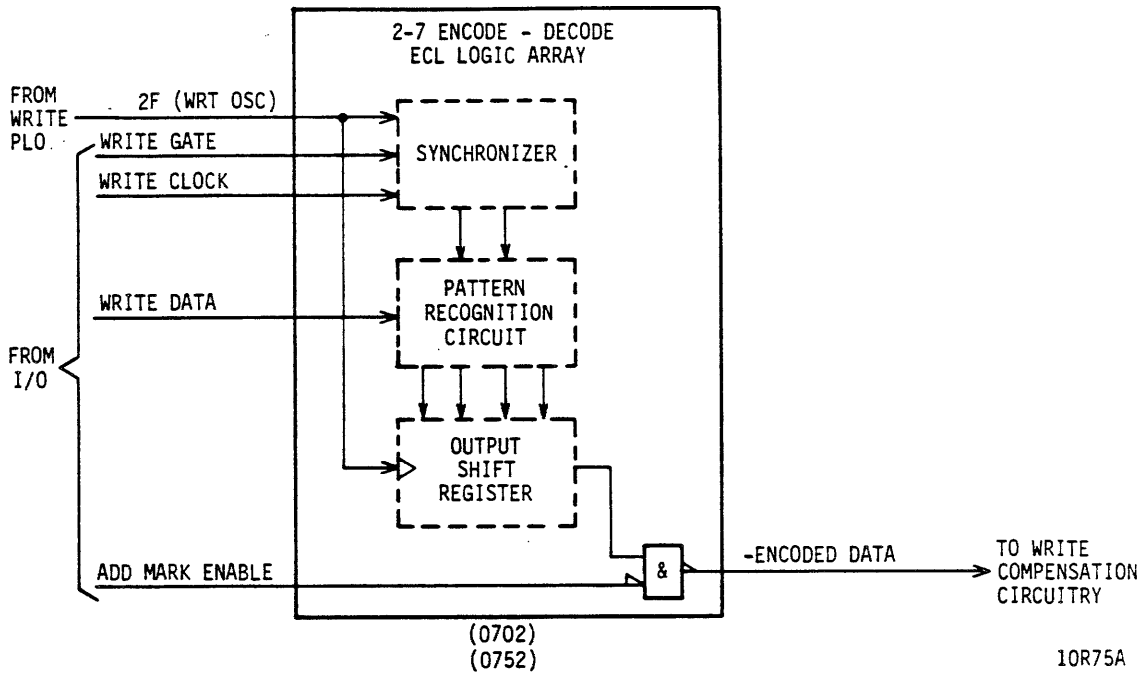


Figure 1-54. 2-7 Encoder Block Diagram

Write Compensation Circuit

The write compensation circuit modifies the timing of transitions in the encoded 2-7 data in a manner that compensates for peak shift (refer to discussion on basic read/write principles).

Encoded 2-7 data contains isolated bit cells at binary one preceded and followed by from two to seven bit cells at binary zero. Each time the data changes from binary zero to binary one, the head reverses its flux direction. Write compensation shifts this positive-going edge away from its nominal timing, and this timing change is related to the number of zeros preceding and trailing a binary one in the data pattern.

The write compensation function takes place in the Write Compensation and PLO ECL Logic Array (see figure 1-55). This chip is capable of following four different compensation schemes as dictated by its "A" and "B" inputs. In this drive, input "A" is pulled low and input "B" is tied high. This selection, and the delays with which the 2F Clock enters chip inputs P1 through P9, produce specified time shifts for each possible data pattern. Table 1-6 specifies the delay for each data pattern relative to the nominal delay present in the circuitry. In the table, negative delays represent earlier timing and positive delays represent later timing.

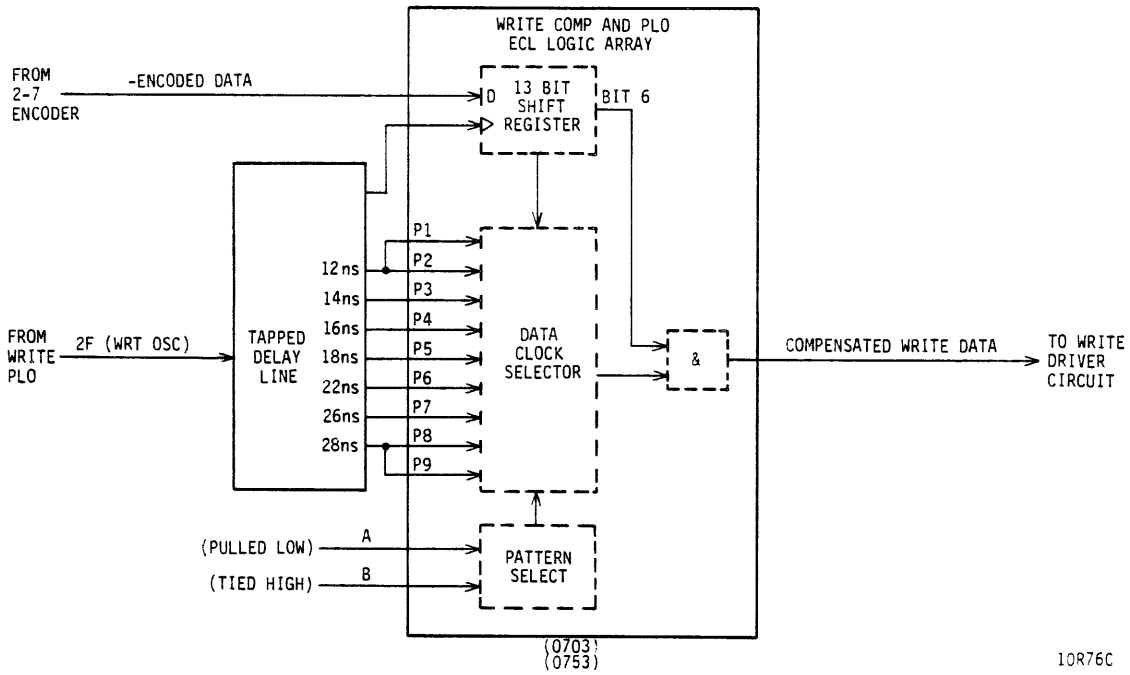


Figure 1-55. Write Compensation Block Diagram

Uncompensated data enters the circuit via the -Encoded Data line. This data is clocked into a 13-bit shift register. The delay line develops the clock input by delaying the 2F clock. When the center bit of the shift register contains a binary one, the circuit looks at the number of register bits which are zero on each side of the center bit. Depending on the number of leading zeros and trailing zeros, one of the delayed clocks P1 through P9 is applied to an AND gate along with the center bit of the register. Thus, the AND gate sees the center register bit go active, followed by the applied clock going active; with both inputs active, the gate outputs a compensated write data pulse. The positive edge of the compensated data pulse is timed by the clock selected.

Table 1-6 specifies the clock input gated out of the write compensation circuit for each possible data pattern. Note that a majority of the data patterns use the P5 clock and have the nominal delay. The nominal delay is the six periods of the 2F Clock required to move a one into the center bit of the shift register plus the 18 ns delay between the P5 clock and the 2F clock.

After being write compensated, the data is transmitted to the write driver circuit.

TABLE 1-6. WRITE COMPENSATION FOR EACH DATA PATTERN

		Number of Trailing Zeros					
		2	3	4	5	6	7
Number of Leading Zeros	2	0 ns* P5**	-2 ns P4	-4 ns P3	-6 ns P2	-6 ns P1	-6 ns P1
	3	+4 ns P6	0 ns P5	0 ns P5	-2 ns P4	-2 ns P4	-2 ns P4
	4	+8 ns P7	0 ns P5	0 ns P5	0 ns P5	0 ns P5	0 ns P5
	5	+10 ns P8	+4 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5
	6	+10 ns P9	+4 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5
	7	+10 ns P9	+4 ns P6	0 ns P5	0 ns P5	0 ns P5	0 ns P5

*Top entry gives delay relative to nominal timing where negative numbers show early timing and positive numbers show late timing.

**Bottom entry indicates which delayed clock enables a compensated output pulse.

Write Driver Circuit

The compensated write data is sent to the Write Driver circuit and is applied as the clock input to a latch. This latch changes state with each positive edge at its clock input. Complementary outputs of the latch drive a push-pull transistor amplifier. Each time the latch changes state, it switches on the transistor that was cut off and switches off the transistor that was conducting. Each transistor drives one of the R/W Data

lines going to the R/W Preamp. During a write operation, these lines alternate going low at each rising edge of compensated write data.

The write driver circuit operates only when the -Write Enable line is active (low). With -Write Enable inactive, the latch remains cleared, and both push-pull transistors are cut off to prevent the R/W Preamp from enabling write current to the data head. The -Write Enable line comes from the Control board and is active only when all the following are true:

- Write Gate is active
- Write Protect is not active
- No faults exist
- Speed OK is active
- Disable Drive FF is cleared

Write Current Control

The write current control is a dc current supply that provides a source of write current for the data head. Figure 1-56 is a simplified block diagram of the write current control and R/W preamp. The current supply is switched on when -Write Enable is active (low) and is biased by a control voltage on the Write Current Level line coming from the Control board. As the cylinder address increases (with the data head closer to the spindle), less write current is needed. Write Current Level, a function of track diameter, adjusts the Write Current amplitude to meet this requirement.

At the end of a seek, the MPU inputs the eight higher-order cylinder address bits to the D/A Converter in the Desired Velocity Generator via D/A bits 0 - 7. At this time, the servo is in the Track Following mode, and the Desired Velocity Generator is removed from the servo loop. The D/A Converter develops an analog voltage on the Write Current Level line. Being unaffected by the two lower-order cylinder address bits, the Write Current Level line is reduced slightly each time the cylinder address is increased by four tracks.

R/W Preamp

The R/W Preamp contains LSI chips that select a data head and either switch write current through the head or amplify the read signal detected by the head (see figure 1-56). These paragraphs concentrate on the preamp's write function and assume that head selection has occurred.

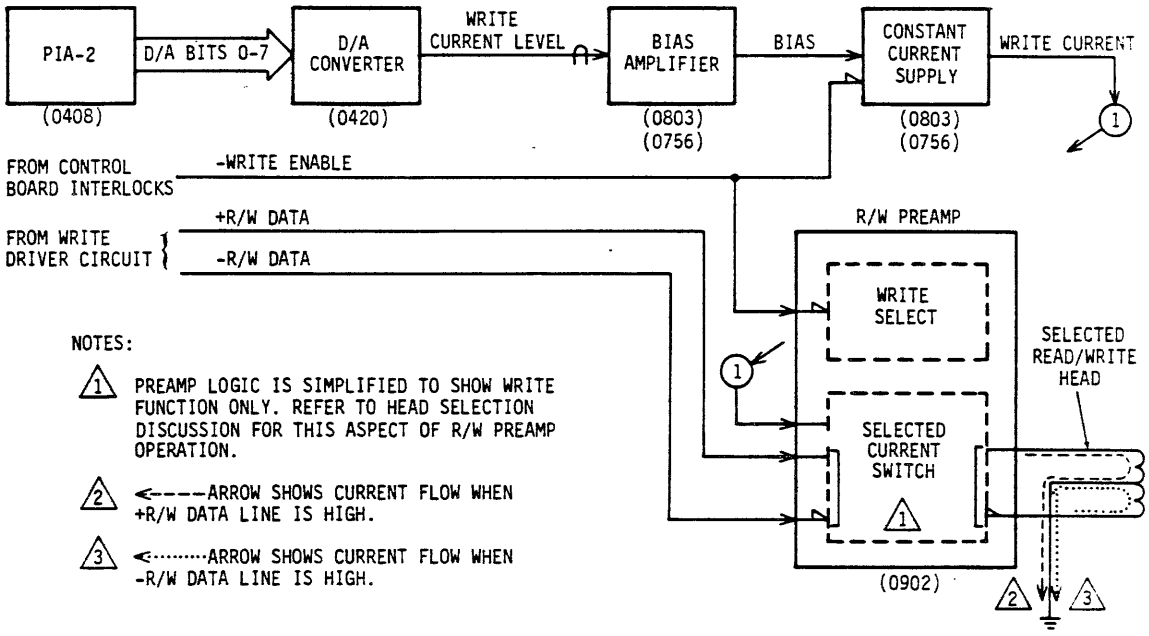


Figure 1-56. Write Current Control and R/W Preamp 10R77A

The LSI chips function as write drivers when the -Write Enable line goes active (low). Each chip develops a regulated voltage source and connects that source to the centertap for its associated heads. Each data head has two opposing coils wound on the same core, and a flux reversal occurs when write current is switched off in one coil and on in the other coil.

Throughout a write operation, Write Current from the Write Current Control is always flowing through one of the head coils. The Write Driver circuit inputs two R/W Data lines to the R/W Preamp. When each of these lines goes low, the selected LSI chip switches the Write Current through the head coil associated with that line. This switching action produces a recorded flux reversal on the disk surface.

While an address mark is being written, there is no switching action, and an unchanging flux is recorded on the disk. Thus, writing an address mark erases a segment of the data track.

READ CIRCUITS

General

Read operations are initiated by a Control Select (Tag 3) with Bus bit 1 true. This enables the preamp circuits, which sense the data written on the disk and generate analog read data signals.

The analog data goes to the Data Latch circuit which changes it into digital 2-7 data.

The Read Comparator and PLO circuit generates a 19.34 MHz Read Clock signal that is phase-locked to the 2-7 read data. The 2-7 Decoder changes the 2-7 data to NRZ data synchronized to a 9.67 MHz Read Clock. Both data and clock are then sent to the controller.

Figure 1-57 shows the main elements in the read circuits and table 1-7 briefly describes each of these elements. The following paragraphs further describe the read circuits.

R/W Preamp

The R/W Preamp contains LSI chips that select a data head and either switch write current through the head or amplify the read signal detected by the head. These paragraphs concentrate on the preamp's read function and assume that head selection has occurred.

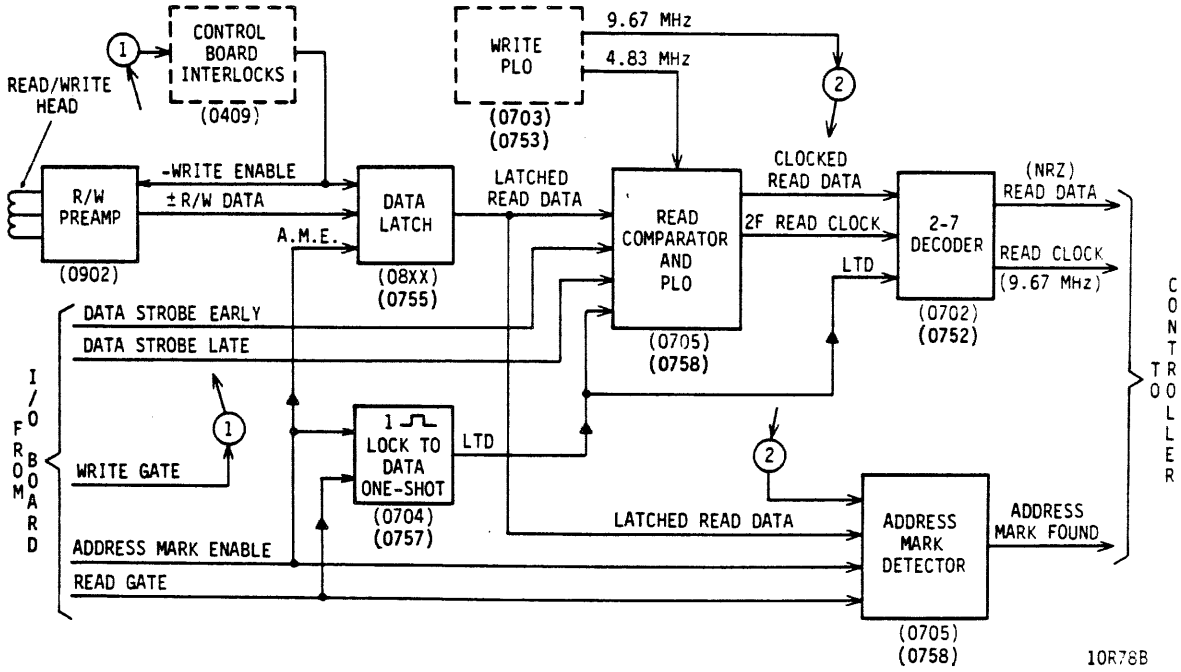


Figure 1-57. Read Circuits Block Diagram

TABLE 1-7. READ CIRCUIT FUNCTIONS

Circuit	Function
R/W Preamp	Processes the analog signal from the data head so that it can be used by the Data Latch circuit.
Data Latch Circuit	Changes the analog 2-7 data into digital 2-7 data. This data is sent to the Read Compensation circuit.
Read Comparator and PLO Circuit	Develops a 19.34 MHz Read Clock that is synchronized to 2-7 read data.
2-7 Decoder	Translates data coding from 2-7 to NRZ modulation and generates 9.67 MHz Read Clock synchronized to NRZ data. NRZ data is sent to the controller with the 9.67 MHz Read Clock.
Address Mark Detector	Detects the address mark and transmits an Address Mark Found to the controller.

The LSI chips function as read preamps when the -Write Enable line is inactive (high). These chips contain a separate differential amplifier for each head, and head selection enables the differential amplifier associated with the desired head. In read operations, both coils in the selected head develop a readback pulse when the head passes over a written flux reversal on the disk. The head coil centertap is not used, and the other two coil leads provide a differential input to the preamp.

The differential amplifier selected in the chip amplifies the read signal and sends it on the R/W Data lines to read circuitry on the Data Latch board.

Data Latch Circuit

Two different data latch circuits are used in this drive. One is for the one board R/W (_RUX) and the other is for the two board R/W (_PGX and _PFX).

Data Latch Circuit (One Board R/W)

The Data Latch circuit receives analog read data from the R/W Preamp and converts it into digital data. As shown in figure 1-58, most of the Data Latch circuit is located inside the Data Latch Analog Master Chip.

The input signal is amplified by the Buffer Amp, provided that -Write Enable is inactive (high). After further amplification (inside the master chip), the signal is split into three signal paths -- the high resolution channel, the low resolution channel, and the hysteresis channel. The high and low resolution channels contain independent wave-shaping circuitry, and they provide separate inputs to the Data Latch FF. The high resolution channel supplies delayed clock pulses to the Data Latch FF, and the low resolution channel supplies a D-input to the

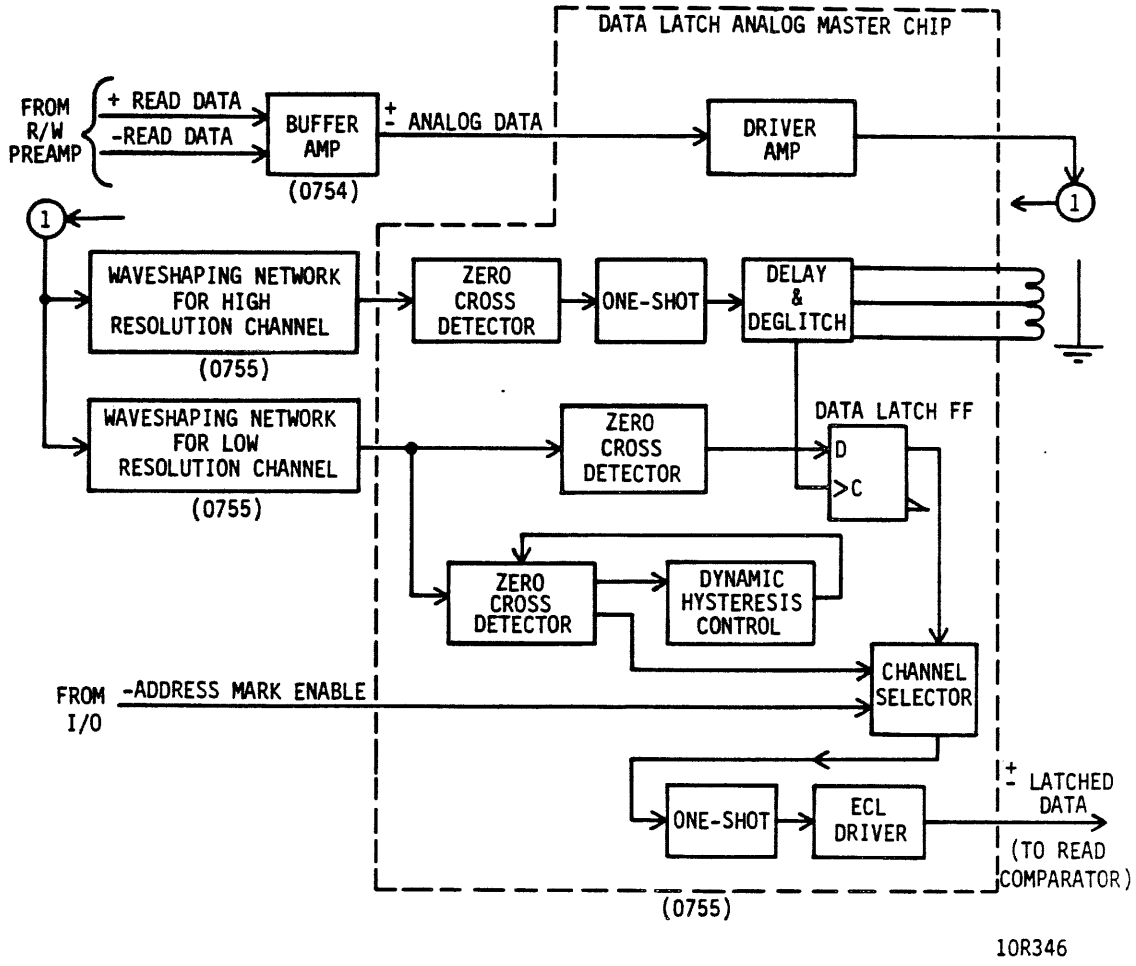


Figure 1-58. Data Latch Block Diagram (One Board R/W)

Data Latch FF. Successive clock pulses toggle the FF when the D-input has changed. During normal write operations, a channel selector sends the output of the Data Latch FF to a one-shot. For each transition of the Data Latch FF, the one-shot pulses the ±Latched Data output lines. Thus, there is an output pulse for each written flux transition sensed by the data head.

Splitting the analog data signal into two paths and combining the high and low resolution channels in the Data Latch FF is a system that discriminates against high frequency noise components in the Analog Data but maintains the timing of the data transitions. The low resolution channel uses a low-pass filter (rolling off at 2.5 MHz) followed by a zero-cross detector to develop a digital waveform similar to the Write Data waveform used in recording. However, filtering out the high frequency components of the input signal lowers the timing resolution of the channel's output signal. The high resolution channel uses a low-pass filter (rolling off at 5.5 MHz) followed by a zero-cross detector and a delayed pulse-forming circuit. With its wider bandwidth, this channel closely follows the timing present at its input. Each change in the low resolution signal is clocked into the Data Latch FF by a delayed clock pulse from the high resolution channel. Erroneous clock pulses from the high resolution channel do not toggle the Data Latch FF because they do not follow a change in the FF's D-input.

The Data Latch circuitry switches into a different operating mode during an address mark search. In an address mark search, the pulses on the ±Latched Data output lines cease when the head is passing over an address mark, which is a previously erased segment of the track. An address mark search is initiated when -Address Mark Enable goes active (low), which happens when the controller issues Control Select (Tag 3) with Bus bits 1 and 5 active. With Address Mark Enable active, the channel selector in the master chip selects the output of the hysteresis channel for the ±Latched Data signal. Inside the master chip, the hysteresis channel contains a zero-cross detector and a dynamic hysteresis control circuit. To regulate operation of this zero-cross detector and to prevent unwanted output pulses during an address mark, the dynamic hysteresis control circuit adjusts the switching thresholds of the zero-cross detector. In this way, noise pulses arising during the address mark are prevented from producing transitions in the output signal.

The ±Latched Data from the Data Latch circuitry is sent to the Read Comparator - Address Mark ECL Logic Array.

Data Latch Circuit (Two Board R/W)

The Data Latch circuit (refer to figure 1-59) receives analog read data from the R/W Preamp and converts it into digital data.

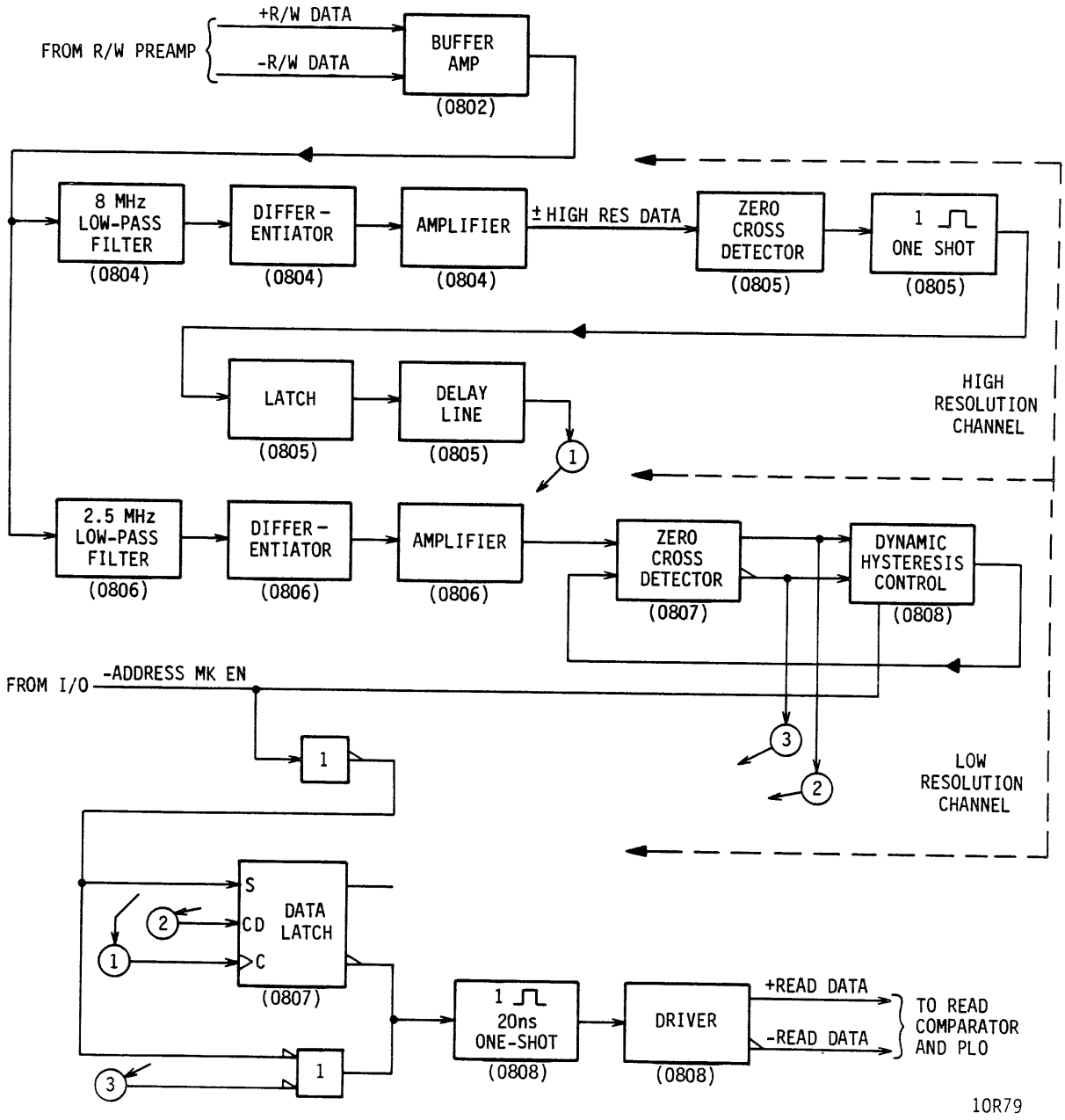


Figure 1-59. Data Latch Block Diagram
(Two Board R/W)

The input signal is amplified by the Buffer Amp provided that -Write Enable is inactive (high). The ±Read Analog Data output from the Buffer Amp splits into two parallel signal paths, the high resolution channel and the low resolution channel. Each channel contains independent wave-shaping circuitry that prepares an input to the Data Latch FF. The high resolution channel supplies delayed clock pulses to the Data Latch FF, and the low resolution channel supplies a D-input to the Data Latch FF. Successive clock pulses toggle the FF when the D-input has changed. Each transition of the Data Latch FF triggers a 20 ns one-shot that pulses the ±Read Data output lines once for each written flux transition sensed by the data head.

Splitting the analog data signal into two paths and combining the high and low resolution channels in the Data Latch FF is a system that discriminates against high frequency noise components in the Read Analog Data but maintains the timing of the data transitions. The low resolution channel uses a low-pass filter (rolling off at 2.5 MHz) followed by a zero-cross detector to develop a digital waveform similar to the Write Data waveform used in recording. However, filtering out the high frequency components of the input signal lowers the timing resolution of the channel's output signal. The high resolution channel uses a low-pass filter (rolling off at 8 MHz) followed by a zero-cross detector and a delayed pulse-forming circuit. With its wider bandwidth, this channel closely follows the timing present at its input. Each change in the low resolution signal is clocked into the Data Latch FF by a delayed clock pulse from the high resolution channel. Erroneous clock pulses from the high resolution channel do not toggle the Data Latch FF because they do not follow a change in the FF's D-input.

The Data Latch circuitry switches into a different operating mode during an address mark search. In an address mark search, the pulses on the ±Read Data output lines cease when the head is passing over an address mark, which is a previously erased segment of the track. An address mark search is initiated when -Address Mark Enable goes active (low), which happens when the controller issues Control Select (Tag 3) with Bus bits 1 and 5 active. This holds the Data Latch FF set and uses the output of the low resolution channel to trigger the 20 ns one-shot that pulses the ±Read Data output lines. The low resolution signal is sufficient for an address mark search because the read signal is not being demodulated. To regulate operation of the zero-cross detector in the low resolution channel and to prevent unwanted output pulses during an address mark, the dynamic hysteresis control circuit adjusts the switching thresholds of the zero-cross detector. In this way, noise pulses arising during the address mark are prevented from producing transitions in the low resolution signal.

The ±Latched Data from the Data Latch circuitry is sent to the Read Comparator - Address Mark ECL Logic Array.

Read Comparator and PLO

The Read Comparator and PLO circuitry uses a phase-locked loop to generate the 19.34 MHz Read Clock, and processes latched read data from the Data Latch circuit to develop clocked read data. Data Strobe commands from the controller condition the timing of clocked read data relative to the read clock to provide a means of error recovery to the read circuitry.

Figure 1-60 is a simplified block diagram of the Read Comparator and PLO circuitry. The phase-locked loop uses the Read Oscillator Control portion of the Read Comparator - Address Mark ECL Logic Array to regulate operation of the Current Pump and to provide stop/start control of the Voltage-Controlled Oscillator (VCO). The Current Pump supplies a Control Voltage signal to the VCO that determines the frequency of the 2F RD OSC signal output from the VCO. The 2F RD OSC signal is fed back to the Read Oscillator Control to complete the loop.

The phase-locked loop locks the VCO frequency to one of two reference signals. When the drive is reading data (-Read Gate and AME low), the phase-locked loop uses the pulse train on the Latched Read Data line as a timing reference. In this case, the Read Oscillator Control uses a quadrature comparator to drive the Pump Up and Pump Down lines as necessary to keep the rising edges of the 2F RD OSC signal coincident with the rising edges of +Latched RD Data pulses. For each Latched RD Data pulse, the quadrature comparator outputs a variable-length pulse on the Pump Up line, followed by a fixed-length pulse on the Pump Down line. When the Pump Up and Pump Down pulses differ in length, the Control Voltage to the VCO varies accordingly to phase shift the VCO and bring it into phase lock.

When the drive is not reading data (-Read Gate high or AME high), the phase-locked loop maintains the VCO frequency close to the value it has during read operations. In this mode, a coincidence comparator in the ECL Logic Array monitors the phase difference between the 4.83 MHz WRT OSC signal (derived from the Write PLO) and the 2F RD OSC signal fed back from the VCO. When the rising edge of the 4.83 MHz signal leads the rising edge of the 2F signal, this comparator pulses the Pump Up line to increase the Read VCO frequency. Conversely, when the rising edge of the 4.83 MHz signal lags the rising edge of the 2F signal, this comparator pulses the Pump Down line to decrease the Read VCO frequency.

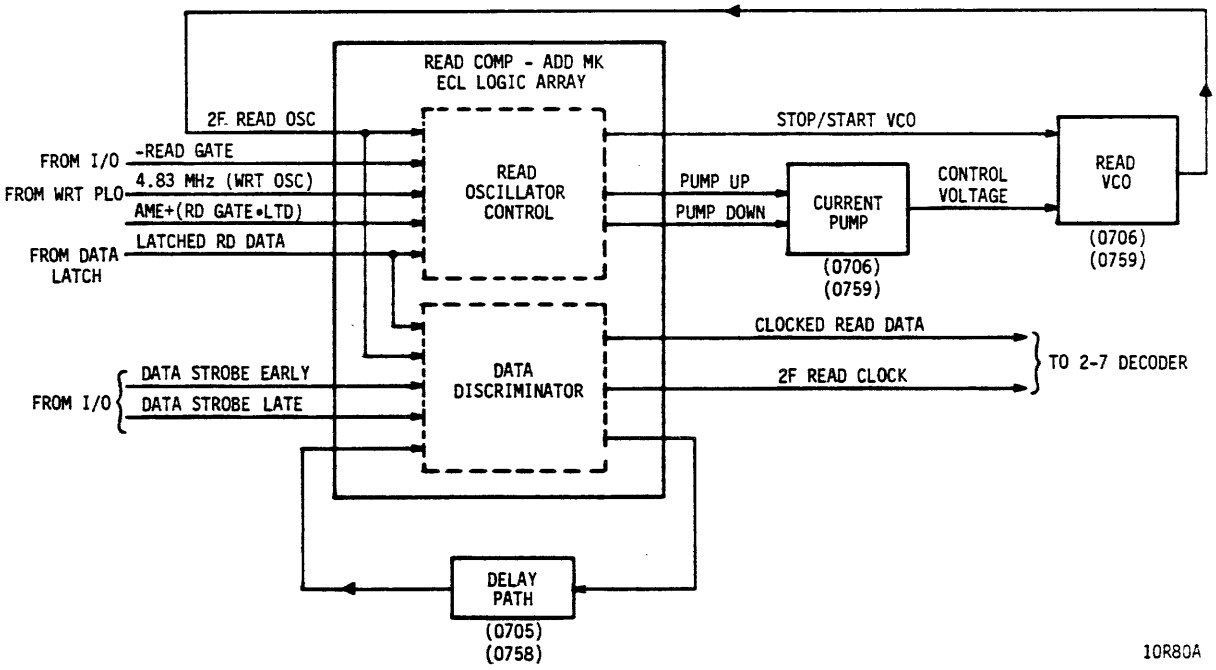


Figure 1-60. Read Comparator and PLO Block Diagram

The Read Oscillator Control circuitry uses the Stop/Start VCO line to control VCO operation while switching between the quadrature and coincidence comparators. The Stop/Start VCO line goes active for approximately 200 ns after the Latched RD Data pulse following a change in the Read Gate signal. While the Stop/Start VCO line is active, the VCO is inhibited, and its control voltage is held constant. This enables the Read PLO to phase lock within 2 microseconds during the switching transitions.

The Data Discriminator portion of the Read Comparator - Address Mark ECL Logic Array conditions the 2F Read Clock and Clocked Read Data signals for use in the 2-7 Decoder (see figure 1-60). With nominal timing, pulses on the Clocked Read Data line are active for one 2F bit cell (51 ns), and positive transitions of the 2F Read Clock coincide with the center of Clocked Read Data pulses. For error recovery, the controller can issue a Data Strobe Early or a Data Strobe Late command to shift this timing either way from its nominal value. The controller commands Data Strobe Early by issuing Tag 3 (Control Select) with Bus bit 7 active. The Data Discriminator responds by routing the clock signal through a 2.9 ns delay path. This

process delays the 2F Read Clock relative to the Clocked Read Data pulses. The controller commands Data Strobe Late by issuing Tag 3 with Bus bit 8 active. The Data Discriminator responds by routing the data signal through a 2.9 ns delay path. This process delays the Clocked Read Data pulses relative to the 2F Read Clock.

The Clocked Read Data and 2F Read Clock signal are input to the 2-7 Decoder, which converts the read data from 2-7 code into NRZ form and generates the 9.67 MHz Read Clock.

2-7 Decoder

The 2-7 Decoder converts 2-7 data into NRZ data and generates the 9.67 MHz Read Clock from the 19.34 MHz Read Clock. Both inputs, the 2-7 data and the 19.34 MHz Read Clock, come from the Read Comparator and PLO circuitry.

As described under Basic Read/Write Principles, there is a one-to-one correspondence between seven 2-7 code words and seven NRZ code words. The decoder recognizes the coding in the 2-7 read data input as a succession of the seven 2-7 words, and outputs a series of NRZ code words, each one translated from its 2-7 equivalent. Table 1-4, presented under Basic Read/Write Principles, shows the translation used between the two groups of seven code words. The 2-7 decoding function takes place within a single ECL Logic Array, the 2-7 Encode/Decode chip.

Figure 1-61 is a simplified block diagram of the 2-7 Decoder. The decoder synchronizes after the +Lock to Data input goes inactive (low). This occurs 2 microseconds after Read Gate goes active unless an address mark search is in progress. If an address mark search is in progress, +Lock to Data goes inactive 2 microseconds after Address Mark Enable goes inactive, provided that Read Gate stays active. Once +Lock to Data goes inactive, synchronization occurs when the 2-7 input data contains three or more binary zeros followed by a binary one. This binary one sets up the proper phase of the 9.67 MHz Read Clock relative to the NRZ Data output line and initiates the decoding process. The clock and decoding operations are discussed in the following paragraphs.

The 9.67 MHz Read Clock is generated from the 19.34 MHz Read Clock as this signal clocks a divide-by-two FF. The Q-output of the FF is inverted and supplied to the D-input through a gate that is enabled as a result of synchronization. Synchronization selects which positive edge of the 19.34 MHz Read Clock determines the positive edge of the 9.67 MHz Clock.

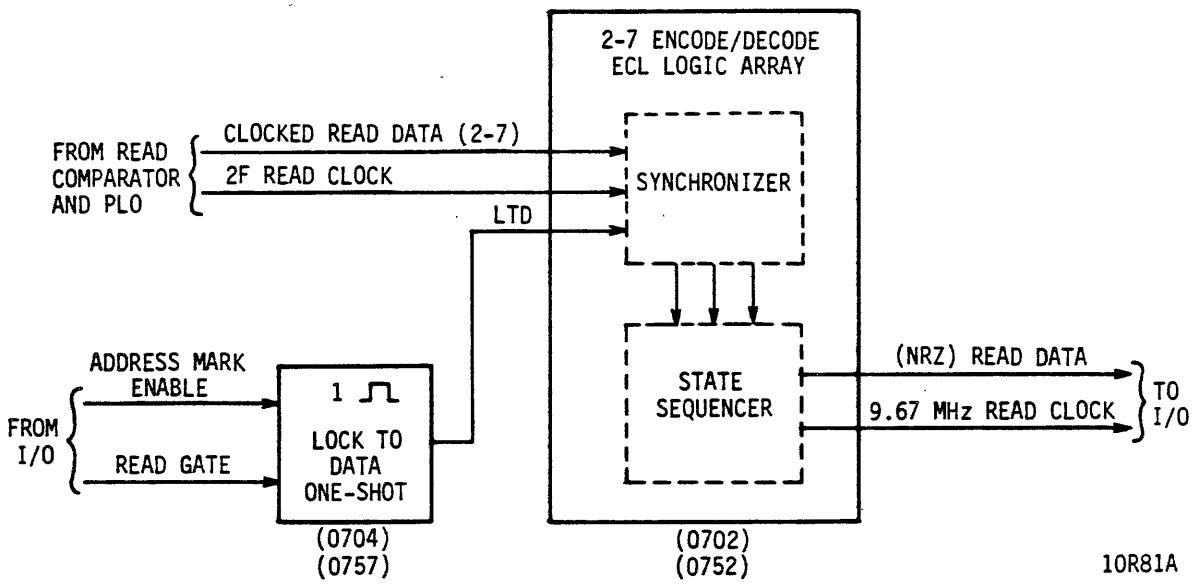


Figure 1-61. 2-7 Decoder Block Diagram

The decoding function is performed by a state sequencer. The state sequencer has eight FFs, and each of the eight states corresponds to one of the FFs being set. It operates by shifting states on each falling edge of the 9.67 MHz Read Clock. Thus, the interval for each state is one NRZ bit cell (103 ns). Two factors determine the current state of the sequencer. These are the previous state and the binary values of the last two 2-7 data bits input to the circuit. Therefore, at any time the state of the sequencer reflects the recent decoder inputs. The binary level decoded on the NRZ Data lines is state-dependent. During two of the states (NRZ bit cells), the output is binary zero, and during the other states, the output is binary one. In summary, the way the sequencer maps one state into the next state implements the specified translation from 2-7 data words into NRZ data words.

The decoder output stays low until synchronization occurs, and there is a processing delay of four 2-7 bit cells within the decoder.

The decoder sends the $\pm$NRZ Read Data and $\pm$Read Clock outputs to the I/O board to be transmitted on the interface to the controller.

Address Mark Detection

The Address Mark Detector, which is part of the Read Comparator - Address Mark ECL Logic Array, monitors the Latched RD Data signal from the Data Latch board during an address mark search. If a gap of 2.1 to 3.6 microseconds is detected between incoming read pulses, the detector sets the Address Mark Found line, and the I/O circuitry sets the Address Mark line on the interface.

Figure 1-62 shows the input and output signals for the Address Mark Detector. An address mark search occurs when the controller issues Tag 3 (Control Select) with Bus bits 1 and 5 active. In this situation, the -Read Gate line is low and the AME line is high. Together, these two signal inputs enable the Address Mark Detector.

The detector contains a counter circuit which is driven by the 9.67 MHz Clock signal from the Write PLO until it is reset by incoming read pulses. If the counter is clocked up over an interval from 20 to 36 clock periods, the Address Mark Found line is set. This line remains set until the lock-to-data interval ends (2 microseconds after Address Mark Enable is cleared) or until -Read Gate goes high.

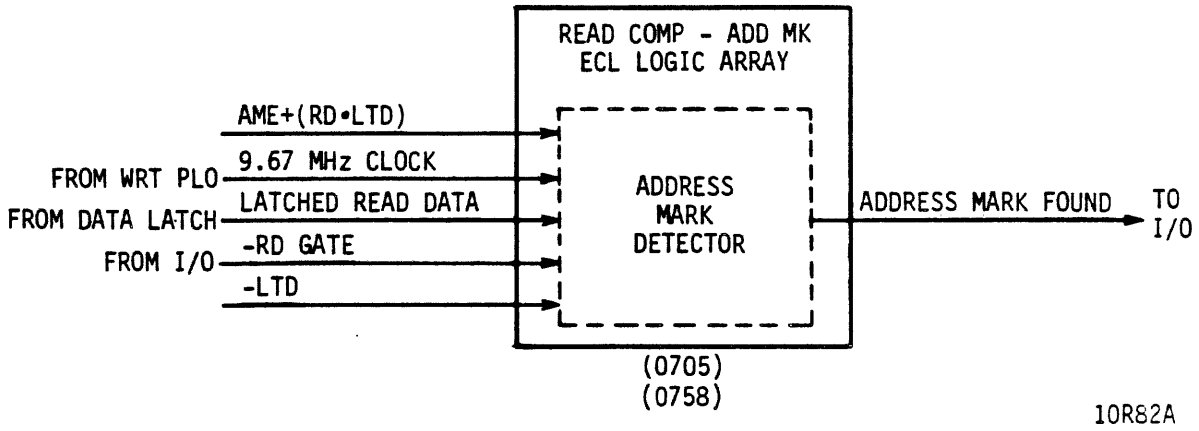


Figure 1-62. Address Mark Detector Block Diagram

The detector also contains a discriminator that distinguishes between read data gaps, caused by media defects, and gaps indicating address marks. If a defect is crossed, the discriminator inhibits the Address Mark Found output.

FAULT AND ERROR CONDITIONS

GENERAL

The following paragraphs describe those conditions which are interpreted by the drive as errors. These errors are divided into two categories: (1) those that generate the Fault signal and (2) those that do not generate the Fault signal. Included in the following descriptions are a list of conditions that produce each error status, the effect of that status on drive operation, and actions that clear the status indication to return the drive to normal operation.

ERRORS INDICATED BY FAULT SIGNAL

General

The drive has monitoring circuitry that recognizes five types of error conditions. When any of these error conditions occurs, it sets the respective latch in the I/O Gate Array. An OR circuit in the gate array receives inputs from the five latches; if one or more of the latches is set, the OR circuit activates the Fault line. The Fault line remains active until the latches are cleared.

When the Fault line goes active, it lights the FAULT indicator on the operator panel, disables write operations, and issues Fault and Write Protected status to the controller. The active Fault line interrupts the MPU at PIA-0 (see figure 1-63). The MPU responds by dropping the Ready signal and by communicating with the I/O Gate Array to identify the fault. The Unit Ready line to the controller goes inactive, and the READY indicator on the operator panel flashes until the fault is cleared.

Communication between the MPU and the I/O Gate Array takes place via I/O Control lines 1-3. Upon receiving the Fault interrupt, the MPU pulses I/O Control lines 1 and 2 to operate a multiplexer inside the gate array. The multiplexer's inputs include the five fault latches inside the gate array, and its output is carried to PIA-0 by the I/O Control 3 line. There are five individual fault LEDs on the Control board, each corresponding to a fault latch in the gate array. Having read the status of the latches, the MPU lights the corresponding LED(s) via outputs of PIA-2.

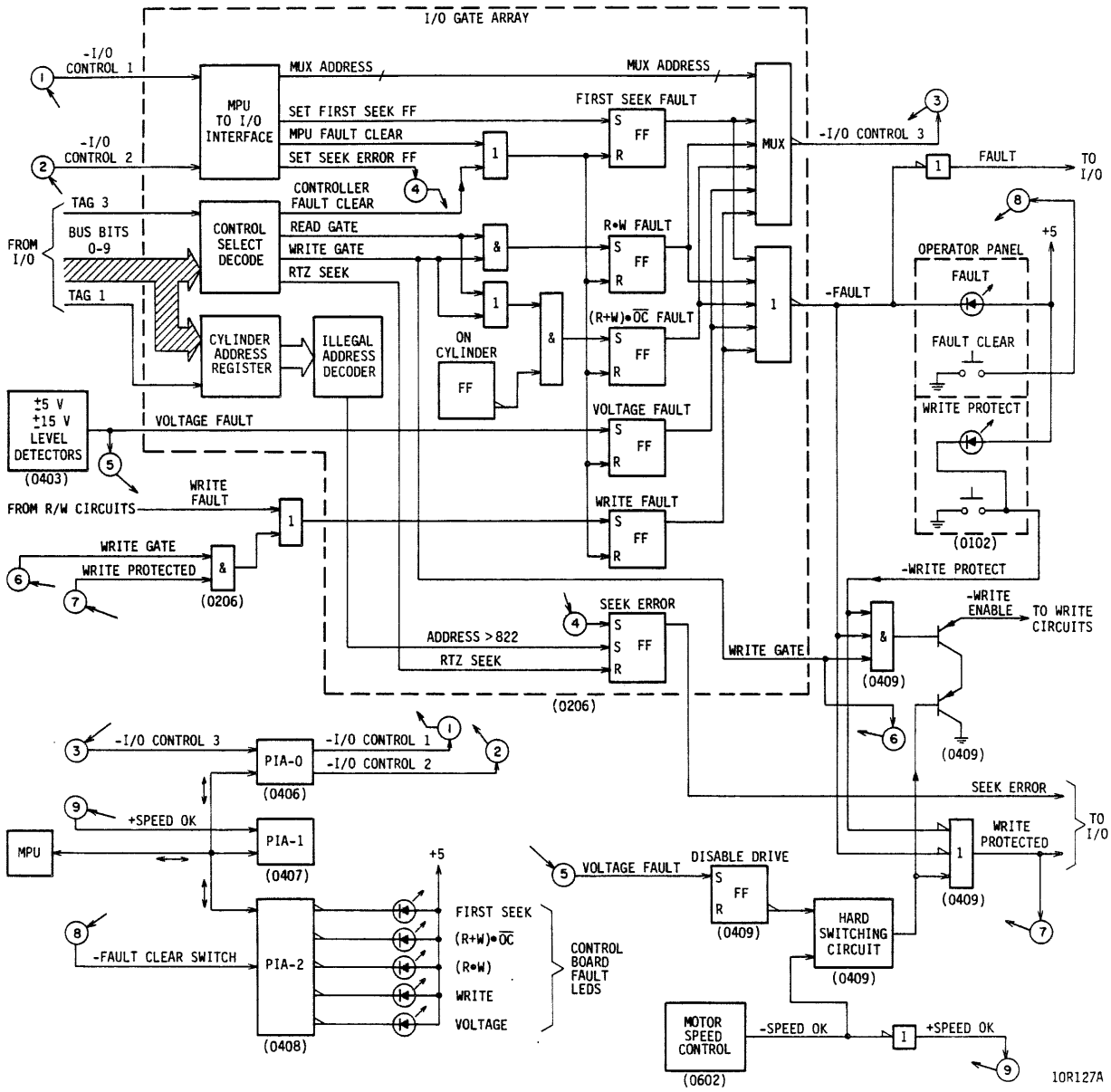


Figure 1-63. Fault and Error Detection Circuitry

Provided the error condition or conditions no longer exist, the Fault signal is cleared by the following:

- Controller Fault Clear command (Tag 3 with Bus bit 4)
- Fault Clear switch on operator panel
- Powering down the drive

The controller Fault Clear command is decoded inside the I/O Gate Array to develop a reset input for the five latches. When the Fault Clear switch is pressed, it interrupts the MPU at PIA-2. The MPU responds by pulsing the I/O Control 1 and 2 lines with a code that develops a reset input for the five latches. In either case, the reset input will clear a latch only if it is no longer being set by the error condition. In the process of removing and reapplying power to the drive, the fault circuitry is initialized as part of the power sequence, and any pre-existing fault status is lost.

The following paragraphs describe the individual fault conditions which set each of the latches in the I/O Gate Array and thus activate the Fault signal.

Voltage Fault

This fault is generated whenever the $\pm$15 or $\pm$5 voltages are detected to be below satisfactory operating levels. Threshold detectors on the Control board activate the Voltage Fault line if any of the following voltages drop:

- The +15 V supply drops to 14.35 V.
- The +5 V supply drops to 4.83 V.
- The -5 V supply drops to -4.90 V.
- The -15 V supply drops to -14.46 V.

When the -Voltage Fault line goes low, it sets the individual fault latch in the I/O Gate Array and sets the Disable Drive FF in the interlocks circuitry on the Control board. Setting the Disable Drive FF adds an additional degree of write protection, needed to safeguard existing data on the disks by inhibiting the write circuitry while a voltage problem exists. A hard switching circuit deactivates the -Write Enable line when the Disable Drive FF is set and keeps it inactive for about 1/2 second after the Disable Drive FF is cleared. This supplements the write protection normally invoked when the Fault line is active or when the drive is placed in the Write Protect mode.

Another result occurring with voltage faults (but not with the other four faults) is that the MPU sets the Seek Error FF to disable the servo system (see Errors not Indicated by Fault Signal).

An additional voltage detector circuit detects when the +5 V supply drops to 4.73 V, making MPU operation unreliable. This condition generates a -Low Vcc signal to produce the Reset signal for the MPU chips and the DC Master Clear signal for the gate arrays.

Read or Write and Off Cylinder

This fault is generated if the drive is in an off cylinder condition and it receives a Read or Write gate from the controller. The I/O Gate Array decodes both gates from Tag 3 commands and contains the On Cylinder FF. When the On Cylinder FF is cleared and either gate goes active, logic in the gate array sets the associated fault latch.

Write Fault

A write fault is encoded if any of the following conditions exist:

- Write Gate received while drive is in Write Protected mode
- No Write Current input to the write driver when Write Enable is active
- No write data transitions when the Write Gate is active (except when the Address Mark Enable signal is active)
- Head open (bad head detected)
- An invalid head address received (other than heads 0-9)

When the controller selects an illegal head, an error is not detected until the controller attempts to write with that head. Since no head has been selected, there will be no Write Current to the write driver and the Write Fault will be encoded.

All conditions except the first one, which is detected on the I/O board, activate the Unsafe line coming from the LSI chips in the R/W Preamp. Gating circuitry develops the Write Fault signal from the Unsafe signal provided that Write Enable is active and Address Mark Enable is inactive. The gating circuitry keeps the Write Fault line inactive during transitions between read and write operation; at these times, the Unsafe line may contain pulses in normal operation. The Write Fault line or the

combination of Write Protect and Write Gate lines active sets the associated latch in the I/O Gate Array.

Read and Write Fault

This fault is generated whenever the drive receives a Read Gate and a Write Gate simultaneously. This condition is detected internally in the I/O Gate Array to set the associated latch.

First Seek Fault

First Seek fault, as opposed to Seek Error, results from error conditions that occur during power on initialization and the load operation. Seek Error, on the other hand, indicates error conditions that occur during normal seeks and RTZ seeks. First Seek faults generate an active Fault signal while Seek Errors activate the Seek Error and Seek End lines to the controller. Seek Errors are discussed in the next topic, and the error conditions that cause a First Seek fault are described in the following paragraphs.

Unlike the other individual fault latches, the latch for First Seek fault is set by the MPU. To set the latch, the MPU inputs the I/O Gate Array with a specific pulse code on I/O Control lines 1 and 2. The error conditions resulting in a First Seek fault are monitored by the MPU during the power on initialization and load operation. Assuming that the MPU is operational, it sets the associated latch in the I/O Gate Array if any of the following errors are detected:

- The Demodulator OK line goes inactive during the part of the load operation where the carriage rests over the data zone.
- The Speed OK line goes inactive during the load operation.
- The Fault line goes active during the load operation.
- The RTZ portion of the load operation requires more than one second for completion.
- The On Cylinder Sense signal drops out three or more times during settle-in of the load operation.

The MPU aborts the load operation when a First Seek fault is indicated. Although a controller Fault Clear command will reset the Fault signal, the MPU waits until the operator panel Fault Clear switch is pressed before attempting another load.

ERRORS NOT INDICATED BY FAULT SIGNAL

General

Two types of errors do not generate the Fault status -- seek errors and the motor speed error. The seek error has an associated status FF, while the motor speed error does not.

Motor Speed Error

The -Speed OK signal is developed by circuitry in the Motor Control Gate Array on the Motor Speed Control board. When the spindle speed falls below 3564 r/min, the -Speed OK signal goes high. The -Speed OK signal is used by several circuits on the Control board (see figure 1-63), and these uses are outlined in the following paragraphs.

An interlock circuit monitors the -Speed OK line to provide write protection if the line goes high. Write protection is needed to safeguard existing data on the disk by inhibiting the write circuitry while a motor speed error exists. A hard switching circuit deactivates the -Write Enable line when -Speed OK goes high and keeps it inactive for about 1/2 second after -Speed OK goes low again.

The MPU monitors the +Speed OK line at PIA-1 and commands an emergency retract operation when there is a loss of motor speed. This operation is discussed under Retract Control Circuitry (part of Seek Functions). In addition, when -Speed OK goes high, it activates the +Disable Drive line. When the +Disable Drive line goes high, it removes the servo input to the Power Amp Drive so that the retract control circuitry has total control of actuator movement.

The MPU has two methods for restoring motor speed when -Speed OK goes high. The MPU checks the +Motor Fault line at PIA-1. If +Motor Fault is active, the MPU drops and then issues the Motor Run command in order to reset the motor fault circuitry in the Motor Control Gate Array. If +Motor Fault is inactive, the MPU keeps the Motor Run command active and tries to bring the motor back up to speed. In either case, the MPU drops the Unit Ready signal to the controller during the low speed condition.

Seek Error

Seek Error is a status signal sent to the controller indicating error conditions that occur during normal seeks and RTZ seeks.

The Seek Error signal is active when the Seek Error FF, located in the I/O Gate Array, is set. This FF gets set if any of the following error conditions exist:

- The controller commands a cylinder select, specifying a cylinder address greater than 822.
- A Voltage Fault occurs.
- The time required for a normal seek exceeds the 65 ms timeout allowed by the MPU.
- The On Cylinder Sense signal goes inactive more than twice during settle-in (normal or RTZ seeks).
- Three or more guard band pulses are detected at PIA-1 during one seek. Inner and outer guard band pulses are counted in normal seeks. Only inner guard band pulses are counted during RTZ seeks.
- The MPU gets a reset input to force it out of a hang condition.

The MPU detects all conditions for Seek Error except the first one listed; for these, it sets the Seek Error FF using I/O Control lines 1 and 2 (see figure 1-63). The first condition is recognized by a decoder circuit connected to the Cylinder Address Register (CAR). The decoder output feeds a separate set input to the Seek Error FF. Detection of this condition is internal to the I/O Gate Array, which contains the CAR, the decoder, and the Seek Error FF.

A Seek Error status signal is generated to the controller via the I/O transmitters. The Seek Error signal is also input to the Sector Counter Gate Array (on the Control board) where it encodes a Seek End status signal to be sent to the controller.

In the event of a Seek Error, the MPU drops all servo commands, allowing the actuator to fall to the resting position over the data zone. The seek error condition cannot be cleared except by a controller RTZ command. An attempt by the controller to perform a read or write operation while the seek error condition exists will result in the generation of a Read or Write and Off Cylinder fault.

SECTION 2

GENERAL MAINTENANCE INFORMATION

GENERAL MAINTENANCE INFORMATION 2

INTRODUCTION

This section contains general information relating to maintenance of the drive. A person performing maintenance should be familiar with the information in this section in addition to being thoroughly familiar with drive operation. Information is divided into the following areas:

- Warnings and Precautions - Lists warnings and precautions that must be observed when working on the drive.
- Electrostatic Discharge Protection - Provides instructions for the proper handling of electrostatically sensitive devices.
- Maintenance Tools and Materials - Lists the tools and materials required to perform maintenance on the drive.
- Testing the Drive - Provides information concerning the electrical testing of the drive.
- Accessing Assemblies for Maintenance - Identifies the various parts of the drive and describes how to access these parts for maintenance.

WARNINGS AND PRECAUTIONS

WARNING

The following topic provides warnings and precautions that must be observed during maintenance. Refer also to Important Safety Information and Precautions located in the front of this manual following the table of contents. Failure to observe the warnings, precautions, and other safety information provided in this manual could result in personal injury.

Observe the following warnings and precautions at all times. Failure to do so may cause equipment damage and/or personal injury.

- Use only CDC/MPI replacement parts. Using non-CDC/MPI replacement parts can adversely affect safety. Using other manufacturers' parts could also degrade reliability, increase maintenance downtime, and void warranty coverage.

- Use care while working with the power supply because line voltages are present.

- Do not attempt to disassemble the module. It is not field repairable. Replace the entire module assembly if it is found to be defective.

- Do not operate the drive over an extended period of time without the top cover installed.

- Always deenergize drive before removing or installing circuit boards, cables, or any other electrical components.

- Observe the precautions listed under Electrostatic Discharge Protection.

- If the remote power supply is placed on a bench for testing, position the supply so that all ventilation holes are open to allow proper air flow to internal components.

ELECTROSTATIC DISCHARGE PROTECTION

All drive electronic assemblies are sensitive to static electricity, due to the electrostatically sensitive devices used within the drive circuitry. Although some of these devices such as metal-oxide semiconductors are extremely sensitive, all semiconductors as well as some resistors and capacitors may be damaged or degraded by exposure to static electricity.

Electrostatic damage to electronic devices may be caused by a direct discharge of a charged conductor, or by exposure to the static fields which surround charged objects. To avoid damage to drive electronic assemblies, service personnel must observe the following precautions when servicing the drive:

- Ground yourself to the drive - whenever the drive electronics are or will be exposed, connect yourself to ground with a wrist strap (see table 2-1). Connection may be made to any metal assembly or to the ground jack at the rear of the drive. As a general rule, remember that you, the drive, and the circuit boards must all be at ground potential to avoid potentially damaging static discharges.

TABLE 2-1. MAINTENANCE TOOLS AND MATERIALS

Description	Part Number
AJWN Servo Status Display Board	CDC 54058100
Brake Adjust Shim	CDC 15363045
Cable (for servo status display board)	
Used on older control board (10 Pin connector, J260)	CDC 81787000
Used on newer control board (20 Pin connector, J80)	CDC 45952100
Field Test Unit (TB216A)	CDC 82338800
Motor Removal Tool	CDC 83350262
Oscilloscope, Dual Trace	Tektronix 475A or equivalent
Scope Probe Tip (Hatchet type)	CDC 12212885
Shipping Damper Adjustment Tool (3 required)	CDC 83350447
Solenoid Wrench	CDC 83350362
Static Shielding Bags and Ground Wrist Straps	See Accessories in parts data (section 4 of hardware maintenance manual, volume 1)
Tester A Cable Adapter	CDC 92439600
Tester B Cable Adapter	CDC 92246300
Vibration Damper Adjustment Tool (4 required)	CDC 85246400
Volt/ohmmeter	Ballantine 345 or equivalent digital voltmeter
Wire Seating Tool (for power harness)	CDC 12263607

- Keep boards in conductive bags - when circuit boards are not installed in the drive, keep them in conductive static shielding bags (see table 2-1). These bags provide absolute protection from direct static discharge and from static fields surrounding charged objects. Remember that these bags are conductive and should not be placed where they might cause an electrical short circuit.

- Remove boards from bags only when you are grounded - all boards received from the factory are in static shielding bags, and should not be removed unless you are grounded.

- Turn off power to drive before removing or installing any circuit boards.

- Never use an ohmmeter on any circuit board.

MAINTENANCE TOOLS AND MATERIALS

The maintenance procedures described in this manual require the use of certain special tools, test equipment, and materials. These are listed in table 2-1 along with the appropriate CDC part number. Note that the list includes only special tools. It is assumed that the service person has normal maintenance tools.

Use of the items listed in table 2-1 is described in the procedures in which they are required. Additional information is provided on the _JWN servo status display board (see section 3, Trouble Analysis) and the field test unit (see Testing the Drive).

TESTING THE DRIVE

GENERAL

During testing and troubleshooting the drive is normally required to perform various operations such as reading and writing test data. Either a field test unit (FTU) or system software can be used to control the drive during these operations.

FIELD TEST UNIT

The TB216A is the FTU recommended for use with the drive (see table 2-1 for part number). The TB216A allows the drive to be operated and controlled independent of the rest of the system.

There are two methods for connecting the FTU to the drive. Connections may be made either to the drive I/O plate or to the drive I/O board. Connecting to the drive I/O board requires adapter cables listed in table 2-1, and is possible only on drives which have I/O boards with detachable I/O cables. When connecting to the drive I/O board, the other drives in a daisy chain system may remain under system control.

See the FTU manual for additional instructions on connecting and operating the FTU.

Connecting FTU To Drive I/O Plate

CAUTION

To avoid possible damage to interface circuitry, always remove ac power from drive, controller, and FTU before removing or installing I/O cables.

During testing, the FTU I/O cables are connected to the drive in place of the system I/O cables. Before disconnecting the system I/O cables, disable the controller and set power supply circuit breaker CB1 to the OFF position. In a daisy chain system, power off all the drives.

When the drive is powered down, remove the system I/O cables from the drive to be tested. Connect the FTU A cable to drive connector J3 and the FTU B cable to drive connector J2. Connect a terminator to drive connector J4. See Accessories table in the parts data section of hardware maintenance manual, volume 1 for the terminator part number. In a daisy chain system, make whatever connections are necessary to ensure that the other drives remain under system control, and restore power to the other drives.

At the completion of testing, restore the drive to normal operation by reversing the process outlined above.

Connecting FTU To Drive I/O Board

CAUTION

To avoid possible damage to interface circuitry, always remove ac power from drive and FTU before removing or installing I/O cables.

During testing, the FTU I/O cables are connected to the I/O board in place of existing internal I/O cables. Before disconnecting cables from the I/O board, set drive power supply circuit breaker CB1 to the OFF position.

When the drive is powered down, disconnect the I/O cables from the I/O board of the drive to be tested. Connect A and B adapter cables (see table 2-1 for part numbers) to I/O board. Connect FTU A and B cables to A and B adapter cables. Connect a terminator to remaining connector on A adapter cable. See Accessories table in the parts data section of hardware maintenance manual, volume 1 for the terminator part number.

At the completion of testing, restore the drive to normal operation by reversing the process outlined above.

SYSTEM SOFTWARE

The drive may also be tested by use of diagnostic test programs. This requires use of the controller and the appropriate software. In this type of testing, the drive communicates with the controller as in normal online operations, and special I/O connections are unnecessary.

Refer to manuals or other documentation applicable to the specific system or subsystem for information concerning the system software routines.

IDENTIFYING TEST POINTS

The drive circuit boards have test points to aid in signal tracing during maintenance and troubleshooting. These test points appear, physically, as shown on figure 2-1 and may be located anywhere on the component side of the circuit boards. The logic diagrams show the test points schematically.

The diagrams and maintenance procedures identify a test point by referring to the coordinate locator code and in some cases letter designator. TP-G620 (B) is an example of a test point reference. Here, G620 is the component locator and "B" is the letter designator. The coordinate locator code indicates where the test point is located on the board. The introduction to diagrams section explains how to use the coordinate locators. The letter designators are letters, silkscreened onto the board, that progress in alphabetical order from left to right and top to bottom (see figure 2-2). Not all test points have letter designators. In the procedures, the letter designator is always in parentheses, following the locator code.

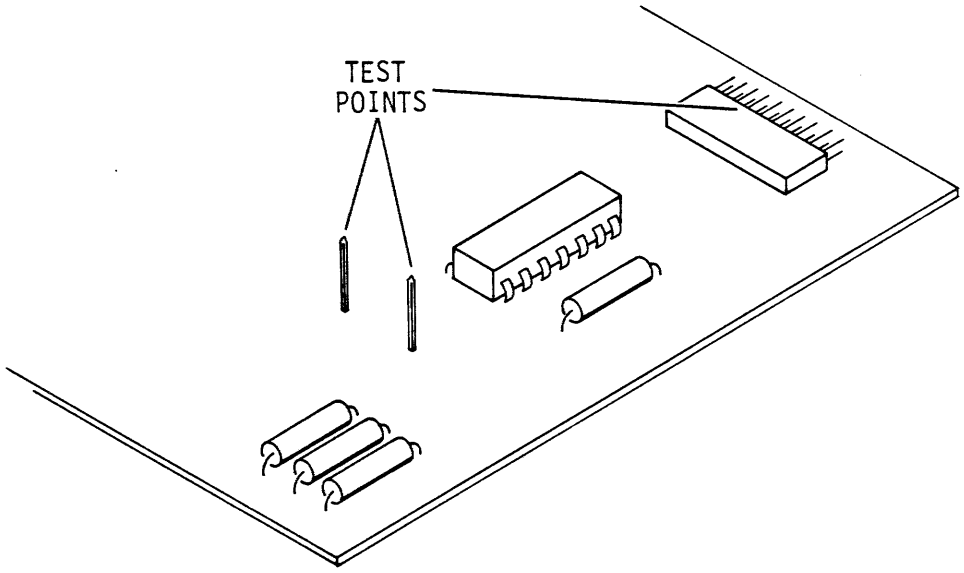


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Figure 2-1. Test Points

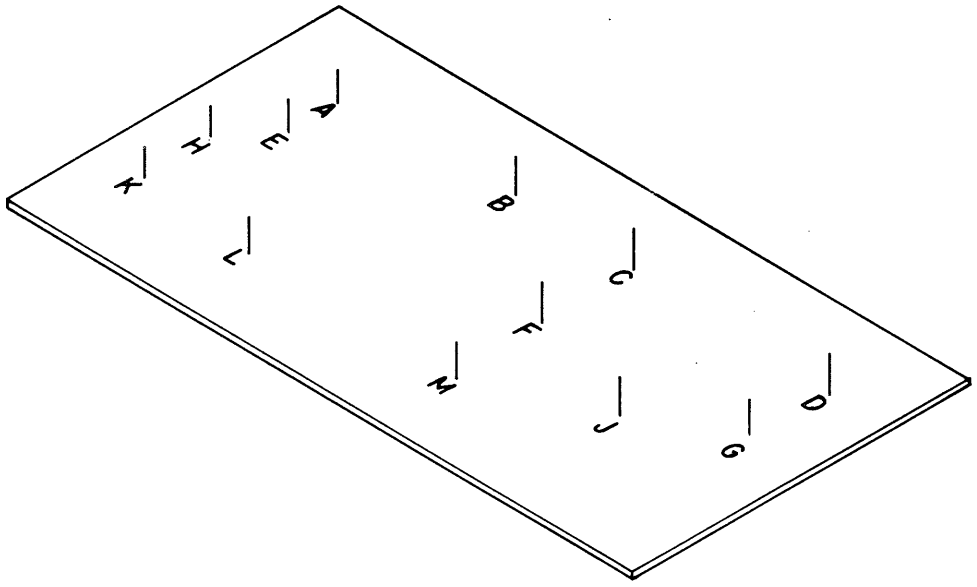

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Figure 2-2. Test Point Letter Designators

ACCESSING ASSEMBLIES FOR MAINTENANCE

The major drive assemblies and components are shown on figure 2-3. These parts are accessed by extending the drive on its slides and removing the top cover.

Extend the drive by using a screwdriver or similar tool to lift the cabinet latch (see figure 2-3), and pulling the drive forward. When extending the drive, exercise caution to ensure that the equipment rack remains stable. Also, take care that the system cabling is not damaged when sliding the drive in and out of the rack.

If it is necessary to remove the drive from the slides, see entire drive removal procedure in section 5 of this manual. Section 5 also contains a top cover removal procedure and procedures for removing most of the other field replaceable parts, including the circuit boards.

Extending the drive and removing the top cover allows access to most circuit board test points. Note that figure 2-3 shows both the one board and two board read/write. As shown on figure 2-3, the _EBN/_EDN, _PGX (two board R/W) or _RUX (one board R/W), and _PXX boards are readily accessible. The _PFX (two board R/W only) is reached by raising the _PGX, which is hinge mounted, to the upright position. The _PMX board is mounted between slide rails at the rear of the drive and slides out for maintenance when the attaching cables are removed. The _QHX board is attached to and slides out with the _PMX. Both the _EYN and _UBN are located within the module and cannot be serviced.

There are two types of power supplies available with the drive. One type is referred to as an integral power supply. The other type is referred to as a remote power supply (see figure 2-3). The integral power supply is attached to the drive rear panel and shipping bracket (inner rail if drive is slide mounted). The remote power supply can be attached to the inner rail (directly behind the drive) or other remote location, provided clearance for proper air flow is available.

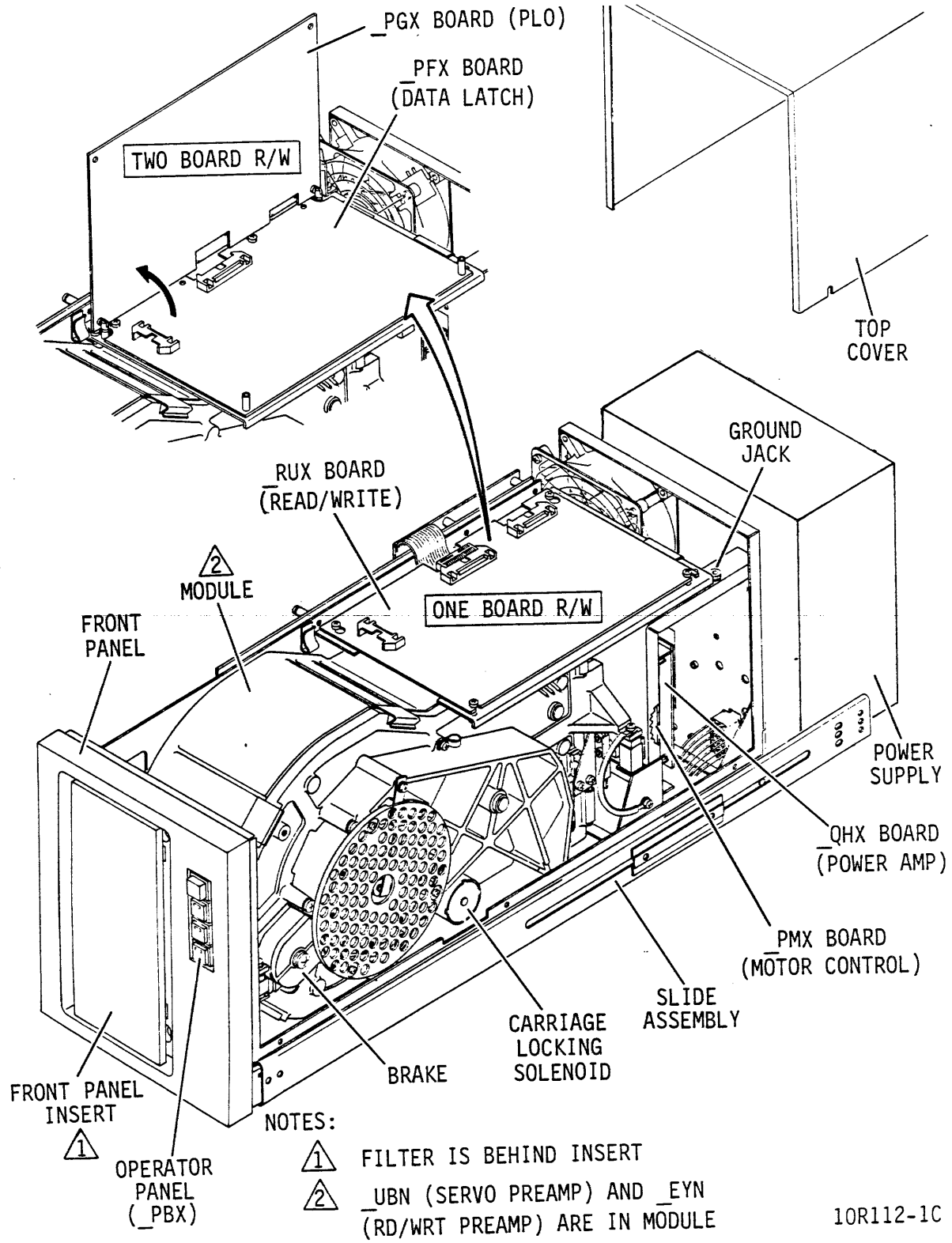

Figure 2-3. Component Locator (Sheet 1 of 8)

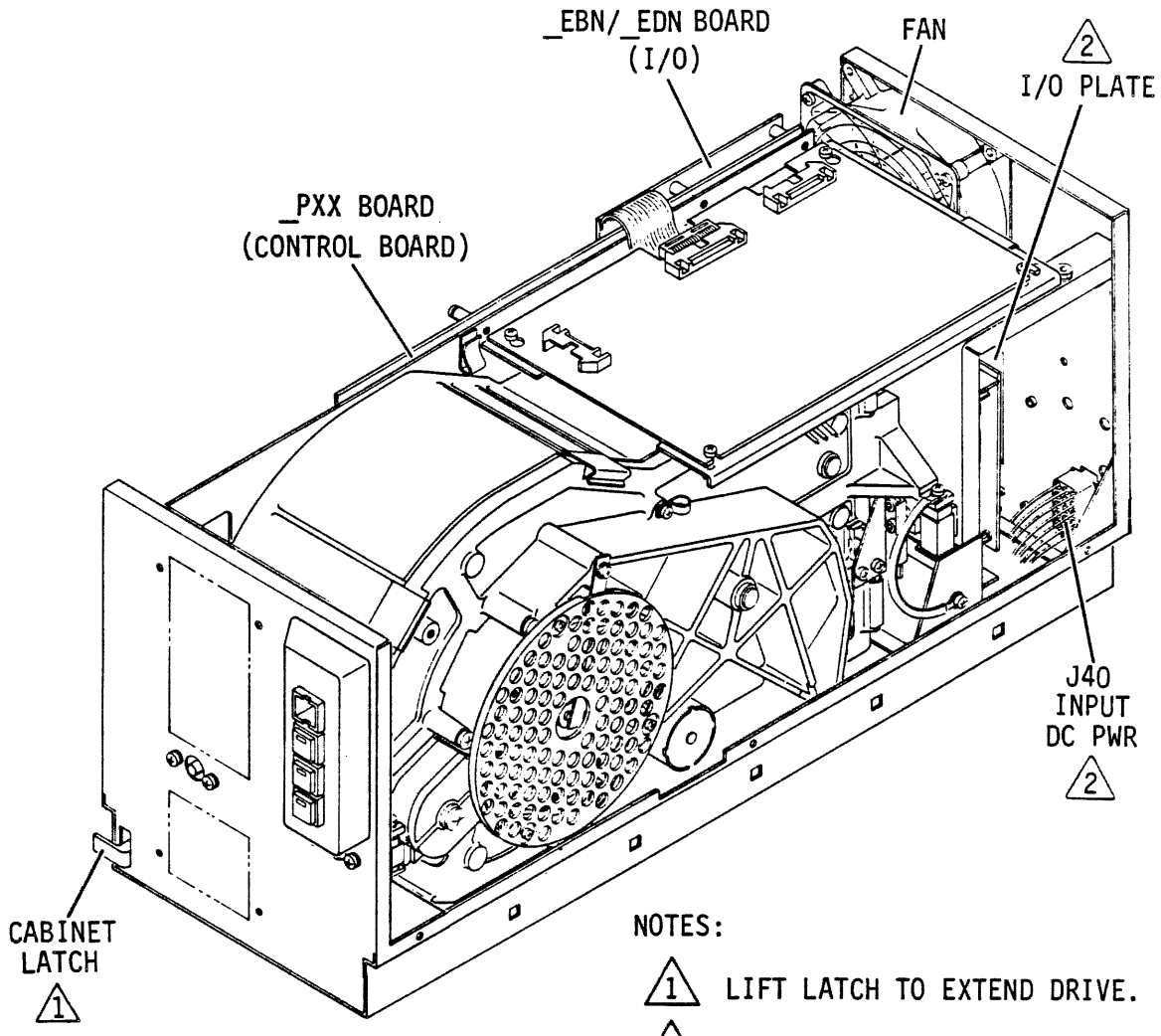

Figure 2-3. Component Locator (Sheet 2)

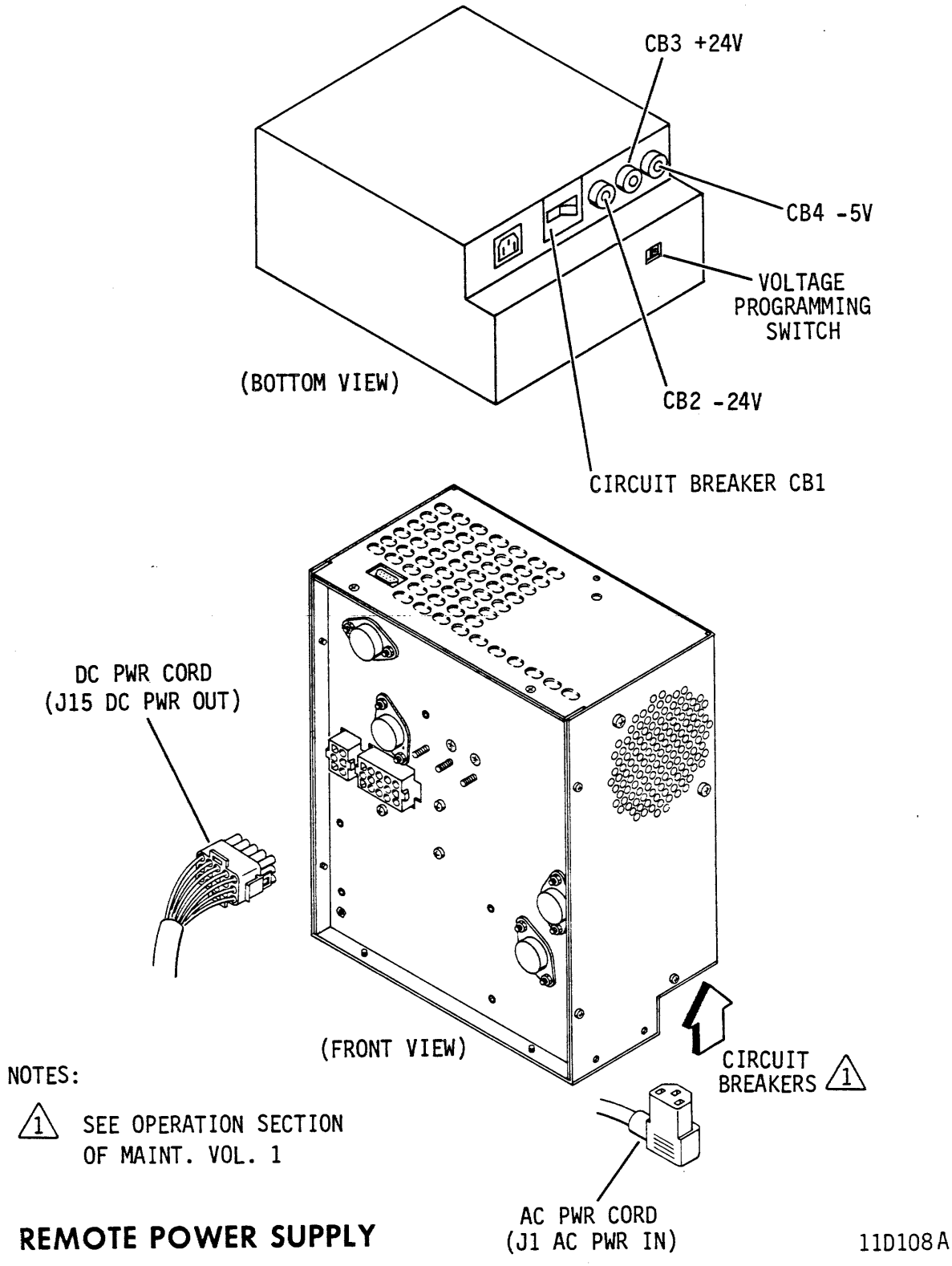

Figure 2-3. Component Locator (Sheet 3)

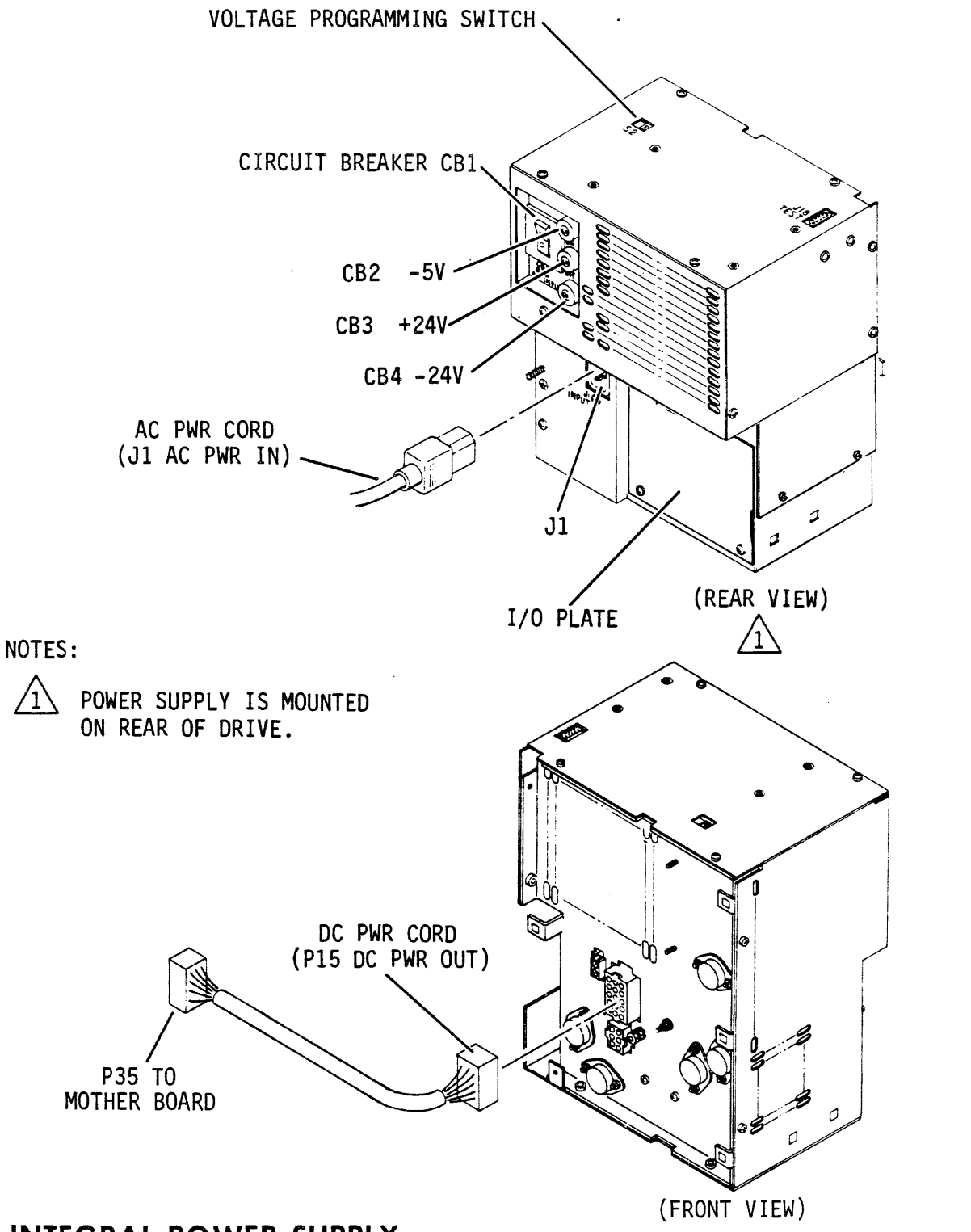

Figure 2-3. Component Locator (Sheet 4)

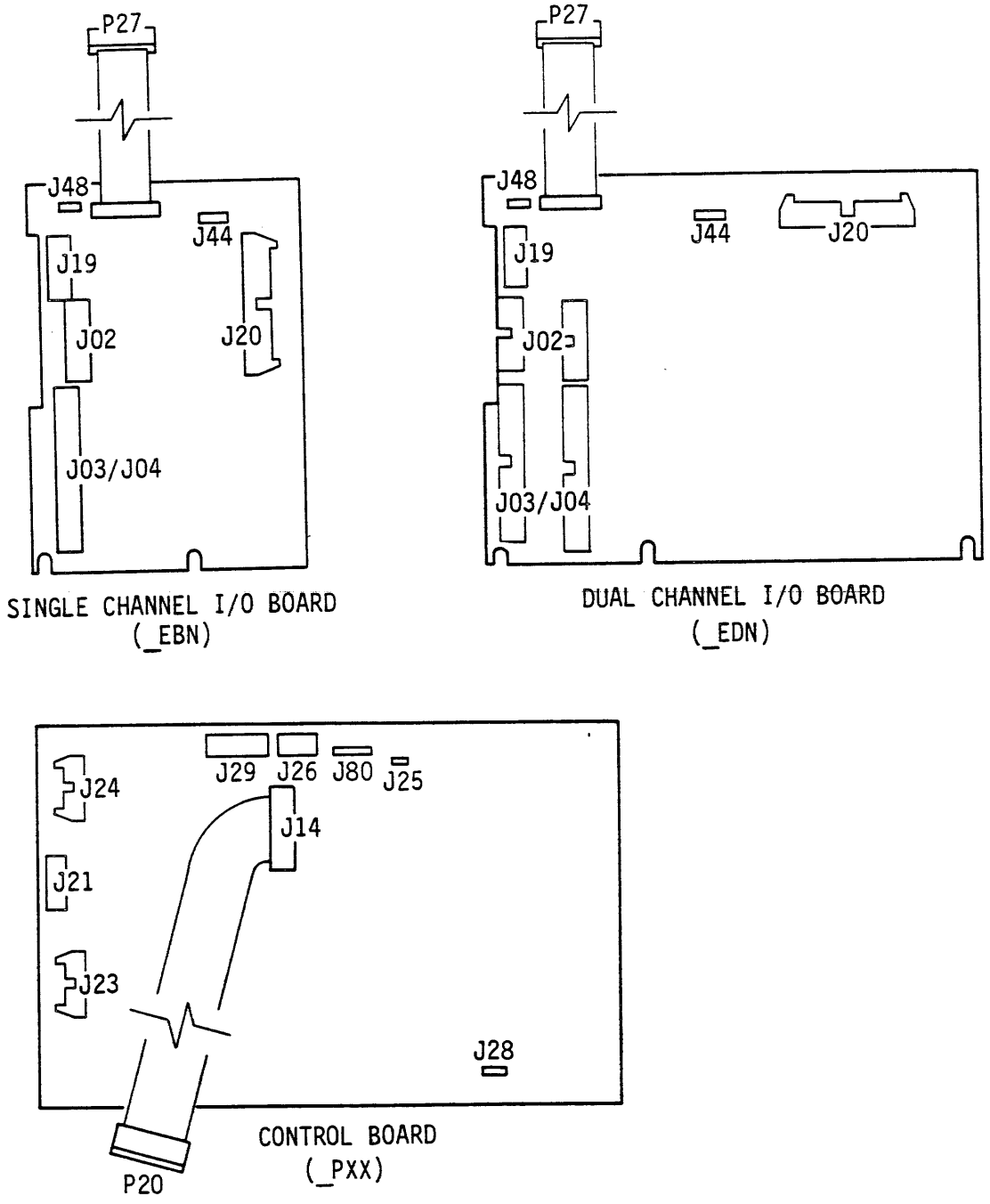

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Figure 2-3. Component Locator (Sheet 5)

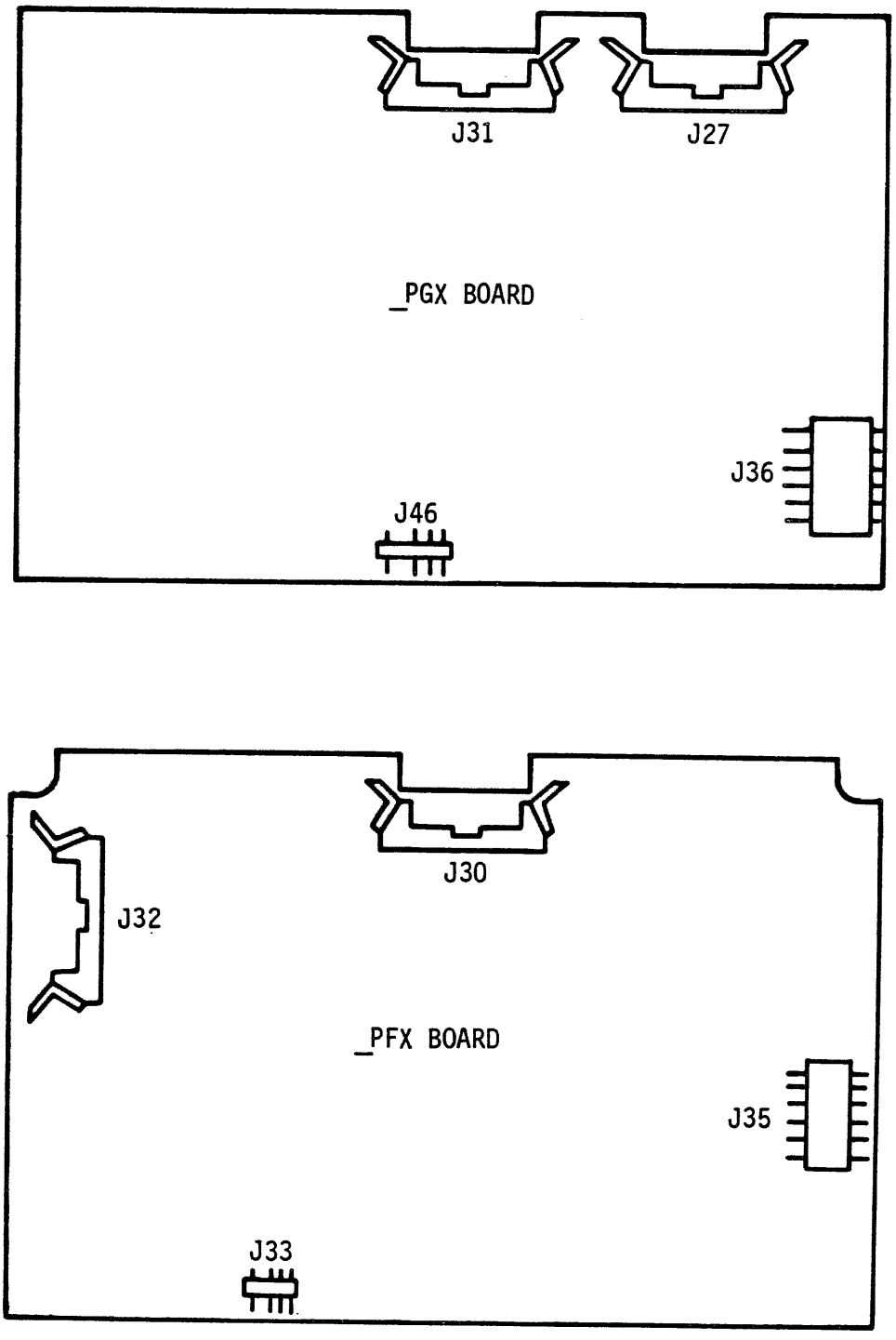


Figure 2-3. Component Locator (Sheet 6)

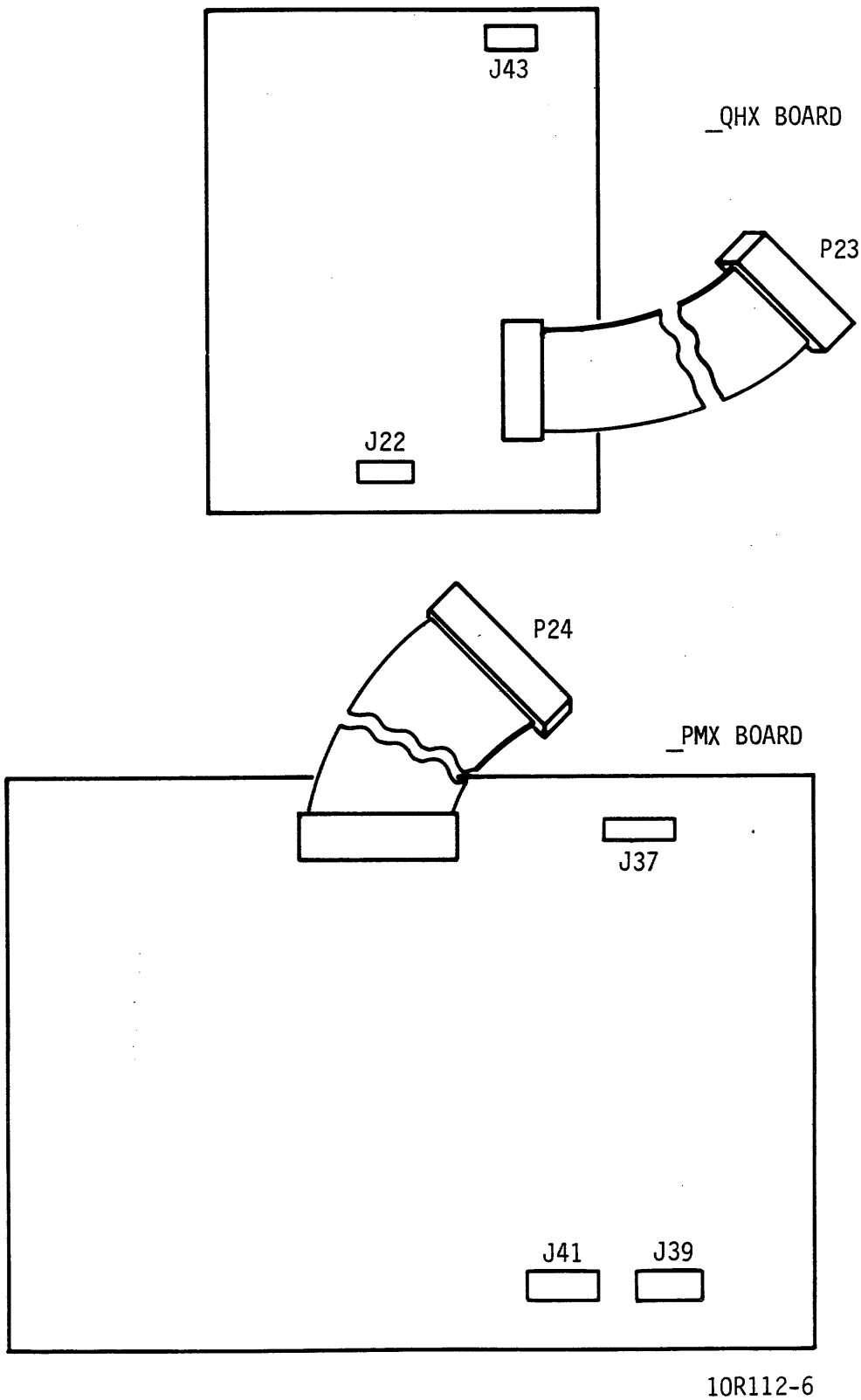


Figure 2-3. Component Locator (Sheet 7)

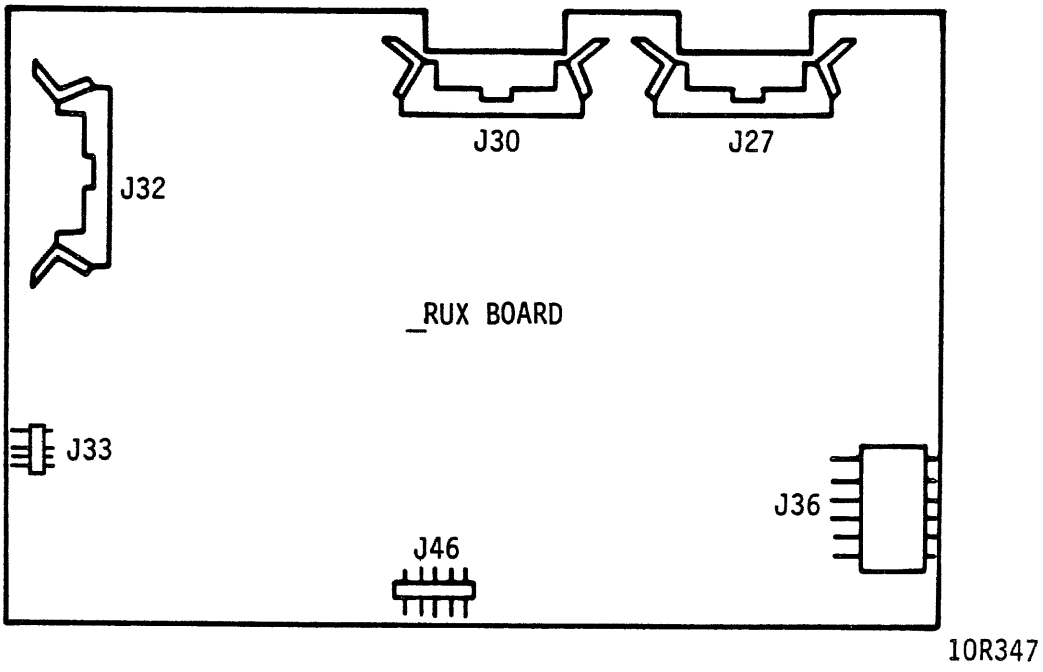


Figure 2-3. Component Locator (Sheet 8)

SECTION 3

TROUBLE ANALYSIS

TROUBLE ANALYSIS 3

CAUTION

When servicing the drive, observe all precautions listed under Electronics Discharge Protection in Section 2 of this manual. Failure to observe these precautions can result in serious damage to drive electronic assemblies.

INTRODUCTION

The trouble analysis section contains information on isolating and correcting problems causing improper drive operation. Persons performing troubleshooting should be thoroughly familiar with drive operation and with all information in the general maintenance section of this manual (particularly the warnings and precautions).

Because of the many types of malfunctions that may occur, the information in this section will not provide a solution to every problem. The intention, therefore, is to solve common problems and to provide a starting point for the rest. The final recommendation in all cases is to call field support.

Trouble analysis information is divided into two parts:

- Troubleshooting Procedures
- Servo Status Codes (not applicable to units with BPXX or CPXX boards)

The troubleshooting procedures describe how to isolate and correct common drive problems. The procedures cover all the major areas of drive operation: power, servo, read, and write. The servo status codes apply specifically to the servo system and describe the status codes presented by the MPU during servo operation. Probable causes and corrective actions are also included with the servo status code definitions.

Many of the corrective actions in this section refer to procedures given in Section 4, Electrical Checks, and Section 5, Repair and Replacement. All procedures are referred to by number. For example, a reference to procedure 4201 refers to 4201 - Tribit Check in section 4. The first digit always indicates the section (4 or 5) where the procedure is found.

TROUBLESHOOTING PROCEDURES

The troubleshooting procedures describe how to isolate and correct common drive problems. Figure 3-1 is an example of a troubleshooting procedure and explains the format. The following paragraphs explain how to use the troubleshooting procedures.

Before starting a procedure, ensure that all assumptions have been satisfied. The assumptions along with other advisory information are given in the introductory paragraph to the procedure and describe conditions that must exist for the procedure to be valid.

When the assumptions are satisfied, proceed to the first step of the procedure. After performing the action or answering the question, follow the line down to the next step. For a question, follow the line beneath the appropriate Y (yes) or N (no) response. Continue until a corrective action is reached.

After taking the first recommended action, retest the unit. If the test results do not change, try recommended action 2, and so on, being sure to retest after each action. The corrective actions which are easier to perform (checking a signal or changing a circuit board, for example) are listed before the more difficult tasks such as replacing the module. If the corrective actions do not solve the problem, call field support.

The procedures appear in the following order:

- TSP1 - Power Check: Provides an overall check of drive power.
- TSP2 - ±5 Volt Check: Shows how to isolate problems in the ±5 volt loads.
- TSP3 - ±24 Volt Load Check: Shows how to isolate problems in the ±24 volt loads.

- TSP4 - First Seek Check: Provides possible causes for the drive failing to successfully complete a first seek.
- TSP5 - Direct or RTZ Seek Check: Provides possible causes for the drive failing to successfully complete a direct or RTZ seek.
- TSP6 - Write Check: Provides information for isolating cause of write errors.
- TSP7 - Read Check: Provides information for isolating cause of read errors.
- TSP8 - Address Mark Check: Provides possible causes for read or write address mark problems.

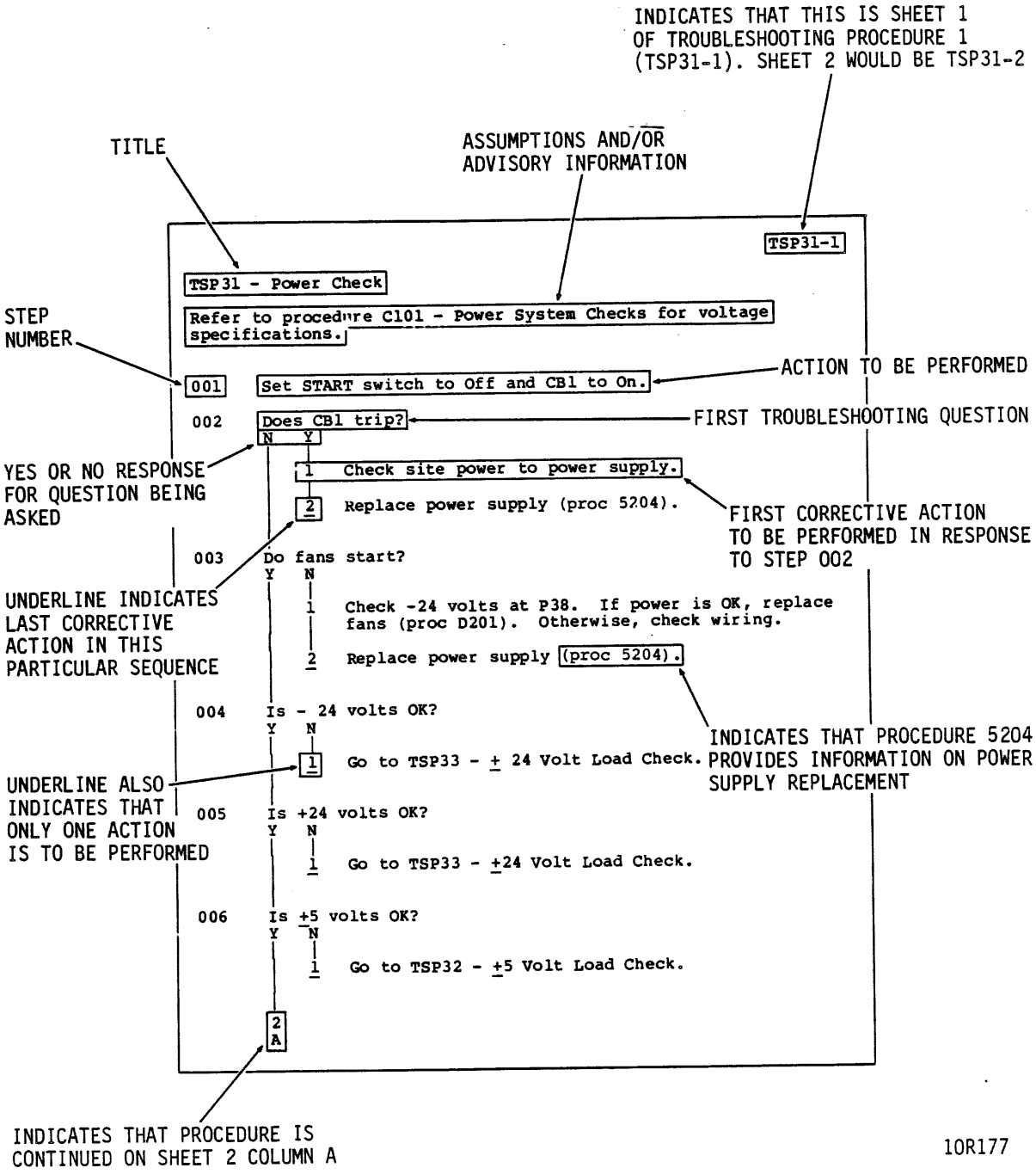


Figure 3-1. Example of Troubleshooting Procedure

TSP1 - Power Check

Refer to procedure 4101 - Power System Checks for voltage specifications.

001 Set START switch to Off and CB1 to On.

↓

002 Does CB1 trip?

N: ↓

Y:
↓
1 Check site power to power supply.
↓
2 Replace power supply (proc 5204).

003 Does fan start?

Y: ↓

N:
↓
1 Check -24 volts at P38 (fan) or P48 (_EBN/_EDN). If power is OK, replace fan (proc 5201). Otherwise, check wiring.
↓
2 Replace power supply (proc 5204).

004 Is - 24 volts OK?

Y: ↓

N:
↓
1 Go to TSP3 - ± 24 Volt Load Check.

005 Is +24 volts OK?

Y: ↓

N:
↓
1 Go to TSP3 - ±24 Volt Load Check.

006 Are ±5 volts OK?

Y: ↓

N:
↓
1 Go to TSP2 - ±5 Volt Load Check.

007 Is -8.3 volts OK?

Y: ↓
2
A

N: ↓
2
B

```
        A   B
        1   1
        |   |
        |   ↓
        |   1   Disconnect P28 (_PXX) and recheck -8.3 volts.  If
        |       -8.3 volts is OK, replace module (proc 5206).  If
        |       -8.3 volts is still abnormal, replace _PXX (proc
        |       5301).
        ↓
008     Is +40 volts OK?
        Y   N
        |   ↓
        |   1   Disconnect P37 (_PMX) and recheck.  If voltage is
        |   |   normal, replace _PMX (proc 5308).  Otherwise,
        |   |   proceed to next action.
        |   ↓
        |   2   Disconnect P22 (_QHX) and recheck.  If voltage is
        |       normal, replace _PDX (proc 5307).
        ↓
009     Power Check OK. If problem persists, call field support.
```

TSP2 - ±5 V Load Check .

This check isolates problems with ±5 volts. Refer to procedure 4101 - DC Power Check for voltage specifications.

001 Deenergize drive and check for short circuits between:

- +5 volts or -5 volts and ground.
- +5 volts and -5 volts.
- ±5 volts and ±24 volts.

↓

002 Do any short circuits exist?

N Y

↓

1 Remove loads (one at a time) to isolate short.

↓

2 Inspect wiring and boards.

↓

003 Remove all loads except _PXX (connector J21) from ±5 volts by disconnecting the following:

- _EYN (in module) at _RUX/_PFX connector J32
- _PMX at _PMX connector J37 and _PXX connector J24
- _PFX (two board R/W only) at _PFX connector J35
- _RUX/_PGX at _RUX/_PGX connector J36
- _EBN/_EDN at _EBN/_EDN connector J19
- Operator panel at _PXX connector J26

Check voltages.

↓

004 Are ±5 volts OK?

Y N

↓

1 Check wiring and power supply.

↓

2 Replace _PXX (proc 5301).

↓

2
A

A
1

↓

005 Deenergize drive, add _PMX to +5 volt load by connecting cables to J24 (_PXX) and J37 (_PMX), then recheck voltages.

↓

006 Is +5 volts OK?

Y | N ↓

1 Replace _PMX (proc 5305).

007 Deenergize drive, add operator panel to +5 volt load by connecting cable to J26 (_PXX), then recheck voltages.

↓

008 Is +5 volts OK?

Y | N ↓

1 Replace operator panel (proc 5202).

009 Deenergize drive, add _EBN/_EDN to ±5 volt load by connecting cable to J19 (_EBN/_EDN), then recheck voltages.

↓

010 Are ±5 volts OK?

Y | N ↓

1 Replace _EBN/_EDN (proc 5302).

011 Deenergize drive, add module to ±5 volt load by connecting cable to J32 (_RUX/_PFX), then recheck voltages.

↓

012 Are ±5 volts OK?

Y | N ↓

1 Replace module (proc 5206).

A
3

ive have only one R/W board (_RUX)?

ze drive, add _PGX to ±5 volt load by connect-
e to J36 (_PGX), then recheck voltages.

olts OK?

Replace _PGX (proc 5303).

ze drive, add _PFX to ±5 volt load by con-
cable to J35 (_PFX), then recheck voltages.

olts OK?

Replace _PFX (proc 5304).

ace power supply (proc 5304). If problem
ists, call field support.

rive, add _RUX to ±5 volt load by connecting
(_RUX), then recheck voltages.

OK?

ace _RUX (proc 5306).

power supply (proc 5204). If problem
, call field support.

TSP3 - ±24 Volt Load Check

This check isolates problems with ±24 volts. Refer to procedure 4101 - Power Checks for voltage specifications.

001 Deenergize drive and check for short circuits between:

- +24 volts and -24 volts and ground.
- +24 volts and -24 volts.
- ±24 volts and ±5 volts.

↓

002 Do any short circuits exist?

N Y

↓

1 Remove loads (one at a time) to isolate short.

↓

2 Inspect wiring and boards.

↓

003 Remove all loads except _PXX (connector J21) from ±24 volts by disconnecting the following:

- _PMX at _PMX connector J37
- _QHX at _QHX connector J22
- _EBN/_EDN at _EBN/_EDN connector J19
- Fan at _EBN/_EDN connector J48

Check voltages.

↓

004 Are ±24 volts OK?

Y N

↓

1 Check wiring and power supply.

↓

2 Replace _PXX (proc 5301).

↓

005 Deenergize drive, add _PMX to +24 volt load by connecting cable to J37 (_PMX), then recheck voltage.

↓

2
A

A
1
↓

006 Is +24 volts OK?
Y N
| ↓
| 1 Replace _PMX (proc 5305).
↓

007 Deenergize drive, add _QHX to ±24 volt load by connecting cable to J22 (_QHX), then recheck voltage.
↓

008 Are ±24 volts OK?
Y N
| ↓
| 1 Replace _QHX (proc 5305).
↓

009 Deenergize drive, add _EBN/_EDN to ±24 volt load by connecting cable to J19, then recheck voltages.
↓

010 Are ±24 volts OK?
Y N
| ↓
| 1 Replace _EBN/_EDN (proc 5302).
↓

011 Deenergize drive, add fan to ±24 volt load by connecting cable to J48, then recheck voltage.
↓

012 Are ±24 volts OK?
Y N
| ↓
| 1 Replace fan (proc 5201).
↓

013 Replace power supply (proc 5204). If problem persists, call field support.

TSP4 - First Seek Check

001 Initiate first seek as follows:

a. Set LOCAL/REMOTE switch to LOCAL.

b. Set CB1 & START switch to ON.

↓

002 Does READY indicator light?

N Y

N: ↓

Y: ↓

003 Drive has successfully completed first seek.

↓

004 Do all fault LEDs light?

N Y

N: ↓

Y: ↓

005 Are ±5 volts OK?

Y N

Y: ↓

N: ↓

1 Check ±5 volts. See TSP2.

↓

2 Check connection at J28 (_PXX).

↓

1 Replace _PXX (proc 5301).

↓

006 Does First Seek Fault LED light?

Y N

Y: ↓

N: ↓

Is Fine Position signal at a dc level between +5 volts and -5 volts?

Y N

Y: ↓

N: ↓

1 Check ±5 volts. See TSP2.

↓

2 Replace _PXX (proc 5301).

↓

1 Check J25 (_PXX) to locking solenoid cable.

↓

2 Replace _PXX (proc 5301).

↓

3 Replace locking solenoid (proc 5205).

↓

008 Does Volt Fault LED light?

N Y

↓ ↓

2 2

A B

```
        A   B
        1   1
        |   |
            |
            1   Check all power harness connections.
            |
            2   Check power when drive is not seeking.  See TSP1.
            |
            3   Replace _PMX (proc 5305).
            |
            4   Replace _PXX (proc 5301).
            |
            5   Replace power supply (proc 5204).
        |
        |
009     Is motor running?
        N   Y
        |   |
            |
010         Are tribits OK?  (proc 4201)
            Y   N
            |   |
            |   1   Check connections at J28 (_PXX).
            |   |
            |   2   Replace _PXX (proc 5301).
            |   |
            |
012         Does Fine Position signal wander between +5 volt and
            -5 volts?
            Y   N
            |   |
            |   1   Check J23 (_PXX) to P23 (_QHX) connection.
            |   |
            |   2   Check  J43 (_QHX) connection.
            |   |
            |   3   Replace _QHX (proc 5305).
            |   |
            |   4   Replace _PXX (proc 5301).
            |   |
            |   5   Replace module (proc 5206).
            |
            1   Check connection at J28 (_PXX).
            |
            2   Replace _PXX (proc 5301).
            |
            3   Replace module (proc 5206).
        |
        |
        3
        A
```

A
2
↓

013 Is Motor Run signal active (_PXX, G738 Pin 10)?

N Y
| ↓
| 1 Replace module (proc 5206).
↓

014 Is Start signal active (_PXX, G738 Pin 13)?

Y N
| ↓
| 1 Check J26 connections (operator panel to _PXX).
| ↓
| 2 Replace operator panel (proc 5202).
| ↓
| 3 Replace _PXX (proc 5301).
↓

015 Replace _PXX (proc 5301). If problem persists, call field support.

TSP5 - Direct or RTZ Seek Check

This test assumes that the following conditions exist: (1) the drive is operating under control of the TB216 and (2) a first seek was successfully completed.

001 Does FAULT indicator light or is Seek Error active?
Y N
| ↓
002 | Direct or RTZ seek is OK.
↓
003 Does Write or Write and Read Fault LED light?
N Y
| ↓
| 1 Read/write problem. See TSP 6 or 7.
↓
004 Does Volt Fault LED light?
N Y
| ↓
| 1 Power problem. See TSP 1.
↓
005 Does On Cylinder go active?
N Y
| ↓
006 | Does error always occur at or near the same cylinder?
| Y N
| | ↓
| | 1 Check module to J28 (_PXX) and J23 (_PXX) to
| | | P23 (_QHX) cable connections.
| | ↓
| | 2 Replace _PXX (5301).
| | ↓
| | 3 Replace module (proc 5206).
| ↓
| 1 Replace module (proc 5206).
↓
2
A

A

1

↓

007 Does error always occur when seeking to or near the same cylinder?

N Y

1 Replace _PXX (proc 5301).

↓

2 Replace _EBN/_EDN (proc 5302).

↓

3 Replace module (proc 5206).

↓

1 Check module to J28 (_PXX) and J23 (_PXX) to P23 (_QHX) cable connections.

↓

2 Replace _EBN/_EDN (proc 5302).

↓

3 Replace _PXX (proc 5301).

↓

4 Replace module (proc 5206). If problem persists, call field support.

TSP6 - Write Check

This check assumes that the drive is performing write or write format operations under control of the TB216.

001 Does Volt Fault LED light?
N Y
Y → 1 Power problem. Go to TSP1.

002 Does Read and Write Fault LED light?
N Y
Y → 1 Check I/O connections.
→ 2 Check _EBN/_EDN to J27 (_RUX/_PGX) cabling.
→ 3 Replace _EBN/_EDN (proc 5302).
→ 4 Replace _RUX (proc 5306) or _PGX (proc 5303).

003 Does Read or Write and Not On Cylinder Fault LED light?
N Y
Y → 1 Servo problem. Go to TSP 4 or 5.

004 Does Write Fault LED light?
N Y
Y →

005 Is problem head related?
N Y
Y →

006 Is Unsafe active (_RUX, chip H856, Pin 9; _PFX, chip L126, Pin 10)?
Y N
N → 1 Replace module (proc 5206).

2A 2B 2C

A 1 | B 1 | C 1

1 Check head/cylinder address bits on _RUX/_PFX. If bits are OK, replace module (proc 5206). Otherwise, proceed to next action.

2 Check I/O connections.

3 Check J20 (_EBN/_EDN) to J14 (_PXX) cabling.

4 Check J32 (_RUX/_PFX) to module cabling.

5 Replace _EBN/_EDN (proc 5302).

6 Replace _PXX (proc 5301).

7 Replace _RUX (proc 5306) or _PFX (proc 5304).

8 Replace module (proc 5206).

007 Is Unsafe active (_RUX, chip H856, Pin 9; _PFX, chip L126, Pin 10)?

Y / N

N:

1 Check for data at output of _RUX/_PFX. If data is absent, perform 4303 - Write Data Check.

2 Check head/cylinder address bits on _RUX/_PFX. If bits are OK, replace module (proc 5206). Otherwise, proceed to next action.

3 Replace module (proc 5206).

Y:

1 Perform procedure 4303 - Write Data Check.

2 Replace _RUX (proc 5306) or _PFX (proc 5304).

3 Replace _PGX (proc 5303). If _RUX was replaced in previous action, go to next action.

4 Replace _PXX (proc 5301).

5 Replace module (proc 5206).

3 A

A
2

↓

008 Perform procedure 4302 - Write PLO Check.

↓

009 Is the 1.612 MHz clock OK?

Y | N
| ↓
| 1 Servo problem. See TSP 4 or 5.
↓

010 Is the 2F clock OK?

Y | N
| ↓
| 1 Replace _RUX (proc 5306) or _PGX (proc 5303).
↓

011 Is the 9.67 MHz clock OK?

Y | N
| ↓
| 1 Replace _RUX (proc 5306) or _PGX (proc 5303).
| ↓
| 2 Replace _EBN/_EDN (proc 5302).
↓

012 Are Write Gate, Write Clock, and Write Data OK? (proc 4303)

Y | N
| ↓
| 1 Check I/O connections.
| ↓
| 2 Check _EBN/_EDN to J27 (_RUX/_PGX) cabling.
| ↓
| 3 Replace _EBN/_EDN (proc 5302).
| ↓
| 4 Replace _RUX (proc 5306) or _PGX (proc 5303).
↓

013 Is Write Data Compensated OK?

Y | N
| ↓
| 1 Replace _RUX (proc 5306) or _PGX (proc 5303).
↓

014 Is Read/Write Data to preamplifier OK?

N | Y
| ↓
↓

015 Write Data Check OK. If problems persist, call field support.

4
A

A
3
↓

016 Is Write Enable OK?

Y | N
| ↓
| 1 Check J29 (_PXX) to J30 (_RUX/_PFX) cabling.
| ↓
| 2 Check J20 (_EBN/_EDN) to J14 (_PXX) cabling.
| ↓
| 3 Replace _PXX (proc 5301).
| ↓
| 4 Replace _RUX (proc 5306) or _PFX (proc 5304).
↓
1 Check J31 (_PGX) to J30 (_PFX) cabling. If _RUX is installed, go to next action.
↓
2 Replace _RUX (proc 5306) or _PFX (proc 5304).
↓
3 Replace module (proc 5206). If problem persists, call field support.

TSP7 - Read Check

This check assumes that the drive is performing read operations under control of the TB216.

001 Does Volt Fault LED light?
N Y
Y
002 1 Power problem. See TSP1.

003 Does Read and Write Fault LED light?
N Y
Y
1 Check I/O connections.
Y
2 Check _EBN/_EDN to J27 (_RUX/_PGX) cabling.
Y
3 Replace _EBN/_EDN (proc 5302).
Y
4 Replace _RUX (proc 5306) or _PGX (proc 5303).

004 Does Read or Write and Not On Cylinder Fault LED light?
N Y
Y
1 Servo problem. See TSP 4 or 5.

005 Is address mark detected?
Y N
Y
1 Perform procedure 4403 - Read AM Check and go to TSP8.

006 Is there a data error?
Y N
Y
007 Read operation is OK.
2
A

```
        A
        1
        |
        ↓
008     Are errors head related?
        N   Y
        |   ↓
        |   1   Check head/cylinder address bits on _RUX/_PFX.
        |   |   If bits are bad, suspect:
        |   |       a.  Cabling problem.
        |   |       b.  _EBN/_EDN, _PXX, _RUX/_PFX, or module.
        |   ↓
        |   2   Replace _RUX (proc 5306) or _PFX (proc 5304).
        |   ↓
        |   3   Replace _PGX (proc 5303).  If _RUX was replaced in
        |   |   previous action, go to next action.
        |   ↓
        |   4   Replace module (proc 5206).
        ↓
009     Perform procedure 4402 - Read Data Check.
        |
        ↓
010     Is Read Gate active?
        Y   N
        |   ↓
        |   1   Check I/O connections.
        |   ↓
        |   2   Check _EBN/_EDN to J27 (_RUX/_PGX) cabling.
        |   ↓
        |   3   Replace _EBN/_EDN (proc 5302).
        |   ↓
        |   4   Replace _RUX (proc 5306) or _PGX (proc 5303).
        ↓
011     Is 1.612 MHz Clock OK?
        Y   N
        |   ↓
        |   1   Servo problem.  See TSP 4 or 5.
        ↓
012     Is Read Clock and 2F Read Oscillator OK?
        Y   N
        |   ↓
        |   1   Replace _RUX (proc 5306) or _PGX (proc 5303).
        ↓
        3
        A
```

A
2
↓

013 Is head and preamplifier output OK?

Y | N ↓

1 Check J32 (_RUX/_PFX) to module cabling.

↓

2 Replace _RUX (proc 5306) or _PFX (proc 5304).

↓

3 Replace module (proc 5206).

014 Is Latched Read Data OK?

Y | N ↓

1 Replace _RUX (proc 5306) or _PFX (proc 5304).

015 Is NRZ Read Data OK?

Y | N ↓

1 Replace _RUX (proc 5306) or _PGX (proc 5303).

016 Is Read Gate and Lock to Data timing OK?

Y | N ↓

1 Replace _RUX (proc 5306) or _PGX (proc 5303).

1 Replace _RUX (proc 5306) or _PFX (proc 5304).

↓

2 Replace _PGX (proc 5303). If _RUX was replaced in previous action, go to next action.

↓

3 Replace _PXX (proc 5301).

↓

4 Replace module (proc 5206). If problem persists, call field support.

TSP8 - Address Mark Check

The following check assumes that the drive is under control of the TB216.

001 Perform procedure 4403 - Read AM Check.

↓

002 Is AM Enable active?

Y N

N ↓

1 Check I/O connections.

↓

2 Check _EBN/_EDN to J27 (_RUX/_PGX) cabling.

↓

3 Check J31 (_PGX) to J30 (_PFX) cabling. If _RUX is installed, go to next action.

↓

4 Replace _RUX (proc 5306) or _PFX (proc 5304).

↓

5 Replace _PGX (proc 5303). Two board R/W only.

Y ↓

003 Is AM Found active?

Y N

N ↓

1 Replace _RUX (proc 5306) or _PGX (proc 5303).

↓

2 Replace _PFX (proc 5304). Two board R/W only.

Y ↓

004 Is AM proper length?

Y N

N ↓

005 Perform procedure 4304 - Write AM Check.

↓

006 Is AM Enable active?

Y N

N ↓

1 Check I/O connections.

↓

2 Check _EBN/_EDN to J27 (_RUX/_PGX) cabling.

↓

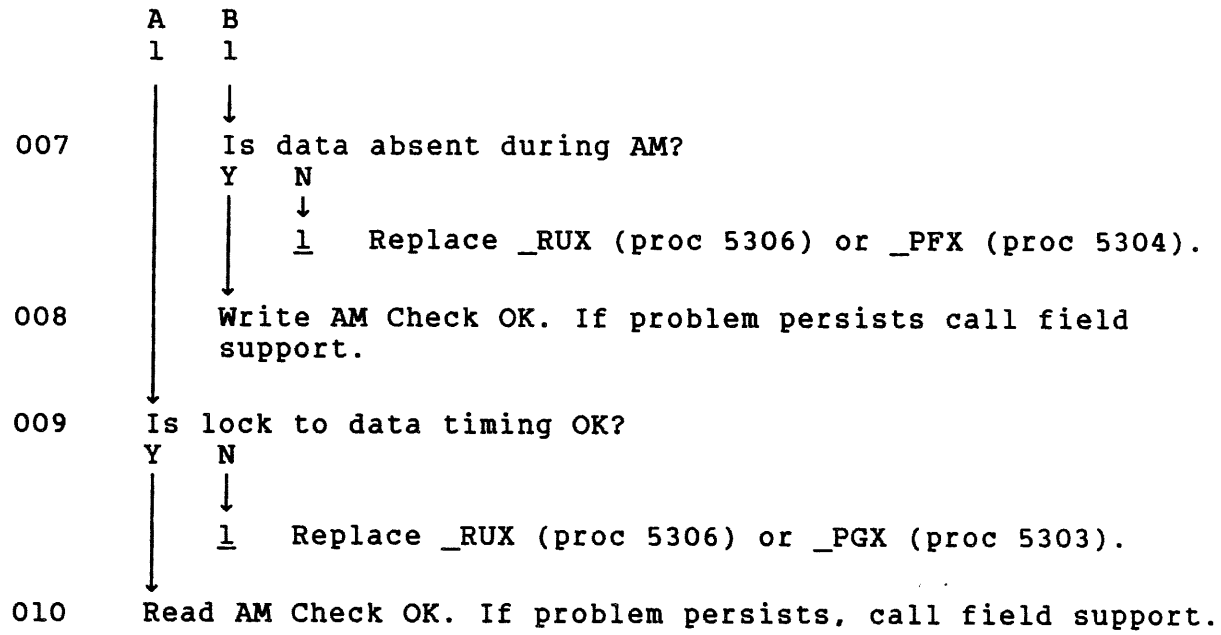
3 Replace _EBN/_EDN (proc 5302).

↓

4 Replace _RUX (proc 5306) or _PGX (proc 5303).

Y (004) ↓ 2A

Y (006) ↓ 2B


A
1
B
1
007
Is data absent during AM?
Y
N
1 Replace _RUX (proc 5306) or _PFX (proc 5304).
008
Write AM Check OK. If problem persists call field support.
009
Is lock to data timing OK?
Y
N
1 Replace _RUX (proc 5306) or _PGX (proc 5303).
010
Read AM Check OK. If problem persists, call field support.

SERVO STATUS CODES

GENERAL

The servo status codes are two digit hexadecimal codes, generated by the MPU, that indicate the operational status of the drive servo system. Whenever the drive is in a power on condition (dc power active), the MPU is periodically checking the operation of the servo system and generating appropriate status codes. The codes can be visually monitored by connecting the servo status display board (_JWN) to a test jack on the _PXX board. The following discussions explain how to install the display board and define the various codes.

Installing the Servo Status Display Board (_JWN)

1. Set START switch and CB1 to off.
2. Connect one end of signal cable to display board (see table 2-1 for part numbers) and the other end to test jack of _PXX board (see figure 3-2).
3. Proceed with testing.

SERVO STATUS CODE DEFINITIONS

Table 3-1 is a summary of all the status codes and table 3-2 provides a definition of each code. Each definition in table 3-2 is divided into three parts:

1. Description: Basic definition of what type of problem the code indicates, during what operations the code appears, what additional error indications are present with the code, and how to initiate a retry or recovery from the error.
2. Probable Causes: What general areas could cause the problem. The purpose here is to provide a general idea of what functional areas could be causing the problem.
3. Actions: What specific things to check to correct the problem. Perform each action and retest the drive before proceeding to the next action. If all actions have been performed and the problem persists, call field support.

When interpreting the status codes it is important to know that not all codes appearing on the display indicate errors. Some indicate that the operation is still in progress, others that the operation has been successfully completed.

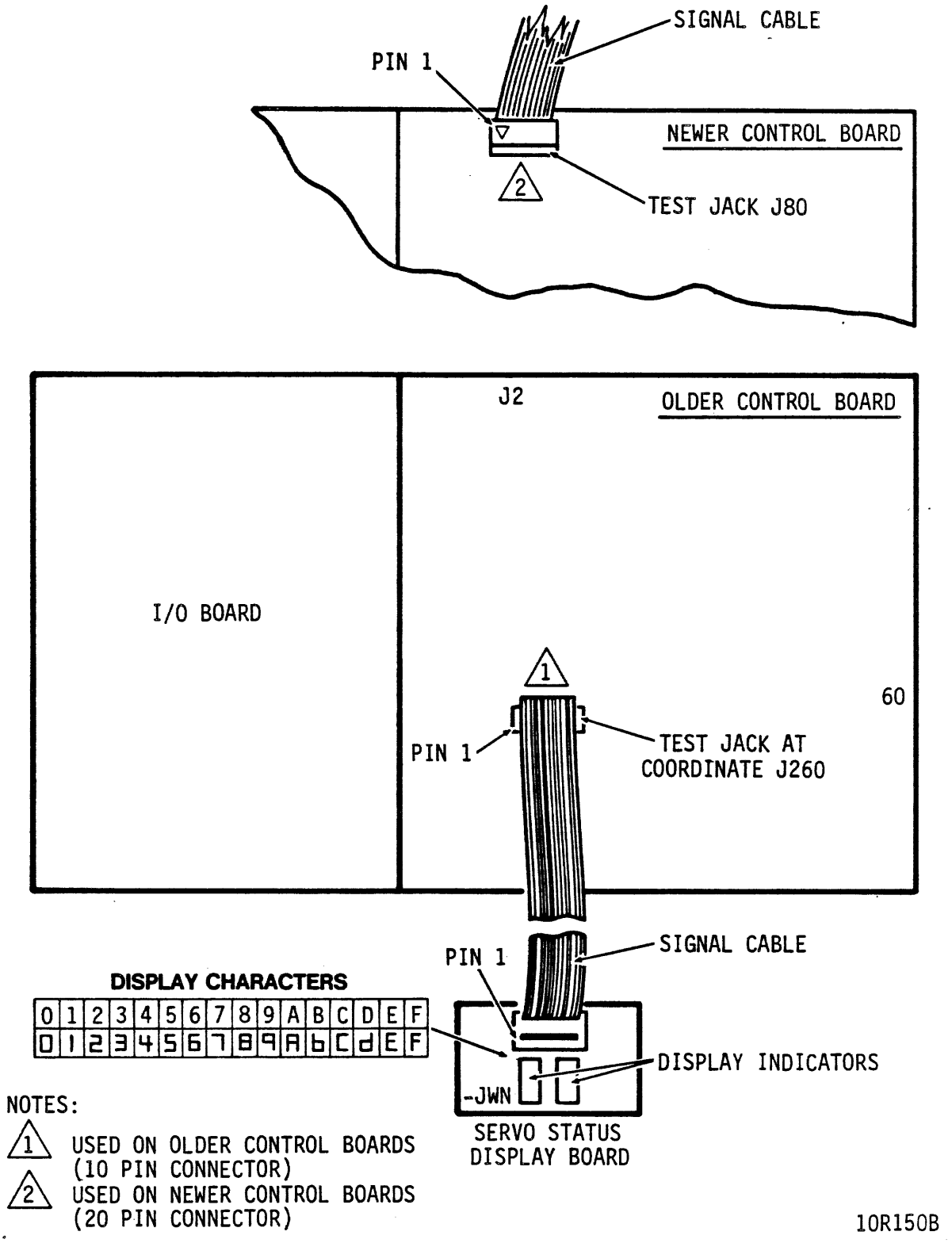


Figure 3-2. Servo Status Display Board Installation

When an operation is in progress, the status is continually changing. Most codes flash on and off very rapidly and are not recognizable. Others will remain for several seconds.

If an operation is successful, the display shows the upper eight bits of the destination cylinder address. For example: after a power on or seek to cylinder 0 the display shows 00, after a seek to cylinder 822 the display shows CD. The destination is displayed until another seek is initiated or an error occurs.

If an error occurs, the status indicates the type of error and where in the sequence the error occurred. The error code remains active until the proper action is taken to reset it (depends on nature of error).

It is possible for an error code to be the same as the desired destination address. Therefore, unless it is obvious from other indications that an error has occurred, always check the On Cylinder signal. If On Cylinder is active the seek was successfully completed.

TABLE 3-1. STATUS CODE SUMMARY

Status Code	Description
	Start/Stop Status
01	Unloading Heads
02	Stopping Motor
03	Motor Stopped OK
08	Motor Start In Progress
0A	Too Long To Get Up To Speed
0B	Too Long To Get Up To Speed (Sensor Fault)
0C	Too Many Startup Failures
	Load Status
24	No Demodulator OK During Load
25	No Cylinder Pulses
26	Timeout (No Guard Bands Found)
2C	Calibrate Error (Seek Error During Calibrate)
	Load or RTZ Status
31	Lost Demodulator OK During RTZ
33	Timeout Error
37	Can't Find Cylinder Pulses In Guard Band Area

Table Continued on Next Page

TABLE 3-1. STATUS CODE SUMMARY (Contd)

Status Code	Description
	Seek or On Cylinder Status
40	Inner Guard Band Detected During Normal Seek
43	Outer Guard Band Detected During Normal Seek
46	Seek Timeout
4A	Too Many On Cylinder Dropouts
4B	Lost On Cylinder Sense
4D	Illegal Cylinder Address
4E	Voltage Fault While On Cylinder
	Miscellaneous
5C	Fan Fault
5F	MPU Failed PIA Test
FF	MPU Failed Power On Test

TABLE 3-2. STATUS CODE DEFINITIONS

Code	Description
01	Title: Unloading Heads Description: The MPU sets code 01 while it is unloading the heads. This status lasts approximately 2 seconds under normal conditions. If the heads unload, the motor stop sequence begins and the status changes to 02. If the MPU does not detect the heads unloaded condition, the status remains at 01 and the motor continues to run. Probable Causes: Drive continues to detect cylinder pulses due to noise, control circuit failure or power amp failure. Actions 1. Replace _PXX board (proc 5301). 2. Replace _QHX board (proc 5305). 3. Replace module (proc 5206).
02	Title: Stopping Motor Description: The MPU sets code 02 during the braking period. When the motor is stopped (typically within 7 seconds), the status changes to 03. If the MPU does not detect a motor stop, the status remains at 02. Probable Causes: Indicates a problem with the motor control circuits or a brake failure.

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	Actions: 1. If motor is running: a. Replace _PMX board (proc 5305). b. Repair or replace brake (proc 5203). 2. If motor is not running: a. Replace _PMX board (proc 5305). b. Replace _PXX board (proc 5301). c. Repair or replace brake (proc 5203).
03	Title: Motor Stopped OK Description: The MPU sets code 02 when it detects that the motor is stopped. This code will be displayed following a normal stop sequence. Probable Causes: Not Applicable Actions: Not Applicable
08	Title: Motor Start in Progress Description: Indicates that the motor has been started. Code 08 is displayed until either an error occurs or the heads successfully reach cylinder 0 and code 0 appears. Probable Cause: Not Applicable Actions: Not Applicable

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
0A	Title: Too Long to Get Up to Speed (No Sensor Fault) Description: Indicates that drive did not come up to speed within 15 seconds of starting. If the motor comes up to speed, and the heads successfully load, code 00 appears. If after three tries the motor does not come up to speed, the motor stops, and display changes to 0C. No more attempts will be made unless the START switch is cycled. Probable Causes: See code 0C. Actions: See code 0C
0B	Title: Too Long to Get Up to Speed (Sensor Fault) Description: Indicates that a motor fault was detected while waiting for drive to come up to speed. The power off sequence begins immediately when this condition is sensed. Probable Causes: Motor or motor control board. Actions: 1. Replace _PMX board (proc 5305). 2. Replace module (proc 5206).
0C	Title: Too Many Startup Failures Description: Indicates that the drive has failed three times to bring the motor up to speed (see code 0A). Setting START switch to Off and back to On causes three more attempts.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	Probable Causes: Power supply, motor control circuits or motor. Actions: 1. Check J40 to J37, (Remote Power Supply), P15 to J37 (Integral Power Supply), P24 to J24, and J39 to motor wiring. 2. Check +40 volts from power supply. 3. Ensure the brake is not energized constantly. If so, replace brake (proc 5203). 4. Replace _PMX board (proc 5305). 5. Replace module (proc 5206).
24	Title: No Demodulator OK During Load Description: Indicates that, during a load sequence, tribits were not detected properly and Demodulator OK did not go active. When the drive displays code 24, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active. Pressing the Fault Clear switch clears the fault and initiates another load. Probable Causes: Bad tribit detection circuit or bad servo disk. Bad cable at J28.

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	Actions: 1. Check cable connection at J28 on the _PXX board. 2. Replace _PXX board (proc 5301). 3. Replace module (proc 5206).
25	Title: No Cylinder Pulses Description: Indicates that, during a load sequence, the MPU did not detect cylinder pulses during its move toward the outer guard band. When the drive displays code 25, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active. Pressing the Fault Clear switch clears the fault and initiates another load. Probable Causes: Bad servo disk or cylinder pulse detection circuits. Actions: 1. Check for the presence of a servo signal at J28 pins 2 and 4 on the _PXX board. 2. Replace _PXX board (proc 5301). 3. Replace locking solenoid (proc 5205).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
26	Title: Timeout (No Guard Bands Found) Description: Indicates that, during a load sequence, the MPU did not detect cylinder pulses during its move toward the outer guard band. When the drive displays code 25, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active. Pressing the Fault Clear switch clears the fault and initiates another load. Probable Causes: Bad servo disk or cylinder pulse detection circuits. Actions: 1. Check for the presence of a servo signal at J28 pins 2 and 4 on the _PXX board. 2. Replace _PXX board (proc 5301). 3. Replace locking solenoid (proc 5205).
2C	Title: Calibrate Error (Seek Error During Calibrate) Description: Indicates that a seek error occurred during the calibrate routine. When the drive displays code 2C, the following error conditions also appear:

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk. • Seek Error and Seek End lines go active. Pressing the Fault Clear switch initiates another load attempt. Probable Causes: Loose cable connections, a failure in the velocity control circuits, or a bad servo disk. Actions: 1. Check for loose cable connections at J28, J23 and J14 to J20 of _PXX board. 2. Replace _QHX board (proc 5305). 3. Replace _PXX board (proc 5301). 4. Replace module (proc 5206).
31	Title: Lost Demodulator OK During RTZ Description: Indicates that during an RTZ, Demodulator OK went inactive. When the drive displays code 31, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active. • Motor continues to run.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	Commanding an RTZ clears the seek error and initiates another retry. Probable Causes: Bad servo disk, loose connection or failure that causes load/retract loop to lose feedback. Actions: 1. Replace _PXX board (proc 5301). 2. Check for the presence of a servo signal at J28 pins 2 and 4, on the _PXX board. If no signal is present, replace the module.
33	Title: Timeout Error Description: Indicates that during a load or RTZ, too much time elapsed before the heads reached the outer guardband. When the drive displays code 33, the following error indications also appear. • First Seek LED lights (first seek only). • FAULT indicator lights and Fault line goes active (first seek only). • Seek Error and Seek End lines go active. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another attempt. Probable Causes: Failure in velocity circuits, bad power amplifier or power amplifier driver circuits.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	Actions: 1. Replace _PXX board (proc 5301). 2. Replace _QHX board (proc 5305). 3. Check the voice coil connection. 4. Replace module (proc 5206).
37	Title: Can't Find Cylinder Pulses In Guard Band Area Description: Indicates that, during a load or RTZ, the drive failed to find four cylinder pulses while in the guard band area. When the drive displays code 37, the following error indications also appear. • First Seek LED lights (first seek only). • Seek Error and Seek End lines go active. • FAULT indicator lights and Fault line goes active (first seeks only). • Motor continues to run. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. Probable Causes: Bad tribit decoder circuit, cylinder pulse detection circuit, or servo disk. Misadjusted end of travel stop within module.
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	Actions: 1. Replace _PXX board (proc 5301). 2. Replace module (proc 5206).
40	Title: Inner Guardband Detected During Normal Seek Description: Indicates that guardband pulses were detected while the heads were moving over the data zone. When the drive displays code 40, the following error indications also appear. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error and Seek End lines go active. An RTZ command clears the seek error and initiates a seek to cylinder 0. Probable Causes: Cylinder pulses missed or miscounted during seek to cylinder 822. Could be caused by bad cylinder pulse detection circuits, bad tribit decoder circuits, faulty cables or connectors, or electrical noise generated by nearby equipment. Actions: 1. Ensure that drive is not located near source of extreme electrical noise. 2. Check all cables for bad connections. 3. Replace _PXX board (proc 5301). 4. Replace module (proc 5206).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
43	Title: Outer Guardband Detected During Normal Seek Description: Indicates that guardband pulses were detected while the heads were moving over the data zone. When the drive displays code 43, the following error indications also appear. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. • Seek Error and Seek End lines go active. A RTZ command clears the seek error and initiates a seek to cylinder 0. Probable Causes: Cylinder pulses missed or miscounted during seek to cylinder 0. Could be caused by bad cylinder pulse detection circuits, faulty cables, or by electrical noise generated by nearby equipment. Actions: 1. Ensure that drive is not located near source of extreme electrical noise. 2. Check all cables for bad connections. 3. Replace _PXX (proc 5301). 4. Replace module (proc 5206).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
46	Title: Seek Timeout Description: Indicates that during a normal seek the drive took longer than 65 milliseconds to reach on cylinder. When the drive displays code 46, the following error indications also appear. • Seek Error and Seek End lines go active. • Motor continues to run but servo system is disabled and the heads, although loaded, drift freely over the disk surfaces. An RTZ clears the seek error and initiates a seek to cylinder 0. Probable Causes: Problem with velocity circuits. Check cylinder pulse circuits and Fine Enable signal. Actions: 1. Replace _PXX board (proc 5301).
4A	Title: Too Many On Cylinder Dropouts Description: Indicates that On Cylinder Sense took too long to stabilize during the settle in phase. When the drive displays code 4A, the following error indications also appear. • First Seek LED lights (first seek only). • Seek Error and Seek End lines go active. • FAULT indicator lights and Fault line goes active (first seek only).

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. If the error occurs during a first seek, pressing the Fault Clear switch clears the fault and initiates another load. If it occurs during an RTZ, commanding another RTZ clears the seek error and initiates another seek to cylinder 0. Probable Causes: Bad servo disk, bad tribit decoder circuits, loose cabling in feedback loop, or poor tracking due to mechanical problems. Actions: Perform sequential forward seeks with read. 1. If error occurs at same cylinder each time, replace the module (proc 5206). 2. If error occurs during random seeks, perform the following steps: a. Check for loose cable connections between module and the _PXX board (proc 5301). b. Check shipping damper adjustment (proc 5206). c. Replace _PXX board (proc 5301). d. Replace module (proc 5206).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
4B	Title: Lost On Cylinder Sense Description: Indicates that On Cylinder Sense went inactive. When the drive displays code 4B, the following error indications also appear. • On Cylinder goes inactive. • Seek Error goes active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk. A RTZ command clears the seek error and initiates a seek to cylinder 0. Probable Causes: Bad servo disk, loose cabling in feedback loop, poor tracking due to mechanical problems, or electrical or mechanical outside interference. Actions: Perform sequential forward seeks with read. 1. If error occurs at same cylinder each time, replace the module. 2. If error occurs at random locations: a. Check for loose cable connections between the module and _PXX board. b. Ensure that malfunction was not caused by excessive vibration levels (for example, from nearby construction activity), or electrical noise generated by nearby equipment (for example, line printers).

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	c. Replace the __PXX board (proc 5301). If problem persists, replace the module (proc 5206).
4D	Title: Illegal Cylinder Address Description: Indicates that, during a normal seek, the MPU received too high a cylinder address (greater than 822). When the drive displays code 4D, the following error indications also appear. • On Cylinder goes inactive. • Seek Error and Seek End go active. • Motor continues to run but the servo system is disabled and the heads, although loaded, float freely over the disk surfaces. Probable Causes: Illegal address from controller not detected by I/O board. Bad address decoding on _PXX board. Actions: 1. Replace _EBN/_EDN board (proc 5302). 2. Replace _PXX board (proc 5301).
4E	Title: Voltage Fault While On Cylinder Description: Indicates that the MPU detected a voltage fault while On Cylinder was active. When the drive displays code 4E, the following error indications also appear.

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	• READY indicator goes out and Ready line goes inactive. • Seek Error goes active. • FAULT indicator lights and Fault line goes active. • Motor continues to run but actuator floats freely. If the fault is no longer present, a Controller Fault Clear followed by an RTZ or pressing Fault Clear switch clears the fault and initiates a load and seek to cylinder 0. Probable Cause: Power failure within drive, power supply or site power. Actions: Check LEDs for cause of fault condition. 1. If voltage fault exists go to TSP1 - Power Check. 2. If a fault other than voltage exists: a. Check I/O cabling. b. Replace _EBN/_EDN board (proc 5302).
Table Continued on Next Page	

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
5C	Title: Fan Fault Description: Indicates that drive cooling fan has failed. If the fan fault stays set for greater than 400 ms, the drive will stop (similar to using Start switch to stop drive). During this period, the MPU will continually attempt to clear the fault. If the MPU is successful in clearing the fault, the drive will start (provided no other faults are present). Probable Causes: Clogged air filter, defective cooling fan, or dc voltage missing from fan cable. Actions: 1. If fan is running: a. Check air filter. Clean or replace if dirty. b. Replace _EBN/_EDN board (proc 5302). 2. If fan is not running: a. If -24 V is present at fan connector, replace fan (proc 5201). b. If -24 V is not present, go to TSP3 (±24 volt load check). c. Replace _EBN/_EDN board (proc 5302).
5F	Title: MPU Failed PIA Test Description: Indicates that the MPU detected a PIA failure during power on initialization. When this occurs, the drive stops the power on sequence and keeps all fault LEDs lit. To clear the error and initiate a retry, set CB1 to OFF and then back to ON.

Table Continued on Next Page

TABLE 3-2. STATUS CODE DEFINITIONS (Contd)

Code	Description
	Probable Causes: Bad PIA or defective chip in MPU system. Actions: 1. Check that no test probes are shorting out PIA outputs. 2. Replace _PXX board (proc 5301).
FF	Title: MPU Failed Power On Test Description: Indicates that MPU failed power on initialization test. When this occurs, the drive stops the power on sequence and keeps all fault LEDs lit. To clear the error and initiate a retry, set CB1 to OFF and then back to ON. Probable Causes: Bad microprocessor, random access memory, or other failure preventing microprocessor from operating. Actions: 1. Replace _PXX board (proc 5301).

SECTION 4

ELECTRICAL CHECKS

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in Section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

This section contains electrical checks intended for use in isolating problems causing improper drive operation. These procedures should be used in conjunction with the troubleshooting information in section 3.

If the drive appears to be operating properly, failure to meet a specification given here does not in itself indicate improper drive operation. The person performing these procedures should be thoroughly familiar with drive operation and with all information in the general maintenance section of this manual (particularly the warnings and precautions).

Each electrical check procedure is assigned a unique number. The numbers are used elsewhere in the manual to reference the procedures. The procedure numbers are organized into five categories: 41XX - power checks, 42XX - servo checks, 43XX - write checks, 44XX - read checks, and 45XX - miscellaneous.

The procedures appear in the following order.

- 4101 - Power Checks
- 4201 - Tribit Check
- 4202 - Position Signal Check
- 4203 - Servo Offset Check
- 4204 - On Cylinder Check
- 4205 - Cylinder Pulse Check
- 4301 - Write Fault Grounding
- 4302 - Write PLO Check

- 4303 - Write Data Check
- 4304 - Write Address Mark Check
- 4305 - Write Current Check
- 4401 - Read PLO Check
- 4402 - Read Data Check
- 4403 - Read Address Mark Check
- 4501 - Index Check
- 4502 - Sector Check

4101 - POWER CHECKS

The following procedure provides an overall check of the dc voltages used by the drive. Table 4-1 shows the voltages required by each drive component. See the diagrams section of hardware maintenance manual, volume 3 for specific information concerning voltage test points.

CAUTION

Because some voltage measurements are on pins adjacent to each other, it is possible to touch both pins simultaneously, thus causing a short circuit. A short circuit will cause serious damage to drive electronic assemblies. Therefore, use extreme caution when performing the following steps.

1. Command continuous seeks between cylinder 0 and 274.

2. Connect voltmeter ground lead to J19-4 (ground).

3. Measure between J19-4 and the appropriate connection points to check the following voltages:

Voltage	Connection	Specification
+5 volts	J19-7 (_EBN/_EDN)	+4.90 to +5.25 volts
-5 volts	J19-1 (_EBN/_EDN)	-4.90 to -5.30 volts
-8.3 volts	J28-6 (_PXX)	-7.7 to -8.8 volts
+24 volts	J19-5 (_EBN/_EDN)	+21.6 to +26.4 volts
-24 volts	J19-6 (_EBN/_EDN)	-21.6 to -26.4 volts
+40 volts	J40-7 (pwr input)	+36 to +42 volts (motor must be running to observe +40 volts)

4. Prceed to next test or return drive to online operation.

TABLE 4-1. DC VOLTAGE DISTRIBUTION

Component	Voltage					
	+5V	-5V	-8.3V	+24V	-24V	+40V
_PXX	X	X	X	X	X	
_RUX	X	X				
_PGX	X	X				
_PFX	X	X				
_EBN/_EDN	X	X		X	X	
_QHX				X	X	X
_PMX	X			X		X
_EYN*	X	X				
_UBN*			X			
Fan					X	
Motor	X					X
Op Pnl (_PBX)	X					

*Located in Module

SERVO CHECKS

4201 - TRIBIT CHECK

1. Connect oscilloscope as shown on figure 4-1.
2. Command direct seek to cylinder 0.
3. Observe that the relationship between +Servo Tribit and -Servo Tribit signals is similar to that on figure 4-1.
4. Connect oscilloscope as shown on figure 4-2.
5. Observe that the +Tribit signal is similar to that on figure 4-2.
6. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	5.0 mv/cm	J28-04 ON _PXX	-SERVO
CH 2	5.0 mV/cm	J28-02 ON _PXX	+SERVO

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1μS/CM MODE:

NOTES:

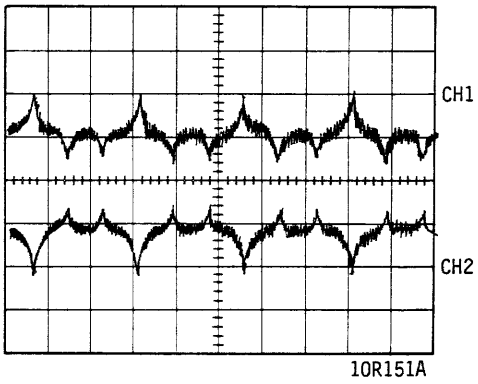


Figure 4-1. Servo Signal Waveform

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/OM	CHIP N356 PIN 10 ON-PXX	+TRIBIT
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 1μ S/CM MODE:

NOTES:

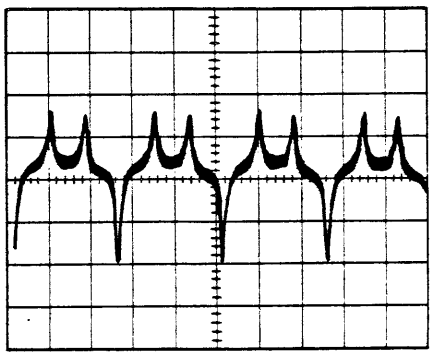


Figure 4-2. Tribits Waveform

4202 - POSITION SIGNAL CHECK

1. Connect oscilloscope as shown on figure 4-3.

2. Command continuous seeks between cylinders 0 and 274.

3. Observe that the peak to peak value of +Position signal remains between 9 and 10 volts over the period of a complete seek.

4. Command continuous seeks between cylinders 0 and 822 and observe that +Position is as described in step 3 (see figure 4-4).

5. Return drive to online operation.

6. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	CHIP D282 PIN 1 ON _PXX	+POSITION
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+EXT	CHIP G738 PIN 2 ON _PXX	-FORWARD

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 5 MS/CM MODE: CH 1

NOTES:

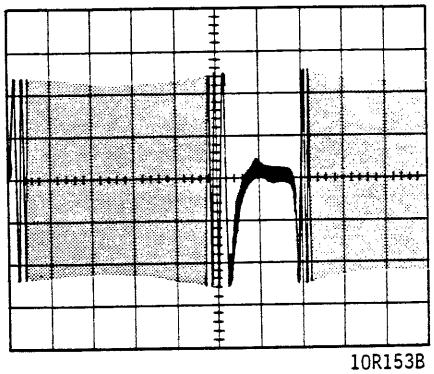


Figure 4-3. Position Signal (Tracks 0-274)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	CHIP D282 PIN 1 ON _PXX	+POSITION
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+EXT	CHIP G738 PIN 2 ON _PXX	-FORWARD

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 5 MS/CM MODE: CH1

NOTES:

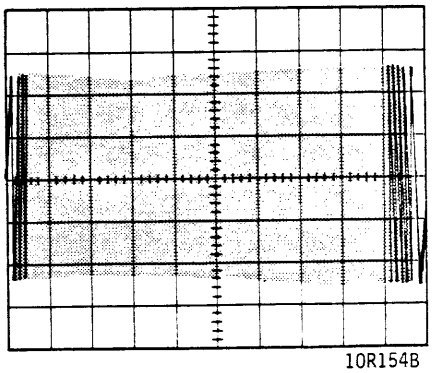


Figure 4-4. Position Signal (Tracks 0 to 822)

4203 - SERVO OFFSET CHECK

This procedure checks the amount of head offset caused by a servo offset command. The measurement is made on the Position signal. The Position signal has an average dc level of zero, when there is no offset and the heads are on cylinder.

1. Connect digital voltmeter between chip D282 Pin 1 and ground (chassis).

2. Command direct seek to cylinder 0 and observe that meter indicates 0 $\pm$ 200 millivolts.

3. Command a read operation with positive (forward) offset and observe that meter indicates an average dc offset between +0.60 and +0.90 volts, except that units with BPXX, CPXX, or DPXX control board should be between +1.35 and +1.65 volts.

4. Command a read operation with negative (reverse) offset and observe that meter indicates an average dc offset between -0.60 and -0.90 volts, except that units with BPXX, CPXX, or DPXX control board whould be between -1.35 and -1.65 volts.

5. Proceed to next test or return drive to online operation.

4204 - ON CYLINDER CHECK

This procedure verifies that On Cylinder goes active.

1. Connect oscilloscope as follows:

   a. Connect channel 1 to TP-D617(G) (+ On Cylinder) on _EBN/_EDN board.

   b. Trigger + Internal.

   c. Set other controls as appropriate to make measurement in step 3.

2. Command continuous seeks between cylinders 0 and 1.

3. Observe that + On Cylinder goes active.

4. Proceed to next test or return drive to online operation.

4205 - CYLINDER PULSE CHECK

This procedure verifies the presence and pulse width of drive cylinder pulses.

1. Connect oscilloscope as follows:

   a. Connect channel 1 to chip E243 Pin 6 (-Cylinder Pulses) on _PXX board.

   b. Trigger + Internal.

   c. Set other controls as appropriate to make measurements in step 3.

2. Command continuous seeks between cylinders 0 and 822.

3. Observe that Cylinder Pulses are present and have a pulse width greater than 1.25 microseconds.

4. Proceed to next test or return drive to online operation.

WRITE CHECKS

The following procedures, 4301 through 4305, check various aspects of drive write circuit operation. Figure 4-5 is a block diagram showing the major components in the write circuits and the test points used in the procedures.

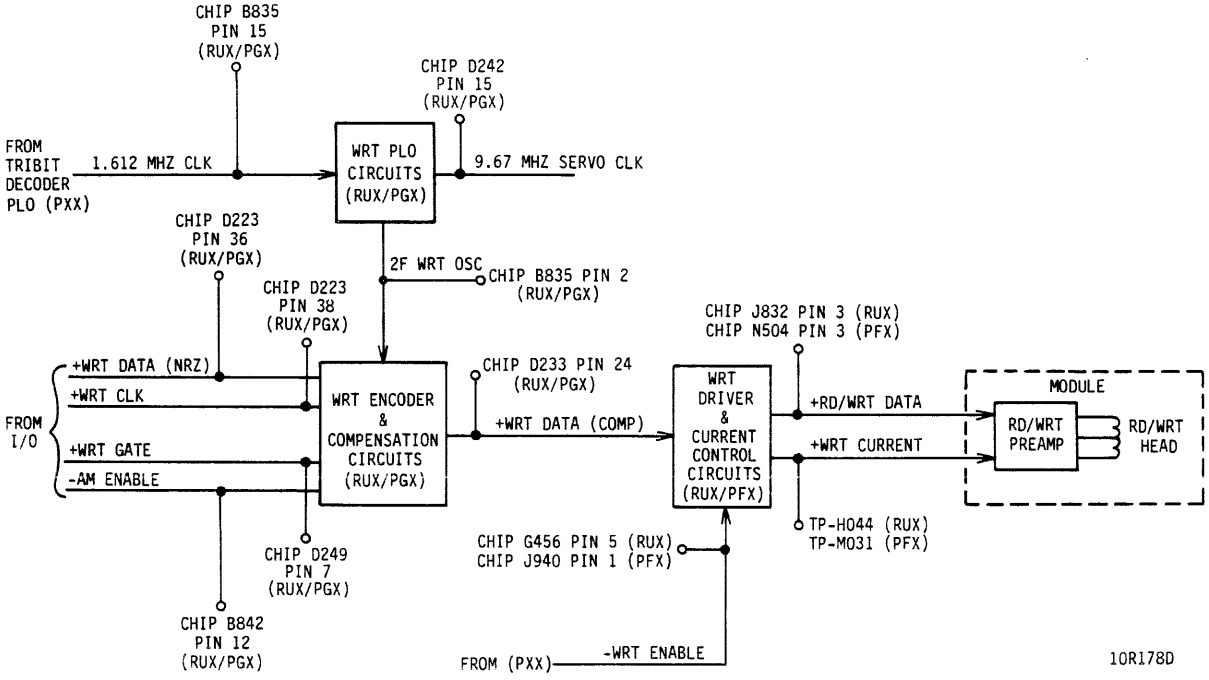


Figure 4-5. Write Circuits Test Points

4301 - WRITE FAULT GROUNDING

If a write fault condition exists, the drive write circuits are disabled. This makes it difficult to test the write circuits and isolate the problem. Grounding the Write Fault signal at the point where it leaves the __RUX/_PGX board disables the write fault function thus allowing the drive to perform write operations even though fault conditions exist. The following procedure describes the proper method for grounding the Write Fault signal.

CAUTION

Perform this procedure only during trouble-shooting when a write fault condition interferes with isolating the problem.

1. Remove power from drive as follows:

   a. Press START switch to stop motor and unload heads.

   b. Set CB1 to OFF.

CAUTION

Be certain to remove jumper wire when testing is complete. Failure to remove wire can result in loss of customer data.

2. Connect jumper wire between TP-C642 (Write Fault) on _RUX/_PGX board and TP-A260 (ground) on __PGX board or TP-D259 (ground) on _RUX board.

3. Power up drive and perform tests. Monitor TP-C643 (Fault) on __RUX/_PGX board to determine if write fault condition persists. When testing is complete, remove jumper wire.

4302 - WRITE PLO CHECK

This procedure checks the operation of the write PLO. The PLO provides timing signals used, during write operations, by both the drive and controller.

1. Connect oscilloscope and observe that 1.612 MHz Clock frequency is approximately as shown on figure 4-6.

2. Connect oscilloscope and observe that 9.67 MHz Clock frequency is approximately as shown on figure 4-7.

3. Connect oscilloscope and observe that 2F Write Oscillator timing is approximately 19.34 MHz (see figure 4-8).

4. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP B835 PIN 15 ON _RUX/_PGX	1.612 MHZ CLK
CH 2			

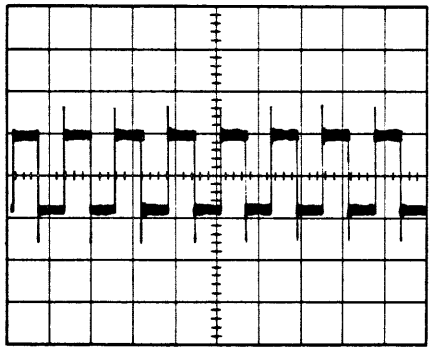
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM MODE:

NOTES:



10R155A

Figure 4-6. 1.612 MHz Clock Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D242 PIN 15 ON _RUX/_PGX	+9.67 MHZ CLK
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.1 µS/CM MODE:

NOTES:

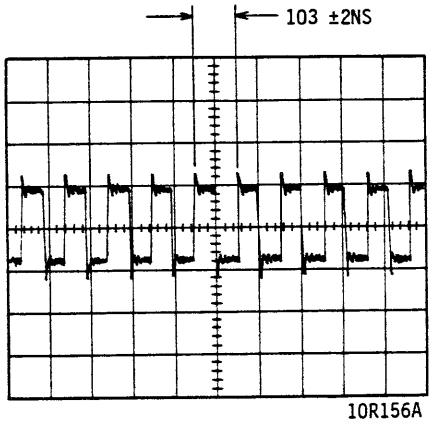


Figure 4-7. 9.67 MHz Servo Clock Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.2 V/CM	CHIP B835 PIN 2 ON _RUX/_PGX	+2F WRT OSC
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.05 µS/CM MODE:

NOTES:

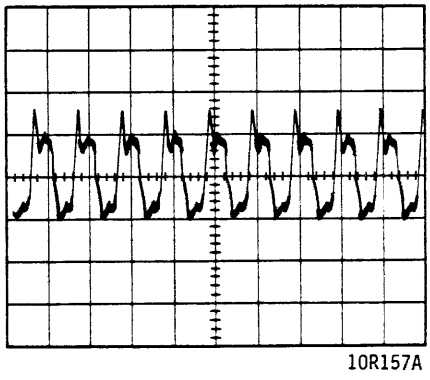


Figure 4-8. 2F Write Oscillator Timing

4303 - WRITE DATA CHECK

This procedure checks for the presence of write data at various points in the write circuits (see figure 4-5). If the signals at these points are correct, it indicates the circuits are performing their basic functions. This procedure will normally be performed because of a write problem. In that case, a write fault condition may exist and it will be necessary to perform procedure 4301 - Write Fault Grounding to perform a write operation.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

1. Command drive to seek to desired cylinder and select desired head.

2. Command drive to write a 1010... pattern.

3. Connect oscilloscope and observe that Write Gate and Write Enable appear as shown on figure 4-9.

4. Check inputs to write encoder and compensation circuits. Timing relationships between these signals, NRZ write data and write clock, must be correct before encoding and write compensation can be properly performed.

   a. Connect oscilloscope as shown on figure 4-10 and observe that Write Clock frequency is approximately 9.67 MHz.

   b. Observe that timing relationship between Write Data (NRZ) and Write Clock is similar to that on figure 4-10. Write Clock should go positive at approximately the center of the data "1" pulses.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	CHIP D249 PIN 7 ON _RUX/_PGX	+WRT GATE
CH 2	2.0 V/CM	CHIP G456 PIN 5 ON _RUX CHIP J940 PIN 1 ON _PFX	-WRT ENABLE

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.1 MS/CM MODE: ALT

NOTES:

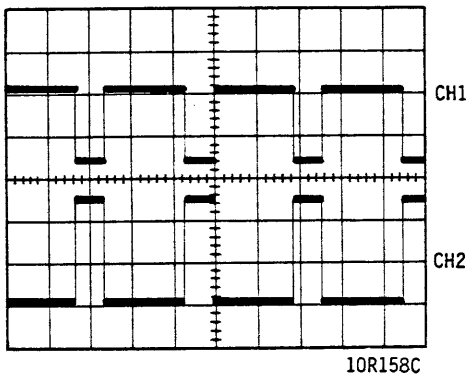


Figure 4-9. Write Gate Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D223 PIN 36 ON _RUX/_PGX	+WRT DATA (NRZ)
CH 2	0.5 V/CM	CHIP D223 PIN 38 ON _RUX/_PGX	+WRT CLK

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50NS/CM MODE: ALT

NOTES:

1. DISREGARD ANY GHOST IMAGES.

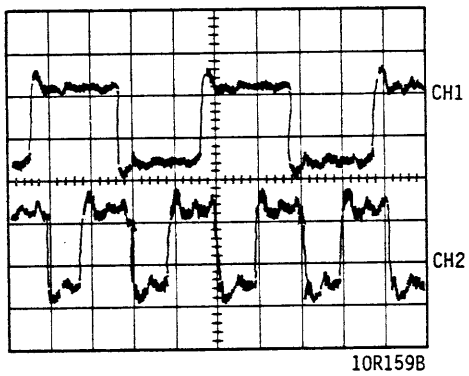


Figure 4-10. Write Data to Clock Timing

5. Check input to write driver and current control circuits.

   a. Connect oscilloscope as shown on figure 4-11.

   b. Observe that Write Data (Compensated) pulses are similar to those on figure 4-11.

6. Check output of write driver and current control circuits. This ensures that data is being sent to the read/write preamplifier.

   a. Connect oscilloscope as shown in figure 4-12.

   b. Observe that signals are approximately as shown on figure 4-12.

7. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D233 PIN 24 ON _RUX/_PGX	+WRT DATA COMP
CH 2	0.5 V/CM	CHIP B835 PIN 2 ON _RUX/_PGX	+2F WRT OSC

TRIGGERING:

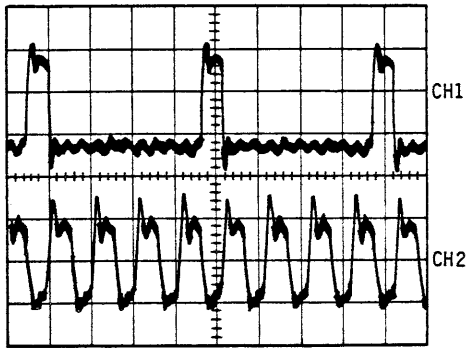
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.05 µS/CM MODE: ALT

NOTES:

1. DISREGARD ANY GHOST IMAGES.



10R160B

Figure 4-11. Compensated Write Data Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D233 PIN 24 ON _RUX/_PGX	+WRT DATA COMP
CH 2	0.2 V/CM	CHIP J832 PIN 3 ON _RUX CHIP N504 PIN 3 ON _PFX	+RD/WRT DATA

TRIGGERING:

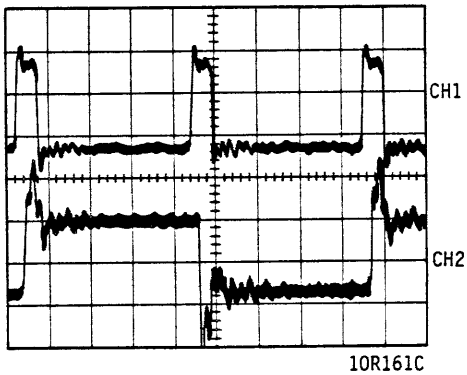
SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH2		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.1 µS/CM MODE: ALT

NOTES:

1. DISREGARD ANY GHOST IMAGES.



10R161C

Figure 4-12. Write Driver Output

4304 - WRITE ADDRESS MARK CHECK

This procedure verifies that the drive is not writing during the time that Address Mark Enable is active.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

1. Command continuous write format with address mark operations using a 1010... data pattern.
2. Connect oscilloscope as shown on figure 4-13.
3. Observe that there are no data "1" pulses during the time that Address Mark Enable is active.
4. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	CHIP B842 PIN 12 ON _RUX/_PGX	-AM ENABLE
CH 2	0.5 V/CM	CHIP D233 PIN 24 ON _RUX/_PGX	+WRT DATA COMP

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM MODE: ALT

NOTES:

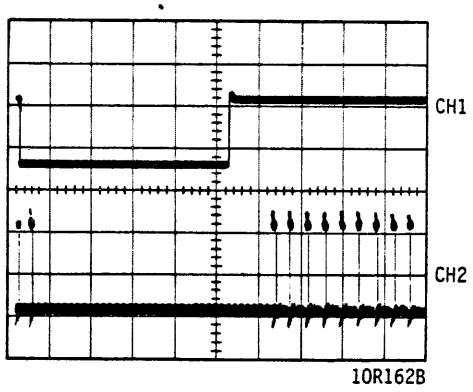


Figure 4-13. Write Address Mark Timing

4305 - WRITE CURRENT CHECK

This procedure checks for the presence of write current to the read/write preamplifier.

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

1. Command drive to seek to desired cylinder and select desired head.
2. Command a continuous write or write format operation using a 1010... pattern.
3. Connect oscilloscope and observe that signals are approximately as shown on figure 4-14.
4. Proceed to next test or prepare drive for online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-H044 ON _RUX TP-M031 ON _PFX	WRT CURRENT
CH 2	0.2 V/CM	CHIP J832 PIN 3 ON _RUX CHIP N504 PIN 3 ON _PFX	+ RD/WRT DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 µS/CM MODE: CHOP

NOTES:

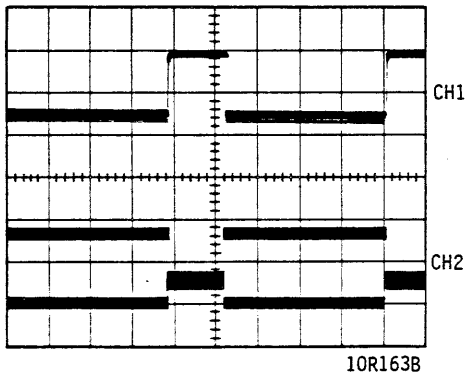


Figure 4-14. Write Current Timing

READ CHECKS

The following procedures, 4401 through 4404, check various aspects of drive read circuit operation. Figure 4-15 is a block diagram showing the major components in the read circuits and the test points used in the procedures.

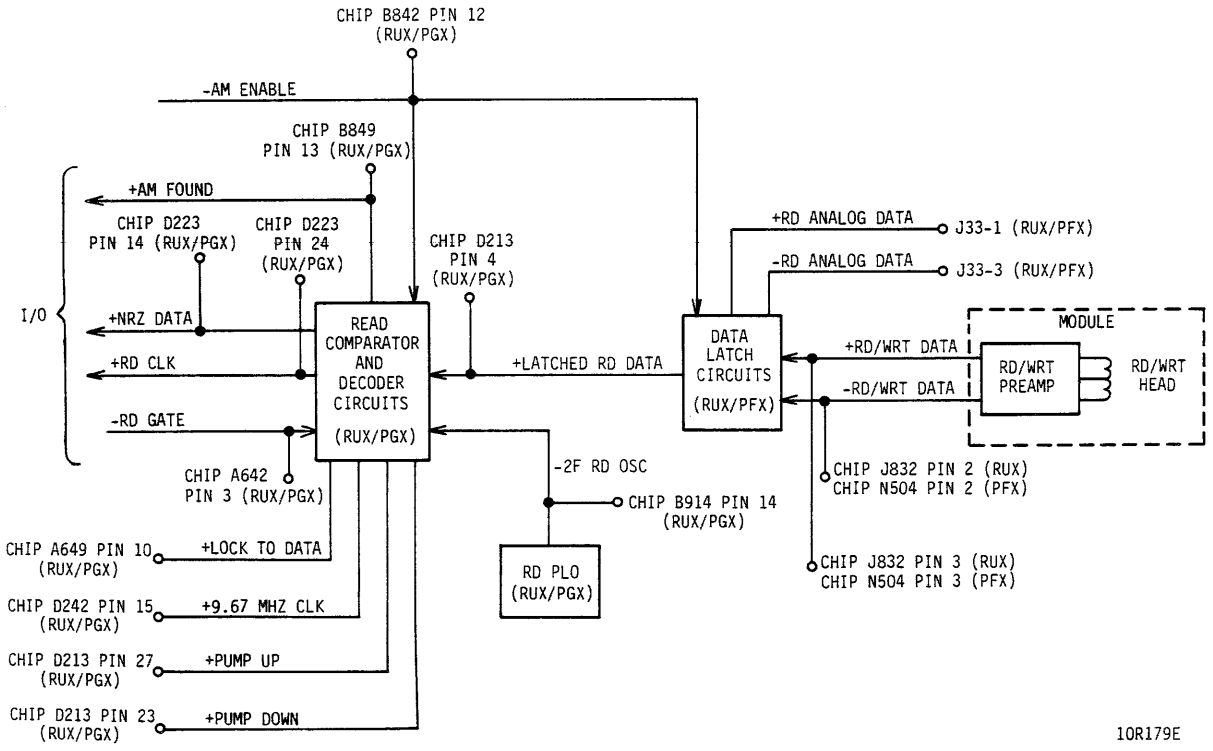


Figure 4-15. Read Circuits Test Points

4401 - READ PLO CHECK

This procedure checks the operation of the read PLO circuits (see figure 4-15). The read PLO provides timing signals used during read operations.

1. Connect oscilloscope as shown on figure 4-16 and observe that 2F Read Oscillator frequency is approximately 19.34 MHz.

2. Connect oscilloscope as shown on figure 4-17 and observe that the + Pump Up and + Pump Down signals are coincident.

3. Command drive to write a 1010... pattern using any head.

4. Command drive to perform continuous read operations.

5. Observe that + Pump Up and + Pump Down signals have the same timing relationship shown on figure 4-18.

6. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP B914 PIN 14 ON _RUX/_PGX	-2F RD OSC
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE:

NOTES:

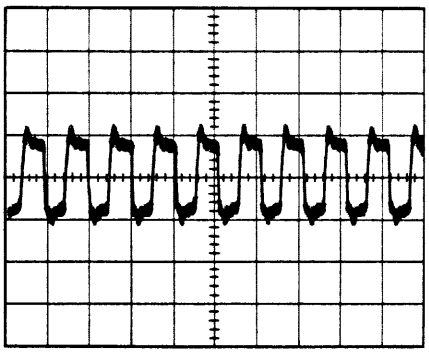


Figure 4-16. 2F Read Oscillator Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D213 PIN 27 ON _RUX/_PGX	+PUMP UP
CH 2	0.5 V/CM	CHIP D213 PIN 23 ON _RUX/_PGX	+PUMP DOWN

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

1. MEASUREMENT IS VALID ONLY IF DRIVE IS NOT READING
2. OBSERVE THAT CH1 AND CH2 SIGNALS ARE COINCIDENT.

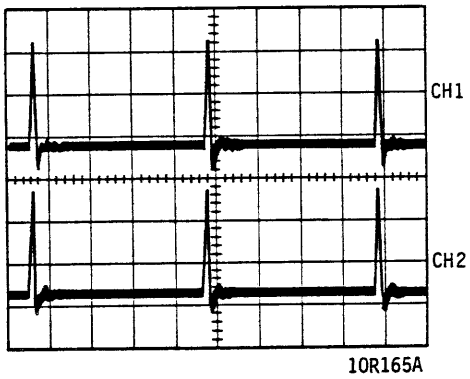


Figure 4-17. Pump Up/Down Timing (Not Reading)

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D213 PIN 27 ON _RUX/_PGX	+PUMP UP
CH 2	0.5 V/CM	CHIP D213 PIN 23 ON _RUX/_PGX	+PUMP DOWN

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

1. SIGNALS ARE OUT OF PHASE DURING READ

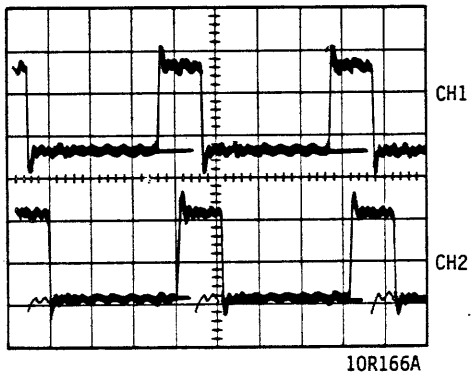


Figure 4-18. Pump Up/Down Timing (Reading)

4402 - READ DATA CHECK

This procedure checks the operation of the heads, preamplifier, data latch, read comparator, and 2-7 decoder circuits.

1. Perform Write Data Check (proc 4303).

2. Perform Read PLO Check (proc 4401).

CAUTION

To avoid possible loss of customer data, select a cylinder and head that will result in data being written on an unused track.

3. Command drive to seek to desired cylinder and select desired head.

4. Command drive to write a 1010... pattern and then to perform continuous read operations.

5. Check output of heads and preamplifier.

   a. Connect and set up oscilloscope as shown on figure 4-19.

   b. Observe that read/write data appears approximately as shown.

6. Check the Latched Read Data signal and its timing relationship with the 2F Read oscillator signal.

   a. Connect oscilloscope as shown on figure 4-20 and observe that Latched Read Data pulse width is as shown.

   b. Observe that Latched Read Data pulses are approximately coincident with 2F Read Oscillator pulses (see figure 4-20).

   c. Observe that the data pattern is correct (see figure 4-20).

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	50 MV/CM	CHIP J832 PIN 2 ON _RUX CHIP N504 PIN 2 ON _PFX	-RD/WRT DATA
CH 2	50 MV/CM	CHIP J832 PIN 3 ON _RUX CHIP N504 PIN 3 ON _PFX	+RD/WRT DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-EXT	CHIP A642 PIN 3 ON _RUX/_PGX	-RD GATE

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 20 µS/CM MODE: INVERT CH2 AND ADD

NOTES:

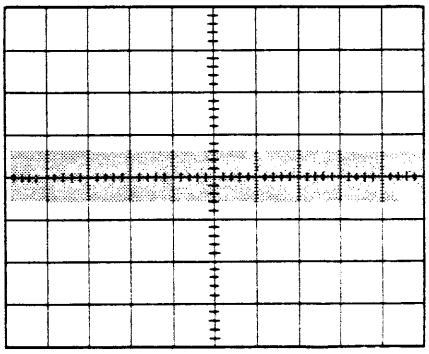


Figure 4-19. Read Preamplifier Output

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D213 PIN 4 ON _RUX/_PGX	+LATCHED RD DATA
CH 2	0.5 V/CM	CHIP B914 PIN 14 ON _RUX/_PGX	-2F RD OSC

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

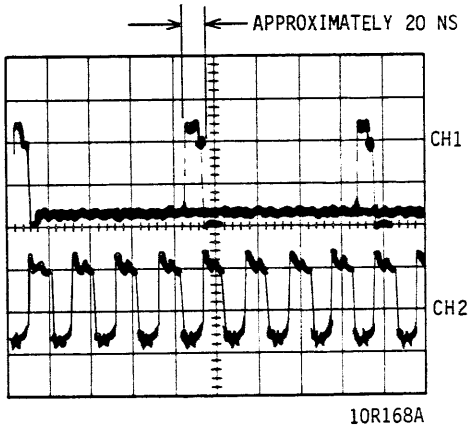


Figure 4-20. Latched Read Data Timing

7. Check Read Data to Read Clock Timing.

   a. Connect oscilloscope as shown on figure 4-21 and observe that Read Clock frequency is approximately 9.67 MHz.

   b. Observe that Read Data to Read Clock timing is approximately as shown. Read Clock should go positive approximately at the center of the data "1" pulses.

   c. Observe that the NRZ data has a 1010... pattern.

8. Check Read Gate to Lock to Data timing.

   a. Connect oscilloscope as shown on figure 4-22.

   b. Observe that +Lock to Data goes low at the proper time (see figure 4-22).

9. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D223 PIN 14 ON _RUX/_PGX	+NRZ RD DATA
CH 2	0.5 V/CM	CHIP D223 PIN 24 ON _RUX/_PGX	+RD CLK

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 50 NS/CM MODE: ALT

NOTES:

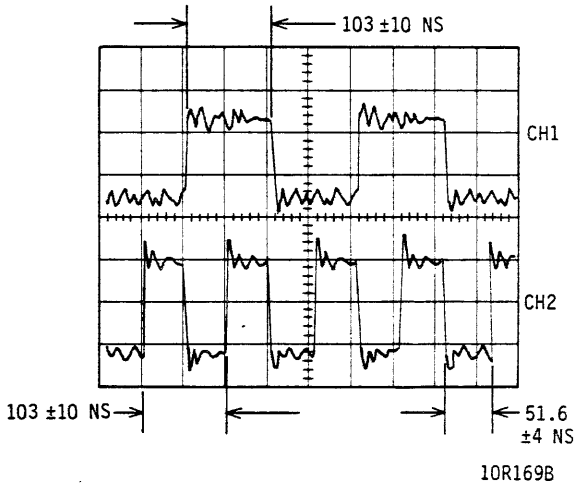


Figure 4-21. NRZ Read Data Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	CHIP A642 PIN 3 ON _RUX/_PGX	-RD GATE
CH 2	2.0 V/CM	CHIP A649 PIN 10 ON _RUX/_PGX	+LOCK TO DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM MODE: ALT

NOTES:

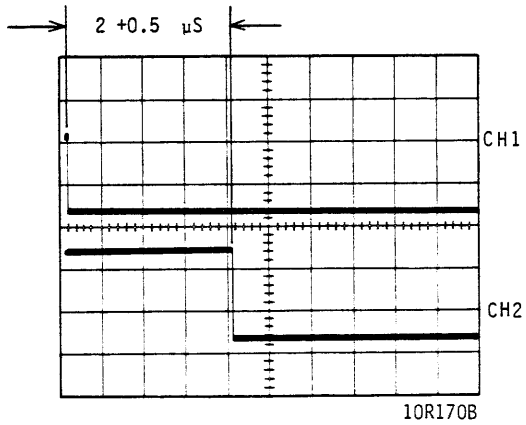


Figure 4-22. Read Gate to Lock to Data Timing

4403 - READ ADDRESS MARK CHECK

This procedure checks for the presence of address marks and verifies that the timing is correct.

CAUTION

To avoid possible loss of customer data, select a head and cylinder that will result in data being written on an unused track.

1. Command a write format in address mark mode using a 1010.. pattern. Then command a continuous read address mark operation.

2. Connect oscilloscope as shown on figure 4-23.

NOTE

In "A Intensified" horizontal mode, the brightened marker highlights the segment of the sweep that is displayed later in "B Delayed" horizontal mode.

3. Adjust DELAY TIME MULTIPLIER on oscilloscope to move intensified marker into data pattern (see figure 4-23). To minimize display instability, use first address mark area following index.

4. Referring to figure 4-24 position oscilloscope HORIZ DISPLAY switch to B DELAYED and TRIGGERING to +EXT CH I.

5. Check that the length of the address mark area is within the limits shown on figure 4-24. If it is outside these limits, the address mark detection circuits may not function properly.

6. Observe that Address Mark Found goes active immediately following the address mark area.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D213 PIN 4 ON _RUX/_PGX	+LATCHED RD DATA
CH 2	2.0 V/CM	CHIP B849 PIN 13 ON _RUX/_PGX	+AM FOUND

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+EXT CH1	TP-M (E329) ON BEBN TP-M (C809) ON _EBN TP-F ON _EDN	+INDEX

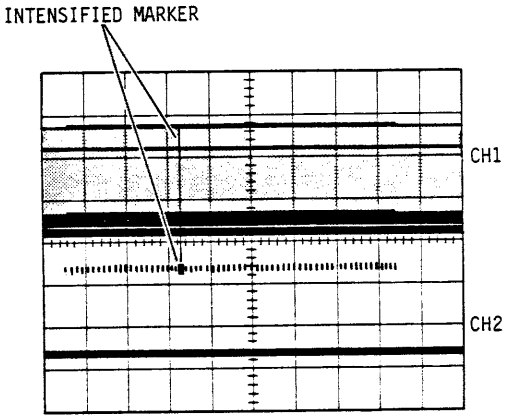
SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

A TIME/DIV: 2 MS/CM MODE:

B TIME/DIV: 0.5 µS/CM

NOTES:

1. SET HORIZONTAL DISPLAY TO "A" INTENSIFIED AND ADJUST DELAY TIME MULTIPLIER TO MOVE MARKER TO ADDRESS MARK.



10R171C

Figure 4-23. Scope Setup for AM Found Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	0.5 V/CM	CHIP D213 PIN 4 ON _RUX/_PGX	+LATCHED RD DATA
CH 2	2.0 V/CM	CHIP B849 PIN 13 ON _RUX/_PGX	+AM FOUND

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+EXT CH1	TP-M (E329) ON BEBN TP-M (C809) ON _EBN TP-F ON _EDN	+INDEX

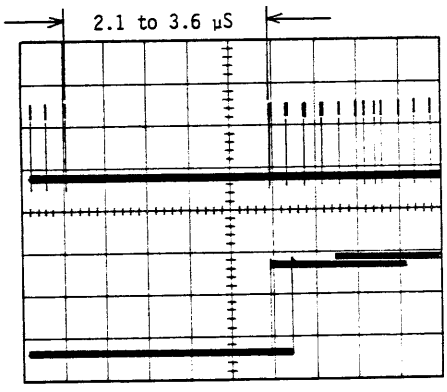
SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

A TIME/DIV: 2 MS/CM MODE:

B TIME/DIV: 0.5 µS/CM

NOTES:

1. SET HORIZONTAL DISPLAY TO "B" (DELAYED) AND ADJUST DELAY MULTIPLIER AS REQUIRED.



10R172C

Figure 4-24. AM Found Timing

7. Connect oscilloscope as shown on figure 4-25.

8. Observe that +Lock to Data goes active at the proper time (see figure 4-25).

9. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	CHIP B842 PIN 12 ON _RUX/_PGX	-AM ENABLE
CH 2	2.0 V/CM	CHIP A649 PIN 10 ON _RUX/_PGX	+LOCK TO DATA

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
-INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE X10 PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM MODE: ALT

NOTES:

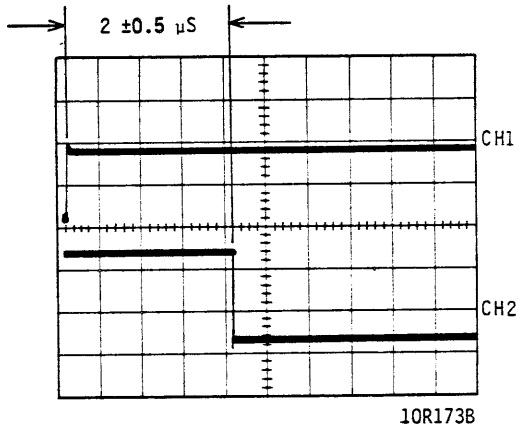


Figure 4-25. AM to Lock To Data Timing

MISCELLANEOUS LOGIC CHECKS

4501 - INDEX CHECK

This procedure checks that Index is present and has the proper pulse width. It also checks the time between successive Index pulses which is an indication of disk pack rotational speed.

1. Connect oscilloscope as shown on figure 4-26.
2. Observe that the Index pulse width is between 2.2 and 2.8 microseconds.
3. Connect oscilloscope as shown on figure 4-27.
4. Observe that the time between Index pulses is between 16.5 and 16.8 milliseconds.
5. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-M (E329) ON BEBN	+INDEX
		TP-M (C809) ON _EBN	
		TP-F ON-EDN	
CH 2			

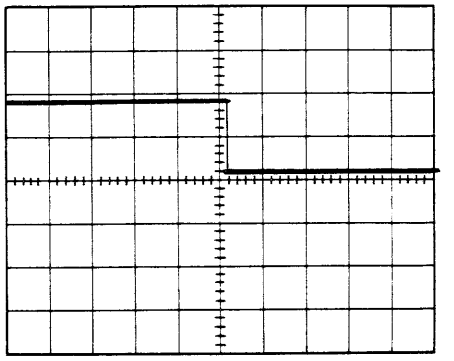
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM MODE:

NOTES:



10R174A

Figure 4-26. Index Pulse Timing

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/CM	TP-M (E329) ON BEBN	+INDEX
		TP-M (C809) ON _EBN	
		TP-F ON _EDN	
CH 2			

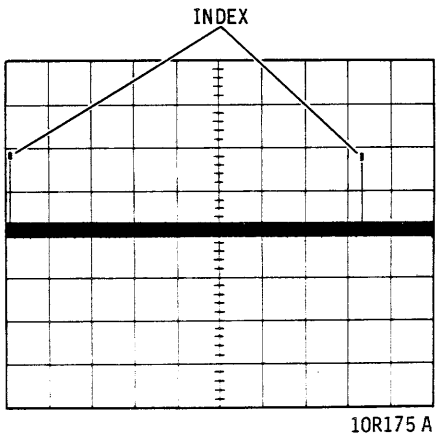
TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 2 MS/CM MODE:

NOTES:



10R175 A

Figure 4-27. Index to Index Timing

4502 - SECTOR CHECK

This procedure checks for the presence of sector pulses and that they have the proper width.

1. Connect oscilloscope as shown on figure 4-28.

2. Observe that the Sector pulse width is between 1.05 and 1.45 microseconds.

3. Proceed to next test or return drive to online operation.

OSCILLOSCOPE SETUP

INPUT:

CHANNEL	VOLTS/DIV	CONNECTION	SIGNAL NAME
CH 1	2.0 V/cm	CHIP H815 PIN 19 ON-PXX	+SECTOR
CH 2			

TRIGGERING:

SLOPE/SOURCE	CONNECTION	SIGNAL NAME
+INT CH1		

SCOPE GND TO GND ON LOGIC CARD.
USE XIO PROBES UNLESS OTHERWISE NOTED.

TIME/DIV: 0.5 µS/CM MODE:

NOTES:

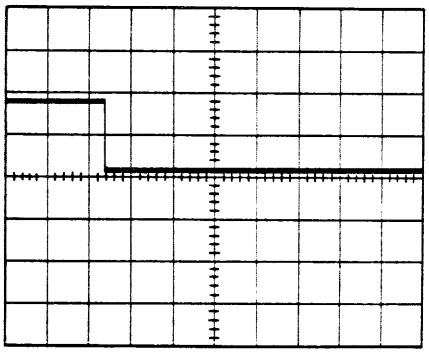


Figure 4-28. Sector Pulse Timing

SECTION 5

REPAIR AND REPLACEMENT

REPAIR AND REPLACEMENT 5

CAUTION

When servicing the drive, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual. Failure to observe these precautions can result in serious damage to electronic assemblies.

INTRODUCTION

Repair of the drive is limited to replacement of defective parts and assemblies. This section describes removal and replacement and, where applicable, adjustment of all major field replaceable parts and assemblies. The information here should be used in conjunction with that in the parts data section of hardware maintenance manual, volume 1.

If adjustments are required as a result of replacing a part, it is specified in the replacement procedure. If an adjustment is included, and there is some doubt as to the need for replacement, perform the adjustment prior to replacing the part.

The procedures in this section assume that the drive is mounted on slides in an equipment rack or cabinet. But unless otherwise specified, it is not necessary to remove the drive from the slides to perform maintenance. All procedures require that power be removed from the drive and power supply. The person performing the maintenance should be thoroughly familiar with the operation of the drive and with all information in the general maintenance section of this manual (particularly warnings and precautions).

Each procedure is assigned a unique number. The numbers are used elsewhere in the manual to reference the procedures. The procedures and numbers are organized into three categories: 51XX - mechanical, 52XX - electromechanical, and 53XX - electronic (circuit boards).

- 5101 - Entire Drive Removal & Replacement
- 5102 - Top Cover Removal & Replacement
- 5103 - Front Panel Removal & Replacement
- 5104 - Slide Removal & Replacement
- 5201 - Fan Removal & Replacement
- 5202 - Operator Panel (_PBX) Removal & Replacement
- 5203 - Brake Removal, Replacement, & Adjustment
- 5204 - Power Supply Removal & Replacement
- 5205 - Locking Solenoid Coil Removal & Replacement
- 5206 - Module Removal & Replacement
- 5207 - Cable Replacement
- 5208 - Motor Assembly Removal & Replacement
- 5301 - Control Board (_PXX) Removal & Replacement
- 5302 - I/O Board (_EBN/_EDN) Removal & Replacement
- 5303 - Read/Write PLO Board (_PGX) Removal & Replacement
- 5304 - Data Latch Board (_PFX) Removal & Replacement
- 5305 - Motor Speed Control Board (_PMX) and Power Amp Board (_QHX) Removal & Replacement
- 5306 - Read/Write Board (_RUX) Removal & Replacement

5101 - ENTIRE DRIVE REMOVAL & REPLACEMENT

The following procedure provides instructions for removing and replacing the entire drive and assumes that the drive is mounted on slides in an equipment rack. If the drive is to be replaced with another and the inner slides are required for the replacement unit, see procedure 5104 - Slide Removal & Replacement. Two persons may be required to lift the drive on and off the slide assemblies.

REMOVAL

NOTE

For drives with remote power supply mounted on slides (rear of drive), perform step 1 and skip to step 7. For drives with integral power supply, begin with step 2.

1. Perform power supply removal procedure (5205).
2. Lift cabinet latch and pull drive to fully extended position.
3. Remove power from drive as follows:
   a. Press START switch to release it from Start position.
   b. Wait for Ready indicator to stop flashing and set CB1 to OFF.
4. Disconnect ac power cable from AC INPUT connector J1 on power supply.
5. Remove system ground cable(s) from power supply.
6. Remove I/O shield (if used) from I/O plate (see figure 5-8).
7. Disconnect external I/O cables from connectors on I/O plate.

CAUTION

Remove terminator by hand. It could be damaged if a pliers or other tool is used.

8. Remove terminator(s) from connector(s) on I/O plate.
9. Press slide lock release and pull drive forward until it is free of slide assemblies.
10. Move drive to desired location.

REPLACEMENT

1. Push intermediate slides on equipment rack to fully retracted positions inside outer slides.

2. Lift drive into position in front of rack and guide inner slides into intermediate slides. Push until lock releases engage; then pull drive to fully extended position.

3. Connect external I/O cables and terminator(s) to connectors on I/O plate.

NOTE

For drives with remote power supply, perform step 4 and skip to step 8. For drives with integral power supply, skip step 4.

4. Perform power supply replacement procedure (5204).

5. Install I/O shield (if used) on I/O plate with attaching hardware.

6. Attach system ground cable(s) to power supply.

7. Connect ac power cable to AC INPUT connector J1 on power supply.

8. Return drive to closed position in rack.

5102 - TOP COVER REMOVAL & REPLACEMENT

REMOVAL

CAUTION

With the top cover removed, electrostatic sensitive components are exposed and may be seriously damaged by static electricity. To avoid possible damage, observe all precautions listed under Electrostatic Discharge Protection in section 2 of this manual.

1. Lift cabinet latch and pull drive to fully extended position.
2. Remove power from drive as follows:
   a. Press START switch to release it from Start position.
   b. Wait for Ready indicator to stop flashing and set CB1 to OFF.
3. Remove screws securing cover to drive.

CAUTION

Cover must be carefully lifted from the center to avoid possible damage to adjacent components.

4. Lift off cover.

REPLACEMENT

CAUTION

When replacing cover, use care to avoid damaging logic boards.

1. Install cover on drive with attaching screws.
2. Return drive to closed position in rack.

5103 - FRONT PANEL REMOVAL & REPLACEMENT

REMOVAL

1. Remove power from drive as follows:

   a. Press START switch to release it from Start position.

   b. Wait for Ready indicator to stop flashing and set CB1 to OFF.

2. Remove front panel insert (see figure 5-1) by pulling it forward to disengage catches that hold it in place.

3. Remove primary filter.

4. Remove screws securing front panel to drive and lift panel off drive.

REPLACEMENT

1. Install front panel (center over switches) with attaching hardware.

2. Install primary filter.

3. Replace front panel insert by aligning catches with slots in front panel and pushing on insert until catches snap in place.

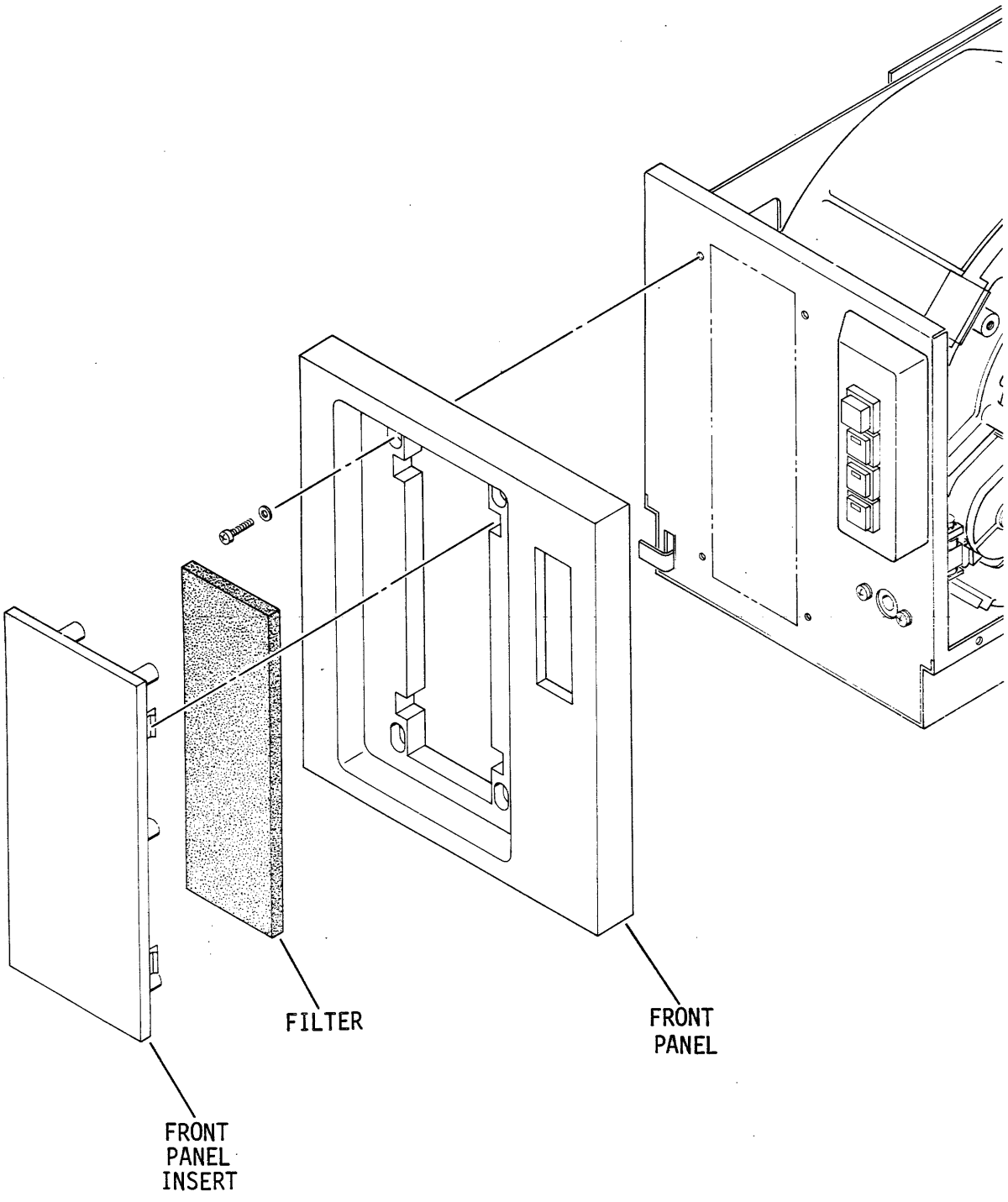


Figure 5-1. Front Panel Removal and Replacement

5104 - SLIDE REMOVAL & REPLACEMENT

The following procedure describes how to remove and replace the inner slide assemblies. This procedure is used to replace a defective inner slide or if the inner slides must be removed from one drive and installed on another.

REMOVAL

1. Perform entire drive removal procedure (5101).
2. Remove remote power supply mounts (if used) by removing attaching hardware (see figure 5-7).
3. Remove screws securing slides to drive (and to integral power supply, if used) and remove slides (see figure 5-2).

REPLACEMENT

1. Mount inner slides on drive (and integral power supply, if used) by installing screws through holes in inner slides into square nuts in drive. Refer to figure 5-2 to determine which slide component is used on the right-hand side of the drive.
2. Install remote power supply mounts (if used) with attaching hardware.
3. Perform entire drive replacement procedure (5101).

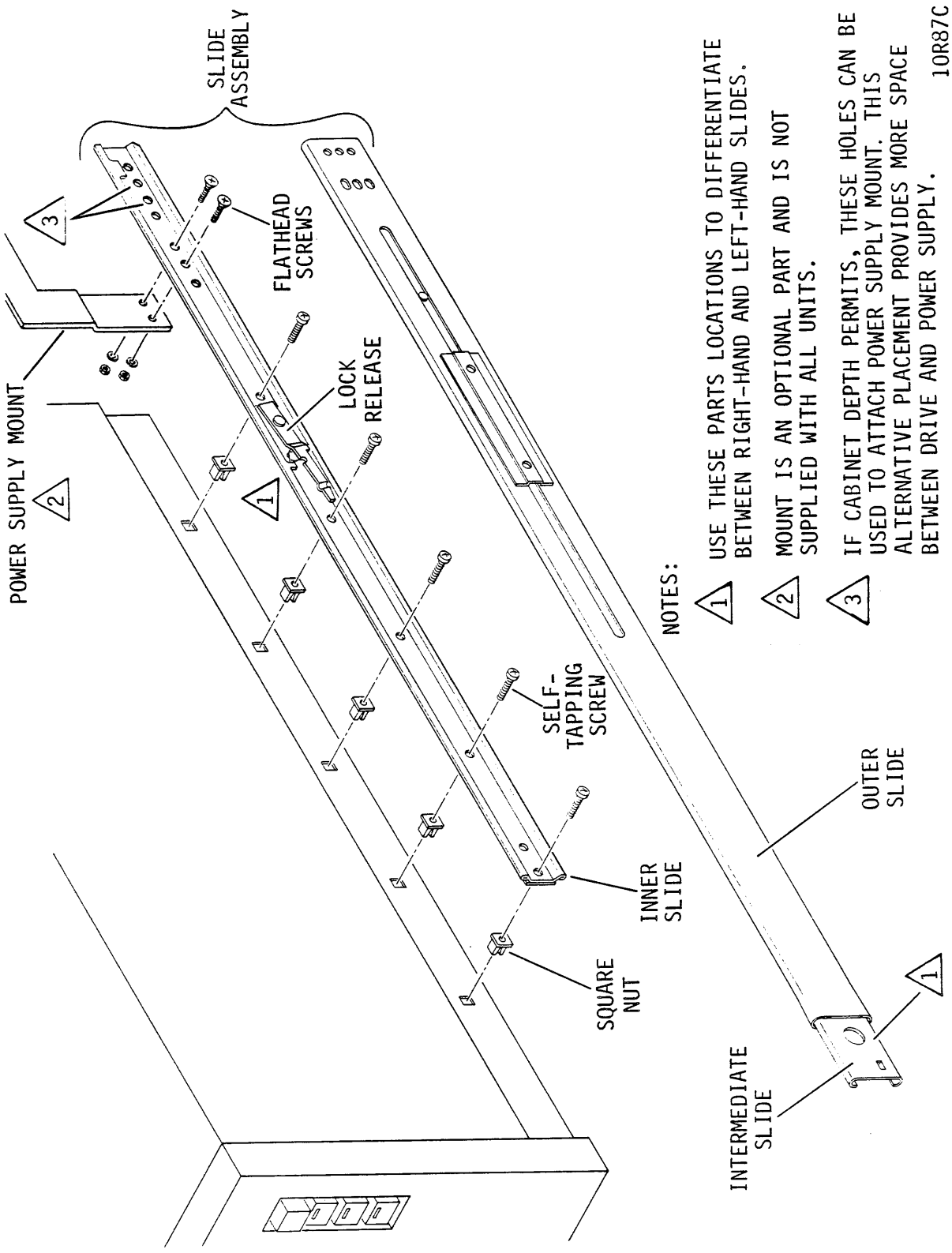


Figure 5-2. Slide Removal and Replacement

5201 - FAN REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).

2. Remove power supply as follows:

   a. For drives with integral power supply, perform power supply removal procedure (5204).

   b. For drives with remote power supply attached directly to slides, remove screws securing front of power supply to slides and tilt supply back far enough to allow access to fan hardware.

   c. For drives with remote power supply attached to bracket and mounts, remove hardware securing bracket to mounts and slide supply back far enough to allow access to fan hardware.

   NOTE

   Cable J48 from fan to I/O board is on newer drives only.

3. Disconnect cable from connector J48 (if used) on I/O board (_EBN/_EDN).

   NOTE

   Cable J38 from dc harness to fan is on older drives only.

4. Disconnect cable from connector J38 (if used) on fan (see figure 5-3).

5. Remove screws attaching board bracket and move bracket and board assembly forward to allow fan removal.

6. Remove screws securing outer finger guard and fan to drive. Remove guard and fan.

7. Remove screws attaching inner finger guard to fan. Remove guard.

REPLACEMENT

1. Install inner finger guard on fan with attaching hardware.

CAUTION

Installing fan backwards will result in improper airflow, which will cause overheating and premature component failure. Orient older fans so P38 contacts are on upper left when facing rear of drive. Orient newer fans so P48 leads are on lower left when facing rear of drive .

2. Align fan to inside, and finger guard to outside, of rear panel. Attach and tighten securely with screws.

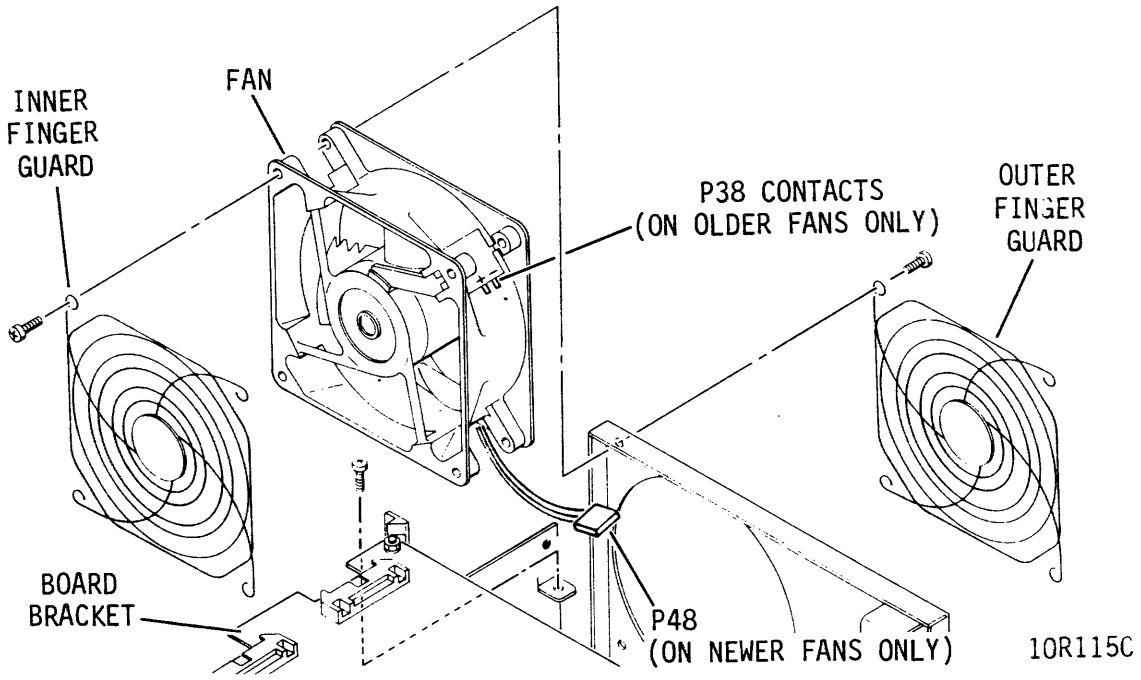


Figure 5-3. Fan Removal and Replacement

NOTE

Early model single channel drives with CPXX or DPXX control board, or BEBN I/O board, do not have operable fan fault sense feature. Replacement fans for drives without this feature are connected via connnector J38 with 1-wire J48 connector not used. Replacement fans for drives with this feature are connected either via connector J38 and 1-wire J48 connector, or via 3-wire J48 connector.

3. On older fans, connect P38 wires to connector J38 on fan. Ensure that black wire goes to + terminal and blue wire to - terminal. On newer fans, connect cable to connector J48 on I/O board.

4. Move bracket and board assembly into position and secure with attaching hardware.

5. Replace power supply as follows:

   a. For drives with integral power supply, perform power supply replacement procedure (5204).

   b. For drives with remote power supply, move power supply into operating position and secure with mounting hardware.

6. Perform top cover replacement procedure (5102).

5202 - OPERATOR PANEL (—PBX) REMOVAL & REPLACEMENT

The operator panel cannot be repaired and, except for the lenses, must be replaced as an assembly. The lenses can be replaced separately and are removed by carefully prying them from the switches (see figure 5-4). The following describes removal and replacement of the entire operator panel.

REMOVAL

1. Perform top cover removal procedure (5102).
2. Perform front panel removal procedure (5103).
3. Remove logic plug from operator panel.
4. Disconnect cable from connector J26 on control board (_PXX) and remove cable from cable clips.
5. Remove hardware attaching switch bracket to chassis and remove operator panel and bracket assembly from drive.
6. Remove hardware attaching operator panel to switch bracket.

REPLACEMENT

1. Install operator panel on switch bracket with attaching hardware.
2. Thread P26 connector and cable through opening in front panel.
3. Install operator panel and bracket assembly on chassis with attaching hardware.
4. Connect cable to connector J26 on control board and secure cable in cable clips.
5. Insert logic plug into slot in operator panel.
6. Perform front panel replacement procedure (5103).
7. Perform top cover replacement procedure (5102).

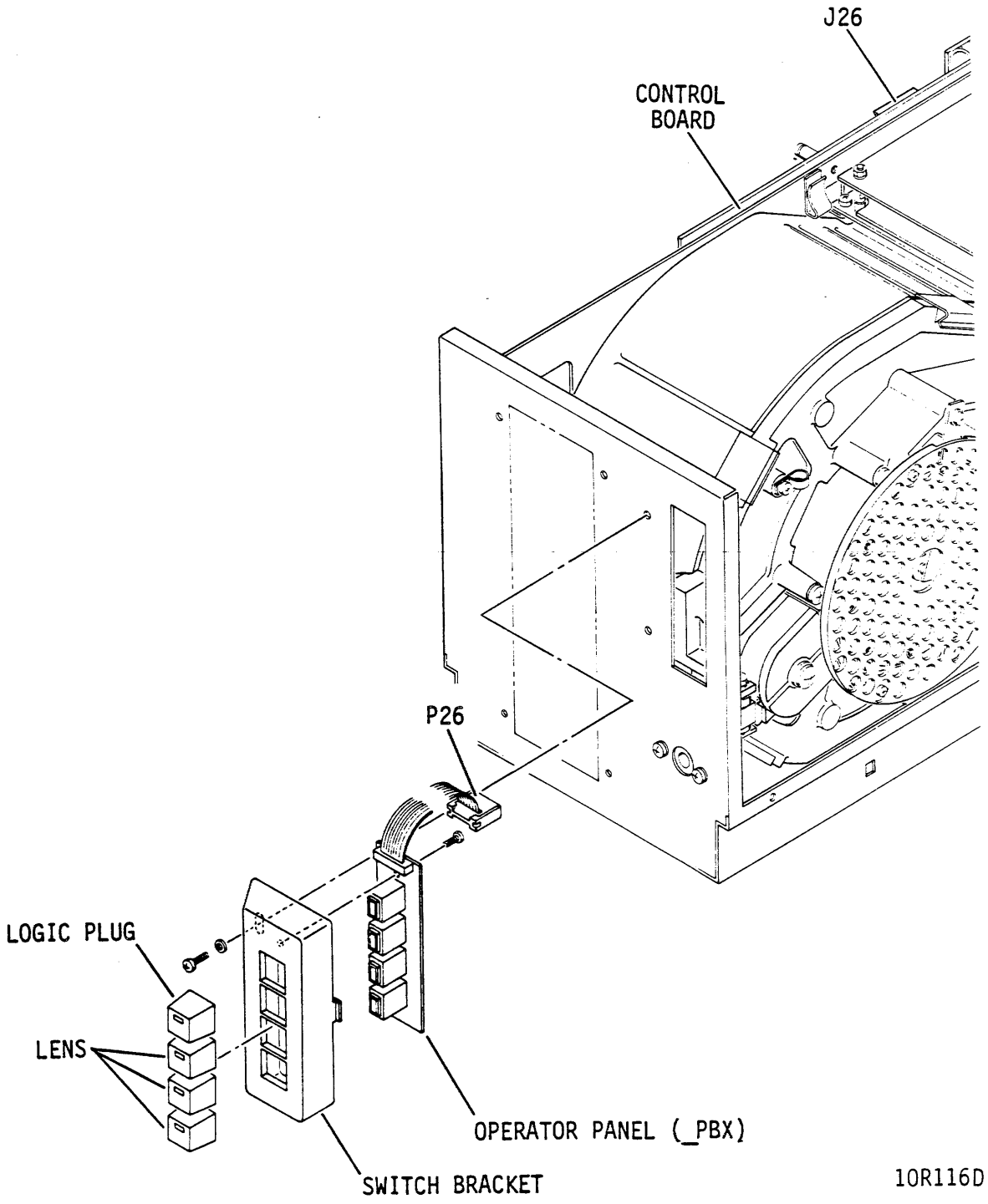


Figure 5-4. Operator Panel Removal and Replacement

5203 - BRAKE REMOVAL, REPLACEMENT & ADJUSTMENT

The brake (see figure 5-5) must be adjusted each time it is replaced, as described in the adjustment procedure below. A special brake adjustment shim (see table 2-1 for part number) is required to adjust brake.

REMOVAL

1. Perform top cover removal procedure (5102).
2. Remove motor shield by removing attaching hardware.
3. Disconnect cable from connector J43 on power amp board (_QHX).
4. Slide motor speed control board (__PMX) and power amp board (__QHX) assembly out far enough to gain access to connector J41 on motor speed control board.
5. Disconnect cable from connector J41 on motor speed control board. Remove cable from tie wraps.
6. Remove hardware attaching brake to module and lift off brake.

REPLACEMENT

1. Loosely install brake on module with attaching hardware.
2. Connect cable to connector J41 on motor speed control board. Secure cable with tie wraps.
3. Slide motor speed control board and power amp board assembly in as far as possible.
4. Connect cable to connector J43 on power amp board.
5. Perform brake adjustment procedure starting with step 4.

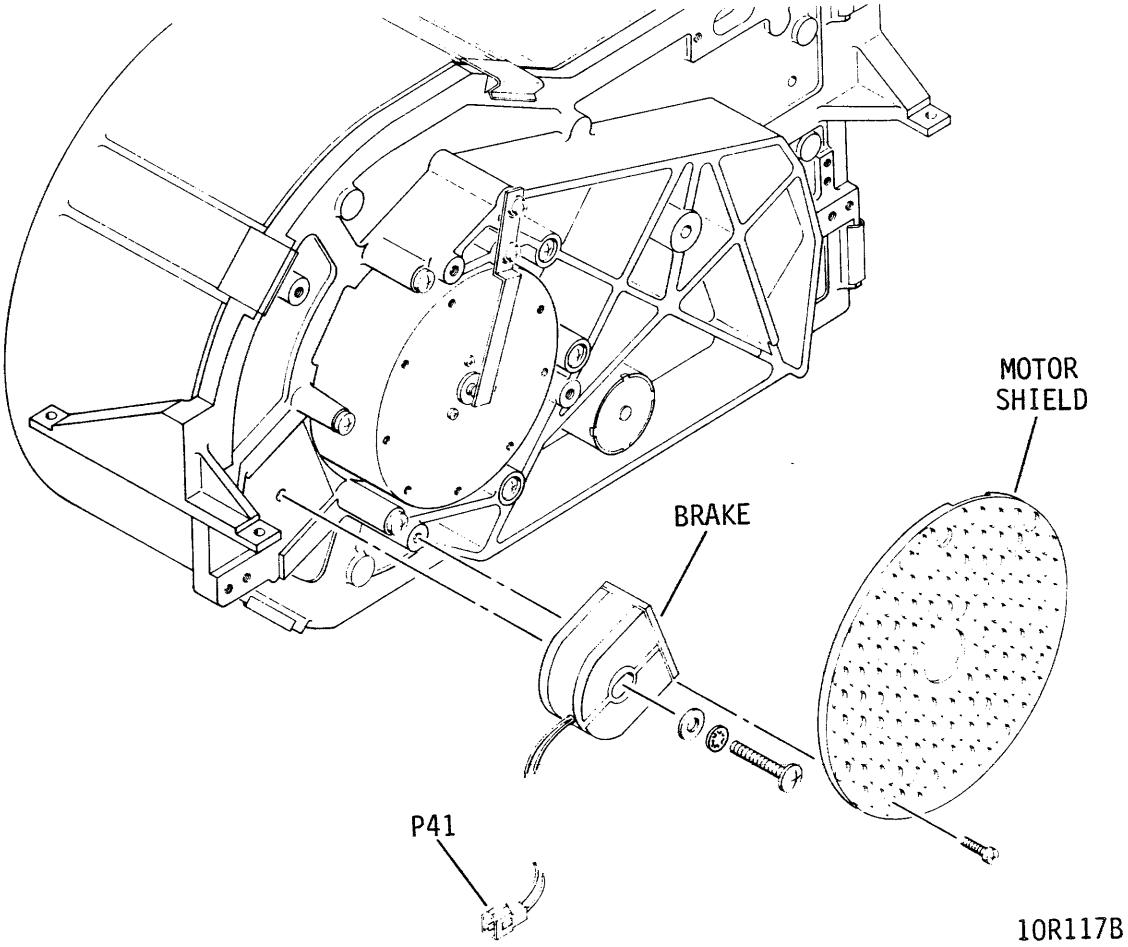


Figure 5-5. Brake Removal and Replacement

ADJUSTMENT

1. Perform top cover removal procedure (5102).
2. Remove motor shield by removing attaching hardware.
3. Loosen screw that attaches brake to module.
4. Insert brake adjustment shim between brake armature and brake housing (see figure 5-6).

NOTE

Heavy pressure may be required to make the adjustment in the following step.

5. Adjust gap between armature and housing to thickness of shim by pushing brake against motor while tightening screw to 5.3 N·m (46 lbf·in).
6. Remove shim and check adjustment.
7. Install motor shield with attaching hardware.
8. Perform top cover replacement procedure (5102).

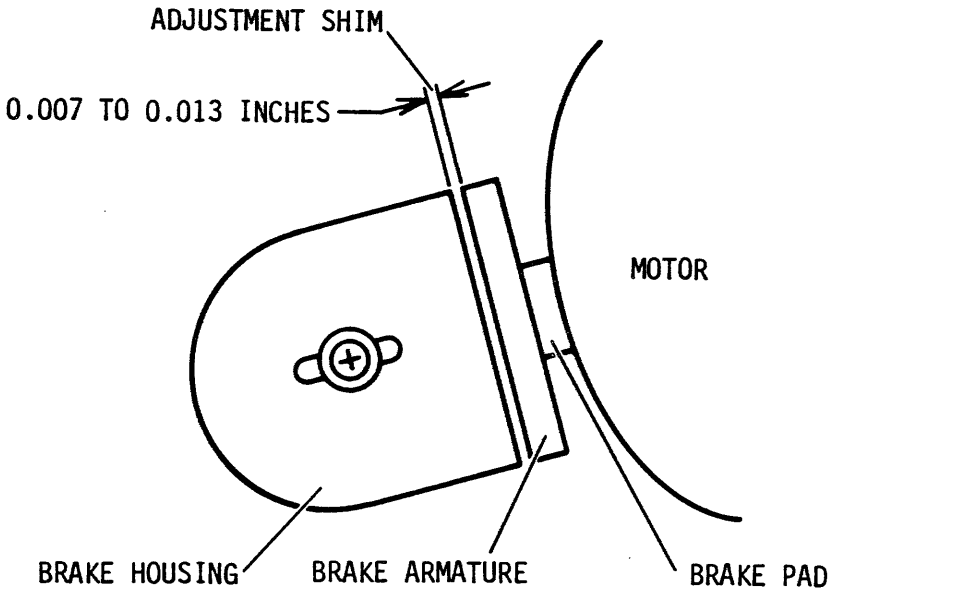


Figure 5-6. Brake Adjustment

5204 - POWER SUPPLY REMOVAL & REPLACEMENT

The following procedures provide instructions for removing and replacing the integral power supply, or remote power supply when it is slide-mounted behind the drive (see figure 5-7). A second person may be needed to support the supply while the mounting hardware is being removed and installed.

REMOVAL (REMOTE POWER SUPPLY)

1. Lift cabinet latch and pull drive to fully extended position.

2. Remove power from drive as follows:

   a. Press START switch to release it from Start position.

   b. Wait for Ready indicator to stop flashing and set CB1 to OFF.

3. Disconnect ac power cable from AC INPUT connector J1 on power supply.

4. On drives with power supply attached directly to slides, remove screws securing front of power supply to slides and tilt supply back far enough to gain access to connector J15 on power supply. On drives with power supply attached to bracket and mounts, remove hardware securing bracket to mounts and slide supply back far enough to gain access to connector J15 on power supply.

5. Disconnect cable from connector J15 on power supply.

6. Disconnect dc ground wire from power supply.

7. Remove system ground cable(s) from power supply.

8. On drives with power supply attached directly to slides, press slide lock releases and pull drive forward just enough to allow access to power supply rear mounting screws. Remove rear mounting screws.

CAUTION

After removing supply, return drive to closed position in rack unless replacement supply is to be installed immediately.

9. Remove power supply.

10. On units with mounting bracket, remove bracket from power supply.

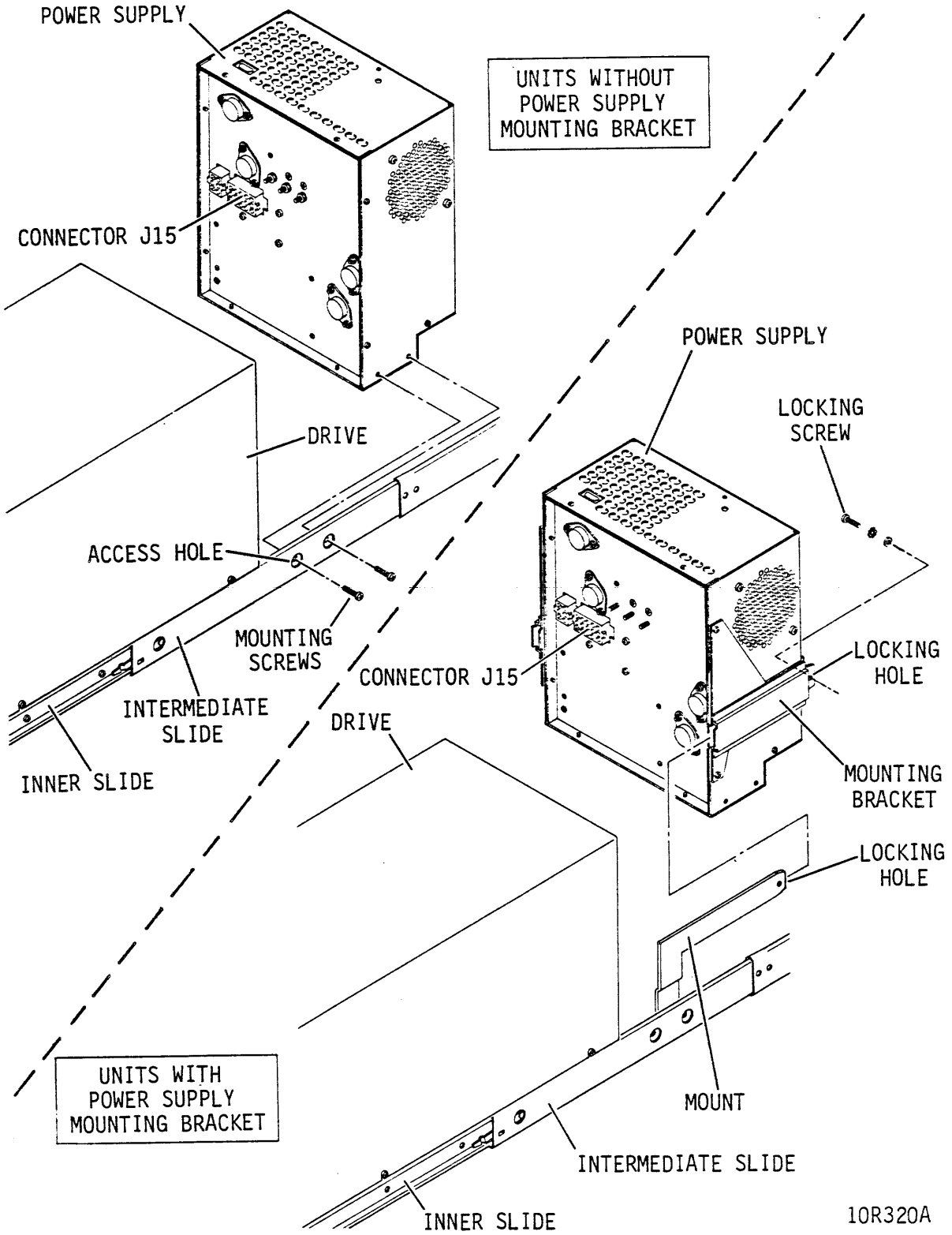


Figure 5-7. Remote Power Supply Removal and Replacement

REPLACEMENT (REMOTE POWER SUPPLY WITHOUT MOUNTING BRACKET)

1. Ensure that replacement power supply is set to correct operating voltage. If necessary, perform power supply voltage conversion procedure (see hardware maintenance manual, volume 1).

2. Press slide lock releases and pull drive forward just enough to allow power supply rear mounting screws to be installed.

3. Align holes in slides to those in power supply and secure with rear mounting screws.

4. Push drive into rack until slide lock releases engage.

5. Tilt supply back and connect cable to connector J15 on power supply.

6. Attach system ground cable(s) to power supply.

7. Connect dc ground wire to power supply.

8. Install and tighten power supply front mounting screws.

9. Connect ac power cable to AC INPUT connector J1.

10. Push drive to closed position in rack.

REPLACEMENT (REMOTE POWER SUPPLY WITH MOUNTING BRACKET)

1. Ensure that replacement power supply is set to correct operating voltage. If necessary, perform power supply voltage conversion procedure (see hardware maintenance manual, volume 1).

2. Install mounting bracket on replacement power supply.

3. Position power supply so that mounts and matching slots in bracket are aligned as shown in figure 5-7.

4. Attach system ground cable(s) to power supply.

5. Connect dc ground wire to power supply.

6. Connect cable to connector J15 on power supply.

7. Slide power supply toward drive until locking holes in bracket align with locking holes in mounts. Secure power supply bracket to mounts with mounting hardware.

8. Connect ac power cable to AC INPUT connector J1.

9. Push drive to closed position in rack.

REMOVAL (INTEGRAL POWER SUPPLY)

1. Perform top cover removal procedure (5102).
2. Perform entire drive removal procedure (5101).
3. Remove hardware attaching cover plate to power supply (see figure 5-8). Remove cover plate.
4. Remove hardware attaching I/O plate to power supply. Free I/O plate and cable assembly from power supply.
5. Remove screws securing power supply to drive rear panel and inner slide (or support bracket).
6. Move power supply away from drive (ensure that RF gasket remains attached to drive) to gain access to connector J15 on power supply.
7. Disconnect cable from connector J15 on power supply.
8. Disconnect dc ground wire from power supply.
9. Remove power supply.

REPLACEMENT (INTEGRAL POWER SUPPLY)

1. Connect dc ground wire to power supply.
2. Connect cable to connector J15 on power supply.
3. Position power supply on drive and inner slide (or support bracket) and secure into place with mounting hardware.
4. Install I/O plate and cable assembly on power supply with attaching hardware.
5. Install cover plate on power supply with attaching hardware.
6. Ensure that replacement power supply is set to correct operating voltage. If necessary, change voltage programming switch to desired setting.
7. Perform entire drive replacement procedure (5101).
8. Perform top cover replacement procedure (5102).

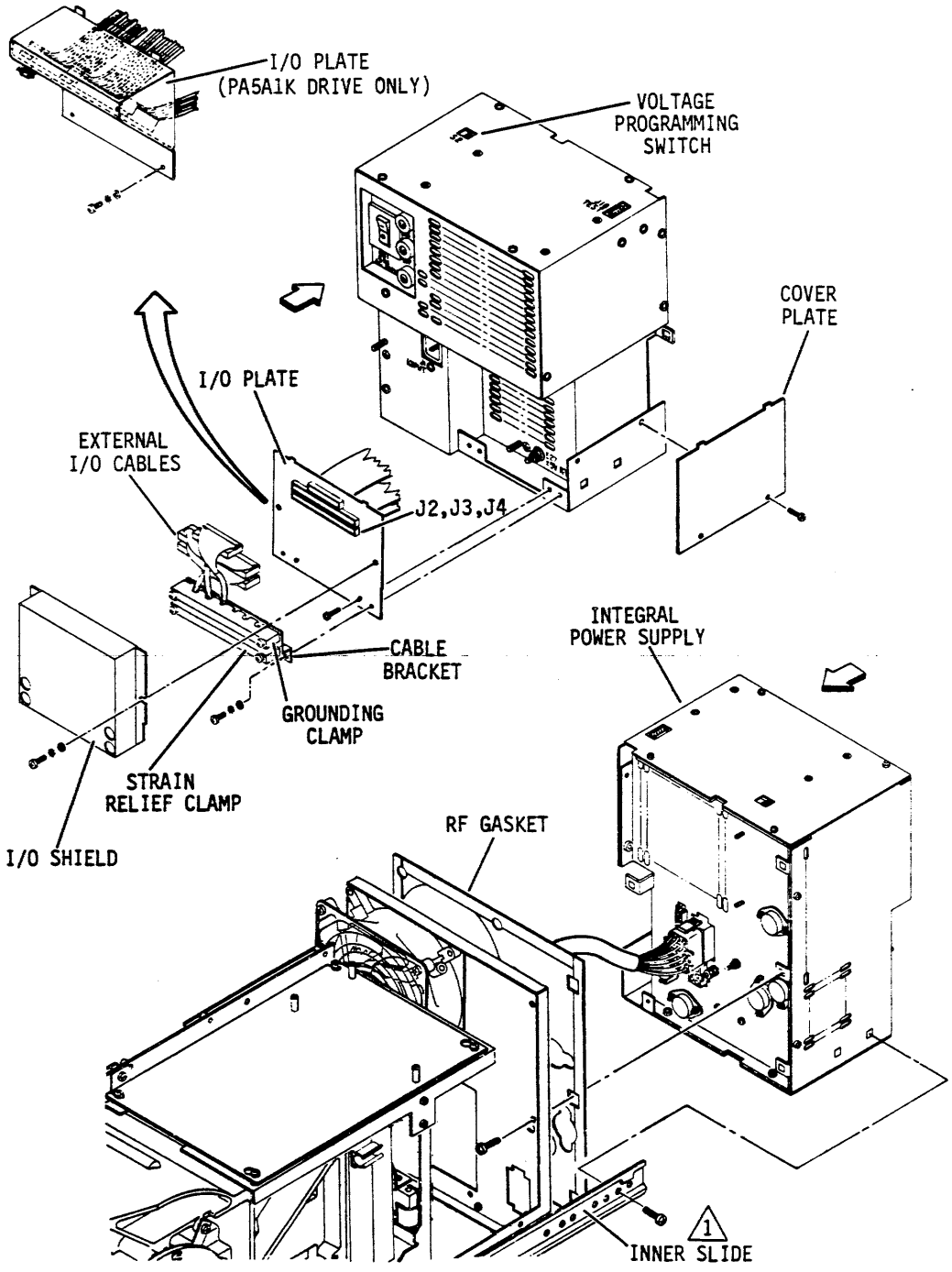


Figure 5-8. Integral Power Supply Removal and Replacement

5205 - LOCKING SOLENOID COIL REMOVAL & REPLACEMENT

This procedure describes how to replace the locking solenoid coil. The coil is contained in a metal cannister that screws into the bottom of the module (see figure 5-9). A special wrench is required to install the solenoid (see table 2-1 for part number).

CAUTION

This procedure should be performed only by qualified service personnel working in a clean dust-free environment. Any contaminants entering the module can damage the heads or disks resulting in loss of customer data.

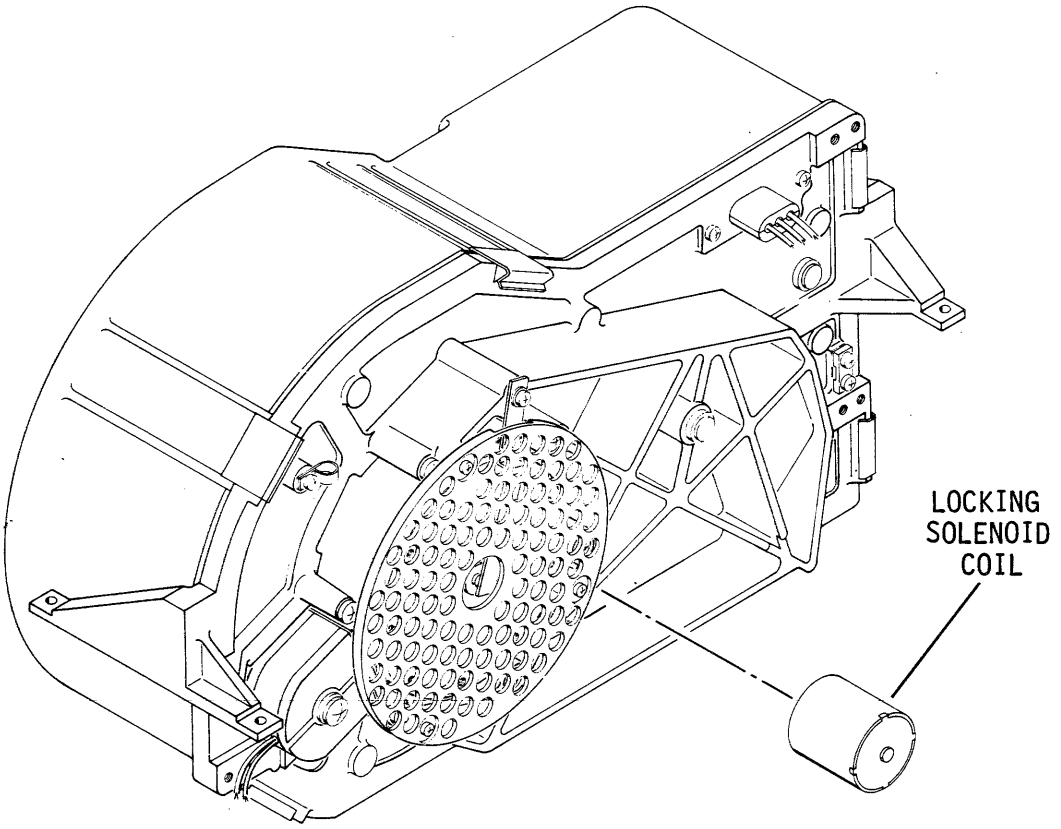
REMOVAL

1. Perform entire drive removal procedure (5101).
2. Move drive to a clean dust-free area.
3. Perform top cover removal procedure (5102).
4. Disconnect cable from connector J25 on control board (_PXX) and remove cable from cable clips.
5. Carefully clean the solenoid, and the area surrounding the base of the solenoid, with a clean, lint-free cloth.

CAUTION

To minimize chance of contamination, install new coil immediately. Do not remove new coil from its packaging until the time of installation.

6. Use solenoid wrench to unscrew locking solenoid coil from module by turning it counterclockwise.



10R111

Figure 5-9. Locking Solenoid Coil Removal and Replacement

REPLACEMENT

1. Remove new coil from its packaging.
2. Use solenoid wrench to screw solenoid coil into module. Tighten to 3.4 N·m (30 lbf·in).
3. Connect cable to connector J25 on control board and secure cable in cable clips.
4. Perform top cover replacement procedure (5102).
5. Perform entire drive replacement procedure (5101).

5206 - MODULE REMOVAL & REPLACEMENT

A temperature stabilization period of 4 or more hours may be required for the replacement module to reach the ambient temperature of the drive environment. Follow the instructions provided with module regarding temperature stabilization.

Two different module mounting methods are used in this drive. Perform the following steps to identify the module removal & replacement procedure needed for your drive.

IDENTIFICATION

1. Perform entire drive removal procedure (5101).
2. Perform top cover removal procedure (5102).
3. On motor side of module, look for either three shipping dampers or two vibration dampers. See figures 5-10 and 5-11.

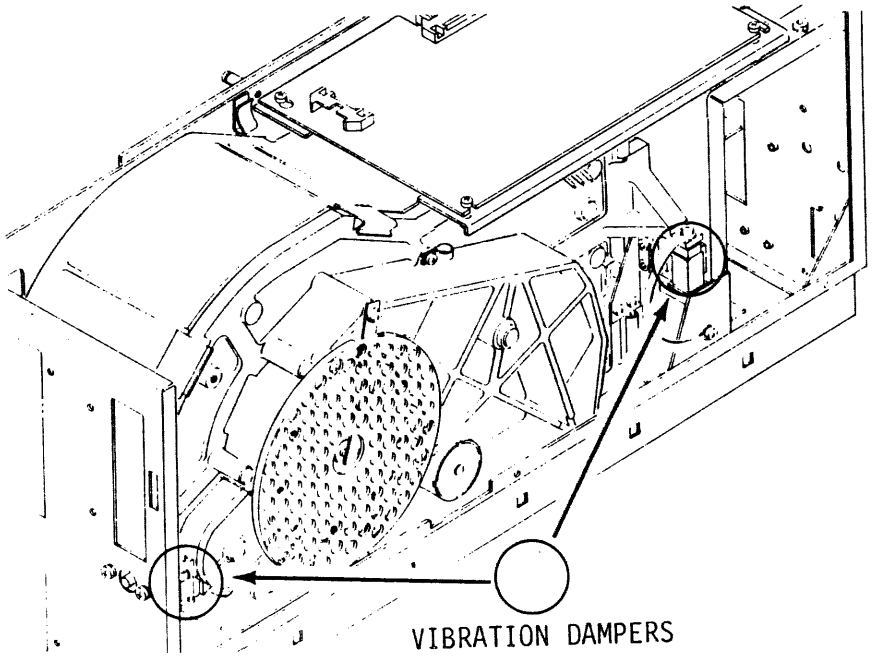


Figure 5-10. Module Mounted with Vibration Dampers

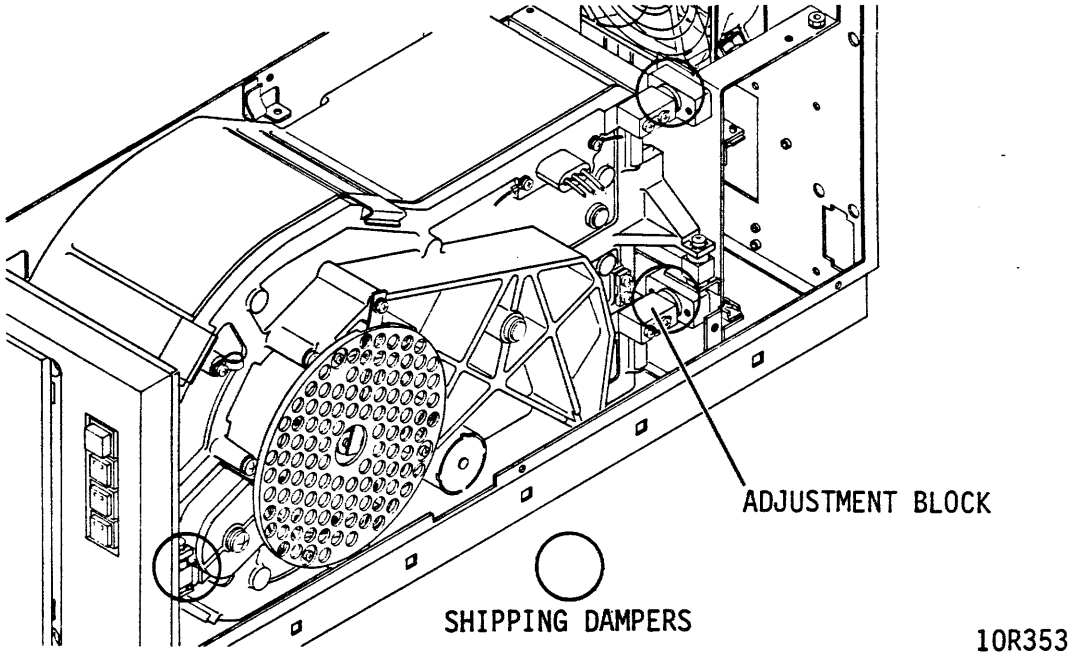


Figure 5-11. Module Mounted with Shipping Dampers

4. If two vibration dampers are installed, use module removal & replacement with vibration dampers.

   If three shipping dampers are installed, use module removal & replacement with shipping dampers.

MODULE REMOVAL & REPLACEMENT WITH SHIPPING DAMPERS

The shipping dampers must be adjusted whenever the module is replaced. Shipping damper adjustment is described following the removal and replacement procedures.

Removal

1. Perform entire drive removal procedure (5101).
2. Perform top cover removal procedure (5102).
3. Perform front panel removal procedure (5103).

NOTE

Steps 4 and 5 are necessary only if the drive has an older type operator panel, which is in the way of module removal. Newer type operator panels do not protrude into the chassis area, and are not in the way of module removal.

4. Disconnect cable from connector J26 on control board (_PXX) and remove cable from cable clamps.

5. Remove screws securing operator panel bracket to chassis and lift bracket, with operator panel and cable attached, from drive.

6. Disconnect cable from connector J29 on control board.

7. Disconnect cables from connectors J27 and J36 on R/W board (_RUX) or R/W PLO board (_PGX).

8. Disconnect cables from connectors J32 and J35 on R/W board (_RUX) or data latch board (_PFX).

9. Remove hardware that attaches read/write board bracket to chassis (see figure 5-12). Remove board and bracket assembly.

10. Perform motor speed control board (__PMX) and power amp board (__QHX) removal procedure (5305), except for separating the two boards.

11. Disconnect cable from connector J25 on control board.

12. Remove hardware that attaches control board to chassis and lift board to gain access to J28 connector. Disconnect cable from connector J28 and route through chassis opening into module area. Carefully pull control board out from drive and allow it to be supported by attached cables.

13. Remove shipping damper adjustment blocks from module (see figure 5-11). Blocks will be used on replacement module.

14. Remove upper rear shipping damper retainer block from chassis.

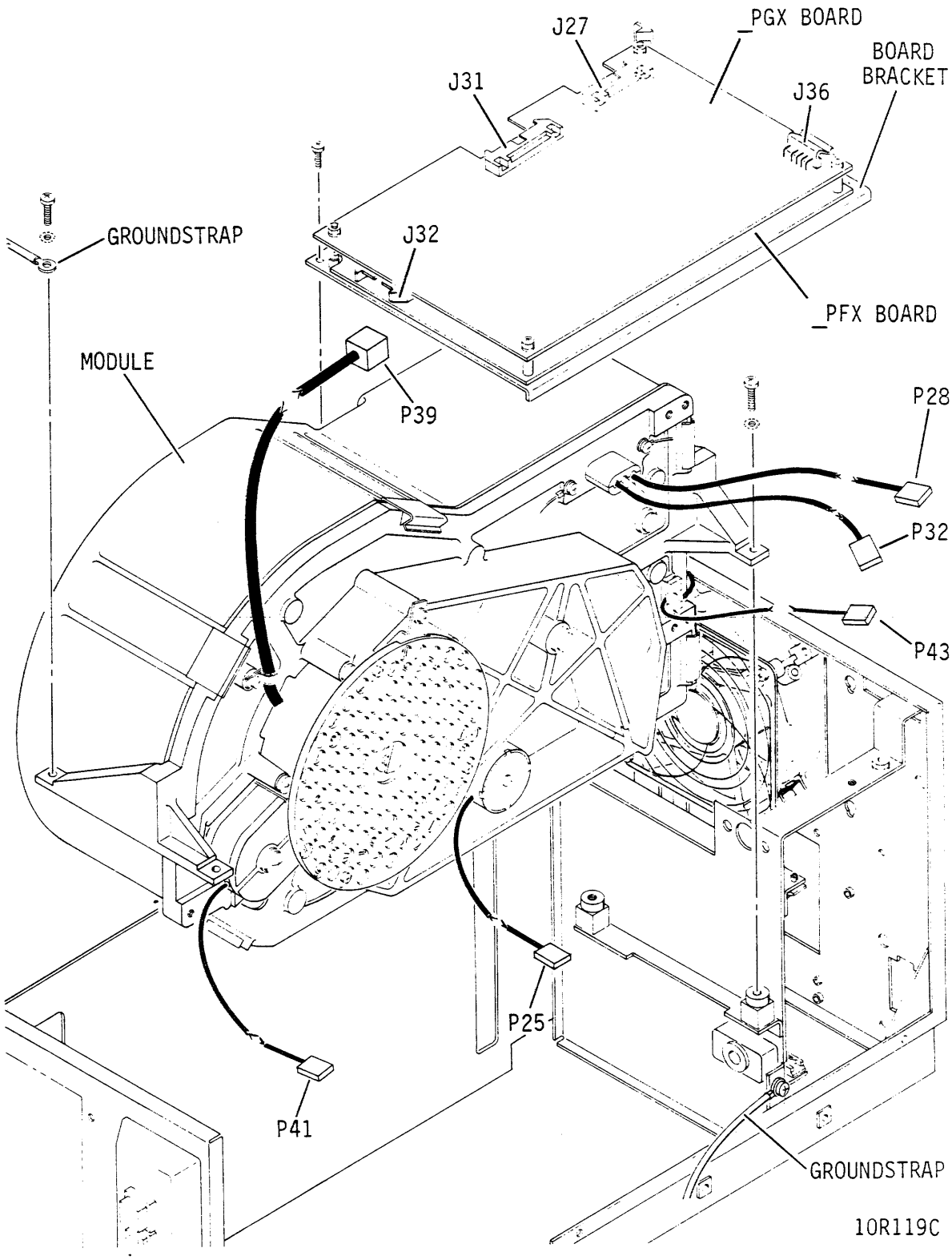


Figure 5-12. Module Removal and Replacement
With Shipping Dampers

CAUTION

Be certain to have a firm grip on module before attempting to lift it from drive. Take care to not damage cables when removing module.

15. Remove screws (and ground straps) securing module to shock mounts. Carefully lift module clear of drive.

Replacement

1. Install module as follows:

   a. Place module on chassis in position shown in figure 5-13. Hold module securely in place and route cable P28 through chassis opening.

   b. Set module on shock mounts and, while holding ground straps in place, loosely install mounting screws.

   c. Hold shock mounts to prevent twisting and tighten mounting screws to 1.3 N·m (10 lbf·in).

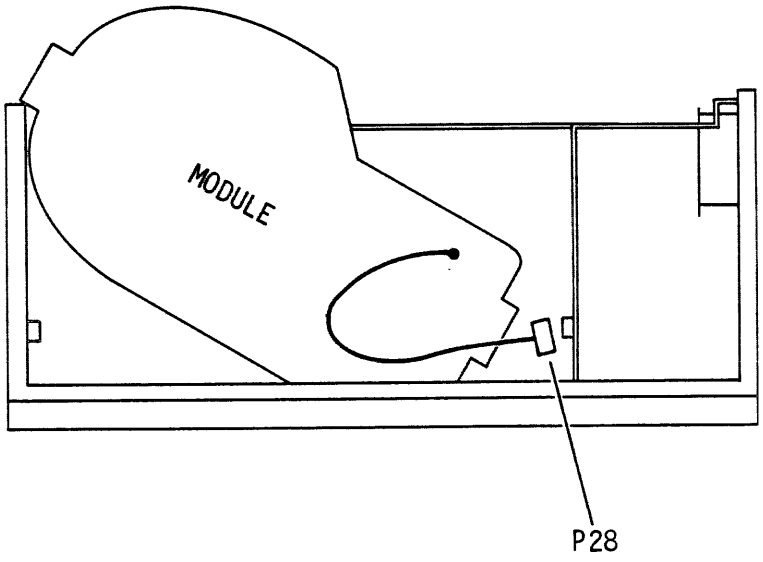


Figure 5-13. Module Position for P28 Cable Routing

2. Install upper rear shipping damper retainer block on chassis.

3. Loosely install lower two shipping damper adjustment blocks on module.

4. Route P39, P41, and P43, then loosely install upper rear shipping damper adjustment block on module.

5. Perform shipping damper adjustment procedure.

6. Connect cable to connector J28 on control board. Place control board in position on chassis and secure with attaching hardware.

7. Connect cable to connector J25 on control board.

NOTE

Steps 8 and 9 are necessary only if operator panel was removed in module removal procedure.

8. Thread operator panel cable and P26 through hole in front of chassis and attach operator panel and bracket to chassis with attaching hardware.

9. Connect cable to connector J26 on control board and secure cable in cable clamps.

10. Perform motor speed control and power amp boards replacement procedure (5305).

11. Install read/write board and bracket assembly on chassis with attaching hardware.

12. Connect cables to connectors J32 and J35 on R/W board or data latch board.

13. Connect cables to connectors J27 and J36 on R/W board or R/W PLO board.

14. Connect cable to connector J29 on control board.

15. Perform front panel replacement procedure (5103).

16. Perform a final check of all cable routing and connections.

17. Perform top cover replacement procedure (5102).

18. Perform entire drive replacement procedure (5101).

Shipping Damper Adjustment

Shipping dampers must be adjusted whenever the module is replaced.

Figure 5-14 shows the shipping dampers and adjustment tool. Three adjustment tools are required (see table 2-1 for part number).

1. Position the three adjustment tools as follows (all three tools must be in place before adjustment can proceed):

   a. Insert hollow end of adjustment tool into retainer block and grommet.

   b. Push tool until shoulder butts against grommet. Hollow end of tool should protrude slightly beyond module end of grommet.

   c. Fit pin on each adjustment block into hollow ends of tools until all three blocks butt tightly against tools. This position must be held while securing adjustment blocks.

2. Secure adjustment block by alternately tightening the two screws, in increments of 1.1 N·m (10 lbf·in), until they are tightened to 3.4 N·m (30 lbf·in). Repeat tightening sequence on other two blocks.

3. Remove adjustment tools.

4. To ensure that the module is free floating on the shock mounts, perform the following check:

   a. Slide one of the adjustment tools onto a pin.

   b. If tool does not slide easily on the pin, without interference from grommet, the adjustment must be repeated.

   c. Repeat check on other two pins.

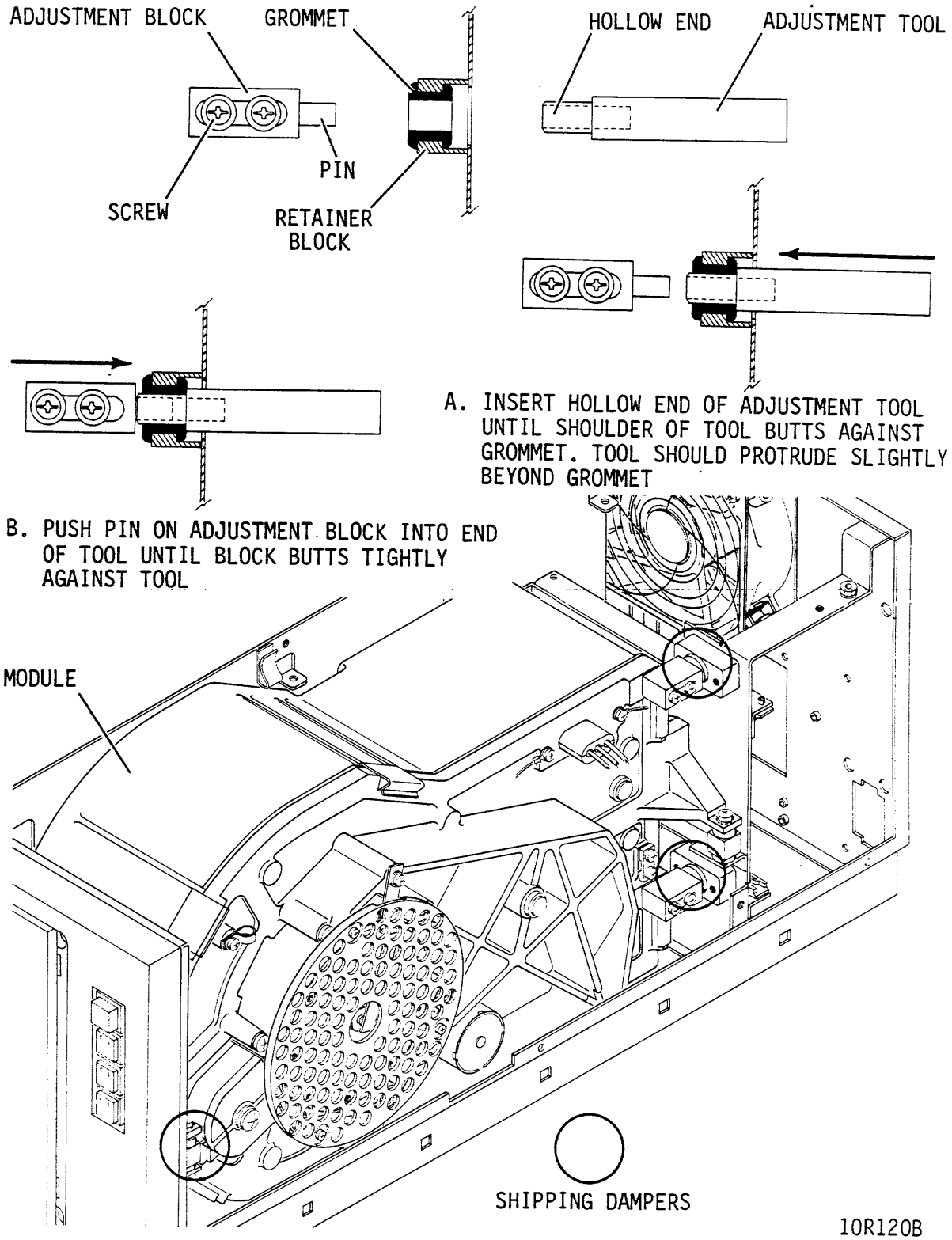


Figure 5-14. Shipping Damper Adjustment

MODULE REMOVAL & REPLACEMENT WITH VIBRATION DAMPERS

It is not normally necessary to adjust the vibration dampers when module is replaced.

Removal

1. Perform entire drive removal procedure (5101).
2. Perform top cover removal procedure (5102).
3. Disconnect cable from connector J29 on control board (_PXX).
4. Disconnect cables from connectors J27 and J36 on R/W board (_RUX) or R/W PLO board (_PGX).
5. Disconnect cables from connectors J32 and J35 on R/W board (_RUX) or data latch board (_PFX).
6. Remove hardware that attaches read/write board bracket to chassis (see figure 5-15). Remove board and bracket assembly.
7. Disconnect cable from connector J25 on control board.
8. Remove hardware that attaches control board to chassis and lift board to gain access to J28 connector. Disconnect cable from connector J28 and route through chassis opening into module area. Carefully pull control board out from drive and allow it to be supported by attached cables.
9. Disconnect cable from connector J43 on power amp board (_QHX).
10. Slide motor speed control board (__PMX) and power amp board (__QHX) out far enough to disconnect cables from connectors J39 and J41 on motor speed control board.
11. Remove the four screws securing two snubber brackets to module.

CAUTION

Be certain to have a firm grip on module before attempting to lift it from drive. Take care not to damage cables when removing module.

12. Remove screws (and ground strap) securing module to retaining bars. Carefully lift module clear of drive.

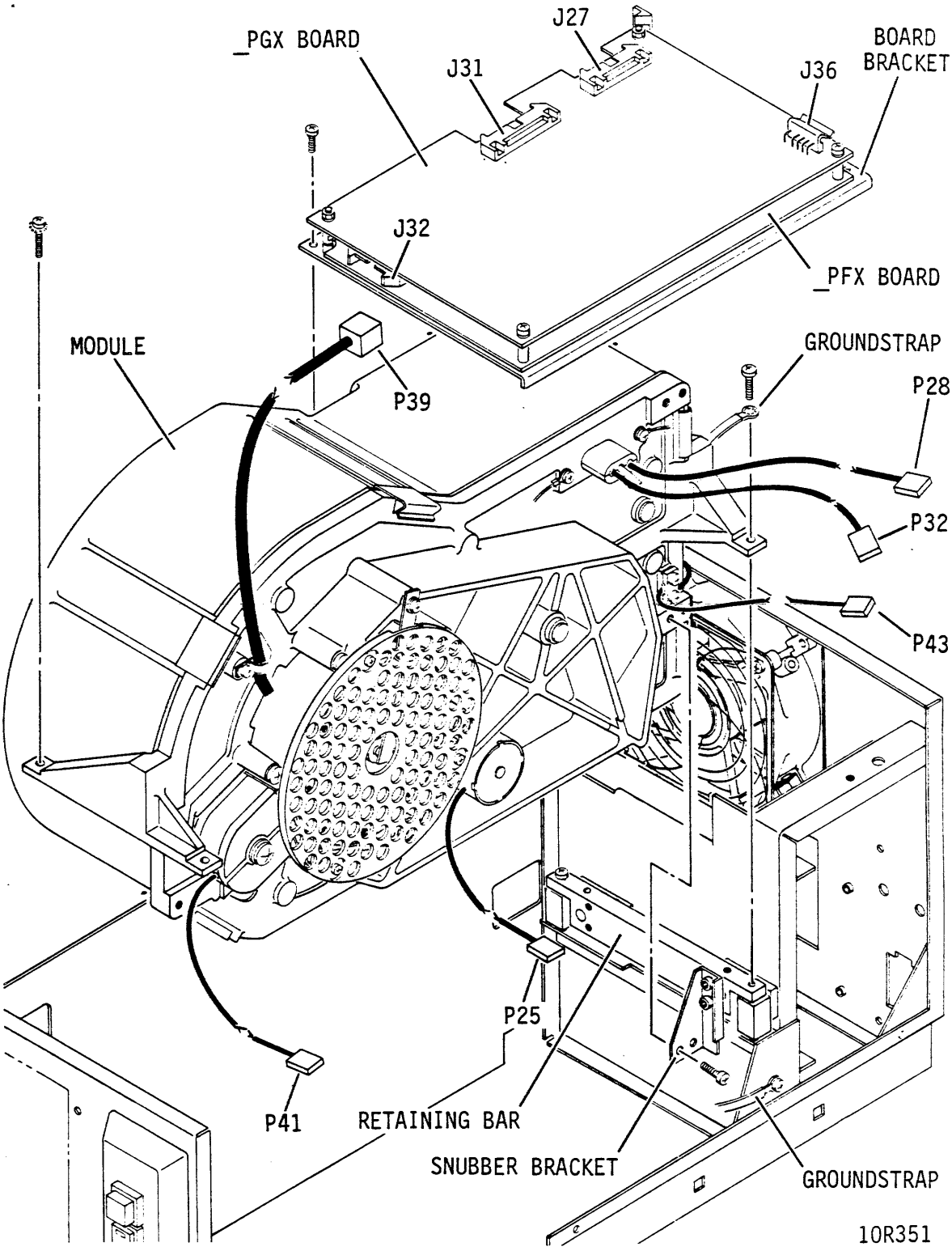


Figure 5-15. Module Removal and Replacement With Vibration Dampers

Replacement

1. Install module as follows:

   a. Place module on chassis in position shown in figure 5-13. Hold module securely in place and route cable P28 through chassis opening.

   b. Set module on retaining bars and, while holding ground strap in place, loosely install mounting screws.

   c. Install screws in snubber brackets and tighten just enough to draw module and snubber brackets together.

   d. Hold shock mounts to prevent twisting and tighten mounting screws to 1.3 N·m (10 lbf·in).

   e. Finish tightening snubber bracket screws.

2. If vibration dampers are to be checked and/or adjusted, it should be done at this point. Refer to vibration damper adjustment procedure.

NOTE

Steps 3, 4, and 5 are necessary only if vibration dampers were NOT adjusted.

3. Connect cables to connectors J39 and J41 on motor speed control board.

4. Slide motor speed control board and power amp board into place.

5. Connect cable to connector J43 on power amp board.

6. Connect cable to connector J28 on control board. Place control board in position on chassis and secure with attaching hardware.

7. Connect cable to connector J25 on control board.

8. Install read/write board and bracket assembly on chassis with attaching hardware.

9. Connect cables to connectors J32 and J35 on R/W board or data latch board.

10. Connect cables to connectors J27 and J36 on R/W board or R/W PLO board.

11. Connect cable to connector J29 on control board.

12. Perform a final check of all cable routing and connections.

13. Perform top cover replacement procedure (5102).

14. Perform entire drive replacement procedure (5101).

Vibration Damper Adjustment

Vibration damper adjustment is necessary only if vibration dampers have been removed or are out of adjustment for some other reason. It is not normally necessary to perform this procedure when replacing module. Four adjustment tools are required (see table 2-1 for part number).

1. Perform front panel removal procedure (5103).

2. Perform motor speed control/power amp board (_PMX/_QHX) removal procedure (5305), except for separating the two boards.

NOTE

A phillips head screwdriver less than 4 inches in length, or a right angle phillips, is required to adjust the vibration dampers located behind the motor speed control/power amp board.

3. Loosen screws securing the four vibration dampers (see figure 5-16).

4. Position the four adjustment tools as follows (all four tools must be in place before adjustment can proceed):

   a. Insert hollow end of adjustment tool into vibration damper and over pin on module retaining bar (see figure 5-16).

   b. Push tool until tool butts against retaining bar.

5. Secure vibration damper by alternately tightening the two screws, in increments of 1.1 N·m (10 lbf·n), until they are tightened to 3.4 N·m (30 lbf·n). Repeat tightening sequence on other three vibration dampers.

6. Remove adjustment tools.

7. To ensure that the module is free floating on the shock mounts, perform the following check:

   a. Slide one adjustment tool onto a pin (see step 4a).

   b. If the tool does not slide easily on pin, without interference from vibration damper, the adjustment must be repeated.

   c. Repeat check on other three pins.

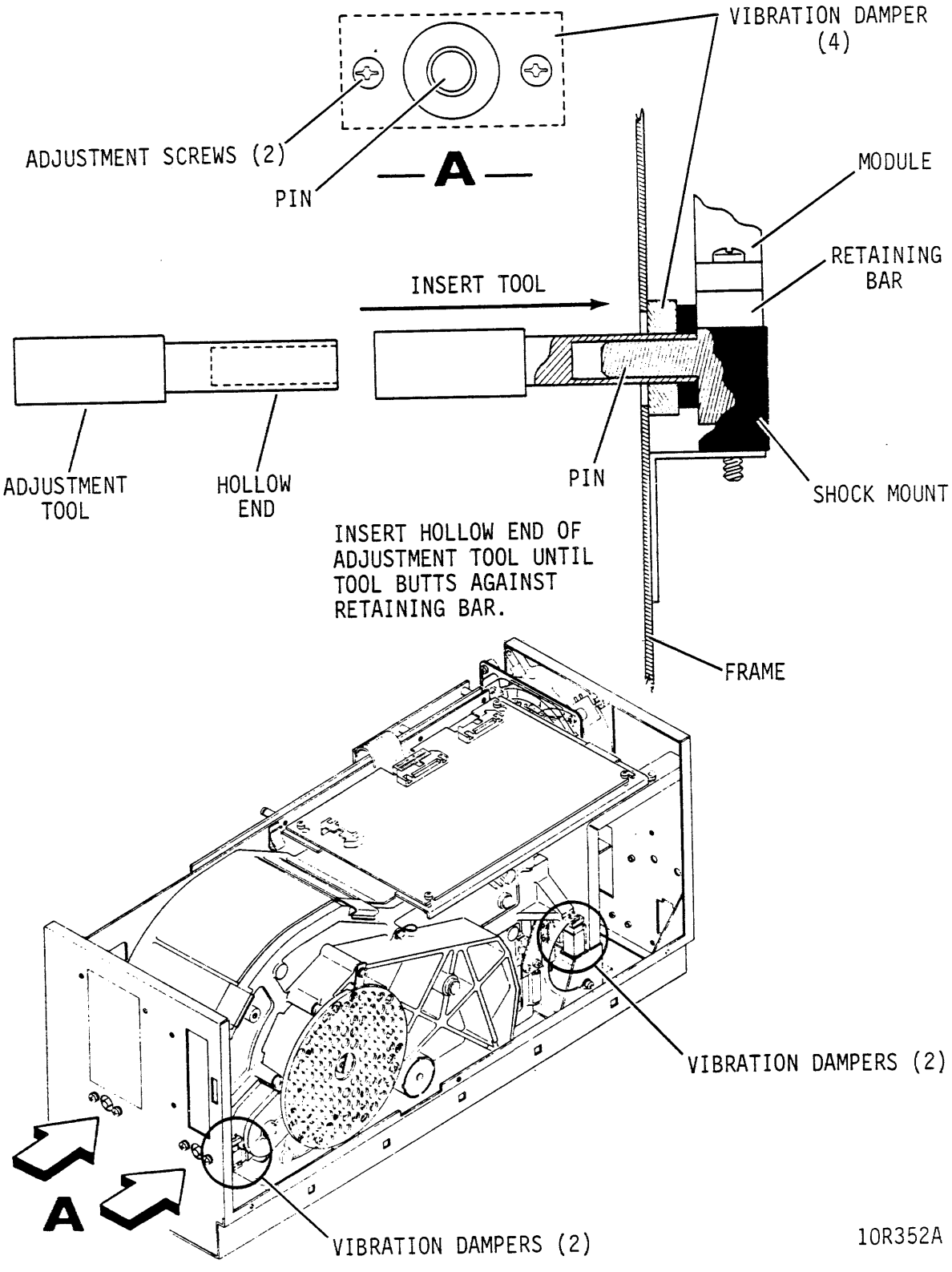


Figure 5-16. Vibration Damper Adjustment

8. Perform motor speed control/power amp board replacement procedure (5305).

9. Perform front panel replacement procedure (5103).

5207 - CABLE REPLACEMENT

All interassembly cables, except the dc power harness, are the flat ribbon type. The dc power harness is made up of individual wires tied together, and routed to the destination assemblies.

Cables cannot be repaired. If a cable, or any part of it (such as a wire or plug), is defective, replace the entire cable. In the case of the dc power harness, a poor connection can sometimes be fixed by using the wire seating tool (see table 2-1 for part number) to reseat the wire.

Flat ribbon cables that have one end permanently attached to an assembly are referred to as trailing cables. When a trailing cable is defective, the cable and attached assembly must be replaced.

5208 - MOTOR ASSEMBLY REMOVAL & REPLACEMENT

This procedure describes how to replace the motor, which is located on the module assembly beneath the motor shield (see figure 5-17). A special motor removal tool (see table 2-1 for part number) is required to remove or install the motor.

REMOVAL

1. Perform top cover removal procedure (5102).
2. Disconnect cable from connector J39 on motor speed control board (_PMX) and remove cable from cable clips.
3. Remove motor shield by removing attaching hardware (see figure 5-17).
4. Remove hardware attaching ground spring and remove spring.
5. Release brake by loosening screw securing brake to bottom of module.
6. Remove three screws securing motor rotor to spindle.
7. Align motor removal tool as shown in figure 5-17. Secure three captive bolts to holes vacated in step 3.
8. Free plunger on tool by disengaging locking pin.

NOTE

In the next step, ensure that central shaft of tool centers on ground spring contact button.

9. Push plunger down and rotate motor rotor to align captive screws with any three of the eight threaded holes in rotor. Tighten captive screws.
10. Remove rotor by pulling plunger.
11. Remove tool and rotor from module by loosening captive bolts.
12. Remove rotor from tool by loosening captive screws.
13. Remove screws securing motor clamp to spindle. Remove motor clamp.
14. Remove motor stator and cable from spindle.

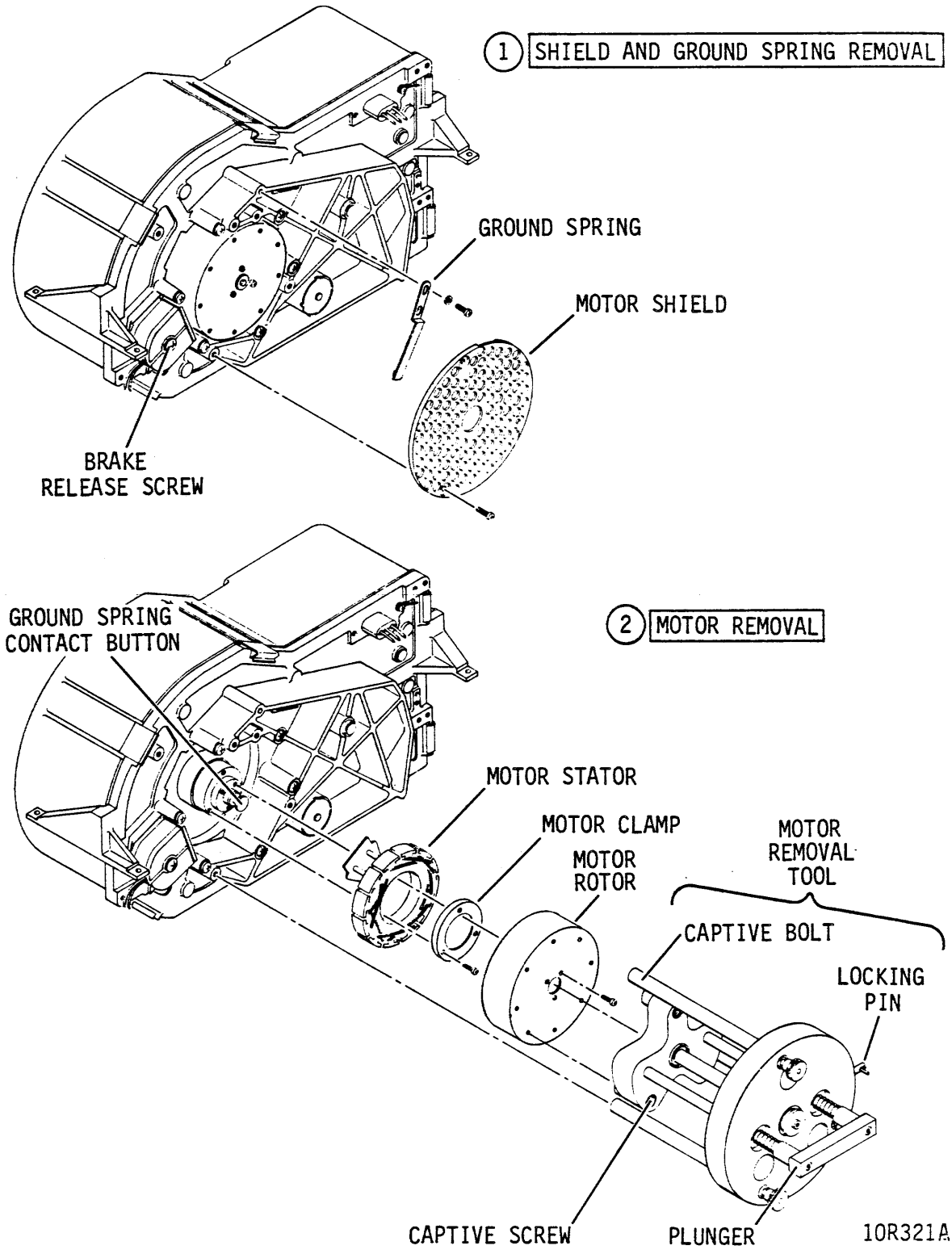


Figure 5-17. Motor Assembly Removal and Replacement

REPLACEMENT

1. Position motor stator and cable on spindle.
2. Install motor clamp over motor with attaching screws.
3. Attach motor rotor to motor removal tool with captive screws on tool.
4. Pull plunger on tool to upward position.
5. Align tool as shown in figure 5-17. Secure three captive bolts to module.

NOTE

In the next step, ensure that central shaft of tool centers on ground spring contact button.

6. Place rotor in position over motor by pushing plunger down.
7. Loosen captive screws attaching tool to rotor.
8. Remove tool by loosening captive bolts.
9. Manually rotate motor to align three holes in rotor with holes in spindle.
10. Attach rotor to spindle with three attaching screws.
11. Perform steps 4, 5, and 6 of brake adjustment procedure (5203).

NOTE

In the next step, ensure that ground spring is centered over contact button.

12. Install ground spring with attaching hardware.
13. Install motor shield with attaching hardware.
14. Connect cable to connector J39 on motor speed control board and secure cable with cable clips.
15. Perform top cover replacement procedure (5102).

5301 - CONTROL BOARD (–PXX) REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).
2. Perform I/O board removal procedure (5302).
3. Disconnect cables from connectors J14, J21, J23, J24, J25, J26, J28, and J29 on control board (see figure 5-18).
4. Remove attaching hardware and lift off control board.

REPLACEMENT

1. Place control board in position on chassis and secure with attaching hardware.
2. Connect cables to connectors J14, J21, J23, J24, J25, J26, J28, and J29 on control board.
3. Ensure that all circuit board switches are set either to match removed board or as indicated in the installation section of hardware maintenance manual, volume 1.
4. Perform I/O board replacement procedure (5302).
5. Perform top cover replacement procedure (5102).

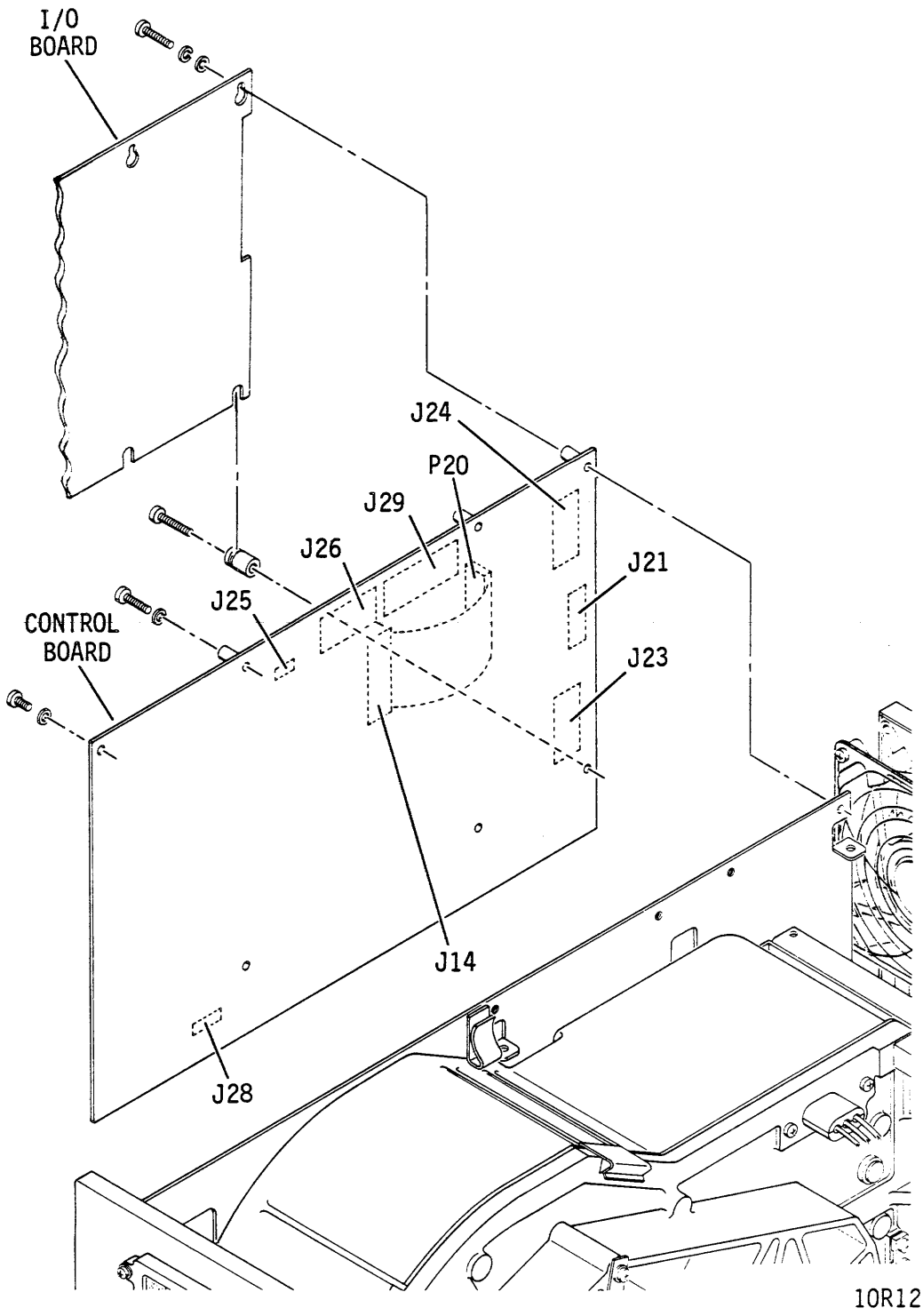


Figure 5-18. Control Board (_PXX) Removal and Replacement

5302 - I/O BOARD (—EBN/—EDN) REMOVAL & REPLACEMENT

The I/O board is mounted on the control board (_PXX) and is connected to the I/O plate via cables and connectors J2, J3, and J4 (see figures 5-18 and 5-19). Newer I/O boards have detachable I/O cables, and older I/O boards (BEBN, DEBN, EEBN, FEBN, AEDN, and CEDN) have fixed (trailing) I/O cables.

The I/O plate on remote power supply drives is mounted on the drive rear panel. The I/O plate on integral power supply drives is mounted on the rear of the power supply.

REMOVAL (I/O BOARDS WITH FIXED I/O CABLES)

1. Perform top cover removal procedure (5102).

2. Disconnect cables from connectors J48 (does not apply to drives without fan fault sense feature), J19, and J20 on I/O board.

3. Disconnect cable from connector J27 on R/W board (_RUX) or R/W PLO board (_PGX).

NOTE

Perform step 4 on drives with remote power supply. Perform step 5 on drives with integral power supply.

4. On drives with remote power supply, perform the following:

   a. On drives with power supply attached directly to slides, remove screws securing front of power supply to slides and tilt supply back far enough to allow I/O plate to be removed. On drives with power supply attached to bracket and mounts, remove hardware securing bracket to mounts and slide supply back far enough to allow I/O plate to be removed.

   b. Disconnect external I/O cables from connectors on I/O plate.

CAUTION

Remove terminator by hand. It could be damaged if a pliers or other tool is used.

   c. Remove terminator(s) from connector(s) on I/O plate.

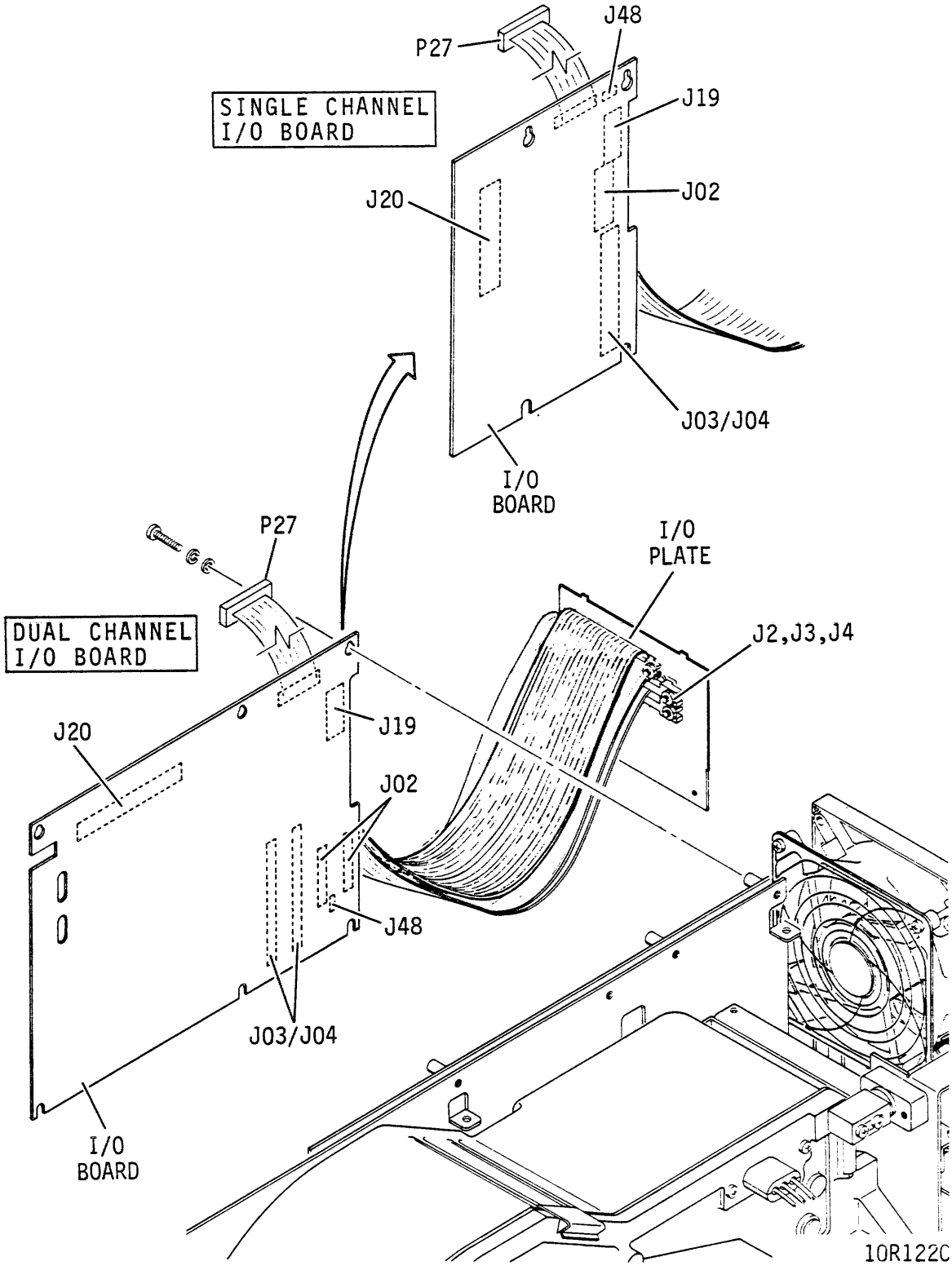


Figure 5-19. I/O Board (_EBN/_EDN) Removal and Replacement

d. Remove hardware attaching I/O plate to rear panel. Free I/O plate and cable assembly from rear panel.

e. Remove hardware attaching I/O cable connectors to I/O plate, and remove connectors from plate.

5. On drives with integral power supply, perform the following:

a. Remove I/O shield (if used) from I/O plate (see figure 5-8).

b. Remove hardware securing cover plate to power supply. Remove cover plate.

c. Disconnect external I/O cables from connectors on I/O plate.

CAUTION

Remove terminator by hand. It could be damaged if a pliers or other tool is used.

d. Remove terminator(s) from connector(s) on I/O plate.

e. Remove hardware attaching I/O plate to power supply. Free I/O plate and cable assembly from power supply.

f. Remove hardware attaching I/O cable connectors to I/O plate, and remove connectors from plate.

6. Loosen the screws (top of board) that secure the I/O board to control board (see figure 5-18).

7. Remove I/O board (out keyhole slots) from control board.

REPLACEMENT (I/O BOARDS WITH FIXED I/O CABLES)

NOTE

Early model single channel drives (drives with CPXX or DPXX control board, or BEBN I/O board) do not have operable fan fault sense feature. For drives without this feature, the replacement board (unless it is a BEBN board) must be modified as directed in step 1 to disable fan fault sense circuit.

1. On drives without fan fault sense feature, modify replacement I/O board as follows:

a. Cut and remove wire wrap connection between pins E323 and E328 on component side.

b. Add wire wrap between pins E317 and E322 on component side.

2. Place I/O board in position over screws on control board. Tighten screws securing I/O board to control board.

NOTE

Perform step 3 on drives with remote power supply. Perform step 4 on drives with integral power supply.

3. On drives with remote power supply, perform the following:

a. Install I/O cable connectors on I/O plate with attaching hardware.

b. Install I/O plate and cable assembly on rear panel with attaching hardware.

c. Connect external I/O cables and terminator(s) to connectors on I/O plate.

d. Move power supply into operating position. Install and tighten mounting hardware.

4. On drives with integral power supply, perform the following:

a. Route internal I/O cables from I/O board through rear panel and around side of power supply. Install I/O cable connectors on I/O plate with attaching hardware.

b. Install I/O plate and cable assembly on power supply with attaching hardware.

c. Connect external I/O cables and terminator(s) to connectors on I/O plate.

d. Install cover plate on power supply with attaching hardware.

e. Install I/O shield (if used) on I/O plate.

5. Connect cable to connector J27 on R/W board or R/W PLO board.

6. Connect cables to connectors J48, J19, and J20 on I/O board.

7. Ensure that all circuit board switches are set either to match removed board or as indicated in the installation section of the hardware maintenance manual, volume 1.

8. Perform top cover replacement procedure (5102).

REMOVAL (I/O BOARDS WITH DETACHABLE I/O CABLES)

1. Perform top cover removal procedure (5102).

2. Disconnect internal I/O cables from connectors on I/O board.

3. Disconnect cables J19, J20, and J48 from connectors on I/O board.

4. Disconnect cable from connector J27 on R/W board (_RUX) or R/W PLO board (_PGX).

5. Loosen the screws (top of board) that secure the I/O board to control board (see figure 5-19).

6. Remove I/O board (out keyhole slots) from control board.

REPLACEMENT (I/O BOARDS WITH DETACHABLE I/O CABLES)

1. On drives without fan fault sense feature, modify the replacement I/O board by moving molded jumper plug E947 to E942.

2. Place I/O board in position over screws on control board. Tighten screws securing I/O board to control board.

3. Connect cable to connector J27 on R/W board or R/W PLO board.

4. Connect cables to connectors on J19, J20, and J48 on I/O board.

5. Connect internal I/O cables to connectors on I/O board.

6. Ensure that all circuit board switches are set either to match removed board or as indicated in the installation section of the hardware maintenance manual, volume 1.

7. Perform top cover replacement procedure (5102).

5303 - READ/WRITE PLO BOARD (–PGX) REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).
2. Disconnect cables from connectors J27, J31, and J36 on R/W PLO board (see figure 5-20).
3. Remove attaching hardware and lift off board.

REPLACEMENT

1. Place R/W PLO board in position on top of data latch board (_PFX) and secure with attaching hardware.
2. Connect cables to connectors J27, J31, and J36 on R/W PLO board.
3. Perform top cover replacement procedure (5102).

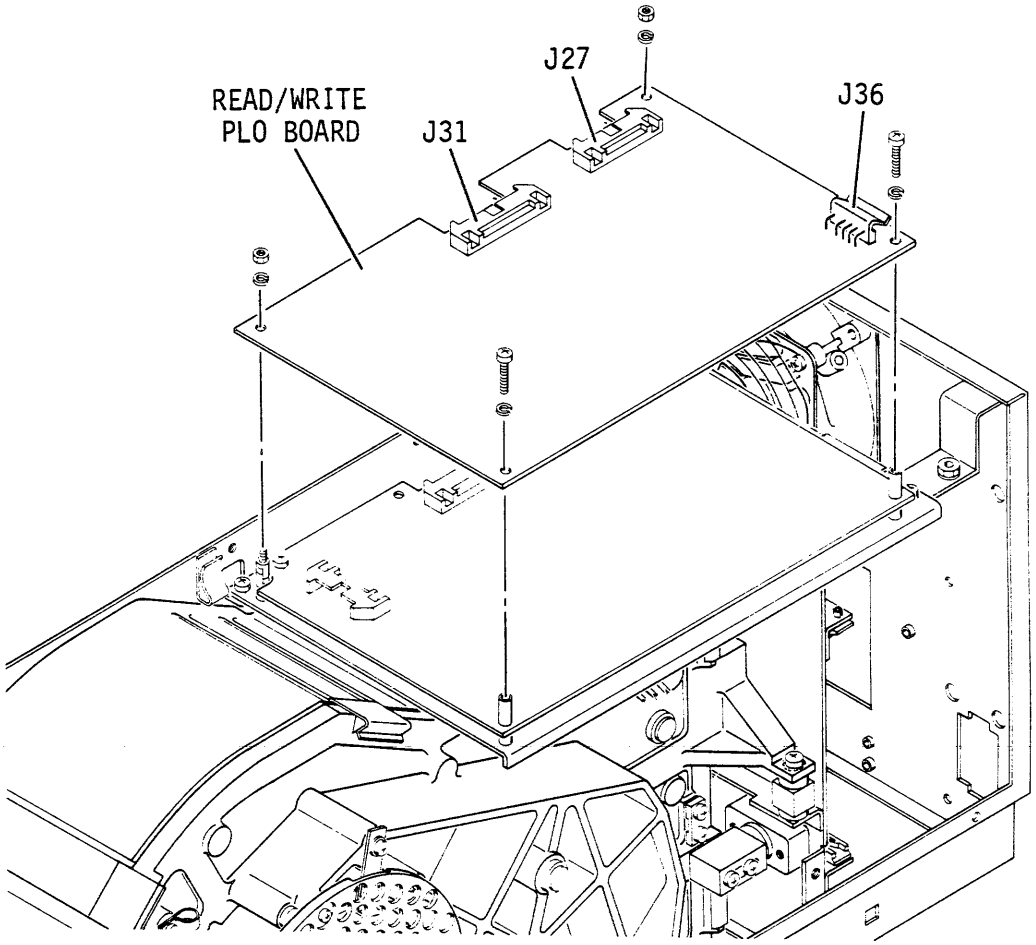


Figure 5-20. Read/Write PLO Board (_PGX)
Removal and Replacement

5304 - DATA LATCH BOARD (–PFX) REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).
2. Remove two screws securing R/W PLO board (_PGX) to data latch board (see figure 5-21).
3. Swing R/W PLO board to upright position (see figure 5-21).
4. Disconnect cables from connectors J30, J32, and J35 on data latch board.
5. Remove attaching hardware and lift off board.

REPLACEMENT

1. Place data latch board in position on board bracket and secure with attaching hardware.
2. Connect cables to connectors J30, J32, and J35 on data latch board.
3. Swing R/W PLO board into position on top of data latch board and secure with attaching hardware.
4. Perform top cover replacement procedure (5102).

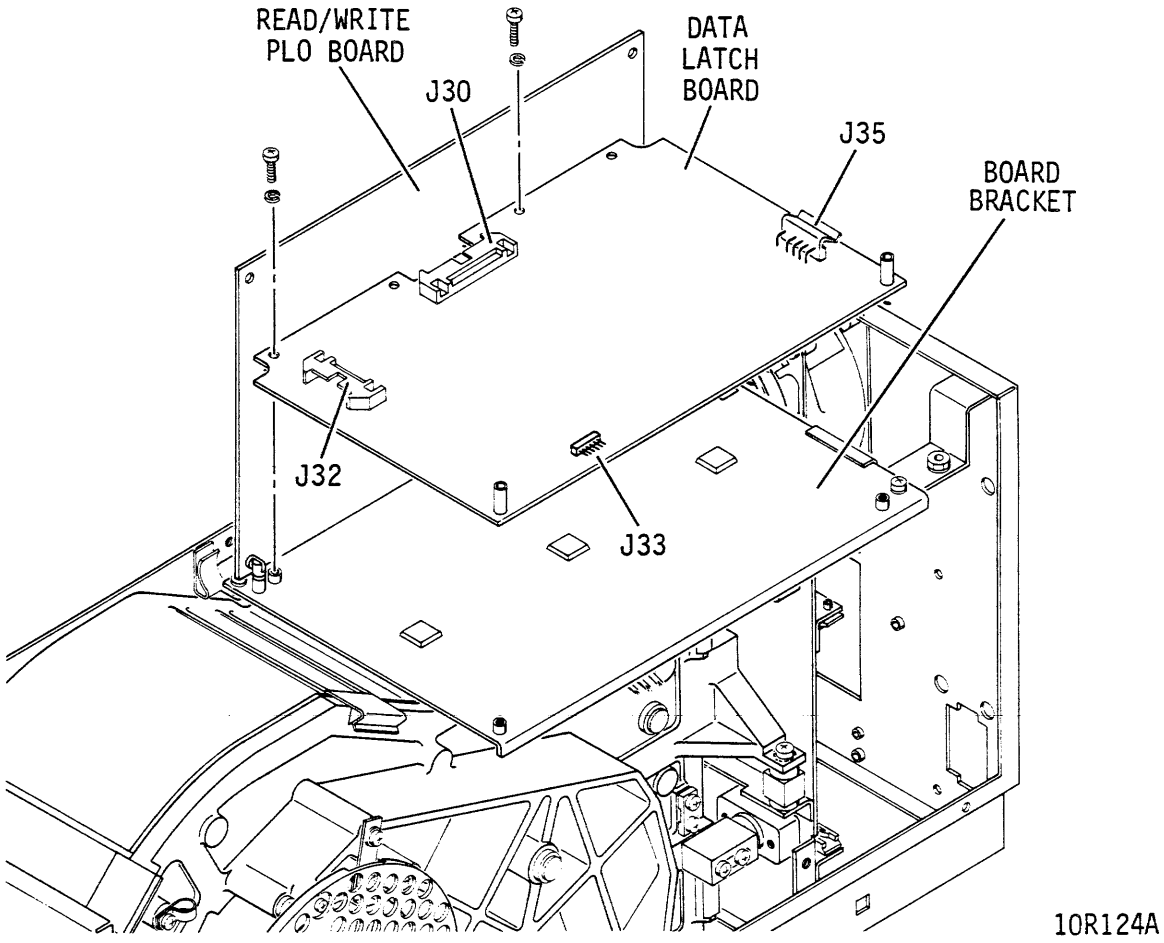


Figure 5-21. Data Latch Board (_PFX) Removal and Replacement

5305 - MOTOR SPEED CONTROL BOARD (–PMX) AND POWER AMP BOARD (–QHX) REMOVAL & REPLACEMENT

The motor speed control board and the power amp board are assembled together and mounted between slide rails at the right rear of the drive (see figure 5-22). To replace either board, it is necessary to remove both and separate them after removal.

REMOVAL

1. Perform top cover removal procedure (5102).
2. Disconnect cable from connector J27 on R/W board (_RUX) or R/W PLO board (_PGX).
3. Disconnect cable from connector J20 on I/O board (_EBN/_EDN).
4. Loosen the screws (top of board) that secure the I/O board to control board (_PXX) (see figure 5-22). Remove I/O board (out keyhole slots) from control board to gain access to control board cables.
5. Disconnect cables from connectors J23 and J24 on control board.
6. Disconnect cable from connector J43 on power amp board.
7. Slide motor speed control board and power amp board assembly out to gain access to all remaining cable connectors.
8. Disconnect cable from connector J22 on power amp board.
9. Disconnect cables from connectors J37, J39, and J41 on motor speed control board.
10. Remove board assembly, taking care to not damage cables from connectors J23 and J24.
11. Separate boards by removing attaching hardware.

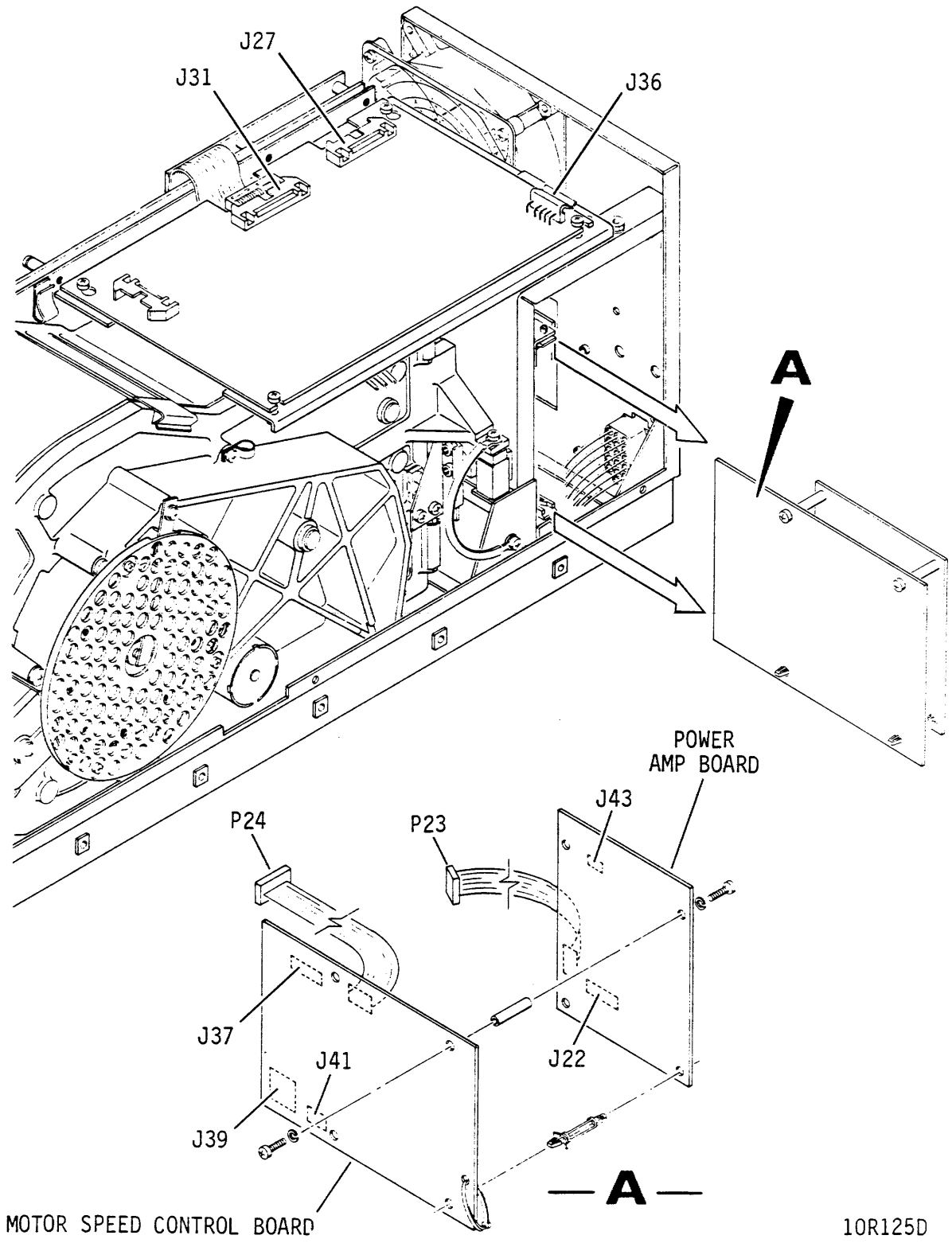


Figure 5-22. Motor Speed Control Board (_PMX) and Power Amp Board (_QHX) Removal & Replacement

REPLACEMENT

1. Assemble motor speed control board and power amp board together with attaching hardware.

CAUTION

Exercise care to prevent damage to cables or wires when installing boards.

2. Place board assembly between slide rails and slide in far enough to allow cables to be connected.

3. Connect cables to connectors J37, J39, and J41 on motor speed control board.

4. Connect cable to connector J22 on power amp board.

5. Slide board assembly in as far as possible.

6. Connect cable to connector J43 on power amp board.

7. Connect cables to connectors J23 and J24 on control board.

8. Place I/O board in position over screws on control board. Tighten screws securing I/O board to control board.

9. Connect cable to connector J20 on I/O board.

10. Connect cable to connector J27 on R/W board or R/W PLO board.

11. Perform top cover replacement procedure (5102).

5309 - READ/WRITE BOARD (_RUX) REMOVAL & REPLACEMENT

REMOVAL

1. Perform top cover removal procedure (5102).
2. Disconnect cables from connectors J27, J30, J32, and J36 from read/write board (see figure 5-23).
3. Loosen the four screws securing the read/write board to the board bracket.
4. Lift read/write board off board bracket (screw heads pass through key hole slots in board) and remove from drive.

REPLACEMENT

1. Position read/write board on board bracket (screw heads pass through key hole slots in board) and tighten the four screws.
2. Connect cables to connectors J27, J30, J32, and J36 on read/write board (see figure 5-23).
3. Perform top cover replacement procedure (5102).

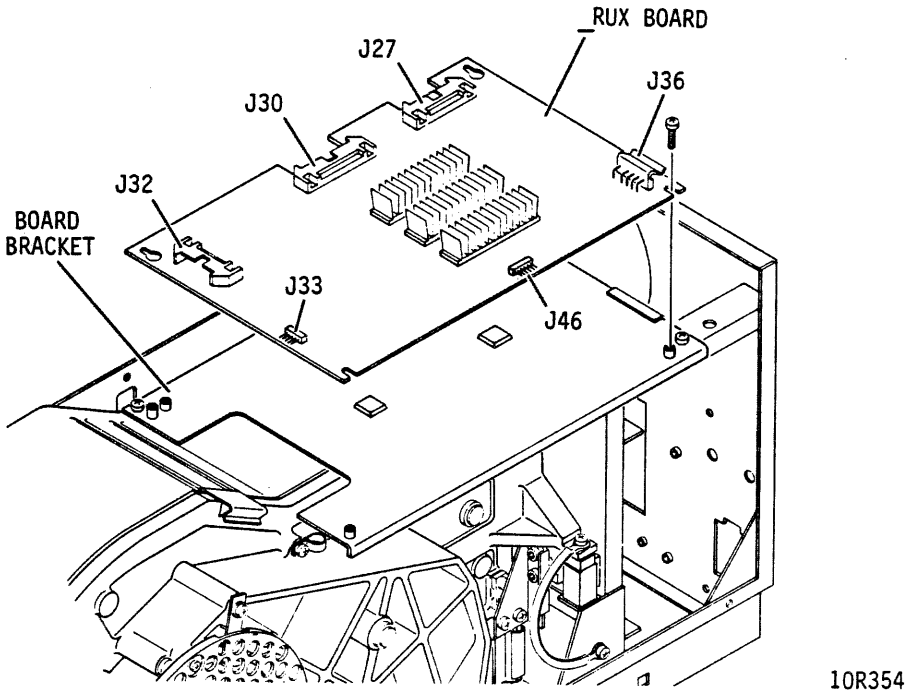


Figure 5-23. Read/Write Board (_RUX) Removal and Replacement

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