PRELIMINARY

CONTROL DATA®

NRZI-LCTT MAGNETIC TAPE TRANSPORT CONTROLLER

FA446-A

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
MAINTENANCE AIDS
PARTS DATA
WIRE LIST
GLOSSARY

CONTROL DATA
CORPORATION

CUSTOMER ENGINEERING MANUAL

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MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

SHEET 1 OF 1

MANUAL REV	FCO OR ECO	EQUIPMENTS					
		SERIES	S/N				
	ECO CK514	01	1				
	ECO CK887	02	101				
01	ECO CK887	03	141				

NOTE: Logic Diagrams released with manual are next higher revision than that shown on logic diagrams. See ECO CK798.

PREFACE

This manual supplies customer engineering information for the CONTROL DATA® FA446-A Magnetic Tape Transport Controller (NRZI-LCTT). This controller is used with the AB107/AB108 Computer to control the 6173/6193 Magnetic Tape Transport. The user of this equipment should be familiar with the computer and magnetic tape transport equipment and software.

The following CONTROL DATA® publications may be useful as references:

Publication	Pub. No.
FA446-A LCTT NRZI Magnetic Tape Transport Controller Reference Manual	89769400
FV497-A/FV618-A Phase Encoding Formatter Customer Engineering Manual	89796100
1748 Computer Reference Manual	89633400
AB10 7/AB108 Computer Customer Engineering Manual	89633300
I/O Specification Manual	89673100

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SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

This section contains the functional and operational description of the CONTROL DATA® FA446-A Magnetic Tape Transport Controller.

The magnetic tape transport controller (LCTTC) contains the logic that interprets the AB107/SB108 Central Processing Unit (CPU) function codes, controls the magnetic tape transport (LCTT) operations, assembles and disassembles 16-bit words between the CPU and the LCTT, and provides the status information to the CPU. The communication between the controller and the CPU is via the A/Q channel and the Direct Storage Access (DSA) channel. Each LCTTC may control as many as four LCTT's in a daisy chain configuration. The FA446-A Magnetic Tape Transport Controller is used with the FV618-A Phase Encoding Formatter whenever it is employed.

The controller logic is mounted on four 50-PAK printed wiring assembly boards. The boards may be mounted in the AB107/AB108 Computer Enclosure, usually in slots 11, 12, 13 and 14, while power for them is supplied by the AB107/AB108 Computer power supply.

CABLES AND CONNECTORS

A single cable connects the controller with the first transport, while each transport has two identical interconnection plugs to enable daisy chain interconnection. Figure 4-1 shows a typical transport to controller configuration. The interconnecting cable between the controller and the first transport is a 24 AWG copper wire twisted pairs cable having a length of 20 feet. The standard cable between each additional transport is 20 feet long with connectors at both ends. The cables required for operation of the controller are listed in Section 8 (Parts Data). A complete wire list is contained in Section 9.

TRANSLATOR — TERMINATOR

Each tape transport requires a combination translator-terminator (P/N 46338700) when connected in a series configuration. The unit is placed on the first LCTT unit in the daisy chain.

TABLE 1-1. SPECIFICATIONS (Each PWB)

Specifications	Explanation
PHYSICAL CHARACTERISTICS	
Dimensions	
Width	$6\frac{13}{16}$ inches
Length	$12\frac{3}{8}$ inches
Depth	$\frac{3}{8}$ inches
Weight	(to be furnished)
ENVIRONMENT	
Temperature	
Shipping	-40°F to 158°F (-40°C to 70°C)
Storage	14°F to 122°F (10°C to 50°C)
Operating	40°F to 120°F (5°C to 50°C)
Humidity	
Shipping	0 to 100% RH non-condensing
Storage	10% to 90% RH non-condensing
Operating	10% to 90% RH non-condensing
POWER	
Input Requirements	5 Volts dc
Signal Level	
Low State (0)	0.4 Volts dc, or less
High State (1)	2.4 Volts dc, or more
Ground	Logic ground is connected to computer logic ground

SECTION 2

OPERATION AND PROGRAMMING

PROGRAMMING

Summary of Programming Information

Tables 2-1 through 2-7 and Figures 2-1 through 2-9 provide the experienced programmer with the information necessary to program the FA446-A. The following paragraphs further define this information.

The FA446-A communicates with the 1784 Processor via the computer A/Q channel and DSA channel.

The Q register designates the equipment to be referenced and directs the operation to be performed upon the input or output instruction execution. Figure 2-1 illustrates the format of the Q register:

Bits 11 - 15 should always be zero.
Bits 7 - 10 select the FA446-A. The bits must match the equipment number of the controller
Bits 2 - 6 are ignored.
Bits 0 - 1 (the Director) specify an operation according to Table 2-2.

The FA446-A has two modes of operation:

1) Direct:

   Operation is initiated and data is transferred via the A/Q channel.

   Direct transfer shall be accomplished by the following sequence:

   1. Control Function (Read Motion and Write Motion).
   2. Input to A or Output from A instruction for every data word.

2) Buffered:

Operation is initiated through the A/Q, and data transfer is via the DSA.

Buffered I/O transfer shall be accomplished by issuing the following sequence:

1. Buffered I/O instruction
   (Controller fetches LWA+1 from FWA-1 and waits)

2. Control Function (Read Motion or Write Motion) instruction. Read Data transfer starts when data block moves under the Read head.

   Write Data transfer starts when pre-record gap has passed under the Write head.

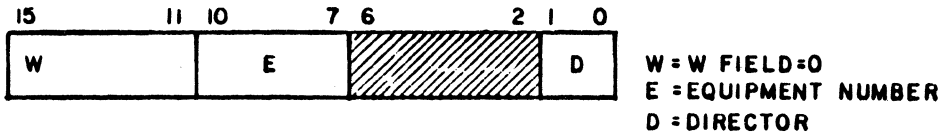

Figure 2-1. Format of Q-Register

Addresses

The W = 0 signal plus bits 10-7 of the Q register are used to select the FA446-A. The W field of Q is always loaded with zeros. Bits 0-1 of Q are used to specify an operation. Figure 2-1 illustrates the format of the Q Register. Table 2-1 lists the values of E required to select a controller with a given equipment number setting.

TABLE 2-1. HEXADECIMAL CODE FOR CONTROLLER ADDRESSES (E FEILD)

Hexa-decimal Code	Q-Register			
	Q10	Q09	Q08	Q07
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

Note

A "1" in the binary code (Q10 - Q07) indicates the presence of a jumper plug in that position on the PW assembly matching the signal present in that bit of the Q-Register. A "0" indicates the absence of a jumper plug matching the Q-Register bits.

Bits 10-7 of the A register are used along with the contents of Q and Output from A to select a tape transport. (See Unit Select).

OPERATIONS

The D field of Q is combined with an AB107/AB108 Input from A or Output from A instructon to specify an operation (see Table 2-2). The operations initiated by an Output from A may be further modified by the contents of the A register (see Table 2-3, Figures 2-2 and 2-3). The following paragraphs define these operations.

Operations Defined by Q and Output from A

Write: A Write transfers data from the computer to the controller generates a parity bit and writes the data plus parity bit on the tape. To perform a Write, load Q with W = 00*, E = Equipment number setting of

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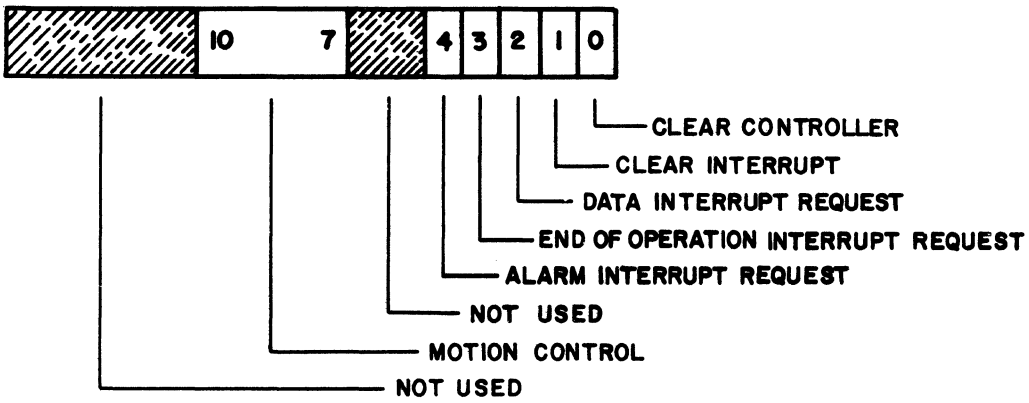
* W is written as two digits; the left, binary; the right, hexadecimal.

desired MTTC controller and D = 00. An Output from A instruction initiates the transfer of the computer word to the tape. Any number of consecutive characters sent to the tape are written (along with a parity bit) on the tape as a single record. Whenever the computer breaks the continuity of the computer word outputs, the controller initiates an End-of-Record sequence. A Write is rejected if Not Ready, Write Motion has not been initiated, Data Status is not set, if Buffered I/O is set or a Program Protect fault occurs. If no new Control Function is received from the computer, tape motion stops at the next interrecord gap.

TABLE 2-2. MTTC OPERATIONS

Computer Instruction		
D	Output from A	Input to A
00	Write	Read
01	Control Function	Director Status 1
10	Unit Select	Director Status 2
11	Buffered Input/Output	Current Address

Control Function: The Control Function specifies operating conditions for the selected controller and transport and initiates tape motion. To perform a Control Function, load Q with W=00, E = Equipment Number, and D = 01. Load A according to Figure 2-2 and Table 2-3, and execute an Output from A.



Fiqure 2-2. Control Function for A-Register

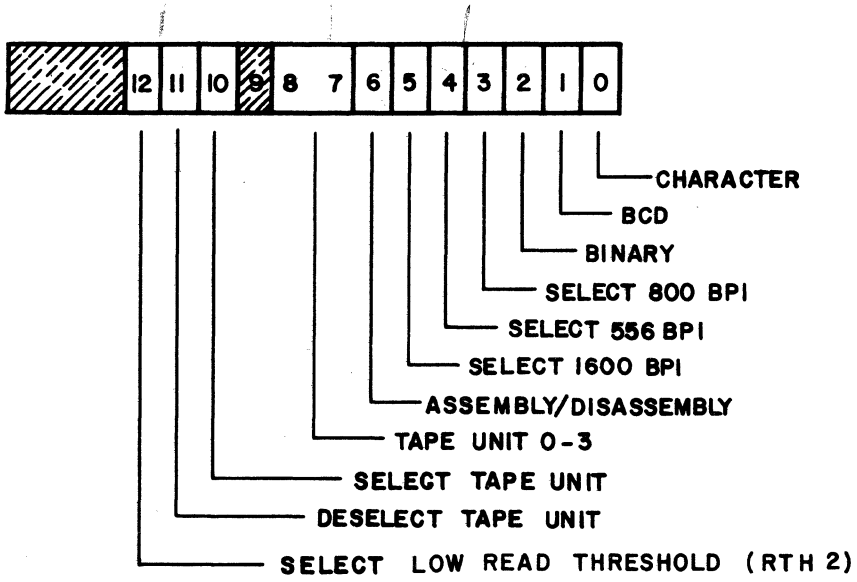


Figure 2-3. Unit Select for A-Register.

If bits 7-10 of A equal zero, the control function is rejected only if a protect fault occurs. Otherwise the controller rejects control functions if it is Not Ready, the End-of-Operation status condition is not present, an illegal code exists in bits 7-10 of A, the tape transport is Busy or if a protect fault occurs. Control Function is not rejected if it is issued after EOP status is set and same motion direction is requested and same data transfer direction (Read or Write) is requested. (See Table 2-3) Write Motion or Write FM/TM is rejected if the file protect ring is absent.

Table 2-3 lists the legal motion control codes. One Motion Function plus any or all Clear and Interrupt selections may be selected simultaneously or individually. The requests are honored in this order: Clears, Interrupt selections and Motion Control.

A New Motion Function clears EOP, Alarm and all causes for Alarm.

The following describes these codes:

1) Clear Controller (A00 = 1) - Master clears the 1732-3 with the following exceptions: Unit Select, Mode Select, Code Select and Format Select.

2) Clear Interrupt (A01 =1) - clears all interrupts and interrupt requests. If an interrupt request is coded along with a Clear Interrupt, that selection is honored, but any previous selections are cleared.

3) Data Interrupt Request (A02 = 1) - causes an interrupt to be generated when an information transfer through A/Q channel may occur. The interrupt response is cleared by the Reply to the data transfer. The request and response are cleared by a Clear Controller or a Clear Interrupt code.

4) End-of-Operation Interrupt Request (A03=1) - causes an interrupt to be generated at the end of an operation. The request and response are cleared by a Clear Controller or a Clear Interrupt code.

5) Alarm Interrupt Request (A4 = 1) - causes an interrupt to be generated upon a condition which warrants program or operator attention. The Alarm Interrupt is generated by any of the following conditions:

1. End-of-Tape
2. Parity Error
3. Lost Data
4. File Mark/Tape Mark
5. The controller goes Not Ready during an operation.
6. Storage Parity Error
7. Protect Fault
8. ID - Abort
9. PE - Lost Data
10. PE - Warning

6) Write Motion (A10-7 = 0001) - initiates Write Motion. If Buffered Input/Output is not set, the Data Status goes true which initiates Direct Data Output. Write Motion is terminated (EOP set) when End-of-Record is detected by the Read head.

If buffered I/O is not set, Write Motion is selected and no data transfer follows, the controller locks out and terminates the Write Motion function when it is time to write the first character on tape. Forward drops to the selected transport and the transport goes Not Busy, but no End-of-Operation is generated.

TABLE 2-3. MOTION CONTROL

Bits 10-7 of A	Motion Function
0001	Write Motion
0010	Read Motion
0011	Backspace
0101	Write File Mark/Tape Mark
0110	Search File Mark/Tape Mark Forward
0111	Search File Mark/Tape Mark Backward
1000	Rewind Load

7) Read Motion (A10-7 = 0010) - initiates Direct or Buffered Data input. Read Motion terminates by absence of data from the magnetic tape transport. If the computer stops requesting characters, data transfer stops, but the tape continues to move to the end of the record. If a data transfer request is not received by the controller in time to complete the transfer properly, the Lost Data status bit is set and subsequent data request are rejected. If a File Mark is encountered the File Mark status is set.

8) Backspace (A10-7 = 0011) - moves tape backward one record. Backspace from Load Point is not rejected (however the tape will not move) and non-stop backspace is possible.

9) Write File Mark (A10-7 = 0101) - moves tape forward approximately 6 inches and writes a File Mark. The normal End-of-Operation sequence follows the File Mark, writing the longitudinal check character.

10) Search File Mark Forward (A10-7 = 0110) - moves tape forward until a File Mark* is detected; an End-of-Operation (EOP) is generated and tape motion stops.

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* A parity error is indicated together with File Mark status.

11) Search File Mark Backward (A10-07= 0111) - moves tape backward until a File Mark is detected. When it has been detected, an End-of-Operation is generated, and tape motion stops. If no File Mark is detected, an End-of-Operation will be generated and motion will stop at Load Point.

12) Rewind Load (A10-07= 1000) - rewinds tape at high speed to Load Point. The controller remains Busy until tape is positioned at load point and End-of-Operation Status/Interrupt occurs. The 1732-3 stays Ready upon acceptance of this command.

Non-Stop Motion: Table 2-4 shows transition time in which a New Motion Function must be initiated to achieve Non-stop Motion after End-of-Operation Status/Interrupt occurs.

TABLE 2-4. NON-STOP MOTION TRANSITION

LCTT Speed	Transition Time		
	Write (Forward)	Read (Forward)	Backspace
25 ips	3.6 msec	2.6 msec	2.6 msec
50 ips	1.8 msec	0.5 msec	0.5 msec
Alternative for next Control Function	1. Write Data Record 2. Write File Mark/ Tape Mark	1. Read Motion 2. Search File Mark/ Tape Mark Forward	1. Backspace 2. Search File Mark/ Tape Mark Backward

Unit Select: A Unit Select selects a tape transport and its operating conditions or deselects a transport. To perform a Unit Select, load Q with W = 00, E = equipment number, D = 10. Load A according to Figure 2-3 and Table 2-5, and do an Output from A. Tape unit, density, and mode (BCD or binary) can be selected simultaneously or individually. Unit Select is rejected if Controller Active or a Program Protect fault occurs or if an illegal code is selected (for example, two densities chosen) or selection does not match the tape transport or controller settings. Unit Select clears the controller.

TABLE 2-5. TAPE UNIT SELECT CODES

Bits 9-7 Of A	Unit Select Jumper Setting
000	0
001	1
010	2
011	3

1) Character (A0 = 1) - This format consists of the lower 6 or 8 bits only of the 16 bit computer word. Master Clear sets character mode.

2) BCD (A1 = 1) - Data is read or written in even parity (615-73 only).

3) Binary (A2 = 1) - Data is read or written in odd parity. Master Clear sets Binary code. Binary is selected by each Director Function that does not call for BCD.

4) Select 800 bpi (A3 = 1) - Data is recorded at a density of 800 bits per inch.

5) Select 556 bpi (A4 = 1) - Data is recorded at a density of 556 bits per inch.

6) Select 1600 bpi (A5 = 1) - Data is recorded at a density of 1600 bpi in the PE format. This bit can only be used with the PE formatter. Switching between NRZI and PE occurs only when tape is at Load Point (BOT).

7) Assembly/Disassembly Mode (A6 = 1) - In this format the computer word is disassembled into two 6-bit (seven-track) or 8-bit (nine-track) tape words. During a Read, the two tape words are assembled into a single computer word.

8) Tape Unit 0-7 (A9 = 7) - This code matches the Unit Select setting of the desired transport.

9) Select Tape Unit (A10 = 1) - This code and bits 9-7 of A select a tape transport.

10) Deselect Tape Unit (A11 = 1) - This bit disconnects a tape transport that is selected. Master Clear deselects all Units.

11) Select Low Read Threshold (A12 = 1) - This bit is used to select the low read threshold level used for data recovery.

The controller reverts to normal read threshold when:

(a) The Unit-Select function contains A12 = 0.

(b) After any EOP.

(c) Master Clear.

Buffered Input/Output: A Buffered I/O instruction initiates the transfer of data between the controller and the computer memory via the DSA. To execute Buffered I/O, load Q with W=00, E= (equipment number) and D=11. Load A with the first word address minus one (FWA-1) which contains the last address plus one (LWA+1). An Output from A instruction transfers the FWA-1 and LWA+1 into the controller (via the A/Q and DSA respectively).

The transfer of data will start after Write or Read Motion. The data transfer will terminate when current word address equals LWA+1, or when reading the End-of-Record is sensed. Lost Data conditions will occur when the DSA does not keep up with the transfer rate.

A Buffered I/O instruction is rejected if EOP status is not set and Busy is set, the tape transport is not ready or a Program Protect Fault occurs.

Operation Defined by Q and Input to A

Read (D = 00): A Read operation transfers data from tape to the computer and checks parity. To perform a Read, load Q with W = 00, E = Equipment Number, and D = 00. An Input to A initiates the transfer of one 6-, 8-, 12- or 16-bit character to the lower bits of the A register.

The controller transfers characters to the computer until the computer stops requesting characters, or until the controller senses the end of a record. If the computer stops requesting characters, data transfer to the computer stops, but tape motion continues until the end of the record. A read is rejected if the controller is Not Ready, read motion has not been set, data status is not set, a Program Protect fault occurs, or a Buffered I/O operation is in process.

Director Status 1 (D = 01): Director status 1 is a status request which loads into the A register a status reply word showing the current operating conditions of the MTTC. The request is initiated by loading Q with W = 00, E = Equipment Number, D = 01, and executing an Input to A. Table 2-6 describes the contents of A register following the execution of this function. The Status Response section defines these bits.

Director Status 2 (D = 10): Director Status 2 is a status request which loads into the A register a status reply word of the MTTC. The request is initiated by loading Q with W = 00, E = equipment number, D = 10, and executing an Input to A. Table 2-7 describes the contents of A register following the execution of this function. The Status Response section defines these bits.

Current Address (D = 11): This instruction is a status request which loads into the A register the address of the next word being transferred. To perform a Current Address, load Q with W = 00, E = equipment number and D = 11, and initiate an Input to A.

Status Response

Director Status 1

Table 2-6 lists the meaning of bits set in the A register following a Status 1 request. These bits are further defined below.

Ready (A0 = 1): The tape transport is connected to the equipment and the tape system can perform a command.

Busy (A1 = 1): Equipment is in motion. The MTTC becomes Busy before a Reply is returned if a function can be performed.

Interrupt (A2 = 1): An interrupt condition exists and interrupt upon this condition has been selected. This bit is cleared when the interrupt is cleared.

Data (A3 = 1): A Read/Write data transfer can now be performed. It is cleared by a data transfer request, Lost Data or End-of-Record sequence.

End of Operation (A4 = 1): A new tape function can now be accepted. This bit sets at the completion of all tape motion functions. During Read and Write, End - of - Operation (EOP) signifies that parity status is valid. Master Clear clears EOP. A New Motion Function can also be used to clear EOP.

TABLE 2-6. DIRECTOR STATUS 1 RESPONSE BITS

Bit Set In A-Register	Meaning
0	Ready
1	Busy
2	Interrupt
3	Data
4	End-of-Operation
5	Alarm
6	Lost Data
7	Protected
8	Parity Error
9	End-of-Tape
10	BOT
11	File Mark
12	Controller Active
13	Fill
14	Storage Parity Error
15	Protect Fault

TABLE 2-7. DIRECTOR STATUS 2 RESPONSE BITS

Bit Set In A-Register	Meaning
0	556 bpi
1	800 bpi
2	1600 bpi
3	Seven Track
4	Write Enable
5	PE-Warning
6	PE-Lost Data
7	PE-Transport
8	ID-Abort
9	Low Read Threshold
10-15	(Not Used)

Alarm (A5 = 1): This status bit monitors those conditions requiring the attention of the program or the operator. The following conditions set this bit as well as their own status bit:

1) End-of-Tape
2) Parity Error
3) Lost Data
4) File Mark
5) The Controller goes Not Ready during an operation
6) Storage Parity Error
7) Protect Fault
8) ID - Abort
9) PE - Lost Data
10) PE - Warning

A New Motion Function or Clear Controller will clear Alarm.

Lost Data (A6 = 1): This bit indicates during an A/Q Read transfer that the Data Transfer register was not empty when a new frame of data was received from the tape transport. This clears Data Status and Data Interrupt.

This bit indicates during a Buffered I/O transfer that the computer's DSA bus has not been able to keep up to the MTTC data transfer requirements. During Buffered Output it initiates an End-of-Record sequence. During Buffered Input it stops data transfer. A New Motion Function clears Lost Data.

Protected (A7 = 1): This bit indicates that the Program Protect Jumper Plug of the selected tape transport is set.

Parity Error (A8 = 1): An error was detected during data transfer from transport, or the controller has read or written a File Mark; or done a Read operation in the wrong mode or density. The parity check is complete and a Parity Error status is valid at end of operation. This condition responds to transverse, longitudinal and cyclic redundancy parity errors. Parity Error is cleared by issuing a New Motion Function and a Clear Controller.

End-of-Tape (A9 = 1): An End-of-Tape (EOT) marker has been sensed. A New Motion Function clears EOT, only once when sensed.

Load Point (A10 = 1): The tape Load Point has been sensed.

File Mark (A11 = 1): A File Mark has been sensed. It is cleared on a New Motion Function.

Controller Active (A12 = 1): MTT Controller is active controlling tape motion.

Fill (A13 = 1): If an odd number of tape words is read, this status will be set to indicate that the lower portion of the Read word is not a tape word. A New Motion Function clears Fill.

Storage Parity Error (A14 = 1): Storage Parity Error has occurred during a DSA channel transfer. A MTT controller New Motion Function clears Storage Parity Error.

Protect Fault (A15 = 1): The computer's Protect Fault flag was active during a MTT controller-DSA channel transfer New Motion Function clears Protect Fault.

Director Status 2

Table 2-7 lists the meaning of bits set in the A register following a Status 2 request. These bits are further defined below:

556 bpi (A0 = 1): The selected tape unit is set to operate at a density of 556 bits per inch.

800 bpi (A1 = 1): The selected tape unit is set to operate at a density of 800 bits per inch.

1600 bpi (A2 = 1): The selected tape unit (nine-track MTT only) is set to operate at a density of 1600 bits per inch.

Seven Track (A3 = 1): The selected tape unit is a seven-track transport.

Write Enable (A4 = 1): The File Protect ring is in the supply reel and the tape has been loaded. Write operations may now be performed.

PE-Warning (A5 = 1): This bit indicates an error in the PE Formatter which did not affect the data transfer. The following conditions set this bit:

a) Corrected Dropout; one dropout occurred during reading of present record.

b) Wrong Postamble; Postamble exceeds 48 zeros or contains ones. This is cleared by a New Motion Function.

PE-Lost Data (A6 = 1): This bit indicates an error in the PE formatter which affected the data transfer. The following conditions set this bit:

a) skew buffer overflow
b) multitrack dropout
c) preamble format error

PE Transport (A7 = 1): Selected transport (nine-track MTT only) can record 1600 bpi density and the PE Formatter is in.

ID Abort (A8 = 1): 1600 bpi was selected (nine-track MTT only) but no Identification burst was detected after starting of tape motion from BØT. ID Abort triggers Alarm and tape motion is stopped. Operation will continue after issuing a New Motion Function and without further check of ID.

Low Read Threshold (A9 = 1) The Low Read Threshold is selected.

INTERRUPTS

Interrupts are selected by the Control Function. They may be cleared by:

1) Issuing a Clear Interrupt which clears both the Interrupt Request and the Interrupt.

2) Re-issuing the Interrupt Request except for the Alarm Interrupt when the Alarm condition still exists, e.g., End-of-Tape.

3) Issuing a Clear Controller.

4) Transferring data in the case of the data interrupt.

5) Reselecting a unit.

OPERATION

The positions for the jumper plugs indicated herein are located on the PWB's as shown in Table 2-8 and in Figures 2-4 and 2-5. The PWB's referred to may be accessed by opening the front cover of the enclosure and removing them after turning power off.

On the Q-Channel PWB (installed in Location 12):

Equipment Number Jumper Plugs

These four jumper plugs are used to represent any number from 0 to 15_{10}. They are used to assign an equipment number to the MTTC. Any instruction sent by the computer must be accompanied by an equipment number (bits Q7-Q10) that matches the settings of the jumper plugs. The W=0 must also be set. The position is set if the jumper plug is inserted. Refer to Figure

Scanner Jumper Plug

When performing maintenance operations and for initial installation of the controller, the Scanner jumper plug should be adjusted. These are four jumper plugs, only one of which should be inserted as follows:

1) Middle
2) First
3) Last
4) One
5) Out (no jumper)

These names reflect the controller's position within the DSA bus and varies with each system.

Protect On/Off Jumper Plugs

There are four jumper plugs; one per tape transport. When any tape transport is selected, this jumper when placed allows only protected instructions (except status requests) to access the MTTC.

If a buffered input is initiated by a Protected instruction, a Protect signal is sent to the computer allowing data to be written into any storage location, regardless of Protect setting.

Speed Select Jumper Plugs

There are four jumper plugs; one per tape transport. These jumpers should be set according to the speed of the corresponding tape transport - either high speed (High = 50 ips) or low speed (25 ips) is selected. With the jumper plug inserted, High speed is selected. With the jumper plug out the low speed is selected.

Track Select Jumper Plugs (Table 2-9)

There are four jumper plugs; one per tape transport. These jumpers should be set according to the track type (seven-track or nine-track) of the corresponding tape transport. With the jumper inserted, it represents a nine-track tape transport.

Modulation Select Jumper Plugs (Table 2-9)

There are four jumper plugs; one per tape transport. These jumpers should be set according to the capability of the tape transport - either NRZI or PE (provided nine-track and Not Dual Mode are selected). With the jumper in, it represents a tape transport using PE modulation only.

Dual Mode Jumper Plugs (Table 2-9)

There are four jumper plugs; one per tape transport. These jumpers must be inserted when the MTT is capable of dual mode operation (NRZI/PE) provided the Track Select jumper plugs are also set to nine-track.

TABLE 2-8. JUMPER PLUG LOCATIONS

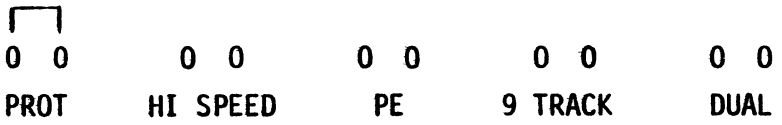
Jumper Plug	Assembly	Slot	Position
Equipment Number	Q-Channel	12	At U2
Scanner Select	Q-Channel	12	At U2
Protect On/Off	Lower Data	13	At U1
Speed Select	↕	13	At U1
Track Select	↕	13	At U18
Modulation Select	↕	13	At U18
Dual Mode Select	Lower Data	13	Above U35

TABLE 2-9. LEGAL TRACK-MODE-MODULATION JUMPER PLUG SETTINGS

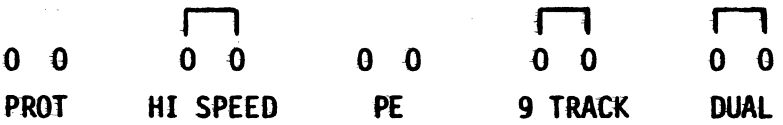
Transport Type	Jumper Setting		
	Track 9	Mode Dual	Modulation PE
7 Track NRZI	OUT	OUT	OUT
9 Track NRZI Only	IN	OUT	OUT
9 Track PE Only	IN	OUT	IN
9 Track Dual Mode	IN	IN	OUT

Example for using jumper plugs (see page 2-25):

7-Track, Protected, 25 ips:



9-Track, Not Protected, 50 ips, Dual Mode:



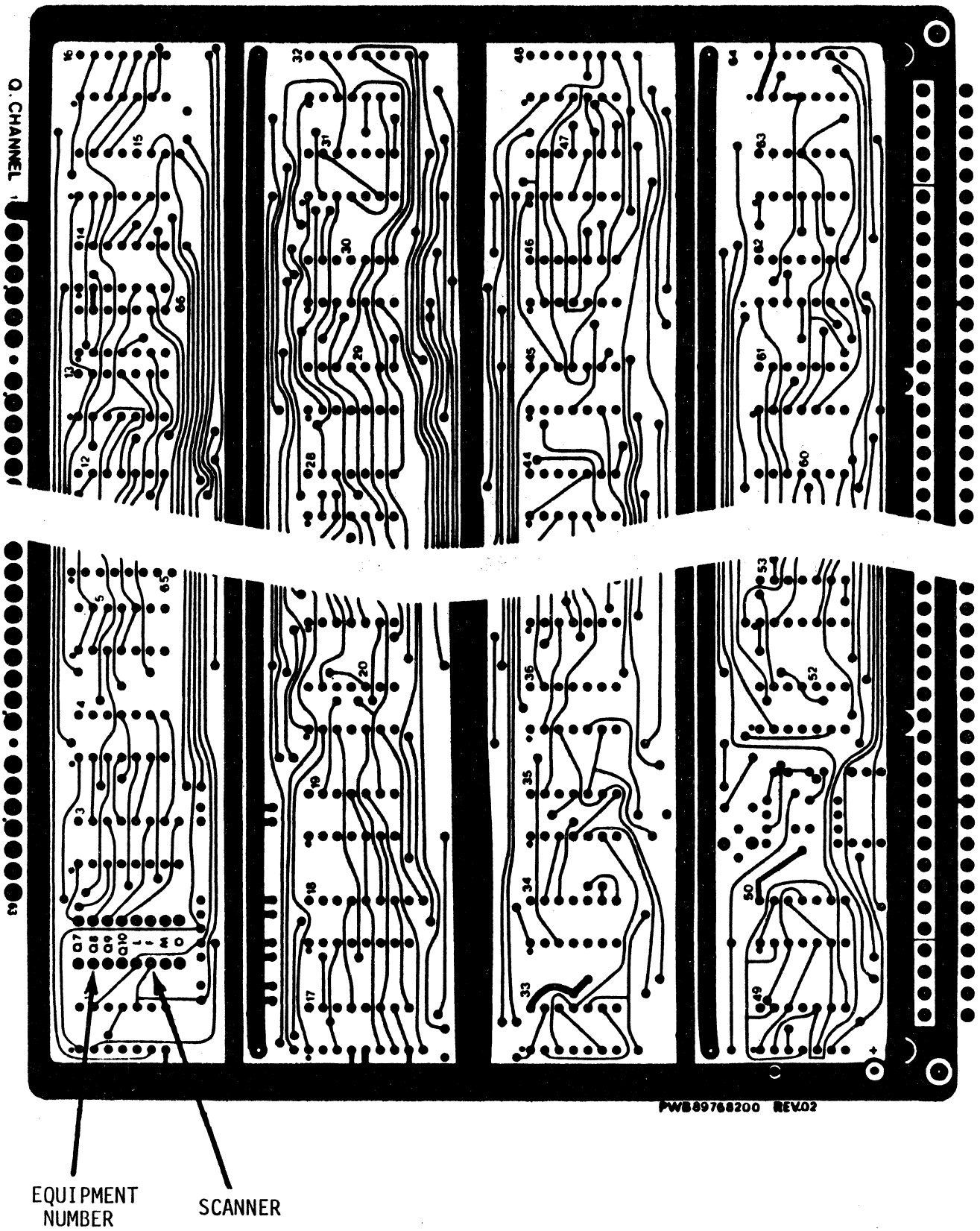


Figure 2-4. Q-Channel Showing Jumper Plug Positions

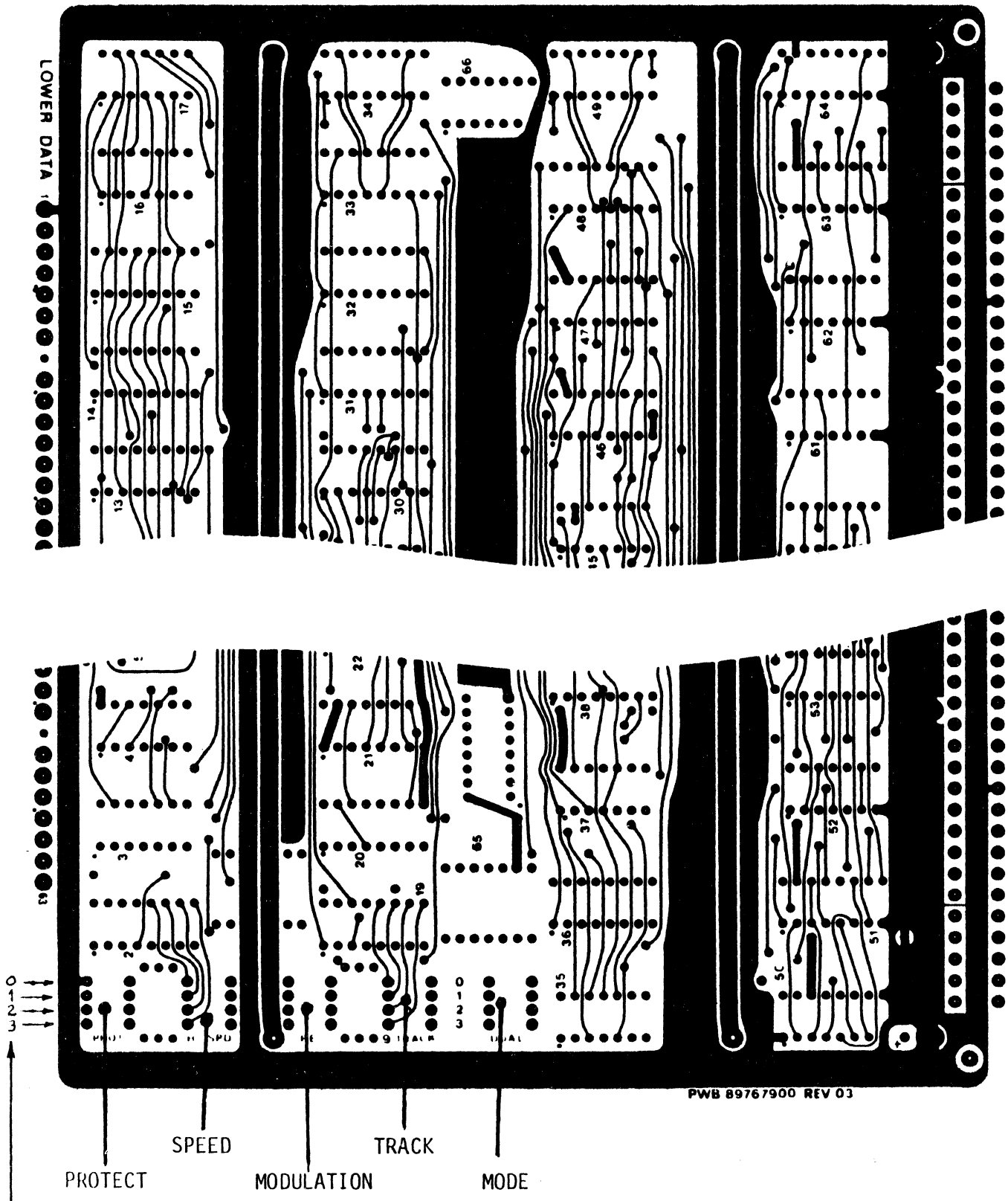


Figure 2-5. Lower Data Section Showing Jumper Plug Positions

SECTION 3

INSTALLATION AND CHECKOUT

INSTALLATION

Unpacking

1. Carefully remove wrapping from the 50-PAK controller cards. Check for physical damage to each card and record damage on the packing list. Check that part numbers agree with parts list.

2. Remove wrapping from cables and check for physical damage. Record damage on packing list. Check that part numbers agree with packing list.

Physical Limitations

Care must be taken to prevent damage to the controller cards. The cards must not be flexed, bent or dropped.

Power Requirements

The controller cards require +5 vdc derived from the power supply of the computer.

Cabling and Connectors

An external interconnecting cable is available for use with the controllers for connection between the computer and the tape transport. The external cable is 20 feet long (part number 89775500).

The internal cable (part number 89700200) used between the back of the computer and the connector pins on the back plane, is 18 inches long.

The interrupt cable (part number 89724702) is 13.8 inches long. Refer to the wire list for pin assignments for this cable.

The Wire List for pin assignments will be found in Section 9.

Cooling Requirements

The controller cards are cooled by the forced air system of the computer. No further cooling is required. Refer to the computer customer engineering manual (89633300) for further information concerning cooling capabilities of the computer.

Environmental Considerations

The environmental considerations necessary for operation (or storage) of the controller cards are listed in the Detailed Specifications of Table 1-1.

Preparation and Installation

To install the controller perform the following:

1. Remove the air-flow block from lower slide of each card slot to be used.

2. Inspect the enclosure, card slots, PW board slides and connector pins, for physical damage.

3. Place the jumper plugs on the Q Channel and Lower Data Section PWB's as indicated in Table 2-9 and Figures 2-4 and 2-5.

CAUTION

Do not install PWB's or cables on computer or expansion enclosure with power on.

4. Place the Interrupt Cable in the positions on the back plane as shown in Table 3-1.

5. Install controller internal cable in location 11, P2, and 14, P2, on back plane and the output connector at the output location provided.

6. Carefully install the controller PWB's in the assigned card slots. The card must slide in smoothly. The slot locations are as shown in Table 3-2.

TABLE 3-1. INTERRUPT CABLE POSITIONS

LCTT Controller	Position
A/Q Interrupt	Slot 12 P2A16

Selection may be made from any of the following:

CPU	(Position)
Line 1	Slot 25 P1B10
" 2	" 25 P1A7
" 3	" 25 P1B7
" 4	" 25 P1A5
" 5	" 25 P1A6
" 6	" 25 P1B6
" 7	" 25 P1B5
" 8	" 26 P1A10
" 9	" 26 P1B10
" 10	" 26 P1A7
" 11	" 26 P1B7
" 12	" 26 P1A5
" 13	" 26 P1A6
" 14	" 26 P1B6
" 15	" 26 P1B5

CHECKOUT

1. Refer to Section 2 of this manual for operation of the controller.

2. Determine that proper voltages are supplied to the controller card measuring +5 vdc between test points 1 and 63 on each card.

3. Perform diagnostics check as described in the System Maintenance Monitor (SMM17) Manual, Publication Number 60182000.

TABLE 3- 2. MTTC PW BOARD LOCATIONS

Assembly	PW Roard Number	Location (Slot) in Computer
Tape Interface	89648000	11*
Q-Channel	89648300	12**
Lower Data Section	89647700	13**
Upper Data Section	89647400	14*

* Internal cables will be connected to back plane at locations 11, P2 and 14, P2.

** Jumper plugs will be located on the PWA's located in slots indicated.

SECTION 4

THEORY OF OPERATION

INTRODUCTION

This section presents general and detailed functional decriptions of the equipment, using aids such as overall and detailed block diagrams and timing diagrams. Descriptions are keyed to the detailed logic diagrams in the diagrams section (section 5) and afford a basis in understanding the detailed description of the specific circuit in that section.

NOTE

It is assumed that the reader is familiar with Control Data equipment and with the programming characteristics of the Computer as described in the 1784 Computer System Reference Manual, Publication number 89637600.

The basic configuration is shown in Figure 4-1 and the block diagram in Figure 4-2.

GENERAL

The FA446-A Magnetic Tape Transport Controller (MTTC) transfers data between the computer and the magnetic tape transport (MTT) either directly in NRZI modulation or in phase modulation via the FV618-A Phase Encoding Formatter (PEF).* Communication with the computer is either via the A/Q Registers or the DSA Channel. The format is either Character or Assembly/Disassembly, one or two character word, respectively.

Communication with the MTT is via nine Read Data and nine Write Data lines with the appropriate strobe signal, according to either nine or seven track (9T, 7T) standard format. Communication with the PEF is via the following 9-bit buses: PEWrite Data In, PEWrite Out, PERead Data Out (with the appropriate strobe signals).

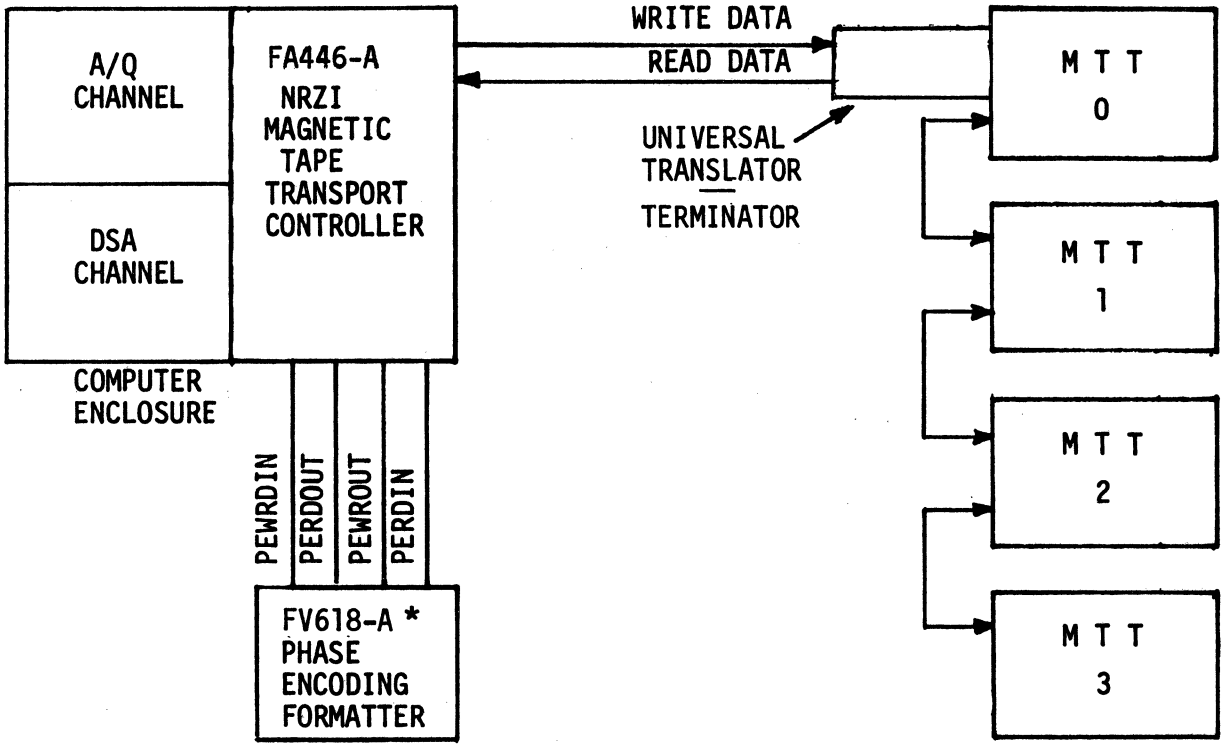


Figure 4-1. Basic Configuration

* Information on FV618-A is not contained in this manual. Refer to FV618-A Phase Encoding Formatter Customer Engineering Manual 89796100.

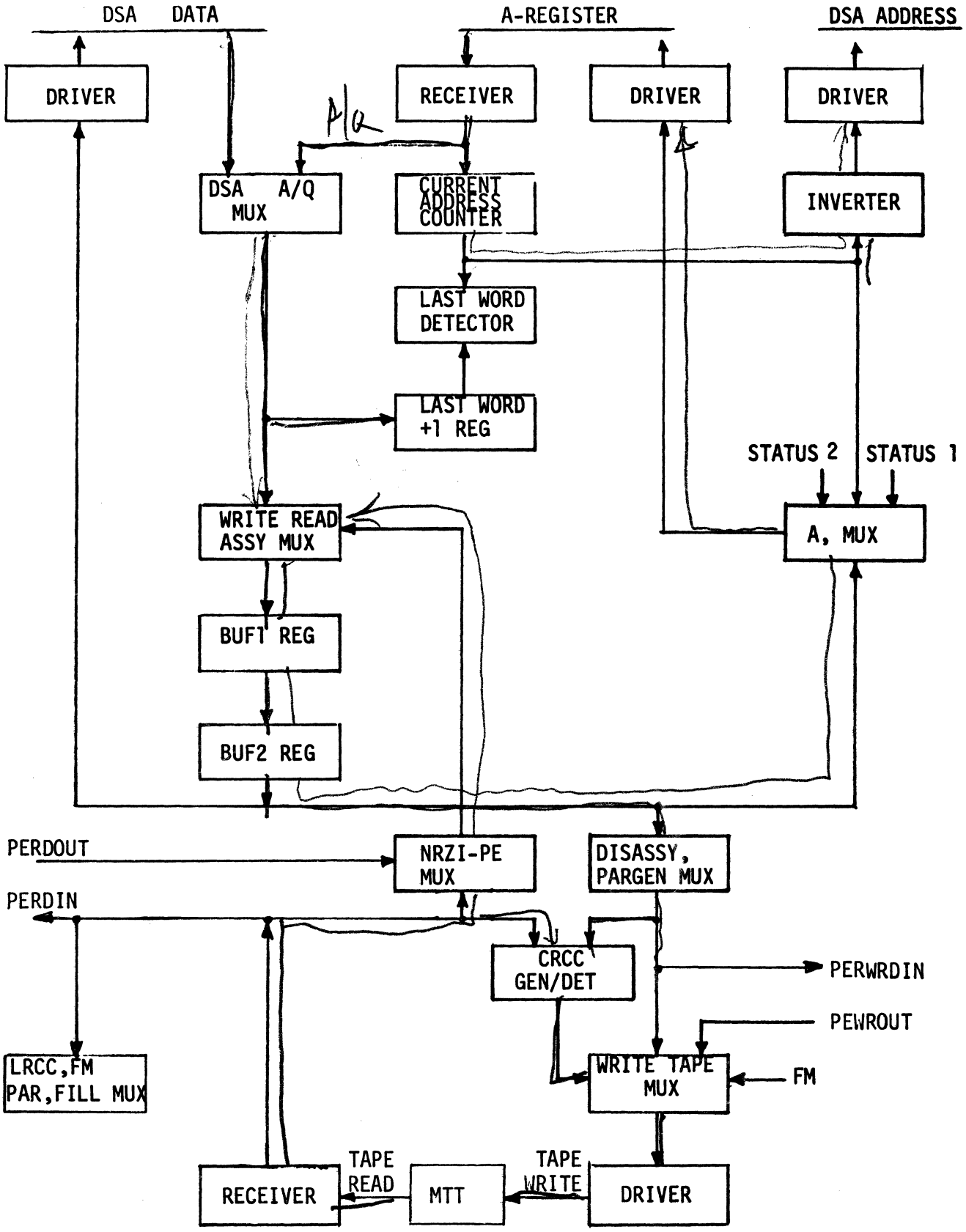


Figure 4-2. Controller Block Diagram

The MTTC executes the following computer instructions according to the system's requirements:

Write Data
Control Function
Unit Select
Buffered I/Ø
Read Data
Read Status 1
Read Status 2
Read Current Address

The MTTC controls the following motion functions of the tape transport:

Write Motion
Read Motion
Backspace
Write File Mark
Search File Mark Forward
Search File Mark Backward
Rewind - Load

Vertical and Horizontal Parity are checked while writing.

Vertical/horizontal Parity and CRC are checked when reading. Two 16-bit Data Buffers are provided for in order to decrease the probability of Lost Data.

The MTTC communicates with up to four tape transports of mixed types, having a speed of either 25 or 50 ips. The MTT may have the densities and modulation as indicated in Table 4-1.

TABLE 4-1. DENSITY - MODULATION SELECTIONS

TRACKS	DENSITY	MODULATION
9	800 BPI	NRZI MODULATION
9	1600 BPI	PE MODULATION
9	800/1600 BPI	DUAL MODE NRZI-800 BPI PE-1600 BPI
7	556/800 BPI	NRZI MODULATION

WRITE DATA PATH

Data from the A-Register or DSA Data Bus is transferred to the tape transport. The block diagram shows the data path.

1. A/Q transfer: A word from the A-Register passes through the receivers to the A/Q-DSA Multiplexer, to the Read/Write Assembly Multiplexer, through the Buffer 1 Registers and Buffer 2 Registers. The characters are transferred via the Write Tape Multiplexer and Drivers to the MTT. Every character passes through the CRCC Generator and at the end of the record the CRCC is transferred to the tape. In order to write a File Mark, the FM character and related LRCC is transferred through the Write Tape Multiplexer.

2. DSA Transfer: The FWA-1 Control Word is transferred from the A-Register to the Current Address Counter. The LWA+1 Control Word is transferred from the DSA Data Bus via the A/Q DSA Multiplexer to the Last Word+1 Register. All the succeeding words pass through the A/Q DSA Multiplexer to Read/Write Assembly Multiplexer and further to the double buffer as in A/Q transfer. When each word is transferred the Current Address Counter is incremented by one, and the contents of the CAW are passed through the Inverters and Drivers to the DSA Address.

READ DATA PATH

Data from the MTT is transferred to the A Register or DSA Data Bus.

1. A/Q Transfer: A character is transferred from the MTT through the Receivers to the NRZI/PE Multiplexer. The character is also transferred to the CRCC Generator and the LRCC, FM, Parity and Fill Check. The character passes through PE Read in the case of the Phase Encoded Read. The character is assembled into a word in the Read/Write Assembly Multiplexer and then transferred to the Double Buffer. From Buffer 2 the word passes through the A-Multiplexer and Driver to the A-Channel.

CLOCK

The basic clock pulse is generated by a 10.24 oscillator. It is divided by 4 to form the Gated Clock pulse train and the four clock time states T1 - T4.

REPLY/REJECT TIMING

When the computer Read or Write signal rises, and the Equipment Number of the Q-Registor matches the setting of the Equipment Number jumpers, the signals R1 - R5 are generated. R1 is set at the first clock pulse after the rise of the Read or Write signal. R1 is reset and R2 is set at the next Clock pulse, then R3, R4, and R5 are set and reset in turn. R5 is reset by falling of the Read or Write pulse.

At this time the following occurs:

At R2:

1. At the rising of R2 the Reply condition is strobed into the Reply Control FF.
2. The Control Function Strobing signal (STRCF) is generated.

At R3:

1. Strobing of one word in an A/Q Write operation (STRWR).
2. Strobing of First Word Address Minus One in a Buffered I/O instruction (STRBUF).

At R4:

1. Strobing of the Unit Select Code (STRUS).
2. Strobing of the Interrupt Selection and Motion Function in a Control Function operation.
3. Setting of the Data Status (or need in the DSA) in Write Motion (STRWMØT).

At R5:

1. Reply or Reject is transmitted to the computer.
2. At the falling of R5 the data transmitted to the computer (ENA, ENARD) is removed from the bus.

BASIC TIMING GENERATOR

The following waveforms are generated from T1 and T3 when the speed of the MTT is 25 ips (frequency is doubled if the tape transport speed is 50 ips):

1. PECHARCLK, frequency 40 kHz, symmetric waveform, changes with rising of T1.
2. PEClock, 160 kHz, symmetric, changes with T3.
3. GapClock, 8 kHz, 70% duty cycle, rising with T1, falling with T3.
4. 2FWC, when the 800 bpi transport is connected the freqency is 20 kHz. One pulse of 375 nanoseconds coinciding with T1. With the 556 bpi transports the frequency is 13.91 kHz.
5. Early WDS, Write Clock and WDS Shifted are at the frequencies shown in Table 4-2.

TABLE 4-2. TIMING GENERATOR FREQUENCIES

Speed/Dens.	800 bpi	556 bpi
25 ips	20 kHz	13.91 kHz
50 ips	40 kHz	27.82 kHz

The relations between the waveforms (Early WDS, Write Clock, WDSShifted) are shown in Figure 4-3. They are generated only at Write Motions after Start rises.

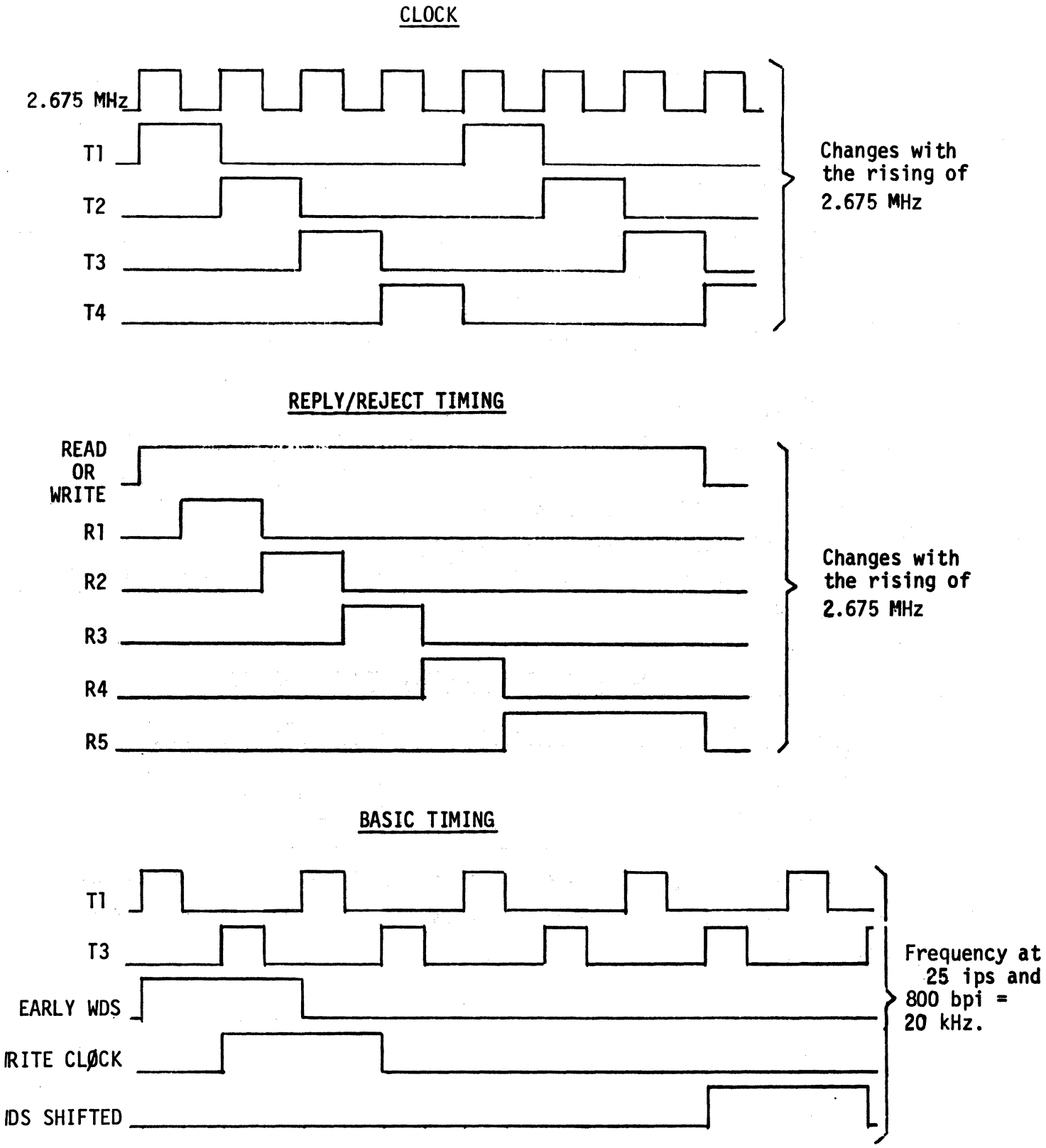


Figure 4-3. Basic Timing Generator Pulses

REPLY CONDITIONS

For every operation the Reply condition is determined and strobed into RC flip-flop (FF) at the rising of R2. The Reply conditions are determined according to the Q-Register, A-Register, Status FF's and return signals from the selected tape transport. The following equations determine the Reply conditions for the operations:

1. Read Data — RMØT·DATA·READY·PROTOK
2. Read Status I: — Always replied to
3. Read Status II: — Always replied to
4. Read Current Address: — Always replied to
5. Write: Data — WMOT·DATA·READY·PRØTØK
6. Control Function: — LEGCF·READY·PRØTØK

   Legal control function: $LEGCF = LEGMF \cdot (A10 + A8 + \overline{FILE\ PROTECT}) (\overline{BUSY} + NSCØND \cdot EOP)$

   Legal motion function: $LEGMF = A7 \cdot A10 + A10 \cdot A8 + \overline{A10} \cdot \overline{A8} \cdot \overline{A10}$

   Non Stop Condition : $NSCØND = LEGMF \cdot \overline{A10}\ (\overline{A7} + MOTCØDE7) (\overline{A8} + MØTCØDE8)$

7. Unit Select: — LEGUS·PROTØK

   Legal Unit select: $LEGUS = Z \cdot Z_F \cdot \overline{CONTACT} \cdot (PC160O + \overline{A5})$

   $Z = DUAL \cdot BØT \cdot 9T + DS(A5 \cdot 9T + A3 \cdot \overline{9T}) + DS(A3 \cdot 9T + A4 \cdot 9T)$

   $Z_F = A4 \cdot 9T + A5 \cdot \overline{9T} + A1 \cdot 9T + (A5 \cdot 9T + A3 \cdot \overline{9T}) \cdot (A3 \cdot 9T + A4 \cdot \overline{9T}) + A0 \cdot A6 + A1 \cdot A2 + A9 + A10 \cdot A11$

8. Buffered I/Ø: — $(EOP + \overline{BUSY}) \cdot READY \cdot PROTØK$

EXECUTION STROBES

The execution strobes are generated only if the appropriate reply conditions hold at time R2-R4, ENA:

ENARD = ENA•RC•RD
STRWR = R3•RC•WR
STRINT = R4•RC•CF
STRCP = R2•RC•CF
STRMF = R4•RC•CF•LEGMF
STRWMØT = R4•RC•CF•A7•$\overline{A8}$•$\overline{A9}$•$\overline{A10}$
STRUS = R4•RC•US
STRBUF = R3•RC•BUF
SELA0 = RD+DSI
SELAI = RD+DS2

UNIT SELECT

Unit Select operation selects the operation conditions. All the conditions are stored in flip-flops that are clocked by STRUS according to the contents of the A-Register. STRUS occurs at R4 if unit select operation is executed and the reply conditions are met. The operation conditions are preset by MC.

1. Select or deselect a tape transport. A transport can be selected only if A10 is set. It is deselected if A11 is set or MC is issued.
2. The Unit Number 0-3 is selected if A10 is set.
3. Character or Assembly/Disassembly format. Preset to Character by MC.
4. BCD or Binary Code. BCD is selected only if A01 is set, in all other cases Binary is set.

5. 800, 556, or 1600 bpi density. Density 800 bpi/1600 bpi can be changed only when a dual mode nine track transport is selected.
   (a) 556 may be selected if: seven-track transport.
   (b) 800 may be selected if: seven-track transport, or nine-track dual transport, or nine-track NRZI transport (not PE transport).
   (c) 1600 may be selected if: nine-track dual transport, or nine-track transport.

OPERATING CONDITIONS

The operation conditions that may be selected by the switches and the unit select operation are:

Switches

1. High or Low Speed: 50 ips or 25 ips.
2. 9T: nine or seven track tape
3. Dual, PE, ModeSel, nine-track and Density Status from the transport determine the operation density, 800, 556 or 1600 bpi.
4. PROTECT: protected or unprotected transport

Unit Select

1. A/D: Character or Assembly/Disassembly format
2. BCD: Binary or BCD code
3. File Protect: a signal from the transport that determines if data can be recorded or not because of the protect ring.

CONTROL FUNCTION

The control function executes three operations in sequence:

1. Clear Controller, if A00=1.
2. Clear interrupt, if A01=1 Select Interrupt if A2, A3 or A4 = 1
3. Motion function, if A07-A10 contains legal motion function.

CLEAR CONTROLLER

There are three levels of clear function in the controller:

1. MC: clears and presets all the flip-flop in the system. It is generated by manual master clear.
2. RES1: clears all flip-flops which contain operation conditions. It is generated by MC+STRUS+STRCF·A00. STRUS occurs at R4 and STRCF occurs at R2 if the reply conditions are met so the control function is executed.
3. RES2: clears the flip-flops that store status information and are not operation conditions. It is generated by RES1+STRMF . STRMF occurs at R4 if reply conditions are met and a motion function is executed.

INTERRUPT

There is one interrupt line, (location 16P2A16) and three kinds of interrupts: Data, EØP, Alarm. There is an enable flip flop for each interrupt, which is set by CØF according to bits 2-4 of the A-Register. The Interrupts are cleared by MC+STRCF·[A (0)+A (1)]. CØF occurs at R4 and STRCF at R2 so that the clear occurs before the setting. If the appropriate interrupts are enabled then the following interrupts can occur:

1. Data Status
2. Leading edge of End of Operation (EØP).
3. Alarm = EØT+Parity Error+Lost Data+File Mark +falling of Ready during an operation, Storage Parity Error, Protect Fault, ID Abort, PE Lost Data, PE Warning.

MOTION FUNCTION

The motion functions are executed by a Motion Function register that stores the function, a decoder that reads the appropriate control signal to the transport, a counter that determines the gaps and a Motion Sequencer that controls all the previous parts.

MOTION REGISTER AND DECODER

STRMF strobes bits 7-10 of the A-Register into the Motion Register. It strobes all legal motion functions except Backspace, SFM Backward and Rewind at BØT. The functions that are decoded from the register are:

RWIND LØAD
RWIND UNLØAD
FØRWARD
REVERSE

The strobing occurs at R4 and sets also Controller Active for all motions except Rewind Unload. The Motion Register is reset by STØP, IDABØRT, LØCKØUT or RES1.

GAP COUNTER

The gap counter is clocked by the Gap Clock circuit. It determines, together with the Function Decoder, 9T and BØT, the pre and post record delays as described in Table 4-3.

TABLE 4-3. GAP COUNT

FUNCTION	TOTAL PRE-RECORD DISTANCE**				TOTAL POST-RECORD DISTANCE***			
	9T		7T		9T		7T	
	BOT SENSOR	BETWEEN RECORDS	BOT SENSOR	BETWEEN RECORDS	BOT SENSOR	BETWEEN RECORDS	BOT SENSOR	BETWEEN RECORDS
Write Motion	*7.79	0.35	*7.79	0.55	0.42	0.42	0.57	0.57
Read Motion	*4.59	0.19	*4.59	0.19	0.26	0.26	0.26	0.26
Backspace	NO EXC	0.19	NO EXC	0.19	NO EXC	0.39	NO EXC	0.39
Write File Mark	*7.79	7.79	*7.79	7.79	0.42	0.42	0.57	0.57
Search FM Forward	4.59	0.19	4.59	1.79	0.27	0.27	0.27	0.27
Search FM Backward	NO EXC	0.19	NO EXC	NO EXC	NO EXC	0.29	NA	0.29

Distance is in inches

END OF OPERATION

End-of-Operation (EØP) is reset by RES2. EØP is set at the detection of a gap in a Read after a Write at WMØT, or RMØT, WFM or Backspace. At Search FM, EØP is set at the detection of a gap if FM is detected. When moving reverse (Backspace or Search FM Backword) and detecting BOT then EØP is set. When REWIND LØAD is executing and Ready rises, EØP is set. EØP is set also by PEEØP.

---

* Subtract 2.8 inches to obtain distance from BOT Marker.

** Total Pre-Record distance is measured from beginning of motion to beginning of data.

*** Total Post-Record distance is measured from end of data to end of motion.

MOTION SEQUENCER

The Motion Sequencer goes through states S0-S32 according to the timing diagram (Figure 4-4). S0 is set by STRMF, S1 by the End Prerecord delay, S2 by EØP, S31 and S32 by Post Record. S1 is the Start signal and S32 the Stop signal. If STRMF rises at S2, a non-stop motion will occur.

WRITE CONTROL

The Write Control directs the data through the Write path. The Write is initiated by STRWMØT that sets DATA FF (in DSA: NEED), requesting a data word from the computer. The computer responds with a Write operation. STRWR strobes the word into Buffer 1. When Buffer 1 is full and Buffer 2 is empty, a Transfer signal transfers the word from BUF1 → BUF2, and Data FF is set. A new word is transferred to Buffer 1 in the same way, but a Transfer is not generated until Buffer 2 is empty. When the Motion Sequencer is in Start the WDS empties Buffer 2 (in case of Assembly/disassembly two WDS are needed to empty Buffer 2).

When Buffer 2 is empty and Buffer 1 is full a Transfer command transfers the word from BUF1 → BUF2 and sets Data FF. Two things happen independently:

1. WDS empties Buffer 2.

2. Write operation fills Buffer 1.

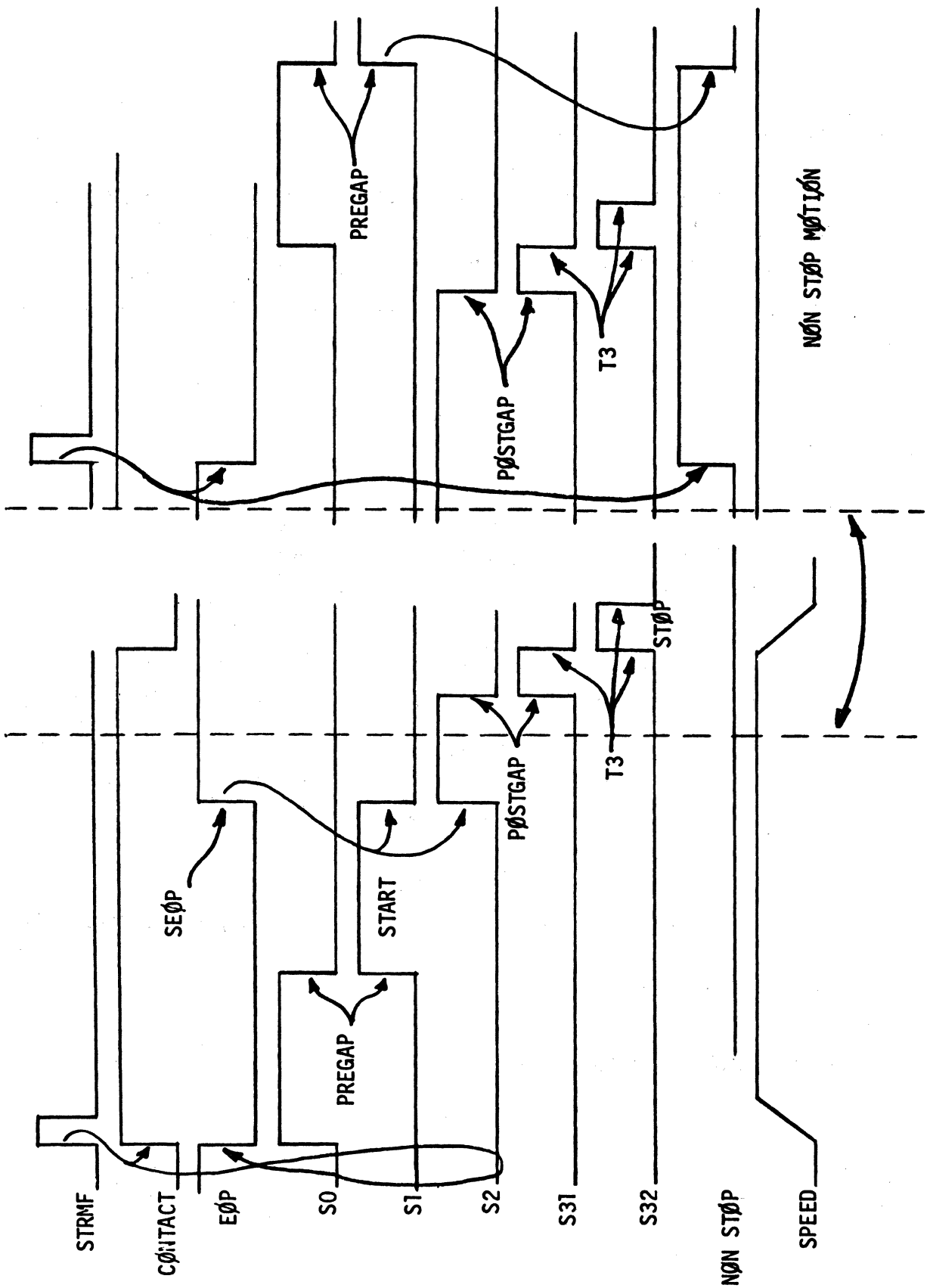


Figure 4-4. Motion Sequence

When the computer stops sending Write operations, both buffers become empty and an End of Record Sequence is set.

FIRST WØRD

The First Word flip flop is set by STRMF and is reset by the falling of the first Write Clock. It is used for two purposes:

1. If an Early WDS rises when Buffer 2 is not full, (i.e., no word was sent from the computer when requesting data) a Lockout condition occurs and the motion stops.
2. In WFM motion, EØRS is set by Early WDS if First Word is not set.

WRITE FM

In this motion the FM character is selected by the Write Tape selector. The FM character 17_8 is on seven-track and 23_8 on 9-track. A WDS to the tape strobes the FM character. In Write FM, only one character is written and then the End of Record Sequence starts.

END-OF-RECORD SEQUENCE

There are four kinds of EØRS:

Data, nine-track: data characters/3 spaces/CRCC/3 spaces/LRCC
FM, nine-track: FM character/7 spaces/LRCC
Data, seven-track: data characters/3 spaces/LRCC
FM, seven-track; FM character/3 spaces/LRCC

The EØRS is started if at Early WDS time, either BUF2 is empty at WMØT or First Word is reset at WFM. The Write EORS counter is enabled and then incremented by WDS Shifted. The presetting and decoding of that counter generates the EØRS.

READ CONTROL

If RMØT is in progress, the first RDS loads data into BUF 1, and as BUF 1 is full and BUF 2 empty, a TRANS signal moves contents of Buffer 1 into Buffer 2 and sets Data FF (or Need: DSA).

Two parallel processes continue:

1. The computer reads a word from BUF 2 in response to Data/Need.

2. The tape transport sends along with data characters the RDS signals. In A/D every second RDS, and in character format every RDS, fills BUFF1.

Every time BUF 1 is full and BUF 2 empty, BUF 1 information moves into BUF 2 and Data/Need is set. The data characters from the tape are checked for FM, LRCC, CRCC and Parity.

If an odd number of characters are read in A/D format and the End of Record is detected (the last character is still in BUF 1), one more transfer is initiated in order to read the last character, and Fill status is set.

The Read signal terminates when an End of Record is detected

SEARCH FM

During every motion (except Rewind) a File Mark is looked for. If two identical characters are detected (23_8 in nine-track and 17_8 in seven-track) with a gap of at least 2.5 characters between them then FM Status is set.

END-OF-RECORD DETECTOR

The EØR Detector is a counter that counts double the character frequency. Every RDS resets the counter to zero. A missing character is detected if the counter reads 4 (2-21/2 character spaces from the previous). The first Missing Character indicates termination of data and the second Missing Character indicates termination of CRCC.

When the EØR detector overflows (16 missing characters after the LRCC), the EØP FF is set, to indicate End-of-Record.

If after 10 counts (5-5 1/2 character spaces) no CRCC is detected, a special Missing CRCC signal toggles the CRCC register once more.

CHARACTER REDUNDANCY CHECK CHARACTER (CRCC)

The CRCC is a cyclic redundancy check character that is generated by manipulating all the characters sent to the tape. This CRCC is generated in the controller and sent to the tape after the data.

During reading, all the characters including the CRCC are manipulated in the CRCC generator, and a final pattern of 111010111 in that register indicates that no CRC error occurred.

LONGITUDINAL REDUNDANCY CHARACTER CHECK (LRCC)

The LRCC is a longitudinal parity check and is generated by the transport and written after the CRCC. When Reading, all the characters including the CRCC and LRCC are checked for even parity in every track.

STATUS

The status of the controller is indicated by various FF's throughout the system. The status information can be transferred to the computer by the two Read Status instructions. Most of the status FF's have been described. The remaining are described herein.

READY STATUS

A signal from the transport that indicates that it is selected and connected. Falling of Ready during an operation causes Alarm.

BUSY STATUS

This signal indicates that the tape is in motion.

LOST DATA STATUS

Lost Data is set if one of the following conditions occur:

1. Both buffers are full and the next RDS is detected in RMØT, if Last Word is not set in BUF I/Ø.

2. During BUF I/O transfer. Lost Data is set if both buffers are empty and WDS is generated in WMØT.

Lost Data is cleared by RES2.

PROTECT STATUS

Indicates that the selected transport is protected.

PARITY ERROR STATUS

Parity Error occurs in one of the following cases:

1. A vertical Parity Error was detected in a Data character.

2. LRC error detected at EØP.

3. CRC error detected at EØP in nine-track.

BEGINNING OF TAPE/END OF TAPE (BØT/EØT)

BØT is set from the detection of the Beginning-Øf-Tape Marker on the tape until the first Start signal rises.

EØT is set from the detection of End-Øf-Tape Marker on the tape until RS2.

FILL

Indicates that an odd number of characters were read from the tape in Assembly/Disassembly mode.

SECTION 5

LOGIC DIAGRAMS

KEY TO LOGIC SYMBOLS

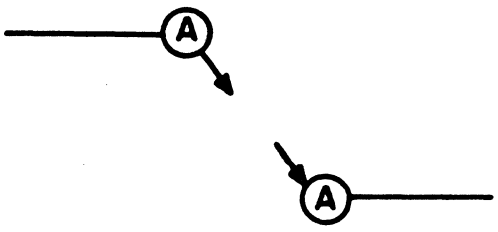
Publication 89723700 (Key to Logic Symbols) or equivalent, lists the symbols used in the logic diagrams in this manual and gives a short description of the functions they represent. The symbols conform generally to Control Data usage (Microcircuit Handbook, publication number 15006100), using the polarity logic convention.

The following paragraphs describe the signal flow conventions used.

SIGNAL FLOW

Input signals are drawn coming from the left or above; output signals are drawn going to the right or down.

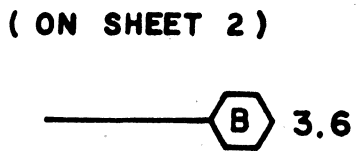
The signal lines are sometimes interrupted to allow logical grouping of components. At each such interruption one of the following indicators is used:

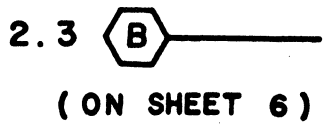


On-Sheet Continuation Reference Symbols

These symbols when used with the logic symbols in the following diagrams indicate that a connection exists between two points on a sheet. The arrows attached to each circle point from signal origin to signal destination. The letters, C, H, I, O and P are not used inside the circles, since they bear special significance on logic diagrams.

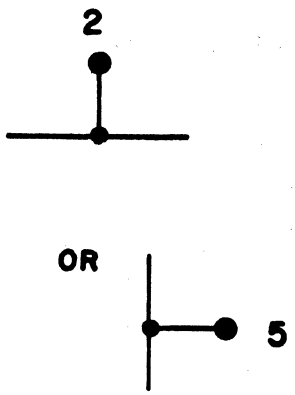
Off-Sheet Continuation Reference Symbols





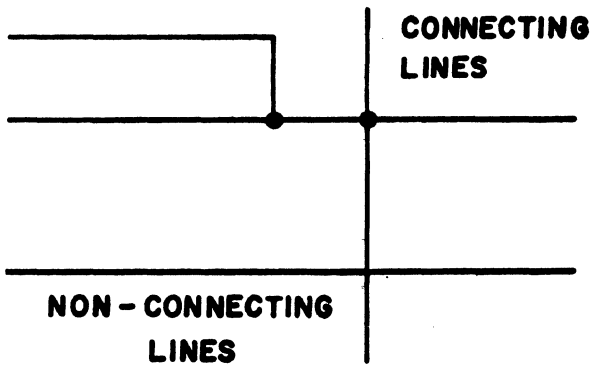
These symbols when used with the logic symbols in the following diagrams indicate that a common signal point exists between two sheets in a series of related drawings. These symbols point from output to direction of input as shown in the illustration. The letters C, H, I, O and P are not used in the hexagons, since they bear special significance on logic diagrams. The number(s) next to each hexagon indicate the sheet(s) that the signal is continued from or on. For instance, the numbers 3.6 refer to sheets 3 and 6, while 2.3 refers to sheets 2 and 3. It should be noted that the referenced sheet number(s) is always placed opposite the line extending from the hexagon. The sheet number where the signal originates is underlined.

Test Points



The test point symbol on the logic diagram shows the connection of a test point on the printed wiring board (PWB). The number adjacent to the symbol refers to the test point position on the PWB at the edge opposite the connectors. Only test point one is labeled on the edge of the PWB.

Connecting and Non-Connecting Lines

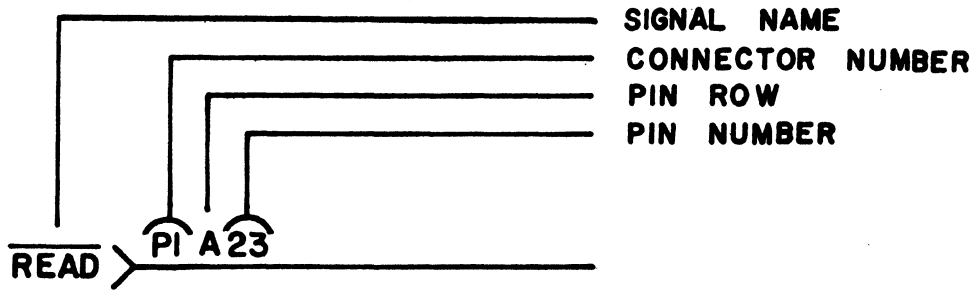


Lines connected to a common point or at a junction point are shown in the upper part of this illustration. No more than four lines are connected to a common point in the diagrams.

Lines crossing but not connected are shown in the lower part of this illustration.

Connectors

Connectors are represented on the logic diagram by the symbol for a female connector, for both input and output signals. The name of the signal is placed in the open end of the connector symbol (shown below), using the full name of the signal or the common abbreviation applicable to logic diagrams. The connector number, pin row and pin number are located above the line extending from the connector symbol.



LOGIC DIAGRAMS

Q CHANNEL PWB LOGIC (Logic Diagram 89768300)

CLOCK AND REPLY/REJECT LOGIC (Logic Diagram 89768300, sheet 2)

Clock

Transistors Q1 and Q2, the crystal, and U36-6 comprise an oscillator operating at 10.24 MHz. When $\overline{\text{STPCLK}}$ is high and EXTCLK is high, the square wave from U36-6 passes through U35-10, U35-8 and -4 to U35-6 and is filtered by the two transistors (Q1 and Q2), and the resistors (R1 thru R7) and capacitors (C1 thru C4). When $\overline{\text{STPCLK}}$ is low, U35-9 is low, U35-8 is high and U35-4 is high, then EXTCLK can be transferred to U35-5 and U35-6. U35-6 can be active with either the internal clock (10.24 MHz), or an external clock (EXTCLK).

The two FF's in U33 divide by four the signal from U35-6 (from U33-11 to U33-6). The output from U33-6 is 2.675 MHz (referred to hereafter as 3 MHz). This signal is divided by four again by the FF's of U50 (from U50-13 to U50-5 and -6, and U50-11 and U50-8 and 9). U49 combines these signals into time states T1 through T4. Refer to Figure 5-1 for time sequence generation.

A Gated Clock output for the Tape Interface, from U9-8 (to P2A29) is derived from the 3MHz output of U33-6 and the Start signal from the Upper Data Section, through P1B25.

---

* A signal name/pin list is included in Section 9.

Reply/Reject Logic

This module generates the timing sequence for all the A/Q interaction with the computer.

The Reply/Reject Timing is initiated by $\overline{\text{A/Q Read}}$ or $\overline{\text{A/Q Write}}$ and 3 MHz.

U24-6 = A/Q Read·Selected + A/Q·Write·Selected
(Selected = QØK)

ENA enables the A bus to the CPU. This signal is set by the falling edge of $\overline{\text{A/Q Read·Selected}}$ and is reset together with the rising of $\overline{\text{A/Q Reply}}$ or $\overline{\text{A/Q Reject}}$. This signal starts with Read, and terminates after falling of Read, together with Reply or Reject.

The R + W signal enables Operation Decoder U40.

R+W = ENA+A/Q Write·Selected

Operation of R0-R4 Shift registers (U8 and U7):

If $\overline{\text{MC}}$ = Logic 1, the FF R0 is set when U24-3 rises. R1 is set at the next rise of the 3 MHz clock. The setting of R1 clears R0, and at the next rising of 3MHz, R1 is reset and R2 is set. At the next clock, R2 is reset and R3 is set. Then R4 is set, R3 is reset and with the rising of next 3 MHz, R4 is reset and R5 is set.

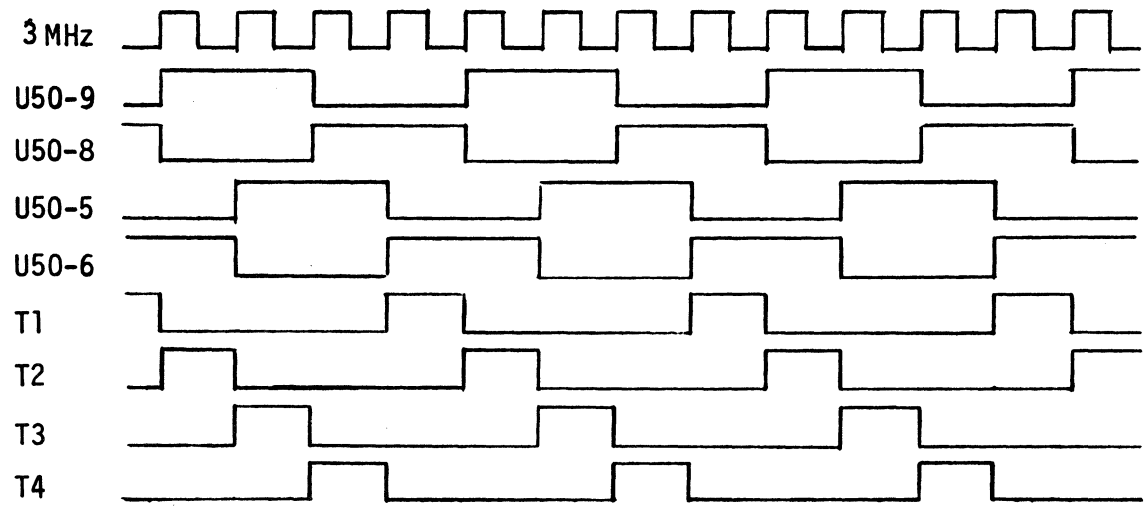


Figure 5-1. Clock-Time Sequence

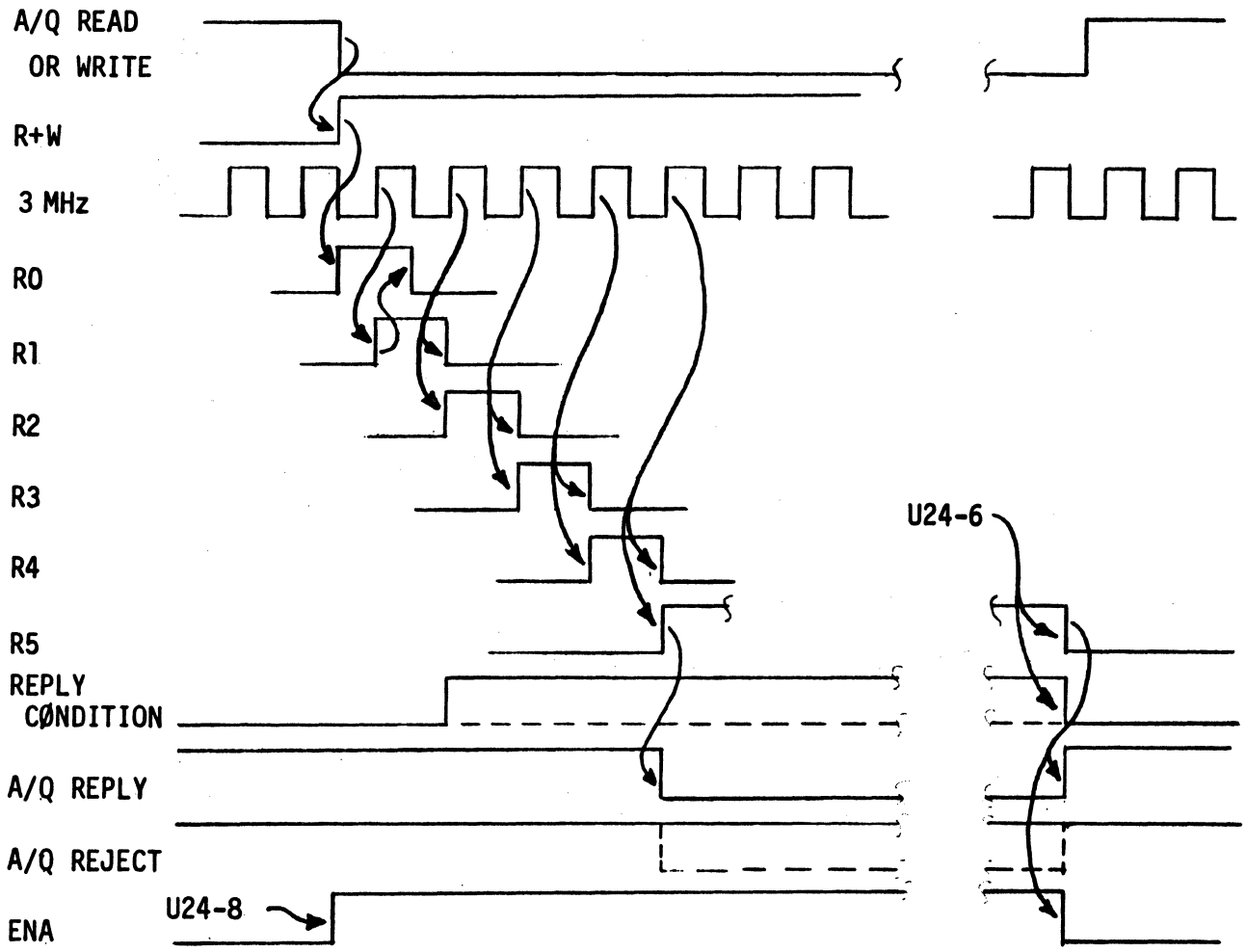


Figure 5-2. Reply/Reject Sequence

R2, R3, R4 are used for output-from-computer timing and ENA is used for the input. U24-6 resets R1 - R5 and RC, R5 resets A/Q Reply, A/Q Reject, and ENA. ENA is generated because the input data must stay valid until the rise of the $\overline{\text{A/Q Reply}}$ signal.

OFF-SHEET REFERENCE

OFF-SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION							
		2	3	4	5	6	7	8	9
A	T1	C-1			D-1				
B	T2	C-1			D-4				
D	T4	C-1			D-2				
E	—	B-2		C-2					
F	—	B-2		D-2					
G	R2	B-2		C-2					
J	R3	B-2		C-2					
K	R4	A-2		D-2					
L	READ EXT	A-4		C-4					
M	R+W	B-3		D-4					
N	SELECTED	B-4	C-2						
P	WRITE	C-4		D-4					
Q	STRMF			D-1	C-4				
R	$\overline{\text{ENARD}}$			C-2	D-4	C-4			
S	$\overline{\text{STR BUF}}$			C-2				B-2	C-4
T	$\overline{\text{STRWR}}$			C-2	C-4	C-4			
U	—			D-3				B-3	
V	DATA			B-4		D-1			
W	RMØT			A-1	D-2				D-4
X	—			B-4				B-2	
Y	WMØT			A-1	B-4				
Z	STRWMØT			A-3		D-4			B-4
AA	$\overline{\text{CONTACT}}$			A-1			A-3		
AB	$\overline{\text{TRANS}}$				C-1	D-4			B-4
AC	$\overline{\text{RES 2}}$				D-4	A-3	C-2		A-4
AD	DSA CØN				A-3				C-4
AE	—				C-1	B-4			
AF	—				C-2	B-4			
AG	BUFF 2 FULL				C-1	B-4	D-4		
AH	$\overline{\text{INCCA}}$				D-4			A-2	B-2
AI	(TI) RDS *				A-4	B-4			
AJ	$\overline{\text{RES 1B}}$				B-1	C-4			C-4
AK	$\overline{\text{RES 1A}}$				B-1		B-3	B-2	
AL	—				D-1				B-2
AM	—				A-3				D-4
AN	EØRS				C-4	C-4	D-2	A-3	
AP	—				C-3	C-4			
AQ	—				B-3	C-4			
AR	WDS SHIFTED				A-3		D-2		
AS	$\overline{\text{EØP}}$				A-3	D-4		B-3	D-4
AT	$\overline{\text{BUF}}$					D-4		A-2	
AU	LØST DATA					B-1		B-3	
AV	$\overline{\text{LØCK ØUT}}$					C-1	A-3		
AW	$\overline{\text{1ST}}$ WØRD					C-3	D-3		
AX	EARLY WDS					B-4	D-2		
AY	LAST WØRD					B-4		A-4	
AZ	A/D (LU)					A-3			C-4
BK				D-3					D-3

SHEET REVISION STATUS

1	2	3	4	5	6	7	8	9	REV
01	01	01	01	01	01	01	01	01	01
02	02	01	01	02	01	01	01	01	02
03	03	01	01	03	01	01	01	01	03
04	03	01	01	04	01	01	01	01	04

REVISION RECORD

ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
CK 690	RELEASED TO CLASS B	[illegible]	June 9.74	[illegible]	[illegible]
CK 766	ADD U9	Norm	Sep. 74	[illegible]	[illegible]
CK 800	ADD U11	Norm	Sep. 74	[illegible]	[illegible]
CK 862	CHANGE U10 FROM 146 TO 146K	Norm	Sep. 74	[illegible]	[illegible]

		2	3	4	5	6	7	8	9
BA	X2					B-4		A-2	B-4
BB	DSA WREN							B-2	C-2
BC	HALT							C-1	B-4
BD	RESET HALT							B-3	B-2
BE	NEED							B-3	C-2
BF	SCAN IN							B-1	B-4
BG	—					B-4			C-3

A.Y. 89844300
A.W. 89768200
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES
TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA

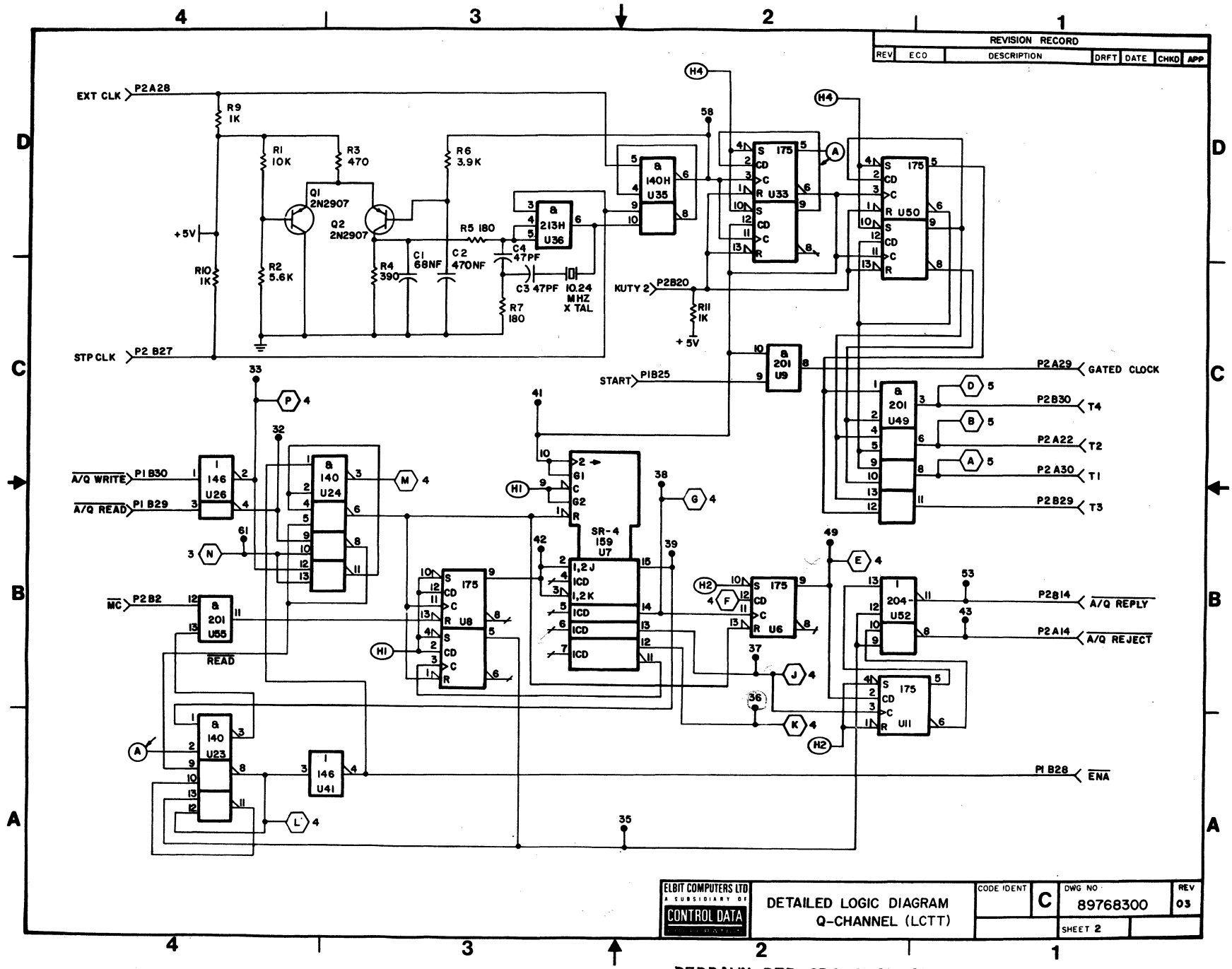
FIRST USED ON FA446-A

DWN	[illegible]	June 9.74
CHKD	[illegible]	Sept 74
ENGR	[illegible]	[illegible]
MFG		
APPR		

TITLE
DETAILED LOGIC DIAGRAM
Q - CHANNEL (LCTT)

CODE IDENT C
DRAWING NO 89768300
SCALE
SHEET 1 OF 9

REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 05



REDRAWN PER CDC STANDARD-ECO CK 798
SHEET IS REV 04

OPERATION DECODER (Logic Diagram 89768300 sheets 3 and 4)

The Operation Decoder generates the waveforms for the control of the interface with the computer. The inputs are from the computer's Q-register, timing signals from the Reply/Reject Logic, and certain status signals from the controller. The outputs are the Strobe and Select signals, and the Reply condition.

QØK is high when Q07 - Q10 match the setting of the Equipment Number and Q11 - Q15 equal to zero.

U40 generates eight active low signals. Each signal is a result of decoding of one of the computer instructions. The signals are decoded from A/Q Q00, A/Q Q01, A/Q Write and ENA. For Write instructions the timing is according to A/Q Write, for Read according to ENA. The signals are enabled by R+W.

$$U38\text{-}8 = RD \cdot Data \cdot RM\emptyset T + WR \cdot Data \cdot WM\emptyset T + CF \cdot LEGCF + BUF \cdot (E\emptyset P + \overline{Busy})$$

$$U37\text{-}8 = U38\text{-}8 \cdot Ready + US \cdot LEGUS + CF \cdot \overline{A_8} \cdot \overline{A_9} \cdot \overline{A_{10}}$$

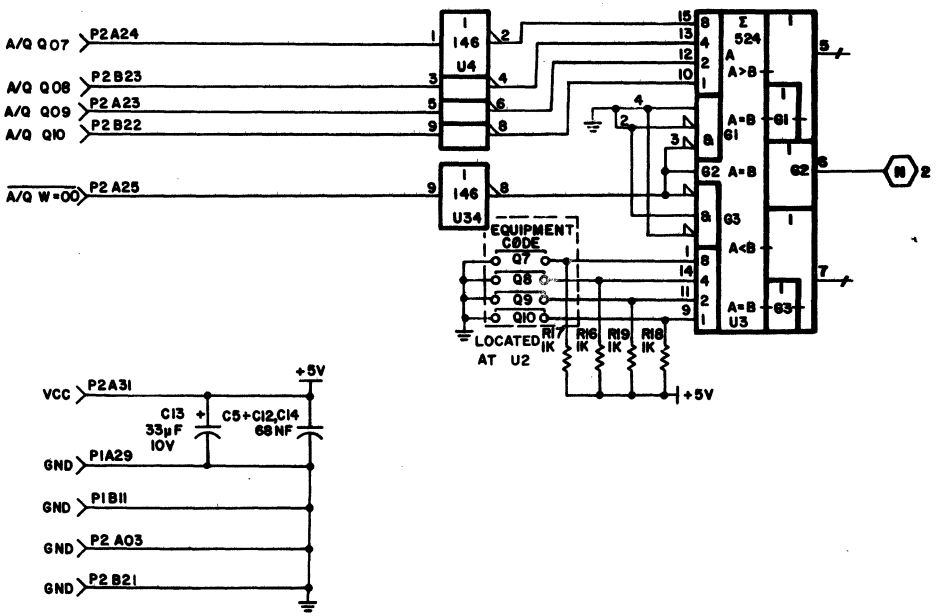
$$Reply = DS1 + DS2 + CA + U37\text{-}8\ (\overline{Protected} + A/Q\ Protected)$$

Signals that execute the computer instructions are listed in Table 5-1.

TABLE 5-1. COMPUTER INSTRUCTION EXECUTION

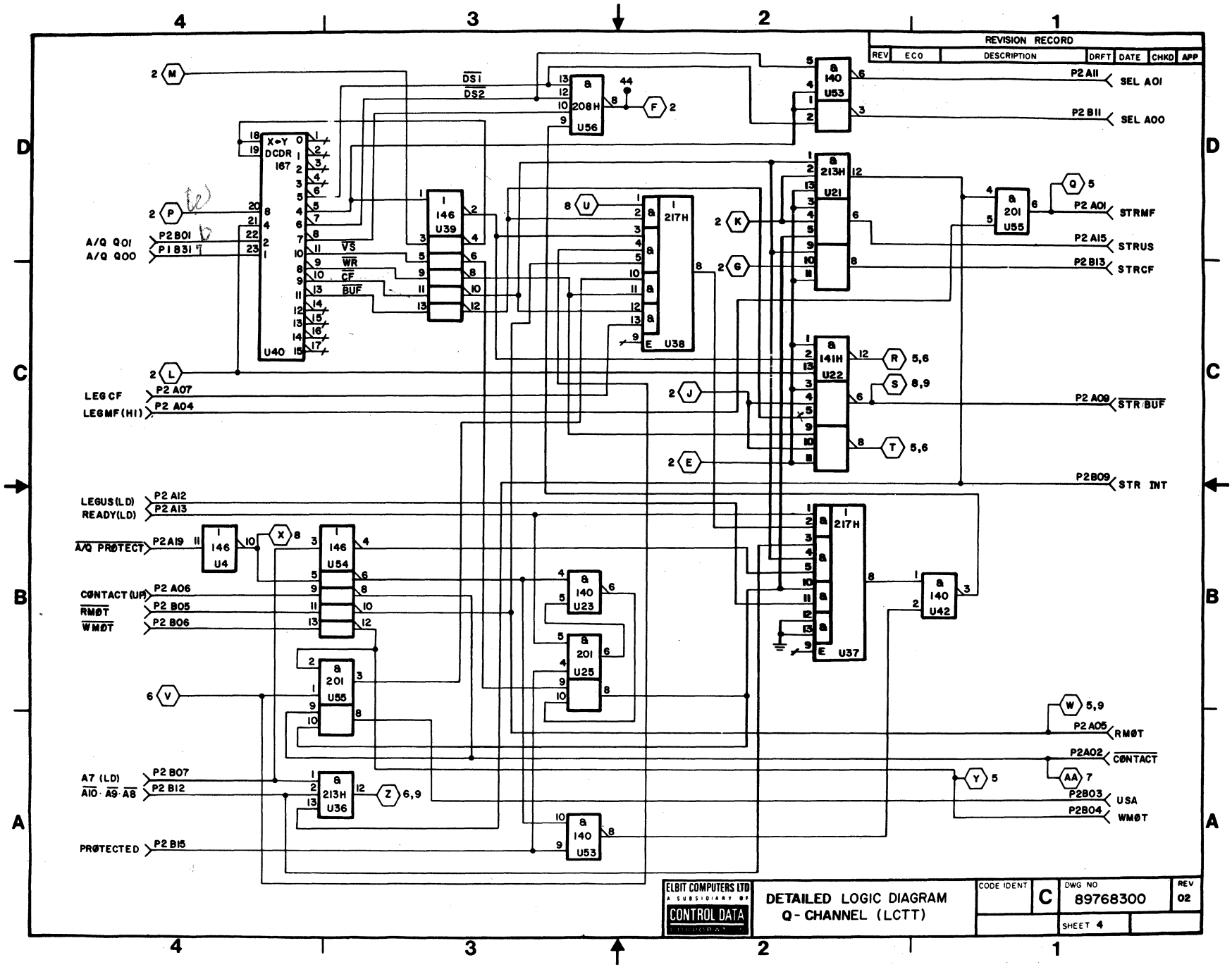
Output	Function	Description
U22-6	$\overline{\text{STRBUF}} = \overline{\text{R3}\cdot\text{RC}\cdot\text{BUF}}$	Starts Buffered I/O instructions
U22-12	$\overline{\text{ENARD}} = \overline{\text{ENA}\cdot\text{RC}\cdot\text{RD}}$	Strobes input data during Read instruction.
U22-8	$\overline{\text{STRWR}} = \overline{\text{R3}\cdot\text{RC}\cdot\text{WR}}$	Strobes output data during Write instruction
U53-3	SELA0 = RD+DS1	Controls input-to-A multiplexer
U53-6	SELA1 = RD+DS2	Control input-to-A multiplexer
U21-12	STRINT = R4•RC•CF	Sets interrupt enable register
U21-6	STRUS = R4•RC•US	Selects unit
U21-8	STRCF = R2•RC•CF	Starts control function
U55-6	STRMF = R4•RC•CF•LEGMF	Starts motion function
U36-12	STRWMØT = $\text{R4}\cdot\text{RC}\cdot\text{CF}\cdot A_7\cdot A_8\cdot A_9\cdot A_{10}$	Starts write motion
U55-8	USA = US•$\overline{\text{Contact}}$	Controls unit select multiplexer in Upper Data PW board

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM Q-CHANNEL (LCTT)	CODE IDENT C	DWG NO 89768300	REV 02
			SHEET 3	

REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 03



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SHEET IS REV 03

DOUBLE BUFFER & DATA CONTROL (Logic Diagram 89768300, sheet 5)

Double Buffer Control

The Double Buffer is described in a later section. The Double Buffer diagram is shown in Figure 5-3. (See Lower-, Upper Double Buffer).

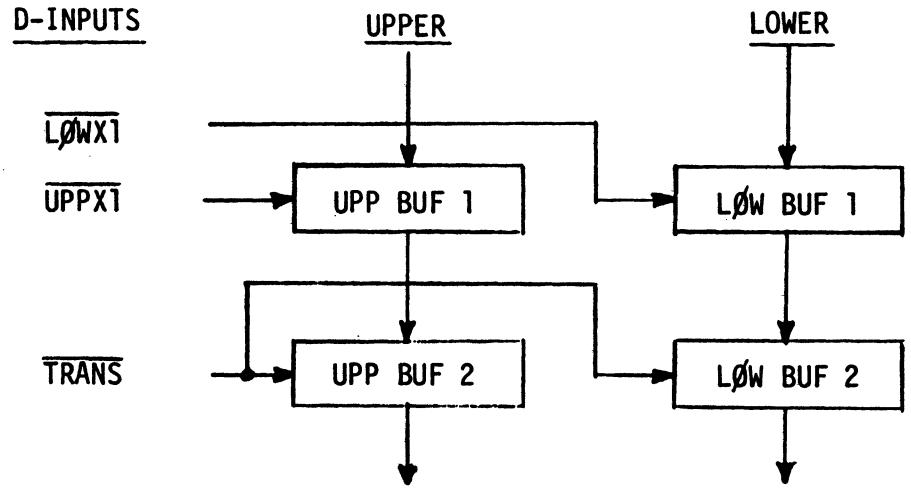


Figure 5-3. Double Buffer Control

The Double Buffer Control controls the transfer of data from the computer's A-register or DSA-Data to the tape interface lines while writing, or from the tape interface lines to the computer while reading. This module also controls the assembly/disassembly of the data.

The Double Buffer Control includes the following FF's:

1. Buf 1 Full: When high it indicates that Buf 1 contains valid data. (U63-9)(TP23)
2. Buf 2 Full: When high it indicates that the data on the output lines (U63-5)(TP9) of the Double Buffer are valid.

3. Upper : (U30-9) — When high the Upper Half Buffer is accessed.

4. Trans: (U42-11) (TP28) — Provides the timing for transfer from Buffer 1 to Buffer 2.

5. CLRLower: (U47-9) (TP25) — Initiates a dummy transfer of zeros in the Lower Half Buffer when an odd number of characters are read (in character format).

The data from/to the A-register is strobed by the rise of $\overline{\text{STRWR}}$ while writing and by the rise of $\overline{\text{ENARD}}$ while reading. The DSA-Data lines are strobed by the rise of $\overline{\text{INCCA}}$ (Increase Current Address). The data to the tape is strobed by WDS (Write Data Strobe), and the data from the tape is strobed by the fall of RDS (Read Data Strobe).

The Character Input signal to CPU has the following equation:

$$\overline{\text{A/Q Char Input}} = \overline{\overline{\text{A/D}} \cdot \text{ENARD}} \text{ (U59-6)}$$

Write Motion: Upper FF is set by STRMF, when A/D is low, Upper stays reset (U30-13) and when A/D is high, Upper toggles after each WDS (in NRZI by $\overline{\text{WDS Shifted}}$ and in PE by $\overline{\text{PWRQ Shifted}}$). U64-6 and 8 produce STRWR·WMØT, and the rise of this signal sets Buffl Full and strobes the A-register into Buf 1.

If Buf 2 Full is low and Buf 1 Full is high then U48-4 and 5 are high, U48-6 is low and U45-10 is high. Trans is set by the rise of T4 and reset by the rise of T2. The fall of Trans strobes Buf 1 into Buf 2 (at the rise of T2) and sets new data request. As WDS rises (strobes into the tape) at the rise of T3 and Buff 2 is strobed at the rise of T2, the data on the interface lines to the tape are valid at least 500 nsec before and after the strobing.

Buf 2 Full is set by the fall of Trans and is set by the rise of WDS if Upper is low (U48-1, 13 and 8).

Read Motion: Upper is set by STRMF when A/D is low. Upper stays reset (U30-13) and when A/D is high, it toggles with the falling of RDS (U44-9 and 8, U29-3 and 6, U45-1 and 2, and U30-11).

If Upper is high, the fall of RDS strobes the data from the tape into UppBuf 1. If Upper is low, the fall of RDS strobes the data from MTT into LowBuf 1 and sets Buf 1 Full.

If Buf 2 is low and Buf 1 Full is high a Trans pulse is generated as in Write Motion.

Buf 2 Full is reset by the rise of $\overline{\text{ENARD}}$, i.e., the strobing of A-register (U62-9 and 8, U48-9, 10 and 8, and U63-3) and is set by the fall of Trans.

If 1ST Space rises and $\overline{\text{Upper}}$·A/D·RMØT is high (U46-12, 13 and 11; U58-1, 2 and 3) then CLRLower is set. If Buf 2 Full is low and CLRLower is high a Trans pulse is generated and a last data request is set.

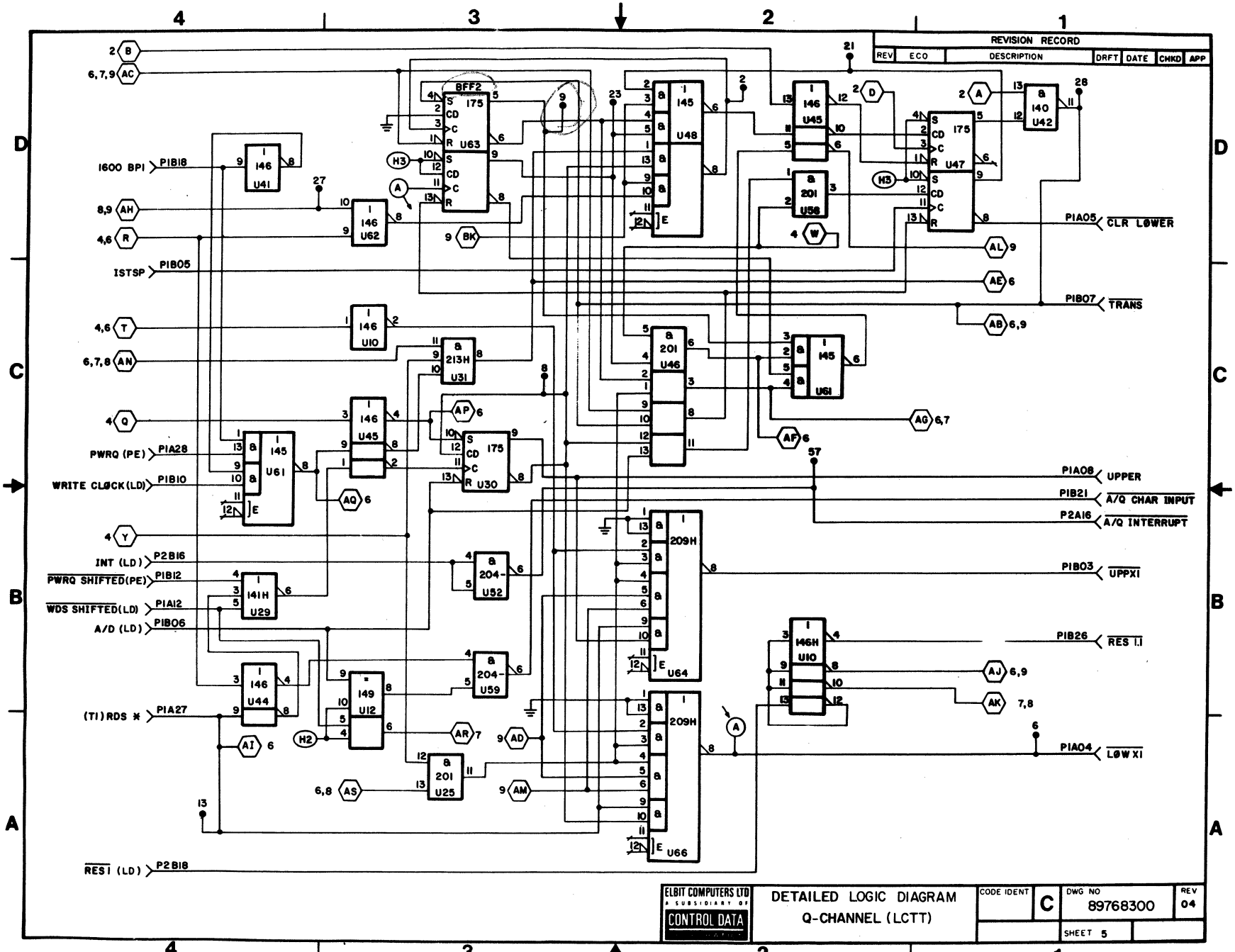
The Double Buffer Control also indicates the following conditions:

1. J46-6 - Buf 1 Full·RMØT sets Lost Data on next RDS

2. U46-3 - $\overline{\text{Buf 2 Full}}$·WMØT condition for Lockout, Priority, Lost Data and EØR Sequence

3. U61-6 - Priority Condition = $\overline{\text{Buf 1 Full·Buf 2 Full}}$·WMØT + Buf 1 Full·Buf 2 Full·RMØT

RES1 clears the FF's Buf 1 Full, Buf 2 Full, CLRLower.



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 05

DATA CIRCUIT (Logic Diagram 89768300 sheet 6)

This module includes three FF's: 1.) Data (U32-9) - request for input or output via the A/Q, 2.) Lost Data (U32-5) - indication of lost data condition, and 3.) 1st Word (U30-5) - high until the first word has been sent to the transport. This module includes also a part of WDS generation.

Data (U32-9) is set only if Buf I/O is low, by either rising of $\overline{\text{Trans}}$ (U42-11) or by STRWMØT (U28-10 and 8; U32-10). $\overline{\text{Trans}}$ transfers the data in the Double Buffer from Buf 1 to Buf 2, so when writing Buf 1 can receive a new computer word, Data is set. When reading, Buf 2 includes valid data that can be sent to the computer if Data is set. When writing, Data is first set by STRWMØT in order to transfer the first word. When reading, Data is first set by the first $\overline{\text{Trans}}$.

Data is reset by:

U31-12 = ENARD+STRWR+EØRS+Lost Data+FM+RES1+EOP

In the normal Data Transfer cycle during writing, STRWR (the signal that transfers the data into Buf 1) resets Data. During reading ENARD resets it. When writing EØRS indicates that the stream of data words is terminated so no more data can be requested from the computer, and Data is reset. If Lost Data is indicated, Data Transfer will terminate. In Read Motion, if a File Mark is detected it will not be transferred to the computer as data, and FM (detection) resets Data.

When U62-6 is high (Buf I/Ø or Lastword) and RDS occurs, and Buf 1 Full is high, then data is lost (data is transferred from the tape when both Buffers are full) and Lost Data is set (U32-2). Lost Data is also set by Buf I/Ø·WMØT·Buf 2 Full·WDS (U29-12). This indicates that a character is to be transferred to the tape although Buf 2 is empty. Note that this condition is a legal termination of Write Motion in A/Q transfer.

WDS is generated according to the following equation:

U29-1: WDS = WMØT·$\overline{\text{EØRS}}$·($\overline{\text{1600BPI}}$·Write Clock+1600BPI·PWRQ)
(sheet 4)

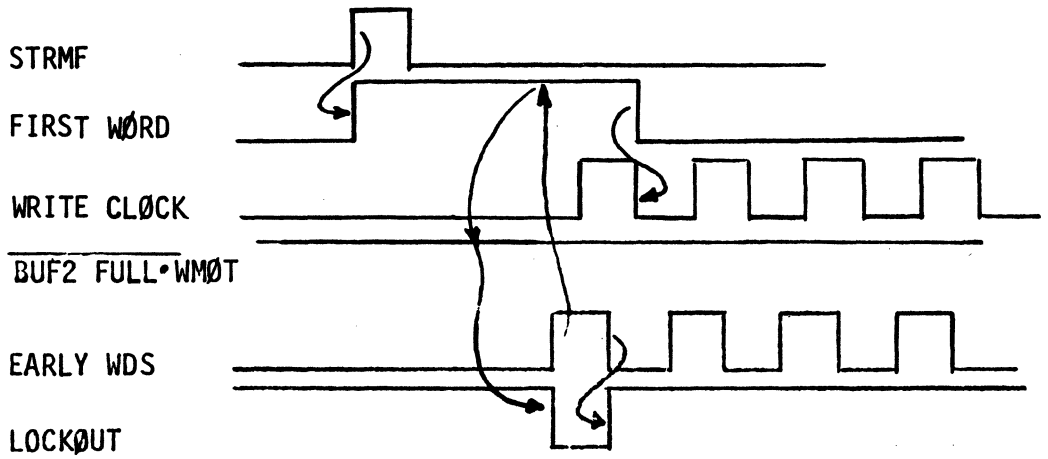
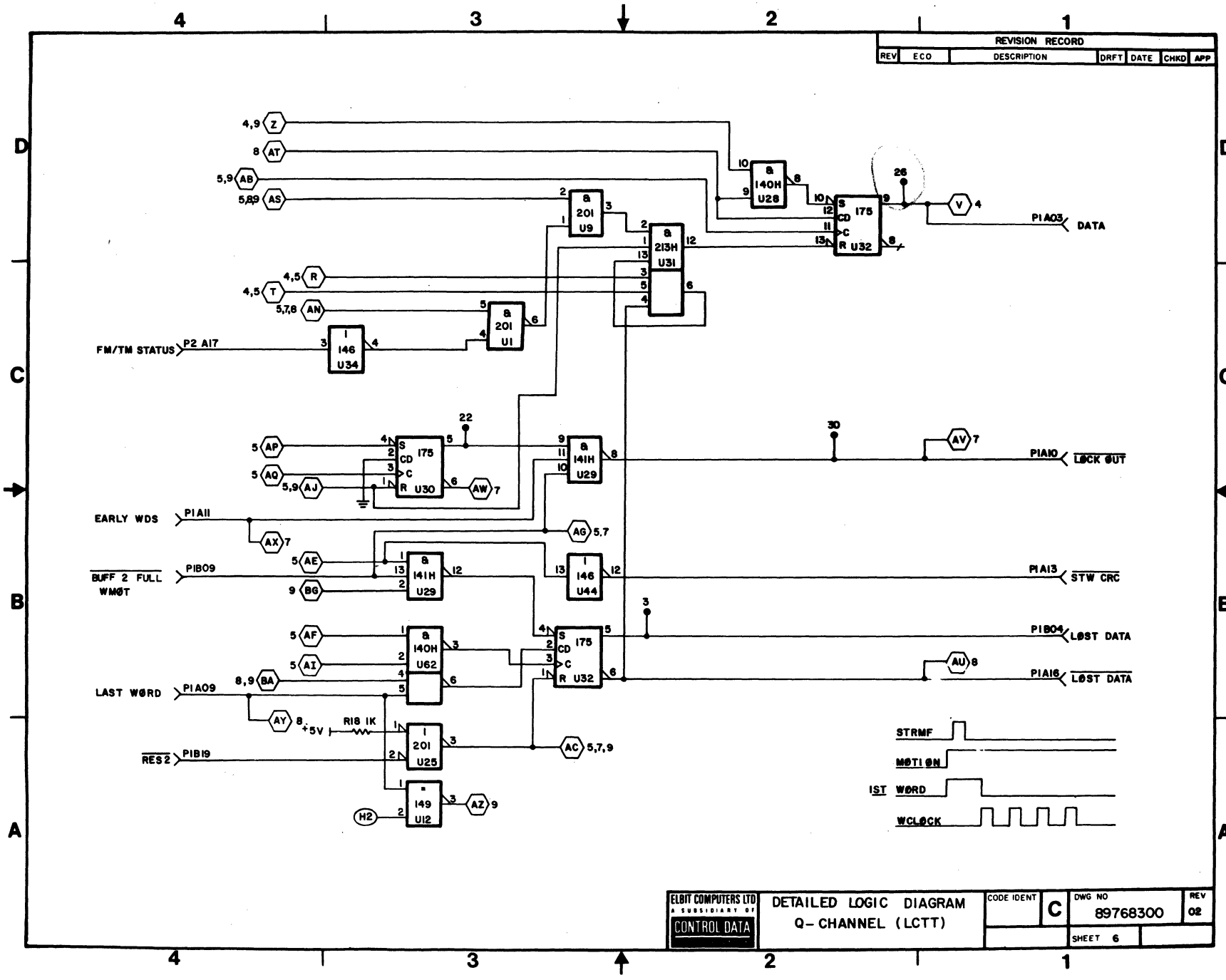


Figure 5-4. Lockout

For details on Write Clock, PWRQ and Early WDS refer to Basic Timing Generation. STRMF sets 1ST Word at U45-3 and 4 (sheet 4), and U30-4. The fall of the first Write Clock resets 1ST Word. If Buf 2 is not full when the first Early WDS occurs a Lockout (U29-8) pulse is generated. If Buf 2 is already full (when writing) no $\overline{\text{Lockout}}$ occurs.



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 03

End-Of-Record Generator Control

There are four End-Of-Record Sequences (EØRS): either Data or FM,with either 9T or 7T,as shown in Figure 5-5.

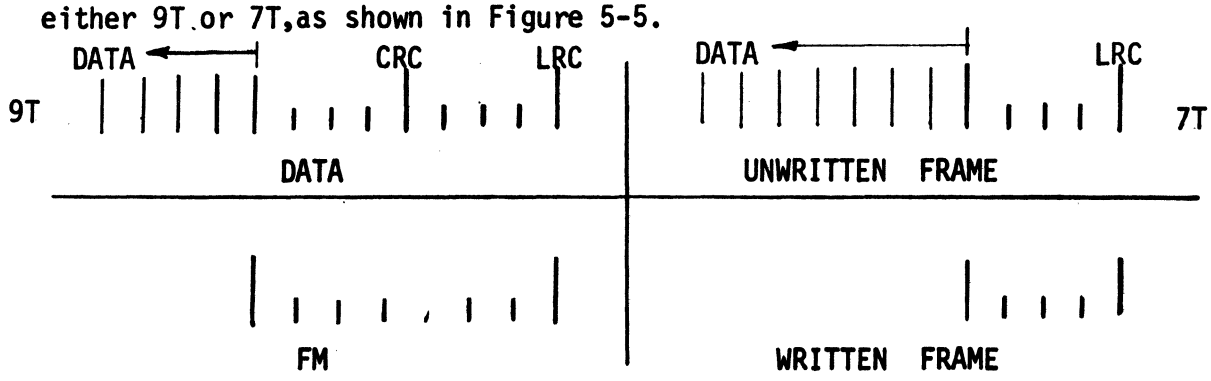


Figure 5-5. EØR Sequences

The first character of the FM is regarded as Data and the second as LRCC. EØRS is set only during Write Motion after the last Data Character is written on tape. This module can be divided into two parts: EØRS FF, and CRCC/LRCC Control Generator.

U11-9 EØRS is set by Early WDS if U11-12 = $\overline{\text{Buf 2 Full}}$•WMØT + $\overline{\text{1ST Word}}$•WFM

(Refer to Figure 5-4)

The W•CRC-LRC Strobe counter is preset while EØRS is low. It is preset either at 1011 for seven track, or at 0111 for nine track. When EØRS is high, WDS-Shifted counts U27 up until the counters overflow. U27-12 locks the counter at U60-10. Refer to Figure 5-6 for the CRCC/LRCC output state.

$\overline{\text{CRCC State}}$ and LRCC State are decoded by:

U42-8: $\overline{\text{CRCC State}} = \overline{Q_A} \cdot Q_B \cdot \overline{Q_C}$

U58-6: LRCC State = $\overline{Q_A} \cdot Q_B \cdot Q_C$

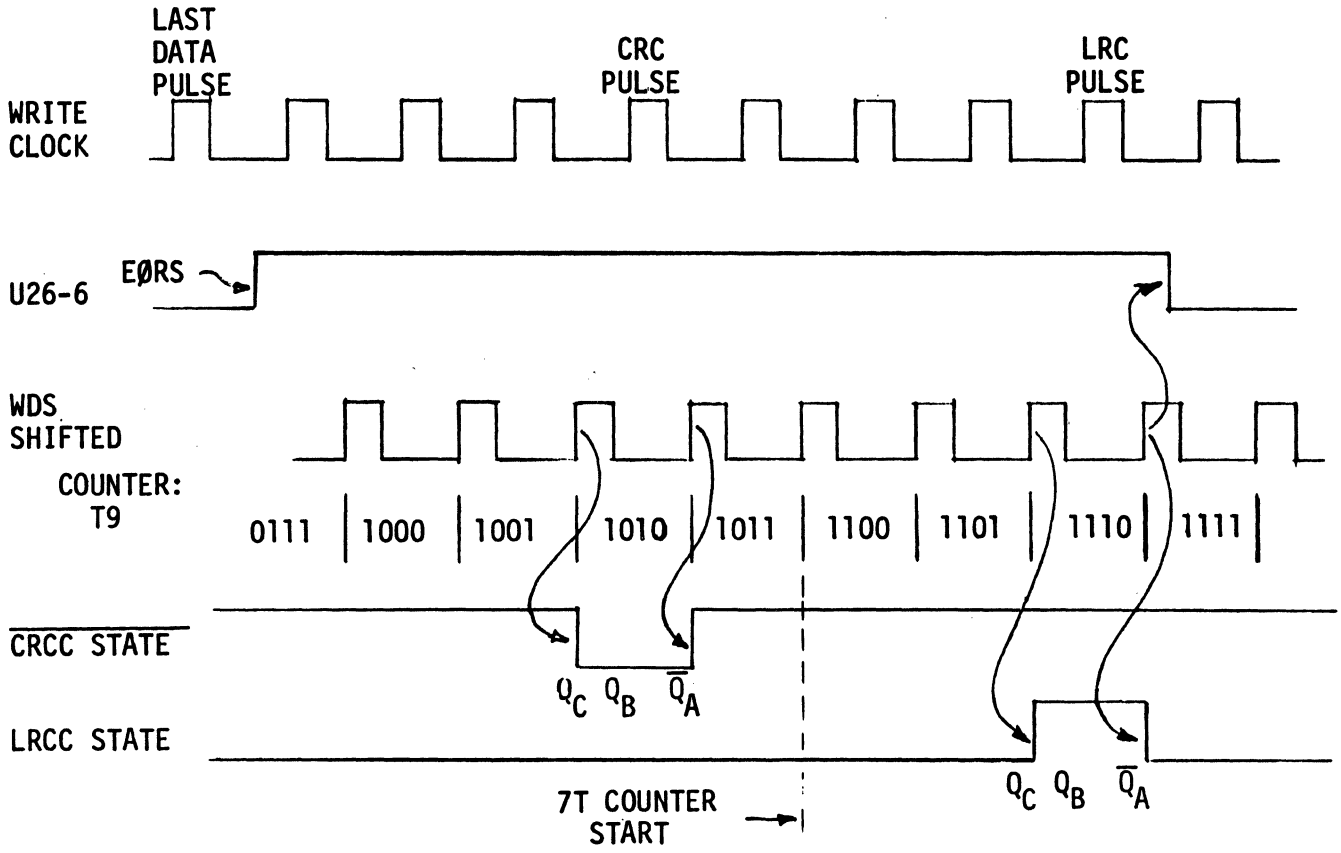


Figure 5-6. CRCC/LRCC State

Stop Distance Circuit

This module consists of two FF's that simulate the TTBusy signal for PEC compatible tape transports. Refer to Figure 5-7.

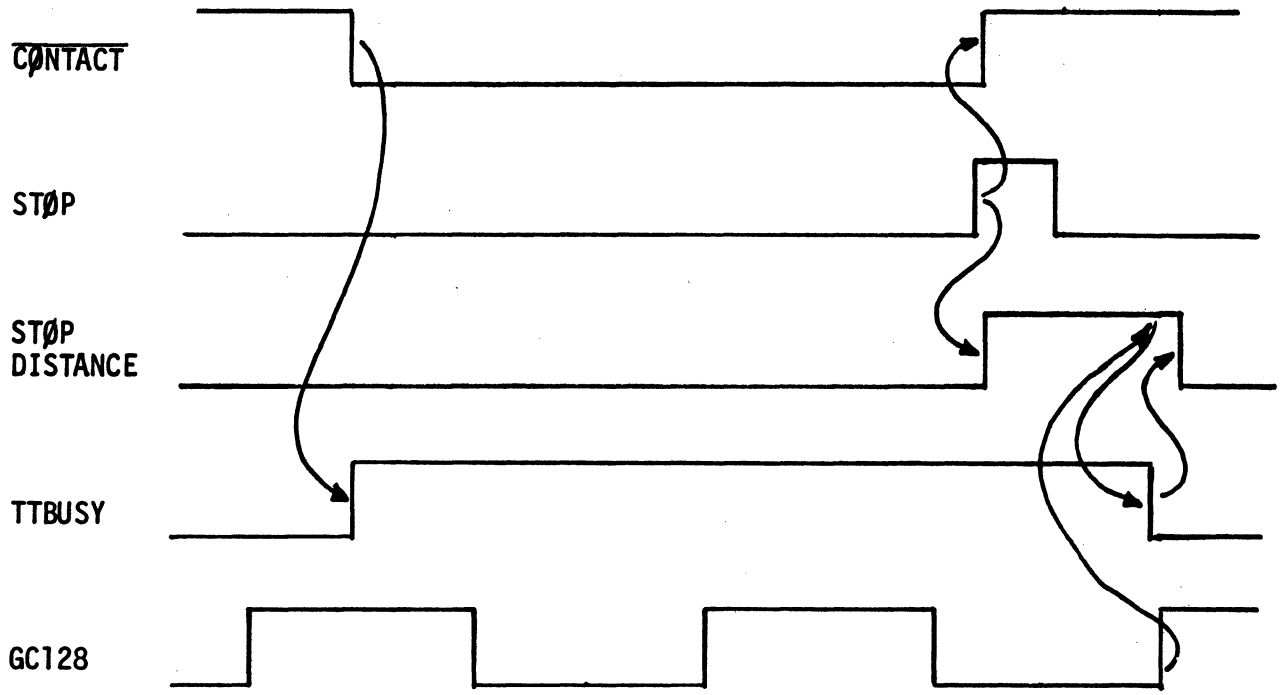
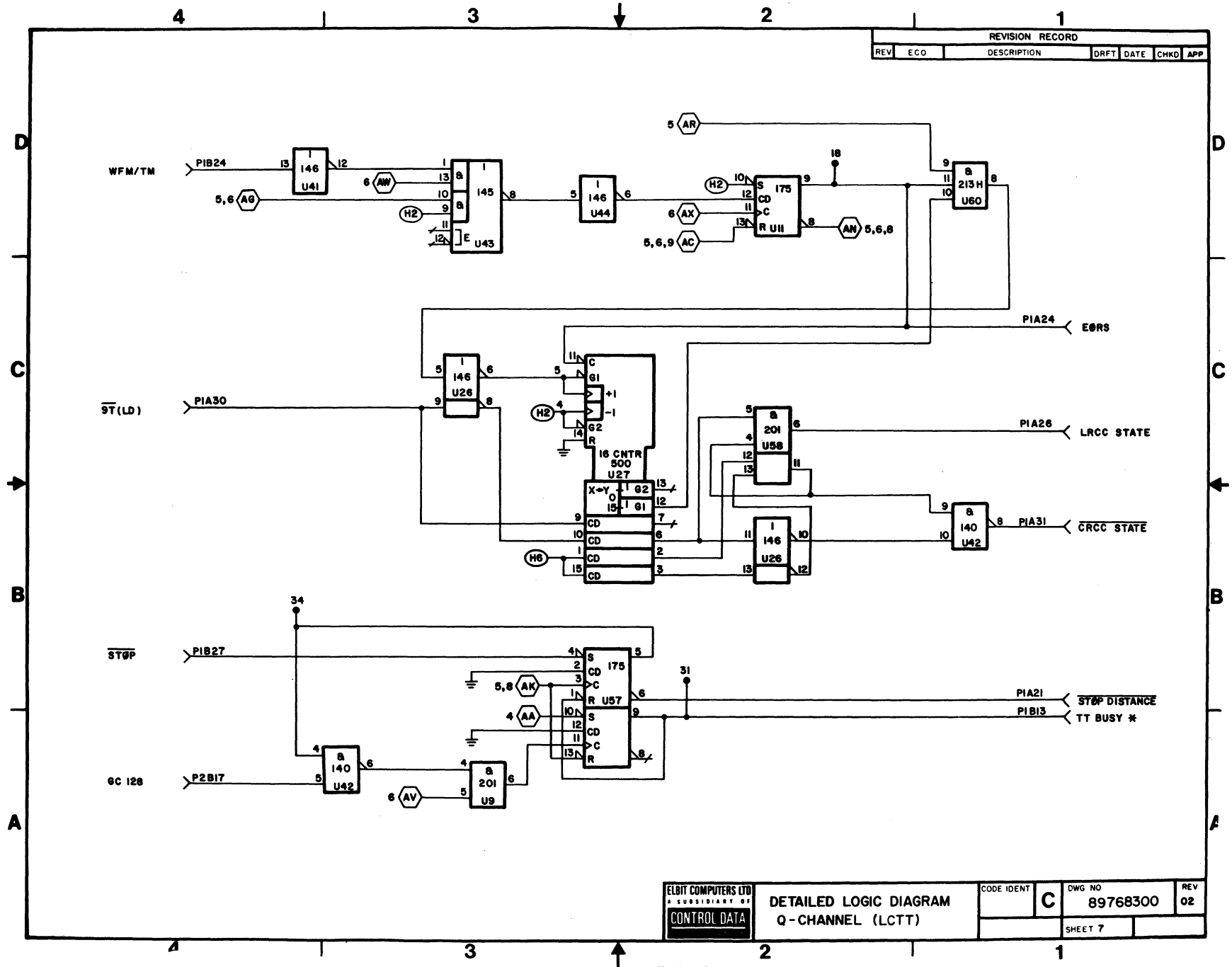


Figure 5-7. Stop Distance



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BUFFERED I/O AND SCANNER (Logic Diagram 89768300 sheet 8)

Buffered I/O

This module stores Buf I/Ø instruction and Protect status and controls fetching of Last Word Address Plus One.

It contains three FF's: Buf I/Ø (U5-9), Protect (6-5) and FCW (U5-6). Buf I/Ø and FCW are set by $\overline{\text{STRBUF}}$ which also strobes A/Q Protect into Protect. All three FF's are reset by $\overline{\text{RESI}}$.

Buf I/Ø indicates that a DSA transfer is in operation and it is cleared be the rising of:

U41-2 = EØRS + Lost Data+EØP+Last Word (EØP+$\overline{\text{Busy}}$)

$\overline{\text{DSA Protect}}$ = $\overline{\text{DSA WREN}\cdot\text{Protect}}$ enables the DSA channel to Write into Protected Storage.

$\overline{\text{LDLWA}}$ falls with the setting of FCW and rises with the first INCCA. $\overline{\text{LDLWA}}$ strobes the Last Word Address Plus One into the LWA latch, it does not change again during the DSA transfer.

Scanner

The Scanner transfers the scanning signal of the whole system through the controller according to the position of the controller in the system as shown in Figure 5-8.

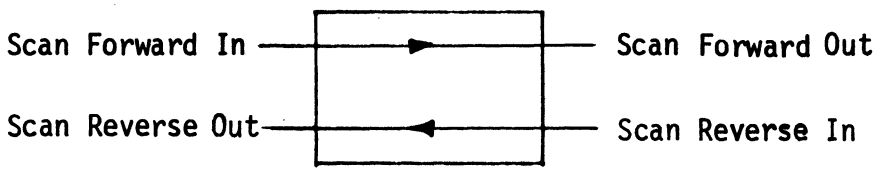


Figure 5-8. Scan Control

Middle: U56-5 = 1. The scanning signal passes Scan For In through U18-15, U1-3, U35-3, U19-6, U17-1, U20-6, U34-6 and Scan For Out. The backward signal passes Scan Rev Out, U17-15, Scan Rev In.

If the Need signal rises during the first time U19-5(which is in the forward scanning path) rises, Halt is set. $\overline{\text{Halt}}$ blocks the Scanner at U35-2 and the second arrival of the high going Scan In sets Request. The Scanner, therefore, is allowed to complete a full loop after Halt is set. See I/O Reference Manual.

The other connection possibilities are:

Last: The scanning path is: Scan For In, U18-15, U1-3, U35-3, U19-6, U17-15, Scan Rev In.

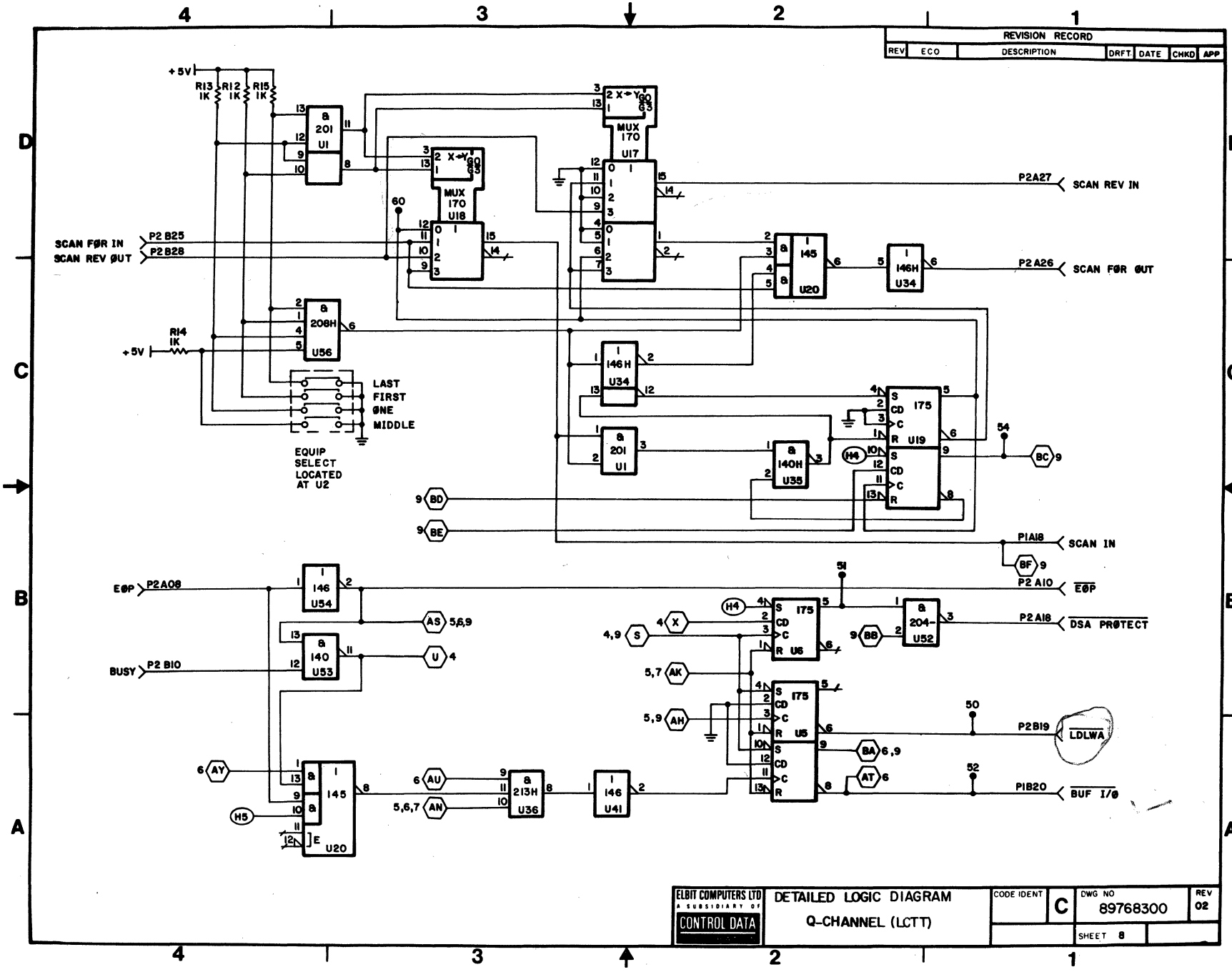
First: The scanning path is: Scan For Out, U18-15, U1-3, U35-3, U19-5, U17-1, U20-6, U34-6 and Scan For Out.

One: The Scanner is in a closed loop and the oscillation period is due to the internal delay of the gates U18-15, U1-3, U35-3 and U19-5.

When no one of the four above is selected, the Scanner is Out and does not scan. To allow the system to work, the controller should be extracted and two jumpers plugged into the back panel.

Jumper 1 (P2B25 and P2A26) should connect Scan For In with Scan For Out.

Jumper 2 (P2A27 and P2B28) should connect Scan Rev In with Scan Rev Out.



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REQUEST/RESUME LOGIC (Logic Diagram 89678300 , sheet 9)

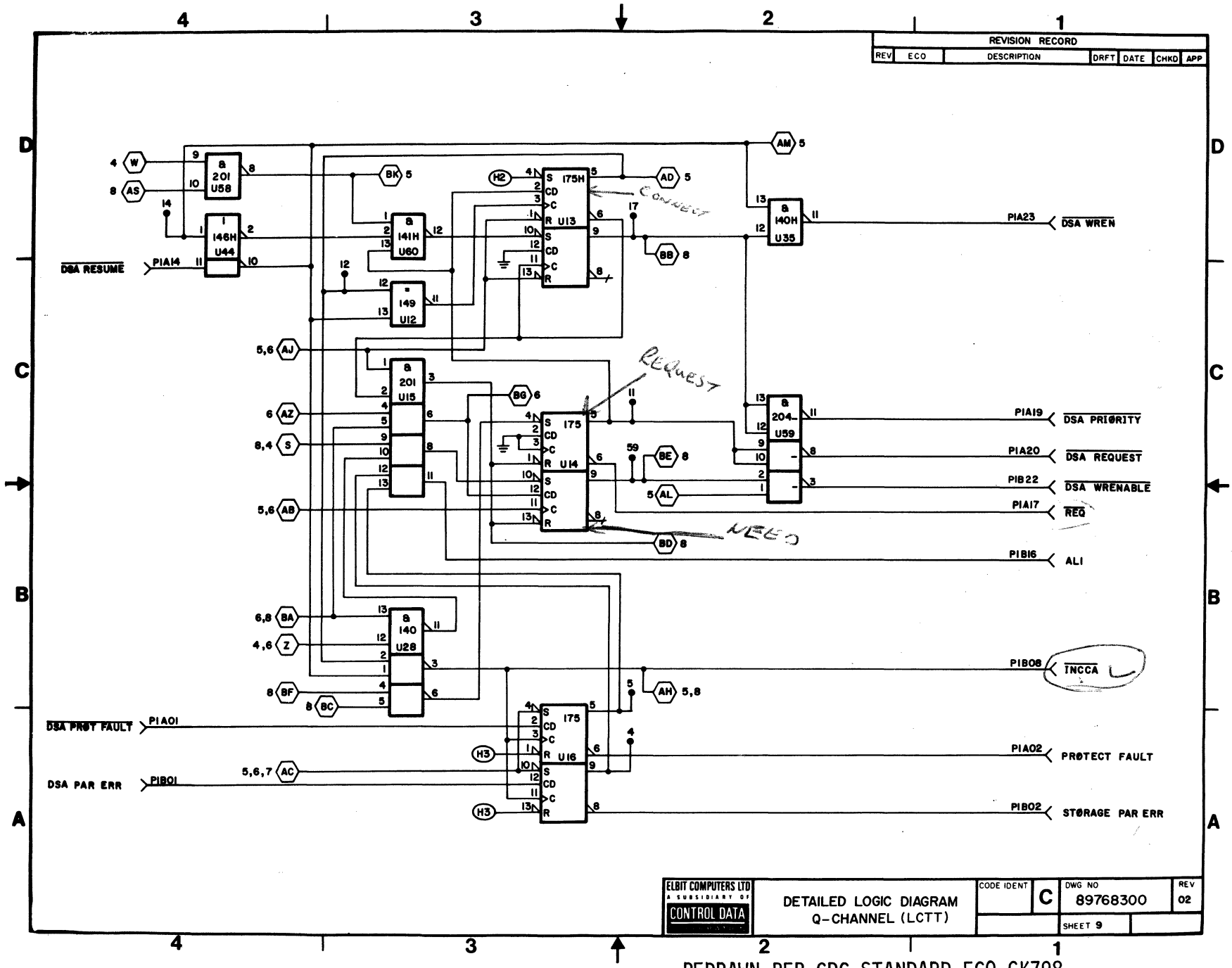
This module consists of four transfer FF's and two status FF's: the Need (U14-9), Request (U14-5), Connect U13-5), DSAWREN (U13-9, PARERR (U16-9) and Protect Fault (16-5) FF's.

The Need FF is set when a data word is to be transferred to or from the DSA channel. Need is set by:

1. $\overline{\text{STRBUF}}$ to transfer the LWA+1.
2. $\overline{\text{STRWMØT}}$•Buf I/O to initiate data transfer (U15-8) during Write Motion (U28-11).
3. Rising of $\overline{\text{Trans}}$ if Buf I/Ø $\overline{\text{Lost Data}}$ is high, for transferring data words. Need is reset by RES1+Connect. If Need is set, the controller blocks the Scanner by raising a Halt and waits for Scan In. Request is set by Halt•Scan In. Request sends the computer a $\overline{\text{DSA Request}}$ and sets Connect.

The computer responds by a $\overline{\text{Resume}}$ pulse, at the end of which the word is strobed in or out of the computer. The leading edge of $\overline{\text{Resume}}$ sets Connect (U12-11) which resets Request and Need. If the computer is in RMØT the rising of Req sets DSA WREN on condition that $\overline{\text{Resume}}$ is not active. The trailing edge of $\overline{\text{Resume}}$ resets Connect which strobes the data into or out of the Double Buffer and resets the DSA WREN signal. A new Need can now be generated.

The PARERR and Protect Fault are set if that signal arrives from the computer and Connect is high. These status bits are then sent back to the computer.



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LOWER DATA SECTION (Logic Diagram 89647900)

BASIC TIMING GENERATOR (Logic Diagram 89647900, sheet 1)

All the timing signals are generated from T1 and T3, having a frequency of 640 kHz, a width of 1/4 cycle, and a delay between them of 1/2 cycle.

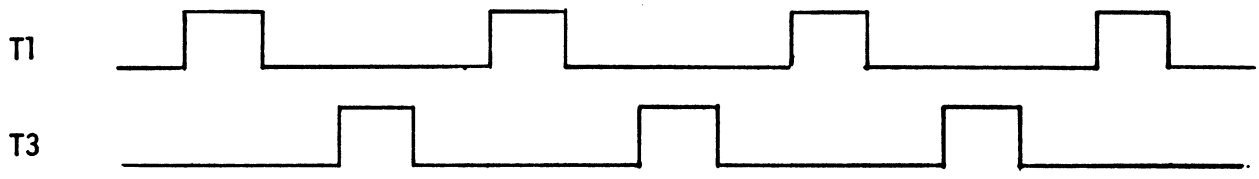


Figure 5-9. T1 - T3 Output

T1 is divided by 2 (U37-5) and by 32 (U50). The outputs are selected by U51 according to the 50 IPS (speed) jumper.

TABLE 5-2. TIMING GENERATOR* OUTPUTS

Speed	U51-9	U51-12	U51-4	U51-7
25 ips	320	160	80	20
50 ips	640	320	160	40

The waveforms are symmetric and changes on the leading edge of T1.

U51-4 is divided by two (U35-5) to generate PECHARCLK at 80/40 kHz, which is symmetric, changing with T1.

U35-9 is strobed by T3 to generate PEClock at 320/160 kHz which is symmetric, changing with T3.

U20 and U4-6 divide U51-4 by ten in order to generate Gaplock at 16/8 kHz with a 70% duty cycle, rising with T1 and falling with T3.

---

* Frequency in kHz.

U51-9 output is divided by 23 in U22-5, U21 and U4-8 to generate (at U21-7) 27.82/13.91 kHz, with a 7/23 duty cycle, rising with T1 and falling with T3.
U5-6 selects the signals from U51-7 and U21-7 according to the Table 5-3 and Figure 5-10.

TABLE 5-3. WRITE CLOCK FREQUENCY* (FWC) AT U5-6

Speed (inches per second)	800 BPI	$\overline{800\ BPI}$
25	20	13.91
50	40	27.82

U6 and U5-8 and U7-6 differentiate the signal from U5-6 to generate 2 FWC (twice the FWC frequency as shown in Table 5-3) with a pulse width of 1.04 µsec, changing with T1, as shown in Figure 5-10.

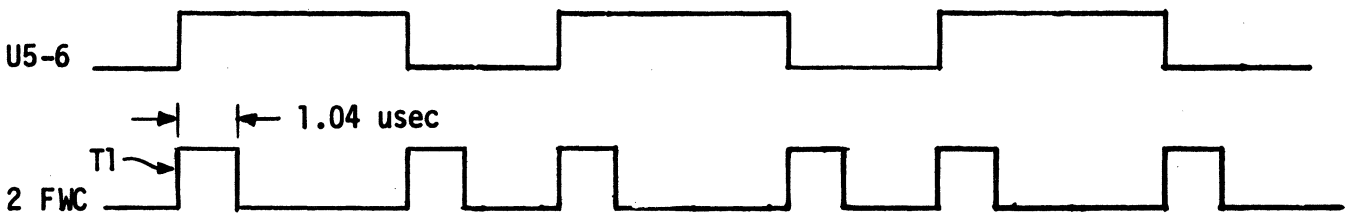


Figure 5-10. 2 FWC Generation

U22-9 enables Early WDS, Write Clock and WDS Shifted with frequencies as in Table 5-3. It is set if PEStart·WRequest is high at the rise of T1. If U22-9 is high, U10-8 and U24 form the pulses shown in Figure 5-11.

* Frequency in kHz

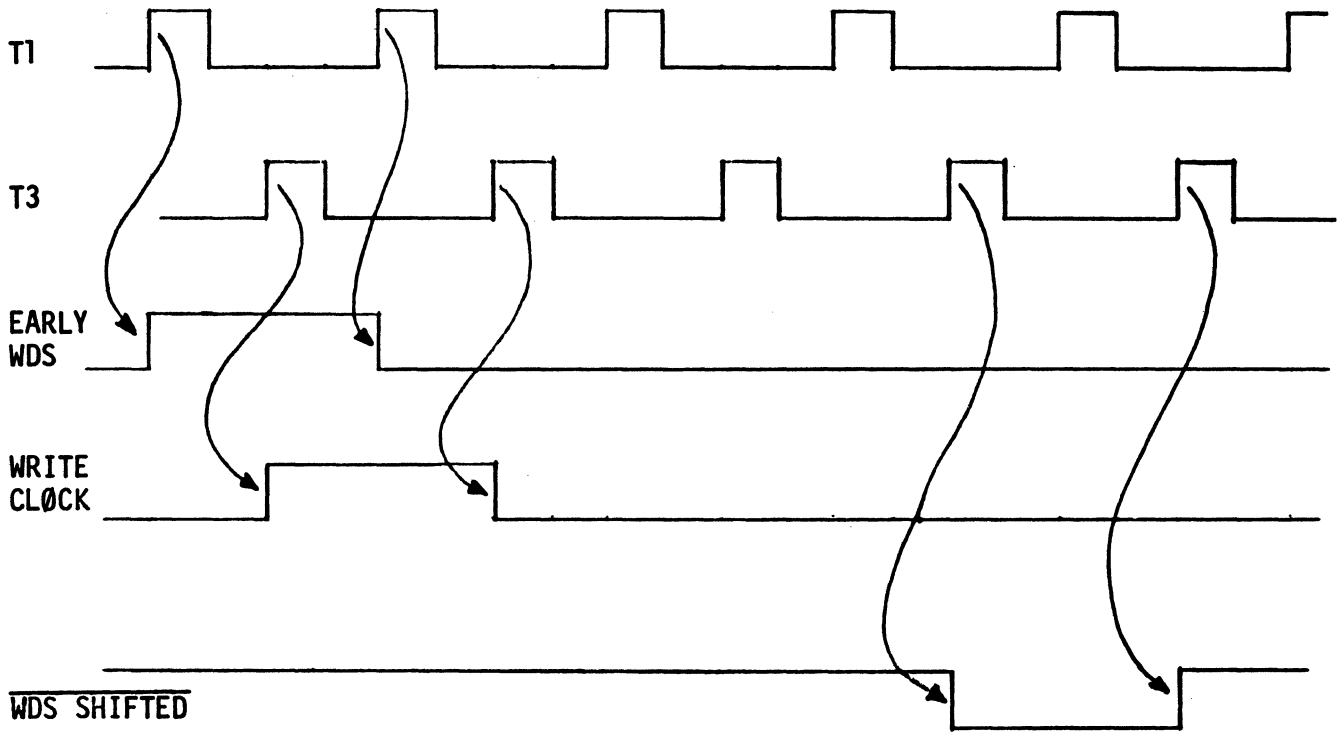


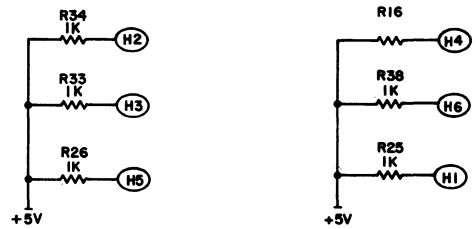
Figure 5-11. Early WDS, Write Clock and WDS Shifter Generation

ØFF-SHEET REFERENCE

ØFF-SHEET REFERENCE LETTER	SIGNALS	SHEET LØCATIØN							
		2	3	4	5	6	7	8	9
A	75IPS	B-4		B-1					
B		D-4	C-1						C-2
C	PE1600	B-4	C-1						
D			A-4			D-2	B-4		C-1
E			C-4		A-4	D-2	B-4		C-3
F	$\overline{9T}$		C-1	C-2					D-4
G	RETRANSPØRT		C-2	A-1					B-4
K	9T		C-4	C-1					
L	1600 BPI		C-1						C-4
M	$\overline{RES1}$		A-1			B-4		B-3	
N	$\overline{RES2}$		A-2		C-3				
P	A0		D-4			D-2	C-4		C-1
Q	A4		C-4		B-4	C-4	C-4		B-1
R	A5		C-4			D-4	C-4		B-1
S	A6		C-4			D-4	C-4		A-2
T	A2		D-4		B-4	D-2	B-4		C-3
W	$\overline{DUAL}$		B-4	D-1					
X	DUAL		B-4	D-1					
Y	RES INT		A-1		A-4				
Z	PE		B-4	B-1					
AA	556BPI		D-1						C-2
AB	PRØTECTED			B-1					B-4
AC	ALARM			B-2					B-2
AD	INT			B-2					C-4
AE	EØP (UP)			A-4					B-2
AF	DATA (Q)			C-4					D-4
AG				D-2					C-2
AK	DATA IN 0					A-2	C-2	D-3	
AL	DATA IN 1					A-2	C-2	C-3	
AM	DATA IN 2					A-2	C-2	C-3	
AN	DATA IN 3					A-2	C-2	C-3	
AO	DATA IN 4					A-4	D-2	B-3	
AP	DATA IN 5					A-4	C-2	B-3	
AQ	DATA IN 6					A-4	C-2	B-3	
AR	DATA IN 7					A-4	C-2	B-3	
AS	WRTAPE 0						B-4	D-1	C-2
AT	WRTAPE 1						B-4	C-1	C-2
AU	WRTAPE 2						B-4	C-1	C-4
AV	WRTAPE 3						B-4	C-1	C-4
AW	WRTAPE 4						D-4	C-1	B-2
AX	WRTAPE 5						C-4	B-1	B-2
AY	WRTAPE 6						D-4	B-1	A-4
AZ	WRTAPE 7						C-4	B-1	A-4
BA	CURAD 0					D-1	A-2		C-2
BB	CURAD 1					D-1	A-2		D-2
BC	CURAD 2					D-1	A-2		C-4
BD	CURAD 3					D-1	A-2		D-4

SHEET REVISION STATUS									REVISION RECORD						
1	2	3	4	5	6	7	8	9	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	01	01	01	01	01	01	01	01	01	CK690	RELEASED TO CLASS B	[illegible]	[illegible]	[illegible]	[illegible]
02	01	01	01	01	01	01	01	01	02	CK770	ADD DETACHED LIST	[illegible]	Sep, 76	[illegible]	[illegible]

		2	3	4	5	6	7	8	9
BE	CURAD 4					D-3	B-2		B-2
BF	CURAD 5					D-3	A-2		B-2
BG	CURAD 6					D-3	B-2		A-4
BH	CURAD 7					D-3	A-2		B-4
BI	A7					D-4	C-4		A-2



AW 89767900
AY 89767800
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA
FIRST USED ON FA446-A

DWN	Nomi Pakosky	23/6/76
CHKD	[illegible]	25 9 76
ENGR	S. [illegible]	25.9.76
MFG		
APPR		

TITLE
DETAILED LOGIC DIAGRAM
LOWER DATA (LCTT)

CODE IDENT: C
DRAWING NO: 89768000
SCALE:
SHEET 1 OF 9

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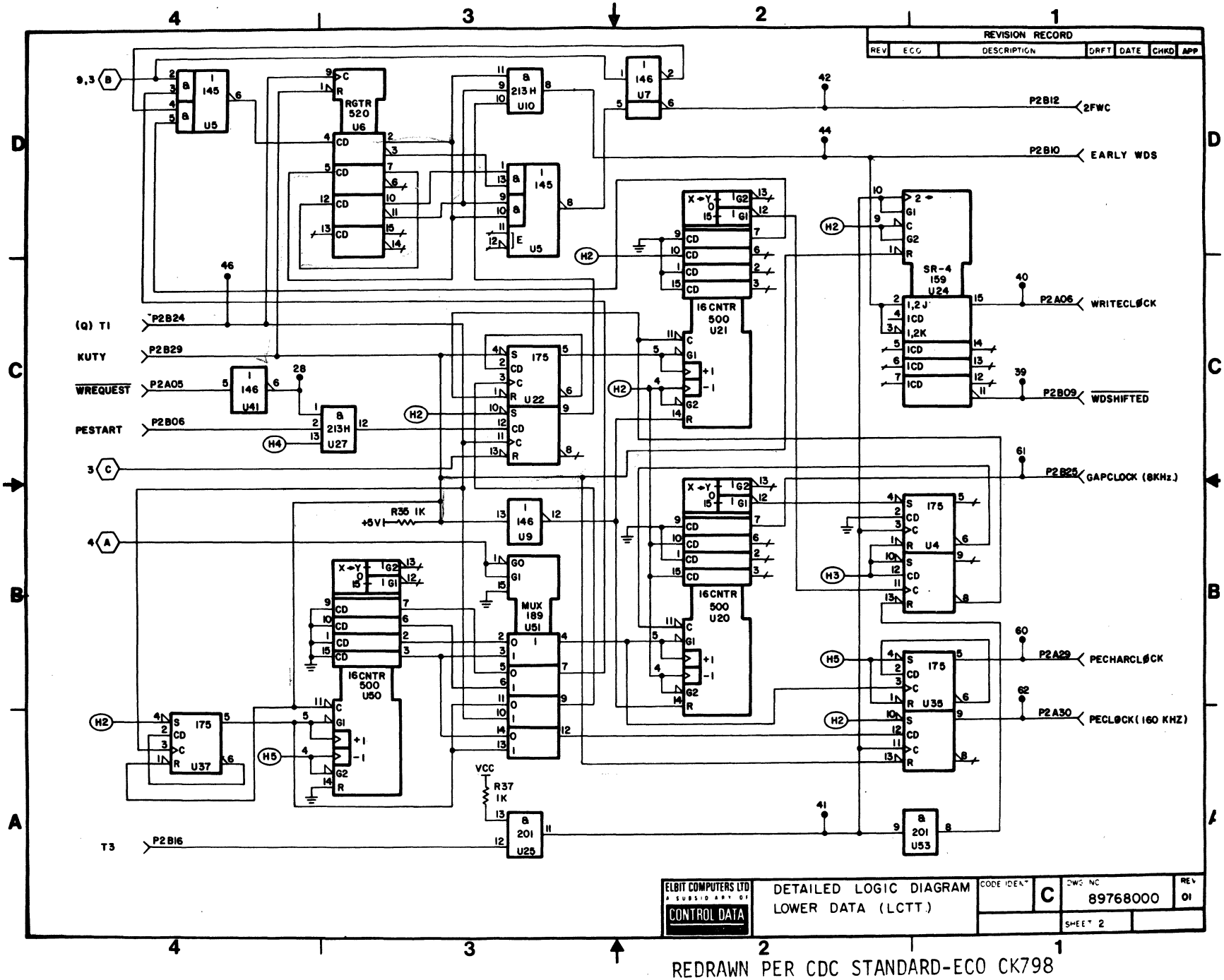

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OPERATION CONDITIONS (Logic Diagram 89647900, sheets 2 and 3)

The operation conditions include all the conditions that define the connection of the controller and the MTT after execution of a unit select operation. The conditions are generated by manually set switches and FF's set by US operation.

This module checks to determine if the unit select instruction is legal, and if so, it signals this to the Reply/Reject logic, and stores the Unit Select information. This module also generates the $\overline{MC}$ and $\overline{REST}$ signals.

Three FF's ModeSEL, $\overline{A/D}$, BCD store the density, format and code of the selected unit.

ModeSEL (U39-5) is high if 1600 bpi density is selected. ModeSEL can be set only if a nine track dual mode transport is selected. ModeSEL is strobed by STRUS according to 9T·A3+9T·A4 (U43-9). It is reset by $\overline{MC}$.

$\overline{A/D}$ (U23-11) is high if Character Format is selected. This FF is strobed by STRUS according to A0 and A6: If A0·A6 is low, $\overline{A/D}$ does not change. If A0 is high $\overline{A/D}$ is set if A6 is high setting $\overline{A/D}$ (Both cannot be set). MC sets $\overline{A/D}$ Format.

BCD (U39-9) is high if the BCD Code is selected. BCD is set by STRUS according to A1. If A1 is high then BCD is set. For every other STRUS, BCD is reset. MC sets the Binary Code.

The signal LEGUS (U27-8) is a combinational function of A0-A6, $\overline{TTDS}$. The Density Status from the tape, BØT, 9T, ILLUSCode (the check for legal unit select from another module), $\overline{PC\text{-}1600}$(which indicates that the phase encoding formatter is inserted in the chassis) Contact, $\overline{Dual}$ and PE, is as follows:

(U43-7) $Z_A = A5 \cdot 9T + A3 \cdot \overline{9T}$

(U43-9) $Z_B = A3 \cdot 9T + A4 \cdot \overline{9T}$

(U43-12) $Z_C = A4 \cdot 9T + A5 \cdot \overline{9T}$

(U43-4) $Z_D = A1 \cdot 9T$

(U42-8) $Z_E = \overline{Z_A \cdot Z_B + A0 \cdot A6 + A1 \cdot A2 + ILLUSCode}$

(U10-12) $Z_F = \overline{Z_C + Z_D + Z_E}$

$DS = TTDS \cdot \overline{9T \cdot Dual} + PE \cdot 9T \cdot Dual$

(U26-8) $Z_G = Dual \cdot 9T + \overline{\overline{DS} \cdot Z_A + DS \cdot Z_B}$

$LEGUS = Z_G \cdot Z_F \cdot \overline{Contact} \cdot (PC1600 \div \overline{A5})$

If LEGUS is high, then the Unit Select instruction will reply as:

(U25-3) 800 BPI = $\overline{\overline{9T} \cdot \overline{DS} + 9T \cdot DS}$

(U7-12) 1600 BPI= $9T \cdot DS$

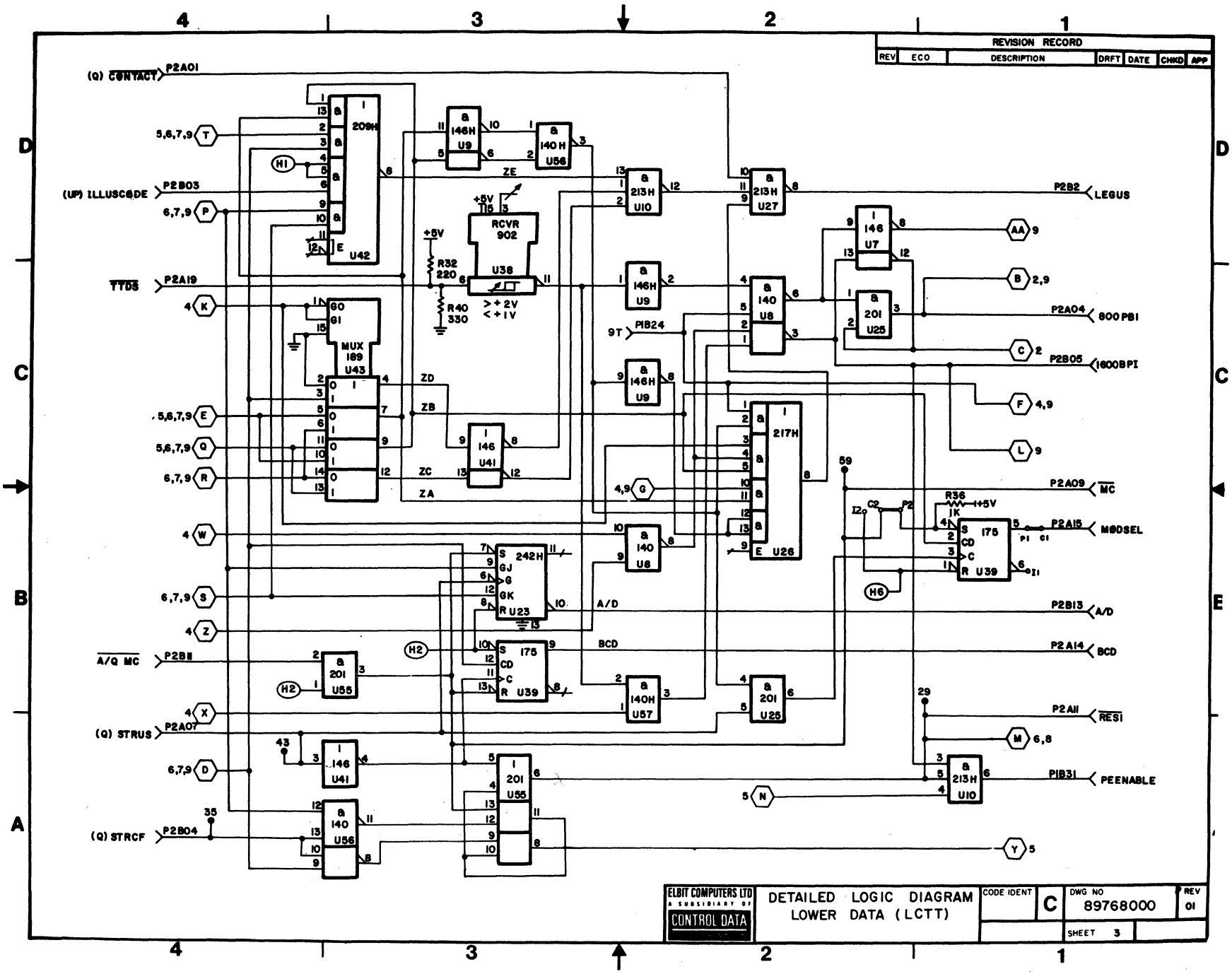
(U7-8) 556 BPI = $\overline{9T} \cdot \overline{DS}$

PEEnable enables the phase encoding formatter and also resets it when low (U10-6). PEEnable = $\overline{RES1} \cdot 1600$

PETransport is a Status signal that indicates that the transport has 1600 bpi capability and the phase encoding formatter is connected (U27-6). PETransport = $PC1600 \cdot 9T \cdot (Dual + PE)$.

RES1 clears most of the FF's in the controller. It is a combination of Strobe Unit Select, MC and Clear Controller (STRCF·A1), so:

(U55-6) RES1 = STRUS+MC+STRCF·A1.



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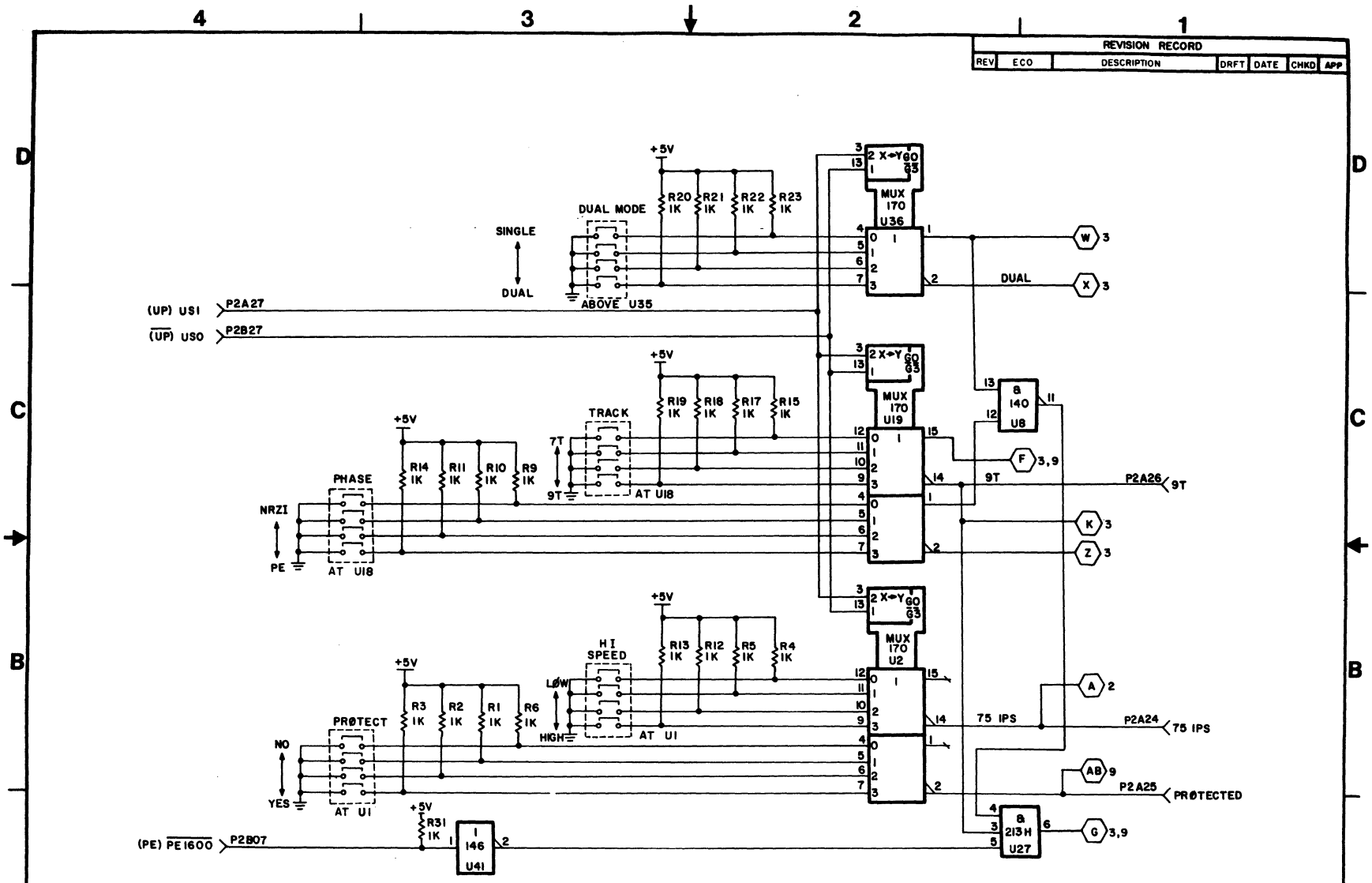

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INTERRUPTS (Logic Diagram 89647900, sheet 4)

Interrupt Circuit

One Interrupt signal is sent to the computer, for at least one Data, EØP or Alarm Interrupt (if enabled). This module includes three Interrupt Enable FF's: DataINT Enable (U23-15), EØPINT Enable (U40-11), AlarmINT Enable (U40-15) and one rising edge detection FF - EØP (U3-9).

The three Enable FF's are reset by U55-8 (RESINT = MC+STRCF(A0+A1). These flip flops are set by STRINT according to A2, A3 and A4, respectively. If A2 is high when strobed, then DataINT Enable is set. If A2 is low when strobed, then DataINT Enable does not change.

EØPINT is set when EØPINT Enable is high and EØP rises.

Interrupt = DATA·DataINT Enable + EØPINT+Alarm·AlarmINT Enable

Alarm Circuit

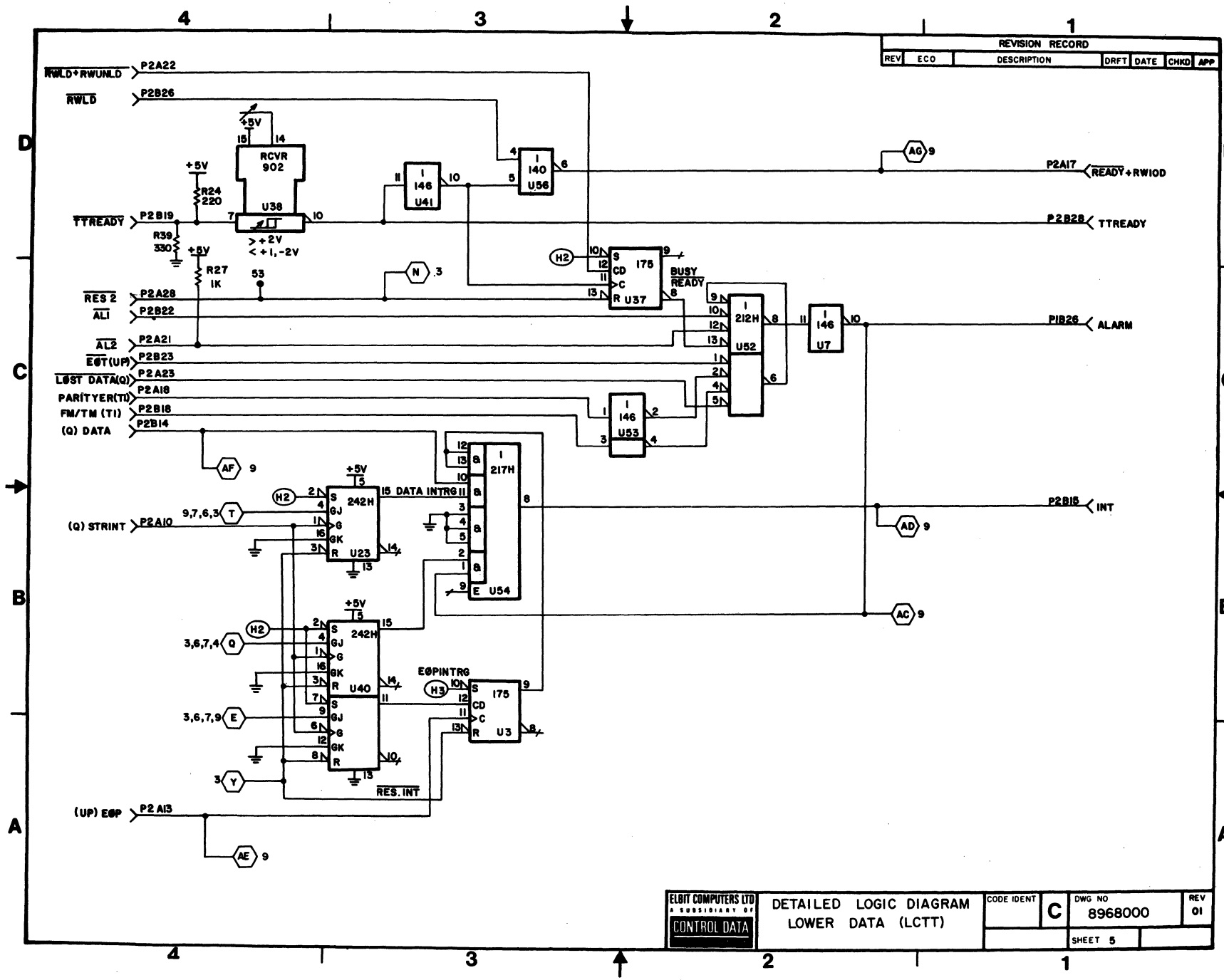
This module includes the Busy·$\overline{\text{Ready}}$ FF's and the combinational circuit that detects Alarm.

(U37-9) Busy·$\overline{\text{Ready}}$ is set by the rise of $\overline{\text{TTReady}}$ if RWLD+RWUNLD is low.

(U8-11) Ready·$\overline{\text{RWLD}}$ = Ready+RWLD (used as the Ready signal in the MTTC)

Alarm = Busy·$\overline{\text{Ready}}$ + EØT+Parity ERR+Lost Data+FM/TM+AL1+AL2

$\overline{\text{AL1}}$ and $\overline{\text{AL2}}$ are auxiliary Alarm conditions from the PEFormatter.



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LOWER DSA DATA PATH (Logic Diagram 89647900, sheets 5 and 6)

$\overline{\text{STRBUF}}$ initiates DSA transfer and presets CURADDR (0-7) to the contents of A(0-7). The A/Q DSA Selector is set by BUFF I/Ø to DSA Selector and the first transfer generates $\overline{\text{LDLWA}}$, that strobes the contents of DSA Data (0-7) into LWA+1.

Every Transfer Request enables the current address on the DSA ADDR lines and the falling of INCCA increments the Current Address. When Writing the data is transferred through DSA Data (0-7), A/Q DSA Selector to the Double Buffer and then to the tape. See Figure 5-12.

When Reading from the computer the data is transferred from the tape, the Double Buffer and DSA WREN enables the data to pass to the computer memory.

A = B is the Comparator signal to the second half of the comparator. CARCURAD is the counter overflow to the second half in the Upper Data card.

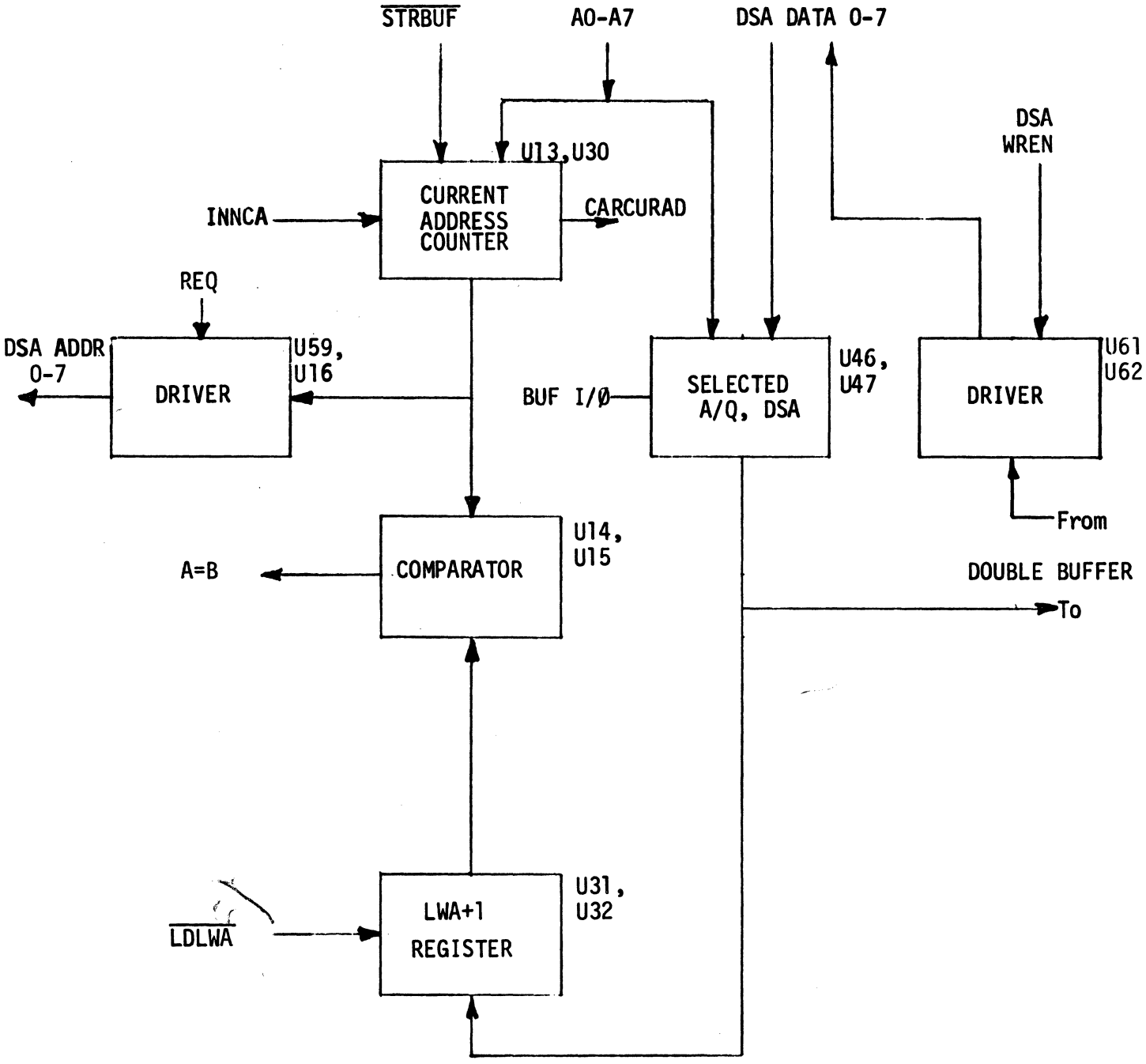
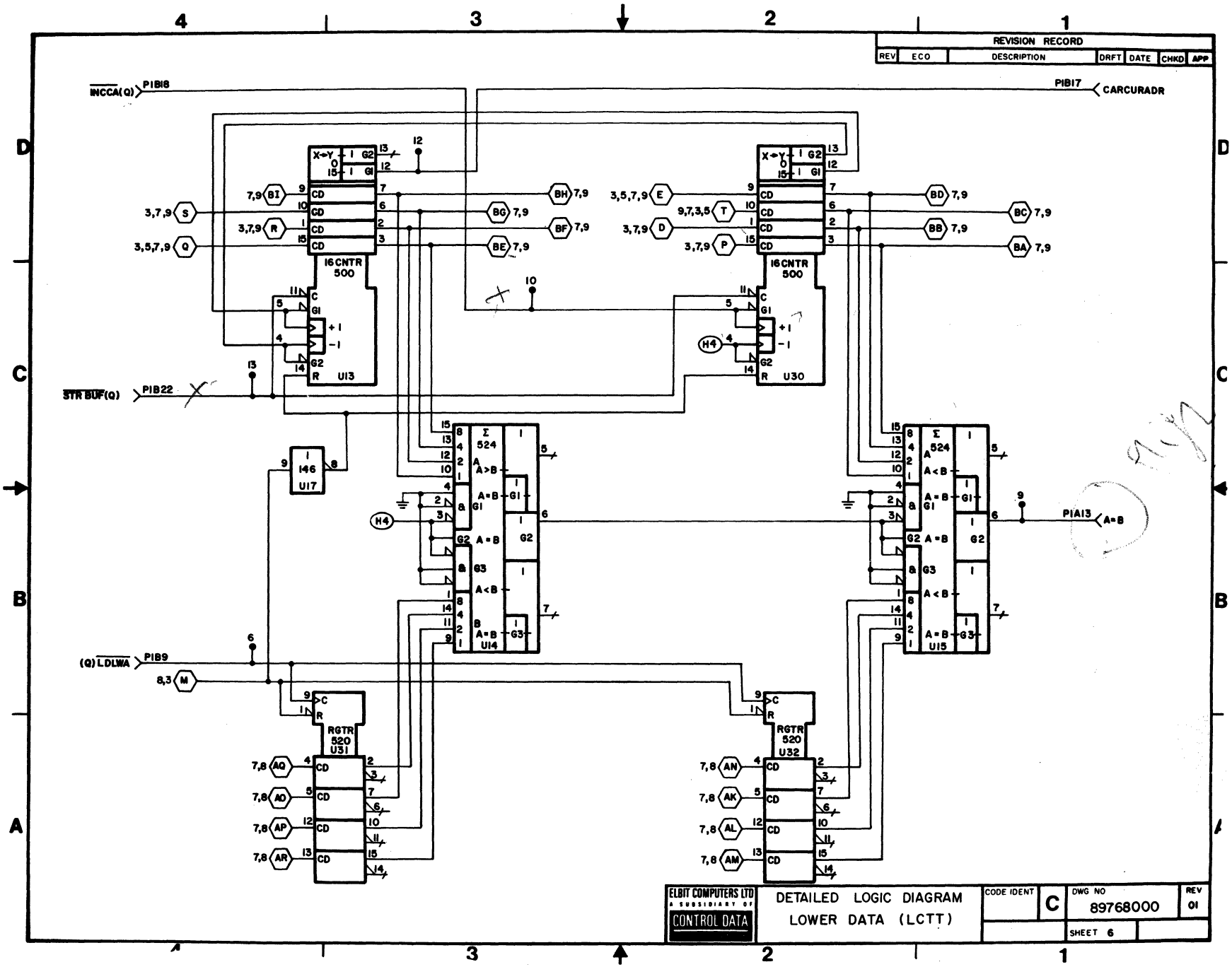


Figure 5-12. Lower DSA Data Path



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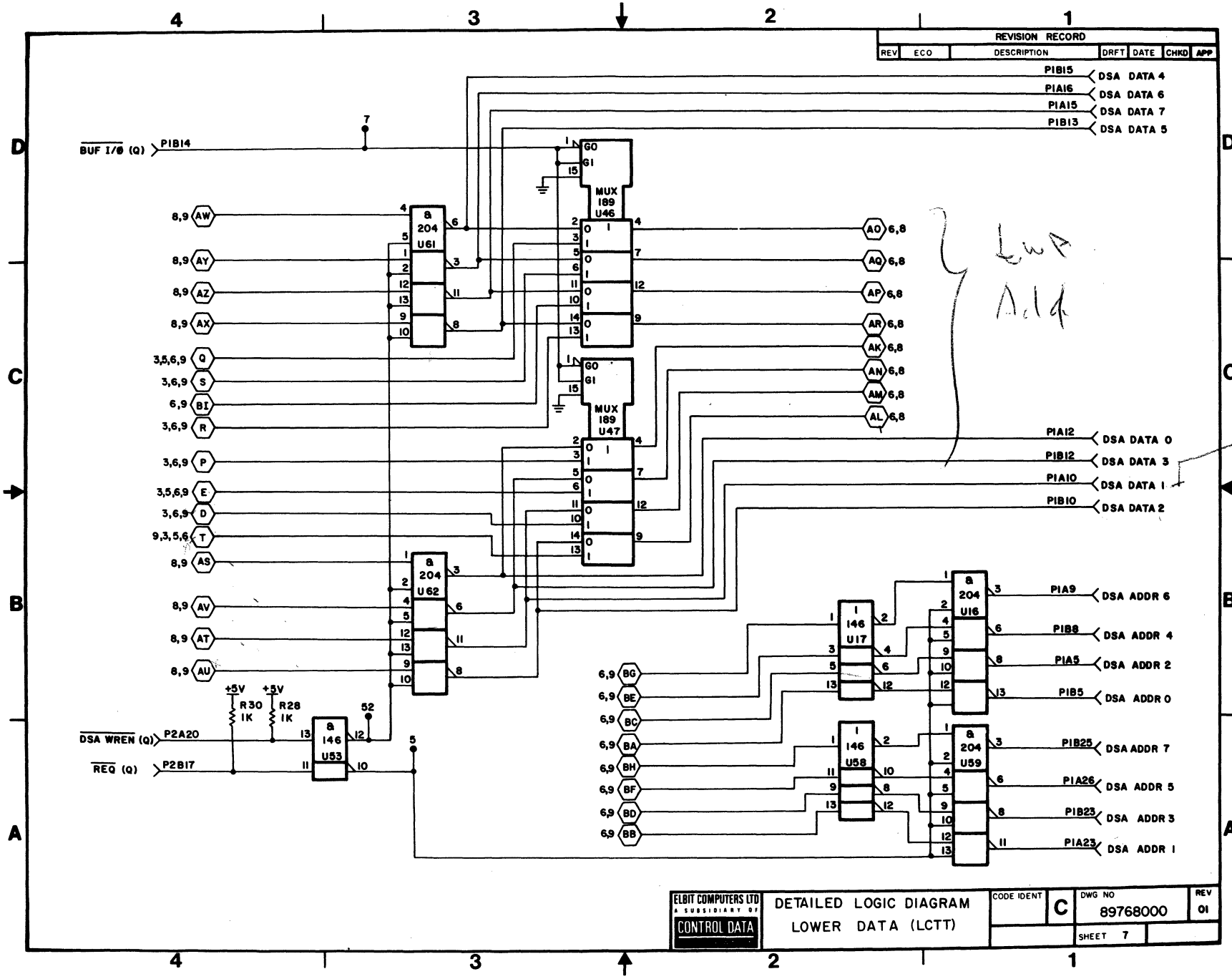


REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

LOWER A DATA PATH (Logic Diagram 89647900, sheets 7 and 8)

For the block diagram of the Lower A Data Path, refer to Figure 5-12.

RDTAPE 0-7 signals from the tape transport are passed through a multiplexer U64 (RDTAPE 0-3) and U63 (RDTAPE 4-7) when $\overline{\text{RMOT}}$ is low. With $\overline{\text{RMOT}}$ high, DATAIN 0-7 signals from the computer are admitted. The output of the multiplexer (Selector 1) is then supplied to Buffer 1 (U49,U34) which is controlled by the signal $\overline{\text{LOWX1}}$ through U49-9 and U34-9. Buffer 1 is cleared by $\overline{\text{CLEARLOWER}} + \overline{\text{RES1}}$ through U25-8 to U34-1 and U49-1. Buffer 2 (U48, U33) further passes the signal to produce WRTAPE 0-7 signals for the tape transport, when the TRANS signal is low (U48-9, U33-9) and $\overline{\text{RMOT}}$ is high at U64-1 and U63-1. Buffer 2 is cleared by $\overline{\text{RES1}}$. With $\overline{\text{RMOT}}$ low, the RDTAPE 0-7 data is available for transfer to Selector 2 (multiplexers U44, U28, U11 and U12), but will only be accepted when the sum of SELA0 and SELA1 represents a binary 3. If SELA0 and SELA1 are both low (binary 0), only STATUS signals are passed on through Selector 2. When SELA0 is high and SELA1 is low (binary 1), STATUS 1 is selected, and if SELA0 is low with SELA1 high (binary 2), STATUS 2 is selected. These signals are NANDed through U60, U29, when enabled by $\overline{\text{ENA}}$ (high) to the A-bus to the computer.

When signals are received from the computer A-bus, they are admitted through U45, U58 to the other Lower Data Section circuitry.

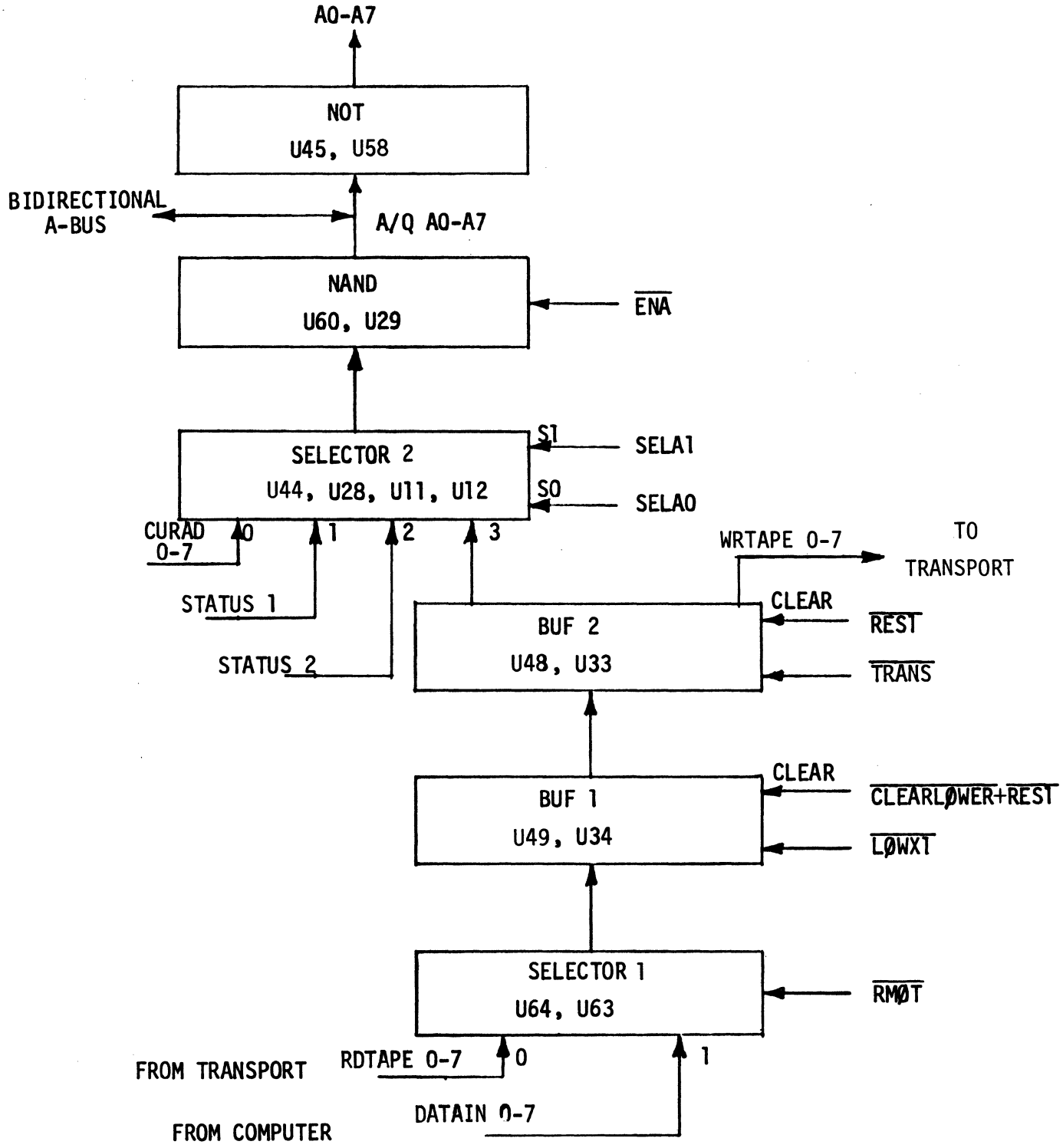
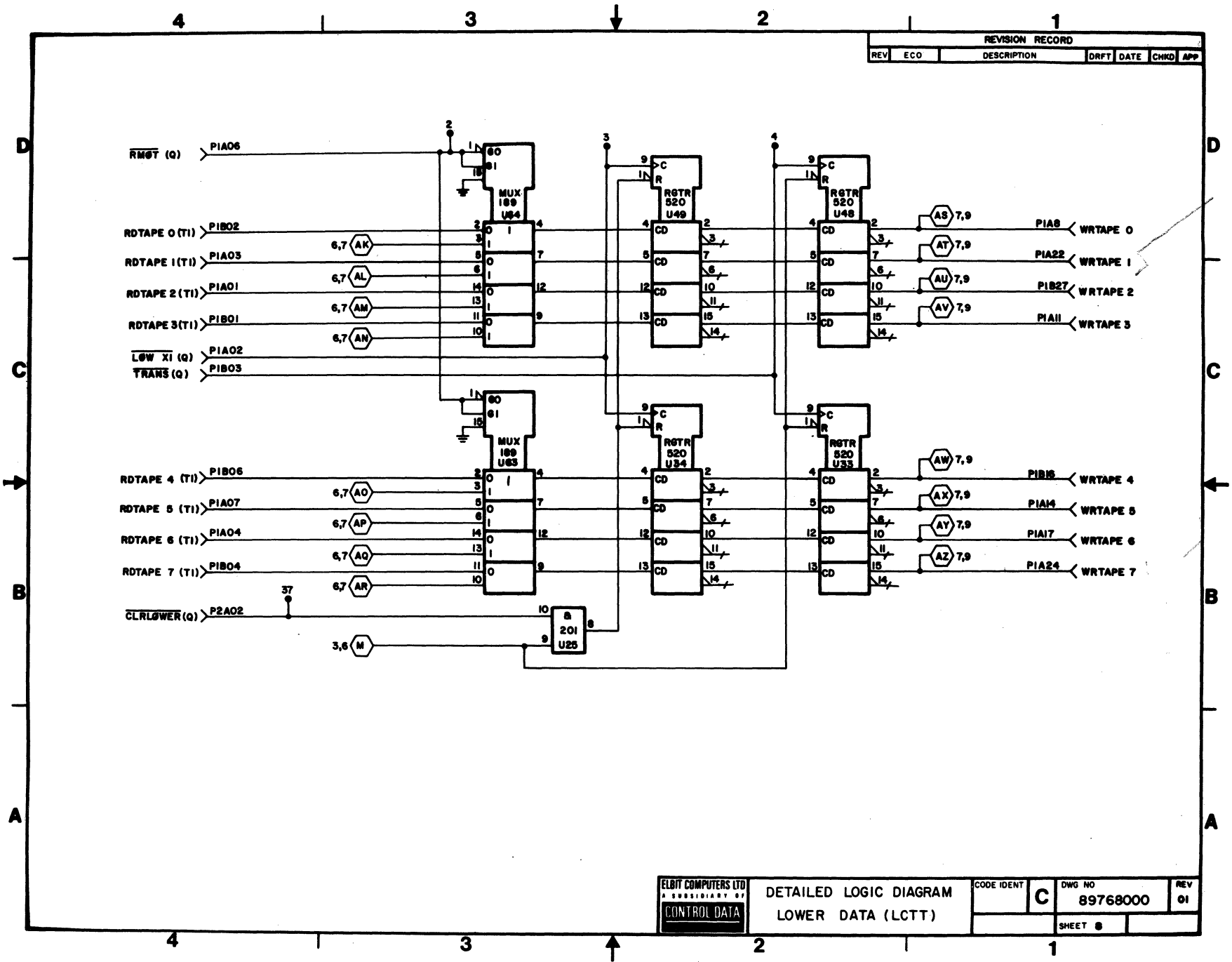
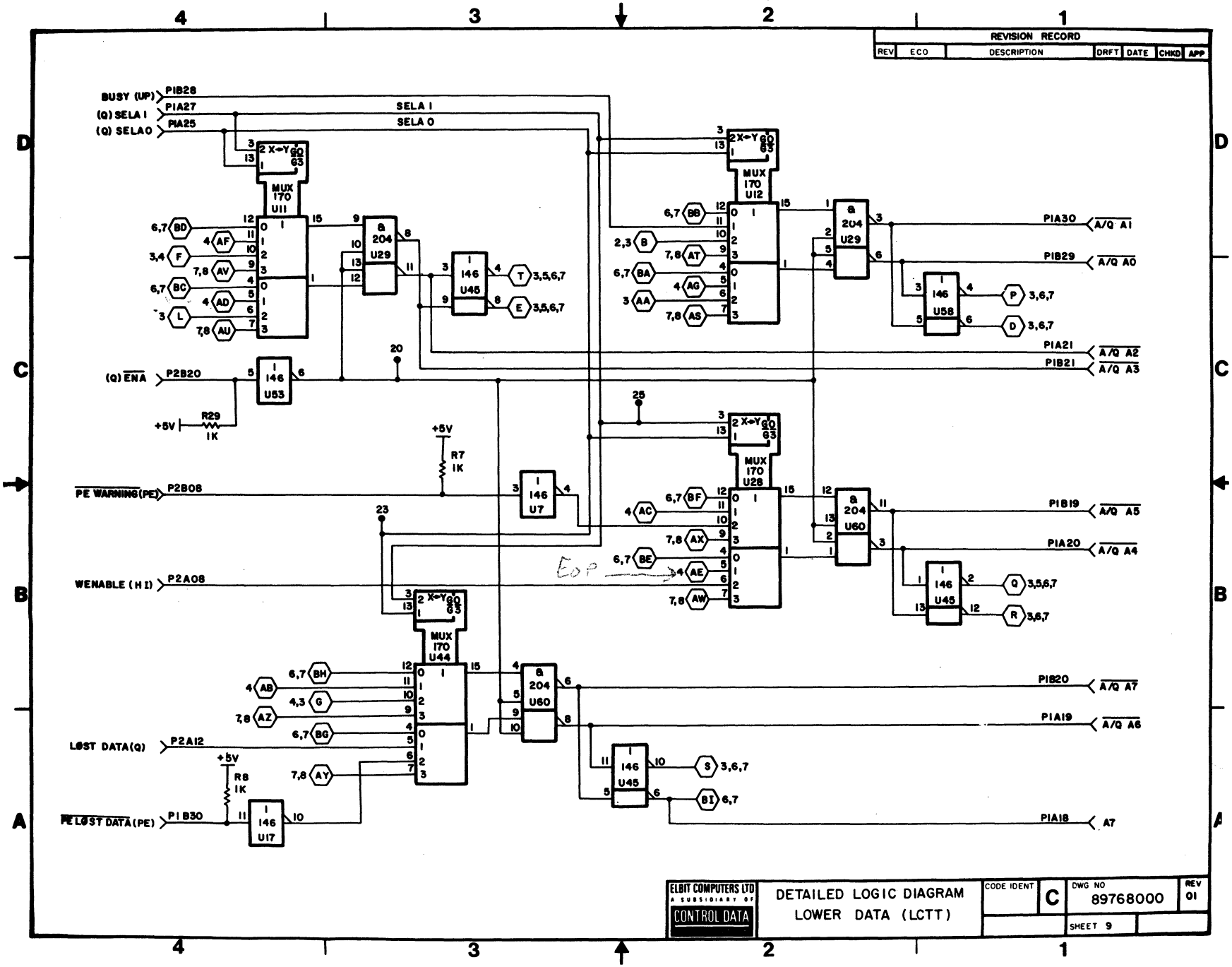


Figure 5-12. Lower A Data Path



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02



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UPPER DATA CARD (Logic Diagram 89767700)

UNIT SELECT CIRCUIT & LEGAL CONTROL FUNCTION DECODER (89767700, sheet 2)

Unit Select Circuit

This module selects (or deselects) a unit and the number of the unit. A three-bit register (U 45) stores this information. A selector (U44) selects the unit according to either the stored unit select number or the new one.

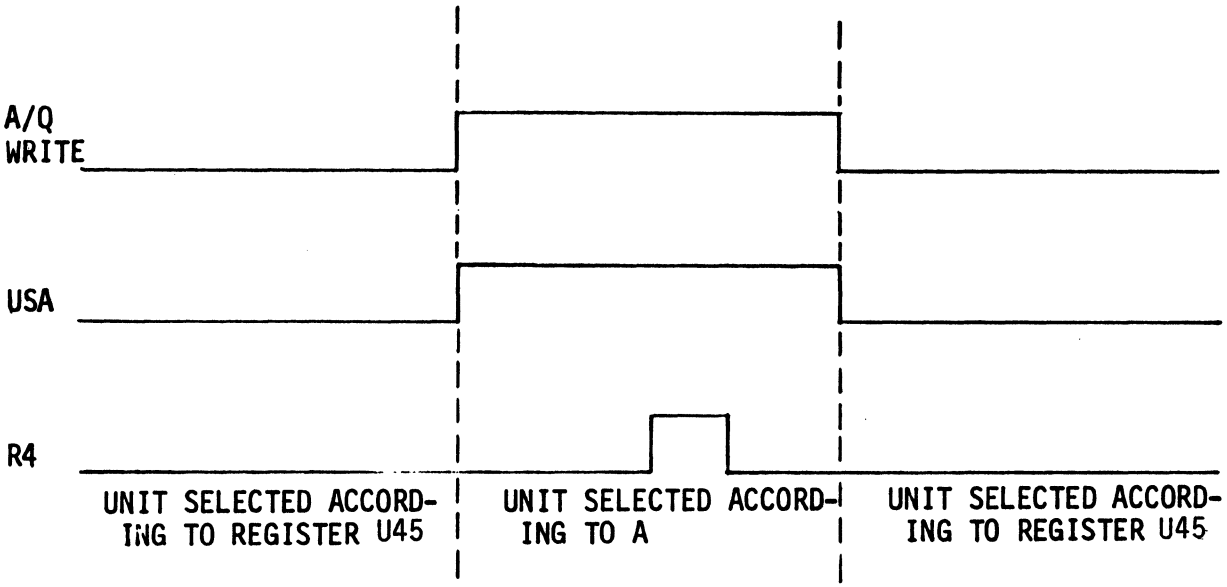

Figure 5-14. Unit Selection

If a Unit Select instruction is sent to the controller, the status of the new unit (if it is changed) is checked, register U45 is bypassed if A10=1, in order to determine if it should be accepted (Reply) or rejected (Reject). If the Unit Select is rejected, the previous unit is reconnected. The purpose of this feature is to reconnect a protected tape transport that has tried to disconnect.

Legal Control Function Decoder

This module computes the following combinational functions:

The illegal combination of the motion functions are:

(U11-8) $\overline{LEGMF} = A7 \cdot A10 + A10 \cdot A8 + \overline{A7} \cdot \overline{A8} \cdot \overline{A10}$

The illegal combinations of the eight most significant bits of the Unit Select Code are:

(U12-8) ILLUSCode = A9+A10·A11

The following function determines the Non-Stop Conditions:

NSCOND = LEGMF·$\overline{A10}$·($\overline{A7}$ ⊕ MØTCode7)·($\overline{A8}$ ⊕ MØTCode8)

The Control Function will be legal if LEGCF is high:

(U42-12) LEGCF = LEGMF·(A10+A8+$\overline{\text{File Protect}}$)·($\overline{\text{Busy}}$+MSCØND·EØP)

Explanation:

For a Control Function to be legal all three conditions must be satisfied:

1. The Motion Function Code must be legal (only 8 bits out of 16 are legal).

2. The Motion Function must not be a Write Function (A8+A10) or the File Protect ring must be placed on the tape.

3. The transport must be Not-Busy or if Non-Stop Motion conditions exist, then EØP must be set.

OFF-SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION 2	3	4	5	6	7	8	9
A	WRTAPE II					4B	ID	4C	
B	$\overline{\text{RMØT}}$	2D	2D				4D		
D					4A	2D	4B		
E					4A	2C	4B		
F					4A	2C	4B		
G					2A	2B	4C		
J					2A	2B	4C		
K					2A	2B	4C		
L					2A	2B	4C		
M	BØT	2D	4B					4C	
N	TT. READY	4D	3A						
P									
Q	A7		4D						4C
R	AII				2D	4C		3C	4C
S	A8		4D		3D	4C		IC	4C
T	A9		4D		2D	4C			4C
U	AIO		4D		3D	4B			4C
V	MØTCODE 8		3D						4B
W	MØTCODE 7		3D						4A
X	AI2				4D			IA	3A
Y	EØP		IC	4C					3A
Z	T3	4A		4C					
AA			4B						3A
AB	$\overline{\text{EØP}}$		IB						3B
AD	TT. BUSY		3B						2A
AE								3C	2B
AF	PREGAP	IB	3D	3C					2B
AG	WFM								
AH	WMØT								
AJ	PØSTGAP	IA		4D					
AK		2B	4D						
AL	REV	2A	IB						
AM	START	3D		2B					
AN	$\overline{\text{RES I.I}}$		3C	3D	4B				
AP									
AQ	CØNTACT		IC	2C				2B	
AR	GAP	4A		IB					
AS	STRMF		4C	2C					
AT	EØT		3A					2D	
AU	$\overline{\text{STOP}}$		4C	IC					
AV	$\overline{\text{RES I.I + CH. MODE}}$				IA		4B		
AW	AI5				4D	4C		3B	
AX	AI4				4D	4C		3B	
AY	AI3				4D	4C			
AZ	CURAD 15				3D	2A		4B	
BA	CURAD 14				3D	2B		4B	
BB	WRTAPE 15					4C	IA	4B	

		SHEET REVISION STATUS 1	2	3	4	5	6	7	8	9	REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
REVISION RECORD		01	01	01	01	01	01	01	01	01	01	CK 690	RELEASE TO CLASS B				
		02	01	02	01	01	01	01	01	01	02	CK 777	INVERTER U23 ADDED BETWEEN U21-1 & U8-11		Sep. 74		

		2	3	4	5	6	7	8	9
BC	CURADI3				3D	2A		2B	
BD	CURADI2				3D	2B		2B	
BE	CURAD II				ID	2E		4C	
BF	CURADIO				ID	2B		4C	
BG	CURAD 9				ID	2A		2C	
BH	CURAD 8				ID	2B		2C	
BJ									
BK									
BL	WRTAPE 9					4B	ID	3C	
BM	WRTAPE IO					4B	ID	4C	
BN	WRTAPE I4					4D	IA	4B	
BP	WRTAPE I2					4D	IB	2B	
BQ	WRTAPE I3					4C	IA	2B	
BR	WRTAPE 8					4B	ID	2C	
BS					4A	2C	4B		
BT									
BU									
BV									
BW									
BX									
BY									
BZ									
CA									
CB									
CD									
CE									

AW 89767500
AY 89767600

DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL

FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA

FIRST USED ON FA446-A

DWN	Naomi Palachy	8/9/74
CHKD		Sept 74
ENGR	S. Cohen	25/9/74
MFG		
APPR		

TITLE
DETAILED LOGIC DIAGRAM
UPPER DATA SECTION (LCTT)

CODE IDENT C

DRAWING NO 89767700

SCALE

SHEET 1 OF 9

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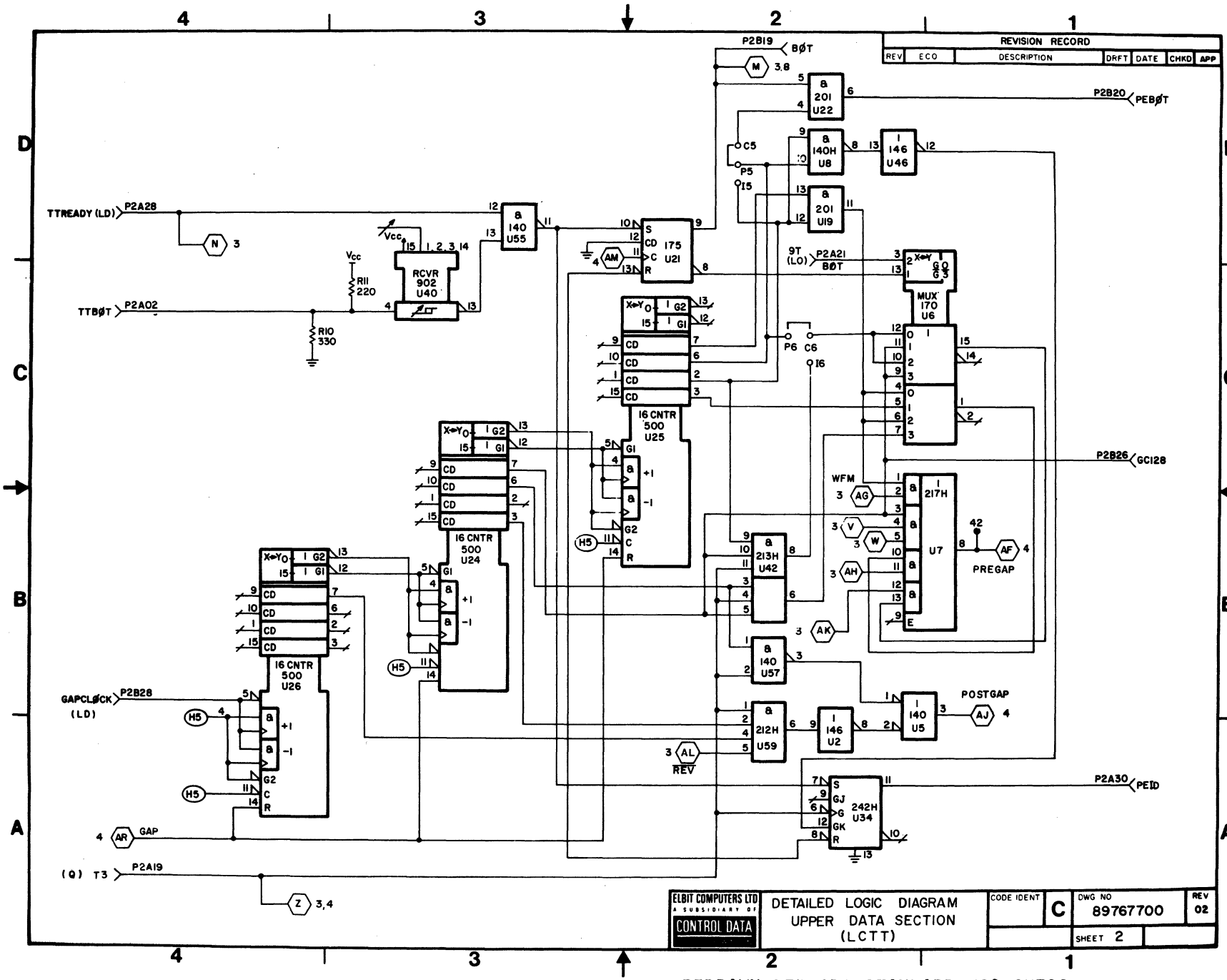
SHEET IS REV 03



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

GAP TIMING GENERATOR (Logic Diagram 89767700, sheet 3)

This module includes the gap counter U24, U25, U26 and timing decoder. It also includes the BØT and EØP FF's.

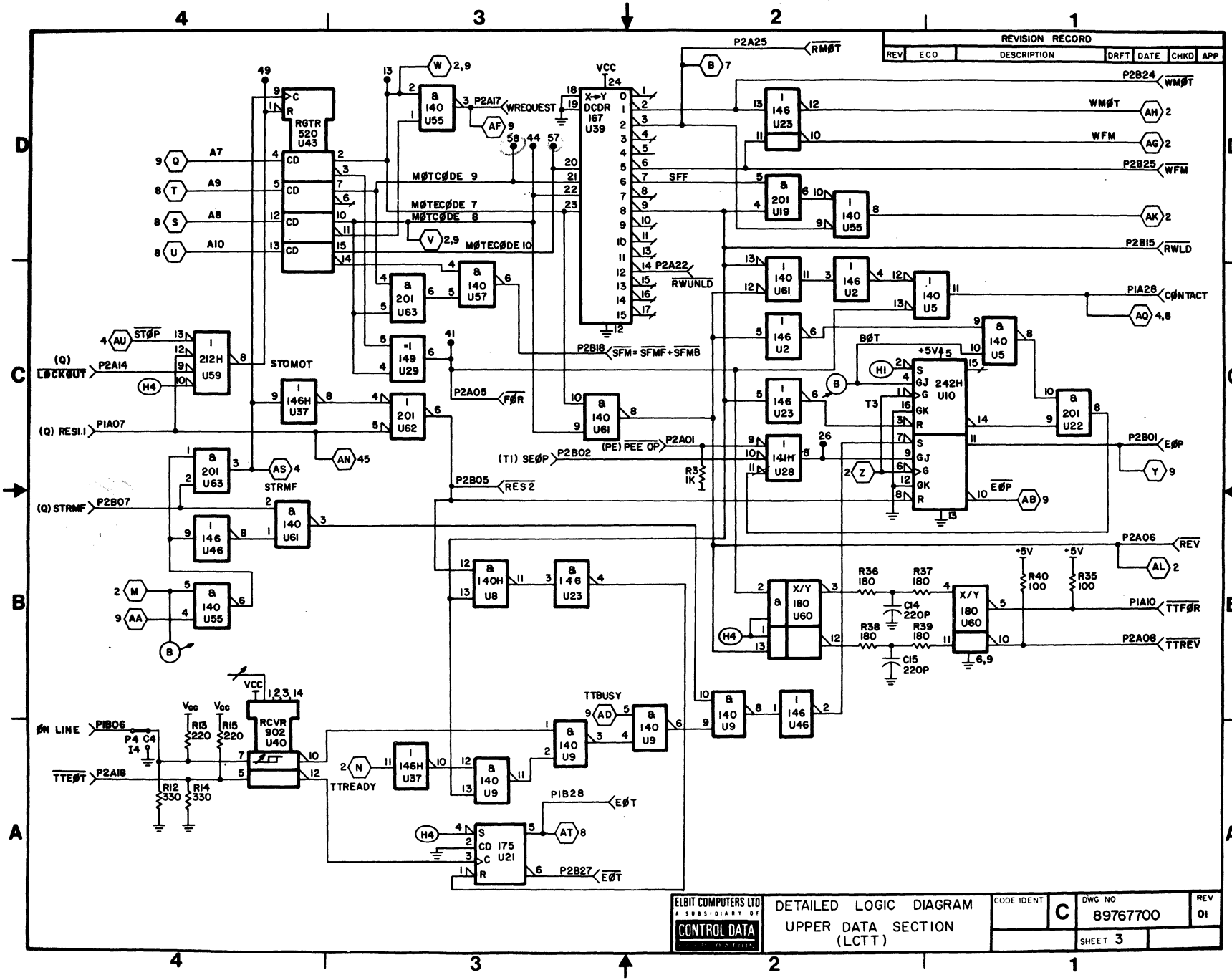
The gap counter counts Gapclock pulses when CountEn is high. The Pregap and Postgap counts are as described in Table 5-4.

TABLE 5-4. PREGAP - POSTGAP COUNTS

SIGNAL	PREGAP COUNT (PULSES AT U7-8 OR TP42)				POSTGAP COUNT (PULSES AT U5-3)			
	9T		7T		9T		7T	
	BØT	$\overline{\text{BØT}}$	BØT	$\overline{\text{BØT}}$	BØT	$\overline{\text{BØT}}$	BØT	$\overline{\text{BØT}}$
READ (U7-12 & 15)(R)	1536	128	1536	128	24	24	24	24
WRITE (U7-10 &111)(W)	2560	192	2560	256	24	24	24	24
BACKSPACE (U7-4 & 4) (B)	NA	128	NA	128	NA	64	NA	64
WRITE FMTM (U7-1 & 2) (F)	2560	2560	2560	2560	24	24	24	24

BØT (U21-9) is set by $\overline{\text{TTBØT}}$ and is reset by the rise of Start.
EØT is set by $\overline{\text{TTEØT}}$ and reset by RES2

PEBØT (U22-6) sets if BØT is high after 1024 Gapclock pulses. PEID (U34-11) is set if BØT is high and is reset after 1536 pulses.



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

MOTION FUNCTION EXECUTION (Logic Diagram 89767700, sheets 3 and 4)

Motion Function Register

This module includes a four-bit Motion Function register (MØTCode (7-10) U43), the logic that sets and clears the register and the logic that decodes the Motion Functions from the register.

The register is set from A7, A8, A9 and A10 (at U3-4, -5, -12, -13).

The register is set by the rising of STRMF if the function is not a Backword Motion at BØT, and not RWUNLD.

$$(U63\text{-}3) = STRMF \cdot B\emptyset T \cdot \overline{(A7 \oplus A8) \cdot A9 \cdot A10}$$

The register is reset by Stop+RES1+Lockout+IDAbort.

The following Motion Functions are decoded from the Motion Function register:

M denotes MØTCode

$WM\emptyset T$	$= M7 \cdot \overline{M8} \cdot \overline{M9} \cdot \overline{M10}$	(U23-12)
$\overline{RM\emptyset T}$	$= \overline{M7} \cdot M8 \cdot \overline{M9} \cdot \overline{M10}$	(U39-3)
WFM	$= M7 \cdot \overline{M8} \cdot M9 \cdot \overline{M10}$	(U23-10)
$\overline{RWLD}$	$= \overline{M7} \cdot \overline{M8} \cdot \overline{M9} \cdot M10$	(U39-9)
$\overline{RWUNLD}$	$= \overline{M7} \cdot \overline{M8} \cdot M9 \cdot M10$	(U39-14)
$\overline{F\emptyset R}$	$= \overline{M7} \oplus M8$	(U29-6)(TP41)
$\overline{REV}$	$= M7 \cdot M8$	(U61-8)
$\overline{WREQUEST}$	$= M7 \cdot \overline{M8}$	(U55-3)
$\overline{SFM}$	$= M8 \cdot M9 \cdot \overline{M10}$	(U57-6)
RMØT+SFF+RWLD		(U55-8)
CØNTACT	= FOR+REV+RWLD	(U5-11)

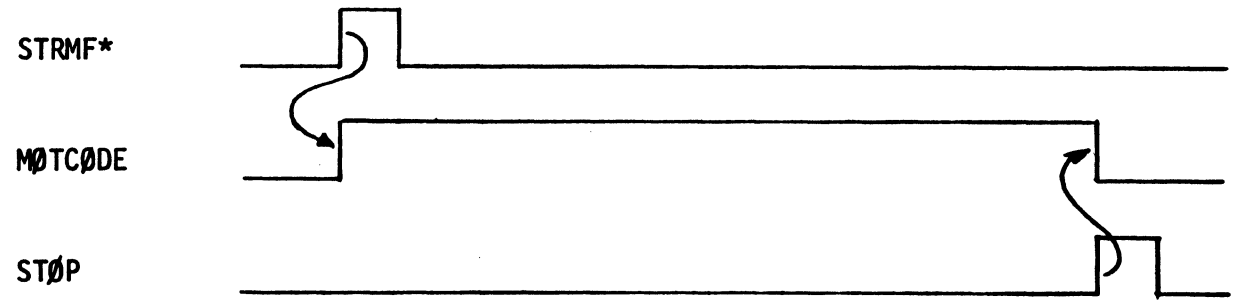


Figure 5-15. Motion Function Control

Motion Sequencer

This module includes the EØP FF and the logic that sets it, and the Motion Sequencer that indicates the Start, Stop and EØG (End of Gap).

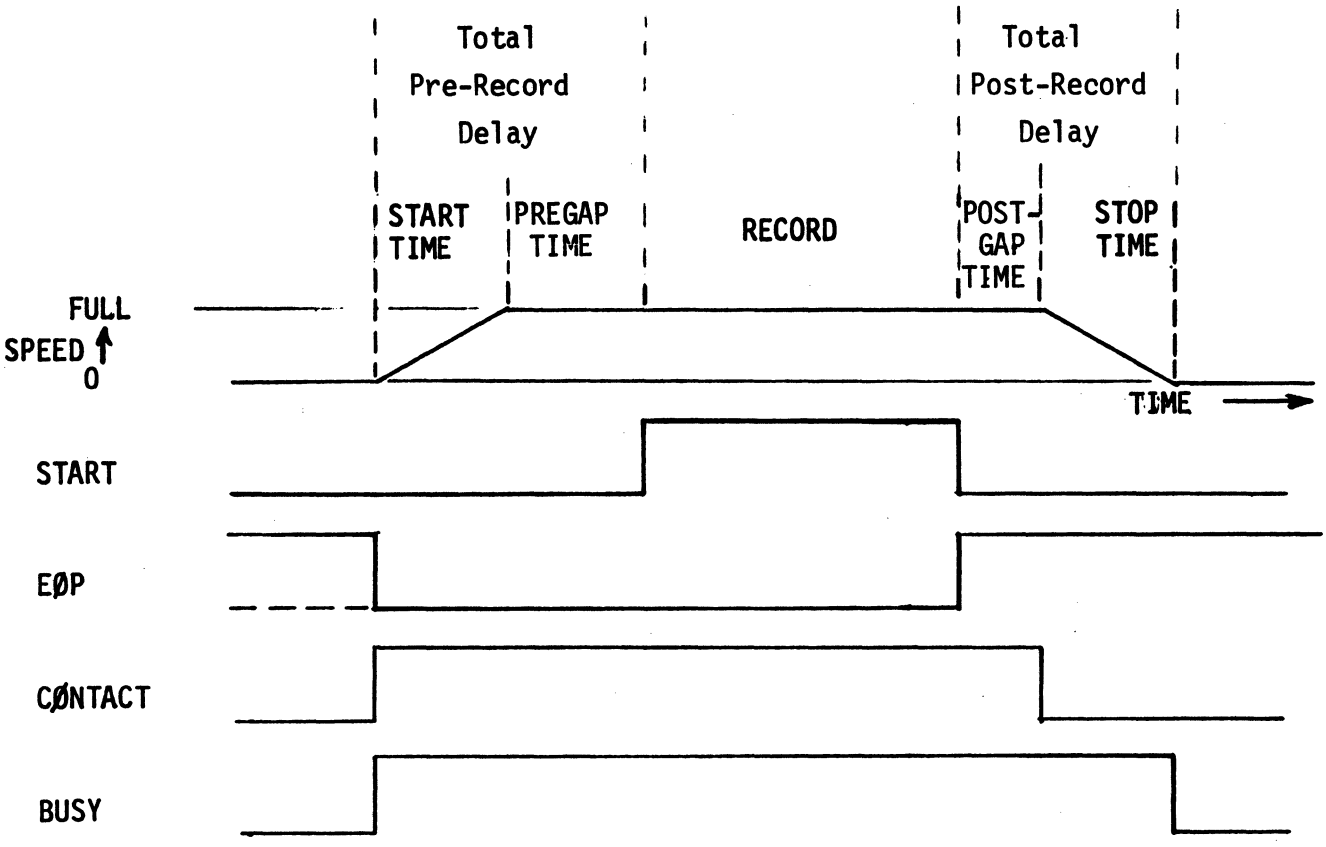


Figure 5-16. Motion Sequencer Control (Single Record Timing)

EØP-FF:

The EØP FF(U10-11)is cleared by:

(U62-6) RES2 = RES1+STRMF

EØP is cleared by one of the following conditions (U28-8):

1. STRMF = STRMF·BØT·($\overline{A7}$ + A8)·$\overline{A9 \cdot A10}$ (U24-3). This is a Reverse Motion Function from BØT, which is replied to, but no motion takes place.
2. Rising of SEØP
3. Rising of PEEØP
4. Rising of BØT if REV motion is in operation (U5-8).
5. Rising of TTReady after finishing RWND operation (U22-8).

Motion Sequencer:

The Motion Sequencer consists of a five-bit shift register S0, S1, S2, S31, S32(U56-9, U3) and a Nonstop FF (U56). Only one of the FF's in the Sequencer is set at any time. First S0 is set, then S1, S2, S31 and S32 in turn.
S0 is set by the rising of STRMF if S2 is low. The "1" is shifted by:

U4-8 = S0 Pregap+S1·EØP+S2·Postgap+(S31+S32)·T3

S1 clears S0, so that only one bit in the Sequencer can be set.

Nonstop is set by STRMF if Contact is high. If Nonstop is low, then the last state of the Sequencer S32, is the Stop signal (U57-11) that resets Contact. If Nonstop is high, then S32 presets S0 and resets the rest of the sequencer (U57-8).

Refer to the motion operations described in Figures 5-17 and 5-18.

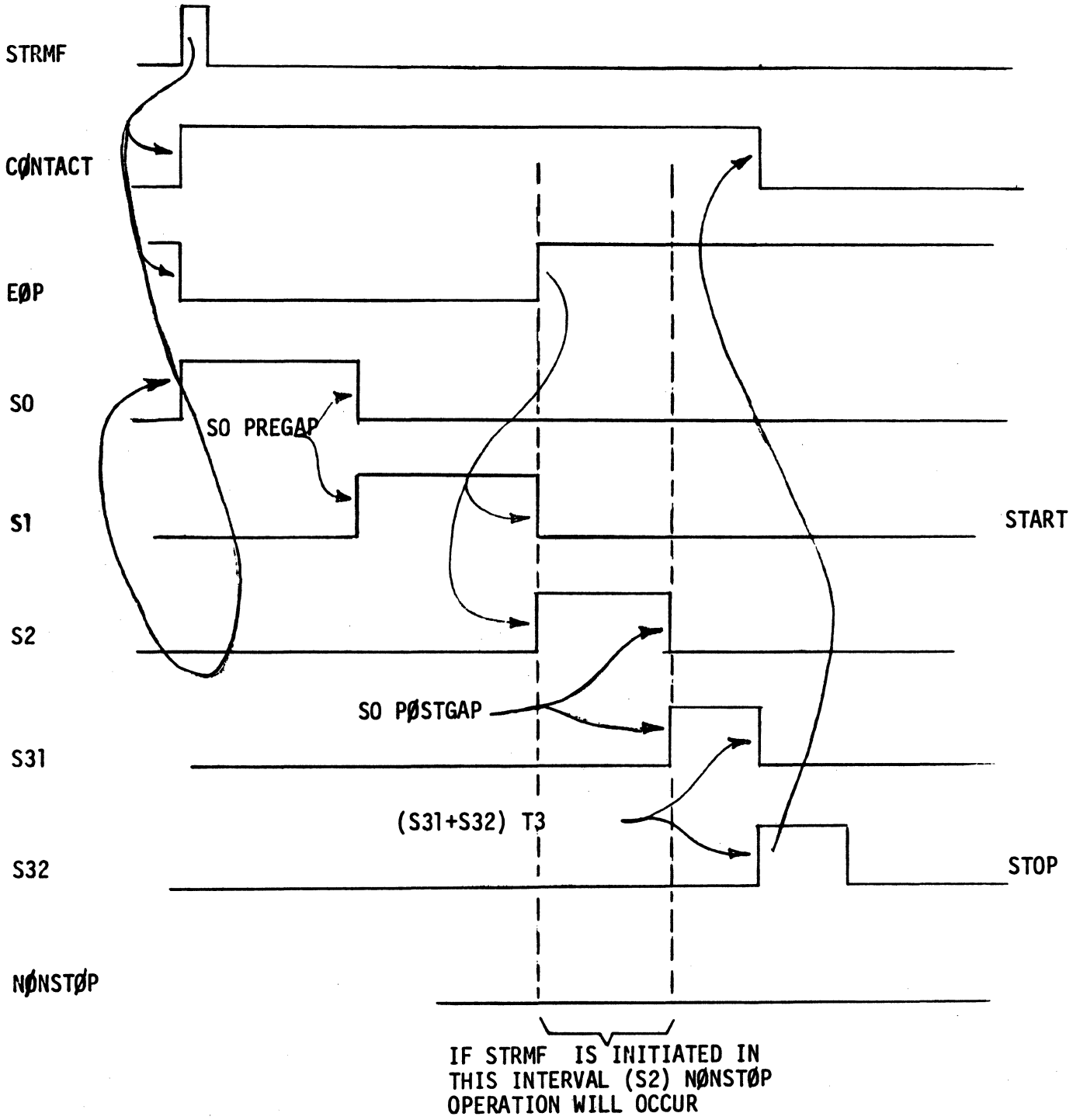


Figure 5-17. Normal Motion Operation

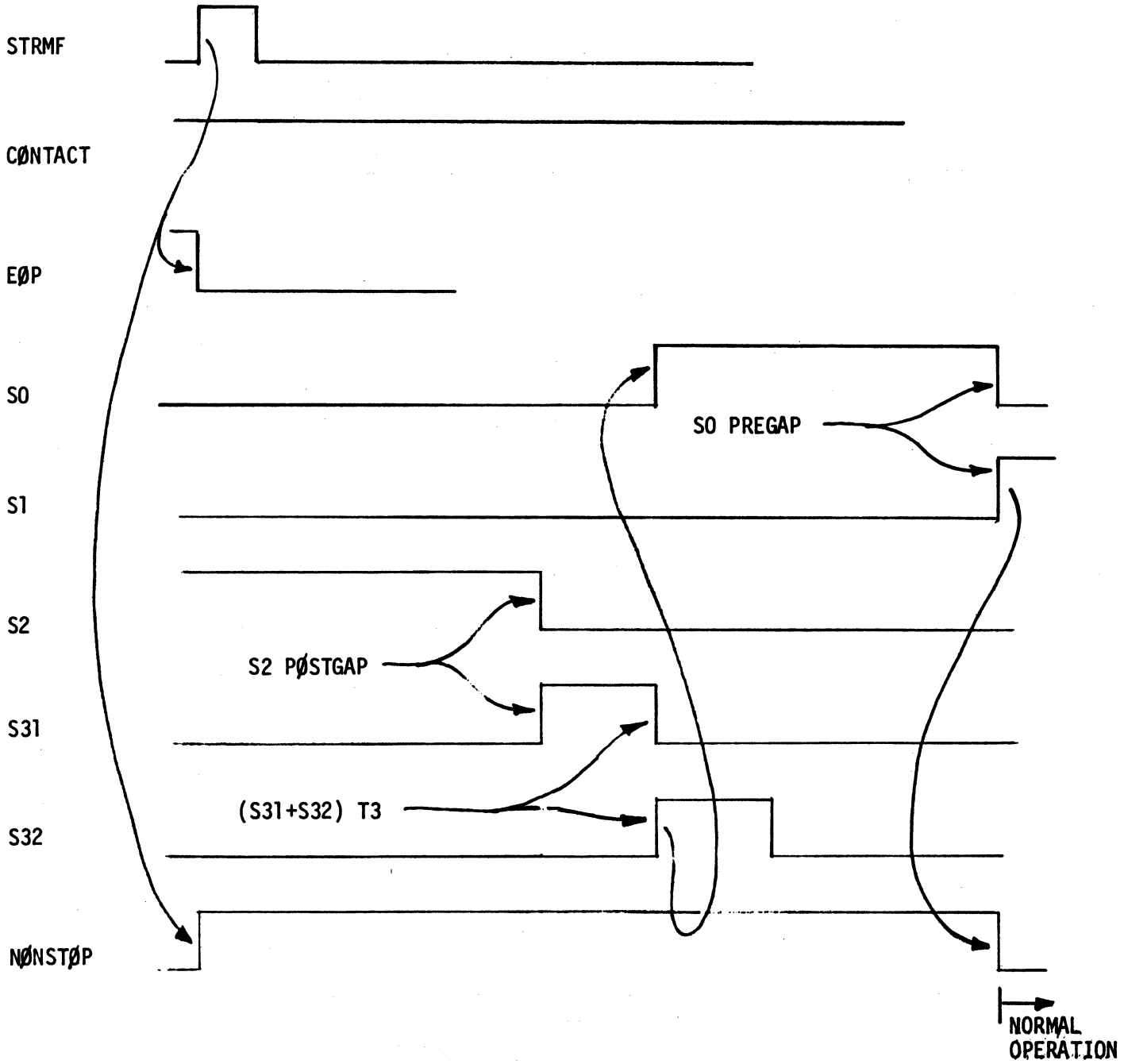
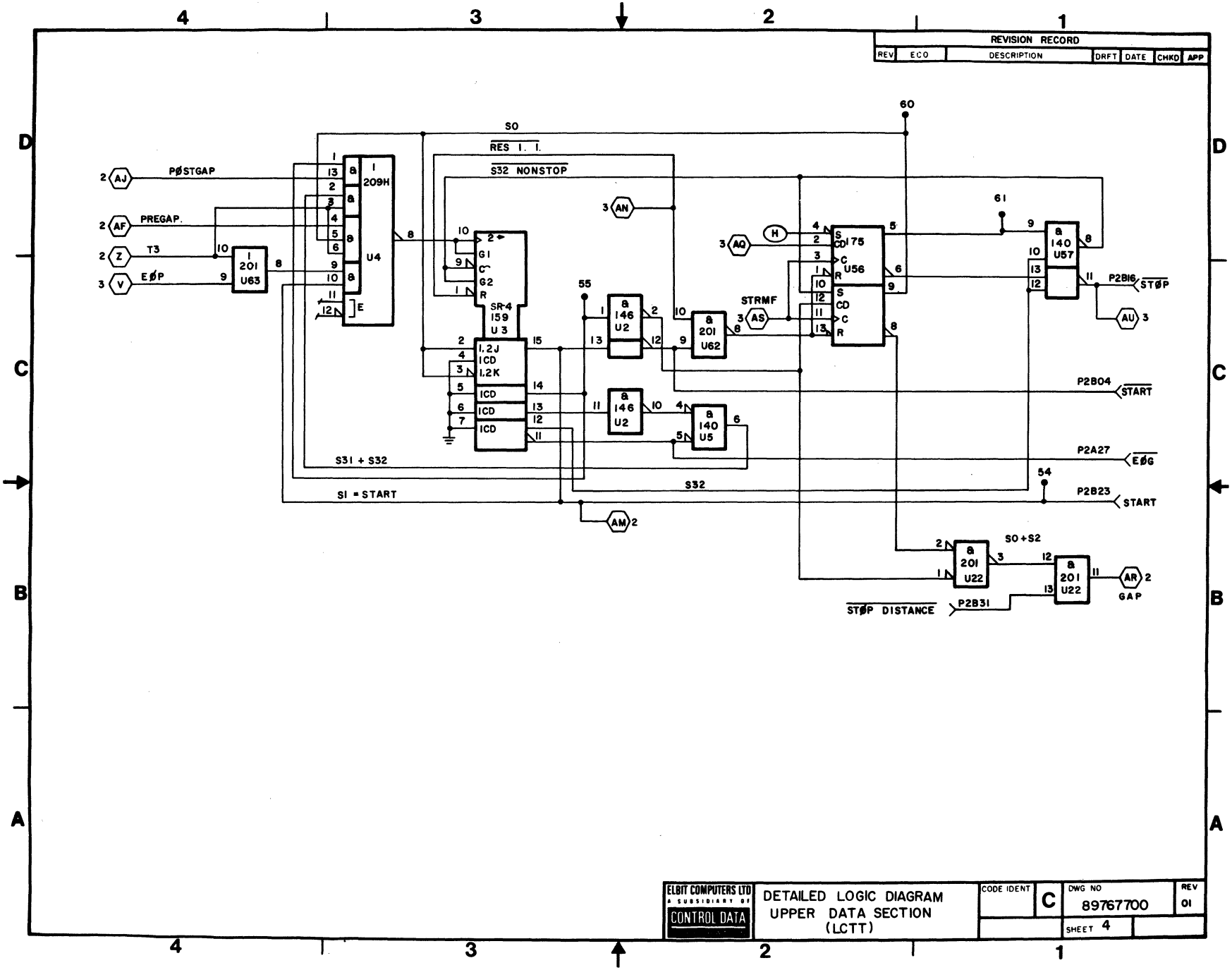


Figure 5-18. Non-Stop Motion Operation



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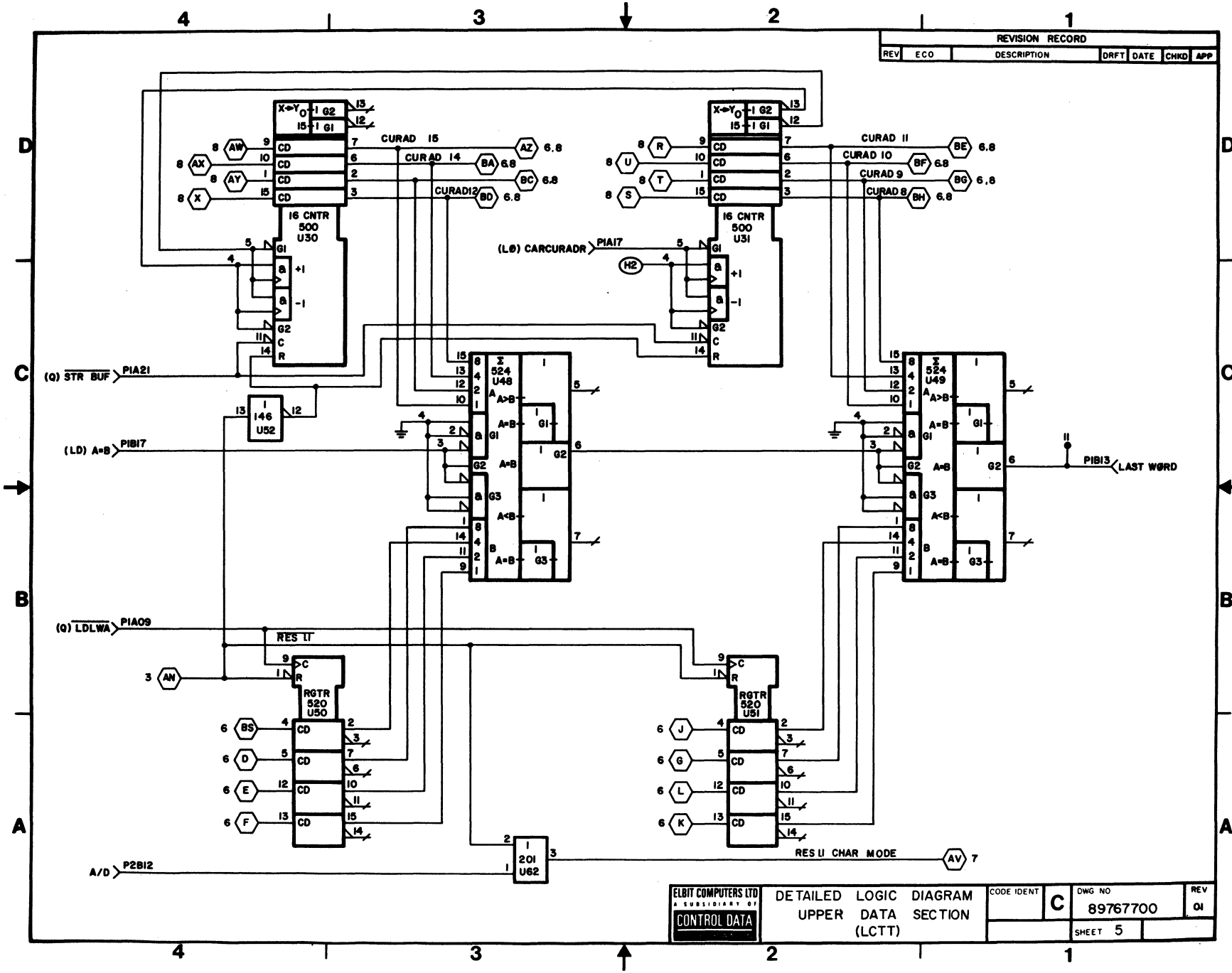


REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

UPPER A DATA PATH (Logic Diagram 89767700, sheets 6 and 7)

For the block diagram of the Upper A Data Path, refer to Figure 5-19.

RDTAPE 0-7 signals from the tape transport are passed through a multiplexer U72 (RDTAPE 0-3) and U71 (RDTAPE 4-7), when $\overline{\text{RMØT}}$ is low. With $\overline{\text{RMØT}}$ high, DATA IN 8-15 signals from the computer through U68, U69, are admitted. The outputs of this multiplexer (Selector 1) are then supplied to Buffer 1 (U54, U53), which is controlled by the signal $\overline{\text{UPPX1}}$, through U54-9 and U53-9. Buffers 1 and 2 are cleared by $\overline{\text{RES1.1}}$+$\overline{\text{CHAR MODE}}$. Buffer 2 (U36, U35) further passes the signal to produce WRTAPE 8-15 signals for the tape transport, when the $\overline{\text{TRANS}}$ signal is low (U36-9, U35-9) and $\overline{\text{RMØT}}$ is high (U72-1 and U71-1). With $\overline{\text{RMØT}}$ low, the RDTAPE 0-7 data is available for transfer to Selector 2 (multiplexers U15, U16, U17 and U18), but will only be accepted when the sum of SELA0 and SELA1 represents a binary 3. If SELA0 and SELA1 signals are both low (binary 0), only STATUS signals are passed through Selector 2. When SELA0 is high and SELA1 is low (binary 1), STATUS 1 is selected, and if SELA0 is low and SELA1 is high (binary 2), STATUS 2 is selected. These signals are NANDed through U64, U47 when enabled by $\overline{\text{ENA}}$ (high), to the A-bus to the computer.

When signals are received from the computer A-bus, they are admitted through U65, U67 to the other Upper Data Section circuitry.

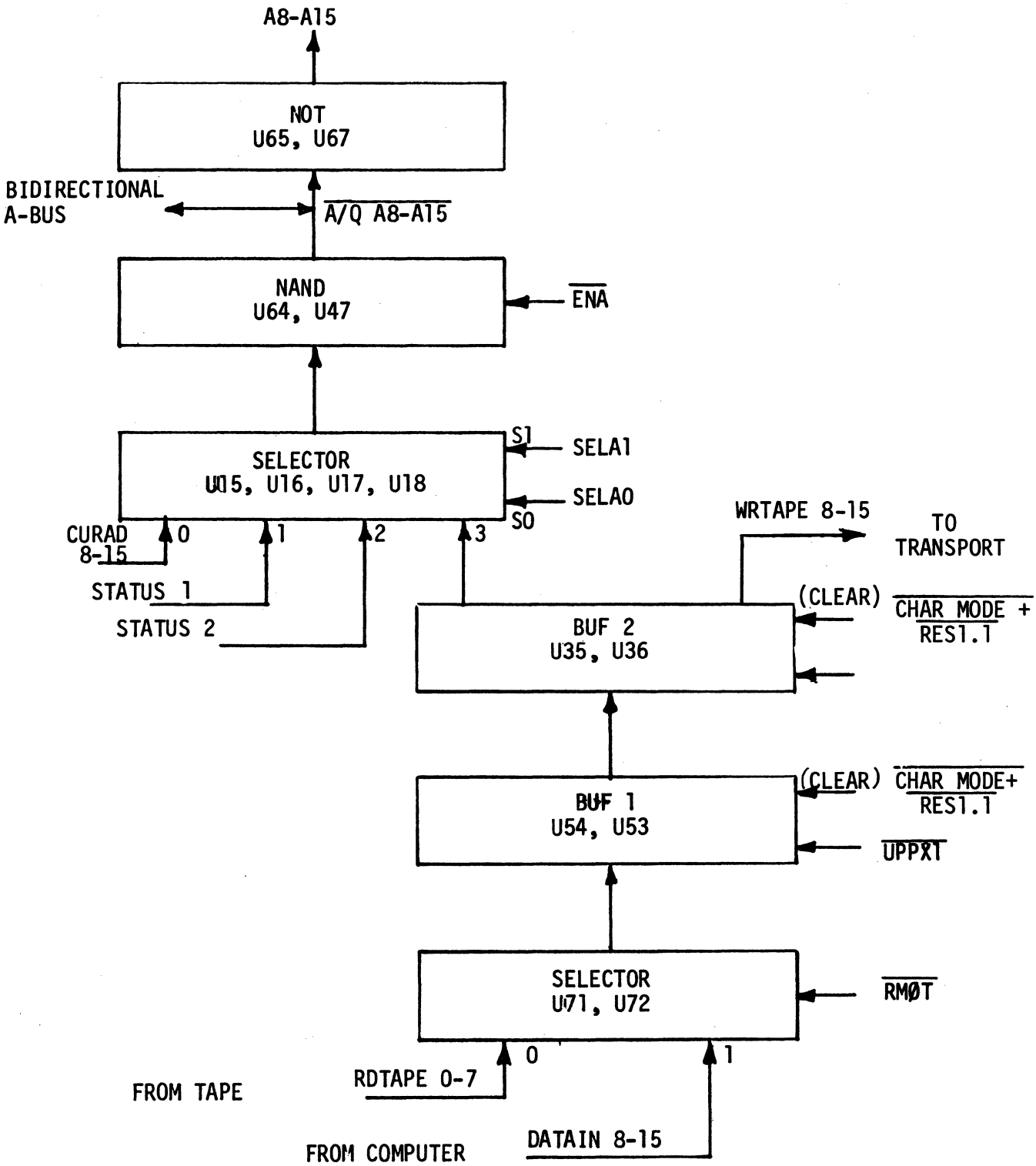
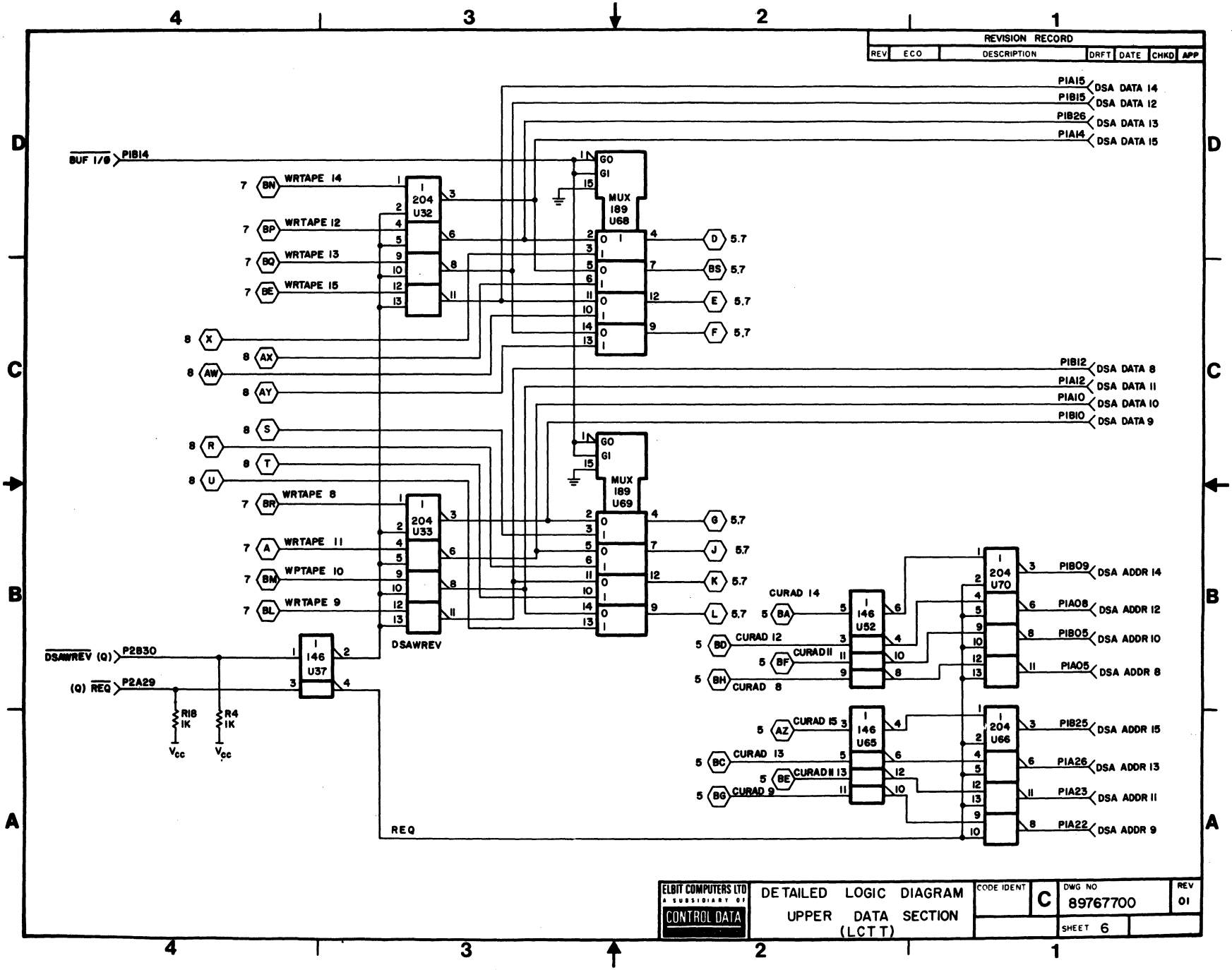
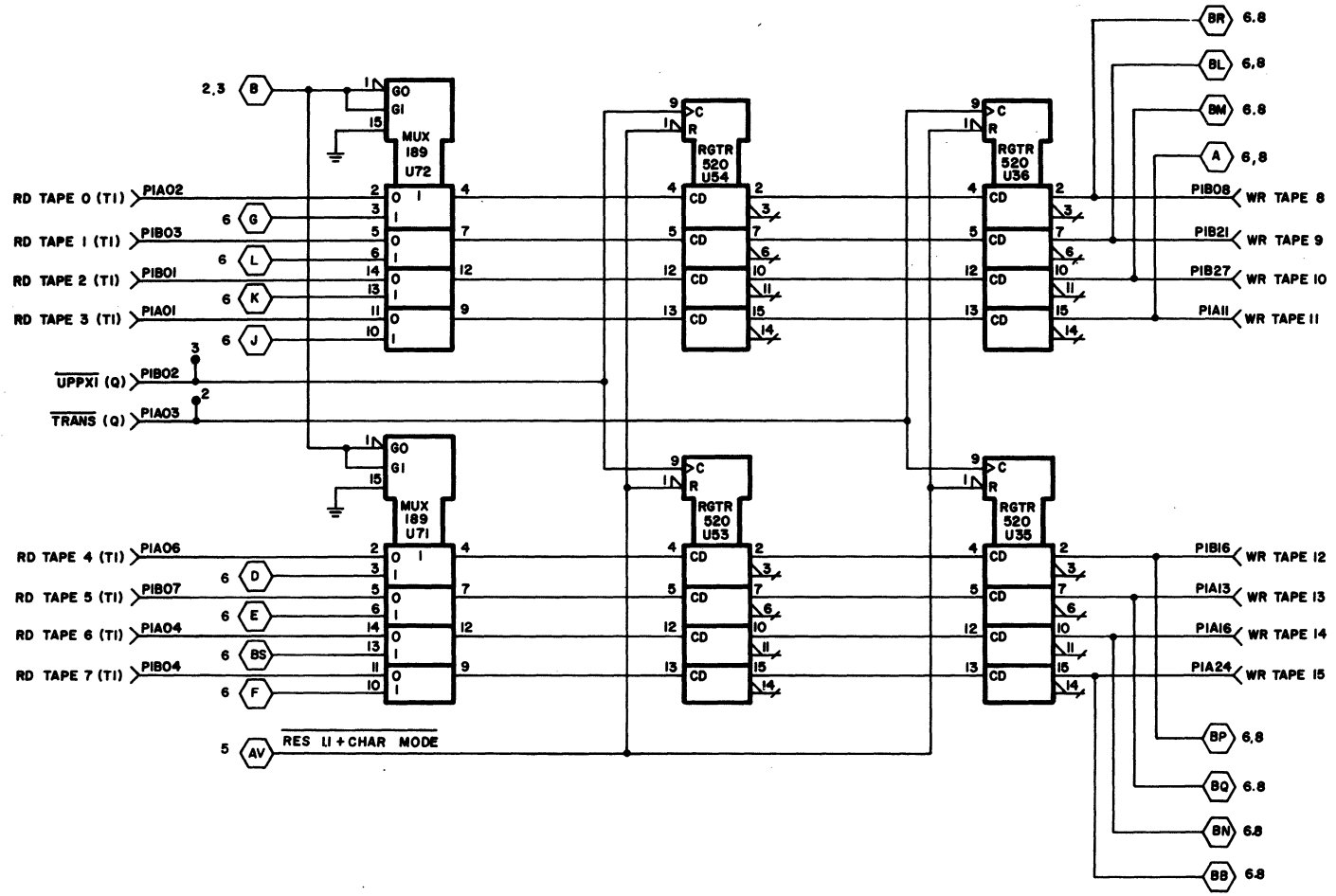


Figure 5-19. Upper A Data Path



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP



ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	DETAILED LOGIC DIAGRAM UPPER DATA SECTION (LCTT)	CODE IDENT C	DWG NO 89767700	REV 01
			SHEET 7	

REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

UPPER DSA DATA PATH (Logic Diagram 89767700, sheets 7 and 8)

$\overline{\text{STRBUF}}$ initiates DSA transfer and presets CURADDR (8-15) to the contents of A(8-15). The A/Q DSA Selector is set by BUF I/O to DSA and $\overline{\text{LDLWA}}$ strobes the contents of DSA Data (8-15) into LWA-1.

For every transfer Request enables the Current Address on the DSA ADDR lines and the falling of INCCA increments the Current Address. When Writing the data is transferred through DSA Data (8-15) A/Q DSA Selector to the Double Buffer.

When Reading from the computer the data is transferred from the tape, the Double Buffer and DSA WREN enables the data to pass to the computer memory.

Last Word is the comparator signal that indicates the detection of the last word.

Refer to Figure 5-20.

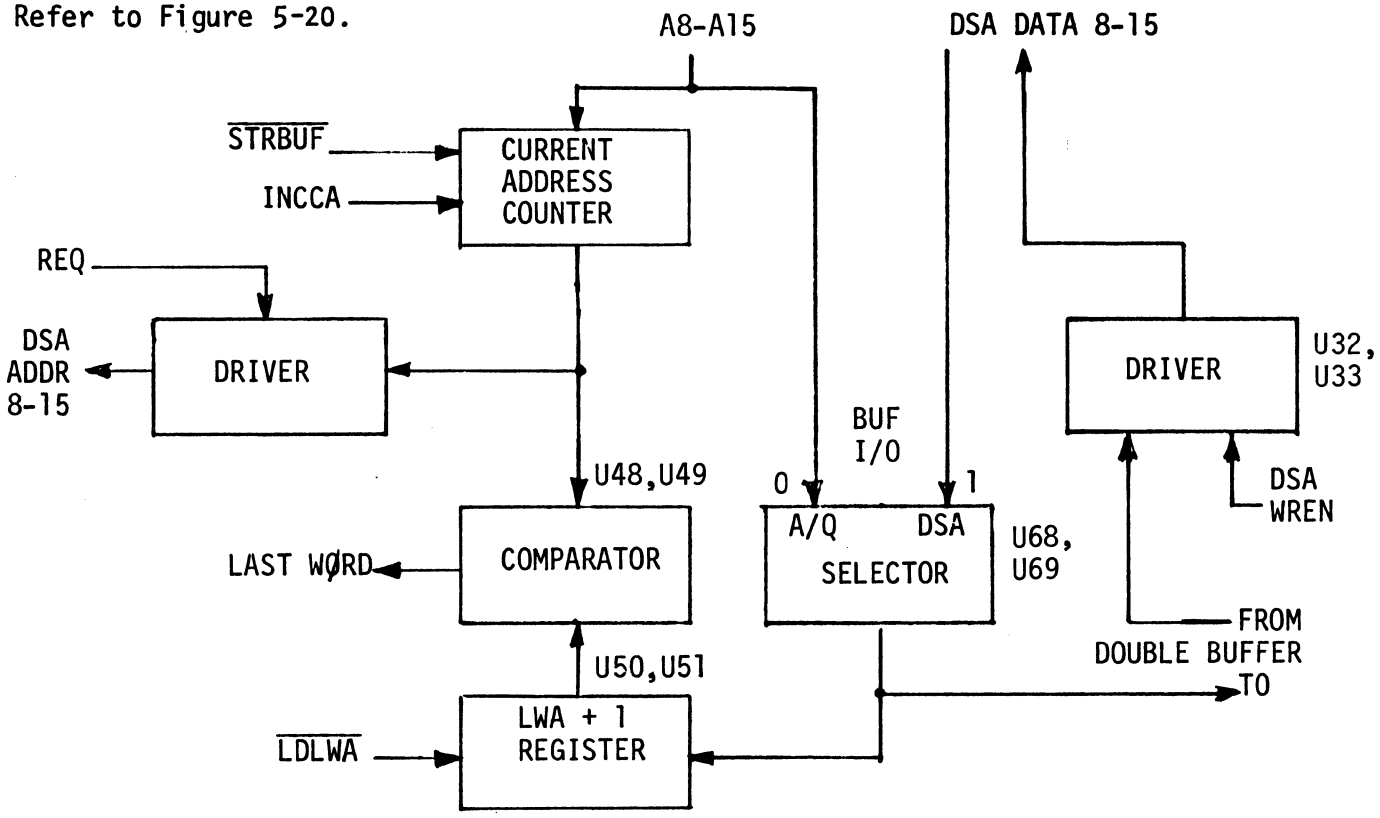
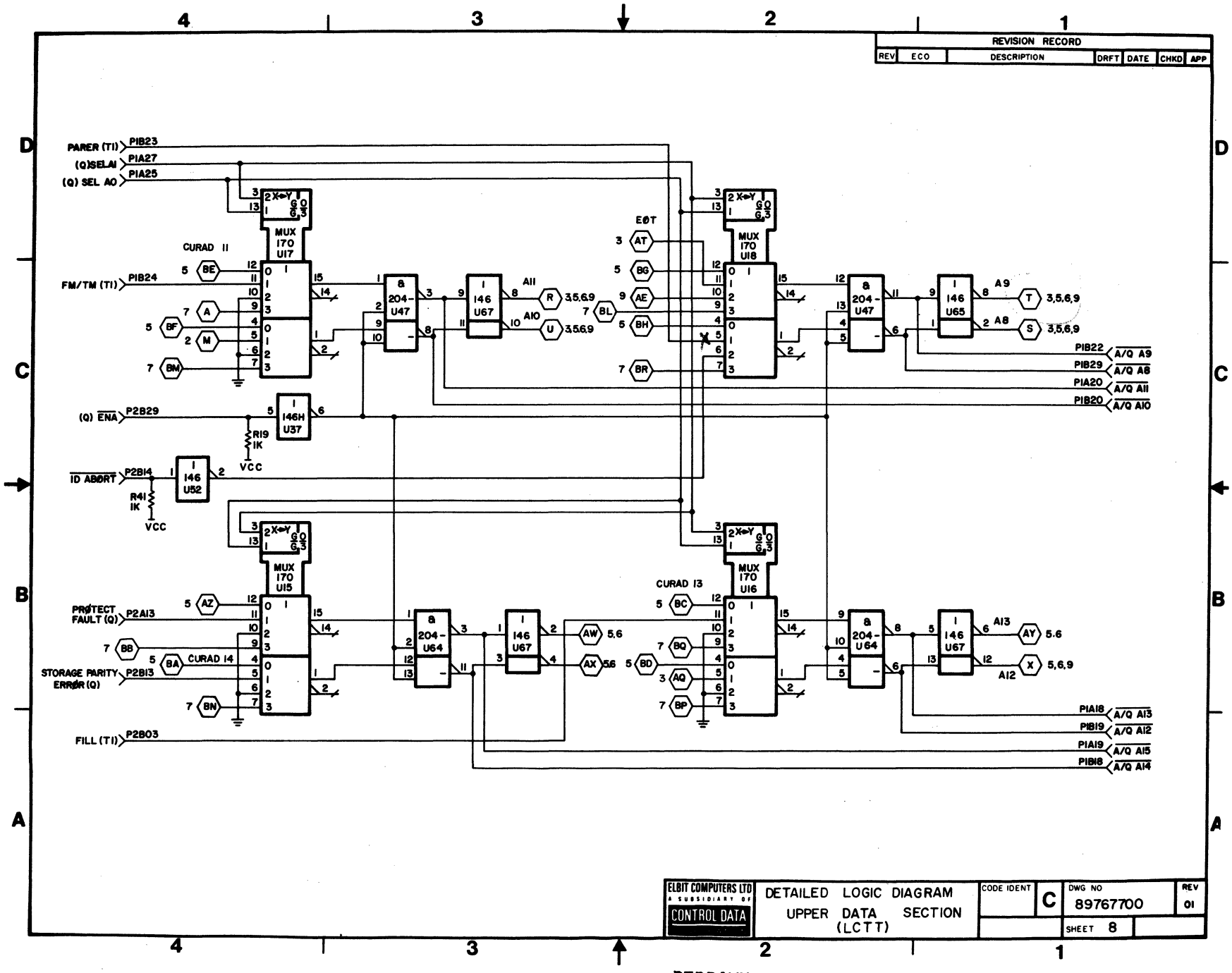
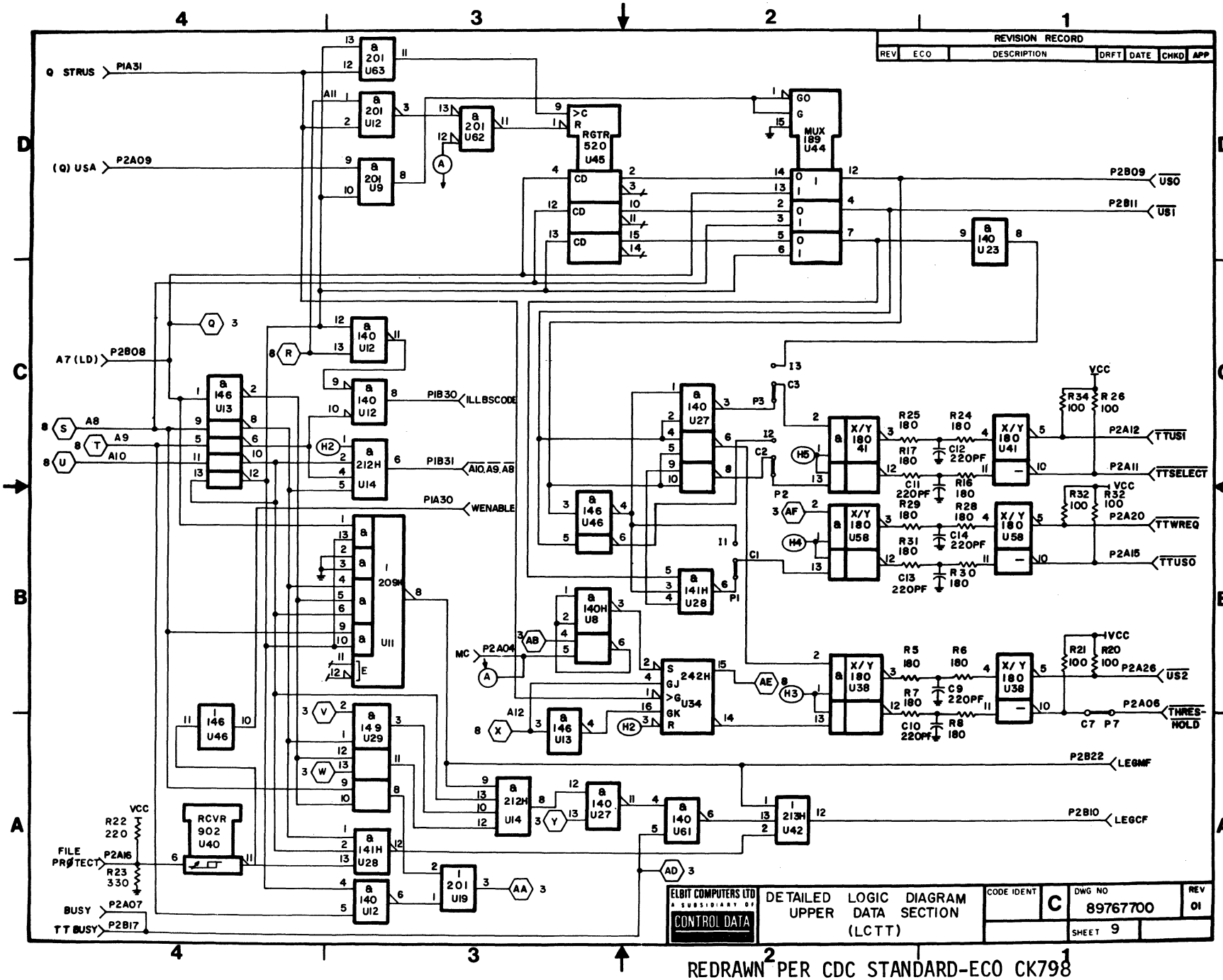


Figure 5-20. Upper DSA Data Path



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

TAPE INTERFACE CARD (Logic Diagram 89768600)

CRC GENERATOR/DETECTOR (Logic Diagram 89768600, sheet 2)

This module consists of the Circular Redundancy Check Character (CRCC) register. It is operational only in nine track, 800 bpi operation.

The CRCC has the following properties:

1. It can be an all zeros character, therefore no RDS is transmitted from MTT.

2. Its value is such that the LRCC always has odd parity (therefore the LRCC can never be all zeros).

3. It has odd parity when there are an even number of data characters, or even parity for an odd number of data characters.

4. When writing, 1 frame of 00_{16} on tape, the CRCC is EB_{16}.

TABLE 5-5. DATA/CRCC RELATIONSHIP

SIGNAL	7	6	5	4	3	2	1	0	P
DATA	0	0	0	0	0	0	0	0	1
CRCC	1	1	1	0	1	0	1	1	1

This module checks and generates a CRCC as described on page

The module also contains CRC-ERR FF and the CRC Strobe logic as described:

(U39-11) Strobe CRC = WDS+RMØT·2NDSP·(RDS+MISCRC)

2NDSP = space between CRCC and LRCC

MISCRC = pseudo RDS, when CRCC is all zeros.

(U58-12) $\overline{\text{CRC ERR CØNDITIØN}}$ =U55-10·9T·$\overline{\text{(WMØT+BKSP) FM STATUS}}$

During WMØT and Backspace,U55-10 is not looked at. During FM STAT a CRC ERR is forced.

The CRC register is toggled at the falling edge of WDS during Write and the falling edge of RDS during Read.

The $\overline{\text{CRC ERR}}$ FF U22-5 is clocked at EØP and preset by $\overline{\text{RES2}}$·$\overline{\text{RWLD+RWUNLD}}$.

OFF-SHEET REFERENCE

OFF-SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION 2	3	4	5	6	7	8	9
A	INCRC 6	B-4							C-3
B	INCRC 5	B-4							C-3
C	INCRC 4	B-4							C-3
D	INCRC 3	B-4							B-1
E	AE	D-4	B-1						
F	$\overline{RDS}$	D-4	C-3						
G	ISTSP	D-4	B-1						
K	INCRC 0	C-4	C-1						
L	AB	D-3			C-3				
M	STRØBE DATA	D-3			B-2			C-3	
N	$\overline{RDS}$	A-4	C-3	A-3	D-3				
P	$\overline{MISCRC}$	A-4	D-4						
Q	INCRC 2	A-4							C-1
R	CLEAR 1	C-3	C-4					B-2	
S	$\overline{2NDSP}$	A-3	B-2						
T	RMØT	A-3						C-2	D-3
W	WMØT	D-3							C-4
X	CRCC 1	A-2					A-4		
Y	CRCC 2	A-2					B-4		
Z	CRCC 3	B-2					C-4		
AA	CRCC 4	B-2					C-4		
AB	CRCC 5	B-2					C-4		
AC	CRCC 6	B-2					C-4		
AD	CRCC 7	B-2					D-4		
AE	CRCC 8	C-2					A-4		
AF	AD	D-1			A-2				
AG	$\overline{FM/TM\ STATUS}$	D-2			C-1				
AK	EØP	D-1	A-4		A-2				
AL	AF	D-1	C-3						
AM	9T	D-2			A-3	B-4	C-4		
AN	INCRC 1	B-1							B-1
AO	CRCCØ	B-1					A-4		
AP	SFM·$\overline{FMSTAT}$		A-2		D-1				
AQ	FM1		B-2		D-4				
AR	GAP		B-3		A-2				
AS	CLEARA		C-3	A-3	D-3				
AT	RWND&RWNDUL		C-4					B-1	
AU	2FWC1		C-4					B-2	
AV	DETLRC			C-1	A-2				
AW	RD7			D-4	C-4				C-3
AX	RD6			C-4	C-4				C-3
AY	RD5			C-4	C-4				C-3
AZ	RD4			C-4	C-4				C-3
BA	RD3			B-4	B-4				D-1
BB	RD2			B-4	C-4				D-1
BC	RD1			B-4	B-4				D-1

SHEET REVISION STATUS

1	2	3	4	5	6	7	8	9
01	01	01	01	01	01	01	01	01
02	01	01	01	01	01	01	02	01

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	CK 690	RELEASED TO CLASS B				
02	CK 733	LOGIC CHANGE U34 & U49				

		2	3	4	5	6	7	8	9
BD	RDO			B-4	C-4				D-1
BE	RDP			A-4	C-4				D-3
BF	RDS*				B-2			C-1	
BG	INCRCP	C-4							D-2
BH	INCRC7	C-4							B-3
BI	$\overline{BCD}$				B-4	A-2			
BJ	$\overline{9T}$				A-2		B-4		
BK	BCD				B-4	A-3			
BL	PWDIN 4					C-2			B-4
BM	PWDIN 5					C-2			B-4
BN	PWDIN 7					C-2			B-4
BO	PWDIN 6					C-2			B-4
BP	PWDIN 3					B-2			B-2
BQ	PWDIN 2					B-2			B-2
BR	PWDIN 0					B-2			C-2
BS	PWDIN 1					B-2			B-2
BT	PWDINP					B-2	A-4		D-3
BU	AA						A-2	C-3	
BV	EØRS						D-4	C-4	
BW	1600						D-4	D-3	B-4
BX	$\overline{WFM/TM}$						D-4	C-4	

AW 89758500
AY 89768400

DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±

DO NOT SCALE DRAWING

MATERIAL

FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

FIRST USED ON FA446-A

DWN	NEOMI P.	15.8.74
CHKD		
ENGR	S.	
MFG		
APPR		

TITLE
TAPE INTERFACE (LCTT)

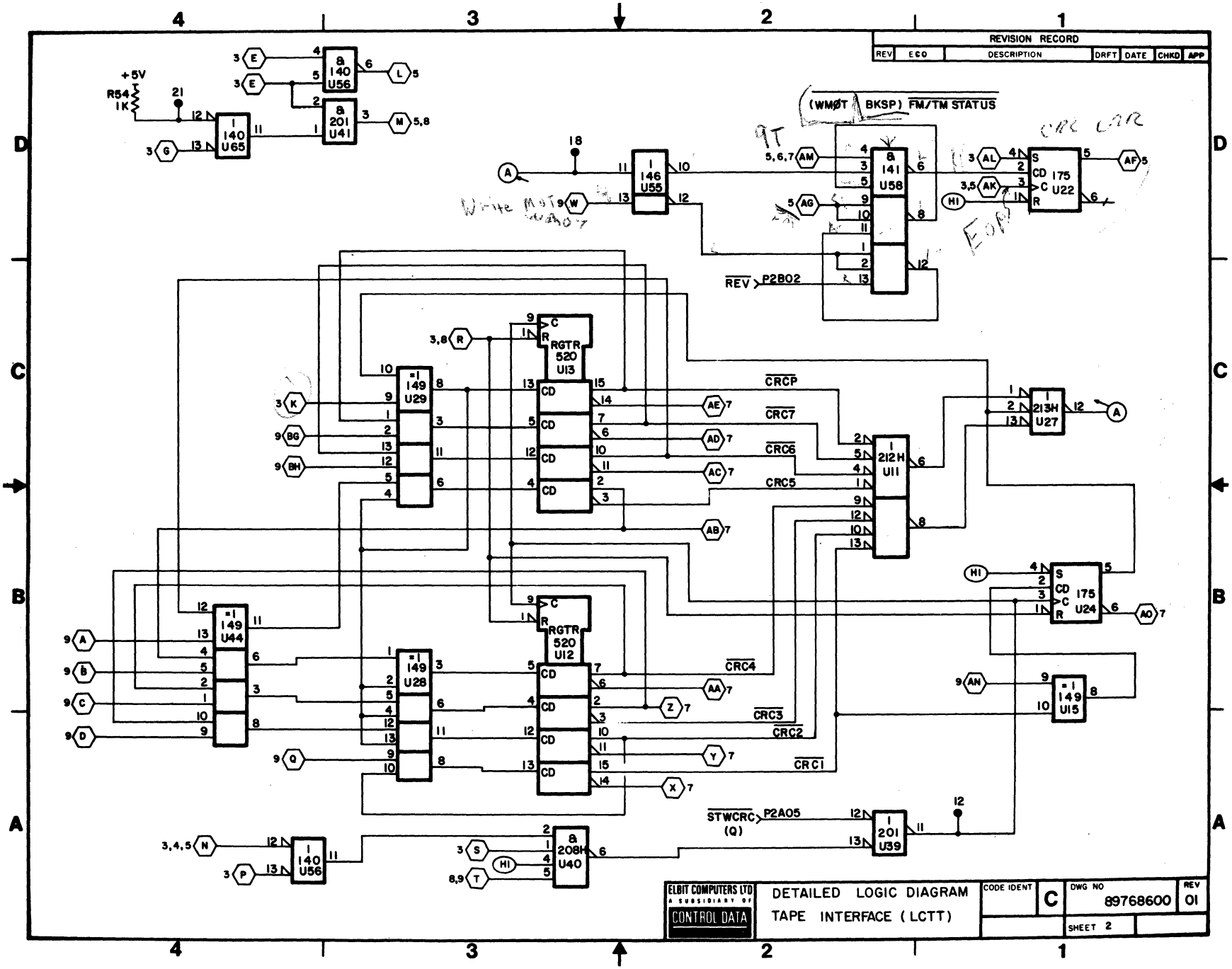
CODE IDENT C

DRAWING NO 89768600

SCALE

SHEET 1 OF 9

REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 03



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

DATA STROBE/EØR DETECTOR (Logic Diagram 89648200, sheet 2)

U7 is a filter that rejects pulses of width less than 250 seconds. It clips 250-500 seconds from the beginning of $\overline{\text{TTRDS}}$.

U24-9 and U25 is the End Of Record Counter which is used during Read Motion and during Write Motion in Read After Write Mode. A 2FWC counts it up. RDS resets the counter. The counter is blocked if it reads 32. MISCAR (U27-6) and MISCRC (U40-8) are decoded from the counter (refer to Figure 5-22).

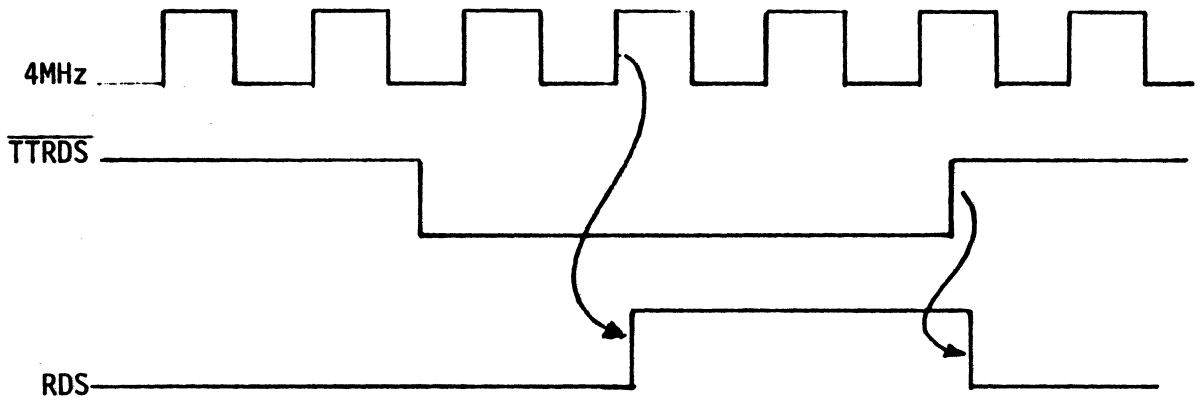


Figure 5-21. Data Strobe Generation

This counter detects gaps, by looking for 16 missing Read Data Strobes. It detects the space (1STSP) between Data Area and CRCC (nine track) or Data Area and LRCC (seven track).

In addition it generates a pseudo-RDS (MISCRC) in the cases where the CRCC is all zeros (Null Character = 000000).

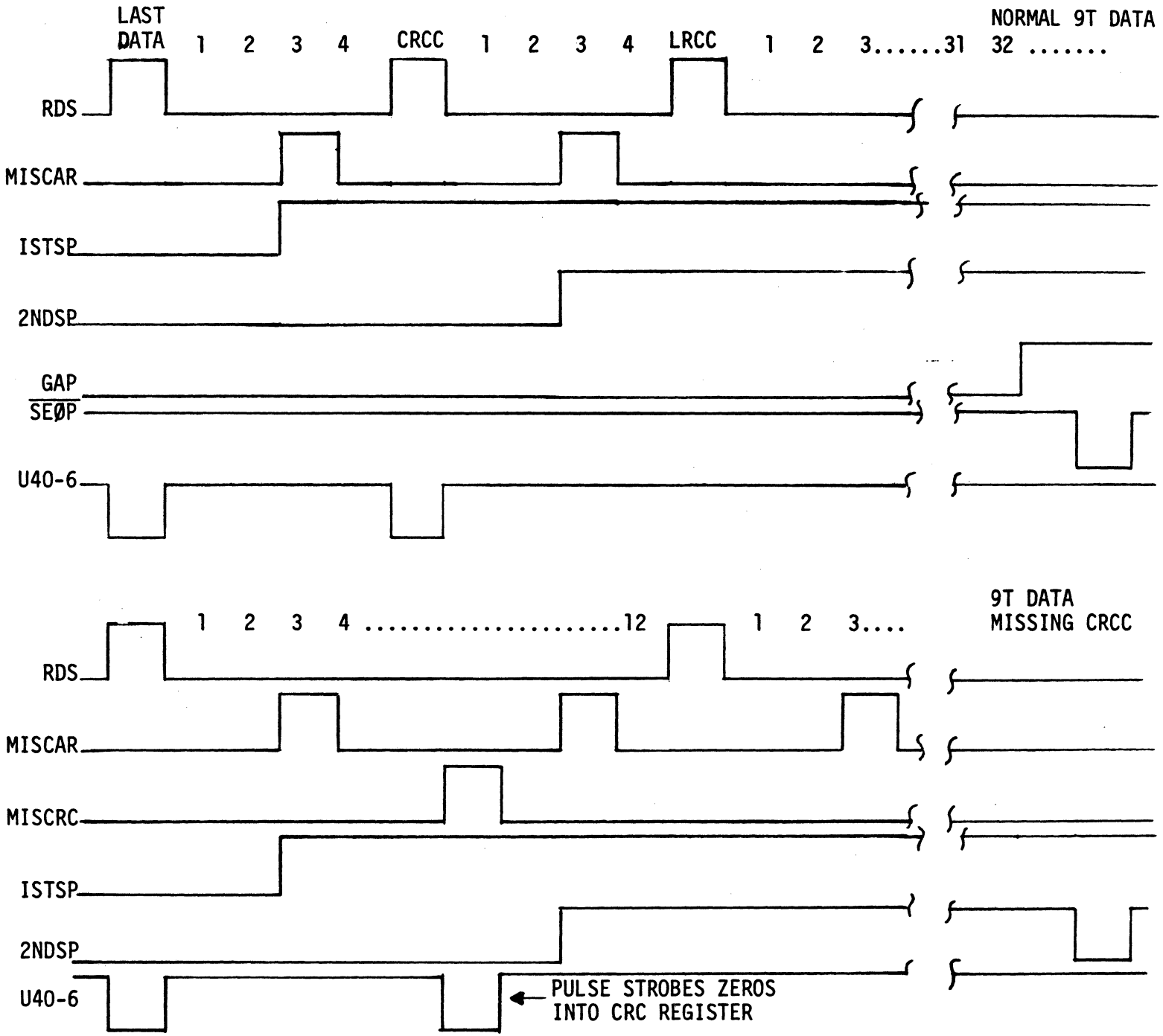
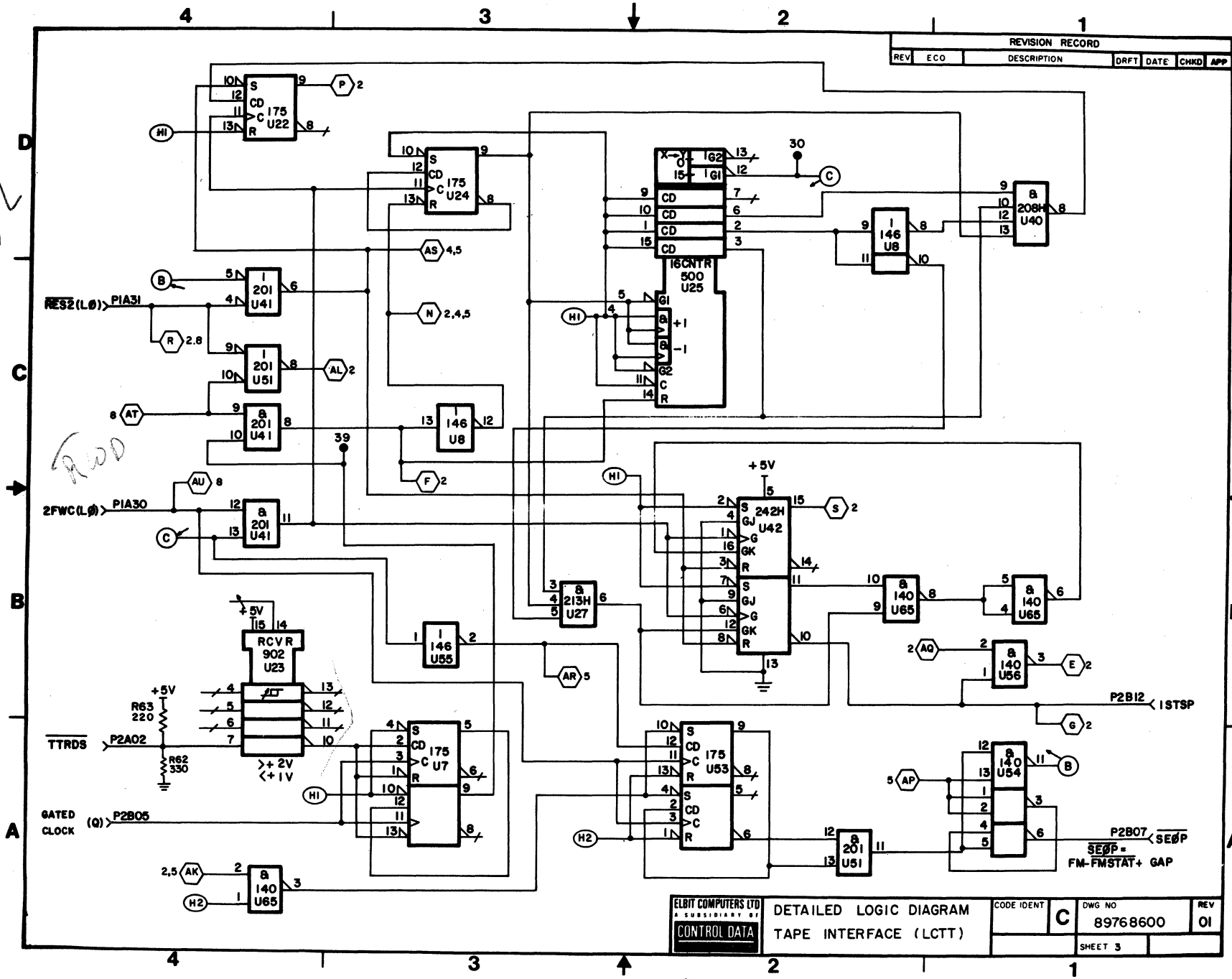


Figure 5-22. Normal Strobed Data



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

LRC DETECTOR (Logic Diagram 89768600, sheet 3)

This module consists of a nine-bit Longitudinal Redundancy Check Register (U14, U45 and U61). Each FF is toggled when the Data Read from the tape is high. It also includes the All Zero Decoder (U27-8), and the strobing signal RDS. While reading any data from the tape every character is added bit by bit to the LRCC register at the moment $\overline{RDS}$ rises.

The LRCC is generated by the MTT in Write Motion when receiving the Write Reset signal (U2-10).

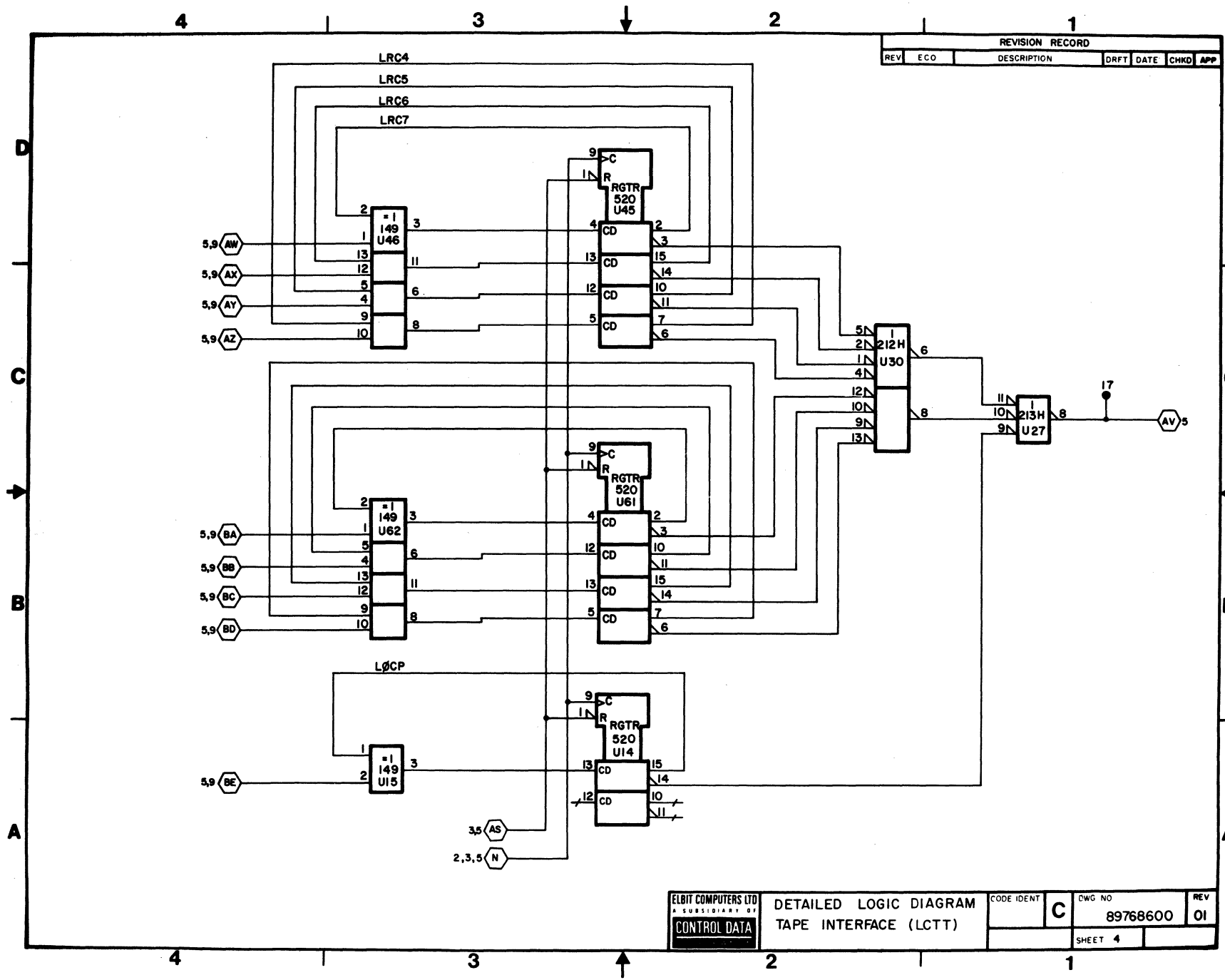
The LRCC is checked by the MTTC during each motion.

These checks are described in Table 5-6.

TABLE 5-6. LRC CHECKS

SIGNAL	CRCC	LRCC	VERT. PAR.
WRITE MØTIØN	Generated by MTTC No checking	Generated by transport Checked by controller	Generated and checked by MTTC
READ MØTIØN	Checked by MTTC	Checked by MTTC	Checked by MTTC
WRITE FM	None	Generated by transport Checked by MTTC.	Generated and checked by MTTC *
READ FM	None	Checked by MTTC	Checked by MTTC *

* In nine track, 800 BPI the MTTC indicates a legal Vertical Parity Error.



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

PARITY ERROR/FILL/FM DETECTOR (Logic Diagram 89648200, sheet 4)

Parity Error

U31 and U15-11 detect the Vertical Parity of the data from the tape, according to Table 5-7. Data Strobe strobes the parity into VPE (Vertical Parity Error) (U10-15) and after this is set, it can be reset only by Clear A. Also $\overline{\text{PEPARER}}$ sets VPE.

TABLE 5-7. PARITY STATE

	Binary	BCD
Vert.Par.	Even	Odd

PAR.ERR Status(U52-8)=(LRCError+CRC ERR) EØP+VPE

Fill

U10-11 is the Fill FF that toggles if A/D is high and is not changed otherwise. The toggling signal is RDS* (RDS for NRZI data only).

File Mark Detector

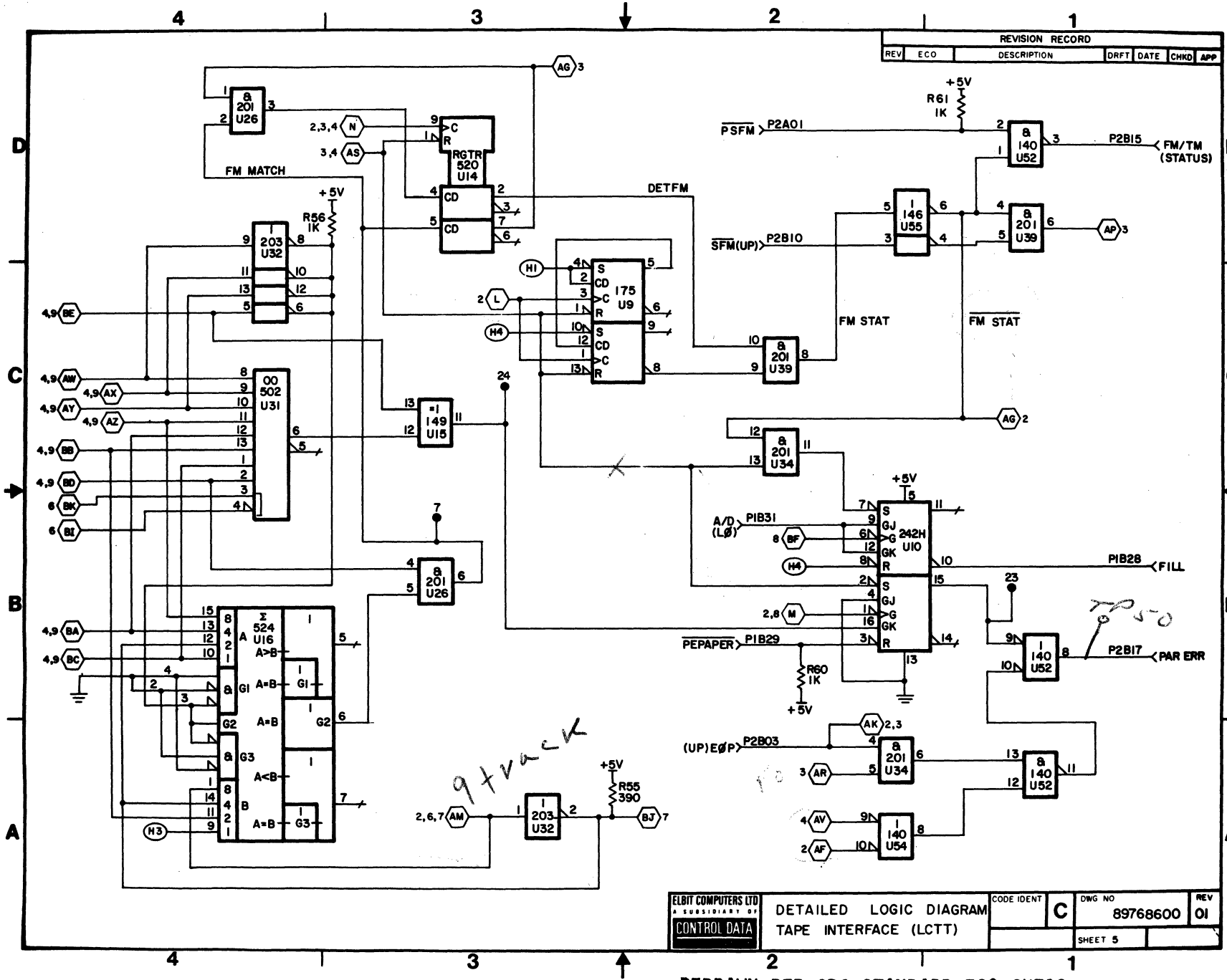
U32, U16, U26/6 compare the incoming character and the FM code according to 9T and produce FM Match is high if FM/TM is detected.

RDS* strobes FM Match into U14/7 if the next RDS* detects an FM MATCH, DET FM is set. U9 counts the number of Strobe Data's and if more than one is detected, $\overline{\text{CHAR2}}$ is low.

FM STAT = $\overline{\text{CHAR2}}$·DET FM

FM = PSFM+FM STAT

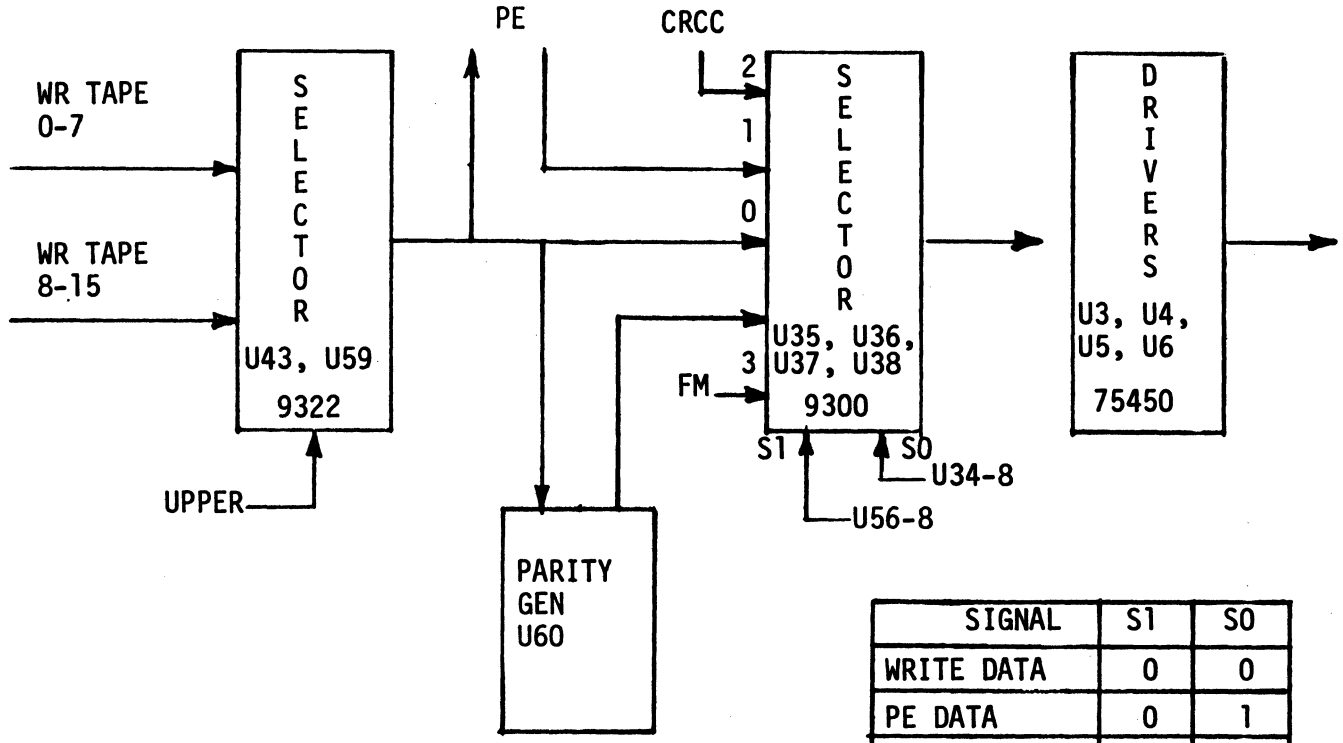
FM is the File Mark status



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

MTT/PE WRITE DATA PATH (Logic Diagram 89648200, sheets 5, 6, and 7)

This module receives a data word from the computer via the Double Buffer and sends it either to the tape or to the PE formatter. It contains also a One Of Four Selector that selects a Data Character, Phase Encoded Data, a File Mark or CRCC and sends it to the tape. Refer to Figure 5-23.



SIGNAL	S1	S0
WRITE DATA	0	0
PE DATA	0	1
CRCC	1	0
NRZI FM	1	1

Figure 5-23. MTT/PE Write Data Path

The computer word WRTape (0-15) is divided into U43, U59 by the Upper signal (assembly/disassembly). The two most significant bits are ANDed with nine tracks (U26). The six- or eight-bit character enters a parity generator (U60) and 7 or 9 bit character is created. This character is sent to the following units: PEWDIN (0-7), CRCC generator (selector U47, U63, U57-5), and Write To Tape Selector (U35, U36, U37 and U38).

This selector receives its data from:

1. NRZI data from the seven- or nine-bit character.

2. PE Data from the formatter (PWØut 0-7).

3. CRCC from the CRC Generator.

4. FM, i.e., DC wired and only bits 2, 3 and 4, depend on nine tracks for constants as shown in Table 5-7.

TABLES 5-7. FM CONSTANTS

TRACKS	7	6	5	4	3	2	1	0	P
9T	0	0	0	1	0	0	1	1	0
7T	0	0	0	0	1	1	1	1	0

Control of the Selector is according to the equations:

$$U34\text{-}8 = \overline{1600}\cdot(E\emptyset RS+WFM/TM)$$

$$U56\text{-}8 = 1600+WFM$$

$\overline{WDS}$ and $\overline{WReset}$ are generated according to:

$$\overline{WDS} = \overline{Write\ Clock\cdot(\overline{E\emptyset RS}+CRCC\ State\cdot\overline{WFM}/TM)} \quad (U20\text{-}11)$$

$$WReset = Write\ Clock\cdot LRCC\ State \quad (U20\text{-}8)$$

There is a PE-NRZI Selector (U18) that selects the Write Strobe (WDS), Write Reset (WReset), Write Parity bit (TTWDP), and RDS* according to 1600:

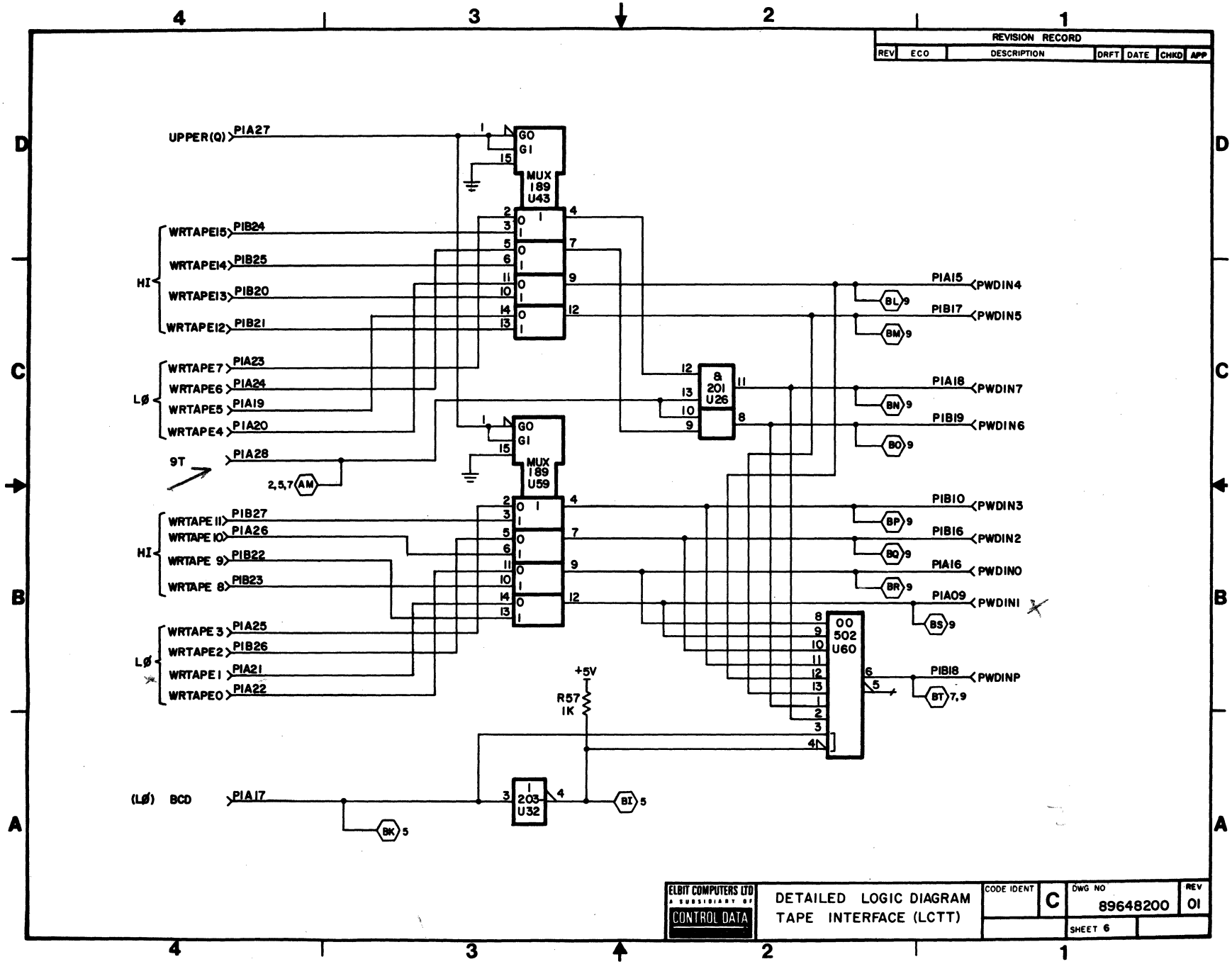
$$\overline{TTWDP} = 1600 \cdot PWOUT + \overline{1600}\ (\overline{U56\text{-}8} \cdot U34\text{-}8 \cdot CRCCP + \overline{U34\text{-}8} \cdot U60\text{-}6)$$

$$\overline{TTWDS} = 1600 \cdot PWCLK + \overline{1600} \cdot \overline{WDS}$$

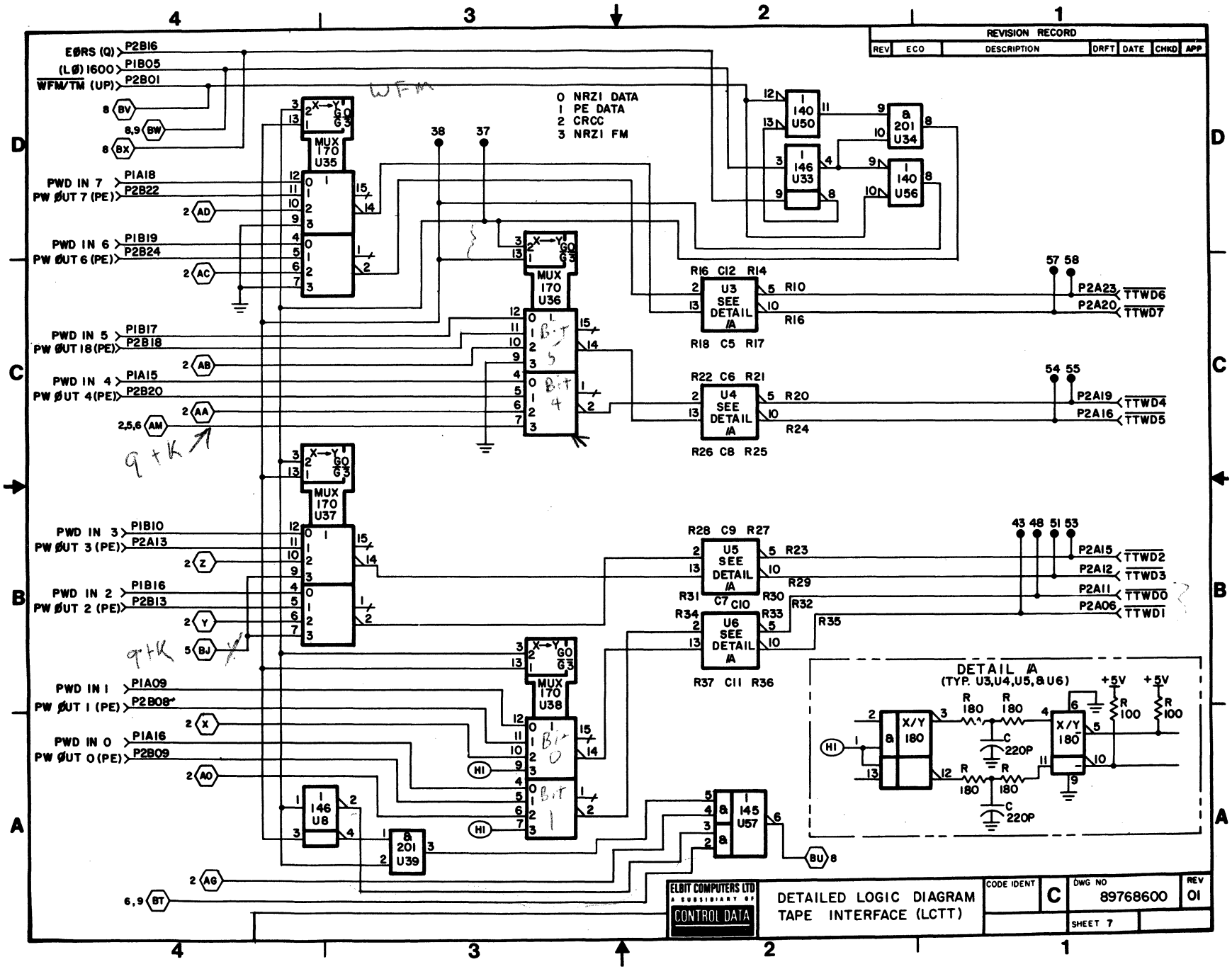
$$\overline{TTWReset} = 1600 \cdot PWReset + \overline{1600} \cdot \overline{WReset}$$

$$RDS^* = RMOT(1600 \cdot PRStrobe + \overline{1600} \cdot RDS)$$

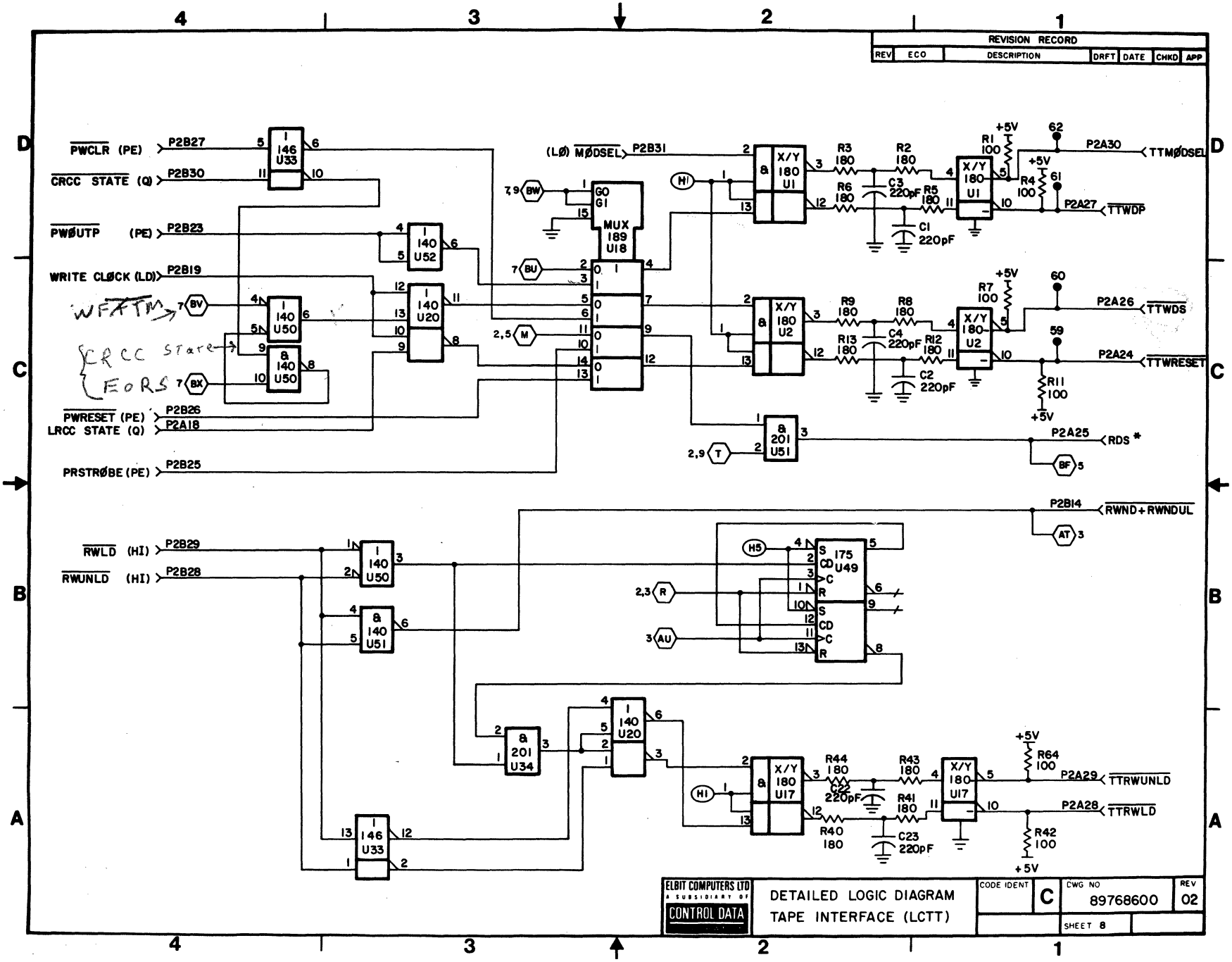
U1 through U6 are drivers to the tape transport.



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 03

MTT/PE READ DATA PATH AND REWIND TRANSMITTER (Logic Diagram 89648200, sheets 7 and 8)

This module includes the data path shown in Figure 5-24.

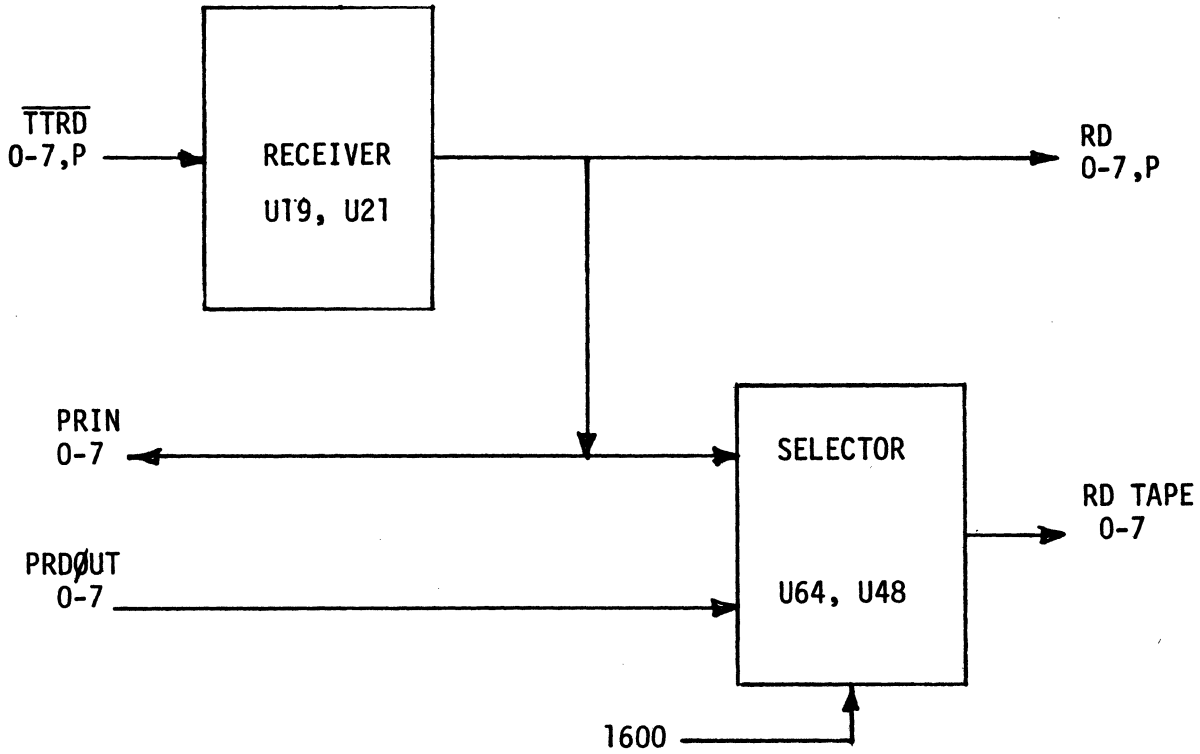
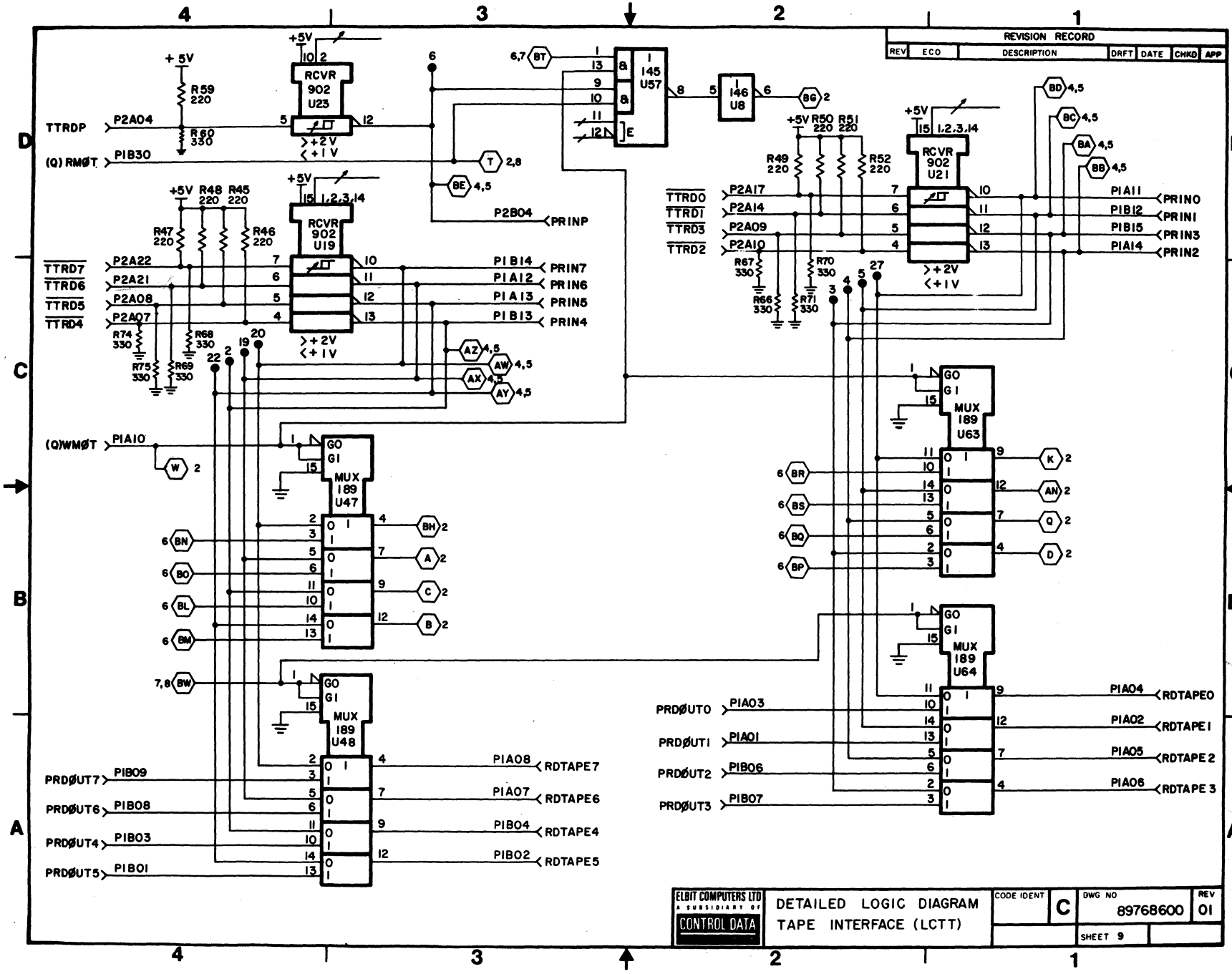


Figure 5-24. MTT/PE Read Data Path

The Rewind and Rewind Unload signals are differentiated at FF U49 by 2FWC and sent to the MTT through drivers U17-10 and U17-5.



REDRAWN PER CDC STANDARD-ECO CK798
SHEET IS REV 02

SECTION 6

MAINTENANCE

SCOPE

This section supplies maintenance references and procedures for the equipment listed in Section 1 of this manual.

The publications listed below are applicable to the equipment.

Publication	Pub. No.
1784 Computer Customer Engineering Manual	89633300
1784 Computer Reference Manual	89633400
1784 Site Preparation Manual	60158400
1700 Computer System Codes Manual	60163500
System Maintenance Monitor (SMM 17)	60182000

Tools and Special Equipment

The following is a list of maintenance tools recommended for this equipment.

Part Number	Part Description	Quantity
89688700	Board, Extender	1
89670300	Board, Extractor	1
	Oscilloscope, Tektronix 453 or Equivalent	1
	Voltmeter, Digital	1

Controller

Preventive maintenance of the controller is not required. After it is determined that the controller has failed, the PW assembly should be replaced with an identical trouble-free PWA. For removal and replacement of the controller, refer to Section 3 of this manual. After replacement, a diagnostic check should be run as described in SMM17.

CAUTION

Do not remove or replace controller, distribution panel or cables with system or external power supply power on.

SECTION 7

MAINTENANCE AIDS
(NOT REQUIRED)

SECTION 8

PARTS DATA

PARTS DATA

The following parts list is applicable to the FA446-A LCTT NRZI Magnetic Tape Transport Controller.

Nomenclature	Part Number
FA446-A Printed Wiring Assemblies	
Upper Data Assembly	89767500
Lower Data Assembly	89767800
Tape Interface Assembly	89768400
Q Channel Assembly	89768100
Interrupt Cable Assembly	89724702
Internal Cable Assembly	89700200
External Cable Assembly	
108-inches	89775501
240-inches	89775500

SECTION 9

WIRE LIST

WIRE LIST

The included wire list is applicable to the FA446-A LCTT NRZI Magnetic Tape Transport Controller.

The pin lists for each PWB are also included in this section.

DWN.	RACHEL S.	5.13.74
CHKD.	HAIM I.	5.13.74
ENG.	S. Coleman	3/77
MFG.		
APPR.		

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA CORPORATION
CODE IDENT

TITLE WIRING LIST
FOR EXTERNAL CABLE ASSY
(LCTT)

PREFIX: W.L.

DOCUMENT No.: 89805300

REV.: 02

FIRST USED ON: FA 446-A

SHEET 1 OF 7

SHEET REVISION STATUS

1	2	3	4	5	6	7
01	01	01	01	01	01	01
02	02	02	02	02	02	02

REVISION RECORD

REV.	ECO	DESCRIPTION	DRFT.	DATE	APP.
01	CK690	RELEASED CLASS B	Rachel	MAY. 13	J.C.
02	CK 751	TAB ADDED TO ASSY & AWG WAS 22	Inga	6 June 74	[illegible]

NOTES:

DETACHED LISTS

TABLE 9-1. EXTERNAL CABLE WIRE LIST

TABLE 9-1. EXTERNAL CABLE WIRE LIST (CONT'D)

ELBIT COMPUTERS LTD A SUBSIDIARY OF [redacted]		CODE IDENT.	SHEET 2	WL	DOCUMENT No. 89805300	REV. 01

PAIR ~~CONDUCTOR~~ IDENT.	FIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	CONTINENTAL ORIGIN		ACCESS FIND No.	ELCO DESTINATION		ACCESS FIND No.	REMARKS
1	5	24	WHT	SEE ASSY. DWG.	3	TAPE	1,2	2	J3	12	READ DATA STROBE
			BLK		4			B			GND
2			ORN		5			1			READ DATA PARITY
			BLK		6			A	J3		GND
3			RED		9			U	J2		WRITE DATA 6
			BLK		10			17	J2		GND
4			YEL		11			9	J3		READ DATA 3
			BLK		12			K			GND
5			BRN		13			8			READ DATA 2
			BLK		14			J			GND
6			BLU		15			14			READ DATA 4
			BLK		16			R			GND
7			GRN		17			15			READ DATA 5
			BLK		18			S	J3		GND
8			VIO		19			V	J2		WRITE DATA 7
			BLK		20			18			GND
9			ORN		21			S			WRITE DATA 4
			WHT					15	J2		GND
10			RED		25			17	J3		READ DATA 6
			WHT		26			U	J3		GND

TABLE 9-1. EXTERNAL CABLE WIRE LIST (CONT'D)

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

CODE IDENT. | SHEET 3 | WL | DOCUMENT No. 89805300 | REV. 02

~~PAIR CONDUCTOR~~ IDENT.	FIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	CONTINENTAL ORIGIN		ACCESS FIND No.	ELCO DESTINATION		ACCESS FIND No.	REMARKS
11	5	24	YEL	SEE ASSY. DWG.	27	TAPE	1,2	T	J2	12	WRITE DATA 5
			WHT		28			16	J2		GND
12			BRN		29			P	J3		READ DATA 2
			WHT		30			13			GND
13			BLU		31			18			READ DATA 7
			WHT		32			V	J3		GND
14			GRN		35			R	J2		WRITE DATA 3
			WHT		36			14			GND
15			VIO		37			M			WRITE DATA 0
			WHT		38			11	J2		GND
16			ORN		39			4	J3		READ DATA 1 *
			BLU		40			D			GND
17			RED		41			3			READ DATA 0
			BLU		42			C	J3		GND
18			YEL		43			M	J2		WRITE DATA 1
			BLU		44			12			GND
19			BRN		45			C			WRITE AMPLIFIER RESET
			BLU		46			3			GND
20			GRN		49			A			WRITE DATA STROBE
			BLU		50			1	J2		GND

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

CODE IDENT. | SHEET 4 | WL | DOCUMENT No. 89805300 | REV. 02

TABLE 9-1. EXTERNAL CABLE WIRE LIST (CONT'D)

~~PAIR CONDUCTOR~~ IDENT.	FIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	CONTINENTAL ORIGIN		ACCESS FIND No.	ELCO DESTINATION		ACCESS FIND No.	REMARKS
21	5	24	VIO	SEE ASSY. DWG.	51	TAPE	1,2	L	J2	12	WRITE DATA PARITY
			BLU		52			10	J2		GND
22			GRN		53			H	J1		REWIND COMMAND
			RED		54			7			GND
23			YEL		57			D			DATA DENSITY SELECT
			RED		58			4	J1		GND
24			BRN		59			F	J2		READ THRESHOLD
			RED		60			6	J2		GND
25			ORN		-			L	J1		SPARE
			RED		-			10			
26			VIO		-			N			
			RED		-			12	J1		
27			YEL		-			10	J3		
			GRN		-			L			
28			ORN		-			11			
			GRN		-			M	J3		SPARE
29			VIO		-			-			NOT USED
			GRN		-			-			
30			BRN		-			-			
			GRN		-			-			NOT USED

TABLE 9-1. EXTERNAL CABLE WIRE LIST (CONT'D)

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA		CODE IDENT.	SHEET 5	WL	DOCUMENT No. 89805300	REV. 02

PAIR CONDUCTOR IDENT.	FIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	CONTINENTAL ORIGIN		ACCESS FIND No.	ELCO DESTINATION		ACCESS FIND No.	REMARKS
31	5	24	V10	SEE ASSY. DWG.	—	TAPE	1,2	-		12	NOT USED
			BRN		-			-			
32			ORN		-			-			
			BRN		-			-			
33			YEL		-			-			
		24	BRN		-	TAPE		-			NOT USED
1	6	22	BRN	SEE ASSY. DWG.	3	UPPER	1,2	R	J1	12	LOAD POINT
			BLK		4			14			GND
2			RED		9			M			ON LINE
			BLK		10			11			GND
3			ORN		13			E			SYNC REVERSE COM
			BLK		14			5			GND
4			YEL		17			C			SYNC FWD COM
		22	BLK		18	UPPER		3	J1		GND

TABLE 9-1. EXTERNAL CABLE WIRE LIST (CONT'D)

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

CODE IDENT. | SHEET 6 | WL | DOCUMENT No. 89805300 | REV. 02

PAIR ~~CONDUCTOR~~ IDENT.	FIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	CONTINENTAL ORIGIN		ACCESS FIND No.	ELCO DESTINATION		ACCESS FIND No.	REMARKS
5	6	22	GRN	SEE ASSY. DWG.	19	UPPER	1,2	18	J1	12	SELECT 2
		↑	BLK		20	↑		8	↑		GND
6			BLU		21			A			SELECT 1
			BLK		22			8			GND
7			VIO		27			J			SELECT 0
			BLK		28			8			GND
8			GRY		29			P			FILE PROTECT
			BLK		30			13			GND
9			WHT		33			U			END OF TAPE
			BLK		34			17			GND
10			RED		37			K			SET WRITE STATUS
			BRN		38			9			GND
11			ORN		43			T			READY
			BRN		44			16			GND
12			YEL		45			F			DATA DENSITY IND
			BRN		46			6			GND
13			GRN		49			V			SELECT 3
			BRN		50			8			GND
14		↓	BLU		-	↓		S	↓		+5V SPARE } TWISTED PAIR
		22	BRN		-	UPPER		S	J1		+5V SPARE }

ET - 5103

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TABLE 9-1. EXTERNAL CABLE WIRE LIST (CONT'D)

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA		CODE IDENT.	SHEET 7	WL	DOCUMENT No. 89805300	REV. 02

~~CONDUCTOR~~ PAIR IDENT.	FIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	CONTINENTAL ORIGIN		ACCESS FIND No.	ELCO DESTINATION	ACCESS FIND No.	REMARKS
15	6	22	VIO	SEE ASSY. DWG.	-	UPPER	1,2	-	12	NOT USED
			BRN		-			-		
16			GRY		-			-		
			BRN		-			-		
17			WHT		-			-		
			BRN		-			-		
18			ORN		-			-		
			RED		-			-		
19			YEL		-			-		
		22	RED		-	UPPER		-		NOT USED

DWN.	SHIMLER M	AUG 19
CHKD.	HAIM IOSEF	AUG 19
ENG.	R. Tsfoni	AUG. 19
MFG.		
APPR.		

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA CORPORATION
CODE IDENT

TITLE WIRING LIST - FOR INTERNAL CABLE ASSEMBLY 89700200

PREFIX: WL

DOCUMENT No.: 89700300

REV.: 02

FIRST USED ON
FA442-A02 (NRZI TAPE CONTROLLER)
FA716-A02 (CARTRIDGE DISK CONTR.)

SHEET 1 OF 5

SHEET REVISION STATUS

1	2	3	4	5
01	01	01	01	01
02	02	02	02	02

REVISION RECORD

REV.	ECO	DESCRIPTION	DRFT.	DATE	APP.
01	CK128	RELEASED CLASS B	SM SHIMLER	AUG 19	Sokol 21 AUG
02	CK 311	REVISED	M	DEC. 3	A

NOTES:

PL89700200
DETACHED LISTS

TABLE 9-2. INTERNAL CABLE WIRE LIST

TABLE 9-2. INTERNAL CABLE WIRE LIST (CONT'D)

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA		CODE IDENT.	SHEET 2	WL	DOCUMENT No. 89700300	REV. 02

CONDUCTOR IDENT.	FIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	ORIGIN		ACCESS FIND No.	CONTINENTAL-TYPE DESTINATION CONNECTOR	ACCESS FIND No.	REMARKS
1		AWG28	WHT-BLK.	(ASSY) SEE DWG	P2	A01		1		
2			BLK.			GND.		2		GND.
3			WHT.-BRN		P2	A02		3		
4			BLK			GND.		4		GND
5			WHT.-RED.		P2	A04		5		
6			BLK.			GND.		6		GND.
7			WHT.-ORN.		P2	A05		7		
8			BLK.		P2	A31		8		TERMINATOR POWER
9			WHT.-YEL		P2	A06		9		
10			BLK.			GND.		10		GND
11			WHT.-GRN.		P2	A07		11		
12			BLK.			GND.		12		GND
13			WHT.-BLU		P2	A08		13		
14			BLK.			GND.		14		GND
15			WHT.-VIO		P2	A09		15		
16			BLK.			GND.		16		GND
17			WHT.-GRA		P2	A10		17		
18			BLK.			GND.		18		GND
19			WHT.-BLK.		P2	A11		19		
20			BRN.			GND.		20		GND

TABLE 9-2. INTERNAL CABLE WIRE LIST (CONT'D)

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

CODE IDENT. | SHEET 3 | WL | DOCUMENT No. 89700300 | REV. 02

CONDUCTOR IDENT.	FIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	ORIGIN		ACCESS FIND No.	DESTINATION	ACCESS FIND No.	REMARKS
21		AWG 28	WHT.-BRN.	(ASSY) SEE DWG	P2	A12		21		
22			BRN.			GND.		22		GND
23			WHT.-RED		P2	A13		23		
24			BRN.			GND		24		GND
25			WHT.-ORN.		P2	A14		25		
26			BRN.			GND		26		GND
27			WHT.-YEL.		P2	A15		27		
28			BRN.			GND.		28		GND
29			WHT.-GRN.		P2	A16		29		
30			BRN.			GND.		30		GND
31			WHT.-BLU		P2	A17		31		
32			BRN.			GND.		32		GND
33			WHT.-VIO		P2	A18		33		
34			BRN.			GND.		34		GND
35			WHT.-GRA		P2	A19		35		
36			BRN.			GND.		36		GND
37			WHT. BLK		P2	A20		37		
38			RED			GND.		38		GND
39			WHT.-BRN.		P2	A21		39		
40			RED			GND.		40		GND

TABLE 9-2. INTERNAL CABLE WIRE LIST (CONT'D)

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA		CODE IDENT.	SHEET 4	WL	DOCUMENT No. 89700300	REV. 02

CONDUCTOR IDENT.	FIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	ORIGIN		ACCESS FIND No.	DESTINATION	ACCESS FIND No.	REMARKS
41		AWG.28	WHT.-RED	(ASSY) SEE DWG.	P2	A22		41		
42			RED			GND.		42		GND.
43			WHT.-ORN.		P2	A23		43		
44			RED.			GND.		44		GND.
45			WHT.-YEL.		P2	A24		45		
46			RED			GND.		46		GND.
47			WHT.-GRN.		P2	A25		47		
48			RED			GND.		48		GND.
49			WHT.-BLU		P2	A26		49		
50			RED			GND.		50		GND.
51			WHT.-VIO.		P2	A27		51		
52			RED			GND.		52		GND.
53			WHT.-GRA		P2	A28		53		
54			RED.			GND.		54		GND.
55			WHT.-BLK.		P2	A29		55		
56			ORN.			GND.		56		GND.
57			WHT.-BRN.		P2	A30		57		
58			ORN.			GND		58		GND.
59			WHT.-RED.		P2	B11		59		
60			ORN					60		GND.

TABLE 9-2. INTERNAL CABLE WIRE LIST (CONT'D)

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

CODE IDENT. | SHEET 5. | WL | DOCUMENT No. 89700300 | REV. 02

CONDUCTOR IDENT.	FIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	ORIGIN		ACCESS FIND No.	DESTINATION	ACCESS FIND No.	REMARKS
61		AWG28	WHT.-ORN.	LASSY SEE DWG.	P2	B12		61		
62			ORN.			GND.		62		GND.
63			WHT.-YEL.		P2	B23		63		
64			ORN.			GND.		64		GND.
65			WHT.-GRN.		P2	B24		65		
66			ORN.			GND.		66		GND.

TABLE 9-3. PIN LIST - Q CHANNEL - INPUT SIGNAL

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1	DSA PRØT FAULT	P1B1	
2		2	
3		3	
4		4	
5		5	ISTSP
6		6	A/D
7		7	$\overline{\text{TRANS}}$
8		8	
9	LAST WØRD	9	
10		10	WRITE CLØCK
11	EARLY WDS	11	
12	$\overline{\text{WDS SHIFTED}}$	12	$\overline{\text{PWRQ SHIFTED}}$
13		13	
14	$\overline{\text{DSA RESUME}}$	14	
15		15	
16		16	
17		17	
18		18	1600 BPI
19		19	$\overline{\text{RES2}}$
20		20	
21		21	
23		23	
24		24	WFM/TM
25		25	
26		26	
27	(T1)RDS	27	$\overline{\text{STØP}}$
28	PWRQ(PE)	28	
29		29	$\overline{\text{A/Q READ}}$
30	$\overline{\text{9T}}$	30	$\overline{\text{A/Q WRITE}}$
31		31	
32		32	
33		33	
P1A34		P1B34	

(Cont.)

TABLE 9-3. PIN LIST - Q CHANNEL - INPUT SIGNAL (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1		P2B1	A/Q Q1
2		2	$\overline{MC}$
3		3	
4	LEGMF	4	
5		5	$\overline{RMØT}$
6	CØNTACT	6	$\overline{WMØT}$
7	LEGCF	7	A7
8	EØP	8	
9		9	
10		10	BUSY
11		11	
12	LEGUS	12	$\overline{A8}\cdot\overline{A9}\cdot\overline{A10}$
13	READY	13	
14		14	
15		15	PRØTECTED
16		16	INT
17	FM/TM STATUS	17	GC128
18		18	$\overline{REST}$
19	$\overline{A/Q\ PRØTECT}$	19	
20		20	
21		21	
22		22	
23		23	
24		24	
25		25	SCAN FØR IN
26		26	
27		27	STPCLK
28	EXT CLK	28	SCAN REV ØUT
29		29	
30		30	
31		31	A/Q Q0
32		32	
33		33	
P2A34		P2B34	

TABLE 9-4. PIN LIST - Q CHANNEL - OUTPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1		P1B1	STORAGE PARERR
2	PRØTECT FAULT	2	
3	DATA	3	$\overline{\text{UPPxT}}$
4	$\overline{\text{LØWXT}}$	4	LØST DATA
5	$\overline{\text{CLRLØWER}}$	5	
6	UPPER	6	
7		7	$\overline{\text{TRANS}}$
8		8	$\overline{\text{INCCA}}$
9		9	$\overline{\text{BUF 2FULL}}\cdot\text{WMØT}$
10	$\overline{\text{LØCKØUT}}$	10	
11		11	
12		12	
13	$\overline{\text{STWCRC}}$	13	TTBUSY
14		14	
15		15	
16	$\overline{\text{LØST DATA}}$	16	AL1
17	$\overline{\text{REQ}}$	17	
18	SCAN IN	18	
19	$\overline{\text{DSA WRENABLE}}$	19	
20	$\overline{\text{DSA REQUEST}}$	20	$\overline{\text{BUF I/Ø}}$
21	$\overline{\text{STOP DISTANCE}}$	21	$\overline{\text{A/Q CHARINPUT}}$
22		22	$\overline{\text{DSA PRIØRITY}}$
23	$\overline{\text{DSAWREN}}$	23	
24		24	
25		25	
26	LRCC STATE	26	$\overline{\text{REST.T}}$
27		27	
28		28	$\overline{\text{ENA}}$
29		29	
30		30	
31	$\overline{\text{CRCC STATE}}$	31	
32		32	
33		33	
P1A34		P1B34	

(Cont.)

TABLE 9-4. PIN LIST - Q CHANNEL - OUTPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1	STRMF	P2B1	
2	$\overline{\text{CONTACT}}$	2	
3		3	USA
4		4	WMØT
5	RMØT	5	
6		6	
7		7	
8		8	
9	$\overline{\text{STRBUF}}$	9	STRINT
10	$\overline{\text{EØP}}$	10	
11	SEL A1	11	SEL A0
12		12	
13		13	STRCF
14	$\overline{\text{A/Q REJECT}}$	14	$\overline{\text{A/Q REPLY}}$
15	STRUS	15	
16	$\overline{\text{A/Q INTERRUPT}}$	16	
17		17	
18	$\overline{\text{DSA PRØTECT}}$	18	
19		19	$\overline{\text{LDLWA}}$
20		20	
21		21	
22	T2	22	
23		23	
24		24	
25		25	START
26	SCAN FOR ØUT	26	
27	SCAN REV IN	27	
28		28	
29	GATED CLOCK	29	T3
30	T1	30	T4
31		31	
32		32	
33		33	
P2A34		P2B34	

TABLE 9-5. PIN LIST - LOWER DATA SECTION-INPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1		P1B1	RD TAPE 3
2	$\overline{\text{LØWERX1}}$	2	RD TAPE 0
3	RD TAPE 1	3	$\overline{\text{TRANS}}$
4	RD TAPE 2	4	RD TAPE 7
5		5	
6	$\overline{\text{RMØT}}$	6	RD TAPE 4
7	RD TAPE 5	7	
8		8	
9		9	$\overline{\text{LDLWA}}$
10		10	
11		11	
12		12	
13		13	
14		14	$\overline{\text{BUF I/Ø}}$
15		15	
16		16	
17		17	
18		18	$\overline{\text{INCCA}}$
19		19	
20		20	
21		21	
22		22	$\overline{\text{BUF}}$
23		23	
24		24	
25	SEL A0	25	
26		26	
27	SEL A1	27	
28		28	BUSY
29		29	
30	$\overline{\text{EØG}}$	30	
31		31	
32		32	
33		33	
P1A34		P1B34	

(Cont.)

TABLE 9-5. PIN LIST - LOWER DATA SECTION - INPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1	$\overline{\text{CØNTACT}}$	P2B1	BØT
2	CLRLØWER	2	
3		3	ILLUSCØPE
4		4	STRCF
5	$\overline{\text{WREQUEST}}$	5	
6		6	PE START
7	STRUS	7	$\overline{\text{PC 1600}}$
8	WENABLE	8	$\overline{\text{PE WARNING}}$
9		9	
10	STRINT	10	
11		11	$\overline{\text{A/Q MC}}$
12	LØST DATA	12	T3
13	EØP	13	
14		14	(Q)DATA
15		15	STRINT
16		16	
17		17	$\overline{\text{REQ}}$
18	PARITY ERR	18	FM/TM (T1)
19		19	$\overline{\text{TTDS}}$
20		20	$\overline{\text{ENA}}$
21	$\overline{\text{AL2}}$	21	
22	$\overline{\text{RWLD+RWUNLD}}$	22	$\overline{\text{AL1}}$
23	$\overline{\text{LØST DATA}}$	23	$\overline{\text{EØT}}$ (UP)
24		24	T1
25		25	
26		26	$\overline{\text{RWLD}}$
27	VS1	27	VS0
28	$\overline{\text{RES2}}$	28	
29		29	KUTY1
30		30	PE LØST DATA
31		31	
32		32	
33		33	
P2A34		P2B34	

TABLE 9-6. PIN LIST - LOWER DATA SECTION - OUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1		P1B1	
2	DSA ADDR 1	2	
3		3	
4	DSA ADDR 6	4	
5	DSA ADDR 2	5	DSA ADDR 0
6		6	
7		7	
8	WRTAPE 0	8	DSA ADDR 4
9		9	
10	DSA DATA 1	10	DSA DATA 2
11	WR TAPE 3	11	
12	DSA DATA 0	12	DSA DATA 3
13	A=B	13	DSA DATA 5
14	WRTAPE 5	14	
15		15	DSA DATA 4
16		16	WRTAPE 4
17	WRTAPE 6	17	
18		18	A7
19	$\overline{\text{A/Q A6}}$	19	$\overline{\text{A/Q A5}}$
20	$\overline{\text{A/Q A4}}$	20	$\overline{\text{A/Q A7}}$
21	$\overline{\text{A/Q A2}}$	21	$\overline{\text{A/Q A3}}$
22	WRTAPE 1	22	
23		23	DSA ADDR 3
24	WRTAPE 7	24	$\overline{\text{9T}}$
25		25	DSA ADDR 7
26	DSA ADDR 5	26	ALARM
27	WRTAPE 2	27	
28		28	
29		29	$\overline{\text{A/Q A0}}$
30	$\overline{\text{A/Q A1}}$	30	
31	PEENABLE	31	
32		32	
33		33	
P1A34		P1B34	

(Cont.)

TABLE 9-6. PIN LIST - LOWER DATA SECTION - OUTPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1		P2B1	
2		2	LEGUS
3		3	
4	800 BPI	4	
5		5	1600 BPI
6	WRITE CLK	6	
7		7	
8		8	
9	$\overline{\text{MC}}$	9	WDSHIFTED
10		10	EARLY WDS
11	$\overline{\text{RES T}}$	11	
12		12	2FCW
13		13	A/D
14	BCD	14	
15	$\overline{\text{MØDSEL}}$	15	INTERRUPT
16		16	
17	$\overline{\text{READY RWLD}}$	17	
18		18	
19		19	
20		20	
21		21	
22		22	
23		23	
24		24	
25	PRØTECTED	25	GAPCLK
26	9T	26	
27		27	
28		28	TT READY
29	PE CHARCLK	29	
30	PE CLØCK	30	
31		31	PE ENABLE
32		32	
33		33	
P2A34	75 IPS	P2B34	

TABLE 9-7. PIN LIST - TAPE INTERFACE - INPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1	PRDØUT 1	P1B1	PRDØUT 5
2		2	
3	PRDØUT 0	3	PRDØUT 4
4		4	
5		5	(LØ)1600
6		6	PRDØUT 2
7		7	PRDØUT 3
8		8	PRDØUT 6
9		9	PRDØUT 7
10	WMØT	10	
11		11	
12		12	
13		13	
14		14	
15		15	
16	PWDIN 0	16	
17	BCD	17	
18		18	PWDINP
19	WRTAPE 5	19	
20	WRTAPE 4	20	WRTAPE 13
21	WRTAPE 1	21	WRTAPE 12
22	WRTAPE 0	22	WRTAPE 9
23	WRTAPE 7	23	WRTAPE 8
24	WRTAPE 6	24	WRTAPE 15
25		25	WRTAPE 14
26	WRTAPE 10	26	WRTAPE 2
27		27	WRTAPE 11
28	9T	28	
29		29	$\overline{\text{PE PAR ER}}$
30	2FWC	30	RMØT
31	$\overline{\text{RES2}}$	31	A/D
32		32	
33		33	
P1A34		P1B34	

(Cont.)

TABLE 9-7. PIN LIST - TAPE INTERFACE - INPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1	$\overline{\text{PSFM}}$	P2B1	$\overline{\text{WFM/TM(UP)}}$
2	$\overline{\text{TTRDS}}$	2	$\overline{\text{REV}}$
3		3	EØP
4	TTRDP	4	
5	$\overline{\text{STWCRC}}$(Q)	5	GATED CLOCK
6		6	
7	$\overline{\text{TTRD4}}$	7	
8	$\overline{\text{TTRD5}}$	8	PWØUT1(PE)
9	$\overline{\text{TTRD3}}$	9	PWØUTO(PE)
10	$\overline{\text{TTRD2}}$	10	$\overline{\text{SFM}}$(UP)
11		11	
12		12	
13	PWØUT 2(PE)	13	PWØUT 2(PE)
14	$\overline{\text{TTRD1}}$	14	
15		15	
16		16	EØRS
17	TTRDO	17	
18	LRCC STATE(Q)	18	PWØUT 18(PE)
19		19	WRITE CLOCK
20		20	PWØUT 4(PE)
21	$\overline{\text{TTRD6}}$	21	
22	$\overline{\text{TTRD7}}$	22	PWØUT 7(PE)
23		23	$\overline{\text{PWØUTP}}$(PE)
24		24	PWØUT 6(PE)
25		25	PRSTRØBE(PE)
26		26	$\overline{\text{PWRESET}}$(PE)
27		27	$\overline{\text{PWCLR}}$(PE)
28		28	$\overline{\text{RWUNLD}}$
29		29	$\overline{\text{RWLD}}$
30		30	$\overline{\text{CRCC STATE}}$(Q)
31		31	$\overline{\text{MØDSEL}}$
32		32	
33		33	
P2A34		P2B34	

TABLE 9-8. PIN LIST - TAPE INTERFACE - OUTPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1	RDTAPE1	P1B1	
2		2	RDTAPE 5
3		3	
4	RDTAPE 0	4	RDTAPE 4
5	RDTAPE 2	5	
6	RDTAPE 3	6	
7	RDTAPE 6	7	
8	RDTAPE 7	8	
9	PWDIN 1	9	
10		10	PWDIN 3
11	PRIN 0	11	
12	PRIN 6	12	PRIN 1
13	PRIN 5	13	PRIN 4
14	PRIN 2	14	PRIN 7
15	PWDIN 4	15	PRIN 3
16	PWDIN 0	16	PWDIN 2
17		17	PWDIN 5
18	PWDIN 7	18	PWDIN P
19		19	PWDIN 6
20		20	
21		21	
22		22	
23		23	
24		24	
25		25	
26		26	
27		27	
28		28	FILL
29		29	
30		30	
P1A31		P1B31	
32		32	
33		33	
P1A34		P1B34	

(Cont.)

TABLE 9-8. PIN LIST - TAPE INTERFACE - OUTPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1		P2B1	
2		2	
3		3	
4		4	
5		5	
6	$\overline{\text{TTWD1}}$	6	
7		7	$\overline{\text{SEØP}}$
8		8	
9		9	
10		10	
11	$\overline{\text{TTWD0}}$	11	
12	$\overline{\text{TTWD3}}$	12	ISTSP
13		13	
14		14	$\overline{\text{RWND + RWNDUL}}$
15	$\overline{\text{TTWD2}}$	15	FM/TM(STATUS)
16	$\overline{\text{TTWD5}}$	16	
17		17	PARERR
18		18	
19	$\overline{\text{TTWD4}}$	19	
20	$\overline{\text{TTWD7}}$	20	
21		21	
22		22	
23	$\overline{\text{TTWD6}}$	23	
24	$\overline{\text{TTWRESET}}$	24	
25	RDS	25	
26	$\overline{\text{TTWDS}}$	26	
27	$\overline{\text{TTWDP}}$	27	
28		28	
29		29	
30	TTMØDSEL	30	
31		31	
32		32	
33		33	
P2A34		P2B34	

TABLE 9-9. PIN LIST - UPPER DATA SECTION - INPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1	RD TAPE 3(T1)	P1B1	RD TAPE 2(T1)
2	RD TAPE 0(T1)	2	$\overline{\text{UPPXT}}$
3	$\overline{\text{TRANS}}$ (Q)	3	RD TAPE 1(T1)
4	RD TAPE 6(T1)	4	RD TAPE 7(T1)
5		5	
6	RD TAPE 4(T1)	6	
7	$\overline{\text{RES1.T}}$	7	RD TAPE 5(T1)
8		8	
9	$\overline{\text{LDLWA}}$	9	
10		10	
11		11	
12		12	
13		13	
14		14	$\overline{\text{BUF I/Ø}}$
15		15	
16		16	
17	$\overline{\text{CARCURADR}}$	17	A=B
18		18	
19		19	
20		20	
21	(Q)$\overline{\text{STRBUF}}$	21	
22		22	
23		23	(T1)PAPER
24		24	FM/TM(T1)
25	(Q)SEL A0	25	
26		26	
27	(Q)SEL A1	27	
28		28	
29		29	
30		30	
31	(Q)STRUS	31	
32		32	
33		33	
P1A34		P1B34	

(Cont.)

TABLE 9-9. PIN LIST - UPPER DATA SECTION - INPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1	PE EØP	P2B1	
2	TT BØT	2	
3		3	(T1)FILL
4		4	
5		5	
6		6	
7	BUSY	7	(Q)STRMF
8		8	A7
9	(Q)USA	9	
10		10	
11		11	
12		12	A/D
13	PRØTECT FAULT(Q)	13	STORAGE PARITY ERROR
14	(Q)LØCKØUT	14	(PE) ID ABØRT
15		15	
16	FILE PRØTECT	16	
17		17	TT BUSY
18	TT EØT	18	
19	T3(Q)	19	
20		20	
21	9T	21	
22		22	
23		23	
24		24	
25		25	
26		26	
27		27	
28	TT READY	28	GAP CLØCK
29	(Q) REQ	29	ENA
30		30	DSAWRBII(Q)
31		31	STØP DISTANCE
32		32	
33		33	
P2A34		P2B34	

TABLE 9-10. PIN LIST - UPPER DATA SECTION - OUTPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1		P1B1	
2		2	
3		3	
4		4	
5	DSA ADDR 8	5	DSA ADDR 10
6		6	
7		7	
8	DSA ADDR 12	8	WR TAPE 8
9		9	DSA ADDR 14
10	DSA DATA 10	10	DSA DATA 9
11	WR TAPE 11	11	
12	DSA DATA 11	12	DSA DATA 8
13	WR TAPE 13	13	LAST WØRD
14	DSA DATA 15	14	
15	DSA DATA 14	15	DSA DATA 12
16	WR TAPE 14	16	WR TAPE 12
17		17	
18	$\overline{\text{A/Q A13}}$	18	$\overline{\text{A/Q A14}}$
19	$\overline{\text{A/Q A15}}$	19	$\overline{\text{A/Q A12}}$
20	$\overline{\text{A/Q A11}}$	20	$\overline{\text{A/Q A10}}$
21		21	WR TAPE 9
22	DSA ADDR 9	22	$\overline{\text{A/Q A9}}$
23	DSA ADDR 11	23	
24	WR TAPE 15	24	
25		25	DSA ADDR 15
26	DSA ADDR 13	26	DSA DATA 13
27		27	WR TAPE 10
28	CØNTACT	28	EØT
29		29	$\overline{\text{A/Q A8}}$
30	WENABLE	30	ILLUSCØDE
31		31	
32		32	
33		33	
P1A 34		P1B 34	

(Cont.)