89723800

CONTROL DATA CORPORATION

CONTROL DATA®
SYSTEM 17
AB107/AB108 COMPUTER

EXECUTION CHARTS

REVISION RECORD

REVISION	DESCRIPTION
01	Released Class B, ECO No. CK539
(03.21.74)	
02	Minor publication changes ECO CK937
(08.28.74)	
A	Released Class A ECO CK 1322
(23.9.75)	

Publication No.
89723800

Address comments concerning this manual to:
Control Data Corporation
Publications and Graphics Division
4455 Eastgate Mall
La Jolla, California 92037
or use Comment Sheet in the back of this manual.

Preface

These charts are intended for a user who is familiar with the programming and functional working of the central processing unit of the CONTROL DATA® AB107/AB108 computer. It is recommended that this document be used in conjunction with the 1784 Computer Reference Manual (89633400) and Customer Engineering Manual (89633300). A brief introduction and explanation is given to the charts.

Contents

AB107/AB108 COMPUTER EXECUTION CHARTS

Introduction

The AB107/AB108 Computer Execution Charts are divided into three groups. The first group describes the calculation of the effective address during memory reference instructions. The second group describes the execution of memory reference instructions themselves. The third group describes the execution of all other instructions plus the enter, sweep, and interrupt sequences. Each execution chart has basically the same format. Each is labeled with the type of instruction it represents along with the corresponding instruction code.

All addressing sequences apply when the F field of the instruction register does not equal zero (memory reference instructions). The Fl field defines the type of addressing, and the Delta (Δ) field may equal zero for one class of addressing or not equal zero for another class. This gives 32 different modes of addressing and 15 different types of memory reference instructions.

When the F field equals zero, the instruction is defined by the contents of the Fl field. This gives 16 different instructions. The enter and sweep sequences are performed through the Programmer's Console switches. The interrupt sequence is initiated by special interrupt logic circuits.

The Execution Charts describe the major activities occurring in the computer during each Central Processing Unit (CPU) cycle. Each division in the horizontal direction shows one CPU cycle. The status of the action during that cycle is shown in the vertical direction.

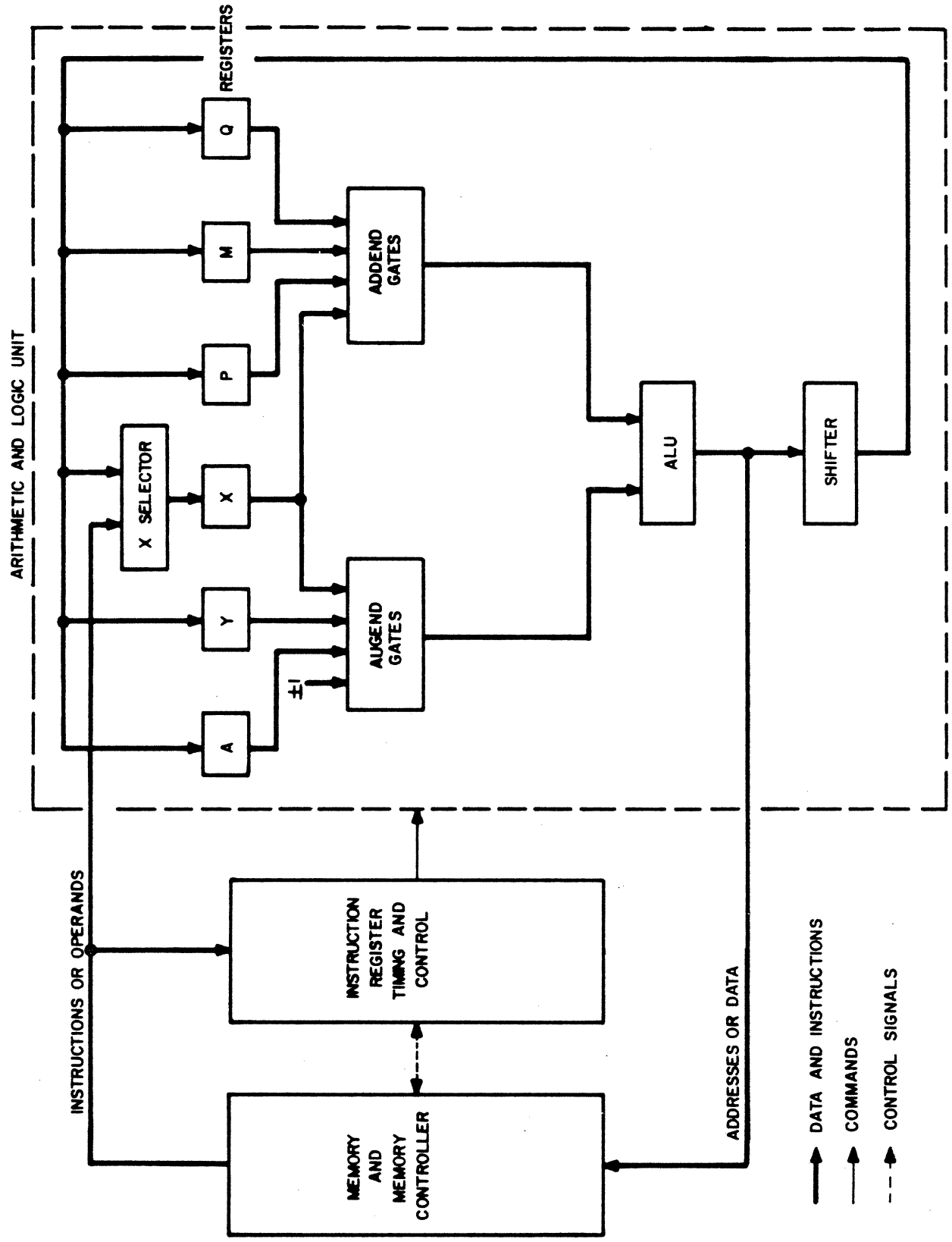
The "State" row refers to the state flip-flops on the "Timing" printed wiring assembly which is active during that cycle. Each instruction begins with the Read Next Instruction (RNI) state active. If additional cycles are needed to calculate the Effective Address (EA), the ADR state becomes active. During the execution of the instruction the Operand 1 (ØP) or Operand 2 (ØP2) states may be active. Every instruction ends with an RNI cycle. There are additional main states such as ITR which is used during shifts, MDS and MDS1 used in multiply/divide, and ENI and ENI2 used in interrupt.

The "Even/Odd/Odd2" row shows which of the EVEN/ODD/ODD2 flip-flops is active. In general, the state will be active for an even number of (Even/Odd) cycles. For example; the RNI state always starts during an even cycle and ends after an odd cycle. The Even/Odd state usually changes every CPU cycle, however, the odd state may sometimes last for two cycles; in which case the second cycle is called ØDD2.

The counter is used during some addressing sequences and during shift and multiply/divide instructions. It is loaded at the beginning of the sequence and counts down to zero.

During each CPU cycle, a data path is established through the Arithmetic and Logic Unit (ALU). This data path usually includes one or two of the six active registers. At the end of a cycle, some registers may be clocked to change their contents.

A memory cycle may be initiated only during an odd CPU cycle. The first data available on the ALU lines,(at the end of the CPU cycle) is usually used as the address for the memory reference. In the subsequent CPU cycle, in the case of a memory read cycle, the data read from the memory is available at the input of the X selector. In a memory write cycle, the data on the ALU lines is written into the memory during the next even CPU cycle. See the following schematic for general description of the Arithmetic and Logic Unit and Data paths.



Schematic of Arithmetic and Logic Unit and Data Paths.

In the execution charts, the labels "Addend Gates" and "Augend Gates" refer to the register, if any, which is gated through the Addend and Augend Gates. The Q, M, P, or X registers may be gated through the Addend gates while the A, Y or X registers or ±1, X_L, X_{SE}, or ∇ may be gated through the Augend gates.

X_L means the delta field with the eight upper bits equal to zero.

X_{SE} means the delta field sign extended.

∇ means the four lower bits of the X register with the 12 upper bits equal to zero.

The ALU control label indicates what function is being performed on the Addend and Augend at the ALU. The function may be: Augend inversion ($\overline{AUG}$); Addend inversion ($\overline{ADD}$); Adding, Augend and Addend (+); Subtracting, Augend minus Addend (-); Logical Product, Augend·Addend (LP); Exclusive-OR (⊕); Inverted Logical Product (NAND); or Inverted Exclusive-OR ($\overline{\oplus}$).

The shifter control label indicates what operation is performed in the shifter. D means the ALU data appears inverted at the output of the shifter. LR1 and LR2 refer to the two steps of a long right shift, used in the multiply and shift instructions, during which the ALU data is shifted one place to the right at the shifter output. LL1D and LL2 refer to the two steps of a long left shift used in the divide instruction. This differs slightly from the long left shift (LL1C) used in shift instructions.

TAQ1 refers to data which appears on the A/Q channel.

TA refers to the interrupt trap address.

A "1" appearing at the "Memory Request" label indicates that a memory reference cycle is initiated during that CPU cycle. During the following CPU cycle a "1" at the "Write" label indicates that data is written into the memory, otherwise it is assumed that data is read from the memory. The label "ALU → Z" shows when data is transferred from the ALU to the memory during a memory write cycle.

Label "XSEL" indicates the status of the X register selector. The symbol "Z" indicates that memory data appears at the input of the X register. The symbol "SH" indicates that the output of the shifter appears at the input of the X register.

The labels SH→Y, XSEL→X, SH→P, SH→M, SH→Q, and SH→A indicate whether the Y, X, P, M, Q and A registers, respectively, are clocked at the end of the cycle.

When EAD (Effective Address and End of Address) appears in "State" it refers to a signal which is always active during the last CPU cycle of addressing.

Read Index (RI) means that the memory cycle initiated during that CPU cycle will reference the index register at location $00FF_{16}$. In this special case the output of the ALU is not an address, and the RI signal produces the address $00FF_{16}$.

An Immediate Operand condition (IM.OP) occurs in read-operand-type instructions in three modes of addressing. In these cases, the Effective Address itself is used as the operand and the last ADR·ØDD cycle of addressing is followed by an ØP·ØDD2 cycle.

The symbol "1532" means that the computer is in 32K mode and the most significant bit (bit 15) of the X register is set.

The Bit Bucket (BB) is a flip-flop located on the "Decoder" printed wiring assembly. It is used during multiply or divide instructions to produce a correctly signed result. In multiplication it is loaded with X15 ⊕ A15 and in division it is loaded with X15 ⊕ Q15.

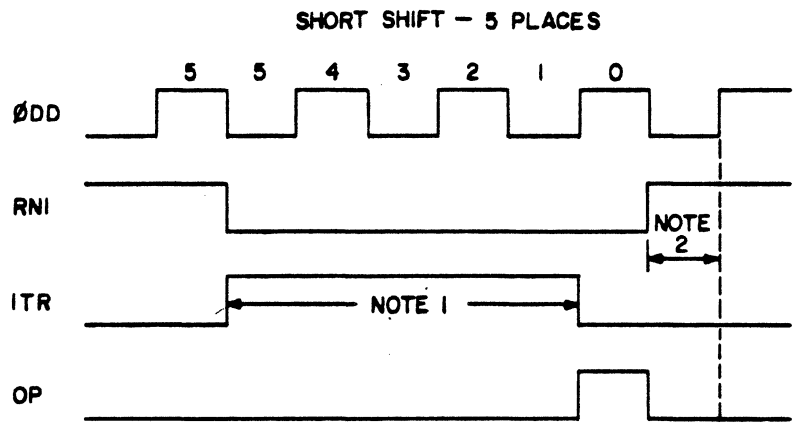
The symbols PRY and PEF appear in the SPA instruction. PRY=1 when the parity bit is equal to 1. PEF is true when the store operation is aborted.

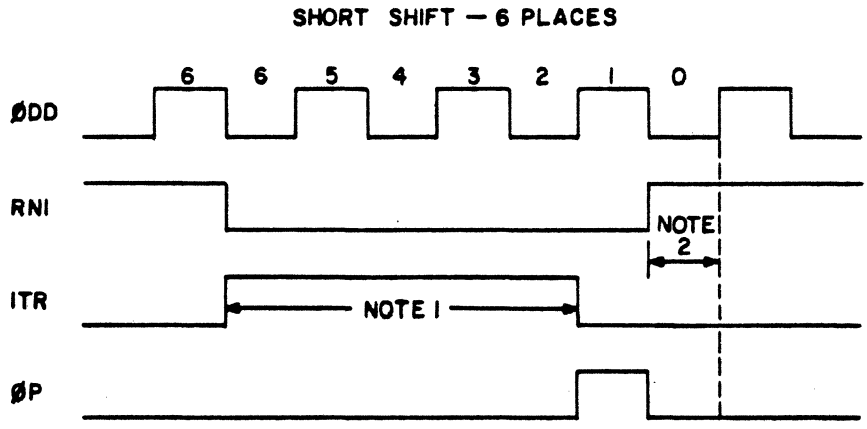
The signal FS is active in the first memory cycle after a Master Clear or P register clear.

The signal SKT is active during a skip instruction if the condition for a skip is met.

The shift instruction uses one of two possible timing schemes, depending on the signal SHI. SHI is active for any shift of zero places or a single shift of one place. The signal K0 is active for any shift of zero or one place. I0 through I7 are the eight least significant bits of the Instruction Register (IR).

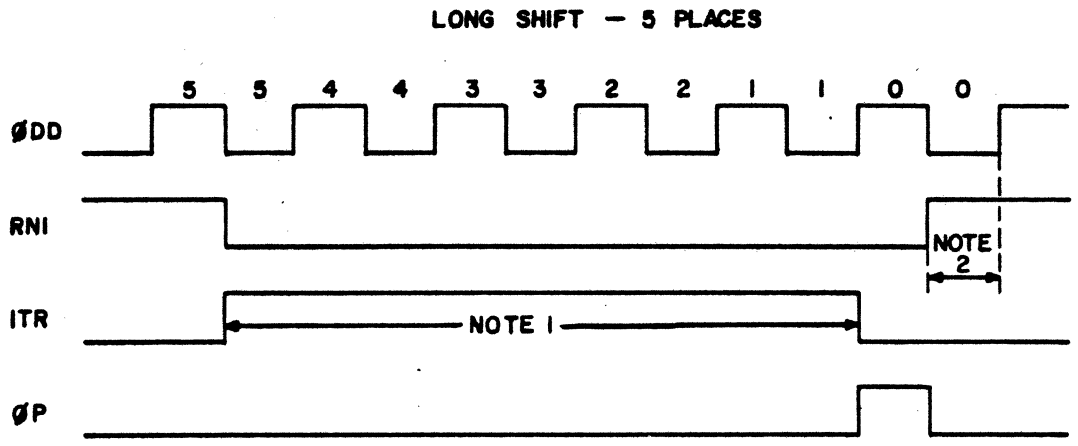
Timing for Shift Instructions





For notes refer to next page.

Timing for Shift Instruction



NOTES:

1. Q Shifted on condition

   [EVEN·15 + $\overline{16}$15]

   A Shifted on condition

   [ØDD·16 + $\overline{15}$16]

2. Q Shifted on condition

   [15$\overline{16}$·(One place or EVEN number of places]

   A Shifted on condition

   [$\overline{15}$16·(One place or EVEN number of places)
   + 1516·(One or more places)]

In the following order:

Fl = 0 $\quad \Delta \neq 0$

Fl = 0 $\quad \Delta = 0$

Fl = 1 $\quad \Delta \neq 0$

Fl = 1 $\quad \Delta = 0$

Fl = 2

:

Fl = F $\quad \Delta = 0$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=0, Δ≠0	REMARKS: E.A.=Δ	

Addend Gates															
Augend Gates	X_L														
A.L.U. Control	⊕														
SHIFTER Control	D														
Memory Request	1														
WRITE															
A.L.U. → Z															
SH → Y	1														
XSEL	SH														
XSEL → X	1														
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI (EAD)														
EVEN/ODD/ODD2	ODD														
Counter	0														

X_L = 00Δ, Delta not Sign Extended

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=0, Δ=0	REMARKS: E.A.=P+1	

Addend Gates	P														
Augend Gates	+1														
A.L.U. Control	+														
SHIFTER Control	D														
Memory Request	1														
WRITE															
A.L.U. → Z															
SH → Y	1														
XSEL	SH														
XSEL → X	1														
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RNI (EAD)														
EVEN/ODD/ODD2	ODD														
Counter	0														

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=1, Δ≠0	REMARKS: E.A.=Δ + (00FF)

Addend Gates		Q	X												
Augend Gates	X_L		Y												
A.L.U. Control	⊕	+	+												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1		1												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR (EAD)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter (decimal)	2	1	0												
RI (Read Index)	1														

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=1, Δ=0	REMARKS: E.A.=(P+1) + (00FF)	

Addend Gates	P		X	Q	X										
Augend Gates	+1				Y										
A.L.U. Control	+	⊕	⊕	+	+										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1*										
WRITE															
A.L.U. → Z															
SH → Y	1		1		1										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR	ADR	ADR (EAD)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2	1	0										
RI			1												

* upon $\overline{\text{Im.Op.}}$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=2, Δ≠0	REMARKS: E.A.=Δ + Q	

Addend Gates	Q														
Augend Gates	X_L														
A.L.U. Control	+														
SHIFTER Control	D														
Memory Request	1														
WRITE															
A.L.U. → Z															
SH → Y	1														
XSEL	SH														
XSEL → X	1														
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI (EAD)														
EVEN/ODD/EVEN2	ODD														
Counter	0														

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=2, Δ=0	REMARKS: E.A.=(P+1) + Q	

Addend Gates	P	Q	X											
Augend Gates	+1		Y											
A.L.U. Control	+	0	+											
SHIFTER Control	D	D	D											
Memory Request	1		1*											
WRITE														
A.L.U. → Z														
SH → Y	1	1	1											
XSEL	SH	Z	SH											
XSEL → X		1	1											
SH → P	1													
SH → M														
SH → Q														
SH → A														
State	RNI	ADR	ADR (EAD)											
EVEN/ODD/ODD2	ODD	EVEN	ODD											
Counter	2	1	0											

* Upon $\overline{\text{Im.Op.}}$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=3, Δ≠0	REMARKS: E.A.=Δ + Q + (00FF)

Addend Gates		Q	X												
Augend Gates	X_L	Y	Y												
A.L.U. Control	⊖	+	+												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1	1	1												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR (EAD)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter	2	1	0												
RI	1														

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=3, Δ=0	REMARKS: E.A.=(P+1) + Q + (00FF)	

Addend Gates	P		X	Q	X										
Augend Gates	+1			Y	Y										
A.L.U. Control	+	⊕	⊕	+	+										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1*										
WRITE															
A.L.U. → Z															
SH → Y	1		1	1	1										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RN1	ADR	ADR	ADR	ADR (EAD)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2	1	0										
RI			1												

* Upon $\overline{\text{Im.Op.}}$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=4, Δ≠0	REMARKS: E.A.=(Δ)

Addend Gates		Q	X												
Augend Gates	X_L	Y													
A.L.U. Control	⊕	+	⊕												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1		1*												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P															
SH → M															
SH → Q															
SH → A															
State	RN1	ADR	ADR (EAD*)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter	2	1	0												

* Upon T532

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=4, Δ=0	REMARKS: E.A.=(P+1)	

Addend Gates	P	Q	X												
Augend Gates	+1	Y													
A.L.U. Control	+	+	⊕												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1		1*												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR (EAD*)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter	2	1	0												

* Upon $\overline{T532}$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=5, Δ≠0	REMARKS: E.A.=(Δ) + (00FF)

Addend Gates			X	Q	X										
Augend Gates	X_L			Y	Y										
A.L.U. Control	⊕	⊕	⊕	+	+										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1										
WRITE															
A.L.U. → Z															
SH → Y	1		1		1										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR	ADR	ADR (EAD)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2*	1	0										
RI			$\overline{1532}$												

* Decrement to 1 only upon $\overline{1532} \cdot$ ODD

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=5, Δ=0	REMARKS: E.A.=(P+1) + (00FF)	

Addend Gates	P		X	Q	X										
Augend Gates	+1			Y	Y										
A.L.U. Control	+	⊕	⊕	+	+										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1										
WRITE															
A.L.U. → Z															
SH → Y	1		1		1										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RN1	ADR	ADR	ADR	ADR (EAD)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2*	1	0										
RI			$\overline{1532}$												

* Decrement to one only upon $\overline{1532} \cdot$ ODD

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=6, Δ≠0	REMARKS: E.A.=(Δ) + Q

Addend Gates		Q	X												
Augend Gates	X_L		Y*												
A.L.U. Control	0	0	+*/0*												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1	1	1*												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR (EAD*)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter	2	1	0												

* Upon $\overline{1532}$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=6, Δ=0	REMARKS: E.A.=(P+1) + Q	

Addend Gates	P	Q	X												
Augend Gates	+1		Y*												
A.L.U. Control	+	⊕	+*/⊕$\bar{*}$												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1	1	1*												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR (EAD*)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter	2	1	0												

* Upon $\overline{1532}$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=7, Δ≠0	REMARKS: E.A.=(Δ) + Q + (00FF)	

Addend Gates			X	Q	X										
Augend Gates	X_L			Y	Y										
A.L.U. Control	⊕	⊕	⊕	+	+										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1										
WRITE															
A.L.U. → Z															
SH → Y	1		1	1	1										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR	ADR	ADR (EAD)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2*	1	0										
RI			$\overline{1532}$												

* Decrement to 1 only upon $\overline{1532}$ ·ODD

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=7, Δ=0	REMARKS: E.A.=(P+1) + Q + (00FF)	

Addend Gates	P		X	Q	X										
Augend Gates	+1			Y	Y										
A.L.U. Control	+	⊕	⊕	+	+										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1										
WRITE															
A.L.U. → Z															
SH → Y	1		1	1	1										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RN1	ADR	ADR	ADR	ADR (EAD)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2*	1	0										
RI			$\overline{1532}$												

* Decrement to 1 only upon $\overline{T532}$·ODD

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=8, Δ≠0	REMARKS: E.A.=P +Δ_s	

Addend Gates	P														
Augend Gates	X_{SE}														
A.L.U. Control	+														
SHIFTER Control	D														
Memory Request	1														
WRITE															
A.L.U. → Z															
SH → Y	1														
XSEL	SH														
XSEL → X															
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI (EAD)														
EVEN/ODD/ODD2	ODD														
Counter	0														

X_{SE} = Delta Sign Extended = Δ_s

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=8, Δ=0	REMARKS: E.A. = P + 1 + (P+1)	

Addend Gates	P	Q	X												
Augend Gates	+1	Y	Y												
A.L.U. Control	+	+	+												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1		1												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RN1	ADR	ADR (EAD)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter	2	1	0												

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=9, Δ≠0	REMARKS: E.A. = P+ Δ_S + (00FF)	

Addend Gates	P	Q	X												
Augend Gates	X_{SE}	Y	Y												
A.L.U. Control	+	+	+												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1		1												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR (EAD)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter	2	1	0												
RI	1														

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=9, Δ=0	REMARKS: E.A. = P+1 + (P+1) + (00FF)	

Addend Gates	P		X	Q	X										
Augend Gates	+1	Y	Y	Y	Y										
A.L.U. Control	+	+	+	+	+										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1										
WRITE															
A.L.U. → Z															
SH → Y	1		1		1										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RN1	ADR	ADR	ADR	ADR (EAD)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2	1	0										
RI			1												

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=A, Δ≠0	REMARKS: E.A. = P + Δ_S + Q	

Addend Gates	P	Q												
Augend Gates	X_{SE}	Y												
A.L.U. Control	+	+												
SHIFTER Control	D	D												
Memory Request		1												
WRITE														
A.L.U. → Z														
SH → Y	1	1												
XSEL	SH	SH												
XSEL → X		1												
SH → P														
SH → M														
SH → Q														
SH → A														
State	RNI	ADR (EAD)												
EVEN/ODD/ODD2	ODD	ODD2												
Counter	0	0												

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=A, Δ=0	REMARKS: E.A. = P + 1 + (P + 1) + Q	

Addend Gates	P	Q	X											
Augend Gates	+1	Y	Y											
A.L.U. Control	+	+	+											
SHIFTER Control	D	D	D											
Memory Request	1		1											
WRITE														
A.L.U. → Z														
SH → Y	1	1	1											
XSEL	SH	Z	SH											
XSEL → X		1	1											
SH → P	1													
SH → M														
SH → Q														
SH → A														
State	RNI	ADR	ADR (EAD)											
EVEN/ODD/ODD2	ODD	EVEN	ODD											
Counter	2	1	0											

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=B, Δ≠0	REMARKS: E.A. = P + Δ_s + Q + (00FF)	

Addend Gates	P	Q	X												
Augend Gates	X_{SE}	Y	Y												
A.L.U. Control	+	+	+												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1	1	1												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR (EAD)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter	2	1	0												
RI	1														

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=B, Δ=0	REMARKS: E.A. = P + 1 + (P+1) + Q + (00FF)	

Addend Gates	P		X	Q	X										
Augend Gates	+1	Y	Y	Y	Y										
A.L.U. Control	+	+	+	+	+										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1										
WRITE															
A.L.U. → Z															
SH → Y	1		1	1	1										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR	ADR	ADR (EAD)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2	1	0										
RI			1												

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=C, Δ≠0	REMARKS: E.A. = $(P+\Delta_S)$	

Addend Gates	P	Q	X												
Augend Gates	X_{SE}	Y													
A.L.U. Control	+	+	⊕												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1		1*												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR (EAD*)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter	2	1	0												

* Only upon $\overline{T532}$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=C, Δ=0	REMARKS: E.A. = [P+1+(P+1)]													
Addend Gates	P		X	Q	X										
Augend Gates	+1	Y	Y	Y											
A.L.U. Control	+	+	+	+	⊕										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1										
WRITE															
A.L.U. → Z															
SH → Y	1		1		1*										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RN1	ADR	ADR	ADR	ADR (EAD*)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2	1	0										

* Only upon $\overline{1532}$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=D, Δ≠0	REMARKS: E.A. = $(P+\Delta_S)$ + (00FF)	

Addend Gates	P		X	Q	X										
Augend Gates	X_{SE}			Y	Y										
A.L.U. Control	+	⊕	⊕	+	+										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1										
WRITE															
A.L.U. → Z															
SH → Y	1		1		1										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR	ADR	ADR (EAD)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2*	1	0										
RI			$\overline{1532}$												

* Dec. only upon $\overline{1532}$·ODD

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=D, Δ=0	REMARKS: E.A. = [P+1+(P+1)] + (00FF)	

Addend Gates	P		X		X	Q	X								
Augend Gates	+1	Y	Y			Y	Y								
A.L.U. Control	+	+	+	⊕	⊕	+	+								
SHIFTER Control	D	D	D	D	D	D	D								
Memory Request	1		1		1		1								
WRITE															
A.L.U. → Z															
SH → Y	1		1		1		1								
XSEL	SH	Z	SH	Z	SH	Z	SH								
XSEL → X		1		1		1	1								
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RN1	ADR	ADR	ADR	ADR	ADR	ADR (EAD)								
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD								
Counter	6	5	4	3	2*	1	0								
RI					$\overline{1532}$										

* Dec. only upon $\overline{1532} \cdot ODD$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=E, Δ≠0	REMARKS: E.A. = (P + Δ_s) + Q	

Addend Gates	P	Q	X												
Augend Gates	X_{SE}		Y*												
A.L.U. Control	+	⊕	+*/⊕̄*												
SHIFTER Control	D	D	D												
Memory Request	1		1												
WRITE															
A.L.U. → Z															
SH → Y	1	1	1*												
XSEL	SH	Z	SH												
XSEL → X		1	1												
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR (EAD*)												
EVEN/ODD/ODD2	ODD	EVEN	ODD												
Counter	2	1	0												

* only upon $\overline{1532}$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=E, Δ=0	REMARKS: E.A. = [P + 1 + (P+1)] + Q	

Addend Gates	P		X	Q	X										
Augend Gates	+1		Y		Y*										
A.L.U. Control	+	⊕	+	⊕	+*/⊕̄*										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1										
WRITE															
A.L.U. → Z															
SH → Y	1		1	1	1*										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR	ADR	ADR (EAD*)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2	1	0										

* Upon $\overline{T532}$

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=F, Δ≠0	REMARKS: E.A.+(P+ Δ_s) + Q + (00FF)	

Addend Gates	P		X	Q	X										
Augend Gates	X_{SE}			Y	Y										
A.L.U. Control	+	⊕	⊕	+	+										
SHIFTER Control	D	D	D	D	D										
Memory Request	1		1		1										
WRITE															
A.L.U. → Z															
SH → Y	1		1	1	1										
XSEL	SH	Z	SH	Z	SH										
XSEL → X		1		1	1										
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI	ADR	ADR	ADR	ADR (EAD)										
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD										
Counter	4	3	2*	1	0										
RI			$\overline{1532}$												

* Decrement Counter only upon $\overline{1532}$ · ODD

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADDRESSING	CODE: F1=F, Δ=0	REMARKS: E.A.= [P + 1 + (P+1)] + Q + (OFF)	

Addend Gates	P		X		X	Q	X								
Augend Gates	+1	Y	Y			Y	Y								
A.L.U. Control	+	+	+	⊕	⊕	+	+								
SHIFTER Control	D	D	D	D	D	D	D								
Memory Request	1		1		1		1								
WRITE															
A.L.U. → Z															
SH → Y	1		1		1	1	1								
XSEL	SH	Z	SH	Z	SH	Z	SH								
XSEL → X		1		1		1	1								
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RN1	ADR	ADR	ADR	ADR	ADR	ADR (EAD)								
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD								
Counter	6	5	4	3	2*	1	0								
RI					$\overline{1532}$										

* Decrement Counter only upon $\overline{1532}$.ODD

In the following order:

F = 1

F = 2

F = 3

.

.

.

.

.

.

F = F

AB107/AB108 EXECUTION CHART

INSTRUCTION: JMP	CODE: F=1	REMARKS:

Addend Gates															
Augend Gates	A														
A.L.U. Control	$\overline{\text{Aug}}$														
SHIFTER Control	D														
Memory Request															
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z														
XSEL → X	1														
SH → P															
SH → M															
SH → Q															
SH → A															
State	RNI														
EVEN/ODD/ODD2	EVEN														

AB107/AB108 EXECUTION CHART

INSTRUCTION: MUL	CODE: F=2	REMARKS:	

Addend Gates		Q			Q		Q	P						
Augend Gates			X	A	X ⑤	A		+1	A					
A.L.U. Control	$\overline{\text{Aug}}$	$\overline{\text{Add}}$	$\overline{\text{Aug}}$	$\overline{\text{Aug}}$	+	⊕	$\overline{\text{Add}}$	+	$\overline{\text{Aug}}$					
SHIFTER Control	D	D	D	D	LR1	LR2	D	D	D					
Memory Request								1						
WRITE														
A.L.U. → Z														
SH → Y														
XSEL	Z		SH						Z					
XSEL → X	①↓		③↓						1					
SH → P								1						
SH → M														
SH → Q		②↓			⑥↓		④↓							
SH → A				④↓		⑥↓			⑦↓					
State	OP	MD21	MDS1	MDS1	MDS	MDS	MD1	OP	RN1					
			MDS2											
EVEN/ODD/ODD2	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN					
Counter*	22	21	20	19	18 ÷ 2 (17 times)		1	0	0					
Clear Q			1											
Set BB		1												

* Decrement upon $\overline{\text{MDS·E}}$

① $\overline{\text{IM.OP.}}$ ② Q15 ③ X15 ④ BB⊕X15 ⑤ A0 ⑥ COUNTER=2 ⑦ BB

AB107/AB108 EXECUTION CHART

INSTRUCTION: DIV	CODE: F=3	REMARKS:

Addend Gates		Q			Q		Q	P							
Augend Gates			X	A	X (5)	A		+1	A						
A.L.U. Control		$\overline{\text{Add}}$	$\overline{\text{Aug}}$	$\overline{\text{Aug}}$	+	⊕	$\overline{\text{Add}}$	+	$\overline{\text{Aug}}$						
SHIFTER Control	D	D	D	D	(6) LL1D/D̄ (6)	LL2	D	D	D						
Memory Request								1							
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z		SH						Z						
XSEL → X	1 (1)		1 (3)						1						
SH → P								1							
SH → M															
SH → Q		1 (2)			1		1 (4)								
SH → A				1 (4)		1			1 (7)						
State	OP	MD21	MDS1	MDS1	MDS	MDS	MD1	OP	RN1						
			MDS2												
EVEN/ODD/ODD2	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN						
Counter*	22	21	20	19	18 ÷ 2 (17 times)		1	0	0						
Set BB		1													

* Decrement upon $\overline{\text{MDS} \cdot \text{E}}$

(1) IM.OP (2) Q15 (3) X15 (4) BB⊕X15 (5) Q<X (6) COUNTER=2 (7) BB

INSTRUCTION: STQ	CODE: F=4	REMARKS:

Addend Gates	Q	P													
Augend Gates		+1													
A.L.U. Control	⊕	+													
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE	1														
A.L.U. → Z	1														
SH → Y															
XSEL	Z		Z												
XSEL → X			1												
SH → P		1													
SH → M															
SH → Q															
SH → A															
State	OP	OP	RNI												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												

AB107/AB108 EXECUTION CHART

INSTRUCTION: RTJ	CODE: F=5	REMARKS:

Addend Gates	P	X													
Augend Gates	+1	+1													
A.L.U. Control	+	+	⊕												
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE	1														
A.L.U. → Z	1														
SH → Y															
XSEL	Z		Z												
XSEL → X			1												
SH → P		1													
SH → M															
SH → Q															
SH → A															
State	OP	OP	RN1												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												

AB107/AB108 EXECUTION CHART

INSTRUCTION: STA	CODE: F=6	REMARKS:

Addend Gates		P													
Augend Gates	A	+1													
A.L.U. Control	⊕	+	⊕												
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE	1														
A.L.U. → Z	1														
SH → Y															
XSEL	Z		Z												
XSEL → X			1												
SH → P		1													
SH → M															
SH → Q															
SH → A															
State	OP	OP	RNI												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												

AB107/AB108 EXECUTION CHART

INSTRUCTION: SPA	CODE: F=7	REMARKS:

Addend Gates		P													
Augend Gates	A	+1	+1 [1]												
A.L.U. Control	●	+	+①/●①												
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE	1														
A.L.U. → Z	1														
SH → Y															
XSEL	Z		Z												
XSEL → X			1												
SH → P		1													
SH → M															
SH → Q															
SH → A			1②												
State	OP	OP	RNI												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												
		NOTES:	①. PRY=1 ②. $\overline{PEF}$=1												

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADD	CODE: F=8	REMARKS:

Addend Gates		P	X												
Augend Gates		+1	A												
A.L.U. Control	0	+	+												
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z		Z												
XSEL → X	1		1												
SH → P		1													
SH → M															
SH → Q															
SH → A			1												
State	OP	OP	RN1												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												

AB107/AB108 EXECUTION CHART

INSTRUCTION: SUB	CODE: F=9	REMARKS:

Addend Gates		P	X												
Augend Gates		+1	A												
A.L.U. Control	●	+	-												
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z		Z												
XSEL → X	1		1												
SH → P		1													
SH → M															
SH → Q															
SH → A			1												
State	OP	OP	RNI												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												

INSTRUCTION: AND	CODE: F=A	REMARKS:

Addend Gates		P	X												
Augend Gates		+1	A												
A.L.U. Control	⊕	+	LP												
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z		Z												
XSEL → X	1		1												
SH → P		1													
SH → M															
SH → Q															
SH → A			1												
State	OP	OP	RNI												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												

AB107/AB108 EXECUTION CHART

INSTRUCTION: EOR	CODE: F=B	REMARKS:

Addend Gates		P	X												
Augend Gates		+1	A												
A.L.U. Control	⊕	+	⊕												
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z		Z												
XSEL → X	1		1												
SH → P		1													
SH → M															
SH → Q															
SH → A			1												
State	OP	OP	RN1												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												

AB107/AB108 EXECUTION CHART

INSTRUCTION: LDA	CODE: F=C	REMARKS:

Addend Gates		P	X												
Augend Gates		+1													
A.L.U. Control	⊕	+	⊕												
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z		Z												
XSEL → X	1		1												
SH → P		1													
SH → M															
SH → Q															
SH → A			1												
State	OP	OP	RNI												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												

AB107/AB108 EXECUTION CHART

INSTRUCTION: RA0	CODE: F=D	REMARKS:

Addend Gates			X	P											
Augend Gates		Y	+1	+1											
A.L.U. Control	⊕	⊕	+	+	⊕										
SHIFTER Control	D	D	D	D	D										
Memory Request		1		1											
WRITE			1												
A.L.U. → Z			1												
SH → Y															
XSEL	Z		Z		Z										
XSEL → X	1				1										
SH → P				1											
SH → M															
SH → Q															
SH → A															
State	OP2	OP2	OP	OP	RN1										
EVEN/ODD/ODD2	EVEN	ODD	EVEN	ODD	EVEN										

AB107/AB108 EXECUTION CHART

INSTRUCTION: LDQ	CODE: F=E	REMARKS:

Addend Gates		P	X												
Augend Gates		+1													
A.L.U. Control	⊕	+	⊕												
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z		Z												
XSEL → X	1		1												
SH → P		1													
SH → M															
SH → Q			1												
SH → A															
State	OP	OP	RNI												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												

AB107/AB108 EXECUTION CHART

INSTRUCTION: ADQ	CODE: F=F	REMARKS:

Addend Gates		P	Q												
Augend Gates		+1	X												
A.L.U. Control	⊕	+	+												
SHIFTER Control	D	D	D												
Memory Request		1													
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z		Z												
XSEL → X	1		1												
SH → P		1													
SH → M															
SH → Q			1												
SH → A															
State	OP	OP	RNI												
EVEN/ODD/ODD2	EVEN	ODD	EVEN												

In the following order:

F1 = 0, ENTER, SWEEP

F1 = 1

F1 = 2,3

F1 = 4,5

F1 = 6,7

F1 = 8

F1 = 9

F1 = A

F1 = B

F1 = C,D

F1 = E

Interrupt

F1 = F

AB107/AB108 EXECUTION CHART

INSTRUCTION: SLS (+ ENTER) (+ SWEEP)	CODE: F1=0	REMARKS:

Addend Gates	P														
Augend Gates	+1 ①	X													
A.L.U. Control	+1 ① / +1 ①	0													
SHIFTER Control	D	D													
Memory Request	1														
WRITE		1 ③													
A.L.U. → Z		1 ③													
SH → Y															
XSEL	Z	Z													
XSEL → X		1 ②													
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RNI	RNI													
EVEN/ODD/ODD2	ODD	EVEN													
NOTES:	①. ES ②. ENTER	③. ENTER													

60

INSTRUCTION: SKIP	CODE: F=0, F1=1	REMARKS:	

Addend Gates	P	P													
Augend Gates	+1	∇*													
A.L.U. Control	+	+*/⊕*													
SHIFTER Control	D	D													
Memory Request		1													
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z	Z	Z												
XSEL → X			1												
SH → P	1	1													
SH → M															
SH → Q															
SH → A															
State	RN1	RN1	RN1												
EVEN/ODD/ODD2	ODD	ODD2	EVEN												
NOTES:		*SKT=1													

89723800 A

AB107/AB108 EXECUTION CHART

INSTRUCTION: INP / OUT	CODE: F=0 F1=2 F1=3	REMARKS:

Addend Gates	P		②P/X③												
Augend Gates	X_{SE}		④+1												
A.L.U. Control	+		+④												
SHIFTER Control	D	TAQ1	D	D											
Memory Request			1												
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	SH			Z											
XSEL → X	1			1											
SH → P			1												
SH → M															
SH → Q															
SH → A		$_1$①													
State	RN1	OP	OP	RN1											
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN											
NOTES:	① INP•REPLY		② REPLY ③ REPLY	④ TRJ											

AB107/AB108 EXECUTION CHART

INSTRUCTION: EIN / IIN	CODE: F=0 F1=4 / F1=5	REMARKS:

Addend Gates	P														
Augend Gates	+1	⊕													
A.L.U. Control	+														
SHIFTER Control	D	D													
Memory Request	1														
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z	Z													
XSEL → X		1													
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RNI	RNI													
EVEN/ODD/ODD2	ODD	EVEN													
Enable Interrupt		EIN*													
Inhibit Interrupt	IIN														

* In next instruction

AB107/AB108 EXECUTION CHART

INSTRUCTION: SPB CPB	CODE: F=0 F1=6 F1=7	REMARKS:

Addend Gates	Q			X	P										
Augend Gates			Y		+1										
A.L.U. Control	⊕	⊕	⊕	⊕	+	⊕									
SHIFTER Control	D	D	D	D	D	D									
Memory Request	1		1		1										
WRITE				1											
A.L.U. → Z				1											
SH → Y	1														
XSEL		Z				Z									
XSEL → X		1	0			1									
SH → P					1										
SH → M															
SH → Q															
SH → A															
State	RNI	OP2	OP2	OP	OP	RNI									
EVEN/ODD/ODD2	ODD	EVEN	ODD	EVEN	ODD	EVEN									
Set Program Protect				SPB											
Clear Program Protect				CPB											

AB107/AB108 EXECUTION CHART

INSTRUCTION: INTERREGISTER	CODE: F=0, F1=8	REMARKS:

Addend Gates	P	(1) Q / (2) M / (3) X
Augend Gates	+1	(4) (5) A/X
A.L.U. Control	+	(6) LP / (7) XR / (8) NAND / (9) +
SHIFTER Control	D	D D
Memory Request	1	
WRITE		
A.L.U. → Z		
SH → Y		
XSEL	Z	Z
XSEL → X	1	1
SH → P	1	
SH → M		1 (10)
SH → Q		1 (11)
SH → A		1 (12)
State	RNI	RNI
EVEN/ODD/ODD2	ODD	EVEN
Set X Register	1	

NOTES:

(1.) 14 (2.) 13 (3.) $\overline{13} \cdot \overline{14}$ (4.) 15 (5.) $\overline{15}$ (6.) $17 \cdot \overline{16}$ (7.) $\overline{17} \cdot 16$ (8.) $17 \cdot 16$ (9.) $\overline{17} \cdot \overline{16}$ (10.) 10 (11.) 11 (12.) 12

AB107/AB108 EXECUTION CHART

INSTRUCTION: INA	CODE: F=0, F1=9	REMARKS:

Addend Gates	P	X													
Augend Gates	+1	A													
A.L.U. Control	+	+													
SHIFTER Control	D	D													
Memory Request	1														
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	Z	Z													
XSEL → X	1 (1)	1													
SH → P	1														
SH → M															
SH → Q															
SH → A		1													
State	RNI	RNI													
EVEN/ODD/ODD2	ODD	EVEN													

(1) Upon 17 to X upper only.

AB107/AB108 EXECUTION CHART

INSTRUCTION: ENA	CODE: F=0, F1=A	REMARKS:

Addend Gates	P														
Augend Gates	+1	X													
A.L.U. Control	+	⊕													
SHIFTER Control	D	D													
Memory Request	1														
WRITE															
A.L.U. → Z															
SH →Y															
XSEL	Z	Z													
XSEL →X	1 (1)	1													
SH→ P	1														
SH→ M															
SH→ Q															
SH→ A		1													
State	RN1	RN1													
EVEN/ODD/ODD2	ODD	EVEN													
	(1) Upon I7 to X upper only														

AB107/AB108 EXECUTION CHART

INSTRUCTION: NOP	CODE: F1=B	REMARKS:

Addend Gates	P														
Augend Gates	+1														
A.L.U. Control	+	⊕													
SHIFTER Control	D	D													
Memory Request	1														
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	SH	Z													
XSEL → X		1													
SH → P	1														
SH → M															
SH → Q															
SH → A															
State	RNI	RNI													
EVEN/ODD/ODD2	ODD	EVEN													

AB107/AB108 EXECUTION CHART

INSTRUCTION: ENQ INQ	CODE: F=0 F1=C F1=D	REMARKS:

Addend Gates	P	Q (2)														
Augend Gates	+1	X														
A.L.U. Control	+	+(2)/-(2)														
SHIFTER Control	D	D														
Memory Request	1															
WRITE																
A.L.U. → Z																
SH → Y																
XSEL	Z	Z														
XSEL → X	1 (1)	1														
SH → P	1															
SH → M																
SH → Q		1														
SH → A																
State	RNI	RNI														
EVEN/ODD/ODD2	ODD	EVEN														

(1) Upon 17, to X upper only.
(2) Upon INQ

AB107/AB108 EXECUTION CHART

INSTRUCTION: EXI	CODE: F=0, F1=E	REMARKS:

Addend Gates	X	X													
Augend Gates	+1			X											
A.L.U. Control	+	⊕	⊕	⊕	⊕										
SHIFTER Control	T.A.	D	D	D	D										
Memory Request		1		1											
WRITE															
A.L.U. → Z															
SH → Y															
XSEL	SH	SH	Z		Z										
XSEL → X	1 ①	1	1		1										
SH → P				1											
SH → M															
SH → Q															
SH → A															
Shift	RNI	RNI	OP	OP	RNI										
EVEN/ODD/ODD2	ODD	ODD2	EVEN	ODD	EVEN										
	① To X upper only														

AB107/AB108 EXECUTION CHART

INSTRUCTION: ENI Interrupt	CODE:	REMARKS:

Addend Gates	P		P	X											
Augend Gates	+1	X	-1 ①	+1											
A.L.U. Control	+		+	+											
SHIFTER Control	TA	D	D	D	D										
Memory Request		1		1											
WRITE			1												
A.L.U. → Z			1												
SH → Y															
XSEL	SH	SH	Z	SH	Z										
XSEL → X	1	1			1										
SH → P				1											
SH → M															
SH → Q															
SH → A															
State	ENI (RNI)*	ENI	ENI ENI2	ENI ENI2	ENI4 RNI										
EVEN/ODD/ODD2	ODD	ODD2	EVEN	ODD	EVEN										
CLRIR	1 ②			1											

NOTE: *RNI is the only state which can remain while ENI, and indicates that an instruction has been completed.

① DEL·$\overline{F=0}$ Otherwise will be (-0)

② ENI·RNI·0

AB107/AB108 EXECUTION CHART

INSTRUCTION: SHIFTS	CODE: F=0, F1=F	REMARKS: See additional timing diagrams (page 7 and 8).	

Addend Gates	P	Q①			P	Q③	P	Q①							
Augend Gates	+1	A④			+1	A⑤	+1	A④							
A.L.U. Control	+	⊕			+	⊕	+	⊕							
SHIFTER Control	D	Shift			D	Shift	D	Shift							
Memory Request	1						1								
WRITE															
A.L.U. → Z															
SH → Y															
XSEL		Z						Z							
XSEL → X		1						1							
SH → P	1						1								
SH → M															
SH → Q		$1^{②}$				$1^{③}$		$1^{②}$							
SH → A		$1^{④}$				$1^{⑤}$		$1^{④}$							
State	RNI	RNI			RNI	ITR	OP	RNI							
EVEN/ODD/ODD2	ODD	EVEN			ODD	EVEN	ODD	EVEN							
Load Counter					1										
SHI	1	1			0	0	0	0							

① $\overline{T6}$
② $\overline{T6} \cdot 15 \cdot (SHI \oplus \overline{T0})$
③ $(EVEN + \overline{T6}) \cdot 15$
④ $16 \cdot 15(\overline{K0} + 10) + 16(SHI \oplus \overline{T0})$
⑤ $(ODD + \overline{15}) \cdot 16$

COMMENT SHEET

MANUAL TITLE CONTROL DATA® SYSTEM 17 AB107/AB108 Computer

Execution Charts

PUBLICATION NO. 89723800 REVISION A

FROM NAME: _____

BUSINESS
ADDRESS: _____

COMMENTS: This form is not intended to be used as an order blank. Your evaluation of this manual will be welcomed by Control Data Corporation. Any errors, suggested additions or deletions, or general comments may be made below. Please include page number.

CUT ALONG LINE

STAPLE

STAPLE

FOLD

FOLD

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 8241 MINNEAPOLIS, MINN.

POSTAGE WILL BE PAID BY

CONTROL DATA CORPORATION
PUBLICATIONS AND GRAPHICS DIVISION
4455 EASTGATE MALL
LA JOLLA, CALIFORNIA 92037

CUT ALONG LINE

FOLD

FOLD