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CONTROL DATA CORPORATION

CONTROL DATA®
SYSTEM 17

KEY TO LOGIC SYMBOLS

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Address comments concerning this manual to:
Control Data Corporation
Publications and Graphics Division
4455 Eastgate Mall
La Jolla, CA 92037
or use Comment Sheet in the back of this manual.

PREFACE

This publication lists the logic symbols used in the Logic Diagrams included in Section 5 of the Customer Engineering (CE) Manuals for the following equipments:

Equipment		CE Manual Publication Number
Identification Number	Name	
AB107-A	Computer, 900 nsec memory cycle	89633300
AB108-A	Computer, 600 nsec memory cycle	89633300
BA201-A	Memory Module, 600 nsec.	89633300
BA201-B	Memory Module, 900 nsec.	89633300
BT148-A	Expansion Enclosure	89633300
BU120-A	Memory Expansion Controller	89633300
CC108	Key Entry Station - 480	89664800
CD126	Key Entry Station - 32	89672400
DJ815-A	Asynchronous Communications Controller	89638300
FA442-A	NRZI-ICL Magnetic Tape Transport Controller	89637700
FA446-A	NRZI-LCTT Magnetic Tape Transport Controller	89769500
FA716-A	Cartridge Disk Crive Controller	89638100
FC106-A	Key Entry Station Controller	89672200
FE119-A	Card Read Controller	89637500
FF524-A	Line Printer Controller	89637300
FJ606-A	Synchronous Communications Controller	89638500
FV497-A	Phase Encoding Formatter	89796100
GN109-A	Key Entry Station Power Distribution Unit	89672200

CONTENTS

KEY TO LOGIC SYMBOLS

INTRODUCTION

The following pages give short functional descriptions of the logic symbols used in Section 5 (Diagrams) of the Customer Engineering Manuals listed in the Preface to this publication. The symbols conform generally to CONTROL DATA® usage (Microcircuit Handbook, publication number 15006100), using the polarity logic convention. Some features of the convention are noted here for convenience and departures from publication 15006100, Rev. 8 are described.

POLARITY LOGIC CONVENTION

The polarity logic convention uses physical states of "High" and "Low"(H and L) rather than "1" and "0", in describing signal flow in the test. A High is the nominally most positive potential in this convention; a Low, the nominally most negative one. The input polarity indicator signifies that a Low is required to make the input active. The output negation indicator signifies that a Low is present at the output when the logic function is active (or "set" in the case of most sequential logic such as flip-flops).

STANDARD LOGIC LEVELS

The standard logic levels for the TTL microcircuit packages used are:

$$+1.8\ V < H < +5.5\ V \quad \text{and} \quad -1.0\ V < L < +0.85\ V$$

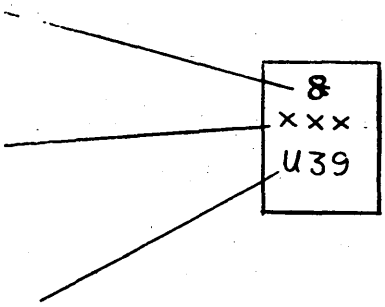
If levels other than these are used at least one non-standard logic indicator (——/——) is used.

Signal levels on other circuits (such as on an MOS) are indicated appropriately on the relevant logic diagram.

LOGIC SYMBOLS

Each symbol is described on the logic diagrams by three groups of letters or numerals within the symbol.

* qualifying symbol: the part of the symbol that specifies the logic function
* CDC element identifier: 3 or 4 digit alphanumeric word assigned to a microcircuit (IC) package
* physical location code: a 3 or 4 digit alphanumeric word (number prefixed by the letter "U") defining the package on the printed wiring board. This code is not shown on the symbol in this key.

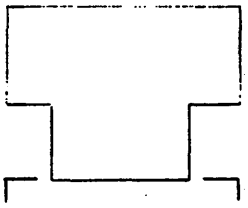


In this key the term name (manufacturers' reference number) of the microcircuits are given but the term name is not used in the logic diagrams. Several element identifiers may have the same logic symbol. Where this occurs they are given in the key and their place on the symbol is indicated by XXX.

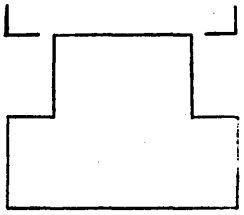
SYMBOL OUTLINE

The outline portion of a symbol is rectangular in shape except for the neck of a common control block. To reduce space requirements of a diagram, separate symbols for basic operations may be joined together (abutted) or incorporated within another outline if there are no external pin numbers, etc., to identify where they share a common boundary. While symbol consistency is highly desireable, no logic significance is attached to the size or aspect ratio of the outline or to the line weights used in the outline. Logic significance is portrayed by the qualifying symbols and designators.

Common Control Block - Signals entering this block on the left are common to more than one section of the circuit. The neck of the common control block abuts the top or bottom of the section(s) it controls.



or



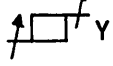
Common Output Block - Signals leaving this block on the right are derived from more than one section of the circuit. The double line of the common output block abuts the top or bottom of the section(s) it obtains its signals from. It is placed at the end opposite the common control block when both are used. Examples may include decoding of counter codes for carry and borrow, or for parity checking or generation.

Explicit and Implicit Signal Flow Across Common Boundaries of Abutted Symbol Outlines - No signal flow is to be implied between vertically abutted symbol outlines except for the common control block and common output block which may connect to any or all symbol outlines vertically abutted to them. In counters and shift registers, it is acknowledged that there is signal interaction between vertically abutted symbols, but this is still symbolically accomplished through actions initiated in the common control block. In horizontally abutted symbol outlines, it is implicit that a single connection is made from the left symbol output to the right symbol input. Additional connections may be explicitly indicated by showing all signal connections (including the first one) with a horizontal dash crossing the common boundary.

Diagram Logic Flow Direction - Signals and succeeding logic functions flow from left to right across the diagram page insofar as possible. The most significant bits of a group are placed nearest the top.

QUALIFYING SYMBOL

A symbol used to specify the required logic operation. In certain cases this symbol is replaced or completed by mathematical or numerical values where necessary to better define the functions of the element. The qualifying symbol is placed in the upper center of its rectangular outline. MIL-STD-12C English abbreviations are usually added in the neck of the common control block or below the qualifying symbol in MSI that does not have a common control block. A list of qualifying symbols follows:

&	All inputs active.
1	Any input active
≥2	Two or more inputs active
=1	Only one input active {exclusive OR}
=2	Only two inputs active; no more, no less
=	All inputs equal; either all active or all inactive
G	Generator or oscillator {waveform may be added}
	Schmitt Trigger {hysteresis characteristic}
	Schmitt Trigger with most positive trigger point adjustable
	Schmitt Trigger with least positive trigger point adjustable
1	One-shot multivibrator
	Time delay {delay period(s) may appear above this symbol}
00	Even Parity
000	Odd Parity
X→Y	X {inputs} decoded or encoded to Y {outputs}
X MAX→Y	The greatest input alone is decoded or encoded to Y {outputs}
X/Y	X {input level} converted to Y {output level}
X  Y	X {input level, with Schmitt Trigger} converted to Y {output level}
∫X/Y	X {input level with integration} converted to Y output level
X↗Y	X {input level with adjustable threshold} converted to Y {output level}
X  Y	X {input level with adjustable Schmitt Trigger thresholds} converted to Y {output level}
Σ	Arithmetic summing circuit
F{x}	Complex function, logic summing, or logic and arithmetic summing
d/dt	Input signal is differentiated to yield the output signal
ODD	Odd register bits {of an interlaced shift register}; shifted by odd shift signal
EVEN	Even register bits {of an interlaced shift register}; shifted by even shift signal.

Note: No qualifying symbol is used to identify a flop-flop. The presence of input signal designators S, R, J, K, D and T, which are used almost exclusively with flip-flops, indicates a flip-flop or a logic element, such as a register or counter, that contains flip-flops.

Qualifying Symbol for Complex Functions - In cases where a straight-forward symbol cannot simply and fully portray the full logic function of a complex element, then the nearest applicable qualifying symbol suffixed with an asterisk(*) is used. If the function differs much from existing qualifying symbols, then an F is used as the qualifying symbol. If space permits, an explanation may be given outside the symbol outline. Example: 7 segment decoders {encoders} are portrayed as "X→Y*".

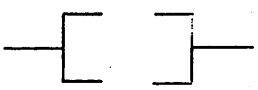
Qualifying Symbol Choices - Some logic functions can be portrayed in multiple ways using different qualifying symbols, or combinations thereof. The qualifying symbol that best indicates the function of interest in a given application is generally given preference. Example: An element used to drive or receive long signal lines, even though it has no non-standard logic level indicators on its input or output, may be assigned the qualifying symbol "X/Y" in place of "1" or in addition to functions like "=, 1, etc." The function of line driving and receiving in this case is best portrayed by using the level converter qualifying symbol "X/Y".

Function Abbreviations - The following abbreviations are used to indicate the overall function of logic elements {such as MSI} made up of a number of related functions:

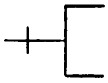
- ALU - Arithmetic and Logic Unit
- mCNTR - Counter. The character m is the maximum number of counts {e.g., 10CNTR or 16CNTR}
- DCDR - Decoder and/or Encoder
- DEMUX - Demultiplexer
- DRVR - Driver
- MEM - Memory
- MUX - Multiplexer
- RCVR - Receiver
- RGTR - Register
- SRn-m - Shift Register. The character n is replaced by the number of registers; if no value is used for n, the number of registers is understood to be one. The character m is replaced by the number of bits in the shift register. EXAMPLE: SR2-32 (i.e., two thirty-two bit shift registers). If prefixed by an arrowhead { ▶ } the shift register is dynamic and requires refreshing.

INDICATORS

Active State Indicators - A symbol used to specify physical states of an input or output connection and to indicate which state is the active state. As a minimum, the active state indicators include definition of static states, but may also indicate dynamic characteristics, non-digital characteristics, etc. Each signal line has its own indicators which are placed on the line when outside the symbol outline, and horizontally in line with the connection when inside the symbol outline. A list of the various indicators, and their defined position relative to the symbol outline when used as inputs or outputs follows:

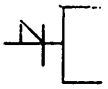


Implies static high in polarity logic convention by absence of polarity and negation indicators.

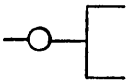


Static high in polarity logic when used with inhibit designators.

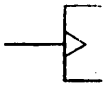
Static low (polarity indicator) in polarity logic.



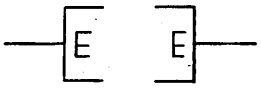
Static low in polarity logic when used with inhibit designator.



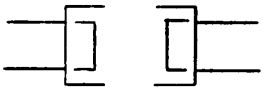
Static 0 (negation indicator) in polarity logic when used with inhibit designator.



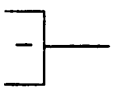
Transition to the static state indicated. (Combine with applicable static indicators above. Not used with outputs).



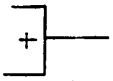
Signal that extends inputs of a function. If combined with grouped connection in following item, the E is inside.



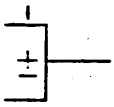
Two or more grouped connections that always maintain a fixed relation in state to each other, unless modified by a gate.



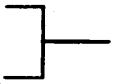
The minus on the output indicates that this element is capable of supplying logic Low's only. A logic High output must come from some other source.



The plus on the output indicates that this element is capable of supplying logic High's only. A logic Low output must come from some other source.



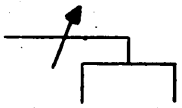
The plus and minus on the output indicates that this element is capable of supplying logic High's and logic Low's only when the associated gate is active. When the gate is not active the output level will be determined by some other source.

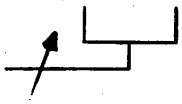


The absence of a plus or minus indicates that this element is always capable of supplying both logic High's and logic Low's.

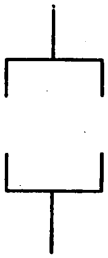
Non-standard level or levels of logic. User must define levels elsewhere.

Analog and non-logic signals.





Variable Parameter Control for varying a characteristic or characteristics of a logic function as indicated by the qualifying symbol and/or information external to the symbol. Indicator may be omitted if adjustable components are shown adjacent to the symbol.



Connection points for external timing components, null and reference components, reference inputs, internal references, terminations, and for other inputs or outputs other than the signal inputs and outputs related directly to the logic function. Non-standard positive voltages or non-standard pin connections for a standard positive voltage are made at the top of the symbol outline only. Non-standard negative voltages or non-standard pin connections for a ground or non-standard negative voltage are made only at the bottom of the symbol outline.

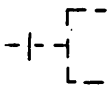
DESIGNATORS

Unique inputs or outputs which require specific definition relative to the qualifying symbol are called designators. Except for the inhibit designator, designators are placed inside the symbol outline and also inside any internal indicators, and in line with the input or output connection line they identify. In the case of grouped inputs or outputs (using a bracket or internal symbol outline), the designator is located vertically between the upper and lower signal line of the group, but not necessarily centered. The following is a list of designators:

0, 1, 2, 3	Designates consecutive numbering only, as opposed to weighting. To be used only as an aid in simplifying the remainder of the symbol function.
1, 2, 4, 8	Designates relative weighting of input or output lines. They may be binary or decimal representation of binary values. Absence of "0" generally implies weighting.
X0, X1, X2	Designates consecutive numbering except that the most significant place is an "irrelevant" condition. May also be used to indicate "irrelevant" bits in binary.
A, B, C	Designates individual groups of signals as further defined by the qualifying symbol or other designators.
A	Without numeric suffix, it designates address dependent input or output. With a numeric suffix, it designates selection of the address identified by the suffix, such as A000, A255. 1, 2, 3, etc., may precede "A" if necessary to distinguish separate addressing ports. The "A" prefix precedes G and C prefixes if they appear together.

C	Designates a clock input that is used to enable D inputs and clock dependent outputs. Separate clock inputs have a suffix (usually numeric) such as C1, C2, etc. A "C" prefix follows A and G prefixes if they appear together. C not used for a clear or count designator.
D	Designates a data input for storage elements (clocked by a C input).
G	Designates a gating input that has an AND relationship with other inputs or outputs that reference it. Separate gating inputs have a suffix (usually numeric) such as G1, G2, etc. A "G" prefix precedes a C prefix, but follows the A prefix if they appear together.
J	Designates J input of J-K flip-flop.
K	Designates K input of J-K flip-flop.
R	Designates reset input of flip-flop or other reset-table function.
S	Designates set input of flip-flop or other settable function.
T	Designates toggle (or complement) input of flip-flop.
-1	Designates decrement-by-one (count down) input.
+1	Designates increment-by-one (count up) input.
→	Designates shift down (right) input.
←	Designates shift up (left) input.

Designates input-controlled delay (trailing edge). Used to designate an output which changes state on the departure of an input from its active state (whether High or Low). The input controlling the delay is implied to be a C input unless a reference prefix identifies a G input. Set or Reset inputs overrule the input controlled delay unless otherwise noted.



Designates an input that inhibits a non-sequential logic function. The vertical line designator appears on the connection line as shown, and requires active-state indicators to be located to its left, but not input pin numbers.

{=1}

Designates a group of inputs directly below it in which one, no more, no less, shall be active at any given time.

ORGANIZATION OF THIS PUBLICATION

The Logic Symbols are listed in the order of CONTROL DATA® Element Identifier, which appear at the top right-hand corner of each page. Note that circuits of the same type having different speeds are listed together. Microcircuits not allocated an Element Identifier are listed at the end of this publication, in Type (Term Name) order. Immediately preceding the pages of description there is a cross-reference index for Type/Element Identifier.

CROSS-REFERENCE INDEX

TYPE (TERM NAME)			ELEMENT IDENTIFIER		
STANDARD	HIGH SPEED	SUPER HIGH SPEED	STANDARD	HIGH SPEED	SUPER HIGH SPEED
7400	74H00	74S00	140	140H	140S
7401	74H01		202	202H	
7403			202		
7404	74H04	74S04	146	146H	146S
7405	74H05		203	203H	
7406			200		
7407			-		
7408	74H08		201	-	
7409			201C		
7410	74H10		141	141H	
7411	74H11	74S11	-	213H	213S
7420	74H20		208	208H	
-	74H21		-	212H	
7430	74H30		206	206H	
7437			210		
7438			204		
7440	74H40		143	143H	
7450	74H50		145	145H	

CROSS-REFERENCE INDEX, Cont'd.

TYPE (TERM NAME)			ELEMENT IDENTIFIER		
STANDARD	HIGH SPEED	SUPER HIGH SPEED	STANDARD	HIGH SPEED	SUPER HIGH SPEED
7451	74H51		-	223H	
	74H52			217H	
7453	74H53		209	209H	
	74H54			-	
	74H62			-	
		74S64			205S
7474	74H74		175	175H	
7485			524		
7486			149		
7496/9396			515		
	74H101			245H	
	74H102			-	
	74H106			242H	
		74S112			243S
74123			193		
		74S140			-
74150			531		
74151/93151			505		
74154/9311			167		
74157/9322			189		
74175		74S175	520		520S
74180			502		

TYPE (TERM NAME)			ELEMENT IDENTIFIER		
STANDARD	HIGH SPEED	SUPER HIGH SPEED	STANDARD	HIGH SPEED	SUPER HIGH SPEED
74181/9341		74S181	509		509S
74182/9342			510		
74192/9360			523		
74193/9366			500		
74195/9300			159		
75108			162C		
75154			902		
75450			180		
9300			159		
9308			168		
9309			170		
9311			167		
9318			532		
9322			189		
9341			509		
9342			510		
9360			523		
9366			500		
9396			515		

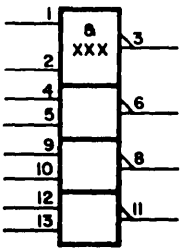
TYPE (TERM NAME)	ELEMENT IDENTIFIER
1103	-
1103-1	-
2518B	-
3342	-
4024	582
4044	-
DM8820A	-
DM8830A	-
KR 2376-NPD	-
MC 1488	900
MC 4044	-
MOC 1000	-
MOC 1003	-
S1685	-
UART	-
µA-723	-
µA-723C	-
µA-741	-

Type (Term name): 7400, 74H00, 74S00

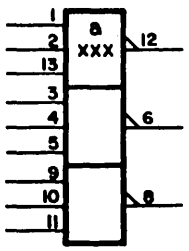
Element Identifier: 140, 140H, 140S

Description: Quadruple 2-Input Positive NAND Gates

Equation: $Y = \overline{AB}$ (each gate)



Type (Term name):	7410, 74H10
Element Identifier:	141, 141H
Description:	Triple, 3-Input Positive NAND Gates
Equation:	$Y = \overline{ABC}$ (each gate)

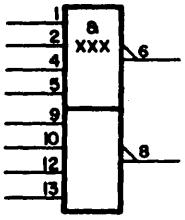


Type (Term name): 7440, 74H40

Element Identifier: 143, 143H

Description: Dual 4-Input Positive NAND Buffers

Equation: $Y = \overline{ABCD}$



NOTE

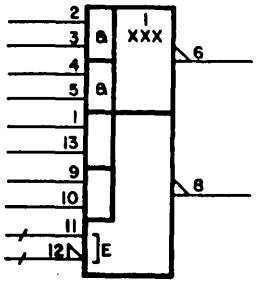
Logic symbol as for type 7420
(element identifier 208)

Type (Term name): 7450, 74H50

Element Identifier: 145, 145H

Description: Dual Expandable 2-Wide 2-In AND-OR-Invert Gates

Equation: $Y = \overline{(AB)+(CD)}$
$XN = \overline{X}$

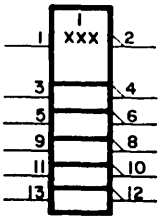


Type (Term name): 7404, 74H04, 74S04

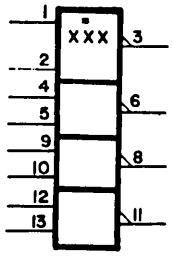
Element Identifier: 146, 146H, 146S

Description: Hex Inverters

Equation: $Y = \overline{A}$ (each inverter)



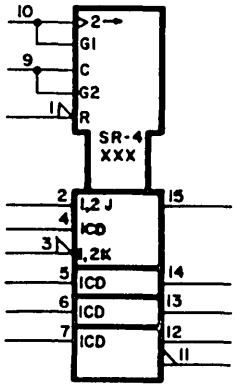
Type (Term name)	7486
Element Identifier:	149
Description:	Quadruple 2-Input Exclusive-OR Gates
Equation:	$Y = A \oplus B$



Type (Term name): 74195/9300

Element Identifier: 159

Description: 4-bit Shift Register



TRUTH TABLE:

t_n		t_{n+1}
J	K	Q_0
L	L	L
L	H	Q_0
H	L	$\overline{Q_0}$
H	H	H

NOTES

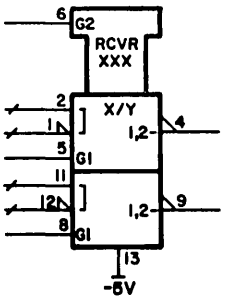
1. A JK input is provided to the first flip-flop in the register similar to conventional JK inputs, except that the low voltage level activates the $\overline{K}$ input.
2. A master asynchronous clear input sets all stages to zero.
3. t_n = bit time before clock pulse
   t_{n+1} = bit time after clock pulse
4. H = logic High, L = logic Low

Type (Term name): 75108

Element Identifier: 162C

Description: Dual Differential Line Receiver

Function: The 75108 is a two-channel line receiver designed to convert input signals of 25 mV or greater to TTL compatible logic levels at an open collector output while rejecting common mode inputs of up to ±3V. Separate and common strobes for the two channels are available.



Type (Term Name): 74154/9311

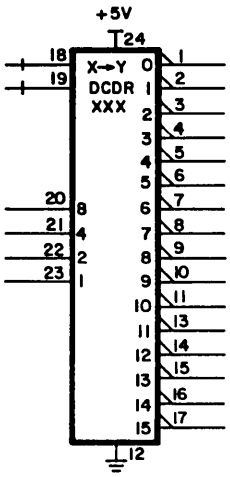
Element Identifier: 167

Description: 1-line to 16-line decoder/demultiplexer

TRUTH TABLE:

INPUTS						OUTPUTS															
G1	G2	8	4	2	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

G1: pin 18; G2: pin 19.
L = logic Low; H = logic High; X = irrelevant.



Type (Term name): 9308

Element Identifier: 168

Description: Dual 4-bit Latch

Function: Allows latched storage. Data can be entered into the latch when both enable inputs are low. If either input goes high the data present in the latch is stored. The master reset overrides all other input conditions: a low at the master reset input forces all outputs of all latches low.

TRUTH TABLE (each latch):

$\overline{R}$	$\overline{C(2)}$	$\overline{C(3)}$	$\overline{CD}$	OUTPUT (Q_n)	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

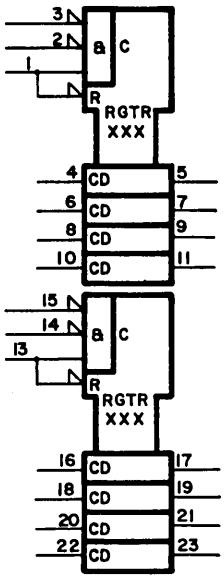
L = logic Low

H = logic High

X = irrelevant

Q_n = present output state

Q_{n-1} = previous output state



Type (Term name): 9309

Element Identifier: 170

Description: Dual four-input multiplexer

Equations: The 9309 is the logic implementation of a two-pole four-position switch. The position of the switch is set by the signals at the two select inputs. The logic equation for the output of each multiplexer is:

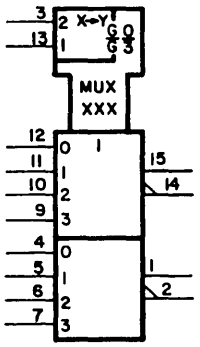
$$Z = I_0\bar{S}_1\bar{S}_0 + I_1\bar{S}_1S_0 + I_2S_1\bar{S}_0 + I_3S_1S_0$$

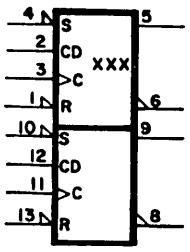
TRUTH TABLE (for each multiplexer):

SELECT INPUTS		INPUTS				OUTPUTS	
S_1	S_2	I_0	I_1	I_2	I_3	Z	$\bar{Z}$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

H = logic High, L = logic Low,

X = irrelevant





Type (Term name): 7474, 74H74

Element Identifier: 175, 175H

Description: Dual D-Type Edge Triggered Flip-Flop

Equation: $Q = \overline{S}+R[CT \cdot D+Q]$

$QN = \overline{R}+\overline{Q}$

NOTE

CT is 1 during the L-H transition of C, otherwise 0.

TRUTH TABLE (each flip-flop):

Synchronous		
t_n	t_{n+1}	
Input	Output	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Asynchronous			
Input		Output	
S	R	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No change	

t_n = bit time before clock pulse

t_{n+1} = bit time after clock pulse

H = logic High, L = logic Low.

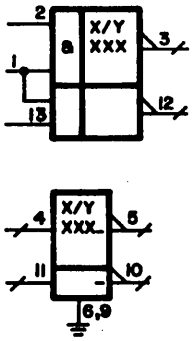
Type (Term name): 75450A

Element Identifier: 180

Description: Dual Peripheral Driver

Function: Contains two standard series 74 TTL gates and two uncommitted high-current high-voltage npn transistors.

Equation (each gate): $C = \overline{AB}$



Type (Term name): 74157/9322

Element Identifier: 189

Description: Multiplexer, Quad 2-Input

Function: Selects four bits of either data or control from two sources. The enable input ($\bar{E}$) is active low. When not activated all outputs are low regardless of all other inputs. This circuit is the logical implementation of a four-pole two position switch, with the position of the switch being set by the signals applied to the one select input.

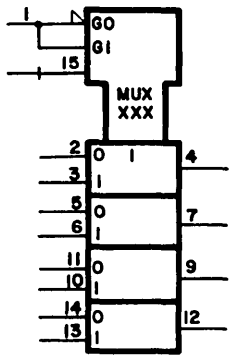
TRUTH TABLE:

Enable	Select Input	Inputs		Output
(pin 15)	G	0	1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

L = logic Low

H = logic High

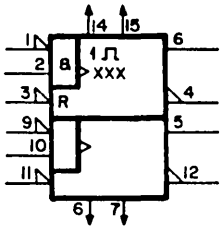
X = irrelevant



Type (Term name): 74123

Element Identifier: 193

Description: Dual retrigger multivibrator.



Note

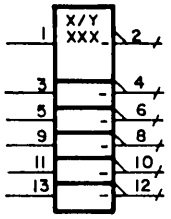
Pins 6, 7, 14 and 15 are for connection to the Timing Network.

Type (Term name): 7406

Element Identifier: 200

Description: Hex Inverter - Buffers/Drivers (Open Collector, High Voltage Output)

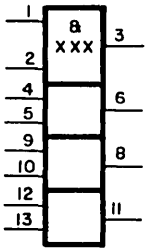
Equation: Y = A (each inverter)



NOTE

Minus (-) sign indicates that the output acts as a load in the High state.

201



Type (Term name): 7408, 74H08

Element Identifier: 201, -

Description: Quadruple 2-Input AND Gates

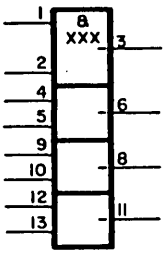
Equation: Y = AB (each gate)

Type (Term name): 7409

Element Identifier: 201C

Description: Quadruple 2-Input Positive AND Gates

Equation: C = AB (each gate)



Type (Term name): 7401, 74H01, 7403

Element Identifier: 202, 202H, 202

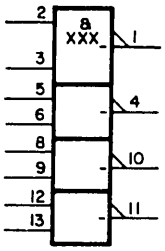
Description: Quadruple 2-Input NAND Gates (Open Collector)

Equation: $Y = \overline{AB}$ (each gate)

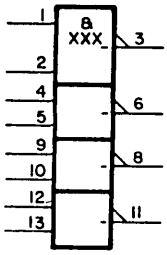
NOTE

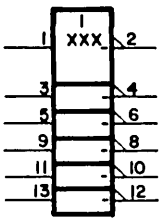
Minus (-) sign indicates that output acts as a load in the High state.

7401, 74H01



7403





Type (Term name): 7405, 74H05

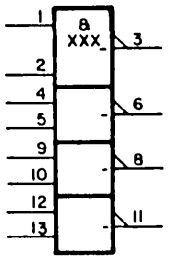
Element Identifier: 203, 203H

Description: Hex Inverters (Open Collector)

Equation: Y = A (each inverter)

NOTE

Minus (-) sign denotes output acts as a load in the High state.



Type (Term name): 7438

Element Identifier: 204

Description: Quadruple 2-Input Positive NAND Buffers (Open Collector)

Equation: $Y = \overline{AB}$ (each buffer)

NOTES

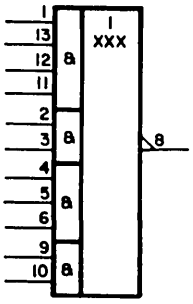
Minus (-) sign denotes output acts as a load in the High output state.

Type (Term name): 74S64

Element Identifier: 205S

Description: 4-2-3-2-Input AND-OR-Invert Gate

Equation: $Y = \overline{ABCD + EF + GHJ + KL}$

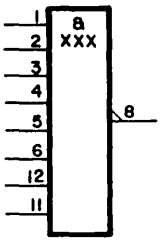


Type (Term name): 7430, 74H30

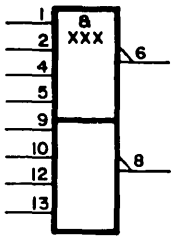
Element Identifier: 206, 206H

Description: 8-Input Positive NAND Gate

Equation: $Y = \overline{ABCDEFGH}$



Type (Term name):	7420, 74H20
Element Identifier:	208, 208H
Description:	Dual 4-Input Positive NAND Gates
Equation:	$Y = \overline{ABCD}$ (each gate)

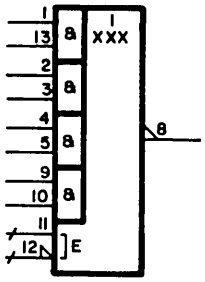


Type (Term name): 7453

Element Identifier: 209

Description: Expandable 4-Wide 2-Input AND-OR-Invert Gates

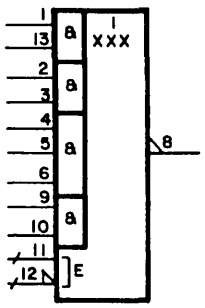
Equation: $Y = \overline{(AB)+(CD)+(EF)+(GH)+(X)}$



NOTE

1. Both expander Inputs (E) may be used simultaneously.

2. X = True Expander Input (Terminal 11).



Type (Term name): 74H53

Element Identifier: 209H

Description: Expandable 4-Wide 2-2-3-2-In AND-OR-Invert Gate

Equation: $Y=\overline{(AB)+(CD)+(EFG)+(HJ)+(X)}$

NOTES

1. Both expander inputs (E) may be used simultaneously.

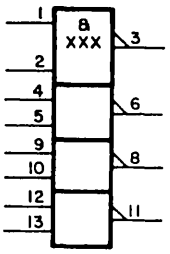
2. X = True Expander Input (terminal 11).

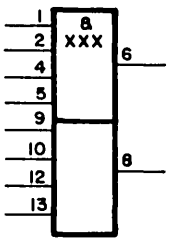
Type (Term name): 7437

Element Identifier: 210

Description: Quadruple 2-Input Positive NAND Buffers

Equation: $Y = \overline{AB}$ (each gate)



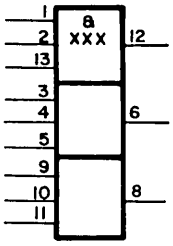


Type (Term name): - 74H21

Element Identifier: - 212H

Description: Dual, 4-Input Positive AND Gates

Equation: Y = ABCD



Type (Term name): 7411, 74H11, 74S11

Element Identifier: - 213H, 213S

Description: Triple 3-Input Positive AND Gates

Equation: Y = ABC (each gate)

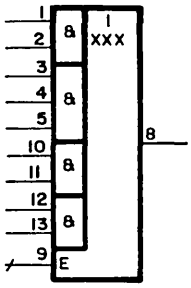
Type (Term name): 74H52

Element Identifier: 217H

Description: 4-Wide 2-3-2-2-In Expandable AND-OR Gate

Equation: Y=(AB)+(CDE)+(FG)+(HI)+(X)

X = Expander (E) Input

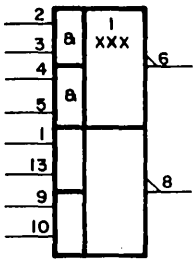


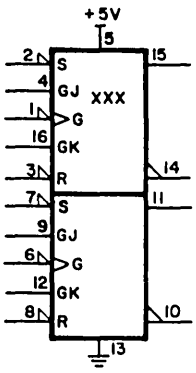
Type (Term name): 7451, 74H51

Element Identifier: - 223H

Description: Dual 2-Wide 2-In AND-OR-Invert Gates

Equation: $Y = \overline{AB + CD}$





Type (Term name): 74106, 74H106

Element Identifier: - 242H

Description: Dual J-K Edge Triggered Flip-Flops

TRUTH TABLE (each flip-flop):

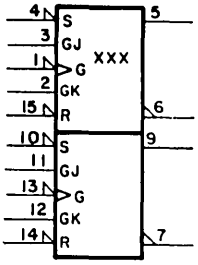
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$

NOTES

t_n = bit time before clock pulse

t_{n+1} = bit time after clock pulse

H = logic High, L = logic Low



Type (Term name): 74S112

Element Identifier: 243S

Description: Dual J-K Flip-Flop

Function: For each flip-flop the outputs change state after the clock pulse transition, depending on the signals at the J-K control inputs.

A low signal at the reset (R) input sets the flip-flop output Q (pins 5 or 9) to low; a low signal at the set (S) input sets the outputs Q to high. The asynchronous set and reset signals override all other inputs.

TRUTH TABLE (each flip-flop):

t_n		t_{n+1}
J_n	K_n	Q_{n+1}
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Qn}$

NOTES

t_n = bit time before clock pulse

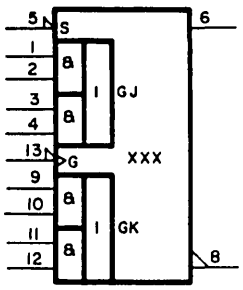
t_{n+1} = bit time after clock pulse

H = logic High, L = logic Low

Type (Term name): 74H101

Element Identifier: 245H

Description: J-K Edge Triggered Flip-Flop



TRUTH TABLE:

t_n		t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Qn}$

NOTES

t_n = bit time before clock pulse

t_{n+1} = bit time after clock pulse

H = logic High, L = logic Low

Type (Term name): 74193/9366

Element Identifier: 500

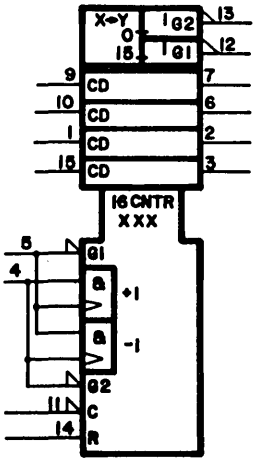
Description: 4-Bit Up-Down Binary Counter

Function: The 74193 is a synchronous 4-bit binary up/down counter which has a parallel load (asynchronous) preset facility. When counting synchronously the outputs change states after the low to high transition of the count-up clock or the count-down clock.

A high signal at the asynchronous master reset input overrides all other inputs and clears the counters.

OPERATING MODES				
R	C	G1	G2	M O D E
H	X	X	X	Preset (Asynchronous)
L	L	X	X	Preset (Asynchronous)
L	H	H	H	No change
L	H	CP	H	Count up
L	H	H	CP	Count down

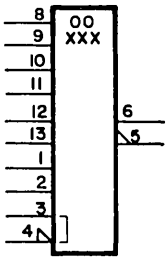
L = logic Low
H = logic High
CP = Clock Pulse
X = irrelevant



Type (Term name): 74180

Element Identifier: 502

Description: 8-bit Odd/Even Parity Generator/Checker



TRUTH TABLE:

	Inputs		Outputs	
$\sum$ of H's AT INPUTS 0 THRU 7	(Pin 3) EVEN	(Pin 4) ODD	(Pin 5) $\sum$ EVEN	(Pin 6) $\sum$ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	L	H	L	L
X	L	L	H	H

L = logic Low

H = logic High

X = irrelevant

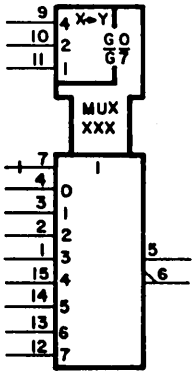
Type (Term name): 74151, 74S151

Element Identifier: 505, 505S

Description: Multiplexer, 8-Input

Equation: $Y = \bar{S}[\bar{A}\bar{B}\bar{C}D_0+A\bar{B}\bar{C}D_1+\bar{A}B\bar{C}D_2+AB\bar{C}D_3+\bar{A}\bar{B}CD_4+A\bar{B}CD_5+\bar{A}BCD_6+ABCD_7]$

S = Strobe



Type (Term name): 74181/9341, 74S181

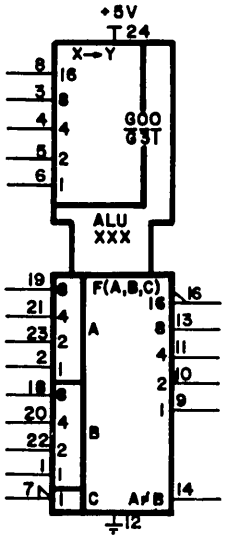
Element Identifier: 509, 509S

Description: Arithmetic Logic Unit (ALU), 4-Bit

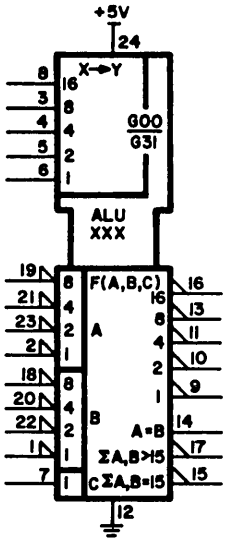
Function: The ALU is controlled by the four Function Select inputs (8,4,2,1) and the Mode Control input (16). It can perform all the 16 possible logic operations or 16 different arithmetic operations.

When the Mode Control input (pin 8) is high, all internal carries are inhibited and the device performs logic operations on the individual bits. When the Mode Control input is low, the carries are enabled and the device performs Arithmetic operations on the two, 4-bit words. The device incorporates full internal look-ahead carry and provides for either ripple carry between devices using output 16, or for carry look-ahead between packages using the signals carry propagate (pin 15) and carry generate (pin 17). Carry propagate and carry generate are not affected by carry in. When speed requirements are not stringent the 74181 can be used in a simple ripple carry mode by the carry out 16 (pin 16) signal to the carry input (C) of the next unit. For high speed operation the 74181 is used in conjunction with the 74182 carry look-ahead circuit. One carry look-ahead package is required for each group of four 74181 devices.

The Function Table (see next page) lists the Arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation.



OR



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FUNCTION TABLE

MODE SELECT INPUTS 8 4 2 1	ACTIVE LOW INPUTS AND OUTPUTS		ACTIVE HIGH INPUTS AND OUTPUTS	
	LOGIC (M = H)	ARITHMETIC** (M = L)(C = H)	LOGIC (M = H)	ARITHMETIC** (M = L)(C = L)
L L L L	$\bar{A}$	A minus 1	$\bar{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L L H L	$\bar{A} + B$	$A\bar{B}$ minus 1	$\bar{A}B$	$A + \bar{B}$
L L H H	Logical 1	minus 1	Logical 0	minus 1
L H L L	$\overline{A + B}$	A plus $(A + \bar{B})$	$\overline{AB}$	A plus $A\bar{B}$
L H L H	$\bar{B}$	AB plus $(A + \bar{B})$	$\bar{B}$	$(A + B)$ plus $A\bar{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L H H H	$A + \bar{B}$	$A + \bar{B}$	$A\bar{B}$	$A\bar{B}$ minus 1
H L L L	$A\bar{B}$	A plus (A + B)	$\bar{A} + B$	A plus AB
H L L H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H L H L	B	AB plus (A + B)	B	$(A + \bar{B})$plus AB
H L H H	A + B	A + B	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\bar{B}$	AB plus A	$A + \bar{B}$	(A + B) plus A
H H H L	AB	AB plus A	A + B	$(A + \bar{B})$ plus A
H H H H	A	A	A	A minus 1

M = Mode Control Input (pin 8)

H = logic High

L = logic Low

* Each bit is shifted to the next more significant position

** Arithmetic operations expressedin 2's complement notation

Type (Term name): 74182/9342

Element Identifier: 510

Description: Look-Ahead Carry Generator

Functions: The 74182 accepts up to four pairs of active low carry-propagate ($\bar{P}0$ thru $\bar{P}3$) and carry-generate ($\bar{G}0$ thru $\bar{G}3$) signals with an active high carry input (Cn). It provides anticipated active high carries (C_{n+X}, C_{n+Y}, C_{n+Z}) across four groups of binary adders; also an active low carry propagate ($\bar{P}$) and carry generate ($\bar{G}$) for further levels of look-ahead.

Equations:

$$C_{n+X} = \overline{G0(\overline{P0} + \overline{C_n})}$$

$$C_{n+Y} = \overline{G1(\overline{P1} + \overline{C_{n+X}})}$$

$$C_{n+Z} = \overline{G2(\overline{P2} + \overline{C_{n+Y}})}$$

$$\bar{G} = \overline{G2 + P2 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0}$$

$$\bar{P} = \overline{P3 \cdot P2 \cdot P1 \cdot P0}$$

Key to Diagram:

Inputs

Symbol	On Diagram	Symbol	On Diagram	Symbol	On Diagram
P0	15	G0	16	C_n	1
P1	240	G1	256		
P2	3840	G2	4096		
P3	60K	G3	64K		

Outputs

Symbol	On Diagram	Symbol	On Diagram
C_{n+X}	16	P	64K-1
C_{n+Y}	256	G	64K
C_{n+Z}	4096		

NOTE
K = 1024

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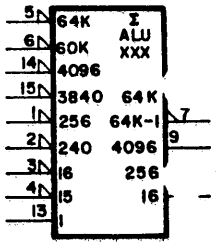
Type (Term name) (Continued): 74182/9342



TRUTH TABLE:

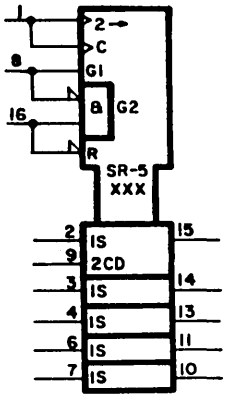
Inputs									Outputs				
C_n	$\bar{G}_0$	$\bar{P}_0$	$\bar{G}_1$	$\bar{P}_1$	$\bar{G}_2$	$\bar{P}_2$	$\bar{G}_3$	$\bar{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	G	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = active High; L = active Low; X = irrelevant.

Type (Term name): 7496/9396

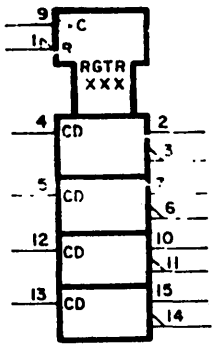
Element Identifier: 515

Description: 5-Bit Shift Register



NOTES

1. A LOW at R clears all flip-flops.
2. Each flip-flop sets High by individual High on S-input and simultaneous High on G1.
3. Contents transferred to output on clock (C) Low→High transition if R=High, S=High.
4. 2CD (terminal 9) = serial input.



Type (Term name): 74175, 74S175

Element Identifier: 520, 520S

Description: Quadruple Storage Register (Latch), D-Type

TRUTH TABLE:

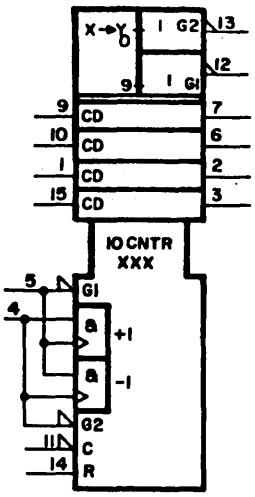
INPUTS			OUTPUTS	
CLEAR	CLOCK	C	Q	$\bar{Q}$
H	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

X = irrelevant; ↑ = Transition from Low to High; H = logic High; L = logic Low; Q_0 = Level of Q before indicated steady state in-out was established.

Type (Term name): 74192/9360

Element Identifier: 523

Description: 4-Bit Binary
Up-Down Counter



Comparing Inputs				Cascading Inputs			Outputs		
A3,B3	A2,B2	A1,B1	A0,B0	A > B	A < B	A = B	A > B	A < B	A = B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H

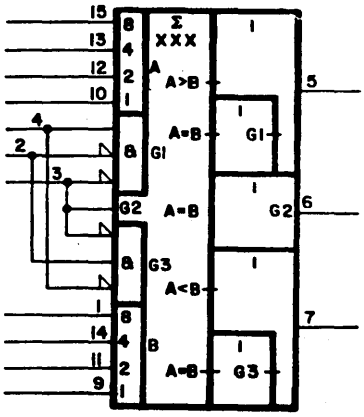
H = active High, L - active Low, X = irrelevant.

Type (Term name): 7485

Element Identifier: 524

Description: 4-Bit Magnitude Comparator

The comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A,B) are made and are externally available at three outputs.



PIN FUNCTION TABLE

Pin	Description/Function		Pin	Description/Function	
1	B3	Data Input	9	B0	Data Inputs
2	A<B	Cascading Inputs	10	A0	
3	A=B		11	B1	
4	A>B		12	A1	
5	A>B	Outputs	13	A2	
6	A=B		14	B2	
7	A<B		15	A3	
8	GND		16	V_{cc}	

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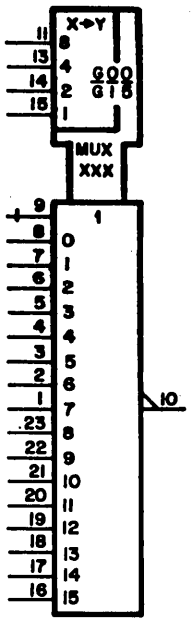
Type (Term name): 74150

Element Identifier: 531

Description: Multiplexor, 16-Input



Type (Term name): 9318

Element Identifier: 532

Description: 8-Input Priority Encoder

Function: The 9318 accepts data from 8 active low inputs and provides a binary weighted representation on 3 active low outputs. A priority is assigned to each input, so that when two or more inputs are active simultaneously, the input with the highest priority is represented at the output. Input line 7 has the highest priority.

A high on the input enable (G) forces all outputs inactive (high) and so allows new data to settle.

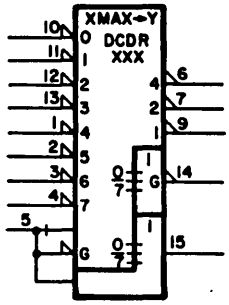
In addition to the data outputs a group signal output (G, pin 14) and an enable output (pin 15) are provided. Output G is active low when any input is low, indicating an active input. The enable output is active low when all inputs are high. Both the output enable and the group signal output are inactive (high) when the input enable is high.

TRUTH TABLE:

Inputs									Outputs					
G	0	1	2	3	4	5	6	7	G	pin 15	1	2	4
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	L	H	H	H
L	X	X	X	X	X	X	X	L	L	H	L	L	L
L	X	X	X	X	X	X	L	H	L	H	H	L	L
L	X	X	X	X	X	L	H	H	L	H	L	H	L
L	X	X	X	X	L	H	H	H	L	H	H	H	L
L	X	X	X	L	H	H	H	H	L	H	L	L	H
L	X	X	L	H	H	H	H	H	L	H	H	L	H
L	X	L	H	H	H	H	H	H	L	H	L	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

NOTES

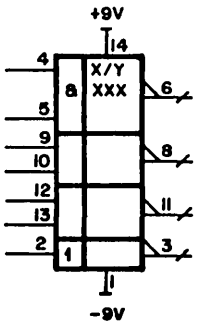
H = logic High,
L = logic Low,
X = irrelevant

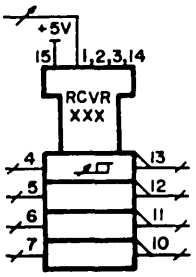


Type (Term name): MC 1488

Element Identifier: 900

Description: Quad Line Driver





Type (Term name): 75154

Element Identifier: 902

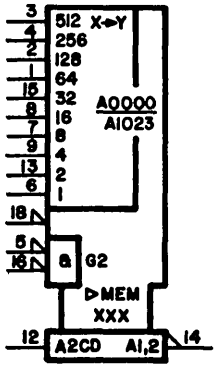
Description: Receiver, Quad Line (RS-232C mode).

Type (Term name): 1103, 1103-1

Element Identifier: - -

Description: 1024 Bit Random Access Memory (RAM)

Function: This is a fully decoded random access 1024 bit memory with non-destructive read-out. All 1024 bits have to be refreshed once in 2 ms (1 ms for 1103-1). A full description and block diagram of the device is given in the Customer Engineering manual for the AB107/AB108 computer, (publication No. 89633300).

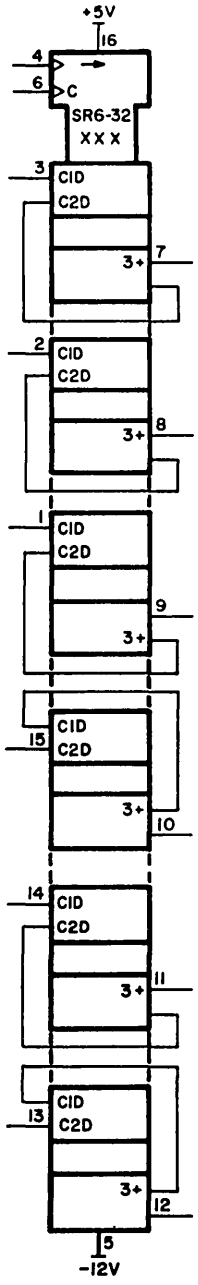


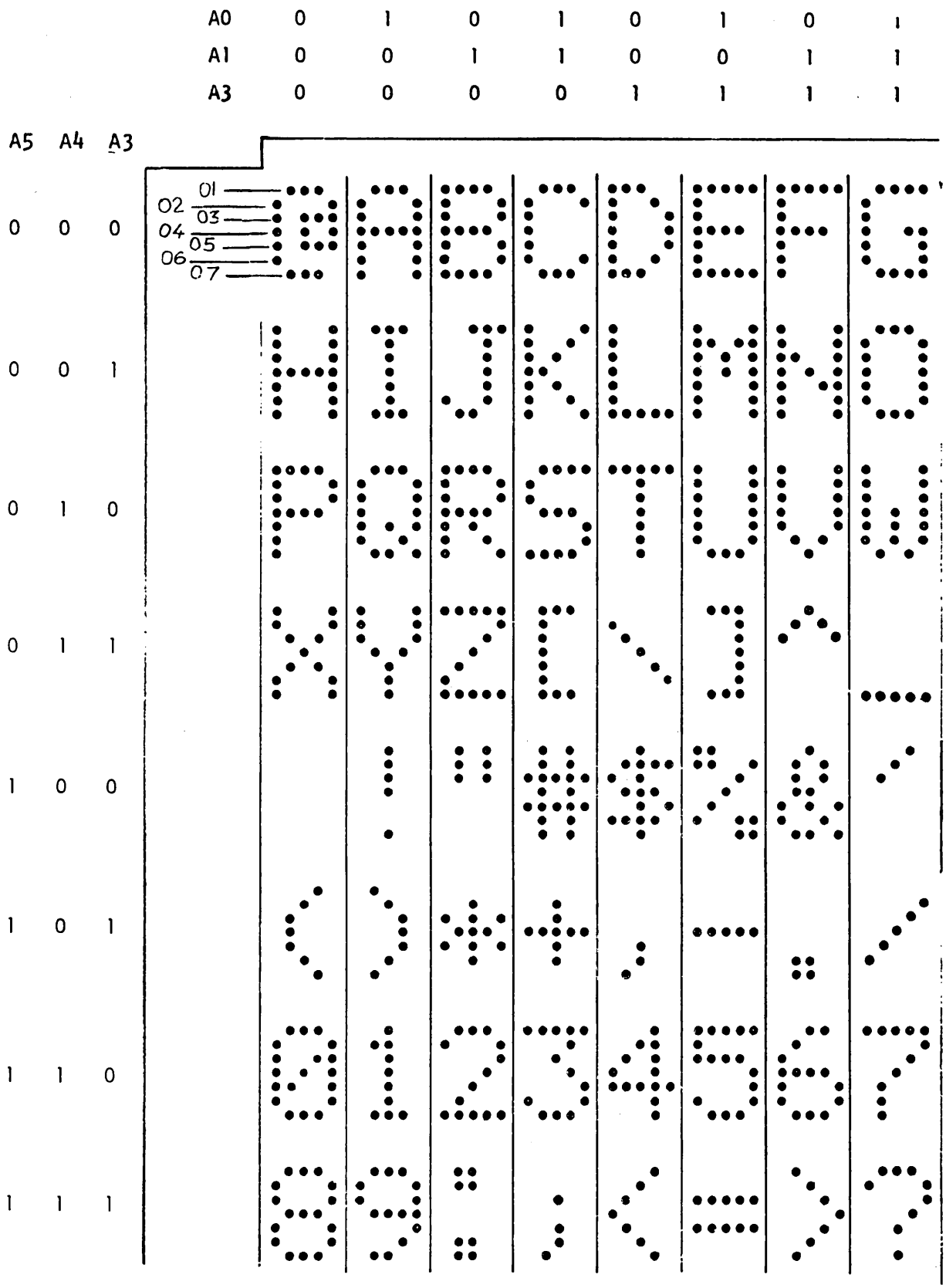
"SYMBOL UNDER REVIEW".

Type (Term name): 2518B

Element Identifier: -

Description: Hex 32-bit
MOS Shift Register





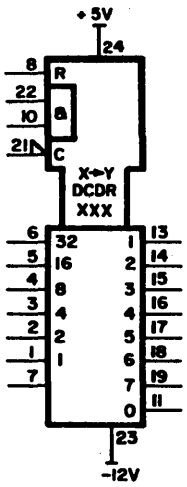
Note: 01 - 07 Outputs
A0 - A5 Address

89723700 A

Type (Term name): 3257A

Element Identifier: -

Description: MOS 64 x 5 x 7
Character Generator



DESCRIPTION OF PIN FUNCTIONS

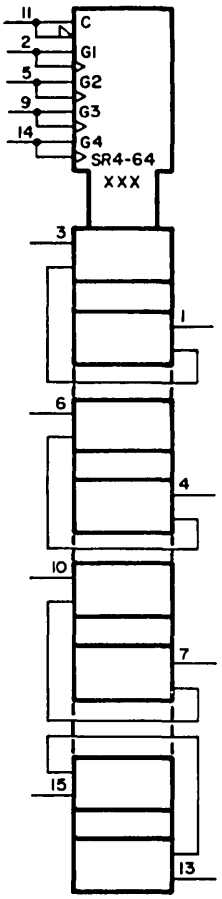
Pin No.	Name	Function
1-6	Address 0-5	Six bits of Address input data
7	Clock Pulse	Input clock pulses which trigger the counter on falling edge.
8	Reset	A low level resets the counter to its last state.
9	Not Connected	
10	Count Control	When high, selects mod 7 resulting in two spaces between characters. When low, mod 6 is selected and only one space will occur between characters.
11	Counter Out	Goes high when the counter reaches its last state.
12	V_{DD} Power Supply	0 Volts
13-19	Output 7-1	Low state indicates output is available
20	Not Connected	
21	Clip Enable	When high, enables the entire chip. When low, the 7 outputs are floated to allow common bussing.
22	Blanking	When low, the outputs will be high, providing blanking independant of the counter state or the character address.
23	V_{GG} Power Supply	-12 Volt Supply
24	V_{SS} Power Supply	+5 Volt Supply

"SYMBOL UNDER REVIEW"

Type (Term name): 3342

Element Identifier: -

Description: Quad 64-bit
MOS Shift Register

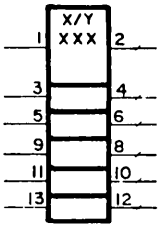


Type (Term name): 7407

Element Identifier: -

Description: Hex Buffers/Drivers (Open Collector)

Equation: Y = A (each buffer)



NOTE

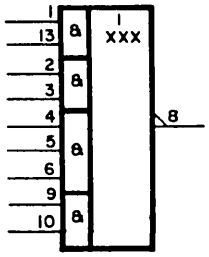
Minus (-) sign indicates that the output acts as a load in the High state.

Type (Term name): 74H54

Element Identifier: -

Description: 4-Wide 2-2-3-2-In AND-OR-Invert Gates

Equation: $Y=\overline{(AB)+(CD)+(EFG)+(HI)}$

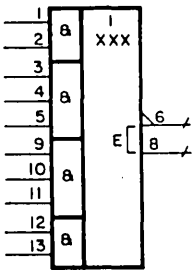


Type (Term name): 74H62

Element Identifier: -

Description: 4-Wide 2-3-3-2-In AND-OR Expander

Equation: $X = \overline{(AB)+(CDE)+(FGH)+(IJ)}$



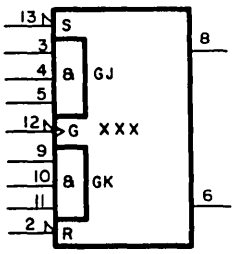
NOTE

Outputs X (terminal 8), $\overline{X}$ (terminal 6) are suitable to drive X and XN inputs of 74H50, 74H53.

Type (Term name): 74H102

Element Identifier: -

Description: J-K Edge-Triggered Flip-Flop



TRUTH TABLE:

t_n		t_{n+1}
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Qn}$

NOTES

t_n = bit time before clock pulse

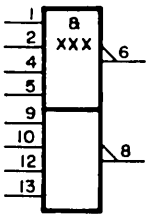
t_{n+1} = bit time after clock pulse

H = logic High, L = logic Low

Type (Term name): 74S140

Element Identifier: -

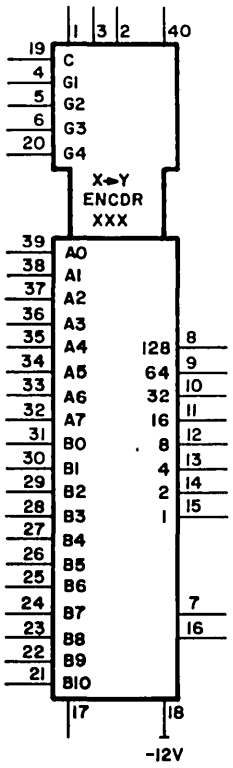
Description: TTL Dual 4-Input
Positive NAND Buffer.



Type (Term name): AY-5-2376

Element Identifier: -

Description: Keyboard Encoder ROM

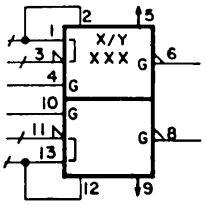


SYMBOL UNDER REVIEW

Type (Term name): DM8820A

Element Identifier: -

Description: Dual Line Receiver



Function: The DM8820A has two independent line receivers. Each has a differential input which responds to small differential signals but rejects large common mode signals; the output is directly compatible with TTL circuits. A low at the strobe input forces the output to high.

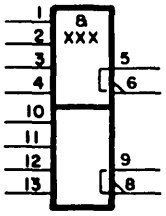
NOTE

Pins 5 and 9:
to response-time capacitor.

Type (Term name): DM8830A

Element Identifier: -

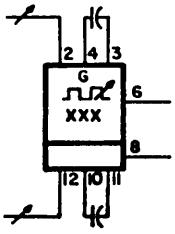
Description: Dual Differential Line Driver



Type (Term name): MC 4024

Element Identifier: -

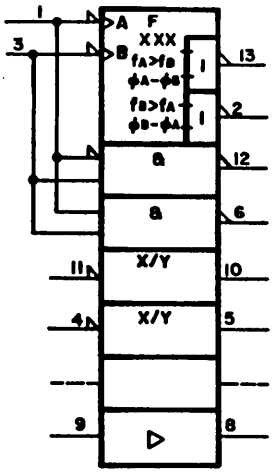
Description: Voltage Controlled Multivibrator



Type (Term name): MC 4044

Element Identifier: -

Description: Phase Detector

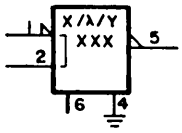


Type (Term name): MOC 1000, MOC 1003

Element Identifier: -

Description: Optical coupler

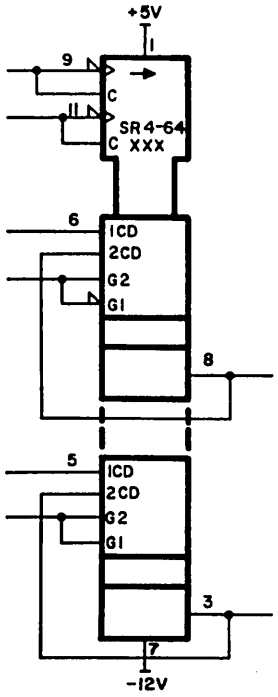
Photo emitting diode and
photo-sensitive transistor.



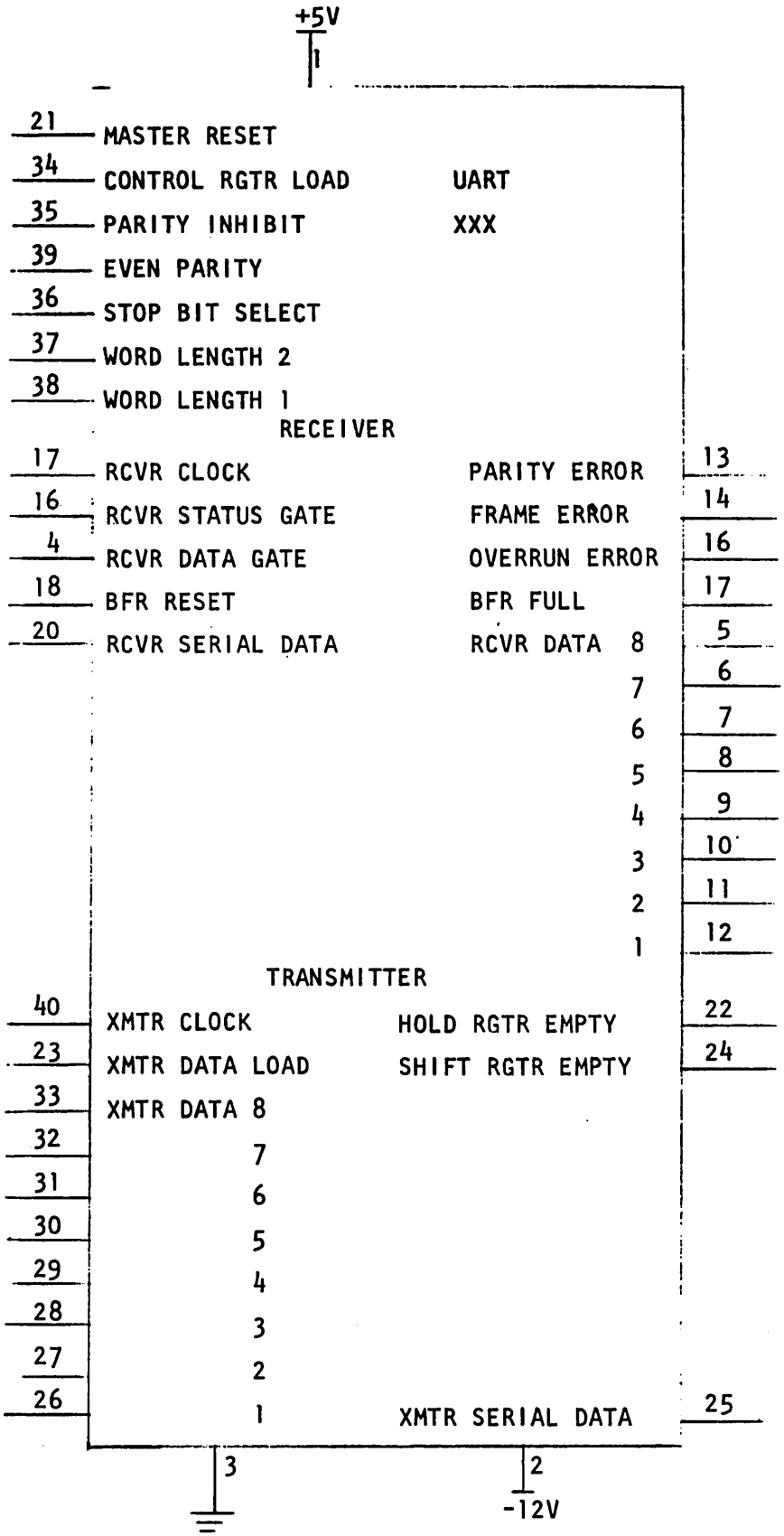
Type (Term name): S1685

Element Identifier: -

Description: Dual 480-bit
MOS Shift Register



SYMBOL UNDER REVIEW



89723700 A

"SYMBOL UNDER REVIEW"

Type (Term name): UAR/T

Element Identifier: -

Description: Universal Asynchronous Receiver/Transmitter

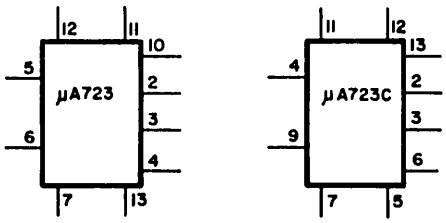
Function: The Universal Asynchronous Receiver/Transmitter (UAR/T) accepts binary characters from either a terminal device or the computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits and either odd/even parity or no parity. The baud rate (bits per word), parity mode and the number of stop bits can be selected externally. All inputs and outputs are directly compatible with MTOS/MTNS logic and also with DTL and TTL. All strobed outputs have tri-state logic.

See next page for pin assignment.

Type (Term name): μA723 , μA723C

Element Identifier: - -

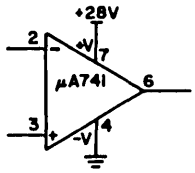
Description: Voltage Regulator



Type (Term name): μA741

Element Identifier: -

Description: Amplifier, Operational
High Performance



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