60346500

CONTROL DATA CORPORATION

CONTROL DATA®
BB372-A
750 NANOSECOND CORE STORAGE MODULE
FV444-A
POWER REGULATOR MODULE

GENERAL DESCRIPTION
THEORY OF OPERATION
DIAGRAMS
PARTS DATA
WIRE LISTS

HARDWARE MAINTENANCE MANUAL

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
BB372-A	A01		Released
FV444-A	A01		Released
	A02	FCO31786	
	A03	ECO32487	

PREFACE

This manual gives Customer Engineering information for the CONTROL DATA® BB372-A Core Storage Module, and the FV444-A Power Regulator Module. Information concerning the storage module appears throughout the manual. An electrical schematic of the FV444-A module is in Section 5. The FV444-A Parts List appears in Section 8.

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SECTION 1

GENERAL DESCRIPTION

GENERAL DESCRIPTION

PHYSICAL DESCRIPTION

The BB372-A is a 2-1/2 Dimension type core storage module utilizing TTL logic. The module is 12.4 inches by 6.8 inches by 2.0 inches. Data, address, and control signals to and from the module are of the single-ended TTL transmission type. The storage module and the FV444 Power Regulator Module together require the following power:

Voltage	Amperage
+5 V	3.5 A
-5 V	4.2 A
+30 V	5.0 A

FUNCTIONAL DESCRIPTION

The storage module provides load, store, and load-modify-store capability for 4096, 18-bit words. A memory protect feature, which disables the write function for protected addresses, is built into the control logic. The module has a 12-bit address register, and an 18-bit data input and data output register. Read access time is about 350n/sec, and total cycle time is about 750 n/sec.

SECTION 2

OPERATION AND PROGRAMMING

(Not Applicable)

SECTION 3

INSTALLATION AND CHECKOUT

INSTALLATION AND CHECKOUT

INSTALLATION

Plug the storage module into the back panel and tighten the two thumbnuts. Refer to Figure 5-1 to determine the top of the module, if in doubt.

CHECKOUT

Checkout procedures are determined by the equipment using the module.

SECTION 4

THEORY OF OPERATION

THEORY OF OPERATION

INTRODUCTION

The storage unit covered in this section is a modified type of linear-select core memory known as a 2 1/2 Dimension memory. This section describes 2 1/2 Dimension memories in general, and the logical and physical makeup of this storage module in particular.

2 1/2 DIMENSION MEMORIES

Figure 4-1 shows corresponding Linear Select (2 D) and 2 1/2 Dimension (2 1/2 D) memories. Both of the memories illustrated can store eight, three bit words.

The 2 D memory shown in Figure 4-1 has 24 cores arranged in a 3 x 8 matrix. Note that there is one word line for each address, and one digit line and one sense line for each bit position.

In the 2 D memory, a three bit address is decoded to select one of eight word lines. During a Read cycle, read word current flows in the selected word line to switch the flux of any cores on that word line that are storing a "1" from the "1" state to the "0" state. Cores storing a "0" do not have their flux switched as a result of word read current. A sense amplifier in each bit position samples the voltage in the sense line to detect whether or not the core that is common to the word line and the sense line switches (indicating a "1") during the Read cycle.

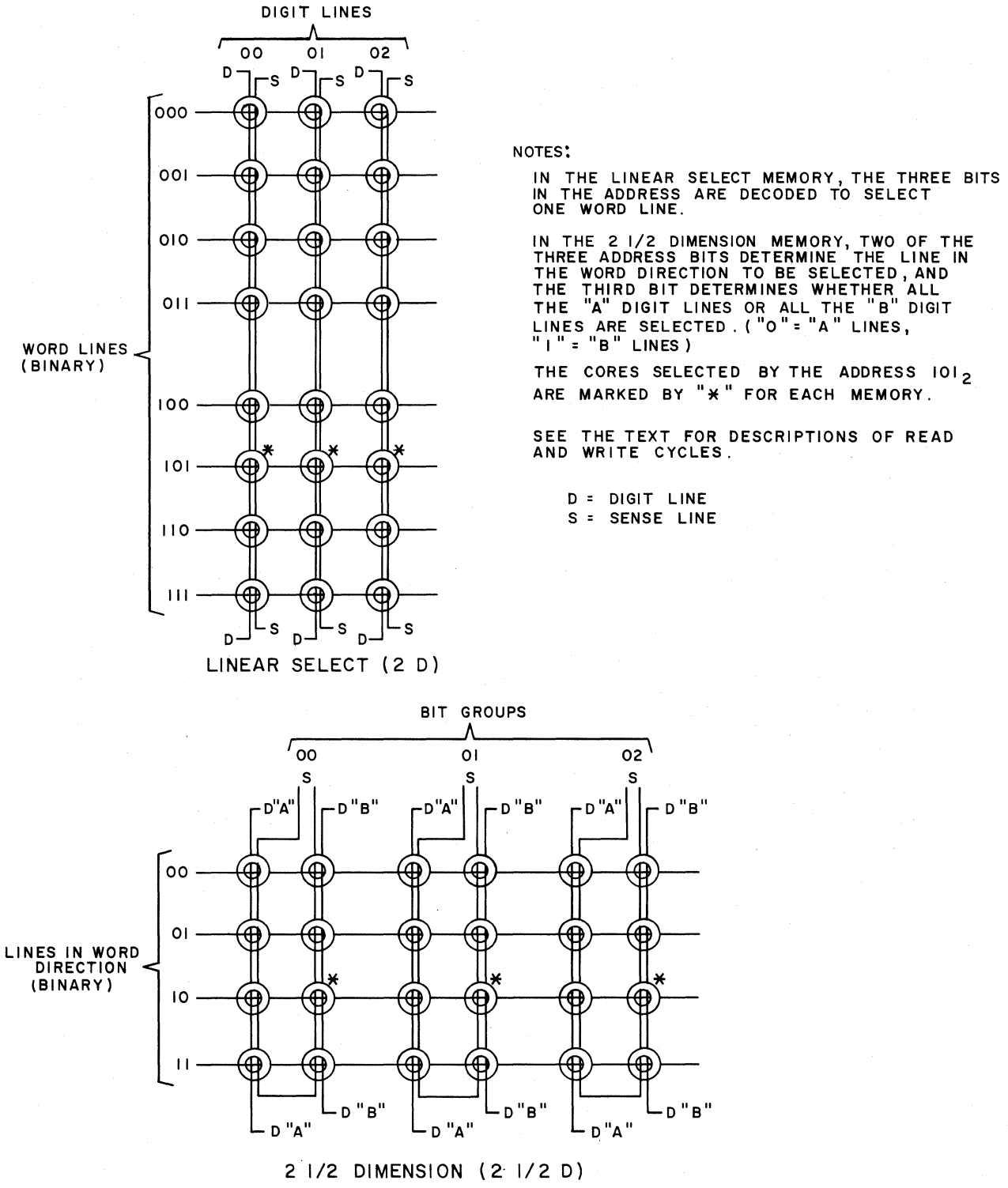


Figure 4-1. Corresponding Linear Select and 2 1/2 Dimension Core Memories

During the Write cycle, write word current flows in the direction opposite read word current. At the same time, the current in each digit line flows in a direction to augment write word current if a "1" is to be written, or to inhibit write word current if a "0" is to be written. Thus, cores storing a "1" have their flux switched from the "0" state to the "1" state, while cores storing a "0" have their flux unchanged.

The 2 1/2 D memory shown in Figure 4-1 also has 24 cores, but they are arranged in a 6 x 4 matrix. Note that each of the four lines in the word direction is used for two addresses, and that there are two digit lines and one sense line for each bit group. Thus, this 2 1/2 D memory in effect divides the word dimension of the 2 D memory by two, while it multiplies the bit dimension of the 2 D memory by two. The 2 1/2 D memory in the example is said to have a lower aspect ratio (word dimension/bit dimension) than the 2 D memory. This means that the core array of the 2 1/2 D memory is more square than the core array of the 2 D memory.

In the 2 1/2 D memory shown, two of the three address bits are decoded to select one of the four lines in the word direction. The third address bit selects one of the two digit lines in each bit group. During the Read cycle, all address selected digit lines (in the example, this would be either all the "A" or all the "B" digit lines) receive read digit current in a direction that augments the read current flowing in the selected line in the word direction. This combination of currents causes the flux to switch only in cores which are in the "1" state and lie at the intersections of selected digit lines and the selected line in the word direction. For each bit group, a sense amplifier detects the presence or absence of a switching core through a sense line which threads all the cores in the bit group. After the Read cycle, all cores at the intersection of the selected line in the word direction and selected digit lines have their flux in the "0" state.

During the Write cycle, write word current (which always flows in the opposite direction of read word current) flows in the line in the word direction selected by the address. At the same time, write digit current (which flows in the opposite direction of read digit current) flows in the address selected digit lines of bit positions that are to store a "1". These write digit currents interact with write word current to switch the flux of the cores from the "0" to the "1" state. During the Write cycle, no digit current flows in digit lines which pass through cores that are to store a "0", and the write word current alone is not of sufficient magnitude to switch a core from the "0" state.

The 2 1/2 D memory shown in Figure 4-1 multiplies the bit dimension of its corresponding 2 D memory by two. The storage module described next in this section multiplies the bit dimension of an equivalent 2 D memory by eight, yielding a core array of 144 x 512 working cores. Its corresponding 2 D memory would have a core array of 18 x 4096 cores.

4096 WORD, 18 BIT, 2 1/2 D STORAGE MODULE

Although this storage module is much larger than the one in Figure 4-1, it retains many of the principles outlined there. The following paragraphs describe in detail the various functional units which make up the 4K module.

CORE ARRAY

The cores (21 mil O. D., 14 mil I. D.) are arranged in two planes, each plane containing a 144 x 256 matrix of data storing cores. (There is also a row of cores around the edge of each plane which protects data storing cores during the fabrication process. These cores will be ignored in future discussions.) Both planes are divided into 18 vertical core groups, each group being 8 cores wide by 256 cores long. A vertical core group on plane 0 and its counterpart in plane 1 are considered to be a bit group (8 cores by 512 cores). Each of the 4096 cores in a bit group acts as a storage element for the same relative bit in the 4096 memory words. For example, the cores for bit 00 of address 0000, bit 00 of address 1000, and bit 00 of address 4096 are all in the same bit group.

Each core in the memory has three lines passing through it: a line in the word direction (hereinafter called an X line); a digit line (hereinafter called a Y line); and a sense line. (See Figure 4-2). The 256 X lines are threaded horizontally, each one passing through a total of 288 cores (144 in each plane). The 144 Y lines are threaded vertically, each one passing through 512 cores (256 in each plane). Each of the 18 sense lines threads all 4096 cores in one bit group.

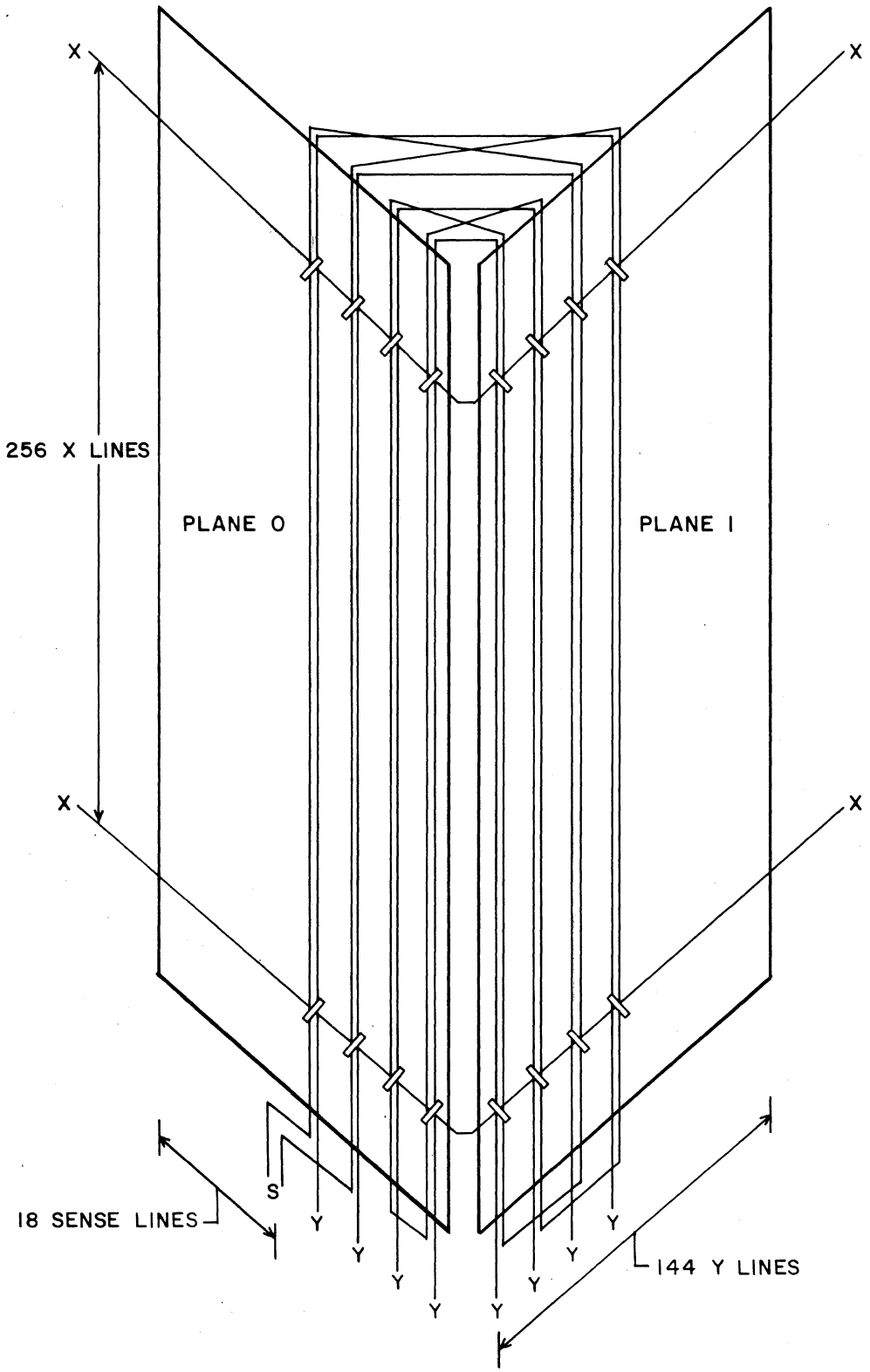


Figure 4-2. X Line, Y Line, and Sense Line Threading

DECODE-DRIVE SYSTEM

Figure 4-3 shows the X and Y decode-drivers which select and supply read and write current to the group of 18 cores specified by the address. X decode-drivers send current through one of 256 X lines. The phase of X current is determined by the address. Y decode-drivers select one of eight Y lines in each bit group to receive Y current.

X Decode-Drive: Phase Selection

Besides selecting one of 256 X lines, the X decode-drive system determines the phase of read and write currents. Figure 4-4 shows how the phase of the read or write X current determines the plane of the addressed word. Y read current (Y_R) augments X read current (X_{R0}) in plane 0 and inhibits X_{R0} in plane 1. The augmented read current (Y_R+X_{R0}) is sufficient to switch the core it passes through, (if the core is in the "1" state) while the inhibited read current (Y_R-X_{R0}) has no significant effect upon the core it passes through. When the phase of the X read current is reversed, (X_{R1}) the core in plane 0 receives inhibited read current, (Y_R-X_{R1}) while the core in plane 1 receives augmented read current (Y_R+X_{R1}).

Phase selection is used during the Write cycle also, with X and Y write currents flowing in the opposite direction of their corresponding read currents. However, when a "0" is to be written in a bit position, no Y write current (Y_W) flows in the address-selected Y line for that bit position.

Expanding the previous examples, note that the phase of the X current determines which of the two words with the same X-Y address receives augmented read and write currents.

X Decode-Drive: X Line Selection

The X decode-drive subsystem selects and drives one of 256 X lines according to nine address bits. Figure 4-5 shows the X decode-drive logic for one X line. Bit 00 of the address interacts with read-write control logic to determine the phase of X currents. Bits 01, 02, 04, and 05 from the address register feed a decoder which enables one of 16 X line drivers. The enabled line driver, under phase and timing control, applies either X drive voltage or ground to 16 X lines through a pair of discrete diodes.

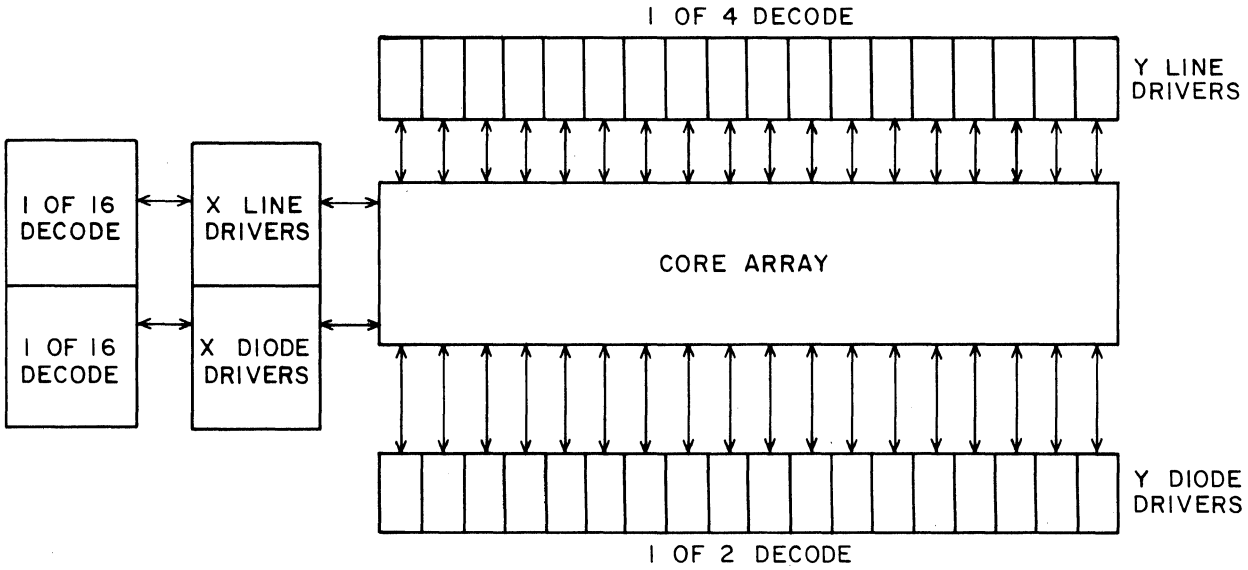
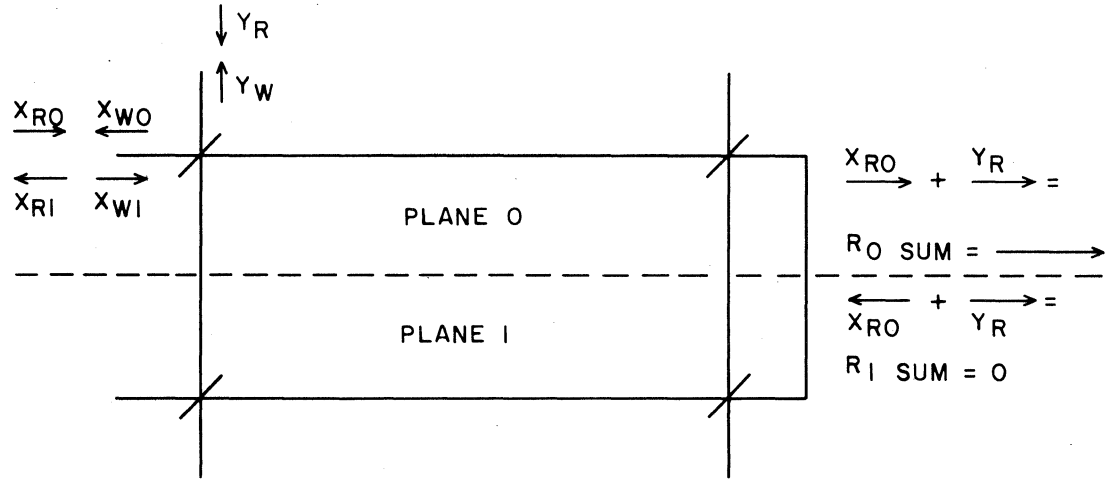


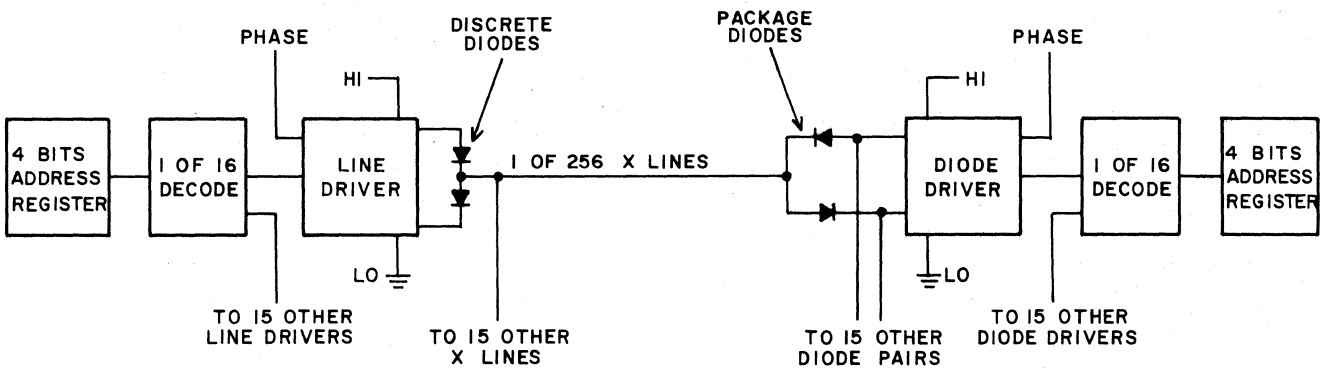
Figure 4-3. Drive System Block Diagram



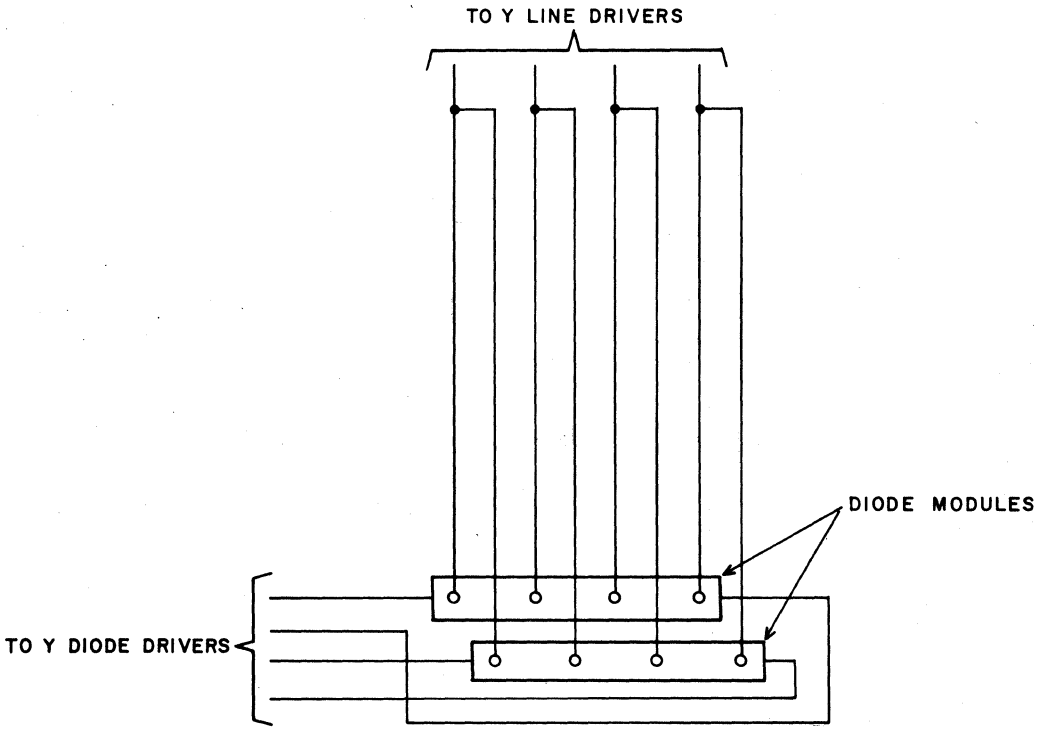
R_O SUM = TOTAL READ CURRENT PASSING THROUGH CORE IN PLANE 0 ON SELECTED X AND Y LINES.

R_I SUM = TOTAL READ CURRENT PASSING THROUGH CORE IN PLANE 1 ON SELECTED X AND Y LINES.

Figure 4-4. Phase Selection of X Currents



X DECODE- DRIVE FOR ONE X LINE



Y DRIVE LINES FOR ONE BIT GROUP

Figure 4-5. X and Y Drive Subsystems

Bits 03, 06, 07, and 08 from the address register feed another decoder which enables one of 16 X diode drivers. The enabled diode driver, also under phase and timing control, applies either ground or X drive voltage to 16 X lines through 16 pairs of diodes (in four packages).

X lines are connected to pads on the line side of the core array, and to diode packages on the diode side. They are connected such that each X line is common to one line driver and one diode driver. Thus, when one line driver is applying X drive voltage to a group of 16 X lines, and one diode driver is applying ground to a group of 16 X lines, (or vice-versa) one X line conducts X drive current.

Y Decode-Drive: Y Line Selection

During Read cycles, the Y decode-drive subsystem supplies Y read current to all address selected Y lines. During Write cycles, the subsystem supplies Y write current only to those address selected Y lines which are to store a "1". (Data register outputs enable only diode drivers that are to write "1's").

Each of the 18 bit groups has four Y line drivers and two Y diode drivers. As shown in Figure 4-5, each Y line is common to one line driver and one diode driver. Thus, when one Y line driver and one Y diode driver apply Y drive voltage and ground, respectively, to their Y line groups, one of the eight Y lines in each bit group conducts drive current. The direction of Y drive current depends on whether a read or a write is being performed.

For all bit groups, address bits 09 and 10 select the Y line drivers, and bit 11 selects the Y diode drivers. (Each address selects 18 line driver/diode driver pairs).

SENSE SYSTEM

The sense system in the module consists of 18 sense lines, 18 sense amplifiers, and an 18-bit data register.

Each of the sense lines threads all 4096 cores in a bit group. Sense lines are twisted between planes (Figure 4-2) to prevent inductive coupling to Y lines.

Sense amplifiers are of the amplitude sensing type, so they detect sense line voltages of either polarity. When strobed, sense amplifiers convert sense line voltages to TTL logic levels, and then feed (through inverters) the pre-set inputs of the data register.

The data register receives data from data input lines, (clocked input) and from sense amplifiers (pre-set input). Q outputs of the data register feed data output lines, and $\overline{Q}$ outputs feed Y diode drivers.

CONTROL LOGIC

Control logic provides control and timing signals to the functional units of the memory in response to input commands. A tapped delay line coupled to a NAND gate generates the primary oscillating signal which clocks timing chain flip-flops. Timing chain Q outputs interact with control signals to initiate and terminate memory functions.

SECTION 5

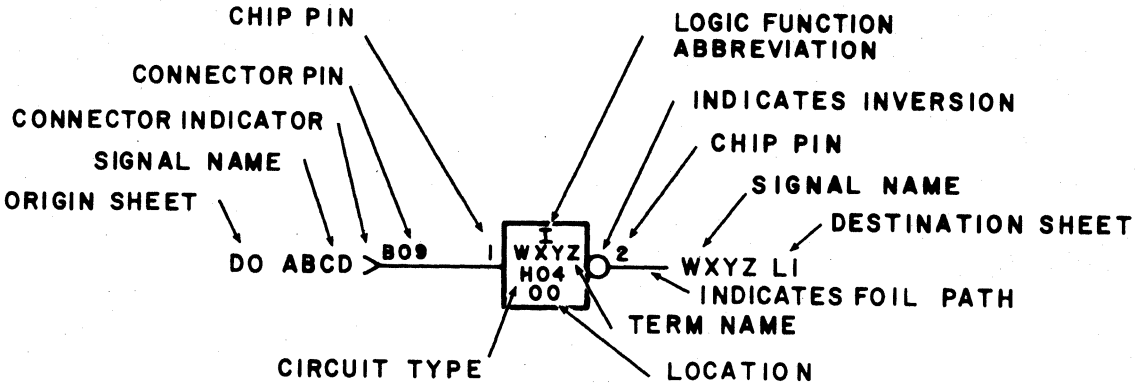
DIAGRAMS

KEY TO LOGIC SYMBOLS

Signal Index

	Mnemonic	Definition
Interface signals	DO00-DO17	Output data bits 00-17
	DI00-DI17	Input data bits 00-17
	S00-S11	Address inputs
	MPTB	Memory protect bit
	MPTE	Memory protect enable
	MREQ	Memory request
	MBSY	Memory busy
	MDRDY	Memory data ready
	STORE	Store command
	LMS	Load-modify-store
	CONT	Continue store cycle of LMS
	MC	Master clear
Internal signals	MDSC	Matrix driver source collector voltage
	CLD0	Clear data register
	CLRD	Clear read register, diode side
	CLRL	Clear read register, line side
	CLWD	Clear write register, diode side
	CLWL	Clear write register, line side
	DDSC	Diode driver source collector voltage
	MCR	Master clear to regulator
	KARA	Clock address register, signal A
	KARB	Clock address register, signal B
	KDR0	Clock data register
	SRD0	Set term RDD0
	SRL0	Set term RDL0
	SRDA	Set term RDDA
	SRLA	Set term RDLA
	STB0	Strobe sense amplifiers
	SWD	Set write register, diode side
	SWL	Set write register, line side
	$\overline{\text{DO00-DO17}}$	Not output data bits 00-17

Typical Logic Element



NOTE

Origin and destination sheets are given only for internal signals. The absence of an origin or destination sheet identifier indicates that the signal in question has an origin or destination outside the storage module.

Abbreviations on Logic Elements

A	=	And
DCDR	=	Decoder
DEL	=	Delay line
I	=	Inverter
MD	=	Memory driver
OR	=	Or
REG	=	Register
SA	=	Sense amplifier

Term Name

Each logic element in the storage module has a unique term name to distinguish it from other elements.

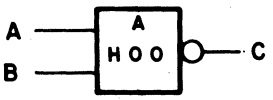
CIRCUIT TYPE

A circuit type indicator appears on each logic element. Table 5-1 cross-references circuit types with manufacturers' part numbers. Brief descriptions of each circuit type follow Table 5-1.

TABLE 5-1. CIRCUIT TYPES VS. PART NUMBER

Circuit Type	CDC Number	TI Number	Motorola Number	Fairchild Number
H00	36188701	74H00	3000	9H00
H04	52335600	74H04	3008	9H04
H20	52335700	74H20	3010	9H20
H50	52335800	74H50	3020	9H50
H74	52335900	74H74	3060	9H74
N95	52335500	7495		995
N154	52337100	74154		
D25	52312201	7525		
D325	52336100	75325		

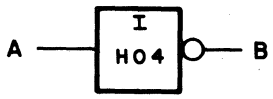
H00: 2-Input positive NAND gate. (Four per package.)



$C = \overline{AB}$

When both inputs are "1", the output is "0".
When either or both inputs are "0", the output is "1".

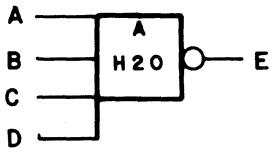
H04: Inverter. (Six per package.)



$B = \overline{A}$

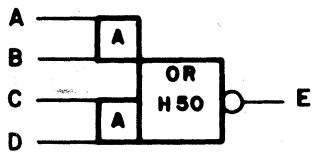
A "1" input gives a "0" output.
A "0" input gives a "1" output.

H20: 4-Input positive NAND gate. (Two per package.)



$E = \overline{ABCD}$

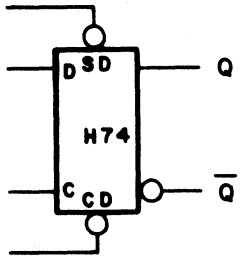
When all inputs are "1", the output is "0".
When any input is "0", the output is "1".



H50: 2-Wide, 2-Input AND-NOR gate. (Two per package.)

$E = \overline{(AB) + (CD)}$

When both inputs of either AND gate are "1", the output is "0". When at least one input of both AND gates is "0", the output is "1".

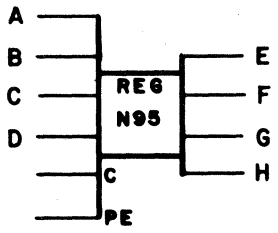


H74: D-type, edge-triggered flip-flop. (Two per package.)

A "1"-going clock pulse applied to the C input enables the bit present at the D input into the flip-flop. The Q and $\overline{Q}$ outputs provide true and inverted outputs, respectively.

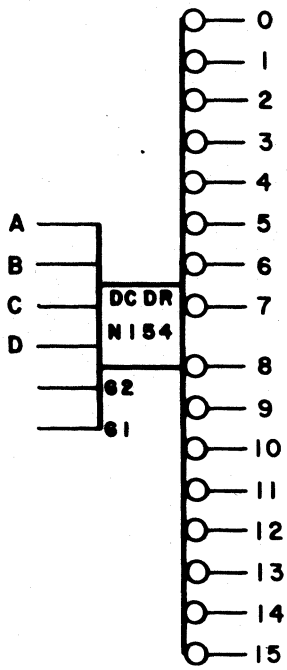
A "0"-going pulse applied to the SD input unconditionally sets the flip-flop. (Q goes to "1", $\overline{Q}$ goes to "0".)

A "0"-going pulse applied to the CD input unconditionally clears the flip-flop. (Q goes to "0", $\overline{Q}$ goes to "1".)



N95: 4-Bit register (parallel, shift). (One per package.)

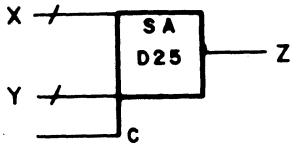
In this equipment, the N95 circuit is used as a parallel holding register, so the PE (parallel enable) input is held at constant "1". A "0"-going clock pulse applied to the C input enables data from A, B, C, D into the register. E, F, G, H reflect the states of A, B, C, D at the time of the clock pulse. Outputs remain stable until the next clock pulse.



N154: 4-Bit to 16 line decoder (gated). (One per package.)

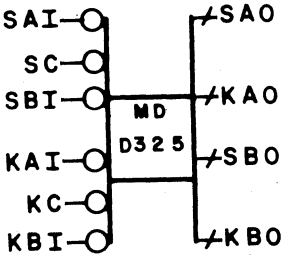
In this equipment, the N154 circuit is used only as a decoder, so the strobe/gate inputs, G1, and G2, are grounded. The circuit performs a one-of-16 decode of A, B, C, D (A is the least significant bit). The selected output is "0", and all other outputs are "1". The relationship between inputs and outputs is as follows:

DCBA	SELECTED OUTPUT	DCBA	SELECTED OUTPUT
0000	0	1000	8
0001	1	1001	9
0010	2	1010	10
0011	3	1011	11
0100	4	1100	12
0101	5	1101	13
0110	6	1110	14
0111	7	1111	15



D25: Amplitude-sensing, TTL output sense amplifier. (Two per package.)

This circuit outputs a "1" from Z when a strobe pulse is applied to C at the same time that a voltage difference occurs across X and Y. The circuit outputs "0" at all other times.



D325: Source-sink memory driver. (Two per package.)

See Figure 5-2 for a logic schematic of this circuit.

The circuit supplies source or sink voltage to the outputs according to enabling (--I) and strobe (-C) inputs. Since the strobe inputs are common to both drivers, a single logic symbol represents both of them. The following table shows the necessary input conditions for active outputs.

Input Conditions	Active Output	Notes:
SAI = "0", SC = "0"	SAO	S = source
KAI = "0", KC = "0"	KAO	K = sink
SBI = "0", SC = "0"	SBO	A = driver "A"
KBI = "0", KC = "0"	KBO	B = driver "B" I = input enable O = output C = input clock

Logic Levels (TTL)

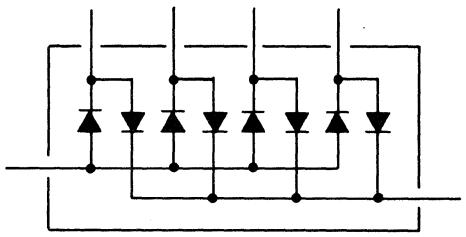
"1" = +3.5 v. nominal
"0" = +0.2 v. nominal

Test Points

x = test point number.

DIODE PACKAGES

All X and Y lines are connected on one end to diode package terminals. Each package contains four pairs of diodes as shown.



DIODE MODULE

DIAGRAM-BOARD RELATIONSHIP

Diagram sheets D0 and D1 show logic on the control and diode driver board, sheets L0 and L1 show the logic on the line driver board, and sheet S0 shows sense board logic. Figure 5-1 shows where these boards are located in the memory.

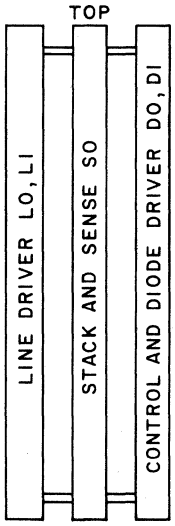


Figure 5-1. Storage Module Board Locations, Front View
(View from card side of chassis)

SHEET B1

The following paragraphs are keyed to the block diagram, which shows the relationship of major storage module sections.

Load Function

The module receives a 12-bit address and a MEMORY REQUEST signal. The MEMORY REQUEST signal starts the timing chain which controls all functions. The X-drive section decodes nine of the address bits to select one X line and the phase of X currents. The Y-drive section decodes the remaining three address bits to select one of eight Y lines in each of the 18-bit groups. Read currents on the selected X and Y lines interact to sweep the stored data from the core array to the data register via the sense system. The data register feeds the output data lines while it enables Y drivers to rewrite the data into the selected address.

Store Function

When the module receives a 12-bit address, a MEMORY REQUEST, and a STORE command, it performs a read as in the Load function. However, before enabling the Y drivers, the module replaces the sense data in the data register with the data to be stored (Input Data). The module then stores the contents of the data register at the selected address.

Load-Modify-Store Function

When the module receives a LOAD-MODIFY-STORE command, a 12-bit address, and a MEMORY REQUEST, it performs a read and halts. At this time, the word that was stored at the selected address is in the data register (and on the output data lines). Upon receipt of a CONTINUE, the module replaces the word in the data register with a new word from the input data lines, and stores this new word at the selected address.

Memory Protect Feature

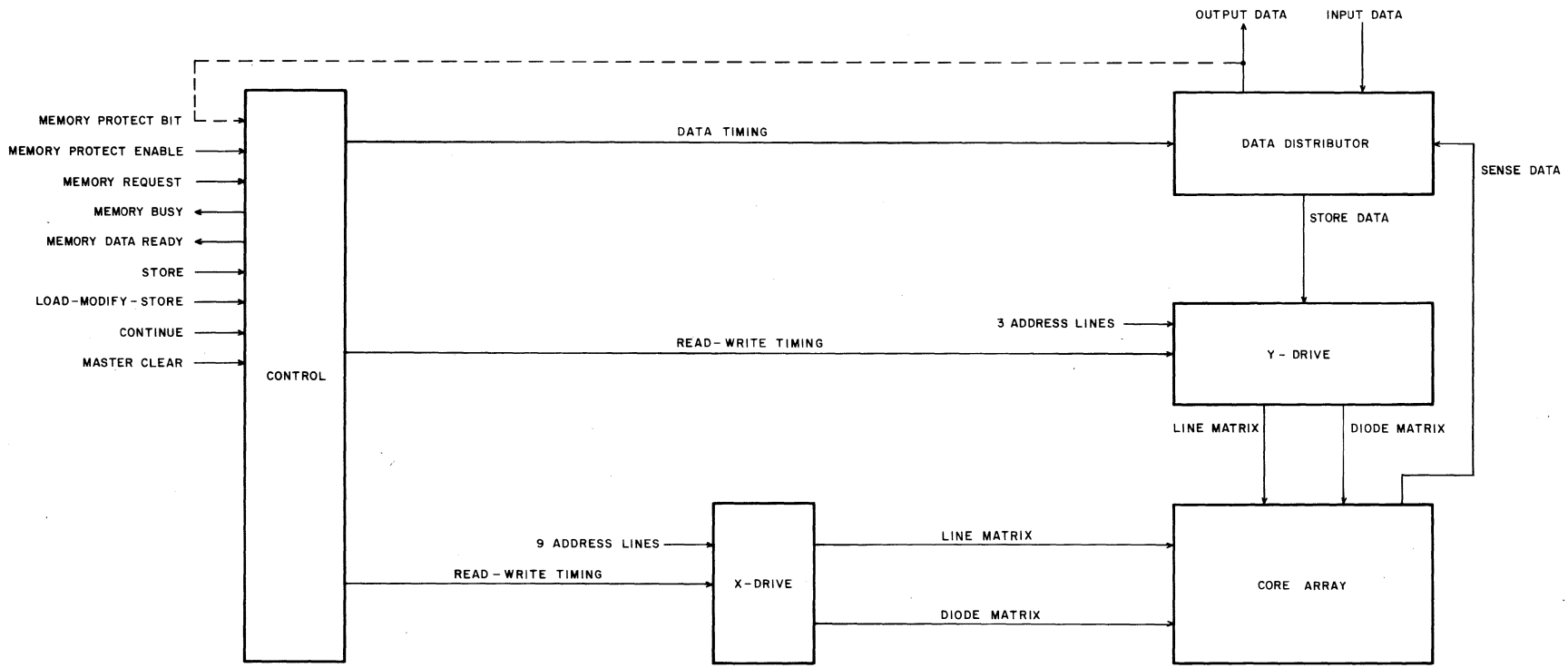
The MEMORY PROTECT ENABLE and MEMORY PROTECT BIT inputs provide read-only capability for certain addresses. (If this feature is not needed, both MPTE and MPTB inputs should be grounded). When the feature is used, one of the 18 bits in the memory word functions as the MEMORY PROTECT BIT. This bit is a "1" for all read-only addresses. When the MPTE and the MPTB are both "1", STORE and CONTINUE commands are disabled, causing the data register to accept data only from sense amplifiers. When either or both MPTE and MPTB are "0", the module functions normally.

Memory Status

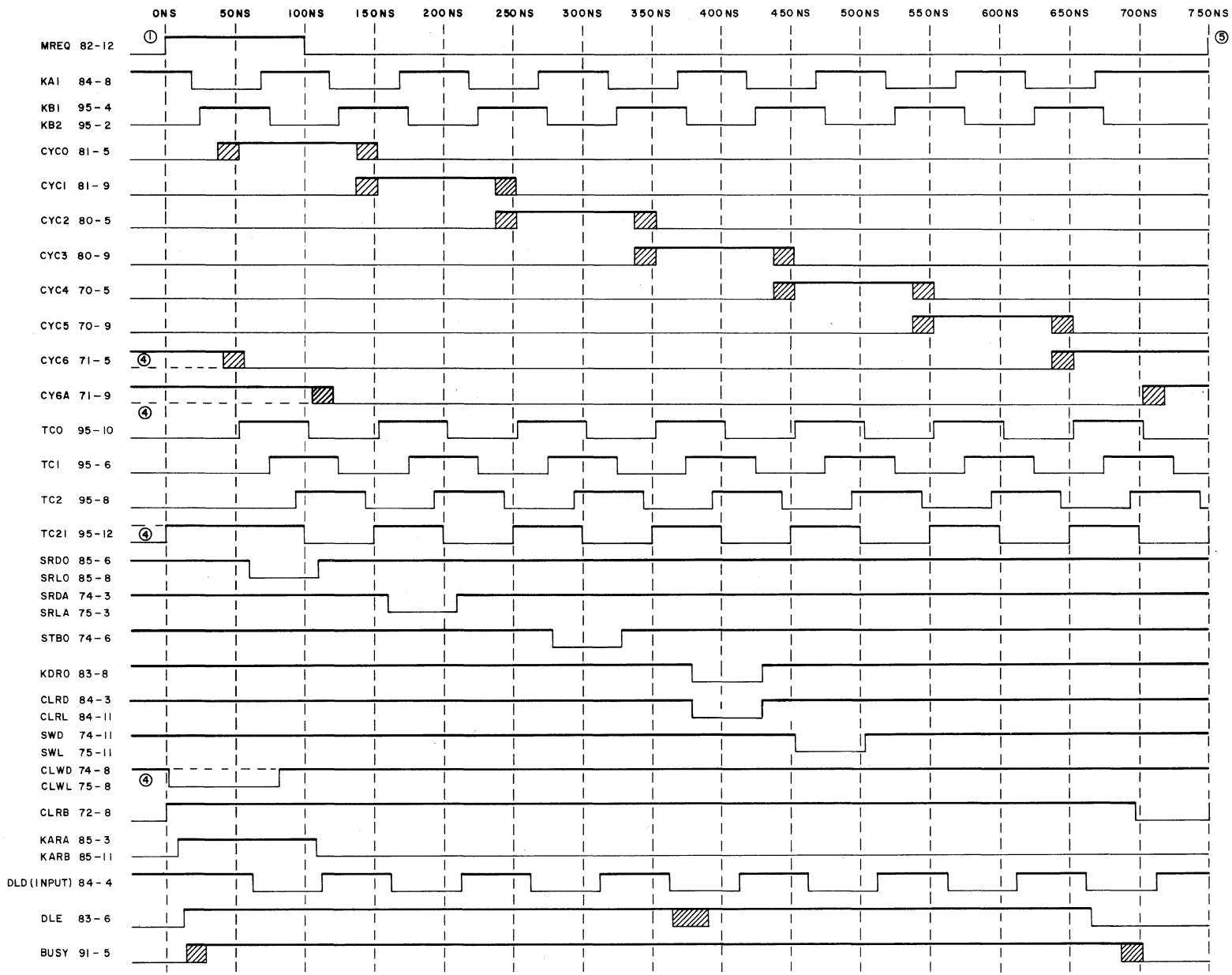
Two output signals indicate the status of the storage module. The MEMORY BUSY signal goes from "0" to "1" just after the module receives a MEMORY REQUEST, and stays at the "1" level for the duration of the function. The MEMORY DATA READY signal goes from "0" to "1" about 350 n/sec after the module receives a MEMORY REQUEST, and stays at the "1" level until the next MEMORY REQUEST is received.

MASTER CLEAR

This signal should be given after the initial power on, and before the initiation of the first memory function.



CONTROL DATA DEVELOPMENT DIVISION	BLOCK DIAGRAM, 4 K, 2 1/2 DIMENSION MEMORY	CODE IDENT 34010	DWG NO 60345600	REV
		C	SHEET B1	PAGE 5-9



NOTES:

① THE NUMBERS SHOW THE CHIP LOCATION AND PIN NUMBER WHERE THE SIGNAL MAY BE CHECKED.

2. ALL LOCATIONS ON BOARD ASSEMBLY 53510700.

3. ALL TIMES ARE NOMINAL.

④ FOLLOWING A MASTER CLEAR, THIS SIGNAL IS AT THE LEVEL INDICATED BY THE DOTTED LINE.

⑤ EARLIEST TIME FOR NEXT MREQ.

CONTROL DATA	TIMING DIAGRAM	CODE IDENT	DWG NO	REV
DEVELOPMENT DIVISION		34010	60345600	
		C	SHEET TO	PAGE 5-11

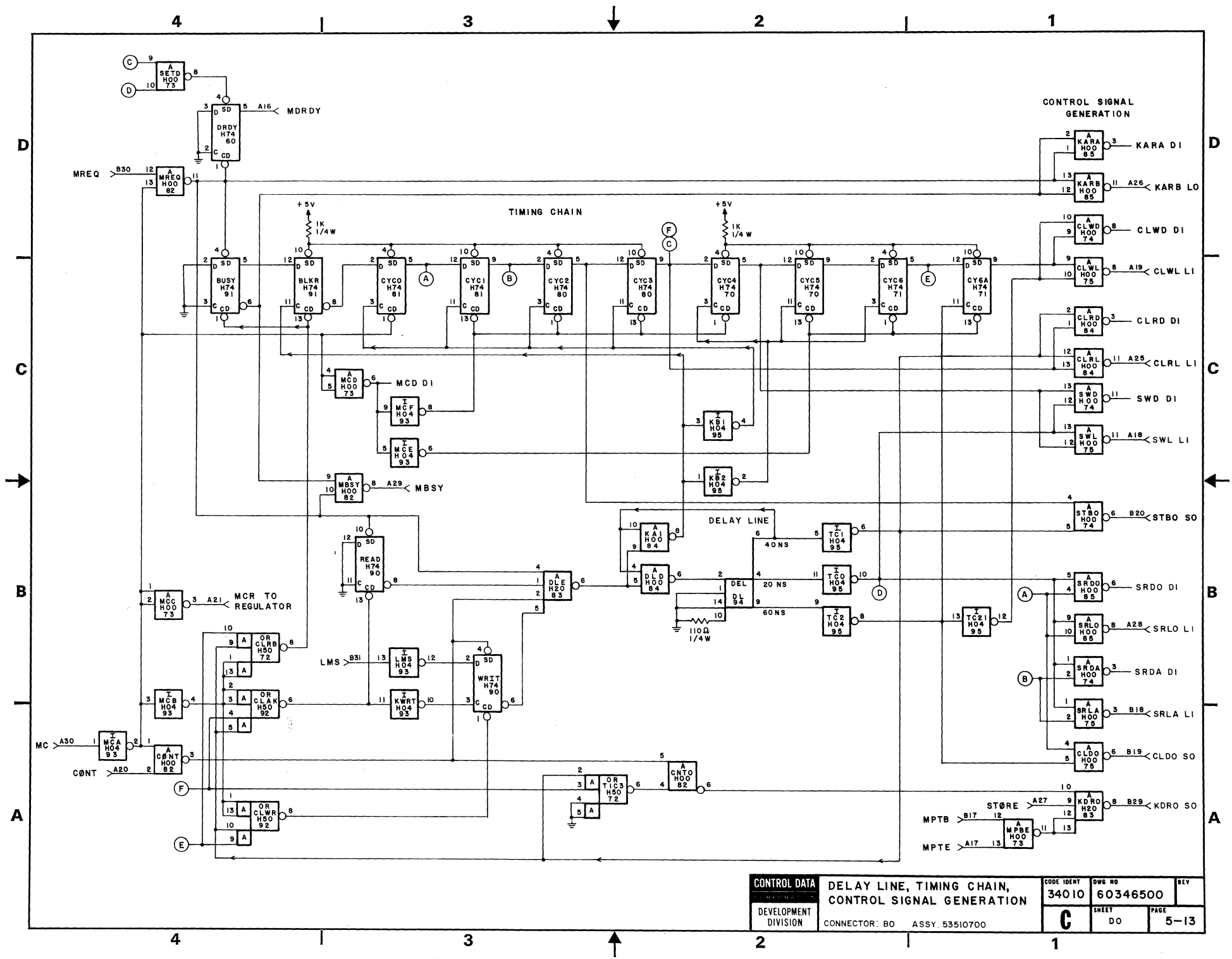
SHEET D0

CONTROL LOGIC

Sheet D0 shows input/output memory control signals, the delay line, and the timing chain.

The circuits shown receive memory function commands, and apply them to load and store logic at times determined by the delay line and timing chain.

Terms DL, $\bar{K}A1$, KB1, and KB2 initiate clock pulses which feed the clock inputs of timing chain flip-flops to generate the CYCx signals shown on sheet T0. CYCx signals combine with control and TCx signals to enable the drivers shown on the right edge of sheet D0. Signals from the drivers control the operation of X and Y drive circuits and the sense logic.


CONTROL SIGNAL GENERATION
TIMING CHAIN
DELAY LINE
MDRDY
MREQ
MCD DI
MBSY
MCR TO REGULATOR
LMS
MC
CONT
STORE
MPTB
MPTE
KARA DI
KARB LO
CLWD DI
CLWL LI
CLRD DI
CLRL LI
SWD DI
SWL LI
STBO SO
SRDO DI
SRLO LI
SRDA DI
SRLA LI
CLDO SO
KDRO SO
+5V
1K 1/4W
40NS
20 NS
60NS
110Ω 1/4W
CONTROL DATA
DEVELOPMENT DIVISION
DELAY LINE, TIMING CHAIN, CONTROL SIGNAL GENERATION
CONNECTOR: BO ASSY. 53510700
CODE IDENT 34010
DWG NO 60346500
REV C
SHEET DO
PAGE 5-13

SHEET D1

Sheet D1 shows the X and Y diode drivers, six of the address bits, and read, write, decode, and phase selection logic.

MEMORY DRIVERS

Two source-sink drive transistor pairs are contained in each MD package. Figure 5-2 shows a schematic of the circuit in an MD package. Note that drivers are enabled and triggered by "0's". X source drive collectors are connected to X drive current and Y source drive collectors are connected to Y drive current Both X and Y sink drive emitters are connected to ground.

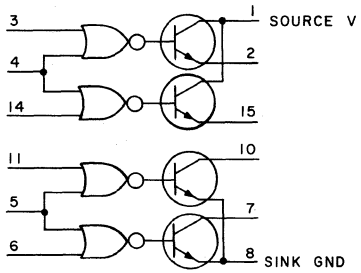


Figure 5-2. Source-Sink Memory Driver

ADDRESS SELECTION

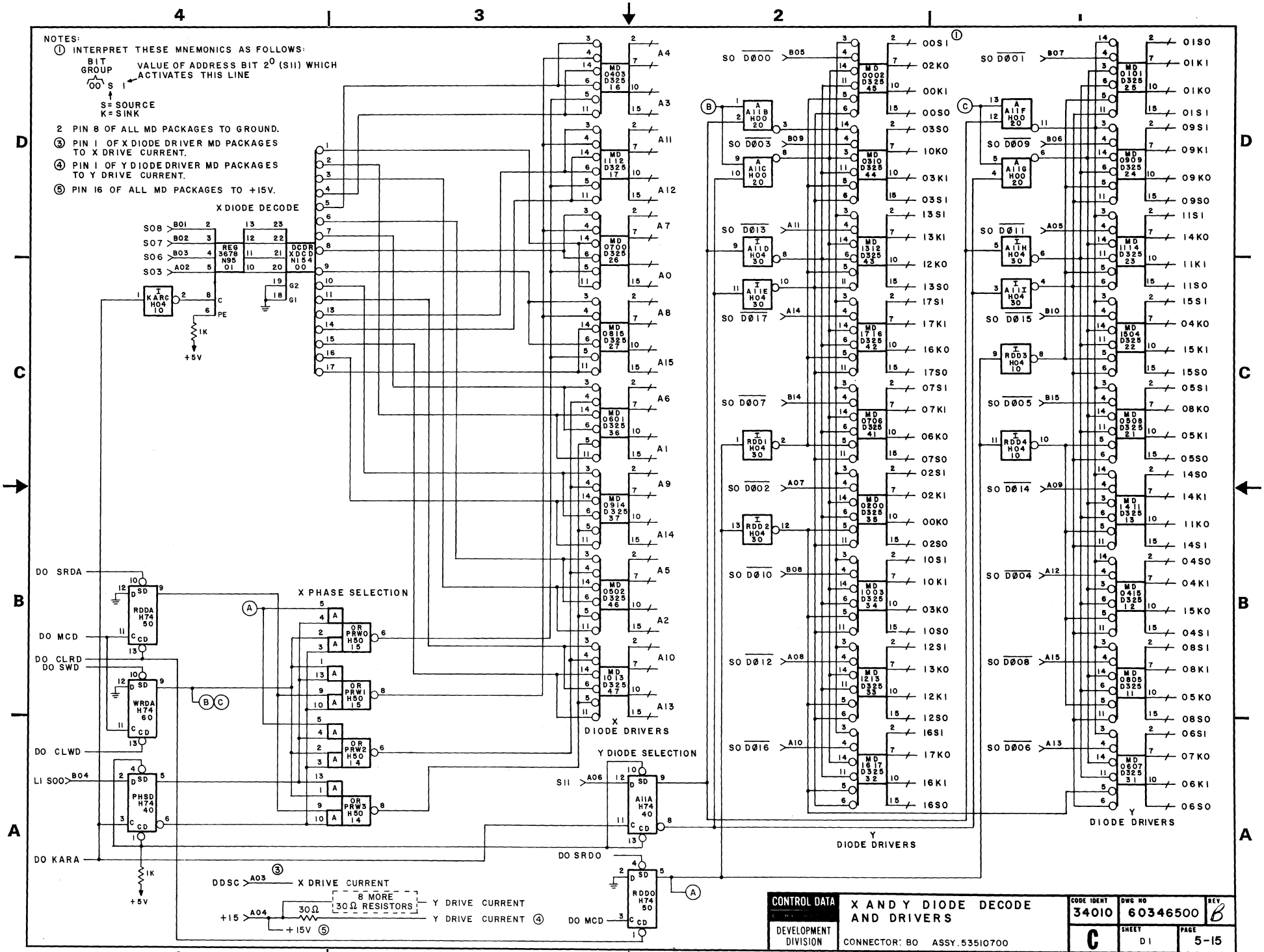
Address bits S03, S06, S07, and S08 feed four bit register 3678 which drives the one-of-16 decoder, XDCD. Address bit S00 feeds the PHSD flip-flop to determine the phase of X currents. Address bit S11 feeds the A11A flip-flop to select 18 of 36 Y diode drivers.

X Diode Drivers

PHSD, RDD0, RDDA, and WRDA flip-flops feed and/nor gates PRW0-PRW3 to determine whether "0's" are presented to all source inputs (pin 4) or all sink inputs (pin 5) of X diode drivers. The X diode driver that receives a "0" from the decoder applies X drive current to 16 X lines through four diode packages when its source input is "0". When its sink input is "0", the X diode driver that receives a "0" from the decoder grounds 16 X lines through four diode packages.

Y Diode Drivers

RDD0, WRDA, and A11A flip-flops feed inverter/drivers to select 18 of the 36 Y diode drivers. All of the 18 selected Y diode drivers receive "0's" from inverters when RDD0 is set, causing each of the drivers to ground four Y lines through a diode package. When WRDA is set, the 18 A11A selected Y drivers that have a "0" input from DO-XX each apply Y drive current to four Y lines through a diode package.

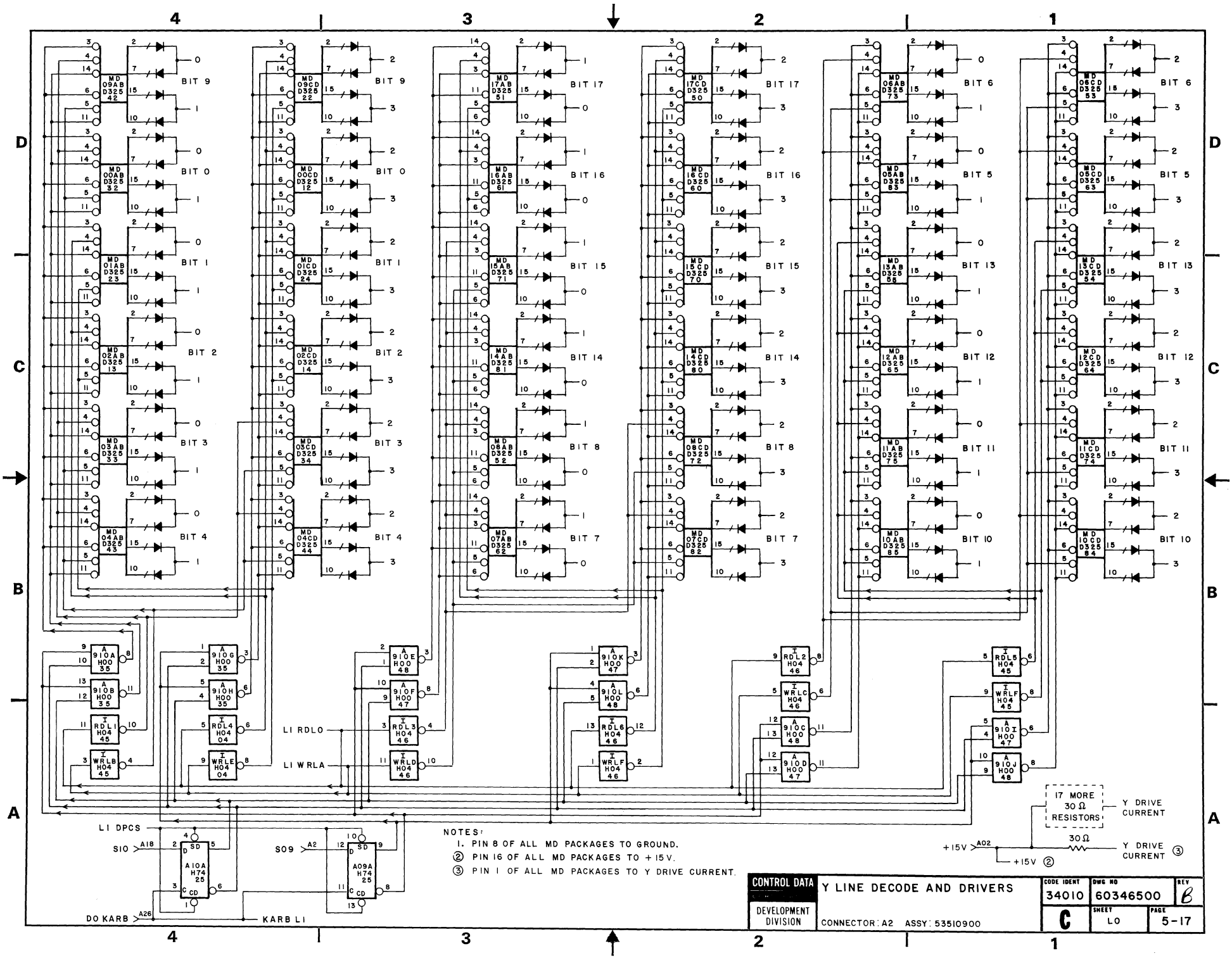

NOTES:
① INTERPRET THESE MNEMONICS AS FOLLOWS:
BIT GROUP
VALUE OF ADDRESS BIT 2^0 (S11) WHICH ACTIVATES THIS LINE
S= SOURCE
K= SINK
2 PIN 8 OF ALL MD PACKAGES TO GROUND.
③ PIN 1 OF X DIODE DRIVER MD PACKAGES TO X DRIVE CURRENT.
④ PIN 1 OF Y DIODE DRIVER MD PACKAGES TO Y DRIVE CURRENT.
⑤ PIN 16 OF ALL MD PACKAGES TO +15V.
X DIODE DECODE
X PHASE SELECTION
X DIODE DRIVERS
Y DIODE SELECTION
Y DIODE DRIVERS
Y DIODE DRIVERS
DO SRDA
DO MCD
DO CLRD
DO SWD
DO CLWD
LI S00
DO KARA
DO SRDO
DDSC
X DRIVE CURRENT
8 MORE 30Ω RESISTORS
Y DRIVE CURRENT
Y DRIVE CURRENT ④
+15
+15V ⑤
+5V
1K
CONTROL DATA
DEVELOPMENT DIVISION
X AND Y DIODE DECODE AND DRIVERS
CONNECTOR: BO ASSY. 53510700
CODE IDENT 34010
DWG NO 60346500
REV B
C
SHEET 01
PAGE 5-15

SHEET L0

Sheet L0 shows address bits S09 and S10 and the Y line drivers.

Y LINE DRIVERS

Address bits S09 and S10 feed flip-flops A09A and A10A respectively. Outputs from these flip-flops combine with RDL0 and WRLA outputs (sheet L1) to enable 18 of 72 Y line sink circuits, or 18 of 72 Y line source circuits. Each source-sink circuit is connected to two Y lines through a pair of discrete diodes (see Figures 4-5 and 5-2). When RDL0 is set, each of the 18 address selected Y line drivers applies Y drive current to two Y lines. When WRLA is set, each of the selected Y line drivers grounds two Y lines.

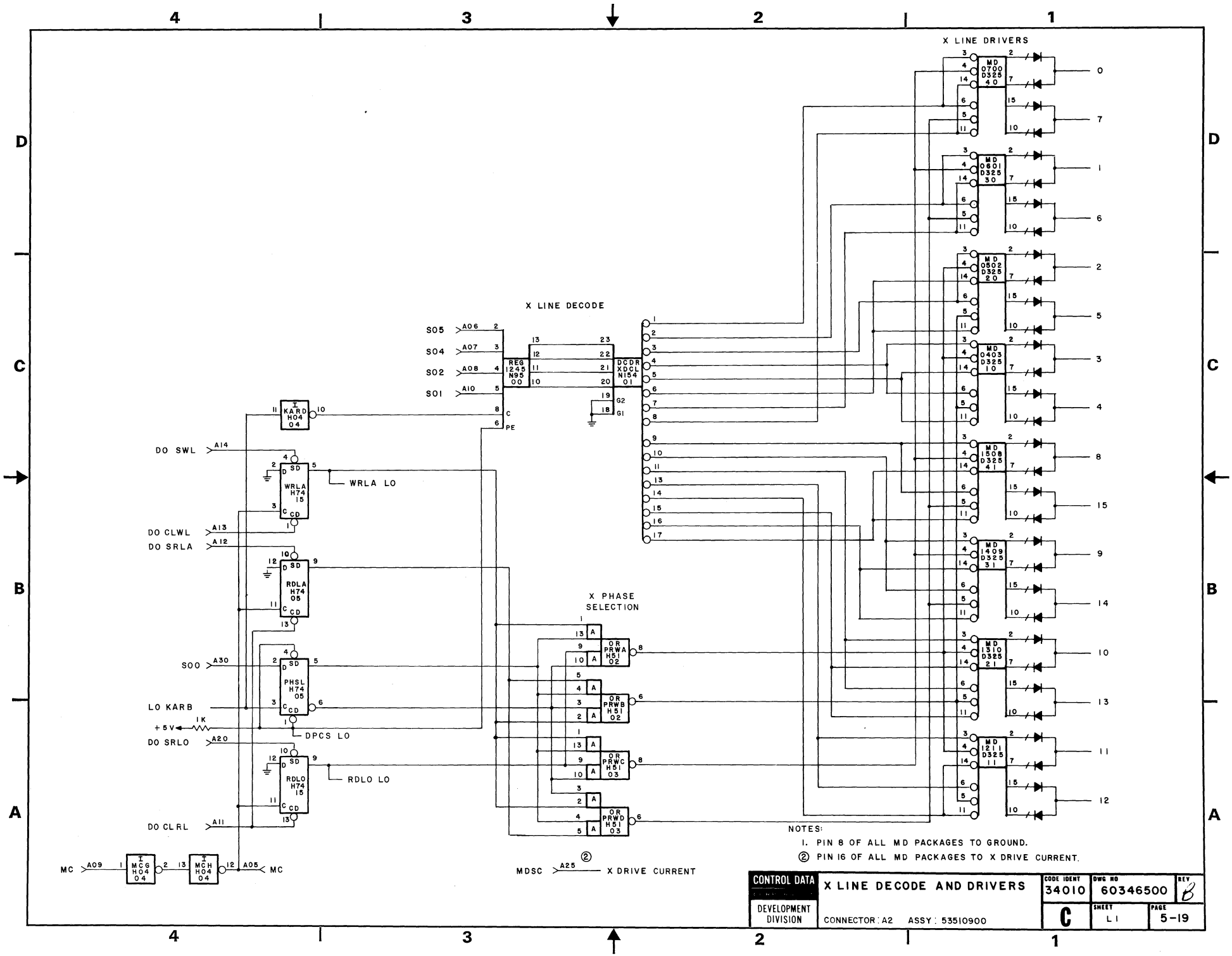

4
3
2
1
D
C
B
A
BIT 9
BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 17
BIT 16
BIT 15
BIT 14
BIT 8
BIT 7
BIT 6
BIT 5
BIT 13
BIT 12
BIT 11
BIT 10
LI RDLO
LI WRLA
LI DPCS
SIO
SO9
DO KARB
KARB LI
17 MORE 30Ω RESISTORS
Y DRIVE CURRENT
30Ω
+15V
NOTES:
1. PIN 8 OF ALL MD PACKAGES TO GROUND.
2. PIN 16 OF ALL MD PACKAGES TO +15V.
3. PIN 1 OF ALL MD PACKAGES TO Y DRIVE CURRENT.
CONTROL DATA
DEVELOPMENT DIVISION
Y LINE DECODE AND DRIVERS
CONNECTOR: A2 ASSY: 53510900
CODE IDENT 34010
DWG NO 60346500
REV B
C
SHEET LO
PAGE 5-17

SHEET L1

Sheet L1 shows X line drivers, and associated read, write, decode, and phase selection logic.

X LINE DRIVERS

X line driver logic is similar to X diode driver logic. Address bits S01, S02, S04, and S05 are decoded to select one of 16 source-sink circuits. Each source-sink circuit drives 16 X lines through a pair of discrete diodes. X line driver phase selection is opposite X diode driver phase selection, so when the selected diode driver supplies X drive voltage, the selected line driver is grounded. When the selected diode driver is grounded, the selected line driver connects to X drive current.


X LINE DRIVERS
X LINE DECODE
X PHASE SELECTION
S05
S04
S02
S01
REG 1245 N95 00
DCDR XDCL N154 01
KARD H04 04
DO SWL
WRLA H74 15
WRLA LO
DO CLWL
DO SRLA
RDLA H74 05
S00
PHSL H74 05
LO KARB
+5V
1K
DPCS LO
DO SRLO
RDLO H74 15
RDLO LO
DO CLRL
MC
MCG H04 04
MCH H04 04
MDSC
X DRIVE CURRENT
OR PRWA H51 02
OR PRWB H51 02
OR PRWC H51 03
OR PRWD H51 03
MD 0700 D325 40
MD 0601 D325 30
MD 0502 D325 20
MD 0403 D325 10
MD 1508 D325 41
MD 1409 D325 31
MD 1310 D325 21
MD 1211 D325 11
NOTES:
1. PIN 8 OF ALL MD PACKAGES TO GROUND.
② PIN 16 OF ALL MD PACKAGES TO X DRIVE CURRENT.
CONTROL DATA
DEVELOPMENT DIVISION
X LINE DECODE AND DRIVERS
CONNECTOR: A2 ASSY: 53510900
CODE IDENT 34010
DWG NO 60346500
REV B
C
SHEET L1
PAGE 5-19

SHEET S0

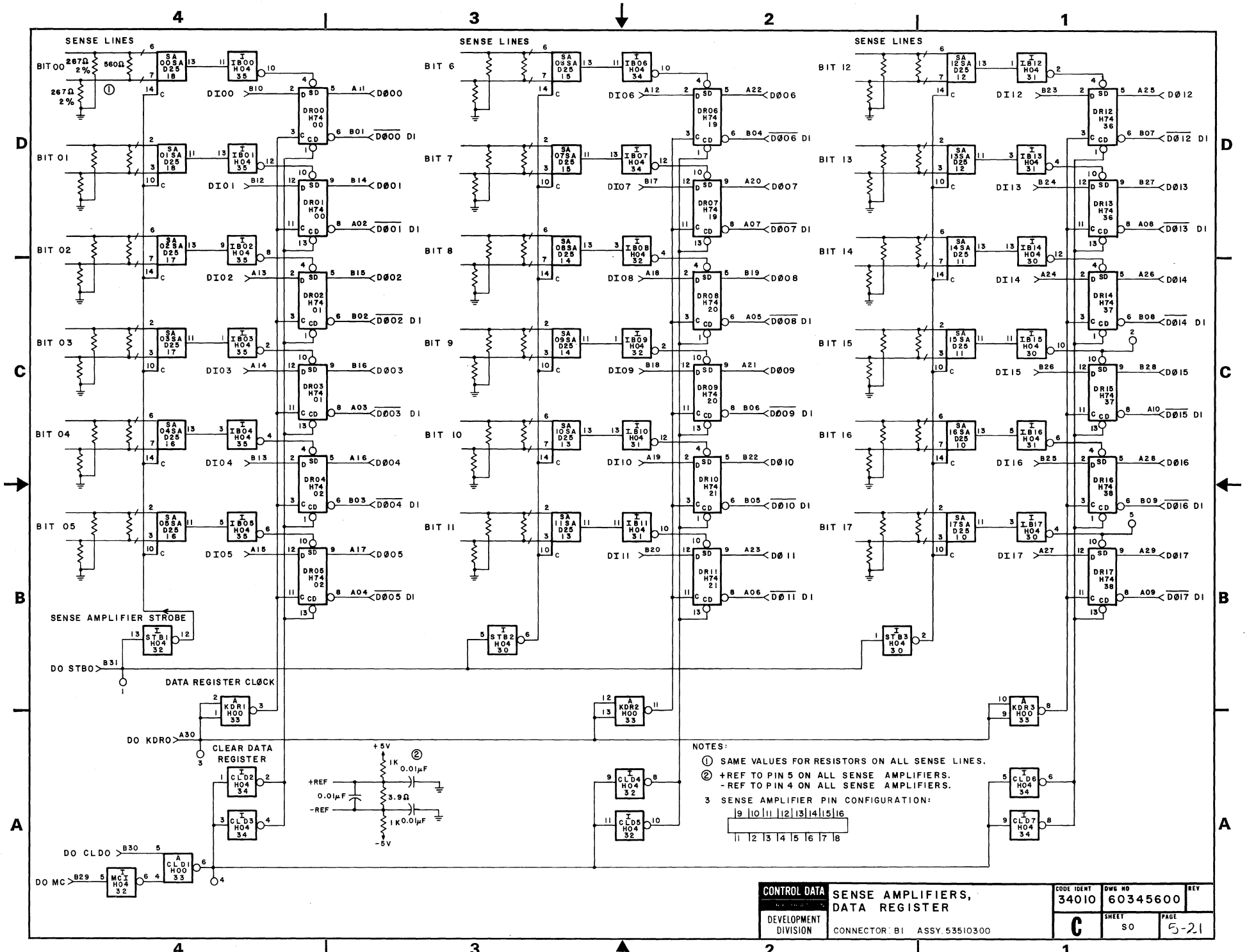
Sheet S0 shows sense amplifiers, the data register, and logic for STROBE, DATA REGISTER CLOCK and CLEAR DATA REGISTER signals.

SENSE AMPLIFIERS

Each sense line loops through all the cores of a bit group and connects to two pins of a sense amplifier. The three resistors on each sense line prevent resonance, but do not significantly attenuate the primary sense signal. When strobed, a sense amplifier generates a "1" if it detects a voltage on its sense line, or it generates a "0" if it fails to detect a voltage. Sense amplifier outputs feed the pre-set inputs of the data register through inverters.

DATA REGISTER

The CLEAR DATA REGISTER signal occurs before every STROBE signal. Sense data enters the data register during both load and store functions. However, during store functions, the DATA REGISTER CLOCK signal causes the word on the input data lines to replace the sense data in the data register.


SENSE LINES
BIT 00
BIT 01
BIT 02
BIT 03
BIT 04
BIT 05
BIT 6
BIT 7
BIT 8
BIT 9
BIT 10
BIT 11
BIT 12
BIT 13
BIT 14
BIT 15
BIT 16
BIT 17
267Ω 2%
560Ω
SENSE AMPLIFIER STROBE
DO STBO
DATA REGISTER CLOCK
DO KDRO
CLEAR DATA REGISTER
DO CLDO
DO MC
+5V
+REF
-REF
0.01μF
3.9Ω
1K
-5V
NOTES:
① SAME VALUES FOR RESISTORS ON ALL SENSE LINES.
② +REF TO PIN 5 ON ALL SENSE AMPLIFIERS.
-REF TO PIN 4 ON ALL SENSE AMPLIFIERS.
3 SENSE AMPLIFIER PIN CONFIGURATION:
CONTROL DATA
DEVELOPMENT DIVISION
SENSE AMPLIFIERS, DATA REGISTER
CONNECTOR: B1 ASSY. 53510300
CODE IDENT 34010
DWG NO 60345600
REV
C
SHEET 80
PAGE 5-21

FV444 POWER REGULATOR MODULE

Sheet R0 shows the current and voltage regulator which supplies one or two storage modules with X and Y drive voltages.

CURRENT AND VOLTAGE REGULATION

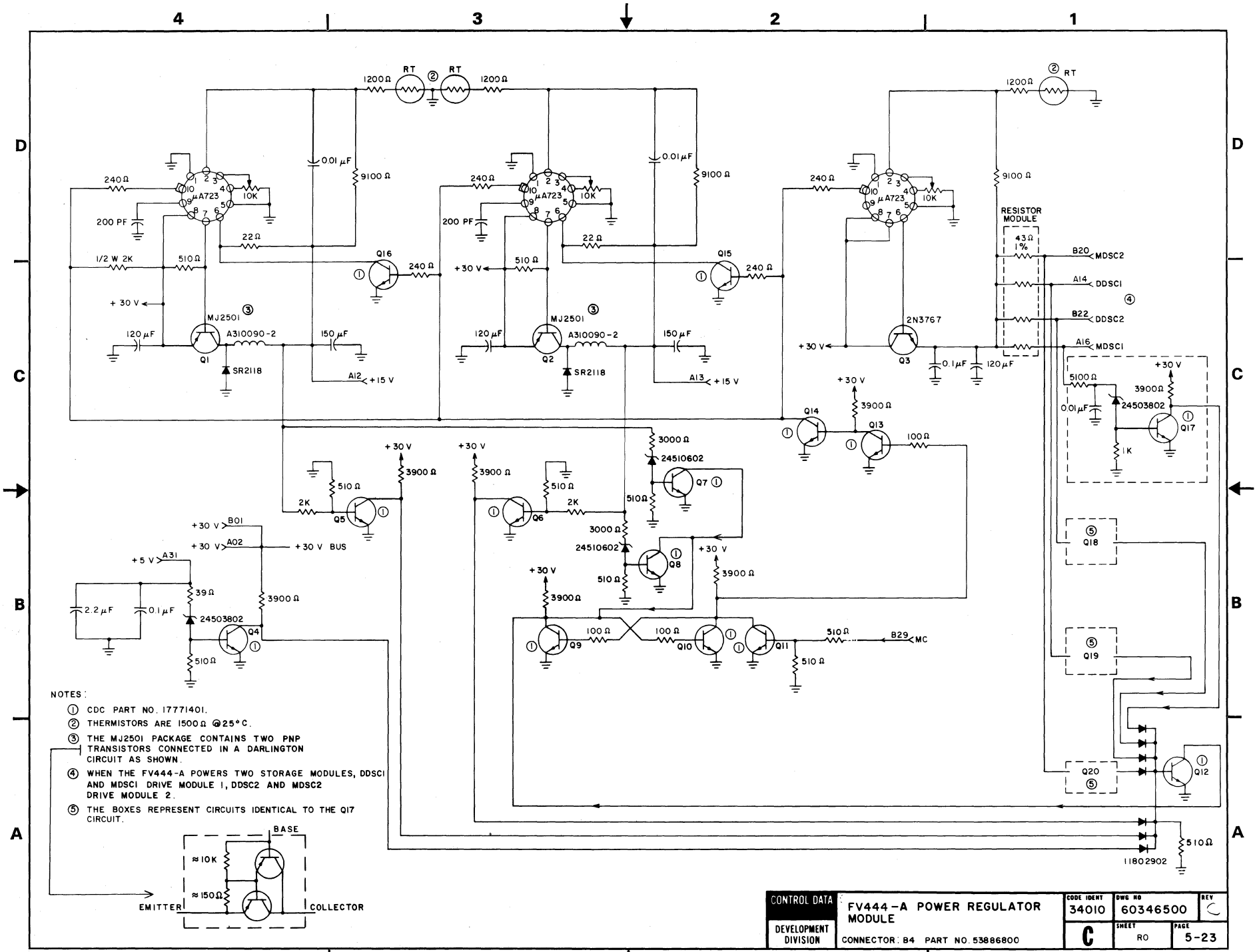
The regulator uses three uA723 integrated circuits to sense voltage conditions and drive the bases of the output power transistors, Q1-Q3. Inductors on Y drive outputs keep current flow constant during Y current variations. The large capacitors on all drive outputs stabilize voltages during transition. A sensistor interacts with each uA723 circuit, causing drive voltages to vary inversely with temperature. This feature keeps drive currents consistent with changes in core switching characteristics over a broad temperature range.

STORAGE MODULE PROTECTION

Transistors Q4-Q20 form a network which clears flip-flop Q9-Q10 under certain conditions. When the flip-flop clears, the uA723 circuits shut down the output power transistors Q1-Q3. The following transistor circuits clear flip-flop Q9-Q10 for the given conditions.

Circuit	Condition
Q4	+5v. source too low
Q5	+15v. output (A12) too low
Q6	+15v. output (A13) too low
Q7	+15v. output (A12) too high
Q8	+15v. output (A13) too high
Q17	MDSC1 output low for more than 100 μsec.
Q18	DDSC2 output low for more than 100 μsec.
Q19	DDSC1 output low for more than 100 μsec.
Q20	MDSC2 output low for more than 100 μsec.

Circuits Q17-Q20 turn off the power to the selected memory driver circuits if the drivers draw current for more than about 100 μsec. This prevents burning out the drivers in the event of an addressing malfunction in the storage module.



NOTES:

① CDC PART NO. 1777140I.

② THERMISTORS ARE 1500Ω @25°C.

③ THE MJ2501 PACKAGE CONTAINS TWO PNP TRANSISTORS CONNECTED IN A DARLINGTON CIRCUIT AS SHOWN.

④ WHEN THE FV444-A POWERS TWO STORAGE MODULES, DDSCI AND MDSCI DRIVE MODULE 1, DDSC2 AND MDSC2 DRIVE MODULE 2.

⑤ THE BOXES REPRESENT CIRCUITS IDENTICAL TO THE Q17 CIRCUIT.

CONTROL DATA	FV444-A POWER REGULATOR MODULE	CODE IDENT 34010	DWG NO 60346500	REV
DEVELOPMENT DIVISION	CONNECTOR: B4 PART NO. 53886800	C	SHEET R0	PAGE 5-23

SECTION 6

MAINTENANCE

SECTION 7

MAINTENANCE AIDS

Since the BB372-A and FV444 are not intended to be field repairable, these sections are not included in this manual.

SECTION 8

PARTS DATA

BB372A 53104300 00 4K MEMORY

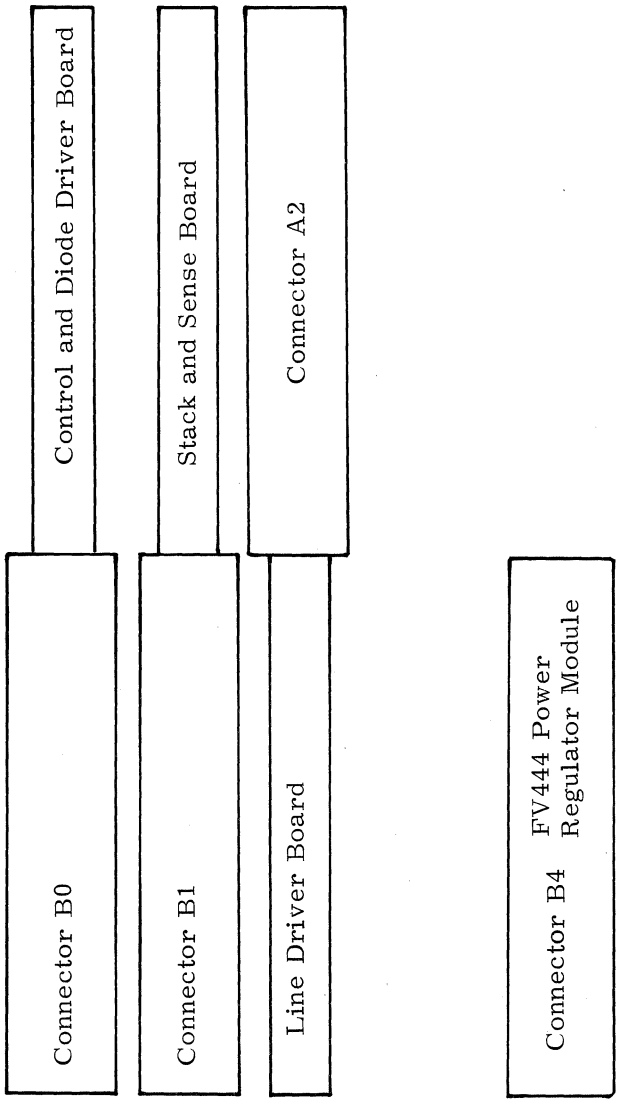
LEVEL	PART-NO	REV	DESCRIPTION	SPARE	ECO-NO
1	15000700	E	EQUIPMENT IDENTIFICATION PLATE	N	IN
1	53670600	A	FINAL ASSY L.C. 18 BIT MEMORY		IN
2	10125102	C	HEXAGON MACHINE SCREW NUTS	N	IN
2	10126101	C	INTERNAL TOOTH LOCK WASHERS	N	IN
2	10127103	D	SCR MACH PAN PHL 4-40	N	IN
2	53510700	A	ASSY , DIODE DRIVER BD		IN
3	24500040	D	RES FXD .25W 110 OHMS	N	IN
3	24500063	D	RES FXD .25W 1000 OHMS	N	IN
3	24504306	E	CAP FIXED SOLID TANTALUM	N	IN
3	24561307	D	CAP FIXED CERAMIC .1UF,25V	N	IN
3	36188701	A	INT CKT 74H00 TTL QUAD 2 INPUT	N	IN
3	52335500	A	ACCEPT.TEST SHIFT REG.4BIT7495	N	IN
3	52335600	A	ACCEPT.TEST HEX.INVERT. 74H04	N	IN
3	52335700	A	ACCEPT.TEST DUAL 4 IN GAT74H20	N	IN
3	52335800	A	ACCEPT.TEST 2W 2IN GATE 74H50	N	IN
3	52335900	A	ACCEPT.TEST F.F. EDGE TR.74H74	N	IN
3	52336100	A	ACCEPT.TEST MEM.DRIVER 75325	N	IN
3	52337100	A	ACCEPT.TEST 4-16 DECODE 74154	N	IN
3	52537300	C	CONNECTOR 62 CONTACT	N	IN
3	52977400	A	CAPACITOR FXD TANTALUM MIN	N	IN
3	53264000	D	DELAY LINE TAPPED TYPE D 100	N	IN
3	53510000	A	PC BD/MA , DIODE DRIVER	N	IN
3	53623100	B	RESISTOR MODULE	N	IN
3	68582317	H	CAP FXD 750 PF	N	IN
2	53510900	A	ASSY, MATRIX DRIVER		IN
3	17622806	A	CAP., FXD CER TEMP-STABLE	N	IN
3	24500063	D	RES FXD .25W 1000 OHMS	N	IN
3	24504361	E	CAP FIXED SOLID TANTALUM	N	IN
3	24553500	L	DIODE SILICON PLANAR	N	IN
3	36188701	A	INT CKT 74H00 TTL QUAD 2 INPUT	N	IN
3	52335500	A	ACCEPT.TEST SHIFT REG.4BIT7495	N	IN
3	52335600	A	ACCEPT.TEST HEX.INVERT. 74H04	N	IN
3	52335800	A	ACCEPT.TEST 2W 2IN GATE 74H50	N	IN
3	52335900	A	ACCEPT.TEST F.F. EDGE TR.74H74	N	IN
3	52336100	A	ACCEPT.TEST MEM.DRIVER 75325	N	IN
3	52337100	A	ACCEPT.TEST 4-16 DECODE 74154	N	IN
3	52537300	C	CONNECTOR 62 CONTACT	N	IN
3	52977400	A	CAPACITOR FXD TANTALUM MIN	N	IN
3	53510800	A	PC BD/MA , MATRIX DRIVER	N	IN
3	53623100	B	RESISTOR MODULE	N	IN
3	68582317	H	CAP FXD 750 PF	N	IN
2	53611200	A	SPEC FOR 18 BIT LOW COST MEM	N	IN
2	53616800	A	STACK ASSY - LC 18 BIT		IN
3	17623809	E	CAPACITOR,FIXED,CERAMIC MINAT	N	IN
3	24504306	E	CAP FIXED SOLID TANTALUM	N	IN
3	24561307	D	CAP FIXED CERAMIC .1UF,25V	N	IN
3	24563002	G	RES FXD COMP 1/8W 3.9 OHMS	N	IN
3	24563028	G	RES FXD COMP 1/8W 560 OHMS	N	IN
3	24563031	G	RES FXD COMP 1/8W 1000 OHMS	N	IN
3	36188701	A	INT CKT 74H00 TTL QUAD 2 INPUT	N	IN
3	52312201	E	INTEGRATED CIRCUIT SENSE AMP	N	IN
3	52335600	A	ACCEPT.TEST HEX.INVERT. 74H04	N	IN
3	52335900	A	ACCEPT.TEST F.F. EDGE TR.74H74	N	IN

BB372A	53184300	00	4K MEMORY		
LEVEL	PART NO	REV	DESCRIPTION	SPARE	ECO NO
3	52537300	C	CONNECTOR 62 CONTACT	N	IN
3	53670800	A	CORE ARRAY ASSY		IN
4	10125100	C	HEXAGON MACHINE SCREW NUTS	N	IN
4	24524425	T	WIRE MAG RD POLY RED	N	IN
4	24524426	T	WIRE MAG RD POLY GREEN	N	IN
4	53510100	A	MODULE ASSY DIODE		IN
5	52597400	A	DIODE MODULES	N	IN
5	53510000	A	PC BD/MA , DIODE	N	IN
4	53510300	A	BD ASSY - SENSE & MATRIX		IN
5	53510200	A	PC BD/MA , SENSE & MATRIX	N	IN
5	68583335	E	RES,FXD, FILM 1/8 W, 1% 267 OH	N	IN
4	53584200	A	SPACER	N	IN
4	53584201	A	SPACER .100 AL 6061-T6	N	IN
4	53584202	A	SPACER .196 AL 6061-T6	N	IN
4	53584203	A	SPACER .248 AL 6061-T6	N	IN
4	53584204	A	SPACER .380 AL 6061-T6	N	IN
4	53584400	A	COVER- LEFT HAND,CORE	N	IN
4	53584500	A	COVER- RIGHT HAND,CORE	N	IN
4	53595800	00	CONN ASSY J19-61 PIN	N	IN
4	53595801	00	CONN ASSY J19-61 PIN (2,56)	N	IN
4	53595802	00	CONN ASSY J19-61 PIN (4,20)	N	IN
4	53616900	A	ARRAY INSULATOR		IN
5	53616901	A	.003 POLYESTER	N	IN
5	53616902	A	.001 COPPER	N	IN
5	53616903	A	POLYESTER ADHESIVE	N	IN
4	53670700	A	CORE TRANSFER ASSY		IN
5	18440202	C	ADH/SEALANT SILICONE RUBBER	N	IN
5	18440206	C	ADHESIVE / SEALANT WHITE	N	IN
5	53584300	A	PLATE TRANSFER	N	IN
5	53648300	A	CORE 20 MIL OD	N	IN
4	68530106	E	MACHINE SCREW,PAN HD, SLOTTED	N	IN
4	93121008	B	ROD THREADED NC	N	IN
4	95670600	B	TAPE MYLAR 1/2 X .001	N	IN
3	68582310	H	CAPACITOR FIXED 10000	N	IN 027758
2	53634600	A	HANDLE		IN
3	53634601	A	HANDLE 18GA .047 CRS	N	IN
3	94894001	F	SCREW- CAPTIVE 6-32X .091	N	IN 028437
2	53634700	A	BRACKET		IN
3	00830301	C	NUT CAPTIVE	N	IN 027828
3	53634701	A	BRACKETALUM 5052-H32 .060	N	IN

FV444	53800800	A	POWER REGULATOR MODULE			
LEVEL	PART NO	REV	DESCRIPTION	SPARE		ECO NO
1	15000700	E	EQUIPMENT IDENTIFICATION PLATE	N	IN	
1	53861600	A	ASSY, REGULATOR BD		IN	
2	09018003	B	SCR, MACH PAN HD PHL NO. 2	N	IN	
2	10125102	C	HEXAGON MACHINE SCREW NUTS	N	IN	
2	10127103	D	SCR MACH PAN PHL 4-40	N	IN	
2	17771401	F	TRANS SILICON NPN DRIVER	N	IN	
2	18435005	B	POT TRIMMER 1/2 W 10000 OHMS	N	IN	
2	24500023	D	RES FXD .25W 22 OHMS	N	IN	
2	24500029	D	RES FXD .25W 39 OHMS	N	IN	
2	24500039	D	RES FXD .25W 100 OHMS	N	IN	
2	24500048	D	RES FXD .25W 240 OHMS	N	IN	
2	24500056	D	RES FXD .25W 510 OHMS	N	IN	
2	24500063	D	RES FXD .25W 1000 OHMS	N	IN	
2	24500065	D	RES FXD .25W 1200 OHMS	N	IN	
2	24500070	D	RES FXD .25W 2000 OHMS	N	IN	
2	24500077	D	RES FXD .25W 3900 OHMS	N	IN	
2	24500080	D	RES FXD .25W 9100 OHMS	N	IN	
2	24500170	C	RES FXD COMP .50 W 5 PERCENT	N	IN	
2	24503802	J	DIODE SILICON ZENER	N	IN	
2	24504306	E	CAP FIXED SOLID TANTALUM	N	IN	
2	24501307	D	CAP FIXED CERAMIC .1UF,25V	N	IN	
2	52537300	C	CONNECTOR 62 CONTACT	N	IN	
2	52596900	A	TRANSISTOR PNP SILICON POWER	N	IN	
2	52599000	A	HEAT SINK TO3	N	IN	
2	52599400	A	RECTIFIER,SIL FAST RECOVERY	N	IN	
2	52600900	A	VOLTAGE REG UA 723C	N	IN	
2	52601000	A	TRANSISTOR NPN SILICON POWER	N	IN	
2	52855500	A	GREASE, THERMAL HEAT SINK	N	IN	
2	52889409	B	THERMISTOR TUBULAR	N	IN	
2	52977402	A	CAPACITOR FXD TANTALUM MIN	N	IN	
2	52977403	A	CAPACITOR FXD TANTALUM MIN	N	IN	
2	53178800	A	PC BD/MA, REGULATOR	N	IN	
2	53623000	A	RESISTOR,5 WATT,NON-INDUCTIVE	N	IN	
2	53648200	A	INDUCTOR,SWITCHING REGULATOR	N	IN	
2	68582310	H	CAPACITOR FIXED 10000	N	IN	027758
2	53623102		RESISTOR MODULE	N	IN	031786
2	52977400		CAPACITOR, FXD, TANTLUM MIN			
2	53847300		POTENTIOMETER, MIN			
2	68582306		CAPACITOR, FIXED 200 PF			

SECTION 9

WIRE LISTS



(View from connector side of module)

Figure 9-1. Connector Locations

Connector A2, Board Assembly 53510900, Diagram sheets L0, L1

PIN	SIGNAL	PIN	SIGNAL
A01		B01	
A02	+15v	B02	
A03		B03	
A04		B04	
A05	MC	B05	
A06	S05	B06	
A07	S04	B07	
A08	S02	B08	
A09	MC	B09	
A10	S01	B10	
A11	CLRL	B11	GROUND
A12	SRLA	B12	
A13	CLWL	B13	
A14	SWL	B14	
A15		B15	
A16		B16	
A17		B17	
A18	S10	B18	
A19		B19	
A20	SRL0	B20	
A21	S09	B21	GROUND
A22		B22	
A23		B23	
A24		B24	
A25	MDSC	B25	
A26	KARB	B26	
A27		B27	
A28		B28	
A29		B29	
A30	S00	B30	
A31	+5v	B31	

NOTE

For definitions of signal mnemonics, see the Signal Index in Key To Logic Symbols, Section 5.

Connector B0, Board Assembly 53510700, Diagram sheets D0, D1

PIN	SIGNAL	PIN	SIGNAL
A01		B01	S08
A02	S03	B02	S07
A03	DDSC	B03	S06
A04	+15v	B04	S00
A05	$\overline{\text{DO11}}$	B05	$\overline{\text{DO00}}$
A06	S11	B06	$\overline{\text{DO09}}$
A07	$\overline{\text{DO02}}$	B07	$\overline{\text{DO01}}$
A08	$\overline{\text{DO12}}$	B08	$\overline{\text{DO10}}$
A09	$\overline{\text{DO14}}$	B09	$\overline{\text{DO03}}$
A10	$\overline{\text{DO16}}$	B10	$\overline{\text{DO15}}$
A11	$\overline{\text{DO13}}$	B11	GROUND
A12	$\overline{\text{DO04}}$	B12	
A13	$\overline{\text{DO06}}$	B13	
A14	$\overline{\text{DO17}}$	B14	$\overline{\text{DO07}}$
A15	$\overline{\text{DO08}}$	B15	$\overline{\text{DO15}}$
A16	MDRDY	B16	
A17	MPTE	B17	MPTB
A18	SWL	B18	SRLA
A19	CLWL	B19	CLD0
A20	CONT	B20	STB0
A21	MCR	B21	GROUND
A22		B22	
A23		B23	
A24		B24	
A25	CLRL	B25	
A26	KARB	B26	
A27	STORE	B27	
A28	SRL0	B28	
A29	MBSY	B29	KDR0
A30	MC	B30	MREQ
A31	+5v	B31	LMS

NOTE

For definitions of signal mnemonics, see the Signal Index in Key To Logic Symbols, Section 5.

Connector B1, Board Assembly 53510300, Diagram sheet S0

PIN	SIGNAL	PIN	SIGNAL
A01	-5v	B01	$\overline{\text{DO00}}$
A02	$\overline{\text{DO01}}$	B02	$\overline{\text{DO02}}$
A03	$\overline{\text{DO03}}$	B03	$\overline{\text{DO04}}$
A04	$\overline{\text{DO05}}$	B04	$\overline{\text{DO06}}$
A05	$\overline{\text{DO08}}$	B05	$\overline{\text{DO10}}$
A06	$\overline{\text{DO11}}$	B06	$\overline{\text{DO09}}$
A07	$\overline{\text{DO07}}$	B07	$\overline{\text{DO12}}$
A08	$\overline{\text{DO13}}$	B08	$\overline{\text{DO14}}$
A09	$\overline{\text{DO17}}$	B09	$\overline{\text{DO16}}$
A10	$\overline{\text{DO15}}$	B10	DI00
A11	DO00	B11	GROUND
A12	DI06	B12	DI01
A13	DI02	B13	DI04
A14	DI03	B14	DO01
A15	DI05	B15	DO02
A16	DO04	B16	DO03
A17	DO05	B17	DI07
A18	DI08	B18	DI09
A19	DI10	B19	DO08
A20	DO07	B20	DI11
A21	DO09	B21	GROUND
A22	DO06	B22	DO10
A23	DO11	B23	DI12
A24	DI14	B24	DI13
A25	DO12	B25	DI16
A26	DO14	B26	DI15
A27	DI17	B27	DO13
A28	DO16	B28	DO15
A29	DO17	B29	MC
A30	KDR0	B30	CLD0
A31	+5v	B31	STB0

NOTE

For definitions of signal mnemonics, see the Signal Index in Key To Logic Symbols, Section 5.

Connector B4, Board Assembly 53510500, Diagram sheet R0

PIN	SIGNAL	PIN	SIGNAL
A01		B01	+30v
A02	+30v	B02	
A03		B03	
A04		B04	
A05		B05	
A06		B06	
A07		B07	
A08		B08	
A09		B09	
A10		B10	
A11		B11	GROUND
A12	+15v	B12	
A13	+15v	B13	
A14	DDSC 1	B14	
A15		B15	
A16	MDSC 1	B16	
A17		B17	
A18		B18	
A19		B19	
A20		B20	MDSC 2
A21		B21	GROUND
A22		B22	DDSC 2
A23		B23	
A24		B24	
A25		B25	
A26		B26	
A27		B27	
A28		B28	
A29		B29	MCR
A30		B30	
A31	+5v	B31	

NOTE

For definitions of signal mnemonics, see the Signal Index in Key To Logic Symbols, Section 5.

Signal	Location From	Location To
+15	A2A02	B4A12
MC	A2A05	B1B29
MC	B1B29	B0A30
CLRRB	A2A11	B0A25
SR2B	A2A12	B0B18
CLWB	A2A13	B0A19
SWRB	A2A14	B0A18
SR18	A2A20	B0A28
MDSC	A2A25	B4A16
SARB	B0A26	A2A26
DDSC	B0A03	B4A14
+15	B0A04	B4A13
$\overline{\text{DO00}}$	B0B05	B1B01
$\overline{\text{DO01}}$	B0B07	B1A02
$\overline{\text{DO02}}$	B0A07	B1B02
$\overline{\text{DO03}}$	B0B09	B1A03
$\overline{\text{DO04}}$	B0A12	B1B03
$\overline{\text{DO05}}$	B0B15	B1A04
$\overline{\text{DO06}}$	B0A13	B1B04
$\overline{\text{DO07}}$	B0B14	B1A07
$\overline{\text{DO08}}$	B0A15	B1A05
$\overline{\text{DO09}}$	B0B06	B1B06
$\overline{\text{DO10}}$	B0B08	B1B05
$\overline{\text{DO11}}$	B0A05	B1A06
$\overline{\text{DO12}}$	B0A08	B1B07
$\overline{\text{DO13}}$	B0A11	B1A08
$\overline{\text{DO14}}$	B0A09	B1B08
$\overline{\text{DO15}}$	B0B10	B1A10
$\overline{\text{DO16}}$	B0A10	B1B09
$\overline{\text{DO17}}$	B0A14	B1A09
CLD	B0B19	B1B30
STB	B0B20	B1B31
MCR	B0A21	B4B29
SDR	B0B29	B1A30

MC	A2A09	master clear
MREQ	B0B30	memory request
LMS	B0B31	load-modify-store
MBSY	B0A29	busy
STORE	B0A27	store cycle
MDRDY	B0A16	data ready
MPTE	B0A17	memory protect enable
MPTB	B0B17	memory protect bit
CONT	B0A20	continue
S00	A2A30	Address bit 2^{11}
S00	B0B04	Address bit 2^{11}
S01	A2A10	Address bit 2^{10}
S02	A2A08	Address bit 2^{9}
S03	B0A02	Address bit 2^{8}
S04	A2A07	Address bit 2^{7}
S05	A2A06	Address bit 2^{6}
S06	B0B03	Address bit 2^{5}
S07	B0B02	Address bit 2^{4}
S08	B0B01	Address bit 2^{3}
S09	A2A21	Address bit 2^{2}
S10	A2A18	Address bit 2^{1}
S11	B0A06	Address bit 2^{0}
DI00	B1B10	data input bit 0
DI01	B1B12	data input bit 1
DI02	B1A13	data input bit 2
DI03	B1A14	data input bit 3
DI04	B1B13	data input bit 4
DI05	B1A15	data input bit 5
DI06	B1A12	data input bit 6
DI07	B1B17	data input bit 7
DI08	B1A18	data input bit 8
DI09	B1B18	data input bit 9
DI10	B1A19	data input bit 10
DI11	B1B20	data input bit 11
DI12	B1B23	data input bit 12
DI13	B1B24	data input bit 13

DI14	B1A24	data input bit 14
DI15	B1B26	data input bit 15
DI16	B1B25	data input bit 16
DI17	B1A27	data input bit 17
DO00	B1A11	data output bit 0
DO01	B1B14	data output bit 1
DO02	B1B15	data output bit 2
DO03	B1B16	data output bit 3
DO04	B1A16	data output bit 4
DO05	B1A17	data output bit 5
DO06	B1A22	data output bit 6
DO07	B1A20	data output bit 7
DO08	B1B19	data output bit 8
DO09	B1A21	data output bit 9
DO10	B1B22	data output bit 10
DO11	B1A23	data output bit 11
DO12	B1A25	data output bit 12
DO13	B1B27	data output bit 13
DO14	B1A26	data output bit 14
DO15	B1B28	data output bit 15
DO16	B1A28	data output bit 16
DO17	B1A29	data output bit 17

SECTION 10

EQUATION SUMMARY

(Not Applicable)

COMMENT SHEET

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