89637700

CONTROL DATA CORPORATION

CONTROL DATA®
MAGNETIC TAPE TRANSPORT CONTROLLERS
FA442-A, FA446-A

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA
WIRE LIST
GLOSSARY

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
01	Released Class B ECO CK986.
(10/10/74)	
A	Released Class A ECO CK1303. Previous revision is obsoleted. Combines ICL & LCTT Manuals.
(3/18/75)	ICL Manual was 89769500.
B	Page 3-1 Last Line: Table 3-1 Changed to 3-6 to match Page 3-3 Item 8. Page 3-3, Item 8:
(12/15/75)	Part Number 89724700 changed to 89724702 to match P/N given at bottom of Page 3-1. as per ECO CK1437.
C	Manual Revised: Pages ii, 5-7, 5-33, 5-61, 5-63, 5-69, 5-71, 5-73, 5-75, 5-79, 5-81, 5-82,
(6/10/76)	5-85, 5-86, 5-89, 5-91, 5-95, 5-103, 5-105, 5-107, 5-109, 8-3, 8-4, 8-5, 8-6, 8-7, 8-8, 8-9, 8-10
	8-20, 8-22, 8-26, Released by ECO CK1524. To incorporate changes of ECO's CK1242, CK1360, CK1438,
	CK1299, CK1343, CK1401, CK1473, CK1524, and CAR'S LJL 53, 100, 142, 143.
D	ECO CK 1693. Tape Interface (LCTT) logic corrected to match PWA 89881400 Rev B. Affected
(Feb. 77)	pages: 5-89, 5-95, 5-97, 5-99, 5-111. (CAR LJL191/510).
	Manual to Equipment Level Correlation Sheet page iii updated. Parts Data page 7-1 updated.

Publication No.
89637700

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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

SHEET 1 OF 1

EQUIPMENTS							
MANUAL REV	FCO ECO (CK)	FA442-A* SERIES	SERIAL				
01	242	A02	51-58 61-65				
01	603	A03	59,60 66-71				
01	635	A04	72				
01	702	A05	75-97				
01	851	A06	98-118				
01	851	A07	119-159				
01	1118	A08	175-214				
A/B/C	1193	A09	301 **				
A/B/C	1343	A10	301				
A/B/C	707	A11	301				
D	707	A11	301				
MAN. REV	FCO ECO (CK)	FA446-A* SERIES	SERIAL				
01	514	A01	n/a				
01	887	A02	101-117				
01	887	A03	118-179				
A/B	1038	A04	231-336				
C	1299	A05	401-410				
C	1343	A06	412-416				
C	1315	A07	501-517				
C	1438	A08	601-638				
D	1438	A08	601-638				

*FA442-A is the ICL NRZI Magnetic Tape Transport Controller.
FA446-A is the Modified NRZI LCTT Controller.

** Serial numbers 301 and up of FA442 were never shipped.

PREFACE

This manual provides customer engineering information for the CONTROL DATA® FA442-A NRZI and FA446-A NRZI - LCTT Magnetic Tape Transport Controllers.
The controller is used with the AB107/AB108 Computer to control either the 615-73/615-93 (NRZI) and the 6173/6193 (NRZI-LCTT) Magnetic Tape Transports. The user of this equipment must be familiar with the computer and magnetic tape transport equipment and software with which these controllers are used.

The following CONTROL DATA® publications may be useful as references:

Publication	Pub. No.
1732-2 NRZI Magnetic Tape Transport Controller and Phase Encoding Formatter Reference Manual	89637600
FV497-A/FV618-A Phase Encoding Formatter Customer Engineering Manual	89796100
1748 Computer Refence Manual	89633400
AB107/AB108 Computer Customer Engineering Manual	89633300
1/O Specification Manual	89673100
System 17 Installation Manual	

CONTENTS

(CONT.)

CONTENTS (Cont'd)

CONTENTS (Cont'd)

LIST OF FIGURES

(CONT.)

LIST OF FIGURES (Cont'd)

(CONT.)

LIST OF FIGURES (Cont'd)

LIST OF TABLES

LIST OF TABLES (Cont'd)

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

This section contains a general description of the CONTROL DATA® FA442-A NRZI and FA446-A NRZI-LCTT Magnetic Tape Transport Controllers.

The FA442-A NRZI Magnetic Tape Transport Controller is capable of handling up as many as four ICL Corporation model 11 NRZI Magnetic Tape Transports (MTT's) in daisy chain. The FA442-A can control these MTT's in 37.5 or 75 ips, 556 or 800 bpi configuration in any combination or singly.

The FA446-A NRZI-LCTT Magnetic Tape Transport Controller is capable of handling four modified CPI LCTT magnetic tape transports operating at 25 or 50 ips, 556 or 800 bpi in any combination (or singally). When more than one CPI MTT is used with this controller, a Pertec Corporation compatible translator board must be used and the controllers must be connected in daisy chain.

Each magnetic tape transport controller (MTTC) contains the logic that interprets the AB107/AB108 Central Processing Unit (CPU) function codes, controls the magnetic tape transport (MTT) operations, assembles and disassembles 16-bit words between the CPU and the MTT, and provides the status information to the CPU. The communication between the controller and the CPU is via the A/Q channel and the Direct Storage Access (DSA) channel. Each MTTC may control as many as four MTT's in a daisy chain configuration.

The controller logic for each controller is mounted on four N-PAK Printed Wiring Boards (PWB's). The boards may be mounted in either the AB107/AB108 Computer Main Enclosure or the BT148-A Expansion Enclosure. Power for these controllers is provided by the power supplies of each enclosure.

TABLE 1-1. SPECIFICATIONS (Each PWB)

Specifications	Explanation
PHYSICAL CHARACTERISTICS	
Dimensions	
Width	$6\frac{13}{16}$ inches
Length	$12\frac{3}{8}$ inches
Depth	$\frac{3}{8}$ inches
ENVIRONMENT	
Temperature	
Shipping	-40°F to 158°F (-40°C to 70°C)
Storage	14°F to 122°F (10°C to 50°C)
Operating	40°F to 120°F (5°C to 50°C)
Humidity	
Shipping	0 to 100% RH non-condensing
Storage	10% to 90% RH non-condensing
Operating	10% to 90% RH non-condensing
POWER	
Input Requirements	5 Volts dc
Signal Level	
Low State (0)	0.4 Volts dc, or less
High State (1)	2.4 Volts dc, or more
Ground	Logic ground is connected to computer logic ground

INTERFACE

A single cable is used to connect either controller with the first transport, while each transport has two identical interconnection plugs to enable daisy chain interconnection. Figure 4-1 shows a typical transport to controller configuration. The interconnecting cable assembly between the controller and the first transport is 20 feet long. The standard cable assembly between each additional transport is 10 feet long. The cables required for operation of the controller are listed in Section 8 (Parts Data).

TERMINATOR

When operating in daisy chain configuration , a terminator (CDC P/N 46338700) is required. The terminator must be placed on the last MTT unit in the daisy chain.

SECTION 2

OPERATION AND PROGRAMMING

PROGRAMMING

SUMMARY OF PROGRAMMING INFORMATION

Tables 2-1 through 2-9 and Figures 2-1 through 2-5 provide the experienced operator with the information necessary to program the magnetic tape transport controller (MTTC). The following paragraphs further define this information.

The MTTC communicates with the AB107/AB108 processor via the computer A/Q channel and DSA channel .

The Q-register designates the equipment to be referenced and directs the operation to be performed upon the input or output instruction execution. Figure 2-1 illustrates the format of the Q-register:

Bits 11-15 must always be zero.
Bits 7-10 select the MTTC; these bits must match the equipment number of the controller.
Bits 2-6 are ignored.
Bits 0-1 (the Director) specify an operation according to Table 2-2.

The MTTC has two modes of operation:

1) Direct:
Operation is initiated and data is transferred via the A/Q channel.

Direct transfer is accomplished in the following sequence:

1. Control Function (Read Motion and Write Motion).
2. Input to A or Output from A instruction for every data word.

2) Buffered:

Operation is initiated through the A/Q, and data transfer is via the DSA.

Buffered I/O transfer is accomplished by issuing the following sequence:

1. Buffered I/O instruction
   (Controller fetches LWA+1 from FWA-1 and waits)
2. Control Function (Read Motion or Write Motion) instruction. Read Data transfer starts when data block moves under the Read head.

   Write Data transfer starts when pre-record gap has passed under the Write head.

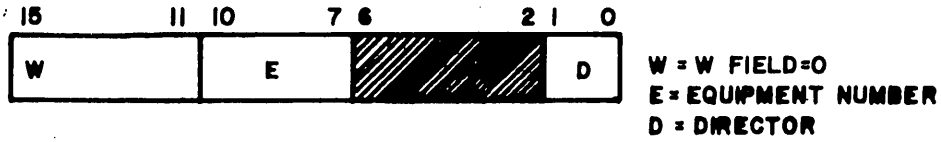

Figure 2-1. Format of Q-Register

Addresses

The W = 0 signal plus bits 10-7 of the Q-register are used to select the MTTC. The W field of Q is always loaded with zeros. Bits 0-1 of Q are used to specify an operation. Figure 2-1 illustrates the format of the Q-Register. Table 2-1 lists the values of E required to select a MTTC with a given Equipment Number setting.

TABLE 2-1. HEXADECIMAL CODE FOR CONTROLLER ADDRESSES

Hexa-decimal code	Jumper Plugs			
	Q10	Q9	Q8	Q7
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

Note:

A "1" in the binary code indicates the presence of a jumper plug for the setting of the equipment code and a "0" indicates its absence.

Bits 10-7 of the A-register are used along with the contents of Q and Output from A to select a tape transport. (See Unit Select).

OPERATIONS

The D field of Q is combined with an AB107/AB108 Input from A or Output from A instruction to specify an operation (see Table 2-2). The operations initiated by an Output from A may be further modified by the contents of the A-register (see Table 2-3, Figures 2-2 and 2-3). The following paragraphs define these operations.

Operations Defined by Q and Output from A

Write: A Write transfers data from the computer to the controller which generates a parity bit and writes the data plus parity bit on the tape. To perform a Write, load Q with $\overline{W}$ = 00*, E = equipment number setting of desired MTTC controller and D = 00.

*$\overline{W}$ is written as two digits; the left, binary; the right, hexadecimal.

An Output from A instruction intiates the transfer of the computer word to the tape. Any number of consecutive characters sent to the tape are written (along with a parity bit) on the tape as a single record. Whenever the computer breaks the continuity of the computer word outputs, the controller initiates an End-of-Record sequence. A Write is rejected if Not Ready, Write Motion has not been initiated, Data Status is not set, if Buffered I/O is set or a Program Protect fault occurs. If no new Control Function is received from the computer, tape motion stops at the next interrecord gap.

TABLE 2-2. MTTC OPERATIONS

Computer Instruction		
D	Output from A	Input to A
00	Write	Read
01	Control Function	Director Status 1
10	Unit Select	Director Status 2
11	Buffered Input/Output	Current Address

Control Function: The Control Function specifies operating conditions for the selected controller and transport and initiates tape motion. To perform a Control Function, load Q with $\overline{W}$=00, E=Equipment Number, and D=01. Load A according to Figure 2-2 and Table 2-3, and execute an Output from A.

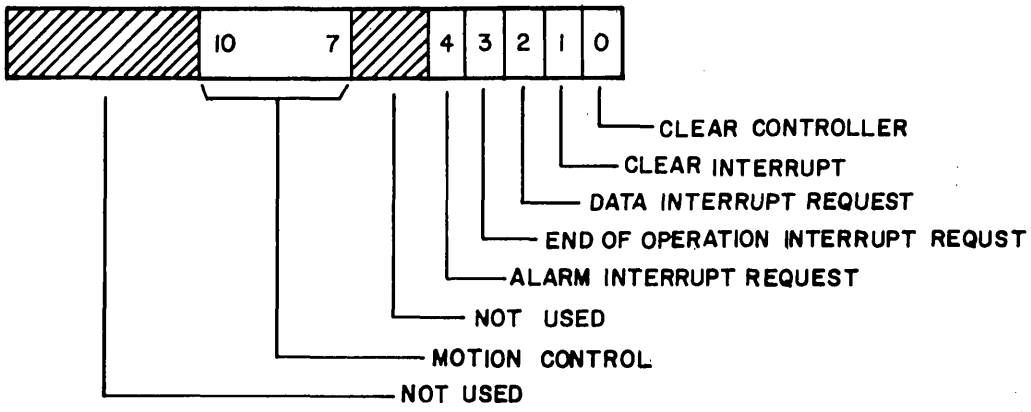

Figure 2-2. Control Function for A-Register

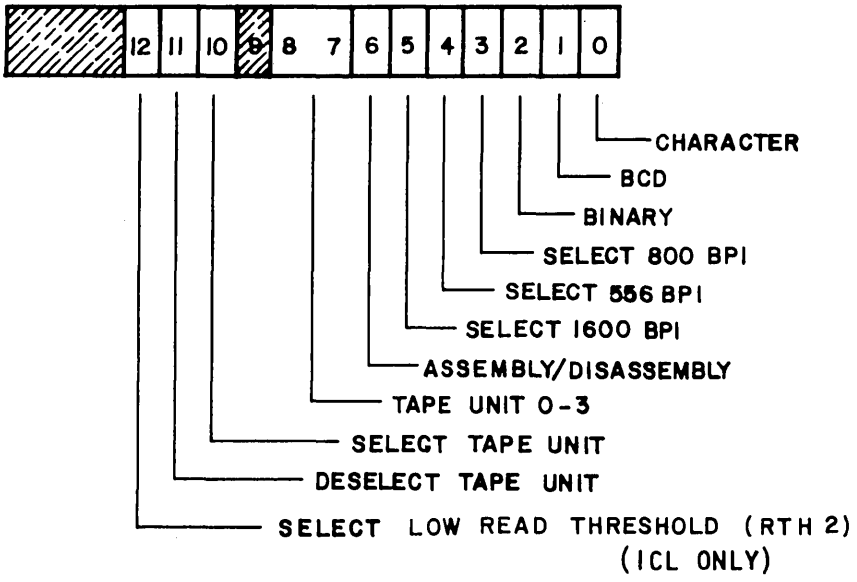

Figure 2-3. Unit Select for A-Register

If bits 7-10 of A equal zero, the control function is rejected only if a protect fault occurs. Otherwise the controller rejects control functions if it is Not Ready, the End-of-Operation status condition is not present, an illegal code exists in bits 7-10 of A, the tape transport is Busy or if a protect fault occurs. Control Function is not rejected if it is issued after EOP status is set and same motion direction is requested and same data transfer direction (Read or Write) is requested (see Table 2-3). Write Motion or Write FM/TM is rejected if the File Protect Ring is absent.

Table 2-3 lists the legal motion control codes. Master clears the MTTC, any or all Clear and Interrupt selections may be selected simultaneously or individually. The requests are honored in this order: Clears, Interrupt selections and Motion Control.

A New Motion Function clears EOP, Alarm and all causes for Alarm.

The following describes these codes:

1) Clear Controller (A00 = 1) - Master clears the MTCC. with the following exceptions: Unit Select, Mode Select, Code Select and Format Select.

2) Clear Interrupt (A01 = 1) - Clears all interruptd and interrupt requests. If an interrupt request is coded along with a Clear Interrupt, that selection is honored, but any previous selections are cleared.

3) Data Interrupt Request (A02 = 1) - causes an interrupt to be generated when an information transfer through A/Q channel may occur. The interrupt response is cleared by the Reply to the data transfer. The request and response are cleared by a Clear Controller or a Clear Interrupt code.

4) End-of-Operation Interrupt Request (A03 =1) - causes an interrupt to be generated at the end of an operation. The request and response are cleared by a Clear Controller or a Clear Interrupt code.

5) Alarm Interrupt Request (A04 = 1) - causes an interrupt to be generated upon a condition which warrants program or operator attention. The Alarm Interrupt is generated by any of the following conditions:

1. End-of-Tape
2. Parity Error
3. Lost Data
4. File Mark/Tape Mark
5. The controller goes Not Ready during an operation.
6. Storage Parity Error
7. Protect Fault
8. ID - Abort
9. PE - Lost Data
10. PE - Warning

6) Write Motion (A10-A07 = 0001) initiates Write Motion if Buffered Input/Output is not set, the Data Status goes true which initiates Direct Data Output. If Buffer I/O is set, Write Motion initiates Buffered Output. Write Motion is terminated (EOP set) when End-of-Record is detected by the Read head.

If buffered I/O is not set, Write Motion is selected and no data transfer follows, the controller locks out and terminates the Write Motion function when it is time to write the first character on tape. Forward drops to the selected transport and the transport goes Not Busy, but no End-of-Operation is generated. To recover from this error condition, a Unit Select or Clear Controller function can be issued to accept another motion function.

TABLE 2-3 MOTION CONTROL

Bits 10-7 of A	Motion Function
0001	Write Motion
0010	Read Motion
0011	Backspace
0101	Write File Mark/Tape Mark
0110	Search File Mark/Tape Mark Forward
0111	Search File Mark/Tape Mark Backward
1000	Rewind Load
1100	Rewind Unload (LCTT Only)

7) Read Motion (A10-A07 = 0010) - initiates Direct or Buffered Data input. Read Motion terminates by absence of data from the magnetic tape transport. If the computer stops requesting characters, data transfer stops, but the tape continues to move to the end of the record. If a data transfer request is not received by the controller in time to complete the transfer properly, the Lost Data status bit is set and subsequent data requests are rejected. If a File Mark is encountered the File Mark status bit is set.

8) Backspace (A10-A07 = 0011) - moves tape backward one record. Backspace from Load Point is not rejected (however the tape will not move) and non-stop backspace is possible.

9) Write File Mark (A10-A07 = 0101) - moves tape forward. approximately 6 inches and writes a File Mark. The normal End-of-Operation sequence follows the File Mark, writing the longitudinal check character.*

10) Search File Mark Forward (A10-A07 = 0110) moves tape forward until a File Mark is detected; an End-of-Operation (EOP) is generated and tape motion stops.

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* A parity error is indicated together with File Mark status if the MTTC is operating in binary format (seven and nine track).

11) Search File Mark Backward (A10-A07 = 0111) - moves tape backward until a File Mark is detected. When it has been detected, an End-of-Operation is generated, and tape motion stops. If no File Mark is detected, an End-Of-Operation will be generated and motion will stop at Load Point.

12) Rewind Load (A10-A07 = 1000) - rewinds tape at high speed to Load Point. The controller remains Busy until tape is positioned at load point and End-of-Operation Status/Interrupt occurs. The MTTC stays Ready upon acceptance of this command.

13) Rewind Unload (A10-A07 = 1100) - rewinds tape to Load Point and unloads. The tape transport becomes Not Ready upon acceptance of the command. Manual intervention is required to reload the tape and place the transport in a Ready condition. (For LCTT only).

Non-Stop Motion: Table 2-4 shows transition time in which a New Motion Function must be initiated to achieve Non-Stop Motion after End-of-Operation Status/Interrupt occurs.

TABLE 2-4. NON-STOP MOTION TRANSITION

Speed	Transition Time		
	Write Forward	Read Forward	Backspace or S.F.B.
ICL 37.5 ips	2.7 msec	2.0 msec	2.7 msec
LCTT 25 ips	3.6 msec	2.6 msec	2.6 msec
LCTT 50 ips	1.8 msec	0.5 msec	0.5 msec
Alternative for next Control Function	1. Write Forward 2. Write File Mark	1. Read Forward 2. Search File Mark Forward	1. Backspace 2. Search File Mark Backward

Unit Select: A Unit Select selects a tape transport and its operating conditions or deselects a transport. To perform a Unit Select, load Q with $\overline{W}$ = 00, E = equipment number, D = 10. Load A according to Figure 2-3 and Table 2-5, and do an Output from A. Tape unit, density, and mode (BCD or binary) can be selected simultaneously or individually. Unit Select is rejected if Controller Active or a Program Protect fault occurs or if an illegal code is selected (for example, two densities chosen) or selection does not match the tape transport or controller settings. Unit Select clears the controller.

Note: After MC, density must be selected again.

TABLE 2-5. TAPE UNIT SELECT CODES

Bits 9-7 Of A	Unit Select Jumper Setting
000	0
001	1
010	2
011	3

1) Character (A0 = 1) - In this format the computer word consists of the lower 6 or 8 bits only. Master Clear sets character format.

2) BCD (A01 = 1) Data is read or written in even parity (615-73 only).

3) Binary (A02 = 1) Data is read or written in odd parity. Master Clear sets Binary code. Binary is selected if BCD is not selected.

4) Select 800 bpi (A03 = 1) Data is recorded at a density of 800 bits per inch. MC sets 800 bpi.

5) Select 556 bpi (A04 = 1) Data is recorded at a density of 556 bits per inch.

6) Select 1600 bpi (A05 = 1) - Data is recorded at a density of 1600 bits per inch in the PE format. This bit can only be used with the PE Formatter.

7) Assembly/Disassembly Mode (A06 = 1) - In this format the computer word consists of 12 or 16 bits which, during a Write, are disassembled into two 6-or 8-bit tape words. During a Read, the tape words are assembled into the original computer word.

8) Tape Unit 0-7 (A09 = 1) - This code matches the Unit Select setting of the desired transport.

9) Select Tape Unit (A10 = 1) - This code and bits 9-7 of A selects a tape transport.

10. Deselect Tape Unit (A11 = 1) - This bit disconnects a tape transport that is selected and protected, thus allowing an unprotected program access to the controller. Deselect Tape Unit must be a singular type function. Master Clear deselects all units.

11. Select Low Read Threshold (A12 = 1) - This bit is used to select the low read threshold level used for data recovery. Used for ICL only.

    The controller reverts to normal read threshold when:

    (a) The Unit-Select function contains A12 = 0.

    (b) After any EOP.

    (c) Master Clear.

Buffered Input/Output: A Buffered I/O instruction initiates the transfer of data between the controller and the computer memory via the DSA. To execute Buffered I/O, load Q with W=00, E= equipment number and D=11. Load A with the first word address minus one (FWA-1) which contains the last address plus one (LWA+1).

An Output from A instruction transfers the FWA-1 and LWA+1 into the controller (via the A/Q and DSA respectively).

The transfer of data will start after Write or Read Motion. The data transfer will terminate when current word address equals LWA+1, or when reading the End-of-Record is sensed. Lost Data conditions will occur when the DSA does not keep up the transfer rate.

A Buffered I/O instruction is rejected if EOP status is not set and Busy is set, the tape transport is not ready or a Program Protect Fault occurs.

Operation Defined by Q and Input to A

Read (D = 00): A Read operation transfers data from tape to the computer and checks parity. To perform a Read, load Q with $\overline{W}$ = 00, E = equipment number, and D = 00. An Input to A initiates the transfer of one 6-, 8-, 12- or 16-bit character to the lower bits of the A-register.

The controller transfers characters to the computer until the computer stops requesting characters, or until the controller senses the end of a record. If the computer stops requesting characters, data transfer to the computer stops, but tape motion continues until the end of the record. A Read is rejected if the controller is Not Ready, read motion has not been set, data status is not set, a Program Protect fault occurs, or a Buffered I/O operation is in process.

Director Status 1 (D = 01): Director status 1 is a status request which loads into the A-register a status reply word showing the current operating conditions of the MTTC. The request is initiated by loading Q with $\overline{W}$ = 00, E = equipment number, D = 01, and executing an Input to A. Table 2-6 describes the contents of A-register following the execution of this function. The Status Response section defines these bits.

Director Status 2 (D = 10): Director Status 2 is a status request which loads the A-register a status reply word of the MTTC. The request is initiated by loading Q with $\overline{W}$ = 00, E = equipment number, D = 10, and executing an Input to A. Table 2-7 describes the contents of A-register following the execution of this function. The Status Response section defines these bits.

Current Address (D = 11): This instruction is a status which loads into the A-register the address of the next word being transferred. To perform a Current Address, load Q with W = 00, E = equipment number and D = 11, and initiates an Input to A.

Status Response

Director Status 1

Table 2-6 lists the meaning of bits set in the A-register following a Status 1 request. These bits are further defined below.

Ready (A00 = 1): The tape transport is connected to the equipment and the tape system can perform a command.

Busy (A01 = 1): Equipment is in motion. The MTTC becomes Busy before a Reply is returned if a function can be performed.

Interrupt (A02 = 1): An interrupt condition exists and interrupt upon this condition has been selected. This bit is cleared when the interrupt is cleared.

Data (A03 = 1): A Read/Write data transfer can now be performed. It is cleared by a data transfer request. Lost Data or End-of-Record sequence.

End-of-Operation (A04 = 1): A new tape function can now be accepted. This bit sets at the completion of all tape motion function except Rewind Unload. During Read and Write, End-of-Operation (EOP) signifies that parity status is valid. Master Clear clears EOP. A New Motion Function can also be used to clear EOP.

TABLE 2-6. DIRECTOR STATUS 1 RESPONSE BITS

Bit Set In A-Register	Meaning
0	Ready
1	Busy
2	Interrupt
3	Data
4	End-of-Operation
5	Alarm
6	Lost Data
7	Protected
8	Parity Error
9	End-of-Tape
10	BOT
11	File Mark
12	Controller Active
13	Fill
14	Storage Parity Error
15	Protect Fault

TABLE 2-7. DIRECTOR STATUS 2 RESPONSE BITS

Bit Set in A-Register	Meaning
0	556 bpi
1	800 bpi
2	1600 bpi
3	Seven Track
4	Write Enable
5	PE-Warning
6	PE-Lost Data
7	PE-Transport
8	ID-Abort
9	Low Read Threshold (For LCTT only)
10	(Not Used)

Alarm (A05 = 1): This status bit monitors those conditions requiring the attention of the program or the operator. The following conditions set this bit as well as their own status bit:

1) End-of-Tape
2) Parity Error
3) Lost Data
4) File Mark
5) The Controller goes Not Ready during an operation
6) Storage Parity Error
7) Protect Fault
8) ID - Abort
9) PE - Lost Data
10) PE - Warning

A New Motion Function or Clear Controller will clear Alarm.

Lost Data (A06 = 1): This bit indicates during an A/Q Read transfer that the Data Transfer register was not empty when a new frame of data was received from the tape transport. This clears Data Status and Data Interrupt.

This bit indicated during a Buffered I/O transfer that the computer's DSA bus has not been able to keep up to the MTTC data transfer rate. During Buffered Output it initiates an End-of-Record sequence. During Buffered Input it stops data transfer. A New Motion Function clears Lost Data.

Protected (A07 = 1): This bit indicates that the Program Protect Jumper Plug of the selected tape transport is set.

Parity Error (A08 = 1): An error was detected during data transfer, or the controller has read or written a File Mark in binary mode; or done a Read operation in the wrong mode or density. The parity check is complete and a Parity Error status is valid at end of operation. Parity is not checked on Backspace. This condition responds to transverse, longitudinal and cyclic redundancy parity errors. When reading PE tapes this bit indicates a Parity Error only when no dropout is detected. Parity error is cleared by issuing a New Motion Function.

End-of-Tape (A09 = 1): An End-of-Tape (EOT) marker has been sensed. A New Motion Function clears EOT.

Load Point (A10 = 1): The tape Load Point has been sensed.

File Mark (A11 = 1): A File Mark has been sensed. It is cleared on a New Motion Function.

Controller Active (A12 = 1): MTT Controller is active controlling tape motion.

Fill (A13 = 1): If an odd number of tape words is read, this status will be set to indicate that the lower portion of the Read word is not a tape word. A New Motion Function clears Fill.

Storage Parity Error (A14 = 1): Storage Parity Error has occurred during a DSA channel transfer. A MTT controller New Motion Function clears Storage Parity Error.

Protect Fault (A15 = 1): The computer's Protect Fault flag was active during a MTT controller-DSA channel transfer New Motion Function clears Protect Fault.

Director Status 2

Table 2-7 lists the meaning of bits set in the A-register following a Status 2 request. These bits are further defined below:

556 bpi (A00 = 1): The selected tape unit is set to operate at a density of 556 bits per inch.

800 bpi (A01 = 1): The selected tape unit is set to operate at a density of 800 bits per inch.

Seven Track (A03 = 1): The selected tape unit is a seven-track transport. This bit should always be set when a seven-track MTT is selected and never be set when a nine-track MTT is selected.

Write Enable (A04 = 1): The File Protect ring is in the supply reel and the tape has been loaded. Write operations may now be performed.

PE Transport (A05 = 1): Selected transport (nine-track MTT only) can record 1600 bpi density and the PE Formatter is in.

The following status bits may be active only with the PE Formatter installed.

1600 bpi (A02 = 1): The selected tape unit (nine-track MTT only) is set to operate at a density of 1600 bits per inch.

PE-Warning (A05 = 1): This bit indicates an error in the PE Formatter which did not affect the data transfer. The following conditions set this bit:

a) Corrected Dropout; one dropout occurred during reading of present record.

b) Wrong Postamble; Postamble exceeds 48 zeros or contains ones. This is cleared by a New Motion Function.

PE-Lost Data (A06 = 1): This bit indicates an error in the PE formatter which affected the data transfer. The following conditions set this bit:

a) skew buffer overflow
b) multitrack dropout
c) preamble format error

ID Abort (A08 = 1): 1600 bpi was selected (nine-track MTT only) but no Identification burst was detected after starting of tape motion from BØT. ID Abort triggers Alarm and tape motion is stopped. Operation will continue after issuing a New Motion Function.

INTERRUPTS

Interrupts are selected by the Control Function. They may be cleared by:

1) Issuing a Clear Interrupt which clears both the Interrupt request and the interrupt.

2) Re-issuing the Interrupt Request except for the Alarm Interrupt when the Alarm condition still exists, e.g., End-of-Tape.

3) Issuing a Clear Controller.

4) Transferring data in the case of the data interrupt.

5) Reselecting a unit.

OPERATION

The jumper plugs indicated herein are located as shown in Tables 3-2 through 3-5 and in Figures 3-2 and 3-3. The PWA's on which the jumper plugs may be installed can be accessed by opening the front door of the computer enclosure. The jumper plug positions are located on two of the controller PWA's as indicated below.

On the Q-Channel PWA (installed in enclosure position 12)

EQUIPMENT NUMBER JUMPER PLUG

These four jumper plugs are used to represent any number from 0 to 15_{10}. They are used to assign an equipment to the MTTC. Any instruction sent by the computer must be accompanied by an equipment number (bits Q10 through Q07 matches the settings of the jumper plugs). The position is set if the jumper plug is inserted.

SCANNER JUMPER PLUG

When performing maintenance operations and for initial installation of the controller, the Scanner jumper plug should be installed in one of the four positions indicated below:

1) Middle
2) First
3) Last
4) One

These names reflect the controller's position within the DSA bus. This varies with the system.

On the Lower Data Section PWA (installed in Location 13):

PROTECT ON/OFF JUMPER PLUGS

There are four jumper plugs; one per tape transport. When any tape transport is selected, the presence of this jumper allows only protected instructions (except status requests) to access the MTTC.

If a buffered input is initiated by a Protected instruction, a Protect signal is sent to the computer allowing data to be written into any storage location.

SPEED SELECT JUMPER PLUGS

There are four jumper plugs; one per tape transport. These jumpers should be set according to the speed of the corresponding tape transport - either high speed (50 ips for ICL and 75 ips for LCTT) or low speed (25 ips and 37.5 ips for LCTT). With the jumper plug inserted, tape speed is high speed.

TRACK SELECT JUMPER PLUGS

There are four jumper plugs; one per tape transport. These jumpers should be set according to the track type (seven-track or nine-track) of the corresponding tape transport. With the jumper inserted, the nine-track tape is selected.

MODULATION SELECT JUMPER PLUGS

There are four jumper plugs; one per tape transport. These jumpers should be set according to the capability of the tape transport - either NRZI or PE (provided nine-track and Not Dual Mode are selected.

DUAL MODE JUMPER PLUGS

There are four jumper plugs; one per tape transport. These jumpers must be inserted when the MTT is capable of dual mode operation (NRZI/PE) provided the Track Select jumper plugs are also set to nine-track.

SECTION 3
INSTALLATION AND CHECKOUT

INSTALLATION

UNPACKING

1. Carefully remove wrapping from the controller cards. Check for physical damage to each card and record damage on the packing list. Check that part numbers agree with parts list.

2. Remove wrapping from cables and check for physical damage. Record damage on packing list. Check that part numbers agree with packing list.

PHYSICAL LIMITATIONS

Care must be taken to prevent damage to the controller cards. The cards must not be flexed, bent or dropped.

POWER REQUIREMENTS

The controller cards require +5 vdc derived from the power supply of the computer.

CABLING AND CONNECTORS

An external interconnecting cable is available for use with the controller for connection between the computer and the first tape transport. The external cable is 20 feet long (part number 89775500 for ICL MTT or 89899000 LCTT MTT).

The two internal cables (part number 89700200 for either the ICL or LCTT MTTC) used between the back of the computer and the connector panel on the backplane, are 18 inches long.

The interrupt cable (part number 89724702) is 13.8 inches long. Refer to Table 3-6 for pin assignments.

The last tape transport must be equipped with a terminator (CDC part number 46338700).

The total length of all interconnecting cables from controller to last unit in daisy chain must not exceed 50 feet.

The wire list for pin assignments will be found in Section 8.

COOLING REQUIREMENTS

The controller cards are cooled by the forced air system of the computer. No further cooling is required.

ENVIRONMENTAL CONSIDERATIONS

The environmental considerations necessary for operation (or storage) of the controller cards are listed in the Detailed Specifications of Table 1-1.

PREPARATION AND INSTALLATION

Refer to the System 17 installation Manual 88996000.

To install the controller perform the following steps with the computer power off:

1. Refer to Figures 3-1 for selection of the proper location for installation of the PWA in the main enclosure. Also see Table 3-1.
2. Inspect the enclosure, PWA slot, slides and connector pins at the locations to be used, to be sure that there is no physical damage to them.
3. Place the internal select jumper plugs in the relevant positions on the controller PWA, as described in Tables 3-2 through 3-5, and in Figures 3-2 and 3-3.

   CAUTION

   Do not install or remove cables or PWA from the enclosure with system power turned on.

4. Carefully install the controller PWA in the assigned enclosure slots as shown in Table 3-1 and Figure 3-1. The PWA must slide into position smoothly and be fully seated before applying power to the system.
5. Remove back cover of enclosure.
6. Install the internal cable (part number 89700200 for either the ICL or LCTT MTT) between the selected slot Connector P2 for the PWA on the backplane and the back of the enclosure.
7. Connect the external cable (part number 89775500 for the ICL MTT or 89899000 for the LCTT MTT) between the internal cable connector on the back of the enclosure and the card punch device.
8. Place the interrupt cable (part number 89724702) on the enclosure backplane as required. Refer to Table 3-6 for selection of position.
9. Replace back cover of enclosure.

TABLE 3-1. MTTC PW BOARD LOCATIONS

Assembly Board	Location (Slot) in Computer
Tape Interface	11*
Q-Channel	12**
Lower Data Section	13**
Upper Data Section	14*

* Internal Cable is connected to PWA backplane at slots indicated. Connection is made at P2 of each location.
** Manual select jumper plugs are placed on PWA's indicated. See Table 3-2.

TABLE 3-2. JUMPER PLUG LOCATIONS

Jumper Plug	Assembly	Slot	Position
Equipment Number	Q-Channel	12	At U2
Scanner Select	Q-Channel	12	At U2
Protect On/Off	Lower Data	13	At U1
Speed Select	↕	13	At U1
Track Select		13	At U18
Modulation Select		13	At U18
Dual Mode Select	Lower Data	13	Above U35

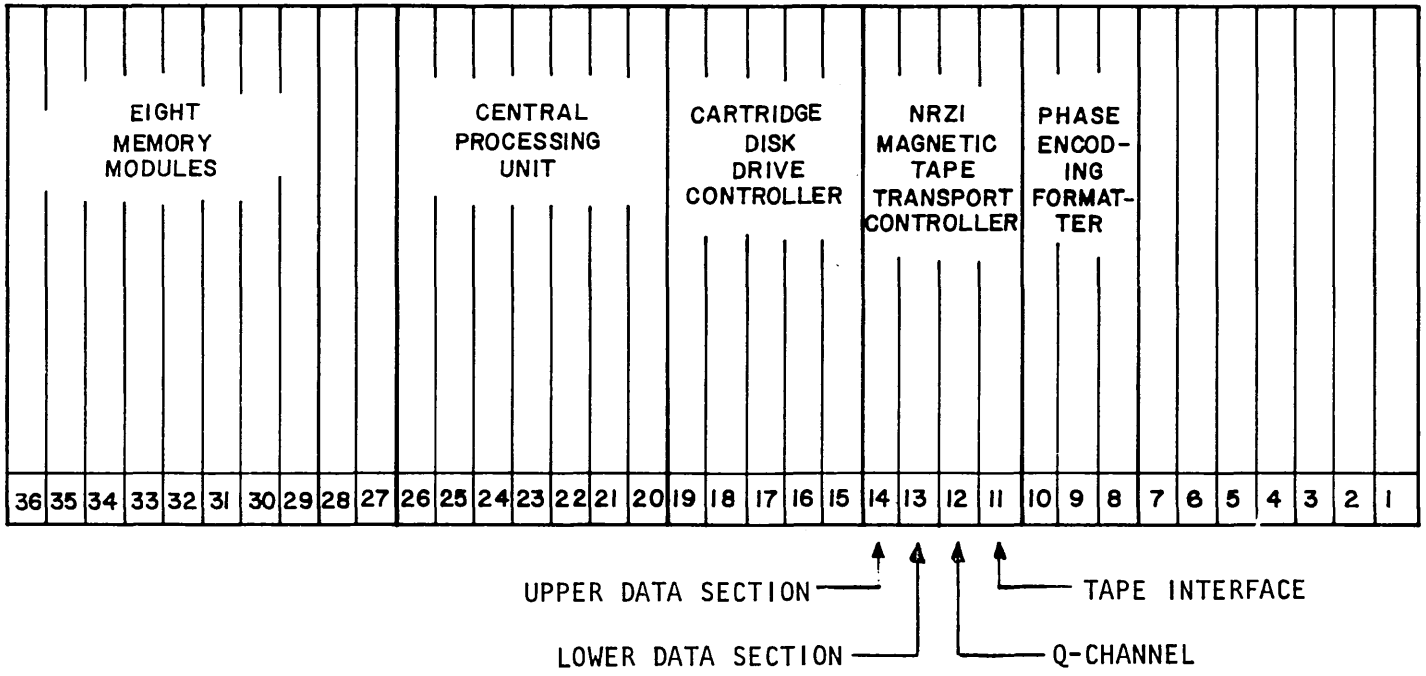


Figure 3-1. Locations for installation of MTT Controller in Main Enclosure.

TABLE 3-3. INTERNAL SELECTIONS ON Q-CHANNEL PWA (See Figure 3-2).

TO SELECT		AT LOCATION	ACTION
EQUIPMENT NUMBER			
(Refer to Table 3-4 and Figure 3-2)	Q07 = "1"	Next to U3	Install Jumper Plug
	Q08 = "1"	" " "	" " "
	Q09 = "1"	" " "	" " "
	Q10 = "1"	" " "	" " "
	Q07 = "0"	" " "	Delete Jumper Plug
	Q08 = "0"	" " "	" " "
	Q09 = "0"	" " "	" " "
	Q10 = "0"	" " "	" " "
SCANNER			
	L = Last F = First M = Middle O = One	Next to U3	Select one position only - For use during installation or maintenance operation.

TABLE 3-4. EQUIPMENT NUMBER REPRESENTATION

HEXADECIMAL CODE OF E-FIELD (Q10-Q07)	INSTALL JUMPER PLUG ON Q-CHANNEL PWA AT			
	Q10	Q09	Q08	Q07
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

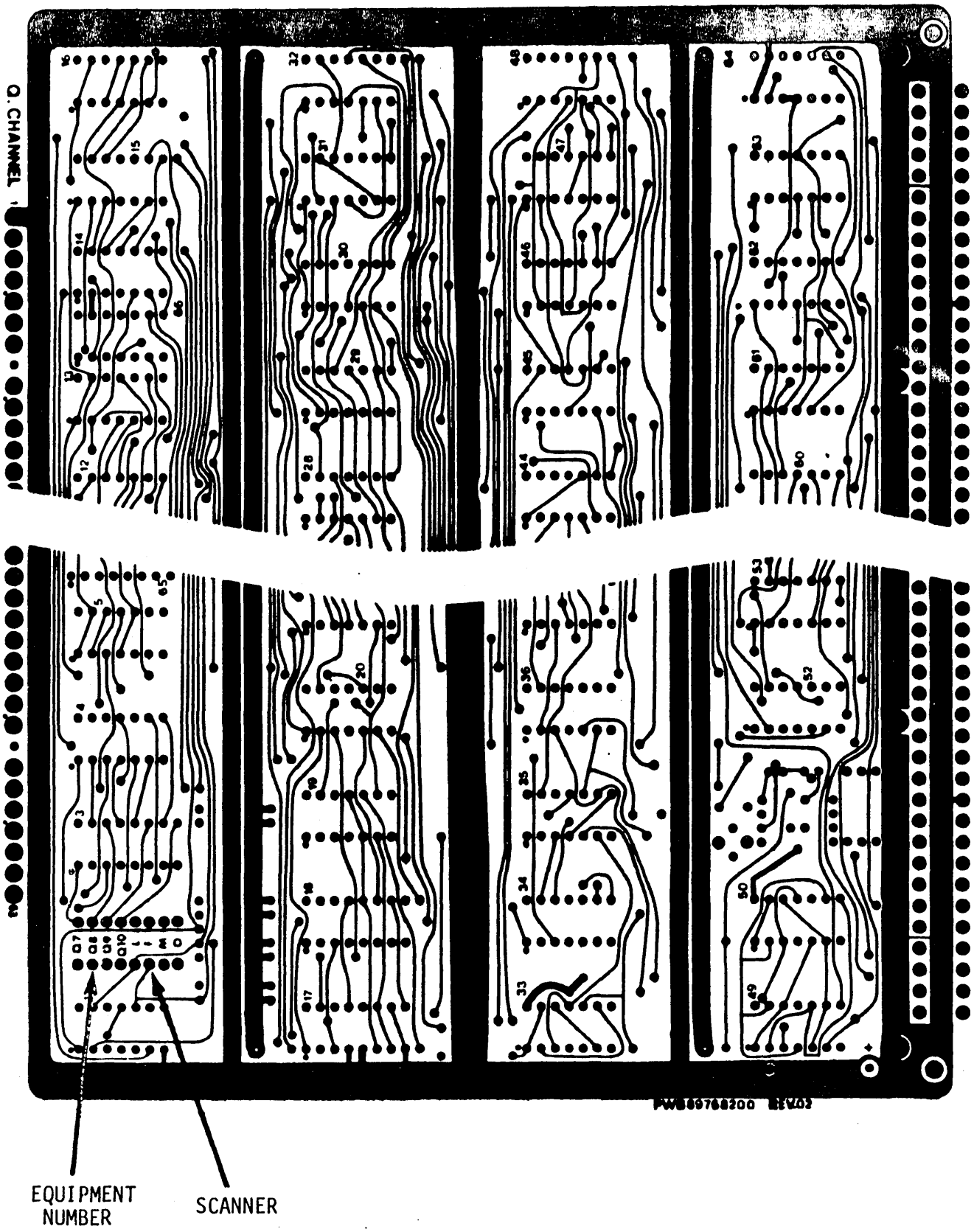


Figure 3-2. Q-Channel Showing Jumper Plug Positions

TABLE 3-5. INTERNAL SELECTIONS ON LOWER DATA PWA (See Figure 3-3)***

For Transport Type	In/Out at location Indicated			Density
	9 TRACK	DUAL (mode)	PE (modulation	
7 Track NRZI	OUT*	OUT	OUT	556/800 bpi
9 Track NRZI Only	IN**	OUT	OUT	800 bpi
9 Track PE Only	IN	OUT	IN	1600 bpi
9 Track Dual Mode	IN	IN	OUT	800/1600 bpi

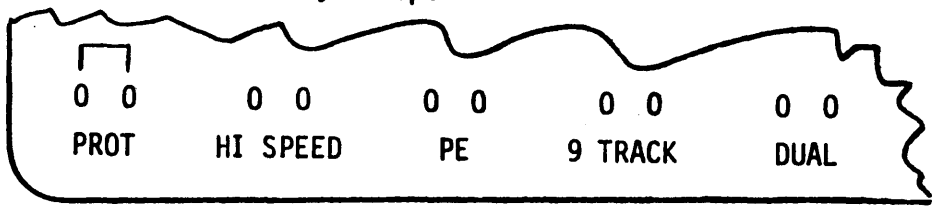
*OUT means remove jumper plug.
**IN means place jumper plug.
***Four positions, for each of four possible MTT's are Provided.

PROTECT Position (Lower Data Section PWA only).

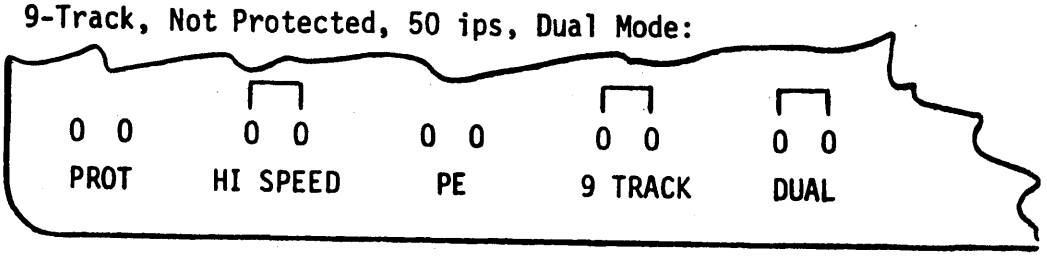
With jumper plug installed, only Protected instructions are accepted. One position for each of the four allowable MTT's is provided. The markings representing each of the MTT's is placed the TRACK and DUAL on this PWA.

Example for using jumper plugs.

7-Track, Protected, 25 ips:



9-Track, Not Protected, 50 ips, Dual Mode:



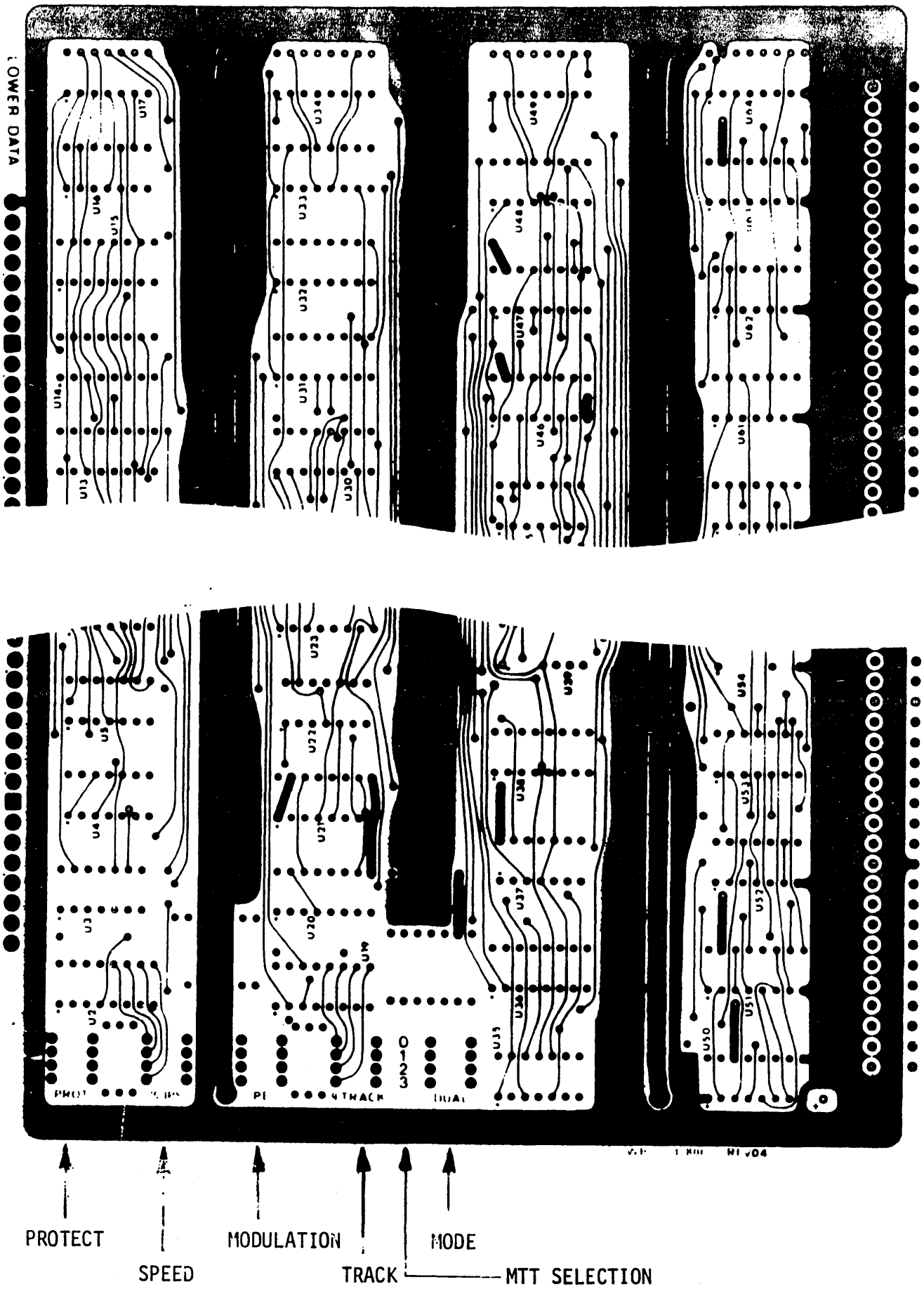


Figure 3-3. Lower Data Section Showing Jumper Plug Positions

89637700 A

TABLE 3-6. INTERRUPT CABLE POSITIONS

Interrupt	Position
A/Q Interrupt	Slot 12 P2A16

Selection may be made from any of the following:

Priority	Position
Line 1	Slot 25 P1B10
" 2	" 25 P1A7
" 3	" 25 P1B7
" 4	" 25 P1A5
" 5	" 25 P1A6
" 6	" 25 P1B6
" 7	" 25 P1B5
" 8	" 26 P1A10
" 9	" 26 P1B10
" 10	" 26 P1A7
" 11	" 26 P1B7
" 12	" 26 P1A5
" 13	" 26 P1A6
" 14	" 26 P1B6
" 15	" 26 P1B5

CHECKOUT

1. Refer to Section 2 of this manual for operation and programming of the controller.
2. Perform a diagnostics check to insure that the controller is operating properly. The diagnostics check is described in the System Maintenance Monitor Manual (SMM17), publication number 60182000.

SECTION 4

THEORY OF OPERATION

FUNCTIONAL DESCRIPTION

INTRODUCTION

This section presents general and detailed functional descriptions of the equipment, using aids such as overall and detailed block diagrams and timing diagrams. Descriptions are keyed to the detailed logic diagrams in the Diagram Section (Section 5) and afford a basis in understanding the detailed description of the specific circuit in that section.

NOTE

It is assumed that the reader is familiar with Control Data equipment and with the programming characteristics of the computer as described in the 1784 Computer System Reference Manual, publication number 89633400.

The basic configuration is shown in Figure 4-1 and the block diagram in Figure 4-2.

GENERAL

Either of the magnetic tape transport controllers transfers data between the computer and the magnetic tape transport (MTT) either directly in NRZI modulation or in phase modulation via the FV497-A (ICL) or FV618-A (LCTT) Phase Encoding Formatter (PEF).* Communication with the computer is either via the A/Q Channel or the DSA Channel of the computer. The formatter is either Character or Assembly/Disassembly, one or two character word, respectively.

Communication with the MTT is via nine Read Data and nine Write Data lines with the appropriate strobe signal, according to either nine or seven track (9T, 7T) standard format. Communication with the PEF is via the following 9-bit buses: PEWRITE DATA IN, PEWRITE OUT, PEREAD DATA OUT or PEREAD DATA IN, with the appropriate strobe signals.

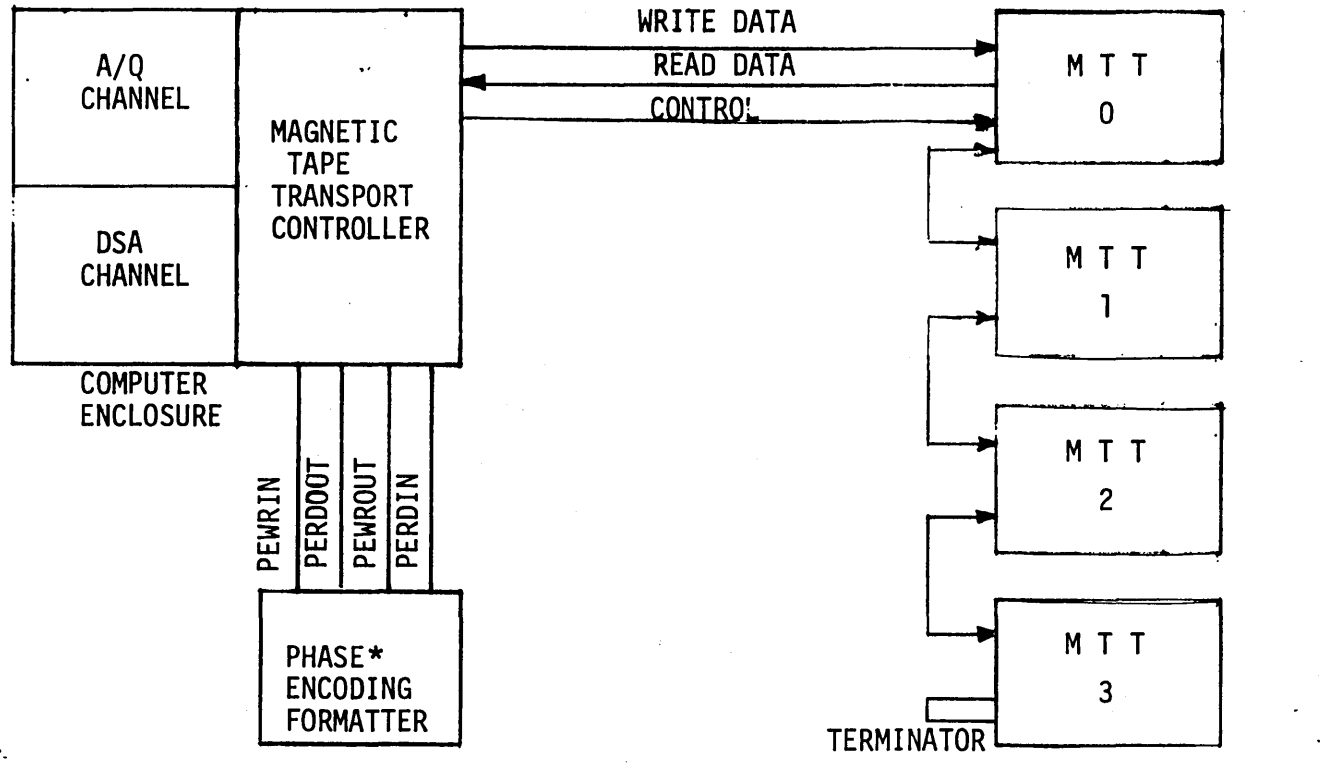


Figure 4-1. Basic Configuration

* Refer to the FV497-A/FV618-A Phase Encoding Formatter Customer Engineering Manual (publication number 8963796100).

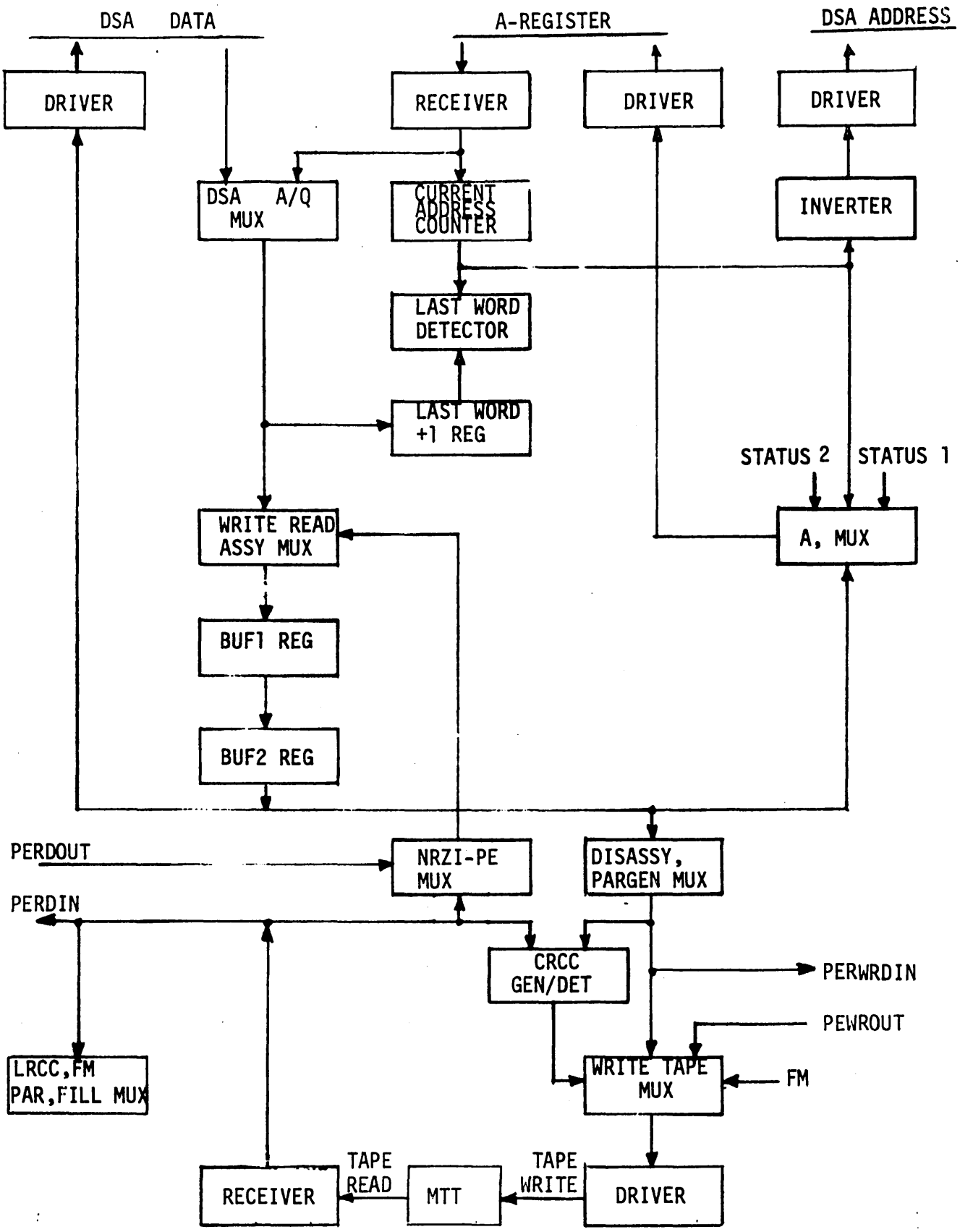


Figure 4-2. Controller Block Diagram

The MTTC executes the following computer instructions according to the system's requirements:

Write Data
Control Function
Unit Select
Buffered I/O
Read Data
Read Status 1
Read Status 2
Read Current Address

The MTTC controls the following motion functions of the tape transport:

Write Motion
Read Motion
Backspace
Write File Mark
Search File Mark Forward
Search File Mark Backward
Rewind - Load
Rewind - Unload

Vertical and Horizontal Parity and CRC are checked when reading. Two 16-bit Data Buffers are provided for in order to double the momentary data rate to decrease the probability of Lost Data.

The MTTC can communicate with up to four tape transports, having speeds of either 37.5 or 75 ips for ICL, and 25 ips for LCTT. The MTT can have the densities and modulations shown in Table 4-1.

TABLE 4-1. DENSITY-MODULATIONS

Density	Modulation	Tracks
800 bpi	NRZI modulation	9
1600 bpi	PE modulation	9
800/1600 bpi	Dual mode	9
556/800 bpi	NRZI modulation	7

WRITE DATA PATH

Data from the A-Register or DSA Data Bus is transferred to the tape transport. The block diagram shows the data path.

1. A/Q transfer: A word from the A-Register passes through the Receivers to the A/Q-DSA Multiplexer, to the Read/Write Assembly Multiplexer, through the Buffer 1 Registers and Buffer 2 Registers. The characters are transferred via the Write Tape Multiplexer and Drivers to the MTT. Every character passes through the CRCC Generator and at the end of the record the CRCC is transferred to the tape. In order to write a File Mark, the FM character and related LRCC is transferred through the Write Tape Multiplexer.

2. DSA transfer: The FWA-1 Control Word is transferred from the A-Register to the Current Address Counter. The LWA+1 Control Word is transferred from the DSA Data Bus vis the A/Q DSA Multiplexer to the Last Word+1 Register. All the succeeding words pass through the A/Q DSA Multiplexer to Read/Write Assembly Multiplexer and further to the double buffer as in A/Q transfer. After every word is transferred the Current Address Counter is incremented by one, the contents of the CAW are then passed through the Inverters and Drivers to the DSA Address.

READ DATA PATH

Data from the MTT is transferred to the A-Register or DSA Data Bus.

A/Q transfer: A character is transferred from the MTT through the Receivers to the NRZI/PE Multiplexer. The character is also transferred to the CRCC Generator and the LRCC, FM, Parity, Fill Check. The character passes through PE Read in the case of the Phase Encoded Read. The character is assembled into a word in the Read/Write Assembly Multiplexer and then transferred to the Double Buffer. From Buffer 2 the word passes through the A-Multiplexer and Driver to the A-Channel.

CLOCK

The basic clock pulse is generated by a crystal oscillator with frequencies of 15.36 MHz for LCTT. It is divided by 4 to form the GATED CLOCK pulse train and the four time states T1 - T4 pulse trains.

REPLY/REJECT TIMING

When the computer READ or WRITE signal rises, and the Equipment Number of the Q-Register matches the setting of the Equipment Number jumpers, the signals R1 - R5 are generated. R1 is set at the first GATED CLOCK pulse after the rise of the READ or WRITE signal. R1 is reset and R2 is set at the next GATED CLOCK pulse, then R3, R4 and R5 are set and reset in turn. R5 is reset by falling of the READ or WRITE pulse.

At this time the following occurs:

At R2:

At the rising of R2 the Reply condition is strobed into the Reply Control FF.

At R3:

1. Strobing of one word in an A/Q Write operation (STRWR).
2. Strobing of First Word Address Minus One in a Buffered I/O instruction (STRBUF).

At R4:

1. Strobing of the Unit Select Code (STRUS).
2. Strobing of the Interrupt Selection and Motion Function in a Control Function operation.
3. Setting of the Data Status (or Need in the DSA) in Write Motion (STRWMØT).

At R5:

1. Reply or Reject is transmitted to the computer.
2. At the falling of R5 the data transmitted to the computer (ENA, ENARD) is removed from the bus.

BASIC TIMING GENERATOR

The following waveforms are generated from T1 and T3 when the speed of the MTT is 37$\frac{1}{2}$ ips for ICL and 25 ips for LCTT frequency is doubled if the tape transport speed is 75 ips for ICL and 50 ips for LCTT):

1. PECHARCLK, frequency 60 kHz for ICL and 40 kHz for LCTT, symmetric waveform, changes with rising of T1.
2. PECLOCK, 240 kHz for ICL and 160 kHz for LCTT, symmetric, changes with T3.
3. GAPCLOCK, 12 kHz for ICL and 8 kHz for LCTT, 70% duty cycle, rising with T1, falling with T3.
4. 2FWC, when the 800 bpi transport is connected the frequency is 30 kHz for ICL and 20 kHz for LCTT. One pulse of 250 nanoseconds for ICL and 375 nanoseconds for LCTT coinciding with T1. With the 556 bpi transports the frequency is 20.87 kHz for ICL and 13.91 kHz for LCTT.
5. Early WDS, Write Clock and WDSShidted are ar the frequencies shown in Table 4-2.

TABLE 4-2. TIMING GENERATOR FREQUENCIES

Speed		Density	
		800 bpi	556 bpi
ICL	37.5 ips	30 kHz	20.87 kHz
	75 ips	60 kHz	41.74 kHz
LCTT			
	25 ips	20 kHz	13.91 kHz
	50 ips	40 kHz	27.82 kHz

The relations between the waveforms (Early WDS, Write Clock, WDSShifted) are shown in Figure 4-3. They are generated only at Write Motions after Start rises.

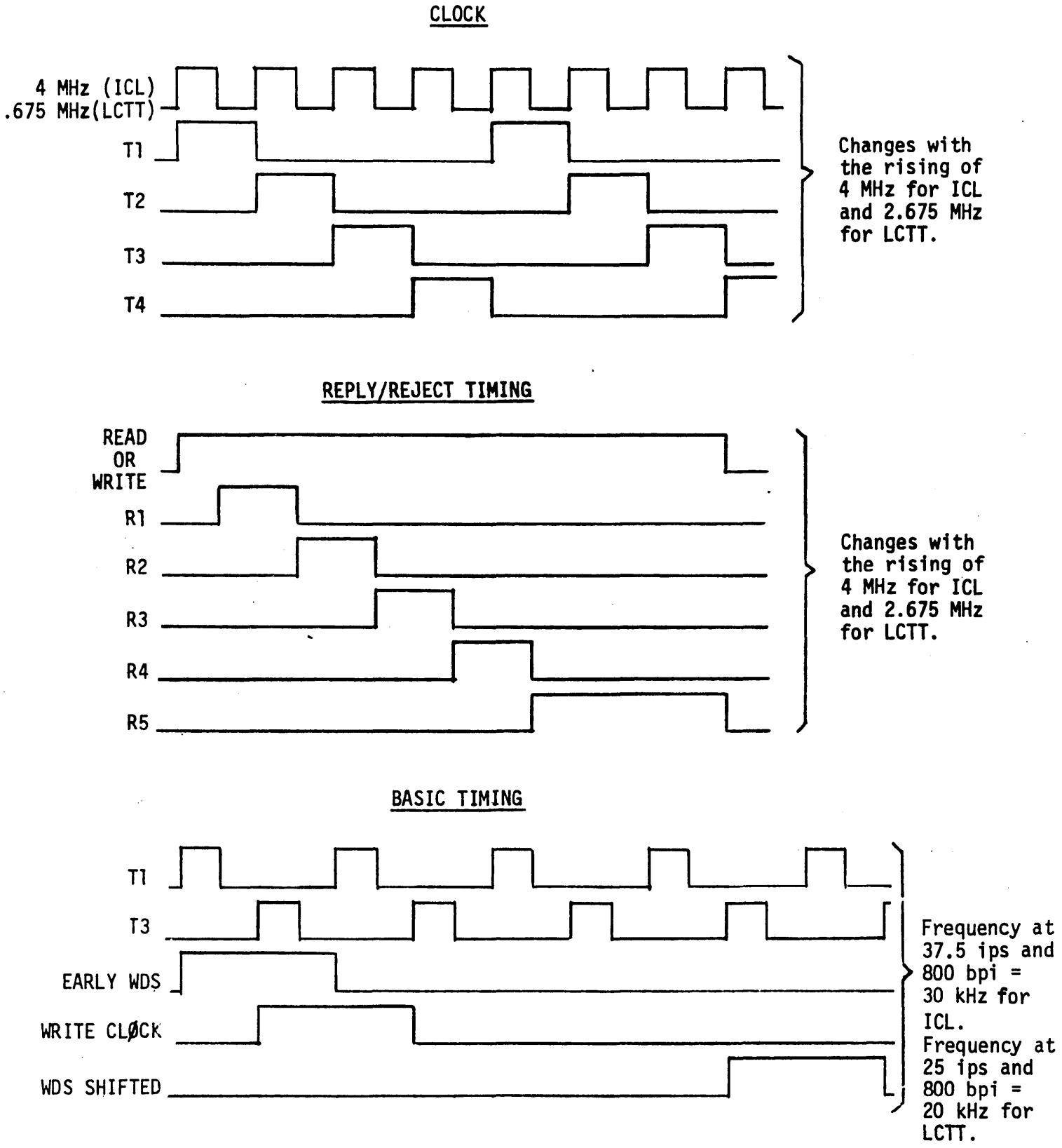


Figure 4-3. Basic Timing Generator Pulses

REPLY CONDITIONS

For every operation the Reply condition is determined and strobed into RC flip-flop (FF) at the rising of R2. The Reply conditions are determined according to the Q-Register, A-Register, Status FF's and return signals from the selected tape transport. The following equations determine the Reply conditions for the operations:

1. Read Data: $RM\emptyset T \cdot DATA \cdot READY \cdot PR\emptyset T\emptyset K$
2. Read Status I: Always replied to
3. Read Status II: Always replied to
4. Read Current Address: Always replied to
5. Write: Data: $WM\emptyset T \cdot DATA \cdot READY \cdot PR\emptyset T\emptyset K$
6. Control Function: $LEGCF \cdot READY \cdot PR\emptyset T\emptyset K$

   Legal control function: $LEGCF = LEGMF \cdot (A10 + A8 + \overline{FILE\ PR\emptyset TECT})\ (\overline{BUSY} + NSC\emptyset ND \cdot E\emptyset P)$

   Legal motion function: $LEGMF = A7 \cdot A10 + A10 \cdot A8 + \overline{A10} \cdot \overline{A8} \cdot \overline{A10}$

   Non Stop Condition : $NSC\emptyset ND = LEGMF \cdot \overline{A10}\ (\overline{A7} + M\emptyset TC\emptyset DE7)\ (\overline{A8} + M\emptyset TC\emptyset DE8)$

7. Unit Select: $LEGUS \cdot PR\emptyset T\emptyset K$

   Legal Unit select: $LEGUS = Z \cdot Z_F \cdot \overline{C\emptyset NTACT} \cdot (PC160\emptyset + \overline{A5})$

   $Z = DUAL \cdot B\emptyset T \cdot 9T + DS(A5 \cdot 9T + A3 \cdot \overline{9T}) + DS(A3 \cdot 9T + A4 \cdot 9T)$

   $Z_F = A4 \cdot 9T + A5 \cdot \overline{9T} + A1 \cdot 9T + (A5 \cdot 9T + A3 \cdot \overline{9T}) \cdot (A3 \cdot 9T + A4 \cdot \overline{9T}) + A0 \cdot A6 + A1 \cdot A2 + A9 + A10 \cdot A11$

8. Buffered I/Ø: $(E\emptyset P + \overline{BUSY}) \cdot READY \cdot PR\emptyset T\emptyset K$

EXECUTION STROBES

The execution strobes are generated only if the appropriate reply conditions hold at time R2-R4, ENA:

ENARD = ENA•RC•RD
STRWR = R3•RC•WR
STRINT = R4•RC•CF
STRCF = R2•RC•CF
STRMF = R4•RC•CF•LEGMF
STRWMØT = R4•RC•CF•A7•$\overline{A8}$•$\overline{A9}$•$\overline{A10}$
STRUS = R4•RC•US
STRBUF = R3•RC•BUF
SELA0 = RD+DS1
SELA1 = RD+DS2

UNIT SELECT

Unit Select operation selects the operation conditions. All the conditions are stored in flip-flops that are clocked by STRUS according to the contents of the A-Register. STRUS occurs at R4 if unit select operation is executed and the reply conditions are met. The operation conditions are preset by MC.

1. Select or deselect a tape transport. A transport can be selected only if A10 is set. It is deselected if A11 is set or MC is issued.
2. The Unit Number 0-3 is selected only if A10 is set.
3. Character or Assembly/Disassembly format. It is preset to Character format by MC.

4. BCD or Binary code. BCD is selected only if A01 is set, in all other cases Binary is set.

5. 800, 556, or 1600 bpi density. Density 800 bpi/1600 bpi can be changed only when a dual mode nine track transport is selected.

6. In the case of LCTT:

   (a) 556 may be selected if: seven-track transport.
   (b) 800 may be selected if: seven-track transport, or nine-track dual transport, or nine-track NRZI transport (not PE transport).
   (c) 1600 may be selected if: nine-track dual transport, or nine-track transport.

OPERATING CONDITIONS

The operation conditions that may be selected by the switches and the unit select operation are:

Switches:

1. High or Low Speed: 75 ips for ICL and 50 ips or 25 ips for LCTT.

2. 9T: nine or seven track tape

3. Dual, PE MODE SEL, nine-track and Density Status from the transport determine the operation density, 800, 556 or 1600 bpi.

4. PRØTECT: protected or unprotected transport

Unit Select

1. A/D: Character or Assembly/Disassembly format

2. BCD: Binary or BCD code

3. File Protect: a signal from the transport that determines if data can be recorded or not because of the protect ring.

CONTROL FUNCTION

The control function executes three operations in sequence:

1. Clear Controller, if A0 = 1
2. Clear interrupt, if A1 = 1. Select Interrupt if A2, A3 or A4 = 1
3. Motion function, if A7-A10 contains legal motion function.

CLEAR CONTROLLER

There are three levels of clear function in the controller:

1. MC: clears and presets all the flip-flop in the system. It is generated by manual master clear.
2. RES1: clears all flip-flops which contain operation conditions. It is generated by MC+STRUS+STRCF·A00. STRUS occurs at R4 and STRCF occurs at R2 if the reply conditions are met so the control function is executed.
3. RES2: clears the flip-flops that store status information and are not operation conditions. It is generated by RES1+STRMF.

   STRMF occurs at R4 if reply conditions are met and a motion function is executed.

INTERRUPT

There is one Interrupt line, (location 16 P2A16) and three kinds of Interrupts: Data, EØP, Alarm. There is an enable flip flop for each interrupt, which is set by CØF according to bits 2-4 of the A-Register. The Interrupts are cleared by MC+STRCF·[A (0)+A (1)]. CØF occurs at R4 and STRCF at R2 so that the clear occurs before the setting. If the appropriate interrupts are enabled then the following interrupts can occur:

1. Data Status
2. Rising of End of Operation (EØP).
3. Alarm = EØT+Parity Error+Lost Data+File Mark +falling of Ready during an operation, Storage Parity Error, Protect Fault, ID Abort, PE Lost Data, PE Warning.

MOTION FUNCTION

The motion functions are executed by a Motion Function register that stores the function, a decoder that reads the appropriate control signal to the transport, a counter that determines the gaps and a Motion Sequencer that controls all the previous parts.

MOTION REGISTER AND DECODER

STRMF strobes bits 7-10 of the A-Register into the Motion Register. It strobes all legal motion functions except Backspace, SFM Backward and Rewind at BØT. The functions that are decoded from the register are:

RWIND LØAD
RWIND UNLØAD
FØRWARD
REVERSE

The strobing occurs at R4 and sets also Controller Active for all motions except Rewind Unload. The Motion Register is reset by STØP, IDABØRT, LØCKØUT or RESl.

GAP COUNTER

The gap counter is clocked by the Gap Clock circuit. It determines, together with the Function Decoder, 9T and BØT, the pre and post record delays as described in Table 4-3.

TABLE 4-3. GAP COUNTER

Function	Total Pre Record Distance**				Total Post Record Distance***			
	9T		7T		9T		7T	
	BØT	BETWEEN RECORDS	BØT	BETWEEN RECORDS	BØT	BETWEEN RECORDS	BØT	BETWEEN RECORDS
Write Motion								
ICL	*6.19	0.39	*6.19	0.59	0.44	0.44	0.44	0.44
LCTT	*7.79	0.35	*7.79	0.55	0.42	0.42	0.57	0.57
Read Motion								
ICL	*1.79	0.19	*1.79	0.19	0.27	0.27	0.27	0.27
LCTT	*4.59	0.19	*4.59	0.19	0.26	0.26	0.26	0.26
Backspace								
ICL	NO EXC	0.19	NO EXC	0.19	NO EXC	0.29	NO EXC	0.29
LCTT	NO EXC	0.19	NO EXC	0.19	NO EXC	0.39	NO EXC	0.39
Write File Mark								
ICL	*6.19	6.19	*6.19	6.19	0.44	0.44	0.44	0.44
LCTT	*7.79	7.79	*7.79	7.79	0.42	9.44	0.57	0.57
Search FM Forward								
ICL	1.79	0.19	0.19	1.79	0.27	0.27	0.27	0.27
LCTT	4.59	0.19	4.59	1.79	0.27	0.27	0.27	0.27
Search FM Backward								
ICL	NO EXC	0.19	NO EXC	NO EXC	NO EXC	0.29	NO EXC	0.29
LCTT	NO EXC	0.19	NO EXC	NO EXC	NO EXC	0.29	NA	0.29

All figures indicated above are inches.

END OF OPERATION

End-of-Operation (EØP) is reset by RES2. EØP is set at the detection of a gap in a Read after Write at WMØT, or RMØT, WFM or Backspace. At Search FM, EØP is set at the detection of a gap if FM is detected. When moving reverse (Backspace or Search FM Backward) and detecting BOT then EØP is set. When REWIND LØAD is executing and Ready rises, EØP is set also by PEEØP.

* Subtract 2.8 inches to obtain distance from BØT Marker.
** Total Pre-Record Distance is measured from beginning of motion to data.
*** Total Post-Record Distance is measured from data to end of motion.

MOTION SEQUENCER

The Motion Sequencer goes through states S0-S32 according to the timing diagram (Figure 4-4). S0 is set by STRMF, S1 by the End Prerecord delay, S2 by EØP, S31 and S32 by Post Record. S1 is the Start signal and S32 the Stop signal. If STRMF rises at S2, a non-stop motion will occur.

WRITE CONTROL

The Write Control directs the data through the Write path. The Write is initiated by STRWMØT that sets DATA FF (in DSA: NEED), requesting a data word from the computer. The computer responds with a Write operation. STRWR strobes the word into Buffer 1. When Buffer 1 is full and Buffer 2 is empty, a Transfer signal transfers the word from BUF1 → BUF2, and Data FF is set. A new word is transferred to Buffer 1 in the same way, but a Transfer is not generated until Buffer 2 is empty. When the Motion Sequencer is in Start the WDS empties Buffer 2 (in case of Assembly/disassembly two WDS are needed to empty Buffer 2).

When Buffer 2 is empty and Buffer 1 is full a Transfer command transfers the word from BUF1 → BUF2 and sets Data FF. Two things happen independently:

1. WDS empties Buffer 2.

2. Write operation fills Buffer 1.

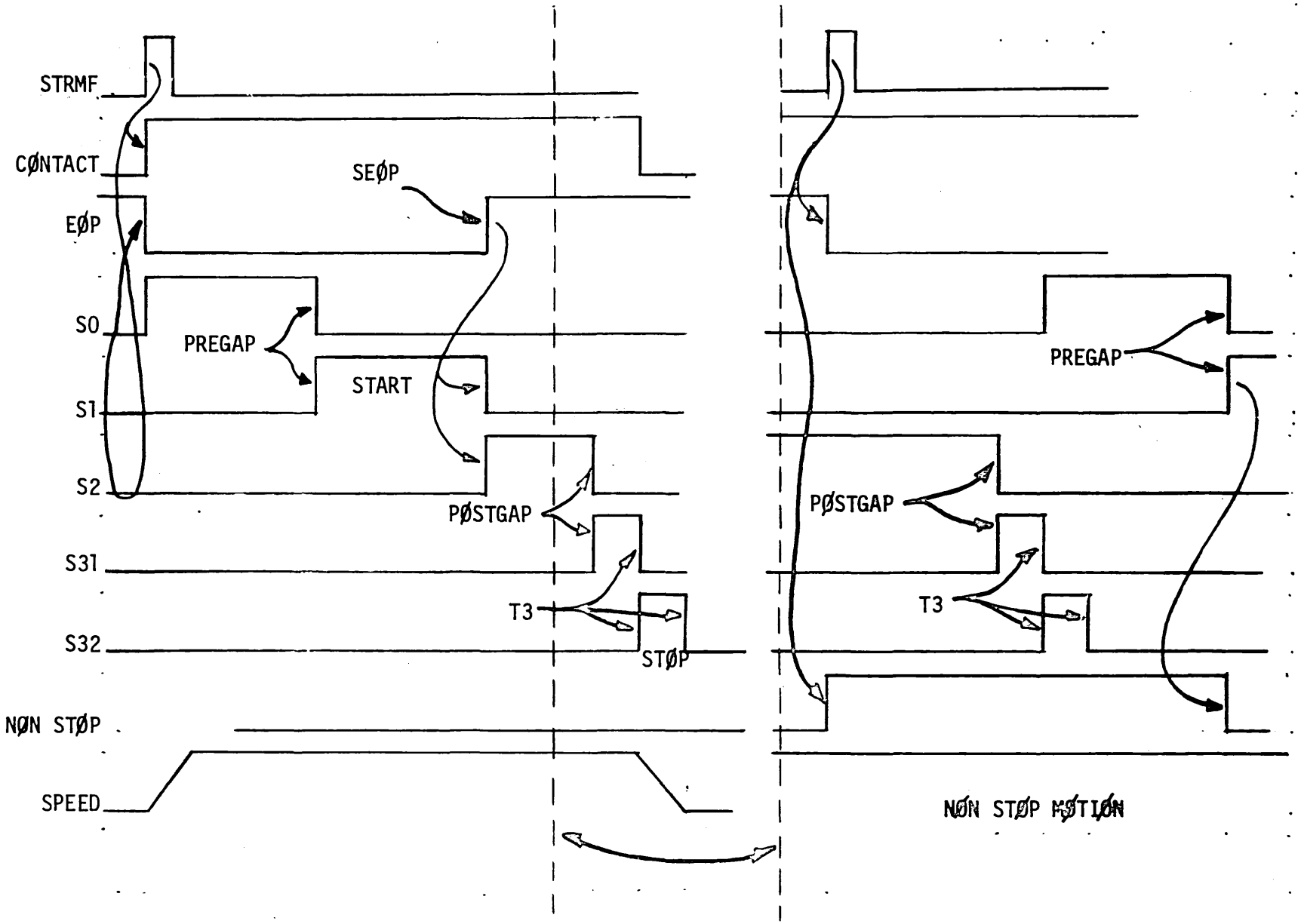


Figure 4-4. Motion Sequence

When the computer stops sending Write operations, both buffers become empty and an End of Record Sequence is set.

FIRST WØRD

The First Word flip flop is set by STRMF and is reset by the falling of the first Write Clock. It is used for two purposes:

1. If an Early WDS rises when Buffer 2 is not full, (i.e., no word was sent from the computer when requesting data) a Lockout condition occurs and the motion stops.
2. In WFM motion, EØRS is set by Early WDS if First Word is not set.

WRITE FM

In this motion the FM character is selected by the Write Tape selector. The FM character 17_8 is on 7-track and 23_8 on 9-track. A WDS to the tape strobes the FM character. In Write FM, only one character is written and then the End of Record Sequence (EØRS) starts.

END-OF-RECORD SEQUENCE

There are four kinds of EØRS:

Data, 9 track: data characters/3 spaces/CRCC/3 spaces/LRCC
FM, 9 track: FM character/7 spaces/LRCC
Data, 7 track: data characters/3 spaces/LRCC
FM, 7 track: FM character/3 spaces/LRCC

The EØRS is started if at Early WDS time, either BUF2 is empty at WMØT or First Word is reset at WFM. The Write EORS counter is enabled and then incremented by WDS Shifted. The presetting and decoding of that counter generates the EØRS.

READ CONTROL

If RMØT is in progress, the first RDS loads data into BUF 1, and as BUF 1 is full and BUF 2 empty, a TRANS signal moves contents of Buffer 1 into Buffer 2 and sets Data FF (or Need: DSA).

Two parallel processes continue:

1. The computer reads a word from BUF 2 in response to Data/Need.

2. The tape transport sends along with data characters the RDS signals. In A/D every second RDS, and in character format every RDS, fills BUFF1.

Every time BUF 1 is full and BUF 2 empty, BUF 1 information moves into BUF 2 and Data/Need is set. The data characters from the tape are checked for FM, LRCC, CRCC and Parity.

If an odd number of characters are read in A/D format and the End of Record is detected (the last character is still in BUF 1), one more transfer is initiated in order to read the last character, and Fill status is set.

The Read signal terminates when an End of Record is detected

SEARCH FM

During every motion (except Rewind) a File Mark is looked for. If two identical characters are detected (23_8 in nine-track and 17_8 in seven-track with a gap of at least 2.5 characters between them then FM Status is set.

END-OF-RECORD DETECTOR

The EØR Detector is a counter that counts double the character frequency. Every RDS resets the counter to zero. A missing character is detected if the counter reads 4 (2-21/2 character spaces from the previous). The first Missing Character indicates termination of data and the second Missing Character indicates termination of CRCC.

When the EØR detector overflows (16 missing characters after the LRCC), the EØP FF is set, to indicate End-of-Record.

If after 10 counts (5-5 1/2 character spaces) no CRCC is detected, a special Missing CRCC signal toggles the CRCC register once more.

CHARACTER REDUNDANCY CHECK CHARACTER (CRCC)

The CRCC is a cyclic redundancy check character that is generated by manipulating all the characters sent to the tape. This CRCC is generated in the controller and sent to the tape after the data.

During reading, all the characters including the CRCC are manipulated in the CRCC generator, and a final pattern of 111010111 in that register indicates that no CRC error occurred.

LONGITUDINAL REDUNDANCY CHARACTER CHECK (LRCC)

The LRCC is a longitudinal parity check and is generated by the transport and written after the CRCC. When Reading, all the characters including the CRCC and LRCC are checked for even parity in every track.

STATUS

The status of the controller is indicated by various FF's throughout the system. The status information can be transferred to the computer by the two Read Status instructions. Most of the status FF's have been described. The remaining are described herein.

READY STATUS

A signal from the transport that indicates that it is selected and connected. Falling of READY during an operation causes Alarm.

BUSY STATUS

This signal indicates that the tape is in motion.

LOST DATA STATUS

Lost Data is set if one of the following conditions occur:

1. Both buffers are full and the next RDS is detected in RMØT, if Last Word is not set in BUF I/Ø.

2. During BUF I/O transfer. Lost Data is set if both buffers are empty and WDS is generated in WMØT.

Lost Data is cleared by RES2.

PROTECT STATUS

Indicates that the selected transport is protected.

PARITY ERROR STATUS

Parity Error occurs in one of the following cases:

1. A vertical Parity Error was detected in a Data character.

2. LRC error detected at EØP.

3. CRC error detected at EØP in nine-track.

BEGINNING OF TAPE/END OF TAPE (BØT/EØT)

BØT is set from the detection of the Beginning-Øf-Tape Marker on the tape until the first START signal rises.

EØT is set from the detection of End-Øf-Tape Marker on the tape until RS2.

FILL

Indicates that an odd number of characters were read from the tape in Assembly/Disassembly mode.

SECTION 5
LOGIC DIAGRAMS

KEY TO LOGIC SYMBOLS

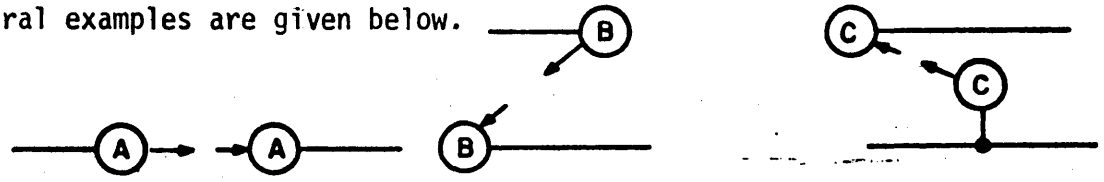
Publication 89723700 (Key to Logic Symbols) or equivalent, lists the symbols used in the logic diagrams in this manual and gives a short description of the function they represent. The symbols conform generally to Control Data usage (Microcircuit Handbook, publication number 15006100), using the polarity logic convention. The following paragraphs describe signal flow conventions, including on-sheet and off-sheet continuation reference symbols, test points, connecting lines, non-connecting lines and connector pin designations.

SIGNAL FLOW

Input signals are drawn coming from the left or above; output signals are drawn going to the right or down. Signal lines are sometime interrupted to allow logical grouping of components. The interruption may be within one drawing sheet or between two or more sheets and requires continuation references.

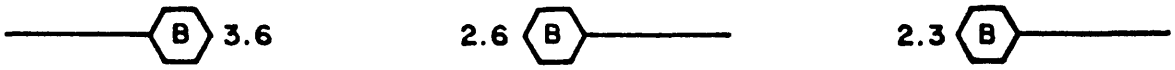
On-Sheet Continuation Reference Symbols

To indicate that a connection exists between two points on a sheet, arrows attached to encircled arbitrary reference letters point from the signal origin to the signal destination. The letters C, H, I, O and P are not generally used as reference letters, since they have special significance in logic diagrams. Several examples are given below.



Off-Sheet Continuation Reference Symbols

These symbols indicate that a common signal point exists between two or more sheets of the same logic drawing. In the illustration that follows, it is assumed that a certain signal originates on sheet 2 and flows into sheets 3 and 6. The numbers next to each hexagon indicate a sheet number where the signal appears. For example, 3.6 means sheets 3 and 6; 2.6 means sheets 2 and 6, and so on.



OUTPUT ON SH2 | INPUT ON SH3 | INPUT ON SH6

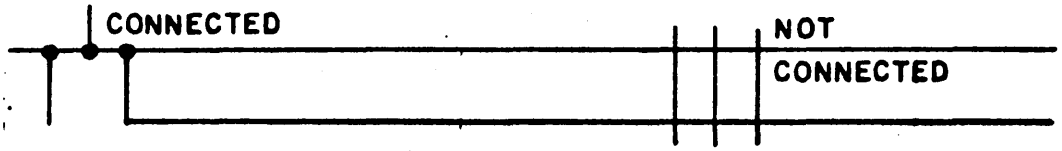
It should be noted that the referenced sheet numbers are always placed opposite the line extending from the hexagon. The line extends left of the hexagon for outputs and right of the hexagon for inputs. As in the case of on-sheet continuation reference symbols, the letters C,H,I,O and P are not generally used as reference letters. Combinations such as AA are used after Z.

TEST POINTS

The test point symbol shows the connection of a test point on the printed wiring board (PWB). The number adjacent to the symbol refers to the test point position on the PWB at the edge opposite the connectors. Only test point 1 and test point 63 are marked on the PWB. Below are two typical test points.

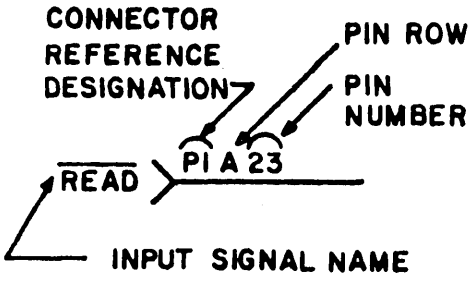
CONNECTING LINES AND NON-CONNECTING LINES

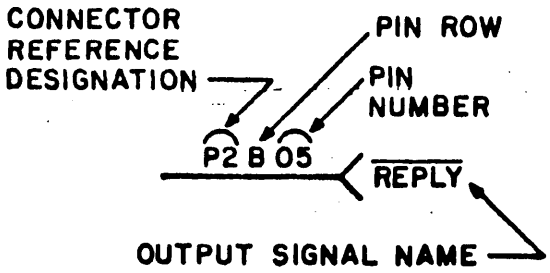
Lines connected to a common point or at a junction point are shown below at the left. No more than three lines are connected to a common point in the diagrams. Lines which cross but are not connected are shown below at the right.



CONNECTORS

For both input and output signals, the symbol for a female connector is used. The full name of the signal, or the abbreviation commonly applicable to logic diagrams, is placed at the open end of the connector symbol. The connector reference designation, pin row and pin number are given above the line which extends from the symbol.





Q-CHANNEL PWB LOGIC (Logic Diagram 89768300)

CLOCK AND REPLY/REJECT LOGIC (Logic Diagram 89768300, Sheet 2) Figures 5-3,5-4.

Clock

Transistors Q1 and Q2, the crystal, and U36-6 comprise an oscillator operating at 15.36 MHz (ICL) or 10.24 MHz (LCTT). With STPCLK and EXTCLK high, the square wave from U36-6 passes through U35-10,U35-8 and -4, to U35-6 and is filtered by two transistors (Q1 and Q2) and the resistors and capacitors (R1 through R7 and C1 through C4). U35-6 can be active with either the internal or the external clock (EXTCLK) operating.

The two FF's in U33 divide the signal from U35-6 by four. The output from U33-6 is 3.84 MHz for ICL operation and 2.675 for LCTT operation. This signal is then divided by four again by the FF's of U50. U49 produces T1 through T4 time states from this signal. Figure 5-1 shows the time sequence generated by the Clock.

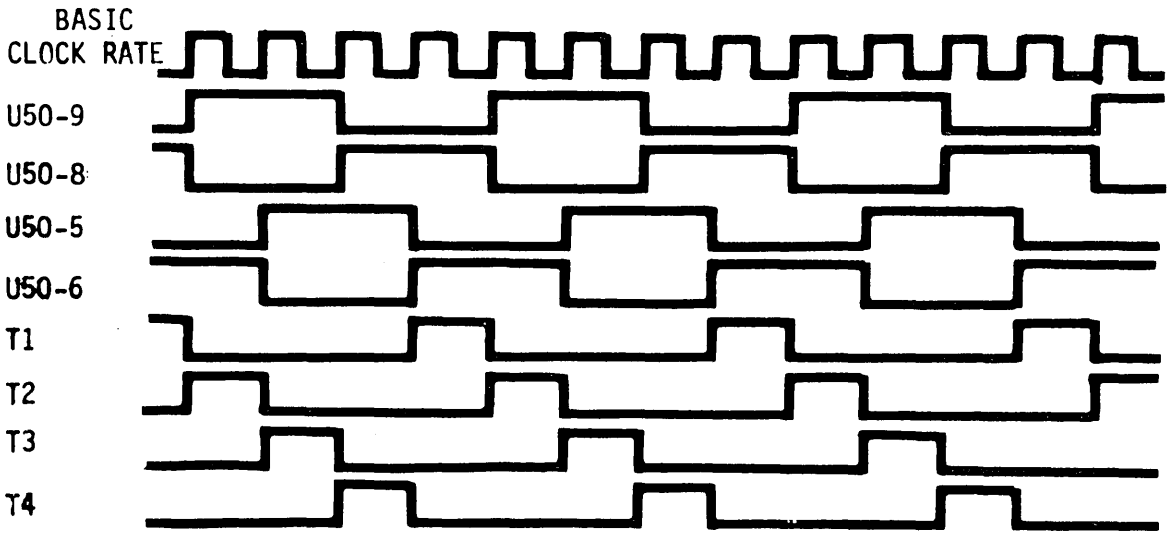


Figure 5-1. Clock Time Sequence

Reply/Reject Logic

This module generates the timing sequence for all the A/Q interaction with the computer.

The Reply/Reject Timing is initiated by A/Q READ or A/Q WRITE and BASIC CLOCK.

$$U24\text{-}6 = \overline{\text{A/Q READ}}\cdot\overline{\text{SELECTED}} + \overline{\text{A/Q WRITE}}\cdot\overline{\text{SELECTED}}$$

(SELECTED = QØK)

Ena enables the A bus to the CPU. This signal is set by the falling edge of $\overline{\text{A/Q READ}}\cdot\overline{\text{SELECTED}}$ and is reset together with the rising of $\overline{\text{A/Q REPLY}}$ or $\overline{\text{A/Q REJECT}}$. This signal starts with READ, and terminates after falling of $\overline{\text{READ}}$, together with REPLY or REJECT.

The R + W signal enables Operation Decoder U40 (Sheet 4)

$$R+W = ENA+A/Q\ WRITE\cdot SELECTED$$

Operation of R0-R4 Shift registers (U8 and U7): (Sheet 2)

If $\overline{\text{MC}}$ = Logic 1, the FF R0 is set when U24-6 rises. R1 FF (U7) is set at the next rise of the BASIC CLOCK pulse. The setting of R1 FF clears R0 FF, and at the next rise of the BASIC CLOCK pulse, R1 FF is reset and R2 FF is set. At the next clock, R2 is reset and R3 is set. Then R4 FF is set, R3 is reset and with the rising of next BASIC CLOCK pulse, R4 is reset and R5 is set.

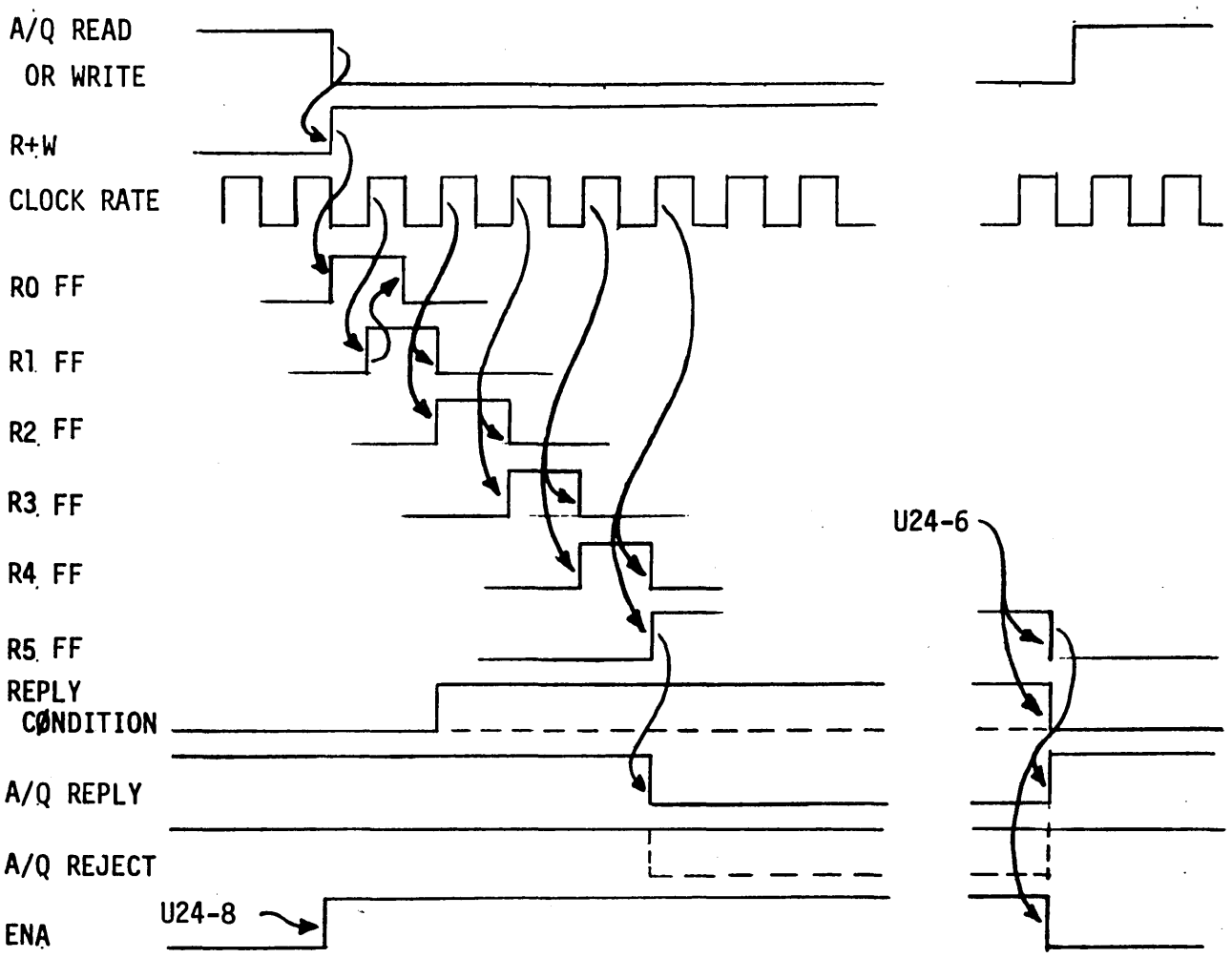
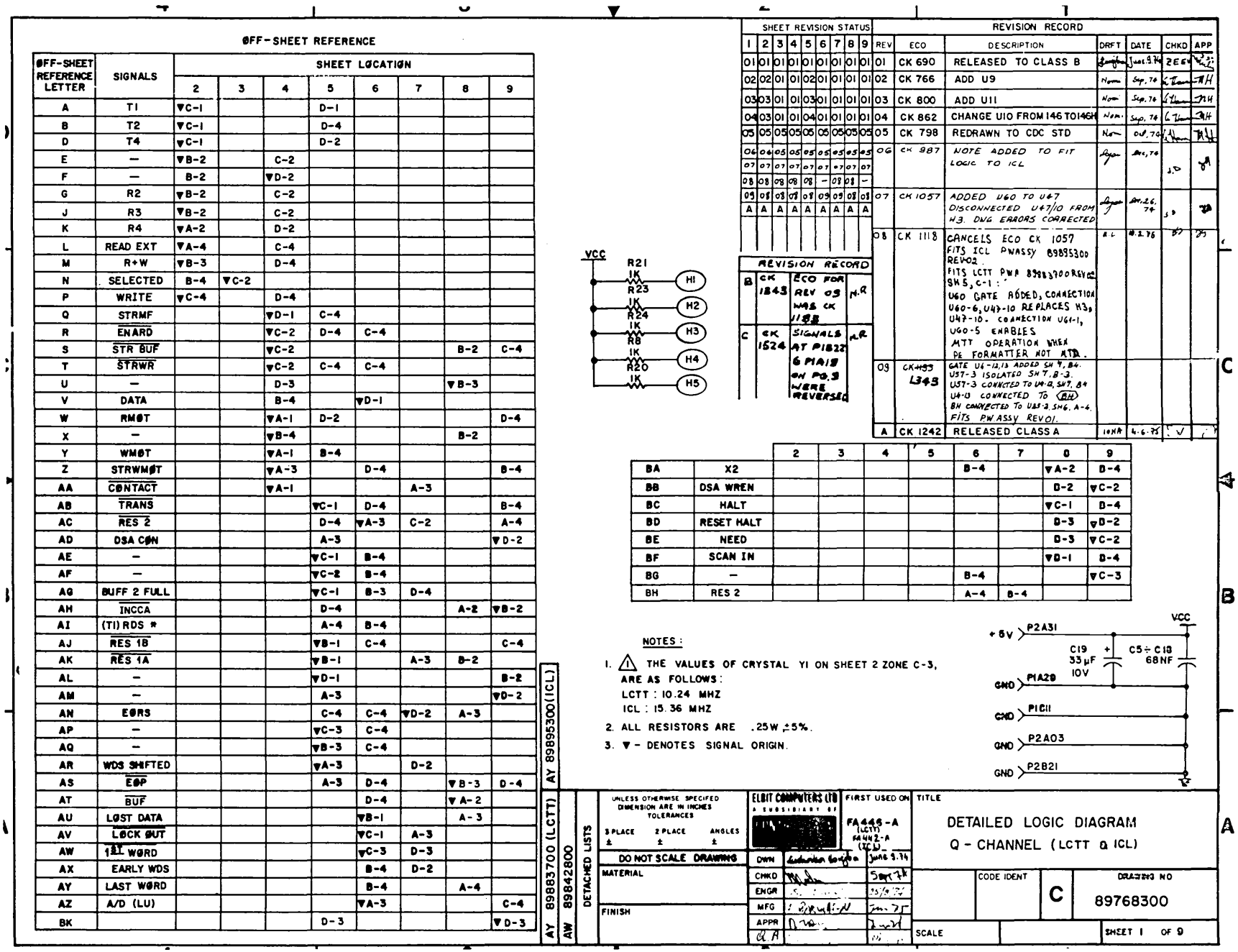


Figure 5-2. Reply/Reject Sequence

R2, R3, R4 are used for output-from-computer timing and ENA is used for the input. U24-6 resets R1 - R5 and RC, R5 resets A/Q Reply, A/Q Reject, and ENA. ENA is generated because the input data must stay valid until the rise of the $\overline{\text{A/Q Reply}}$ signal.



OFF-SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION 2	3	4	5	6	7	8	9
A	T1	▼C-1			D-1				
B	T2	▼C-1			D-4				
D	T4	▼C-1			D-2				
E	—	▼B-2		C-2					
F	—	B-2		▼D-2					
G	R2	▼B-2		C-2					
J	R3	▼B-2		C-2					
K	R4	▼A-2		D-2					
L	READ EXT	▼A-4		C-4					
M	R+W	▼B-3		D-4					
N	SELECTED	B-4	▼C-2						
P	WRITE	▼C-4		D-4					
Q	STRMF			▼D-1	C-4				
R	$\overline{\text{ENARD}}$			▼C-2	D-4	C-4			
S	$\overline{\text{STR BUF}}$			▼C-2				B-2	C-4
T	$\overline{\text{STRWR}}$			▼C-2	C-4	C-4			
U	—			D-3				▼B-3	
V	DATA			B-4		▼D-1			
W	RMØT			▼A-1	D-2				D-4
X	—			▼B-4				B-2	
Y	WMØT			▼A-1	B-4				
Z	STRWMØT			▼A-3		D-4			B-4
AA	$\overline{\text{CONTACT}}$			▼A-1			A-3		
AB	$\overline{\text{TRANS}}$				▼C-1	D-4			B-4
AC	$\overline{\text{RES 2}}$				D-4	▼A-3	C-2		A-4
AD	DSA CØN				A-3				▼D-2
AE	—				▼C-1	B-4			
AF	—				▼C-2	B-4			
AG	BUFF 2 FULL				▼C-1	B-3	D-4		
AH	$\overline{\text{INCCA}}$				D-4			A-2	▼B-2
AI	(TI) RDS *				A-4	B-4			
AJ	$\overline{\text{RES 1B}}$				▼B-1	C-4			C-4
AK	$\overline{\text{RES 1A}}$				▼B-1		A-3	B-2	
AL	—				▼D-1				B-2
AM	—				A-3				▼D-2
AN	EØRS				C-4	C-4	▼D-2	A-3	
AP	—				▼C-3	C-4			
AQ	—				▼B-3	C-4			
AR	WDS SHIFTED				▼A-3		D-2		
AS	$\overline{\text{EØP}}$				A-3	D-4		▼B-3	D-4
AT	$\overline{\text{BUF}}$					D-4		▼A-2	
AU	LØST DATA					▼B-1		A-3	
AV	$\overline{\text{LØCK ØUT}}$					▼C-1	A-3		
AW	$\overline{\text{1ST}}$ WØRD					▼C-3	D-3		
AX	EARLY WDS					B-4	D-2		
AY	LAST WØRD					B-4		A-4	
AZ	A/D (LU)					▼A-3			C-4
BK					D-3				▼D-3

		2	3	4	5	6	7	8	9
BA	X2					B-4		▼A-2	B-4
BB	DSA WREN							D-2	▼C-2
BC	HALT							▼C-1	B-4
BD	RESET HALT							B-3	▼D-2
BE	NEED							B-3	▼C-2
BF	SCAN IN							▼D-1	B-4
BG	—					B-4			▼C-3
BH	RES 2					A-4	B-4		

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	CK 690	RELEASED TO CLASS B		June 9.74	ZEG	
02	CK 766	ADD U9	Norm	Sep. 74		TH
03	CK 800	ADD U11	Norm	Sep. 74		TH
04	CK 862	CHANGE U10 FROM 146 TO 146H	Norm	Sep. 74		TH
05	CK 798	REDRAWN TO CDC STD	Norm	Oct. 74		TH
06	CK 987	NOTE ADDED TO FIT LOGIC TO ICL	Ayan	Dec. 74	JD	
07	CK 1057	ADDED U60 TO U47 DISCONNECTED U47/10 FROM H3. DWG ERRORS CORRECTED	Ayan	Dec. 26. 74	JD	
08	CK 1118	CANCELS ECO CK 1057 FITS ICL PWASSY 89895300 REV02. FITS LCTT PWA 89883700 REV02 SH 5, C-1 : U60 GATE ADDED, CONNECTION U60-6, U47-10 REPLACES H3, U47-10. CONNECTION U61-1, U60-5 ENABLES MTT OPERATION WHEN PE FORMATTER NOT ATD.	A.L	10.2.75		
09	CK-1133 L343	GATE U4-12,13 ADDED SH 9, B4. U57-3 ISOLATED SH 7, B-3. U57-3 CONNECTED TO U4-12, SH7, B4 U4-13 CONNECTED TO (RH) BH CONNECTED TO U53-3, SH6, A-4. FITS PWASSY REV01.				
A	CK 1242	RELEASED CLASS A	IONA	4.6.75	V	

REVISION RECORD			
B	CK 1843	ECO FOR REV 09 WAS CK 1188	N.R
C	CK 1524	SIGNALS AT P1B22 & P1A19 ON PG.3 WERE REVERSED	N.R

SHEET REVISION STATUS 1	2	3	4	5	6	7	8	9	REV
01	01	01	01	01	01	01	01	01	01
02	02	01	01	02	01	01	01	01	02
03	03	01	01	03	01	01	01	01	03
04	03	01	01	04	01	01	01	01	04
05	05	05	05	05	05	05	05	05	05
06	06	05	05	05	05	05	05	05	06
07	07	07	07	07	07	07	07	07	
08	08	08	08	08	–	08	08	–	
09	08	08	08	08	09	09	08	08	07
A	A	A	A	A	A	A	A	A	

Figure 5-3. Q-Channel Logic Diagram Reference Sheet

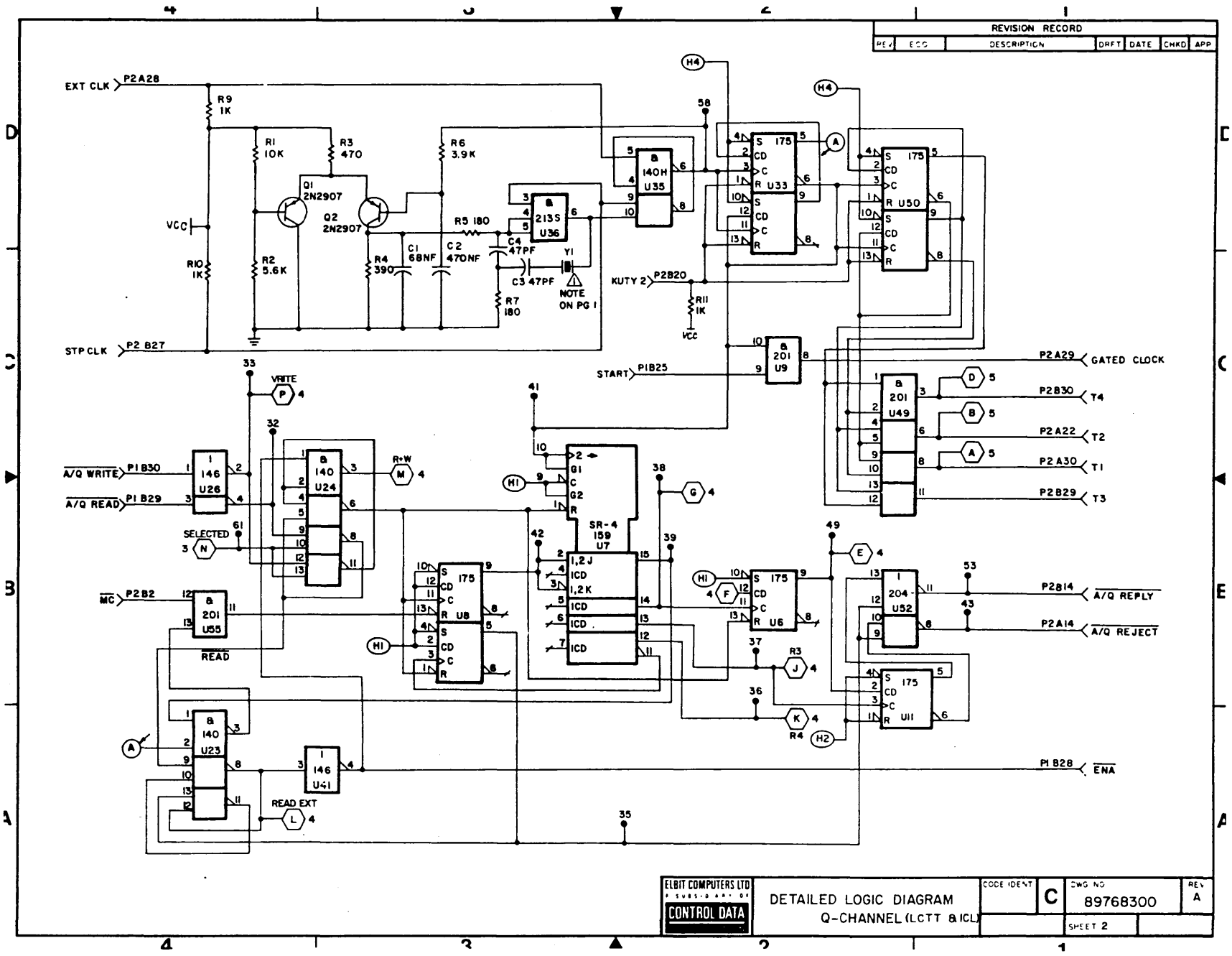


Figure 5-4. Q-Channel - Clock and Reply/Reject Logic Diagram

OPERATION DECODER (Logic Diagram 89768300, Sheets 3 and 4) Figures 5-5 and 5-6.

The Operation Decoder (U40 on Sheet 4) generates the waveforms for the control of the interface with the computer. The inputs are from the computer's Q-register, timing signals from the Reply/Reject Logic, and certain status signals from the controller. The outputs are the STROBE and SELECT signals, and the Reply condition.

QØK (U3-6 , Sheet 3) is high when Q07-Q10 match the setting of the Equipment Number and Q11-Q15 equal to zero.

U40 generates eight active low signals. Each signal is a result of decoding of one of the computer instructions. The signals are decoded from A/Q Q0, A/Q Q1, A/Q WRITE and ENA. For Write instructions the timing is according to A/Q WRITE, for READ according to ENA. The signals are enabled by R+W.

$$U38\text{-}8 = RD \cdot DATA \cdot RM\emptyset T + WR \cdot DATA \cdot WM\emptyset T + CF \cdot LEGCF + BUF \cdot (E\emptyset P + BUSY)$$

$$U37\text{-}8 = U38\text{-}8 \cdot READY + US \cdot LEGUS + CF \cdot \overline{A_8} \cdot \overline{A_9} \cdot \overline{A_{10}}$$

$$REPLY = DS1 + DS2 + CA + U37\text{-}8\ (\overline{PROTECTED} + A/Q\ PROTECTED)$$

RD = READ

Signals that execute the computer instructions are listed in Table 5-1.

TABLE 5-1. COMPUTER INSTRUCTION EXECUTION

Output	Function	Description
U22-6	$\overline{\text{STRBUF}} = \overline{\text{R3}\cdot\text{RC}\cdot\text{BUF}}$	Starts Buffered I/O instructions
U22-12	$\overline{\text{ENARD}} = \overline{\text{ENA}\cdot\text{RC}\cdot\text{RD}}$	Strobes input data during Read instruction.
U22-8	$\overline{\text{STRWR}} = \overline{\text{R3}\cdot\text{RC}\cdot\text{WR}}$	Strobes output data during Write instruction
U53-3	SELA0 = RD+DS1	Controls input-to-A multiplexer
U53-6	SELA1 = RD+DS2	Control input-to-A multiplexer
U21-12	STRINT = R4·RC·CF	Sets interrupt enable register
U21-6	STRUS = R4·RC·US	Selects unit
U21-8	STRCF = R2·RC·CF	Starts control function
U55-6	STRMF = R4·RC·CF·LEGMF	Starts motion function
U36-12	STRWMØT = $\text{R4}\cdot\text{RC}\cdot\text{CF}\cdot A_7\cdot A_8\cdot A_9\cdot A_{10}$	Starts write motion
U55-8	USA = $\text{US}\cdot\overline{\text{CONTACT}}$	Controls unit select multiplexer in Upper Data PW board

RC = REPLY CØNDITIØN

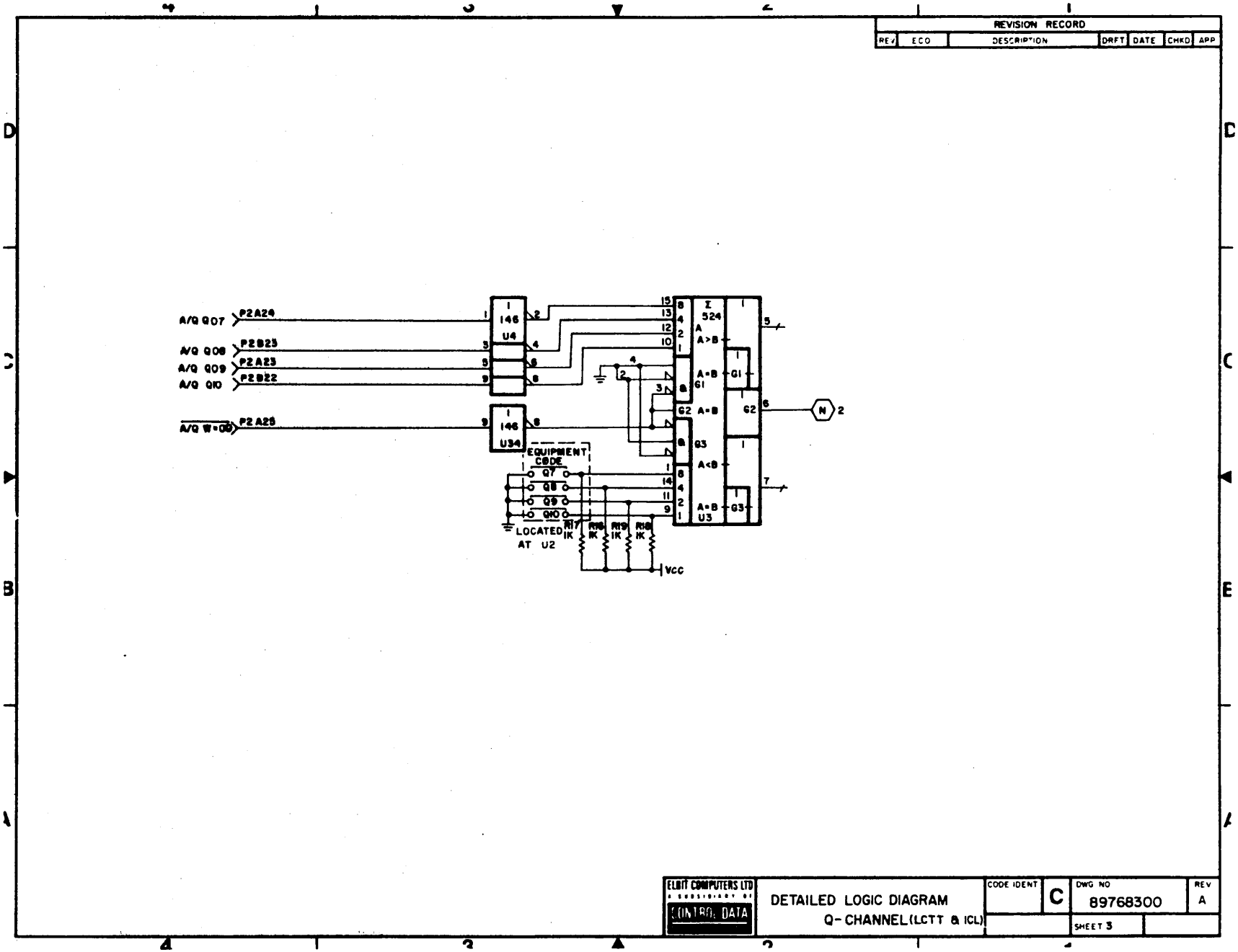


Figure 5-5. Q-Channel - Operation Decoder Logic Diagram

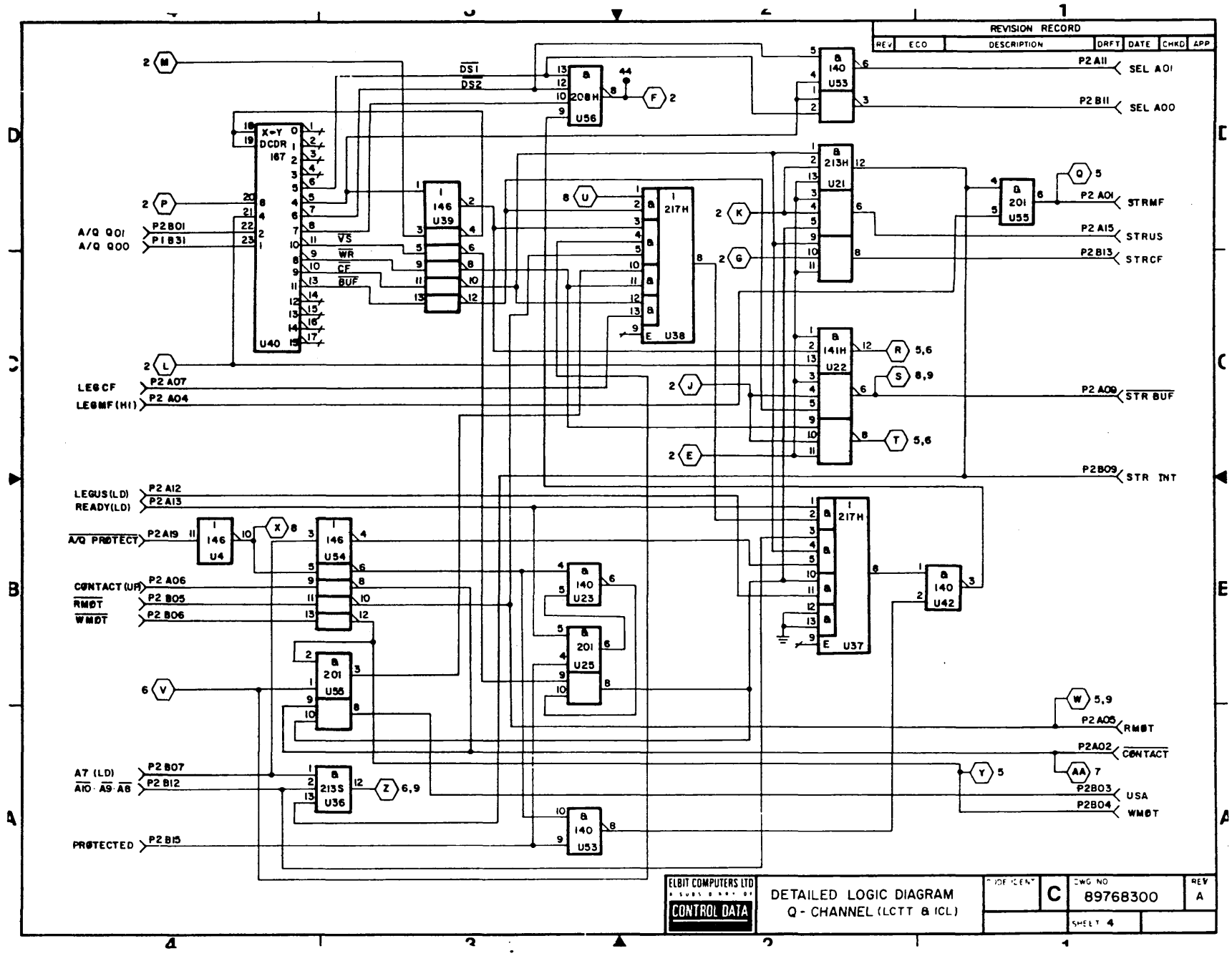


Figure 5-6. Q-Channel - Operation Decoder Logic Diagram (Cont'd)

DOUBLE BUFFER & DATA CONTROL (Logic Diagram 89768300, Sheet 5) Figure 5-8.

Double Buffer Control

The Double Buffer is described in a later section. The Double Buffer diagram is shown in Figure 5-7 (See Lower-, Upper Double Buffer).

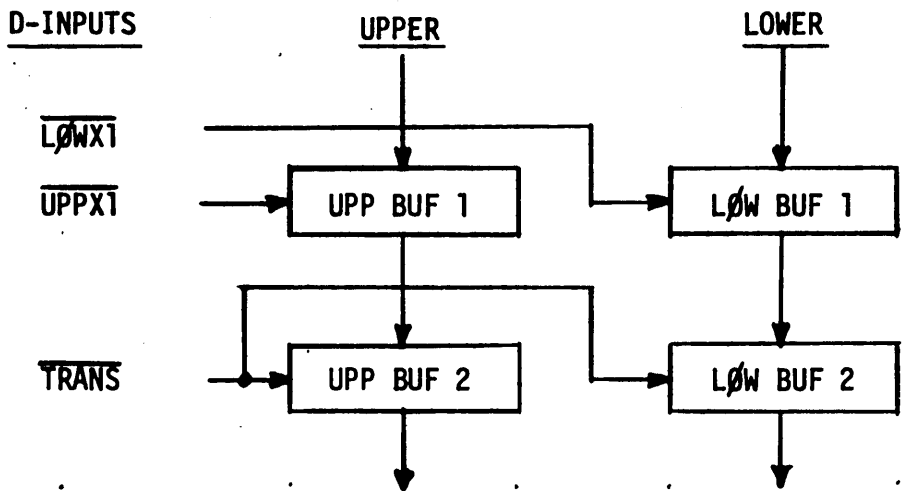


Figure 5-7. Double Buffer Control

The Double Buffer Control controls the transfer of data from the computer's A-register or DSA-Data to the tape interface lines while writing, or from the tape interface lines to the computer while reading. This module also controls the assembly/disassembly of the data.

The Double Buffer Control includes the following DD's:

1. BUF 1 FULL: When high it indicates that BUF 1 contains valid data. (U63-9)(TP23)
2. BUF 2 FULL: When high it indicates that the data on the output lines (U63-5)(TP9) of the Double Buffer are valid.

3. UPPER (U30-9): When high the Upper Half Buffer is accessed.

4. TRANS (U42-11)(TP28): Provides the timing for transfer from Buffer 1 to Buffer 2.

5. CLRLOWER (U47-9)(TP25): Initiates a dummy transfer of zeros in the Lower Half Buffer when an odd number of characters are read (in character format).

The data from/to the A-register is strobed by the rise of $\overline{\text{STRWR}}$ while writing and by the rise of $\overline{\text{ENARD}}$ while reading. The DSA-Data lines are strobed by the rise of $\overline{\text{INCCA}}$ (Increase Current Address). The data to the tape is strobed by WDS (Write Data Strobe), and the data from the tape is strobed by the fall of RDS (Read Data Strobe).

The Character Input signal to CPU has the following equation:

$$\overline{\text{A/Q CHAR INPUT}} = \overline{\text{A/D}} \cdot \text{ENARD} \quad \text{(U59-6)}$$

Write Motion: UPPER FF is set by STRMF, when A/D is low, UPPER stays reset (U30-13) and when A/D is high, UPPER toggles after each WDS (in NRZI by $\overline{\text{WDS SHIFTED}}$ and in PE by $\overline{\text{PWRQ SHIFTED}}$). U64-6 and 8 produce STRWR·WMØT, and the rise of this signal sets BUF 1 FULL and strobes the A-register into BUF 1.

If BUF 2 Full is low and BUF 1 Full is high then U48-4 and 5 are high, U48-6 is low and U45-10 is high. TRANS is set by the rise of T4 and reset by the rise of T2. The fall of TRANS strobes BUF 1 into BUF 2 (at the rise of T2) and sets new data request. As WDS rises (strobes into the tape) at the rise of T3 and Buff 2 is strobed at the rise of T2, the data on the interface lines to the tape are valid at least 500 nsec before and after the strobing.

BUF 2 FULL is set by the fall of TRANS and is set by the rise of WDS if UPPER is low (U48-1, 13 and 8).

Read Motion (Sheet 4): UPPER is set by STRMF when A/D is low. UPPER stays reset (U30-13) and when A/D is high, it toggles with the falling of RDS (U44-9 and 8, U29-3 and 6, U45-1 and 2, and U30-11).

If UPPER is high, the fall of RDS strobes the data from the tape into UPPBUF 1
If UPPER is low, the fall of RDS strobes the data from MTT into LOWBUF 1
sets BUF 1 FULL.

If BUF 2 is low and BUF 1 FULL is high a $\overline{\text{TRANS}}$ pulse is generated as in WRITE MOTION.

BUF 2 FULL is reset by the rise of $\overline{\text{ENARD}}$, i.e., the strobing of A-register (U62-9 and 8, U48-9, 10 and 8, and U63-3) and is set by the fall of $\overline{\text{TRANS}}$.

If ISTSP rises and $\overline{\text{UPPER}}$·A/D·RMØT is high (U46-12, 13 and 11; U58-1, 2 and 3) then CLRLOWER is set. If BUF 2 FULL is low and $\overline{\text{CLRLOWER}}$ is high a $\overline{\text{TRANS}}$ pulse is generated and a last data request is set.

The Double Buffer Control also indicates the following conditions:

1. U46-6 - BUF 1 FULL·RMØT sets LOST DATA on next RDS

2. U46-3 - $\overline{\text{BUF 2 FULL}}$·WMØT condition for Lockout, Priority, Lost Data and EØR Sequence

3. U61-6 - Priority Condition = $\overline{\text{BUF 1 FULL·BUF 2 FULL·WMØT}}$ + $\overline{\text{BUF 1 FULL·BUF 2 FULL·RMØT}}$

$\overline{\text{REST}}$ clears the FF's BUF 1 FULL, BUF 2 FULL, CLRLOWER.

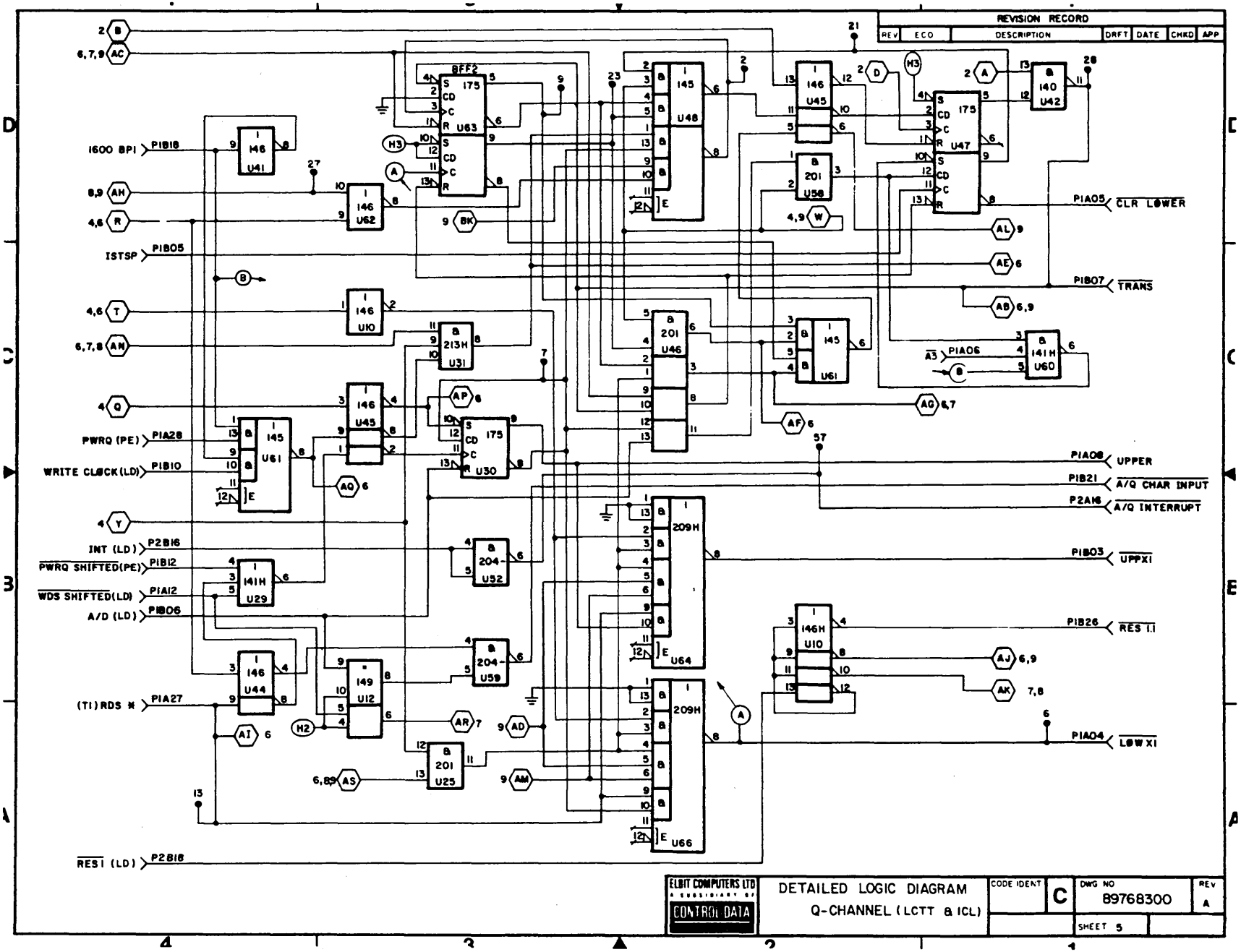


Figure 5-8. Q-Channel - Double Buffer and Data Control Logic Diagram

DATA CIRCUIT (Logic Diagram 89768300, Sheet 6) Figure 5-10.

This module includes three FF's: 1.) DATA (U32-9) - request for input or output via the A/Q, 2.) LOST DATA (U32-5) - indication of lost data condition, and 3.) 1ST WORD (U30-5) - high until the first word has been sent to the transport. This module includes also a part of WDS generation.

DATA (U32-9) is set only if BUF I/O is low, by either rising of $\overline{\text{TRANS}}$ (U42-11 Sheet 4) or by STRWMØT (U28-10 and 8; U32-10). $\overline{\text{TRANS}}$ transfers the data in the Double Buffer from BUF 1 to BUF 2, so when writing BUF 1 can receive a new computer word, DATA is set. When reading, BUF 2 includes valid data that can be sent to the computer if DATA is set. When writing, DATA is first set by STRWMØT in order to transfer the first word. When reading, DATA is first set by the first $\overline{\text{TRANS}}$.

DATA is reset by:

$$\text{U31-12} = \text{ENARD}+\text{STRWR}+\text{EØRS}+\text{LOST DATA}+\text{FM}+\text{RES1}+\text{EOP}$$

In the normal Data Transfer cycle during writing, STRWR (the signal that transfers the data into BUF 1) resets DATA. During reading ENARD resets it. When writing EØRS indicates that the stream of data words is terminated so no more data can be requested from the computer, and DATA is reset. If LOST DATA is indicated, DATA TRANSFER will terminate. In Read Motion, if a File Mark is detected it will not be transferred to the computer as data, and FM (detection) resets DATA.

When U62-6 (Sheet 5) is high (BUF I/Ø or LASTWORD) and RDS occurs, and BUF 1 FULL is high, then data is lost (data is transferred from the tape when both Buffers are full) and LOST DATA is set (U32-2). LOST DATA is also set by BUF I/Ø·WMØT·BUF 2 FULL·WDS (U29-12). This indicates that a character is to be transferred to the tape although BUF 2 is empty. Note that this condition is a legal termination of Write Motion in A/Q transfer.

WDS is generated according to the following equation:

U29-1: $WDS = WM\emptyset T \cdot \overline{E\emptyset RS} \cdot (\overline{1600BPI} \cdot WRITE\ CLOCK + 1600BPI \cdot PWRQ)$
(sheet 4)

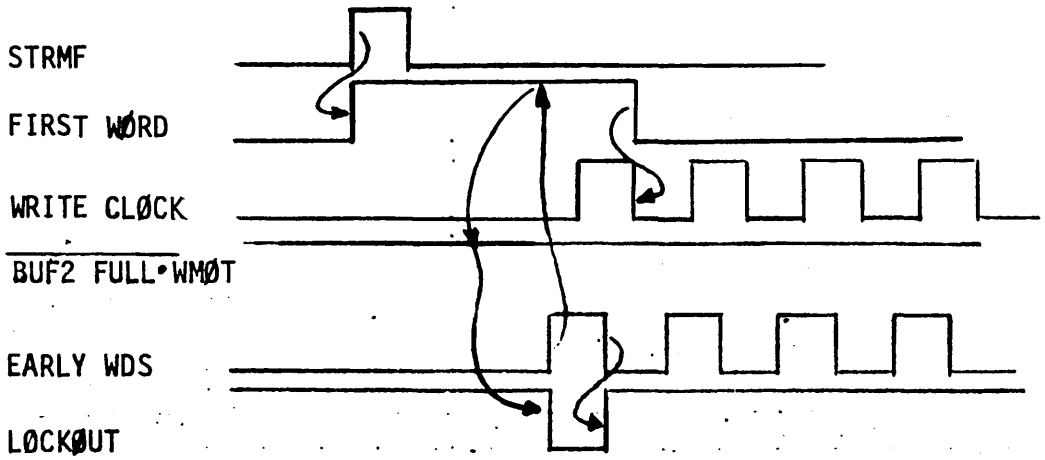


Figure 5-9. Lockout

For details on WRITE CLOCK PWRQ and EARLY WDS refer to Basic Timing Generation. STRMF sets 1ST WORD at U45-3 and 4 (sheet 4), and U30-4. The fall of the first WRITE CLOCK resets 1ST WORD. If BUF 2 is not full when the first EARLY WDS occurs a $\overline{LOCKOUT}$ (U29-8) pulse is generated. If BUF 2 is already full (when writing) no $\overline{LOCKOUT}$ occurs (see Figure 5-9).

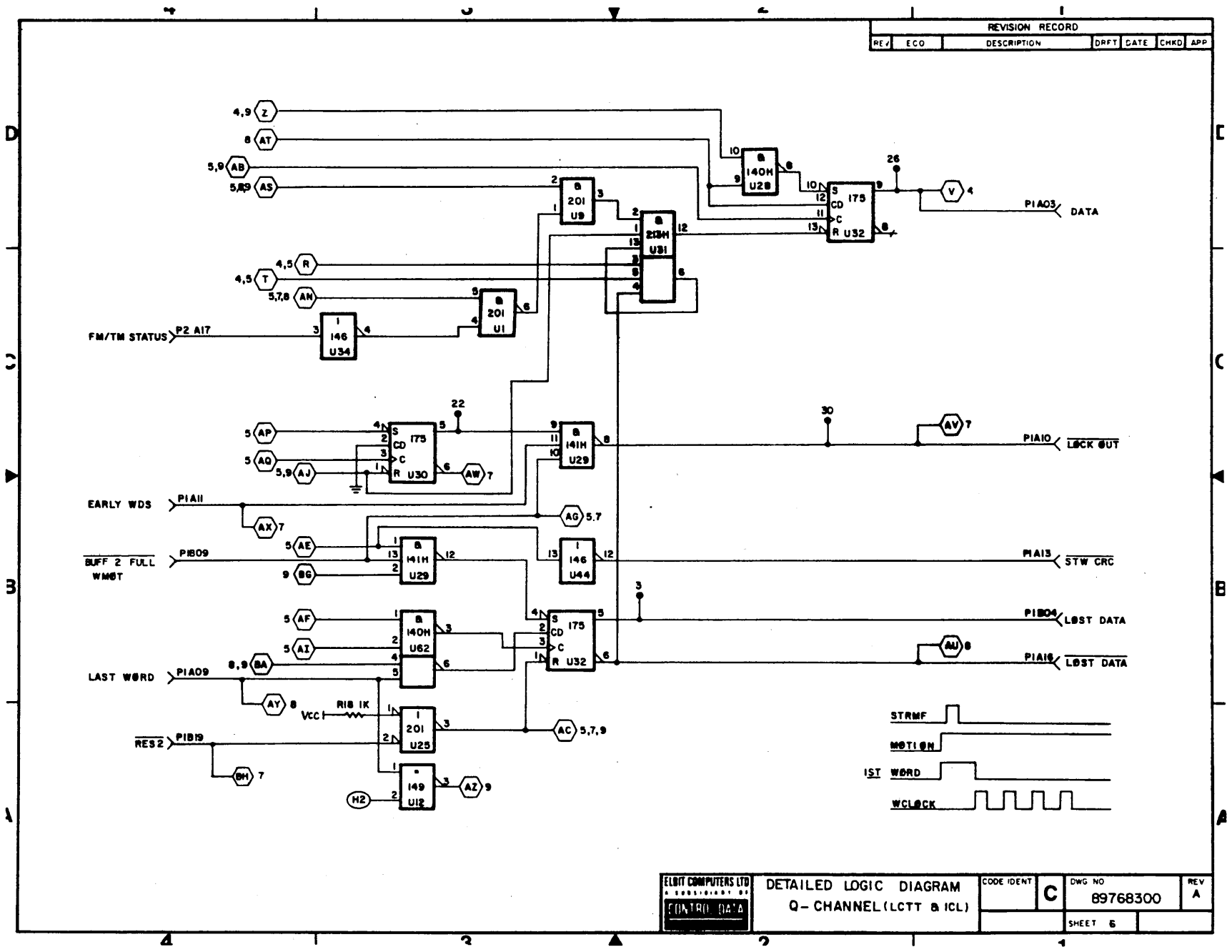


Figure 5-10. Q-Channel - Data Circuit Logic Diagram

END-OF-RECORD GENERATOR CONTROL AND STOP DISTANCE (Logic Diagram 89768300, Sheet 7) Figure 5-14.

End of Record Generator Control

There are four End-of-Record Sequences (EØRS): either Data or FM, with either 9T or 7T, as shown in Figure 5-11.

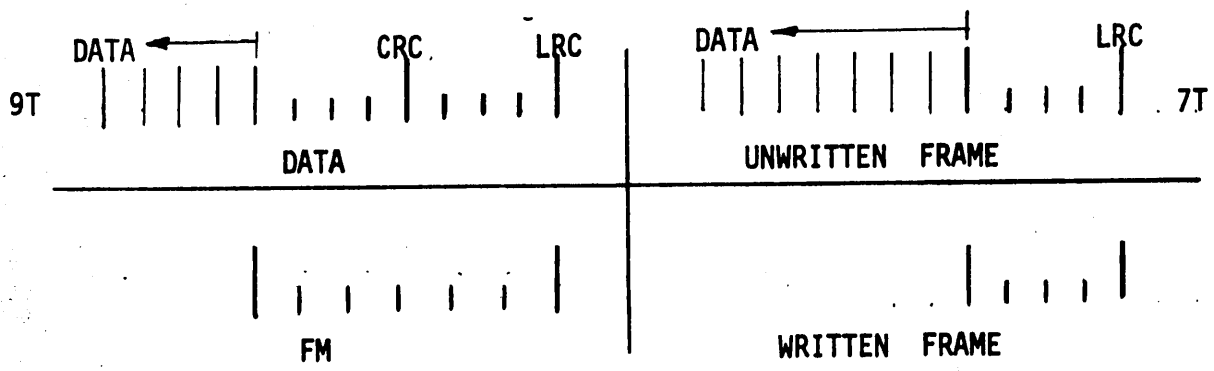


Figure 5-11. EØR Sequences

The first character of the FM is regarded as Data and the second as LRCC. EØRS is set only during Write Motion after the last Data Character is written on tape. This module can be divided into two parts: EØRS FF, and CRCC/LRCC Control Generator.

U11-9 EØRS is set by EARLY WDS if U11-12 = $\overline{\text{BUF 2 FULL}}$·WMOT + $\overline{\text{1ST WORD}}$·WFM

The W·CRC-LRC Strobe counter is preset while EØRS is low. It is preset either at 1011 for seven track, or at 0111 for nine track. When EØRS is high, WDS-SHIFTED counts U27 up until the counters overflow. U27-12 locks the counter at U60-10. Refer to Figure 5-12 for the CRCC/LRCC Output state.

$\overline{\text{CRCC STATE}}$ and LRCC STATE are decoded by:

U42-8: $\overline{\text{CRCC STATE}} = \overline{Q_A} \cdot Q_B \cdot \overline{Q_C}$

U58-6: LRCC STATE = $\overline{Q_A} \cdot Q_B \cdot Q_C$

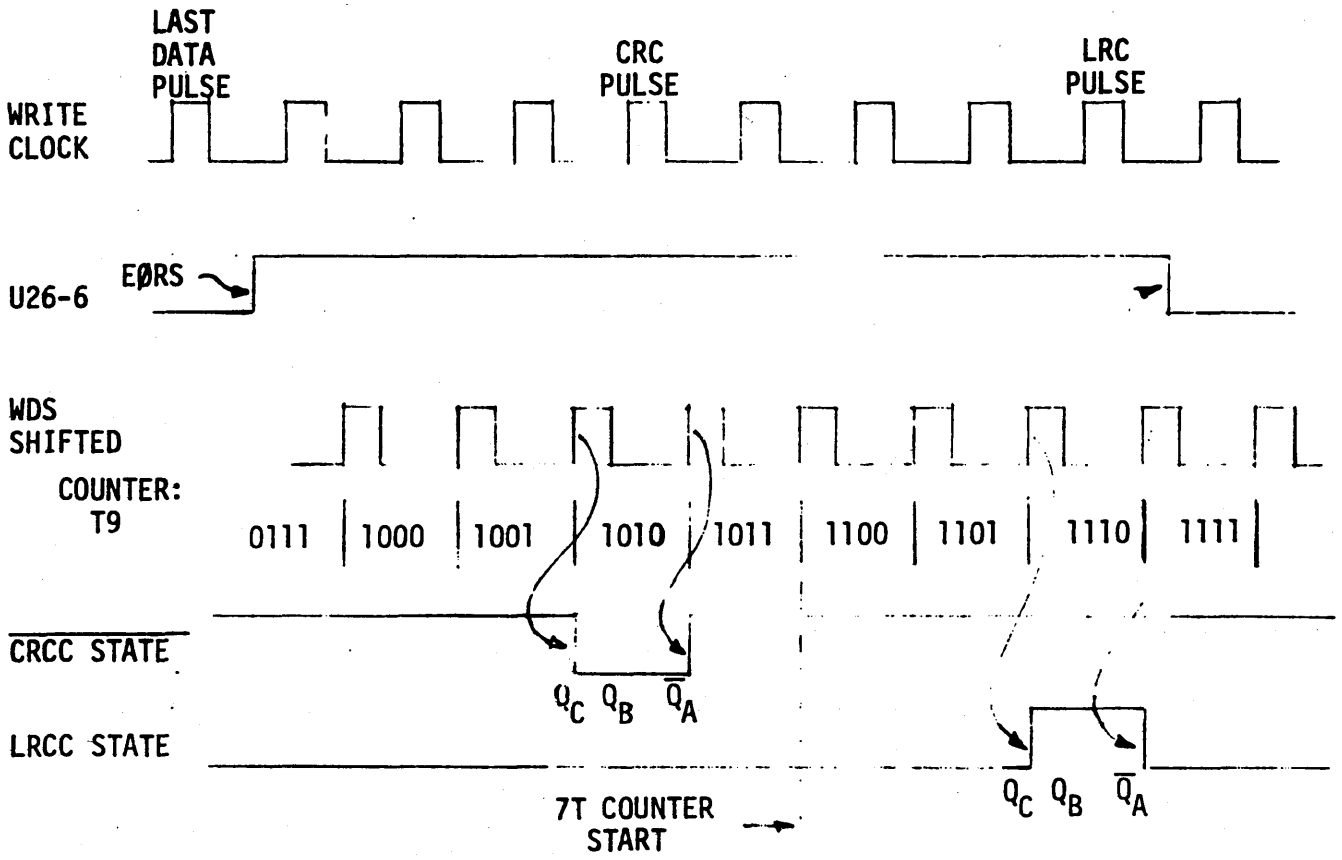


Figure 5-12. CRCC/LRCC State

Stop Distance Circuit

This module consists of two FF's that simulate the TTBUSY signal for PEC compatible tape transports. Refer to Figure 5-13.

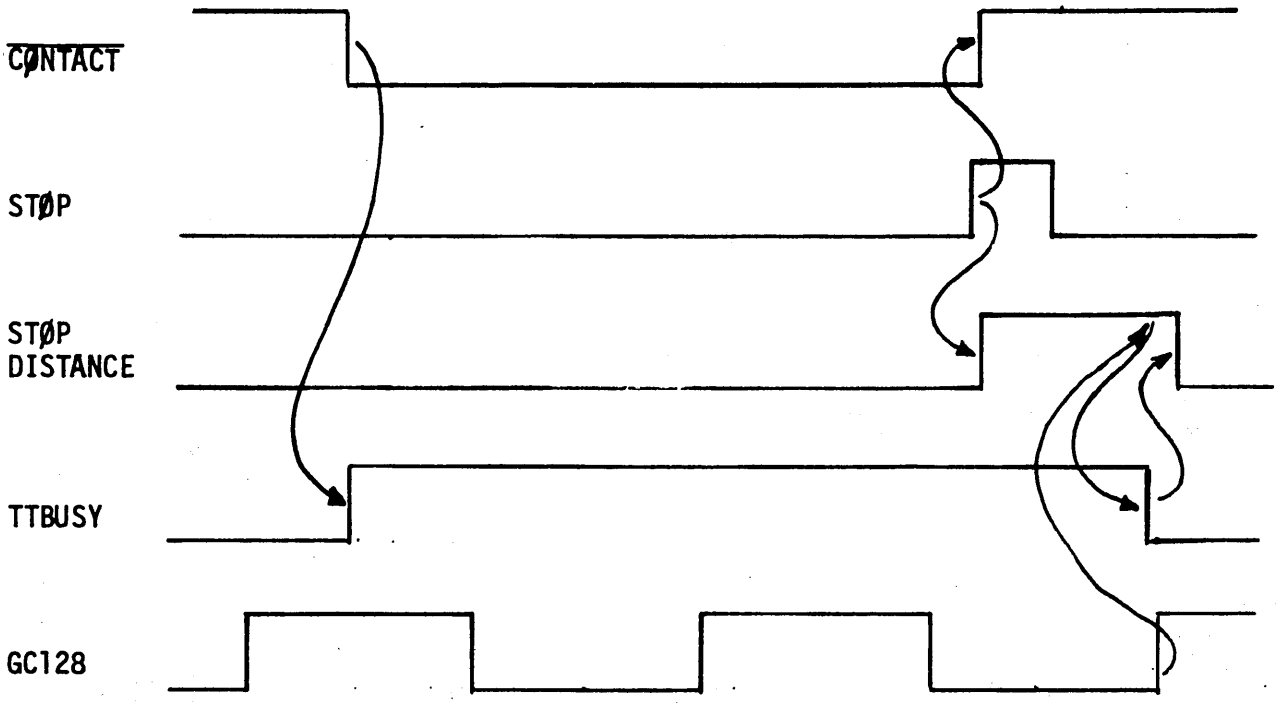


Figure 5-13. Stop Distance

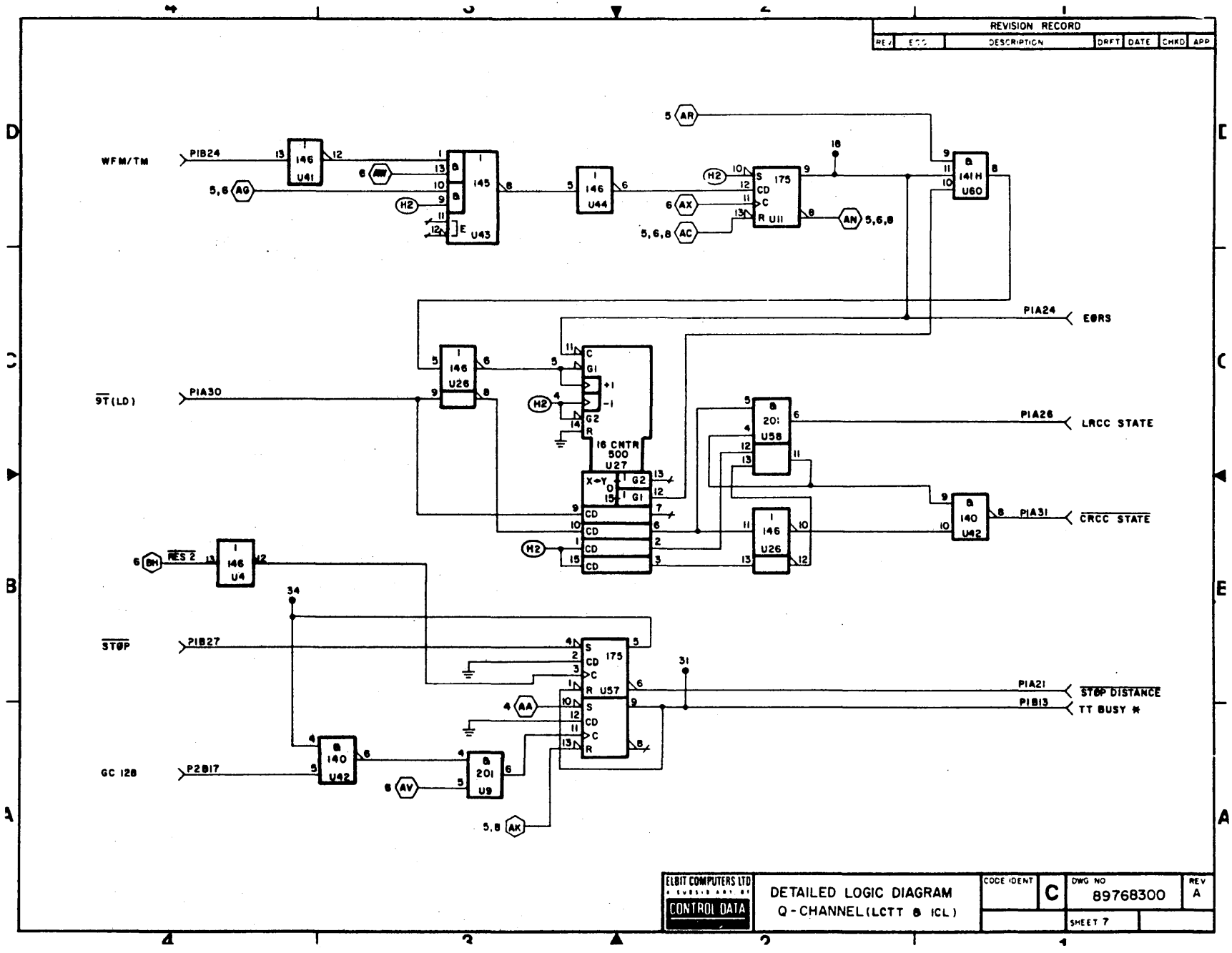


Figure 5-14. Q-Channel - End Of Record Generator Control and Stop Distance Logic Diagram

BUFFERED I/O AND SCANNER (Logic Diagram 89768300, Sheet 8) Figure 5-16.

Buffered I/O

This module stores BUF I/Ø instruction and Protect status and controls fetching of Last Word Address Plus One.

It contains three FF's: BUF I/Ø (U5-9), PROTECT (6-5) and FCW (FETCH CONTROL WORD U5-6). BUF I/Ø and FCW are set by $\overline{\text{STRBUF}}$ which also strobes A/Q PROTECT into PROTECT. All three FF's are reset by RESI.

BUF I/Ø indicates that a DSA transfer is in operation and it is cleared be the rising of:

$$\text{U41-2} = \text{EØRS} + \text{LOST DATA} + \text{EØP} + \text{LAST WORD (EØP} + \overline{\text{Busy}})$$

$\overline{\text{DSA PROTECT}}$ = $\overline{\text{DSA WREN PROTECT}}$ enables the DSA channel to Write into Protected Storage.

$\overline{\text{LDLWA}}$ falls with the setting of FCW and rises with the first INCCA. $\overline{\text{LDLWA}}$ strobes the Last Word Address Plus One into the LWA latch, it does not change again during the DSA transfer.

Scanner

The Scanner transfers the scanning signal of the whole system through the controller according to the position of the controller in the system as shown in Figure 5-15.

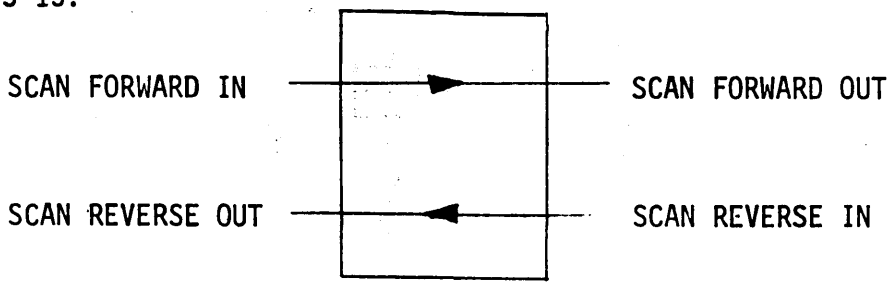


Figure 5-15. Scan Control

Middle: U56-5 = 1. The scanning signal passes SCAN FOR IN through U18-15, U1-3, U35-3, U19-6, U17-1, U20-6, U34-6 and SCAN FOR OUT. The backward signal passes SCAN REV OUT, U17-15, SCAN REV IN.

If the NEED signal rises during the first time U19-5 (which is in the forward scanning path) rises, HALT is set. $\overline{\text{HALT}}$ blocks the Scanner at U35-2 and the second arrival of the high going SCAN IN sets REQUEST. The Scanner, therefore, is allowed to complete a full loop after HALT is set. See I/O Reference Manual.

The other connection possibilities are:

Last: The scanning path is: SCAN IN, U18-15, U1-3, U35-3, U19-6, U17-15, SCAN REV IN.

First: The scanning path is: SCAN REV OUT,U18-15, U1-3, U35-3, U19-5, U17-1, U20-6, U34-6 and SCAN FOR OUT.

One: The Scanner is in a closed loop and the oscillation period is due to the internal delay of the gates U18-15, U1-3, U35-3 and U19-5.

When no one of the four above is selected, the Scanner is Out and does not scan. To allow the system to work, the controller should be extracted and two jumpers plugged into the back panel.

Jumper 1 (P2B25 and P2A26) should connect SCAN IN with SCAN FOR OUT.

Jumper 2 (P2A27 and P2B28) should connect SCAN REV IN with SCAN REV OUT.

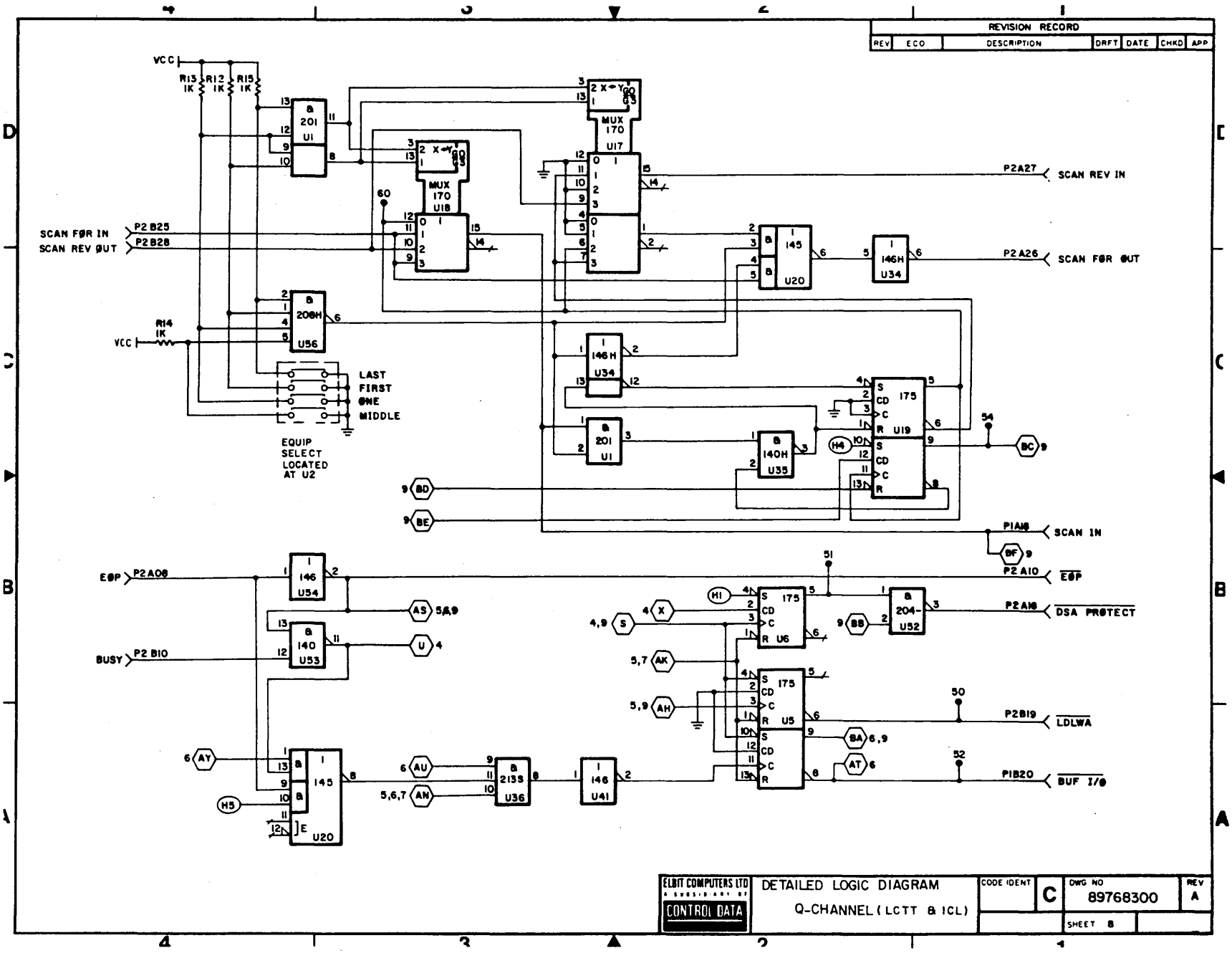


Figure 5-16. Q-Channel - Buffered I/O and Scanner Logic Diagram

REQUEST/RESUME LOGIC (Logic Diagram 89768300, Sheet 9)

This module consists of four transfer FD's and two status FF's: the need (J14-9), REQUEST (U14-5), CONNECT (U13-5), DSAWREN (U13-9), PARERR (U16-9) and PROTECT FAULT (16-5) FF's.

The NEED is set when a data word is to be transferred to or from the DSA channel. NEED is set by:

1. $\overline{\text{STRBUF}}$ to transfer the LWA+1
2. STRWMØT·BUF I/O to initiate data transfer (U15-8) during Write Motion (U28-11).
3. Rising of $\overline{\text{TRANS}}$ if BUF I/Ø·LOST DATA is high, for transferring data words. NEED is reset by RES1+CONNECT. If NEED is set, the controller blocks the Scanner by raising a HALT and waits for SCAN IN. REQUEST is set by HALT·SCAN·IN. REQUEST sends the computer a $\overline{\text{DSA REQUEST}}$ and sets CONNECT.

The computer responds by a $\overline{\text{RESUME}}$ pulse, at the end of which the word is strobed in or out of the computer. The leading edge of $\overline{\text{RESUME}}$ sets Connect (U12-11) which resets REQUEST and NEED. If the computer is in RMØT the rising of REQ sets DSA WREN on condition that $\overline{\text{RESUME}}$ is not active. The trailing edge of $\overline{\text{RESUME}}$ resets CONNECT which strobes the data into or out of the Double Buffer and resets the DSA WREN signal. A new NEED can now be generated.

The PARERR and PROTECT FAULT are set if that signal arrives from the computer and CONNECT is high. These status bits are then sent back to the computer.

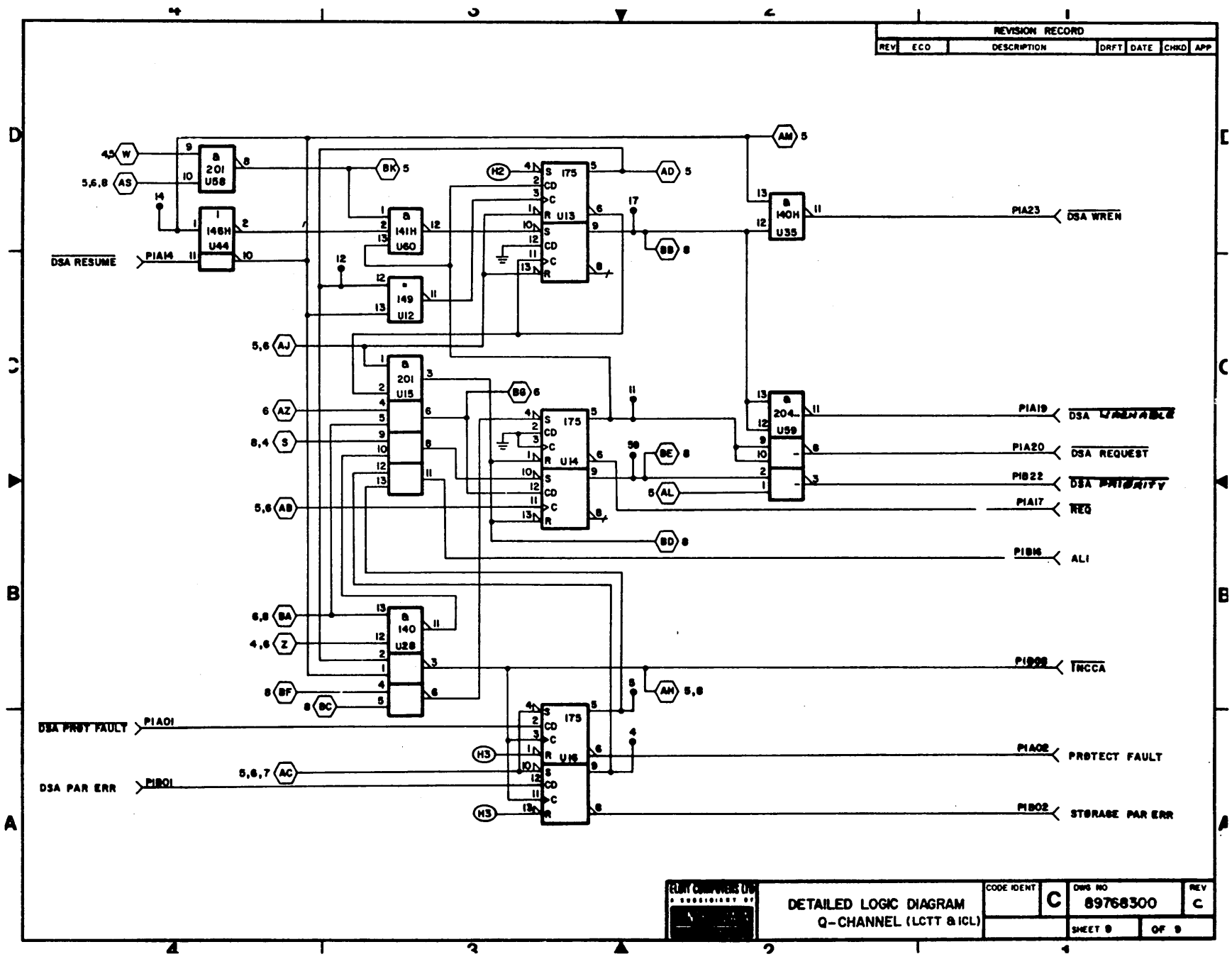


Figure 5-17. Q-Channel - Request Resume Logic Diagram

LOWER DATA SECTION (Logic Diagram 89768000)

BASIC TIMING GENERATOR (Logic Diagram 89768000, Sheet 2) Figures 5-21 and 5-22.

All the timing signals are generated from T1 and T3, having a frequency of 640 kHz for the LCTT MTTC and 960 kHz for the ICL MTTC, a width of 1/4 cycle, and a delay between them of 1/2 cycle. Refer to Figure 5-18.

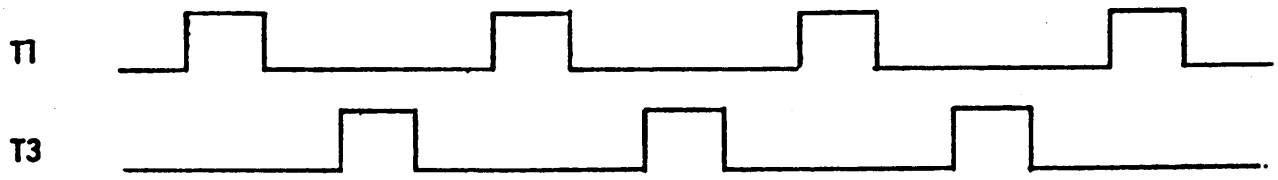


Figure 5-18. T1 - T3 Output

T1 is divided by 2 (U37-5) and by 32 (U50). The outputs are selected by U51 according to the Speed jumper.

TABLE 5-2. TIMING GENERATOR* OUTPUTS

Speed	U51-9	U51-12	U51-4	U51-7
ICL				
37.5 ips	480	240	120	30
75 ips	960	480	240	60
LCTT				
35 ips	320	160	80	20
50 ips	640	320	160	40

* Frequency in kHz.

The waveforms are symmetric and changes on the passing edge of T1.

U51-4 is divided by two (U35-5) to generate PECHARCLK at 80/160 kHz for the LCTT or 120/240 for the ICL which is symmetric, changing with T1.

U51-12 is strobed by T3 to generate PECLOCK at 320/160 kHz (LCTT) or 480/240 kHz (ICL) which is symmetric, changing with T3.

U20 and U4-6 divide by ten in order to generate GAPCLK at 16/8 kHz (LCTT) or 24/12 kHz (ICL) with a 70% duty cycle, rising with T1 and falling with T3.

U51-9 output is divided by 23 in U22-5, U21 and U4-8 to generate (at U21-7) 27.82/13.91 kHz (LCTT) or 41.74/20.87 (ICL) with a 7/23 duty cycle, rising with T1 and falling with T3.

U5-6 selects the signals from U51-7 and U21-7 according to the Table 5-3 and Figure 5-19.

TABLE 5-3. WRITE CLOCK FREQUENCY (FWC)* AT U5-6

Speed (inches per second)	800 BPI	$\overline{800\ BPI}$
LCTT		
25	20	13.91
50	40	27.82
ICL		
37.5	30	20.87
75	60	41.74

U6 and U5-8 and U7-6 differentiate the signal from U5-6 to generate 2 FWC (FETCH WORD CONTROL) (twice the frequency as shown in Table 5-3) with a pulse width of 1.04 uSec, changing with T1, as shown in Figure 5-19.

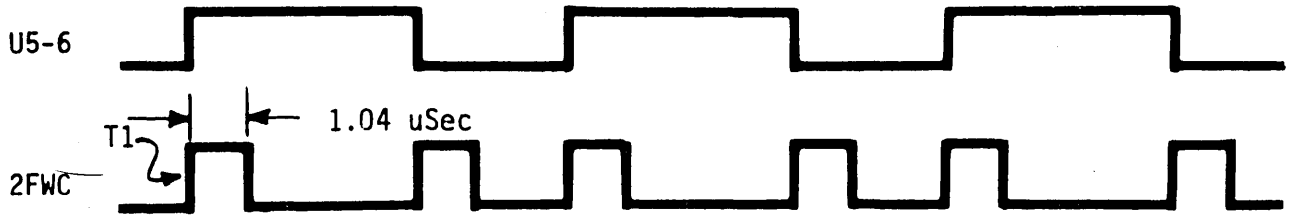


Figure 5-19. 2 FWC Generation

* Frequency in kHz

U22-9 enables EARLY WDS, SRITE CLOCK and WDS SHIFTED with frequencies as in Table 5-3. It is set if PESTART WREQUEST is high at the rise of T1. If U22-9 is high, U10-8 and U24 form the pulses shown in Figure 5-20.

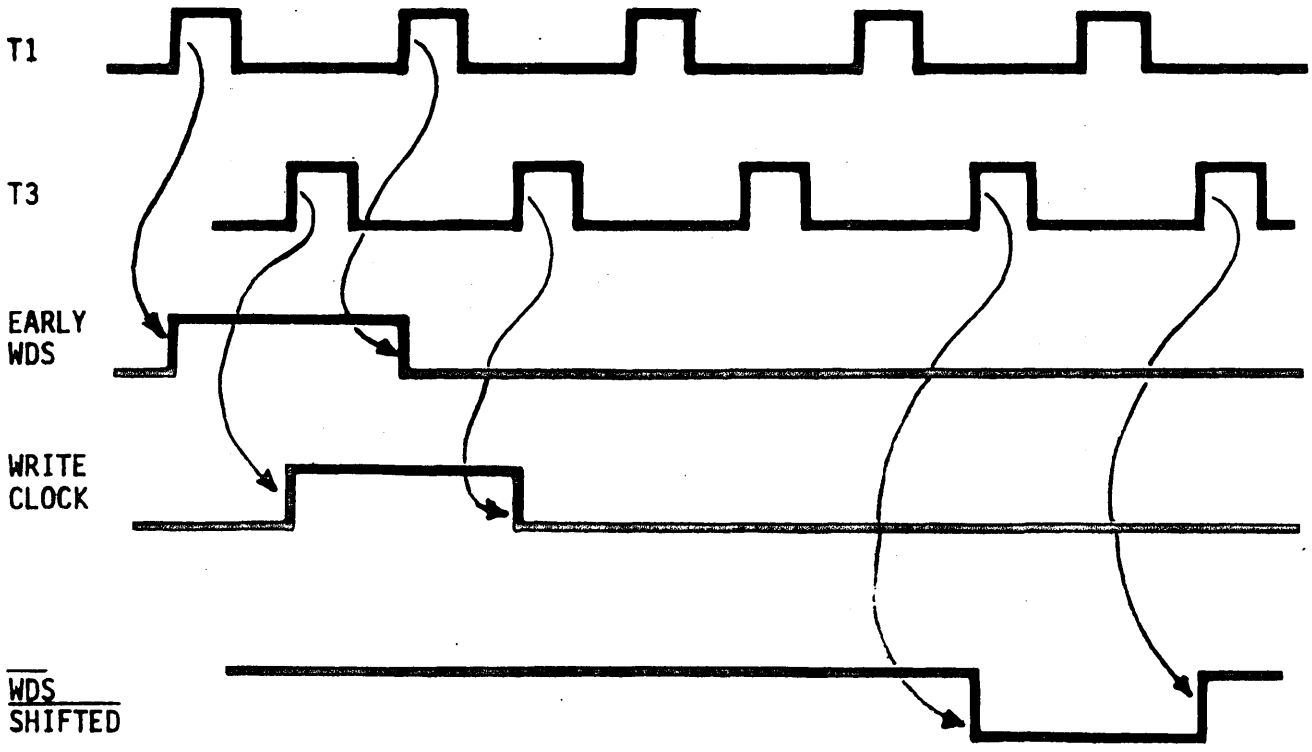


Figure 5-20. EARLY WDS, WRITE CLK and WDS SHIFTED Generation

ØFF-SHEET REFERENCE

ØFF-SHEET REFERENCE LETTER	SIGNALS	SHEET LØCATIØN 2	3	4	5	6	7	8	9
A	75IPS	B-4		B-1▼					
B	800 PBI	D-4	C-1▼						C-2
C	PE1600	B-4	C-1▼						
D			A-4			D-2	B-4		C-1▼
E			C-4		A-4	D-2	B-4		C-3▼
F	9T		C-1	C-2▼					D-4
G	RETRANSPØRT		C-2	A-1▼					B-4
K	9T		C-4	C-1					
L	1600 BPI		C-1▼						C-4
M	RES1		A-1▼			B-4		B-3	
N	RES2		A-2		C-3				
P	A0		D-4			D-2	C-4		C-1▼
Q	A4		C-4		B-4	C-4	C-4		B-1▼
R	A5		C-4			D-4	C-4		B-1▼
S	A6		C-4			D-4	C-4		A-2▼
T	A2		D-4		B-4	D-2	B-4		C-3▼
W	DUAL		B-4	D-1▼					
X	DUAL		B-4	D-1▼					
Y	RES INT		A-1▼		A-4				
Z	PE		B-4	B-1▼					
AA	556BPI		D-1▼						C-2
AB	PRØTECTED			B-1▼					B-4
AC	ALARM				B-2▼				B-2
AD	INT				B-2▼				C-4
AE	EØP (UP)				A-4				B-2
AF	DATA (Q)				C-4				D-4
AG	READY-RWIØD				D-2▼				C-2
AK	DATA IN 0					A-2	▼C-2	D-3	
AL	DATA IN 1					A-2	▼C-2	C-3	
AM	DATA IN 2					A-2	▼C-2	C-3	
AN	DATA IN 3					A-2	▼C-2	C-3	
AO	DATA IN 4					A-4	▼D-2	B-3	
AP	DATA IN 5					A-4	▼C-2	B-3	
AQ	DATA IN 6					A-4	▼C-2	B-3	
AR	DATA IN 7					A-4	▼C-2	B-3	
AS	WRTAPE 0						B-4	D-1▼	C-2
AT	WRTAPE 1						B-4	C-1▼	C-2
AU	WRTAPE 2						B-4	C-1▼	C-4
AV	WRTAPE 3						B-4	C-1▼	C-4
AW	WRTAPE 4						D-4	C-1▼	B-2
AX	WRTAPE 5						C-4	B-1▼	B-2
AY	WRTAPE 6						D-4	B-1▼	A-4
AZ	WRTAPE 7						C-4	B-1▼	A-4
BA	CURAD 0					D-1▼	A-2		C-2
BB	CURAD 1					D-1▼	A-2		D-2
BC	CURAD 2					D-1▼	A-2		C-4
BD	CURAD 3					D-1▼	A-2		D-4

SHEET REVISION STATUS

1	2	3	4	5	6	7	8	9
01	01	01	01	01	01	01	01	01
02	01	01	01	01	01	01	01	01
03	03	03	03	03	03	03	03	03
04	04	04	04	04	04	04	04	04
A	A	A	A	A	A	A	A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	CK690	RELEASED TO CLASS B				
02	CK770	ADD DETACHED LIST				
03	CK 798	REDRAWN TO CDC STD				
04	CK 987	NOTE ADDED TO FIT LOGIC TO ICL U53, SH 2. WAS 201				
A	CK 1242	RELEASED CLASS A				

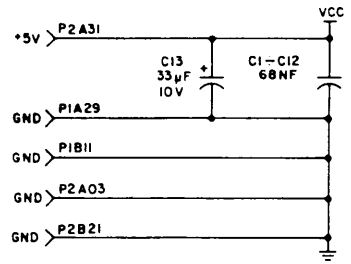
		2	3	4	5	6	7	8	9
BE	CURAD 4					D-3▼	B-2		B-2
BF	CURAD 5					D-3▼	A-2		B-2
BG	CURAD 6					D-3▼	B-2		A-4
BH	CURAD 7					D-3▼	A-2		B-4
BI	A7					D-4	C-4		A-2▼

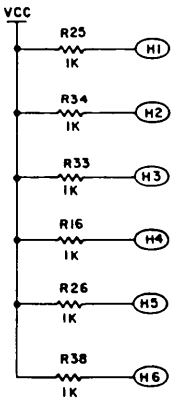
NOTES

1. ⚠1 JUMP CONFIGURATION (ON LOGIC SH 3)

	LCTT	ICL
JUMP:	C1 WITH P1	C1 WITH I1
	C2 WITH P2	C2 WITH I2

2. ALL RESISTØRS ARE 25W ± 5%
3. ▼ - DENØTES SIGNAL ØRIGIN





AW 89767900
AY 89767800 (LCTT)
AY 89841600 (ICL)
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA

DWN	[illegible]	23/6/76
CHKD	[illegible]	[illegible]
ENGR	[illegible]	[illegible]
MFG	[illegible]	[illegible]
APPR	[illegible]	[illegible]
Q A	[illegible]	[illegible]

FIRST USED ON
FA446-A
FA442-A

TITLE
DETAILED LOGIC DIAGRAM
LOWER DATA (LCTT & ICL)

CODE IDENT	DRAWING NO
C	89768000

SCALE
SHEET 1 OF 9

Figure 5-21. Lower Data Section Logic Diagram Reference Sheet

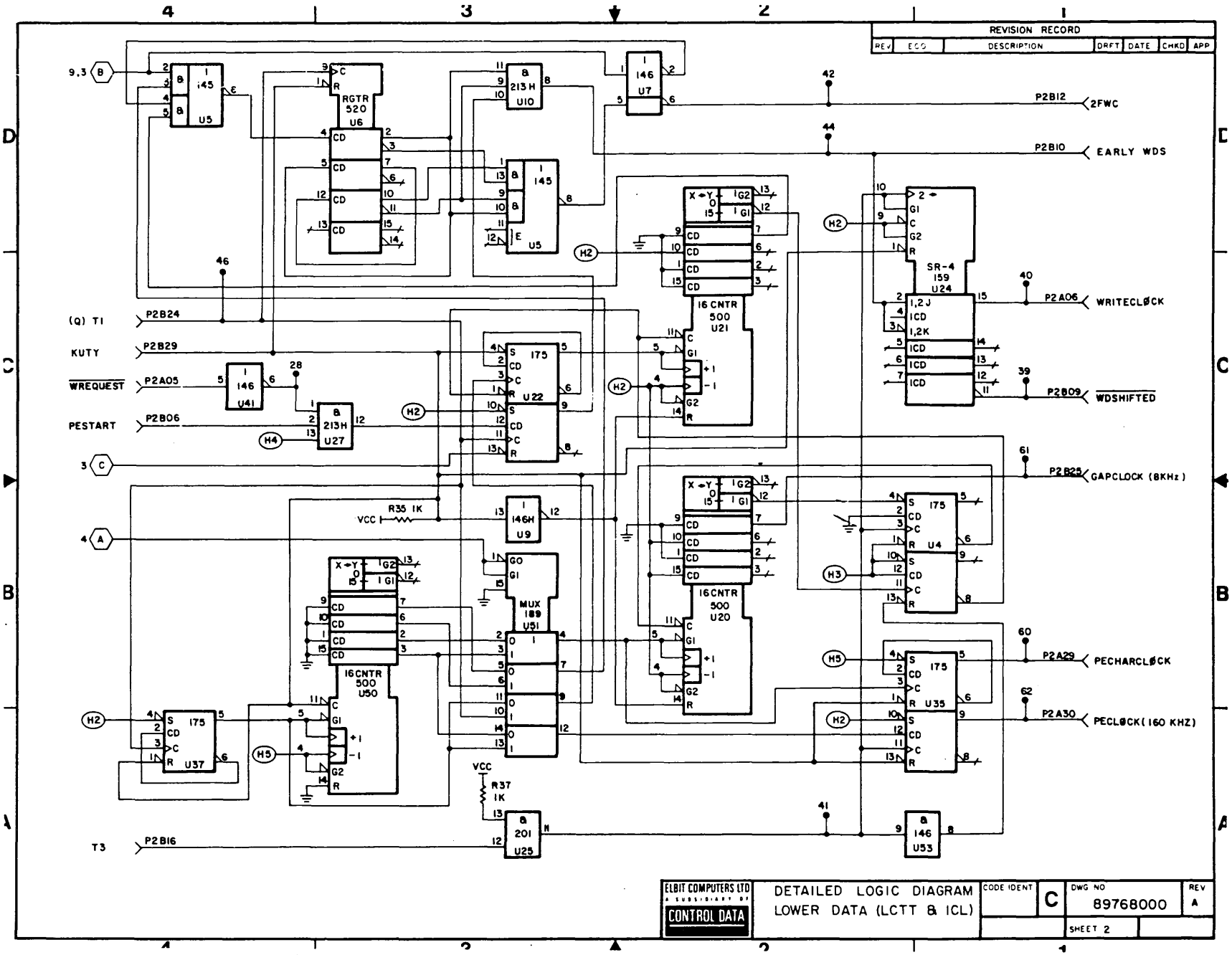


Figure 5-22. Lower Data Section - Basic Timing Generator Logic Diagram

OPERATION CONDITIONS (Logic Diagram 89766000, Sheets 3 and 4) Figures 5-23, 5-24.

The operation conditions include all the conditions that define the connection of the controller and the MTT after execution of a unit select operation. The conditions are generated by manually set switches and FF's set by UNIT SELECT (US) operation.

This module checks to determine if the UNIT SELECT instruction is legal, and if so, it signals this to the Reply/Reject logic, and stores the UNIT SELECT information. This module also generates the $\overline{MC}$ and $\overline{REST}$ signals.

Three FF's MØDSEL, A/D, BCD store the density, format and code of the selected unit.

$\overline{MODSEL}$ (U39-6) is high if 1600 bpi density is selected. $\overline{MODSEL}$ can be set only if a nine track dual mode transport is slected. MODSEL is strobed by STRUS according to 9T·A3+9T·A4 (U43-9). It is reset by $\overline{MC}$.

$\overline{A/D}$ (U23-10) is high if Character Format is selected. This FF is strobed by STRUS according to A0 and A6: If A0·A6 is low, $\overline{A/D}$ does not change. If A0 is high $\overline{A/D}$ is set if A6 is high setting $\overline{A/D}$ (Both cannot be set). MC sets A/D Format.

BCD (U39-9) is high if the BCD Code is selected. BCD is set by STRUS according to A1. If A1 is high then BCD is set. For every other STRUS, BCD is reset. MC sets the Binary Code.

The signal LEGUS (LEGAL UNIT SELECT, U57-8) is a combinational function of A0-A6, $\overline{TTDS}$. The Density Status from the tape, BØT, 9T, ILLUSCODE (the check for legal unit select from another module), $\overline{PC\text{-}1600}$ (which indicates that the phase encoding formatter is inserted in the chassis), CONTACT, $\overline{DUAL}$ and PE, is as follows:

(U43-7) $Z_A = A5 \cdot 9T + A3 \cdot \overline{9T}$

(U43-9) $Z_B = A3 \cdot 9T + A4 \cdot \overline{9T}$

(U43-12) $Z_C = A4 \cdot 9T + A5 \cdot \overline{9T}$

(U43-4) $Z_D = A1 \cdot 9T$

(U42-8) $Z_E = \overline{Z_A \cdot Z_B + A0 \cdot A6 + A1 \cdot A2 + ILLUSCODE}$

(U57-6) $Z_F = \overline{Z_C + Z_D + \overline{Z_E}}$

$DS = TTDS \cdot \overline{9T \cdot Dual} + PE \cdot 9T \cdot DUAL$

(U8-8) $Z_G = DUAL \cdot 9T + \overline{\overline{DS} \cdot Z_A + DS \cdot Z_B}$

$LEGUS = Z_G \cdot Z_F \cdot \overline{CONTACT} \cdot (PC1600 \div \overline{A5})$

If LEGUS is high, then the UNIT SELECT instruction will reply as:

(U25-3) 800 BPI = $\overline{\overline{9T} \cdot \overline{DS} + 9T \cdot DS}$

(U7-12) 1600 BPI = $9T \cdot DS$

(U7-8) 556 BPI = $\overline{9T} \cdot \overline{DS}$

PEENABLE enables the phase encoding formatter and also resets it when low (U10-6). PEENABLE = $\overline{REST} \cdot 1600$

PETRANSPORT on Sheet 3 is a Status signal that indicates that the transport has 1600 bpi capability and the phase encoding formatter is connected (U27-6 on Sheet 3). PETRANSPORT = $PC1600 \cdot 9T \cdot (DUAL + PE)$.

RES1 on Sheet 2 clears most of the FF's in the controller. It is a combination of STROBE UNIT SELECT, MC and CLEAR CONTROLLER (STRCF·A1), so:

(U55-6) RES1 = STRUS+MC+STRCF·A1.

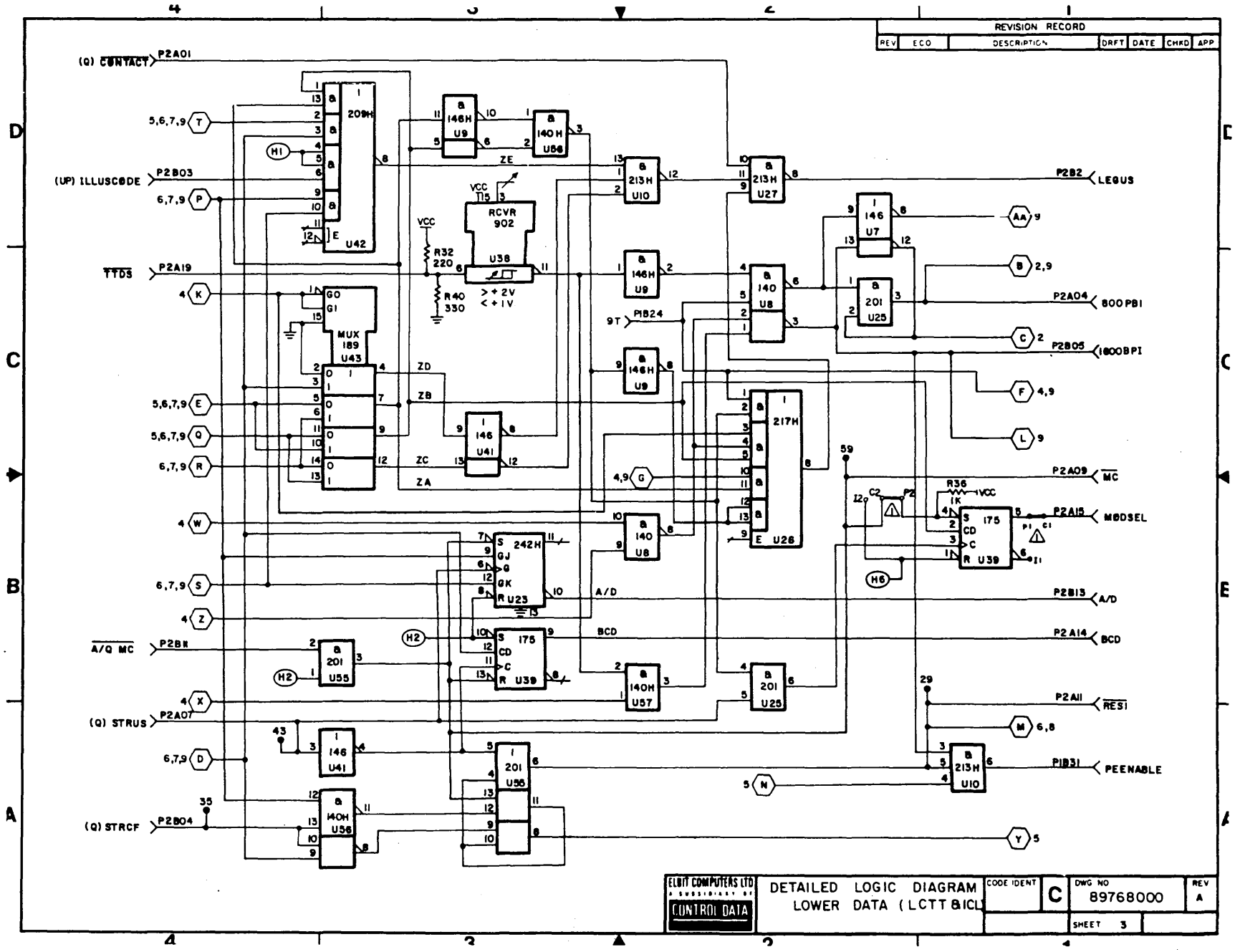


Figure 5-23. Lower Data Section - Operation Conditions Logic Diagram

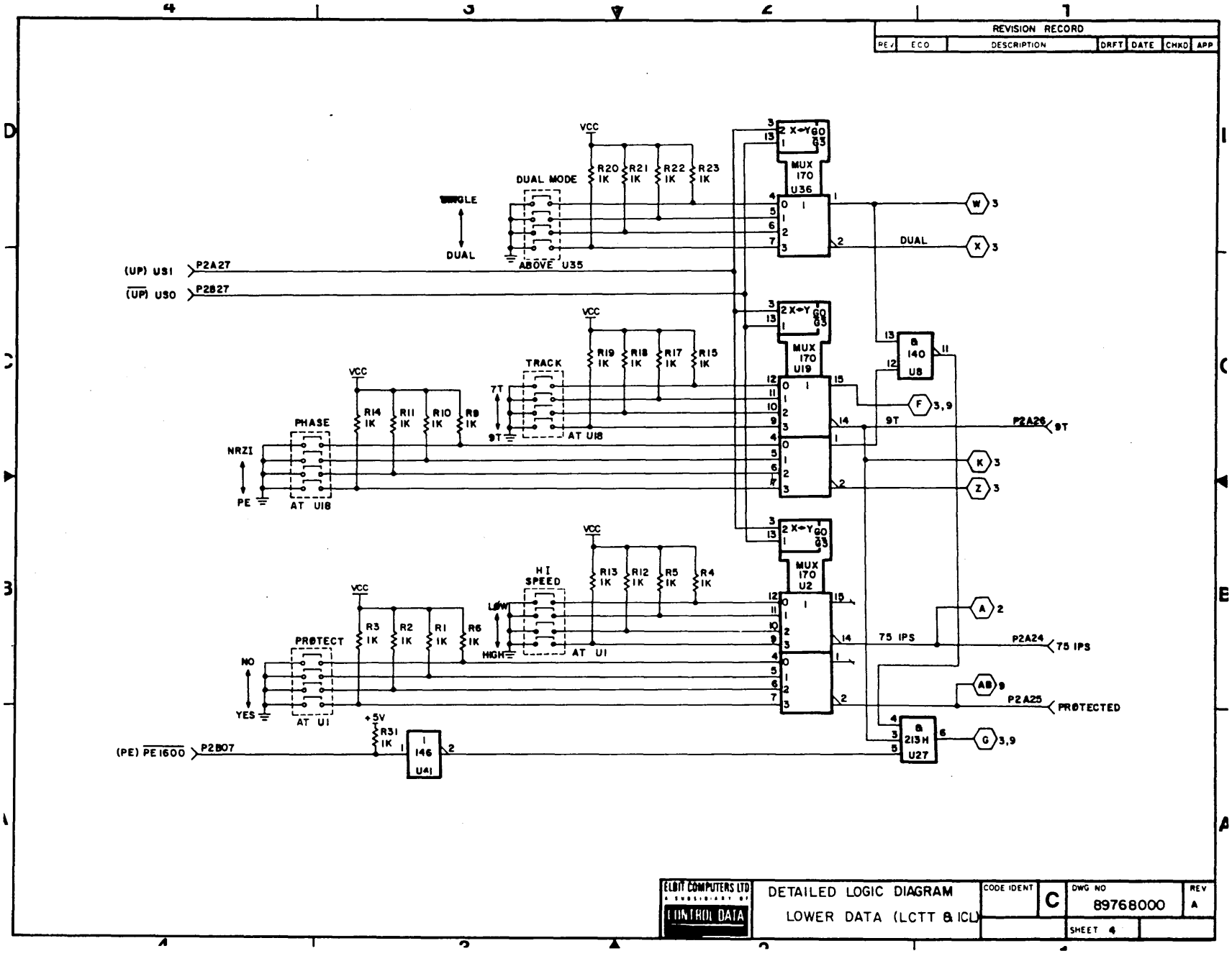


Figure 5-24. Lower Data Section - Operation Conditions Logic Diagram (Cont'd)

INTERRUPTS (Logic Diagram 89638000, Sheet 5) Figure 5-24.

Interrupt Circuit

One Interrupt signal is sent to the computer, for at least one DATA, EØP or ALARM INTERRUPT (if enabled). This module includes three Interrupt Enable FF's: DATAINT Enable (U23-15), EØPINT Enable (U40-11), ALARMINT (U40-15) and one Rising Edge Detection FF - EØP (U3-9).

The three Enable FF's are reset by U55-8 (Sheet 3) (RESINT = MC+STRCF(A0+A1). These flip flops are set by STRINT according to A2, A3 and A4, respectively. If A2 is high when strobed, then the DATAINT Enable FF is set. If A2 is low when strobed, then the DATAINT Enable FF does not change.

EØPINT is set when the EØPINT Enable FF is high and EØP rises.

INTERRUPT = DATA·DATAINT ENABLE + EØPINT+ALARM·ALARMINT ENABLE

Alarm Circuit

This module includes the BUSY·$\overline{\text{READY}}$ FF's and the combinational circuit that detects Alarm:

U37-8 on Sheet 5 (BUSY·READY) is set by the rise of TTREADY if RWLD+RWUNLD is low.

ALARM (Sheet 5) = BUSY·$\overline{\text{READY}}$ + EQT+PARITY ERR+LOST DATA+FM/TM+AL1+AL2

AL1 and AL2 are auxiliary Alarm conditions from the PE Formatter.

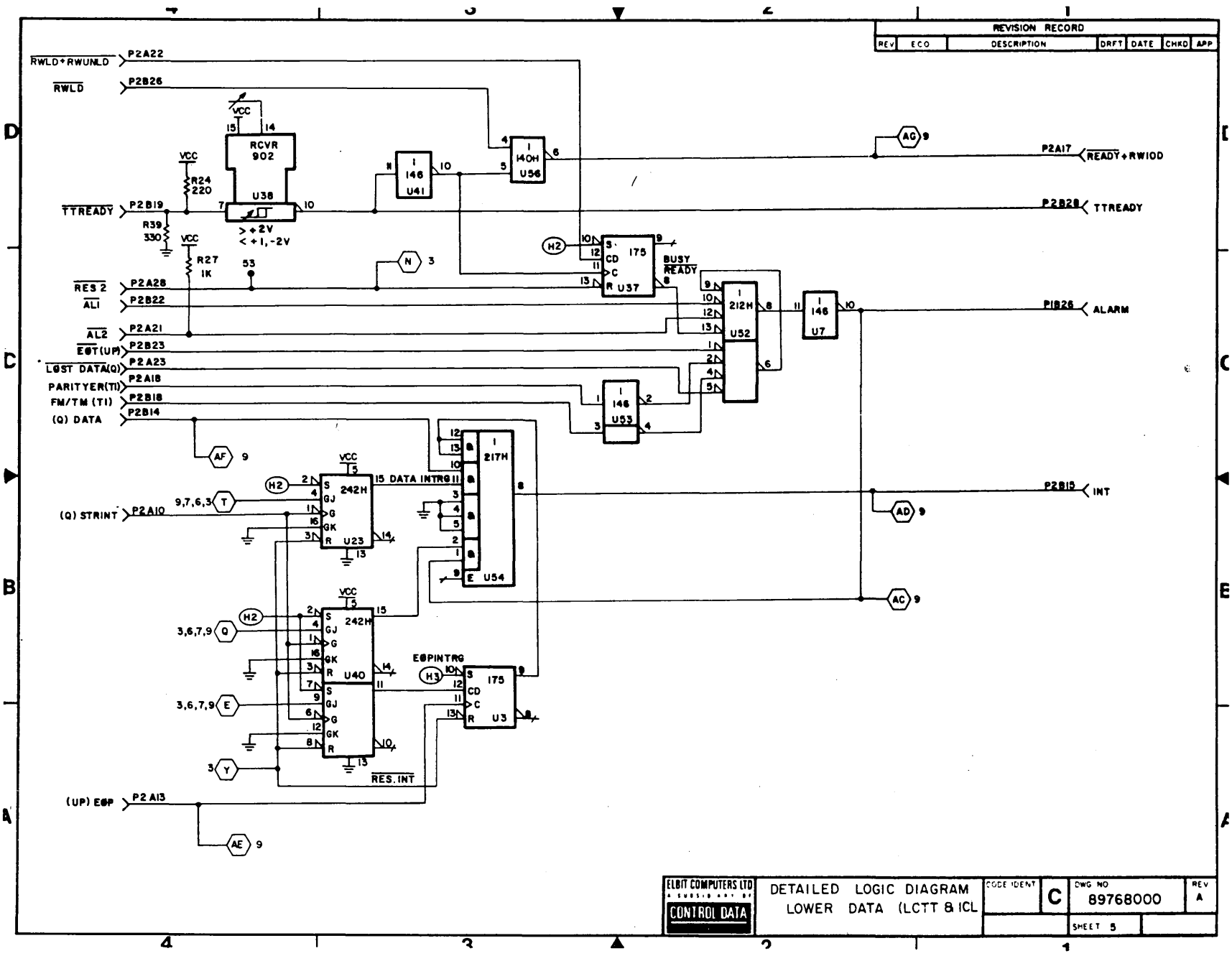


Figure 5-24. Lower Data Section - Interrupts Logic Diagram

LOWER DSA DATA PATH (Logic Diagram 89768000, Sheets 6 and 7) Figures 5-27, 5-28.

$\overline{\text{STRBUF}}$ initiates DSA transfer and presets CURADOR (0-7) to the contents of A00-A07. The A/Q DSA Selector is set by BUFF I/O to DSA Selector and the first transfer generates $\overline{\text{LDLWA}}$, that strobes the contents of DSA Data (0-7) into LWA+1.

Every Transfer Request enables the current address on the DSA ADDR lines and the falling of INCCA increments the Current Address. When Writing, the data is transferred through DSA Data (0-7), A/Q DSA Selector to the Double Buffer and then to the tape. See Figure 5-26.

When Reading from the computer, the data is transferred from the tape, the Double Buffer and DSA WREN enables the data to pass to the computer memory.

A = B is the Comparator signal to the second half of the Comparator.
CARCURAD is the Counter overflow to the second half in the Upper Data card.

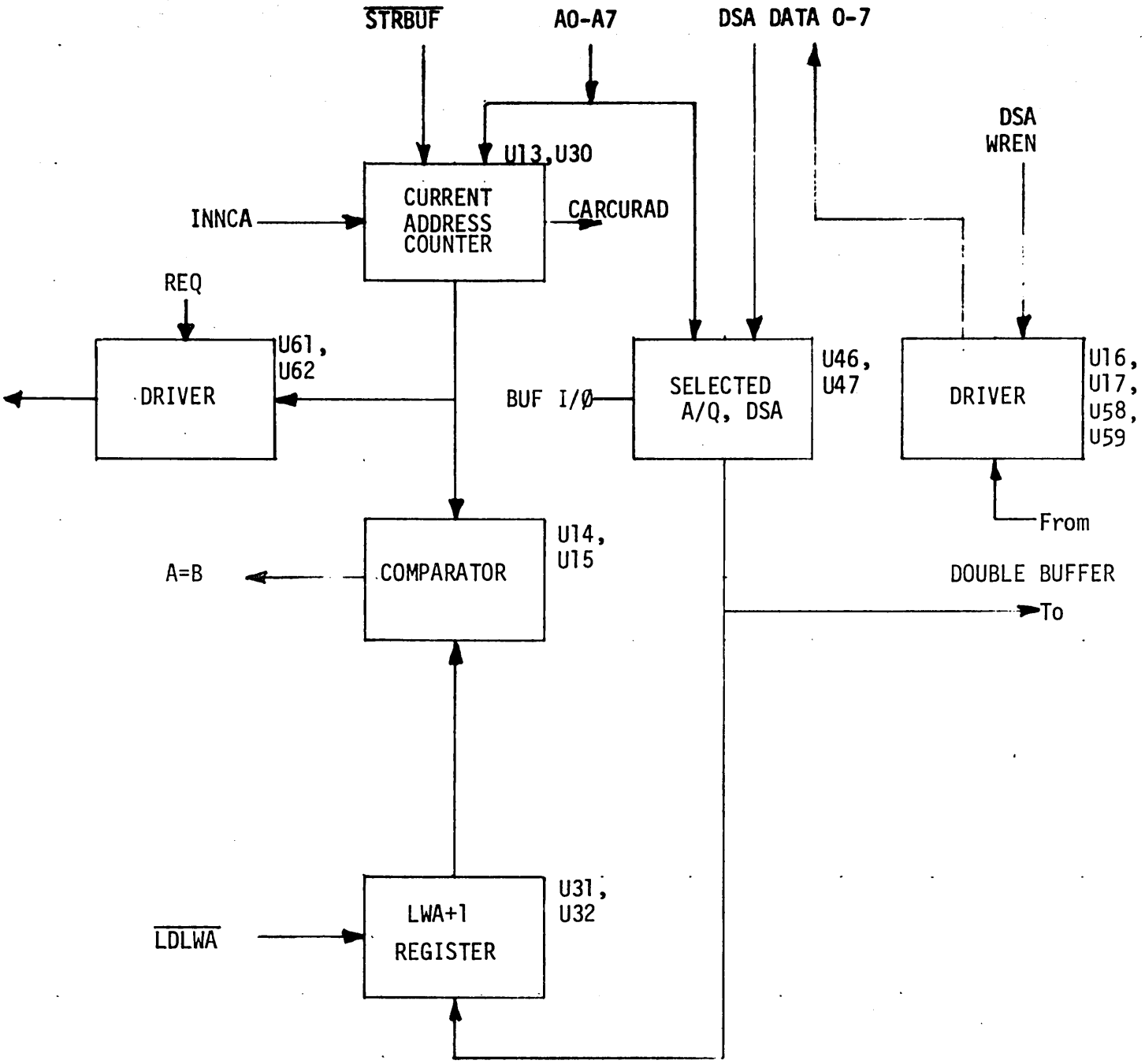


Figure 5-26. Lower DSA Data Path

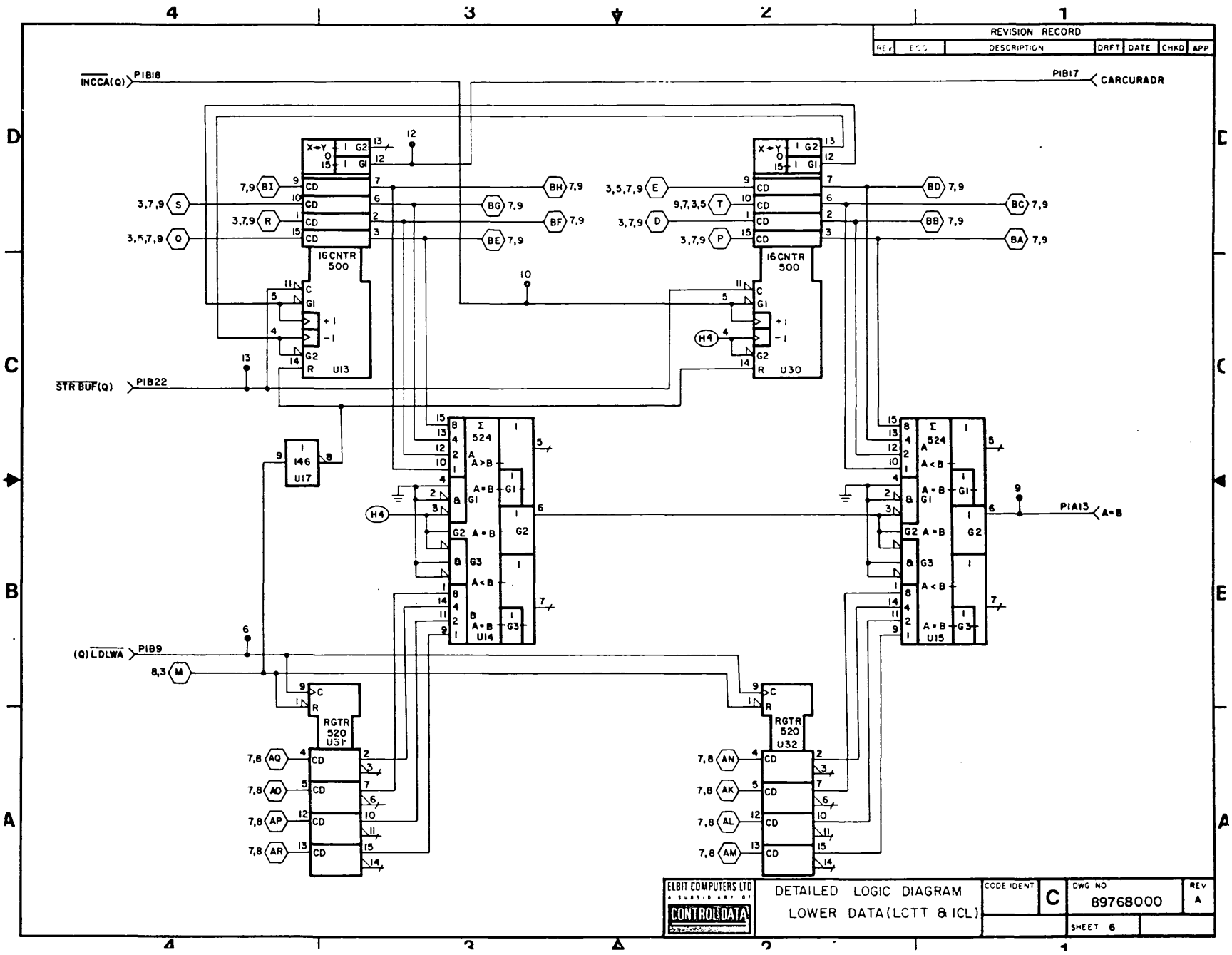


Figure 5-27. Lower Data Section - Lower DSA Data Path Logic Diagram

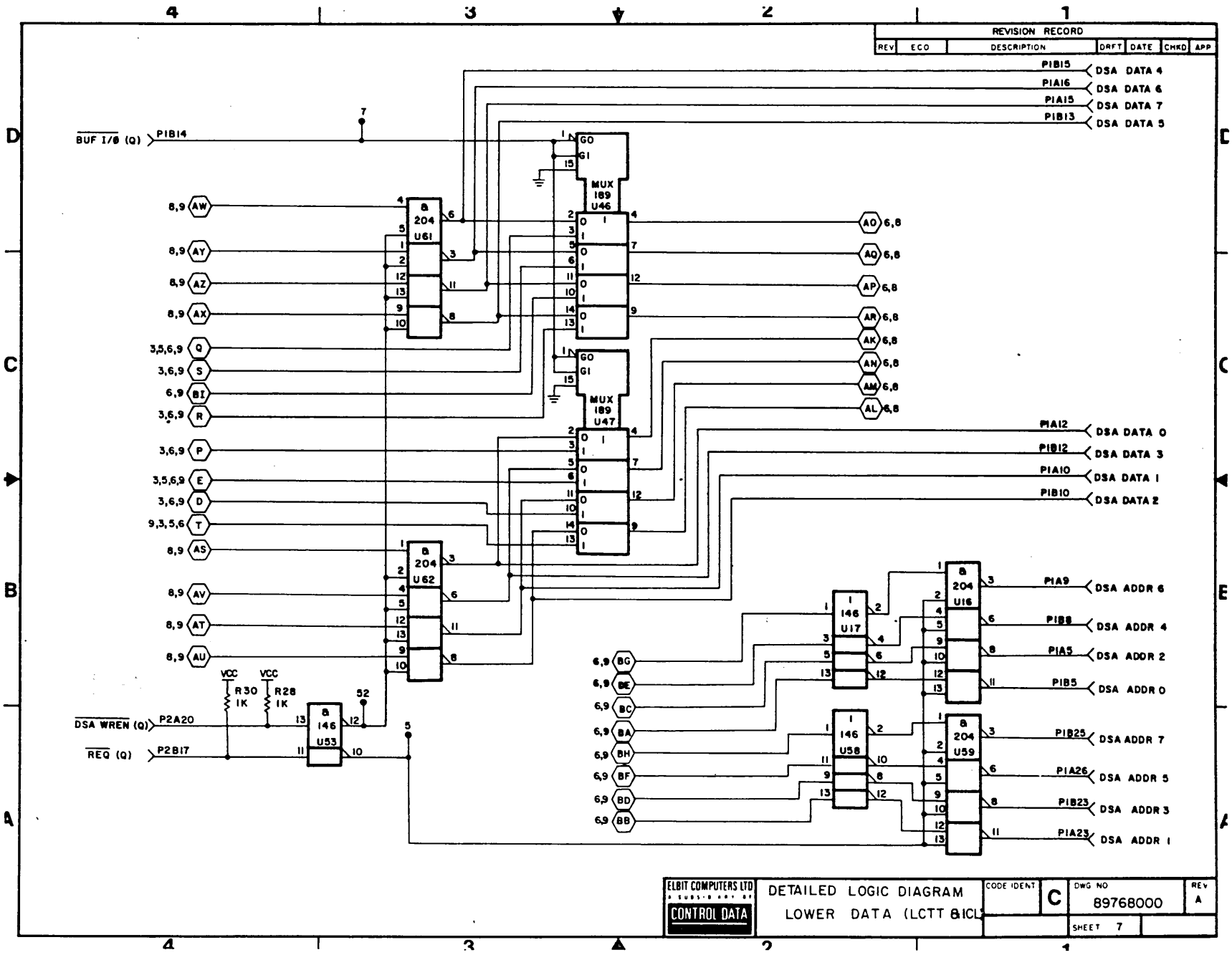


Figure 5-28. Lower Data Section - Lower DSA Data Path Logic Diagram (Cont'd)

LOWER A DATA PATH (Logic Diagram 89768000, Sheets 8 and 9) Figures 5-30, 5-31.

For the block diagram of the Lower A Data Path, refer to Figure 5-29.

RSTAPE 0-7 signals from the tape transport are passed through a multiplexer U64 (RDTAPE 0-3) and U62 (RDTAPE 4-7) when $\overline{\text{RMOT}}$ is low. With $\overline{\text{RMOT}}$ high, DATAIN 0-7 signals from the computer are admitted. The output of the multiplexer (Selector 1) is then supplied to Buffer 1 (U49, U34) which is controlled by the signal $\overline{\text{LOWXT}}$ through U49-9 and U34-9. Buffer 1 is cleared by $\overline{\text{CLEARLOWER}}$ + $\overline{\text{REST}}$ through U25-8 to U34-1 and U49-1. BUFFER 2 (U48, U33) further passes the signal to produce WRTAPE 0-7 signals for the tape transport, when the TRANS signal is low (U48-9, U33-9) and $\overline{\text{RMOT}}$ is high at U64-1 and U63-1. Buffer 2 is cleared by $\overline{\text{REST}}$. With $\overline{\text{RMOT}}$ low, the RDTAPE 0-7 data is available for transfer to Selector 2 (multiplexers U44, U28, U11 and U12, Sheet 8), but will only be accepted when the sum of SELA0 and SELA1 represents a binary 3. If both signals are binary 0, Current Address status is selected. If SELA0 and SELA1 are other than binary 3, only STATUS signals are passed on through Selector 2. When SELA0 is high and SELA1 is low (binary 1), STATUS 1 is selected, and if SELA0 is low with SELA1 high (binary 2), STATUS 2 is selected. These signals are NANDed through U60, U29, when enabled by $\overline{\text{ENA}}$ (high) to the A-bus to the computer.

When signals are received from the computer A-bus, they are admitted through U45, U58 to the other Lower Data Section circuitry.

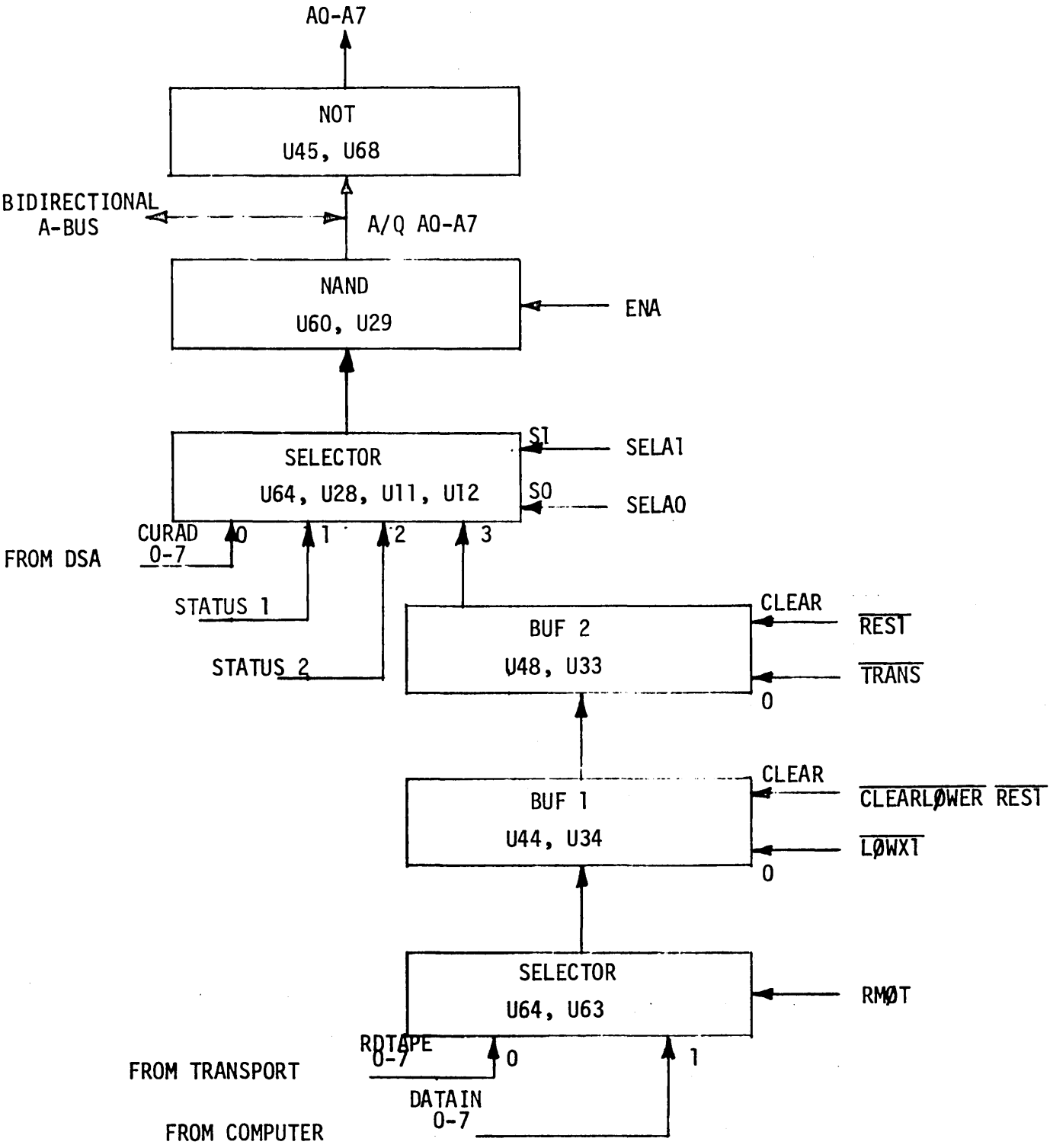


Figure 5-29. Lower A Data Path

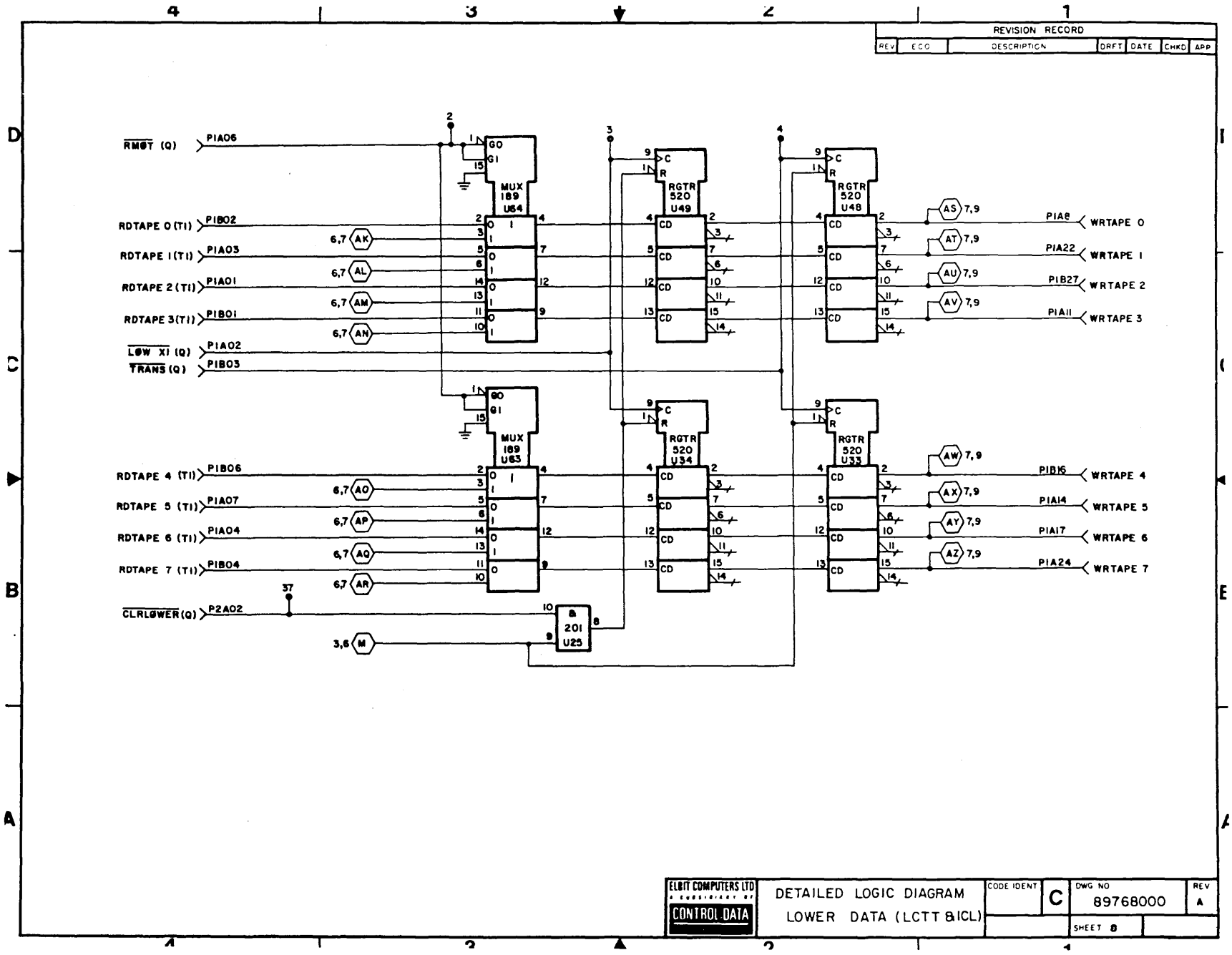


Figure 5-30. Lower Data Section - Lower A Data Path Logic Diagram

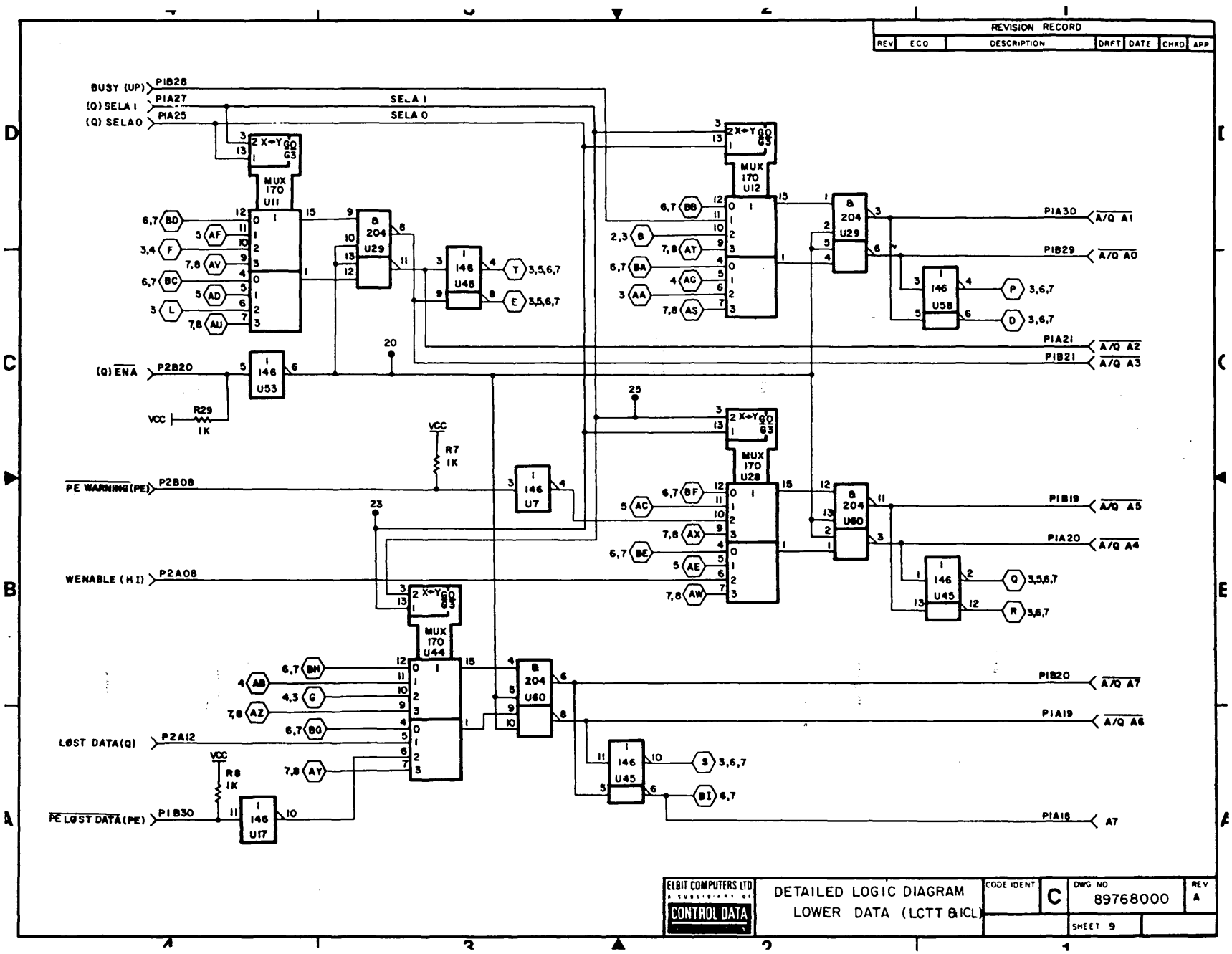


Figure 5-31. Lower Data Section - Lower A Data Path Logic Diagram (Cont'd)

UPPER DATA SECTION (Logic Diagram 89767700)
GAP TIMING GENERATOR (Logic Diagram 89767700, Sheet 2) Figures 5-32 and 5-33.

This module includes the Gap Counter (U19, U51, U36) and Timing Decoder. It also includes BØT (BEGINNING ØF TAPE) and EØP FF's.

The Gap Counter counts GAPCLOCK pulses when GAPCLOCK is low. The PREGAP (U7-8) and POSTGAP (U5-3) are determined according to Table 5-4.

TABLES 5-4. PREGAP - POSTGAP COUNTS

SIGNAL	PREGAP (U7-8)				POSTGAP (U5-8)			
	9T		7T		9T		7T	
	BOT	$\overline{BOT}$	BOT	$\overline{BOT}$	BOT	$\overline{BOT}$	BOT	$\overline{BOT}$
READ								
ICL	640	128	640	128	24	24	24	24
LCTT	1536	128	1536	128	24	24	24	24
WRITE								
ICL	2048	192	2048	256	32	32	32	32
LCTT	2560	192	2560	256	24	24	24	24
READ REVERSE								
ICL	128	128	128	128	32	32	32	32
LCTT	NA	128	NA	128	NA	64	NA	64
WRITE FMTH								
ICL	2048	2048	2048	2048	32	32	32	32
LCTT	2560	2560	2560	2560	24	24	24	24

BØT (U1-9) is set by $\overline{TTBØT}$ and is reset by the rising of START:

EØT is set by $\overline{TTEØT}$ and reset by RES2.

PEBØT (U52-11) sets if BØT is high after 512 GAPCLOCK pulses. PEID (U35-9) is set if BØT is high after 1152 GAPCLOCK pulses and is reset after 2176 pulses.

OFF-SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION 2	3	4	5	6	7	8	9
A	WRTAPE II					4B	▼1D	4C	
B	PMØT		2D				4D		
D					4A	▼2D	4B		
E					4A	▼2C	4B		
F					4A	▼2C	4B		
G					2A	▼2B	4C		
J					2A	▼2B	4C		
K					2A	▼2B	4C		
L					2A	▼2B	4C		
M	BØT	▼2D	4B					4C	
N	TT. READY	4D	3A						
P									
Q	A7	4C	4D						4C
R	A11				2D	4C		▼3C	4C
S	A8	4C	4D		3D	4C		▼1C	4C
T	A9		4D		2D	4C		▼1C	4C
U	A10		4D						4C
V	MØTCODE 8	2B	▼3D						
W	MØTCODE 7	2B	▼3D						
X	A12				4D	4C		▼1A	3A
Y	EØP		▼1C	4C					3A
Z	T3	4A	2C	4C					
AA			4B						▼3A
AB	EØP		▼1B						3B
AD	TT. BUSY		3B						2A
AE								3C	▼2B
AF	PREØAP	▼1B		3C					
AG	WFM	2B	▼1D						
AH	WRØT	2B	▼1D						
AJ	PØSTØAP	▼1A		4D					
AK		2B	▼1D						
AL	REV	2A	▼1B						
AM	START	3D		▼2B					
AN	RES 1.1	3C	3C	3D	4B				
AP	WREQUEST		▼3D						2B
AQ	CONTACT		▼1C	2C				2B	
AR	GAP	4A		▼1B					
AS	STRMF	4C	▼4C	2D					
AT	EØT		▼3A					2D	
AU	STOP		4C	▼1C					
AV	RES I.I + CH. MODE				▼1A		4B		
AW	A15				4D	4C		▼3B	
AX	A14				4D	4C		▼3B	
AY	A13				4D	4C		▼1B	
AZ	CURAD 15				▼3D	2A		4B	
BA	CURAD 14				▼3D	2B		4B	
BB	WRTAPE 15					4C	▼1A	4B	

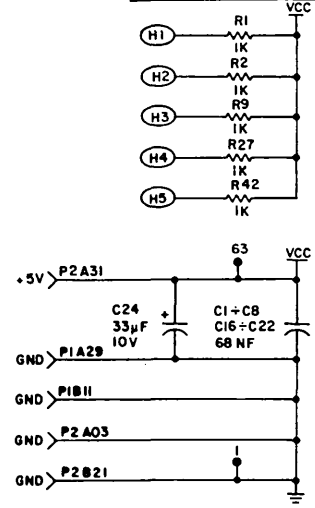
CONTINUED ON PAG. 10

SHEET REVISION STATUS

1	2	3	4	5	6	7	8	9	10
C	B	A	B	A	A	A	A	A	1
D	D	D	B	A	A	A	A	D	D
E	D	D	B	A	A	A	A	E	D
F	D	F	B	A	A	A	A	F	D

SHEET REVISION STATUS

1	2	3	4	5	6	7	8	9	10
01	01	01	01	01	01	01	01	01	01
02	01	02	01	01	01	01	01	01	01
03	03	03	03	03	03	03	03	03	03
04	04	04	03	04	04	03	04	04	04
05	05	05	05	05	05	05	05	05	05
06	06	06	06	05	05	05	05	05	05
A	A	A	A	A	A	A	A	A	A
B	B	A	B	A	A	A	A	A	A



REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	CK 690	RELEASE TO CLASS B	[illegible]	1.9.74	[illegible]	[illegible]
02	CK 777	INVERTER U23 ADDED BETWEEN U21-1 & U8-11	[illegible]	Sep. 74	[illegible]	[illegible]
03	CK 798	REDRAWN TO CDC STD	[illegible]	24, 74	[illegible]	[illegible]
04	CK 891	UI AND ITS CONNECTIONS ADDED U29-2 CUT FROM U43-10 U29-13 CUT FROM U43-2 P6(C-3) ISOLATED, THEN CONNECTED TO U46-12 U34-3 WAS U34-2 U34-2 WAS U34-3 FITS ASSY 89845200 REV.01	S.D	24, 17, 74	[illegible]	[illegible]
05	CK 987	U37 WAS 74H04 NOTE ADDED TO FIT LOGIC TO ICL	[illegible]	2.7.74	S.D	[illegible]
06	CK 1195 1299	~~SH'4 U56-11 ISOLATED~~ ~~U56-11 CONNECTED TO (8X)~~ ~~SH'3 (8X) CONNECTED TO U37-8~~ FITS 89949400/89949500-A SH'2: CUT U6-5 FROM U25-3 U6-5 CONNECTED TO U6-7 U42-3 ISOLATED. U42-3 CONNECTED TO U24-2	LIZET	2.6.75		
A	CK 1242	RELEASED CLASS A	IONA	4.6.75		
B	CK 1299	REV 06 WAS CK 1193	IONA	29.9.75		
C	CK 1343	SH 4 U56-11 ISOLATED. U56-11 CONN. TO (8X). SH 3 (8X) CONN TO U37 8	RC	[illegible]	/	
D	CK 1401	TO FIT ECO 891: CONNECTION U1-2 (SH.2 C-3) / U29-13 (SH 9, A-3) REPLACES U43-2 (SH 9, D3) / U29-13. ASSY. 89935600-E.	Nony	31.12.75		
E	CK 1438	SH 9: P1-C1, P2-C2, P3-C3 DISCONNECTED U20 ADDED.	Nony	31.12.75		
F	CK 1473	SIGNAL NAMES	S.D	Jan. 76		
G	1584	CHANGED ACCORDING TO THIS ECO	IA	6/76		

NOTES

⚠1 JUMP CONFIGURATION (ON LOGIC SH'S 2,3 &9)

JUMPERS:	LCTT	ICL
	C4 WITH P4	C1 WITH I1
	C5 WITH P5	C2 WITH I2
	C6 WITH P6	C3 WITH I3
	C7 WITH P7	C4 WITH I4
		C5 WITH I5
		C6 WITH I6

⚠2 U20 IS USED ONLY FOR LCTT APPLICATION
U38-2 IS CONNECTED DIRECTLY TO U27-6 IN ICL APPLICATION

2. ALL RESISTORS ARE 0.25 W, ±5%

3 ▼DENOTES SIGNAL ORIGIN

4 ALL SIGNAL NAMES IN BRACKETS APPLY TO ICL

AW
AY 89985200 (LCTT)
AY 89935400 (ICL)
DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES
TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

ELBIT COMPUTERS LTD
A SUBSIDIARY OF CONTROL DATA

DWN	Nava Paladay	8/9/74
CHKD	[illegible]	Sept 74
ENGR	S. [illegible]	25/9/74
MFG	[illegible]	[illegible]
APPR	[illegible]	[illegible]
Q.A.		

FIRST USED ON: FA446-A, FA442-A

TITLE: DETAILED LOGIC DIAGRAM
UPPER DATA SECTION (LCTT & ICL)

CODE IDENT: C
DRAWING NO: 89767700
SCALE:
SHEET 1 OF 10

Figure 5-32. Upper Data Section Logic Diagram Reference Sheet

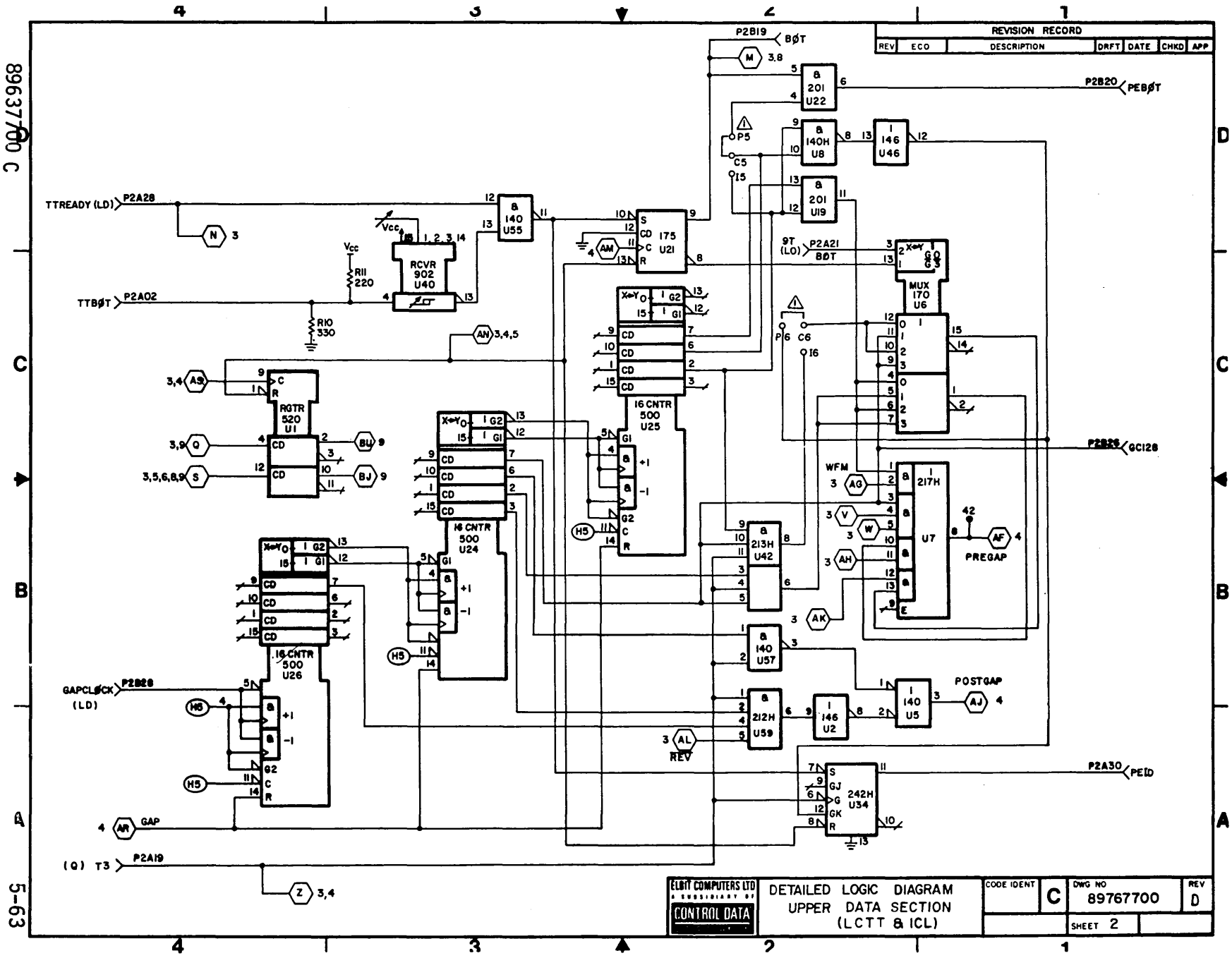


Figure 5-33. Upper Data Section - Gap Timing Generator Logic Diagram

MOTION FUNCTION EXECUTION (Logic Diagram 89767700, Sheets 3 and 4) Figures 5-38, and 5-39.

Motion Function Register

This module includes a four-bit Motion Function register (MØTCODE 7-10 U21), the logic that sets and clears the register and the logic that decodes the Motion Functions from the register. See Figures 5-34 and 5-35.

The register is set from A7, A8, A9 and A10 (at U3-4), -5, -12, -13).

The register is set by the rising of STRMF if the function is not Backward Motion at BØT, and not RWUNLD (REWIND UNLOAD).

$$U63 = STRMF \cdot B\O T \cdot \overline{(\overline{A7} \oplus AB) \cdot \overline{A9 \cdot A10}}$$

The register is reset by STOP+RES1+LOCKOUT+IDABORT.

The following Motion Functions are decoded from the Motion Function register:

WMØT	$= \overline{M7} \cdot \overline{M8} \cdot \overline{M9} \cdot \overline{M10}$	(U23-12)	WRITE MOTION
RMØT	$= \overline{M7} \cdot \overline{M8} \cdot \overline{M9} \cdot \overline{M10}$	(U39-12)	READ MOTION
WFM	$= \overline{M7} \cdot \overline{M8} \cdot \overline{M9} \cdot \overline{M10}$	(U23-10)	WRITE FILE MARK
RWLD	$= \overline{M7} \cdot \overline{M8} \cdot \overline{M9} \cdot \overline{M10}$	(U39-9)	REWIND LOAD
RWUNLD	$= \overline{M7} \cdot \overline{M8} \cdot \overline{M9} \cdot \overline{M10}$	(U39-14)	REWIND UNLOAD
FØR	$= \overline{M7} \oplus M8$	(U29-4)	FORWARD (TP 41)
REV	$= M7 \cdot M8$	(U61-8)	REVERSE
WREQUEST	$= M7 \cdot \overline{M8}$	(U55-3)	WRITE REQUEST
SFM	$= M8 \cdot M9 \cdot \overline{M10}$	(U57-6)	SEARCH FILE MARK
BA	= RMOT+SFF+RWLD	(U55-8)	Signal BA to Sheet 2
CØNTACT	= FOR+REV+RWLD	(U5-11)	CONTROLLER ACTIVE

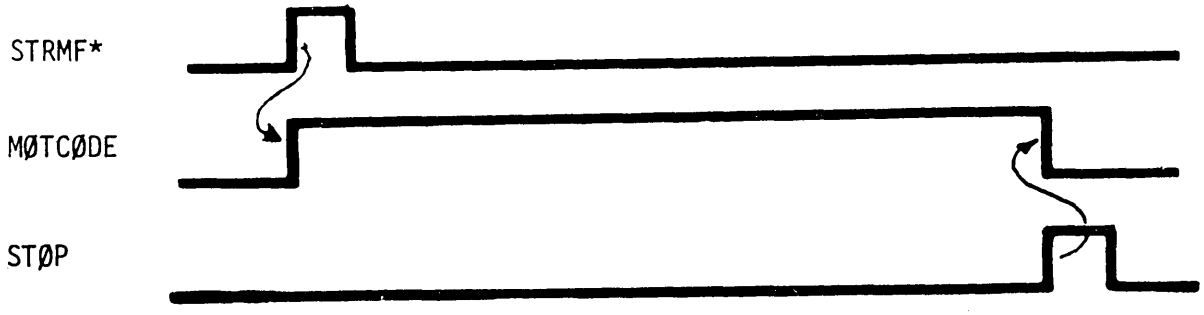


Figure 5-34. Motion Function Control

Motion Sequencer

This module includes the EØP FF and the logic that sets it, and the Motion Sequencer that indicates the START, STOP and EØG (END OF GAP).

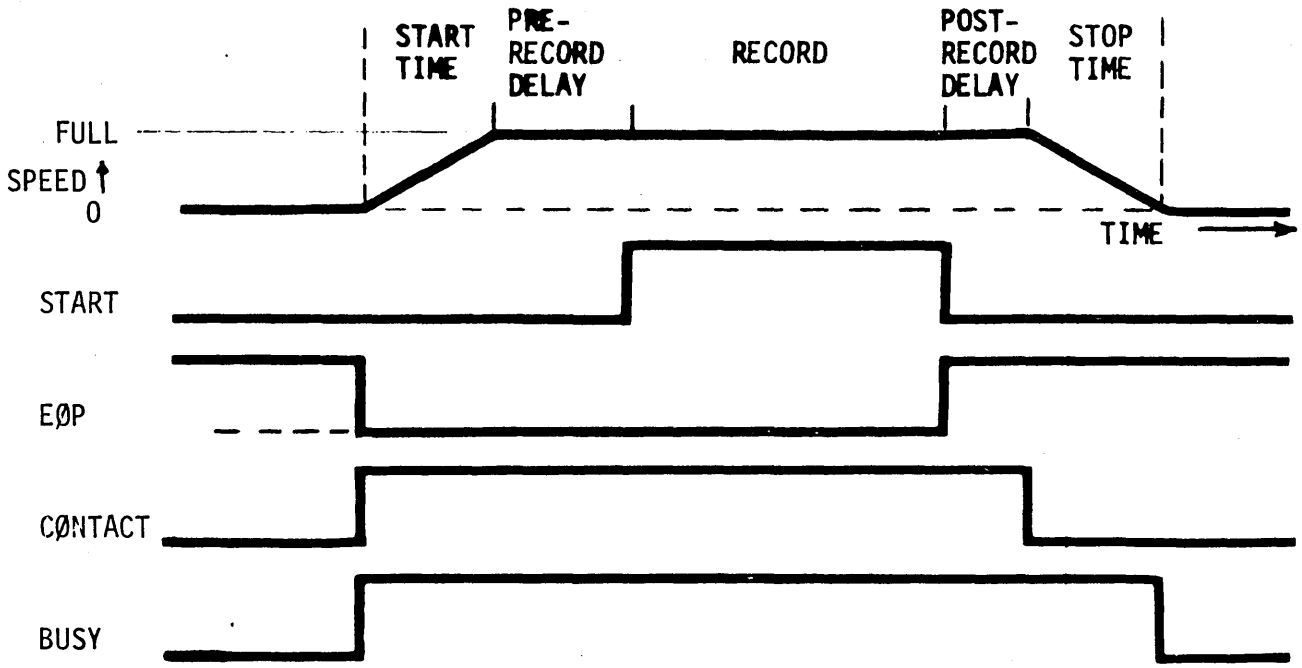


Figure 5-35. Motion Sequencer Control (Single Record Timing)

EØP-FF:

The EØP FF (U9-5) is cleared by:

U8-6) RES2 = RES1+STRMF

EØP is cleared by one of the following conditions (U26-6):

1. STRMF = STRMF·BØT·($\overline{A7}$ + A8)·A9·A10 (U24-3). This is a Reverse Motion Function from BØT, which is replied to, but no motion takes place.
2. Rising of SEØP
3. Rising of PEEØP
4. Rising of BØT if REV motion is in operation (U24-11).
5. Rising of TTREADY after finishing RWND operation (U18-5).

Motion Sequencer:

The Motion Sequencer consists of a five-bit shift register S0, S1, S2, S31, S32 (U3-9, U37) and a NONSTOP FF (U3-5). Only one of the FF's in the Sequencer is set at any time. First S0 is set, then S1, S2, S31 and S32 in turn.

S0 is set by the rising of STRMF if S2 is low. The "1" is shifted:

U4-8 = S0 PREGAP+S1·EOP+S2·POSTGAP+S31+S32)·T3

S1 clears S0, so that only one bit in the Sequencer can be set.

NONSTOP is set by STRMF if CONTACT is high. If NONSTOP is low, then the last state of the Sequencer S32, is the STOP signal (U2-8) that resets the CONTACT. If NONSTOP is high, then S32 presets S0 and resets the rest of the sequencer (U2-6).

Refer to the motion operations described in Figures 5-36 and 5-37.

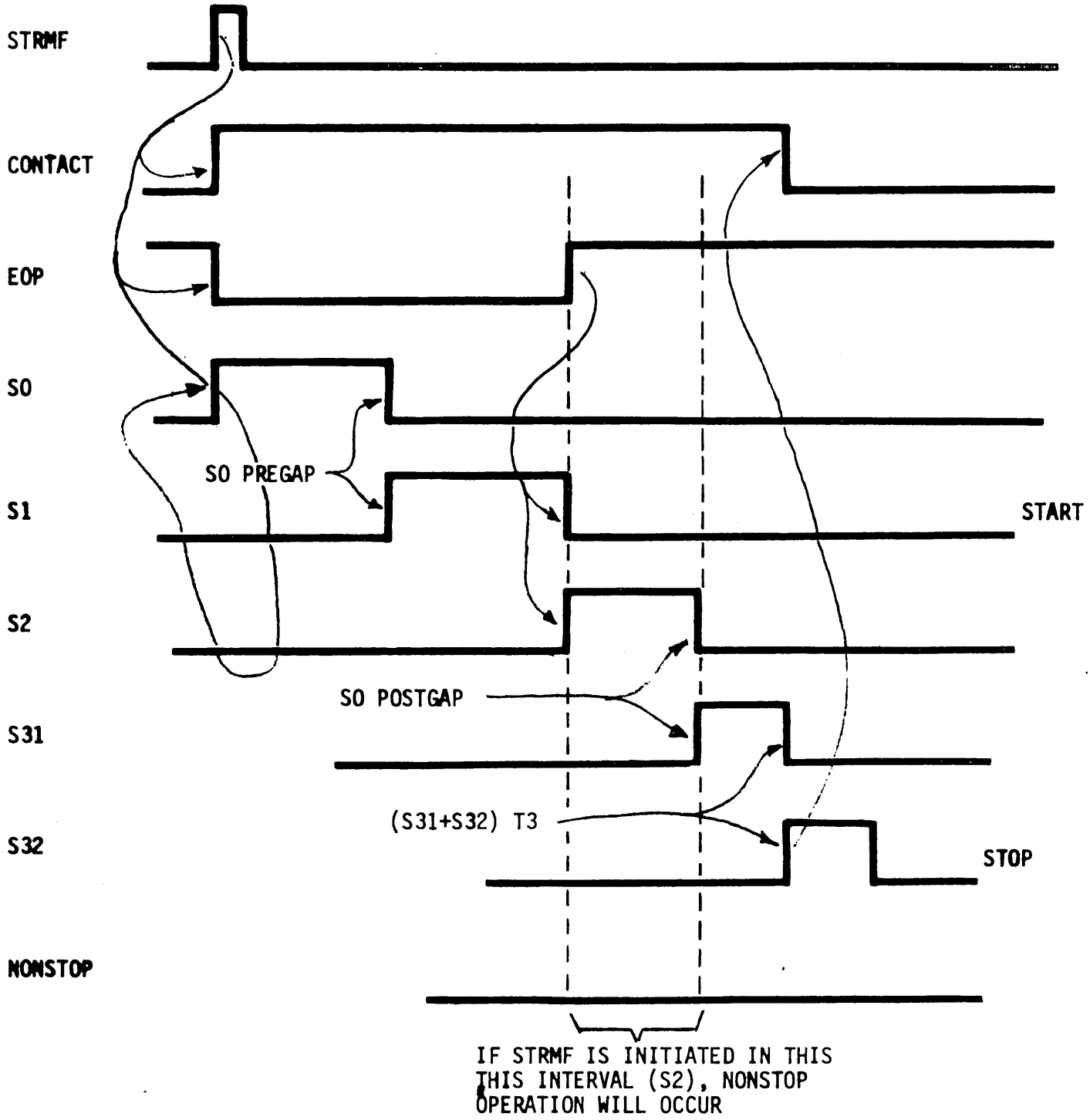


Figure 5-36. Normal Motion Operation

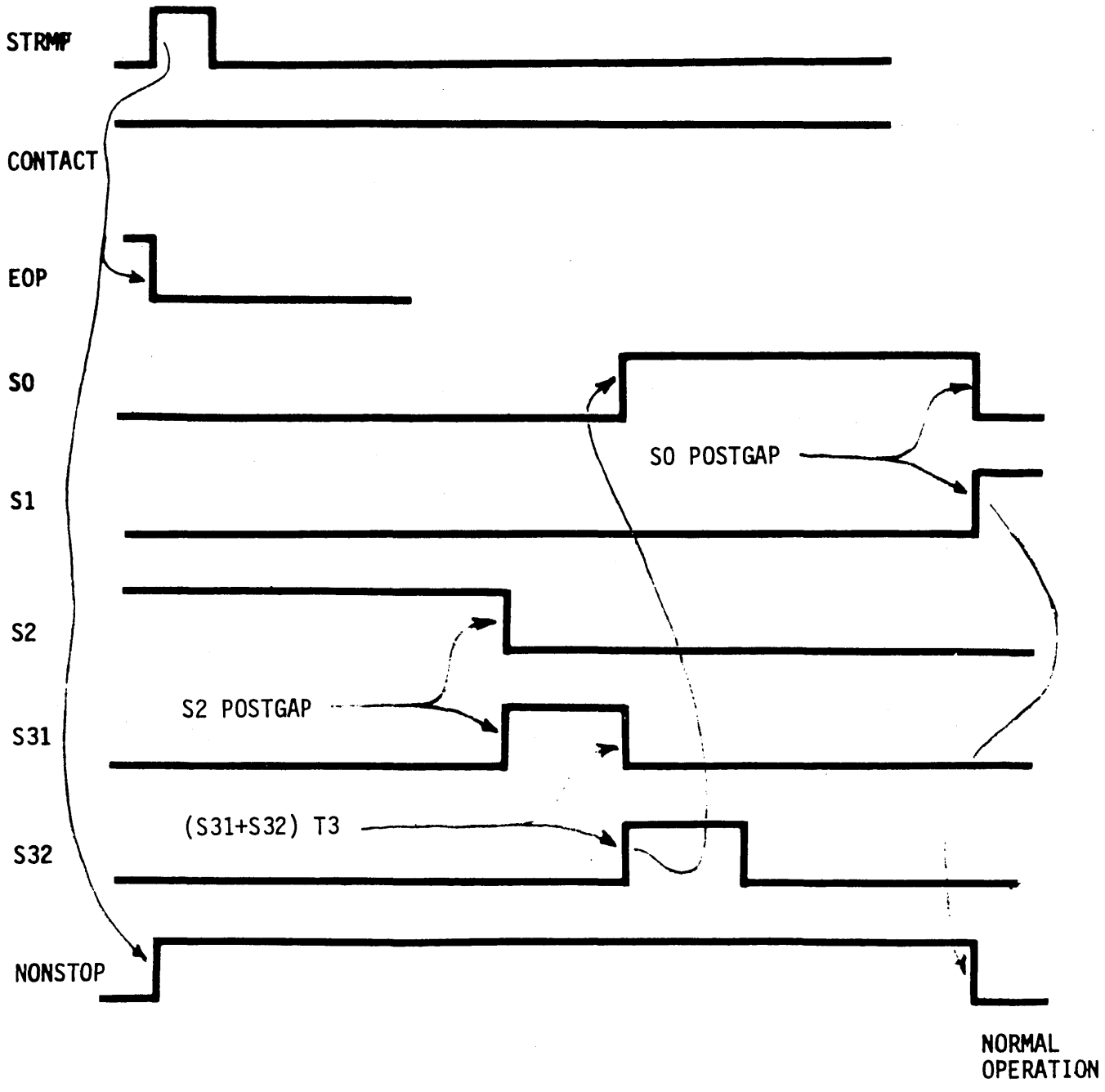


Figure 5-37. Non-Stop Motion Operation

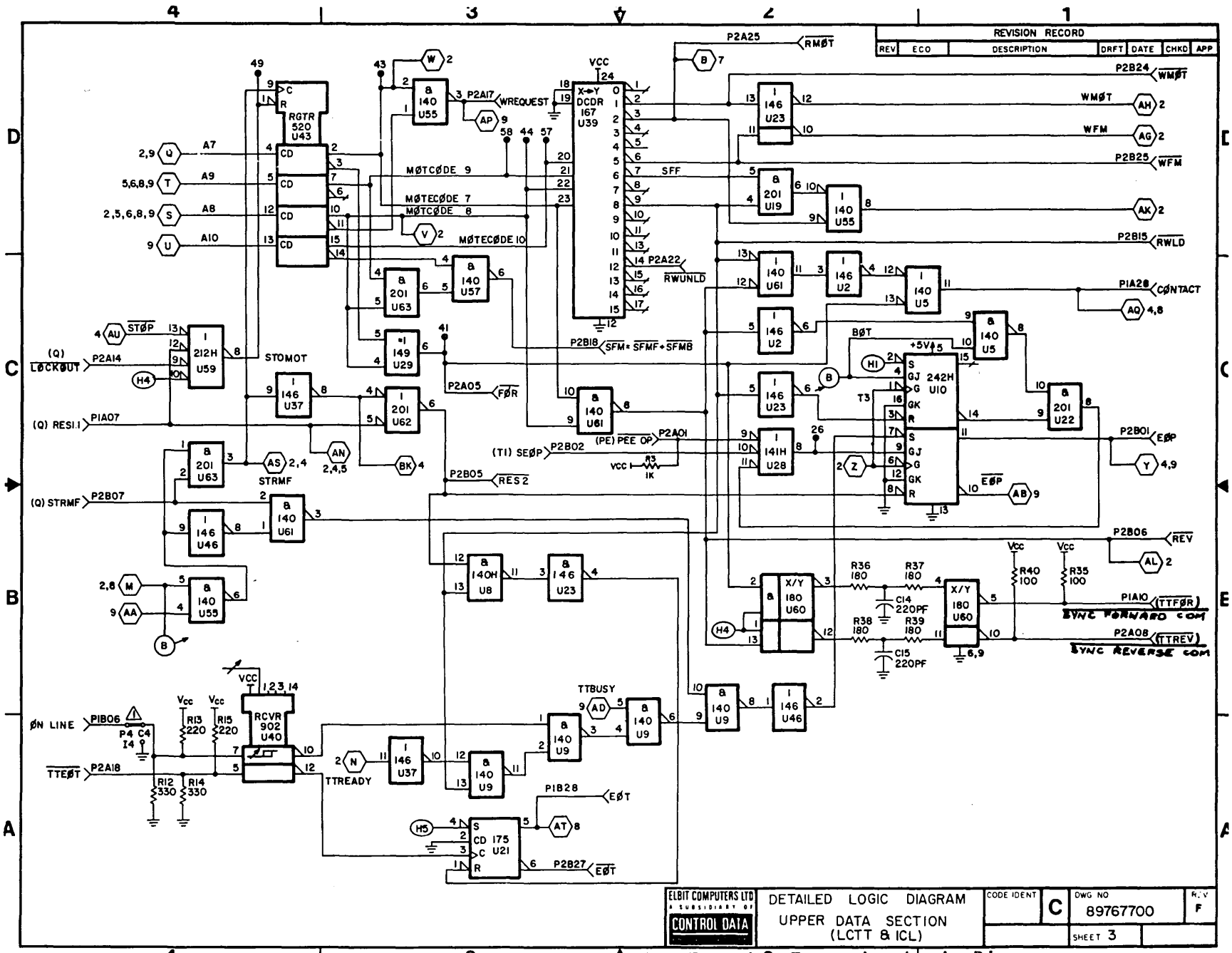


Figure 5-38. Upper Data Section - Motion Function Execution Logic Diagram

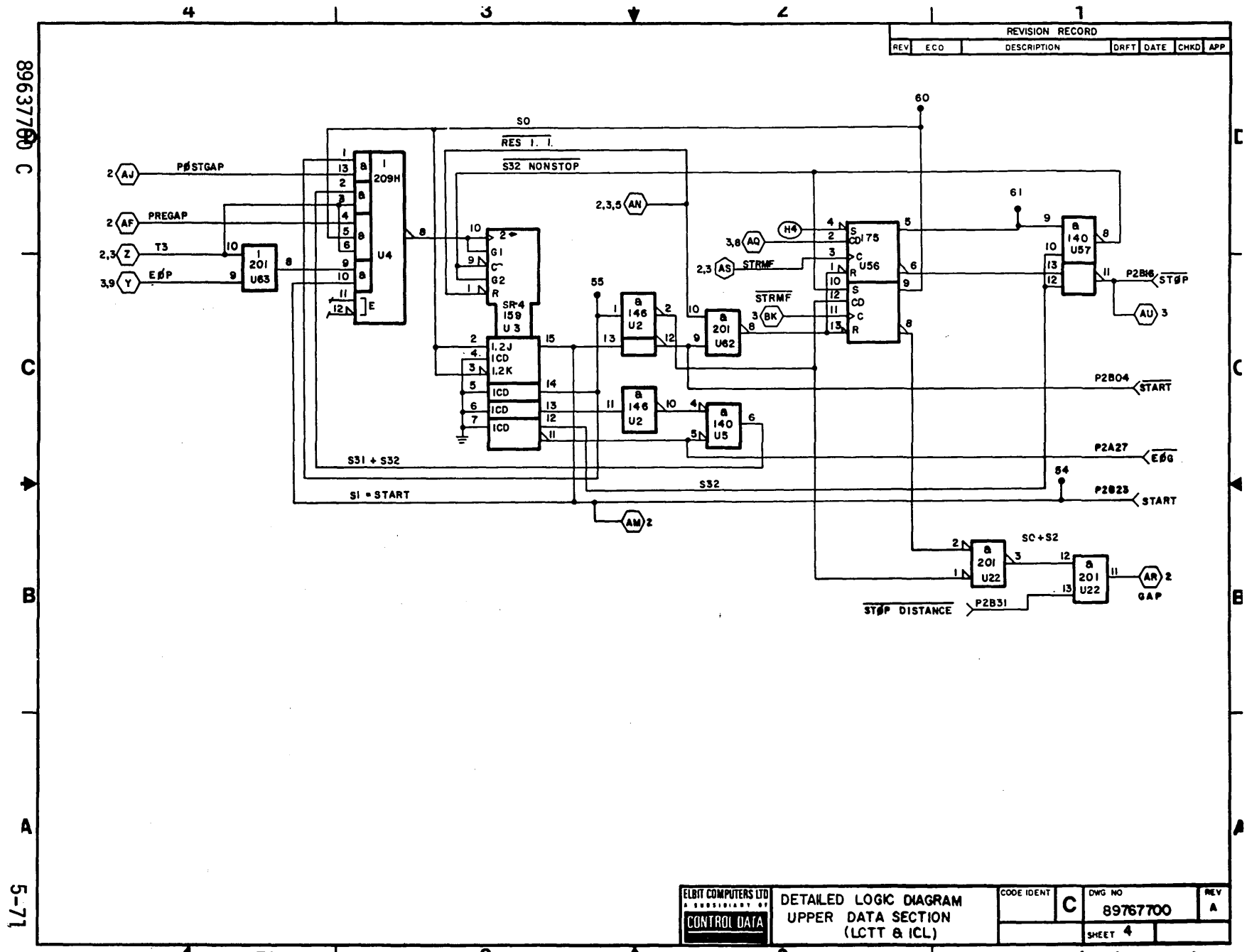


Figure 5-39. Upper Data Section - Motion Function Execution Logic Diagram (Cont'd)

UPPER DSA DATA PATH (Logic Diagram 89767700, Sheets 5 and 6) Figures 5-41 and 5-42.

$\overline{\text{STRBUF}}$ (Sheet 7 of Q -Channel, 89648500) initiates DSA transfer and presets CURAD (8-15 Sheet 5) to the contents of A(8-15). The A/Q DSA Selector (Sheet 5) is set by $\overline{\text{BUF I/O}}$ (Sheet 6) to DSA and $\overline{\text{LDLWA}}$ strobes (Sheet 5) the contents of DSA Data (8-15 Sheet 6 into LWA-1).

For every DSA transfer $\overline{\text{REQUEST}}$ enables the CURRENT ADDRESS on the DSA ADDR lines and the falling of $\overline{\text{CARCURADR}}$ increments the CURRENT ADDRESS. When writing, the data is transferred through DSA Data (8-15) and A/Q DSA Selector, to the Double Buffer.

When reading from the computer (the data is transferred from the tape) the Double Buffer and DSA WREN enables the data to pass to the computer memory.

LAST WORD is the comparator signal that indicates the detection of the last word. Refer to Figure 5-40.

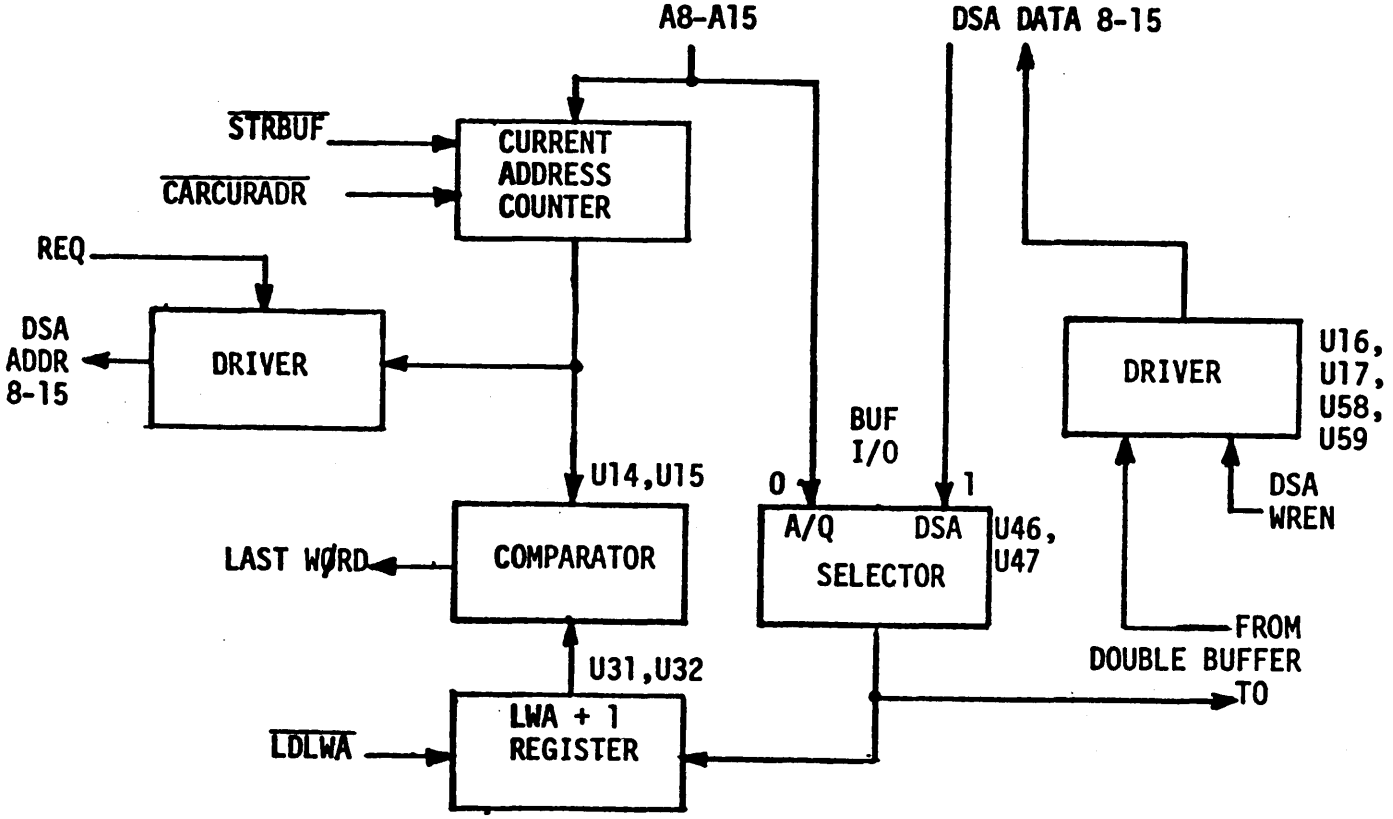


Figure 5-40. Upper DSA Data Path

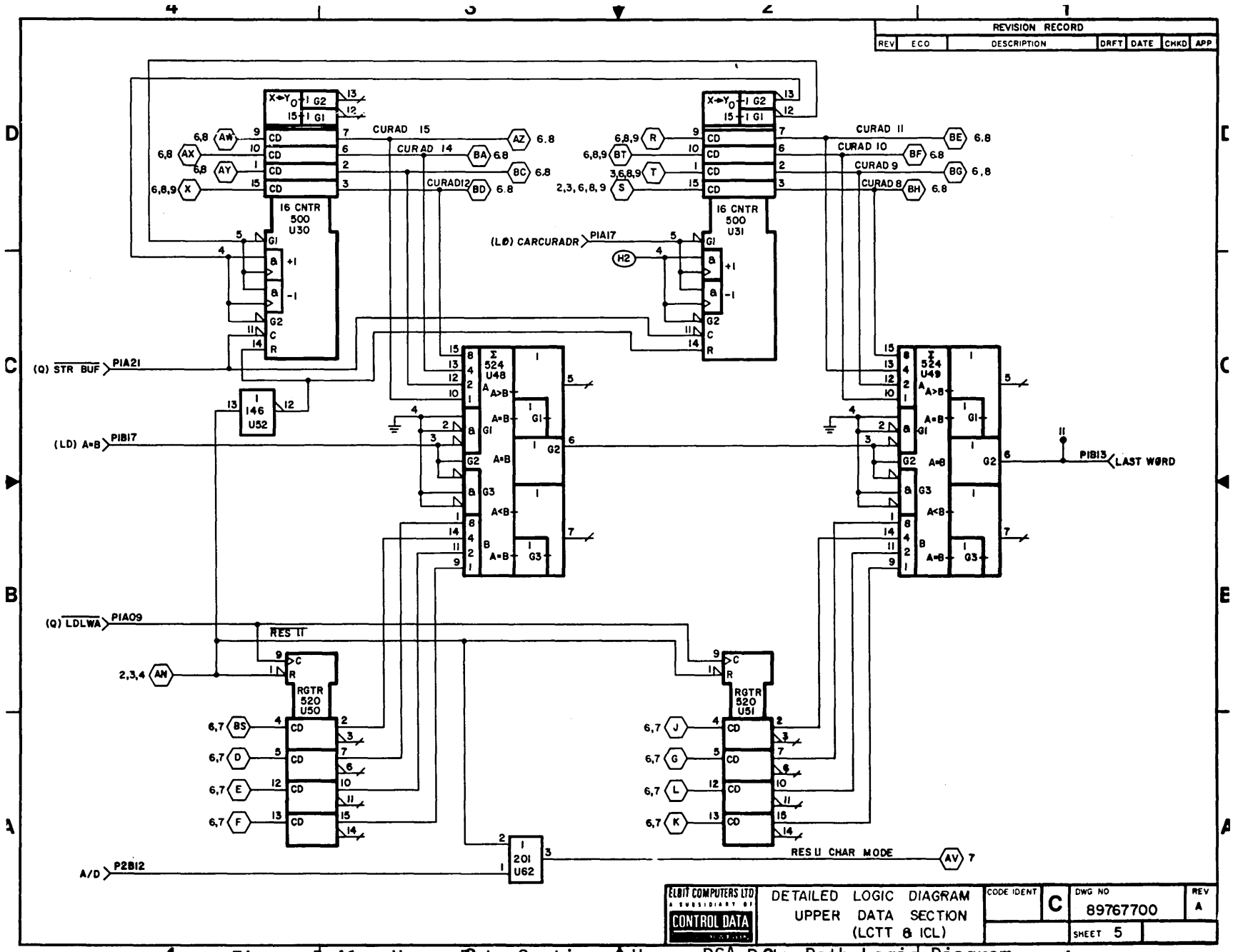


Figure 5-41. Upper Data Section Upper DSA Data Path Logic Diagram

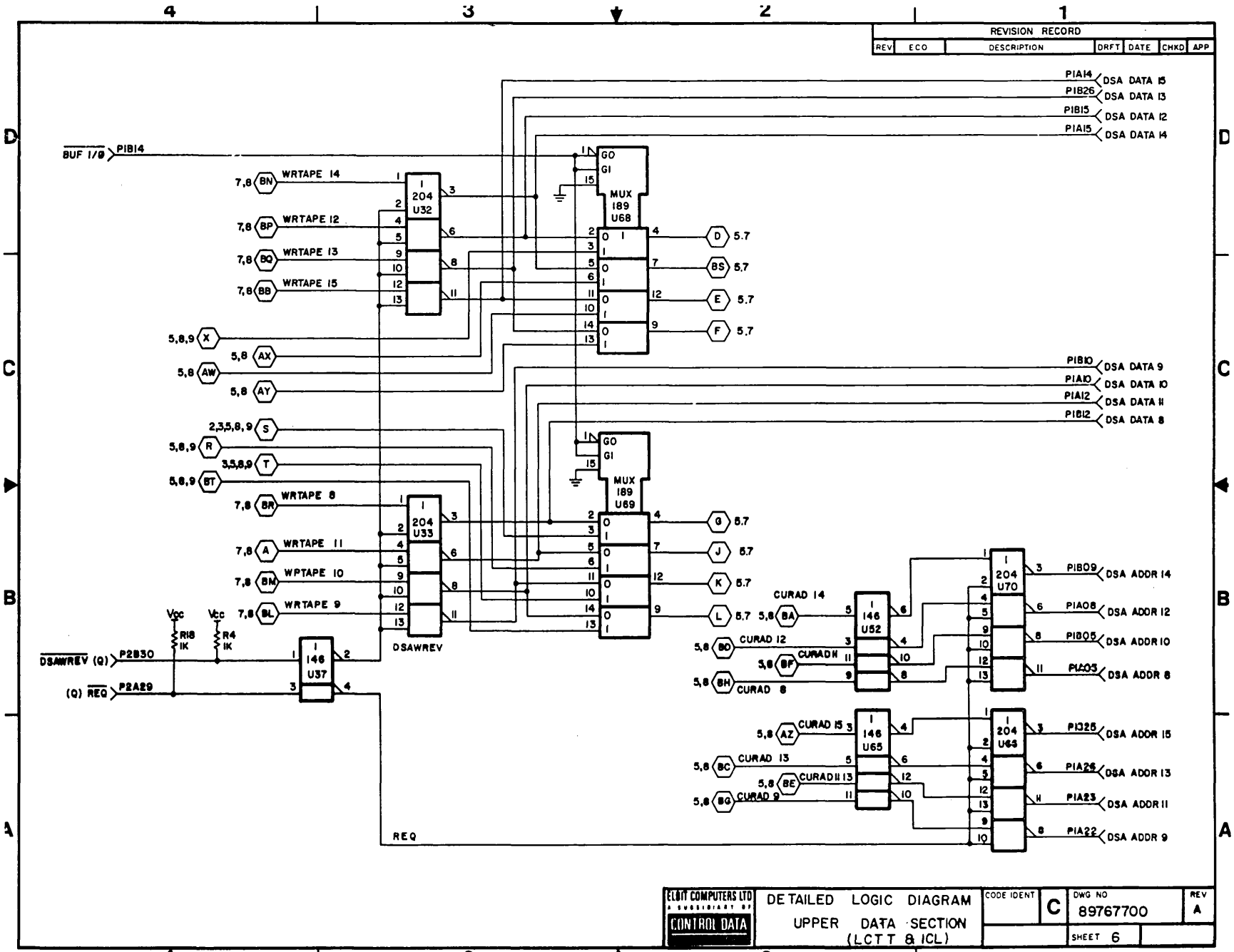


Figure 5-42. Upper Data Section - Upper DSA Data Path Logic Diagram (Cont'd)

UPPER A DATA PATH (Logic Diagram 89767700, Sheets 7 and 8) Figures 5-44 and 5-45.

For the block diagram of the Upper A Data Path, refer to Figure 5-43.

RDTAPE 0-7 signals from the tape transport are passed through multiplexer U72 (RDTAPE 0-3) and U71 (RDTAPE 4-7), when RMØT is low. With $\overline{\text{RMØT}}$ high, DATA IN 8-15 signals from the computer through U46, U47, are admitted. The outputs of this multiplexer (SELECTOR 1) are then supplied to Buffer 1 (U54, U53), which is controlled by the signal $\overline{\text{UPPXT}}$. Buffers 1 and 2 are cleared by $\overline{\text{RESET+CHAR MODE}}$. Buffer 2 (U36, U35) further passes the signal to produce WRTAPE 8-15 signals for the tape transport, when the $\overline{\text{TRANS}}$ is polled and RMØT is high. With $\overline{\text{RMØT}}$ low, the RDTAPE 0-7 data is available for transfer to Selector 2 (multiplexers U15, U16, U17 and U18), will only be accepted when the sum of SELA0 and SELA1 represents a binary 3. If both signals are binary, Current Address status is selected. If SELA0 and SELA1 signals are other than binary 3, only STATUS signals are passed through Selector 2. When SELA0 is high and SELA1 is low (binary 1), STATUS 1 is selected, and if SELA0 is low and SELA1 is high (binary 2), STATUS 2 is selected. These signals are NANDED through U64, U47 when enabled by $\overline{\text{ENA}}$ (High), to the A-bus to the computer.

When signals are received from the computer A-bus, they are admitted through U65, U67 to the other Upper Data Section circuitry.

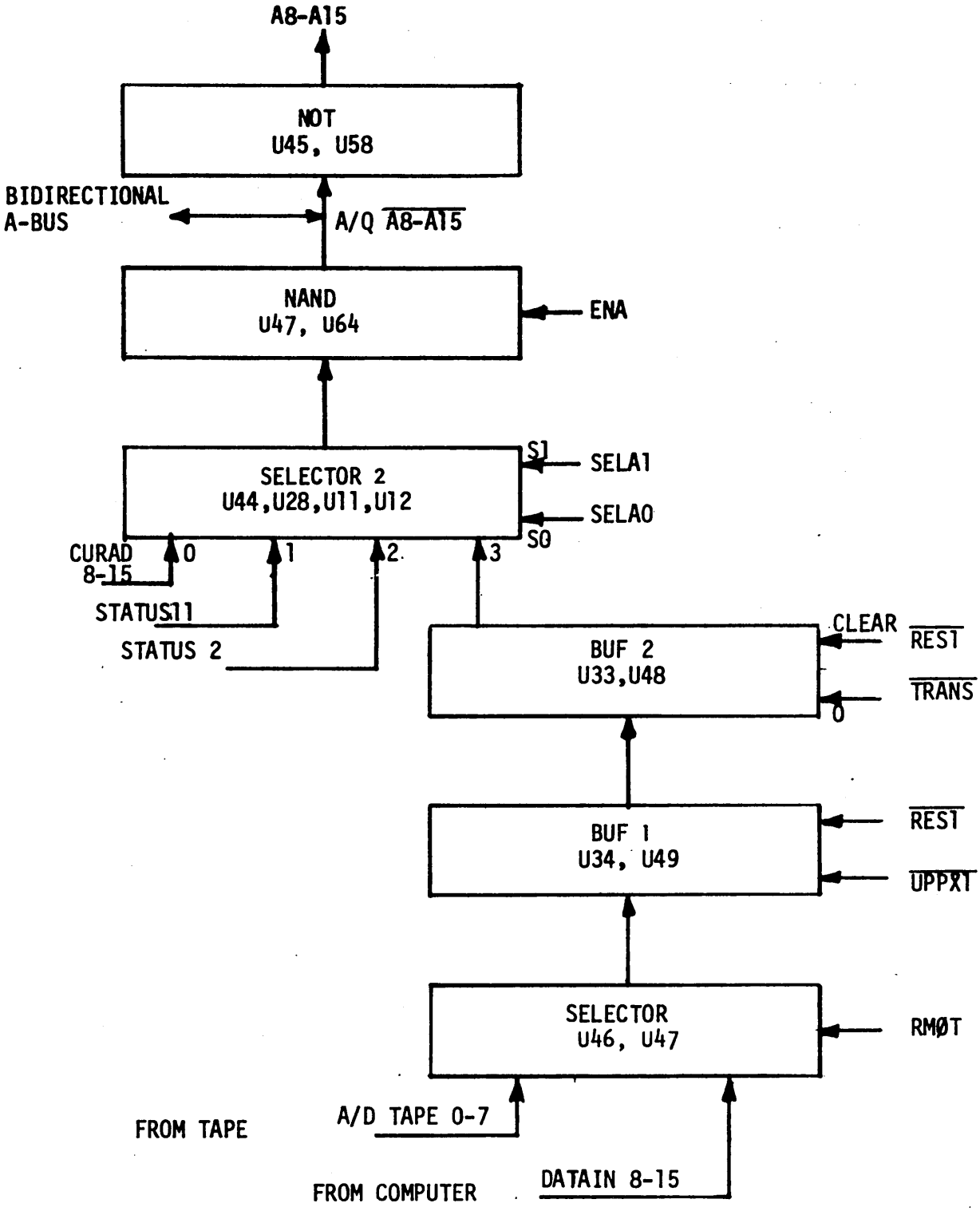


Figure 5-43. Upper A Data Path

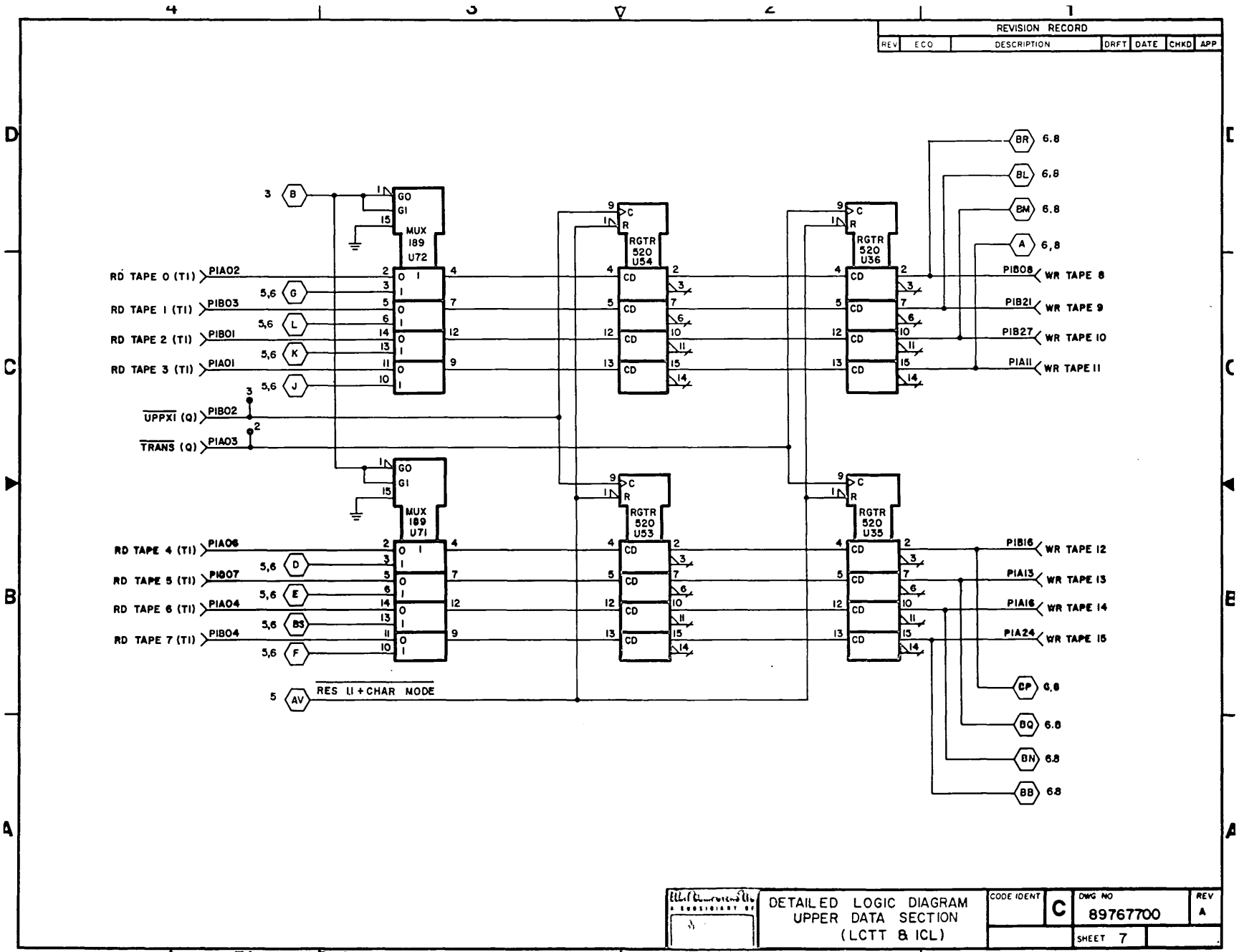


Figure 5-44. Upper Data Section Upper A Data Path Logic Diagram

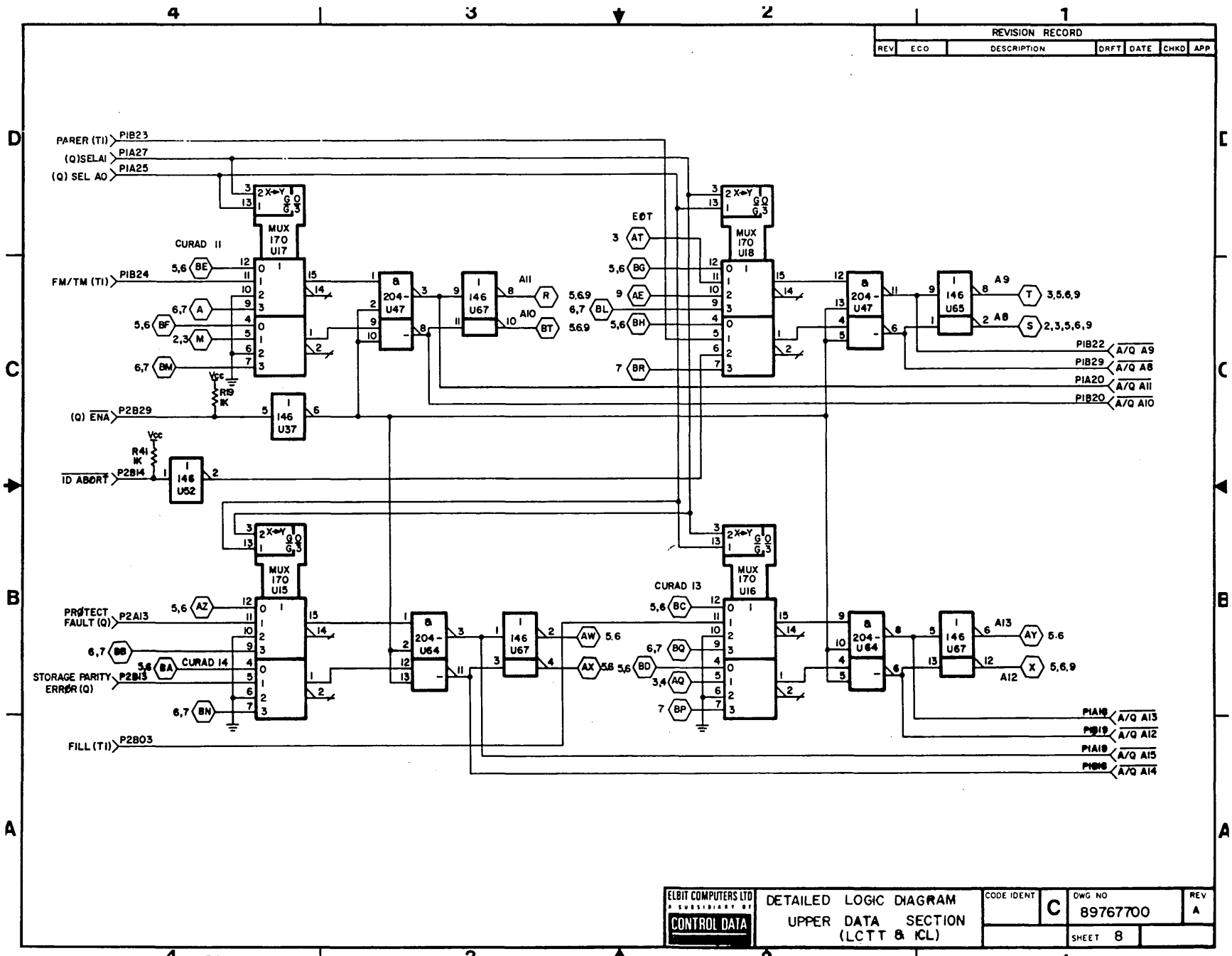


Figure 5-45. Upper Data Section - Upper A Data Path Logic Diagram (Cont'd)

UNIT SELECT CIRCUIT & LEGAL CONTROL FUNCTION DECODER (89767700, Sheet 9) Figure 5-47.

Unit Select Circuit

This module selects (or deselects) a unit and the number of the unit. A three-bit register U45 stores this information. A selector U44 selects the unit according to either the stored unit select number or the new one (see Figure 5-46).

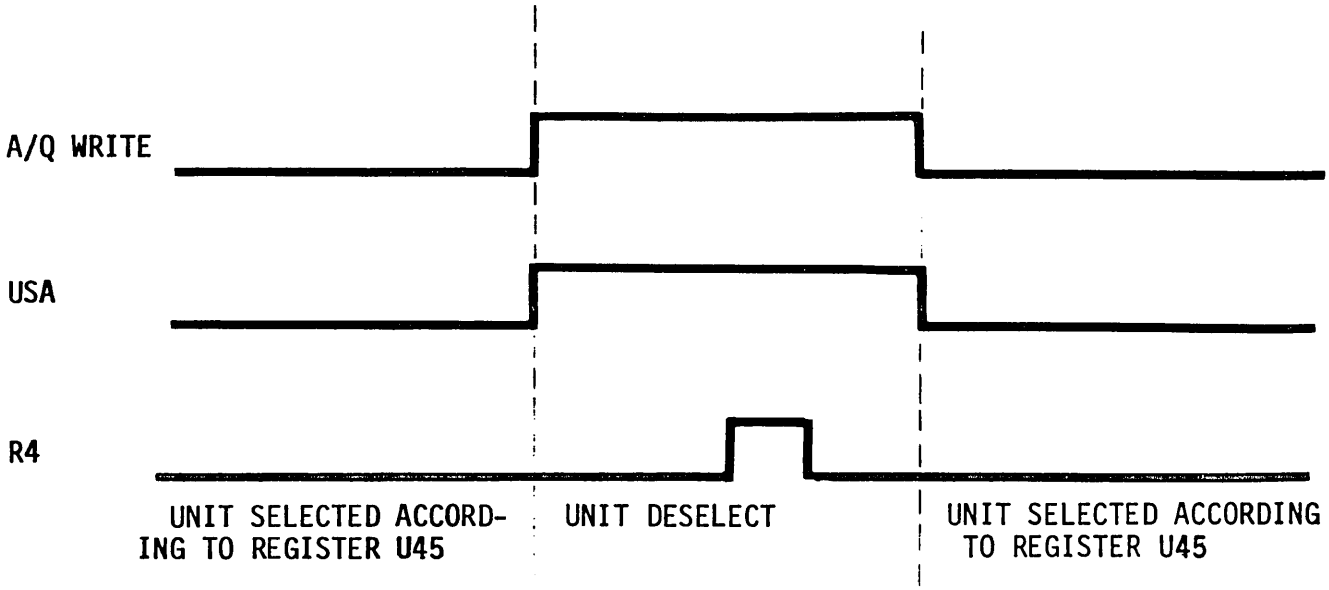


Figure 5-46. Unit Selection

If a UNIT SELECT instruction is sent to the controller, the status of the new unit (if it is changed) is checked, register U45 is bypassed if A10=1, in order to determine if it should be accepted (REPLY) or rejected (REJECT). If the UNIT SELECT is rejected, the previous unit is reconnected. The purpose of this feature is to reconnect a protected tape transport that has tried to disconnect.

Legal Control Function Decoder

This module computes the following combination functions:

The illegal combination of the motion functions are:

(U11-8) LEGMF = A7·A10·A8+$\overline{A7}$·$\overline{A8}$·$\overline{A10}$

The illegal combinations of the eight most significant bits of the Unit Select Code are:

(U12-8) ILLUSCODE = A9+A10·A11

The following function determines the Non-Stop Conditions:

NSCOND = LEGMF·$\overline{A10}$·($\overline{A7}$ ⊕ MØTCODE7) ($\overline{A8}$ ⊕ MOTCODE8)

The Control Function will be legal if LEGCF (LEGAL CØNTRØL FUNCTIØN)

(U41-12) LEGCF = LEGMF·(A10+A8+FILE PROTECT)·(BUSY+NSCØND·EØP)

Explanation:

For a Control Function to be legal all three conditions must be satisfied:

1. The Motion Function Code must be legal (only 8 bits out of 16 are legal).
2. The Motion must not be a Write Function (A8+A10) or the File Protect ring must be removed from the tape.
3. The transport must be Not-Busy or if Non-Stop Motion conditions exist, then EØP must be set.

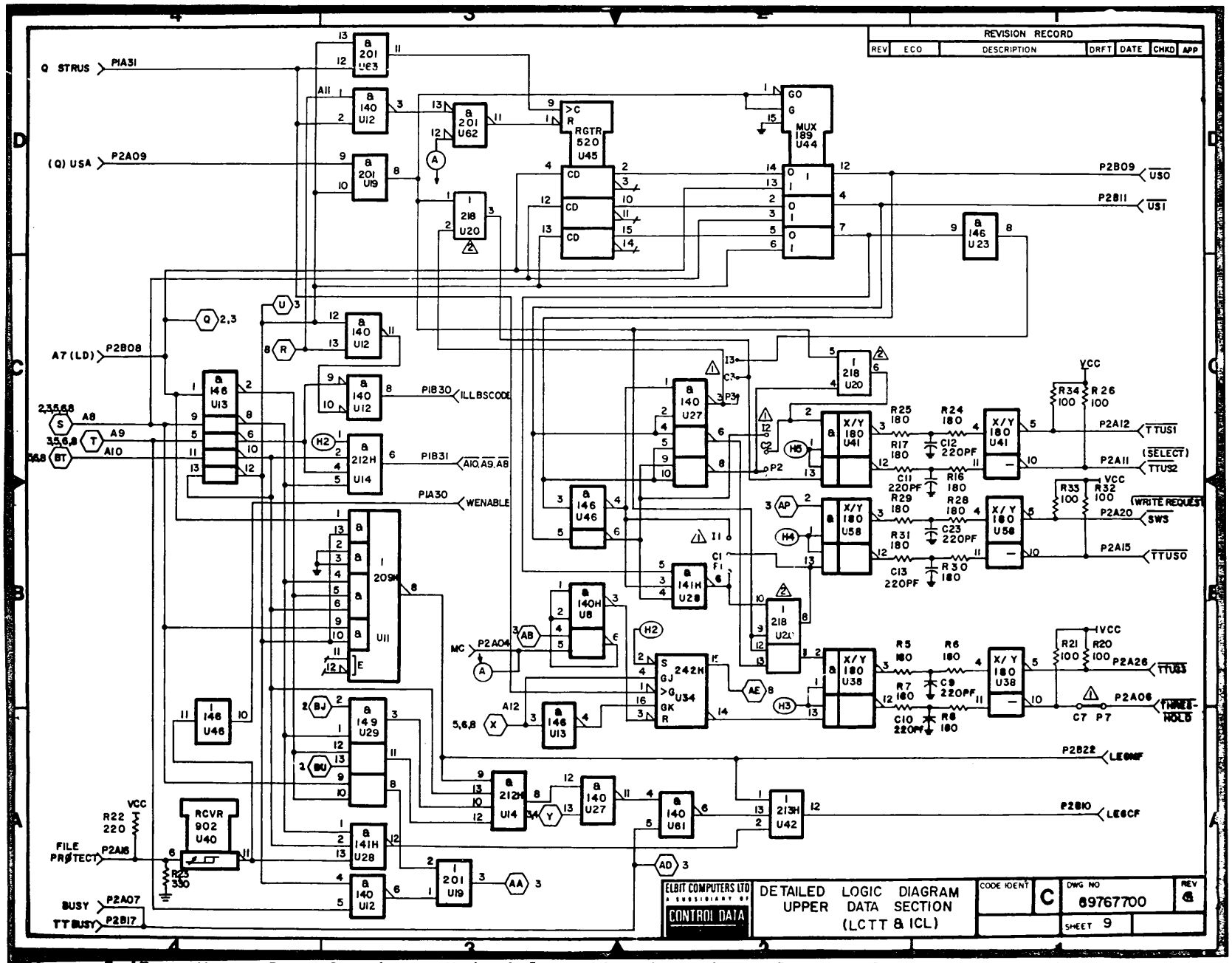


Figure 5-47. Upper Data Section - Unit Select Circuit and Legal Control Function Decoder Logic Diagram

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

CONTINUED FROM PAG. 1

OFF-SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION							
		2	3	4	5	6	7	8	9
BC	CURAD13				▼3D	2A		2B	
BD	CURAD12				▼3D	2B		2B	
BE	CURAD 11				▼1D	2B		4C	
BF	CURAD 10				▼1D	2B		4C	
BG	CURAD 9				▼1D	2A		2C	
BH	CURAD 8				▼1D	2B		2C	
BJ		▼3C							4B
BK	STRAP		3C	2C					
BL	WRTAPE 9					4B	▼1D	3C	
BM	WRTAPE 10					4B	▼1D	4C	
BN	WRTAPE 14					4D	▼1A	4B	
BP	WRTAPE 12					4D	▼1B	2B	
BQ	WRTAPE 13					4C	▼1A	2B	
BR	WRTAPE 8					4B	▼1D	2C	
BS					4A	▼2C	4B		
BT					2D	4C		▼3C	4C
BU		▼3C							3A

CONTROL DATA	DETAILED LOGIC DIAGRAM	CODE IDENT C	DWG NO 89767700	REV D
	UPPER DATA SECTION(LCTT&ICL)		SHEET 10 OF 10	

Figure 5-47a. Upper Data Section Logic Diagram Reference Sheet

TAPE INTERFACE PWA (Logic Diagram 89768600)

CRC GENERATOR/DETECTOR (Logic Diagram 89768600, Sheet 2) Figure 5-48 and 5-49.

This module consists of the Circular Redundance Check Character (CRCC) Register. It is operational only in nine track, 800 bpi operation.

The CRCC has the following properties:

1. It can be an all zeros character, therefore no RDS is transmitted from MTT.
2. Its value is such that the LRCC always has odd parity (therefore the LRCC can never be all zeros).
3. It has odd parity when there are even number of data characters, or even parity for an odd number of data characters.
4. When writing, 1 frame of 00_{16} on tape, the CRCC is EB_{16}.

TABLE 5-5. DATA/CRCC RELATIONSHIP

SIGNAL	TRACKS								
	7	6	5	4	3	2	1	0	P
DATA	0	0	0	0	0	0	0	0	1
CRCC	1	1	1	0	1	0	1	1	1

The module also contains CRC-ERR FF and the CRC Strobe logic as described:

Strobe CRC (U39-11 = WDS+RMØT·2NDSP·(RDS+MISCRC)

2NDSP = space between CRCC and LRCC

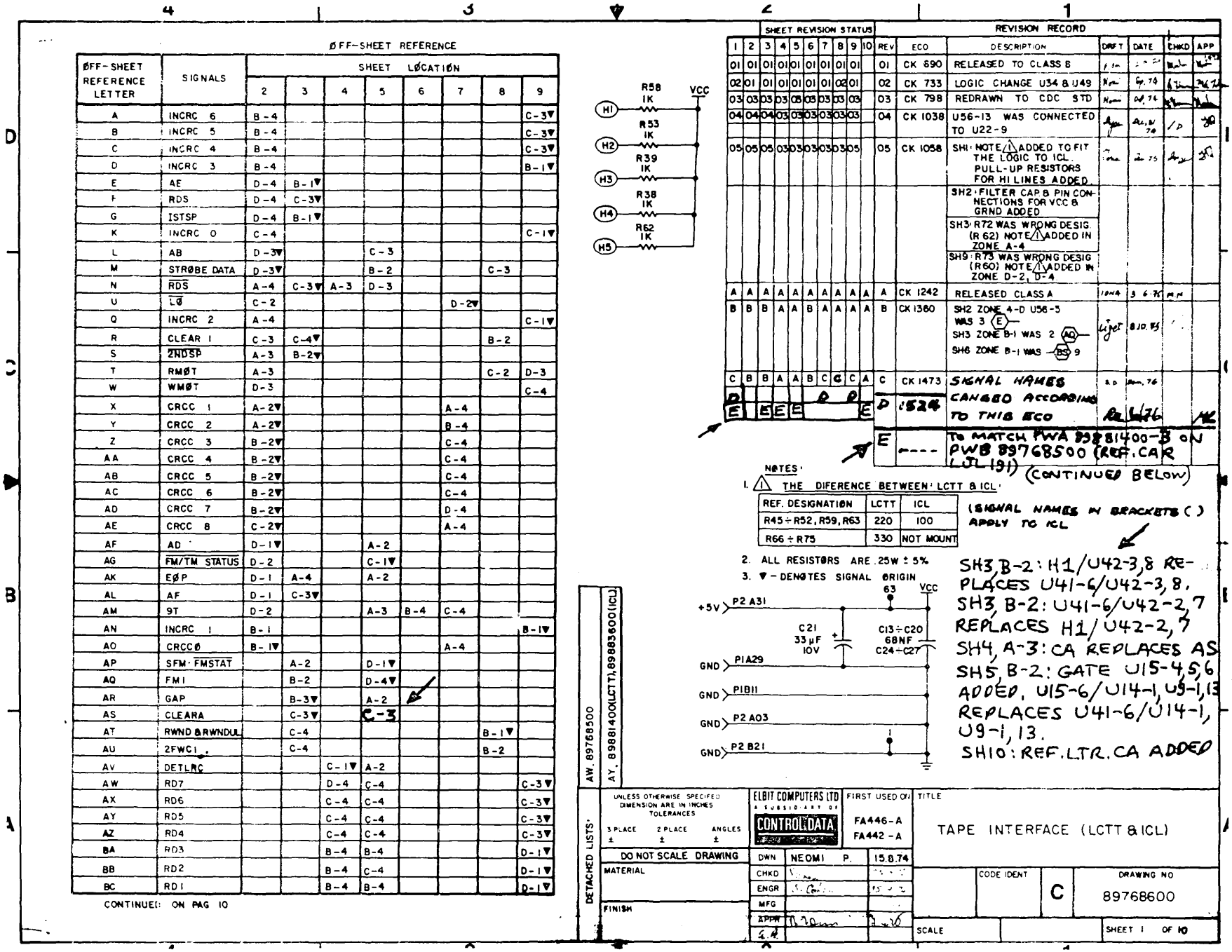
$\overline{\text{MISCRC}}$ = pseudo RDS, when CRCC is all zeros.

$\overline{\text{CRC ERR CØNDITIØN}}$ = (U58-12) = U55-10·9T·($\overline{\text{WMØT+BKSP) FM STATUS}}$

During WMØT and Backspace, U55-10 is not looked at. During FM STAT a CRC ERR is forced.

The CRC register is toggled at the falling edge of WDS during Write operation and the falling edge of RDS during Read operation.

The CRC ERR FF U22-5 is clocked at EØP and preset by $\overline{\text{RES2·RWLD+RWUNLD}}$.



ØFF-SHEET REFERENCE

ØFF-SHEET REFERENCE LETTER	SIGNALS	SHEET LØCATIØN 2	3	4	5	6	7	8	9
A	INCRC 6	B-4							C-3▼
B	INCRC 5	B-4							C-3▼
C	INCRC 4	B-4							C-3▼
D	INCRC 3	B-4							B-1▼
E	AE	D-4	B-1▼						
F	RDS	D-4	C-3▼						
G	ISTSP	D-4	B-1▼						
K	INCRC 0	C-4							C-1▼
L	AB	D-3▼			C-3				
M	STRØBE DATA	D-3▼			B-2			C-3	
N	$\overline{RDS}$	A-4	C-3▼	A-3	D-3				
U	$\overline{LØ}$	C-2					D-2▼		
Q	INCRC 2	A-4							C-1▼
R	CLEAR 1	C-3	C-4▼					B-2	
S	$\overline{2NDSP}$	A-3	B-2▼						
T	RMØT	A-3						C-2	D-3
W	WMØT	D-3							C-4
X	CRCC 1	A-2▼					A-4		
Y	CRCC 2	A-2▼					B-4		
Z	CRCC 3	B-2▼					C-4		
AA	CRCC 4	B-2▼					C-4		
AB	CRCC 5	B-2▼					C-4		
AC	CRCC 6	B-2▼					C-4		
AD	CRCC 7	B-2▼					D-4		
AE	CRCC 8	C-2▼					A-4		
AF	AD	D-1▼			A-2				
AG	FM/TM STATUS	D-2			C-1▼				
AK	EØP	D-1	A-4		A-2				
AL	AF	D-1	C-3▼						
AM	9T	D-2			A-3	B-4	C-4		
AN	INCRC 1	B-1							B-1▼
AO	CRCCØ	B-1▼					A-4		
AP	SFM·FMSTAT		A-2		D-1▼				
AQ	FM1		B-2		D-4▼				
AR	GAP		B-3▼		A-2				
AS	CLEARA		C-3▼		C-3				
AT	RWND&RWNDUL		C-4					B-1▼	
AU	2FWC1		C-4					B-2	
AV	DETLRC			C-1▼	A-2				
AW	RD7			D-4	C-4				C-3▼
AX	RD6			C-4	C-4				C-3▼
AY	RD5			C-4	C-4				C-3▼
AZ	RD4			C-4	C-4				C-3▼
BA	RD3			B-4	B-4				D-1▼
BB	RD2			B-4	C-4				D-1▼
BC	RD1			B-4	B-4				D-1▼

CONTINUED ON PAG 10

R58 1K VCC
H1 R53 1K
H2 R39 1K
H3 R38 1K
H4 R62 1K
H5

SHEET REVISION STATUS

1	2	3	4	5	6	7	8	9	10	REV
01	01	01	01	01	01	01	01	01		01
02	01	01	01	01	01	01	02	01		02
03	03	03	03	03	03	03	03	03		03
04	04	04	03	03	03	03	03	03		04
05	05	05	03	03	03	03	03	05		05
A	A	A	A	A	A	A	A	A	A	A
B	B	B	A	A	B	A	A	A	A	B
C	B	B	A	A	B	C	C	C	A	C
D										D
E	E	E	E						E	E

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
01	CK 690	RELEASED TO CLASS B				
02	CK 733	LOGIC CHANGE U34 & U49				
03	CK 798	REDRAWN TO CDC STD				
04	CK 1038	U56-13 WAS CONNECTED TO U22-9				
05	CK 1058	SH1: NOTE 1 ADDED TO FIT THE LOGIC TO ICL. PULL-UP RESISTORS FOR HI LINES ADDED				
		SH2: FILTER CAP B PIN CONNECTIONS FOR VCC & GRND ADDED				
		SH3: R72 WAS WRONG DESIG (R 62) NOTE 1 ADDED IN ZONE A-4				
		SH9: R73 WAS WRONG DESIG (R60) NOTE 1 ADDED IN ZONE D-2, D-4				
A	CK 1242	RELEASED CLASS A				
B	CK 1360	SH2 ZONE 4-D U56-5 WAS 3 (E); SH3 ZONE B-1 WAS 2 (AQ); SH6 ZONE B-1 WAS (BS) 9				
C	CK 1473	SIGNAL NAMES CANGED ACCORDING TO THIS ECO				
D	1524					
E	----	TO MATCH PWA 89881400-B ON PWB 89768500 (REF. CAR LJL 191) (CONTINUED BELOW)				

NOTES:
1. ⚠1 THE DIFERENCE BETWEEN LCTT & ICL:

REF. DESIGNATION	LCTT	ICL
R45÷R52, R59, R63	220	100
R66÷R75	330	NOT MOUNT

(SIGNAL NAMES IN BRACKETS ( ) APPLY TO ICL

2. ALL RESISTØRS ARE .25W ± 5%
3. ▼ - DENØTES SIGNAL ØRIGIN

+5V P2 A31
63 VCC
C21 33µF 10V
C13÷C20 68NF C24÷C27
GND P1A29
GND P1B11
GND P2 A03
GND P2 B21

SH3, B-2: H1/U42-3,8 REPLACES U41-6/U42-3,8.
SH3, B-2: U41-6/U42-2,7 REPLACES H1/U42-2,7
SH4, A-3: CA REPLACES AS
SH5, B-2: GATE U15-4,5,6 ADDED, U15-6/U14-1, U9-1,13 REPLACES U41-6/U14-1, U9-1,13.
SH10: REF.LTR.CA ADDED

AW. 89768500
AY. 89881400(LCTT), 89883600(ICL)

DETACHED LISTS:

UNLESS OTHERWISE SPECIFIED DIMENSION ARE IN INCHES TOLERANCES
3 PLACE ± 2 PLACE ± ANGLES ±
DO NOT SCALE DRAWING
MATERIAL
FINISH

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA
FIRST USED ON: FA446-A FA442-A

DWN	NEOMI P.	15.8.74
CHKD		
ENGR		
MFG		
APPR		
Q.A.		

TITLE: TAPE INTERFACE (LCTT & ICL)

CODE IDENT: C
DRAWING NO: 89768600
SCALE
SHEET 1 OF 10

Figure 5-48. Tape Interface Logic Diagram Reference Sheet

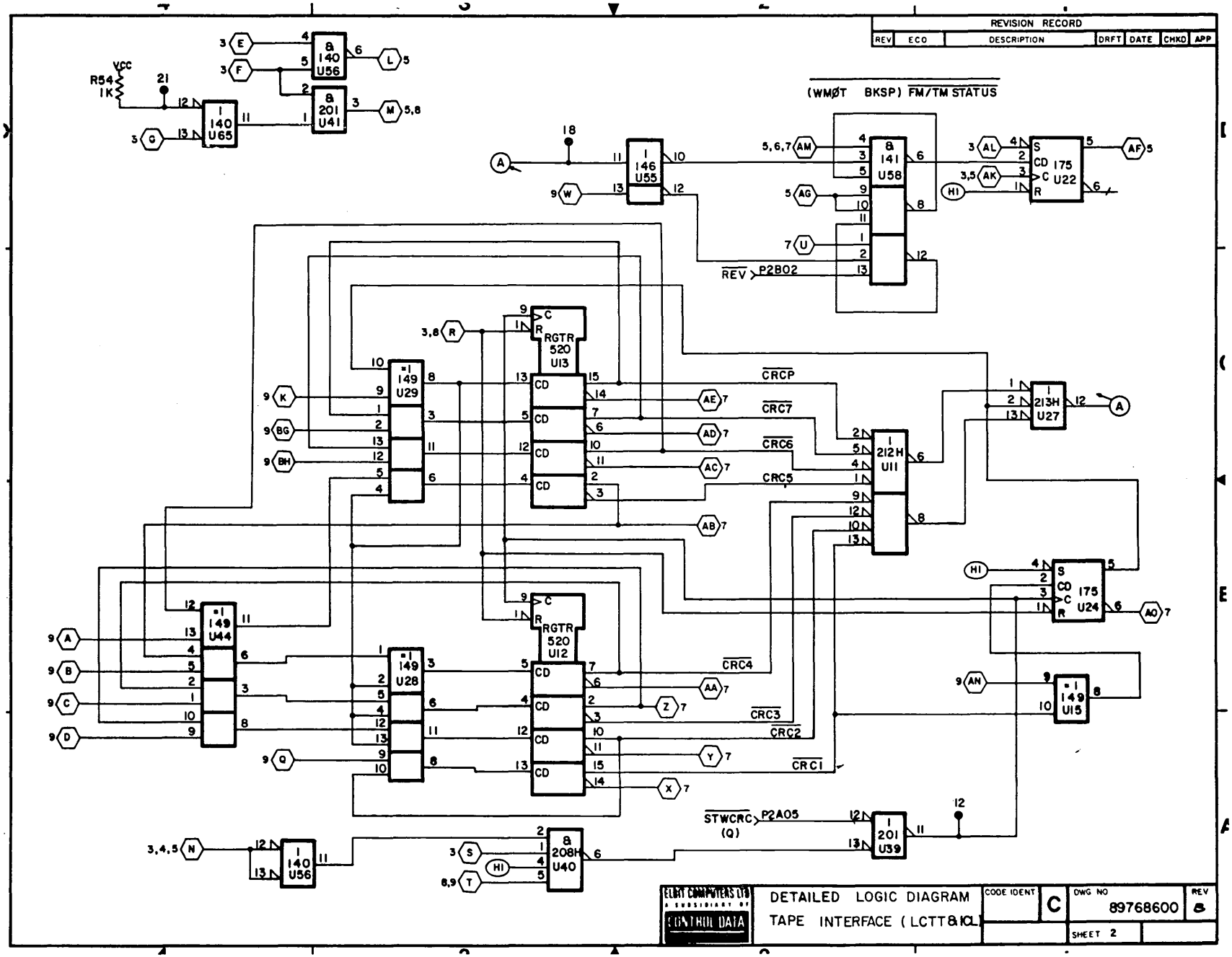


Figure 5-49. Tape Interface - CRC Generator Detector Logic Diagram

DATA STROBE/EØR DETECTOR (Logic Diagram 89768600, Sheet 3) Figure 5-52.

U7 is a filter that rejects pulses of width less than 250 uSecs. It clips 250-500 uSecs from the beginning of $\overline{\text{TTRDS}}$. Refer to Figure 5-50.

U24-9 and U25 are the End Of Record Counter which is used during Read Motion and during Write Motion in Read After Write Mode. A 2FWC counts it up and RDS resets the counter. The counter is blocked if it reads 32. MISCAR (U27-6) and MISCR (U40-8) are decoded from the counter (refer to Figure 5-51).

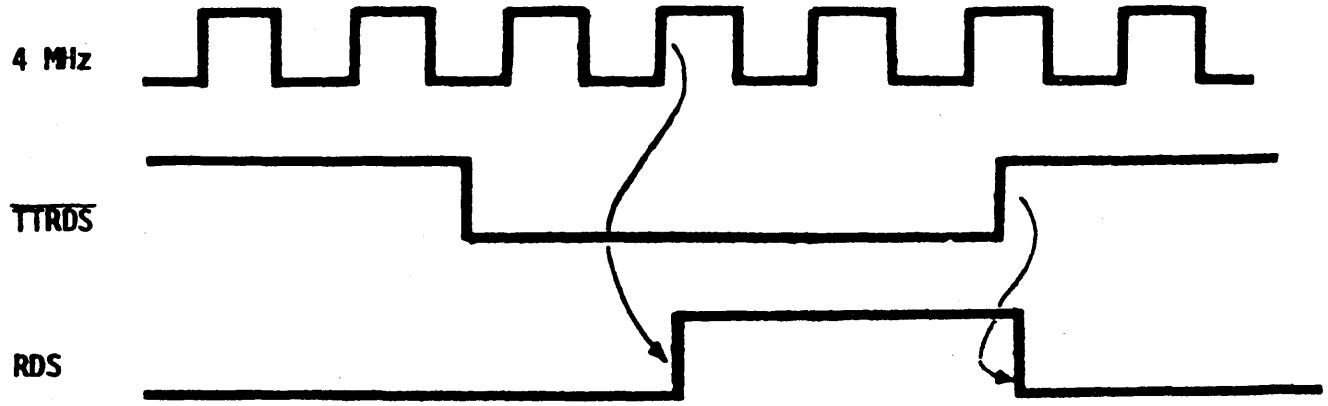


Figure 5-50. Data Strobe Generation

This counter detects gaps, by looking for 16 missing READ DATA strobes. It detects the space (1STSP) between Data Area and CRCC (nine track) or Data Area and LRCC (seven track).

In addition it generates a pseudo-RDS (MISCRC) in the cases where the CRCC is all zeros (Null Character = 000000).

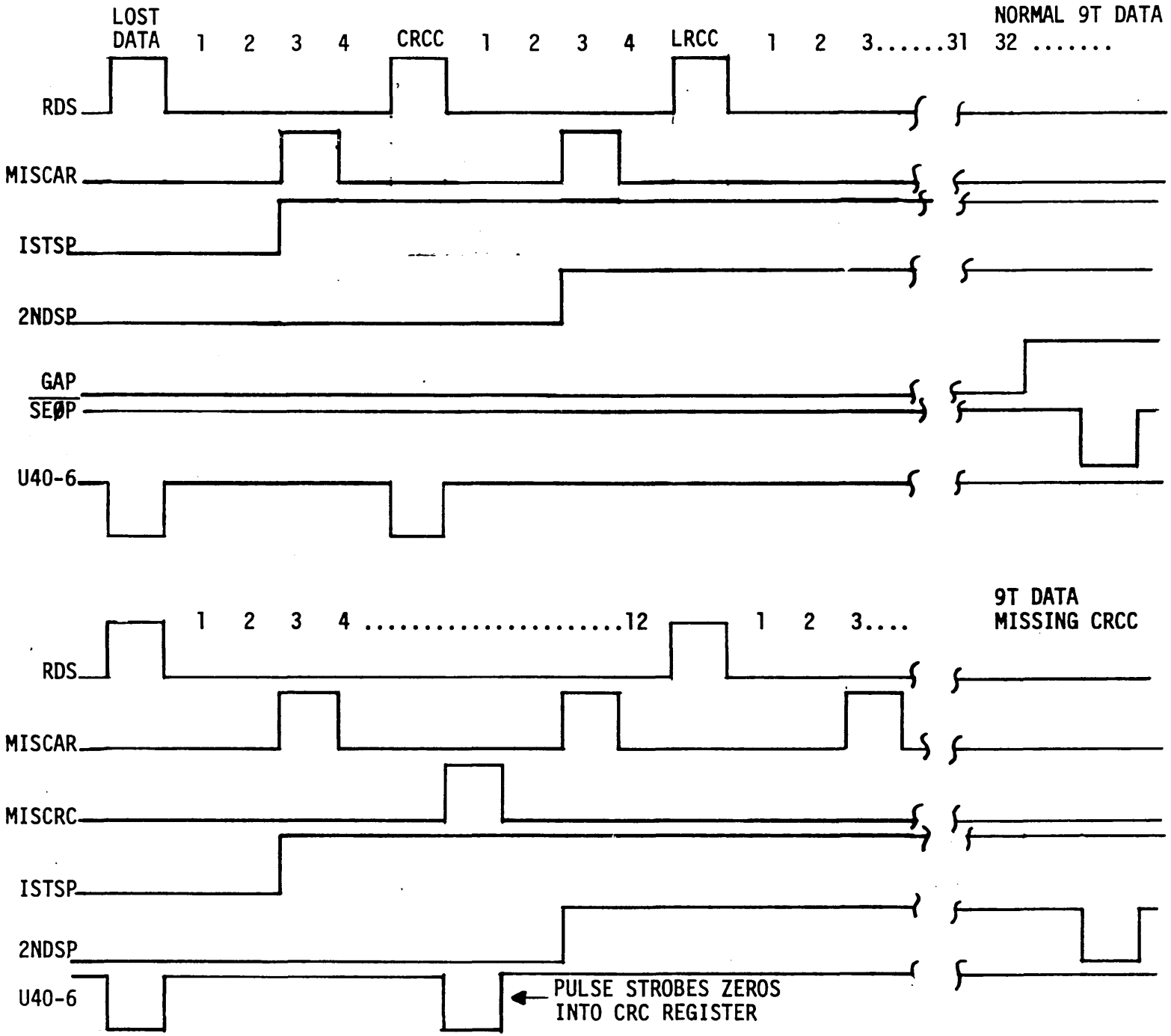


Figure 5-51. Normal Strobed Data

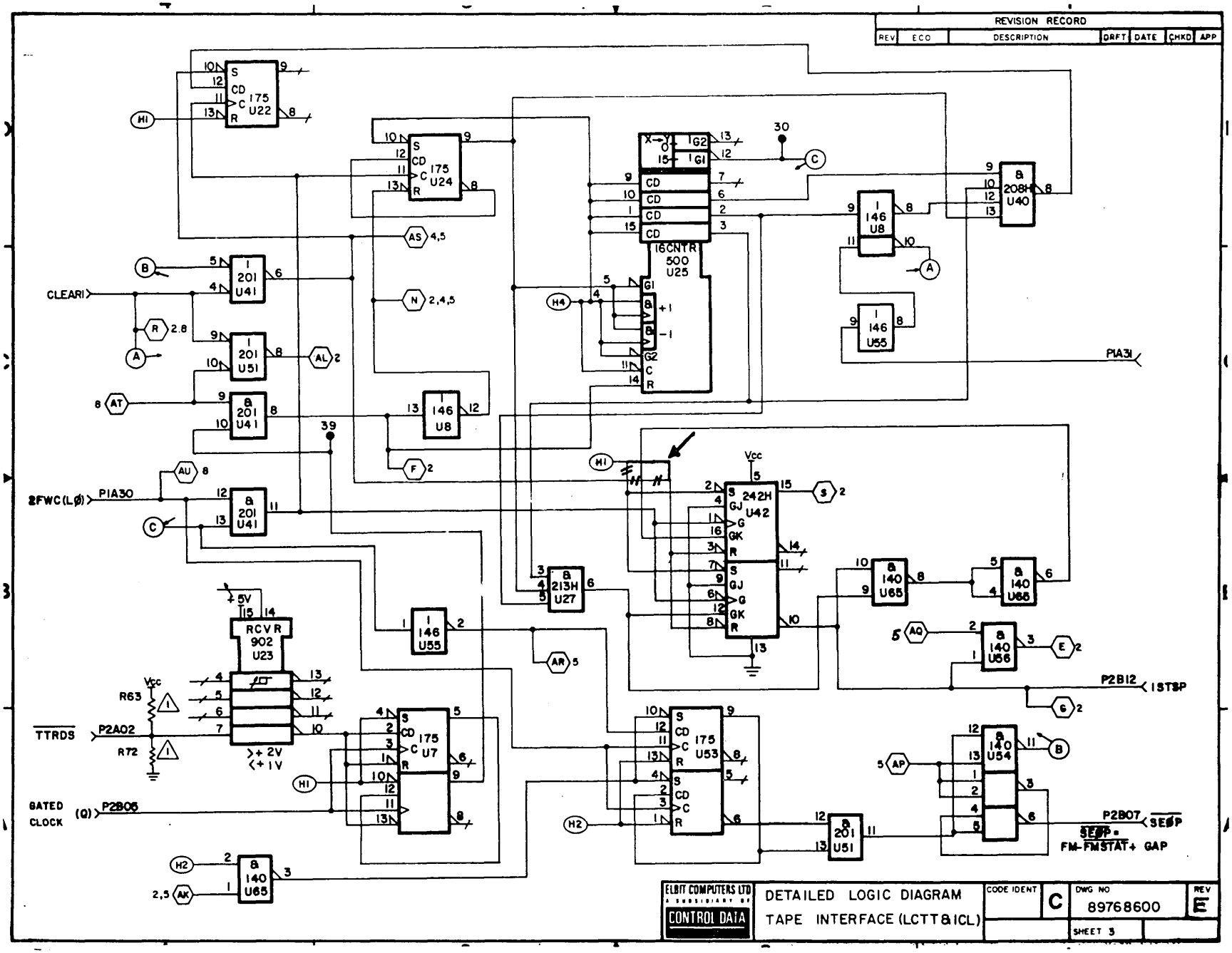


Figure 5-52. Tape Interface - Data Strobe/EOR Detector Logic Diagram

LRC DETECTOR (Logic Diagram 897686000, Sheet 4) Figure 5-53.

This module consists of a nine-bit Longitudinal Redundancy Check (LRCC) Register (U14, U45 and U61). Each FF is toggled when the Data Read from the tape is high. It also includes the All Zero Decoder (U27-8), and the strobing signal RDS. While reading any data from the tape every character is added bit by bit to the LRCC register at the moment RDS rises.

The LRCC is generated by the MTT in Write Motion when receiving the WRITE RESET signal (U2-10 on Sheet 8).

The LRCC is checked by the MTTC during each motion.

The CRCC and LRCC checks are described in Table 5-6.

TABLE 5-6. CRCC & LRCC CHECKS

SIGNAL	CRCC	LRCC	VERT. PAR.
WRITE MØTIØN	Generated by MTTC No checking	Generated by transport Checked by controller	Generated and checked by MTTC
READ MØTIØN	Checked by MTTC	Checked by MTTC	Checked by MTTC
WRITE FM	None	Generated by transport Checked by MTTC.	Generated and checked by MTTC *
READ FM	None	Checked by MTTC	Checked by MTTC *

* In nine track, 800 BPI the MTTC indicates a legal Vertical Parity Error.

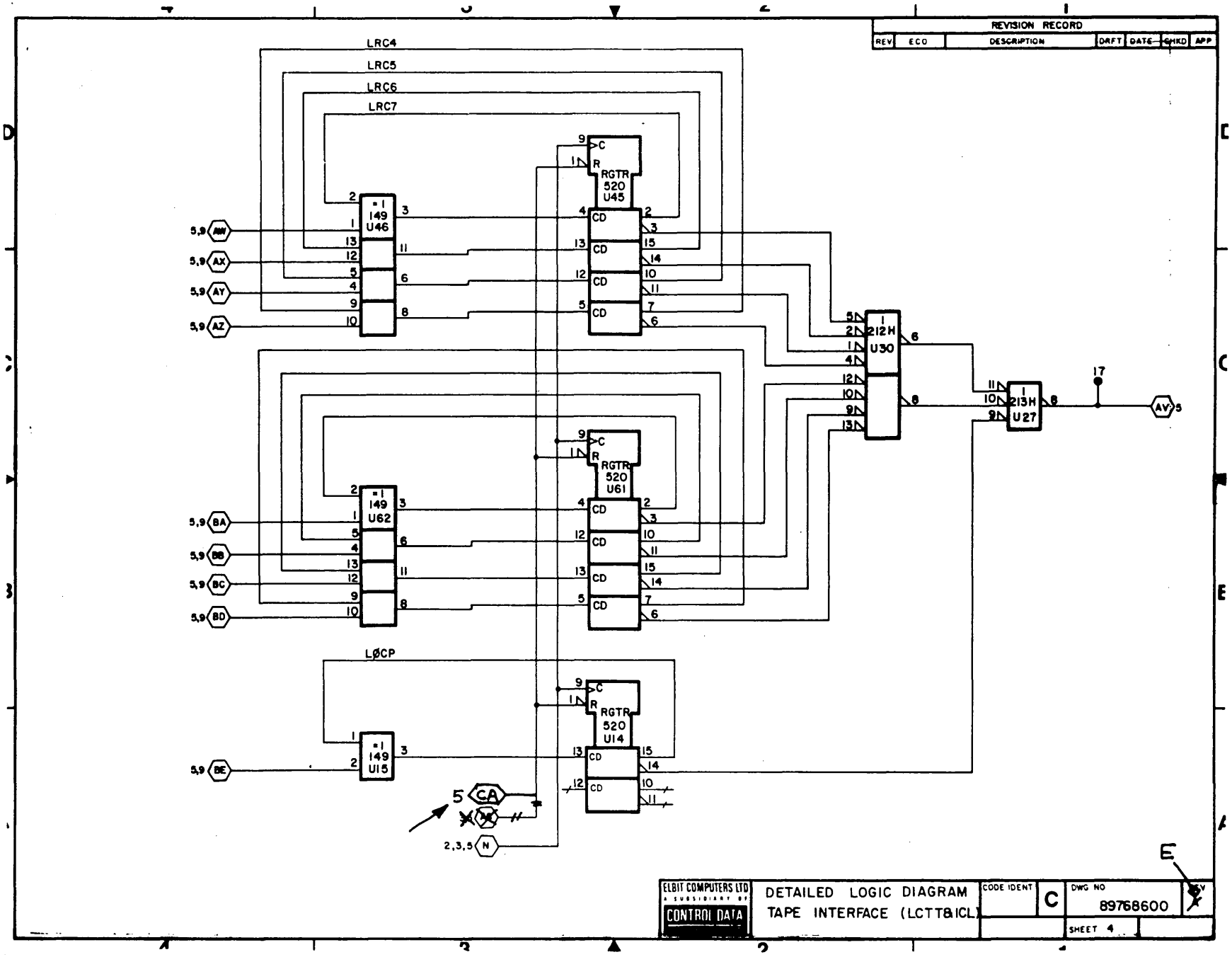


Figure 5-53. Tape Interface - LRC Detector Logic Diagram

PARITY ERROR/FILL/FM DETECTOR (Logic Diagram 89768600, Sheet 5) Figure 5-54.

Parity Error

U31 and U15-11 detect the Vertical Parity of the data from the tape, according to Table 5-7. DATA STROBE strobes the Parity into VPE (VERTICAL PARITY ERROR) (U10-15) and after this is set, it can be reset only by Clear A. Also $\overline{\text{PEPARER}}$ sets VPE.

TABLE 5-7. PARITY STATE

	Binary	BCD
Vertical Parity	Even	Odd

PARR ERR Status (U52-8)=(LRCERROR+CRCERR) EØP+VPE

Fill

U10-10 is the fill FF that toggles if A/D is high and is not changed otherwise. The toggling signal is RDS. (RDS for NRZI data only).

File Mark Detector

U32, U16, U26/6 compare the incoming character and the FM code according to 9T and produce FM Match is high if FM/TM is detected.

$\overline{\text{RDS}}$ strobes FM MATCH into U14-7 if the next $\overline{\text{RDS}}$ detects an FM MATCH, DET FM is set. U9 counts the number of STROBE DATA'S and if more that one is detected, $\overline{\text{CHAR2}}$ is low (U9-8).

FM STAT = CHAR2·DET FM

FM = PSFM+FM STAT

FM is the FILE MARK status

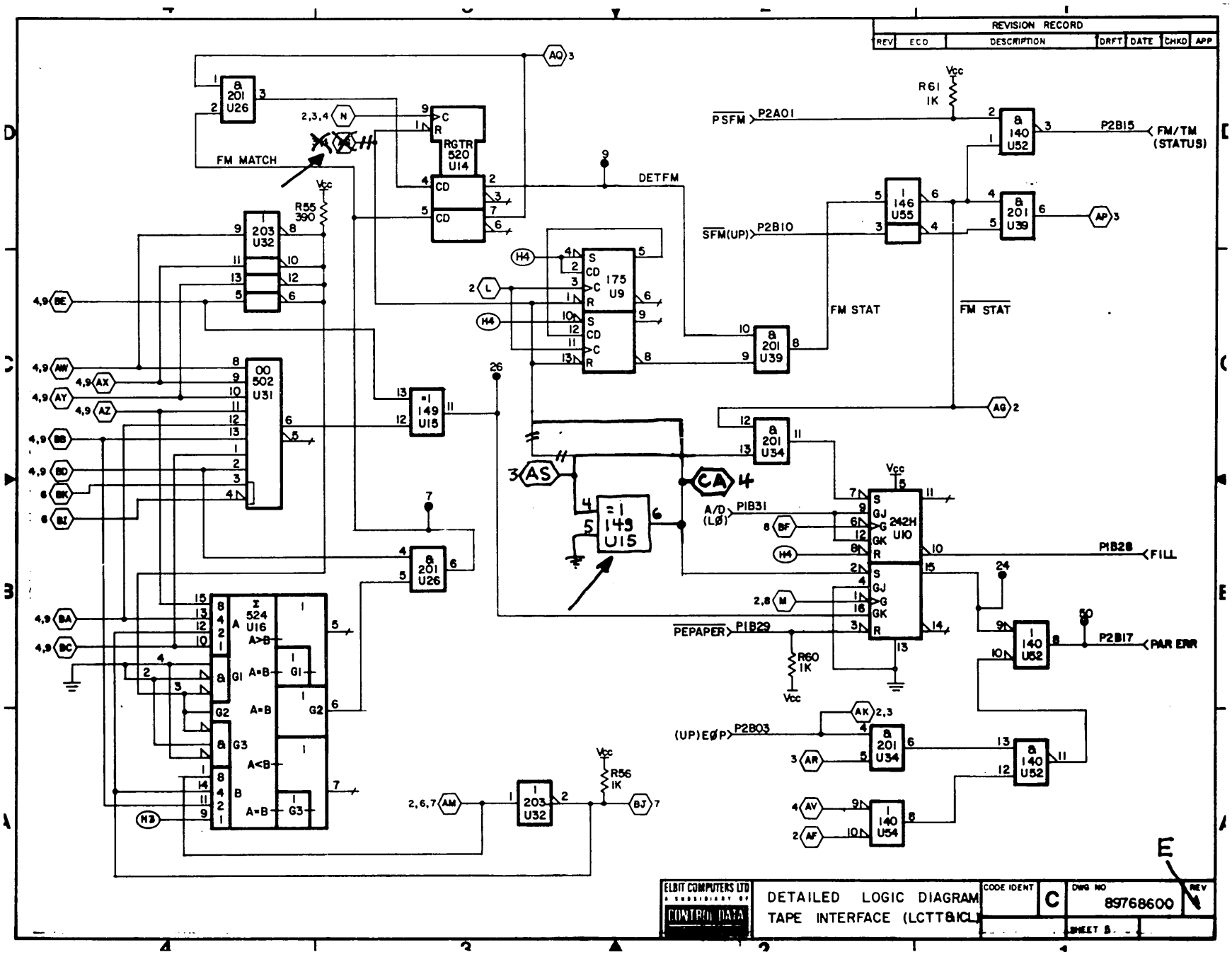


Figure 5-54. Tape Interface - Parity Error/Fill/FM Detector Logic Diagram

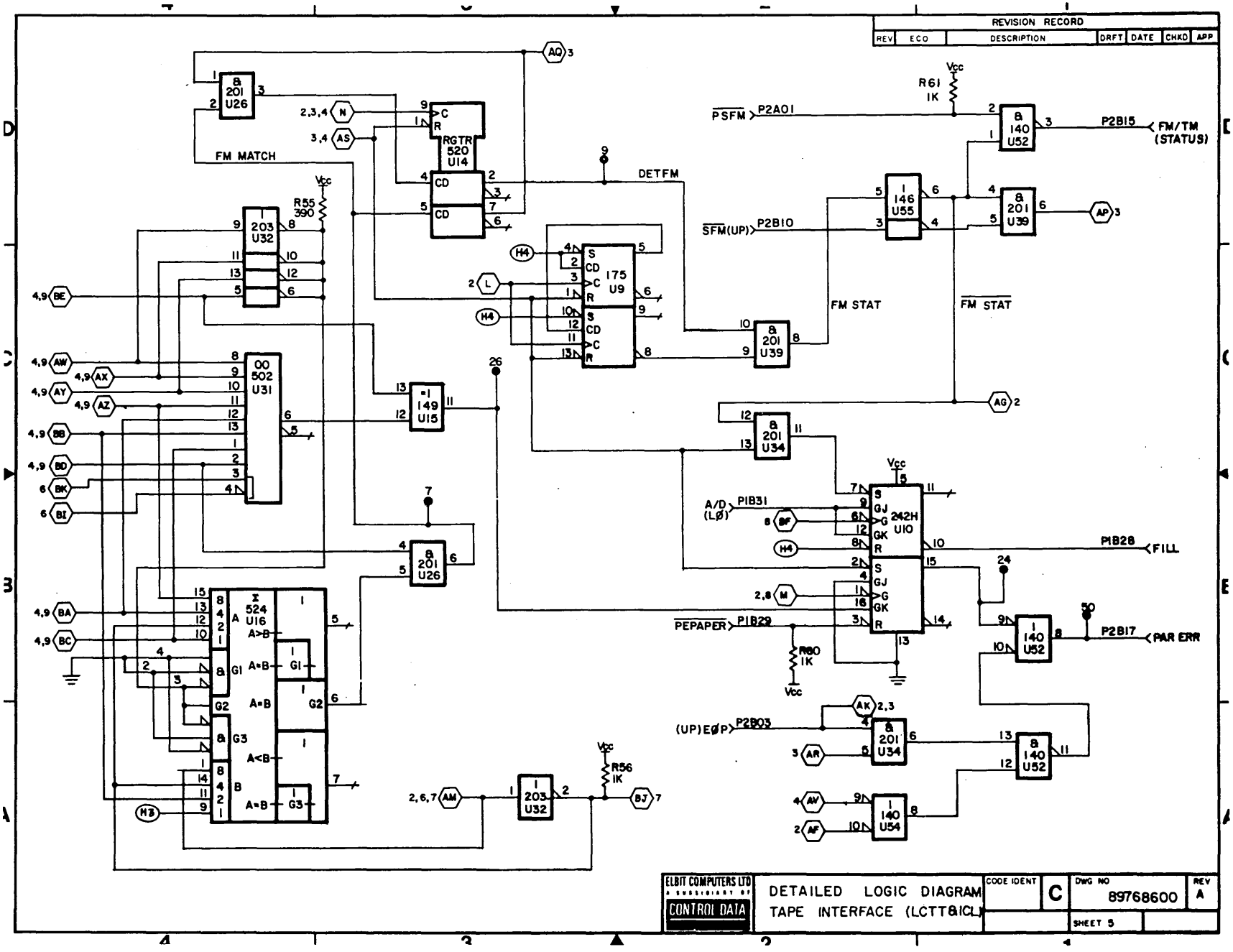
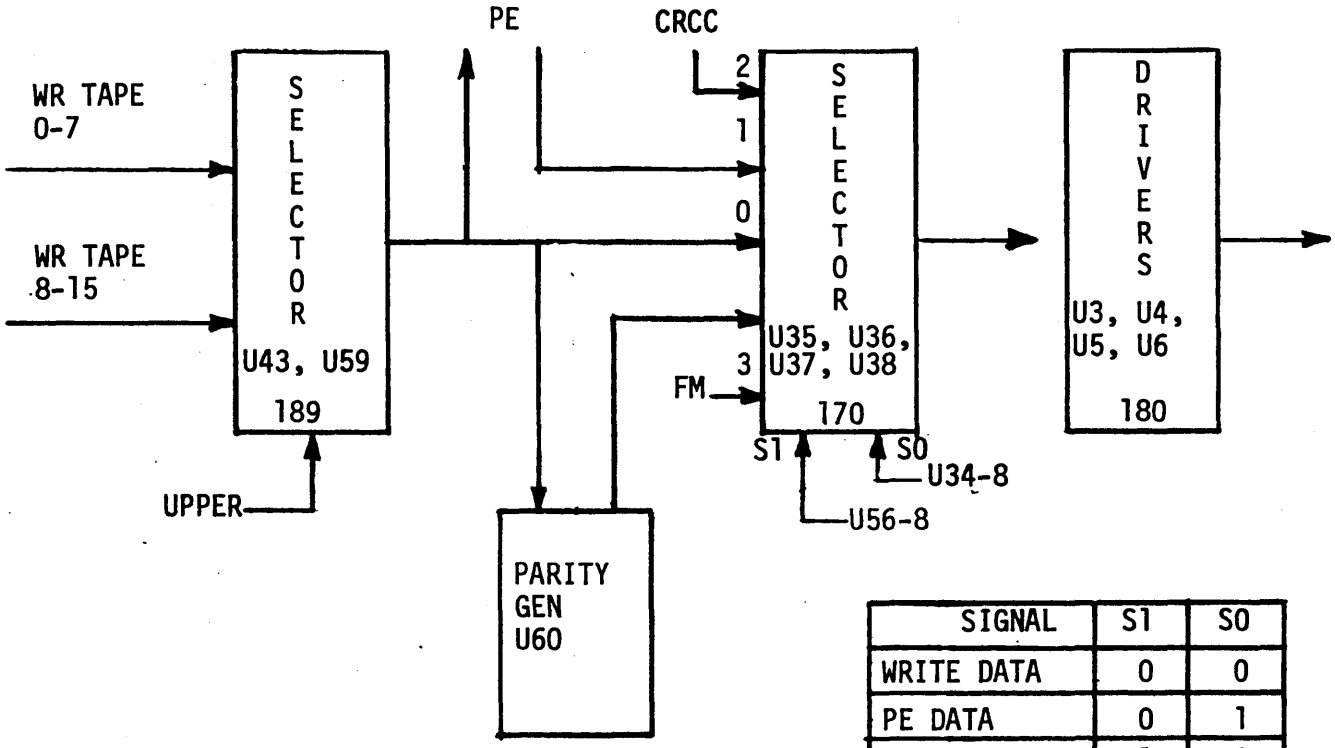


Figure 5-54. Tape Interface - Parity Error/Fill/FM Detector Logic Diagram

MTT/PE WRITE DATA PATH (Logic Diagram 89768600, Sheets 6, 7, and 8)
Figures 5-55, 5-56 and 5-57.

This module receives a data word from the computer via the Double Buffer and sends it either to the tape or to the PE formatter. It contains also a One Of Four Selector that selects a Data Character, Phase Encoded Data, a File Mark or CRCC and sends it to the tape. Refer to Figure 5-55.



SIGNAL	S1	S0
WRITE DATA	0	0
PE DATA	0	1
CRCC	1	0
NRZI FM	1	1

Figure 5-55. MTT/PE Write Data Path

The computer word WRTAPE (0-15) is divided into U43, U59 by the UPPER signal (assembly/disassembly). The two most significant bits are ENDed with 9 TRACK (U26). The six-or eight bit character enters a parity generator (U60) and a 7 or 9 bit character is created. This character is sent to the following units: PWDIN (0-7), CRCC generator (selector U47, U63 on Sheet 8, U57 on Sheet 6), and WRITE To Tape Selector (U35, U36, U37 and U38 Sheet 6).

This selector receives its data from:

1. NRZI data from the seven or nine-bit character.
2. PE Data from the formatter (PWOUT 0-7).
3. CRCC from the CRC Generator.
4. FM, i.e., DC wired and only bits 2, 3 and 4, depend on nine tracks for contstants as shown in Table 5-8.

TABLES 5-8 FM CONSTANTS

TRACKS	7	6	5	4	3	2	1	0	P
9T	0	0	0	1	0	0	1	1	0
7T	0	0	0	0	1	1	1	1	0

Control of the Selector is according to the equations:

$$U34\text{-}8 = \overline{1600}\cdot(E\emptyset RS+WFM/TM)$$

$$U56\text{-}8 = 1600+WFM$$

$\overline{WDS}$ and $\overline{WReset}$ are generated according to:

$$\overline{WDS} = WRITE\ CLOCK\ \cdot(E\emptyset RS+CRCC\ STATE\cdot WFM/TM \quad (U20\text{-}11)$$

$$WRESET = WRITE\ CLOCK\ \cdot LRCC\ STATE \quad (U20\text{-}8)$$

There is a PE-NRZI Selector (U18 Sheet 7) that selects the WRITE STROBE (WDS), WRITE RESET (WRESET), WRITE PARITY bit (TTWDP), and RDS* according to 1600:

$$TTWDP = = 1600\cdot PWOUT+\overline{1600}\ (\overline{U56}\text{-}8\ U34\text{-}8\cdot CRCCP+\overline{U34}\text{-}8\cdot U60\text{-}6)$$

$$TTWDS = = 1600\cdot PWCLK+\overline{1600}\cdot\overline{WDS}$$

$$TTWRESET = 1600\cdot PWRESET+\overline{1600}\cdot\overline{WRESET}$$

$$RDS* = RMOT(1600\cdot PRSTROBE+\overline{1600}\cdot RDS)$$

U2, U3, U4, U5 and U6 are Drivers to the tape transport.

There is a PE-NRZI Selector (U18 Sheet 7) that selects the WRITE STROBE (WDS), WRITE RESET (WRESET), WRITE PARITY bit (TTWDP), and RDS* according to 1600:

$$\overline{TTWDP} = 1600 \cdot PWOUT + \overline{1600}\ (\overline{U56\text{-}8} \cdot U34\text{-}8 \cdot CRCCP + \overline{U34\text{-}8} \cdot U60\text{-}6)$$

$$\overline{TTWDS} = 1600 \cdot PWCLK + 1600 \cdot WDS$$

$$TTWRESET = 1600 \cdot PWRESET + 1600 \cdot WRESET$$

$$RDS^* = RMOT(1600 \cdot PRSTROBE + 1600 \cdot RDS)$$

U2, U3, U4, U5 and U6 are Drivers to the tape transport.

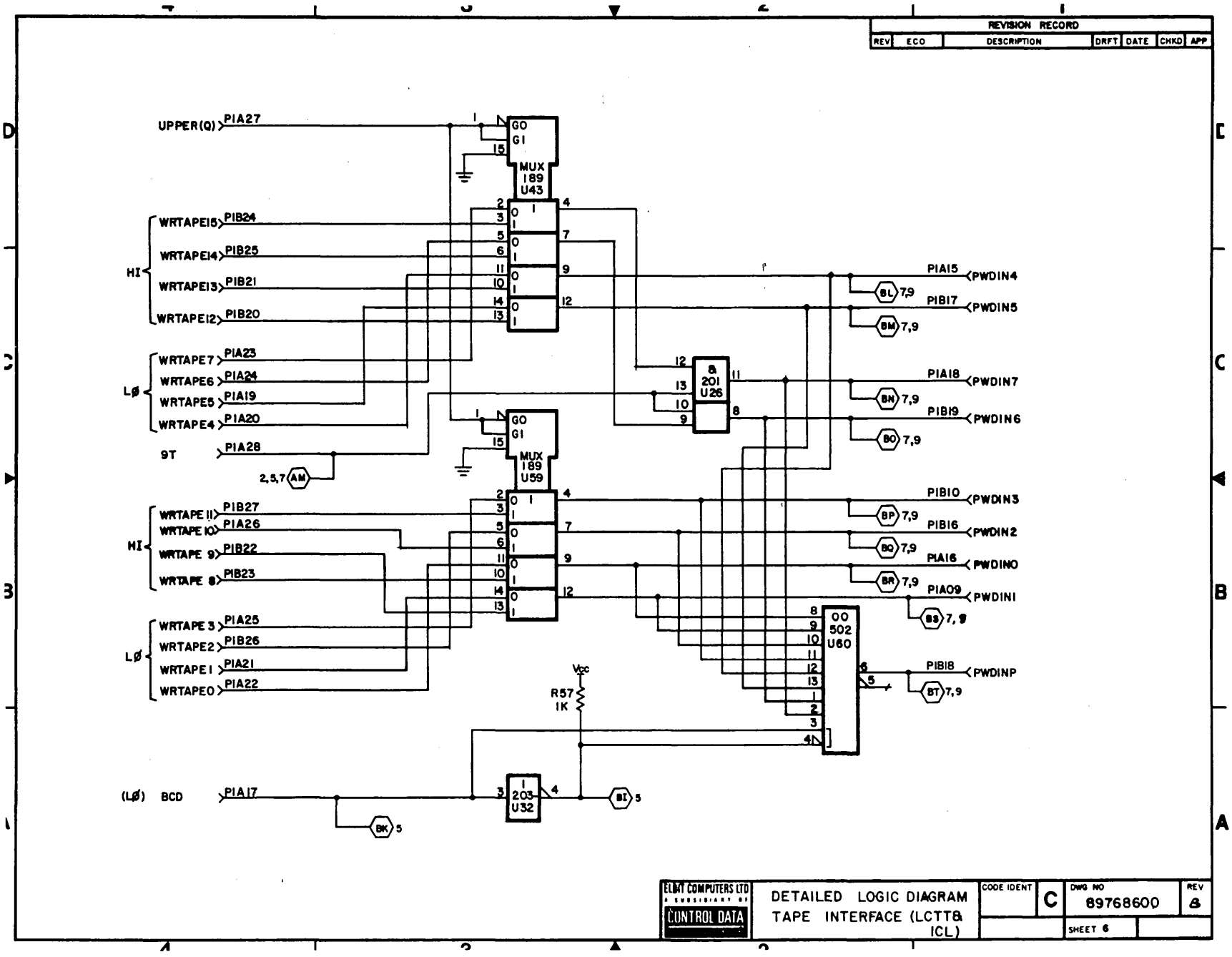


Figure 5-56. Tape Interface - MTT/PE Write Data Path Logic Diagram

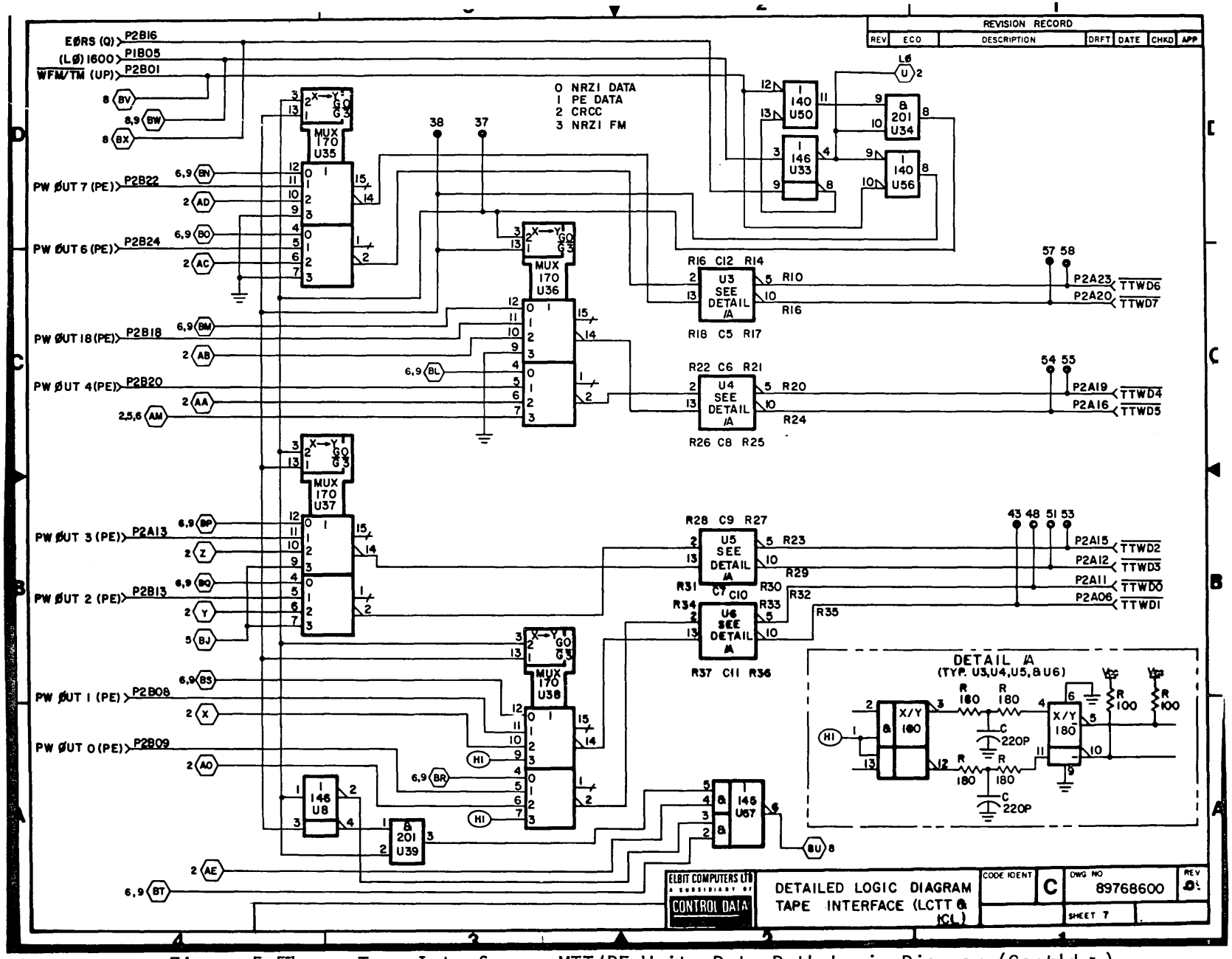


Figure 5-57. Tape Interface - MTT/PE Write Dota Path Logic Diagram (Cont'd 1)

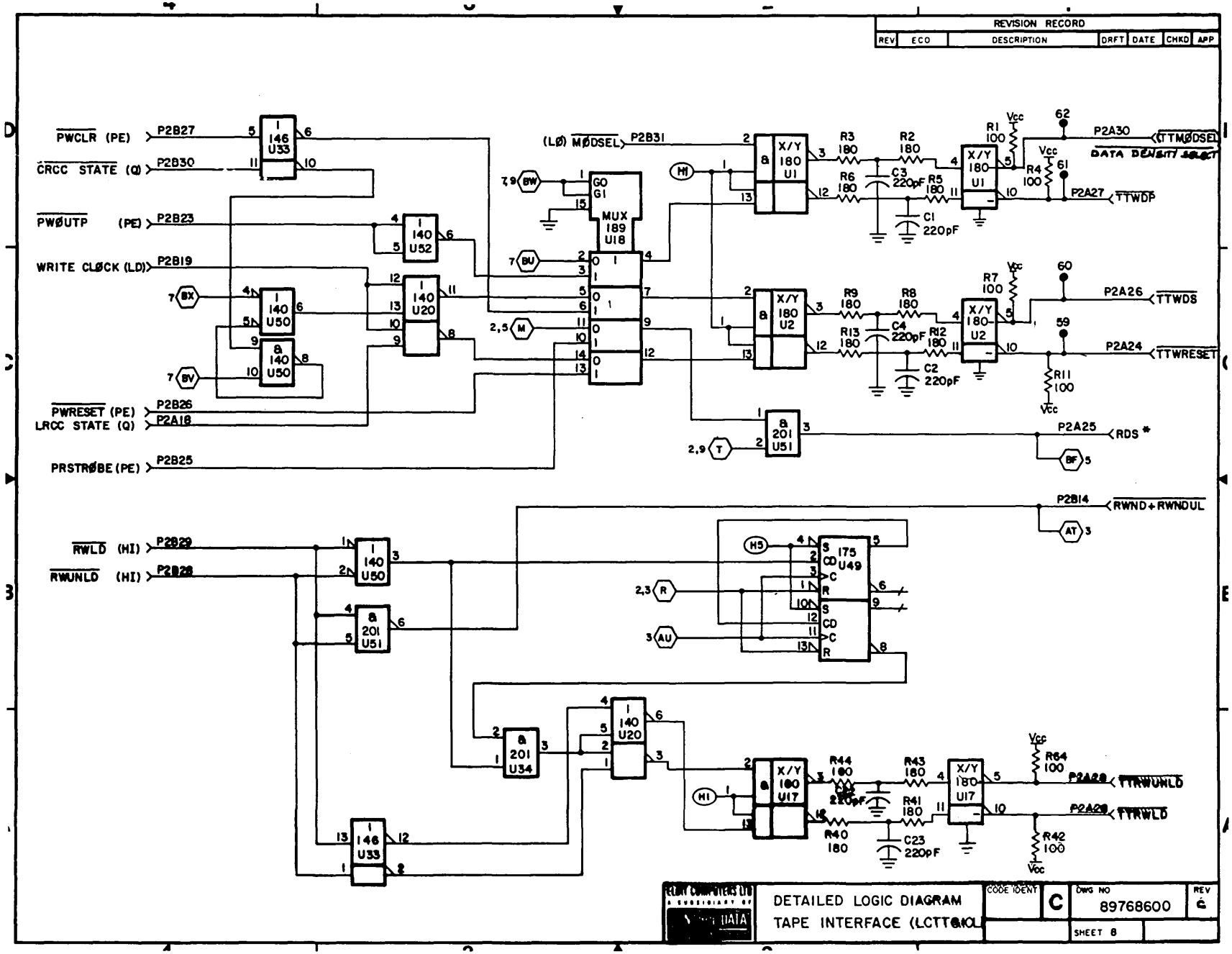


Figure 5-58. Tape Interface - MTT/PE Write Data Path Logic Diagram (Cont'd 2)

MTT/PE READ DATA PATH AND REWIND TRANSMITTER (Logic Diagram 89768600) Sheets 8 and 9).

This module includes the data path shown in Figure 5-59.

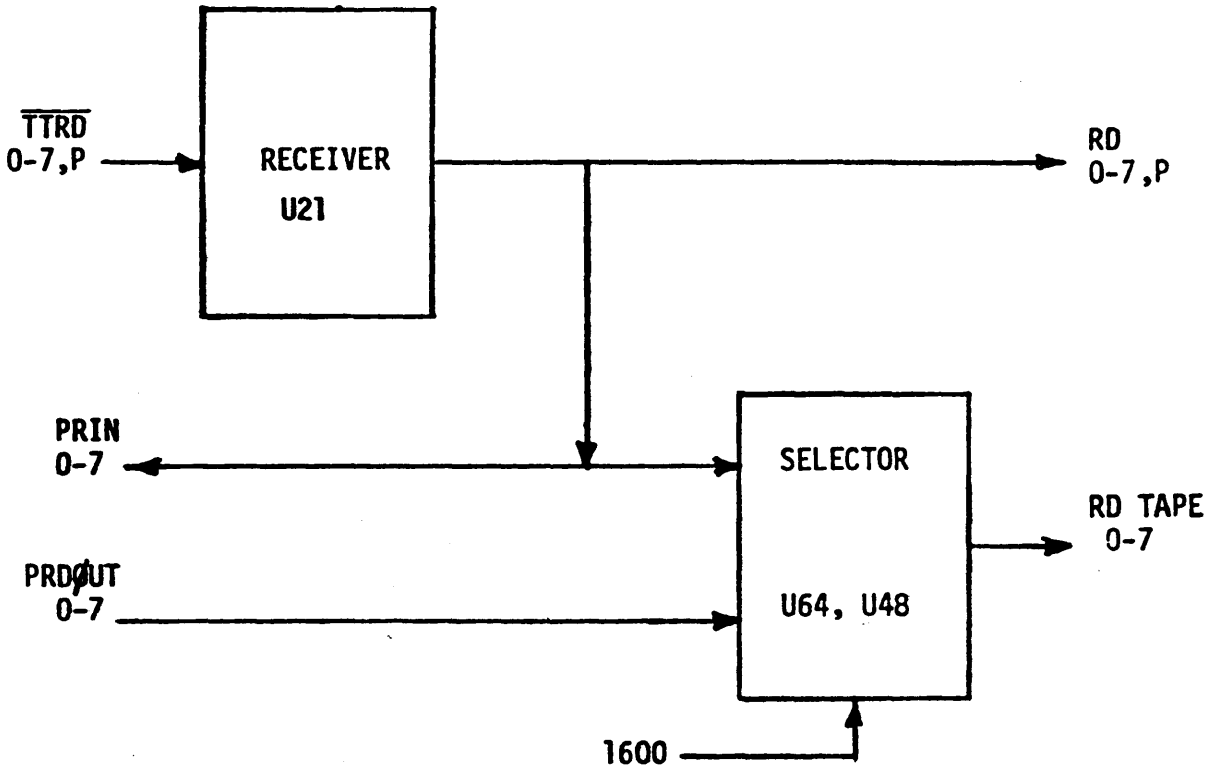


Figure 5-59. MTT/PE Read Data Path

The REWIND and REWIND UNLOAD signals are differentiated at FF U49 by 2FWC and sent to the MTT through drivers U17-10 and U17-5.

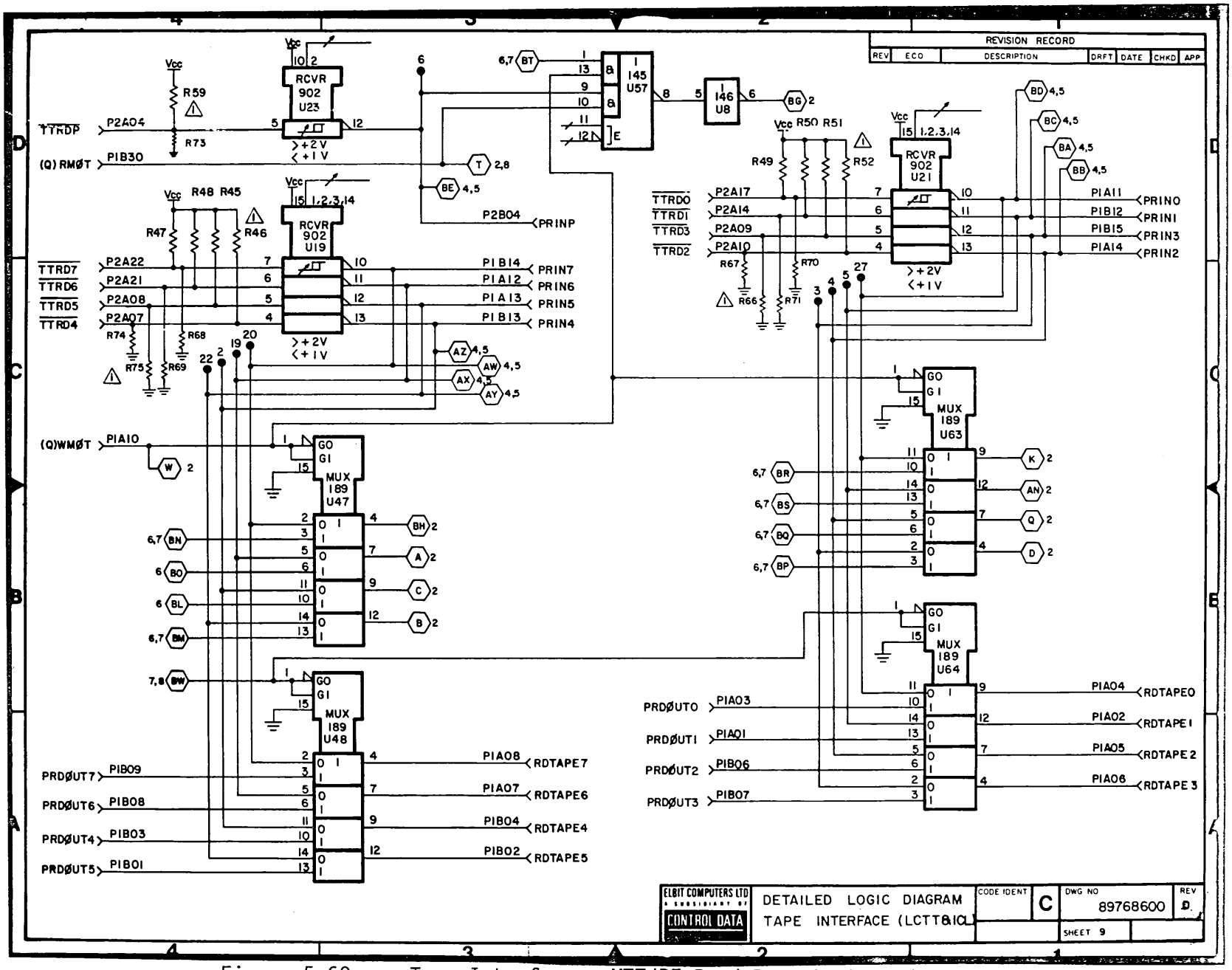


Figure 5-60. Tape Interface - MTT/PE Read Data Path Logic Diagram

REVISION RECORD						
REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

CONTINUED FROM PAG I

ØFF - SHEET REFERENCE

ØFF - SHEET REFERENCE LETTER	SIGNALS	SHEET LØCATIØN							
		2	3	4	5	6	7	8	9
BD	RDO			B-4	C-4				D-1▼
BE	RDP			A-4	C-4				D-3▼
BF	RDS*				B-2			C-1▼	
BG	INCRCP	C-4							D-2▼
BH	INCRC7	C-4							B-3▼
BI	$\overline{BCD}$				B-4	A-2▼			
BJ	$\overline{9T}$				A-2▼		B-4		
BK	BCD				B-4	A-3			
BL	PWDIN 4					C-2▼	C-3		B-4
BM	PWDIN 5					C-2▼	C-4		B-4
BN	PWDIN 7					C-2▼	D-4		B-4
BO	PWDIN 6					C-2▼	D-4		B-4
BP	PWDIN 3					B-2▼	B-4		B-2
BQ	PWDIN 2					B-2▼	B-4		B-2
BR	PWDIN 0					B-2▼	A-3		C-2
BS	PWDIN 1					B-2▼	B-4		B-2
BT	PWDINP					B-2▼	A-4		D-3
BU	AA						A-2▼	C-3	
BV	$\overline{WFM/TM}$						D-4	C-4	
BW	1600 LØ						D-4	D-3	B-4
BX	EØRS						D-4	C-4	
CA				A-3	C-2▼				

ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	TAPE INTERFACE (LCTT & ICL)	CODE IDENT C	DWG NO 89768600	REV E
			SHEET 10	OF 10

Figure 5-61. Tape Interface Logic Diagram Reference Sheet (continued)

SECTION 6

MAINTENANCE

SCOPE

This section gives maintenance references and procedures for the equipment listed in Section 1 of this manual.

TOOLS AND SPECIAL EQUIPMENT

The following is a list of maintenance tools required for this equipment.

Part Number	Part Description	Quantity
89688700	Board Extender	1
89670300	Board Extractor	1
	Oscilloscope	1
	Voltmeter	1

The publications listed below are applicable to the equipment.

Publication	Pub. No.
1784 Computer Customer Engineering Manual	89633300
1784 Computer Reference Manual	89633400
1700 Computer System Codes Manual	60163500
System Maintenance Monitor (SMM 17)	60182000

MAINTENANCE

Preventive maintenance of the controller is not required. After it is determined that the controller has failed, the controller PW board should be removed and replaced with an identical PW board. Failure should be located by removing and replacing each PW board with an identical proble-free board until the failed card is located. For removal and replacement of the card, refer to Section 3 of this manual. After replacement, a diagnostic check should be run according to SMM 17.

SECTION 7

PARTS LIST

The following parts list is applicable to the FA442-A and FA446-A Magnetic Tape Transport Controllers.

Nomenclature	Part Number
FA442-A Printed Wiring Assemblies	FA442-A11 (ICL)
Upper Data Assembly	89935400
Lower Data Assembly	89841600
Tape Interface Assembly	89883600
Q Channel Assembly	89935300
Interrupt Cable Assembly	89724702
Internal Cable Assembly	89700200
External Cable Assembly, Shielded	89818400
FA446-A Printed Wiring Assemblies	FA446-A08 (LCTT)
Upper Data Assembly	~~89985200~~ 89949500
Lower Data Assembly	89767800
Tape Interface Assembly	89881400
Q Channel Assembly	89935500
Interrupt Cable Assembly	89724702
Internal Cable Assembly	89700200
External Cable Assembly, Shielded	
132-inches	89950601
264-inches	89950600

SECTION 8

WIRE LISTS

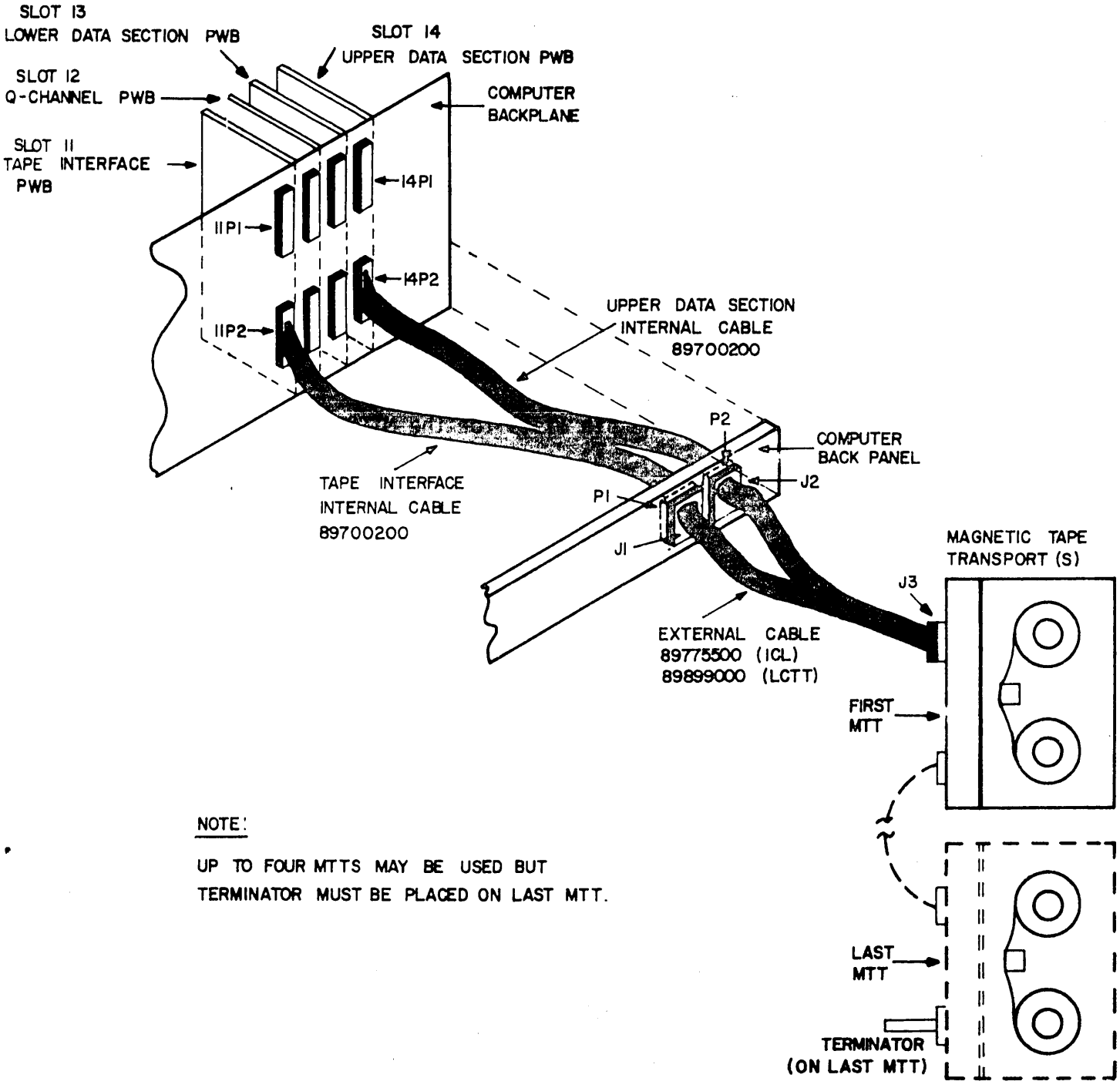
WIRE LISTS

Figure 8-1 shows the placement of the external and internal cables, and the positions for the MTTC PWA's in the enclosure.

Table 8-1 is the wire list for the ICL MTTC internal and external cables.

Table 8-2 is the wire list for the LCTT MTTC internal and external cables.

Tables 8-3 through 8-10 are the pin lists for the MTTC PWA's.



NOTE:

UP TO FOUR MTTS MAY BE USED BUT TERMINATOR MUST BE PLACED ON LAST MTT.

Figure 8-1. Placement of Cables

TABLE 8-1. WIRE LIST - FA442-A (ICL) MTTC TO MTT

INTERNAL CABLE ASSY 89700200			EXTERNAL CABLE ASSY 89818400			
SLOT/ CONNECTOR/ PIN	COLOR	BACKPANEL CONNECTOR/ PIN	BACKPANEL CONNECTOR/ PIN	COLOR	MTT CONNECTOR/ PIN	SIGNAL NAME
11P2A01	WHT-BLK	J1-1	P1-1		P3	
	BLK	-2	-2			
02	WHT-BRN	-3	-3	BLK	-AZ	$\overline{\text{READ DATA STROBE}}$
	BLK	-4	-4	GRN	-BA	GND
04	WHT-RED	-5	-5	BLK	-BR	$\overline{\text{READ } 2^8\text{-PARITY}}$
	BLK	-6	-6	YEL	-BX	GND
05	WHT-ORN	-7	-7			
06	WHT-YEL	-9	-9	YEL	-C	$\overline{\text{WRITE } 2^1}$
	BLK	-10	-10	WHT	-D	GND
07	WHT-GRN	-11	-11	BRN	-BL	$\overline{\text{READ } 2^4}$
	BLK	-12	-12	BLU	-BM	GND
08	WHT-BLU	-13	-13	BLK	-BF	$\overline{\text{READ } 2^5}$
	BLK	-14	-14	BLU	-BP	GND
09	WHT-VIO	-15	-15	VIO	-BJ	$\overline{\text{READ } 2^3}$
	BLK	-16	-16	BLU	-BK	GND
10	WHT-GRA	-17	-17	RED	-BB	$\overline{\text{READ } 2^2}$
	BLK	-18	-18	BLU	-BH	GND
11	WHT-BLK	-19	-19	BRN	-A	$\overline{\text{WRITE } 2^0}$
	BRN	-20	-20	RED	-B	GND
12	WHT-BRN	-21	-21	YEL	-H	$\overline{\text{WRITE } 2^3}$
	BRN	-22	-22	RED	-J	GND
13	WHT-RED	-23	-23			
	BRN	-24	-24			
14	WHT-ORN	-25	-25	YEL	-BD	$\overline{\text{READ } 2^1}$
	BRN	-26	-26	BLU	-BE	GND
15	WHT-YEL	-27	-27	BRN	-E	$\overline{\text{WRITE } 2^2}$
	BRN	-28	-28	WHT	-F	GND
16	WHT-GRN	-29	-29	RED	-M	$\overline{\text{WRITE } 2^5}$
	BRN	-30	-30	GRN	-N	GND
17	WHT-BLU	-31	-31	ORN	-AX	$\overline{\text{READ } 2^0}$
	BRN	-32	-32	GRN	-BC	GND
18	WHT-VIO	-33	-33			
	BRN	-34	-34			
11P2A19	WHT-GRA	J1-35	P1-35	WHT	P3 -K	$\overline{\text{WRITE } 2^4}$

(CONT.)

TABLE 8-1. WIRE LIST - FA442-A (ICL) MTTC TO MTT (Cont'd)

INTERNAL CABLE ASSY 89700200			EXTERNAL CABLE ASSY 89818400			SIGNAL NAME
SLOT/ CONNECTOR/ PIN	COLOR	BACKPANEL CONNECTOR/ PIN	BACKPANEL CONNECTOR/ PIN	COLOR	MTT CONNECTOR/ PIN	
11P2A20	WHT-BLK	J1-37	P1-37	WHT	P3-V	WRITE 2^7
	RED	-38	-38	BLU	-U	GND
21	WHT-BRN	-39	-39	GRN	-BN	READ 2^6
	RED	-40	-40	YEL	-BV	GND
22	WHT-RED	-41	-41	BRN	-BU	READ 2^7
	RED	-42	-42	YEL	-BT	GND
23	WHT-ORN	-43	-43	VIO	-P	WRITE 2^6
	RED	-44	-44	BLK	-W	GND
24	WHT-YEL	-45	-45	BLU	-AS	WRITE RESET
	RED	-46	-46	GRN	-AT	GND
25	WHT-GRN	-47	-47			
	RED	-48	-48			
26	WHT-BLU	-49	-49	RED	-R	WRITE DATA STROBE
	RED	-50	-50	WHT	-X	GND
27	WHT-VIO	-51	-51	GRN	-T	WRITE 2^8 - PARITY
	RED	-52	-52	VIO	-S	GND
28	WHT-GRA	-53	-53	GRN	-AE	REWIND
	RED	-54	-54	WHT	-AF	GND
29	WHT-BLK	-55	-55	BRN	-AH	REWIND-UNLOAD
	ORN	-56	-56	GRN	-AJ	GND
30	WHT-BRN	-57	-57	RED	-CJ	MODE SELECT
	ORN	-58	-58	BLK	-CK	GND
11P2A31	BLK	- 8	- 8	BRN	-CW	TERMINATOR POWER
11P2B11	WHT-RED	-59	-59			
	ORN	-60	-60			
12	WHT-ORN	-61	-61			
	ORN	-62	-62			
23	WHT-YEL	-63	-63			
	ORN	-64	-64			
11P2B24	WHT-GRN	-65	-65			
	ORN	J1-66	P1-66		P3	

(CONT.)

TABLE 8-1. WIRE LIST - FA442-A (ICL) MTTC TO MTT (Cont'd)

INTERNAL CABLE ASSY 89700200			EXTERNAL CABLE ASSY 89818400			SIGNAL NAME
SLOT/ CONNECTOR/ PIN	COLOR	BACKPANEL CONNECTOR/ PIN	BACKPANEL CONNECTOR/ PIN	COLOR	MTT CONNECTOR/ PIN	
14P2A01	WHT-BLK	J2-1	P2-1		P3	
	BLK	-2	-2			
02	WHT-BRN	-3	-3	VIO	-AU	$\overline{\text{BEGINNING OF TAPE}}$
	BLK	-4	-4	BLK	-AY	GND
04	WHT-RED	-5	-5			
	BLK	-6	-6			
05	WHT-ORN	-7	-7			
06	WHT-YEL	-9	-9	WHT	-BZ	$\overline{\text{BUSY}}$
	BLK	-10	-10	BLK	-CA	GND
07	WHT-GRN	-11	-11			
	BLK	-12	-12			
08	WHT-BLU	-13	-13	GRN	-AM	$\overline{\text{REVERSE}}$
	BLK	-14	-14	BLK	-AN	GND
09	WHT-VIO	-15	-15			
	BLK	-16	-16			
10	WHT-GRA	-17	-17	YEL	-AK	$\overline{\text{FORWARD}}$
	BLK	-18	-18	BLK	-AL	GND
11	WHT-BLK	-19	-19	BRN	-Y	$\overline{\text{SELECT}}$
	BRN	-20	-20	BLK	-Z	GND
12	WHT-BRN	-21	-21	ORN	-AC	$\overline{\text{UNIT SELECT S}^1}$
	BRN	-22	-22	BLK	-AD	GND
13	WHT-RED	-23	-23			
	BRN	-24	-24			
14	WHT-ORN	-25	-25			
	BRN	-26	-26			
15	WHT-YEL	-27	-27	RED	-AA	$\overline{\text{UNIT SELECT S}^0}$
	BRN	-28	-28	BLK	-AB	GND
16	WHT-GRN	-29	-29	YEL	-CL	$\overline{\text{FILE PROTECT}}$
	BRN	-30	-30	BRN	-CM	GND
17	WHT-BLU	-31	-31			
	BRN	-32	-32			
18	WHT-VIO	-33	-33	GRA	-BS	$\overline{\text{END OF TAPE}}$
	BRN	-34	-34	BLK	-BY	GND
14P2A19	WHT-GRA	-35	-35		P3	
	BRN	J2-36	P2-36			

(CONT.)

TABLE 8-1. WIRE LIST - FA442-A (ICL) MTTC TO MTT (Cont'd)

INTERNAL CABLE ASSY 89700200			EXTERNAL CABLE ASSY 89818400			SIGNAL NAME
SLOT/ CONNECTOR/ PIN	COLOR	BACKPANEL CONNECTOR/ PIN	BACKPANEL CONNECTOR/ PIN	COLOR	MTT CONNECTOR/ PIN	
14P2A20	WHT-BLK	J2-37	P2-37	BLU	P3-AP	WRITE REQUEST
	RED	-38	-38	BLK	-AR	GND
21	WHT-BRN	-39	-39			
	RED	-40	-40			
22	WHT-RED	-41	-41			
	RED	-42	-42			
23	WHT-ORN	-43	-43	RED	-CB	READY
	RED	-44	-44	BRN	-CC	GND
24	WHT-YEL	-45	-45	ORN	-CF	DENSITY STATUS
	RED	-46	-46	BRN	P3-CH	GND
25	WHT-GRN	-47	-47			
	RED	-48	-48			
26	WHT-BLU	-49	-49			
	RED	-50	-50			
27	WHT-VIO	-51	-51			
	RED	-52	-52			
28	WHT-GRA	-53	-53			
	RED	-54	-54			
29	WHT-BLK	-55	-55			
	ORN	-56	-56			
30	WHT-BRN	-57	-57			
	ORN	-58	-58			
14P2A31	BLK	- 8	- 8			
11P2B11	WHT-RED	-59	-59			
	ORN	-60	-60			
12	WHT-ORN	-61	-61			
	ORN	-62	-62			
23	WHT-YEL	-63	-63			
	ORN	-64	-64			
11P2B24	WHT-GRN	-65	-65			
	ORN	J2-66	P2-66			

TABLE 8-2. WIRE LIST - FA446-A (LCTT) MTTC TO MTT

INTERNAL CABLE ASSY 89700200			EXTERNAL CABLE ASSY 89899000			SIGNAL
SLOT/ CONNECTOR/ PIN	COLOR	BACKPANEL CONNECTOR/ PIN	BACKPANEL CONNECTOR/ PIN	COLOR	MTT CONNECTOR/ PIN	
11P2A01	WHT-BLK	J1-1	P1-1			
	BLK	-2	-2			
02	WHT-BRN	-3	-3	WHT	J3-2	$\overline{\text{READ DATA STROBE}}$
	BLK	-4	-4	GRN	J3-B	GND
	BLK	--	--			
04	WHT-RED	-5	-5	ORN	J3-1	$\overline{\text{READ } 2^8\text{-PARITY}}$
	BLK	-6	-6	BLK	J3-1	GND
05	WHT-ORN	-7	-7	-	--	
06	WHT-YEL	-9	-9	RED	J@-U	$\overline{\text{WRITE DATA 1}}$
	BLK	-10	-10	BLK	J2-7	GND
07	WHT-GRN	-11	-11	YEL	J3-9	$\overline{\text{READ DATA 4}}$
	BLK	-12	-12	BLK	J3-K	GND
08	WHT-BLU	-13	-13	BRN	J3-8	$\overline{\text{READ DATA 5}}$
	BLK	-14	-14	BLK	J3-J	GND
09	WHT-VIO	-15	-15	BLU	J3-14	$\overline{\text{READ DATA 3}}$
	BLK	-16	-16	BLK	J3-R	GND
10	WHT-GRA	-17	-17	ORN	J3-15	$\overline{\text{READ DATA 2}}$
	BLK	-18	-18	BLK	J3-5	GND
11	WHT-BLK	-19	-19	V10	J2-V	$\overline{\text{WRITE DATA 0}}$
	BRN	-20	-20	BLK	J2-18	GND
12	WHT-BRN	-21	-21	ORN	J2-S	$\overline{\text{WRITE DATA 3}}$
	BRN	-22	-22	WHT	J2-15	GND
13	WHT-RED	-23	-23	-		
	BRN	-24	-24	-		
14	WHT-ORN	-25	-25	RED	J3-17	$\overline{\text{READ DATA 1}}$
	BRN	-26	-26	WHT	J3-U	GND
15	WHT-YEL	-27	-27	YEL	J2-T	$\overline{\text{WRITE DATA 2}}$
	BRN	-28	-28	WHT	J2-16	GND
16	WHT-GRN	-20	-29	BRN	J2- P	$\overline{\text{WRITE DATA 5}}$
	BRN	-30	-30	WHT	J2-13	GND
17	WHT-BLU	-31	-31	BLU	J3-18	$\overline{\text{READ DATA 0}}$
	BRN	-32	-32	WHT	J3-V	GND
18	WHT-VIO	-33	-33			
	BRN	-34	-34			
11P2A19	WHT-GRA	-35	-35	GRN	J2-R	$\overline{\text{WRITE DATA 4}}$
	BRN	J1-36	P1-36	WHT	J2-14	GND

(CONT.)

TABLE 8-2. WIRE LIST - FA446-A (LCTT) MTTC TO MTT (Cont'd)

INTERNAL CABLE ASSY 89700200			EXTERNAL CABLE ASSY 89899000			
SLOT/ CONNECTOR PIN	COLOR	BACKPANEL CONNECTOR/ PIN	BACKPANEL CONNECTOR/ PIN	COLOR	MTT CONNECTOR/ PIN	SIGNAL NAME
11P2A20	WHT-BLK	J1-37	P1-37	VIO	J2-M	WRITE DATA 7
	RED	-38	-38	WHT	J2-11	GND
21	WHT-BRN	-39	-39	ORN	J3-4	READ DATA 6
	RED	-40	-40	BLU	J3-D	GND
22	WHT-RED	-41	-41	RED	J3-3	READ DATA 7
	RED	-42	-42	BLU	J3-C	GND
23	WHT-ORN	-43	-43	YEL	J2-N	WRITE DATA 6
	RED	-44	-44	BLU	J3-12	GND
24	WHT-YEL	-45	-45	BNR	J3-C	WRITE AMPL RESET
	RED	-46	-46	BLU	J3-3	GND
25	WHT-GRN	-47	-47			
	RED	-48	-48			
26	WHT-BLU	-49	-49	GRN	J3-A	WRITE DATA STROBE
	RED	-50	-50	BLU	J2-1	GND
27	WHT-VIO	-51	-51	VIO	J2-L	WRITE 2^8-PARITY
	RED	-52	-52	BLU	J2-10	GND
28	WHT-GRA	-53	-53	GRN	J1-H	REWIND
	RED	-54	-54	RED	J1-7	GND
29	WHT-BLK	-55	-55			
	ORN	-56	-56			
30	WHT-BRN	-57	-57	YEL	J1-D	DATA DENSITY SEL.
	ORN	-58	-58	RED	J1-4	GND
11P2A31	BLK	- 8	- 8	BRN	-CW	TERMINATOR POWER
11P2B11	WHT-RED	-59	-59	BRN	J1-M	ON LINE
	ORN	-60	-60	RED	J1-11	GND
12	WHT-ORN	-61	-61			
	ORN	-62	-62			
23	WHT-YEL	-63	-63			
	ORN	-64	-64			
11P2B24	WHT-GRN	-65	-65			
	ORN	J1-66	P1-66			

TABLE 8-2. WIRE LIST - FA446-A (LCTT) MTTC TO MTT (Cont'd)

INTERNAL CABLE ASSY 89700200			EXTERNAL CABLE ASSY 89899000			SIGNAL NAME
SLOT/ CONNECTOR/ PIN	COLOR	BACKPANEL CONNECTOR/ PIN	BACKPANEL CONNECTOR/ PIN	COLOR	MTT CONNECTOR PIN	
142A01	WHT-BLK	J2-1	P2-1			
	BLK	-2	-2			
02	WHT-BRN	-3	-3	BRN	J1-R	BOT
	BLK	-4	-4	BLK	J1-14	GND
	BLK					
04	WHT-RED	-5	-5			
	BLK	-6	-6			
05	WHT-ORN	-7	-7			
06	WHT-YEL	-9	-9	RED	J2-F	READ THRESHOLD
	BLK	-10	-10	BLK	J2-6	GND
07	WHT-GRN	-11	-11			
	BLK	-12	-12			
08	WHT-BLU	-13	-13	ORN	J1-E	SYNC REVERSE COM
	BLK	-14	-14	BLK	J1-5	GND
09	WHT-VIO	-15	-15			
	BLK	-16	-16			
10	WHT-GRA	-17	-17	YEL	J1-C	SYNC FORWARD COM
	BLK	-18	-18	BLK	JL-3	GND
11	WHT-BLK	-19	-19	GRN	J1-18	SELECT 2
	BRN	-20	-20	BLK	J1-8	GND
12	WHT-BRN	-21	-21	BLU	J1-	SELECT 1
	BRN	-22	-22	BLK	J1-8	GND
13	WHT-RED	-23	-23			
	BRN	-24	-24			
14	WHT-ORN	-25	-25			
	BRN	-26	-26			
15	WHT-YEL	-27	-27	VIO	J1-JA	SELECT 0
	BRN	-28	-28	BLK	J1-8	GND
16	WHT-GRN	-29	-29	GRA	J1-P	FILE PROTECT
	BRN	-30	-30	BLK	J1-13	GND
17	WHT-BLU	-31	-31			
	BRN	-32	-32			
18	WHT-VIO	-33	-33	WHT	J1-U	END OF TAPE
	BRN	-34	-34	BLK	J1-17	GND
142A19	WHT-GRA	-35	-35			
	BRN	J2-36	P2-36			

(CONT.)

TABLE 8-2. WIRE LIST - FA446-A (LCTT) MTTC TO MTT (Cont'd)

INTERNAL CABLE ASSY 89700200			EXTERNAL CABLE ASSY 89899000			SIGNAL NAME
SLOT/ CONNECTOR/ PIN	COLOR	BACKPANEL CONNECTOR PIN	BACKPANEL CONNECTOR PIN	COLOR	MTT CONNECTOR/ PIN	
14P2A20	WHT-BLK	J2-37	P2-37	RED	J1-K	$\overline{\text{SET WRITE STATUS}}$
	RED	-38	-38	BRN	J1-9	GND
21	WHT-BRN	-39	-39			
	RED	-40	-40			
22	WHT-RED	-41	-41			
	RED	-42	-42			
23	WHT-ORN	-43	-43			
	RED	-44	-44			
24	WHT-YEL	-45	-45	YEL	J1-F	$\overline{\text{DATA DENSITY IN}}$
	RED	-46	-46	BRN	J1-6	GND
25	WHT-GRN	-47	-47			
	RED	-48	-48			
26	WHT-BLU	-49	-49	GRN	J1-V	$\overline{\text{SELECT 3}}$
	RED	-50	-50	BRN	J1-8	GND
27	WHT-VIO	-51	-51	BLU	J1-S	+5V SPARE } TWISTED
	RED	-52	-52	BRN	J1-S	+5V SPARE } PAIR
28	WHT-GRA	-53	-53	ORN	J1-T	$\overline{\text{TT READY}}$
	RED	-54	-54	BRN	J1-16	
29	WHT-BLK	-55	-55			
	ORN	-56	-56			
30	WHT-BRN	-57	-57			
	ORN	-58	-58			
14P2A31	BLK	- 8	- 8			
11P2B11	WHT-RED	-59	-59			
	ORN	-60	-60			
12	WHT-ORN	-61	-61			
	ORN	-62	-62			
23	WHT-YEL	-63	-63			
	ORN	-64	-64			
11P2B24	WHT-GRN	-65	-65			
	ORN	J2-66	P2-66			

TABLE 8-3. PIN LIST - Q CHANNEL - INPUT SIGNAL

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1	DSA PRØT FAULT	P1B1	
2		2	
3		3	
4		4	
5		5	ISTSP
6		6	A/D
7		7	$\overline{\text{TRANS}}$
8		8	
9	LAST WØRD	9	
10		10	WRITE CLØCK
11	EARLY WDS	11	
12	$\overline{\text{WDS SHIFTED}}$	12	$\overline{\text{PWRQ SHIFTED}}$
13		13	
14	$\overline{\text{DSA RESUME}}$	14	
15		15	
16		16	
17		17	
18		18	1600 BPI
19		19	$\overline{\text{RES2}}$
20		20	
21		21	
23		23	
24		24	WFM/TM
25		25	
26		26	
27	(T1)RDS	27	$\overline{\text{STØP}}$
28	PWRQ(PE)	28	
29		29	$\overline{\text{A/Q READ}}$
30	$\overline{\text{9T}}$	30	$\overline{\text{A/Q WRITE}}$
31		31	
32		32	
33		33	
P1A34		P1B34	

(CONT.)

TABLE 8-3. PIN LIST - Q CHANNEL - INPUT SIGNAL (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1		P2B1	A/Q Q1
2		2	$\overline{MC}$
3		3	
4	LEGMF	4	
5		5	$\overline{RMØT}$
6	CØNTACT	6	$\overline{WMØT}$
7	LEGCF	7	A7
8	EØP	8	
9		9	
10		10	BUSY
11		11	
12	LEGUS	12	$\overline{A8 \cdot A9 \cdot A10}$
13	READY	13	
14		14	
15		15	PRØTECTED
16		16	INT
17	FM/TM STATUS	17	GC128
18		18	$\overline{REST}$
19	$\overline{A/Q\ PRØTECT}$	19	
20		20	
21		21	
22		22	
23		23	
24		24	
25		25	SCAN FØR IN
26		26	
27		27	STPCLK
28	EXT CLK	28	SCAN REV ØUT
29		29	
30		30	
31		31	A/Q Q0
32		32	
33		33	
P2A34		P2B34	

TABLE 8-4. PIN LIST - Q CHANNEL - OUTPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1		P1B1	STORAGE PARERR
2	PRØTECT FAULT	2	
3	DATA	3	$\overline{\text{UPPxT}}$
4	$\overline{\text{LØWXT}}$	4	LØST DATA
5	$\overline{\text{CLRLØWER}}$	5	
6	UPPER	6	
7		7	$\overline{\text{TRANS}}$
8		8	$\overline{\text{INCCA}}$
9		9	$\overline{\text{BUF 2FULL}}\cdot\text{WMØT}$
10	$\overline{\text{LØCKØUT}}$	10	
11		11	
12		12	
13	$\overline{\text{STWCRC}}$	13	TTBUSY
14		14	
15		15	
16	$\overline{\text{LØST DATA}}$	16	AL1
17	$\overline{\text{REQ}}$	17	
18	SCAN IN	18	
19	$\overline{\text{DSA WRENABLE}}$	19	
20	$\overline{\text{DSA REQUEST}}$	20	$\overline{\text{BUF I/Ø}}$
21	$\overline{\text{STOP DISTANCE}}$	21	$\overline{\text{A/Q CHARINPUT}}$
22		22	$\overline{\text{DSA PRIØRITY}}$
23	$\overline{\text{DSAWREN}}$	23	
24		24	
25		25	
26	LRCC STATE	26	$\overline{\text{RES1.1}}$
27		27	
28		28	$\overline{\text{ENA}}$
29		29	
30		30	
31	$\overline{\text{CRCC STATE}}$	31	
32		32	
33		33	
P1A34		P1B34	

(CONT.)

TABLE 8-4. PIN LIST - Q CHANNEL - OUTPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1	STRMF	P2B1	
2	CONTACT	2	
3		3	USA
4		4	WMØT
5	RMØT	5	
6		6	
7		7	
8		8	
9	STRBUF	9	STRINT
10	EØP	10	
11	SEL A1	11	SEL A0
12		12	
13		13	STRCF
14	A/Q REJECT	14	A/Q REPLY
15	STRUS	15	
16	A/Q INTERRUPT	16	
17		17	
18	DSA PRØTECT	18	
19		19	LDLWA
20		20	
21		21	
22	T2	22	
23		23	
24		24	
25		25	
26	SCAN FOR ØUT	26	
27	SCAN REV IN	27	
28		28	
29	4 MHZ	29	T3
30	T1	30	T4
31		31	
32		32	
33		33	
P2A34		P2B34	

TABLE 8-5. PIN LIST - LOWER DATA SECTION-INPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1		P1B1	RD TAPE 3
2	LØWERX1	2	RD TAPE 0
3	RD TAPE 1	3	TRANS
4	RD TAPE 2	4	RD TAPE 7
5		5	
6	RMØT	6	RD TAPE 4
7	RD TAPE 5	7	
8		8	
9		9	LDLWA
10		10	
11		11	
12		12	
13		13	
14		14	BUF I/Ø
15		15	
16		16	
17		17	
18		18	INCCA
19		19	
20		20	
21		21	
22		22	BUF
23		23	
24		24	
25	SEL A0	25	
26		26	
27	SEL A1	27	
28		28	BUSY
29		29	
30	EØG	30	
31		31	
32		32	
33		33	
P1A34		P1B34	

(CONT.)

TABLE 8-5. PIN LIST - LOWER DATA SECTION - INPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1	$\overline{\text{CØNTACT}}$	P2B1	BØT
2	CLRLØWER	2	
3		3	ILLUSCØPE
4		4	STRCF
5	$\overline{\text{WREQUEST}}$	5	
6		6	PE START
7	STRUS	7	$\overline{\text{PC 1600}}$
8	WENABLE	8	$\overline{\text{PE WARNING}}$
9		9	
10	STRINT	10	
11		11	$\overline{\text{A/Q MC}}$
12	LØST DATA	12	T3
13	EØP	13	
14		14	(Q)DATA
15		15	STRINT
16		16	
17		17	$\overline{\text{REQ}}$
18	PARITY ERR	18	FM/TM (T1)
19		19	$\overline{\text{TTDS}}$
20		20	$\overline{\text{ENA}}$
21	$\overline{\text{AL2}}$	21	
22	$\overline{\text{RWLD+RWUNLD}}$	22	$\overline{\text{AL1}}$
23	$\overline{\text{LØST DATA}}$	23	$\overline{\text{EØT}}$ (UP)
24		24	T1
25		25	
26		26	$\overline{\text{RWLD}}$
27	VS1	27	VS0
28	$\overline{\text{RES2}}$	28	
29		29	KUTY1
30		30	PE LØST DATA
31		31	
32		32	
33		33	
P2A34		P2B34	

TABLE 8-6. PIN LIST - LOWER DATA SECTION - OUTPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1		P1B1	
2	DSA ADDR 1	2	
3		3	
4	DSA ADDR 6	4	
5	DSA ADDR 2	5	DSA ADDR 0
6		6	
7		7	
8	WRTAPE 0	8	DSA ADDR 4
9		9	
10	DSA DATA 1	10	DSA DATA 2
11	WR TAPE 3	11	
12	DSA DATA 0	12	DSA DATA 3
13	A=B	13	DSA DATA 5
14	WRTAPE 5	14	
15		15	DSA DATA 4
16		16	WRTAPE 4
17	WRTAPE 6	17	
18		18	A7
19	$\overline{\text{A/Q A6}}$	19	$\overline{\text{A/Q A5}}$
20	$\overline{\text{A/Q A4}}$	20	$\overline{\text{A/Q A7}}$
21	$\overline{\text{A/Q A2}}$	21	$\overline{\text{A/Q A3}}$
22	WRTAPE 1	22	
23		23	DSA ADDR 3
24	WRTAPE 7	24	$\overline{\text{9T}}$
25		25	DSA ADDR 7
26	DSA ADDR 5	26	ALARM
27	WRTAPE 2	27	
28		28	
29		29	$\overline{\text{A/Q A0}}$
30	$\overline{\text{A/Q A1}}$	30	
31	PEENABLE	31	
32		32	
33		33	
P1A34		P1B34	

(CONT.)

TABLE 8-6. PIN LIST - LOWER DATA SECTION - OUTPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1		P2B1	
2		2	LEGUS
3		3	
4	800 BPI	4	
5		5	1600 BPI
6	WRITE CLK	6	
7		7	
8		8	
9	$\overline{\text{MC}}$	9	WDSHIFTED
10		10	EARLY WDS
11	$\overline{\text{RES T}}$	11	
12		12	2FCW
13		13	A/D
14	BCD	14	
15	$\overline{\text{MØDSEL}}$	15	INTERRUPT
16		16	
17	$\overline{\text{READY RWLD}}$	17	
18		18	
19		19	
20		20	
21		21	
22		22	
23		23	
24		24	
25	PRØTECTED	25	GAPCLK
26	9T	26	
27		27	
28		28	TT READY
29	PE CHARCLK	29	
30	PE CLØCK	30	
31		31	PE ENABLE
32		32	
33		33	
P2A34	75 IPS	P2B34	

TABLE 8-7. PIN LIST - TAPE INTERFACE - INPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1	PRDØUT 1	P1B1	PRDØUT 5
2		2	
3	PRDØUT 0	3	PRDØUT 4
4		4	
5		5	(LØ)1600
6		6	PRDØUT 2
7		7	PRDØUT 3
8		8	PRDØUT 6
9		9	PRDØUT 7
10	WMØT	10	
11		11	
12		12	
13		13	
14		14	
15		15	
16	PWDIN 0	16	
17	BCD	17	
18		18	PWDINP
19	WRTAPE 5	19	
20	WRTAPE 4	20	WRTAPE 13
21	WRTAPE 1	21	WRTAPE 12
22	WRTAPE 0	22	WRTAPE 9
23	WRTAPE 7	23	WRTAPE 8
24	WRTAPE 6	24	WRTAPE 15
25		25	WRTAPE 14
26	WRTAPE 10	26	WRTAPE 2
27		27	WRTAPE 11
28	9T	28	
29		29	$\overline{\text{PE PAR ER}}$
30	2FWC	30	RMØT
31	$\overline{\text{RES2}}$	31	A/D
32		32	
33		33	
P1A34		P1B34	

(CONT.)

TABLE 8-7. PIN LIST - TAPE INTERFACE - INPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1	PSFM	P2B1	WFM/TM(UP)
2	TTRDS	2	REV
3		3	EØP
4	TTRDP	4	
5	STWCRC(Q)	5	4 MHZ(Q)
6		6	
7	TTRD3	7	
8	TTRD2	8	PWØUT1(PE)
9	TTRD4	9	PWØUT0(PE)
10	TTRD5	10	SFM(UP)
11		11	
12		12	
13	PWØUT 2(PE)	13	PWØUT 2(PE)
14	TTRD6	14	
15		15	
16		16	EØRS
17	TTRD7	17	
18	LRCC STATE(Q)	18	PWØUT 18(PE)
19		19	WRITE CLOCK
20		20	PWØUT 4(PE)
21	TTRD1	21	
22	TTRD10	22	PWØUT 7(PE)
23		23	PWØUTP(PE)
24		24	PWØUT 6(PE)
25		25	PRSTRØBE(PE)
26		26	PWRESET(PE)
27		27	PWCLR(PE)
28		28	RWUNLD
29		29	RWLD
30		30	CRCC STATE(Q)
31		31	MØDSEL
32		32	
33		33	
P2A34		P2B34	

TABLE 8-8. PIN LIST - TAPE INTERFACE - OUTPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1	RDTAPE1	P1B1	
2		2	RDTAPE 5
3		3	
4	RDTAPE 0	4	RDTAPE 4
5	RDTAPE 2	5	
6	RDTAPE 3	6	
7	RDTAPE 6	7	
8	RDTAPE 7	8	
9	PWDIN 1	9	
10		10	PWDIN 3
11	PRIN 0	11	
12	PRIN 6	12	PRIN 1
13	PRIN 5	13	PRIN 4
14	PRIN 2	14	PRIN 7
15	PWDIN 4	15	PRIN 3
16	PWDIN 0	16	PWDIN 2
17		17	PWDIN 5
18	PWDIN 7	18	PWDIN P
19		19	PWDIN 6
20		20	
21		21	
22		22	
23		23	
24		24	
25		25	
26		26	
27		27	
28		28	FILL
29		29	
30		30	
31		31	
32		32	
33		33	
P1A34		P1B34	

(CONT.)

TABLE 8-8. PIN LIST - TAPE INTERFACE - OUTPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1		P2B1	
2		2	
3		3	
4		4	
5		5	
6	$\overline{\text{TTWD6}}$	6	
7		7	$\overline{\text{SEØP}}$
8		8	
9		9	
10		10	
11	$\overline{\text{TTWD7}}$	11	
12	$\overline{\text{TTWD4}}$	12	ISTSP
13		13	
14		14	$\overline{\text{RWND + RWNDUL}}$
15	$\overline{\text{TTWD5}}$	15	FM/TM(STATUS)
16	$\overline{\text{TTWD2}}$	16	
17		17	PARERR
18		18	
19	$\overline{\text{TTWD3}}$	19	
20	$\overline{\text{TTWDO}}$	20	
21		21	
22		22	
23	$\overline{\text{TTWD1}}$	23	
24	$\overline{\text{TTWRESET}}$	24	
25	RDS	25	
26	$\overline{\text{TTWDS}}$	26	
27	$\overline{\text{TTWDP}}$	27	
28	$\overline{\text{TTRWLD}}$	28	
29	$\overline{\text{TTRWULD}}$	29	
30	TTMØDSEL	30	
31		31	
32		32	
33		33	
P2A34		P2B34	

TABLE 8-9. PIN LIST - UPPER DATA SECTION - INPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1	RD TAPE 3(T1)	P1B1	RD TAPE 2(T1)
2	RD TAPE 0(T1)	2	$\overline{\text{UPPXT}}$
3	$\overline{\text{TRANS}}$ (Q)	3	RD TAPE 1(T1)
4	RD TAPE 6(T1)	4	RD TAPE 7(T1)
5		5	
6	RD TAPE 4(T1)	6	
7	$\overline{\text{RES1.1}}$	7	RD TAPE 5(T1)
8		8	
9	$\overline{\text{LDLWA}}$	9	
10		10	
11		11	
12		12	
13		13	
14		14	$\overline{\text{BUF I/Ø}}$
15		15	
16		16	
17	$\overline{\text{CARCURADR}}$	17	A=B
18		18	
19		19	
20		20	
21	(Q)$\overline{\text{STRBUF}}$	21	
22		22	
23		23	(T1)PAPER
24		24	FM/TM(T1)
25	(Q)SEL A0	25	
26		26	
27	(Q)SEL A1	27	
28		28	
29		29	
30		30	
31	(Q)STRUS	31	
32		32	
33		33	
P1A34		P1B34	

(CONT.)

TABLE 8-9. PIN LIST - UPPER DATA SECTION - INPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1	PE EØP	P2B1	
2	TT BØT	2	
3		3	(T1)FILL
4		4	
5		5	
6		6	
7	BUSY	7	(Q)STRMF
8		8	A7
9	(Q)USA	9	
10		10	
11		11	
12		12	A/D
13	PRØTECT FAULT(Q)	13	STORAGE PARITY ERROR
14	(Q)LØCKØUT	14	(PE) ID ABØRT
15		15	
16	FILE PRØTECT	16	
17		17	TT BUSY
18	TT EØT	18	
19	T3(Q)	19	
20		20	
21	9T	21	
22		22	
23		23	
24		24	
25		25	
26		26	
27		27	
28	TT READY	28	GAP CLØCK
29	(Q) REQ	29	ENA
30		30	DSAWRBII(Q)
31		31	STØP DISTANCE
32		32	
33		33	
P2A34		P2B34	

TABLE 8-10. PIN LIST - UPPER DATA SECTION - OUTPUT SIGNALS

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1		P1B1	
2		2	
3		3	
4		4	
5	DSA ADDR 8	5	DSA ADDR 10
6		6	
7		7	
8	DSA ADDR 12	8	WR TAPE 8
9		9	DSA ADDR 14
10	DSA DATA 10	10	DSA DATA 9
11	WR TAPE 11	11	
12	DSA DATA 11	12	DSA DATA 8
13	WR TAPE 13	13	LAST WØRD
14	DSA DATA 15	14	
15	DSA DATA 14	15	DSA DATA 12
16	WR TAPE 14	16	WR TAPE 12
17		17	
18	$\overline{\text{A/Q A13}}$	18	$\overline{\text{A/Q A14}}$
19	$\overline{\text{A/Q A15}}$	19	$\overline{\text{A/Q A12}}$
20	$\overline{\text{A/Q A11}}$	20	$\overline{\text{A/Q A10}}$
21		21	WR TAPE 9
22	DSA ADDR 9	22	$\overline{\text{A/Q A9}}$
23	DSA ADDR 11	23	
24	WR TAPE 15	24	
25		25	DSA ADDR 15
26	DSA ADDR 13	26	DSA DATA 13
27		27	WR TAPE 10
28	CØNTACT	28	EØT
29		29	$\overline{\text{A/Q A8}}$
30	WENABLE	30	ILLUSCØDE
31		31	
32		32	
33		33	
P1A 34		P1B 34	

(CONT.)

TABLE 8-10. PIN LIST - UPPER DATA SECTION - OUTPUT SIGNALS (CONT'D)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1		P2B1	EØP
2		2	
3		3	
4		4	START
5	FØR	5	RES 2
6	READ THRESHOLD	6	REV
7		7	
8	TT REV	8	
9		9	USO
10	TT FØR	10	
11	TT SELECT 3	11	UST
12	TTUST	12	LEGCF
13		13	
14		14	
15	TT USO	15	RWLD
16		16	STØP
17	WREQUEST	17	
18		18	SMF
19		19	BØT
20	TT SWS	20	PE BØT
21		21	
22	RWUNLD	22	LEGMF
23		23	START
24		24	WMØT
25	RMØT	25	WFM
26	SELECT 3	26	GC128
27	EØG	27	EØT
28		28	
29		29	
30	PEID	30	
31		31	
32		32	
33		33	
P2A34		P2B34	

COMMENT SHEET

MANUAL TITLE MAGNETIC TAPE TRANSPORT CONTROLLERS
FA442-A (ICL) and FA446-A (LCTT)

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