CONTROL DATA
CORPORATION

CONTROL DATA®
1700 COMPUTER SYSTEM

1716–A COUPLING DATA CHANNEL REFERENCE MANUAL

REVISION RECORD

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A	Manual released; this manual supersedes the 1716-A Coupling Data Channel section of the
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PREFACE

This manual gives reference information for the CONTROL DATA® 1716-A Coupling Data Channel which may be used in conjunction with the 1705 Interrupt Data Channel of the 1700 Computer. For reference information on 1700 Basic Peripheral Equipments (which attach directly to the 1704 Basic Computer) see the 1700 Computer System Reference Manual, Pub. No. 60153100.

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1716 COUPLING DATA CHANNEL

INTRODUCTION

This section describes the CONTROL DATA* 1716-A Coupling Data Channel, its physical system and programming information. There is no operating information, as there are no controls or indicators on the 1716 other than the Program Protect Switches, which are covered under Program Protection.

FUNCTIONAL DESCRIPTION

System Relationship

The 1716 provides a bidirectional 16-bit data path between two 1704 Computers, each with a 1705 Interrupt Data Channel. It also provides a Buffered Data Channel to which may be attached up to eight peripheral equipments. Figure 1 shows the relationship between the 1716 and other equipments.

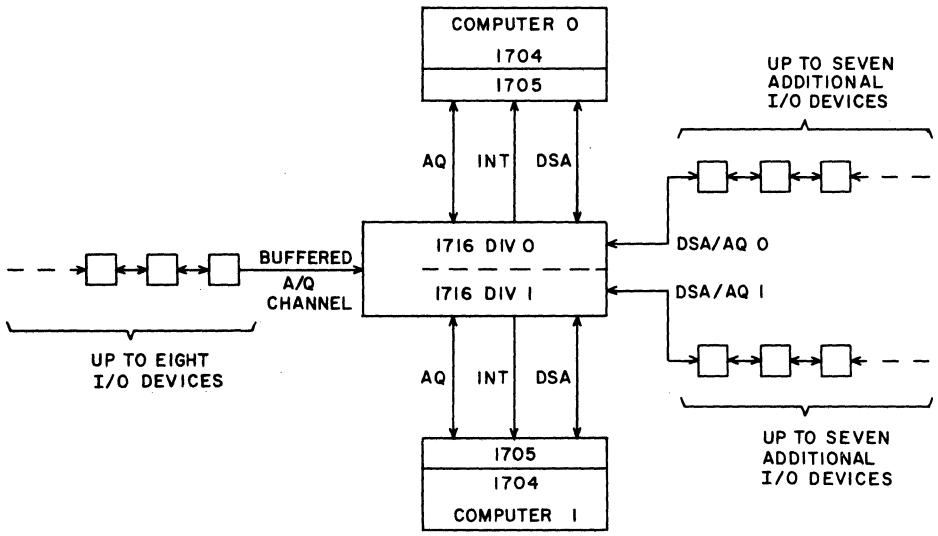

Figure 1. Typical 1716 Configuration

The 1716 is divided into two sections, called division 0 and division 1. Each of these sections is connected to a 1705 Interrupt Data Channel and a 1704 computer. The computer attached to division 0 will be called computer 0, the one on division one, computer 1. A maximum of three 1716's may be connected to a 1705 Interrupt Data channel. A 1706 Buffered Data Channel may replace any or all of the 1716's.

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With the exception of the Program Protect switches, the 1716 is controlled entirely by the Input to A and Output from A instructions from the 1704. The operations for the 1716 are the same as those for the 1706 BDC, with the addition of a Buffered Transfer operation. This operation allows the sending of data directly between the storage of the two connected computers, or from one portion of one computer's storage to another portion of the same computer's storage. In response to an I/O instruction from either computer (and the contents of the respective Q registers) the 1716 connects the computer to the other computer, or to one of the peripheral equipments, and sends the appropriate Read or Write signal; it then controls the transfer of the information. On buffered operations, the 1716 obtains access to storage through the Direct Storage Access Bus of either computer. Either computer 0 access or computer 1 access can be disabled. If an access is disabled, no signals can be sent from the 1716 via the access that is disabled.

Power is supplied to the Direct Storage Access (DSA) distributed scanner stages in the 1716 (one for each 1700 attached to the 1716) from the terminator power. In dual 1700 Systems if power is lost on one system (which also drops power to the 1716) the other system will remain operable. To remain operable, its DSA distributed scanner (one stage in the 1716) will continue to run. Each stage of DSA Scanner in the 1716 has power supplied to it when the computer associated with that access has power up. The terminator power supplies are directly tied together in a dual 1700 system.

Interrupt

The 1716 has one interrupt line to each computer. The interrupts are generated by End of Operation (if enabled) or by matching conditions in the flag and mask bits. The End of Operation interrupt is sent to the computer that initiated the operation. The Flag/Mask interrupt is sent to the computer having a mask bit matching the corresponding flag bit. The flags are shared while each computer has its own mask bits. Use of the interrupt conditions is explained in detail under the Function operation.

Program Protection

The 1716 has two Program Protect switches, one associated with each division. When a switch is ON, only those I/O instructions having a "1" on the protect line will be recognized. An instruction not having a "1" on the protect line will be rejected. The Function instruction will not be rejected; it will be ignored. When the switch is OFF, protected and unprotected instructions will be recognized.

Reply/Reject

The 1716 responds within 4 microseconds to an Input to A or Output from A instruction with either a Reply or a Reject signal. A Reply will be sent whenever the computer can perform the requested operation. The following conditions will cause a Reject to be sent:

1) a program protect violation
2) the 1716 is Busy (if attempting a direct or buffered operation)
3) a device returns a Reject (direct output or input)

If the computer receives no response, it will generate an internal Reject. Function is not rejected on a program protect violation.

PROGRAMMING

Summary of Programming Information

Tables 1, 2, and 3 are a summary of the information necessary to program the 1716. Explanations of the information presented here can be found in the following sections. The tables here are intended as a quick reference for the experienced programmer, and a summary for the reader interested in the general programming capabilities of the 1716.

TABLE 1. 1716 ADDRESSES AND OPERATIONS

W*			COMPUTER INSTRUCTION	
1716 #3	1716 #2	1716 #1	INPUT TO A	OUTPUT FROM A
0B	06	01		Buffered Transfer
0C	07	02	Direct Input	Direct Output
0D	08	03	Terminate Buffer 1716 Current Address	Function (See 1716 Function Table)
0E	09	04	1716 Status	Buffered Output
0F	0A	05	1716 Current Address	Buffered Input

*The left digit is binary, the right digit hexidecimal.

TABLE 2. 1716 FUNCTIONS

BIT IN A REGISTER	MEANING
A15=1	Set condition for ones in A14-A00*
A15=0	Clear condition for ones in A14-A00*
A14	Flag 4
A13	Flag 3
A12	Flag 2
A11	Flag 1
A10	Flag 0
A09	Mask 4
A08	Mask 3
A07	Mask 2
A06	Mask 1
A05	Mask 0
A04	(Not defined)
A03	Reserve flag
A02	(Not defined)
A01	(Not defined)
A00	Interrupt on 1716 End of Operation*

*Functions also used in the 1706.

TABLE 3. 1716 STATUS BITS

BIT SET IN A REGISTER	MEANING
15	(Not used)
14	Flag 4
13	Flag 3
12	Flag 2
11	Flag 1
10	Flag 0
9	Device Reply*
8	Device Reject*
7	(Not used)
6	Program Protect Fault*
5	(Not used)
4	End of Operation*
3	Reserve Flag
2	Interrupt*
1	Busy*
0	Ready*

*Status also used in the 1706.

Addresses

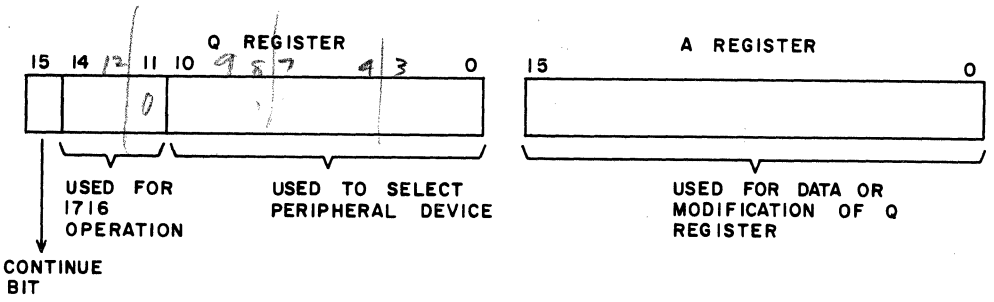


Figure 2. 1700 Q and A Registers

Bits 11-15 of the Q register are used to select the desired 1716 operation, while bits 00-10 are used to select the desired peripheral device. (See Figure 2). The 1716 provides a W = 0 signal to devices connected to it. Bits 11-14 are used to define 1716 operations (see Table 1) and bit 15 is the continue bit, * used as follows:

1) Address the device with Q15 = 0 and the remainder of Q set to select that device; the device is then connected.

2) All succeeding addresses with Q15 = 1 will be recognized by this device. Thus 15 bits of addressing are available to the device.

3) The next address with Q15 = 0 will disconnect the device unless it is the address of that device.

The 1716 will interpret an address with Q15 = 1 as a direct input on an Input to A instruction, and as a direct output on an Output from A instruction.

Operations

Besides selecting a particular 1716, the W field of Q, combined with a 1704 Input to A or Output from A instruction, specifies an operation. The Function operation may be further modified by the contents of the A register. Tables 1 and 2 list the addresses, operations, and functions. Because W is a 5-bit field and bit 15 is used as a Continue bit, W is expressed as a 2-digit number: the right digit is hexadecimal (4 bits), the left digit binary (1 bit).

Operations Defined by W and Input to A

Direct Input: Whenever the computer executes an Input to A instruction to a 1716 with the W field of Q selecting a direct input, Q is stored in the 1716 and presented to the devices attached to the 1716 and one 16-bit word is transferred into the A register from the selected device. The word may be a data word or the status of a device on the 1716. This mode of operation is in every way identical to that of the AQ channel. The Continue bit functions as described previously. If an attempt is made to do a direct input when the 1716 is busy, the 1716 will respond with a Reject. It is therefore impossible to status a device on the 1716 during a buffered operation.

*This only on certain devices. The 1718 is one such device.

*Terminate Buffer, 1716 Current Address: This terminates a buffered operation and loads the current address of the word being transferred into the A register. This instruction is intended to terminate hung-up input buffers, and in this case the A register will contain the address of the next word to be transferred. Otherwise, the address sent may be either that of the last word or the next word. Which one will depend on the timing of the 1704/1716 device; i. e., when the instruction reaches the 1716. Terminate Buffer instruction will not clear RESERVE FLAGS if bit zero of the Q register of the computer executing the instruction is set when the instruction is executed.

1716 Status: This operation will load the status word from the 1716 into the A Register of the computer. Table 3 lists the bits in the status word. The following list explains their meaning.

Flag 4 (Bit 14 = 1) - Shared flag 4 is set.**
Flag 3 (Bit 13 = 1) - Shared flag 3 is set.
Flag 2 (Bit 12 = 1) - Shared flag 2 is set.
Flag 1 (Bit 11 = 1) - Shared flag 1 is set.
Flag 0 (Bit 10 - 1) - Shared flag 0 is set.

Device Reply (Bit 9 = 1) - The peripheral device accepted the last word transfer attempted from the 1716.

Device Reject (Bit 8 = 1) - The peripheral device rejected the last word transfer attempted from the 1716.

Program Protect Fault (Bit 6 = 1) - A reference to computer storage has caused a program protect violation.

End Of Operation (Bit 4 = 1) - A buffered input, output, or transfer has been completed.

Reserve Flag (Bit 3 = 1) - The reserve flag for this computer is set. This indicates that the other computer is not using the 1716.

Interrupt (Bit 2 = 1) - An interrupt has been sent from the 1716 to the computer.

Busy (Bit 1 = 1) - This bit is set from the time the 1716 accepts an output word from the computer initiating a block transfer until the transfer is completed, or during a direct input or output operation.

Ready (Bit 0 = 1) - The power is on.

1716 Current Address: This code will cause the address of the current word being transferred on a buffered operation to be loaded into the A register of the computer requesting the status. This same word is also loaded into the A register following a Terminate Buffer operation.

NOTE

Status requests are never rejected on the 1716 unless a program protect violation has occurred.

*Terminate buffer operation will cause the 1716 to remain busy for 10 μsec.

**Flags are explained in more detail under 1716 Function.

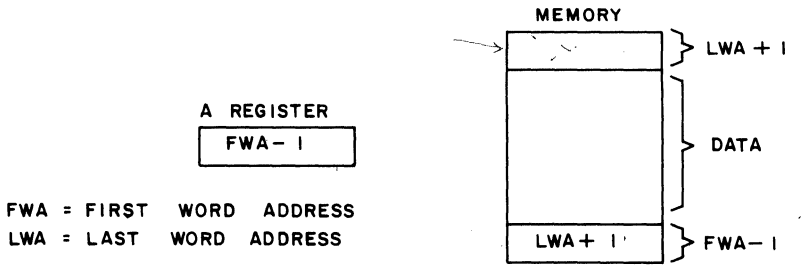


Figure 3. Address Arrangement for Buffered Input and Output

Buffered Output: A buffered output is initiated when the computer executes an Output from A instruction and the W field of Q selects a buffered output. (See Figure 3.) Q is stored in the 1716, then placed on the 1716 channel, and the contents of A is transferred to the 1716. The contents of A specifies the first word address minus one (FWA-1) of the block to be transferred. The contents of location FWA-1 specifies the last word address plus one (LWA+1) of the block to be transferred. The 1716 begins the data transfer by raising the Write signal to the device. The device responds within four microseconds by raising the Reply signal to the 1716. The 1716 then advances to the next data word, repeating this cycle until the block of data has been transferred.

If the 1716 receives a Reject, it indefinitely repeats the transfer of the word until the word is accepted. The address is not reissued to storage. The 1716 does not generate an internal reject. If an attempt is made to establish a buffered output when the 1716 is busy, the 1716 responds with a Reject.

Buffered Input: A buffered input is initiated when the computer executes an Output from A instruction and the W field of Q selects a buffered input. (See Figure 3.) Q is stored in the 1716, then placed on the 1716 channel and the contents of A is transferred to the 1716. The contents of A specifies the location of the first word address minus one (FWA-1) of the block where the data is to be stored. The contents of the location FWA-1 specifies the last word address plus one (LWA+1) of this block. The 1716 begins the data transfer by raising the Read signal to the device. The device responds within four microseconds by raising the Reply signal to the 1716. The 1716 then advances to the next data word and repeats this cycle until the block of data has been transferred.

If the 1716 receives a Reject from the device, it repeats the transfer of the word indefinitely until the word is accepted. The 1716 does not generate an internal reject. If an attempt is made to establish a buffered input when the 1716 is busy, the 1716 will respond with a Reject.

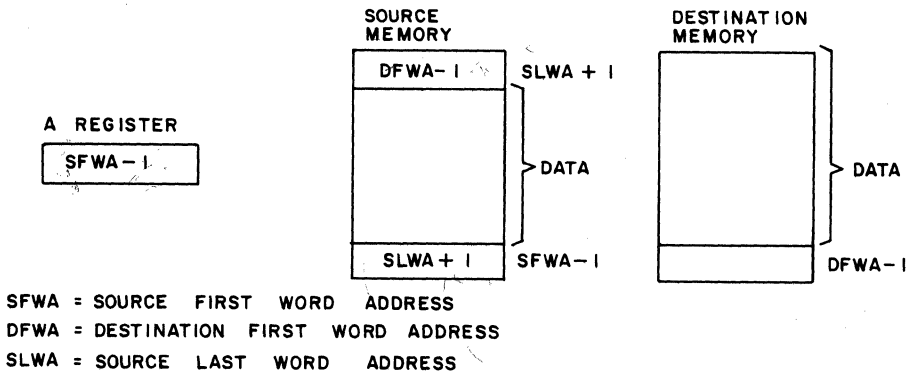


Figure 4. Address Arrangement for Buffered Transfer

Buffered Transfer: In this mode, data is transferred directly to/from computer core storage via the 1716 (see Figure 4). The transfer is initiated by one computer executing an Output from A instruction with the W field of Q selecting a buffered transfer (see Table 4). The transfer is accomplished by defining the bounds of the source data and the FWA-1 of the destination location. The output to the 1716 initiates the buffer transfer and sends via the A register the source data FWA-1 (SFWA-1). The contents of SFWA-1 is the source data LWA+1 (SLWA+1). The contents of SLWA+1 is the destination data FWA-1 (DFWA-1). Bit 15 of all these addresses refers to the "other" computer if it is set; "this" computer if not set. It is thus possible to make a block transfer within a single computer's core storage. All flag, mask, and status functions of the 1716 are availabe in the buffer transfer mode. The 1716 will have a Buffered Transfer Protect Switch associated with each computer access. When the switch is on, the protect line to the 1700 Direct Storage Access is disabled during a Buffered Transfer operation only. In this mode data can be transferred only into the unprotected memory of the destination computer.

1704 Instruction	Q Register	Step	Action
LDQ	Selected 1716 Status Request	1)	Initiate operating status check of desired 1716.
INP		2)	A register now contains the operating status of the desired 1716.
		3)	Check status in A for Ready and Not Busy.
LDQ	Selected 1716 Function	4)	Initiate setting of reserve flag.
LDA		5)	Set reserve flag.
OUT		6)	If reserve flag is available, it will be set.
		7)	Repeat 1-3 to check for reserve flag set. If not set, wait and repeat 1-6.
LDQ	W = Direct Input on selected 1716, Bits 0-10 specify status request for equipment	8)	Initiate status check of equipment to be used.
INP		9)	A register now contains the equipment status.
		10)	Check equipment status for desired conditions.
		11)	Repeat 8-10 for station and unit, if necessary.
LDQ	Selected 1716 Function	12)	Initiate selection or clearing of Interrupt on End of Operation.
LDA		13)	Load A with desired operation.
OUT		14)	Interrupt on End of Operation is now enabled or disabled. Any existing interrupt is cleared.
LDQ	W = Direct Output on selected 1716. Bits 0-10 specify an operation on the equipment or station.	15)	Initiate selection of peripheral equipment operating conditions and interrupts.
LDA		16)	If necessary, load A with the code further specifying the operation indicated by (Q).
OUT		17)	Execute Output from A instruction
		18)	Repeat 15-17 until all desired operating conditions are specified.

1704 Instruction	Q Register	Step	Action
For a Direct Input or Output of Data			
LDQ	W = Direct Input or Direct Output on selected 1716. Bits 1-10 select equipment and station. Bit 0 = "0" for data transfer.	19D*)	Select desired type of I/O.
LDA		20D)	If doing a direct output, load the data into A; if direct input, skip this step.
INP or OUT		21D)	Execute 1704 Input to A or Output from A, depending on desired direction of data transfer.
		22D)	Skip to 22B.
For a Buffered Input or Output of Data			
LDQ	W = Buffered Input or Buffered Output on selected 1716. Bits 1-10 select equipment and station. Bit 0 = "0" for data transfer.	19B†)	Select desired type of buffered I/O.
LDA		20B)	Load A with the FWA-1 of the buffer area. The contents of memory at this address must contain the LWA + 1 of the buffer area.
OUT		21B)	The buffered transfer is now initiated and under control of the 1716.
		22B)	Status the converter (as in steps 1-3, checking for desired conditions, or by using the 1716 current address status) or proceed with the main program until an interrupt occurs. Using interrupts takes advantage of the capabilities of the buffered data channel to do I/O without hanging up the computer. It is not possible to status a device connected to the 1716 as long as the 1716 is Busy.

* D indicates a step for the direct transfer of data.

† B indicates a step for the buffered input or output of data.

Buffered Transfer

The buffered transfer is programmed in much the same way as the buffered input or buffered output. There are four basic transfers:

1) "this" computer to "this" computer
2) "this" computer to "other" computer
3) "other" computer to "this" computer
4) "other" computer to "other" computer

Bit 15 of the 3-address word determines the type of transfer.

1) this to this - Bit 15 of SFWA*, SLWA+1, and DFWA-1 is zero. This transfer can be used to relocate data in memory.

Computer 1 Computer 2

Q = W For Buffer XFER
A = | O | SFWA-11 |
INSTR = OUT

SFWA-1 | O | SLWA+1 |
DATA OUT
SLWA+1 | O | DFWA-1 |
DFWA | DATA IN |

2) this to other - Bit 15 of SFWA-1, SLWA+1 is zero. Bit 15 of DFWA-1 is one. This will transfer data to the other computer and store it beginning at DFWA.

Computer 1 Computer 2

Q = W For Buffer XFER
A = | O | SFWA-1 |
INSTR = OUT

SFWA-1 | O | SLWA+1 |
DATA OUT
SLWA+1 | 1 | DFWA-1 |

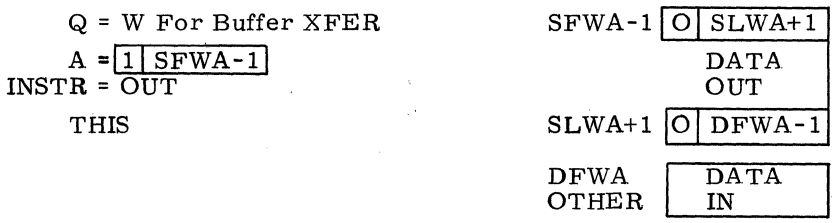
DFWA | DATA IN |

3) other to this - Bit 15 of S FWA-1 is a one, SLWA+1 is a zero. Bit 15 of DFWA-1 is one. This will move data from the other computer and store it in this computer, beginning at DFWA. Use of this transfer requires some prearranged programming so this computer knows where in the other computer the data to be transferred is located.

Computer 1 Computer 2

Q = W For Buffer XFER
A = | 1 | SFWA-1 |
INSTR = OUT

4) other to other - Bit 15 of SFWA-1 is a one, SLWA+1 is a zero. Bit 15 of DFWA-1 is a zero. This transfer will move data in the other computer's memory. This requires some prearranged programming so this computer knows where the other computer's data is initially



Because of the dependence of the buffered transfer on the system programming, no attempt is made to give a specific sample program. Cases 3 and 4 will not be discussed further because of the special programming required to execute such transfers.

Case 1: "This to this" requires no particular programming effort other than properly establishing the addresses, all with bit 15 equal to zero.

Case 2: "This to other" may be done without any special preparation by merely sending the data at any time to the other computer. It is preferable to send some control or identification word as part of the data to allow the other computer to determine its origin.

If some notification or communication is desired, the flags and masks may be used; this computer can send an interrupt to the other using the flag/mask interrupt, or the other computer can status the flags. Both methods require some prearranged meaning for the flag and mask bits. All mask, flag, and status functions are available to both computers during a buffered transfer.

* SFWA = Source First Word Address
SLWA = Source Last Word Address
DFWA = Destination First Word Address

If a buffered operation becomes hung up, LDQ with W selecting Terminate Buffer for the appropriate 1716, and execute an INP instruction. The buffered operation is terminated and the current address is sent to A. The program can check this address and take the desired action. Terminate Buffer instruction will not clear RESERVE FLAGS if bit zero of the Q register of the computer executing the instruction is set when the instruction is executed.

One method of determining if the 1716 is hung up is to select the device's Interrupt on End of Operation. When the interrupt is recognized, check the operating status of the 1716. If the 1716 is still Busy, the buffered operation is hung up. Do a status check of the 1716 current address. If the current address does not equal the LWA + 1, the equipment is hung up.

A second method is to do a status check of the 1716 current address. Then wait until at least one more word should have been transferred and again check the current address. If it is unchanged, the buffered operation is hung up. This method requires knowing instruction execution times and the rate of data transfer.

If an INP or OUT instruction results in a Reject, the program proceeds as described in connection with these instructions in the computer reference manual.

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