CONTROL DATA® BG504A-H DRUM MEMORY SUBSYSTEM

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
MAINTENANCE AIDS
PARTS DATA
WIRE LIST

CONTROL DATA CORPORATION

HARDWARE REFERENCE/
CUSTOMER ENGINEERING MANUAL

BG504A-H DRUM MEMORY SUBSYSTEM

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Section One

GENERAL DESCRIPTION

1.1 GENERAL

The BG504 is a single-rack, stand-alone drum memory subsystem providing fast access mass storage for Control Data 1700-series computers. The BG504 system configuration is shown in Figure 1.1.

Features Include:

- Single rack configuration.
- Compatible with SC1700, standard 1700, and 65K core 1700 computers.
- Storage capacities from 196,608 words to 1,572,864 words; field expandable (see Table 1.1).

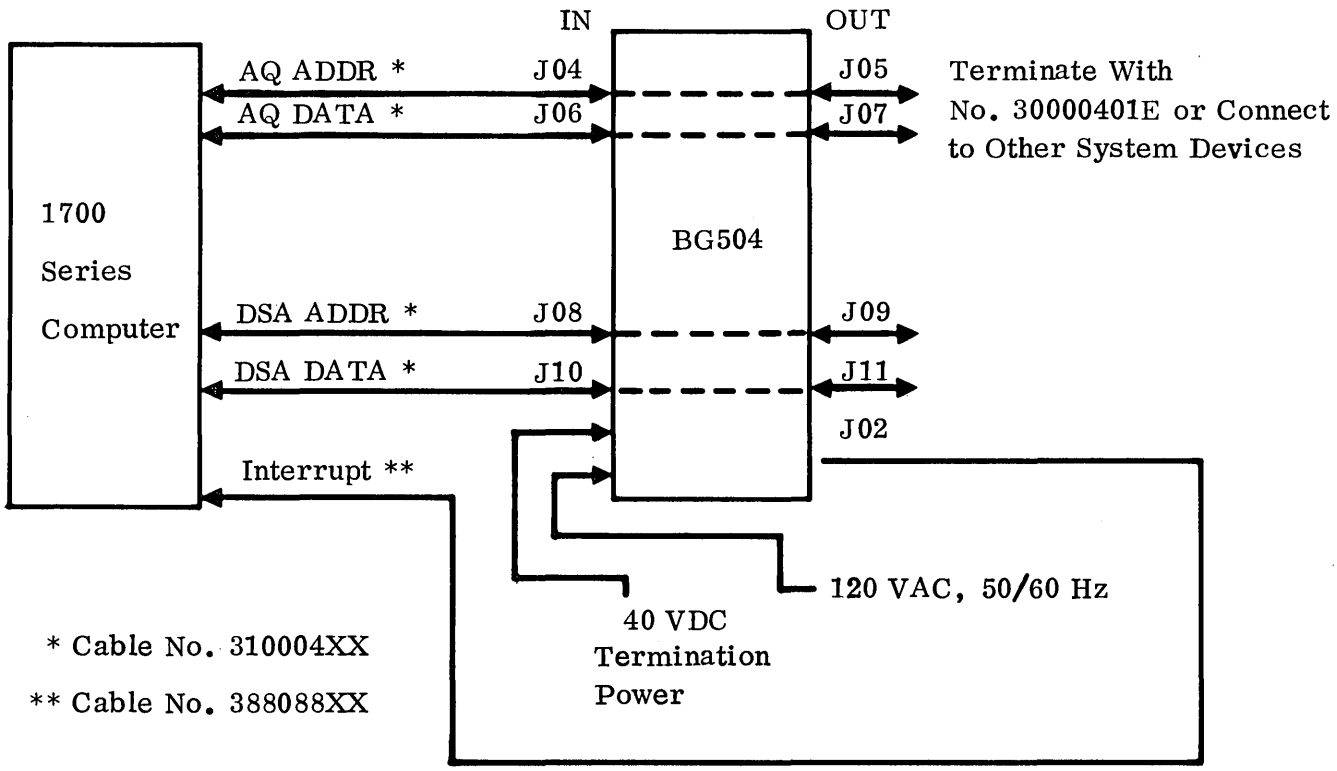


Figure 1.1. BG504 System Configuration

Table 1.1. BG504 Storage Capacities

PRODUCT NUMBER	EQUIPMENT NUMBER	ASSEMBLY NUMBER	DRUM MEMORY UNIT NUMBER	NUMBER OF WORDS	NUMBER OF SECTORS	NUMBER OF TRACKS	COMMENTS (1.)
1752-1	BG504-A	39744600	39668602	196,608	2,048	64	Field Expandable
	-B	39744601	03	393,216	4,096	128	
1752-2	-C	02	04	589,824	6,144	192	(2.)
	-D	03	05	786,432	8,192	256	
	-E	04	06	983,040	10,240	320	Field Expandable
1752-3	-F	05	07	1,179,648	12,288	384	
	-G	06	08	1,376,256	14,336	448	(2.)
1752-4	BG504-H	39744607	09	1,572,864	16,384	512	
QSE	QSE	QSE	10	1,769,472	18,432	576	Field Expandable
			11	1,966,080	20,480	640	3Ø Power
			12	2,162,688	22,528	704	Required (2.)
			13	2,359,296	24,576	768	
			14	2,555,904	26,624	832	Field Expandable
			15	2,752,512	28,672	896	3Ø Power
			16	2,949,120	30,720	960	Required (2.)
QSE	QSE	QSE	39668617	3,145,728	32,768	1024	

(1.) Field expandable in increments of 64 tracks

(2.) Expandable only within the group

- Single phase 120 vac, 50/60 Hz only primary power required.
- Access time: 8.7 milliseconds nominal; 17.4 milliseconds maximum (60 Hz power).
- Word transfer rate 183 kHz nominal (60 Hz power).
- Sector oriented hardware; driver accepts either sector or word address requests.
- Sector size: 96 data words plus one 16-bit checkword.
- Standard driver, MSOS system initializer, Olympus and Utopia modules, and SMM17 diagnostic available.
- High reliability: Gold-plated contacts and transistor - transistor logic (TTL) throughout controller, and drum. Drum is sealed in dry inert helium gas for long bearing life and full temperature operation.
- Autoloads first 1536 words from drum into core.
- Guarded address capability: No drum writing below selected track address; switch enabled; address determined by front plane U-jumpers (1 through 256 tracks can be guarded).
- Sector overrange detection: No Drum Write or Drum Read operation can be performed on non-existent sectors.
- UL listing
- No control words imbedded in data buffer; all control via computer AQ channel and all data transfer via computer direct storage access (DSA).
- Partial sector write feature: If fewer than 96 words are transferred into a sector, the area between last word and checkword is filled with zeros.

1.2 PHYSICAL DESCRIPTION

Major components for the BG504 are described in the following paragraphs.

1.2.1 RACK (39291400)

The BG504 is completely contained in one standard 19-inch rack. Nominal dimensions are: height, 75 inches; width, 24 inches; depth, 28 inches. Front and rear doors, and louvered-removable top are light gray; frame and removable sides, black-gray. Total uncrated BG504 weight is 730 pounds.

1.2.2 DRUM POWER SUPPLY PANEL (396686XX)

This 5.25-inch high module mounts in the top of the rack, and provides dc operating voltages for the drum memory unit.

1.2.3 CONTROLLER POWER SUPPLY PANEL (39738900)

Controller dc operating voltages are supplied by this 7-inch high module which mounts beneath the drum power supply panel.

1.2.4 DRUM CONTROLLER (39740900)

This 14-inch high double module mounts beneath the controller power supply panel. Thirty-nine logic cards plug into the front; each card edge has abundant test points. The rear panel contains A/Q, DSA, interrupt and other connectors. The panel is hinged to allow easy access to the wire-wrapped back-plane.

1.2.5 BLOWER (39514900)

The 5.25-inch high blower module mounts beneath the controller. It cools the rack with an upward directed airflow of 540 CFM. A self-contained filter is removable from the front.

1.2.6 DRUM MEMORY UNIT (396686XX)

The rotating fixed-head drum memory unit is mounted on slides near the bottom of the rack. Table 1.1 specifies standard available word sizes and field expandability (added head plates). Cable lengths allow drum operation with the slides extended. The drum may be removed from the rack by simply lifting it off the extended slides (slides extend only after blank front panels are removed).

1.2.7 POWER DISTRIBUTION BOX (39739400)

This assembly is mounted in the bottom of the rack and is accessible from the rear. All power and ground wiring is terminated by solderless connection to labeled terminal blocks located beneath a removable panel. Two circuit breakers function as separate power switches for the drum unit and controller/blower.

1.2.8 CONTROLS, INDICATORS, AND ADJUSTMENTS

Drum Unit Power Supply (P. S.) Panel Adjustments

Title	Description	Location
+25 vdc Adjustment	Potentiometer	Rear Access
+ 5 vdc Adjustment	Potentiometer	Rear Access
-12 vdc Adjustment	Potentiometer	Rear Access

Controller Power Supply (P.S.) Panel Adjustments

Title	Description	Location
+ 6 vdc Adjustment	Potentiometer	Rear Access
+ 5 vdc Adjustment	Potentiometer	Rear Access
- 6 vdc Adjustment	Potentiometer	Rear Access

Controller Controls, Indicators, and Adjustments

Title/Function	Description	Location
EQUIPMENT NUMBER	16-Position Thumb-wheel Switch	Card Position B36
AUTO LOAD	Pushbutton Switch	Card Position B36
PROGRAM PROTECT	Toggle Switch	Card Position B36
ENABLE GUARDED ADDRESS	Toggle Switch	Card Position B36
"DSA Scanner" Switch	5-Position Rotary Switch	Card Position B2
READY	Indicator	Card Position B36
BUSY	Indicator	Card Position B36
ALARM	Indicator	Card Position B36
WREN Adjustment	Potentiometer	Card Position A26
Clock Adjustment	Potentiometer	Card Position A26

Drum Memory Unit Controls and Indicators

Title/Function	Description	Location
MOTOR RESET	Pushbutton	Front Panel
Master/Spare Timing	Toggle Switch	Lower Front Access
MOTOR POWER ON	Indicator	Front Panel
SPEED LOW	Indicator	Front Panel
PUMP ON	Indicator	Front Panel
TEMP HIGH	Indicator	Front Panel
BOTTLE PRESSURE LOW	Indicator	Front Panel
Helium Atmos. Pressure	Guage	Front Panel
Helium Cylinder Pressure	Guage	Left Side Access

Power Distribution Box Controls

Title	Description	Location
DRUM	5 amp Circuit Breaker	Panel (Rear Access)
CONTROLLER/BLOWER	5 amp Circuit Breaker	Panel (Rear Access)

1.3 ELECTRICAL DESCRIPTION

1.3.1 PRIMARY POWER

BG504 AC Power

Unit	Maximum at 120 VAC, 50/60 Hz, Single Phase	Protection
Controller/P.S./Fan	2.5 amp	5-amp Circuit Breaker
Drum Unit/P.S.	3.5 amp	5-amp Circuit Breaker
BG504 Total	6.0 amp	-

1.3.2 DC POWER

Drum Memory Unit DC Power

Drum Memory Unit Requirements	Drum P.S. Panel Output
+25v ±5%, 2.0 amp Maximum	22-35v, 1.1 amp Minimum at 60°C
+ 5v ±5%, 4.0 amp Maximum	3-7v, 5.4 amp Minimum at 60°C
-12v ±5%, 1.5 amp Maximum	8 to -14 v, 1.8 amp Minimum at 60°C

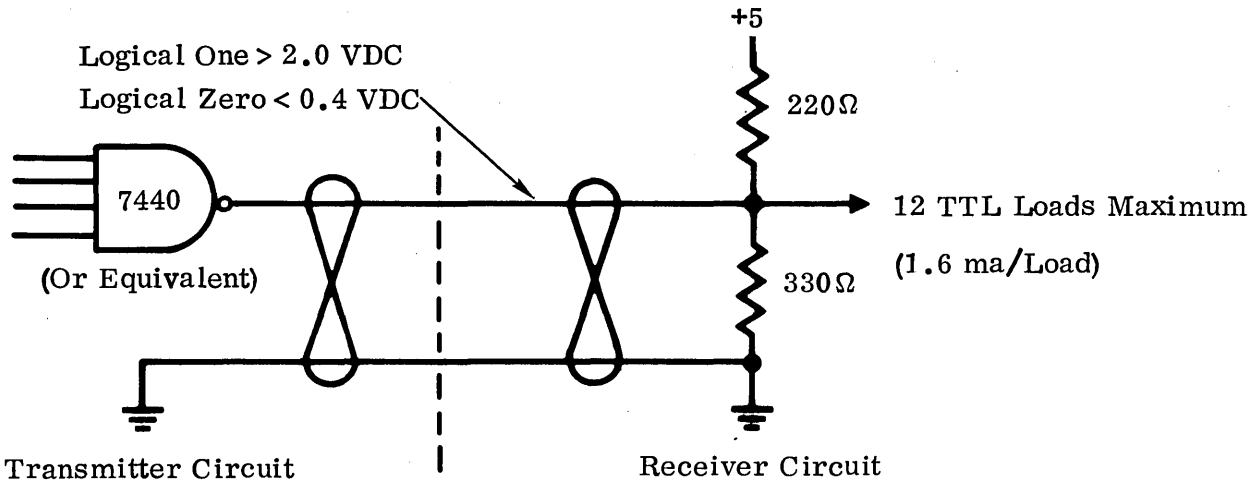
Controller DC Power

Each supply has short circuit and overvoltage protection.

Controller Requirements	Controller P.S. Panel Output
40v ±10%, Terminator Power	From Terminator Power Supply
+6v ±10%, 6.5 amp Maximum	+6 ±0.3v, 8.1 amp Minimum at 55°C
+5v ±5%, 4.5 amp Maximum	+5 ±0.25v, 8.5 amp Minimum at 55°C
-6v ±10%, 3.5 amp Maximum	-6 ±0.3v, 4.4 amp Minimum at 55°C

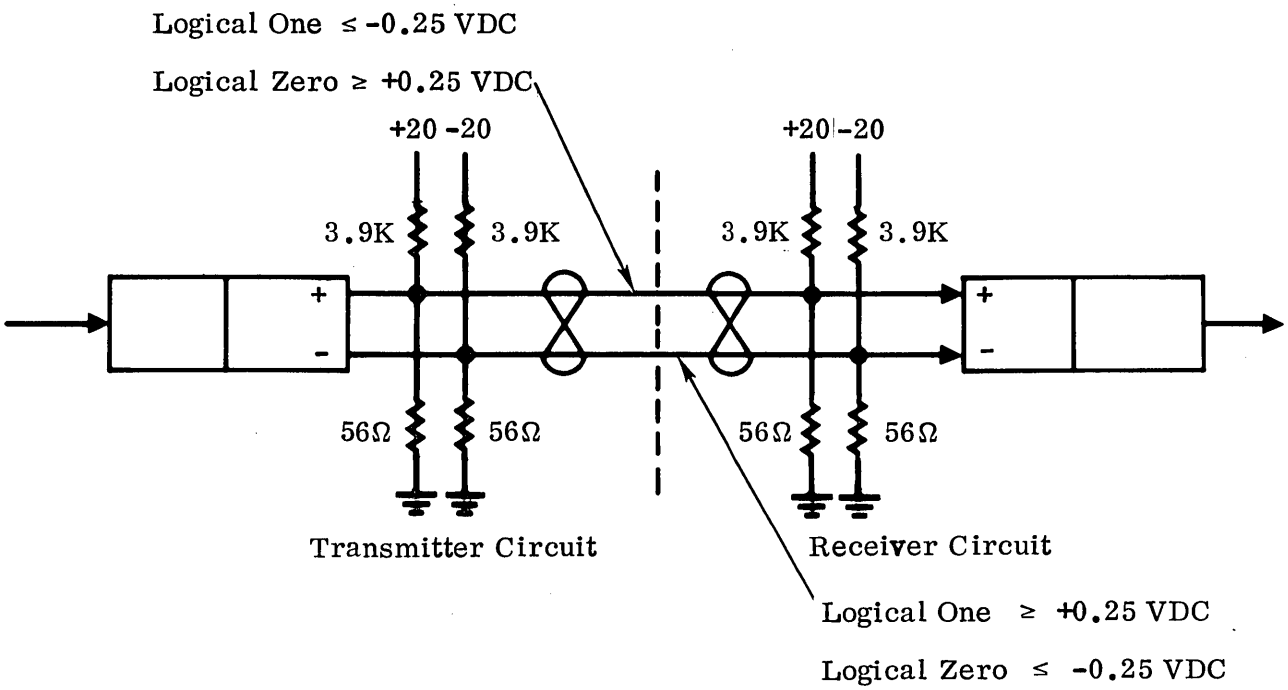
1.3.3 CONTROLLER/DRUM INTERFACE

Interface transmitter and receiver circuits are commercial 7400-series TTL. Schematically, these circuits are as follows:



1.3.4 CONTROLLER/CPU INTERFACE

Interface transmitter and receiver circuits are Control Data DTL Intebrid party-line IC's. Schematically, these circuits are as follows:



1.4 PERFORMANCE/CHARACTERISTICS SUMMARY

1.4.1 PERFORMANCE

1.4.1.1 Storage Capacity

Standard capacities from 196,608 words to 1,572,864 words in increments of 196,608 words (see Table 1.1).

1.4.1.2 Access Time

At 60 Hz power:

- 17.4 millisecond maximum
- 8.7 millisecond nominal

At 50 Hz power:

- 21.0 millisecond maximum
- 10.5 millisecond nominal

1.4.1.3 Word Transfer Rate

Data transfers bit - serially between the drum unit and controller at the following constant rates:

- 183 kHz nominal word transfer rate (60 Hz power).
- 153 kHz nominal word transfer rate (50 Hz power).

Computer/controller data transfers occur bit-parallel at the preceding rates on the average; however, the controller has double-buffering capability which permits word transfers to/from computer core on two consecutive core memory cycles. The BG504 never acquires more than two consecutive memory cycles.

1.4.1.4 Track Organization/Timing

Track organization/timing is as follows:

- Sector Format – 1 Word Preamble*
  96 Words Data
  1 Word Checkword
  1 Word Postamble*
- Bits/Word – 16
- Data Words/Sector – 96
- Sectors/Track – 32
- Tracks/Drum – See Table 1.1

*Preamble and postamble are generated by the drum memory unit.

- Data words/Track – 3072
- Track Timing – See Figure 1.2

1.4.1.5 Autoload Operation

Sectors $0 through $F (1536 words) are transferred to core locations $00 through $5F when the AUTO LOAD pushbutton is depressed. Autoload into protected core is allowed; the controller sends a true Program Protect signal to the computer during Autoload.

1.4.1.6 Partial Sector Write/Read

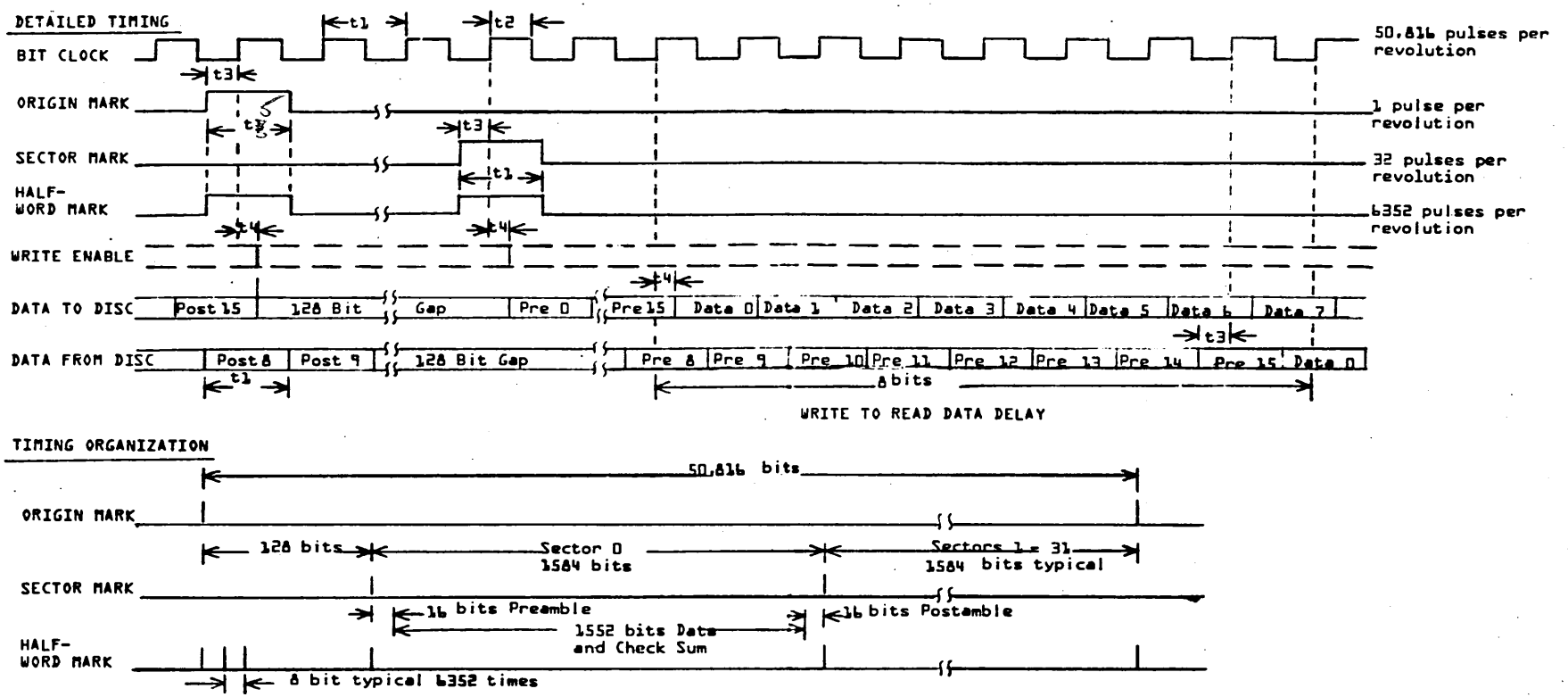
Data transfers of word length one or greater are allowed; all data transfers begin at a sector boundary. If fewer than 96 words are transferred into a sector, the controller fills the area between the last word and the checkword with zero. If fewer than 96 words are transferred to the CPU, the controller continues to the end of the sector to verify the checkword.

1.4.1.7 Guarded Address Detection

Front plane U-jumpers (39025100) inserted into card position A16 specify the highest Guarded Track Address. Drum Write operations into guarded addresses are not allowed while the ENABLE GUARDED ADDRESS switch is up; the controller aborts the attempted operation and sets appropriate alarm status bits.

1.4.1.8 Sector Overrange Detection

Front plane U-jumpers (39025100) inserted into card position A16 specify the highest Addressable Track Address. Drum Read or Write operations are not allowed beyond this address; the controller aborts the attempted operation and sets appropriate alarm status bits.



NOTES

1. All timing is shown at the memory system interface.

2. Timing tolerances include the effect of speed variations from 3300 RPM to 3600 RPM.

60Hz	50Hz
t1 = 342 ±20 nsec.	t1 = 410 ±20 nsec.
t2 = t1/2 ±20 nsec.	t2 = t1/2 ±20 nsec.
t3 = 75 nsec. min; t2 max.	t3 = 75 nsec. min; t2 max.
t4 = 200 nsec. max.	t4 = 200 nsec. max.

3. Following the ORIGIN MARK, and preceeding SECTOR 0 mark, 128-bit drum memory recovery period (allows continuous read/write operations).

4. 16 bits of sector preamble (PRE 0 to PRE 15) are generated by the drum memory and written following each SECTOR MARK (when WRITE ENABLE is TRUE).

5. 16 bits of postamble (Post 0 to Post 15) are generated by the drum memory system and written before each SECTOR MARK (WRITE ENABLE is TRUE).

6. Recovery time required by the memory system to read after switching tracks and writing is 25 usec and 30 usec respectively.

Figure 1.2. Drum Memory Timing

1.4.1.9 Power Failure Response

Upon loss of primary power, the power failure status bit sets one millisecond (minimum) before controller DC operating voltages fall 5%. If the controller is programmed for an Alarm Interrupt, this allows one millisecond (minimum) for software to respond to the interrupt and status the controller before it becomes inoperative.

Power failure can result in loss of drum data only when the failure occurs during a Drum Write operation; the affected data will be on only the track addressed at the time of failure.

1.4.1.10 Performance Limitations

Total DSA cable length shall not exceed 80 feet. Total A/Q cable length shall not exceed 200 feet.

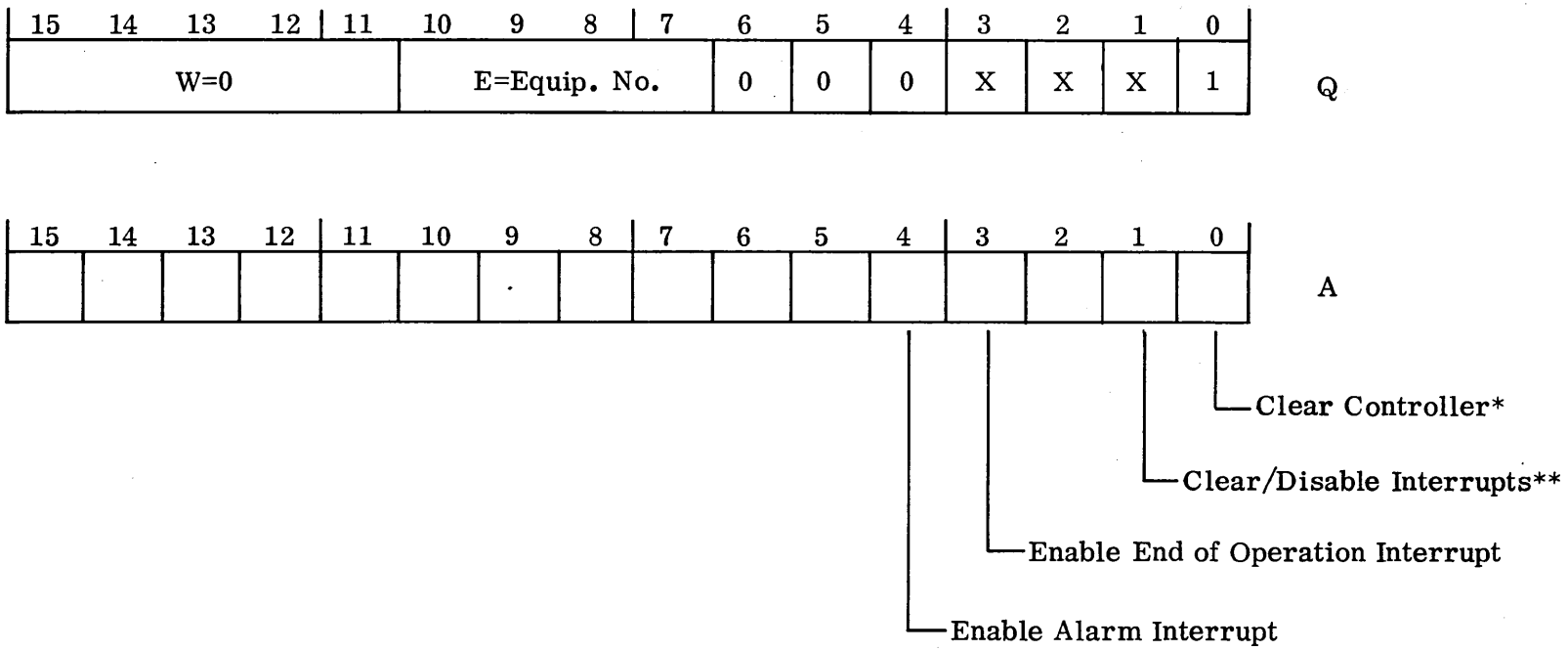
The error free data recovery window is 40°F: the temperature at which data is read from the drum must be within ±40°F of the temperature at which data is written on the drum.

1.4.1.11 Programming Codes

BG504 programming codes conform to manual 60165800 (see Table 1.4). The codes are illustrated in Figures 1.3 through 1.11.

1.4.1.12 Program Protect Operation

A/Q and DSA program protect (P.P.) operations are summarized in Tables 1.2 and 1.3 respectively.

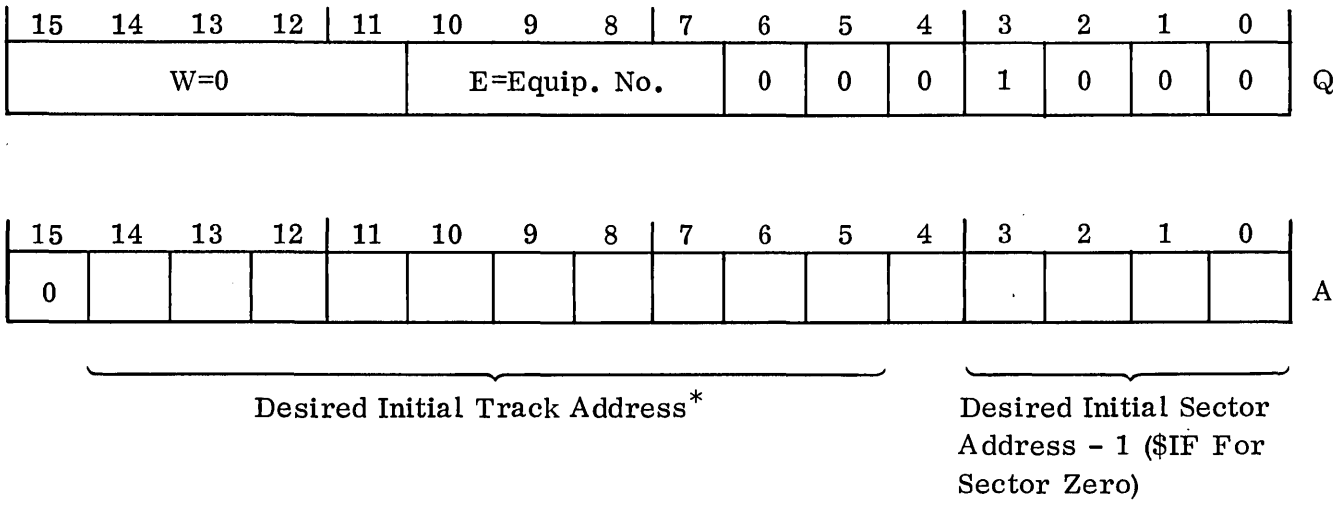


*Takes precedence over bits A3 and A4

**Subordinate to bits A3 and A4

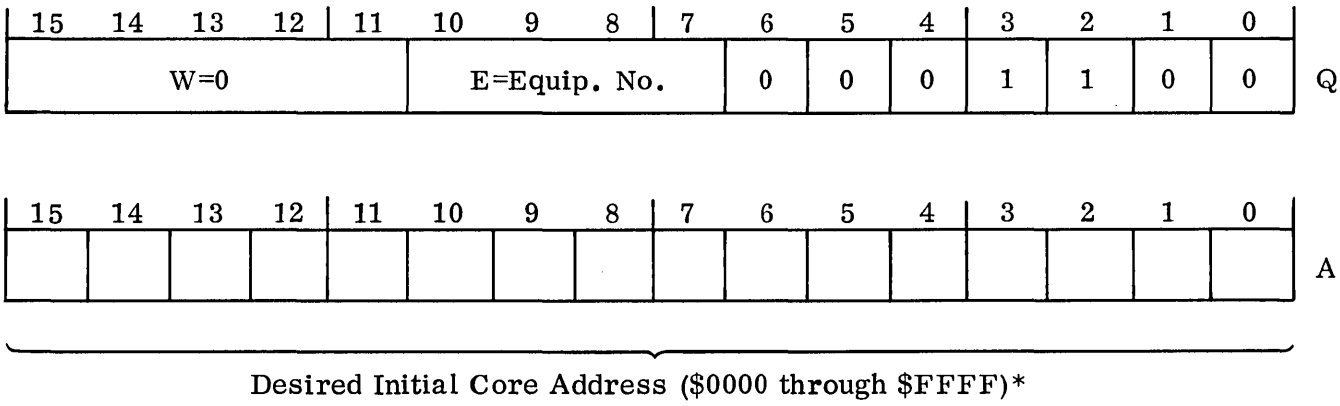
X Not applicable

Figure 1.3. Director Function (Out)



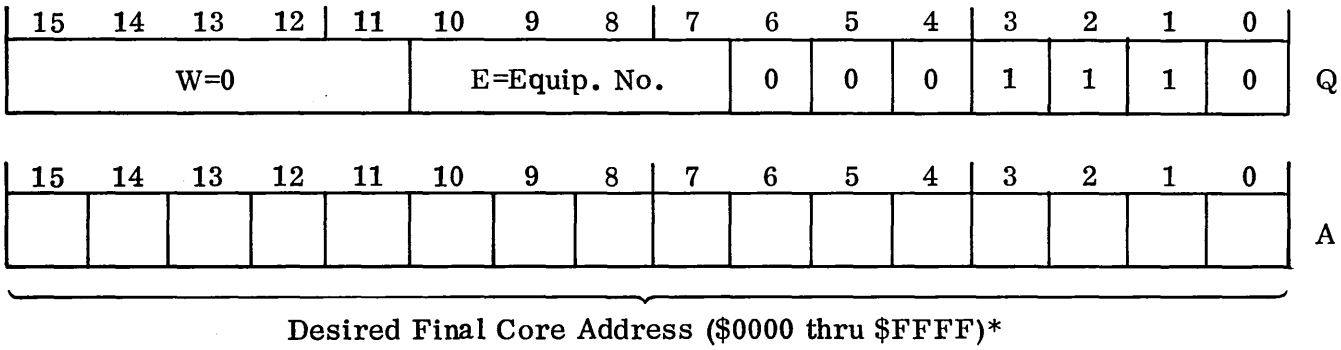
*Value incremented at each origin mark during Drum Read or Write operation

Figure 1.4. Load Initial Sector Address Register (Out)



*Value increments during each data transfer during Drum Read or Write operation

Figure 1.5. Load Initial Core Address Register (Out)



*Value unaltered during Drum Read or Write operation

Figure 1.6. Load Final Core Address Register (Out)

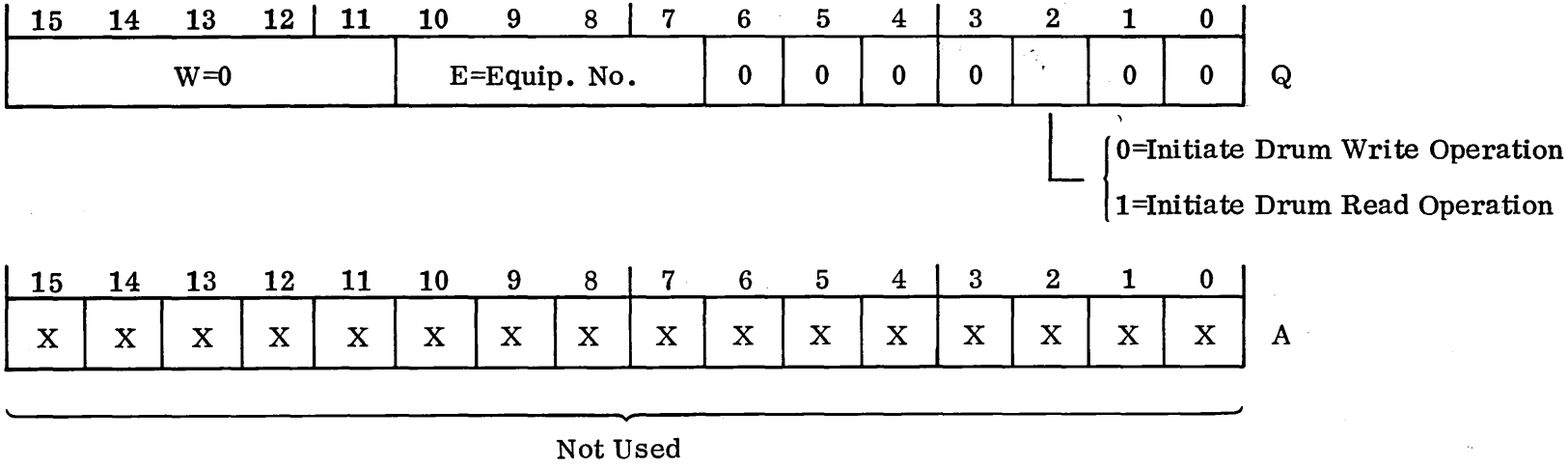
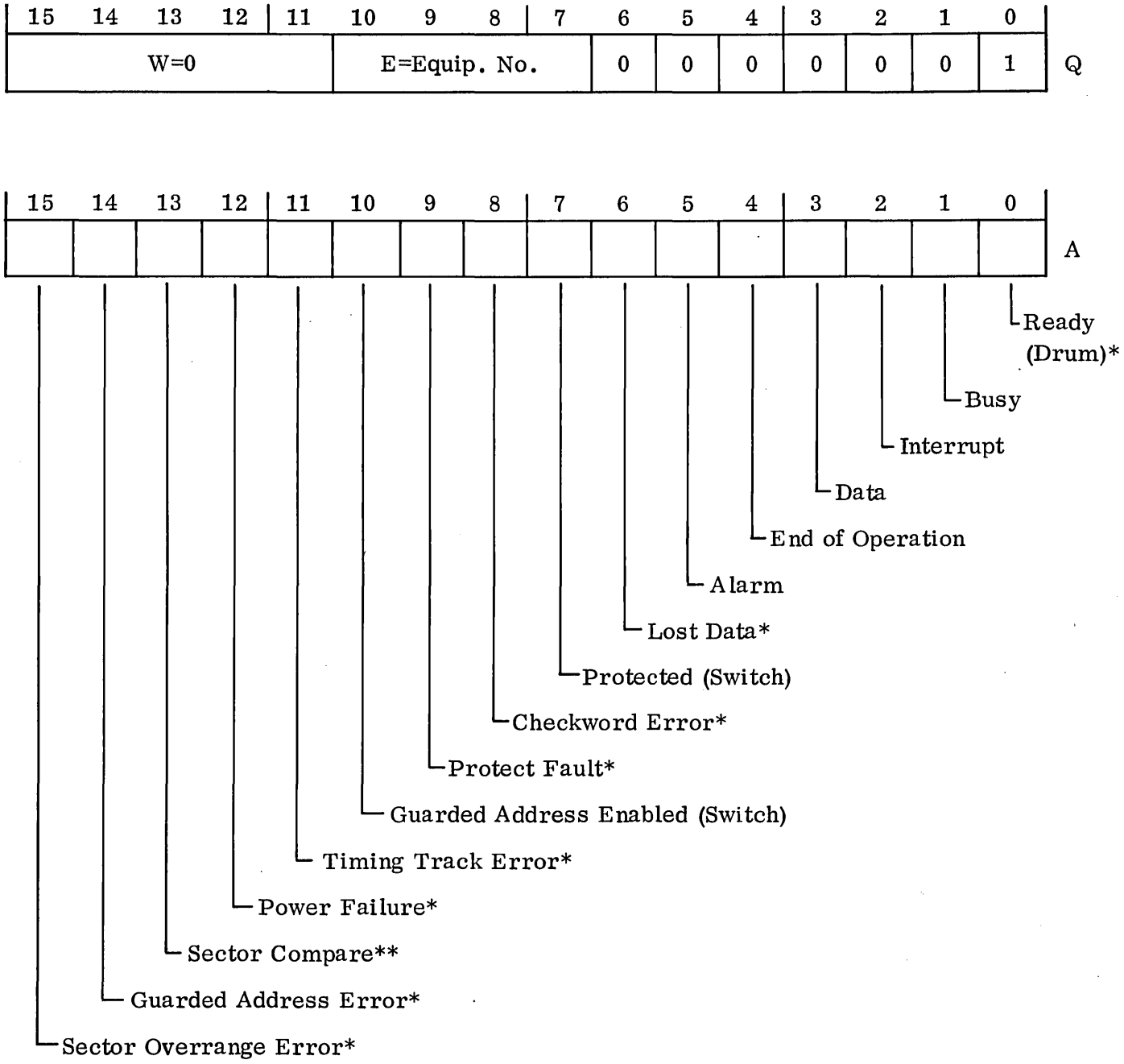
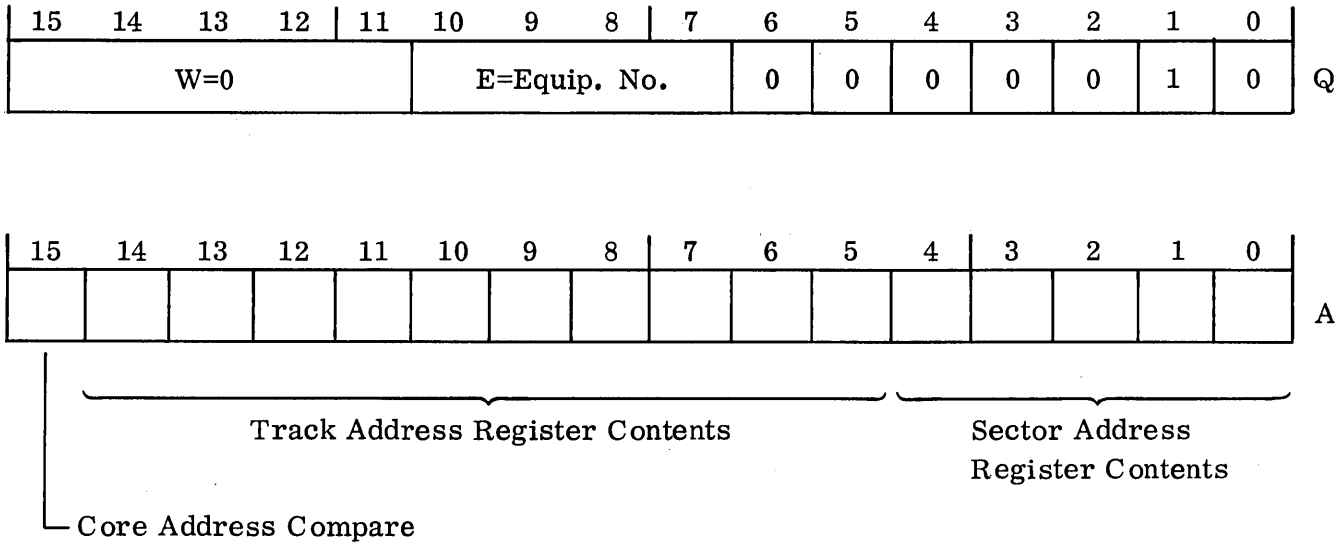


Figure 1.7. Initiate Drum Read/Write Operation (Out)



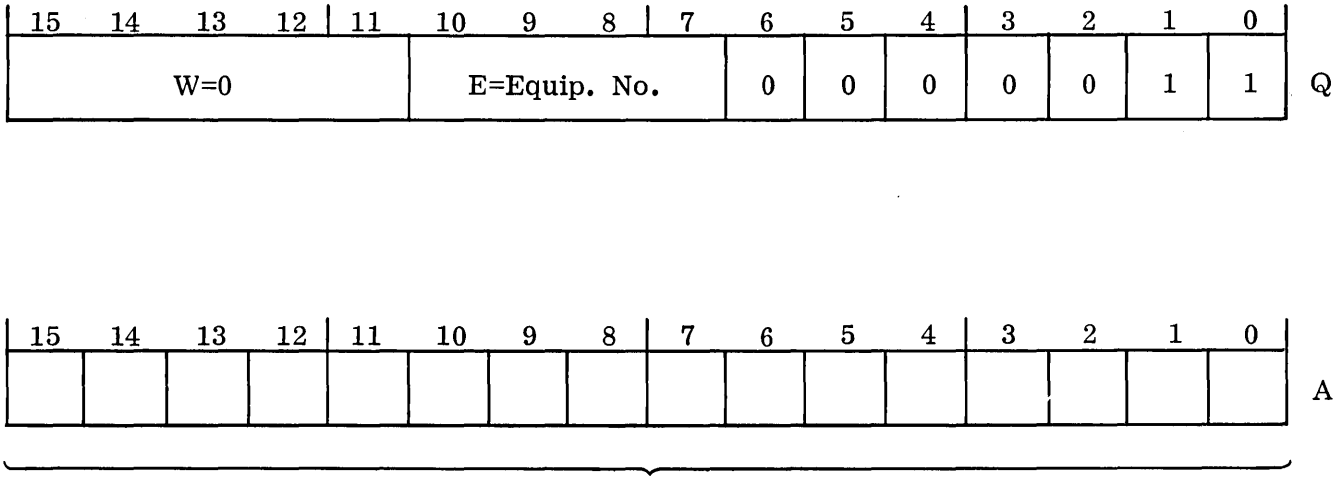
*Alarm Conditions
**For Diagnostic Purpose

Figure 1.8. Director Status (INP)



Bits A0 - A14 contain the current contents of the Sector Address Register. This allows the driver or diagnostic to check the current drum position, or at what sector an operation terminated. It is not cleared on reading status or by Clear Controller. Bit A15 is Core Address Compare (Core Address Register equals Final Core Address Register). This allows the diagnostic to check Initial and Final Core Address Register Load/Compare operation via A/Q (without DSA data transfers).

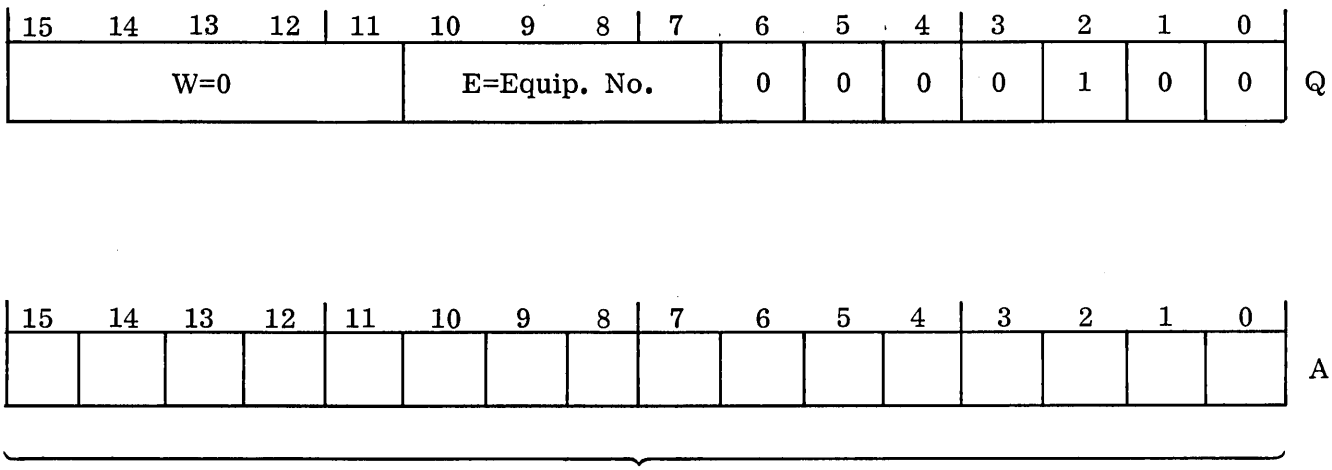
Figure 1.9. Sector Address Status (INP)



Core Address Register Contents

Bits A0 - A15 contain the current contents of the Core Address Register. The driver may use this status to check if a transfer completed properly. The diagnostic can determine where in-core transfers were made. It is not cleared on reading status or by Clear Controller (After EOP, should equal LWA + 1).

Figure 1.10. Core Address Status (INP)



Bits A0 - A15 contain the current contents of the controller register which shifts data to/from the drum memory unit. After Drum Read/Write operation Bits A0 - A15 contain the last word transferred to/from core. This status enables the diagnostic to determine whether bad data is occurring in the drum or the DSA interface. It is not cleared on reading status or by Clear Controller.

Figure 1.11. Data Status (INP)

1.4.1.13 Controls

Control functions are as follows:

- Scanner Switch - Routes transmission lines which form distributed DSA scanner. Refer to 60165800 (see Table 1.4) for a detailed description.
- EQUIPMENT NUMBER Switch - Selects controller equipment number $0 through $F.
- PROGRAM PROTECT Switch - In the up position, causes controller to reject all non-protected INP and OUT instructions.
- ENABLE GUARDED ADDRESS Switch - In up position, inhibits Drum Write operation into designated tracks.
- AUTO LOAD Switch - While depressed, causes controller to read first 1536 drum words into core (beginning at core location $0000). Operation repeats as long as switch is depressed.
- CONTROLLER/BLOWER Circuit Breaker - Overload protection and power switch (located on power distribution box).
- DRUM Circuit Breaker - Overload protection and power switch (located on power distribution box).
- Drum memory unit controls - Described in the drum memory unit manual (see Table 1.4).

1.4.1.14 Indicators

Indicator functions are as follows:

- READY - Drum memory unit is ready for data transfers.
- BUSY - Drum controller is performing Drum Read, Drum Write, or Clear Timing Error operation.

Table 1.2. A/Q Program Protect Summary

CONTROLLER P.P. SWITCH	INP/OUT P.P. BIT	CONTROLLER RESPONSE
1	1	RPLY
1	0	RJT (EXT)
0	1	RPLY
0	0	RPLY

Table 1.3. DSA Program Protect Summary

INITIATE DRUM READ/WRITE INSTR. P.P. BIT	DRUM READ/WRITE DATA BUFFER P.P. BIT	CONTROLLER P.P. FAULT	COMPUTER P.P. FAULT
1	1	No	No
1	0	No	No
0	1	Yes, Drum Read and Write	Yes, Drum Read Only
0	0	No	No

- ALARM - Drum controller has detected one (or more) of eight possible conditions which inhibit Drum Read and Write operations.
- Drum memory unit indicators - Described in the drum memory unit manual (see Table 1.4).

1.4.1.15 Jumpers

Jumper functions are as follows:

- Guarded Address Jumpers - Front plane U-jumpers in card position A16 which select the highest Guarded Track Address (0 through 255). The

address is assigned by an eight-position binary jumper configuration (see sheet 18 of Appendix A). Factory assigned highest Guarded Track Address is zero (no jumpers).

- Sector Overrange Jumpers - Front plane U-jumpers in card position A16 which select the highest addressable Track Address. The address is assigned (during factory checkout) by an eight-position binary jumper configuration (see sheet 18 of Appendix A).
- Eight spare U-jumpers (39025100) are inserted into card position A16 to allow the user to assign any desired Guarded Address.

1.4.1.16 UL Listing

The BG504 meets safety standards established by Underwriters' Laboratories (UL).

1.4.2 RELIABILITY

1.4.2.1 Mean Time Between Failures (MTBF)

The MTBF of the major components is as follows:

• BG504 Drum Memory Subsystem	2600 hours
• Drum Controller	7200 hours
• Drum Memory Unit	4000 hours

1.4.2.2 Fail Safe Features

- Power Failure Response - See Paragraph 1.4.1.9.
- Alarm Detection - See Figure 1.8.

1.4.2.3 Marginal Checking Characteristics. All BG504 dc operating voltages are adjustable allowing the diagnostic to be run at plus and minus five percent voltage margins.

1.4.3 MAINTAINABILITY

1.4.3.1 Design Features

- Four status words available to the diagnostic for identifying hardware failures and isolating their causes (see Figures 1.8 through 1.11).
- Functional printed circuit card layout of control functions to minimize the number of cards associated with any failure.
- Use of like cards for non-control functions to enable card swapping and to reduce spares: 9 card types out of 20 are used more than once.
- Adjustable dc voltages (see paragraph 1.4.2.3).

1.4.3.2 Accessibility

Description	Drum Controller	Drum Memory Unit
Circuits	Soldered IC's in pluggable cards. Card edge test points. Cards operate on extenders.	Pluggable IC's on single card (behind hinged front panel)
Operating Controls	Card edge panels	See Drum Memory Unit Manual (Ref. Table 1.4)
Status Indicators	Card edge panel	Front panel
Clock and WREN adjustments	Card edge potentiometer and test points	–
DC voltage adjustments	Power supplies (rear access)	Power supplies (rear access)
Comments	All DC voltages on card edge test points	Operates on slide extended 18 inches

1.4.3.3 Required Adjustments (See Section Six for procedures)

- Drum Controller - dc voltages (+6 vdc, +5 vdc, -6 vdc), Clock, and Write Enable (DSA).
- Drum Memory Unit - Helium gas flow (regulator).

1.4.3.4 Maintenance Philosophy

- Preventive Maintenance - Perform regularly
- Corrective Maintenance - Isolate failure through diagnostic and replace defective assembly (e.g. printed circuit card, power supply, blower, etc.).

1.4.3.5 Mean Time to Repair (MTTR)

• BG504 Drum Memory Subsystem	3.0 hours
• Drum Controller	1.0 hours
• Drum Memory Unit (Includes 4-hour cool down)	6.0 hours

1.4.3.6 Preventative Maintenance (PM)

- Monthly - Check helium pressure (5 minutes).
- Monthly - Check power supplies and filter (15 minutes).
- Quarterly - Run diagnostic (10 minutes).
- Annually - Run diagnostic with voltage margins (55 minutes).

1.4.3.7 Interchangeability

- Nine card types in drum controller.
- Head plates in drum memory unit.

1.4.3.8 Special Test Equipment Requirements or Options

- No special requirements.

1.4.3.9 Diagnostics Available

- See Appendix B.

1.4.4 HUMAN ENGINEERING AND SAFETY

No special requirements.

1.4.5 REFURNISHMENT

The helium bottle beneath the drum memory unit must be replaced at approximately six-month intervals.

1.4.6 MATERIALS, PROCESSES, AND PARTS

All connector contacts except J01, Terminator Power, are gold plated. All switch contacts are gold plated or sealed.

1.4.7 ELECTROMAGNETIC INTERFERENCE

Electromagnetic compatibility conforms to CDC-STD 1.30.022 (see Table 1.4) except for internal grounding: the BG504 incorporates a single point ground (SPG).

1.4.8 TRANSPORTABILITY/PACKAGING

Packaging for shipment shall conform to CDC Procedure 13-004 (see Table 1.4).

1.4.9 EQUIPMENT SPECIFICATION DATA SHEETS

Specification requirements for the BG504 are outlined in Figures 1.12 through 1.15.

1.5 EQUIPMENT CONFIGURATION

Each BG504 includes all major components described in paragraph 1.2. Component part number differences are listed in Table 1.1.

1.6 APPLICABLE DOCUMENTS

The documents listed in Table 1.4 are applicable to the extent specified herein.

Table 1.4. Applicable Documents

DESCRIPTION	PUBLICATION NO.
1700 Imput/Output Specification	60165800
DTL Intebrid Logic General Information	84785000
Drum Memory Unit Maintenance Manual Digital Development Corporation Models 5575 Kearny Villa Road 7311 San Diego, California, 92123 7312 (714) 278-9920 (7313)	None
Olympus 1700 Diagnostic Package Software User's Manual	39268100
1700 System Maintenance Monitor (SMM17) Reference Manual	60182000
1700 Computer Reference Manual	60153100
Electro-magnetic Compatibility Performance Requirements and Test Methods	CDC-STD 1.30.022
CDC Supplier Packaging Specification	CDC Procedure 13-004

GENERAL INFORMATION

Equipment Identification Number BG504 A through H

Equipment Name DRUM MEMORY SUBSYSTEM

Top Assembly Part Number 39744600

Is Equipment a stand alone (black box) unit? YES

PHYSICAL CHARACTERISTICS

Dimensions and Weight:

	Uncrated	Crated - Van (if known)	Crated - Air (if known)
Height	75 in.		
Width	24 in.		
Depth	28 in.		
Weight	730 lbs.		

Equipment Support:

Number of Casters 0
Number of Leveling Pads 4
Area of each Pad 4.9 in. sq.

Vibration Limits:

Operating And Non-operating

0 - 10 Hz 0.005 in. total excursion
10 - 25 Hz 0.002
25 - 50 Hz 0.001
Over 50 Hz 0.0005
MAXIMUM VIBRATION NTE 2 G's

LOGIC CHARACTERISTICS

Logic Cable From	Logic Cable To	Number of Cables	Terminating Connector Type	Maximum Cable Length	Distance from Cable con. to Floor
Rack	AQ	2	61 pin	200 ft.	48 in.
Rack	DSA	2	61 pin	80 ft.	48 in.
Rack	INT	1	3 pin MS	200 ft.	51 in.

Figure 1.12. BG504 Physical Characteristics

ELECTRICAL CHARACTERISTICS

Terminal Identifier	Volts	Freq.	Phase	#Wires Excl. Safety Ground	A/Ø (MAX)	KVA (MAX)	KW	EST.	MEAS. (NOM)
TB01	120	50/60	1	2	6.0	0.72			0.60
	40	DC Terminator Power is required?					Yes X	No	

Figures shown in above table are standard per DCD-STD 1.30.011. If some are not applicable, please cross out.

Motor Load (Name plate ratings of individual or combined motors, arranged to start together, that exceed 1 HP or 6 AMPS full load current ratings):

HP	V.	FREQ.	Ø	FLA	LRA	FUNCTION

Power Field Terminal Location:

400 Hz_____in. above base of cabinet
50 Hz_____in. above base of cabinet
50/60 Hz 1 in. above base of cabinet
Terminator Power 1 in. above base of cabinet
Number of Terminator Resistor Assemblies: NONE SUPPLIED, 0 - 4 REQUIRED

Describe unusual starting characteristics such as disks, drum and printers:

DRUM MEMORY REQUIRES 6 MIN. (NOM.) TO GET UP TO SPEED. IF CONTROLLER POWERED UP WITH DRUM, ALARM CONDITION PREVAILS. IF CONTROLLER POWERED UP 6 MIN. AFTER DRUM, NO ALARM CONDITION.

Figure 1.13. BG504 Electrical Characteristics

ENVIRONMENTAL CHARACTERISTICS

Temperature:

Operating 40 (min.) °F to 120 (max.) °F (Error free recovery window = 40°F)

Non-operating -30 (min.) °F to +150 (max.) °F

Max. Temp. Gradient 0.2 °F per hour

Recommended Operating Temperature 70 °F

Relative Humidity:

Operating 10 (min.) % to 90 (max.) % NO CONDENSATION

Non-operating 5 (min.) % to 95 (max.) % NO CONDENSATION

Altitude (above S.L.)

Max. Altitude 10,000 feet (OPER/NON-OPER)

Heat Dissipation (BTU/Hr):

Air 2050 Water _____ Total _____

Type of Equipment Cooling:

	Yes	No
Natural Convection	X	
Internal Fans	X	
Rating 540 CFM		
Direct Water Cooled		X
Refrigeration System:		X
Quantity and Size of Condensing Units:		
Qty. _____ TONS _____		
Condensing Unit Location:		
Internal		X
External		X
Air Cooled Condensing Unit		X
Water Cooled Condensing Unit		X

Water Supply Conditions:

	Min.	Recommended	Max.
Temperature (°F)			
Flow (gallons/min.)			
Pressure Drop (psi)			

Figure 1.14. BG504 Environmental Characteristics

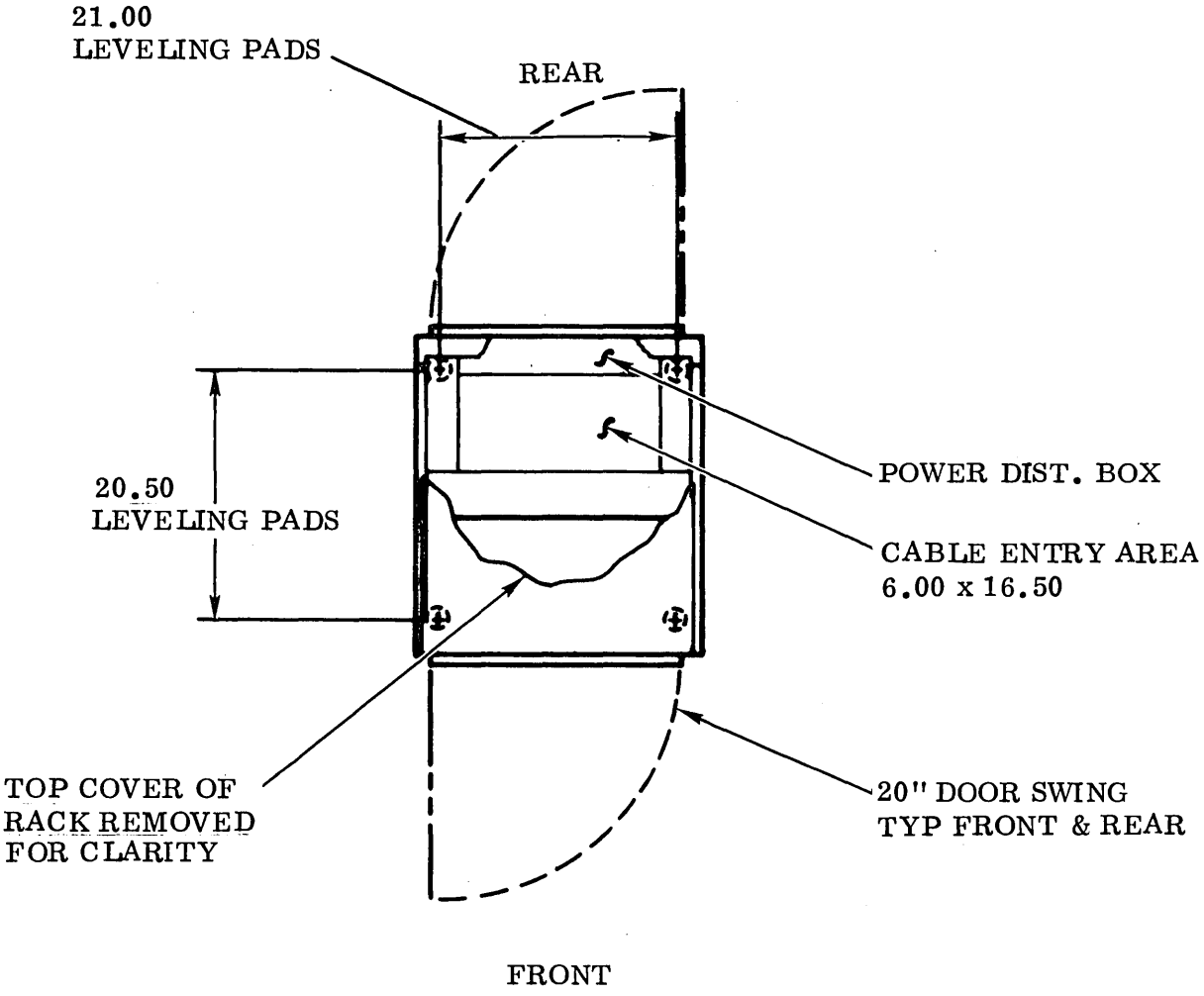


Figure 1.15. BG504 Plan View

Section Two

OPERATION AND PROGRAMMING

2.1 CONTROLS AND OPERATING PROCEDURE

All BG504 operator controls are described in paragraph 1.4.1.13.

2.2 JUMPERS AND OTHER EQUIPMENT CHANGES

2.2.1 GUARDED ADDRESS JUMPERS

Guarded Address jumpers are described in paragraph 1.4.1.15. For an example of jumper configurations refer to Table 2.1.

Table 2.1. Guarded Address Jumper Configuration Example

U JUMPER CONFIGURATION (A16 PINS)								GUARDED TRACKS
31 - 32	33 - 34	35 - 36	37 - 38	39 - 40	41 - 42	43 - 44	45 - 46	
1	1	1	1	1	1	1	1	0 - 255
1								0 - 128
	1							0 - 64
		1						0 - 32
			1					0 - 16
				1				0 - 8
					1			0 - 4
						1		0 - 2
							1	0 - 1
								0

2.2.2 SECTOR OVERRANGE JUMPERS

Sector Overrange jumpers are described in paragraph 1.4.1.15.

2.3 PROGRAMMING INFORMATION

2.3.1 GENERAL

2.3.1.1 Equipment Number

Each INP or OUT instruction to the BG504 must have bits Q7 through Q10 set to the equivalent binary code of the hexidecimal number displayed on the BG504 EQUIPMENT NUMBER switch. The standard BG504 equipment number is two.

2.3.1.2 A/Q OUT Commands

The BG504 responds to the following five A/Q OUT commands:

- Director Function (DF)
- Load Initial Sector Address Register (LISA)
- Load Initial Core Address Register (LICA)
- Load Final Core Address Register (LFCA)
- Initiate Drum Read/Write Operation (IRW)

Each command has a separate station address. (Bits Q0 through Q6.) All five commands must be executed to perform a Drum Read or Drum Write operation; command sequence requires only that IRW occur last.

The Clear Controller OUT command is accepted anytime; other OUT commands are accepted only if the controller is not busy and no alarms exist. The controller goes Busy only after an Initiate Drum Read or Initiate Drum Write OUT command.

2.3.1.3 A/Q INP Commands

The BG504 responds to the following four A/Q INP commands:

- Director Status (DIS)
- Sector Address Status (SAS)
- Core Address Status (CAS)
- Data Status (DAS)

Each INP command has a separate station address. Status other than DIS is provided primarily for the diagnostic. INP commands are accepted at all times by the controller (see paragraph 2.3.12.2).

2.3.2 DIRECTOR FUNCTION OUT COMMAND

The A/Q bit configuration is shown in Figure 1.3. Director function bit definitions are as follows:

- A0 Clear Controller - Initializes all controller logic, clears all interrupts and interrupt enables. Clears Alarm conditions and Timing Error Cleared Interrupt (see paragraph 2.3.11.3).
- A1 Clear/Disable Interrupts - Resets Enable Interrupt flip-flops (FF's) if bits A3 and A4 zero. EOP and Alarm Interrupts cannot occur if respective Enable Interrupt flip-flop (FF) is reset.

- A3 Enable EOP Interrupt - Sets Enable End of Operation Interrupt FF which results in interrupt after Drum Read or Drum Write operation.
- A4 Enable Alarm Interrupt - Sets Enable Alarm Interrupt FF which results in interrupt on any Alarm condition.

2.3.3 LOAD INITIAL SECTOR ADDRESS REGISTER OUT COMMAND

The A/Q bit configuration is shown in Figure 1.4.

A 15-bit address is placed in the A Register for this OUT command: bits A0 through A4 are the desired Initial Sector Address (ISA), and bits A5 through A14 are the desired Initial Track Address (ITA). The controller must be loaded with the desired ISA minus one. If data transfers begin at sector zero of any track, load A0 through A4 with $1F. For other desired ISA's load A0 through A4 with the desired ISA minus one ($00 through $1E).

This command is required for every Drum Read or Write operation because the ITA is incremented (at each origin mark) during data transfers.

2.3.4 LOAD INITIAL CORE ADDRESS REGISTER OUT COMMAND

The A/Q bit configuration is shown in Figure 1.5. This command must be loaded into the controller before every Drum Read or Write operation because the 16-bit Initial Core Address is incremented during data transfers to core.

2.3.5 LOAD FINAL CORE ADDRESS REGISTER OUT COMMAND

The A/Q bit configuration is shown in Figure 1.6.

This 16-bit address is unaltered during Drum Read or Write operations.

2.3.6 INITIATE DRUM READ/WRITE OUT COMMANDS

The A/Q bit configuration is shown in Figure 1.7.

The controller goes Busy immediately after either of these OUT commands. For a Drum Write operation, data transfers from core begin immediately and data transfers to the drum occur only after the desired initial sector rotates into position under the fixed - read/write headplates.

For a Drum Read operation, data transfers from the drum to core only after the desired initial sector is positioned under the headplates.

Once drum data transfers begin the controller remains Busy until the end of the last sector at which data transfers occur.

2.3.7 DIRECTOR STATUS INP COMMAND

The A/Q bit configuration is shown in Figure 1.8.

Director status bit definitions are as follows:

- A0 Ready - Drum up to speed and ac power up. Drum temperature and pressure OK. Alarm sets if Ready drops.
- A1 Busy - Controller performing Drum Read/Write or Clear Timing Error. Output commands rejected (except Clear Controller).
- A2 Interrupt - Alarm, EOP, or Timing Error Cleared interrupt present. Alarm and Timing Error Cleared interrupts cleared by Master Clear or Clear Controller. EOP interrupt cleared by any non-rejected output (Interrupt Enable cleared only by Master Clear, Clear Controller, or Clear Interrupt).
- A3 Data - Ready for data transfer (Alarm Busy).

- A4 End of Operation (EOP) - Data transfer is completed. EOP interrupt is set. Reset by non-rejected output.
- A5 Alarm - Alarm condition is present:
  - Drum going Not Ready
  - Lost data
  - Checkword error
  - Protect fault
  - Timing track error
  - Power failure
  - Guarded Address error
  - Sector Overrange error

Reset by Clear Controller function or Master Clear.

- A6 Lost Data
  - Read from Drum operation - Data not transferred to core before new data taken from drum. Data transfer is terminated; Alarm sets.
  - Write on Drum operation - Data not retrieved from core in time to be written on drum. Data transfer is terminated; Alarm sets.
- A7 Protected - PROGRAM PROTECT switch in PROTECT position. All unprotected INP and OUT commands are rejected.
- A8 Checkword Error - Checkword error during Drum Read, data transfer terminated; Alarm sets.
- A9 Protect Fault - An unprotected instruction has attempted to access protected core location (Drum Read or Write). Terminates data transfers; Alarm sets. See Table 1.3.

- A10 Guarded Address Enabled - Switch is in position to inhibit writing into Guarded Track Addresses.
- A11 Timing Track Error - Loss of drum timing pulse(s) (Origin, Bit Clock, Sector Mark, Word Mark). Terminates data transfers; Alarm sets.
- A12 Power Failure - Disables Write Enable to the drum memory unit and data transfers. Alarm sets 1 millisecond before controller voltages sag (triggered by loss of approximately two ac power cycles).
- A13 Sector Compare Bit - True when Sector Address Counter = Initial Sector Address Register (for diagnostic use).
- A14 Guarded Address Error - Write on drum attempted at Guarded Address. Transfers terminated; Alarm sets.
- A15 Sector Overrange Error - Drum Read or Write attempted on non-existent drum track. Data transfers terminate and Alarm sets.

2.3.8 SECTOR ADDRESS STATUS INP COMMAND

The A/Q bit configuration is shown in Figure 1.9.

2.3.9 CORE ADDRESS STATUS INP COMMAND

The A/Q bit configuration is shown in Figure 1.10.

2.3.10 DATA STATUS INP COMMAND

The A/Q bit configuration is shown in Figure 1.11.

2.3.11 INTERRUPTS

There is one interrupt line between the BG504 and the CPU. The number assigned to this line is determined by which of the 15 connectors at the CPU

the line is plugged into. The standard BG504 interrupt line number is five. Three sources of interrupt share this line.

2.3.11.1 End of Operation Interrupt

The End of Operation (EOP) interrupt occurs at the end of every Drum Read or Drum Write operation when Program Enabled. The EOP interrupt is cleared by any non-rejected OUT instruction or by a Master Clear.

2.3.11.2 Alarm Interrupt

The eight conditions which cause an alarm are described in paragraph 2.3.7. The Alarm interrupt occurs when Program Enabled.

The Alarm interrupt is cleared by a Clear interrupt or Clear Controller function (paragraph 2.3.2) or by a Master Clear.

2.3.11.3 Timing Error Cleared Interrupt

A non-programmable interrupt occurs after a timing error is cleared. This interrupt is required by the driver.

The TEC interrupt is cleared by either a Clear Controller function or a Master Clear.

2.3.12 REJECTS

2.3.12.1 Internal Rejects

Internal rejects occur if the BG504 controller is OFF or if bits Q7 through Q10 of the INP/OUT instruction do not match the setting of the EQUIPMENT NUMBER switch.

2.3.12.2 External Rejects

All unprotected INP and OUT instructions are rejected if the BG504 PROGRAM PROTECT switch is up (see Table 1.2). All OUT instructions except for Clear Controller are rejected if the BG504 is either Busy or in an Alarm condition.

2.3.13 MASTER CLEAR

Master Clear and Clear Controller result in the same BG504 activity: all controller logic is initialized and all interrupts and interrupt enables are cleared.

2.4 SAMPLE PROGRAM

The following 1700 machine code program repeats Drum Write (or Read) operations of $C00 words beginning at core location $7000 to (from) sector zero of the BG504. See Table 2.2.

Table 2.2. Sample 1700 Machine Code Program

CORE LOCATION		CORE CONTENTS	COMMENTS
P		E000	
P+	1	0101	(Equipment No. = 2)
	2	0A01	
	3	0B00	
	4	03FE	Clear Controller
	5	E000	
	6	010C	
	7	C000	
	8	7000	
	9	0B00	

Table 2.2. Sample 1700 Machine Code Program (Continued)

CORE LOCATION	CORE CONTENTS	COMMENTS
A	03FE	Load ICA = $7000
B	E000	
C	010E	
D	C000	
E	7C00	
F	0B00	
10	03FE	Load FCA = $7C00
1	E000	
2	0108	
3	C000	
4	001F	
5	0B00	
6	03FE	Load ISA = IF
7	E000	
8	0100	(0104 for Drum Read)
9	0B00	
A	03FE	Initiate Drum Write (Read) Operation
P+ 1B	18E9	Jump Back and Repeat

Section Three

INSTALLATION AND CHECKOUT

3.1 INSTALLATION REQUIREMENTS

The BG504 is a stand-alone unit occupying one standard 19-inch rack. Refer to paragraphs 1.2 and 1.4.9 for a detailed physical description. The installation procedure is:

- Unpack
- Inspect for damage and loose connections (paragraph 3.7).
- Wire 120 vac, 40 vdc, and system ground to the power distribution box (paragraph 3.2).
- Connect system cables and inspect internal BG504 cables (paragraph 3.3).
- Energize (paragraph 3.7).

3.2 POWER REQUIREMENTS

The BG504 requires external 120 vac and 40 vdc power as specified in paragraph 1.3. Wire termination is solderless: strip and insert into screw-down terminal. A number ten screw is provided for system ground termination. Refer to Figure 5.1 for wiring details.

3.3 CABLING AND CONNECTORS

Cable requirements are specified in Table 3.1.

Table 3.1. BG504 Cable Requirements

PART NUMBER	DESCRIPTION	FROM	TO
38927902	Terminator Power	J01 Controller	TB01 Power Distribution Box
388088XX	Interrupt (Optional)	J02	CPU
39738102	Drum	J03	J10 Drum
310004XX	A/Q Address In	J04	Other A/Q Device or CPU
↓	A/Q Address Out	J05	Other A/Q Device (or Terminate).
	A/Q Data In	J06	Other A/Q Device or CPU
	A/Q Data Out	J07	Other A/Q Device (or Terminate).
	DSA Address In	J08	Other DSA Device or CPU
	DSA Address Out	J09	Other DSA Device (or Terminate).
	DSA Data In	J10	Other DSA Device or CPU
310004XX	DSA Data Out	J11	Other DSA Device (or Terminate).
	120 VAC (Blower)	J12 Controller	Blower
	DC Power	J2 Drum	Drum Power Supply Panel
	AC Power	J4 Drum	J02 Power Distribution Box
	AC Power	Drum Power Supply Panel	J01 Power Distribution Box

3.4 INTERFACE CHARACTERISTICS

The BG504/CPU interface conforms to Specifications 60165800 (see Table 1.4).

DSA loading is specified in paragraph 1.4.1.3.

Interface transmitter and receiver circuits are described in paragraph 1.3.4.

3.5 COOLING REQUIREMENTS

BG504 cooling is provided by internal fans. See paragraph 1.2.5.

3.6 ENVIRONMENTAL LIMITATIONS

See paragraph 1.4.9.

3.7 PREPARATION FOR USE

3.7.1 PRELIMINARY INSPECTION

Before power is brought into the power distribution box, examine the BG504 for damage and for loose mechanical and electrical connections:

- Does the drum unit helium atmosphere pressure gauge indicate some positive pressure? Refer to drum unit manual (see Table 1.4) for further details.
- Are the drum unit slides secured to the rack and is the drum unit set properly on the slides?
- Any loose screws or wiring on power supplies?
- Any loose connectors?

3.7.2 START UP PROCEDURE

Turn on circuit breakers:

- Motor POWER ON indicator should illuminate - disregard other indicators.
- Blowers must force air up through the controller module.
- After six minutes the READY indicator should illuminate.

Master Clear CPU:

- READY should be the only illuminated indicator on the controller module. Refer to drum unit manual (see Table 1.4) for status of other indicators.

Run diagnostic SMM17 V3.0 Test 80 (see Appendix B).

Section Four

THEORY OF OPERATION

4.1 GENERAL

This section describes only BG504 controller operation. Refer to the drum memory unit manual (see Table 1.4) for BG504 drum memory unit operation.

Controller logic is implemented with CDC DTL, and commercial TTL circuits. Logic symbols are defined in Section Seven.

The controller logic package is Appendix A. See Table 4.1 for a definition of terms. Positive logic is used throughout; terms ending in F are false-oriented. Terms preceded by $ are twisted-wire pairs.

Table 4.1. Glossary of Terms

TERM	DESCRIPTION
AINTF	Alarm Interrupt False
ALARM	Alarm (FF)
ALSF	Autoload Switch False
ARJT	Reject (to AQ)
ARMF	Alarm False
ARPLY	Reply (to AQ)
AQPP	Program Protect (from A/Q)
AQPPF	Program Protect False (from A/Q)
A0-A15	A Register Bits 0-15
A0F-A4F	A Register Bits 0-4 False
BADF	Bad False (GAE or SOR Alarm input)
BCC	Bit Clock Counter

Table 4.1. Glossary of Terms (Continued)

TERM	DESCRIPTION
BC6	Bit Count 6
BC6F	Bit Count 6 False
BC7F	Bit Count 7 False
BZ	Busy (FF)
BZF	Busy False (FF)
CAC	Core Address Compare
CACAF	Core Address Compare A False (bits 0-7)
CACD	Core Address Compare Delayed (FF)
CARC	Core Address Register Carry (bits 0-7 to bits 8-15)
CARMF	Clear Alarm Interrupt False
CAS	Core Address Status
CA0-CA15	Core Address Register Bits 0-15
CA0F-CA15F	Core Address Register Bits 0-15 False
CEOPF	Clear EOP F.F. False
CIOPF	Clear I/O Instruction Protected F.F. False
CLEF	Clear False (director function)
CLKF+	Clock False
CLK2	Clock 2 (inverted CLKF+)
CLR	Clear (director function or MCL)
CLRF	Clear False (director function or MCL)
CNCT	Connect
CNCTF	Connect False
COPIF	Clear EOP Interrupt False
CRUNF	Clear Run False
CS1F	Core Status 1 False (enables bits 0-7)
CS2F	Core Status 2 False (enables bits 8-15)

Table 4.1. Glossary of Terms (Continued)

TERM	DESCRIPTION
CTE	Clear Timing Error
CTEF	Clear Timing Error False
CW	Checkword
CWAZF	Checkword A Zero False (bits 0-7)
CWBZ	Checkword B Zero False (bits 8-15)
CWE	Checkword Error (FF)
CWEF	Checkword Error False
CWZ	Checkword is Zero
CW0F-CW15F	Checkword Register Bits 0-15 False
CW15	Checkword Register Bit 15
DAS	Data Status
DAS1F	Data Status 1 False (enables bits 0-7)
DAS2F	Data Status 2 False (enables bits 8-15)
DATA	Data (FF)
DATAF	Data False
DB0-DB15	Data Bits 0-15 (DSA)
DF	Director Function
DFE	Director Function Enable (interrupt enable/clear)
DIS	Director Status
DMC	Drum Memory Cycle Latch
DR	Drum Ready (inverted DRF+)
DRF+	Drum Ready False (from drum unit)
DSAPB	Program Protect Bit (from DSA)
DSAPP	Program Protect (to DSA)
DS1F	Director Status 1 False (enables bits 0-7)
DS2F	Director Status 2 False (enables bits 8-15)

Table 4.1. Glossary of Terms (Continued)

TERM	DESCRIPTION
DW	Drum Write (FF)
DWC0F	Drum Write Control 0 False (FF)
DWC1F	Drum Write Control 1 False (FF)
DWF	Drum Write False (FF)
DW1F	(Partially) Decoded Halfword Count 1 False
EARMF	Enable Alarm Interrupt False
EEOPF	Enable EOP Interrupt False
EGAE	Enable Guarded Address
EGAS	Enable Guarded Address Switch
EINTF	EOP Interrupt False
ELAR	Enable Load Address Register
EOP	End of Operation (FF)
ERS	Enable Read Shift (checkword/data in)
ERSF	Enable Read Shift False (checkword/data in)
ERW	Enable Read/Write
EWS0F	Enable Write Shift 0 False (data out)
EWS1	Enable Write Shift 1 (checkword out)
EWS2F	Enable Write Shift 2 False (checkword in)
FCA	Final Core Address
FC0-FC15	Final Core Address Register Bits 0-15
FC0F-FC15F	Final Core Address Register Bits 0-15 False
GAE	Guarded Address Error (FF)
GAJ0-GAJ7	Guarded Address Jumpers 0-7
GAP	Gap FF (track switching time)
GAPF	Gap False (FF)
GATEF	Gate False (1F → ISA for autoload)

Table 4.1. Glossary of Terms (Continued)

TERM	DESCRIPTION
GA0-GA4	Gated A Register Bits 0-4 (ISA inputs)
GCLKF	Gated Clock False
GCLK1	Gated Clock 1
HALT	Halt (Scanner) False (FF)
HWM+	Half Word Mark (from drum unit)
ICA	Initial Core Address
INT	Interrupt
IOP	I/O Instruction Protected (FF)
IOPF	I/O Instruction Protected False (FF)
IRW	Initiate Read or Write
ISA	Initial Sector Address
ITAF	Increment Track Address Register False
LD	Lost Data (FF)
LDF	Lost Data False (FF)
LDRF	Lost Data (On Drum) Read False
LDWF	Lost Data (On Drum) Write False
LFCAF	Load Final Core Address Register False
LICAF	Load Initial Core Address Register False
LR0RF	Load Register 0 on Drum Read False
LR0WF	Load Register 0 on Drum Write False
LR1RF	Load Register 1 on Drum Read False
LR2RF	Load Register 2 on Drum Read False
LR2WF	Load Register 2 on Drum Write False
LSAF	Load (Initial) Sector Address Register False
LTAF	Load Track Address Register False
MCLF	Master Clear False

Table 4.1. Glossary of Terms (Continued)

TERM	DESCRIPTION
ME2	Me Too (FF)
NAP	Enable EOP Interrupt (FF)
NAPF	Enable EOP Interrupt False (FF)
NARM	Enable Alarm Interrupt (FF)
NARMF	Enable Alarm Interrupt False (FF)
(N0)	Need Zero
(N1)	Need 1
OM+	Origin Mark
ONE	One
ORA6-ORA9	Sector Overrange Address Jumpers 6-9
ORD	Our Reply Delayed
ORF	Our Reply False
PCL	Power Clear (5 sec)
PF	Power Failure (FF)
PFF	Power Failure False (FF)
PRIOR	(DSA) Priority
PROF	(DSA) Protect Fault (FF)
PROFF	(DSA) Protect Fault False (FF)
PROK	(A/Q) Protect OK
PROTS	Protect Switch
QIS04	Q Register Is 0 or 4
QIS0-QISE	Q Register Is 0-E
Q0-Q3	Q Register Bits 0-3
RCS3F	Read Control Step 3 False
RC0F	Read Control 0 False (FF)

Table 4.1. Glossary of Terms (Continued)

TERM	DESCRIPTION
RDATA	Reset Data
RDC	Read Data Compare (CWG input)
RDCF	Read Data Compare False (CWG input)
RDF	Read Data False
READ	Read (from A/Q)
RFDF	Read From Drum False
RJTWF	Reject on Drum Write False
ROSRF	Run Or Set Run False
ROW	Read Or Write (from A/Q)
RP	Read Pulse
RPLY	Reply (from DSA)
RPLYF	Reply False (from DSA)
RQST	Request (FF, to DSA)
RQSTF	Request False (to DSA)
RRUN	Reset Run
RUN	Run (FF)
RUNF	Run False (FF)
RWP	Read or Write Pulse (from A/Q)
R00-R015	Register 0 Bits 0-15
R00F-R015F	Register 0 Bits 0-15 False
R20-R215	Register 2 Bits 0-15
SAC	Sector Address Compare
SAS	Sector Address Status
SBZ	Set Busy
SC	Sector Counter
SCN1	Scanner Forward

Table 4.1. Glossary of Terms (Continued)

TERM	DESCRIPTION
SC0-SC4	Sector Count Register Bits 0-4
SC31F	Sector Count 31 False
SET1F-SET3F	Set Reject 1-3 False
SIOPF	Set I/O Instruction Protected False
SLD	Set Lost Data
SM+	Sector Mark
SOR	Sector Overrange (FF)
S.O.T.	Select On Test
SPROF	Set Protect Fault False
SRJT	Set Reject
SRJTF	Set Reject False
SRUN	Set Run (FF)
SRW	Start Read/Write
SSRUN	Set Set Run
SS1F	Sector Status 1 False (enables bits 0-7)
SS2F	Sector Status 2 False (enable bits 8-15)
STS	Status
STDF	Settling Time Delay False
STEC	Set Timing Error Cleared
STECF	Set Timing Error Cleared False
SUPF	Set Up False (autoload)
TA	Track Address (Register)
TAC	Track Address Carry
TA0-TA9	Track Address Register Bits 0-9
TA0F-TA9F	Track Address Register Bits 0-9 False
TE	Timing Error (FF)

Table 4.1. Glossary of Terms (Continued)

TERM	DESCRIPTION
TEC	Timing Error Cleared
TECF	Timing Error Cleared False
TEF	Timing Error False
TLK	Trailing Clock
TLKF	Trailing Clock False
VCTT	Center Tap for Terminators
WBF	Write Busy False
WB15	Write Bit 15
WCS5F	Write Control Step 5 False
WCW	Write Checkword
WCWF	Write Checkword False
WC0F	Write Control 0 False (FF)
WDC	Write Data Compare (CWG input)
WDCF	Write Data Compare False (CWG input)
WENF1	Write Enable False 1
WENF2	Write Enable False 2
WFSMF	Wait For Sector Mark False (FF)
WN0F	Write Need 0 False
WN1F	Write Need 1 False
WODF	Write On Drum False (director function)
WP	(A/Q) Write Pulse
WREN	Write Enable
WRF	Write Reply False
WRITE	Write (from A/Q)
WRJT	Write Reject
W2F	Halfword Count 2 False

Table 4.1. Glossary of Terms (Continued)

TERM	DESCRIPTION
W15F	Halfword Count 15 False
W193F	Halfword Count 193 False
W196F	Halfword Count 196 False
W197F	Halfword Count 197 False
$AB0-$AB15	Address Bits 0-15 (to DSA)
$APLY	Reply (to A/Q)
$APRI	(A/Q) Priority (not used in controller)
$AQPP	Program Protect (from A/Q)
$ARJT	Reject (to A/Q)
$AR0-$AR15	A Register Bits 0-15 (to/from A/Q)
$BC	Bit Clock (from drum unit)
$BUFF	Buffer Active (not used in controller)
$CHIN	Character Input (not used in controller)
$CLKF	Clock False
$DB0-$DB15	Data Bits 0-15 (to/from DSA)
$DMCL	(DSA) Master Clear (not used in controller)
$DRF	Drum Ready False (from drum unit)
$DSAP	Program Protect (to DSA)
$HWM	Halfword Mark (from drum unit)
$IMAF	Increment Memory Address False
$INT	Interrupt
$LINE	Line Voltage (stepped down for PF detect)
$MCL	Master Clear (from A/Q)
$NT1-$NT15	Interrupt Lines to DSA (not used in controller; however, note that $NT14 is wired to output of DSA Address bit 15 transmitter)
$OM	Origin Mark (from drum unit)

Table 4.1. Glossary of Terms (Continued)

TERM	DESCRIPTION
$PIOR	Priority (to DSA)
$PPF	(DSA) Program Protect Fault (not used in controller)
$PROT	Program Protect Bit (from DSA)
$QR0-$QR15	Q Register Bits 0-15 (from A/Q)
$RD	Read Data (from drum unit)
$READ	Read (from A/Q)
$RITE	Write (from A/Q)
$RPLY	Reply (from DSA)
$RQST	Request (to DSA)
$SCN1	(DSA) Scanner Forward Input
$SCN2	(DSA) Scanner Return Output
$SCN3	(DSA) Scanner Return Input
$SCN4	(DSA) Scanner Forward Output
$SM	Sector Mark (from drum unit)
$SP	(DSA) Storage Storage Parity Bit (not used in controller)
$SPE	(DSA) Storage Parity Error (not used in controller)
$TA0-$TA9	Track Address Bits 0-9 (to drum unit)
$TIME	(A/Q) Timing Pulse (not used in controller)
$TLKF	Trailing Clock False
$V20+, $V20-	Terminator Power
$WD	Write Data (to drum unit)
$WDIS	Write Disable (to drum unit)
$WEF	Write Enable False (to drum unit)
$WISZ	W Is Zero (from A/Q)
$WREN	Write Enable (to DSA)
$WS0F	Write Sync 0 False
*	Symbol for card edge test point

4.2 PRINCIPLE OF OPERATION

The controller logic is divided into the following three functional groups:

- A/Q interface - 17 cards (approximately).
- DSA interface - 16 cards (approximately).
- Drum interface - 11 cards (approximately).

Some cards are shared by two functional groups so that the total card count is only 39.

Sheets three and four of Appendix A are the functional block diagram. Note that the A module (top) is strictly TTL logic, and the B module is CDC DTL logic.

The A module contains the majority of the controller logic including the interface circuits (see paragraph 1.3.3) which connect to the drum memory unit.

The B module contains balanced-current mode transmitters and receivers (see 1.3.4) which connect to the 1700 A/Q and DSA channels.

Refer to the A module functional block on sheet 3 of Appendix A. As stated in paragraph 2.3.1.2, a Drum Read or Drum Write operation occurs only after a sequence of the following five OUT commands:

- Director Function (DF) - Enable/Disable interrupts. The DF output exercises the general purpose TTL logic in the lower left corner of sheet 3 of Appendix A. Clock card A26 in the center of the sheet decodes the Q-bits, provides basic A/Q function timing, and supplies the TTL logic with a two-phase clock synchronized to the rotating drum surface.
- Load Initial Sector Address Register (ISA) - Bits A0-A4 are loaded into the ISA register (card A14) via fan-in logic (card A30) in lower right corner of sheet three; track timing logic is also on card A14. Bits A5 and A6 drop

into track address register bits 0 and 1 (card A15); card A15 also has ten track address line drivers and timing error logic. Bits A 7 - A14 load into TA register bits 2-9 (card A17).

- Load Initial Core Address Register (ICA) - Bits A0 - A15 load into the core address register (cards A19 and A22), top left corner of sheet.
- Load Final Core Address Register (FCA) - Bits A0 - A15 load into the final core address register (cards A21 and A24), top left corner of sheet.
- Initiate Drum Read/Write Operation (IRW) - Either IRW function sets the RUN flip-flop (FF), left side of sheet. Initiate Drum Read operation gives control to card A11 - top right corner of the sheet.

Read data from the drum shifts bit - serially into data register zero (cards A6 and A7). When DRO is full, the 16-bit word drops into data register one. When data register two is empty, the word drops from DR1 to DR2. The DSA control logic (card A11) then requests a core access. After the word in DR2 is sent to core, DR2 goes empty. A double core access occurs whenever DR1 and DR2 are both filled. Core accesses continue until there is a core address compare - top left corner (cards A20 and A23). The checkword generator (card A8) is active during Drum Read and Write operations. At the end of each sector during Drum Read operations, the checkword generator is tested for all zeros (card A9).

Initiate Drum Write operation gives control to card A12 - right edge of sheet three. A core access is requested, and the 16 data bits drop into DR1. Like the Drum Read operation, a parallel data transfer occurs between a full data register and an empty one. Therefore, DR1 drops into DR2 and then DR2 transfers into DR0. DR0 is shifted to the drum bit-serially on the write data line via card A12. The 16-bit generated checkword is gated onto the write data line at the end of each sector.

4.3 DETAILED THEORY OF OPERATION

4.3.1 TRACK TIMING NO. 1 (CARD A14)

4.3.1.1 Track Organization. The BG504 is a sector-oriented storage device with 96 data words per sector (see paragraph 1.4.1.4). The following four timing signals from the drum memory unit enable the controller to synchronize the transfer of data into and out of the proper positions on the rotating drum-recording surface:

- Origin Mark (OM) - Defines the start of a track (sector zero) during each revolution of the drum.
- Sector Mark (SM) - Defines the start of each sector recorded on a track.
- Half-Word-Mark (HWM) - Defines the start and middle of each word recorded on a track.
- Bit Clock (BC) - Defines each bit cell location on a track. There are eight BC's for every HWM.

See Figure 5.1 for timing relationships between the four signals.

4.3.1.2 Sector Counter. The sector counter is a 5-bit binary counter which increments on every SM. Note that the clock which increments each of the counters on card A14 is term (OO) . If a timing error occurs (OO) is disabled. The counter is cleared only on CTE. Sector counter outputs are available for sector address status. (See Figure 1.9).

4.3.1.3 Initial Sector Address (ISA) Register and Sector Address Compare (SAC). The ISA register is loaded from bits A0 - A4 on a load ISA function output or set to all ones during Autoload. See sheet 8 of Appendix A for the fan-in logic.

SAC is true when the sector counter and the ISA register are equal; drum data transfers begin at the next sector.

4.3.1.4 Half-Word Counter. Term (OO) increments the 8-bit half-word counter at each HWM. The counter is cleared at each OM or SM. Count sequence is 0 - 15 after OM and 0 - 197 after each SM.

The decoded outputs are required by the read control, write control, and timing error logic.

4.3.1.5 Bit Clock Counter. Every controller clock pulse increments this 3-bit counter. Two decoded outputs, BC6F and BC7F, are used by the read control and write control logic.

4.3.1.6 Gap. Read circuitry in the drum requires 30 microseconds recovery time after track switching. To enable a continuous read from one track to another, SM zero occurs 128 BC's after OM. During this period the GAP flip-flop (FF) is set and no drum data transfers occur.

4.3.2 TRACK TIMING NO. 2 (CARD A15)

4.3.2.1 Track Timing Error Detect. If the three counters on card A14 are not at their predicted states for OM, SM, or HWM two FF's set: one denotes which counter is in error and the other is the TE FF. The TE FF inhibits further incrementing of the counters so that the error condition can be examined with a scope. The error FF's are reset by CTE. Refer to Figure 5.2 for further TE details.

4.3.2.2 Track Address Register 0 and 1. Bits A5 and A6 are loaded into TA0 and TA1 during the load ISA function output. The TA register increments at OM during

Drum Read and Drum Write operation (RCOF or DWC1F false) TAC enables TA2 - TA9 incrementing.

4.3.2.3 Track Address Drivers. The drum memory unit decodes ten track address lines from the controller to select one head. Each line is a twisted-wire pair driven from card A15. See paragraph 1.3.3 for a description of the controller/drum interface circuits.

4.3.3 TRACK ADDRESS REGISTER BITS 2 - 9 (CARD A17)

The eight most significant TA bits are stored on card A17. Bits A7 - A14 are loaded into TA2 - TA9 by LTAF during the load ISA function output. Figure 5.2 shows that the TA increments at each OM during Drum Read and Drum Write operations. The incrementing logic is located on card A15: terms TAC and ITAF.

During Autoload the register is cleared by SUPF. Register outputs TA2 - TA9 are used by the guarded address error and sector overrange error logic (card A18) and by the A-register balanced current mode drivers (cards B12-B14) for sector address status. Outputs TA2F - TA9F are TA driver inputs.

4.3.4 DATA REGISTERS (CARDS A06, A07)

4.3.4.1 Data Flow. Card A06 contains bits 0-7 of the three data registers and card A07, bits 8-15. Data flows through the registers as illustrated in Figure 5.3. Note that the parallel transfer of data from one register to another is the same for Drum Read and Drum Write operations; only the entry and exit points are different. Control of the data registers is located on drum read control (card A11) and drum write control (card A12). Transfers occur from a "full" register into an "empty" register.

4.3.4.2 Data Register Zero. DR0 performs as a serial in/parallel out register for Drum Read operations and as a parallel in/serial out register for Drum Write operations. Data shifts right on each clock when enabled by EWS0F during Drum Write and ERSF during Drum Read.

Read data, RDF, shifts into R00 during Drum Read; R015F shifts in as an "end around carry" during Drum Write. During Drum Write operations DR2 transfers to DR0 after the sixteenth bit of each word is shifted into the drum (LR0WF and $CLKF+ both false). DR0 transfers to DR1 during Drum Read operations.

DR0 outputs are brought off the cards for A/Q data status. DAS provides a two way check on data flow: from core to the input to the drum, and from the output of the drum to core.

4.3.4.3 Data Register One. DSA data drops into DR1 at the trailing edge of reply during Drum Write operations (WBF and $WS0F+ both false). Note the commercial DTL wired - AND gates into DR1. DR1 is loaded with complemented data, so the reset output of each FF connects to DR2.

During Drum Read operations, DR0 transfers to DR1 after the sixteenth bit of each word is shifted into DR0 (LR1RF and $TLKF+ both false).

4.3.4.4 Data Register Two. DR1 drops into DR2 during Drum Read operations (LR2RF and (DD) both false) and also during Drum Write operations (LR2WF and (CC) both false). DR2 outputs are sent to DSA (via cards B6 - B9) along with Write Enable (via card B2) during Drum Read operations.

4.3.5 CORE ADDRESS REGISTER (CARDS A19, A22)

Card A19 contains bits 0-7 and card A22, bits 8-15. During Load Initial Core Address function output the register is loaded with bits A0 - A15 by LICAF.

$IMAF+ increments the register on the leading edge of reply. Outputs are used by the core address compare logic, DSA core address drivers, and core address status drivers. SUPF clears the register during Autoload.

4.3.6 FINAL CORE ADDRESS REGISTER (CARDS A21, A24)

Two identical cards store the 16-bit final core address which is loaded during Load Final Core Address function output by LFCAF. The double-rail outputs are needed by the core address compare logic. GATEF loads $5FF into the register during Autoload.

4.3.7 CORE ADDRESS COMPARE (CARDS A20, A23)

If bits 0-7 of the ICA and FCA registers compare, CACAF is false. If bits 8-15 also compare CAC is true. CAC is sent to the DSA logic on card A11 and to an A/Q status driver.

4.3.8 A/Q RESPONSE (CARDS A26, A28-A36)

A/Q logic is implemented with nine general purpose TTL cards and portions of the controller clock card.

To understand the theory of operation of the A/Q function and status response refer to the following:

- A/Q Response Flow Chart - Figure 5.4
- A/Q Response Timing Diagram - Figure 5.5
- A/Q Flow Logic Diagrams - Sheets 5-8 of logic package (see Appendix A).

The A/Q Flow Logic Diagrams illustrate the functional operation of the nine general purpose TTL cards in positions A28-A36. The card location of each

logic element is indicated within the logic symbol. The logic sheet number of each signal source or destination is indicated in parentheses near the input and output pins. Signals which do not leave a logic sheet are designated by lines not terminated with a pin-block-symbol.

4.3.8.1 Set Run/Run (See Sheet 6 of Appendix A). The RUN flip-flop (FF) enables either the Drum Write control or the Drum Read control logic. The SET RUN FF is set by an Initiate Drum Write (WODF) or Initiate Drum Read (RFDF) output function or by initiating an Autoload (SUPF). RUN then sets after the track address lines have settled 33 microseconds (STDF true). RUN resets at the end of either a Drum Write (WCS5F) or Drum Read (RCS3F) operation. RUN is also cleared by CLR or ALARM.

4.3.8.2 ME2/EOP (See Sheet 6 of Appendix A). The EOP FF sets at the end of a Drum Write or Drum Read operation (RUN reset and ME2 set). EOP is cleared by any non-rejected output function (A36*5 false) or by CLR.

4.3.8.3 BUSY/DATA (See Sheet 7 of Appendix A). The states of the BUSY and DATA FF's determine whether A/Q output functions are rejected. To prevent these FF's from changing state during the output function, GCLK1 is disabled (held false).

BUSY is set whenever the BG504 is unable to perform another operation.
BUSY = SRUN + RUN + CTE.

DATA sets whenever the BG504 is ready to perform a data transfer (Drum Read or Drum Write operation). DATA = $\overline{\text{RUN}} \cdot \overline{\text{CTE}} \cdot \overline{\text{ALARM}}$.

4.3.9 DSA CONTROL (CARD A11)

Refer to publication 60165800 (see Table 1.4) for an in-depth description of the 1700 DSA bus.

The DSA control logic on card A11 can be understood with the aid of Figures 5.6 and 5.7 (flowchart and timing diagram) and the following brief paragraphs.

4.3.9.1 Need Zero. DSA activity starts with N0. A11*21 is true when the write or read control logic needs an access.

4.3.9.2 Need One. N1 instructs the DSA logic not to release the scanner after the first core access: the read control or write control logic must send N1 before Reply is received from the first access to get a second access.

4.3.9.3 Drum Memory Cycle Latch. All DSA devices receive reply. DMC "tells" the BG504 logic to which reply it should "listen".

4.3.9.4 Priority Latch. When the controller wants to access core, it transmits PRIOR to the 1700 to speed-up the DSA scanner operation: once any peripheral has accessed core the CPU is locked out until the PRIOR line is "dropped".

4.3.9.5 Write Enable Delay Latch. During Drum Read operations WREN must be sent to DSA 350 ±50 nanoseconds following request. The WREN Delay Latch drives the delay circuit, Q1. Request cannot drive the delay directly because it can be as narrow as 125 nanoseconds.

4.3.9.6 Increment Memory Address. IMA resets the Priority Latch when A11*25 is true: this releases the DSA scanner. $IMAF+ increments the Core Address Register.

4.3.9.7 Two Only. The TWO ONLY FF prevents the BG504 from getting more than two consecutive memory accesses.

4.3.9.8 Double Access Enable. The decision whether or not to release the scanner is made on the leading edge of reply: IMA strobes A11*25 (Double Access Enable False). The scanner is not released if N1 · $\overline{\text{2 ONLY}}$ · $\overline{\text{CAC}}$ = 1.

4.3.9.9 Core Address Compare Delayed. The CACD flip-flop (FF) enables one additional core access after CAC goes true. This permits one word Drum Read and Drum Write operations. As a result, Core Address Status is always FCA+1 after EOP.

4.3.10 DRUM WRITE OPERATION (CARD A12)

4.3.10.1 Drum Write Control. Each Drum Write operation consists of a six-step sequence as described in Figure 5.8 (flow chart). DWC0, DWC1, and DWC2 FF's form a three-bit shift register which determines which step is active. The register advances each time a clock pulse is gated to A12*16. Note that A12*12 keeps the register cleared whenever a Drum Write operation is not in process.

4.3.10.2 Data Register Load Control (Write). The flow of data through the data registers is illustrated in Figure 5.3.

WR1L, WR2L, and WR0L maintain the "empty/full" status of DR1, DR2 and DR0 during Drum Write operations. Term (S0) keeps the load control FF's cleared during step zero. At the end of reply, during steps one and two, $WS0F+ loads DSA data into DR1 (cards A6 and A7). The load control FF's then enable register-to-register transfers after WR1L is set by WS1. DR2 load-enable is LR2WF (A12*38) and DR0 load enable is LROWF (A12*20).

The data register load timing during steps two and three is illustrated in Figure 5.9. A12*26 is true during step one so DR0 loading does not necessarily wait until WB15 time.

4.3.10.3 Shift Enable (Write). The DATA TIME and CW TIME FF's in conjunction with track timing signals from card A14 determine at what times, during step two through four, data (or zeros) or CW must be shifted to the drum memory unit.

EWS2F shifts write data into the CW generator during steps two through four.

Note that gate C6C inhibits DR0 shift at the time DR2 transfers to DR0 (WB15 Time).

Drum write sector timing is illustrated in Figure 5.10.

4.3.10.4 Need Memory Cycle (Write). The BG504 controller needs a memory cycle whenever DR1 is empty during write control steps one and two. If both DR1 and DR2 are empty a double access is required. WN0F sets the Priority Latch on card A11, and WN1F holds the scanner if a second access is needed.

4.3.10.5 Checkword Generator Input/Write Data. EWS1 and EWS2F are the CWG shift enables during Drum Write operations. The mode of shifting ($0 \rightarrow CW_0$ and $CW_N \rightarrow CW_{N+1}$ or $1 \rightarrow CW_0$ and $\overline{CW}_N \rightarrow CW_{N+1}$) is controlled by WDC and WDCF during data time. WCW and WCWF enable $CW_{15} \rightarrow CW_0$ and $CW_N \rightarrow CW_{N+1}$ during CW time. Bug A2.5 gates CW15F to WDC during step four when zeros are written on the drum. The CWG algorithm is described in Paragraph 4.3.13.

During steps two and three, term (AD) gates R015 onto the $WD+ line while term (AE) gates CW15. Both (AD) and (AE) are false during step four which forces zeros onto the $WD+ line.

4.3.10.6 Lost Data (Write). If DR2 is not full during write control steps two and three when the DR2 → DR0 transfer occurs (WB15 time) lost data occurs.

4.3.11 DRUM READ OPERATION (CARD A11)

4.3.11.1 Drum Read Control. Only four steps are involved in a Drum Read operation (see Figure 5.11). The read control shift register, RC0 and RC1, operates like the write control shift register. A11*9 keeps the register cleared when a Drum Read operation is not in process.

Transfer from step two to step three is delayed until after the CW is tested (see Figure 5.10).

The DR2 → DR0 transfer in step three permits the last data word transferred to core to re-enter DR0 for A/Q data status.

To read the recorded CW via A/Q data status simply ground A11*26. The DR2 → DR0 transfer is inhibited which leaves the CW in DR0.

4.3.11.2 Data Register Load Control (Read). The flow of data through the data registers is illustrated in Figure 5.3.

The "empty/full" status of DR1 and DR2 is maintained by RR1L and RR2L during Drum Read operation. Term (S1) keeps the two flip-flops (FF's) cleared at all times except step one. Register load timing is illustrated in Figure 5.12.

Note that although read data is shifted into DR0 with CLK, all data register-to-data register transfers occur with TLKF.

Figure 5.10 illustrates an eight-bit delay between write data and read data: write data sent to the drum memory unit is not recorded on the rotating surface till eight bit-times later.

RB15 and WB15 are also eight bit-times apart. These two terms define the end of read data words and write data words at the serial controller/drum-memory unit interface.

DR0 doesn't need a FF to remember when it is full. Since DR0 shifts during data and CW times for Drum Read operation it is full only for one bit-time (RB15 time).

4.3.11.3 Shift Enable (Read). ERSF enables DR0 and CWG shift operation during data and CW times in steps one and two (see Figure 5.10).

4.3.11.4 Need Memory Cycle (Read). A core access is required when read data transfers into DR2 (term (K) false). The scanner is held for a second access if DR1 is also full (term (J) false) on the leading edge of a reply.

See Figure 5.3 for a detailed DSA timing diagram for Drum Read operations.

4.3.11.5 Checkword Generator Input For Read. The CRC compare terms (RDC and RDCF) needed during Drum Read operation are generated by bug A2 and gated to card A08 by gates C2A and C2C.

4.3.11.6 Lost Data (Read). If DR1 is already loaded at RB15 time A11*35 is false and the LD FF sets (card A35). Capacitor C11 insures that A11*35 remains true during the CLK pulse at the end of RB15-time even though RR1L is set by the preceeding TLK.

4.3.11.7 Checkword Error. Figure 5.10 illustrates the gross timing of the CWZ strobe. Checkword errors can occur only during Drum Read steps one and two (term (A) true).

4.3.12 AUTOLOAD

So long as the AUTO LOAD push button is depressed, all the data in sectors 0-15 is repeatedly transferred to core locations 0-1535 ($0-$5FF).

The flow chart for this special Drum Read operation is Figure 5.13.

4.3.12.1 Initiate Autoload (Card A26). Like all Drum Read operations, Autoload can be initiated only if a data transfer is capable (DATA true). GATEF and SUPF initialize the controller as described in Figure 5.13. Once the RUN FF sets a normal Drum Read operation is in progress and Figure 5.11 describes the operational sequence.

4.3.13 CHECKWORD GENERATOR (CARD A08)

During Drum Write operation all data from core is processed by the checkword generator and the resulting 16-bit code is written on the drum as the 97th word of each sector.

After 96 data words are processed by the CWG during Drum Read operations, the CWG should contain the same pattern as the recorded CW which follows. After the recorded CW is processed, the CWG should contain all zeros.

Checkword operation is described in Figure 5.14 (flowchart). Note that the CW is generated during data and CW times for Drum Read operation (ERS true); however, for Drum Write operations, only during data time (EWS2 true). When the CW is gated onto the $WD+ line during Drum Write CW-time the CWG simply shifts-right. An end-around-carry feature (CW15 → CW0) leaves the CW in the CWG after Drum Write operations for examination (test points only).

A clip lead can enable the recorded CW to be read via A/Q data status following Drum Read operations (see Paragraph 4.3.11.1).

4.3.14 CLEAR TIMING ERROR (CARD A26)

The CTE FF is set by CLR · TE, where CLR = MCL+ Clear Controller. The CTE sequence is described in Figure 5.15 (flowchart). Note that CTE resets at the beginning of Sector Zero and allows all track timing counters to resume incrementing from a cleared state.

4.3.15 ALARMS

The eight inputs to the ALARM FF are shown on sheet 7 of Appendix A. Only three alarm conditions need explanation.

4.3.15.1 Power Failure (Card A26). A 10v peak-to-peak sine wave appears at A26-9. A26*6 is the integrated value which turns on Q2 and Q3 after the loss of about two ac cycles. A26*22 sets the PF latch at least one millisecond before dc voltages in the controller and drum sag.

4.3.15.2 Guarded Address/SOR Errors (Card A18). These two circuits operate similarly. A full adder produces a carry whenever the contents of the TA register exceed the one's complement of a jumper-assigned number.

During Drum Write operations the carry prevents GAE from setting. Note from card A33 that EGAE = DW · TA8F · TA9F so that even with no carry GAE will not set if either high-order TA bit is set.

A carry sets SOR during Drum Read and Drum Write operations if A18*2 is true. Gate C1C prevents SOR errors when performing Drum Read operations on the last sector of a drum: the TA increments at OM.

4.3.16 SETTLING TIME DELAY (CARD A18)

STDF inhibits the setting of RUN during the 33 microsecond period following TA register loading. The drum memory unit is therefore always provided a 25-microsecond track switching delay which it requires during Drum Read operations.

4.3.17 INTERRUPTS

The three sources of BG504 interrupt are shown in sheet 8 of Appendix A. Note that the TEC interrupt is not programmable.

4.3.18 CONTROLLER CLOCK (CARD A26)

The positive edge of $BC+ triggers the first of three tandem one shots. The first one shot is (factory) adjusted to position the negative edge of $CLKF+ in coincidence with the positive edge of $BC+. The timing relationship between the two clock phases and the bit clock are shown in Figure 5.1.

Section Five

DIAGRAMS

5.1 GENERAL

This section contains the following diagrams:

Figure Number	Title
5.1	Track Timing Diagram
5.2	Track Timing Error Flowchart
5.3	Data Flow Diagram
5.4	A/Q Response Flowchart
5.5	A/Q Response Timing Diagram
5.6	DSA Operation Flowchart
5.7	DSA Single Access Timing Diagram (Drum Read)
5.8	Drum Write Control Flowchart
5.9	Drum Write Data Register Load Timing Diagram
5.10	Sector Timing Diagram
5.11	Drum Read Control Flowchart
5.12	Drum Read Data Register Load Timing Diagram
5.13	Autoload Flowchart
5.14	Checkword Generator Flowchart
5.15	Clear Timing Error Flowchart
5.16	Power Wiring Diagram

5.2 DIAGRAMS

The following pages contain the preceding listed diagrams.

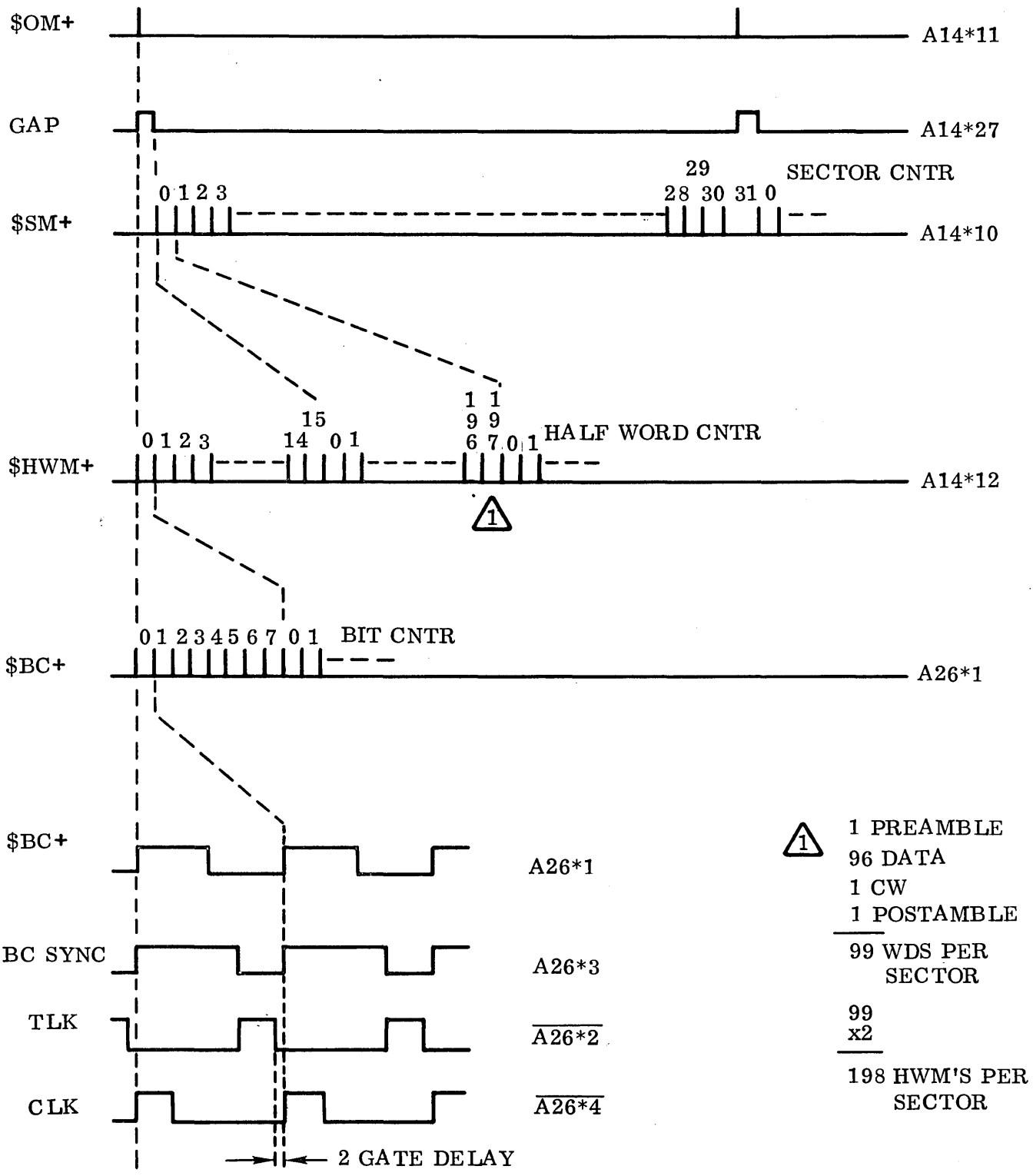


Figure 5.1. Track Timing Diagram

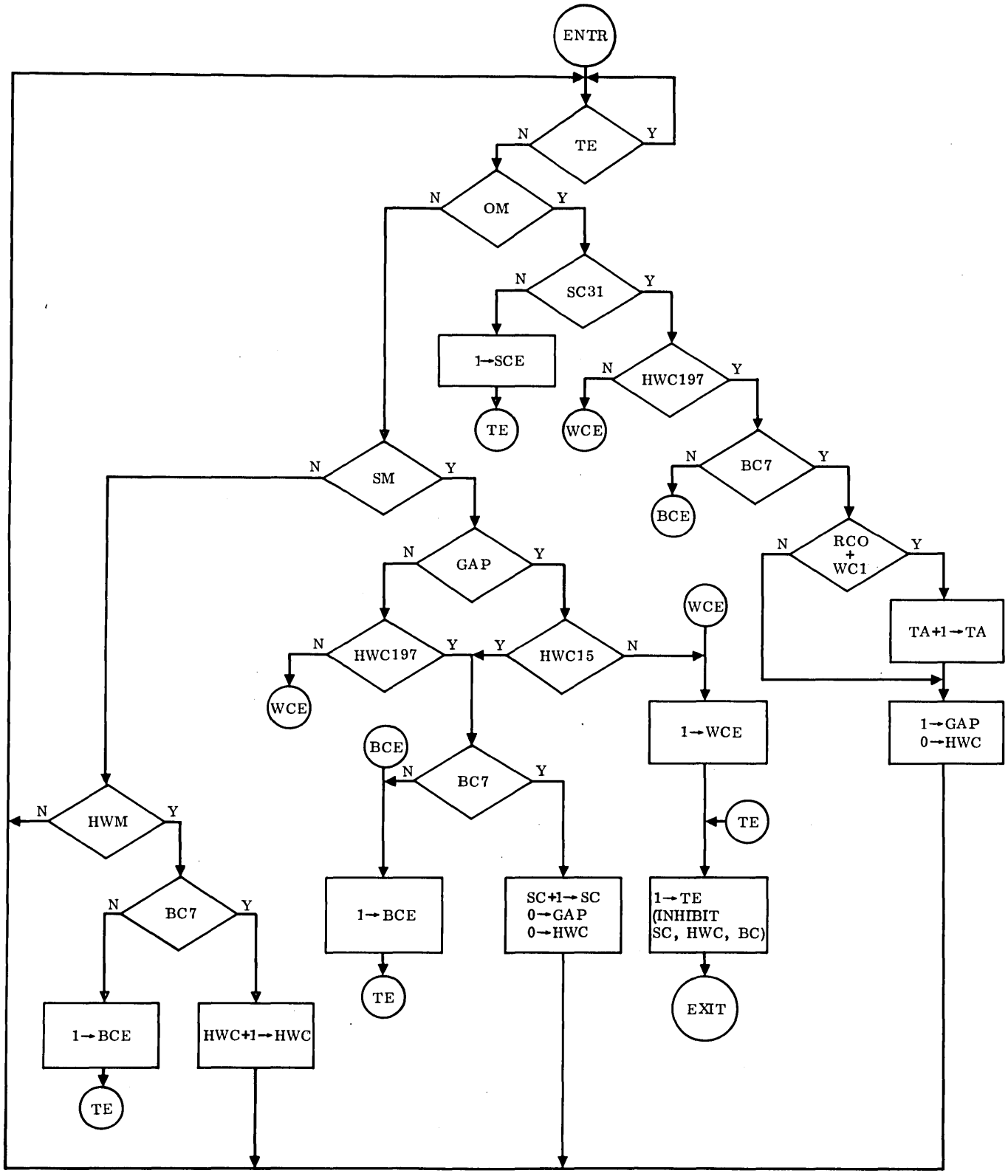


Figure 5.2. Track Timing Error Flowchart

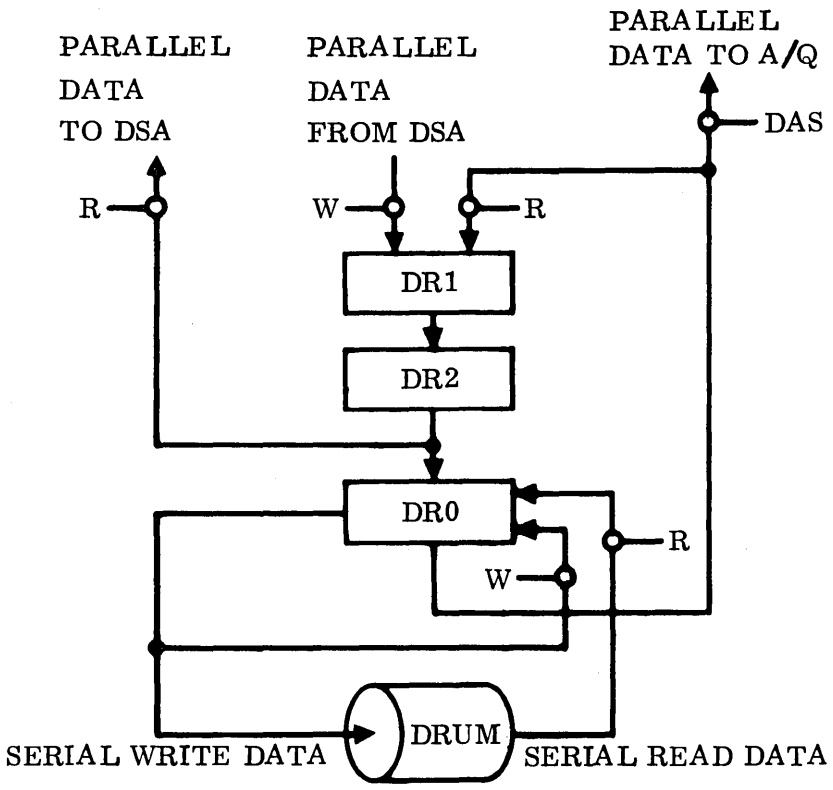
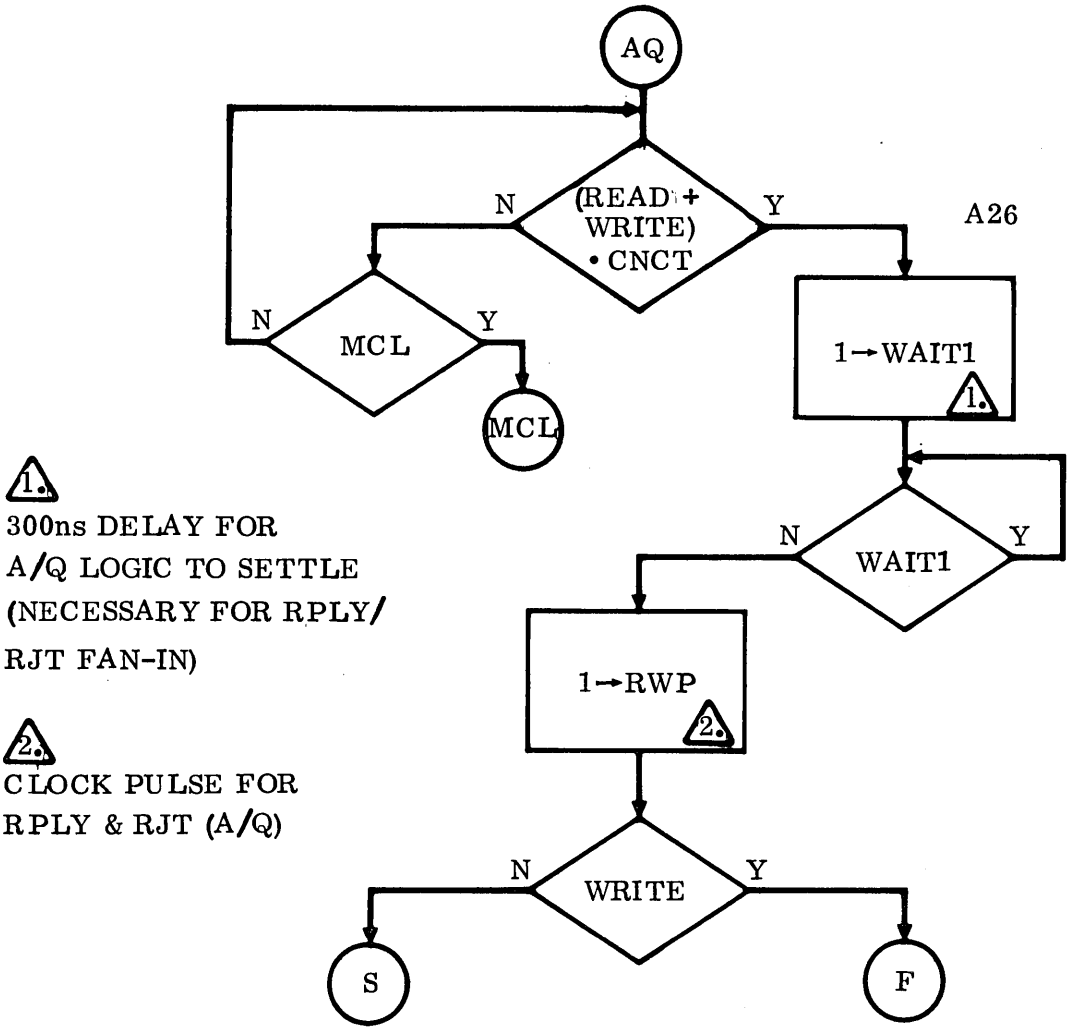


Figure 5.3. Data Flow Diagram



Note: Numbers outside symbols identify card position or sheet on which logic is located (see Appendix A)

Figure 5.4. A/Q Response Flowchart (Sheet 1 of 5)

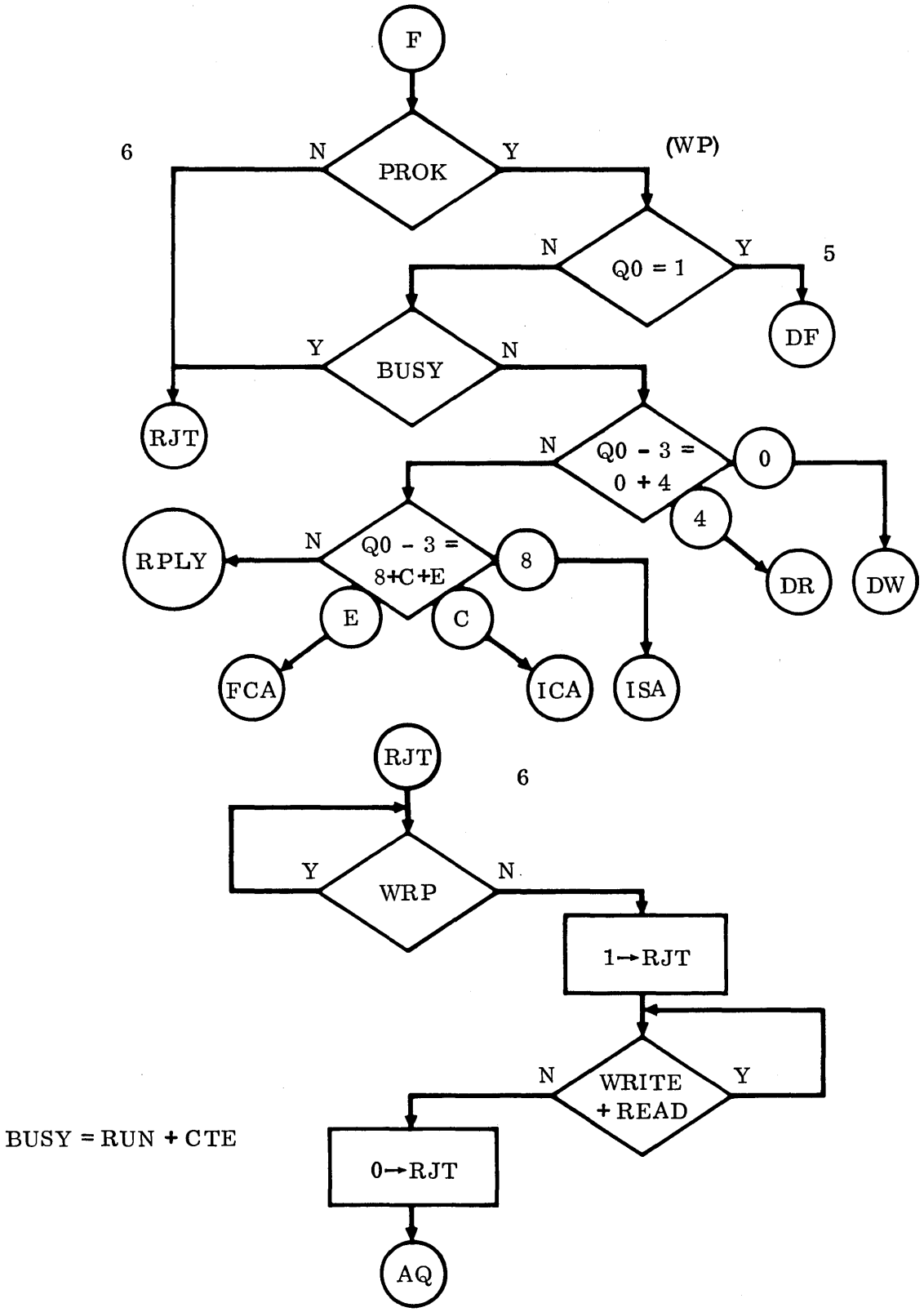


Figure 5.4. A/Q Response Flowchart (Sheet 2 of 5)

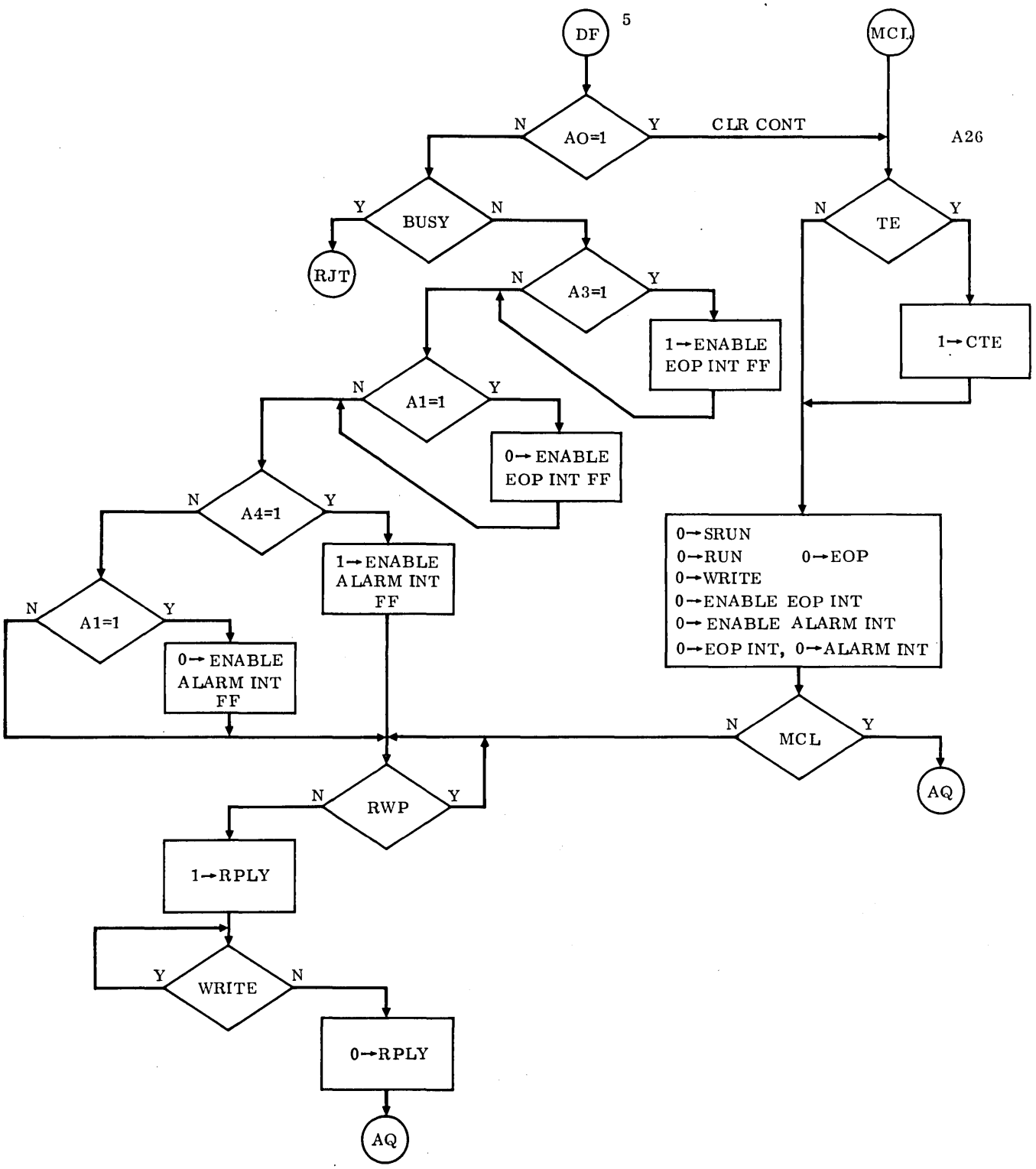


Figure 5.4. A/Q Response Flowchart (Sheet 3 of 5)

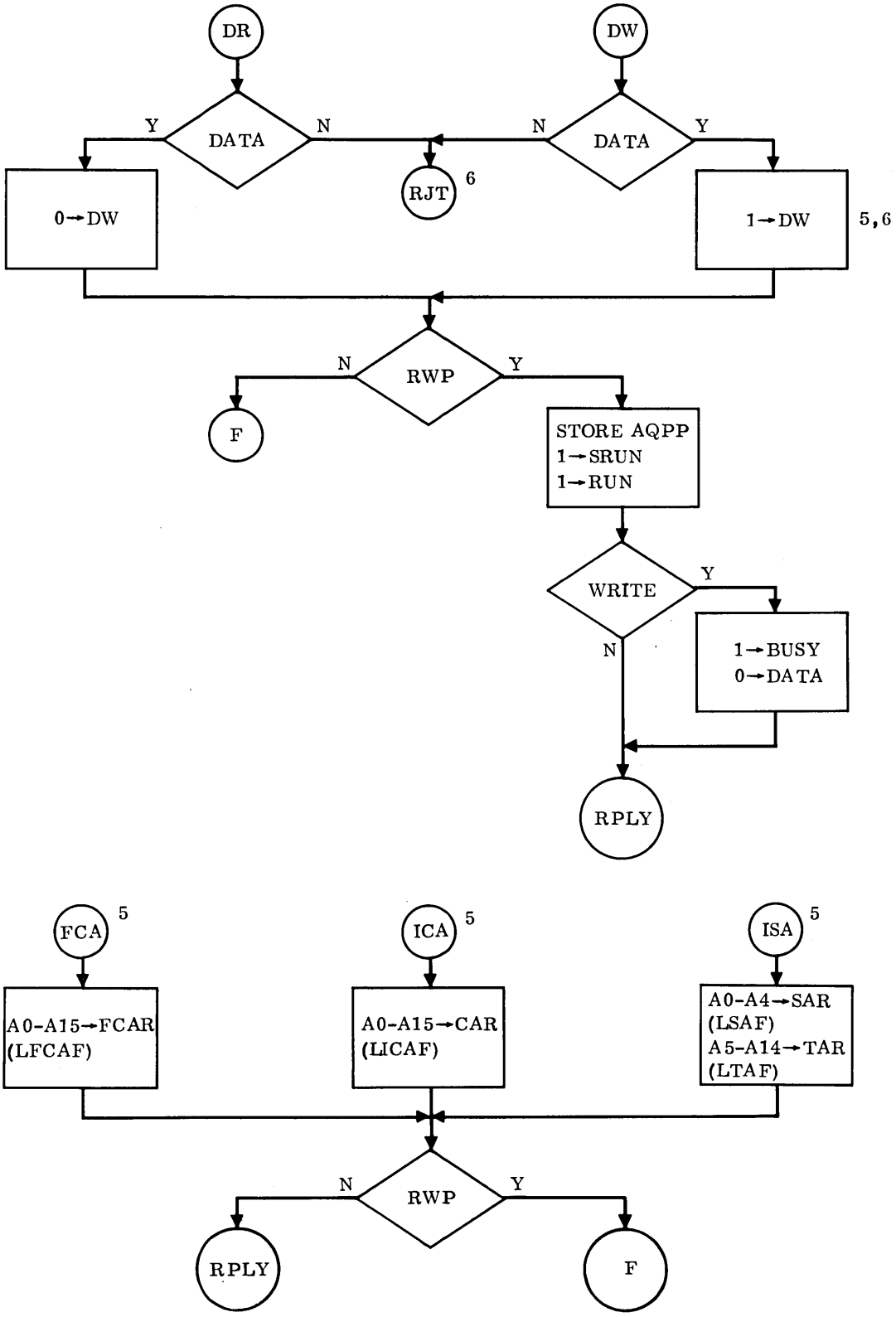


Figure 5.4. A/Q Response Flowchart (Sheet 4 of 5)

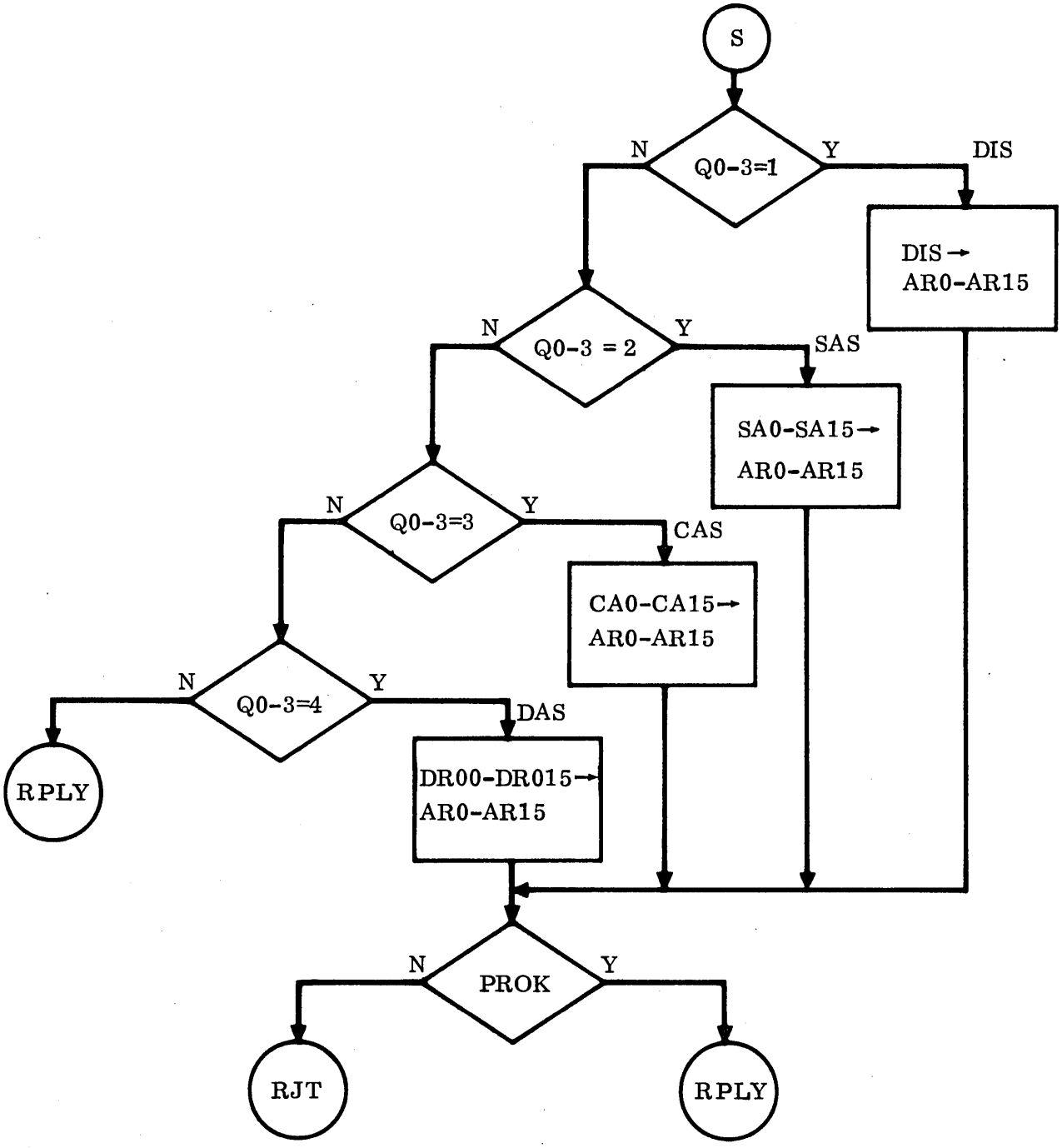


Figure 5.4. A/Q Response Flowchart (Sheet 5 of 5)

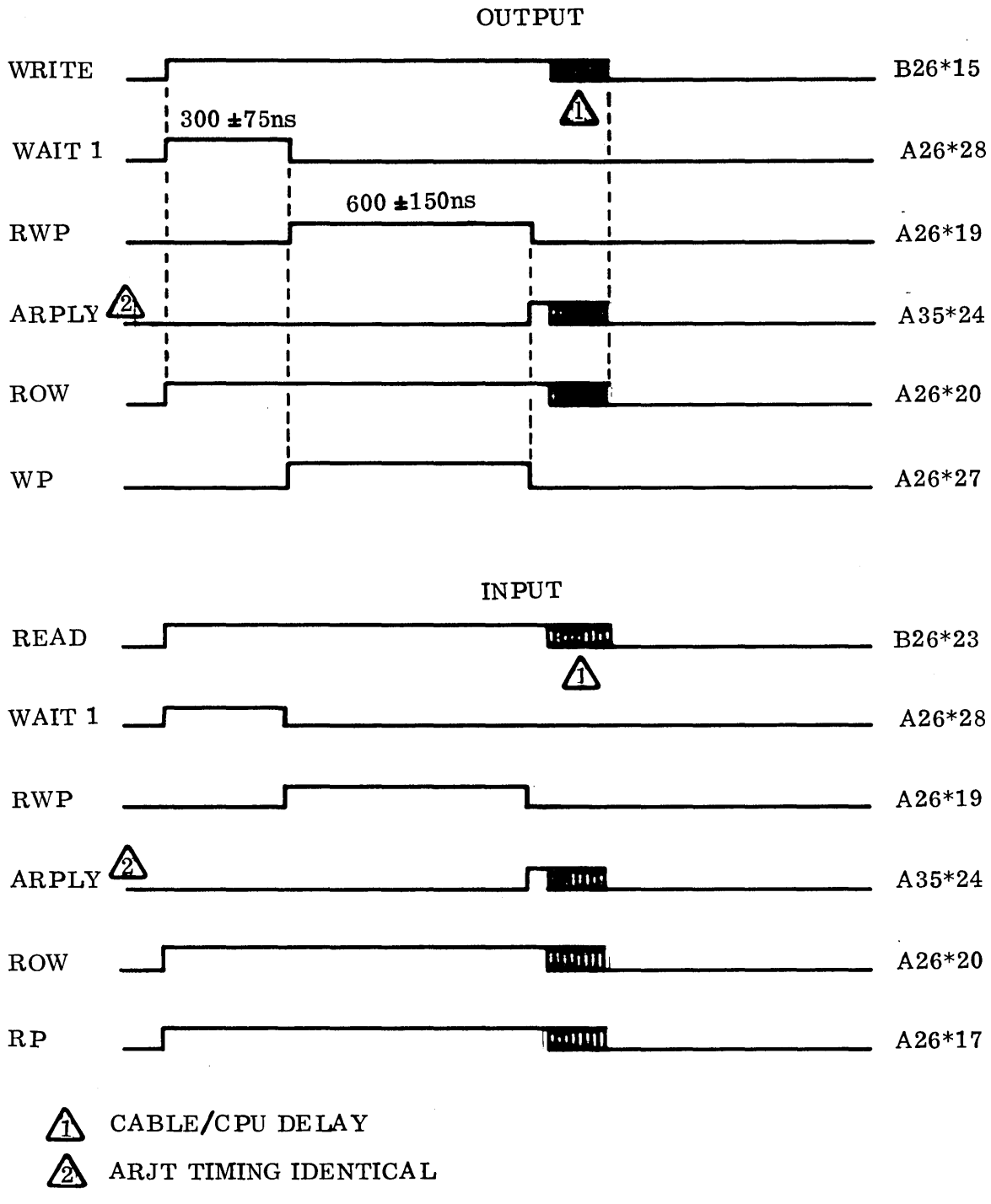


Figure 5.5. A/Q Response Timing Diagram

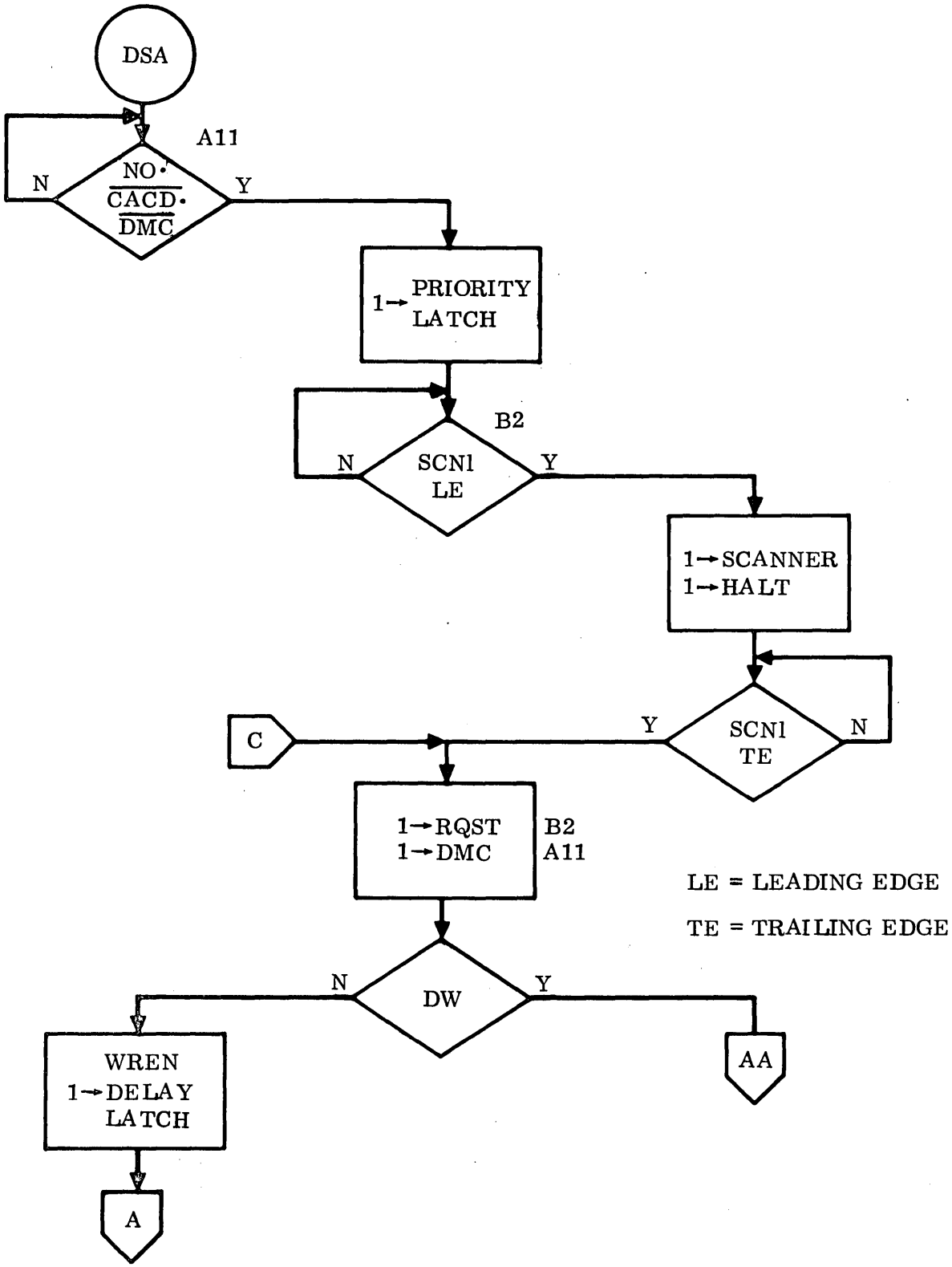


Figure 5.6. DSA Operation Flowchart (Sheet 1 of 3)

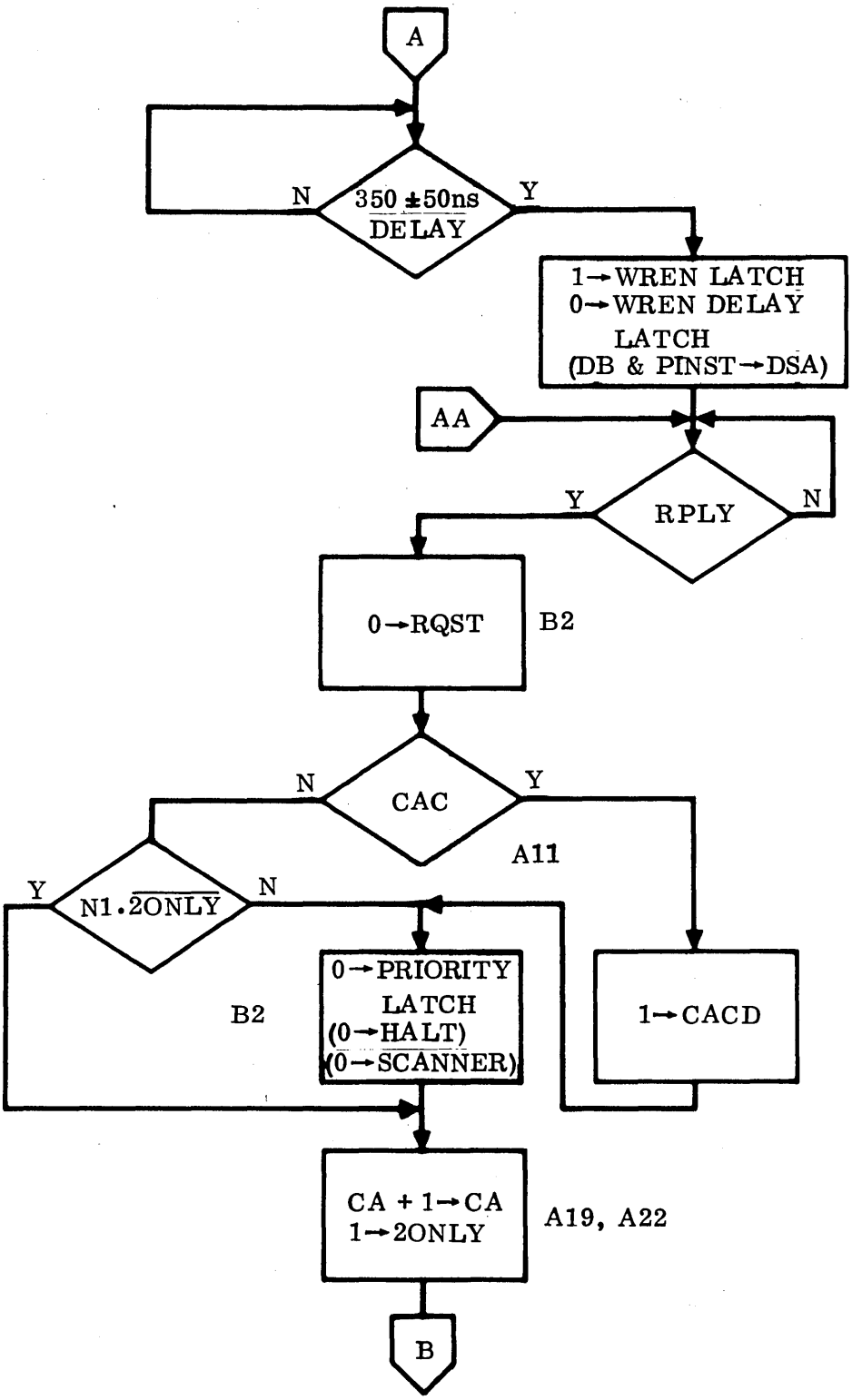


Figure 5.6. DSA Operation Flowchart (Sheet 2 of 3)

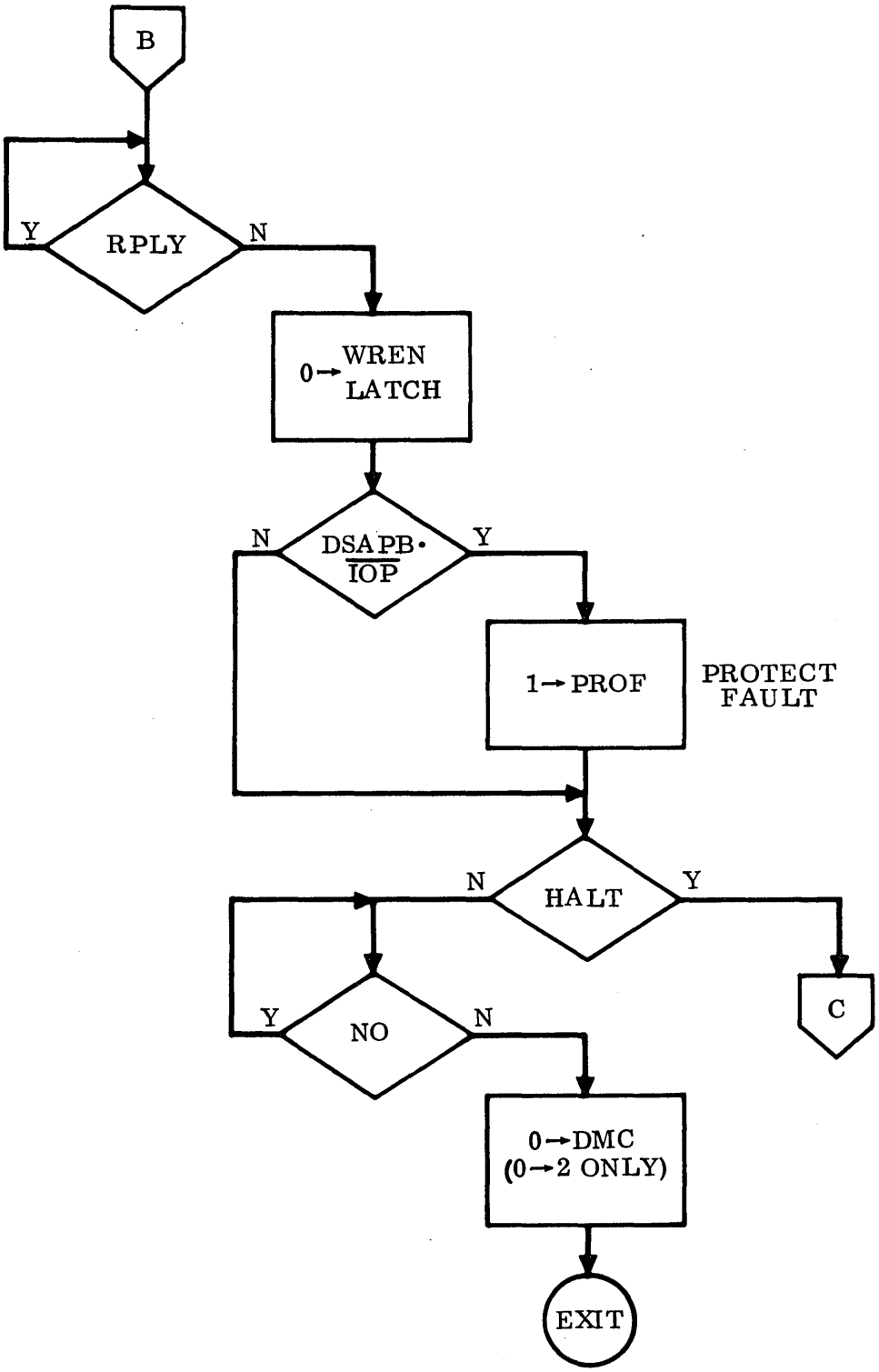


Figure 5.6. DSA Operation Flowchart (Sheet 3 of 3)

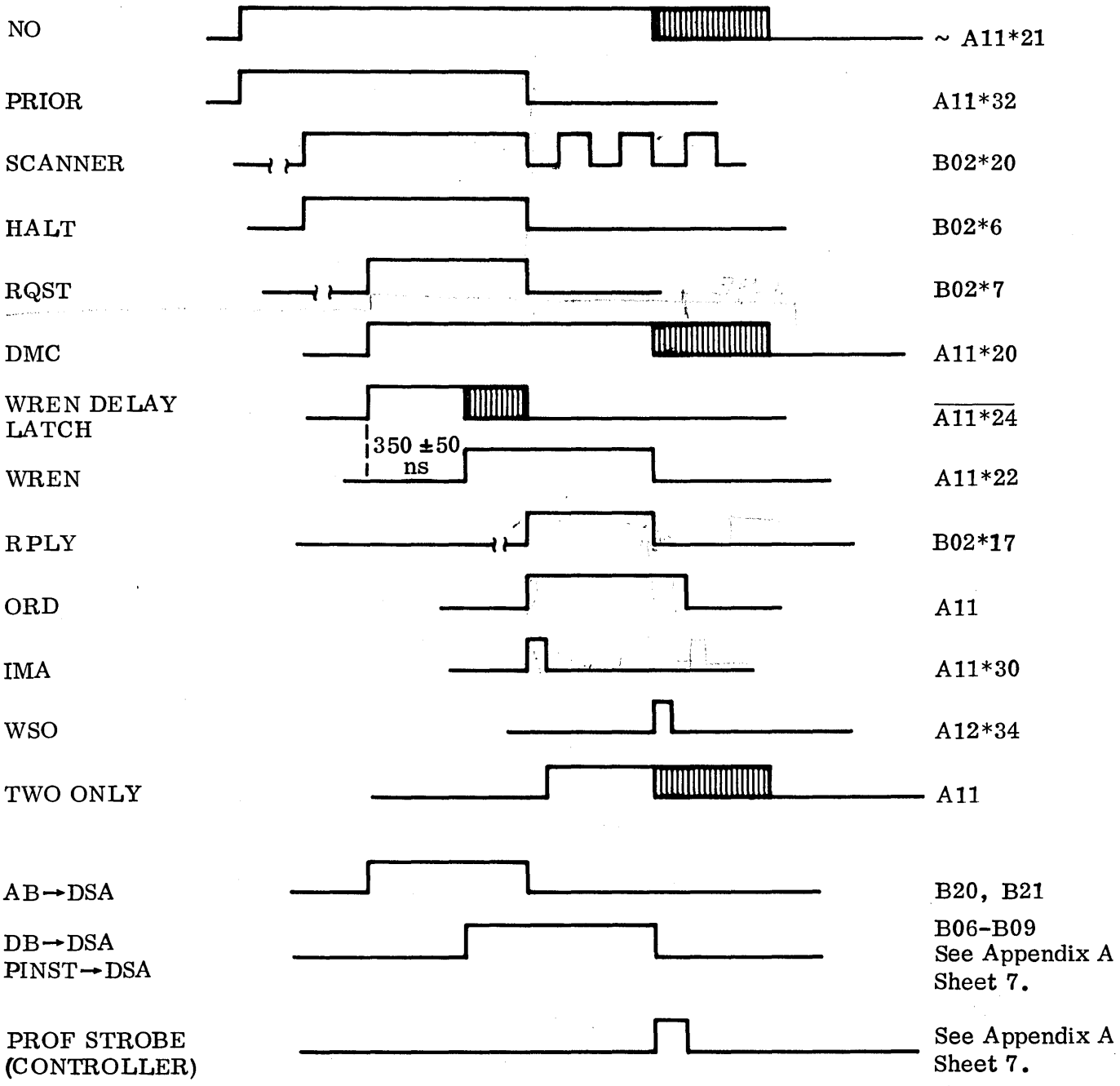


Figure 5.7. DSA Single Access Timing Diagram (Drum Read)

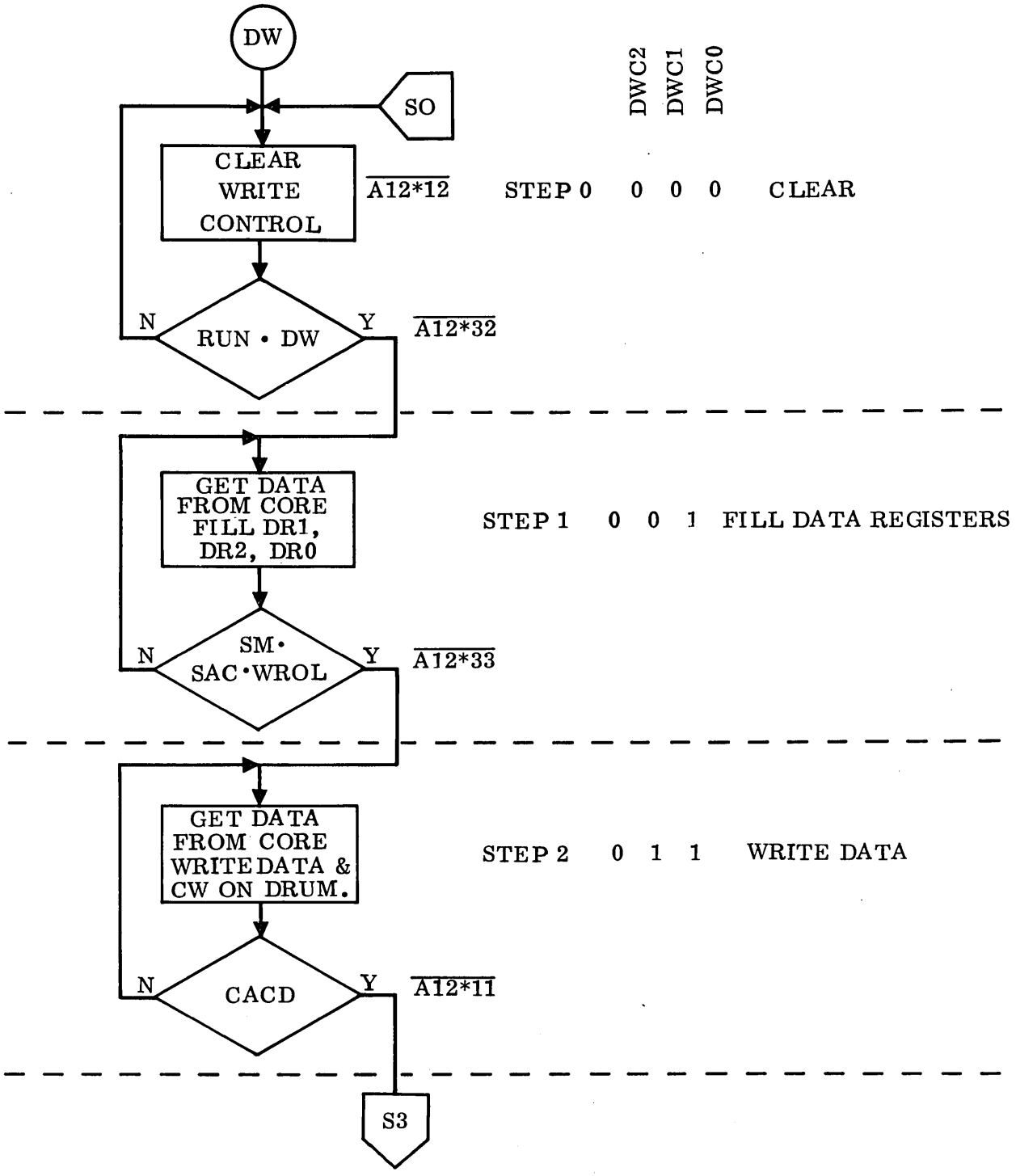


Figure 5.8. Drum Write Control Flowchart (Sheet 1 of 2)

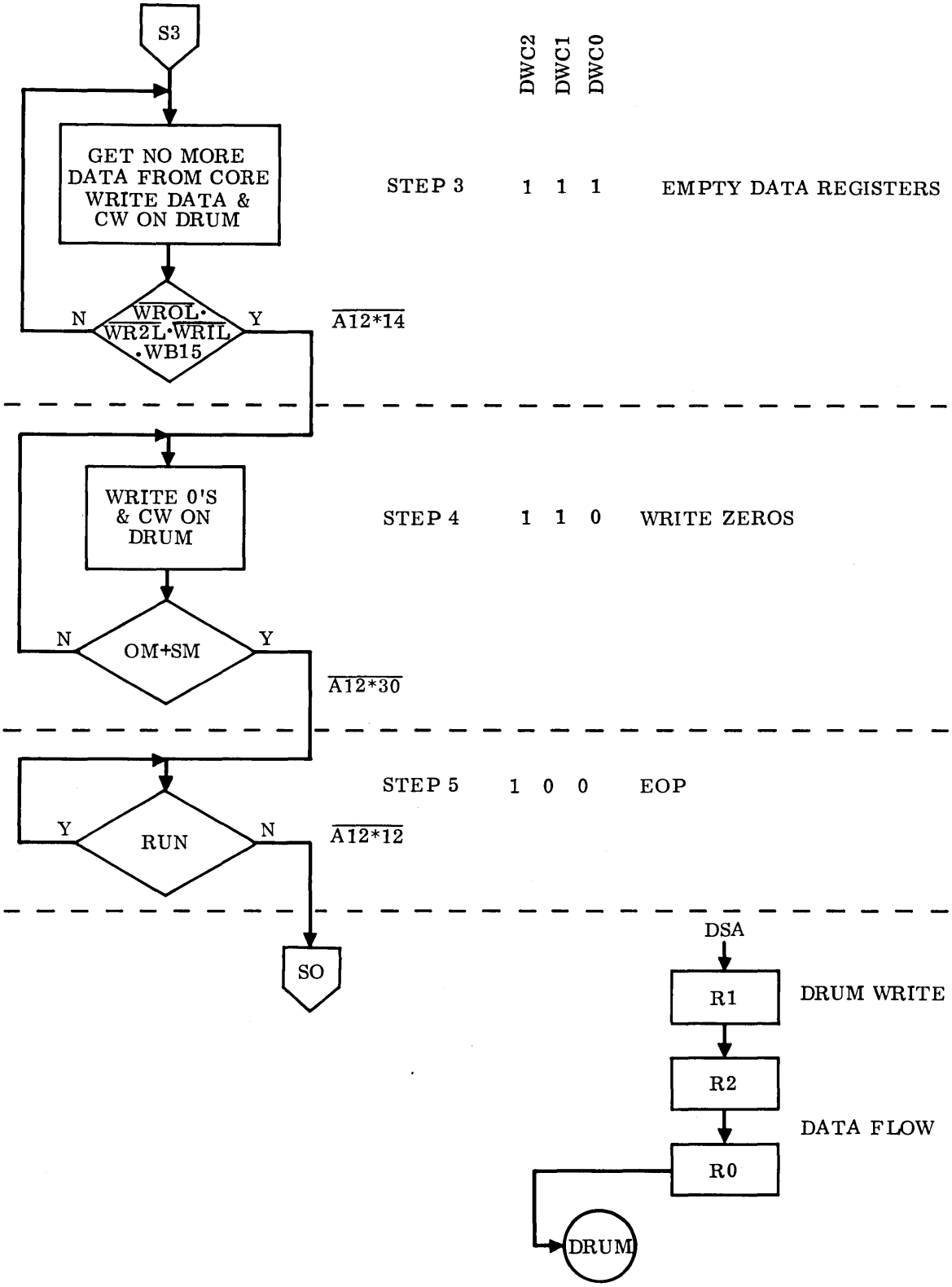


Figure 5.8. Drum Write Control Flowchart (Sheet 2 of 2)

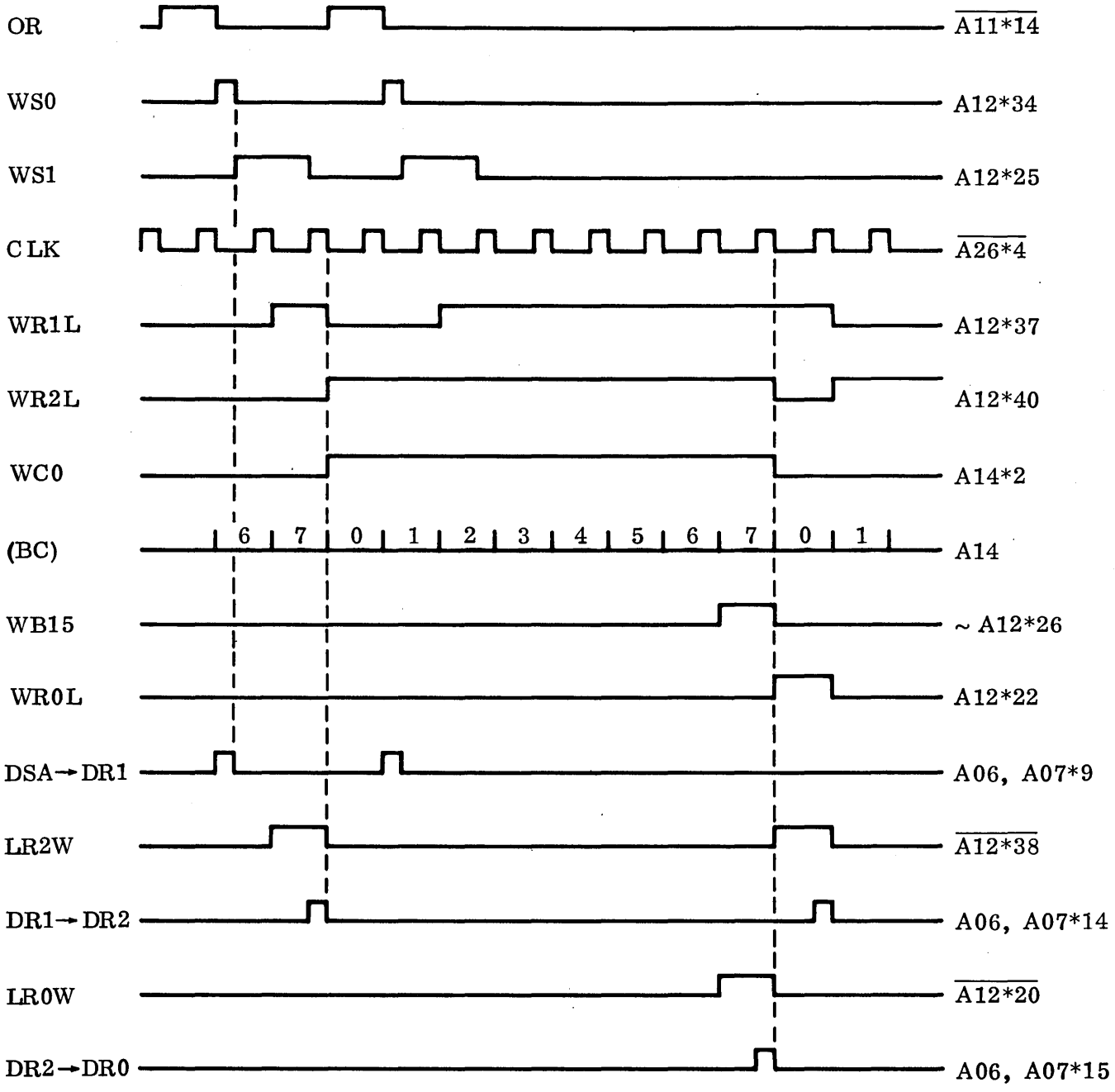


Figure 5.9. Drum Write Data Register Load Timing Diagram

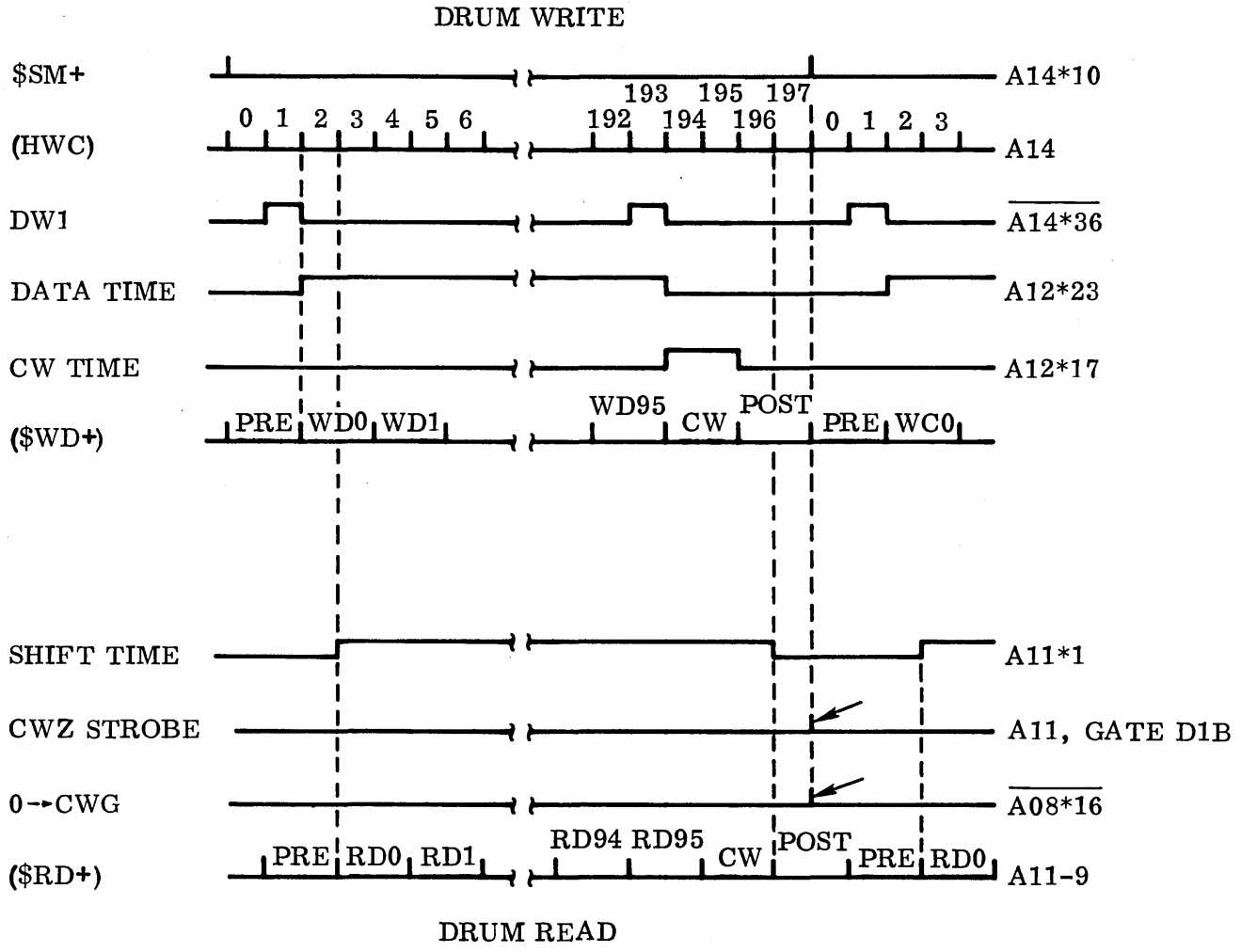


Figure 5.10. Sector Timing Diagram

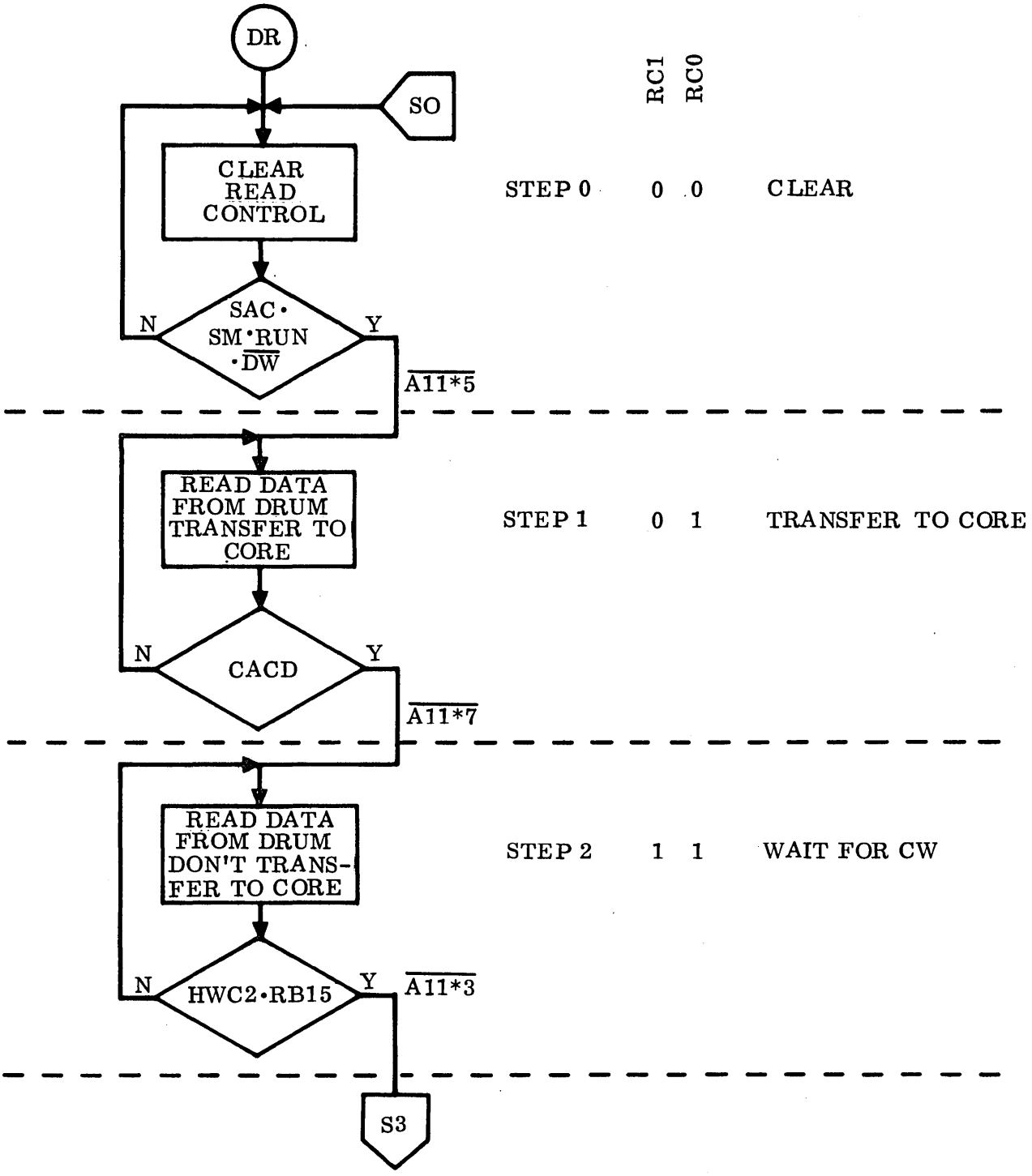


Figure 5.11. Drum Read Control Flowchart (Sheet 1 of 2)

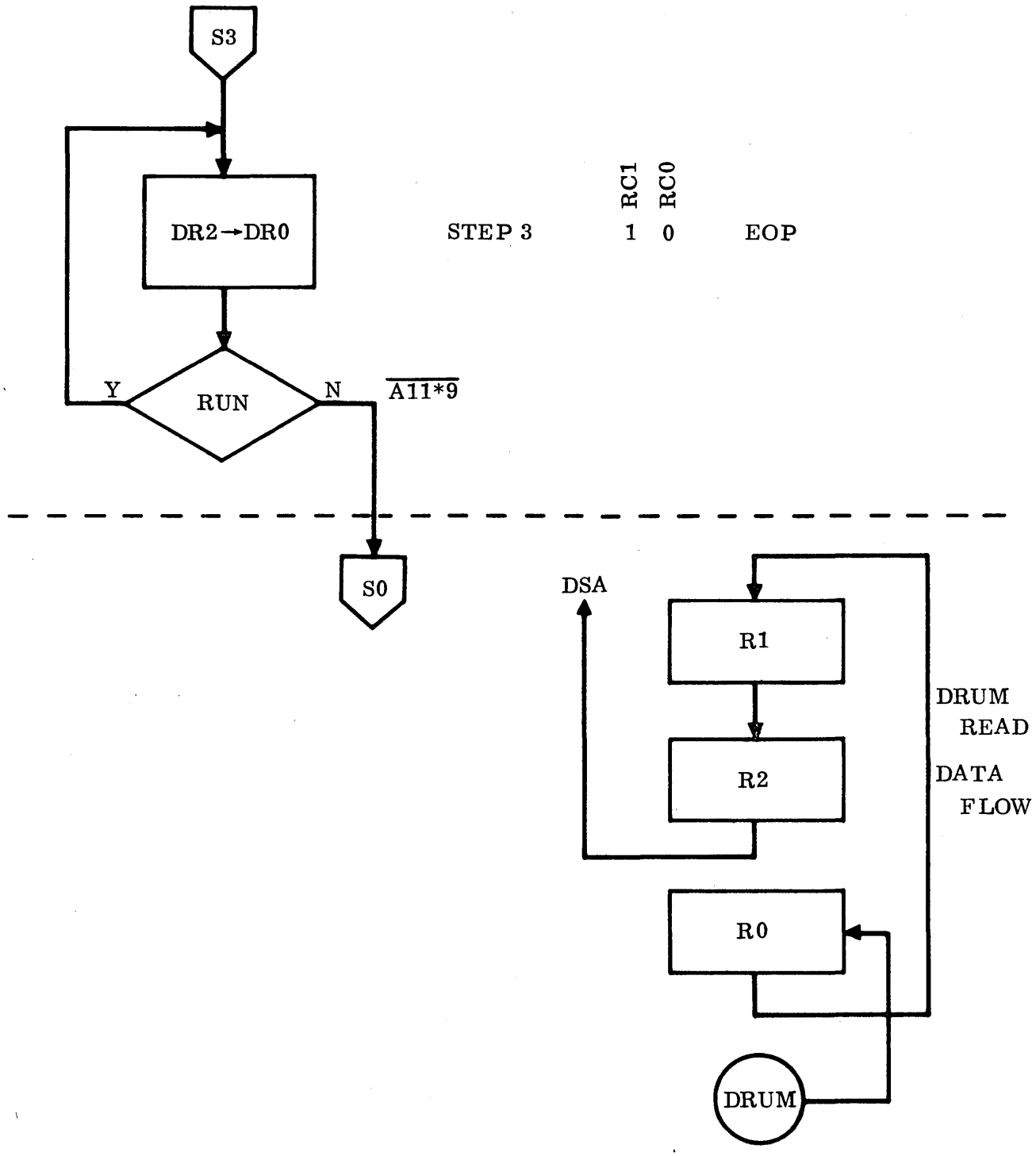


Figure 5.11. Drum Read Control Flowchart (Sheet 2 of 2)

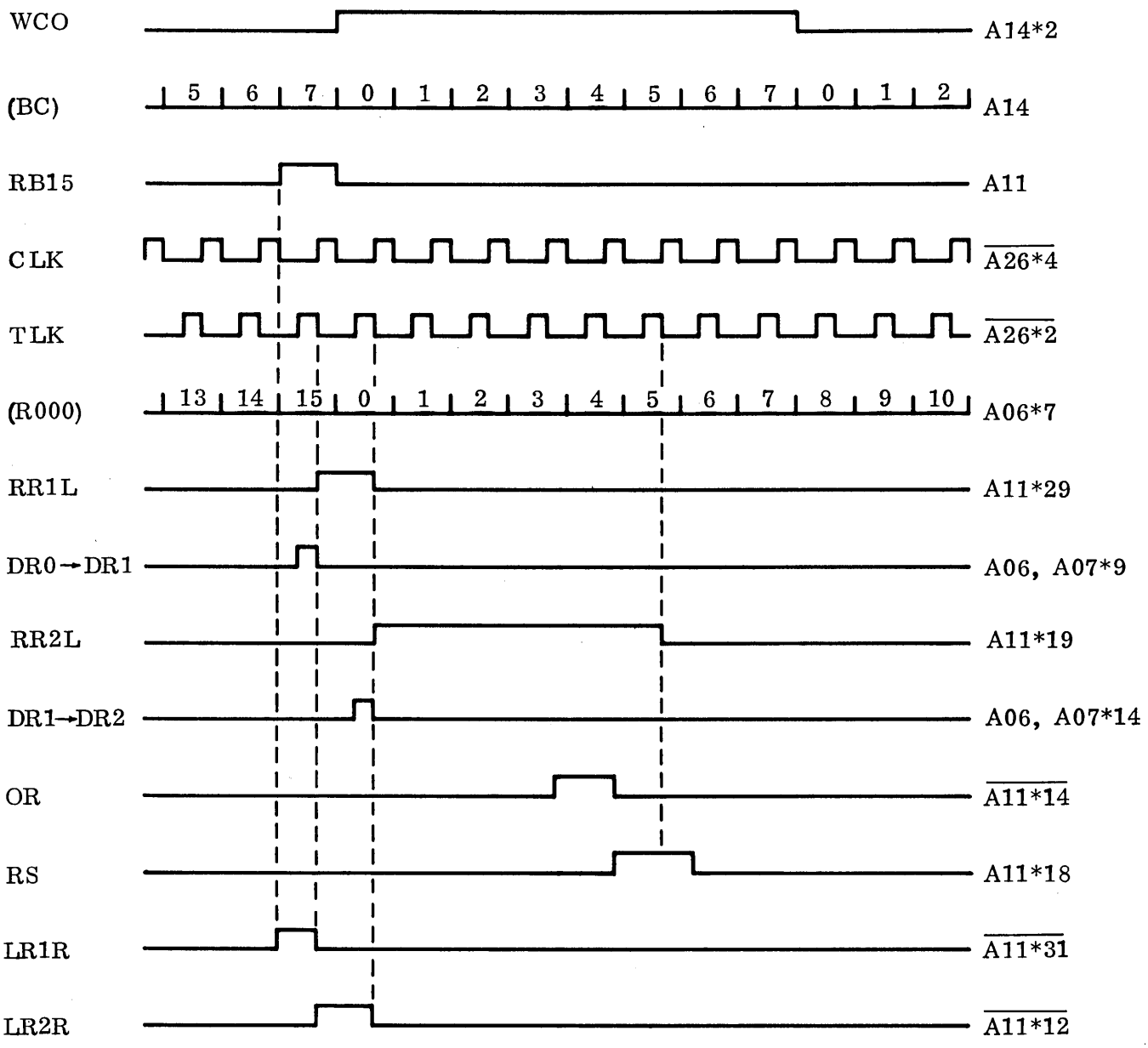


Figure 5.12. Drum Read Data Register Load Timing Diagram

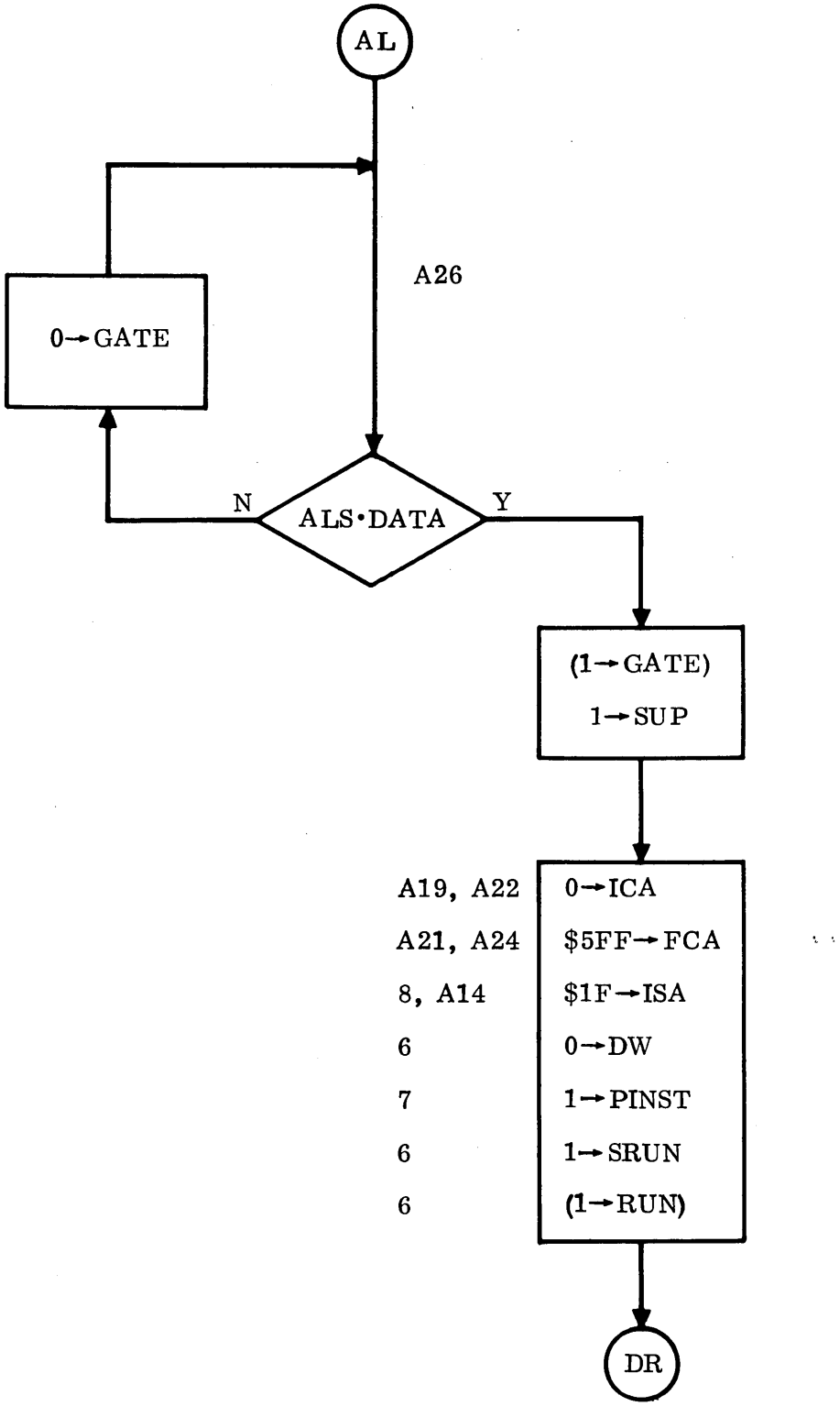


Figure 5.13. Autoload Flowchart

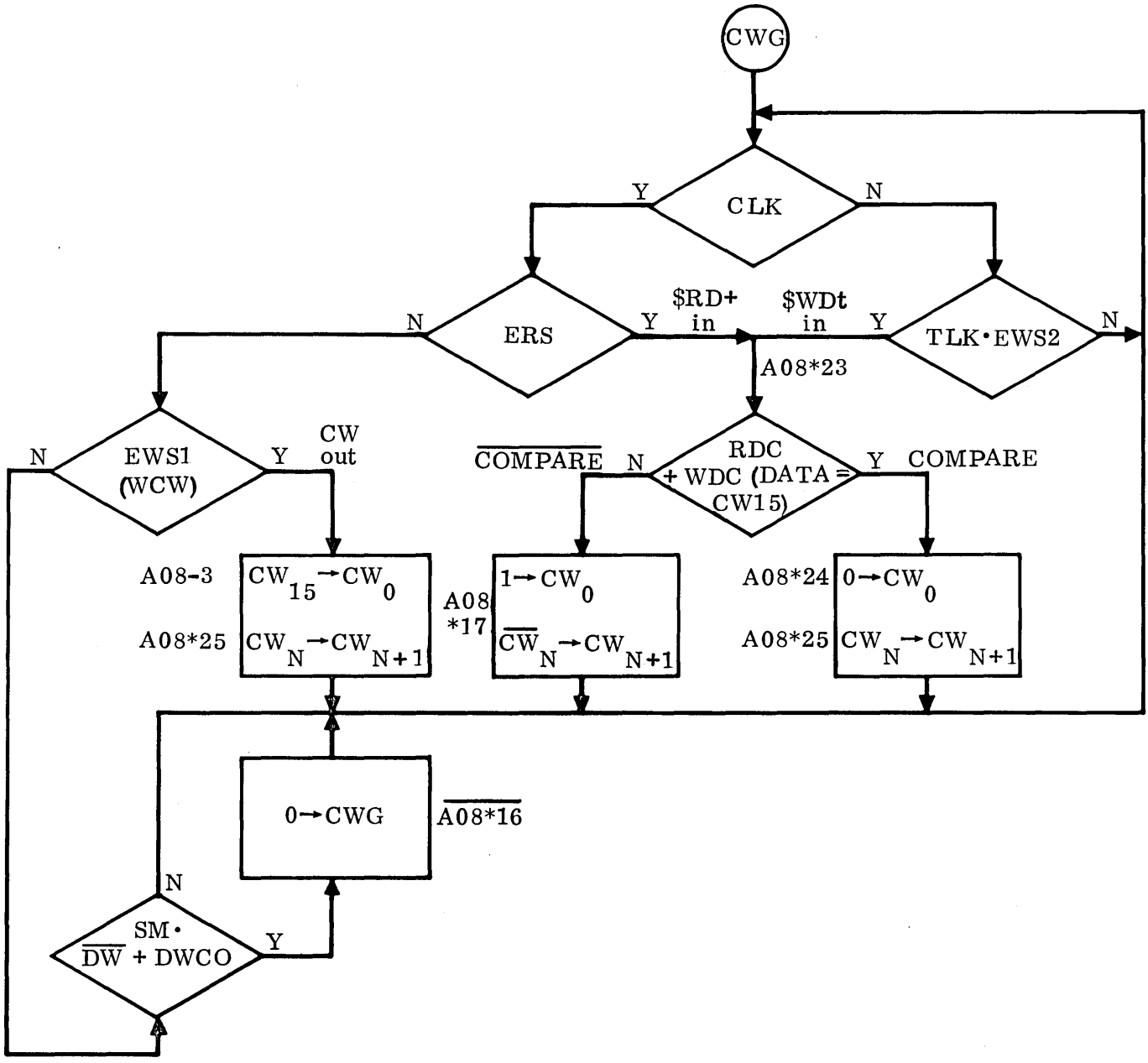


Figure 5.14. Checkword Generator Flowchart

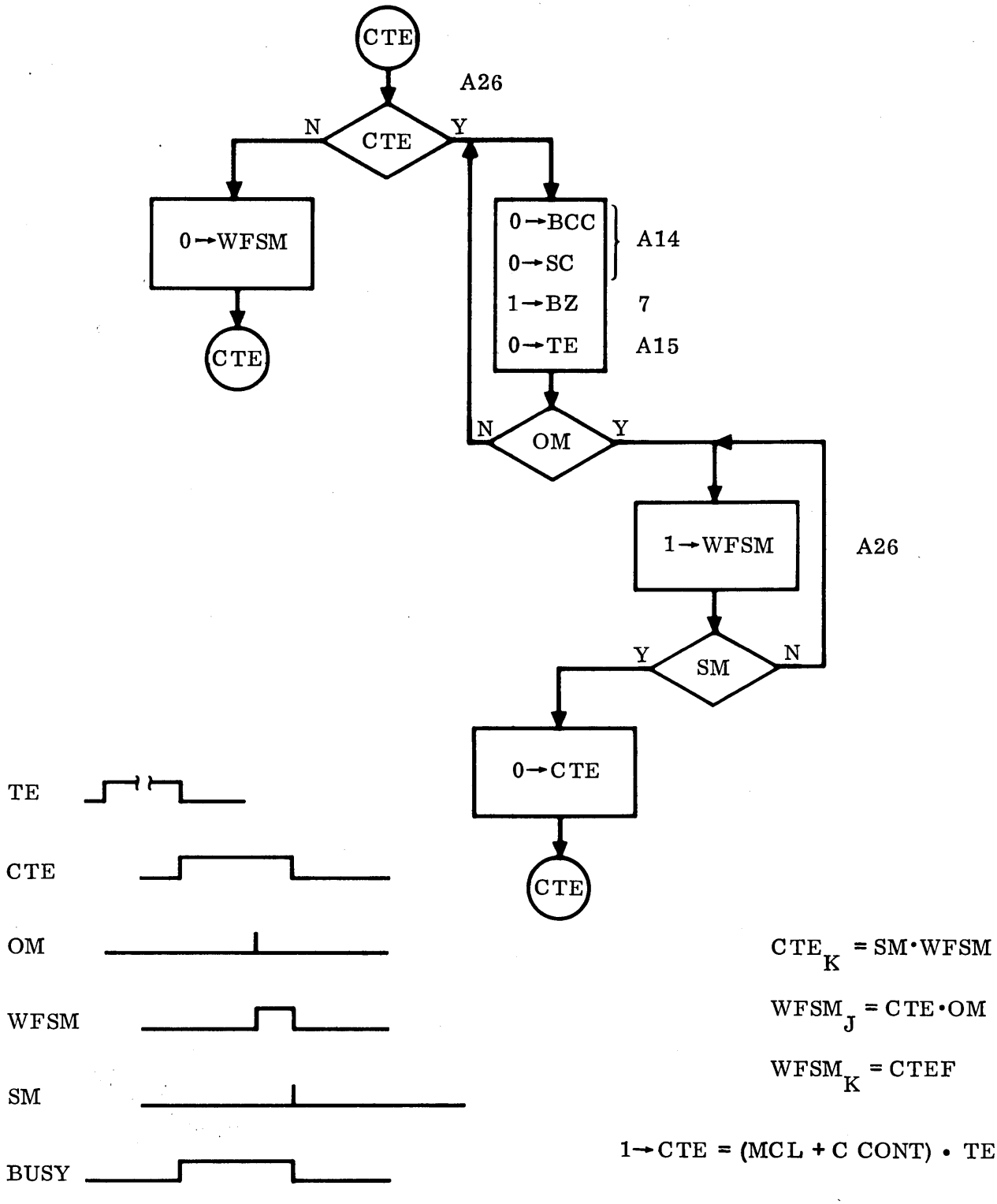


Figure 5.15. Clear Timing Error Flowchart

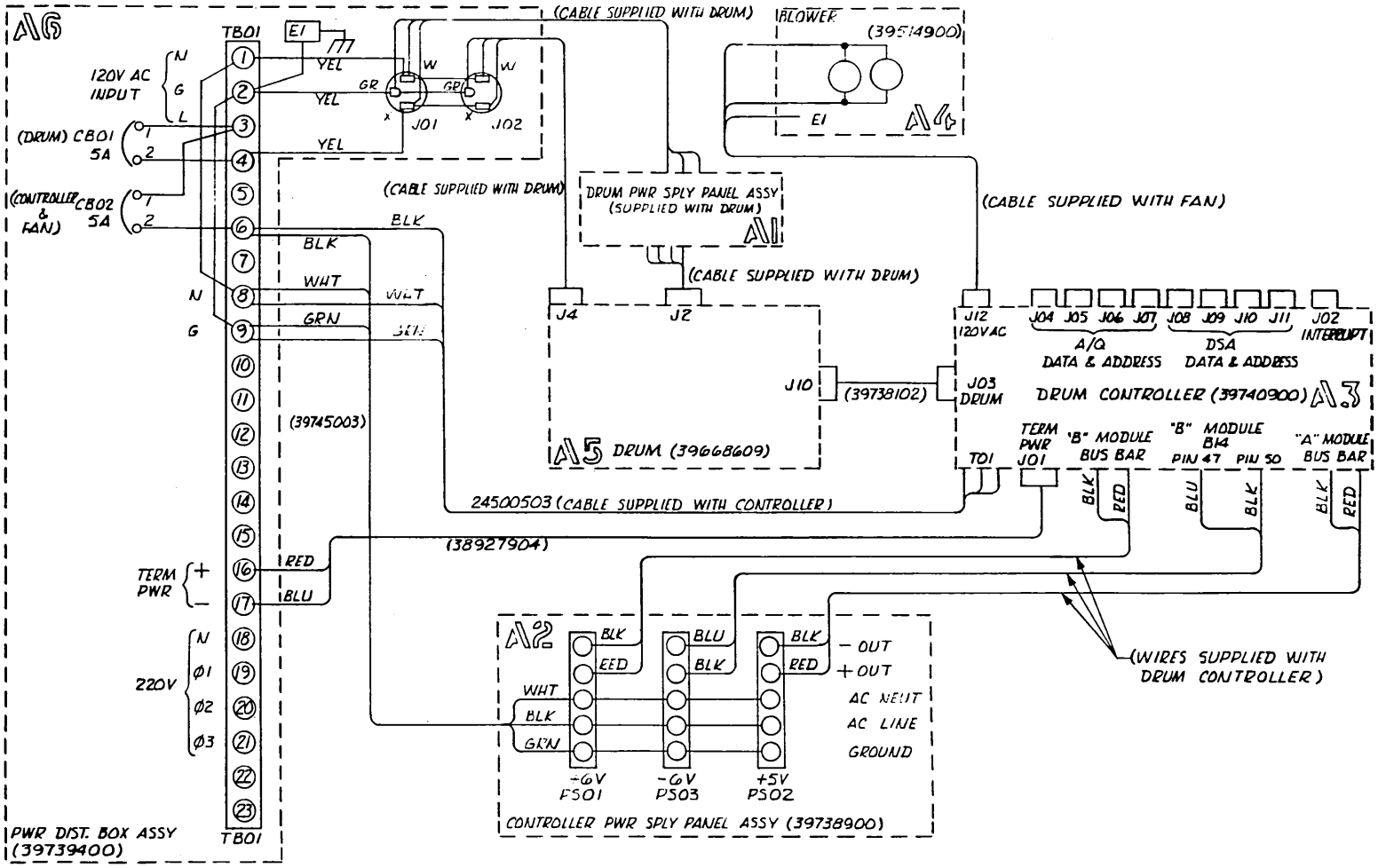


Figure 5.16. Power Wiring Diagram

Section Six

MAINTENANCE

6.1 PREVENTIVE MAINTENANCE INDEX

Perform preventive maintenance as follows:

- Level 1----------Monthly
- Level 2----------Quarterly
- Level 3----------Annually

Estimated Time (Minutes)	Level	Ref. Paragraph	Preventive Maintenance
5	1	6.1.1	Check helium pressure
15	1	6.1.2	Check power supplies and filter
10	2	6.1.3	Run diagnostic
55	3	6.1.4	Run diagnostic with voltage margins

The preceding index provides recommended frequency for performing preventive maintenance on this equipment. Scheduling of this maintenance is a site responsibility. Scheduling may include variations in the recommended frequency due to individual site conditions (i.e., usage, environment, time, etc.,).

6.1.1 CHECK HELIUM PRESSURE

Check/Conditions	Action
Step 1 - Observe helium atmosphere on small gauge on front of drum chassis. It should be between 0.1 and 1.5 psi.	
CHECK: Is pressure acceptable?	
Yes ↓	No → 1. Readjust regulator. Relieve under-cover pressure. Wait for settling. Repeat procedure until reading is 1/4 - 1/2 psi.
	2. If this procedure is necessary too often, a faulty regulator or a leak in the system may be the cause. Monitor the ACUATION PRESSURE LOW lamp to see if it cycles more than about every 10 minutes. If it does, there is a leak in the pressure system. It may then be necessary to call Technical Support for drum maintenance.
Step 2 - Remove front panel and slide drum out to read high pressure gauge. Use a suitable mirror (see paragraph 7.1.2) to read this gauge from the rear. This can be accomplished without removing the panel or extending the chassis. The pressure should read from 300 to 2200 psi.	

Check/Conditions	Action
CHECK: Is reading above 300 psi?	
Yes	No → 1. Turn off drum power. 2. Replace helium bottle by executing following steps: a. Turn off helium bottle pressure valve. b. Turn off regulator. c. Remove old bottle. d. Inspect and clean mating surfaces. e. Install new bottle. f. Turn on helium bottle, fully open. g. Relieve under cover pressure. h. Open regulator to a slight flow. i. Relieve pressure again and wait for new setting to settle out. j. Repeat as necessary to achieve approximately 1/4 psi.
↓	
Next Item	

6.1.2 CHECK POWER SUPPLIES AND FILTER

Check/Conditions	Action
Step 1 - Measure all supplies for their nominal voltages and ripple tolerances. Keep a record to see if there is a degrading history.	

Check/Conditions	Action
±6 vdc, +5 vdc ---- 25 millivolt RMS ripple (70 millivolt peak to peak) - Controller +5 vdc, + 25 vdc, -12 vdc --- 300 microvolt RMS ripple (3 millivolt peak to peak) - Drum Memory	
CHECK: Power supplies acceptable?	
Yes ↓	No → 1. Check for blown fuses, circuit shorts, open diodes, proper input voltages, proper grounding, etc... Repair or replace defective components or supply. Do not void drum memory unit warranty.
Step 2 - Check the blower filter.	
CHECK: Filter clean?	
Yes ↓ Next Item	No → 1. Vacuum the filter or clean with mild soap and water if necessary. 2. If filter cannot be easily cleaned, replace.

6.1.3 RUN DIAGNOSTIC

Check/Conditions	Action
Step 1 - Run SMM17, V3.0, Test 80 (See Appendix B)	
Step 2 - Repeat the test several times.	

Check/Conditions	Action
CHECK: Any diagnostic errors ?	
No ↓ Next Item Yes ⟶	1. The flexibility and usefulness of the drum diagnostic as described in Appendix B, should allow relatively quick problem isolation. Repair or replace the faulty component or assembly. Note: Any failure indicated as being under the drum cover shall require qualified personnel from Regional Technical Support. Do not void drum memory unit warranty.

6.1.4 RUN DIAGNOSTIC WITH VOLTAGE MARGINS

Check/Conditions	Action
Step 1 - Run the drum diagnostic (See Appendix B) but omit Section 0 (Clock Adjustment).	
Step 2 - Repeat the diagnostic at nominal voltage settings.	
CHECK: Any diagnostic errors ?	
No ↓ Yes ⟶	1. Repair or replace faulty component.
Step 3 - Run the diagnostic twice with all supplies at +5% margins.	Note: See above note (Paragraph 6.1.3).

Check/Conditions	Action
CHECK: Any diagnostic errors?	
No ↓ Yes →	1. Check for deterioration in grounds, power supplies, cabling, or connectors, IC's, etc.,. Repair or replace failing part. Do not void drum memory unit warranty.
Step 4 - Run the diagnostic twice at -5% margins.	
CHECK: Any diagnostic errors?	
No ↓ Yes →	1. Same as preceding action.
Step 5 - Return system to nominal voltage settings. Re-run the entire diagnostic to verify operation while lightly shock testing the unit.	
CHECK: Any diagnostic errors?	
No ↓ Yes →	1. Replace shock sensitive component or assembly.
End of Maintenance	

6.2 CALIBRATION AND ALIGNMENT

The following two potentiometers in the controller are factory set and therefore not likely to need further adjustment.

6.2.1 CONTROLLER CLOCK ADJUSTMENT (CARD A26)

This adjustment synchronizes the controller clock to the track timing recorded on the drum surface. Adjustment can be made during all power-on conditions

of the BG504. The negative-going edge of $CLKF (A26*4) is aligned with the positive-going edge of $BC+(A26*1) within ±5 nanoseconds. See paragraph 4.3.18 for a description of the circuit.

6.2.2 DSA WRITE ENABLE ADJUSTMENT (CARD A11)

This adjustment establishes the time delay between transmission of $RQST and $WREN by the BG504 during Drum Read operations. The delay must be 350 ±50 nanoseconds. Refer to publication 60165800 (see Table 1.4). Adjustment must be made during Drum Read operations. The positive-going edge of WREN (A11*22) must be delayed 350 ±50 nanoseconds from the positive-going edge of RQST (B02*7).

6.3 TROUBLESHOOTING

The recommended troubleshooting procedure is to run entire diagnostic and examine printouts (see Appendix B). If the failure can be localized to a specific logic area, replace suspected assembly (for example card substitution in controller or IC replacement on drum memory unit logic card). If the failure cannot be isolated, program diagnostic to loop on first section which fails and signal trace; disable the printout for this mode.

If the failure occurs under shroud of drum memory unit, call Technical Support. Only qualified personnel may make repairs under the drum cover. Do not void drum memory unit warranty.

Controller Card Interchangeability

Card Type	Card Description	Card Positions
1LCT	Data Register	A06, A07
9GJT	TTL Gate, High Fan In	A09, A33
9GET	TTL Inc. Reg, 8-Bit	A17, A19, A22
9GHT	TTL Compare, 8-EOR	A20, A23
9GFT	TTL CNTR/Reg, 8-Bit	A21, A24
9GKT	TTL Gate, Low Fan In	A28, A30, A32, A34, A36
9GLT	JK Flip-Flop, 5	A31, A35
1LKT	3/4/4 Gated T/R, TTL	B06, B07, B08, B09, B11, B12, B13, B14
1LLT	GP Transmitter, TTL	B20, B21

Section Seven

MAINTENANCE AIDS

7.1 MAINTENANCE AIDS

7.1.1 TEST POINTS

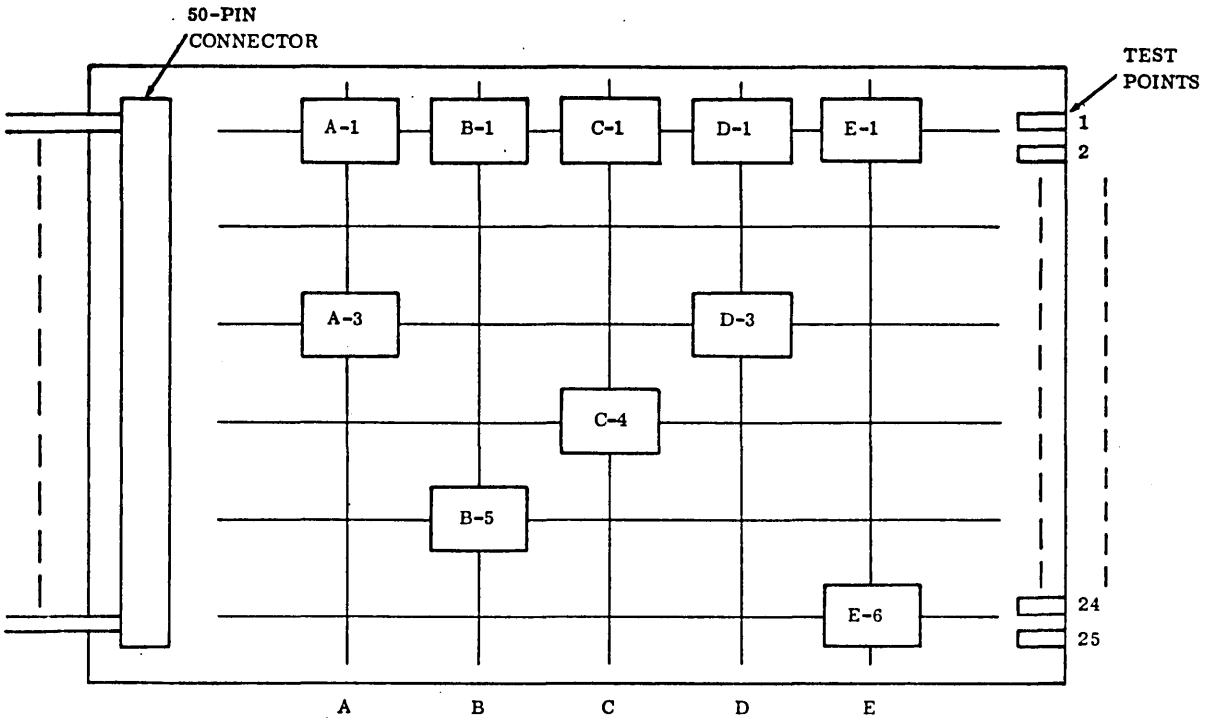
- All*26: Keeps checkword in DR0 after drum read operation when grounded so that checkword can be read via AQ data status.
- B02*5: Inhibits $WREN when grounded so that BG504 cannot write into core.

7.1.2 TOOLS

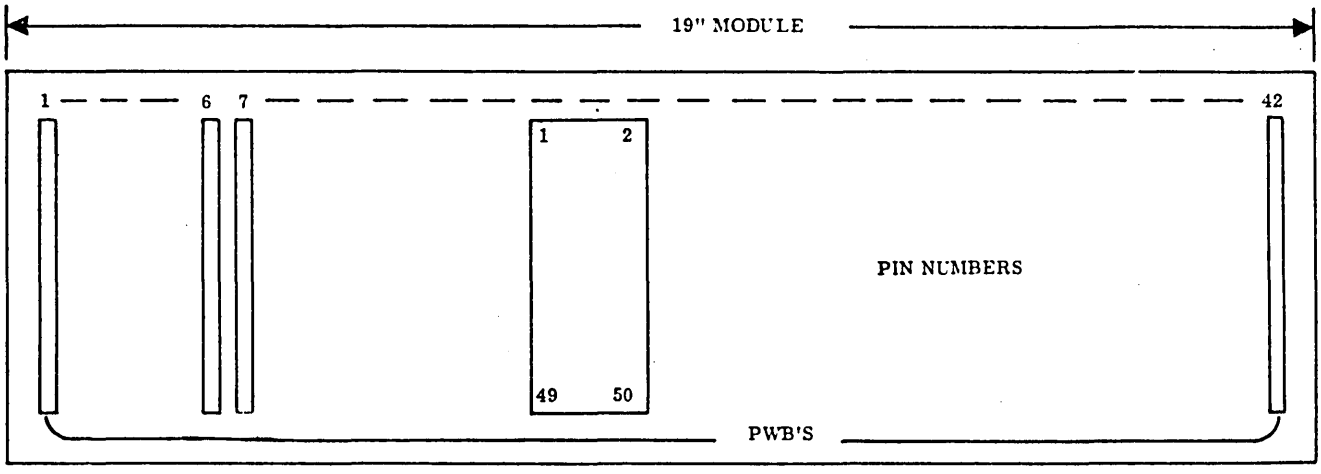
- Card extractor (Flotron 6121-174A, CDC Part No. 38862900).
- Card extender, 6-inch (CQ Card No. 38837100).
- Small adjustable hand mirror (General 555 or equivalent) for reading helium gas bottle pressure from rear of cabinet.
- Refer to drum memory unit manual (see Table 1.4) for additional information.

7.1.3 DIAGRAMS

- Card and chip locations (Figure 7.1).
- Intebrid IC pin configuration (Figure 7.2).
- TTL IC pin configuration (Figure 7.3).
- TTL IC logic diagrams (Figures 7.4 through 7.9).
- Refer to drum memory unit manual (see Table 1.4) for additional information.



PRINTED WIRING BOARD (PWB) COMPONENT SIDE CHIP LOCATIONS



MODULE CONFIGURATION

Figure 7.1. Card and Chip Locations

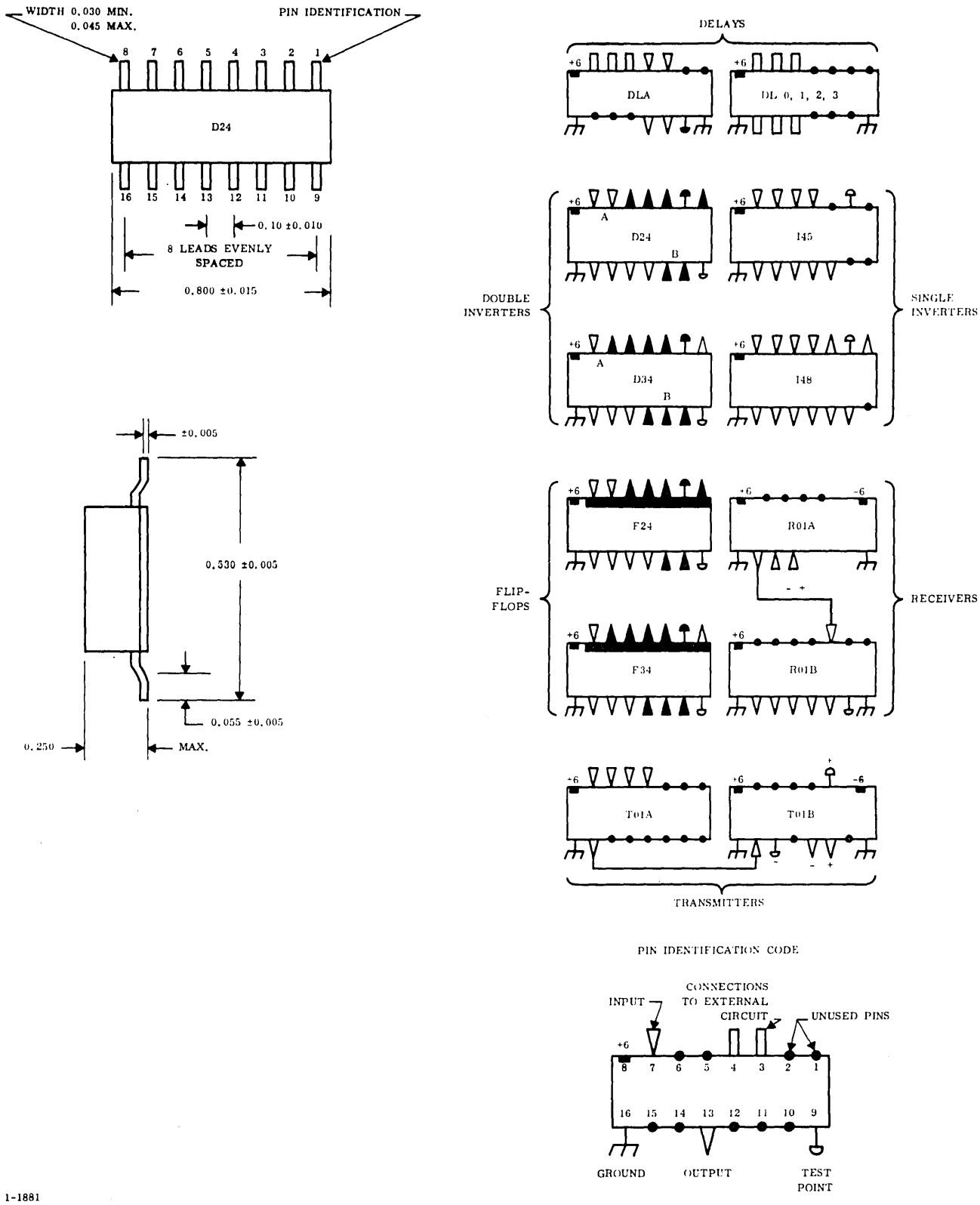


Figure 7.2. Intebrid Circuit Pin Assignments and Dimensions

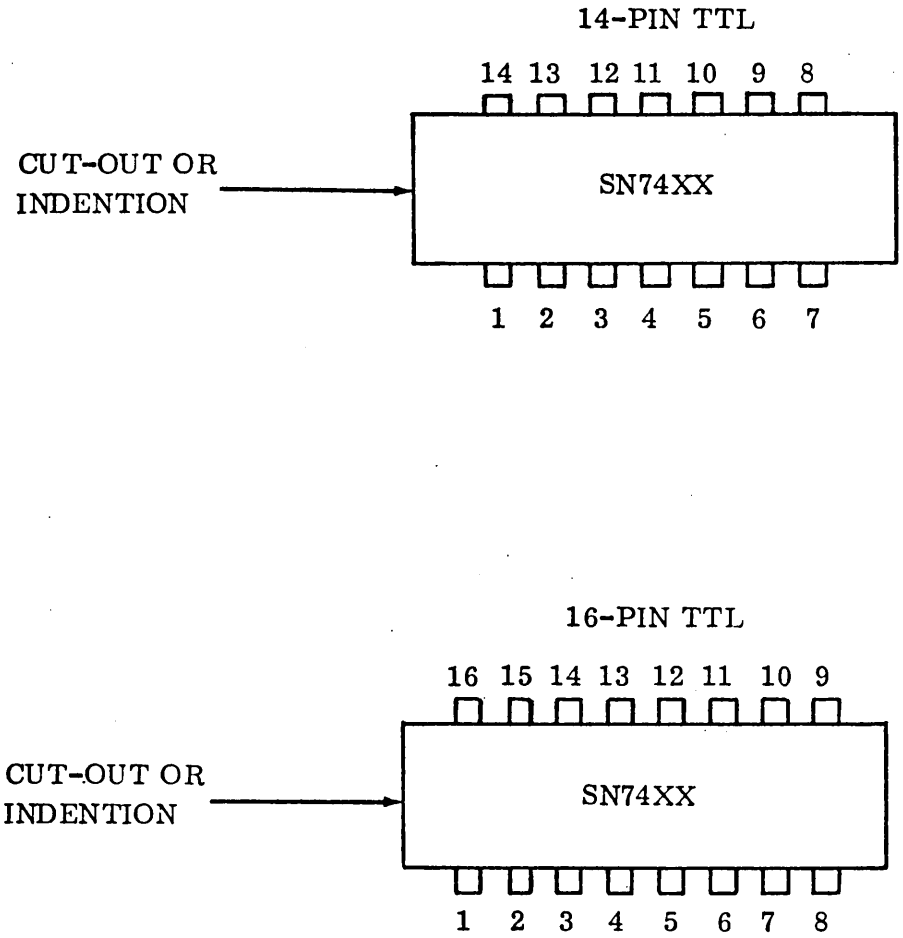
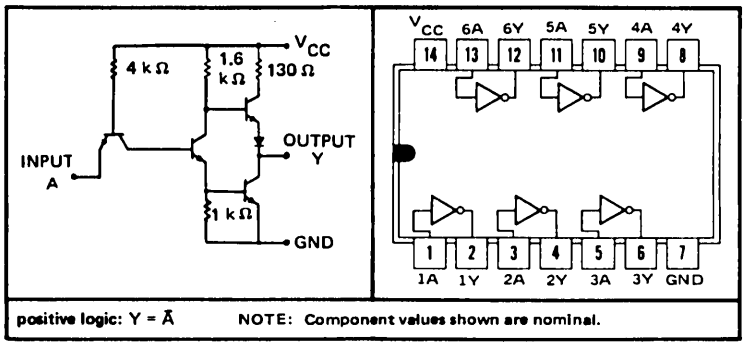
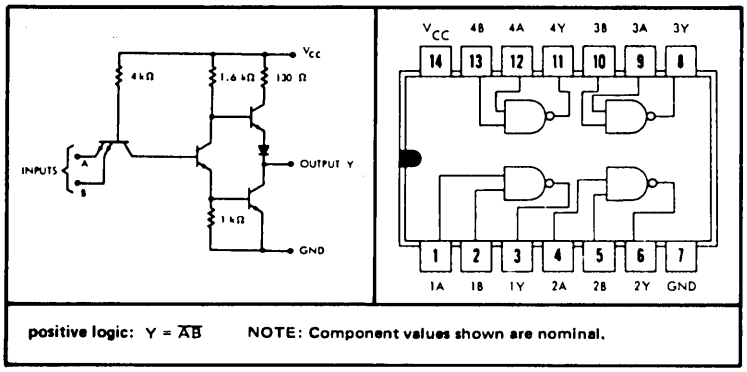


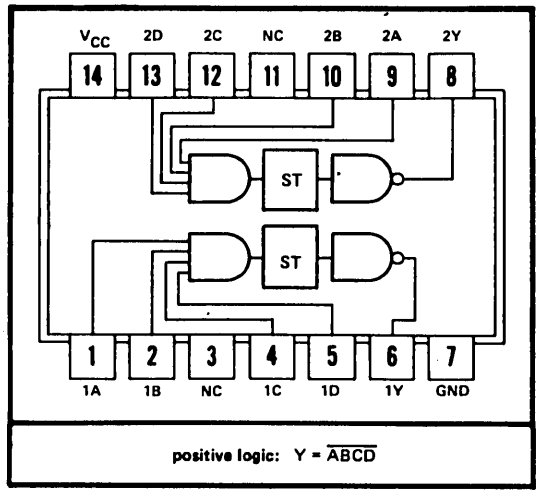
Figure 7.3. TTL IC Pin Configuration, Top View



SN7400
QUADRUPLE 2-INPUT
POSITIVE NAND GATE

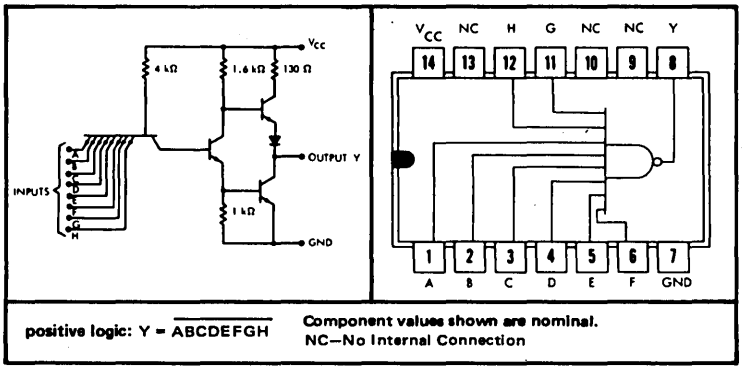


SN7404
HEX INVERTER

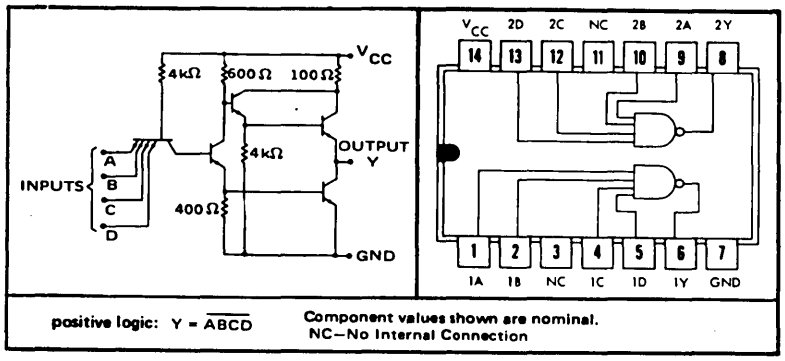


SN7413
DUAL NAND SCHMITT TRIGGER

Figure 7.4. IC Logic Diagram

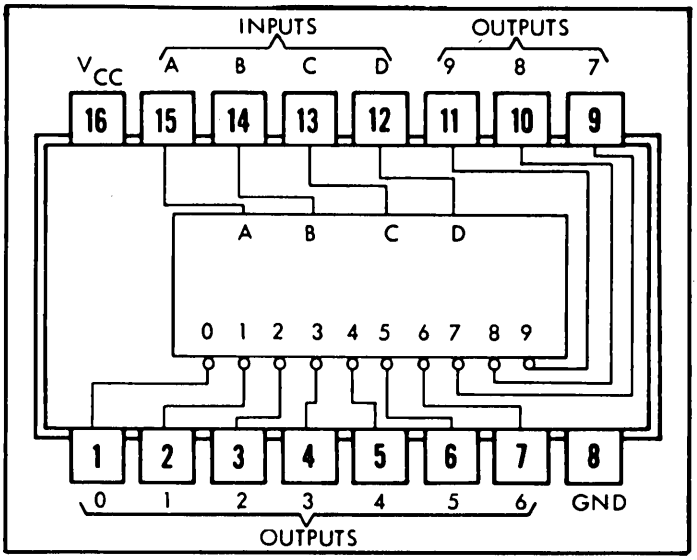


SN7430
8-INPUT POSITIVE
NAND GATE

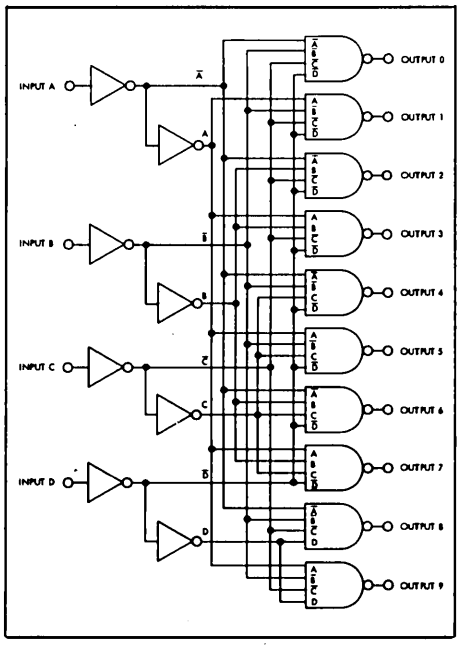


SN7440
DUAL 4-INPUT POSITIVE
NAND BUFFER

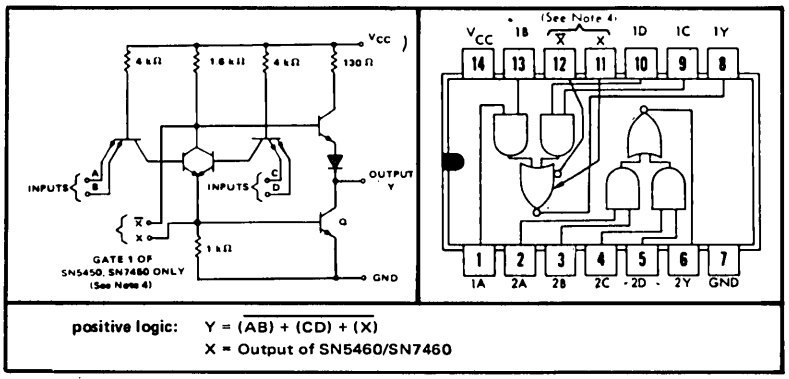
Figure 7.5. IC Logic Diagram



SN7442
4-LINE-TO-10-LINE DECODER
(1-OF-10)



SN7442
4-LINE-TO-10-LINE DECODER
(1-OF-10)

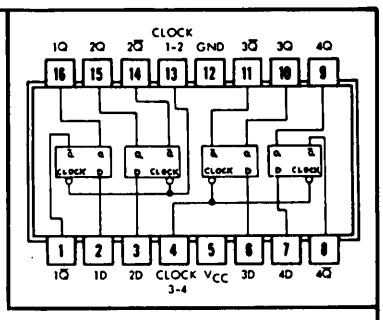


SN7450
EXPANDABLE DUAL 2-WIDE
2-INPUT AND-OR-INVERT
GATE

Figure 7.6. IC Logic Diagram

TRUTH TABLE (Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

NOTES: 1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

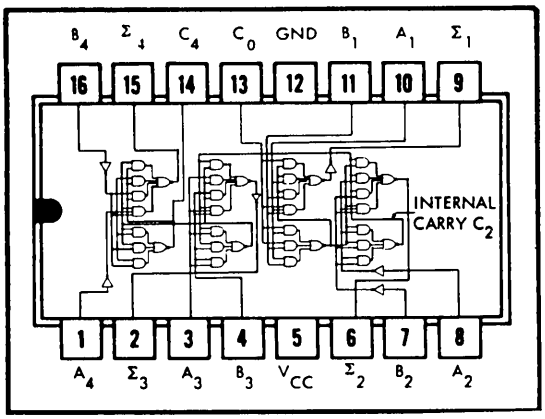


NC—No internal connection

SN7475
4-BIT BISTABLE LATCH

INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
				WHEN $C_2 = 0$			WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

NOTE 1: Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

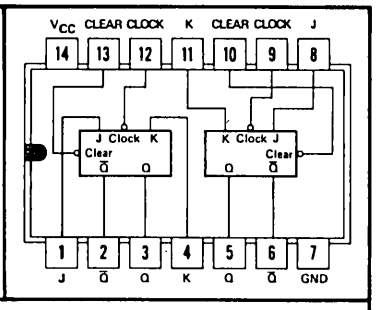


SN7483
4-BIT BINARY FULL ADDER

Figure 7.7. IC Logic Diagram

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

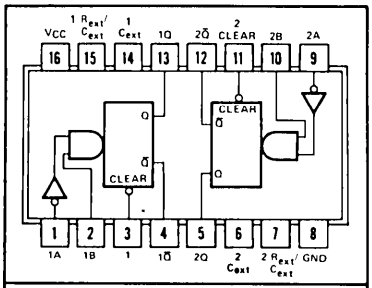
NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.



positive logic:
Low input to clear sets Q to logical 0.
Clear is independent of clock.

SN74107
DUAL J-K MASTER-SLAVE
FLIP-FLOP

INPUTS		OUTPUTS	
A	B	Q	$\bar{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎎
↓	H	⎍	⎎

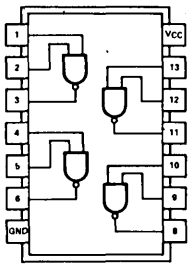


positive logic:
Low input to clear resets Q to low level and inhibits data inputs

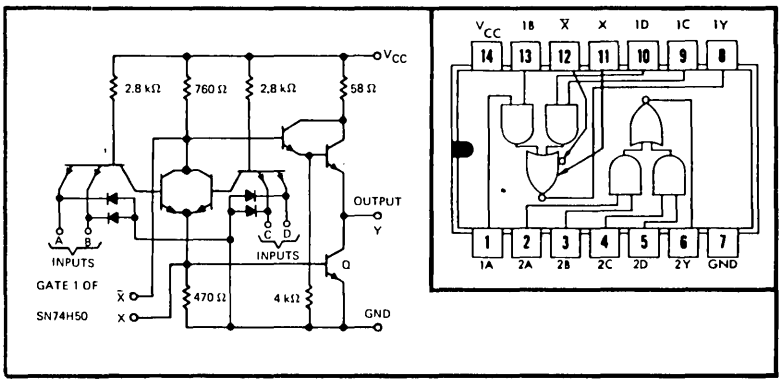
NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions).
B. NC = No internal connection.
C. To use the internal timing resistor of SN54122/SN74122 (10 kΩ nominal), connect R_{int} to V_{CC}.
D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

SN74123
RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

Figure 7.8. IC Logic Diagram



849
QUAD 2-INPUT NAND GATE



SN74H50
DUAL 2-WIDE 2-INPUT
AND-OR-INVERT GATE

Figure 7.9. IC Logic Diagram

7.1.4 PRINTED CIRCUIT BOARD REPAIR

The maintenance and repair of 30-pak assemblies includes removing and replacing integrated circuits, cutting copper foil conductors to facilitate wiring changes, and adding discrete wires and components.

Usually, failure analysis is effective only when the defective circuits are received in an as-failed condition. Therefore, the following general precautions are given to minimize further damage to either the printed circuit board or any component (integrated circuit or discrete component) on the board:

- Refrain from multiple bending of component leads. A lead may break off after being bent only a few times.
- To avoid damage to the substrate of an integrated circuit chip, do not twist its leads.
- Heat application from a soldering iron must not exceed five seconds. Excessive heat damages and shortens the life of components and loosens the copper foil from the printed circuit boards.

7.1.4.1 Removal of Integrated Circuit Chips

The following paragraphs contain two separate and distinct methods for removal of integrated circuit chips. They are given in the order of preference.

Destructive Removal Procedure

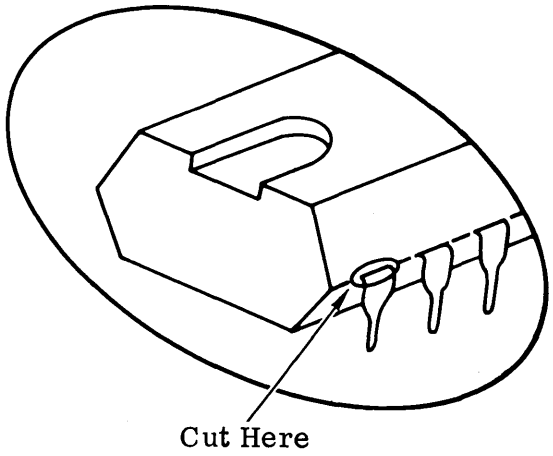
To complete the removal procedure described in this paragraph, the following tools are needed:

- One miniature diagonal cutters
- One miniature soldering iron with pencil tip (25-watt)

- One miniature long-nosed pliers
- One solder sucker

Perform the following steps:

- Using the diagonal cutters, clip leads on one side of the chip being removed at a point as near to the chip as possible as shown in the following illustration:



Cutting IC Chip Leads

- After leads on one side of the chip are cut, either bend the chip back and forth several times to break the leads from the other side, or cut them with the diagonal cutters.
- Mount the printed wiring assembly in a vertical position.
- Using miniature soldering iron with pencil tip, heat one of the severed leads on printed wiring side of the assembly. When solder melts, pull lead out of hole in assembly from component side of assembly, using miniature long-nosed pliers.
- After each lead is removed, re-heat each vacated hole and remove excess solder with a solder sucker.

Desoldering Each Lead Procedure

To remove an integrated circuit chip, the following tools are needed:

- One miniature soldering iron with pencil tip (25-watt)
- One solder sucker
- One length of copper wick

Perform the following steps:

- Mount the printed wiring assembly in a vertical position.
- Using the pencil-tipped soldering iron heated to maximum temperature, heat one lead of the chip on the component side of the assembly.
- When the solder melts, remove it with a solder sucker.
- Repeat preceding step for all leads of the chip to be removed.
- After majority of solder has been removed by the solder sucker, reapply heat and use a copper wick to remove small amounts of remaining solder from each lead.
- Repeat any of the preceding steps, as required, until all leads of the chip are free and the chip may be removed.

7.1.4.2 Replacement of Integrated Circuit Chips

Perform the following steps:

- Before mounting replacement chip on assembly, inspect holes where the chip leads will be inserted to be sure that no residue solder is in the holes.

- Position replacement chip over holes so that either the small recessed area or the notch is to the left. Do not use the lettering on the chip as an indicator of a correctly-positioned chip.
- Gently push chip down until all leads pass through holes in the board. If too much resistance is felt as chip is inserted, recheck holes for residue solder and remove if necessary. When chip feels firmly seated on board, turn board over and check that all pins of chip came through proper holes.
- Solder each lead on printed wiring side of board. When soldering is complete, inspect holes on component side of board where chip leads went through the board to ensure that solder filled holes around leads.
- Clean and inspect all soldering. Trichlorethylene is preferred as a cleaning agent.

7.1.4.3 Cutting Copper Foil Conductors

Perform the following steps:

- Using an Exacto knife, cut copper foil in two places, approximately 1/32 inch apart.
- Peel off the small copper strip between the two knife cuts. It is not necessary to remove entire copper strip.

7.1.4.4 Adding Discrete Wires

Perform the following steps:

- On printed wiring side of the board, measure desired length of 30 AWG wire to be used and add 3 or 4 inches of wire to that measured.
- Strip 1 1/2 to 2 inches of insulation from one end of the 30 AWG wire and make a small loop of the bare wire close to the insulation.

- Place loop of wire over pin of the chip and pull loop snug against solder around the pin. Then hold hot pencil-tipped soldering iron against pin and wire loop until solder melts and covers wire loop. Add more solder, if necessary.
- Holding free end of the 30 AWG wire taut, measure distance to the pin to which the free end will be soldered. Strip wire at that point, pull it tight, and wrap wire around the pin.
- Hold hot soldering iron against the wire and pin until solder melts and flows around the wire and pin. Trim any excess wire from both pins and clean solder joints, if necessary, using trichlorethylene.

7.1.5 DIAGNOSTIC DESCRIPTION

See Appendix B.

Section Eight

PARTS DATA

8.1 PARTS DATA

Parts data is provided in this section by copies of the following released CDC drawings:

- Figure 8.1 Drum Memory Subsystem Drawing 39744600 (Sheets 1 through 6)
- Figure 8.2 Spare Parts List for Drum Memory Subsystem Drawing SP39744600 (Sheets 1 through 5)
- Figure 8.3 Panel Assembly – Power Supplies PL39738900 (Sheets 1 and 2)

Figure 8.1. Drum Memory Subsystem Parts List

REVISION RECORD						
REV	CO	DESCRIPTION	DRFT	DATE	CHKD	APP
FOR REVISIONS SEE SHEET 6						

1. TABULATION OF ASSEMBLY NO. AND SECTOR OVER-RANGE JUMPER INSTALLATION: (U-JUMPERS TO BE INSTALLED IN DRUM CONTROLLER)

EQUIPMENT NO.	ASSEMBLY NO.	DRUM F/N	NO. OF WORDS	NO. OF TRACKS	SECTOR OVER-RANGE JUMPER CARD POSITION A16 U-JUMPER (FN25) BETWEEN PINS		
					5-6	7-8	9-10
BG504-A	39744600	15	196,608	64			
B	01	16	393,216	128			1
C	02	17	589,824	192		1	
D	03	18	786,432	256		1	1
E	04	19	983,040	320	1		
F	05	20	1,179,648	384	1		1
G	06	21	1,376,256	448	1	1	
BG504-H	39744607	22	1,572,864	512	1	1	1

2. FOR CABLING AND WIRING INFORMATION SEE DWG 39745500.

SP 39744600 | EC 39744600 | DETACHED LIST

DWN	Bob Livingston	6-24-71
CHKD	G. Fage *	7-8-71
ENG	E Brown	7-7-71
MFG		
APP	E. Krause	7-9-71

CONTROL DATA

LA JOLLA SYSTEMS DIVISION La Jolla, Calif. 92037

TITLE: DRUM MEMORY SUBSYSTEM

BG504 | CODE IDENT 09132 | A | DWG NO 39744600

SCALE | SHEET 1 OF 6

NOTES: CON'T

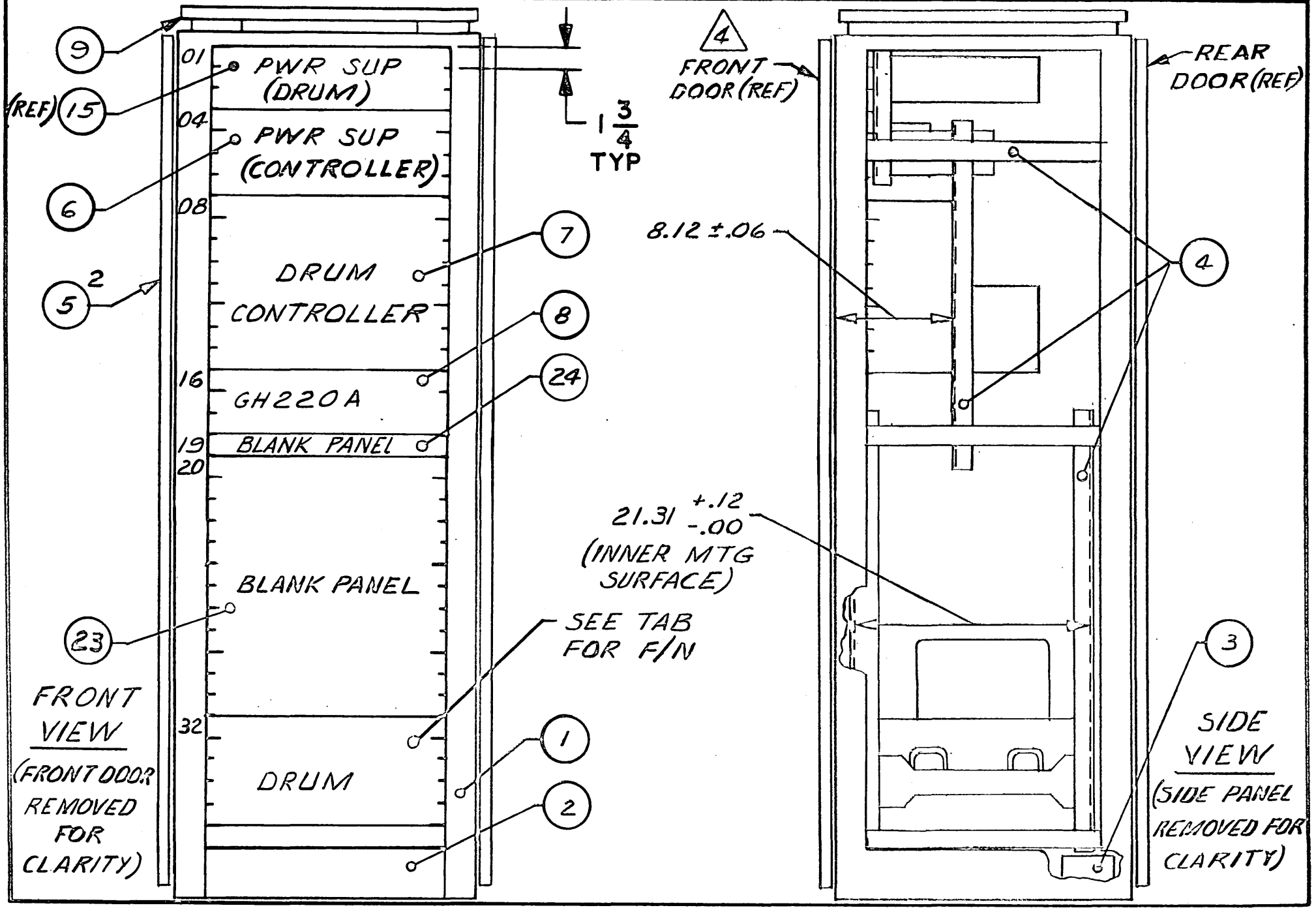
3. SPARE U-JUMPERS (FN 25) TO BE INSTALLED IN DRUM CONTROLLER CARD POSITION A16, AS FOLLOWS:

BETWEEN PINS			
11-12	15-16	19-20	23-24
13-14	17-18	21-22	25-26

THESE U-JUMPERS MAY BE USED IN "GUARDED ADDRESS JUMPER CONFIGURATION" AS DETERMINED BY PROGRAM REQUIREMENTS.

4. IDENTIFY (FN 14) WITH PART NO. & EQUIP NO., LOCATE INSIDE FRONT DOOR.

CONTROL DATA CORPORAT	LA JOLLA SYSTEMS DIVISION La Jolla, Calif. 92037	CODE IDENT 09132	SHEET 3		DOCUMENT NO. 39744600	REV. C



CONTROL DATA CORPORATION	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	CODE IDENT 09132	SHEET 4	PL	DOCUMENT NO 39744600	REV. E

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED 00	01	02	03	04	05	06	07			UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	39291400	1	1	1	1	1	1	1	1					STANDARD 19" RACK	
2	39005000	1	1	1	1	1	1	1	1					FILLER MEMBER	
3	39739400	1	1	1	1	1	1	1	1					PWR DIST BOX	A6
4	39049100	1	1	1	1	1	1	1	1					RACK MOD KIT	
5	39203400	2	2	2	2	2	2	2	2					SIDE PANEL	
6	39738900	1	1	1	1	1	1	1	1					PANEL W/PWR SUP	A2
7	39740900	1	1	1	1	1	1	1	1					DRUM CONTROLLER	A3
8	39514900	1	1	1	1	1	1	1	1					BLOWER (GH22OA)	A4
9	39271000	1	1	1	1	1	1	1	1					COVER, TOP-LOUVERED	LT GRAY
10	39745500	REF	REF	REF	REF	REF	REF	REF	REF					PWR WIRING DIAGRAM	
11	39738102	1	1	1	1	1	1	1	1					CABLE ASSY- 50 PIN TO 50 PIN	
12	38927904	1	1	1	1	1	1	1	1					CABLE ASSY- 2 PIN TO PIGTAILS	
13	39745003	1	1	1	1	1	1	1	1					CABLE ASSY- 3 TERM TO PIGTAILS	
14	38933500	1	1	1	1	1	1	1	1					IDENT PLATE	
15	39668602	1												PWR SUP (DRUM)	A1
														DRUM-196,608 WORDS	A5
16	39668603		1											PWR SUP (DRUM)	A1
														DRUM-393,216 WORDS	A5
17	39668604			1										PWR SUP (DRUM)	A1
														DRUM-589,824 WORDS	A5

CONTROL DATA CORPORATION	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	CODE IDENT 09132	SHEET 5	PL	DOCUMENT NO 39744600	REV. A

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED 00	01	02	03	04	05	06	07			UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
18	39668605				1									PWR SUP (DRUM)	A1
														DRUM- 786,432 WORDS	A5
19	39668606					1								PWR SUP (DRUM)	A1
														DRUM 983,040 WORDS	A5
20	39668607						1							PWR SUP (DRUM)	A1
														DRUM-1,179,648 WORDS	A5
21	39668608							1						PWR SUP (DRUM)	A1
														DRUM 1,376,256 WORDS	A5
22	39668609								1					PWR SUP (DRUM)	A1
														DRUM-1,572,864 WORDS	A5
23	38968723	1	1	1	1	1	1	1	1					BLANK PANEL	
24	38968712	1	1	1	1	1	1	1	1					BLANK PANEL	
25	39025100	8	9	9	10	9	10	10	11					U-JUMPER	

DWN			CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD			ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	DRUM MEMORY SUBSYSTEM		39744600	E
ENG							
MFG							
APPR			CODE IDENT 09132	FIRST USED ON		SHEET 6	

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A		RELEASED	BL	7-9-71	E. L.
B	DDC	ADDED SPARE PARTS LIST ECR 4569	BL	10-27-71	E. L.
C	DDC	ADDED FN 9 ECR 4569	BL	12-16-71	E. L.
D	DDC	SEE SPARE PARTS LIST ECR 4569	T.H.	6-16-72	E. L.
E	DDC	FN 12 WAS 38927902, ECR 3146	T.H.	7-25-72	E. L.

NOTES:

DETACHED LISTS

Figure 8.2. Spare Parts List for Drum Memory Subsystem

DWN	[illegible]	10-27-71	CONTROL DATA
CHKD	R. Gilbert	10-27-71	
ENG			ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037
MFG			
APPR	E. [illegible]	10-27-71	CODE IDENT 09132

TITLE

SPARE PARTS LIST FOR
DRUM MEMORY SUBSYSTEM

PREFIX	DOCUMENT NO.	REV
SP	39744600	E

FIRST USED ON

BG504A-H

SHEET 1 of 5

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
B	DDC	RELEASED	BG	10-27-71	E. [illegible]
D	DDC	FN 8 & 22 WAS 39702900 & 24536100 ECR 4648 BM	JN.	6-16-72	E. [illegible]

NOTES:

DETACHED LISTS

AA3180

PRINTED IN U.S.A.

CONTROL DATA CORPORATION	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	CODE IDENT 09132	SHEET 2	PL	DOCUMENT NO SP39744600	REV. D

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED										UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
		00	01	02	03	04	05	06	07						
1	39233400	1	1	1	1	1	1	1	1					PWA TTL Incre Reg 8 Bit	9GET
2	39233700	1	1	1	1	1	1	1	1					TTL Counter/Reg 8 Bit	9GFT
3	39234300	1	1	1	1	1	1	1	1					TTL Compare 8 EOR	9GHT
4	39234600	1	1	1	1	1	1	1	1					TTL Gate High Fan In	9GJT
5	39234900	1	1	1	1	1	1	1	1					TTL Gate Low Fan In	9GKT
6	39235200	1	1	1	1	1	1	1	1					JK Flip Flop 5	9GLT
7	39377400	1	1	1	1	1	1	1	1					TTL NAND 2 Input	9DDT
8	39709200	1	1	1	1	1	1	1	1					3/4/4 Gated Xceiver	1LKT
9	39705100	1	1	1	1	1	1	1	1					Track Timing No. 1	1LAT
10	39705400	1	1	1	1	1	1	1	1					Check Word Gen	1LBT
11	39705700	1	1	1	1	1	1	1	1					Data Register	1LCT
12	39706000	1	1	1	1	1	1	1	1					Drum Read/DSA Control	1LDT
13	39706300	1	1	1	1	1	1	1	1					Track Timing No. 2	1LET
14	39706600	1	1	1	1	1	1	1	1					Drum Write Control	1LFT
15	39708300	1	1	1	1	1	1	1	1					Controller Clock	1LGT
16	39708600	1	1	1	1	1	1	1	1					Equip Select	1LHT
17	39708900	1	1	1	1	1	1	1	1					Memory Scanner TTL	1LJT
18	39709500	1	1	1	1	1	1	1	1					Gen Pur Xmitter	1LLT
19	39709800	1	1	1	1	1	1	1	1					Gen Pur Receiver	1LMT
20	39715300	1	1	1	1	1	1	1	1					PWA Guarder Addr/or Detect	1MBT

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED 00	01	02	03	04	05	06	07			UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
21	39283405	1	1	1	1	1	1	1	1					Circuit Breaker 5 Amp	
22	24536500	1	1	1	1	1	1	1	1					Fan, Axial	
23	11824400	5	5	5	5	5	5	5	5					IC Party Line Xmitter T01A	
24	11824500	5	5	5	5	5	5	5	5					Party Line Xmitter T31B	
25	11826500	1	1	1	1	1	1	1	1					Flip Flop F34	
26	11826900	5	5	5	5	5	5	5	5					Party Line Receiver R01A	
27	11827000	5	5	5	5	5	5	5	5					Party Line Receiver R01B	
28	11848500	3	3	3	3	3	3	3	3					Inverter I48M	
29	38385300	1	1	1	1	1	1	1	1					844	
30	39385500	1	1	1	1	1	1	1	1					849	
31	39385800	1	1	1	1	1	1	1	1					7442	
32	39388300	7	7	7	7	7	7	7	7					7400	
33	39388400	4	4	4	4	4	4	4	4					7430	
34	39388500	9	9	9	9	9	9	9	9					7450	
35	39388600	7	7	7	7	7	7	7	7					7472	
36	39388700	1	1	1	1	1	1	1	1					7475	
37	39388800	1	1	1	1	1	1	1	1					7483	
38	39389200	2	2	2	2	2	2	2	2					7440	
39	39389300	1	1	1	1	1	1	1	1					7493	
40	39389700	1	1	1	1	1	1	1	1					IC 7404	

CONTROL DATA CORPORATION	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	CODE IDENT 09132	SHEET 4	PL	DOCUMENT NO SP39744600	REV. B

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED										UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
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41	39389800	1	1	1	1	1	1	1	1					IC 74123	
42	39389900	1	1	1	1	1	1	1	1					7413	
43	39390000	2	2	2	2	2	2	2	2					74107	
44	52301300	1	1	1	1	1	1	1	1					Double Inverter D34M	
45	52301400	1	1	1	1	1	1	1	1					IC Flip Flop F34M	
46	25175800	20	20	20	20	20	20	20	20					Diode	
47	24562100	1	1	1	1	1	1	1	1					Transistor	
48	39054700	1	1	1	1	1	1	1	1					Transistor 2N4250	
49	39547000	1	1	1	1	1	1	1	1					Transistor 2N5210	
50	12211703	1	1	1	1	1	1	1	1					Helium	DDC 13465
51	12248466	1	1	1	1	1	1	1	1					PWA Phase Lock Loop	DDC 21295
52	12248467	1	1	1	1	1	1	1	1					PWA Peak Detector	DDC 21245
53	12248468	1	1	1	1	1	1	1	1					PWA Filter Terminator	DDC 21301
54	12248469	1	1	1	1	1	1	1	1					PWA Filter Term. & Reg.	DDC 21302
55	12248470	1	1	1	1	1	1	1	1					PWA Line Terminator	DDC 21300
56	12248471	1	1	1	1	1	1	1	1					PWA Filter	DDC 21305
57	12220182	1	1	1	1	1	1	1	1					I.C. Decoder N8250A	
58	50254600	1	1	1	1	1	1	1	1					I.C. Gate 74S00	
59	12220183	1	1	1	1	1	1	1	1					I.C. Flip-Flop 74S112	
60	94918801	2	2	2	2	2	2	2	2					I.C. Gate 74H00	

CONTROL DATA CORPORATION	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	CODE IDENT 09132	SHEET 5	PL	DOCUMENT NO SP39744600	REV. B

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED										UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
		00	01	02	03	04	05	06	07						
61	15104600	1	1	1	1	1	1	1	1					I.C. Gate 74H10	
62	94918800	2	2	2	2	2	2	2	2					I.C. Inverter 74H04	
63	52343700	1	1	1	1	1	1	1	1					I.C. Gate 74H51	
64	52335900	2	2	2	2	2	2	2	2					I.C. Flip-Flop 74H74	
65	94918809	1	1	1	1	1	1	1	1					I.C. Gate 7400	
66	94918810	1	1	1	1	1	1	1	1					I.C. Gate 7402	
67	17183800	1	1	1	1	1	1	1	1					I.C. Buffer Driver 7416	
68	17183900	1	1	1	1	1	1	1	1					I.C. Buffer Driver 7417	
69	94918813	1	1	1	1	1	1	1	1					I.C. Gate 7420	
70	94918817	2	2	2	2	2	2	2	2					I.C. Buffer Driver 7440	
71	94916109	3	3	3	3	3	3	3	3					I.C. Flip-Flop 7474	
72	50252900	1	1	1	1	1	1	1	1					I.C. Line Receiver 75107	
73	12220184	1	1	1	1	1	1	1	1					I.C. Pullups S161	
74	12231108	1	1	1	1	1	1	1	1					Power Supply Sorenson	QSA28-2.0
75	12231126	1	1	1	1	1	1	1	1					Power Supply Sorenson	QSA12-2.1
76	12231127	1	1	1	1	1	1	1	1					Power Supply Sorenson	QSA5-6.4

Figure 8.3. Panel Assembly - Power Supplies, Parts List

DWN	T. Gyman	6-8-71
CHKD	R. Gilbert	7-1-71
ENG	[signature]	7-2-71
MFG	[signature]	
APPR	E. Krumm	7-9-71

CONTROL DATA

ANALOG - DIGITAL SYSTEMS DIVISION
La Jolla, Calif. 92037

CODE IDENT 09132

TITLE: PANEL ASSEMBY- POWER SUPPLIES

PREFIX	DOCUMENT NO.	REV
PL	39738900	B

FIRST USED ON: BG504

SHEET 1 OF 2

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP'D
A		RELEASED	TC	7-9-71	E.K.
B		F/N 3 WAS PS01, F/N 7 WAS PS03 (ECR 3110) RS	RS	10-27-71	E.K.

NOTES:

DETACHED LISTS

CONTROL DATA	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	CODE IDENT 09132	SHEET 2	PL	DOCUMENT NO 39738900	REV B

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS	NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1	39738200	1		PANEL	
2	39698500	1		GD117-A PWR SPLY 5V 6.5A	PS02
3	39698501	1		GD117-B PWR SPLY, 6V 3.4A	PS03
4	38933500	1		PLATE, IDENT	
5	84820002	12		SCREW, TAPPING, PHIL, PAN HD, 8-B x .50 LG	
6	93464444	1		WIRE, ELECT., STRD, TIN. (YELLOW) 16 AWG	
7	39698502	1		GD117-C PWR SPLY, 6V, 6.2A	PS01
8					
9	25198804	12		TERMINAL-RING TONGUE, INSUL.	

Section Nine

WIRE LIST

9.1 WIRE LIST

39740700 D DRUM CONTROLLER

ALARM	A34-020	B12-008	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
ALARM	B12-008	B36-001	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
ALSF	A26-011	B36-035	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
ARJT	A35-040	B20-041	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
ARPIY	A35-039	B20-042	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A0	A30-034	B11-012	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A0F	A09-021	A30-031	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A1	A30-013	B11-020	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A10	A24-048	B13-040	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A11	A24-045	B13-048	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A12	A24-004	B14-012	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A13	A24-001	B14-020	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A14	A17-045	B14-040	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A15	A22-045	B14-048	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A2	A21-048	B11-040	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A3	A21-045	B11-048	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A4	A19-047	B12-012	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING

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A5	A15-042	B12-020	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A6	A15-043	B12-040	
A7	A19-045	B12-048	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A8	A24-044	B13-012	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
A9	A24-043	B13-020	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
BZ	A36-030	B36-004	
BZ	B11-008	B36-004	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
BZF	A09-028	A29-007	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA0	A20-045	B20-034	
CA0	B11-003	B20-034	
CA1	A20-046	B20-033	
CA1	B11-004	B20-033	
CA10	A23-036	B21-022	
CA10	B13-031	B21-022	
CA11	A23-033	B13-030	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA11	B13-030	B21-021	
CA12	A23-021	B14-003	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA12	B14-003	B21-014	
CA13	A23-020	B14-004	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA13	B14-004	B21-013	
CA14	A23-010	B14-031	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA14	B14-031	B21-004	
CA15	A23-009	B14-030	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA15	B14-030	B21-003	

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CA2	A20-036	B11-031	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA2	B11-031	B20-022	
CA3	A20-033	B11-030	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA3	B11-030	B20-021	
CA4	A20-021	B12-003	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA4	B12-003	B20-014	
CA5	A20-020	B12-004	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA5	B12-004	B20-013	
CA6	A20-010	B12-031	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA6	B12-031	B20-004	
CA7	A20-009	B12-030	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA7	B12-030	B20-003	
CA8	A23-045	B13-003	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA8	B13-003	B21-034	
CA9	A23-046	B13-004	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CA9	B13-004	B21-033	
CLKF+	A32-004	A34-033	
CS1F	A28-046	B11-026	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CS2F	A28-047	B13-026	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
CWE	A11-012	B13-006	
CWE	A11-012	A34-005	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DAS1F	A28-038	B11-025	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DAS2F	A28-041	B13-025	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING

DATA	A26-008	B11-036	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DFE	A09-023	A30-045	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DR	A28-008	B11-006	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DR	B11-006	B36-003	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DRF*	A26-013	A28-005	
DSAPB	A33-033	B26-045	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DSAPP	A29-001	B21-041	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DS1F	A28-027	B12-022	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DS2F	A28-032	B13-022	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DW	A11-021	A22-018	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
DW	A22-018	A28-018	
DW	A28-018	A33-011	
EGAE	A18-027	A33-022	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
EGAS	A18-003	A28-013	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
EGAS	A18-003	B13-032	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
EGAS	B13-032	B36-036	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
EOP	A32-030	B12-006	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
GAE	A18-024	B14-032	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
GAP	A18-013	A14-035	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
GA0	A14-033	A30-046	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
GA2	A14-032	A30-017	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING

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GA3	A14-024	A30-032	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
GRD	B14-050	PS-+TER	16 GA. WIRE
GRD	X02- C	TB1-030	22 GA. STRANDED WIRE
HALT	A11-044	B02-036	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
INT	A33-024	B11-032	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
INT+	TB1-043	TB1-044	TB1-045
INT-	TB1-046	TB1-047	TB1-048
LD	A35-006	B12-032	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
LDRF	A11-038	A34-028	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
LDWF	A12-023	A34-023	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
MCLF	A29-014	B36-027	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
OM+	A12-022	A14-013	A15-013 A26-035
ORD	A11-047	A33-036	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
PCLR	A26-015	B36-026	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
PF	A26-016	B14-006	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
PRIOR	A11-046	B02-011	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
PRIOR	B02-033	B21-042	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
PROF	A36-046	B13-008	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING

PROTS	B12-036	B36-037	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
PWRB	X12- X	PWR-CRD	BLACK
PWRB	X12- X	T1-001	BLACK 16 GA. WIRE
PWRG	X12-GRD	E1	GREEN 16 GA. WIRE
PWRG	X12-GRD	PWR-CRD	GREEN
PWRW	X12- W	PWR-CRD	WHITE
PWRW	X12- W	T1-002	WHITE 16 GA. WIRE
Q0	A09-027	A26-020	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
Q0	A26-020	B26-023	
RCS3F	A11-027	A32-045	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
RFDF	A09-046	A29-024	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
RPLY	A11-039	A32-005	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
RPLY	A11-039	B02-032	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
RQST	A11-045	B02-012	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
RQSTF	B02-020	B20-039	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
RUNF	A11-024	A12-019	
RUNF	A12-019	A31-019	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R00	A06-005	B11-028	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R01	A06-006	B11-001	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R010	A07-011	B13-034	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R011	A07-027	B13-027	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING

R012	A07-038	B14-028	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R013	A07-041	B14-001	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R014	A07-042	B14-034	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R015	A12-005	B14-027	
R02	A06-011	B11-034	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R03	A06-027	B11-027	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R04	A06-038	B12-028	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R05	A06-041	B12-001	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R06	A06-042	B12-034	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R07	A06-043	B12-027	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R08	A07-005	B13-028	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
R09	A07-006	B13-001	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
SC0	A14-021	B11-005	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
SC1	A14-029	B11-019	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
SC2	A14-028	B11-029	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
SC3	A14-027	B11-033	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
SS1F	A28-017	B11-024	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING

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SS2F	A28-022	B13-024	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA0	A18-035	B12-019	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA1	A18-040	B12-029	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA2	A18-038	B12-033	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA3	A18-037	B13-005	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA4	A18-031	B13-019	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA5	A18-039	B13-029	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA6	A17-033	B13-033	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA7	A17-030	B14-005	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA8	A17-036	B14-019	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA8F	A17-037	A33-020	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA8F	A33-019	A33-020	
TA9	A17-029	B14-029	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TA9F	A15-047	A17-031	
TA9F	A17-031	A33-017	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING
TE	A34-007	B13-036	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING

V+20	TB1-001	TB1-002	TB1-003	TB1-004	TB1-005	TB1-006
V+20	TB1-006	TB1-007	TB1-008	TB1-009	TB1-020	TB1-033

V+5	PS-+	BUS-BAR + TER. A MODULE	16 GA. WIRE
V+5	PS--	BUS-BAR - TER. A MODULE	16 GA. WIRE

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V+6	PS-+	BUS-BAR + TER. B MODULE	16 GA. WIRE			
V+6	PS--	BUS-BAR - TER. B MODULE	16 GA. WIRE			
V-20	TB1-015	TB1-016	TB1-017	TB1-018	TB1-019	TB1-040
V-20	TB1-040	TB1-038				
V-20	TB1-041	TB1-011	TB1-012	TB1-013	TB1-014	TB1-015
V-6	B14-047	PS--TER	16 GA. WIRE			
VCTT	B02-050	TB1-029				
VCTT	TB1-010	TB1-050	TB1-037	TB1-034		
VCTT	TB1-021	TB1-022	TB1-023	TB1-024	TB1-025	TB1-026
VCTT	TB1-026	TB1-027	TB1-028	TB1-029	TB1-030	TB1-010
VCTT	X04-CTR	TB1-021				
VCTT	X05-CTR	TB1-022				
VCTT	X06-CTR	TB1-023				
VCTT	X07-CTR	TB1-024				
VCTT	X08-CTR	TB1-025				
VCTT	X09-CTR	TB1-026				
VCTT	X10-CTR	TB1-027				
VCTT	X11-CTR	TB1-028				
WENF1	A19-011	B06-026	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING			
WENF2	A19-014	B08-026	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING			
WODF	A09-032	A29-019	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING			
WP	A09-030	A26-040	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING			
WREN	A11-042	B02-003	WIRE AGAINST BACKPLANE WITH MIN. BUNDLING			
WRITE	A26-024	B26-031				
$AB0+	X08- A1	B20-036	X08- A2	B20-035	$AB0-	
$AB0+	X09- A1	B20-036	X09- A2	B20-035	$AB0-	
$AB1+	X08- A3	B20-038	X08- A4	B20-037	$AB1-	
$AB1+	X09- A3	B20-038	X09- A4	B20-037	$AB1-	

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$AB10+	X08- C1	B21-024	X08- C2	B21-023	$AB10-
$AB10+	X09- C1	B21-024	X09- C2	B21-023	$AB10-
$AB11+	X08- C3	B21-026	X08- C4	B21-025	$AB11-
$AB11+	X09- C3	B21-026	X09- C4	B21-025	$AB11-
$AB12+	X08- C5	B21-015	X08- C6	B21-016	$AB12-
$AB12+	X09- C5	B21-015	X09- C6	B21-016	$AB12-
$AB13+	X08- C7	B21-017	X08- C8	B21-018	$AB13-
$AB13+	X09- C7	B21-017	X09- C8	B21-018	$AB13-
$AB14+	X08- C9	B21-005	X08- C0	B21-006	$AB14-
$AB14+	X09- C9	B21-005	X09- C0	B21-006	$AB14-
$AB15+	X08- F3	B21-007	X08- F4	B21-008	$AB15-
$AB15+	X09- F3	B21-007	X09- F4	B21-008	$AB15-
$AB2+	X08- A5	B20-024	X08- A6	B20-023	$AB2-
$AB2+	X09- A5	B20-024	X09- A6	B20-023	$AB2-
$AB3+	X08- A7	B20-026	X08- A8	B20-025	$AB3-
$AB3+	X09- A7	B20-026	X09- A8	B20-025	$AB3-
$AB4+	X08- A9	B20-015	X08- A0	B20-016	$AB4-
$AB4+	X09- A9	B20-015	X09- A0	B20-016	$AB4-
$AB5+	X08- B1	B20-017	X08- B2	B20-018	$AB5-
$AB5+	X09- B1	B20-017	X09- B2	B20-018	$AB5-
$AB6+	X08- B3	B20-005	X08- B4	B20-006	$AB6-
$AB6+	X09- B3	B20-005	X09- B4	B20-006	$AB6-
$AB7+	X08- B5	B20-007	X08- B6	B20-008	$AB7-
$AB7+	X09- B5	B20-007	X09- B6	B20-008	$AB7-
$AB8+	X08- B7	B21-036	X08- B8	B21-035	$AB8-
$AB8+	X09- B7	B21-036	X09- B8	B21-035	$AB8-

$AB9+	X08- B9	B21-038	X08- B0	B21-037	$AB9-
$AB9+	X09- B9	B21-038	X09- B0	B21-037	$AB9-
$APLY+	X06- D3	B20-046	X06- D4	B20-045	$APLY-
$APLY+	X07- D3	B20-046	X07- D4	B20-045	$APLY-
$APRI+	X06- D9	X07- D9	X06- D0	X07- D0	$APRI-
$AQPP+	X04- D9	B36-045	X04- D0	B36-046	$AQPP-
$AQPP+	X05- D9	B36-045	X05- D0	B36-046	$AQPP-
$ARJT+	X06- D5	B20-044	X06- D6	B20-043	$ARJT-
$ARJT+	X07- D5	B20-044	X07- D6	B20-043	$ARJT-
$AR0+	X06- A1	B11-018	X06- A2	B11-017	$AR0-
$AR0+	X07- A1	B11-018	X07- A2	B11-017	$AR0-
$AR1+	X06- A3	B11-016	X06- A4	B11-015	$AR1-
AR1+	X07- A3	B11-016	X07- A4	B11-015	$AR1-
$AR10+	X06- C1	B13-046	X06- C2	B13-045	$AR10-
$AR10+	X07- C1	B13-046	X07- C2	B13-045	$AR10-
$AR11+	X06- C3	B13-044	X06- C4	B13-043	$AR11-
$AR11+	X07- C3	B13-044	X07- C4	B13-043	$AR11-
$AR12+	X06- C5	B14-018	X06- C6	B14-017	$AR12-
$AR12+	X07- C5	B14-018	X07- C6	B14-017	$AR12-
$AR13+	X06- C7	B14-016	X06- C8	B14-015	$AR13-
$AR13+	X07- C7	B14-016	X07- C8	B14-015	$AR13-
$AR14+	X06- C9	B14-046	X06- C0	B14-045	$AR14-
$AR14+	X07- C9	B14-046	X07- C0	B14-045	$AR14-
$AR15+	X06- D1	B14-044	X06- D2	B14-043	$AR15-
$AR15+	X07- D1	B14-044	X07- D2	B14-043	$AR15-
$AR2+	X06- A5	B11-046	X06- A6	B11-045	$AR2-

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$AR2+	X07- A5	B11-046	X07- A6	B11-045	$AR2-
$AR3+	X06- A7	B11-044	X06- A8	B11-043	$AR3-
$AR3+	X07- A7	B11-044	X07- A8	B11-043	$AR3-
$AR4+	X06- A9	B12-018	X06- A0	B12-017	$AR4-
$AR4+	X07- A9	B12-018	X07- A0	B12-017	$AR4-
$AR5+	X06- B1	B12-016	X06- B2	B12-015	$AR5-
$AR5+	X07- B1	B12-016	X07- B2	B12-015	$AR5-
$AR6+	X06- B3	B12-046	X06- B4	B12-045	$AR6-
$AR6+	X07- B3	B12-046	X07- B4	B12-045	$AR6-
$AR7+	X06- B5	B12-044	X06- B6	B12-043	$AR7-
$AR7+	X07- B5	B12-044	X07- B6	B12-043	$AR7-
$AR8+	X06- B7	B13-018	X06- B8	B13-017	$AR8-
$AR8+	X07- B7	B13-018	X07- B8	B13-017	$AR8-
$AR9+	X06- B9	B13-016	X06- B0	B13-015	$AR9-
$AR9+	X07- B9	B13-016	X07- B0	B13-015	$AR9-
$BC+	X03-001	A26-001	X03-002	A26-002	$BC-
$BUFF+	X04- E1	X05- E1	X04- E2	X05- E2	$BUFF-
$CHIN+	X06- D7	X07- D7	X06- D8	X07- D8	$CHIN-
$CLKF+	A06-021	A07-021	A06-022	A07-022	$CLKF-
$CLKF+	A07-021	A08-039	A07-022	A08-040	$CLKF-
$CLKF+	A08-039	A11-015	A08-040	A11-025	$CLKF-
$CLKF+	A11-015	A12-028	A11-025	A12-026	$CLKF-
$CLKF+	A12-028	A14-047	A12-026	A14-048	$CLKF-
$CLKF+	A14-047	A15-029	A14-048	A15-025	$CLKF-
$CLKF+	A15-029	A17-006	A15-025	A17-002	$CLKF-
$CLKF+	A17-006	A18-007	A17-002	A18-005	$CLKF-
$CLKF+	A18-007	A21-047	A18-005	A21-050	$CLKF-
$CLKF+	A21-047	A24-047	A21-050	A24-050	$CLKF-
$CLKF+	A24-047	A26-005	A24-050	A26-006	$CLKF-
$CLKF+	A26-005	A32-004	A26-006	A32-002	$CLKF-

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$DB0+	X10- A1	B06-018	X10- A2	B06-017	$DB0-
$DB0+	X11- A1	B06-018	X11- A2	B06-017	$DB0-
$DB1+	X10- A3	B06-016	X10- A4	B06-015	$DB1-
$DB1+	X11- A3	B06-016	X11- A4	B06-015	$DB1-
$DB10+	X10- C1	B08-046	X10- C2	B08-045	$DB10-
$DB10+	X11- C1	B08-046	X11- C2	B08-045	$DB10-
$DB11+	X10- C3	B08-044	X10- C4	B08-043	$DB11-
$DB11+	X11- C3	B08-044	X11- C4	B08-043	$DB11-
$DB12+	X10- C5	B09-018	X10- C6	B09-017	$DB12-
$DB12+	X11- C5	B09-018	X11- C6	B09-017	$DB12-
$DB13+	X10- C7	B09-016	X10- C8	B09-015	$DB13-
$DB13+	X11- C7	B09-016	X11- C8	B09-015	$DB13-
$DB14+	X10- C9	B09-046	X10- C0	B09-045	$DB14-
$DB14+	X11- C9	B09-046	X11- C0	B09-045	$DB14-
$DB15+	X10- D1	B09-044	X10- D2	B09-043	$DB15-
$DB15+	X11- D1	B09-044	X11- D2	B09-043	$DB15-
$DB2+	X10- A5	B06-046	X10- A6	B06-045	$DB2-
$DB2+	X11- A5	B06-046	X11- A6	B06-045	$DB2-
$DB3+	X10- A7	B06-044	X10- A8	B06-043	$DB3-
$DB3+	X11- A7	B06-044	X11- A8	B06-043	$DB3-
$DB4+	X10- A9	B07-018	X10- A0	B07-017	$DB4-
$DB4+	X11- A9	B07-018	X11- A0	B07-017	$DB4-
$DB5+	X10- B1	B07-016	X10- B2	B07-015	$DB5-
$DB5+	X11- B1	B07-016	X11- B2	B07-015	$DB5-
DB6+	X10- B3	B07-046	X10- B4	B07-045	$DB6-
$DB6+	X11- B3	B07-046	X11- B4	B07-045	$DB6-

$DB7+	X10- B5	B07-044	X10- B6	B07-043		$DB7-
$DB7+	X11- B5	B07-044	X11- B6	B07-043		$DB7-
$DB8+	X10- B7	B08-018	X10- B8	B08-017		$DB8-
$DB8+	X11- B7	B08-018	X11- B8	B08-017		$DB8-
$DB9+	X10- B9	B08-016	X10- B0	B08-015		$DB9-
$DB9+	X11- B9	B08-016	X11- B0	B08-015		$DB9-
$DMCL+	X08- E1	X09- E1	X08- E2	X09- E2		$DMCL-
$DRF+	X03-037	A26-013	X03-038	A26-014		$DRF-
$DSAP+	X08- D5	B21-044	X08- D6	B21-043		$DSAP-
$DSAP+	X09- D5	B21-044	X09- D6	B21-043		$DSAP-
$HWM+	X03-015	A14-017	X03-016	A14-018		$HWM-
$IMAF+	A11-035	A19-006	A11-025	A19-002		$IMAF-
$IMAF+	A19-006	A22-006	A19-002	A22-002		$IMAF-
$INT+	TB1-045	B20-010	TB1-046	B20-009	$INT-	STRANDED WIRE
$INT+	X02- A	TB1-045	X02- B	TB1-046	$INT-	STRANDED WIRE
$LINE	A26-009	T1-005	A26-010	T1-003		$LINE
$MCL+	X04- D7	B36-042	X04- D8	B36-041		$MCL-
$MCL+	X05- D7	B36-042	X05- D8	B36-041		$MCL-
$NT1+	X10- F3	X11- E3	X10- E4	X11- E4		$NT1-
$NT10+	X08- F5	X09- E5	X08- E6	X09- E6		$NT10-
$NT11+	X08- E7	X09- E7	X08- E8	X09- E8		$NT11-
$NT12+	X08- E9	X09- E9	X08- E0	X09- E0		$NT12-

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$NT13+	X08- F1	X09- F1	X08- F2	X09- F2	$NT13-
$NT15+	X08- F5	X09- F5	X08- F6	X09- F6	$NT15-
$NT2+	X10- F5	X11- E5	X10- E6	X11- E6	$NT2-
$NT3+	X10- F7	X11- E7	X10- E8	X11- E8	$NT3-
$NT4+	X10- F9	X11- E9	X10- E0	X11- E0	$NT4-
$NT5+	X10- F1	X11- F1	X10- F2	X11- F2	$NT5-
$NT6+	X10- F3	X11- F3	X10- F4	X11- F4	$NT6-
$NT7+	X10- F5	X11- F5	X10- F6	X11- F6	$NT7-
$NT8+	X10- F7	X11- F7	X10- F8	X11- F8	$NT8-
$NT9+	X08- F3	X09- E3	X08- E4	X09- E4	$NT9-
$OM+	X03-003	A14-013	X03-004	A14-014	$OM-
$PIOR+	X08- D3	B21-046	X08- D4	B21-045	$PIOR-
$PIOR+	X09- D3	B21-046	X09- D4	B21-045	PIOR-
$PPF+	X10- F1	X11- E1	X10- E2	X11- E2	$PPF-
$PROT+	X10- D5	B26-043	X10- D6	B26-044	$PROT-
$PROT+	X11- D5	B26-043	X11- D6	B26-044	$PROT-
$QR0+	X04- A1	B26-030	X04- A2	B26-029	$QR0-
$QR0+	X05- A1	B26-030	X05- A2	B26-029	$QR0-
QR1+	X04- A3	B26-028	X04- A4	B26-027	$QR1-
$QR1+	X05- A3	B26-028	X05- A4	B26-027	$QR1-

$QR10+	X04- C1	B36-008	X04- C2	B36-007	$QR10-
$QR10+	X05- C1	B36-008	X05- C2	B36-007	$QR10-
$QR11+	X04- C3	X05- C3	X04- C4	X05- C4	$QR11-
$QR12+	X04- C5	X05- C5	X04- C6	X05- C6	$QR12-
$QR13+	X04- C7	X05- C7	X04- C8	X05- C8	$QR13-
$QR14+	X04- C9	X05- C9	X04- C0	X05- C0	$QR14-
$QR15+	X04- D1	X05- D1	X04- D2	X05- D2	$QR15-
$QR2+	X04- A5	B26-020	X04- A6	B26-019	$QR2-
$QR2+	X05- A5	B26-020	X05- A6	B26-019	$QR2-
$QR3+	X04- A7	B26-014	X04- A8	B26-013	$QR3-
$QR3+	X05- A7	B26-014	X05- A8	B26-013	$QR3-
$QR4+	X04- A9	X05- A9	X04- A0	X05- A0	$QR4-
$QR5+	X04- B1	X05- B1	X04- B2	X05- B2	$QR5-
$QR6+	X04- B3	X05- B3	X04- B4	X05- B4	$QR6-
$QR7+	X04- B5	B36-030	X04- B6	B36-031	$QR7-
$QR7+	X05- B5	B36-030	X05- B6	B36-031	$QR7-
$QR8+	X04- B7	B36-021	X04- B8	B36-022	$QR8-
$QR8+	X05- B7	B36-021	X05- B8	B36-022	$QR8-
$QR9+	X04- B9	B36-012	X04- B0	B36-013	$QR9-
$QR9+	X05- B9	B36-012	X05- B0	B36-013	$QR9-
$RD+	X03-011	A11-009	X03-012	A11-002	$RD-

$READ+	X04- D3	B26-048	X04- D4	B26-046	$READ-
$READ+	X05- D3	B26-048	X05- D4	B26-046	$READ-
$RITE+	X04- D5	B26-040	X04- D6	B26-039	$RITE-
$RITE+	X05- D5	B26-040	X05- D6	B26-039	$RITE-
$RPLY+	X10- D7	B02-026	X10- D8	B02-025	$RPLY-
$RPLY+	X11- D7	B02-026	X11- D8	B02-025	$RPLY-
$RQST+	X08- D7	B02-015	X08- D8	B02-016	$RQST-
$RQST+	X09- D7	B02-015	X09- D8	B02-016	$RQST-
$SCN1+	X08- D1	B02-008	X08- D2	B02-007	$SCN1-
$SCN2+	X08- F7	B02-010	X08- F8	B02-009	$SCN2-
$SCN3+	X09- F7	B02-024	X09- F8	B02-023	$SCN3-
$SCN4+	X09- D1	B02-022	X09- D2	B02-021	$SCN4-
$SM+	X03-013	A14-015	X03-014	A14-016	$SM-
$SP+	X10- D3	X11- D3	X10- D4	X11- D4	$SP-
$SPE+	X10- D9	X11- D9	X10- D0	X11- D0	$SPE-
$TA0+	X03-017	A15-028	X03-018	A15-026	$TA0-
$TA1+	X03-019	A15-024	X03-020	A15-026	$TA1-
$TA2+	X03-021	A15-023	X03-022	A15-025	$TA2-
$TA3+	X03-023	A15-027	X03-024	A15-025	$TA3-
$TA4+	X03-025	A15-001	X03-026	A15-002	$TA4-

$TA5+	X03-027	A15-008	X03-028	A15-010		$TA5-
$TA6+	X03-029	A15-003	X03-030	A15-002		$TA6-
$TA7+	X03-031	A15-007	X03-032	A15-010		$TA7-
$TA8+	X03-033	A15-046	X03-034	A15-050		$TA8-
$TA9+	X03-035	A15-048	X03-036	A15-050		$TA9-
$TIME+	X04- F3	X05- E3	X04- E4	X05- E4		$TIME-
$TLKF+	A06-017	A07-017	A06-018	A07-018		$TLKF-
$TLKF+	A07-017	A08-037	A07-018	A08-038		$TLKF-
$TLKF+	A08-037	A11-028	A08-038	A11-026		$TLKF-
$TLKF+	A11-028	A26-003	A11-026	A26-004		$TLKF-
$V+20	B02-045	B36-034	B02-046	B36-032		$V-20
$V+20	B02-045	TB1-009	B02-046	TB1-019		$V-20
$V+20	X01- A	TB1-020	X01- B	TB1-040	$V-20	STRANDED WIRE
$V+20	X04- F9	TB1-001	X04- F0	TB1-011		$V-20
$V+20	X05- F9	TB1-002	X05- F0	TB1-012		$V-20
$V+20	X06- F9	TB1-003	X06- F0	TB1-013		$V-20
$V+20	X07- F9	TB1-004	X07- F0	TB1-014		$V-20
$V+20	X08- F9	TB1-005	X08- F0	TB1-015		$V-20
$V+20	X09- F9	TB1-006	X09- F0	TB1-016		$V-20
$V+20	X10- F9	TB1-007	X10- F0	TB1-017		$V-20
$V+20	X11- F9	TB1-008	X11- F0	TB1-018		$V-20
$WD+	X03-009	A12-004	X03-010	A12-002		$WD-
$WDIS+	X03-007	A26-027	X03-008	A26-025		$WDIS-
$WEF+	X03-005	A12-001	X03-006	A12-002		$WEF-
$WISZ+	X04- F7	B36-039	X04- F8	B36-040		$WISZ-
$WISZ+	X05- F7	B36-039	X05- F8	B36-040		$WISZ-
$WREN+	X08- D9	B02-005	X08- D0	B02-006		$WREN-

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$WREN+	X09- D9	B02-005	X09- D0	B02-006	$WREN-
$WS0F	A07-028	A12-027	A07-026	A12-025	$WS0F-
$WS0F+	A06-028	A07-028	A06-026	A07-026	$WS0F-

ΔINTF	A32-022
ΔINTF	A33-027
ΔLARM	A32-024
ΔLARM	A32-033
ΔLARM	A33-003
ΔLARM	A34-020
ΔQPP	A34-048
ΔQPP	A36-004
ΔQPP	B36-043
QPPF	A36-001
ΔQPPF	A36-037
ΔRMF	A33-001
ΔRMF	A34-014
ΔRMF	A34-017
ΔRMF	A35-018
Δ0	A19-005
Δ0	A21-044
Δ0	A28-011
Δ0	A30-034
Δ0F	A30-031
Δ0F	A30-044
Δ0F	A36-029
Δ1	A19-008
Δ1	A21-043
Δ1	A30-004
Δ1	A30-011
Δ1	A30-013

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A1F	A30-001
A1F	A30-024
A10	A17-004
A10	A22-003
A10	A24-048
A11	A17-047
A11	A22-004
A11	A24-045
A12	A17-048
A12	A22-047
A12	A24-004
A13	A17-043
A13	A22-048
A13	A24-001
A14	A17-045
A14	A22-043
A14	A24-006
A15	A22-045
A15	A24-005
A2	A19-003
A2	A21-048
A2	A30-003
A2F	A30-006
A2F	A30-020
A3	A19-004
A3	A21-045
A3	A30-007
A3	A30-048
A3F	A30-009
A3F	A30-010
A3F	A30-030

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A4	A19-047
A4	A21-004
A4	A30-005
A4	A30-037
A4F	A30-008
A4F	A30-018
A4F	A30-028
A5	A15-042
A5	A19-048
A5	A21-001
A6	A15-043
A6	A19-043
A6	A21-006
A7	A17-005
A7	A19-045
7	A21-005
A8	A17-008
A8	A22-005
A8	A24-044
A9	A17-003
A9	A22-008
A9	A24-043
BADF	A28-035
BADF	A33-010
BC6	A11-010
BC6	A17-011
BC6F	A11-005
BC6F	A14-043
BC6F	A17-015
BC6F	A17-018
BC7F	A11-023

BC7F	A12-047
BC7F	A14-036
BC7F	A15-015
BZ	A35-020
BZ	A36-028
BZ	A36-030
BZF	A29-007
BZF	A35-030
CAC	A11-041
CAC	A23-017
CAC	B14-033
CACAF	A20-032
CACAF	A23-018
CACD	A11-029
CACD	A12-021
CARC	A19-046
CARC	A22-012
CARMF	A30-016
CARMF	A32-015
CA0	A19-009
CA0	A20-045
CA0F	A19-020
CA0F	A20-043
CA1	A19-021
CA1	A20-046
CA1F	A19-027
CA1F	A20-040
CA10	A22-010

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CA10	A23-036
CA10F	A22-019
CA10F	A23-034
CA11	A22-022
CA11	A23-033
CA11F	A22-023
CA11F	A23-027
CA12	A22-033
CA12	A23-021
CA12F	A22-039
CA12F	A23-023
CA13	A22-030
CA13	A23-020
CA13F	A22-034
CA13F	A23-014
CA14	A22-036
CA14	A23-010
CA14F	A22-037
CA14F	A23-008
CA15	A22-029
CA15	A23-009
CA15F	A22-031
CA15F	A23-003
CA2	A19-010
CA2	A20-036
CA2F	A19-019

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CA2F	A20-034
CA3	A19-022
CA3	A20-033
CA3F	A19-023
CA3F	A20-027
CA4	A19-033
CA4	A20-021
CA4F	A19-039
CA4F	A20-023
CA5	A19-030
CA5	A20-020
CA5F	A19-034
CA5F	A20-014
CA6	A19-036
CA6	A20-010
CA6F	A19-037
CA6F	A20-008
CA7	A19-029
CA7	A20-009
CA7F	A19-031
CA7F	A20-003
CA8	A22-009
CA8	A23-045
CA8F	A22-020
CA8F	A23-043
CA9	A22-021

CA9	A23-046
CA9F	A22-027
CA9F	A23-040
CEOPF	A31-034
CEOPF	A36-012
CIOPF	A34-021
CIOPF	A34-046
CLEF	A28-012
CLEF	A29-013
CLK2	A31-003
CLK2	A31-014
CLK2	A31-022
CLK2	A31-032
CLK2	A32-001
CLK2	A35-003
CLR	A26-039
CLR	A29-016
CLR	A29-040
CLR	A29-041
CLR	A31-029
CLR	A31-031
CLR	A32-036
CLRF	A09-047
CLRF	A11-001
CLRF	A18-004
CLRF	A29-015
CLRF	A29-042
CLRF	A32-014
CLRF	A32-018
CLRF	A32-019
CLRF	A32-042
CLRF	A34-019
CLRF	A35-033
CLRF	A36-048
CNCT	A33-041
CNCT	A36-009

CNCT A36-031

CNCTF A26-046
CNCTF A36-034
CNCTF B36-025

COPIF A30-012
COPIF A32-011

CRUNF A31-013
CRUNF A31-033
CRUNF A32-035

CS1F B11-026
CS1F B12-026

CS2F B13-026
CS2F B14-026

CTE A14-037
CTE A15-034
CTE A26-030
CTE A30-036
CTE A34-034

CTEF A34-011
CTEF A34-029
CTEF A34-031
CTEF A35-016
CTEF A35-019

CWAZF A09-013
CWAZF A09-040

CWBZ A09-012
CWBZ A09-037

CWEF A33-006
CWEF A34-008

CWZ A09-039

CWZ	A11-ōō6
CW0F	A08-ōō5
CW0F	A09-020
CW1F	A08-ōō4
CW1F	A09-ōī9
CW10F	A08-029
CW10F	A09-ōō8
CW11F	A08-028
CW11F	A09-ōō7
CW12F	A08-031
CW12F	A09-ōō6
CW13F	A08-030
CW13F	A09-ōō5
CW14F	A08-032
CW14F	A09-ōō4
CW15	A08-ōō6
CW15	A11-018
CW15	A12-ōō8
CW15F	A08-ōō7
CW15F	A09-ōō1
CW15F	A11-ōī9
CW15F	A12-ōō9
CW2F	A08-ōō9
CW2F	A09-ōī8
CW3F	A08-ōī0
CW3F	A09-ōī7
CW4F	A08-ōī5
CW4F	A09-ōī6

CW5F	A08-013
CW5F	A09-015
CW6F	A08-019
CW6F	A09-014
CW7F	A08-020
CW7F	A09-011
CW8F	A08-027
CW8F	A09-010
CW9F	A08-023
CW9F	A09-009
DAS1F	B11-025
DAS1F	B12-025
DAS2F	B13-025
DAS2F	B14-025
DATA	A26-008
DATA	A28-015
DATA	A29-012
DATA	A35-009
DATAF	A35-017
DATAF	A36-019
DB0	A06-009
DB0	B06-012
DB1	A06-008
DB1	B06-020
DB10	A07-007
DB10	B08-040

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DB11	A07-013
DB11	B08-048
DB12	A07-029
DB12	B09-012
DB13	A07-037
DB13	B09-020
DB14	A07-040
DB14	B09-040
DB15	A07-039
DB15	B09-048
DB2	A06-007
DB2	B06-040
DB3	A06-013
DB3	B06-048
DB4	A06-029
DB4	B07-012
DB5	A06-037
DB5	B07-020
DB6	A06-040
DB6	B07-040
DB7	A06-039
DB7	B07-048
DB8	A07-009
DB8	B08-012
DB9	A07-008
DB9	B08-020

39740700 D DRUM CONTROLLER

DFF	A30-014
DFE	A30-015
DFE	A30-040
DFE	A30-045
DR	A28-008
DR	A33-004
DS1F	B11-022
DS1F	B12-022
DS2F	B13-022
DS2F	B14-022
DW	A08-048
DW	A09-031
DW	A09-045
DW	A11-021
DWC0F	A08-001
DWC0F	A12-010
DWC1F	A12-020
DWC1F	A15-019
DWF	A06-034
DWF	A07-034
DWF	A09-036
DWF	A09-043
DWF	A12-017
DW1F	A12-033
DW1F	A14-044
EARMF	A30-038
EARMF	A32-044
EEOPF	A30-047
EEOPF	A32-028
EINTF	A32-032

EINTF	A33-021
ELAR	A29-004
ELAR	A29-039
ELAR	A29-044
ELAR	A29-046
EOP	A31-040
EOP	A32-030
ERS	A08-033
ERS	A17-014
ERSF	A06-032
ERSF	A07-032
ERSF	A11-036
ERSF	A17-013
ERW	A29-018
RW	A29-021
ERW	A29-023
EWS0F	A06-031
EWS0F	A07-031
EWS0F	A12-045
EWS1	A08-035
EWS1	A12-007
EWS2F	A08-047
EWS2F	A12-018
FC0	A20-044
FC0	A21-036
FC0F	A20-048
FC0F	A21-041
FC1	A20-039
C1	A21-038

FC1F	A20-042
FC1F	A21-039
FC10	A23-031
FC10	A24-028
FC10F	A23-035
FC10F	A24-033
FC11	A23-030
FC11	A24-030
FC11F	A23-029
FC11F	A24-031
FC12	A23-019
FC12	A24-017
FC12F	A23-022
FC12F	A24-024
FC13	A23-015
FC13	A24-019
FC13F	A23-016
FC13F	A24-022
FC14	A23-007
FC14	A24-010
FC14F	A23-011
FC14F	A24-016
FC15	A23-004
FC15	A24-012
FC15F	A23-005
FC15F	A24-014

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FC2	A20-031
FC2	A21-028
FC2F	A20-035
FC2F	A21-033
FC3	A20-030
FC3	A21-030
FC3F	A20-029
FC3F	A21-031
FC4	A20-019
FC4	A21-017
FC4F	A20-022
FC4F	A21-024
FC5	A20-015
FC5	A21-019
FC5F	A20-016
FC5F	A21-022
FC6	A20-007
FC6	A21-010
FC6F	A20-011
FC6F	A21-016
FC7	A20-004
FC7	A21-012
FC7F	A20-005
FC7F	A21-014
C8	A23-044
C8	A24-036

FC8F	A23-048
FC8F	A24-041
FC9	A23-039
FC9	A24-038
FC9F	A23-042
FC9F	A24-039
GAE	A18-024
GAE	A28-036
GAJ0	A16-046
GAJ0	A18-033
GAJ1	A16-044
GAJ1	A18-036
GAJ2	A16-042
GAJ2	A18-034
GAJ3	A16-040
GAJ3	A18-032
GAJ4	A16-038
GAJ4	A18-030
GAJ5	A16-036
GAJ5	A18-028
GAJ6	A16-034
GAJ6	A18-029
GAJ7	A16-032
GAJ7	A18-020
GAPF	A11-004
GAPF	A12-031
GAPF	A14-034

GAPF	A15-040
GATEF	A21-046
GATEF	A24-046
GATEF	A26-044
GATEF	A30-019
GATEF	A30-021
GATEF	A30-023
GATEF	A30-029
GATEF	A30-043
GA1	A14-031
GA1	A30-022
GA4	A14-023
GA4	A30-027
GCLKF	A33-039
GCLKF	A34-036
GCLK1	A34-035
GCLK1	A35-014
GCLK1	A35-022
GRD	A11-002
GRD	A11-025
GRD	A16-002
GRD	A16-003
GRD	A16-005
GRD	A16-007
GRD	A16-009
GRD	A16-031
GRD	A16-033
GRD	A16-035
GRD	A16-037
GRD	A16-039
GRD	A16-041
GRD	A16-043
GRD	A16-045
GRD	A16-050

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GRD A19-002
GRD A19-007

GRD A21-002
GRD A21-009
GRD A21-011
GRD A21-018
GRD A21-020

GRD A21-027
GRD A21-029
GRD A21-035
GRD A21-037
GRD A21-050

GRD A22-002
GRD A22-007

GRD A24-002
GRD A24-013
GRD A24-015
GRD A24-021
GRD A24-023

GRD A24-027
GRD A24-032
GRD A24-035
GRD A24-040
GRD A24-050

GRD A26-025
GRD A26-026
GRD A26-050

GRD A28-002
GRD A28-003
GRD A28-004

GRD A33-040
GRD A33-050

GRD A35-001
GRD A35-002

GRD	A35-029
GRD	A35-041
GRD	A35-050
GRD	B02-002
GRD	B02-019
GRD	B02-031
GRD	B02-050
GRD	B11-002
GRD	B11-021
GRD	B11-023
GRD	B12-002
GRD	B12-021
GRD	B12-023
GRD	B13-002
GRD	B13-021
GRD	B13-023
GRD	B14-002
GRD	B14-021
GRD	B14-023
HWM+	A12-046
HWM+	A14-017
HWM+	A15-031
INT	B11-032
INT	B20-011
IOP	A29-006
IOP	A34-016
IOP	A34-024
IOPF	A33-032
IOPF	A34-018
IOPF	A34-022

TTAF A15-032
TTAF A17-007

LDF A33-005
LDF A35-010

LFCAF A21-007
LFCAF A21-008
LFCAF A24-007
LFCAF A24-008
LFCAF A29-037

LICAF A19-017
LICAF A22-017
LICAF A29-048

LR0RF A06-019
LR0RF A07-019
LR0RF A11-040

LR0WF A06-020
LR0WF A07-020
LR0WF A12-040

LR1RF A06-036
LR1RF A07-036
LR1RF A11-037

LR2RF A06-033
LR2RF A07-033
LR2RF A11-030

LR2WF A06-016
LR2WF A07-016
LR2WF A12-044

LSAF A14-041
LSAF A18-018
LSAF A29-034

LTAF A15-038
LTAF A17-017
LTAF A29-031
LTAF A29-043

ME2 A31-020
ME2 A31-036

NAP A32-009
NAP A32-027
NAP A32-029

NAPF A32-012
NAPF A32-023

NARM A32-013
NARM A32-021
NARM A32-046

ARMF A32-016
ARMF A32-043

ONE A09-033
ONE A09-034
ONE A09-041
ONE A09-042
ONE A09-044
ONE A12-011
ONE A12-014
ONE A17-016
ONE A19-012
ONE A19-013
ONE A19-015
ONE A21-003
ONE A21-013
ONE A21-015
ONE A21-021
ONE A21-023
ONE A21-032
ONE A21-034
ONE A21-040
ONE A21-042
ONE A24-003
ONE A24-009
NE A24-011
NE A24-018

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ONE A24-020
ONE A24-029
ONE A24-034
ONE A24-037
ONE A24-042
ONE A26-028
ONE A28-001
ONE A28-006
ONE A31-004
ONE A31-007
ONE A31-008
ONE A31-011
ONE A31-016
ONE A31-021
ONE A31-024
ONE A31-027
ONE A31-028
ONE A31-038
ONE A33-030
ONE A33-044
ONE A33-045
ONE A35-007
ONE A35-008
ONE A35-011
ONE A35-013
ONE A35-024
ONE A35-027
ONE A35-028
ONE A35-036
ONE A35-038
ONE A35-045
ONE A35-048

OR A22-014
OR A22-015

ORA6 A16-010
ORA6 A18-011

ORA7 A16-008
ORA7 A18-017

ORA8 A16-006
ORA8 A18-014

ORA9 A16-004
ORA9 A18-012

ORF	A11-034
ORF	A22-013
ORF	A22-016
PF	A26-016
PF	A34-003
PFF	A33-009
PFF	A34-006
PRIOR	B02-011
PRIOR	B02-033
PROF	A36-045
PROF	A36-046
PROFF	A33-007
PROFF	A36-043
ROFF	A36-047
PROK	A26-045
PROK	A33-042
PROK	A36-038
PROK	A36-039
PROTS	A36-040
PROTS	B36-037
QISC	A26-033
QISC	A29-047
QISE	A26-037
QISE	A29-038
QISO	A26-019
QISO	A29-022
ISO4	A26-012
ISO4	A36-020

QIS1	A26-021
QIS1	A28-028
QIS1	A28-030
QIS2	A26-022
QIS2	A28-020
QIS2	A28-024
QIS3	A26-023
QIS3	A28-044
QIS3	A28-048
QIS4	A26-018
QIS4	A28-040
QIS4	A28-042
QIS4	A29-027
QIS8	A26-017
QIS8	A29-045
Q0	A26-020
Q0	A28-009
Q0	A36-005
Q0F	A36-008
Q0F	A36-023
Q1	A26-034
Q1	B26-025
Q2	A26-031
Q2	B26-011
Q3	A26-032
Q3	B26-017
RC0F	A11-031
RC0F	A15-020

RDATA	A34-012
RDATA	A35-012
RDC	A08-045
RDC	A11-016
RDCF	A08-043
RDCF	A11-022
RDF	A06-024
RDF	A11-014
READ	A26-043
READ	B26-041
RFDF	A29-024
RFDF	A34-042
RFDF	A36-015
RJTWF	A36-022
RJTWF	A36-042
ROSRF	A34-030
ROSRF	A35-021
ROSRF	A36-035
ROW	A26-048
ROW	A35-034
ROW	A35-046
RP	A26-047
RP	A28-019
RP	A28-021
RP	A28-023
RP	A28-029
RP	A28-037
RP	A28-039
RP	A28-043
RP	A28-045
RPLYF	A32-008
RPLYF	A33-034

RQSTF B20-039
RQSTF B21-039

RRUN A31-012
RRUN A32-047

RUN A18-006
RUN A31-001
RUN A31-009
RUN A31-023
RUN A36-036

RUNF A31-017
RUNF A31-019
RUNF A31-035
RUNF A34-009
RUNF A35-015

RWP A26-041
RWP A35-032
RWP A35-043

R015 A07-043
R015 A12-005

R015F A06-023
R015F A07-048
R015F A12-006

R07F A06-048
R07F A07-023
R07F A07-024

R20 A06-001
R20 B06-003

R21 A06-003
R21 B06-004

R210 A07-004

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R210	B08-031
R211	A07-015
R211	B08-030
R212	A07-045
R212	B09-003
R213	A07-046
R213	B09-004
R214	A07-047
R214	B09-031
R215	A07-044
R215	B09-030
R22	A06-004
R22	B06-031
R23	A06-015
R23	B06-030
R24	A06-045
R24	B07-003
R25	A06-046
R25	B07-004
R26	A06-047
R26	B07-031
R27	A06-044
R27	B07-030
R28	A07-001
R28	B08-003
R29	A07-003

B29	B08-004
SAC	A11-020
SAC	A12-029
SAC	A14-019
SAC	B14-008
SBZ	A34-032
SBZ	A35-023
SC31F	A14-039
SC31F	A15-014
SC4	A14-030
SC4	B12-005
SET1F	A33-046
SET1F	A36-027
SET2F	A33-047
SET2F	A36-032
SET3F	A33-048
SET3F	A36-017
SIOPF	A34-015
SIOPF	A34-044
SIOPF	A34-047
SLD	A34-027
SLD	A35-005
SM+	A08-046
SM+	A11-017
SM+	A12-024
SM+	A14-015
SM+	A15-041
SM+	A26-029
SOR	A18-001
SOR	A28-033

SOR B14-036

SPROF A33-031
SPROF A36-044

SRJT A35-035
SRJT A36-003
SRJT A36-041

SRJTF A35-047
SRJTF A36-006
SRJTF A36-011

SRUN A31-006
SRUN A31-018
SRUN A36-033

SRW A34-041
SRW A34-043
SRW A34-045

SSRUN A31-005
SSRUN A36-016

SS1F B11-024
SS1F B12-024

SS2F B13-024
SS2F B14-024

STDF A18-022
STDF A31-015

STEC A30-035
STEC A32-020

STECF A32-017
STECF A32-037

SUPF A09-048

SUPF A15-033
SUPF A17-035
SUPF A19-035
SUPF A22-035
SUPF A26-007
SUPF A29-032
SUPF A34-013
SUPF A36-018

TAC A15-021
TAC A17-012

TA0 A15-017
TA0 A18-035

TA1 A15-018
TA1 A18-040

TA2 A17-009
TA2 A18-038

TA2F A15-022
TA2F A17-020

TA3 A17-021
TA3 A18-037

TA3F A15-030
TA3F A17-027

TA4 A17-010
TA4 A18-031

TA4F A15-004
TA4F A17-019

TA5 A17-022
TA5 A18-039

TA5F A15-005
TA5F A17-023

TA6	A17-033
TA6	A18-010
TA6F	A15-006
TA6F	A17-039
TA7	A17-030
TA7	A18-016
TA7F	A15-009
TA7F	A17-034
TA8	A17-036
TA8	A18-015
TA8F	A15-045
TA8F	A17-037
TA9	A17-029
TA9	A18-009
TA9F	A33-014
TA9F	A33-015
TA9F	A33-016
TA9F	A33-017
TE	A14-045
TE	A15-037
TE	A26-038
TE	A34-007
TEC	A32-038
TEC	A32-039
TECF	A32-040
TECF	A32-041
TECF	A33-028
TEF	A33-008

TEF	A34-010
V+5	A36-049
V+5	B36-023
V-6	B02-047
V-6	B06-047
V-6	B07-047
V-6	B08-047
V-6	B09-047
V-6	B11-047
V-6	B12-047
V-6	B13-047
V-6	B14-047
V-6	B20-047
V-6	B21-047
V-6	B26-047
V-6	B36-047
WBF	A06-014
WBF	A07-014
WBF	A12-030
WCS5F	A12-039
WCS5F	A32-048
WCW	A08-003
WCW	A12-013
WCWF	A08-042
WCWF	A12-015
WC0F	A11-013
WC0F	A12-037
WC0F	A14-007
WDC	A08-044
WDC	A12-012
WDCF	A08-041
WDCF	A12-003

WENF1 B06-026
WENF1 B07-026

WENF2 B08-026
WENF2 B09-026

WFSMF A26-036
WFSMF A30-033

WN0F A11-043
WN0F A12-043

WN1F A11-048
WN1F A12-041

WODF A29-019
WODF A34-039
WODF A36-013

WP A26-040
WP A28-014
WP A29-010
WP A29-011

WREN A11-042
WREN A19-016
WREN A19-018
WREN A29-005

WRF A12-035
WRF A22-011

WRITE A26-042
WRITE A33-037
WRITE A36-014
WRITE A36-024
WRITE B26-031

WRJT A33-043
WRJT A36-021

W15F	A14-006
W15F	A15-044
W15F	A18-041
W193F	A12-034
W193F	A14-004
W196F	A11-008
W196F	A14-008
W197F	A11-003
W197F	A14-005
W197F	A15-039
W2F	A11-007
W2F	A14-003

Appendix A

LOGIC PACKAGE

The document presented in this appendix is a CDC released drawing and is identified by Drawing Number 39745600. The document is complete within itself and has not been renumbered to agree with page numbers of this manual.

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
A		RELEASED		7-9-71		
B	DDC	REVISED SHTS 5-9, 13-16, 18, 19, 20, 24, 25, 27, 28, 29, 33, 35, 36, 37, 42, 45, 49, 50, 51. ECR 4480	TC	10-13-71		
C	DDC	REVISED SHT 15. ECR 4535		11-23-71		
D	13099	REVISED SHTS 9, 10, 14, 15, 16, 21, & 37.	TC	4-19-72		
E	13127	REVISED SHT 27 PER ECO		6-16-72		
F	DDC	REV SHT 3, 14, 16, 17, 28, 36, 10, 9 AND 45 PER ECR 4677		7-7-72		

39745600

REFERENCE DRAWINGS	CONTROL DATA	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	TITLE
	FIRST USED ON		LOGIC DIAGRAM — DRUM CONTROLLER
	DR	7-1-71	
	CHK	7-1-71	
	ENGR	7-8-71	
	MFG		
	APPD	7-9-71	

COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES			
CAP.			

CODE IDENT NO.	DRAWING NUMBER
09132	39745600
39740900	SHEET 1 OF 59

MODULE B

MODULE A

		1		
ILLT	MEMORY SCANNER, TTL	2		
		3		
		4		
		5		
ILET	DSA DATA INTERFACE BITS 0-3	6	DATA REGISTER (BITS 0-7)	ILCT
ILET	DSA DATA INTERFACE BITS 4-7	7	DATA REGISTER (BITS 8-15)	ILCT
ILET	DSA DATA INTERFACE BITS 8-11	8	CHECKWORD GEN	ILBT 96JT
ILET	DSA DATA INTERFACE BITS 12-15	9	TTL GATE, HIGH FAN IN	
		10		
ILAT	A-REGISTER INTERFACE BITS 0-3	11	DRUM READ/DSA CONTROL	ILDT
ILAT	A-REGISTER INTERFACE BITS 4-7	12	DRUM WRITE CONTROL	ILFT
ILAT	A-REGISTER INTERFACE BITS 8-11	13		
ILAT	A-REGISTER INTERFACE BITS 12-15	14	TRACK TIMING #1	ILAT
		15	TRACK TIMING #2	ILE7
		16	GUARDED ADDRESS / SECTOR OVER-RANGE JUMPERS	
		17	TRACK ADDRESS REGISTER BITS 2-9	96ET
		18	GUARDED ADDR/SECTOR OVER-RANGE ERROR DETECT	IMBT 96GT
		19	CORE ADDRESS REGISTER BITS 0-7	96JT
ILLT	CORE ADDRESS TRANSMITTER BITS 0-7	20	CORE ADDRESS COMPARE BITS 0-7	96JT
ILLT	CORE ADDRESS TRANSMITTER BITS 8-15	21	FINAL CORE ADDRESS REGISTER BITS 0-7	96FT
		22	CORE ADDRESS REGISTER BITS 8-15	96ET
		23	CORE ADDRESS COMPARE BITS 8-15	96JT
		24	FINAL CORE ADDRESS REGISTER BITS 8-15	96FT
		25		
ILMT	MISC RECEIVERS	26	CONTROLLER CLOCK	ILGT
		27		
		28	TTL GATE, LOW FAN IN	93KT
		29	NAND 2-INPUT SGL/DBL INV.	96DT
		30	TTL GATE LOW FAN IN	96KT
		31	JK FLIP-FLOP, 5	96JT
		32	TTL GATE, LOW FAN IN	93KT
		33	TTL GATE, HIGH FAN IN	96JT
		34	TTL GATE, LOW FAN IN	93KT
		35	JK FLIP-FLOP, 5	96JT
ILHT	EQUIPMENT SELECT, TTL	36	TTL GATE, LOW FAN IN	93KT
		37		
		38		
		39		
		40		
		41		
		42		

CARD TYPE / PRODUCT

CARD TITLE

CARD DWG. NO.

REV.

CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE CARD PLACEMENT

MODEL

DWG. NO. 397456C

REV. A

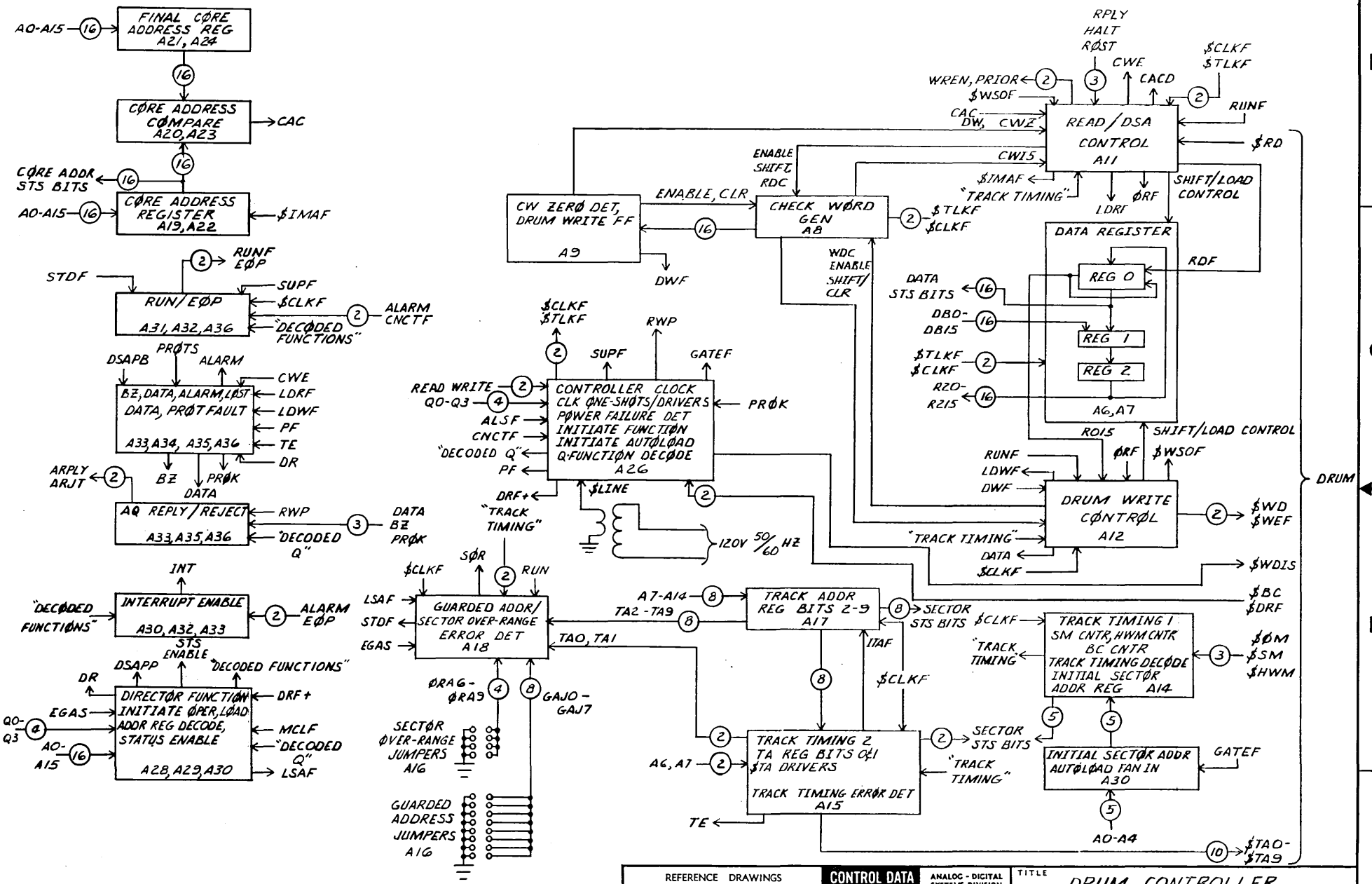
SHEET 2

PAGE

CARD POS.

5V TTL CARDS
"A" MODULE

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD



REFERENCE DRAWINGS	CONTROL DATA	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037
	FIRST USED ON	
	DR	
	CHK	
COMPONENTS, EXCEPT AS NOTED	ENGR	
TOLERANCE / VALUE / RATING	MFG	
RES	APPD	
CAP.		

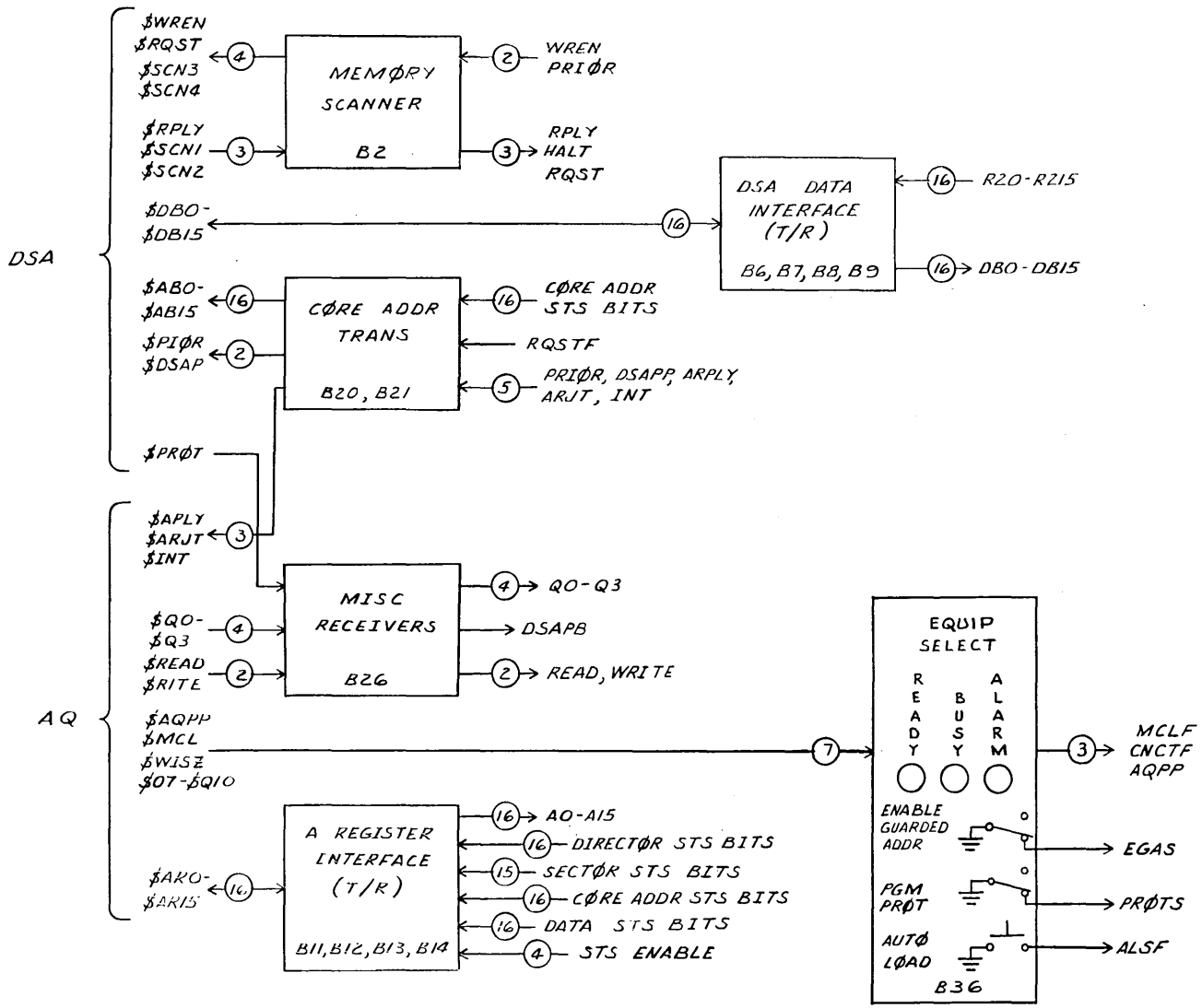
TITLE: DRUM CONTROLLER "FUNCTIONAL" BLOCK DIAGRAM

CODE IDENT NO.	DRAWING NUMBER	REV
C 09132	39745600	F

SHEET 3 OF

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD

6V DTL CARDS
"B" MODULE



REFERENCE DRAWINGS	CONTROL DATA CORPORATION	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	TITLE
			DRUM CONTROLLER "FUNCTIONAL" BLOCK DIAGRAM

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES			
CAP.			

FIRST USED ON			
DR			
CHK			
ENGR			
MFG			
APPD			

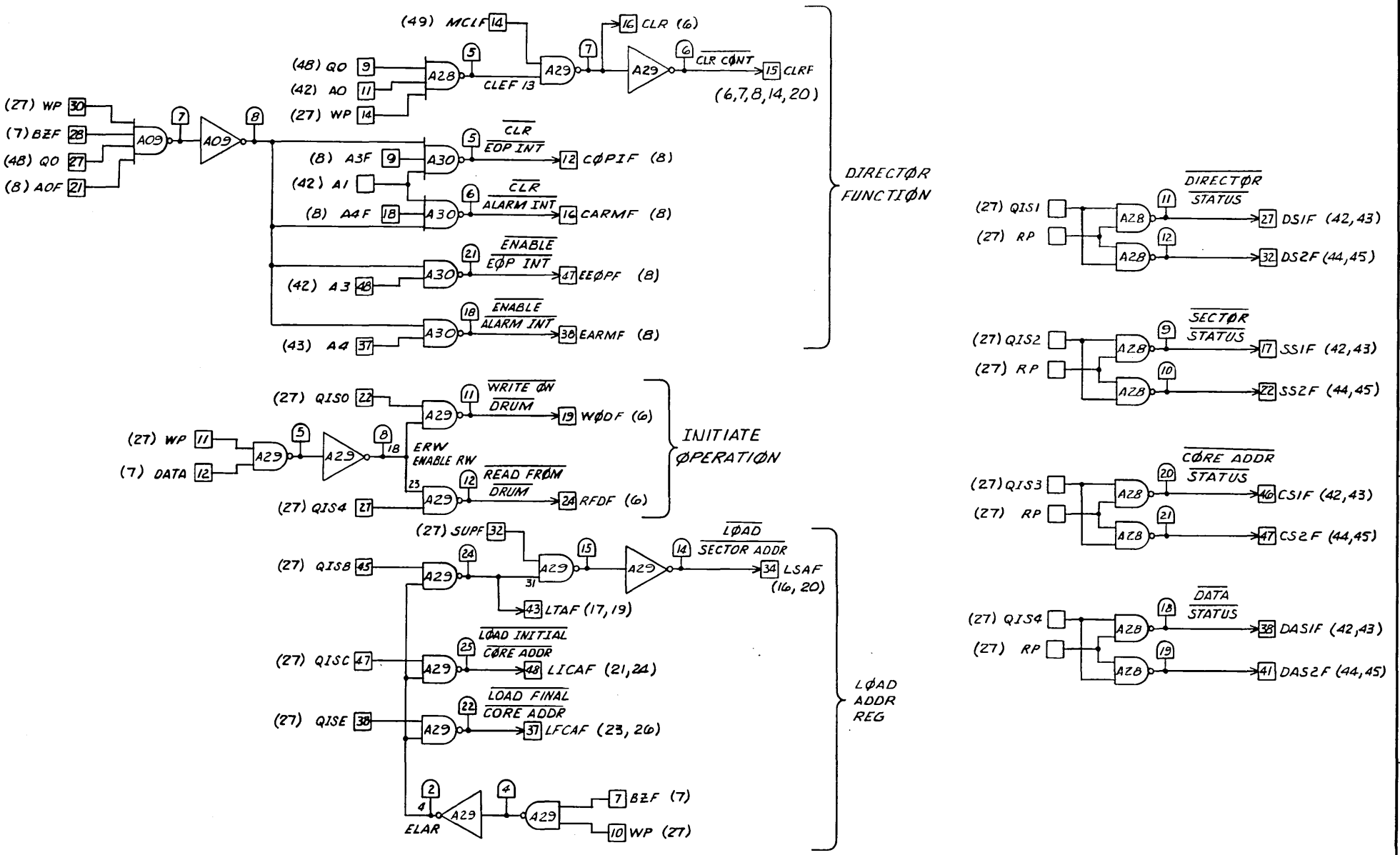
	CODE IDENT NO.	DRAWING NUMBER
C	09132	39745600

SHEET 4 OF

D C B A

4 3 2 1

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD

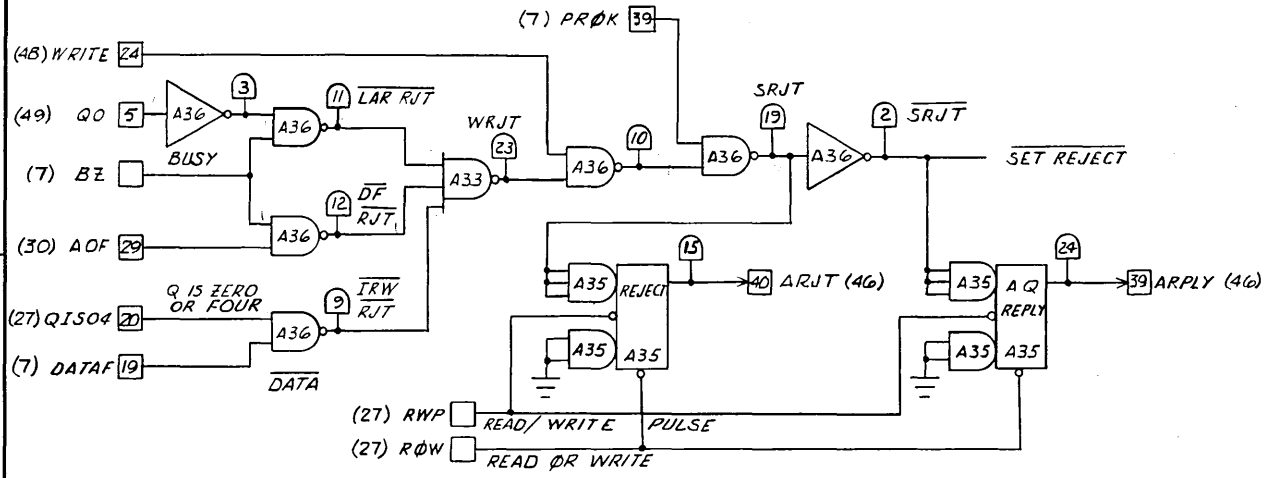


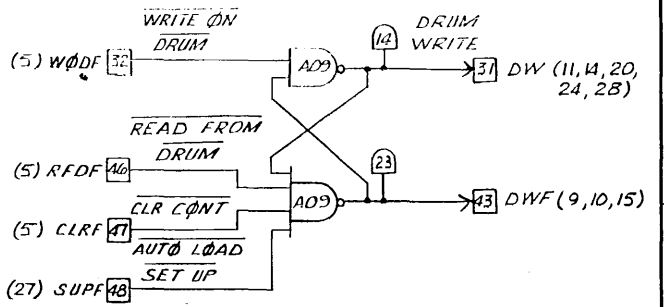
REFERENCE DRAWINGS	CONTROL DATA	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037
COMPONENTS, EXCEPT AS NOTED	FIRST USED ON	TITLE: DRUM CONTROLLER FUNCTION / STATUS DECODE "FLOW" LOGIC DIAGRAM
TOLERANCE / VALUE / RATING	DR	
RES	CHK	
CAP.	ENGR	
	MFG	
	APPD	

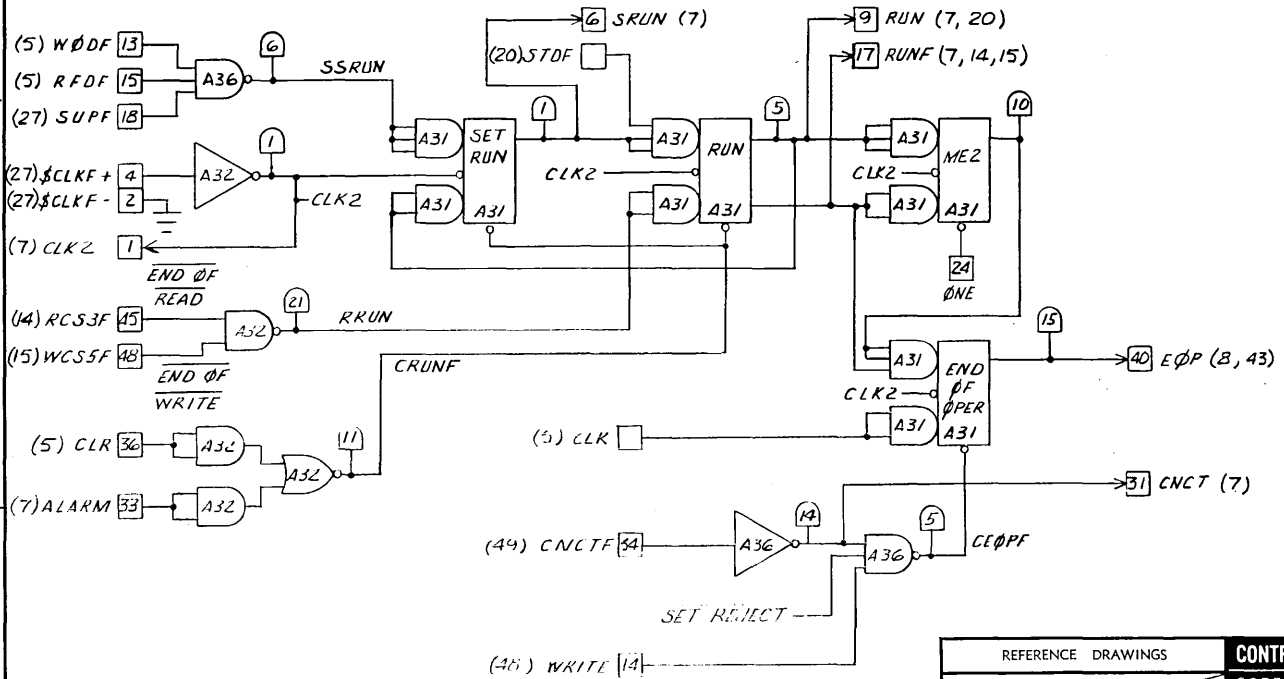
CODE IDENT NO.	DRAWING NUMBER	REV
C 09132	39745600	B

SHEET 5 OF

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD







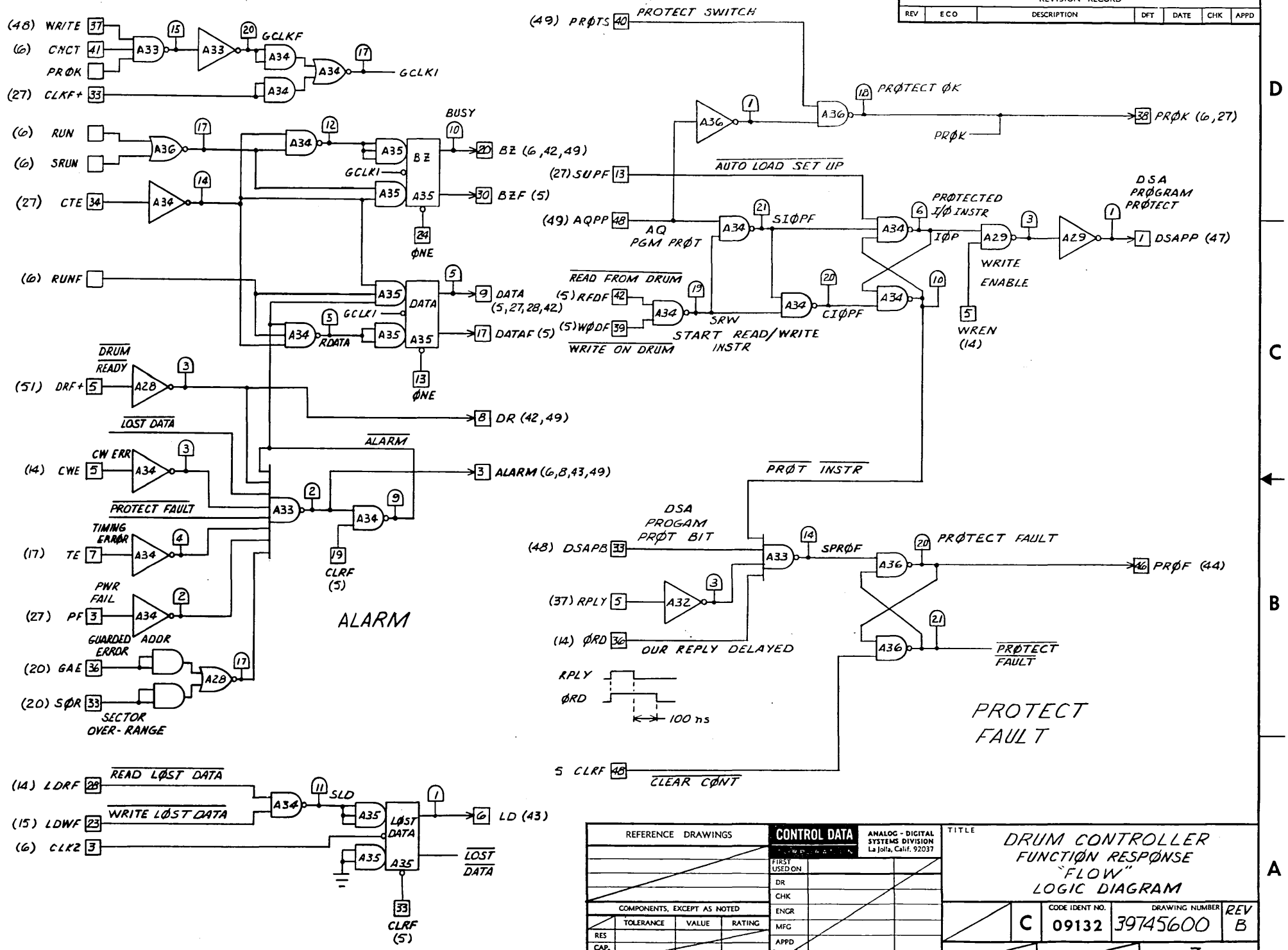
REFERENCE DRAWINGS	CONTROL DATA CORPORATION	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	TITLE
	FIRST USED ON		DRUM CONTRØLLER A/Q RESPØNSE CØNTRØL "FLØW" LØGIC DIAGRAM
COMPONENTS, EXCEPT AS NOTED	DR		
TOLERANCE / VALUE / RATING	CHK		
RES	ENGR		
CAP.	MFG		
	APPD		

SIZE	CODE IDENT NO.	DRAWING NUMBER	REV
C	09132	39745600	B

SHEET 6 OF

3 2 1

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD



REFERENCE DRAWINGS			

COMPONENTS, EXCEPT AS NOTED			
	TOLERANCE	VALUE	RATING
RES			
CAP.			

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON			
DR			
CHK			
ENGR			
MFG			
APPD			

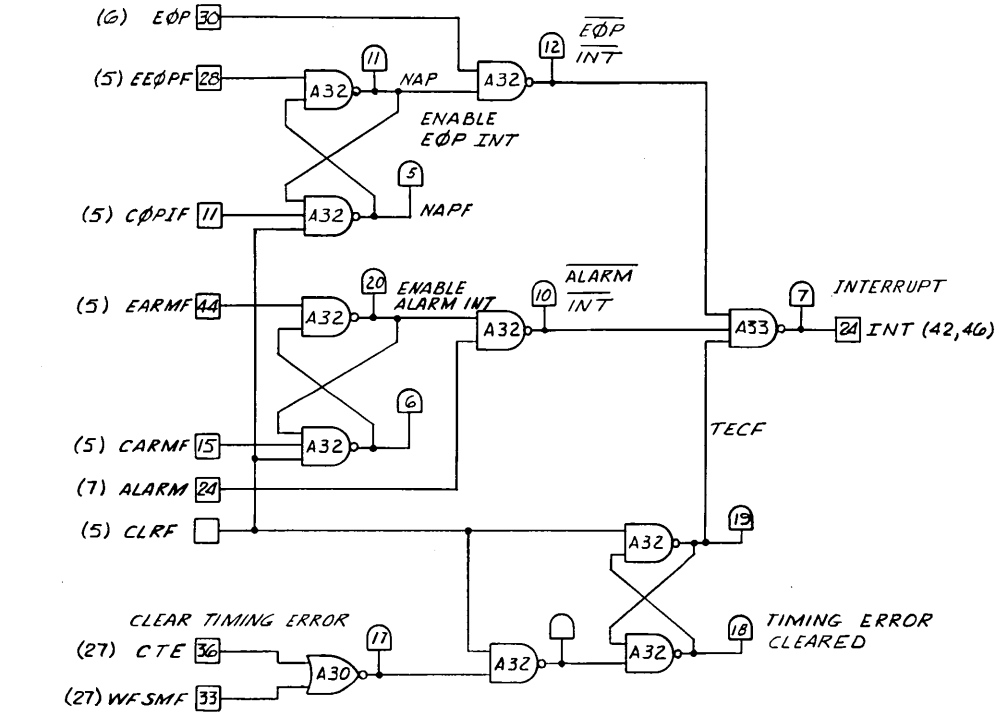
TITLE

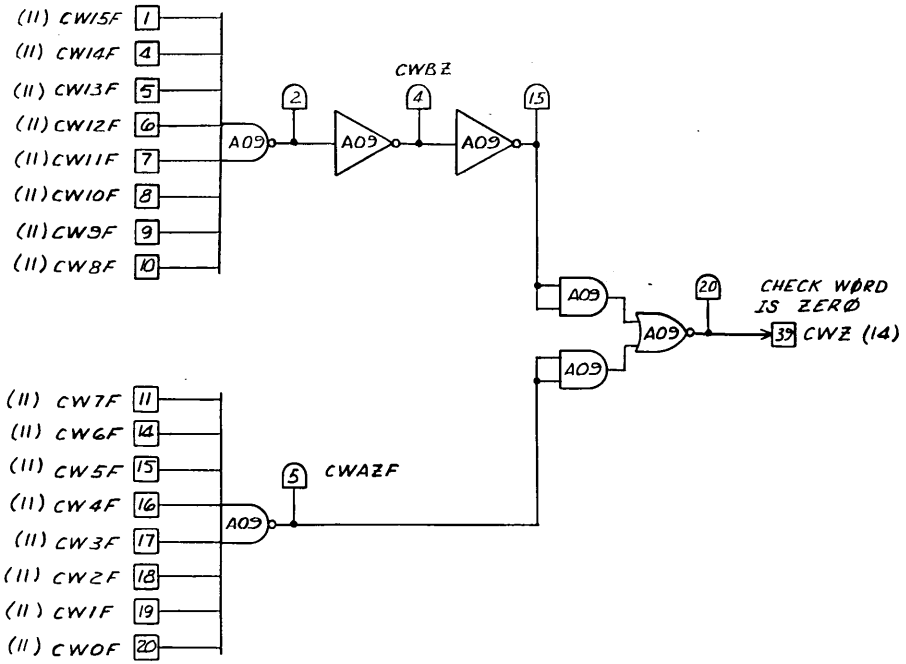
DRUM CONTROLLER FUNCTIØN RESPØNSE "FLOW" LOGIC DIAGRAM

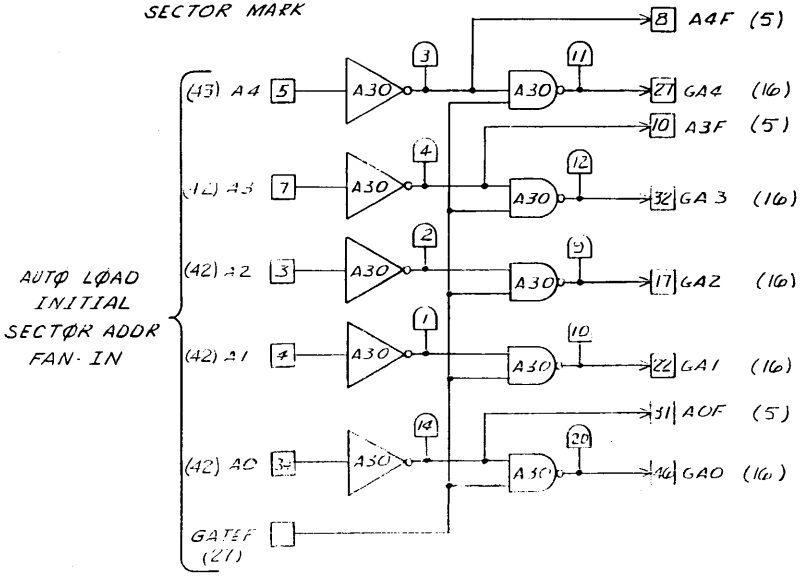
CODE IDENT NO.	DRAWING NUMBER	REV
C 09132	39745600	B

SHEET 7 OF

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD





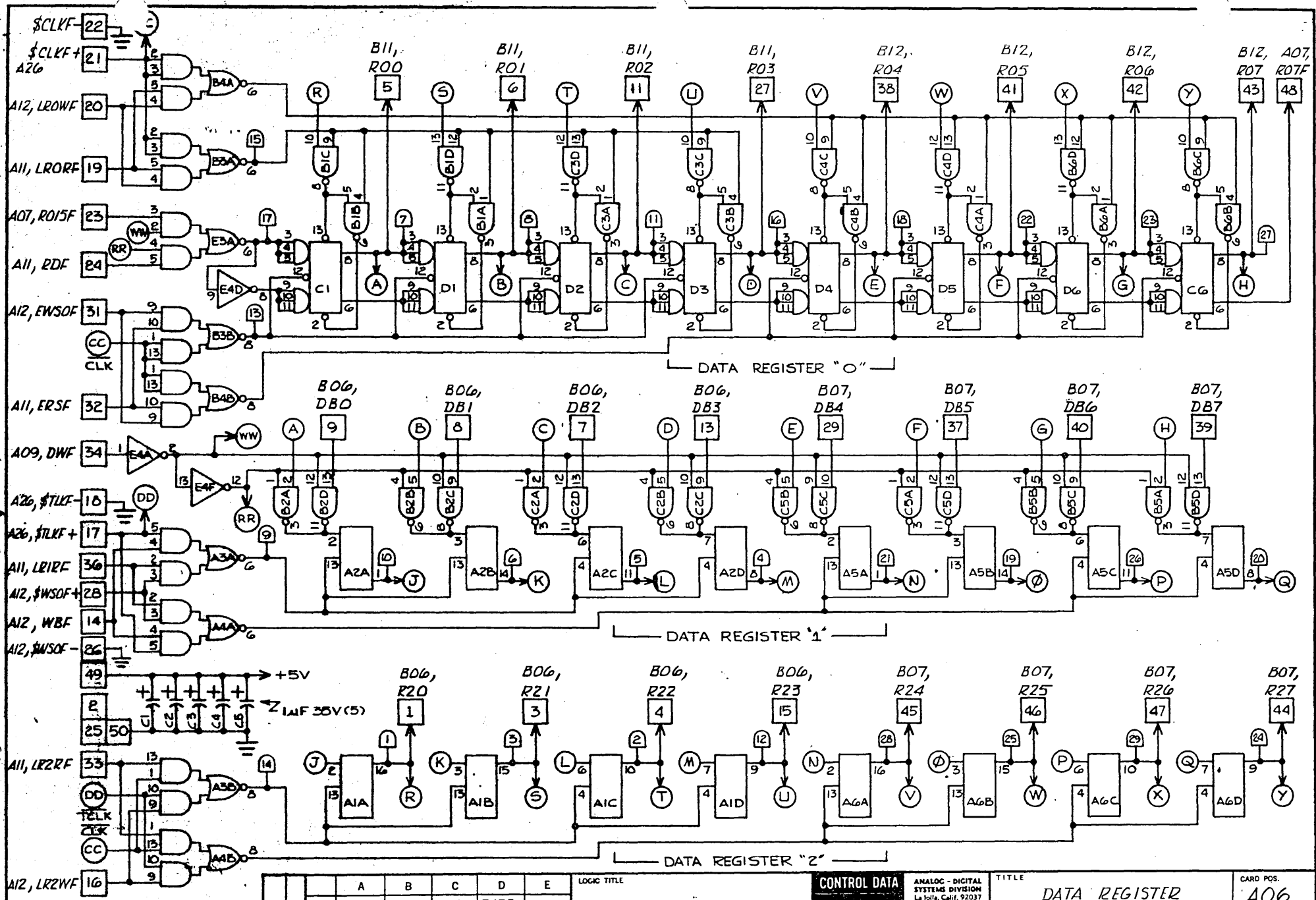


REFERENCE DRAWINGS	CONTROL DATA CORPORATION — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037	TITLE
COMPONENTS, EXCEPT AS NOTED	FIRST USED ON	DRUM CONTROLLER "FLOW" LOGIC DIAGRAM
TOLERANCE / VALUE / RATING	DR	
RES	CHK	
CAP.	ENGR	
	MFG	
	APPD	

SIZE	CODE IDENT NO.	DRAWING NUMBER	REV
C	09132	39745600	

SHEET 8 OF

3 2 1



	A	B	C	D	E
1	7475	7400	7472	7472	
2	7475	849	849	7472	
3	7450	7450	7400	7472	7450
4	7450	7450	7400	7472	7404
5	7475	849	849	7472	
6	7475	7400	7472	7472	

DR 39705800
DETACHED LISTS

1. E3B, E4B, E4C, & E4E ARE NOT USED.

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: DATA REGISTER

LOGIC DWG. NO.: 39705800 REV. A

PWA NO.: 39705700 PWB NO.: 39705600

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	B. HOELSCHER	3-29-71
CHK	R. Faye	4-2-71
ENGR		
MFG		
APPD		

TITLE: DATA REGISTER BITS 0-7

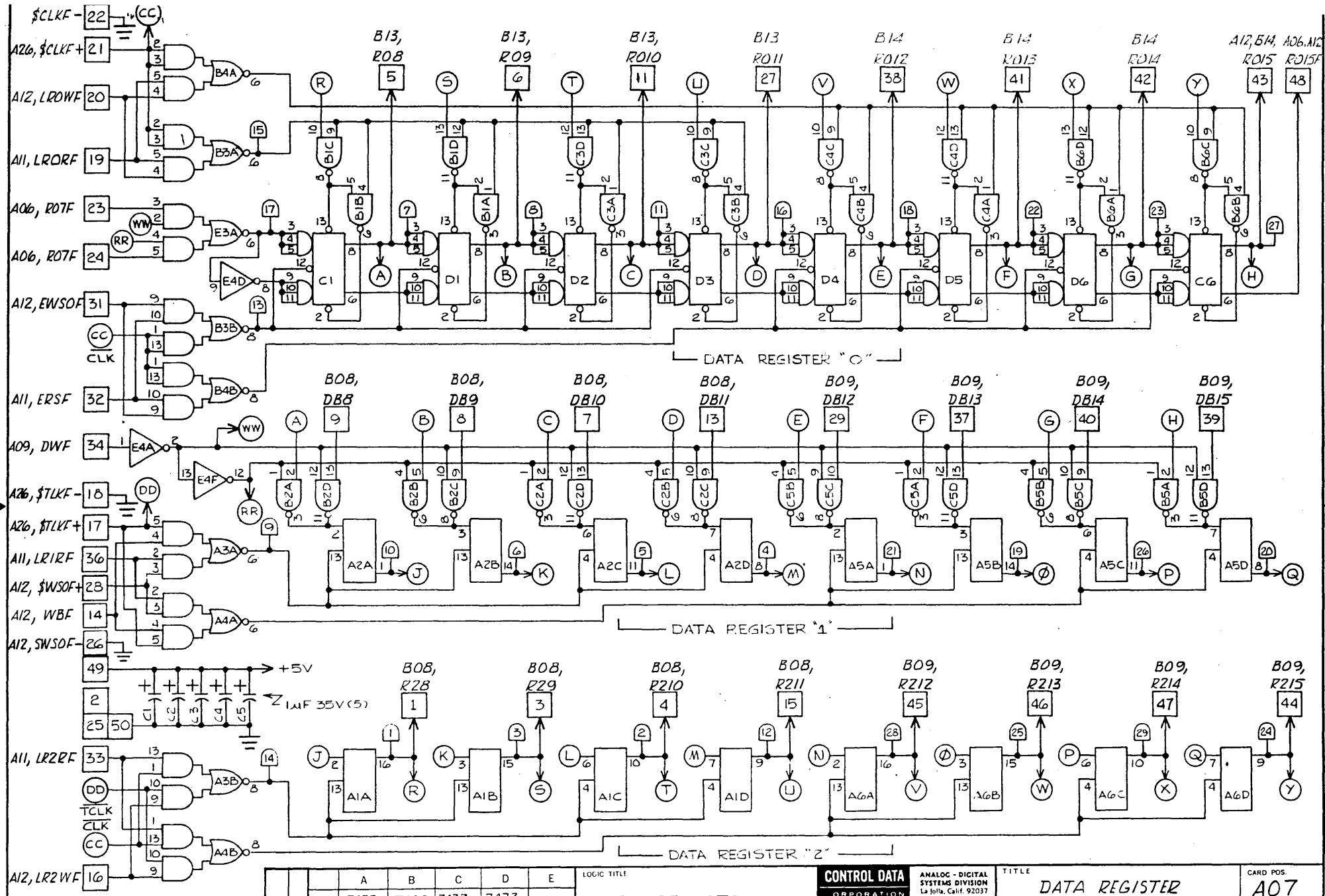
CARD POS.: A06

LOGIC TYPE: ILCT

CODE IDENT NO.: C 09132

DRAWING NUMBER: 39745600 REV D

SHEET 9 OF



	A	B	C	D	E
1	7475	7400	7472	7472	
2	7475	849	849	7472	
3	7450	7450	7400	7472	7450
4	7450	7450	7400	7472	7404
5	7475	849	849	7472	
6	7475	7400	7472	7472	

DR 39705800 DETACHED LISTS

1. E3B, E4B, E4C, & E4E ARE NOT USED.

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: DATA REGISTER

LOGIC DWG. NO. 39705800 REV A

PWA NO 39705700 PWB NO. 39705600

CONTROL DATA ORPORATION — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

DON		
	Shreckhise	3-29-71
CK	C. Page	4-2-71
GR		
FG		
PD		

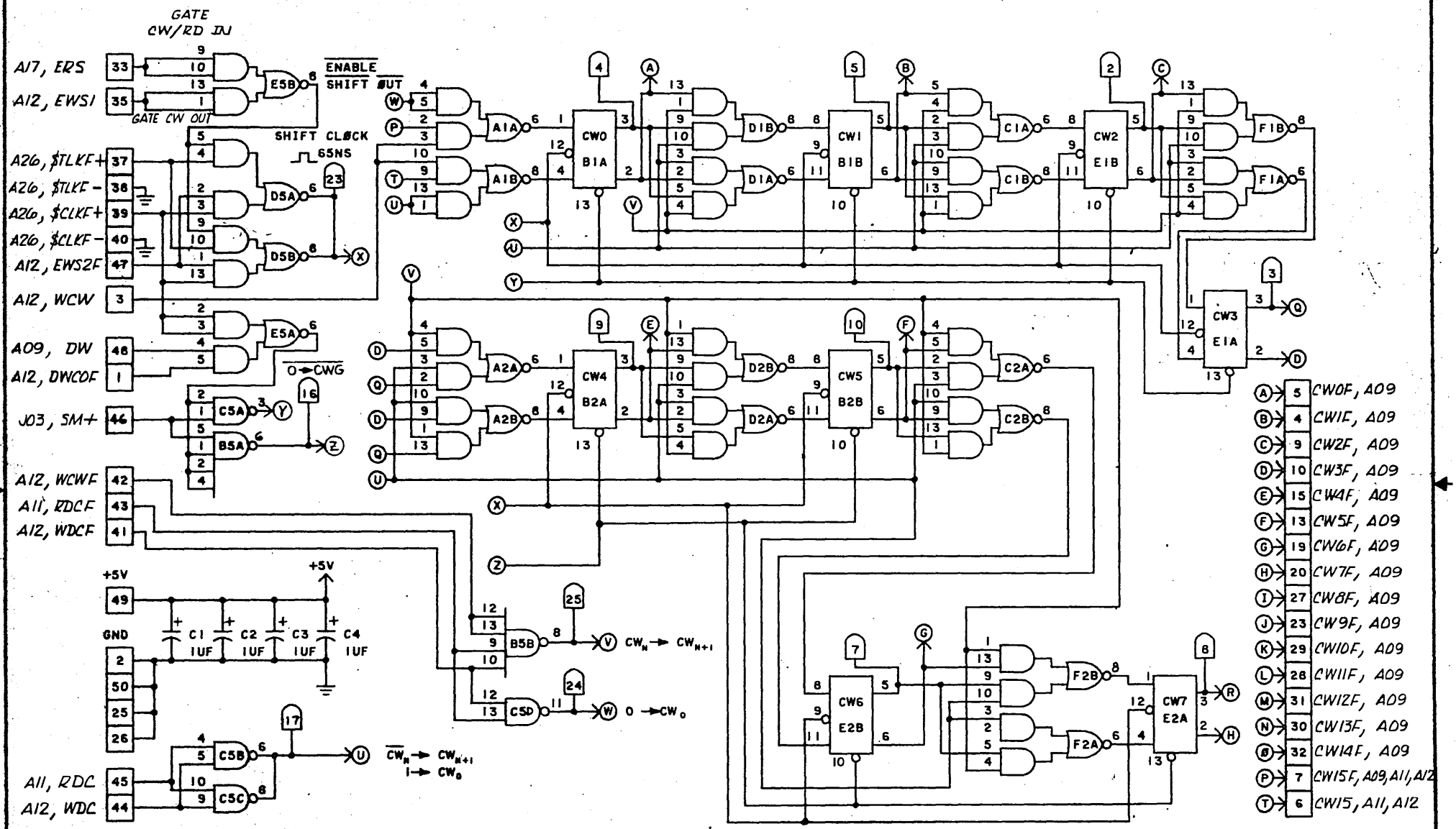
TITLE: DATA REGISTER BITS 8-15

CARD POS. A07

LOGIC TYPE ILCT

C | CODE IDENT NO. 09132 | DRAWING NUMBER 39745600 | REV D

SHEET 10 OF



SHEET 1 OF 2

	A	B	C	D	E	F
1	7450	74107	7450	7450	74107	7450
2	7450	74107	7450	7450	74107	7450
3	7450	74107	7450	7450	74107	7450
4	7450	74107	7450	7450	74107	7450
5		7440	7400	7450	7450	
6						

DR 39705500 DETACHED LIST

1. ALL GATES ARE USED.

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: CHECKWORD GENERATOR

LOGIC DWG. NO.: 39705500 REV.: A

PWA NO.: 39705400 PWB NO.: 39705300

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

FIRST USED ON	B6504-A
DR	6/11/71
CHK	6-14-71
ENGR	
MFG	
APPD	

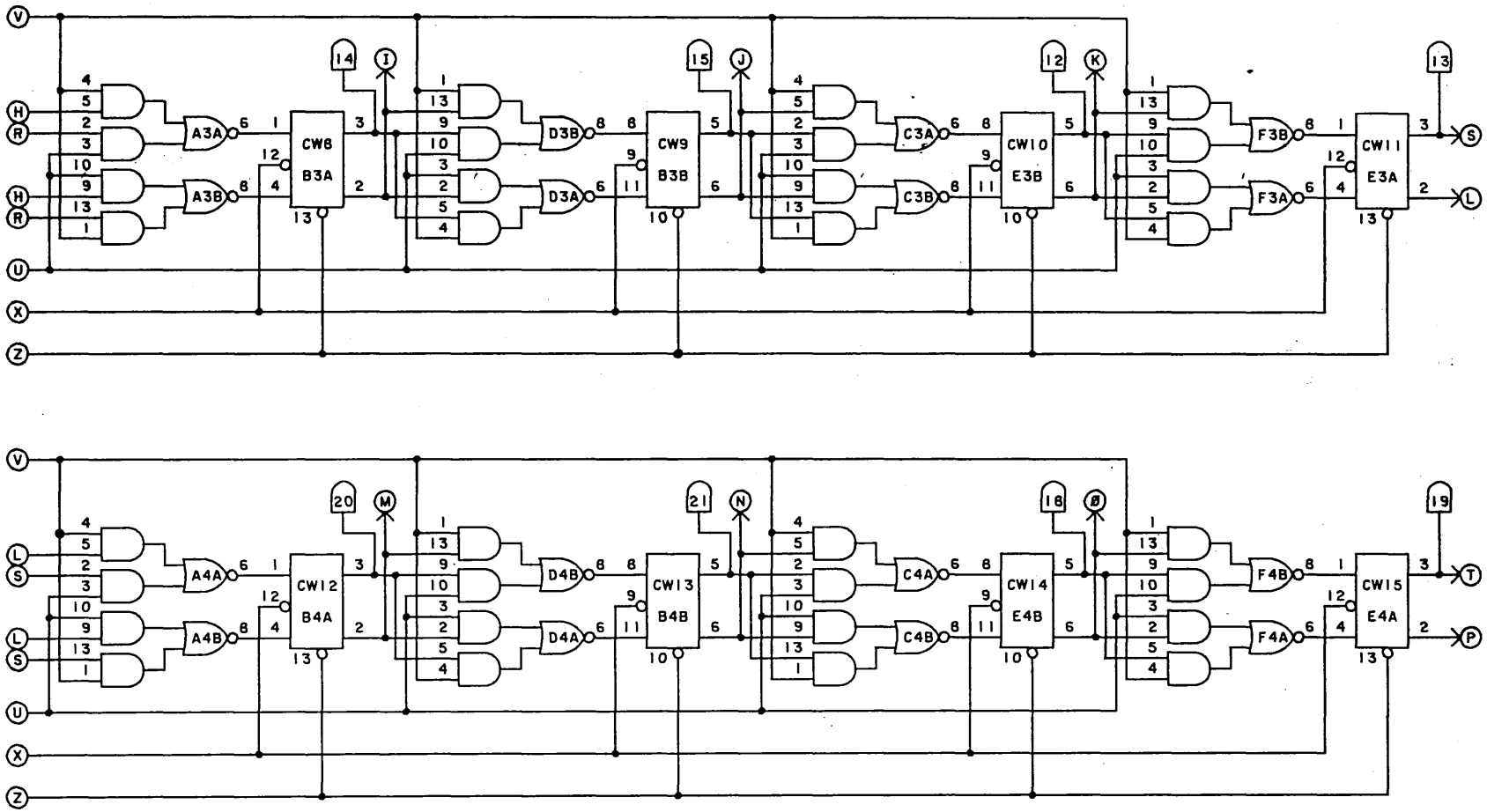
TITLE: CHECKWORD GENERATOR

CARD POS.: A08

LOGIC TYPE: 1LBT

C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600

SHEET 11 OF



SHEET 2 OF 2

	A	B	C	D	E
1					
2					
3					
4					
5					
6					

LOGIC TITLE: CHECKWORD GENERATOR

LOGIC DWG. NO.: 39705500 REV.: A

PWA NO. | PWB NO.

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR		
CHK		
ENGR		
MFG		
APPD		

TITLE: CHECKWORD GENERATOR

CARD POS.: A08

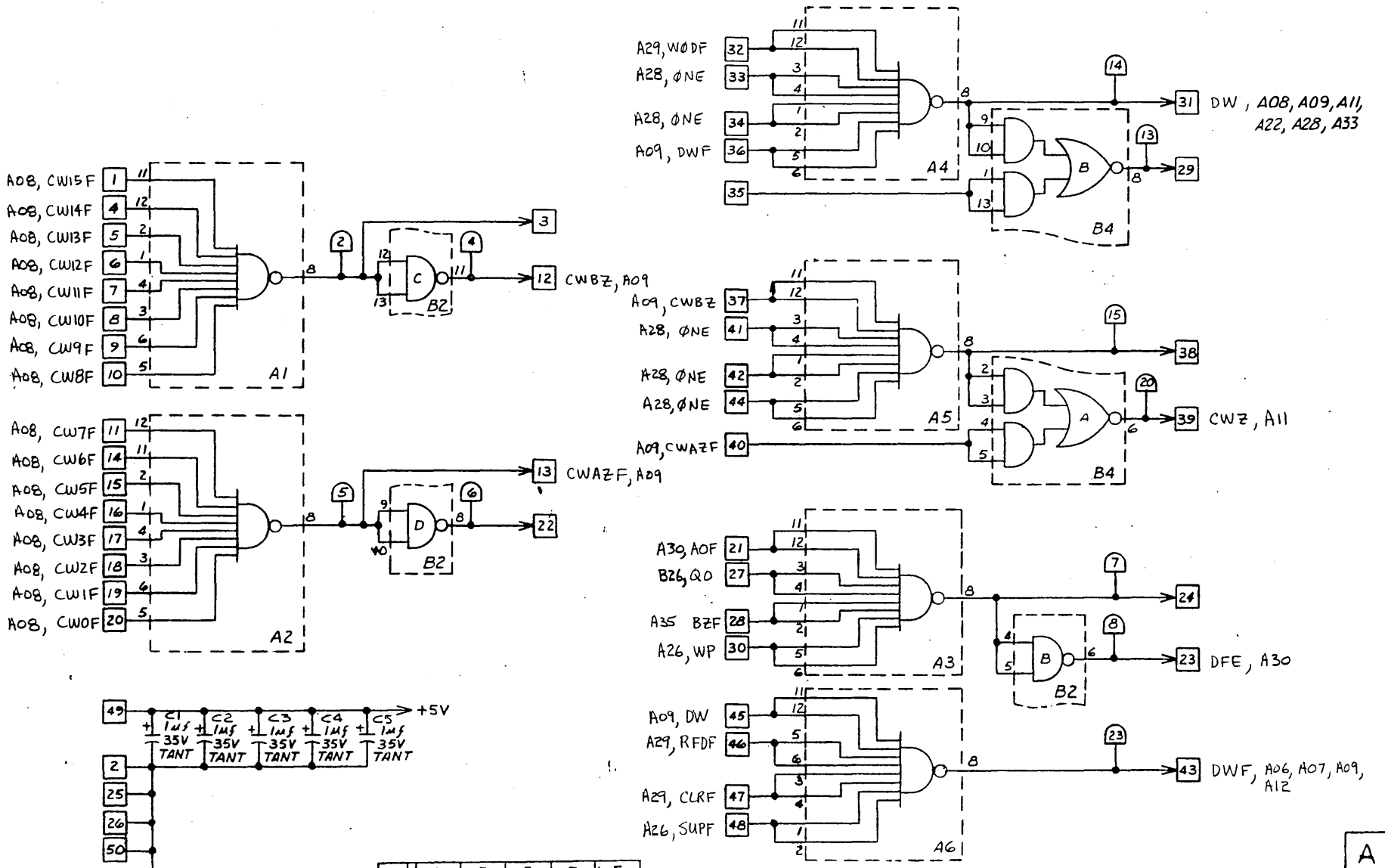
LOGIC TYPE: 1LBT

C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600

SHEET 12 OF

NOTES: UNLESS OTHERWISE SPECIFIED

REVISION RECORD					
REV	ECO	DESCRIPTION	DR	DATE	CHK	APPD



2. ALL CHIPS – PIN 7 IS GRD, PIN 14 IS Vcc.
1. B2A NOT USED.

NOTE: UNLESS OTHERWISE SPECIFIED,

	A	B	C	D	E
1	SN7454				
2	SN7430	SN7400			
3	SN7430				
4	SN7430	SN7450			
5	SN7402				
6	SN745				

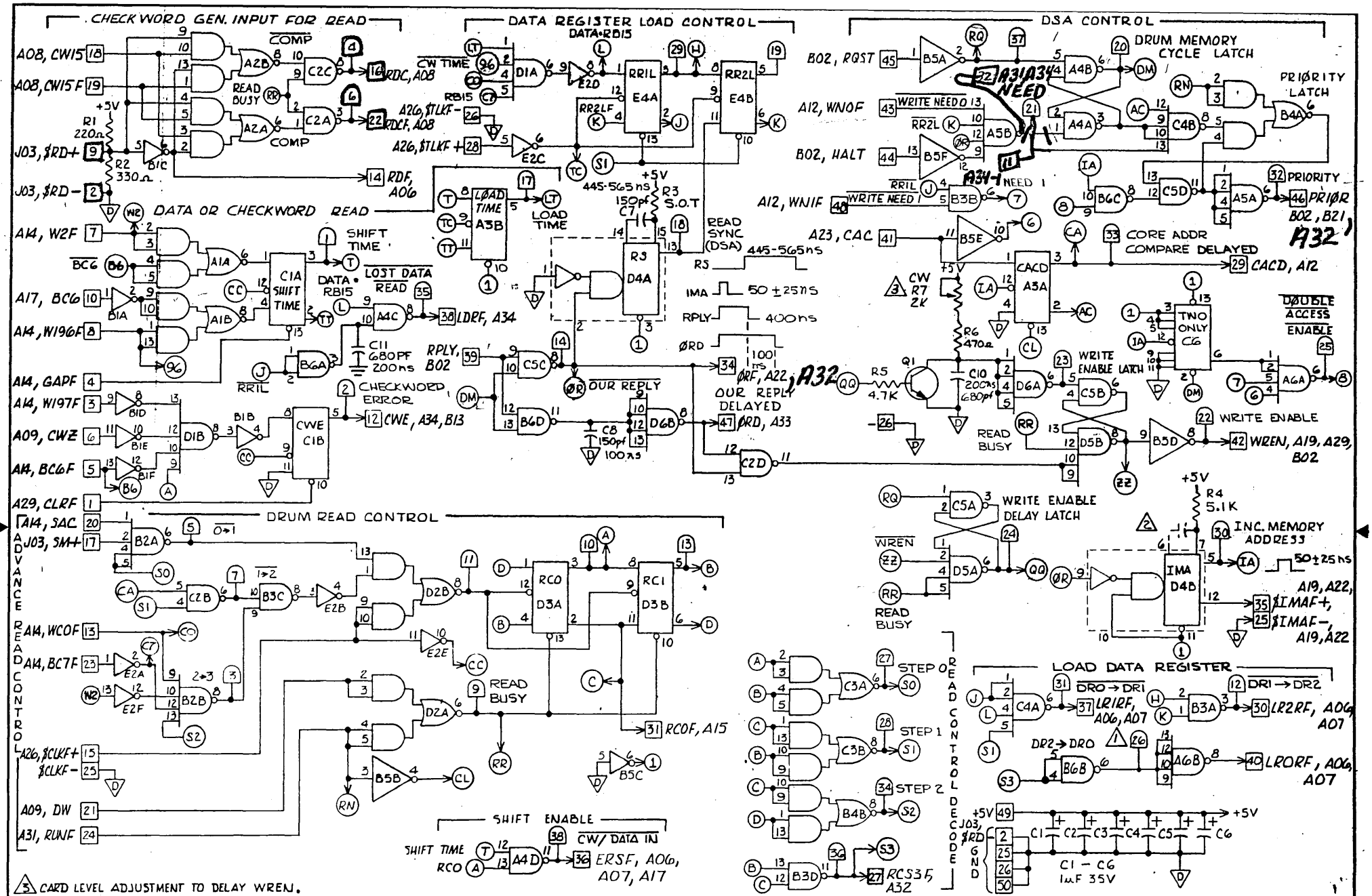
CARD TYPE	CARD TITLE
9GJT	TTL GATE – HIGH FAN IN
PRODUCT	CARD DWG NO	REV.
1500	39234600	

CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE	CARD POS.
TTL GATE -HIGH FAN IN	A6;9

MODEL	DWG. NO.	REV.	SHEET	PAGE
	39234600	B	13	

A



	A	B	C	D	E
1	7450	7404	74107	7440	
2	7450	7440	7400	7450	7404
3	74107	7400	7450	74107	
4	7400	7450	7440	74123	74107
5	7440	7404	7400	7440	
6	7440	849	7472	7413	

LOGIC TITLE: DRUM READ/DSA CONTROL

LOGIC DWG. NO.: 39706100 REV. C

PWA NO.: 39706[illegible] PWB NO.: 39705900

CONTROL DATA CORPORATION — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

FIRST USED ON	BG504-A	
DR	B. Roberts	5-6-71
CHK	[illegible]	5-7-71
ENGR	[illegible]	7-1-71
MFG		
APPD	[illegible]	7-9-71
	[illegible]	7-1-71

TITLE: DRUM READ / DSA CONTROL

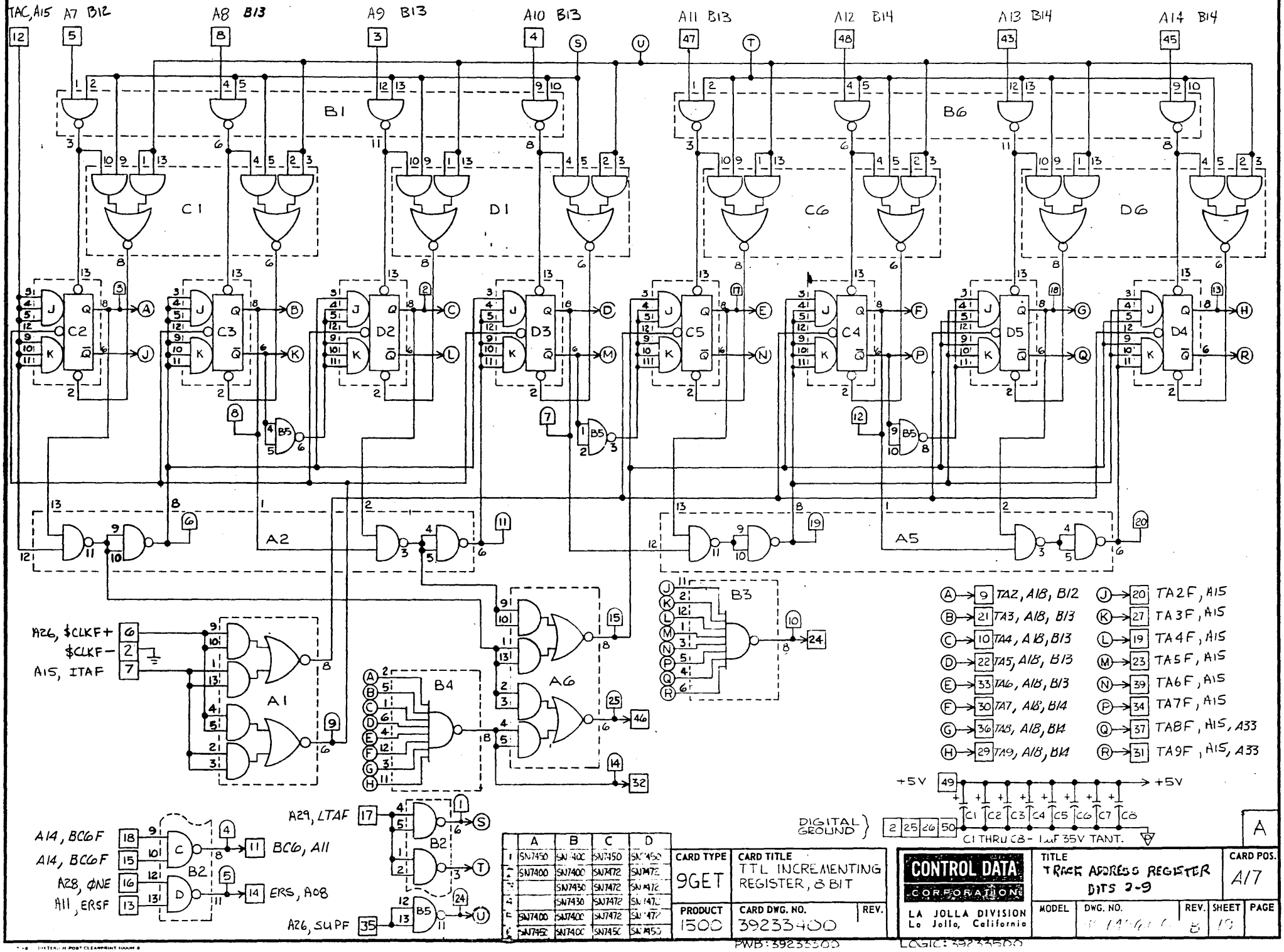
CARD POS.: A11

LOGIC TYPE: 1LDT

CODE IDENT NO.: C 09132

DRAWING NUMBER: 39745600 REV F

SHEET 14 OF



	A	B	C	D
1	SN7450	SN7400	SN7450	SN7450
2	SN7400	SN7400	SN7472	SN7472
3		SN7430	SN7472	SN7472
4		SN7430	SN7472	SN7472
5	SN7400	SN7400	SN7472	SN7472
6	SN7452	SN7400	SN7450	SN7450

CARD TYPE	CARD TITLE
9GET	TTL INCREMENTING REGISTER, 8 BIT
PRODUCT	CARD DWG. NO. / REV.
1500	39233400

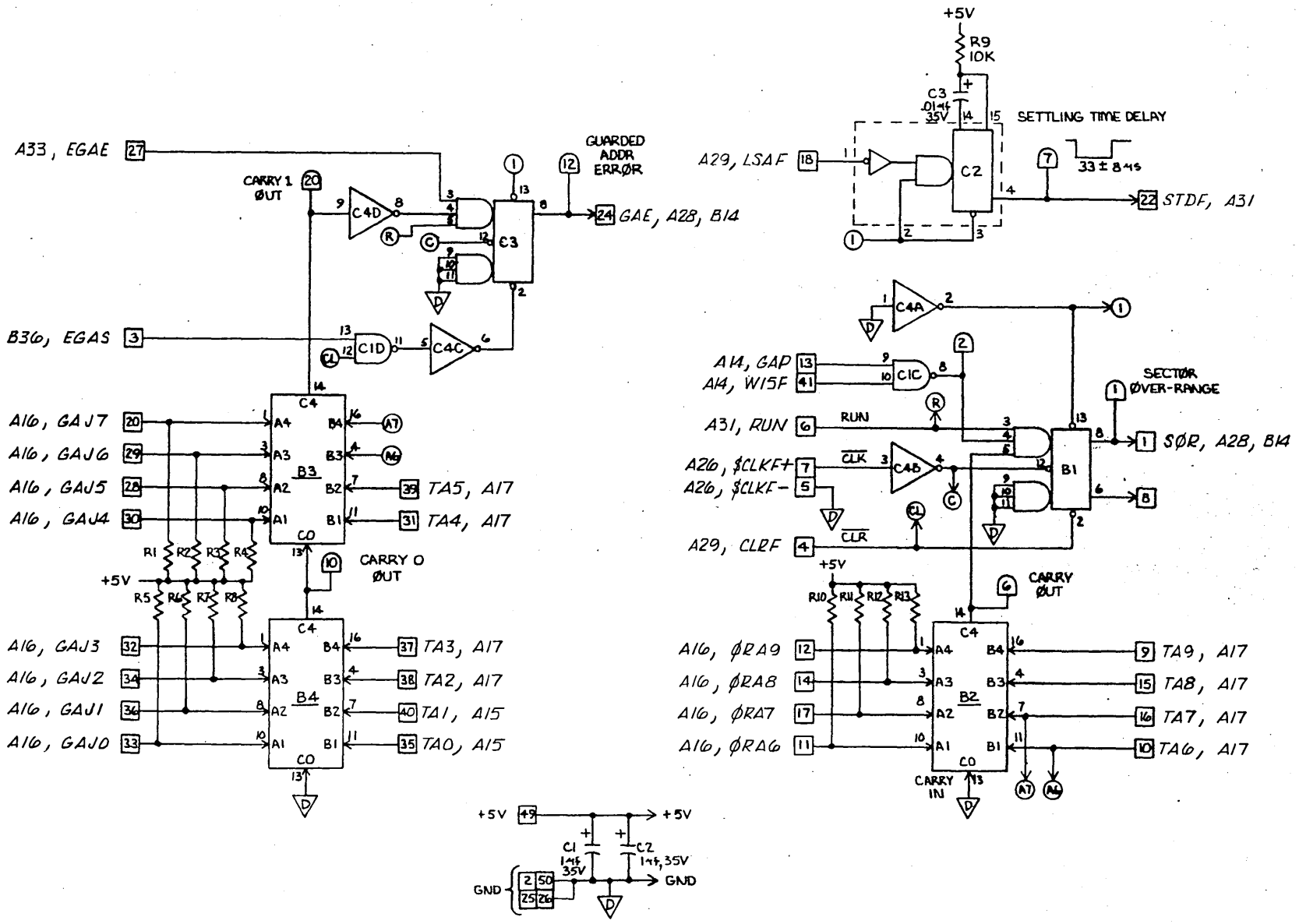
PWB: 39233500 LOGIC: 39233600

CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE: TRACK ADDRESS REGISTER BITS 2-9

CARD POS. A17

MODEL	DWG. NO.	REV.	SHEET	PAGE
		B	13	



2. RESISTORS ARE C.C. 1/4W, 2.4K.
1. C1A, C1B, C2B, C4E, C4F NOT USED.

NOTES: UNLESS OTHERWISE SPECIFIED

DR 39715400 DETACHED LIST

	A	B	C	D	E
1		7472	7400		
2		7483	74123		
3		7483	7472		
4		7483	7404		
5					
6					

LOGIC TITLE: GUARDED ADDR/ ØVER-RANGE ERROR DETECT

LOGIC DWG. NO.: 39715400 REV.: A

PWA NO.: 39715300 PWB NO.: 39715200

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON	BG504-A	
DR		6/25/71
CHK		6-30-71
ENGR		
MFG		
APPD		

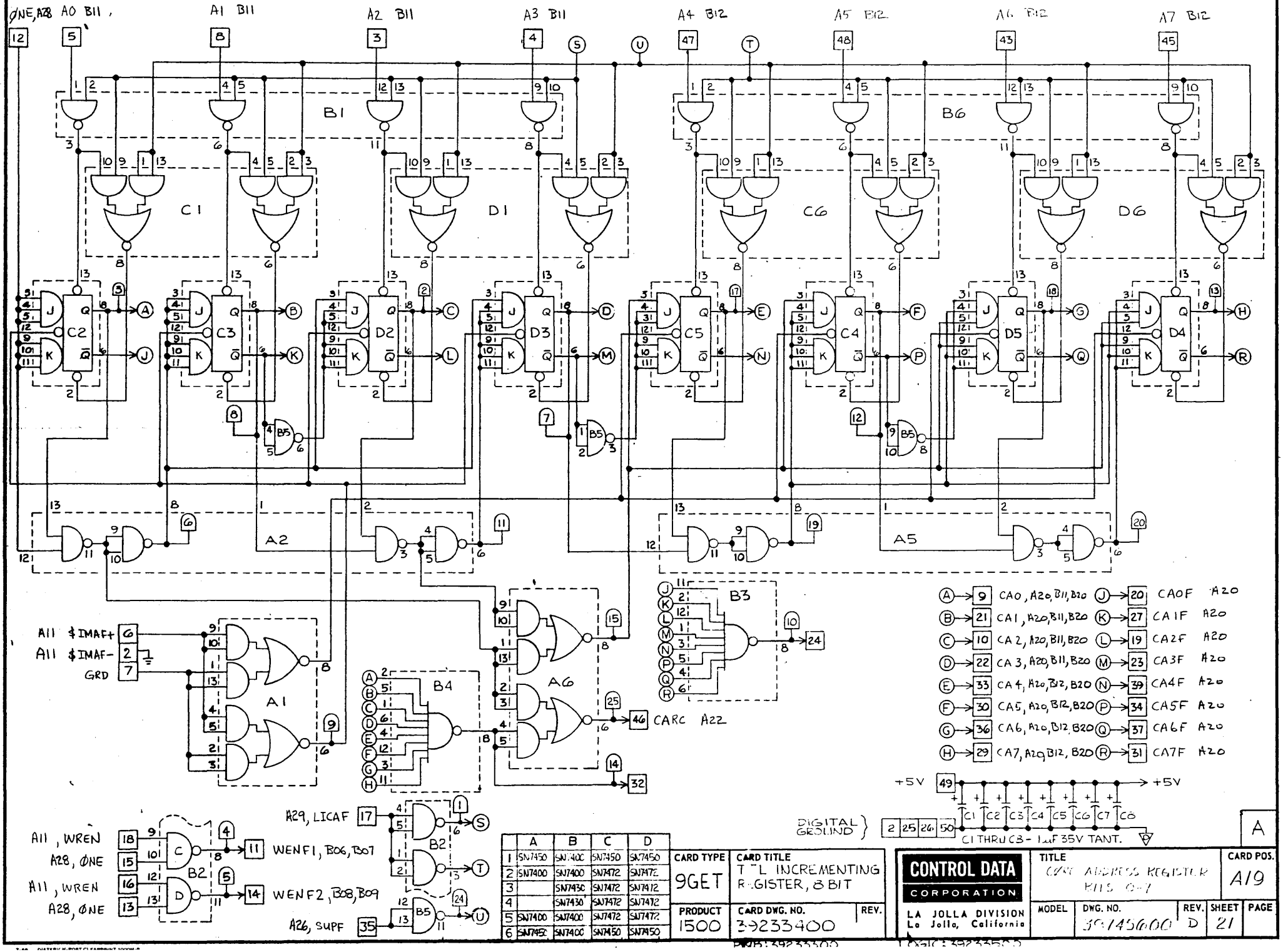
TITLE: GUARDED ADDR/OVER-RANGE ERROR DETECT

CARD POS.: A18

LOGIC TYPE: IM13T

C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600 | REV: B

SHEET 20 OF



	A	B	C	D
1	SN7450	SN7400	SN7450	SN7450
2	SN7400	SN7400	SN7472	SN7472
3		SN7430	SN7472	SN7472
4		SN7430	SN7472	SN7472
5	SN7400	SN7400	SN7472	SN7472
6	SN7452	SN7400	SN7450	SN7450

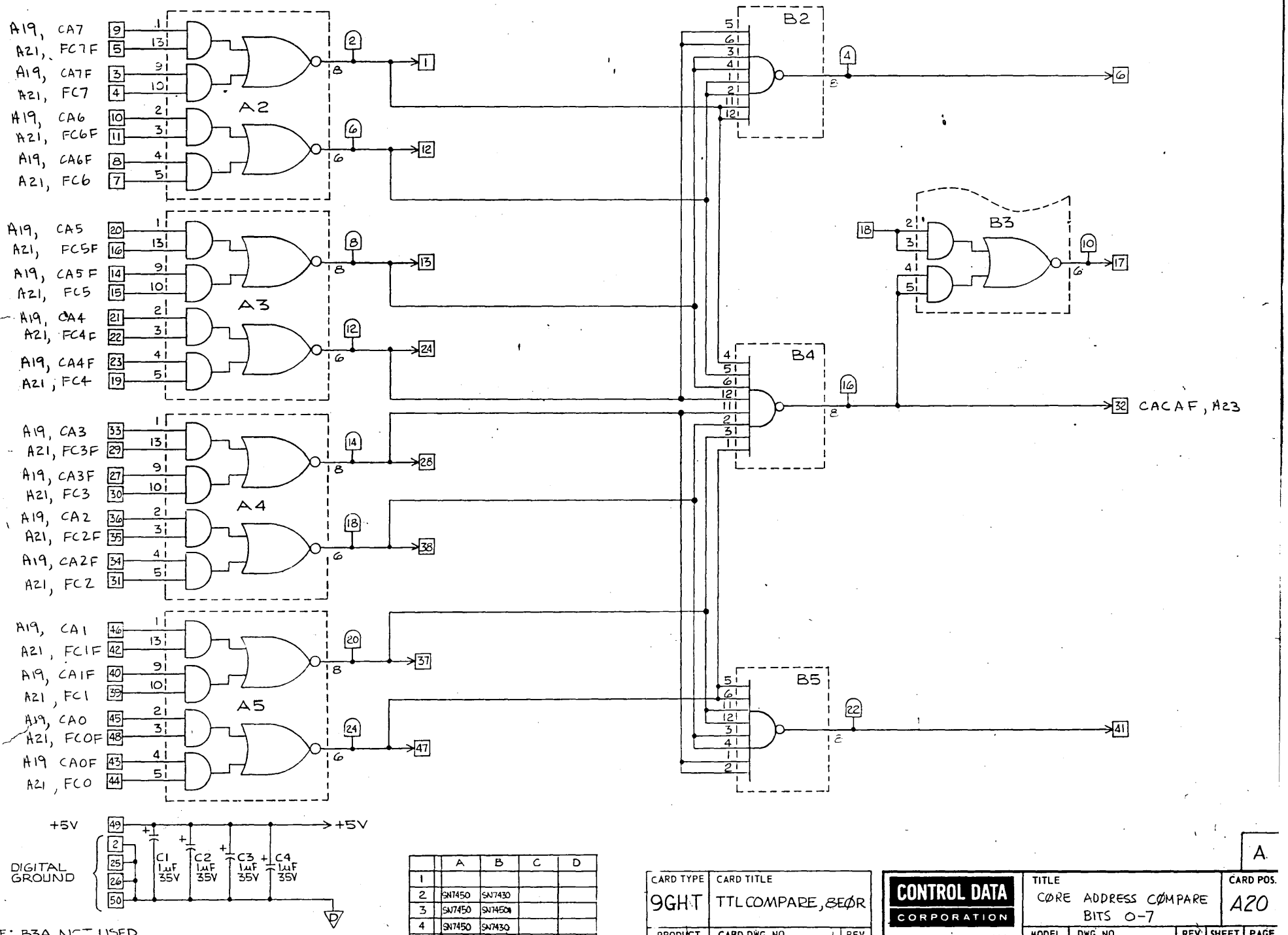
CARD TYPE	CARD TITLE		
9GET	T²L INCREMENTING REGISTER, 8 BIT		
PRODUCT	CARD DWG. NO.	REV.	
1500	3923400		

CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE	CARD POS.
CPU ADDRESS REGISTER BITS 0-7	A19

MODEL	DWG. NO.	REV.	SHEET	PAGE
	39145600	D	21	

A



NOTE: B3A NOT USED

ALL CHIPS - 14 Vcc, PIN 7 GRD.

	A	B	C	D
1				
2	SN7450	SN7430		
3	SN7450	SN7450		
4	SN7450	SN7430		
5	SN7450	SN7430		
6				

CARD TYPE	CARD TITLE	
9GHT	TTL COMPARE, 8EØR	
PRODUCT	CARD DWG. NO.	REV.
1500	39234300	

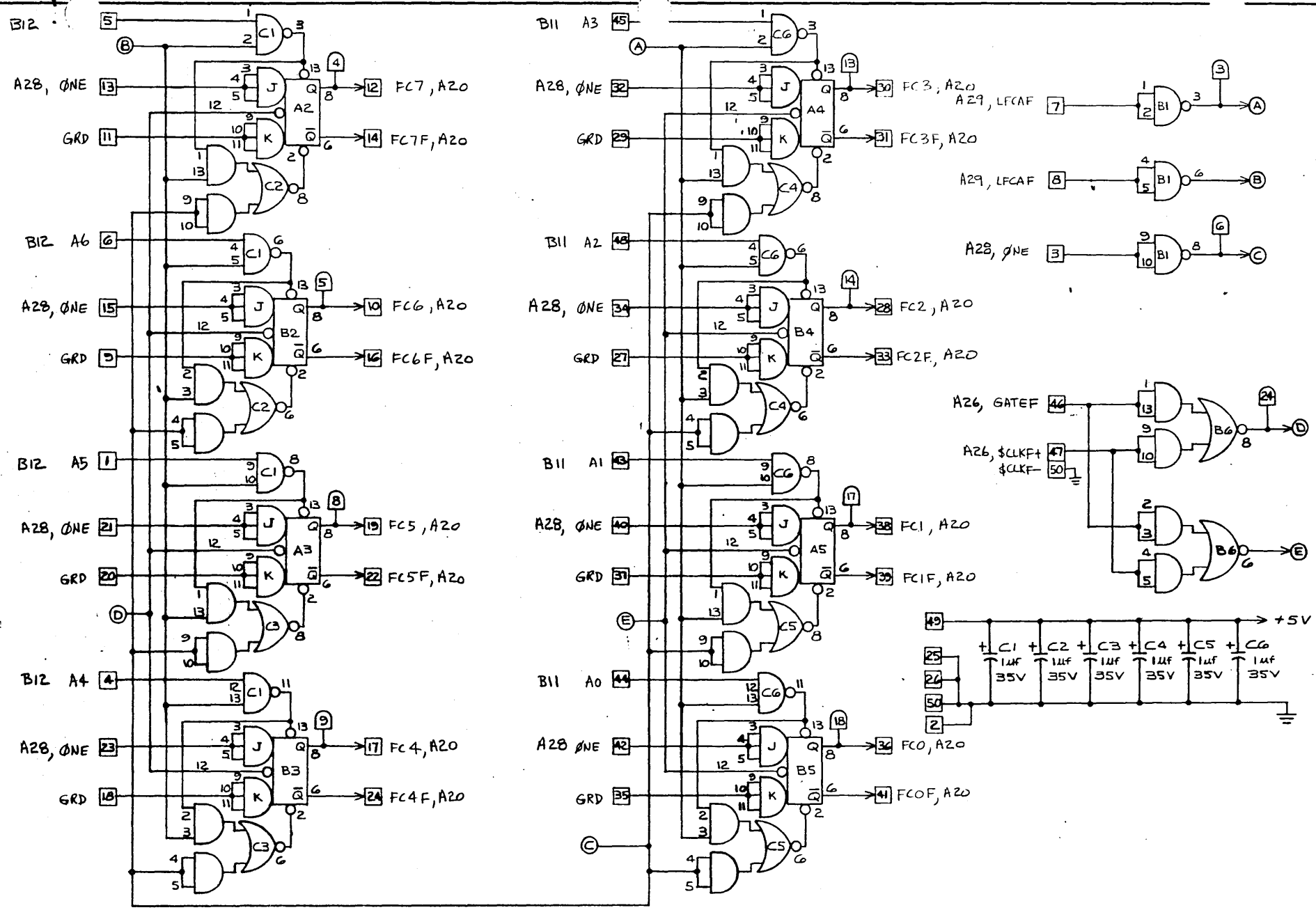
CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE	CARD POS.
CØRE ADDRESS CØMPARE BITS 0-7	A20

MODEL	DWG. NO.	REV.	SHEET	PAGE
	397456	A	22	

A

PWB 39234200 LOGIC 39234400



	A	B	C	D	E
1		SN7400	SN7400		
2	SN7472	SN7472	SN7450		
3	SN7472	SN7472	SN7450		
4	SN7472	SN7472	SN7450		
5	SN7472	SN7472	SN7450		
6		SN7450	SN7400		

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: TTL COUNTER/ REGISTER, 8 BIT

LOGIC DWG. NO.: 39233800 REV. A

PWA NO.: 39233700 PWB NO.: 39233600

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	D. HOSAKA	1-23-70
CHK	Guy B. Bibb	3-10-70
ENGR	[illegible]	3-16-70
MFG		
APPD	[illegible]	3-18-70
	[illegible]	3-17-70

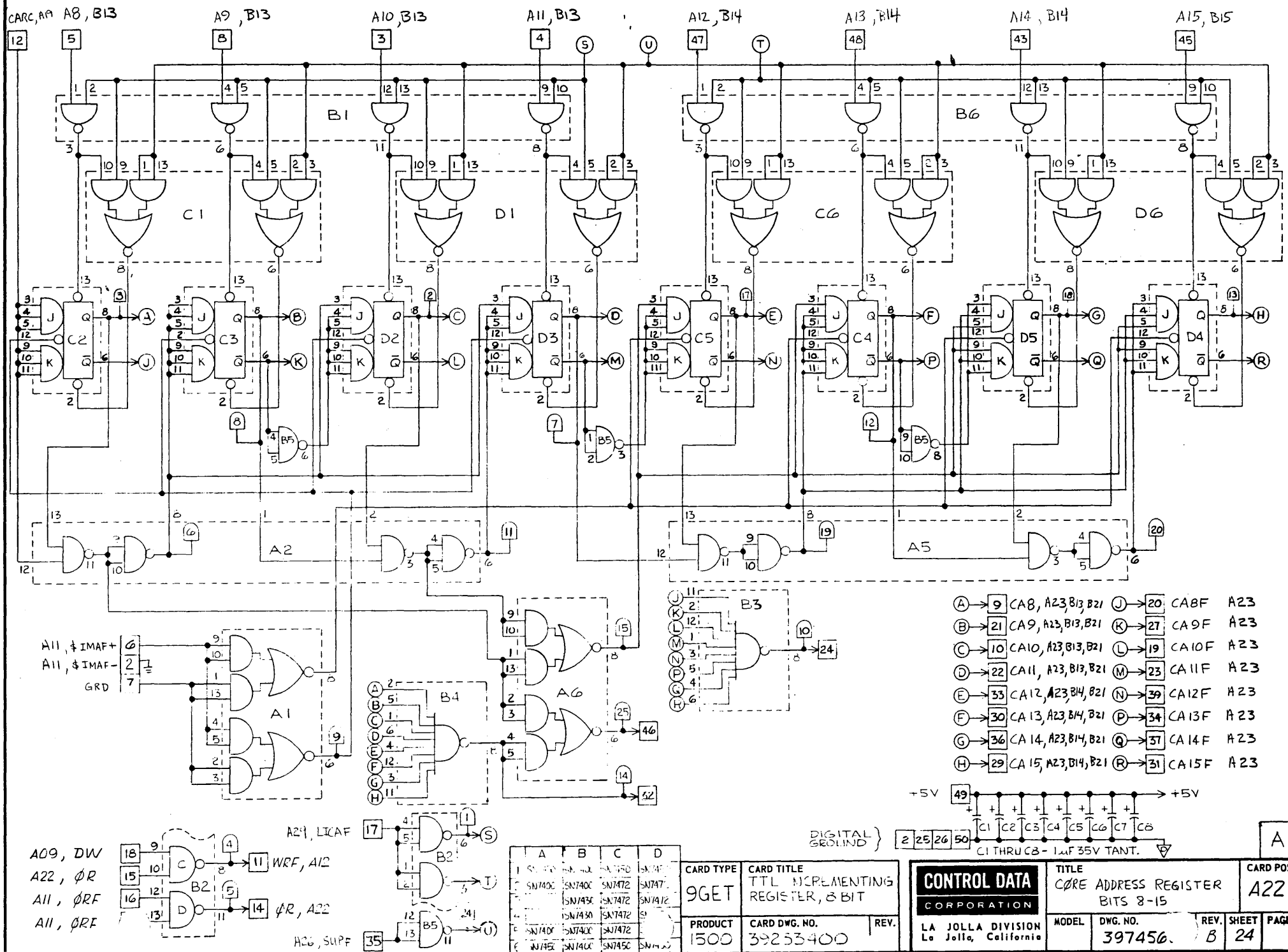
TITLE: FINAL CORE ADDRESS REGISTER BITS 0-7

CARD POS.: A21

LOGIC TYPE: 9GFT

C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600

SHEET 23 OF



A	B	C	D
SN7400	SN7400	SN7472	SN7472
	SN7430	SN7472	SN7472
SN7400	SN7400	SN7472	
SN7450	SN7400	SN7450	

CARD TYPE	CARD TITLE
9GET	TTL INCREMENTING REGISTER, 8 BIT
PRODUCT 1500	CARD DWG. NO. 39253400 REV.

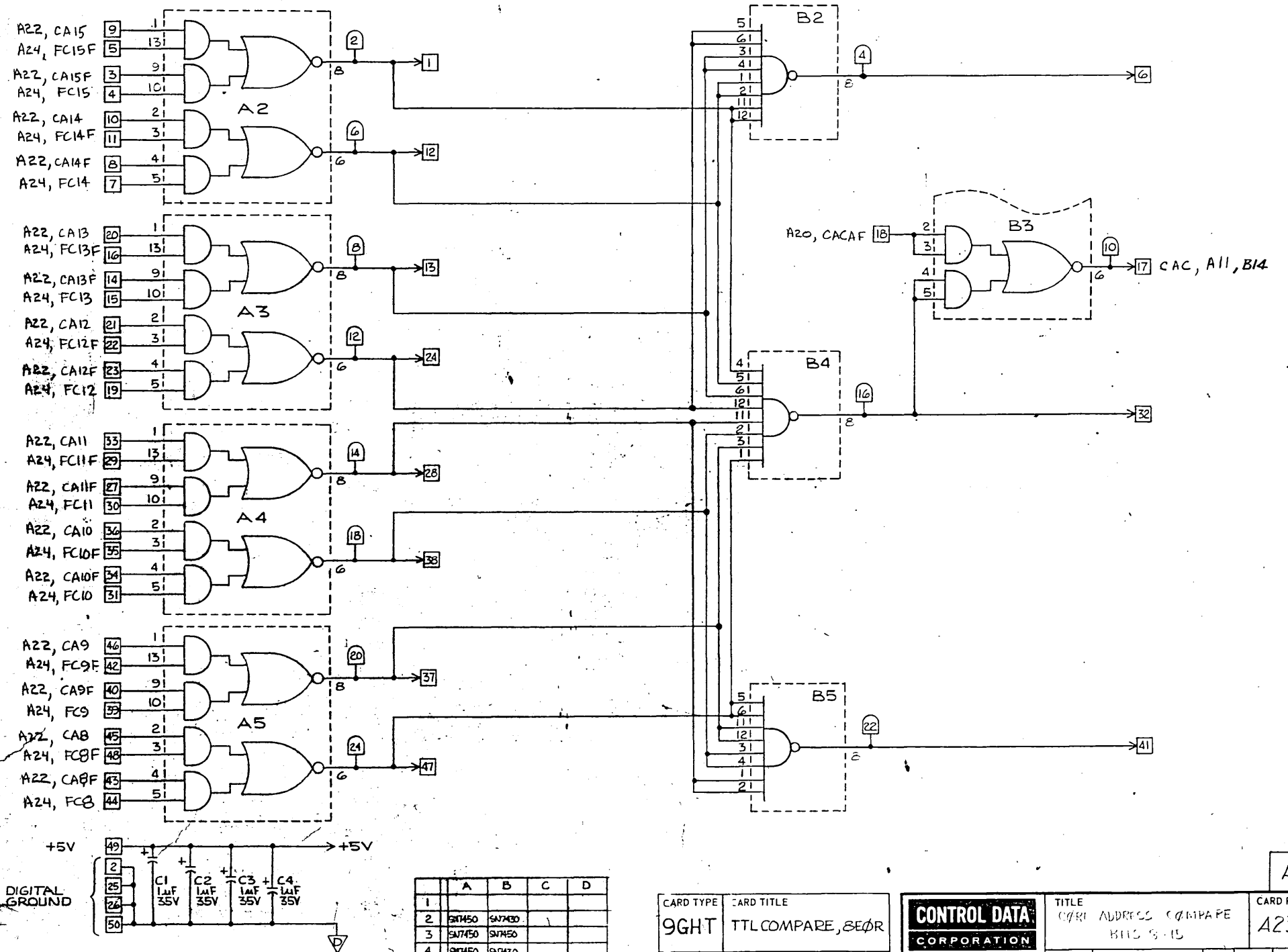
CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE: CORE ADDRESS REGISTER BITS 8-15

CARD POS. A22

MODEL	DWG. NO.	REV.	SHEET	PAGE
	397456	B	24	

SOURCE: 39253400
LOGIC: 39253500



NOTE: B3A NOT USED

ALL CHIPS - PIN 14 Vcc, PIN 7 GRD.

	A	B	C	D
1				
2	SN7450	SN7430		
3	SN7450	SN7450		
4	SN7450	SN7430		
5	SN7450	SN7430		
6				

CARD TYPE	CARD TITLE
9GHT	TTL COMPARE, BE0R
PRODUCT	CARD DWG. NO. / REV.
1500	39234300

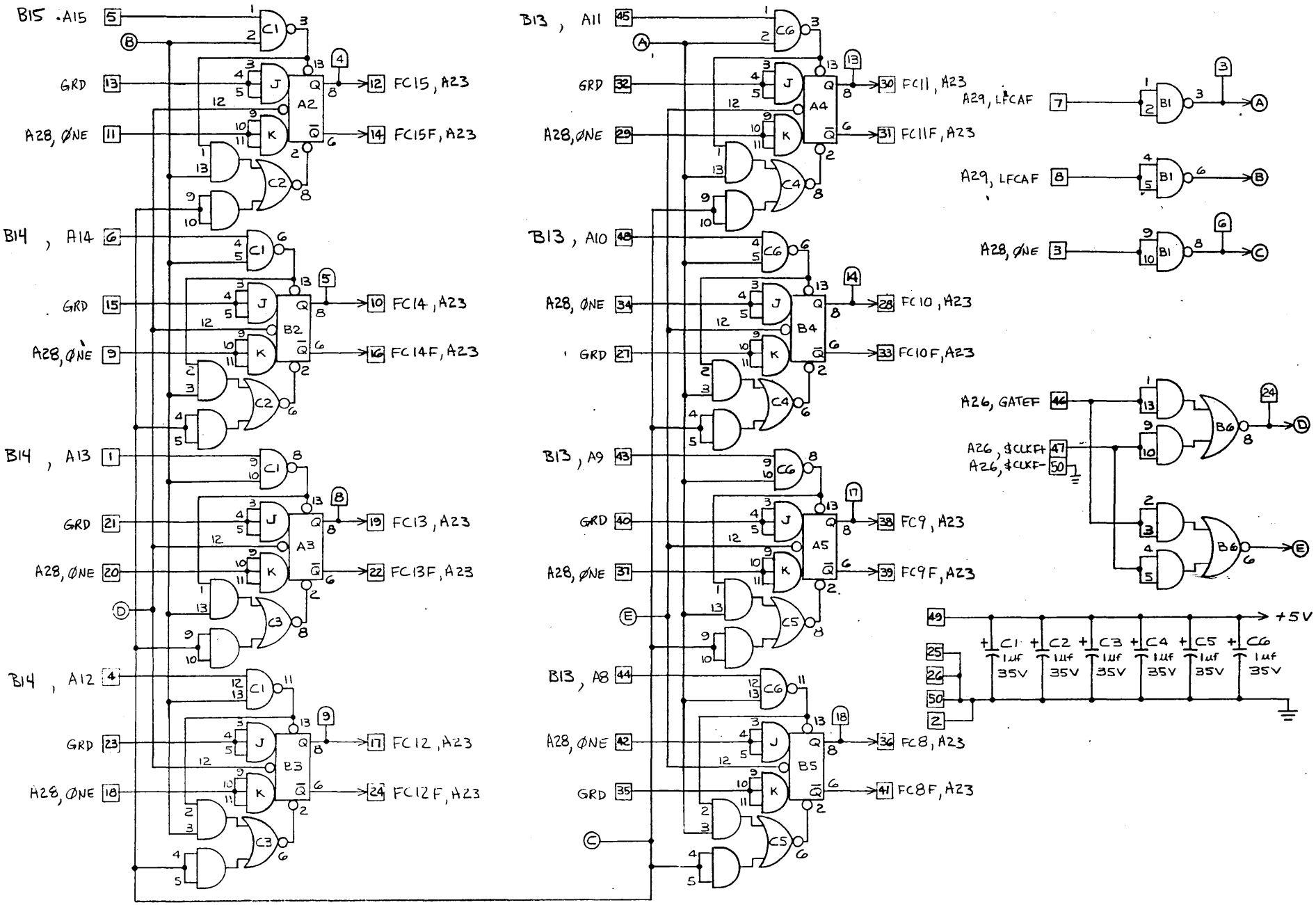
CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE: CYBER ADDRESS COMPARE BITS 5-15

CARD POS. A23

MODEL	DWG. NO.	REV.	SHEET	PAGE
	39234600	B	25	

A



	A	B	C	D	E
1		SN7400	SN7400		
2	SN7472	SN7472	SN7450		
3	SN7472	SN7472	SN7450		
4	SN7472	SN7472	SN7450		
5	SN7472	SN7472	SN7450		
6		SN7450	SN7400		

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: TTL COUNTER/ REGISTER, 8 BIT

LOGIC DWG. NO.: 39233300 REV. A

PWA NO.: 39233700 PWB NO.: 39233600

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	D. HOSAKA	1-23-70
CHK	Guy B. Brito	3-10-70
ENGR		3-16-70
MFG		
APPD	E. [illegible]	3-18-70
	a. Wer	3-17-70

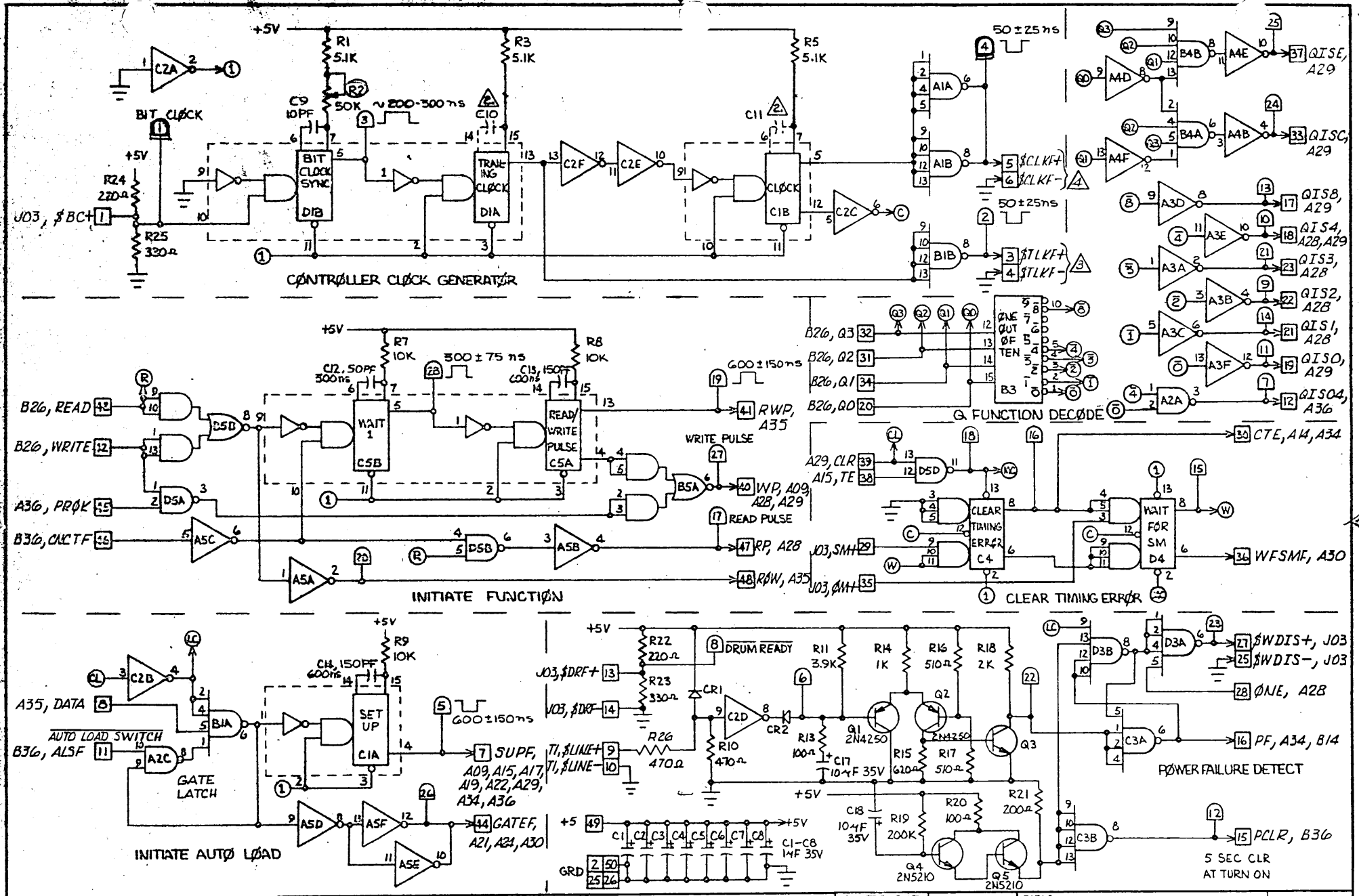
TITLE: FINAL CORE ADDRESS REGISTER BITS 8-15

CARD POS.: A24

LOGIC TYPE: 9GFT

C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600

SHEET 26 OF



4. A06, A07, A08, A11, A12, A14, A15, A17, A21, A24, A26, A32, A34.

3. A06, A07, A08, A11.

2. PROVISION FOR CAPACITOR ON PWB.

1. A2B, A2D, A4A, A4C, D5C ARE NOT USED

NOTES: UNLESS OTHERWISE SPECIFIED

DR 39708400 DETACHED LISTS

	A	B	C	D	E
1	7440	7440	74123	74123	
2	7400		7404		
3	7404	7447	7413	7440	
4	7404	7440	7472	7472	
5	7404	7450	74123	7400	
6					

LOGIC TITLE: CONTROLLER CLOCK

LOGIC DWG. NO.: 39708400 REV. B

PWA NO.: 39708300 PWB NO.: 39708200

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

FIRST USED ON	BG504-A	
DR		4/26/71
CHK		5-7-71
ENGR		
MFG		
APPD		

TITLE: CONTROLLER CLOCK

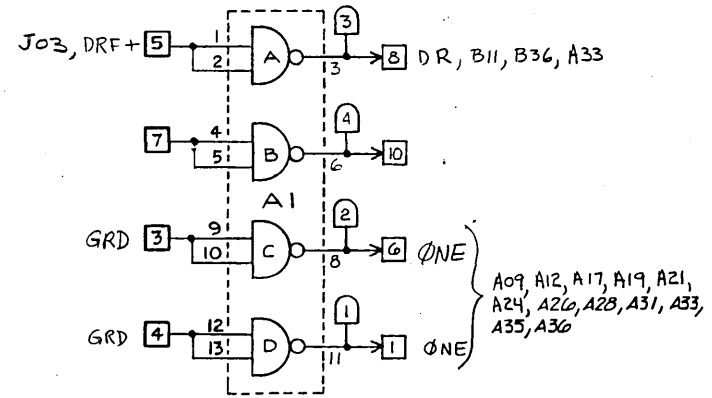
CARD POS.: A26

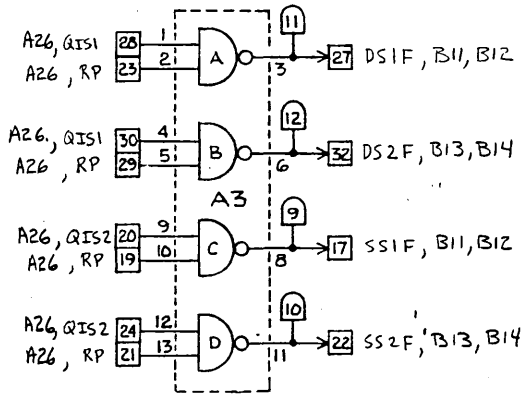
LOGIC TYPE: 1LGT

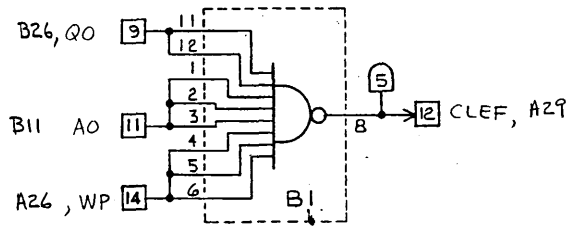
C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600 | REV: E

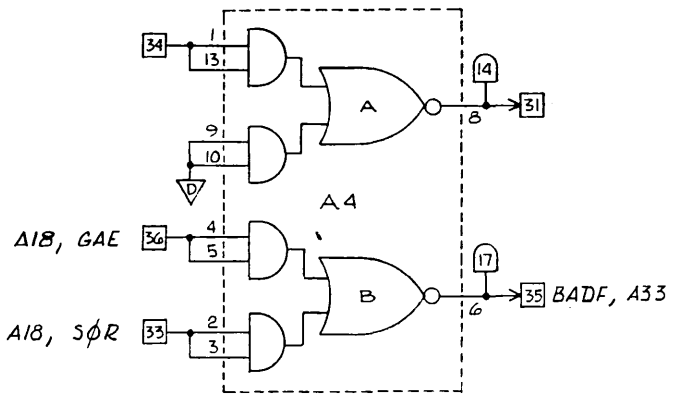
SHEET 27 OF

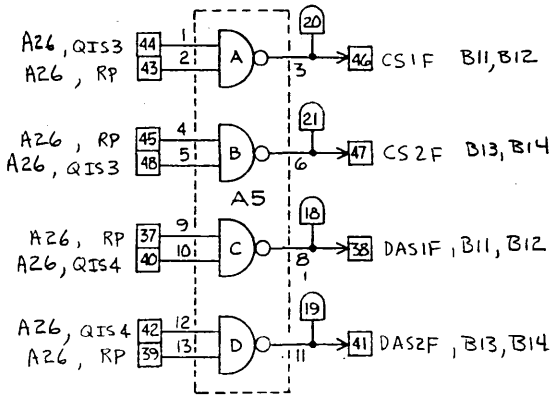
REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD

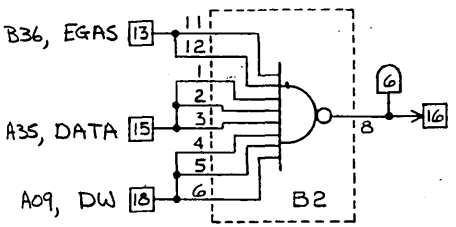


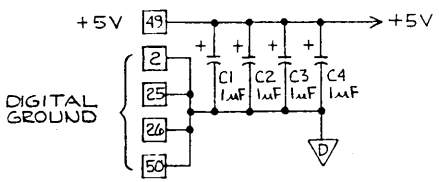












	A	B	C	D	E
1	SN7400	SN7430			
2		SN7430			
3	SN7400				
4	SN7450				
5	SN7400				
6					

TTL GATE, LOW FAN IN

DRAWING NO. 39235000 REV. A

PWA NO. 39234900 PWB NO. 39234800

CONTROL DATA CORPORATION — ANALOG • DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

DR	A. Wells	1-28-70
CHK	Guy B. Brim	3-11-70
ENGR	[illegible]	3-16-70
MFG		
APPD	[illegible]	3-18-70
	A. Wells	3-17-70

TITLE: TTL GATE, LOW FAN IN

PARD NO. A28

LOGIC TYPE 9GKT

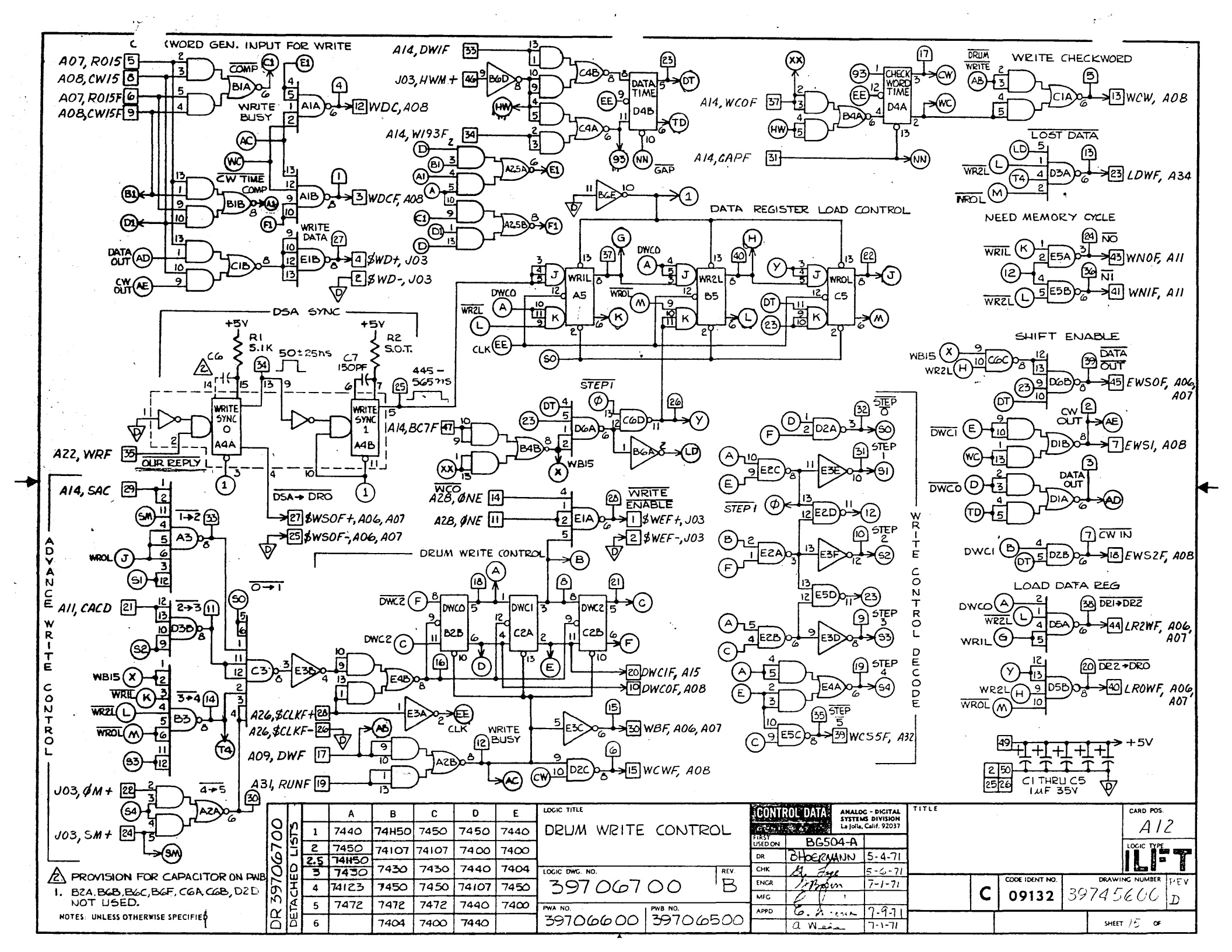
CODE IDENT NO. 09132

DRAWING NUMBER 39745600 RFV F

SHEET 28 OF

3/69 DIETERI LEARPRINT 1000H-8

4 3 2 1



⚠2. PROVISION FOR CAPACITOR ON PWB

1. B2A, B6B, B6C, B6F, C6A, C6B, D2D NOT USED.

NOTES: UNLESS OTHERWISE SPECIFIED

DR 39706700

DETACHED LISTS

	A	B	C	D	E
1	7440	74H50	7450	7450	7440
2	7450	74107	74107	7400	7400
2.5	74H50				
3	7430	7430	7430	7440	7404
4	74123	7450	7450	74107	7450
5	7472	7472	7472	7440	7400
6		7404	7400	7440	

LOGIC TITLE: DRUM WRITE CONTROL

LOGIC DWG. NO.: 39706700 REV. B

PWA NO.: 39706600 PWB NO.: 39706500

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

FIRST USED ON	B6504-A	
DR	DHOERMANN	5-4-71
CHK		5-6-71
ENGR		7-1-71
MFG		
APPD		7-9-71
		7-1-71

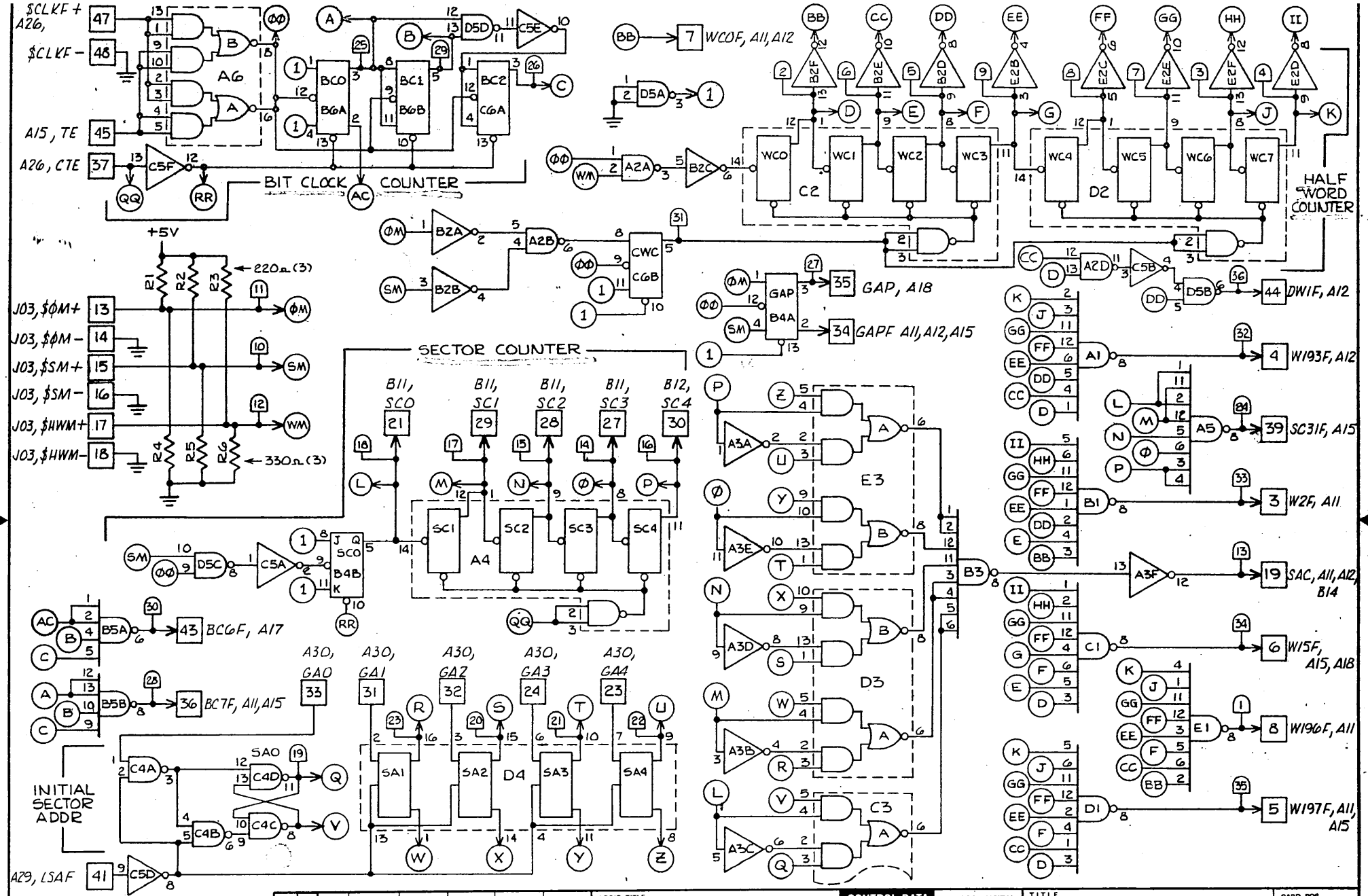
TITLE

CARD POS. A12

LOGIC TYPE ILIFT

C | CODE IDENT NO. 09132 | DRAWING NUMBER 39745600 | REV D

SHEET 15 OF



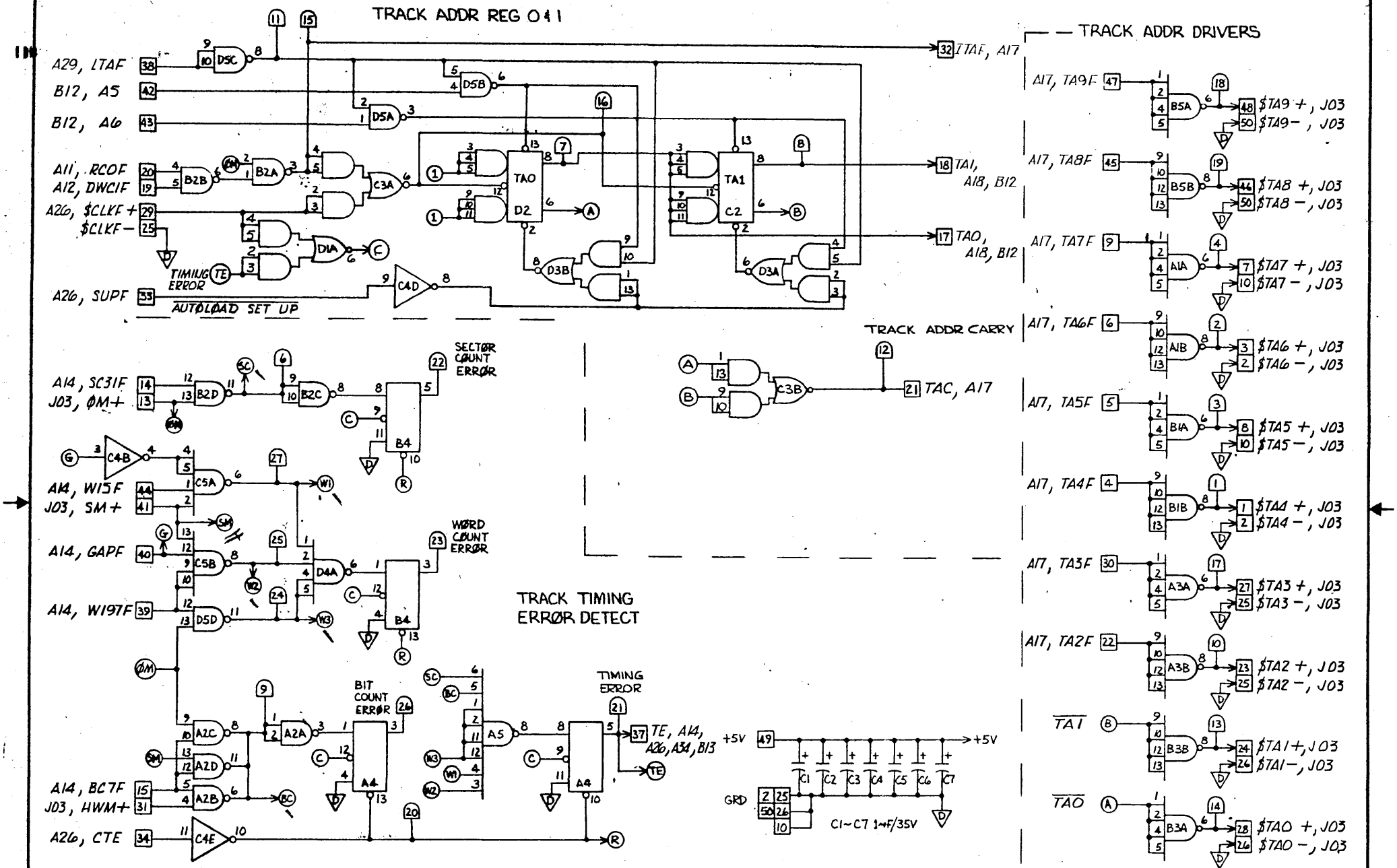
DR: 39705200 DETACHED LISTS	A	B	C	D	E
1	7430	7430	7430	7430	7430
2	7400	7404	7493	7493	7404
3	7404	7430	7450	7450	7450
4	7493	74107	7400	7475	
5	7430	7440	7404	7400	
6	7450	74107	74107		

LOGIC TITLE: TRACK TIMING NO. 1
LOGIC DWG. NO.: 39705200 REV.: A
PWA NO.: 39705100 PWB NO.: 39705000

CONTROL DATA CORPORATION — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

FIRST USED ON		
DR	D Hoermann	3-18-71
CHK	E. Lyge	3-22-71
ENGR		
MFG		
APPD		

TITLE: TRACK TIMING NO. 1
CARD POS.: A14
LOGIC TYPE: ILAT
CODE IDENT NO.: C 09132
DRAWING NUMBER: 39745600 REV: F
SHEET 16 OF



	A	B	C	D	E
1	7440	7440	7472	7450	
2	849	7400	7472	7472	
3	7440	7440	7450	7450	
4	74107	74107	7404	7440	
5	7430	7440	7440	7400	
6					

DR 39706400 DETACHED LISTS

1. C4F, D1B NOT USED

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: TRACK TIMING # 2

LOGIC DWG. NO.: 39706400 REV. A

PWA NO.: 39706300 PWB NO.: 39706200

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

HI-ST USED	BG504-A	
DR		5/7/71
CHK		5-7-71
ENGR		
MFG		
APPD		

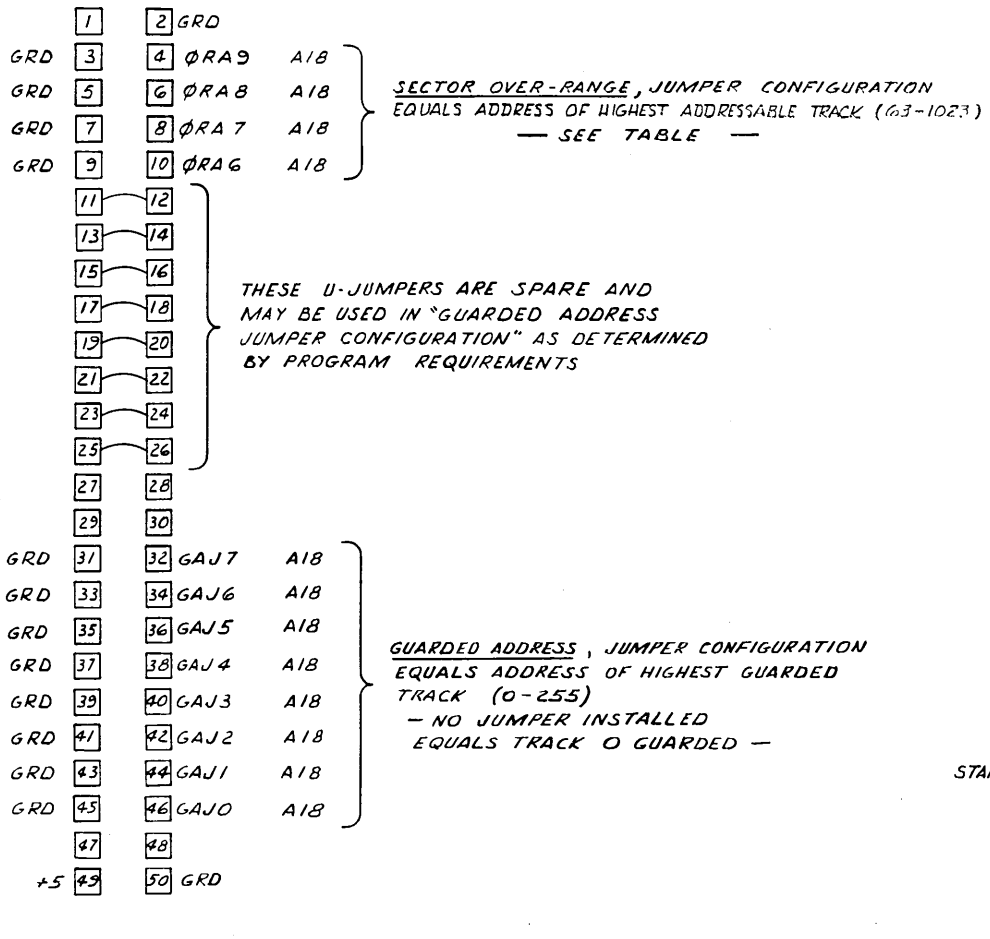
TITLE: TRACK TIMING # 2

CARD POS.: A15

LOGIC TYPE: ILET

C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600 | REV: F

SHEET 17 OF



SECTOR OVER-RANGE JUMPER CONFIGURATION

	DRUM PART NO.	NO. OF TRACKS	U-JUMPERS BETWEEN PINS 3-4	5-6	7-8	9-10
STANDARD	39668602	64				
	03	128				1
	04	192			1	
	05	256			1	1
	06	320		1		
	07	384		1		1
	08	448		1	1	
	09	512		1	1	1
QSE ONLY	10	576	1			
	11	640	1			1
	12	704	1		1	
	13	768	1		1	1
	14	832	1	1		
	15	896	1	1		1
	16	960	1	1	1	
	39668617	1024	1	1	1	1

• 0400_{16}

NOTES: UNLESS OTHERWISE SPECIFIED

	A	B	C	D	E
1					
2					
3					
4					
5					
6					

LOGIC TITLE

LOGIC DWG. NO. REV.

PWA NO. PWB NO.

CONTROL DATA CORPORATION
ANALOG - DIGITAL SYSTEMS DIVISION
La Jolla, Calif. 92037

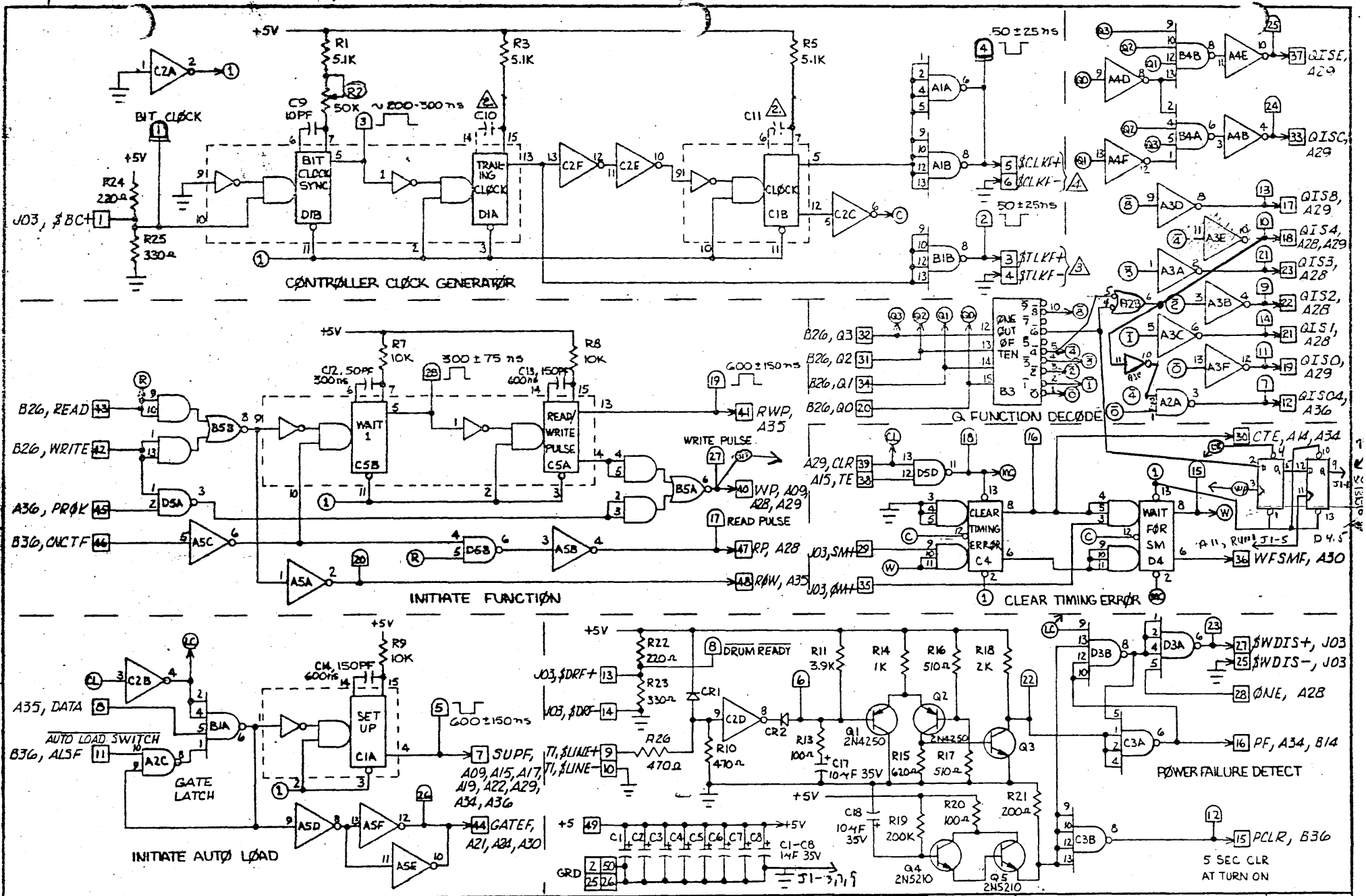
	FIRST USED ON
DR	
CHK	
ENGR	
MFG	
APPD	

TITLE
GUARDED ADDRESS/
SECTOR OVER-RANGE
JUMPERS

CARD POS. A16
LOGIC TYPE

CODE IDENT NO. C 09132
DRAWING NUMBER 39745600
REV B

SHEET 18 OF



4. A06, A07, A08, A11, A12, A14, A15, A17, A21, A24, A26, A32, A34.

3. A06, A07, A08, A11.

2. PROVISION FOR CAPACITOR ON PWB.

1. A2B, A2D, A4A, A4C, D5C ARE NOT USED

NOTES: UNLESS OT I SPECIFIED

DR 3970400 DETACHED LISTS

	A	B	C	D	E
1	7440	7440	74123	74123	
2	7400		7404		
3	7404	7447	7413	7440	
4	7404	7440	7472	7472	
5	7404	7450	74123	7400	
6					

LOGIC TITLE: CONTROLLER CLOCK

LOGIC DWG. NO.: 39708400 REV.: B

PWA NO.: 3970830 PWB NO.: 39708200

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

	FIRST USED ON	DR	CHK	ENGR	MFG	APPD
	BG504-A					
		4/26/71	5-7-71			

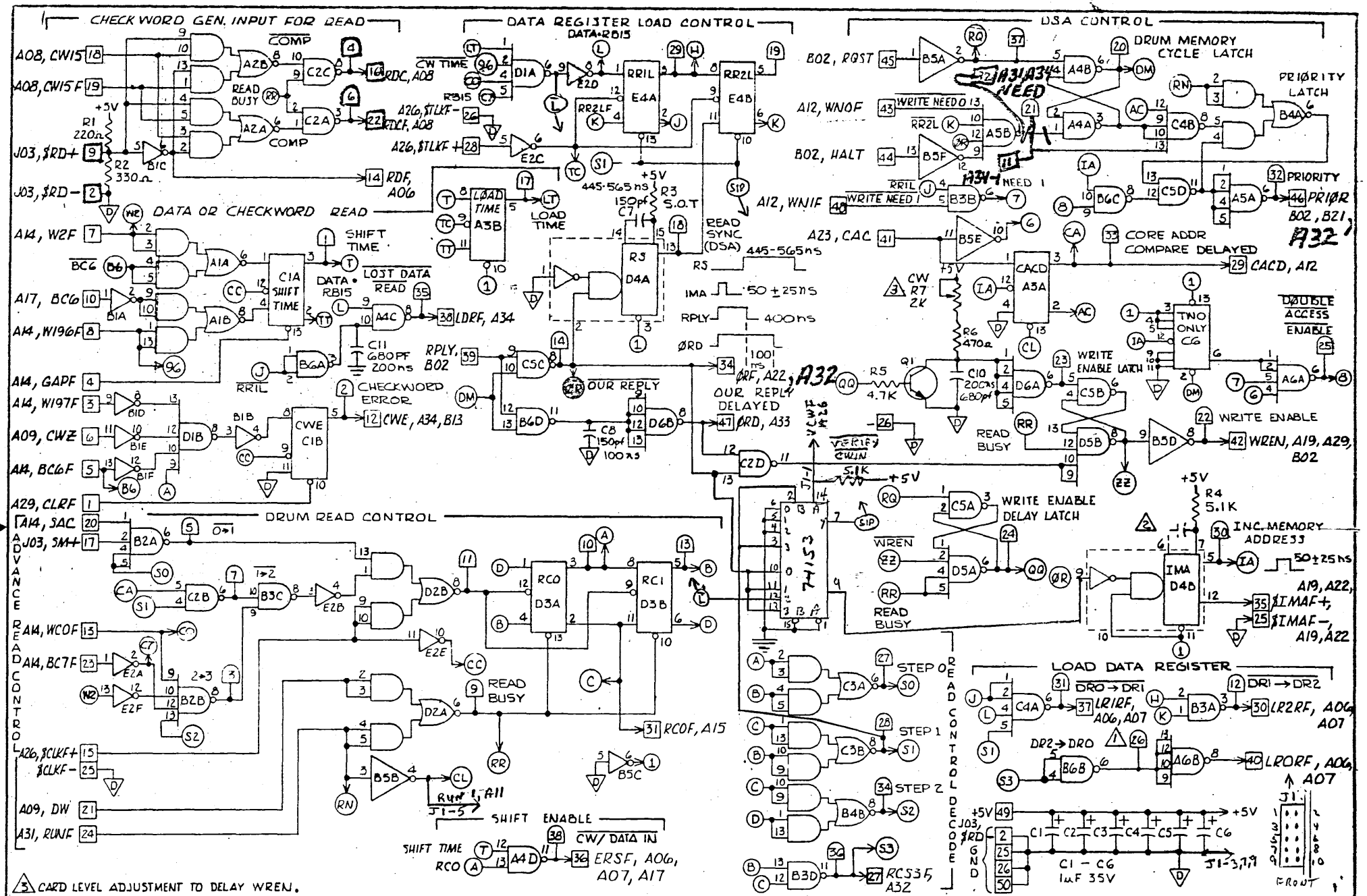
TITLE: CONTROLLER CLOCK

CARD POS: A26

LOGIC TYPE: 1LGT

CODE IDENT NO.: C 09132

DRAWING NUMBER: 3974560 REV: E



	A	B	C	D	E
1	7450	7404	74107	7440	
2	7450	7440	7400	7450	7404
3	74107	7400	7450	74107	
4	7400	7450	7440	74123	74107
5	7440	7404	7400	7440	
6	7440	849	7472	7413	

LOGIC TITLE: DRUM READ/DSA CONTROL

LOGIC DWG NO.: 39706100 REV: C

PWA NO: 39706[illegible] PWB NO.: 39705900

CONTROL DATA CORPORATION — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

FIRST USED ON	BG504-A	
DR	B. Roberts	5-6-71
CHK	[illegible]	5-7-71
ENGR	[illegible]	7-1-71
MFG		
APPD	[illegible]	7-9-71
	[illegible]	7-1-71

TITLE: DRUM READ/DSA CONTROL

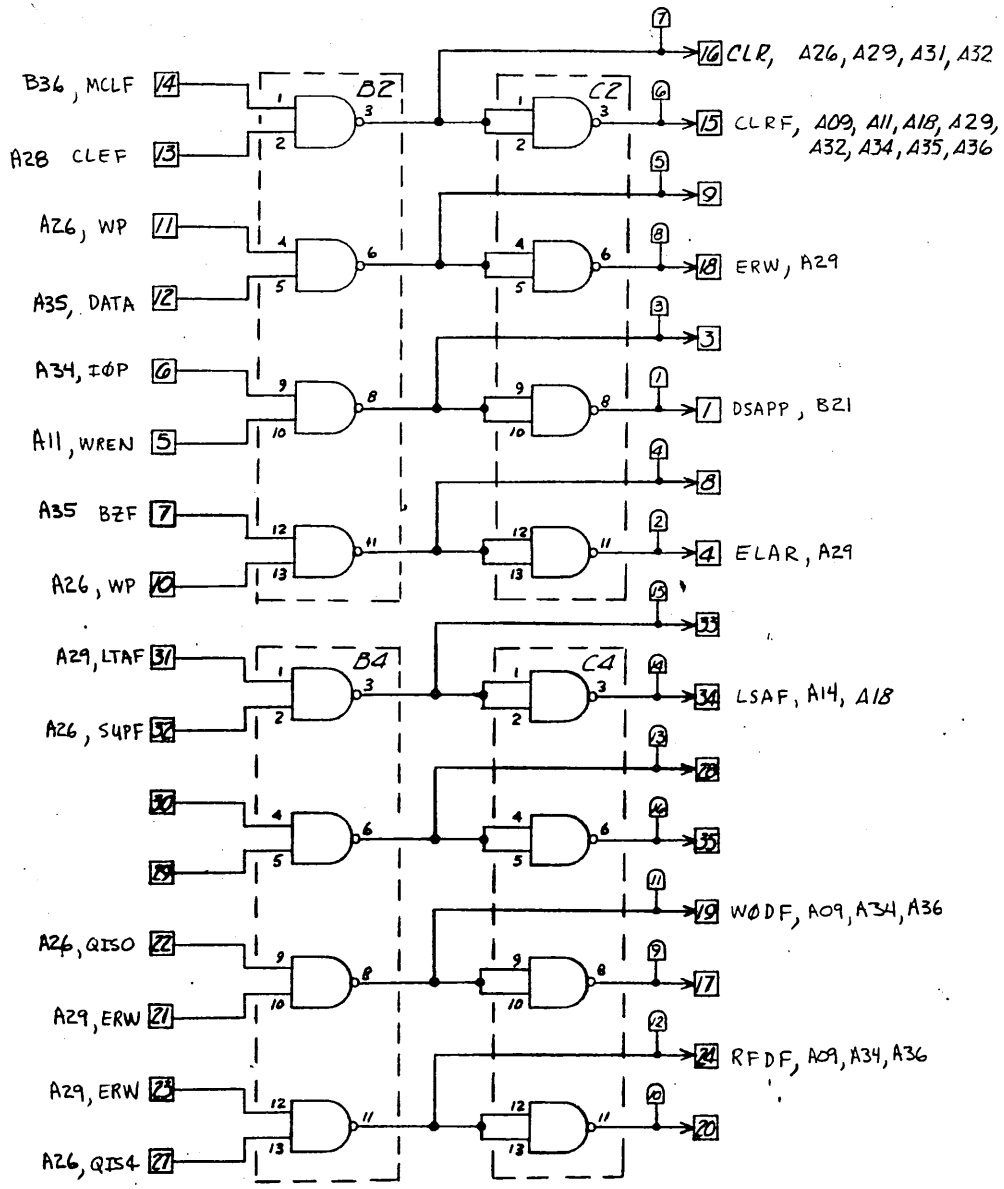
CARD POS.: A11

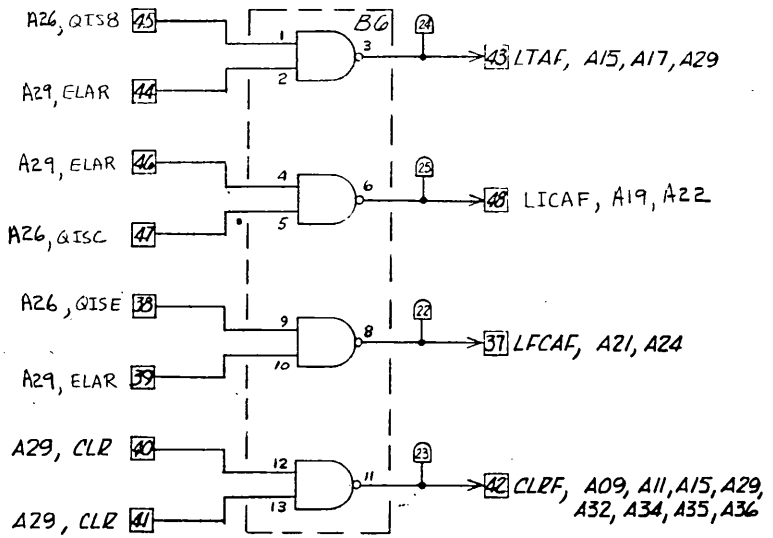
LOGIC TYPE: 1LDT

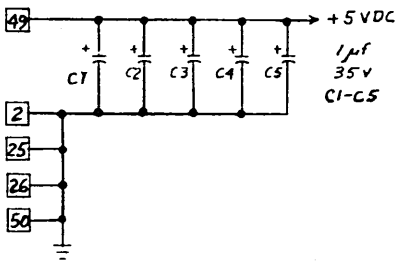
CODE IDENT NO.: C 09132

DRAWING NUMBER: 39745600 REV: F

SHEET 14 OF







ALL 8165 SN7400 (S)
49 = US
50 = SEE NOTE 7

NOTES: UNLESS OTHERWISE SPECIFIED

	A	B	C	D	E
1					
2		SN7400	SN7400		
3					
4		SN7400	SN7400		
5					
6		SN7400			

LOGIC TITLE: NAND 2-INPUT SINGLE/DOUBLE INVERT

LOGIC DWG. NO. 39377500 REV. A

PWA NO. 39377400 PWB NO. 39377300

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON	DE101-A	
DR	M. Hanel	12-11-9
CHK	G.J. Brim	12-16-69
ENGR	Cunningham	8-6-70
MFG		
APPD	Gum J Smith	5-4-70
	WDH	5-6-0

TITLE: LOGIC DIAGRAM - NAND 2-INPUT SINGLE/DOUBLE INVERT

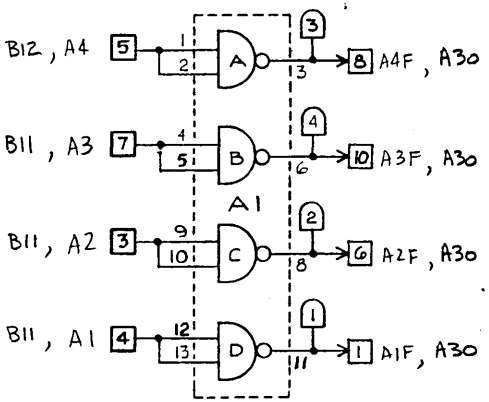
CARD POS. A29

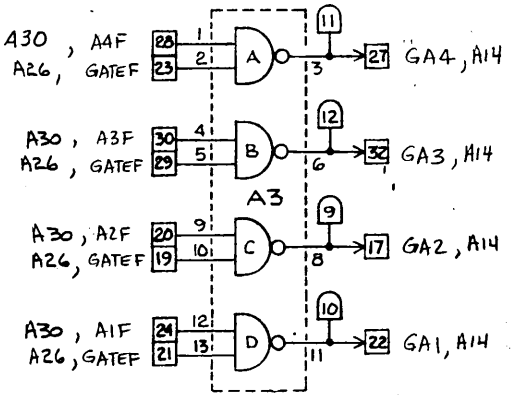
LOGIC TYPE 9DDT

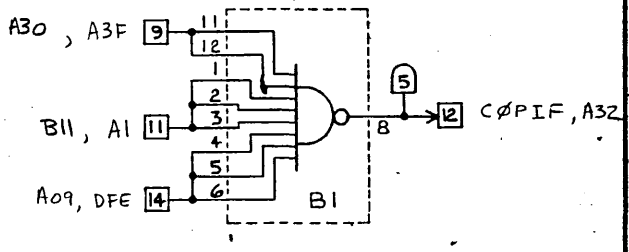
C | CODE IDENT NO. 09132 | DRAWING NUMBER 39745600 | REV B

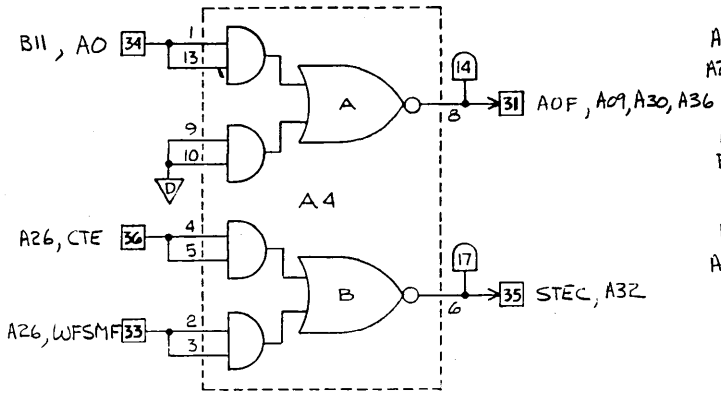
SHEET 29 OF

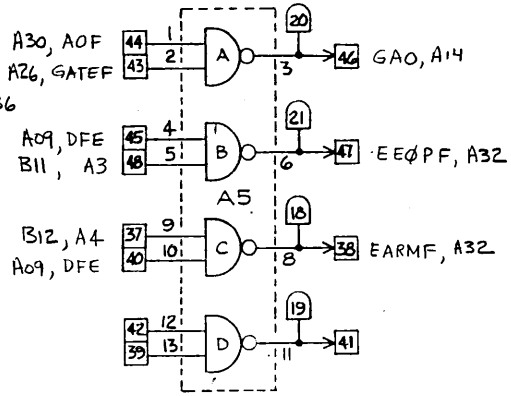
REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD

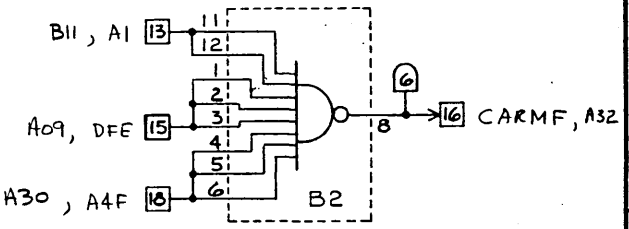


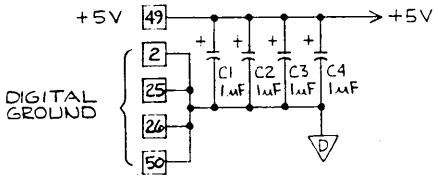












	A	B	C	D	E
1	SN7400	SN7430			
2		SN7430			
3	SN7400				
4	SN7450				
5	SN7400				
6					

TTL GATE, LOW FAN IN

39235000 A

PWB NO. 39234900 | PWB NO. 39234800

CONTROL DATA CORPORATION — ANALOG • DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

DR	A. Wells	1-28-70
CHK	Guy B. Brown	3-11-70
ENGR	[illegible]	3-16-70
MFG		
APPD	[illegible]	3-18-70
	A. Wells	3-17-70

TITLE: TTL GATE, LOW FAN IN

CARD PGM: A30

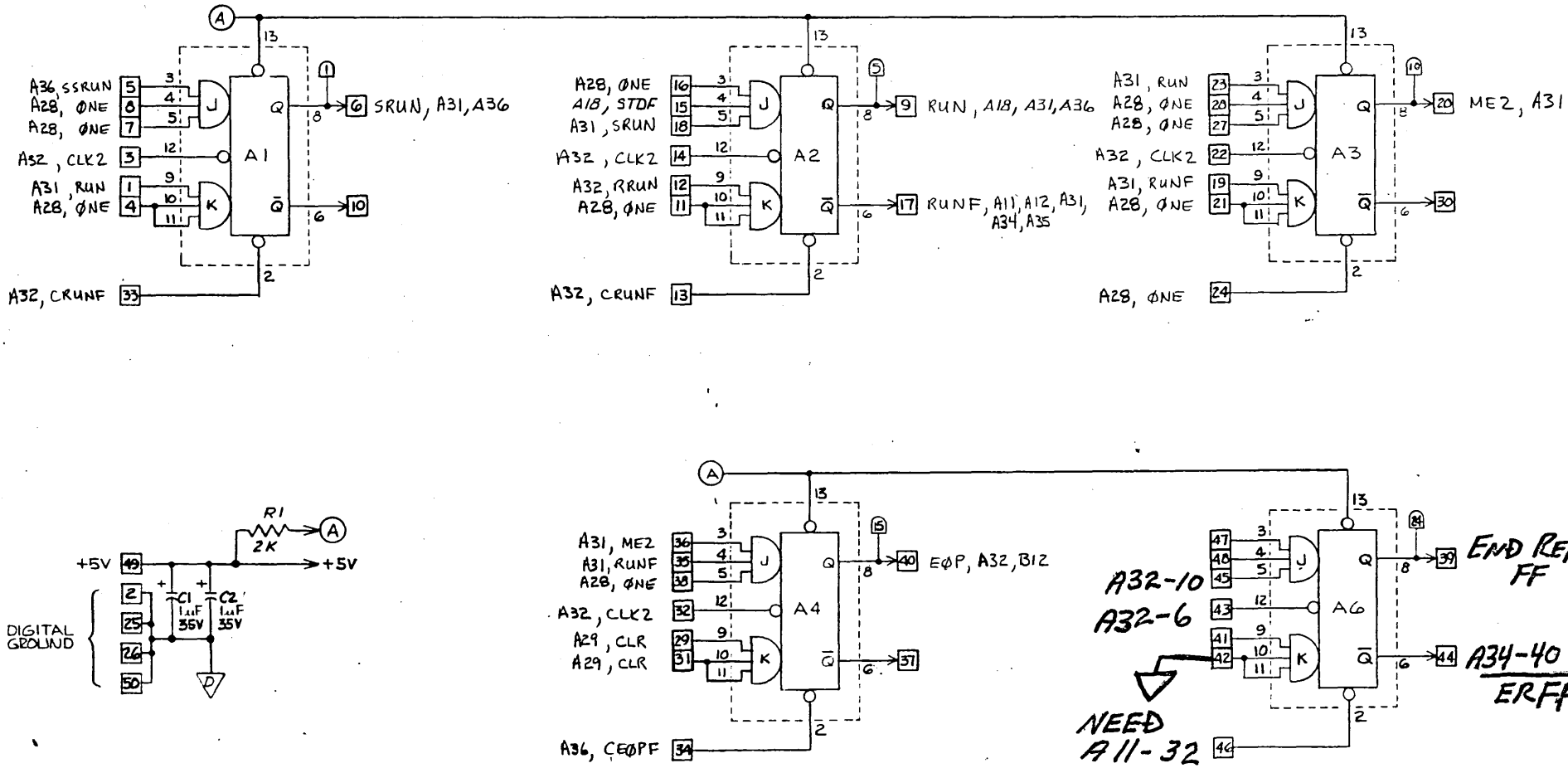
LOGIC TYPE: 9GKT

C | CODE IDENT NO. 09132 | DRAWING NUMBER 39745600

SHEET 30 OF

4 3 2 1

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD



ALL CHIPS: PIN 14 Vcc, PIN 7 GRD.

	A	B	C	D	E
1	SN7472				
2	SN7472				
3	SN7472				
4	SN7472				
5					
6	SN7472				

CARD TYPE	CARD TITLE	
9GLT	TTL JK FLIP FLOP - 5	
PRODUCT	CARD DWG. NO.	REV.
	39235200	

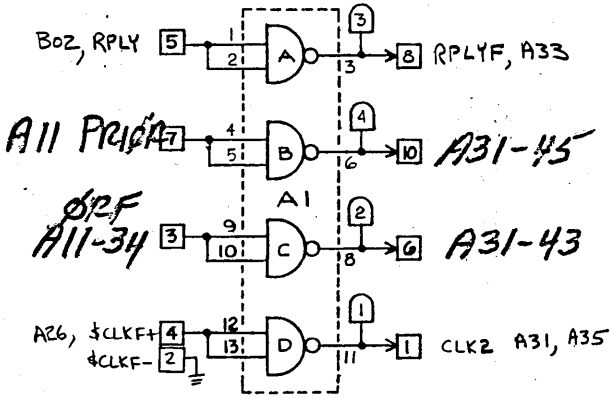
CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

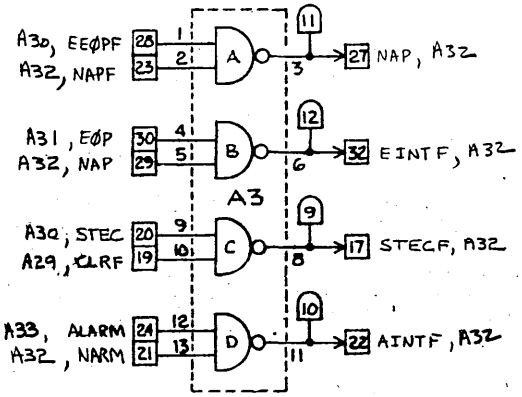
TITLE	CARD POS.
TTL JK FLIP FLOP - 5	A31

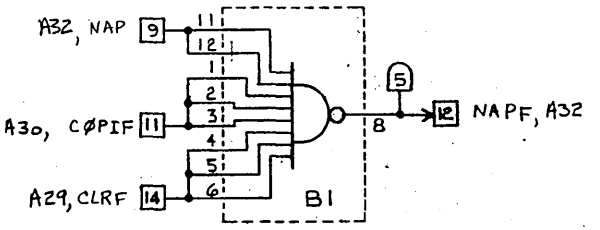
MODEL	DWG. NO.	REV.	SHEET	PAGE
-	[illegible]	A	31	

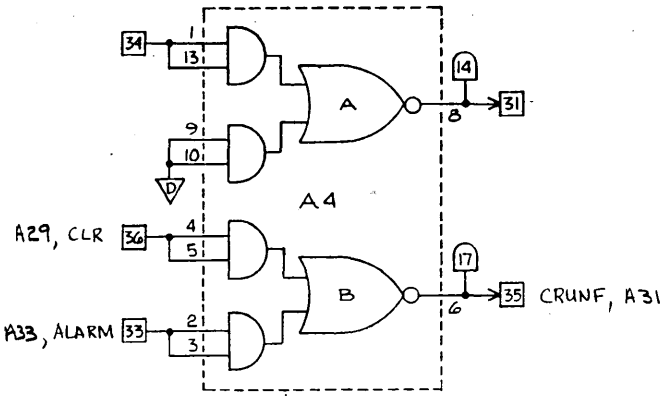
A

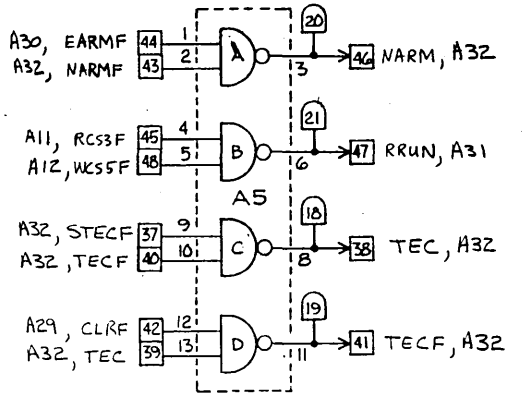
REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD

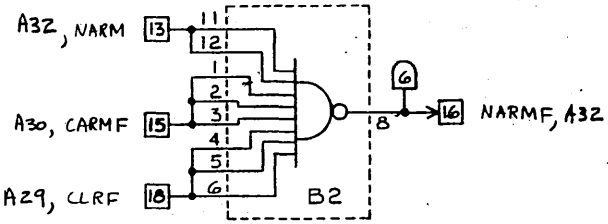


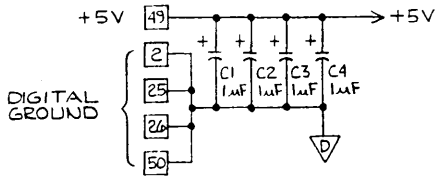












	A	B	C	D	E
1	SN7400	SN7430			
2		SN7430			
3	SN7400				
4	SN7450				
5	SN7400				
6					

TTL GATE, LOW FAN IN

39235000 REV A

39234900 39234800

CONTROL DATA COMPONENTS — ANALOG + DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

DR	A. Wells	1-28-70
CHK	Guy B. Brion	3-11-70
ENGR	[illegible]	3-16-70
MFG		
APPD	[illegible]	3-18-70
	A. Wells	3-17-70

TITLE: TTL GATE, LOW FAN IN

CARD POS. A32

LOGIC TYPE 9GKT

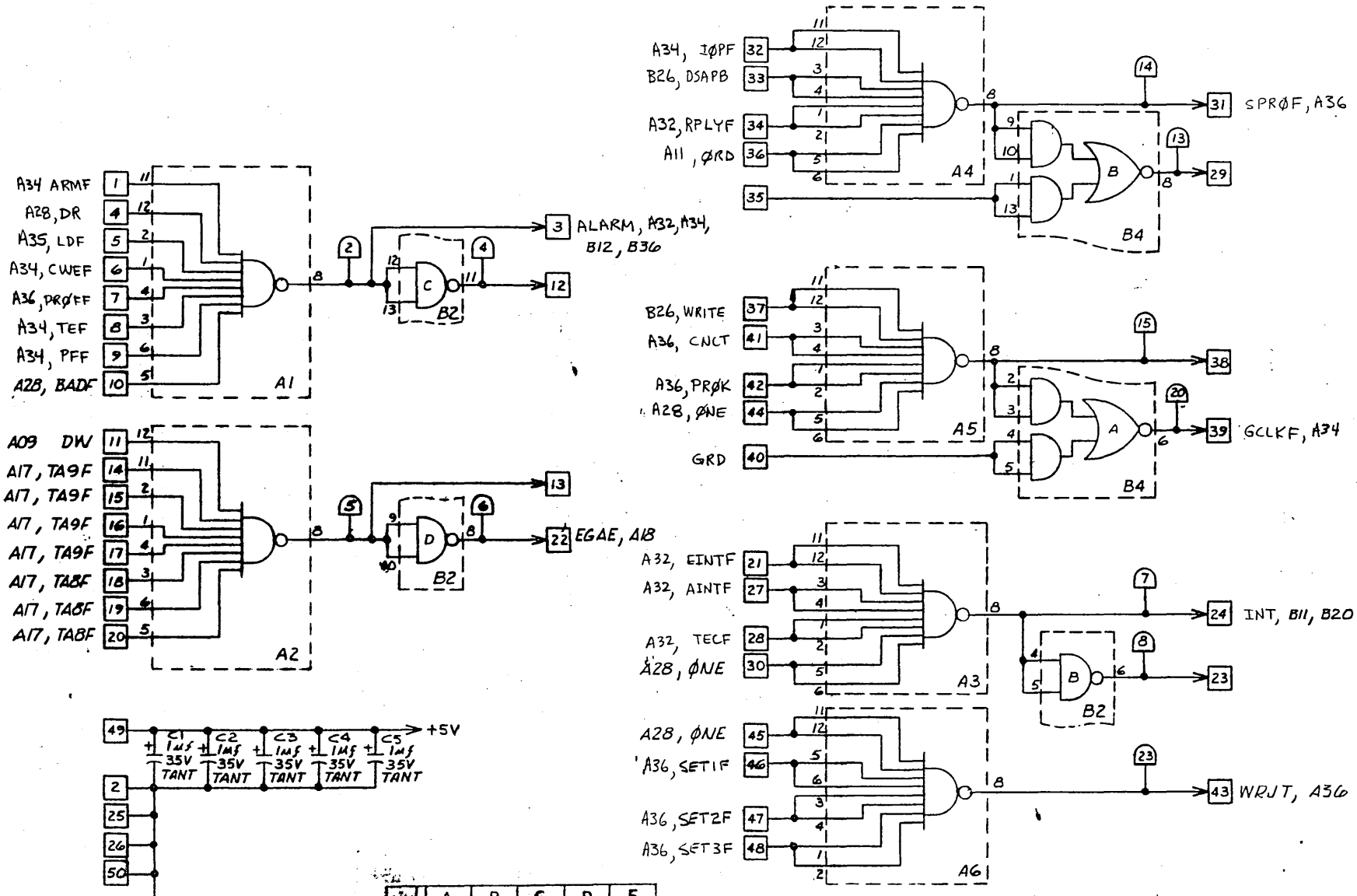
C | CODE IDENT NO. 09132 | DRAWING NUMBER 39745600

SHEET 32 OF

3/69 DIETERI LARPRINT 1000H-8

4 3 2 1

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD



	A	B	C	D	E
1	SN7432				
2	SN7430	SN7400			
3	SN7430				
4	SN7430	SN7450			
5	SN7430				
6	SN7409				

2. ALL CHIPS – PIN 7 IS GRD, PIN 14 IS Vcc.
1. B2A NOT USED.

NOTE: UNLESS OTHERWISE SPECIFIED,

CARD TYPE	CARD TITLE
9GJT	TTL GATE – HIGH FAN IN
PRODUCT	CARD DWG. NO / REV.
300	39234600

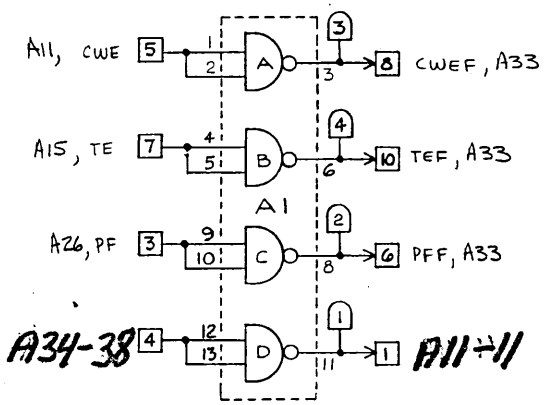
CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

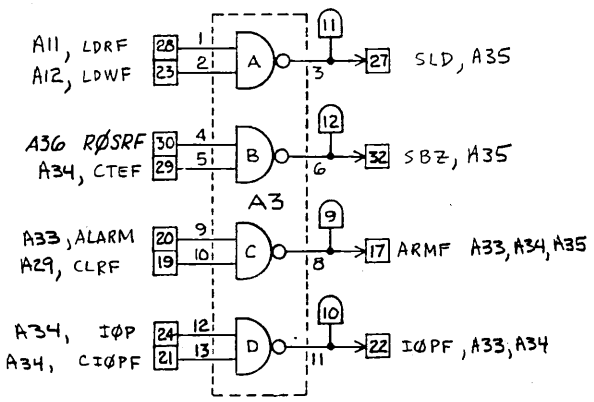
TITLE	CARD POS.
TTL GATE – HIGH FAN IN	A33

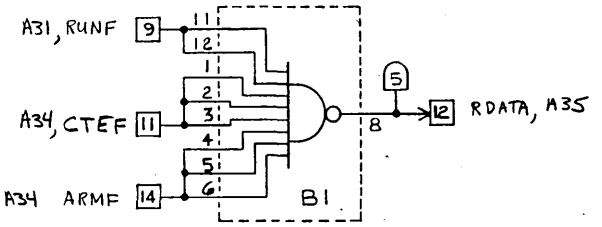
MODEL	DWG. NO.	REV.	SHEET	PAGE
	[illegible]	B	55	

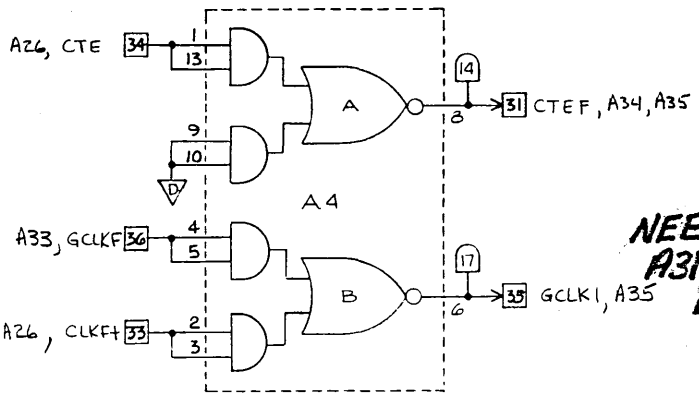
A

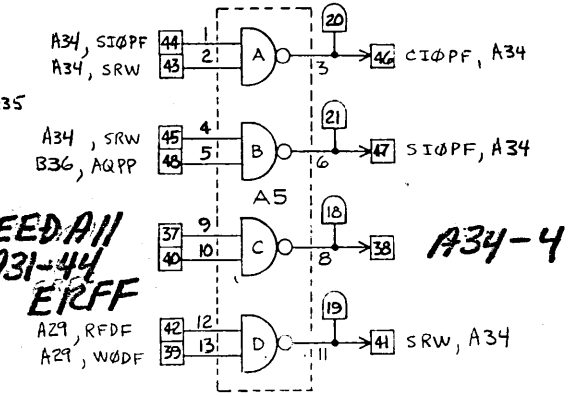
REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD

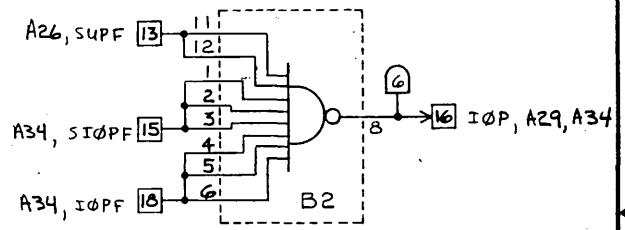


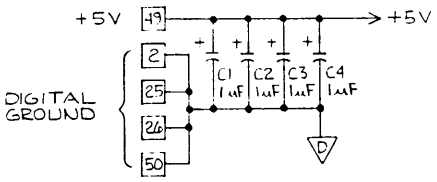












1	SN7400 SN7430
2	SN7430
3	SN7400
4	SN7450
5	SN7400
6	

TTL GATE, LOW FAN IN

39235000 A

39234900 | 39234800

CONTROL DATA CORPORATION — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

A. Weiss	1-28-70
[illegible]	3-11-70
[illegible]	3-16-70
[illegible]	3-18-70
A. Weiss	3-17-70

TITLE: TTL GATE, LOW FAN IN

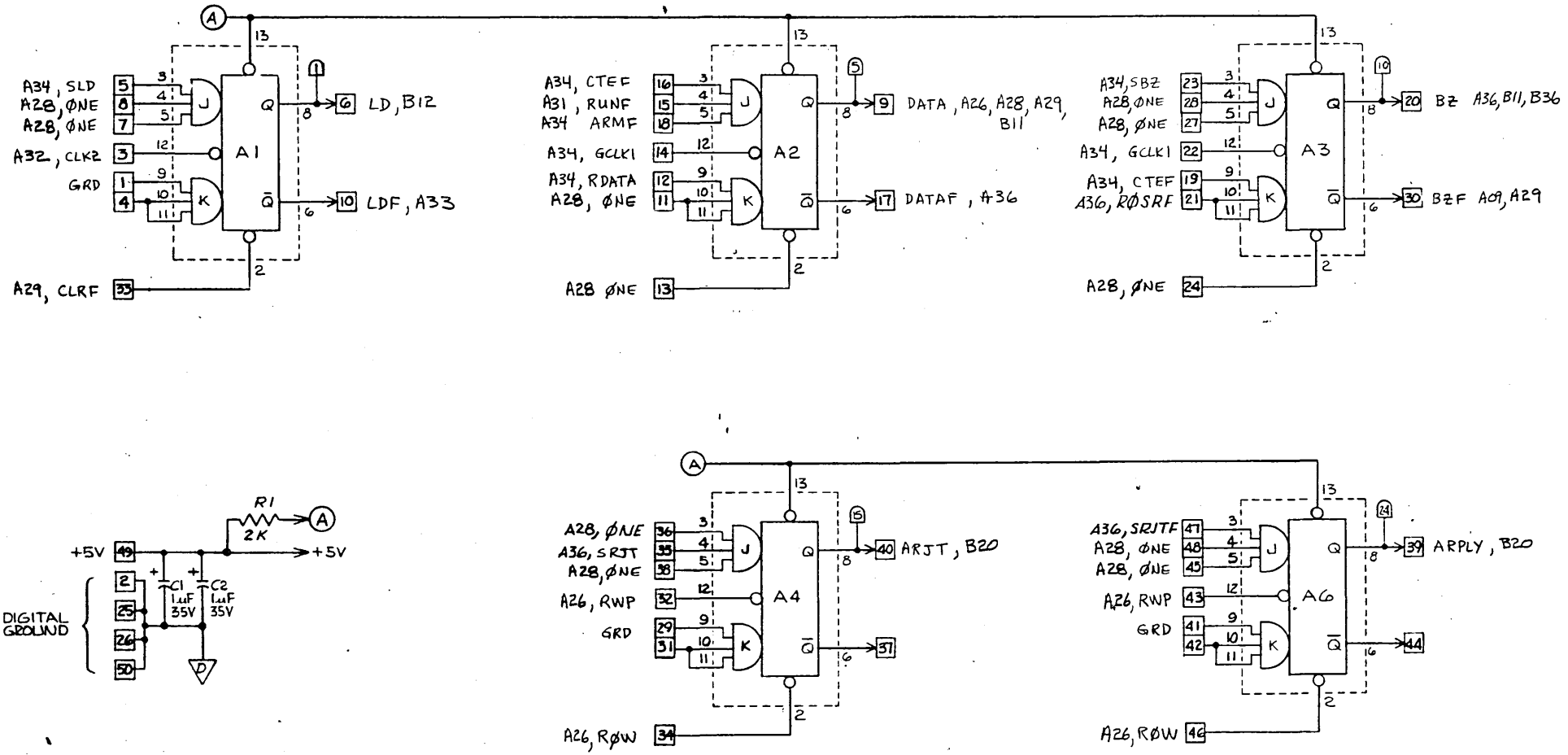
CARD POS: A34

LOGIC TYPE: 9GKT

SIZE: C | CODE IDENT NO: 09132 | DRAWING NUMBER: 39745600

SHEET 34 OF

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD



ALL CHIPS: PIN 14 Vcc, PIN 7 GRD.

	A	B	C	D	E
1	SN7472				
2	SN7472				
3	SN7472				
4	SN7472				
5					
6	SN7472				

CARD TYPE	CARD TITLE	
9GLT	TTL JK FLIP FLOP-5	
PRODUCT	CARD DWG. NO.	REV.
	39235200	

CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

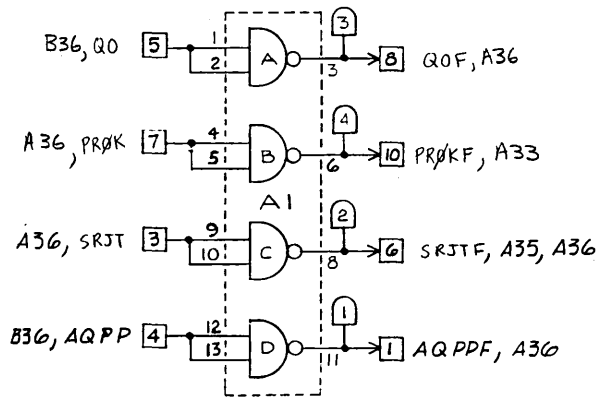
TITLE	CARD POS.
TTL JK FLIP FLOP-5	A35

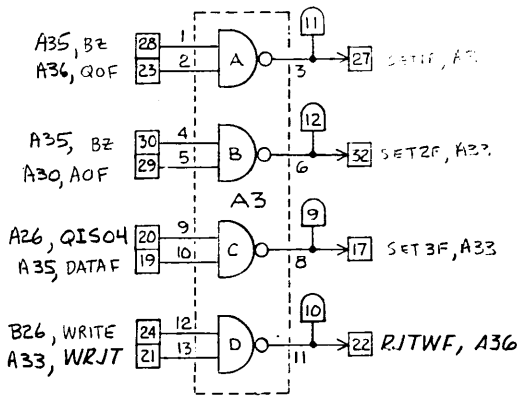
MODEL	DWG. NO.	REV.	SHEET	PAGE
-	[illegible]	B	35	

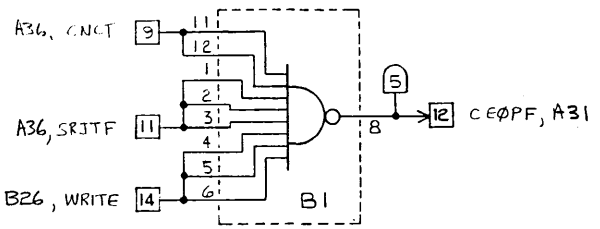
PWB 39235100

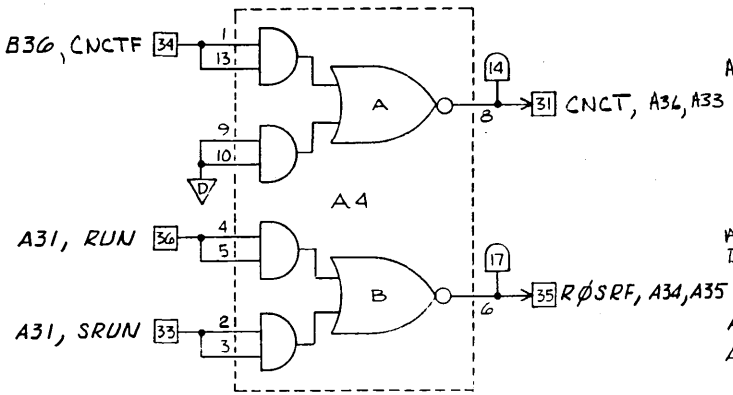
3/69 DIETERICH-POST CLEARPRINT 2000H-B

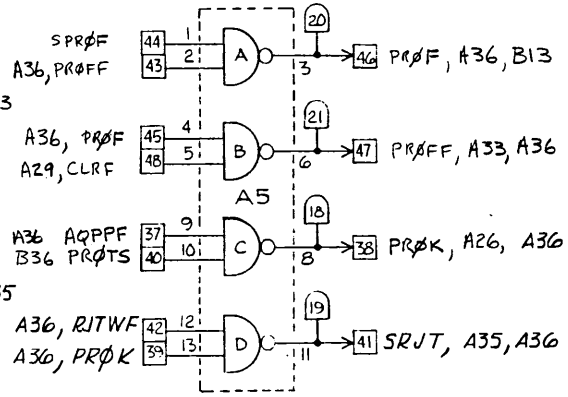
REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD

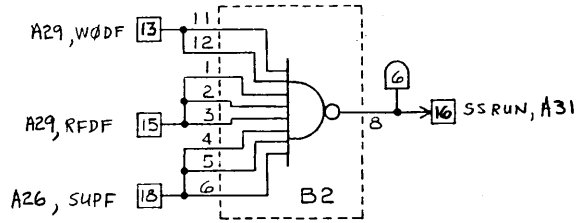


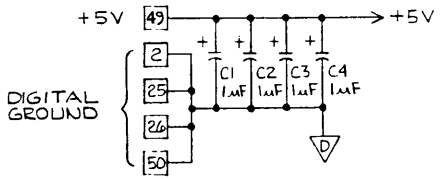












	A	B	C
1	SN7400	SN7430	
2		SN7430	
3	SN7400		
4	SN7450		
5	SN7400		
6			

TTL GATE, LOW FAN IN

39235000 REV A

FWB NO 3923490 FWB NO 3923480

CONTROL DATA CORPORATION — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

DESIGN	A. Wells	1-28-70
CHK	Guy B. Brisse	3-11-70
ENGR	[illegible]	3-16-70
MFG		
APPD	[illegible]	3-18-70
	A. Wells	3-17-70

TITLE: TTL GATE, LOW FAN IN

CARD POS: A36

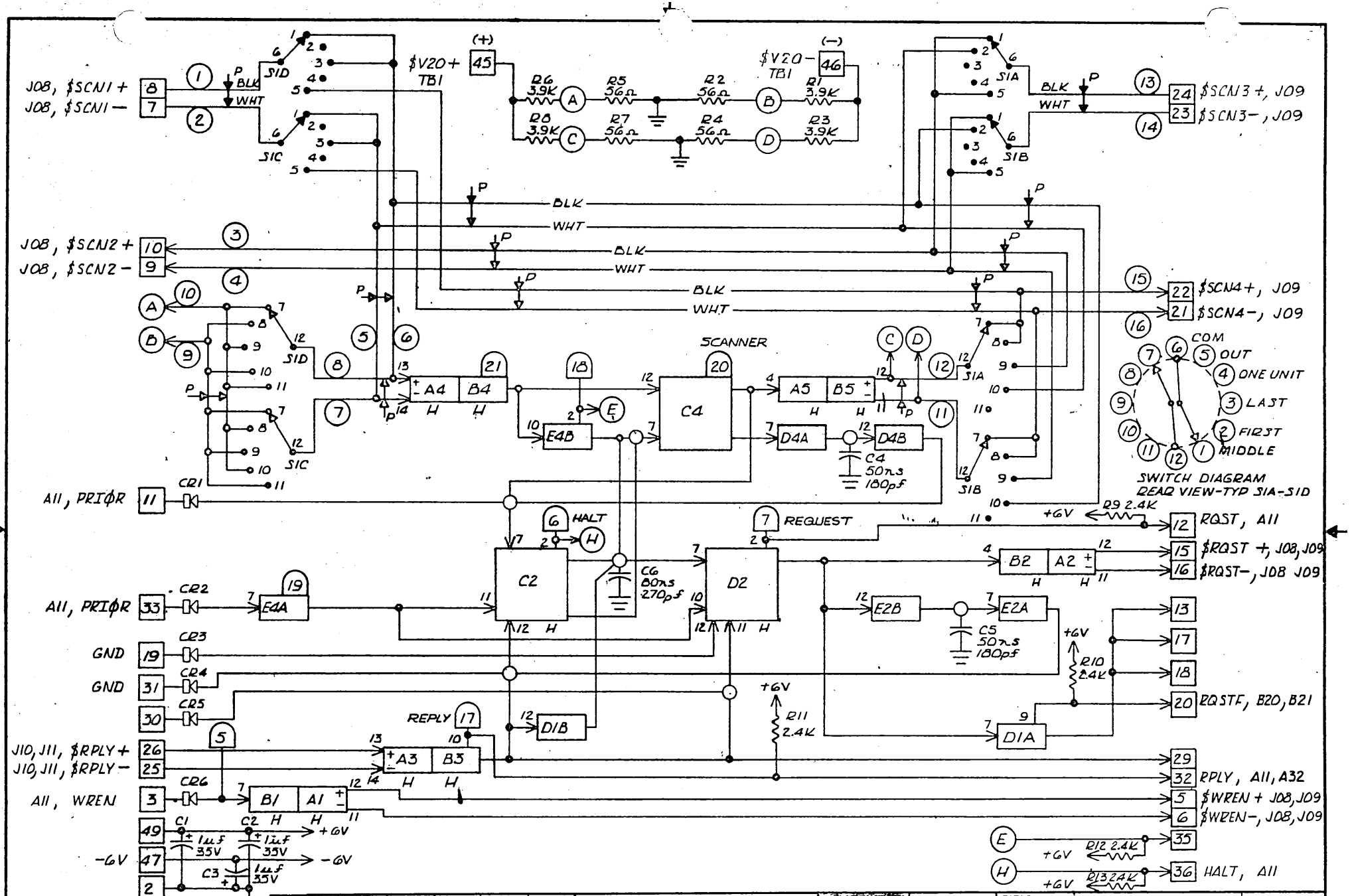
LOGIC TYPE: 9GKT

SIZE: C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600 | REV: F

SHEET 36 OF

3-69 DIETERICH-A ARPRINT 1000H-8

4 3 2 1



1. NUMBERS IN CIRCLES REFER TO CORRESPONDING NUMBERS ON CARD.

NOTES: UNLESS OTHERWISE SPECIFIED

DETACHED LISTS 39709000

	A	B	C	D	E
1	T31BH	T01AH		D34M	
2	T31BH	T01AH	F34H	F34H	D34M
3	R01AH	R01BH			
4	R01AH	R01BH	F34M	D34M	D34M
5	T01AH	T31BH			
6					

LOGIC TITLE: MEMORY SCANNER, TTL

LOGIC DWG. NO.: 39709000 REV. A

PWA NO.: 39708900 PWB NO.: 39708800

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

FIRST USED ON		
DR	B. Roberts	4-26-71
CHK	B. Frye	5-7-71
ENGR		
MFG		
APPD		

TITLE: MEMORY SCANNER, TTL

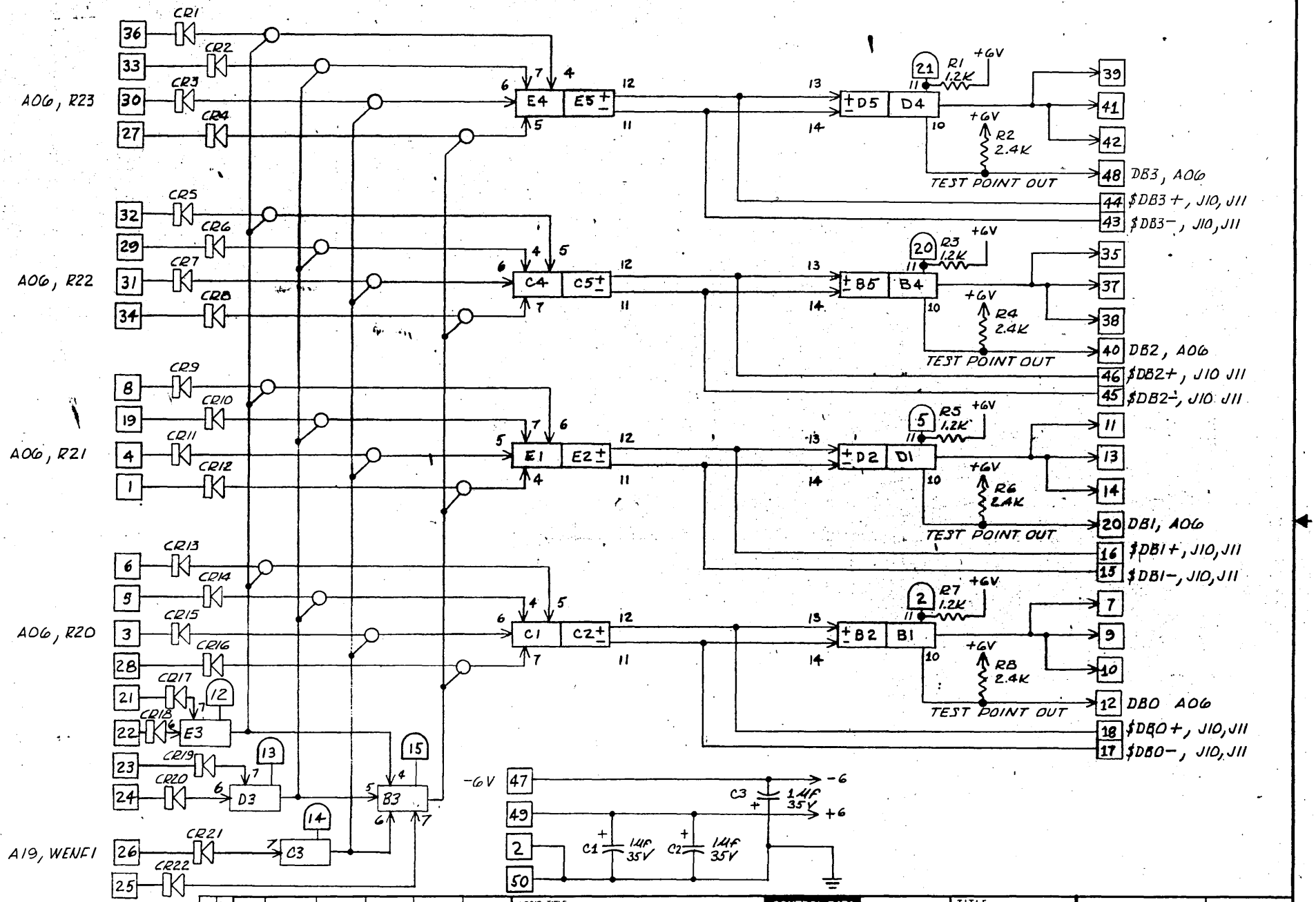
CARD POS. B02

LOGIC TYPE 1LJT

CODE IDENT NO. C 09132

DRAWING NUMBER 39745600 REV D

SHEET 37 OF



NOTES: UNLESS OTHERWISE SPECIFIED

DR 39709300 DETACHED LISTS

	A	B	C	D	E
1		R01B	T01A	R01B	T01A
2		R01A	T31B	R01A	T31B
3		I48M	I48M	I48M	I48M
4		R01B	T01A	R01B	T01A
5		R01A	T31B	R01A	T31B
6					

LOGIC TITLE: 3/4/4 GATED TRANSCEIVER, TTL

LOGIC DWG NO: 39709300 REV: A

PWA NO: 3970920^ PWB NO: 39709100

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	B. Roberts	4-29-71
CHK	G. Lage	5-3-71
ENGR		
MFG		
APPD		

TITLE: DSA DATA INTERFACE BITS 0-3

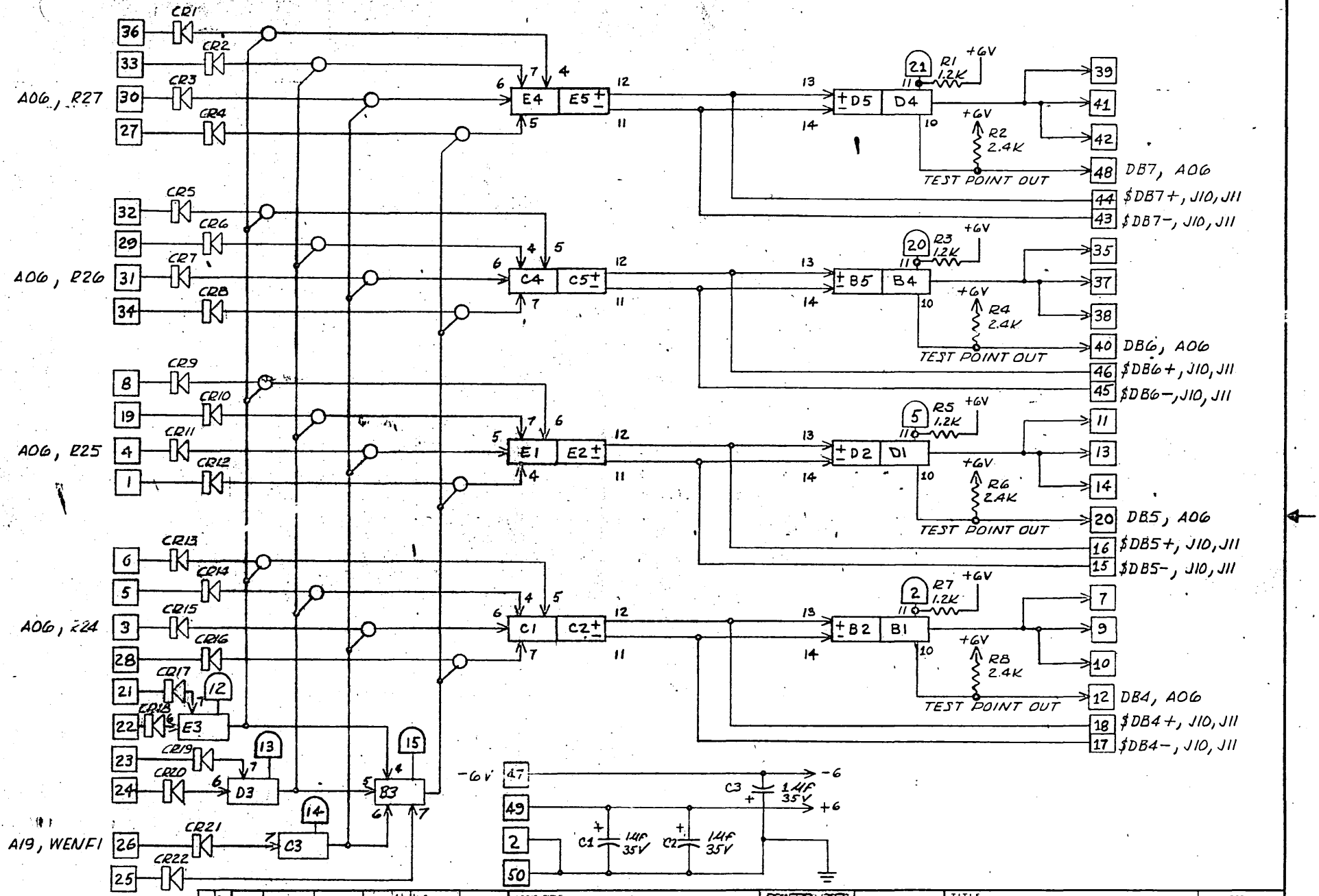
CARD POS.: B06

LOGIC TYPE: 1LKT

CODE IDENT NO.: C 09132

DRAWING NUMBER: 39745600

SHEET 38 OF



	A	B	C	D	E
1		R01B	T01A	R01B	T01A
2		R01A	T31B	R01A	T31B
3		I48M	I48M	I48M	I48M
4		R01B	T01A	R01B	T01A
5		R01A	T31B	R01A	T31B
6					

DR 39709300 DETACHED LISTS

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: 3/4/4 GATED TRANSCEIVER, TTL

LOGIC DWG NO: 39709300 REV: A

PWA NO: 39709200 PWB NO: 39709100

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	B. Roberts	4-29-71
CHK	G. Lage	5-3-71
ENGR		
MFG		
APPD		

TITLE: DSA DATA INTERFACE BITS 4-7

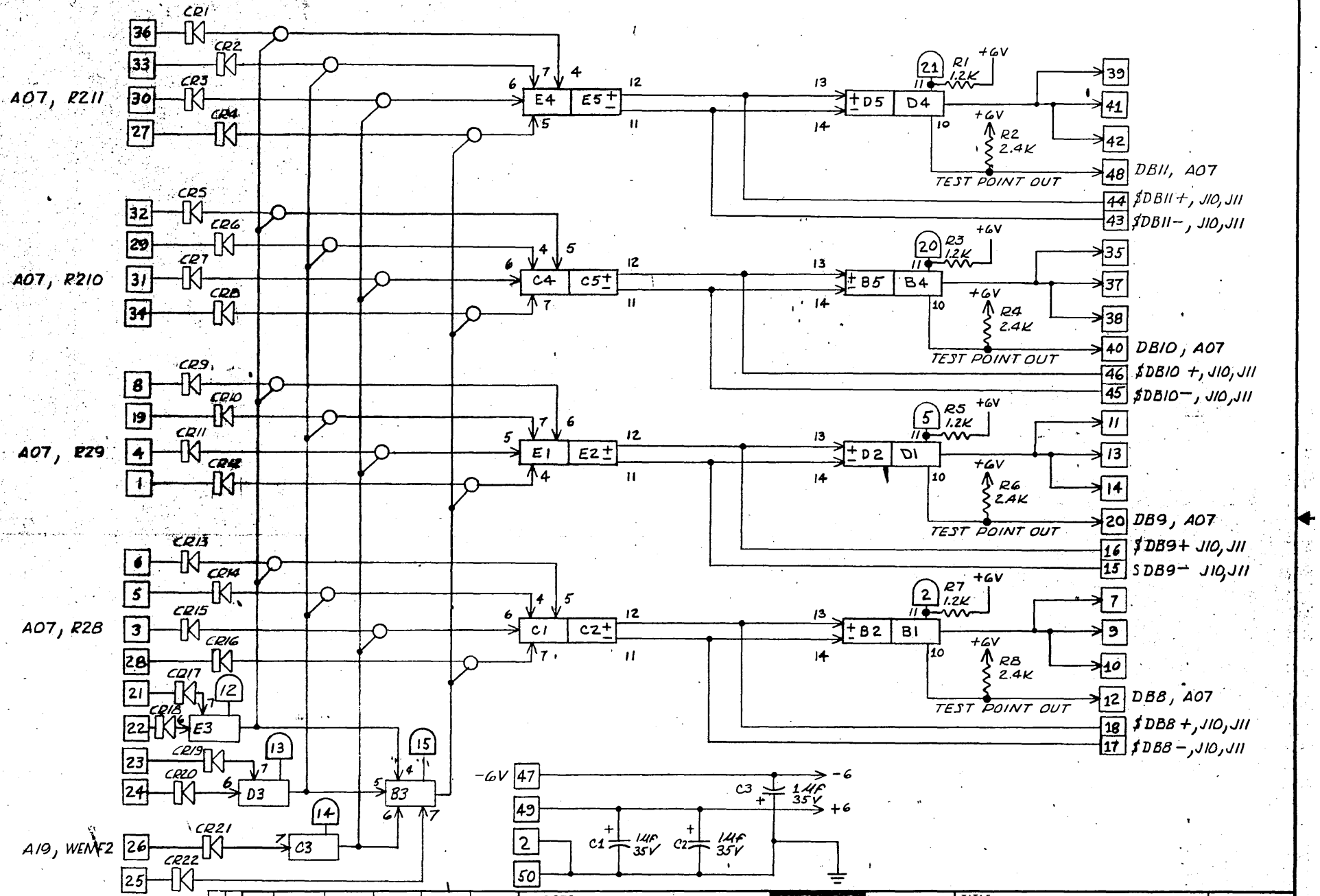
CARD POS.: B07

LOGIC TYPE: 1LKT

CODE IDENT NO.: 09132

DRAWING NUMBER: 39709300

SHEET 39 OF



DR 39709300 DETACHED LISTS	A	B	C	D	E
1		R01B	T01A	R01B	T01A
2		R01A	T31B	R01A	T31B
3		I48M	I48M	I48M	I48M
4		R01B	T01A	R01B	T01A
5		R01A	T31B	R01A	T31B
6					

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: 3/4/4 GATED TRANSCEIVER, TTL

LOGIC DWG NO: 39709300 REV: A

PWA NO: 3970920C PWB NO: 39709100

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	B. Roberts	4-29-71
CHK	H. Lage	5-3-71
ENGR		
MFG		
APPD		

TITLE: DSA DATA INTERFACE BITS 8-11

CARD POS.: B08

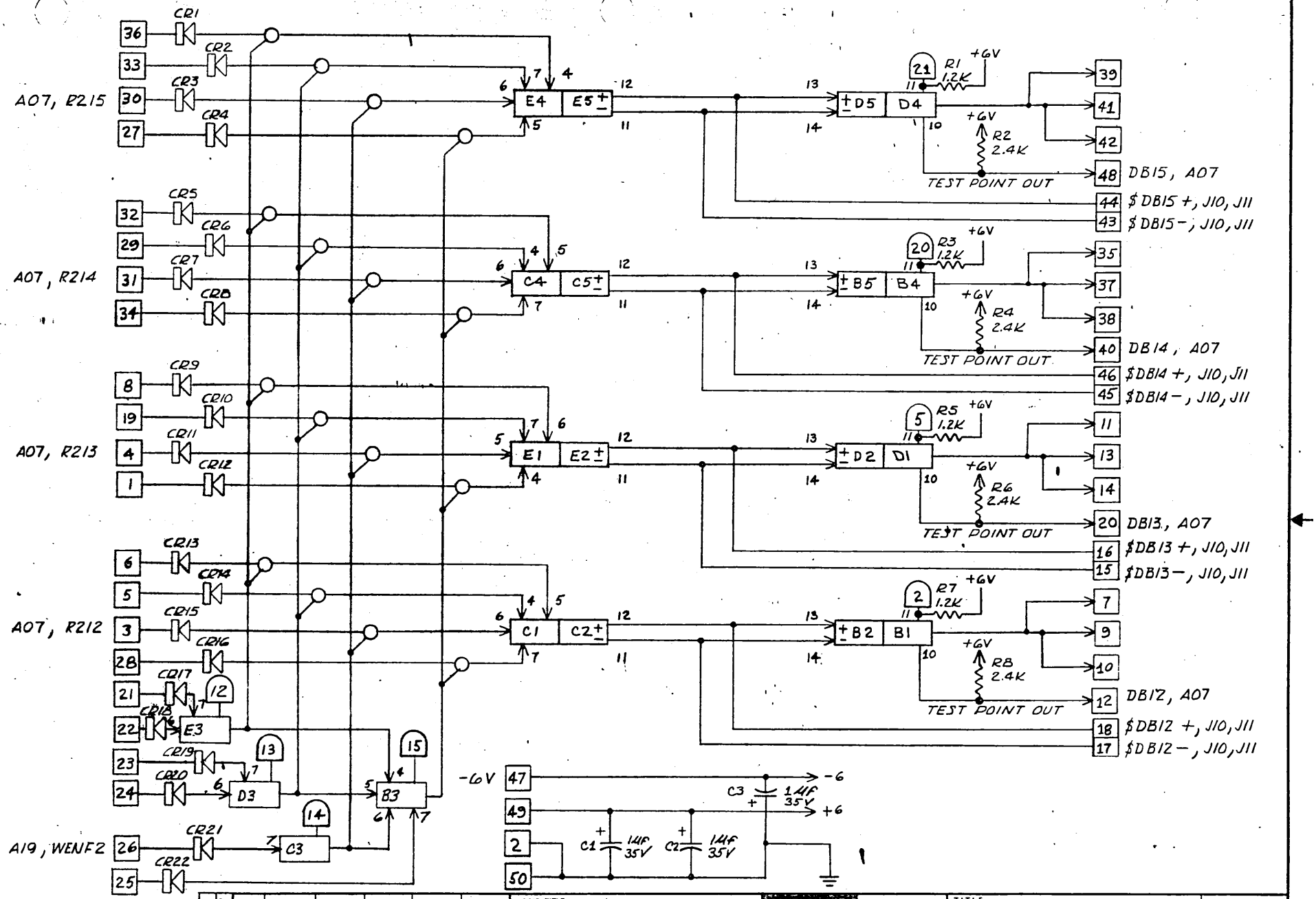
LOGIC TYPE: 1LKT

CODE IDENT NO.: 09132

DRAWING NUMBER: 39745600

SIZE: C

SHEET 40 OF



	A	B	C	D	E
1		R01B	T01A	R01B	T01A
2		R01A	T31B	R01A	T31B
3		I48M	I48M	I48M	I48M
4		R01B	T01A	R01B	T01A
5		R01A	T31B	R01A	T31B
6					

DR 39709300
DETACHED LISTS

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: 3/4/4 GATED TRANSCEIVER, TTL

LOGIC DWG NO: 39709300 REV: A

PWA NO: 39709200 PWB NO: 39709100

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	B. Roberts	4-29-71
CHK	E. Lage	5-3-71
ENGR		
MFG		
APPD		

TITLE: DSA DATA INTERFACE BITS 12-15

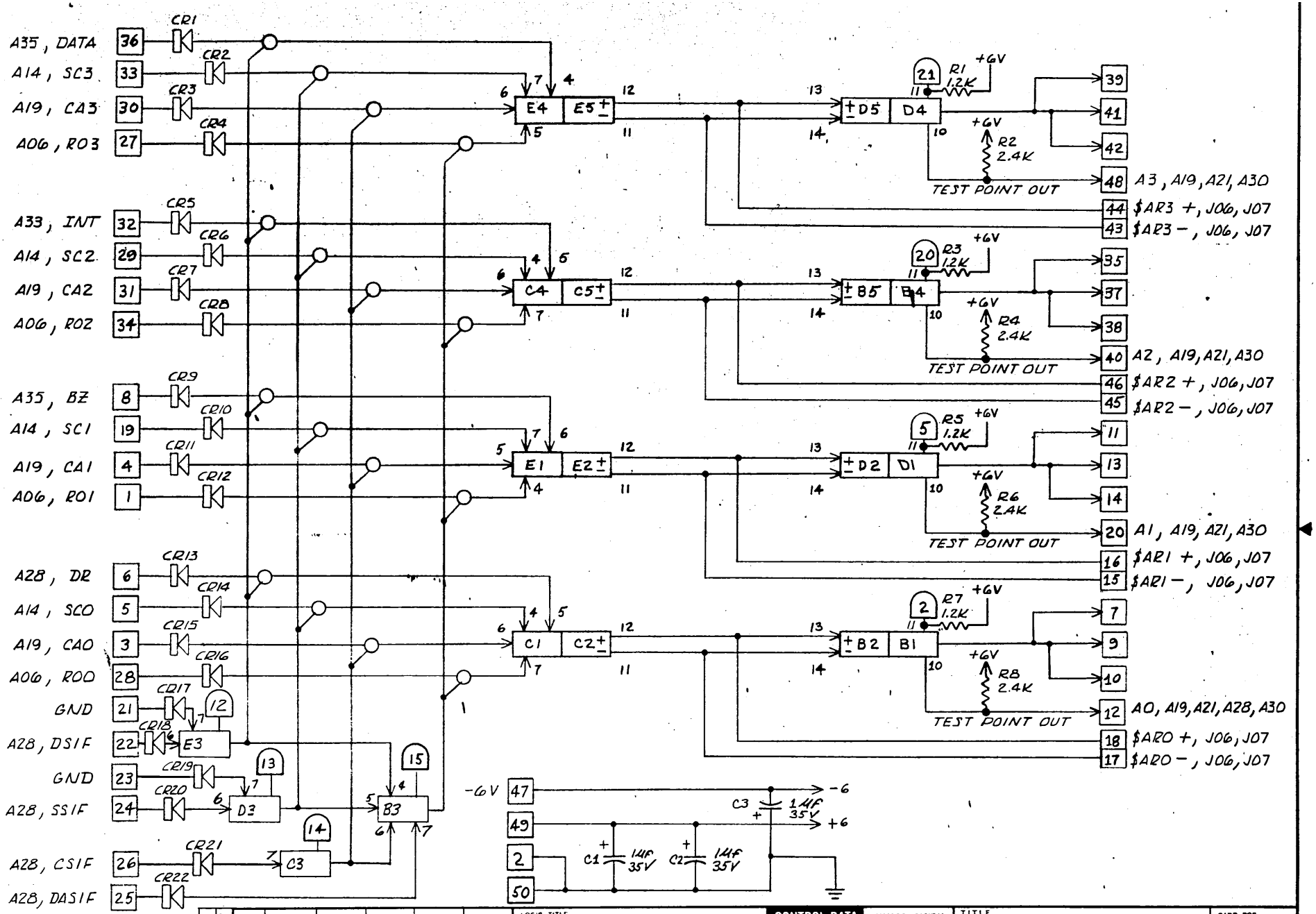
CARD POS.: B09

LOGIC TYPE: 1LKT

CODE IDENT NO.: C 09132

DRAWING NUMBER: 39745600

SHEET 41 OF



NOTES: UNLESS OTHERWISE SPECIFIED

DR 39709300 DETACHED LISTS

	A	B	C	D	E
1		R01B	T01A	R01B	T01A
2		R01A	T31B	R01A	T31B
3		I48M	I48M	I48M	I48M
4		R01B	T01A	R01B	T01A
5		R01A	T31B	R01A	T31B
6					

LOGIC TITLE: 3/4/4 GATED TRANSCEIVER, TTL

LOGIC DWG NO: 39709300 REV: A

PWA NO: 39709200 PWB NO: 39709100

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	B. Roberts	4-29-71
CHK	G. Lage	5-3-71
ENGR		
MFG		
APPD		

TITLE: A-REGISTER INTERFACE BITS 0-3

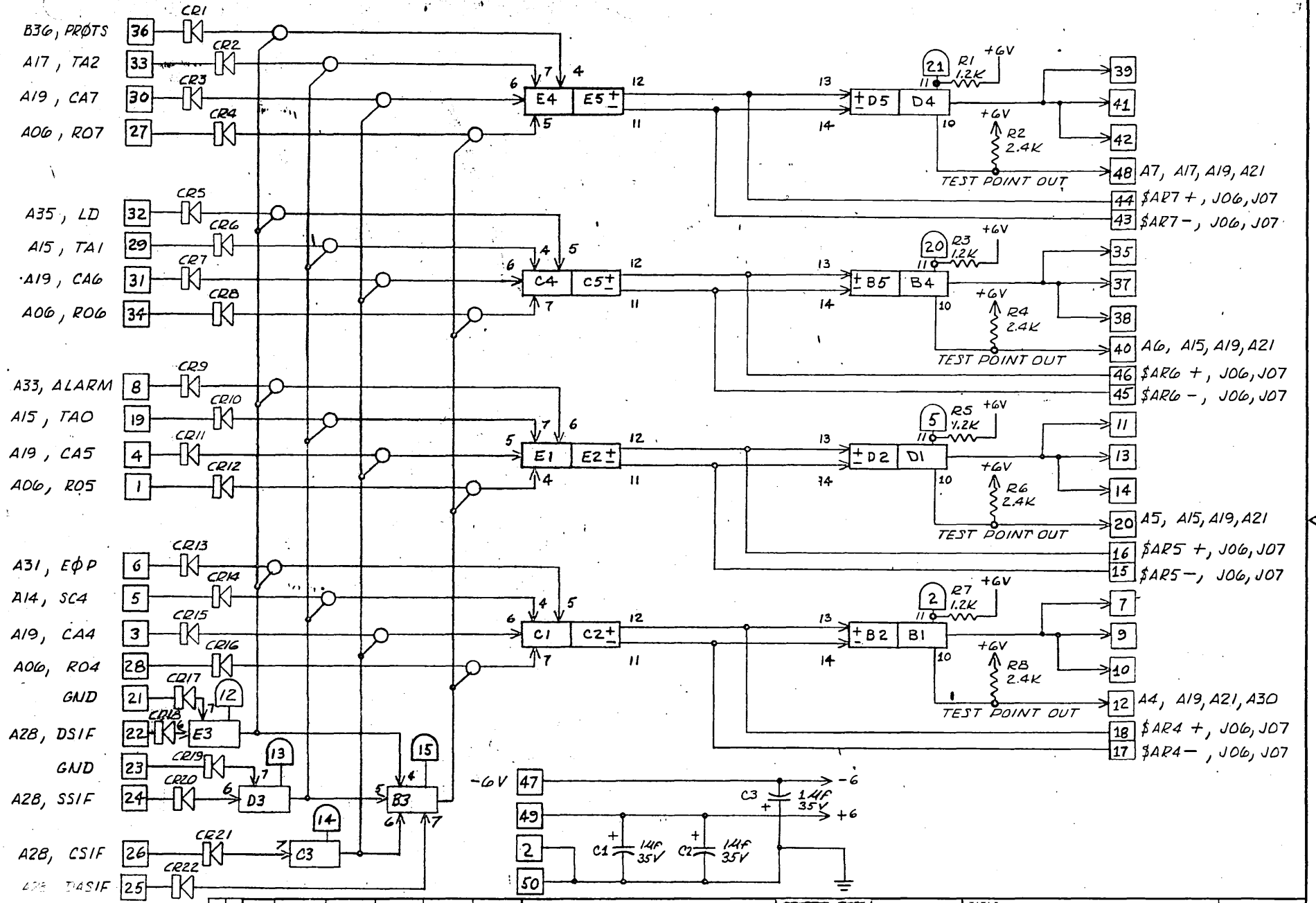
CARD POS.: B11

LOGIC TYPE: 1LKT

CODE IDENT NO.: C 09132

DRAWING NUMBER: 39745600 REV: B

SHEET 42 OF



DR 39709300 DETACHED LISTS	A	B	C	D	E
1		RO1B	TO1A	RO1B	TO1A
2		RO1A	T31B	RO1A	T31B
3		I48M	I48M	I48M	I48M
4		RO1B	TO1A	RO1B	TO1A
5		RO1A	T31B	RO1A	T31B
6					

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: 3/4/4 GATED TRANSCEIVER, TTL

LOGIC DWG NO: 39709300 REV: A

PWA NO: 39709200 PWB NO: 39709100

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	B. Roberts	4-29-71
CHK	G. Tagg	5-3-71
ENGR		
MFG		
APPD		

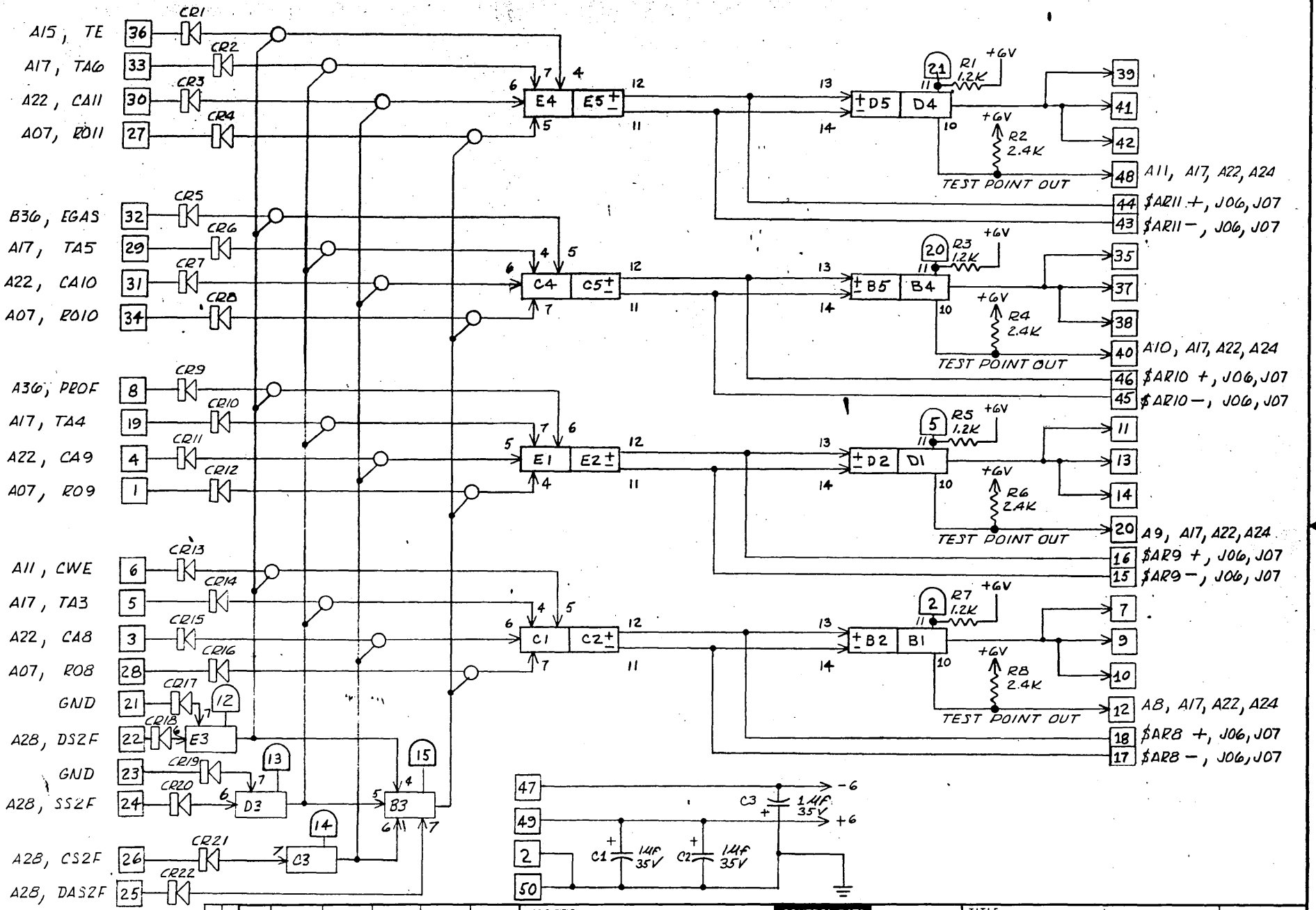
TITLE: A-REGISTER INTERFACE BITS 4 - 7

CARD POS: B12

LOGIC TYPE: 1LKT

C | CODE IDENT NO. 09132 | DRAWING NUMBER 39145600

SHEET 45 OF



	A	B	C	D	E
1		R01B	T01A	R01B	T01A
2		R01A	T31B	R01A	T31B
3		I48M	I48M	I48M	I48M
4		R01B	T01A	R01B	T01A
5		R01A	T31B	R01A	T31B
6					

DR 3970930O DETACHED LISTS

LOGIC TITLE: 3/4/4 GATED TRANSCEIVER, TTL

LOGIC DWG NO: 39709300 REV: A

PWA NO: 3970920 PWB NO: 39709100

CONTROL DATA ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037

FIRST USED ON		
DR	B. Roberts	4-29-71
CHK	G. Page	5-3-71
ENGR		
MFG		
APPD		

TITLE: A-REGISTER INTERFACE BITS 8-11

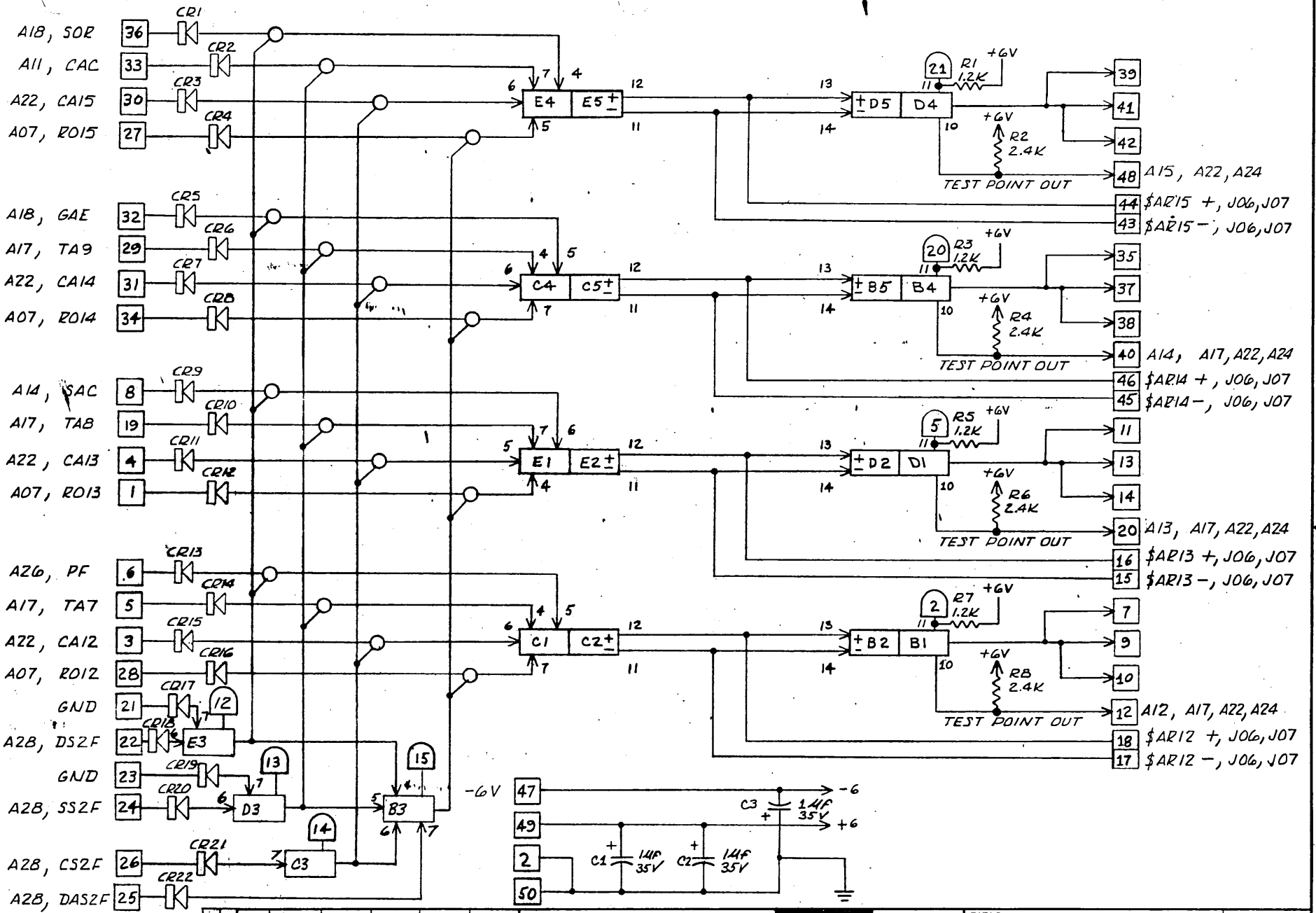
CARD POS.: B13

LOGIC TYPE: 1LKT

C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600

SHEET 44 OF

NOTES: UNLESS OTHERWISE SPECIFIED



	A	B	C	D	E
1		RO1B	TO1A	RO1B	TO1A
2		RO1A	T31B	RO1A	T31B
3		I48M	I48M	I48M	I48M
4		RO1B	TO1A	RO1B	TO1A
5		RO1A	T31B	RO1A	T31B
6					

DR 39709300
DETACHED LISTS

NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC TITLE: 3/4/4 GATED TRANSCEIVER, TTL

LOGIC DWG NO: 39709300 REV: A

PWA NO: 39709200 PWB NO: 39709100

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	B. Roberts	4-29-71
CHK	G. Page	5-3-71
ENGR		
MFG		
APPD		

TITLE: A-REGISTER INTERFACE BITS 12-15

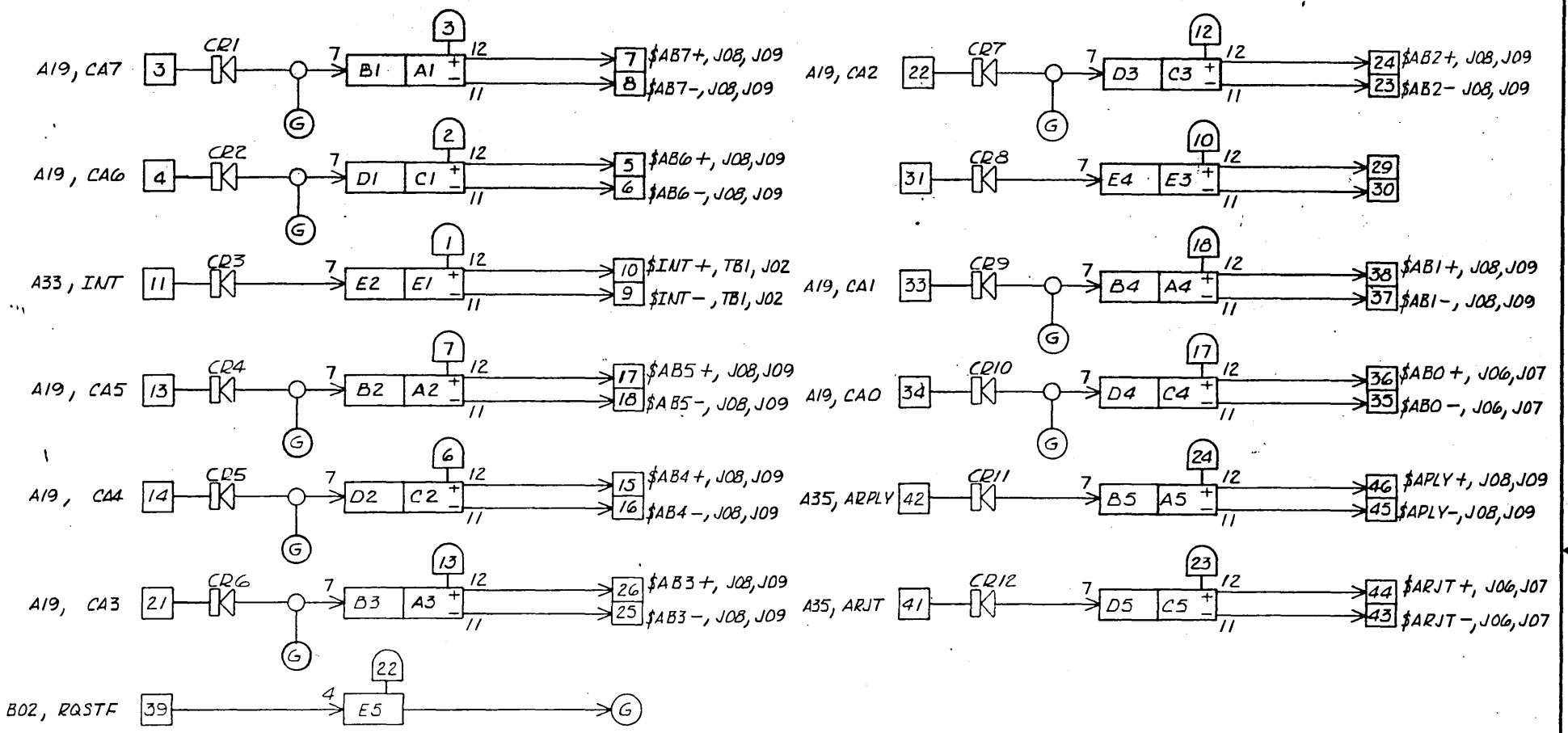
CARD POS.: B14

LOGIC TYPE: ILKT

CODE IDENT NO.: C 09132

DRAWING NUMBER: 39709300 REV: F

SHEET 45 OF



1. TEST POINT VOLTAGES:
LOGICAL "1" IN: TYPICAL 2.1V
LOGICAL "0" IN: TYPICAL 2.0V

NOTES: UNLESS OTHERWISE SPECIFIED

DETACHED LISTS DL 39709600

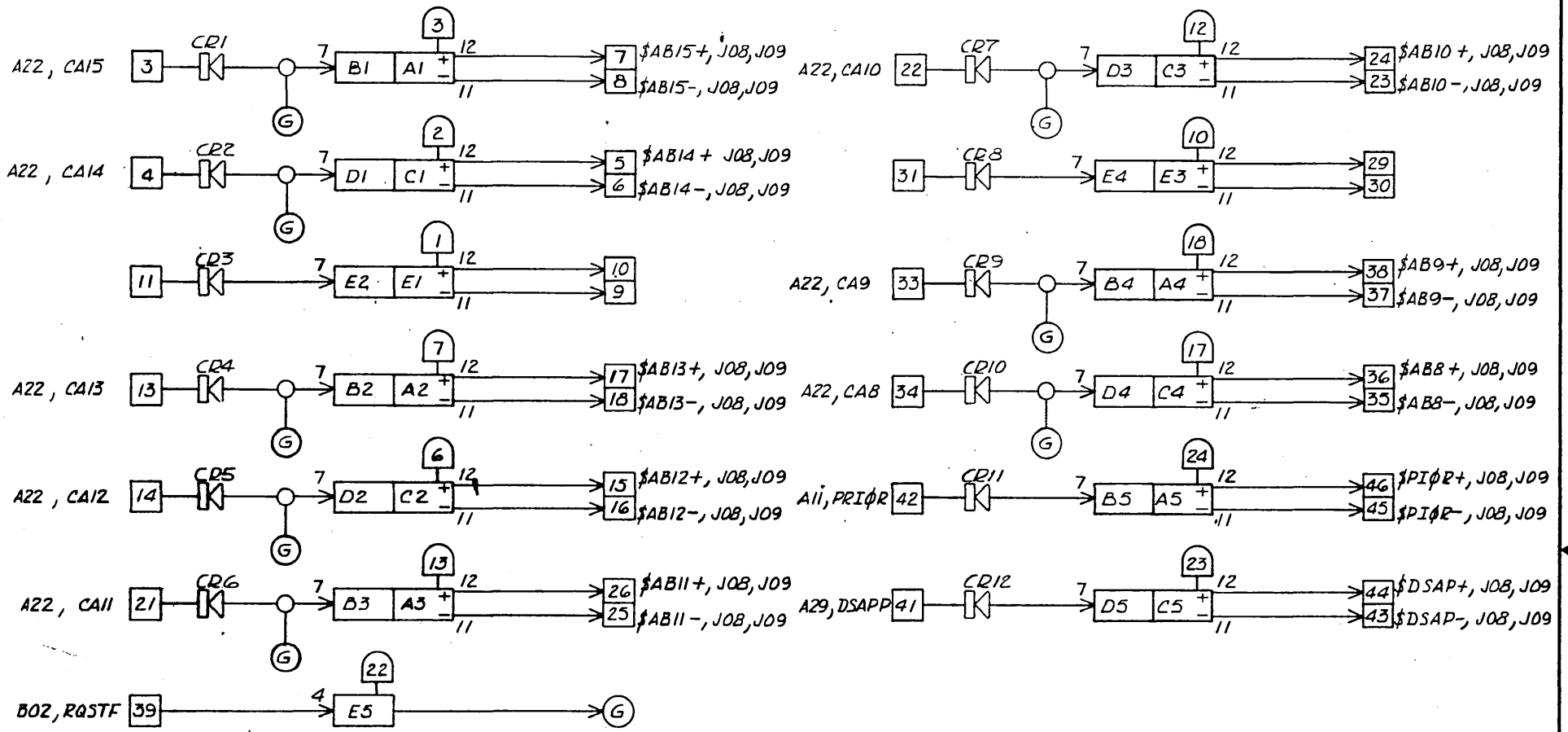
	A	B	C	D	E
1	T31B	T01A	T31B	T01A	T31B
2	T31B	T01A	T31B	T01A	T01A
3	T31B	T01A	T31B	T01A	T31B
4	T31B	T01A	T31B	T01A	T01A
5	T31B	T01A	T31B	T01A	I48M
6					

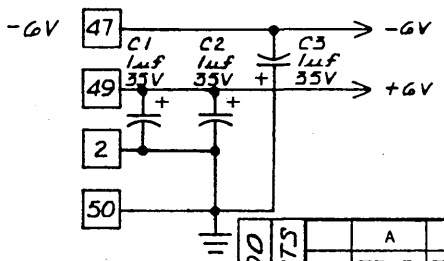
LOGIC TITLE: GENERAL PURPOSE TRANSMITTER, TTL
LOGIC DWG. NO.: 39709600 REV.: A
PWA NO.: 39709500 PWB NO.: 39709400

CONTROL DATA CORPORATION — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

FIRST USED ON		
DR	B. Roberts	4-23-71
CHK	A. Inge	4-26-71
ENGR		
MFG		
APPD		

TITLE: GENERAL PURPOSE TRANSMITTER, TTL
CARD POS.: B20
LOGIC TYPE: 1LLT
C
CODE IDENT NO.: 09132
DRAWING NUMBER: 39745600
SHEET 46 OF





1. TEST POINT VOLTAGES:
LOGICAL "1" IN: TYPICAL 2.1V
LOGICAL "0" IN: TYPICAL 2.0V

NOTES: UNLESS OTHERWISE SPECIFIED

DR 3709600 DETACHED LISTS

	A	B	C	D	E
1	T31B	T01A	T31B	T01A	T31B
2	T31B	T01A	T31B	T01A	T01A
3	T31B	T01A	T31B	T01A	T31B
4	T31B	T01A	T31B	T01A	T01A
5	T31B	T01A	T31B	T01A	I48M
6					

LOGIC TITLE: GENERAL PURPOSE TRANSMITTER, TTL

LOGIC DWG. NO.: 39709600 REV.: A

PWA NO.: 39709500 PWB NO.: 39709400

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

	FIRST USED ON		
DR		B. Roberts	4-23-71
CHK		B. Segre	4-26-71
ENGR			
MFG			
APPD			

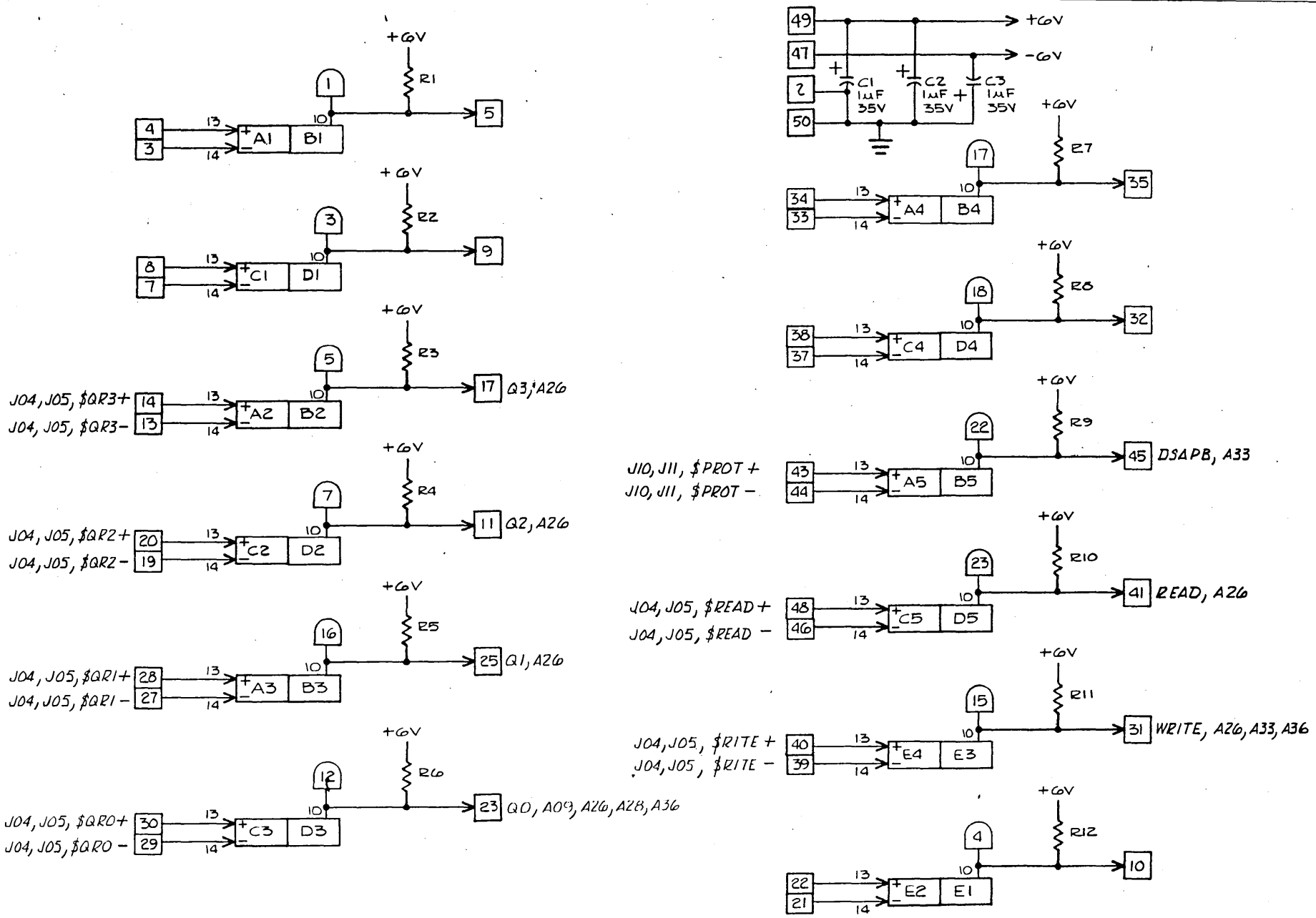
TITLE: GENERAL PURPOSE TRANSMITTER, TTL.

CARD POS.: B21

LOGIC TYPE: 1LLT

C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600

SHEET 47 OF



1. ALL RESISTORS ARE 2.4K 1/8W C.C.

NOTES: UNLESS OTHERWISE SPECIFIED

DR 39709900

DETACHED LIST

	A	B	C	D	E
1	R01A	R01B	R01A	R01B	R01B
2	R01A	R01B	R01A	R01B	R01A
3	R01A	R01B	R01A	R01B	R01B
4	R01A	R01B	R01A	R01B	R01A
5	R01A	R01B	R01A	R01B	
6					

LOGIC TITLE: GENERAL PURPOSE RECEIVER, TTL

LOGIC DWG. NO.: 39709900 REV.: A

PWA NO.: 39709800 PWB NO.: 39709700

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

	FIRST USED ON	
DR	BROWN	4-23-71
CHK	L. Page	4-23-71
ENGR		
MFG		
APPD		

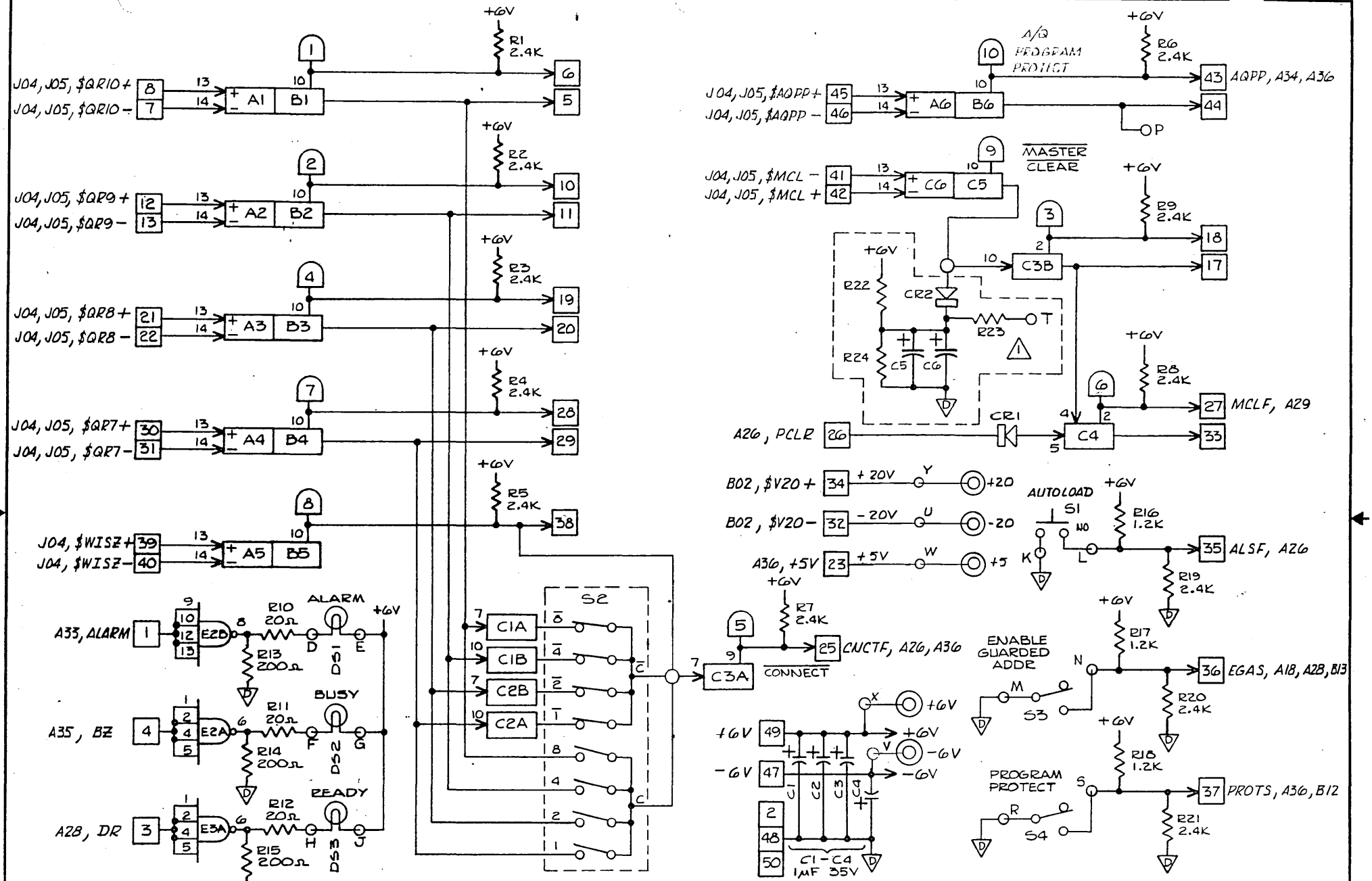
TITLE: MISC RECEIVERS

CARD POS.: B26

LOGIC TYPE: ILMT

C | CODE IDENT NO.: 09132 | DRAWING NUMBER: 39745600

SHEET 48 OF



⚠ PROVISION FOR THESE COMPONENTS ON THE PWB.

NOTES: UNLESS OTHERWISE SPECIFIED

DR 39708700 DETACHED LIST

	A	B	C	D	E
1	R01A	R01B	D34M		
2	R01A	R01B	D34M		844
3	R01A	R01B	D34M		844
4	R01A	R01B	I48M		
5	R01A	R01B	R01B		
6	R01A	R01B	R01A		

LOGIC TITLE: EQUIPMENT SELECT, TTL

LOGIC DWG. NO: 39708700 REV: A

PWA NO: 39708600 PWB NO: 39708500

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION, La Jolla, Calif. 92037

	FIRST USED ON	
DR	B HOEGMAN	4-29-71
CHK	[illegible]	4-30-71
ENGR		
MFG		
APPD		

TITLE: EQUIPMENT SELECT, TTL

CARD POS.: B36

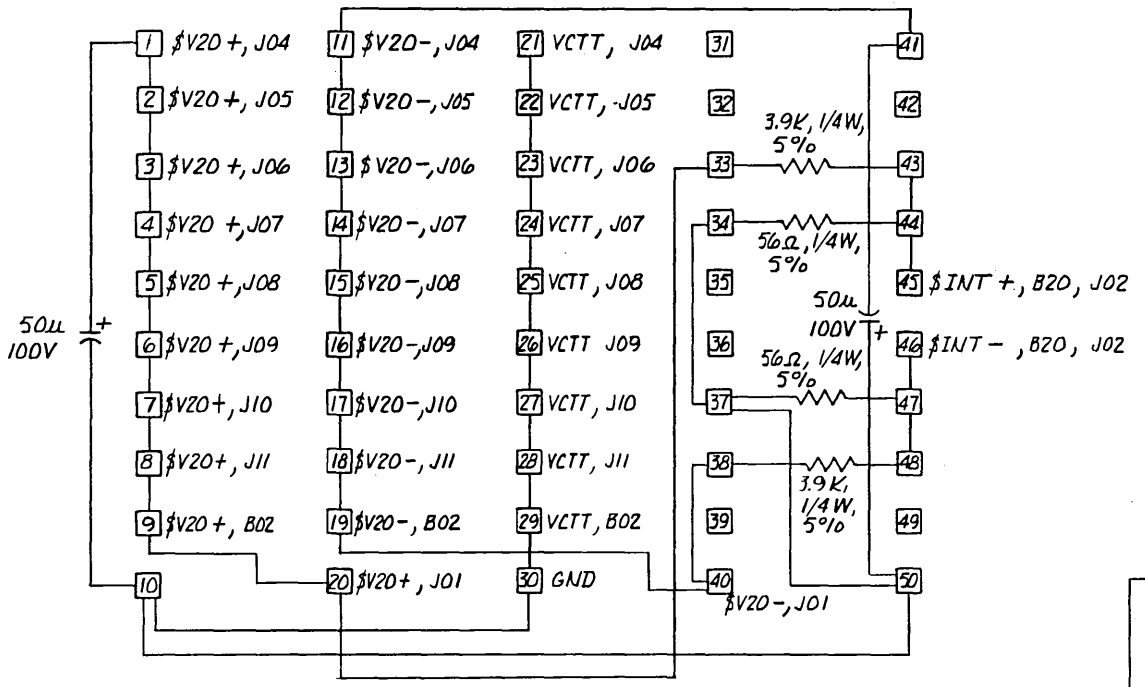
LOGIC TYPE: ILHT

CODE IDENT NO.: C 09132

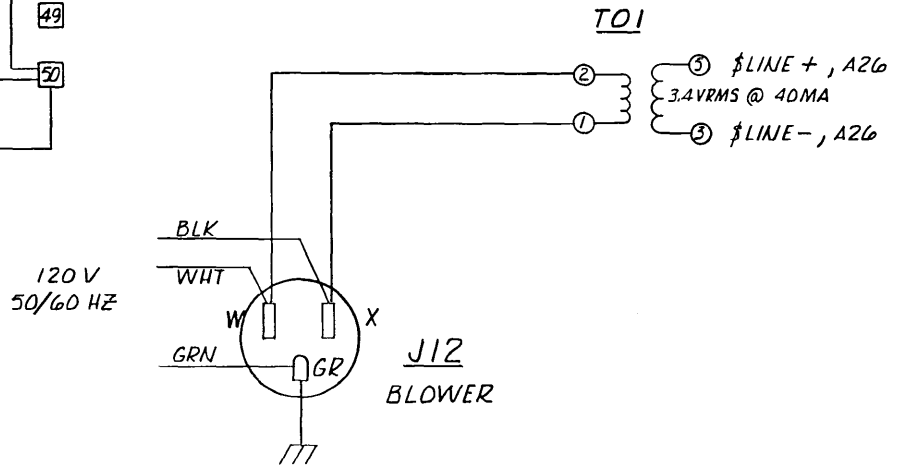
DRAWING NUMBER: 39145600 REV: B

SHEET 49 OF

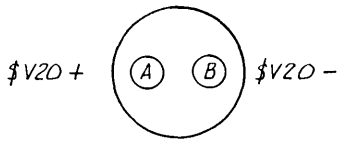
REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD



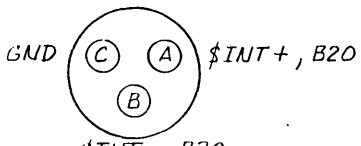
TB1



J12
BLOWER



J01
TERMINATOR POWER



$INT−, B20
J02
INTERRUPT

REFERENCE DRAWINGS			
COMPONENTS, EXCEPT AS NOTED	TOLERANCE	VALUE	RATING
RES			
CAP.			

CONTROL DATA CORPORATION
ANALOG - DIGITAL SYSTEMS DIVISION
La Jolla, Calif. 92037

FIRST USED ON		
DR	T. Cyman	6-14-71
CHK		
ENGR		
MFG		
APPD		

TITLE
J01, J02, J12, TB1 & TO1

SIZE	CODE IDENT NO.	DRAWING NUMBER	REV
C	09132	39745600	B

SHEET 50 OF

4 3 2 1

1 $BC+ A26	2 $BC- A26	27 $TA5+ A15	28 $TA5- A15
3 $ØM+ A14, A12, A15, A26	4 $ØM- A14	29 $TA6+ A15	30 $TA6- A15
5 $WEF+ A12	6 $WEF- A12	31 $TA7+ A15	32 $TA7- A15
7 $WDIS+ A26	8 $WDIS- A26	33 $TA8+ A15	34 $TA8- A15
9 $WD+ J03	10 $WD- J03	35 $TA9+ A15	36 $TA9- A15
11 $RD+ A11	12 $RD- A11	37 $DRF+ A26, A28, A33	38 $DRF- A26
13 $SM+ A14, A11, A12, A15, A26	14 $SM- A14	39	40
15 $HWM+, A14, A12, A15	16 $HWM- A14	41	42
17 $TA0+ A15	18 $TA0- A15	43	44
19 $TA1+ A15	20 $TA1- A15	45	46
21 $TA2+ A15	22 $TA2- A15	47	48
23 $TA3+ A15	24 $TA3- A15	49	50
25 $TA4+ A15	26 $TA4- A15		

CONNECTOR

CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE J03
DRUM CONNECTOR

CARD POS.

MODEL	DWG. NO.	REV.	SHEET	PAGE
	30[illegible]	B	51	

A1 $QR0+ J05,B26	A2 $QR0- J05,B26	D3 $READ+ B26	D4 $READ- B26
A3 $QR1+ J05,B26	A4 $QR1- J05,B26	D5 $RITE+ J05,B26	D6 $RITE- J05,B26
A5 $QR2+ J05,B26	A6 $QR2- J05,B26	D7 $MCL+ B36	D8 $MCL- B36
A7 $QR3+ J05,B26	A8 $QR3- J05,B26	D9 $AQPP+ B36	D10 $AQPP- B36
A9 $QR4+ J05	A10 $QR4- J05	E1 $BUFF+ J05	E2 $BUFF- J05
B1 $QR5+ J05	B2 $QR5- J05	E3 $TIME+ J05	E4 $TIME- J05
B3 $QR6+ J05	B4 $QR6- J05	E5	E6
B5 $QR7+ J05,B36	B6 $QR7- J05,B36	E7	E8
B7 $QR8+ J05,B36	B8 $QR8- J05,B36	E9	E10
B9 $QR9+ J05,B36	B10 $QR9- J05,B36	F1	F2
C1 $QR10+ J05,B36	C2 $QR10- J05,B36	F3	F4
C3 $QR11+ J05	C4 $QR11- J05	F5	F6
C5 $QR12+ J05	C6 $QR12- J05	F7 $WISZ+ J05,B36	F8 $WISZ- J05,B36
C7 $QR13+ J05	C8 $QR13- J05	F9 V20+ TB1	F10 V20- TB1
C9 $QR14+ J05	C10 $QR14- J05	CTR VCTT TB1	
D1 $QR15+ J05	D2 $QR15- J05		

CONNECTOR

CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE: J04, AQ ADDRESS IN CONNECTOR

CARD POS.

MODEL	DWG. NO.	REV.	SHEET	PAGE
	3974560	A	52	

A1 $QR0+ J04,B26	A2 $QR0- J04,B26	D3 $READ+ B26	D4 $READ- B26
A3 $QR1+ J04,B26	A4 $QR1- J04,B26	D5 $RITE+ J04,B26	D6 $RITE- J04,B26
A5 $QR2+ J04,B26	A6 $QR2- J04,B26	D7 $MCL+ B36	D8 $MCL- B36
A7 $QR3+ J04,B26	A8 $QR3- J04,B26	D9 $AQPP+ B36	D10 $AQPP- B36
A9 $QR4+ J04	A10 $QR4- J04	E1 $BUFF+ J04	E2 $BUFF- J04
B1 $QR5+ J04	B2 $QR5- J04	E3 $TIME+ J04	E4 $TIME- J04
B3 $QR6+ J04	B4 $QR6- J04	E5	E6
B5 $QR7+ J04,B36	B6 $QR7- J04,B36	E7	E8
B7 $QR8+ J04,B36	B8 $QR8- J04,B36	E9	E10
B9 $QR9+ J04,B36	B10 $QR9- J04,B36	F1	F2
C1 $QR10+ J05,B36	C2 $QR10- J05,B36	F3	F4
C3 $QR11+ J04	C4 $QR11- J04	F5	F6
C5 $QR12+ J04	C6 $QR12- J04	F7 $WISZ+ J04,B36	F8 $WISZ- J04,B36
C7 $QR13+ J04	C8 $QR13- J04	F9 V20+ TB1	F10 V20- TB1
C9 $QR14+ J04	C10 $QR14- J04	CTR VCTT TB1	
D1 $QR15+ J04	D2 $QR15- J04		

CONNECTOR

CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE: J05, AQ ADDRESS QUT CONNECTOR

CARD POS.

MODEL	DWG. NO.	REV.	SHEET	PAGE
	3014560	A	53	

A1 $AR0+ B11	A2 $AR0- B11	D3 $APLY+ B20	D4 $APLY- B20
A3 $AR1+ B11	A4 $AR1- B11	D5 $ARJT+ B20	D6 $ARJT- B20
A5 $AR2+ B11	A6 $AR2- B11	D7 $CHIN+ J07	D8 $CHIN- J07
A7 $AR3+ B11	A8 $AR3- B11	D9 $APRI+ J07	D10 $APRI- J07
A9 $AR4+ B12	A10 $AR4- B12	E1	E2
B1 $AR5+ B12	B2 $AR5- B12	E3	E4
B3 $AR6+ B12	B4 $AR6- B12	E5	E6
B5 $AR7+ B12	B6 $AR7- B12	E7	E8
B7 $AR8+ B13	B8 $AR8- B13	E9	E10
B9 $AR9+ B13	B10 $AR9- B13	F1	F2
C1 $AR10+ B13	C2 $AR10- B13	F3	F4
C3 $AR11+ B13	C4 $AR11- B13	F5	F6
C5 $AR12+ B14	C6 $AR12- B14	F7	F8
C7 $AR13+ B14	C8 $AR13- B14	F9 V20+ TB1	F10 V20- TB1
C9 $AR14+ B14	C10 $AR14- B14	CTR VCTT TB1	
D1 $AR15+ B14	D2 $AR15- B14		

CONNECTOR

CONTROL DATA	TITLE J06, AQ DATA IN CONNECTOR				CARD POS.
LA JOLLA DIVISION La Jolla, California	MODEL	DWG. NO. 3974560	REV. 1	SHEET 54	PAGE

A1 $AR0+ B11	A2 $AR0- B11	D3 $APLY+ B20	D4 $APLY- B20
A3 $AR1+ B11	A4 $AR1- B11	D5 $ARJT+ B20	D6 $ARJT- B20
A5 $AR2+ B11	A6 $AR2- B11	D7 $CHIN+ J06	D8 $CHIN- J06
A7 $AR3+ B11	A8 $AR3- B11	D9 $APRI+ J06	D10 $APRI- J06
A9 $AR4+ B12	A10 $AR4- B12	E1	E2
B1 $AR5+ B12	B2 $AR5- B12	E3	E4
B3 $AR6+ B12	B4 $AR6- B12	E5	E6
B5 $AR7+ B12	B6 $AR7- B12	E7	E8
B7 $AR8+ B13	B8 $AR8- B13	E9	E10
B9 $AR9+ B13	B10 $AR9- B13	F1	F2
C1 $AR10+ B13	C2 $AR10- B13	F3	F4
C3 $AR11+ B13	C4 $AR11- B13	F5	F6
C5 $AR12+ B14	C6 $AR12- B14	F7	F8
C7 $AR13+ B14	C8 $AR13- B14	F9 V20+ TB1	F10 V20- TB1
C9 $AR14+ B14	C10 $AR14- B14	CTR VCTT TB1	
D1 $AR15+ B14	D2 $AR15- B14		

CONNECTOR

CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE: J07, AQ DATA QUAD CONNECTOR

CARD POS.

MODEL	DWG. NO.	REV.	SHEET	PAGE
	39145600	A	55	

A1 $ABO+ B20	A2 $ABO- B20	D3 $PIØR+ B21, J09	D4 $PIØR - B21, J09
A3 $AB1+ B20	A4 $AB1- B20	D5 $DSAP+ J09, B21	D6 $DSAP - J09, B21
A5 $AB2+ B20	A6 $AB2- B20	D7 $RØST+ J09, B02	D8 $RQST- J09, B02
A7 $AB3+ B20	A8 $AB3- B20	D9 $WREN+ J09, B02	D10 $WREN - J09, B02
A9 $AB4+ B20	A10 $AB4- B20	E1 $DMCL+ J09	E2 $DMCL - J09
B1 $AB5+ B20	B2 $AB5- B20	E3 $NT9+ J09	E4 $NT9 - J09
B3 $AB6+ B20	B4 $AB6- B20	E5 $NT10+ J09	E6 $NT10 - J09
B5 $AB7+ B20	B6 $AB7- B20	E7 $NT11+ J09	E8 $NT11 - J09
B7 $AB8+ B21	B8 $AB8- B21	E9 $NT12+ J09	E10 $NT12- J09
B9 $AB9+ B21	B10 $AB9- B21	F1 $NT13+ J09	F2 $NT13- J09
C1 $AB10+ B21	C2 $AB10- B21	F3 $AB15+ B21	F4 $AB15- B21
C3 $AB11+ B21	C4 $AB11- B21	F5 $NT15+ J09	F6 $NT15- J09
C5 $AB12+ B21	C6 $AB12- B21	F7 $SCN2+ B02	F8 SSCN2- B02
C7 $AB13+ B21	C8 $AB13- B21	F9 $V20+ TB1	F10 $V20- TB1
C9 $AB14+ B21	C10 $AB14- B21	CTR VCTT TB1	
D1 $SCN1+ B02	D2 $SCN1- B02		

CONNECTOR

CONTROL DATA CORPORATION LA JOLLA DIVISION La Jolla, California	TITLE JOB DSA ADDRESS IN CONNECTOR			CARD POS.
	MODEL	DWG. NO. 3974561	REV. 7	SHEET 56
				PAGE

A1	$AB0+ B20	A2	$AB0- B20	D3	$PIOT+ B21, J08	D4	$PIOR- B21, J08
A3	$AB1+ B20	A4	$AB1- B20	D5	$DSAP+ J08, B21	D6	$DSAP- J08, B21
A5	$AB2+ B20	A6	$AB2- B20	D7	$RQST+ J08, B02	D8	$RQST- J08, B02
A7	$AB3+ B20	A8	$AB3- B20	D9	$WREN+ J08, B2	D10	$WREN- J08, B2
A9	$AB4+ B20	A10	$AB4- B20	E1	$DMCL+ J08	E2	$DMCL- J08
B1	$AB5+ B20	B2	$AB5- B20	E3	$NT9+ J08	E4	$NT9- J08
B3	$AB6+ B20	B4	$AB6- B20	E5	$NT10+ J08	E6	$NT10- J08
B5	$AB7+ B20	B6	$AB7- B20	E7	$NT11+ J08	E8	$NT11- J08
B7	$AB8+ B21	B8	$AB8- B21	E9	$NT12+ J08	E10	$NT12- J08
B9	$AB9+ B21	B10	$AB9- B21	F1	$NT13+ J08	F2	$NT13- J08
C1	$AB10+ B21	C2	$AB10- B21	F3	$AB15+ B21	F4	$AB15- B21
C3	$AB11+ B21	C4	$AB11- B21	F5	$NT15+ J08	F6	$NT15- J08
C5	$AB12+ B21	C6	$AB12- B21	F7	$SCN3+ B02	F8	$SCN3- B02
C7	$AB13+ B21	C8	$AB13- B21	F9	$V20+ TB1	F10	$V20- TB1
C9	$AB14+ B21	C10	$AB14- B21	CTR	VCTT TB1		
D1	$SCN4+ B02	D2	$SCN4- B02				

CONNECTOR

CONTROL DATA CORPORATION
LA JOLLA DIVISION
La Jolla, California

TITLE: J09, USA ADDRESS CUIT CONNECTOR

CARD POS.

MODEL	DWG. NO.	REV.	SHEET	PAGE
	39145600	A	57	

A1 $DBO + J11, B06	A2 $DBO- J11, B26	D3 $SP+ J11	D4 $SP- J11
A3 $DB1 + J11, B06	A4 $DB1- J11, B06	D5 $PRØT + B26	D6 $PRØT- B26
A5 SDB2+ J11, B06	A6 $DB2- J11, B06	D7 $RPLY+ J11, B02	D8 $RPLY- J11, B02
A7 $DB3+ J11, B06	A8 $DB3- J11, B06	D9 $SPE+ J11	D10 $SPE- J11
A9 $DB4 + J11, B07	A10 $DB4- J11, B07	E1 $PPF + J11	E2 $PP- J11
B1 $DB5+ J11, B07	B2 $DB5 - J11, B07	E3 $NT1 + J11	E4 $NT1- J11
B3 $DB6+ J11, B07	B4 $DB6- J11, B07	E5 $NT2 + J11	E6 $NT2- J11
B5 $DB7+ J11, B07	B6 $DB7- J11, B07	E7 $NT3+ J11	E8 $NT3- J11
B7 SDB8+ J11, B08	B8 $DB8- J11, B08	E9 $NT4+ J11	E10 $NT4- J11
B9 $DB9+ J11, B08	B10 $DB9- J11, B08	F1 $NT5 + J11	F2 $NT6- J11
C1 $DB10+ J11, B08	C2 $DB10- J11, B08	F3 $NT6+ J11	F4 $NT6- J11
C3 $DB11 + J11, B08	C4 $DB11- J11, B08	F5 $NT7+ J11	F6 $NT7- J11
C5 $DB12+ J11, B09	C6 $DB12- J11, B09	F7 $NT8+ J11	F8 $NT8- J11
C7 $DB13+ J11, B09	C8 $DB13- J11, B09	F9 $V20+ TB1	F10 $V20- TB1
C9 $DB14+ J11, B09	C10 $DB14- J11, B09	CTR VCTT TB1	
D1 $DB15+ J11, B09	D2 $DB15- J11, B09		

CONNECTOR

CONTROL DATA
LA JOLLA DIVISION
La Jolla, California

TITLE J10
DSA DATA
IN CONNECTOR

CARD POS.

MODEL | DWG. NO. 397456 | REV. A | SHEET 58 | PAGE

A1 $DB0+ J10, B6	A2 $DB0- J10, B6	D3 $SP+ J10	D4 $SP- J10
A3 $DB1+ J10, B6	A4 $DB1- J10, B6	D5 $PRØT+ B26	D6 $PRØT- B26
A5 $DB2+ J10, B6	A6 $DB2- J10, B6	D7 $RPLY+ J10, B02	D8 $RPLY- J10, B02
A7 $DB3+ J10, B6	A8 $DB3- J10, B6	D9 $SPE+ J10	D10 $SPE- J10
A9 $DB4+ J10, B7	A10 $DB4- J10, B7	E1 $PPF+ J10	E2 $PPF- J10
B1 $DB5+ J10, B7	B2 $DB5- J10, B7	E3 $NT1+ J10	E4 $NT1- J10
B3 $DB6+ J10, B7	B4 $DB6- J10, B7	E5 $NT2+ J10	E6 $NT2- J10
B5 $DB7+ J10, B7	B6 $DB7- J10, B7	E7 $NT3+ J10	E8 $NT3- J10
B7 $DB8+ J10, B8	B8 $DB8- J10, B8	E9 $NT4+ J10	E10 $NT4- J10
B9 $DB9+ J10, B8	B10 $DB9- J10, B8	F1 $NT5+ J10	F2 $NT5- J10
C1 $DB10+ J10, B8	C2 $DB10- J10, B8	F3 $NT6+ J10	F4 $NT6- J10
C3 $DB11+ J10, B8	C4 $DB11- J10, B8	F5 $NT7+ J10	F6 $NT7- J10
C5 $DB12+ J10, B9	C6 $DB12- J10, B9	F7 $NT8+ J10	F8 $NT8- J10
C7 $DB13+ J10, B9	C8 $DB13- J10, B9	F9 $V20+ TB1	F10 $V20- TB1
C9 $DB14+ J10, B9	C10 $DB14- J10, B9	CTR VCTT TB1	
D1 $DB15+ J10, B9	D2 $DB15- J10, B9		

CONNECTOR

CONTROL DATA CORPORATION LA JOLLA DIVISION La Jolla, California	TITLE J1 DSA DATA CABLE CONNECTOR			CARD POS.
MODEL	DWG. NO. 39745600	REV. A	SHEET 59	PAGE

Appendix B

BG504A/H DRUM MEMORY SUBSYSTEM DIAGNOSTIC

The document presented in this appendix is a CDC Programming Specification identified as 39932200. The document is complete within itself and has not been renumbered to agree with page and paragraph numbers of this manual.

EXTERNAL REFERENCE SPECIFICATION

SMM17 V3.0 TEST NO. 80

BG504A/H DRUM

APPLICATION SOFTWARE PRODUCT

The software product described herein was developed by the La Jolla Systems Division for specific applications and is not supported by Control Data Corporation as a standard product. It is available only on an individual system quotation basis.

For information on standard software products, please consult the software configurator.

DISCLAIMER: THIS DOCUMENT IS A WORKING PAPER ONLY AND DOES NOT NECESSARILY REPRESENT ANY OFFICIAL INTENT ON THE PART OF CONTROL DATA CORPORATION.

[illegible signature]	G.E. Briggs	[illegible signature]	[illegible signature] 1-31-72		

REVISION RECORD

REV.	PAGE	PARAGRAPH	DATA	E.C.O.	APP.	DATE
A	All		Released	-		7/31/72

1.0 SCOPE

1.1 This specification describes the BG504A/H Drum Controller diagnostic. It will operate under the control of SMM17 V3.0 or above and has been assigned Test No. 80 in the SMM17 library list. The purpose of this specification is to describe the comprehensive set of test sections for both factory checkout and field maintenance.

2.0 APPLICABLE DOCUMENTS

2.1 Software

2.1.1 1500/VW SMM17 Software Subset of SMM17 V3.0.

2.1.2 SMM17 Manual Publication No. 60182000.

2.1.3 MBS subset of SMM17 V3.0 ERS.

2.2 Hardware

2.2.1 1700 Reference Manual Pub. No. 60153100

2.2.2 SC-1700 Reference Manual Pub. No. 60270600

2.2.3 BG504 Drum Subsystem Pub. No. 39731700

3.0 DESCRIPTION

3.1 Communication

3.1.1 Communication with the diagnostic will be through either 1) Console; 2) Teletype. Refer to latest SMM17 manual for loading information.

3.2 General Test Description

3.2.1 The following areas will be tested:

1. Functions
2. Status
3. Interrupts
4. Data
5. Alarms

3.2.2 The method of testing is to make each succeeding test section more complex, forming a bootstrapping-sequential technique aimed at reducing troubleshooting time. For example:

1. Sector, initial core and final core address registers will be verified prior to drum transfers.
2. All controller data registers will be verified prior to checking drum transfers.

3.2.3 The type of response (reply, reject) to all I/O instructions, except when reading status, will be verified against predicted values. This will include timer information to the nearest millisecond. For example, the controller may be busy, external reject, up to 17 millisec after initiating a write operation. The actual checking is performed in the monitor, the test supplies the data.

3.2.4 All four status words are copied after each function, read or write. The only exception is section two where only director and sector address status is copied. Although four status words are copied, only those applicable to the I/O operation will be verified.

3.2.5 To verify all 8 alarm conditions it will be necessary to "bug" specific logic areas. To achieve this a card extender and clipped lead are required. Although this procedure is primarily used by Q.A., it can be helpful both in checkout and in the field.

3.2.6 Preset Input Parameters

	A	Q
Stop 1	8051	0201
Stop 2	0FDE	0200
Stop 3	4500	0000
Stop 4	0000	0000
Stop 5	5A5A	8060

3.2.6.1 Refer to latest edition of SMM17 reference manual for an explanation of Stop 1.

3.2.6.2 Stop 2 Sections

(A) BIT

0	Bit clock adjust procedure/buffer addresses
1	Sector address counter
2	Initial sector address register/sector address compare
3	Initial and final core address/core address compare
4	Sector overrange/data registers
5	Guarded address
6	Serialize test
7	Worst case patterns
8	C. E. section (manipulative)
9	Auto load/protect
10	Checkword check
11	Clear timing error
12	Not used
13	Not used
14	"ON" = 50 Hz, "OFF" = 60 Hz
15	Indicates the maintenance bell troubleshooting aid. If set, the teletype bell will be rung prior to each error message. It is to be used in conjunction with the omit typeouts and repeat conditions features as an aid to isolating intermittant errors.

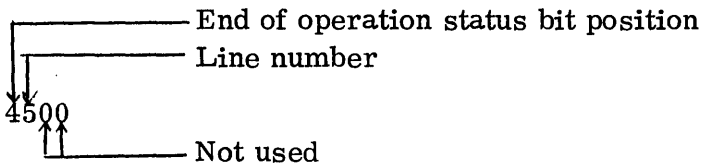
(Q) Number of tracks (drum size). Bit 06=64 tracks, bit 07=128 tracks, etc.

3.2.6.3 Stop 3

(A) Interrupt data in the form BLBL.

B = bit position in director status

L = Line number



(Q) = 0

3.2.6.4 Stop 4

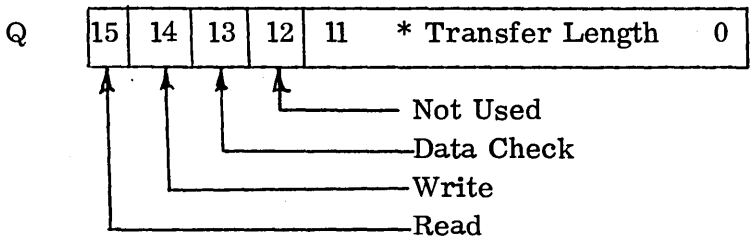
(A) Bits 0-14 = first available track/sector address.

(Q) = Highest guarded track address.

3.2.6.5 Stop 5

(A) Section 4, 8 data pattern

(Q) Section 8 control



*Transfer length: Max. = 3072 (1 track)

Min. = 1 word

3.3 I/O CYCLE

3.3.1 The I/O cycle is a collection of monitor calls, common to all test sections.

All I/O requests to the monitor including status, function output, read, write, status and interrupt timing are grouped in a specific order and located near the beginning of the test. It is called as a subroutine with the name tag "IOCYL".

All function requests result in an "early I/O Cycle exit". Requests for data transfers complete the I/O cycle, see flow chart.

3.3.2 The following monitor calls are used in the I/O Cycle:

Monitor Subroutine	Description	I/O Cycle Pointer No.	Monitor Error No.(s)
Check Status	Copy and check requested no. of status words against predicted values.	X0	0003
Function	Output values to load ICA, FCA and ISA registers. Begin copying status 60us after output. Reply to output instruction is verified against the predicted reply. External reject (if any) timing is checked. Maximum time to wait = 32,767 milliseconds.	X1	0001, 0002
Read/Write	Initiate read or write operation. Response and timing same as Function. Begin copying status approx. 100us after output.	X6/X7	0001, 0002
Recheck	Verify last status(s) copied against predicted values.	X2	0003

Monitor Subroutine	Description	I/O Cycle pointer no.	Monitor Error no.
Recognize Interrupt	Copy and check all requested status while waiting for an interrupt. Control is passed to the monitor while waiting.	X3	0003, 0004
Monitor Status	Copy and check all requested status while waiting for a specific status bit to change state within a specified time. The last status(s) copied which saw the bit change is not verified.	X4	0000, 0003
Recheck	Same as above.	X5	0003
Select Interrupt	Makes the occurrence of an interrupt legal to the monitor.	NONE	NONE
Deselect Interrupt	Makes the occurrence of an interrupt illegal.	NONE	NONE

3.3.3 Interrupt Processor

The interrupt processor, like the test sections, uses the I/O Cycle to acknowledge interrupts. The I/O Cycle pointer no. for Check Status, Function and (1st) Recheck Status is changed to X8, X9 and XA respectively. Error messages are shorter for acknowledge interrupt because only the 1st two status words are copied.

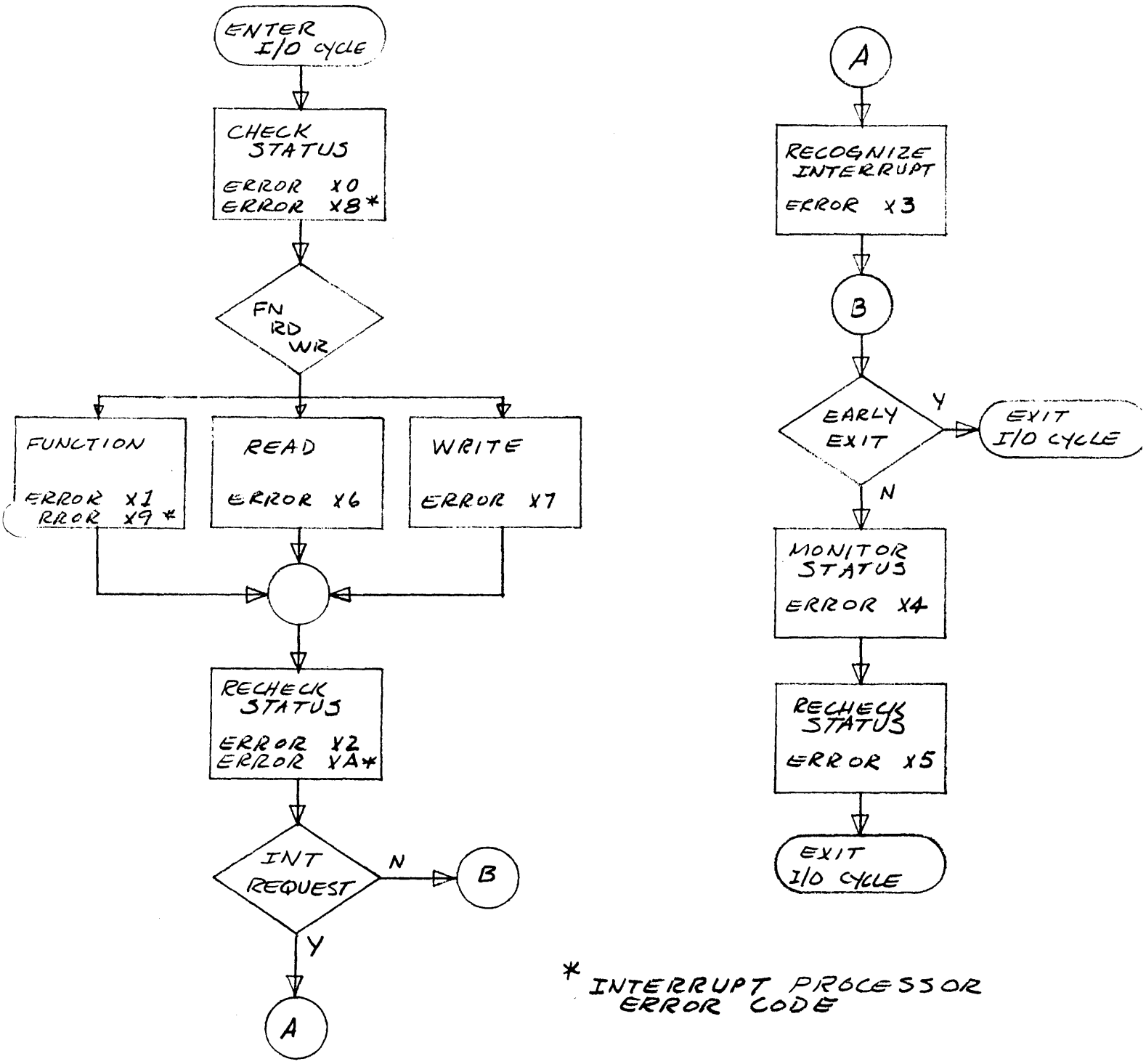
Alarm interrupts results in the following:

1. Clear controller
2. Enable or disable end of operation and/or alarm interrupt as requested by the test section.
3. Deselect the line to the monitor thereby making the occurrance of an interrupt illegal. The line is reselected prior to the next request for a data transfer.

CONTROL DATA CORPORATION

PROGRAMMING SPECIFICATION

LA JOLLA SYSTEMS DIVISION



* INTERRUPT PROCESSOR ERROR CODE

TITLE DRUM I/O CYCLE			DRG. NO.
			REVISION
DRAWN BY M S SATTER	PROJ.	DATE	SHEET 1 OF 1

CSD 203 ANALYSIS

End of operation interrupt results in 2 and 3 of the above.

3.4 INITIALIZE

3.4.1 A task of the section search routine, located at the beginning of the test, is to initialize each section prior to passing control to that section.

Initialize performs the following sequence of operations:

1. Adjust timing values if connected to 50Hz power.
2. Clear all status calls (except last Recheck Status) in the I/O Cycle.
3. I/O Cycle switches:
   a) set early exit
   b) set function
   c) clear interrupt
4. Set error code to zero (SSEE).
5. Direct monitor to copy status 1 and 2 only. See 6.0 for status description.
6. Set 1st Recheck Status, status 1 value to expect ready and data.
7. Execute clear controller.
8. Direct monitor to copy all 4 status words.
9. Set Check Status, status 1 value to expect ready and data.
10. Return to section search routine.

3.5 Error detection reporting

3.5.1 The test uses 6 monitor subroutines to perform the following operations.

1. Execute I/O
   a) Read
   b) Write
   c) Function
2. Process interrupts
3. Copy status
4. Check status
5. Monitor status
6. Detect errors

The test calls these subroutines from a common area near the front of the test. The sequence of calls is referred to as the "I/O CYCLE", see the I/O cycle flow chart. The monitor supplies the error type number for all monitor detected errors.

NOTE: Data errors are reported by the test.

The I/O cycle position pointer and test section pointer is supplied in each message.

3.5.2 Generalized Error Format:

A1	Q1	A 2	Q 2
XXY8	S/J	SSE_1E_2	RTN ADDR

XX - Test no.

Y - No. of A/Q pairs

8 - Error message

S/J - Stop jump parameter

STOPS

Bit 0	Stop 1	Stop to enter test parameters
Bit 1	Stop 2	Stop at end of test section
Bit 2	Stop 4	Stop at end of test
Bit 3	Stop 8	Stop on error

JUMPS

Bit 4	Repeat conditions
Bit 5	Repeat test section
Bit 6	Repeat test
Bit 7	Build test list
Bit 8	Omit typeouts
Bit 9	Display memory address in Stops
Bit 10	Re-enter test parameters
Bits 11-15	Not used

SS - Section No.

E_{1} - Section position pointer

E_{2} - I/O cycle position pointer

RTN ADDR - Memory location of error routine

3.5.3 DATA ERRORS - A dummy I/O cycle pointer (XXXF) is used for data errors. For all data errors the information following the generalized error format will be as follows:

A3	Q3	A4	Q4	A5	Q5
Actual	Expected	Read buffer address	Error address	Transfer length attempted	This track address

3.5.3.1 Data Error Example:

8058	0241	07AF	OF29	F339	F3B9	182B	193B	OC00	0022
				Actual Data	Expected Data	Read Buffer	Addr of error	Length	Track/ Sector

Section No.
Section pointer
I/O cycle pointer - data error
Test error routine return address

The error indicates bit 07 was dropped in track 1 sector 2. The transfer length attempted was 3072 words or 1 complete track.

3.5.4 Monitor Detected Errors

For monitor detected errors, the I/O cycle pointer will be X0 --XA, numbers X8 --XA are used for the interrupt processor. The message following the generalized error format will be in two parts.

PART 1

A3	Q3	A4	Q4
Monitor error Number	LORR	Last Operation (A)	Last Operation (Q)

3.5.4.1 Monitor error no.

0000 *Busy status bit did not change state within specified time (status time out), 2 revolutions.

0001 *I/O time out. External reject to output instruction for a period longer than specified.

0002 I/O response error. Reply to output instruction was other than predicted.

PART 2

Monitor Error No.	A5	Q5	A6	Q6	A7	Q7
00	Actual Status 1	Actual Status 2	Actual Status 3	Actual Status 4	Actual Time(msec)	*Status control Word
01	Actual Status 1	Actual Status 2	Actual Status 3	Actual Status 4	Actual Time(msec)	0000 (not used)
02	Actual Status 1	Actual Status 2	Actual Status 3	Actual Status 4		
03	Actual Status	Expected Status 1	Actual Status 2	Expected Status 2	Actual Status 3	Expected Status 3
	Actual Status 4	Expected Status 4				
04	Actual Status 1	Actual Status 2	Actual Status 3	Actual Status 4	Actual Time(msec)	Mask Register
	Expected int. line	0000 (not used) one hex character per line.				

Status 1 = director status (ST1) Status 3 = memory address (ST 3)

Status 2 = sector address (ST 2) Status 4 = last data word (ST 4)

See 6.0 for complete status description.

* Status control word = 0CBS

0 = Not used

C = Condition; 1 = wait for status bit to go "off"
0 = wait for status bit to go "on"

B= Bit position in status word

S = Status word (0-3)

0003 Status error. Actual did not equal expected.

0004 *Interrupt time out. Interrupt did not occur within specified time.

*Time is measured to the nearest millisecond.

3.5.4.2 LO = Last operation performed

10 = Write

20 = Read

30 = Function

3.5.4.2.1 RR = Response to last operation output instruction

10 = Reply

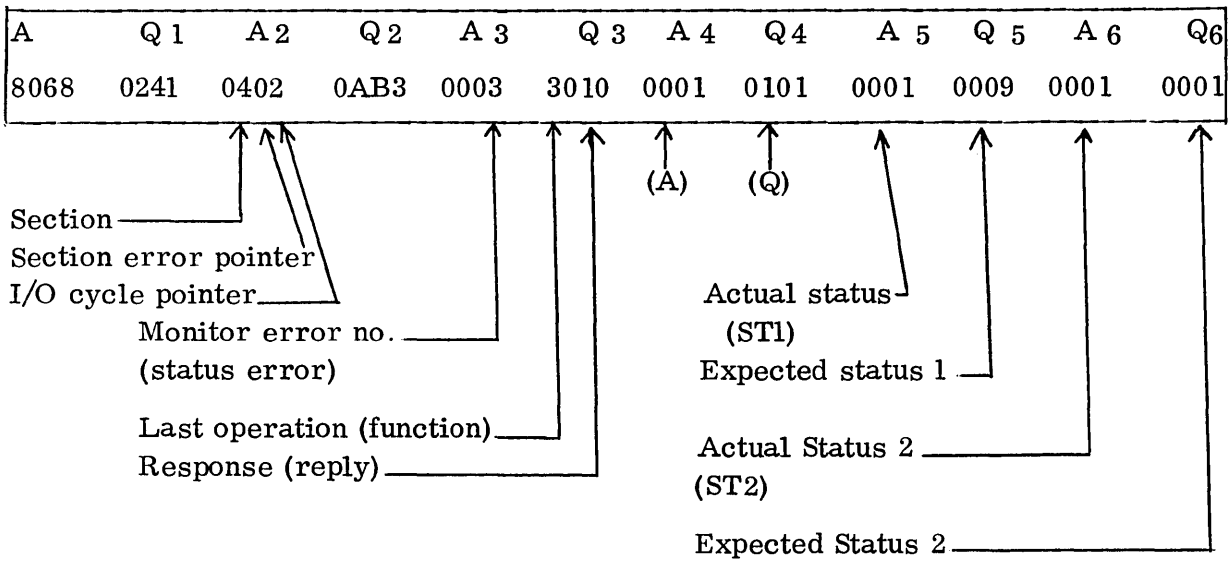
20 = External reject

30 = Internal reject

3.5.4.3 Last Operation (A) = contents of the A register for last operation.

3.5.4.4 Last Operation (Q) = contents of the Q register for last operation.

3.5.5 Monitor error example:



This error indicates that the data status (bit 03) is missing from ST1 after a clear controller to equipment no. 2. The section error pointer indicates the function was issued from the initialize routine. The I/O cycle pointer indicates the error was detected in the 1st recheck status subroutine which verifies the status copied after issuing the clear controller function (see I/O cycle flow chart).

Note the actual and expected values for ST2 (A6, Q6) are equal. Although the status error is in ST1, the error message will contain actual and expected values for all status words copied as a diagnostic aid.

4.0 TEST SECTIONS

4.1 SECTION 0

4.1.1 Controller Clock Adjustment/Buffer Addresses

This section does not require the computer for I/O. Its purpose is to instruct personnel in adjusting the controller clock to be in sync with the bit clock on the drum. The bit clock is approximately 342 nanoseconds for a 60 Hz drum and 400 nanoseconds for a 50 Hz drum.

4.1.2 The following message will be output:

CONTROLLER CLOCK ADJ *= TEST POINT

1. SYNC (+) CARD A26*1
2. ADJUST ZERO GOING CLOCK A26* 4+/-5NSEC.
3. ALL MEASUREMENTS REF. AT +1.5V.

READ BUFFER = YYYY

WRITE BUFFER = ZZZZ

4.1.3 The clock should be adjusted every six months or whenever the drum is replaced.

4.2 SECTION 1

4.2.1 Sector address counter

4.2.2 The purpose of this section is to verify the sector address counter. The diagnostic will test for the following conditions:

1. A bit "stuck" on
2. A bit "stuck" off
3. An intermittant bit

Either of the above conditions would cause addressing errors, resulting in potential catastrophic failures.

4.2.3 To accomplish this the sector address register status is read at approximately 40 kHz rate for 17 milliseconds, or one revolution, and the status stored in a continuous 850 word buffer. The data is then examined for proper incrementing. To scope this section set bits 5, 8 in the SMM stop/jump word. Bit 05 sets repeat section, bit 08 omits the typeout.

4.2.4 The following sequence is performed.

Operation	Section Error Pointer
1. Read sector address status for 1 revolution.	0 1 1X
2. Check for data = all zeroes.	0 12X
3. Verify the incremented sector addresses.	0 13X

4.3 SECTION 2

4.3.1 Initial Sector Address Register/Sector Address Compare

4.3.2 This section will verify the Initial Sector Address (ISA) Register and Sector Address Compare logic using all 32 sectors. The ISA will be preloaded at zero. The sector address compare bit and sector address status will be monitored to see that a complete revolution does not occur without sensing sector compare. After detecting sector address compare, the sector address status will be verified. This will check for improper loading of the ISA register.

4.3.3 The following sequence is performed.

Operation	Section Error Pointer
1. Load ISA register (1st time = zero).	021X
2. Wait for sector address compare, verify sector address status.	022X
3. Increment sector address and repeat steps 1 and 2. Exit after last sector.	

4.4 SECTION 3

4.4.1 Initial Core/Final Core Address/Core Address Compare

4.4.2 This section will verify the loading of the initial/final core address registers and the address compare logic. This test does not require DSA transfers, therefore the incrementing logic will be checked in another section. The method is as follows:

1. Load initial and final address registers to zero, verify compare and core address status.
2. The final address register bit 00 is set and no compare compare verified.
3. The initial address register bit 00 is set and compare status verified.
4. The procedure is repeated with bits 00 and 01. After each pass the next significant bit is added until all the bits are verified.

A sliding ones/zeros and random pattern will then be used to determine if there is interaction on the A-write lines.

4.4.3 Improper loading of the initial core address register will be verified by the final core address status. Since the same register is used for both operations, this will be a quick check.

4.4.4 The following sequence is performed.

Operation	Section Error Pointer
1. Set 1st pattern	
2. Load ICA register, do not expect core address compare.	031X
3. Load FCA register with pattern from step 2, expect core address compare status.	032X
4. Shift pattern one place and repeat from step 2. After 16 shifts get next word type and repeat from step 2. There are 4 word types.	

4.5 SECTION 4

4.5.1 Sector Overrange/Drum Data Register

4.5.2 The purpose of this section is to verify the sector overrange logic and the three data registers between DSA and the drum. The section will perform a drum write using the data pattern from the 5th parameter stop, see 3.2.6.

4.5.3 To verify sector overrange (SOR) an attempt is made to write into the 1st non-existent sector as determined from the second parameter stop (see 3.2.6). Refer to Table 1.0 for SOR jumper assignment.

4.5.4 The following sequence is performed.

	Operation	Section Error Pointer
1.	Load ICA with write buffer address.	041X
2.	Load FCA with write buffer address (ICA).	042X
3.	Load ISA with illegal address.	043X
4.	Enable alarm interrupt if requested.	044X
5.	Attempt a 1 word write on 1st non existent sector.	045X
6.	Clear controller if interrupts not selected.	046X
7.	Enable end of operation interrupt.	047X
8.	Load last good ISA value.	048X
9.	Initiate a 1 word write on last sector.	049X

The data register cards located on cards A06-A07 are checked.

DSA control for drum write is checked on card A11.

Drum write control on A12 is checked except for checkword generation and transfer of write data to the drum.

No. of Tracks	SOR Jumper Positions 3-4	5-6	7-8	9-10
64	0	0	0	0
128	0	0	0	1
192	0	0	1	0
256	0	0	1	1
320	0	1	0	0
384	0	1	0	1
448	0	1	1	0
512	0	1	1	1
576	1	0	0	0
640	1	0	0	1
704	1	0	1	0
768	1	0	1	1
832	1	1	0	0
896	1	1	0	1
960	1	1	1	0
1024	1	1	1	1

TABLE 1.0

Card Position A16

4.6 SECTIONS 5

4.6.1 Guarded address

4.6.2 The purpose of this section is to verify the guarded address logic and the enable guarded address switch. A message will be output to set the switch.

4.6.3 The highest guarded address parameter (see 3.2.6) determines which track will be used (sector 0) to verify the illegal write. Refer to table 2.0 for track address jumper assignment.

4.6.4 After reading from the guarded sector, the section attempts a write to the same address. The error is verified, and a one sector write on the last track, sector 0 is performed. The guarded address switch is reset and the previously guarded sector is written using the same data.

4.6.5 Interrupts are not required for this section.

4.6.6 The following sequence is performed.

	Operation	Section Error Pointer
1.	Output message to set guarded address switch.	
2.	Load ICA register with address of read buffer.	051X
3.	Load FCA register with address of read buffer +95.	052X
4.	Load ISA registers with highest guarded track, sector zero.	053X
5.	Initiate read operation	054X
6.	Load ICA register with address of read buffer.	055X
7.	Initiate write operation on guarded track, sector zero. Expect error.	056X
8.	Clear Controller	057X
9.	Load ISA register with last track address, sector zero.	058X
10.	Initiate write operation on last track, sector zero.	059X
11.	Load ISA register with highest guarded address, sector zero.	05AX
12.	Load ICA register with address of read buffer.	05BX
13.	Output message to clear guarded address switch.	
14.	Initiate write operation on a guarded sector using the same data (see step 7) to preserve the guarded sector.	05CX

JUMPER ADDRESS		HIGHEST GUARDED TRACK
31	32	128
33	34	64
35	36	32
37	38	16
39	40	8
41	42	4
43	44	2
45	46	1

CARD SLOT A-16

TABLE 2.0

NOTE: No jumper = track 0

4.7 Section 6

4.7.1 Surface address test

4.7.2 The purpose of this section is to verify the address logic from the controller to the drum surface. The serialize method is used to write each sector with its own address. For 512 tracks, the data would appear on the drum as follows:

Track	Sector	Word 0	Word 1	Word 95
0	0	0000	0000 — — — —	0000
0	1	0001	0001 — — — —	0001
1	0	0010	0010 — — — —	0010
1	10	001A	001A — — — —	001A
511	0	03F0	03F0 — — — —	03F0
511	31	03FF	03FF — — — —	03FF

4.7.3 The entire drum surface, or that area specified by the input parameters (see 3.2.6), is also data checked. After serializing is complete, the sector address is reset to the 1st track, then read and compared to predicted values for that track. This procedure is repeated until all tracks have been verified.

4.7.4 The following sequence is performed.

	Operation	Error Section Pointer
1.	Enable end of operation interrupt if requested.	061X
2.	Load final core address register	062X
3.	Load initial core address register.	063X
4.	Load initial sector address register.	064X
5.	Set up write buffer (1 track).	
6.	Write 1 track.	065X
7.	Repeat from step 3 until all tracks written.	
8.	Load final core address register.	066X

4.7.4 (Cont.)

	Operation	Error Section Pointer
9.	Load initial core address register.	067X
10.	Load initial core address register.	068X
11.	Generate 1st (next) track in write buffer.	
12.	Read 1 track.	069X
13.	Compare read and write buffers.	06AF
14.	Repeat from step 9 until last track read and checked.	

4.8 Section 7

4.8.1 Worst Case Patterns

4.8.2 The purpose of this section is first, to test the drum surface for bad spots and second, to test check the head assembly and drum electronics for rate sensitivity problems. Each track is written with the same data which contains 37 sets of data. Except for one, each set is 83 words in length, see table 3.0.

DATA	LENGTH	DESCRIPTION
Random	83	Random
Sliding zeroes	83	Each of 16 patterns is 83 words
Sliding ones	83	Each of 16 patterns is 83 words
101010101010	83	Maximum rate change
110011001100	83	50.0% max.
000111000111	84	33.3% max.
000011110000	83	25.0% max.
	3072 Total	

TABLE 3.0

Table 3.0

4.8.3 The following sequence is performed.

Operation		Section Error Pointer
1.	Enable end of operation interrupt if requested.	071X
2.	Load final core address register.	072X
3.	Load initial core address register.	073X
4.	Load initial sector address register.	074X
5.	Write 1 track.	075X
6.	Load final core address register.	076X
7.	Load initial core address register.	077X
8.	Load initial sector address register.	078X
9.	Read 1 track.	079X
10.	Verify the data.	07AF
11.	If last track verified exit, if not increment the track address and go to step 2.	

4.9 Section 8

4.9.1 Maintenance

4.9.2 The purpose of this section is to allow the operator to design a mini diagnostic which operates under I/O Cycle control. The following modes are available as defined in 3.2.6.2:

4.9.2 (Cont.)

Operating Mode

1. Write only
2. Read only
3. Write, read
4. Write, read and data check
5. Read only, data check

4.9.3 Data transfers may be made with or without interrupts as determined by stop 3, see 3.2.6.3.

4.9.4 The initial track/sector address is entered via stop 4, see 3.2.6.4. for example, track 4 sector 12 = 008C.

4.9.5 The transfer length is entered concurrent with the operating mode.

4.9.6 The data pattern to be written is entered via stop 5, see 3.2.6.2.

4.9.7 This section is designed to loop indefinitely. The method used to stop execution and redefine the operating conditions is as follows:

1. Set the skip key.
   A = SMM ID word Q = S/J
2. Set bit 10 in the stop/jump word. This is a request to stop to re-enter parameters.
3. Hit run, the second SMM stop is displayed.
4. Hit run again, the test will stop for parameter entry. Remove bit 10 from the stop jump word and make parameter changes.

The skip key is checked a maximum of six times in the I/O Cycle and once in the monitor. Therefore, it's possible to repeat step 1 seven times (worst case) before reaching the re-enter parameter stop.

4.9.8 This section should be used as a diagnostic aid in troubleshooting specific problem areas. A high degree of sync control for scoping is available through the length of transfer and initial sector address value parameters.

4.9.9 The following sequence is performed.

	Operation	Section Error Pointer
1.	Enable end of operation interrupt if requested.	081X
2.	Load final core address based on length parameter.	082X
3.	Load initial core address register.	083X
4.	Load initial sector address based on parameter data.	084X
5.	Write, length based on parameter data.	085X
6.	Repeat steps 1 - 6 for write only. Continue to step 7 for read.	
7.	Load final core address based on length parameter.	086X
8.	Load initial core address register.	087X
9.	Load initial sector address value from step 4.	088X
10.	Read, length based on parameter data.	089X
11.	Verify data if requested, if not go to step 1.	08AF

Step 1 also checks the skip key to determine if a stop to re-enter parameters has been requested.

4.10 Section 9

4.10.1 Auto load and Program Protect

4.10.2 This section is in two parts. Part 1 verifies the auto load logic, part 2 checks the protect logic.

4.10.3 Part 1 is checked by saving the auto load image (1536 words) in the write buffer, writing the auto load area , clearing core from 0 - 5FF, initiating an auto load and comparing the data to the write buffer. If an error is detected the write buffer image is returned to low core and the data error reported. Note the actual error is destroyed.

4.10.4 Part 2 verifies both the controller and computer protect fault logic. The conditions stated in table 4.0 are checked for the proper response.

Controller PP Switch	I/O PP Bit	Controller Response
1	1	Reply
1	0	Ext. Reject
0	1	Reply
0	0	Reply

Table 4.0

4.10.5 To verify controller protect fault a read drum is initiated under the following conditions:

1. Read buffer, length = 1536 words, is protected.
2. Drum protect switch is off.
3. CPU protect switch is on.
4. Output instruction is not protected.

After processing the protect fault, the read buffer is checked to insure no DSA transfers had taken place. If a data error is detected, the following message is added to the normal data error:

CPU SHOULD NOT HAVE ACCEPTED DSA
DATA DURING FORCED PROTECT FAULT.

4.10.6 It is possible for the controller to write, under protected conditions, to the CPU and not detect a protect fault. An example is as follows:

Conditions

1. Read buffer protected
2. Output instruction protected
3. CPU protect switch on

A faulty DSA transmitter for bit 17 (protect) would indicate to the CPU that the output instruction was not protected and would not write into memory. The CPU sends the DSA protect fault signal but it is not sensed in the controller. The problem could be a bad cable, receiver or another DSA device holding down bit 17.

4.10.7 The missed protect fault is checked as follows:

1. Generate random data in read buffer.
2. Generate same data in write buffer.
3. Read auto load area under protected conditions (4.10.6).

4. Compare read/write buffers, expect no compare.

5. Print the following message after compare:

   DSA PROTECT FAULT NOT

   DETECTED BY CONTROLLER

   P = XXXX

The following sequence is performed.

	Operation	Section Error Pointer
1.	Enable end of operation interrupt if requested	091X
2.	Load FCA register = WRBUF+1535	092X
3.	Load ICA register = WRBUF	093X
4.	Load ISA register = track 0, sector 0	094X
5.	Write auto load area	095X
6.	Print auto load message, clear core from 0-5FF, wait 10 seconds	
7.	Verify the data	096F
8.	Print message to set drum and console protect switches	
9.	Load FCA register = RDBUF+1535 (auto load area)	097X

	Operation	Section Error Pointer
10.	Load ICA register = RDBUF.	098X
11.	Fill read and write buffers with same data.	
12.	Initiate read, expect external reject.	099X
13.	Print message to clear drum protect switch. Protect read buffer.	
14.	Initiate read, expect protect fault. Verify memory address status =RDB UF+1.	09AX
15.	Clear controller if interrupt mode not selected. Go to 16. for interrupt mode selected.	09BX
16.	Check read buffer data to verify no DSA transfers. A special message is added to the normal data error.	
17.	Load ICA register = RDBUF.	09CX
18.	Read 16 sectors beginning track 0, sector 0. Output instruction is protected.	09DX
19.	Check data determine if protect fault occurred. If yes print special message.	
20.	Clear read buffer protect bits.	

4.11 Section 10

4.11.1 Checkword check

4.11.2 This section should be run to check the drum surface when the customer will not allow writing on the drum.

4.11.3 That portion of the drum surface as defined to the test during parameter input time, is read a track at a time. The data is stored in the read buffer but not checked. Status is checked before, during and after each operation.

4.11.4 For 60Hz power timing is approximately 30 tracks per second.

4.11.5 The following sequence is performed.

	Operation	Section Error Pointer
1.	Enable end of operation interrupt if requested	0A1X
2.	Load FCA register	0A2X
3.	Load ICA register	0A3X
4.	Load ISA register	0A4X
5.	Initiate read operation	0A5X
6.	Check for last track. If not last increment track address and repeat from step 3. If last, exit.	

4.12 Section 11

4.12.1 Clear timing error

4.12.2 This section verifies that a clear controller function issued after sensing a timing error interrupt will result in a clear timing interrupt.

4.12.3 The interrupt line must be connected in order to execute this section.

4.12.4 The following sequence is performed.

	Operation	Section Error Pointer
1.	Print the generate timing error message: MOMENTARILY GND A14*2.	
2.	Enable alarm interrupt	0B1X
3.	Output a dummy function to enable I/O cycle to select interrupts then wait for clear timing error interrupt.	0B2X

4.12.5 A 1 second delay after sensing the timing error prevents multiple interrupts.

5.0 SPECIAL TESTS

5.1 CHECKWORD CHECK

5.1.1 The checkword will be held in ST4 (status word 4) when test point A11*26 is grounded. Four unique checkwords will be verified using section 8 to control the number of words written on the drum.

5.1.2 Set the stop on error bit (03) in the Stop/Jump word.
Set up section 8, see 3.2.6.5, to perform a write only using the values in table 5.0. Ground test point A11*26. Start test and observe the error. The actual value for ST4 should contain the checkword as described in table 5.0.

Repeat for all 4 conditions.

No.	No. of Words	Data	Expected checkword
1	96	0000	0000
2	↓	5555	FFF5
3		AAAA	0015
4	96	FFFF	FFE0

Table 5.0

6.0 STATUS DESCRIPTION

STATUS 1 (ST 1) DIRECTOR STATUS

A0	Ready *
A1	Busy
A2	Interrupt
A3	Data (Ready not busy)
A4	End of operation
A5	Alarm
A6	Lost data *
A7	Protected
A8	Checkword error *
A9	Protect fault *
A10	Guarded address enable
A11	Timing track error *
A12	Power failure *
A13	Sector address compare
A14	Guarded address error *
A15	Sector over-range *

* Generates alarm

STATUS 2 (ST 2) SECTOR ADDRESS STATUS

A0 - A4	Sector
A5 - A14	Track
A15	Core address compare

STATUS 3 (ST 3) CORE ADDRESS STATUS

A0 - A15 Core address

STATUS 4 (ST 4) LAST DATA STATUS

A0 - 15 Last drum data word

7.0 FUNCTIONAL DESCRIPTIONS

Q3	Q2	Q1	Q0	Function
0	0	0	0	Write
0	0	0	1	A0 Clear Controller A1 Disable/Clear Interrupt A3 Enable EOP Interrupt A4 Enable Alarm "
0	1	0	0	Read
1	0	0	0	Load initial sector address
1	1	0	0	Load initial core address
1	1	1	0	Load final core address

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