I/O Channel Introduction

CONTROL DATA

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Introduction to the I/O Channel

To receive data to be processed or to send out the processing results, a central processor (or CPU) requires a communication path to an external device. This path allows data to move from a peripheral to the CPU memory, or the reverse. The circuits that provide this input and output path commonly are referred to as the input/output (I/O) channel. This text examines the requirements of an I/O channel and describes two methods of data transfer.

I/O Channel Requirements

The transfer of data between the I/O channel and peripheral devices must be conducted in an orderly sequence; it cannot conflict with the speeds of the various peripheral devices. To accomplish this sequencing, control signals accompany the data. For example, when outgoing data is placed on the data lines, a write signal is sent to the device to signal that data is available. If the data is accepted, the peripheral device sends a reply signal back to the CPU.

Data transfer between the computer and external devices can be accomplished in several ways. Two of these methods, direct memory access (DMA) and programmed I/O, are described in this reading. Because programmed I/O is used more frequently, it is discussed in greater detail.

DMA Data Transfer

Direct memory access is a method of transferring data between the processor memory and external devices; it requires little or no involvement of the CPU. Generally, the CPU initiates the data transfer. It is then free to do other things while the transfer takes place. A peripheral controller will handle control of the I/O. This is normally a buffered operation, which means that the controller will have some method of holding the data temporarily as it is being transferred from memory to a peripheral device. On the CYBER 18 system, the storage module drive uses the DMA type of data transfer.

Programmed I/O Data Transfer

In programmed I/O, data transfer between the processor and external device is controlled completely by a program executed in the CPU.

Programmed I/O uses what is called the A/Q channel, an I/O channel that derives its name from its use of the A- and Q-registers of the CPU. These two sixteen-bit registers are used for a variety of purposes during an I/O operation. The Q-register holds the address of a peripheral; also, certain bits of this register control and direct information on the A/Q channel. The A-register holds function codes, accepts status information from peripheral equipment, and transfers data into and out of the computer memory. The A/Q channel operates in a nonbuffered mode; in other words, data is transferred to the computer memory or to the peripheral equipment directly, as it is received.

The simplified block diagram in figure 1-1 is an example of the method by which peripheral devices are connected to the A/Q channel. It does not show all the equipment that uses this channel to communicate with the CPU.

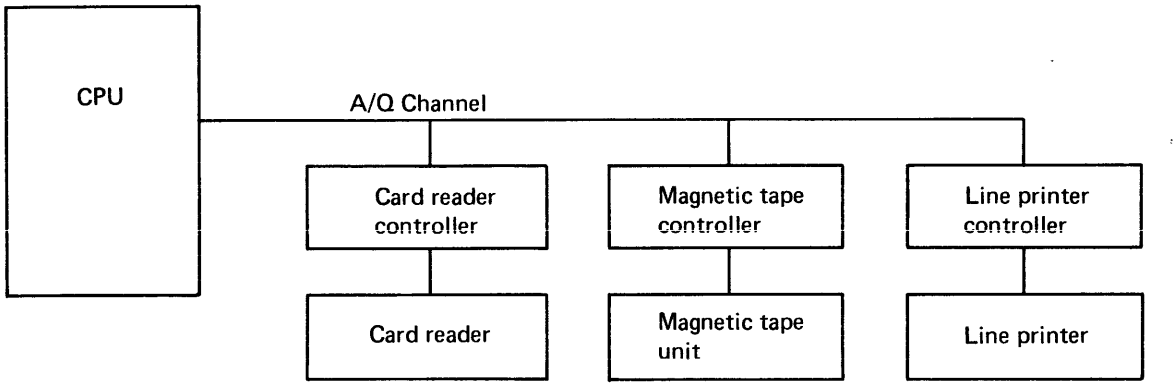


Figure 1-1. Connection of Peripherals to A/Q Channel

Summary

To operate, the computer requires a method of receiving data from external devices and transmitting it to such devices. Two methods for doing this are:

- Direct memory access (DMA), in which transfer of data occurs with little or no involvement of the CPU.
- Programmed I/O, in which transfer of data is controlled by the CPU and makes use of both A- and Q-registers in what is called the A/Q channel.

Q-Register Equipment Addressing

During I/O operations the Q-register specifies the peripheral device to be used and the type of operation being performed. This reading examines the Q-register I/O addressing format.

Addressing Format

The Q-register format during I/O is shown in figure 1-2. The bits are numbered from right to left with bit 0 being the least significant (LSD) and bit 15 the most significant (MSD). The format is divided into three portions: W, E, and command.

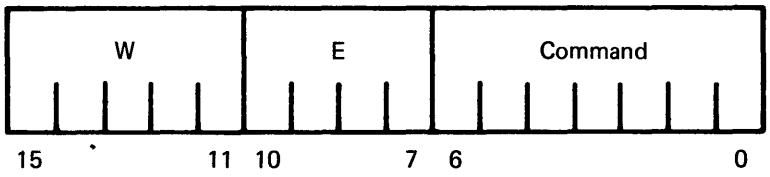


Figure 1-2. Q-Register I/O Addressing Format

During equipment addressing, the W portion (bits 11 to 15) of the register is not used.

The E portion contains the equipment code, which identifies the peripheral device to be used. This four-bit code is sent to all equipment on the I/O channel. When the device with an identification number equivalent to the equipment code replies, the I/O operation may be completed.

Each peripheral device connected to an I/O channel has its own identification number. These numbers are selected during installation by setting the equipment address to the desired number. This can be done by the use of a switch or jumper plugs (the CYBER 18 uses only jumper plugs). The equipment and address codes listed in table 1-1 are in common use and are those used in this unit unless other codes are stated.

TABLE 1-1
Equipment Address Codes

Equipment	Address Codes	Q 10	09	08	07
Card reader	B_{16}	1	0	1	1
Line printer	4_{16}	0	1	0	0
Magnetic tape	9_{16}	1	0	0	1
Conversational display terminal	1_{16}	0	0	0	1
Dual channel communications line adapter	A_{16}	1	0	1	0
Flexible disk	E_{16}	1	1	1	0
Available for additional equipment add-on	0, 2, 3, 5, 6, 7, 8, C D, F				

The command code is made up of the seven lower bits (0 through 6) of the Q-register.

This portion controls I/O operations by:

- Specifying the direction of data transfer
- Directing control functions
- Directing the status and status levels

The command code (or field) is divided into two sections, one called the S, or station code, the other called the D, or director code. The use of these sections differs from device to device; in most cases, all the bits are not used.

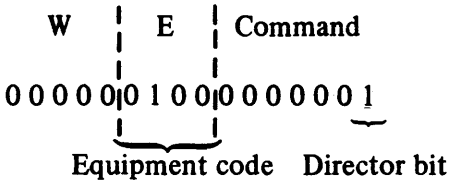
In this unit, you are concerned only with the LSD bit (0) called the director bit. Unless told otherwise, assume other bits in the command field to be 0. The director bit specifies whether an outgoing code is data to be written or a function code commanding a specified operation in a peripheral device. It also specifies whether an incoming code is data read from a device or the status code of a peripheral device. The use of director bit 0 is shown in table 1-2.

TABLE 1-2
Use of Director Bit 0

Director Bit 0	Instruction Executed	Peripheral Operation
0	Output from A	Write data
0	Input to A	Read data
1	Output from A	Function code to device
1	Input to A	Status code from device

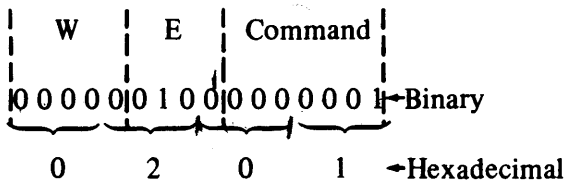
Example of Addressing Format

Assume that a function code is to be sent to the line printer. Assume also that this line printer has its equipment code decoder set to 4_{16}. In binary form, the line printer's address is 0100. This code appears in bits 7 through 10 of the Q-register (the E portion). The director bit is 1, because a function code is being sent to the line printer. All the bits in the W portion and the remainder of the command field are unused and, therefore, 0's. In binary form, the contents of the Q-register are:



In hexadecimal, the Q-register contains the code 0201.

Because the E portion of the Q-register is not equivalent to the second most significant hexadecimal digit, you probably will find it necessary to transform the hexadecimal value of the Q-register into binary to identify the four bits in the E portion. You can then transform those four bits back into hexadecimal and, based on table 1-1, identify what piece of equipment is being identified. The transformation looks like this:



In this case the E portion of the Q-register indicates 0100 or 4_{16}, thus identifying the line printer.

When the output instruction is executed, the function code from the A-register is sent to the printer. If the instruction executed were an input instruction, the printer status would be input to the A-register.

See table 1-3 for a decimal-hexadecimal-binary conversion table.

TABLE 1-3
Decimal-Hexadecimal-Binary Relationships

Decimal	Hexa-decimal	Binary	Decimal	Hexa-decimal	Binary
0	0	0000	8	8	1000
1	1	0001	9	9	1001
2	2	0010	10	A	1010
3	3	0011	11	B	1011
4	4	0100	12	C	1100
5	5	0101	13	D	1101
6	6	0110	14	E	1110
7	7	0111	15	F	1111

Summary

The Q-register is used as follows during I/O operations:

- The W portion of the register is not used.
- The E portion identifies the device to be used.
- Bit 0 of the command portion identifies the type of operation to be performed.

Check Your Understanding

DIRECTIONS: In the blank space to the right of each address code, indicate the device being addressed. Do not be concerned with the director bits—only the address codes. Note that the four most significant bits are 0's. Use the equipment address codes specified in "Q-Register Equipment Addressing."

1. 0581_____.

2. 0200_____.

3. 0081_____.

4. 0701_____.

5. 0500_____.

6. 0481_____.

ANSWERS

1. Card reader 2. Line printer 3. Conversational display terminal
4. Flexible disk 5. Dual channel communications line adapter
6. Magnetic tape

A-Register Function Codes

You are aware that, during an I/O operation, the A-register transfers data into or out of the computer, accepts status information from peripheral equipment, and sends function codes to the equipment. The specific action depends on the value of bits 0 through 6 in the A-register. This reading examines the relationship of the A-register to the Q-register and details the functions of bits 0 through 6.

Relating the A- and Q-Registers

The director bit in the Q-register and the type of I/O instruction being executed determine whether the A-register contains data, status information, or a function code. When director bit 0 of the Q-register address code is a 1, and an output instruction is being executed, the lines from the A-register are directed to control the functions of a peripheral unit. The function code sent to the peripheral controller will be stored there until it is cleared or changed. Each one of bits 0 through 6 in the A-register represents one of those functions, as shown in figure 1-3. (The information in this figure is general, indicating some of the functions that may be performed. Obviously, different peripherals perform differing functions, so this figure should not be taken to cover all situations.) Following the figure are definitions of its format and function bits.

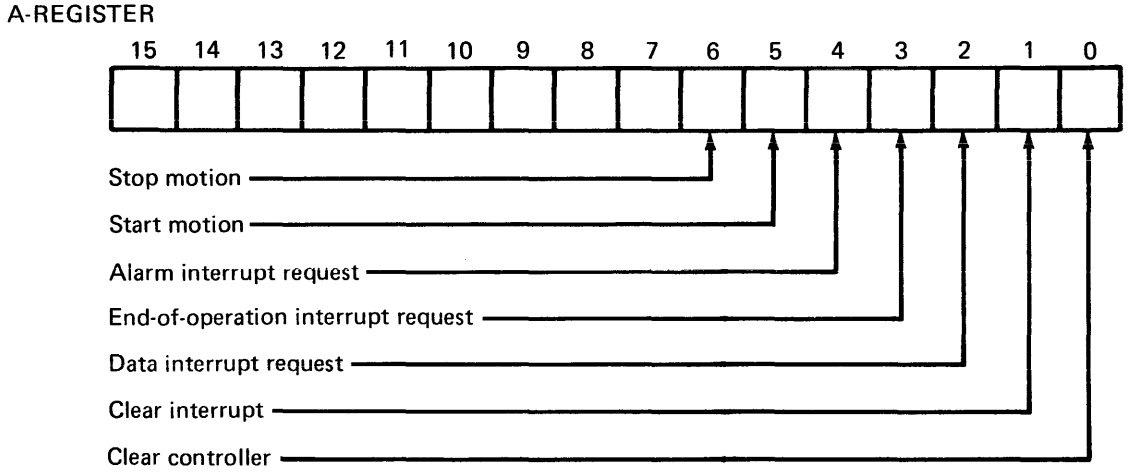


Figure 1-3. A-Register Function Bit Definitions

Function Bit Definitions

Clear Controller. Bit 0 clears all interrupt requests and responses, motion requests, errors, and other logic circuits. A function code in which bit 0 is set and any of bits 2 through 6 are set will first clear all previous functions and then immediately set the function conditions indicated by bits 2 through 6. In this way, more than one function may be indicated in each code.

Clear Interrupt. Bit 1 clears all interrupt requests and responses. In an interrupt, an external device interrupts the main program and allows the processor to attend to the needs of the device. The interrupt may indicate that data is ready to be transferred, an error has occurred, or the equipment has lost its ready condition. In any case, the program must request any interrupts.

Data Interrupt Request. Bit 2 sets a data interrupt request, which generates an interrupt response as soon as a data transfer is possible. The interrupt response is cleared by the reply to the data transfer. Both the interrupt request and response are cleared by the clear controller, clear interrupt, or master clear signals.

End-of-Operation Interrupt Request. Bit 3 selects the end-of-operation interrupt request. This generates an end-of-operation interrupt any time continuous data transfer is stopped (for example, at an end-of-record request).

Alarm Interrupt Request. Bit 4 selects the alarm interrupt request. This causes an interrupt to be generated when an alarm condition occurs. An alarm may indicate a change of status (for example, the equipment shifting to a not ready condition) or an error (for example, lost data). Each piece of equipment must specify the manner in which the alarm is used and must provide a status indication for each condition causing an alarm.

Start Motion. Bit 5 directs the device to start motion in its storage medium (for example, to feed a card or start the tape drive).

Stop Motion. Bit 6 halts the operation begun by start motion. Stop motion takes precedence over start motion.

Although bits 7 through 15 are not shown here, they may be used at the discretion of the designer of the particular system. To determine the function bits used with each peripheral device, refer to the manual for the particular device.

Check Your Understanding

DIRECTIONS: For the following exercise, assume that the director bit of the Q-register is a 1 and that an output instruction is being executed. Fill in the blanks, stating what function or functions are to be performed by the codes shown.

Functions	A-Register Contents
1._____	0020
2._____	0008
3._____ and _____	004 1
4._____ , _____ and _____	0034
5._____ and _____	0042
6._____ , _____ and _____	0029

ANSWERS

1. Start motion 2. End of operation interrupt request 3. Stop motion and clear controller 4. Start motion, alarm interrupt request, and data interrupt request 5. Stop motion and clear interrupt 6. Start motion, end-of-operation interrupt request, and clear controller

A-Register Status Codes

In addition to sending function codes during I/O operations, the A-register can be used to receive status codes from peripherals and to transfer these codes to the processor. As with function codes, the Q-register directs the operation. When the director bit of Q is a 1 and an input instruction is being executed, the A-register receives the status of the peripheral device. Each bit in A set to a 1 then represents a specific status condition. Figure 1-4 shows the bit assignments for typical status conditions. Different types of peripherals may have status bit meanings other than those shown. The status bit assignment for each peripheral device is found in the manual for that device. Following figure 1-4 are typical status bit definitions.

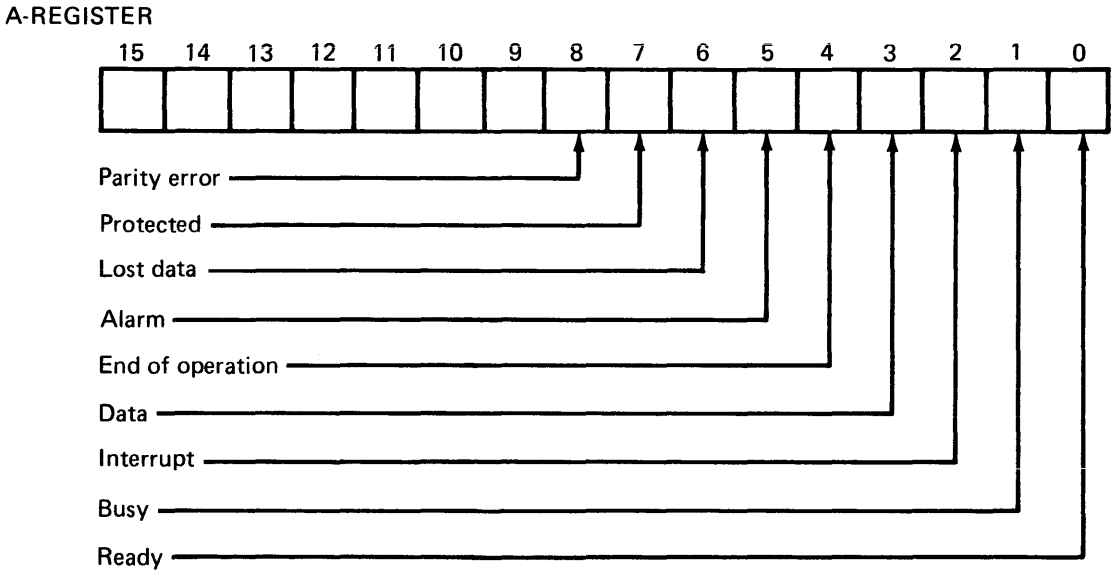


Figure 1-4. Status Bit Definitions

Status Bit Definitions

Ready. Bit 0 set to a 1 indicates that a unit is ready to perform an operation when requested by a start request function. Equipment that requires manual intervention must be made ready manually.

Busy. Bit 1 set to a 1 indicates that the unit is busy or in operation. It becomes busy immediately on initiation of the start operation, if the operation can be performed. Under normal conditions, the unit remains busy until it has finished all activity and is able to perform another operation.

Interrupt. Bit 2 set to a 1 indicates that an interrupt response has been sent from this peripheral controller. Other bits must be monitored to determine the cause of the interrupt.

Data. Bit 3 set to a 1 indicates that the peripheral controller is ready to perform a data transfer. If a data interrupt was selected, this bit also indicates the type of interrupt that occurred.

End of Operation. Bit 4 set to a 1 indicates that an end of operation has occurred, which means that the last operation initiated has been completed. If an interrupt signal has been selected, it indicates the cause of the interrupt. Each peripheral device has a specific condition that constitutes an end of operation.

Alarm. Bit 5 set to a 1 indicates an alarm, which may be in response to any one of several equipment conditions. See reference information for each device for the specific conditions.

Lost Data. Bit 6 set to a 1 indicates that data may have been lost. This occurs when the computer does not service the controller within the prescribed time for the device. This loss should be detected and displayed.

Protected. Several peripheral devices may have a PROGRAM PROTECT switch that, when set, keeps the information from being inadvertently destroyed. Bit 7 set to a 1 indicates that the PROGRAM PROTECT switch for a device has been placed manually in the protected position. This bit also may indicate that the device, if connected to a DMA, is able to enter data into protected memory areas.

Parity Error. Bit 8 set to a 1 indicates that a parity error has occurred in a storage device that incorporates parity as part of its format.

Bits 9 through 15 are not shown, but these may be used in some site configurations at the discretion of the designer. To determine the function bits used with each peripheral device, refer to the manuals for that device.

Check Your Understanding

DIRECTIONS: Fill in the blank or blanks to the left of each status code, identifying the status indicated. Assume that bit 0 of the Q-register is a logic 1 and that an input instruction is being executed.

Status	A-Register Contents
1._____ and _____	0009
2._____ , _____ and _____	0122
3._____ , _____ and _____	0064
4._____ , _____ and _____	0112
5._____ , _____ , _____ , _____ , and _____ .	0073

ANSWERS

1. Data, ready 2. Parity error, alarm, busy 3. Lost data, alarm, interrupt
4. Parity error, end of operation, busy 5. Lost data, alarm, end of operation, busy, ready

Data Input and Output

Input/output operations in the CYBER 18-20 system are initiated by two instructions: input to A (INP) and output from A (OUT). The Q-register director bit 0 determines the significance of the incoming or outgoing information. When the director bit is a logic 1, incoming information is the equipment status and outgoing information is a function code. When the director bit is a logic 0, data will be transferred into or out from A. In this reading, you examine what occurs with INP and OUT instructions, and you are shown the sequence of activities necessary for their proper operation.

INP and OUT Instructions

The INP instruction initiates a read operation, which inputs a single word to the A-register. The computer signals its request for data by activating the read line. The selected peripheral device responds with a REPLY signal when the data is available on the lines to the A-register.

If no data is available when the READ signal arrives, the device responds with a REJECT signal. The peripheral device must respond with a REPLY or a REJECT within a certain period of time, generally less than twenty microseconds. If no REPLY or REJECT is received within a certain time, the CPU generates an internal REJECT to clear the INP/OUT instruction.

In most cases, a REPLY allows the computer to continue executing the program and a REJECT causes the program to check for errors and loop back to the INP instruction until a REPLY is received and the program can continue.

An OUT instruction initiates a write operation, which outputs a single word from the A-register. The write signal line becomes active when output data is present on the data lines. The selected peripheral responds with a REPLY if it can receive the data. When received, the REPLY indicates that the data has been transferred and that execution of the program continues.

If unable to receive the data, the device responds with a REJECT. In this case, the data is not transferred, and the program checks for errors and then loops back to the OUT instruction until the equipment sends a REPLY.

Sequence of Activities

The following summarizes the activities that must take place during an I/O operation, in the sequence required for proper operation.

Input Data on A/Q Channel

1. The peripheral device must be ready.
2. The address of the peripheral device is placed in the Q-register.
3. The director bit of Q must be a logic 0.
4. The computer requests data by making the read line active when the INP instruction is executed.
5. The peripheral device sends a REPLY if it has data available on the lines.
6. A single word is input to the A-register as the INP instruction is executed.

An example of an input device is the card reader. The above sequence is followed and the single-word input to the A-register is a single-column read from the card. The same procedure is needed for each column of the card.

Output Data on A/Q Channel

1. The peripheral device must be ready.
2. The address of the peripheral device must be in the Q-register.
3. The director bit of Q must be a 0.
4. The computer indicates that it has data on the output lines by making the write line active when the OUT instruction is executed.
5. The peripheral device sends a REPLY if it can accept the data.
6. A single word is sent to the peripheral device as the OUT instruction is executed.

An example of a device used in output is the line printer. The above sequence is followed and the single-word output from A is one character to be printed; 136 characters are required for one full line of print.

Summary

Two instructions are used to initiate input/output operations:

- INP initiates a read operation that inputs into the A-register a single word from a specific peripheral.
- OUT initiates a write operation that outputs from the A-register a single word to a specific peripheral.

I/O Control Signals

The A/Q channel relies on the A-register for access to storage. In these nonbuffered transfers, data is transferred a word at a time through the A-register. Because the sixteen bits of the word are transferred in parallel mode, sixteen lines are used to transfer data between the CPU and the peripheral devices. More lines are needed, however; these lines carry signals, called control signals, that direct I/O operations. This text defines six control signals and describes four instructions used in read or write operations.

Control Signal Definitions

READ. This signal indicates a request for an input operation. If data is available in response to the READ signal, the data and a REPLY are returned within a preset time. If data is not available, a REJECT signal must be returned within that time.

WRITE. This signal indicates a request for an output operation. If the data available on the lines can be used, a REPLY is returned within a specified time. If the data cannot be used, a REJECT signal must be returned within that time.

REPLY. This signal causes different actions, depending on whether an input or output instruction is being executed.

During an input operation, if data is available when the READ signal becomes active, the following sequence of events occurs:

1. The data available is gated to the data lines.
2. The REPLY is returned within a predetermined time.
3. The REPLY causes the read line to drop.
4. When the READ signal drops, the REPLY drops.
5. When the REPLY drops, the data lines drop.

During an output operation, if the peripheral can accept data when the WRITE signal becomes active, the following sequence of events occurs:

1. The channel transfers data to the appropriate peripheral equipment.
2. The peripheral equipment sends a REPLY to the channel within a predetermined time.
3. The channel drops the WRITE signal when it receives the REPLY.
4. When the WRITE signal drops, the REPLY drops.
5. The data lines drop very shortly after the WRITE drops.

REJECT. If the specified operation cannot be performed in response to the READ or WRITE signal, a REJECT will be returned within a predetermined time.

PROGRAM PROTECT. This signal is generated by the CPU if the I/O instruction requires access to a protected device. If this signal is not present, the protected device returns a REJECT for all access attempts except status requests.

CHARACTER INPUT. This signal is generated by the peripheral device if the data transfer is an eight-bit character or less in the low order bit positions. On devices that never exceed an eight-bit transfer, this line is normally active continuously during data transfer.

LDA, STA, INP, OUT Instructions

In addition to the preceding control signals, four instructions are used during a read or write operation: LDA, STA, INP, and OUT.

LDA. The load A instruction takes information from the computer memory and places it in the A register in preparation for an output operation.

STA. During an input operation, the store A instruction takes the information the A-register received from a peripheral device and stores it in the computer memory.

INP. The input to A instruction causes a peripheral device to place data into the A-register.

OUT. The output from A instruction causes the information in the A-register to be sent to a peripheral device.

Summary

The following control signals direct I/O operations:

- READ, which requests an input operation
- WRITE, which requests an output operation
- REPLY, which acts in different ways, depending on whether an input or output instruction is being executed
- REJECT, which occurs when a specific operation cannot be performed
- PROGRAM PROTECT, which provides access to protected devices
- CHARACTER INPUT, which is generated for characters of eight bits or less in the low order bit positions

The following instructions are used in a read or write operation: LDA, STA, INP, and OUT.

Check Your Understanding

DIRECTIONS: Complete the following statements.

1. **An eight-bit data transfer is accomplished by having the _____ _____signal active.**

2. **If a specified operation cannot be performed, a _____signal is returned.**

3. **If the WRITE signal is active, it signifies a request for a/an _____operation.**

4. **A request for an input operation is signified by the _____signal going active.**

5. **Attempts to access a protected device results in a_____ if the _____ _____ signal is not present.**

6. During a reply to a write operation, the REPLY signal drops when the _____ _____signal drops.

7. During a reply to a read operation, the READ signal drops when the_____ is received.

ANSWERS

1. CHARACTER INPUT 2. REJECT 3. Output 4. READ
5. REJECT, PROGRAM PROTECT 6. WRITE 7. REPLY

I/O Sequencing

For any input/output operation to be successful, events must occur in the proper sequence. The following is a typical I/O sequence. The sequence may differ slightly in some computers, but the method is similar.

Sequence for an Input Operation (INP)

1. The peripheral device must be ready. Whenever the device is not ready, it will return a REJECT when a read or write is attempted.
2. The address of the peripheral device is placed in the Q-register.
3. A function code is placed in the A-register. (A function code will be sent to the peripheral device to initiate input by feeding a card, moving the tape, etc. The director bit of Q must be a logic to indicate that the A-register contains a function rather than data.)
4. An OUT instruction must be executed.
5. The director bit of Q must be changed to a logic 0.
6. An INP instruction is executed.
7. The read signal becomes active during the INP instruction.
8. Data is gated to the data lines during the INP.
9. A REPLY is returned within a specified time during the INP.
10. The read line drops when the REPLY is received during the INP.
11. The READ signal's dropping causes the REPLY signal to drop, allowing termination of the INP.
12. When the REPLY signal drops, it causes the data lines to drop.

Sequence for an Output Operation (OUT)

1. The peripheral equipment must be ready.
2. The address of the equipment is placed in the Q-register.
3. A function code is placed in the A-register. (A function code will be sent to the peripheral device to prepare it to receive data. The director bit of Q must be a logic 1.)
4. An OUT instruction must be executed.
5. The director bit of Q must be changed to a logic 0.
6. The information to be output is placed in the A-register.
7. A second OUT instruction is executed.
8. The write becomes active during this OUT instruction.
9. The data lines transfer information to the peripheral equipment during the OUT.

10. The peripheral device sends a REPLY during the OUT.
11. The WRITE signal drops when the REPLY is received during the OUT.
12. When the WRITE signal drops, the REPLY signal drops.
13. The data lines drop.

The sequence of events that occurs during an input or output operation ensures that no data is lost during a transfer.

Check Your Understanding

DIRECTIONS: Place the following list of events for an input operation into the correct sequence. More than one entry may go on a numbered blank.

1. _____	READ signal drops
2. _____	Change director bit in Q
3. _____	REPLY
4. _____	INP instruction
5. _____	READ signal becomes active
6. _____	Function code placed in A-register
7. _____	Data lines drop
8. _____	OUT instruction
9. _____	Peripheral ready
10. _____	REPLY drops
11. _____	Address of peripheral in Q
12. _____	Data gated to data lines

DIRECTIONS: Place the following list of events for an output operation into the correct sequence. More than one entry may go on a numbered blank.

13._____	Address of peripheral in Q
14._____	WRITE signal becomes active
15._____	Data lines transfer information
16._____	Function code placed in A-register
17._____	Information places in A-register
18._____	Change director bit in Q
19._____	Peripheral ready
20._____	2nd OUT instruction
21._____	Data lines drop
22._____	REPLY
23._____	WRITE signal drops
24._____	REPLY drops
25._____	1st OUT instruction

ANSWERS

1. Peripheral ready 2. Address of peripheral in Q 3. Function code placed in A-register 4. OUT instruction 5. Change director bit in Q 6. INP instruction 7. READ signal becomes active 8. Data gated to data lines 9. REPLY 10. READ signal drops 11. REPLY drops 12. Data lines drop 13. Peripheral ready 14. Address of peripheral in Q 15. Function code placed in A-register 16. 1st OUT instruction 17. Change director in Q 18. Information placed in A-register 19. 2nd OUT instruction 20. WRITE signal becomes active 21. Data lines transfer information 22. REPLY 23. WRITE signal drops 24. REPLY drops 25. Data lines drop

PROGRESS CHECK

1. During an I/O operation on the CYBER 18, bits 7 through 10 of the Q register contain the _____.

   a. equipment code
   b. status code
   c. function code
   d. DMA

2. On the CYBER 18, which peripheral uses the DMA data transfer method?

   a. Magnetic tape
   b. Magnetic disk (storage module drive)
   c. Line printer
   d. Card reader

3. On the CYBER 18, during equipment addressing, how is the W field used?

   a. It holds a function code.
   b. It holds a peripheral address code.
   c. It is not used.
   d. Only bit 11 is used.

4. Data transfer between the CPU of the CYBER 18 and peripherals that is completely controlled by program execution is called _____.

   a. DMA
   b. status code
   c. programmed I/O
   d. data

5. On the CYBER 18-20, if no data is available from the peripheral when demanded, with what does the peripheral respond?

   a. Reply
   b. Reject
   c. Standby
   d. Wait

6. Input/output operations in the CYBER 18-20 system are initiated by _____ instruction(s).

   a. one
   b. two
   c. three
   d. four