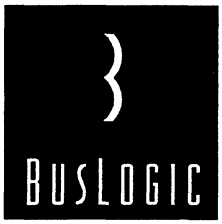
Technical Reference Manual



BT-646

FAST SCSI MICRO CHANNEL HOST ADAPTER

REVISION HISTORY

Revision	Change Activity	Date
A	Release	05/01/92
B	Release	10/30/92

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operations.

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PREFACE

AUDIENCE

This manual is intended for individuals who will be installing and configuring the BusLogic BT-646 host adapter board in a Micro Channel™ host system. It is also intended for system design engineers interested in designing software drivers for either single or multitasking operating systems.

SCOPE

This manual contains the information an individual needs to unpack, to install, and to configure the BT-646 in a Micro Channel host system. It also contains a complete operational description of the BT-646's hardware control registers. Finally, the manual explains the software interface between the Micro Channel host system and the BT-646.

CONTENTS

The information in this manual is divided into five sections and three appendices:

- Section 1 provides a functional description and overview of the BT-646's major components.
- Section 2 contains installation and configuration instructions.
- Section 3 describes the connector pin assignments for the Micro Channel bus, for the SCSI bus, and for the floppy interface.
- Section 4 explains the BT-646's hardware operation.
- Section 5 describes the BT-646's software operation. It explains how the Micro Channel host system and the BT-646 communicate.
- Appendix A discusses the BT-646's internal diagnostics.
- Appendix B describes 32-bit mode addressing.
- Appendix C provides a list of acronyms used in this manual.

Related Publications

- BusLogic's Micro Channel SCSI Host Adapter BT-646 Data Sheet
- BusLogic's Micro Channel SCSI Host Adapter BT-646 Installation Guide
- The Micro Channel installation and set-up guide
- The operating system installation and user's guide
- The Micro Channel computer technical reference manual (optional)
- The installation guide for third-party device drivers (optional)
- Small Computer System Interface, ANSI X3.131-1986 American National Standards (optional).

Notational Conventions

The following conventions are used throughout this manual:

Convention	Description
UPPERCASE	Used to indicate the names of keys.
-	A hyphen indicates an active low signal.
+	A plus sign indicates an active high signal.
BT-646	The term used to refer inclusively to the BT-646S and BT-646D boards.

1

INTRODUCTION

This section provides a functional description of the BusLogic BT-646 host adapter. It also supplies an overview of the BT-646's major components.

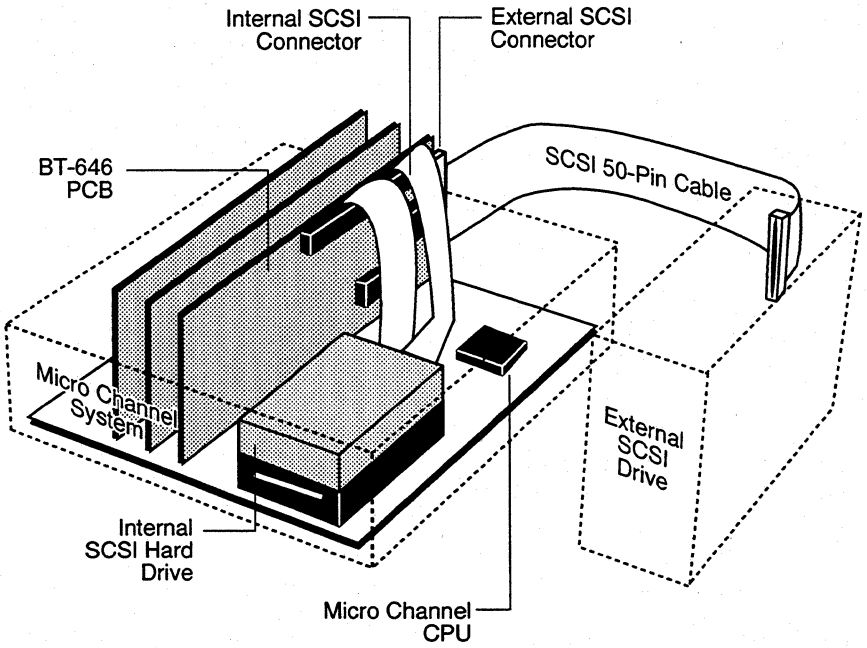
PRODUCT OVERVIEW

The BusLogic BT-646 host adapter is an intelligent Micro Channel to SCSI bus master host adapter product based on a BusLogic-designed, universal ASIC technology. It provides a high-performance interconnection between the Micro Channel bus and Small Computer System Interface (SCSI) peripheral devices. The BT-646 is designed for multitasking applications such as UNIX™, XENIX™, NetWare™, and OS/2. Already fully supported by these and other popular operating systems, the BT-646 requires no special software drivers. This is because it already provides a superset of the AHA-1646's™ I/O registers and command protocol at the interface level. A BusLogic-designed bus master controller ASIC, an advanced SCSI controller chip and a 16-bit microprocessor provide higher speed, lower power consumption, fewer parts and higher reliability.

The BT-646 supports a full 32-bit address path and can access up to four Gigabytes of system memory. Thus the total memory supported is limited only by the packaging constraints of the individual product rather than by the system architecture.

Bus master 8-, 16-, or 32-bit data transfers are performed at speeds of up to 40 MBytes/sec on the Micro Channel bus. The BT-646S supports single-ended SCSI drives with asynchronous data rates of up to 7 MBytes/sec and synchronous data rates of up to 10 MBytes/sec with the proper termination and cabling. The BT-646S uses low dropout voltage regulator and 100 ohm resistor to provide active termination on the SCSI bus. The BT-646D supports differential SCSI drives with asynchronous data rates of up to 7 MBytes/sec and synchronous data rates of up to 10 MBytes/sec. The BT-646D uses the 330 ohm/150 ohm/330 ohm resistor sets for the SCSI bus termination. Both internal and external 50-pin connectors are included on the board for flexibility in attaching SCSI devices to the system.

As illustrated in Figure 1-1, the BT-646 plugs into a Micro Channel system and supports the attachment of internal SCSI drives or the connection to external SCSI peripheral devices in add-on enclosures.



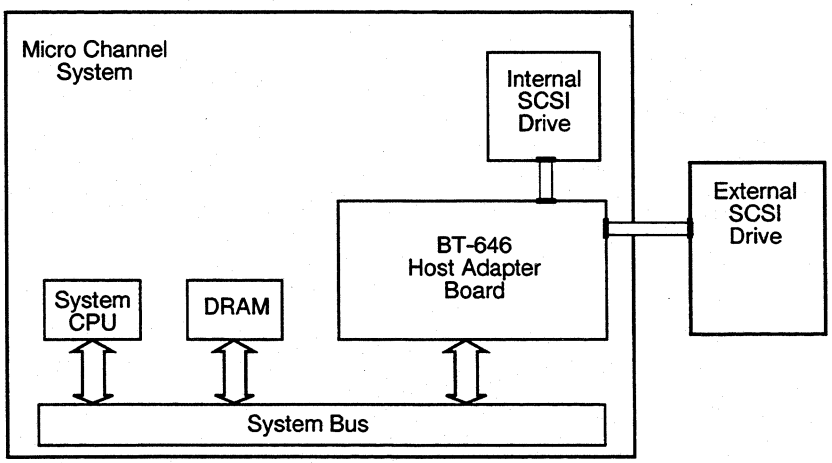


Figure 1-1. System Architecture

Figure 1-2 is a functional block diagram illustrating the major elements in the BT-646's design. The following paragraphs describe each component. The circled numbers in the text corresponds to the circled numbers in the figure.

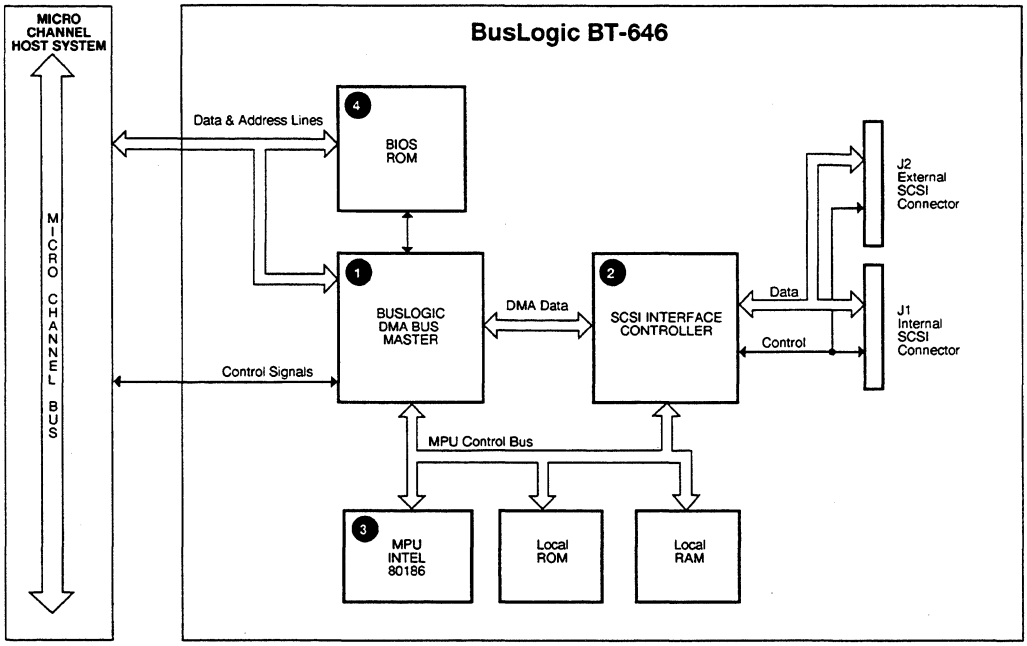


Figure 1-2. Host Adapter Architecture

Bus Master DMA Controller

All Micro Channel host bus interface logic is provided on the board by the BusLogic-designed bus master ASIC ❶. This chip provides bus master capabilities which greatly reduce the involvement of the host system's CPU in I/O control and data transfer activities. Under control of this chip, 8-,16-, or 32-bit bus master transfers of at up to 40 MBytes/sec to and from the main system memory are possible with the use of its internal 128-byte FIFO. A true multi-tasking mailbox structure supports up to 255 tasks. The BT-646 automatically enables and disables the data streaming to match the hardware capability of the motherboard. If the motherboard supports data streaming, the BT-646 will transfer data in streaming mode. If the motherboard does not support data streaming, the BT-646 will transfer data in non-streaming mode. This performance and improved bus utilization significantly enhances multitasking and multi-user applications.

Advanced SCSI Controller

On-board control of the interface to SCSI peripheral devices is provided by another ASIC, the advanced SCSI interface controller ❷. Up to 10 MBytes/sec synchronous and 7 MBytes/sec asynchronous SCSI data transfers are supported by the SCSI interface controller. With this chip, the BT-646 can operate either in an initiator or target role. This low-power, high-performance CMOS component completely conforms to the ANSI standard, X3.131-1986 for the Small Computer System Interface. The chip reduces protocol overhead by performing common SCSI algorithms or sequences in response to a single host command.

Microprocessor Unit (MPU)

An on-board, 16-bit Intel 80186 microprocessor unit ❸ coordinates all of the activity on the BT-646 under the direction of the board's firmware PROM. Consequently, the on-board MPU orchestrates such activities as the initialization, command decoding, interrupt generation and the control of the data flow among the board's components.

Local BIOS PROM

The BT-646 can be used in place of or in conjunction with a standard Micro Channel hard disk controller. The BT-646's on-board local BIOS ❹ provides a compatible method of attaching a SCSI hard drive to a Micro Channel system just as any other type of hard disk is connected. The BT-646's BIOS intercepts each host software interrupt that requests a disk I/O service and manages these interrupts according to the address of the requested drive. If the designated drive is a disk assigned to the Micro Channel system's internal disk controller, the BT-646's BIOS passes the command on to that disk controller. If the designated disk is one of the SCSI disks attached to the BT-646, the BT-646's BIOS responds to the request and instructs the BT-646 to execute the command.

SPECIFICATIONS

Table 1-1. Physical and Electrical Specifications

Size	Length: 11.5"	Width: 3.5"	Height: 0.5"
Operating Voltage	5 ± 0.25V		
Operating Current	1.5 Amperes Max.		
Max. Ripple/Noise	100 mV		
Temperature	0°C to 60°C (32–140°F)		
Relative Humidity	10–95% Non-condensing		
Altitude	0–10,000 ft. (Operating) 0–15,000 ft. (Storage)		

HARDWARE AND SOFTWARE REQUIREMENTS

The BT-646 can be installed in any Micro Channel compatible computer. To install the BT-646 successfully you must have part or all of the following hardware and software.

Hardware

Micro Channel computer system with the following:

- One available Micro Channel 16-bit or 32-bit expansion slot
- DC power for an internal 5.25" or 3.5" SCSI drive or an external subsystem with the corresponding D-shell, 50-pin external cable
- One Common Command Set (CCS) SCSI-2 compatible disk drive
- One 50-pin flat ribbon cable to connect internal SCSI devices to the BT-646.

Software

- PC-DOS or MS-DOS
- IBM OS/2 or MS-OS/2
- Interactive Unix or SCO UNIX/XENIX "GT" version
- Novell NetWare 286/386
- Micro Channel configuration diskette
- Included or third-party device drivers for each operating system.

REFERENCE DOCUMENTS

- BusLogic's Micro Channel SCSI Host Adapter BT-646 Data Sheet
- BusLogic's Micro Channel SCSI Host Adapter BT-646 Installation Guide
- The Micro Channel installation and set-up guide
- The operating system installation and user's guide
- The Micro Channel computer technical reference manual (optional)
- The installation guide for third-party device drivers (optional)
- Small Computer System Interface, ANSI X3.131-1986 American National Standards (optional).

2

UNPACKING AND INSTALLATION

This section describes how to unpack, to inspect, to configure, and to install the BT-646S and BT-646D host adapter boards in a Micro Channel host system. It also describes how to initialize the software and set the host adapter options for operation in Micro Channel-compatible systems. Refer to Figure 2-1 for an illustration of the BT-646 board.

UNPACKING AND INSTALLATION

Before handling the BT-646, please take the necessary electro-static discharge precautions. Touch your computer on a metal part to discharge static electricity before handling the board. The board should always be held by the edges even after static electricity is discharged.

While practicing appropriate anti-static precautions, remove the BT-646 from its protective envelope. Verify that no physical damage occurred during shipping by inspecting the board for bent pins, loose parts, broken traces, and chipped or broken connectors.

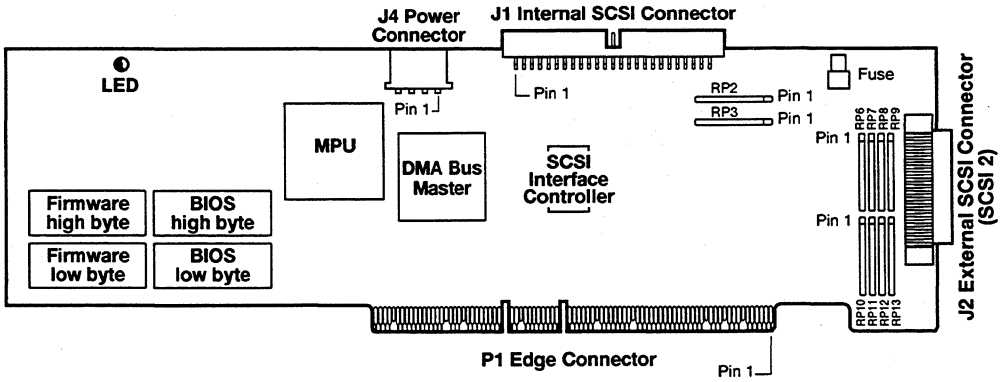


Figure 2-1. The BT-646 Host Adapter Board

INSTALLATION TOOLS

The following items, available from any authorized dealer, may be needed to assist with the installation of the BusLogic BT-646 board for your Micro Channel system:

- Micro Channel technical manuals
- Hard disk drive(s) manuals
- Micro Channel system reference diskette(s)
- Micro Channel CF (Configuration) program
- **SETUP**, **FDISK**, and **FORMAT** programs
- Small screwdriver
- Small needle-nosed pliers.

CONFIGURATION INSTRUCTIONS

General

The BT-646 must be configured for use by performing the following actions:

- Configuring SCSI devices
- Verifying that the terminators are installed correctly
- Placing the BT-646 board into the Micro Channel computer slot
- Setting host adapter software options
- Cabling the on-board connector to a SCSI target.

HOST ADAPTER INTEGRATION

This section describes device termination, cabling requirements, and SCSI device ID selection.

Device Termination

SCSI devices are daisy chained together with a common cable. All SCSI devices operate on common signals, and both ends of the cable are terminated with hardware "terminators." Terminators, which can be connected to either SCSI devices or SCSI cables, are required to make data transfers on the SCSI bus reliable.

Devices connected to SCSI chains must have the correct number of terminators for proper operation and to prevent damage to the SCSI chip on the BT-646 board. There can be no more than two terminators in a chain of SCSI devices—one at each end of the physical chain. This means that, if more than two SCSI devices are connected in a SCSI daisy chain, the middle device(s) in the control cable must have the terminator resistor packs on the device(s) removed. See Figure 2-2 for the possible configurations of terminators in a SCSI system.

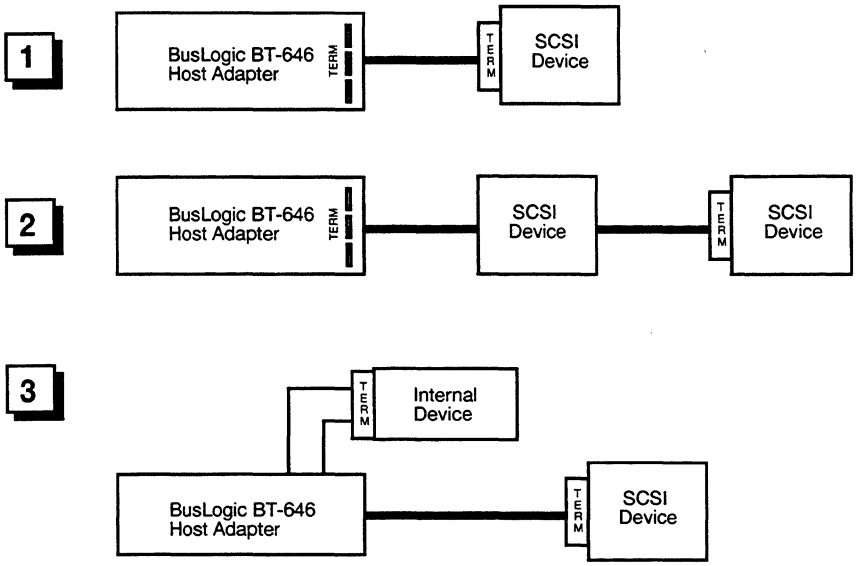


Figure 2-2. SCSI Terminator Configurations

Cabling Requirements

Selecting the proper SCSI cable for a particular system configuration is of great importance. If two or more SCSI devices are configured in a SCSI daisy chain, the devices must be connected by a 50-conductor daisy-chain cable.

Before plugging in cable connectors, check that the "▼" mark molded on the connector or the colored stripe on the cable (indicating the location of Pin 1) matches Pin 1 of the connector on the BT-646 board.

SCSI Device ID Selection

The SCSI ID is a number between 0 and 7 assigned to any SCSI device. The SCSI ID number is used by the computer to communicate with the devices connected to it. All SCSI devices must have a unique SCSI number to identify it on the SCSI chain. A SCSI device is usually fixed as either an initiator or a target, when two or more SCSI devices communicate, but some devices are capable of performing either role. Devices with higher ID numbers have a higher priority in communicating with the computer.

Most SCSI peripheral devices are shipped with a preassigned SCSI ID number. A SCSI ID switch is usually located on the back panel of such devices. Change the SCSI ID of other peripheral devices only as recommended in the owner's manual. Refer to the heading, "Micro Channel Configuration Settings," later in this manual for procedures on how to set the SCSI ID number of the BT-646.

Disk Drive Power Connector

A 4-pin disk drive power connector (J4) is located at the top edge of the BT-646 board next to the SCSI connector J1. This connector provides standard +12V and +5V power to disk drives.

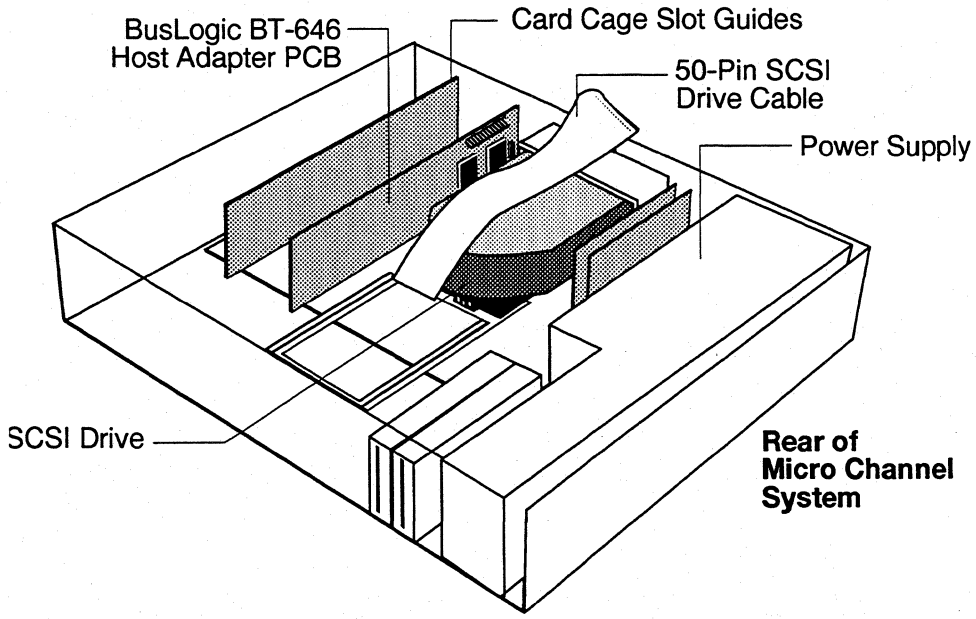
Note: *The BT-646 brings the 12 volt power supply to the 4-pin power connector (J4) via three gold fingers on the edge connector. The power rating of the Micro Channel edge connector on the 12 volt is one ampere per finger. Consequently, the maximum power allowed from the 12 volts (Pin 1 of J4) is three amperes. Because certain large SCSI drives may require more than three amperes when their motors are spinning up, BusLogic recommends that this connector* not *be connected to these large SCSI drives.*

Based on the power rating of the SCSI drives, it is generally recommended that this power connector not *be daisy chained to multiple drives.*

INSTALLING THE BT-646

This section describes how to install the BT-646 in a 16-bit or 32-bit slot inside the Micro Channel host system and how to connect it to other devices. Install the BT-646 in your computer by performing the following steps:

1. Remove power from the host system.
2. Referring to the host system owner's manual, open the case to gain access to the motherboard and expansion slots. If the computer has been on, wait a few minutes until the power supply case has cooled down inside the computer. If the power supply case is cold, touch it to discharge any static electricity that may be on your clothes or body. If a disk controller drive board has been installed, remove all connecting cables to the board and then lift it out of the host computer.



Front of Micro Channel System

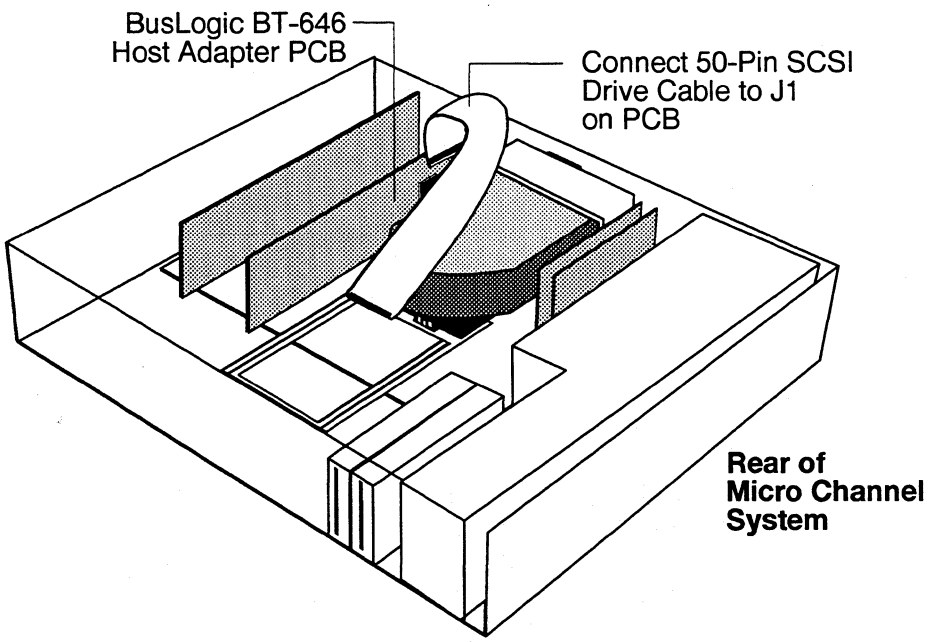
3. Remove the mounting screw and the existing bracket from the rear panel behind the 16-bit or 32-bit slot that has been selected for insertion of the BT-646. The Micro Channel slot closest to the internal hard drive(s) is the best choice.

4. If the BT-646 will be installed in a host which is not at either end of the SCSI bus, terminators on the board will need to be removed.

   For the BT-646S, RP2 and RP3 are the terminators. RP2 and RP3 are resistor packs containing 9 bused 100 ohm resistors.

   For the BT-646D, RP6 through RP13 are the terminators. RP6, RP8, RP10, and RP12 are resistor packs containing 5 isolated 150 ohm resistors. RP7, RP9, RP11, and RP13 are resistor packs containing 9 bused 330 ohm resistors.

   See the heading, "Host Adapter Integration," in this manual for more information regarding device termination. The BT-646 is shipped with terminators installed.



Front of Micro Channel System

5. Press the BT-646 downward into the selected 16-bit or 32-bit slot, align the mounting bracket, and reinstall the mounting screw.

Caution: *Make sure that the board is properly seated in the slot.*

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6. Connect the large 50-pin connector within the host computer to the single-ended SCSI connector, J1. Place the connector cable around the power supply and over any other boards. Depending on the configuration of your computer, other types of cables could be used. See the heading, "Cabling Requirements," for details.

7. Verify that all connections are secure.

8. Reattach and close the cover of the host computer as described in the system owner's manual.

MICRO CHANNEL CONFIGURATION SETTINGS

The BT-646 fully supports the Micro Channel automatic configuration facility and is operational with most computers using the default settings in the BT-646 configuration diskette supplied with the board. The host adapter configuration options will need to be changed if conflicting port assignments or memory allocation is encountered. Every BusLogic Micro Channel controller comes with a floppy diskette which contains the BusLogic configuration file (@0708.ADF).

Before starting, perform the following steps:

1. Prepare a back-up copy of the system reference diskette provided with your host computer.

2. Place the back-up system reference diskette in the floppy drive and then reboot your system by pressing the CONTROL, ALTERNATE, and DELETE keys simultaneously.

3. After the boot is completed, the system's main menu will appear. Select the Copy on Option Diskette command and follow the instructions to copy the @0708.ADF file from the BusLogic-supplied diskette.

4. When the main menu reappears, select the Set Configuration command. Select the Change Configuration command and then follow the directions on your screen to select the BT-646.

The default settings for configuration options as shown on the screen are illustrated in Figure 2-3. Move the cursor to the field desired, press the **F5** or **F6** keys to scroll through the selections for each option and then leave the field to select the option desired.

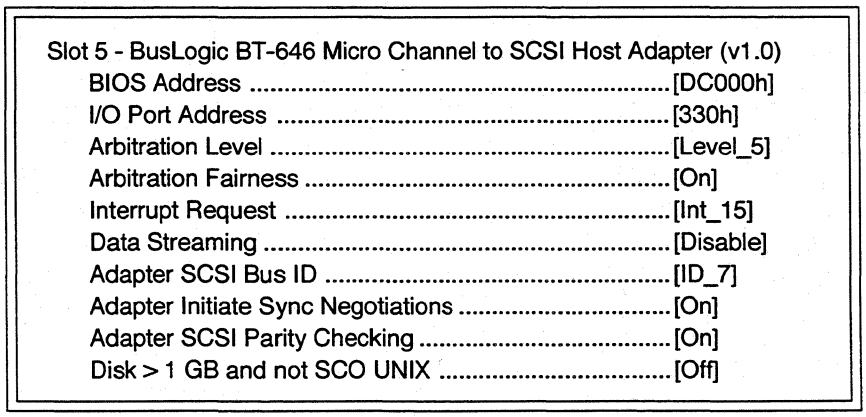


Figure 2-3. Configuration Settings

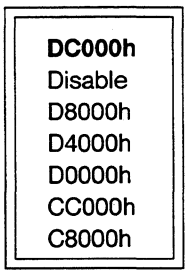
Note: *For details on greater than 1 GB drive support, refer to the heading, "Disk > 1GB and not SCO UNIX," later in this section.*

Before operating the BT-646, verify that the configuration settings have been set according to the target system's operating requirements. The following paragraphs describe the settings for each configuration option.

BIOS Address. The BIOS address resides within the host memory map and is executed by the host even though it is physically located on the BT-646. The BIOS intercepts host interrupt 13H and then dispatches a command to the BT-646 for all host to SCSI disk accesses under the DOS environment. This setting allows you to select the starting address of a 16K Byte memory slot within the host memory space for the BIOS.

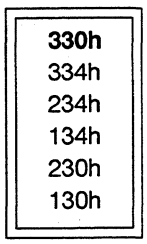
If more than one host adapter is installed within the same Micro Channel host system, only one can have the BIOS enabled. The BIOS on each additional host adapter must be disabled. *The default setting for this option is DC000H.*

BIOS Address



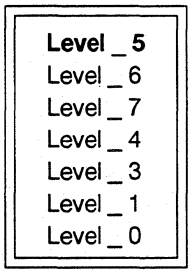
I/O Port Address. The host communicates with the BT-646 via the BT-646's three I/O registers. (Refer to Section 4 of this manual for more details on these registers.) This setting lets you define the base I/O address of these three registers within the host I/O map. Note that each board within the same Micro Channel host system must have its unique I/O register addresses to prevent hardware conflicts. *The default starting address is 330H.*

Host Adapter Configuration
I/O Port Address



Arbitration Level. In order for the BT-646 to become a bus master on the Micro Channel bus, it must make a request to start a bus arbitration. Once a request is made, the arbitration cycle is initiated by the central arbiter of the system as soon as the present bus master releases the bus. Among all of the participating arbiters, the one with the highest priority will win control of the channel. This option allows the user to define the arbitration level for the BT-646. Arbitration level 0 has the highest priority and level 7 has the lowest priority. *The default setting is level 5.*

Arbitration Level

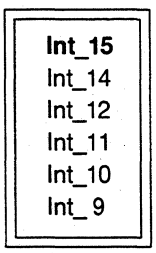


Arbitration Fairness. In order for the lower priority arbiters to gain control of the channel, the Micro Channel has an arbitration fairness feature. If the arbitration fairness feature is turned off, the arbitrating device that owns the channel may immediately participate in the next arbitration cycle as soon as it releases the channel. If the arbitration fairness feature is turned on, it will not participate in any arbitration cycle until all other requesting devices have been serviced. This option allows you to set the arbitration fairness on or off. *The default setting is fairness on.*

Interrupt Request. The BT-646 generates a hardware interrupt to the host whenever an interrupt condition exists. (Refer to the description of the Interrupt Register in Section 4 of this manual for details on this register.) You can use this setting to specify the hardware interrupt line on the Micro Channel bus that the BT-646 should use to generate interrupts to the host.

Each selected hardware line is level triggered. Level-triggered interrupts assert interrupts low. Level-triggered interrupts allow multiple boards to share the same hardware interrupt line on the Micro Channel bus. Note that unless the device drivers have the capability of handling shared interrupts, each board in the Micro Channel host system must be assigned a unique hardware interrupt line to prevent conflicts. *The default setting for this option is Channel 15*

Interrupt Request



Data Streaming. The streaming data procedure on the Micro Channel bus provides performance improvements over basic transfer procedures for block transfers. Data transfer rates of up to 40 MBytes/sec are supported. The transfer of a data block is supported by using a single address followed by multiple 16 or 32-bit data transfers within a single streaming data cycle. Note, however, that certain motherboards may not support data streaming. This option allows you to enable or disable data streaming based upon the motherboard used. *The default setting is to have data streaming disabled.*

Data Streaming

Disable
Enable

Adapter SCSI Bus ID. There are eight SCSI IDs (0–7) on a SCSI bus. SCSI ID 7 has the highest priority. Each initiator or target on a SCSI bus must be assigned a unique SCSI ID.

This setting enables you to define the SCSI ID for the BT-646 on the SCSI bus. Because the BT-646 is an initiator on the SCSI bus dispatching host commands to all SCSI targets on the bus, the default SCSI ID is 7. Note that the BT-646's on-board BIOS requires that your SCSI drives be configured for SCSI ID 0 and 1. This requirement is important only if you intend to boot your system from the BT-646. *The as-shipped (default) SCSI ID is 7.*

SCSI Configuration
Adapter SCSI Bus ID

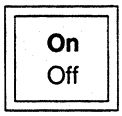
ID = 7
ID = 6
ID = 5
ID = 4
ID = 3
ID = 2
ID = 1
ID = 0

Adapter Initiate Synchronous Negotiation. The SCSI protocol allows synchronous negotiation to determine the REQ/ACK offset and the data transfer rate for synchronous transfers between an initiator and a target on the SCSI bus. The actual data transfer rate is determined by the lower of the rates between the initiator and the target. Because the BT-646 is capable of up to 10 MBytes/sec SCSI data transfers, the actual data transfer rate is determined by the SCSI drive if the drive has a data transfer rate lower than or equal to 10 MBytes/sec. *The default setting is on.*

The default mode assumes that a SCSI target device connected to the BT-646 will initiate the synchronous negotiation. Some target devices require that they initiate the synchronous negotiation. Such devices may fail to respond to commands from the BT-646 if a synchronous negotiation occurs unexpectedly. Conversely, other target devices may expect an initiator to begin the synchronous negotiation se-

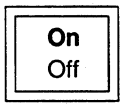
quence. If this class of SCSI target devices is connected to the BT-646, the option may be enabled to allow the host adapter board to initiate the negotiation for a synchronous data transfer with a selected SCSI target device.

Adapter Initiate
Sync Negotiation



Adapter SCSI Parity Checking. There are 8 bits of data plus one bit of parity on a standard SCSI bus. This setting allows you to turn parity on or off on the SCSI bus. *The default setting is to have parity turned on.*

Adapter SCSI Parity Checking



Disk > 1 GB and not SCO UNIX. In the DOS environment, INT 13 calls are routed through the BT-646's ROM BIOS. This on-board BIOS intercepts host interrupt 13H calls and dispatches a command to the BT-646 for all host to SCSI disk accesses. When the >1GB option is turned on, the BT-646 BIOS can access up to 8 GBytes per disk. Otherwise, it can only access the first 1 GBytes even if the formatted disk capacity is greater than 1GByte.

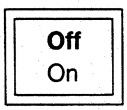
This 1GByte restriction does not apply to other operating systems, such as NetWare, UNIX, SCO UNIX 3.2.4, or OS/2 if the operating system can boot without accessing > 1 GBytes. If the operating system's bootable image resides below 1 GBytes then it can boot via Interrupt 13H. Once any of these operating systems are booted, the disk accesses are not routed through Interrupt 13H and the operating system can access the entire disk space even if the > 1 GB option is not turned on.

Under SCO UNIX 3.2.2, the >1GB option must be turned off because the operating system itself has a 1 GByte limitation. Otherwise, disk images may be corrupted when the 1 GByte boundary is reached. For SCO UNIX 3.2.4, the operating system does not impose the 1 GByte limit, and this option can be turned on or off accordingly.

Consequently, the >1GByte support must be turned on under the following two conditions: (1) the combined space of all the DOS partitions exceeds 1GByte, or (2) >1GByte disk accesses are required to boot the operating system. To enable the > 1 GB support, turn on this option.

Note: *If this option is changed, you must reformat the disk to avoid corrupting the existing file system.*

Disk > 1 GB and not SCO UNIX



HARD DISK INITIALIZATION

This section describes the system set up, initialization, partitioning and formatting of hard disk drives used with the BT-646. These procedures will erase all data on your disk drives. Before following these procedures make sure that all necessary data is backed up on another drive.

Set-up, Initialization and Partitioning Procedure

To perform set up, initialization, and partitioning, proceed as follows:

1. Reboot the host system and insert the MS-DOS diskette containing the **DEBUG** program.

2. After the MS-DOS prompt, type the following for low-level format:

   debug <RETURN>

   The system responds with the "-" prompt.

   A) Type **g=dc00:6 <RETURN>** if the host BIOS address is set for this; otherwise, enter the correct BIOS address.

3. Perform the following steps on your screen monitor to configure and perform a low-level format on attached devices:

   A) The **SCSI Fixed Disk Format Utility** appears on the screen. Enter **1** to view the attached devices and then press **<RETURN>**.

   SCSI Fixed Disk Format Utility

   ```
   1. Show all installed drives
   2. Select next drive
   3. Format current drive
   4. Verify current drive
   5. Quit (exit to DOS)

   Enter Your Option: __
   ```

   B) A list of all attached drives appears under the option prompt. Press the **2** key until the drive to be formatted is the current drive.

   C) Press **3 <RETURN>** to format the drive. The following prompt appears:

   ```
   All data on this drive will be lost!
   Proceed with low level formatting? (Y/N) __
   ```

   Enter **Y** to proceed with low-level formatting and follow the instructions as they appear on the screen.

D) The system will format the SCSI drive selected. When the format is completed, press any key to go back to the main menu shown in the preceding Step 3A. Enter **4** to verify the drive and then press **<RETURN>**. The following prompt appears.

```
All data on this drive will be verified.
and bad data areas will be reassigned.
Proceed with low level verification? (Y/N) __
```

Enter **Y** to proceed with verification.

E) When the verification is finished, press any key to go back to the main menu shown in the preceding Step 3A. To exit to DOS, type:

5 <RETURN>

The following Steps 4 and 5 may not be necessary if the operating system to be installed is not DOS.

4. Run the DOS **FDISK** program to partition the disk for the number of cylinders to be used by DOS. The following steps are recommended for users who are not familiar with the DOS **FDISK** program. See your DOS manual for information on the **FDISK** command.

A) Enter **fdisk <RETURN>.** The following menu appears.

```
FDISK Options
Current Fixed Disk Drive: C
Choose one of the following:
 1. Create DOS Partition
 2. Change active Partition
 3. Delete DOS Partition
 4. Display Partition Information
Enter Choice: [1]
```

B) Enter **1 <RETURN>** to create a DOS partition. The following menu appears.

```
Create DOS Partition
Current Fixed Disk Drive: C
Choose one of the following:
 1. Create Primary DOS Partition
 2. Create Extended DOS Partition
Enter Choice: [1]
```

C) Enter **1 <RETURN>** to create a primary DOS partition. The next menu appears.

```
Create Primary DOS Partition
Current Fixed Disk Drive: C
Choose one of the following:
Do you wish to use the maximum size
for a DOS partition and make the DOS
partition active (Y/N).....? [Y]
```

D) Enter **Y <RETURN>** to create a primary DOS drive partition with the maximum size. The following prompt appears.

```
System will now restart
Insert DOS diskette in drive A:
Press any key when ready . . .
```

When the partitioning has been completed (indicated by another prompt), press any key to return to DOS.

5. Install DOS by running the **FORMAT** program as instructed by DOS normal installation procedures. The next steps are recommended for operators who are not familiar with the DOS **FORMAT** program.

A) Run the **FORMAT** program by typing:

format c:/s/v <RETURN>

B) The system displays the following format warning:

```
WARNING: ALL DATA ON NON-REMOVABLE DISK
DRIVE C: WILL BE LOST!
Proceed with Format (Y/N)?
```

C) Type**Y <RETURN>.**

D) When the format has been completed, the following prompt appears.

```
Format complete
System transferred
Volume label ( 11 characters, ENTER for name )?
```

E) Enter any legal file name to label the volume just created. Refer to your system operator's manual for more details on the DOS format procedures.

This concludes the BT-646 hardware and software installation procedures.

If damage to the board has occurred, return it in the protective envelope with this manual to your BusLogic board supplier. The shipping agent should also be notified if the unit has been damaged during shipment. The BusLogic warranty conditions are given in the back of this manual.

3

ELECTRICAL INTERFACE

This section provides the user with a complete description of the name, function, and applicable logic level of all signals between the BT-646 and the host system. It also describes the signals processed by the SCSI protocol chip and the floppy controller chip. This section is divided into two parts:

- Micro Channel System Bus Electrical Interface and
- SCSI Bus Electrical Interface.

MICRO CHANNEL SYSTEM BUS ELECTRICAL INTERFACE

The BT-646 is electrically and mechanically compatible with the Input/Output (I/O) bus used in Micro Channel computers. Physically, this I/O bus is contained on the card edge connector. The bus master control logic on the BT-646 controls the Micro Channel system bus arbitration and data transfer operations. During bus master data transfers, the BT-646 takes control of the system bus and transfers data directly to and from the main system memory. Both odd and even starting addresses are supported by the BT-646.

The Micro Channel system I/O bus provides the necessary hardware interface to the host Central Processing Unit (CPU) to allow it to communicate with the BT-646. Figure 3-1 identifies the positions of connector rows on the BT-646's board edge.

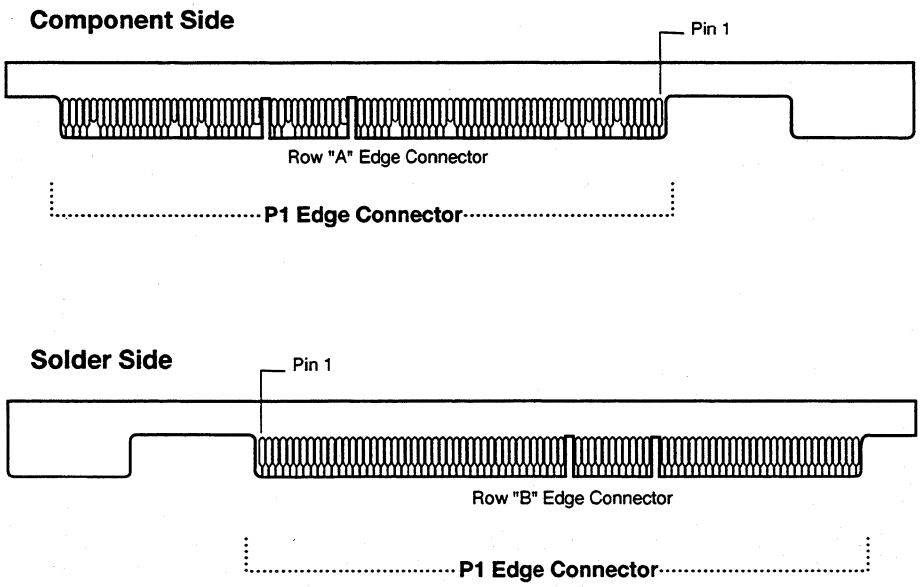


Figure 3-1. Connector Rows on the BT-646 Board Edge

Summary of Micro Channel Signals

Tables 3-1 through 3-4 show the signals on the Micro Channel connectors that support the Micro Channel bus. The pin assignments for the I/O channel connectors on both sides of P1, an 89-pin edge connector are summarized.

Table 3-1. P1 Component Side Row "A" Edge Connector

Signal Pin #	Signal Name	Direction
A1	- CD SETUP	Input
A2	MADE 24	I/O
A3	GND	Ground
A4	A11	I/O
A5	A10	I/O
A6	A09	I/O
A7	+ 5Vdc	Power
A8	A08	I/O
A9	A07	I/O
A10	A06	I/O
A11	+ 5Vdc	Power
A12	A05	I/O
A13	A04	I/O
A14	A03	I/O
A15	+ 5 Vdc	Power
A16	A02	I/O
A17	A01	I/O
A18	A00	I/O
A19	+ 12 Vdc	Not Used
A20	- ADL	I/O
A21	- PREEMPT	I/O
A22	- BURST	I/O
A23	- 12 Vdc	Not Used
A24	ARB 00	I/O
A25	ARB 01	I/O
A26	ARB 02	I/O
A27	- 12 Vdc	Not Used
A28	ARB 03	I/O
A29	ARB/-GNT	Input
A30	- TC	Not Used
A31	+ 5Vdc	Power
A32	- S0	I/O
A33	- S1	I/O
A34	M/-IO	I/O
A35	+ 12Vdc	Power
A36	CD CHRDY	Output
A37	D00	I/O
A38	D02	I/O
A39	+ 5Vdc	Power
A40	D05	I/O
A41	D06	I/O

Table 3-1. P1 Component Side Row "A" Edge Connector (Continued)

Signal Pin #	Signal Name	Direction
A42	D07	I/O
A43	GND	Ground
A44	- DS 16 RTN	Input
A45	- REFRESH	Not Used
A46	Access Key	Access Key
A47	Access Key	Access Key
A48	+ 5 Vdc	Power
A49	D10	I/O
A50	D11	I/O
A51	D13	I/O
A52	+ 12 Vdc	Power
A53	RESERVED	Not Used
A54	- SBHE	I/O
A55	- CD DS 16	Not Used
A56	+ 5 Vdc	Power
A57	- IRQ 14	Output
A58	- IRQ 15	Output
A59	RESERVED	Not Used
A60	RESERVED	Not Used
A61	GND	Ground
A62	RESERVED	Not Used
A63	RESERVED	Not Used
A64	RESERVED	Not Used
A65	+ 12 Vdc	Not Used
A66	D19	I/O
A67	D20	I/O
A68	D21	I/O
A69	+ 5Vdc	Power
A70	D24	I/O
A71	D25	I/O
A72	D26	I/O
A73	+ 5 Vdc	Power
A74	D30	I/O
A75	D31	I/O
A76	RESERVED	Not Used
A77	+ 12 Vdc	Power
A78	- BE3	Output
A79	- DS 32 RTN	Input
A80	- CD DS 32	Not Used
A81	+ 5 Vdc	Power
A82	A26	I/O
A83	A27	I/O
A84	A28	I/O
A85	+ 5 Vdc	Power
A86	RESERVED	Not Used
A87	RESERVED	Not Used
A88	RESERVED	Not Used
A89	GND	Ground

Table 3-2. P1 Solder Side Row "B" Edge Connector

Signal Pin #	Signal Name	Direction
B1	AUDIO GND	Not Used
B2	AUDIO	Not Used
B3	GND	Ground
B4	14.3 MHz OSC	Not Used
B5	GND	Ground
B6	A23	I/O
B7	A22	I/O
B8	A21	I/O
B9	GND	Ground
B10	A20	I/O
B11	A19	I/O
B12	A18	I/O
B13	GND	Ground
B14	A17	I/O
B15	A16	I/O
B16	A15	I/O
B17	GND	Ground
B18	A14	I/O
B19	A13	I/O
B20	A12	I/O
B21	GND	Ground
B22	- IRQ 09	Output
B23	- IRQ 03	Not Used
B24	- IRQ 04	Not Used
B25	GND	Ground
B26	- IRQ 05	Not Used
B27	- IRQ 06	Not Used
B28	- IRQ 07	Not Used
B29	GND	Ground
B30	RESERVED	Not Used
B31	RESERVED	Not Used
B32	- CHCK	Input
B33	GND	Ground
B34	- CMD	I/O
B35	CHRDYRTN	Input
B36	- CD SFDBK	Output
B37	GND	Ground
B38	D01	I/O
B39	D03	I/O
B40	D04	I/O
B41	GND	Ground
B42	CHRESET	Input
B43	RESERVED	Not Used
B44	RESERVED	Not Used
B45	GND	Ground

Table 3-2. P1 Solder Side Row "B" Edge Connector (Continued)

Signal Pin #	Signal Name	Direction
B46	Access Key	Access Key
B47	Access Key	Access Key
B48	D08	I/O
B49	D09	I/O
B50	GND	Ground
B51	D12	I/O
B52	D14	I/O
B53	D15	I/O
B54	GND	Ground
B55	- IRQ 10	Output
B56	- IRQ 11	Output
B57	- IRQ 12	Output
B58	GND	Ground
B59	RESERVED	Not Used
B60	RESERVED	Not Used
B61	RESERVED	Not Used
B62	RESERVED	Not Used
B63	GND	Ground
B64	D16	I/O
B65	D17	I/O
B66	D18	I/O
B67	GND	Ground
B68	D22	I/O
B69	D23	I/O
B70	RESERVED	Not Used
B71	GND	Ground
B72	D27	I/O
B73	D28	I/O
B74	D29	I/O
B75	GND	Ground
B76	- BE0	Output
B77	- BE1	Output
B78	- BE2	Output
B79	GND	Ground
B80	TR32	Output
B81	A24	I/O
B82	B25	I/O
B83	GND	Ground
B84	A29	I/O
B85	A30	I/O
B86	A31	I/O
B87	GND	Ground
B88	RESERVED	Not Used
B89	RESERVED	Not Used

P1 Input/Output Signal Descriptions

This section describes signals from each connector of the Micro Channel bus signals. I/O adapters should be designed with a maximum of two low-power Shottky (LS) loads per line. Signals preceded by a hyphen (-) indicate an active low signal.

Table 3-3. P1 Signal Descriptions

SIGNAL	DEFINITION
A0-A23	**Address Bits 0-23**: These signals are used to address memory and I/O slaves attached to the channel. A0 is the least significant bit (LSB) and A23 is the most significant bit (MSB). These 24 address lines allow access of up to 16 MBytes of memory. Only the lower 16 address lines (A0-A15) are for I/O operations, and all 16 lines must be decoded by the I/O slave. A0-A23 are generated by the controlling master. Valid addresses generated by the controlling master are unlatched on the channel and, if required must be latched by the slaves using either the leading or trailing edge of the Address Decode Latch signal or the leading edge of the Command signal. A0-A23 must be driven with tristate drivers.
A24-A31	**Address Bits 24-31**: These signals are used with A0-A23 to address memory attached to the channel. A0 is the LSB and A31 is the MSB. These 32 address lines allow access of up to 4 GBytes of memory. Only the lower 16 address lines (A0 -A15) are used for I/O operations. A24-A31 are generated by the controlling master. Valid addresses generated by the controlling master are unlatched on the channel and, if required, must be latched by the slaves using either the leading or trailing edge of the Address Decode Latch signal or the leading edge of the Command signal. The Address Bits 0-31 signals must be driven with tristate drivers.
-ADL	**Address Decode Latch**: This signal, driven by the controlling master, is provided as a convenient way for the slave to latch valid addresses and status bits. This signal can be used by slaves to latch the address from the bus. This signal is not active during Matched-Memory cycles. This signal is driven with a tristate driver.
ARB0-ARB3	**Arbitration Bus Priority Levels**: These signals comprise the Arbitration bus and are used to present priority levels for participants seeking control of the bus. The Arbitration Bus Priority Level 0-3 signals, the least significant through most significant bits respectively, support up to 16 priority levels. The highest hexadecimal value of the Arbitration bus (Hex F) has the lowest priority, and the lowest value (Hex 0) has the highest priority. A participant is allowed to change the state of the Arbitration bus only immediately after the rising edge of the Arbitrate/-Grant signal. All participants monitor the Arbitration bus and the lower priority participants withdraw their priority levels by not activating less-significant arbitration bits. The hexadecimal code of the highest priority requester is valid on the Arbitration bus after a settling time. After the channel is granted to a requester, the highest priority participant continues to drive its priority lines. These bidirectional lines are active high and must be driven with open-collector drivers.
ARB/-GNT	**Arbitrate/-Grant**: When the signal is high, it indicates an Arbitration cycle is in process. When it is low, it is the acknowledgment from the central arbitration control point to an Arbitrating bus participant (local arbiter) and the DMA controller that channel control has been granted. This signal is driven high by the central arbitration control point within a specified time after the Status Bits 0 and 1 signals, the Burst and the Command signal become inactive. The negative-to-positive transition of this signal initiates an Arbitration cycle; the positive-to-negative transition terminates the Arbitration cycle. Only the central arbitration control point activates and deactivates this signal. The signal must be used by all local arbiters to gate their address data and transfer control bus drivers off during Arbitration cycles. This signal is driven with a bus driver.

Table 3-3. P1 Signal Descriptions (Continued)

SIGNAL	DEFINITION
-BE0 — -BE3	**Byte Enable 0-3**: These signals are used during data transfers with 32-bit slaves to indicate which data bytes will be placed on the bus. Data transfer of 8,16,24, or 32 contiguous bits are controlled by these signals during transfers involving 32-bit slaves only. These signals are driven by the controlling master when the Translate 32 signal is inactive, and by the Central Translator Logic (for those operations involving a 16-bit master with a 32-bit slave) when the Translate 32 signal is active. These signals are unlatched on the bus and, if required, must be latched by 32-bit slaves. These signals are driven with tristate drivers.
-BURST:	**Burst**: This signal indicates to the central arbitration control point the extended use of the channel for transferring a block of data. This type of data transfer is called a Burst cycle. This signal is shared by all local arbiters. This signal is driven active by the local arbiter after being granted the channel. The local arbiter must deactivate this signal during the last transfer cycle. This signal must be driven with an open-collector driver.
-CD SFDBK (n)	**Card Selected Feedback**: When the controlling master addresses a memory slave or an I/O slave, the addressed slave drives this signal active as a positive acknowledgment of its presence at the address specified. The (n) indicates this signal is unique to each channel connector (one independent signal line per connector). This signal is unlatched by any slave with a valid select decode and is driven by any slave selected by any select mechanism except the Card Setup signal. The slave does not drive this signal during the Configuration cycle. This signal is driven with a totem-pole driver.
-CD SETUP (n)	**Card Setup**: This signal is driven by system logic to select individual channel connectors during system configuration and error-recovery procedures. The (n) indicates this signal is unique to each channel connector (one independent signal line per connector). When this signal is activated, a specific channel connector is selected and access to the adapter's configuration data space is obtained. The ID and configuration data can be obtained by an I/O Read operation; the configuration data is stored by an I/O Write operation. Each channel connector has a unique card setup signal. This signal is driven with a totem-pole driver.
CD CHRDY (n)	**Channel Ready**: This signal, normally active (ready), is pulled inactive (not ready) by a memory or I/O slave to allow additional time to complete a channel operation. The (n) indicates this signal is unique to each channel connector (one independent signal line per connector). During a Read operation, a slave ensures that data will be valid on the data bus within the time specified after releasing the signal to a Ready state. The slave also holds the data long enough for the controlling master to sample. A slave may also use this signal during a Write operation if more time is needed to store the data from the bus. This signal is derived with a valid address decode ANDed with status. This signal is driven with a totem-pole driver.
-CD DS 32_(n)	**Card Data Size 32**: This signal is driven by 32-bit slaves to provide an indication on the bus of a 32-bit data port at the location addressed. The (n) indicates this signal is unique to a channel connector position (one independent signal per connector). This signal is unlatched and derived from a valid address decode. All 32-bit slaves must drive this signal. This signal is inactive for an 8- or 16-bit data port. It must be driven with a totem-pole driver.
-CHCK	**Channel Check**: This signal is used to indicate a serious error (such as a parity error) that threatens the continued operation of the system. This signal is driven active to indicate the error condition and must remain active until the Channel Check signal's interrupt handler resets it. This signal is driven with an open-collector driver to allow sharing.

Table 3-3. P1 Signal Descriptions (Continued)

SIGNAL	DEFINITION
CHRDYRTN	**Channel Ready Return**: This output signal is a positive AND of the Channel Ready signals. If all devices drive the Channel Ready signal active, this output is active. It is provided to allow the controlling master to monitor the ready information. This signal must be driven with a bus driver.
CHRESET	**Channel Reset**: This signal is generated by the system logic to reset or to initialize all adapters at power on or during a low line voltage condition. During a power-on sequence, this signal is active for a specified minimum time. The system can also activate this signal under program control. This signal is driven with a bus driver.
-CMD	**Command**: This signal is used to define when data is valid on the data bus. The trailing edge of this signal indicates the end of the bus cycle. This signal indicates to the slave how long data is valid on the bus. During Write operations, the data is valid on the bus as long as this signal is active. During Read operations, the data is valid on the bus between the leading and trailing edges of this signal and must be held on the bus until after it goes inactive. This signal can be used by the slaves to latch the address on the bus. Latched status lines gated by this signal provide the timing control of valid data. Slaves should use transparent latches to latch address and status information with the leading edge of this signal. This signal is not active during Matched-Memory cycles. It must be driven with a tristate driver.
-DS 32 RTN	**Data Size 32 Return**: This output signal is a negative OR of the Card Data Size 32 signal from each channel connector. If any device drives its Card Data Size 32 signal active, then this output is active. This signal is provided to allow controlling masters to monitor data size information. This signal must be driven with a bus driver.
D0-D15	**Data Bits 0-15**: These signals provide data bus Bits 0-7 (low byte) and 8-15 (high byte) for the controlling master and slaves. D0 is the LSB and D15 the MSB. All 8-bit slaves on the channel must use D0-D7 to communicate with the controlling master. During Read cycles, data is valid on these signals after the leading edge but before the trailing edge of the Command signal, and must remain valid until after the trailing edge of the Command signal. However, during Write cycles, data is valid as long as the Command signal is active. These signals must be driven with tristate drivers.
D16-D31	**Data Bits 16-31**: These signals are used with the Data Bits 0-15 signals to provide data bus bits to the controlling master and slaves. D0 is the LSB and D31 the MSB. All 32-bit transfers from the controlling master to 8-bit slaves are converted to four 8-bit transfers, and all are transmitted on the Data Bits 0-7 signals. All 32-bit transfers from the controlling master to 16-bit slaves are converted to two 16-bit transfers, and all are transmitted on the Data Bits 0-15 signals. During Read cycles, data is valid on these signals after the leading edge of the Command signal but before the trailing edge of the Command signal. However, during Write cycles, data is valid as long as the Command signal is active. These signals must be driven with tristate drivers.
-DS 16 RTN	**Data Size 16 Return**: This output signal is a negative OR of the Card Data Size 16 signal from each channel connector. If any device drives its Card Data Size 16 signal active, this output is active. This signal is provided to allow the controlling master to monitor the data size information. This signal must be driven with a bus driver.

Table 3-3. P1 Signal Descriptions (Continued)

SIGNAL	DEFINITION
-IRQ 9-12, & -IRQ 14-15	**Interrupt Request**: These signals are used to signal that a device requires attention. The interrupt priority sequence is Interrupt Request 9-12, 14, 15, 3-7. An interrupt request is generated when a slave drives one of the interrupt request signals low. The polarity of the interrupt request signals makes it possible for multiple slave to share the same interrupt level. This is called interrupt sharing. These signals must be driven with an open-collector driver.
MADE 24	**Memory Address Enable 24**: This signal indicates when an extended address is used on the bus. If a Memory cycle is in progress and this signal is inactive, an extended address greater than 16 MBytes is being presented; if this signal is active, an unextended address less than or equal to 16 MBytes is being presented. This signal is driven by the controlling master and is decoded by all memory slaves, regardless of their address space size. It is driven with a tristate driver.
M/-IO	**Memory/-Input Output**: This signal distinguishes a Memory cycle from an I/O cycle. When this signal is high, a Memory cycle is in progress. When M/-IO is low, an I/O cycle is in progress. This signal is driven with a tristate driver.
-PREEMPT	**Preempt**: This signal is used by arbitrating bus participants (local arbiters) to request use of the channel through arbitration. Any local arbiter with a channel request activates this signal and causes an Arbitration cycle to occur. A local arbiter removes its preempt signal upon being granted the channel. This bidirectional signal must be driven with an open-collector driver.
-S0,-S1	**Status Bits 0 and 1**: These signals indicate the start of a Channel cycle and also define the type of Channel cycle. When used with the Memory/-Input Output signal, memory Read/Write operations are distinguished from I/O Read/Write operations. These signals are latched by the slave, as required, using the leading edge of the Command signal or the trailing edge of the Address Decode Latch signal. These signals are driven with a tristate driver. Data is moved to or from the bus based on the Command signal and a latched decode of the address, the status lines (the Status Bit 0 signal exclusive or the Status Bit 1 signal), and the Memory/-Input Output signal. Slaves must support a full decode of the Status Bit 0 signal and the Status Bit 1 signal. The following table shows the proper states of the Memory/-Input Output signal, the Status Bit 0 signal , and the Status Bit 1 signal in decoding I/O and memory Read/Write commands.

I/O and Memory Transfer Controls

M/-IO	S0	-S1	Function
0	0	0	Reserved
0	0	1	I/O Write Command
0	1	0	I/O Read Command
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Memory Write Command
1	1	0	Memory Read Command
1	1	1	Reserved

Table 3-3. P1 Signal Descriptions (Continued)

SIGNAL	DEFINITION
	An I/O Write command instructs an I/O slave to store the data on the data bus. The data must be valid on the bus from the leading edge of the Command signal and must be held on the bus until after the Command signal goes inactive. Addresses on the bus must be valid before the Status Bit 0 signal goes active. An I/O Read command instructs an I/O slave to drive its data on to the data bus. The data must be placed on the bus following the leading edge of the Command signal, must be valid before the trailing edge of the Command signal, and must be held on the bus until the Command signal goes inactive. Addresses on the bus must be valid before the Status Bit 1 signal goes active. A memory Write command instructs the memory to read the data on the data bus. The data must be valid on the bus from the leading edge of the Command signal and must be held on the bus until after the Command signal goes inactive. Addresses on the bus must be valid before the Status Bit 0 signal goes active. A memory Read command instructs the memory to drive its data onto the data bus. The data must be placed on the bus following the leading edge of the Command signal. The data must be valid before the trailing edge of the Command signal, and must be held on the bus until the Command signal goes inactive. Addresses on the bus must be valid before the Status Bit 1 signal goes active.
-SBHE	**System Byte High Enable**: This signal indicates and enables transfer of data on the high byte of the data bus (D8-D15), and is used with the Address Bit 0 signal to distinguish between high-byte transfers (D8- D15) and low-byte transfers (D0- D7). All 16-bit slaves decode this line, but 8-bit slaves do not. This signal is driven with a tristate driver.
-TC	**Terminal Count**: This signal provides a pulse during a Read or Write command to indicate that the terminal count of the current DMA channel has been reached. This indicates to the DMA slave the last cycle to be performed of a preprogrammed DMA block transfer. This signal is available on the channel only during DMA operations. It is driven with a tristate driver by the DMA controller.
Tr 32	**Translate 32**: This signal is driven inactive by 32-bit controlling masters and received by the Central Translator Logic. This signal can also be received by any 32-bit slave. When this signal is inactive, a 32-bit controlling master drives the Byte Enable 0-3 signals. When this signal is active, the Central Translator Logic drives the Byte Enable 0-3 signals. It must be driven by a tristate driver.

SCSI Electrical/Physical

The BT-646 interfaces the Micro Channel bus to a SCSI general purpose 8-bit bidirectional bus. The SCSI port is controlled by a SCSI interface chip which supports arbitration, selection, and reselection with a minimum need for processor attention. The SCSI interface controller supports target mode and synchronous SCSI transfers. The BT-646S includes single-ended drivers and receivers (built into the SCSI interface chip) which allow a maximum cable length of six meters. The BT-646D includes differential drivers and receivers which allow a maximum cable length of 25 meters.

A minimum conductor size of 28 AWG should be employed to minimize noise effects and ensure proper distribution of terminator power.

J1 is a 50-pin, non-shielded SCSI device connector consisting of two rows of 25 male pins with adjacent pins 2.54 mm (0.1 in) apart. J2 is a 50-contact, shielded SCSI device connector.

For the BT-646S to support a 10 MBytes/sec synchronous and a 7 MBytes/sec asynchronous SCSI data rate in single-ended mode, proper termination and cabling are important. The BT-646S uses regulated termination with 100 ohm resistors. It is recommended that regulated termination be used at both ends of the SCSI cable.

For the BT-646D, all signals are terminated with 330 ohms from the differ-ential nodes to +5 volts and ground, respectively, and with 150 ohms between each differential pair.

Single-Ended Output Characteristics. Each signal driven has the following output characteristics when measured at the connector:

Signal assertion	= 0.0 volts dc to 0.4 volts
Minimum driver output capability	= 48 milliamps (sinking) at 0.5 volts dc (7438 or equivalent)
Signal negation	= 2.0 volts dc to 5.25 volts dc.

Devices receiving the BT-646S's output should be of the SCHMITT trigger type to improve noise immunity, 74LS14, 74LS240, or the equivalent. The device should not load the bus with more than two standard low-power Shottky (LS) input loads per line, and should terminate the controller output signals with 100 ohm terminators if the BT-646S is used.

Single-Ended Input Characteristics. Each signal received by the controller should have the following input characteristics when measured at the SCSI device's connector:

Signal true	= 0.0 volts dc to 0.8 volts dc
Maximum total input load	= -0.4 milliamps at 0.4 volts dc
Signal false	= 2.0 volts dc to 5.25 volts dc
Minimum input hysteresis	= 0.2 volts dc.

Differential Output Characteristics. Each signal driven should have the following output characteristics when measured at the connector:

Signal true	= when +SIGNAL is more positive than -SIGNAL
Minimum low-level output current	= 55 milliamps at 1.7 volts dc maximum
Minimum high-level output current	= -55 milliamps at 2.7 volts dc minimum

Differential Input Characteristics. Each signal received by the controller should have the following input characteristics when measured at the SCSI device's connector:

Signal true	= when +SIGNAL is more positive	than -SIGNAL
Maximum input load	= ±2.0 milliamps	
Maximum input capacitance	= 25 pF	
Minimum input hysteresis	= 35 millivolts.	

Terminator Power (Pin 26). Usually only SCSI initiators should provide termination power.

VTerm. = 4.25 volts dc to 5.25 volts dc
1.0 amp minimum source drive capability
1.0 milliamp maximum sink capability.

Refer to Figure 3-2 for a schematic representation of how terminator power is provided on the BT-646.

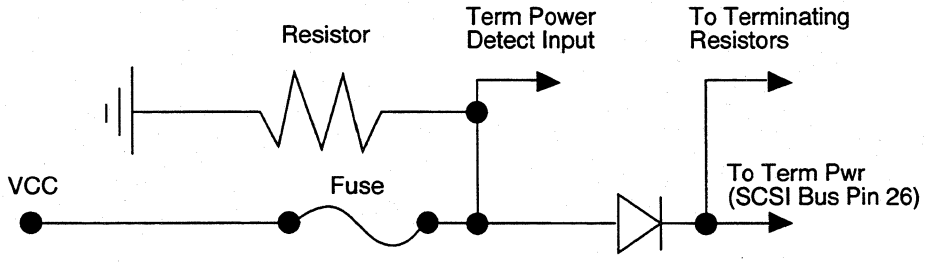


Figure 3-2. Terminator Power Schematic

Terminators. SCSI devices are daisy chained together using a common cable. All signals are common between all SCSI devices, and both ends of the cable are terminated with small hardware components called terminators. Terminators, which are connected to SCSI devices or SCSI cables, make data transfer on a SCSI network more reliable.

Devices connected to SCSI chains must have the correct number of terminators for proper operation and to prevent damage to the SCSI chip on the BT-646. There can be no more than two terminators in a chain of SCSI devices—each at one physical end of the chain. Therefore, if more than two SCSI devices are connected in a SCSI daisy chain, the middle devices in the control cable must have their terminator resistor packs removed. See Section 2, the "Unpacking and Installation" section, of this manual for additional details on installation.

SCSI Signal Interface

The BT-646 single-ended SCSI interface signals for J1 and J2 are shown in Table 3-4. Table 3-5 lists the BT-646 differential SCSI interface signals for J1 and J2. A plus sign (+) denotes an active high signal. A hyphen (–) denotes an active low signal.

The pin descriptions for J4, a 4-pin disk drive power connector are shown in Table 3-6.

Table 3-4. J1 & J2 Single-Ended SCSI Interface Signal Pin Assignments

Signal Pin	Signal Name	Signal Pin	Signal Name	Direction (Initiator)
1	Ground	2	–DB0	I/O
3	Ground	4	–DB1	I/O
5	Ground	6	–DB2	I/O
7	Ground	8	–DB3	I/O
9	Ground	10	–DB4	I/O
11	Ground	12	–DB5	I/O
13	Ground	14	–DB6	I/O
15	Ground	16	–DB7	I/O
17	Ground	18	–DBP	
19	Ground	20	Ground	
21	Ground	22	Ground	
23	Reserved	24	Reserved	
25	Open	26	TERMPWR	
27	Reserved	28	Reserved	
29	Ground	30	Ground	
31	Ground	32	–ATN	Output
33	Ground	34	Ground	
35	Ground	36	–BSY	
37	Ground	38	–ACK	Output
39	Ground	40	–RST	Output
41	Ground	42	–MSG	Input
43	Ground	44	–SEL	Input
45	Ground	46	–C/D	Input
47	Ground	48	–REQ	Input
49	Ground	50	–I/O	Input

Table 3-5. J1 & J2 Differential SCSI Interface Signal Pin Assignments

Signal Pin	Signal Name	Signal Pin	Signal Name	Direction (Initiator)
1	Ground	2	Ground	
3	+DB0	4	–DB0	I/O
5	+DB1	6	–DB1	I/O
7	+DB2	8	–DB2	I/O
9	+DB3	10	–DB3	I/O
11	+DB4	12	–DB4	I/O
13	+DB5	14	–DB5	I/O
15	+DB6	16	–DB6	I/O
17	+DB7	18	–DB7	I/O
19	+DBP	20	–DBP	
21	+DIFFSENS	22	Ground	
23	Reserved	24	Reserved	
25	TERMPWR	26	TERMPWR	
27	Reserved	28	Reserved	
29	+ATN	30	–ATN	Output
31	Ground	32	Ground	
33	+BSY	34	–BSY	
35	+ACK	36	–ACK	Output
37	+RST	38	–RST	Output
39	+MSG	40	–MSG	Output
41	+SEL	42	–SEL	Input
43	+C/D	44	–C/D	I/O
45	+REQ	46	–REQ	Input
47	+I/O	48	–I/O	Input
49	Ground	50	Ground	

As Table 3-6 indicates, J4 is a 4-pin disk drive connector. Pins 2 and 3 are connected to ground. This connector provides standard +12V and +5V power to disk drives.

Table 3-6. J4 Disk Drive Power Connector Pin Descriptions

Pin #	Signal Name	Description
1	+12V	+12V power
2	GND	Ground
3	GND	Ground
4	+5V	+5V power

SCSI Signal Definitions

The definitions for SCSI interface signals are shown in Table 3-7.

Table 3-7. J1 & J2 SCSI Interface Signal Descriptions

Differential Signal	Single-Ended Signal	Definition
-RST **+RST**	**-RST**	**Reset**: This "OR Tied" signal, which is asserted by the initiator, causes the SCSI bus to cease all operations and return to the Idle condition. This signal is normally used during a power-up sequence. A reset during a Write operation would cause incorrect data to be written on the disk.
-SEL **+SEL**	**-SEL**	**Select**: When this signal is asserted by the initiator, along with an initiator ID and target ID data bit (0 -7), it causes the addressed target to be selected. This signal must be deasserted by the initiator after the target asserts the Busy (-BSY) signal in response to a proper selection.
-BSY **+BSY**	**-BSY**	**Busy**: When this "OR Tied" signal is asserted, it indicates that the bus is being used.
-C/D **+C/D**	**-C/D**	**Control/Data**: When this signal is asserted by the target, it indicates that control information is to be transferred on the data bus. Deassertion of this signal indicates that data information is to be transferred on the data bus.
-I/O **+I/O**	**-I/O**	**Input/Output**: When this signal is asserted by the target, it indicates that information will be transferred to the initiator from the target. Deassertion indicates that information will be transferred to the target from the initiator. This signal is also used to distinguish between the Selection and Reselection phases.
-REQ **+REQ**	**-REQ**	**Request**: When this signal is asserted by the target, it indicates that an 8-bit byte is to be transferred on the data bus. The Request (REQ) signal is deasserted following the assertion of the Acknowledge (ACK) signal from the host. The Request (REQ) and Acknowledge (ACK) signals control the handshaking.
-ACK **+ACK**	**-ACK**	**Acknowledge**: When this signal is asserted by the initiator, it indicates data has been accepted by the initiator or that data is ready to be transferred from the initiator to the target.
-ATN **+ATN**	**-ATN**	**Attention**: This signal is driven by the initiator to indicate the Attention condition.
-MSG **+MSG**	**-MSG**	**Message**: When this signal is asserted by the target, it indicates the Message phase. The state of the Input/Output (-I/O) signal when it is asserted indicates MESSAGE IN or MESSAGE OUT.
-DB0-7 & -DBP **+DB0-7 & +DBP**	**-DB0-7 & -DBP**	**Data Bits & Parity**: These eight bidirectional data lines and one odd parity signal are used to transfer 8-bit parallel data over the SCSI bus. Bit 7 is the MSB and has highest priority during the Arbitration phase. Parity is not valid during the Arbitration phase. The use of the parity bit is an option. See Section 2 of this manual for the switch settings to enable or disable SCSI parity.

4

HARDWARE DESCRIPTION

This section describes the functional hardware operation of the BT-646. This description encompasses the hardware control registers that are mapped into the Micro Channel system's I/O address space. The issuance of commands, the coordination of data flow, and the basic management of the BT-646's hardware components are discussed. A complete understanding of the hardware control registers and their operation will enable the system software programmer to (1) fully understand the software interface description in Section 5, the "Software Interface" section of this manual, and (2) develop a fully functional software driver for single or multitasking operating systems.

HOST DMA DATA TRANSFER CONTROL

All host data transfers are performed by the BT-646 as a Micro Channel 16-bit or 32-bit bus master. This is the most efficient method to transfer data between the SCSI devices and the system memory. The BT-646 senses the speed of the Micro Channel system and adjusts its data transfer rate accordingly.

HARDWARE CONTROL REGISTERS

The BT-646's I/O interface consists of three hardware control registers that are used by the host to issue start commands to the BT-646, to gain status information about the BT-646's operation, and to manage interrupts generated by the BT-646. These registers are located in the Micro Channel I/O address space at three consecutive addresses. The beginning or base address is determined by the I/O base address switch settings described in Section 2. Table 4-1 provides a summary of these registers. Each of these registers is 8-bits wide and performs the functions described as follows.

Table 4-1. BT-646's Hardware Control Registers

ADDRESS	TYPE	DESCRIPTION
I/O Base Address + 0	W	Control Register
I/O Base Address + 0	R	Status Register
I/O Base Address + 1	W	Command/Parameter Register
I/O Base Address + 1	R	Data In Register
I/O Base Address + 2	R	Interrupt Register

Control Register (Write Only) I/O Base Address + 0

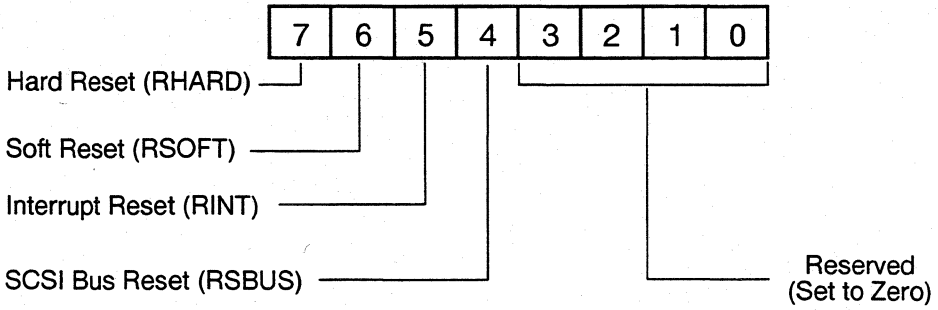


Figure 4-1. Control Register (Write)

The host system's CPU uses this register to specify programmable options within the BT-646 (e.g., soft reset, hard reset, SCSI bus reset). For example, the host system's CPU can stop all BT-646 activity immediately by setting this register's Bit 6, the Soft Reset bit (RSOFT). This is a write-only register.

Bits 0-3–These bits are reserved and must be set to zero.

Bit 4 Reset SCSI Bus (RSBUS)–When this bit is set to a one, the Reset signal on the SCSI bus is maintained true for at least 25 microseconds. This Reset condition immediately clears all SCSI devices from the bus. The assertion of the SCSI Reset condition supersedes all other activity on the SCSI bus. See the heading "Reset Operations" later in this section for additional details on the Reset operation.

Bit 5 Reset Interrupt (RINT)–The Micro Channel system's CPU sets this bit to acknowledge a BT-646 interrupt. When this bit is set to one by the Micro Channel CPU, the BT-646's hardware-generated interrupt is reset and the Interrupt Register is cleared. Note that all bits in the Interrupt Register are cleared by the setting this bit.

Bit 6 Soft Reset (RSOFT)–When this bit is set to one, it causes all BT-646 activity to stop immediately. All mailboxes, command control blocks, and any pending commands are discarded by the BT-646. Previous mailbox pointers must be cleared by host processes. The primary difference between a hard and soft reset is that this bit does not effect a SCSI Bus Reset condition. Once the soft reset activity has been completed by the BT-646, the BT-646 must be reinitialized for any future operation. This state is indicated by the setting of the Host Adapter Ready bit (HARDY) and the Initialization Required bit (INREQ) in the Status Register.

Bit 7 Hard Reset (RHARD)–The setting of this bit causes the BT-646 to enter an initial condition power-on state. Any command in process is stopped and pending commands are abandoned. The BT-646 will execute its internal diagnostic function and report any errors. During reset, the Diagnostic Active bit (DACT) is set. Once the hard reset activity has been completed by the BT-646, the BT-646 must be reinitialized for any future operation. This state is indicated by the setting of the Host Adapter Ready bit (HARDY) and the Initialization Required bit (INREQ) in the Status Register.

Specific operation bits in the Control Register are automatically reset by the BT-646 when the specific operation is completed. The host-controlling software is not required to reset the operational control bit for a specific function.

Status Register (Read Only) I/O Base Address + 0

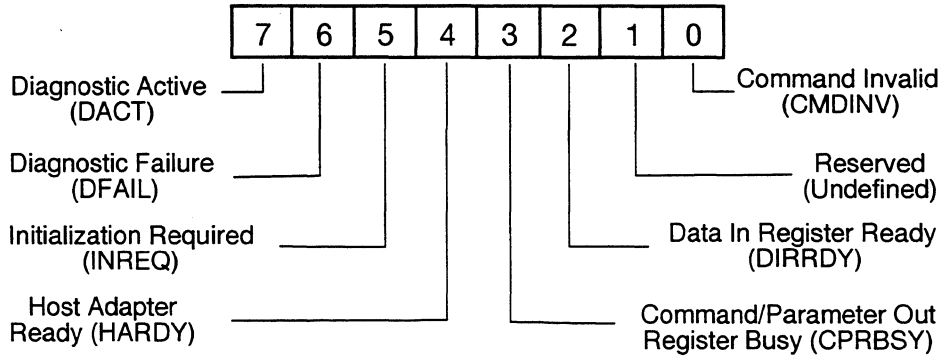


Figure 4-2. Status Register (Read)

The BT-646 uses this register to report the status of its condition to the Micro Channel system's CPU. For example, the BT-646 sets this register's Data In Register Ready bit (DIRRDY) when it has written data to its Data In Register. By setting this bit, the BT-646 notifies the host system's CPU that there is fresh data in the Data In Register that should be read. As soon as the host system's CPU reads the Data In Register, the BT-646 immediately resets the Data In Register Ready bit (DIRRDY). The BT-646 resets this bit to zero to ensure that the host system's CPU does not reread the same data in the Data In Register. When the BT-646 writes fresh data to its Data In Register, it will then set the Data In Register Ready bit (DIRRDY) to one again.

The host system's CPU can also read this register to check for error conditions. For example, the BT-646 sets this register's Command Invalid bit (CMDINV) when it detects an invalid command or parameter byte in its Command/Parameter Register. Consequently, the host system's CPU can check the Command Invalid bit (CMDINV) to see if such an error condition currently exists. This is a read-only register.

Bit 0 Command Invalid (CMDINV)–The BT-646 sets this bit immediately upon detection of an invalid command or parameter byte in the Command/Parameter Register. When the host is sending a single or multibyte command, the BT-646 terminates the data transfer sequence by setting the Command Complete bit (CMDC) in the Interrupt Register and by generating a hardware interrupt. The BT-646 terminates all commands (valid or invalid) by this method. Invalid commands are indicated by the setting of this bit. The condition of this bit is only meaningful while the Command Complete bit (CMDC) is true.

Bit 1–This bit is reserved and is set to zero.

Bit 2 Data In Register Ready (DIRRDY)–This status bit is used to synchronize the transfer of status information from the BT-646 to the host system. The BT-646 sets this bit to one when it has placed a byte of data in the Data In Register. This condition notifies the host that it may read and process the data. When the host reads the data byte in the Data In Register, this bit is reset to zero by the BT-646. This sequence is repeated for multi-byte data transfers.

Bit 3 Command/Parameter Register Busy (CPRBSY)–This status bit is used to synchronize the transfer of command and associated parameter bytes from the Micro Channel system host to the BT-646. When this bit is reset to zero the host may place a command or parameter byte in the Command/Parameter Register. When the host writes a byte to the Command/Parameter Register, the BT-646 will set this bit to a one indicating a Busy condition. The BT-646 will reset this bit when it has read and processed the command/parameter byte. This sequence is repeated for multibyte data transfers.

Bit 4 Host Adapter Ready (HARDY)–This bit indicates the ready or not ready internal command state of the BT-646. When this bit is set, the BT-646 is ready for a new host adapter command. In general the Micro Channel host system's processor may only issue host adapter commands while this bit is set.

***Exception**: The multitasking design of the BT-646's firmware permits the following commands to be issued regardless of the busy or not-busy state of the BT-646.*

- Start SCSI (02) command
- Enable Outgoing Mailbox Ready Interrupt (05) command.

See Section 5, the "Software Interface" section, for details on these commands.

Bit 5 Initialization Required (INREQ)–When this bit is set to one, it indicates that the mailbox structures must be initialized. This bit is typically set immediately after the completion of self-diagnostic tests following a reset. This bit is not set if diagnostics fail (the Diagnostic Failure bit (DFAIL) is set). The Micro Channel host system must now issue an Initialize Mailbox command (01) to inform the BT-646 of the base memory address of the mailbox structure area. The BT-646 will reset this bit after successful completion of the Initialize Mailbox command.

Bit 6 Diagnostic Failure (DFAIL)–When this bit is set, it indicates that the BT-646's internal self diagnostic has detected an error. This bit may be reset only by a hard reset initiated either by hardware or by the host software (See Section 5, the "Software Interface" section.). Self-test errors are reported by flashing the on-board LED. See Appendix A for details.

Bit 7 Diagnostic Active (DACT)–This bit is set when the BT-646 begins its self-testing activity immediately after a power-on reset or a programmed hard reset (Control Register, Bit 7 is set). This bit is reset upon the successful completion of the self-test activity. If the diagnostics fail, this bit may not be reset indicating that the self-test programs could not be completed. In the case of most failures, the Diagnostic Failure bit (DFAIL) will also be set. See Appendix A for additional details on diagnostic procedures.

Command/Parameter Register (Write Only) I/O Base Address + 1

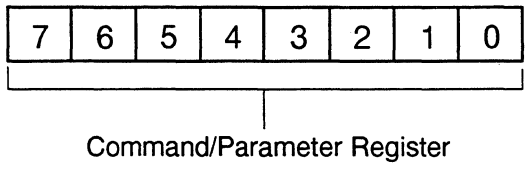


Figure 4-3. Command/Parameter Register (Write)

The Command/Parameter Register serves as the input port through which the Micro Channel host system software may issue commands and associated parameter bytes to the BT-646. The commands issued to the BT-646 by this method provide initialization and establish control specifications for subsequent operations. SCSI-bus related commands are issued through a mailbox command structure (See Section 5, the "Software Interface" section.). The host is responsible for issuing the correct number of command and parameter bytes for each operation. Otherwise, incorrect operation may occur along with the cessation of command acceptance by the BT-646. This condition is indicated by the setting of the Command Invalid bit (CMDINV) in the Status Register.

The coordination of command and parameter data byte transfers between the BT-646 and the Micro Channel host system is governed by the Host Adapter Ready bit (HARDY), the Command/Parameter Register Busy bit (CPRBSY), and the Data In Register Ready bit (DIRRDY). All host adapter commands, with the exception of Enable OMBR Interrupt (05) and Start SCSI (02), require the Host Adapter Ready bit (HARDY) to be set. Parameter data bytes are written to the Command/Parameter Register. The host must first test the Command/Parameter Register Busy bit (CPRBSY) for a not set condition to determine if the BT-646 is ready to accept a command parameter data byte. When the host writes a command or parameter byte to the Command/Parameter Register, the BT-646 sets the Command/Parameter Register Busy bit (CPRBSY) to a one. When the local MPU has read the byte, the BT-646 will reset the Command/Parameter Register Busy bit (CPRBSY) to indicate that the host can write another byte.

When all the bytes for a particular command have been transferred, the BT-646 will set the Command Complete bit (CMDC) in the Interrupt Register. If an error is detected in the command, the Command Invalid bit (CMDINV) will be set in the Status Register.

Data In Register (Read Only) I/O Base Address + 1

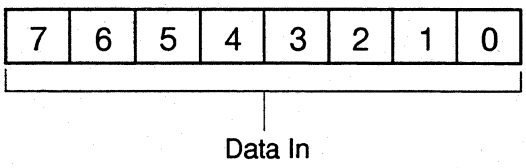


Figure 4-4. Data In Register (Read)

The BT-646 uses this register to return information bytes to the host system. For commands that return information bytes to the host, the Data In Register Ready bit (DIRRDY) is used to synchronize data byte transfers. The BT-646 sets the Data In Register Ready bit (DIRRDY) to a one when a data byte is available to be read by the host system. The Data In Register Ready bit (DIRRDY) is automatically reset to zero by the BT-646 when the host system reads the data byte from the BT-646's Data In Register.

For multiple data byte transfers, the host should wait for the Data In Register Ready bit (DIRRDY) to return to the set state before reading additional data. When the last byte of an information block (single or multiple byte) has been transferred, the BT-646 will set the Command Complete bit (CMDC) in the Interrupt Register. This is a read-only register.

Interrupt Register (Read Only) I/O Base Address + 2

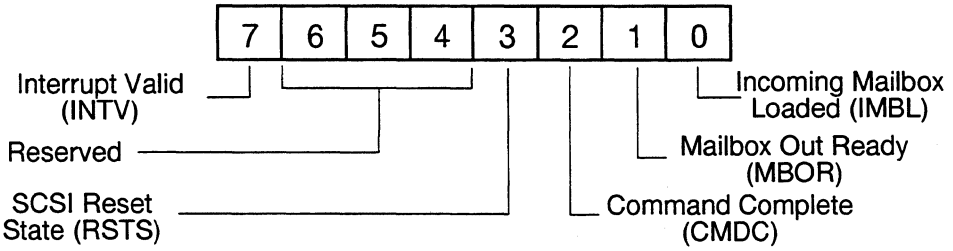


Figure 4-5. Interrupt Register (Read Only)

The BT-646 uses this read-only register to tell the host system the reason why it generated a hardware interrupt signal. The following are the four conditions under which the BT-646 can generate a hardware interrupt to the host system:

1. Incoming Mailbox Loaded interrupt (IMBL): the BT-646 has made an entry in an incoming mailbox.
2. Mailbox Out Ready interrupt (MBOR): an outgoing mailbox location(s) is ready for the host system to use.
3. Command Complete interrupt (CMDC): the BT-646 has completed a command.
4. SCSI Reset State interrupt (RSTS): the BT-646 has detected a SCSI Bus Reset condition.

When the BT-646 generates a hardware interrupt signal for one of the preceding four reasons, the BT-646 sets bits in this register to provide the host system with more information about the interrupt. The BT-646 completes the following actions:

1. It sets Bit 7, the Interrupt Valid bit (INTV), to indicate that the interrupt is valid.
2. It also sets one of the other unreserved bits to indicate why it generated a hardware interrupt signal to the host system. These bits (Bits 0-3) are collectively referred to as interrupt cause bits. This group of bits include the Incoming Mailbox Loaded bit (IMBL), the Mailbox Out Ready bit (MBOR), the Command Complete bit (CMDC), and the SCSI Reset State bit (RSTS).

In response to this interrupt request by the BT-646, the host system should execute the following sequence to service the interrupt:

1. Read the Interrupt Register. The host should maintain this value internally for further interrupt processing.
2. Clear the Interrupt Register. This is accomplished by setting the BT-646's Control Register's Reset Interrupt bit (RINT).
3. Determine the interrupt cause (from the saved Interrupt Register value in the preceding Step 1) and then execute the appropriate interrupt service routine.

Note: A hard reset, a soft reset, or initial board power-on condition will cause the Interrupt Register to be cleared, i.e., no interrupts pending.

The BT-646 sets the priority of certain interrupt conditions. This topic will be discussed before describing the individual bits of the Interrupt Register. Refer to the following heading "Interrupt Timing and Synchronization".

Interrupt Timing and Synchronization. The BT-646 sets the priority of certain interrupt conditions. The posting of a mailbox-related interrupt is withheld if a SCSI Reset State interrupt (RSTS) or a Command Complete interrupt (CMDC) is pending service from the host. Once the SCSI Reset State interrupt (RSTS) or the Command Complete interrupt (CMDC) is cleared, the BT-646 will post the mailbox interrupt(s). Likewise, a SCSI Reset State interrupt (RSTS) or a Command Complete interrupt (CMDC) will only be presented if the Interrupt Register has been cleared, and the Data In Ready bit (DIRRDY) shows no additional data is pending.

Because all outbound host mailboxes are typically controlled by host-resident software, it is not necessary to enable the Outgoing Mailbox Ready interrupt (OMBR) unless all mailboxes are being utilized. This technique also lessens the possibility of missed interrupt notification for an Incoming Mailbox Loaded (IMBL) condition. If all outgoing mailboxes are in use, then the host could enable the Outgoing Mailboxes Ready interrupt (OMBR) to gain notification of a Mailbox Ready condition. See the Enable Outgoing Mailbox Ready command description in Section 5, the "Software Interface" section, for instructions on how to enable the Outgoing Mailboxes interrupts (OMBR).

Bit 0 Incoming Mailbox Loaded (IMBL)–When this bit is set, it indicates that the BT-646 has made an entry in an incoming mailbox location. This bit is qualified by the Interrupt Valid bit (INTV) also being set and by the generation of a Micro Channel bus interrupt signal. The host should service this interrupt as soon as possible to allow additional BT-646 interrupts to be posted. The multitasking firmware of the BT-646 continues to process outstanding SCSI commands after the posting of an Incoming Mailbox Loaded interrupt (IMBL). If additional outstanding commands are completed before the servicing of a previous Incoming Mailbox Loaded interrupt (IMBL), the status of completed commands will be placed in an available incoming mailbox location. The host should therefore scan all mailboxes to determine if additional data has been provided. The BT-646 will use Incoming Mailbox locations in a round-robin order permitting the host to scan in the same manner. When a vacant mailbox is found the host may discontinue its scan.

Bit 1 Outgoing Mailbox Ready (OMBR)–When this bit is set to a one, it indicates that one or more of the outgoing mailbox locations is available for use by the host. This bit is qualified by the Interrupt Valid bit (INTV) also being set and by the generation of a Micro Channel bus interrupt signal. The Outgoing Mailboxes Ready interrupt (OMBR) is generated only when Outgoing Mailbox interrupts (OMBR) have been enabled and an outgoing mailbox entry is cleared by the BT-646. An Outgoing Mailbox Ready interrupt (OMBR) is suppressed if a SCSI Reset State (RSTS) or a Command Complete (CMDC) interrupt is pending service. When these previous interrupts are cleared by the host, the pending Outgoing Mailboxes Ready interrupt (OMBR) will be issued by the BT-646.

Application Note: *It is recommended that the Outgoing Mailbox Ready interrupt (OMBR) not be enabled unless all outgoing mailbox locations are in use. For most applications, the BT-646 will process command requests faster than a host will issue them. If the situation does occur where all outgoing mailbox locations are busy, the host may issue the Enable Outgoing Mailbox Ready Interrupt command without waiting for the status of the Host Adapter Ready bit (HARDY).*

Bit 2 Command Complete (CMDC)–This bit is set to a one when the Command/Parameter Register is ready to accept a command. Any previous command will have been completed, either normally or abnormally. If a previous command completed with an error condition or was aborted for any reason, this bit will still be set along with the Command Invalid bit (CMDINV) in the Status Register. Normally completed commands are indicated by the setting of this bit without any accompanying error condition status bits. This bit is qualified by the Interrupt Valid bit (INTV) also being set and by the generation of a Micro Channel bus interrupt signal. A Command Complete interrupt (CMDC) is suppressed if an Interrupt Valid bit (INTV) is set (indicating an interrupt is pending service) or if the Data In Register Ready bit (DIRRDY) is set. When these previous interrupts are cleared by the host, the temporarily withheld Command Complete interrupt (CMDC) will be issued by the BT-646.

Bit 3 SCSI Reset State (RSTS)–When this bit is set, it indicates that a SCSI Bus Reset condition has been detected by the BT-646. This bit is qualified by the Interrupt Valid bit (INTV) also being set and by the generation of a Micro Channel bus hardware interrupt signal. In cooperation with Micro Channel host system driver software, the BT-646 can implement the SCSI specification soft reset option. BT-646 queued operations will resume once the SCSI bus has returned to the operational state. If a currently running command was aborted due to the SCSI Bus Reset condition, the BT-646 may have to restart the command.

The host may convert the SCSI bus soft reset to a SCSI bus hard reset by setting the Soft Reset bit (RSOFT) in the BT-646's Control Register. In this case, all queued commands are abandoned and the BT-646 must be reinitialized. See the heading "Reset Operations" later in this section for details on the reset conditions.

Bit 4 Reserved–Value read is zero.

Bit 5 Reserved–Value read is zero.

Bit 6 Reserved–Value read is zero.

Bit 7 Interrupt Valid (INTV)–When this bit is set, it indicates that a valid interrupt has been generated by the BT-646. This bit reflects the state of the BT-646 generated interrupt signal on the Micro Channel bus. The specific reason for the interrupt condition is determined by Bits 0-3 of this register.

RESET OPERATIONS

Reset conditions associated with the operation of the BT-646 are initiated from two different vantage points: the Micro Channel bus and the SCSI bus. A description of each follows.

Micro Channel Host Initiated Reset Operation

The BT-646 may be reset to an initial power-on condition through two different operations, one hardware and the other software.

Hardware Reset–The BT-646 is fully reset and initialized to a power-on initial condition when the Reset signal is true on the Micro Channel system bus. The Reset signal is asserted to a true condition by the host during power on or host detected low-power conditions. The Reset signal is applied universally to all installed host adapters in the Micro Channel system I/O channel bus.

Software Reset–The BT-646 may be fully reset to an initial state by a software command, just the same as if a hardware reset had been received. The setting of the Hard Reset bit (RHARD) will cause a Reset condition to occur immediately. This Reset condition will affect the BT-646 only, not other host adapters installed in the Micro Channel system I/O channel.

Either type of Micro Channel host initiated reset will cause the following conditions on the BT-646.

- A SCSI Bus Reset condition will be placed on the SCSI bus by the BT-646. This will reset all peripheral devices, whether a target or initiator.
- The control registers of all intelligent logic modules on the BT-646 will be initialized to a known state.
- All pending operations are aborted and all data structures are initialized to a no operation pending state.
- The BT-646 executes all internal diagnostic functions. While the diagnostic functions are in process, the BT-646 will indicate this condition by setting the Diagnostic Active bit (DACT) to true in the Status Register.

After completion of a hard reset, the BT-646 indicates that it is now in an initial condition by asserting the Initialization Required bit (INREQ) in the BT-646's Status Register. This condition requires that all mailbox, command control blocks, and BT-646 operation parameters be established before operations may begin.

SCSI Bus Reset Operations

The SCSI Bus Reset condition is used to clear all SCSI devices immediately from the SCSI bus. When the SCSI bus Reset signal is asserted, the SCSI Bus Reset condition takes precedence over all other bus phases. A SCSI Bus Reset condition may be forced by any device on the bus, whether a target or initiator. Whenever a SCSI Reset condition occurs, a Bus Free phase always follows the Reset condition.

The four ways in which a SCSI bus reset may be either asserted or sensed by the BT-646 are as follows:

R1 The SCSI Bus Reset condition is always asserted when the BT-646 is reset by the Micro Channel host system. This is described earlier in this section under the heading "Micro Channel Host Initiated Reset Operation".

R2 If the Reset SCSI Bus bit (RSBUS) is set by the Micro Channel host system control software the BT-646 will assert the SCSI bus Reset signal on the SCSI bus. Because the host initiated this condition the SCSI Reset State bit (RSTS) in the Interrupt Register is not set.

R3 The BT-646 may initiate a SCSI Bus Reset condition in reaction to a detected bus phase error. The BT-646 constantly monitors the SCSI bus for invalid conditions. If an invalid phase is detected, the BT-646 will perform a normal SCSI Bus Reset operation which includes the assertion of the SCSI bus Reset signal. The Micro Channel host system will be notified of this condition by the generation of a Micro Channel system hardware interrupt and the setting of both the SCSI Reset State bit (RSTS) and the Interrupt Valid bit (INTV) in the BT-646's Interrupt Register.

R4 The BT-646 will detect and respond to a SCSI Bus Reset condition that is asserted by another device on the bus. Other SCSI devices may normally assert the Reset signal during either initialization or certain error recovery states. The BT-646 will notify the Micro Channel host system of the SCSI Bus Reset condition by the generation of a Micro Channel hardware interrupt and by setting both the SCSI Reset State bit (RSTS) and the Interrupt Valid bit (INTV) in the BT-646's Interrupt Register.

The SCSI specification defines two methods by which the SCSI bus may be reset, either by the hard reset option or the soft reset option. The effect of the SCSI Bus Reset condition on uncompleted commands, SCSI device reservations, and SCSI device operating modes is determined by which method is implemented. SCSI devices must implement one of the reset options.

SCSI Bus Soft Reset Option

The BT-646 implements the soft reset option. This allows the SCSI bus to be reset, yet not destroy all initialization and configuration data in each SCSI device. The soft reset option allows a single initiator to reset the SCSI bus without disturbing the operation of other initiators in a multiple initiator system. This means that status and pointer information is not destroyed, and that disconnected or outstanding commands may be allowed to resume. The soft reset option is very useful in multiple initiator SCSI bus implementations that are typical in multiprocessor or multitasking systems. For the soft reset option to function properly, all devices on the SCSI bus must implement the option. The soft reset option performs the following:

- Attempts to complete any uncompleted command(s) that were fully identified. (See the SCSI specification for a description of "fully identified".)
- Preserves all SCSI device reservations.
- Preserves any SCSI device operating modes.

SCSI Bus Hard Reset Option

The SCSI bus hard reset option restores ALL SCSI devices, target or initiator, to the initial power-on condition. All system activity is lost, and all devices must be completely reinitialized before normal operations may be restored. SCSI devices that implement the hard reset option perform the following operations:

- Clear all uncompleted commands.
- Release all SCSI device reservations.
- Return any SCSI device operating modes to their default condition.

The BT-646 performs only a soft reset operation. If a hard reset implementation is required, the Micro Channel system may direct the BT-646 to return to a fully reset initial condition, thus implementing the hard SCSI bus reset option. This is accomplished by the following sequence:

1. Upon detection of a SCSI Bus Reset condition, the BT-646 will assert a Micro Channel hardware interrupt and will set the SCSI Reset State bit (RSTS) in its Interrupt Register. Refer to the preceding SCSI RESET description R3 or R4 in the heading "SCSI Bus Reset Operations" in this section.

2. The Micro Channel host system may convert the BT-646 soft reset to a hard reset by executing a host-initiated Reset operation. The Micro Channel host system must set the Reset SCSI Bus bit (RSBUS) within 290 microseconds after the SCSI Reset State bit (RSTS) has been set. This prevents the resumption of activity according to the rules of the soft SCSI reset. All BT-646 CCB's will be abandoned, and the BT-646 will ready itself to accept new initialization commands. No secondary Reset signal is generated on the SCSI bus by the BT-646. Reinitialization of all mailbox and command control blocks are required.

3. A full hard reset is required, with a secondary Reset condition generated by the SCSI bus by the BT-646, the Micro Channel host system may assert the Hard Reset bit (RHARD). This places the BT-646 in an initial power-on condition.

5

SOFTWARE INTERFACE

For the BT-646 to operate properly, the Micro Channel host system must issue the correct command and associated parameters to the BT-646. The BT-646 has its own set of executable instructions that the host system can issue to the BT-646. This command set can be subdivided into the following three groups:

1. Host adapter commands
2. Mailbox commands, and
3. BIOS commands.

The Micro Channel host system uses the host adapter commands to initialize and to establish control specifications for subsequent operations of the BT-646. The host system uses the BT-646's Command/Parameter Register as an input port through which it issues any host adapter commands and associated parameter bytes to the BT-646. For more details on each of these host adapter commands refer to the heading "Host Adapter Commands" later in this section.

The second category of commands, mailbox commands, is issued to the BT-646 when multithreading operations are required. Mailboxes are reserved storage areas which reside at a fixed contiguous memory location in the host system's main memory. The mailboxes coordinate communications between the host system and the BT-646 when the BT-646 is operating in multithreading mode. This software interface enables the BT-646 to execute multiple commands concurrently for multiple targets with minimal intervention from the host system. For more details on these mailbox commands refer to the heading "Mailbox Commands" later in this section.

The third category of commands, BIOS commands, is issued to the BT-646 when single-threaded operations are required. In this case the BIOS commands work with the BT-646's on-board BIOS. These commands in unison with the on-board BIOS function in a manner fully compatible with MS-DOS and the standard Micro Channel system BIOS interface as defined in the host system's technical reference manual. For more details on each of these BIOS commands refer to the heading "BIOS Command Interface" later in this section.

Before these commands are discussed in detail, a brief look at how the BT-646 acts as bus master to transfer data on the memory bus and how it requests interrupt service from the host is presented.

BUS MASTER DIRECT MEMORY ACCESS (DMA)

As briefly described in Section 1, the "Introduction" section, the DMA control logic manages bus arbitration and data transfer coordination. The BT-646 operates as a Micro Channel bus master during data transfers. The BT-646 arbitrates for Micro Channel bus access and once granted, it takes over control of the bus. It generates the Micro Channel bus address and command strobes. The BT-646 supports both odd and even starting addresses, commonly known respectively as aligned and unaligned transfers. If presented with an even transfer count beginning at an odd memory starting address, the BT-646 will first transfer a single byte (data bits D24-D31). The remaining data is then transferred as double words (32 bits) until the last byte which is transferred as a single byte (data bits D0-D7). While odd byte data transfers are fully supported, it is recommended that when possible Micro Channel host buffers be double-word aligned to gain better data transfer performance.

During the Boot phase the BT-640's BIOS automatically initializes the DMA controller to the correct masked condition. This automatic set up enables the BT-646 to begin normal DMA operations without any further program initialization. If other programs alter this initial DMA set up, the original masked condition can be restored by using either the DMA compatibility mode or the DMA extended mode. Each of these modes is described in the following two sections.

DMA Compatibility Mode

The DMA controller can be restored to its initial masked condition if the programmer sets the proper control bits using the DMA compatibility mode. The Mask Register (Set/Clear) can be used to mask the DMA controller if the program has information concerning the single DMA channel. The Write Mask Register can be used to set four of the DMA channels to the correct masked or unmasked condition simultaneously if the program has information concerning all of the DMA channels. The system's microprocessor must use 8-bit I/O instructions in order to access the DMA controller.

I/O Register Address	Mask Register
000A	Channel 0-3, Mask Register (Set/Clear)
000F	Channel 0-3, Write Mask Register
00D4	Channel 4-7, Mask Register (Set/Clear)
00DE	Channel 4-7, Write Mask Register

The definitions of the Mask Register's bits are as follows:

Register Bit	Bit Definition
0,1	If 00 then set/clear Channel 0 or 4 If 01 then set/clear Channel 2 or 6 If 10 then set/clear Channel 1 or 5 If 11 then set/clear Channel 3 or 7
2	If 0 then clear mask bit If 1 then set mask bit
3-7	RESERVED = 0

The definitions of the Write Mask Register's bits are as follows:

Register Bit	Bit Definition
0	If 0 then unmask Channel 0 or 4 If 1 then mask Channel 0 or 4
1	If 0 then unmask Channel 1 or 5 If 1 then mask Channel 1 or 5
2	If 0 then unmask Channel 2 or 6 If 1 then mask Channel 2 or 6
3	If 0 then unmask Channel 3 or 7 If 1 then mask Channel 3 or 7
4-7	RESERVED = 0

The following is an example of how to use the addresses of the Mask Register (Set/Clear) to mask Channel 2:

Set the I/O address 000A to the value 06H.

DMA Extended Mode

As mentioned previously in the heading "Bus Master Direct Memory Access (DMA)" the DMA extended mode can be used to restore the DMA controller to its initial mask condition. The extended mode of DMA control can be used to mask the DMA controller channels as follows. In this mode the I/O address 0018 is used as a function register. This function register is used to specify the operation that is to be performed. The I/O address 001A is used to provide additional parameters for the functions specified in the function register. In this mode, the control functions of the Mask Register do not use the I/O address 001A register.

The following is the definition of bits for mask control functions executed by setting I/O address 0018:

Register Bit	Bit Definition
0-2	Channel number to which the Program Command will apply
3	RESERVED = 0
4-7	Program Command If 9H then set specified mask bit If AH then clear specified mask bit If DH then clear all mask bits

INTERRUPT PROCESSING

Several interrupt channels are available to the BT-646. The channel to be used by each host adapter board is specified by configuration settings as described in Section 2, the "Unpacking and Installation" section, of this manual. The default value when only one host adapter is installed in a system is Channel 15. If additional host adapters are present in the same system, they must use different interrupt channel values.

The Micro Channel host system contains a programmable interrupt controller which receives all interrupts and directs the host's CPU to a corresponding vector location which in turn contains a memory address for the software Interrupt Service routine which performs the necessary actions required by each interrupt. It also contains a Mask Register whose bits may be set to mask or cleared to permit corresponding interrupt channels to be acknowledged.

In order to respond correctly to BT-646 interrupts during normal operation, the host interrupt controller must be programmed appropriately. The software driver will have to program the host's Interrupt Mask Register and interrupt vector before attempting to use interrupts from the BT-646. The interrupt vector locations and Interrupt Mask Register's bits which need to be cleared to permit acknowledgment of each interrupt channel are listed as follows:

Hardware Interrupt Line	Vector Location In Memory (Hex)	Interrupt Mask Register Hex Address A1
IRQ9	1C4-1C7	Bit 1
IRQ10	1C8-1CB	Bit 2
IRQ11	1CC-1CF	Bit 3
IRQ12	1D0-1D3	Bit 4
IRQ14	1D8-1DB	Bit 6
Default IRQ15	**1DC-1DF**	**Bit 7**

If the BT-646 is configured for Interrupt Channel 15, for example, the Micro Channel system's interrupt controller must be initialized by **clearing** Bit 7 in its Interrupt Mask Register. The address of the interrupt service routine for Channel 15 will be contained in the four bytes of memory beginning at memory address 1DCH.

The remainder of this section describes the structure and operation of the three categories of commands that the host can issue to the BT-646.

HOST ADAPTER COMMANDS

Host adapter command codes and associated parameter bytes are supplied to the BT-646's Control Register under the coordination of certain bits in the BT-646's Status Register. Table 5-1 provides a summary of these commands.

Table 5-1. Host Adapter Commands

Operation Code Hex Value	Host Adapter Command
00	Test CMDC interrupt
01	Initialize Mailbox
02	Start Mailbox command
03	Start BIOS command
04	Inquire Board ID
05	Enable OMBR interrupt
06	Set SCSI Selection Time-Out
07	Set Time On Bus
08	Set Time Off Bus
09	Set Bus Transfer Rate
0A	Inquire Installed Devices
0B	Inquire Configuration
0C	Set Target Mode
0D	Inquire Set-up Information
1A	Write Adapter Local RAM
1B	Read Adapter Local RAM
1C	Write Bus Master Chip FIFO
1D	Read Bus Master Chip FIFO
1F	Echo Data Byte
20	Host Adapter Diagnostic
21	Set Adapter Options
8D	Inquire Extended Set-up Information
9A	Write Inquiry Data Buffer (Target Mode Only)
9B	Read Inquiry Data Buffer (Target Mode Only)

The host system can write a command to the Command/Parameter Register only after checking to see that the Host Adapter Ready bit (HARDY) is set to one, except that the Start Mailbox command and the Enable OMBR Interrupt command may be written at any time. After writing a command, the host may write a predetermined number of parameter bytes to the Command/Parameter Register after checking that the Command/Parameter Register Busy bit (CPRBSY) is zero, indicating that the Command/Parameter Register is not busy and can accept another parameter byte.

In response to some commands, the BT-646 may transfer a predetermined number of parameter bytes back to the host. The BT-646 places each byte into the Data In Register and then sets the Data In Register Ready bit (DIRRDY) to indicate to the host that the byte is ready to be read by the host. After the host has read the input data byte, the BT-646 resets the Data In Register Ready bit (DIRRDY).

The following table lists each host adapter command code along with the associated number of parameter bytes coming into or being sent out from the BT-646 and a brief description of the function performed.

Operation Code	Command	Parameter Byte Count	Direction
00	***TEST CMDC INTERRUPT***	None	None

Description. The BT-646's only response to this command is to set the Command Complete bit (CMDC) in the Interrupt Register. When this bit is set, the host can verify proper functioning of this bit.

Operation Code	Command	Parameter Byte Count	Direction
01	***INITIALIZE MAILBOX***	4	Out

Description. This command specifies the number of mailboxes used by the BT-646, and the base memory location of the mailbox array to be used when executing mailbox commands. Four parameter bytes follow the command byte to provide the following information:

Byte	Description
0	Number of mailboxes needed–must be greater than zero.
1–3	Base mailbox address–specifies the location of the first byte of the mailbox array. Byte 1 is the most significant byte (MSB).

Each mailbox location in memory will occupy four outgoing mailbox bytes and four incoming mailbox bytes. The Command Invalid bit (CMDINV) will be set with the Command Complete bit (CMDC) if the number of mailboxes is specified as zero. At command completion, the Command Complete bit (CMDC) is set to one and the Initialization Required bit (INREQ) is reset to zero to acknowledge that initialization is unnecessary. See the heading "Mailbox Commands" later in this section for more information on the mailbox structure.

Operation Code	Command	Parameter Byte Count	Direction
02	***START MAILBOX COMMAND***	None	None

Description. This command is normally issued every time the host makes an outgoing mailbox entry. Upon receipt of this command, the BT-646 begins scanning for active outgoing mailbox entries and continues scanning until all outgoing mailbox entries have been serviced. This can be accomplished by either beginning the requested operations or queuing the commands and executing them later. To avoid unnecessary interrupt servicing by the host, the Command Complete bit (CMDC) is *not* set after receipt of this command. If this command is received before the Initialize Mailbox command, however, the BT-646 will then set both the Command Invalid bit (CMDINV) and the Command Complete bit (CMDC) in the Status Register.

Operation Code	Command	Parameter Byte Count	Direction
03	***START BIOS COMMAND***	None	None

Description. This command is used exclusively by the BT-646's BIOS to communicate with the BT-646's firmware. This command is *not* used by application programs.

Operation Code	Command	Parameter Byte Count	Direction
04	***INQUIRE BOARD ID***	4	In

Description. Upon receipt of this command, the BT-646 sends four bytes of data to the host which contain identification and revision information about itself. Refer to the following byte contents:

Byte **Description**

0 BusLogic Board Type–value allows software support for PC/AT, Micro Channel and Micro Channel BusLogic host adapters.

Hex Value	Meaning
41	Board is a BT-542B or BT-742A with 64-head BIOS
42	Board is a BT-646 with 64-head BIOS
Other	Reserved

1 Custom Features–indicates what custom features may be supported by the BT-646.

Hex Value	Meaning
41	Standard BT-646
Other	Reserved

2 Firmware Revision Level–a byte designating the revision level of the BT-646 firmware. ASCII "0"–"9"

3 Firmware Version–a byte designating the revision level of the installed firmware

Once the four bytes of data have been transferred, the Command Complete bit (CMDC) is set indicating normal command completion.

Operation Code	Command	Parameter Byte Count	Direction
05	***ENABLE OMBR INTERRUPT***	1	Out

Description. This command specifies whether the Outgoing Mailbox Ready bit (OMBR) should be set when an outgoing mailbox entry is cleared by the BT-646. The single parameter byte from the host instructs the BT-646 as follows:

Hex Value	Meaning
00	The Outgoing Mailbox Ready Interrupt bit (OMBR) is *not* to be set.
01	The Outgoing Mailbox Ready Interrupt bit (OMBR) is to be set once the outgoing mailbox has been cleared by the BT-646.

To avoid unnecessary interrupt servicing by the host, the Command Complete bit (CMDC) is not set after receipt of this command. If the parameter byte contains a value other than 00H or 01H, however, the Command Invalid bit (CMDINV) is set, as well as the Command Complete bit (CMDC), to indicate receipt of an invalid command.

Operation Code	Command	Parameter Byte Count	Direction
06	***SET SCSI SELECTION TIME-OUT***	4	Out

Description. This command specifies the wait time used to determine whether or not a SCSI selection was successful. If the SCSI Busy signal is *not* returned within the specified time-out period, the selection will be terminated and the appropriate error message recorded in the returned CCB. The contents of the four parameter bytes received with this command are as follows:

Byte	Description
0	Enable/Disable SCSI Selection Time-Out–specifies whether or not the SCSI Selection time-out is used. Refer to the following values.

Hex Value	Meaning
00	No time-out is performed.
01	The time specified in Bytes 02 and 03 is used as the SCSI time-out period.

1	Reserved–must be set to zero.
2–3	Time-Out Value–specifies the SCSI selection time-out period in milliseconds. The default value is 250 milliseconds. Byte 2 is the most significant byte.

After command completion, the Command Complete bit (CMDC) is set indicating normal command completion. The Command Invalid bit (CMDINV) is set only if data Byte 0 is invalid (neither 00H nor 01H) or data Byte 1 is not zero which indicates an invalid command.

Operation Code	Command	Parameter Byte Count	Direction
07	***SET PREEMPT TIME ON BUS***	1	Out

Description. This command specifies the time the BT-646 is allowed on the Micro Channel bus after being preempted. One parameter byte is sent to the BT-646 indicating the length of time in microseconds. This time can be from 2 to 15 microseconds. The default value is 7 microseconds. After command completion, the Command Complete bit (CMDC) is set indicating normal command completion. If the data byte value is greater than 15, the Command Invalid bit (CMDINV) is set indicating that an invalid command was received.

Operation Code	Command	Parameter Byte Count	Direction
08	***SET TIME OFF BUS***	1	Out

Description. This command specifies the time the BT-646 will spend off the Micro Channel bus. One parameter byte is sent to the BT-646 indicating the length of time in microseconds. This command is treated as a no operation command. It is supported for software compatibility to ISA software.

Operation Code	Command	Parameter Byte Count	Direction
09	***SET BUS TRANSFER RATE***	1	Out

Description. This command is treated as a no operation command. It is supported for software compatibility to ISA software.

Operation Code	Command	Parameter Byte Count	Direction
0A	***INQUIRE INSTALLED DEVICES***	8	In

Description. This command asks the BT-646 to indicate the devices connected to the SCSI bus. The BT-646 issues the SCSI Test Unit Ready command to each target/Logical Unit Number (LUN) combination and reports the results using eight bytes of data returned to the host through the Data In Register. Each byte has an associated target device; i.e., Byte 2 represents Target 2. If a bit has a value of one, the associated LU (Logical Unit) is installed. Each bit within a byte has an associated LU; i.e., Bit 3 represents LU 3, etc.

The byte associated with the BT-646 will always be zero. Once all information has been transferred, the Command Complete bit (CMDC) is set to indicate normal command completion.

Operation Code	Command	Parameter Byte Count	Direction
0B	***INQUIRE CONFIGURATION***	3	In

Description. The BT-646 returns three bytes of data describing the host DMA channel, the interrupt channel, and the SCSI ID values set during configuration set up.

The BT-646 receives these parameters through the Programmable Option Select (POS) registers. For compatibility with ISA software they can be read by the system using this command.

Byte	Description	Byte	Description	Byte	Description
0	Host DMA channel	1	Interrupt channel	2	SCSI ID
	Bit 0 = Reserved		Bit 0 = IRQ9		Bit 0-2 = SCSI ID, binary value
	Bit 1 = Reserved		Bit 1 = IRQ10		Bit 3-7 = Reserved, set to zero
	Bit 2 = Reserved		Bit 2 = IRQ11		
	Bit 3 = Reserved		Bit 3 = IRQ12		
	Bit 4 = Reserved		Bit 4 = Reserved		
	Bit 5 = Reserved		Bit 5 = IRQ14		
	Bit 6 = Reserved		Bit 6 = IRQ15		
	Bit 7 = Reserved		Bit 7 = Reserved		

Operation Code	Command	Parameter Byte Count	Direction
0C	***SET TARGET MODE***	2	Out

Description. Two parameter bytes specify if the BT-646 will operate in target mode. The contents of these bytes are as follows:

Byte	Description
0	Specifies the SCSI operating modes the BT-646 will use. Byte values are as follows:

Hex Value	Meaning
00	Operate as an initiator only. This is the default value after a hard reset, soft reset, or power-on reset.
01	Operate as both an initiator and a target SCSI device.
Other	Invalid

Byte	Description
1	Each bit of this byte is used to specify which Logical Units will respond in target mode. Only when a bit value is one will the corresponding LU be recognized as installed. If Byte 0 contains 00H, Byte 1 is ignored. If Byte 0 contains 01H, Byte 1 must have at least one bit set to indicate at least one LU to operate in target mode.

If target mode is not specified, the BT-646 operates just like any other SCSI initiator. If target mode is not specified or if the corresponding LUN is not enabled, then the BT-646 will respond with the following: (1) a Check Condition status, (2) a Sense Code equal to 2 (Not Ready), and (3) Additional Sense Key equal to 4 (Not Ready).

If target mode is specified but the BT-646 is busy processing another process, then the BT-646 will respond to an initiator's selection with a Busy status.

If the BT-646 does not have target mode support installed, the BT-646 will indicate that the command is invalid. If this command is issued to change from target mode to initiator only mode while there are still target mode CCB's being processed by the BT-646, the BT-646 will also respond by setting the Command Invalid status bit (CMDINV).

Operation Code	Command	Parameter Byte Count	Direction
0D	***INQUIRE SETUP INFORMATION***	1	Out
		16	In

Description. This command asks the BT-646 to provide information on its the current set-up status. This command is followed by a parameter which specifies the number of bytes which the BT-646 will send to the host. The BT-646 normally transfers 16 bytes of information.

Parameter Byte

Byte	Description
0	Specifies the number of data bytes, from 0 to 255, to be sent to the host.

Data In Byte/Bit Assignments

Byte	Description
0	SCSI synchronous negotiation and parity status.

Bit	Meaning
0	A value of zero indicates that SCSI synchronous negotiation will not be initiated by the BT-646. A value of one indicates that SCSI synchronous negotiation will be initiated by the BT-646 when appropriate. See the heading "Micro Channel Configuration Settings" in Section 2 of this manual for details.
1	A value of zero indicates that inbound SCSI transfers are not parity checked. A value of one indicates that parity checking on inbound SCSI transfers is enabled. See the heading "Micro Channel Configuration Settings" in Section 2 of this manual for details.
2–7	Reserved (zero).

1	BUS TRANSFER RATE–Returns the value set by the Set Bus Transfer Rate command.
2	TIME ON BUS–Returns the time set by the Set Time On Bus command.
3	TIME OFF BUS–Indicates the time set by the Set Time Off Bus command.
4	NUMBER OF MAILBOXES–Returns the number of mailboxes established by a previous Initialize Mailbox command. If the Initialize Mailbox command has not yet been completed successfully, the returned number will be 00H.

Byte	Description (Continued)
5–7	Base Mailbox Address–Returns the base address of the mailbox array established by a previous Initialize Mailbox command. The MSB is Byte 5. If the Initialize Mailbox command has not been completed successfully, these bytes have no meaning.
8	SYNCHRONOUS VALUES FOR TARGET 0–Contains information resulting from synchronous negotiation with Target 0. If the address is that of the BT-646 or a non-existent target, this byte will contain 00H.

Bit	Meaning
0–3	Contain the negotiated **offset** value, usually between 1 and 15.
4–6	Contain a value between 0 and 7 that defines the synchronous **transfer period** according to the following equation. Period = 200 + 50 (value) nanoseconds.
7	Set (one) if synchronous transfer is negotiated. Reset (zero) if asynchronous transfers are used.

The following bytes have the same structure as Byte 8, but for Targets 1-7.

9	SYNCHRONOUS VALUES FOR TARGET 1
10	SYNCHRONOUS VALUES FOR TARGET 2
11	SYNCHRONOUS VALUES FOR TARGET 3
12	SYNCHRONOUS VALUES FOR TARGET 4
13	SYNCHRONOUS VALUES FOR TARGET 5
14	SYNCHRONOUS VALUES FOR TARGET 6
15	SYNCHRONOUS VALUES FOR TARGET 7
16	RETURN OF BYTE 1 OF OPC0DE 21

Operation Code	Command	Parameter Byte Count	Direction
1A	***WRITE ADAPTER LOCAL RAM***	3	Out

Description. The three parameter bytes contain a 24-bit address (first parameter byte is MSB) which points to a 64-byte area in the main system memory. Upon receipt of this command the BT-646 performs a bus master DMA transfer of the designated 64 bytes from the host's main memory into its own local RAM memory. Once the 64 bytes have been successfully transferred to the BT-646, the Command Complete bit (CMDC) is set indicating that this command has been completed.

Operation Code	Command	Parameter Byte Count	Direction
1B	***READ ADAPTER LOCAL RAM***	3	Out

Description. The three parameter bytes contain a 24-bit address (first parameter byte is MSB) which points to a 64-byte area in the main system memory. Upon receipt of this command the BT-646 performs a bus master DMA transfer of 64 bytes of data from its own local RAM into the designated 64 bytes in the host's main memory. Once the 64 bytes have been successfully transferred to the host's memory, the Command Complete bit (CMDC) is set indicating that this command has been completed.

Operation Code	Command	Parameter Byte Count	Direction
1C	***WRITE BUS MASTER CHIP FIFO***	3	Out

Description. The three parameter bytes contain a 24-bit address (first parameter byte is MSB) which points to a 54-byte area in main system memory. Upon receipt of this command the BT-646 performs a bus master DMA transfer of the designated 54 bytes from the host's main memory into its own bus master chip FIFO. Once the 54 bytes have been successfully transferred to the BT-646, the Command Complete bit (CMDC) is set indicating that this command has been completed.

Operation Code	Command	Parameter Byte Count	Direction
1D	***READ BUS MASTER CHIP FIFO***	3	Out

Description. The three parameter bytes contain a 24-bit address (first parameter byte is MSB) which points to a 54-byte area in the main system memory. Upon receipt of this command the BT-646 performs a bus master DMA transfer of 54 bytes of data from its bus master chip FIFO into the designated 54 bytes in the host's main memory. Once the 54 bytes have been successfully transferred to the host's memory, the Command Complete bit (CMDC) is set indicating that this command has been completed.

Operation Code	Command	Parameter Byte Count	Direction
1F	***ECHO COMMAND DATA***	1	Out
		1	In

Description. This command is used to test the Command/Parameter and Data In Registers and the associated control bits in the remaining I/O registers. The BT-646 receives one parameter byte in the Command/Parameter Register and then instructs the host to read the same byte back from the Data In Register by setting the Data In Register Ready bit (DIRRDY). After the host has read the byte, the Command Complete bit (CMDC) is set indicating that this command has been completed.

Operation Code	Command	Parameter Byte Count	Direction
20	***HOST ADAPTER DIAGNOSTIC***	0	Out
		0	In

Description. This command instructs the BT-646 to conduct its self-diagnostic tests. A hard reset of the BT-646 will occur without issuing a SCSI bus reset. After this command is executed, the BT-646 must be reinitialized before normal operation can continue. After issuing this command, the host should monitor the BT-646's Status Register to obtain this command's status. It should also wait until the Diagnostic Active bit (DACT) of the Status Register is reset indicating that the self-diagnostics have been completed successfully. It then should wait for one or more of the following bits to be set: the Diagnostic Failure bit (DFAIL), the Host Adapter Ready bit (HARDY), or the Data In Register Ready bit (DIRRDY). If the Host Adapter Ready bit (HARDY) is set and the Diagnostic Failure bit (DFAIL) is reset, then an error did not occur during the diagnostics.

If the Diagnostic Failure bit (DFAIL) or the Data In Register Ready bit (DIRRDY) is set, then an error did occur during the diagnostics. In this case, after the Data In Register Ready bit (DIRRDY) is set, then the Data In Register should be read for the error code that will equal the number of failed diagnostic tests. No data byte is returned if there is no error. When this command is completed, the Interrupt Register will be updated as follows: the Command Complete bit (CMDC) and the Interrupt Valid bit (INTV) will be set.

Operation Code	Command	Parameter Byte Count	Direction
21	***SET ADAPTER OPTIONS***	3	Out

Description. The host can use this command to specify certain configuration options for the BT-646. The host sends the specified configuration options to the BT-646 via a parameter list. This three-byte parameter list follows the command opcode. As the default, Bytes 1 and 2 of the parameter list are set. The parameter list is as follows:

Parameter Byte

Byte	Description
0	Specifies the number of bytes remaining in the parameter list. This specified length equals the total number of bytes in the parameter list minus one.
1	Disables the SCSI disconnection option. Each bit corresponds to a SCSI device (e.g., Bit 0 represents the SCSI device assigned to SCSI address 0). When the bit is set, the BT-646 will prevent the corresponding SCSI device from disconnecting. When the bit is reset, the BT-646 will allow the corresponding SCSI device to disconnect. Byte 16 of the Inquire Setup command reflects the state of this byte.
2	Disables the SCSI Busy retry option. Each bit corresponds to a SCSI device (e.g., Bit 0 represents the SCSI device assigned to SCSI address 0). When the bit is set, the BT-646 will prevent the corresponding SCSI device from being retried when the SCSI device returns a Busy status. When the bit is reset, the BT-646 will allow the corresponding SCSI device to be retried when the SCSI device returns a Busy status.

Operation Code	Command	Parameter Byte Count	Direction
8D	***INQUIRE EXTENDED SETUP INFORMATION***	1 4	Out In

Description. This command asks the BT-646 to provide information concerning its set up. This command is followed by a parameter which specifies the number of bytes which the BT-646 will send to the host. The BT-646 normally transfers four bytes of information.

Parameter Byte

Byte	Description
0	Specifies the number of data bytes, from 0 to 255, to be sent to the host.

Data In Byte/Bit Assignments

0	ASCII code specifying host adapter bus type "A" for PC/AT Bus "E" for EISA Bus "M" for Micro Channel
1	BIOS Address Code C8 for 0C8000H CC for 0CC000H D0 for 0D0000H D4 for 0D4000H D8 for 0D8000H DC for 0DC000H 00 for BIOS Disabled

Data In Byte/Bit Assignments (Continued)

2-3 Maximum number of segments permitted in the scatter-gather list for this host adapter

Byte 2 is LSB = 00H

Byte 3 is MSB = 20H (8192)

Operation Code	Command	Parameter Byte Count	Direction
9A	***WRITE INQUIRY DATA BUFFER***	4	Out

Description. When the BT-646 is in target mode, it reserves a 64-byte Inquiry Data Buffer to store the Inquiry data. This command copies 64 bytes of data from the system memory into the Inquiry Data Buffer. Upon the receipt of an Inquiry command from an initiator, the Inquiry data is returned to the initiator. The actual number of bytes returned is defined by Byte 4 of the CDB of the Inquiry command issued by the initiator.

Byte	Description
0	Byte 0 (the least significant byte) of the system memory address where the 64-byte data is to be copied from.
1	Byte 1 of the system memory address
2	Byte 2 of the system memory address
3	Byte 3 (the most significant byte) of the system memory address

Operation Code	Command	Parameter Byte Count	Direction
9B	***READ INQUIRY DATA BUFFER***	4	Out

Description. When the BT-646 is in target mode, it reserves a 64-byte Inquiry Data Buffer to store the Inquiry data. This command copies the contents of the Inquiry Data Buffer into the system memory.

Byte	Description
0	Byte 0 (the least significant byte) of the system memory address where the 64-byte data is to be copied to.
1	Byte 1 of the system memory address
2	Byte 2 of the system memory address
3	Byte 3 (the most significant byte) of the system memory address

MAILBOX COMMANDS

With today's application requirements, sophisticated operating systems, and performance capabilities of the latest systems using faster CPUs and higher bus transfer rates, it is desirable to have several different tasks running simultaneously in support of many different users. These tasks require a wide variety of I/O peripheral devices such as hard disks, tape backup units and optical drives.

One advantage offered by the SCSI bus is that up to seven I/O devices may be connected to one host adapter. An effective method is needed to manage the processing of each separate task in a system where individual users make use of many different SCSI I/O devices. A method that takes advantage of the local microprocessor, bus master ASIC, and other intelligence features of the BT-646 is needed. Otherwise, the main system CPU would be loaded down. One such method is the mailbox structure of communication between the host system and the BT-646.

Mailboxes are reserved storage areas which reside at a fixed contiguous memory location in the host system. The mailboxes coordinate communications between the host system and the BT-646. Outgoing mailboxes are used for sending command information to the BT-646 and incoming mailboxes are used by the BT-646 to return status information about completed commands to the host or, in target mode with a CCB not available, to request CCBs from the host.

This interface architecture provides a means of passing SCSI device commands from a task, by means of a software driver, to the BT-646 in a multi-tasking, multi-user environment with minimal host intervention. In this mode the BT-646 can concurrently execute multiple commands for multiple targets. The BT-646's on-board intelligence allows it to complete bus master data transfers, to manage SCSI disconnects and reconnects and to perform other activities which reduce host intervention; thereby, increasing overall system I/O throughput. The following few pages describe the organization and operation of this approach.

With most procedures in a computer system, some means of initialization must be performed to establish starting reference conditions. After power is applied to a system, many system initialization functions are carried out before any application programs are activated.

Similarly, before any mailbox commands can be supplied to the BT-646, another specific initialization process must be conducted.

First, the host system allocates storage space at a fixed contiguous location somewhere in the main system memory where the communication mailboxes will be placed. The host creates the required number of 4-byte outgoing mailboxes, followed immediately in memory by *an equal number* of 4-byte incoming mailboxes. The host then sends an **Initialize Mailbox** command to the BT-646. This command tells the BT-646 how many mailboxes will be used and the base address of the first outgoing mailbox in the main system memory as described in the heading "Host Adapter Commands" earlier in this section. There should typically be at least one set of Out/In mailboxes for each active and independent task. Figure 5-1 illustrates an array of four outgoing and four incoming mailboxes.

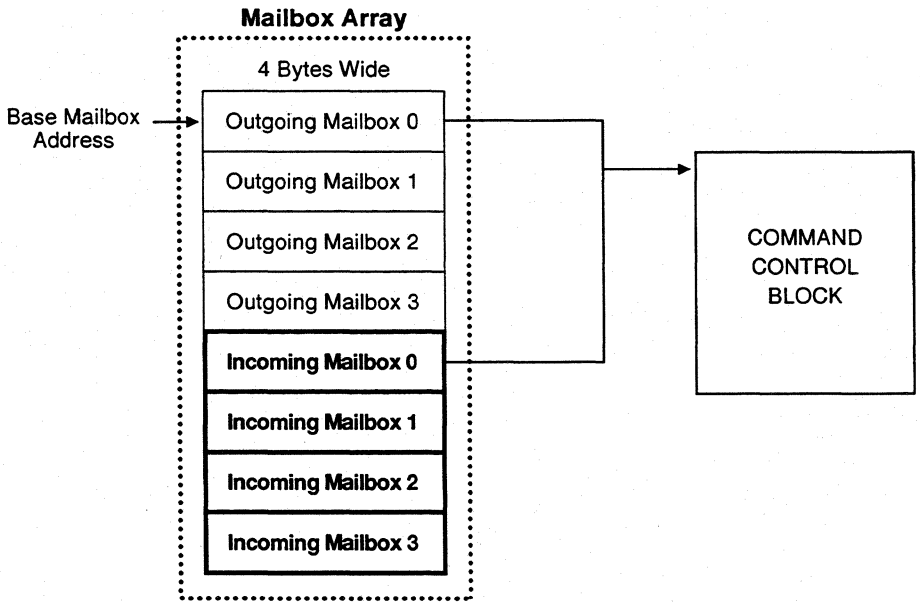


Figure 5-1. Mailbox Array

Before describing the use of outgoing and incoming mailboxes, their structure and contents will be defined.

OUTGOING MAILBOX STRUCTURE

The following are the possible contents of the four bytes of each outgoing mailbox.

Byte	Function	
0	Action Code	
	Hex Value	**Definition**
	00	Outgoing Mailbox is not in use
	01	Start a Mailbox command
	02	Abort a Mailbox command
1-3	CCB Address (Byte 1 is MSB)	

The first byte of the outgoing mailbox is the "action" code. If the byte is zero in any particular outgoing mailbox, the host can place a CCB address in the last three bytes of that mailbox and set the first byte in the same mailbox to start or to abort the command contained in the designated CCB. After the BT-646 has copied the information in an outgoing mailbox in the course of executing commands, it releases that mailbox by clearing its first byte so the host can use it again.

INCOMING MAILBOX STRUCTURE

When a CCB has been provided to the BT-646 in initiator mode or target mode, the BT-646 uses incoming mailboxes to provide information regarding the completion of the CCB to the host. The possible contents of the four bytes of each incoming mailbox of this type are as follows:

Byte	Function	
0	Completion Code	
	Hex Value	**Definition**
	00	Incoming Mailbox is not in use
	01	CCB completed without error
	02	CCB aborted at request of host
	03	Aborted CCB not found
	04	CCB completed with error
1-3	CCB Address (Byte 1 is MSB)	

If the first byte in an incoming mailbox is zero in any particular incoming mailbox, the BT-646 can place the address of the completed CCB in the last three bytes of that mailbox and can set the first byte in the same mailbox to indicate the manner in which the command was completed.

The format for an incoming mailbox used by the BT-646 in target mode to request a CCB will be discussed under the heading "Host Adapter Target Mode Operation—CCB Not Available" later in this section.

To establish communication between the BT-646 and an attached SCSI device to execute some command, either the BT-646 or the SCSI device can initiate the SCSI command. The other party in the communication is the target. The default case is for the BT-646 to be the initiator. If the BT-646 is to be the target, however, the host must send another host adapter command to the BT-646 to **Set Target Mode**. The use of the mailbox architecture with the BT-646 in initiator mode will be described first.

Assuming that a task is running and that communication with a SCSI device is required the host system performs the following preparation to process the I/O request:

- Allocates an area in the main system memory for data storage or retrieval
- Creates a CCB which identifies the SCSI I/O device, provides an address which points to the data area in the main memory and specifies other detailed information about the SCSI command
- Places an address pointer to the CCB and an "action" code in an outgoing mailbox
- Sends a Start Mailbox command to the BT-646.

When the BT-646 has received the Start Mailbox command, it performs the following activities:

- Begins scanning the outgoing mailboxes to find entries with action codes using a round-robin scheme
- Copies outgoing mailbox information into its local RAM and then releases the outgoing mailbox
- Copies the CCB pointed to by the outgoing mailbox into its local RAM
- Executes the SCSI command specified in the CCB as soon as the SCSI bus is not busy.

The action taken by the BT-646 to release an outgoing mailbox once its information has been copied to local RAM depends on the host adapter command **Enable OMBR Interrupt.** If this command has been issued to the BT-646 to enable the Outgoing Mailbox interrupt (OMBR), the BT-646 will do one of the following:

- If no interrupt bits are set in the Interrupt Register, the BT-646 will set the Outgoing Mailbox Ready (OMBR) and the Interrupt Valid (INTV) bits in the Interrupt Register, and then will assert the Interrupt Request signal on the Micro Channel bus.
- If the Outgoing Mailbox Ready bit (OMBR) is already set to indicate that a previous outgoing mailbox was released and the interrupt was not yet cleared by the host then no additional notification to the host is required.
- If interrupts other than Outgoing Mailbox Ready interrupt (OMBR) are pending, the BT-646 will wait for all of them to be cleared before setting the Outgoing Mailbox Ready bit (OMBR).

After processing an outgoing mailbox, the BT-646 will scan for another active entry beginning with the outgoing mailbox following the one just completed. The host can ensure that the BT-646 will always find the next command with minimum overhead by placing commands in the outgoing mailboxes in consecutive, round-robin order. The BT-646 will look for additional outgoing mailbox entries until it finds an empty outgoing mailbox, at which time it will stop scanning. It will start scanning again when the host issues a Start Mailbox command to indicate that another entry has been made. Active entries are transferred into local RAM and placed in a command queue. The local RAM has enough space to store up to 32 CCBs at any one time.

The commands are taken from the queue in a first-in first-out basis to be executed as soon as the SCSI bus is not busy. Commands will not necessarily be completed in the same order because the execution time of each command may be different.

If a Busy condition from the target device temporarily prevents the execution of a command, it is returned to the end of the queue and will be retried when queued up again. This process will continue until the Busy condition is resolved and the command can be completed.

When an outgoing mailbox is found to contain an abort code, the associated CCB pointer is used by the BT-646 to locate the mailbox command to be aborted. The designated CCB may be active or queued. If the CCB can be found the command is terminated as soon as possible. The BT-646 then makes an incoming mailbox entry to indicate that the command was terminated.

If the CCB can not be found, the command may have already been completed in a normal manner or may have been previously aborted. This situation will also be reported to the host in an incoming mailbox entry.

At the completion of each mailbox command, the target device can report that the completion was "GOOD" or that it has additional status which must be checked. In the latter case, the BT-646 may automatically issue a Request Sense command to get the additional status data from the target device. This sense data is stored in a designated area at the end of the CCB in host memory. The ability of the BT-646 to issue the Request Sense command automatically requires that Auto Sense be enabled as described in Section 2, the "Unpacking and Installation" section.

At the completion of a mailbox command, the BT-646 writes status information into the BTSTAT and SDSTAT fields in the CCB in the main system memory. The BT-646 then writes into an incoming mailbox a completion status byte and a pointer to the completed CCB.

After placing an entry into an incoming mailbox, the BT-646 will take one of the following actions:

- If no interrupt bits are set in the Interrupt Register, the BT-646 will set the Incoming Mailbox Loaded (IMBL) and the Interrupt Valid (INTV) bits in the Interrupt Register and then will assert the Interrupt Request signal on the Micro Channel bus.
- If the Incoming Mailbox Loaded bit (IMBL) is already set to indicate that a previous incoming mailbox was loaded and the interrupt has not yet been cleared by the host then no additional notification to the host is required.
- If interrupts other than Incoming Mailbox Loaded interrupt (IMBL) are pending, the BT-646 will wait for all of them to be cleared before setting the Incoming Mailbox Loaded bit (IMBL).

Whenever the host sees that the Incoming Mailbox Loaded bit (IMBL) is set, it begins to scan the incoming mailboxes for active entries. The host will read each active incoming mailbox to obtain status information and pointers to the completed CCBs and then will release the incoming mailboxes for future use. When all active incoming mailboxes have been processed, the host then clears the Incoming Mailbox Loaded bit (IMBL) and the Interrupt Invalid bit (INTV) in the BT-646's Interrupt Register.

The BT-646 places **no** restrictions on the data segment address boundaries and lengths that are allowed. For maximum performance, however, it is recommended that all starting addresses (mailboxes, CCBs and data pointers) be on 32-bit (double-word) boundaries and all transfer byte counts be a multiple of four.

HOST ADAPTER IN TARGET MODE

When the Set Target Mode host adapter command is issued by the host to the BT-646 to place it in target mode, Byte 1 of the command serves as a LUN mask byte to specify which of up to eight LUNs may respond to initiator- generated SCSI commands. Seven SCSI commands may be issued from another host adapter to the BT-646 in this mode:

TEST UNIT READY
REQUEST SENSE
INQUIRY
SEND
RECEIVE
RESERVE
RELEASE.

There are also two host adapter commands that the BT-646 supports when it is in target mode. For information on the Write Inquiry Data Buffer command (9A) and the Read Inquiry Data Buffer command (9B), refer to their description in the section, "Host Adapter Commands" earlier in this chapter.

The BT-646 will respond to any other command with a Check Condition status code. Subsequent sense information provided in response to a Request Sense command from the initiator will be Illegal Request (Sense Key 05H) and Invalid Command Operation Code (Additional Sense Key 20H).

The first three of the valid commands involve no data transfers and are responded to directly by the BT-646 without the need of any CCBs. The Send and Receive commands, however, require the host to provide a CCB containing information necessary to complete the command such as the data buffer address, initiator address, LUN number and direction bits. CCBs for the Send and Receive commands may be provided to the BT-646 before the SCSI command is received or the BT-646 may request the CCBs after it receives the SCSI command.

If target mode is not specified or if the corresponding LUN is not enabled, then the BT-646 will respond with the following: (1) a Check Condition status, (2) a Sense Code equal to 2 (Not Ready), and (3) Additional Sense Key equal to 4 (Not Ready).

If target mode is specified but the BT-646 is busy processing another process, then the BT-646 will respond to an initiator's selection with a Busy status.

Host Adapter Target Mode Operation—CCB Available

After issuing the Set Target Mode command to the BT-646, the host uses its knowledge of the system configuration to get ready for possible future communication to or from the BT-646. The host generates for the BT-646 two CCBs for each LUN enabled by the LUN mask byte in the Set Target Mode command and for each initiator which might transfer data to or from one of these host adapter LUNs.

One of these CCB pairs specifies a data buffer area for outgoing data from the initiator using the Send command.

The second of these CCB pairs functions as a data buffer area for incoming data to the initiator using the Receive command.

The initiator will request configuration and availability information using the Test Unit Ready, Request Sense and Inquiry commands. When it has identified the host adapter target, it may then issue the Send and Receive commands to the selected LUN to send or to receive data packets.

The BT-646 accepts the SCSI command and transfers data into or out from the data area assigned by the appropriate CCBs. After the SCSI command is completed, the BT-646 notifies the host of the completion by posting completion information in the appropriate CCB fields, loading an incoming mailbox entry and generating the Incoming Mailbox Loaded interrupt (IMBL).

Host Adapter Target Mode Operation—CCB Not Available

An initiator may attempt to issue a SCSI command to the BT-646 as a target before the required CCBs have been established by the host.

If the BT-646 has not been set to target mode, it will respond to its Target ID with a Busy status.

If the BT-646 has been set to target mode, it will respond to its Target ID and the Test Unit Ready, Request Sense and Inquiry commands. When it receives a Send or Receive command, however, it will obtain the IDENTIFY MESSAGE OUT to identify which LUN has been specified. It will then request the CDB from the initiator and will disconnect.

Using information from the CDB, the BT-646 will then load an incoming mailbox to notify the host that a new CCB for a specific data address, length and direction must be provided. The format of the incoming mailbox when used by the BT-646 in target mode to request a CCB is as follows:

Byte	Function	
0	Status Code	
	Hex Value	**Definition**
	10	Indicates that the host adapter in target mode received a command for which no CCB was available.
1		
	Bits 0-2	LUN number specified by the command from the Initiator.
	Bit 3	SCSI command is a Send command. The host must prepare a CCB to transmit data from the initiator to the host adapter.
	Bit 4	SCSI command is a Receive command. The host must prepare a CCB to transmit data from the host adapter to the initiator.
	Bits 5-7	SCSI ID of initiator.
2-3	Data Length	These bytes repeat the high order two bytes of the data length specified in the Send or Receive command. This informs the host that the CCB must point to a data buffer large enough to transmit this amount of data and up to 256 additional bytes.

After obtaining the information from the incoming mailbox, the host will create the requested CCB and make it available to the BT-646 by making an outgoing mailbox entry. Now having the necessary CCB, the BT-646 reconnects and completes the Send or the Receive SCSI command.

COMMAND CONTROL BLOCK STRUCTURE

A CCB contains detailed information about a SCSI command. The basis structure is presented in the following table. Detailed descriptions of each byte or field in the CCB follow this table.

COMMAND CONTROL BLOCK FORMAT

BYTE	DESCRIPTION
0	CCB Operation Code
	Hex Value **Meaning**
	00 Initiator CCB
	01 Target CCB
	02 Initiator CCB with scatter-gather
	03 Initiator CCB with residual data length returned
	04 Initiator CCB with scatter-gather, and residual data length returned
	81 SCSI bus device reset
1	SCSI ID and Direction Control
	Bits 2-0 Logical Unit Number (LUN)
	Bits 4-3 Specify direction of data transfer and whether data length is checked
	Bits 7-5 Target ID if an initiator CCB Initiator ID if a target CCB
2	Length of SCSI Command Descriptor Block
3	Request Sense Allocation Length/Disable Auto Sense
4–6	Data Length (Byte 4 is MSB)
7–9	Data Pointer (Byte 7 is MSB)
10–12	Link Pointer (Byte 10 is MSB)
13	Command Linking Identifier
14	BT-646 Status (BTSTAT)
15	SCSI Device Status (SDSTAT)
16–17	Reserved and set to zero
18–n	SCSI Command Descriptor Block (Length specified by Byte 2)
n–m	Reserved For Request Sense Information Bytes (Length of reserved space is specified in Byte 3)

COMMAND CONTROL BLOCK FIELD DEFINITIONS

BYTE	FIELD	DESCRIPTION
0	CCB Operation Code (Hex)	
	00	The BT-646 acts as the initiator to issue the SCSI command specified in the CDB field of the CCB to the specified target SCSI device.
	01	The BT-646 operates in target mode and the CCB is used to service a command sent to it from another initiator. If this operation code is sent to a BT-646 that has not yet been set to target mode, the BT-646 returns a 1AH code in the Btstat field.
	02	The BT-646 acts as the initiator to issue a command to the specified target device in which scatter-gather data transfers are performed. In this case, the Data Length and Data Pointer fields of the CCB have a different meaning as described later in this section.
	03	The BT-646 functions as described in the preceding operation code 00H. The only difference between operation code 00H and 03H is the updating of Bytes 4-6 (Data Length field) after the command has been completed. Refer to the description of the Data Length field later in this section for more information on this topic.
	04	The BT-646 functions as described in the preceding operation code 02H. The only difference between operation code 02H and 04H is the updating of Bytes 4-6 (Data Length field) after the command has been completed. Refer to the description of the Data Length field later in this section for more information on this topic.
	81	A BUS DEVICE RESET message is sent by the BT-646 to the specified target. This forces the BT-646 to abort all outstanding tasks against the selected target and to ignore all remaining CCB bytes.
1	Address and Control	Identifies the address of the devices involved in the command and provides information about the expected direction of data flow.
	Bits 7–6–5	Specifies the target SCSI ID if the CCB is an initiator CCB. Specifies the initiator ID if the host adapter is in target mode.
	Bits 4–3	Set to determine the direction of the data transfer as follows:

Initiator CCB

Bit 4	Bit 3	Host Adapter Action
0	0	Direction of data transfer determined by the SCSI command being executed.
0	1	Data transferred from SCSI device to host adapter. Data transfer will be a Data In phase. Data length will be checked.
1	0	Data transferred from host adapter to SCSI device. Data transfer will be a Data Out phase. Data length will be checked.
1	1	No data transfer.

COMMAND CONTROL BLOCK FIELD DEFINITIONS (Continued)

BYTE	FIELD	DESCRIPTION
		Target CCB 0 0 Return Invalid Target Direction code in Btstat field. 0 1 Data transferred from SCSI device to host adapter. Data transfer will be a Data Out phase. 1 0 Data transferred from host adapter to SCSI device. Data transfer will be Data In phase. 1 1 Return Invalid Target Direction code in Btstat field.
	Bits 2–0	Target LUN if an initiator CCB. If the target accepts an IDENTIFY message out, these bits will be provided in the LUN field of the message byte. The LUN field in the SCSI CDB is expected to be zero. If the target does not accept an IDENTIFY message out, the LUN field in the SCSI CDB must contain the correct LUN address. All SCSI-II devices or devices supporting Common Command Set (CCS) accept the IDENTIFY message out. Any device not meeting these requirements should be examined individually to determine whether the LUN address should be placed in Byte 1 of the CCB or in the SCSI CDB.
2	Length of SCSI Command Descriptor Block	Specifies the number of bytes in the SCSI CDB beginning at Byte 18 of the CCB.
3	Request Sense Allocation Length/	Indicates the number of bytes in the CCB following the CDB reserved for information that may be obtained by allocation length as its byte count in the CDB for the Request Sense command it issues in response to a Check Condition status received from a target SCSI device at the completion of a command. Sense information is placed in the specified request sense allocation area with a length not exceeding the request sense allocation length. This byte also provides a software method for disabling the Automatic Sense function to override the switch settings described in Section 2, the "Unpacking and Installation" section. The following values are defined for this byte: **Hex Value** — **Meaning** 00 — Allocate 14 bytes for request sense data 01 — Disable automatic request sense 02-07 — Reserved 08-FF — Valid allocation lengths for SCSI sense data If the BT-646 is in target mode and returns a Check Condition status to the initiator at the completion of a SCSI command, the initiator should issue a Request Sense command to the BT-646. The BT-646 will then provide the appropriate sense information. However, if the command that originally failed was a Send or a Receive command, the same sense information bytes that will be sent to the initiator are also sent to the host when the CCB is returned.

COMMAND CONTROL BLOCK FIELD DEFINITIONS (Continued)

BYTE	FIELD	DESCRIPTION
4–6	Data Length	Specify the byte length of the data transfer. Error code 12H is posted in the Btstat field if a data overrun occurs. If a scatter-gather operation is specified by the CCB, the Data Length field contains the total number of bytes in the Data Segment List. With operation code 00H or 02H these bytes are not changed after the command is completed; however, with operation code 01H the BT-646 will set these bytes to the actual number of bytes transferred after the command is completed. With operation codes 03H and 04H, the BT-646 will set these bytes to the difference in the data length originally specified by the host and the actual data length (number of bytes) transferred across the SCSI bus. With operation code 04H the original data length is the segment data length's sum.
7–9	Data Pointer	Specify the real address of the first byte of the data area to be used during the data phase of a SCSI command. If a scatter-gather operation is specified by the CCB, the Data Pointer field contains the pointer to the first byte in the Data Segment List.
10–12	Link Pointer	Used when a Link or Link With Tag bit is set in a SCSI command. Upon completion of a linked command, the BT-646 uses the contents of this field as a pointer to the next CCB to execute. If the Linked Flag bit is set, an interrupt will be generated before the next command is begun. A completed CCB is always reported back in an incoming mailbox. However, Incoming Mailbox interrupts (IMBL) are only reported if the linked set of commands is finished or if a Link with Flag message is presented. There must be enough incoming mailbox entries to receive the entire set of linked commands. NOT SUPPORTED IN TARGET MODE.
13	Command Linking Identifier	Used in conjunction with linked commands. Set by the host to identify commands in a command chain. NOT SUPPORTED IN TARGET MODE.
14	Btstat	BT-646 status reported to the host.
	Hex Value	
	00	CCB completed normally with no errors.
	0A	Linked command completed with no errors. The SCSI command was completed and linked with no errors.
	0B	Linked command was completed with no errors and an interrupt was generated. The SCSI command was completed and was linked with a LINKED COMMAND COMPLETE WITH FLAG message.
	11	SCSI Selection time out. Initiator selection or target reselection did not complete within the set SCSI selection time-out period.
	12	Data over run/under run. The target attempted to transfer more or less data than was allocated by the Data Length field or the sum of the Scatter-Gather Data Length fields.
	13	Unexpected bus free.
	14	An invalid bus phase or sequence was requested by the target. The BT-646 generated a SCSI Reset state, notifying the host with a SCSI Reset State interrupt (RSTS).

COMMAND CONTROL BLOCK FIELD DEFINITIONS (Continued)

BYTE	FIELD	DESCRIPTION
	15	Invalid action code in Byte 0 of the outgoing mailbox.
	16	Invalid operation code in Byte 0 of the CCB.
	17	Linked CCB does not have the same LUN as the first CCB.
	18	Invalid target direction in a target mode CCB.
	19	Duplicate CCB received in target mode.
	1A	Invalid parameter in CCB or segment list.
	1B	Auto request sense failed.
	1C	SCSI-2 tagged queueing message was rejected by the target.
	20	The host adapter hardware failed.
	21	The target did not respond to SCSI ATN and the host adapter consequently issued a SCSI bus reset to clear up the failure.
	22	The host adapter asserted a SCSI bus reset.
	23	Other SCSI devices asserted a SCSI bus reset.
15	SDSTAT	SCSI Device Status. If the BT-646 is the initiator, the target will send a status byte to the BT-646 at the termination of each SCSI command. The BT-646 places that status code in this byte of the CCB to report it to the host. If a Busy status is returned in the SCSI command, the command is executed a second time. The BT-646 requeues the command and automatically restarts it until the command completes with a status other than Busy. If the BT-646 is in target mode, it will send a status byte to the initiator at the termination of each SCSI command. The BT-646 also places that code in this byte of the CCB to inform the host what code is sent to the initiator. Status codes reported to the initiator by the target and reported to the host in this byte may have the following values: **Hex Value — Status Meaning** 00 — Good 02 — Check Condition. See CCB Byte 3 discussion of Request Sense in response to Check Condition. 08 — Busy
16–17	Reserved	Must be set to zero.
18–n	SCSI Command Descriptor Block	Contains the SCSI CDB Its length is defined in CCB Byte 2. For initiator CCB's, the CDB provided by the host is transmitted to the target. As for target mode CCB's, the CDB provided from the initiator is returned to the host in this area of the CCB.
n–m	Sense Data	If the BT-646 detects a Check Condition status once an operation is completed on the SCSI bus, it automatically executes a Request Sense command with the number of bytes specified by the Request Sense Allocation Length in CCB Byte 3. The bytes returned, up to the maximum indicated by the Request Sense Allocation Length, are placed in this area. If the BT-646 is operating in target mode, when a Check condition is detected by the BT-646, the same information that will later be recovered by the initiator that received the Check Condition status is placed in this area to inform the host of the failure.

In normal CCB operations using SCSI Initiator (00H) and SCSI Target (01H) codes, the CCB contains the pointer (CCB, Bytes 7-9) to the first byte of a contiguous area of data of a specified length (CCB, Bytes 4-6).

Unlike the preceding operation codes, the SCSI initiator with Scatter-Gather code (02H) uses CCB, Bytes 7-9 as a pointer to a list of data segments to be transferred. Bytes 4-6 in the CCB specify the length of the Data Segment List. Each entry in the list contains a three-byte field specifying the length of a data segment and a second three-byte field containing a 24-bit address which points to the corresponding data segment in host memory. The Data Segment List is arranged in the order in which data is to be "gathered" or "scattered". The first entry in the list, pointed to by the Data Segment List Pointer in CCB Bytes 7-9, will be used first. A Data Segment List can identify up to 8,192 separate segments of memory. An invalid Data Segment List error will be posted in the Btstat field (1AH) if a list contains zero or more than 8,192 segments.

The structure of the Data Segment List is as follows:

	3 Bytes		3 Bytes	
	MSB	LSB	MSB	LSB
Data Segment List Pointer →	Segment 0 Byte Count		**Segment 0 Data Pointer**	
	Segment 1 Byte Count		**Segment 1 Data Pointer**	
	Segment 2 Byte Count		**Segment 2 Data Pointer**	
	Segment 3 Byte Count		**Segment 3 Data Pointer**	
	Segment 4 Byte Count		**Segment 4 Data Pointer**	

Figure 5-2. Scatter-Gather

The BT-646 places **no** restrictions on the data segment address boundaries and lengths that are allowed. For information on 32-bit memory addressing, refer to Appendix B.

Programmer's Note: *To enhance performance, it is recommended that all starting addresses (mailboxes, CCBs and data pointers) be on 32-bit (double-word) boundaries and that all transfer byte counts be a multiple of four. If an error occurs during execution of a Scatter-Gather command, the entire command must be retried. It is not possible to determine which segment produced the error.*

Micro Channel compatible systems provide for a Basic Input/Output System (BIOS) interface in ROM on the system motherboard or on I/O option boards. These BIOS ROMs contain programs which control communication between the Disk Operating System (DOS) and the corresponding I/O peripheral device. Access to each BIOS occurs through a software interrupt of the host CPU. In the case of a hard disk, the software interrupt is Interrupt 13H.

On a standard Micro Channel system, the motherboard BIOS includes support for up to two device-level interfaced hard disks. The BIOS on the BT-646 provides equivalent support for up to two SCSI hard disks by intercepting the Interrupt 13H call and by responding to its SCSI device IDs. Control of any additional hard disk drives requires the use of a software driver using mailbox commands.

If two standard hard disks are present in a Micro Channel system, the BT-646's BIOS cannot support additional SCSI drives without a software driver. If no standard hard disks are installed, the BT-646's BIOS can support up to two SCSI hard disks. In this case, Drive 0 (C:) is Device 0, LUN0. Drive 1 (D:) is SCSI Device 1, LUN0. Booting can only be done from SCSI Device 0, LUN0.

If one standard hard disk is installed, it is accessed as Drive 0 (C:). The system may be booted only from this internal hard disk. One SCSI hard disk may be concurrently supported by the BT-646. Its identity is Device 0, LUN0 (D:).

Parameters required to execute commands associated with the control of the hard disks are transferred to and from the BIOS program routines with the use of the host CPU's general registers and segment registers. This interface is capable only with single-threaded operation.

The BT-646's BIOS can accept functions from the MS-DOS operating system that are required for normal operation, system booting, basic maintenance and verification functions.

The BT-646 is notified by its on-board BIOS when Interrupt 13H operations are in process by the Start BIOS host adapter command (03H). The BT-646 will not respond properly to the Start BIOS command if it is issued by any other source than the on-board BIOS.

BIOS Commands and Input Parameters

The BIOS command code is passed to the BT-646 through the CPU's Register AH. The drive number is provided to the BT-646 through the CPU's Register DL. The drive number for each command will be 80H or 81H. Refer to the following table for a summary of valid BIOS disk functions. Other input parameters required by the BT-646 to execute some of these commands will be described following the table.

Valid BT-646 BIOS Disk Functions

Command Code in AH Register (Hex Value)	Command	Description
00	Reset Disk System	The BIOS issues a reset to the SCSI bus.It then sends this command on to the standard Micro Channel BIOS so it can reset other floppy or hard disks in the system.
01	Read Status of Last Operation	The BT-646 reports the status of the last operation performed by the specified disk. No SCSI activity occurs and the disk status is reset to zero.
02	Read Desired Sectors Into Memory	The requested sectors, defined by the input parameters, are read from the disk to the system memory. This function maps to a SCSI Read command (SCSI Opcode 08).
03	Write Desired Sectors From Memory	The requested sectors, defined by the input parameters, are written from the system memory to the indicated disk. This function maps to a SCSI Write command (SCSI Opcode 0A).
04	Verify Desired Sectors	The requested sectors, defined by the input parameters, are verified to be written correctly on the SCSI disk. This function maps to a SCSI Verify Command (SCSI Opcode 2F). In some special cases, for targets that do not support the 2F command, this function maps to a SCSI Read command (SCSI Opcode 08) and discards the received data.
06	Identify SCSI Devices	This command is used to determine the number of the first SCSI drive attached to the BT-646.
08	Read Drive Parameters	This function maps to a SCSI Read Capacity command (SCSI Opcode 25). The total logical capacity is then converted to pseudo-physical parameters.
09	Initialize Drive Pair Characteristics	Because SCSI CCS drives are self-configuring, this command performs no operation.
0C	Seek	This function performs a Seek command (SCSI Opcode 0B) to the logical block address as defined by the physical parameters. This command is not required for CCS commands nor for proper SCSI device operations. Because the Seek operation is performed automatically by the Read and Write operations, it is not necessary to generate a Seek command to access data.
0D	Alternate Disk Reset	The BIOS sends a SCSI bus reset to the target specified in the DL Register. A reset function request is also passed to the system's BIOS so that any internally installed hard or floppy disk(s) can be reset.
10	Test Drive Ready	This function maps to a SCSI Test Unit Ready command (SCSI Opcode 00). After executing a Reset function, the BT-646's BIOS issues this function internally until the Target is no longer busy and the Unit Attention condition is cleared.
11	Recalibrate	This function maps to a Re-zero Unit command (SCSI Opcode 01).

Valid BT-646 BIOS Disk Functions Continued

15	Read DASD Type	The BIOS of the BT-646 checks the Peripheral Device Type Qualifier (returned by the SCSI Inquiry command) to verify that the device is a Direct Access Device. The BIOS then returns the logical capacity reported by the SCSI Read Capacity command in the CX and DX Registers.

Additional input parameters are required by the Read (02H), Write (03H) and Verify (04H) BIOS commands and are supplied in the following registers:

CPU Register	Input Parameter
AL	Number of Sectors
CH	Low-Order Byte of the Cylinder Number
CL	Cylinder and Sector Numbers Bits 7 and 6: High-Order Cylinder Bits Bits 5 to 0: Sector Number
DH	Head number
DL	Drive Number
ES:BX	Address of Data Buffer Area

The Seek BIOS command (0C) requires only the cylinder and head numbers from Registers CL, CH and DH. In this case, the sector number bits in Register CL are zero.

The physical starting disk address provided in the preceding registers is converted by the BT-646's BIOS into a logical block address before being sent to the designated SCSI device. The physical address consists of 10 bits to specify up to 1024 cylinders, 8 bits to specify up to 64 heads and 6 bits to specify up to 32 sectors. These bits are combined to form a 21-bit logical block address for the SCSI drive as follows:

Physical Cylinder Number	Physical Head Number	Physical Sector number-1
10 bits	6 bits	5 bits

21-bit Logical Block Address

BIOS Command Completion Status

When the BT-646 has completed the BIOS command, control is returned to the requesting program at the next instruction after the software Interrupt 13H.

The BT-646's BIOS places a completion code in the Carry Flag (CF). If CF is zero, the BIOS command was completed normally and there is no additional status to report. If CF is set to one, normal command completion did not occur and a non-zero status byte will be placed into the CPU's Register AH by the BT-646. This status byte is to be interpreted as follows:

Completion Status Byte Hex Value	Meaning	Hex Sense Code Returned To The BT-646 From The Request Sense Command
00	No error. Normal Completion.	
01	Invalid Command Request	
02	Address Mark Not Found	12–No AM Found on Disk 21–Illegal Logical Block Address
03	Write Protect Error	27–Write Protected
04	Read Error	14–No Record Found 16–Data Sync Error
10	Uncorrectable ECC Error	10–ID ECC Error 11–Unrecovered Read Error
11	ECC Corrected Data Error	17–Recovered Read Error w/o ECC 18–Recovered Read Error w/ ECC
20	Controller Failure or one of many Additional Sense Codes was returned	01 03 05 06 07 08 09 1B 1C 1D 40-49
40	Seek Operation Failed	15–Seek Positioning Error 02–No Seek Complete
80	Selection Time-Out	Drive did not respond to host adapter
AA	Device Not Ready	04–LUN Not Ready 28–Medium Changed 29–Power On or Reset or Bus Device Reset Occurred 2A–Mode Select Parameter Changed
BB	Unknown Target Sense Error	Unknown Additional Sense Code from SCSI Device
FF	Sense Operation Failed	No sense information from

Additional output parameters are required by three BIOS commands and are supplied in the following CPU registers:

Command (HEX)	CPU Register	Output Parameter
06 Identify SCSI Devices	AL	Drive Number of First SCSI Drive Attached 80 if no standard hard disk 81 if one standard hard disk
08 Read Drive Parameters	DL	Number of SCSI Drives Attached
	DH	Max value for head number (3F)
	CH	Max value for Cylinder Range (Low Byte)
	CL	Max value for Sector and Cylinder Bits 7-6 High Order Cylinder Bits Bits 5-0 Max Sector Number (20)
15 Read DASD	AH	Status of Operation 00 Drive not present or DL invalid 01 Reserved 02 Reserved 03 Fixed Disk installed
	CX,DX	Number of 512 byte blocks available on disk

The BT-646's BIOS can accept functions from the MS-DOS operating system that are required for normal operation, system booting, and normal disk operation, basic maintenance and verification functions. Refer to the following table for a summary of valid BIOS disk functions. Detailed explanations of the operation of each BIOS command follow the table.

Valid BIOS Disk Functions

Command Value in AH Register (Hex Value)	Description
00	Reset Disk System
01	Read Status of Last Operation
02	Read Desired Sectors to Memory
03	Write Desired Sectors from Memory
04	Verify Desired Sectors
06	Identify SCSI Devices
08	Read Drive Parameters
09	Initialize Drive Pair Characteristics
0C	Seek
0D	Alternate Disk Reset
10	Test Drive Ready
11	Recalibrate
15	Read DASD Type

In the following descriptions, all references to the SCSI operation codes or parameters input from the host and output back to the host through the various CPU registers are stated in their Hex value for each BIOS command.

00—Reset Disk System. The BIOS issues a reset to the SCSI bus. It then sends this command on to the standard Micro Channel BIOS so it can reset other floppy or hard disks in the system.

Input Parameters: AH=00H
DL=Drive Number (80H or 81H)

Output Parameters: AH=Status of Operation
CF=Return Code

01—Read Status of Last Operation. The BT-646 reports the status of the last operation performed by the specified disk. No SCSI activity occurs and the disk status is reset to zero.

Input Parameters: AH=01
DL=Drive Number (80H or 81H)

Output Parameters: AH=Status of Operation
CF=Completion Code

02—Read Desired Sectors to Memory. The requested sectors, defined by the input parameters, are read from the disk to the system memory. This function maps to a SCSI Read command (SCSI Opcode 08).

Input Parameters:
AH=02H
DL=Drive Number (80H or 81H)
DH=Head Number
CH=Low-order Byte of Cylinder Number
CL=High-cylinder Bit and Sector Numbers
AL=Number of Sectors to Read
ES:BX=Address of Data Buffer Area

Output Parameters:
AH=Status of Operation
CF=Completion Code

03—Write Desired Sectors from Memory. The requested sectors, defined by the input parameters, are written from the system memory to the indicated disk. This function maps to a SCSI Write command (SCSI Opcode 0A).

Input Parameters:
AH=03H
DL=Drive Number (80H or 81H)
DH=Head
CH=Low-order Byte of Cylinder Number
CL=High-cylinder Bit and Sector Numbers
AL=Number of Sectors to Write
ES:BX=Address of Buffer Area

Output Parameters:
AH=Status of Operation
CF=Return Code

04—Verify Desired Sectors. The requested sectors, defined by the input parameters, are verified to be written correctly on the SCSI disk. This function maps to a SCSI Verify command (SCSI Opcode 2F). In some special cases, for targets that do not support the SCSI Verify command, this function maps to a SCSI Read command (SCSI Opcode 08) and discards the received data.

Input Parameters:
AH=04H
DL=Drive Number (80H or 81H)
DH=Head
CH=Low-order Byte of Cylinder Number
CL=High-cylinder Bit and Sector Numbers
AL=Number of Sectors to Verify
ES:BX=Address of Buffer Area

Output Parameters:
AH=Status of Operation
CF=Completion Code

06—Identify SCSI Devices. This command is used to determine the number of the first SCSI drive attached to the BT-646.

Input Parameters: AH=06

Output Parameters: AH=Status of Operation
AL= Drive Number of First SCSI Drive Attached
80H if no standard hard disk
81H if one standard hard disk
CF=Completion Code

08—Read Drive Parameters. This function maps to a SCSI Read Capacity command (SCSI Opcode 25). The total logical capacity is then converted to pseudo-physical parameters.

Input Parameters: AH=08H
DL=Drive Number (80H or 81H)

Output Parameters: AH=Status of Operation
DL=Number of SCSI Drives Attached
DH=Max value for head number (3Fh)
CH=Max value for Cylinder Range (Low Byte)
CL=Max value for Sector and Cylinder
Bits 7-6 High-order Cylinder Bits
Bits 5-0 Max Sector Number (20h)
CF=Completion Code

09—Initialize Drive Pair Characteristics. Because SCSI CCS drives are self-configuring, this command performs no operation.

Input Parameters: AH=09H
DL=Drive Number (80H or 81H)

Output Parameters: AH=Status of Operation
CF=Completion Code

0C—Seek. This function performs a Seek operation (SCSI Opcode 0B) to the logical block address as defined by the physical parameters. This command is not required for CCS commands nor for proper SCSI device operations. Because the Seek operation is performed automatically by the Read and Write operations, it is not necessary to generate a Seek command to access data. If the addressed device reports that the Extended Seek command is not supported, the BIOS command will be completed as normal.

Input Parameters: AH=0CH
DL=Drive Number (80H or 81H)
DH=Head
CH=Cylinder
CL=High Cylinder (Sector bits=0)

Output Parameters: AH=Status of Operation
CF=Completion Code

0D—Alternate Disk Reset. The BIOS sends a SCSI bus reset to the target specified in the DL Register. A reset function request is also passed to the system's BIOS so that any internally installed hard or floppy disk(s) can be reset.

Input Parameters: AH=0DH
DL=Drive Number (80H or 81H)

Output Parameters: AH=Status of Operation
CF=Completion Code

10—Test Unit Ready. This function maps to a SCSI Test Unit Ready command (SCSI Opcode 00). After executing a Reset function, the BT-646's BIOS issues this function internally until the target is no longer busy and the Unit Attention condition is cleared.

Input Parameters: AH=10H
DL=Drive Number (80H or 81H)

Output Parameters: AH=Status of Operation
CF=Completion Code

11—Recalibrate. This function maps to a Re-zero Unit command (SCSI Opcode 01).

Input Parameters: AH=11H
DL=Drive Number (80H or 81H)

Output Parameters: AH=Status of Operation
CF=Completion Code

15—Read DASD. The BIOS of the BT-646 checks the Peripheral Device Type Qualifier (returned by the SCSI Inquiry command) to verify that the device is a Direct Access Device. The BIOS then returns the logical capacity reported by the SCSI Read Capacity command in the CX and DX Registers.

Input Parameters: AH=15H
DL=Drive Number (80H or 81H)

Output Parameters: AH=Status of Operation
- 00 Drive not present or DL invalid
- 01 Reserved
- 02 Reserved
- 03 Fixed Disk installed

CX,DX= Number of 512 byte blocks available on disk
CF=Completion Code

A

BT-646 INTERNAL DIAGNOSTICS

When power is first applied to the BT-646, an on-board diagnostic routine is run to verify that the major functional components of the board are operating correctly. The bus master chip, the SCSI controller chip, the firmware PROM, the local RAM and internal data buses are tested. Results of the tests are indicated by an LED on the board.

The LED will first turn on when power is applied. If the diagnostics find no malfunctions, the LED will then go off. In normal operation, the LED will be illuminated when command or SCSI bus activity occurs on the board.

If an error is detected by the diagnostics, the LED will repeatedly flash a specific number of times, with a long pause between flashes, to indicate the board function which failed. This will continue until the board is powered down or reset. Failure interpretation from the number of flashes is as follows:

Number of LED Flashes	**Interpretation of Failure**
Always On	BT-646 is not operating or terminators are missing
1	Firmware ROM checksum failure
2	Local RAM test failure
3	SCSI controller chip or SCSI interface failure
4	Internal data bus failure
5	Internal address bus failure
6	Bus master chip failure
7	SCSI drive type mismatch*
Constantly Flashing	Fuse Blown.

*This error message is applicable to the BT-646 when single-ended SCSI drives are connected to the differential SCSI bus.

B

32-BIT MODE ADDRESSING

PURPOSE

As originally designed, the host interface of the BT-646 uses a superset of the register set and command protocol in the AHA-1646 PC/AT host adapter. This interface is currently supported by many popular operating systems. The command mailbox structure provides for a memory address of 24 bits that permits direct addressing of only 16 MBytes of memory. Such a memory limit is often too constraining in advanced, high performance Micro Channel systems designed for multiple processors and multi-tasking operations. This document describes a method for implementing a 32-bit memory addressing capability in the BT-646 that will provide unrestricted access to more than 4 Gigabytes of memory.

DESCRIPTION

In the present design, a four-byte Initialize Mailbox command is issued by the host to the BT-646. One byte of this command specifies the number of mailboxes to be used by the host adapter and three bytes specify the base memory address (24 bits) of the array of mailboxes in the main memory that will contain the Command Control Blocks (CCBs) during normal data transfer operation.

An extended address mode allowing 32-bit addressing can be implemented as follows:

Use the host adapter command 81H to send the host adapter a new command called **Initialize Extended Mailbox**. This command is just like the original **Initialize Mailbox** command except that it sends a one-byte mailbox count followed by a four-byte, 32-bit address pointing to the first mailbox located anywhere within the 4 Gigabyte memory range. The description of the bytes is as follows:

Byte	Description	
0	Mailbox count	(Greater than 0)
1	Base Mailbox Address	(LSB)
2	Base Mailbox Address	
3	Base Mailbox Address	
4	Base Mailbox Address	(MSB)

The software driver may return the host adapter to the original 24-bit address mode using old data structures by issuing the Initialize Mailbox command (01H).

NEW MAILBOX STRUCTURE

Communication between the host and the host adapter is coordinated by the use of outgoing and incoming mailboxes. These mailboxes contain control and status information, and address pointers to CCBs that contain the details of each SCSI command to be processed. The mailbox structures have been changed to the following format:

OUTGOING MAILBOXES

Byte 0	Byte 1	Byte 2	Byte 3
LSB	32-Bit CCB	Pointer	MSB
Reserved	Reserved	Reserved	Action Code
Byte 4	Byte 5	Byte 6	Byte 7

Valid Action Codes are as follows:

Hex Value	Definition
00	Outgoing mailbox is not in use
01	Start a mailbox command
02	Abort a mailbox command.

INCOMING MAILBOXES

Byte 0	Byte 1	Byte 2	Byte 3
LSB	32-Bit CCB	Pointer	MSB
BTSTAT	SDSTAT	Reserved	Completion Code
Byte 4	Byte 5	Byte 6	Byte 7

Valid Completion Codes are as follows:

Hex Value	Definition
00	Incoming mailbox is not in use
01	CCB completed without error
02	CCB aborted at request of host
03	Aborted CCB not found
04	CCB completed with error.

NEW CCB STRUCTURE

Byte	Description
0	Operation Code
1	Data Direction Control
2	Length of CDB
3	Length of Sense Area
4	LSB
5	Data
6	Length
7	MSB
8	LSB
9	Data
10	Pointer
11	MSB
12	Reserved
13	Reserved
14	BTSTAT
15	SDSTAT
16	Target ID
17	LUN & Tag
18-29	Command Descriptor Block (12 Bytes)
30	CCB Control
31	Link ID
32	LSB
33	Link
34	Pointer
35	MSB
36	LSB
37	Sense
38	Pointer
39	MSB

Note: *In the extended address mode, Bits 3 and 4 of Byte 1 (the Data Direction Control byte) are used as in standard mode. Bits 0-2 and 5-7, however, are reserved in extended mode.*

Note that all reserved bytes and bits should always be set to zero.

Many fields of this new CCB are identical to the original CCB. Data address fields have been expanded to four-byte fields to contain full 32-bit address pointers. The byte order has been reversed, with the LSB coming first rather than the MSB. To enhance symmetry, the Data Length field has been expanded to four bytes as well.

The BTSTAT (BT-646 status) field contains host adapter status information at the completion of a SCSI command. In this new proposal, the contents of this field are written by the host adapter into the incoming mailbox as well as back into the CCB in the main memory to give the host the option of not having to access the CCB again for completion status.

The SDSTAT (SCSI device status) field contains status information from the target SCSI device at the completion of the SCSI command. In this new proposal, the contents of this field are written by the host adapter into the incoming mailbox as well as back into the CCB in the main memory to give the host the option of not having to access the CCB again for completion status.

Target ID and LUN numbers have been given their own bytes rather than having to share a byte with specification of data direction and length checking in Byte 1 of the CCB.

A Sense Pointer has been included. This offers the option of allocating a storage area anywhere in the main memory for the information returned in response to a Request Sense command. One option is to have the Sense Pointer point to the bytes immediately following itself at the end of the CCB. Refer to the following table for a description of the byte or field in this new CCB.

COMMAND CONTROL BLOCK FIELD DEFINITIONS

BYTE	FIELD	DESCRIPTION
14	BTSTAT	New status available.

Value	Description
1B	Auto Request Sense failed.
1C	A SCSI II Tagged Queuing message was rejected by the Target.
20	The host adapter hardware failed.
21	The Target did not respond to SCSI ATN so the host adapter issued a SCSI RST to clear up the failure.
22	The host adapter asserted SCSI RST.
23	Other SCSI devices asserted SCSI RST.
24	The target device reconnected improperly (without tag). An Abort message was issued.
25	The host adapter issued BUS DEVICE RESET.
26	Abort Queue generated.

COMMAND CONTROL BLOCK FIELD DEFINITIONS (Continued)

BYTE	FIELD	DESCRIPTION
17	Logical Unit Number (LUN) and Tag	
	Bits 2-0	Specifies the Logical Unit Number (LUN).
	Bits 4-3	Reserved.
	Bit 5	Tag enable. When this bit is set, the host adapter will support the tag queueing feature according to the SCSI-2 specifications. When this bit is reset, the host adapter will not support this feature.
	6,7	Specifies the tag type. These two bits have no meaning if bit 5 (the Tag Enable bit) is not set. When bit 5 is set, bits 6 and 7 have the following meaning:

Bit 7	Bit 6	Message to be sent to the target after IDENTIFY
0	0	Simple Queue Tag (20H) + Unique Tag ID
0	1	Head of Queue Tag (21H) + Unique Tag ID
1	0	Ordered Queue Tag (22H) + Unique Tag ID
1	1	Reserved (Do not use this value.)

NOT SUPPORTED IN TARGET MODE.

30 CCB Control

Bit	Name	Description when the bit is set to 1
Bits 2-0		Reserved.
Bit 3	NoDisc	No disconnect. When this bit is set, the host adapter will select the target with IDENTIFY MESSAGE byte value 80H which will disallow the target from disconnecting the current selection. When this bit is reset, the host adapter will act according to the value of the host adapter command 21H's (Set Adapter Options command) Byte 1. If that value is not programmed it will always allow disconnect.
Bit 4	NoUnd	No underrun error report. When this bit is set, the host adapter will not report a data overrun/underrun error (BTSTAT value 12H). If this bit is reset, the host adapter will report a data overrun/underrun error whenever the count of the data transfer between the target and the host differs from the count specified in the CCB data count bytes and/or the combined scatter-gather count. The residual count will be posted in the CCB data counts bytes if the CCB opcode is 03 or 04.
Bit 5	NoData	No data transfer. When this bit is set, the host adapter will not transfer any data between the host adapter and host memory. If this bit is reset, the host adapter will transfer data between the host adapter and host memory.
Bit 6	NoStat	No CCB status if zero. When this bit is set, the host adapter will not update any CCB status byte if the status to be reported is zero. If this bit is reset, all status bytes will be updated. This bit can be used for performance improvement.

COMMAND CONTROL BLOCK FIELD DEFINITIONS (Continued)

BYTE	FIELD	DESCRIPTION		
		Bit	**Name**	**Description when the bit is set to 1**
		Bit 7	NoIntr	No interrupts. When this bit is set, the host adapter will not interrupt the host after a command is completed. If this bit is reset, the host adapter will interrupt the host after a command is completed.
		NOT SUPPORTED IN TARGET MODE		

SCATTER-GATHER OPERATION

Within the current design when a scatter-gather data transfer is performed, the CCB points to a list of the separate data segments involved in the transfer. This list contains a three-byte field specifying the length of each individual data segment and a second three-byte field containing a 24-bit address that points to the corresponding data segment.

With extended addressing, the scatter-gather list must be expanded to pairs of four-byte fields for each data segment in place of the present pairs of three-byte fields. These 32-bit addresses provide unrestricted access to any area of the 4 Gigabyte memory space. The structure of the expanded data segment list is as follows:

Scatter-Gather Data Segment List

	4 Bytes		4 Bytes	
	LSB	**MSB**	**LSB**	**MSB**
CCB Bytes 8-11				
Segment List Pointer —>	Segment 0 Byte Count		Segment 0 Data Pointer	
	Segment 1 Byte Count		Segment 1 Data Pointer	
	Segment 2 Byte Count		Segment 2 Data Pointer	
	Segment 3 Byte Count		Segment 3 Data Pointer	
	Segment 4 Byte Count		Segment 4 Data Pointer	

In the BusLogic implementation of the BT-646, such a data segment list can have from 1 **to 8192 segments**.

COMMAND QUEUING

The BT-646 now supports command queuing. The following are some device driver notes related to command queuing.

1. Once a device queues up Tag Queue commands, the Initiator should not issue a Non-Tag Queue command (with the exception of Contingent Allegiance condition) until all queued commands have been processed. Therefore, avoid mixing Tag Queue commands with Non-Tag Queue commands.

2. If a CCB is aborted in a Tag queue environment, the host adapter can no longer issue an Abort message to the target. It will have to wait until the Target reestablishes the I_T_L_Q NEXUS. Consequently, it is recommended that a CCB not be aborted in a Tag Queue environment.

3. When a Bus Device Reset is issued, the Target will flush all queued I/O commands. Consequently, the host adapter must return SCSI Reset status for all the CCBs sent to the Target.

4. When a SCSI Bus Reset is issued, all Targets will flush all queued I/O commands. Note that the host adapter will flush all existing TCB in the Disconnect TCB Link List and the Abort TCB Link List. Consequently, the host adapter must return SCSI Reset status for all the CCBs sent out.

5. If there are any outstanding Tag Queue commands and a Target attempts to reconnect without a Tag message, the host adapter will generate an Abort message. The host adapter will flush all outstanding CCBs sent to that Target. All these CCBs will be returned to the host with Host Adapter Status 24H. Refer to the description of the BTSTAT field in this appendix for new host adapter status.

6. Because a Tag message must be sent right after an ID message, synchronous transfer negotiation initiated by the Initiator takes precedence over a Tag Queue message. This is because most devices that support Tag Queuing may not be able to handle an ID message, followed by a Tag Message, followed by a Synchronous Transfer Negotiations message .

   Consequently, it is recommended that the first couple of commands be sent in Non-tag Queue fashion. This will allow the host adapter and Target to establish Synchronous Transfer mode after each Reset condition.

7. The Auto Sense capability is a useful feature that can be enabled or disabled. If Auto Sense is enabled and a Contingent Allegiance condition occurs, the host adapter will issue a Request Sense command. When a Request Sense command is issued, the Contingent Allegiance condition will be cleared and the Target can continue processing the queued commands.

   When Auto Sense is disabled, the host can deal with the Contingent Allegiance condition itself and decide which recovery procedure to use.

IMPLEMENTATION REQUIREMENTS

Existing drivers must be modified to issue the Initialize Extended Mailbox command and to set up the new mailbox and CCB structures. To support scatter-gather transfers an expanded scatter-gather list structure must be provided.

BT-646 firmware will be modified to recognize the Initialize Extended Mailbox command to find the designated section of memory where the CCBs will be located. It will then recognize the specified 32-bit data pointer in each CCB when performing DMA data transfers and the expanded scatter-gather list.

PROJECT RELATIONSHIP

BusLogic will be pleased to work closely with the software supplier or customer in planning and implementing this extended addressing concept that will enhance SCSI data storage capacities on Micro Channel systems.

C

A List of Acronyms

BIOS	Basic Input/Output System
CCB	Command Control Block
CCS	Common Command Set
CDB	Command Descriptor Block
CPU	Central Processing Unit
DMA	Direct Memory Access
DRAM	Dynamic Random-Access Memory
FCC	Federal Communications Commission
FIFO	First-In First-Out
I/O	Input/Output
ISA	Industry Standard Architecture
LSB	Least Significant Bit
LU	Logical Unit
LUN	Logical Unit Number
MPU	Microprocessor Unit
MSB	Most Significant Bit
PCB	Personal Computer Board
POS	Programmable Option Select
PROM	Programmable Read-Only Memory
RAM	Random-Access Memory
RFI/EMI	Radio Frequency Interference/Electromagnetic Interference
ROM	Read-Only Memory
SCSI	Small Computer System Interface
SCSI ID	Small Computer System Interface Identification

Class B Equipment

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio or television technician for help.

Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by BusLogic Inc. may void the user's authority to operate the equipment.

Cables

Connections to this device must be made with shielded cables with metallic RFI/EMI connector hoods in order to maintain compliance with FCC Rules and Regulations.

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