BiiN 60™ System
Technical Overview

BiiN™

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The BiiN 60™ system, the high-end member of the BiiN family of computers, offers a wide range of computational and transaction processing capabilities. Featuring symmetric multiprocessing, the BiiN 60 can be sized to fit current application needs and extended in processing power, memory, and I/O bandwidth as application requirements expand. For instance, more compute power is attained simply by adding processors, without any application software changes. By adding peripheral extension towers, disk mass storage capacities of over 40G bytes per disk channel are available. These configuration changes are completely transparent to users.

The BiiN 60™ system uses the extensible, multi-user, multitasking BiiN™ Operating System (BiiN/OS™) executive to provide reliable multiprocessing and secure distributed computing. The BiiN 60 provides a complete software support environment for fast program development, including five high-level languages, a complete set of programming tools, and a powerful relational database.

The BiiN 60™ system was designed to meet all of the stringent requirements of mission-critical computing, on-line transaction processing, and real-time applications.

- **Hardware-Implemented Symmetric Multiprocessing:** Multiple processors access a common memory and automatically share a common workload for higher throughput.
- **Hardware-Implemented Fault Tolerance:** Hardware automatically detects errors, reports faults, and recovers from errors, totally transparent to applications.
- **Dynamically Selectable Levels of Fault Tolerance:** Replication of hardware modules is the technique used to expand throughput and increase levels of fault tolerance. BiiN/OS configures modules for three levels of fault tolerance.
- **Stable-Store Memory for High-Performance Transaction Processing:** Highly reliable battery backed-up memory is used as a file cache to reduce both disk reads and writes.
- **Fine-Grained Protection for Security and Reliability:** VLSI-implemented object addressing promotes increased security and software reliability without sacrificing performance.
- **Expandable High-Speed I/O:** Specially designed intelligent channel processor is capable of transfers of up to 32M bytes per second and handles a variety of peripherals and communication interfaces.
- **Adherence to Industry Standards:** The BiiN 60™ system conforms to industry-recognized standards to connect to commonly available peripheral devices.
- **Built-in Error Monitoring and Diagnostic System:** Special circuitry monitors environmental conditions and voltage levels to ensure proper operating conditions at all times.
- **Software Compatibility:** Application programs can be run on any BiiN system without recompilation or relinking.

Symmetric Multiprocessing Architecture Provides Scalability from Mini to Mainframe

All processors and I/O channels directly access a common shared memory for powerful, expandable symmetric multiprocessing. This capability allows the BiiN 60 to expand easily as application needs change, preserving original hardware and software investments. Memory, I/O, and processing power are all extensible simply by adding the appropriate boards to the BiiN 60. This approach requires no software changes or complex system performance analysis and tuning as the number of processors changes. In addition, concurrent programming is made easier and more efficient by using shared memory.

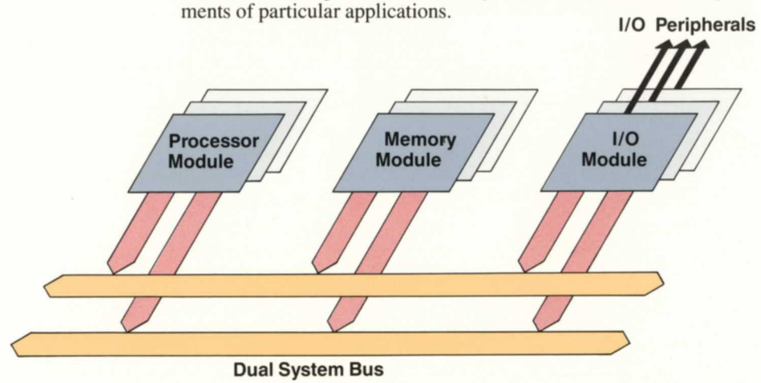
To achieve efficient symmetric multiprocessing and concurrent programming, key facilities were designed into the VLSI processor and BiiN/OS. The processor implements low-level scheduling functions based on parameters set by the high-level BiiN/OS scheduler. Interprocess synchronization and communication are integrated with the processor scheduling, so that the processor can block one process and schedule another without BiiN/OS intervention. All processors in the computer share a queue of ready-to-run processes to automatically balance the workload.

Other features of the BiiN architecture include floating-point processing, independent I/O processing, and high data integrity. Fine-grained protection and reliability are achieved through an object-addressing mechanism that allow software modules to be grouped into a protected address space, accessible only through defined interfaces.

VLSI-Based Modules Offer Wide Range of Performance and Capabilities

The BiiN architecture divides the system into three basic modules: processor, memory, and I/O. These modules, connected by a dual system bus, can be replicated to offer a wide range of CPU, memory, and I/O performance, as shown in Figure 1. Moreover, these modules can be configured in several ways to meet the individual requirements of particular applications.

Figure 1: BiiN Modular, Extensible System Architecture



BiiN uses a comprehensive VLSI approach to build a balanced and modular computer architecture. BiiN implemented a separate VLSI component for each of the four functional blocks of a computer: processor, memory, bus, and I/O. The processor module uses the CPU for the computational engine and the Bus Exchange Unit (BXU) for the bus interface. The memory module uses the Memory Control Unit (MCU) for a memory controller and bus interface. The I/O module uses the Channel Processor (CP) as the I/O engine and the BXU for the bus interface. These components, specifically designed to implement the BiiN architecture, provide expansion of throughput by adding processor, memory, and I/O modules.

Implementing the BiiN architecture in VLSI reduces total chip count and interconnections to enhance system reliability. Because the probability of a component failure cannot be reduced to zero, BiiN provides fault-tolerant computing through VLSI replication.

Software Dynamically Selects the Level of Fault Tolerance for Optimum Flexibility

The BiiN 60 supports three levels of fault tolerance: standard, fault-checking, and continuous operation. The standard configuration provides several functions that contribute to high reliability. These include a processor self-test, integrity tests, single-bit memory error correction (ECC), spare-bit replacement, and retry mechanism for bus errors. The fault-checking level pairs modules to detect hardware errors. If a non-recoverable error occurs, processing stops to prevent corruption. The failed module is then excluded in the subsequent, automatic re-initialization of the computer. The continuous-operation level duplicates fault-checking module pairs, such that if a permanent error occurs, the faulty module is immediately replaced by its partner, without impacting program execution.

At the direction of the system administrator, BiiN/OS dynamically configures modules to function in lockstep providing levels of fault tolerance, or to function independently providing levels of throughput. For example, BiiN/OS can initially configure eight processor modules to act as two processors in continuous operation, or as four processors in fault-checking operation, or as eight processors in the standard configuration. The system administrator can change the level of fault tolerance while the computer is operating. For example, the BiiN 60 can be configured for continuous operation during the day to handle critical on-line activities, and configured for fault-checking operation at night to handle back-office activities at twice the processing throughput. Both the level of fault tolerance and switching between different levels are transparent to applications.

Dual, High-Speed, Packetized System Bus Efficiently Handles Independent Operations

The BiiN 60 employs two identical, yet independent buses to provide fast, efficient memory access for the processor and I/O modules. Each bus is a synchronous, packetized bus that contains 32 multiplexed address/data lines and control lines, such as arbitration, clock and error signals. Designed to maximize throughput in a multiprocessing environment, each bus handles different requests from the processor and provides a message passing facility for processor-to-processor or processor-to-CP communications.

Each bus provides an effective bandwidth of 40M bytes per second by implementing three techniques: burst transfers, packetizing, and memory interleaving. Burst transfers allow a packet from 1 to 16 bytes of information to be transferred in one bus transaction to minimize the number of memory accesses. Packetizing divides bus operations into request and reply packets to maximize bus usage. For example, the bus can handle another request while waiting for a reply from the previous request. The bus handles up to three outstanding request packets and supports memory interleaving on 16-byte boundaries.

The BiiN 60 uses two buses to provide a total effective bus bandwidth of 80M bytes per second, with up to six memory requests in progress at the same time. By interleaving the requests on 16-byte boundaries, the bus controllers (BXUs and MCUs) assure even distribution over the two buses.

The dual buses provide high data integrity and fault tolerance. The bus controllers perform parity checks on the data, address, and other signal transmissions. If a parity error is detected, the retry mechanism automatically performs the operation again. If an error occurs on the retry operation, the error is classified as permanent. In this case, the bus controllers immediately and automatically switch bus traffic from the failed bus to the remaining functional bus, completely transparent to software. After the switchover is complete, hardware asynchronously notifies BiiN/OS of the error and bus switch.

High Performance Processor Module Features Advanced 32-bit CPU and High-Speed Cache

The processor module performs all the computational and data processing tasks for the system. Each processor module represents an independent processing unit that shares the system's computational load and system memory. In the standard configuration, two processor modules are contained on one BiiN 60 processor board, as shown in Figure 2.

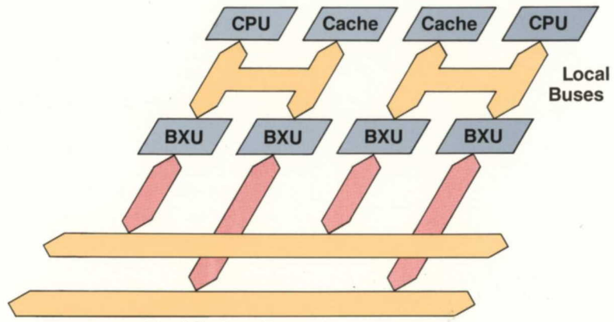


Figure 2: Simplified Block Diagram of the Processor Board

The advanced 32-bit BiiN CPU incorporates not only many Reduced Instruction Set Computer (RISC) principles for computational performance, but also key data processing capabilities found in established architectures. The key data processing capabilities include the ability to access operands on any byte boundary and instructions for block data movement. To minimize component count and maximize performance, the CPU implements virtual address translation, floating-point operations, and a 512-byte instruction cache. The physical address space of the CPU is 4G bytes, and the virtual address space is 2^{58} bytes.

The CPU incorporates several performance features that are typical of RISC architectures, such as a large register set (16 local, 16 global, and four 80-bit floating-point registers) and an on-chip register cache that stores four sets of local registers for implementing a high-performance subprogram call/return mechanism. When memory access is necessary, the CPU can perform burst transactions that access up to four data words, with one word transferred per system clock cycle.

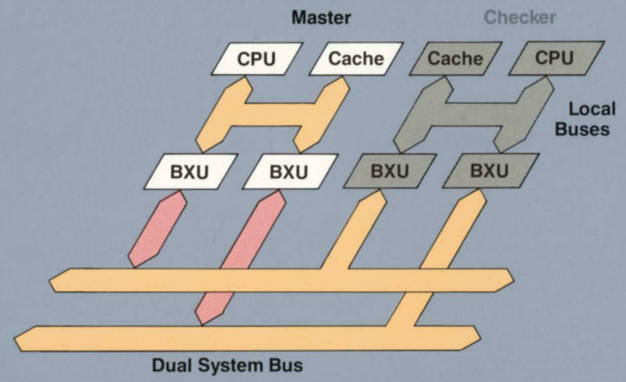
The CPU employs several other design techniques to enhance performance. The CPU overlaps memory accesses with computational operations using two mechanisms: write buffering and register scoreboarding. Write buffering allows a STORE instruction to complete execution as soon as the operand is transferred to the on-chip write buffer. Register scoreboarding permits instruction execution to continue while data is being fetched. These two mechanisms reduce the effect of memory latency and optimize execution speed. In addition, the CPU uses simple instruction formats to speed decoding of instructions. Many frequently used instructions are executed during single clock cycles, permitting maximum processor speed.

The BiiN CPU Takes a Step Beyond RISC

The BiiN CPU takes a step beyond RISC and traditional architectures by providing support for system functions, such as symmetric multiprocessing, object-oriented computing, and multitasking. Although many computer systems support symmetric multiprocessing, only the BiiN CPU embeds operating system mechanisms in VLSI to increase the efficiency and throughput of a multiprocessor system. Similarly, the BiiN CPU implements object addressing as the enabling technology for making BiiN/OS extensible, reliable, and secure, without sacrificing performance.

The processor module includes a write-through cache memory for intermediate storage of data and code fetched from system memory. The BXU contains the cache interface circuitry and maintains complete data coherency among caches on other processor boards. With cache memory, system throughput is enhanced by minimizing accesses to the system bus. The BXU also transfers information between the local bus of the CPU and the system bus, handles the system bus arbitration, and provides fault detection and recovery mechanisms, and interprocessor communication and control.

Figure 3:
One Processor Board Supports Fault-Checking Capability by Forming Master/ Checker Pairs



Fault-Checking Capability of the Processor Module Comprehensively Detects and Confines Errors

In the fault-checking configuration, one BiiN 60 processor board forms one processor module, as shown in Figure 3. Software configures the system for fault-checking capability by pairing BXUs and their associated CPUs to function as a single logical unit, with one operating as a master and the other as a checker. On every clock cycle, the checker compares its internal bus data with the data it actually observes on the system bus, which is driven by its master. The entire logical unit is run in lockstep, executing identical instructions with identical data. The master and checker reverse roles on every clock cycle, alternately driving the bus to detect latent faults and ensure high quality error detection.

If a master/checker pair detects a discrepancy, the bus transaction is tried again to determine whether a transient or permanent error occurred. If the error is transient, normal operation resumes, starting from the last successfully completed transaction. If the error is permanent, normal processing is halted to prevent system corruption, the front panel and board lights are illuminated, and the faulty module is removed from the operating configuration when the system is re-initialized. By distinguishing between transient errors and permanent errors, only truly faulty boards are replaced, saving unneeded service calls.

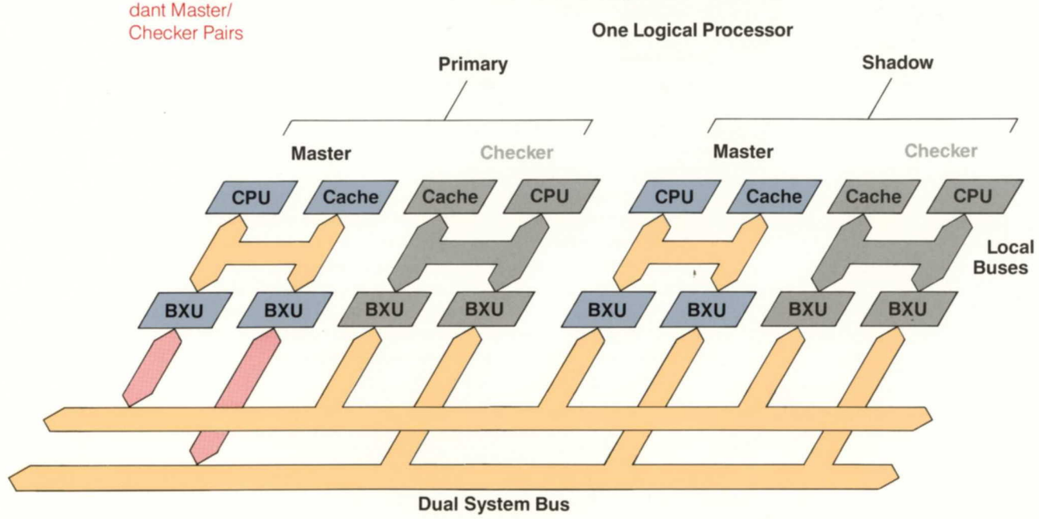
For Continuous Operation, the Processor Module Transparently and Automatically Recovers from Errors

In the continuous-operation configuration, two BiiN 60 processor boards form one logical processor module, as shown in Figure 4. Software configures the system for continuous operation by combining or "marrying" master/checker pairs; one pair is designated as the primary, the other, as the shadow. The shadow master/checker pair operates in lockstep with the primary master/checker pair, with only one BXU driving the system bus at any given time. On every clock cycle, the BXUs rotate roles, alternately driving the system to detect latent faults, as shown in Figure 4. This operation is done automatically without intervention by the CPU.

Similar to fault-checking operation, if a master/checker pair detects a discrepancy, the transaction is tried again to determine whether a transient or permanent error occurred. If the error is transient, normal operation resumes, starting from the last successfully completed transaction. If the error is permanent, the faulty master/checker pair removes itself from operation, and its partner master/checker pair continues to execute the program at normal speeds. Having performed the error detection, error isolation, and recovery (typically within 32 microseconds), the hardware informs the operating system of the event. All errors are logged for later use by service personnel.

These reconfiguration and recovery actions are performed by the hardware without any software intervention or interruption in service. After recovery is complete, system software can make policy decisions regarding the optimum system configuration, given the resources remaining in the system. Policy decisions are carried out while normal system operation continues.

Figure 4:
Two Processor Boards Support Continuous Operation by Providing Redundant Master/ Checker Pairs



Memory Module Provides Reliable Operation with ECC and Spare-Bit Replacement

The BiiN 60 can accommodate multiple memory modules that can be added as needed for up to 80M bytes of total system memory. Each memory module has the following features:

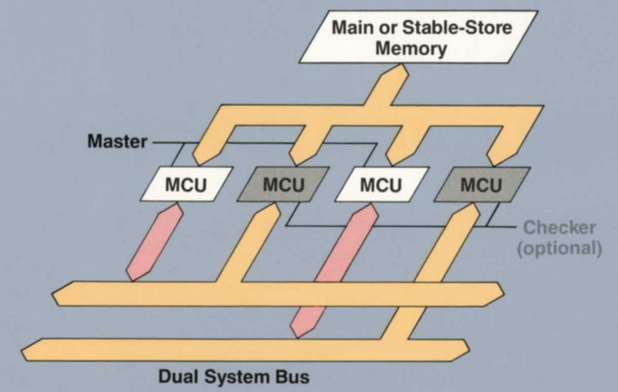
- 8 or 16M bytes of random-access memory per module (with the capability to expand to 32M and 64M bytes with 4M-bit DRAMs)
- Built-in ECC on both data and address lines
- Diagnostic facilities that check ECC logic
- Spare-bit feature for on-line replacement of a failed DRAM component
- Main or stable-store memory configurations

In the standard configuration, one memory module is contained on one BiiN 60 memory board with the optional capability for fault-checking or continuous operation, as shown in Figure 5. The MCU controls the memory array, performs ECC operation, supports memory scrubbing, transfers information between memory and the system bus, handles the system bus arbitration, and provides fault detection and recovery mechanisms. Multiple memory boards can be combined to provide more system memory, and higher throughput can be attained by interleaving memory.

In the fault-checking configuration, one BiiN 60 memory board forms one memory module. Faults are detected by using master/checker MCU pairs and ECC. Similar to the processor module, software configures a memory for fault-checking capability by pairing MCUs to function as a single unit, with one operating as a master and the other as a checker. On every clock cycle, the checker compares its internal bus data with the data it actually observes on the system bus, which is driven by its master. The MCUs run in lockstep, executing identical operations with identical data. The master and checker reverse roles on every clock cycle alternately driving the bus to ensure high quality error detection. The memory array is not duplicated, however, because ECC detects all double-bit errors and corrects all single-bit errors. Moreover, if any single memory component fails, BiiN/OS can configure a spare component in its place without interrupting service.

In the continuous-operation configuration, two BiiN 60 memory boards form one memory module. In this configuration, the contents of the memory array on one board, the primary array, is mirrored on the other board, the shadow array. If the primary array experiences a failure, such as an uncorrectable memory error, the access is automatically switched over to the shadow array, and the primary array is removed from operation, totally transparent to software. After the switchover is complete, hardware asynchronously notifies BiiN/OS of the error and board switch.

Figure 5: Simplified Block Diagram of the Memory Board



File Cache Using Stable-Store Memory is the Key to High-Speed Transaction Processing

The memory board can be configured for stable-store operation. Stable-store memory consists of highly reliable battery-backed memory that retains its contents in the event of a power failure or system crash. For continuous-operation configurations, the stable-store memory is duplicated. The reliability of stable-store memory is comparable to that of a mirrored-disk subsystem because of several BiiN hardware capabilities, such as a high-function memory controller integrated in the MCU, ECC, support for memory scrubbing, the accessibility of both buses, memory mirroring, battery backup, and the option for redundant power supplies. Currently, the BiiN 60 provides up to 16M bytes of high-speed stable-store memory, with the capability to expand to 64M bytes when 4M-bit DRAMs are available.

BiiN/OS uses stable-store memory to implement a file cache, which is the key mechanism for high-speed transaction processing. Other operating systems and database management systems implement a file cache with regular memory to reduce reads to disk. Since the BiiN file cache uses stable-store memory, BiiN/OS can—in addition to reducing disk reads—postpone and eliminate disk writes. Consequently, stable-store memory increases throughput by removing the disk as the I/O bottleneck.

I/O Processor Module Contains Intelligent Channel Processor for High Throughput

The I/O processor module allows a variety of standard peripherals to connect to the system. Operating independently, it performs complex I/O tasks without the need for constant direction from the processor module. In the standard configuration, one I/O module is contained on a BiiN 60 I/O processor board with the option to configure it for fault-checking capability, as shown in Figure 6.

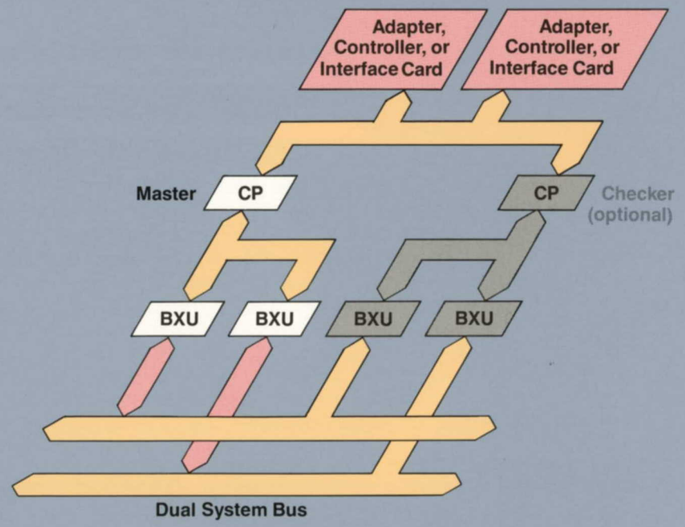


Figure 6: Simplified Block Diagram of I/O Processor Board

The CP, a fully programmable device specially designed for communications and I/O, is capable of transfers of up to 32M bytes per second. Even more importantly, the CP can handle eight I/O tasks concurrently, even if each of the tasks requires a different I/O protocol. This feature allows the CP to move data quickly and efficiently between memory and a variety of peripheral devices. The CP contains a 512-byte register file for buffering data transfers and responds to interrupts with a worst-case latency of 250 nanoseconds. The CP communicates with the CPU using shared memory and interrupts.

The BXUs provide the interface to the dual system bus. To maintain a high data transfer rate, the BXUs can prefetch 64 bytes of data ahead of the CP and store it in an on-chip buffer. Thus, device underruns are effectively eliminated, even when the system bus is heavily utilized. Write-buffering in the BXUs provide the corresponding support and benefit for input data transfers.

The I/O processor board provides access for up to two connections to various adapters, controllers, and interface cards that mount on top of the I/O processor board. These cards offer a host of I/O capabilities, including standard interfaces for mass storage, communications, and networks. These interfaces support a variety of peripheral devices, such as fixed-disk drives, tape drives, terminals, modems, and printers.

The various adapters or controllers include the following:

Model Number	Description
ICA-20	Small Computer System Interface (SCSI) Adapter
ICA-25	Intelligent Peripheral Interface (IPI-3) Adapter
ICA-30	Two-Line High-Speed RS-422 Interface with the capability of transmitting data at a rate of 1M bits per second.
ICA-40	Ethernet*/802.3 Controller
CIS-10	Communication Interface Subsystem that supports a combination of RS-232, RS-422, or 20mA Current Loop Interfaces.

The CIS-10 Communication Interface Subsystem consists of the following items: an I/O processor bus-extender card that mounts on an I/O processor board, a four-slot auxiliary card cage for I/O interface cards, circuitry that allows the interface cards to communicate to the I/O Processor bus-extender card, and a cable that connects the I/O processor bus-extender card to the auxiliary card cage.

I/O Processor Fault-Checking Capability and Continuous Operation Supports Mirroring of Devices

In the fault-checking configuration, one BiiN 60 I/O processor board forms one I/O processor module. The I/O module provides fault-checking capability at the system bus interface by pairing BXUs to check data to and from the I/O module. The CP optionally appends an end-to-end checksum to mass storage transfers while data flows through the CP. This feature detects errors in industry-standard disk controllers, which would otherwise be undetected.

BiiN/OS implements the I/O recovery functions to achieve continuous operation. For example, consider disk mirroring and communications. BiiN/OS performs disk mirroring by writing a file to two different disks connected to two different I/O modules, as shown in Figure 7. If an error in the disk I/O subsystem occurs, data integrity and the availability of the file is maintained. After the error is corrected, BiiN/OS can re-establish mirroring as a background process. The BiiN 60 can be interconnected by several communication lines. If a line or an I/O subsystem is not available, communications are automatically routed to an available line through a different I/O subsystem.

Figure 7:
Continuous
Operation by
Mirroring I/O
Devices

Additional Fault-Tolerant Facilities

Fault-tolerant facilities extend beyond the computational, memory, and I/O subsystems. Environmental control devices, such as heat sensors, fans, and blowers with variable speeds are configured with redundant resources to maintain continuous operation. An option is available for redundant power supplies. Continuous operation is achieved by automatically switching to redundant resources if a fault occurs.

On-Line Replacement of Faulty Parts Virtually Eliminates System Downtime

To reduce system downtime and simplify repair and servicing, the BiiN 60 provides on-line replacement facilities of parts, such as processor, memory, and I/O processor boards, communication interface cards, AC and DC power supplies, and peripherals. On-line replacement procedures are simple and easy. A BiiN/OS utility steps the operator through the on-line repair process. After the new part is in place, diagnostics tests can be run to ensure that it is functioning properly. Upon successful completion of the diagnostic tests, BiiN/OS configures the part in the system. This entire process can be done while the system is operating. The on-line repair procedure can also be used to expand the capability of the BiiN 60. For example, the additional processor boards can be inserted while the computer is operating.

Built-in Error Monitoring System Ensures Proper Operating Conditions

Computer-wide error monitoring is performed by the system support subsystem (SSS) to ensure proper operating conditions. The SSS is an integral part of the BiiN 60, which monitors environmental conditions and voltage levels. The SSS consists of the system support module, the serial system bus, the control panel, and microcontrollers in the processor, memory, and I/O processor boards. The system support module, the heart of the SSS, monitors the temperature and airflow within the BiiN 60 enclosure, communicates with BiiN/OS, controls power-up and power-down of the computer, initiates a system reset, and provides a time-of-day timer. A redundant system support module is provided with the power supply option.

Initial Confidence Tests and On-Line Diagnostics Contribute to High Reliability

All systems include power-up diagnostics to detect potential problems before they occur. When a BiiN 60 is turned on, the CPU performs a self-test and a core integrity test. Next, basic confidence tests are run on all key system components, including the boot path, memory, cache, stable-store memory, system buses, I/O devices, and processors. Upon successful completion of the confidence tests, the system automatically initializes the VLSI components and builds a configuration table that records pertinent information, such as the number and types of boards and slot locations. If the initial confidence test identifies a faulty VLSI component, the component is removed from operation and the system is reconfigured, all within milliseconds.

The BiiN 60 supports on-line diagnostic tests that operate under BiiN/OS. The on-line diagnostic test consists of application-level programs that allow users to examine the status of system hardware, initiate utility programs to test specific configurations, and run diagnostic test programs. The on-line diagnostics provide high flexibility; they can be run in parallel to apply maximum stress, or be run serially to focus on a specific area, or be run using a combination of both.

Open System Standards Assure Interoperability

Adherence to industry standards allows the BiiN 60 to be easily connected to commonly available peripheral devices. The industry-recognized standards compatible with the BiiN 60 are shown in Table 1.

Table 1. List of Standards

Standard	Interface
ANSI	X3.131-1986 (SCSI), IPI X3T9.3 (IPI)
EIA	RS-232-C, RS-449/422
CCITT	X.21, X.24/X.27, and X.150 V.21, V.22, V.22bis, V.23, V.24/V.28, V.25bis, V.26, V.26bis, V.26ter, V.27, V.27bis, V.27ter, V.29, V.32, and V.54
IEEE	802.3 LAN, (Ethernet Blue Book Version 2.0 LAN), 754 (Floating Point), POSTX 1000.3
DoD	TCP/IP, FTP, TELNET, SMTP
SNA	3270, 3770, and LU 6.2, LU 0,1,2,3
ISO	Transport Class 4, FTAM, X.25

Modular Packaging Supports Configurability

The BiiN 60 offers unique, contemporary styling in a modular package design to enhance configurability. This modularity allows entry-level systems to be configured for a wide range of applications and existing systems to be easily expanded to match evolving computational or I/O needs. The BiiN 60 enclosure allows operation in a wide range of environments, including offices, shop floors, and customer service areas. This container, which is no higher than a desk, provides sufficient rear-panel space for orderly cable connections to networks and peripherals.

BiiN 60 Versatile Configurations Easily Expanded

The BiiN 60 offers versatile configurations that can be tailored to any application need in terms of processor, memory, or I/O requirements. For simplification, BiiN offers base system configurations, as shown in Table 2. These systems vary primarily in processor capability, ranging from the 60/20 system using two processors to the 60/80 system using eight processors. Each system supports up to 64 direct connection for terminals; eight are chosen to specifically support the RS-232 interface, the other connections are left as options for RS-232, RS-422, or 20mA Current Loop interfaces.

These systems support standard or fault-checking configurations. The 60/40 and 60/80 also support continuous operation and require the Continuous-Operation Power Supply Upgrade Kit for redundant power supplies.

Table 2. BiiN 60 Base System Configurations

Configuration	60/20	60/40	60/60	60/80
CPUs	2	4	6	8
Memory	32MB	64MB	64MB	64MB
Mass Storage				
Total Formatted Capacity	640MB	640MB	1280MB	1280MB
Formatted Capacity of 5.25 Inch Fixed-Disk Drive	320MB	320MB	320MB	320MB
Number of Fixed-Disk Drives	2	2	4	4
Cartridge Tape	125/150MB	125/150MB	125/150MB	125/150MB
Communication Devices				
Ethernet/802.3	Yes	Yes	Yes	Yes
Serial Communication Interfaces	8	8	8	8

Related Products and Upgrade Kits Allows the BiiN 60 to Expand as the Applications Grow

Modular and incrementally expandable, the BiiN 60 offers many options that customize the system to specific requirements, as shown in Table 3. Mass storage can be expanded to 40G bytes by connecting peripheral extension towers. The peripheral extension tower accommodates up to two 620M-Bytes (formatted capacity) IPI-2 fixed-disk drives and an IPI-3/2 controller.

The BiiN 60 can easily grow as applications requirements expand. Performance upgrade kits increase performance by adding processors without software conversions, or costly programming. The Continuous-Operation Power Supply Upgrade Kit provides the necessary power supplies and power conditioning modules to equip the BiiN 60 with a fully redundant power supply subsystem.

Table 3. The BiiN 60 Related Products

Add-In Boards	MMS-61 8M-Byte Stable-Store Memory Board
	MMS-62 16M-Byte Stable-Store Memory Board
	MEM-62 16M-Byte Memory Board
	IOP-60 I/O Processor Board
I/O Adapters Controllers, and Interfaces	ICA-20 SCSI Adapter
	ICA-25 IPI-3 Adapter
	ICA-30 Two-Line High-Speed RS-422 Interface
	ICA-40 Ethernet/802.3 Controller
Serial Interfaces	CSI-10 Four-Line RS-232 Interface
	CSI-20 Two-Line RS-232 and Two-Line RS-422 Interface
	CSI-30 20mA Current Loop Interface
	CIS-10 Communication Interface Subsystem
Mass Storage (formatted capacity)	FDF-20 320M-Byte Fixed-Disk Drive
	CTU-10 125/150M-Byte Cartridge Tape Drive
Expanded Mass Storage (formatted capacity)	FDN-20 620M-Byte IPI-2 Fixed-Disk Drive
	CTL-20 IPI-3/2 Controller
	EXT-40 Peripheral Extension Tower
Upgrade Kits	PUG-64 Two to Four Processor Upgrade Kit
	PUG-66 Four to Six Processor Upgrade Kit
	PUG-68 Six to Eight Processor Upgrade Kit
	PWR-60 Continuous-Operation Power Supply Upgrade Kit

The Extensible BiiN Operating System is Designed in Concert with BiiN Hardware

To take full advantage of the hardware features, all BiiN systems offer the advanced BiiN/OS. This operating system features multiuser and multitasking operation; transaction processing support; flexible object-based protection of software modules; transparent distribution of operating system resources among system nodes; record structured files with multiple indexes; extensive communications support; and both a window-style user interface and a POSIX interface. Additional system support is provided by means of a database management system; a full complement of languages (including Ada, C, COBOL, FORTRAN, and Pascal); and a complete program development environment. Because of the modularity of the BiiN 60, software developed on any model within the family is transparently transferable to any other system in the family. The operating system includes high-level diagnostics that can be run to determine the cause of errors.

For more information, in North America call 1-800-252-BiiN. In Oregon call (503) 696-4800. In Europe, call (49) 911 5219 0. Or write BiiN, 2111 NE 25th Avenue, Hillsboro, Oregon 97124-5961.

Documentation

For more information on the BiiN 60, refer to the following manuals:

Getting Started with BiiN Systems
BiiN Hardware Subsystems Reference Manual
BiiN Hardware System Description
BiiN Diagnostics User's Guide
BiiN System Overview
BiiN Command Language Executive Guide
BiiN Commands Reference Manual
BiiN Operating System User's Guide
BiiN Operating System Reference Manual

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