BELL TELEPHONE LABORATORIES
INCORPORATED

SUBJECT: GRAPHIC 2 - Hardware Organization
Case - 39991

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MEMORANDUM FOR FILE

The GRAPHIC 2 display console consists of an unmodified PDP-9 computer, a display processor, a cathode-ray-tube (CRT) display, and several input-output devices. The input devices are a console keyboard, eight pushbuttons and a light pen. A DATA-PHONE Type 201-A data set connects the console to a large central computer. Manufacturer's options included with the PDP-9 are a memory multiplexor, extended arithmetic element, and automatic priority interupt (API).* The total configuration is outlined in Fig. 1. A memorandum for file Interactive Graphics Consols Feb 1, 1968 by L. Rosler and P. E. Rosefeld contains the complete specifications for Graphic 2.

The display surface on which a picture is generated consists of a matrix of 1024×1024 addressable points. Lines and characters are generated by successively intensifying an appropriate series of dots.

The information to be displayed is stored in the memory of the PDP-9. The display processor produces a picture on the CRT by fetching the display data from the PDP-9 memory via the memory multiplexor, one word at a time. Each word is interpreted by the display processor according to the formats shown in Fig. 2.

A monitor program, running in the PDP-9, controls the display processor. The program attends to such functions as telling the display processor the memory address of the first word in a display list, restarting the display after a display list is finished, accepting real-time inputs from the operator, and controlling the DATA-PHONE communication with the central computer.

Appendix 1 contains a list of IOT instructions used to control the display processor. Signals from the display processor to the PDP-9 activate the Program Interrupt and an API channel (if the computer is equipped with that operation).

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* The automatic-priority-interrupt feature is not essential. When it is not available the standard program-interrupt facility is used, resulting in a slight (≈10%) decrease in display operating speed.

Figure 3 shows the organization of the display processor. The function of the various elements shown on this drawing will be discussed in the following text.

1. Display Address Register - The DAR is a 13-bit register used to specify to the PDP-9 memory the address from which the display processor wishes to fetch a word. The DAR is initialized by the monitor program via the I/O bus , and is incremented by one every time a display command is fetched. The contents of the DAR can be read back into the PDP-9 over the I/O bus . Thus, if the display halts, the monitor program can tell what word was being processed.

2. Memory Data Break Control - This circuit generates a signal which tells the PDP-9 that the display processor wants to steal a memory cycle. This "Break Request" signal is generated as the result of one of two conditions: either the display processor has finished executing a command and is ready to go to work on another, or the monitor program wishes to start the display processor and has executed an IOT instruction which causes the Memory Data Break Control to issue a Break Request. The Break Request signal will be generated only if the display is in the "Continuous Run" (as opposed to the "Single Step") state. In the Single Step state, the display processor halts after executing each command. The monitor program selects the Continuous Run or Single Step state by executing an appropriate IOT instruction.

3. Buffer Register - All commands (display data words) coming into the display processor are placed in the Buffer Register. This register can be loaded either directly from the PDP-9 memory (during a data break) or from the accumulator via the I/O bus (under control of an IOT instruction). The contents of the Buffer Register can be read back into the PDP-9 over the I/O bus . When a word is brought into the Buffer Register, the first four bits (which comprise the operation code) are decoded and a start pulse is sent to the appropriate control circuit.

4. X-Y Control - When a word brought into the Buffer Register is decoded as an X-Y command, control of the display processor passes to this circuit, which takes the following action:

a. If bit 6 in the Buffer Register is a Zero, the contents of bits 8 through 17 are placed in the 10-bit X register.

b. If bit 6 in the Buffer Register is a ONE, the contents of bits 8 through 17 are placed in the Y register.

c. If bit 5 of the Buffer Register is a ONE, a spot on the CRT is momentarily intensified after the appropriate register has been loaded.

d. If bit 4 of the Buffer Register is a ONE, 35 μsec of beam settling time is provided between the time the X or Y register is loaded and the time the spot is intensified and/or a "Task Completed" signal is sent to the Memory Data Break Control. If bit 4 is a ZERO, no delay is provided.

5. Parameter & Control Command Control - This circuit is activated if a word in the Buffer Register is decoded to be either a Parameter or a Control command. The registers which store the parameter information are set to the values contained in the command if the corresponding "Set" bits in the word are ONE. If any "Set" bit is a ZERO, the contents of the resister with which it is associated are left unchanged, with the exception of the Symmetries Store. If the Symmetry set bit is ZERO, the transformation called for by the contents of bits 9, 10 and 11 in the Buffer Register is accumulated with the transformation presently stored in the Symmetries Store and the result is then replaced in the Symmetries Store.

The parameters are:

BLINK - causes figures drawn while this feature is enabled to blink at about 2 Hz.

LIGHT PEN - enables or disables the light pen. The light pen will be discussed further under the section on Light-Pen Control.

SYMMETRY - determines whether succeeding X and Y move commands generated by the character, Increment or Vector Control logic will be complemented and/or exchanged before being forwarded to the X and Y registers. The three bits are the Exchange bit, the Complement-X bit and the

Complement-Y bit. When both complementing and exchanging are to occur, complementing occurs first.

SCALE - determines whether succeeding figures will be drawn in scale 1, 2, 4 or 8. Scaling is discussed further in the section describing the X Register. The scale setting has no effect on X-Y commands, as these are absolute rather than relative positioning commands.

INTENSITY - selects one of four brightness levels for the CRT.

OVERRIDE - causes figures drawn while this feature is enabled to be invisible. Override can also be turned on or off by IOT instructions.

BROKEN LINE - causes vectors drawn while this feature is enabled to appear as broken (dashed) lines.

After the parameter storage registers are loaded, a "Task Completed" signal is normally sent to the Memory Data Break Control. However, if the command in the Buffer register is a Control command with the Stop bit set, or with the Conditional-Stop bit set and the Conditional-Stop circuitry activated (by previous execution of the appropriate IOT instruction by the monitor program), then the Task completed signal is not sent to the Memory Data Break Control. Instead the display processor halts, after signaling the PDP-9 via the API why it is stopping.

6. Vector & Short Vector Control - This circuit takes control if the word in the Buffer Register is a Vector or Short Vector command. It first loads the DELTA-X or DELTA-Y holding register (both registers at once in the case of a short vector), and then issues appropriate move-X and move-Y pulses to the Scaling and Rotation circuits to produce the desired vector.. The Binary Rate Multiplier determines the sequence in which the move-X and move-Y pulses are generated so as best to approximate the desired straight line.

If the X and/or the Y register overflows or underflows, or if a light-pen strike occurs, the generation of the vector immediately halts and the PDP-9 is signaled via the API. The generation of the vector can be resumed if the monitor program issues the appropriate IOT instruction. If a vector is resumed after a register overflow or underflow (also known as an "edge violation") it will reappear on the opposite side of the screen from which it went off.

When the vector is completed, a Task Completed signal is sent to the Memory Data Break Control.

7. Increment Control - This circuit is very similar to the Vector Control logic, except that increments are packed two to a command, can go only in eight discrete directions, and must be 0 to 7 dots in length. Increments are affected the same as vectors by scaling, rotation, edge violations and light-pen strikes.

8. Character Control - This circuit generates the two characters specified in a character command. It issues move-X and move-Y commands in much the same manner as the Increment and Vector Controls. It also is affected by scaling, rotation, edge violations and light-pen strikes. The sequence of moves to form a character is determined by consulting a table stored in the memory of the PDP-9. This is the reason for the dashed line between the Character Control and the PDP-9 memory on the block diagram. Changing the table in the memory changes the character font.

9. Trap - If the word brought into the Buffer Register is decoded as a Trap command, the display processor first notifies the PDP-9, via the API, that a Trap command has been encountered, and then halts. A Trap command generates one of eight different API signals corresponding to the setting of bits 1, 2 and 3, thus facilitating the use of up to eight different trap-handling subroutines in the monitor program.

10. Rotation Circuit - This circuitry receives move-X and move-Y commands from the Character, Increment and Vector Control circuits. It also receives information from the parameter storage registers about the present setting of symmetry. It then dispatches increment or decrement commands to the X and the Y registers as a function of these inputs.

11. X Register - This is a 10-bit up/down counter which can also be set to an intial value by the X-Y control. The contents of the X register can also be read into the PDP-9 by the monitor program via the I/O bus . The counter is incremented or decremented by 1, 2, 4 or 8 for each step-X input pulse, depending on the scale setting presently in the parameter store. Thus if a vector is generated in scale 1, adjacent addressable points on the CRT will be brightened. In scale 2 every second addressable point will be brightened. The length of the vector will be twice as long as in scale 1, although the total number

of brightened points will be the same. Similarly, in scales 4 or 8 every fourth or eighth point is brightened, and the length of the vector will be four or eight times greater than it would be in scale 1. If the counter overflows or underflows, a signal is sent to the Edge Detection logic. The parallel output of the X Register drives the X Digital-to-Analog converter which positions the beam on the CRT in the X direction.

12. Y Register - Same as the X register, but for the Y direction.

13. Edge Detector - If the X or Y register overflows or underflows, the Edge Detector sends a halt signal to the Character, Increment and Vector Control circuits. It also signals the PDP-9 via the API. The monitor program can then examine the contents of the Edge Detector via the I/O bus to determine whether the X and/or the Y register caused the halt and whether it overflowed or underflowed.

14. Pushbutton Control - The Pushbutton Control responds to IOT instructions executed by the monitor program to selectively illuminate any or all of the eight pushbutton switches. It also signals the PDP-9 via the API whenever a pushbutton is depressed. The monitor program can then determine which button is pressed by examining the state of the buttons via the I/O bus . This signal disappears when the button is released.

15. Console Keyboard - Whenever a key on the console keyboard is depressed, the PDP-9 is signaled via the API. The monitor program can then determine which key is depressed by reading the output of the keyboard over the I/O bus . This signal disappears when the key is released.

16. Light-Pen Control - The Light-Pen Control circuit turns the light pen on and off under control of a flip-flop in the parameter store. This flip-flop can be turned on or off by the monitor program by execution of the appropriate IOT instructions, as well as by a parameter command. If the light pen is enabled and a spot is produced on the surface of the CRT within its field of view, the circuit immediately sends a halt signal to the Character, Increment and Vector Control circuits, and signals the PDP-9 via the API that a light-pen strike has occurred. The monitor program can resume the execution of the command that caused the light-pen strike by executing an IOT instruction.

17. Data-Phone Interface - The Data-Phone Interface enables the PDP-9 to communicate with a remote computer over a Data-Phone by sending and receiving information in 8-bit bytes. Seven of the eight bits are data bits. The eighth bit is a parity bit which is automatically added, checked, and removed by the interface. Operation using either even or odd parity can be selected by the monitor program by issuing IOT instructions. Since the monitor program can select a different parity for each 7-bit byte it wants to send, it can be programmed to send, in effect, 8-bit data bytes without parity. Information is transferred between the interface and the PDP-9 via the I/O bus. The interface signals the PDP-9 via the API when it is ready to accept another byte and wants to pass it on.

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Appendix 1

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