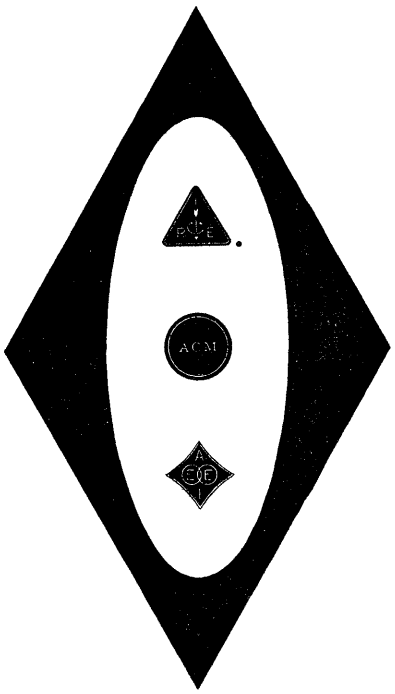
T-92

Proceedings of the

EASTERN JOINT COMPUTER CONFERENCE

December 10–12, 1956 New York, N. Y.



THEME: NEW DEVELOPMENTS IN COMPUTERS

Sponsors:

AMERICAN INSTITUTE OF ELECTRICAL ENGINEERS
Committee on Computing Devices
THE ASSOCIATION FOR COMPUTING MACHINERY
THE INSTITUTE OF RADIO ENGINEERS
Professional Group on Electric Computers

Printed in the United States of America

Price $3.00

ADDITIONAL COPIES

Additional copies may be purchased at $3.00 per copy. Checks should be made payable to any one of the following sponsoring societies:

AMERICAN INSTITUTE OF ELECTRICAL ENGINEERS
33 West 39th Street, New York 18, N. Y.

ASSOCIATION FOR COMPUTING MACHINERY
2 East 63rd Street, New York 21, N. Y.

INSTITUTE OF RADIO ENGINEERS
1 East 79th Street, New York 21, N. Y.

PROCEEDINGS OF THE EASTERN JOINT COMPUTER CONFERENCE

PAPERS AND DISCUSSIONS PRESENTED
AT THE JOINT COMPUTER CONFERENCE
NEW YORK, N. Y., DECEMBER 10–12, 1956

THEME: NEW DEVELOPMENTS IN COMPUTERS

SPONSORS
AMERICAN INSTITUTE OF ELECTRICAL ENGINEERS
Committee on Computing Devices
THE ASSOCIATION OF COMPUTING MACHINERY
THE INSTITUTE OF RADIO ENGINEERS
Professional Group on Electronic Computers

Published by
American Institute of Electrical Engineers
33 West 39th Street, New York 18, N. Y.

NATIONAL JOINT COMPUTER CONFERENCE

Chairman

M. M. ASTRAHAN, International Business Machines Corporation

Chairman for the Eastern Joint Computer Conference, 1956

J. R. WEINER, Remington Rand Univac

Chairman for the Western Joint Computer Conference, 1957

J. L. BARNES, Systems Laboratories Corporation

AIEE Representatives

J. G. BRAINERD, University of Pennsylvania
H. F. MITCHELL, Sperry Rand Corporation
P. L. MORTON, University of California, Berkeley
D. C. ROSS, International Business Machines Corporation

Ex-Officio—E. L. HARDER
Westinghouse Electric Corporation
Chairman, AIEE Committee on Computing Devices
Headquarters Representative—R. S. GARDNER
Assistant Secretary, AIEE

ACM Representatives

J. L. BARNES, Systems Laboratories Corporation
G. W. KING, International Telemeter Corporation
R. J. GROSCH, General Electric Company
A. PERLIS, Carnegie Institute of Technology

Ex-Officio—J. W. CARR III
University of Michigan
President, ACM
Headquarters Representative—J. MOSHMAN
Bell Telephone Laboratories
Secretary, ACM

IRE Representatives

W. F. GUNNING, Beckman Instrument
D. HAAGENS, Underwood Corporation
W. S. SPEER, Nordan-Ketay Corporation
J. R. WEINER, Remington Rand Univac

Ex-Officio—J. NOE
Stanford Research Institute
Chairman, IRE Professional Group on Electronic Computers
Headquarters Representative—L. G. CUMMINGS
Technical Secretary, IRE

The charter of the National Joint Computer Conference was revised on December 12, 1956, and appears on page 1.

EASTERN JOINT COMPUTER CONFERENCE COMMITTEE

1956

Chairman: J. R. WEINER, Remington Rand Univac

LOCAL ARRANGEMENTS COMMITTEE

Chairman: J. A. HADDAD, International Business Machines Corporation

Secretary: C. E. STEVENS, International Business Machines Corporation
Exhibits: A. D. MEACHAM, Remington Rand
Finance: A. R. MOHR, Waldorf Instrument Corporation
Hotel: J. A. GRUNDY, Remington Rand
Inspection Trips: M. GRIESER, Underwood Corporation
Printing: P. E. MAGDEBURGER, Underwood Corporation
Publicity: A. J. FORMAN, Tele-Tech and Electronics Industries
Registration: W. P. HEISING, International Business Machines Corporation

PROGRAM COMMITTEE

Chairman: J. W. LEAS, Radio Corporation of America

J. A. BAIRD, Bell Telephone Laboratories
U. C. S. DILKS, Burroughs Corporation
J. J. EACHUS, DATAmatic Corporation
J. P. ECKERT, Jr., Remington Rand Univac
R. D. ELBOURN, National Bureau of Standards
W. HALSTEAD, Radio Corporation of America
D. R. HEARSUM, National Cash Register Company
R. E. MEAGHER, University of Illinois
J. A. O'BRIEN, Lincoln Laboratories, Massachusetts Institute of Technology
R. L. PALMER, International Business Machines Corporation
E. A. SMITH, Bureau of Ships, Navy Department
T. T. PATTERSON, Radio Corporation of America
J. C. SIMS, Jr., Remington Rand Univac

PUBLICATIONS COMMITTEE

Chairman: V. N. VAUGHAN, Jr., American Telephone and Telegraph Company

C. COLE, Radio Corporation of America
J. W. GUPPY, Bell Telephone Laboratories
L. HOBBS, Remington Rand Univac
A. KATZ, Radio Corporation of America
W. R. SMITH, American Telephone and Telegraph Company
W. F. STEAGALL, Remington Rand Univac

Contents

Organization of the National Joint Computer Committee

Resolution adopted by the National Joint Computer Committee, December 12, 1956, subject to ratification by the sponsoring societies

A. Name and Object

1. *Name.* This Committee shall be known as the National Joint Computer Committee, herein identified by the abbreviation "NJCC."

2. *Sponsorship.* The NJCC shall be jointly and equally sponsored by the following three organizations:

Association for Computing Machinery

Committee on Computing Devices of the American Institute of Electrical Engineers

Professional Group on Electronic Computers of the Institute of Radio Engineers, Inc.

3. *Object.* The Committee shall aid in the promotion of close cooperation and coordination in the activities of the sponsoring societies related to the field of computer engineering and allied arts and sciences. Its objects shall be scientific, literary, and educational in character and in harmony with the aims of its sponsors.

B. Field of Interest

1. *Scope of NJCC.* The general scope of the NJCC shall be that which stems from the scope of the Association for Computing Machinery, the Committee on Computing Devices of the AIEE, and the Professional Group on Electronic Computers of the IRE.

2. *Major Interests.* The major field of interest of the NJCC shall be the design, development, manufacture, and use of computers, but shall also include an interest in the various activities that contribute to this field or utilize the products or techniques of this field. The term "computers" shall be interpreted broadly to include data, and information handling and processing systems useful in scientific computation, business accounting, and industrial and military control problems.

C. Committee Formation and Management

1. *Committee Structure.* The NJCC shall derive its authority from the three sponsoring groups referred to in Section A2. The heads of these three groups, namely, the President of the Association for Computing Machinery, the Chairman of the AIEE Committee on Computing Devices, and the Chairman of the IRE Professional Group on Electronic Computers, shall be ex officio voting members and shall each name four voting members in addition to themselves. They shall also designate one member or previous member as Chairman and another member as Vice-Chairman. The Chairman shall appoint a Secretary-Treasurer. In addition, the Technical Society representatives of the sponsoring societies shall be ex officio non-voting members of the NJCC. An important consideration in the selection of members shall be their ability and willingness to attend the committee meetings.

2. *Tenure.* The terms of office of the committee members appointed by the sponsoring societies shall be two years, two new members being appointed each year from each society.

In selecting committee members, each society shall attempt to secure a balanced geographic representation according to the needs of the NJCC and the society. The NJCC Chairman may recommend areas.

It is recommended that members from each area of the country be suggested by the respective active organizations in that area.

3. *Terms of NJCC Officers.* The officers' terms shall normally coincide with the calendar year and the incumbents shall continue to serve until their successors are selected. The selection of officers should be made as soon as expedient following the appointment of new committee members.

4. *Committee Meetings.* The NJCC shall meet at least twice a year, to set policies, make plans, and discuss problems within its field of interest. The meetings shall be distinct from meetings of the Steering Committees operating the Conferences.

5. *Executive Committee.* Questions of NJCC policy or NJCC decisions not conveniently settled at a meeting of the NJCC as a whole and not otherwise specifically delegated by the Charter or by the NJCC as a whole should be decided by the Executive Committee which shall consist of the heads of the three sponsoring groups and the NJCC Chairman.

6. *NJCC Chairman.* The NJCC Chairman, the chief executive officer of the NJCC, shall—be generally responsible for the implementation of NJCC policy or decisions—act as representative of the three societies in setting reasonable and consistent conference policies—call and preside over NJCC meetings—obtain clearance from the three societies for specific conference operations and fiscal plans—appoint and delegate individuals to carry out the work of the NJCC, such as the preparation of specialized unified mailing lists.

7. *Vice-Chairman.* The NJCC Vice-Chairman shall assist the Chairman in executive matters and shall act for the Chairman in his absence.

For the sake of continuity, it is recommended that the Vice-Chairman succeed the Chairman. It is further recommended that he be selected from a different geographical area from the Chairman.

8. *Secretary-Treasurer.* The NJCC Secretary-Treasurer shall record and circulate minutes of the NJCC meetings—arrange for final summary reports of each conference to be sent to the NJCC members, to the three sponsoring societies, and to other interested parties—act as financial liaison between the Finance Chairman of each conference and the three sponsoring societies.

9. *Voting Procedure.* Questions submitted to the Committee for vote shall be decided by a majority of the voting members. The Chairman shall vote only if his vote will decide an otherwise inconclusive vote.

D. Committee Activities

1. *Conferences.* The NJCC shall sponsor annually one or more conferences. Such conferences are not to be considered as being in competition with or a replacement of the regular activities of the spon-

soring societies. Instead, the conferences are to represent the combined efforts of the sponsors to produce major technical meetings of a specialized nature. Each conference is to treat a selected theme in the computer field in a thorough and authoritative manner; inspection trips and exhibits are to be featured; formal and informal discussions are to be encouraged; and a conference report is to be published. The quality and coherence of the technical programs shall be such that the publications resulting from the conferences will be useful as current and authoritative text or reference books covering the various phases of the computer field.

The NJCC will concern itself with such conference questions as can best be considered on the national level. Examples of such questions might include:

Decision on location of conference;

Decision on topic or theme of conference;

Decision on scheduling of conference to optimize coordination with other conferences and to improve long-range planning;

Recommendations of procedures and standards for publications, publicity, and exhibit policies of each conference.

At least a year in advance of a proposed meeting, the NJCC chairman with the advice of the committee shall appoint a general chairman to plan and operate each NJCC conference. The general chairman shall be responsible for forming a conference steering committee from interested and capable people in the geographical area of the conference. This steering committee will work with local organizations in the actual initiation and management of the conference. The steering committee shall consist of, in addition to the general chairman, a finance chairman, a local arrangements chairman, a technical program chairman, and a publications chairman.

(a) *General Chairman.* The general chairman shall have the general executive responsibility for the conference and shall have the power to appoint additional members to the steering committee, where required, to carry out its work.

(b) *Finance Chairman.* The finance chairman shall be responsible for all financial transactions and accounts concerned with a particular conference.

(c) *Technical Program Chairman.* The technical program chairman shall be responsible for implementing all phases of the technical program. This includes selection of and arrangements with all speakers and session chairmen, and procurement of written material as required by the publication committee and local arrangements committee.

(d) *Local Arrangements Chairman.* The local arrangements chairman shall be responsible for all local arrangements, including registration, inspection trips, exhibits, hotel arrangements. He shall also be responsible for all conference publicity, both local and national.

(e) *Publications Chairman.* The publications chairman shall be responsible for the preparation of the Proceedings of the conference.

2. *Other Activities.* The NJCC may establish other committees as required to carry out its work. Such committees may, for example, be established to study and recommend long-range coordinated plans for national and international conferences, exhibits, and publications in the computer field, to study and make recommendations concerning standardization in the computer field, or to study and make recommendations concerning education in the computer field. The sponsoring societies may also, if it is mutually agreeable, request the NJCC to undertake other projects in the computer field which may be particularly expedited through the joint and coordinated action of the committee.

E. Financial Considerations

1. *Conference Financial Matters.* The previous conferences and publications sponsored by the National Joint Computer Committee have been so successful from a monetary point of view that financial support of future conferences appears definite. However, in order to insure that the basic responsibility for the management of future conferences always springs from, and resides in, the three sponsoring societies, the National Joint Computer Committee shall treat each future conference as an independent project requiring separate approval and initial loans from, and financial accountability to, the sponsoring societies. The Finance Chairman of each conference will be responsible to these Societies through the NJCC Secretary-Treasurer for the financial affairs of his own group.

2. *General Financial Procedure.* Approximately one year in advance of a conference, the steering committee for the conference shall formulate a tentative plan of action together with a conference budget and submit this for approval to the Sponsoring Societies through the NJCC Chairman. If the plans are approved by the Sponsoring Societies, the NJCC chairman shall request an appropriate loan from each of the sponsors and forward the money to the Finance Chairman of the Conference Steering Committee.

3. *Disposition of Surplus Funds.* All surplus funds resulting from the operation of a conference shall be distributed equally to the three sponsors by the NJCC Secretary-Treasurer within one year after the date of the conference.

4. *Committee Expenses.* The NJCC shall formulate a budget of expenses which it expects to incur in connection with its activities, but not chargeable directly to a particular conference. As for instance, committee stationery, preparation of a unified mailing list, and the like. This budget will be submitted to each of the sponsoring societies accompanied by a request for an appropriation from these sponsoring societies covering these expenses. These funds will be turned over to the Secretary-Treasurer, who will account for them to the sponsoring societies.

Keynote Address

H. T. ENGSTROM

I AM deeply honored to be invited to furnish the keynote to this important conference. As a mathematician by training, I am perhaps somewhat misplaced in this role. However, by a curious sequence of circumstances, I have been in a position to observe the progress of electronic digital data handling since the beginning of World War II. Although the term "electronic computing" covers a wide range of equipment, I am using the term in the sense of the large-scale internally programmed digital computers which have made so many contributions to the scientific and business life of the country during the past 5 years.

As you all know, the great impetus to this art came from the military during World War II. The impact of military needs on scientfic progress is not new. It probably began with Archimedes, who helped his cousin the tyrant of Syracuse to defend that city against the Romans in 212 B.C. I quote from Plutarch's *Life of Marcellus* in this regard:

> The king prayed him to make him some engines, both to assault and defend, in all manner of sieges and assaults. So Archimedes made him many engines, but King Hieron never occupied any of them, because he reigned the most part of his time in peace without any wars.

The electronic computing engines were constructed during World War II, and some of them made significant contributions to our victory. However, it was not really until the end of World War II that the general-purpose electronic computing devices began to be delivered. The conviction of their practicality, and faith in the future rested principally among those people who had been working in the field for the military during the war. The Defense Department in general was convinced of the necessity of pursuing research and development in this area in the soluion of military problems. American industry in 1946, however, was not so convinced. As a result, in the post-war period, many individuals with faith in the future of the field established small independent companies which were financed by the Defense Department. I do not need to name these companies since I am sure most of you are familiar with them. Some of the universities, such as Harvard, Princeton, and the University of Pennsylvania, also carried on research and development in the logical structure and component development in the field. Again, in these universities the program was stimulated essentially by individuals who had faith in the future of large-scale computing devices. University management was not convinced, and in some cases still remains unconvinced, that the field of logical structure design of computing devices was one with proper academic stature.

In 1950, many of the problems with respect to memories, input-output devices, and peripheral equipment had been solved so that well-balanced large-scale computing devices were put into operation. At this time, big business became strongly interested in the field. Many of the small companies who had had a difficult financial struggle to keep going, were merged with the large companies, so that in the early 1950's the electronic data-processing industry achieved a financial stability as well as a technical maturity. It is difficult to estimate the phenomenal growth of the industry. It is certainly true that the present volume of business in electronic data-handling equipment is in excess of one billion dollars per year. Speculations as to its ultimate position are difficult, but certainly the industry will not reach a saturation point before expanding by at least a factor of ten.

The delivery of many of these equipments to industry and government has opened up a tremendous activity in the field of applications. The most important aspect of electronic computation in the last several years has been precisely in the area of a better understanding of the value of this equipment in our scientific and business problems.

Although the industry has achieved technical reliability and financial stability, there are many areas in which serious problems still exist, and I should like to point out some of these areas which come to mind, and which the members of this Computer Conference can assist in clarifying.

The enthusiasm with which electronic data handling and automation possibilities have been greeted is astonishing. I should not like to state categorically that the field has been much oversold, but I do think the overoptimism of engineers and scientists in connection with the field is a definite fact. This optimism causes serious complications. If an industry or the Department of Defense relies upon estimates of delivery and performance which are made by you engineers, they must have some degree of confidence in your technical and financial judgment. There have been too many cases of long delays in the delivery of vital equipment. Many of these delays could have been avoided had the project been less ambitious technically. It is better to have equipment on time, even though it may operate at only one half the speed which may be technically feasible. Another aspect of the industry, which I believe you should consider rather seriously, is that of engineering manpower. On the basis of scientific optimism, the Defense Department is pursuing many projects in electronic computing. These projects result in many contracts with private industry. The usual procedure following the award of one of these major contracts is for an industry to proselytize engineering personnel from its competitors. As a result, there is an inflationary spiral of salaries for engineering and scientific personnel. You may well say that a man is worthy of his hire. I do not subscribe completely to this point of view. The usurer who extracts excessive interest rates is not particularly admirable, nor is prostitution recognized as a reputable profession. I believe that it is within the power of you technical people to assist in rectifying this situation. I believe you have lost a great deal of dignity in participating so actively in this mad scramble for personnel. Engineers can be of great assistance to the national defense in assessing proposed employment changes, not only on the basis of salary, but on the basis of the technical merit of the projects concerned and your potential (technical) achievement. It is certainly your responsibility to see that our industrial and defense program is on a sound basis.

I hope you will not feel that these criticisms of overoptimism and personnel instability detract from your achievement over the past 10 years in the creation of a tremendous industry which is one of the important elements of our national defense. The many papers presented at this conference are a witness to the continued dynamic advance in the art as well as the industry. However, the soundness of your position in American economic life is clearly dependent upon

---

Full text of the keynote address presented at the Eastern Joint Computer Conference, New York, N. Y., December 10, 1956.

HOWARD T. ENGSTROM is with the National Security Administration, Washington, D. C.

your personal integrity, and I believe we should all give more attention to the two points I have tried to make, with respect to dependability in the matter of prediction of achievements in regard to time, money, and engineering manpower.

One of your previous speakers quoted the great German novelist, Thomas Mann, as follows:

> What perplexes the world is disparity between the swiftness of the spirit and the immense unwieldiness, sluggishness, inertia, and permanence of matter.

As to the arts with which we are concerned, I think this statement may well be reversed. We have developed computing equipment of great speed and capacity, and what perplexes the industry and the Department of Defense is the sluggishness of the human spirit in participating in their fundamental problems.

Discussion

Eugene H. Jacobs (Rand Corporation): Why doesn't the Defense Department stop giving new contracts to companies which do not have sufficient personnel on hand?

H. T. Engstrom: The situation is that there is no spare scientific and technical manpower available, so that whenever the Defense Department gives a contract, it is expected that the companies will get the personnel from some other source presumably from other occupations.

The program of the Defense Department is to put these people upon projects which we feel are more vital to the defense problem; some of the change in personnel is necessary, since there is no idle manpower. I might add, in this regard, that my agency in Washington is also looking for people.

W. C. Richey (Lockheed): Have you examined or found ways to use computer equipment to expedite security clearances?

H. T. Engstrom: I might explain that although my agency is the National Security Agency, it is not responsible for security clearances. However, to my knowledge, large-scale computing equipment has not been applied to the problem of security clearances.

Introduction

JAMES R. WEINER

ON BEHALF of the Joint Computer Committee and the three sponsoring societies, the American Institute of Electrical Engineers, the Institute of Radio Engineers, and the Association for Computing Machinery, I should like to welcome you to the sixth annual Eastern Joint Computer Conference. It would appear from our registration at this point, that this is our largest meeting to date. The major portion of the credit for the success of this conference should go to the three conference committees and their chairmen, J. W. Leas of the Program Committee, J. A. Haddad of the Local Arrangements Committee, and V. N. Vaughan of the Publication Committee. These men and the members of their committees have devoted a great amount of time to this conference, and we owe our thanks to them as well as to their employers who have encouraged them in their efforts.

As mentioned previously, this is the sixth annual Eastern Joint Computer Conference. The first was held in Philadelphia in December, 1951. It was sponsored by the same three societies, and the attendance was somewhat less than 1,000. Since that time, conferences have been held annually, both on the east and west coasts, and our meetings, originally known as the Joint Computer Conferences are now called Eastern in deference to meetings held in the West.

If we review the previous meetings we find their themes to be the following:

1951 Review of Electronic Digital Computers
1952 Review of Input and Output Equipment Used in Computing Systems
1953 Information Processing Systems-Reliability and Requirements
1954 Design and Application of Small Digital Computers
1955 Computers in Business and Industrial Systems

In addition, two West Coast conferences have been held: one on trends in computers, automatic control, and data processing; and another on tutorial sessions and discussions on digital and analog devices. At this conference, whose theme is "New Developments in Computers," we discuss some elements of each of the topics listed. Moreover, we may be starting a second cycle because we are concerned now primarily with the solid-state computer, utilizing either the transistor or the magnetic amplifier. It is quite possible that, except for certain specialized applications involving extreme ambient conditions, the role of the vacuum tube in digital data-processing equipment may be over in the near future. This has led to many new engineering and systems considerations, some of which are described at this conference.

Our conference is organized in the following manner: First, a session devoted to new computers and computer systems almost all of a solid-state nature; then two sessions essentially on new components and circuits interspersed with two sessions on input-output devices. The first component session is entitled Circuits and Components, and is concerned wholly with the sort of elements that would be used primarily in the arithmetic element of the central computer. The second component session is devoted to high-speed memories. The two input-output sessions cover first a rather diverse group of equipment and, second, some individual solutions to the random access file problem.

We hope you find the program both interesting and informative. We thank you for attending this conference which you believe to be of sufficient interest to attract you here from all parts of the civilized world.

JAMES R. WEINER, Chairman Eastern Joint Computer Conference, is with Remington Rand Univac, Division of the Sperry Rand Corporation, Philadelphia, Pa.

New Computer Developments Around the World

EVERETT S. CALHOUN

IT HAS been an interesting assignment to travel during the past 4 months through 20 countries to observe the developments in electronic computers and office automation. Ninety-five visits have turned up over 35 different computers and a host of electromechanical devices for data recording.

Inasmuch as my primary interest was in automatic data-processing no special effort was made to visit analog computers laboratories or scientific computer installations. However, as in the United States, nearly all of the European computers were originally designed for military or scientific-mathematical purposes. To capture a share of the larger business data-processing market, most of these are now being altered to provide better input-output facilities.

The concepts of IDP (integrated data-processing) and EDP (electronic data-processing) and office automation are already accepted by big business abroad. Government bureaus, banks, insurance companies, manufacturers, department stores, and mail order houses eagerly await the day when automation will supply an answer to their rising office costs. Although salaries appear low compared to ours when converted to U. S. dollars, the percentage of clerical costs to total overhead is too high, and good clerks are scarce in Europe also. The knowledge is widespread that new business tools will soon be available which will not only do routine work automatically, but also provide management with better and quicker information.

Europe is undergoing a building boom that is unprecedented. Many parts of the world, particularly our former enemies, are approaching a prosperity similar to ours in the 1920's. New factories, stores offices, and apartments are replacing the bomb shattered obsolescence of the 1930's, and the most modern equipment is being installed. Business men speak about Univac and the 650 and Datatron with the same familiarity as in this country.

In the Far East most of the electronic developments are coming from Tokyo. The Shibaura Electric Company built their first computer, the TAC (Tokyo automatic computer), for Tokyo University. This serial-digital binary machine has both electrostatic tube and magnetic-drum storage. A second model is nearly completed. In the government electrotechnical laboratory a partly transistorized computer was demonstrated, called the ETL Mark III. Along with 55 vacuum tubes and 1,600 germanium diodes, 120 transistors are used. Stored in glass supersonic delay lines are 256 words, providing multiplication in less than one millisecond. Kyto University is also using a computer in its mathematical department, and several other firms are designing new machines. When entering the air-conditioned room where a large relay computer was in use at the telephone company the writer was asked to remove his shoes "to prevent the entry of dust." Removing shoes is of course a common occurrence in Japan, but perhaps some of our magnetic tape installation could adopt this plan as a cure for dropped bits.

The Statistical Institute of India has ordered a URAL computer from Russia. This decision followed a trip to the U. S. to investigate available equipment. Dr. Mahalinobis, the director, was not sure of the characteristics or specifications, nor the type of input and output equipment which would be furnished, but is appears to be in the class with a Univac no. 120 or an IBM no. 607 or a BULL Gamma.

Discussions with several people who have visited Russian computer developments indicate that the Russians have completed a number of designs of modern computers at several laboratories, the principal one being the BESM at the Institute of Exact Mechanics and Computing Techniques at the Academy of Sciences at Moscow. I heard a speech at the instruments and measurements conference in Stockholm by S. A. Lebedev of this organization. He described the installation of Williams tubes in the BESM, replacing the mercury-delay lines. He seemed rather disappointed that even the inventor of the tube agrees that the cathode-ray tube storage is becoming obsolete, and that every other speaker was emphasizing the replacement of cathode-ray tubes with magnetic-core store. I have no doubt, however, that their reputed 30 million document library in Lomonosoff University, translated from every language by the 10,000 technical foreign language staff, has access to every process and patent published anywhere, including full data on ferrites. Mr. Lebedev also discussed the use of magnetic drums and tapes, and the existence of a rotary-wheel printer and another output device projecting 200 digits per second to photographic film. The BESM computer is reported to have an average operating speed of 7,000 to 8,000 3-address operations per second including access time.

A visit to the Leipzig Fair in East Germany proved fruitless as far as electronic machines were concerned. Eastern Germany was the location of the office-equipment industry before the war. Firms like Rheinmettal, Astra, Mercedes and others are still in operation, and doing considerable export business to all the world except the U. S. While the quality of these machines suffered as a result of poor quality steel after the war, most users now report very satisfactory quality in recent production. It was significant that not one word regarding Russia was included in the publicity, and not one display was marked "made in the USSR." In former years such products formed a prominent part of the huge trade fair.

An exciting documentary could be written about the reestablishment of the office equipment industry in Germany since 1945. Many plants were demolished in the war, and, particularly in Berlin, the remaining equipment was looted by the Russians and taken to their Zone. Branch factories of large U. S. firms were left with only a shell of a building, and without a tool or even a light bulb. These plants have all been restored with modern tooling and machines now, and there is no evidence that the Russians ever put the pilfered equipment into production.

I talked with a number of East German factory executives who fled with microfilms and worthless marks across the line by bicycle. They reassembled, pooled their resources, acquired financing and personnel. Buildings were constructed for production of typewriters, adding machines, and bookkeeping machines to meet the needs of western Europe. The basic superiority and talent of German technicians in the mechanical arts has resulted in a surprising comeback, and has established Germany as the largest exporter of office equipment.

EVERETT S. CALHOUN is with the Stanford Research Institute, Menlo Park, Calif.

Computer developments in Germany have been sponsored by the Deutsche Forschungs Gemeinschaft (DFG) organization, with members representing various industries and branches of government. With a budget of many millions of marks for the advancement of science, they have allocated to several universities sufficient money to build electronic computers. Goettingen University was putting the finishing touches on Mark III when I was there, and they have been operating G-1 since 1952. G-1 and G-2 were built from U. S. war surplus for the most part, and are relatively slow; but G-3 is a ferrite-core storage parallel machine of much more ambitious proportions. The G-2 model includes a magnetic drum with 2,096 words of storage, and is serial in operation.

When one wishes to find out about computers in Germany he visits Prof. Alwin Walther at Darmstadt Technische Hochschule. His staff maintains the best library of computer information in Europe. Prof. Walther has been the inspiration in the design and construction of computers in several other schools in Germany, and his own group has nearly finished the DERA (Darmstadt electronic recorder automatic), which they will use in the mathematics department. Another group has been working for 4 years at the Munich Technical Highschool (6,000-student enrollment, college level) on the PERM, a computer with an exceptionally fast drum, 15,000 rpm. Completion is being delayed by the replacement of 100,000 faulty connectors, a not-too-uncommon complaint of current computers.

The only operation in Germany where a quantity of computers have been made and sold is in a barn in Neukirchen-Hunfeld where Dr. Konrad Zuse has built 12 relay analog machines. He is currently finishing the first digital-electronic magnetic-drum model, and reports that he has a backlog of half-a-dozen orders. The price will be in the neighborhood of 100,000 marks ($25,000). This can be better understood when salaries of $100 per month and plant rent of perhaps $100 per month are taken into account.

The center of full-fledged production of electronic computers in Germany will probably be at Stuttgart, a beautiful, thriving, modern industrial city of one million skilled people. International Business Machine Corp. has established its first no. 650 production-line here. Standard Electric Co., a subsidiary of International Telephone and Telegraph Corp., have formed the "Informatik" division of their 10,000-man operation to build transistorized computers. They are closely linked with large operations in Pforzheim, and in Belgium, where two computers have been built, one for an American buyer. In Britain, Standard Electric Co. is also mass producing a computer designed in Holland, and together with their communication facilities and teletypewriter subsidiary, Lorenz, A. G., the International Telephone and Telegraph Corp., operations are impressive.

The first installation of a large-scale electronic data-processing system in Europe is at the Battelle Institute in Frankfurt where Remington Rand have installed a Univac system. A new modern building, complete with air-conditioning and 60-cycle power source was built for this elaborate and new first-class facility. The machine will be used by industry and government as a computing center. I talked to people as far away as Madrid who were attending programming classes in Frankfurt, and many firms are planning to train personnel in the use of this equipment. International Business Machine Corp. will use a no. 650 at Stuttgart for computing service, and plans are being discussed for a no. 705 at some other location in the near future. One of the finest programs of technical development and group research is in the progressive Scandinavian countries. Here the various technical schools have cooperated and the result is an excellent high-speed computer called the BESK. To avoid maintenance requirements, increase its speed, and to enlarge its storage capacity, the Williams Tubes have recently been replaced by a 4,000-word ferrite-core store. These new core matrix boards were assembled at the technical school in Stockholm at minimum cost from cores of General Ceramics manufacture, and they were very proud that it worked perfectly 3 days after installation. Duplicates of this machine have been built at several commercial and governmental installations in Sweden, and a copy is nearing completion in Copenhagen. The University of Lund saved money on their copy by installing a magnetic drum initially.

One cannot help admiring the fact that, in spite of limited capital and resources, each of the smaller countries of Europe has some activity toward building computers. Norway has a small drum machine in the Central Institute at Blindern University, and partly as a result, the government is to receive the first Mercury Computer from Ferranti. The Mathematics Center at Amsterdam built a small relay computer four years ago. Now they have a new electronic core model, and they have built a duplicate for the Fokker Aircraft Company. Because of the interest created the Shell Company bought a Pegasus computer, and the government Telephone & Telegraph laboratory built a series of computers, one of them for mass production. This machine incorporates a novel system of programming, each instruction word includes a "long" and a "short" address plus up to 12 functional operations, each designated by one character.

The inspiration for a number of computer and electronic developments in Europe is the operation known as PTT (Postal, Telegraph and Telephone), which operates the banking system of the various governments. This is the largest single data-processing operation in the world, unless our Social Security tops it. Every day, in each large center in Europe, hundreds of thousands of postal checks are issued, and a statement is mailed each day to every depositor whose account is active. The problem of sorting the paper is a major one, and great interest is prevalent in magnetic ink character recognition. The Holland group is trying to find a method of reading handwriting. The Bull Company in Paris is demonstrating a magnetic-ink coded check sorter. In Switzerland they have punched 40 holes, 1/4 inch diameter, in the checks so they can be sorted, but the result looks like Swiss cheese. Some solution is bound to come to the problem before long.

Switzerland and Italy have no commercial developments in computers as yet. The Technical Highschool at Zurich had the Ermeth built for them by Hasler, A. G. in Bern. International Business Machine Corp. have just dedicated their new research laboratory in Zurich and the director is Dr. Speiser who designed the Ermeth machine. In Italy, Spain and Portugal, the business machines industry is dominated by Olivetti, and it will probably not be too long before some announcements in the electronic field will be forthcoming. Olivetti sponsored research is under way at Pisa University on electronic computer design. A Ferranti computer is in use at the University of Rome, and many Italian banks are using machines such as the Univac no. 120, the IBM no. 604 and the Bull Gamma, all punched-card-programmed electronic calculators.

If punched-card-programmed calculators are included, then the largest producer of electronic computers in Europe is the Compagnie des Machines Bull in Paris. This firm has installed several hundred Gamma machines, largely in banks, and is now starting to produce a new faster model incorporating a magnetic drum with

8,000 words of storage. Magnetic tapes will probably be added also, although there has been little if any effort to develop magnetic tape devices anywhere in Europe. At the other commercial computer factory in France, the Society for Electronics and Automation, Francois Raymond is installing Potter Tape units on the CAB no. 3,000, which is nearing completion, at a price of about $250,000. A still faster model operating at 200-kc will perform multiplication in 0.21-ms, according to the announcements. I learned that a printer, called the "Numerograph," consisting of a cathode-ray tube projection on film, would be delivered on a business-data processing application in March, 1957, but the prototype had not been started as yet. This organization has produced, however, about 50 analog machines, mostly for machine tool control. I visited an installation of the first CAB no. 2,000 digital computer in a defense plant in Paris and I was told it had performed excellently for one year with only part-time maintenance.

There is little doubt that the principal commercial production of electronic computers, especially for export, will come from Great Britain. The Universities have produced an able group of electronic designers, and the knowledge of computer circuitry and component design is on a level with that in the U. S. A number of well financed manufacturers have passed the prototype building stages, and now have a backlog of orders which would probably total over $10 billion. The government, through the National Research and Development Council, is stimulating and supporting developments in this field as evidenced by the granting, through the University Grants Committee, of six Ferranti computers to as many colleges for use in mathematics and research. Export sales to very remote countries are being made, and others considered, without fully considering the need for adequate maintenance facilities. Ferranti have sold machines in Italy, Canada, Sweden, Switzerland and South Africa, and Elliott Bros. will deliver machines in 1957 as far away as Australia from service facilities. Therefore we can assume there would be no hesitation to accept orders from the U. S. whose dollar credits are so very desirable at this time.

British electronics firms operating in their domestic market, are finding, however, that the lack of established sales and service facilities is a serious handicap, especially in the new field of business data-processing. They are following the lead of the U. S. by joining with business machines distributors whose knowledge of system selling and installation is based on sound experience. The machines of Ferranti will be sold by Powers-Samas, and Elliott Bros. have concluded a sales agreement with National Cash Register. British Tabulating Machine Co. has joined with Laboratory for Electronics in Boston. Standard Electric, Electrical and Musical Industries (EMI) Electronics, English Electric and Decca are still independent, but none has faced the sales problems as yet.

No report of British computer progress would be complete without some mention of LEO (Lyons Electronic Office). The Lyons Tea Co. is a large, diversified firm, with 250 bakeries and restaurants and 400 kinds of tea distributed house to house. Even so, it was quite a departure to start building an electronic data-processing machine in 1950. This 6,000-tube machine with mercury delay-line store has been in operation on payrolls since early 1954, and now computes 30,000 checks semi-monthly for the bakeries. A separate subsidiary has been established to build the computers which other firms are ordering, and 70 people are employed. A large co-operative chain will be the first customer for the first of "Leo II" machines, which are four times faster because of a shortening of the mercury lines. Bull or Samas printers will be used for output.

A number of unique design features are included in British computers which we are not using in the U. S. One is nickel delay lines for fast storage, first used in the Nicholas computer built by Elliott Bros. and continued in their newer data-processing models, the no. 404 and no. 405. Nickel lines will be used in the new Ferranti Data-Processor and probably in the EMI transistorized computer. Bull of Paris has incorporated nickel lines in its newest drum Gamma. For bulk storage, however, Elliott Bros. have provided both a 4,096-word drum and a 16,384-word aluminum disc, 1/2 inch thick and 19 inch diameter. This appears to be considerably more simple in construction than most of the magnetic drums which are in almost universal use. Elliott Bros. are also alone in using 35-mm film instead of plastic or mylar for magnetic tape storage, the film movement of 30 inches per second being controlled by the sprocket perforations. Two high-speed wire-matrix data printers are under development which will be used by the various computer manufacturers who wish faster speeds of output than the punched-card tabulators. One by Samas has been demonstrated here by Underwood-Elecom, which represents Samas in the U. S.

In conclusion, I want to emphasize what I believe to be the most pressing problem in the computer industry, not only in all the countries I visited but here at home also. This is the lack of trained manpower to design, build, program, install, and maintain these rather complicated new business tools. I was sorry to see that the colleges and universities are buying machines rather than designing and building their own. It was by this process that all of our present progress was made, and from these design groups have come the electronics engineers who are now able to assist industry in the use of the systems.

I was disappointed to find business machines firms funnelling the cream of all the university design groups into commercial product developments, lured by higher salaries of course. The entire group from BESK at Stockholm has recently moved to Atvidaberg, makers of Facit Calculators. The heads of the design groups at Darmstadt and Munich have gone to Standard, Telefunken, International Business Machines Corp. and Siemens. There is not sufficient training taking place to replace these pioneers, and some unfinished computer projects are left without experienced men to complete the work. The answer is to establish, at once, computer design and operation courses in our universities all over the world, and to increase the training given by manufacturers.

The electronic automation business, like most other highly scientific fields, recognizes few national boundary limitations. We should give technical assistance to less prosperous countries instead of robbing them of their best talent. This does not refer to temporary transfers or exchanges, which are most welcome. One of the most complimentary things I heard about the U. S. was that a college here granted the money to send a scientist over there to help them build an electron microscope. He stayed a year, made friends, and taught a group the techniques he was expert in. They like that much more than just money, and the whole world benefits any time knowledge is spread. Let us do it in the computer business. Let us have an international computer congress soon, and hold it in Europe, because the one thing they don't have is dollars. We have no monopoly on brains, and much can be learned from discussions with the wonderful group of dedicated engineers I met during my trip.

Discussion

Irving Cohen Radio Corporation of America (RCA): What is the present status of the Gottingen machine?

Mr. Calhoun: The status of the Mark III was at the state that I am always told a machine is in when it can not be demonstrated. It is 80 per cent completed.

J. F. Swatton International Business Machine Corp. (IBM): What type transistors are being used in European machines and what comments have you heard on transistor reliability?

Mr. Calhoun: I have heard many remarks that the reliability was now sufficient to get equal results as with tubes. Most of them are buying transistors from Philips in Holland or from Mullard in England, and they are all junction type. They are buying them in Germany for 4 marks, which is about one dollar, each. I saw at least three transistorized computers under construction in Europe which are all going to use these transistors. Most engineers thought that it would be foolish to build a tube machine at this time.

W. K. Halstead (RCA): Can you give some more details of the British machine with the novel approach to programming?

Mr. Calhoun: Not too much. This machine is in paper form and not even in prototype form yet. It is, however, a development of Dr. Kosten and Dr. Van der Poel of the Hague, Holland. Dr. Kosten explained it to me; it follows the Ptera machine, which they built, in logic, but is quite improved. This 15-character portion of the instruction word does permit (according to Dr. Kosten, who has gone now to Delft University as a professor) up to 12 functional operations all combined in one instruction word. For instance, bring the figure from slow memory, put it in fast memory, put it in the accumulator, add it to something else and store it somewhere else, this can all be done in one instruction word. So while the machine is slow, the functional arrangement of the program, it seems to me, is unique, at this point anyway.

Leon Gamen (Sperry Rand Corporation): Without magnetic tapes, what type of data processing problem is typical of the European commercial installations?

Mr. Calhoun: It is similar to talking about data processing installations in the United States two years ago. I would say that's about the lag over there. The data processing installations there have been principally on punch-card-program machines, and 90 per cent of them at the beginning were in banks. 50 per cent of them are still in banks. The reason banks use them over there is not for processing vast quantities of checks, but because every check handled in a bank in Europe has to have the interest calculated on it. There is interest paid on every item in and out of the bank, even if it is one dayand at 1 per cent, it's still calculated on punch cards. So they have a different problem than we do.

B. Housman (IBM): What is the memory speed of the BESK?

Mr. Calhoun: It will perform about 20 additions or 3 multiplications per millisecond. Its memory was a cathode-ray tube and it was described as most resembling a no. 1103 in speed. It now has 40,000 bits of ferrite-core storage and operates at the normal speeds that would result from such design. The core store was built on principles that were pretty well known in this country, as I said.

By the way, this job was done by six completely inexperienced girls hired from a newspaper ad, who took the cores and the etched circuit boards and all the wires home with a soldering iron, and in 6 weeks all six of the women returned with finished matrix boards. They put them into the assembly, wired them laterally, all the boards together, and in three days after they brought them back this memory was working. They only had to replace one ferrite core in the whole 40,000. This is the way they do things over in Europe.

B. Housman (IBM): How strong is the basic research on solid state components such as transistors? Where is this work concentrated?

Mr. Calhoun: I can name a lot of companies. I would not want to rate them; I don't think it would be appropriate here. But the companies in the electronics industry, Philips, Mullard, Standard, Siemens, Lorenz, Telefunken, and IBM are companies who are certainly doing top-level work in this field. Then there are a great many university groups who are doing small amounts of work in the field. There are real, serious, efforts on solid state physics in every company in Europe which has an electronics laboratory. I would say that solid state physics is one of the major efforts of research, and they are developing reliable transistors.

Professor Chorafas (Catholic University): How do you evaluate Professor Piloty's approach in building the Perm with a drum for fast memory?

Mr. Calhoun: I, personally, am a little worried about the high-speed mechanical developments they are getting into in trying to achieve speed. This is just one of them. Some of our other large capacity data-storage devices with low access time also are worrying me. If you try to get a heavy drum to rotate at 15,000 rpm, and try to hold a 1 mill clearance with the head, you have a mechanical problem that can be very severe. They put the ball bearings under high-pressure tension, in order to minimize the runout. They say it's working, that is, it's working in test, but I think that the first one will probably not work perfectly. I am personally afraid of driving mechanics to this extent, because maintenance may become a problem. As soon as we can arrive at non-mechanical methods of getting adequate capacities and speeds of memories, certainly we will have made a great stride.

Professor Chorafas: Do you think that a large business computer like Univac or 705 can develop from the actual European models?

Mr. Calhoun: They think ours are a little too big. They think they would do better to have them just a little bit smaller. But they think their input-output facilities should be as large or better. And they look at our large computers, if I may say so, just a little bit like I looked at the Auto Show last night, and like the French newspapers are reporting it. They just think we do things a little bit too big. I was impressed that we have a little too much rear light on our cars.

Mr. Graney (Westinghouse Electric Corporation): What are the advantages of nickel delay lines over other types of memory devices?

Mr. Calhoun: They are cheaper.

R. C. Dorp (IBM): What future do magnetic drums seem to have in European computers?

Mr. Calhoun: Well, they are like the clutch pedal on a car. They are going, but they are still in everything. There is a magnetic drum on almost every computer I have seen. In every case they hope to replace them.

Mr. Fischer (Naval Training Device Center): Can you give more detail on the aluminum disc memory?

Mr. Calhoun: Yes. The magnetically coated disc revolves in a vertical plane at 1,500 rpm. It has about 40-milliseconds maximum access, and therefore, about 20-milliseconds minimum access. I think they break the records up into 100-character words and they have 64 tracks on each side of the disc. They read both sides of the disc.

The disc is made of a 1/2-inch thick piece of aluminum, 19 inches in diameter, revolving with fixed read-write heads on both sides. I think you can imagine the result. It is very simple; the bearings, mechanics, all are very simple.

A. Steele (IBM World Trade Corporation): Did you see any Ferranti magnetic tape operation, or 35 mm tape operation in England?

Mr. Calhoun: Yes, I think I mentioned that Elliott Bros. are using 35-mm coated film base tape and have used it for some little time. They also, however, are using a 1/4-inch mylar tape in the same system. Ferranti does have some tape operations, however. I believe they have selected the Electrodata tape unit rather than to try to develop their own.

R. E. Montijo (RCA): To what do you attribute the apparent lag in design and development of magnetic tape equipment in Europe?

Mr. Calhoun: I would say the lack of realization in Europe that business data processing is economically feasible. In other words, all the computers that have been built are either for mathematics departments or for scientific research, which did not require magnetic tape. We must admit that we have had only two years actual use of plastic magnetic tape for data processing in the United States, and many problems still remain.

They are just beginning to realize that business could use computers to an advantage. It must be remembered that, as short as five years ago, there was an article in a technical journal in London which stated that one large-scale electronic computer like those in the United States would do all of the computing necessary in England; therefore, there was certainly no need to make any. Now they are all embarrassed

that this was actually thought to be true only five years ago. But England is building computers, and they are going to have lots of them. They will soon have a large business in data-processing equipment.

Harold Kantner (Armour Research Foundation): Can you describe briefly the machine referred to as the "Numerograph" which was attributed to a Paris company?

Mr. Calhoun: There is no prototype built yet. I do know, however, that it is a projection of a cathode-ray tube image in rapid sequence onto film, which is developed, and then printed on photographic paper in a continuous flow process.

W. W. Davis (Naval Ordnance Lab.): Did you see computers being used in industrial control applications?

Mr. Calhoun: No. I went to a number of places to find them also. I was told that Renault Automobile Company in Paris had the greatest automation in Europe. It has been written up as such. I spent a day there and I saw a wonderful example of electromechanical automation, but I did not see one bit of an electronic control. They don't believe in it; they think it's not reliable. They think electric relays and motors can be handled by the ordinary maintenance mechanic, but they are just very afraid of electronic controls. However, a number of firms are making electronic machine tools, individually controlled machine tools, but not very much in electronic process control.

R. O. Skatrud (IBM): Are European countries, or Asian for that matter, developing high-speed computers for applications to defense problems?

Mr. Calhoun: Oh yes, I would say that with most of the first computers, the sales are to defense plants, and to nuclear energy research organizations. In Paris I saw the machine that the Society for Electronics and Automation built for a defense plant, and in England there is some relationship between all the early computers and government defense. The first "Mercury" core-memory computer built in England will be installed by Ferranti in a Norwegian defense establishment, at the Royal Academy of Science in Oslo. The man who will run that, by the way, is known to many of you, Dr. Ernst Selmer, who was the designer of the logic for the Electrodata-datatron.

J. Reitman: (Teleregister Corporation): Did you see any on-line applications in service or prospect?

Mr. Calhoun: The nearest to that would be in Nuremberg, where a large system is being installed in a mail order house, which processes up to 750,000 line items of sales per day. They will have fully transistorized price index, inventory, and billing machines operated direct from the keyboard input of the orders. Funnelled in the most clever manner I have ever seen, the merchandise comes down from five floors, through 25 elevators, to carrier belts; so that the entire order is automatically assembled at one wrapping desk, where the stamp is put on it and it goes to the post office. This is all done by complete automation. They are going to use an on-line operation. As the order arrives, they would code it on a printer-punch, and from the coding everything else—the filling of the order, the billing, the establishment of the proper price and so on—would be handled within an automatic cycle.

J. Reitman: Did you see any large drum storages? What was the largest drum storage you saw?

Mr. Calhoun: I think the largest drum storage was 16,000 words at Bull in Paris, which is the same number of words that are on the Elliott disc I described. Most of the other drums are 4,096 words. That seems to be a standard. I saw very few, if any, smaller drums being constructed, although there were some 2,000-word ones in use. Everyone is going to at least 4,000 or an 8,000 words, and, in the case of Bull, to 16,000 words of storage.

S. Gorn (Moore School of Electical Engineering, University of Pennsylvania): What is the attitude in Europe to building in floating point?

Mr. Calhoun: Built-in floating point is accepted as a proper inclusion in a scientific machine and it is already in about at least 10 out of 35, I would say. I did not make a list of those. In all the new ones that are planned for data processing, of course they're eliminating expensive floating points. I think that's pretty much in line with our United States concept.

Mr. Baker (Rand Corporation): What progress has been made in automatic coding techniques?

Mr. Calhoun: I did not see very much progress in automatic coding. There has been much talk at meetings and discussion, but I was not told that anyone had accomplished automatic coding, which I take to mean putting a program into machine language automatically, not putting data into a coded form automatically. The question could be taken either way. I did see a lot of equipment for putting data into code-form automatically, and that would be automatic coding in one respect.

M. L. Aitel (RCA): Can the training courses in computer techniques be covered adequately by universities, or must industry participate to provide the manpower and money?

Mr. Calhoun: I think the industry must provide most of the money, computers, and some of the manpower, and I think the colleges must be encouraged and supported to do more of the teaching. But I think industry must take a very heavy responsibility in the training of people for the data processing industry, because it's going to take a lot of them.

Much of this will have to be done after college age also, but we must not fail to bring along a large group of basically trained people out of our universities, people capable of becoming technically trained in this specific art, at least. We must make high school mathematics and science courses more attractive, so that everyone won't just study sociology.

Evaluation of New Computer Components, Equipments, and Systems for Naval Use

L. D. WHITELOCK

THE THEME of this conference, "New Developments in Computers" is most appropriate at this time as we enter the first generation of solid state computers, and an era of advanced systems design. Let us consider briefly why new developments occur. Some new developments are made to meet a need expressed by a customer, or user; others are made to meet their anticipated needs. How well the user's needs are met in contrast with the capabilities and costs of available equipment determines the degree of success of any new development. However, the user's view of a new development is not always as enthusiastic as that of its creator. The user's evaluation of the suitability and acceptability of the new development may differ from that of the creator because of variations in the method of evaluation, in technical background, and in the scope of related information, such as "what is available from competitors." Fortunately, there are many prospective users of computers, and their needs differ to such an extent that the field of interest for new developments is very wide. There is a natural urge for the user to partially or fully evaluate all

L. D. WHITELOCK is with the Department of the Navy, Bureau of Ships, Washington, D. C.

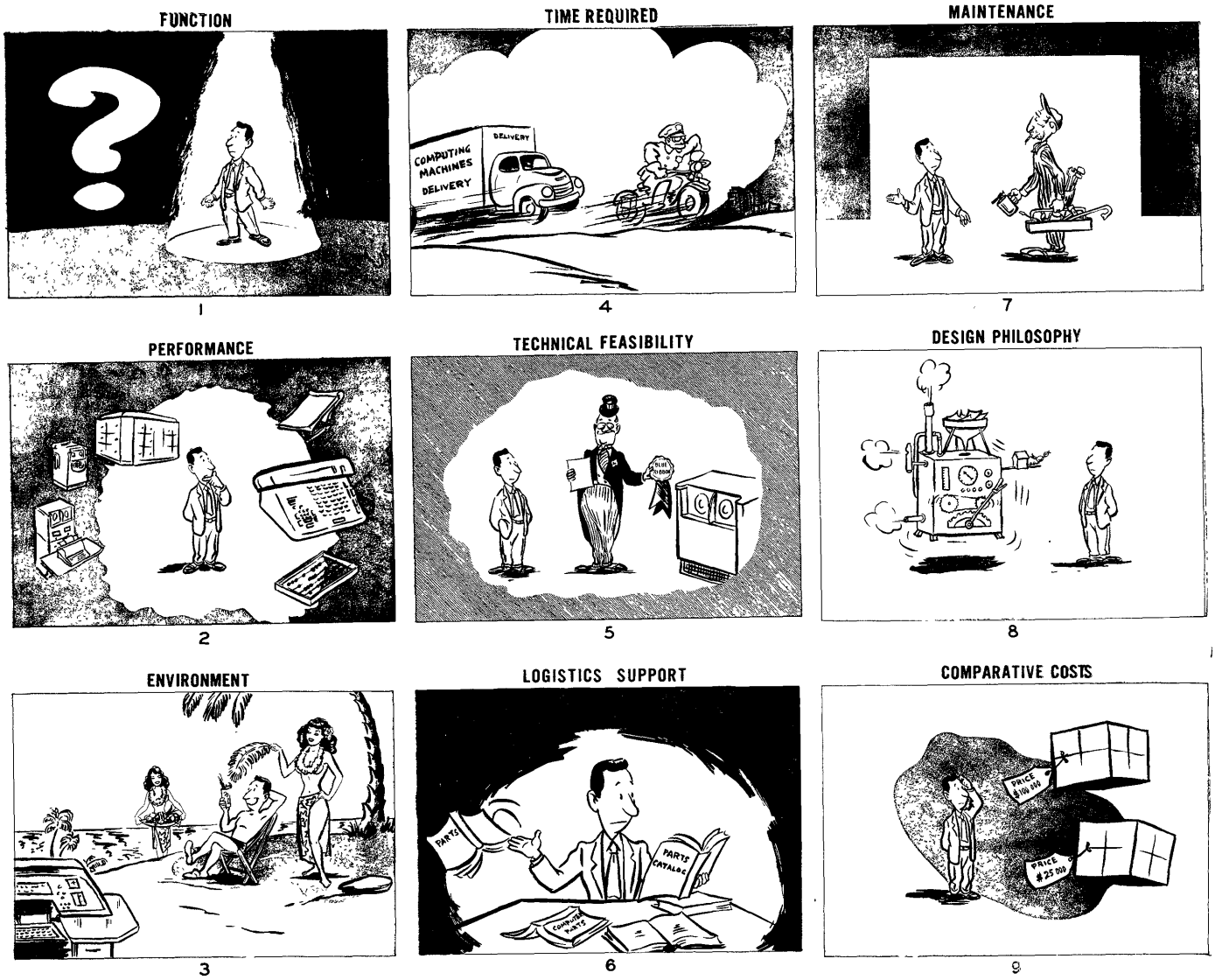


Fig. 1. Evaluation factors

new developments within his field of interest. Obviously, poorly conceived and poorly executed developments fall by the wayside because of lack of customer, or user acceptance.

It may be of interest to the relatively new computer industry to look at some brief examples, and to review the general philosophy of user evaluation and user needs. The user in this case is the Bureau of Ships. This Bureau is an extensive user of digital computer components, equipment, and systems in the following categories:

1. Shore based, commercial design.
2. Shore based, research, development and production to military performance specifications.
3. Shipboard, research, development and production to military performance specifications.

The same basic approach to evaluation is used regardless of the equipment category, and regardless of whether or not the equipment or system exists or has yet to be developed. The philosophy of approach is keyed to nine basic evaluation factors. For each specific evaluation, the basic evaluation factors are expanded by appropriate, carefully considered questions. The basic factors, Fig. 1, together with sample questions to illustrate the method are the following:

1. Function. What is the job to be done? Is it a necessary job? Can it be modified or combined with other functions to make the equipment less complex?

2. Performance. Is it clearly defined technically? Have we asked for too much? Too little? Are tolerances reasonable with respect to the intended use? Will commercial equipment do? Are there equipments with similar performance which should be considered? What is the efficiency of performance?

3. Environment. Will it be installed on shipboard? On shore? Indoors? Outdoors? Does it meet the temperature, humidity, shock, vibration, and similar requirements for this application?

4. Time required. When must the equipment be delivered and installed? What delay can be tolerated? Is the available lead time realistic? What is time phasing with related items?

5. Technical feasibility. Has technical feasibility been proved? Have Navy laboratories evaluated the project? Is it expected to be proved with the test of equipment being produced under a research and development contract? Are there alternate approaches with more promise?

6. Logistic support. How many equipments are expected to be involved? Where and when will equipment be used? Where will major parts supplies be located? What is the lead time for ordering replacement parts?

7. Maintenance. Where will equipment be located? Who will maintain it? Are any unusual maintenance problems expected? Does the equipment design assure accessibility for maintenance? Are parts

available? Is special training required for maintenance personnel?

8. Design philosophy. Is the design conservative? Critical? Reliable? How does it compare with the best in the industry? Are standard parts used where possible?

9. Comparative costs. What are the alternate approaches which appear to be technically feasible? What is the over-all cost of each approach? Is the over-all cost reasonable for the function to be performed? Should we buy or rent? Is the output the same for each alternative? What is the cost per unit of output for each alternative?

The foregoing factors, after collecting information and facts in the general areas indicated by the sample questions, will usually permit a sound choice with a minimum of deliberation. Many times the final choice is simplified by marked differences in costs of alternatives or by a drastic reduction of the number of alternatives. Two abbreviated examples are given in the following paragraphs.

In the first example, an evaluation or analysis was made of equipment suitable for printing 1,000,000 lines per week, 120 characters per line, from magnetic tape. Equipment considered was either available or was available with a moderate amount of additional development. Equipment could be operated in three shifts if necessary. Of the seven initial alternatives, three were eliminated by the "time required" and "technical feasibility" factors, and further evaluation-factor analysis was made of the remaining four alternatives. After consideration of printing speed, efficiency, operating labor, maintenance labor, overhead, replacement parts, amortization (or depreciation) on a 10 year basis, night differentials, and the cost of developmental units where required, the over-all cost per week of each alternative was calculated with the results as shown in Table I.

Table I indicates that alternatives B and C are the only feasible selections, with final choice dependent on availability of funds, policy with respect to rental versus purchase, and similar factors.

Table I. Comparative Costs

Equipment to Print 1,000,000 Lines per Week from Magnetic Tape

	Alternative, Dollars			
Cost	A	B	C	D
Per week	15,840	1,241	980	8,580
Per year	823,680	64,532	50,960	446,160
Difference	772,720	13,572	0	395,200

A = multiple printers.
B = high speed printer, rental.
C = high speed printer, purchase.
D = alternate multiple printers.

In the second example, an evaluation was made of computers appropriate for the variety and volume of work indicated by a detailed survey of representative problems. The evaluation was made by a panel selected from personnel competent in the computer research, development, and production field, and from the computer application and programming field. The full details of this evaluation are considered to be beyond the scope of this paper. However, in summary, several alternatives were outlined and the evaluation-factor approach applied. Information was developed concerning estimated times to do the sample problems on each computer; total estimated volume of work and type of work load; availability of computer time on a rental basis; purchase versus rental of a computer; availability, price and operational cost of available computers; comparisons of hand, punched card and high-speed computer costs for sample jobs; and the relationship of total operational cost per hour to the cost of handling 1,000,000 characters of input. The latter relationship is summarized in Table II.

Table II. Computer Comparisons

Computer Type	Input Speed Characters/ Second	Est. Total Operational Cost, Dollars, per Hour*	Cost, Dollars, to Process 1,000,000 Characters of Input
A	10,000	110	3.05
B	37	110	.825.00
C	8	10	406.00
D	200	55	89.20

* Includes cost of programmers, operators and maintenance.

In the foregoing example, final evaluation-factor analysis resulted in a reduction of alternatives to only one logical choice.

These examples cover evaluation of equipment available at the time of evaluation or expected to be available shortly thereafter. In many military systems requirements, the need either cannot be met with available equipment or it can be only partially met with such equipment. In such cases, the evaluation-factor analysis is made to determine what requirements should be included in performance specifications on which research and development or production contracts can be based. Performance specifications always include references to other military specifications which have been developed over the years to cover design and test criteria found essential to reliable operation of electronic equipment in a military environment. The most important of these is "Electronic Equipment, Naval Ship and Shore: General Specification."[1] This general specification covers construction practices and the conditions under which equipment for Naval ship or shore use must operate. For example, Table III shows the temperature range requirements as listed in the general specification. The equipment class is identified for a particular equipment in the performance specification.

The general specification stresses the reliability of electronics parts as one key to equipment reliability. Many material and parts specifications and military standards are referenced therein. Two standards of particular importance are "Electronic Equipment Parts" and "Test Methods for Electronic and Electric Component Parts."[2,3] The current situation and probable trends in the field of standard electronic parts for military equipment is covered in considerable detail by a paper by George C. Neuschaefer.[4]

The general specification also stresses the importance of reliability, simplicity, and ease of installation and maintenance to military equipment. Extensive studies of electronic failures over the past several years have shown that the design engineer has the power to improve these factors materially over past performance. In addition to the benefit derived from the reliable parts program, the design engineer must design the system for reliability and simplicity. He must make conservative parts applications with due consideration to the problems of stability and reproducibility. While this area of discussion is vitally important to military electronics in general, it assumes even greater importance in the design of computers for military applications. The tremendous number of components and circuits in computers makes the achievement of reliability, simplicity, and ease of maintenance a real challenge to the designer. To those of you who wish more detail on this subject, I strongly recommend that you read a paper by N. H. Taylor.[5]

Have we any proof that the application of the principles and requirements of the general specification[1] to computer design and development is worthwhile? We are positive we have. During the past few years, several developmental computers constructed for shore use and following, in general, the requirements of the general specification have performed with outstanding reliability and maintainability. However, these computers could not be readily used aboard ship because of their size and power requirements. The rapid

Table III. Temperature Ranges, Ambient

Class	Operating, C	Nonoperating, C	Type
1	−54 to +65	−62 to +75	shore–exposed
2	−28 to +65	−62 to +75	shipboard–exposed
3	−40 to +50	−62 to +75	shore–unheated shelter
4	− 0 to +50	−62 to +75	ship/shore–housed-heated shelter

development of small, low power, solid state computers, such as those described in papers presented in sessions of this conference, bring computers which will meet the general specification requirements for shipboard use closer to reality. The ability of such equipment to withstand shock, vibration, humidity, and other shipboard environmental conditions now becomes important.

The use of digital computers in the Navy is increasing in three major areas: business and logistics applications, scientific problems, and military systems for ship and shore. Future requirements in these areas cannot be covered in detail in this paper. However, some general development trends or goals to meet needs now existing or foreseen are outlined as follows:

a. Computer speed: Continued improvements in computer speeds are essential. Many applications require multiple-problem use of a computer, or multiple computers, through time sharing. Real time operation is often required. Obviously, the faster computer can handle more problems or larger problems, which further enhances the inherent flexibility of the digital computer. Increased speed does not necessarily mean that the size of the computer is increased; it may decrease in size. It does not seem unreasonable technically to expect in the near future addition times of 1 microsecond with a correspondingly low multiplication time. If such computers follow the pattern of past generations of computers, speed increases will result in a lower over-all cost per unit of data processed.

b. Computer memory: The speed of random-access computer memories is not keeping pace with speed improvements in logical circuitry where speeds measured in milli-microseconds appear attainable. A high speed memory with access time under 1 microsecond, and with power requirements which can be supplied by transistors is urgently needed. Present ferrite-core memories will be much more valuable if the practicability of operating them with 5 microsecond access in assemblies of up to 100,000 words with reasonable driving power is demonstrated.

c. Visual displays: Many applications require visual displays of computer output. This application is expected to increase and will require simplified methods of presenting numerals, letters, and other characters on a flickerless display either for direct viewing, for projection, or for large-scale direct viewing. Simplified methods of analog-to-digital and digital-to-analog conversion are required both for special computer inputs and outputs, and for use with displays. However, direct operation of displays from computer output without intermediate conversion is a possibility worthy of further thought.

d. Computer physical characteristics: Present vacuum tube versions of computers are too large, require too much power, and lack the reliability necessary for many applications. It is now certain that size and power requirements can be reduced by factors of 20 or more, and reliability greatly improved by the use of solid-state electronics. Militarized versions will be required.

e. High speed printers: Printing speeds of 600 to 1,500 lines per minute seem to cover most applications. However, simplicity and reliability need to be improved, and the present costs appear high. Printing by other than mechanical means seems to offer some promise to simplify these devices.

f. Standardization: The difficulty of standardization in a rapidly developing field may delay action in areas where standardization now appears feasible. Standardization of magnetic tapes, tape drives, and tape coding would be very helpful. The panel discussion on "Standardization of Magnetic Tape Records" at the 1955 Eastern Joint Computer Conference was a step in the right direction.

In conclusion, let us review the evaluation-factors. They are: function, performance, environment, time required, technical feasibility, logistics support, maintenance, design philosophy, and comparative costs. We have found the philosophy of the evaluation-factor approach valuable in making decisions either as to what to buy or what to develop. The decisions reached as a result of such analysis appear to be valid based on the five steps in decision making as defined in the classical scholastic manner by the University of Pittsburgh, School of Business Administration. The five steps are:

1. Define issue.
2. Analyze existing situation; fact finding.
3. Calculate alternatives.
   a. What are they?
   b. What are their consequences?
4. Deliberation.
5. Choice.

Note that the evaluation-factor analysis covers the first 3 steps, thus making the fourth and fifth steps of deliberation and choice follow naturally and almost automatically.

References

1. Electronic Equipment, Naval Ship and Shore: General Specification. *MIL-E-16400A-(SHIPS)*. Bureau of Ships, Washington, D. C.

2. Electronic Equipment Parts. *MIL-STD-242. Ibid.*

3. Test Methods for Electronic and Electric Component Parts. *MIL-STD-202. Ibid.*

4. Standard Parts Can Be Versatile. **G. C. Neuschaefer.** Third National Symposium on Reliability and Quality Control, Jan. 14–16, 1957, Washington, D. C.

5. Designing for Reliability. **N. H. Taylor.** *Technical Report no. 102*, Massachusetts Institute of Technology, Cambridge, Mass., Dec. 9, 1955.

Discussion

Mr. McKenna (Wheelock Signals): Will you predict the future of the electromechanical relay used in the computer field; i.e., do you see a trend against it or not, and why? Please comment on this subject from the international point of view.

Mr. Whitelock: The use of relays depends on the type of computer. In the case of the computers we are interested in, relays are used very little except in connection with circuits for performing specific tests, marginal checking, or similar applications.

Mr. Calhoun: From an international standpoint, in a one-minute answer, I'd say all the relay computers are being dismantled. The first one in Stockholm, the Bark, which worked very well is dismantled and thrown away. The reasons are that the cost of running slow relay computers is just as great or greater than running fast electronic computers. The cost of programming, the cost of maintenance, the cost of operating personnel are just as high, and, therefore, I think electronic methods rather than mechanical relays will certainly take the place of relays in the computer business. I think that relays are being improved, but they are still too slow for computers.

D. Jackson (Remington Rand, Div. of Sperry Rand Corp.): Will the Bureau of Ships consider the use of limited techniques, using transistors, in tactical shipboard equipment?

Mr. Whitelock: The answer is yes.

Mr. Fischer (Naval Training Device Center): Are shipboard computers supposed to meet all the rough and rigid requirements of corrosion resistance, shock, vibration, and so forth, required of other operational gear?

Mr. Whitelock: That is correct.

A. S. Goble (International Business Machine Corp.): Internal speeds were mentioned, but magnetic tape input speeds were not. What character rates are desired?

Mr. Whitelock: The present rates of 10 to 20,000 characters per second take care of most of our problems. In many of the military systems, the tape input is really not used, except for very special inputs, because usually inputs are keyed to other equipment, thus placing a premium on simplified conversion to feed directly into the computer.

H. N. Laden (C. & O. Railway): Has the Bureau of Ships evaluated plastic versus metallic tape? What was the outcome?

Mr. Whitelock: We use both types. I would not say we have thoroughly evaluated them at the moment, that is, not in such a manner that we can say one is better than the other.

Chairman Leas: Mr. J. J. Lamb, of Sperry Rand, who is chairman of the computer and data processing sections of the Radio Electronic Television Manufacturers Association, would like the group to be informed that a panel on automation and computers of RETMA is now working on various tape standardization proposals.

The Transac S-1000 Computer

J. L. MADDOX J. B. O'TOOLE S. Y. WONG

Synopsis: The Transac S-1000 is a scientific-type computer mechanized with direct-coupled transistor circuits. Double-address instructions are employed with a 36-binary-digit word length. A 4,096-word magnetic-core memory is used for high-speed storage. The machine is designed to accommodate such peripheral equipment as magnetic drum, magnetic tape, punched card, and paper tape. The packaging consists of printed circuitry so that the entire control computer occupies the volume allowed in a standard office desk (approximately 36 cubic feet). The total power dissipation is about 1.2 kilowatts. The speed of operation is at least as fast and in most cases faster then its vacuum-tube counterparts.

ONE OF of the greatest impacts on the computer world was the announcement of the transistor. Because of the general characteristics of transistors in contrast to vacuum tubes, digital computers were to become smaller, to require less power, and consequently to find a greater variety of applications. The development of digital computers using transistor circuits parallels the development of semiconductor devices and associated components. The advantages of transistors over vacuum tubes, however, was only a vision until surface-barrier transistors were developed, which compete with vacuum tubes in speed.

The announcement of direct-coupled transistor circuits[1] added impetus to the concept of small physical size and low power consumption. The design and construction of Transac S-1000 is a study of the application of direct-coupled transistor circuits to large-scale data-processing systems. The instruction list classifies it as a scientific computer.

J. B. O'TOOLE is with Hughes Aircraft Company, Culver City, Calif.; J. L. MADDOX and S. Y. WONG are with the Philco Corporation, G. and I. Division, Philadelphia, Pa.

The computer proper, which consists of approximately 7000 transistors, a smaller number of resistors, and very few capacitors, is packaged on 132 printed wiring boards. The packaging philosophy was derived from the requirement that the computer should be included in a standard office desk which allows a volume of approximately 36 cubic feet, of which about half is used for knee space and a storage drawer. Also packaged in this space is a 147,456-bit magnetic-core memory which utilizes semiconductor components exclusively.*

List of Symbols

A = accumulator register
( ) = contents of
Q = multiplier register
X = exchange register
bit = binary digit
PCR = program-control register
MAR = memory-address register
A_l = left half of accumulator-register
A_r = right half of accumulator-register
MDR = memory-buffer register
PAC = program-address counter
TSR = temporary storage for repeat
u = u portion of command
v = v portion of command
s = modifier for u
t = modifier for v
$E(u)$ = normal transfer of (u)
$S(u)$ = split transfer of (u)
(u_0) = whole of u, 36 bits
(u_1) = right 12 bits of u
(u_2) = middle 12 bits of u
(u_3) = left 12 bits of u
$(X)'$ = *one's* complement of (X)
$(X)Y$ = transfer (X) to Y
$\oplus$ = addition without carry
$\cap$ = logical product
U = logical alternation (inclusive)

The Logical System

The logic of the system may be divided into storage equipment and control equipment. The storage equipment consists of registers, counters, gates, and logical networks such as a subtracter. The control equipment sequences the storage equipment to perform the necessary operations.

* Developed and constructed by Remington Rand Univac, ERA Division of Sperry Rand

Storage Equipment

The storage equipment is outlined in the block diagram of Fig. 1. The storage equipment of the computer proper may be divided into program section and arithmetic section. The memory-data register (MDR), which is an integral part of the memory, is a 36-bit register acting as a buffer storage between the memory and the program and arithmetic sections. The exchange register (X), a 36-bit double-rank register, performs the double duty of handling operands for arithmetic operations, as well as serving as the main terminal for information coming in and out of the computer. The gates between the X and MDR are arranged so that 12-bit words may be handled as well as the normal 36. The X-register is double rank to accommodate the formation of the *one's* complement of a number without involving the accumulator (A_L,A_R) and the multiplier-quotient register (Q).

The gates between the master and slave of the X-register, and the gates from the Q-register to the X-register are arranged in a manner to facilitate the logical operations, which are described in the instructions. The accumulator is a 72-bit register (double-word length) to accommodate double-precision multiplication without destroying the multiplier, which is contained in the Q-register. The slave ranks of the A- and X-registers are not gated but tied directly to the subtracter network, such that the subtrahend is contained in the X-register and the minuend is contained in the A-register. The difference (output from the subtracter), is gated to the master rank of the accumulator. Practically all of the transfers are done on the clear-transfer basis. Since 1's complement arithmetic is performed in the computer, the accumulator is designed to perform left-circular shifts (end around). Likewise the Q-register is a left-circular shifting register which contains the multiplier during multiplication and the quotient at the end of division.

Since the accumulator is a 72-bit register, the subtracter network is required to have 72 stages. Addition is performed by complementing the contents of the X-register. The design of the subtracter more than any other unit, with the exception of the memory, determines the speed of the computer because of borrow propagation. Since speed was not the prime objective, no special logical techniques were employed to speed up the borrow propagation, such as asynchronous sensing. With direct-coupled circuits, the borrow line passing through a stage switches, at most, one transistor. This means that the maximum time for borrow propagation, which is the time used, is 72 times the average switching time of a transistor in a common-emitter configuration.

The double-address instruction being performed is contained in the 36-bit program control register (PCR). The 13-bit memory address register (MAR) is tied directly to the selection network of the magnetic core memory. The 12-bit program address register (PAC) contains the address of the next consecutive instruction to be performed. The gates from the MAR to the PAC are arranged so that one is added to the contents of MAR during the transfer. The 12-bit temporary storage for repeat register (TSR) contains the address of the instruction to be jumped to at the completion of a repeat operation.

The counter shown in the block diagram of Fig. 1, is called the "shifting counter" since in a shift instruction the contents of the v address of PCR are transferred to the counter, to count the number of shifts performed. Since it is a subtracting type counter, it is also employed to solve the modular equation of the scale-factor instruction. The number of steps in the multiplication and division algorithms are also controlled by the counter

Control Equipment

The various control units used are illustrated by the block diagram of Fig. 2. The responsibilities may be stated as follows:

1. Program control: The program control is responsible for sequencing the instructions of the program, and initiating the instruction control.

2. Repeat control: The repeat control has a function similar to the program control, except that it modifies the two addresses of an instruction that is being repeated. It is also responsible for determining the number of times the repeated instruction has been executed.

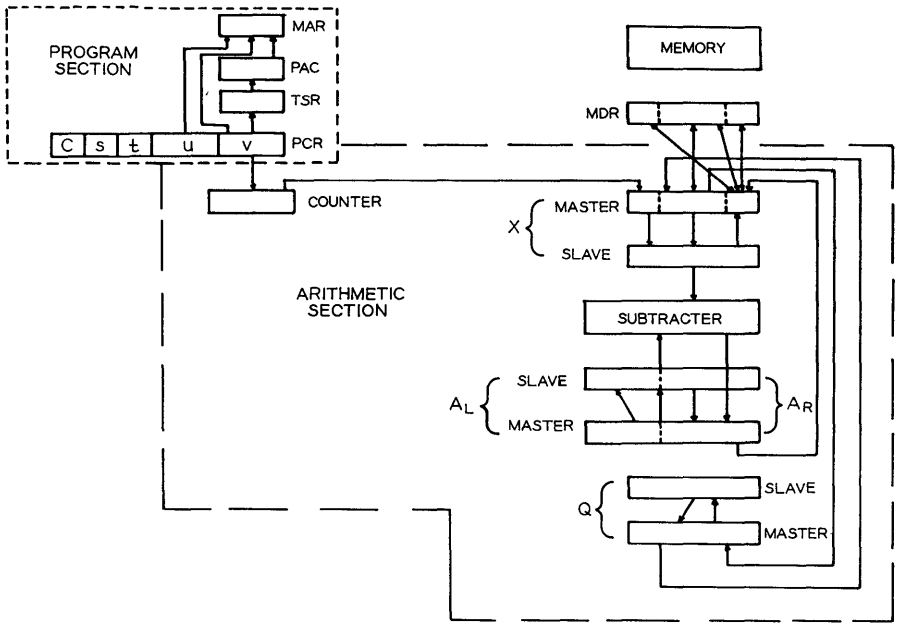


Fig. 1. Block diagram of storage equipment

3. Instruction control: The instruction control is responsible for positioning operands and results that are processed by the arithmetic or input-output controls.

4. Arithmetic control: The arithmetic control sequences the clears and transfer equipment of the arithmetic section to perform: addition, subtraction, multiplication, division, shifting.

5. Input-output control: The input-output control acts as a buffer between the computer and input-output devices.

The underlying, unifying philosophy in the design of controls, is that each is composed of several units, in such a way that each unit performs a certain operation (a micro instruction, for example), and upon execution of its function, routes the control signal to another unit. The instruction code determines a certain path through the various units. The routing of control signals for a given list of instructions makes the designing almost a problem in combinatorial analysis.

Instruction

Composition of an Instruction. An instruction word consists of 36 bits, which may be denoted by $x_{35}, x_{34}, \ldots, x_0$. The portions of the word are described in accordance with the following scheme:

Command Portion	s, Modifier	t, Modifier	u, Portion	v, Portion
$X_{35}, \ldots, X_{30}$	$X_{29}, \ldots, X_{27}$	$X_{26}, \ldots, X_{24}$	$X_{23}, \ldots, X_{12}$	$X_{11}, \ldots, X_0$

An operator uses the octal system of notation for coding the instructions.

The command portion of the instruction tells the function of the instruction, e.g., addition. Since there are six bits available, the machine may accommodate $2^6 = 64$ instructions. Not all of these instructions, however, are recognized as meaningful by the computer. If the computer is directed to execute a meaningless instruction it stops, and a fault indicator is illuminated.

For most instruction the u and v portions of the instruction are memory addresses for datum words that are used as operands, or one of them is the memory address at which the result of the operation is stored. The rule admits exceptions. For example: in some instructions the v portion of the instruction is not a memory address, rather it is the number of places a register is to be shifted. The u and v portions of some instructions are the addresses to which a "jump" is to be made. The list of instruction makes clear the use to which u, v are put for each instruction.

The s, t modifiers of an instruction word determine the manner in which the u, v portions respectively are to be interpreted. The general rule is that if $s=0, 1, 2, 3$ or $t=0, 1, 2, 3$, the u portion of the instruction, or v portion, is a memory address. The modifier does not indicate whether one is reading from, or writing into, the memory address indicated by u or v; it indicates merely that the memory address is referenced. If the

modifier is 0, the whole word of the memory address is referenced. If the modifier is 1, 2, 3, the right 12 bits, middle 12 bits, and left 12 bits respectively of the word of the memory address are referenced. Whether writing into or reading from a memory address takes place is made clear from the description of each instruction. If $s=6, 7$, u is not interpreted as a memory address at all; rather the A, Q registers respectively are referenced. By the same token, if $t=6, 7$, v is not a memory address, and the A, Q registers respectively are referenced. There are few instructions in which 4, 5 are admissible modifiers.

For each admissible instruction there are certain values of the s and t modifiers that are recognized as meaningless by the computer. If the computer attempts to execute an instruction with a meaningless modifier it stops, and a fault light is illuminated.

Types of Instructions. There are three types of instructions:

a. Ordinary instructions: This class comprises almost all instructions. A number of instructions facilitate the handling of data, such as the different types of transmit-data instructions, the logical-multiply, and logical-substitute instructions.

b. Input-output instructions: There are six instructions for the input-output equipments: An interlock jump instruction is provided that permits optimal use of the computer while the input-output devices are being used.

c. Repeat instruction: It causes the instruction obtained from the next memory address to be repeated the number of times indicates by its u portion, each time increasing the u, v addresses of the repeated instruction by s_0, t_0 respectively, where s_0, t_0 are the s, t modifiers of the repeat instruction. At the end of the repeat, a jump is then made to the v address of the repeat instruction.

List of Instructions. The system of coding and arithmetic is *one's* complement. If therefore n bits are transferred to a register of p bits (where $p>n$), the n bits are transferred, keeping their relative order, to the right hand of the register. The remaining $p-n$ bits are made equal to the left bit of the n bit word. Such a transfer is used for most instructions. They are called "normal" instructions.

There is another method of transfer. When a word of n bits is transferred to a p bit register, where $p>n$, the remaining $p-n$ bits are equal to zero. There are a few instructions during which a transfer takes place in this fashion. They are called "split" instructions.

In the following list of instructions, an arrow indicates that the data in the register occurring before the arrow are transmitted to the register indicated after the arrow. If u is a memory address or register, (u) indicates the contents of that memory address. $E(u)$ indicates that the contents of u is transferred in normal fashion. $S(u)$ indicates the contents of u, if transferred to a larger register, is transmitted in split fashion. The right, middle, and left 12 bits of the word at memory location u are indicated by (u_1), (u_2), (u_3) respectively. The whole word is indicated by (u_0).

The coding, admissible modifiers, name, and function of each meaningful instruction is given in the following list. In general, the description remains accurate for the case other than $s=t=0$ if the interpretation given under the composition of an instruction is adopted.

11,*s,t,u,v.* Transmit Positive. $s, t=0, 1, 2, 3, 6, 7$. $E(u_s)\rightarrow v_t$. If $t=6, 7$, left shift A, Q resp. by v places.

12,*s,t,u,v.* Split Positive Transmit. $s, t=0, 1, 2, 3, 6, 7$. $S(u_s)\rightarrow v_t$. If $t=6, 7$, left shift A, Q resp. by v places.

13,*s,t,u,v.* Transmit Negative. $s, t=0, 1, 2, 3, 6, 7$. $(E(u_s))'\rightarrow v_t$. If $t=6, 7$, left shift, A, Q resp. v places.

14,*s,t,u,v.* Split Negative Transmit. $s, t=0, 1, 2, 3, 6, 7$. $(S(u_s))'\rightarrow v_t$. If $t=6, 7$, left shift A, Q resp. v places.

21,*s,t,u,v.* Replace Add. $s, t=0, 1, 2, 3, 6, 7$. $E(u_s)+E(v_t)\rightarrow a_s$.

22,*s,t,u,v.* Add Modular. $s, t=0, 1, 2, 3, 6, 7$. $E(u_s)+E(v_t)-E(Q)\rightarrow u_s$, if $E(u_s)+E(v_t)-E(Q)\geq 0$. Otherwise $E(u_s)+E(v_t)\rightarrow u_s$.

23,*s,t,u,v.* Replace Subtract. $s, t=0, 1, 2, 3, 6, 7$. $E(u_s)-E(v_t)\rightarrow u_s$.

24,*s,t,u,v.* Subtract Modular. $s, t=0, 1, 2, 3, 6, 7$. $E(u_s)-E(v_t)\rightarrow u_s$, if $E(u_s)-E(v_t)\geq 0$. Otherwise, $E(u_s)-E(v_t)+E(Q)\rightarrow u_s$.

27,*s,t,u,v.* Replace Add without carry. $s, t=0, 1, 2, 3, 6, 7$. $S(u_s)\oplus S(v_t)\oplus(A_L)\rightarrow u_s$, where $\oplus$ denotes the sum without carry.

32,*s,t,u,v.* Split Add. $s, t=0, 1, 2, 3, 6, 7$. $(A)+S(u_s)\rightarrow v_t$. If $t=6, 7$, then left shift A, Q, resp. v places.

34,*s,t,u,v.* Split Subtract. $s, t=0, 1, 2, 3, 6, 7$. $(A)-S(u_s)\rightarrow v_t$. If $t=6, 7$, left shift A, Q resp. v places.

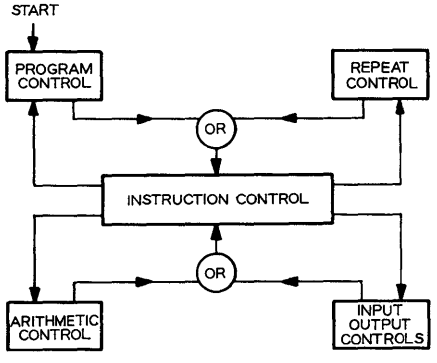


Fig. 2. Block diagram of controls

35,*s,t,u,v.* Ordinary Add. $s, t=0, 1, 2, 3, 6, 7$. $(A)+E(u_s)\rightarrow v_t$. If $t=6, 7$, then left shift A, Q resp. by v places.

36,*s,t,u,v.* Ordinary Subtract. $s, t=0, 1, 2, 3, 6, 7$. $(A)-E(u_s)\rightarrow v_t$. If $t=6, 7$, then left shift A, Q resp. v places.

41,*s,t,u,v.* Index. $s=0, 1, 2, 3, 6, 7$; $t=0$. $E(u_s)-1\rightarrow u_s$ and jump to v, if $E(u_s)-1\geq 0$. Otherwise continue with present sequence of instructions (without transfer of data).

43,*s,t,u,v.* Subtract Modular. $s=0, 1, 2, 3, 6, 7$. $t=0, 1$. Sense $(A)-E(u_s)$ for sign. If $t=0$, jump to v on positive sign; if $t=1$, jump to v on negative sign. The contents of the registers are undisturbed.

42,*s,t,u,v.* Equality Jump. $s=0, 1, 2, 3, 6, 7$; $t=0, 1$. Make decision on criterion $(A)=E(u_s)$. If $t=0$, jump on equality; if $t=1$, jump on inequality. The contents of the registers are unchanged.

44,*s,t,u,v.* Shift Jump. $s=0, 1$; $t=6, 7$. Sense sign of A, Q (if $t=6, 7$ resp.). If negative, jump to u; if non-negative, jump to v. If $s=1$, shift register 1 place left.

45,*s,t,u,v.* Optional Jump or Stop. $s=0, 1, 2, 3, 4$; $t=1, 2, 3, 4, 5$. Stop if $t=5$ or if $t-th$ "stop" switch is on. If not stop, then jump to u if $s-th$ "jump" switch is on and if $s=1, 2, 3, 4$; jump to v if $s-th$ "jump" switch is off and if $s=1, 2, 3, 4$ or if $s=0$.

46,*s,t,u,v.* Return Jump. $s=0, 1, 2, 3, 6, 7$; $t=0$. $(PAC)+1\rightarrow u_s$. Then jump to v.

51,*s,t,u,v.* Logical Multiply. $s, t=0, 1, 2, 3, 6, 7$. $S(u_s)\cap S(Q)\rightarrow v_t$. ($\cap$ denotes the logical product.)

52,*s,t,u,v.* Logical Multiply Add. $s, t=0, 1, 2, 3, 6, 7$. $(A)+(S(u_s)\cap S(Q))\rightarrow v_t$.

53,*s,t,u,v.* Logical Substitute. $s, t=0, 1, 2, 3, 6, 7$. $(S(Q)\cap(u_s))\cup(S(Q)'\cap(v_t))\rightarrow v_t$.

54,*s,t,u,v.* Shift accumulator left. $s=0, 1, 2, 3, 6, 7$; $t=6, 7$. If $s=6$, shift (A) v places left. If $s\neq 6$, $E(u_s)\rightarrow A$, shift $(A)v$ places, then $(A)\rightarrow u_s$.

55,*s,t,u,v.* Shift Q-register left. $s=0, 1, 2, 3, 6, 7$; $t=6, 7$. If $s=6$, shift (A) v places left. If $s\neq 6$, $S(u_s)\rightarrow A$, shift (A) v places left, then $(A)\rightarrow u_s$.

56,*s,t,u,v.* Expand transfer. $s=0, 1, 2, 3, 6, 7$; $t=0$. Shift (A) left v places. Then $S(Q)\cap S(A)\rightarrow u_s$.

61,*s,t,u,v.* Magnetic drum is involved. $s=0$ write onto drum, $s=1$ read from drum, u specifies address on drum, v specifies address in magnetic core memory. (Used in conjunction with repeat.)

62,*s,t,u,v.* Magnetic tape is involved. t designates which tape unit. u designates position on tape (in this case, t may share bits of u portion to increase the number of possible tape units). v designates the address in the magnetic core memory of the computer, and s designates whether the instruction is read, write, advance tape, or back tape. (Used in conjunction with repeat.)

63,s,t,u,v. Punch card reproducer is involved. s designates read or punch. u designates number of cards involved. v designates starting address in the magnetic core memory of the computer.

64,s,t,u,v. Print and punch. $s=1, 2, 3$; $t=0, 1, 2, 3, 6, 7$. Transfer right 6 (or 7 bits) of (v_t) to specified output device. If $s=1, 2, 3$ the output device is the printer and reperforator, high-speed punch, printer, respectively.

65,s,t,u,v. Read in. $s=0, 1$; $t=0, 1, 2, 3, 6, 7$. Transfer right 6, (or 7 bits), of input device to v_t. If $s=0, 1$, the device specified is the low-speed reader, high-speed reader respectively.

66,s,t,u,v. Interlock jump. $s=0, 1, 2, 3$; $t=0$. If specified input-output device is in operation, jump to u. Otherwise, jump to v. $s=0, 1, 2, 3, 4, 5$ specifies the keyboard, high-speed reader, high-speed punch, printer magnetic tape, punch cards respectively.

71,s,t,u,v. Multiply. $s, t=0, 1, 2, 3, 6, 7$. $E(u_s)\times E(v_t)\rightarrow A$.

72,s,t,u,v. Multiply add. $s, t=0, 1, 2, 3, 6, 7$. $(A)+(E(u_s)\times E(v_t))\rightarrow A$.

73,s,t,u,v. Divide. $s, t=0, 1, 2, 3, 6, 7$. $(A)\div E(u_s)\rightarrow v_t$. Remainder is in A.

74,s,t,u,v. Scale factor. $s=0, 1, 2, 3, 6, 7$; $t=1, 2, 3$. $E(u_s)\rightarrow A$. Shift (A) left until $a_{34}\pm a_{35}$. Then transfer to v_t number of places necessary to shift (A) to restore word to original position.

75,s_0,t_0,n,v_0. Repeat. $s, t=0, 1, 2, 3, 4, 5, 6, 7$. Perform instruction obtained from next memory address n times. Each time order is performed, increase its u, v portions by s_0, t_0 resp. After instruction has been executed n times, jump to v_0.

References

1. Surface-Barrier Transistor Switching Circuits. **R. H. Beter, W. E. Bradley, R. B. Brown, and M. Rubinoff.** *Convention Record*, Institute of Radio Engineers, New York, N. Y., Mar 21, 1955, pp 139–45.

Discussion

R. E. Porter (Boeing Aircraft): Why was the Sperry-Rand model 1103A chosen as the program instruction model for the Transac?

Mr. Maddox: We desired one which embodied many of the ideas present in the 1103A. The two address instructions seemed reasonable, as did the parallel control, among others.

C. W. Rosenthal (Bell Telephone Laboratories): Can you describe your operating experience with Transac?

Mr. Maddox: I am afraid not, because Transac is not in operating condition, though it is more than 80 per cent finished. So far it has performed all the instructions that it is designed to do, except that we haven't tested the input-output equipment or checked the memory.

E. P. Dundatscheck, International Business Machine Corp. (IBM): What is the approximate packing factor obtained in the Transac, that is, how many cubic inches per transistor?

Mr. Maddox: In this model we had learned from past experience not to pack it too tightly. For example, one of the computers was packed by a mechanical engineer who was taken off hearing aids, and there were some comments about it. However, I would say that in the top level of the arithmetic section, we're getting about two transistors and two resistors per cubic inch.

Mr. Housman, (IBM): Why do you use a subtracter rather than an adder?

Mr. Maddox: I did not want to use both an adder and a subtracter, so it was a question of which we would use. The only difference I could see is that the ambiguous 0 is eliminated by using the subtracter.

Mr. Peck (IBM): What logical, nonarithmetic, operations are incorporated in the Transac?

Mr. Maddox: We have a logical multiply that performs by getting the zero's of one operand into a register containing the other operand. The latter register then contains *ones* only in those positions where *ones* were present in both operands. Also, there is an instruction that uses a logical substitute routine, that is, using two operands that are corresponding to similar operands in the Q register. There is also an instruction that does the logical multiply operation, which is nonarithmetic, and combines this operation with an addition operation to obtain a logical multiply-add operation.

Mr. Chang (Sylvania Electrical Products, Inc.): What is the switching speed of the transistors?

Mr. Maddox: We are using selected-surface barrier-transistor and our switching speed is about 0.06 microsecond.

Mr. Feigenbaum (Carnegie Institute of Technology): Transistor circuitry is not noted for its high reliability, yet nothing was mentioned about checking on this machine.

Mr. Maddox: There are special periods reserved on the machine for checking routines. We have the usual marginal test where the machine may be sequenced manually. Of course, there are standard procedures printed for this purpose. As far as reliability is concerned, we have never had a transistor fail to date, once it was installed in the computer.

Mr. Gariano (Burroughs): What transistor was used most extensively in Transac? What silicon transistor will replace this device?

Mr. Maddox: We used the surface barrier S-3101 transistor exclusively in Transac and, frankly, I do not know which silicon transistor is going to replace it. This is the next step.

C. H. Propster (Radio Corporation of America): What is the typical delay through each surface-barrier transistor-stage under minimum and maximum load conditions?

Mr. Maddox: I can only give you the average, the figure I gave a moment ago on the switching speed, 0.06 microsecond.

Univac-Larc, the Next Step in Computer Design

J. P. ECKERT

Univac®-Larc, the Livermore Atomic Research Computer, is being built for the University of California's Radiation Laboratories at Livermore, California. Larc (Fig. 1), is Remington Rand Univac's newest all solid-state large-scale computer, over 100 times faster than today's scientific computers and internally 1,000 times faster than today's business data-processing system. The design is based entirely on existing components. The customer can expect delivery in 1958. My paper is directed primarily at the systems aspect of the design.

The great speed and flexibility of Larc are achieved in part by the inclusion, for the first time in a single system, of parallel-decimal arithmetic (both fixed- and floating-point), complete checking, megacycle pulse rates, multiple arithmetic and index registers, and simultaneous

J. P. Eckert is with Remington Rand Univac, Division of Sperry Rand Corporation, Philadelphia, Pa.

® Registered trade-mark, Remington Rand Univac, Division of Sperry Rand Corp.

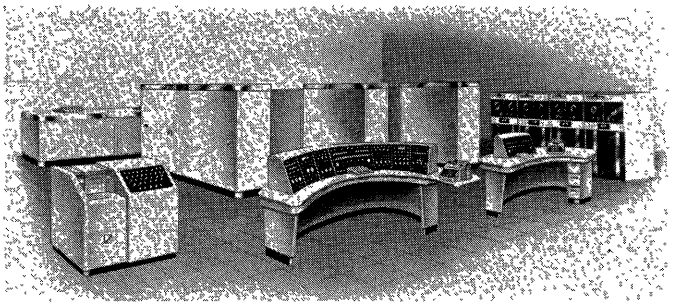


Fig. 1. Univac's newest all solid-state large-scale computer

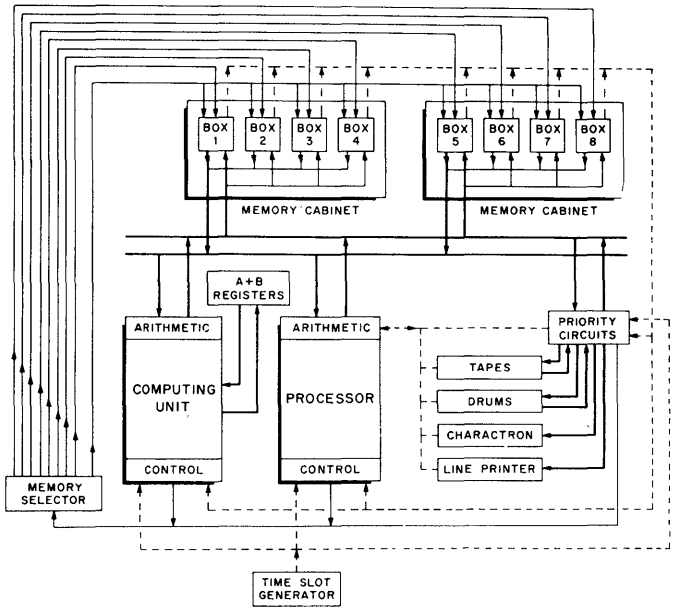


Fig. 2 (right). Operation of Larc system

operation of input-output equipment and computer circuits. While these items have been used in various business and scientific calculators in the past, this is the first time they have all been integrated into a single system.

Such a combination of the most desirable features of existing systems would in itself have constituted a more-than-usual step forward. In addition, however, Larc has three entirely new features, all new forms of parallel operation within a computer. First, there are two computing systems, one for arithmetic, and one to process and control the input-output data and prepare it for the computer. Second, each of these computers has overlap operation within its structure, allowing for simultaneous handling of the computer s instructions, the index registers, and the operands. Third, a second arithmetic computer can be connected to the system and fed from common input-output equipment. These three new forms of parallelism account for much of the advance in speed which Larc achieves. Even without them it would be much faster than existing computers.

Formerly, the term "parallel computer" implied a kind of ultimate in speed of operation. Actually, it was nothing of the sort. Although all of the digits of a word did in fact function in parallel, almost nothing else did, neither the control circuits, the input-output equipment, nor very much in the way of memory. Curiously, Univac I, although called a serial computer, because of the serial type of the memory and computing systems used, actually had considerable parallelism in it, in that checking and input-output functions went on in parallel with computing. Larc is the first computer in which the parallel principle is carried out consistently throughout the entire system to achieve a new concept in speed.

Influence of Programming on Design

Larc's increased speed is due in part to a complex and highly organized order code the use of which is made possible by modern automatic-programming techniques. These techniques, developed largely by Dr. Grace M. Hopper and Dr. John W. Mauchly, enable nearly optimum programs to be generated and assembled in detailed form from generalized-program instruction. Previously, the programmer was required to formulate the program step-by-step, and at the same time keep track of the many subroutines and their addresses. As a result of these programming limitations Univac I had considerably fewer order codes than Larc. In addition, the order codes in themselves were simpler. Since with automatic programming it is not necessary for the programmer to remember or directly use the order code, Larc uses a large order code containing many sometimes almost identical order codes required to minimize the number of steps in a problem.

With automatic programming compromises are no longer necessary in a design aimed primarily at achieving the greatest speed within a reasonable cost limitation. Considerations imposed by the programmer's limited memory, his slow speed, and his general scarcity no longer compromise the design. Consequently, Larc has been designed with 69 complex order codes and with accommodations for more. Not only does automatic programming enable the use of a greater number of order codes, but order codes of a greater complexity than was formerly practical may be included without hesitation. Actually, the complex orders are in themselves small subroutines.

Automatic programming has made practical the design of a system which combines for the first time all of the advanced features of earlier electronic computers plus three major new advances. Equally important to the practical realization of such a complex system have been the advances in reliable high speed, solid-state circuitry, and core-memory designs, as well as the development of a new high-capacity high-reliability drum-memory system.

As a result of the combined advances in system design and automatic programming, a new order of parallelism has been achieved, and has led to a system in which a large part of the equipment is kept functioning most of the time. By contrast, in present day large-scale scientific computers, many parts of the system are idle much of the time, since relatively few parts of the system are in simultaneous operation.

The system which has been evolved increases the speed of scientific calculations over 100 times, while the cost of the equipment over previous systems increases a little more than two times.

Description

A detailed description of Larc is beyond the scope of this paper. Briefly, the system operates as shown in Fig. 2. Input either from magnetic tape or punched cards is fed to the processor,

which contains an internally programmed computer, priority circuits, and from 5 to 8 synchronizers. The processor handles communications between the high-speed core memories, the large-capacity drum memories, and the input-output equipment. The processor also edits input and output data for the various tape units and printers.

Each high-capacity magnetic drum-memory unit is capable of storing 250,000 words of 11-decimal digits and a sign. Larc will contain 12 such drums, and the system can be expanded to accommodate 24. The magnetic drums have a high order of reliability achieved by the use of an air-floated head that does not wear the magnetic recording surface in any way.[1]

The high-speed magnetic-core memory is shared by the processor and the arithmetic computing unit. Each 2,500-word memory unit may be addressed independently of any other memory unit and may operate in parallel with it. The high-speed core memories are addressed on an essentially asynchronous basis. Larc has eight such units, 20,000 words, and the system may contain as many as 39 units, 97,500 words.

The arithmetic computer has both fixed- and floating-point arithmetic built in, since many scientific problems require floating-point arithmetic, and are speeded up by a factor of as much as 50 to 1 when the necessity for programming floating-point operation from fixed-point orders is eliminated. In addition, instructions are overlapped so that the time required for executing arithmetic instruction is devoted entirely to arithmetic operation, access-time having been overlapped with execution of the previous instruction. Typical cycles for execution of either floating- or fixed-decimal arithmetic operations are 4 microseconds for addition, 8 microseconds for floating rounded off multiplication. High speed is further achieved through the use of both A- and B-registers. The A-registers hold operands and immediate results. The B-registers are index registers. They permit shifting of operations to different parts of the high-speed memory system and avoid much loss of time which would otherwise result if addresses had to be modified by program steps, or if data had always to be moved to and processed in areas which were assigned on a fixed basis.

Four microseconds are required for the transfer of the contents of a memory location into any arithmetic register, the transfer of the contents of any arithmetic register to any other arithmetic register, or the transfer of the contents of any arithmetic register into any memory location. Comparison of the contents of two arithmetic registers to determine whether they are equal takes 4 microseconds. In the event that the comparison results in a conditional transfer of control, eight additional microseconds are required to make the transfer.

The input-output tape units have a data-handling rate of 20,000 alphanumeric characters per second. Available as optional output equipment are a directly connected high-speed print head, which can produce output copy at 1,200 lines a minute, and a Charactron cathode-ray tube printing and plotting unit. The Charactron is a special-purpose display tube which can be viewed directly or used to produce a permanent photographic record. The output rate of the Charactron display is 25,000 characters per second, or over 12,000 lines per minute.

This brief description of the system gives some idea of the degree of parallelism used in Larc. Should this parallelism result in a demand for information not available, the situation is automatically controlled by the resequencer, a unit of the system not previously referred to. Such a co-ordinated system could not have been balanced had not existing components with known performance characteristics been available at the beginning of the project.

Balance or proper proportion between the various units is perhaps the most important factor in the design of a complex system. Many present day computers have suffered greatly due to poor balance, poor budgeting if you will, of the available money between the various functions and units. Not only were some units made the wrong size or speed to match others, but useless features were frequently included to the exclusion of items of great necessity.

In Larc not only has extensive study of scientific problems resulted in balance, but sufficient flexibility, both in order code and in optional features, has been designed into the system to allow ready adaptation to the demands of a wide range of users. A good example of this flexibility in design is the memory system described in the following paragraphs.

Memory System

Larc's great speed depends on four levels of magnetic memory: first, the very fast 1-microsecond A- and B-registers, second, the 4-microsecond high-speed core memories, third, the large-capacity drum memories, and, fourth, the magnetic-tape system. This hierarchy of memories results from four requirements: that the memory system be very large, that it match the high speed of the arithmetic computing unit without restricting the nature of the problem which can be run at top computer speed, and that it be reasonable both from the point of view of reliability and of economy. Since speed and large capacity are economically antagonistic, the speed and large-storage requirements were met by four separate memories. The major burden falls on the 4-microsecond core memory and the multi-million-word drum memory. Such an arrangement would not have been efficient, of course, without the processor, which keeps the various memories co-ordinated in simultaneous operation without loss of time.

The idea of more levels in the memory system was considered and rejected for a number of reasons. The idea would be economically attractive only if the size of an added stage of high-speed memory were severely limited; but limited high-speed memory capacity, other than the A and B registers placed between the main core memory and the arithmetic circuits, can present awkward programming problems. Problems which are completely contained in the highest stage of the memory can be handled at exceedingly high speed, but, unfortunately many problems demand a sudden choice among more data than can be economically stored in this highest-speed stage. This information must then be obtained at lower speed in the main core memory. Moreover, the transfer of data to and from a very limited size high-speed memory can not always be anticipated in automatic programming, since it can depend on computations as they are actually going on in the problem. At best, the programmer must keep these restrictions in mind when he sets up the program. At worst, it is frequently impossible to fit some problems into such an elaborate hierarchy. The more stages there are the more difficult it becomes to automatically program a given problem. The idea of another level in the high-speed memory was rejected, therefore, as being undesirable, if avoidable; that is, if another way could be found to spend the cost of the extra memory to provide speed with greater flexibility.

Another type of high-speed memory that might have been used is the interlaced core-memory system. In this type of memory, two (or more) 6- to 8-microsecond memory units, which are less expensive than 4-microsecond units, might be interlaced to yield an access time of 4 microseconds or less. Problems in programming arise with this system, how-

ever, since an item of data may be called for from the first memory at one time and from the second memory at another. Since the data cannot always be located in the memory available at the next cycle, it may be necessary to wait to find it in the second memory, thus doubling access time on some operating cycles.

Considerable study led to the conclusion that to break a single-speed high-speed core memory into several groups that could be addressed almost simultaneously and at random offered the most for the money and placed the fewest restrictions on programming. In fact, it would still be necessary with either a multi-level or an interlaced system to have several groups at each level to handle the demands resulting from the arithmetic speed and the super-parallelism of the Larc system.

Design Approach

The design approach to Larc was conservative with respect to circuitry and to the choice of components, and radical with respect to logic. The system was balanced at a time when all of the components were in hand, so that design balance would not be upset by component changes during the design period.

The very great speed of Larc has been obtained primarily by logical sophistication both in the system design and the circuit design, rather than by trying to extend the pulse rate of the system beyond a safe rate for the present state of the art. Actually, the 2-megacycle pulse rate used is slightly less than that of Univac I, which was 2.25 megacycles, although a shift from tube to solid-state circuitry has occurred. Pulse rates were deliberately kept as low as possible, since the lower the pulse rate necessary to achieve an over-all operation in the required time, the smaller the percentage of the operating cycle consumed by sampling and retiming operations, which in themselves contribute little to the logical ability of the circuit. Even with the present 2-megacycle pulse rate, nearly one-third of the circuit operating time is consumed by these operations.

In order to allow this relatively slow pulse rate, very extensive networks of up to eight logical levels are activated between sample or pulse times. For example, in the adder, Fig. 3, the desired digits are computed, complemented if required, and checked in a single 0.5-microsecond pulse time. Carry over and unit adding for 11 decimal digits require another 0.5-microsecond pulse time.

To keep the number of wires and switching circuits which interconnect the many units of Larc down to a reasonable number, and at the same time allow for almost simultaneous communication between the various units (a necessity for the high degree of parallel operation achieved), a time-multiplex system of inter-unit communication is used. While this is an old technique in communications equipment, its use in the interconnection of the elements of a computer is quite new, and is one of the many new ideas which have given such a great increase in speed and flexibility without a corresponding increase in cost.

The result of this design approach is that today a very powerful new computer is under construction with assurance that it will be completed in 1958, since the logical structure of the equipment cannot be seriously compromised through the failure of the components to perform as expected. Test data accumulated over a period of years indicate that the over-all reliability and performance of Larc will exceed that of Univac I, in spite of the much greater complexity of the Larc.

Conclusions

To sum up, Larc's great computing speed is obtained in five ways: first, by combining for the first time in one machine checking, fixed- and floating-point decimal operation, multiple A- and B-registers and complete input-output buffering of the system; second, by the addition of a data processor and over-lapped operation of the arithmetic computer; third, by use of a main-core memory which is not only inherently faster than any existing core memory, but is divided into groups that may be used simultaneously; fourth, by the use of circuitry two or three times faster than that used in present parallel computers: or, alternately, circuits which in a pulse cycle can carry out logic several times as complex as that which existing serial computers can carry out in a pulse cycle of about the same duration; fifth, by providing for connection of a second arithmetic computer into the system. On certain types of problem, the addition of this computer can mean an increase in speed of almost 100% while the cost of the system will be increased by less than 50%.

Since Larc is a highly optimized computer from the logical point of view, future increases in speed will have to come in great part from the component direction until Larc has paved the way for system sophistication beyond our present problem-planning and automatic-programming ability. Higher-speed circuits and memory units are under development, and will increase the speed even more as time goes on. Work on a new form of high-speed memory is well along.[2]

Univac-Larc is our latest, fully planned step forward in a long-range plan for super computers. We feel that Larc will achieve more speed than most customers will be able to absorb in the next few years. In addition, there will be problems in adapting to such a new speed range, and problems in trying to get the most out of a flexible new system.

References

1. Proceedings of the Eastern Joint Computer Conference. *AIEE Special Publication T-92.* "A Large-Capacity Drum-File Memory System," **H. F. Welsh, V. J. Porter.** May 1957, pp. 136–38.

2. *Ibid.* "A Compact Coincident-Current Memory," **A. V. Pohm, S. M. Rubens.** May 1957, pp. 120–23.

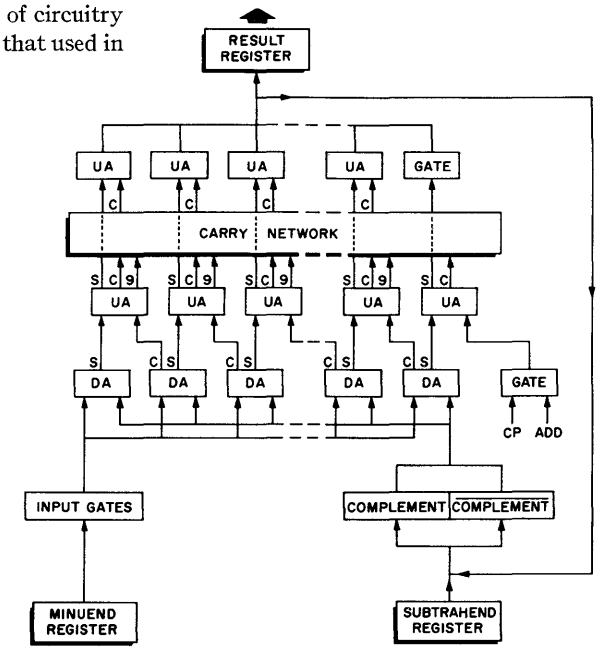


Fig. 3. System's adder

Discussion

Mr. Morison (Douglas Aircraft Missile Engineering): How do you overcome the limitations of human programmers when you program the "automatic programming" compilers?

Mr. Eckert: I don't quite understand what is meant by "the limitations." The purpose of automatic programming is to overcome some of these limitations, and it takes a lot of work, and a lot of manpower, to design the compilers and to do the automatic programming itself; we do not know the way to get around that. However, we have arrived at a point where our automatic programming is good enough to use automatic-programming techniques which have already been developed in producing the compilers for Larc.

A. Abrams (International Business Machine Corp.): What type of marginal checking, if any, is applied to the transistors in Larc?

Mr. Eckert: In most of the Larc circuits there is a load resistor on the transistors which provides a minimum load. By varying the potential applied to this load resistor a load greater than normal can be put on the circuit. In this way, we can cause the circuit to fail, and have a quantitative measure of how much additional load the system can stand.

Mr. Schorr-Kon (Massachusetts Institute of Technology, Lincoln Laboratory): Does "automatic programming" refer to the fact that your orders are complex, or do you actually have a machine language with higher orders of abstraction?

Mr. Eckert: Remington Rand has developed several automatic-programming techniques already. The particular programming technique we are using in this machine is called "general programming." In this type of automatic programming the programs are put together in such a way that one can interpret them moderately well later, and make changes without going back and doing the entire automatic programming process all over again. The process starts with a pseudo-code or a code which is not in the machine language. It works into machine language in several stages.

A. L. Tritter (Massachusetts Institute of Technology, Lincoln Laboratory): What "parallelism" is contemplated between the two machines to be linked to a single input-output system?

Mr. Eckert: Actually, the two computers and the processor can all be synchronized on one problem by a fairly simple expedient. Ordinarily, in fact, the processor and the calculator are coordinated by the same simple expedient. First, they both use a common memory. They both are then able to read the conditional transfer orders placed in the memory by the other machine. Either machine can place an order or modify an order that lay in the path of the other machine, and in this way they can exert any desired influence on each other, depending largely on how far one goes in programming.

They cannot take a problem and perform parallel operations in a very microscopic sense. The problems cannot be of the type where you tear the problem apart and then give the first multiplication problem to one computer and the second one to another; but they are problems in which short subroutines or short sections can be given over to one computer or the other. A kind of macroscopic parallelism rather than microscopic.

Mr. M. Glatt (General Electric Co.): Does Remington Rand believe computers will continue to become even larger, and is your company going to do anything about the vacuum developing between the desk calculator and your large computers?

Mr. Eckert: Yes, we are. Actually, within the past year we have published some papers on a small machine called the Univac Magnetic Computer. This magnetic computer is a one-of-a-kind machine, built for the Air Force. A somewhat more comprehensive magnetic of the same type machine, which has a variety of input-output equipment options, will be placed on the market in the future.

Design Objectives for the IBM Stretch Computer

S. W. DUNWELL

IT IS APPARENT to every user of an electronic computer that there are areas in which major improvements are desired. Present computer speeds, remarkable as they are, still fall short of the requirements of many of today's business and technical applications. The labor of programming often delays or prevents the application of new problems to the machines. Maintenance continues to consume a significant fraction of the working day, and requires highly skilled engineers to locate and repair machine faults.

The experience gained by the builders and users of computers, together with the advent of new solid-state components, now makes possible computers which are significantly better in all of these respects. Project Stretch has the goal of producing such a system for both technical and business use. As the name implies, we are endeavoring to employ the most advanced techniques and components possible with today's technology Many of these techniques are still in the research phase of their development.

International Business Machine Corporation recently contracted to deliver the first Stretch system to the Los Alamos Scientific Laboratory of the Atomic Energy Commission. A joint mathematical planning group has been set up to examine the advanced problems which future machines will be required to solve, and to assist in developing the Stretch system along these lines.

Since the project is still in the research phase, a number of important design decisions are still to be made. While confident that continued research will provide a satisfactory solution in each case, it is recognized that these decisions may have some influence on the ultimate speed of the computer system.

It is estimated that the operating speed of the system on typical technical applications will be at least 100 times that of the fastest general purpose computer now in use. This will be obtained through a combination of higher speeds for arithmetic and logical operations, multiplexing to allow several parts of the system to operate concurrently, and new instructions designed to reduce the number of steps required for common operations.

It is evident that a computer system operating 100 times faster than today's fastest machines and consuming in the process a million or more instructions a second, cannot be programmed effectively by any process which demands that a human write each instruction to be executed. The program will have to be assembled largely by the computer itself from a much simpler statement in mathematical and logical notation. A system of computer-assisted programming, or "automatic programming" as we call it, will be developed concurrently with the development of the instruction system for the Stretch computer, so that the least

S. W. DUNWELL is with the International Business Machines Corporation, Poughkeepsie, N. Y.

possible human effort be required for programming.

Experience with solid-state components indicates that their use alone will greatly increase the reliability of the Stretch system over that of vacuum tube machines. This, combined with a greater ease of locating and correcting those falts which do occur, will have an important bearing both on the amount of useful work which the system can accomplish and on the size of the engineering staff required to maintain it. It is planned that the computer include a thorough system of automatic checking, together with means for indicating within narrow limits, the location of any part of the mechanism which is creating errors. Since automatic checking cannot insure the accuracy of the input data or the program, it cannot insure the accuracy of the computed results. Instead, its presence will be primarily to facilitate the repair of the machine. Automatic error correction also will be provided in several areas. It will, for example, be used in association with the magnetic tapes to insure a level of accuracy which cannot be obtained in any other way.

The system will consist of three major computer sections, all of which communicate with one multi-section memory. The operations required of the computer system will be divided so that each section performs a portion of the over-all task. The three sections of the computer are an input-output section to maintain communication with the individual input-output units, a serial computer section for editing the flow of input-output data, and a high-speed parallel arithmetic section to operate upon the organized data of the problem. The division of the computer into separable major sections is sufficiently unconventional to deserve explanation here. From the standpoint of engineering design, it allows the choice of the most appropriate mechanism in each part of the system. This is evidenced by the choice of a serial arithmetic mechanism for the complex editing of data, and of a parallel arithmetic system for high-speed operation upon previously organized data. Furthermore, separation of the computer into sections enables us to schedule efficiently the design and manufacture of each section.

The section which provides communication between the various input-output units and the computer memory is known as the "exchange" because of its functional resemblance to a telephone exchange. The mechanism is capable of communicating simultaneously with many input-output units. These will include the various kinds of computer input-output devices which we know today, such as magnetic tapes, paper tapes, printers, manual keyboards and typewriters, card readers and card punches. New input-output devices being designed for the Stretch system include a magnetic disk memory capable of holding one million words of data, and of communicating with the computer at the rate of one word each 4 microseconds. These disk memories will be available in multiples to supplement the high-speed ferrite memory. Also, magnetic tape units capable of operating at nearly the same speed are planned for availability by the time the first system is delivered.

Particular attention is being given to making the input-output system as general as possible, so that it can readily accept the input-output devices of the future. It is anticipated that these will include electronic printers and plotters, units for direct visual display of data, and devices for the direct reading of typed input data. The interpretation of speech and handwritten data are recognized as being less immediately achievable, but it is assumed that they will become possible within the life span of the Stretch system. The system will be capable of operating on-line with analog and digital devices of many kinds, and of being fitted into business systems requiring direct over-wire interrogation of large memory reservoirs from remote locations. As an example, an interrogation typewriter might communicate with the computer over long distance telephone lines to obtain company-wide availability data on any desired product.

The serial computer section will operate in both decimal and binary arithmetic modes. It will include the full complement of instructions necessary for fixed- and floating-point operation, and for handling data with fields and records of variable length. Its use to edit the flow of data into and out of the high-speed arithmetic section will be facilitated by instructions designed specifically for converting between binary and decimal radices, and for converting between the codes used by the individual input-output units and a preferred code within the computer. It will also include means for accepting instructions and data words in the original format in which they were transcribed by humans, and of condensing them into the more efficient format used within the computer. In a similar manner, results will be expanded into the format necessary for printing and ready for human comprehension.

Because the arithmetic unit of the serial computer section will operate on data words of varying lengths, the speed of arithmetic operations can be expressed best as ranges. Addition will require 2–3 microseconds, and multiplication 5–15 microseconds. Logical operations will be more comprehensive than the transfer of control operations of present computers, and will often perform the equivalent of several present logical operations in 2 microseconds.

The complex nature of typical editing processes requires that the serial section provide all of the classes of operations of which the system as a whole is capable and perform them at considerable speed. It is, in fact, a very versatile computer within a computer. The serial computer alone has an operating speed at least 10 times that of present day vacuum tube machines, such as the International Business Machine types 704 and 705.

The high-speed arithmetic mechanism has the function of rapidly executing the operations called for by the mathematician in his description of the problem. Since the other sections of the system relieve it of all secondary responsibilities, the high-speed computer section will be able to perform useful work on the arithmetic portion of the problem at between 75 per cent and 90 per cent of its theoretical maximum rate. This compares very favorably with present computers, which spend a large part of their time on secondary operations. Addition and subtraction in floating point notation will require 0.6 microsecond. Multiplication will require 1.2 microsecond. Approximately 0.2 microsecond must be added to these times for each data word transferred over the bus system between the arithmetic unit and the memory. Specific times cannot be given for logical and housekeeping operations, since they will, to a large extent, be executed simultaneously with the arithmetic of the problem.

In order to achieve the level of performance which has been described, it is necessary that all of the active components in the system be new and of types not now in use. The transistors will be what we know as the 10-megapulse class, by which is meant that they can be used with a 10-megacycle repetition rate in common devices such as adders. These transistors in both the p-n-p and n-p-n types are available in limited quantities for circuit design, where they are exhibiting, under test, rise and fall times short enough to permit their use by Stretch. The transistor circuits to be used are discussed in a paper by Mr. R. A. Henle.[1]

Two classes of ferrite memory will be used. Both of these memories are discussed in a paper by Mr. W. W. Lawrence.[2] One class of memory will be provided in units of 8,192 words and will have a full cycle time of 2 microseconds. When reading, a data word will be available for use at the end of 0.8 microsecond. The second class of memory will be provided in units of 512 words and will have a full cycle time of 0.5 microsecond. When reading from this memory, a data word will be available for use at the end of 0.2 microsecond of its cycle. To further increase the speed of operation of the memory, multiple sections in each class will be provided, with each section capable of operating concurrently with the others. It is recognized that a large memory is one of the most important needs of the computer of the future. For this reason, the addressing system of the Stretch computer will be designed for the ultimate use of randomly addressable memories of up to a million words capacity. In addition, the external memories in the form of magnetic disks and of magnetic tape devices may ultimately provide data in blocks up to a total capacity of possibly 100 million words.

The many investigations necessary to carry the project through its present research phase are proceeding in close conformity to the original schedule, and we look forward with considerable confidence to being able to put the Stretch computer into production in the near future.

References

1. Proceedings of the Eastern Joint Computer Conference. AIEE Special Publication T-92. "High-Speed Transistor Computer Circuit Design," R. A. Henle. May 1957, pp. 64–66.

2. *Ibid.* "Recent Developments in Very-High-Speed Magnetic Storage Techniques," W. W. Lawrence, Jr. May 1957, pp 101–03

A New Large-Scale Data-Handling System, DATAmatic 1000

J. ERNEST SMITH

THE DATAmatic 1000 (D-1000) is a high-capacity electronic data-processing system designed specifically for application to the increasingly complex problems and procedures of present-day business. The system incorporates significant new systems techniques, as well as several basically new component developments. One of the outstanding features of the D-1000 is its ability to feed information from magnetic tape into the central processor at a sustained rate of 60,000 decimal-digits per second, and to deliver data after processing back to magnetic tape at this same rate. The operational speed of the central processor maintains full compatibility with the high speed of information transfer. Consequently, the difficulties caused by programs which are either tape limited or processing-time limited do not arise in the majority of commercial applications of this system.

The basic unit of information in the D-1000 is the word, which contains 52 bit positions. One word will store a complete instruction or, alternatively, an amount of information ranging from 8 alphanumeric characters to 12 decimal digits. The system admits two distinct types of character representation; an alphanumeric character is represented by 6 bits, whereas a numeric digit may be represented by just 4 bits. This duality of information coding leads to substantial economy in the storage and manipulation of business data. Whenever, as is often the case, great masses of information are in numeric form, the 4-bit representation is used. When, however, data words comprising alphabetic information are involved, the 6-bit character coding is used. The 6-bit code covers all 56 symbols of the D-1000 system, including the 26 letters of the alphabet, the 10 digits, and the 20 special symbols. The 4-bit mode is intended to cover primarily the 10 decimal digits.

Two typical D-1000 words are shown by Fig. 1. The upper section illustrates an 8-character alphanumeric word; the lower section shows an 11-decimal-digit numeric word with the appended sign. Note that it is possible to mix alphanumeric information not only within a given record, but even within a particular word of that record.

The basic instruction of the system is of the 3-address class. Two of the addresses generally serve to locate the memory position of the operands of the order, and the third position generally identifies the location to which the result of the order is to be transmitted. The order word also identifies the operation to be performed by its code, and contains, as does every word in the system, four positions of checking information. Fig. 2 shows a typical addition order as it is stored within the space of one word.

The central processor embodies the arithmetic and control sections of the equipment, as well as the main high-speed memory and the auxiliary or buffer memory. The main memory consists of a ferrite-core array of 2,000 words, each having 52 binary positions; see Fig. 3. The complete cycle time for this memory is approximately 14 microseconds, which is indicative of the rate at which repeated access to the memory may be accomplished. The arithmetic unit is serial in structure, operating at a pulse repetition rate of 2.2 megacycles per second. Typical operation times for this unit are: 4,300 addition or subtraction operations per second; 5,500 comparison operations per second. These times apply to complete operations; for example, the addition operation as here defined includes the extraction of both the addend and the augend from memory, the addition of these quantities, the transmission of their sum back to memory, the complete verification of the transmission of the operands and the result, the automatic checking of the addition process itself, and finally the transmission to the control unit of the next succeeding order to be processed. The control section is responsible for the orderly performance of all operations within the processor, including the interpretation of the orders, and verification that the proper sequence of controls has been called into action in accordance with the requirements of each instruction being executed.

The buffer, or auxiliary memory of the D-1000 is of primary importance in that this unit sustains the high rate of information transfer to and from the

J. Ernest Smith is with the DATAmatic Corporation, Newton Highlands, Mass.

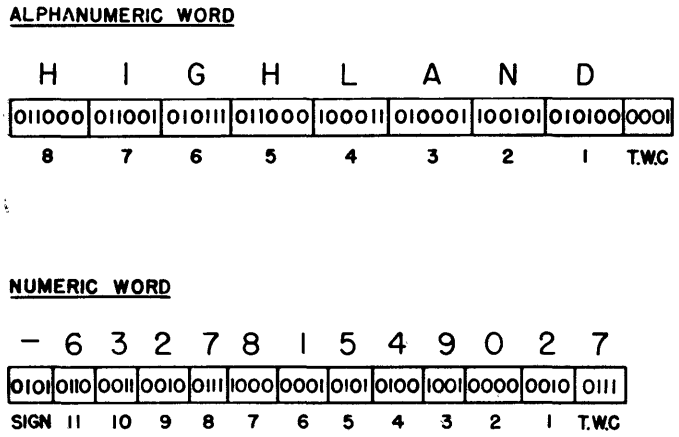


Fig. 1. Typical D-1000 words

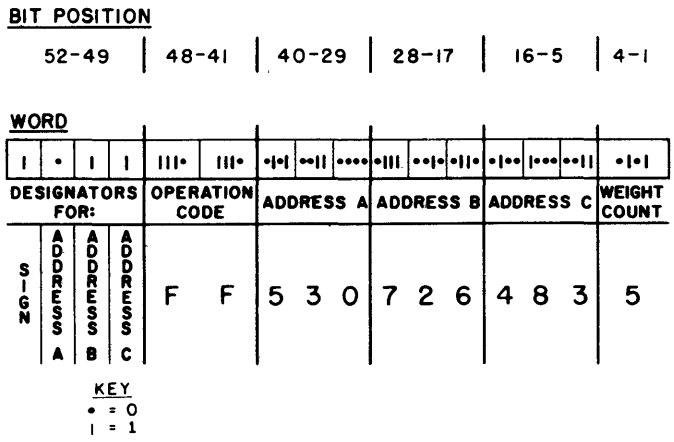


Fig. 2. D-1000 addition order

magnetic tapes of the system. The input buffer which receives information from the tapes is divided into two sections, each having a capacity of 62 words. The design of this input section is such that the central machine may be in operation while information is being read from the tapes. Furthermore, it is possible for several tapes to be feeding this buffer section sequentially with no resultant loss in the input information rate of 60,000 digits per second. The output section of the buffer likewise contains two sections, each of 62 words, and permits operations to proceed within the main processor while information is being recorded in a continual stream upon one or more tapes of the system.

The magnetic tape system of the D-1000 embodies many new features which have great significance in the overall performance of the system. The tape itself is 3 inches wide and it embodies a new technique of tape construction. Unlike conventional plastic tapes, the actual recording surface is sealed within a protective sheath of mylar. Fig. 4 shows an enlarged cross-sectional view of the tape. Because of this construction no frictional contact between the recording surface and the read-record head is possible; furthermore, the mylar prevents the recording surface from being damaged by handling. The resulting wear upon either the tape or the recording head after millions of passes of the tape is negligible, as life tests in our laboratories have shown; in fact, no perceptible loss of the recorded signal has been noted after the same segment of tape has passed the reading head several million times.

A new time-modulation technique of recording has been employed in the D-1000 system to reduce the adverse effects of signal variability and noise. In many ways it bears the same relationship to conventional recording techniques that frequency-modulation transmission bears to amplitude-modulation transmission in the field of radio. Essentially, a "one" is distinguished from a zero by means of a time differentiation scheme. The "one" occupies approximately twice the time interval of a zero in both reading and recording. The polarity of the pulse upon the tape is of no significance in the determination of the information, nor is the sensing of the information directly a function of the amplitude or the strength of the signal. Fig. 5 shows a pulse train of information as it appears in the D-1000 recording system. A total of 31 information channels are recorded on the broad tape. The successive bits of each character are recorded longitudinally along each channel of the tape, and successive characters follow one another within the channel. This is in direct contrast to conventional information patterns on tape wherein the successive bits of each character occupy corresponding positions in six or seven distinct tape channels; see Fig. 6. It should be noted that in the D-1000 information array there exists no particular time relationship between the data in one channel and the data in any other channel; each channel is treated individually, thereby making unnecessary any requirements for synchronization of pulses across the tape. This arrangement of information has a further advantage in that it enables searching to proceed upon several tape mechanisms simultaneously without a multiplicity of reading equipment, the cost of which would be prohibitive. The searching process is made possible by the fact that the key word or argument which is being sought always resides wholly within one channel; thus, by appropriate switching means, as many as ten tape mechanisms may be searching for information simultaneously, using only the standard complement of reading and amplification equipment.

Table I. Sorting on Six D-1000 Tapes

Number of Records	Length of Record, Decimal Digits	Type of Sorting	Time, Minutes
390,000	48	merge	82
110,000	120	merge	29
21,000	72	merge	4
10,000	36	digital	1

Sixty-two Datamatic words are recorded in a unit block upon magnetic tape. They are arrayed, as shown in Fig. 7 with two words occupying each channel within a block. The block is read as a complete unit into the input-buffer memory system. A tape length of approximately 2,700 feet leads to a total capacity of 50,000 blocks, or 3,100,000 words per reel of tape. This capacity is the equivalent of 37 million decimal-digits of information on a single-tape reel. The information storage on tape has been increased substantially through the use of an interlacing scheme of block positions on the tape, as shown in Fig. 8. Successive blocks of data are recorded in alternate block positions on the tape. Beginning at the physical end of the tape, the "omitted" tape blocks are then utilized for the second half of the recorded data. Consequently, no "dead spaces" are required for acceleration and deacceleration of the tape mechanism. The alternate block construction provides a full block length for acceleration and deacceleration purposes whenever a tape stop is required in a given direction. On the reverse scan of the tape, the role of the blocks is

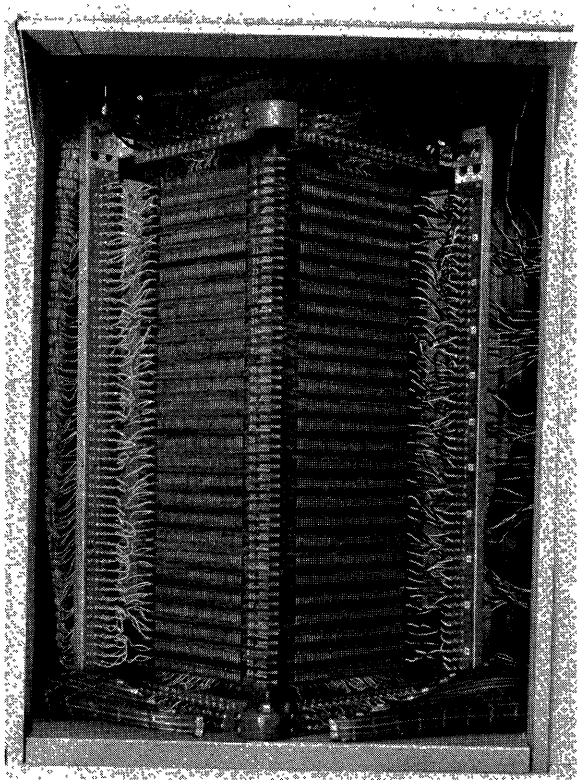


Fig. 3. Main memory

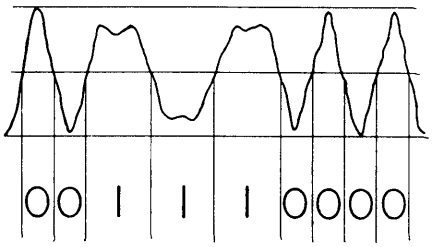


Fig. 5. Typical pulse train of D-1000 information

interchanged and the former recording space is now used for interblock stops and starts; the information presently of interest resides in what formerly had been the acceleration space. The magnetic-tape transport operates when reading and recording with a tape speed of 100 inches per second, which yields an input rate from a single tape device of 60,000-decimal-digits per second. This rate is not the instantaneous rate of reading or recording; rather it is the mean effective rate at which information is continuously made available to the central machine from a single tape device. The over-all design of the D-1000 system is such that the central processor can normally accept the information at this rate, thus enabling this high-input rate to be maintained for substantial periods. A reading from one tape may be in process simultaneously with writing upon another tape, and both may be in process while the central processor is manipulating or calculating data.

In the D-1000 system there are a total of 33 fundamental instructions which span across several categories of orders; these orders include the standard calculating orders as well as orders used to perform memory and buffer transfers, word shifting, comparison, printing, and many other functions. The scope of this paper does not permit of any detailed consideration of the array of orders of this machine. However, it is important to note that the instructions which govern the D-1000 system have been specially devised to simplify the complicated programming requirements in many business applications. Specifically, the order structure is devised to minimize the number of program steps to accomplish such common requirements in business-data processing as sorting, merging, searching, infiling, and extraction of record information. Furthermore, through the incorporation of many special control features in the design of the equipment, the need for what are commonly called "housekeeping" orders and routines has been greatly reduced. The calling forth of successive orders from the memory normally proceeds sequentially under control of a sequence register. However, several orders are of a class whereby the third address may designate an arbitrary memory position for the location of the next order. This type of instruction call is termed the "subsequence mode" of operation. It conveniently enables subroutines to be called into execution at the conclusion of which the normal sequence of instructions may be resumed. The need for the usual subroutine entrance and exit orders is eliminated. The order structure is conjunction with the high input-output speeds of the D-1000 enables such operations as sorting and merging to be accomplished with great rapidity. Table I gives certain

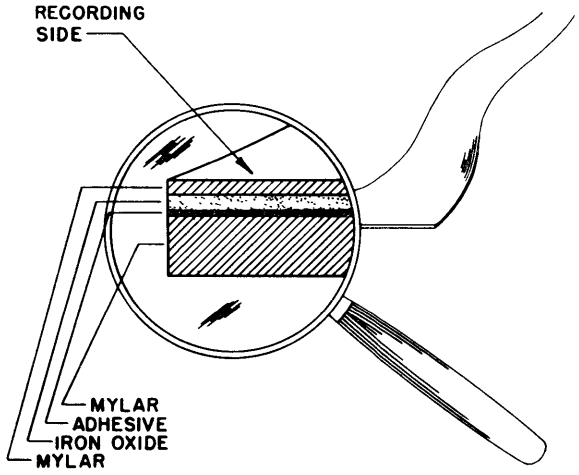


Fig. 4 (left). Enlarged section of D-1000 magnetic tape

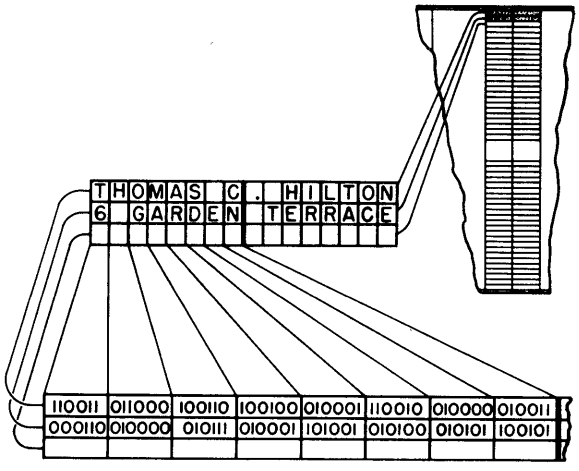


Fig. 6 (right). Information arrangement within D-1000 words

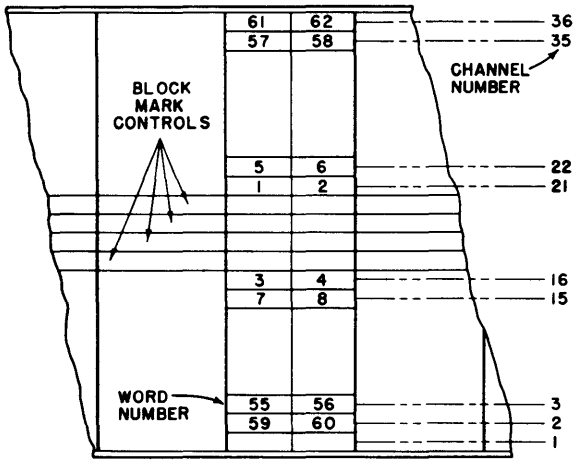
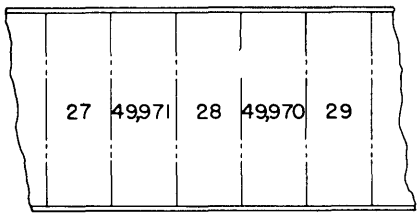


Fig. 7 (left). D-1000 arrangement of words on magnetic tape



"FORWARD"- INFORMATION IS READ 27; 28;29
"REVERSE"- INFORMATION IS READ 49,970; 49,971

Fig. 8 (right). Interlace of D-1000 blocks on magnetic tape

typical sorting speeds where six tape mechanisms are being used in the operation. As an example of the file-updating process, consider a main file containing 500,000 items, each item of which contains 320 alphabetic characters and 240 decimal digits. Assuming that certain simple changes are made to 5,000 items of this file, the total file of 500,000 items will have been updated in less than 20 minutes.

Complete self-checking has been incorporated into the design of the D-1000 system. Every word of information as well as every instruction word possesses a weight-count decimal digit which remains with the information through the course of all information transfer and manipulation. Generally, whenever a word is transmitted from one unit to another, a weighted counting process is inaugurated upon the digits or characters of the word to verify that no information has been gained or lost in the transmission. The checking system detects all single bit errors, and is instrumental in detecting double and multiple bit acquisitions or deletions. This same weight-count digit is used in the case of numeric information to verify that arithmetic operations such as addition, multiplication, shifting, etc., are correctly performed. The weight-count technique of information monitoring is further employed in the reading of information from all magnetic tapes; in this case when a weight-count error is sensed by the equipment, the program is usually arranged to cause the D-1000 to reread the information from tape automatically. The equipment may be programmed to stop after an arbitrary succession of misreadings of this information. Several situations which normally confront the programmer are automatically sensed by the equipment, enabling special subroutines to be called into play without stoppage of the machine. Included in this category are such features as overflow control in the addition and subtraction processes, improper relative magnitudes of the divisor and the dividend in division, physical end or beginning of magnetic tape, and the automatic rerun features in the case of weight-count error detection as already mentioned.

The central console of the D-1000 has provision for entering on, or reading from, any memory position of the machine as well as certain selected special registers of the central processor. It is also equipped with an array of diagnostic indicators which will enable an informed operator to determine not only the type of error which has occurred, but frequently the precise location of such equipment difficulties. Provisions are also made for reducing the amount of time lost in preparing for reruns. This is accomplished through the use of automatic rerun controls at the console. When the problem has been properly programmed, it is possible through the use of this console feature for the operator merely to press an appropriate button, causing the program to revert automatically to the proper point in the program for purposes of the rerun. In this case, the operator may not be aware of the specific point in the maze of programming at which the machine has come to a stop; yet, within a matter of one or two seconds, the machine will have resumed operation at the proper rerun point.

An extensive system of marginal checking is employed in the D-1000, utilizing controlled variation of certain voltage levels in the equipment. By means of a built-in switching system it is possible to subject entire racks of equipment to marginal check or, when localization is desired, the voltage variation may be applied to but a few packages of a single chassis.

The magnetic file units of the system are used for directly connected input and output to the central machine. They are also employed in conjunction with the input and output converter sections of the system. The deployment of

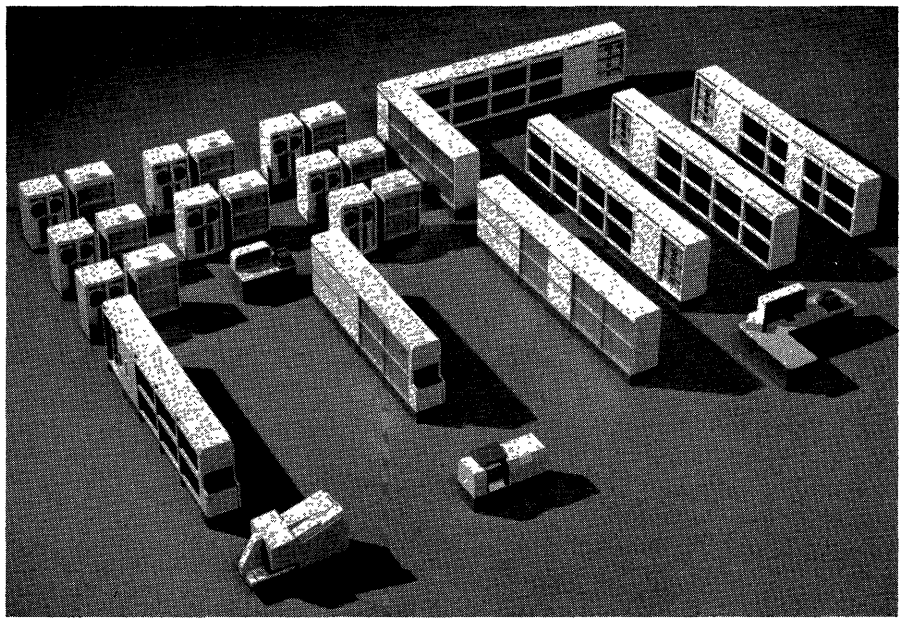


Fig. 9. Typical D-1000 installation

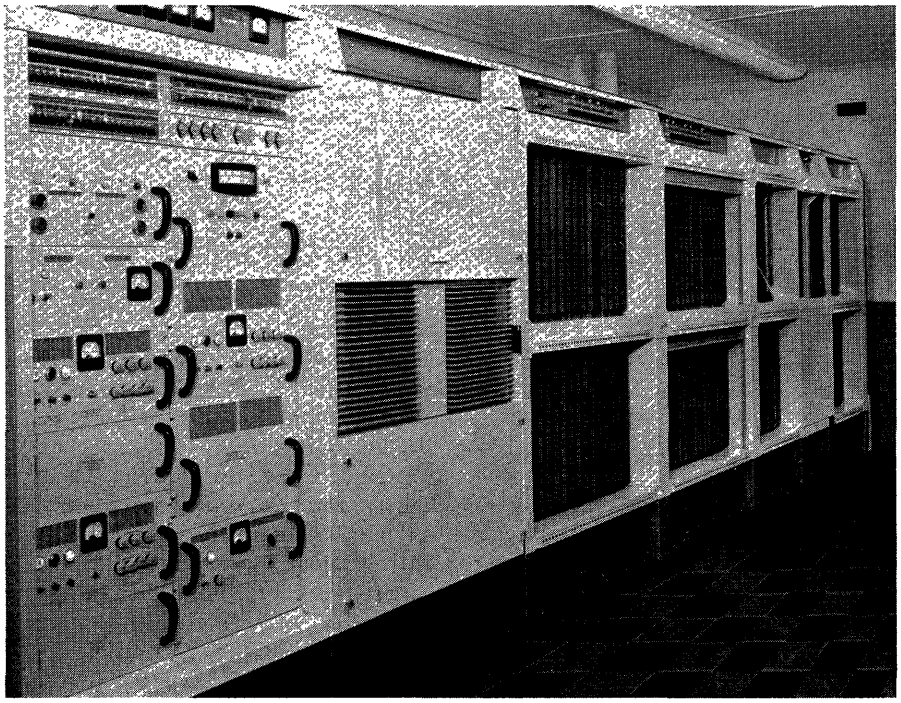


Fig. 10. Arithmetic section, D-1000, open-wire side

tape mechanisms for various applications in a given installation may vary greatly. In standard minimal installations the number of mechanisms which may be feeding and receiving information from the central processor might well vary from three or four to eight mechanisms. Correspondingly, the number of mechanisms which may be in use by the conversion equipment may also vary from period to period within a normal working day. An elaborate switching network is incorporated in the D-1000 system in order that time lost in switching tape mechanisms from one usage to another, or in changing reels of tape from one mechanism to another, may be kept to a minimum. This switching network may be used, in the event of an emergency, to tie into the system a spare tape device for any usage whatever in a matter of seconds. The installation may then proceed with its normal running of the day's transactions, while investigation and maintenance, if necessary, of the mechanism in question proceeds without interference. The goal then, in this entire magnetic-tape system, has been to minimize the amount of machine-time losses due to human interference and, correspondingly, to increase the percentage of useful running time of the equipment during an 8-hour day's operation.

Prime input to the D-1000 is frequently in punch card form. The card-to-tape converter operates completely independently of the central processor and thus may be in operation simultaneously with the central machine. Cards are fed at the rate of 900 cards per minute, and the punched information is recorded on the standard broad tape after the conversion process for each card has been completed. The tape, in its original tape transport, is now ready for direct input to the D-1000 system. The cards are read at two reading stations, each having 80 brushes; the cards are then sent either to the normal output hopper or to a reject hopper, depending upon certain conditions which will be described shortly. The two reading stations act to check, one upon the other, and the converter unit ascertains that there is no discrepancy between the two readings before proceeding with the conversion. A substantial amount of editing of the card information is accomplished within the converter itself. A particular card column may be converted into 6-bit alphanumeric code, or into 4-bit numeric or hexadecimal code. Several other code configurations, based upon various common practices in the punching of cards, are translated in special ways. For example,

Fig. 11. Arithmetic section, D-1000, tube side

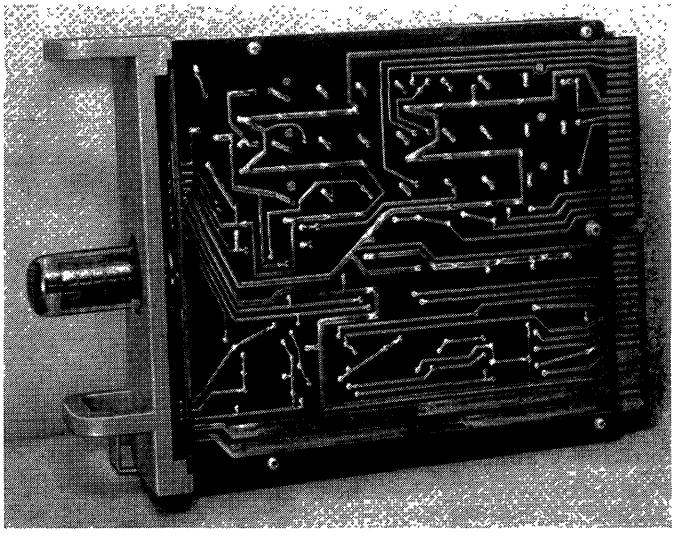


Fig. 12. Standard package, D-1000, side view

overpunching of particular columns to indicate sign information is readily handled by the converter, as well as dual information-punching in any given column. The converter is equipped to detect erroneous blank columns as well as illegal or impossible punch configurations. Whenever an illegal punch is sensed, the machine may be arranged either to stop or to proceed with the conversion, automatically recording upon the tape a code indicating the illegality of the punch. This recording is later automatically sensed by the central processor and appropriate subroutines are called into action. Rejected cards are transmitted to an appropriate reject hopper. Extensive built-in checking provisions are incorporated in this converter to minimize the danger of undetected errors.

The output converter consists of the equipment which converts into final printed form data recorded on magnetic tape. The printing is accomplished by a 120-column line printer at a speed of 900 lines per minute. Extensive editing of the information recorded on the tape is performed by the converter; the most complicated printed formats are obtainable with a minimal amount of preediting required in the central processor. In fact, in many instances it is possible to print final copy intended for customer distribution from a main-file tape of the system which had not been specially edited for use on the output converter. Not only is the emission of special symbols and legend material possible, but also the printing of certain parts of the form may be suppressed, depending upon the content of other data within the particular record. Furthermore, the same output tape may be used for several different types of printing runs by simply inserting appropriate prewired plugboards into the equipment. The sequence of information within the record on magnetic tape need not have any relation to the sequence of printing of information within a given line. It is, moreover, possible to scan a record on the tape several times, on each occasion deriving different combinations of data to be printed on a given form; data from the tape may be rejected or printed several times at will. From the moment that information is read from the magnetic tape to the actual printing process itself, a complete train of information monitoring exists to preclude the possibility of erroneous information being printed. This system includes a readback signal from the actual printing hammer to the original information stored to verify the correctness of the character being printed in every column of the form. This same output converter system may be directly connected to standard high-speed card punching equipment; in this configuration, the dual-purpose converter becomes a magnetic-tape-to-punch-card converter. When the equipment is employed in this way, all of the previously described editing and checking features of the converter are maintained.

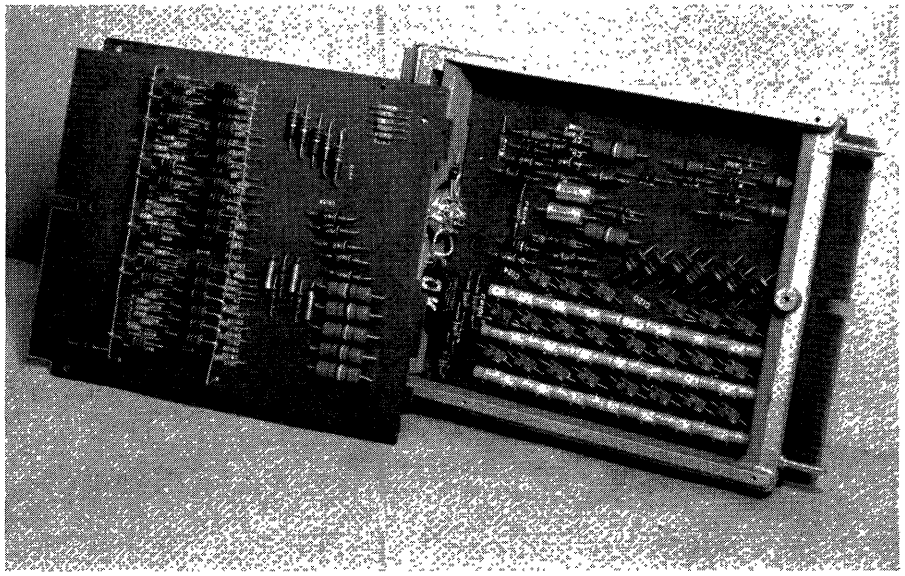


Fig. 13. Standard package, D-1000, open view

In many instances it is desirable to query the main tape files of the system to ascertain the contents of a particular account or record. The file reference unit, a standard unit of the D-1000, is used for purposes of such interrogation. This unit may have access to any of several tape mechanisms of the installation at any time, provided only that such mechanisms are not being called upon at that instant by the central machine or other auxiliary conversion equipment. Provisions of the file reference system are such that it is possible to obtain a random record from the file in a relatively short period. For example, assume a complete file of 200,000 records to be distributed across four tape mechanisms; each record say, is 30 words or approximately 300 characters in length. A random record in this file can be located and printed out by the file reference unit with an average access time of approximately 40 seconds, a figure which is made possible by the serio-parallel nature of the magnetic-tape storage.

An over-all view of a typical D-1000 installation is shown in Fig. 9. The central processor consists of six major equipment sections. Two sections of the central processor house the main arithmetic and the central control units of the system. The main memory and its associated driving and control circuitry occupies a third section. The L-shaped section contains the auxiliary or buffer memory, comprising 124 words of magnetic-core input storage, as well as 124 words of core output storage. Reading and writing central amplifiers as well as the switching networks for the magnetic-file units are located in the fifth bay of equipment. Completing the complement of equipment of the processor is the central console of the system. The entire central processor is contained within a single enclosed area of the installation.

A second area is devoted to the array of magnetic file units; each unit comprises a tape-transport device and an associated rack containing the tape control and preamplifier circuitry. A separate air-conditioning system is used in the magnetic file room to minimize the effect of any possible adverse environmental factors upon the reading and recording operations.

Finally, the input and output converters are located in a third compartment in the installation. Included in this area are the high-speed printers, the card-feeding equipment, and the card-punching equipment which are directly connected to the input and output conversion systems.

Each section or bay contains its own local cooling system. A heat exchanger transmits low-temperature air internally

through the entire bay. The flow is properly channeled in accordance with the heat load of the various racks constituting the bay, and is exhausted into the room enclosure. The cycle is completed as the room air is drawn back into the air-cooling rack of each bay. Figs. 10 and 11 show a front and back view of one of the two bays of the arithmetic and the control sections of the central processor.

A unit package method of construction has been employed with full standardization of package types, thus facilitating maintenance and package replacement. Figs. 12 and 13 show two views of one of the standard packages of the D-1000 system.

This paper is intended to give a broad, general introduction to the D-1000 system. Many of the new equipment design techniques, as well as the new programming concepts which relate to the system, will be detailed in other papers soon to be published.

Discussion

K. Phillips (Remington-Rand Corporation): Can you write both in the forward and the backward direction on one tape through the computer?

Mr. Smith: Not in both directions in the same block. We do write forward physically on one set of alternate blocks and backward on the other set of alternate blocks; logically, however, writing is nondirectional.

F. M. Goetz (Bell Telephone Laboratories): Who manufactures the magnetic tape used in this system?

Mr. Smith: The Minnesota Mining & Manufacturing Company.

W. L. Martin (Marchant Research, Inc.): What type of circuitry are you using? What do you mean by a dynamic package?

Mr. Smith: The circuitry utilizes standardized logical blocks of the buffer-gate-buffer variety and utilizes tube diode configurations. A dynamic package simply refers to a physical package or logical block, whose output is of a dynamic or continually pulsed variety. It is a 2.2-megacycle circuitry.

R. W. Beckwith (General Electric Company): How do you handle timing problems with a two-to-one difference between words consisting of nearly all zeros and words consisting of nearly all "one's?"

Mr. Smith: Actually, the words are made of equal length by adding an appropriate number of filler zeros. Since the system is asynchronous, there are no interchannel timing problems. As a matter of interest, if the number of "one's" exceeds 26, the machine automatically reverses the polarity of the signal. This refinement permits somewhat more efficient storage on the tape.

L. S. Michaels (Bendix Computer): How can you rewrite on tape when the number of one's determines the length of tape block?

Mr. Smith: A block is fixed and the physical length of the word is adjusted by adding zeros, so that the total word length on tape is considered essentially constant in the writing operation.

R. C. Jackson (International Business Machines): Does Datamatic have any plans to increase the memory capacity beyond the present 2,000 words? If so, will this necessitate a change in order-word format or word size so that memory locations beyond 2,000 can be addressed?

Mr. Smith: The memory may be increased by the addition of 2,000 words of storage; such additional memory capacity does not require any change in order-word format; instead, special memory shift-orders are utilized. It should be kept in mind, though, that the need for added memory is minimized in most instances because of the high tape input speed of the equipment, as well as the instructional content of an order itself in the D-1000 system.

R. R. Bender (International Business Machines): When a write instruction is given, how much time is required to transfer the data to be written from *A*-output buffer to *B*-output buffer before writing may begin?

Mr. Smith: The 62-word transfer from the *A*-output buffer to the *B*-output buffer is accomplished in approximately 25 microseconds. Since this is occurring concurrently with interblock tape motion, the writing operation suffers no delay whatever due to this interbuffer transfer.

D. Dittberner (International Business Machines): What do you anticipate as the largest memory which will be made available for the Datamatic? What is the memory size and what are the input-output speeds?

Mr. Smith: There might be reason to increase it to 4,000 words in some applications. The internal memory contains 2,000 words of 52 bits each. The complete access time for one word including reading and rewriting is 14 microseconds. The input-output system may operate at a sustained rate of 60,000 decimal characters per second toand from magnetic tape.

G. Bullock (Electrodata Corporation): What is meant by the term "subsequence mode?" Does this mean that the computer has more than one mode of operation?

Mr. Smith: A large class of the full complement of D-1000 orders, over and above their normal function, possess the further ability to transfer control to an arbitrary position in memory as specified by one of the addresses of the order. When this occurs, the normal sequential selection of instructions is temporarily suspended. During this suspension, the machine is said to be operating under the subsequence mode of instruction determination.

Schorr-Kon (Massachusetts Institute of Technology): Does your redundant coding dispense completely with the need for checking?

Mr. Smith: If I understand the question to refer to programmed checking, then I would say that the power of the D-1000 automatic-checking system precludes the necessity for program checks.

E. Verd (California Texas Oil Company): When will the D-1000 be ready for delivery? What is the sale or rental price?

Mr. Smith: The delivery schedule on several machines has been published. I believe the first machine is scheduled for delivery in July, 1957. The machine varies in size depending upon the application; a minimal installation runs in the range of 1.6-million dollars sales price or $35,000 per month rental including maintenance.

The Tradic Leprechaun Computer

J. A. GITHENS

Synopsis: Leprechaun is a general-purpose, stored-program, digital computer using more than 5,000 transistors Storage for 1,024 18-digit binary words is provided by a coincident-current magnetic-core memory requiring only 160 transistors. The logic of the computer is mechanized using direct-coupled transistor logic (DCTL) circuitry.

Designed for use in programming and logical design research on digital computers for military real-time control applications, Leprechaun features extreme flexibility in the logical interconnections. The computer also serves as a research vehicle for the study of the operating characteristics and reliability of transistors in DCTL circuitry and in driving a magnetic-core memory.

This paper describes the design, and construction of the computer.

PERHAPS the best starting point for any description of this computer is with the name, Leprechaun; it always evokes a number of questions. In keeping with the present trend in naming computers, it should be possible by some strange cryptography to expand the letters of Leprechaun to obtain a lengthy, more meaningful title. However, Leprechaun is merely a name which was chosen in a little contest held to determine a name. The fact that Leprechaun was the only name suggested should not detract from its fitness. For when one turns to Webster, as everyone must to check the spelling, one finds that it is a very appropriate name. Leprechaun is from the Middle Irish *lu*, meaning "little" and from *corpán*, diminutive of *corp; corp* is from the Latin *corpus* meaning "body." Little body—that is just what we were after when we started designing this machine. Further, the dictionary reveals that in Irish folklore a leprechaun is a little fairy generally conceived as a tricky old man, who if caught may reveal the hiding place of treasure. After about a year of struggle, we have caught our Leprechaun; although, we are still seeking the treasure.

Leprechaun is a solid-state digital computer developed under Air Force contract with several definite objectives in mind. First, the computer was built to demonstrate the feasibility of a DCTL system involving a large number of transistors and a moderate size magnetic-core memory driven by transistors. The computer also serves as a vehicle for continuing research and study of the operating characteristics and reliability of transistors in these techniques. Second, Leprechaun was designed for use in programming and logical design research on digital computers for military real-time control applications. To meet this last objective, the computer possesses some novel features which permit extreme flexibility in the logical interconnections.

Logical Organization

Strictly speaking, Leprechaun is a special purpose computer because the word length was determined from the control application. The machine handles 17 binary digits including sign. However, in all other respects, Leprechaun is a general-purpose computer. It is a single-address, stored-program machine with a 1,024-word random-access magnetic-core memory.

The operation code for the computer is quite complete; it provides all the common arithmetic, logical, and transfer operations as follows:

Arithmetic operations
- CLEAR AND ADD
- CLEAR AND SUBTRACT
- CLEAR AND ADD ABSOLUTE VALUE
- CLEAR, ADD AND INCREASE
- ADD
- SUBTRACT
- MULTIPLY
- DIVIDE
- ADD WITHOUT CARRY
- EXTRACT
- SHIFTRIGHT
- SHIFT LEFT

Load and store operations
- LOAD MQR
- STORE
- STORE ADDRESS
- STORE MQR

Jump operations
- UNCONDITIONAL JUMP
- JUMP IF PLUS
- JUMP ON OVERFLOW
- JUMP ON NON-ZERO
- STOP AND JUMP
- SUBROUTINE JUMP

Input-output operations
- READ CHARACTERS
- PRINT CHARACTERS
- READ AND STORE
- PRINT FROM STORE

Miscellaneous
- REPEAT
- SET ADDRESS MODIFIER

The code has been designed to eliminate the need for many of the usual red-tape operations. For instance, a special unconditional jump operation (subroutine jump) is provided to simplify the inclusion of short subroutines in a program. The first use of the operation transfers control to the desired loop in the program; the second use returns control to the point in the main program from which the jump was made.

Studies show that the ability to operate on instructions is no great advantage in control computers because the stored copy of the original program must be retained intact. A *B*-box or index register would be very useful. However, a *B*-box is quite expensive and slow in a parallel machine. Instead, Leprechaun incorporates a simplified-address modification operation in which modification is accomplished by direct substitution. The contents of a 5-bit address modifier register are substituted for the five least significant address digits of all instructions in which these five digits are zeros. This does not alter the stored instruction and requires no tags on the instructions to be modified.

The inclusion of such operations at a modest cost for equipment saves program steps and time, items of particular importance in real-time control computers. In logical organization, Leprechaun can be considered a member of the "Institute of Advanced Study" machine family for it is parallel, asynchronous, and all shifting registers and counters use the double rank technique. In general, the major units of the computer operate almost independently, at their own speed, doing as much as they can until forced to stop and wait for the services of some other unit which is busy.

Direct-Coupled Transistor Logic

The logic of the Leprechaun is mechanized by using DCTL. DCTL is our name for the switching circuit technique in which transistors are used to perform logic as well as to provide gain. This circuitry is similar to that described by Beter, Brown, Bradley, and Rubinoff of Philco at the 1955 Institute of Radio Engineers Convention,[1] and in the paper by Maddox, O'Toole, and Wong[2] presented at this conference, except that we use alloy junction transistors for the most part. Our design philosophy and transistor specifications were described in general terms by J. R. Harris and J. W. Easley.[3]

J. A. GITHENS is with Bell Telephone Laboratories, Inc., Whippany, N J.

Leprechaun was developed under a program sponsored by the Air Material Command, U.S. Air Force on Contract AF33(600)-21536

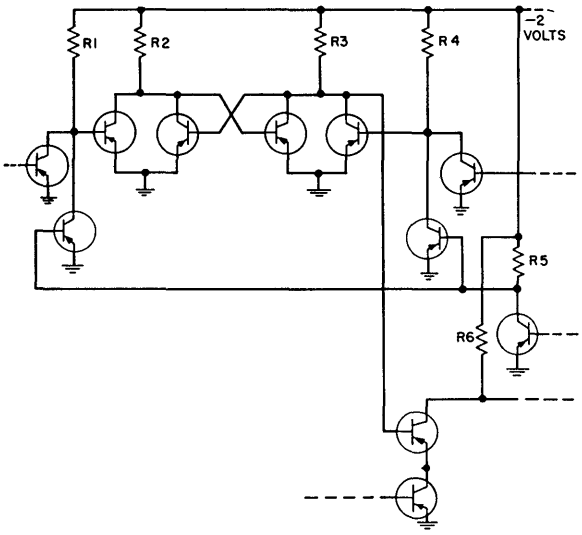


Fig. 1 (left). Typical DCTL circuit

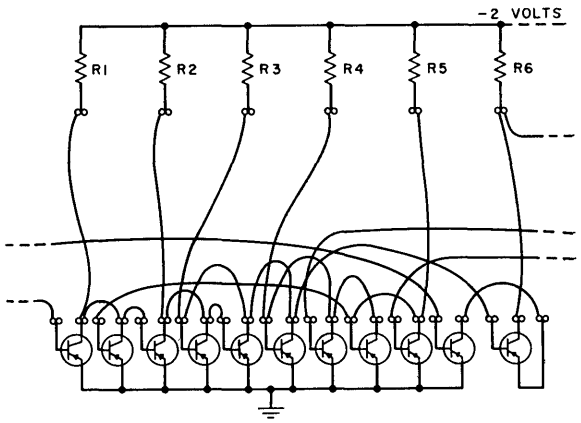


Fig. 2 (right). Same circuit redrawn in different form

The extreme flexibility desired in the logical interconnections has led to an unusual packaging of the computer. In this use has been made of the unique properties of DCTL. To illustrate, consider the typical DCTL circuit shown in Fig. 1. This circuit, which is actually a portion of a shift register, was chosen because it contains all of the commonly encountered DCTL circuit configurations. There are a number of interesting points. First, of course, is the much advertised fact that DCTL uses only two components, resistors and transistors, and only a single voltage supply. Note that the ratio of resistors to transistors is about one-half. Also, we find that advantages in construction and flexibility of making these resistors all a single standard value outweigh the slight circuit inefficiency. The point to note here is that there are only two basic transistor connections, the parallel and the series connection. The more sophisticated circuits are all simply combinations of these basic configurations. For example, the flip-flop circuit is merely two parallel circuits intercoupled.

The same circuit in a different form is shown in Fig. 2. Here it has been redrawn to achieve complete order in the components and all the complexity that is the logic resides in the interconnections. Thus, since it was just noted that any DCTL circuit can be realized using these basic configurations, this arrangement can be used to make up any desired DCTL circuit by simply changing the interconnections. To facilitate changing, the interconnections are made with jumpers as indicated. To reduce the crosstalk inherent in this technology, we have designed our packages to minimize the common emitter or ground connection.

The construction details are illustrated in Fig. 3. A ground plane is pierced with posts to which the transistor-emitters are solderless wrap-connected. The transistor base and collector leads are each connected to two taper-pin receptacles. Similarly, one end of each supply resistor is connected to the voltage buss, the other end to two taper-pin receptacles. This end of each supply resistor, which is a circuit nodal point, is also brought out as a test point. The interconnecting jumpers use Aircraft-Marine Products taper pins.

One of these assemblies is shown in Fig. 4. It is a 3-member assembly in which the center member contains the grounded-emitter transistors, and the two identical outer members contain the supply resistors and transistors having receptacles on all three leads for use in series circuits. The ground plane runs through the middle of the center member with transistors mounted on both sides. The center member mounts 720 grounded-emitter transistors in an area of only 7 by 9.5 inches. All the points of interest in the unit are available as test points on the outer surface of each outer member. The outer members are hinged and swing out to give access to the wiring surfaces. In all, the package, if it can still be called that, contains 976 transistors and 504 supply resistors. It occupies less than 0.8 cubic foot, and weighs 34 pounds when fully wired. The nominal supply voltage is 2 volts, and the standard supply resistor value is 510 ohms giving a 4-milliampere current level in DCTL circuitry.

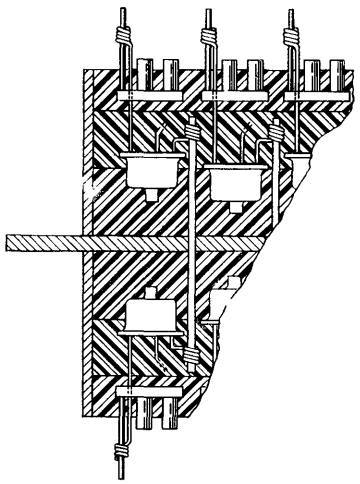


Fig. 3. Same circuit redrawn in different form

Thus, with the logic of the computer mechanized and using six of these units, with the interconnections made with jumpers which provide reliable electrical connections, yet are easily connected and disconnected, the flexibility objective has been fulfilled. The result, in effect, is a pluggable computer that can be used to test any number of logical designs and permits micro-micro-programming.

Magnetic Core Memory

Storage in Leprechaun is provided by an 18,000-bit coincident-current magnetic-core memory driven by 160 transistors. The memory is organized to store 1,024 18-digit words including a parity check bit that serves as a check on memory operation only. Access to the 1,024 words is provided by coincident-voltage magnetic core-diode switches,[4] which use 48 switch cores and 160 diodes.

The cores were developed, manufactured, and assembled to our specifications by the International Telemeter Corporation. The digit planes are rectangular folded arrays of 64 rows of 16 cores each as shown in Fig. 5 (a portion of this photograph has been enlarged to show the core details). Eighteen planes are assembled into a three dimensional array which occupies less than 0.9 cubic foot as shown in Fig. 6.

The core material used resembles the S3 ferrite material and switches in slightly less than 4 microseconds on a current of

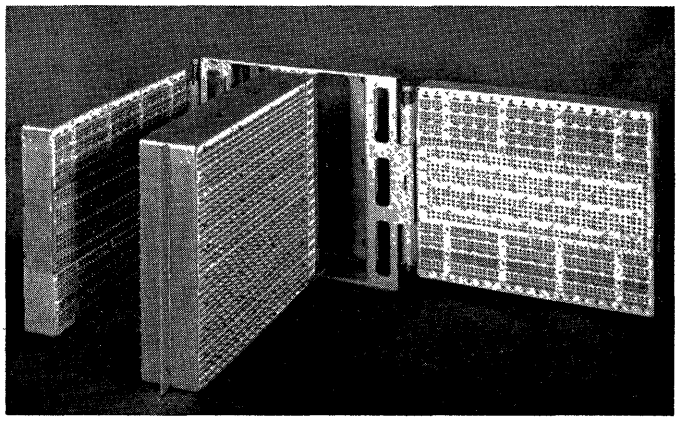


Fig. 4. Three-member assembly

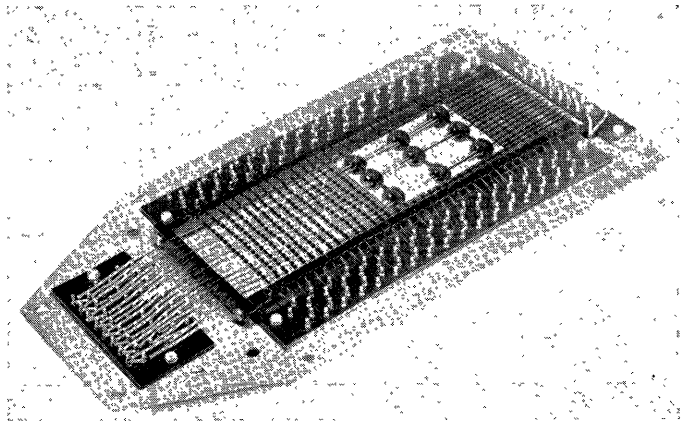


Fig. 5. Memory digit plane

360 milliamperes. We make use of International Telemeter's system of staggered read drives[5] in which the read current applied to the columns (the long dimensions of the rectangular planes) precedes the read current applied to the rows. This allows the larger disturbance caused by the column drive to die out before the row drive is applied. We use a stagger of 2 microseconds and obtain a very good one to zero ratio. A measure of the one to zero ratio is provided by the fact that the memory operates over a temperature range of 50 to 100 degrees Fahrenheit with good margins and without any adjustment or compensation. Using this core material and the staggered drives we achieve a 20 microsecond read-write cycle.

To provide the read and write drives, to inhibit the writing action in those digit planes where zeros are to be written, and to set the access switches, the memory uses 62 two-stage transistor amplifiers. These circuits amplify the DCTL inputs to provide drive currents ranging from 70 to 200 milliamperes. In addition, 36 transistors are used in two-stage read amplifiers to raise the 18 parallel output signals to a sufficient level to drive DCTL circuitry. This memory system was described in detail by E. L. Younken.[6]

Power Supplies

In keeping with the rest of the computer, the power supplies are solid-state circuits also. Basically they are fast magnetic regulators using transistorized drivers. The coincident-current operation of the magnetic-core memory places some rather severe requirements on the supplies. For example, the 8±2 volt supply for the memory has a static regulation of ±1% (per cent) for an output current range of 0 to 1.8 amperes and its dynamic regulation is less than ±3% under a pulsing load of 1.6 amperes. This is a high performance supply and yet, as shown in Fig. 7, it is a very small unit, occupying less than 0.2 cubic foot.

The DCTL portion of the computer operates at −2 volts and dissipates about 20 watts. Of this figure, less than 2.5 watts are dissipated in the transistors. The memory uses two voltages, −22.5 and −8 volts, and dissipates about 48 watts. By way of contrast, roughly 50 indicator lamp circuits, which operate from a 5 volt supply, dissipate 10 watts. This adds up to a total dissipation of 78 watts and, with the power supplies 50% efficient, the input power is only about 160 watts, slightly more than your home television receiver uses.

Components

One of the advantages of DCTL is the drastic reduction in the number of components; excluding the magnetic cores, Leprechaun uses only on the order of 9,000 electrical components. More than half of these are transistors. The computer actually contains more transistors than this because, with the DCTL packaging used, it is very difficult to remove and replace transistors. Therefore, extra transistors are packaged right in the assemblies to be used for future expansion in keeping with the flexibility requirement and to serve as spares in the event of failures. The fact that such a technique was used willingly indicates our confidence in the reliability of transistors in general and in DCTL circuitry in particular.

For DCTL p-n-p germanium alloy junction transistors with 7-megacycles alpha cutoff selected to our DCTL specifications are used. The computer contains three varieties: selected Raytheon *CK761* transistors and two codes of selected General Electric *2N137* transistors. The yields of these transistors to our specifications are 35 to 40% for the *2N137* and 50 to 60% for the *CK761*. To a looser specification, which necessitates some circuit limitations, the yields are increased to about 80% for the *2N137*. The *CK761* transistors selected to this looser specification would give practically 100% yield. Roughly 6% of the DCTL transistors are selected Philco Surface Barrier *SB100* transistors. The greater speed of these units is used in those places where accurate timing is important, e.g., the timing relation between memory read drives and the strobe. To develop the high current drives required in the memory, the computer uses Western Electric *GA52830* transistors.

The Computer Assembly

Now that all of the major components of the computer have been discussed, what does a complete Leprechaun look like? A front view of the computer is shown in Fig. 8. The upper portion of the front of the machine is occupied by the control panel. At this point provision is made to display the contents of all registers in the machine and the state of the critical control flip-flops. The control panel also contains all the manual control switches and selectors. For program debugging and trouble shooting purposes, provision is made for manually setting of the registers and control flip-flops and for a manual break-point setting.

The lower portion of the front of the machine is occupied by the power supply control panel. This panel contains the power supply adjustments, current and voltage test points, and the fuses. A hinged panel which contains the marginal checking equipment is shown in the lowered position. This panel contains switches that divide the DCTL portion of the computer into 36 parts for marginal checking purposes.

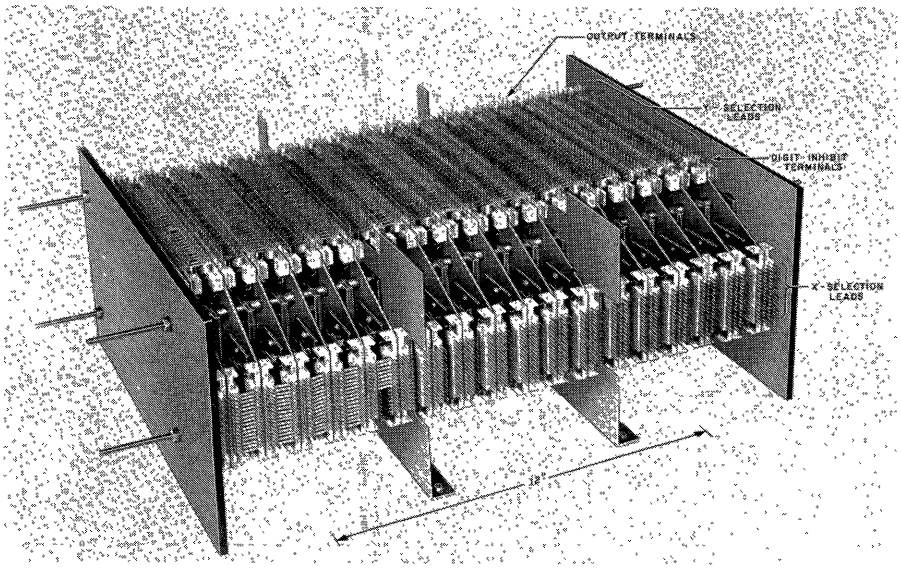


Fig. 6. Memory storage array

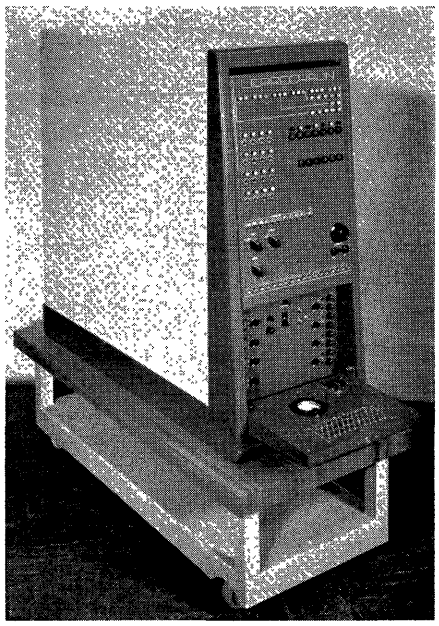


Fig. 8. Front view of computer, cover on

Fig. 9 shows a side view of the computer with the cover removed. Directly behind the control panels are mounted the eight power supplies used by the computer. The six DCTL assemblies are mounted behind these. One of the assemblies is shown open giving access to the interconnecting wiring. The memory array is mounted above the DCTL section. The associated transistor circuitry is located about the array on printed circuit plug-in cards.

In all, the computer occupies slightly over 15 cubic feet. This is the complete computer with the exception of input-output equipment. In their normal use, control computers must accept analog inputs and produce analog outputs for the most part (with intermediate conversion, of course). To make Leprechaun useful for programming research, however, it is provided with paper-tape input and output equipment. The primary input is a Ferranti photoelectric reader and the primary output is a Teletype high-speed punch. A manual keyboard for input and an electric typewriter for output are provided for optional use.

Summary

Leprechaun is a special-purpose, low-power, solid-state, digital computer having general-purpose capability. The extreme flexibility permitted by the design makes the computer an ideal test bed for logical design innovations. The present operation code makes the computer very versatile. However, should it ever prove inadequate, the operation code can be expanded or modified with comparative ease. Finally, I should say that Leprechaun is a good example of the impact that transistors and solid-state devices are having on the computer art.

It must be obvious that a project of this nature is the work of many people from several departments of the Bell Telephone Laboratories. Some of the people instrumental in the program were mentioned in the text. Mentioned but unnamed was our logical designer, R. A.

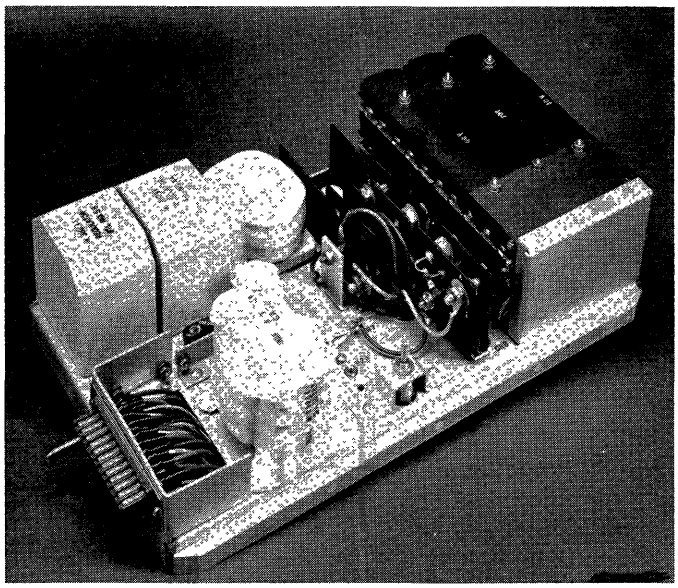


Fig. 7. Power supply unit

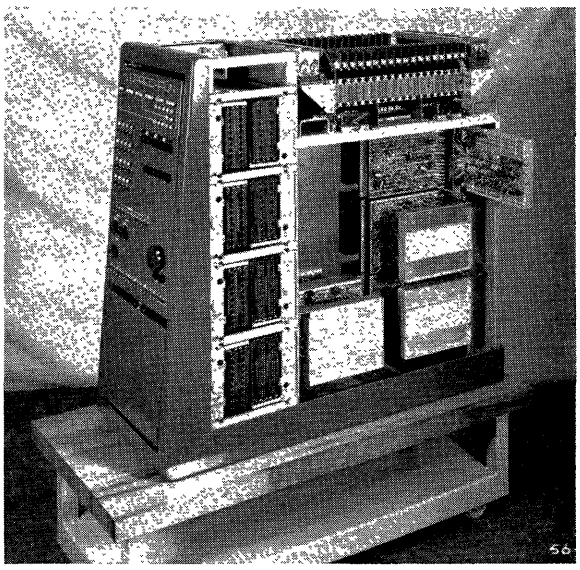


Fig. 9. Side view of computer, cover off

Kudlich, who was responsible for the system and logical design, but will probably be remembered longest for contributing the name Leprechaun.

References

1. Surface Barrier Transistor Switching Circuits, **R. H. Beter, R. B. Brown, W. E. Bradley, M. Rubinoff.** *Convention Record,* Institute of Radio Engineers, New York, N Y, pt IV, Mar. 21, 1955, pp. 139–45.

2. Eastern Joint Computer Conference *AIEE Special Publication T-92.* "The Transac S-1000 Computer," **J. L. Maddox, J. B. O'Toole, S. Y. Wong.** May 1957, pp 13–16.

3. Direct-Coupled Transistor Logic Circuitry in Digital Computers, **J. R. Harris.** Transistor Requirements for Direct-Coupled Transistor Logic Circuits, **J. W. Easley.** Joint IRE–AIEE Transistor Circuits Conference, Philadelphia, Pa., Feb. 1956.

4. Pulse-Switching Circuits Using Magnetic Cores, **M. Karnaugh.** *Proceedings,* Institute of Radio Engineers, New York, N. Y., vol. 43, 1955, p. 570.

5. Recent Advances in Coincident Current Magnetic Memory Techniques, **R. Stewart-Williams, M. Rosenberg, M. A. Alexander.** *Proceedings,* Association for Computing Machinery, Ann Arbor, Michigan, June 1954.

6. A Transistor-Driven Magnetic-Core Memory, **E. L. Younker.** *Transactions,* Institute of Radio Engineers, New York, N Y, vol. EC6, no. 1, Mar. 1957.

Discussion

V. Sferrino (Lincoln Laboratory, Massachusetts Institute of Technology): Do you contemplate the design of an all-transistor memory using S1 cores which require higher drive currents but which switch faster than the S3 cores?

Mr. Githens: I think that we will undoubtedly get to it because of the ever present need for faster operation. The S3 material was used first for the reason you state, that is, because it is, at least in order of magnitude a greater problem to provide the higher drives and the greater speeds required for the S1 material with presently available transistors.

A. S. Robinson (Bendix Aviation Corporation): Do you feel that the DCTL technique is superior in all respects to standard implementations? If not, would you discuss limitations you have encountered?

Mr. Githens: The answer to that must be a qualified yes. Yes, if speed is not of primary importance. The greatest attraction of DCTL is its simplicity, reduction in number of components, and reliability. Several systems have been described this afternoon, each of which proposes the use of thousands and thousands of transistors. Undoubtedly, larger systems will be built. If systems of this size are to be practical, the circuits used must be simple so that they will lend themselves both to understanding and to automation techniques, and, above all, they must be reliable.

These features in DCTL are not achieved without some cost. The outstanding cost is a reduction in speed due to the fact that DCTL relies on saturating the transistors. In our system, 7-megacycles alpha cutoff transistors are used and achieve something like 300-kilocycles per second operation. By using more components to either keep the transistors out of saturation or to pull them out fast when turned off, one might be able to operate reliably at 1 or 1.5 megacycles with the same transistors. Similarly, at a cost of more components, another power supply, and more power dissipation, one could back-bias off transistors and reduce the crosstalk.

Thus, if speed is of paramount importance or if the units can not be made compact enough to control the crosstalk, then DCTL is not the technique to use. Otherwise, I think it is. It should be noted that with diffused base techniques the silicon transistors on the near horizon, the prospects for increasing the speed and decreasing the susceptibility to crosstalk with DCTL are very good.

G. E. Knausenberger (Haller, Raymond and Brown): For which circuits do you use spare transistors? Can you indicate the total fraction of spare transistors built in?

Mr. Githens: Each book, as we call them, or transistor assembly contains 976 transistors and the logical designer was told that he should use about 850 and leave the rest for spares. These spares serve both for future expansion, in keeping with the flexibility objective if the unit were asked to do more than was originally intended, and for replacement of failures; so that the total is about 15% at present. Of these half were for future expansion and half for replacements.

H. Boynton (Philco): How many bases can be driven from one collector? Do you use circuits other than grounded-emitter configuration?

Mr. Githens: With parallel circuits, we specify the number of collectors and bases that can be attached to one supply resistor, and that results in any combination totaling seven. In the extremes, you can have one collector driving six bases or you can have a six terminal circuit, or six collectors, driving a single base.

We provide for some series circuits. In each assembly, roughly 25% of the transistors have all three terminals available for use in series circuits. However, our logical design rules permit only two-terminal series circuits and each series circuit input requires $2\frac{1}{2}$ times as much current as a parallel circuit. You can understand this by the fact that in a workable system the top collector in a series connection of transistors when turned on must get down to the same level as a collector in an on-parallel circuit. Therefore, you say the series circuit has only 40% of the gain of a parallel circuit.

While the series circuit is logically quite useful, the parallel circuit with its inversion does provide a complete logical set; and because of the restrictive gain, the series circuit finds very little use, and there are very few series circuits in the computer.

E. F. Morris (International Business Machines Corp.): How many n-p-n transistors do you use?

Mr. Githens: None. We only have a single negative voltage supply. No particular reason for choosing p-n-p units over n-p-n units, but, of course, there is a big advantage in using only one polarity.

C. M. Theiss (A.C. Spark Plug, General Motors Corporation): What are the temperature limitations?

Mr. Githens: The temperature limitations are set by the magnetic-core memory, which operates from 50 to 100 degree Fahrenheit. We have set up the logical design rules for the DCTL circuitry to operate up to 40 degrees centigrade. There is no reason to push it any higher, since the memory will not work above that level.

A. Weinberger (National Bureau of Standards): What are the operation times of the Leprechaun Computer with and without memory reference time?

Mr. Githens: With the stored program operation and a 20-microsecond memory read-write cycle, simple operations, such as addition or subtraction, can be performed in 40 microseconds. Multiplication takes, on the average, 370 microseconds. The basic addition time is about 18 microseconds

Chairman Scott: Any data on reliability? How many Leprechauns are there in current use?

Mr. Githens: None on Leprechaun, as it has not been assembled yet. But enough has been done with DCTL and magnetic-core memory to convince us that they are reliable. The magnetic-core memory has been in operation for some six months in a memory test system which involves 1,000 transistors in DCTL circuitry to exercise, control, and check the operation of the memory. The operation of both the transistor driven memory and the DCTL has been completely satisfactory and we are proceeding at full-speed. There is only one Leprechaun, and it is not yet complete.

Functional Description of the NCR 304 Data-Processing System for Business Applications

M. SHIOWITZ A. A. CHERIN M. J. MENDELSON

THE National Cash Register Company (NCR) 304 system is a moderate-sized electronic data-processor for general business use. It incorporates many new design concepts which result in performance capabilities comparable to those of a large scale system. Each of the features was designed to provide maximum versatility in the handling of business data. The NCR 304 system offers the advantages of electronic data-processing to many organizations that have not yet found it economically feasible.

System Components

The major components of the NCR 304 system are depicted in the system block diagram of Fig. 1. They include the following:

Input Devices

A variety of keyboard data-entry devices which capture input information on punched paper-tape as a by-product of essential decentralized transaction recordings; these include cash registers, unit media readers (for reading price tags, customer tokens, clerk tokens, etc.) accounting machines, adding machines, window posting machines, and electric typewriters; all these devices are equipped with punched paper-tape recorders, and programming plugboards which permit flexible data arrangement.

Control Console

The control console provides the power control, indicator lights, and operating switches for all units in the system which are connected directly to the central processor. The operator's control panel contains a lighted display for processor operation and for the operation of auxiliary equipment, and a paper-tape or keyboard operated electric typewriter which provides direct communication with the processor memory.

Central Processor

The Central Processor controls and, to a large extent, executes the stored program of data-processing operations. The high-speed main memory is of magnetic-core construction with a storage capacity of 1,000, 2,000, or 4,000 ten-character words. Transistors and magnetic cores are employed throughout as logical elements because of their low power requirements, low heat generation, high reliability, and compact size.

Access to the main memory is fully parallel, one word at a time. Processing is carried out in serio-parallel fashion, the bits of a character being treated in parallel, and the characters of a word treated serially. The basic repetition rate of the processor is 400,000 characters per second. A word is accessed, processed, and stored (or restored) in 60 microseconds, constituting a minor cycle of the machine.

Paper Tape Reader

High-speed photoelectric punched-paper tape reading is provided by the NCR Model 360. For flexibility, the reader is capable of reading five, six, seven, or eight channel tape. Any punched-hole code can be translated by the reader provided it contains fewer than 65 distinct characters. The reader operates on an individual character stop-start basis with a continuous reading rate of 1,000 characters per second.

Punched Card Reader

The NCR Model 380 photoelectric card reader provides high-speed punched card input. The reader is capable of handling 80-column IBM (International Business Machines, Corp.) cards. Provision is made for reading a portion, or the full 80 columns, of each card. Each card column may contain numeric, alphabetic, or symbolic punching. Card reading is performed at the rate of 500 cards per minute.

Magnetic Tape File

The NCR Model 330 magnetic-tape file provides large capacity auxiliary storage. Data is stored on the tape in the form of records which may be of variable length. Each 2,400 foot-reel of tape stores approximately 4,300,000 characters. Information is recorded on tape at a density of 150 characters per inch, without gaps, between records. The tape moves at 100 inches per second with an acceleration time of 5 milliseconds. The information transfer rate is 15,000 characters per second. A minimum file consists of one control unit with up to eight tape handlers under its control. As many as eight controller units can be employed in a single system.

Line Printer

The NCR Model 340 line printer produces printed output either directly from the processor memory or from magnetic tape. The printer is capable of printing 120 characters per line at a rate of 600 lines per minute. Fifty-six different characters may be printed. All paper spacing functions where no printing is required are performed at the rate of 72 lines per second. Multiple copies may be produced efficiently through the use of NCR carbonless paper, or standard carbon interleaved forms.

Multi-Purpose Converter

The NCR Model 320 converter transcribes records from one form of storage to another. Specifically, the converter can perform the following transcriptions: magnetic tape to printer, magnetic tape to punched paper tape, magnetic tape to punched cards, and punched cards to magnetic tape.

Printer-Converter

The NCR 322 converter transcribes data from magnetic tape to the high speed printer

Paper Tape Punch

The NCR Model 370 paper-tape punch provides punched paper-tape output directly from the Model 304 central processor, or from the Model 320 converter. Two different hole codes may be obtained at a punching rate of 60 characters per second. One of these codes is the processor code and the other is optional, and may be specified by the user to conform with leased line communication equipment being used in integrated data-processing systems.

M. Shiowitz and A. A. Cherin are with the Electronics Division, National Cash Register Company, Hawthorne, Calif. M. J. Mendelson formerly with National Cash Register is now with Norden-Ketay, Hawthorne, Calif.

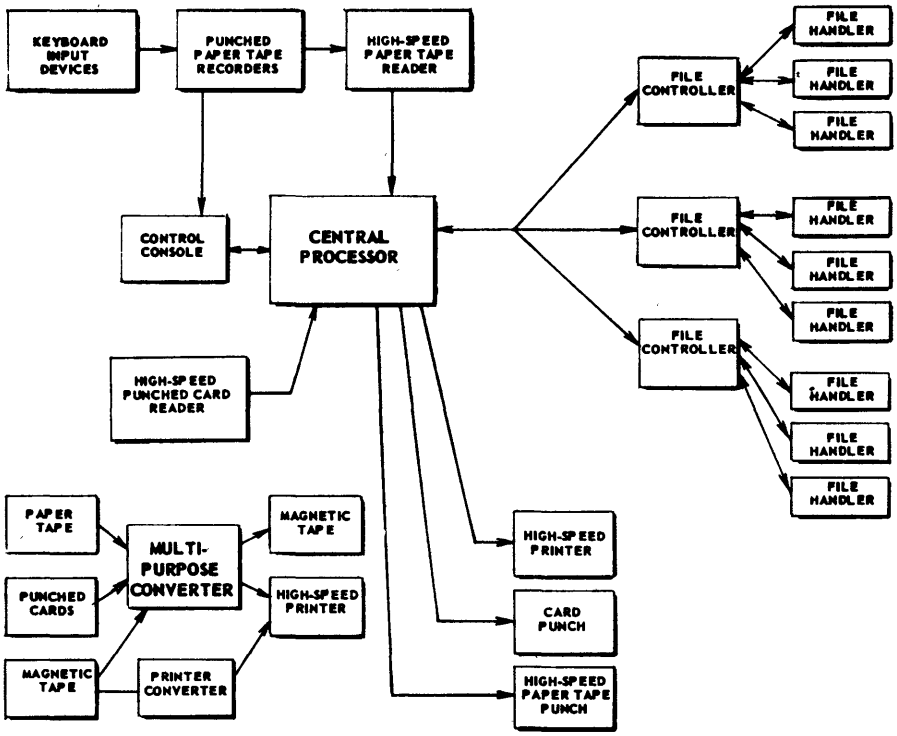


Fig. 1. Major components of the NCR 304 system

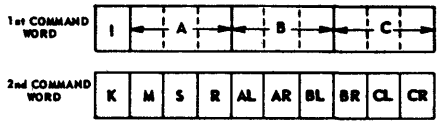


Fig. 2. Structure and component parts of a typical two-word command

Card Punch

Punched card output is provided from magnetic tape through the converter to an IBM Type 523 Summary Punch. Card punching is performed at the rate of 100 cards per minute.

Central Processor Characteristics

Code and Number System

Six-bit alphanumeric characters comprise the basic code of the system. An excess-zero binary coded decimal number representation is used for numeric characters, with the fifth bit of the most significant decimal digit of a numeric field serving as an algebraic sign. For decimal arithmetic operations, operands, and results are regarded as absolute value and sign.

Addressing and Field Specification

Because of the variability of field size in business-data processing applications, both within a single application and among several applications, the 304 utilizes a rather unique language for addressing and specifying the variable size of units of information to be processed.

In addressing ten-character words in the 1,000, 2,000, or 4,000 word core memory, addresses consisting of three characters are used. To refer to addresses other than 000–999 (i.e., in machines with the larger core memories) use is made of an alphabetic character in the most significant position of the address.

A sequential group of from one to ten characters within a word comprise an addressable field. These partial word fields are specified by two decimal digits used in conjunction with the three-character word address; one being used to locate the least significant, the other the most significant, characters of the field within the word. In arithmetic operations each field is treated as an individual unit containing its own sign. Alignment of fields for proper operation is performed automatically by the machine.

Since a variety of multiple-word fields must be addressed and processed in business applications, an appropriate addressing scheme for each type has been incorporated in the command structure.

1. Lists of fixed-length multiple-word items: when a sequential group or list of items of common length are to be processed as a unit, the item length in words is specified within appropriate commands by a two or three character quantity. The total size of the list is determined in either of two functionally equivalent fashions: if the size of the list is a function of and is generated by the data being processed, which is often the case in transfers of lists of items between the processor and the input transcribers or the magnetic file, size specification usually consists of a tally of the number of items in the list; if the list size is essentially independent of the data being processed and is generated by the programmer, it is generally indicated by the specification of a terminal word address which locates the end of the list. Accompanying the item length and an initial word address locating the first word of the first item, either the item tally or the terminal address completely specify the location, size, and structure of the list.

2. Variable-length multiple-word items: in those cases where the length is a function of the data, e.g., in multiple-word instructions and variable-length magnetic file records, the information specifying item length is contained in the item field itself.

Where the programmer generally specifies item length, it is contained in the instruction which calls for the operations on the item. Control words, such as a key in a sorting process, contained in multiple-word items are addressed by specifying their position relative to the first word of the item.

Relative Addressing

Every command can utilize a relative address facility to permit automatic selective modification of command addresses for the execution of repeated routines and other useful memory indexing operations, thus saving considerable command storage space and execution time.

Address Modification

With respect to all automatic processor operations, such as augmenting control number, index register modification, automatic tallying during command execution, etc., the word addresses are continuous and cyclic.

The circuitry associated with the addition involved in these operations is mechanized to count sequentially from the first thousand to the second, third, or fourth thousand words, (depending on memory size), and cycle back to 000 when the end of the memory is reached. Thus address modification is modulo the size of the memory.

Special Memory Cells

In addition to the main memory, 40 special addressable cells are provided. These special memory cells may be used as data addresses in any command,

but are not included in the cyclic portion of the memory. Six of these addressable cells have special functions and are used by the machine during normal operation. The functions of these special cells are as follows: one is used to store automatic tallies generated on input and magnetic file operations, and for results in certain arithmetic commands and is named the tally register; another is the control register which contains the address of the next command in sequence during automatic processor operation, as well as an unconditional jump address. Four additional cells are used to store information during an automatic monitoring procedure.

The remaining 34 cells are available for storage at the discretion of the programmer. Since the special cell addresses are not included in the normal modification cycle of the machine, information stored therein will remain unaltered unless referred to specifically and individually.

Command Sequencing

During the automatic processor operation commands are normally executed sequentially, the address of the first word of successive commands being obtained by augmenting the right-hand address part, or *C* address, of the control register by the word length of the command being executed. When a transfer of control or jump is to occur, the contents of the *C* portion of the control register are replaced by the jump address.

In addition to the conditional jumps or branches which occur as the result of explicitly programmed examination of operands, a number of automatic branch operations are possible when exceptional conditions arise in the data or status of the components handling the data media. The sensing of these conditions is essentially a motor function performed by the logical elements of the control section of the processor. This automatic branch facility provides for execution of a number of control decisions inherent in all applications without explicit programming of the test.

A self-linking feature of the processor provides each command with the optional ability to automatically cause an unconditional jump and storage of a link address. The unconditional jump address is taken from the middle address part, or *B* address, of the control register, and the link address is stored by an interchange of the *B* and *C* portions prior to the access of the next command. This control of command sequencing is specified by one of the bits in each instruction. It is valuable in many areas of programming, such as the design of closed subroutines.

Command Structure

The general characteristics of the 304 commands are difficult to classify in terms presently prevalent in the field. Enlarging the definition of the term address to include, where applicable, the variable size as well as the location of the operand or field, it can then be stated that the 304 has a multiple-address code with the number of addresses per command ranging from three to eleven, with optional automatic relative address modification, automonitor control, self-linking, and automatic branching.

A majority of the commands in the 304 repertoire consist of two words; the structure and component parts of a typical two-word command are shown in Fig. 2, and are explained as follows:

I and *K*, (each one character) specify the operation to be performed; the sign of *K* controls the self-linking characteristic described above.

A, *B*, *C*, (each three characters) are normally used as operand word addresses.

M, (one character) specifies the level of automatic program monitoring to be executed during processor operation in the monitor mode. Optional operator control of automonitoring is permitted by a switch on the control console.

R, (one character) specifies the index register to be used for relative modification of addresses *A*, *B*, *C* prior to execution of the command.

S, (one character) selectively specifies the combination of addresses *A*, *B*, *C*, to be modified by the corresponding contents of *R*.

AL, *AR*, *BL*, *BR*, *CL*, *CR* (each one character) identify the left-most and right-most digit positions of the partial word fields within *A*, *B*, and *C* respectively.

Since the use of the relative address and partial word modifiers are optional, the total effective operand will be briefly referred to hereinafter as *A*, *B*, or *C*.

Internal Two-Word Commands

The command list of the central processor contains 22 internal operations which are specified by two words of instruction information:

Decimal Arithmetic Commands

The five operations comprising this group are:

1. Add: *A* is added to *B*, the sum is stored in *C*.
2. Subtract: *B* is subtracted from *A*, the difference is stored in *C*.
3. Multiply: *A* is multiplied by *B*, the most significant portion is optionally rounded and stored in *C*, and the remaining portion of the product is stored in the tally register.
4. Divide integers: *B* is divided by *A*, the integer quotient is optionally rounded and stored in *C*, and the integer remainder retaining the sign of *B* is stored in the tally register.
5. Divide fractions: *B* is divided by *A*, the rounded quotient is stored in *C*.

The signed numeric operands have their decimal point immediately to the right of the least significant digit in operations 1, 2, 3, and 4. In the divide fractions command, the decimal point is immediately to the left of the most significant digit. In commands 3 and 4, the rounding option is specified by instruction character *K;* the digit position in which rounding occurs is automatically determined by the number of digits allocated to result storage in *C*.

Overflow occurs in those cases of execution of add, subtract or divide integers commands where the number of significant (non-zero) digits of the result exceeds the capacity of the storage field specified by the digits, *CL*, *CR*. In this event, an overflow alarm indication is automatically stored in the control of the machine, and unless the next command executed is a branch command which tests this overflow alarm, an error halt occurs.

Non-Decimal Arithmetic Commands

Because the arithmetic requirements of address modification and other program control operations in multi-address computers differ markedly from those of decimal calculations involving business data, the command code includes three non-decimal arithmetic instructions. Two operations expressly designed to permit flexible and efficient memory indexing are:

6. Modify add: *A* is added to *B* and the sum is stored in *C*.
7. Modify subtract: *A* is subtracted from *B* and the result is stored in *C*.

These operations are modular with respect to memory size, and all carries are suppressed between adjacent triads (3-character addresses) in multiple-address operand fields. Hence the execution of a single additive or subtractive modification can provide for the simultaneous indexing of up to three addresses.

The usefulness of the relative address facility is further enhanced by the following command:

8. Index: A is added to one of the 10 index registers and the sum stored in the same index register; the addition is performed as described above, following the modification, a specified portion of the index register is compared with the number contained in the B address part of the command, and an optional branch address is chosen on the basis of the comparison. This structure permits the automatic termination of a modification loop.

Compare Commands

The three compare operations include:

9. Compare numeric: A and B are compared algebraically, and a branch to C occurs if A is greater than B.

10. Compare alphanumeric: A and B are compared alphanumerically, and a branch to C occurs if A is greater than B.

11. Compare equality: A and B are compared alphanumerically, and a branch to C occurs if A is equal to B.

Due to the nature of sign representation in the processor, execution of command 11 with numeric operands will result in a branch if and only if the signs as well as the absolute values are equal.

Editing Commands

Five commands were designed for fast flexible editing and rearrangement of data, which are necessary procedures in all business programs.

12. Compress: the fields A and B are assembled and the resultant combination field is stored in C.

13. Distribute: the field A is distributed into (the partial word field storage locations) B and C. An optional sign split-off in the field distributed is specified by the value of K. Sign split-off consists of generating a nonsignificant or signed-zero character, and inserting it in the extreme left character position of the stored field. (Sign compression, which is the inverse operation, occurs automatically as a result of logical mechanization.)

14. Zero suppress: the field A is zero suppressed, and the result with optional sign split-off is distributed into B and C.

15. Edit: the field A is either zero suppressed, or check protected and distributed into B and C. The option of suppression or protection is exercised by specifying the value of K.

16. Transfer: the contents of a consecutively numbered block of memory word cells beginning at A, are transferred to a block of cells beginning at C. The number of words transferred may range from 1 to 1,000, 2,000, or 4,000, depending on memory size.

Binary Commands

In many programming areas the advantages in storage efficiency of binary codes is not offset by the requirement for frequent conversions to decimal or alphabetic representation. The processor design allows for optimum economy of hardware application in these areas by providing five commands of binary nature:

17. Extract: the bits of A are logically multiplied by the bits of B and the logical product is stored in C.

18. Insert: the logical product of A and B, and the logical product of C and the complement of B are formed. Then the logical sum of these two products is formed and stored in C.

19. Test Bit: a bit by bit test of A and B is made; if A has a bit value of one in every bit position in which B contains a bit value of one, a branch to C occurs.

20. Pack: this command packs a group of consecutive three-word blocks of positive-numeric data into a group of consecutive two-word blocks by dropping the two most significant bits of each six-bit character. It should be noted that for positive-numeric data, these bits are uniformly zero.

21. Unpack: the inverse of the pack command.

Test Command

The final command in this list is a general-purpose jump command:

22. Test: this command tests the status of a set of control-console switches, the paper-tape punch, the paper-tape reader, or the overflow alarm, as determined by the value of K. The program can branch as a result of the test, thereby permitting operator intervention to control program execution.

Internal Multiple Word Commands

The NCR 304 includes a set of instructions which are equivalent to complete subroutines in machines with conventional codes. These commands have been carefully chosen to be of general applicability to all business data processing, and have been designed to insure maximum flexibility. The usage of a single command to carry out a substantial processing subroutine provides considerable savings in execution time and storage requirements over conventional programmed subroutines. Three of these are internal multiple-word commands.

23. Merge: this command merges two distinct sorted groups of consecutively stored, multiple-word items (groups A and B) into a single sorted sequence (group C). The data in groups A and B must be standardized such that each item contains the same number of words, and the control key characters (the numbers which determine the sort sequence) must occupy the same relative positions within each item. It is however not necessary to have the same number of items in groups A and B.

This command may be executed in two alternative fashions: one mode is used when the data to be sorted can be completely stored in the internal memory; the other mode is used when the volume of data exceeds the memory capacity and magnetic tape is used for auxiliary storage. In either mode, the command is specified by six words of control information, in which the programmer specifies the following variables:

The location of the first words of the first items of group A and group B.

The size of each group (A and B).

The number of words per item.

The location of the first word of the first item to be put away in group C.

The size of group C.

The mode of operation (internal or external).

The number of words containing the sort-key (one or two words).

The relative location within the item of the word (or words), containing the control key, and the location within these words of the characters comprising the control key.

A set of three alternate addresses, one of which may be selected to specify the location of the next instruction depending upon the status of the data at command termination.

When the command is executed in the internal mode, both group A and B are fully merged and stored as group C before the command is terminated. No branch occurs in this mode. When the command is executed in the external mode, the command will terminate when any of the following occur: group A is exhausted, group B is exhausted, or group C is filled. A different branch address is chosen in each case, which permits the introduction of new data from magnetic tape in the first two alternatives or the storage of group C on magnetic tape in the third alternative. After the appropriate tape operation has been carried out, subsequent execution of the same merge instruction will automatically pick up the process at the same point (in the non-exhausted groups) where it was interrupted.

24. Sift: this command assumes the existence of a sorted group of multiple-word items stored in consecutive memory cells. The command compares specified control characters of each successive item with those of a "standard" item. The number of items whose control key is less than or equal to the control key of the standard are tallied and stored. When the first item is found whose control key is greater than that of the standard, or when a specified terminal address is reached, the sift command terminates and the processor proceeds to the next normal command. This instruc-

tion is specified by three words of control information containing:

The location of the first word of the first item to be sifted.

The location of the first word of the standard item: this standard may itself be a member of the group to be sifted.

The number of words in each item.

The location of the control words within each item and the location of the control characters within each control word.

The location of the put away for the sift tally.

The total number of items to be sifted.

This command may be used in two distinct applications. As a table look-up command, the tally provides the location of a desired table entry. During report preparations, this command, in conjunction with the summarize command (see operation 25) permits the rapid accumulation of control totals.

25. Summarize: this command accumulates algebraically the contents of specified fields contained in successive multiple-word items stored in memory. This command is specified by three words of control information.

The location of the summarization field in the first item.

The number of words per item.

The storage location of the accumulated total.

The location of the number of items to be summarized.

The tally which is generated by the sift command (as explained in operation 24) may be directly referenced in that portion of the summarize instruction which determines the number of items to be summarized. These two commands, used in conjunction, therefore automatically provide a summarization of all those items whose control keys are identical, which is precisely the objective of summary report preparation.

Input-Output Commands

Nine two-word commands enable the NCR 304 Processor to communicate with and control its associated input-output equipment; these commands provide the ability to read and write on magnetic tape, search magnetic tape, read and punch paper tape, read punch cards, and print on the high speed printer.

Reliability Checking

The error checking that has been incorporated into the 304 system is based on the philosophy that checking should be performed whenever errors are probable, and that the thoroughness of the check should be a function of the probability of the occurrence and the relative importance of the error.

The types of checks that exist in the system can be classified into read-write checks, transmission checks, and functional checks. The read-write checks are performed on all input-output information that enters or leaves the system. Transmission checks are performed whenever information is transmitted between components within the system. Functional checks are performed by the individual components to insure the correct execution of their functions.

The errors that are detected by the 304 system are roughly divided into two classes. The first class contains errors that might be corrected by programming. For example, read errors on magnetic tape, where errors are assumed to be caused by foreign particles on the tape, might be corrected by re-reading.

Detection of these errors does not necessarily halt the operation, but allows it to continue until some reference point is reached. Where appropriate, an automatic program branch occurs, and the programmer is given the option in an attempt to correct the error of repeating the operation, of halting the equipment and signalling the operator, or of noting the error and continuing.

The second class of errors is characterized by the fact that they cannot be corrected by programming. An example would be the detection of a broken tape on a tape handler. This type of error requires operator intervention; the operation is accordingly halted in these cases, and no programming option is provided.

Summary

Effective application of a business data-processing system dictates that the system design provide maximum flexibility in programming the solution of a problem. On the other hand, economy of programming effort and of hardware utilization can best be achieved by rigidly structuring the automation of the data handling involved in, and the control of, those processes which are common components of broad classes of problem solutions.

Conventional system designs usually meet only one of the two foregoing requirements. If a system meets the former, it is referred to as a "general-purpose" system, and, if the latter, a "special purpose" system.

Programmers have indicated recognition of these conflicting requirements, and have attacked the portion of the problem concerned with conservation of programming effort by developing a number of techniques. For example, many programmers are presently using various pseudocoding techniques, in conjunction with generator programs, in an attempt to provide a workable scheme for the reduction of general programs to detailed machine codes for conventional general purpose systems. Application of this resultant combination of hardware and pseudo codes achieves a reduction in programming effort, but no economy in hardware utilization is obtained, since the computer time spent in processing control information in the resultant routines is essentially unchanged, and data transfers are often needlessly repeated.

To resolve the conflicting requirements outlined above, the design of the 304 system is based on simultaneously achieving the advantages of both general and special purpose systems. The automation of processes, and of the control of processes, which are common to all business data-processing problems (such as sorting, summarizing, editing, etc.), is a characteristic of the 304 system which gains the advantages of the automaticity inherent in special purpose designs, without any loss in programming flexibility. For a given process and information transfer rate, execution time is reduced because the specific transfers of, and operations on, the data and control information which occur are tailored to the specific needs of the process. Complete programming flexibility is retained not only within the structure of the electronic subroutine commands themselves, but also by the inclusion of a full complement of commands of a general purpose nature.

Discussion

C. B. Poland (General Electric Company): On off-line copy, what happens when a new record must be inserted between two old records?

Mr. Cherin: The copy operation as executed on the 304 is one of proceeding from the present position, so to speak, in the file to a new position and stopping at that point, that is, copying until a specified control configuration has been reached. In all processing, some identification is required for each record and this identification is used to control the copy. Thus, specifically, because the programmer knows that he must insert a new record, and as a result of this he knows what this record's control configuration, address, or account number for

it is, he can specify that the file shall be copied from one tape to another until a record is encountered whose address is greater than the one he wishes to insert. Then the new record is written on the output tape and the copy proceeds.

C. C. Gotlieb (University of Toronto): How do you distinguish which of the three addresses is referenced by *R*?

Mr. Cherin: Each portion of this indexing operation is specified by *S*. That is, *S* acts as a modifier of *R* and the two digits completely determine the actual address modification which is to occur.

E. J. Schubert (Westinghouse): What kind of circuitry (tubes or semiconductors to drive magnetics) is used?

Mr. Cherin: I don't believe I made the point quite clear. The computer, including the memory, is mechanized completely from transistors, diodes, and cores; the cores in particular are driven with transistors.

Mr. Bindloss (Liberty Mutual Insurance): Does the 304 system have a file interrogation unit for determining the status of a particular item in the file on an unscheduled demand basis? If so, what is the search and read-out time? How many tape drivers can the NCR 304 accomodate?

Mr. Cherin: Not as yet. The searching rate in such an operation would be, though, the same as the read or write rate which is 15,000 characters per second. The magnetic tape, as we all know, is not a very good medium to use for random-access interrogations. The system accommodates a maximum of 64 tape drives per system.

R. Douthitt (Sperry-Rand Corporation): Does the sort command still exist in the 304?

Mr. Cherin: It has been renamed and is the merge command which contains the six-words of control information.

L. C. Hobbs (Sperry-Rand Corporation): I have previously heard the card rate of your machine described as 1,000 cards per minute, but you stated 500 cards per minute. Is this an interim unit?

Mr. Cherin: No. I would say that this is a conservative figure.

A Technique for Using Memory Cores as Logical Elements

L. J. ANDREWS

OVER THE YEARS there have been many outstanding papers which can be assembled under the collective title "Component Failure Analysis." Included in this group are the tube-life prediction tables, the derating charts for condensors, the maximum current versus useful life curves for diodes, etc.; and each company that has a customer service organization has in its files records loosely titled "Plug-in Failures, Their Cause and Cure." An examination of the records will show that in the majority of cases the "active" elements are at fault. Active elements are defined here as those elements which amplify a changed state of their inputs. It would seem, then, that the path to reliability is to remove as many active elements as possible from the system; that is, given some specific design problem, to time-share the active elements as much as possible in keeping with the flexibility required of the overall design. But this philosophy is not without its attendant apparent disadvantage. To use a minimum of active elements, a maximum of switching elements is required. To utilize the minimum active elements concept, a switching element approaching the ideal is required.

The ideal switching element should have the following characteristics: 1. there should be a minimum number of passive elements per switch, 2. the switch should not load the logical propositions, 3. the switch should be lossless, 4. the switch should have high discrimination, 5. the switch should be compatible with other system components, 6. the switch should be easily fabricated, and 7. it should have all the miscellaneous properties such as high speed, high output, and small physical size; and should be inexpensive, shock resistant, temperature insensitive, etc.

An available item that to a reasonable degree fulfills the miscellaneous properties is the small ferrite core usually used in memory applications. How these cores can approach the ideal switch and perform other useful functions as a result of a unique system concept is the subject of this paper.

The Inhibit-Wound Core

The inhibit-wound core is a deceptively simple component. In its rudimentary form it consists of a small ferrite core with one or more driving sources, an inhibiting proposition, and a sense winding. Each "winding" consists of a single wire through the core; the clocks and propositions each carry half-select current. Using the mirror symbols for core-winding senses[1,2] it is apparent that the core in Fig. 1 will change state from a *one* to a *zero* and back again as the C_R terminal alternates between positive and negative potential. A *one* is defined here as the up direction when current flowing into a slant bar is seemingly reflected up. A *zero* is thus also defined as current into a slant bar reflected down the core. The polarity of the sense signal need not be specified at this time.

In Fig. 1, then, the clock C_R has the ability to write a *one* when positive, and can read a *one* or *zero* when negative. The previous *one* or *zero* state is detected during read by the presence or absence of a large flux change and corresponding voltage induced in the sense winding. The propositions X_i have the restrictions that they may have current only during the write phases of the clock, their currents may only be of half-select or zero amplitude, and their currents will be only positive, i.e., away from the terminus of Fig. 1, and then only if the proposition is true. The relations between the propositions and the clock phases is best illustrated by referring to Fig. 2. During time T_0, proposition X_i is true, current is then flowing in the wire X_i in the direction previously designated as positive. The proposition X_i' (if it exists for use elsewhere) does not have current during the T_0 write time. Conversely, during T_1 and T_2 the wire designated X_i carries no current while wire X_i' has half-select current during write periods. It is a natural consequence, of course, that the core of Fig 1, wired with proposition X_i and subjected to the wave forms of Fig. 2, will have the states 0, 1, 1, and 0 at the end of timing periods T_0, T_1, T_2, and T_3 respectively. The core then can be said to have taken the complement of the information held in sequence by the proposition X_i within the framework of the system defined. Of more immediate interest is the case where not X_i but X_i' is the proposition present as an inhibitory signal. Here the core will assume information as repre-

L. J. ANDREWS is with the Electronics Division of the National Cash Register Company, Hawthorne, Calif.

The author expresses his appreciation to Walt Edwards and James Hudson, who supplied the initial impetus for this work.

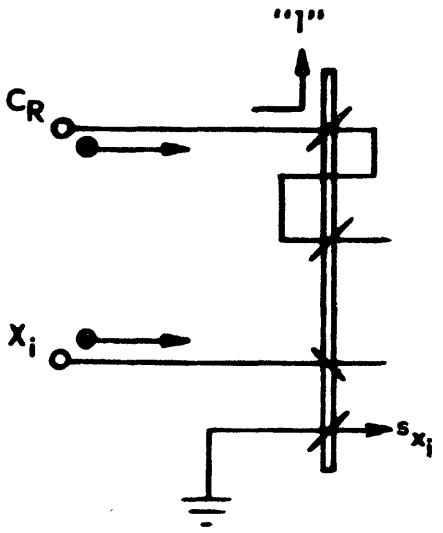


Fig. 1. Basic inhibit-core logical element

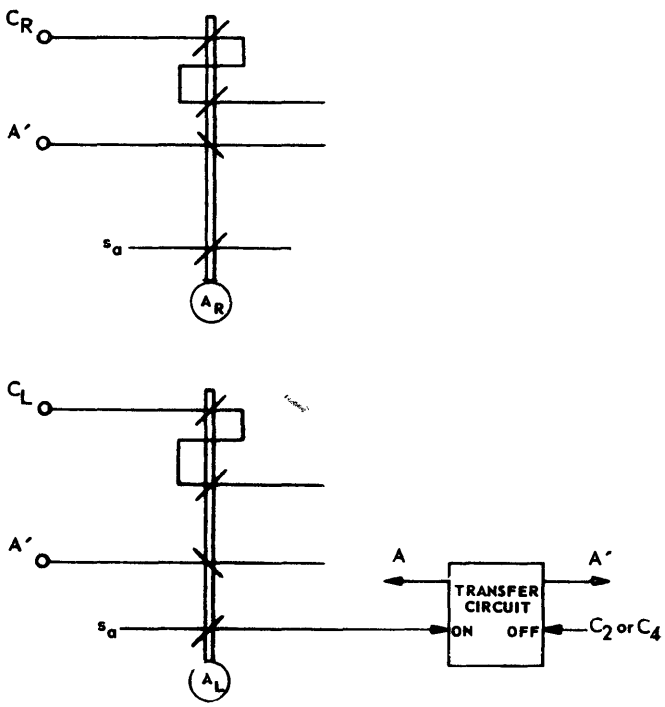


Fig. 3. Inhibit-core logic recirculation

sented by the true term, sequentially 1, 0, 0, 1. A magnetic core with a read-write clocking term, the prime of the proposition to be present in the core as an inhibiting winding, and provision for sensing signal comprise the fundamental unit for Inhibit-Core Logic.

Inhibit-Core Logic

Of prime importance in a computing system is the ability to read information out of storage. If the reading process is destructive, means must be provided to recirculate the just read information in case it is needed at some later time.

Consider the schematic diagram of Fig. 3 in which the two clocks C_R and C_L have the phase relationship illustrated in Fig 4. Note particularly that core A_R is similar to that of Fig. 1 and core A_L is also the same, with the exception that the cycle write-read is introduced in the interval between the read-write of core A_R. All similarly labeled terms are assumed to be in series. The box labeled "transfer circuit" is in essence merely a half-cycle delay amplifier pair, but for this example may be considered to be a d-c flip-flop with the following characteristics. The flip-flop will respond to the voltage on the sense wire corresponding to a changed core only during the read intervals (C_1 or C_3 of Fig. 4). This voltage may only turn the flip-flop on. The flip-flop will always go off at the end of a write interval (C_2 or C_4 of Fig. 4). The outputs A and A' are considered to be gated by the two write intervals. Therefore, a pulse of half-select current is present on either the A or A' during, and only during, each of the write intervals.

A *zero* in core A_R of Fig. 3 at the beginning of time T_1 is subjected to the wave form of Fig. 4. At read interval C_1 clock C_R is negative, current is then flowing in the direction to set the core to the *zero* state. Core A_L is dormant so there is ideally no signal present on the sense

Fig. 2 (below). Time relationships between propositions and clocking phases

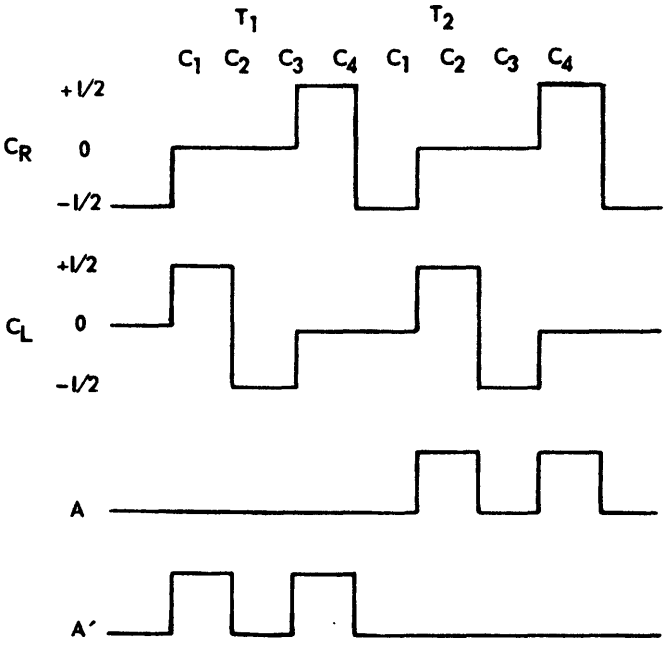
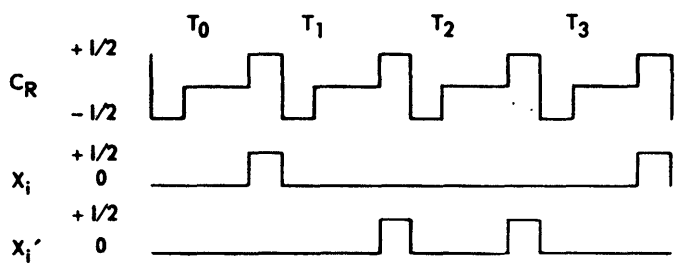


Fig. 4 (right). Phase relationships between register clock, logic clock, and wave forms obtained during recirculation



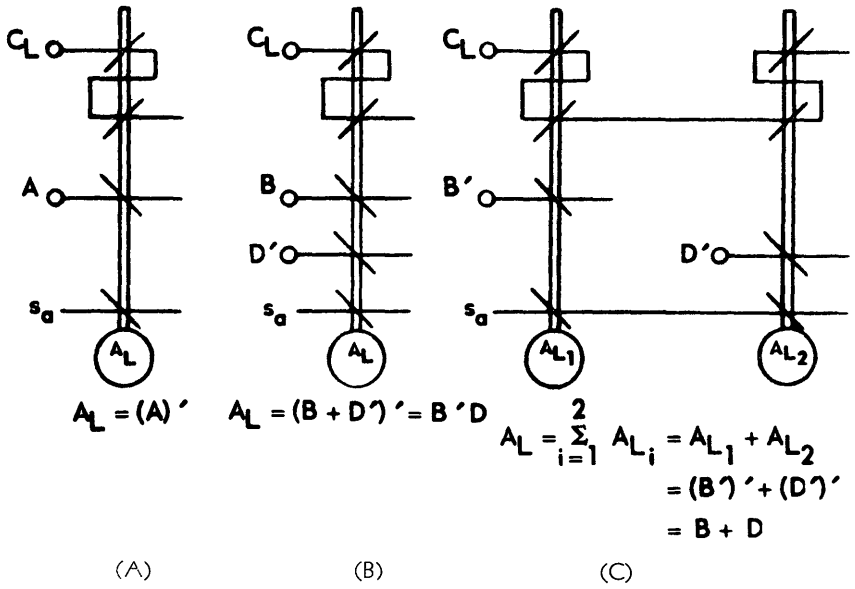


Fig. 5. Logical negation, product and sum

winding. The transfer circuit will then have an output during the write cycle C_2 on output line A'. Core A_L, if it is originally in the *zero* state, would ordinarily be set to the up or *one* state by clock C_L. However, current flowing in line A' inhibits the writing and A_L remains a *zero*. A' has no effect upon core A_R. Clock C_L now reverses sense, but the core, having remained in the *zero* state, has no flux change. A', then, again is true during write phase C_4 and inhibits the writing of a *one* in core A_R. At the end of time T_1 the two cores are in their original states. Conversely if there is a *one* in core A_R at the beginning of time T_2, C_R will now change the *one* to a *zero* during C_1. This change is sensed and the transfer circuit provides current on A during C_2 but no current on A'. Clock C_L is then able to write a *one* in A_L. The *one* is immediately read at C_3, the transfer circuit again has no output on A' at C_4 and the *one* is rewritten in core A_R. Again the original conditions are obtained. The significant point is that the inhibit-wound core A_L was used to control the inhibit-wound core A_R during recirculation of that core. All this is accomplished with a single time-shared transfer circuit. This basic philosophy which will be shown to be simple, inexpensive, and extremely versatile should be carried in mind throughout.

In the following, A_R will be the controlled core and will be wired as shown in Fig. 3. The wiring of the control cores will then establish a selected function in A_R. The previous example of recirculation shows that a signal on the sense winding during C_3 will allow C_R to write a *one* in A_R at C_4.

Negation can be accomplished by the circuit of Fig. 5(A). A *one* read from A_R will inhibit this logic (controlling) core during C_2. There is no output at C_3; A' is then true at C_4 and inhibits the writing of a *one* back in A_R leaving A_R a *zero*. A *zero* read during C_1 will not cause an inhibition in the logic core. The logic core therefore has an output at C_3 and C_R writes a *one*. *One's* and *zero's* are then interchanged in this operation.

Logical AND can be accomplished in a single core as shown in Fig. 5(B). The logical equations pertaining to these circuits will be discussed later but the physical argument is as follows: It is known that if a *one* is allowed to be written in the logic core a *one* will then be written in the controlled core. It is desired that the result of the logical product $B'D$ be in A_R; in Fig. 5(B) if proposition B is true it is not this case, so let B inhibit A_L. If D' is true it is not this case, so let D' also inhibit A_L. Thus the only time A_L is not inhibited is when the proposition $B'D$ is true. $B'D$ then appears in A_R.

Logical OR requires an inhibit-wound core for each proposition of the sum. The summing actually takes place on a common sense winding. Again reasoning physically in Fig. 5(C): the logical sum $B+D$ is wanted in the controlled core; core A_{L_1} will have a *one* if B is true (if not inhibited by B'), core A_{L_2} will have a *one* if D is true. If either or both of these cores has an output during C_3 the transfer circuit will respond. The sum $B+D$ will then appear in A_R.

These three basic functions are of interest, but the equations of a respectable computing system are almost never composed of single logical terms of a few elements. To point out the versatility of inhibit-core logic the basic circuits must be re-examined in the light of their logical equations.

In the circuit of Fig. 1 it may be verified, from a truth table, for instance, that the equation Core$=(X_i)'$ represents the state of the core at the end of its clock cycle. The proposition X_i may be any combination of AND's and OR's. If, as it is used, the proposition X_i is the inhibiting term the equation becomes Core$=(X_i')'=X_i$. Now if it is agreed for the present that the inhibiting term for the controlled core shall always be the prime output of the transfer circuit whose input

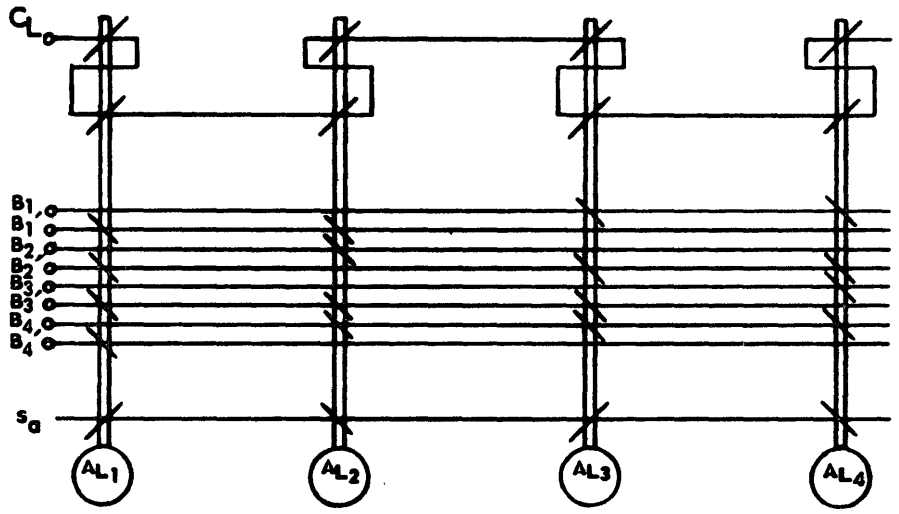


Fig. 6. A more general example of the mechanization of a Boolean function

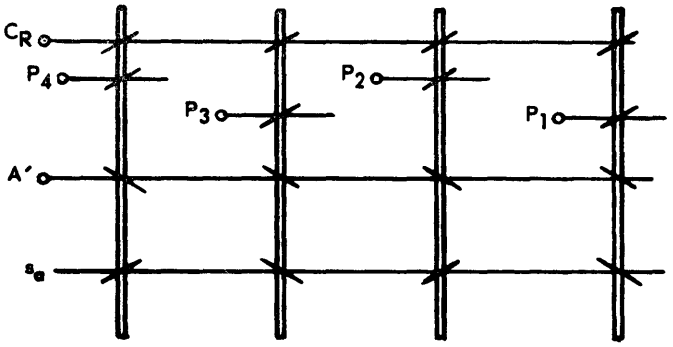


Fig. 7. Four-bit serial register

is the sense winding of the controlled core, the controlled core such as A_R of Fig. 3 will have the equation $A_R=(A')'=A$. It has been demonstrated that if the sense winding for the transfer circuit A_R has a voltage representative of a large change in flux in any of the A_L control cores during the C_3 read time, A_R will be true. The equation for A_R can then be written $A_R=A_L=A_{L1}+A_{L2}+A_{L3}+\ \ldots\ +A_{Ln}$, where the plus sign indicates the logical sum. The A_{Li} terms are each inhibit-wound cores and so have the expression $A_{Li}=(Y')'$ where Y again is some arbitrary desired Boolean function. Since a magnetic core can be inhibited by one or a number of inhibiting terms, all having essentially equivalent effect, the controlling core provides a logical sum of its input windings. Thus the equation $Y'=y_1'+y_2'+y_3'+\ \ldots\ +y_j'+\ \ldots\ +y_n'$ can be written, where the y_j' are the single term propositions each threading a A_{Li} control core. The logical equation can be expressed as follows:

$$A_R=A_L=\sum_{i=1}^{n}A_{Li}=A_{L1}+A_{L2}+\ \ldots\ +A_{Ln}$$
$$=(Y_1')'+(Y_2')'\ \ldots\ (Y_n')'$$
$$=(y_{11}'+y_{12}'_r+\ \ldots\ y_{1r}')'+(y_{21}'+y_{22}'+\ldots y_{2s}')'+\ldots(y_{n1}'+y_{n2}'+\ldots y_{nt}')'$$

Thus

$$A_R=(y_{11}y_{12}y_{12}\ \ldots\ y_{1r})+(y_{21}y_{22}y_{23}\ \ldots\ y_{2s})+\ \ldots\ (y_{n1}y_{n2}y_{n3}\ \ldots\ y_{nt})$$

where the meaning of the subscripts is obvious.

The logical function to appear in the controlled core becomes the result of the individual inhibiting terms threaded through the controlling cores. It should be noted that this expression is the general case of a Boolean function expressed as a sum of products. There exists[3] a rigorous mathematical proof for the identity, (see last step of foregoing logical equation), but the derivation in this manner has additional merit. Working backwards gives a prescription for mechanizing any Boolean function. Perhaps an example here will be of value.

Suppose a function is to be mechanized in A_R:

$$A_R=B_1B_2B_3B_4+B_1B_2'B_3B_4'+B_1'B_2B_3B_4'+B_1'B_2B_3'B_4'$$

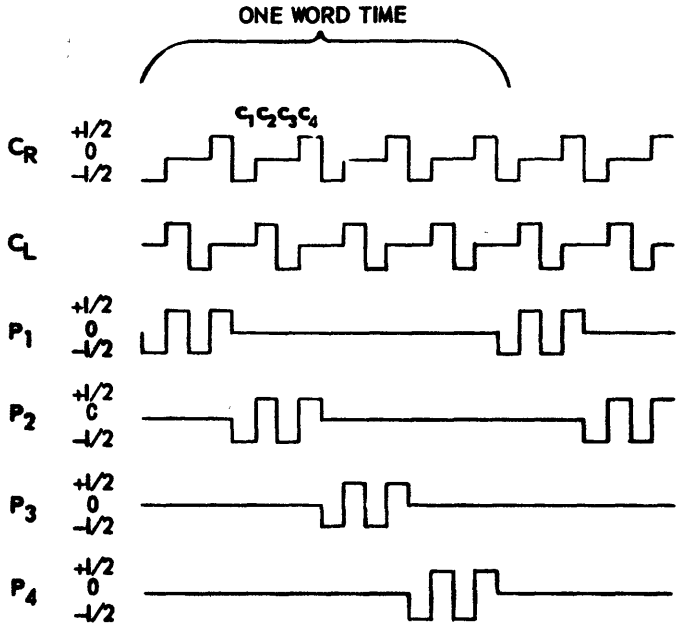
Going back one step in the derivation, A_R can be written:

$$A_R=(B_1'+B_2'+B_3'+B_4')'+(B_1'+B_2+B_3'+B_4)'+(B_1+B_2'+B_3'+B_4)'+(B_1+B_2'+B_3+B_4)'$$

The control can be immediately wired; the bracketed sums are formed in the control cores, the external sums are formed by the common sense winding. The wired control cores for this expression are shown in Fig. 6. The A_R core wiring remains the same and of course the transfer circuit remains unchanged.

The Inhibit-Core Register

The inhibit-wound cores can be arranged as a serial register. The cores of the register have a common register clock, C_R; a common inhibiting term, A'; and a common sense-winding leading to a single transfer circuit. If now these cores are to perform as part of a serial register they must be scanned sequentially by some noninterfering wave form. Further, in a practical register provision must be made for treating the digits in the register both individually or collectively. For instance, if a register is merely read, the digits are each treated alike, but if an arithmetic process is being carred out on the information the logic for the sign digit must be different than for the rest. The schematic of a 4-bit serial register is illustrated in Fig. 7, and wave forms which allow performance as required are shown in Fig. 8. It requires a coincidence between one of the clocks and a P timing signal each of half-select amplitude to have sufficient drive to switch a core. These coincidences have special significance; the $P-C_R$ coincidence during C_1 is



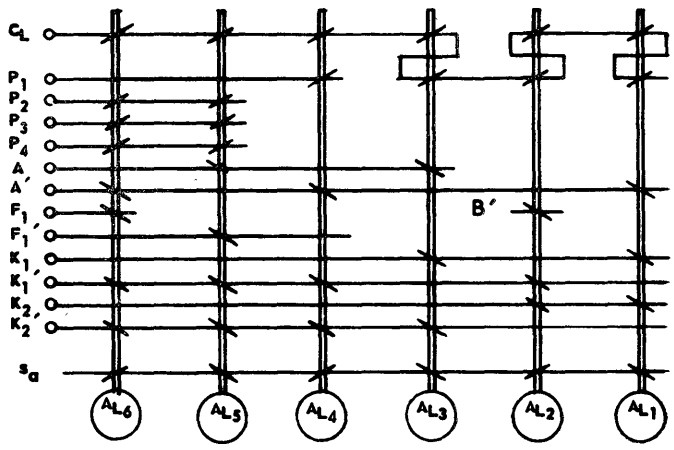


Fig. 8 (left). Wave forms for four-bit serial register

Fig. 9 (above). Control logic for four-bit register

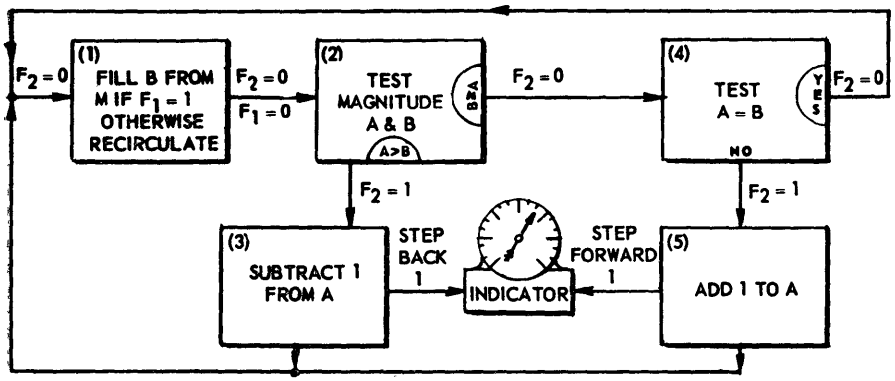


Fig. 10. Block schematic for positioning device

called "read register," the $P-C_L$ coincidence at C_2 is called "write logic," the $P-C_L$ coincidence at C_3 is called "read logic," and the last coincidence of $P-C_R$ is labeled "write register." At each P-time, then, the operation sequence is as follows: 1. read the information contained in the core of the register corresponding to the active P term and put the result in the transfer circuit; 2. using the information contained in this and any other transfer circuits, store the result of the prewired logical function to be performed on the register digit at this time in a logic core; 3. read the results of this logical manipulation into the original transfer circuit; 4. inhibit or not the writing of a *one* into the selected digit of the register. Fig. 9 shows the total number of cores and the wiring schematic to perform the logic required for recirculation, transferring, complementing, and counting in the 4-bit register. These operations should be taken as representative rather than exhaustive. The two propositions K_1 and K_2 define which of the four operations is to be done and correspond to program control. When $K_2'K_1'$ is true the programming inhibits are released from core A_{L_1} and the A' inhibit term then controls recirculation of the register at all P-times just as in Fig. 3. If $K_2'K_1$ is true it should be apparent that if B' is the output of another similar register, its formation will be transferred digit by digit to the A register by means of core A_{L_2}. Core A_{L_3} provides complementation of the information in register A including the sign position (assumed to be in the LSD digit, P_1). Of special interest are the three cores A_{L_4}, A_{L_5}, and A_{L_6}. If proposition F_1 is considered to be the output of some carry flip-flop, after the sign digit is recirculated unchanged by core A_{L_4}, cores A_{L_5} and A_{L_6} provide the addition of one (under command of K_2K_1) to the number held in the three other digits. The register will now count. It is to be noted that no additional logical cores are required to perform these same operations on a register of any length; these four operations, and in fact any number of logical manipulations, are possible on a register of any length with the one transfer circuit required of this simple case.

Flip-Flops

Flip-flops, such as the F_1 term referred to in the previous section, are a special case of the inhibit-core register concept. The register consists of only one core. Since the output of a flip-flop usually must be available at each P-time the single core is supplied with the continuous clock C_R and therefore is wired like the A_R core in Fig. 3. The logic (controlling propositions or grid equations) are then mechanized in a fashion similar to that for the actual registers. It is significant that no matter how complex the switching may have to be in order to time-share a particular flip-flop, only a single transfer circuit is required.

An Illustrative System

An example to demonstrate the technique is a position device. It could be used to set a pointer, shaft position, or graph plotter corresponding to some binary number. Only the pertinent detail necessary to illustrate the technique will be given.

A block schematic for the positioning device is shown in Fig. 10. The loop is considered to be continuously running initially with the pointer at zero, and the registers cleared. New information is taken from a memory register M into a storage register B. The third register A keeps account of the current position of the pointer. When the number in A reaches the number held in B the pointer will have been supplied with a sufficient number of pulses to indicate the number in B. New information can be inserted any time the cycle passes through block 1 becoming the new or present desired setting. Fig. 10 is the block schematic for the example. Figs. 11, 12, 13, and 14 show the core wiring for the complete switching operations for the A register,

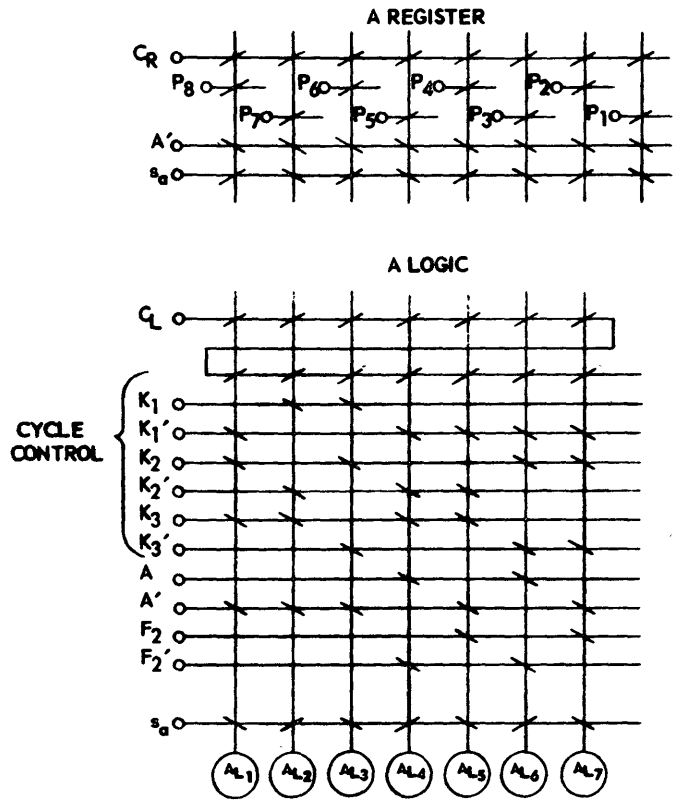
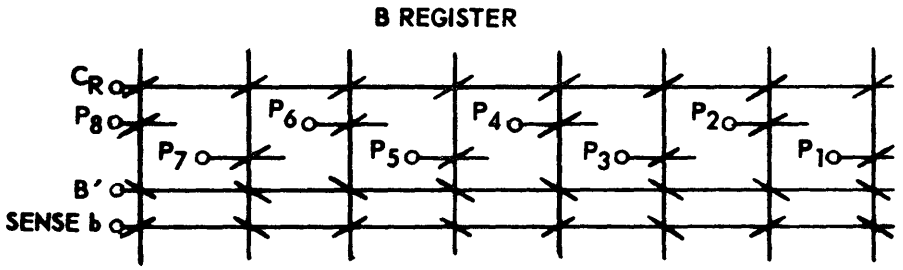


Fig. 11. The A register schematic



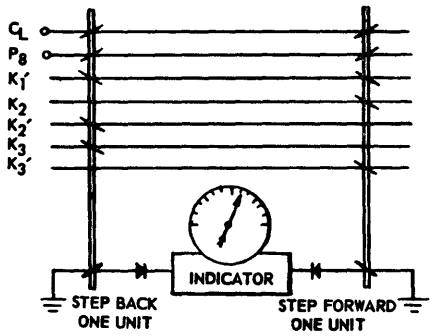


Fig. 14. Output schematic

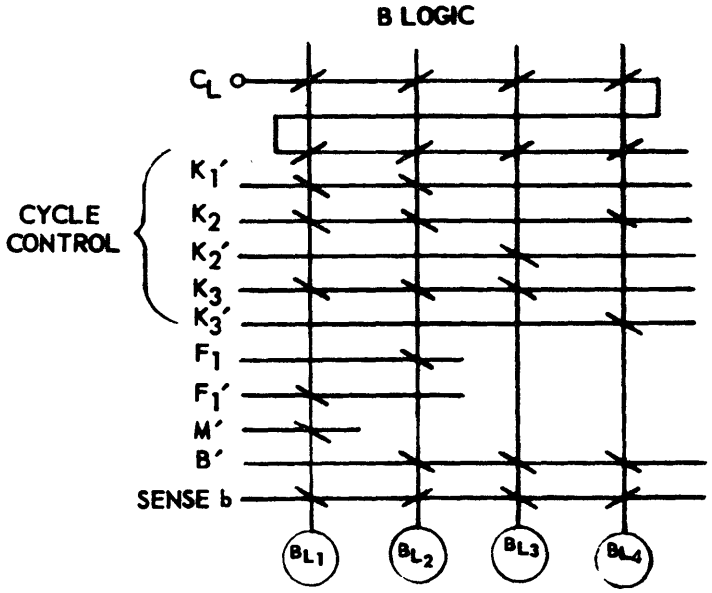


Fig. 12 (above). The B register schematic

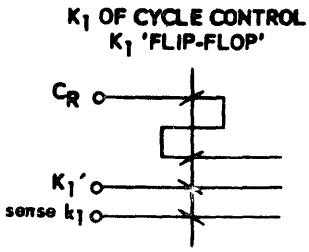
Fig. 13 (below left). The F_2 flip-flop

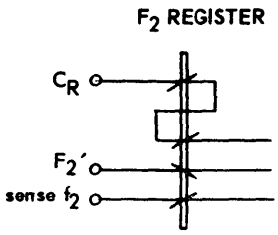
Fig. 15 (below right). Typical cycle control

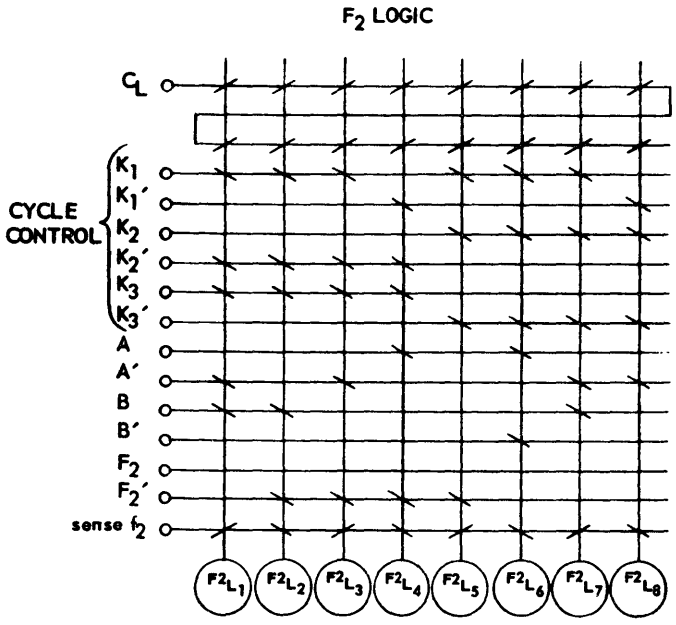
B register, F_2 flip-flop, and output circuit respectively. The operation cycle is controlled by the three flip-flops K_1, K_2, K_3, and will be discussed later.

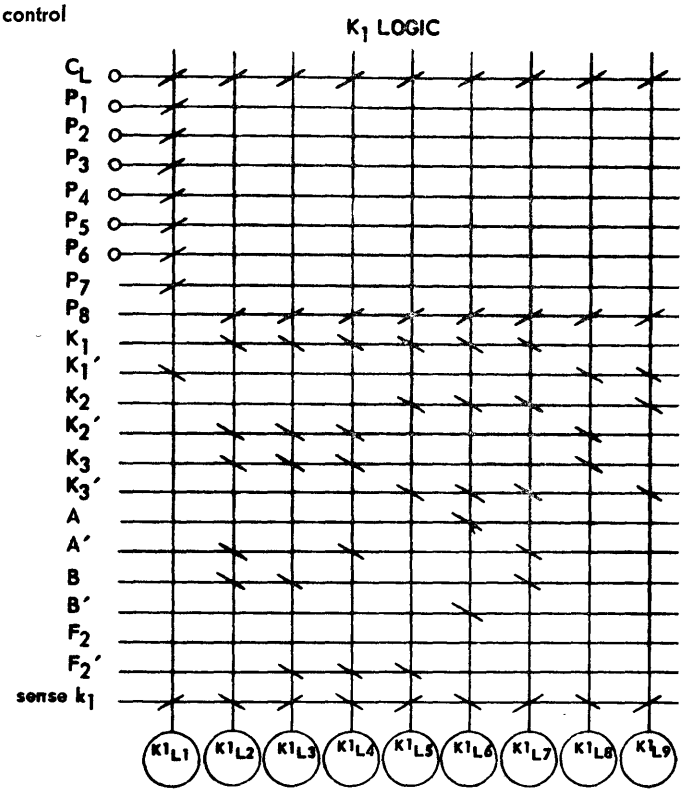
In the A logic, cores A_{L1}, A_{L2}, and A_{L3} provide recirculation in blocks 1, 2, and 4 respectively; cores A_{L4} and A_{L5} contain the logic for the subtraction of one in block 3; cores A_{L6} and A_{L7} contain the logic for the addition of one in block 5.

In the B register, core B_{L1} inserts information from the M register if flip-flop









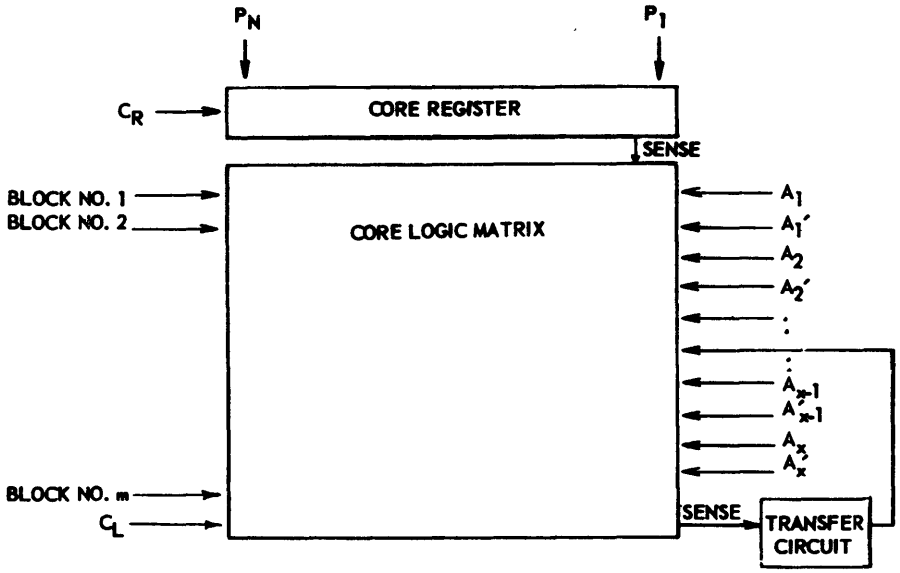


Fig. 15. Format of register

F_1 is true, core B_{L_2} recirculates the old information if F_1 is false, and cores B_{L_3} and B_{L_4} recirculate the B register during blocks 2, 3, 4 and 5. It is perfectly permissible to simplify logically the expression for the control before specifying the wiring of the cores.

The time-sharing aspect of the over-all concept is not very well brought out in examining the registers. More insight is obtained from the flip-flop logic. In Fig. 13 cores $F2_{L_1}$, $F2_{L_2}$, and $F2_{L_3}$ provide the logic required for F_2 to contain the results of the test magnitude specified in block 2; core $F2_{L_4}$ makes F_2 provide the borrow operation in block 3; cores $F2_{L_5}$, $F2_{L_6}$ and $F2_{L_7}$ provide the logic required for F_2 to contain the result of the Test Equality in block 4; finally, core $F2_{L_8}$ provides the carry for the addition operation of block 5. There is no control core corresponding to block 1. This implies that F_2 will be automatically set to zero as it should be.

The output circuit of Fig. 14 is self-explanatory. If the loop containing block 3 is traversed a positive pulse is delivered to the indicator to step back; if the loop contains block 5 a pulse to step forward is entered.

Of special interest is the cycle control since it directs the sequence of events based upon decisions obtained during the course of operation. An example is the LSD digit of the block counter $K1$ the logic for which is illustrated in Fig. 15. The cycle control must supply an inhibit-or-not pulse at C_2 for each of the eight bits of the P-times. These are automatically provided by arranging the cycle counter flip-flops to recirculate the information supplied them at the previous word time during the next word time. In Fig. 15 this function is provided by core $K1_{L_1}$. The absence of a controlling core during P_8 of block 1 will set zero to be recirculated in block 2. In block 2 a loop split is made based in a test magnitude operation. The result of the test will appear in flip-flop F_2, and in particular the result will be written in F_2 at P_8 time. If this decision is presented and written in K_1 at the same time, K_1 will provide the correct path during the next word time. Cores $K1_{L_2}$, $K1_{L_3}$, and $K1_{L_4}$, are wired to make this decision P_8 time. In the same manner the decision in block 4 is made by cores $K1_{L_5}$, $K1_{L_6}$, and $K1_{L_7}$. Cores $K1_{L_8}$ and $K1_{L_9}$ could have been wired as a recirculation since K_1 will not change going from either block 3 or 5 back to block 1, instead they are wired to set *one* unconditionally (a lack of inhibiting terms on the logic core automatically allows setting of the register core to *one*). The wiring for the other two flip-flops, K_2 and K_3, follows a similar pattern.

The storage, logical operations, output gating, and operational cycling have been done with a total of 6 required transfer circuits and about 70 small ferrite memory cores in addition to the clock and P sources. Of course in a larger system the ratio of cores to active elements is a great deal higher.

A Small Complete Machine

Looking back through Figs. 11, 12, 13, and 15 it can be seen that the wiring has a particular format, namely, that of Fig. 16. For each register there is associated a group of logic cores and a transfer circuit. These three items form a structure complete in itself which is operationally as reliable as the one transistor that may be required in the transfer circuit and as versatile as the designer may demand.

To establish the feasibility of this concept a small computer was constructed It has a fixed program; an 8-bit word; and an 8-word memory, four words of which are available for storing selectable three-address commands. Information is inserted manually into the memory. The operations the machine will perform are addition, subtraction, test magnitude and multiplication. There are 22 block numbers. In operation the operator selects the control number and the machine will carry out the command named by that number. The registers, logic, and memory entail 193 size F-394 S-3 ferrite cores and eight transfer circuits complete. The design technique was essentially that described in this paper with the exception of the cycle control scheme; an 8-beat controllable shift register is used. The machine, since it uses S-3 ferrite cores and is serial in operation, has a bit operation time of 20 microseconds. Fig. 17 shows the machine; of course no attempt has been made to reduce the size.

Because of the small sample of the parts concerned, statistical data on operation would be of little value. However, the machine has been running continuously for some time and has yet to suffer an operational malfunction.

Conclusion

A computer design philosophy based on an inhibit-wound magnetic-core concept has been discussed. The major advantages are the following: 1. a minimum number of active elements are used for computation and control, 2. since all logical terms are inhibits they are never required to furnish power to their load, 3. all switching is done magnetically but never with a core driving core unit, 4. these elements are completely compatible with themselves and other system units, 5. since the propositions are entered in the logic core as single wires the number of terms of a product that can be formed in a core is limited only by the number of wires that the hole will accommodate, and 6. the system of logic inherently allows low power consumption. In fact, these advantages are very similar to the desired characteristics of the ideal switch discussed in the introduction.

The major disadvantages are the following: 1. the rather intricate wiring that is required is not conducive to automatic wiring techniques, 2. the 4-cycle clock and the inherent switching time of a ferrite core when changed with two half-

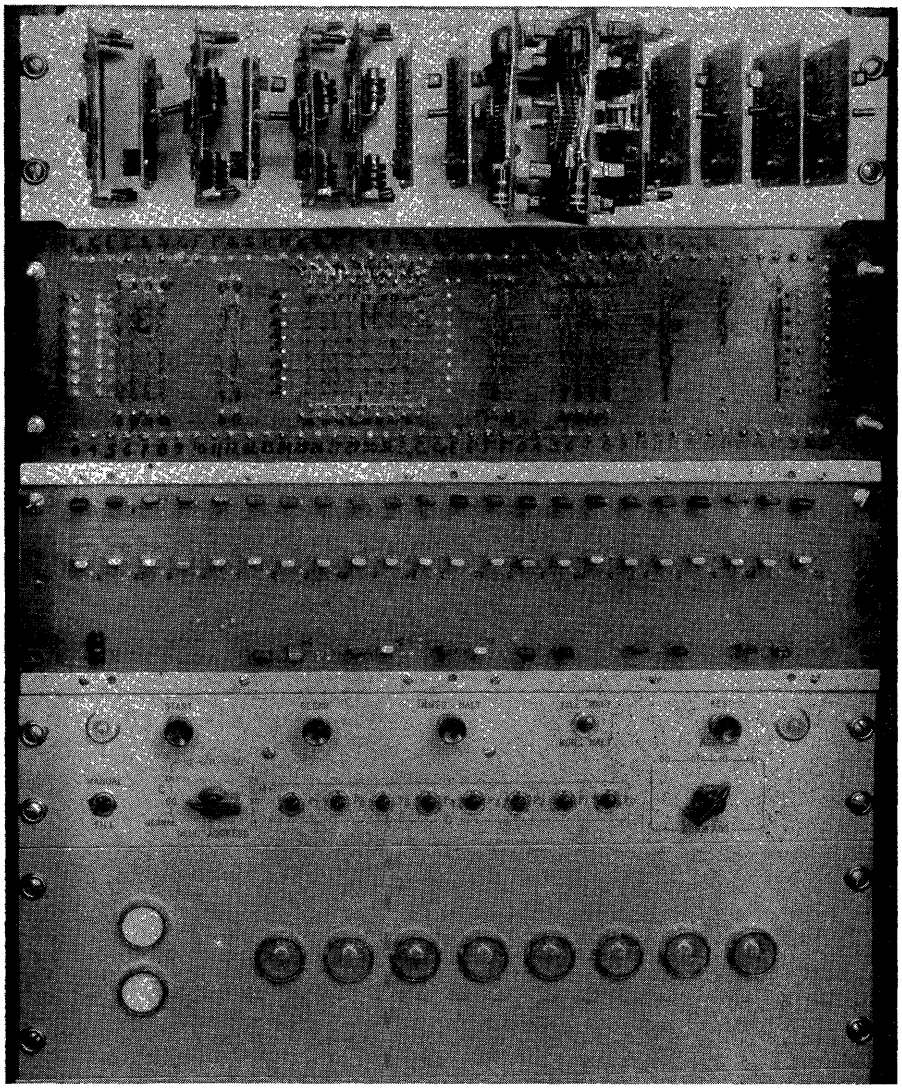


Fig. 17. Small core computer

select coincident currents make the basic operations in a serial machine relatively slow, and 3. the ferrites are supposedly temperature-sensitive although no trouble has been experienced and this aspect has not yet been investigated.

Thus far only the surface has been scratched in considering a few examples in relation to the serial system. The powerful tools represented by the design concepts presented in this paper are versatile and simple, and they require a minimum of parts. It is felt that this system can be profitably utilized in the design of a great many data processors and is indeed a major step toward increased reliability.

References

1. Pulse-Switching Circuits Using Magnetic Cores, **M. Karnough.** *Proceedings*, Institute of Radio Engineers, New York, N. Y., vol. 43, no. V, Aug. 1952, pp. 570–84.

2. A Proposed Symbol for Magnetic Circuits, **R. P. Mayer.** *Engineering Note E-472*, Digital Computer Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.,

3. Inverted-Core Logic and the Synthesis of Boolean Functions Therefrom, **David Ellis, Lad Andrews.** *Research Report*, NCR-ED Bulletin no. 111, National Cash Register Company, Hawthorne, Calif., Oct. 1956.

Discussion

Y. J. Lubkin (W. L. Maxson Company): What are the current tolerances and levels for your signals, and how do you maintain tolerances?

Mr. Andrews: Because we are using S-3 cores, and a half-select system in this machine, 180 milliamperes of driving current at roughly 5-per-cent regulation is required over a temperature range of 50 to 100 degress Fahrenheit. Transistors driven to saturation and a fixed limiting register suffice.

K. Prestor, Jr. (Bell Telephone Laboratories): What type of circuitry is used to provide pulses to such core circuits?

Mr. Andrews: These cores require only 180 milliamperes of inhibition current, and this then becomes our half-select current. The transistor is well able to supply it. It should be kept in mind that since all signal propositions are inhibiting terms they are never called upon to overcome the large back voltage generated by a switching core.

F. Raasch (General Mills, Inc.): In the case of ferrite cores, how is the necessary gain obtained between stages of the serial shift register?

Mr. Andrews: In the serial shift register the gain is again provided by transistors. There is a transistor in between each stage in this particular model. The program control technique described in the foregoing is considered to be superior to that of a shifting register.

A Magnetically Controlled Gating Element

D. A. BUCK

Synopsis: A computer component based on the magnetic destruction of superconductivity has been proposed,[1] and an information-handling system involving a large number of such elements is described in a companion paper.[2] In this paper attention is directed toward the electrical characteristics of superconductive components. Also recently measured switching-time characteristics, switching from an energy standpoint, and a comparison of switching in superconductors with switching in magnetic and ferroelectric materials are discussed. A brief description of the component is first given.

THE electrical resistance of metals drops as the temperature is lowered, and gradually levelling off to a constant value as absolute zero is approached. Twenty-three elements exhibit the remarkable property whereby every vestige of resistance suddenly disappears at some temperature above absolute zero, the element then becomes a superconductor, capable of supporting a circulating electric current indefinitely. A magnetic field, however, will cause the normal resistance to reappear. Fig. 1 is a plot of the magnetic field intensity required to destroy superconductivity at any temperature for nine common superconductors.

A magnetically controlled gating element based on this nonlinearity consists of a wire or evaporated film of superconductive material placed in the magnetic field of a second wire or film. For example, over a 1-inch length of tantalum wire a single-layer control winding of insulated niobium wire can be wound. Current in the control winding produces a magnetic field which causes the central wire to switch from its superconducting to its normal state. Operation of the device is therefore up and down on a vertical (constant-temperature) line in Fig 1. The central conductor can carry more current in its superconducting state than is required to switch an identical device into the normal state. Therefore, the device, named the "cryotron" after the Greek *kryos* meaning cold, has current gain. The maximum current that can be carried by a superconducting wire is limited by the magnetic field of that current. When the self-field reaches the intensity given by Fig. 1, the wire switches to its normal state. When both a self-field and a control field are present, as is commonly the case, the two fields add in space quadrature, and when the vector resultant field reaches the critical value for that operating temperature, switching occurs. The volt-ampere characteristics of a cryotron can therefore be plotted in three dimensions with the control field as the third dimension (Fig. 2). The resulting transition points lie on the intersection of a plane and a right ellipsoidal cylinder. Note the interesting symmetries offered by such a component.

It is interesting to compare electronic components with one another with respect to what circuit relationship is being controlled, and whether an electric or a magnetic field is effecting the control, and thus place the cryotron in its relative position (Table I). To the extent that lumped-parameter equivalent-circuit elements are valid, one can divide the controlled-circuit elements into three groups R, L, and C. More properly, since rectangular-hysteresis-loop magnetic cores and ferroelectric condensers are more nearly dissipative elements than storage elements, one can divide components into three groups according to the circuit-variable relationships being controlled as follows: V versus i, $\int v dt$ versus i, and $\int i dt$ versus v. The cryotron falls in the column of components where the v versus i characteristics are controlled, and in the row of components where control is effected by a magnetic field. In this respect, cryotrons are similar to electromechanical relays. Table I, while it gives a picture of where the cryotron fits into the component picture, is by no means exhaustive. Hall effect devices, for example, fall into both boxes of the first column. Note the two empty boxes.

Switching Time

Measurements made by Pippard and Faber[3] of the time required for tin rods to switch between superconducting and normal states indicate a hyperbolic relationship between switching time and magnetic-field intensity above the critical field. Inverting one coordinate, the time, transforms the hyperbola into a straight line whose intercept is the critical magnetic-field intensity corresponding to the operating temperature, and whose slope is a function of the delay mechanisms involved.

Reciprocal switching-time measurements on tantalum wires at 4.2 degrees Kelvin also exhibit a straight-line dependence on magnetic-field intensity. In this experiment, a steady gate-current flows through the superconductive wire. A step longitudinal magnetic field is applied to the wire by applying a current step to a single-layer insulated niobium control winding wound over the wire under test, and the voltage across the gate circuit is displayed on an oscilloscope. The transition is defined as complete when the voltage reaches 90 per cent of its steady state value.

A delay is observed between the time of application of the step magnetic field and the first appearance of voltage across the superconductor. During this interval the net external magnetic field is sweeping through the superconductor from outside, toward the center, leaving behind a normal region. Eddy currents which flow circumferentially around the wire in the normal region limit the rate at which the boundary regions can move. When the normal region has swept to the wire center in at least one spot, resistance appears which then increases to the normal value.

During this interval, between the application of the step longitudinal magnetic field and the first appearance of resistance, the gate current contributes to the external magnetic field and thus influences the length of this interval. The net external field causing switching is

$$|H|_{net} = \sqrt{H_o^2 + \left(\frac{I_g}{\pi d}\right)^2}$$

where d is the wire diameter, H_o is the applied longitudinal magnetic field intensity, and I_g is the gate current. H_o is given quite closely by $H_o = NI_c/L$ where N/L is the pitch at the control winding in turns per meter and I_c is control current. The angle made by the net field with the centerline of the wire is given by

$$\tan \alpha = \frac{I_g}{\pi d H_o} = \frac{L}{\pi d N} \cdot \frac{I_g}{I_c}$$

The flow lines of magnetic field intensity are helices about the wire, but until now no particular significance has been attached to the direction of the net field for

D. A. Buck is with the Massachusetts Institute of Technology, Cambridge, Mass.

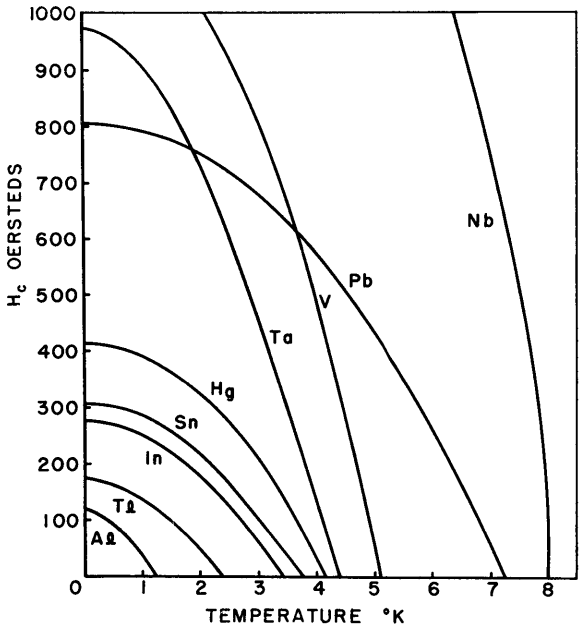


Fig 1 (left). Threshold magnetic field versus temperature for several common superconductors

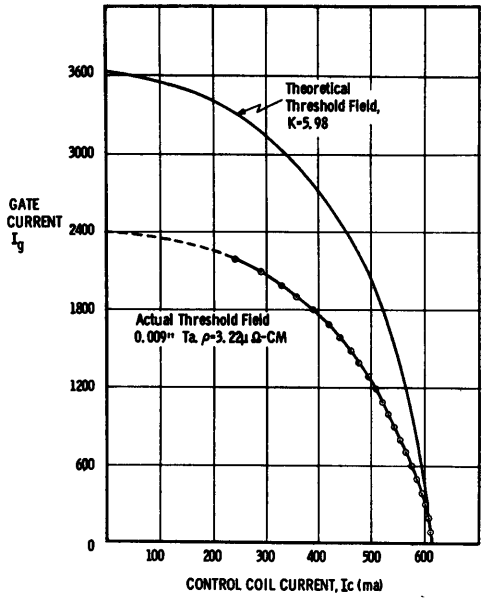


Fig. 3 (right). Variation of threshold field as a function of orientation of applied field

this geometry. However, the problem of switching in the presence of a measuring current is by no means a solved problem. The locus of threshold points for the destruction of superconductivity in the I_g versus I_c plane fall on an ellipse of smaller major- to minor-axis ratio than would be predicted from the expression for H given above. When the switching process is better understood, the orientation angle α may become significant in explaining the discrepancy. Turk[4] has, in fact, postulated that the critical magnetic field required to destroy superconductivity is a function of α. For a piece of 0.009-inch tantalum wire, measured threshold points lie on an ellipse of $K=4$ instead of $K=6$ (Fig. 3), where K is the theoretical major- to minor-axis ratio, then

$$K=\frac{\pi dN}{L}$$

The interval between the first appearance of resistance and the completion of the transient is characterized by the wire having both superconducting and normal regions, with eddy currents flowing in the normal regions, and an electric field existing in the normal regions equal in magnitude to the current density divided by the normal volume resistivity at that temperature. Both magnetic and electric forces act on the boundaries. Possible domain structures have been suggested by London, Schoenberg, and others.[4,5] As the normal regions grow at the expense of the superconducting regions, the normal resistance returns.

Fig. 4 is a plot of the reciprocal (inverse) switching time versus control current for 0.005-inch, 0.010-inch, and 0.015-inch tantalum wire, and a sample of 0.015-inch 92 per cent indium plus 8 per cent bismuth alloy wire, showing the variability in the switching characteristics as resistivity, wire size, and gate current are changed. With the exception of the vacuum-fired tantalum sample, the curves show a straight line relationship between reciprocal switching time and magnetic-field intensity for short switching times, and a departure from linearity, presumably due to Joule heating, for long switching-times. The curvature in the case of vacuum-fired tantalum has not yet been explained. An increase in the gate current can be seen to shorten the switching time for a given control current. All measurements were made near a temperature of 4.21 degrees Kelvin The control coil pitch is 8,600 turns per meter.

The upper end of Fig. 4 cuts off at 10 microseconds because of limitations in the apparatus. In one measurement made on an evaporated film cryotron, destruction of superconductivity by gate current was observed in 0.1 microsecond.

Very little has been said about switching from the normal to superconducting state upon removal of the magnetic field. Even in the presence of a gate current, switching in this direction occurs rapidly. For the experiments whose data is presented in Fig. 4, the superconductive state is reestablished in about 1 microsecond. As soon as a single path capable of carrying the gate current becomes superconductive, the gate voltage be comes zero. Further changes may be taking place but these have not been studied.

Switching Energy

In the absence of gate current, one can compute the energy involved in switching a superconductive wire from one state to the other by means of a longitudinal magnetic field. The inductance of the control

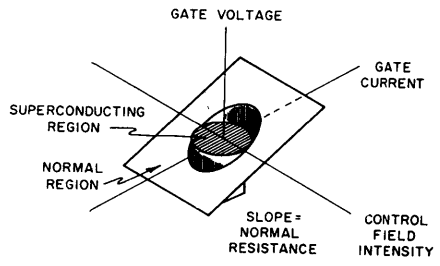


Fig. 2. Static cryotron characteristics

Table I. Relationship Between Cryotron and Other Components

	Circuit Relationships Being Controlled		
	R Voltage versus current	L Volt-time integral versus current	C Current-time integral versus voltage
Controlled by electric field	Vacuum-tube, Transistor		Ferroelectric condenser
Controlled by magnetic field	Magnetoresistive, devices, cryotron, electromechanical relay	Magnetic-core, magnetic amplifier	

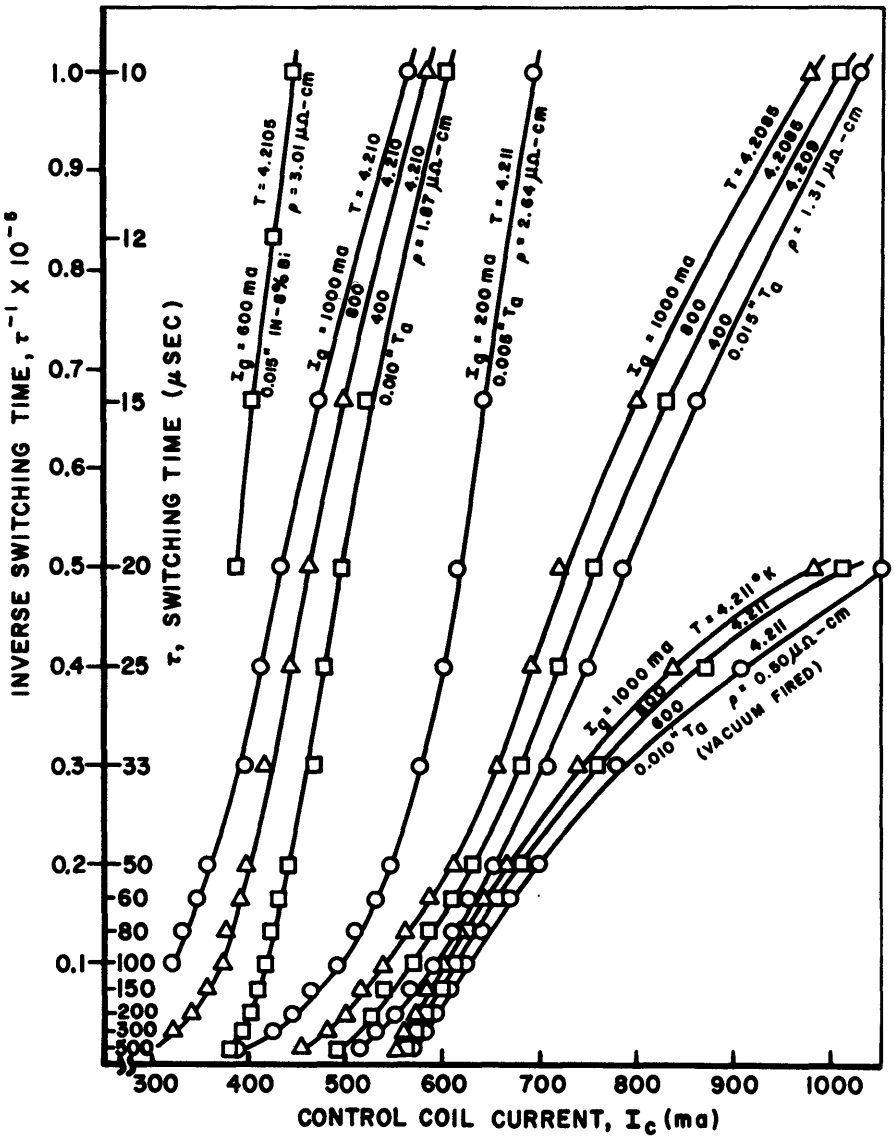


Fig. 4. Inverse switching speed as a function of control current

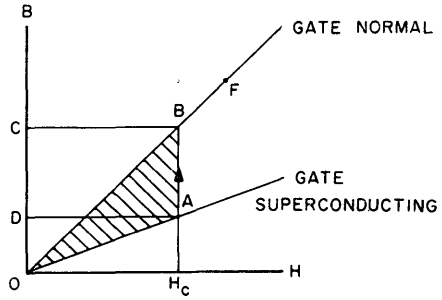


Fig. 5. B-H loop of an inductor containing a superconductive core

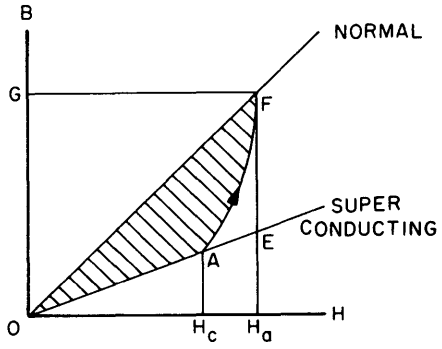


Fig. 6. Switching locus for $H > H_c$

coil which sets up the longitudinal field is smaller when the gate circuit is superconductive than when it is normal. The effect is caused by the exclusion of magnetic flux from the body of a superconductor, an effect discovered by Meissner and Ochsenfeld[7] in 1933, which is, in fact, the basis for the most common method of identifying new superconductors. Therefore, there are two *B-H* lines, Fig. 5, for an inductor with a superconductive core. As one applies an external magnetic field, H, the induction increases along the low-inductance line OA. When H reaches H_c, switching occurs, and the induction increases along path AB as flux enters the superconductor. For $H > H_c$, induction increases along the higher inductance line BF.

During the switching process, an average energy density equal to the area $ABCD$ is added to the volume of the inductance by the source maintaining H. The average energy density in the volume before the superconductor switches is equal to the area OAD and after switching to the area OBC. The energy per unit volume lost in eddy currents during switching is equal to the energy added before and during switching minus the energy stored after switching, and is equal to the area $OAD+ABCD-OBC=OAB$. The energy dissipated per unit volume of superconductor OAB, is half that added during switching, $ABCD$, and is equal to $\mu_o H_c^2/2$. The other half is analogous to a latent heat.

During switching caused by H larger than H_c, the exact switching path in the *B-H* plane depends on the rate of rise of the step longitudinal magnetic-field intensity relative to the rate of propagation of the superconducting-normal boundaries through the material, Fig. 6. The maximum energy dissipation, equal to $\mu_o H_a^2/2$ would result from a field which rises from O to H_a (B increases along line OE) in zero time. The path illustrated in Fig. 6 implies an average B and H over the superconductive body. Actually, it is believed that the magnetic field intensity on the superconducting-normal boundaries is nearly equal to H_c; the difference between the H applied and H_c is the counter-H due to eddy currents.

Switching in the presence of a conduction current is more difficult to analyze from an energy standpoint. If the gate current has a constant value throughout the switching interval, a power dissipation, which increases with time as the resistance reappears, plus an additional energy storage term due to the self-field of the gate current must be taken into account. In many cryotron circuits, the gate current in a given cryotron is being rerouted into a new path by the switching of that cryotron, and in this case, an amount of energy must be dissipated which is equal to that stored in the new and old paths by the gate current.

The energy dissipated per unit volume per switching operation can be approximated by $\mu_o H^2/2$ for the purpose of comparison with other devices. A typical cryotron using tantalum wire at 4.2 degrees Kelvin switches in a field of 4,000 ampere-turns per meter. The average energy dissipated per unit volume during switching is therefore 10 joules per cubic meter. This loss can be compared with that of a ferrite memory core with $H_c=1$ oersted$=79.5$ ampere-turns per meter, and $Br=1{,}000$ gauss$=0.1$ weber per square meter. The area of two quadrants

of the *B-H* loop in about 16 joules per cubic meter. The loss can be further compared with that of a ferroelectric condenser made of $BaTiO_3$ with $E_c = 500$ volts per centimeter = 50,000 volts per meter, and $Dr = 0.18$ coulombs per square meter. The area of two quadrants of the *D-E* loop is about 18,000 joules per cubic meter.

Conclusion

Experimental results indicate a straight-line relationship between reciprocal switching time and applied magnetic field for superconductors. The fastest switching observed to date at Massachusetts Institute of Technology is 0.1 microsecond for a thin-film cryotron. Switching energy density is approximately 2.5 joules per cubic meter as contrasted to about 8 for ferrites and 9,000 for ferroelectric barium titanate.

References

1. THE CRYOTRON—A SUPERCONDUCTIVE COMPUTER COMPONENT, **D. A. Buck.** *Proceedings*, Institute of Radio Engineers, New York, N. Y., vol. 44, pt IV, April 1956, pp. 482–93.

2 PROCEEDINGS OF THE EASTERN JOINT COMPUTER CONFERENCE *AIEE Special Publication T-92.* "A Cryotron Catalog Memory System," **A. E. Slade, H. O. McMahon.** May 1957, pp. 115–20.

3 THE PHASE TRANSITION IN SUPERCONDUCTORS II. PHASE PROPAGATION ABOVE THE CRITICAL FIELD, **T. E. Faber.** *Proceedings*, Royal Society, London, England, pt. A, vol. 219, 1953, pp. 75–88.

4. NORMALIZED SWITCHING FUNCTIONS OF CRYOTRONS, **C. Turk.** *MS Thesis*, Massachusetts Institute of Technology, Cambridge, Mass., 1956.

5. SUPERFLUIDS (book), **F. London.** John Wiley & Sons, Inc., New York, N. Y., 1950, pp. 120–24.

6. SUPERCONDUCTIVITY (book), **D. Schoenberg.** Cambridge University Press, Cambridge, England, 1952, pp. 130–37.

7. **W. Meissner, R. Ochsenfeld.** *Naturwissenschaften*, Berlin-Charlottenberg, Germany, vol. 21, 1933, p. 787.

Discussion

J. L. Nevins (Massachusetts Institute of Technology Instrument Laboratory): What is the present switching time for cryotron elements?

Mr. Slade: Dudley Buck has reported switching a single film cryotron in 0.1 microseconds and there have been unofficial reports of faster switching times. However, the control coil of a cryotron is entirely inductive, and if it is being driven by the gate of another cryotron, as it often is, the switching time of the circuit is much longer. The time constant of such a circuit is governed by the coil inductance divided by the gate resistance. For present-day cryotrons this switching time is about 500 microseconds.

H. Robbins (Hughes Aircraft): How many watts of refrigerator power are needed for each watt of power dissipated in the cryotrons?

Mr. Slade: A theoretically perfect refrigeration machine would require a ratio of input power to dissipated power approximately equal to the ratio of room temperature to 4 degrees absolute: or about 100 to 1. Because of the inefficiency of the machine I would estimate that for an actual machine the ratio is about 600 watts input power for every watt dissipated. This is not as serious as it might seem because cryotrons dissipate so little power. For instance, in a particular cryotron memory system, reported in this issue, no power is dissipated under steady state conditions, and the memory dissipates only 5 microwatts during a normal interrogation.

E. J. Schubert (Westinghouse Electric Corporation): What are the limits of switching time (transition periods) in view of the penetration depth with respect to the dimensions of the superconductor?

Mr. Slade: Switching of superconductors has not been observed in times shorter than 10^{-8} seconds because of instrumentation difficulties. The low magnetic-field strength steady-state behavior of superconductors as measured by the Q of a resonant superconductive cavity show that superconductors start to show small amounts of resistance in the 3,000 megacycle region. In the infrared region materials do not exhibit superconductivity at all. Therefore, one may infer that there is a relaxation spectrum for superconductivity which falls off somewhere in the short microwaves. Recent measurements at the Westinghouse Research Laboratory in East Pittsburgh, Pa., verify this. It is not possible to conclude at what upper frequency superconductors can be switched, but if the high magnetic-field strength and low magnetic-field strength characteristics drop off at the same frequency then the shortest switching time may be in the 10^{-9} region.

R. Jepperson (International Business Machines Corp.): Are not difficulties encountered in connecting inputs and outputs, since a wire passing from room temperature to operating temperature would have many conducting states?

Mr. Slade: No, there are no difficulties in this respect. Zero-resistance interconnecting wires are of course desirable in order to minimize joule heating, but they are not necessary. The resistance of the input and output leads merely adds to the resistance of the external equipment. Superconducting wires are only necessary within a logical building block such as a flip-flop or a multiposition switch.

A 2.5-Megacycle Ferractor Accumulator

R. D. TORREY T. H. BONN

INVESTIGATIONS of magnetic amplifiers at high frequencies indicate that reliable operation with a power gain of about three or four is possible at an information frequency of 2.5 megacycles using series pulse-type magnetic amplifiers. A unit employing several cores was constructed in order to gain experience in packaging and with operating problems at this frequency. Before going into a description of the unit itself a short explanation of the operation of the magnetic cores is given.

The clock- or power-pulse source for the cores is a low impedance 2.5-megacycle sine-wave source with a peak amplitude of 20 volts. A tapped output transformer is used supplying two phases of clock power 180 degrees apart at both full- and half-amplitude voltages.

At this frequency a sine-wave clock offers advantages over square wave or other discontinuous types of clock wave forms. Several of these advantages are

1. Ease of generation and distribution. Generation of sine-wave power at high frequencies offers no problems. The requirement of a low source impedance means a distribution system with high distributed capacity, and a sine-wave clock supply that allows this capacity to be tuned out.

2. Reduction of diode-enhancement effects. Measurements of effective reverse leakage have been made on rapid-recovery type diodes at 2.5 megacycles. These measurements indicate that the effective reverse leakage using a sine wave is about one half the leakage expected using a square-wave clock. The reduction in leakage results from the fact that diode currents are decreasing toward the end of the cycle.

3. The losses due to core winding and wiring inductances are minimized when using sine waves. These losses appear as a phase shift of output, with most of the energy

R. D. TORREY and T. H. BONN are with Remington Rand Univac, Division of Sperry Rand Corporation, Philadelphia, Pa.

This work was supported by the Air Force Cambridge Research Center, Lawrence G Hanscom Field, under contract AF19(604)-1376. The authors are indebted to J. Presper Eckert for his encouragement and support of this work.

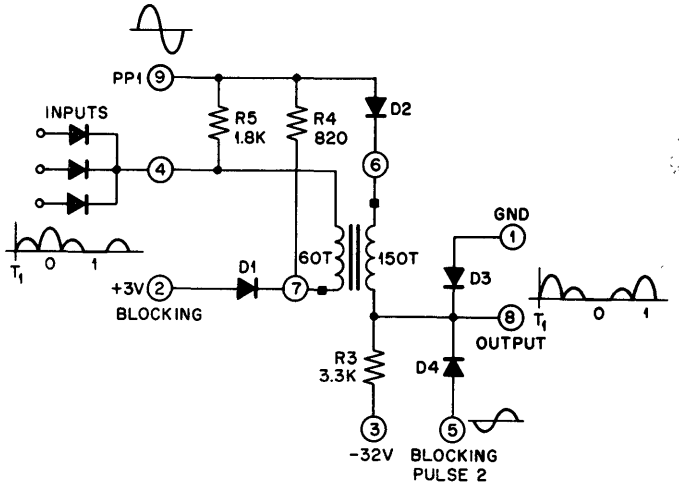


Fig. 1. Complementing or inverting type amplifier

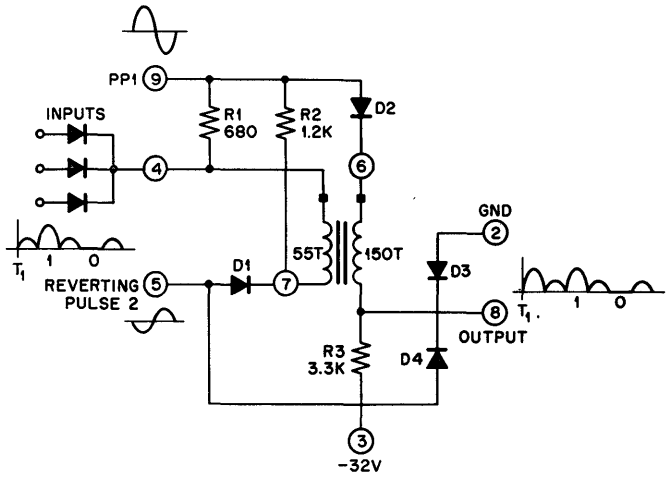


Fig. 2. Noninverting type of amplifier

stored in the inductors being regained toward the end of the cycle. This advantage is not realized if diode-resistor constant-current gating networks are used between cores, for then the core loads may appear as constant-current sinks. In this case the energy stored in the inductors is returned to the clock source rather than to the loads.

The magnetic amplifiers used are of two types, an amplifier which gives an output on receipt of a signal, and an inverting or complementing type amplifier which gives an output only when no input signal is present. These two types of amplifiers are all that are necessary to perform all logical functions.

The amplifiers are series pulse type amplifiers, with a cycle of operation divided into an input period and an output period. Thus, there is a pulse time delay of 0.2 microsecond in going through each amplifier. A diagram of the complementing or inverting type amplifier is shown in Fig. 1.

The core itself consists of five wraps of $^1/_{32}$-inch wide, $^1/_8$-mil thick, 4-79 Moly-Permalloy wound on a 0.1-inch diameter stainless steel bobbin. Input and output windings of no. 43 high-frequency wire are applied as shown. Operation of the circuit is as follows:

At the end of a power pulse the core is left in a state of positive saturation. As the power pulse at terminal nine goes negative, resistor R_4 will clamp in at +3 volts through diode D_1. The lower end of R_5 will be clamped at ground potential through the input diodes and diode D_3 of the previous stages.

In the absence of an input pulse during the time the power pulse is negative, a current will flow from the 3 volt blocking source through the input winding and resistor R_5 to the now negative clock line. This current will overcome any reverse leakage through the output diode D_2, and maintain the core at positive saturation. The core is then a low impedance to the following positive clock pulse and a large output will result.

If, however, an input pulse is present as the clock goes negative, the input terminal four will be raised above 3 volts, and a current will flow from the input terminal through the input winding and resistor R_4 to the now negative clock line. This current is in a direction to switch the core from positive to negative saturation. When at negative saturation, the core will present a large impedance to the following positive clock pulse as it switches from negative to positive saturation, and only a small magnetizing current will flow in the output winding as the core switches from negative to positive saturation.

The combination of R_3 and diode D_3 provide a current sink that will absorb this small output current so no voltage will appear at the output during the power-pulse period.

A positive blocking pulse of half the power-pulse voltage is applied to the output circuit through diode D_4 during the time the power pulse is negative. This insures that there is sufficient back voltage across diode D_2 to keep it open while an input signal is switching the core from positive to negative saturation.

The input circuit of the core is disconnected during its power-pulse period since the whole input winding is raised by the positive power pulse, opening the input diodes and diode D_1. Therefore, the presence of the blocking pulse from other cores on the input line during this time has no effect on the circuit.

Resistor R_4 and diode D_1 are used only as current limiting devices to prevent a short circuit to the input pulse if an input signal drives the core to negative saturation.

The input signal to this core comes directly from the preceding cores through the input isolating diodes. If the lack of an input signal is regarded as an information "one" then this core is a gate, for all input signals must be absent to produce an output. At the output terminal the presence of a pulse is regarded as an information "one."

If the presence of an input signal is regarded as an information "one," then the core is an "or" circuit, for any input pulse will result in no output. Of course, the lack of output is still regarded as an information "one." It can be seen that a series chain of these cores will yield the logical configuration "and," "or," "and," "or," etc.

A noninverting type of amplifier is shown in Fig. 2. This amplifier will give an output pulse only on receipt of an input pulse. This amplifier is primarily used to provide a pulse time delay to allow negation in the inverting cores. The operation of this circuit is much like that of the complementer except for the reversed polarity of the input winding.

At the end of a positive clock pulse the core will be left in a state of positive saturation. As the clock pulse goes negative, resistor R_2 will clamp in at the potential of the positive half-voltage reverting pulse through diode D_1. The lower end of resistor R_1 will be clamped to the ground through the input diode and diode D_3 of the previous stage.

In the absence of an input pulse, a current will flow from the reverting pulse source through diode D_1, the input winding and the resistor R_1 to the now negative clock line. This current is in a direction to reset the core from positive to negative saturation. When at negative saturation the core presents a large impedance to the following positive clock pulse as the clock pulse switches the core from negative to positive saturation. During this time

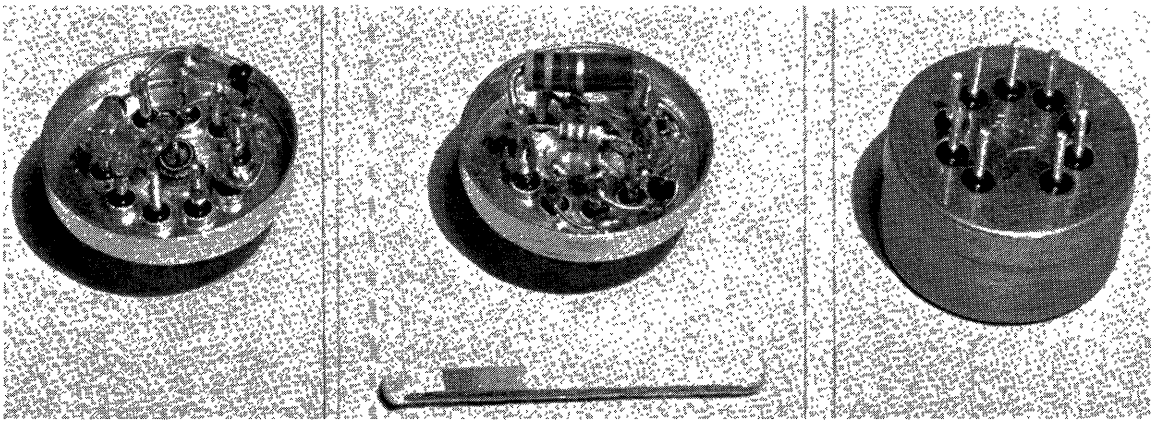


Fig. 3. Three package types

only a small magnetizing current flows in the output circuit, and this current is absorbed by the combination of resistor R_3 and diode D_3, yielding no output pulse.

If, however, an input pulse is present during the time the power pulse goes negative, the input terminal will be raised in potential above the reverting pulse, and a current will flow from the input terminal through the input winding and resistor R_2 to the negative clock line. This current is in the direction to hold the core at positive saturation, and to overcome any reverse leakage through diode D_2 tending to reset the core to negative saturation.

The same output blocking-pulse considerations apply to the amplifier as well as the complementer, for when the reverting pulse switches the core from positive to negative saturation a voltage will be induced in the output winding to cause diode D_2 to conduct and load the input winding. In this amplifier the same wave form is used for reverting the core and blocking the output winding.

The numbered terminals appearing on the figure refer to the pin numbers of the novel header in which the core is mounted. Because of the small physical size of the components, a core and all associated resistors and diodes can be mounted in a small sealed header, yielding a completely self-contained logical package. Input diodes are also mounted in clusters in a header.

Thus, only three package types are necessary for all logical operations. The body of the accumulator itself consists only of sockets and the wiring between sockets. The three package types are shown in Fig. 3. Four sine-wave power pulses are required, and their distribution presents problems because of the low impedance of the unit. Open-wire lines have too high an inductance and are not acceptable.

The problems of inductance can be seen when it is considered that the unit represents a load of approximately 15 ohms on the clock source. An inductance of 1 microhenry has a reactive impedance equal to this at the operating frequency of 2.5 megacycles, and therefore leakage and load inductances must be kept at extremely low values for reasonable power-pulse regulation. Distributed capacity at these impedance levels is relatively unimportant, and the major concern is with inductance.

The clock transformer is illustrated in Fig. 4. It is of special construction to minimize leakage inductance. The primary winding is of single-layer center-tapped construction, and the output winding consists of a thin, flat strip with the same over-all width as the primary. This type of construction yields a transformer with an output-winding leakage inductance of approximately 5 milli-microhenries.

The radio-frequency transmission line is effectively an extension of the transformer output winding, and consists of five strips of 4-mil copper tape separated by layers of 2.5-mil insulation. The inductance of the transmission line between adjacent conductors is approximately 0.4 milli-microhenries per inch. Distribution of the clock pulses within the unit itself presents problems, though not of the magnitude presented in the transmission line which must supply power to all cores simultaneously.

The method for the distribution of power pulses within the unit is again an extension of the parallel flat-conductor principle, but here the parallel conductors have been expanded into a laminated structure of five conducting sheets with insulation between each foil sheet. Each sheet carries a different power pulse, and

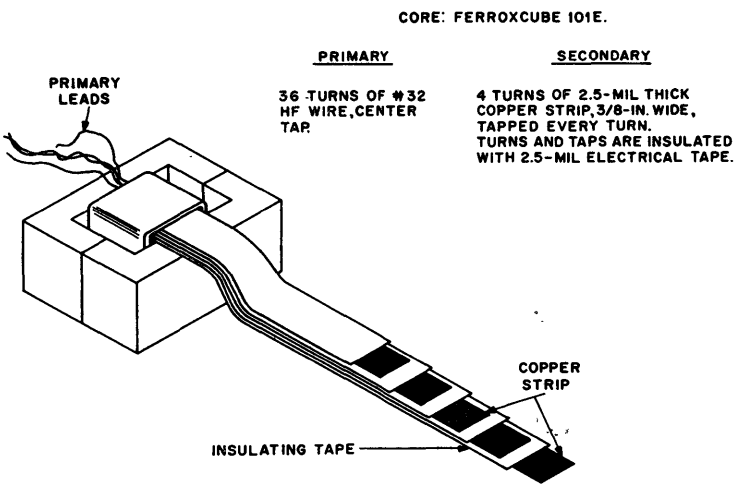


Fig. 4. Clock transformer

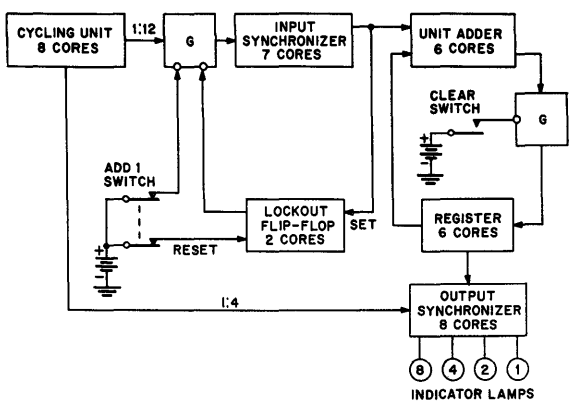


Fig. 5. Block diagram of the accumulator

turret lugs spaced symmetrically on the structure make contact to the separate sheets. Each core socket is surrounded by terminals to any one of the four power pulses required, keeping lead length of the clock lines to a minimum.

This type of construction offers another advantage. So far all effort has been geared toward keeping the power distribution lines to low inductances, but it is just as important to have low inductance in the output lines of the magnetic amplifiers since these lines also carry relatively large currents.

The laminated structure described inherently provides a ground plane for all currents. If the wiring between cores is spaced closely to the clock distribution sheets, then the circuit loops are small and the inductance is low. It should be pointed out that for a unit of this size and power level the pains taken with the distribution system are not necessary. However, the method employed is in the right direction for handling low-impedance circuits, and appears adaptable to mass-production techniques such as stamped or printed construction.

A block diagram of the accumulator is shown in Fig. 5. It consists of a unit adder and a four-bit circulating register. Provision is made to add in unity each time a push button is pressed, and for the accumulated count to be displayed by means of incandescent lamps powered directly from cores. Thirty-seven cores are used altogether, 12 being used in the adder and register, the other 25 used for cycling and input and output synchronization.

The cycling unit presents every twelfth pulse to the gate *G* which is enabled when the ADD switch is depressed. The synchronizing unit ignores the first input pulse since it may be marginal, and presents the second input pulse to the adder while closing the gate by means of the lockout flip-flop to prevent further input signals. Releasing the ADD button opens gate *G* and resets the lockout flip-flop.

Since the register is circulating, the contents may be sampled only once every four pulse-times to display the contents. The indicator lamps are therefore only energized on an approximate 10 per cent duty cycle, but still provide enough illumination for display purposes. Fig. 6 shows the complete unit.

At this frequency each core is capable of driving three to four other cores. Noncritical components have been used in the unit, with each core having an allowable flux variation of ± 5 per cent, and all resistors being ± 10 per cent stock-value carbon resistors. Satisfactory operation is obtained over a clock voltage range of 18 to 25 volts. The clock source is a single oscillator tube.

The clock input power is approximately 15 watts, or 400 milliwatts per core. An additional 10 watts of d-c power is used to supply clamp voltages. As each core is a complete logical element, the total input power is only 666 milliwatts for each gate or buffer, which compares very favorably with any other type of computer circuitry.

As was pointed out earlier, this unit was constructed only to test the operation of magnetic amplifiers in the megacycle range. The unit has shown that operation at 2.5 megacycles using practical tolerances and components is feasible.

Discussion

R. E. Montijo (Radio Corporation of America): What advantages do you claim for the magnetic circuits described over functionally comparable transistor circuits?

Mr. Torrey: Comparable transistor circuits capable of driving three or four others at an information rate of 2.5 megacycles are not very common at present and are fairly expensive. However, this situation will certainly improve. The attractive features of magnetic amplifiers are their long life expectancy and relative lack of sensitivity to environmental conditions, particularly temperature, humidity, and electrical noise. Also, where high speed is combined with high power levels, such as driving coincident-current memories or heavily loaded busses, magnetic amplifiers can perform functions impossible with presently available transistors.

K. Preston, Jr. (Bell Telephone Laboratories): What type of diodes are used in your circuitry?

Mr. Torrey: The diodes used are germanium diodes with low-forward voltage drop. The output diodes are further characterized by being the so called "fast recovery" type and are of gold-bonded construction. Several manufacturers make these types of diodes for computer applications.

E. Cohler (Sylvania Electric Products): What is the "add" time of the 2.5-megacycle accumulator?

Mr. Torrey: Being a serial adder, the addition time is dependent upon word length. The adder has three cascaded stages, and produces a 0.6 microsecond delay from input to output. However, being serial, digits can be fed to the adder at a 2.5 megacycle rate.

J. C. Lozier (Bell Telephone Laboratories): Since your amplifier does not regenerate each pulse, what limitations does this place on logical design, reliability of pile up, and so forth?

Mr. Torrey: The pulses are reshaped and relocked in each stage by means of the regularly recurring power pulse. Regeneration is not used, but if a signal is above a certain critical amplitude, in a long chain of amplifiers, it will grow to be a full amplitude pulse. The limitations put upon the logical designer are:

1. As this is a 2-phase synchronous system, he must keep track of phase and of delays to insure that the signal arrives at its destination in the right phase and at the right time.

2. The logical designer must not load the output of any stage so heavily that there is a chance the output may fall below the critical level, and thus be attenuated as it progresses from stage to stage.

High-Temperature Silicon-Transistor Computer Circuits

JAMES B. ANGELL

Synopsis: This paper considers the application of silicon-alloy transistors to digital-computer circuits, such as flip-flops and gates, suitable for operation at high temperatures. Circuits using the T-1159 silicon surface-alloy transistor will perform at temperatures as high as 140 C (degrees centigrade) with switching times on the order of tenths of a microsecond (μsec). No particular precautions or compensating components are required in order to obtain such performance.

THE Philco T-1159 silicon surface-alloy transistor is a p-n-p transistor with precision geometry and the desirable characteristics of wafer transistors which make such units the most suitable transistors for switching service. This transistor, a particular version of the class recently described by Thornton and colleagues,[1] has a precision geometry obtained in two steps. Initially, electrochemical jet etching is used to shape the wafer. The emitter and collector are applied by evaporation and a very carefully controlled alloying process. A cross-sectional diagram is shown in Fig. 1; the width of the base is typically 0.0001 inch, with a collector diameter of 0.0011 inch.

Typical T-1159 electrical parameters are as follows:

$h_{fe} = 18$
$f_\alpha = 13$ megacycles
$r_{SAT} = 5$ ohms
$I_{CO}(-3 \text{ volts}) = 10^{-10}$ amperes
$C_{ob} = 7$ micromicrofarads
$f_{MAX} = 15$ megacycles
$r_b' = 400$ ohms
$r_{ob} = 600$ kilohms
$h_{ib} = 50$ ohms

The most significant of these parameters for switching service are the alpha cutoff frequency, the saturation resistance ($r_{SAT} = V_{CE}/I_C$ with $I_C = -10$ *ma*, $I_B = -3$ *ma*), the current amplification factor, and the extremely low collector cutoff current, I_{CO}.

An indirect result of the extremely low I_{CO} and the low saturation resistance is the ability of this transistor to serve as a direct-coupled unit, in direct-coupled transistor logic circuits. This point is emphasized by the superposed collector characteristics and feedback characteristics shown in Fig. 2. It can be seen from the room-temperature collector characteristics, which are plots of collector to emitter voltage versus collector current for different values of base current, that the current gain and output impedance are high for voltages more negative than 0.1 to 0.2 volt. The feedback characteristics, which are plots of base to emitter voltage versus the same scale of collector current for the same steps of base current, show that the base voltage of a transistor in conduction is greater than 0.6 volt. The high ratio of base voltage to collector voltage at the edge of saturation is the basic requirement for direct coupling, as has been described previously.[2]

The alpha cutoff frequency of these transistors is sufficiently high that switching times of 0.1 to 0.2 μsec are typical. The significant cutoff frequency, of the internal transistor action, cannot be conveniently measured directly, because the ohmic base resistance affects the cutoff frequency of the short-circuit common-base current amplification. However, this internal "alpha" cutoff frequency can be closely approximated by measuring the common-emitter short-circuit current transfer ratio, h_{fe}, at a high frequency. Since h_{fe} is inversely proportional to frequency, the product of this ratio at any frequency and the frequency of measurement indicates the frequency at which the current transfer ratio is unity. The frequency of unity current gain is close to, although slightly less than, the internal alpha cutoff frequency; it is the frequency of unity current gain that is typically 15 megacycles in these transistors.

Transistor Parameters Versus Temperature

The variation of the electrical parameters of the T-1159 silicon-alloy transistor will be considered next, before optimum circuits for high-temperature operation are studied. Changes in the static characteristics, as shown in Fig. 2, will be described first. The variation in the collector characteristics with temperature is not appreciable, except that the current transfer ratio, h_{fe}, obviously increases. While the saturation resistance rises somewhat with temperature, the concurrent increase in current gain means that the saturation voltage for given currents does not increase noticeably.

The feedback (base voltage) characteristics are somewhat more temperature dependent than the collector characteristics. It can be seen that the base voltage at the onset of significant conduction drops from 0.6 volt at room temperature to about 0.4 volt at +140 C. It can also be noted that the base spreading resistance, r_b', increases with temperature; this fact is responsible for the greater vertical separation of adjacent feedback characteristics in Fig. 2.

The variation in input characteristics can also be seen by reference to Fig. 3, which shows plots of input current versus input voltage (base to emitter) for a fixed collector voltage. Here again, it can be seen that the threshold base voltage, above which conduction takes place, decreases with temperature, whereas the incremental input impedance, inversely proportional to the slope of the input characteristics, increases. In this figure the slope of these curves in the linear region is very close to $1/r_b'$.

Even though the base to emitter voltage corresponding to the threshold of conduction decreases with increasing temperature, these transistors still have direct coupling characteristics at 140 C which are superior to those of germanium transistors at room temperature.

Normalized curves of the variation of various small-signal parameters with temperature are shown in Fig. 4. The increase in short-circuit current transfer ratio, h_{fe}, with increasing temperature is desirable; the decrease of this quantity at low temperatures may be significant in cases where low-temperature operation is required. The slight variations of input impedance, h_{ib}, and output admittance, h_{ob}, are not particularly significant in switching service. The collector cutoff current, I_{CO}, follows very closely a rate of change of 7 per cent per degree centigrade, and is generally less than one microampere at +140 C. This figure is small enough to be insignificant in most switching services other than direct-coupled gating, where the character-

JAMES B. ANGELL is with the Research Division, Philco Corporation, Philadelphia, Pa.

The contributions of Joseph Karew and Irving Horn in studying the high temperature characteristics of these transistors and their circuits, and in developing many concepts which simplify the understanding of the importance of various transistor parameters in such circuits, are gratefully acknowledged. Much of the work on which this paper was based was made possible by the support of the Air Force Cambridge Research Center through contract AF19(604)-1586.

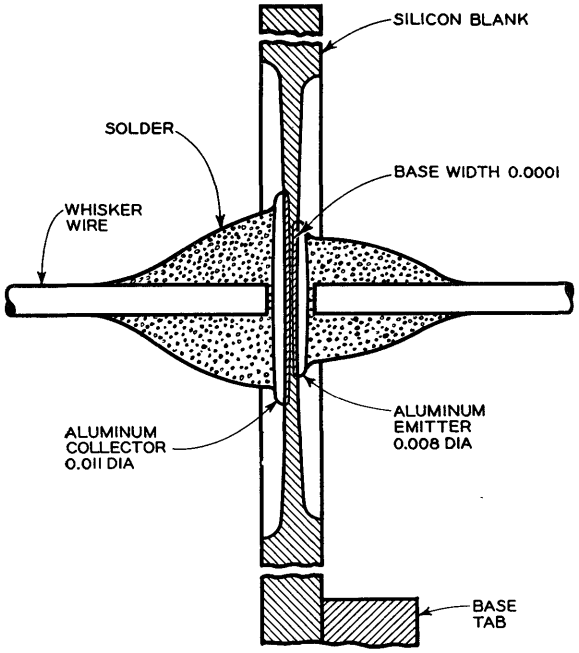


Fig. 1. Silicon surface-alloy transistor

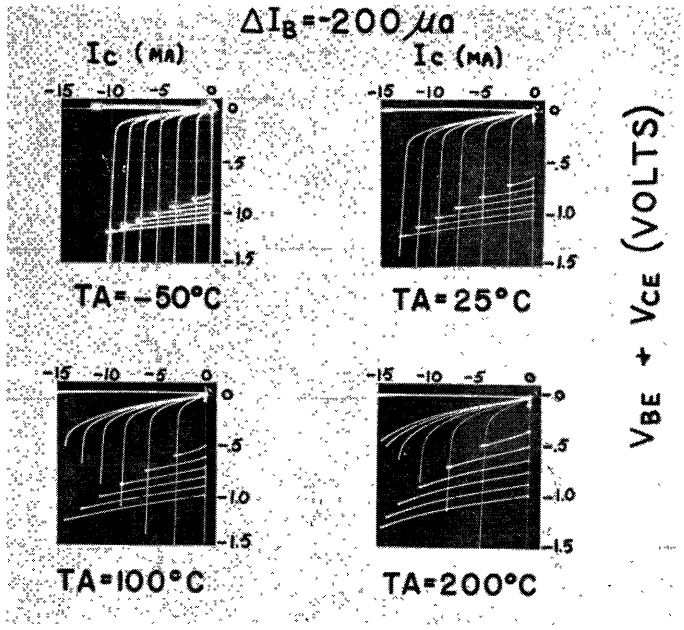


Fig. 2. T-1159 common-emitter collector and feedback characteristics

istics displayed in Fig. 2 give an adequate clue to performance.

Among the high-frequency transistor parameters, the only one that varies significantly is the base spreading resistance, r_b'. This variation is illustrated in Fig. 3. It is found that the base resistance varies roughly linearly with temperature, and is approximately double its room temperature value at +140 C. This variation in r_b' can be significant in some cases because it may limit the speed with which the transistor can be brought out of saturation by a turn-off signal applied to the base.

High-Temperature Circuits

Now that the variations of transistor parameters with temperature have been considered, it is possible to compare some basic switching circuits. It is appropriate to start with the direct-coupled class of switching circuits, in which these transistors are so well suited.

Direct-Coupled Flip-Flop

The circuit of a typical loaded direct-coupled flip-flop is shown in Fig. 5. Shown in the circuit are the two gates used to set the flip-flop and the three loads (bases of controlled transistors) on each side of the flip-flop. Although both of the load resistors are normally returned to the same supply voltage, one is shown returned to a variable voltage, called the "handle", with which a so-called "schmoo"* diagram of the operation of the flip-flop can be obtained. Schmoo diagrams for various temperatures are shown in Fig. 6. The curves in this diagram were obtained by varying the handle, for a given temperature and for a given equal load resistances, in each direction until the flip-flop could no longer be set or reset. The upper and lower limits of operation are plotted. After repeating this procedure for different load resistances and plotting the corresponding limits of operation, it is possible, by connecting the plotted points, to draw a curve representing the limits of operation of the flip-flop. Various curves, obtained for different temperatures, frequently resemble schmoos in shape, hence the name. The plots of Fig. 6 show that the flip-flop, loaded with four bases on each side, has a wider range of operation at high temperatures than at low temperatures. The increased range of operation at high temperature is associated with the increased h_{fe} of the transistors. It can be seen that even at +140 C the circuit is definitely noncritical, whereas at −50 C the range of operation is quite restricted. The assymetrical appearance of the various curves around 3 volts results from the fact that the transistors used in the flip-flop were chosen to have considerably different h_{fe}, in order to illustrate the most unfavorable case.

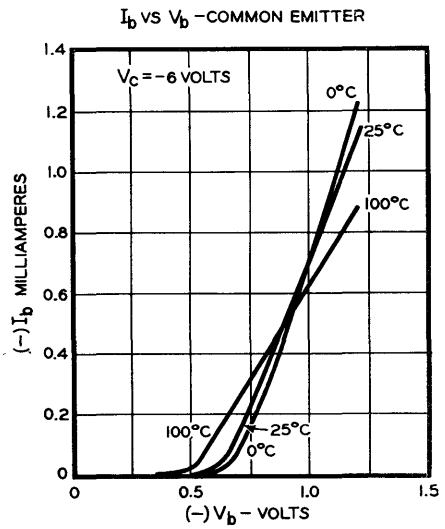


Fig. 3. T-1159 common-emitter input characteristics

The speed of a direct-coupled flip-flop is illustrated by the curves of Figs. 7 and 8. Fig. 7 shows the delay time of a direct-coupled flip-flop loaded with two bases on each side, while Fig. 8 shows the fall time of the same circuit. The higher speed associated with the larger load resistances is attributable to the reduced effect of the base spreading resistance, r_b', of the transistor, when compared to the load impedance. The increase in delay time and fall time with temperature is similarly due primarily to the variation in r_b' with temperature.

R-C (Resistance-Capacitance) Coupled Flip-Flop

The *R-C* coupled flip-flop is similar to the direct-coupled flip-flop, except that parallel combinations of a resistor and capacitance are included in each base lead. The resistor tends to limit the base current, so that hole-storage delay time

* A mythical animal created by cartoonist Al Capp.

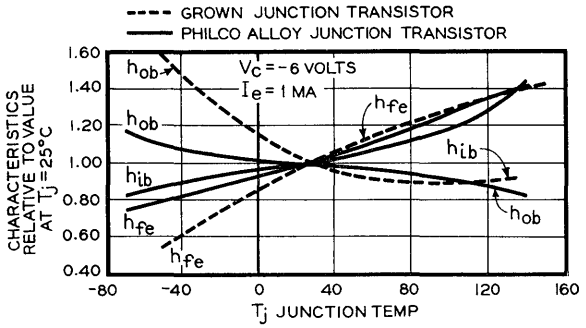


Fig. 4 (above). Normalized temperature dependence of T-1159 small-signal parameters

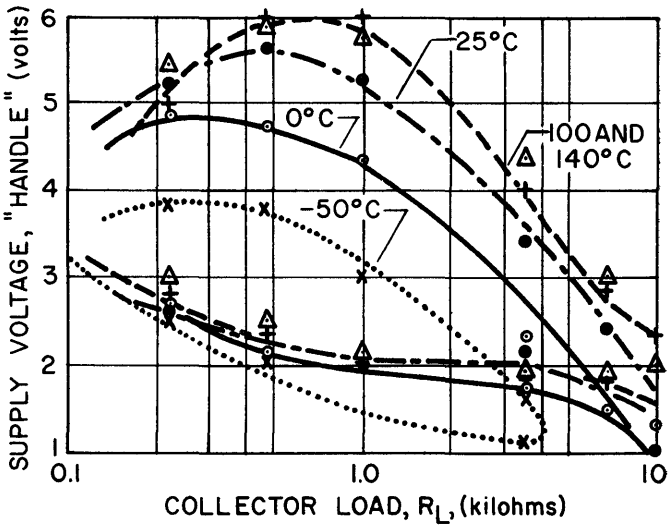


Fig. 6 (right). Operational boundary, schmoo diagram of direct-coupled-flip-flop

is reduced, while the capacitance assists in turning off a transistor by driving its base to a positive potential. Fig. 9 shows a typical *R-C* coupled flip-flop circuit.

It is found that the additional resistance in the base lead tends to reduce the stability of a *R-C*-coupled flip-flop circuit, because it reduces the base current into the conducting transistor. The reduction in stability, when compared to the direct-coupled circuit, is emphasized by the data in Table I. This table compares the stability of flip-flops loaded on each side with two bases.

Table I. Flip-Flop Stability

Temperature, C	R-C Coupled Stability	Direct-Coupled Stability
+140	0.72	0.86
+25	0.46	0.74
−40	0 26	0.70

Stability in this sense is defined quantitatively in terms of the current gain from the base of one transistor in the flip-flop to the base of the other transistor or to one of the loads $S=1-1/G=1-K+N/h_{FE}$ where $K=R_B/R_L$ and N is the number of bases tied to each collector. The stability factor is unity if the transistor gain is infinite, and is zero if the transistors have a net gain of unity, just sufficient to provide operation. This table shows that the direct-coupled circuit is the more stable at any temperature, and that the stability of each circuit inceases with increasing temperature. In general, a stability of 0.4 is adequate for reliable flip-flop operation.

Other Flip-Flops

Other more elaborate switching circuits can be employed where it is desired to obtain greater switching speeds without sacrificing stability of operation.[3] For example, emitter followers can be added in the cross-coupling arms of the *R-C* coupled flip-flop to improve both speed and stability. Also, it is possible to eliminate the delay time due to hole storage by adding a resistance common to the emitters of both flip-flop transistors.[4] Typical room-temperature values of switching times are listed in Table II, which compares various circuits with different numbers of loads on each side of the flip-flop. The use of nonsaturating circuitry generally halves the delay time of the *R-C*-coupled or emitter-follower-coupled flip-flops.

Table II. Switching Times of Silicon Transistor Flip-Flops

Flip-Flop	Loads on Each Side	Rise Time	Delay Time	Fall Time
		Millimicroseconds		
Direct-Coupled	0	50	200	80
	4	150	80	120
R-C Coupled	0	25	60	300
	4	30	50	250
Emitter-Follower Coupled	0	60	70	140
	4	100	120	140

Associated High-Temperature Components

Considerable care must be taken in the selection of other circuit components, such as resistors and capacitors, in order to achieve good over-all reliability at high temperatures. In direct-coupled circuits, resistors are the principal component other than transistors. The great majority of resistors required for assembling complex computer circuits have a resistance no greater than a few kilohms. It has been

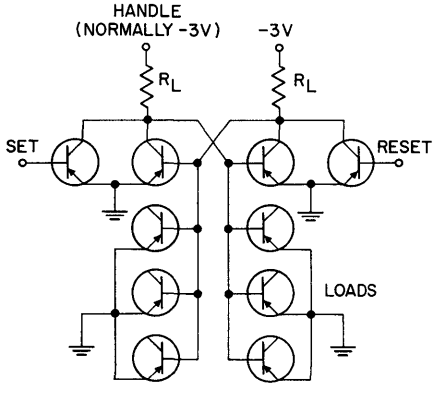


Fig. 5 (left). Direct-coupled flip-flop

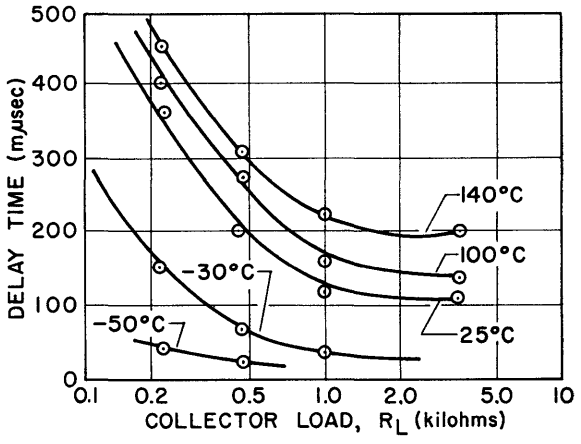


Fig. 7 (right). Delay time of direct-coupled flip-flop

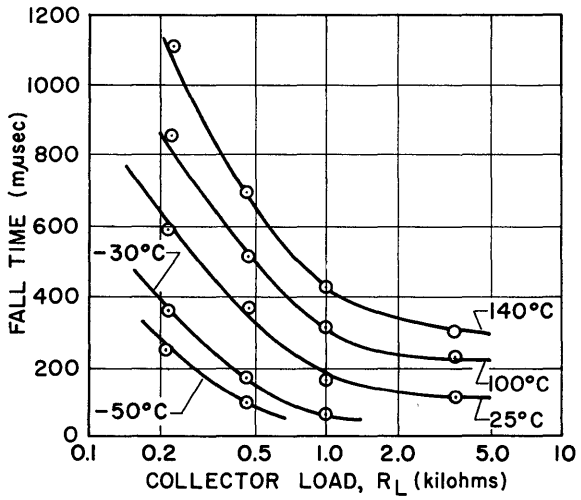


Fig. 8 (left). Fall time of direct-coupled flip-flop

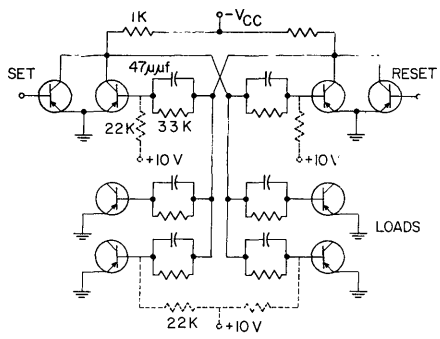


Fig. 9 (right). R-C coupled flip-flop

found that wire-wound resistors rated for high-temperature service have adequately low inductance that they can be used without appreciably affecting the maximum speed of direct-coupled circuit operation with T-1159 transistors. Boron-carbon resistors have been made for the temperature range up to 150 C; such resistors have appreciably less inductance and might be required in circuits demanding the ultimate possible speed. A number of suppliers have recently made available capacitors, such as certain ceramic and Mylar film capacitors, which are capable of operation at sustained temperatures on the order of 150 C. Therefore it is possible to obtain the various components needed in high temperature circuits, although care must be taken in the selection of such components that are capable of withstanding the operation for many thousands of hours at 140 C of which the transistor seems capable.

Conclusion

Silicon transistors are available whose characteristics make possible the design of digital-computer circuits suitable for operation at temperatures as high as 140 C. Direct-coupled transistor logic circuitry is perhaps the most suitable circuit for taking advantage of these characteristics, since its demands on current gain of the transistor are modest. Higher switching speeds may require the use of R-C coupled circuits, to which the addition of emitter followers or higher-gain transistors of the future ensures adequate stability.

References

1. Silicon High-Frequency Transistors, **C. Thornton, J. Roschen, T. Miles.** Presented at the Institute of Radio Engineers Radio Fall Meeting, Syracuse, N. Y., Oct. 15–17, 1956.

2. Directly Coupled Transistor Circuits, **R. Beter, W. Bradley, R. Brown, M. Rubinoff.** *Electronics*, New York, N. Y., vol. 28, no. 6, June 1955, pp. 132–36.

3. High-Speed Transistor Computer Circuits, **S. Y. Wong, A. K. Rapp.** *Electronics*, New York, N. Y., vol. 29, no. 12, Dec. 1956, pp. 180–81.

4. Designing Transistor Flip-Flops, **R. E. McMahon.** *Electronic Design*, vol. 3, no. 10, Oct 1955, pp. 24–28.

Discussion

J. Ricketts (General Motors Corporation): What transistors do you use? Are they available commercially? If not, for military contractors? Who makes the high-temperature resistors and capacitors?

Dr. Angell: The transistors have recently been advertised, and they are Philco transistors. They are available in sample quantities from the Lansdale Tube Company as the T-1159. The advertisements have appeared within the last 2 months in *Electronics*, *Electronic Design*, and *Teletech*. The high-temperature wire-wound resistors that we use were made, I believe, by International Resistance Company. We have also used samples from Bradford Components, Bradford, Pa. The ceramic capacitors were made by Vitramon.

T. H. Bonn (Remington Rand Univac): Why are the *R-C* coupled circuits less stable than direct-coupled circuits?

Dr. Angell: The reason for the lower stability of the *R-C* coupled circuit is the fact that you are limiting base current in that circuit by means of a series base resistor. These transistors, as is characteristic of all silicon transistors, are not remarkably excessive in the way of current gain, so that any limitation on base current likewise limits the stability. Remember that the base current in any gate is equal to the total collector current of the controlling transistor divided by the number of gates you are controlling, times some shrinking factor due to the effect of base resistance.

V. Sferrino (Massachusetts Institute of Technology): How well does the current gain hold up for high collector currents in these transistors at different temperatures?

Dr. Angell: If you will recall Fig. 2, where some typical collector characteristics were shown, the current gain is almost linear out to 15 milliamps. It begins to drop very severely by the time 50 milliamps is reached. This effect is true essentially at all temperatures. Of course, the current gain varies with temperature, but the linearity is certainly good up to 15 mils.

T. Ellis (Rand Corporation): Would you give some figures on maximum ratings?

Dr. Angell: So far as maximum ratings are concerned, 150 milliwatts of dissipation has been set arbitrarily merely because we have not conducted sufficient life tests to know what a good room temperature rating is. Because of the solder question 150 C has been set, it is not known whether that has been increased yet. The voltage is about 10 volts. Above 10 volts, punch-through may occur. It is not a life question chiefly, but a punch-through question. As current is concerned, the number is not known, but 25 milliampere does it no harm.

T. P. Bothwell (Radio Corporation of America): In paralleling gates on a direct coupled flip-flop, how can adequate division of current to each be assured in face of variations of input-breakdown voltage?

Dr. Angell: The question of sharing the current of paralleled bases has not been specified on the general switching transistor that is now being talked about, so that it is a matter of selection at this point. However, as the art matures and as we develop a transistor particularly specified for direct-coupled service, I think that it will be simple to ensure that no transistor will use too much of the current and none will get too little, by setting the specifications just as has been done on germanium transistors specified for direct-coupled switching. In short, it has not been done yet, but there is no particular problem because voltage at the onset of conduction at room temperature is quite repeatable from transistor to transistor. It does not vary by more than perhaps 0.1 volt out of 0.6 volt or more.

A Saturable-Transformer Digital Amplifier with Diode Switching

E. W. HOGUE

Synopsis: A digital amplifier of simple noncritical design incorporating a saturable voltage transformer is described. The clock is a 2-phase, sine-wave voltage source in the 100-kc range. In structure and mode of operation the amplifier stage is particularly suited for use with 2-level diode gating to provide the "and" and "or" logical functions. A complementer employing two saturable transformers provides the "not" function. The volt-second transfer characteristic of the stage critically determines the stability of transmission of binary signals in a long register, or in any closed loop. Factors governing the shape of this characteristic are discussed. The over-all characteristic for n stages is then derived and used to predict binary transmission stability.

SEMICONDUCTOR diode gating of the type shown in Fig. 1 is one of the most satisfactory ways to realize the logical functions of a digital machine. This type of gating is economical in components, straightforward in concept, flexible, and dependable. However, because signal power is lost in transmission through the gates, it is necessary to insert amplifiers at intervals within the gating structure to regenerate the signal. Fig. 1 represents in simplified form the basic logical building block or package used in several well-known computing machines. These machines, SEAC and DYSEAC, etc., are of the synchronous type employing dynamic circuitry. The digital amplifier represented as a black box in this package has both a signal output and an inhibit output. The package therefore provides the logical functions "and," "or," and "not." This amplifier must fulfill the following four conditions:

1. It must be compatible with diode gating.
2. It must have power gain.
3. There must be no possibility of reverse transmission of signal.
4. It must have a transfer characteristic that will ensure stable circulation of binary signals in closed logical loops or long cascades.

E. W. HOGUE is with the National Bureau of Standards, Washington, D. C.

This work was sponsored by the Computer Laboratory, Electronics Research Directorate, Air Force Cambridge Research Center.

Vacuum tubes and transistors have been successfully used to provide the power gain within the black box, with an output transformer for matching, and d-c isolation.

Digital Amplifier Transfer Characteristic

This paper describes a low-power rapid-response magnetic digital amplifier which fulfills the criteria just enumerated. Because the operation of the new amplifier is best understood in terms of its transfer characteristic, the steps in the evolution of an ideal characteristic for binary transmission will first be described. Then, the evolution of the magnetic digital amplifier in terms of each of these steps will be given.

Fig. 2(a) is the characteristic of a linear amplifier having a gain of unity up to its output saturation level S. If signal amplitude S represents the binary *one* and total absence of signal represents the binary *zero*, then it is seen that the amplifier will transmit perfect *ones* and perfect *zeros* without distortion. But it will not emit perfect signals unless it receives perfect signals. A long cascade, or a closed loop of such amplifiers, would not transmit binary signals with stability. In Fig. 2(b) the characteristic has been given a threshold by displacing the point Q to the right. It can be seen that imperfect *zeros* received within the limits O-Q can now be emitted as perfect *zeros*. There is no tolerance to *ones*. In Fig. 2(c) the point P has been displaced to the left. As a result of this characteristic the amplifier will in addition emit perfect *ones* for imperfect *ones* received within the limits PN. The amplifier has a gain of greater than unity above the point R and of less than unity below the point R. In Fig. 2(d) the portion PQ is given an infinite slope. This maximizes the tolerance regions OQ and PN, and minimizes the region for which an imperfect *one* or *zero* can be emitted. Fig. 2(d) is the ideal binary repeater characteristic. The characteristic of the magnetic digital amplifier or magnetic binary repeater to be described approximates that of Fig. 2(c). The over-all characteristic of a cascade of N of these stages approaches Fig. 2(d) for increasing N, with $N=4$ differing from the ideal by a negligible amount.

Saturable Transformer Digital Amplifier

In Fig. 3(b) a transformer having a toroidal core of rectangular loop material is driven by an a-c source having an amplitude e_i and a wave form approximating either a square or a sine wave as shown in Fig. 3(a). The convention will be taken that the positive half-cycle of e_i puts the core in the *one* state; see Fig. 3(c). During the positive half-wave the core is said to "receive" information. The negative half-wave returns the core to its *zero* state. During this time, the core "transmits" the signal it had previously received. The voltage e_o appearing across the output winding during the transmit half-cycle is the output signal of the transformer. The voltage appearing across the output winding during the receiving half-cycle of e_i has no significance, and as will later develop, has negligible effect on the following stage. The transfer characteristic of the conventional amplifier is usually a plot of the output-signal voltage versus input-signal voltage. In a cascade of these amplifiers, voltage amplitude is the quantity that is transmitted. A cascade of like direct-coupled voltage amplifiers whose output is connected in phase to the input will have two stable states, provided the individual voltage transfer characteristics are of the shape of Fig. 2(c), having a region of gain greater than unity and a region of gain less than unity. A similar statement can be made about a closed loop of magnetic amplifiers provided its volt-second transfer characteristic is similar to Fig. 2(c). This is so because the quantity which is transmitted and incidentally stored in each core is magnetic flux. This is proportional to the voltage-time integral of the received signal.

Fig. 3(d) is the volt-second transfer characteristic of the transformer in Fig. 3(b). The voltage-time integral of the signal received by the transformer is plotted on the x-axis; the voltage-time integral of the signal emitted by the transformer during the transmit half-cycle is plotted on the y-axis. The slope of this characteristic is equal to n_2/n_1, the turns ratio. It is shown for the case $n_2=n_1$. A transformer having a one-to-one turns ratio has unity volt-second gain. The core saturates at a volt-second amplitude $2a$ which is equal to the number of turns times the total available change in flux

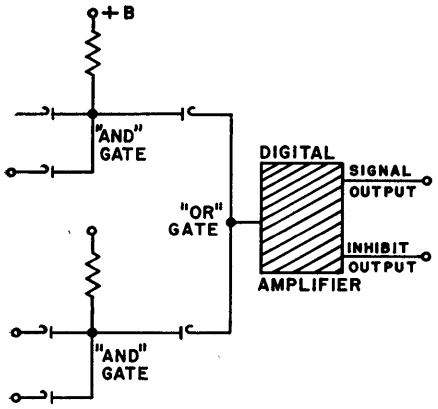


Fig. 1 (left). Diode gating with black-box digital amplifier

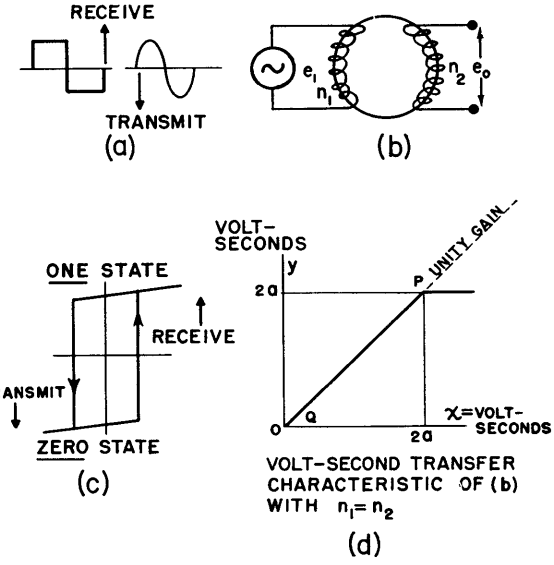


Fig. 3 (right). Linear magnetic repeater

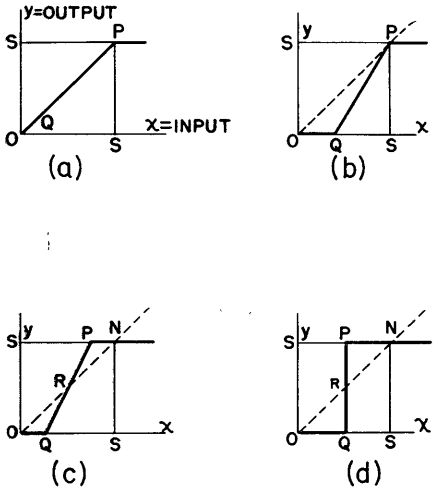
in going from the *one* state to the *zero* state. The transfer characteristic in Fig. 3(d), like that in Fig. 2(a), gives no tolerance to *zeros* or to *ones*.

In Fig. 4(a), a resistor R_s has been added. Because the drop $R_s i_m$ caused by the magnetizing current i_m reduces the signal applied to the primary, the turns ratio has been increased to compensate, keeping e_o equal to e_i, in accordance with the relation $e_o = n_2(e_i - R_s i_m)/n_1$. Fig. 4(b) shows the volt-second characteristic of Fig. 4(a) for $n_2 = 2n_1$. There is now a tolerance to *zeros* of an amount

$OQ = \int_0^{T/2} R_s i_m dt$, where T is the clock period

Before the next step in the evolution of the transfer characteristic is taken, provision is made for the introduction of signals to the stage by the modification shown in Fig. 5(a). Source e_i of Fig. 4(a) is replaced by the combination of R_p, called the pull-up resistor, connected to a positive voltage $+B$ to provide a constant-current pull-up, semiconductor diode D_c called the clock diode, e_c an alternating voltage source called the clock, and D_i called the input diode. A switch S is provided for the manual introduction of *ones* and *zeros* to the stage. R_p is kept large compared with the impedance to ground from point J, and $+B$ is made large enough to provide a constant current sufficiently greater than i_m to keep D_c conducting even on the most positive excursion of the clock. With S open, the core is made to traverse its loop along the path 1-2-3-4-5-1, as in Fig. 5(b), just as it did when the alternating source e_i was directly connected to R_s. See the first 2 cycles of Fig. 5(c) for the wave form at J, and of Fig. 5(d) for the output wave form at L. With S closed, D_i clamps the point J to ground level, taking all the pull-up current. Observe the last 2 cycles of Fig. 5(c). Diode D_c simply opens on the clock upstroke, and no signal is received by the core to reset it to the *one* state. It remains at 1 in Fig. 5(b) until the end of the receive half-cycle of the clock. During the transmit half-cycle which follows, the core travels the path 1-5-6-5-1. Its impedance during this time is low and R_s limits the clock current. The last 2 cycles of Fig. 5(d) show the output wave at L when S is closed. There is a negligible voltage output, and the impedance of the output winding is very low. When S is open, the stage transmits binary *ones*. When S is closed it transmits binary *zeros*. The condition required for the stage to transmit *ones* is that the impedance to ground looking to the left from the point J be high during the receiving half-cycle. The condition required for the stage to transmit *zeros* is that this impedance be low during the receiving half-cycle. During the transmitting half-cycle, this impedance must always be high. The latter condition is ensured by the polarity of the input diode D_i.

Fig. 6(a) shows two magnetic binary repeater stages connected in cascade. Binary signals are introduced into stage A by means of the switch. These signals are then transmitted to stage B, which in turn repeats them at its output L_B. The



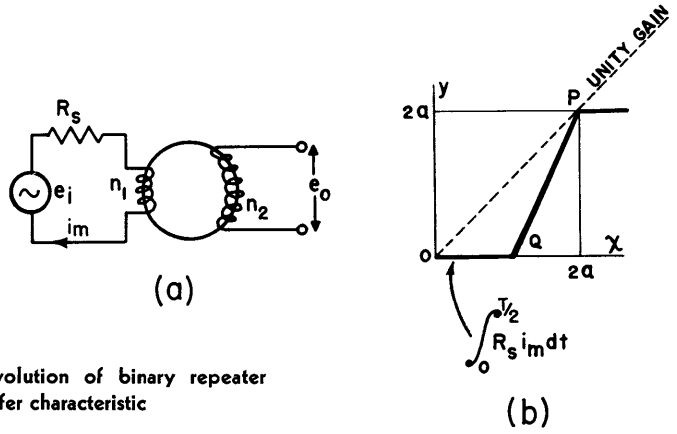
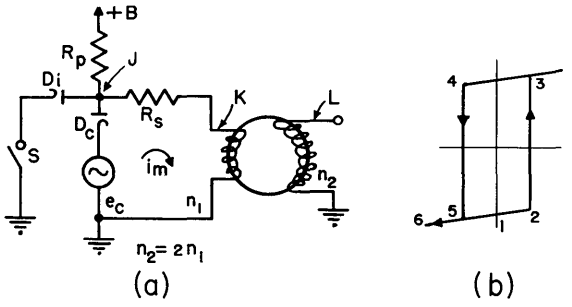
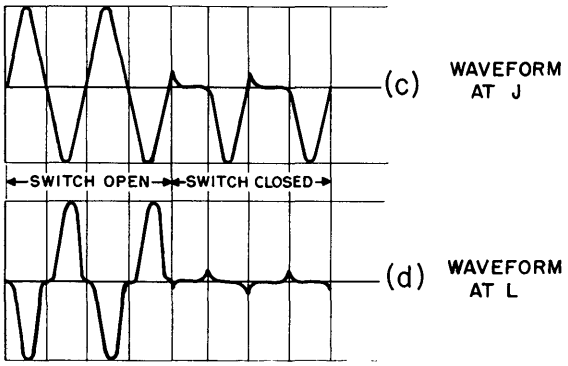
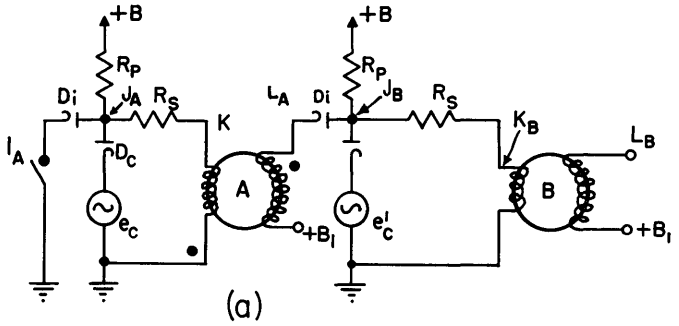


Fig. 2 (left). Evolution of binary repeater transfer characteristic

Fig. 4 (above). Nonlinear magnetic repeater having tolerance to zeros







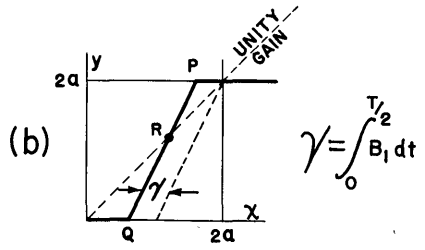


Fig. 5 (left). Nonlinear magnetic repeater modified to allow introduction of signals by means of a switch

Fig. 6 (above). (a) Manner of connecting two repeater stages in cascade. (b) How presence of B_1 alters stage transfer-characteristic to give tolerance to ones

small, positive bias B_1 has been added to the circuit. B_1 is in the reverse sense with respect to the input diode D_i, and is of the order of one tenth the peak clock-voltage. The transformer introduces a polarity reversal as shown by the dots. To understand how binary signals are received by stage B from stage A, it is necessary to consider the impedance to ground looking to the left from point J_B. With switch S closed, so that *zeros* are transmitted, the output winding of A generates little or no electromotive force (emf), and its inductance is very low as a result of the saturated state of the core. Therefore, on the receive half-cycle of stage B, its input diode D_i conducts strongly, clamping J_B to the level $+B_1$. The impedance to ground seen by J_B therefore is low, being the sum of the forward resistance of D_i, the saturation inductance of the output winding of transformer A, and the internal impedance of B_1. During the transmit half-cycle, the cathode of D_i remains at the $+B_1$ level, but its anode is carried negatively by the clock so that D_i opens and presents a very high resistance to J_B. Parenthetically, it is important to observe at this point that D_i prevents the backward transmission of signals from B to A, for in order to reset core A to the *one* state, a negative signal must be applied to its secondary. This is prevented by the polarity of D_i. With switch S open, A transmits *ones*. That is to say, the wave form generated by its secondary at the point L_A very nearly matches, in shape and amplitude, the wave form at J_B. As a result of the latter and the back-biasing effect of B_1, D_i, the input diode to stage B, has a high resistance during most of the receiving and transmitting half-cycles. The impedance seen looking to the left from the point J_B is then given by

$$Z_{J_B}=\frac{e_c}{i}=\frac{e_c}{\frac{e_c-e_o}{R_{Di}}}$$

$$=\frac{e_c}{e_c-e_o}R_{Di}$$

where e_o is the amplitude of the output emf from stage A, and R_{Di} is the resistance of the diode. Because e_c and e_o are very nearly equal, $e_c/(e_c-e_o)$ is much greater than unity. This makes $Z_{J_B}>>R_{Di}$ which adequately fulfills the condition for the transmission of *ones*.

The final step in the evolution of the transfer characteristic of the binary repeater stage was accomplished by the addition of the positive bias B_1. In Fig. 6(b) the portion PQ of the characteristic has been translated an amount γ to the left of its former position by the presence of B_1. γ represents the tolerance to *ones* obtained and is given by

$$\gamma=\int_0^{T/2} B_1 dt$$

The over-all transfer characteristics for one, two, four, and an infinite number of identical cascaded stages are shown in Fig. 7. The portion PQ is linear with a slope equal to 2^N where N is the number of stages in the cascade. It is seen that four stages have a characteristic which is very nearly that of the ideal, $N=\infty$. The ideal characteristic gives maximum tolerance to *ones* and *zeros*, and therefore has maximum stability. In a closed cascade or register of these stages, stability increases with the number of stages in the loop. The signal regenerating property of the stage is strong also because of the low impedance looking from J_B through D_c to the clock. This tends to provide reshaping or "reclocking" of the input signal.

In Fig. 8 the final improvement in the repeater stage takes the form of a high-

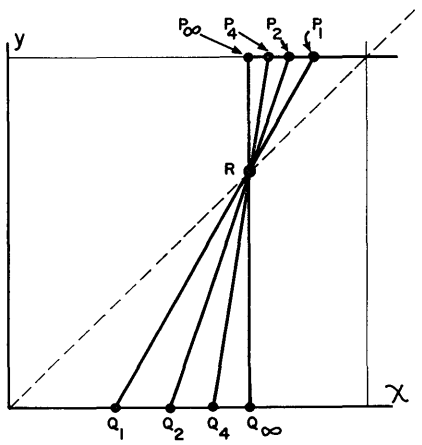


Fig. 7. Over-all transfer characteristic for one, two, four, and an infinite number of stages

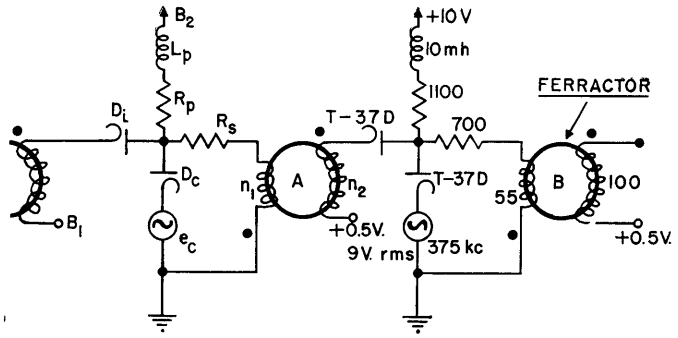


Fig. 8 (top left). Repeater stages in final form showing values of components when a Ferractor is used as saturable transformer

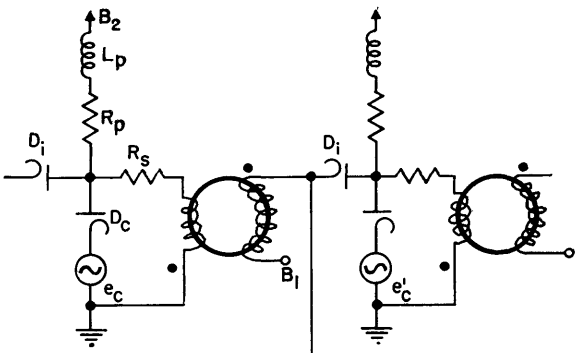


Fig. 9 (right). Manner of connecting a stage to transmit to several others

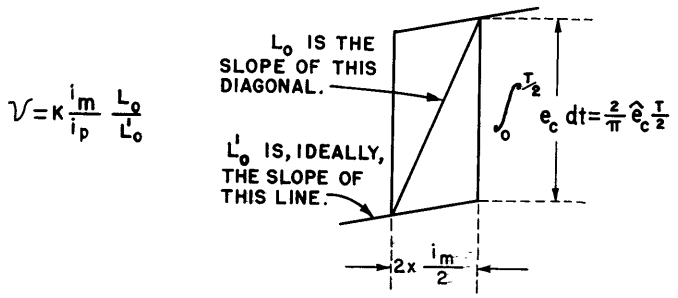


Fig. 10 (left). Factors which determine ν, the logical amplifying power of a stage

reactance (at clock frequency) choke in the constant-current pull-up branch. The use of the choke L_p permits low values of B_2 and R_p, greatly reducing the waste of d-c power in R_p. The voltages and component values shown have been used successfully with a Remington-Rand Ferractor having the type 101 core with about 20 wraps of stressed *4-79* Mo Permalloy $^1/_8$-mil ribbon. The allowable peak back voltage of the National Union *T-37D* diodes used was 12 to 15 volts. This, together with the maximum flux-turn figure of the Ferractor, limited the clock frequency to 375 kc. Maximum d-c power consumed per stage was approximately 0.1 watt, a-c power was 0.17 watt, giving a total of 0.27 watt per stage. A summary of important features which characterize the operation of the magnetic binary repeater stage follows:

1. The magnetic element acts in two ways: as a voltage transformer, and as a saturated reactor.
2. Clock and bias currents are not widely different for *ones* and *zeros*.
3. The magnitudes of the currents in diodes and resistors are independent of the logical load.
4. Only one diode per core which does not perform a logical function is required.
5. Reverse transmission is prevented by the stage input diode.
6. An impedance-multiplying effect results from the matching of the clock wave form and the stage output winding in the transmission of *ones*.
7. Signal reshaping or "reclocking" is provided by the low impedance of the clock branch of the circuit.
8. All power is provided by low-voltage, low-impedance, ground-referenced sources.
9. Operating power is low.

Amplifier Gain Considerations

Fig. 9 shows a repeater stage connected to transmit to three other stage simultaneously. In the case of *ones* very little current flows in the output winding of the transmitting stage. In the case of *zeros* the sum of the pull-up currents i_p of all the receiving stages passes through this winding. If its saturation inductance were zero, there would be no limit to the number of stages which could be connected to it to receive its signal. However, because this inductance is finite in any real case, a counter emf is generated across it at the moment the pull-up currents are transferred to it. If the voltage-time integral of this counter emf becomes too large, a false *one* will be transmitted. The largest number of similar stages which can be properly driven by a stage is called its logical amplifying power. The logical amplifying power of the stage in Fig. 8 employing the Ferractor has been found experimentally to be in the neighborhood of 6 to 8. The following equation for the logical amplifying power ν has been worked out as

$$\nu = K \frac{i_m}{i_p} \frac{L_o}{L_o'}$$

where K is the ratio of the largest permissible voltage-time integral of the counter-emf to the voltage-time area under a half-clock cycle; i_m is the primary magnetizing current of the transformer; i_p is the pull-up current; L_o is the maximum unsaturated inductance of the transformer secondary, defined as the ratio of the clock half-cycle voltage-time area to twice the secondary magnetizing current (the slope of the diagonal of the secondary volt-second current hysteresis loop); and L_o' is the saturation inductance of the secondary; see Fig. 10. Experiments with stages using *S-3* ferrite memory cores for the transformers indicated only a value of 2 for ν at 200 kc. The ratio L_o/L_o' for this ferrite was much lower than that of the Ferractor.

A Register of Ferrite Stages

Fig. 11 shows a 6-stage circulating register using ferrite memory cores. Points *I*1 and *L*6 are connected, and *ones* are inserted at stage 5 through diode gating by discharging the 0.1-microfarad capacitor through the 50-ohm resistor. The register is cleared by momentarily short-circuiting any input to B_1. Fig. 12(a) shows the pattern at the point J of one of the stages, and Fig. 12(b) shows the wave form at the output (point L) with three *ones*, two *ones*, and a single *one* circulating in the register. Operational tolerances for stable operation of this register are at least $\pm 20\%$ for B_1; $\pm 20\%$ for B_2; $\pm 25\%$ for e_c; -50% $+100\%$ for f_c; $\pm 5\%$ for R_s; and $\pm 50\%$ for R_p. Fig. 13 shows an input to a stage through two levels of diode gating.

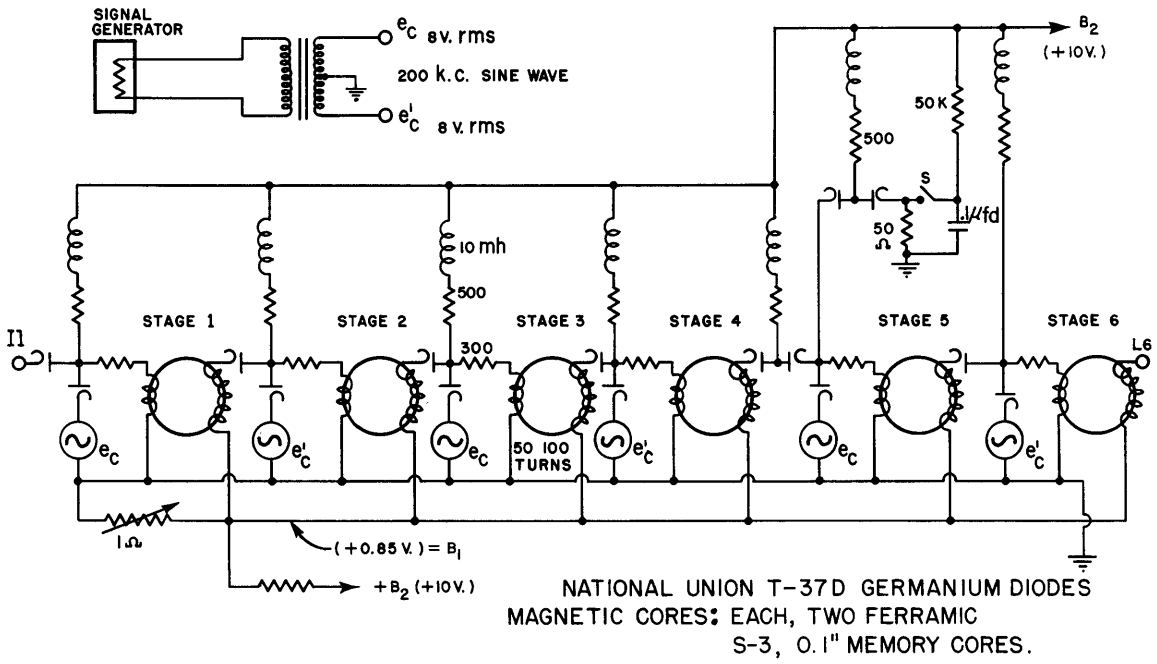


Fig. 11. Six-stage ferrite-core register with diode gating

A 2-Stage Complementer

Fig. 14(a) shows a complementer for obtaining the "not" function. It requires two stages. Therefore there is a delay of an extra half-cycle through the complementer.

An understanding of the operation of the complementer hinges around the behavior of the point P; see Fig. 14(b). Stage B is continually provided with a transmit pulse by clock Y through R_s', but its receive or reset pulse must come from the point P. When stage A transmits *zeros*, its output winding is very nearly a short circuit. Therefore, on its positive excursion, clock X carries P along with it because of the low impedance of the output winding and diode M. Diode N is open during this interval. Current from X resets core B through series resistor R_s. Negligible current passes throush R_s' because of the positive excursion of clock Y which is in phase with X. On the negative or transmit half-cycle for core B, diode N clamps P at the level $+B_1$, and M opens. It is seen that a reset pulse is provided for B when A transmits *zeros;* therefore, B transmits *ones*. Conversely, when A transmits *ones*, it generates an emf which just opposes that of the clock X. During this time, as a result of the positive bias given to the winding by $+B_1$, diode M remains open, and P remains clamped at the $+B_1$ level. Therefore, because no reset pulse is available to core B, it transmits *zeros*. The cores in both stages operate under the same conditions and in the same manner as in the simple repeater stage.

Fig. 15(a) shows, at the top, *zeros* introduced to the input of a complementer from a repeater stage and, at the bottom, *ones* being introduced. Fig. 15(b) shows, at the top, the wave form at P for *zeros* at the input and, below, the wave form for *ones* introduced. Fig. 16(a) shows, at the top, the *ones* transmitted by the complementer to a following stage and, below, the *zeros*. The peak amplitude of the *ones* was 10 volts and the clock frequency was

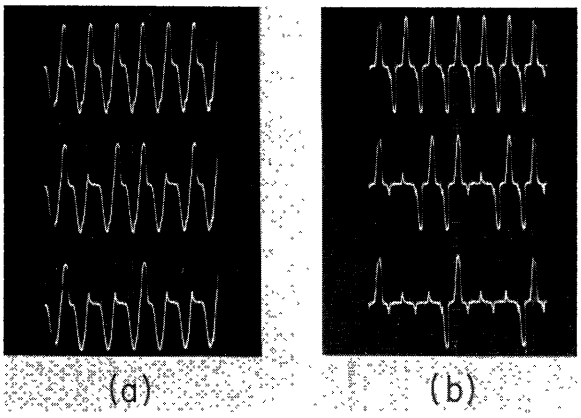


Fig. 12 (above). Wave forms of binary digits stored in ferrite-core register

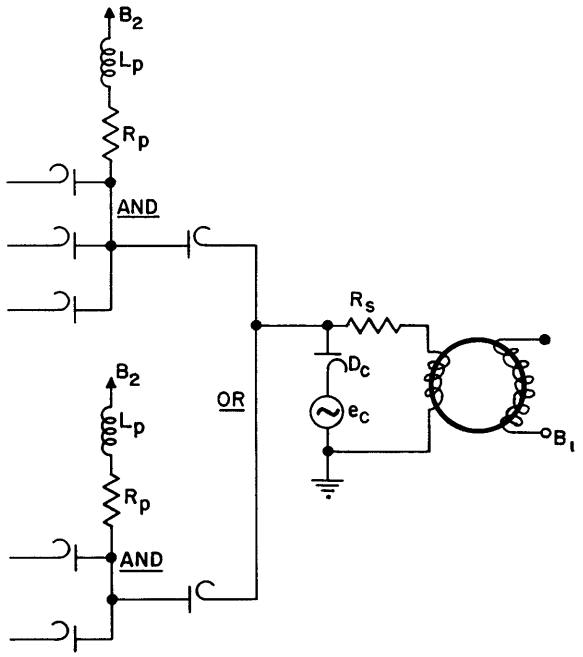


Fig. 13 (right). Stage input modified to provide two levels of diode gating

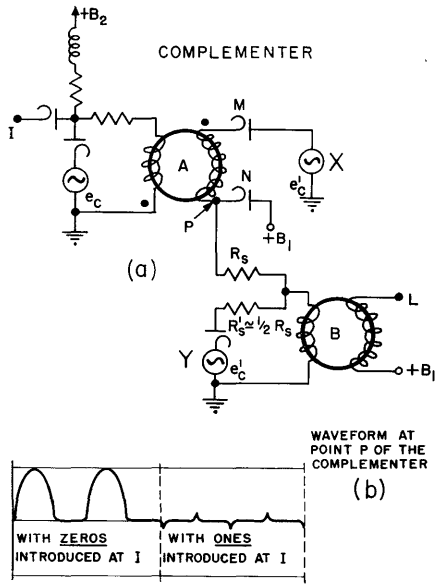


Fig. 14. (a) Two-stage complementer. (b) Wave form at point P of complementer

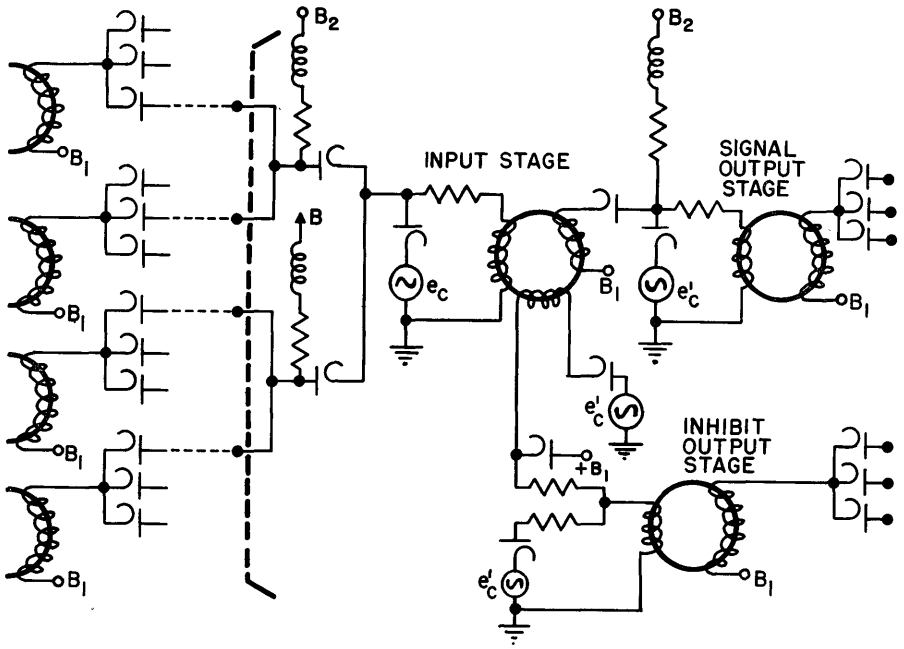


Fig. 17. Possible design for a magnetic logical package

250 kc. Ferrite core stages were used Fig. 16(b) shows two patterns obtained when two stages of the 6-core register were rewired to form a complementer.

Amplifying Power of a Cascade of Stages

The logical amplifying power of a repeater stage depends upon, among other things, the reactance of the transformer output winding. The most obvious way of reducing this is to reduce the number of turns. For example, if the clock amplitude and frequency are to be kept the same, the number of turns in the winding can be reduced by a certain factor if the core cross-sectional area is increased by the same factor. In this way the inductance, and therefore the impedance, of the winding will be reduced by the same factor that the turns were reduced, but the number of turns in the primary winding must also be reduced in this ratio. Therefore i_m, the magnetizing current of the primary is increased by the same factor that the output inductance is reduced. It is seen that no increase in the logical amplifying power of single-stage repeaters, which must drive similar repeaters, can be accomplished merely by reducing the turns in the windings. Although the impedance of the output winding is lowered, the current which it must handle to drive the same number of similar stages is increased in the same ratio. However, it is possible to obtain an increase in gain by the use of repeaters made up of cascaded stages, if one is willing to accept the additional time delay.

The design of such a repeater results from the following reasoning. If a given stage, call it type 1, is capable of driving ν stages like itself, then it is capable of driving a single stage, call it type 2, which has an input magnetizing current ν times that of the type 1, and an output impedance $1/\nu$ times that of the type 1. Such a stage is easily constructed by reducing the number of turns in each winding by $1/\nu$ and increasing the core cross-section as just described. Now if it is assumed that the type 2 stage can drive ν other type 2 stages, then it can drive ν^2 type 1 stages. Therefore the logical amplifying power of a repeater composed of a type 1 stage and a type 2 stage in cascade is ν^2. In general, if the repeater is built of n stages designed and cascaded in this manner, its logical

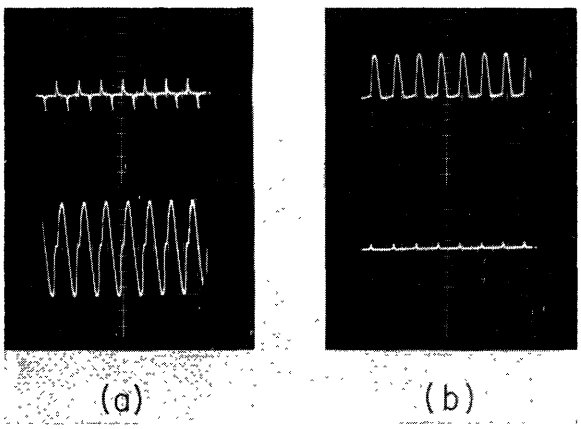


Fig. 15. (a) Top: Zeros entering the complementer; Bottom: Ones entering the complementer. (b) Wave forms at P for (at top) zeros in; (at bottom) ones in

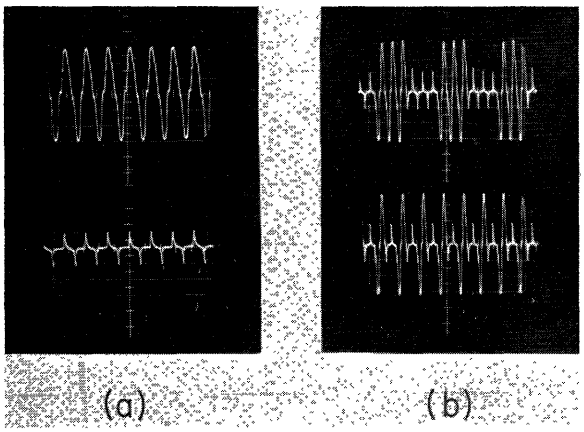


Fig. 16. (a) At top, ones leaving complementer; below, zeros leaving complementer. (b) Two patterns obtained when two stages of 6-core ferrite register were rewired to form a complementer

gain will be equal to ν^n. The delay through this repeater will be $n/2$ clock cycles.

A Proposed Type of Magnetic Logical Package

Fig. 17 shows a proposed type of magnetic repeater making use of cascading for increased amplifying power, and incorporating a complementer for inhibiting. A complete logical package is shown to the right of the dotted line. It consists of portions of and-gates followed by an or-gate, an input repeater stage, and two output stages in cascade with it. The upper stage provides an amplified signal output. The lower stage provides an amplified inhibit output. The and-gate diodes are directly associated with the outputs of the package rather than with the inputs, in order to place the package interconnecting lead capacitive load on the anode side of the input diodes rather than on the cathode side. During the transmission of *ones* the impedance from the cathode side to ground is considerably higher than that from the anode side to ground. This arrangement also ensures that the pull-up currents of the driven stages will not be combined in a single long lead. The inductance of such a lead could well exceed the saturation inductance of the stage output winding. There is a delay of one full clock cycle through the package.

References

1. Dynamic Circuit Techniques Used in SEAC and DYSEAC, **R. D. Elbourn, R. P. Witt.** *Proceedings*, Institute of Radio Engineers, New York, N. Y., vol. 41, no. 10, Oct. 1953.

2. The Single-Core Magnetic Amplifier as a Computer Element, **R. A. Ramey.** *AIEE Transactions*, vol. 71, pt. I, 1952 (Jan. 1953 section), pp. 442–46.

3. Proceedings of the Eastern Joint Computer Conference, *AIEE Special Publication T-70.* "Performance of TRADIC Transistor Digital Computer," **J. H. Felker,** April 1954, pp 46–48.

4. Magnetic Logic Circuits for Industrial Control Systems, **W. G. Evans, W. G. Hall, R. I. Van Nice.** *AIEE Transactions*, pt. II, July 1956, pp. 166–71.

High-Speed Transistor Computer Circuit Design

R. A. HENLE

THE REALIZATION of the computer described by S. W. Dunwell[1] calls for high-frequency circuits capable of passing a signal through five sequential logical stages in 100 millimicroseconds. At the start of the project a study of available devices and techniques indicated that this goal would be difficult to reach without significant improvements either in the devices or the circuits, or both. Such an improvement came about in the device area with the availability of drift type transistors for research work. The characteristics of these transistors made necessary a new approach to circuit design which has resulted in circuits which not only meet the speed requirements, but also are relatively simple, reliable, and insensitive to noise.

Drift Transistor Characteristics

Typical electrical characteristics of drift transistors are shown in Table I. It can be noted that the transistor has a number of advantages and disadvantages when compared with other high frequency transistors. The major advantages are the following: 1. A very high frequency response: 200 to greater than 500 megacycles. 2. A high collector breakdown voltage: greater than 50 volts. 3. A low base restistance: less than 50 ohms.

These characteristics represent significant improvements in some of the switching parameters of transistors. The disadvantages of the transistor are a high collector saturation resistance: 50 to 150 ohms; and low reverse emitter breakdown: 0.5 to 5 volts.

The seriousness of the disadvantages depends to a large extent on the circuit design philosophy chosen. The collector saturation resistance becomes of major importance in saturating type circuits, and the low emitter breakdown voltage does not allow certain types of emitter-follower logical circuits to be used without modification. However, in some types of circuits, where it is desirable to limit the reverse bias on an emitter, this characteristic can be used to advantage. An example of this is an inverter circuit design such as is shown in Fig. 1. In the usual circuit of this type a diode is used to limit the reverse bias on the emitter junction, thereby reducing the circuit's turn-on delay. With drift transistors, the low emitter breakdown voltage can be used for this purpose, eliminating the need for the diode.

Additional information about the d-c and a-c parameters of the transistor is given in Fig. 2. This figure shows the collector V–I plot of a p-n-p unit. Also plotted are contours of constant cut-off frequency and constant collector capacitance. It will be noted that the contours of constant frequency response take on roughly the form of hyperbolas with frequency response decreasing as either the low current or the low voltage regions are approached. Collector capacitance decreases as the collector voltage becomes higher. As with other transistors, hole storage delays the response when the transistor is driven out of the collector saturation region. For fast operation one must either control the degree of saturation or stay out of the saturation region completely. It follows from these considerations that the most desirable operating region for this transistor lies in an area which avoids either low values of collector voltage or very low values of collector current.

The collector V–I plot of an n-p-n drift transistor is shown in Fig. 3. This transistor has electrical characteristics similar to those described for the p-n-p unit.

Fig. 4 shows the grounded-base transient response of a drift transistor at two values of collector voltage. The applied current input of 0 to 5 milliamperes is shown in 4(a); 4(b) shows the output wave form taken with a load resistance of 200 ohms and a supply voltage of $1^1/_2$ volts; and 4(c) is the output wave form into the same load with a collector supply voltage of 10 volts. (The minimum rise time of the oscilloscope was 7 millimicroseconds.) It will be noted that an appreciable improvement in response is obtained by operating at a higher collector voltage in the region of higher frequency response and lower collector ca-

R. A. Henle is with International Business Machines Corporation, Poughkeepsie, New York.

The work reported here represents the combined efforts of a number of people at the International Business Machines Corporation Research Center.

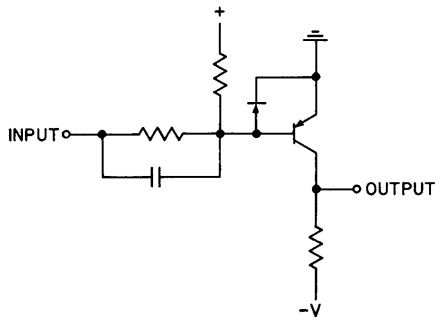


Fig. 1. Inverter designed for minimum turn on delay

pacitance. Only a very slight improvement in response has been noted in operating the transistor entirely class *A*, avoiding the very low collector current region.

Circuit Design

The need for very fast operation of circuits makes it imperative that careful consideration be given to all aspects of circuit design. One consideration is the signal voltage swing at the output of the circuit. As the speed of switching circuits becomes higher, the power consumption of the circuits must go up according to the equation:

$$\text{power consumption} = C\ V^2\ F$$

where C is the shunt load capacitance, V the signal voltage swing, and F the pulse repetition frequency. For high-speed circuits, then, the voltage swing should be as small as is consistent with reliable operation. It is apparent also that every attempt must be made to keep capacities low.

Since small voltage swings are desirable for high-speed operation, careful consideration must be given to the method of performing logic. Diodes, because of their small size and fast operation, warrant consideration as logical elements. Several problems are encountered, however, in their use in high-speed circuits. At low signal levels the voltage drop across the diode becomes an appreciable percentage of the voltage swing. For example, if one has diodes with a 0.3 volt forward drop and attempts to use voltage swings of 1.5 volts, the resulting level shifts of the signal through the diode represents 20 per cent of the usable signal swing. Also, relatively large currents must be used to switch diode logical circuits at millimicrosecond rates. This limits the number of logical stages that may be driven by one transistor.

Both of these disadvantages of diodes can be overcome by using transistors as logical elements. Transistors will switch completely on small signal swings, and the power gain of the transistor can be used to increase the parallel cascading factor of each stage.

The characteristics of drift transistors are such that the most favorable operation is found in a higher-voltage, higher-current region. It follows from this that the circuits will be nonsaturating. It has also been shown that the circuits must be capable of operating at a low signal voltage. An obvious requirement is that the circuits control the operating region of the transistor to keep it within its voltage and current rating.

To meet these requirements a philosophy of circuit design based on controlled current switching was investigated. In the past, most switching circuits have placed close tolerances on the voltage swings. This has proved an acceptable mode of design with both vacuum tubes and transistors. However, a current switch has some desirable features. Fig. 5 illustrates a current driver connected to a load, R_L, through a series inductance, a noise generator, and a resistance. The value of the current received at the load is not affected by these series elements. The voltage developed at the load is that required to pass the current I, while the voltage developed at the current generator may be many times higher. From this line of reasoning, it became evident that one could develop a set of switching circuits by using a transistor as a current generator driving other transistors. This system would be tolerant of noise and would require very low voltage swings. It is plain that shunt elements would deteriorate the operation of these circuits, and care would have to be taken to keep them to a minimum.

Table I. Drift Transistor Characteristics

f_{co}	200 → 500 megacycles
α_{cb}	20 → 80
I_{co}	2 → 10 microampere
R_{sat}	50 → 150 ohms
C_c	1 → 8 micromicrofarads
V_{cb}, max	> 50 volts
V_{eb}, min	> 0.5 volts
r_b'	< 50 ohms
Transit time delay	< 5 millimicroseconds

Circuits which satisfy the necessary conditions may be either a-c or d-c coupled. Both modes of operation have advantages and disadvantages, and it is difficult to prove conclusively that one is superior. Indeed, it could well be that the optimum system is a combination which incorporates the better features of each. In general, we have tended toward the d-c philosophy because of ease of servicing, avoidance of pulse transformers, and less critical timing relationships.

Circuits

A number of circuit schemes have been investigated which satisfy the requirements of operating on small signal swings, keeping the transistor out of saturation, allowing operation of the transistor in its most favorable operating region, and operation as a current switch. Fig. 6 shows a way in which transistors may be coupled together, by means of alternate n-p-n and p-n-p stages, without the use of interstage coupling networks. The voltage swing at the collector of the p-n-p stage need only be from $V+$

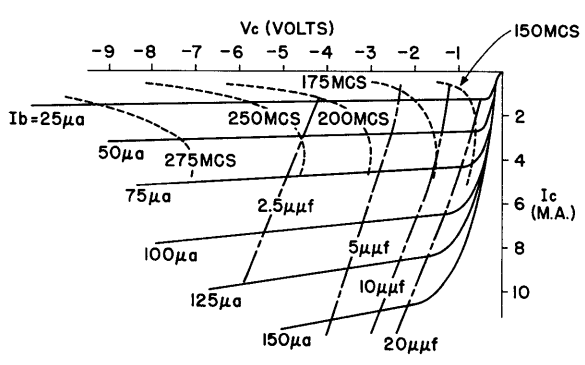


Fig. 2 (left). P-n-p collector V_c–I_c characteristic

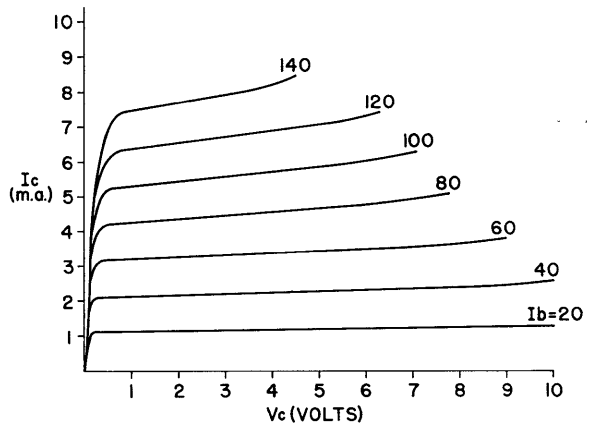


Fig. 3 (right). N-p-n collector V_c–I_c characteristic

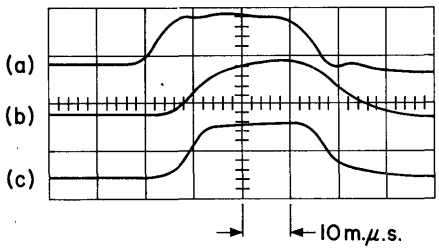


Fig. 4. Drift-transistor transient response

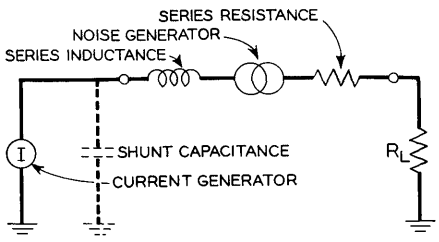


Fig. 5. Current generator driving a load

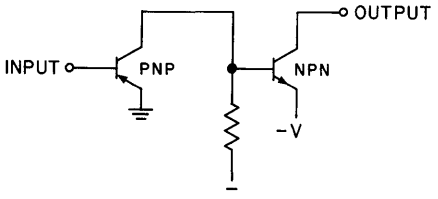


Fig. 6. Direct coupled p-n-p and n-p-n transistors

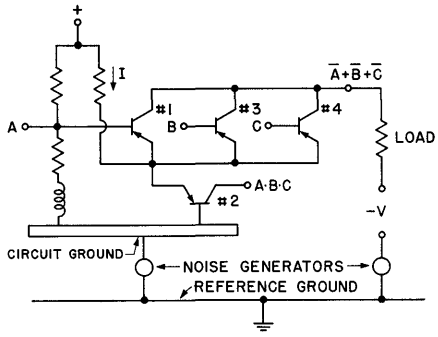


Fig. 7. Current-switching circuit

0.3 to $V-0.3$ volt to completely switch the n-p-n transistor. To limit power dissipation in the p-n-p transistor, it is necessary in some way to limit the collector current. A scheme for accomplishing this is shown in Fig. 7. Here the emitter current of transistors no. 1, no. 2, no. 3, and no. 4 is limited to I. If the inputs to A, B, and C are at an up level, transistor no. 2 conducts all of the current, I, and gives an output which is logically $A \cdot B \cdot C$. If one or more inputs to either A or B or C are at their down level, these transistors will conduct the current I and give an output which is logically $\bar{A}+\bar{B}+\bar{C}$.

It will be noted that $\bar{A}+\bar{B}+\bar{C}$ is the complement of $A \cdot B \cdot C$ and, in general, circuits of this type will generate both a given logical function and its complement. When a number of circuits are combined, logic is done on two voltage levels depending on whether an n-p-n or a p-n-p stage is being driven. The output of an n-p-n is used to drive p-n-p inputs and vice versa. Since any logical expression can be constructed with either type of input, complete freedom in constructing logical expressions is retained. This method of coupling allows us to choose the operating voltage of the collector on the basis of speed and power considerations. The circuits are non-saturating and the voltage swing need be no greater than that required to switch the transistor.

Fig. 7 is shown with several noise generators introduced into the circuits. With an input circuit such as is shown at input A to transistor no. 1 and the driving signal supplied from a current source, noise generators in the circuit do not affect either the bias on transistor no. 1 or the current supplied to the load.

Conclusions

Circuits of this type are one way of satisfying most of the requirements which were found desirable for high-speed switching. Results with circuits similar to these, using commercially available high frequency transistors, indicate that signal delays average about 16 millimicroseconds per logical stage. Loaded rise times are of the order of 20 millimicroseconds. Delays are cumulative when going through successive logical stages; rise times are not.

High-speed logical circuits, using drift transistors and current-switching techniques, show a great deal of promise. Drift transistors appear capable of operating reliably at speeds well above what was previously possible with economical vacuum tube circuitry.

Reference

1. Proceedings of the Eastern Joint Computer Conference. *AIEE Special Publication T-92*. "Design Objectives of the IBM Stretch Computer," **S. W. Dunwell**. April 1957, pp. 20–22.

Discussion

M. Cooper (Motoroia, Inc.): Are the transistors described in your talk commercially available, and if so, from whom?

Mr. Henle: These are not commercially available transistors. The transistors were made by the Component Research Group in the Poughkeepsie Laboratories.

N. Prywes (Remington Rand Univac): On which scope, and at what rise time was Fig. 4 taken?

Mr. Henle: Fig. 4 was taken from a Tektronix 517 oscilloscope. Feeding a signal directly into the plates of this oscilloscope, rise times have been measured, of unloaded circuits, of 2 to 3 millimicroseconds.

Mr. Chang (Sylvania Electric Products, Inc.): Is the transistor a p-n-i-p structure or n-p-i-n structure?

Mr. Henle: The transistor is a graded-base transistor with a drift field in the base and a very thin base region, both of which improve the transistor's transient response.

T. R. Finch (Bell Laboratories Incorporated): Is the design philosophy proposed weighted heavily by speed consideratins, reliability, or economy as compared to Dr. Angell's direct-coupled transistor logic proposal, as outlined in his paper

Mr. Henle: We feel that this technique has much of the simplicity of the direct-coupled transistor logic circuit approach, and probably represents a faster way of using the transistor because it is non-saturating and it does keep the transistor out of its most unfavorable operating regions.

Are Computers Important?

SIR ROBERT WATSON-WATT

THANK YOU Mr. Chairman, for your generous introduction which is clearly designed to ensure me, up to this moment, some measure of respect. You were too polite to suspect that what I really need is your sympathy: yesterday afternoon tea and sympathy (preferably from my dear friend, Deborah Kerr), and today luncheon and sympathy from E. J. C. C. It is a terrible thing to be the only confused person among 2,500 pellucid philosophers busily propogating their electric poetry through electric plumbing.

Yesterday, my wandering ions of thought were deflected towards that Dark Age which preceded the Electronic Age; that Dark Age when we did not have the sense to know how happy we were. Then, the first electrons were just being deflected from their straight and narrow path in the first cathode-ray tube, while my schoolboy steps were being deflected from the goal of the higher journalism, through a brief encounter with heavy electrical engineering, towards becoming "Assistant to the Professor of Natural Philosophy." At a neighboring university a distinguished professor of natural history had just set an essay subject to his students. They were to write about "The Petrel," a bird which he failed to identify unambiguously by its hackneyed prefix "stormy." You will be aware that in Great Britain, that citadel of colonialism (of the old-fashioned, simple-minded, well-intentioned colonialism), the barbarous natives call gasoline by a name of six letters beginning with p and ending with l. So an earnest student turned in an essay on "Petrol," which, of course, has only very recently acquired the same prefix "stormy." The professor made only one annotation, it was "Hail to thee, blithe spirit!—Bird thou never wert."

I listened yesterday to the fascinating talk about the 50%, 80%, and 90% points on the curve of delivery dates, in its asymptotic approach to Orwell's 1984; it took no great *Stretch* to deflect my thoughts from one "Ode to a *Larc* in the Sky" to this other "Ode to a Skylark." And this in turn made me think that it was very desirable that the philosophers should, in their poetic plumbing, not neglect philology. Which brings me to the logical and delay circuits which lie beween me and a YES-NO decision on my selected problem, "Are Computers Important?"

There are two classes of people who are accused of taking cover behind the phrase "It depends what you mean by X." On the one hand are the serried ranks of the escapists, whose other refuge is "Don't fence me in." I hasten to add that I am not consciously throwing stones at the glass house which overlooks the eastern reaches of Forty-second Street, as it overlooks so much else. I am, in fact, looking towards the other class, the constructive philosophers. In saying "It depends what you mean by X," they are declaring war on the escapists, with their shrugged sholders and flabby hand-wave "Oh, that, that is just Semantics!"

What I believe this serious computer conference now needs is a good stiff dose of semantics, till it hurts! If, in asking "Are computers important?" I mean by "computers" merely ingenious and elegant means for doing sums quickly, my answer is a firm "No." And if you ask "What do you mean by 'No'?" I reply that I mean the same color of "No" as I would use in answering a question, put to myself, "Are you important?" I mean that the subject or object under discussion may have interesting individual qualities and potentialities, but that these remain of merely abstract interest, and ("with a little bit of luck" if I may quote from "My Fair Lady") aesthetically satisfying, unless they are consciously and actively matched and embodied into a more comprehensive system or organization. That system or organization must be planned to satisfy a closely studied, carefully ascertained, and unambiguously specified group of operational requirements. If a computer is merely an instrument, it is a pretty toy, not insignificant, but, in the main, impotent.

If, on the other hand, what I mean by "Computer" is such an assemblage, ensemble, system, organization as I have tried to define obliquely by the purpose it is to serve, the operational requirement it is to meet, then the answer to my question is an almost terrifyingly universal "Yes." By the time when the fiftieth birthday of the electronic computer (whenever that may be and whatever it may be) comes to be celebrated, the question of whether it is etymologically and semantically justifiable to call that anniversary a "Jubilee" will have been answered, with much joy, and with much sadness, in proportions which we are in part determining in these three days of co-operative thinking. No member of this nation will by then be immune from some share of the joy, and of the sorrow.

Our year-end review of the inspirations of 1955 and earlier, of the bread-boards and prototypes of 1956, of the production models of 1957 and later, is bringing to mid-stage two major, and a multitude of more than minor, sets of achievements. The big two are, first, the release from building on a foundation of vacuum, and, second, the advent of a capacious memory. The solid-state computer is now with us; the liquid-state computer (if I may be permitted that frivolous offence against semantics) is peeping tantalizingly from the wings. The transistor is now a relatively solid citizen; magnetic cores, ferractors, show up in increasingly varied roles; and it would be an unwise man who would underestimate the practical or the poetic importance of that beautiful new baby to which Mr. Slade stood godfather this morning, the cryotron. I shall not forget the memories, but first I would like to ask for a mental preview of generalized "printed circuits," printed cores, perhaps printed transistors, possibly printed circuits of multiple cores and multiple transistors; perhaps even of other printed honeycombs, to be found along the paths which have just been opened.

We have already the assurance of an immediate forward jump in speed, compactness, durability, cheapness. In particular, all these three last-mentioned qualities improve much more than linearly with the reduction in the complexity of the individual component and its "fuel." As for speed, we are well on the way to avoiding, among other defects, the sluggish transport or our vital pulses over the relatively long, unplanned, delay-lines which are necessary for connecting together our conventional, but obsolescent, bulky components.

Serviceability has taken a correspondingly big forward leap, but this does not discharge us from the need for removing all possible excuses for the neglect of easy preventive maintenance. This means that, more than before, we must lay great stress on accessibility and easy replacement, even though this latter

Full text of the luncheon address presented at the Eastern Joint Computer Conference, New York, N. Y., December 11, 1957.

SIR ROBERT WATSON-WATT is President of Adalia Ltd., and Adalia Computations Ltd., Montreal, Canada.

will be required less frequently than before.

We have gained a factor of ten or a hundred times in internal speed, but over the greater part of our field of application this merely accentuates the already great mismatch between the intrinsic speed of the computer, in the narrow sense, and of the input-output devices without which it is a computer only in the abstract.

No less remarkable than those at which I have thus superficially glanced are the advances in very high-speed, short access-time, large-capacity memories. Indeed I am not sure that 1956 will not be remembered primarily as the year of memories. I may have nostalgic regrets, from my 45 years of affectionate intimacy with cathode-ray tubes, that the magnetic core has killed (by superior speed and superior reliability) the electrostatic storage tube with which my colleague of 20 years ago, F. C. Williams, revolutionized the storage problem of 10 years ago. I have fewer regrets that the core should have killed also the metallic planned-delay line. Both these casualties began life as products from a common stem, the radar laboratories, from which electronic computers in general grew as another and rich main crop.

If my first *bête noir* in the semantics of our somewhat loose vocabulary is an adjectivally nude "computer," my biggest black beast is that deformed and shapeless (if that be semantically possible!) monster the random-access memory. You may well remind me that the alleged and ageing entity into which I have just been dipping is, indeed and alas, a random-access memory. But that is just the point of my hostility. That kind of random-access memory may be interesting enough, but its irritation value is a steeply rising non-linear function of its randomness. Nobody really wants a random-access memory; what he really wants when he asks for a random-access memory is usually a large-capacity storage system with a high access rate and a small access delay-time, the latter differing in many cases by an order of magnitude or more from a direct reciprocal of the former. When he asks for a random-access memory, the client usually wants to have whatever may be the converse of a serial-access memory. Physically the answer has reduced to a very rapid-access (and still, most frequently, a serial-access) device, but philosophically, in the end it need not, and practically it should not, do so.

I have no semantic "Beauty" to oppose to my semantic "Beast." Beauties are by definition set apart from random access. But as something to live with meanwhile, I suggest the poor but honest, if unbeautiful term "Parallel partial-identifier search," to describe the beautiful operation which the client seeks to have at his disposal. Up to date we have offered him rather poor half-measures, wasteful use of storage accommodation, cumbersome directory look-up, statistical condensations, and so on. It may be that tomorrow Mr. Slade will be uncovering for us the first practical satisfaction of an ideal which in common with others my colleagues have sought for several years now. He is promising us a "system which is interrogated by comparing a new word with the entire catalog (by which I assume he means 'with each word in the entire catalog') simultaneously." We are, in any case to have some half-dozen new devices for multiple parallel search described to us in the appropriate session.

But why, apart from this problem of the internal composition of our computer system, do we submit quietly to the prospect of going about the world festooned with miles of paper tape or loaded with stacks of stiff paper rectangles counted in megacards? There is basically one reason for cards, that they are not inconvenient for manual use. There is basically only one reason for filing, to wit, subsequent retrieval. It is a semantic danger to concentrate on the passive and limited concept "file" when what we really want is assured timely individual retrieval by selection, preferably by parallel interrogation of the system's "memory." Joanna West's culinary injunction "First cage your hare, then cook it" still holds, but we can cage it more elegantly than by tying it up with tape or by enveloping it in cardboard. All she prescribes in essence is "First find your entry, then read it"; the finding is a mere accessory, a regrettable preliminary, to the essential reading. The bibliographer, the lawyer, the librarian, are among the hosts of impatient clients who are clamouring for a system which gives them not exact coincidence (which would deny them the compilation of relevant, related but not identical references), but partial coincidence, entries with a key-part in common but containing supplementary, non-coincident data which are the "literature" of the specific "subject" which is used as an identifier.

All this talk is a preamble to a charity appeal. I am begging for a still better co-operative effort than has yet been made, to build up an accepted glossary of terms into which the specification of the potentials users' problems can be dissected. This is quite other than the "common machine language" towards which we should also be working. It is not merely quite other, it is vastly more difficult because it is vastly more diverse and disparate. It is so for the same reasons that make me treat the "computer" *per se* as relatively unimportant, the input-output and storage devices which must be gathered round the computer-kernel as being extremely important, and embarrassingly less tractable.

Any mathematician in the civilized, or in the uncivilized world, (I need not remind you that Russians are good at mathematics) can debate with any other mathematician in a common language. Until we can achieve the corresponding result at the aesthetically lower economically higher level of the office, the store and the production plant, we shall be shackled against our efforts to do, in the way he wants, the things that your client wants.

I have one other, but a brief, appeal. Two weeks ago I spoke, in this city at a luncheon not dissimilar to this one, under the subtitle Matching the Machine to the Man. I was dealing with cases where there had been no time in which to match the man to the machine. But if the big scale deliveries are indeed to come in 1960 and after, we have at least some time in the high schools, the colleges, in the offices and in the plants, to do something towards matching the man and the woman to the machine. In the end we shall all benefit by the introduction of "Automation," but only if we plan and act now can we save grave hardships for some of the displaced persons of the second Industrial Revolution.

Automatic Input for Business Data-Processing Systems

K. R. ELDREDGE F. J. KAMPHOEFNER P. H. WENDT

Synopsis: Computers for business applications are generally input limited and require excessive manpower for data preparation. This can be reduced, and gains can be made in speed and reliability if the data forms for the computer and the human being are compatible. Documents must be prepared for manual use in conjunction with many phases of automatic business or technical data handling, and such documents with suitable format arrangements can be fed directly to the computer input with the techniques described. The numbers and symbols on the document are printed in magnetic ink in conventional form and size, and machine reading can be accomplished at rates exceeding 5,000 characters per second. The documents themselves have been handled at rates up to 50 per second.

IT would be difficult to define the limits of application of computers to the problems encountered in business operations. It can be stated, however, that one of the most important fields of application lies in control of business transactions. Up to a comparatively short time ago such control was achieved largely by manually produced documents, which necessitates a great deal of clerical effort. Lately, the trend to use computers to perform the chores of preparing payrolls, inventories, and gathering statistical data of many types has reduced the cost and manpower required to perform some of these necessary tasks.

One of the difficulties which has seriously limited the application of computers to business problems lies in the fact that information in human language, such as is found on business documents, can not be fed to the computer without translation into the machine language of the computer. Generally, a considerable amount of manual transcription is required to process the data before it can be fed into the computer. This can be reduced, and gains made in speed and reliability if the data forms for the computer and human being are compatible. The techniques developed at the Stanford Research Institute permit the entry of information into a computer directly from business documents in the form of conventional numbers and symbols printed in magnetic ink. Machine reading can be accomplished at rates exceeding 5,000 characters per second, and the paper documents themselves have been handled at rates exceeding 50 per second.

Most of the work in these techniques has been aimed at developing a check handling system for banks, but the same techniques are readily adaptable to other business applications such as charge tickets, payroll systems, and cost accounting of all types.

Work on the computer input system which has been developed may be conveniently divided into three categories. The first consists of the development of the techniques for the reliable machine reading of characters and symbols printed in magnetic ink. The second is the development of a series of magnetic inks suitable for character reading, and at the same time compatible with a wide range of printing methods and practices. The third category is in the area of development of electromechanical machinery which is capable of reliably handling individual pieces of paper of varying sizes, weights, and degrees of mutilation.

Stanford Research Institute Character Reading System

In the Stanford Research Institute character reading system the questions relating to magnetic ink printing, to document handling, and to electronic decoding circuitry, are all grouped into a single problem, since variations arising in any one of the areas affect the other two areas. It is recognized for instance that magnetic ink printing has to be adaptable to most of the current techniques for imprinting on paper, but in order to keep the electronics reasonably simple, certain minimal demands are put on printing in order to maintain adequate machine reading quality. On the other hand, the electronics are designed to handle a wide range of registration tolerance in both printing and document handling, so that there is a considerable relaxation of these tolerances for the printing and paper handling machinery. To further relax the tolerances in both printing and electronics, it was decided to use a degree of styling in the design of the characters such that the wave forms would be more distinct for the machine, but which would not prejudice reading by eye. Throughout the whole of this magnetic character reading system, limited compromises have been made which go far to reduce the cost and to increase the reliability of the equipment.

Character Reading

Character reading, properly speaking, begins at the magnetic read head that is in contact with the paper upon which the magnetic characters are printed. The quality of signal derived, in turn, depends on the quality of the printing, but for the purpose of discussing character reading it will be assumed that the signals are adequate.

The magnetic read head used for this type of character reading is conventional in style. The air gap of the read head is positioned at right angles to the line of the paper carrying numbers, and in general the numbers are read from right to left. The length of the air gap must be at least equal to the height of the numbers, and in addition has some greater length depending upon how much space is left for registration tolerance. Heads having more than 1 inch of gap length have been used. Read head inductance is matched to the frequency and impedance requirements for the amplifier input.

In Fig. 1 is shown a simplified block diagram of the electronic reader. The input signals are generated by first passing the magnetic characters through the field of a permanent magnet, such that the polarization is from left to right across the numbers. The output signal from the read head then corresponds in a first approximation, to the differentiation of the plane area of the number as it passes under the read head. The signals are rather small at this point, only in the neighborhood of 200-microvolts peak. This is occasioned by the fact that the layers of printed ink are quite thin, in the neighborhood of 0.0001 inch thick, and consequently, contain very little magnetic oxide.

The signal has a wave form appropriate to the character involved, but up to the present time it has been found that the very high frequencies are less reliable as far as the decode characteristics are con-

K. R. ELDREDGE, F. J. KAMPHOEFNER, and P. H. WENDT are with the Stanford Research Institute, Menlo Park, Calif.

The work described in this report was done under contract for the Bank of America, NTSA, and subsequently continued for the General Electric Company, Industrial Computer Department.

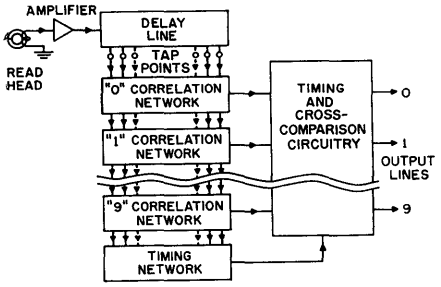


Fig. 1. Simplified block diagram electronic reader

cerned, whereas the lower frequencies are much more reliable. During the process of amplification then, the signals are filtered such that the maximum wave length acceptable from the number is of the order of one sixth of the width of the number. The amplification is such that the signals have a median peak level in the order of 50 volts. The signals in actuality may be materially greater or materially less than this value. If printing is light the signal level may be only one fifth that from characters which are printed heavily. Consequently, the whole of the electronic system has been devised to take care of this order of level shift.

The amplified signals are fed into a lumped constant delay line. At a paper speed of 150 inches per second and with characters printed at 8 to the inch, character rate is 1,200 characters per second. The delay line would be just longer than one character, and consequently have a delay time of approximately 800 microseconds. For 5,000 characters per second the delay time is correspondingly shorter or about 190 microseconds. In the presently used equipment, the delay line has essentially zero attenuation and linear phase shift within the band width of the information used. In addition, the delay line is provided with 18 taps along its length. The number 18 tap provides a 50% safety factor in the number that sample theory predicts to be required to completely redefine the wave form within the band width selected.

From the delay line onward the circuitry is divided into a number of channels equal to that of the number of characters to be decoded. At the head of each channel there is a correlation network from which auto- and cross-correlation voltages are derived for each character as it is sent through the delay line.

Each correlation network is computed on the basis of the expected wave form for its corresponding number, and if the wave form from that number is passed through the delay line this particular correlation network will have a higher output than any other correlation network at the time that particular wave form is properly stationed within the delay line. All of the remaining correlation networks will have lesser outputs, and recognition is premised on the basis of the maximum voltage.

To distinguish between the channel carrying the maximum output and those carrying lesser outputs, differential detectors are used. The differential detectors are high gain difference amplifiers in which one side carries the channel voltage and the other side carries a reference voltage. This reference voltage is derived from a diode mixer associated with all channels, and which reaches the maximum voltage carried by any channel.

In addition to the character channels, there is an additional timing or "character-presence" channel. This character presence channel is composed of a network which is so disposed that it produces an output at the time when about one third of the character has passed. This output is dependent entirely on the shape of the first portion of the character, and is independent of the amplitude of the character. Stray noise and fuzzy edges of the character play little part in affecting the decisions of the character presence circuitry.

The output of the character presence circuitry is appropriately delayed until the character wave form is stationed in the delay line in the design position. The design position is that for which the correlation networks were computed. At that time instant a gate pulse is briefly applied to the differential detector circuitry, and the character channel output lines each carry a positive or a negative pulse depending upon the state of the several differential detectors.

In the normal case only one channel is positive and the remainder of the channels are negative. Because the system is based on probability for recognition it is possible that two or more of the channels may become positive during the recognition interval. Such multiple recognition activates reject circuitry.

The use of probability in this system makes it possible to exert a control over the error-reject ratio in the results. In this case errors are spoken of as being faults which the machine does not know it makes; whereas, rejects are faults which the machine recognizes it has made. The distinction between these two is important because the unknown fault is carried along with the good material; whereas, the rejected fault can be placed aside for manual intervention. In the discussion

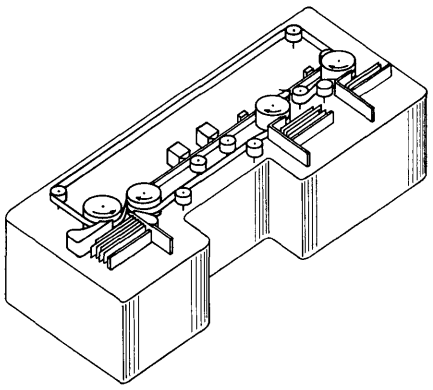


Fig. 2. Document feeder

of the differential detector circuitry above it was mentioned that the reference line carried the maximum voltage of any of the character channels. Control over the error-reject ratio may be exerted by controlling the fraction of the maximum voltage which is applied to the reference lines of the differential detector circuitry. For instance, if 100% of the value of maximum voltage is supplied to the reference line then in all cases the most probable number will be accepted. If, however, 90% of the maximum voltage is applied as a reference then not only will the most probable number be accepted but also any number having 90% or greater probability will also be accepted. This percentage value may be carried to lower values to increase the chances of producing a reject by reason of two or more recognitions from one signal and thus reduce the chances of accepting an error.

The magnetic-ink character reading system is secure against most of the common types of defacement. Over-printing, dirt, or writing across the numbers causes no trouble. Embossing caused by ball point pens ordinarily causes no problems nor does wrinkled or sharply creased paper. In the process of reading, close contact with the read head is desirable, but a layer of transparent adhesive tape over the numbers causes no trouble. This means that the bulk of torn material can be repaired if necessary. Material printed with magnetic ink is highly durable, and thousands of transits across the head cause no impairment of the signal.

Magnetic Ink Printing

Magnetic ink is little different from ordinary printing ink except that it contains pigment which is magnetic in quality. Because the amount of ink transferred to paper in ordinary printing processes is not large, it is desirable to use a material which

has a large **B-H** product. The best materials so far found are those ferrites which are commonly used for magnetic tape. These materials give useful signals even with light printing although considerable care must be used in the mechanical and electronic design in order to minimize circuit and other noises.

Satisfactory inks have been prepared for both letterpress and offset printing, and there is no doubt that suitable inks can be prepared for essentially any other wet printing process. A magnetic transfer tape has also been prepared which has been used successfully on electric typewriters and some types of adding machine mechanisms. No success has so far been achieved with ordinary ribbon type transfer because we seek in this process to transfer an appreciable amount of the solid pigment and not merely a visible amount of a dye.

The several inks developed have each been tailored to transfer to the paper roughly the same amount of magnetic material. Letterpress characteristically transfers more material than does offset printing, and consequently, the offset inks carry more magnetic oxide than do the letterpress inks. Both of these inks are designed to match the magnetic transfer tape so that all three processes give roughly the same signal amplitudes. Another quality has been added to the transfer tape, namely: that of complete transfer. Without complete transfer the ink layer is not uniform and noisy electrical signals are produced, but when transfer is complete or nearly complete they produce uniform and highly reproducible electrical signals.

Engineering standards have not been established for printing and to do so may prove to be difficult. In the work carried out so far, the definition of "good commercial printing" has been adequate to produce machine readable results. Printing that is poor enough to cause a significant increase in reject rate has proven to be discernable to the eye, and is generally in the categories of smudgy or gray printing. The most probable fault is expected to be in the region of light printing where the print is definitely gray by comparison to better printing. In tests carried out, the amount of ink transferred has varied by a factor of about five to one for badly over-inked material where such faults as squeeze-out are present, to somewhat under inked material where blank spaces or grayness begin to appear. The electronic circuitry can handle this range of printing. Material has been obtained from many print shops with a wide range of printing quality and the number of rejects has been very small.

Document Handling

Basically, the paper handling problem is one of presenting individual documents to a reading device and storing them in an orderly manner after they have been read. A document sorting operation can often be conveniently performed in conjunction with this operation.

It should be kept in mind that the documents from which the information is to be read into the computer in most cases are not in new condition. They have been manhandled and mutilated to various degrees, and are not necessarily of the same size or of the same kind of paper. They may have originated from many different sources and have received all sorts of treatment. It therefore becomes impossible to base the design of the equipment upon the physical characteristics of a specific document type or even on the physical properties of a certain kind or type of paper.

A schematic presentation of the mechanical arrangement of presently used equipment is shown in Fig. 2. The equipment performs several basic paper handling functions. These consist of (1) separating the first document to be fed from the remainder of the documents in a stack, (2) feeding this document into a transport system and past a magnetic read head, and (3) stacking the document in one of several stacking bins.

In Fig. 3 a stack of documents imprinted in magnetic ink with the information to be fed to the computer is placed into the feeder bin. Vacuum nozzles within the rotating feeder drum pull the first check in the stack against the release fingers. This action seals the vacuum nozzles in the feeder drum, stopping air flow in the feeder drum nozzles and preventing additional checks from being picked up. A command from the computer energizes the release finger solenoid. The solenoid retracts the release fingers to a position below the periphery of the feeder drum, permitting the document to be sucked against the rotating drum. Friction between the document and the drum conveys the document into the double-belt transport system. Before the entire document has

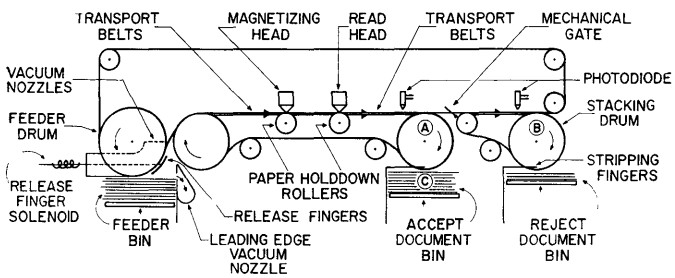


Fig. 3 (above). Document feeder details

Fig. 4 (right). Document feeder

been pulled into the double-belt-transport system, the release fingers are restored to their initial position outside of the periphery of the feeder drum. As the trailing edge of the document passes into the double-belt transport system, the vacuum nozzles in the feeder drum are uncovered and the next document is pulled against the release fingers. The next document is then ready to be fed as soon as the previous one has cleared into the transport system.

It has been found that paper documents have a tendency to stick together because of perforations, bent corners, static electricity, and for numerous other reasons. To overcome this tendency, a leading edge vacuum nozzle is incorporated in the feeder. The air flow into this nozzle separates the first document from the second as the first one is pulled against the release fingers.

It should be noted that no large valves or heavy mechanical components need to be actuated in the feeder configuration. The forces which are exerted on the paper, however, are comparatively great. This becomes apparent when one considers that the weight of a commercial document is in the order of one to two grams while the friction force between the feed drum and the paper while it is being accelerated is about two pounds. The mechanism is therefore suitable for high-speed operation.

The document is held firmly between two rubber impregnated canvas belts while it travels from the feeder past the magnetizing head and read head to the stacking drum. Rubber rollers hold the document firmly to the magnetizing and read heads to insure reliable signal output from the magnetic ink printed material, even though the paper may be wrinkled or embossed.

While the document travels from the read head toward stacking drum A, the information received by the read head is interpreted by the computer, resulting in a command that the document should be stacked in either stacking drum A or B.

This arrangement serves to sort the documents into two categories. The addition of more stacking bins transforms the machine into a sorter which may be used for sorting by decimal or other means.

The stacking drums are essentially hollow cylindrical drums with rows of small holes drilled circumferentially along the axis of the cylinder. Each axial row of holes is interconnected to a vacuum valve. If the computer commands that the document is to be stacked by stacking drum A, a photodiode in the track senses the presence and location of the document. The diode actuates a solenoid which in turn opens the required vacuum valves of the stacking drum. When the document reaches the stacking drum, it is attached to the drum by the air flowing into the vacuum holes and transported to stack C. As the document reaches the stripping fingers the vacuum valves are closed and the document is deposited in stack C. If the paper is to be directed to the other stacking drum B it is permitted to continue in its path, and the same stacking procedure is followed when it reaches stacking drum B.

In some cases it has been found to be advantageous to install a mechanical gate at each stacking drum. Such gates are used to provide a bridge to enable mutilated documents to travel smoothly to subsequent stacking drums. They are not used to deflect the document to a specific drum since this action can be achieved more positively by means of the suction holes of the stacking drum.

An experimental model of the document handling machine has been operated at rates as high as fifty-five per second with a document transport speed of 450 inches per second. Fig. 4 shows a version of an input machine which is used by the Bank of America to handle and read travelers checks. A ten-pocket bank check sorter has been in commercial operation since January 1956. All customary sizes and weights of bank checks are handled at the rate of ten per second. In the ordinary day to day operation rejects for all causes are less than one per thousand passes.

Conclusion

In the system described, character reading, printing, and document handling are strongly interrelated. The system is secure against usual defacement problems and most torn documents can be repeaired with ordinary transparent adhesive tape. Printing can be achieved with commercial equipment with little more than ordinary care. Documents can be handled and information can be read with rates and accuracy that are compatible with a large class of computer input requirements.

Discussion

W. F. Luebbert (U. S. Army Signal Corps Engineering Laboratories): In reading characters produced by a typewriter, is the reading accuracy strongly or weakly dependent upon the condition and cleanliness of the typewriter?

Dr. Kamphoefner: The typewriter should be in good adjustment. Cleanliness of the type is not a serious problem because the type strikes only the uncoated side of the mylar ribbon, and thus does not pick up ink, fibers, or dirt. Smudging between characters could be troublesome, and for that reason a special ribbon was developed that gives complete transfer of pigment with very little smear.

C. Rosenthal (Bell Telephone Laboratories): Have magnetic-ink techniques been applied to alphabetic characters?

Dr. Kamphoefner: No. We have some thoughts on the subject, but we are currently reading only ten numerals plus four symbols.

M. Marcovitz (Burroughs Corporation): How is the time at which the delay line is sampled determined?

Dr. Kamphoefner: The timing circuit that I mentioned works from the leading edge of the wave form. The initial rise has a shape common to all of the digits, so that as a result we get quite consistent timing.

W. L. Poland (Sperry Rand Corporation): How does the machine's ability to accommodate variations in signal level compare with the variations in signal level and wave form encountered in commercial printing with magnetic inks?

Dr. Kamphoefner: It has been found that if the printing is acceptable as being good commercial printing to the eye, the ink density will be satisfactory for the machine.

Chairman Burkhart: How does the reader compensate for differences in amplitude of magnetic signal?

Dr. Kamphoefner: It carries the variations in signal level, which may be on the order of 5 to 1, right up to the point that the actual decoding occurs; at that point, a differential amplifier is used for this function.

R. P. Coleman (Burroughs Corporation): What kind of circuit is in correlator networks? What is meant by 'assigning maximum on basis of probability'?

Dr. Kamphoefner: Each correlation network is a resistance matrix which, when combined with the delay line, creates a matched filter that will give a maximum output signal when it sees the wave form for which it was designed. The statement that it decodes on a probability basis is justified by several points: first, the voltage at each sample point of the delay line is carried as an analog value; i.e., information is not discarded by quantizing to only a two-state or three-state signal for each sample point; and second, the voltage from the 18 sample points of the delay line are combined before they are used. This permits a convenient means of allowing a predetermined amount of distortion in the wave forms, so that rejection rates will not be excessive for marginal printing quality. The technique for doing this is described in the text of the paper.

J. Weinstein (U. S. Army Signal Corps): Can both sides of the paper be given magnetic ink imprints without interference in read out?

Dr. Kamphoefner: No. Systems have existed that might permit this, but this particular system is purposely designed so that small accidental spacings can be tolerated between the paper and the read head. This makes the holddown of the paper at the read head less critical.

H. Freeman (Sperry Gyroscope): Have special precautions been incorporated to prevent forgery of numerals?

Dr. Kamphoefner: No special precautions, except that the magnetic ink is difficult to purchase, and we require a particular type style which must be accurately reproduced.

E. C. Greanias (IBM (International Business Machines Corporation)): Would you give the most recent error and rejection rates that you have achieved with this device and describe the type of documents read.

Dr. Kamphoefner: The only operational results on items actually circulated to the public are for the binary code; these have about a 1 in 1,000 reject rate, and a negligible error rate. A laboratory test for 100,000 checks using our first Arabic reader indicates a reject rate of about 1 in 400, and an error rate which was too small to measure accurately for this sample size; i.e., perhaps 1 in 50,000. A similar test on 100,000 checks with the most recent reader indicates a reject rate of less than 1 in 500 and an error rate on the order of 1 in 20,000 items. (These are smaller numerals without obvious stylization.)

All of the foregoing figures refer to checks or similar pieces of paper having a ten-digit number printed on each; i.e., a 1/4% reject rate corresponds to reading about 4,000 digits correctly between each check that is rejected as being unreadable, and an error rate of 1 in 20,000 corresponds to reading almost a quarter of a million digits between each check that is read incorrectly.

E. A. Coil (Martin Aircraft): Is there some safeguard against portions of two characters being simultaneously read by the wide read head?

Dr. Kamphoefner: Yes; if you had two lines spaced this closely together, they would produce wave forms which did not correspond to any predicted wave form, and the machine would automatically reject the reading. Normally, we assume that you want to permit as loose a registration as is possible for printing, and thus we use the wide head. We could use a smaller head if it were necessary to print two rows of numerals with less spacing between them.

M. J. Mendelson (Norden-Ketay): How many delay line "taps" would be necessary for a 64-character code? What are the effects of skewed paper motion?

Dr. Kamphoefner: Actually, it is not a matter of increasing the number of taps. There is not enough information available in the wave form as now derived to handle that many possibilities. The present machine starts to reject items when the skew corresponds to about plus or minus a quarter-inch over a 5-inch length.

A. G. Steele (IBM World Trade Corporation): On a document containing source information, must all pertinent data be on one horizontal plane? If so, how can we intermix different height documents?

Dr. Kamphoefner: No; several heads can be used to accommodate the various levels. In order to economize and use a single reader, you can use a head for each line of printing, and stagger the heads down the track, so that the reader first receives the signal from the first head, and then from the second head, and so forth.

M. B. Stad (Remington Rand Corporation): Does not wrinkled paper affect the shape of the output signal of a number to the point of possible unreliability?

Dr. Kamphoefner: It has been found that if you take a check, crumple it up in a tight ball in order to wrinkle it, and then spread it out, it may read or it may reject, but it normally passes through the machine without difficulty and it does not make a reading error. As for checks that are folded in a normal use, these creases are less sharp, and the machine will normally read them.

I. T. Vanderhoof (New York Life Insurance Company): Have you done any work on a machine to convert data (tape, cards, etc.) to other machine output? Or can this device be added to existent computing machines?

Dr. Kamphoefner: Yes, one of the machines shown among the slides was finished a year ago, and its purpose was to punch cards automatically with the serial number and denomination from travelers checks.

E. D. Spina (IBM): How does the printer know if he is printing correctly?

Dr. Kamphoefner: The initial type manufacture must be monitored to be sure that type style is correct and that the tolerances are satisfactory. We also have to insure that he uses magnetic ink, and beyond that if it is a good commercial job to the eye that is all that we can ask for. The registration tolerances are quite loose.

W. E. Barnes (General Electric Corporation): What provisions exist to protect the bank client from a fraudently printed check?

Dr. Kamphoefner: This question has all ready been answered, but I might add a point. If someone attempts to alter a number on a legitimate check with ordinary ink, the machine ignores this entirely. It reads the original number. Also, I might point out that the "signature" is the identification used when cashing a check, and this situation will not be changed when account numbers are added.

W. A. Hosier (Lincoln Laboratory, Massachusetts Institute of Technology): Have you tried an analogous technique with photocells and optical reading? What difficulties do you see in an optical system not present in the magnetic one?

Dr. Kamphoefner: Optical reading of numbers could be done with exactly the same system, substituting a slit optical scan, rather than the magnetic head. The most obvious difficulty, of course, is the fact that for documents circulated to the public, they sometimes acquire stray writing, overstamping, and dirt, and these would cause more trouble with an optical scan.

The Burroughs Electrographic Printer-Plotter for Ordnance Computing

H. EPSTEIN P. KINTNER

Synopsis: This paper will be in four parts, the first section will cover a system concept involving an automatic digital data-handling system feeding a high-speed output directly rather than through a buffer such as a tape storage system. Some representative programming details are indicated for this type of system involving the Ordvac computer. The next part covers the design approach, and details of the particular mechanization which was chosen to satisfy the requirement based upon electrographic recording. The electrographic recording technique is reviewed and the various relevant parts of the plotter and its capability are discussed. The third part covers the details of the computer programming required to achieve the direct output described in the first section. Part four covers some of the results obtained on the feasibility model of the printer-plotter in actual use.

THE Ballistic Research Laboratories have for some time been concerned with the development of a digital plotter capable of absorbing the output of present and future high-speed digital computers used in processing of missible ballistic data. The desired characteristics of the

H. EPSTEIN is with Burroughs Corporation, Paoli, Pa P. KINTNER, formerly with Ballistics Research Laboratory, Aberdeen Proving Grounds, Md., is now with Hoover Electronics Company, Ohio.

The authors acknowledge the significant contribution to the success of the development program of the Burroughs personnel on the project, particularly Robert E. Benn.

plotter have been formulated as follows: (1) speed, 100 points per second minimum; (2) resolution, one part in one thousand of full scale; and (3) appearance, suitable for incorporation into flight data reports. It has been additionally specified that alphameric information, such as titles, should be automatically incorporated during the plotting action. Lastly, a basic decision has been made to avoid photographic methods because of the inherent difficulties associated with film processing. However, ease of reproducibility is still to be obtained.

A number of recording methods have been investigated for possible use in the proposed plotter. Among these have been systems using electro-chemical, magnetic, and electrostatic techniques. Of those investigated, the electrostatic recording method appeared to offer the best possibility of meeting the desired performance characteristics from the standpoint of speed, appearance, and adaptability to digital plotting. A contract was let to the Burroughs Corporation to develop a preliminary model of plotter based on their electrostatic recording technique, known as the electrographic process.[1] This model was delivered during June, 1956, and has been under test and evaluation operating in conjunction with the Ordvac Computer at the Ballistic Research Laboratories. The unit has been named the Bepoc (Burroughs Electrographic Printer-Plotter for Ordnance Computing).

The Burroughs Electrographic Printer-Plotter is, as finally developed, actually a general purpose data-recording device, and represents one specific embodiment of the electrographic recording technique. The printer-plotter has capabilities for recording data consistent with the needs of the greatest digital computer capacity presently available.

The original specification of 100 points per second minimum plotting speed has been accomplished at a 300 points per second rate. The Bepoc imposes no practical limit on the recording resolution. Legends and graph lines are automatically incorporated. Reproducibility of the original record has been obtained by use of translucent paper and normal blueprint reproducing machines. Although not originally required, the machine functions as a high-speed page printer.

System Approach

An early consideration in the formulation of a system for the Bepoc was the development of a method of translating computer words into plotting positions and alphameric information. Two basic approaches were considered: (1) a decoding system external to the computer, and (2) internal computer translation. Suitable external decoding systems are readily available based on conventional digital computer components. Methods of internal translation are somewhat less familiar and understood.

The most prevalent use of internal translation is in the systems of card input-output in use on several computers. In such systems, card input is accomplished by placing an "image" of the card into the computer memory with a one-to-one correspondence between bit positions and card hole positions. A simple computer program suffices to translate the image into computer words representing the information originally punched onto the card. Conversely, card output is accomplished by a program which constructs a card image within the computer memory from the computer words desired to be punched as card numbers, and "dumps" that image onto the card, again with a one-to-one correspondence between memory bit positions and card hole positions.

Internal translation obviously saves a great deal of electronic equipment, since extensive decoding apparatus can be replaced by the computer itself. A less obvious advantage is that the flexibility of an internal translation system is limited only by the capabilities of the computer and the ingenuity of the programmers devising the translation programs. The one disadvantage is, of course, that both computer time and memory must be committed to the translation process. For the intended application, it was finally decided that the economy and flexibility of internal translation outweighted the disadvantage of requiring computer time and memory. More than anything else, the requirement for numbering and titling of the plot along with the plotting action forced the choice of the internal system, for it soon became evident that an unreasonable amount of external apparatus would be required to accomplish plotting and printing simultaneously through external translation.

Design Approach

Characteristics

The device is designed to record in page-form the output of a high-speed computer in either amphameric (printer or graphical (plotter) form, or both. The record is made on a continuous roll of 11-inch wide paper with 1/4-inch margins on either side giving $10^1/_2$-inch line-length. The record is made by printing data in dot form. Each dot is 0.010 to 0.012 inch in diameter in a matrix 50 by 50 per inch. The paper is scanned transversely by a wheel carrying a row of 30 printing pins spaced 0.020 inch apart printing a section of the paper 0.6 inch by $10^1/_2$ inches, 30 by 500 dots, on each scan. The paper is advanced 0.6 inch between scans, the recording being done while the paper is stationary.

The alphameric information, three complete lines, can be recorded during each scan, each character printed in a 5 by 7 matrix, 0.08 by 0.12 inch, 5 lines per inch, 7.14 characters per inch, or 72 characters per line. If graphical infor-

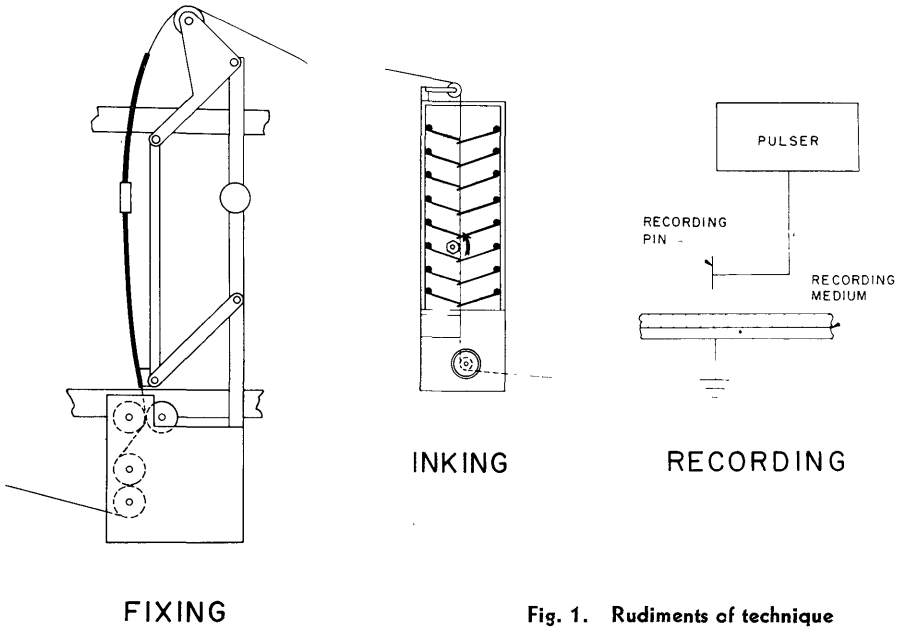


Fig. 1. Rudiments of technique

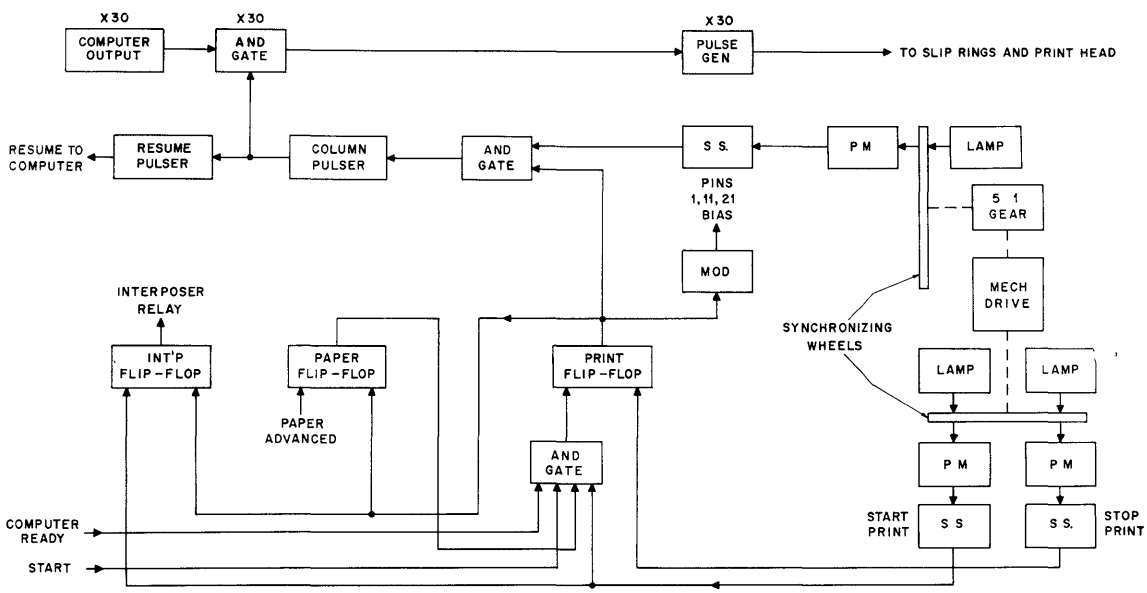


Fig. 2. Block diagram of electronic control circuitry associated with printer-plotter designed to operate on-line with high-speed digital computer

mation is recorded, the normal format allows a 1/2 inch of the $10^1/_2$-inch wide record for legend with a plot area 10 inches wide and as long as desired. Provision is made for recording faint graph lines at 5 lines per inch in each of the two co-ordinates.

As stated previously, format control in the present design rests entirely with the data handling system or computer which provides the source information. As was discussed in detail in the first section, the entire organization of the plot or printing patterns can be accomplished by internal programming within the computer. The printer can essentially be regarded in this instance as a high-speed means of recording a memory "dump"; that is, the printer at each of the 500 printing stations in a scan records a 30-bit word from the computer output register, resulting in 500 recorded words in each scan. At the normal speed of 10 scans per second, a scan occupies 20 milliseconds, during which 15,000 bits of information are fed from the computer; during the remaining 80 milliseconds of the cycle no information is fed to the printer. The word rate during the 20 milliseconds recording interval is 25 kc, 30-bit words recorded per second. The presence of each individual word in the computer output register is not indicated to the printer; it is assumed that the computer can provide information at the 25-kc rate. The recording of a word is followed by a "resume" signal from the printer to computer indicating that the computer should reload the output register with the next word. The "computer ready" signal is required from the computer before the start of the 20 milliseconds recording period. If the computer is not ready to provide the printer information for a full scan the absence of a computer ready signal will keep the printer from printing and advancing the paper.

While the printer-plotter was designed for on-line recording with the format control left entirely with the data source, the device can be extended with additional buffering circuitry to operate from magnetic tape. The particular mechanization using the scanning head allows for a minimum amount of electronic circuitry associated with the printer for high-speed serial systems.

The Electrographic Recording Technique

The printer-plotter is based upon the electrographic recording technique. Fig. 1 shows the rudiments of the technique. The electrographic recording technique produces controlled, visible dots by electrical pulse means directly. In its essentials, the process utilizes a controlled source of charge to form small charged areas on a high-resistivity surface such as a coated paper. The electrostatic latent image formed by the charged areas is made visible by inking with a single suitable powder and made permanent by thermal fixing. In applications in which the images are to be erased and the medium reused, the thermal fixing stage is eliminated. During the recording stage the electrical discharge from the point electrode to a grounded metal plate is used as the source of charge to form the electrostatic latent image on the high-resistivity paper surface. The size and shape of the image depend mainly upon the polarity, the electric field strength, and the surface coating used on the paper. A relatively low negative voltage applied to the point electrode gives small round dots suitable, for instance, for high-speed matrix printing. The recording medium is a relatively low-cost, uniformly and smoothly coated paper. The coating is a colorless, high-resistivity, thermoplastic coating. The thermoplastic feature of the coating in combination with a suitable ink, and appropriate heat processing makes it possible to make the development electrographic image completely permanent. The electrographic ink consists of a single powder consisting of material colored as desired. To ink the latent image the paper is passed through an inker containing the powder to give a visible image with virtually no background discoloration. The image is made permanently visible by passing the inked paper over a temperature-controlled hot plate. The three steps in the recording process are necessarily consecutive, and are performed as the paper moves continuously at the appropriate speed for the particular recording application.

Scanning

No known computer will transmit in one operation a 30 by 500 matrix to an external device. It is evident that the computer's output order must "scan" the matrix as it exists in the computer's memory, and that the Bepoc must follow suit, scanning its recording medium in a one-to-one correspondence.

Two types of scanning for the recording device come to mind: (1) electronic and (2) mechanical. A possible electronic scheme could be based on a single row of recording stylii, whose number is equal to the number of plotting levels, and a means of gating successive computer words into successive groups of stylii (successive computer words representing the scan action of the recording

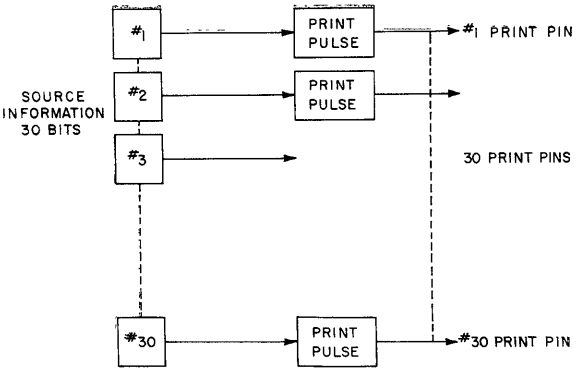


Fig. 3. Printer input circuitry for each of 30 channels

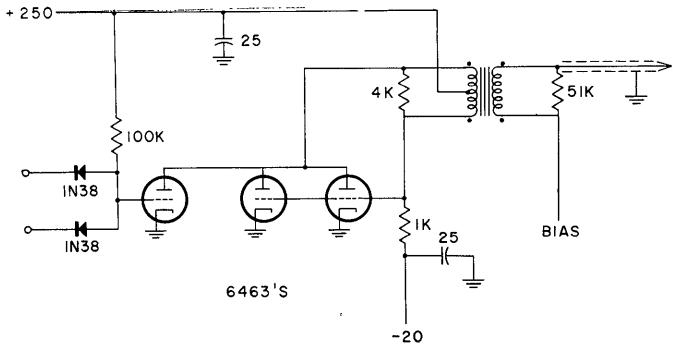


Fig. 4. Printer pulse generator with associated input gate

matrix). Such a scheme was not adopted because of the large number of stylii and gates required (500). The mechanical scanning system adopted consists of a group of 30 stylii mounted on a rotating wheel which is moved transversely across the recording medium with 500 plotting levels defined by a "clock" wheel attached to the recording wheel. Successive computer words are fed in parallel fashion to the stylii as they move and coincide with positions defined by the clock. The stylii are thereby time-shared and it is possible to record a comparatively large matrix with a small number of stylii. In this system of scanning, the computer words are oriented in the short or abscissa direction of the matrix and the matrix is scanned along its long or ordinate direction. Plotting levels have a one-to-one correspondence with the memory addresses of the matrix, and abscissa positions are determined by the relative bit positions within the computer words. It might be mentioned in passing that the electrographic process facilitates mechanical scanning since the stylii do not have to be in contact with the recording medium.

Details of the Bepoc

A block diagram of the electronic control circuitry associated with the printer-plotter designed to operate on-line with a high-speed digital computer is shown in Fig. 2. The computer is assumed to be able to provide a 30-bit output in parallel, 1 bit for each of the recording pins. Four signals are needed in order to allow a printing scan to take place: the machine "start" button has to be depressed, the computer ready signal indicating that the computer has available the information to be printed, the "start print" pulse from the timing wheel associated with the plotter, and the output indicating that the paper has advanced to the next print position must be present concurrently to set the print flip-flop. This allows for each of the synchronizing or clock print pulses derived from a notched timing wheel to set the column pulser, and read-out the 30-bit word from the computer into the 30 pulse generators. The pulses from the pulse generators are fed through slip-rings, and to the print head and recording pins. This is accomplished for each of the print positions across the paper, namely 500, after which a "stop print" pulse derived for the timing wheels on the printer resets the print flip-flop, and causes the paper to be advanced and excites the interposing flip-flop. Whenever graph lines in the transverse direction are desired pins 1, 11, and 21, or every tenth pin, are excited to print faint graph lines. If a computer ready signal is not derived from the computer and the paper remains stationary the scanning wheel, as discussed in a later section, goes through the scan but no printing takes place. It should be noted that the computer must have available the information to be printed in one scan. This is indicated to the printer-plotter by means of the computer ready signal. The printer-plotter then provides its own clock signals to derive this information from the computer and print the information at the proper positions in the scan cycle.

The printer input circuitry for each of the 30 channels is quite simple. As each of the 30-bit words is read out serially, each of the 30 bits is fed into a printer pulser and fed into each of the 30 pins in parallel as indicated in Fig. 3. The printer pulse generator with the associated input gates shown in Fig. 4. The printer pulse generator in this case is a blocking oscillator with a step-up output winding on the pulse transformer coupled to the pin. The circuitry involves conventional miniature tubes and standard supply voltages.

The 30 pins in the printing head are mounted on the periphery of a cylindrical disc which rotates at 10 times a second. Fig. 5 schematically shows the recording wheel, Fig. 6 shows the recording head mounted in the wheel. The paper is curved in a trough to conform with a trough of a vacuum anvil with the coated side of the paper facing the printing pins. As the print head scans across the paper it prints out the 30-bit word in the 500 printing stations as synchronized by the printer timing wheel and associated circuitry. The paper path through the machine is indicated in Fig. 7. The paper is taken from a supply reel and fed through a friction drive. The metering mechanism allows 0.6 inch of paper to be advanced as the printing for each scan is completed. The mechanism basically operates by clamping one side of the paper and unclamping the other side allowing a roller to pull through 0.6 inch of paper from the supply reel. The clamps cycle to the opposite phase allowing the paper to be fed through to the printing station. There is a drive at either end, one supplying the paper to the metering mechanism, and the other to pull the paper through the remainder of the machine. The paper travels through the metering mechanism, through a neutralizing device in order to electrically clean the surface of the paper, thence to the printing station. The paper is then taken through the inker and fixer and onto the take-up reels. A single scan is pictured in Fig. 8. The 30-bit word takes up 0.6 inch of paper, since the printing pins, packed at a 50 per inch density, scan across the paper through the 500 printing positions so that for each scan a band 0.6 inch by $10^1/_2$ inches wide is printed, comprising the roughly 15,000 possible dot locations. This printing is done while the paper is stationary in 20 milliseconds. The 80 milliseconds remaining part of the cycle is taken in moving the paper and allowing the source device to accumulate the data to be printed in the subsequent 20 milliseconds. A schematic representative output is

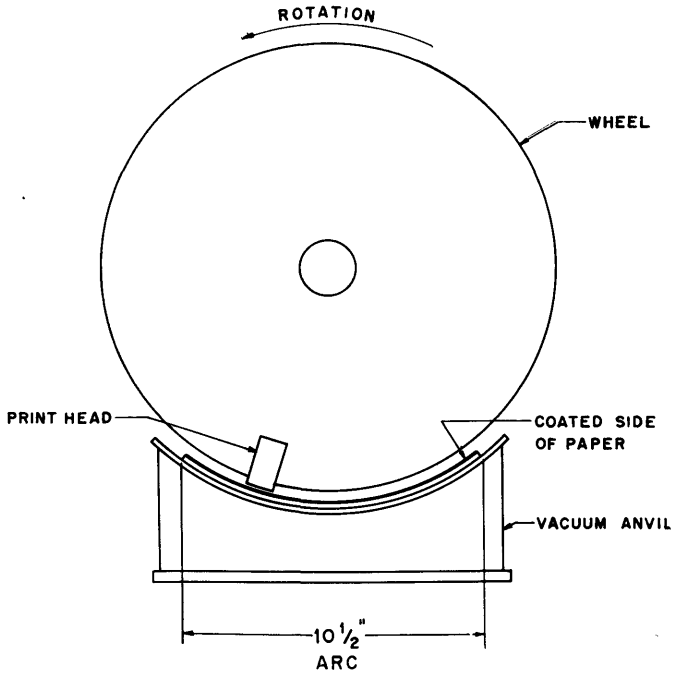


Fig. 5. Schematic of recording wheel

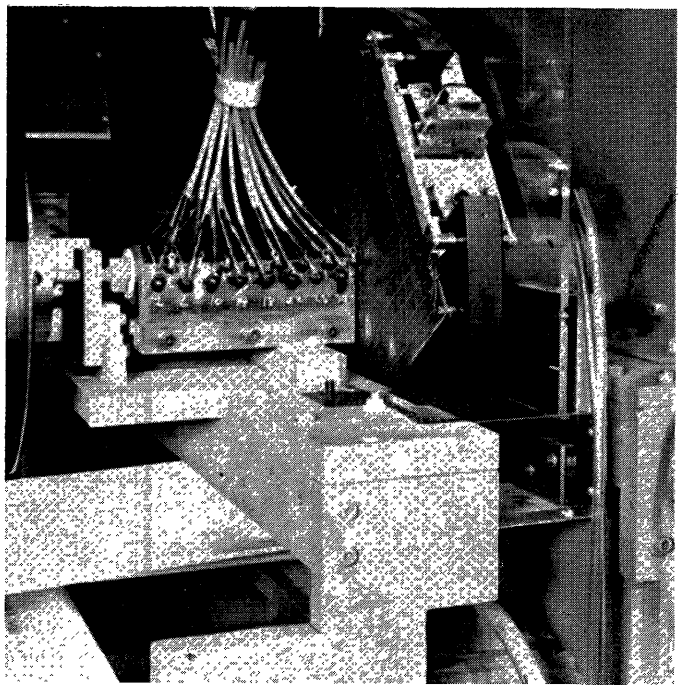


Fig. 6. Recording head mounted on wheel

shown in Fig. 9. Faint graph lines 5 per inch each way or one for every pin can be provided; legends in either coordinate axis can be printed along with plots built up by a succession of points. Any number of plots can be multiplexed into the output record, and the alphameric printing can be accomplished and are entirely dependent upon the computer programming and capability as will be discussed in the next section.

Computer Programming

Plotting

As stated previously, the recording matrix for the Bepoc has a one-to-one correspondence between plotting levels, and memory addresses of words within the matrix. A translation program for the translation of plot values into a plotting pattern within the recording matrix is accomplished simply by "planting" binary *one's* in the matrix, and at addresses fixed by the plot values. The position of a binary *one* within a word at a given address is based on the abscissa value of the point being plotted.

The exact nature of a translation program depends, of course, upon the particular order structure of the computer. One possible scheme is to have 30 "plant" orders as follows:

1 Transmit from A_1 to B_1
2 Transmit from A_2 to B_2
3 Transmit from A_3 to B_3
⋮
30 Transmit from A_{30} to B_{30}

The A addresses contain the binary *one's* to be planted and the B addresses are those of the recording matrix.

The Bepoc is intended to be primarily applied to missile data processing, and such data is almost plotted in respect to sequentially increasing time values as the abscissa of plots. In this case, the contents of the A address would be as follows:

A_1 00000...00001
A_2 00000...00010
A_3 00000...00100
⋮
A_{30} 10000.. 00000

The values to be plotted must be normalized to fit the number of plotting levels (500) and then placed in turn into the B address portions of the plant orders. Before the plant orders are executed, the entire recording matrix must be cleared to binary *zero's*.

The nature of the plant orders needs further discussion. A simple transmit from address A to address B will not suffice, since when plotting a constant value, a given B-address in the matrix will receive a series of *one's*. It is evident that the transmit into B must be of such a nature as not to destroy previously transmitted binary *one's*. A transmit add order, where A is added to B and the result stored in B, will take care of the situation for single-valued data plots. However, for multiple-value plots a binary *one* may not only be transmitted to the same word in succession but also to the same bit position. An ADD action in this case would produce a *zero* together with a carry to the next position. To prevent such an action, the transmit action should be of a type where the bit-by-bit logical sum of the contents of A and B is formed, and the result stored in B. A logical summing action as is well known, is given by the following:

0+0=0
1+0=1
0+1=1
1+1=1

No carries, of course, are permitted to take place.

Recording

Recording is based on a series of submatrices which represent alphameric information in dot form. A prevalent system of dot-matrix representation of alphameric information is based on 5 by 7 matrices as shown in Fig. 10.

It is assumed that a complete set of patterns as shown in Fig. 10 is stored within the computer memory, at a place other than the recording matrix. Placing alphameric information into the matrix is accomplished simply by transferring submatrices from the stored pattern or "bank" portion of the memory into the recording matrix portion of the memory. The basic order is

Transmit from address A to address B.

Address A is set in accordance with the location in the bank of desired alphameric character to be recorded, and address B is set according to the position on the plot

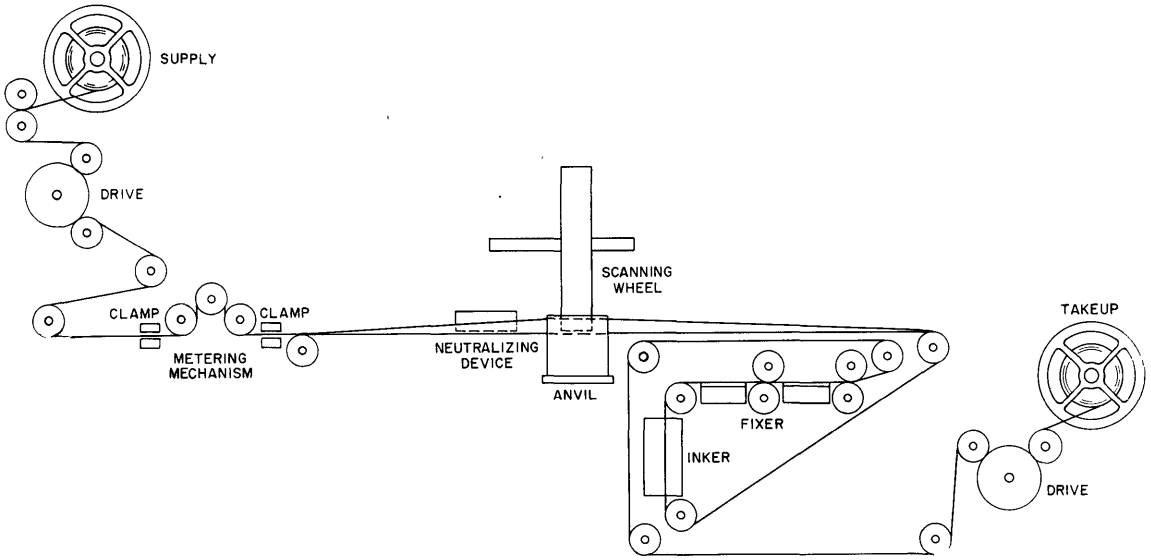


Fig 7. Paper path through machine

where the alphameric information is desired to be placed. The action is seen to parallel that of a hand typesetter. The basic order states that a type is to be picked from the type bank and placed in a type stick. Address A determines the type to be picked and address B determines the place where the type is placed by the compositor. It should be added that the basic order must be repeated 5 to 7 times, depending upon orientation of the sub-matrix, with both addresses increasing by *one* on each action, until the entire submatrix has been transferred.

Actually, address B in the above described basic order only allows placement along the long dimension of the matrix. Placement along the short dimension could be accomplished by shifting the pattern between picking it from the bank and storing in the matrix. However, this would be time consuming. A better method is to store the pattern in multiple within the bank, repeating it say three times for three possible positions in the short or abscissa dimension of the matrix, and then to "extract" into the recording matrix against a control "mask" which effectively chooses one of the sets of patterns corresponding to the abscissa position desired. This would give sufficient placement discrimination for normal plot tilting, and would fit in directly with a system for straight printing. It is to be noted that repeating the pattern in the bank in the manner described does not require additional memory space over a single listing of the pattern.

Program Times

The time required to carry out a translation program is dependent, of course, upon the computer being used. The Bepoc was originally designed to be used with a Univac Scientific (Engineering Research Associates 1103) computer, and typical times will be given from this machine.

Plotting. It is assumed that any plotting scheme will require a normalizing action and that normalizing therefore should not be charged to the translation process. Also, as data is generated in a normalized fashion, it can be stored in the "plant" orders. This leaves only the time to clear the recording matrix and the time to perform 30 plant orders chargeable to the translation program. Typical times on the Univac scientific computer for these are: clear matrix in 12 milliseconds; perform plant orders in 1.5 milliseconds, or a total of 13.5 milliseconds. It has been shown that the mechanical design of the Bepoc requires 20 milliseconds for recording the matrix,

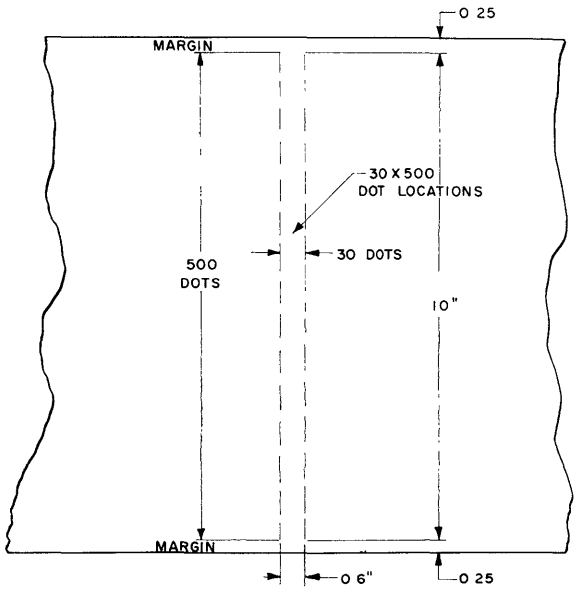


Fig. 8 (left). Single scan

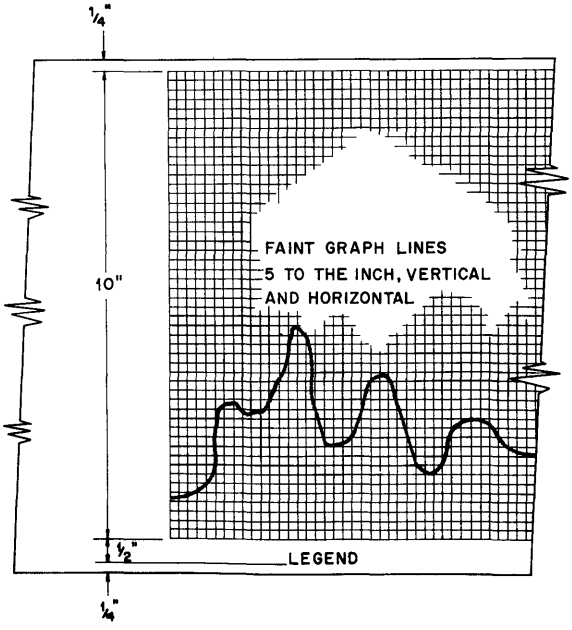


Fig. 9 (right). Schematic representative output

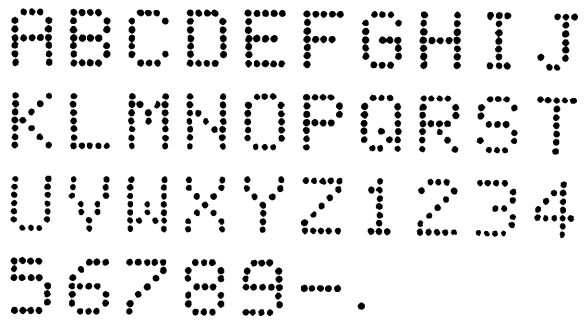


Fig. 10. Prevalent system of dot-matrix representation of alphameric information is based on 5 by 7 matrices

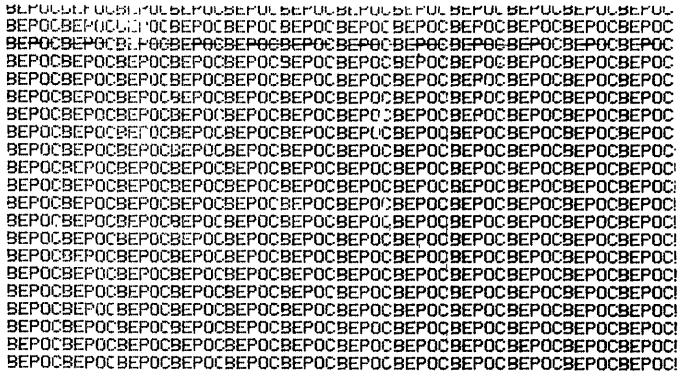


Fig. 11. Printing pattern obtained from simulator

and that 80 milliseconds is available for a translation program or other action between recordings. It is evident that there is more than enough time available for the translation program in this instance.

Recording. The Univac Scientific has within its order structure an order, the so-called REPEAT order, which greatly facilitates the transmitting of alphameric submatrices into the recording matrix. Utilizing this order, the time for the transmission of a single character is approximately 0.5 millisecond. Allowing time for the clearing of the matrix and the recording process results in an over-all printing rate of approximately 1,000 characters per second, of the same order of magnitude as parallel wide-line high-speed mechanical printers.

Computer Design to Facilitate Internal Programming

The above program times could be considerably shortened if some consideration could be given in the design of the computer for this particular internal programming. One simple addition would be an output order which cleared the memory position from which it took information, so that the matrix clear action would not have to be performed by the translation program. This could be accomplished by simply inhibiting the "restore" action which regenerates a memory position after the usual destructive readout. The result would be that not only is the need for a clear action eliminated, but also the output order is speeded up.

The second possibility is to store the alphameric patterns in a separate section of the memory, with non-destructive readout. Such a system might transmit ten times faster than the conventional transmit, where restoring action, etc. must be performed. It should be possible then to obtain translation rates of around 20,000 characters per second.

As has been indicated previously, the order structure of the computer can greatly facilitate the internal translation required for the Bepoc. Desirable orders are the logical sum, or bit-by-bit OR, and the logical product, or bit-by-bit AND, sometimes termed an EXTRACT order. A means of repeating an n times, with the order addresses automatically advanced by *one* for each action is extremely valuable for manipulating alphameric submatrices.

Results

Patterns fed to the Bepoc during the developmental phase have been from a "simulator" consisting of a group of shift registers arranged to give a 30 by 10 matrix. Patterns placed in shift registers are repeated 50 times on a scan action.

Fig. 11 shows a printing pattern obtained from the simulator. Fig. 12 shows graph lines as recorded by the Bepoc. Fig. 13 indicated a plot of a function along with the numerical value of the function given periodically. This plot was made with the Bepoc coupled on line to the Ordvac.

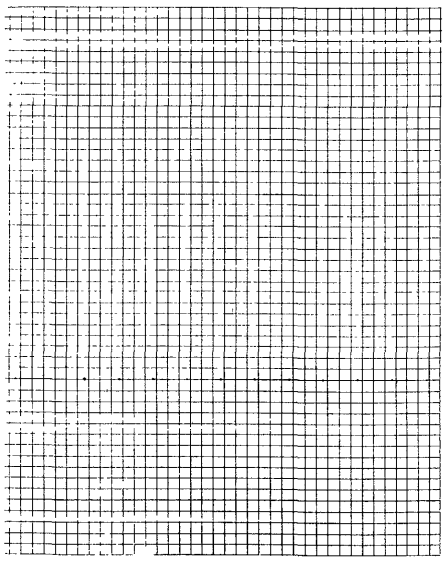


Fig. 12. Graph lines as recorded by Bepoc

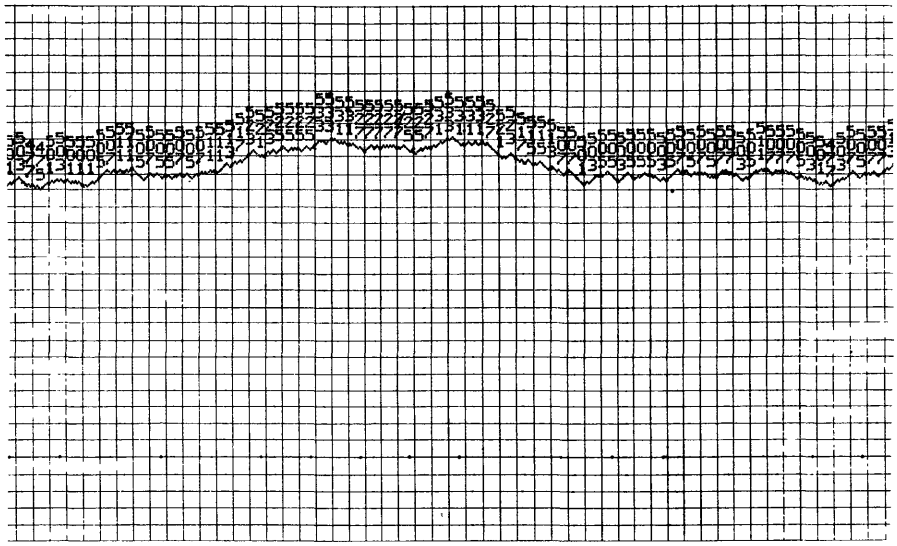


Fig. 13. Plot of function along with numerical value of function given periodically

Conclusion

A device for high-speed plotting, printing or both has been described. The device is intended specifically for the high-speed recording of the output of computers used for the processing of missile ballistic data, but is actually a general purpose data recording device, and has capabilities for recording data consistent with the greatest digital computer capacity presently available. Results obtained from the feasibility model indicate that this device is capable of substantially advancing the art of high-speed recording of digital computer outputs.

Reference

1. Proceedings of the Western Joint Computer Conference. *Special Publication T-76*, Institute of Radio Engineers, New York, N Y. "The Electrographic Recording Technique," **Herman Epstein**, March 1955, pp. 116–18

Discussion

J. L. Hill (Remington Rand Univac Corporation): Are the blocking oscillator transformers on the wheel or are the high voltage leads carried through the slip rings?

Dr. Epstein: The blocking oscillators are not on the wheel. The shielded cable from the secondary of the blocking oscillator is fed through the slip ring and hence to the wheel.

M. Weinberg (Monroe Calculating Machine Company): How do you prevent the fields produced by the arcing from introducing errors in the computer?

Dr. Epstein: A different embodiment of the electrographic recording technique was tested recently at the Signal Corps Engineering Laboratory for noise measurements. The noise which is produced by the printing technique and the associated equipment in this particular device was very small, below the noise level of the receivers in some of the tests.

R. B. Bonney (Electronic Engineering Company of California): How many vacuum tubes are used to drive the writing points for the complete matrix?

Dr. Epstein: The total machine has 38 tubes, of which 15 are used for the 30 printing pins in the head.

N. Newby (Bell Telephone Laboratories): What coating is used on the paper, and what maximum delay is possible between charging the paper and inking?

Dr. Epstein: The coating on the paper is a high resistivity resin, and depending upon the electrical surface and various other characteristics of the coating, the delay between charging the paper and inking can be either milliseconds or years.

J. R. Roberts: What is the operational meaning of "100 points per second?" Is not meaning a function of point-to-point distance? In other words, is not "points speed" meaningless?

Dr. Epstein: The machine plots 300 points per second at the spacing of 50 points to the inch. There are 30 pins, each pin represents one channel. If, during each scan, each of the pins were pulsed once, it would give 30 points along the graph. Since with the machine cycling ten times a second, the plot is derived at a rate of 300 points per second. However, during the plotting time, if a point is recorded at every available printing position across the paper, the recording is accomplished at the rate of 25,000 times a second for each of the 30 points, or at the rate of 750,000 points per second.

M. B. Stad (Remington Rand Corporation): Was the large-diameter disc shown in the slide the actual recorder, or an additional wheel?

Dr. Epstein: The actual wheel circumference is 5 times 10 inches, roughly 50 inches; the diameter is roughly 17 inches. The other wheel you are referring to is the optical synchronizing wheel. In other words, there are two synchronizing wheels, one for synchronizing pulses for printing at each of the 500 positions, and then there is an additional wheel to provide the stop and start scan pulses.

A Transistorized Transcribing Card Punch

C. T. COLE, Jr. K. L. CHIEN C. H. PROPSTER, Jr.

THE RCA (Radio Corporation of America) BIZMAC Transistorized Transcribing Card Punch described in this paper provides a means for converting large volumes of data stored on magnetic tape in the Bizmac code into characters punched on electronic accounting machine cards using the IBM (International Business Machines Corporation) code. This output device will transcribe information at the rate of 150 cards per minute, and provides accuracy control features to assure correct data punching. The functional operation of the transcribing card punch is compatible with the Bizmac system and with general punched-card system requirements as well.

The device consists of two packages. The electronic circuits are housed in racks which permit rapid access to vertical mounting panels for servicing. Plug-ins are used throughout, and a simple transistor circuit element which performs all the logical functions is employed. The results of a review of punching methods, coupled with a requirement for easy replacement of parts, guided the mechanical design of the card transport and punch mechanisms. These are placed in a separate cabinet with removable covers. Input and output hoppers are at a convenient height. Design emphasis was primarily directed toward obtaining a high degree of accuracy control in a device with maximum functional flexibility.

Functional Description

Input messages to the Transcribing Card Punch are received from a BIZMAC magnetic tape station through seven channels. Character rates of 10 to 30 kc are acceptable. The Transcribing Card Punch requires that messages from magnetic tape be of fixed field format. BIZMAC alphanumeric characters and the eight punctuation marks which have IBM 407 punch equivalents are translated and punched on cards. The six BIZMAC punctuation marks which do not have IBM equivalents are translated as blank columns on the cards. All BIZMAC control symbols such as start message, item separator, and end message, are eliminated during translation and do not create blank columns.

A plugboard is incorporated to permit data rearrangement and character insertion. Specifically, the plugboard provides the three following functions: (1) The formation from magnetic tape can be rearranged in any sequence on the cards. (2) Control symbols can be overpunched into the same card column with numeric punches. and (3) Fixed data may be

C T. Cole, Jr., K. L. Chien, and C H. Propster, Jr. are with the Radio Corporation of America, Camden, New Jersey.

The authors wish to acknowledge the contributions of J. E. Palmer, R F. Bov, H. H. Cramer, and J. O'Donnell on this project.

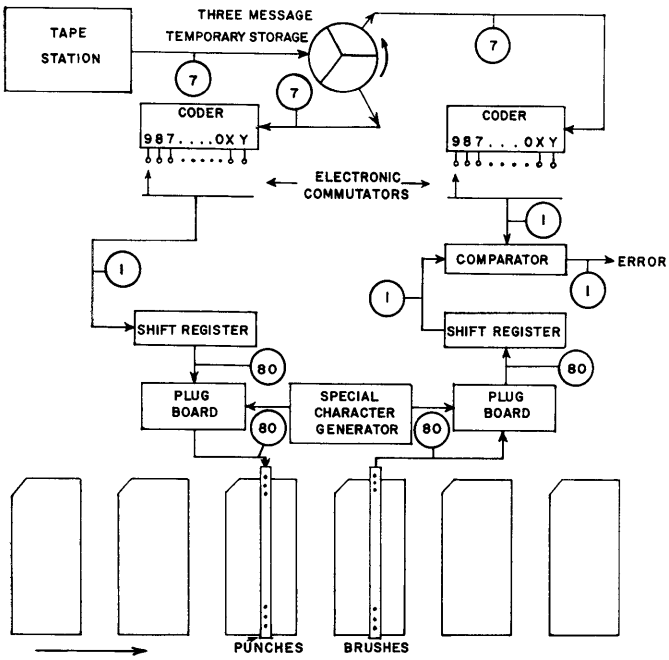


Fig. 1. Block diagram of Transcribing Card Punch

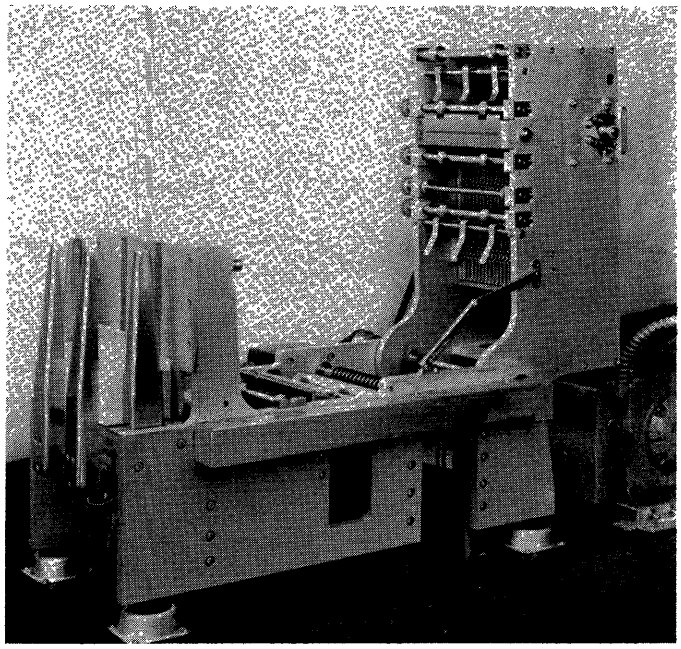


Fig. 2. Card handling mechanism

punched as required. The plugboard wiring used for punching is duplicated for checking purposes.

Logical Operation

A block diagram of the transcribing card punch is shown in Fig. 1. Three messages are in process at any one time. One is being read-in while the second is being punched and the third is being checked. The operation will be described by following one message through a complete machine cycle.

1. *Read-in Cycle*: During this time, the temporary storage is erased and connected to the tape station. The tape is started, a complete message is read into the temporary storage, and the tape is stopped. This provides almost one complete card cycle of 400 milliseconds for read-in. At the end of this cycle, the temporary storage sector containing the message just read in is switched to the punch channels.

2. *Punch Cycle*: Throughout the course of the punch cycle, the information is read from the temporary storage into the BIZMAC to IBM coder. The output of the coder is fed to a 12-channel electronic commutator which is synchronized with the card advance. The commutator sequentially selects the output channel from the coder corresponding to the row to be punched. From the commutator the serial data is sent to the shift register which converts the information from serial to parallel form. All 80 bits of information are read out simultaneously through the plugboard to a register which drives the 80 punch magnets. Thus, one card row is punched. This process is repeated 12 times and then one card is completely punched After a card is punched, it is transported to the check station.

3. Check Cycle: During the check cycle, the card is read, one row at a time, by 80 brushes and the information relayed through the plugboard into a second shift register. This shift register converts information from parallel to serial form and its output is routed into a single channel comparator. In the meantime, the temporary storage containing the original information has been switched from the punch channel to the check channel. The information in the temporary storage is translated again, by a second BIZMAC-to IBM coder, into 12-channel IBM code. Another 12-channel commutator selects and routes the correct channel to the Comparator to be checked with the information read back from the brushes.

It can be seen that the temporary storage contains three sections which are switched cyclically around the read-in, punch, and check channels. Three messages, one being read in, another being punched, and another being checked, are in process simultaneously.

A high degree of accuracy is maintained during transcription by reading back the data punched on the card and comparing it with the original message which is retained in the transcribing card punch memory. A duplicate BIZMAC to IBM coder is used in this operation. The sequence of start message and end message symbols is monitored to insure that all messages are punched in their entirety. In addition, input information is checked for parity prior to translation.

Mechanical Design

Fig. 2 shows the card handling mechanism. Construction features were incorporated to facilitate operation and servicing. As shown in Fig. 2, the top rollers, punch mechanism, and magnetic structure can be raised for easy access. Rapid replacement of machine parts is realized via unitized construction. The punch and solenoid assembly can be removed from the frame of the card mechanism as a unit. A spare punch or solenoid assembly can be quickly installed and the unit replaced with only minor field adjustments. The punches and associated holding magnets were designed to give maximum life while operating at 150 cards per minute.

To begin operation, blank cards are placed into the input hopper where they are held above the continuously reciprocating picker knife by solenoid operated plungers. When the solenoid is energized, the plungers are retracted, lowering the cards onto the picker knife and permitting them to be fed, nines edge first, into the mechanism.

The cards are moved intermittently, one row at a time, and are momentarily stopped while each row is punched. The intermittent drive action, which approaches a sinusoidal form during the card advance cycle to minimize impact.

Fig. 3 illustrates the knee-action punch mechanism. With no current applied to the solenoid, shown to the right of the knee-action mechanism, the solid line drawings show the action resulting when the continuously driven eccentric, shown at the top of the figure, operates in synchronism with the card advance mechanism. No punching occurs with the solenoid de-energized, but at the start of each punch cycle, shown on the left side of the drawing, the solenoid armature is returned to the solenoid proper.

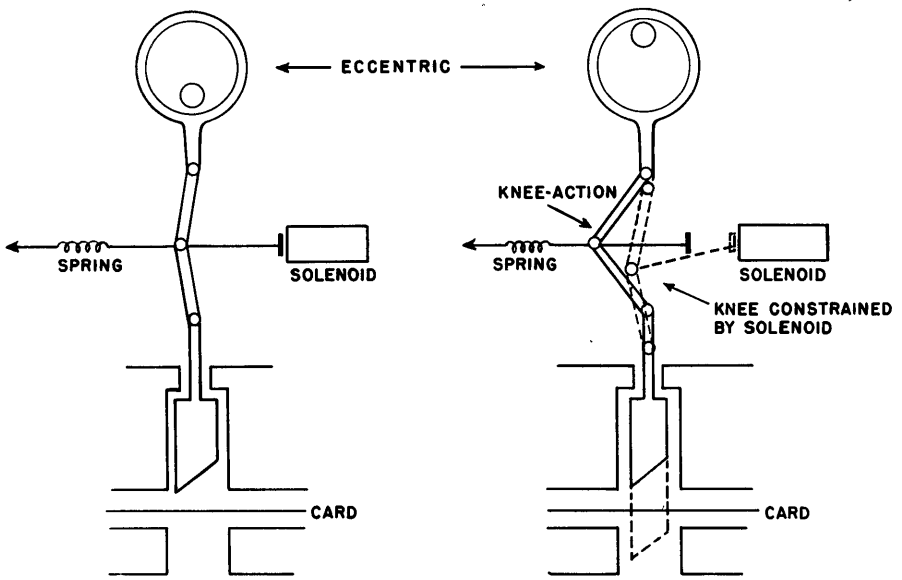


Fig. 3. Knee-action punch mechanism

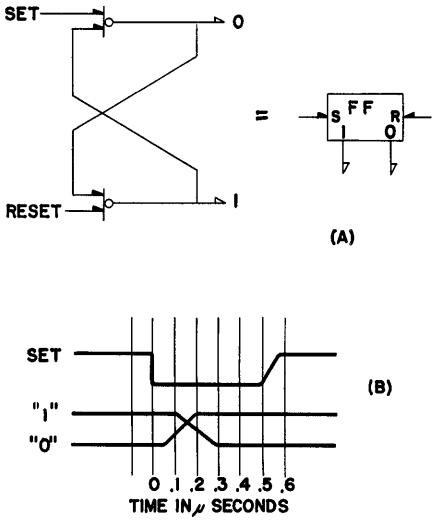


Fig. 5. Basic elements connected to produce a flip-flop

When the eccentric is at the "top" position, the solenoid, if energized, is required to move no mechanical mass, but simply to prevent the knee from bending. This requires relatively little force. A dotted representation of the mechanism on the down cycle with the solenoid energized for punching is shown on the right side of the figure.

Two advantages of this mechanical design are noteworthy. The solenoids, which actuate punching, are required to merely hold the linkage during its punching stroke. Thus, the actuation time of the punch is limited only by the energizing time of the solenoid coil. Secondly, the manner in which the intermittent drive is obtained permits smooth card acceleration.

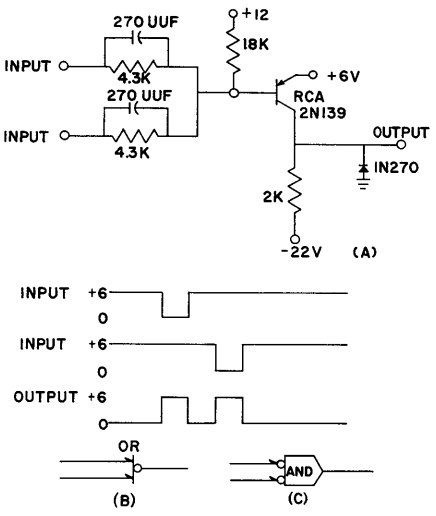


Fig. 4. Transcribing Card Punch in simplified form

Transistorized Circuits

The basic circuit chosen to meet the logic requirements of the BIZMAC Transcribing Card Punch is shown in simplified form in Fig. 4. It is known as a two-input resistor gate. This element provides not only the gating function, but signal amplification and standardization as well, all with one transistor. The circuit has proved a very powerful logical element since any number of stages may be directly cascaded to synthesize any logical array. The logic designer is no longer concerned with the problem of inserting signal re-standardizing and amplifying elements such as pulse amplifiers. Indeed, few pulses are required in machines using these d-c circuits. The avoidance of pulses is in itself a substantial step forward for the logic designer. More improtantly perhaps, the maintenance man in the field may now employ rather simple d-c testing techniques. Both the logic designer and maintenance man find their work simplified since they must learn only one simple, though very flexible, logic element. Due to this new simplicity, errors in logic design have been sharply reduced.

Referring to Fig. 4 then, observe that if either input is lowered to ground potential, current will flow through the base of the transistor, turning it on and raising the ouptut to plus 6 volts. Hence, for negative going signals, assumed to be standard information signals, the element acts like an OR gate followed by an inverter. Fig. 4 shows this logical representation of the element. If only one input is used, then element functions as a simple power amplifier-inverter.

Notice that when, and only when, both inputs are at plus 6 volts, the output will be at ground. Thus, another logical representation may be used, the AND function. Since this requires positive signals and the normal signals are negative, we indicate this by showing logical inverters at the input of the AND gate to denote that NOT signals are required. In this operation, the element may also be looked upon as a double inhibit gate.

The capacitors shown across the input resistors of the circuit of Fig. 4 are used to speed up circuit operation. Their primary purpose is to quickly rid the transistor of the stored charge which accumulates in the base region when the transistor is "bottomed."

Typical signal delays of 0.2 microsecond per stage are obtained when elements are connected in series. The output resistor of each element can absorb 10 milliamps from the stages it drives, and 1.6 millamps are required by each gate input. Hence, up to six gate

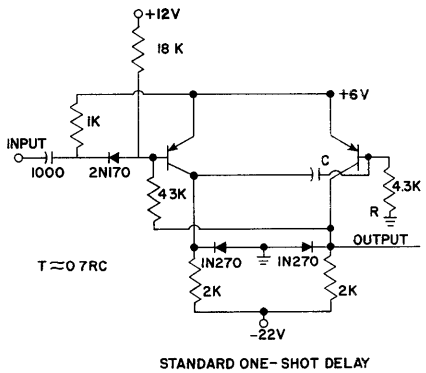


Fig. 6. Standard one-shot delay

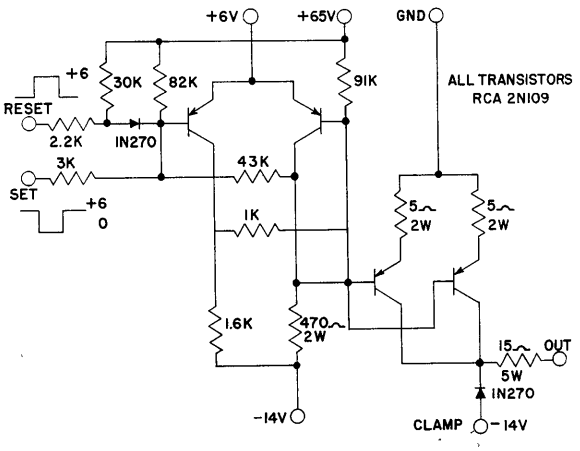


Fig. 7. Relay and solenoid driver

inputs may be driven from each element. The 18,000-ohm resistor is used to supply leakage currents when the transistor is OFF.

The RCA Transistorized Transcribing Card Punch uses this element, packaged four per plug-in, for all except specialized logic functions like shift registers.

It is necessary to provide for the flip-flop or storage function and Fig. 5 shows how two basic elements may be connected to produce a flip-flop. Typical unloaded wave forms are also shown. Such a flip-flop may be set and reset at a 1-megacycle rate, although such speeds are seldom required by input or output devices.

It is important that time delay or pulse forming circuits be available to the logic designer. An accurate time delay or pulse forming one-shot multivibrator is easily built using transistors. The one-shot chosen as the "standard" transistor delay element is shown simplified in Fig. 6. This circuit is designed so that large changes in supply voltages or transistor parameters do not appreciably affect the output pulse width.

The Transcribing Card Punch requires storage for the data to be punched and also for the data read from the checking station. Shift registers are applicable since in the former case serial to parallel conversion is required and in the latter case, parallel to serial conversion. Magnetic elements were considered, but a transistor shift register was finally chosen since it is more easily understood by maintenance personnel, costs being approximately equal.

Transistors have proved capable of handling much of the medium power applications in digital computer work. Over 5 watts at a 20 per cent duty cycle (400 milliamps at 14 volts) are delivered from the circuit shown in Fig. 7. This circuit is used to drive punch solenoids and relays. Three circuits are packaged per plug-in. A flip-flop is included as part of the package to provide for bit storage, and to serve as a power preamplifier for the two output *2N109* transistors in the circuit.

In summary then, the choice of the resistor gate greatly simplified the circuit design problems. Here, with only one circuit, can be had the OR gate, AND gate, NOT gate, inverter, power amplifier, and flip-flop. The transistor has not only reduced equipment size and power requirements, but has simplified design problems as well.

Conclusion

By means of the transistor plug-in elements and card punching mechanism described in this paper, material advantages are immediately obtained. Circuit simplicity is enhanced and the training of competent service personnel is shortened. Equipment size is reduced as are power and air conditioning requirements. Higher speed punching has been made feasible, and maintenance and replacement of parts is simplified.

Furthermore, life test results and reports on reliability of equipment in the field indicate a transistor circuit failure rate of less than 0.1 per cent per thousand hours.

Discussion

C. Kagan (Western Electric Company): Reference has been made to application of this unit with BIZMAC Systems. Is RCA prepared to produce data-processing equipment such as this and BIZMAC or is this merely an exposition of RCA developmental work?

Mr. Propster: As far as is known, RCA intends to stay in the computer business.

A. Krell (Remington Rand Univac): Please describe in more detail the temporary storage.

Mr. Propster: The temporary storage consists of, in effect, three storage sections. The sections are switched cyclically, in order to allow three cards to be in process at any one time.

M. J. DiCarlo-Cottone (Bell Telephone Laboratories): If I understood correctly, a duplicate plugboard is used for checking. Why is not echo pulse' circuitry utilized?

Mr. Propster: When you try to punch a card, it is all very well to energize the punch, but for one reason or another, it may, for example, stick and not punch, or, even though punched, the hole may not be readable. It was felt that it would be better to check that the card is readable, rather than that the punch was energized or that the punch had moved. By the way, there is not a duplicate plugboard; there is one plugboard with duplicate wiring on that plugboard.

C. K. Vanderhoof (Prudential Insurance Company): What check is made that the data has been accurately transcribed from tape to card?

Mr. Propster: There is a parity check on the data coming from tape, so that loss of a single bit in any character will turn up as an error.

B. Jenkins (Computing Devices of Canada): What is the indication if the card has been punched incorrectly?

Mr. Propster: The card with the error is rejected, together with the cards that have already been fed and are in the mechanism, so that we get 3 or 4 cards in a reject pocket and the machine stops. Appropriate indications are made of the kind of error that stopped the machine.

Mr. Lippel (IBM): What is your procedure for error correction?

Mr. Propster: Let us suppose first that it is a transient error of one sort or another. There is a button to be pushed which backs up the magnetic tape the appropriate number of messages, the machine then restarts and a second attempt is made to go through without error. However, if it is a machine failure and not a transient error, it will be necessary for corrective maintenance of the machine.

Apparatus for Magnetic Storage on Three-Inch Wide Tapes

R. B. LAWRANCE R. E. WILKINS R. A. PENDLETON

IN DESCRIBING the tape transport of the DATAmatic 1000, it is perhaps well to begin by reviewing the influential system features and their resulting requirements in the following sections:

Information Rate

The central processor communicates with the magnetic file units through the input and output buffers at the steady average rate of a quarter of a million bits per second. With any presently practicable tape speed and recording density, this requires a tape width greater than the conventional half inch or so. DATAmatic-1000 tape has a nominal width of 3 inches (actually 3.056), carries 31 channels of information and 5 channels of prewritten magnetic block marks, is transported in either direction at a speed of 100 inches per second, and utilizes bit densities per channel of 320 and 160 bits per inch.

Organization of Words and Channels

As mentioned earlier by J. E. Smith[1] 48 information bits and 4 checking bits are grouped together in each word. In writing or reading, all the bits of a word are fed sequentially to a single channel so that characters and words are organized completely longitudinally rather than across the tape. In recording, a timing relationship does exist between bits being written in the various information channels, but this is only incidental and a matter of convenience; in playback there need be no interchannel timing relationship at all. Transfer of information from a tape into the input buffer or output converter is asynchronous. There is no synchronous channel and no requirement for simultaneous sensing of bits in the information channels. The major potential source of trouble from skew is thus eliminated.

Organization of Words Into Blocks

The locations on tape into which information is written are pre-established and marked by magnetic block marks, which are placed on the tape before it is magnetically inspected and put in service; these block marks are never altered thereafter. As shown in Figs. 1 and 2, information space and stop-start space are alternated in an interlaced pattern with an over-all length of 1.23 inches. The tape, approximately 2,600 feet long, contains 50,000 blocks, of which 25,000 belong to the so called "first half," normally scanned in the physical forward direction, and 25,000 to the "second half," normally scanned in the physical reverse direction. On scanning the first half, the interlaced second-half information space serves for stop-start space (somewhat over 0.6 inch) and similarly, for scanning the second-half information space, the first-half information space is available for stopping and starting. Apart from the improved efficiency of tape utilization, this has the considerable advantage that no separate rewind operation is required.

Reading and Writing

The same magnetic head assembly is used for writing and reading. Because of the pre-established information spaces and block mark pattern, and because of the nature of the recording system, it is possible to alter information, when required, simply by writing new information over the old, in as few or as many channels as desired. It is thus required of the tape mechanism that at the time of rerecording, the relationship of head and tape must be closely controlled both laterally and longitudinally to be essentially the same as when the original recording was made. Since it is a feature of the DATAmatic-1000 system that tapes recorded on any individual tape drive may be played back or rerecorded on any other tape drive, the channel locations on the magnetic heads and the tracking of the tape must be held to within a very few thousands of an inch.

Ability to Scan Information In Either Direction

In the DATAmatic 1000, recording of information is always done with the tape moving in the logical forward direction, physical forward for first half blocks and physical reverse for second half blocks. Playback however, can be done in either direction. The tape mechanism is thus required to scan information in either direction under a variety of continuous motion and stop-start-reversal conditions; hence the stopping, acceleration to nominal speed, accuracy of nominal speed, and tracking all must satisfy certain rather stringent conditions.

In addition to the system requirements outlined briefly in the foregoing, various other requirements must be met by the tape mechanism. Of prime importance is the requirement that no normal operation or conceivable malfunction of the tape mechanism shall result in deterioration or destruction of the tape or its information content.

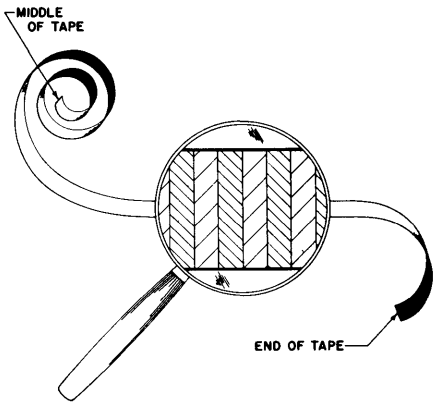


Fig. 1. Alternating first-half and second-half information spaces on D-1000 magnetic tape

The tape employed has a special construction shown in Fig. 3. The magnetic head does not come in contact with the magnetic recording oxide but is separated from it by a 0.5-mil layer of Mylar. In manufacturing, the oxide layer, whose thickness is also 0.5 mil, is deposited on this Mylar overlayer so that the oxide surface nearest the head gap has the smoothness characteristic of the Mylar sheet rather than the less perfect surface characteristics of the air-dried mixture of oxide and binder. A laminating adhesive whose thickness is approximately 1/4 mil is then used to attach the composite oxide and Mylar sheet to a base of 2.0-mil Mylar. The result is a tape which produces much less wear on the magnetic head than do direct contact tapes; furthermore, the information-carrying oxide is protected from abrasion, scratch-

R. B. LAWRANCE, R. E. WILKINS, and R. A. PENDLETON are with the DATAmatic Corporation, Newton Highlands, Mass.

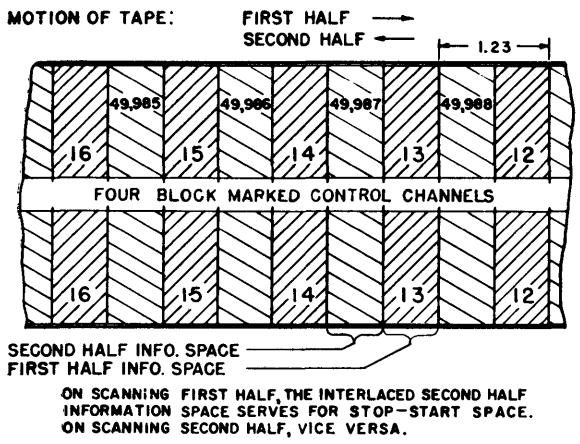


Fig. 2 (left). Organization of information spaces and block mark channels

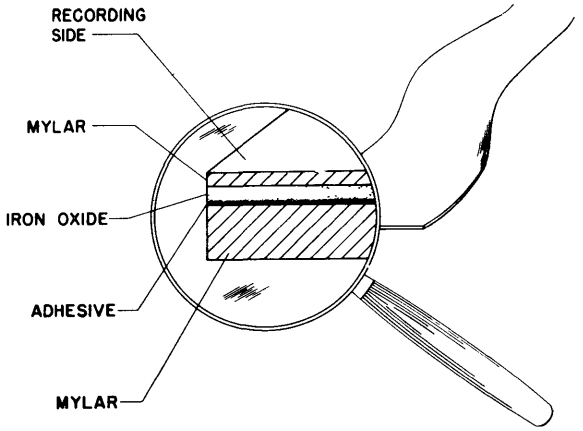


Fig. 3 (right). Enlarged section D-1000 magnetic tape

ing, flaking, embedment of dust, moisture, and other forms of deterioration.

Fig. 4 shows two magnetic head assemblies, one of which is shown unmounted and the other mounted in its cylindrical cartridge. The heads are of staggered gap construction and have the following significant dimensions and specifications:

Number of channels: 36
Offset of alternate channels (stagger): 0.20 inch on centers
Gap width: 1 mil (.001 inch)
Gap shim: 1 mil beryllium copper
Channel width: 60 mils
Gap height: 20 mils
Spacing of channels on centers: 82 mils
Tolerance on channel locations: ±1.5 mils
Radius of curvature of head and cartridge: 2 inches
Magnetic material: 3 mil mu-metal laminations
Number of turns: 100
Voltage output on normal playback; 10 millivolts peak-to-peak

Tape Transport Mechanism

The appearance of information recorded on tape is shown in Fig. 5. For clarity, only the locations of information pertaining to first-half record spaces are shown; those pertaining to second-half information would be interlaced in accordance with Fig. 2. The alternating pattern due to the staggered gap construction is evident from Fig. 5, although for simplicity it was not shown in Figs. 1 and 2. In the enlarged portion of the figure is shown the appearance of a portion of a typical word as it would be made visible by magnetic development with colloidal Fe_3O_4. The vertical lines correspond to pole concentrations, alternately north and south, produced by reversal of the head current. It will be noticed that the spacings of pole concentrations have two characteristic values, approximately 3.0 and 6.0 mils (30 and 60 μsec) as written on tape. A 30 μsec interval between head current reversals represents a *zero* bit and a 60 μsec interval represents a *one* bit. It is possible with a little practice to read visually the bits of a word when the magnetic image is carefully developed and viewed under a medium power microscope.

The attainment of the high bit densities quoted above, with the relatively wide head gap and the unusually large 0.5-mil separation between the pole face and the magnetic oxide, is due to the characteristics of the recording and playback system, which represents a radical departure from present practice. Space does not permit further description of these features in the present paper.

As indicated in the opening section of this paper a considerable part of the flexibility of the DATAmatic-1000 system results from the use of unnumbered but accurately located information spaces specified by the permanently placed magnetic block marks. The action of the tape handling equipment in decelerating, reversing, and accelerating tape must accordingly be fast and reproducible under all conditions of motion. In one important mode of motion the tape moves continuously; this mode is so simple that it does not require further discussion. In stop-start motion, when the tape is instructed to stop after scanning a block it must come to rest well within the allotted space before the next information space. Upon restarting in either direction it must reach full speed and be in steady motion by the time the next information space is entered, as indicated by sensing the beginning block mark. In order to fulfill these requirements, considerable care has gone into the evolution of the assembly shown in Fig. 6, which shows a closeup of the capstan, brake, head mounting, valve, and actuator assembly, with the tape draped in position. The contour of the tape and the relative locations of the surfaces with which it comes in contact are shown in more detail in Fig. 7.

Two continuously counter-rotating capstans of approximately 10-inch circumference are used, and these are driven at approximately 10 revolutions per second by a synchronous motor. To move the tape in a desired direction, the slotted

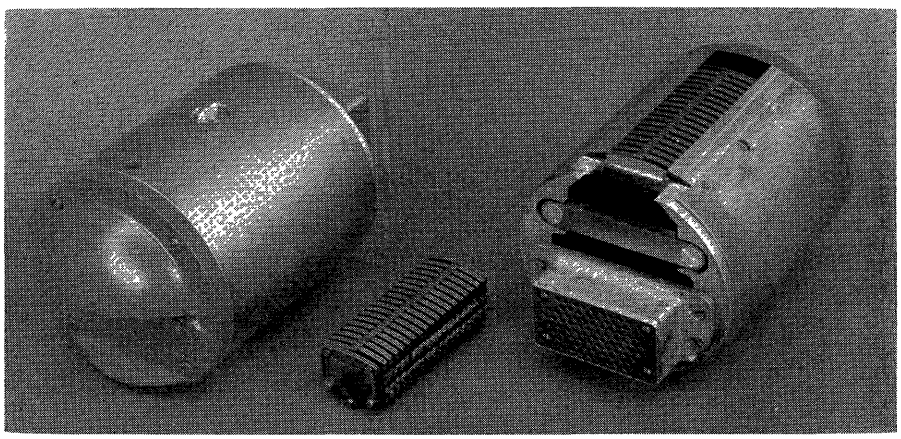


Fig. 4. Two magnetic head assemblies, right: head mounted in cylindrical cartridge; left: head unmounted

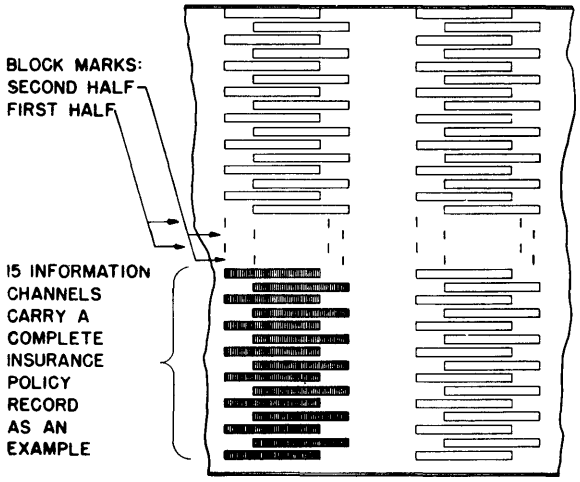


Fig. 5. Information on tape, showing channel stagger

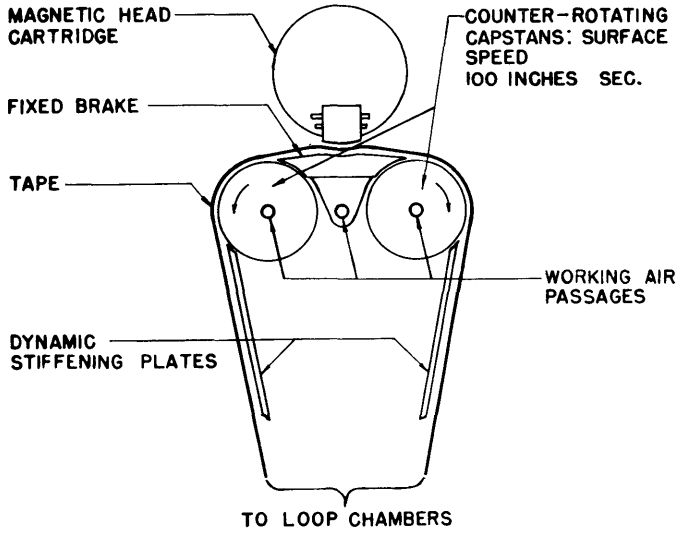


Fig. 7. Capstan, brake, and head assembly

surface of the appropriate capstan is communicated (through an internal commutator, a hollow shaft, and a fast-acting electro-pneumatic valve) to a reservoir containing air at reduced pressure. Atmospheric pressure then presses the tape into contact with a portion of the surface of the chosen capstan.

For arresting the motion of the tape a stationary brake surface of similar slotted construction is used. The brake is located closely adjacent to the magnetic head assembly and surrounds it on both sides. This has the desirable effect that when tape motion is arrested by engaging the tape to the brake surface there is a minimum of lateral or longitudinal displacement relative to the head. Upon subsequent resumption of tape motion in either direction, the tape in contact with the head needs to make essentially no tracking adjustment before it is again running true.

The contour of the brake and its location relative to the magnetic head are such that the tape has a slight wrap

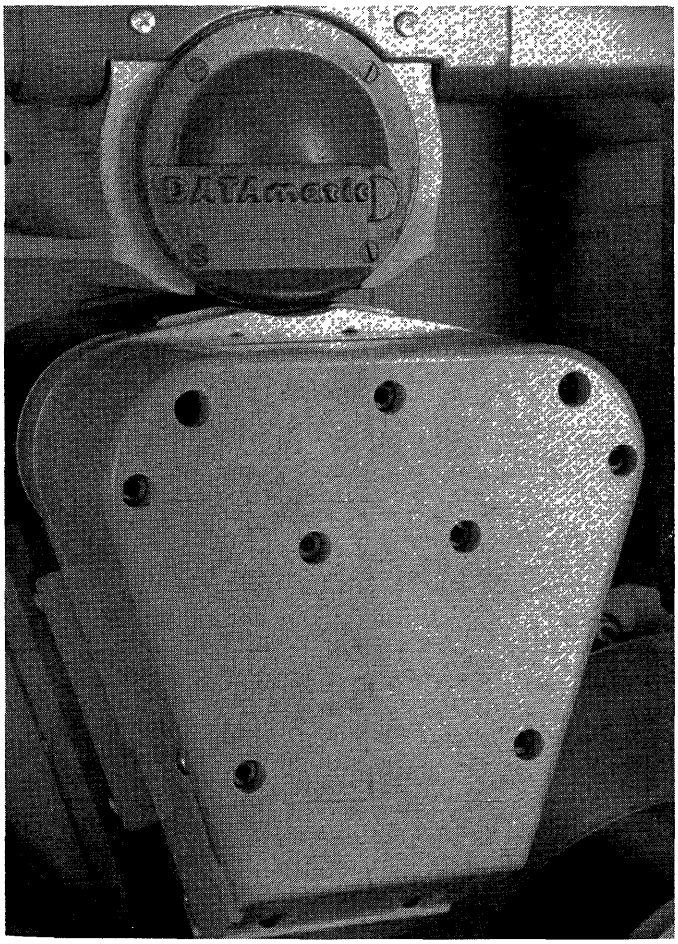


Fig. 6. Capstan assembly, showing tape in position

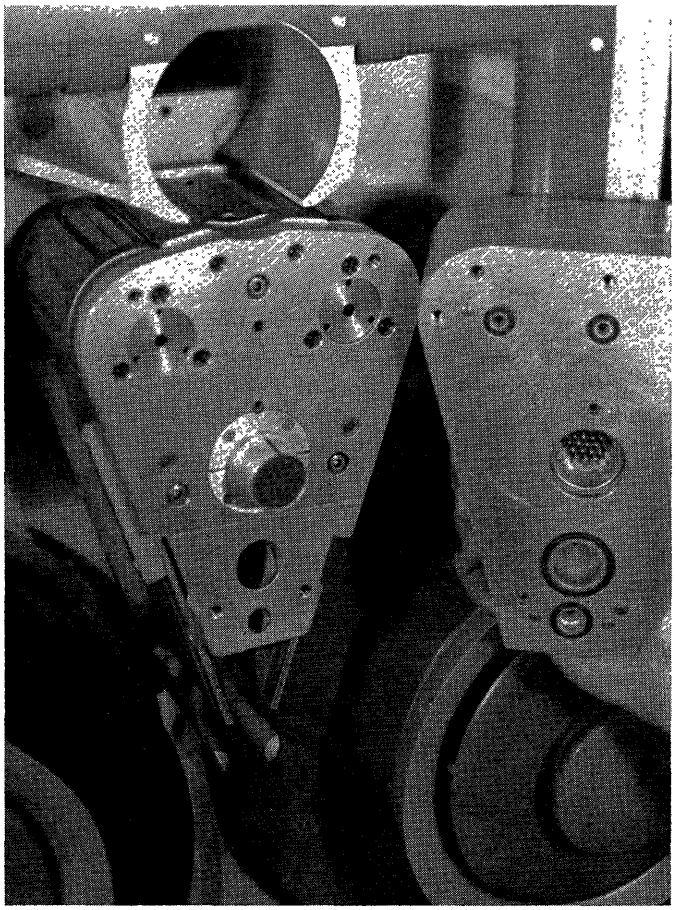


Fig. 8. Capstan assembly, with valve and actuator assembly removed. Note slotted surfaces of capstan

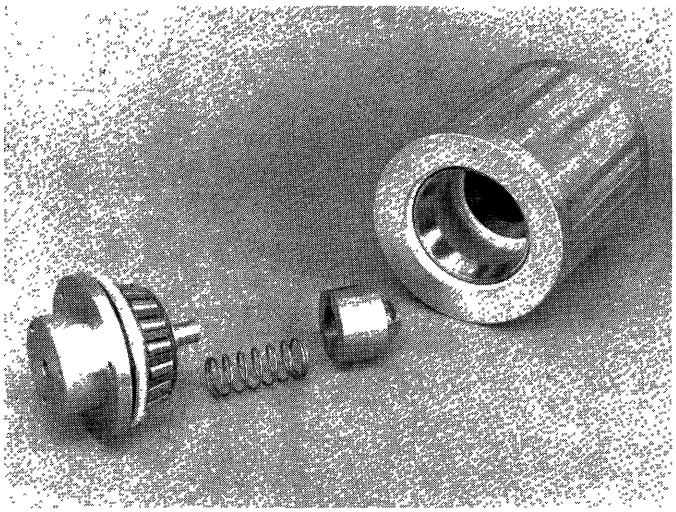


Fig. 9. Capstan, showing internal commutator

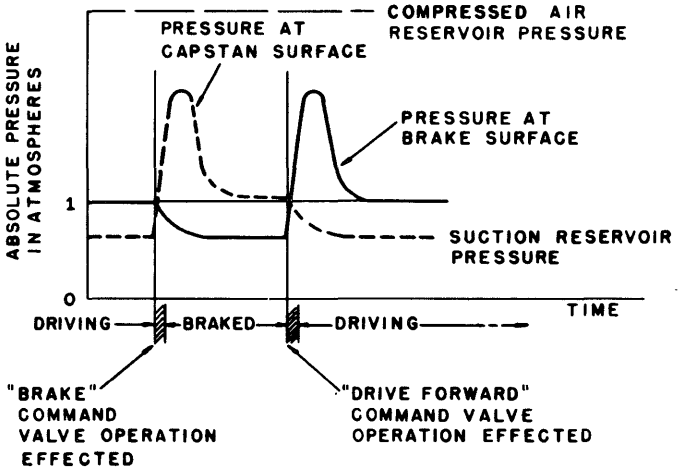


Fig. 10. Approximate pressure wave forms during a drive-brake-drive cycle

around the head, thus assuring good contact for reading and writing. The spacing between brake and head is several times as wide as the thickness of the tape however, so that edgewise insertion of the tape is very easy. Edge guides mounted on the brake provide accurate tracking of the tape in the vicinity of the head.

Adjacent to and beneath each capstan there is mounted a long flat inclined plate which is also equipped with edge guides. The top end of the plate is adjacent to the capstan and assists in separating the tape from the capstan. Since the plate is closely adjacent to the normal path of the tape it serves as a dynamic stiffener and oscillation damper for the tape in the vicinity of the capstan assembly.

Fig. 8 is a closeup view similar to Fig. 6 but with the valve and actuator assembly removed, and with the tape removed from the capstans so as to show the slotted surfaces which connect internally to the working air passages. The entrances to the two capstan air passages are visible as 1/4 inch diameter O-ring sealed apertures on the front of the valve mounting plate. A similar aperture leading to the brake is midway between the two capstan apertures. The medium size aperture exposed at the bottom is the line carrying compressed air to the valve and actuator assembly, and the larger hole immediately above is the connection to the vacuum reservoir.

A closeup view of a capstan and its internal commutator is shown in Fig. 9. The purpose of the commutator is to communicate vacuum to only that portion of the capstan about which the tape is wrapped. The circumference of the capstan is accordingly divided into segments each of which is connected to one passage on the commutator, and the number of commutator segments connected to the vacuum line at any one time varies between two and three as the capstan rotates.

Since a vacuum system is used for controlling tape motion and since compressed air is used in the valving arrangement, it is a simple matter to provide air lubrication for those capstan surfaces not in engagement with the tape. By this means friction, tape wear, and the generation of Mylar dust are greatly reduced. There is still another way in which controlled selective injection of compressed air into the capstan and brake is of great benefit. Consider the vacuum to be applied to the right-hand (clock-wise rotating) capstan so that the tape is moving to the right, in the forward direction. If it is now desired to stop, the vacuum is shifted to the brake member and disconnected from the right-hand capstan. In order to disengage the tape rapidly and affirmatively from the capstan a short puff of medium pressure air is blown into the right-hand capstan immediately following disconnection of the vacuum supply. This puff reaches the capstan and disengages the tape at essentially the same time as the vacuum newly applied to the brake causes the tape to be attracted to the brake. Transfer of the tape from engagement with the moving capstan to engagement with the stationary brake is thereby quickly accomplished without subjecting the tape to a tug-of-war between these two surfaces. Tape abrasion and the maximum stresses in the tape are accordingly greatly reduced.

Fig. 10 shows a typical cycle of operating pressures in a drive capstan and in the brake, as a braking operation and a subsequent start in the same direction are performed. Similar considerations apply to a braking operation followed by acceleration in the opposite direction.

Air/vacuum connections to the two capstans and the brake are controlled by three individual identical assemblies, each of which consists of two electrical actuators and a control valve. A schematic of one of these electro-pneumatic valves is shown in Fig. 11. Compressed air at approximately 35 pounds per square inch (gauge) is contained in a chamber with two compressed air exit ports, each of which is normally closed by the armature of an electromagnet. On the control valve sides these two apertures are adjacent to the two faces of a control vane, which teeters about a resilent fulcrum which also acts as a pressure sealing barrier. On the other side of the control vane a large passage equipped with a seal communicates to the vacuum reservoir, and another passage equipped with a seal at one end bypasses the sealing fulcrum barrier. A little consideration shows that two stable positions of the control vane are possible, with the holding force being supplied by the vacuum reservoir in both instances. Since the two positions of the control vane are stable, the valve is a mechanical non-binary flip-flop, and only a short puff of high-pressure air on the proper surface is required to effect a transition. These puffs of air are initiated by a short burst of current in the appropriate electromagnet, whose armature uncovers the aperture and allows air to escape from the compressed air chamber and impinge on the control vane.

Immediately after the vacuum is disconnected from a passage by driving actuator A' the partially spent compressed air is directed into the working air passage and thence to the capstan (or brake) providing the pressure blow off

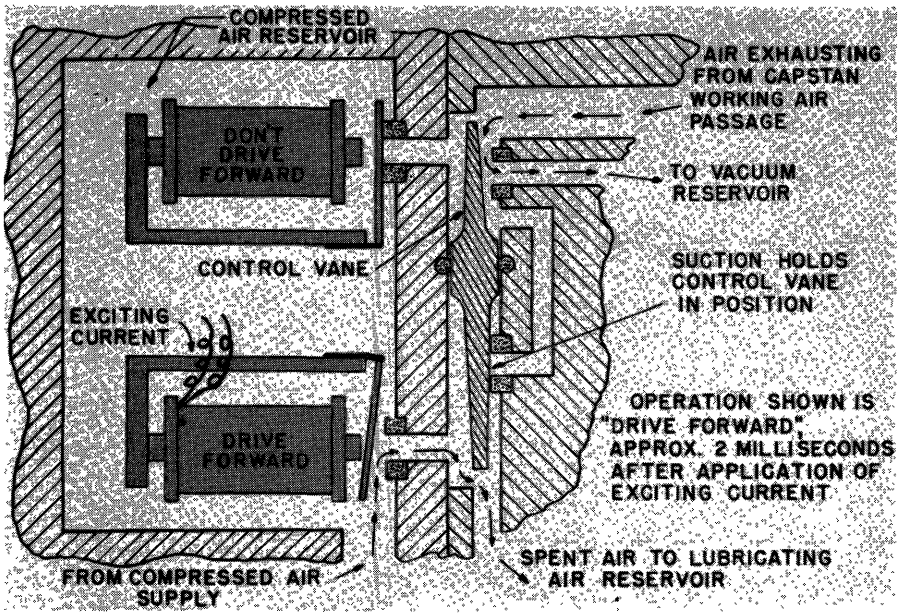


Fig. 11. Schematic of electro-pneumatic valve

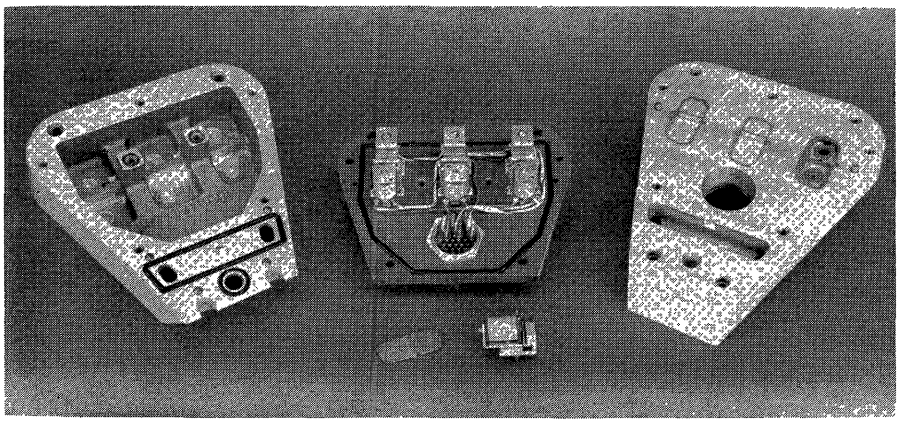


Fig. 12. Valve and actuator mechanism

described above. Spent air from actuator B' is conserved by leading it to the reservoir of low pressure air used for lubrication; the pressure of air in this chamber is regulated by a feather vane which controls the exhaust to atmosphere.

The principal components of the valve and actuator mechanism are shown in Fig. 12. The control vane is made of surface-hardened aluminum and fits into the cavity with a clearance of approximately 2 mils. Both in the mounting of the control vane and in the mounting of the relay armatures use is made of resilient pivots held in compression. Valve seats are of silicone rubber to avoid sticking when fast operation is required after a long interval of tight closure. The entire valve and actuator assembly can be removed from the capstan by unscrewing four easily accessible machine screws, and the chamber containing the actuators is similarly easily disassembled. Passages from the vacuum reservoir and the compressed air line are cast into the heavy aluminum housing, which serves both to contain the medium pressure compressed air and to shield the nearby magnetic heads and tape from the magnetic fields generated by the actuators. Since the actuators are driven in pairs the actuator connections are arranged so that the external fields in the vicinity of the head substantially cancel each other and cause no difficulty.

The power handling capacity of the actuator coils in this application is greater than ordinary since the coils are effectively cooled by the flow of compressed air which they control.

Fig. 13 shows a typical curve of velocity and distance, measured at the head, as a function of the time elapsed from the issuing of a brake command. Current from a low impedance hard-tube driver starts to flow within a few μsecs of the command and builds up with a time constant on the order of 0.7 millisecond. The actuator armature starts to move, uncovering the compressed air exit port, in slightly under 0.3 millisecond and the control vane is flipped to its new position in about 1.7 milliseconds. In rather less than 3 milliseconds the pressure at the under surface of the tape has changed sufficiently to start engagement (vacuum) or disengagement (pressure puff), and a brief period of tape deceleration ensues. As seen from the curve the tape comes completely to rest after having traveled a little over 0.3 inch from its location at the time the brake command was issued.

A similar record of the tape acceleration characteristics is given in Fig. 14, which also particularly shows the velocity of the tape at the time when a beginning block mark is normally encountered. In stopping, the tape comes to rest somewhat beyond the center of the available stop-start space. The available distance for acceleration is thus less when the original direction of tape motion is resumed, as shown in this figure; approximately 0.2 inch more is available if the tape restarts in the opposite direction.

It will be noted that the implementation is such that it is not necessary for a braking operation to be completed before a reverse direction or restart command can be accepted and acted upon. Detailed discussion of the actuator, valve, and tape motion as a function of the interval between brake and drive commands is, however, beyond the scope of this paper.

In preparing tape for use on DATA matic 1000 a complete inspection procedure is followed, using an equipment called the tape certifier, which is shown in Fig. 15. After laying down all of the block marks, including special block marks identifying the "end" and the "middle" of the tape (as indicated in Fig. 1) the block marks and the entire information space are inspected for playback adequacy and freedom from any imperfections which would prevent full and accurate recovery of recorded information. Block marks which are substandard or which surround information regions containing tape defects are magnetically erased so that at no time does the DATAmatic 1000 attempt to deposit information onto any tape location except those known to be fully up to standard. By this means, and without requiring any additional equipment in magnetic file units or central processor, a small defect rate in the manufactured tape can be tolerated, all defects being detected and

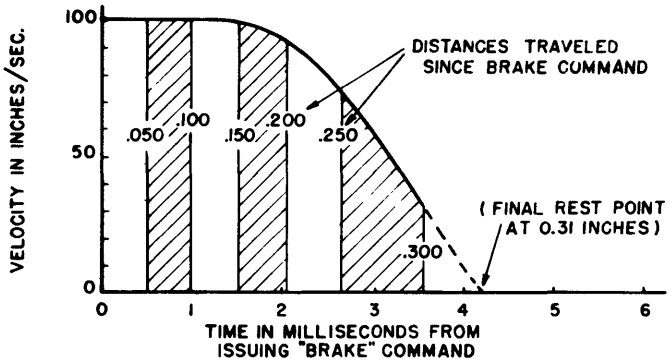


Fig. 13. Typical curve of velocity and distance versus time during braking operation

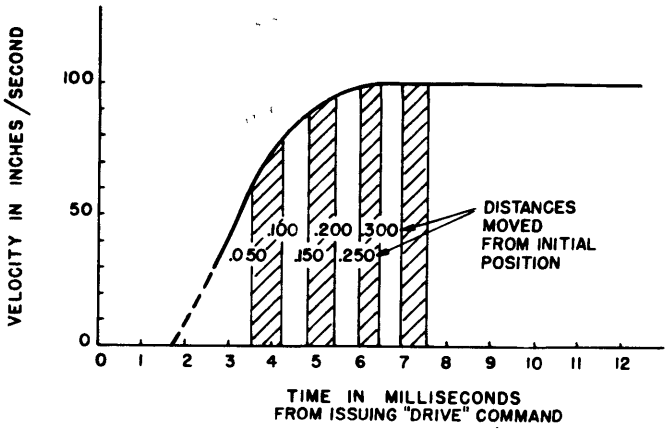


Fig. 14. Typical curve of velocity and distance versus time during a drive operation

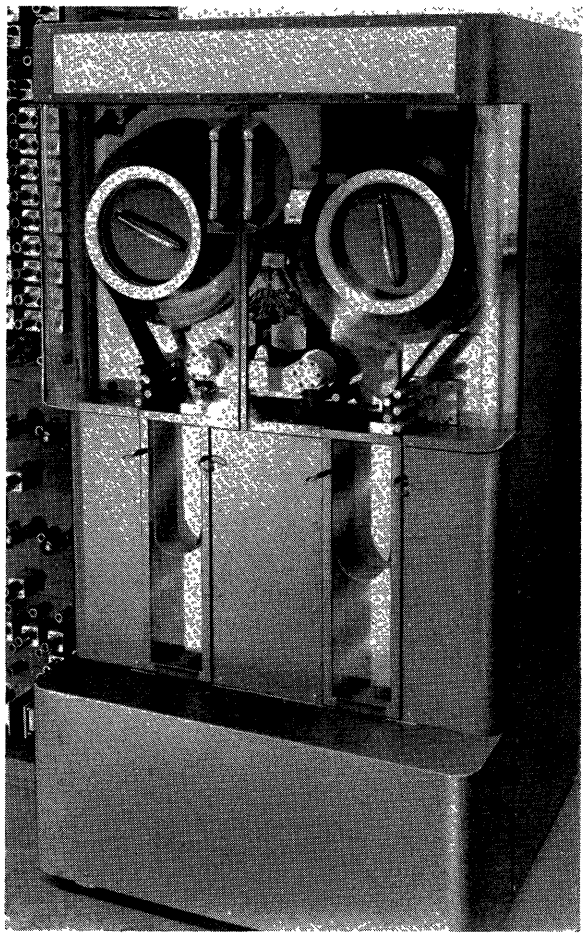


Fig. 15. Tape certifier

completely avoided in the finished "certified" tape. The inherent economies are obvious and important.

Space permits only a brief description of the remaining features of the tape handling mechanism. In conventional fashion pneumatic loop chambers are interposed between the capstan assembly and the tape supply and takeup reels. An innovation is the control of the reel servo motors by pneumatic contactors which derive their motive force from the loop chamber suction. Not only are the complications and time delays of electrical contactor arrangements thereby avoided, but because of the large viscous damping any contact bounce is automatically suppressed. In addition, fail-safe design guards against tape damage from loss of suction.

The tape mechanism sits adjacent to a companion unit containing preamplifiers switching relays and auxiliary gear, and the combination of the two units is referred to as a single magnetic file unit. All mechanisms in an installation are supplied with high-pressure air and subatmospheric air from a common pumping and manifold system. The enclosures of the tape handling mechanisms are acoustically treated. Gasketed double doors of transparent plastic provide visual observation and attenuation of the sound fields generated by the tape mechanism.

Reference

1. Proceedings of the Eastern Joint Computer Conference *AIEE Special Publication T-92* "A New Large-Scale Data-Handling System, DATAmatic 1000," **J. Ernest Smith.** May, 1957, pp. 22–28.

Discussion

W. A. Farrand (Autonetics Division of North American Aviation): What is the land area between channels? Why is this particular recording code used?

Dr. Lawrance: As given in the tabulation the channel width is 60 mils; the center to center spacing of channels is 82 mils and the land between channels is 22 mils. The recording system used is believed to be capable of very high fidelity in both the reading and the writing processes, because of the time modulation features of the system.

H. L. Gross (National Cash Register Company): Can one read or write successive blocks of information continuously without stopping and starting the tape after each block?

Dr. Lawrance: Yes, in fact, successive blocks of information are generally written or read continuously without any interruption of tape motion.

R. M. Gordon (Electrodata): May the tape be searched for a specific block? If the answer is yes, describe briefly the search procedure.

Dr. Lawrance: A channel of each block of information is devoted specifically to information that enables searching to be performed readily. The search procedure involves high-speed comparisons of the

identification of key information with the tape in continuous motion; in fact, this search may proceed simultaneously on ten tapes with all tapes in continuous motion.

R. A. Frontiero (International Business Machines Corporation): Does the DATAmatic system allow file searching and/or record searching within a file without reading all preceding files or records on the tape reel? If so, what method is used?

Dr. Lawrance: Only a small fraction of the information in each record, namely, the identification key, need be read in the search process. All satellite information is passed over without reading until the desired record has been reached.

N. Dean (Ramo-Woolridge): Is it possible to record selectively on the tape, i.e., write only selected blocks? Is it possible to read and write on the same tape on the same pass?

Dr. Lawrance: Selective recording on the tape is possible and, in fact, desirable in many DATAmatic-1000 applications. Consecutive intervals of reading and writing during a single pass of a given tape is definitely a permitted procedure in this system.

B. Scheff (Massachusetts Institute of Technology): Have there been any problems with tape stretching? If so, how have they been remedied?

Dr. Lawrance: There have been no problems with tape stretching due to operation of the capstans, brake, or reel servos. Even though the accelerations produced by the capstan and brake are of the order of 250 *g*, the mass of tape accelerated is so small that we remain safely below the elastic limit. The reel servo control setup has been designed to be essentially fail-safe, so that a triple failure is required before any danger of tape stretching is encountered. Furthermore, in the event of such a failure, a puff of compressed air is supplied to both capstans and to the brake, so that the tape is completely free to move through the capstan assembly.

J. K. Lewis (Department of Defense, Washington, D. C.): What is the thickness of the mylar cover film, and the thickness of oxide. Is it correct to assume that the head is in contact with the mylar cover film? Who makes the tape?

Dr. Lawrance: The thickness of the mylar overlayer is 1/2 mil, and the thickness of the oxide is also 1/2 mil. The laminating adhesive between the underside of the oxide and the 2-mil bottom layer of mylar is about 0.2 mils thick. This makes an overall thickness of approximately 3.2 mils. The head is, indeed, in contact with the top surface of the film. The tape is made for us by special arrangement with Minnesota Mining and Manufacturing Company.

H. H. Stein (Ferranti Electric-Canada): Are two channels used for block marks in order to eliminate erroneous readout of a mark due to noise or other tape defect? Is there ever a need for splices and, if so, do tape splices produce signals in the blockmark read amplifiers, which may be read as marks?

Dr. Lawrance: The double blockmark channels are employed in a special cross-checking function to verify the position of information on the tape. The need for splicing should be very rare, but splices do not induce spurious signals into the blockmark signals.

M. B. Stad (Remington-Rand Corporation): How does this sandwich tape compare in cost to "ordinary" coated tape? Do you have stretch problems or edge wrinkling due to 3 inches width?

Dr. Lawrance: The DATAmatic-1000 tape is more expensive initially than ordinary coated tape because of the more complex laminar construction. Each roll of tape released by DATAmatic must satisfactorily pass an exacting inspection process, such that the tape is certified to be error-free in all recording areas. No, the 3 inch width gives us no difficulty with stretching or edge wrinkling.

M. E. Montijo (Radio Corporation of America): Why was the electrostatic clutch principle in your mechanism abandoned?

Dr. Lawrance: At the stage progressed with the electrostatic clutch development, magnetic tape life was as yet too short to satisfy the performance standards of the DATAmatic-1000 system.

H. E. Van Winkle (International Business Machines Corporation): What type of reel servo is used?

Dr. Lawrance: The type reel servos used are 400 watt, 2 phase servo motors with two different gradations of dynamic braking. Sensing of the tape position is done by pneumatic elements which control the motor circuits directly.

M. Stein (National Bureau of Standards): Does the tape ever move faster than 100 inch per second during the first 8 milliseconds or shortly after while the servos are settling down?

Dr. Lawrance: Detailed evidence such as shown in Fig. 14 shows that over-speeding of the tape in the vicinity of the head is limited to a figure well within the capabilities of the read-write system.

Synchronization of a Magnetic Computer

J. KIELSOHN G. SMOLIAR

IN COMPUTER DESIGN the problem of communication between the central computer and the outside world is always present. This paper describes how this problem was solved for the Cambridge computer with a new type of shift register employing the Ferractor*, the magnetic core developed by Remington Rand Univac. The computer and the magnetic amplifiers which it uses were described in some detail in other papers. The shift register itself has many unique features, however, and the design and application merit a separate discussion.

The Cambridge computer is a magnetic device in the sense that all of the normal amplifying functions are performed with Ferractors. Germanium diodes are used for the logical operations of gating and buffing. Pulse shaping and delay are accomplished by the magnetic amplifiers, and therefore separate components are not needed to perform these functions.

The synchronizer of a computer must act as a link in both directions between the essentially uniform pulses circulating in the computer and the input and output pulses occurring at random. The Cambridge computer, although relatively restricted in input-output functions, still has many external communication paths. There are data links for real-time operation, an in-and-out paper-tape punch and reader, and a modified typewriter for input and output. Consideration of the typewriter only, however, will involve all of the fundamental principles of synchronizer operation.

Transfer of data from the typewriter is made through a shift register, *rO*, in which the ten characters of a computer word are assembled. The digits coming from the typewriter occur at random and in reverse order with respect to the sequence in which they are carried in the computer. In other words, an operator types the most-significant digit first, while the word is carried in the computer with the least-significant digit first, for the usual reason that the result of a carry may be recorded after the carry. The

J. KIELSOHN and G. SMOLIAR are with Remington Rand Univac, Division of Sperry Rand Corporation, Philadelphia, Pa.

The work reported here was sponsored by the Air Force Cambridge Research Center under contract AF 30(602)-1055.

* Trade-mark, Sperry Rand Corporation.

sign of a word is stored separately during computing, and, even though it is part of the word-pulse sequence within the memory, it presents no special synchronizing problems and it will not be discussed here.

Before discussion of the actual circuit of the shift register used for data transfer, the magnetic amplifier from which it is derived will be described. In the simplest form, this amplifier consists of two windings on a toroid of square hysteresis-loop magnetic material. A pulse applied to the input will bring the core from the normal state of plus B_r to the opposite point on the hysteresis loop, minus B_r; see Fig. 1. The core will then present a high impedance to a power pulse, and the power pulse will return the core to plus B_r without producing appreciable output. If there is no input pulse, the core stays at plus B_r for the entire input period, and the power pulse, encountering a low impedance, produces an output pulse; see Fig. 2.

Since the power required to flip the core is much less than the power that can be

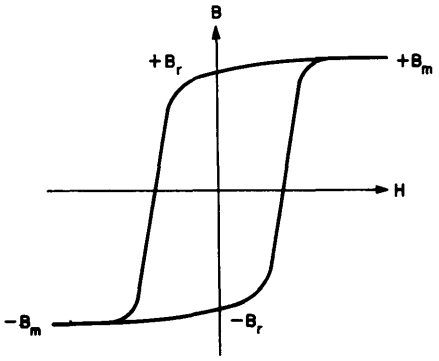


Fig. 1. Hysteresis loop

sent through the output winding, the device is an amplifier, and it is easy to see that the core also reshapes and delays the pulses as in Fig. 2. This circuit, with only minor modifications, is the one that is most frequently used in the Cambridge computer. It complements the information; that is, it substitutes pulses for no pulses and vice versa. The circuit is modified to make a true amplifier by the addition of a bias winding which carries direct current and which is phased opposite to the input winding; see Fig. 3. In the amplifier, an input pulse brings the core to plus B_r, so that the power pulse finds it in the low-impedance state, while during the absence of an input pulse the bias current drives the core to minus B_r, with the result that the succeeding power pulse will produce no output.

Recirculating registers may be made by cascading strings of these amplifiers and connecting the output of the string back to the input. However, for the assembly and transfer of asynchronous information a true shift register is preferred; that is, a component which can hold the information in an essentially static form or circulate it, either at computer rate or at one pulse space at a time. The Cambridge computer shift register is based on the noninverting amplifier described above. It has two input-circuit differences and one difference in operation timing. Fig. 4 shows the shift-

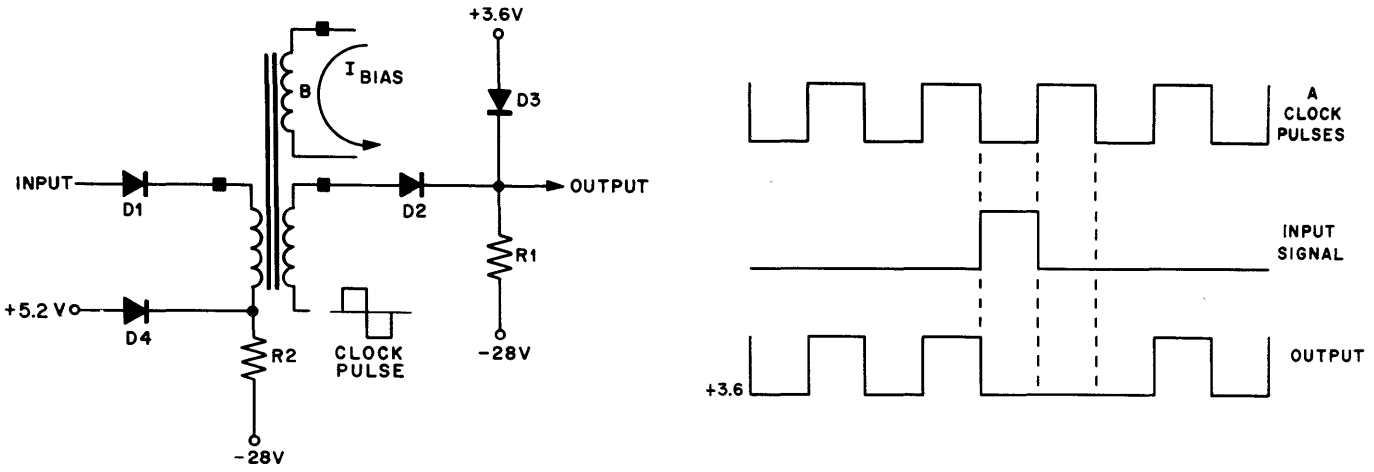


Fig. 2. Complementing magnetic amplifier

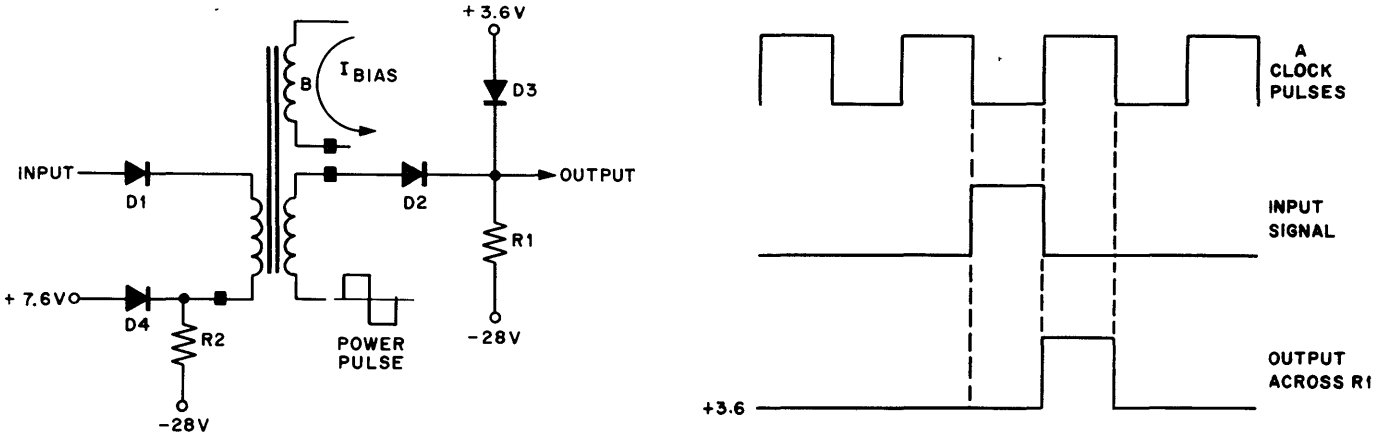
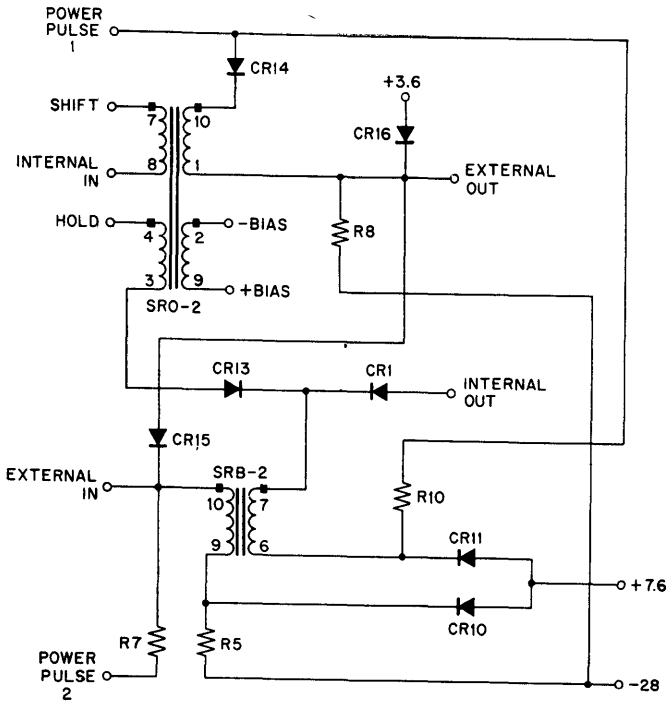


Fig. 3. Noncomplementing magnetic amplifier



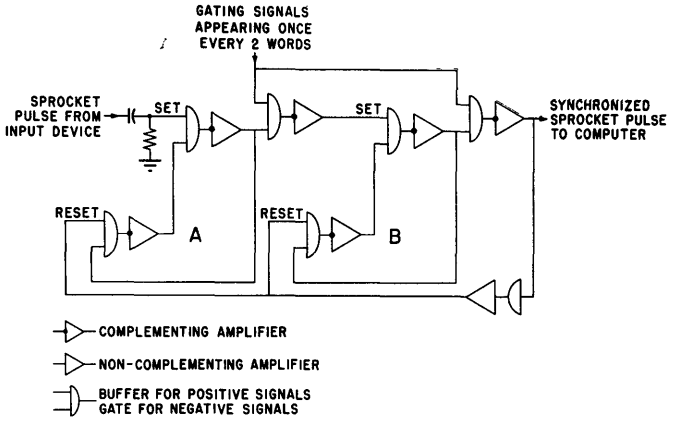


Fig. 4 (left). Shift-register circuit

Fig. 5 (above). Synchronizer logic

register circuitry. Note that there is an additional input winding for each amplifier, and a second core (besides the amplifier) with two windings for each bit of information.

While the shift register operates with the same timing as the rest of the computer, the action is in three steps instead of the two steps, input and power, of the simple amplifiers. Information enters the shift register through the lower Ferractor, shown in Fig. 4, which is called the blocking core. A pulse applied at the external input terminal makes the blocking core a low impedance. One half-cycle later an interrogating pulse in the hold winding tries to send current through both cores. If the blocking core has been brought to low impedance by the input, the hold pulse brings the amplifying or output core to plus B_r, so that on the third half-cycle the power pulse will produce an output. When the shift register is used for static information storage, a series of hold pulses causes the information to circulate back and forth between the output and the blocking cores. The output of the upper core is connected through a diode to the input of the lower core; see Fig. 4. If no shift or hold pulses are applied for 1 cycle, the register is cleared, since the bias resets the output core and the negative excursion of power pulse 2 resets the blocking core. Shifting is accomplished by reading into an output core from the preceding blocking core, rather than from the one shown directly below the output core in Fig. 4. In this way, a series of shift pulses will move the information through the register at computer rate. Interconnection of shift-register stages is accomplished by joining the *internal out* to the *internal in* terminal of the stage immediately to the right. In these circumstances, information would move from left to right. Obviously, either direction could have been chosen, or, if both were needed, one more winding on each output core and one more diode at the *CR13-CR1* junction would suffice. In operation both left and right shifts are needed, but, since plenty of time is available, the left shift is accomplished by moving the information ten places to the right in the 11-bit loop. Information can enter the computer in parallel through all of the external input terminals, or serially through any of the terminals with a series of shifts. It can be read out in either form as well.

The operator register of the Cambridge computer, which is used for most input-output operations, consists of 4 loops of 11 bits each, each loop containing one of the 4 bits of a character. All entries in the register are made at the most-significant digit position. Information from input devices is presented to the computer in the form of five bits (the fifth being a parity bit for checking purposes) and a sprocket. Since the sprocket appears at an arbitrary time and must trigger logical operations in the computer, it must be shaped to a computer-size pulse and properly timed. The sprocket pulse is shaped through a resistance-capacitance

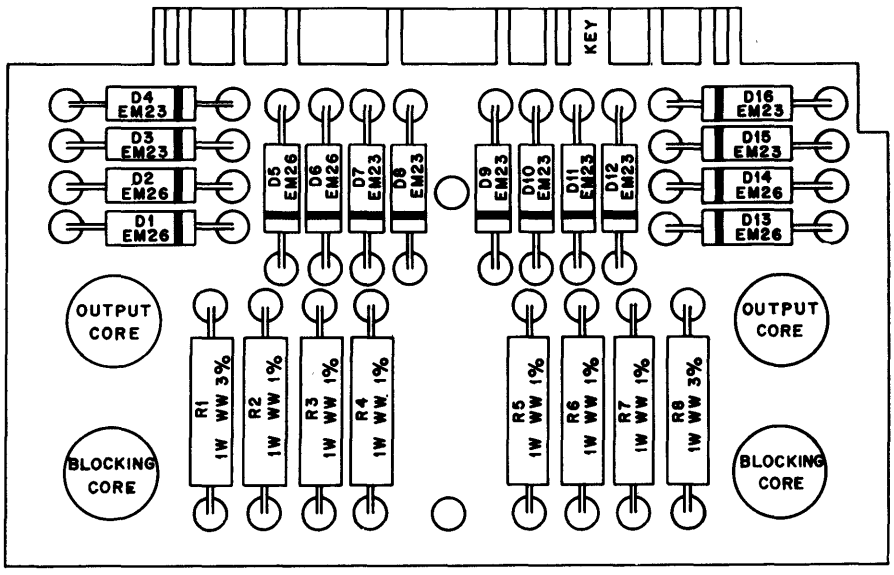


Fig. 6. Shift-register package

network so that it is longer than 3 computer-pulse times but shorter than 2 word times or 24 computer-pulse times. This pulse then sets flip-flop A (Fig. 5), and shapes the sprocket to computer-pulse size. To time the pulse is the function of flip-flop B; see Fig. 5. At the proper time the state of flip-flop A is sampled. The flip-flop may be set, partially set, or reset. The result of this sampling is placed in flip-flop B. If flip-flop A was fully set, flip-flop B will be fully set, but if flip-flop A was in the process of being set, a partial set will be passed to flip-flop B. (It is the possibility of a partial set in flip-flop A that makes flip-flop B necessary.) The partial set is allowed to recirculate in flip-flop B long enough to cause the partial set to either disappear or build up to full size. The result is then sampled and either a full-sized sprocket or no pulse is obtained. If no pulse is received, a second sampling of flip-flop A is made which will always result in a full set of flip-flop B, and (at the end of the waiting time) a full-sized sprocket. Generation of the sprocket clears flip-flops A and B, allows the four information bits of the input data to be placed in the most-significant position of rO, and starts rO shifting to the right ten places. Since the register is 11 digits long, the information is now in the least-significant position. This arrangement ensures that the computer will operate on the least-significant digit first. The computer is now ready to accept another input character.

This operation can be terminated either by a special fill character or by a counter which keeps track of the number of characters in the word. Then, by means of a full word of shift pulses, the information, which is now in computer sequence, goes out of the register at computer rate, and the transfer operation is complete.

Like most of the computer components, the shift registers are made up of standard printed-wiring cards, which are interconnected by means of the backboard wiring of the machine. Fig. 6 shows the shift register on a single card which holds four cores and the associated circuitry; that is, 2 bits of shift-register storage.

The versatility of the shift register makes testing of it in the computer very simple. In normal sequence of testing, operation of the typewriter is checked out and then used to generate the characters to fill the shift register. Operation of the register is observed when it is holding information in static form and when it is continuously shifting. A check is made to see that the characters are correct and that they can be cleared out by dropping the hold and shift lines.

Maintenance experience on these components has been very satisfactory to date. Another example of the excellent reliability of Ferractor magnetic-core amplifiers.

TX-0, A Transistor Computer with a 256 by 256 Memory

J. L. MITCHELL K. H. OLSEN

Synopsis: TX-0 is a high-speed digital computer which was built at Lincoln Laboratory to demonstrate and operationally test 5-megapulse transistor circuitry and a 65,536-word magnetic-core memory. The word length is 19 bits; 1 bit is a parity check bit for memory, 16 bits are assigned to memory addressing, and the 2 remaining bits are used to select among three memory-reference instructions and one micro-programming instruction. The logic is performed by standardized packages using surface barrier transistors. Fig. 1 shows TX-0 with the arithmetic element just beyond the console and the memory on the far left. Part I of this paper covers the TX-0 memory, and Part II the TX-0 circuitry.

Part I, The TX-0 Memory

THE TX-0 MEMORY, Fig. 2, is a high-speed, random-access, coincident-current magnetic-core unit with a storage capacity of 65,536 19-bit words. The bits in the word are read out in parallel, and the cycle time is 7.0 μsec (microseconds). (Cycle time is defined as the time between successive read operations.) Two 256-position magnetic-core switches are used to supply the read and write current pulses to selection lines. The memory system contains 425 dual triodes and 625 transistors. It is interesting to note that the presently available 4,000-register magnetic-core memories use almost as many active elements as are used in this 65,000-register memory. The memory was designed both electrically and mechanically so that the word length can be expanded to 37 bits. Two co-ordinates are used to select a register during the read operation, and three co-ordinates are used for writing. A 2 to 1 current selection ratio is used. A block diagram of the memory system and the timing diagram is shown in Fig. 3. The basic operation of this type of memory system has been adequately described in the literature and will not be repeated here.[1]

Memory Array

The memory array contains $1\frac{1}{4}$ million ferrite cores which were manufactured at the Lincoln Laboratory. The outside diameter of the core is 80 mils, the inside diameter 50 mils, and the height 22 mils. When driven with an 820-milliampere current pulse, the cores switch in 1 μsec and give a peak output voltage of 100 millivolts. The cores used in this memory have a somewhat greater signal-to-noise ratio than available commercial cores. The cores are wired into 64 by 64 subassemblies, each subassembly being a complete operating memory plane with its own sense and digit winding. The same winding configurations are used in the 64 by 64 subassemblies as were used in the previous memories built at the Lincoln Laboratory.[2] Sixteen 64 by 64 subassemblies are assembled in a square array and connected together to form each 256 by 256 plane.[3] The choice of a 64 by 64 subassembly size was a compromise between the number of soldered connections in the 256 by 256 plane and the ease of construction and test of the subassemblies.

The digit-plane winding in each 256 by 256 plane is divided into quarters, each quarter being made up of the digit winding of four subassemblies connected in series as shown in Fig. 4. Each quarter looks like a delay line with a characteristic impedance of 150 ohms

J. L. MITCHELL, author of Part I, and K. H. OLSEN, author of Part II, are with Massachusetts Institute of Technology, Lincoln Laboratory, Cambridge, Mass.

The research in this paper was supported jointly by the Army, Navy, and Air Force under contract with the Massachusetts Institute of Technology.

Fig. 1. TX-0 computer

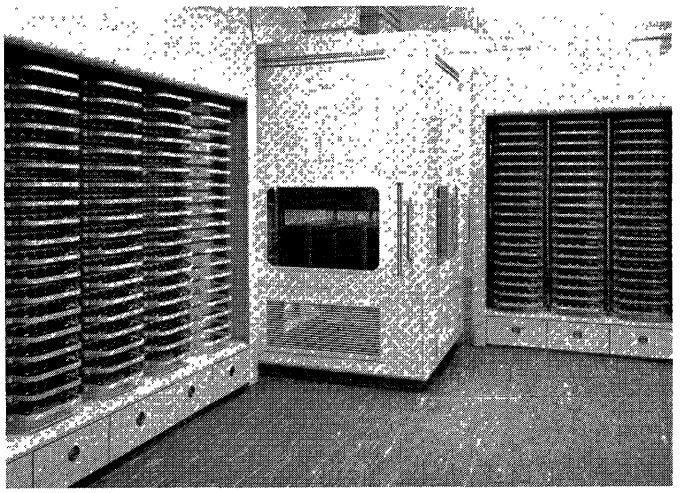


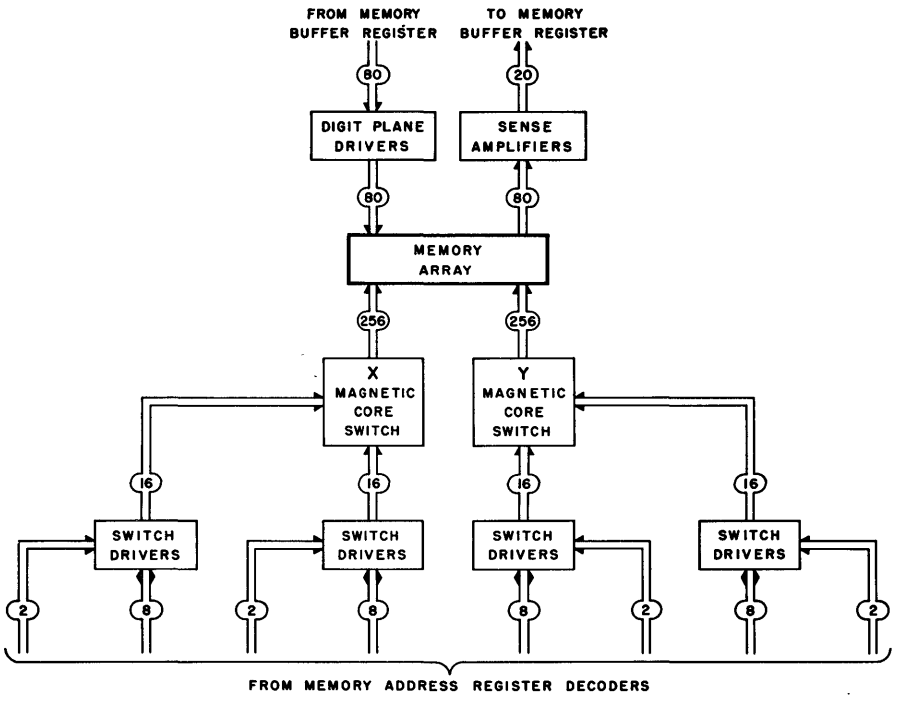
Fig. 2. TX-0 memory

and a delay time of 0.4 μsec. The choice of connecting only four subassemblies in series is a compromise between delay time and equipment. Any increase in digit-plane winding delay would result in an increased memory cycle time; for example, using one digit-plane winding per 256 by 256 plane would add 2 μsec to the cycle time.

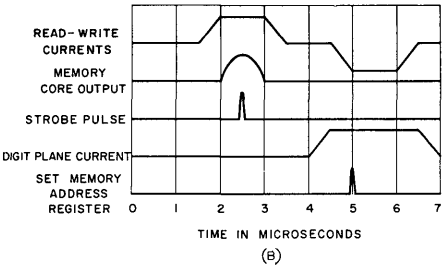
It should be noted that during the operation of the memory, it is practical to drive only one of the digit-plane winding quarters in a given 256 by 256 plane at any one time. When a pulse of current is supplied to the digit-plane winding the resultant voltages cause transient currents to flow through the interwinding capacities from the digit winding to the X, Y, and sense windings. If the quarters of all the planes are driven at once, the currents flowing through the interwinding capacities are of sufficient magnitude to cause distortion of the digit-plane current pulse, and to create undesirable transients on the sense winding. When only one of the digit-plane winding quarters is pulsed at a given time, these effects are not harmful.

The sense winding in a 256 by 256 plane is also broken up into four sections, each section consisting of the sense windings from four 64 by 64 subassemblies. The subassemblies on a given sense winding are connected in such a manner that no two subassemblies on the same sense winding section are common to the same X or Y drive line; see Fig. 5. It should be noted that with this method of connection the voltage induced in the sense winding by the half-selected cores is equal to that induced in a 64 by 64 memory.[4] Each sense winding is also a delay line. To reduce the delay and resultant signal distortion, the four subassemblies on a given sense winding section are connected in series parallel as shown in Fig. 3 rather than in series. Of course, this type of connection halves the signal amplitude seen at the output terminals of the sense winding section.

Twenty 256 by 256 planes are stacked on $^1/_2$-inch centers and the X and Y wires are connected in series to form the complete memory array; see Fig. 6. Nineteen of the planes are used, and the 20th plane is retained as a spare. The total dimensions of the memory array are 31 by 31 by 10 inches. The X and Y windings are also delay lines, with a characteristic impedance of 150 ohms and a delay of 0.15 μsec. It is interesting to note that the delay time for each



(A)



(B)

Fig. 3(A). Block diagram, 256 by 256 Memory. 3(B). Memory timing chart

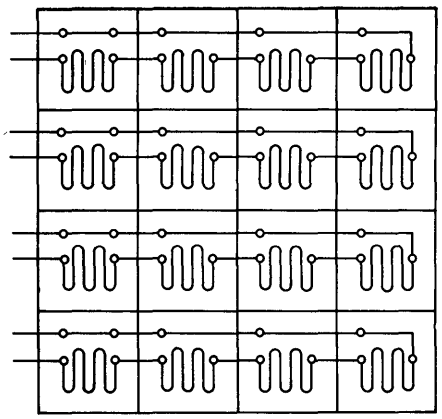


Fig. 4 (left). Digit-plane winding connection schematic, 256 by 256 memory plane

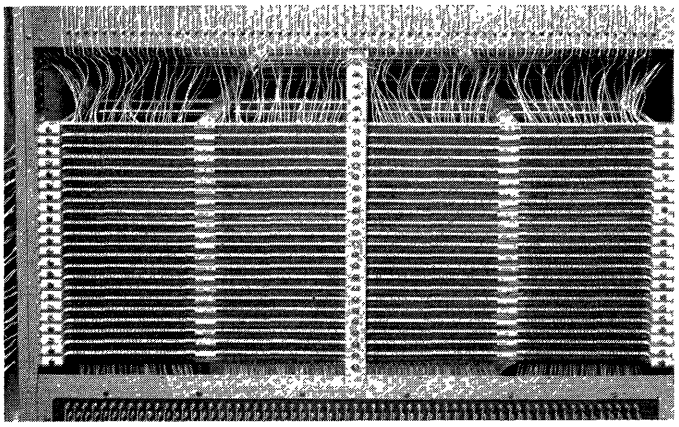


Fig. 6 (right). Memory array

of the various types of winding in the memory is roughly 0.1 μsec per 4,000 cores.

Magnetic-Core Switches

Each magnetic-core switch is made up of 256 tape-wound cores, each core containing 100 wraps of 4-79 Mopermalloy tape $^1/_4$-mil thick and $^1/_4$-inch wide, wound on a bobbin with an inside diameter of $^1/_4$ inch. Four windings are placed on each core: two 12-turn drive windings, a 16-turn output winding, and a 2-turn bias winding. These cores are connected into a square array to form a 2-co-ordinate switch. The operation of the switch is shown in Fig. 7. All the cores in the switch are biased to point A with a d-c bias current. The application of either the u or v current pulses alone does not switch a core. The application of u and v together to a given core causes the core to switch and generate a 410 milliampere read current pulse at the secondary. When the u and v pulses end, the bias current switches the previously selected core back to point A, generating the write pulse. The selected core is allowed to switch completely. The cores in the switch were selected for uniformity of open-circuit output voltage and switching time. The switch was wound as a current step-down device in order to match the characteristics of the driver tubes to that of the 150-ohm X and Y selection lines. All current outputs from the switch are uniform within 5%.

Circuits

The switch driver circuit used to drive one co-ordinate of a switch is shown in Fig. 8. A particular line in the switch is selected by first grounding one of the grid input lines and then pulsing one of the current regulators. For example, to select line O, grid input O is grounded and current regulator input O is pulsed. The current regulators hold the current constant to within 3% over the life of the tubes.

The digit-plane driver circuit is shown in Fig. 9, and it is similar to the current regulator in the switch drive circuit. Four such circuits are associated with each 256 by 256 plane, one for each quarter of the digit winding.

The sense amplifier circuit is shown in Fig. 10. The specifications on the sense amplifier are as follows: it must accept

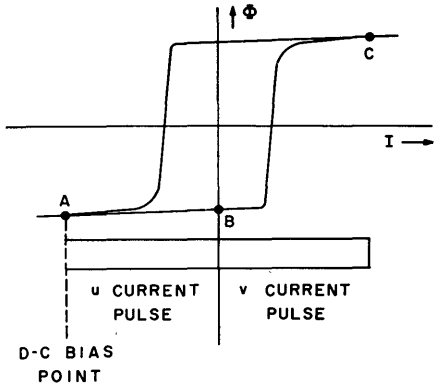
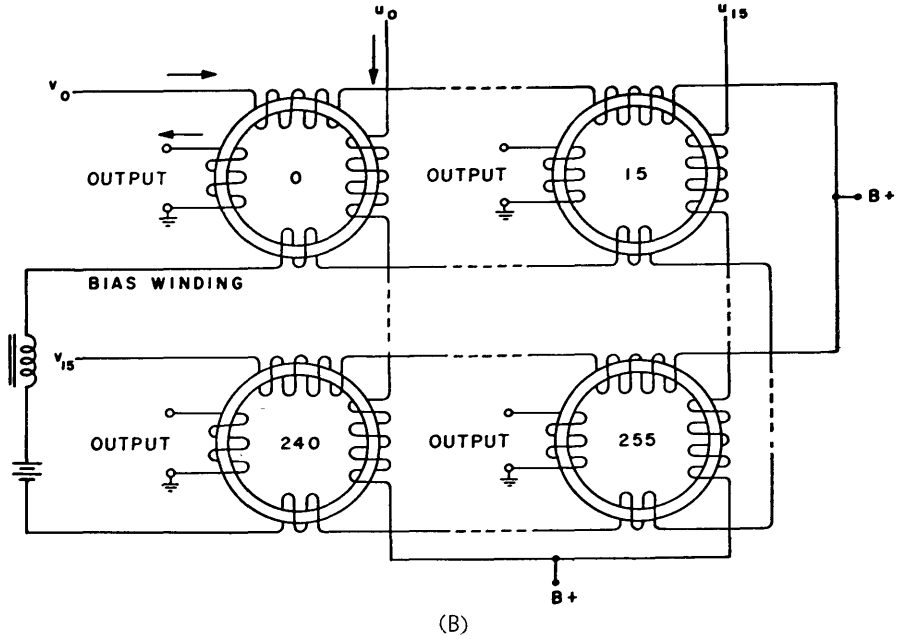


Fig. 7(A) (right). Operation of switch core. 7(B) (below). Schematic, magnetic-core switch



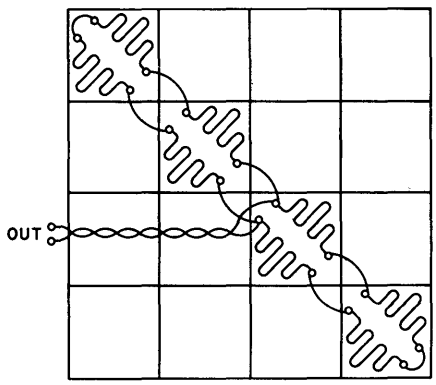
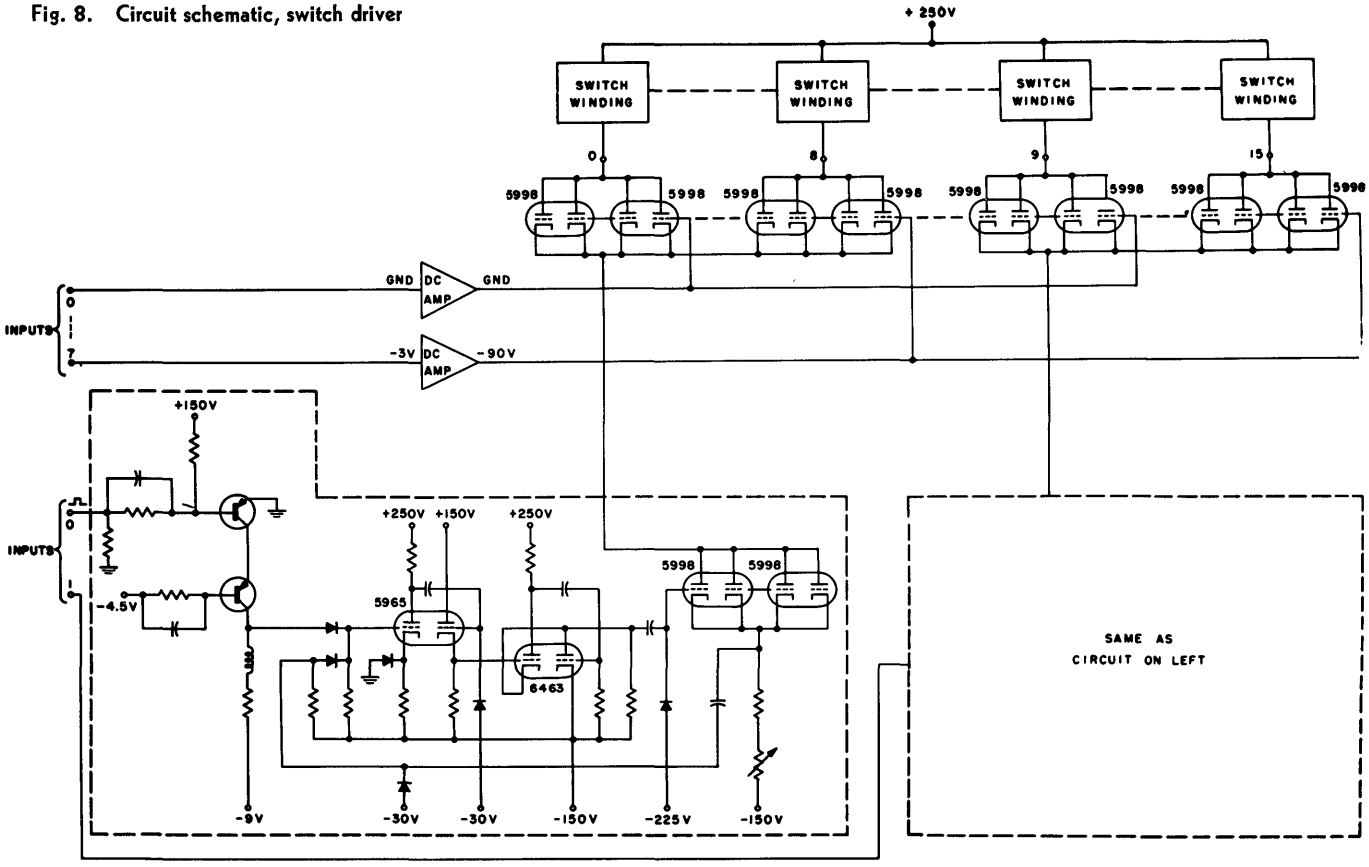


Fig. 5. Sense-winding connection schematic for one sense-winding section, 256 by 256 memory plane

Fig. 8. Circuit schematic, switch driver



bipolar input signals, it must have balanced input and must reject common-mode signals, it must not block when hit by large voltage transients, it must accept a train of unipolarity signals, and it must have constant gain over reasonable periods of time. The circuit shown meets these specifications satisfactorily. The unwanted signal due to voltages from half-selected cores and *zeros* is sliced out by applying the proper bias voltage to the center tap of the secondary of the transformer. The transformer bias voltage can be varied to give a measure of the signal to the noise ratio of the signal coming out of the sense winding. This is the method used to determine the margins of the system. The amplified input signals are mixed and rectified in the emitter-follower circuit, and then further amplified in the pulse-amplifier section to a voltage of 3 volts if a *one* was read out and to zero volts if a *zero* was read out of the memory plane. The signal is transmitted to the memory buffer register where it is sampled with a 0.1-μsec strobe pulse. One 4-input sense amplifier is associated with each 256 by 256 plane.

Results

The memory system has been under test in the TX-0 computer for several months with very satisfactory results. A number of the parameters of the system have been plotted versus the sense-amplifier transformer bias voltage. One of the most important plots is shown in Fig. 11. In this test the current in one switch-driver current regulator was varied, and the sense amplifier transformer bias voltage to all 19 sense amplifiers was varied until an incorrect read-out occurred. The test program used shifts itself through all memory addresses. It is as "tough" on the memory margins as an average program. When the switch drive current is varied, the amplitude of the read current pulse and the amplitude and shape of the write current pulse are changed; the switch drive current is therefore one of the most

(*Continued on p. 98*)

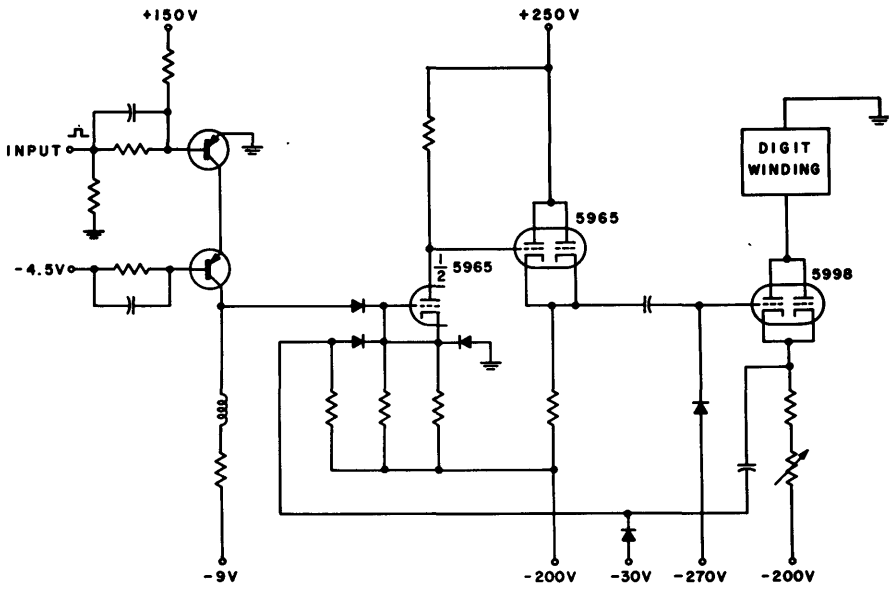


Fig. 9. Circuit schematic, digit plane driver

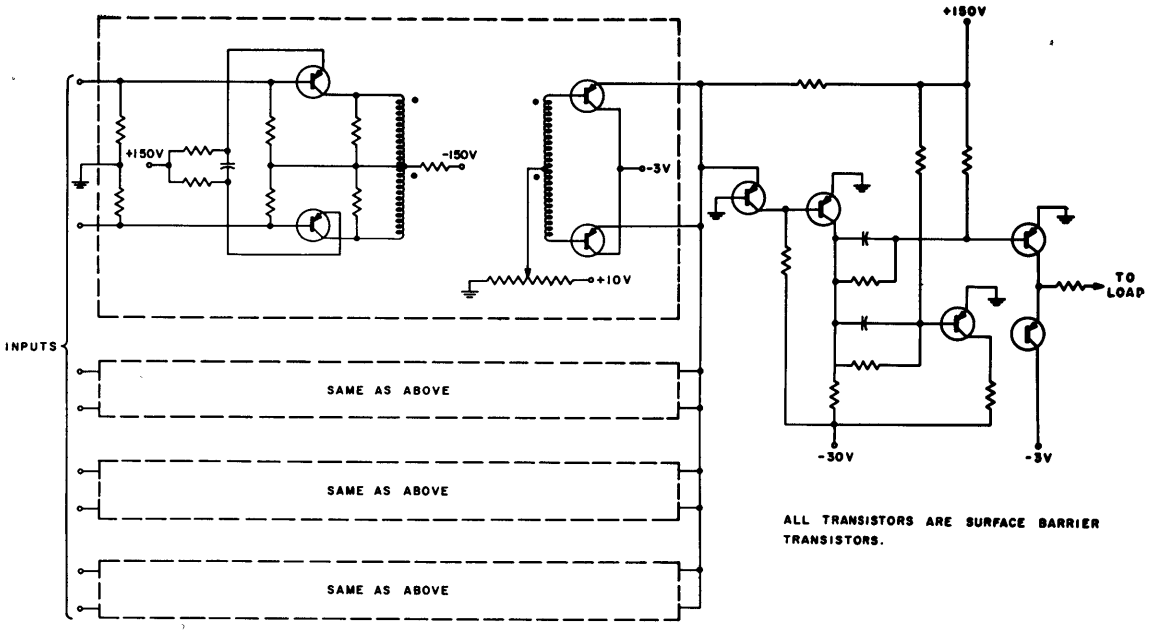


Fig. 10. Circuit schematic, sense amplifier

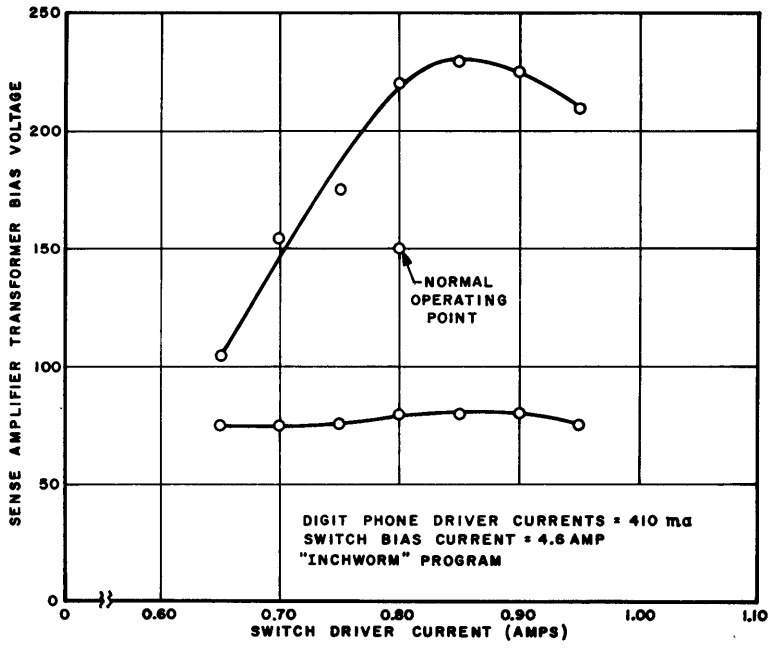


Fig. 11. Switch driver current margins

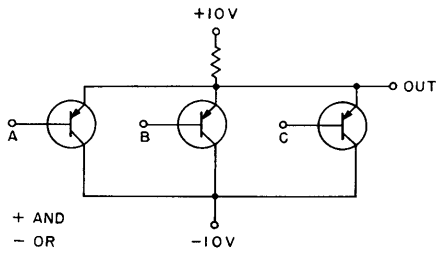


Fig. 13. Parallel emitter followers

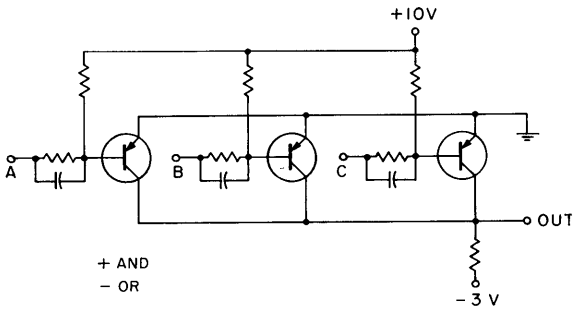


Fig. 14. Parallel inverters

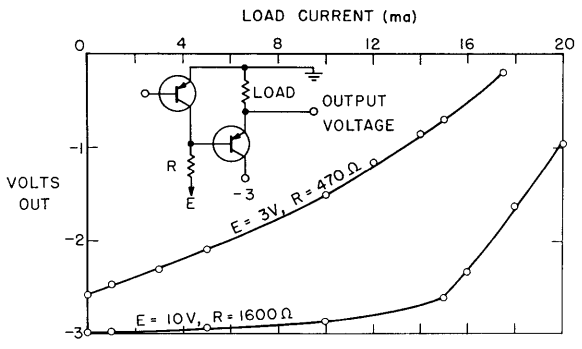


Fig. 12 (left). Saturated emitter follower

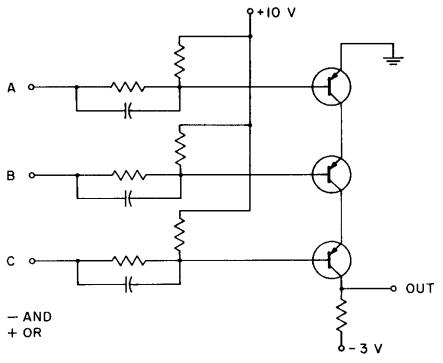


Fig. 15 (right). Series inverters

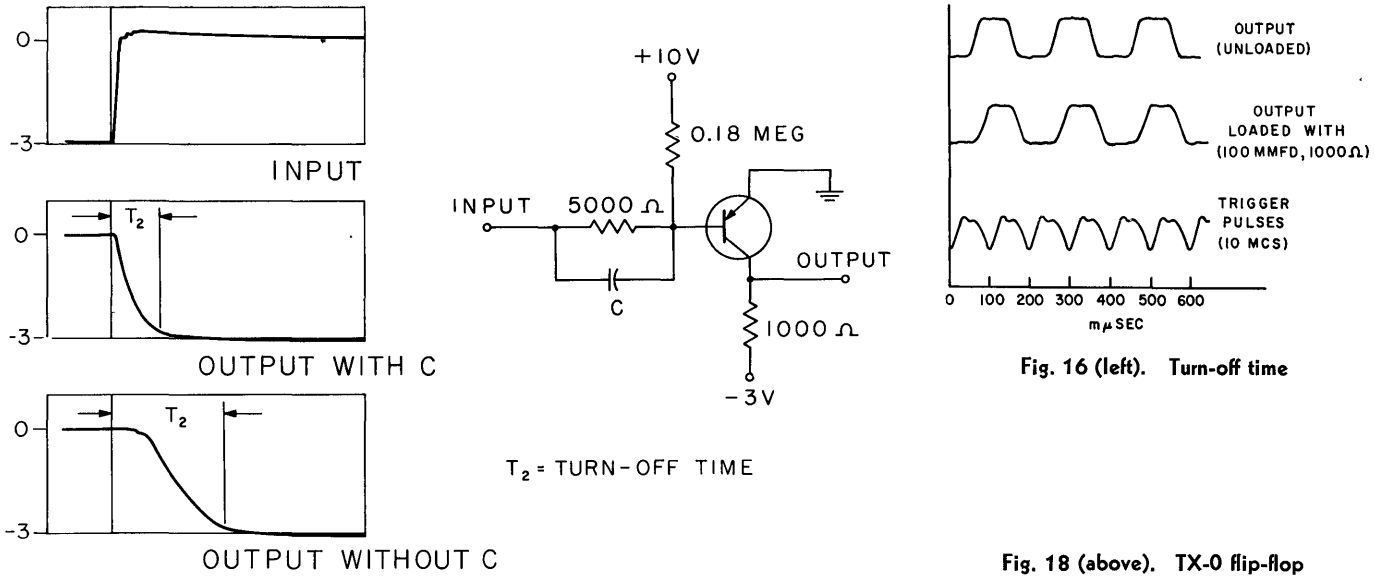


Fig. 16 (left). Turn-off time

Fig. 18 (above). TX-0 flip-flop

critical in the system. The upper curve in Fig. 9 corresponds to failure to read out a *one* and the lower curve represents failure to read out a *zero* correctly. The margins shown are comparable to those obtained on the 4,096-word MTC memory at the Lincoln Laboratory.

During the coming months the word length of the memory will be increased to 37-bits to bring the total storage capacity to 2.5 million bits, and the memory cycle time will be reduced to 6 μsec.

Part II, TX-0 Circuitry

Reliability has been one of the promised advantages of transistors in computer circuits, and indeed it has proved to be so. Reliability has come largely from the gross reduction in the number of parts, and from the expected long life of the transistors. But, in addition to reliability, it is found that transistors also can give improvements in speed and tolerance to parameter variations, and that they lend themselves to standardized building blocks.

Faster circuit speed is not a result of the fact that transistors are faster than vacuum tubes, for as yet they are not, but because they operate at much lower voltage levels. A vacuum tube takes a signal of several volts to turn it from fully ON to fully OFF but a transistor takes less than one volt to do this.

Tolerance to parameter variations is the result of being able to saturate the transistor. Unlike vacuum tubes, which always need an appreciable voltage across them for operation, an ON transistor can have almost no voltage across it. In fact, it can be usually considered as a switch that is either open or closed. This feature of the transistor makes possible very simple and very stable circuits.

Standardized building blocks are practical because of the small number of types of circuits required in a system, and because of the large driving capabilities of the saturated transistor. Even though the rated power dissipation of the transistor may be low, it can drive a large load because there is so little voltage across a saturated transistor.

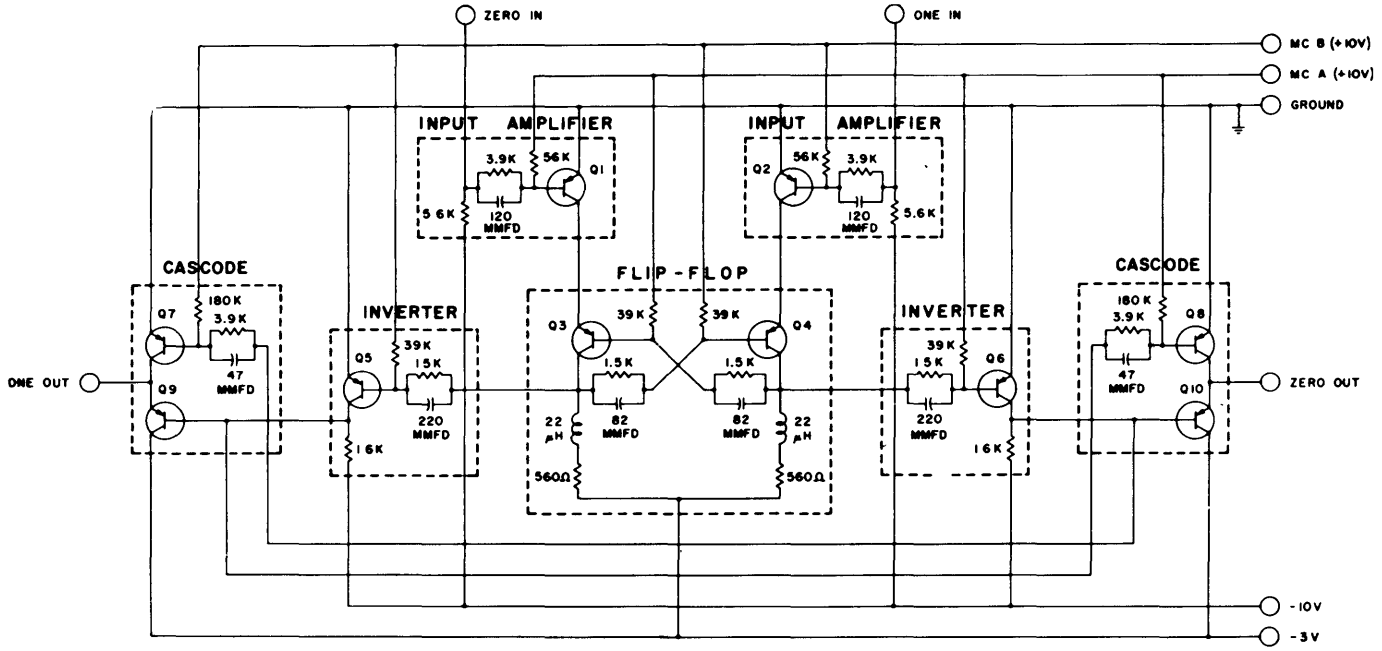


Fig. 17. TX-0 flip-flop

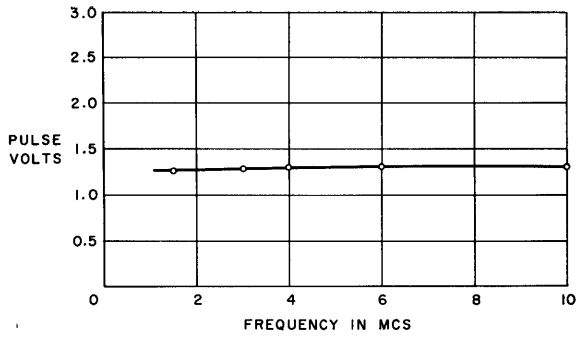


Fig. 19 (left). Trigger sensitivity

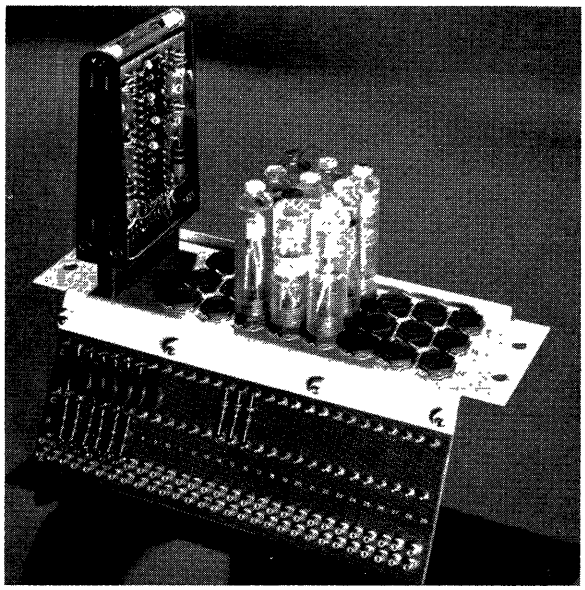


Fig. 22 (right). TX-0 mounting panels

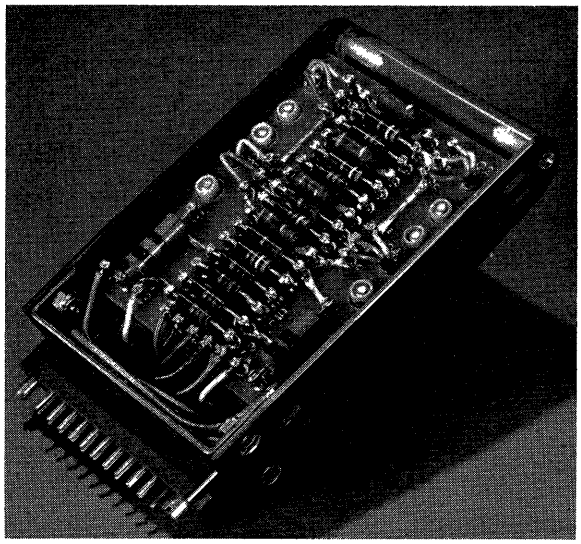


Fig. 20 (left). TX-0 flip-flop

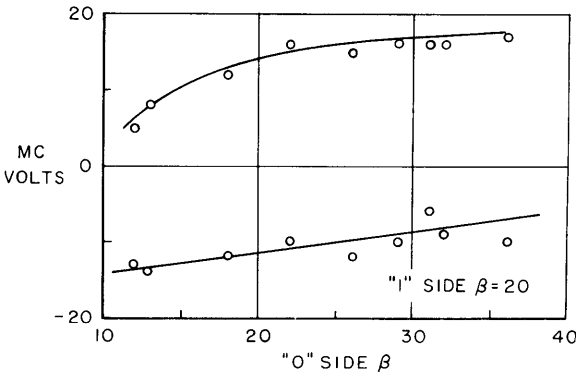


Fig. 23 (right). Beta margins

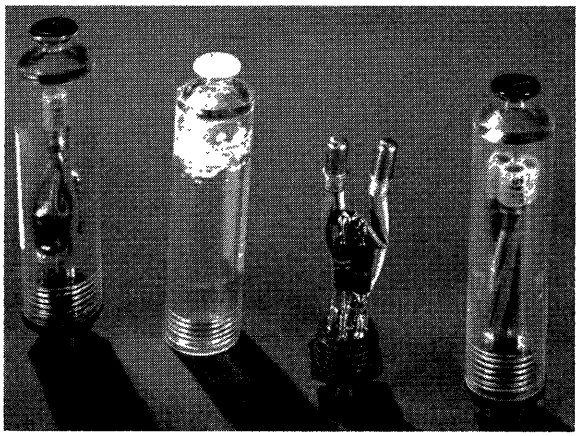


Fig. 21 (right). TX-0 logic units

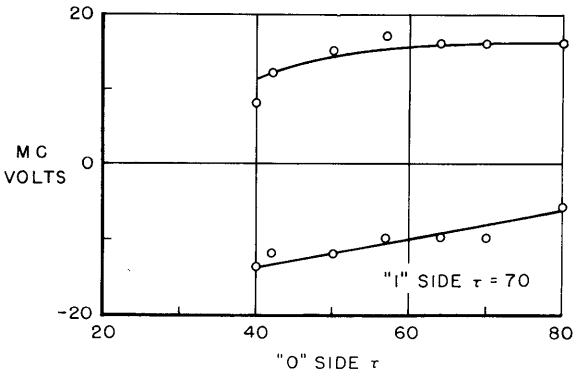


Fig. 24 (right). Tau margins

Circuit Types

There are two general circuit configurations in TX-0: the saturated inverter, and the saturated emitter follower. When a transistor in these circuits is saturated or ON there is only about 0.1 volt across it, so that an ON inverter clamps its output to ground and an ON emitter follower clamps its output to the supply voltage.

The saturated emitter follower is, in general, driven by an inverter as shown in Fig. 12. The output voltage as a function of load current is plotted first with R returned to the −3 supply to show the characteristic of an unsaturated emitter follower, and then with R returned to −10 to show that the output voltage remains almost constant with load variations for a saturated emitter follower. R was changed to keep the inverter current the same in both cases.

Transistor networks are used to perform logical operations. Emitter followers are combined in parallel to form noninverting AND circuits for positive signals and OR circuits for negative signals, as in Fig. 13. Inverters are combined in parallel and in series, as in Figs. 14 and 15, and series-parallel combinations for other operations. The output of a logical network is combined with a sensing pulse to set a flip-flop.

In the schematic of the saturated inverter shown in Fig. 16 the input resistor is selected so that in the ON condition, enough current, plus a safety factor, flows from the base to keep the transistor saturated with less than 100 millivolts, collector to emitter. The resistor to the +10 supply voltage is chosen so that

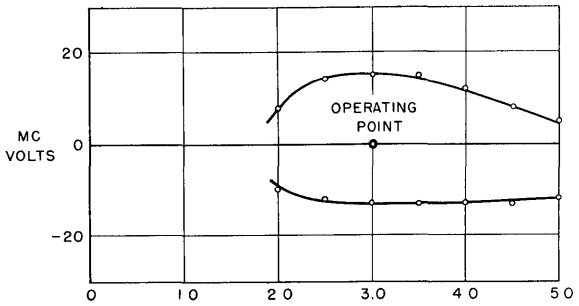


Fig. 25 (left). —3-volt supply margins

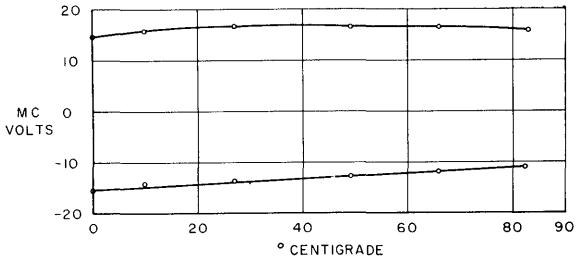


Fig. 27 (right). Temperature margins

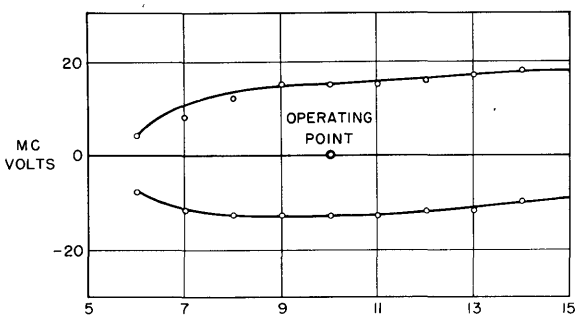


Fig. 26 (left). —10-volt supply margins

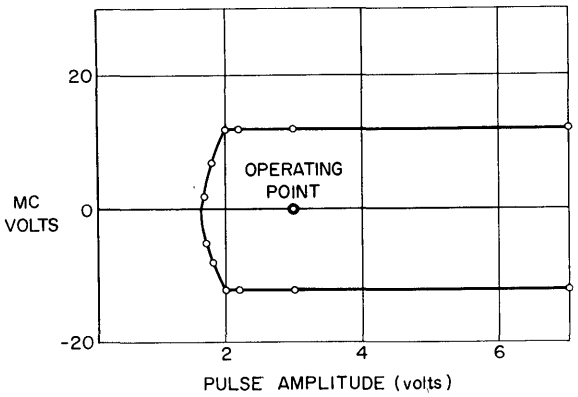


Fig. 28 (right). Pulse margins

when the input is close to ground and the transistor is cut off, the base is biased positive to give tolerance to noise and spurious signals. The by-pass capacitor C is made large enough to take all the holes out of the base during the turn off transient. Fig. 16 shows the effect of this capacitor on the turn-off time. With surface barrier transistors, the holes are removed so fast that the turn-off delay is difficult to measure.

The input impedance of the saturated inverter is roughly equal to the parallel RC in the base, so for driving economy R is made only small enough to saturate safely the transistor with the lowest expected current gain, and C is made only large enough to turn off safely the transistor with the largest specified amount of hole storage. Minimum current gain and maximum hole storage were specified to give reasonably large yields from transistor production.

Flip-Flop

In designing TX-0 it was decided that the advantages of having one standard flip-flop would be worth the cost of some complication in the circuitry. The circuit diagram of the flip-flop package in Fig. 17 shows an Eccles-Jordan flip-flop followed by a 3-transistor amplifier on each side. The output amplifiers give excellent rise time. Input amplifiers isolate the pulse input circuits and raise the input impedance. Also these amplifiers act as a delay line which allows the flip-flop to be set at the same time that it is being sampled. Fig. 18 shows the wave forms of this flip-flop package. The rise and fall times, about 25 mμsec, are faster than one normally sees in an inverter or emitter follower because on each output there is an inverter that pulls to ground and an emitter follower that pulls to -3 volts. Fig. 19 shows the pulse amplitude necessary to complement the flip-flop at various frequencies. Although this circuit will operate at a 10-megapulse rate, it is normally run at a maximum of 5 megapulses per second.

Circuits which are repeated often were designed with as few components as possible. In the case of less frequently used circuits, added components and even redundancy were incorporated when they could simplify the system. For example, the number of flip-flops in a system like TX-0 is quite small compared to the gates which transfer information from one group of flip-flops to another. So the TX-0 transfer gates were made very simple. A transfer gate is in fact only a single inverter; the emitter is connected to the output of the flip-flop being read, and the collector is connected to the input of the flip-flop being set. The output impedance of the flip-flop is so low that when the output is at the ground level, a pulse on the base of the transfer gate sets the other flip-flop.

Packaging

Simple construction and maintenance of TX-0 was accomplished by using large numbers of a few types of plug-in units. For example, one package, Fig. 20, contained only a standard flip-flop. Even smaller packages, Fig. 21, contained only one to three inverters or emitter followers. These then were plugged into panels like the one in Fig. 22, and in turn were interconnected with solderless connectors.

Marginal Checking

Marginal checking was incorporated in these circuits to locate deteriorating components before they failed. It was also useful for locating the design center of the various parameters, and for indicating the tolerance of circuits to these parameters. In addition, marginal checking was used after the TX-0 system was operating to find noise and other system faults which were not serious enough to cause failure, but which would have decreased the reliability.

Operating conditions of the circuits can be indicated by varying the inverter bias. In the flip-flop schematic in Fig. 17, the inverters were divided into two groups for marginal checking, and the two leads labeled *MCA* and *MCB* are varied one at a time for most critical checking of the circuit.

Sample plots of margins as a function

of various parameters are shown in the figures. Fig. 23 shows the tolerance to the transistor current gain, and how marginal checking will indicate its deterioration.

Fig. 24 shows the tolerance to τ, a measure of hole storage. Margins to supply voltages, temperature, and pulse amplitude are shown in Figs. 25 through 28.

References

1. Digital Information Storage in Three Dimensions Using Magnetic Cores, **Jay W. Forrester.** *Journal of Applied Physics*, vol. 22, Jan. 1951, pp. 44–48.

2. New Ferrite-Core Memory Uses Pulse Transformers, **William N. Papian.** *Electronics*, vol. 28, March 1955, pp. 194–97.

3. An Improved Technique for the Assembly of Core Memory Planes, **Elis A. Guditz, Lloyd B. Smith.** *Electronics*, vol. 29, Feb. 1956, pp. 214–28.

4. Pulse Responses of Ferrite Memory Cores, **James R. Freeman.** *Proceedings of the Wescon Computer Sessions*, Institute of Radio Engineers, New York, N. Y., August 25–27, 1954.

Discussion

I. D. Nehama (Bell Telephone Laboratories): How do large core memories like your 256 by 256 compare with drum memory on cost per bit?

Mr. Mitchell: I am not familiar with the current cost per bit of drum memories, but I can give you some idea of the reproduction cost of this memory, in calculating which, it is assumed that all drawings are available and no additional engineering is necessary. The current price for tested memory cores in large quantities is approximately 6 cents a core; the cost of stringing the memory planes and assembling the planes to form the memory array is about 4 cents a core. Thus, the cost of the memory array is about 10 cents a core. The estimate of the cost of the electronics for a memory of this size is 10 cents a bit. Therefore the reproduction cost would be about 20 cents a bit. A research laboratory for various reasons is not in a good position to give estimates on the sales cost.

D. E. Cowgill (Arma Corporation): What is the operating temperature range of this storage system?

Mr. Mitchell: Approximately 72±7 degrees Fahrenheit.

Recent Developments in Very-High-Speed Magnetic Storage Techniques

W. W. LAWRENCE, JR.

Synopsis: Developments of new magnetic elements have shown that rapid-access memory systems with complete operating cycles of a fraction of a microsecond are feasible. This paper describes the theory of operation of some of these elements and presents experimental data on the performance of samples.

THIS PAPER will discuss an approach to the problem of achieving a very-high-speed memory for the IBM (International Business Machines Corporation) Stretch Computer described by S. W. Dunwell.[1] The speed limitations of present day coincident-current core memories will first be outlined, followed by a description of a 4-legged magnetic core structure. Lastly, experimental data on the performance of samples of these structures will be presented and the over-all memory problem will be summarized.

The high-speed, random-access magnetic-core memories used in today's large computers and data processing machines have received very favorable acceptance as reliable and durable memory systems. Once selected and wound into the array, the small toroidal cores become a permanent part of the machine's hardware requiring no maintenance or replacement.

The switching speed of magnetic cores operated in the conventional coincident-current memory system is about 1.0 to 1.5 μsec (microseconds). A rather simple means of selecting one core out of a large array is possible, due to the square **B-H** loop characteristic of these magnetic materials. It is possible to select a value of current insufficient to switch a core, but one such that twice this magnitude will switch the core. (This technique is a familiar one that is widely used.) Since the switching speed of a core is proportional to the magnitude of the magnetomotive force applied, a core thus selected will only switch as fast as the material's characteristic allows. More specifically, a given magnetic core has a definite switching constant defined as the product of excess magnetomotive force and switching time. In Fig. 1 a plot of the reciprocal of switching time versus the magnetomotive applied (H) is a straight line that intersects the H-axis at the coercive force H_c. Using a 2 to 1 current selection system the switching time would be 1.0 μsec. This is the shortest switching time possible since the half-select current equals the coercive force. By changing the core material and processing to obtain the dotted line characteristic shown to the right, it appears possible from early experimental data to increase the switching speed by a factor of five. However, carrying these changes to the limit causes a deterioration in the squareness of the **B-H** loop, which results in poorer operation. Thus, in a straightforward coincident-current system, the switching speed is limited by the core material.

This limitation can be overcome by the use of a core structure, and a method of operation in which the speed is not limited by the material. An arbitrarily fast selection system can be obtained with present-day materials by using a biasing method that is similar to core-matrix switch operations. Fig. 2 shows a square-shaped core with a d-c bias winding that magnetizes the material into saturation at the left of the ϕ-I loop drawing, marked X. Each drive winding X and Y carries a current equal, but opposite in direction, to the bias current. Thus, one unit of current (I_b) cancels the bias, but two units of current switch the core to the opposite magnetic state. Note in this method that the magnitude of the currents need have no upper limit. The only requirement is that the half-select current equal the bias magnitude. Thus we have a 2 to 1 selection system plus the ability to drive very hard to get fast switching speeds even with present-day materials. A very important driving property is

W. W. Lawrence, Jr. is with the International Business Machines Corporation, Poughkeepsie, New York.

The work on which this paper is based was supported in part by the Department of Defense. The author wishes to acknowledge the contributions of a great many people, especially the following: S. K. Raker who was associated with the development of the actual multipath core operation described; F. L. Post who has made major contributions to the understanding of similar multi-path core structures

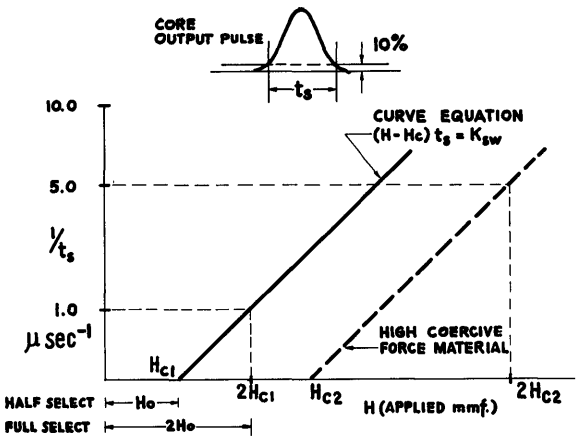


Fig. 1 (left). Inverse switching time versus applied magneto-motive force

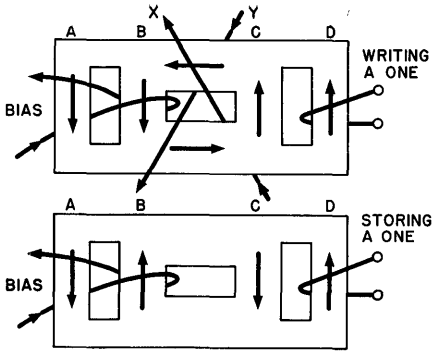


Fig. 3. High-speed multi-path core operation: writing a One, storing a One

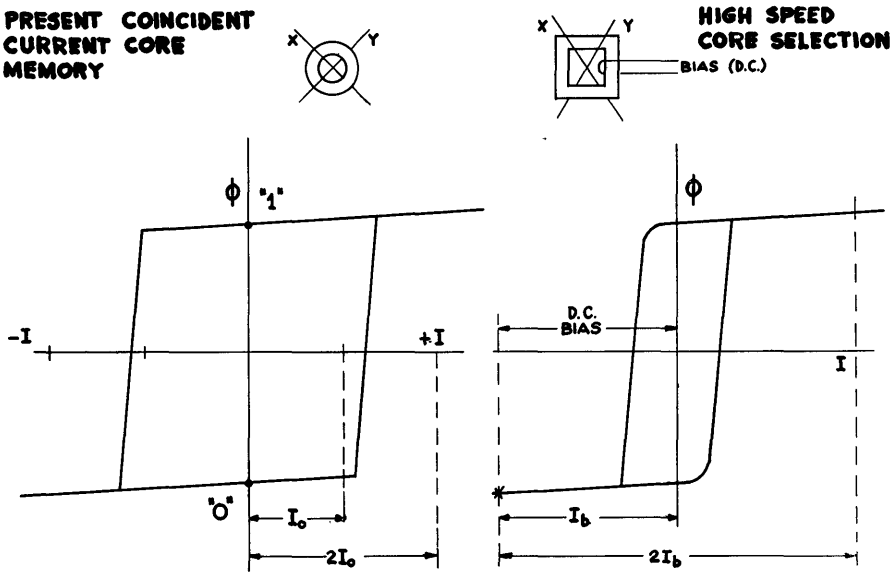
that half-select currents drive the core material only along a low permeability path that is reversible. For the reader familiar with the so-called coincident-flux type of operation as described by Bauer, and Hunter,[2] this biasing technique eliminates the problem of driving back-voltages which are caused by switching of flux around the drive hold in half-selected cores.

It must be noted that this simple core structure has no memory when used as shown in Fig. 2. As soon as the driving currents are turned off, the bias switches the core back to its original saturation state. Thus we are two-thirds of the way to our goal of achieving selection, speed, and memory all in the same element.

The multi-path core shown in Fig. 3 will illustrate one method of obtaining all three functions in one element. The core has four vertical legs with cross connecting material. The X and Y drive lines can go through the center hole, a sense winding around the last leg D, and a bias or Z winding on legs A and B. The top drawing shows the operation of writing a '*one*' with both drive windings X and Y active. The bias is cancelled and all 4 legs are magnetized to give an over-all counter-clockwise direction to the flux. Note that the last leg D under the sense winding is magnetized in the up direction. The lower drawing shows the state of the core when the above writing currents have been removed and the bias winding switches leg B back to the opposite saturation state. Since flux lines are continuous and the reluctance of path D is greater than C, an equal change takes place in leg C. Thus the last leg D under the sense winding is still in the up direction, storing a *one*.

The upper drawing in Fig. 4 shows the operation of reading, which is just the opposite of writing. The X and Y drive currents are applied in the other polarity, switching the core to an over-all clockwise flux pattern. In the reading operation, legs A and D are reversed. Since the flux in leg D is changed, a signal is generated on the sense winding indicating a stored *one* condition. When the read currents are removed, the bias switches leg A back to its normal saturation condition. Leg C will also switch to the opposite direction for the same reasons as discussed for writing a *one*. The core's flux condition now stands for the storage of a *zero*. It is evident that this multi-path core structure can have two distinctly different flux patterns for storage, even with a biased saturated condition on the left side. Legs A and B always return to the same direction of flux regardless of the stored information. This also implies that the current drivers connected to the array have the same load whether *ones* or *zeros* are stored, and they need not regulate current under changing load conditions.

The bias winding shown can serve another function in the selection scheme. By pulsing the bias winding with an added current during write time, we achieve the function of a Z or inhibit line and can thus obtain a three dimensional array with its inherent savings in the number of driving devices. The added current magnitude on the bias winding does not affect unselected cores because the magnetic material is simply driven further into saturation along a reversible magnetic path. The bias cur-



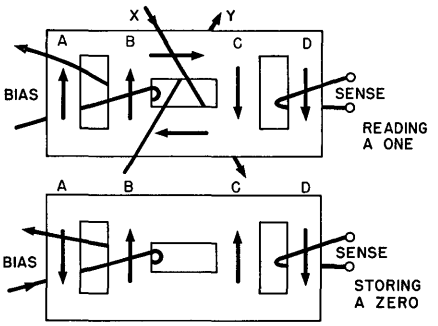


Fig. 2 (left). Comparison of selection methods

Fig. 4 (above). High-speed multi-path core operation: reading a One, storing a Zero

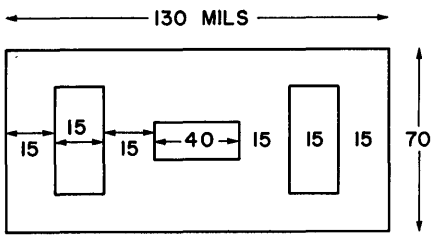


Fig. 5. Ferrite core sample

rent can be direct-current, or pulsed and timed with the read and write operations.

This operation of a multi-path core structure achieves selection and memory properties in the same element. Furthermore, this element can be driven at arbitrarily high speeds which are not restricted by the core material. The memory system can be built without changing the number of wires in the array or the general aspects of the driving, selecting, and sensing schemes now in a common use. Although the core structure is more complex than a toroid, new ideas in the field of automatic methods assembly show promise of simplifying the construction of these arrays.

Fig. 5 shows an actual core sample with dimensions indicated on each leg. The four vertical legs are all of equal cross sectional areas while the cross connecting material is twice that value. This core was made of conventional square loop ferrite material and was fabricated out of a larger piece of ferrite by means of an ultrasonic impact grinder. These early core samples were made rather large so that dimensions could be carefully controlled. Since the linear dimensions were large, the windings had several turns to generate the required magnetomotive force with reasonable available currents. As an example of the drives and signals obtained from a core of this type Fig. 6 shows typical outputs, with amplitudes, and pulse widths shown.

The top pulse lines show the X and Y drive currents, each 5 ampere-turns in magnitude, with rise times of 50 mμ-sec. The horizontal axis corresponds to time. First the write one operation is performed with both X and Y currents on and in the same direction. The second step corresponds to the full-select read of this stored one. The core output voltage on the sense winding has a peak amplitude of 1.8 volts per turn, and a switching time of 100 mμsec. The next step is reading again, and corresponds to reading a stored zero. The core output signal is 0.2 volt per turn with about a 50 mμsec-pulse width (essentially the rise time of the current). The last current pulse shown on the X line shows a half-select condition causing only a 50-millivolt signal on the sense winding. A core storing a *one* generates a similarly small signal when half-selected. The *one* to *zero* ratio here is 9 to 1, and the half-select noise is 1/36 of the signal. Since all the core signals are of the same polarity, half-select noise cancellation with an alternating sense winding is possible in an array.

The external circuits associated with this high-speed memory, such as selection and driving circuits, and sensing amplifiers, are being developed with the use of high-speed drift transistors. Switching and control transistor circuits are being tested in the 10-megapulse speed range. These circuits provide pulses with 20-mμsec rise times. The low impedance level of transistors makes a good impedance match to the magnetic core lines. Since transistors are primarily current operated devices, they work well with magnetic cores, which are current controlled elements.

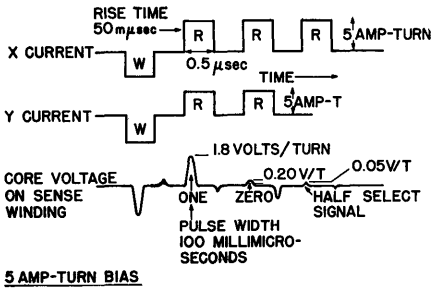


Fig. 6. Multi-path core operation signals

Another important phase of an over-all memory design that becomes more critical with higher speeds is the compactness of the physical layout. Here again the transistor circuitry will make smaller and more efficient designs possible. Short leads and carefully placed parts are important to the final operation of circuits transmitting millimicrosecond pulses. Printed circuit techniques and other automation methods are making the production of these high-speed systems economically feasible.

In summary, the speed limitations of present day coincident-current core memories have been overcome by a new way of using a multi-path core structure. High-speed operation is obtained with a substantial reduction over previous methods in back-voltage on the driving lines. Experimental data on sample units have shown favorable *one* to *zero* ratios.

References

1. Proceedings of the Eastern Joint Computer Conference, *AIEE Special Publication T-92*. "Design Objectives for the IBM Stretch Computer," **S. W. Dunwell.** May 1957, pp 20–22.

2. High-Speed Coincident-Flux Magnetic Storage Principles, **E. W. Bauer, L. P. Hunter.** *Journal of Applied Physics*, vol. 27, no. 11, Nov. 1956, pp. 1257–61.

Discussion

S. M. Rubens (Sperry Rand Corporation): How does the bias winding switch the magnetization in leg C in writing a *zero*?

Mr. Lawrence: In writing a *zero*, no switching takes place.

D. R. Brown (Massachusetts Institute of Technology): Will not power dissipation in the core material limit the frequency of access to a given storage location?

Mr. Lawrence: Using a ferrite core of this type at this high repetition rate creates a heating problem. The cores must be cooled by more than just forced air. Sample units of this type already are operating at 2 megacycles. With a 1/2-μsec cycle they have operated very well. The type of cooling is not settled.

V. J. Sferrino (Massachusetts Institute of Technology): What current was used on X and Y windings at 50-mμsec rise times?

Mr. Lawrence: The magnetomotive force shown in the last slide was 5-ampere turns. It was mentioned it has a number of turns, so that it reduces the actual current. With 8-turn windings the X current and the Y current each were 5/8 amperes.

G. Smith (Daystrom Instrument): What "times" are involved in returning a core to its biased state?

Mr. Lawrence: That time is approximately the same as the reading operation, since a 5-ampere turn drive is applied to the material.

L. C. Hobbs (Sperry Rand Corporation): Do you have information on the relative cost of these cores, and the cost of memory-plane assemblies compared to those of normal toroidal cores and assemblies?

Mr. Lawrence: No, only experimental single elements have been tested and the various sizes, shapes and materials investigated. When the best one is settled on, quantities will then be made, put in an array, and then it will be possible to go on from there.

Megabit Memory

R. A. TRACY

THE PRESENT STATUS of the coincident-current matrix memory is largely one of hope for the future, in so far as very large memory systems are concerned. Memories made to use presently available materials are limited by cost and associated engineering problems. The problems arise largely from the use of ferrite cores. The major problem is the nonuniformity of the cores. Procurement, core testing, matrix wiring, matrix testing, and core replacement also present serious difficulties. Complicating these problems are the material properties of the ferrites, such as temperature and strain sensitivity, the necessity for operating on a minor hysteresis loop, and the difficulties encountered in varying the magnetic parameters to fit a core to a system.

Description of New Memory Element

A new magnetic memory element has been discovered by Douglas Wendell of Burroughs Corporation. It consists of a short length of 4-79 Molybdenum Permalloy ultra-thin tape wrapped directly around a bundle of insulated wires and then glued. Although the material has a relatively large coercive force, the small diameter obtained by wrapping directly on the wires more than compensates for this, so that the current required to switch the core is comparable to that required by the ferrites. The tape is used as it is received from the rolling mill. No heat treatment is required. The original concept specified that this tape, wrapped on four wires, constituted a memory element. Fig. 1 shows such an element, and suggests how the original name of "bug" evolved. The individual elements were then soldered into a matrix array. The first matrix made in this way is shown in Fig. 2.

While this arrangement for a complete matrix array has proved to be very advantageous, the fact that there are a number of solder connections for each element introduces a rather extensive fabrication operation. Examination of the wiring array was made to determine possibilities of reducing the number of connections. It was found that a string of elements having three common wires and one unique wire was possible. The matrix could then be made in halves as shown in Fig. 3. A machine was designed and built to perform the wrapping operation on a semi-automatic basis.

The problem of the numerous solder connections was, of course, referred back to the original inventor and his associates. It was then pointed out that the tape could be wrapped at the appropriate stations in a pre-wired matrix array. A matrix made using this new technique is shown in Fig. 4. Several of these matrices have been built to test uniformity and to study techniques. Refined techniques of wrapping are available whereby many cores can be wrapped simultaneously.

Properties of New Memory Element

The properties of the metal tape eliminate many of the problems associated with the ferrite cores. The 4-79 Molybdenum permalloy ultra-thin tape has a 60-cycle per second hysteresis characteristic as shown in Fig. 5(A). Minor loops are included to provide a better comparison with the ferrite material which is shown in Fig. 5(B). These figures indicate the reason for outer-loop operation with the metal tape in contrast to the inner-loop operation required with the ferrite. Coincident-current operation would not be possible using the outer loop of the ferrite. The value of the field at the knee of the hysteresis loop does not vary greatly in the different loops for the metal. This is not true in the case of the ferrite. Thus, the inner loop operation makes the configuration sensitive to transient currents which can drive the core to an outer loop, and in this way require demagnetization before using.

Other material properties of interest are temperature, sensitivity, strain sensitivity, and uniformity of magnetic properties. The temperature sensitivity is shown in the graph of Fig. 6. The lower temperature sensitivity of the metal tape is understood when the Curie temperature is considered. The ferrite has a Curie temperature under 200 degrees centigrade which is less than half the metal Curie temperature of 430 degrees centigrade. The closer the operating temperature is to the Curie temperature, the greater will be the temperature sensitivity. Sensitivity to strain is negligible in the metal tape. The material has been strained to the breaking point with no noticeable change in properties. This is understandable when it is recalled that a 95% cold reduction occurred in the rolling process, and no strain relief anneal has been applied. The cores may be potted directly in an epoxy resin with no change in properties. The uniformity of the material is very good for tape from the same melt with the same processing history. Deviations from uniformity

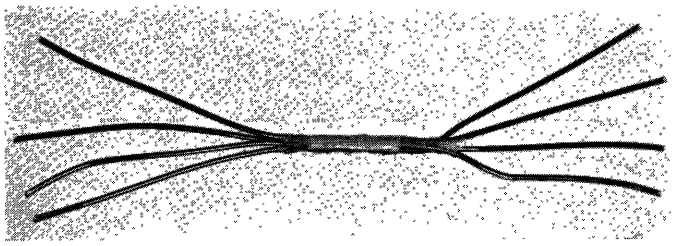


Fig. 1 (left). Bug memory element

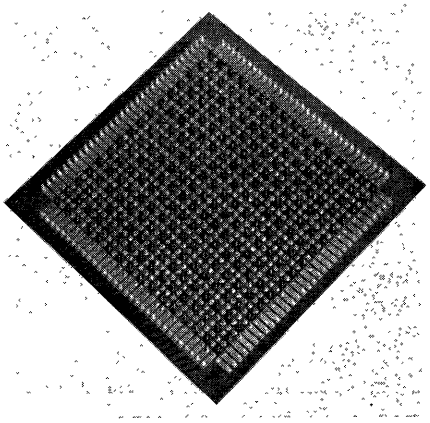


Fig. 2 (below left). First matrix memory

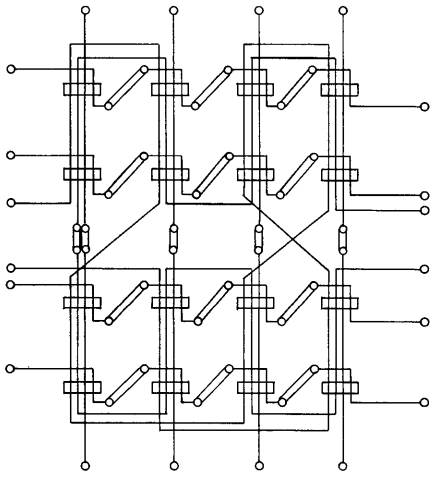


Fig. 3 (below). Second matrix memory

R. A. TRACY is with the Burroughs Corporation Research Center, Paoli, Pa.

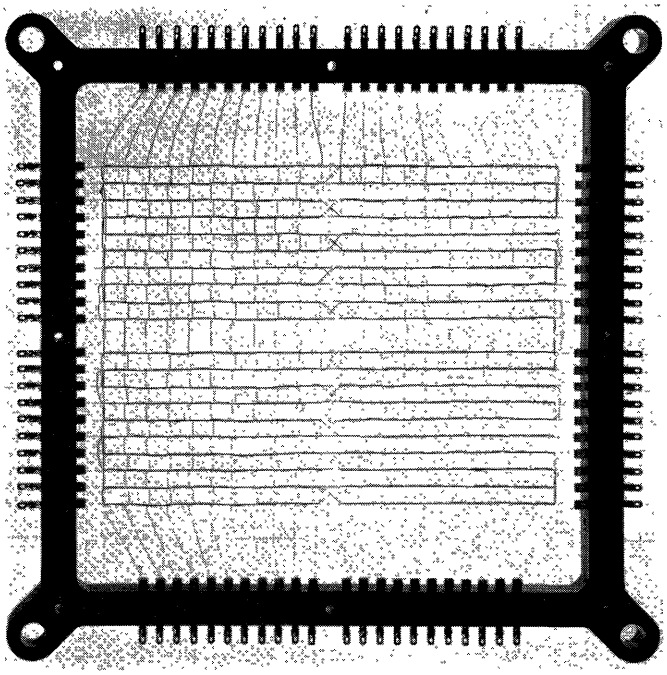


Fig. 4. Final matrix memory

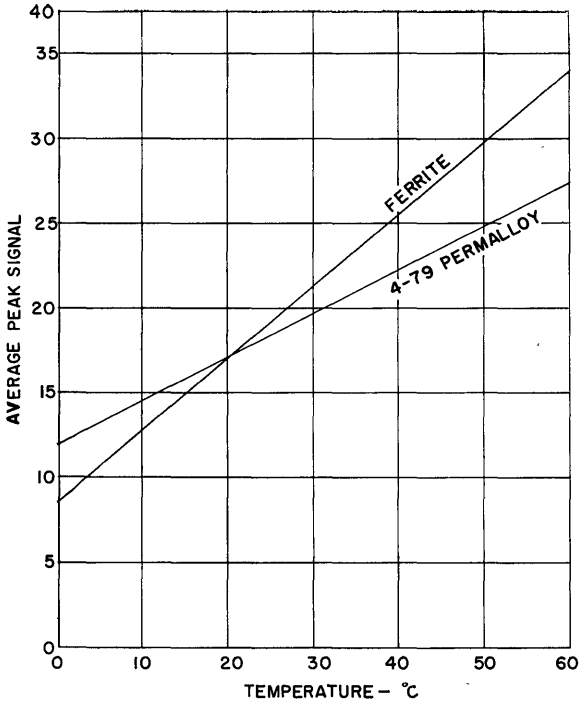


Fig. 6. Temperature sensitivity

within a batch are due to mechanical tolerances in thickness. This is a maximum of 10% and effects only the total flux. Large deviations exist for material from different melts, and smaller deviations for material subjected to different processing schedules. This, however, is not serious because a 50-pound melt will make between 10 and 20 million memory elements.

The behavior of the memory element under pulsed operation is quite similar to the ferrites. Fig. 7 shows the output voltage of a ferrite and the metal under identical operating conditions. A graph of the variation of output signal and noise versus driving current provides a more detailed comparison of these elements. This is shown in Fig. 8. It can be seen that the metal tape is usable over a wider current range.

A very important advance is the variability of pulse operation that can be obtained by varying dimensional parameters. A longer metal tape or a wider tape will give a greater output voltage. A variation in wire size varies the core diameter allowing the driving currents to be preselected. The range of half-select current was from 150 milliamperes to an unlimited amplitude for the material as shown in Figs. 5 and 7.

The full range of properties attainable for various materials and processing techniques is not known. The majority of work has been done on metals which can replace the slow (5 second) ferrites. Materials which can operate at much

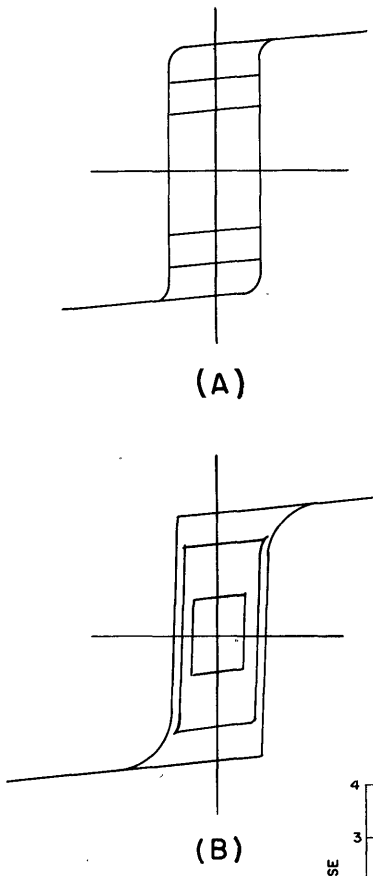


Fig. 5(A). 4-79 Molybdenum permalloy hysteresis loop. 5(B) Ferrite hysteresis loop

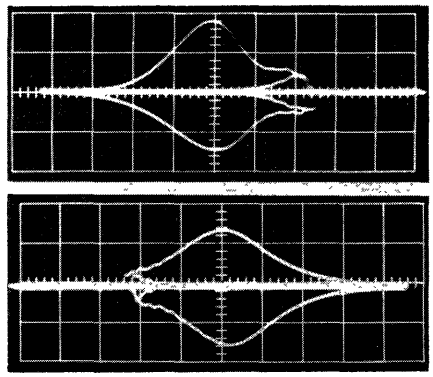
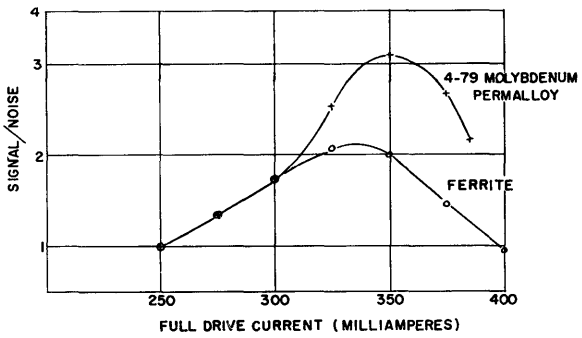


Fig. 7 (above). Voltage output

Fig. 8 (below). Signal and noise variation



higher speeds have been observed. The latter, of course, requires higher driving currents.

Cost Considerations

An analysis of the cost of these memory elements is in part a guess since they are not yet in production. Materials cost per element is 3 cents. Testing before fabrication of the matrix is not required once a batch of material has been selected. Fabrication cost includes pre-wiring the matrix and wrapping the cores. This can be accomplished by automatic means, this should not exceed 2 cents, and will probably be less. Testing of the matrix is identical to ferrite planes. However, replacement of cores which are not within specifications is simply a matter of removing the old tape and rewrapping a new one at that station. No wiring is involved. This provides a factor of ten cost advantage over ferrite cores and also a time advantage in fabrication. Further advantages can be realized in associated memory equipment such as drivers and sense amplifiers. The superior properties of the metal tape permit the use of less critical specifications on these equipments, thereby permitting an additional cost reduction.

Conclusions

This new memory element removes many of the limitations presently restricting matrix memory size. Uniformity, cost of materials, cost of fabrication, and testing are all improved to the extent that million-bit matrix memories become quite feasible.

Discussion

G. Myers (U. S. Air Force): Is there any trouble getting uniform core diameters? How are diameters controlled?

Mr. Tracy: The information on how the magnetic tape is wrapped around the wires cannot be released right now. Uniform diameters are gotten, though. One way of determining this is to measure the value of the current required to begin to upset the flux of the core. This measures the value of the knee of the hysteresis loop, which in turn measures the core diameter since the loops of the material are uniform.

D. Meier (National Cash Register Corporation): Are the switching times comparable to those of conventional S-3 ferrite cores?

Mr. Tracy: It was attempted to replace directly the S-3 core. When the diameter which could best be used with the currents required for the S-3 was obtained, the switching time was 4 rather than 5 microseconds.

R. Schultz (General Electric Company): What was the thickness of the tape?

Mr. Tracy: 1/8 mil.

K. Preston, Jr. (Bell Telephone Laboratories): How large a working memory has been constructed from these elements? What tolerances have you been able to maintain on the magnitude of half-select current required for a batch of elements?

Mr. Tracy: Twenty by 20 planes have been fabricated and tested. A working memory was not constructed. Secondly, the condition was imposed that the drive current must be able to vary by 10% and the cores must fit the system. The system then was not analyzed to determine if the spread was below 10%. The 3-sigma value was within that 10% tolerance.

W. W. Davis (Naval Ordnance Laboratories): How do you get even reasonable loop squareness following the wrapping operation?

Mr. Tracy: The material, as received from the rolling mill, has a high degree of strain anisotropy. This affects the magnetic properties, producing an anisotropic magnetic material such as 50-50 nickel-iron. Since the material is insensitive to the strains encountered in the wrapping operation, the squareness was retained.

R. F. Mauger (National Cash Register Corporation): Is core loss due to eddy currents a limiting factor at very high frequencies?

Mr. Tracy: In an operating matrix memory, the frequencies encountered are below those that will give eddy-current losses in 1/8-mil tape.

D. R. Brown (Lincoln Laboratories, Massachusetts Institute of Technology): Are the curves in Fig. 8 for a memory array, a plane, or a single core? How is signal-noise defined?

Mr. Tracy: The curves in Fig. 8 are for a single core. Signal-noise is defined by measuring the noise and signal at the peaks.

W. J. Bartik (Sperry Rand Corporation): What output voltages are obtained for a *one*? How many wraps of 4-79 Molybdenum permalloy are used?

Mr. Tracy: This depends on the length of tape that is used. If a 1/2 inch length of tape is used, the output will be approximately 30 to 40 millivolts. If 1 inch of tape is used, the output will be approximately twice as much. The 30 millivolt output was aimed for. This can be varied by varying the length of tape. The number of wraps are not controlled, the length of tape is controlled; a 1/2 inch was the standard length.

R. M. Clinehens (National Cash Register Company): I would like to ask where the unannealed 4-79 Molybdenum permalloy can be purchased and what is the over-all dimension of a single finished core? I know that you have not yet fabricated an array of this type as large as a million bits, yet I would like to ask what your estimate would be of the dimensional volume space that would be occupied by such an array?

Mr. Tracy: The unannealed 4-79 Molybdenum permalloy tape can be purchased from Armco. The dimensions of a single core are 1/8 inch long by approximately 20 mils diameter. The miniaturization will probably be limited by the number of contacts that must be made to a plane. The memory plane can be folded several times after fabrication to realize this small space.

Ferrite Apertured Plate for Random-Access Memory

J. A. RAJCHMAN

TO STORE digital information, it is natural to provide an artificially constructed discrete cell for every bit. This is in keeping with the philosophy of not confiding digital information to any analog variable. Most of the early solutions to the problem of the high-speed memory of reasonably large storage capacity (acoustic delay lines and electrostatic storage tubes) resorted to storing the bits on nonsegregated areas of a homogeneous medium, in violation of this philosophy. The advent of magnetic materials with fast switching and square hysteresis loop provided the first practical means of building relatively large numbers of individual storing cells, each being merely a tiny toroidal core.[1,2,3] The core memory proved orders of magnitude more reliable and better in most respects than the earlier types, and it is now the classical solution to the problem.

The two directions of magnetic remanence provide natural storage for a bit of information, and the square hysteresis loop allows the storing magnetic element itself to participate in the switching required for its selection in a memory system. Some years ago when we first realized that these properties were ideal for a large capacity high-speed random-access memory, we sought various artifices to fabricate at once arrays of large numbers of cells. At first we used individual cores mostly to test the ideas of complete memory systems. We found that the making, testing, and assembling of individual cores was not too laborious a task as long as the number of cores was in the hundreds or even thousands. The fact is that, with the presently well evolved techniques, the cost of assemblies with thousands and even hundreds of thousands of cores is comparable to the cost of the auxiliary electronic equipment required for operating the memory. But for larger storage capacities, millions or scores of millions of bits, the fabrication, the testing, and the assembly of separately made individual cores becomes prohibitive.

For this reason, the original investigations for ways to fabricate whole arrays of storage cells was carried on, along with experiments with single cores. Some years ago, we conceived the idea of molding a plate with an array of holes out of ferrite material having a square hysteresis loop. Such a plate can provide the many storage sites inherent in the use of a continuous medium and yet preserve the distinctiveness of the cells. This is because the areas on the plate are artificially defined by the apertures to form separate storing cells. Pierced metal sheets were considered by R. C. Minnick and R. L. Ashenhurst[4]. These authors believed it preferable to etch out individual toroids from a sheet cemented on a bakelite support.

The development of our apertured plate has now reached a stage which opens possibilities of memories of very large capacities: millions of bits. Because it requires much less driving power, it promises also to reduce and simplify the associated electronic circuits. Furthermore, it makes possible very compact memories of relatively small capacity.

This paper describes the principle of operation of the aperture plate, its fabrication by molding, means of making printed windings, and the characteristics of an experimental prototype plate with 16 by 16 = 256 apertures of which thousands were made. A system is proposed to drive the memory plates by a switch, itself made from plates. The operation of the system is based on several novel switching methods which make possible large storage capacities, read-out signals free from disturbances, fast access, and large tolerances in the amplitudes of the electronic driving circuits. The use of the plates in a conventional current-coincident operation is considered.

The Apertured Plate

Consider a regular array of round holes in a plate of magnetic material having a perfect square hysteresis loop. Let the direction of the remanent magnetization around each hole store one bit of information. It should be expected that each hole acts independently as though it were the hole of an individual core, and that there is no effect due to repeated access to adjacent holes. This is for the following reason. For a given current linking an aperture the magnetizing force H diminishes gradually with distance. Near the hole, nearly perfect radial symmetry can be assumed, so that the H lines are circles and the value of H is inversely proportional to the radius. Therefore, there will be some circle of radius R_o within which the magnetizing force is more than some critical value H_c required to reverse the flux in square loop materials and beyond which it is less than this critical value. Hence, there should be complete reversal within the circle and none without. For a judicious choice of the energizing current, bringing this circle to less than half the width of the legs separating adjacent holes, there should be no interaction between adjacent holes.

In reality, there is a family of hysteresis loops, and the loops are not completely square so that there is a gradual rather than a discontinuous radial change of flux. To determine whether these deviations from perfect rectangularity would produce detrimental cross-talk, a number of experimental plates were made, all of as identical a material as was possible to make. Each plate had an array of 9 holes of a given diameter d, and spaced at a center-to-center distance D, the ratio d/D being different for the various plates; see Fig. 1. The current I_o in the center hole was adjusted in every case to produce maximum discrimination under the conventional 2-to-1 current regime. The percentage change in the signal obtained from the excitation of I_o as a result of repeated excitations of an adjacent hole by a current I_1, made equal to I_o, was taken as a measure of the interaction. It is apparent from Fig. 1 that the interaction becomes significant only when the holes are so close that the distance between hole peripheries is less than the radius of the holes. The current producing optimum discrimination is seen to increase linearly with hole size except for a slight deviation from linearity for large holes. The resulting output voltage curve also starts by rising linearly with hole size because the optimum current renders the cross section area of the material in which flux reverses proportional to the hole diameter.

J. A. RAJCHMAN is with the Radio Corporation of America Research Laboratories, Princeton, New Jersey.

The success of this work was made possible by many members of the Radio Corporation of America Laboratories. C. Wentworth developed the plate processing. W. Wales and G. R. Briggs worked in the early phases of the investigation. H C. Crane and W. F. Kosonocky worked in the later stages and contributed many ideas. A. W. Lo was active throughout the project and developed the sensing circuit. Most of the mechanical work was done by J. Walentine B. M. Quinn and C. H. Morris contributed to the shop work.

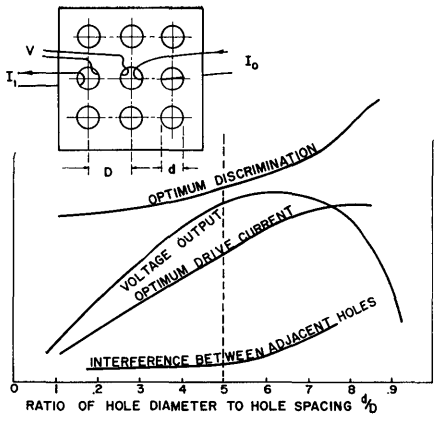


Fig. 1. Effect of hole size and spacing

The voltage reaches a maximum and then decreases as the available cross section area diminishes because the legs between adjacent holes become thinner. The curve of maximum discrimination rises, at first slowly and then more rapidly. This is because the region where flux reverses, which is between the aperture and its nearest neighbors, becomes thinner; therefore the hysteresis loop, which is an average of elementary zonal hysteresis loops, is squarer as the averaging extends over a smaller radial spread.

Because of unavoidable differences in the nature of the material of the various plates and the difficulties of measurements, no absolute numerical significance can be attached to the plots of Fig. 1. However, these plots indicate the general behavior of the interaction, amount of useful signal, and discrimination, as a function of the geometry of the array. The ratio of hole diameter d to hole spacing D of $1/2$ is approximately in the center of an optimum range for which there is practically no cross-talk, the signals are high, and the discrimination is relatively large. This simple ratio was adopted for an experimental prototype plate.

The Experimental Prototype Plate

A prototype plate design was adopted for most of our experiments. The plate has an array of 16 by 16=256 holes. The holes are 0.025 inch in diameter, and are spaced 0.050 inch center-to-center. The plate is a square 0.830 by 0.830 inch; see Fig. 2. The plates were molded with the array of holes. This required fairly elaborate punches and dies. Considerable experimentation was necessary to develop the right powder, composition, binder, and consistency to obtain satisfactory molding and satisfactory magnetic properties. The firing of the plates is somewhat more critical than the firing of individual cores. This is mostly because precaution must be taken to keep the temperature uniform throughout the area of the plate. Prefiring in tunnel type furnaces in air, followed by final firing in controlled atmospheres, yielded uniform plates with fairly square loop characteristics. These characteristics are described in more detail in the following.

The Printed Winding

The ferrite plate is non-conducting, in fact a fairly good insulator. It is possible to coat it with a metallic conductive layer so as to link the holes and thereby obtain a "winding" without the necessity of threading a wire through the holes. This method is particularly suitable for making a winding which links all the holes in series. To obtain such a winding the ferrite plate is first coated with a metal conductive layer on its entire surface including the inside walls of the holes. Then, the coating is removed along cross-lines so that little islands of metal remain on the surface of the plates; see Figs. 2, 3, 4, 5. Each island is a rectangle comprising two holes. The rectangles on one side of the plates are staggered with respect to those on the other side. The continuity of current flow is, therefore, through one island, then through the coating of the walls of the hole, then through the island on the other side, back through the coating on the walls of the next hole to the next island, etc.; see Fig. 3. The pattern of islands is so designed that a winding, linking all holes in series, is obtained. The removal of the metallic coating along appropriate straight lines can be done in various ways such as grinding grooves, using photoengraving techniques, etc. A particularly convenient method is to mold the plates with a pattern of ridges corresponding to the lines along which the coating is to be removed. These ridges are only a few thousandths of an

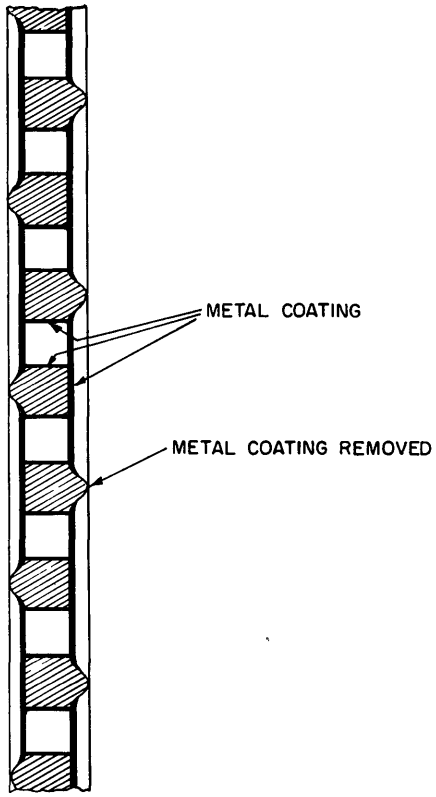


Fig. 3. Enlarged cross section of ferrite plate

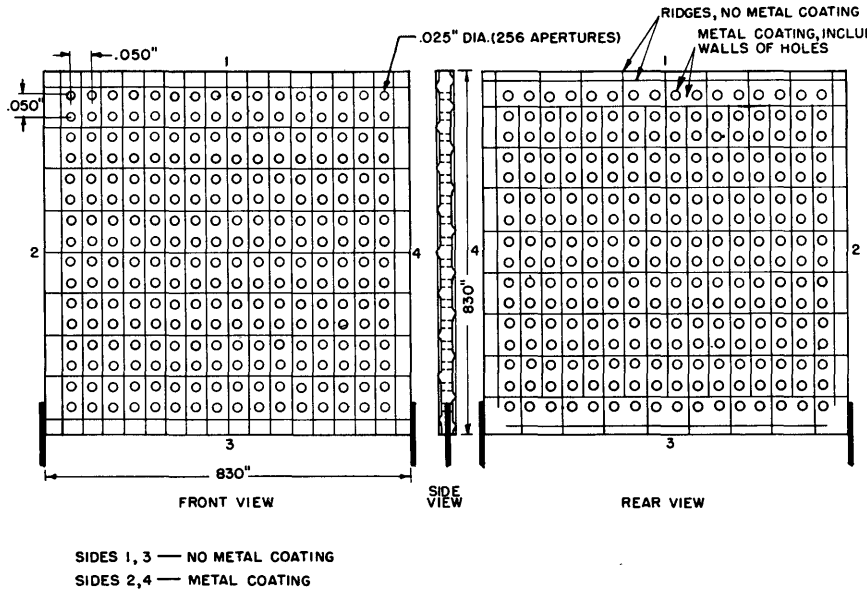


Fig. 2. The experimental prototype apertured ferrite plate

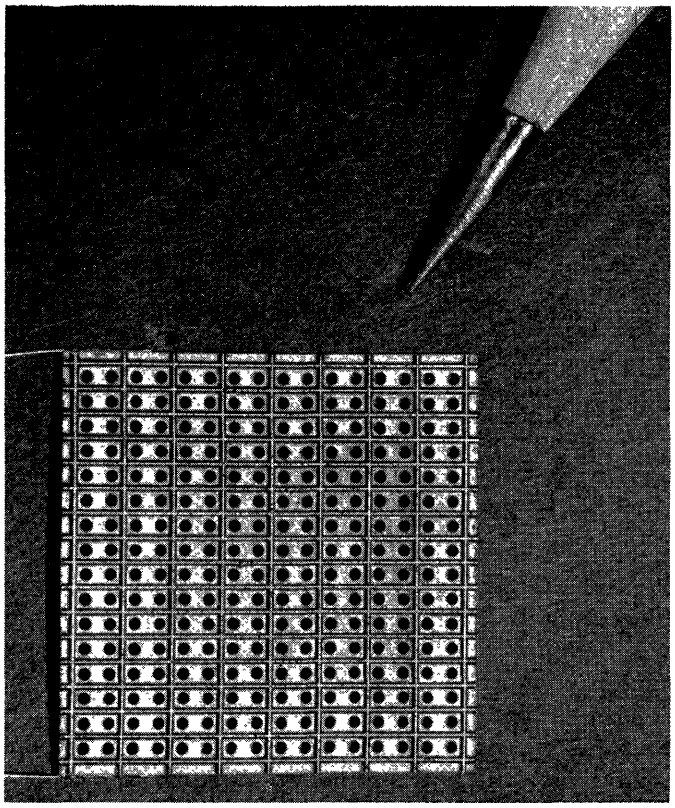


Fig. 4. Experimental prototype memory plate with an array of 16 by 16 = 256 apertures

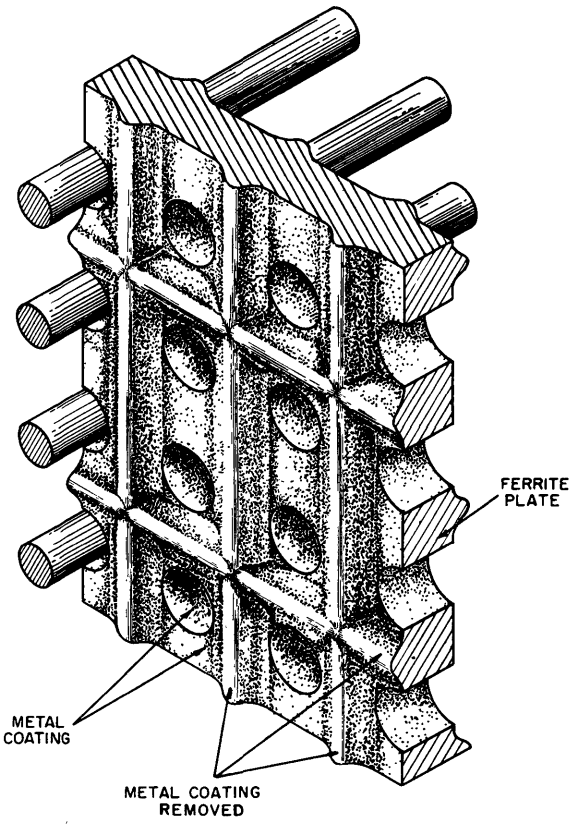


Fig. 5. Perspective view of section of prototype plate

inch high. After spraying the entire surface of the plate it is merely sufficient to remove the metal coating on the top of the ridges to obtain the desired pattern. Fig. 4 shows the plate with its printed winding. The two terminals are 0.007-inch bare copper wires, silver pasted to two sides of the plate; slides 2 and 4 on Fig. 2. The silver on the two other sides (1 and 3) of the plate is removed to prevent a short between the terminals.

The plates undergo considerable shrinkage during firing, about 20% in linear dimensions. The exact final size depends on the nature of the ferrite, the pressure of molding, and the heat treatment. It is found to be remarkably constant, perhaps within ± 0.001 for the 0.830 inch side of the plate, provided accurate control of parameters is maintained. But during the developmental stage, when different materials and processing are used and the size may vary considerably, the ridges are a particularly convenient way of insuring that there is no misalignment between the pattern of lines and the pattern of holes. The ridges have also another important advantage in that they tend to strengthen the plate, particularly when it is very thin. Plates were made with a thickness of only 0.007 inch at the significant location around the holes, although thickness of about 0.020 inch was selected for the prototype plates.

Plate Testing

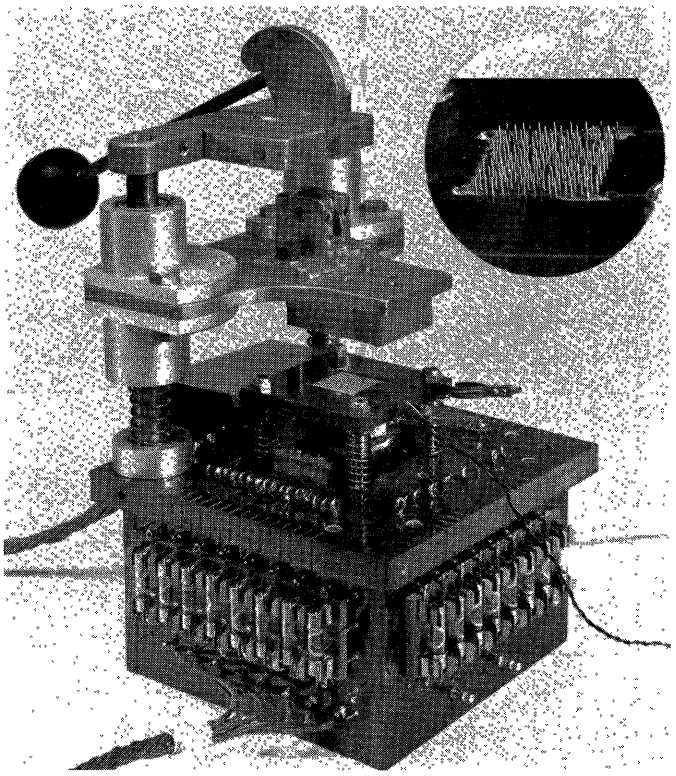
After being provided with its printed winding, the entire plate can be tested easily in a single operation by means of a special tester. The tester has an array or "forest" of parallel conductors over which the plate is inserted. The electric circuit of the conductors is closed by shorting the conductors after insertion of the plate. The pins are energized serially by means of a magnetic switch, itself made of plates (of a type described in the following). The outputs from the successive holes are obtained from the printed winding and are conveniently displayed as a superposition of traces on an oscilloscope. A glance at the bundle of traces suffices to determine whether or not the plate is acceptable. An experimental semi-automatic tester was built (Fig. 6) which had only 128 pins (shown on the insert) so that two insertions are necessary to test the whole array of 256 holes.

Plate Characteristics

Many thousands of prototype plates were fabricated in an experimental batch. Fair uniformity was observed on sample tests of about a hundred plates each. Typically, the amount of flux reversed around the aperture for a given current excitation varied $\pm 5\%$ from the average, within a given plate as well as between plates.

The operation under the conventional 2-to-1 current drive is shown on Fig. 7. An aperture was energized by a train of current pulses ($P\frac{N}{2}\frac{N}{2}PN$ as shown on Fig. 7) used in routine checking of discrimination for conventional cores. The wanted flux reversal ϕ_1 for a given current excitation, and the unwanted disturbing flux ϕ_4 obtained after two disturbances, of half the given current excitation, are plotted as a function of the current excitation. These flux reversals do not include the reversible part subtracted at the end of the current pulses, and thus include both reversible and irreversible flux changes. The ratio of wanted to unwanted fluxes ϕ_4/θ_1 exhibits a maximum for an excitation of about 330 ma (milliamperes). The switching time τ is plotted also as a function of I and is seen to be about 1.5 μsec (microseconds) for the nominal excitation of 330 ma.

Read-out signals obtained from the printed winding are shown by the photograph of oscilloscope traces on Fig. 8.



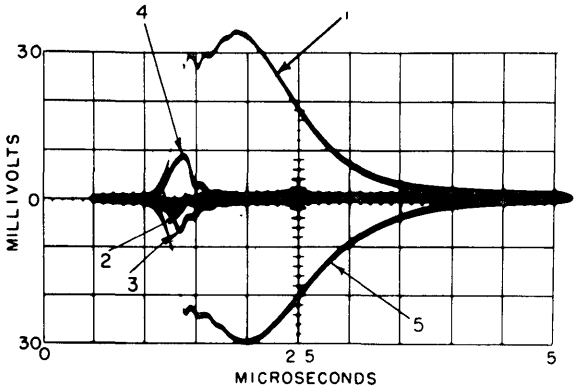


Fig. 6 (left). Semi-automatic experimental plate tester

Fig. 8 (above). Read-out signals from aperture plate

The full current was at the nominal amplitude of 330 ma. The wanted signal (1) occurs at the first positive pulse (P), the disturbing signal (4) of interest occurs at the second positive pulse (P) after two half-amplitude negative demagnetization pulses. The discrimination of this experimental ferrite plate is comparable to that of early cores, and somewhat inferior to that of present day relatively evolved cores. On the other hand, the aperture of the plate requires about 3 times less current and only about $2\text{x}10^{-8}$ joules or about 5 times less energy than the conventional memory core. This economy results from the fact that it is practical to use only a very small volume of material in a plate of manageable dimensions, while an individual core of the same volume would be unmanageably small.

The observed amount of cross-talk between adjacent holes of the prototype plate is very small, as illustrated by the plots of Figs. 9 and 10. The spread of flux from an energized aperture outward is apparent on Fig. 9 which is a plot, as a function of current amplitude, of the total flux ϕ_1 around the aperture, the flux ϕ_2 in the region up to the nearest adjacent holes, and finally of flux ϕ_3 in the next surrounding zone. This spread is as should be expected when assuming that the flux reverses up to a critical circle of radius proportional to current. If the current is kept below the value for which the circle bisects the leg between adjacent holes, there should be no interaction, as was mentioned. This is verified approximately by the measurements of the variations of flux in a leg between two adjacent holes as a function of current excitations in one and then the other hole, as shown on Fig. 10. The entire plate is first brought to a standard condition of flux distribution by a current I_0 through the printed winding, (directions of flux around the holes in a checkerboard pattern). Then a current I_1 is applied through one of the holes and produces a flux change ϕ_A in the intermediary leg. If, before the flux is restored by a new pulse I_0, a pulse of current I_2 (equal to I_1) is applied to the other hole, the resultant flux change ϕ_B in the intermediary leg has not, in general, the same value as ϕ_A, since some of the flux in that leg was previously reversed by the pulse I_1. However, the values of ϕ_B and ϕ_A are almost identical for values of current that produce about half the total possible flux change in the intermediary leg. For the optimum operating current of about 330 mA, the value of ϕ_B is only slightly less than ϕ_A, showing that there is only negligible cross-talk between the apertures which, for all practical purposes, can be considered to operate independently. A considerably larger current, about twice the optimum value, may still be used, even though it will reduce, in general, the strength of the signal obtained from an adjacent aperture.

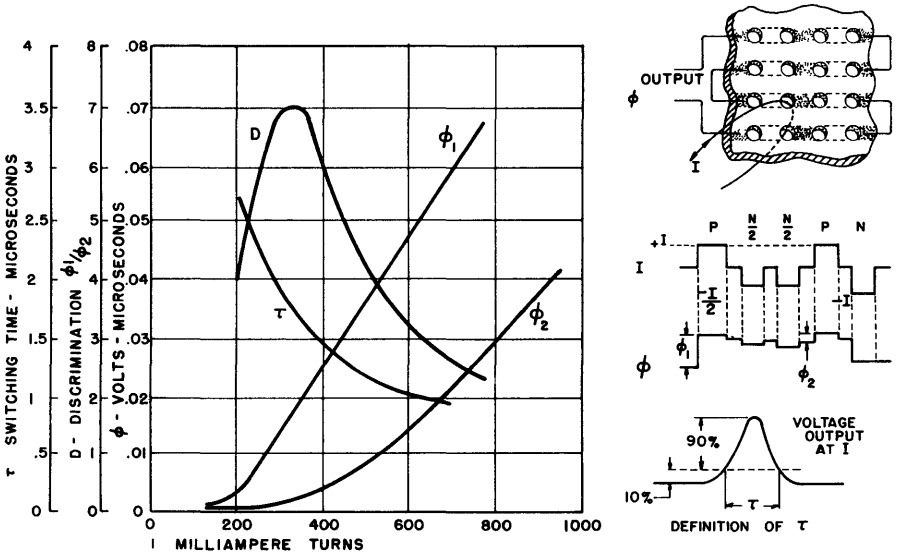


Fig. 7. Flux changes, discrimination, and switching time around an aperture of experimental prototype plate

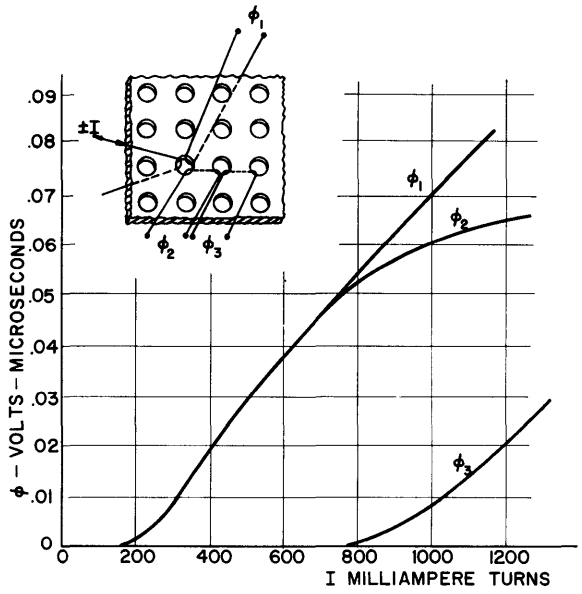


Fig. 9 (above). Flux spread in apertured plate

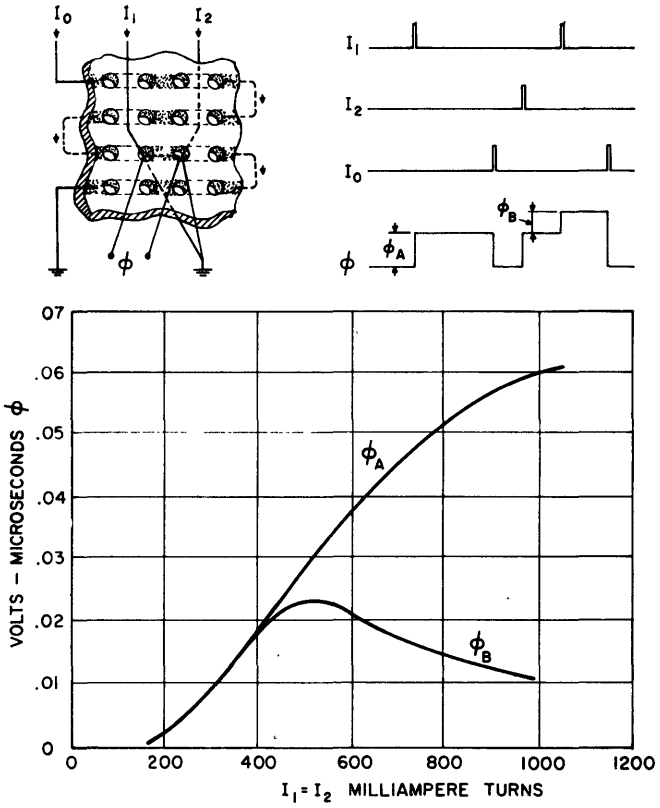


Fig. 10 (right). Effect of access to adjacent hole

Current-Coincident Plate Memory

For most applications of high-speed memories, random access to a word composed of a number M of bits is desired. This number M is typically between a few and a hundred. The plates are particularly suitable for such a parallel memory as they are conveniently stacked with all their apertures in perfect register. The stack is wired as a unit with address selecting wires so that the same location in each of the M plates (or plate pairs) is reached simultaneously. The printed or "digit" winding on the individual plates serves for read-out and write-in of the digits of the word.

The plate memories can be operated in a current-coincident mode, just as do the conventional core memories. The holes of the stack of plates are threaded back and forth by rows X and columns Y, as shown on Fig. 11. This threading is not too exacting a task, even though the holes are only 0.025 inch or half the inside diameter of conventional memory cores, because the wires go straight through the holes which are in perfect axial register. This wire threading is a unique operation and need not be repeated separately for each plane, as is customary with memory-core planes. The numerous separate digit windings, so tedious to thread in core planes, are obtained by the printed technique on the plates. It is apparent therefore that the complete wiring of the stack of plates is much simpler than with individual cores. However, only three conductors are provided in each aperture: the printed digit Z winding in the form of metal coating on the wall of the hole and the X and Y selecting wires. It is not convenient (although possible with a modification of the printed technique) to provide two digit windings, one for read-out and one for write-in, as is customary with core planes, so that the single Z winding must serve for both functions. This poses some problems

It will be recalled that in most current-coincidence operating modes there are 2 cycles: a reading cycle in which the selecting wires X and Y are energized with $+I/2$, and the signal is read-out from the Z winding; and a writing (or rewriting) cycle in which the selecting wires X and Y are energized with $-I/2$ and the Z windings of the various planes are either not energized or energized with inhibiting currents of $+I/2$ depending on the nature of the digits to be written-in. The logic of the writing requires that the three windings X, Y and Z link every aperture in the plate in the same sense. This is achieved by threading the X and Y windings back and forth through the stack to conform with the physical checkerboard pattern of the Z printed windings, as is shown on Fig. 11. Therefore, during the read-out, the voltages induced by the half excitations of the apertures on the selected row and column, add up, rather than tend to cancel each other as in conventional read-out windings, and produce an appreciable masking signal. This signal could be neutralized by a fixed voltage derived from an auxiliary core excited at the instant of read-out.

A better way to cancel the disturbing signals is to use a a pair of plates for every digit. A bit is stored by magnetizing around an aperture in one plate in one direction, and around the corresponding aperture in the other plate, in the opposite direction. The Z windings of the plates are connected in series opposition, as shown on Fig. 11. Therefore on reading, the disturbing signals of the two plates tend to cancel each other, and the polarity of the net signal is indicative of the stored bit. For writing, the inhibitng current is sent through the Z winding of one or the other plate. The use of a pair, instead of a single plate per word digit, is reasonable and not as extravagant as would be the use of two core arrays. The cost of the molded plate with its printed winding is inherently low, and the doubling of the number of plates has no effect on the labor involved in threading the stack.

To obtain storage capacities with more words than there are holes in a plate, an array of plates can be used for each digit, the Z windings being connected in series. The threading of the X and Y wires in the larger stack of plate arrays can be made in a single operation or by connecting together individually threaded plate

stacks. The limit to the possible number of words depends mostly on the method used to overcome the effect of the disturbances. Any of the methods developed for core memories are applicable. For example, strobing at a time where the disturbing voltage has decayed and the voltage due to the slower irreversible flux is near maximum, dividing the read cycle in two to allow the disturbance due the excitation of X to decay before Y is excited, or integrating over a positive and negative excitation cycle. The hysteresis loop of the plates is almost as square as that of the conventional individual cores, but the uniformity of properties between apertures is not quite as good as that resulting from the most severe core segregation, thus a somewhat greater reliance must be placed on the foregoing methods.

Switch Driven Plate Memory

In the early stages of development of the ferrite apertured plate, there was some doubt whether sufficient loop rectangularity could be obtained to operate by current coincidence. A method tolerating poor plate characteristics was devised. It consists of driving the memory plate stack by a switch which energizes the selected word location without half exciting any other locations. In this way the function of address selection is performed by the switch and that of storing by the memory stack. This method is advantageous even when the presently available prototype plates with good rectangularity are used, because the read-out signal is inherently devoid of any disturbances and is simpler to detect, the operation can be faster, and the drives can have larger tolerances.

The address selecting switch is itself made of a stack of plates identical with those of the memory stack, but without the printed windings, as shown on Fig. 12. The switch stack is threaded by X and Y windings, and is set in perfect geometrical register with the memory stack. Both stacks are threaded through straight address selecting conductors, one for each aperture. The threading of this forest of wires is relatively simple as it amounts to dropping a straight wire into each of the apertures. The ends of these wires are short circuited by rows in a manner to be described.

The "end-on" switch can produce outputs on one of the address selecting conductors as a result of the energization of the corresponding row X and column Y in a number of ways. For example, it could be biased with a pulsed or d-c inhibiting drive overcoming one of the lines drives, or it could be driven by driving the selected row and inhibitng all columns but the selected one, as was done in previous types of memory driving switches.

A novel method called "set-a-line" was found which has many advantages over previous types. Consider an array of switching elements, cores or apertures in a plate, shown for simplicity as an array of nxn cores on Fig. 13, ($n=4$). The loads to be driven by the switch and assumed of equal impedance z, are connected in parallel by rows, as shown on the Fig. 13(A). Let all cores be initially in a normal state N [Fig. 13(B)]. In a first step, a current pulse is applied to the selected row tending to drive all cores of the row toward P, and at the same time (or with a slight advance) another pulse is applied to the selected column tending to drive all the cores of the column towards N. As a result, all cores of the selected row are switched to the state P, except the one on the selected column which is kept in its initial state by the column inhibiting current. This produces the intermediary pattern of core states, Fig. 13(D). The voltage V_1 induced on the (n-1) cores which are switched over causes currents to flow in the corresponding loads and returns through the selected load. The equivalent circuit is that of a source V_1 connected in series with the selected load and the remaining (n-1) loads in parallel. Therefore the current I in the selected load is $+(V_1/Z)(n\text{-}1/n)$, while the current in each of the remaining (n-1) loads is $-(V_1/Z)(1/n)$. In a second step, a current is applied to the selected row tending to restore all cores to N. The inhibiting current on the selected column may or may not be left on during this step. This causes the (n-1) cores which were switched in the first step to switch back and induce voltages V_2, and thereby cause the flow of a current I in the selected load equal to $-(V_2/Z)(n\text{-}1/n)$ and a current $+(V_2/Z)(1/n)$ to flow in the remaining (n-1) loads. For both steps the currents in the unselected loads are (n-1) times smaller than the selected load current and therefore negligible in most practical cases when n is fairly large. The rate of change of flux of the switching cores can be made very high as the logic of the switch operation does not depend on the amplitude of the drive-row current which can be made as large as desired. Of course, the inhibiting column current must be made consequently larger. Therefore the voltages pulses V_1 and V_2 can be made of high amplitude and short duration. For symmetrical excitation V_1 and V_2 will be symmetrical, i.e. of equal and opposite amplitude. Asymmetrical operation is possible also, yielding a high and short positive pulse followed by a low and long negative pulse or vice-versa.

The polarities of energization of the

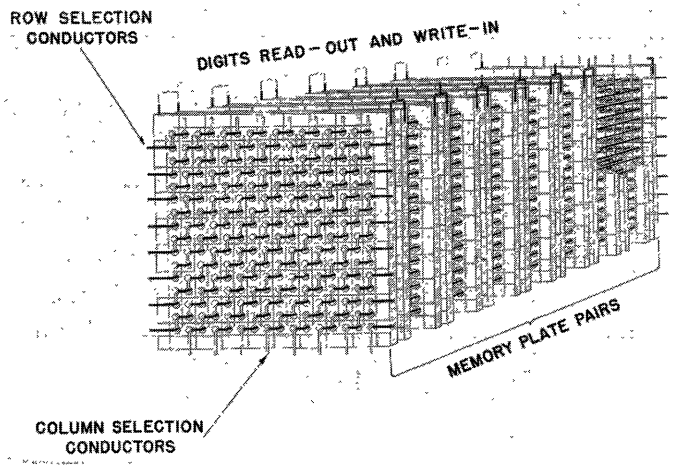


Fig. 11. Current-coincident ferrite plate memory

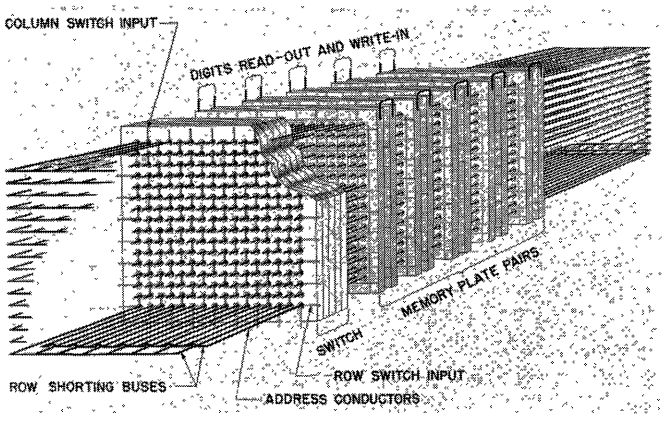


Fig. 12. Switch driven ferrite plate memory

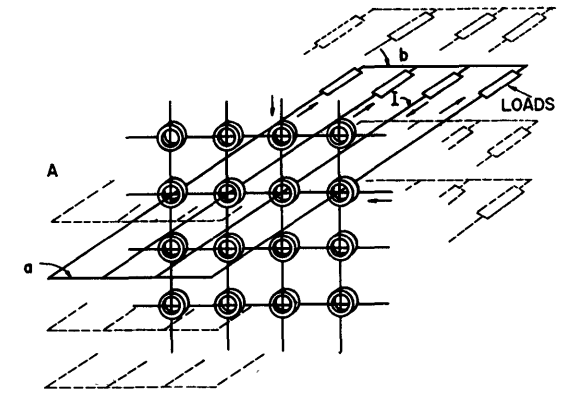
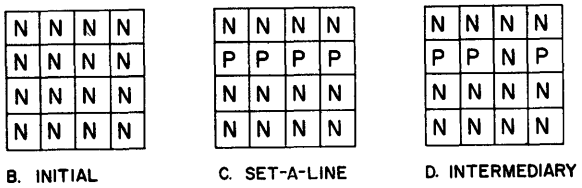
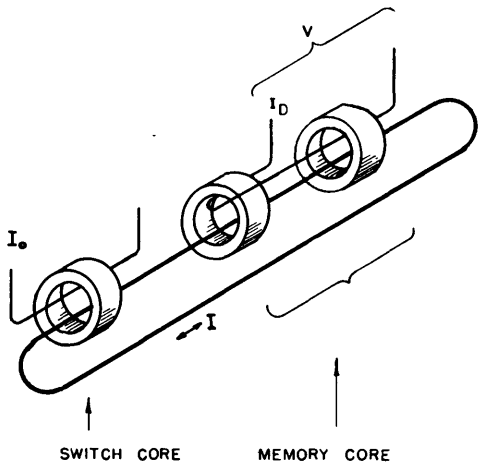


Fig. 13 (left). Operation of set-a-line magnetic switch





INITIAL	N	N	P
READ	P	N	N
REWRITE OR WRITE	N	N	P

Fig. 14 (right). Flux limited switch drive

load address conductors must alternate along rows and columns to conform with the checkerboarding because of the printed Z windings of the memory plates. This determines the back and forth threading of the row and column windings on the switch, and the use of interlaced shorting row buses on the ends of the address conductors, shown on Fig. 12.

It is of interest to note parenthetically that the first operating step could be split in two; a row drive and a subsequent column drive. The row drive swtiches over or "sets" all cores of the selected row and brings about the pattern of Fig. 13(C). These switch-overs produce a voltage between the shorting buses a and b, but no load currents, as there is no available return path for the current. The subsequent column drive, brings about the intermediary state shown on Fig. 13(D) and causes the same currents to flow in the loads as was the case when the row and drive pulses were simultaneous. This mode of operation involves no coincidences of driving currents. It may be useful in cases where the logic of addressing furnishes row information prior to column information.

The switch produces very small disturbing currents in the unselected loads corresponding to the selected row and column. On the row, these currents are due to the fact that the unselected loads are a part of the return circuit for the current of the selected load. They are small for all practical cases when there are many columns (i.e., $n>8$), as was mentioned. On the column, there are small disturbing voltages due to reversible flux changes around the apertures driven further into saturation by the column inhibiting current. Therefore the read-out signal from the switch-driven plate memory is almost solely due to the drive of the selected address conductor and is practically devoid of any masking disturbance.

A pair of memory plates is used for every bit of the word. A bit is stored by magnetizing around corresponding apertures of the two plates in opposite directions, in one direction or the other. This pairing was proposed for cancelling masking signals on read-out in the coincident-current operation, but is not necessary for that purpose in the switch-drive mode since there are practically no such signals. The purpose of the pairing is primarily to render constant the load presented to the switch by the memory. Irrespective of the nature of the stored word, there will be precisely M apertures around which flux reverses irreversibly, and M apertures around which flux reverses reversibly, since in every plate pair the two apertures are left in opposite states.

The use of plates in pairs permits operation of the system in a flux-limited fashion. To understand the system consider first the case of three identical square loop cores linked by a shortening loop of negligible ohmic resistance, as shown on Fig. 14. Initially, the switch core and one of the memory cores are assumed at N and the other memory core at P. In a first, read-out step, the switch core is reversed from N to P by a drive current I_o. Because the ohmic voltage drop in the shorting loop is negligible, the change of flux in the switch core must produce an equal total irreversible flux change in the memory cores, and therefore cause the memory core initially at P to switch to N, bringing both cores to N. The polarity of the read-out voltage induced on a digit winding linking the two cores in series opposition identifies which of the two cores switches over. In a second, write-in step, the switch core is restored from P to N by a drive current I_o of the opposite polarity. At the same time, or preferably with a slight advance, a current I_D is sent through the digit winding in one or the other direction depending on the digit to be written or rewritten-in. This current I_D favors the turning over of one of the memory cores and hinders that of the other. Consequently the flux from the switch core will be transferred to the memory cores in unequal parts, a larger part to the favored and a lesser part to the hindered core. For a sufficiently large amplitude I_{Do} of the digit write current I_D, all the flux will appear in one of the cores. For smaller amplitudes, there will still be a difference between the fluxes transferred to the two cores and consequently a logical write-in, which can subsequently produce a read-out signal of correct polarity even though it is of reduced amplitude.

The example of the three identical cores illustrates the operation at one address of the flux-limited end-on switch driven plate memory system. Let the number of plates making up the switch be such that the maximum amount of flux that can be reversed in the switch be just equal to the amount of flux to be reversed in M memory plates, one for each pair. When plates of the same thickness as the memory plates are used this number is equal to M. Fewer thicker plates can be used also. The elements of the ideal-

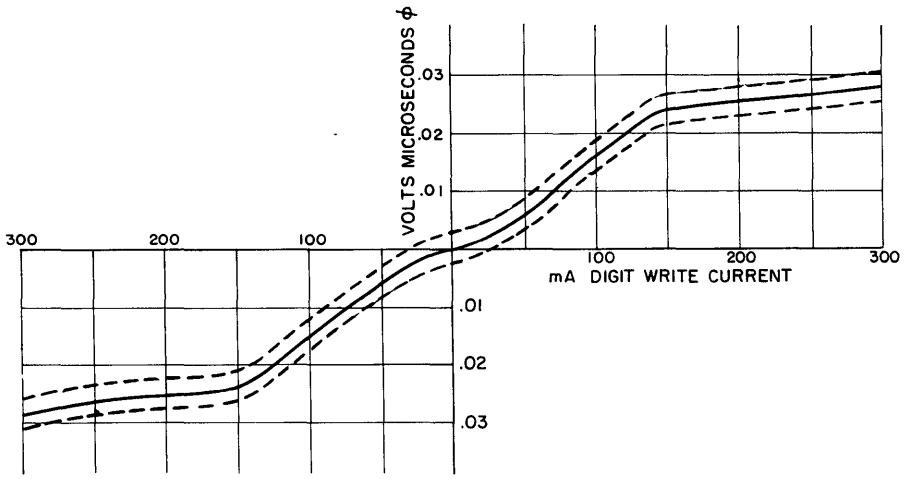


Fig. 15. Read-out as a function of digit write current

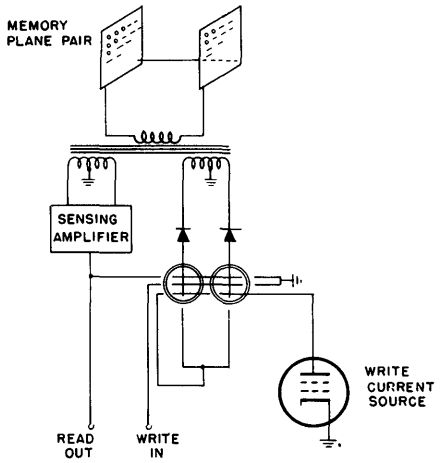


Fig. 16. Digit sensing and writing circuit

ized circuit of Fig. 14 are approximated at every location as follows: the switch core by the (n-1) row apertures around which the flux reverses, the shorting loop by the address conductor in series with the (n-1) other conductors in parallel, and the two memory cores by the $2M$ apertures of the memory plates. The circuit includes also the selected aperture of the switch, which does not switch-over during selection, and which adds negligible impedance to the loop.

The flux limited mode of operation has a number of advantages. Because the amount of flux transferred to the memory is strictly limited by that available in the switch, very large drive currents I_0 (and consequently large but short loop current pulses I) can be used to obtain fast switch over and large read-out voltages for relatively small stored-in write energy. Considerably faster speeds are possible than those obtained with a nominal current adjusted for maximum 2-to-1 discrimination. There is considerable tolerance in the amplitude of the write-in digit current. This is illustrated by typical plots of the net read-out signal (difference in flux between the two plates of the pair) as a function of that current; see fig. 15. The middle full curve is obtained when the two plates of the pair are identical, and the dotted curves are indicative of curves that could be obtained with plates differing in thickness or some other parameter. There is a minimum to the allowable digit write-in current necessary to compensate for possible differences between plates. There is a maximum over which the write-in digit current would produce irreversible demagnetizations in the nonselected apertures of the plate. This maximum is considerably greater than the value for which substantial read-out signals are obtained. The allowable extreme values depend somewhat on the switchover time. In practice, there is a tolerance of about 2-to-1 in the amplitude of the digit write-in current.

Associated Circuits

The plates are provided with a single digit winding obtained by a fairly simple printed technique. The more complex techniques for printing two windings are not necessary because the use of a pair of plates per digit makes it possible to design fairly simple circuits operating on a single winding for both sensing the read-out and writing the desired digit.

Such a typical circuit is shown by the block diagram of Fig. 16. The digit winding is coupled through a transformer to a sensing amplifier which produces a current of one or the other polarity depending on the polarity of memory output. This current sets an auxiliary pair of square loop cores, one core in state N and the other in state P or vice-versa. Rewriting is obtained by steering a current from a driving source through one or another of two windings wound in opposite directions on the transformer and thereby inducing a current in the digit winding in one or the other direction. During rewrite the sensing amplifier is gated off. For writing new information, the auxiliary cores are set by the write-in signal instead of the sensing amplifier. It is convenient to use transistors for the sensing amplifier and a tube drive current source common to all digit circuits.

The address circuits for the plate memory can be one of the many types used with core memories. In general the requirements are less severe. In the current-coincident mode considerably less driving power is required than that required for the core memory, because the energy stored per bit is about 5 times smaller around the aperture of a plate than in a conventional core. Also the smaller amplitude of the row and column currents gives a better match to tubes or transistors. The switch-driven plate memory requires more power because the switch itself dissipates power. However, the very large tolerances of the driving currents make possible simpler circuits.

Conclusion

Apertured ferrite plates are proposed for building high-speed random-access memories. They provide a simple means to fabricate large numbers of discrete storing cells in convenient packages which can be easily assembled into large memory systems. Furthermore, the cells can be made small so as to require little energy to store each bit.

A prototype experimental plate and means to use it in memory systems were developed which realize to a large extend the expectations of this proposal. The findings of the development may be summarized as follows.

The prototype is a molded square plate 0.830 by 0.830 inch having 16 by 16 = 256 apertures 0.025 inch in diameter and spaced on 0.050 inch centers. Measurements show that:

(a) There is negligible interaction between apertures.

(b) In lots of hundreds of plates taken from thousands the properties between apertures of a given or different plate are approximately within ±5% of an average value.

(c) The hysteresis loop around each aperture has good rectangularity.

(d) At 330 ma drive the flux reversal around

each aperture occurs in 2 μsec and produces a peak voltage of 30 millivolts. The energy stored per bit is less than 2×10^{-8} joules.

(e) The fabrication, testing, and assembly of memory plates is relatively simple.

The memory plates can be used with conventional 2-to-1 current-coincidence drive. This is particularly suitable for compact, lower power consuming, transistor driven, memories of relatively small capacity.

A new method is proposed of driving memories particularly suitable for plates. The memory plates are driven by an end-on switch itself made of plates. The switch operates in a set-a-line and flux-limited fashion and the memory uses plates in push-pull operated pairs. This results in a mode of operation permitting fast access, large storage capacities, and allowing large tolerances in the timing and amplitudes of driving currents.

We ventured to predict 3 years ago[3] that microsecond random-access memories with capacities reckoned in millions of bits, megabits, would be available at a relatively low cost in a distant future. We believe that the ferrite aperture plate is now ready to usher in the era of such memories. It will follow the present era of core memories with capacities of hundreds of thousands of bits. But the demand for larger and faster memories is incessant, and we may look forward to the development of new techniques making possible storage of billions of bits.

References

1 Digital Information Storage in Three Dimensions Using Magnetic Cores, **J. W. Forrester.** *Journal of Applied Physics*, vol. 22, Jan. 1951, pp 44–48

2 Static Magnetic Matrix Memory and Switching Circuits, **J. A. Rajchman.** *Radio Corporation of America Review*, vol 13 June, 1952, pp. 183–201.

3 A Myriabit Core Matrix Memory, **J. A. Rajchman.** *Proceedings*, Institute of Radio Engineers, vol. 41 (October, 1953), pp. 1407–21.

4. Multiple Magnetic Storage Systems, **R. C. Minnick, R. L. Ashenhurst.** *Journal of Applied Physics*, vol. 26, no. 5, May, 1955, pp 575–77.

A Cryotron Catalog Memory System

A. E. SLADE H. O. McMAHON

THE CRYOTRON,[1] a new computer component based on the phenomenon of superconductivity, may have an important influence on future developments in the field of computers and data-handling machines. At the present time the cryotron has a slower switching speed than transistors, but there are reasons for believing that the speed can be increased considerably.

The cryotron is extremely small, inexpensive, and, from all that is known, highly reliable. These advantages tend to offset the disadvantage imposed by the necessity for a constant supply of liquid helium.

Description of the Cryotron

The cryotron is a computer element whose operation is based on the destruction of superconductivity by a magnetic field. In its present form the cryotron is a tantalum wire nine mils in diameter (called the "gate") around which is wound a 3-mil niobium wire (called the control coil); see Fig. 1. When the cryotron is immersed in liquid helium both the control coil and the gate become superconductive; i.e., they have zero resistance. Superconductivity was dramatically demonstrated by Prof. S. C. Collins by an experiment in which a persistent current of several hundred amperes was induced in a lead ring immersed in liquid helium. The current continued from March 16, 1954 to September 11, 1956, at which time the experiment was voluntarily discontinued. During that time there was no measurable decrease in the magnitude of the current.

Fig. 2 is a plot of resistance versus control coil current for a typical niobium-tantalum cryotron. The slope of the curve in the transition region is dependent upon the current in the gate. The curve shown is for a gate current of 50 milliamperes. Larger gate currents produce a slight heating effect when the wire starts to become resistive and thereby causing a more abrupt transition. If a current of suitable strength is passed through the niobium control coil, the magnetic field will restore the tantalum gate to its normal resistance, while the niobium which has a much higher transition temperature, will remain superconductive.

Fig. 3 is a plot of the critical magnetic field (the field necessary to cause a superconductor to become resistive) versus temperature for a number of superconducting materials. In each case the curve represents the outer boundary of the superconductive state. Tantalum is a convenient gate material because it is restored to the resistive state by a relatively small external magnetic field whereas niobium remains superconductive in very-high magnetic fields. Both materials are available in wire form.

Principle of Operation

There are certain general principles that apply to all cryotron circuitry. The first of these is that the cryotron, in its present form at least, is a low impedance device and must therefore be operated from a current source, although it is conceivable that similar devices may eventually be developed which have such a high resistance that this restriction will no longer apply. The second is that, when the cryotron is used as a switch, the ratio of ON resistance to OFF resistance is infinite; consequently, in cryotron circuitry when current is offered a choice between two cryotrons, one superconductive and the other resistive, all of the current will flow in the zero resistance path. A third principle is that multiple superconducting paths in parallel usually are avoided. If parallel superconducting paths were allowed, the current would initially divide inversely as the ratio of the inductances, but a subsequent slow redistribution would occur if there were any slight imperfections that would cause minute parasitic resistances. Moreover, an arbitrary division of current among several paths would reduce the current in any one path to so low a value that it would be inadequate for a control coil. In general the current flows in a series superconductive path through gates and coils, the specific order and arrangement of which are characteristic of the particular circuit. One current source can usually supply all of the d-c requirements of the circuit.

A. E. Slade and H O. McMahon are with A. D. Little, Incorporated, Cambridge, Mass

The authors wish to thank D. A Buck for his help and enthusiasm in all phases of this work The work reported in this paper is supported by the U. S Army Signal Corp under Contract No DA 49-170-SC-1986.

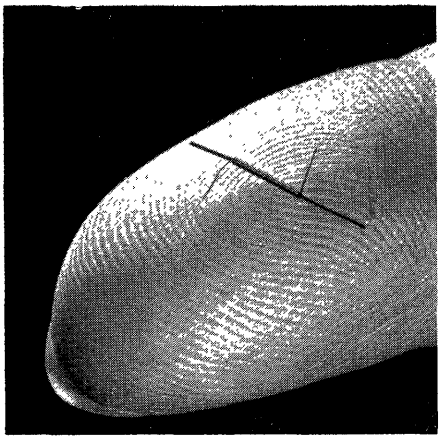


Fig. 1. The cryotron

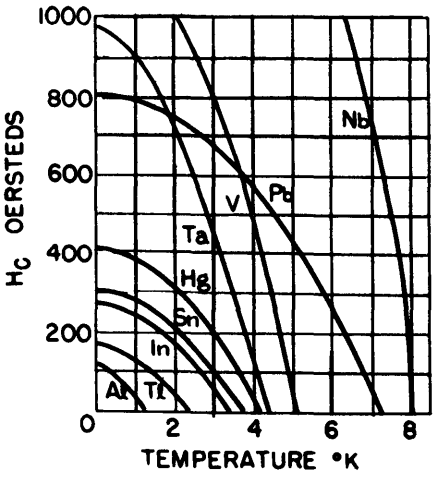


Fig. 3. Critical field versus temperature for various superconductors

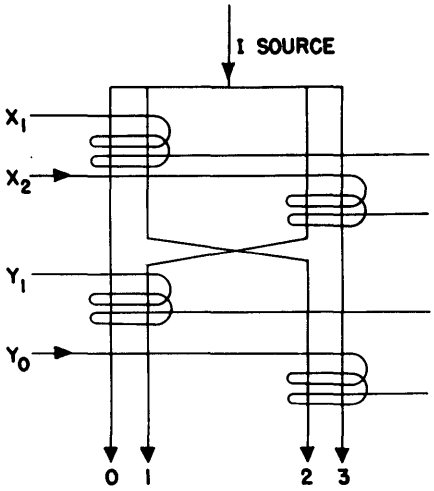


Fig. 5. Single-pole four-position cryotron switch using multiple gate cryotrons

The binary switch shown in Fig. 4 is an example of a simple cryotron circuit. The heavy lines represent tantalum wire; all other lines represent niobium wire. The cryotrons are arranged in this circuit so as to form a single-pole 4-position switch. If control circuits X_o and Y_o are energized, current is carried only in path zero, since all other paths contain at least one resistive tantalum gate. Each binary combination of inputs selects a single specific current path, zero through three.

It is possible to control more than one gate by means of a single coil. The only restriction on the number of gates that can be used in this manner is that the current in the coil must create a supercritical magnetic field within its entire cross-sectional area. With this modification, Fig. 4 can be redrawn as shown in Fig. 5, where, for simplicity of construction, single lengths of insulated tantalum wire are threaded through the coils. It is obvious that a very large switch could be constructed if one threaded a great many tantalum wires through an appropriately large number of coil forms. The number of paths or poles is related to the number of binary coil pairs by the expression $2^c \geq n$ where c equals the number of coil pairs and n equals the number of switching paths.

D. A. Buck[1] has shown that cryotrons can be interconnected to form a flip-flop, and to perform logical functions provided they are constructed so as to have current gain. That is, if one calculates the maximum current that can be passed through the gate without quenching because of its own magnetic field, and then divides that current by the minimum control winding current necessary to quench the gate, the ratio must be greater than one. Fortunately, this is not difficult to achieve. It can be shown that the current gain is determined only by the ratio of diameters of the wires used to construct the gate and control coil, provided the latter is close wound, i.e., in such a way that each turn is adjacent to the next. The maximum current the gate can carry without self quenching is:

$$I_{g\,\max} = H_c \pi d_g$$

where H_c is the critical field for the gate material in ampere turns per meter and d_g is the diameter of the gate in meters. The minimum control winding current necessary to quench the gate is given by:

$$I_{c\,\min} = \frac{H_c L}{N}$$

where again H_c is the critical field for the gate material in ampere turns per meter. Since N/L is the number of turns per meter, then in a close wound coil N/L is equal to the diameter of the control coil wire, d_c. Hence:

$$I_{c\,\min} = H_c d_c$$

and the current again is therefore

$$\frac{I_{g\max}}{I_{c\,\min}} = \frac{\pi d_g}{d_c}$$

A flip-flop can be constructed with two cryotrons, as shown in Fig. 6. A current source will flow through one or the other of the two gates but not through both, since the gate of one is connected in series with the control coil of the other. The circuit is bistable, i.e., once the current is established in either path it will lock in by causing the alternative path to be resistive. Fig. 7 shows how a complete flip-flop is constructed with input cryotrons C_5 and C_6 to provide a

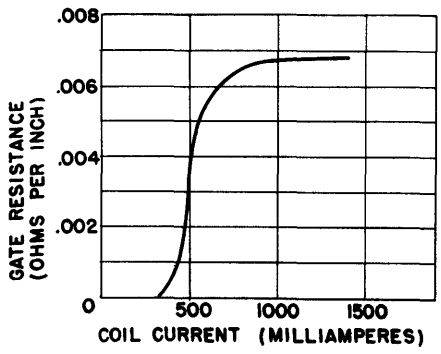


Fig. 2. Gate resistance versus coil current for a tantalum-niobium cryotron

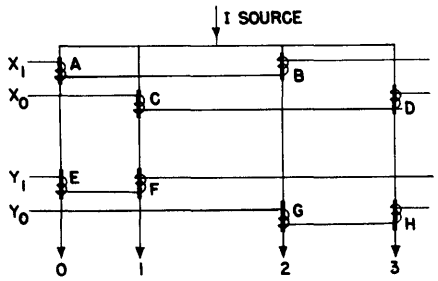


Fig. 4. Single-pole four-position cryotron switch

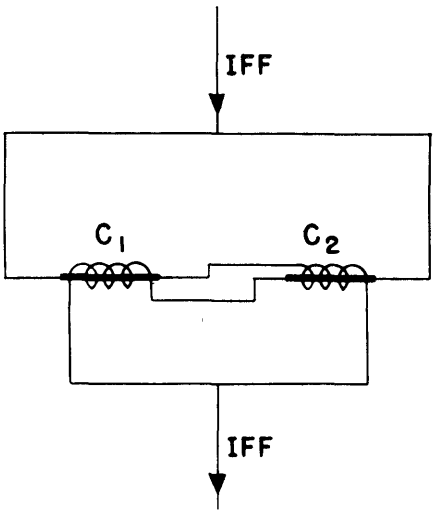


Fig. 6. Cryotron flip-flop

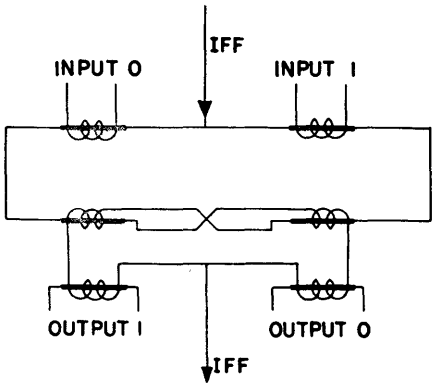


Fig. 7. Cryotron flip-flop with input and output gates

means for switching the flip-flop and output cryotrons C_3 and C_4 to provide a signal to other cryotron circuits.

The switch of Fig. 5 and the flip-flop of Fig. 7 are the basic circuit elements used in the design of the following catalog memory.

A Parallel Bit-Series Word Memory

The particular memory system about to be described differs somewhat from the random-access memory commonly used as the main internal memory for digital computers in that a word is recognized as being contained in the memory but can not be read-out.

Fig. 8 is a block diagram of a cryotron catalog memory. The current source flows from bus bar A through word no. 1 to bus bar B, from bus bar B through word No. 2 to bus bar C, and so on. Each word is composed of N parallel paths, and each path is a cryotron circuit capable of storing and recognizing

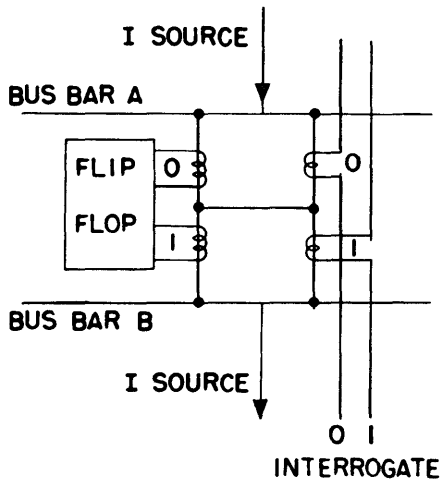


Fig. 9. One bit of cryotron memory showing interrogation circuitry

one bit of information. When the memory is interrogated, some of the bit-circuits become resistive and some remain superconductive. If the interrogation word exactly matches a word in the memory, than all of the bits of that word become resistive. A matched condition is signaled by a voltmeter indication of the IR (current-resistance) drop across the word bus bars.

Fig. 9 is a circuit diagram of one bit of the memory showing the interrogation circuitry. Each bit of the memory resembles a capital "H" suspended between the bus bars. The *zero* and *one* interrogation coils are wrapped around one vertical line of the "H", and the *zero* and *one* output coils of a cryotron flip-flop are wrapped around the other vertical line.

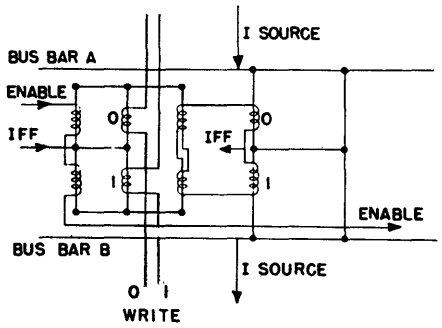


Fig. 11. One bit of cryotron memory showing write circuitry

Either the *zero* or the *one* coil of the flip-flop will always have current in it. Similarly, when the memory is being interrogated, either the *zero* or the *one* interrogation coil will have current in it. The purpose of the "H" is to provide a superconductive path from one bus bar to the other if, and only if, the interrogation bit does not match the bit stored in the flip-flop.

Fig. 10 is a diagram of a 9-bit memory where each bit is similar to the bit shown in Fig. 9. An example will illustrate how the memory functions. Assume that three words *010*, *011* and *000*, have been stored in the memory. These words are indicated in Fig. 10 by the arrows in the output coils of the flip-flops. Assume also that the memory is interrogated with the word *000*. All of the *zero* interrogate coils in all the words will carry current and the portion of the "H" under these coils will become resistive. In word no. 1, the current can flow through the second "H" but not the first or third.

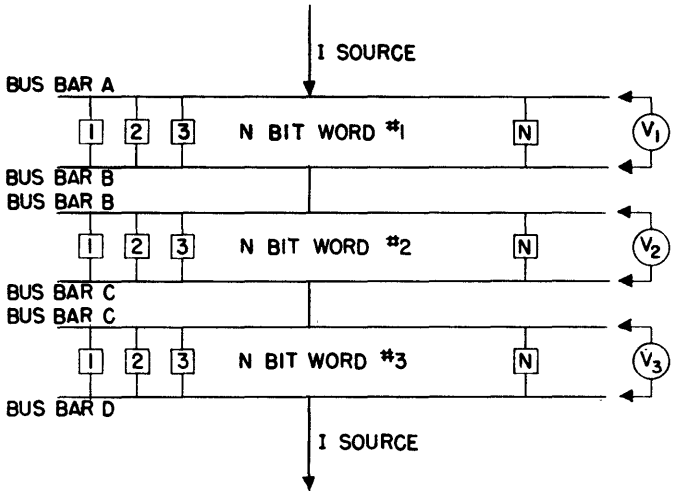


Fig. 8. Block diagram of cryotron catalog memory

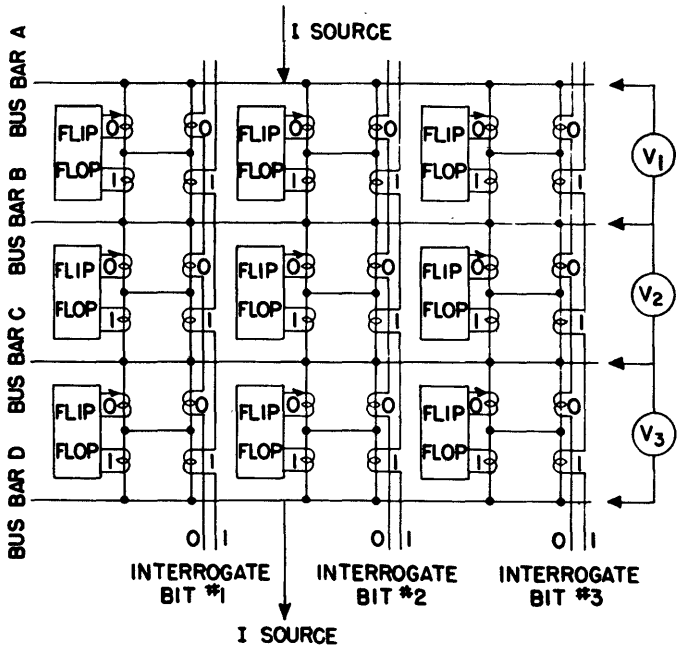
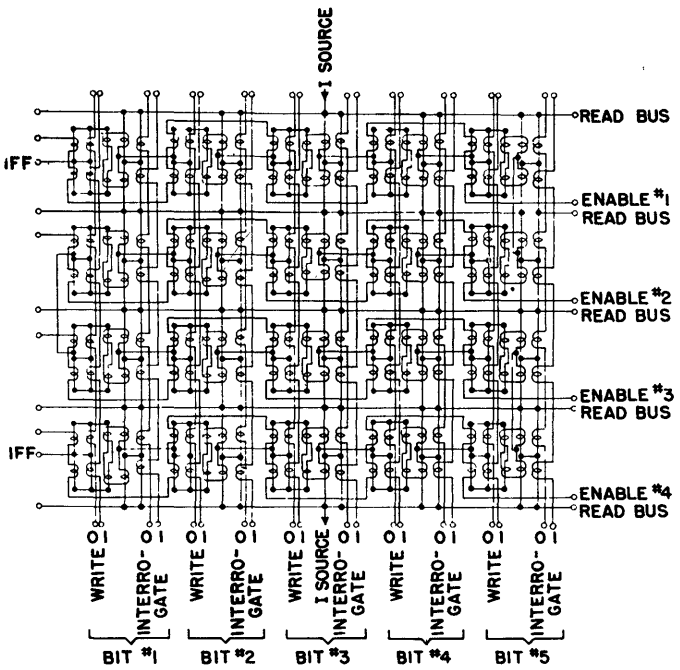


Fig. 10. Nine-bit cryotron memory



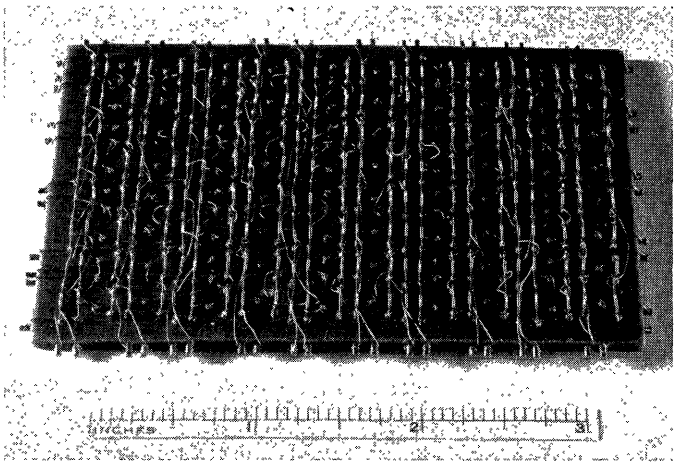


Fig. 12 (left). Detail of a 20-bit portion of cryotron catalog memory

Fig. 13 (above). Cryotron memory mounted on phenolic board

V_1 will read zero because the second "H" is a superconductive short. In word no. 2, current can flow in the second and third "H" but not the first, and V_2 will read zero. In word no. 3, there is no superconductive path since that word exactly matches the inerrogation word, and V_3 reads the resulting IR drop.

The magnitude of the IR drop may be quite small for a memory with a long word length since there are many small resistances in parallel. In general, for the circuit of Fig. 10,

$$V = I_{\text{source}} \frac{R_g}{2N}$$

where R_g is the resistance of one gate and N is the number of bits per word. Typical values for tantalum-niobium circuits are:

$I_{\text{source}} = 500 \times 10^{-3}$ amperes
$R_g = .001$ ohms
$N = 25$ for one particular circuit

Therefore, the voltage drop is of the order of 10 microvolts.

Such a small output voltage creates a considerable problem but not an insurmountable one. The noise voltage is exceedingly low; noise energy due to thermal agitation is lower than that at room temperature by a factor of 4/293, and noise voltage for a given noise energy is low due to the low impedance level, and shielding provided by the double-dewar helium vessel is near-perfect. Several methods of amplification have been considered. It is possible to use an alternating current for I_{source} and obtain considerable voltage amplification by use of a small superconductive transformer immersed in the liquid helium. The gain-bandwidth product required for sensing the 10-microvolt signal at 100 kilocycles per second can be achieved with conventional vacuum-tube-amplifier techniques.

Another possibility is to provide an alternate path for the source current through the control coil of an output cryotron. In this case, before the memory is interrogated, one path (the memory) would have zero resistance and low inductance, whereas the other path (the output cryotron control coil) would have zero resistance and high inductance. Under these conditions the current would flow preferentially through the memory rather than through the output cryotron winding and would retain such a distribution if no parasitic resistances were present. As soon as one word in the memory becomes resistive, however, all of the current would be shunted through the output cryotron winding and indicate the event by causing the output gate to become resistive. This third method would be somewhat slower than the other two because of the time involved in switching the current from the memory to the output cryotron.

In a large memory it would not be feasible to have a separate voltage-indicating device for each word as shown in

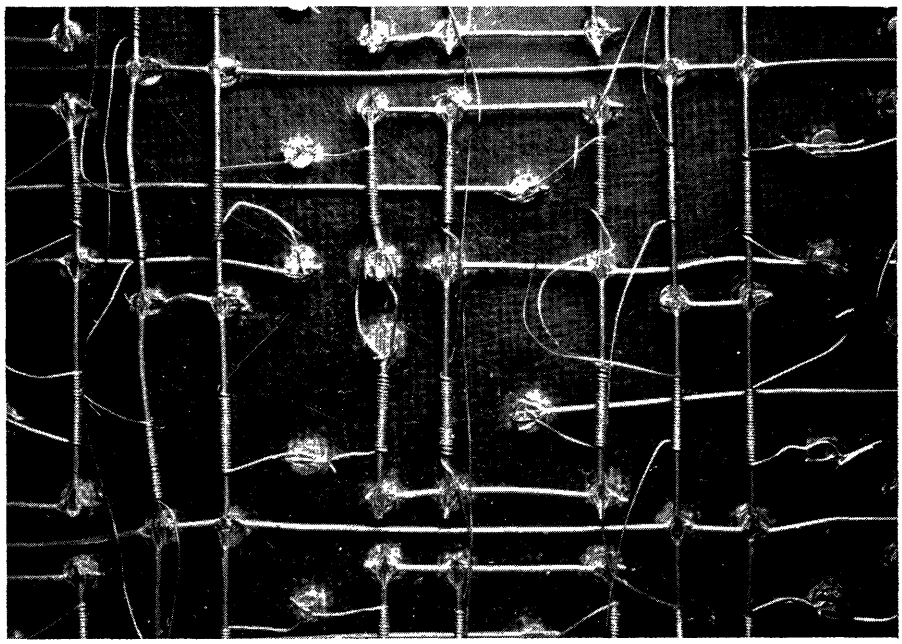


Fig. 14. One bit of cryotron memory enlarged

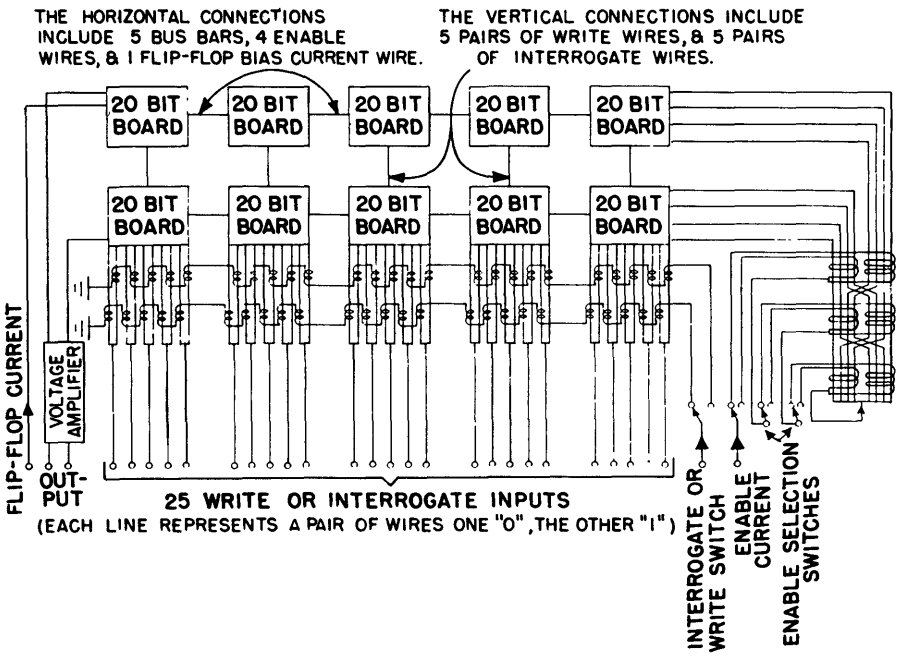


Fig. 15. The 200-bit feasibility model

Fig. 10. A memory of this kind in its simplest form would have only one voltage-indicating device connected across the output circuits of all of the words. The output would only indicate whether the interrogated word is included within the memory. It is possible to add additional sensing amplifiers and break the output circuit up in a variety of ways. For instance, the information in the memory might be ordered into any number of categories, there being provided one output for each category. When interrogated, an output would indicate not only that the word is stored but also its category.

Existing words can be erased from the memory and new words written at will. This is accomplished by changing the setting of the flip-flops. Fig. 11 is a diagram of one bit of the memory showing details of the flip-flop and input circuits. The flip-flop in the memory is similar to the flip-flop of Fig. 7 except an "and gate" has been added to the input. For the flip-flop to be changed, both the "enable" coils and a write coil must be activated. All of the enable coils of one word are connected in series. A cryotron switch similar to the one in Fig. 5, then selects the word to be written in by routing current to the enable coils of that word. After the enable coils are selected, the write coils are energized and a new word is written into the memory.

A detailed circuit diagram of a cryotron memory containing four 5-bit words is shown in Fig. 12. This 20-bit memory, made by welding cryotrons to niobium pins set in a phenolic board, is now under test see Fig. 13. The completed construction looks very much like the circuit diagram. Fig. 14 is an enlarged view of one bit showing the "H" circuit and the flip-flop circuit in greater detail.

The board shown in Fig. 13 is a building block for a 200-bit feasibility model under construction at Arthur D. Little, Incorporated. The boards will be stacked one on another to form a package about 3 inches wide by 3 inches deep by 4 inches high. They will be interconnected by means of superconducting wires connected to the pins on their edges. Fig. 15 is a diagram showing how the boards are interconnected to form a 200-bit memory.

The principal objectives of the present project are first, to demonstrate feasibility of cryotron circuitry in its present primitive state of development, and second, to explore the various engineering problems involved. A parallel project is being carried out to develop more economical means for constructing, assembling, and joining cryotrons. Only modest improvements in present techniques will be required in order to make the construction of a much larger memory feasible.

The present feasibility model will operate within a vacuum-jacketed container partially filled with liquid helium. This, in turn, is placed in a larger vacuum-jacketed vessel containing liquid nitrogen in order to minimize the helium evaporation rate. The joule heating that the memory will dissipate into the liquid helium is small compared with the normal evaporation loss of the container resulting from imperfect thermal isolation.

Conclusions

The cryotron memory described in this paper is designed to be used in a system with the following requirements: (1) capacity for storage of a large number of fixed-length words, (2) parallel interrogation with simultaneous access to the whole memory and (3) many interrogate operations and relatively few erase and write operations.

Cryotrons are rather limited in their operating speed at the present time. The exact interrogate and write speed capability of the memory is not known as yet; however, it is calculated that the memory can be interrogated every 10 microseconds and a new word can be written in about 500 microseconds.

The cryotron, even in its present relatively underdeveloped state, shows a great deal of promise for the construction of large information memories requiring fast access. Its principal advantages are the following.

Size: An individual cryotron, as shown in Fig. 1, is a very small device. Moreover, it appears that the only limitation on the density of assembly is determined by construction techniques. Unless other limitations appear, with greater experience, it is reasonable to expect that a large-scale digital computer would require less than 1 cubic foot of cryotrons.

Cost: Because of the inexpensive raw materials and the simplicity of construction the cost per bit is expected to be extremely low.

Reliability: No reliability experience has been accumulated on the cryotron. The most likely sources of trouble in present devices are the welded joints and the insulation. Once a circuit is assembled, however, it will be exposed to an almost ideal environment for the remainder of its life: an inert atmosphere at a temperature where all thermal activity has virtually ceased, electrically and thermally shielded from its surroundings.

References

1. The Cryotron—A Superconductive Computer Component, **D. A. Buck.** *Proceedings*, Institute of Radio Engineers, vol. 44, no. 4, April, 1956.

2. Superconductivity (book), **D. Shoenberg,** Cambridge University Press, 1942.

Discussion

L. R. Brown (Burroughs Corporation): How are interconnecting leads kept from being superconductors? What conductors do not offer superconductivity?

Mr. Slade: In cryotron circuitry the low impedance levels dictate the use of a constant current source. Since the amount of current is regulated at its source it is possible to use zero resistance interconnecting leads. Superconducting interconnecting leads are desirable in order to minimize joule heating. There are 21 known elements that display the phenomena of superconductivity in addition to many alloys. In general, however, the metals that are good conductors at room temperature (copper, silver, etc.) do not become superconductors at low temperatures.

M. L. Aitel (Radio Corporation of America): What is the size ratio between the memory and the required refrigeration system?

Mr. Slade: A large system like a cryotron general-purpose computer would probably have a self-sufficient refrigeration system. If the cryotrons used, say, one cubic foot of space, a helium liquefier designed for this system might use 20 to 30 times that much space. On the other hand, for a small system, such as a memory or function table, it might be satisfactory to have liquid helium delivered on a regular schedule. In that case the only space needed for the refrigeration system is the space for a dewar. The ratio of refrigeration equipment space to cryotron space would now be about 5 to 1, which is considerably less.

J. M. Feeney: What is the frequency response of the cryotron?

Mr. Slade: Dudley Buck has reported switching a single cryotron in 0.1 microsecond and there have been unofficial reports of faster switching times. However, the control coil of a cryotron is entirely inductive and if it is being driven by the gate of another cryotron, as it often is, the switching time of the circuit is much longer. The time constant of such a circuit is governed by the coil inductance divided by the gate resistance. For present-day cryotrons this switching time is about 500 microseconds.

J. W. Lacey (Dept. of Defense): Can some idea be given of the magnitude of current gain in a cryotron? Is it yet possible to predict which metals or alloys will be most suitable for cryotrons, or must an exhaustive search be made for better materials?

Mr. Slade: Yes, the magnitude of the current gain is calculated to be about 6 for present cryotrons. However, the actual current gain is usually somewhat less than this for reasons not yet clearly understood. A search must be made to find an alloy with a high normal resistance, a sharp transition from the normal to superconductive state, and a convenient transition temperature in order to achieve higher switching speeds while retaining other desirable characteristics.

J. R. Stock (Union Carbide and Carbon Corporation): What insulation is used for the niobium coil?

Mr. Slade: Teflon insulation is used for the coil and gate. This enables us to spot-weld through the insulation.

R. A. Stasin (General Electric Company): Is there any data on wire insulation and weld reliability when temperature is cycled from room temperature to 4 degrees absolute?

Mr. Slade: No, there is no data on this subject. However, troubles have not been encountered with either in conducting experiments.

W. H. Farrard (Autonetics Division of North American Airlines): What is the resistance of the 1/2 inch of wire when resistive? What currents are involved?

Mr. Slade: 0.001 ohm per inch is the normal resistance of 9-mil annealed tantalum wire. One current source of between five- and six-hundred milliamperes can serve for all of the power requirements in a circuit.

G. Hollander (Clevite Research Company): With how many gates have you actually loaded a flip-flop?

Mr. Slade: On the input to the flip-flop as many "or gates" as are needed can be used without any measurable circuit degradation. Input "and gates" are limited to two on the "set one" side and two on "set zero" side, unless special cryotrons with high resistance gates are used. On the output to the flip-flop the number of series output coils that can be used is limited only by the reduction in frequency response which can be tolerated by the addition of inductance to the circuit.

A Compact Coincident-Current Memory

A. V. POHM S. M. RUBENS

IN DEVELOPING higher speed computing equipment it is generally necessary also to develop faster memory systems which are reliable and efficient, and yet do not have prohibitive costs. This need has prompted many investigations of new materials and new fabrication methods.

One such investigation of the properties of ferromagnetic films evaporated in the presence of a magnetic field has been carried on by a group at the Naval Ordnance Laboratory at Corona, California. Their investigation revealed that it was possible to deposit thin films of permalloy or perminvar on glass substrates which had exceedingly rectangular hysteresis loops with almost the necessary coercive forces for coincident-current operation. The switching characteristics of these films also seemed as good or better than those of ferrite materials.

Because of the encouraging initial results, research in this field was continued by the Remington Rand Univac Division of the Sperry Rand Corporation in order to further investigate the properties of deposited ferromagnetic materials, and to determine the feasibility of using such materials in a coincident-current memory.

In the course of this investigation it was discovered that thin films of permalloy and, in particular, those with a zero magnetostrictive composition can be switched in a manner entirely different from the wall-motion switching which characterized the remagnetization process in bulk material. Experimental evidence indicates that with the application of a small magnetic field in the plane of the film, but perpendicular to the easy direction of the magnetization (cross-field), the films can be switched by a very rapid process equivalent to simple rotation of the total magnetization. (This has been discussed by C. D. Olsen, E. N. Mitchell, A. V. Pohm, and S. M. Rubens, in a paper submitted to *The Physical Review*.) Fig. 1 illustrates a family of switching curves with various cross-fields of a circular sample of evaporated nonmagnetostrictive permalloy 1-centimeter in diameter and about 2,000-A (Angstrom unit) thick as compared with 1/8-mil permalloy and S1 and S3 ferrites. Switching time here is defined as the period between the time the drive field reaches the coercive force and the time at which the output voltage has dropped to 10% of its peak value. Note that the slopes of the switching curves for the evaporated materials under these conditions are 4 to 8 times greater than that for 1/8-mil Mopermalloy, and 15 to 20 times greater than those for the fer-

A. V. POHM and S. M. RUBENS are with Remington Rand Univac, Division of Sperry Rand Corporation, St. Paul, Minn.

The authors wish to thank J. W. DeFord, C D. Olson, and other members of the St. Paul Phyics Department of the Remington Rand Univac Division of the Sperry Rand Corporation for their assistance in making the measurements and calculations which appeared in this paper.

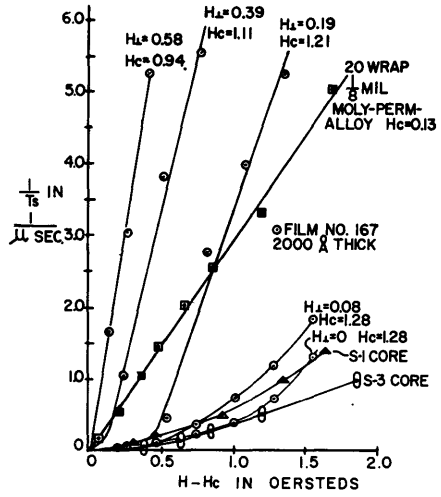


Fig. 1. Switching curves for 1-cm diameter of nonmagnetostrictive sample of evaporated permalloy as compared to other magnetic materials.

rite materials. Fig. 1 illustrates the very rectangular hysteresis loops which normally characterize evaporated permalloy materials.

For drive fields whose magnitude corresponds to points below the break or knee of the film switching curves of Fig. 1, switching occurs primarily by wall motion. Beyond the knee, switching occurs by means of the fast simple rotation process.

The threshold of the rotational switching process can be predicted with reasonable accuracy on the basis of a simple energy model, assuming that the potential energy varies as $\sin^2\theta$, θ being the angle between the total magnetization acting as as a simple dipole and the easy direction of magnetization. Fig. 2 illustrates the agreement within experimental error between threshold field conditions predicted by the model and those experimentally measured. $H_\perp'$ is defined as the magnitude of cross-field necessary to produce saturation in the transverse direction. H_s is defined as the magnitude of the switching field, and $H_\perp$ is defined as the magnitude of cross-field during the

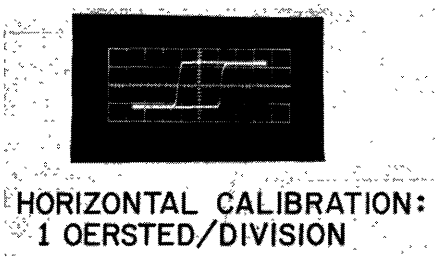


Fig. 2. Typical evaporated film 60-cycles per second hysteresis loop

switching process. Because of the good agreement between the values predicted by the model and those experimentally measured, the model can be used as an analytic tool.

In designing an evaporated core memory a compromise has to be reached between the various design requirements. Specifically, small drive currents, low power, easily fabricated etched-circuit wiring, adequate signal-to-noise ratios, maximum speed, and satisfactory reliability are desirable.

There are several satisfactory techniques which can be used to fabricate an evaporated core memory with etched wiring. In general, the choice of techniques will depend upon the type of operation and use of the memory. The coincident-current memory design, to be discussed in this paper, is one specifically intended for very-high-speed operation and uses the most simple construction techniques. Total memory cycle time is about 2 microseconds (μsec), and access time is something less than 1 μsec.

As indicated in Fig. 1, 1-centimeter (cm) circular evaporated plate-like films of 2,000 A thickness with coercive forces of 1 oersted are capable of coincident-current switching in times as short as 0.1 μsec when a suitable transverse field is applied.

The 1-cm plate-like sample on which these measurements were made is obviously much larger than an appropriate size to include in a memory. For a 2,000-A thick film, it is found that the diameter of the films can be reduced to 0.35 or 0.4 cm before film properties become seriously affected. If the diameter of a film is decreased beyond this, the demagnetization fields arising from free poles at the edges of the films cause the hysteresis loops to shear and the switching time to be considerably increased. The increase in switching time apparently results from areas of reverse magnetization created by the demagnetizing fields which impede the simple rotation process. The size of the memory element can be reduced further if some method is used to diminish the demagnetizing field. This can be accomplished, for example, with a suitable high permeability backing material.

The memory being described has simple film cores or "bits" 0.4 cm in diameter spaced on 0.8 cm centers. A circular shape was chosen to eliminate shape anisotropy effects as the magnetization undergoes rotation during the switching process.

The memory has a capacity of 1,024 words (32 by 32), 24 bits in length. The

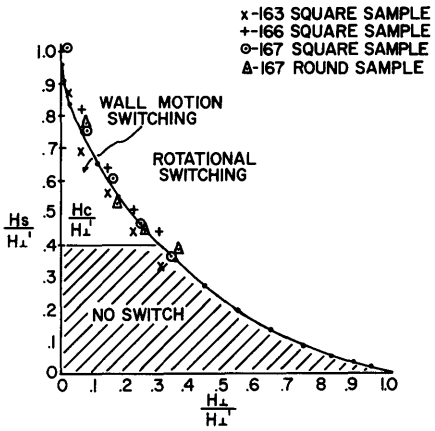


Fig. 3. Comparison of theoretical and experimental rotation threshold fields

memory elements are being evaporated in 16 by 16 element submatrices on about 30-mil thick glass plates about 5 inches square. In production, the core elements for a whole plane could be evaporated at one time.

One of the major fabrication problems in an ordinary ferrite core memory involves stringing the drive, inhibit, and sense lines through the individual toroids. The plate-like memory elements which are being used in this memory provide an opportunity to use simple multilayer etched wiring in place of the difficult stringing technique. Thin flat conductors are used for the drive and inhibit lines. The fields along the surface of the conductors are fairly uniform, and the core elements are placed in close proximity with the conductors. At the element positions, the horizontal, vertical, and inhibit conductors run parallel so that their fields superimpose and add algebraically to give

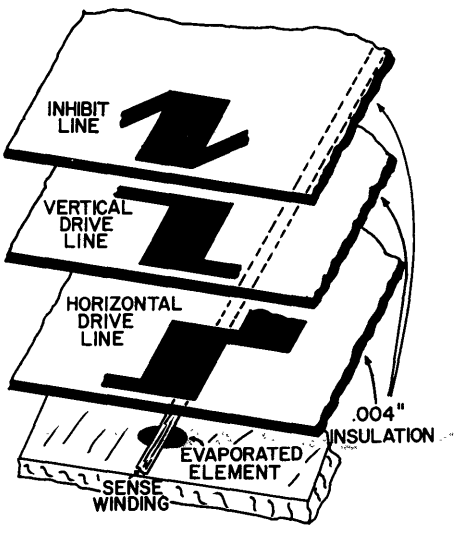


Fig. 4. Exploded view of wiring at evaporated memory element location

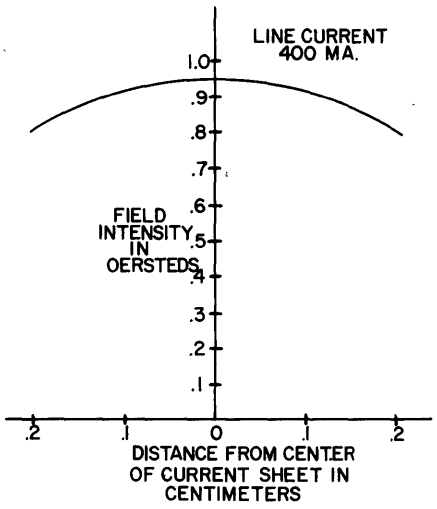


Fig. 5. Field distribution at element position

the necessary coincident-current operation.

Fig. 4 shows an exploded view of the etched wiring sandwich at a bit position. The sense winding is closest to the element, for maximum coupling, followed by the two drive lines and the inhibit windings. One-ounce copper is used for the windings with about 4 mils of insulation between the layers.

To minimize the drive current requirements and the inductance of the drive lines, the windings are placed on the top and bottom of the thin glass sheets on which the core elements are deposited to form thin loops. The drive lines in the region of the core elements are slit to prevent eddy currents which would damp the rotational switching. The slits are twisted slightly to alter the current flow direction in order to correct for the slight misalignment of the field caused by the bending of the drive lines in passing from one bit to the next. The field distribution from the top and bottom parts of a drive line at an element position is shown in Fig. 5.

The inductance of an isolated drive line is 2 to 3 microhenries, although, because of laminated etched wiring construction, the individual drive lines appear as low impedance transmission lines with characteristic impedances of 10 to 15 ohms. The propagation time down the full length of a drive line was computed to be 0.12 μsec with an attenuation of 7%. By breaking the drive lines into two halves, attenuation is kept to 3.5%, and propagation time is diminished to 0.07 μsec. By analyzing the drive pulse into its frequency components and checking the delay and attenuation for each component, it was found that very little distortion of pulse shape occurred. To provide the necessary 1-oersted fields per drive line, drive currents of about 400 milliamperes are necessary.

To achieve the rapid rotational switching it is necessary to provide a cross-field. This can be achieved in either of two ways. One can provide a cross-field by using an additional winding or coil, or one can provide the cross-field by rotating the "easy direction" of the magnetic element slightly with respect to the drive field. The best angle can be selected by employing the previously described model as an analytical tool. The slight-rotation method is being used because of its simplicity in the memory being described.

The sense winding is wound in a diagonal manner in each quadrant submatrix. The submatrix sense windings are connected together in a plus-minus-plus-minus manner in a clockwise direction. With perfect placement of the etched windings and the sense winding is very nearly zero.

Although the hysteresis loops of evaporated films are exceedingly rectangular, delta-flux changes do occur in the unselected cores when the film elements are switched by means of the simple rotation mechanism. This occurs because the field generated by the current in a single drive line causes a small rotation even though it is not large enough to cause the core element to switch. However, by rotating the sense winding by a slight angle it is possible to cancel delta noise completely irrespective of the digit distribution in the memory. This is achieved by positioning the sense winding so that the delta pickup arising from a stored *one* is exactly equal to that for a stored *zero*. Since the sense winding links successive bits along a given drive line with alternating polarity, exact delta noise cancellation is theoretically possible. The correct angle can be directly computed by employing the simple rotational model.

In order to make a practical memory, it is necessary to obtain adequate signal-to-noise ratios. Adequate signal-to-noise ratios have been demonstrated by physical measurement as indicated in Fig. 6 which shows the *zero* and the *one* signals from a bit in a 16 by 16 test matrix employing wall motion switching. By direct computation it can be shown that adequate signal-to-noise ratios are obtainable.

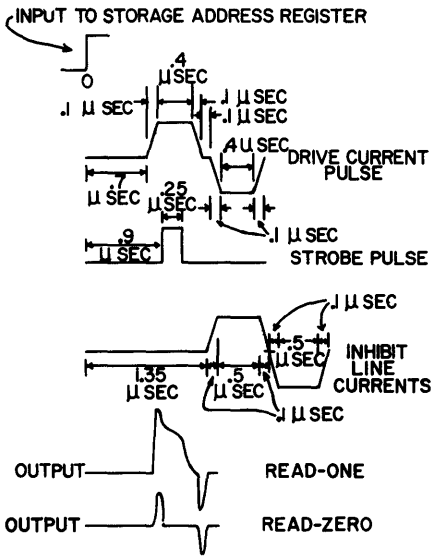


Fig. 7. Pulse timing

When a 0.4-cm core element is switched in 0.5 μsec a signal of about 4 millivolts is induced in the sense winding which has a characteristic impedance of about 20 ohms. The total voltage integral arising from the switching of a core element amounts to 1 millivoltμsec or a flux linkage of 0.1 line.

Etched-circuit engineers have indicated that the lateral registration of the various winding in the etched wiring can be kept in registration within 3 or 4 mils, and that the separation of layers can be kept uniform with 1 or 2 mils. If a random 2-mil variation in separation or 5-mil lateral displacement occurs between the drive lines and the sense winding, at a bit position, a net unbalanced linked air flux of about 0.003 line occurs. When a bit is selected by the coincidence of currents, the 62 unselected bit positions along the two drive lines, which are assumed to have random error variation in their positioning, give on the average an unbalanced mutual noise signal resulting from linking 0.025 line. Thus the unbalanced mutual coupling signal which occurs only during the rise and fall of the line pulses would have only one fourth the voltage integral of the switch signal. By strobing the output signal, good signal-to-noise ratios are obtained.

A second possible source of noise arises from the capacitive coupling between a selected drive line and the sense winding.

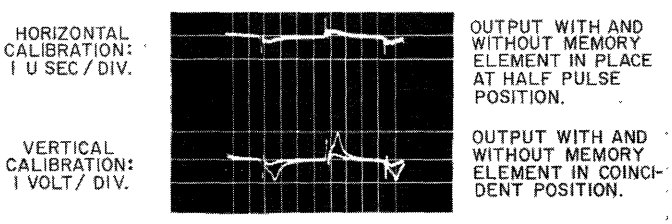


Fig. 6. Output from 16 by 16 test matrix plane using an resistance - capacitance coupled amplifier

By taking into account the coupling capacity, the drive voltage, the characteristic impedance of the sense winding and the phase delay, it can be computed that a noise pulse equivalent to linking 0.04 line of flux occurs. This again is considerably smaller than that which arises from switching a core element, and adequate signal-to-noise ratios are obtained by strobing.

A third possible source of noise arises from the capacity to ground of the primary winding on the transformer which matches the impedance of the sense amplifier to that of the sense line. By balancing the capacity to a grounded shield, the noise from this source is reduced by a factor of 10 to 100 below the noise arising from the unbalanced air mutual. Thus, as was experimentally indicated, the total signal-to-noise ratio is adequate.

The memory operating cycle is broken up into essentially three periods. A period of 0.6 microsecond is allowed for selection to take place. Two periods of about 0.7 microsecond are allowed for reading the information and then restoring. A diagram of the pulse shapes and time phasing are shown in Fig. 7. All of the necessary logical components are transistorized except the final line drivers, inhibit generators and the clock. Surface barrier transistors are used in the storage address register which is direct-current coupled to transistorized translators employing General Electric Type *2N123* and *2N167* transistors. The sense amplifier consists of a 3-transistor resistance-capacitance coupled amplifier with negative feedback. The inhibit-gating functions and digit storage are accomplished by transistorized components.

If the memory is to be interrogated every 2 μsec, each "on" drive line or inhibit line requires an input of about 2.5 watts with most of the energy being expended in the terminating resistors. If slower speed operation were satisfactory, power input to the inhibit or drive lines could be reduced to 1.3 watts by connecting in series the two halves of the drive lines or inhibit lines which are driven in parallel in the faster arrangement.

In a crude experimental setup it is estimated that evaporated core elements can be produced for 1 cent apiece or less. Production techniques costs per bit element could be reduced to a few tenths or a few hundredths of a cent. Matrix wiring costs are estimated to be less than 1 cent per bit.

It appears that evaporated core memories offer considerably higher speeds at lower power levels and cost than are available with existing ferrite memories.

Discussion

O. J. Van Sant (Naval Ordnance Laboratory): What is the smallest value of the observed switching constant?

Dr. Pohm: It is assumed that you are interested in the comparison between the switching constants of films and the switching constants of other materials. It turns out that in the wall-motion switching mode, the film switching constant is roughly comparable to that of the ferrites. In the rotational switching mode in any reasonable film, if one defines the switching constant S by the equation $1/T = S(H - H_c)$, as we have done, the switching constant has values ranging anywhere from 10 upwards, simply meaning that a 1 oersted net drive will cause a film to switch in a 0.1 μsec or less.

C. R. Smallman (Arthur D. Little, Incorporated): Why not evaporate the necessary insulation and drive lines onto the glass substrate along with the evaporated cores?

Dr. Pohm: This is a very fine suggestion and offers the next positive step. As an initial effort, etched techniques were resorted to because they are well developed. This prevented involvement with additional problems, but it looks entirely feasible that evaporative wiring can be used, and economically so.

W. M. Wittenberg (International Business Corporation): What is your output voltage measured at the sense winding?

Dr. Pohm: The output voltage for a 1/2-μsec switch is about 4 millivolts.

T. R. Long (Bell Telephone Laboratories): How is heat dissipation in the system taken care of considering the insulating materials employed?

Dr. Pohm: There is very little magnetic material involved and the heat dissipation problem is negligible because of the large dissipating area. At most about 25 watts were put into the total memory, running at peak operating speeds. About 24 watts are being dissipated in terminating resistors so one has essentially the bulk of the whole memory dissipating about 1 watt. The films are not temperature-sensitive. One could probably operate them anywhere from -100 to about 100 degrees centigrade.

H. Moss (Burroughs Corporation): How is the effect of air flux interference avoided?

Dr. Pohm: The sense winding is essentially wound with zero mutual coupling to the drive, the only linkage that occurs between the two windings results from the presence of the elements.

K. Preston, Jr. (Bell Telephone Laboratories): What is the access time required for the 1,024 word memory? What driving current amplitude is required?

Dr. Pohm: The access time is primarily limited by the electronics. In the system being built, this will be about 0.8 μsec. The driving current is 400 milliamperes. per line.

R. M. Clinehans (National Cash Register Corporation): What is the signal-to-noise ratio? What is the ratio of output of *one* to *zero* disturb?

Dr. Pohm: The major signal-to-noise problem does not involve the core material. The core material itself is essentially perfect in this regard. The problem one has is essentially that of eliminating the noise contribution from unbalanced mutual flux and capacitive pickup. In the system that we have operated (namely, a 16 by 16 text matrix) the signal-to-noise ratio is of the order of 10-to-100-to-1 at strobe time

Datafile—A New Tool for Extensive File Storage

D. N. MACDONALD

Synopsis: This paper discusses the design and application of an advanced magnetic-tape storage system with facilities for automatic access to files as large as 200 million characters with average access times in the 5 to 20 second range. The Datafile System, which employs standard magnetic-tape and recording techniques, also provides an economical solution to many medium-speed random-access problems and avoids awkward and time consuming tape-handling processes.

ONE OF the natural extensions of magnetic tape from its original use as a sound recording medium has been as a high-capacity memory and input-output medium for digital computer systems. In this application the inherent advantages of plastic-based magnetic tape such as low-cost, high-recording reliability, and amenability to selective alteration, have greatly extended the usefulness of the computer system in a few short years, particularly in applications where the handling of large commercial files is involved. In adapting magnetic tape to digital use, it was fairly easy to modify a basic sound recording machine to provide rapid starting and stopping of the memory by employing servo controlled reels, and by adding parallel recording channels to obtain useful density. Since computer input-output operations and sound recording both involve a time-series operation, the use of reels has proved very practical, since it is easy to load the system manually at intervals. However, in many cases these very qualities place the technique at a serious disadvantage, particularly where access to and from memory is always under computer control. Here, the ideal device has a very large storage capacity, the time required to reach any one portion is the same as any other portion, and in any case is as short as possible. Furthermore, information is generally transferred to and from storage in discontinuous blocks or unit records.

This is the description of a time-parallel storage system, diametrically opposed to the conventional magnetic tape system. While a great deal of attention has been given recently to the solution of the generalized bulk storage problem through the use of rotating memories such as large drums or disks, very little has been paid to the use of normal magnetic tape for this application. There seems to be a strong tendency to associate its use completely with conventional machines and systems. The excessive access time and the trickiness and complexities of servo-controlled reels and manual tape handling lead us to the more expensive systems without first examining other desirable alternatives.

The Datafile system was developed on the basis of just this reasoning, with the object of retaining the low cost, inherent simplicity, and reliability of plastic magnetic tape while eliminating many of the difficulties of the more standard systems. Although capable of rather good random-access performance in many applications, it is not primarily a random-access system but rather a high-capacity magnetic-tape storage system designed specifically for digital computer system use. As such, its performance generally equals or exceeds that of corresponding conventional magnetic-tape systems with higher reliability and performance per dollar than either conventional systems or random-access systems.

It is not too far wrong to say that Datafile has been created to satisfy the problem of the user who needs one hundred or more tape machines but can not possibly afford them, and the problem of the field engineer who could not service them in any case. Let us take a look at one of the units in the system. Fig. 1 shows it with the covers on ready for use. Each machine handles 12,500 feet of 3/4-inch wide tape in 50 discontinuous 250 foot lengths. These 50 lengths are stored loosely in a partitioned tub or multiple bin, and brought out over a guide system which runs the length of the machine, as do a pair of large drive rollers.

A servo-positioned head carriage operates on a track underneath the tapes to position the recording heads underneath a selected tape, and this carriage carries a set of solenoid-operated pinch rollers to drive the selected tape. Only one tape at a time is driven, the others remaining in their last selected position.

It is immediately apparent that this is a two parameter selection system where any point in memory may be reached by selecting the proper tape and driving it to the proper position, thus making the Datafile system intermediate between the single parameter reel magnetic-tape system, and most three parameter random-access memory systems. Laid out flat, the recording surface is 3 feet wide by 250 feet long with facilities for positioning recording heads at any point on this surface. Of course, the basic Datafile technique can be employed with any standard digital recording system. since tape widths, speeds, recording systems, and formats can be varied to suit the occasion. Most of the following discussion, however, will be centered about its application to the Datatron computing system, to which the Datafile has first been attached.

This version employs 50 separate lengths of tape, with dual recording lanes on each tape to provide 100 selectable information lanes, each 1000 blocks long, for a total machine capacity of 22 million digits of information. At a tape speed of 60 inches per second any point in memory may be reached from any other in 14 seconds on the average. Of course, this average random-access time is directly related to the amount of storage required by a particular application. Where access to only 5 million digits is required, the average random access time reduces to 3.9 seconds. Fig. 2 shows the relationship between random-access time and capacity for a one machine system. The operating point on this curve is determined by the program. While the Datafile will operate with any length of tape less than maximum, it is generally kept loaded for the problem requiring the longest capacity, with other points on the curve obtained by restricting the area of tape searched, and the corresponding file size.

The addition of the Datafile system as an auxiliary to the Datatron magnetic-tape system requires little change to the central computer or tape control equipment. As in the standard system, a six channel parallel format is employed, utilizing four channels for binary coded decimal information, the fifth channel for parity code, and the sixth for marking blocks of twenty 11-digit computer words. The 3-digit block address associated with the block marker is carried in the formation channels, preceding the block.

D. N. MacDonald is with the Burroughs Corporation, Pasadena, Calif.

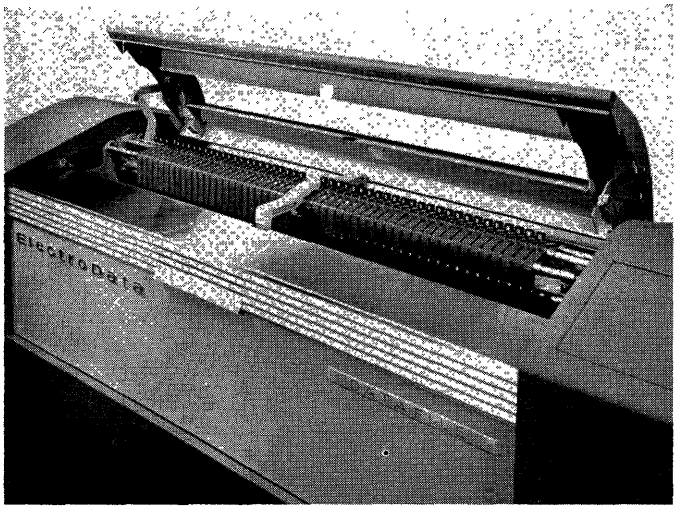


Fig. 1. Complete Datafile

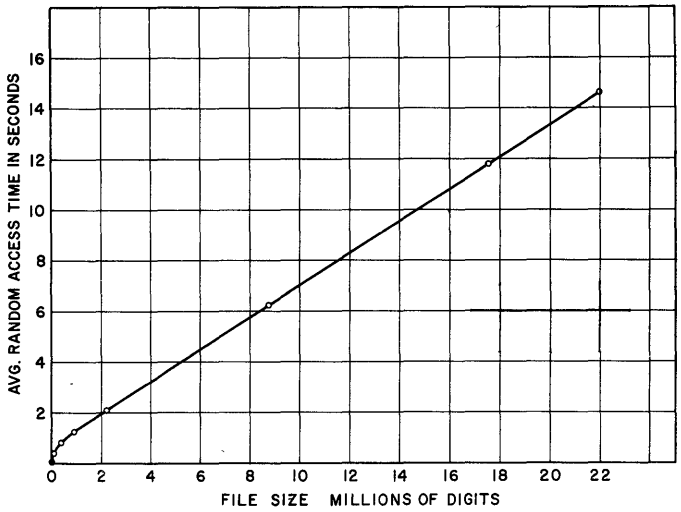


Fig. 2. Random-access time versus capacity

Nonreturn-to-zero recording is used, with a flux change representing a zero. The two recording lanes on each tape are interlaced, with the associated heads permanently connected in series to the read-write amplifiers. Switching from one lane to the other on a particular tape is accomplished by lifting the tape from the unselected head, which acts as a cross-talk cancellation transformer for the selected head. This dual lane arrangement, while not fundamental to the Datafile technique, has the advantages of reducing the number of individual tapes and associated hardware in the unit, increasing the efficiency of tape usage, and simplifying the job of the head positioning controls. Up to 10 Datafiles may be connected to the central computer system providing a practical machine-controlled memory of just under 1 billion bits for the first time. Like the normal magnetic-tape system, sections of the file may be replaced manually with new file sections, while individual tapes may be precalibrated for use and parity checked during operation to provide error free service. Standard instrumentation Mylar magnetic tape is used.

Fig. 3 shows the Datafile with the cabinet covers removed, and leads us to a discussion of the basic construction. While the handling of magnetic tape in bins is not new, two major difficulties have prevented more extensive application of this technique; the creasing of tape in the lower part of the bins due to the weight of additional folds on top, and the serious problems of cumulative electrostatic charge on the tape surface, causing the tape folds to stick together and interfere with normal bin loading. Creasing is avoided in the Datafile by limiting the tape length to 250 feet, and using baffles in the bin to support the tape folds. The electrostatic problem is minimized by the perforated metal bin partitions, which not only assist in drawing off electrostatic charges from the surface of the tape, but also prevent the buildup of air pockets underneath the tape as it is driven into the top of the bin. With this design it is possible to use standard tape over a wide range of environment with superior results, avoiding the use of conductive tape coatings.

Fig. 4 illustrates a cross section of the drive system at any particular tape position. The recording heads and magnetically operated pinch roller assemblies are mounted on the head carriage, while all other elements shown are fixed. Drive power is transmitted to the tape on the uncoated side to avoid tape wear. Tape tension against the heads and guides is provided by a pair of vacuum drag manifolds which apply a frictional drag on the back side of the tape only. These manifolds also detect the arrival of perforated leaders and trailers on each tape to prevent accidental unthreading of the machine by disconnecting the drive at the end of the tape. The head carriage assembly shown in Fig. 5 can be positioned at any tape by a servo-controlled metal band drive and operates on ball bearing rollers. Fig. 6 shows the time required for the head carriage to move between successive selected tapes. The average random traverse time is just under 1 second, corresponding to an interval of one third the total, or 17 tapes. This performance is obtained with an error-rate damped analog servo system operating in a precision d-c resistance

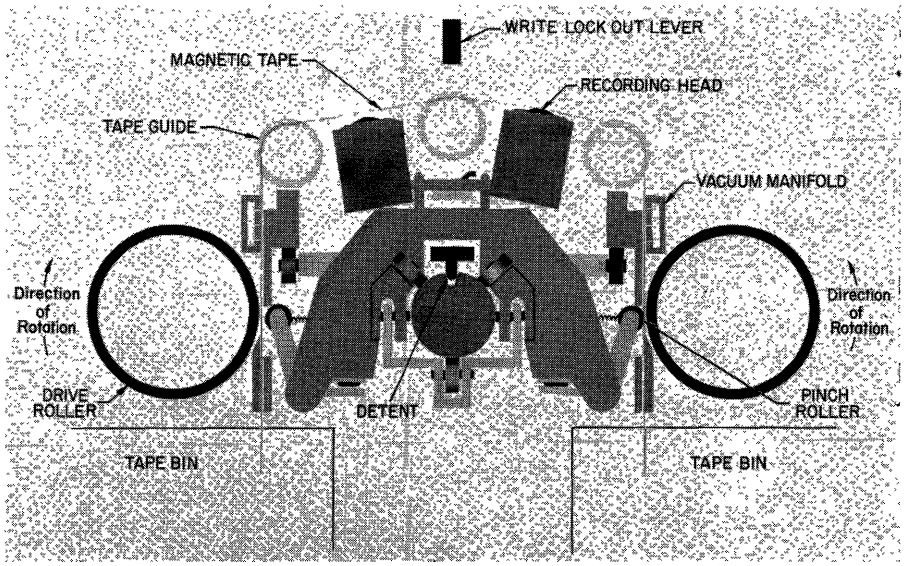


Fig. 3. Covers removed

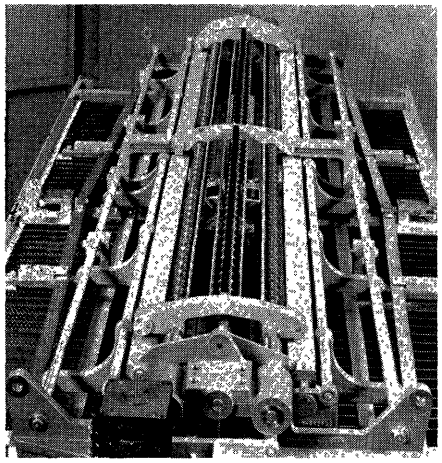


Fig. 4 (left). Drive system schematic arrangement

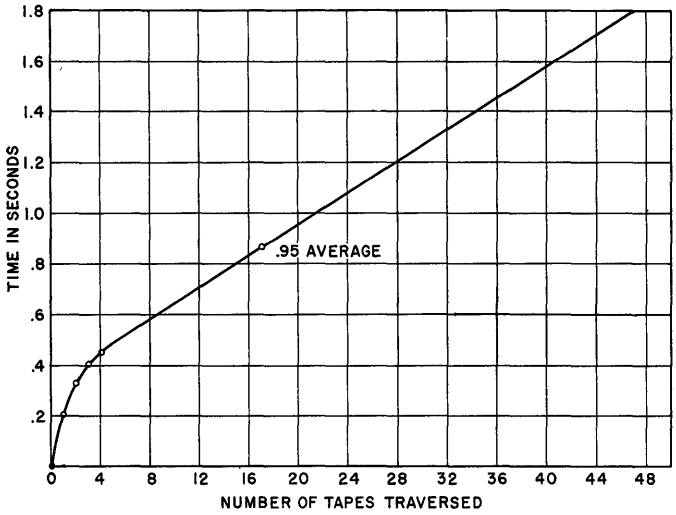


Fig. 6 (right). Head traverse time

bridge. On side of the bridge is resistance controlled by mercury relays to accomplish the initial digital to analog conversion. The carriage includes a magnetically operated detent which locks it into position underneath each tape in order to make head location independent of the servo system. This detent mechanism also serves to retract the heads from the tapes during the head positioning motion. Electrical connections to the head carriage solenoids and recording heads are brought in through a flexible cable which hangs freely below the head carriage in a space between the two sets of bin partitions.

The Datafile employs a built-in file protection mechanism to prevent inadvertent alteration of a portion of the file either by programming or machine error. Each tape position is provided with a lever which may be set and thrown to operate a switch on the head carriage at that tape position to prevent the two associated recording lanes from being altered. Any combination of lanes may be so protected. Individual Datafile tapes are stored on small reels when removed from the machine, and are loaded by means of a motor driven reel which can be positioned to any one of the bins. The drive rollers are retractable to provide for easy loading. Threading of the tape is accomplished by clipping a small weight to its end and dropping it into the bin.

In addition to servo controls, drive circuits for the mechanism, and preamplifiers for the recording heads, each unit has an automatic sequencing circuit which allows the machine to be completely rewound under local control after receipt of a rewind instruction from the computer. This is particularly useful for zeroing the memory without tieing up the central control, for operations such as sorting and sequential file processing. Used in conjunction with the Datatron tape control unit, the Datafile system is controlled by four basic instructions: search, read, write, and rewind. In the search instruction one digit specifies the desired Datafile unit, two digits specify the lane in that machine, and three digits specify the block in the lane selected. When the search instruction is received by the tape control unit, the central computer is cleared for computation while the search is executed independently. First, the particular unit is selected, and the two lane selection digits routed to it. Control circuits within the unit choose the proper recording head and convert the information to an analog voltage to control the head carriage drive. Upon completion of the lane selection the tape is driven in the proper direction and the block addresses on the tape are read and compared with the stored three digit block number until equality is reached, when the tape is stopped ready for the next instruction. This will usually be either a read or write instruction for up to 100 blocks of information, starting at the selected address.

Without going into the detailed application of the Datafile to machine filing systems, it is important to note some of the more significant factors involved, since file organization directly affects the efficiency of the system. The usual file is neither completely random nor completely sequential with respect to inquiries and transactions, but is frequently composed of random blocks of information which are internally ordered. If the file is forced into some sequence on

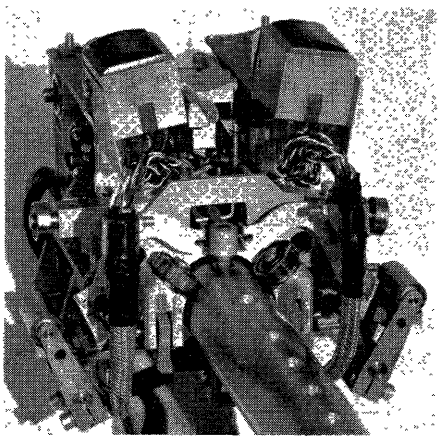


Fig. 5 (left). Head carriage

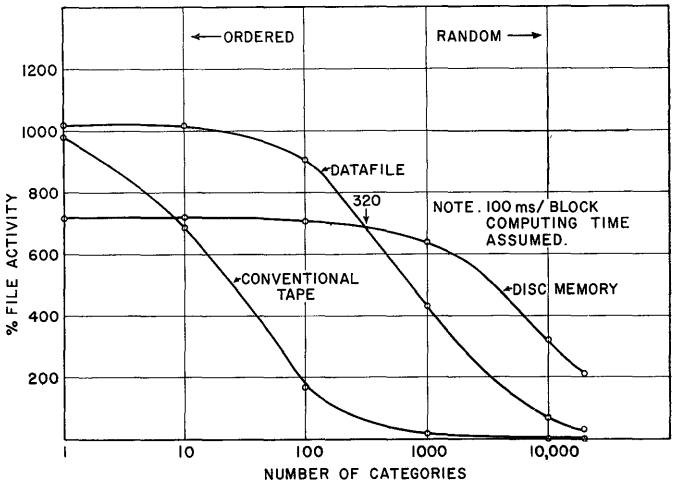


Fig. 7 (right). Performance comparison curves

tape, the transactions must generally be presorted if any system efficiency is to be maintained. On the other hand, the use of an expensive fractional-second random-access system is frequently unwarranted either because the randomness applies only to large blocks of internally ordered information, because the random access can be handled in the internal memory of the machine at high speed, or in the case of some problems where complete random access is required, the access time is not critical.

We are speaking qualitatively here of a figure of merit, since a better match between the machine filing system and the problem at hand allows the user to obtain higher capacity for his money, or to spend less money, or to do the job in less time, as he chooses. This situation is shown graphically in Fig. 7, which plots file activity against randomness for a conventional magnetic-tape system, the Datafile system, and a typical disc memory system. File activity is defined as the percentage of the total file which can be processed in a single 8-hour shift. For purposes of comparison the chart shows the results for a 20-thousand block file (4,400,000 digits). At the right hand side the superiority of the disc memory is clearly evident. Here, access time is all important in determining the efficiency of processing, since the systems are jumping rapidly from one small unit record to another. As we move left on the spectrum and pick up some degree of sequence the Datafile system takes over in preference because it is able to transfer strings of data at the higher rate of a conventional tape system, in this case 6,000 per second. At the purely sequential end, the conventional tape system and Datafile system are about equal in their ability to handle the file because of this fact, while the random access system has fallen far below. The chart indicates that the Datafile is superior in all cases to a conventional tape system in its efficiency, and indeed this is often the case. However, we must remember that the comparison was on the basis of a relatively small file. There are still many applications for sequential processing of large files where it is economically desirable to employ a storage cabinet full of tape reels in lieu of the automatic Datafile.

With these factors in mind, the hybrid role of the system becomes more clearly evident. Sometimes dubbed the poor man's random-access memory, it does combine entirely creditable pure random-access performance at rates up to several thousand transactions per hour with low system cost, and is the logical choice for extremely large but relatively inactive machine files. At the other end of the spectrum, in comparison with conventional tape systems, high performance magnetic tape operation is provided, while completely eliminating operational difficulties of manual tape handling and threading. Where the automation of highly important master records is involved, the elimination of all manual handling, the provision for foolproof file protection, and the increased reliability resulting from the absence of complex tape handling mechanism opens a new era in the electronic processing of business data, and provides the first economic solution to the large file problem. Conceived as an engineering solution to the problems of computer tape systems, the Datafile appears to provide an optimum match to the large majority of file applications, and represents a final departure from the difficulties incurred in the application of sound recording technology to the antagonistic requirements of digital data processing.

Discussion

S. Gitchick (International Business Machines Corp.): If the tapes were in the form of continuous loops, rather than free hanging, would not the search time be decreased?

Mr. MacDonald: The answer is yes. They were made discontinuous loops, primarily to avoid the problems of slip connections to the head carriage, and to simplify loading. We felt that the provision of the hanging connecting cable was more important than lowering the access time.

L. Lipschitz (International Business Machines Corp.): What pulls the tape off the friction surface and to the bin on the discharge side?

Mr. MacDonald: The geometry provides two drive points with pinch roller and capstan drive, forward and reverse. The friction drag means are in between these two drive sources, so that the drive in either direction is pulling against the drag means, and the heads were positioned in between. I think this may be a problem of confusion in the geometry of the drive.

J. N. Harris (Hycon Eastern): What is the expected operating life and reliability of the tape? What is the tape width used in the system?

Mr. MacDonald: This is a very difficult question to answer quantitatively since it depends upon the tape used and involves a discussion of particular tape brands. In general, however, tape life is in excess of about 30,000 passes; 3/4 inch in this particular application.

M. Muller (International Business Machines Corp.): Please explain the reading or writing action of file when a tape is at its end position? Also, can tapes be read in two directions?

Mr. MacDonald: This operation is again almost identical to that of the Datatron tape system, if the question has been understood correctly. The search operation proceeds in either direction, and the block address recorded on the tape can be read either forward or backward. However, the reading-writing operation occurs in the forward direction only.

E. Hertz (Sperry Gyroscope): Can rewind be controlled for individual lanes, or must all 50 have to be rewound together?

Mr. MacDonald: All 50.

L. J. Dean (Ramo-Woolridge): Is it possible to interrupt a posting program to interrogate the Datafile on demand?

Mr. MacDonald: Under program control, yes.

M. L. Aitel (Radio Corporation of America): Is dual recording used for each bit to obtain reliability, or is each bit recorded only once?

Mr. MacDonald: Each bit is recorded only once. The two heads function independently of each other.

Chairman Howard: How does the rubber drive capstan perform with respect to wow, etc., considering long-time wear effects as well as performance when new?

Mr. MacDonald: Generally, wow or flutter is not too significant in a digital system. In the Datafile, we hold it below 5%, which is quite adequate, and provides for reasonable wear.

W. L. Martin (Marchant Research): Is there a Mylar layer between the tape and the head?

Mr. MacDonald: No, there is not.

C. A. R. Kagan (Western Electric Company): One must assume that the servo-controlled movable read-write head is the more economical solution. How much more would a static 50 head electrically switched read-write system cost and how much would the access time be reduced?

Mr. MacDonald: Generally speaking a multi-channel recording head is in the $200 bracket, and if you multiply it by 100 heads, you have a great deal of money tied up in heads, as much or more than the Datafile

machine itself, while the access time has only been reduced by 1 second. Remember that 100 individual drive mechanisms are now also required.

R. M. Clinehens (National Cash Register Corporation): Can longer lengths of tape (1,000 feet) and higher tape speeds (240 inch per second) be used with this equipment to increase storage without increasing access time with only the obvious modifications?

Mr. MacDonald: Yes, the particular Datafile we have been speaking of is actually system-limited to the 6 kilocycles data-transfer rate. Higher densities and speeds have been successfully used. The Datafile has operated quite successfully up to 100 inches per second. The only limitation on capacity is physical size of the machine since we want to maintain the average tape density in the bins that we have now.

W. W. Sturdy (U. S. Army): Can the material at a given address be erased and new material be inserted in one tape pass?

Mr. MacDonald: Yes. The recording system erases by rewriting over the previous information.

Quasi-Random Access Memory Systems

GERHARD L. HOLLANDER

Synopsis: To select an economical memory for business data-processing systems, the memory characteristics must be matched to the work cycle, processing rate, and permissible delay time of the system. Quasi-random systems feature the low memory cost of serial memories, high processing rates, short delay times, and minimum sorting. An efficient addressing method and rapid cross references reduce the total storage requirements. Typical business examples illustrate the principles.

A RECENT paper[1] described a novel data-storage device, the TapeDRUM.* Before launching a development program, the characteristics of such a unit must be compared to the requirements of many applications to determine the practicability of the concept and the eventual specifications.

The TapeDRUM appears best suited for business applications. A business system is usually characterized by large storage and relatively simple computational requirements.[2] The need to store one billion bits of information is not rare. Often, any piece of the information must be accessible on short notice. For example, available credit on a charge account must be cleared within a few seconds to avoid annoying the customer. As the TapeDRUM is a new tool, a new approach to the organization of large-scale data-processing systems is needed. This paper summarizes several application studies which illustrate some new principles that may be applied to other memories of similar characteristics.

Many memory devices with different characteristics are available.[3,4] They are often classified as serial-access or random-access, and are usually selected according to their cost and access time (time needed to extract the desired information from the memory).

For any application, the lowest priced memory should be used if its access time meets the system requirements. By taking into account three new criteria, low-cost serial memory systems can be arranged to appear as if their access time were shorter. Thus the term "quasi-random" access has been coined for configurations useful to many business systems.

These quasi-random configurations generally combine large low-cost serial memories with smaller random-access devices, so that the average cost per unit of information storage is low. Significant savings over conventional approaches can be realized, which are illustrated by typical, but greatly simplified, examples. However, first the characteristics of various memories will be examined.

Memory Characteristics and System Requirements

Total storage requirements for a job often depend on the type of memory. Many memories require duplication of entries to facilitate rapid processing. The efficiency of storing addresses depends largely on the characteristics of the memory. In some memories address information must be repeated, while others do not record the address at all, but imply it in the physical location of the data.

Access times are usually specified on a random-access basis. Random access means that it takes equal time to locate any piece of information. An example of random access would be a telephone book, where access to any page and any name on the page takes about the same time, regardless of whether the name starts with an *A* or a *Z*. If the telephone directory were printed on a scroll, a serial-access system, the time to reach the next name would depend on which portion is unrolled. For example, if it were presently open at the names beginning with *C*, it would take much longer to find names with the initial *S* than names beginning with *D*.

The meaning of random-access has become relative.[5] A magnetic drum is not a random-access device, because it may take more than one-half a revolution, about 20 milliseconds, to reach some blocks of information. Yet, business circles consider it random-access because the 20-millisecond delay is negligible compared to their requirements.

The accepted figures of merit for a memory are access time and cost per bit of information. These figures of merit must be related to the total storage requirement, since the low cost per bit in many memories applies only if many million bits are stored.

These figures of merit do not tell the whole story. Conventional access time alone is significant only if all information is demanded in completely unordered fashion. In many applications, the work cycle calls for several accesses to data that are located close to each other. For example, in a typical inventory system, the previous balance on an item would first be looked up, this look-up would be verified, the new balance stored in the same location, and the result that has just been stored verified. At the same time, price and statistical information concerning that item may have been recorded or compared. In this case, while five to ten accesses to near-by locations were necessary, only the first access was truly random. The optimum memory minimizes the entire work cycle, not just the first access.

Two important criteria for selecting memories are delay time and processing rate, which are defined as follows:

Processing rate = maximum number of transactions per unit time.
Delay time = maximum permissible delay before an input trans-

GERHARD L. HOLLANDER formerly with the Clevite Research Center, Cleveland, Ohio, is now with The Philco Corporation, Philadelphia, Pa.

* Trade-mark of the Clevite Corporation.

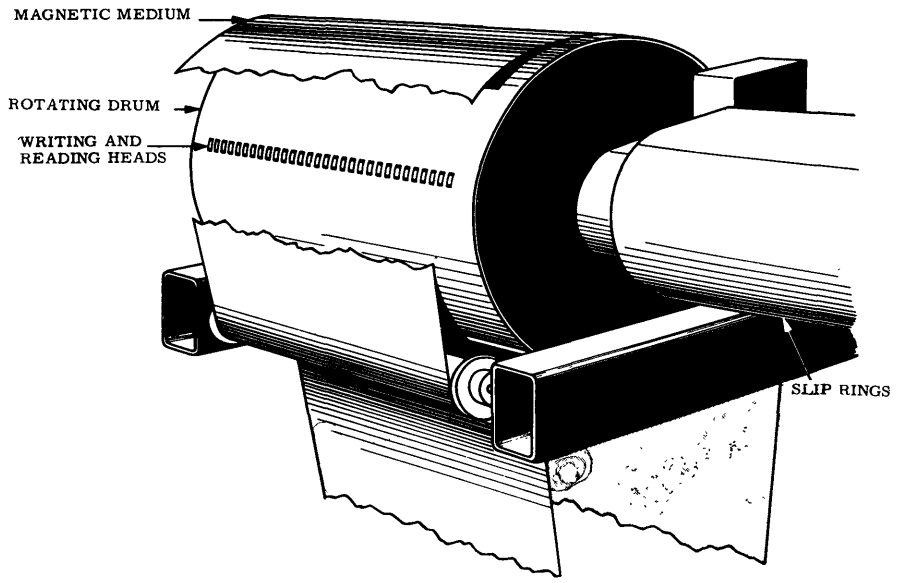


Fig. 1. TapeDRUM showing drum detail

action must be reflected in output information

$$\text{Processing Time} = (\text{processing rate})^{-1}$$

The processing rate expresses how many items must be processed per unit time. For example, a department store may have to process 240 transactions per minute, corresponding to a processing time of 0.25 second per transaction. The delay time, or pipeline time,[5] measures how soon output information has to be affected by the most recent entry. A store can tolerate a delay of several minutes before a sale is deducted from inventory, but a customer should not wait more than a few seconds before his credit balance is verified. Notice that while some applications allow much longer delay times than others (many minutes versus a few seconds) the delay time is usually longer and never shorter than the processing time (0.25 second).

The access time of a memory should not be specified to equal the processing time, since in the quasi-random approach the access time can be longer.

$$\text{Processing time} < \text{access time} < \text{delay time} \quad (1)$$

The quasi-random approach does not apply when the processing time equals the delay time. Except for this limiting case, significant savings can be effected by specifying processing time and delay time instead of the access time of the memory. For example, a 20-million bit, 100-page TapeDRUM has an average access time of about 5.5 seconds. However, this same TapeDRUM, when used as a quasi-random access memory, can have a processing time of 0.1 second with an average delay time of 45 seconds.

Comparison of Memories

The ideal computer memory would have instant access to every item and would cost nothing. However, Table I shows that the cost of memories generally increases as access times are shorter. Because of their higher cost, high-speed memories are used only where access times of microseconds are essential. Business systems requiring large amounts of data, store most of their records in the low-cost memories.

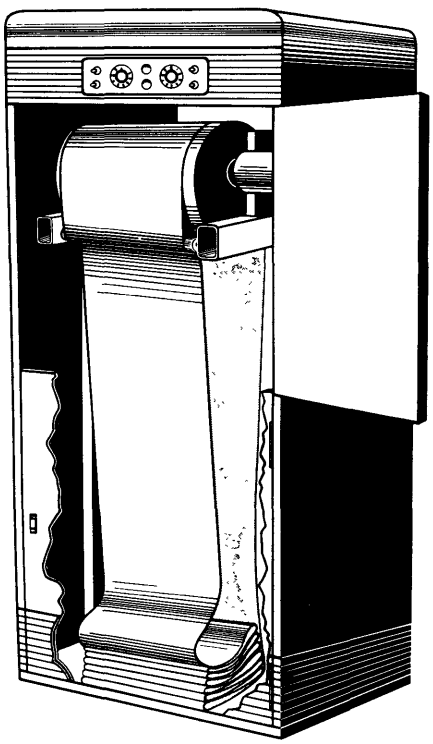


Fig. 2. TapeDRUM basket storage

Table I. Comparison of Memories

Memory Class	Typical Devices	Cost/Bit, Dollars	Access Time, Seconds
High-speed random access	ferrite cores	1.00	$\ldots 10^{-6}$
	cathode-ray tube	1.00	$\ldots 10^{-6}$
	vacuum tubes	10 00	$\ldots 10^{-6}$
Medium access	magnetic drum	0.01	$\ldots 10^{-2}$
Slow access	magnetic tape	0.0001	$\ldots 10^{2}$

Several memories have appeared on the market which combine some of the characteristics of the medium-access memories with other characteristics of the slow-access devices. A typical memory of this type is the TapeDRUM.

Characteristics of the TapeDRUM

The TapeDRUM combines the large storage capacity with fast access time at a reasonable cost. Using the same basis as Table I, the cost to store a bit of information on a TapeDRUM is on the order of \$0.0001. Following are the design specifications for the TapeDRUM:

Drum diameter	12 inches
Drum speed	1,200 rpm
Number of tracks	128
Track density	10 tracks per inch
Tape advance speed*	5 pages per second plus 0.25 second
Recorded pulse packing	100 pulses per inch
Maximum basket storage	400 pages
Approx. capacity per page	200,000 binary digits

Within any one section the access time on the TapeDRUM is equivalent to the access time of a drum. This permits the direct communication between the TapeDRUM and the arithmetic element, eliminating an intermediate random-access memory. For many business applications, the arithmetic speed just matches the drum speed, resulting in a slower and less expensive arithmetic element.[2]

The TapeDRUM may be thought of as a drum turned inside out. In a standard drum the information is stored on the circumference of the drum and stationary heads scan the data as the drum revolves. In the TapeDRUM, a piece of tape that contains the information is held stationary over the drum, while 128 magnetic heads, imbedded in the drum, rotate and scan the stationary magnetic surface (Fig. 1). The relative motion between the heads and the storage medium is retained, which is necessary

* This means that a single page advance requires 0.45 second, but that 10 pages can be advanced in 2.25 seconds.

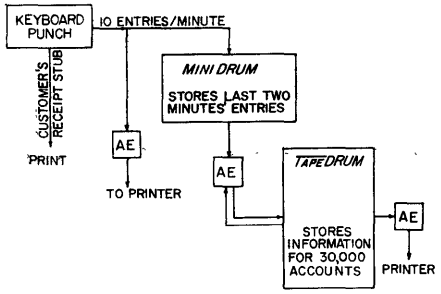


Fig. 3. Accounting system for a savings bank

to induce a voltage in conventional magnetic recording heads and to scan the entire information.

Unlike a standard drum, the storage capacity of the TapeDRUM is not limited by the available circumference of the drum. If the capacity of the drum circumference is exceeded, a new section of the tape, called a "page," can be moved into position to be scanned by the drum. As shown in Fig. 2, many pages of tape can be stored in a bin or on reels to extend the capacity of the TapeDRUM to 100 million bits of information or more.

Two interesting technical features should be pointed out. The tape actually does not touch the drum but is separated by a thin boundary layer of air. This layer makes tape wear negligible. Exact position of the tape on the drum is not critical because the reference information is recorded on the tape along with the useful data.

While the TapeDRUM stores the information on inexpensive tape, many advantages of a drum are gained:

1. *Higher relative velocity.* The scanning velocity is 10 to 25 times greater than is possible with the best tape drives.

2. *Continuous scanning within a page.* Normally, a problem requires repeated access to the same location. With a tape device the start, stop, and reversal time to return to that same location would have to be allowed for.

3. *Large amount of rapid-access storage.* A page, which can be scanned 20 times a second, contains almost 250,000 bits of information. This permits placing the directory and reference tables in the rapid-access area, so that the total storage requirements can be minimized as illustrated in later examples.

These features make the TapeDRUM particularly practical for applications involving few and noniterative computations or for straight data-processing applications where the information can be sectionalized.

The specifications show that the TapeDRUM has actually two levels of access time:

1. The access within a page.
2. The access to any page in the tape.

The maximum access time within a page is only 0.05 second, and the second access time depends on the total length of tape used.

Savings Bank Example

The quasi-random access approach can be illustrated with a simple example. A savings bank wants to maintain records on 30,000 accounts. Each account requires about 700 decimal digits of information to store the detailed deposits and withdrawals, and significant information concerning the depositor. Ten deposits or withdrawals must be entered in the memory every minute. These entries come from various tellers in random sequence.

These requirements call for a storage of 21 million decimal digits, or approximately 500 pages on the TapeDRUM. The average access time to any one of these 500 pages is about 25 seconds. Of course, this access time can be decreased by using eight TapeDRUMs so that each of them has only 60 pages. In that case, the maximum access time to any item on one TapeDRUM is less than 6 seconds. Furthermore, the probability that all entries will call for the same TapeDRUM is very small, so that somewhat longer access times than 6 seconds can be actually tolerated.

According to this calculation it appears as if eight TapeDRUMs were needed to satisfy the entry rate requirements. Actually, only a processing rate of 10 transactions per minute is needed. Fig. 3 shows how this can be done. Instead of entering all transactions directly into the TapeDRUM, an intermediate buffer drum stores the entire transaction until the TapeDRUM has moved to the proper position. The buffer storage may be a very small conventional drum.

The time T for the tape to go around, the system delay, is on the average

$$T = (\text{number of pages})/(\text{page advance rate in pages per second}) + (\text{time to stop})(\text{number of stops}) + (\text{time to enter on drum})(\text{number of entries}) \quad (2)$$

For the TapeDRUM specifications cited, then

$$T = 0.2\,(\text{number of pages}) + 0.25\,(\text{number of stops}) + 0.1\,(\text{number of entries}) \quad (3)$$

Solving equation 3 for this example yields

$$T = 100 + 4 + 2 = 106 \text{ seconds} \quad (4)$$

The required space in the buffer storage can be expressed by

$$\text{Buffer storage} = (\text{digits per entry})(\text{entries per second})(\text{time for tape to go around}) \quad (5)$$

For entries consisting of 40 characters each, the buffer must store less than 1,000 characters.

How does a quasi-random system work? Every entry is originally stored in the buffer drum. The TapeDRUM does not attempt to move randomly to the storage location of the next item. Instead, the TapeDRUM cycles from one page to the next in steps. At every page the tape determines if the buffer drum contains any items for the TapeDRUM. These items are then processed at a rate determined by the drum velocity. For the foregoing specifications a transaction can be entered every 0.1 second.

By use of this quasi-random access approach, a system that had originally required eight TapeDRUMs has now been reduced to a conventional drum and a single TapeDRUM, a considerable saving in price and complexity.

The quasi-random approach described above has certain drawbacks. If a true random-access time (delay time) of 6 seconds had been provided, the teller could have obtained an output as well as recording new information. The quasi-random access approach as described assures only that information can flow into the main store, but no information can flow back until after the main store has come to the proper location, a maximum delay time of almost 2 minutes.

Reducing the Delay Time

The quasi-random access system can be modified to reduce the delay time for some information. If the teller had to know whether the customer has sufficient funds on deposit to cover a withdrawal, the account balance must be supplied to

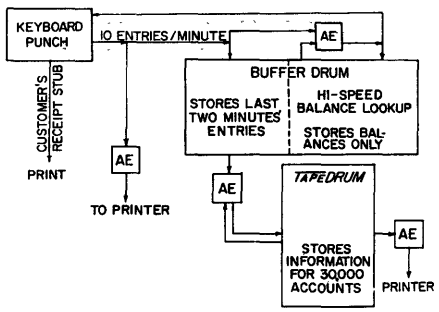


Fig. 4. Accounting system for savings bank with high-speed look-up

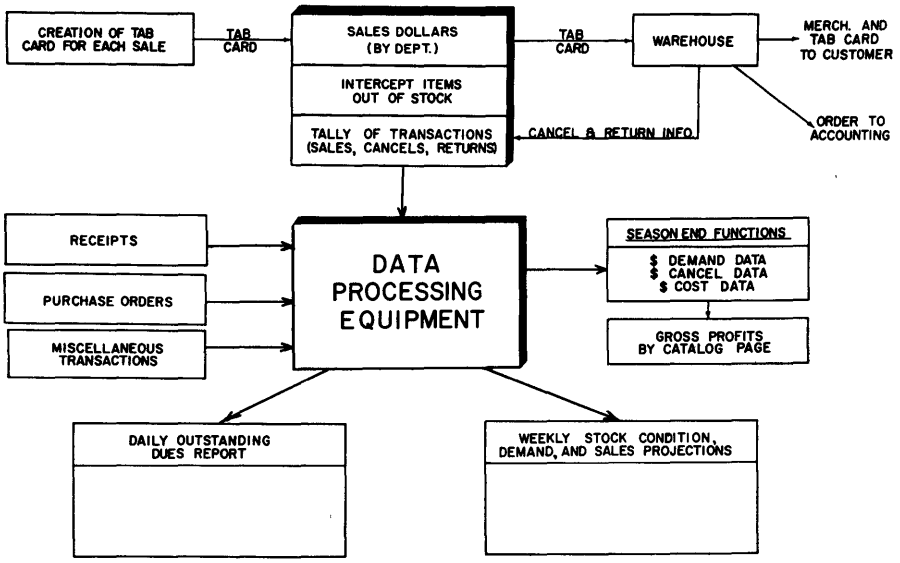


Fig. 5. Inventory control system

the teller in about 30 seconds. While the main memory stores approximately 700 digits of information to list in detail every transaction, the short delay is needed for only the balance, which may amount to 10 digits per account. Ten to 20 digits per account result in approximately 500,000 decimal digits of information, which can be stored on a standard drum.

Fig. 4 shows how this is accomplished. Since the buffer drum requires very few digits in this application, the drum containing the buffer can also store the balances. In Fig. 4 both the TapeDRUM and the balance drum must be updated by each transaction.

In the foregoing example, the quasi-random approach satisfies the requirements of the application for access time and storage capacity. The combined system still requires only two drums in place of the eight drums, had complete random access been required.

Comparison with Conventional Tape Memory

Compare this system to a conventional tape system. Only items that are actually being modified are routed through the arithmetic element. An item is updated in its original location. Thus, no operator is needed to move tape reels. Furthermore, once an item is in the main store, it stays in that location without any further electronic operation on it.

Because only approximately 20 to 30 mathematical computations per minute are performed, arithmetic elements can be very slow and therefore rather inexpensive. Furthermore, no sorting in the conventional sense of tape systems is needed to update the information.

Principles Illustrated

This savings bank example then shows that the quasi-random access approach will yield the following desirable features:

1. A single master memory with longer access time is sufficient.
2. Lower speed arithmetic elements.
3. No sorting in the conventional sense.

Inventory Control Example

Buffer storage can be used in different ways. A typical example might be the inventory control system for mail-order houses. This system is very similar to other applications which involve billing and pricing.

A mail-order house must have just enough merchandise to fill all orders received during the life of a catalog. This requires close stock control and sales prediction to avoid overstocking or cancellations. Order processing is on a tight schedule.

The basic operation is shown in Fig. 5. For every item on a customer's purchase order a tabulating card is created, which contains the item identification and price. These cards are batched in 20-minute intervals and presorted in the order in which the merchandise is stocked in the warehouse. Before an order is filled, the transaction must be tallied, and cards for items that are out of stock must be intercepted to save handling in the warehouse. Finally, an up-to-date balance of sales and cancellations for each department should be kept at all times for inquiry by the purchasing personnel. While these functions must be performed as the card is flowing through the regular process, the information obtained is combined later with other data to provide the purchasing personnel with up-to-date inventory, sales records, and statistical data from which merchandising trends can be observed. Finally, gross profit figures are available at the end of the year.

About 20,000 different items are shown in the catalog. However, due to breakdowns in sizes and colors, actually 100,000 items must be stocked. Moreover, different prices and other statistical require-

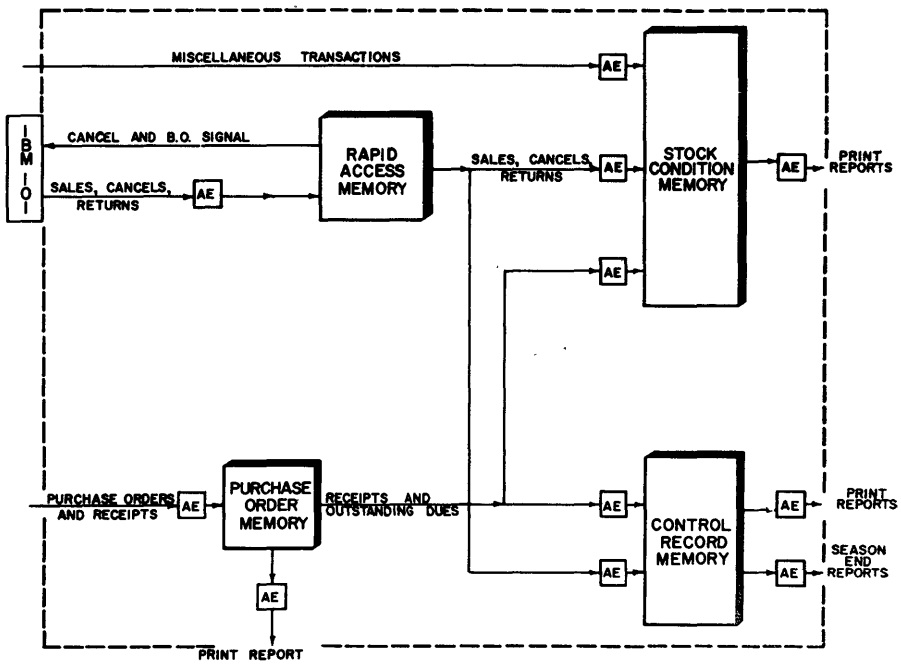


Fig. 6. Organization of inventory control system

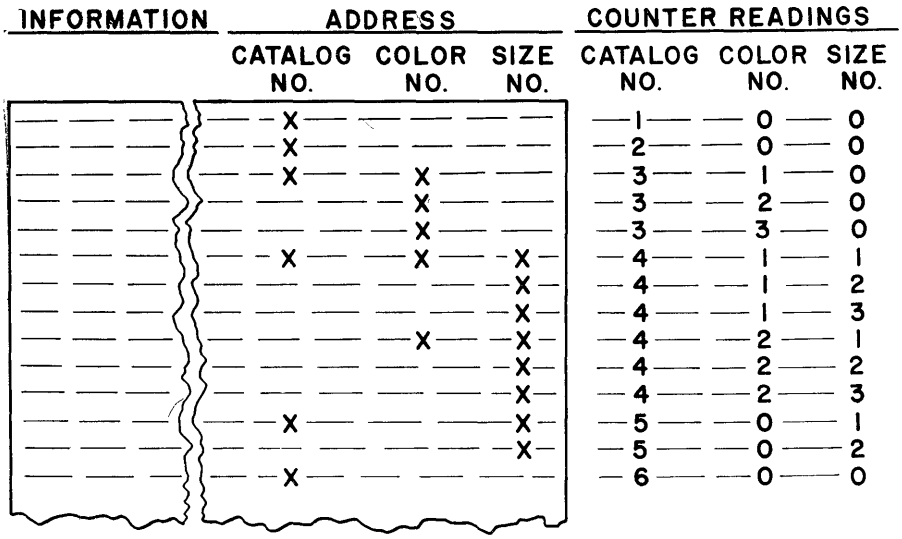


Fig. 7. Method for addressing drum

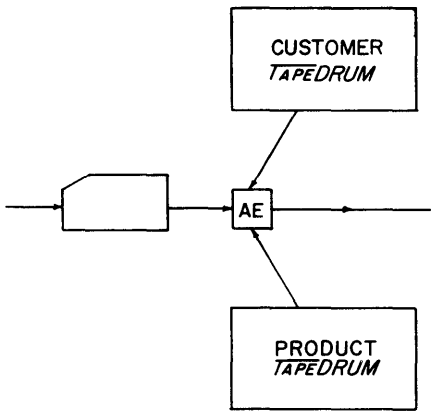


Fig. 8. Organization of billing example

ments make it necessary to keep track of the sales by about 200,000 classifications. At a peak load about 25,000 sales per hour or approximately 420 sales per minute must be tallied.

At first it appeared as if about 1,500 characters would have to be stored for each of the 200,000 classifications, or a total of 300 million decimal digits. This total has been reduced to less than 70 million decimal digits by organizing the system as shown in Fig. 6. The 1,500 digits per item were needed only for about 30,000 classifications, which are stored in the control-record memory. The stock-condition memory retains 90 digits for 100,000 different classifications. Thus, separating the information achieves a significant saving in storage. Even these smaller memories are so large that it would be difficult to enter information at the rate of seven cards per second. The rapid-access memory, a TapeDRUM, provides merely the tallying and the departmental subtotaling functions, and acts as a buffer for the rest of the system.

Since the tab cards are presorted at least by warehouse departments, page division in all memories is by department or portions of departments. Thus, the tape moves in only one direction on all memories, and the up-dating time from the rapid-access memory to the larger memories is at drum speed. Furthermore, items not requiring changes undergo no electronic processing.

Only sales, cancellations, and returns for the current week are tallied on the rapid-access memory drum. In addition, a symbol for back orders and cancellations appears when merchandise is not available. Since the TapeDRUM rotates at 20 revolutions per second, it takes only 0.1 second to look up the old balance, subtract the quantity sold, and record the new balance in the position of the old. At the same time, if a back order or cancellation signal appears, the card can be rejected immediately so that the customer can be notified. This rapid-access memory needs to store only 23x200,000, or approximately 5 million decimal characters. By the address-reduction method to be described, this requirement can be cut in half, so that only approximately $2^1/_2$ million decimal digits need to be stored. With this relatively small storage on one TapeDRUM, and because the cards had been presorted, only 30 seconds of the 20-minute batching period are used for page shifting, so that an effective entry rate of 9.5 cards per second could be maintained. Besides, all information is now presorted and can be entered easily into the master data-processing equipment without any further sorting.

The rapidly rotating drum yields another advantage for this application. To up-date the total departmental sales and cancellations it is not necessary to make another random access to a different location. Since each page contains only the items for one particular department, one location on the page summarizes the total sales for this page. Thus, if two or three pages are needed to store the rapid access data for a single department, it is merely necessary to add on demand the total sales and cancellations for two or three adjacent pages. Notice that no new original random access is needed to subtotal sales, because the large area of the drum permits rapid access to a large number of bits.

Addressing Method

On first examination it appeared as if each of the 200,000 items on the rapid-access memory would require 11 characters as address information, and 12.5 characters as other useful information. The drum-type operation of the TapeDRUM permits a large reduction of digits by an efficient method of addressing that is not possible with tapes using only a small number of tracks. It is well known that a single track on a drum can identify every item by its peripheral location. Such a method is best suited for a continuous numbering system. In this application some items were divided by color, size, or other distinctive features. This method takes care of such cases without requiring a special directory, which relates the mixed number (catalog number, color, and size), to the purely numerical location identified only as peripheral position.

An example of this new method is shown in Fig. 7. Assume that three tracks are used for address information, and the other 125 contain the useful data concerning each item. Assume further the useful information is stored on the same line as the address. Fig. 7 shows an arbitrary sequence of items some of which have no breakdown, such as catalog numbers 1, 2, and 6; others are broken down by only color or size such as items 3 and 5; while still another is broken down by both color and size, such as catalog no. 4.

A counter is connected to each of the address tracks with logical interconnection so that a pulse on a catalog-number track will reset the size and color counter. Similarly, a pulse on the color track will

Table II. Comparison of File Arrangements

Arrangement	Searching Time	Sorting Time	Unused Storage
Random	large	none	none
Block sort	smaller	none	smaller
Sorted, loose	none	small	large
Sorted, tight	none	large	none

reset the size counter. Fig. 7 shows that at all times the counters will read the proper catalog number, color, and size in response to the pulses in the three address tracks. Thus, the drum type of storage has made possible large savings in the total storage requirements.

PRINCIPLES ILLUSTRATED

1. Intermediate storage allows rapid access to selected data and eliminates further sorting.
2. The subtotals and other summary information can be entered without reference to another random location.
3. Savings in total storage requirements can be effected by an addressing efficiency possible only in storage media having drum characteristics.
4. When the final output contains only summarized information, data should be summarized as soon as possible to reduce storage requirements, even if this increases the number of distinct files.

Billing Example

An interesting application of a TapeDRUM is pricing problems where the original information is sorted in customer sequence, as well as product sequence. This application illustrates a general principle of reducing storage requirements by using several TapeDRUMs for on-line processing of records requiring look-up of mutually orthogonal data. This involves no repeated sorting as would be necessary in usual serial file operations.

An oil company has approximately 150,000 customers who are identified and classified by 22 decimal digits each. The company sells 5,000 different items at the rate of 14,000 sales per day. Sales by depots and field salesmen are punched into a tabulating card for each item on an order. The regional depots send in 14,000 cards daily. To prepare bills from these cards the proper price must be looked up, which should not take more than half of the daily schedule.

The problem here is a wide variety of prices for each item depending upon:

1. The quantity purchased.
2. The class of trade.
3. The location of the customer.
4. Special contract prices for large purchasers.

Variation of price with location occurs only for 12 out of 5,000 products. However, 75 per cent of all sales are for these 12 products.

Fig. 8 shows how this can be accomplished. The customer TapeDRUM has 72 pages and contains the information concerning the customer, as well as any special contract prices applying to his purchases. The product TapeDRUM contains only 9 pages. The slower moving items require 72 decimal digits each and can be stored on eight pages. The 12 fast movers are stored on a single page. Since prices vary from one location to another, provisions are made for 22 different price structures, each in itself broken down by quantity brackets. Thus, each item requires approximately 1,000 decimal digits, or 12,000 decimal digits for the 12 fast moving items. Since prices vary from one location to another, the customer's location is determined from the customer TapeDRUM, and the remaining 35,000 digits on the page are available as a reference table to match a given price code to a given location.

It is interesting to compute the time needed to process 14,000 cards, of which only 3,500 are for the slow movers. The cards are received from each depot in sequence by customer, so that it takes only one revolution to locate the customer on the customer TapeDRUM. The time required to look up prices for all items is as follows:

	Seconds	Minutes
14,000 cards	700	12
3,500 slow movers (9 pages+ 2 stops)	8,050	134
Total		146

Each card can be processed in one drum revolution if the page is in place. For the slow movers the TapeDRUM has to travel nine pages and make two stops, one at the proper page and one again on the page for the fast movers. This time computation is generous, but still well within the specifications. Actually the card reader may limit the speed to 100 cards per minute, which changes the computation to:

	Seconds	Minutes
11,500 fast movers		115
3,500 slow movers	8,400	140
Total		255

After processing, the cards are still in proper order by customer so that invoices can be prepared on a conventional tabulator without resorting.

PRINCIPLES ILLUSTRATED

1. The use of several TapeDRUMs avoids sorting a file by several classes.
2. By arranging the data to minimize page movement, the processing time is limited only by the drum speed, or 20 operations per second.
3. The large number of simultaneously accessible items allows rapid cross reference that reduces the total storage requirements by a large factor.

Mailing List Example

Maintenance of large and rapidly changing mailing lists is a problem that besets many business houses. Mailing lists of larger magazines contain several million names using a billion characters, with nearly 100,000 changes a day. The method described in this section can be applied to such mailing lists, or any other

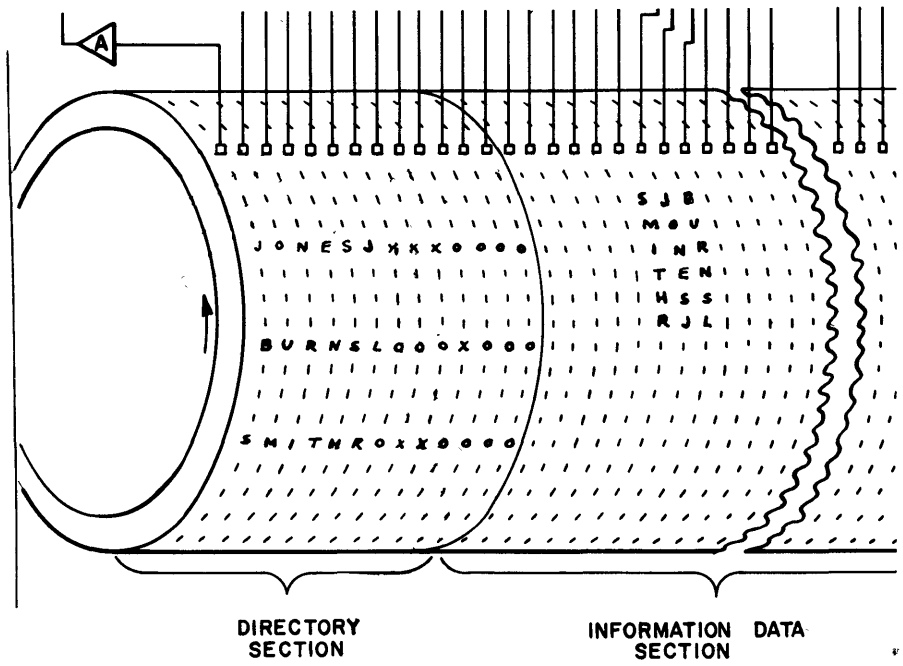


Fig. 9. Directory for mailing list

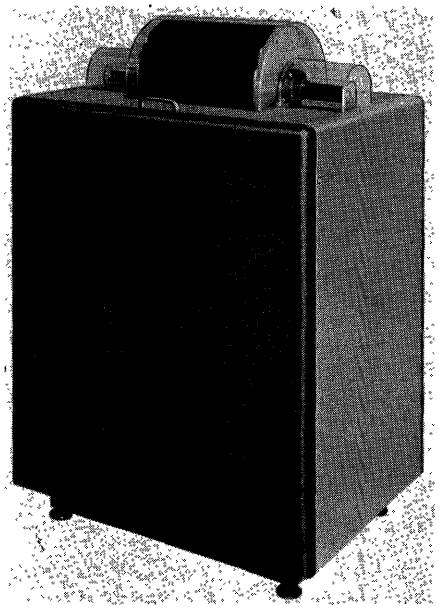


Fig. 10. Experimental TapeDRUM unit

files in which only a few of many possible items in a sequence occur at one time.

Classification of Files

To store nearly a billion characters and still have access to any one of them for the necessary changes is a major problem in the mailing list type of memory. Three factors must be minimized:

1. Required search time to find an item.
2. Required sorting time to place an item in its proper location.
3. Unused storage to allow for addition of future items in their proper place.

This paper considers "searching" to be the examination of every item to determine if it is the desired one. "Sorting" is considered to be the arranging of data into a given sequence. From these definitions the access time to a predetermined location is not considered part of the searching or sorting time. Similarly, unused storage for an increase of the total number of items in the file is not considered.

For a file like a mailing list, the arrangement of the data determines the amount of the three factors just mentioned. Characteristics of typical arrangements are summarized in Table II.

If data are randomly placed in any empty location as they arrive, the entire file has to be searched when an item must be changed. While all available storage area is used and no initial sorting is needed, the searching time is long when the information must be recovered or modified.

In a block sort, the names or other items are broken into a number of logical blocks. For example, a mailing list might be divided by the first letter of each name. There still is no initial sorting, but the storage area for each letter must be large enough to store names that may come in later. Thus, some storage area is unused, but search time is reduced considerably because only one letter has to be searched instead of the entire file.

When all items are sorted in exact sequence, searching time vanishes, since the location of the proper item is known. However, either considerable space must be left between all items to allow later additions to be filed in exactly the correct place, or the entire file must be resorted when new items are added. Thus, in the loosely sorted group much storage space is unused, while in the tightly sorted group much time is spent in resorting the information.

Addition of a Directory

The searching time on the random arrangement, or the random portion of the block-sorted arrangement, can be reduced by use of a directory. The directory stores only the identifying information and the location of the item in the main file. While the directory takes up additional space, the searching time is reduced from searching an entire file to searching a short directory.

A particularly advantageous combination of block sorting and a directory is possible with quasi-random access devices like the TapeDRUM. Each page is divided into a small directory section, and the larger information (main-file) section. Data can now be stored randomly in the information section, since after reference to the directory the location of the information is known.

Read-out equipment can be saved by placing all information concerning an entry serially into a single track; see Fig. 9. Thus, only a single amplifier is needed for all information tracks. This amplifier can be switched after the proper track number has been found in the directory.

The size of the directory can be reduced by relating the space co-ordinates of the directory item to a track number. Thus, an item appearing on the first line of the directory could be associated with the first portion of the first information track. Similarly, the 21st item might be associated with the first portion of the second information track. The directory's size can be reduced still further by advanced coding methods, which eliminate some redundancy common in the English language. In a typical directory of this sort, 5 to 10 per cent of the page capacity is used for directory; the remainder, for useful information.

Operation of This System

A typical subscription list might illustrate how this system works. The information section of each page, Fig. 9, contains the name, address, and pertinent subscription and billing data for each subscriber, which might take 300 alphanumeric characters per entry. The pages are arranged by city and state, so that all customers in the same post office are

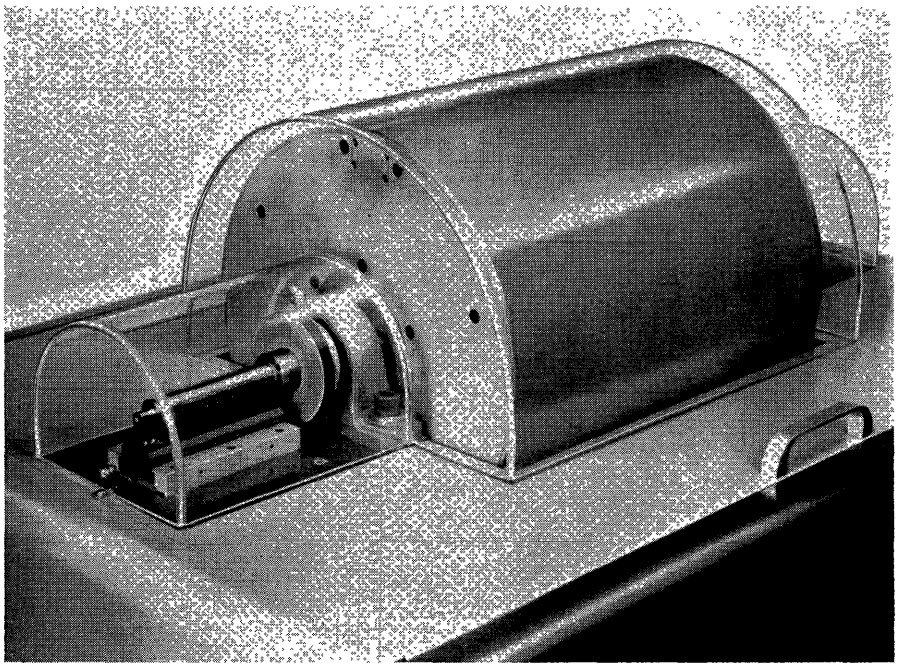


Fig. 11. Close-up of experimental TapeDRUM

located on the same page. Exceptionally large post offices might occupy several pages while several small ones would share a single page.

To enter a subscription extension or address change, the proper page is determined by direct examination of the city and state. Once that page is reached, usually after storage in a buffer, the name is compared with all names in the directory section during one revolution of the drum to find the track number. On the next revolution of the drum, the detailed entry is up-dated in the information section on the same page.

This example is somewhat oversimplified. Additional data, such as house numbers, may be stored in the directory section to uniquely identify a subscriber. On the other hand, the name itself can be compressed. Furthermore, if one page contains subscribers for only a few post offices, the name of that post office need not be repeated for each entry, but can be stored separately on that page. A code symbol in each subscriber record selects the proper post office or other common information.

PRINCIPLES ILLUSTRATED

1. The page arrangement is particularly adaptable for the rather efficient block sort.

2. The large number of characters simultaneously accessible allow the use of the efficient directory method for the location of random items within the block.

Conclusions

To select an economical memory for business data-processing applications, the characteristics of the memory must be matched to these system criteria: work cycle, processing rate, and delay time. The memory is often overspecified, if its access time is specified as the reciprocal of the system processing rate. If longer delay times (as defined on p. 128) can be tolerated, quasi-random access systems can handle the task with slower and less expensive memories.

The TapeDRUM and similar memory devices represent a compromise between low cost and short access time. Systems planned to take advantage of their features often result in the most economical solution for a business data-processing task. Despite their low memory cost, on the order of serial memories, the quasi-random access systems described feature:

1. Processing rates of many items per second.

2. Delay times measured in seconds or minutes.

3. Minimum, if any, sorting.

4. Saving in total storage requirements by efficient addressing methods, and rapid cross references.

5. A drum scanning rate easily matched to inexpensive arithmetic elements.

While much progress has been made in the development of the TapeDRUM since its initial announcement,[1] this paper is limited to system studies. The examples are based on the design specifications of the experimental prototypes shown in Figs. 10 and 11.

References

1. MAGNETIC MEMORY DEVICE FOR BUSINESS MACHINES, **S. J. Begun.** *Electrical Engineering*, vol. 74, June 1955, pp. 466–68.

2. DATA PROCESSING WITH A QUASI-RANDOM-ACCESS MEMORY, **Gerhard L. Hollander.** *Instruments and Automation*, Pittsburgh, Pa., vol. 29, Apr. 1956, pp. 690–94.

3. ELECTRONIC DATA-PROCESSING IN INDUSTRY (book), "Automatic Date-Processing Equipment: A Survey," **Charles W. Adams.** American Management Association, New York, N. Y., 1955, pp. 125–39.

4. EVALUATION OF SORTING METHODS, **J. C. Hosken.** *Proceedings*, Eastern Joint Computer Conference (Institute of Radio Engineers, New York, N. Y., 1955, pp. 39–55.

5. THE MANUAL USE OF AUTOMATIC RECORDS, **A. G. Oettinger.** *Ibid.*, 1955, pp. 33–38.

Discussion

Chairman Howard: We have similar questions on slip rings from T. D. Best (Burroughs Corporation), A. E. Olson (National Cash Register Co.), and Dave Silverman (Helipot Corporation). The question is: In transferring information from the heads to the amplifiers, are slip rings used and, if so, is there not a noise problem associated with the slip rings?

Mr. Hollander: Figs. 1 and 11 show that the signals are transferred from the heads to the amplifier via slip rings. The noise problems associated with these slip rings are interesting.

On first examination, we would note that the playback signal of the head is measured in millivolts, while the noise of slip rings is generally specified in microvolts. However, remember that the slip-ring noise specification is an rms voltage. Occasional spikes of many volts might contribute only a fraction of a microvolt to the average or rms value of noise. Still, when such a noise pulse equals or exceeds the value of the minimum playback signal from the head, which determines the threshold value of the amplifier, the equipment will make an error. If such errors occur very rarely, they can either be neglected, or in critical applications they can be detected or corrected with redundant codes.

The slip-ring problem has received much attention during our research and development work. Many materials were tried and discarded. Finally, we found a combination for which preliminary tests at Clevite Research Center indicate that the error rate and life expectancy are satisfactory.

Further product design of the TapeDRUM is the responsibility of the Brush Electronics Company, Division of Clevite Corporation. For this reason, this paper concerns itself more with system design than with the product characteristics of the TapeDRUM.

R. Townsend (British Tabulating Machine Company, Ltd.): How do you handle the synchronization problem between the MINIDRUM and TapeDRUM?

Mr. Hollander: In the savings bank example, the MINIDRUM rotates several times faster than the TapeDRUM, so that information can be transferred several times for each TapeDRUM revolution. Since the MINIDRUM is much smaller, the surface velocities and the pulse rates of the two units are nominally equivalent. The information is transferred via some small static memory, such as core storage.

In many actual business applications no separate buffer is needed. As shown in the savings bank example, the old balance must be transferred to an arithmetic element where the withdrawal is subtracted from it. Thus, the arithmetic element itself serves as the statisizer. While a static buffer is necessary between the MINIDRUM and the TapeDRUM, usually the arithmetic element will handle this function.

W. W. Sturdy (U. S. Army): How is friction between the drum and the tape avoided?

Mr. Hollander: Nature graciously supplies a boundary layer of air which floats the tape away from the drum. By applying tension to the tape when it is stopped, the boundary layer is held to about 0.0002 inch.

A. I. Dumey: At 10 pages per second, are you moving the tape at 160 inches per second? Can you read and write simultaneously?

Mr. Hollander: When the tape is advanced, it moves at very high speed. Depending on the model, tape speeds of 120 to 400 inches per second have been specified. It must be remembered that for the systems that we have designed, the tape is read only when it is stopped. Thus, flutter, skew, and other problems during this fast tape motion can be neglected.

Simultaneous reading and writing is limited only by cross-talk between adjacent heads and in the cabling. On our experimental models, we could not read a head while the immediately adjacent head received record pulses. The effects of such crosstalk could be eliminated by a more sophisticated playback signal amplifier, but for the systems that we have designed it was not necessary to complicate our equipment.

A Large-Capacity Drum-File Memory System

H. F. WELSH V. J. PORTER

Synopsis: The magnetic drum-file memory system described in this paper was designed for the Univac-Larc computing system as storage that would be intermediate in speed and in capacity between the Uniservo magnetic tapes and the ultra high-speed magnetic-core memory. Although designed for Univac-Larc, the drum-file memory system may be used for any type of systematic data processing where extremely short access time is not required and economy is an important consideration. Economy is achieved through the use of a single flying head, which can move parallel to the axis of the drum and perform the read-write operations for the entire drum. This arrangement eliminates the need for close mechanical tolerances and elaborate switching devices. The drum-file memory may also be used as a random-access device where a delay of a second or two is not critical, as, for example, in checking a particular item of an inventory.

Univac-Larc System

THE Univac-Larc, for which the drum-file memory was designed, is an ultra high-speed scientific computer designed to solve problems of great complexity. To operate at peak efficiency, it must accept data at a rate of 360,000 decimal digits per second, and it must have storage available for intermediate results. The Uniservo tapes which serve Univac as a secondary memory are not nearly fast enough to keep up with Univac-Larc. In the latter system, the Uniservos are to be used solely as input-output devices and another device had to be designed that would be intermediate in speed and in capacity between the tapes and the internal memory shared by the central computer and the input-output processor. The result was the magnetic drum-memory system described here, which is 50 times faster than Uniservo I and has a capacity of 250,000 12-digit words per drum.

Head Design

The major objective in designing the drum-memory for Univac-Larc was to get as much information on the drum as practical at a reasonable cost. In the interests of economy, it was important to minimize machining and temperature-control problems and to avoid the use of complicated switching devices. In the interests of achieving high-information density, it was necessary for the heads to ride as close as possible to the drum, since the maximum usable pulse density of a recorded signal decreases with any increase in the distance between the head and the recording surface. Contact between head and drum would not be feasible, of course, at the surface velocity involved—1,000 inches per second.

In view of the fact that the data on the drum were to be processed systematically, a single flying head assembly that would read or write all of the tracks on the drum sequentially would meet the requirements for simplicity, economy, and close spacing with the drum.

A head that moves the length of the drum eliminates the need for multiple heads and complicated switching mechanisms. Use of the flying head assembly enables the head units to run much closer to the drum than would be possible for a fixed head and, further, makes it possible to use a large drum without holding the tight tolerances that would be costly to maintain for so large an area. (The drum is approximately 24 inches in diameter by 24 inches in length.) Compressed air might have been used to support the head, but the flying head eliminates not only the need for a compressed-air system but also the possibility of the introduction of foreign matter by such a system. Cleanliness is of the utmost importance, of course, in the operation of a mechanism like the magnetic-drum memory.

The head design is based on the Kingsbury oil-supported bearing principle. (In this application, air is used instead of oil for support.) The center of pressure on the head is nearer to the trailing than to the leading edge of the head; see Fig. 1. The wedge of air under the leading edge is drawn along by the surface friction of the rapidly rotating drum, and the trailing edge is maintained in equilibrium at about 1/10 mil from the drum surface. Self-alignment of the head with the drum is provided by gimbals, which enable the head to move radially with respect to the axis of the drum and to rotate about two axes parallel to the surface of the drum. Since the head weighs only 1 gram and supports a spring load of 6 ounces, the gimbals enable it to react with considerable sensitivity to any irregularities in the surface of the drum.

Six read-write head units are located close to the trailing edge of the head assembly so as to ride about 1/2 mil from the surface of the drum. An erase head is located somewhat forward of the read-write heads.

Organization of Drums

The drum has 100 circumferential bands, each capable of storing 2,500 computer words. The bands are divided evenly into 25 sectors of 100 words each, making it possible to start reading or writing at any one of 25 access points around the circumference of the drum. This arrangement reduces the time lost in beginning to read or write on a new band to 1/2 a sector, and in random application reduces the amount of information that must be read or written to 1/25 of a drum revolution.

The words and the digits of the words are stored serially, while the bits are stored in parallel on the six tracks that compose a band. There are four information bits in a digit, plus check and sprocket bits. The head assembly has six read-write head units.

In addition to the 100 information bands there are two single tracks with a flying head assembly at one end of the drum. One of these tracks is a master sprocket track which generates uniformly spaced sprocket pulses to control the writing frequency; the other is a time-selection track used to address the sectors.

One of the ways in which the high information density of the drum is achieved is by the physical arrangement of the tracks. The tracks of one band are interlaced with the tracks of another so that the head units in the head assembly can be spaced to read alternate tracks. When the head assembly has recorded on one band, it shifts one track over to the second band and then 11 tracks over to the third band. This arrangement makes a density of 29 tracks to the inch practical, cuts down on crosstalk, and makes the head assembly easier to manufacture.

Physical Description of Drums

The drum consists of a thin-walled, extruded, seamless brass tube shrunk over

H. F. WELSH and V. J. PORTER are with the Remington Rand Univac Division of Sperry Rand Corporation, Philadelphia, Pa.

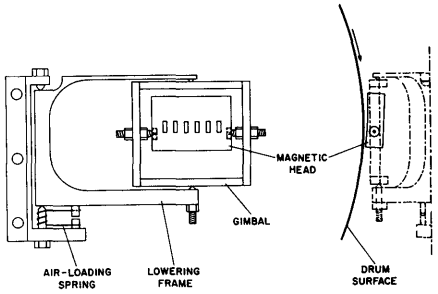


Fig. 1. Head assembly

a supporting tube of cast magnesium alloy. The function of the cast tube is to support the outer tube while the surface is being machined and ground, and to maintain the shape of the drum in service. After the drum surface has been finished, it is electroplated with a nickel-cobalt alloy by a process similar to the one used to plate the magnetic tapes for the Univac system.

The drum is 24 inches in diameter and 24 inches long. It is driven at 860 revolutions per minute to attain a surface velocity of over 1,000 inches per second. A phase-modulated system of recording is used in which the read-back signal is sampled to detect the polarity of the signal.

Band Selection

The head assembly is moved from one band to another across the drum by a band-selector mechanism designed to provide rapid, accurate, and positive positioning of the head. Three independently controlled mechanisms are involved in selecting a band; see Fig. 2. The interlace mechanism moves the head assembly 0.035 inch from one band to the second band with which the first is interlaced. A second mechanism, the stepping mechanism, moves the head assembly 0.420 inch from one band of an interlaced pair to the equivalent band in the adjacent pair. (It is also possible to step the head assembly 12 tracks forward and at the same time move it back one track, so it will read the first instead of the second band of the next pair.) A third mechanism reverses the direction of stepping.

The head assembly is mounted on a lightweight carriage which rides on rollers along a pair of guide rods parallel to the axis of the drum, as in Fig. 3. The stepping mechanism moves the carriage along the guide rods. Pairs of miniature ball bearings are mounted along opposite sides of a shaft. A bearing engages a cam surface on the carriage. Every time the shaft is rotated 180 degrees, a new bearing engages the cam surface and moves the carriage a distance of 0.420 inch, or the equivalent of one step. A cable connects the carriage to a tension spring which preloads the cam surface against the bearing.

The ball bearing and cam arrangement ensures accurate repositioning of the carriage, even if the angular positioning of the shaft is slightly inaccurate, because the ball bearings are in the dwell area of the cam when the carriage stops. Since only rolling action is involved, there will be less wear than one would expect from a mechanism like a lead screw.

The carriage drive shaft is operated through a Geneva mechanism and a set of reversing gears from an actuator-controlled wrap-spring clutch. The clutch consists of a helical spring which couples the input shaft of the mechanism to a constantly driven shaft. Normally the spring is held distended and disengaged by an actuator-controlled stop. When the actuator is energized, the stop releases the spring, allowing it to contract and couple the two shafts. After 1/3 of a revolution, the spring is distended once again by the stop and the two shafts disengage. A three-position detent cam accurately positions the drive shaft every 1/3 revolution.

From the clutch, the rotation is transmitted to a 5-to-3 ratio Geneva mechanism. The Geneva has the characteristic of producing a dwell period at the beginning of each cycle, after which it produces a slow starting movement which gradually accelerates and then slows down before reaching the stopping point. The Geneva prevents the full inertia of the drive shaft from being applied to the clutch until the clutch is fully engaged.

The output of the Geneva rotates the carriage drive shaft at a 2-to-5 ratio through one of two spur gear trains, one of which contains an idler. The selection of one gear train or the other determines the direction of stepping. A key on the carriage drive shaft, when actuated by a solenoid, couples the shaft to one gear train and at the same time uncouples it from the other. The bearings which

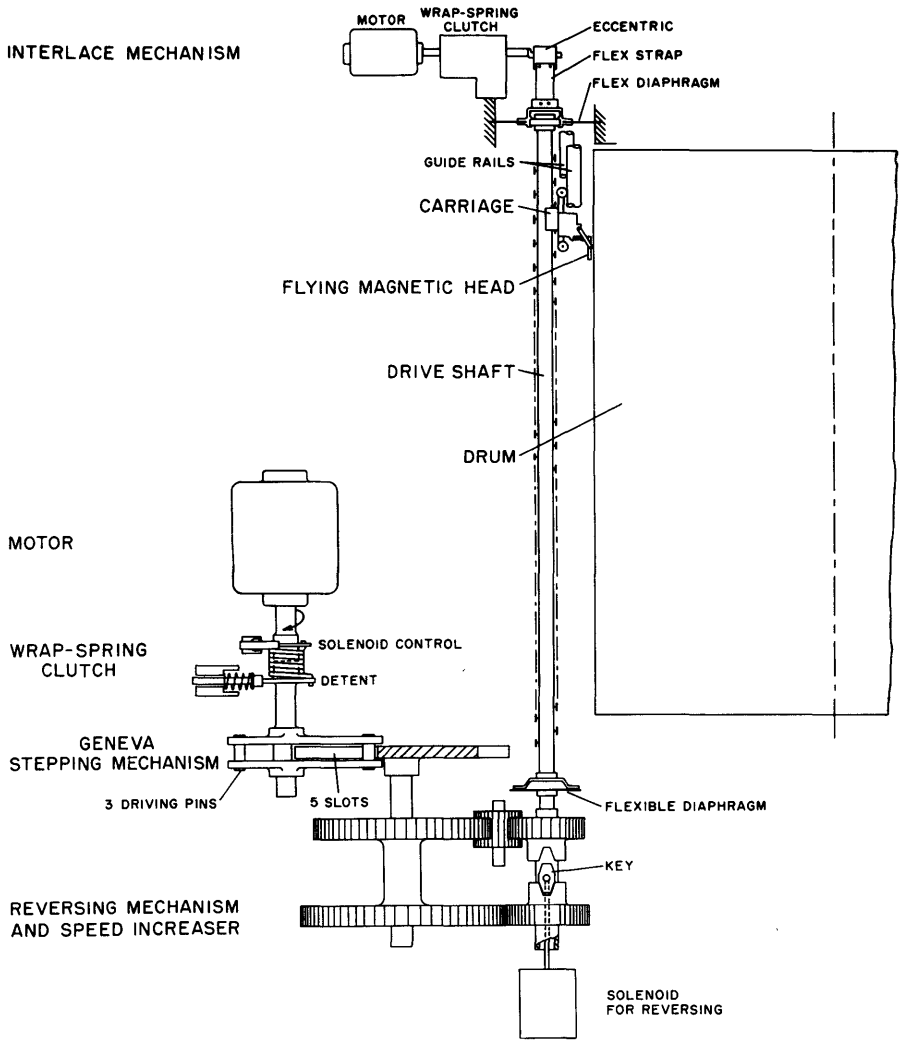


Fig. 2. Band-selection mechanisms

support the carriage drive shaft are supported on flexible diaphragms or spiders which allow axial travel of the shaft. The interlace movement is produced by shifting the carriage drive shaft axially a distance of 0.035 inch. Since the position of the cam bearings on the drive shaft determines the position of the head-assembly carriage, the carriage will also be shifted 0.035 inch. This movement is produced by the rotation of an eccentric which engages the end of the carriage drive shaft. The eccentric is rotated by an actuator-controlled two-position wrap-spring clutch similar to the one in the stepping mechanism.

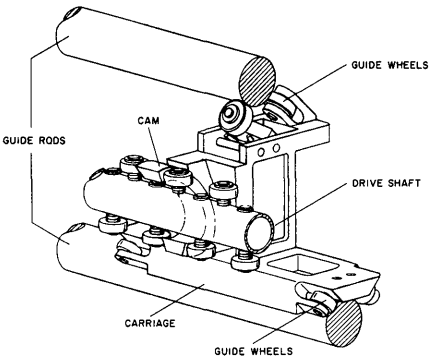


Fig. 3. Carriage assembly

Access Time

Moving the head assembly from one band to the band interlaced with it takes about 50 milliseconds. Moving the head assembly a full step to an adjacent pair of bands takes approximately 70 milliseconds, except when the head assembly is continuously stepped without reading or writing, in which case about 50 milliseconds are required for each step after the first. Because the stepping and interlace mechanisms are independently controlled, both movements can be performed simultaneously.

From 100 to 125 milliseconds are required to set the reversing mechanism that changes the direction of stepping. Since the mechanism operates independently, it is possible to overlap the time of this setting with reading, writing, or interlace-movement time.

Maximum access time from either end of the drum to any band location is 2.6 seconds. If a complete band of 2,500 words is to be written or read, the reading or writing can begin as soon as the next space between sectors has been traversed. Therefore, one sector interval may have to elapse before access to a complete band is obtained. If a specific sector on a band is to be addressed, as much as a full drum revolution may be required to reach it. However, any number of the sectors on a band can be read or written during one drum revolution plus one sector traverse.

Head-assembly movements are possible in less than one drum revolution. By interlacing the operation of two drums, sequentially, a continuous read rate of 2,500 words every 83 milliseconds can be achieved. This is equivalent to the data-transfer rate of 360,000 decimal digits per second, required by the Univac-Larc. For reading and writing at 360,000 decimal digits per second, four drums are required. The first Univac-Larc will have 12 drums, all of which are capable of simultaneous head-positioning operations. Reading and writing can be accomplished in parallel with the computing process.

Business Applications

The Univac-Larc drum memory is not a true random-access device, since it is necessary to step through all intervening head positions when moving from one head position to another. Neither is it a purely sequential device in that it is not necessary to read every band when moving from one band to another. Since it is possible to go from any one place on the Larc drum to any other place at random, the drum can be considered to be a random-access storage unit with a maximum random-access time of 2.6 seconds and an average random-access time of 1 second.

As such, it is obviously adaptable to a number of commercial uses, such as inventory control or airline reservations systems, where 1 or 2 seconds of delay is not critical. Two drums could be mounted in a single cabinet to provide a total capacity of 4,000,000 alphanumeric characters.

The information rate resulting from the fact that the Univac-Larc drum reads the four information tracks on a band simultaneously is much higher than would be required for most commercial applications. Therefore a commercial drum memory need provide a read-write amplifier for only one head unit. The single amplifier could be switched electronically from one head unit to another. The bits of an alphanumeric character could be recorded serially on a single track to provide a character rate of 50 kilocycles per second.

The system would be particularly adaptable to applications in which random interrogation of a file is required during sequential processing, since random interrogation can be made by interrupting routine processing for a maximum of 5.2 seconds, 2.6 seconds to make the interrogation, and another 2.6 seconds to return to the point at which the routine processing was interrupted.

It is evident, then, that although the large-capacity drum-file memory system described in this paper was designed for use in the Univac-Larc Computing system, it has many other possible applications.

Discussion

W. A. Farrand (Autonetics Division of N.A.A.): What prevents Kingsbury pad scraping when the drum starts up?

Mr. Welsh: The head is lifted away from the surface of the drum whenever the drum speed is not adequate. When the drum is started, it is brought to speed first, then the head is lowered onto the surface of the drum. This is called landing the head. It is a little like but opposite from flying an airplane, where one starts down on the ground and has to get up into the air. Here one starts away up in the air and has to bring this head down into flying position on the surface, very close to the surface. There is also a centrifugal switch on the shaft of the drum so that if, for any reason, the drum should slow down, the head will automatically be raised.

L. Jones (Westinghouse Electric Corporation): What is the number of bits per inch along each track?

Mr. Welsh: The system just described is based on 400 bits per inch.

J. J. Selfridge (International Business Machines Corporation): It was mentioned that an erase head is just forward of the read-write head. Is erasing performed prior to writing? What is the signal strength at the head?

Mr. Welsh: The signal strength at the head is of the order of 10 millivolts. Erasing is performed while writing, so that no extra time is required on the machine for this operation.

N. Dean (Ramo-Woolridge): Is it necessary to write a whole sector, or is it possible to write individual digits? What type of magnetic recording is used?

Mr. Welsh: Yes, it is necessary to write the whole sector, because of the type of

recording, which is called phase modulation. Other people have different names for it. It is such that you have to write a whole sector. That is one of the reasons for dividing the circumference of the drum up into sectors. However, this is really no disadvantage, because what is normally done, when one wishes to modify a sector, is to read this sector into the high-speed core storage, modify the information there, and then rewrite the whole sector on another drum revolution.

W. S. MacDonald (Comtronics Corporation): What is the error in positioning of heads in the direction of drum rotation due to dirt on head ways?

Mr. Welsh: This would depend upon the thickness of the particular piece of dirt that would be on the ways. Elaborate precautions are being made against that, not only because of dirt on the ways, but because dirt on the surface of the drum when the head is only flying a fraction of a thousandths of an inch away, would cause difficulty. The entire drum will be in a closely sealed container containing a precipitron to remove any dust from that container and from the air in the container.

The RAMAC Data-Processing Machine: System Organization of the IBM 305

M. L. LESSER J. W. HAANSTRA

Synopsis: A new automatic data-processing machine for business applications, utilizing a random-access memory system, is described. Unlike the usual batch method of machine-processing business transactions, the technique used permits transfer of information between any two points in the system and makes multi-choice decisions according to the current status of the information. This in-line operational concept is discussed in detail and the data transfer routes and processing controls are shown. Employing punched card input and printed-record output, the IBM (International Business Machines Corporation) 305 accounting machine is designed to handle 10,000 line-transactions per day.

IN CONTRAST TO the batch-type operations of conventional automatic data-processing machines, the new IBM 305 Random-Access Memory Accounting Machine (RAMAC) is designed to process business transactions as they occur. The sequential-access, large-memory systems ordinarily used up to this time in automatic accounting machines have usually necessitated a waiting period for accumulation of a batch of data to process.

The advent of the Type 350 Magnetic-Disk Random-Access File has permitted the design of a machine system for in-line processing of business transactions as they occur. The IBM 305 was thus designed specifically for in-line applications, thereby permitting data processing to be on a current basis at all times

The first part of this paper discusses the systems study of this in-line concept in business applications leading to the design of the IBM 305. In particular, it was found that arithmetic power, per se, was very much secondary to the ability to manipulate variable field lengths of alpha-numeric data in a direct fashion, and to make direct multi-choice decisions based on the current status of the information being transferred. It was also considered necessary that the programming technique be as straightforward as possible, to eliminate the necessity for a high degree of special training on the part of potential users.

The resulting system employs stored-program control only for information transfer, including arithmetic. Each instruction is self-contained and transfers a field of information from any place in the system to any other, on a fully variable-length basis. All logical decision is based on control-panel logic, where selectors indicating the status of the information processing to date may be interrogated in any sequence at any desired time. For example, the sign status (positive, negative or zero) of each or any of the ten accumulators may be used directly for making multi-choice decisions.

The In-Line Processing Concept

Historically, the processing of business data originated as an in-line operation. We might assume that with the earliest direct barter systems, data processing began and ended when the bartered material changed hands. Thus, the operation was not only in-line, but was also immediate.

As more formalized business-record systems come into being, data processing lost some of its immediacy but still remained more or less an in-line affair. In general, transactions were posted to their final record forms in the sequence that they occurred, preferably with no intermediate posting operations, and most certainly without awaiting the accumulation of sufficient similar transactions in order to make an economical run of data. In modern machine accounting terminology, there was no sorting or collating except by distribution directly to the appropriate ledgers.

With the steady increase in volume, the manual in-line process could not keep up with the demands for relativity current data in an easily digestible form. The solution to this problem has been the mechanization of business data processing by various devices and in various degrees. Inherent in most mechanization schemes of any magnitude, to date, has been the batch concept. According to the traditions of mass-production technology, the process of mechanization was approached by the route of many simple repetitive operations. An array of single-purpose machines was built and the information passed through them in turn. A little more of the job was done with each machine pass, until the final report could be assembled from all the individual subassemblies which had been fashioned on the machines. The time necessary to accumulate a batch was accepted as a small loss in view of the large time savings available by the mechanization of data processing. Some continue to accept this as a "way of life," even in the face of evidence to the effect that the batch accumulation time is now growing longer than the process time in some applications not inherently adaptable to batching. Faster and more costly devices are now being built in an attempt to salvage a sense of immediacy from data that grew cold even before they were presented to the machine. This is done by building multipurpose electronic machines that carry out all the operations formerly handled by the battery of single-purpose machines. Although all this is done within a single set of cabinets and with no manual intervention between opera-

M. L. LESSER and J. W. HAANSTRA are with the International Business Machines Corporation, San Jose, Calif.

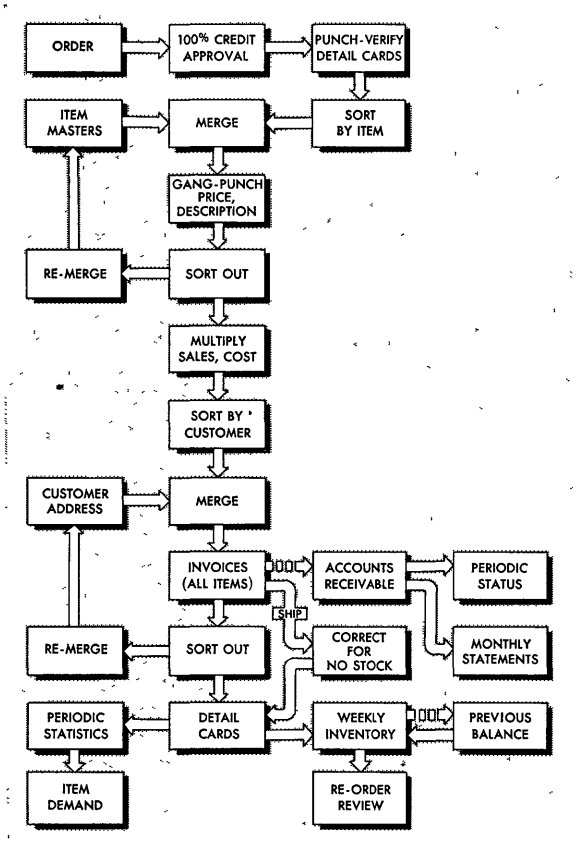


Fig. 1. Typical flow chart for a job handled with conventional punched-card equipment

tions, nothing has really been done to eliminate the necessity for batching.

The requirement for batching is not inherent in any simple operation ability of our machinery. Modern machines are quite capable of continuing long and reasonably involved process chains with a small collection of input data. However, the large memory system still restricts us to a batch operation, by its serial nature. Business data processing, in general, is a file-maintenance operation. A little new input information is combined with a lot of information already in the system to obtain a small amount of new action information as output. While this is done, the status file is modified to show the effect of the change. If an item in the status file can be found only by reading through the file from the beginning, a little useful work can be done at the same time by putting all requests for file information into the sequence in which the information will be encountered. If the next file needed in the process is in a different sequence, data is resorted to this new sequence before processing against this new file.

The statements made in the preceding paragraph hold for any system of data filing that can be economically reached only in a sequential fashion—be it punched cards or magnetic tape. The difference is one of physical handling, volume, and speed, but not one of philosophy. The point might be illustrated with Fig. 1. Shown here is a typical flow chart for a job handled with conventional punched-card equipment. The job is one of billing and invoicing, with the maintenance of a perpetual inventory, and is the source operation for data going to accounts receivable and sales statistics analysis operations. The number of files to be consulted is small. Only the inventory file is maintained by the system in any way other than to replace the information removed from it. The "sorts," "collates," and "card moving" stages are all shown. If the flow chart is translated to tape terms, the remaining sorts and collates are still necessary. Most of the decisions required are not shown, and will be discussed later.

However, if the restriction that file information is available only in a fixed, predetermined serial order is removed, the batching requirement is eliminated. If there is random access, with equal facility, to any place in the memory, it is possible to pick out directly the necessary items from each of the reference files in the sequence established by the order in which the input data is received and the secondary order established by the transaction. In theory, a machine can be built to take an input transaction record and carry it all the way to final output document, distributing by-product information to the proper files en route, with no regard as to whether or not the next input refers to the same type of transaction. This is mechanized in-line data processing. It can just as well be run as the transactions occur because the unit machine process time per transaction is independent of the number of transactions of a given type that are run together. The flow chart would then look like Fig. 2. With this ability, batch processing techniques can be reserved for those applications, such as statistical analysis, that have an inherent batching requirement. The simplification introduced by random storage is thus illustrated by this new flow chart.

Machine System Requirements for In-Line Processing

In this part of this paper will be discussed the system requirements established for the complete data-processing machine, IBM Type 305, designed specifically to make use of the disk file. The detailed characteristics of the machine will then be described. Only the over-all aspects of the system will be considered at first, as indicated in the block diagram shown in Fig. 3, with emphasis on the desired characteristics of the unit marked "process" in that diagram. Physically, this is a small magnetic drum carrying multiple tracks, each capable of storing a single 100-character record, and surrounded by a control system. We will neglect the input-output system, and the file itself, except for pointing out that they are connected to the process unit by information channels and are so buffered to the process unit that all mechanical time delays may be overlapped by process operations.

Briefly, the original requirements for the machine as designed were as follows:

1. An in-line accounting machine that would handle, from card input to printed-record output, 10,000 line-transactions per day. This implies posting the basic data for each transaction to the record or records involved, thereby maintaining all pertinent files on a current basis as a direct adjunct to transaction processing, and also making all those routine decisions that could be relegated to an automatic machine. The intention is to approach "management by exception," where only those decisions essentially requiring manual handling are brought to the attention of the operators.

2. During the processing of these transactions, the system was to allow manual inquiry as to the status of any record in the disk file at any time, producing a printed output independent of the primary output from the machine.

3. The whole machine system was to be made available at a cost that would be considered reasonable to a user for whom

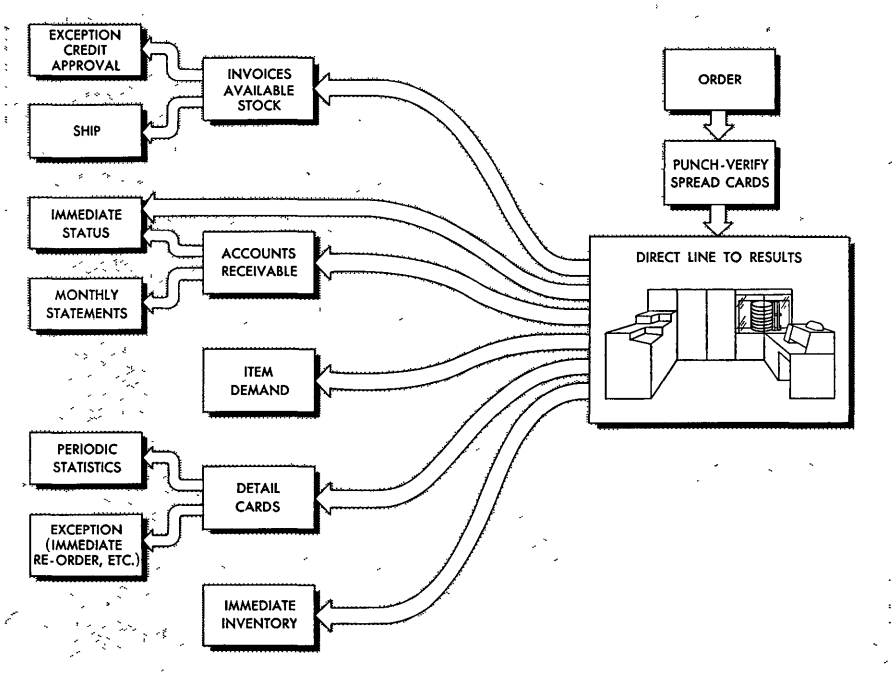


Fig. 2. Flow chart

10,000 transactions was a very large day's business.

A secondary requirement that was observed throughout the system design was that the operating procedure of the machine should be as straightforward as possible. The form of instruction chosen should be as suited to the task as possible; there should be a minimum of programming restrictions chargeable to the machine, as opposed to those chargeable to the application; and the operating procedure, in general, should be easily understood by persons already familiar with conventional punched-card techniques.

In the design of a machine system, practically the entire arrangement centers around the method chosen for control. In general, previous flexible machine systems were based on one of two techniques: a fully stored program, or a fully wired, control panel, program. For the IBM 305, our approach to the control problem was based on a study of the operations the machine would be required to perform. When a conclusion was reached as to the form desired (an optimum combination of the two techniques), the general organization requirements of the machine followed directly.

In an accounting operation sequence, such as shown in Fig. 1, the majority of operations are of the reproduction type, consisting of straight information transfers, with a relatively small amount of computation. There are also a large number of multichoice decisions to be made, most of which are not shown explicitly in that illustration. The "sort" and "collate" operations are not applicable to the system under design. A typical accounting application, as opposed to computing, consists largely of reproducing variable amounts of information, without change, from the input record, and from each of several file records, to a final output record assembly. Updated information also must be returned to the file records where necessary. A limited number of simple arithmetic operations are performed during the processing of transactions. If large amounts of machine-required arithmetic operations can be avoided, arithmetic power essentially becomes subordinate to the information-transfer requirement. This, in itself, might be considered as the major difference between an accounting machine and a computer. However, some arithmetic requirements, such as the fact that the same quantity must usually be summed into several separate running totals, lead to interesting possibilities for avoiding lost motion. In any case, it appeared that the proposed control system should be slanted toward the ability to mass-transfer large quantities of variable field-length information and the arithmetic requirements should be met as an adjunct to this ability.

In addition to the transfer and arithmetic operations, this machine system requires the ability to make three distinct types of decisions if it is to operate successfully as an automation. These are as follows:

1. Decisions based on static information wholly contained in a given record might be considered as "type of record" decisions and can usually be handled most efficiently by recognition of a code mark or character in the record. Thus, for example, the machine can make a decision based on the type of input card as to whether this transaction is an order, a stock receipt, or a customer payment record, and can go immediately to the program and procedure necessary to process that transaction.

2. Decisions based on the status of the transaction processing to date are usually the result of arithmetic operations and serve to indicate such basic items as "out of stock, check for substitute or back order"; "below minimum reorder level, signal for stock reorder"; "customer's credit allowance has been exceeded, so signal for manual credit authorization before shipment"; etc.

3. Decisions based solely on the sequence of processing to date is easily understood by the example of the case of substitutions allowed for out-of-stock orders. If it is assumed that item A may be substituted for item B if necessary, and vice versa, the procedure must prevent a second substitution if, after the first is tried, the second item is found to be also out of stock.

It is recognized that machine systems have been built that handled all three types of decisions by means of a single decision element actuated as a result of arithmetic operations. However, for all decision types other than the second, this method increases the requirement for arithmetic operations not associated directly with the requirements of the problem, which, in turn increases the complexity of programming otherwise straight-forward applications.

It was early recognized that the most direct method of machine-actuated decision-making was through the use of the control-panel concept and direct relay-switching of control impulses. The concept of the selector is well understood, and separate selector systems could be provided for each of the three types of decision element required. However, control-panel operation of the information-transfer function becomes unwieldy for large amounts of relatively poorly-sequenced data, particularly if the nature of the problem eliminates the possibility of considering the information as being

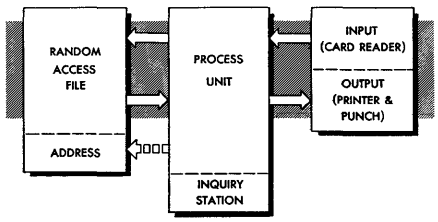


Fig. 3. Over-all aspects of the system

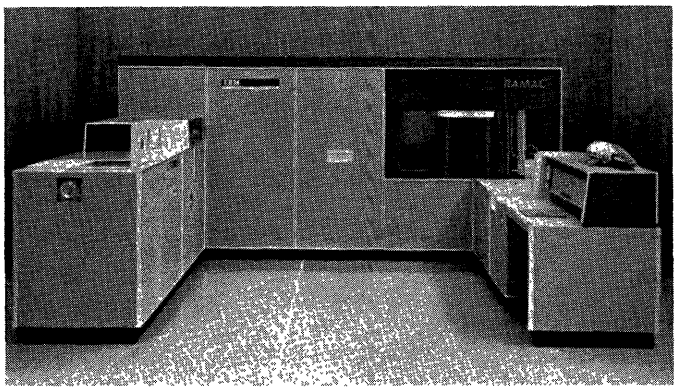


Fig. 4. IBM Type 305 RAMAC

grouped in elements of fixed word length. Thus, to handle variable-length information fields on a pure control-panel basis, it would appear necessary to utilize the technique of the basic tabulating accounting machine, that of carrying an individual wire for each character to be transferred and utilizing mass selection to program the problem. While this offers several advantages for the limited amount of format change required in output printing, and is used in the system for that application, it does not appear feasible for the major information transfer system.

Stored-program concepts used to date also offered several disadvantages. Various solutions to the variable-field-length problem are available, usually based on a record mark either inherent in the record itself or programmed into the machine by way of an intermediate transfer register. Both of these approaches put artificial restrictions on the programming and, in general, introduce program steps that are necessary because of machine restrictions and do not contribute directly to the processing of the transaction. Decision-making by way of traditional stored-program concepts was too unwieldy even to be considered (as it usually is based on single binary choices resulting from real or induced arithmetic inequalities).

The basic control system for the IBM Type 305 is a compromise offering the best features of both the control panel and the stored-program control systems. All information transfers during transaction processing are made through a stored program. The necessity for record marks is eliminated by specifying the number of characters to be transferred as part of the instruction. Each ten-character instruction thus completely specifies a single reproducing operation. The track and starting column addresses of both the sending and receiving process drum tracks involved are written, followed by the two-digit quantity of the number of characters to be transmitted. Arithmetic operations, in the form of addition, subtraction, distribution, and multiplication (absolute values only) were treated as information-transfers and programmed with the same form of instruction. Arithmetic entered into the basic format specification only because of our language inconsistencies. We read alphabetic information from left to right and do arithmetic from right to left. In order to propagate carries during arithmetic processes, the internal information transfers are made in a right-to-left manner. Thus, the starting column address for any transfer is the low-order column of the field. The system is completely analogous to setting up card processing routines, with added conveniences, such as the ability to distribute a single quantity into up to ten adjacent accumulators on two instructions, one of which would probably be necessary for a later multiplication in any case.

All logical decisions are made by means of selector wiring on the control panel. Process control may be passed at will between the two forms of control. Instructions follow in numerical sequence until after one is executed that is "flagged" by one of 47 symbols denoting transfer to the control panel. At this time, a control pulse is available from the corresponding one of 47 exit hubs on the panel. This pulse may be sent through a selector network and control returned to any instruction in the stored program, thus restarting the sequence. In this manner, multichoice decisions are made on a single operating cycle to the control panel.

The available decision elements, as noted in the foregoing, are all selectors. The three types of decisions are handled by three differently actuated sets of selectors. These are as follows:

1. Recognition decisions are made by means of a character selector that consists of points on a selector tree that is actually a single-character relay register. Any character in any record may be sent to this register, replacing its previous contents. This character then controls up to a 48-way choice by a single interrogation of the character selector.

2. Status decisions are made on several bases. Each of the ten accumulators carries its sign in relay storage, the points of which are available as selectors on the control panel. Thus, decisions may be made as to the status (plus, zero, or minus) of each of up to ten accumulators, at any time. Further status decisions may be made as a result of field comparison, identical or not, and on whether or not any significant information other than *zero* or *blank* was transmitted on the most recent information transfer. This arrangement is very convenient in spread-card applications.

3. Positional decisions may be made using latch-type relay selectors that can be picked up or dropped out by control pulses on the panel. Means for pulse-delay are also provided to eliminate relay races in setting up selector sequences through the points of controlled selectors.

Operation of the resulting system has demonstrated the flexibility and ease of programming built into the design. As predicted, programming has turned out to be essentially a matter of layout card forms for conventional punched-card systems. Most process decisions necessary are reached as by-products of useful operations and usually are built by a straight-through programming by information transfer—coming to the control panel once after all preliminary conditions are established. Although the machine has facilities for modifying its own stored instructions by internal operations, this is very rarely done. The main reason is that the instruction used is extremely powerful as compared to the conventional single-address operation, and all instructions are directly useful operations. Thus, the total number of instructions necessary to perform most transaction processing is usually relatively small. The secondary reason is that if the immediate instruction capacity of the process system should be exceeded for a given application, it is usually easier and faster to bring in ten new instructions as a single record than it is to perform arithmetic operations on one or two. Thus, the objectives of designing a straightforward process system to handle inline mechanized accounting were met largely by a correct choice of basic control procedure. This procedure should prove to be equally applicable to larger, faster machine systems designed for in-line processing.

General System Organization

Fig. 4 is a picture of the IBM Type 305 RAMAC. Physically, there are four distinct units within the system. At the right of the picture is the console which contains a card reader, switches and lights for control of the machine, and a keyboard and printer for file inquiry and

system test. The unit in the center is called the main frame and consists of the magnetic disk random access file at the right, the processing unit behind the two center panels, and the power supply behind the panel to the far left. To the left are the output units. In the background is the Type 323 card punch and in the foreground is the Type 370 printer.

Fig. 5 shows the system organization of the Type 305 RAMAC. Information enters the system via the card reader shown in the upper right-hand edge of the diagram. The information is written directly from the reading brushes onto a magnetic drum housed in the processing unit. On the next card cycle the information is read at a check station and compared with the data on the drum. Following a successful check the information is available under program control within the process unit. With the use of two tracks for input it is possible to parallel card feeding and processing operations.

The processing unit contains a magnetic drum with 33 tracks of 100 characters each and the circuitry for manipulating information on the drum according to a program that is also stored on the drum. Twenty of the drum tracks can be directly addressed from the program counter and make 200 program steps directly available for use. Additional program steps may be brought from any storage in the system and the 20 program tracks may be used for general storage as well as program storage. In addition, there are four general storage tracks, three tracks used in the arithmetic system, a track for use with the keyboard and printer unit on the console, two tracks used for output, and a timing track. The random-access file is connected to the processing unit at two points. The address register, which specifices the record to be read from the file, is a five position storage unit. Numbers from any part of the process unit may be sent to this unit. The selected record of the file unit, as specified by the address register, is available to the process unit for reading to procure information from the file and for writing to place new information in the file. The results of the processing are sent to the output track on the drum. The printer and punch take data directly from this track and print and punch it according to the rules set down on their respective control panels.

An inquiry system to allow calling records from the file independently of normal processing operations had been provided. The location of the required record is keyed into the keyboard, and at an appropriate time this record is procured from the file and placed on a special track into the process unit. Typing of the record from this track proceeds independently of normal processing.

Information Transfer

Information transfer between the process drum and the file occurs in blocks of 100 characters. Information transfer within the process drum may occur in blocks of from 1 to 100 characters according to the stored program instructions. Fig. 5, which depicts the transfer of information between two tracks of the process drum and the input-output section, shows how the first eight characters of the basic instruction are used to specify this transfer of information. Fig. 6 shows the means depicted for executing the basic transfer instruction.

All information transfers are routed through a 100-column core buffer unit. For the execution of any given instruction, the input to the core buffer is switched to the track which is to deliver the information. On the reading cycle the path from that track to the core buffer is closed at a time corresponding to that when the first position to be read is under the head on that track. The path remains closed until the number of characters specified by the "length" in the instruction have been transmitted, at which time the path is opened. The output of the core buffer is switched to the track which is to receive information, and that path is closed and opened during the writing cycle according to the position where writing is to start, as specified in the instruction.

The processing unit executes information-transfer instructions in sequence, as specified by a program counter which controls the next instruction to be read. The instruction reading is indicated in the center of Fig. 5. The "tens" position of the instruction register controls which program track is to be read from, and the "units" position controls which of the ten-position instructions on that track is to be read into the instruction register. Once an instruction is in the instruction register, the static contents of this register control the actual information transfer, as outlined above.

Arithmetic operations in this machine are handled in substantially the same manner as information transfer instructions. The accumulator system is a track on the process drum plus the necessary circuitry to handle algebraic addition and subtractions. If the accumulator track is specified as the receiving track in an information transfer instruction, the numeric value of that information is added to the value already on the accumulator track and the result is written on the accumulator track. Actually, the accumulator track may be specified as the receiving track in two ways, ADD or SUBTRACT. In either case the arithmetic system notes the signs of the two numbers passing through it, notes the instruction specification of ADD or SUBTRACT, derives the proper result, and writes this result back on the accumulator track. The circuitry is arranged to treat the 100 positions of the accumulator track as ten individual ten-position accumulators. Each of the ten accumulators has its own sign associated with it. Carries between accumulators are not allowed, and an overflow device is included to indicate this condition, should it occur. Transfers out of the accumulator track can either reset the part read out or not, according to the way that the accumulator is specified on the read-out instruction. There is no restriction as to the number of positions that may be read to the accumulator

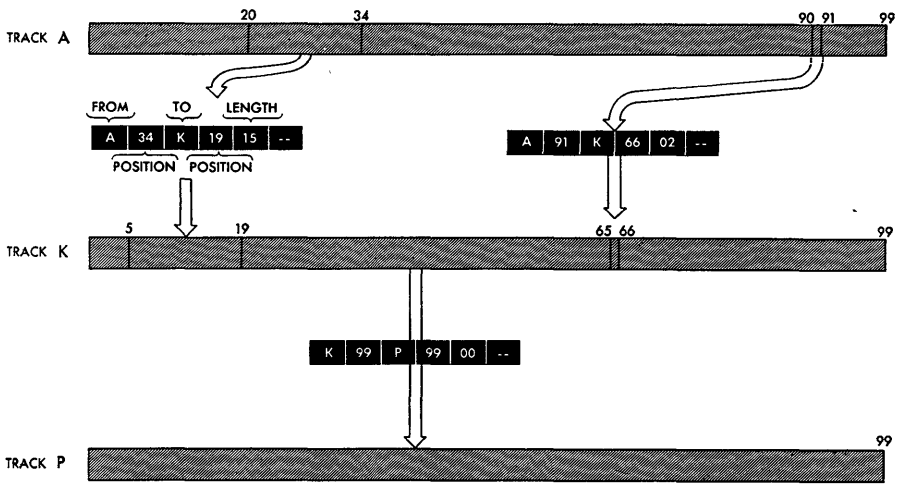


Fig. 5. Means depicted for executing basic transfer instruction

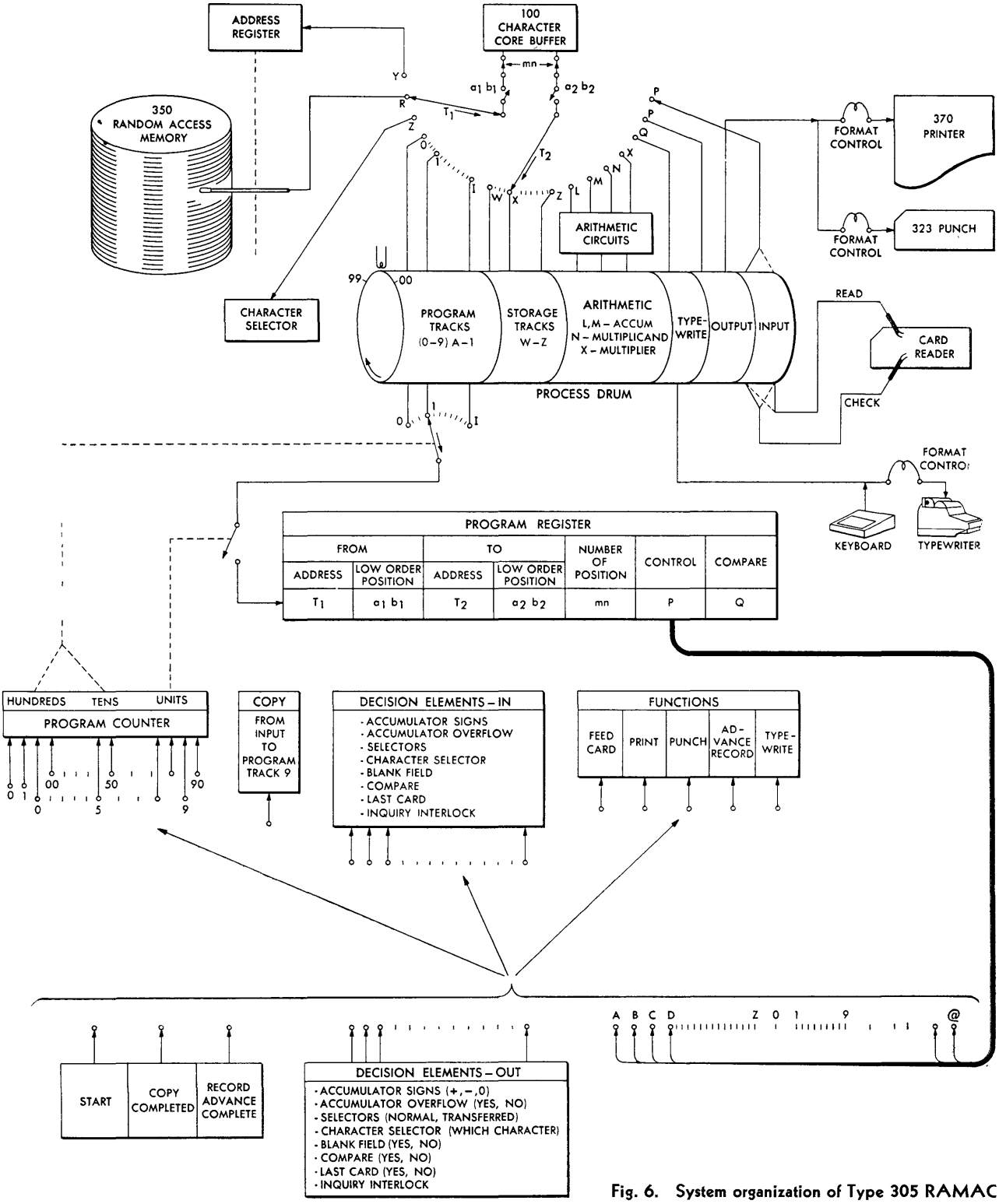


Fig. 6. System organization of Type 305 RAMAC

track on a transfer instruction. Thus, several additions may be completed on a single instruction.

As with addition, multiplication is also handled as an information-transfer instruction. There is a multiplicand track, and specification of this as the receiving track will cause the number transmitted to be written on this track ten times. A maximum of nine characters can be read to this track. Specification of the multiplier as the receiving track in an instruction will cause multiplication of the number transmitted on this instruction by the number on the multiplicand track. The product is stored in the first two accumulators on the accumulator track. The multiplication process is simple, in that each multiplier digit merely chooses when to start adding the information on the multiplicand track into the product register. The multiplicand track may be used for operations other than multiplication. One such use is to send a number there and then add all or part of this track to the accumulator track. In this manner the same number can be used to affect balances in several accumulators in a single instruction. This distribution function is the reason for writing the tenth field

on the multiplicand track of the arithmetic system.

Any information-transfer instruction can be converted from an actual transfer to a comparison of the data specified on the "From" and "To" tracks by placing a *1* in the tenth position of the instruction. The result of the comparison is made available for control operations to be described later. Thus, if we wish to compare a name that is on track *A* from positions *20* to *44* with a name that is on track *J* from positions *65* to *89*, we would write the following instruction:

A 44 J 89 25 ( )1

There is also a field compare operation made possible by inserting a *2* in the tenth position of the instruction. This instruction compares the data from the two tracks specified and makes comparison results from each block of ten characters on the tracks available for control operations to be described later.

In addition to the drum tracks already mentioned, there are two other units that may be specified as receiving locations in an information transfer instruction; these are the address register and the character selector. The address register is a five-digit storage unit where numbers are placed to specify the location of the records required from the file. A regular information transfer instruction is used to place a number in the register. A subsequent operation causes the arm on the file unit to go to the location specified. The character selector is a one-position storage unit to which any character in the system may be sent using an information transfer instruction. This may be analyzed partially or completely during a control operation.

This completes the discussion of the information-transfer aspects of the 305 system design. In summary, the objectives were to provide an effective yet readily understandable means for manipulating information in a manner required in business data processing. In general, the 305 has achieved this by:

1. Handling alphabetic and numeric information with equal facility.
2. Providing for variable-length transfers as a basic characteristic of the system.
3. Including an arithmetic system capable of handling several numeric balances simultaneously.
4. Providing an alpha-numeric comparison facility.

Processing Control

Among the requirements of data processing are a means for altering the way in which different situations are handled. As was pointed out in the first portion of this paper, the 305 uses two mechanisms for accomplishing the required results. A stored program is used for information transfer and a control panel for the control functions. The general approach is to set up the conditions for control with the information transfer instructions and then to wire the means of considering these conditions on a control panel. The ninth character of the instruction provides the means for testing these conditions at a predetermined point in the instruction sequence. An alphabetic character is placed in the ninth position of an instruction, and at the completion of the execution of this instruction the number in the program counter is dropped, and an impulse is made available on the control panel via the hub corresponding to the letter used in the instruction. This hub will be wired through various decision elements back to an entry point in the instruction sequence. Physically, the impulse travels through relay points controlled by the decision elements and picks up a new position in the program counter. The position that is picked up is determined by the status of the decision elements and the control panel wiring.

The decision elements available on the control panel are as follows:

1. Condition of the 10 accumulators—plus, minus, and zero.
2. Contents of the character selector.
3. Status of the latest comparison made.
4. Status (blank field or not) of the latest information transfer or field comparisons made.
5. Status of a group of latch selectors (relays) that have been picked or dropped at previous control points.

With these decision elements, the normal process in programming an application is to set up the conditions for several decisions and then to make a multiple branch in the program. The net result of the control system is to provide a mechanism whereby many instructions do not have to be utilized in making the decisions necessary in the process.

This aim is accomplished by concentrating the decisions to a few points on the program. Another feature of the system lies in the programming simplicity achieved, where the programmer can physically put his decisions together on the panel without an elaborate review and rearrangement of the stored program. This latter feature is particularly advantageous, as it is usually in the control area that the more intricate problems in a program develop, and here the programmer has a chance to consider these problems independent of the more voluminous but less intricate information transfer.

Input-Output File Controls

An important part of the 305 design is the operation and control of the input, output, and file units. The three aspects of importance in considering these units are: (1). the means of initiating operations of each unit, (2). the controls within each unit are substantially independent of the process unit, and (3). the interlock system between these units and the process unit. Operations for the input, output, and file units are initiated by control panel wiring.

The controls within each unit must be discussed for each unit. On the card reader two tracks are provided. The card reads directly to one track, while the other track is available to the process unit. A card-feed impulse transfers the track just used by the process unit to card-read status, and the other track from card-read status to availability to the process unit. This impulse also initiates feeding a new card to the track just placed in the card-read status.

The printer and punch both obtain information from a single output track. The control as to what information to print or punch and how, is within the print and punch units. In this manner the process unit only need place the required information on the output track. Print functions such as format arrangement, zero suppression, etc, are specified on the print control panel. Punch arrangement on the card is specified on a punch control panel. The print or punch signal initiates the proper operation. Information on the output track is analyzed to determine the specification as to the mode of printing and punching.

The file is given a new address by transferring a number to the address register which starts the file access mechanism into motion.

A similar interlock system is used for integrating the operations of all peripheral units with the process unit. The basic approach in the interlocking system is to achieve a basic overlap of operations such as card feeding, processing, printing, punching, and file seeking. This overlap has been achieved by providing sufficient controls for each unit such that interlocks are required only when there is a conflict in the needs of two of the units. An example of such a conflict would be for the process unit to attempt writing on the output track when printing and punching of the data there from the previous operations had not been completed.

At such points an interlock would be effected. Writing on the output track would be prevented until such time as printing and punching were complete. Similar interlocks are effected for card reading and other operations where these conflicts can develop.

The result of the interlocking and input-output-file controls is such that for any given application the time chargeable to a transaction on the machine is the longest of the card feed, print, punch or processing functions for that transaction instead of the sum of these. At any given time, it will be normal for the machine to be processing a given transaction, feeding the card for the next transaction, and printing the results of the previous transaction.

Table I. Machine Speeds

Unit	Speed
Card feed	125 cards per minute
Printer	50 columns per second . 30 cards per minute
Punch	100 cards per minute
Process unit	30 ms per STEP + 20 ms per STEP with control transfer
File	.08 second maximum . . 0 15 second minimum

Machine Speeds

The speeds of the various units within the RAMAC system were set to achieve a balance in the time that each unit spends upon a given transaction. The printer was the first unit chosen and the speeds in the remainder of the system are balanced to the printer speed. Tables I gives the speeds of the various units in the RAMAC system.

In any given problem the over-all machine speed will be limited by one of these units. In loading the file from cards, the machine will normally be card-feed limited, and in punching the file on cards, punch-limited. In a typical billing job it would probably be printer-limited. At two seconds per line we get 1,800 lines per hour. At reasonable utilization rates, the objective for the machine of 10,000 line items per day can be achieved.

Discussion

W. Y. Stevens (Cornell University): Can you give a rough monthly rental figure for the equipment shown in Fig. 4?

Mr. Lesser: Strictly speaking, this is a matter outside of engineering, but the last number that was heard, which seems correct, is $3,200 a month.

W. L. Wetmore (Corning Glass Works): Can more than one memory unit be attached to one such computer unit?

Mr. Lesser: Again, to use an answer from one of the previous speakers, from a logical point of view there is nothing that would prevent this.

Chairman Howard: If not, can separate units (complete) have access to data contained in the other? In either case, what are the practical limits?

Mr. Lesser: This machine system is a first attempt at this kind of a device, and no such options have been announced to date. One of the things about the large file concept is that it makes a very fine large-scale buffer between devices of different kinds. From a theoretical standpoint, there is no reason why you could not have multiple processing stations operating on a single file or, conversely, multiple files operating on a single processing station. The probable limitations would be a matter of balance, rather than anything else. In other words, to oversimplify, it probably would not pay to have several thousand files attached to a single device doing 10,000 transactions a day.

C. Lammers (John Diebold & Associates): What is the access time per record when the access arm is at the desired disk? When the access arm must search for the desired disk, what is the access time per disk?

Mr. Lesser: The access time per record when the access arm is at the desired disk and track is exactly the same situation as on a drum. If the disk array rotates at 1,200 revolutions per minute, you always have to wait a full drum revolution (in spite of "averages") because your record is always the furthest one away. In theory, it would be half a disk revolution or of the order of 25 milliseconds. When one uses the access mechanism as a receiving address and sends a 5-digit number which corresponds to one of the 50,000 records being looked for, the arm takes off immediately. There is complete overlap, so that the machine can continue processing until it needs the information from the file. An interlock is only hit if the needed information has not arrived. The mechanical access time runs between about 150 milliseconds if one is on or very close to the same track on the same disk, up to 200 milliseconds if on the same disk, and up to about 750 or 800 milliseconds if one must go from inside the top disk to inside the bottom disk. Statistically, it works out to about 600 milliseconds on the average, on a true random basis.

E. Buejer (Underwood): How many tubes in the equipment?

Mr. Lesser: There are 1,520 tubes in the version described.

M. J. Mendelson (Norden-Ketay): What do you do about description-type stock numbers which are not commensurate with your coordinate system of addressing?

Mr. Lesser: This is called automatic addressing and is a subject of several papers. There seem to be two classes of papers on this. One of them, of course, is a group of highly mathematical "randomizing" approaches. The other line is a rather clever "let us try and do it and see what happens." In essence, one performs some kind of repeatable randomizing operation—randomizing is a poor word. What you are trying to do is get a more or less uniform distribution of the part numbers of interest in the portion of the file that you have allotted for them. One way is to take a certain segment of the descriptive part number, square it, take a piece out of that and multiply that by a packing factor and use this as an address. The "optimum" segment of the part number is picked—this is where the cleverness pays off.

One of the properties of the device is that ten records are available at one mechanical location of the access mechanism. A technique that has been used (it seems to work quite well) is to compute only a four-digit address, and then use one of the ten records thus found for an index to the other nine. Then the actual part number is used to find which of the other nine records available at the access location is the desired one, or if it is "overflowed" to another location, or if the desired record is not in the file at all. Overflows on very simple-minded randomizing schemes (trying to pack the file 80 per cent full, say) are of the order of 7 per cent. There is an old rule in the business that is known as the 20–80 rule: 20 per cent of your items are 80 per cent of your activity. So when the file is loaded in the first place, the very active items are put in first, the very dead items last, with all others in between (using the same technique to load as will later be used to search). Thus, the very great majority of activity is directly to the desired disk track, and the occasional overflows (requiring another mechanical access) are so infrequent as to make little difference to the average transaction rate of of the system.

Conference Summary

JOHN W. CARR III

HARDLY had our Conference chairman, on Monday, opened the sessions than the major problems of our somewhat diffuse computer field began to raise their ugly heads one by one from the platform.

Mr. Engstrom, who works for the Defense Department, immediately raised for most of us and for himself the question—How can an art, a science, an industry, if you will (depending upon how you look at it), with such tremendous "pay-off" in individual human effort, fail to be inflationary in its own requirements for manpower and material? The questioner from the audience who facetiously asked Mr. Engstrom (and I don't know whether he was so facetious, after all) why his organization did not stop creating demand for computer personnel might just as well have, like King Canute, ordered the waters to roll back. The stakes in automatic digital information machines in the Defense Department and its grim war games are so high that such things as the hushed salary discussions in a corner of the lobby, or the quiet descriptions of the newest project that can be worked on, have to be allowed to continue.

Even Mr. Whitelock of the Navy Department cannot hide the problem that his and every other organization must face, both before and after the equipments are obtained: Where are the people to come from who will develop, maintain, and use these new monsters, devourers of both information and personnel? Mr. Calhoun, in his travelog of computers through 15 countries, returned to this theme. In England and on the continent, he notes, the men who a few months ago were leaders in university laboratories have now left their graduate students behind, or else have taken these students with them, to work in one of many new commercial computer design laboratories. Here in this country the program for these sessions has reiterated the problem.

Three years ago, a joint computer conference was studded with papers by university personnel and members of university laboratories. Today, with the exception of ably presented papers from the Massachusetts Institute of Technology's Lincoln Laboratory and the Stanford Research Institute, no university representatives are participating except in the less important positions of chairmen and, of course, conference summarizers.

This is not a complaint, but a call to meditation. There are in fact still activities continuing in universities, and I might mention a few. First of all, Prof. Perlis and a small group at Purdue University and the Carnegie Institute of Technology are among the first to write an algebraic language and a translater for two different (and competing) machines, so that problems in the same language can be performed both an IBM (International Business Machines Corporation) and Datatron equipment. Prof. Scott and a small group at Michigan are developing important teaching techniques in computer design. Their building-block computer has been begun, and they are carrying on fundamental research in high-speed components. Prof. Rubinoff of the University of Pennsylvania, with graduate students and other professors, has finally shown that digital computers can outdo analog computers in real-time simulation. Prof. Meagher and his group at Illinois University have plans for a computer with speeds to match any discussed at the conference. And there are others.

These are, however, I am afraid, isolated cases with tenuous futures. In general, the problem can be stated thus: In the area of computer design, are we letting the wells run dry at the source? First, the role of the universities here shall be that of a critic. As someone has said, if you cannot produce, teach; if you cannot teach, become a critic.

There were other omissions from the program that are worth pointing out. First, the absence of automatic programming techniques and any discussion about them should be marked. This is not in criticism of the program committee; I have in my files a copy of a letter of some months ago written by one of the members bemoaning the lack of papers in that area. We have not heard any discussions about automatic programming techniques at the meetings, but there do exist such new computer techniques in the languages such as that of Professor Perlis' common language for the 650 and the Datatron, the Boeing common language for the Univac Scientific and the IBM types 650 and 701, the Fortran language for the 704, and the AT-3 algebraic translators planned for the Univac.

The absence here, I think, is one of communication, and instead of the artificial wall tumbling down between the logical designer in hardware on the one side and the logical designer in stored programs on the other side, it appears from this meeting that the wall rises higher than ever.

Take, for example, the idea of what I shall call "associative memory." We all have it. When you think of Christmas, you think, perhaps, in terms of snow and your overshoes and your wife, who reminds you to put them on, and so forth.

The first such man-planned associative memory that I know of has been proprogrammed by Cliff Shaw at the Rand Corporation, working with Newell and Simon of the Carnegie Institute of Technology. They term this rather amorphous portion of the Johnniac internal memory "The Pit," because they can toss any piece of information they wish to remember at random into any vacant position in this "blob," if you will, with the full anticipation of retrieving it later on as part of a sequence of associations. Remembering how B-boxes and floating-point finally became part of the hardware, I will rather softly predict that perhaps one of the future uses of Mr. Buck's cryotron might be in such an associative memory.

Our third problem, then, is communication; and no one put it more eruditely or wittily than Sir Watson-Watt. Those of us who had the pleasure of hearing him at the luncheon heard him beg us to break our semantical chains in computer communications. I extend the plea to urge all of us to try to overcome the artificial barriers that appear more and more to isolate the user from the designer.

Here, then, are three problems that have thrust themselves rather ostentatiously before us, starting from Mr. Engstrom's opening remarks:

1. The problem of manpower, or how to continue to find personnel to satisfy the needs of an everexpanding computer research economy.

2. The problem of the preservation and rehabilitation of the position of the universities in the area of computer circuits, design, and logic.

JOHN W CARR III is professor of mathematics at the University of Michigan, Ann Arbor, Mich

This is a condensed text of the Conference Summary presented at the Eastern Joint Computer Conference in New York, N. Y., December 12, 1956.

3. The problem of intercommunication across the artificial barriers, such as, for example, that which separates the logical program designer from the logical hardware designer.

I do not pretend, of course, to have the complete answers to these three problems, or that there are any, but I shall put forth a tentative beginning toward a solution.

The three problems are intimately interrelated. They all involve, as you might suspect, our university research and educational programs. This tentative solution does not, oddly enough, require vast sums of money, but instead requires a great deal of something more often in much shorter supply, even in our own field—imagination.

The shortage of professional computer manpower cannot be relieved by artificially bidding up what little there now is in supply. New additions must, as Mr. Engstrom says, come from outside. And I add, they can only come from below, from persons developed by university professional graduate programs. One obviously cannot relieve the shortage by hiring those university electrical engineering and mathematics professors that show signs of ability, and taking them away from their present posts. And may I add, on the subject of prostitution, that when a university professor finds a student of 4 years before earning 4 or 5 thousand dollars more than he does, even his professional chastity begins to totter. Nor can one relieve the shortage by drawing away the better graduate students to the computer design and development laboratories before they acquire their Ph.D.'s. No matter how one disguises it, a commercial laboratory, in my opinion, is not a university.

Instead, a little "seed money," judiciously placed, might prove an exceedingly high "payoff." Suppose the high light of the Joint Computer Conference 2 years from now were to be the presentation of the prize-winning paper by a university graduate student in the area of information systems design? A prize of $5,000 for further study in the area of computers, provided by, perhaps, Mr. Engstrom's employers, supervised by the National Science Foundation, and judged under the auspices of the Joint Computer Conference, would be, it seems to me, a worth while enticement to many a bright young engineer or scientist.

Or what about the professors? The trend has been obviously, on purpose or not, away from using university research talent at the universities. The trend has been, rightly or wrongly, away from encouraging university work on computer systems. Even if those who parcel out the resources in Washington believe that the day of the university over-all systems design is dead (and I believe that that decision would be utterly absurd), university research and talent can still be used on smaller portions of the over-all problem: Paper designs of systems, storage components and circuitry, and automatic programming. When university research in computers disappears, university teaching in that area crumbles, and when the latter happens, not even a trickle of qualified graduate students educated in any depth will talk to your recruiting personnel as they make the rounds.

Finally, on the problem of communications: How is a discipline organized so that it can intercommunicate? Generally, that job is a labor of love by university professors who pass the discipline on, better organized, better evaluated, and better placed in the proper perspective. Who write the treatises and the textbooks that serve as the starting points for the newcomers in the field? Again, persons in the universities. Who, in the final analysis, develop the glossaries and the standard terminology? Committees of the professional and technical societies, nominally, yes, but the university teachers accept or reject them, mold and shape them, in passing them on to the next generation.

There is no easy solution to these problems that have been jointly posed. My argument is that the answer is not in killing the goose that lays the golden eggs, by hiring away professors, neglecting the granting of university contracts in computer design and development, leaving the universities as the last research areas in our societies to have adequate high-powered computational equipment.

Nevertheless, I do not want to underestimate the assistance given to the universities by several organizations. The industry, and the government that receives its benefits, owe much to the beginnings made at the University of Pennsylvania, the Massachusetts Institute of Technology, the Institute for Advanced Study, the University of Illinois, and other schools. The rules of research productivity do not change overnight.

Therefore I should like to say, as the result of our meditations, that if a lack of imagination, not of money, a lack of reasoned self-interest on the part of some manufacturers and, perhaps, a weakening under obvious pressures on the part of Mr. Engstrom's employers, leave no computer systems design or circuitry research in the universitites, or very little, as a result, your new designs may fit only the average commercial user's adequate pocketbook and inadequate imagination.

Feed a little "seed money" of the many millions being spent into this area, and there is a chance that the problems of personnel, advanced research, and intercommunication may still be resolved.

Again, as a critic in the more nearly true sense of the word, let us go on from Mr. Engstrom's and Mr. Whitelock's discussion. Let us evaluate the technical and relatively noncontroversial problem portions of our program. What are the goals of our present computer technology? The apparent goal is to solve new problems with the following characteristics:

1. Much more input and working data to be required.
2. Necessity for higher speeds in processing.
3. Necessity for more rapid and more nearly random access to the large amounts of data required.
4. The extreme difficulty of formulation, and later programming, with the use of conventional methods.

It is my contention that giant strides have been made and discussed in the 3 days in the first three of these areas. But in the fourth, the extreme difficulty of formulation and later programming still looms, almost completely untouched, as the largest problem of all.

How are these problems to be solved? By producing equipment as follows:

1. More efficiently mass produced, with a lower cost and smaller size.
2. Much more rapid and therefore much less expensive per unit operational cost.
3. Having more reliable individual elements and therefore much greater over-all systems reliability.
4. Matching better the human to the machine, and meanwhile operating more automatically and therefore more reliably.

Again, great strides have been made and discussed during the three days' session in the first three areas: production and size, speed and expense, and component and systems reliability; but the improvements in the area of systems match to human being, for example, and over-all automatism must again await the final results of systems which have been merely broached or discussed here.

To meet the needs for greater amounts of internal storage combined with more

nearly automatic production than that offered by the six Swedish girls who wired the BESK memory in their living rooms, we have been offered, among other things, some very interesting devices. A wound memory element to replace cores has been described by Mr. Tracy. Dr. Rajchman proposes solid plates of material, easily machined. Pohm and Rubens would use magnetic film strips to aid in the production problems.

As to reliability, there seems to be common agreement that the burial of the vacuum tube is long overdue. "The King is dead," but there is violent disagreement over who the new king should be. We have computer circuits with almost every possible combination of elements.

There are computers or circuits that generally use only transistors and resistors in Direct-Coupled Transistor-Logic circuitry, such as the Transac described by Mr. Maddox, and the Tradic Leprechaun described by Mr. Githens. Mr. Andrews bases his logic on a nonlinear inductance. Mr. Hogue proposes a combination of diode gating with nonlinear inductance. And finally, Mr. Buck proposes circuits made up of nonlinear resistance alone in the cryotron, with driving power now furnished by a refrigerator. The logical designer should be a happy man. He apparently has no dearth of building blocks to work with.

The problem of input-output data handling, if the number of papers is any criterion, has not received the attention that the more glamorous but no more important circuitry has obtained. The three gentlemen from Stanford have neatly combined two signals in one carrier—magnetic—ink and have shown that the presence of large amounts of optical noise does not affect magnetic reading. Let us hope that they will have the chance to extend their device to many more symbols on arbitrary page formats.

The ubiquitous transistor turns up once again in the Radio Corporation of America's transistorized card punch. We can only chide the authors mildly by reminding them that, while eliminating the vacuum tube, they have not yet eliminated the punched card. The electrographic printer and recorder of Epstein and Kintner is a working system that deserves further study. It shows the computer user that he is not forever bound to mechanical and photographic devices. Further effort will be greatly appreciated by persons using computing machines to see that the technique of simplified display-plotting can be extended.

We might divide new systems very quickly into "conventional" or "unconventional" devices, with "conventional" or "unconventional" approach. Under the first category, which I will call "conventional devices with unconventional approach," one might list the DATAmatic 1000, the TAPEDrum, the National Cash Register Corporation (NCR)-304 machine, and the Datafile addition to the Datatron system.

For example, the DATAmatic 1000, as discussed by Mr. Smith, is basically similar to most data processors, but its designers felt that the key element was getting information in and out of the machine, so they widened their tape. Mr. Hollander's discussion this afternoon of the TAPEDrum, of course, carries this procedure to the logical extreme. The NCR-304 produces again a conventional machine, but with some unconventional procedures that are well worth noting—for example, the concept of a multilength, multiaddress instruction logic on their various sorting and file instructions.

The Datatron system with the Datafile, at about twice the cost of an ordinary tape mechanism, apparently, is a device which will far better satisfy the vast majority of the users' needs.

A second list might be "unconventional devices with a conventional approach." The Tradic computer uses the newest DCTL circuitry, but to me it is very much like the old Whirlwind I of almost 8 years ago, in a smaller box. The Transac S-1000, discussed by Mr. Maddox, is an all-transistor computer, unique in its circuitry, but surprisingly like the Univac Scientific. The TX-0 is a very simple machine, built around a fantastically large memory.

Then we can list "unconventional devices with an unconventional approach," where nothing is spared both in circuitry and in components, and logic of design. First in the time schedule, apparently, is the Univac-Larc for being the first machine produced. Dr. Eckert discussed the problem of parallelism of structure. There are to be both editing and calculating devices running at the same time, with the possibility of two independent calculators. There will be solid-state components techniques. We have heard about several, which may be the forerunners, from Mr. Bonn and Mr. Torrey, Mr. Keilsohn and Mr. Smoliar, on the accumulator and the shift register that they have devised, using ferractors. We heard about the drum file with moving and floating heads, of 18-megabit size.

The machine which was projected further into the future, and which therefore used more "blue sky" components, was the IBM Stretch. Mr. Dunwell again showed that they intended to use parallelism of structure. New techniques and circuits are still under development, aiming at 10-megapulse transistor circuitry. Mr. Lawrence showed us an unusual magnetic-core structure at speeds of possibly smaller than microseconds' access time. Mr. Lesser and Mr. Haanstra have talked about the magnetic disk, which is part of a 305 system, but which is also to be part of the Stretch, if the discussion is correct.

Finally, we have had the projected new catalog method, making use of the cryotron, discussed by Mr. Slade and Mr. Buck, in which they told us that they could simultaneously detect in coincidence one item out of half million in about 10 microseconds.

One last point which I think is of interest is that both the Larc and the Stretch are to be built for the first time apparently from the outside in, or somewhat so, as an integrated system, in an integrated systems approach, with the external language of communication as the starting point and with automatic programming techniques in carrying the language on into the middle of the machine. The delivery of the machine will contain complete compiling systems in both cases.

There is one last omission I would note, and I am afraid it will remain with us for a while. It is that last break-through from the pattern of the general-purpose selective-sequence stored-program calculator as we know it.

There are already minor cracks in the armor of our historical patterns. We see systems in which there are several operations being performed concurrently. Information is forced through channels at a rapid rate by paralleling beyond our recent dreams. But our machines are still the same old combination of desk calculator, girl operator, and notebook, that was the model for the EDVAC and the Princeton series. Perhaps the girl now has two notebooks, or writes with both hands, or works two desk calculators at once, but the same structure is basically there.

Criticisms of this sort, by nonproducing critics, are of course a prerogative only of the university person. What have I to offer in return? Just this: Some day, on a similar occasion, an engineer or a mathematician will come before an audience such as I am addressing and describe a device which will accept information from its environment, process it

inductively, meet situations not specifically planned for by its designer or designers, and make decisions on a basis of "studied reasoning"—whatever that may mean.

To me, this is our ultimate challenge, perhaps an unattainable Eldorado, but nevertheless, the "controlled thermonuclear reaction" of the computer world, the "big job," toward which parallel computers and megabit memories and solid-state designs are only the stepping-stones and not the ends in themselves.

Such machines must automatically have the ability to accept one another's languages, the ability to accept problems which have not been formulated formally, for which there has not yet been a detailed program set down; and they must of course have a reliability far beyond that of a human being to avoid any momentary aberration.

Men are thinking about such machines now, sometimes in the large commercial laboratories, but more often in university departments or independent laboratories, talking of inductive machines, learning devices, theorem-provers, and environment adaptation.

Those of us who are readying the components should be kept aware of the needs. Those of us who are dealing with systems should remember our systems' present limitations. The job of intercommunication, as Sir Watson-Watt noted, is most important.

What can be done in the final analysis? I have heard comments, for example, on the size of the meeting. I think its growth is vigorous, but the dinosaur also had its day of collapse. I offer as a companion alternative to complement such affairs comparatively tiny meetings —10 to 30 people from different organizations, meeting across occupational boundaries: logical designers with programmers, circuitry personnel with automation specialists, language specialists with programmers, and so on. Such meetings have already been held, more or less successfully—for example, the microprogramming conference at the Massachusetts Institute of Technology or the automatic programming conference at the Carnegie Instiute of Technology.

The universities, I think, will be pleased to serve as stimuli. Meanwhile, as a British friend of mine has said, "This is the best one of these meetings I have ever attended. A lot is going on."