REVISION RECORD

REV	CHANGE DESCRIPTION	DATE	APPR	ECO	M/F
A	INITIAL RELEASE	1-7-83		10083	

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FINISH	APPR	
DIMENSIONS ARE IN INCHES TOLERANCES - UNLESS NOTED .XX ± .XXX ± ANGLES ± °	DO NOT SCALE DRAWING SCALE	TITLE: 8432 PRODUCT SPEC. SHEET OF
USED ON: 84-9801-4809-8	CLASS CODE	SIZE: A PART NO.: 78-8026-6052-8 REV: A

TABLE OF CONTENTS

1.0 SCOPE

This document outlines the specifications for one 3M 8432 Compact Disk Drive.

2.0 INTRODUCTION

The 3M Model 8432 Disk Drive is a dual 210 millimeter diameter platter, 20 megabyte disk drive that uses Winchester technology. The controller interface to the drive is the ANSI Standard X3T9/1226 Interface for Eight Inch Rigid Disk Drives. The disk drive system is modular and is comprised of a Disk Module (DM) and an Electronics Module (EM).

3.0 REFERENCE DOCUMENTS

3.1 Users Manual, Model 8431/8432 Compact Disk Drive.

3.2 ANSI X3T9/1226 Standard for 8 Inch Rigid Disk Drives.

3.3 UL 478, Electronic Data Processing and Systems.

3.4 CSA Standard C22.2 No. 154 Data Processing Equipment.

4.0 FUNCTIONAL OUTLINE

4.1 Disk Module (DM)

Electronics for the Disk Module consist of three PC boards. A large PC board, termed the DM Board, contains the preamp control, stepper drive, spindle control and spindle drive circuitry. This board mounts to the factory sealed "clean air" enclosure which contains two disks, brushless spindle motor, stepper motor, four R/W heads, head arm, and a head preamplifier/write drive chip affixed to the arm. A second, and smaller, PC board contains the photo sensors used in the commutation of the brushless DC spindle motor and the index sensor. This PCB is also mounted on the deck casting. A third PC board contains the spindle motor filters.

4.2 Electronics Module (EM)

The EM consists of a Mother Board and three plug-in PC boards. These boards contain the following functional elements:

4.2.1 Mother Board

+ 12 volt regulators;
+ 6 volt regulator;
- 4 volt regulator;
Board Edge Connectors for the other three boards;
DC power connector;
All interconnects between boards;

4.2.2 Interface Board

Microprocessor, RAM, ROM, Timers;
Line Drivers;
Line Receivers;
Control Registers;
ANSI Interface Cable Connector.

4.2.3 Control Board

Fault Logic;
NRZ to MFM Encode;
Write Pre-compensation;
Crystal Reference Clock;
A-D Converter;
Write Current DAC
Temperature Compensation

4.2.4 Data Recovery Board

Read Clock Phase-locked Loop;
Read Window Generation;
MFM to NRZ Decode;
Early/Late Data Strobe.

4.3 Indicators and Switches (See Figure 4.5)

4.3.1 Write Protect Switch (WPS)

When this switch is set to the ON position, write current is inhibited to the head, regardless of all other conditions. A write attempt, in this situation, will produce a FAULT condition.

4.3.2 Indicators

A red LED above the Write Protect Switch is illuminated when the Write Protect Switch is ON. A green READY light, to the right of the WPS, is illuminated when the system is able to accept and execute commands from the controller.

4.4 Functional Diagram (See Figure 4.4)

4.5 System Configuration (See Figure 4.5)

5.0 DISK DRIVE SPECIFICATION

See Table 5-1 for detailed drive specifications.

5.1 Power Requirements

If the operating environment exceeds 40°C (measured 3" in front of the drive card cage), the voltage tolerances are changed to:

+ 5V	5V ± 5% @ 2.7A
- 5V	-5V ± 5% @ 0.5A
+24V	24V +2% -10% @ 3.5A*

The stated tolerances include ripple and noise.

*The 3.5A may be exceeded for 1.0 second during drive start-up.

5.2 Operating Temperature (Non-Refrigerated)

The operating environment must be moving air (10 CFM Min, 40°C Max) to minimize hot spots at various locations on the drive. If the operating environment exceeds 40°C but not 50°C, the air flow must be 100 CFM minimum to maintain the drive casting temperature below its maximum of 65°C. This temperature may be monitored by use of the vendor unique command "30" (see paragraph 7.5 for details) or a thermocouple/RTD may be mounted as shown in Figure 4.5.

5.3 Power Connection

Power connection to the 8432 drive must be made such that "24 Ret" and "GND" are tied together at the supplies to prevent damage to the drive. See Figure 5.3.

5.4 Rezero

This command will cause the drive to position the heads over cylinder zero and reset Read Control to normal. The General Status Byte is returned to the controller during the Parameter Byte portion of the command sequence. Upon the completion of the positioning of the heads over cylinder zero, the drive will generate an Attention Condition.

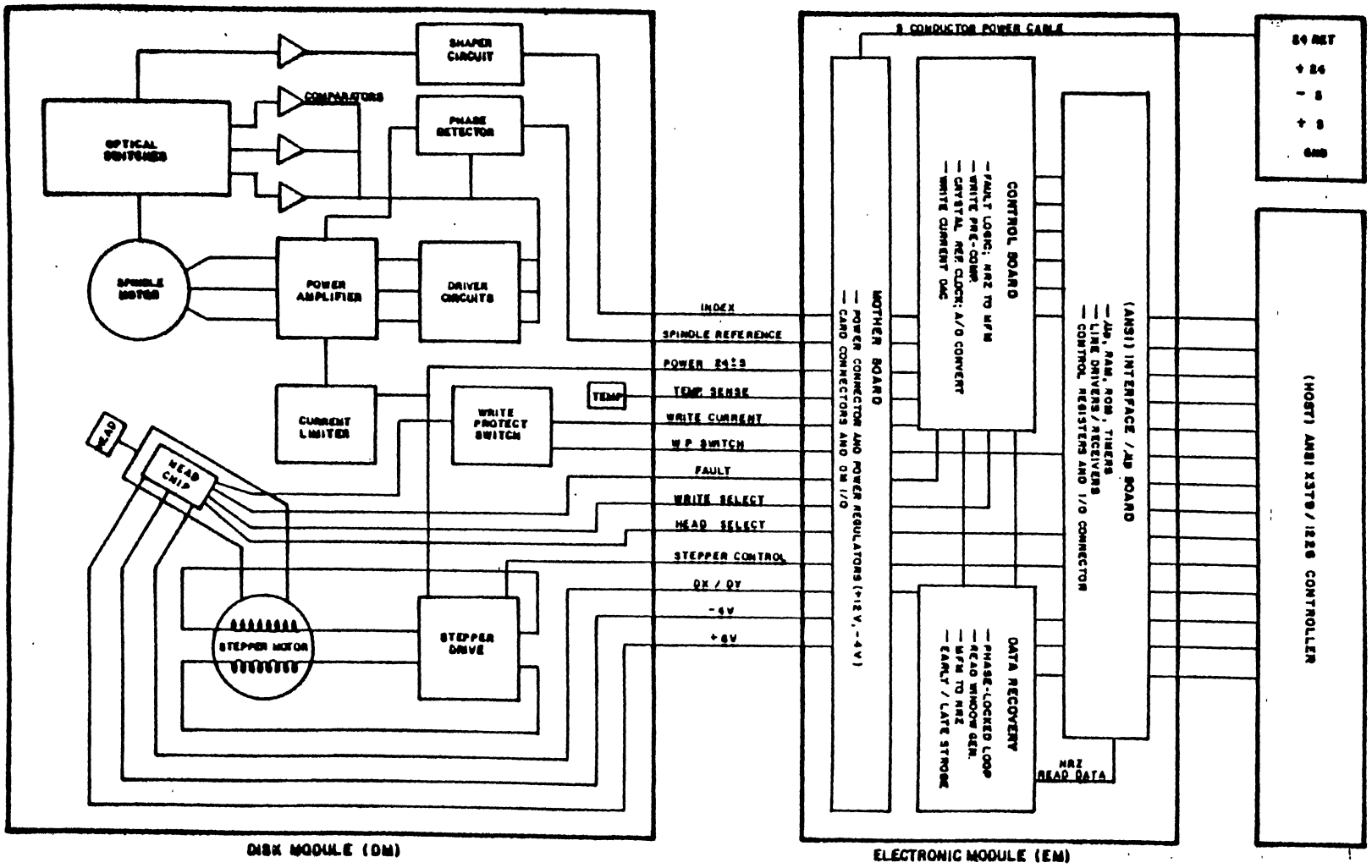
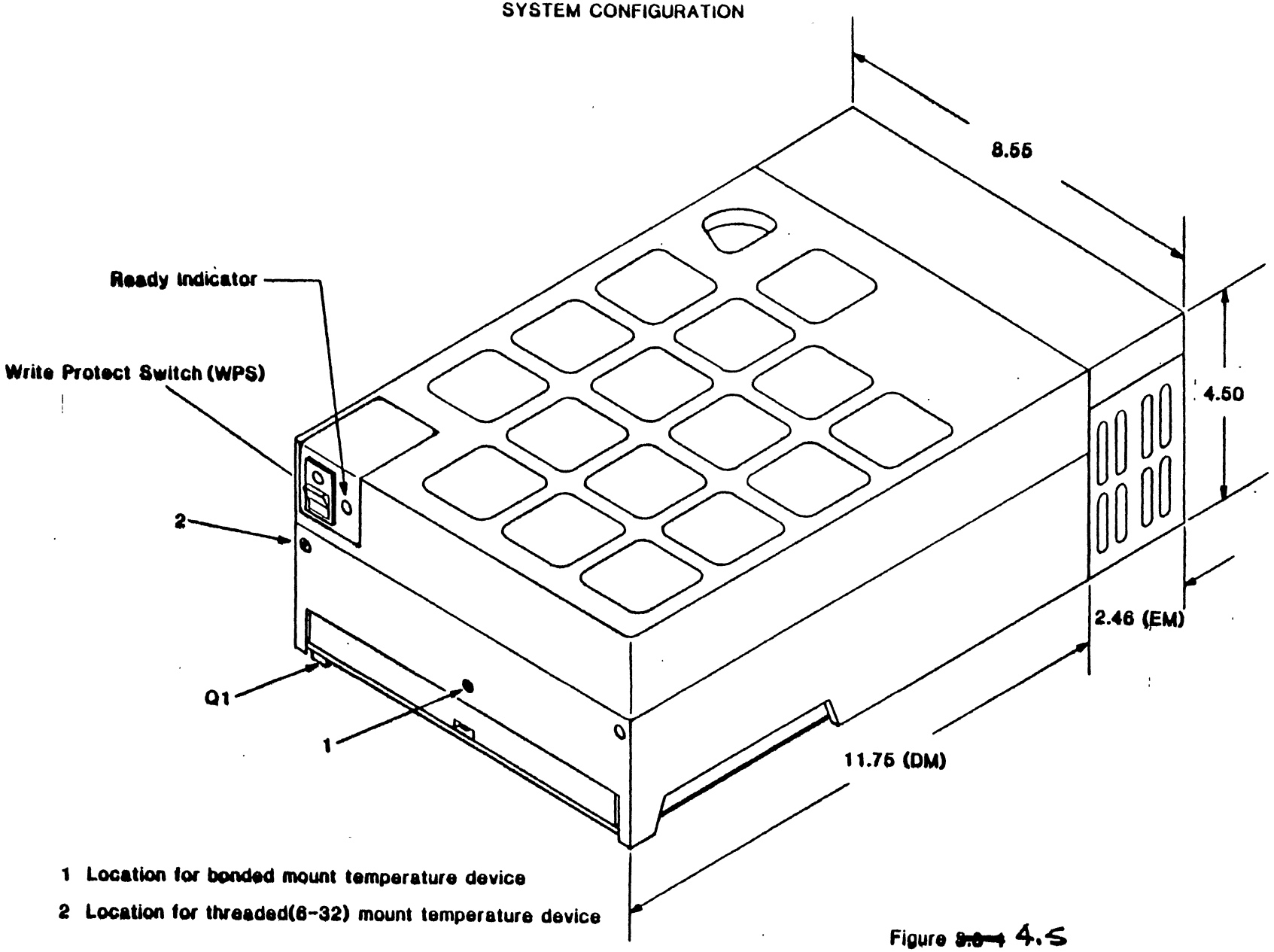

SHAPER CIRCUIT
COMPARATORS
PHASE DETECTOR
OPTICAL SWITCHES
SPINDLE MOTOR
POWER AMPLIFIER
DRIVER CIRCUITS
CURRENT LIMITER
WRITE PROTECT SWITCH
TEMP
R/W
HEAD CHIP
STEPPER MOTOR
STEPPER DRIVE
INDEX
SPINDLE REFERENCE
POWER 24±8
TEMP SENSE
WRITE CURRENT
WP SWITCH
FAULT
WRITE SELECT
HEAD SELECT
STEPPER CONTROL
DX / DY
-6V
+6V
DISK MODULE (DM)
8 CONDUCTOR POWER CABLE
MOTHER BOARD
— POWER CONNECTOR AND POWER REGULATORS (+12V, -6V)
— CARD CONNECTORS AND DM I/O
CONTROL BOARD
— FAULT LOGIC; NRZ TO MFM
— WRITE PRE-COMP
— CRYSTAL REF CLOCK; A/D CONVERT
— WRITE CURRENT DAC
DATA RECOVERY
— PHASE-LOCKED LOOP
— READ WINDOW GEN.
— MFM TO NRZ
— EARLY / LATE STROBE
(ANSI) INTERFACE / MB BOARD
— MP, RAM, ROM, TIMERS
— LINE DRIVERS / RECEIVERS
— CONTROL REGISTERS AND I/O CONNECTOR
NRZ READ DATA
84 RET
+ 24
- 6
+ 6
GND
(HOST) ANSI X3T9/1228 CONTROLLER
ELECTRONIC MODULE (EM)

Figure 4.4

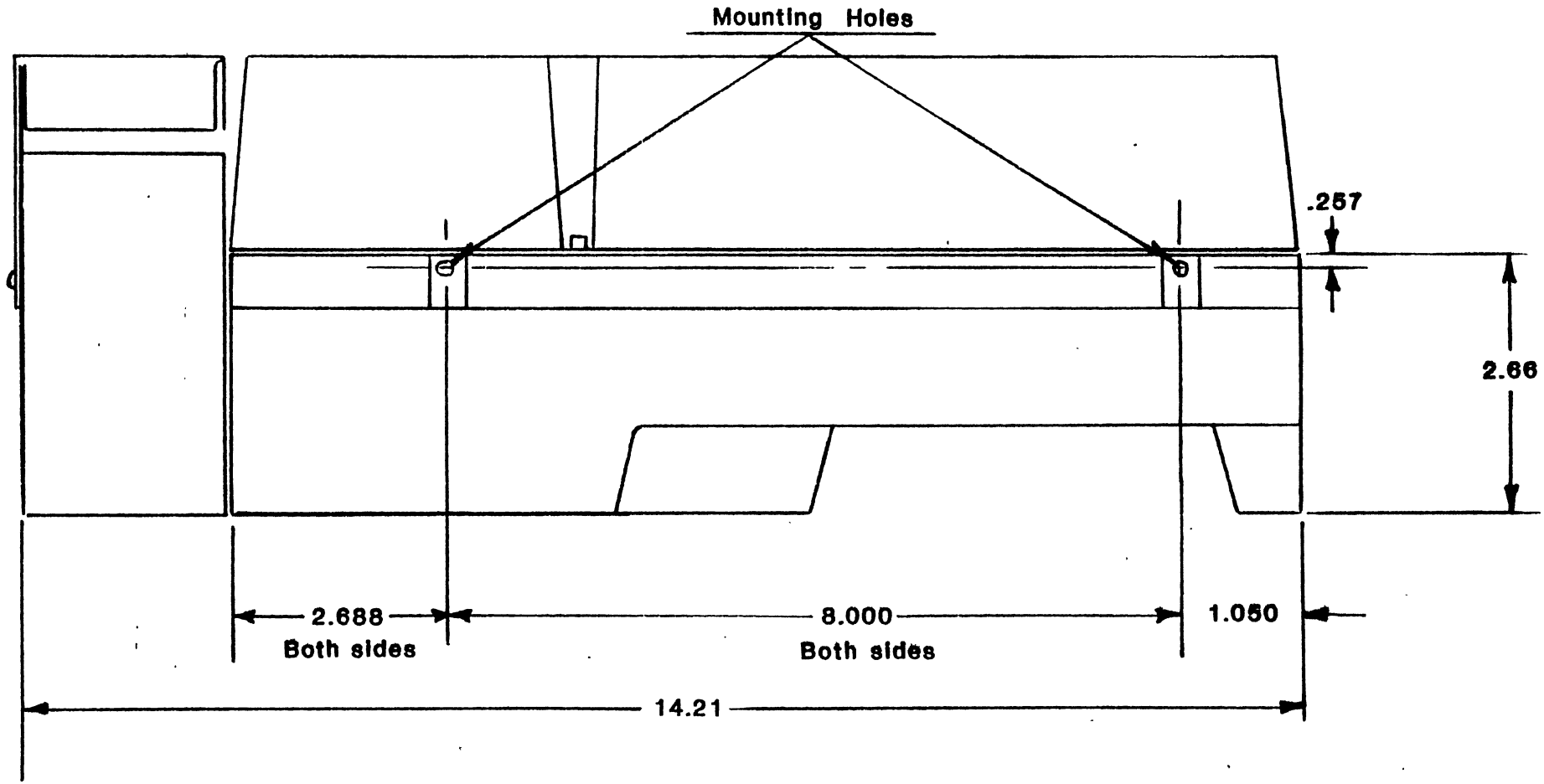


1 Location for bonded mount temperature device

2 Location for threaded(6-32) mount temperature device

Figure ~~3.0-1~~ 4.5

DRIVE MOUNTING DETAILS



1 - All mounting holes are 8-32 UNC-2B.

2 - Drives are to be electrically isolated from system chassis.

3 - All dimensions are in inches.

Figure 5.1

MODEL 8432 DISK DRIVE SPECIFICATIONS

STORAGE CAPACITY

CAPACITY (MAXIMUM)	PER MODULE	SECTORS PER TRK.	PER TRACK
Unformatted	20 Mbytes	1	17,920 bytes
Formatted 1024 bytes/sec.	18.3 Mbytes	16**	16,384 bytes
Typical, *512 bytes/sec.	17.2 Mbytes	30**	15,360 bytes
(1120) Tracks 256 bytes/sec.	14.9 Mbytes	52**	13,312 bytes
128 bytes/sec.	12.0 Mbytes	84**	10,752 bytes
Disks	2		
Data Surfaces	4		
Heads/Surface	1		
Total Tracks/Surface	280		
Total Tracks/Drive	1120		
Guaranteed Tracks/Drive	1100		
Track Density	219 Tracks Per Inch, Average		
Bit Density	8649 Bits Per Inch, Maximum		
Disk Size	210 mm, (8.27 inches)		

PERFORMANCE PARAMETERS

Track-to-Track Seek Time	18.6 ms Low to High cylinder 25.0 ms High to Low cylinder
Random Average Seek Time	65 ms
Full Stroke Seek Time	110 ms
Average Latency	9.6 mx
Rezero	See Sec. 5.4

*Default Format (See Section 9.5)

**Overhead - 84 Bytes Per Sector

TABLE 5-1

MODEL 8432 DISK DRIVE SPECIFICATIONS

PERFORMANCE PARAMETERS (Continued)	
Data Transfer Rate	933 Kbytes per Sec.
Read Error Rate (Recoverable)	1 X 10^{10} bits
Read Error Rate (Unrecoverable	1 X 10^{12} bits
Seek Errors	1 X 10^{6} seeks
Start/Stop Time	60 seconds maximum
Interface	ANSI X3T9/1226
PHYSICAL PARAMETERS	
Size	
Height	4.51 inches, (114,6 mm)
Width	8.55 inches, (217,2 mm)
Length	14.21 inches, (360,9 mm)
Weight	17 pounds, (7,65 kg)
Mounting (Fig. 5-1)	Horizontal, (PCB up or down) or side(not on end)
Media	Particulate oxide
Air Filter	0.3 micron, absolute
Head Positioner	Stepper motor drive, band-actuated, rotary
Spindle Motor	Brushless DC
Spindle Speed	3125 rpm $\pm$ 0.05%
Mechanical Shock & Vibration	
Operating (3 Axis)	0.5G's (sinusoidal 5-2000 HZ)
Shipping (Storage)	0.5G's

TABLE 5-1

MODEL 8432 DISK DRIVE SPECIFICATIONS

RELIABILITY PARAMETERS

MTBF System	10,000 hours
MTBF Elements in Clean Air Enclosure	25,000 hours
MTTR	0.5 hours
Design Life	10 Years
Scheduled Maintenance	None

POWER REQUIREMENTS (See paragraph 5.1, if 40°C operating environment is exceeded)

External DC only* (Worst Case Including Start-up Surge) (Fig. 3.6-3 for power connection)	+24V ± 10% @ 3.5A +5V ± 5% @ 2.7A -5V ± 5% @ 0.5A	Includes Noise & Ripple
Running Power Intake (Including Worst Case Seeking)	80 Watts	
Voltage Ripple Tolerance		
+24V	1 Volt (P-P) Max.	
± 5V	100MV (P-P) Max.	

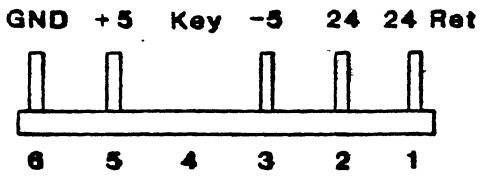
ENVIRONMENTAL REQUIREMENTS

Operating Temperature	See Paragraph 5.2
Operating Humidity	10% to 80% RH (Non-condensing)
Storage Temperature	-40° to 158°F (-40° to 70°C)
Storage Humidity	5% to 95% RH (Non-condensing)
OPERATING ALTITUDE	500 feet, (152 m), below sea level to 8,500 feet, (2591 m), above sea level

*External supplies must be overvoltage protected to prevent damage to voltage sensitive components in the drive.

TABLE 5-1

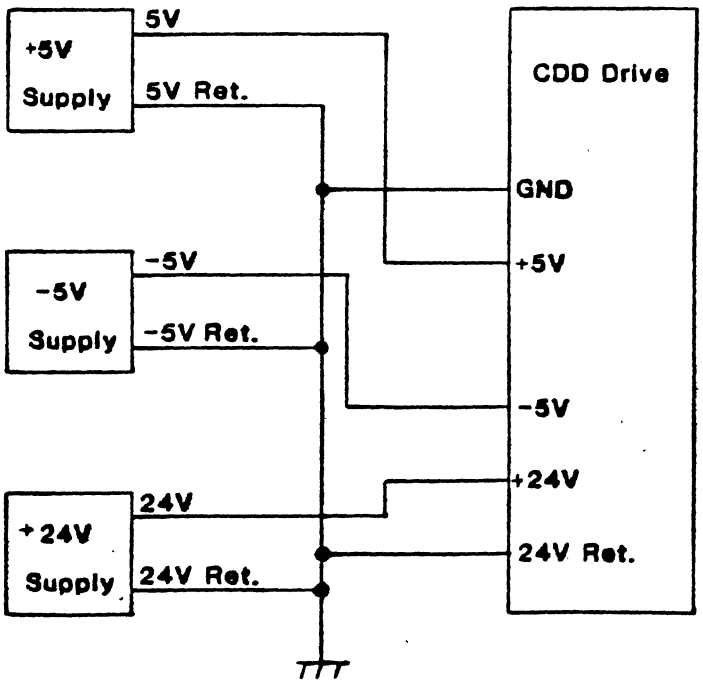
POWER CONNECTOR



Power Connector Looking at the Back of the Disk Drive

Figure 5.3 a

POWER CONNECTION DIAGRAM



Power Supply Returns are to be Tied Together at the Supplies

Figure 5.3 b

In conjunction with an internal diagnostic, the Rezero Command will be executed in two ways.

Cylinder 0 Location - whenever the microprocessor is unsure of the heads physical location, a deliberate slow speed seek to Cylinder Zero will be performed. This procedure will be used on Power Up, seek from Landing Zone, recovery from a Spin Control Command, Selective Reset, deassertion of Port Enable and Power or Spindle fault. The entire Rezero procedure will require about 13 sec.

Error Recovery - For purposes other than Cylinder 0 determination, such as error recovery routines, a modified high speed, Rezero seek will be used. This seek will require 0.6 to 1.0 seconds depending upon the starting position of the head. The ANSI Command Code 04 will always be used, with the microprocessor and internal diagnostics determining the execution mode.

6.0 INTERFACE

6.1 The Model 8432 Disk Drive interface conforms to ANSI Standard X3T9/1226 for 8-inch Rigid Disk Drives. All control, status, timing and data communications between the controller (host system) and up to eight Model 8432 Disk Drives are via a standard 50 conductor I/0 cable. Line names, cable structure, and cable pin assignments for this I/0 cable are shown in Table 2-3 of ANSI Standard.

All input control and output response signals are TTL compatible. Industry standard line transmitters and single-ended receivers are used to provide a transmission system suitable for long-line operation in an electrically noisy environment (for circuit details refer to ANSI Standard.)

Data and reference clock are transmitted and received with differential line drivers and receivers.

For a detailed description of the interface signals see ANSI Standard X3T9/1226.

6.2 Detailed in the following section will be exceptions, clarifications or additions to the ANSI Standard interface.

6.2.1 Initial State

Conditions of initial state in addition to ANSI Standard are:

a. The spindle will start spinning, if it previously had not been doing so.
b. The sector format is set to its initial (default) configuration. (See Section 9.5)
c. The heads are moved to cylinder zero.

6.2.2 Index

Index is valid at all times, if the drive is selected and ready.

6.2.3 Sector

Sector pulses are valid at all times, if the drive is selected and ready.

6.2.4 Read/Write Signals

6.2.4.1 Write Clock

Jumper options are provided in the drive to phase write clock to write data to account for variations in cable and logic propagation delays. Jumper position "W2" is the normal position. See Figure 8.9.

6.2.4.2 Write Gate

De-assertion of Write Gate must be delayed for 2 bytes after the host transmits the last byte of Write Data to insure all Write Data is written on the disk. This is necessary to purge the serial registers of the write encode and precompensation circuitry. See Figure 8.9 which illustrates Write Gate Delay.

7.0 COMMAND STRUCTURE

7.1 Outlined in this section are exceptions, clarifications and additions to the ANSI Standard Interface.

7.2.1 Optional Device Attribute Functions not Supported:

Attribute	Hex Number
Revision ID	03
Encoding Method #1	30
Preamble #1 Length	31
Preamble #1 Pattern	32
Sync #1 Pattern	33
Postamble #1 Length	34
Postamble #1 Pattern	35
Gap #1 Length	36
Gap #1 Pattern	37
Encoding Method #2	40
Preamble #2	41
Preamble #2 Pattern	42
Sync #2 Pattern	43
Postamble #2 Length	44
Postamble #2 Pattern	45
Gap #2 Length	46
Gap #2 Pattern	47

7.3 Commands with Parameters Out.

7.3.1 Mandatory Commands

All mandatory commands are implemented as defined in the ANSI Standard

7.3.2 Optional Commands

All optional commands are supported except for those listed below:

Function	Hex Command Code
Select Fixed Head	52
Offset Control	54

Issuance of an unsupported command will result in an error.

7.4 Commands with Parameters In

7.4.1 Mandatory Commands

All mandatory commands are implemented as defined in the ANSI Standard.

7.4.2 Optional Commands

All optional commands are supported except for those listed below:

Function	Hex Command Code
Reserve Device	12
Release Device	13

Issuance of an unsupported command will result in an error.

7.5 Vendor Unique Commands

One vendor unique command is implemented.

Function	Hex Command Code	Parameter In	Temp °F
Report Drive Internal Temp	30	00	Below 75
		01	76-80
		02	81-85
		03	86-90
		04	91-95
		05	96-100
		06	101-105
		07	106-110
		08	111-115
		09	116-120
		0A	121-125

Function	Hex Command Code	Parameter In	Temp °F
		0B	126-130
		0C	131-135
		0D	136-140
		0E	141-145
		0F	Over 145 (Unsafe)

This command may be used by the host to monitor drive temperature. Power to the drive should be shut down if the Parameter In of 0F is reported as this temperature exceeds the drive safe operating limitations.

7.6 Device Attribute Commands

The device attribute command responses are listed in Table 7.6.

7.7 Sense Byte and Status Reporting

7.7.1 General Status - As defined by ANSI X3T9/1226

7.7.2 Sense Byte 1

Bits 6 and 7 are not used.

7.7.1.1 Power Fault

This bit will be set for the following conditions:

Voltage	Over Voltage	Under Voltage
+5V	Yes	Yes
-5V	Yes	Yes
+24V	No	Yes
+12	No	Yes
-12	No	Yes
+6	No	Yes
-4	No	Yes

This bit will be reset by the Clear Fault Command, if the fault has been removed.

7.7.3 Sense Byte 2

Bits 2, 3, 4, and 7 are not used.

7.7.4 Command Busy/Not Ready Relationships - See Table 7.7 for details.

DEVICE ATTRIBUTE

ATTRIBUTE	NO	PARAMETER	DEFAULT	TYPE	CMDs TO* MODIFY
User ID	00	User Defined	00	R/W	50,51
Model ID High	01	MSB of CDD Model #	84	R/O	
Model ID Low	02	LSB of CDD Model #	32		
Device Bype ID	0D	Non-Removable Disk Drive	01	R/O	
Table Modification	0E	Action Dependent	40	R/W	50,51
Table ID	0F	ANSI Compatible Indicator For Device Attributes	01	R/O	
Bytes per Track High	10	MSB of # of Bytes	00	R/O	
Bytes per Track Med	11	MedSB of # of Bytes	46	R/O	
Bytes per Track Low	12	LSB of # of Bytes	00	R/O	
Bytes per Sec. High	13	MSB of # of Bytes	00	R/O	56,16
Bytes per Sec. Med	14	MedSB of # of Bytes	02	R/O	57,16
Bytes per Sec. Low	15	LSB of # of Bytes	54	R/O	58,16
Sec. Pulses per Trk High	16	MSB of # of Sec Pulses	00	R/O	59,16
Sec. Pulses per Trk Med	17	MedSB of # of Sec Pulses	00	R/O	5A,16
Sec. Pulses per Trk Low	18	LSB of # of Sec Pulses	1D	R/O	5B,16
Sectoring Method	19	Sectoring Method	01	R/O	
Number of Cyl. High	20	MSB of # of Cyl.	01	R/O	
Number of Cyl. Low	21	LSB of # of Cyl.	18	R/O	
Number of Mov Heads	22	Number of Heads	04	R/O	
Number of Fixed Heads	23	Number of Heads	00	R/O	
Head Select Mode	24	Head Select Mode	00	R/O	

R/W = Read/Write . R/O = Read Only

NOTE: ALL UNUSED BITS IN PARAMETERS MUST BE ZEROS

*All Attributes are read with the 50, 10 command sequence.

TABLE 7.6

COMMAND BUSY/NOT READY RELATIONSHIPS

FUNCTION	BUSY SIGNAL	NOT READY STATUS	BUSY EXECUTING STATUS
No Power	0	N/A	N/A
Motor Stopped	0	1	0
Idle Condition	0	0	0
Power Fault ***	0	1	0
R/W Operation	0 **	0	0
In Landing Zone	0	1	0
Any Time Dependent CMD*	1	N/A	N/A

* During the execution of any time Dependent Command the Busy line is set, so that status communication is not possible.

** WARNING: A command transfer during a read or write operation may result in data errors.

*** Status is as indicated for non-catastrophic power faults. Catastrophic power faults result in undefined state for the three signals.

TABLE 7.7

8.0 TIMING REQUIREMENTS

8.1 Select Timing Sequence - See Figure 5-1 of ANSI Standard.

8.2 Attention Timing Sequence - See Figure 5-2 of ANSI Standard.

8.3 Command/Parameter Out Sequence - See Figure 5-3 of ANSI Standard.

8.4 Command/Parameter In Sequence - See Figure 5-4 of ANSI Standard.

8.5 Index/Sector Timing (Hard Sectoring)

The drive will provide hard sectoring for all combinations except for 2 and 3 sectors per track. Because of hardware limitations, these two formats cannot be implemented. However, single sector (Index only, track mode) and sectoring formats of 4 or more sectors may be implemented. See Figure 5-5 of ANSI Standard.

8.6 Reference Clock Timing - See Figure 8.7.

8.7 Read Timing - See Figure 8.8.

8.8 Write Timing - See Figure 8.9.

9.0 FORMATTING GUIDELINES

Since the Model 8432 Disk Drive does not utilize a servo track, sector pulses are not generated directly from readback data. Rather, they are generated by a countdown chain driven by the same crystal controlled clock that controls spindle motor speed. This method of generating sector pulses results in a format efficiency that is lower than the format efficiencies typical of drives using servo track derived sector pulses. A factor called "Sector Pulse Tolerance" must be taken into account.

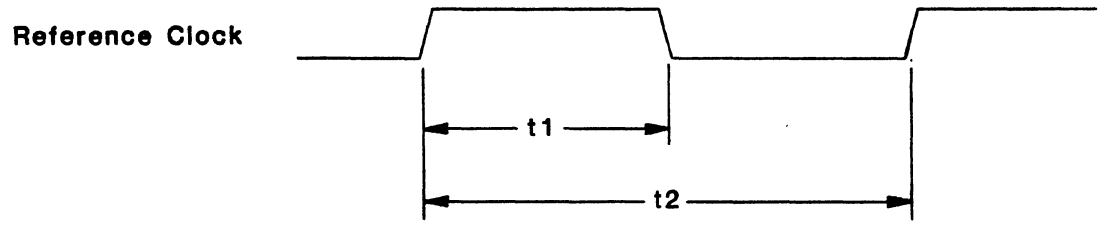
The format defined in this section is a guideline, not a mandatory requirement. Variations from this guideline are permissable with Write Gate Delay, the Effective Inter-Sector Gap and Read PLO Synchronization times defined as minimums.

9.1 Boundary Conditions

9.1.1 Spindle Speed = 3125 + .05% RPM
= 19.20 ms/rev. $\pm$ .05%

9.1.2 Data Rate = 7.46667 megabits/sec
= 133.92857 ns/bit
= 1.0714285 us/byte

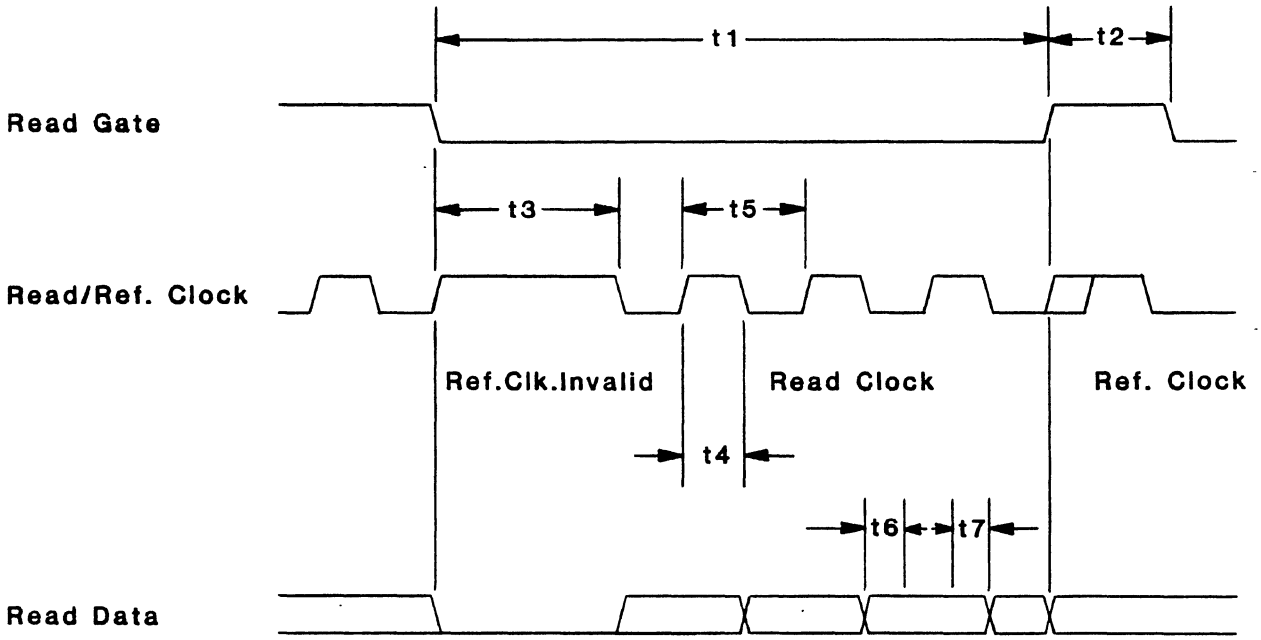
REFERENCE CLOCK TIMING



Label	Description	Min.	Max.	Units
t1	Reference Clock "ON" Time	54	80	nanoseconds
t2	Reference Clock period (Read)	127	141	nanoseconds
	Reference Clock Period (Write)	133.8	134.0	nanoseconds
tp	Nominal Reference Clock Period	133.9		nanoseconds

Figure 8.7

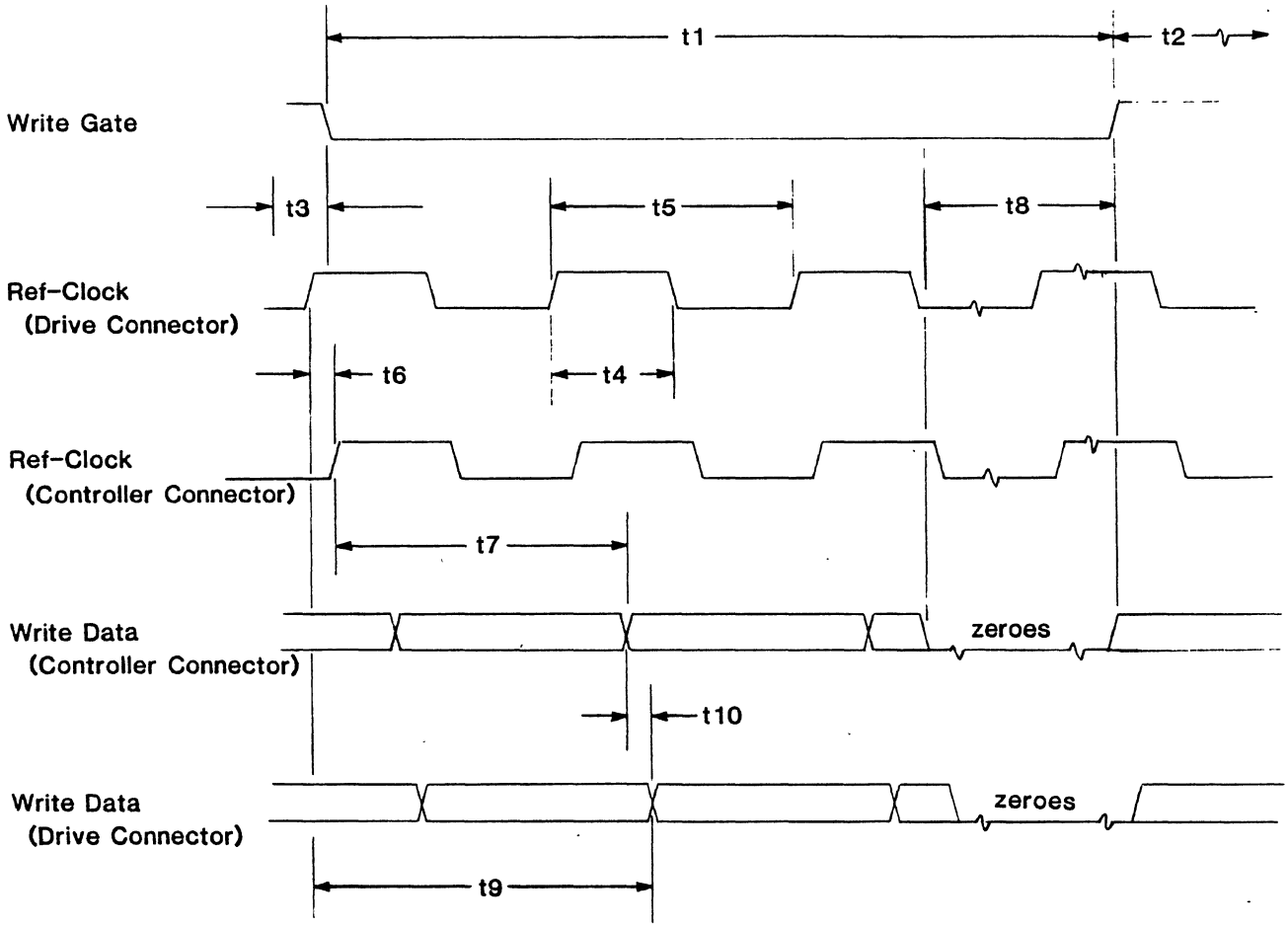
READ TIMING



Label	Description	Min.	Max.	Units
t1	Read Gate active	0	---	nanoseconds
t2	Read Gate inactive	268	---	nanoseconds
t3	Read Gate to valid Read Data and Read Clock	8	---	microseconds
t4	Read Clock "ON" time	54	80	nanoseconds
t5	Read Clock period	127	141	nanoseconds
t6	Read Data setup time	33	---	nanoseconds
t7	Read Data hold time	33	---	nanoseconds
tp	Nominal Reference Clock period	133.9		nanoseconds

Figure 8.8

WRITE TIMING



Label	Description	Min.	Typ.	Max.	Units
t1	Write Gate Active	0	---	---	nanoseconds
t2	Write Gate Inactive	0	---	---	nanoseconds
t3	Write Clock Valid	133.8	---	2142	nanoseconds
t4	Write Clock "ON" Time	66		68	nanoseconds
t5	Write Clock Period	133.8	---	134.0	nanoseconds
t6	Cable Delay (1.5 ns/ft)	---	---	15	
t7	Controller Data Clocking	92	---	146	
t8	Write Gate Delay	2142	---	---	nanoseconds
t9	Total Data Delay (Including Cable Delay)	110	---	176	nanoseconds
t10	Cable Delay (1.5 ns/ft)		---	15	nanoseconds
tp	Nominal Ref-Clock Period		133.9		nanoseconds

Figure 8.9

NOTE: Only nominal values shown.

9.1.3 Total number of bytes = 17,920 per track, unformatted

9.1.4 Index Pulse Jitter = $\pm$ 1 us

9.1.5 PLO Lockup Time = 8 us

9.1.6 Read-to-Write Recovery Time = 5 us

9.1.7 From 9.1.1 and 9.1.4 Sector Pulse Tolerance Equals:

$$\pm 1 \text{ us} \pm \frac{.05 \times 19200 \text{ us}}{100}$$

$$= \pm 1 \text{ us} \pm 9.6 \text{ us}$$

$$= \pm 10.6 \text{ us}$$

9.2 Format Calculations

This discussion will refer to the format shown in Figure 9.3.1.

9.2.1 Effective Inter-Sector Gap

The required length of the part of the format, which is made up of the Postamble and Preamble 1, is determined by the following factors:

A. Sector Pulse Tolerance, which affects both Postamble and Preamble.

B. PLO Lockup Time, which affects only Preamble 1.

C. Write-to-Read Recovery Time, which affects only the Postamble.

From the calculations shown in 9.1.7, Sector Pulse Tolerance is $\pm$ 10.6 us. An examination of how the Sector Pulse will vary in time during readback (relative to where it was, in time, during formatting) indicates that 2X this value is required to insure that the Sector Pulse will not, under worst conditions, be detected outside of the Effective Inter-Sector Gap. This Value is:

$\pm$ 21.2 us

Which yields a total time of:

42.4 us

Combining this value with PLO Lockup Time and Write-to-Read Recovery Time, the total length of the Effective Inter-Sector Gap is:

= 42.4 us + 8 us + 5 us

= 55.4 us = 52 bytes minimum

Observing Figure 9.3.1, the 54 bytes is split with 25 bytes of Postamble and 29 bytes of Preamble.

The length of the Postamble portion of the Effective Inter-Sector Gap must contain the following:

2 X Sector Pulse Tolerance + Write-to-Read Recovery

= (2 X 10.6 us) + 5 us

= 26.2 us = 24 bytes minimum

The length of the Preamble portion of the Effective Inter-Sector Gap must contain the following:

2 X Sector Tolerance + PLO Recovery

= (2 X 10.6 us) + 8 us

= 29.6 us = 28 bytes minimum

During formatting, the Effective Inter-Sector Gap is written in a continuous manner as 54 bytes, rather than in two parts. This is with the exception of the first sector after Index, in which only the Preamble 1 length of 28 bytes is written.

9.2.2 Write Turn-on Guard

This time is required to allow for write current rise time, controller decision making after header verification and 1 byte of margin.

9.2.3 Write Gate Delay

This delay is necessary to insure that all write data transmitted by the controller (host) is written on the disk. The Write data pre-compensation circuitry provides serial storage, and this must be purged by two bytes of clocks after the last data byte from the controller. During this time, the host should send data zeroes so that the serial register will begin the next Write (preamble) with zeroes.

9.2.4 Write Turn-Off Guard

This time is required to account for write current turn-off time.

9.2.5 Length of Preamble 2

Preamble 2 is to re-establish PLO Lockup just before reading data. Therefore, its length is:

= 8 us

= 8 bytes

9.2.6 Total Sector Length

From the above calculations and referring to Figure 9.3.1, total sector length is:

84 bytes of overhead + data

Some variations around this minimum format are user optional.

9.3 Minimum Format

9.3.1 Initialize Mode (Reformat) (Figure 9.3-1)

The minimum, format for initialize should contain the following:

Function	Bytes	Data
Preamble 1	29	Zeroes
Address Sync	1	Other than all zeroes pattern.
Address	4	XXXX
ECC	4	XXXX
Preamble 2	13	Zeroes
Data Sync	1	Other than all zeroes pattern.
Data	N	XXX
ECC	4	XX
Write Delay	2	Zeroes
R/W Splice	1	Zeroes
Postamble	25	Zeroes

Preamble 2 is 13 bytes to account for 4 bytes (Write Turn-On Guard) and 9 bytes of actual Preamble 2 necessary for read PLO sync up.

The Postamble is 28 bytes which accounts for 2 bytes (Write Gate Delay), 1 byte (Write Turn-Off Guard) and 25 bytes of actual Postamble.

The Write Gate Delay at the end of the sector is required in interleave format only. In sequential format this delay is after the last sector.

9.3.2 Read Mode (Figure 9.3.2)

The Read Mode format is shown to illustrate the Read Gate timing. Read Gate should be de-asserted after address ECC for 6 bytes and re-asserted during Preamble 2 to provide time for read PLO lock-up. The Read Gate is de-asserted during Write-Turn-On Guard to prevent the read PLO from being driven outside of its capture range when reading through a write splice.

9.3.3 Write Data Mode (Figure 9.3.3)

In the Write Data Mode Write Gate must be delayed two bytes after Data ECC to insure that all of the host write data is clocked out of the write pre-compensation circuitry and onto the disk. During this two byte delay the host should send zeroes on the Write Data line.

9.4 Number of Sector/Track

Figure 9.4.1 is a chart giving the maximum number of sectors for various sizes of the data field and 84 bytes of overhead/sector. The total unformatted byte count/track is 17,920. Also shown is the format efficiency for each data field value and the "End of Track Gap." See paragraph 8.5 for limitations on the number of sectors per track.

The relationships between the columns in the chart are:

A. Data Bytes/Sector - Chosen

B. Overhead Bytes/Sector - Given

C. Maximum Number of Sectors equals the whole number portion of:

$$\frac{17920}{\text{(No. of Data Bytes + (No. of Overhead Bytes)}}$$

D. Number of bytes remainder is equal to:

17920 - (No. of Sectors X (Data Bytes + Overhead Bytes))

E. Format Efficiency, in percentile, is equal to:

$$\frac{\text{No. of Sectors X Data Bytes per Sector X 100}}{17920}$$

9.5 Default Format

Each Model 8432 Disk Drive is programmed with a default sector format.

Number of sectors/track 30 (29 sector pulses & index)

Number of bytes/sector 596
(Data and Overhead = 512 bytes + 84 bytes)

The above information is contained in the microprocessor memory such that when power is first applied to the drive, it will default to the above values. This implies that there will be 29 sector pulses, plus the index pulse (for a total of 30 sectors), per revolution, with 596 bytes between sector pulses and 636 bytes nominal between the last sector pulse and the index pulse. This format provides for 512 data bytes and 84 overhead bytes. The default format has the same overhead as the minimum format of Section 9.3.

If a format different from this default format is desired, command codes 56 through 5B and 16 may be used to set up any desired format. It should be noted that values given to the drive using these commands are not checked by the drive to ensure that the specified number of bytes per sector fit with the number of sectors per track.

See Table 7.6 for Attributes used in the default format.

MAXIMUM NUMBER OF SECTORS FOR VARIOUS DATA FIELD VALUES*

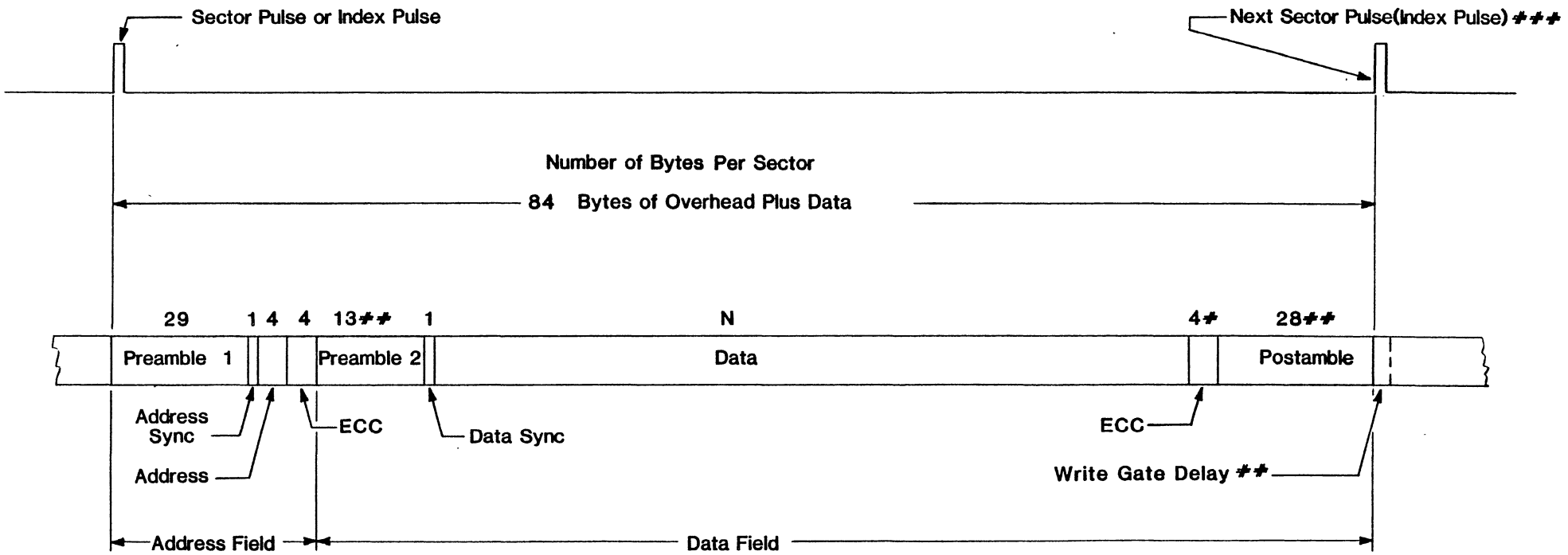
DATA BYTES PER SECTOR	MAX. NUMBER OF SECTORS	NO. OF BYTES REMAINDER **	FORMAT EFFICIENCY	FORMATTED CAPACITY/TRACK
64	121	12	43%	7,744
128	84	112	60%	10,752
256	52	240	74%	13,312
512	30	40	86%	15,360
1024	16	192	91%	16,384
2048	8	864	91%	16,384

*Overhead per Sector = 84 Bytes

**Number of Bytes Remainder = End of Track Gap
(See Figure 9.4-2)

FIGURE 9.4-1

MINIMUM FORMAT - INITIALIZE MODE



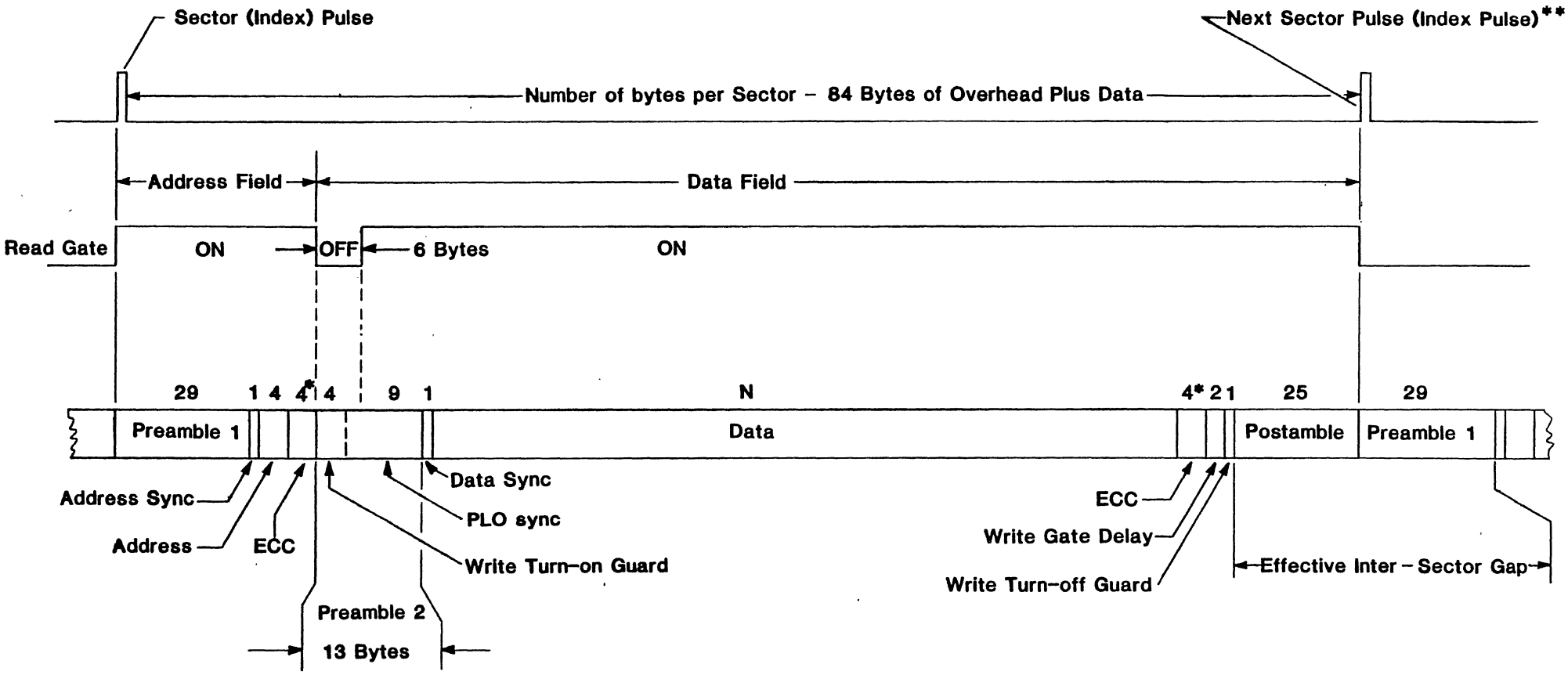
* If CRC is used in this location, reduce overhead by 2 bytes.

** See Paragraph 9.3.1

*** If this pulse is Index, then the preceding Postamble will contain the remaining overhead bytes of this track. The Postamble should continue to the net sector (Index) pulse.

Figure 9.3-1

MINIMUM FORMAT – READ MODE

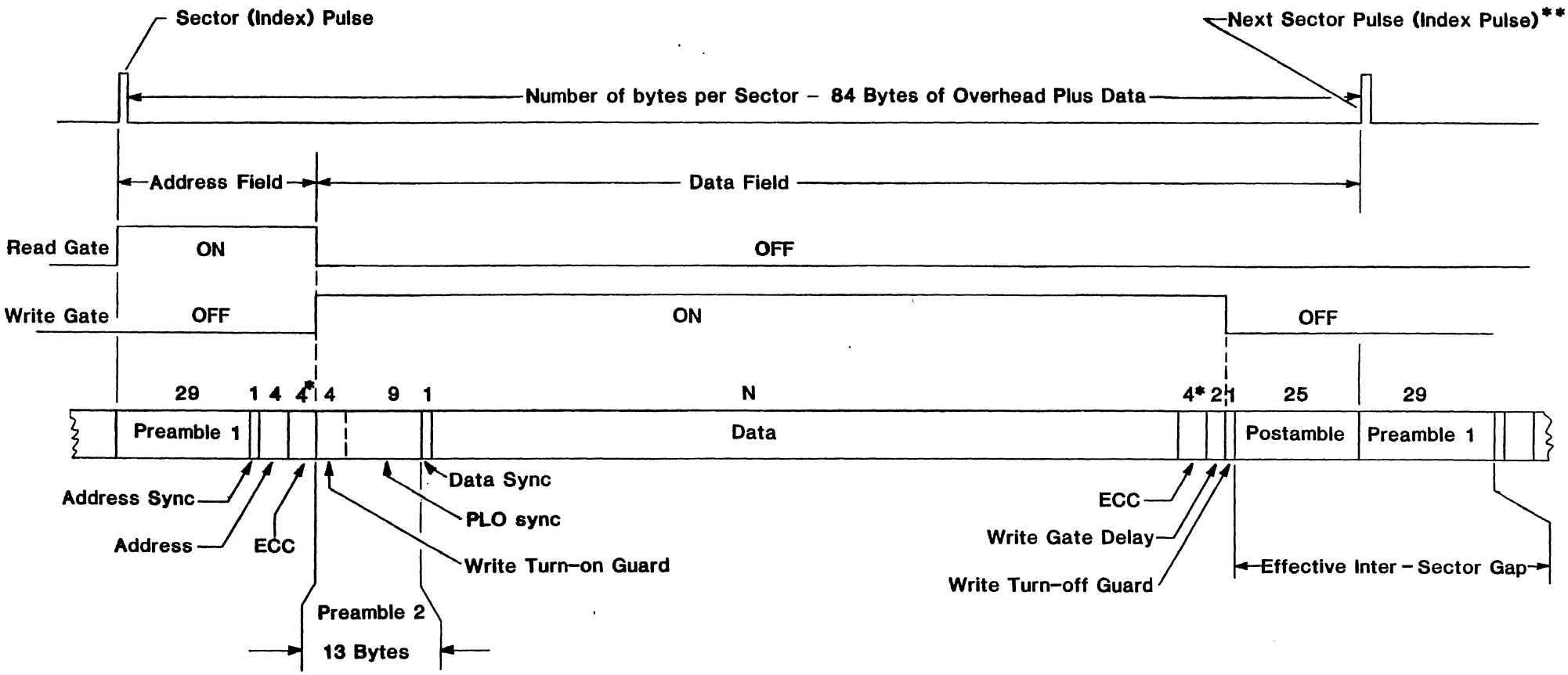


* If CRC is used in this location, reduce overhead by two bytes.

** If this pulse is Index, then the preceding Postamble will contain the remaining overhead bytes for this track.

Figure 9.3–2

MINIMUM FORMAT - WRITE MODE



* If CRC is used in this location, reduce overhead by two bytes.

** If this pulse is Index, then the preceding Postamble will contain the remaining overhead bytes for this track.

Figure 9.3-3